

Lattice™

Lattice Data Book 1994

Lattice Data Book



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Lattice™

pLSI and ispLSI Product Index

PART #	Pins	Density (PLD Gates)	Tpd (ns)	Fmax (MHz)	Icc (mA)	Description	Page
pLSI / ispLSI 1016	44	2000	10, 12, 15, 20	110, 90, 80, 60	150	64 Macrocell High-Density PLD	2-61
pLSI / ispLSI 1024	68	4000	12, 15, 20	90, 80, 60	190	96 Macrocell High-Density PLD	2-81
pLSI / ispLSI 1032	84	6000	12, 15, 20	90, 80, 60	195	128 Macrocell High-Density PLD	2-97
pLSI / ispLSI 1048	120	8000	15, 18, 24	80, 70, 50	235	192 Macrocell High-Density PLD	2-117
pLSI / ispLSI 1048C	128	8000	18, 24	70, 50	235	192 Macrocell High-Density PLD	2-133
pLSI / ispLSI 2032	44	1000	7.5, 10, 15	135, 110, 80	—	32 Macrocell High-Density PLD	2-151
pLSI / ispLSI 3256	160	11000	15, 17, 23	80, 70, 50	—	256 Macrocell High-Density PLD	2-169

GAL Product Index

PART #	Pins	Tpd (ns)	Fmax (MHz)	Icc (mA)	I _{sb} (μA)	Description	Page
GAL16V8	20	5, 7.5, 10, 15, 25	166, 100, 62.5, 41.6	55, 90, 115	—	Universal 20-Pin PLD	3-5
GAL16V8Z/ZD	20	12, 15	83.3, 62.5	55	100	Zero-Power 20-Pin PLD	3-29
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In-System Programmable Generic Digital Switch Product Index

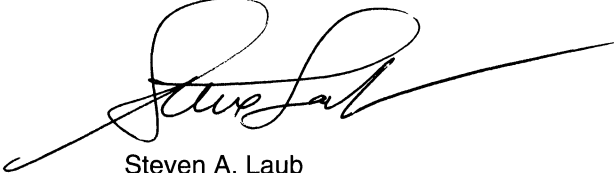
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ispGDS18	24	7.5	50	40	9 x 9 Programmable Switch Matrix	4-5
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Thank you for your interest in Lattice Semiconductor's programmable logic products. Lattice offers the world's highest performance and broadest product line of low density and high density CMOS PLDs.

This data book includes our industry standard GAL® product line and our new High-Density PLDs, the pLSI® and ispLSI™ 1000, 2000, and 3000 families. The pLSI and ispLSI families combine the performance and ease of use of PLDs with the density and flexibility of FPGAs.

Lattice Semiconductor, the worldwide leader in E²CMOS PLDs, is committed to supplying you with the optimal solution to all of your programmable logic requirements.

Sincerely,



Steven A. Laub
Vice President and General Manager



Lattice Semiconductor Corporation

1994 Data Book





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Introduction

Background

Lattice Semiconductor Corporation, founded in 1983 and based in Hillsboro, Oregon, has completed its tenth year of supplying innovative solutions for the high performance system design needs of its customers. Through its pioneering efforts at applying E²CMOS[®] technology to programmable logic, Lattice has established the GAL[®] family of products as the industry standard worldwide. With the introduction of the high-density programmable Large Scale Integration (pLSI[®]) devices and in-system programmable Large Scale Integration (ispLSI[™]) devices, Lattice has become the world's largest supplier of low-density CMOS PLDs and the fastest growing supplier of high-density CMOS PLDs.

Lattice has recently introduced two new low-density in-system programmable devices: the ispGAL22V10 and ispGDS[™]. The ispGAL22V10 brings on-the-fly system logic reconfigurability to the industry standard GAL22V10. The ispGDS (in-system programmable Generic Digital Switch) family further extends Lattice's programmable technology beyond logic to board interconnect and signal routing. ispGDS opens new possibilities for system designers and is just the first of a number of application specific programmable solutions which will be addressed by Lattice in the future.

The Lattice Advantage

Time-to-Market

E²CMOS PLDs enable system designers to meet ever-shrinking time-to-market constraints while avoiding the significant development costs, lead times and dedicated inventories associated with traditional ASIC and bipolar PLD solutions.

Flexibility

Programmable and reprogrammable devices enable fast and easy modifications to system designs.

Product Differentiation

Programmable devices support end-product differentiation through proprietary feature enhancements. This is particularly true when a system utilizes the non-volatile ISP[™] (In-System Programmable) technology pioneered by Lattice.

Inventory Reduction

A single standard part type can be used in multiple, diverse applications. Just 5 GAL architectures replace virtually all bipolar PAL[®] architectures (see figure 1).

Products

The Lattice PLD product offering can be segmented into two strategic product thrusts:

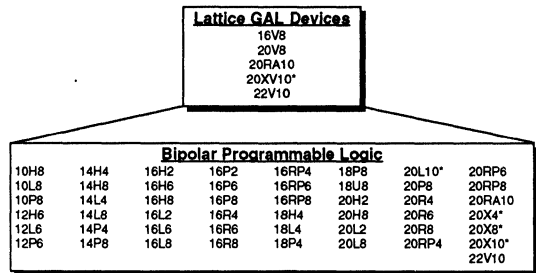
Low Density: GAL Family

- 100 - 1,000 Gates
- The Highest Performance PLDs from any Supplier
- Superior Replacements for Bipolar and CMOS PLD Architectures
- E²CMOS Low-Power, Quality and Reliability
- Broadest Range of PLD Architectures Offering Features not Available in other PLDs

High Density: pLSI and ispLSI Families

- 1,000 - 14,000 Gates (World's Largest)
- World's Fastest High-Density PLDs (HDPLDs)
- Superior HDPLD Architecture (Flexible, Predictable Performance)
- Pioneering Non-volatile In-System Programmability (ISP)
- Range of Effective Development Tool Options

Figure 1. Five GAL devices replace virtually all bipolar PAL devices.



* GAL20XV10 replaces 20L10, 20X10, 20X8 and 20X4

Introduction

Lattice Product Features

There are three fundamental features which Lattice PLDs share: E²CMOS technology, performance leadership and innovation.

E²CMOS Technology

All GAL, pLSI and ispLSI devices are manufactured using Lattice's proprietary high-speed UltraMOS[®] E²CMOS technology. Lattice is unique among "fab-less" companies in that the process technology development is actually done by Lattice. UltraMOS technology successfully combines the best features of CMOS and NMOS process technology to yield PLDs with the following key features:

- Industry Leading Performance
- High Logic Densities
- Low Power Consumption
- Non-Volatile, In-System Programmability
- Fast Erase and Reprogram Times
- 100% Full Parametric Testability
- 100% Programming and Functional Yields

Performance Leadership

Lattice continues its long track record of producing the fastest CMOS PLDs in the market. These industry-leading high-performance products are typically available to the market months ahead of any other PLD supplier. As a result, Lattice customers have always been able to take full advantage of next generation microprocessor speeds and bring out industry leading end products of their own, thus fueling their own success.

While speed continues to be a top priority, Lattice has also introduced PLD families which address other logic design concerns such as low power ("Zero-Power" GAL16/20V8Z and GAL16/20V8ZD), high output drive (GAL16/20VP8) and logic density (GAL26CV12).

Innovation

The third, and perhaps the most important attribute of Lattice's products is technology and architectural innovation. Lattice's most far-reaching innovation may have been the decision in 1984 to combine E²CMOS technology with the PLD architecture when all other PLD suppliers were offering UV erasable EPROM technology. This marriage yielded the GAL product family - the "1st Revolution in PLD design."

Lattice innovation also started the "2nd Revolution in PLD design" with the introduction of the first non-volatile

in-system programmable high-density PLD family — ispLSI, as well as the ispGAL22V10 and ispGDS.

The ISP concept, and the ispLSI, ispGAL and ispGDS families in particular, dramatically impact system development and manufacturing. Lattice ISP solutions deliver:

Effortless Prototyping: Design iterations can be downloaded directly to the ISP device soldered onto the prototype board.

Reconfigurable Systems: A single generic board can be "personalized" to one of many system configurations at final board level test.

Simplified Manufacturing: Eliminates all stand-alone programming steps. Device programming can be done as part of board-level testing. The result is no misprogrammed devices, no inventory headaches keeping track of patterned devices, and no PLD rework costs.

No More Bent Leads: ISP technology also solves the handling problems associated with high pin count, fine pitch packages (PQFP, TQFP etc.). It eliminates bent leads and unreliable solder joints by programming devices in-system.

Summary

Lattice, the leader in E²CMOS PLDs, is committed to providing its customers with industry-leading programmable solutions. We realize that your system design requirements and time-to-market pressures will only get tougher in the future. Lattice is committed to supporting you with state-of-the-art products with the performance, architecture, quality and reliability to meet your needs.

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Introduction to pLSI[®] and ispLSI[™] Families

The Lattice pLSI and ispLSI Families

The Lattice programmable Large Scale Integration (pLSI) and in-system programmable Large Scale Integration (ispLSI) families are the logical choice for your next design project. They're the first programmable logic devices to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs. And at 135 MHz system speed, and up to 14000 PLD gates, they're the world's fastest and highest density programmable logic devices!

There are three pLSI and ispLSI families to fit your specific application needs. Lattice's premier pLSI and ispLSI 1000 family implements high integration functions such as controllers, LANs and encoders at high speeds. The high performance pLSI and ispLSI 2000 family with its large number of I/Os handles timers, counters as well as timing critical interfaces to high speed RISC/CISC microprocessors. The highest density pLSI and ispLSI 3000 family integrates complete system logic, DSP functions, and entire encryption or compression logic into a single package, while delivering superior performance.

The ispLSI 1000, 2000 and 3000 families pioneer non-volatile, in-system programmability, a technology that allows real-time programming, less expensive manufacturing and end-user system reconfiguration.

All the development tools you need are available from Lattice - tools ranging from Lattice's own entry level software to higher level, third-party design environments. With these tools, you'll be completing your circuit designs in hours instead of weeks or months.

pLSI and ispLSI 1000: The Premier High Density Family

- 110 MHz system performance
- 10 ns pin-to-pin delay (maximum)
- 2000-8000 PLD gates
- 44-pin to 128-pin packages

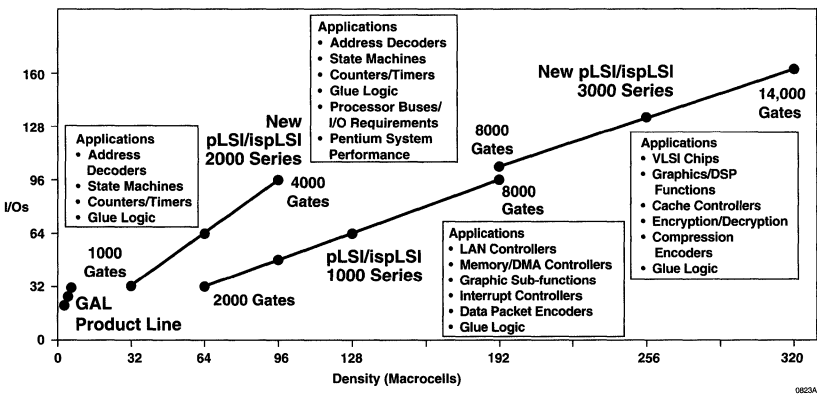
pLSI and ispLSI 2000: Unparalleled System Performance

- 135 MHz system performance (world's fastest!)
- 7.5 ns pin-to-pin delay (maximum)
- 1000-4000 PLD gates
- 44-pin to 128-pin packages
- High I/O to Logic Ratio

pLSI and ispLSI 3000: Density with Performance

- 110 MHz system performance
- 10 ns pin-to-pin delay (maximum)
- 8000-14000 PLD gates (world's largest!)
- 128-pin to 208-pin packages
- Boundary scan for enhanced testability (IEEE 1149.1)

Lattice's pLSI and ispLSI Families



Introduction to pLSI and ispLSI

Family Overview

From registers to counters, from multiplexers to complex state machines, these families of high-density programmable logic will address your high-performance system logic needs.

With PLD gate densities ranging from 1,000 to 14,000, the pLSI and ispLSI devices provide the range of programmable logic solutions you need to meet design requirements today and tomorrow.

Each device contains multiple Generic Logic Blocks (GLBs), architected to maximize system flexibility and performance. And a generous supply of registers and I/O cells provides the optimum balance of internal logic and external connections. A global interconnect scheme ties everything together, enabling high logic utilization.

Table 1. pLSI and ispLSI Family Attributes

pLSI and ispLSI 1000

	ispLSI 1016	ispLSI 1024	ispLSI 1032	ispLSI 1048/1048C
Density (PLD Gates)	2000	4000	6000	8000
Speed: Fmax (MHz)	110	90	90	80
Speed: Tpd (ns)	10	12	12	15
Macrocells	64	96	128	192
Registers	96	144	192	288
Inputs & I/Os	36	54	72	106/110
Pins/Package	44-PLCC 44-TQFP 44-JLCC	68-PLCC 68-JLCC	84-PLCC 100-TQFP 84-CPGA	120-PQFP 128-PQFP

1/2/3000-2A

Introduction to pLSI and ispLSI

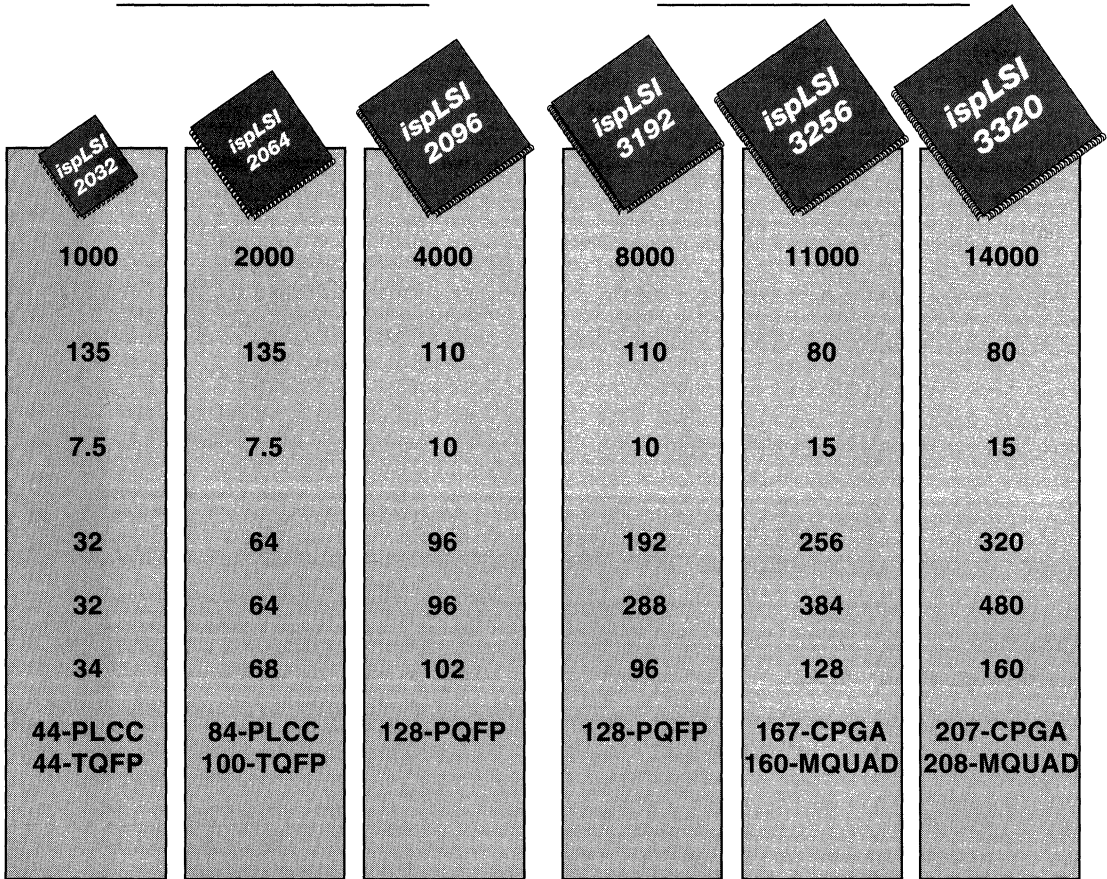
pLSI and ispLSI Architecture

The pLSI and ispLSI architecture was constructed with real system design requirements in mind. Figure 1 shows the representation of the pLSI 3256 architecture. This architecture provides the designer with the following advantages.

- High Speed
- Predictable performance
- Low power
- Flexible architecture
- Easy to use
- Design portability across all the families
- Non-volatile in-system programmable (ispLSI)
- Advanced Global Clock Network
- Boundary Scan (3000 Family)

pLSI and ispLSI 2000

pLSI and ispLSI 3000



1/2/3000-3A

Introduction to pLSI and ispLSI

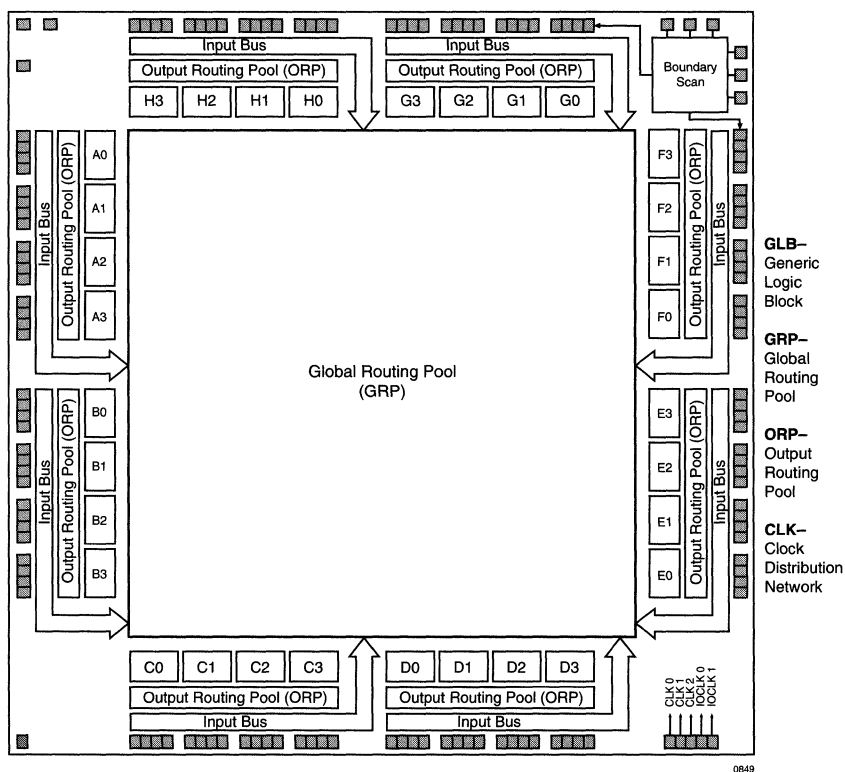
The Global Routing Pool

Central to the pLSI and ispLSI architecture is the Global Routing Pool (GRP), which connects all of the internal logic and makes it available to the designer. The GRP provides complete interconnectivity with fixed and predictable delays. This unique interconnect scheme consistently provides high performance and allows effortless implementation of complex designs.

The Output Routing Pool (ORP)

The Output Routing Pool (ORP) is a unique pLSI and ispLSI architectural feature which provides flexible connections between the GLB outputs and the output pins. This flexibility allows for "last minute" logic design changes to be implemented without changing the external pin-out.

Figure 1. pLSI 3256 Functional Block Diagram



Generic Logic Block (GLB)

The key element in the pLSI and ispLSI architecture is the Generic Logic Block (GLB). This powerful logic block provides a high input-to-output ratio for best logic efficiency. The GLB (figure 2) used in the pLSI and ispLSI 1000 and 2000 families feature 18 inputs which drive an array of 20 Product Terms (PTs). These product terms feed four outputs which effectively handle both wide and narrow gating functions. The pLSI and ispLSI 3000 family

utilizes a Twin GLB which delivers wider logic functionality. The Twin GLB accepts 24 inputs and feeds two arrays of 20 Product Terms that ultimately drive two sets of four outputs.

The architectural flexibility of the pLSI and ispLSI GLB, combined with its optimum input-to-output ratio, allows the GLB to implement virtually all 4-bit and 8-bit MSI functions.

An additional element of architectural flexibility is the Product Term Sharing Array (PTSA). The PTSA allows the 20 PTs from the AND array to be shared with any and all of the four GLB outputs. This ability to share PTs between all of the four GLB outputs provides a highly efficient means to implement complex state machines by eliminating duplicate product term groups.

Each of the four outputs from the PTSA feeds into a flexible Output Logic Macrocell (OLMC), consisting of a D-type flip-flop with an Exclusive-OR gate on the input.

The OLMC allows each GLB output to be configured as either combinatorial or registered. Combinatorial mode is available as AND-OR or Exclusive-OR. Registered mode is available as D, T or J-K.

The power of the GLB is further enhanced by a flexible clock distribution network. This network provides a choice of clock signals to each GLB: global synchronous clock signals or internally generated asynchronous product term clock signals.

Figure 2. pLSI and ispLSI 1000 and 2000 Family GLB

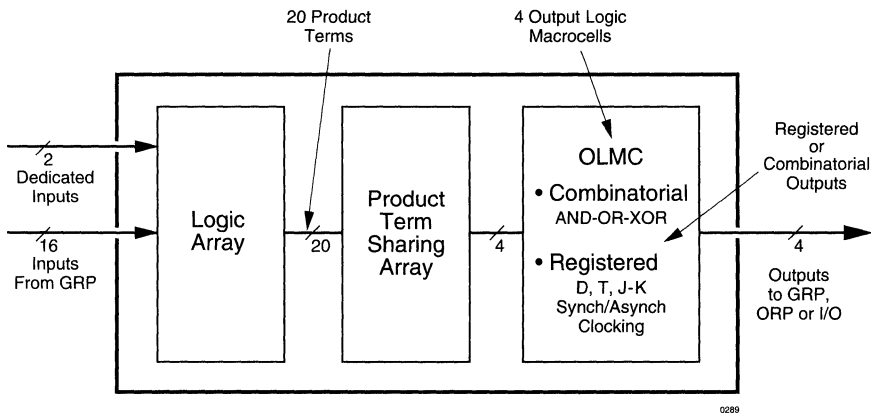
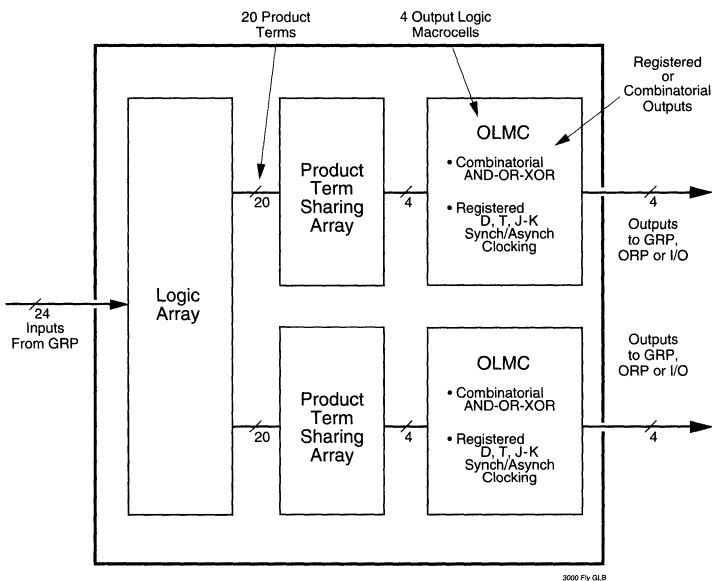
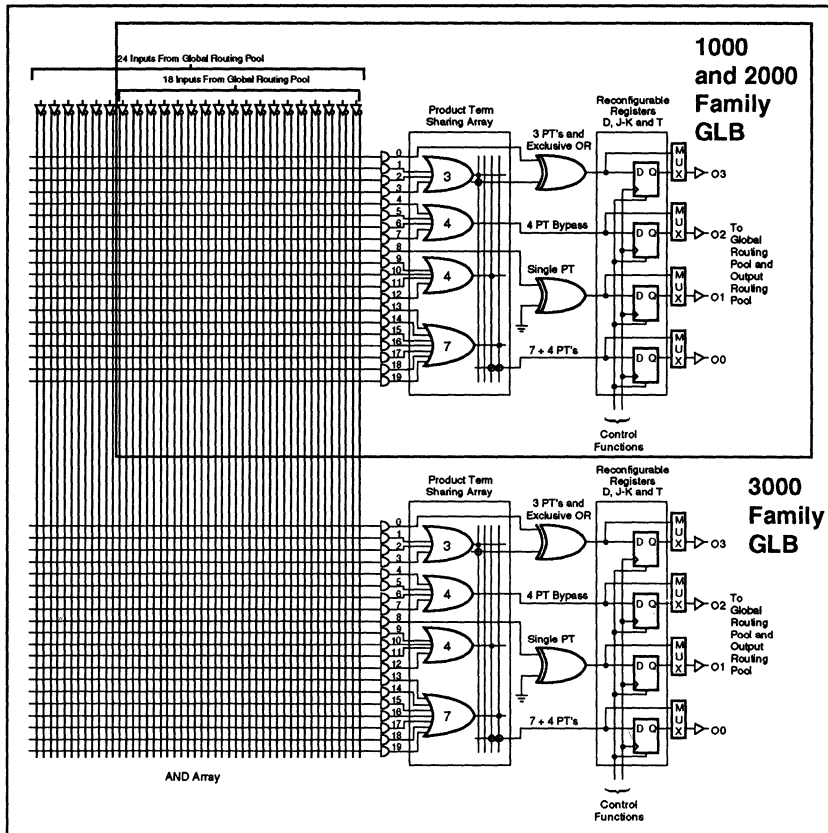


Figure 3. pLSI and ispLSI 3000 Family "Twin GLB"



Introduction to pLSI and ispLSI

Figure 4. GLB: Multi-Mode Configuration



0845

Standard Configuration

- GLB Outputs Comprised of 4, 4, 5 and 7 Product Terms
- The PTSA can Combine up to 20 Product Terms per GLB Output to Meet the Needs of Both Wide and Narrow Logic Functions

High-Speed Bypass Configuration

- For Speed-Critical Timing Paths
- Bypasses the PTSA and the Internal Exclusive-OR gate of the OLMC
- Provides Four Product Terms per Output
- Supports Design of Fast Address Decoders

Exclusive-XOR Configuration

- Utilizes Powerful Exclusive-XOR Architecture
- Great for Counters, Comparators and ALU Functions

Single PT Configuration

- Small Logic Functions at Fast Speed

Multi-Mode Configuration

- Individual Outputs are Independently Configurable
- PTSA Gives Flexibility in the Number and Selection of Product Terms per Output

Security Cell

A security cell is provided in the pLSI and ispLSI devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed.

Device Programming

pLSI and ispLSI devices can be programmed using a Lattice-approved device programmer, available from a number of third party manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is automatic and is completely transparent to the user. In-system programming is also available with ispLSI devices which allows programming on the circuit board using Lattice programming algorithms and standard 5V system power.

Latch-up Protection

pLSI and ispLSI devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the internal circuitry to latch-up. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

In-system programmability

Lattice's ispLSI devices (in-system programmable) are the industry's only high-density programmable logic family offering non-volatile, in-system reconfigurability.

ispLSI devices are available in all three families: 1000, 2000 and 3000. The ispLSI devices are 100 percent functionally and parametrically compatible with their pLSI counterparts, with the added capability for 5-volt in-system programmability and reprogrammability.

Complex logic functions can be implemented in multiple ispLSI devices with complete on-board configurability. In-system programming of a multiple ispLSI chip solution is easily achieved through a proprietary in-system erase/program/verify technique.

In-system programmability can revolutionize the way you design, manufacture and service systems.

Prototype Board Designs

In-system programming allows you to program and modify your logic designs "in-system" without removing the device(s) from the board. This accelerates the system and board-level debug process and enables you to define the board layout earlier in the design process.

Fine Pitch Package Handling

When programming traditional PLDs, manual handling is required during both design/debugging and manufacturing stages. When using PQFPs or TQFPs, fragile leads as thin as 0.5 mm can easily bend in the programmer socket causing coplanarity damage. With ispLSI, you can solder these packages onto your printed circuit board and still program and reprogram the devices during debugging and manufacturing – without ever losing a single part due to bent leads.

Reconfigurable Systems

Your options become boundless when you have the ability to change the functionality of devices already soldered on a p.c. board. You can now implement multiple hardware configurations with the same circuit board design. A variety of protocols or system interfaces can be implemented on a generic board as the last step in the manufacturing flow.

Easier Field Updates

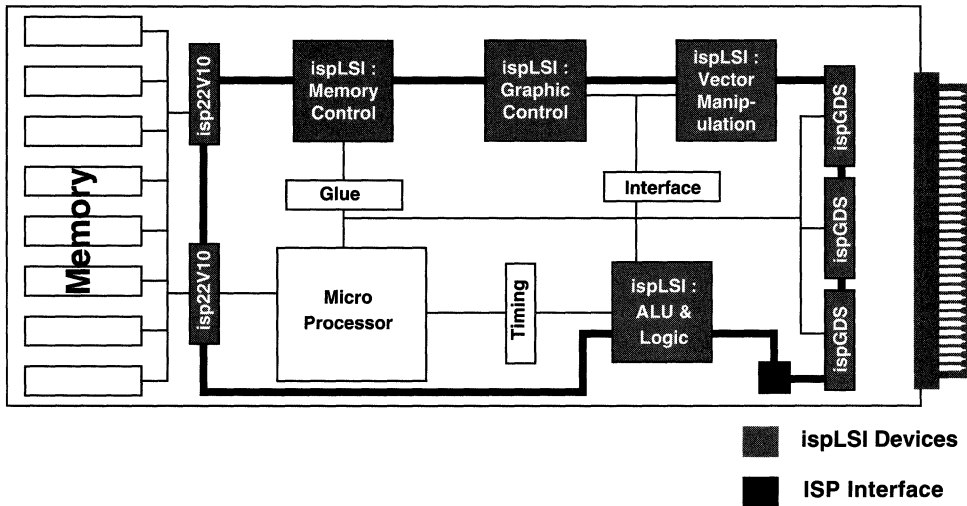
With software reconfigurable systems, field updates are as easy as loading a new configuration from a floppy or downloading it through a modem.

Enhanced Manufacturing Flow with ispLSI

Perhaps the most exciting benefit of the ispLSI family is its potential to streamline the manufacturing process by eliminating the separate programming and labeling steps usually associated with PLDs. Quality is enhanced when product handling steps are reduced, in this case, those associated with programming, labeling and re-inventorying multiple device types. Eliminating socketing further improves quality and reduces board cost. Figure 6 shows the enhanced manufacturing with the ispLSI device.

Introduction to pLSI and ispLSI

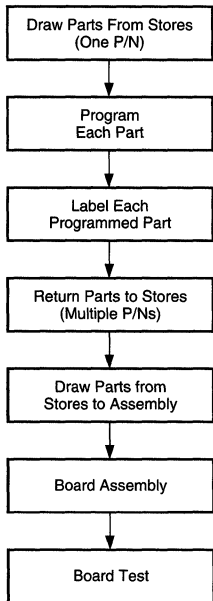
Figure 5. In-System Programmable Graphics Board



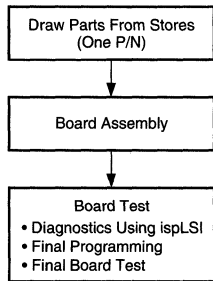
0290D

Figure 6. Manufacturing Flow Comparison

Standard Flow Using PLDs/FPGAs

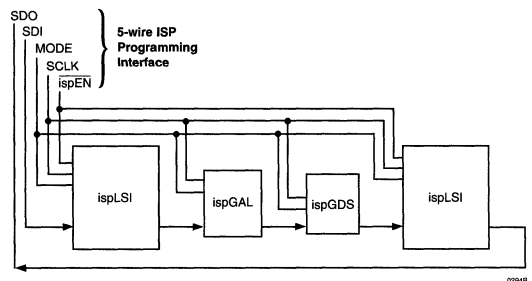


Enhanced Flow Using ispLSI Devices



All necessary programming is achieved via five TTL-level logic interface signals (see figure 7). These five signals control the on-chip programming circuitry, which protects against inadvertent reprogramming via on-chip state machines. The ispLSI family can also be programmed using popular third-party logic programmers.

Figure 7. In-System Programming Interface (Multi-Chip Solution)



0294B

Boundary Scan

An emerging trend in board-level testing is boundary scan test, an attractive feature helping designers test system boards efficiently while lowering test and manufacturing costs. The pLSI and ispLSI 3000 family offers dedicated IEEE 1149.1 boundary scan support for all test functions required by the standard. By using pLSI and ispLSI devices you not only eliminate expensive "bed-of-nails" testers but also simplify testing of surface-mount boards, multi-layer boards and boards using fine-pitch packages. Boundary scan is ideal wherever tight board layout limits access to logic signals.

It only takes 4 pins to implement the boundary scan interface. The ispLSI 3000 devices share the four boundary scan signals with the in-system programming pins. This enhances the testability of system designs allowing logic to be reconfigured to improve controllability and observability.

Lattice Development Systems

The Lattice pLSI/ispLSI Development System (pDS) software is used to implement designs in pLSI and ispLSI devices. Design alternatives can be quickly implemented using Lattice's low cost pDS software or the pDS+ family of Fitters that interface with third-party development software packages. This section describes the pDS and pDS+ Development Systems. Programmer support is also discussed.

pLSI/ispLSI Development System (pDS)

Features

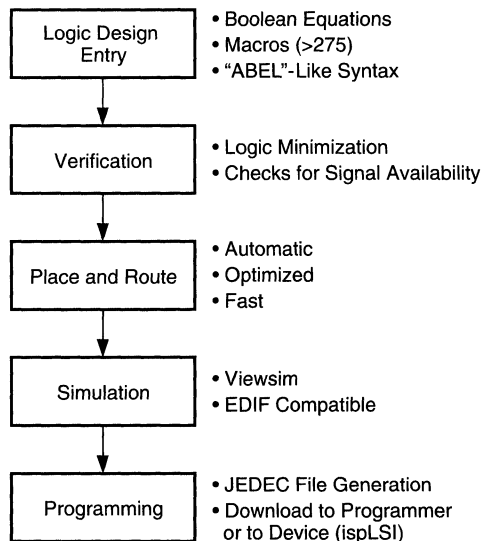
- High-Performance, Low-Cost Development Environment
- Supports pLSI and ispLSI Device Families
- Boolean Logic and Text File Design Entry
- Windows Based Graphical User Interface
- Over 275 Macros Available
- Automatic Place and Route
- Static Timing Table
- Logic Simulation with Viewlogic™ Viewsim™
- JEDEC File Download Direct to Programmer or ispLSI Device

General Description

All pLSI and ispLSI families are supported by Lattice's low-cost pDS software. It runs on IBM-compatible (386/486/Pentium) PCs with Microsoft® Windows.

The graphical user interface employs an easy-to-use mouse and pull-down menu driven approach. Combined with Boolean logic data entry using an ABEL™-like syntax, pDS makes design entry with pLSI and ispLSI quick and straightforward (see figure 8).

Figure 8. pDS Design Flow



0292A

The pDS software supports over 275 macros to assist the design process. These macros cover most TTL functions, from gate primitives to 16-bit counters. The software also supports user-definable macros which can be modifications of existing macros or custom creations.

The pDS software automatically verifies the design, performs logic minimization and checks for signal availability.

The Lattice Place and Route software assigns pins and critical speed paths while routing the design.

Quick compilation speeds the design, debug and rework process dramatically. Incremental design techniques are also supported.

Introduction to pLSI and ispLSI

Timing and functional simulation is available from Lattice, using Viewsim simulation software.

The Windows graphical user interface makes programming easy, using pull-down menus, intuitive point-and-click commands and self explanatory instructions. Without any up-front training, designs can be completed within hours instead of days or weeks.

pLSI/ispLSI Development System Plus (pDS+)

Features

- Supports pLSI and ispLSI Device Families
- Schematic Capture, State Machine, Design Entry HDL, and Boolean Equations
- Expanded Macro Library (>300)
- Automatic Logic Minimization and Partitioning
- Automatic Place and Route
- Logic and Timing Simulation
- EDIF Compatible
- JEDEC File Download Direct to Programmer or ispLSI Device

General Description

For higher level design entry environments, Lattice offers pDS+ development software packages, which expand on the core capabilities of pDS. Schematic capture, state machine, HDL and Boolean entry are supported, along with an expanded macro library.

The pDS+ software utilizes industry standard third-party design environments such as Viewlogic's Viewdraw™ and Data I/O's ABEL.

Running on IBM compatible (386/486/Pentium) PCs or workstation platforms, pDS+ software supports automatic logic minimization and partitioning as well as place and route, resulting in high logic utilization.

For logic and timing simulation, support is available from Lattice through Viewlogic Viewsim simulation tools.

Third Party Programming Support

The pLSI and ispLSI families are supported by popular third-party logic programmers including Data I/O, Logical Devices, BP-Microsystems, Stag, System General, SMS Micro Systems and Advin. Table 2 describes each vendor's specific programmer models that support the

pLSI and ispLSI devices. No proprietary, expensive, high pin-count programmers are required.

High pin-count socket adapters are available from Emulation Technology, Procon Technology, EDI Corporation and Logical Systems Corporation.

Additionally, the ispLSI family can be programmed on the board (in-system), which eliminates the need for a stand-alone programmer. For specific details refer to the Lattice Programming Tools Guide available from your local Sales Representative.

Table 2. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

isp Engineering Kit

The ispLSI family may also be programmed with Lattice's isp Engineering Kit Model 100 for PCs and Model 200 for Sun workstations. The kit is designed for engineering purposes only and is not intended for production use. By connecting an 8 wire cable to the parallel printer port of a PC, JEDEC files can be easily downloaded into the ispLSI device. Additionally, this cable can be connected directly to the circuit board facilitating on-board in-system programming.

1000 Family

Architectural Description

pLSI and ispLSI 1000 Family Introduction

The basic unit of logic for the pLSI and ispLSI families is the Generic Logic Block (GLB). Figure 1 illustrates the pLSI 1032 with its 32 GLBs labelled A0, A1 .. D7. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the Global Routing Pool (GRP) and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

As an example, the pLSI 1032 has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

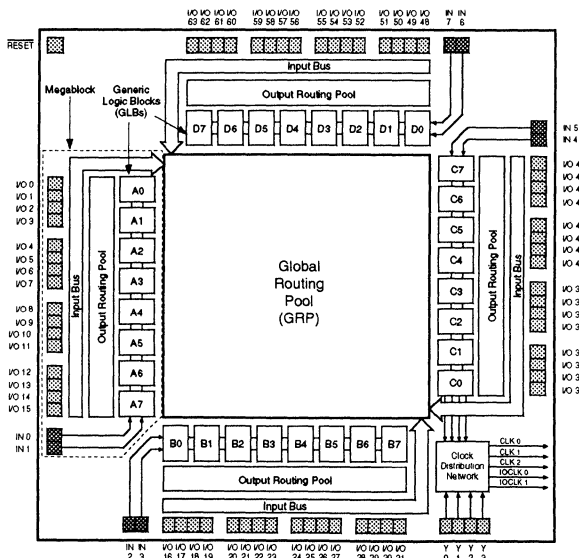
The I/O cells are grouped into sets of 16 as shown in figure 1. Each of these I/O groups is associated with a Megablock through the use of the Output Routing Pool (ORP).

Eight GLBs, 16 I/O cells, one ORP and two dedicated inputs are connected together to make a Megablock. The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each Megablock shares a common Output Enable (OE) signal. The pLSI 1032 device, shown in figure 1 contains four Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the devices are selected using the Clock Distribution Network. The dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five outputs (CLK 0, CLK1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special GLB (C0 on the pLSI and ispLSI 1032 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Figure 1. pLSI 1032 Functional Block Diagram



1000 Family Architectural Description

Generic Logic Block

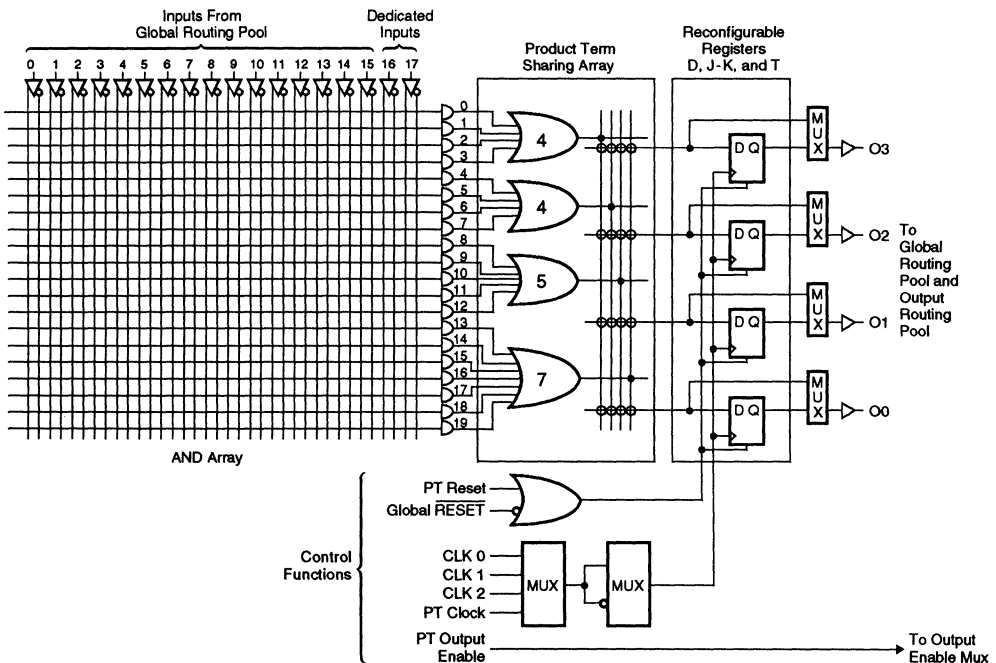
The Generic Logic Block (GLB) is the standard logic block of the Lattice high-density pLSI and ispLSI devices. A GLB has 18 inputs, four outputs and the logic necessary to implement most standard logic functions. The internal logic of the GLB is divided into four separate sections: the AND Array, the Product Term Sharing Array (PTSA), the Reconfigurable Registers, and the Control Functions (see figure 2). The AND array consists of 20 product terms which can produce the logical sum of any of the 18 GLB inputs. Sixteen of the inputs come from the Global Routing Pool, and are either feedback signals from any of the GLBs or inputs from the external I/O cells. The two remaining inputs come directly from two dedicated input pins. These signals are available to the product terms in both the logical true and the complemented forms which makes boolean logic reduction more efficient.

The PTSA takes the 20 product terms and routes them to the four GLB outputs. There are four OR gates, with four, four, five and seven product terms each (see figure

2). The output of any of these OR gates can be routed to any of the four GLB outputs, and if more product terms are needed, the PTSA can combine them as necessary. In addition, the PTSA can share product terms similar to an FPLA device. If the user's main concern is speed, the PTSA can use a bypass circuit which provides four product terms to each output, to increase the performance of the cell (see figure 3). This can be done to any or all of the four outputs from the GLB.

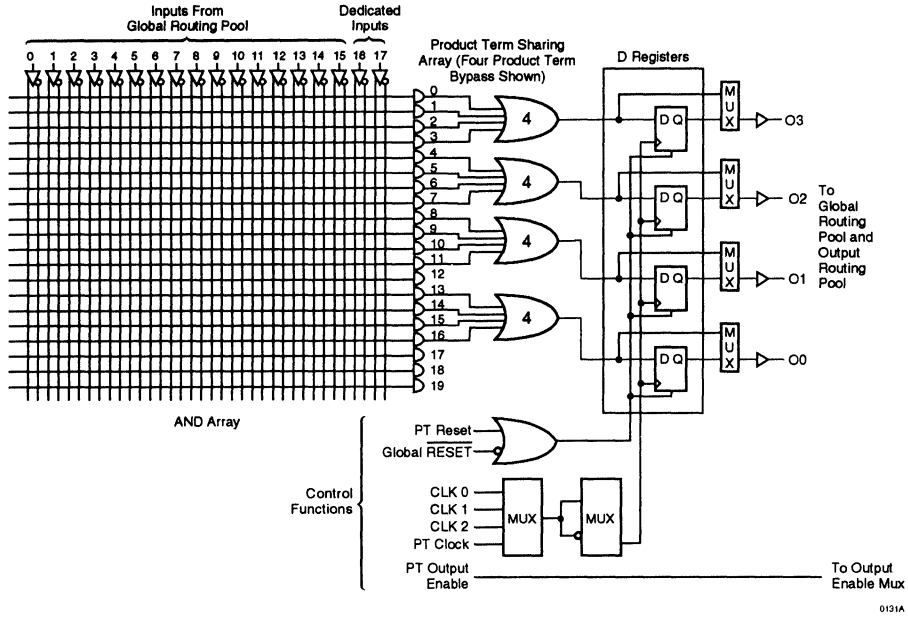
The Reconfigurable Registers consist of four D-type flip-flops with an XOR gate on the input. The XOR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K or T-type flip-flop (see figure 4). This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used.

Figure 2. GLB: Product Term Sharing Array Example



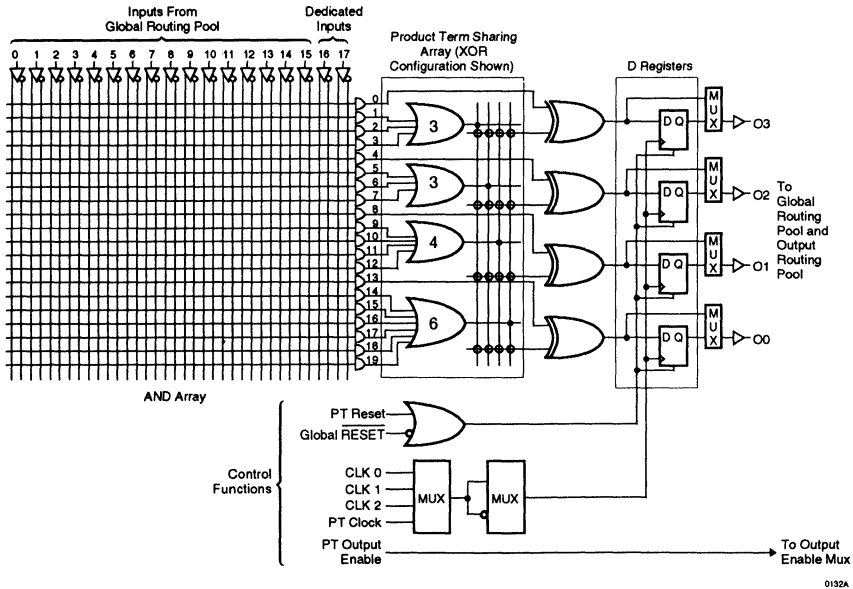
1000 Family Architectural Description

Figure 3. GLB: Four Product Term Bypass Example



2

Figure 4. GLB: XOR Gate Example



1000 Family Architectural Description

Generic Logic Block (continued)

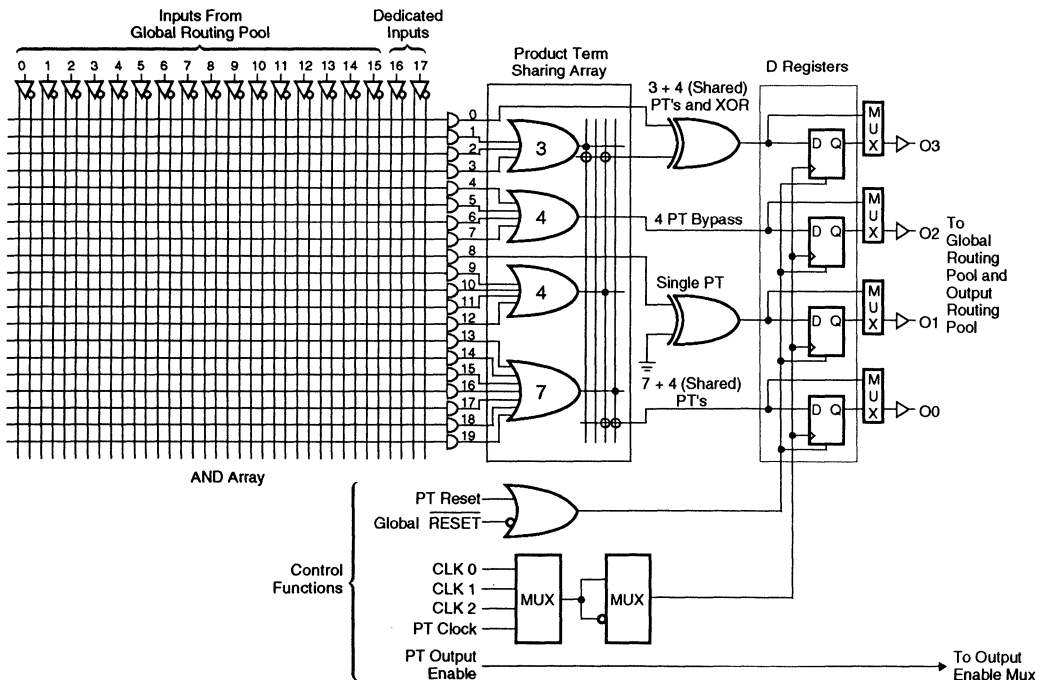
The PTSA is flexible enough to allow these features to be used in virtually any combination that the user desires. In the GLB shown in figure 5, Output Three (O3) is configured using the XOR gate while Output Two (O2) is configured using the four Product Term Bypass. Output One (O1) uses one of the inputs from the five Product Term OR gate while Output Zero (O0) combines the remaining four product terms with all of the product terms from the seven Product Term OR gate for a total of eleven (7+4).

Various signals which control the operation of the GLB outputs are driven from the Control Functions (see figure 5). The clock for the registers can come from any of three sources developed in the Clock Distribution Network (see Clock Distribution Network section) or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin (RESET) or from a

product term within the block. The global reset pin is always connected and is logically "ORed" with the PT reset (if used). An active reset signal always sets the Q of the registers to a logic 0 state. The Output Enable for the I/O cells associated with the GLB comes from a product term within the block. Use of a product term for a control function makes that product term unavailable for use as a logic term. Refer to the Product Term Sharing Matrix (table 1) to determine which logic functions are affected.

There are many additional features in a GLB which allow implementation of logic intensive functions. These features are accessible using the Hard Macros from the software and require no intervention on the part of the user.

Figure 5. GLB: Mixed Mode Configuration Example



1000 Family Architectural Description

Product Term Sharing Matrix

This matrix shows how each of the product terms are used in the various modes. As an example, Product Term 12 can be used as an input to the five input OR gate in the standard configuration. This OR gate under standard configuration can be routed to any of the four GLB outputs. Product Term 12 is not used in the four

product term bypass mode. When GLB output one is used in the XOR mode Product Term 12 becomes one of the inputs to the four input OR Gate. If Product Term 12 is not used in the logic, then it is available for use as either the Asynchronous Clock signal or the GLB Reset signal.

Table 1. Product Term Sharing Matrix

Product Term #	Standard Configuration Output Number	Four Product Term Bypass Output Number	Single Product Term Output Number	XOR Function Output Number								Alternate Function		
	3 2 1 0	3 2 1 0	3 2 1 0	3 3 2 2 1 1 0 0										
0	■ ■ ■ ■	■	■	■										
1	■ ■ ■ ■	■			■									
2	■ ■ ■ ■	■			■									
3	■ ■ ■ ■	■			■									
4	■ ■ ■ ■		■			■								
5	■ ■ ■ ■	■					■							
6	■ ■ ■ ■	■					■							
7	■ ■ ■ ■	■					■							
8	■ ■ ■ ■		■					■						
9	■ ■ ■ ■			■					■					
10	■ ■ ■ ■				■					■				
11	■ ■ ■ ■					■					■			
12	■ ■ ■ ■											■	CLK/Reset	
13	■ ■ ■ ■			■										
14	■ ■ ■ ■				■									
15	■ ■ ■ ■					■								
16	■ ■ ■ ■						■							
17	■ ■ ■ ■							■						
18	■ ■ ■ ■								■					
19	■ ■ ■ ■									■				OE/Reset

The Megablock

A Megablock consists of eight GLBs, an ORP, 16 I/O cells, two dedicated inputs and a common product term OE. Each of these will be explained in detail in the following sections. These elements are coupled together as shown in figure 6. The various members of the pLSI and ispLSI families combine from one to eight Megablocks on a single device (see table 2).

For the 1000 Family, the eight GLBs within the Megablock share two dedicated input pins. These dedicated input pins are not available to GLBs in any other Megablock. These pins are dedicated (non-registered) inputs only

and are automatically assigned by software. The product term OE signal is generated within the Megablock and is common to all 16 of the I/O cells in the Megablock. The OE signal can be generated using a product term (PT19) in any of the eight GLBs within the Megablock (see the section on the Output Enable Control for further details).

Because of the shared logic within the Megablock, signals which share a common function (counters, busses, etc.) should be grouped within a Megablock. This will allow the user to obtain the best utilization of the logic within the device and eliminate routing bottlenecks.

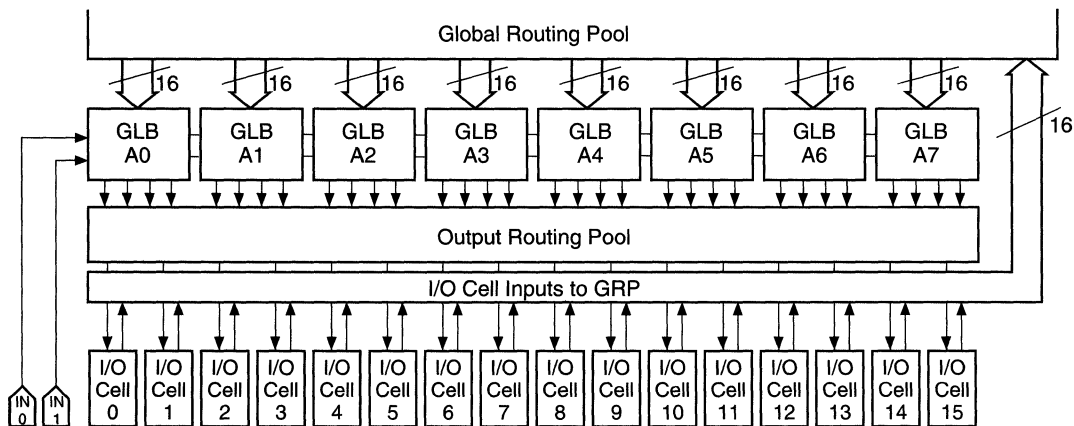
1000 Family Architectural Description

Table 2. Device Resources

pLSI and ispLSI Devices	Megablocks	GLBs	I/O Cells	Dedicated Inputs
1016	2	16	32	4
1024	3	24	48	6
1032	4	32	64	8
1048/1048C	6	48	96	10/12

Table 2-0015B

Figure 6. The Megablock Block Diagram



Input Routing

Signal inputs are handled in two ways within the device. First, each I/O cell within the device has its input routed directly to the GRP. This gives every GLB within the device access to each I/O cell input. Second, each Megablock has two dedicated inputs which are directly routed to the eight GLBs within the Megablock. Both input paths are shown in figure 6.

The Output Routing Pool

The ORP routes signals from the GLB outputs to I/O cells configured as outputs or bi-directional pins (see figure 7). The purpose of the ORP is to allow greater flexibility when assigning I/O pins. It also simplifies the job for the routing software which results in a higher degree of utilization.

By examining the ORP in figure 7, it can be seen that a GLB output can be connected to one of four I/O cells. Further flexibility is provided by using the PTSA, (figures 2 through 5) which makes the GLB outputs completely interchangeable. This allows the routing program to freely interchange the outputs to achieve the best routability. This is an automatic process and requires no intervention on the part of the user.

The ORP bypass connections (see figure 8) further increase the flexibility of the device. The ORP bypass connects specific GLB outputs to specific I/O cells at a faster speed. The bypass path tends to restrict the routability of the device and should only be used for critical signals.

1000 Family Architectural Description

Figure 7. Output Routing Pool

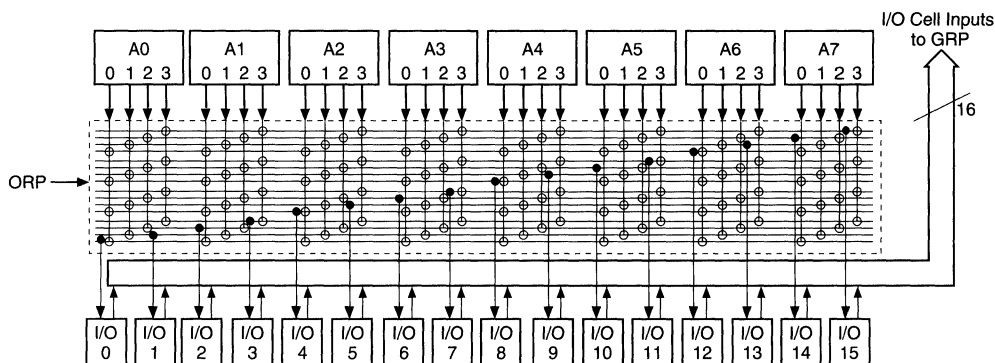
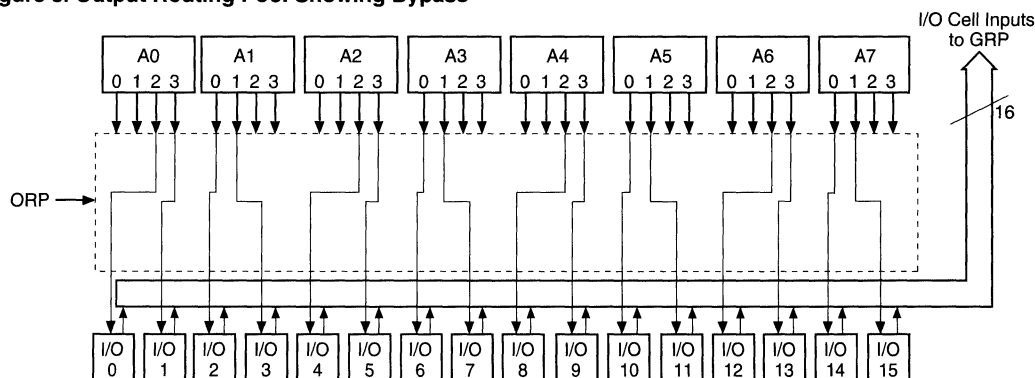


Figure 8. Output Routing Pool Showing Bypass



I/O Cell

The I/O cell (see figure 9) is used to route input, output or bi-directional signals connected to the I/O pin. The two logic inputs come from the ORP (see figure 9). One comes from the ORP, and the other comes from the faster ORP bypass. A pair of multiplexers select which signal will be used, and its polarity. The Output Enable of the I/O cell is controlled by the OE signal generated within each Megablock.

As with the data path, a multiplexer selects the signal polarity. The Output Enable can be set to a logic high (enabled) when an output pin is desired, or logic low (disabled) when an input pin is needed. The Global Reset ($\overline{\text{RESET}}$) signal is driven by the active low chip reset pin. This reset is always connected to all GLB and I/O registers. Each I/O cell can individually select one of

the two clock signals (IOCLK 0 or IOCLK 1). These clock signals are generated by the Clock Distribution Network.

Using the multiplexers, the I/O cell can be configured as an input, an output, a 3-stated output or a bi-directional I/O. The D-type register can be configured as a level sensitive transparent latch or an edge triggered flip-flop to store the incoming data. Figure 10 illustrates some of the various I/O cell configurations possible.

There is an active pull-up resistor on the I/O pins which is automatically used when the pin is not connected. An option exists to have active pull-up resistors connected to all pins. This improves the noise immunity and reduces lcc for the device.

1000 Family Architectural Description

Figure 9. I/O Cell Architecture

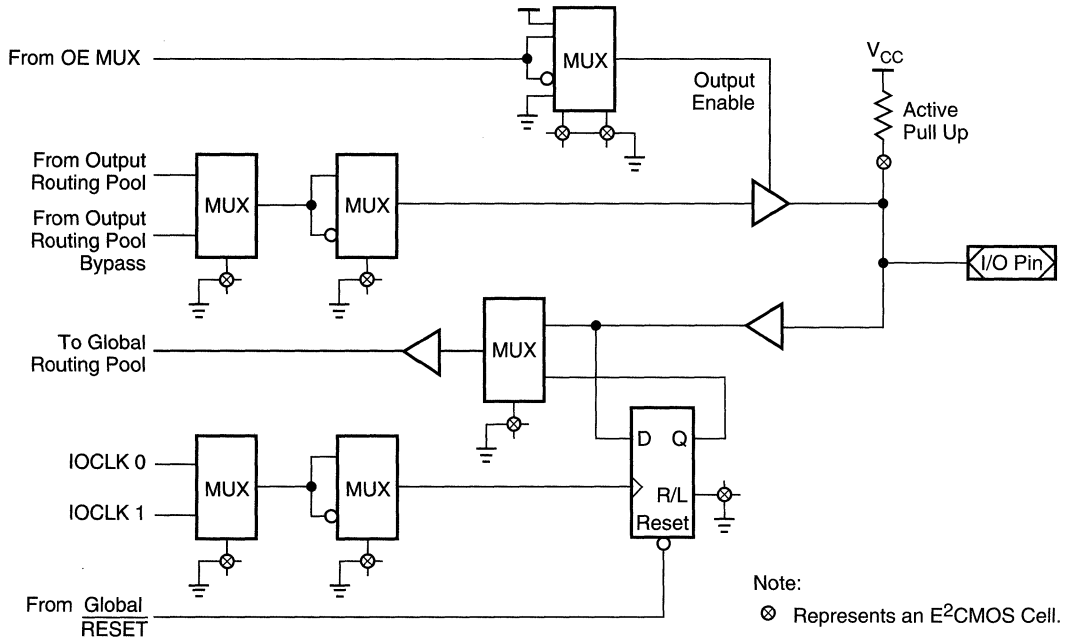
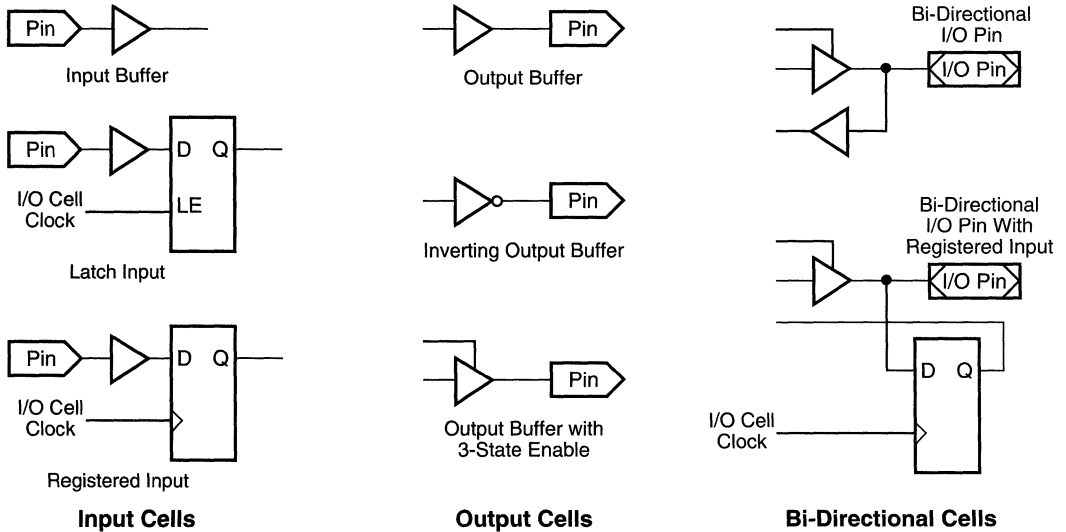


Figure 10. Examples of I/O Cell Configurations

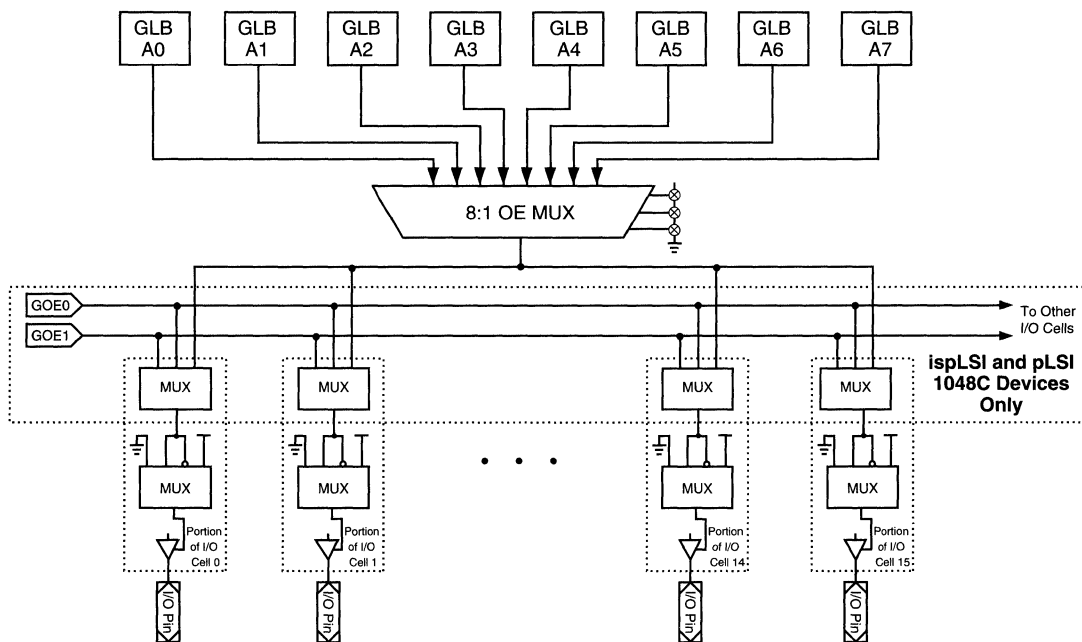


The Output Enable Control

One OE signal can be generated within each GLB using the OE Product Term (PT19). One of the eight OE signals within a Megablock is then routed to all of the I/O cells within that Megablock (see figure 11). This OE signal can simultaneously control all of the 16 I/O cells which are used in 3-state mode. Individual I/O cells also have independent control for permanently enabling or

disabling the output buffer (refer to the I/O cell section). Only one OE signal is allowed per Megablock for 3-state operation. The advantage to this approach is that the OE signal can be generated in any GLB within the Megablock which happens to have an unused OE product term. This frees up the other OE product terms for use as logic.

Figure 11. Output Enable Control for a Megablock



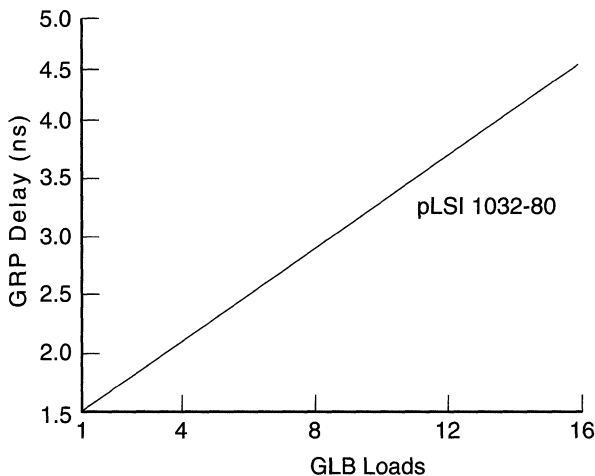
1000 Family Architectural Description

Global Routing Pool

The GRP is a Lattice proprietary interconnect structure which offers fast predictable speeds with complete connectivity. The GRP allows the outputs from the GLBs or the I/O cell inputs to be connected to the inputs of the GLBs. Any GLB output is available to the input of all other GLBs, and similarly an input from an I/O pin is available

as an input to all of the GLBs. Because of the uniform architecture of the pLSI and ispLSI devices, the delays through the GRP are both consistent and predictable. However, they are slightly affected by GLB loading as shown in the example pLSI 1032-80 GLB Loading Delay graph (see figure 12).

Figure 12. Example Graph of GRP Delay vs GLB Loading



Clock Distribution Network

The Clock Distribution Networks are shown in figure 13. They generate five global clock signals CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1. The first three, CLK 0, CLK 1 and CLK 2 are used for clocking all the GLBs in the device. Similarly, IOCLK 0 and IOCLK 1 signals are used for clocking all of the I/O cells in the device. There are four dedicated system clock pins (Y0, Y1, Y2, Y3), three for the pLSI and ispLSI 1016 (Y0, Y1, Y2), which can be directed to any GLB or any I/O cell using the Clock Distribution Network. The other inputs to the Clock Distribution Network are the four outputs of a dedicated clock GLB ("C0" for the pLSI 1032 is shown in figure 1). These clock GLB outputs can be used to create a user-defined internal clocking scheme.

For example, the clock GLB can be clocked using the external main clock pin Y0 connected to global clock

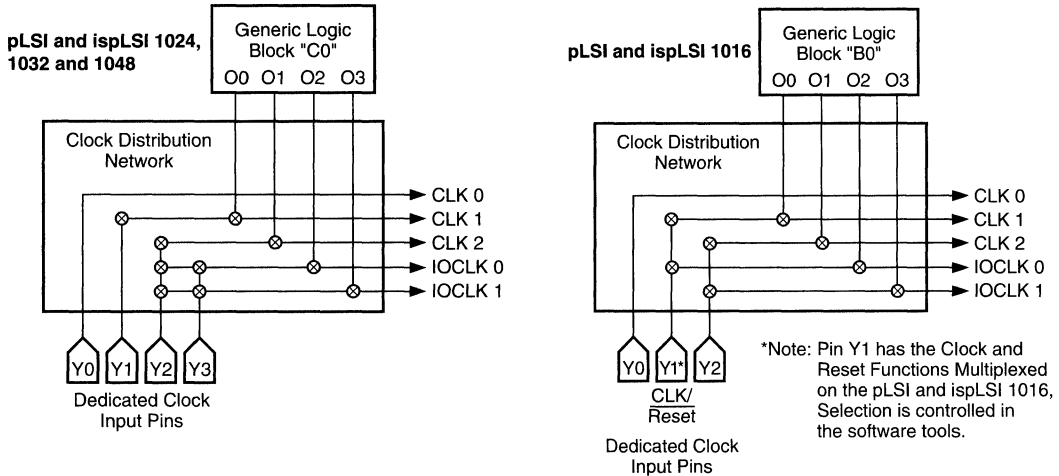
signal CLK 0. The outputs of the clock GLB in turn can generate a "divide by" signal of the CLK 0 which can be connected to CLK 1, CLK 2, IOCLK 0 or IOCLK 1 global clock lines.

All GLBs have the capability of generating their own asynchronous clocks using the clock Product Term (PT12). CLK 0, CLK 1 and CLK 2 feed to their corresponding clock MUX inputs on all the GLBs (see figure 2).

The two I/O clocks generated in the Clock Distribution Network IOCLK 0 and IOCLK 1, are brought to all the I/O cells and the user programs the I/O cell to use one of the two.

1000 Family Architectural Description

Figure 13. Clock Distribution Networks



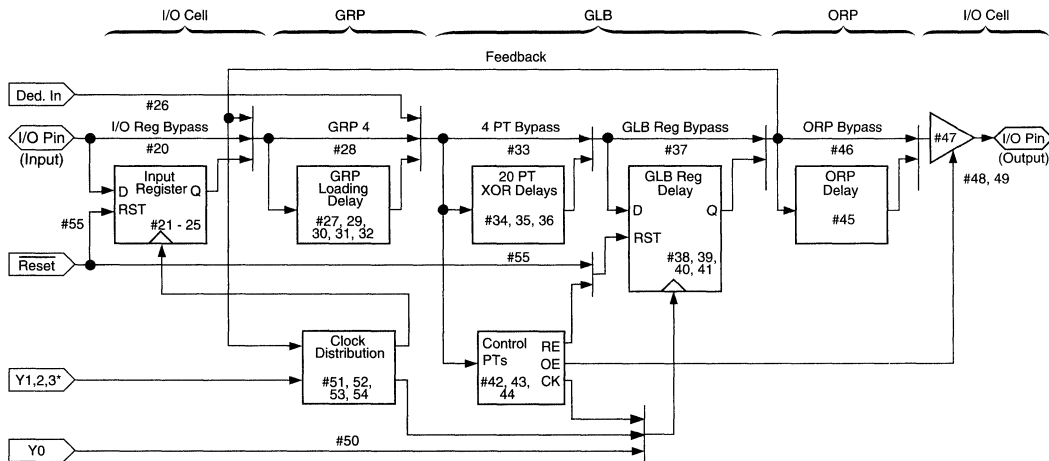
2

Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in figure 14. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (figure 15). Critical timing paths

are shown in figure 14, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. (External timing parameters are tested and guaranteed on every device).

Figure 14. pLSI and ispLSI Timing Model¹



¹Note: Y1 and Y2 only for the pLSI and ispLSI 1016.

1000 Family Architectural Description

Figure 15. pLSI and ispLSI Timing Model Examples¹

Combinatorial Paths

$$\begin{aligned} \text{tpd1} &= \text{tiobp} + \text{tgrp4} + \text{t4ptbp} + \text{torpbp} + \text{tob} \\ \#1 &= \#20 + \#28 + \#33 + \#46 + \#47 \end{aligned}$$

$$\begin{aligned} \text{tpd2} &= \text{tiobp} + \text{tgrp4} + \text{txoradj} + \text{torp} + \text{tob} \\ \#2 &= \#20 + \#28 + \#36 + \#45 + \#47 \end{aligned}$$

Registered Paths

General Form:

$$\text{tsu} = \text{Logic} + \text{Regsu} - \text{Clock(min)}$$

$$\text{th} = \text{Clock(max)} + \text{Regh} - \text{Logic}$$

$$\text{tco} = \text{Clock(max)} + \text{Regco} + \text{Output}$$

Specific Examples:

$$\begin{aligned} \text{tsu1} &= (\text{tiobp} + \text{tgrp4} + \text{t4ptbp}) + \text{tgsu} - \text{tgy0(min)} \\ \#6 &= (\#20 + \#28 + \#33) + \#38 - \#50 \end{aligned}$$

$$\begin{aligned} \text{th1} &= \text{tgy0(max)} + \text{tgh} - (\text{tiobp} + \text{tgrp4} + \text{t4ptbp}) \\ \#8 &= \#50 + \#39 - (\#20 + \#28 + \#33) \end{aligned}$$

$$\begin{aligned} \text{tco1} &= \text{tgy0(max)} + \text{tgco} + (\text{torpbp} + \text{tob}) \\ \#7 &= \#50 + \#40 + (\#46 + \#47) \end{aligned}$$

$$\begin{aligned} \text{tsu2} &= (\text{tiobp} + \text{tgrp4} + \text{txoradj}) + \text{tgsu} + \text{tgy0(min)} \\ \#9 &= (\#20 + \#28 + \#36) + \#38 + \#50 \end{aligned}$$

$$\begin{aligned} \text{th2} &= \text{tgy0(max)} + \text{tgh} - (\text{tiobp} + \text{tgrp4} + \text{txoradj}) \\ \#11 &= \#50 + \#39 - (\#20 + \#28 + \#36) \end{aligned}$$

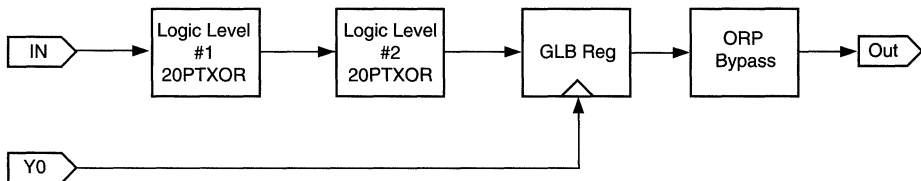
$$\begin{aligned} \text{tco2} &= \text{tgy0(max)} + \text{tgco} + (\text{torp} + \text{tob}) \\ \#10 &= \#50 + \#40 + (\#45 + \#47) \end{aligned}$$

1. The timing parameter reference numbers refer to the Internal Timing Parameters contained in the individual data sheets.

Circuit Timing Example

Figure 16. Timing Calculation Example

A design requires two logic levels (each uses the 20PTXOR path). The design then uses a GLB register before exiting the device using the ORP bypass. Calculate tsu , th and tco .



1000 Family Architectural Description

Figure 16. Timing Calculation Example (continued)

$$\begin{aligned}t_{su} &= \text{Logic} + \text{Reg su} - \text{Clock (min)} \\ &= (\mathbf{t_{iobp}} + \mathbf{t_{grp4}} + \mathbf{t_{20ptxor}} + \mathbf{t_{gbp}} + \mathbf{t_{grp4}} + \mathbf{t_{20ptxor}}) + \mathbf{t_{gsu}} - \mathbf{t_{gy0(min)}} \\ &= (\#20 + \#28 + \#35 + \#37 + \#28 + \#35) + \#38 - \#50 \\ 19.5 \text{ ns} &= (2.0 + 2.0 + 8.0 + 1.0 + 2.0 + 8.0) + 1.0 - 4.5 \\ \\t_h &= \text{Clock (max)} + \text{Reg h} - \text{Logic} \\ &= \mathbf{t_{gy0(max)}} + \mathbf{t_{gh}} - (\mathbf{t_{iobp}} + \mathbf{t_{grp4}} + \mathbf{t_{20ptxor}} + \mathbf{t_{gbp}} + \mathbf{t_{grp4}} + \mathbf{t_{20ptxor}}) \\ &= \#50 + \#39 - (\#20 + \#28 + \#35 + \#37 + \#28 + \#35) \\ -14.0 \text{ ns} &= 4.5 + 4.5 - (2.0 + 2.0 + 8.0 + 1.0 + 2.0 + 8.0) \\ \\t_{co} &= \text{Clock (max)} + \text{Reg co} + \text{Output} \\ &= \mathbf{t_{gy0(max)}} + \mathbf{t_{gco}} + (\mathbf{t_{orpbp}} + \mathbf{t_{ob}}) \\ &= \#50 + \#40 + (\#46 + \#47) \\ 10.0 \text{ ns} &= 4.5 + 2.0 + (0.5 + 3.0)\end{aligned}$$

1. The delay values used are for a pLSI 1032-80 device.

Notes

2000 Family

Architectural Description

pLSI and ispLSI 2000 Family Introduction

The basic unit of logic of the pLSI and ispLSI 2000 family is essentially the same as that of the pLSI and ispLSI 1000 family. However, there are some specific architectural differences: Global clock structure, I/O Cell and OE structure, and ORP structure. A functional block diagram of the 2032 device is shown in figure 1. These architectural differences are described in detail below.

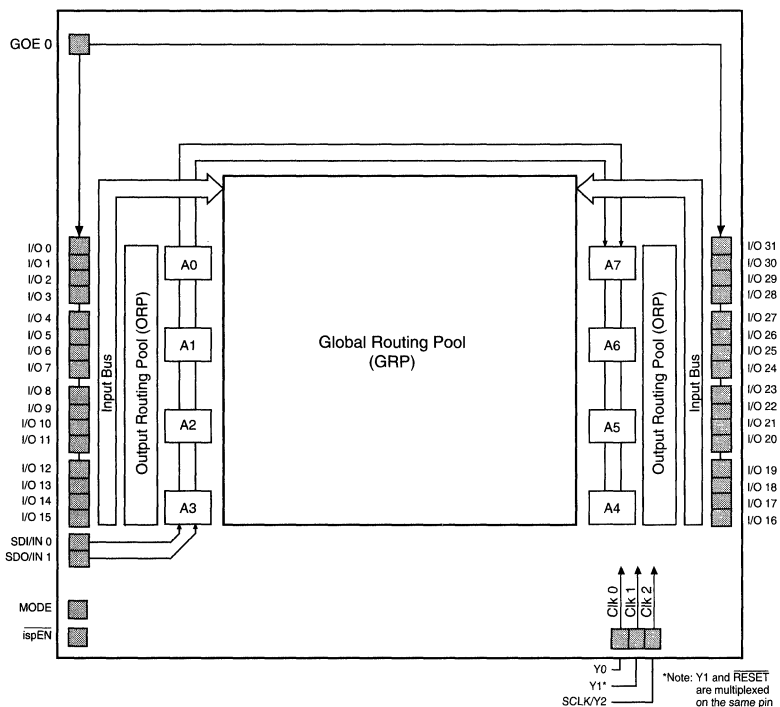
Global Clock Structure

The clock GLB distribution network of the 1000 family has been eliminated and replaced by three dedicated global

GLB clock input signals CLK0, CLK1, and CLK2. These three clocks are used for clocking all the GLBs configured as registers in the device. They feed directly to the GLB clock input via a clock multiplexer. CLK0 is associated with system clock pin Y0, CLK1 corresponds to system clock pin Y1, and finally CLK3 corresponds to system clock pin Y2. This is illustrated in figure 2. The GLB global clocks do not have inversion capability, but all GLBs continue to have the capability of generating their own asynchronous clocks using the clock product term (PT12) with inversion capability. The GLB global clocks and the GLB product term clock feed to their corresponding clock multiplexer shown in figure 3.

2

Figure 1. pLSI 2032 Functional Block Diagram



2000 Family Architectural Description

Figure 2. Global Clock Structure

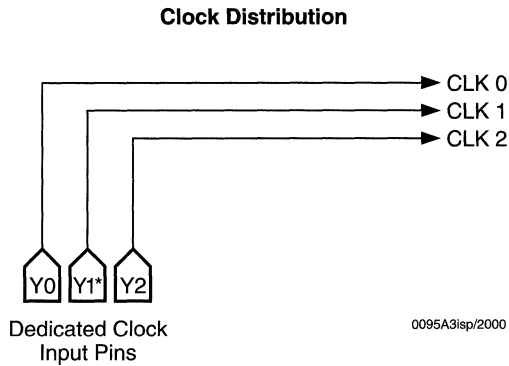
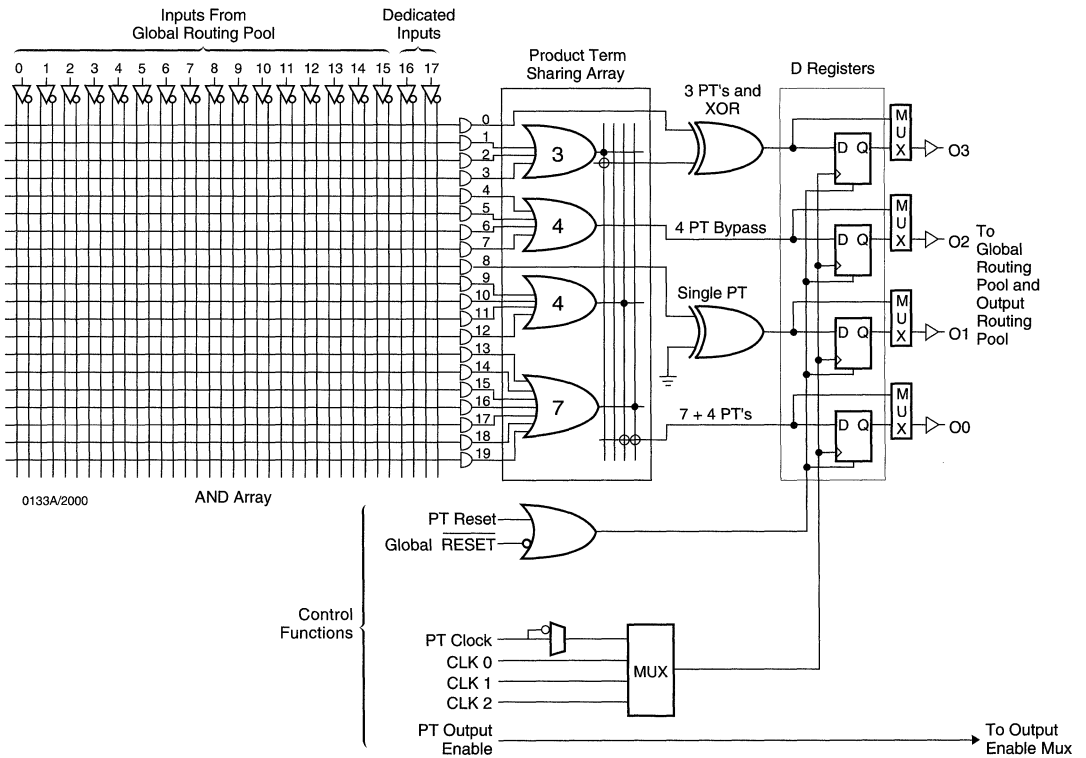


Figure 3. GLB with Clock Multiplexer Scheme



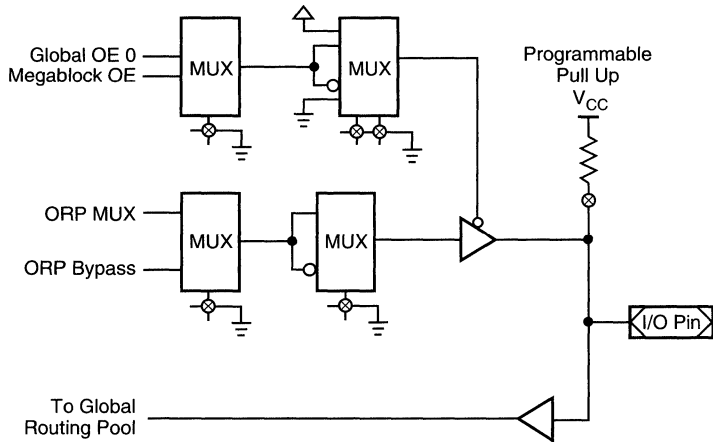
0133A/2000

I/O Cell and OE Structure

The reconfigurable input register or latch has been removed to simplify the I/O cell architecture. Each I/O cell can be individually programmed to be a combinatorial input, combinatorial output, or a bi-directional I/O pin with 3-state control. With the simplified I/O cell architecture, the I/O clocks have also been removed. This is illustrated in figure 4. The product term output enable (PTOE)

signal is still generated within each GLB using product term 19. The PTOE is generated in one of the eight GLBs. In addition to the PTOE, there is a global output enable (GOE) pin which can control any of the device's 3-state output buffers. The multiplexing between the GOE and PTOE is illustrated in figure 5. The 2032 device has one GOE, and the 2064 and 2096 devices each have 2 GOEs.

Figure 4. pLSI and ispLSI 2000 Family I/O Cell Architecture

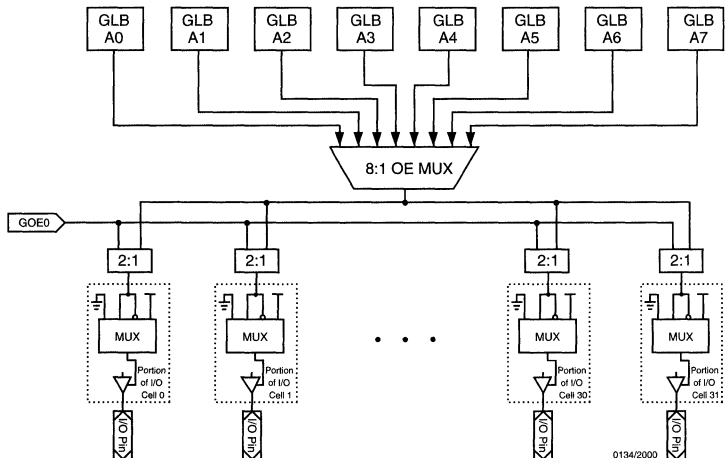


Note:

⊗ Represents an E²CMOS Cell.

0138A-7/2000

Figure 5. pLSI and ispLSI 2000 Family Output Enable Controls



0134/2000

2000 Family Architectural Description

Output Routing Pool (ORP)

Each megablock now contains two ORPs to increase output routability. A set of four GLBs is associated with one of the two ORPs within the megablock. The 16 outputs of the four GLBs within a megablock will feed to any of the 16 associated I/O cells. In the 1000 family, the

32 GLB outputs feed only 16 associated I/O cells. In this device family, 32 GLB outputs of a megablock can feed 32 I/O cells. Output routability has doubled. This is illustrated in figure 6. Each GLB output has an ORP bypass capability so more designs can have critical output signals. This is shown in figure 7.

Figure 6. pLSI and ispLSI 2000 Family Output Routing Pool

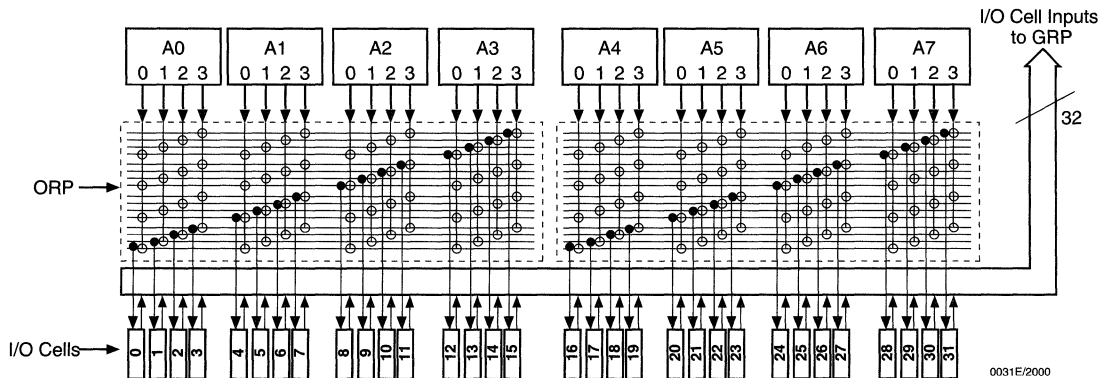
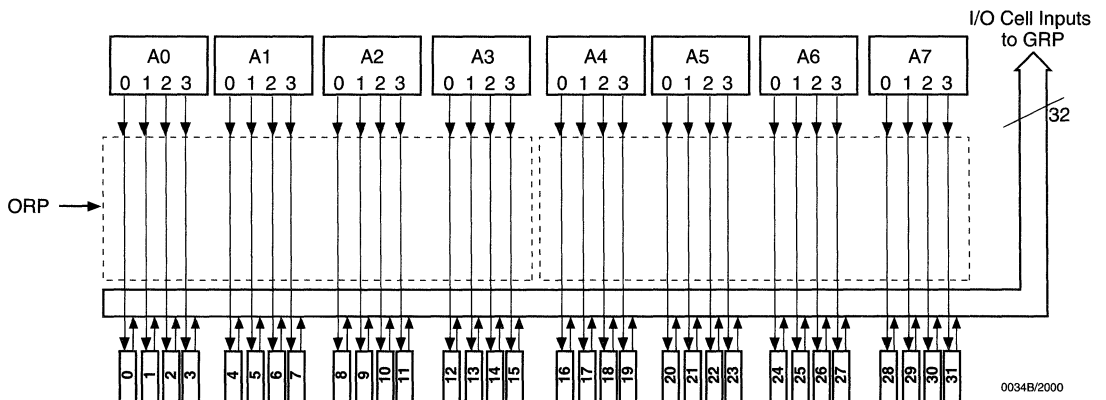


Figure 7. pLSI and ispLSI 2000 Family Output Routing Pool Showing Bypass

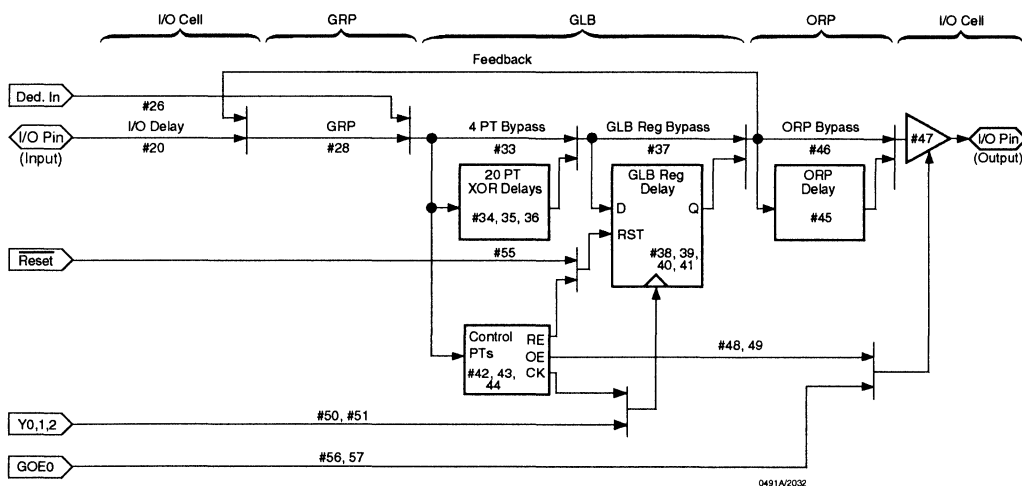


Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in figure 8. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (figure 8). Critical timing paths

are shown in figure 8, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. (External timing parameters are tested and guaranteed on every device).

Figure 8. pLSI and ispLSI 2032 Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp} + t_{ptck(min)}) \\
 &= (\#24 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 2.2 \text{ ns} &= (1.0 + 1.3 + 4.7) + (0.8) - (1.0 + 1.3 + 3.3) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 1.6 \text{ ns} &= (1.0 + 1.3 + 3.3) + (3.0) - (1.0 + 1.3 + 4.7) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{iobp} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 8.8 \text{ ns} &= (1.0 + 1.3 + 3.3) + (0.7) + (1.3 + 1.2)
 \end{aligned}$$

1. Calculations are based upon timing specs for the pLSI and ispLSI 2032-135L

Notes

3000 Family

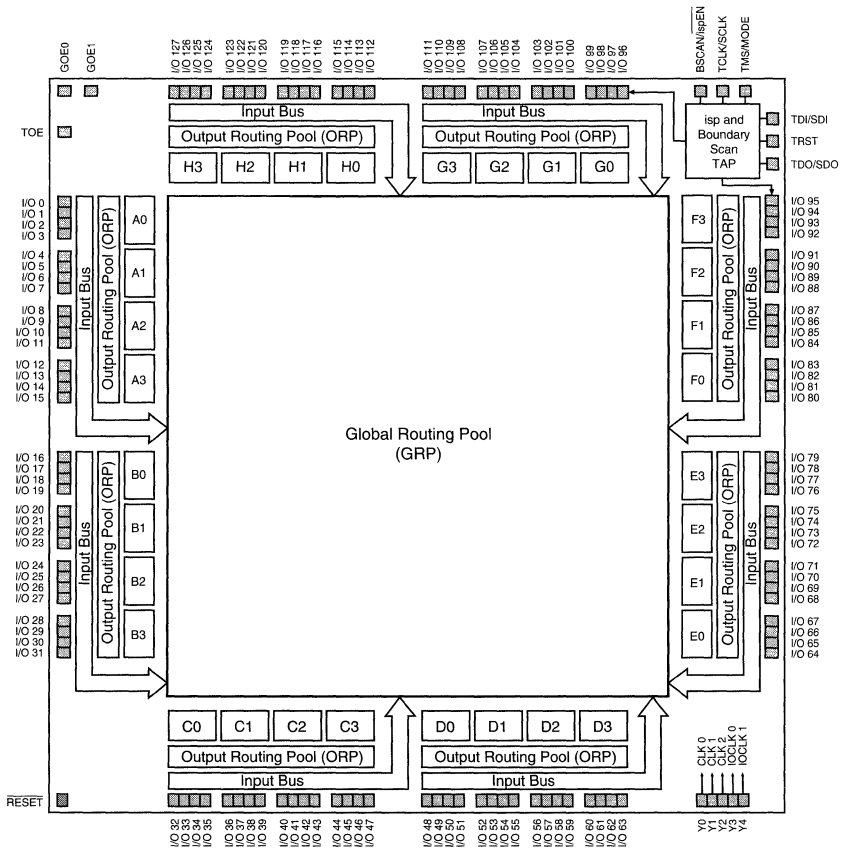
Architectural Description

pLSI and ispLSI 3000 Family Introduction

The basic unit of logic of the pLSI and ispLSI 3000 family is closely related to that of the pLSI and ispLSI 1000 family. However, there are some notable architectural

differences: Boundary Scan, Megablock and GLB structure, Global clock structure, and I/O cell structure. A functional block diagram of the ispLSI 3256 device is shown in figure 1. The architectural differences are described in the following sections.

Figure 1. ispLSI 3256 Functional Block Diagram



0139Aisp3256

3000 Family Architectural Description

Generic Logic Block

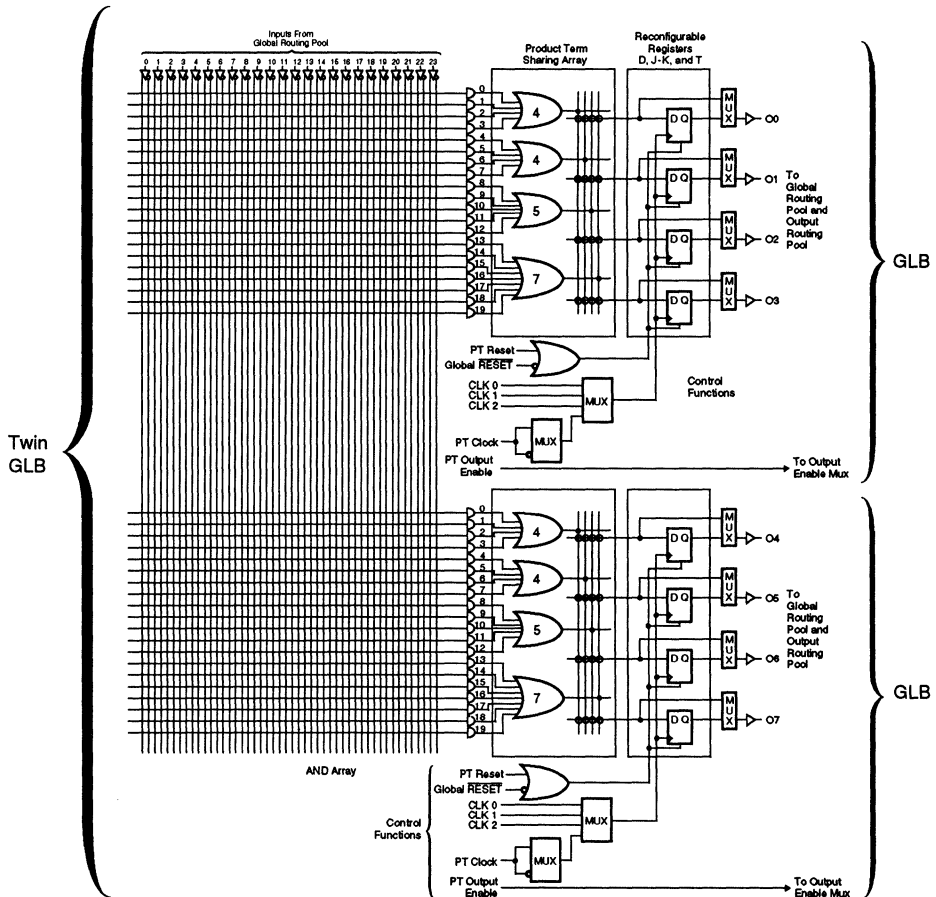
The Twin GLB is the standard logic block of the Lattice pLSI and ispLSI 3000 Family. This Twin GLB has 24 inputs, eight outputs and the logic necessary to implement most standard logic functions. The internal logic of the Twin GLB is divided into four separate sections: The AND Array, the Product Term Sharing Array, the Reconfigurable Registers, and the Control section.

The AND array consists of two 20 Product Term Sharing Arrays which can produce the logical sum of any of the 24 Twin GLB inputs. These inputs all come from the GRP, and are either feedback signals from any of the 32 Twin GLBs or inputs from the external I/O Cells. All Twin GLB

input signals are available to the Product Terms in both the logical true and complemented forms which makes Boolean logic reduction easier.

The two Product Term Sharing Arrays (PTSA) take the 20 Product Terms each and allocate them to four Twin GLB outputs. There are four OR gates, with four, four, five and seven inputs respectively. The output of any of these gates can be routed to any of the four Twin GLB outputs, and if more Product Terms are needed, the PTSA can combine them as necessary. If the user's main concern is speed, the PTSA can use a bypass circuit with four Product Terms to increase the performance of the cell. This can be done to any or all of the eight outputs of the Twin GLB.

Figure 2. Twin GLB: Product Term Sharing Array



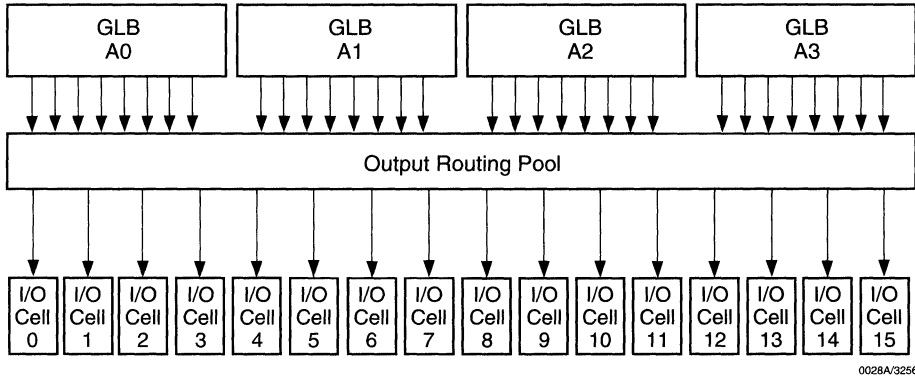
3000 Family Architectural Description

Megablock Structure

Four Twin GLBs make up a Megablock. Each GLB has a maximum fan-in of 24 inputs, and no dedicated inputs associated with any Megablock. A GLB has eight asso-

ciated outputs. A total of 32 GLB outputs are fed to the ORP. However, only 16 out of the 32 outputs feed to 16 I/O cells. The Megablock structure is shown in figure 3.

Figure 3. pLSI and ispLSI 3000 Family Megablock Block Diagram

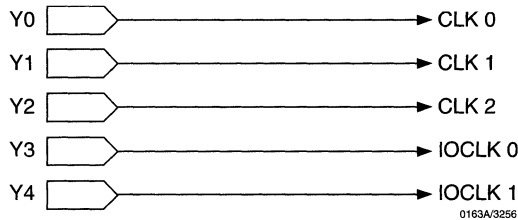


Global Clock Structure

The global clock structure is made up of five global clock input pins, Y0, Y1, Y2, Y3, and Y4. This is shown in figure 4. Three of the clock pins are dedicated for GLB clocks and the remaining two clock pins are dedicated for I/O register clocks. The clock GLB generation network which

is designed into the 1000 device family has been removed so all input clock signals are fed directly to the GLB clock input via a clock multiplexer. The GLB global clocks do not have inversion capability, but the product term clock does have inversion capability before it reaches the clock multiplexer.

Figure 4. pLSI and ispLSI 3000 Family Global Clock Structure



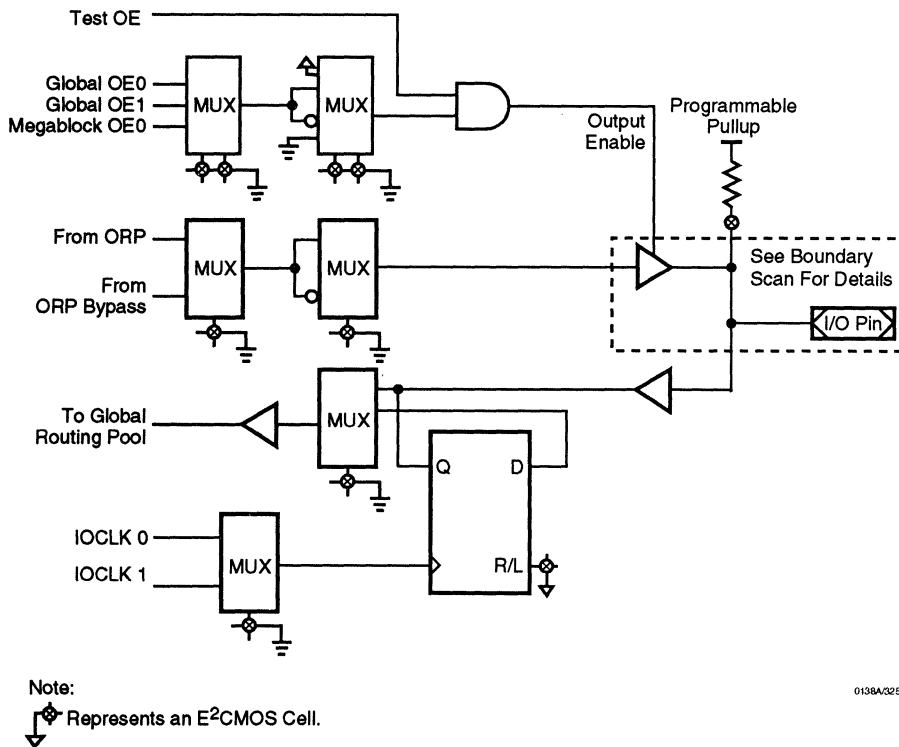
3000 Family Architectural Description

I/O Cells

The I/O cell structure architecture remains nearly the same as the 1000 Family as illustrated in figure 5. Each I/O cell now contains Boundary Scan Registers as shown in figure 8. An input pin has only one scan register as shown in figure 9. A global test OE signal is hardwired to

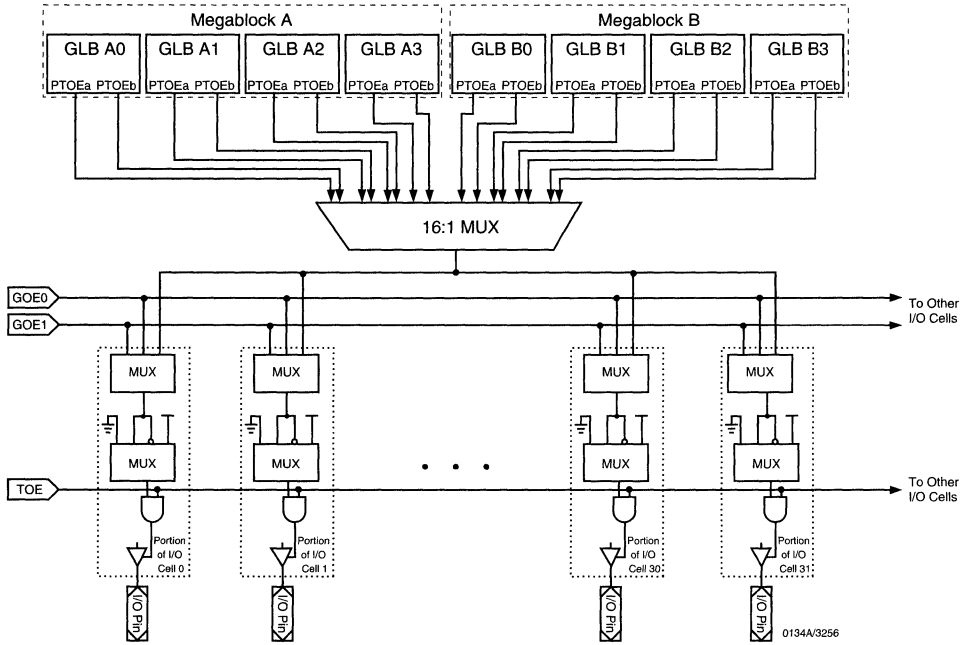
all I/O cells and is useful to perform static testing of all the 3-state output buffers within the device. In addition to the test OE signal, two global OEs are connected to all I/O pins. The product term OE is shared between two Megablocks resulting in twice the GLBs being able to use a single OE signal. The Megablock OE signal and global OE signal are fed to an OE multiplexer. The OE signals, with the exception of the test OE, have inversion capability after going through the OE multiplexer as shown in figure 6.

Figure 5. pLSI and ispLSI 3000 Family I/O Cell Architecture



0138A/0256

Figure 6. pLSI and ispLSI 3000 Family Output Enable Controls

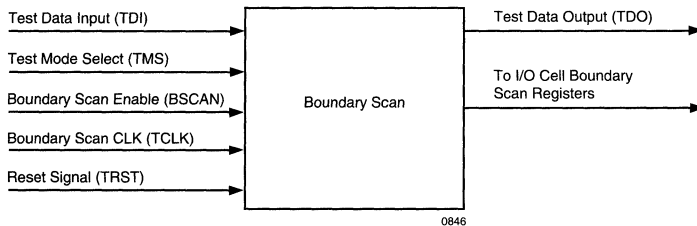


Boundary Scan

Boundary Scan (IEEE 1149.1 compatible) is a test feature incorporated within the device to provide on-chip test capabilities during PCB testing. Five input signal pins, BSCAN, TDI, TCLK, TMS, TRST, and one output signal pin, TDO, are associated with the boundary scan logic cells. These signal pins occupy the same dedicated signal pins used for ISP programming. The signal BSCAN is associated with the ispEN pin, TDI corresponds to the SDI pin, TCLK corresponds to the SCLK pin, TMS corre-

sponds to the MODE pin, and TDO corresponds to the SDO pin. When ispEN is asserted low, the MODE, SDI, SDO, and SCLK options become active for ISP programming. Otherwise, BSCAN, TDI, TCLK, TMS, TDO, and TRST options become active for boundary scan testing of the device. The boundary scan block diagram is shown in figure 7. TDI is the test data serial input, TCLK is the boundary scan clock associated with the serial shift register, TMS is the test mode select input, TDO is the test data output, and finally TRST is the reset signal pin.

Figure 7. Boundary Scan Block Diagram



3000 Family Architectural Description

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset (TRST) and Test Clock (TCK).

The TAP controls the operation of the Boundary Scan Registers after decoding the instruction code sent to the instruction register (see table 1).

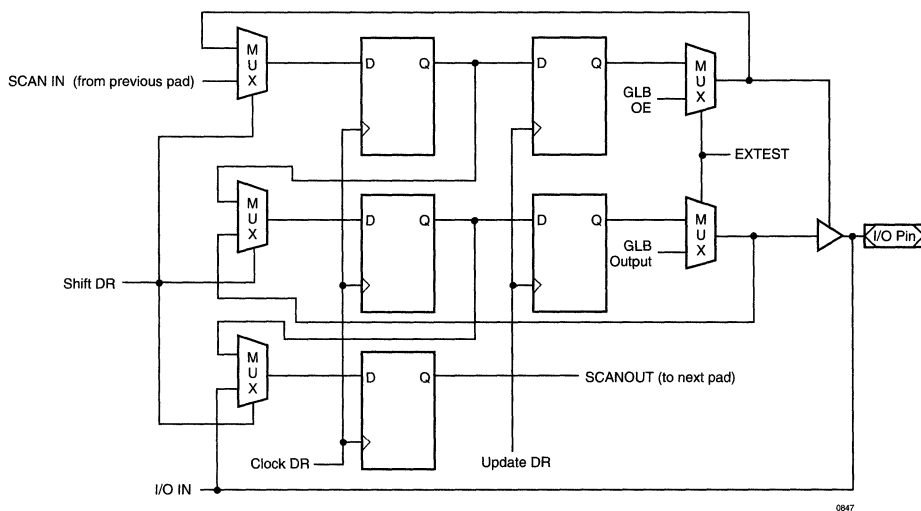
The Boundary Scan Registers for the I/O cells are shown in figure 8. As illustrated in the figure, each I/O cell contains 3 registers, 2 latches and 5 multiplexers to

implement the ability to capture the state of the I/O cell or set the state of the output path of the cell or function as a conventional I/O cell.

The Boundary Scan Registers required for an input only cell are shown in figure 9. An input only cell can only have its state captured, which only requires one MUX and one register.

All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells are connected in the following order: TDI to IO63 thru IO32 to Y4, Y3, Y2, Y1, Reset, TOE, GOE1, GOE0, Y0, IO31 thru IO0 to IO64 thru IO127 to TDO.

Figure 8. Boundary Scan Registers for I/O Cells



3000 Family Architectural Description

Figure 9. Boundary Scan Registers for an Input Only Cell

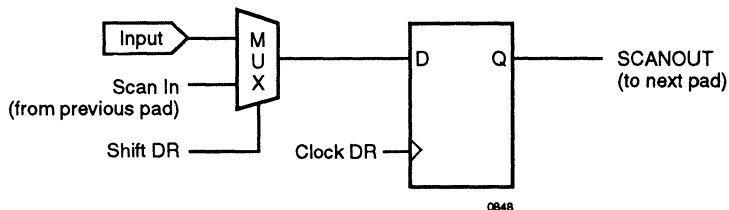


Table 1. Boundary Scan Instruction Codes

Instruction Name	Code	Description
SAMPLE/ PRELOAD	10	Loads and shifts data into BScan registers
EXTEST	00	Drives external I/O with BScan registers
BYPASS	11	Bypasses registers of selected device(s)

Note: LSB shifts in 1st.

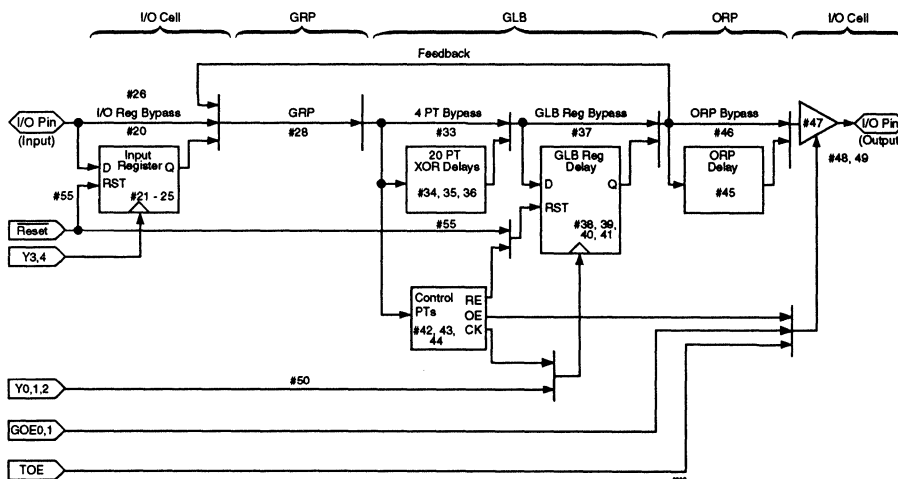
Table 10-0006

Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in figure 10. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the

various delays together (figure 11). Critical timing paths are shown in figure 10, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. (External timing parameters are tested and guaranteed on every device).

Figure 10. pLSI and ispLSI 3256 Timing Model



3000 Family Architectural Description

Figure 11. Timing Calculation Example

Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

$$\begin{aligned}t_{su} &= \text{Logic} + \text{Reg su} - \text{Clock (min)} \\ &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\ &= (\#24 + \#31 + \#39) + (\#42) - (\#24 + \#31 + \#48) \\ 6.5 \text{ ns} &= (2 + 4 + 8.5) + (1.5) - (2 + 4 + 3.5) \\ t_h &= \text{Clock (max)} + \text{Reg h} - \text{Logic} \\ &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\ &= (\#24 + \#31 + \#48) + (\#43) - (\#24 + \#31 + \#39) \\ 8 \text{ ns} &= (2 + 4 + 7.5) + (9) - (2 + 4 + 8.5) \\ t_{co} &= \text{Clock (max)} + \text{Reg co} + \text{Output} \\ &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\ &= (\#24 + \#31 + \#48) + (\#44) + (\#49 + \#51) \\ 20 \text{ ns} &= (2 + 4 + 7.5) + (1.5) + (2 + 3)\end{aligned}$$

1. Calculations are based upon timing specs for the pLSI and ispLSI 3256-70L

ispLSI Architecture and Programming

ispLSI Programming Information

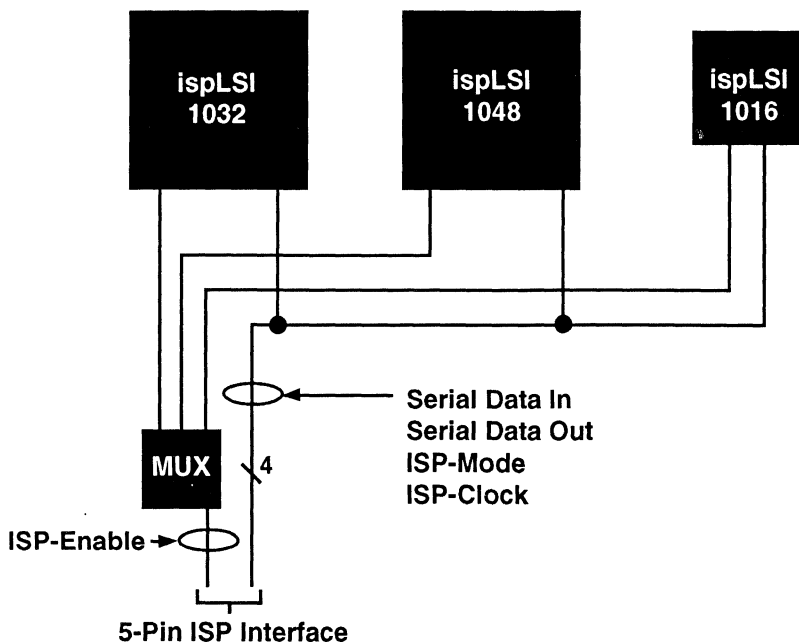
The following general programming information on the ispLSI (in-system programmable Large Scale Integration) devices describes how the internal state machine is implemented for programming and how to use the five programming interface signals to step through the state machine. The device specific information, such as timing and pin-outs, can be found in the individual data sheets. The programming information given in this section applies to all ispLSI devices.

Programming Overview

To distinguish between normal operation and programming, two modes are defined: normal mode and edit mode. Once the device is in edit mode, the entire programming operation of the device is controlled by the internal ISP state machine. The in-system programming enable (ispEN) signal controls the device operation modes.

The programming is controlled by the on-chip state machine via five programming interface signals. The ispEN signal is used to enable and disable the four programming control signals which include Serial Data In (SDI), Mode (MODE), Serial Data Out (SDO) and Serial Clock (SCLK). When the device is in normal mode, the four programming control signal pins can be used as normal Dedicated Input Pins. Figure 1 illustrates one such possible configuration for programming multiple ispLSI devices. With this scheme the ispEN signal for individual devices is enabled separately and one device is placed in the edit mode at a time. Since the other devices are in the normal mode, they can continue to perform normal system functions. This simple scheme requires connecting all four programming control signal pins together and precludes their use as dedicated inputs for normal system functions. ispEN is the only programming interface signal that is dedicated to a pin.

Figure 1. ispLSI Programming Interface



ispLSI Architecture and Programming

Normal Mode

In Normal Mode the four programming control pins become Dedicated Input pins. By multiplexing the programming control pins, these programming control pins can have a normal input function during Normal Mode. Figures 2 illustrates how to utilize the four programming control signal pins for performing normal system functions. Internal to the device, the programming functions are completely isolated from the normal operating functions when the device is in Normal Mode. Keeping the $\overline{\text{ispEN}}$ signal high puts the device in Normal Mode. For simplicity, the four programming control pins can be left unused for normal input functions. These pins can be reserved for ISP by using the ISP switch in the development tools. By leaving these pins unused, the programming interface is simplified when the programming signals and the Normal Mode input signals are not multiplexed.

Edit Mode

Programming circuitry is enabled by driving the $\overline{\text{ispEN}}$ signal low which puts the device in Edit Mode. In Edit Mode, all the functional I/O pins and input pins that are not used during programming are 3-stated. With the exception of the SDO signal, the remainder of the programming interface signals are input signals. When multiplexing the programming interface signals, the input driving the SDO pin must be 3-stated to make sure that there is no signal contention. All programming is accomplished in the Edit Mode by controlling the programming state machine with the MODE and SDI signals. SCLK is used to clock programming data in and out through SDI and SDO pins. SDI has a dual role as one of the two control signals for the state machine and as the serial data input. To avoid any internal register data contentions, Lattice recommends that the device Reset pin be pulled to ground when the device is in Edit Mode.

Programming Interface

The five programming interface pins are $\overline{\text{ispEN}}$, SDI, MODE, SDO and SCLK. Once in Edit Mode, programming is controlled by SDI, MODE, SDO and SCLK signals. In Normal Mode, the programming control pins can be used as dedicated inputs to the device.

$\overline{\text{ispEN}}$ is an active low, dedicated enable pin, which enables the four programming control pins when it is driven low (V_{IL}) and disables the programming control pins when it is driven high (V_{IH}). All other I/O pins are 3-stated during Edit Mode and pulled up by the internal active pull-up resistors (equivalent to 100K Ω).

SDI performs two different functions. First, as the input to the serial shift register and second, as one of the two control pins for the programming state machine. Because of this dual role, SDI's function is controlled by the MODE signal. When MODE is low SDI is the serial input to the shift registers and when MODE is high SDI becomes the control signal. Internal to the device, the SDI is multiplexed to address shift register, high order data shift register and low order data shift register. The different shift instructions of the state machine determine which of these shift registers gets the input of the SDI.

The MODE signal combined with the SDI signal controls the programming state machine. This signal connects in parallel to all ispLSI devices.

SCLK is the serial shift register clock that is used to clock the internal serial shift registers. A low-to-high (positive) clock transition clocks the state machine. It also connects in parallel to all ispLSI devices. Similar to SDI, the shift instructions determine which of the shift registers are clocked for the data input from SDI.

SDO is the output of the serial shift registers. The selection of the shift register is determined by the state machine's shift instruction. In the flow through instruction and when MODE is driven high, SDO connects directly to SDI, and bypasses the device's shift registers. Since this is the only output pin for the Edit Mode, this signal will drive the external devices that are connected to this pin.

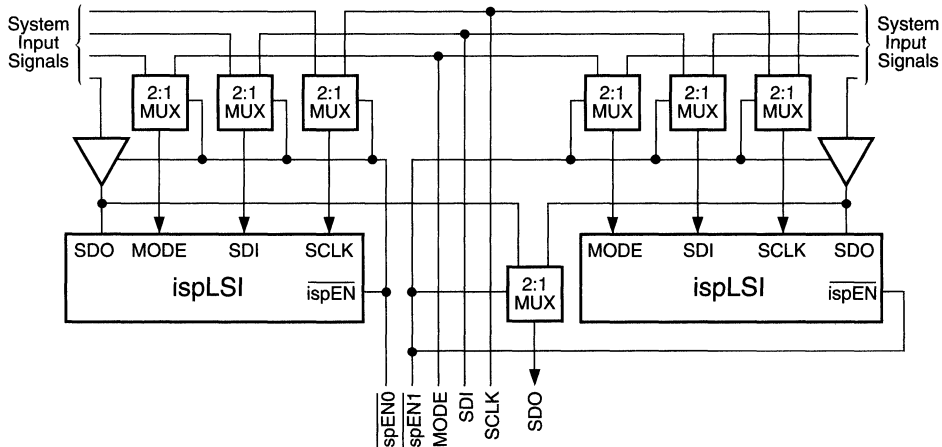
Programming Details

Programming is completely controlled by the state machine, once the device is in the Edit Mode. The state machine consists of three states, in which all programming related operations are performed. In order to run these programming operations, five bit instructions are defined (see table 2). Each instruction is then shifted into the device in one of the three states and executed in another state. The initial state of the state machine is used when the device is idle during edit, or to shift out the eight bit device identification code.

The following sections describe the general information about the critical timing parameters, state machine, state machine instructions, and device layout that apply to all the ispLSI devices. Any device specific information like the size of the shift registers and the device specific timing information can be found in the individual device data sheets.

There are various ways of programming the ispLSI devices. The easiest is to dedicate the ISP programming pins only for the programming functions. With dedicated ISP pins, one can either program the devices in a serial daisy chain configuration (figure 1) or in a parallel programming configuration where the programming signals are multiplexed. The parallel multiplexed programming method gives the user another advantage of being able to use the programming pins for system functions. Figure 2 illustrates a multiplexing scheme which allows the user to control the ISP programming through multiple ispEN signals. The multiple ispEN signals not only control the ispEN inputs of the ispLSI devices, but also is the control signal for multiplexing the functional signals and the ISP programming signals. The ISP programming signals MODE, SDI and SCLK function as inputs for normal functional mode as well as the ISP programming mode. SDO, however, functions as an input in normal functional mode and as an output in ISP programming mode. Figure 2 also shows the difference in controlling these different programming signals.

Figure 2. The Scan and Multiplex Programming Mode



ispLSI Architecture and Programming

Critical Timing Parameters

When programming ispLSI devices, there are several critical timing parameters that must be met to ensure proper programming. The two most critical parameters are the programming pulse width (t_{pwp}) and the bulk erase pulse width (t_{bew}). These pulse widths determine the programming and erasing of the E² cells. Figure 4 shows these critical program and erase timing specifications.

Along with the two programming and erasing specification, the following timing specifications must also be met.

t_{isp} - Specifies the time it takes to get into the ISP mode after \overline{ispEN} signal is activated or the time it takes to come out from the ISP mode after the \overline{ispEN} becomes inactive.

t_{su} - Set up time of the control signals before the SCLK or the set up time of input signals against other control signals where applicable.

t_h - Hold time of the control signal after the SCLK. It also applies to the same input signals from the set up time.

t_{clkL} , t_{clkH} - Minimum clock pulse width.

t_{pww} - Verify or read pulse width. The minimum time requirement from the rising clock edge of verify/load instruction execution to the next rising clock edge (see figure 4).

t_{rst} - Power on reset timing requirement. t_{rst} must elapse after power up before any operations are performed on the device.

All the programming timing parameters are summarized in the timing diagram (see figure 5).

Figure 4. Program, Verify & Bulk Erase Timing

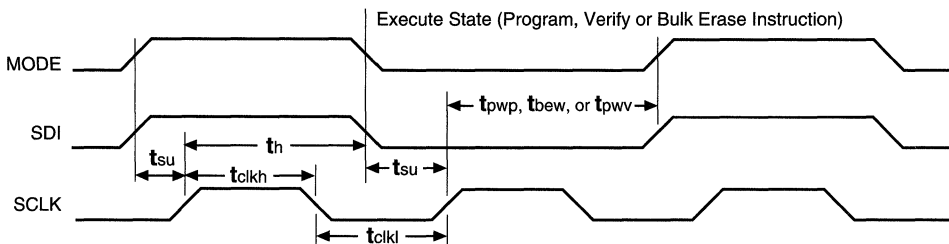


Figure 5. ISP Programming Timing Requirements

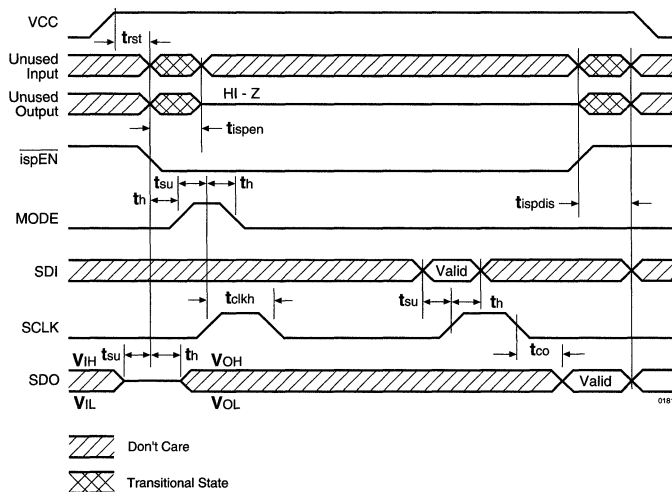
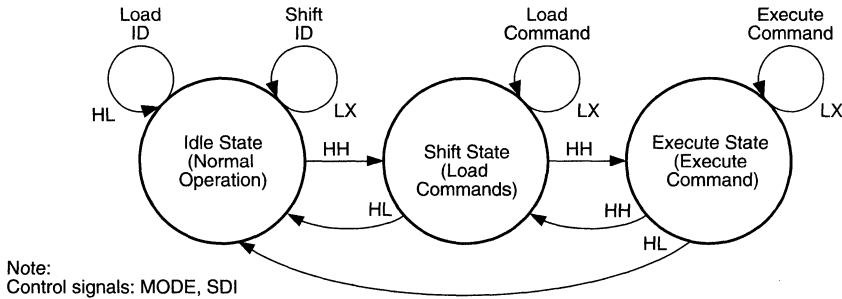


Figure 6. Programming State Machine



State Machine Operation

The state machine has three states to control programming and uses the MODE and SDI signals as inputs for each state. Based on these input signals, the state machine makes decisions to either stay in the same state or to branch to another state. The three states are Idle/ID State, Command Shift State and Execute State. The programming state machine diagram in figure 6 shows the three states and the logic levels of the control signals needed to force each transition state.

Idle/ID State

The Idle/ID state is the first state which is active when the device gets into the Edit Mode. The state machine is in the Idle/ID state when the device is idle, in the Edit Mode, or when the user needs to read the device identification. The eight bit device identification is loaded into the shift register by driving MODE high, SDI low and clocking the state machine with SCLK. Once the ID is loaded, it is read out serially by driving MODE low. Notice that when reading the device ID serially, SDI can either be high or low (don't care) and the state machine needs only seven clocks to read out eight bits of ID. The default state for the control signals is MODE high and SDI low. State transition to Command Shift State occurs when both MODE and SDI are high while state machine gets a clock transition. Table 1 lists the eight bit device ID's for all the ispLSI devices. As with most shift registers the Least Significant Bit (LSB) of the ID gets shifted out from the SDO first.

Command Shift State

This state is strictly used for shifting in the command instructions into the state machine. The entire five-bit instruction set is listed in the next section. When MODE is low and SDI is don't care in the Command Shift State,

Table 1. ispLSI Device ID Codes

Device	MSB	LSB
ispLSI 1016	00000001	
ispLSI 1024	00000010	
ispLSI 1032	00000011	
ispLSI 1048	00000100	
ispLSI 1048C	00000101	
ispLSI 2032	00010101	
ispLSI 3256	00100010	

SCLK shifts the instruction into the state machine. Once the instruction is shifted into the state machine, the state machine must transition to the Execute State to execute the instruction. Driving both MODE and SDI high and applying the clock will transfer the state machine from the Command Shift State to Execute State. If needed, the state machine can move from Command Shift State to Idle/ID State by driving MODE high and SDI low.

Execute State

In the Execute State, the state machine executes instructions that are loaded into the device in the Command Shift State. For some instructions, the state machine requires more than one clock to execute the command. An example of this multiple clock requirement is the address or data shift instruction. The number of clock pulses required for these instructions depends on the device shift register sizes (refer to the ISP programming section of the data sheet). When executing instructions such as Program, Verify or Bulk Erase, the necessary timing requirements must be followed to make sure that the commands are executed properly. For specific timing information refer to the individual data sheets.

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To execute a command, the MODE is driven low and SDI is "don't care." For multiple clock instructions the control signals must remain in the same state throughout the duration of the execution. MODE high and SDI high will take the state machine back to the Command Shift State and MODE high and SDI low will take the state machine to the Idle/ID State.

Instructions

Table 2 lists the instructions that can be loaded into the state machine in the Command Shift State and then executed in the Execute State. Notice that reading the

device identification is done during the Idle/ID State and does not require an instruction.

While it is possible to erase the individual arrays of the device, it is recommended that the entire device be erased (UBE) and programmed in one operation. This Bulk Erase operation should precede every programming cycle as an initialization.

When a device is secured by programming the security cell (PRGMSC), the on-chip verify and load circuitry is disabled. Securing of the device should be done as the last procedure after all the device verifications have been completed. The only way to erase the security cell is to perform a bulk erase on the device.

Table 2. State Machine Instruction Set

Instruction	Operation	Description
00000	NOP	No operation performed
00001	ADDSHFT	Address Register Shift: Shifts address into the address shift register from SDIN.
00010	DATASHFT	Data Register Shift: Shifts data into or out of the data serial shift register.
00011	UBE	User Bulk Erase: Erase the entire device.
00100	GRPBE	Global Routing Pool Bulk Erase: Bulk erases the GRP array only.
00101	GLBBE	Generic Logic Block Bulk Erase: Bulk erases all the GLB array only.
00110	ARCHBE	Architecture Bulk Erase: Bulk erases the architecture array and I/O configuration only.
00111	PRGMH	Program High Order Bits: The data in the data shift register is programmed into the addressed row's high order bits.
01000	PRGML	Program Low Order Bits: The data in the data shift register is programmed into the addressed row's low order bits.
01001	PRGMSC	Program Security Cell: Programs the security cell of the device.
01010	VER/LDH	Verify/Load High Order Bits: Load the data from the selected row's high order bits into the data shift register for verification.
01011	VER/LDL	Verify/Load Low Order Bits: Load the data from the selected row's low order bits into the data shift register for verification.
01100	GLBPRLD	Generic Logic Block Preload: Preloads the registers in the GLB with the data from SDIN. All registers in the GLB form a serial shift register. Refer to device layout section for details.
01101	IOPRLD	I/O Preload: Preloads the I/O registers with the data from SDIN. All registers in the I/O cell form a serial shift register (the same order as GLB registers).
01110	FLOWTHRU	Flow Through: Bypasses all the internal shift registers and SDOUT becomes the same as SDIN.
10010	VE/LDH	Verify Erase/Load High Order Bits: Load the data from the selected row's high order bits into the data shift register for erased verification.
10011	VE/LDL	Verify Erase/Load Low Order Bits: Load the data from the selected row's low order bits into the data shift register for erased verification.

Device Layout

The purpose of knowing the device layout is to be able to translate the JEDEC format programming file into the serial data stream format for programming ispLSI devices. Two main factors determine how the translation is implemented: the length of the address shift register and the length of the data shift register. The length of the address shift register indicates how many rows of data are to be programmed into the device. The length of the data shift register indicates how many bits are to be programmed in each row. Both registers operate on the First In First Out (FIFO) basis where the Least Significant Bit (LSB) of the data or address is shifted in first and the Most Significant Bit (MSB) of the data or address is shifted in last. For the data shift register, the low order bits and the high order bits are separately shifted.

Each ispLSI device has a predefined number of address rows and data bits needed to access its E²CMOS[®] cells during programming. The data bits span the columns of the E² array. From this information the number of programming cells (or fuses) are determined. Table 3 highlights the address and data shift register (SR) sizes for all ispLSI devices. The JEDEC file for these ispLSI devices will reflect the number of cells (fuses) seen in table 3. The total number of cells becomes critical if the programming patterns are to be stored in an on-board memory storage of limited capacity such as EPROM or PROM.

The L field in the JEDEC programming file indicates the first cell number of each row. The JEDEC standard requires that there is at least the beginning cell number L00000. L fields of the subsequent lines are optional. From this reference cell location all other cell locations can be determined. Zero in the cell location indicates that the E² cell in that particular location is programmed (or has a logic connection equivalent to a metal fuse being intact). A one (1) in the cell location indicates that the cell is erased (equivalent to a blown fuse). The fusemap operation in the Lattice software generates this JEDEC standard programming file.

Fuse Map to Device Conversion

One of the major elements needed to program an ispLSI device is the JEDEC fuse map in which the specific logic implementation is stored. While the ispCODE software takes care of these details, it is important to understand how this JEDEC fuse map is mapped onto the physical ispLSI device during programming. The physical layout of the fuse pattern begins with Address Row 0 and ends with the maximum Address Row N and is determined by the length of the Address SR as described in table 3. Spanning the Address Rows are the outputs of the High-Order Data SR and Low-Order Data SR, as described in table 4. Programming fuses on a given row are enabled by a "1" within the Address Shift Register for the appropriate row and the use of state machine instructions that selectively operate on the High-Order Data SR or the Low-Order Data SR. For example, the PRGMH instruction programs the High-Order data bits within the device for the selected Address Row and the PRGML instruction programs the Low-Order data bits (table 2 lists the ISP state machine instructions). Referring to figure 7, the starting cell (L00000) of the JEDEC fuse map shifts into the device at the physical location corresponding to Address Row 0, High-Order Data SR bit 0. n and m in the figure refer to the Address SR length and the Data SR length, respectively, of the device (refer to table 3). A series of sequential shifts eventually results in the last cell location (Total # of Cells - 1) of the JEDEC fuse map shifting into Address Row (n-1), Low-Order Data SR bit (m-1) on the actual device.

The ispCODE Software routines make use of a bit packed data format, called ispSTREAM[™], to transfer data between the JEDEC fuse map and the physical device locations. The JEDEC fuse map can be translated into ispSTREAM using the isp_jedtoisp function and the ispSTREAM format can be translated into a JEDEC fuse map using the isp_istptojed function.

Command Stream

The first step of programming the ispLSI devices is to determine the type of device to be programmed. This can be done by reading the eight-bit device ID of all the devices.

Table 3. ispLSI Address and Data Shift Register and Total Cell Summary

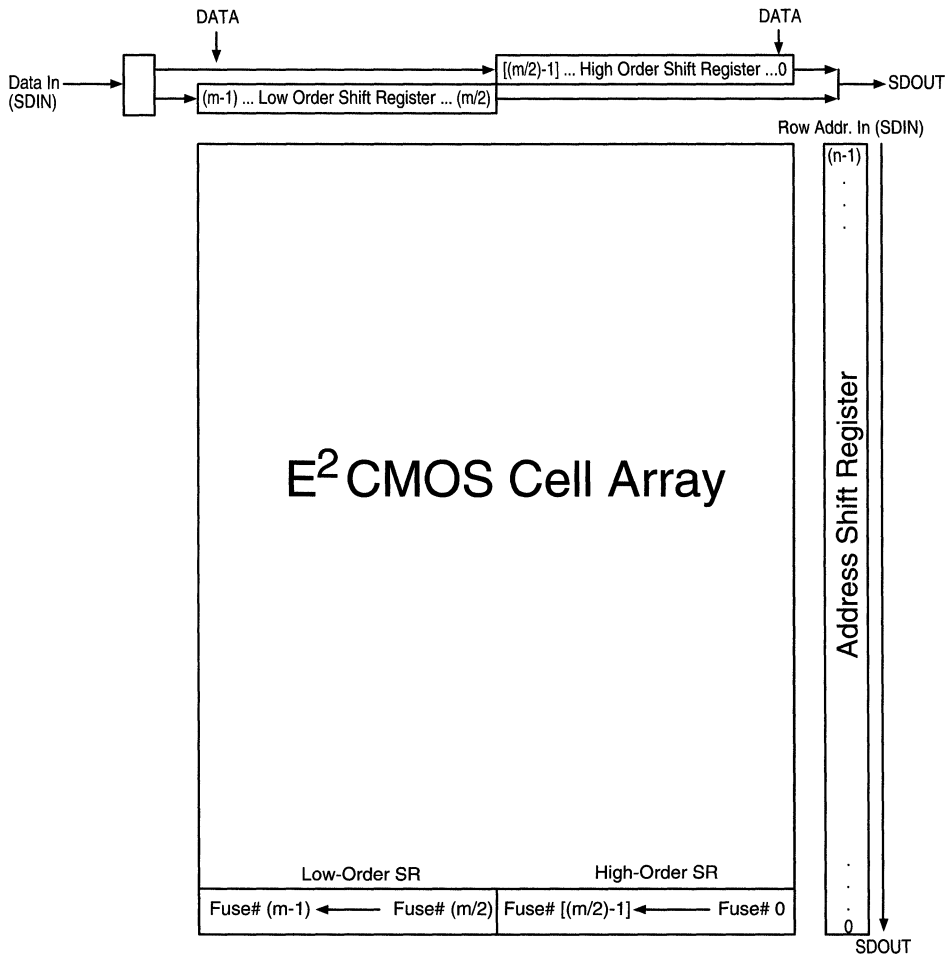
	ispLSI 1016	ispLSI 1024	ispLSI 1032	ispLSI 1048	ispLSI 2032	ispLSI 3256
Address SR Length	96	102	108	120	102	180
Data SR Length/Address	160	240	320	480	80	676
Total Number of Cells	15,360	24,480	34,560	57,600	8,160	121,680

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Table 4. Summary of Data Shift Register Bits

Data SR Bits	ispLSI 1016	ispLSI 1024	ispLSI 1032	ispLSI 1048
High Order Data SR LSB	0	0	0	0
High Order Data SR MSB	79	119	159	239
Low Order Data SR LSB	80	120	160	240
Low Order Data SR MSB	159	239	319	479
Data SR Size (Bits)	160	240	320	480

Figure 7. ispLSI Device to Fuse Map Translation



By keeping the SDI to a known level (either high or low), the ID shift can be terminated when a sequence of eight ones or eight zeros is read. From the device ID the serial bit stream for programming can be arranged. A typical programming sequence is as follows:

- 1) ADDSHFT command shift
- 2) Execute ADDSHFT command
- 3) Shift address
- 4) DATASHFT command shift
- 5) Execute DATASHFT command
- 6) Shift high order data
- 7) PRGMH command shift
- 8) Execute PRGMH
- 9) DATASHFT command shift
- 10) Execute DATASHFT command
- 11) Shift low order data
- 12) PRGML command shift
- 13) Execute PRGML
- 14) Repeat from 1) until all rows are programmed.

Diagnostic Register Preload

This section explains how to preload all of the buried registers and I/O registers to a known state to test the logic function of a device. The process of loading the register will reduce the time necessary to test a function that is deeply embedded in the logic of an ispLSI device.

To preload a device the ISP state machine is used with the same five pins that are used for programming ispEN, SDI, MODE, SDO and SCLK. Two state machine commands

preload all of the registers: GLBPRLD and IOPRLD. These two commands enable two different shift registers and enable data to be loaded into the device. The process of loading data into the device is:

1. Enter the ISP programming mode by driving $\overline{\text{ispEN}}$ pin to Vil.
2. Load command GLBPRLD and execute command (wait one t_{clk}).
3. Clock in the GLB preload data.
4. Load the command IOPRLD and execute the command (wait one t_{clk}).
5. Clock in the I/O preload data.
6. Return to the normal mode by driving the $\overline{\text{ispEN}}$ pin to Vih.
7. Execute the vectors.

When preloading a device it is important to keep the dedicated input pins (RESET, Y0, Y1, Y2 and Y3) in the same state as the previous vector. If the state of these pins is switched during the preload sequence the register may not load correctly and the results cannot be guaranteed.

The preload feature is not recommended on designs which use product term resets. The asynchronous nature of these resets can cause registers to be reset unexpectedly, therefore the results cannot be guaranteed.

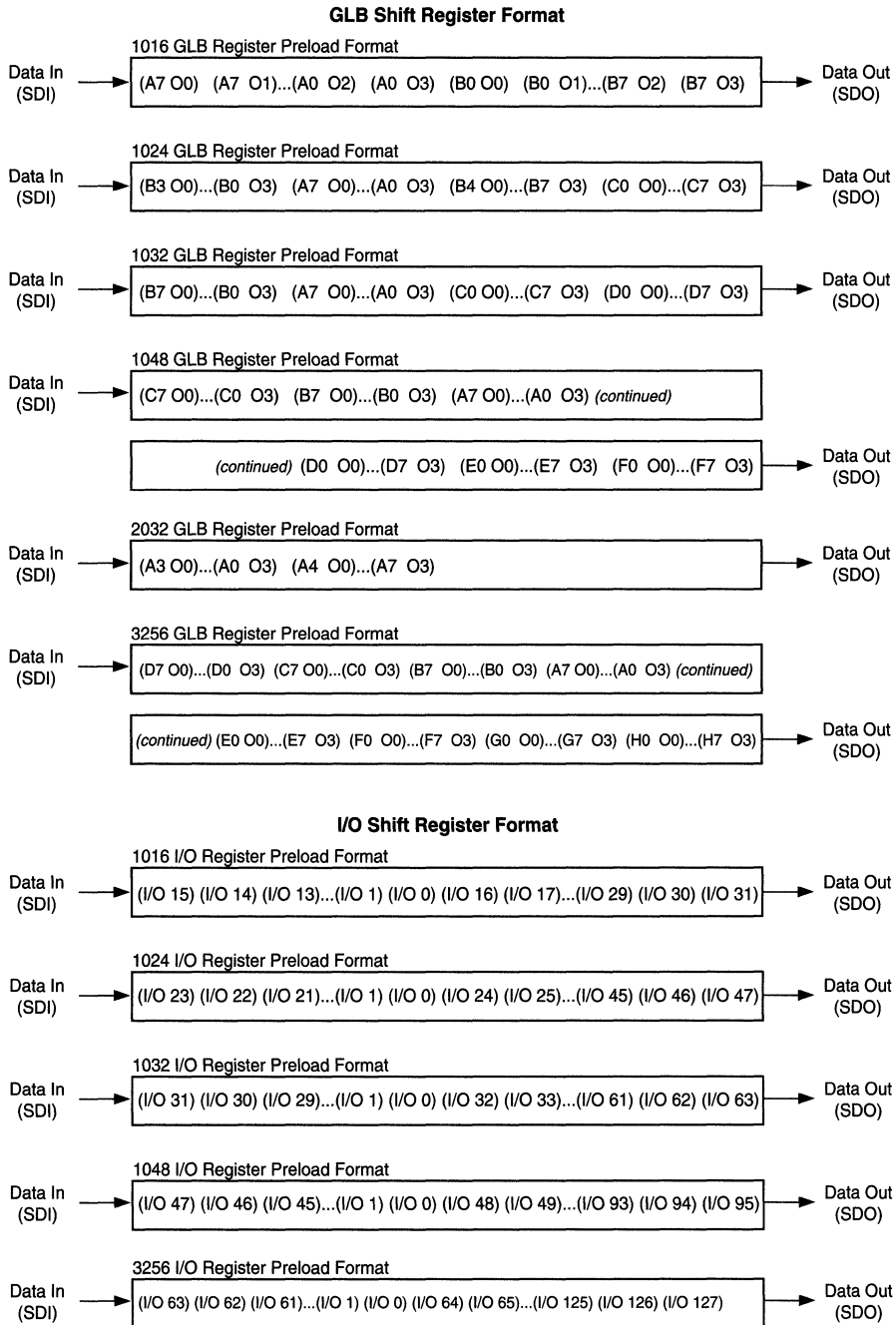
There are two shift registers used to preload an ispLSI device, the GLB shift register and the I/O shift register (see table 6). The data format for both devices is shown in figure 9. The GLB registers are listed with their outputs (i.e. (A7 00) indicating output 0, of GLB A7).

Table 6. Preload Shift Registers

Device	GLB Shift Reg. Length	I/O Shift Reg. Length
ispLSI 1016	64 bits	32 bits
ispLSI 1024	96 bits	48 bits
ispLSI 1032	128 bits	64 bits
ispLSI 1048	192 bits	96 bits
ispLSI 2032	32 bits	N/A
ispLSI 3256	256 bits	128 bits

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Figure 9. GLB Shift Register and I/O Shift Register Format



ISP Programming Support

To assist users in implementing the ISP programming, Lattice provides the isp Engineering Kit hardware and ispCODE C language software routines which implement the basic ISP functions for programming. The Lattice ISP programming support uses the PC parallel port to program the devices.

isp Engineering Kit Hardware Definition

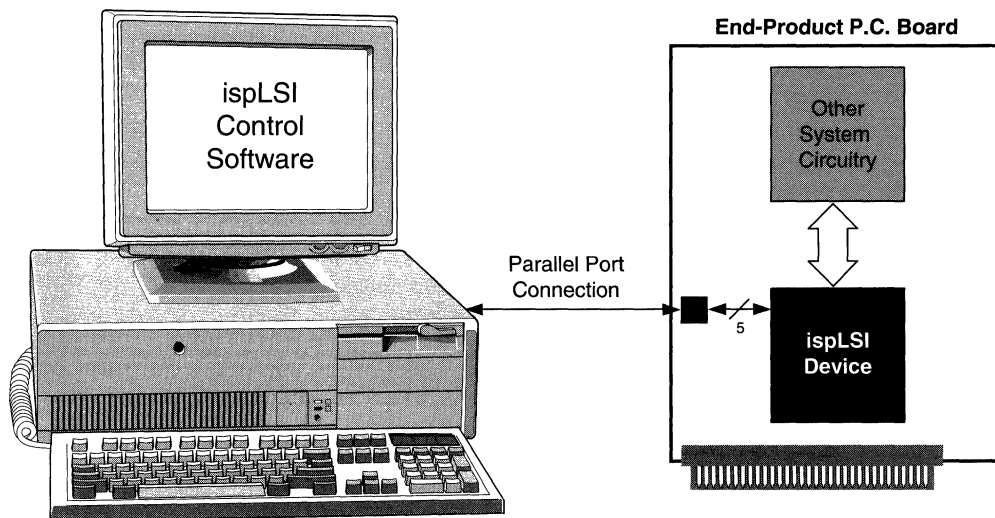
Lattice provides both a PC-based (Model 100) and a Sun Workstation-based (Model 200) isp Engineering Kit. PC-based, parallel I/O port programming interface implementation is explained in this section. For details on the Model 200 refer to the Model 200 isp Engineering Kit datasheet. The main function of this ispLSI programming interface is to provide four properly timed programming signals and the ispEN signal to the device. The PC parallel port is used in the isp Engineering Kit to provide these programming signals. The signals driven by the parallel port can be used either by the Lattice isp Programming Module (part of isp Engineering Kit Model 100) or on the

system board if the circuit board is built with provisions to connect the ISP programming signals to the appropriate traces.

In the case of users using the PC serial port as the I/O port for programming, the serial data must be converted by additional circuitry into the appropriate programming signals. There must also be timing circuitry that translates the serial instructions into timed ISP programming signals. This section only discuss the parallel port interface. Lattice's isp Engineering Kit Model 200 supports serial port programming.

In order to use the PC parallel port, the parallel port operation must be defined properly. After defining the port, it is just a matter of developing the programming software to read and write from the parallel port. To guarantee the signal integrity and drive capability, a 74HC367 buffer should be directly connected at the parallel port's DB25 connector. Figure 11 defines the parallel port DB25 pins and the associated ISP programming signals. The global RESET signal is also provided to ensure a proper register reset after programming.

Figure 10. Configuring an ispLSI Device from a Remote System



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The buffer then drives the cable that connects the output of the buffer to the ISP pins of the device. It is important to keep the cable length to a minimum to reduce the loading on the signal drivers. Since ispEN, SDI, SCLK and MODE are inputs to the ispLSI device, they are being driven by the buffer connected to the parallel port. SDO, on the other hand, is an output signal which the ispLSI device has to drive. If the load on the SDO signal is more than a minimum length cable and the parallel port input, it is recommended that the user provide a buffer on the circuit board to ensure signal integrity.

For the parallel port interface, the software must access the proper parallel port address. Once the port is defined, the data transfer is accomplished by simply reading from the port and writing to the port. The software must also guarantee proper timing between the ISP programming signals. When the programming software is executed, most of the shorter hardware timing requirements are automatically met due to the relatively long instruction execution times. The programming pulse width (tpwp) and bulk erase pulse width (tbew), which are in the 40ms to 200ms range, are the hardware timings that typically require wait states in the software. The example functions in the ispCODE illustrates reading of the computer's timer chip to generate these wait states.

Based on the programming pulse width requirement, the total programming time can be estimated. Since the shifting the address and data is relatively small compared to the programming time, the total programming time can be estimated by the following formula.

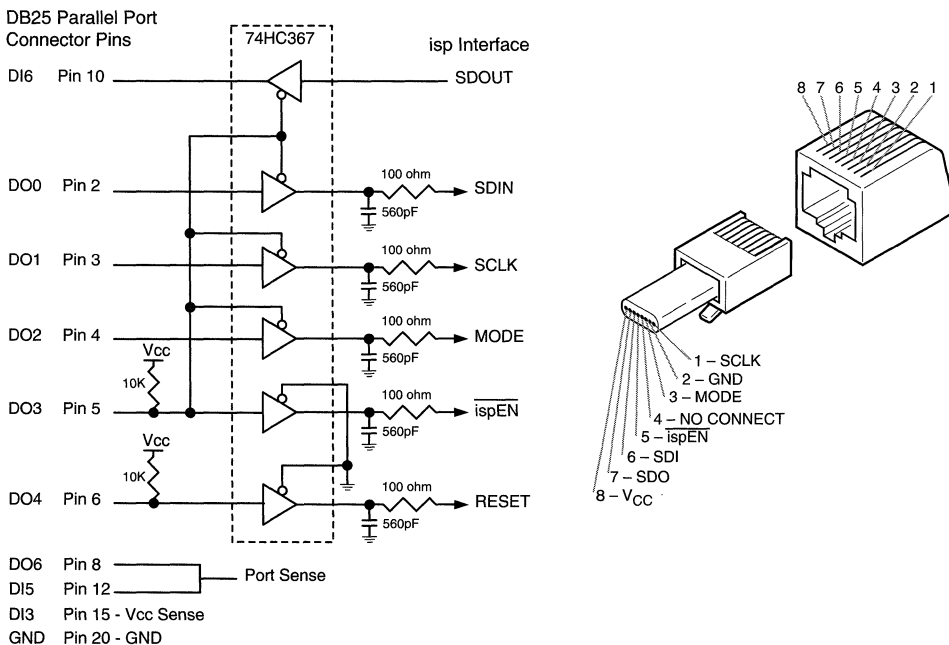
$$\text{Total Programming Time} = \text{Address SR Length} \times 2 \times \text{tpwp}$$

Assuming that the programming pulse width (tpwp) is 100ms, the total programming time for the ispLSI 1048 is approximately 24 seconds.

Microprocessor-Based Programming

Similar to PC-based I/O port controlled programming, a processor or a microprocessor can be used to directly supply the ISP programming signals with minimum decoding logic and an optional storage device (see figure 12). The discussion in this section pertains to the implementation of ISP programming on a circuit board with a microprocessor. The discussion is based on the assumption that the patterns and the code are stored in EPROMs. Since an efficient use of storage is desirable, the bit packed ispSTREAM format will use the least amount of storage. The basic requirement here, again, is to supply properly timed ISP programming signals.

Figure 11. PC Parallel Port Buffer & RJ45 Connector Definition



Hardware Configuration

There are several ways to define the ISP programming hardware depending on the type of storage device and how the ispLSI devices are to be programmed. The hardware configuration shown in figure 13 uses an 8-bit wide EPROM to store the fuse maps and code. The patterns are then read from the EPROM by the microprocessor and converted into serial stream format. The ISP signals are driven from the decoder and I/O port which decodes the proper ISP read/write address space similar to the I/O port definition of the previous setup. Similarly, fuse map memory addresses must also be defined to be properly read from the EPROM.

Programming pattern storage requirements are directly dependent upon the ispLSI device type and which ISP functions must be executed by the microprocessor. Assuming the bit packed ispSTREAM format for the fuse map, the number of bytes required for each ispLSI device is simply the total number of cells divided by eight. In the case of ispLSI 1048, 7.2K bytes is required to store the JEDEC fuse map.

Similar to the parallel port interface, most hardware timing requirements can be satisfied by the software instruction execution time. Only the program, verify and bulk erase times requires the software to have wait cycles. Many microprocessor boards will not have a timer chip to time the wait states. However, the instruction execution times typically can be accurately estimated. Therefore, timing loops must be inserted into the instructions control critical hardware timing.

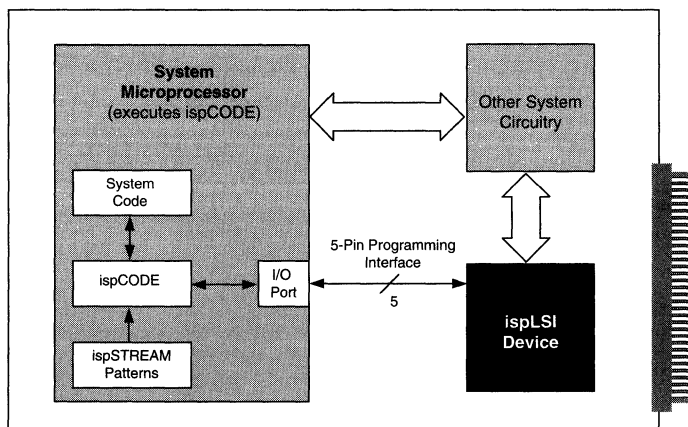
Software support for this case is very similar to the previous. Within the software, however, address spaces for the ISP read/write locations and the EPROM read locations must be defined. The storage space requirement for the code must also be determined if the code is going to reside in the storage device. Based on the ispCODE functions, the object code which is capable of executing basic ISP functions typically does not exceed 8K byte of memory. This memory requirement is directly proportional to the amount of ISP and user interface functions.

ISP Software Interface

In addition to the hardware interface, the ispCODE C language routines take care of the ispLSI programming software interface. The software interface must implement routines to read and write from the parallel port, to translate the JEDEC fusemap to and from the stream file format, and to toggle the ISP hardware signals connected at the output port. Predefined routines for these functions such as isp_program, isp_read, isp_verify, etc. are provided with the ispCODE. The ispLSI user only needs to integrate these routines into their overall system software.

The ispCODE routines makes use of the ispSTREAM bit packed data format to transfer data between the JEDEC fuse map and the physical device location. The JEDEC fuse map can be translated into ispSTREAM using the isp_jedtoisp function and the ispSTREAM format can be translated into a JEDEC fuse map using the isp_isptojed function. In addition to the fuse map translation routines, the ispCODE provides functions to check the device ID, to read and write the User Electronic Signature (UES), and to

Figure 12. Configuring an ispLSI Device from an On-Board Microprocessor



ispLSI Architecture and Programming

keep track of the program cycle counter. Refer to the ispCODE User Manual for more details.

ispLSI Device Special Features

In addition to transferring the fuse pattern into the ispLSI device with proper ISP timing, there are a few administrative functions that can make device programming more efficient when implemented in the ISP programming algorithm.

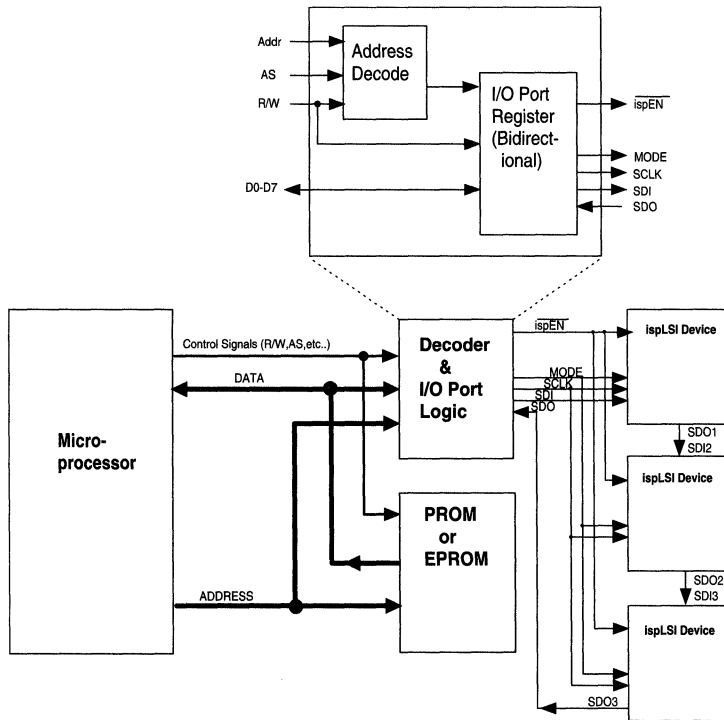
All ispLSI devices have hardwired device identification codes. These ID codes should be used to identify proper device and fuse map compatibility. The ID check should be run as the very first procedure before any device programming procedures. The ispCODE routines provided by Lattice include the `isp_get_id` function to facilitate this process.

The ispLSI devices also provide several programmable locations for the UES and program cycle counter. The UES can be used to identify which pattern is programmed into

the device. This is a very useful way of electronically identifying the devices and their programs, especially when the devices are secured. A 16-bit program cycle counter can be implemented within the reserved location, similar to the UES, to keep track of the number of program cycles which the device experiences to avoid exceeding the maximum programming cycle limit. UES and program cycle counter routines are provided as part of Lattice's ispCODE software.

One of the diagnostic features of the ispLSI devices is register preload. GLB and I/O registers become serial shift registers during the register preload command execution. Data can either be shifted into or out of these shift registers for system diagnostic functions. Special attention must be paid to the GLB and I/O clocks in order to use the register preload features properly. One must drive all GLB or all I/O clocks high throughout the execution of the GLB or I/O preload commands. This means that when defining the test pattern that uses the preload commands all GLB or all I/O clock polarities must be the same.

Figure 13. Microprocessor Board Configuration



Boundary Scan

The Lattice 3000 family of devices supports the IEEE 1149.1 Boundary Scan specifications. The following sections explain in detail how to interface to the devices through the Test Access Port (TAP), how the boundary scan registers are implemented within the devices, and the boundary scan instructions that are supported by the pLSI and ispLSI 3000 family

Test Access Port (TAP)

The test access port of the boundary scan is accessed through six interface signals. These interface signals have dual functions in the case of ispLSI 3000 family and are used for Boundary Scan interface and in-system programming interface signals. For the pLSI 3000 family the six interface signals are only used for the boundary scan TAP interface. Table 7 describes the interface signals.

The above mentioned six signals are dedicated for Boundary Scan use for the pLSI family of devices. Since ISP programming is accomplished through the same pins, five of the six signals have both Boundary Scan interface and ISP functions on the ispLSI devices. The TRST is the only signal that does not have a dual function. It is only used to reset the TAP controller state machine. The sequencing of test routines are governed by the TAP controller state machine. The state machine uses the TMS and TCK signals as its inputs to sequence the states. Figure 14A is the IEEE1149.1 specified state machine where the condition for the state transition is the state of the TMS input condition before TCK within a given state. The timing specification is also shown on figure 14B.

The main features of the TAP controller state machine consists of Test-Logic-Reset state to reset the controller and the Run-Test states. Two main components of the Run-Test states are Data Register (DR) control states and Instruction Register (IR) control states. Both of these register control states are organized in a similar manner where one can capture the registers, shift the register string, or update the registers. Capturing the DRs simply loads the DR with the data from the corresponding functional input, output, or I/O pins. The IR capture, on the other hand, loads the IRs with the previously executed instruction bits. Shift register states serially shifts the DR and IR. In the case of DR shift, the data is shifted according to the order of the inputs, outputs, and I/Os defined in the Boundary Scan section of each device data sheet. The IRs are shifted out from the least significant bit first. During update registers states, the DRs update the latches to drive the external pins and IRs update the instruction bits with the instruction that is to be executed.

Boundary Scan Registers

In order to support Boundary Scan, two types of data registers are defined for the ispLSI/pLSI devices -- I/O cell registers and input cell registers. The main purpose of these registers is to capture test data from the appropriate signals and shift data to either drive the test pins or examine captured test data.

Figure 15 describes the register for the I/O cell. The I/O cell, by definition, must have three components. One register component captures the output enable (OE) signal, the second component captures the output data and the third

Table 7. Boundary Scan Interface Signals

pLSI 3000 Family	ispLSI 3000 Family	Pin Function Description
BSCAN	BSCAN/ispEN	Active high signal on this pin selects the Boundary Scan function while active low signal selects the ISP function on the ispLSI devices. Internal pullup on this pin drives the signal high when the external pin is not driven.
TCK	TCK/SCLK	Test Clock function for Boundary Scan and serial clock for the ISP function.
TMS	TMS/MODE	Test Mode Select for Boundary Scan and MODE control for ISP function.
TDI	TDI/SDI	Test Data Input for Boundary Scan and Serial Data Input for ISP pin functions as serial data input pin for both interfaces.
TRST	TRST	Test Reset Input is an asynchronous signal to initialize the TAP controller to Test-Logic-Reset state.
TDO	TDO/SDO	Test Data Output for Boundary Scan and Serial Data Output for ISP pin functions as serial data output pin for both interfaces.

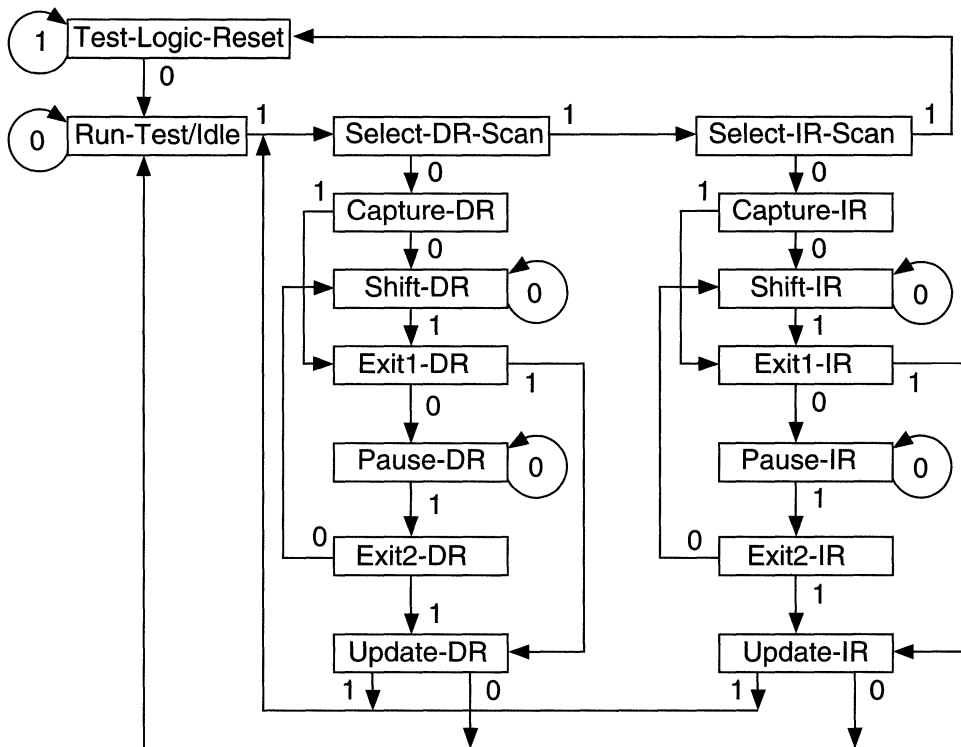


Figure 14A. TAP Controller State Machine

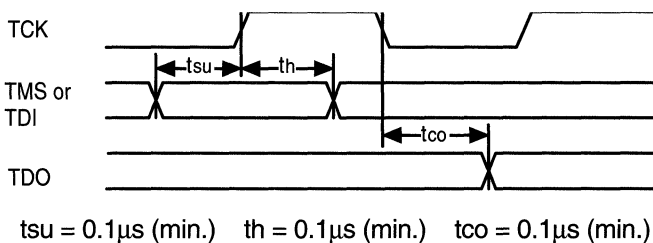


Figure 14B. TAP Controller Timing Diagram

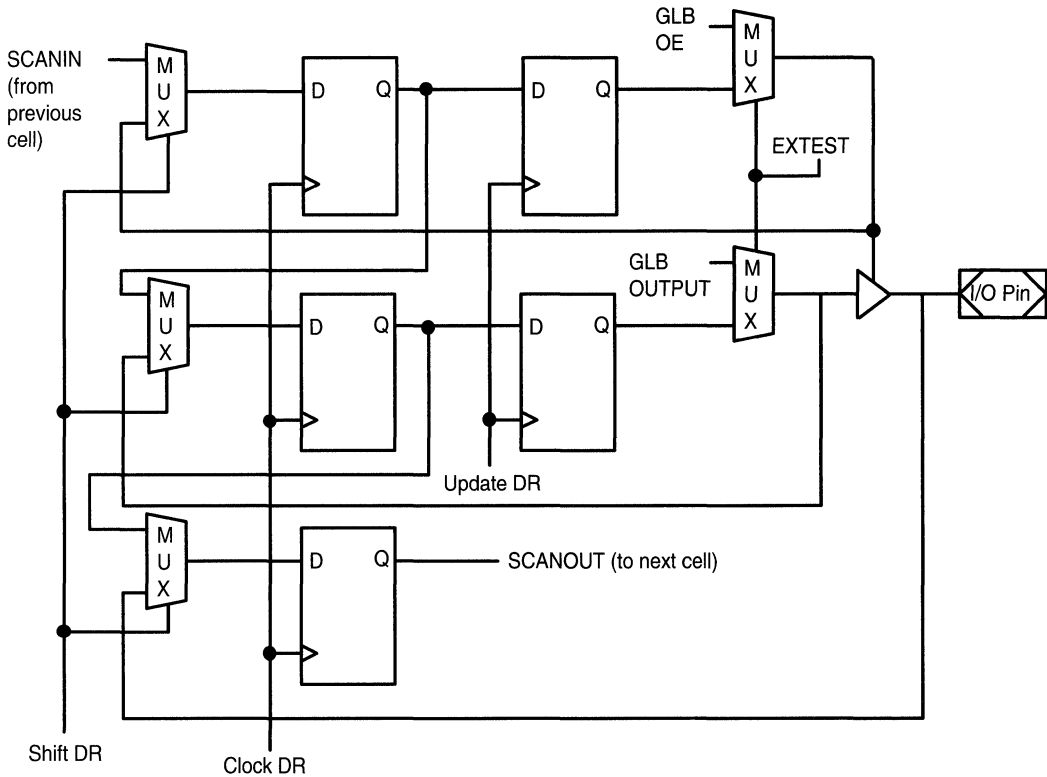


Figure 15. Boundary Scan I/O Cell

captures the input data. These components make up the three registers that are part of the shift register string for each of the I/O pins. Only parts of the I/O cell registers will have valid data when I/O pins are configured as input only or output only and the test routines must be able to monitor the appropriate register bits. The update registers are used mainly to store data that is to be driven onto the I/O pins. The multiplexer controls are driven by the signal from the TAP controller at appropriate states.

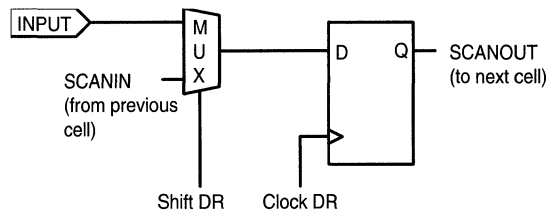


Figure 16. Boundary Scan Input Cell

The function of an input cell register is much simpler than that of an I/O cell. Figure 16 illustrates the single input register cell. The purpose of the I/O cell is to capture the input test data and shift the data out of the shift register string.

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Boundary Scan Instructions

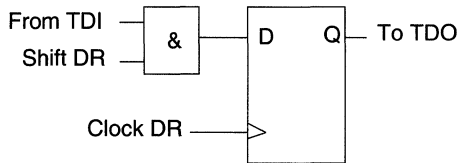
Lattice pLSI and ispLSI devices support the three mandatory instructions defined by the Boundary Scan definition. The following paragraphs describe each of the instructions and its instruction code. A two bit long shift register is defined within the devices to implement the instruction shift register.

The SAMPLE/PRELOAD (Instruction Code - 01) instruction is used to sample the pins that are to be tested. During Capture-DR state, while executing this instruction, the DRs are loaded with the state of the pins which can then be examined after shifting the data through TDO. The PRELOAD part of this instruction is simply loading the DRs during Shift-DR state with the desired condition for each of the pins.

The EXTEST (Instruction Code - 00) instruction drives the external pins with the previously updated values from the DR during Update-DR state.

The BYPASS (Instruction Code - 11) instruction is used to bypass any device that is not accessed during any part of the test. The definition of BYPASS instruction allows the TDI not to be driven during Shift-IR state. In order to shift in the correct instruction code the TDI pin has an internal pull-up to drive a logic high. A bypassed boundary scan device has a single bypass register as shown in figure 17 below.

Figure 17. Bypass Register



Introduction to *pLSI[®] and ispLSI[™] 1000 Family*

Introduction to pLSI/ispLSI 1000 Family

Lattice Semiconductor's pLSI (programmable Large Scale Integration) and ispLSI (in-system programmable Large Scale Integration) are high-density and high-performance E²CMOS[®] programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The Lattice pLSI and ispLSI 1000 Families combine the performance and ease of use of PLDs with the density and flexibility of FPGAs.

The pLSI and ispLSI 1000 Families are ideal for designs requiring high speeds with highly integrated logic.

The ispLSI devices have also pioneered non-volatile, in-system programmability, a technology that allows real-time programming, less expensive manufacturing and end-user feature reconfiguration.

Lattice's E²CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from Lattice and third-party vendors. Development tools offered range from Lattice's low cost pDS[®] software, featuring Boolean entry in a graphical Windows[™] based environment, to the pDS+[™] family of Fitters that interface with third party development software packages. Design systems interfacing with pDS+ Fitters feature schematic capture, state machine and HDL design entry. Designs can now be completed in hours as opposed to days or weeks.

pLSI and ispLSI Product 1000 Family

- 110 MHz System Performance
- 10 ns Pin-to-Pin Delay
- Deterministic Performance
- High Density (2,000-8,000 PLD Gates)
- 44 Pin to 128 Pin Package Options
- Flexible Architecture
- Easy-to-Use
- In-System Programmable (ispLSI)

pLSI and ispLSI Technology

- UltraMOS E²CMOS — the PLD Technology of Choice
- Electrically Erasable/Programmable/Reprogrammable
- 100% Tested During Manufacture
- 100% Programming Yield
- Fast Programming

pLSI and ispLSI Development Tools

- Low Cost, Fully Integrated pDS Design System for the PC
- pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- HDL, VHDL Boolean Equation, State Machine and Schematic Capture Entry
- Timing and Functional Simulation
- PC and Workstation Platforms

Introduction to pLSI and ispLSI 1000 Family

1000 Family Overview

The pLSI and ispLSI 1000 family of high-density devices address high-performance system logic needs, ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD densities ranging from 2,000 to 8,000 gates, the pLSI and ispLSI 1000 Families provide a wide range of programmable logic solutions which meet tomorrow's design requirements today.

Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

Table 1. pLSI and ispLSI 1000 Family Attributes

Family Member	1016	1024	1032	1048/1048C
Density (PLD Gates)	2,000	4,000	6,000	8,000
Speed: f_{max} (MHz)	110	90	90	80
Speed: t_{pd} (ns)	10	12	12	15
GLBs	16	24	32	48
Registers	96	144	192	288
Inputs + I/O	36	54	72	106/110*
Pin/Package	44-pin PLCC 44-pin TQFP 44-pin JLCC	68-pin PLCC 68-pin JLCC	84-pin PLCC 100-pin TQFP 84-pin CPGA	120-pin PQFP 128-pin PQFP*

* pLSI/ispLSI 1048C Only

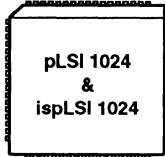
Table 1-0003A

Introduction to pLSI and ispLSI 1000 Family

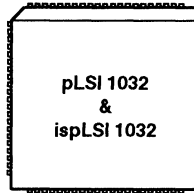
Figure 1. 1000 Family Packages



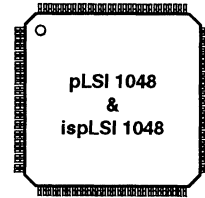
44-Pin PLCC



68-Pin PLCC



84-Pin PLCC



120-Pin PQFP

pLSI 1016
&
ispLSI 1016



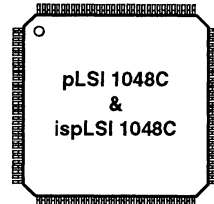
44-Pin TQFP

pLSI 1032
&
ispLSI 1032



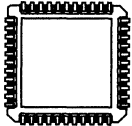
100-Pin TQFP

pLSI 1048C
&
ispLSI 1048C



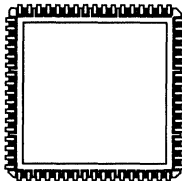
128-Pin PQFP

pLSI
1016/883
&
ispLSI 1016/883



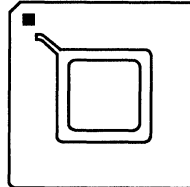
44-Pin JLCC

pLSI 1024/883
&
ispLSI 1024/883



68-Pin JLCC

pLSI 1032/883
&
ispLSI 1032/883



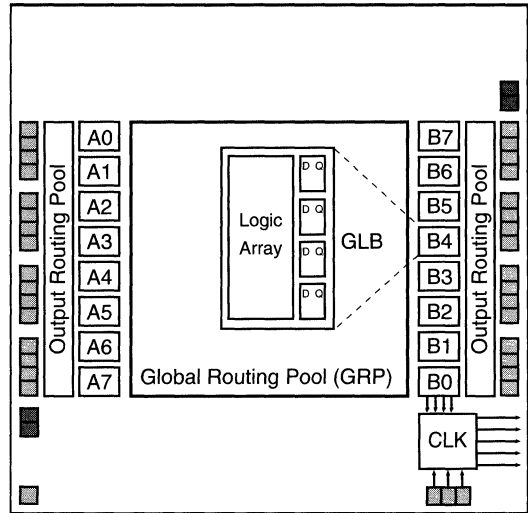
84-Pin CPGA

0288C

Features

- **PROGRAMMABLE AND IN-SYSTEM PROGRAMMABLE HIGH DENSITY LOGIC**
 - High-Speed Global Interconnect
 - 2000 PLD Gates
 - 32 I/O Pins, Four Dedicated Inputs
 - 96 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - $f_{max} = 110$ MHz Maximum Operating Frequency
 - $f_{max} = 60$ MHz for Industrial and Military/883 Devices
 - $t_{pd} = 10$ ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile E²CMOS Technology
 - 100% Tested
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System Programmable 5-Volt Only
 - Change Logic and Interconnects "On-the-Fly" in Seconds
 - Reprogram Soldered Device for Debugging
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Three Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS[®])**
 - pDS Software**
 - Easy to Use PC Windows[™] Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+[™] Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning
 - Automatic Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



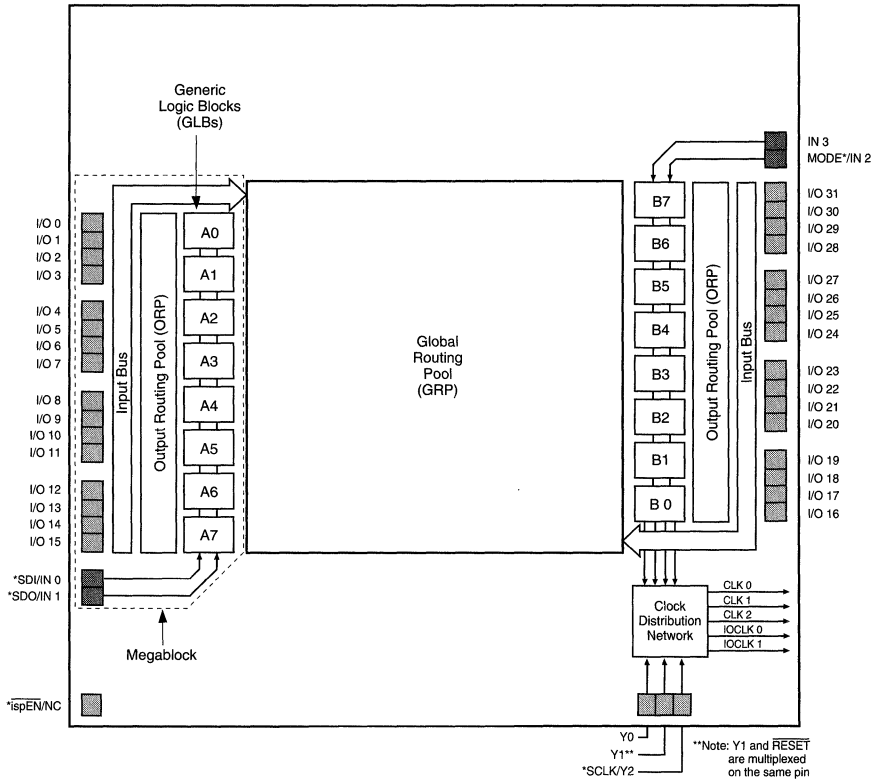
Description

The Lattice pLSI and ispLSI 1016 are High-Density Programmable Logic Devices containing 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1016 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1016 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the pLSI and ispLSI 1016 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. B7 (see figure 1). There are a total of 16 GLBs in the pLSI and ispLSI 1016 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. pLSI and ispLSI 1016 Functional Block Diagram



* ISP Control Functions for ispLSI 1016 Only

0139B(1a)-isp.eps

The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The pLSI and ispLSI 1016 devices contain two of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI and ispLSI 1016 devices are selected using the Clock Distribution Network. Three dedicated clock pins (Y0, Y1 and Y2) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B0 on the pLSI and ispLSI 1016 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings ¹

- Supply Voltage V_{CC} -0.5 to +7.0V
- Input Voltage Applied. -2.5 to $V_{CC} + 1.0V$
- Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Storage Temperature -65 to 150°C
- Case Temp. with Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
V_{CC}	Supply Voltage	Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	4.75	5.25	V
		Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.5	5.5	
		Military/883 $T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$	4.5	5.5	
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	

Table 2-0005Aisp w/mil.epc

Capacitance ($T_A=25^\circ\text{C}$, $f=1.0\text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS	
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	$V_{CC}=5.0V$, $V_{IN}=2.0V$
		Military	10	pf	$V_{CC}=5.0V$, $V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V$, V_{IO} , $V_V=2.0V$	

1. Guaranteed but not 100% tested.

Table 2-0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	-	YEARS
ispLSI Erase/Reprogram Cycles	1000	-	CYCLES
pLSI Erase/Reprogram Cycles	100	-	CYCLES

Table 2-0008A-isp

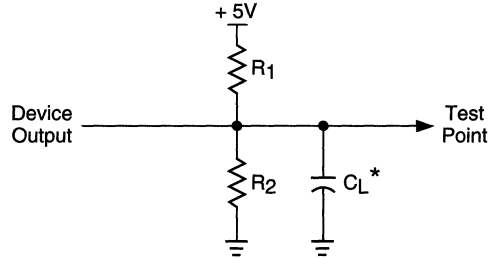
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2-0003

Figure 2. Test Load



* C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition	R1	R2	CL
A	470Ω	390Ω	35pF
B	Active High	∞	390Ω
	Active Low	470Ω	390Ω
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω

Table 2-0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS	
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	-	-	0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	-	-	V	
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	-	-	-10	μA	
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	-	-	10	μA	
I_{IL-isp}	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	-	-	-150	μA	
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	-	-	-150	μA	
I_{OS}^1	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	-60	-	-200	mA	
I_{CC}^2	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$	Commercial	-	100	150	mA
		$f_{TOGGLE} = 1 \text{ MHz}$	Industrial/Military	-	100	170	mA

1. One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Table 2-0007A-16 w/ml

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND. ⁵	# ²	DESCRIPTION ¹	-110		-90		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	10	–	12	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	14.5	–	17	ns
f_{max}	A	3	Clock Frequency with Internal Feedback ³	111	–	90.9	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback ($\frac{1}{t_{su2} + t_{co1}}$)	70.1	–	58.8	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle ⁴	125	–	125	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	4.5	–	6	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	7	–	8	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	9	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	8.5	–	10	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	14	–	15	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	10	–	ns
t_{en}	B	14	Input to Output Enable	–	15	–	15	ns
t_{dis}	C	15	Input to Output Disable	–	15	–	15	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	4	–	4	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	4	–	4	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	–	2	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	5.5	–	6.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Table 2-0030-16/110,90C

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST ⁵ COND.	# ²	DESCRIPTION ¹	-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	
t _{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	20	ns
t _{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	20	–	25	ns
f _{max}	A	3	Clock Frequency with Internal Feedback ³	80	–	60	–	MHz
f _{max} (Ext.)	–	4	Clock Frequency with External Feedback ($\frac{1}{t_{su2} + t_{co1}}$)	50	–	38	–	MHz
f _{max} (Tog.)	–	5	Clock Frequency, Max Toggle ⁴	100	–	83	–	MHz
t _{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	ns
t _{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	13	ns
t _{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t _{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	13	–	ns
t _{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	16	ns
t _{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t _{r1}	A	12	Ext. Reset Pin to Output Delay	–	17	–	22.5	ns
t _{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t _{en}	B	14	Input to Output Enable	–	18	–	24	ns
t _{dis}	C	15	Input to Output Disable	–	18	–	24	ns
t _{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	ns
t _{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	ns
t _{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	–	2.5	–	ns
t _{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	6.5	–	8.5	–	ns

Table 2-0030-16/80,60C

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-110		-90		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	20	I/O Register Bypass	–	0.8	–	1.0	ns
t_{iolat}	21	I/O Latch Delay	–	1.7	–	2.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	4.1	–	4.5	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.8	–	2.0	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	1.7	–	2.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.1	–	2.5	ns
t_{din}	26	Dedicated Input Delay	–	1.7	–	2.0	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	0.6	–	0.7	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	0.8	–	1.0	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	1.5	–	1.8	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	2.1	–	2.6	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	2.8	–	3.4	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.3	–	6.5	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	6.1	–	7.0	ns
t_{20ptxor}	35	20 Product Term/XOR Path Delay	–	6.6	–	8.0	ns
t_{xoradj}	36	XOR Adjacent Path Delay ³	–	8.2	–	9.5	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.5	–	0.5	ns
t_{gsu}	38	GLB Register Setup Time before Clock	0.3	–	1.0	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	2.9	–	3.5	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	1.5	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.1	–	2.5	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	8.2	–	10.0	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	9.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	2.8	6.2	3.5	7.5	ns
ORP							
t_{orp}	45	ORP Delay	–	2.0	–	2.5	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	ns

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

3. The XOR Adjacent path can only be used by Lattice Hard Macros.

2

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-110		-90		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	2.1	–	2.5	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	3.3	–	4.0	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	3.3	–	4.0	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.9	2.9	3.5	3.5	ns
t_{gy1/2}	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.1	3.8	2.5	4.5	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.2	1.0	5.0	ns
t_{ioy1/2}	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	2.1	3.8	2.5	4.5	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.2	1.0	5.0	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	7.9	–	7.5	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t _{iobp}	20	I/O Register Bypass	–	2.0	–	2.7	ns
t _{iolat}	21	I/O Latch Delay	–	3.0	–	4.0	ns
t _{iosu}	22	I/O Register Setup Time before Clock	5.5	–	7.3	–	ns
t _{ioh}	23	I/O Register Hold Time after Clock	1.0	–	1.3	–	ns
t _{ioco}	24	I/O Register Clock to Out Delay	–	3.0	–	4.0	ns
t _{ior}	25	I/O Register Reset to Out Delay	–	2.5	–	3.3	ns
t _{din}	26	Dedicated Input Delay	–	4.0	–	5.3	ns
GRP							
t _{grp1}	27	GRP Delay, 1 GLB Load	–	1.5	–	2.0	ns
t _{grp4}	28	GRP Delay, 4 GLB Loads	–	2.0	–	2.7	ns
t _{grp8}	29	GRP Delay, 8 GLB Loads	–	3.0	–	4.0	ns
t _{grp12}	30	GRP Delay, 12 GLB Loads	–	3.8	–	5.0	ns
t _{grp16}	31	GRP Delay, 16 GLB Loads	–	4.5	–	6.0	ns
GLB							
t _{4ptbp}	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t _{1ptxor}	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
t _{20ptxor}	35	20 Product Term/XOR Path Delay	–	8.0	–	10.6	ns
t _{xoradj}	36	XOR Adjacent Path Delay ³	–	9.5	–	12.7	ns
t _{gbp}	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t _{gsu}	38	GLB Register Setup Time before Clock	1.0	–	1.3	–	ns
t _{gh}	39	GLB Register Hold Time after Clock	4.5	–	6.0	–	ns
t _{gco}	40	GLB Register Clock to Output Delay	–	2.0	–	2.7	ns
t _{gr}	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t _{ptre}	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t _{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	12.0	ns
t _{ptck}	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t _{orp}	45	ORP Delay	–	2.5	–	3.3	ns
t _{orpbp}	46	ORP Bypass Delay	–	0.5	–	0.7	ns

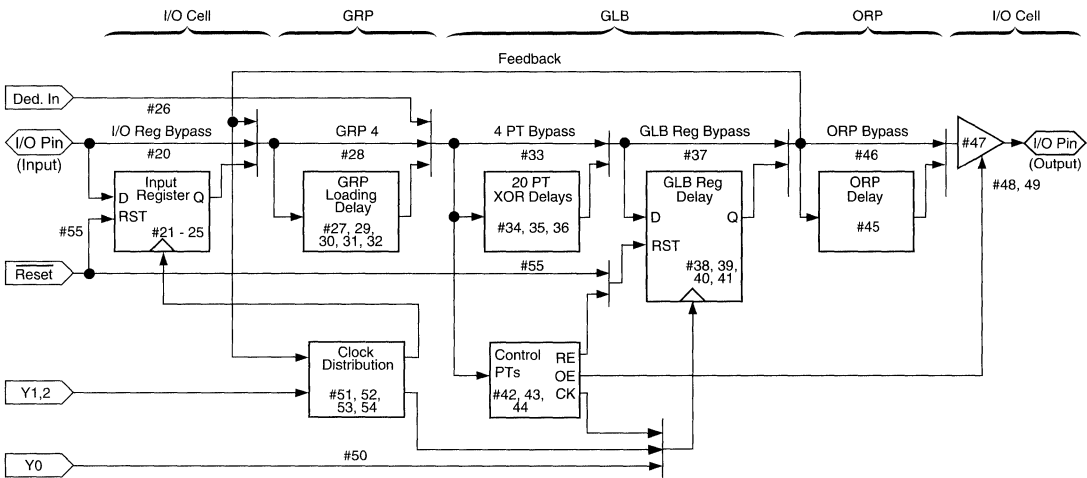
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.5	4.5	6.0	6.0	ns
t_{gy1/2}	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
t_{ioy1/2}	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI and ispLSI 1016 Timing Model



2

Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

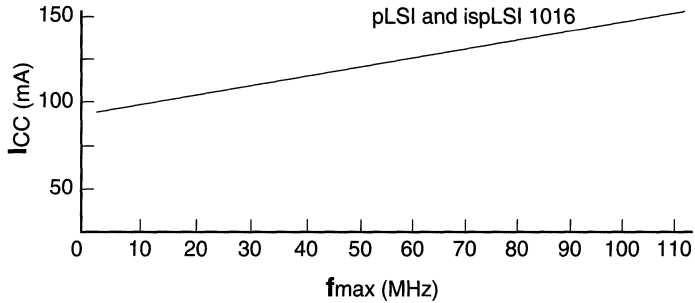
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 5.5 \text{ ns} &= (1.0 + 1.0 + 8.0) + (1.0) - (1.0 + 1.0 + 3.5) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 3.0 \text{ ns} &= (1.0 + 1.0 + 7.5) + (3.5) - (1.0 + 1.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 16.0 \text{ ns} &= (1.0 + 1.0 + 7.5) + (1.5) + (2.5 + 2.5)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
 5.0 \text{ ns} &= (1.0 + 1.0 + 8.0) + (1.0) - (3.5 + 1.5 + 1.0) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
 3.5 \text{ ns} &= (3.5 + 1.5 + 5.0) + (3.5) - (1.0 + 1.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
 16.5 \text{ ns} &= (3.5 + 1.5 + 5.0) + (1.5) + (2.5 + 2.5)
 \end{aligned}$$

1. Calculations are based upon timing specs for the ispLSI 1016-90.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25°C

ICC can be estimated for the pLSI and ispLSI 1016 using the following equation:

$$I_{CC} = 31 + (\# \text{ of PTs} * 0.45) + (\# \text{ of nets} * \text{Max. freq} * 0.009) \text{ where:}$$

of PTs = Number of Product Terms used in design

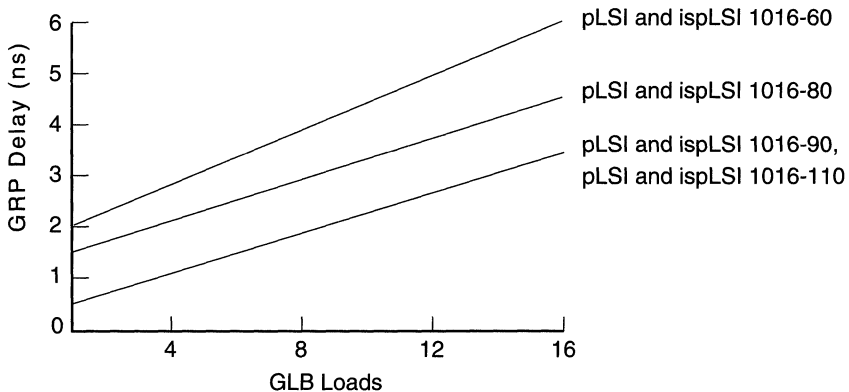
of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions ($V_{CC} = 5.0V$, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A-16-80-isp.eps

Figure 4. Maximum GRP Delay vs GLB loads



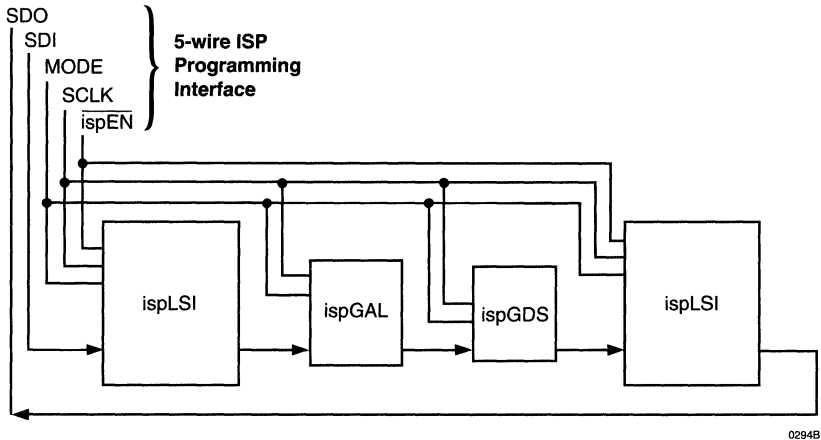
0126A-80-16-isp.eps

In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this Data Book.

Figure 5. ISP Programming Interface



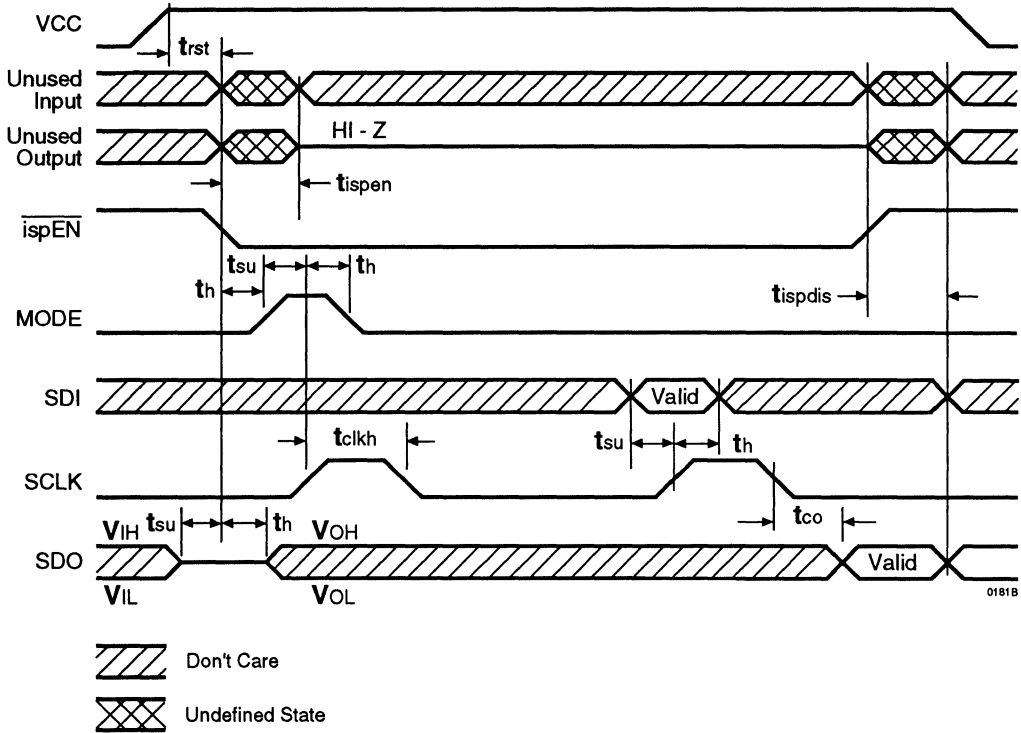
ISP Programming Voltage/Timing Specifications¹

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCP}	Programming Voltage		4.75	5	5.25	V
I _{CCP}	Programming Supply Current		–	50	100	mA
V _{IHP}	Input Voltage High	ispEN = Low	2.0	–	V _{CCP}	V
V _{ILP}	Input Voltage Low		0	–	0.8	V
I _{IP}	Input Current		–	100	200	μA
V _{OHP}	Output Voltage High	I _{OH} = -3.2 mA	2.4	–	V _{CCP}	V
V _{OLP}	Output Voltage Low	I _{OL} = 5 mA	0	–	0.5	V
t _r , t _f	Input Rise and Fall		–	–	0.1	μs
t _{ispen}	ispEN to Output 3-State Enabled		–	2	10	μs
t _{ispdis}	ispEN to Output 3-State Disabled		–	2	10	μs
t _{su}	Setup Time		0.1	0.5	–	μs
t _{co}	Clock to Output		0.1	0.5	–	μs
t _h	Hold Time		0.1	0.5	–	μs
t _{clkh} , t _{ckl}	Clock Pulse Width, High and Low		0.5	1	–	μs
t _{pw}	Verify Pulse Width		20	30	–	μs
t _{pwp}	Programming Pulse Width		40	–	100	ms
t _{bew}	Bulk Erase Pulse Width		200	–	–	ms
t _{rst}	Reset Time From Valid V _{CCP}		45	–	–	μs

 1. ISP Programming is guaranteed for T_A = 0°C to 70°C Operation only.

Table 2-0029 isp-C

Figure 6. Timing Waveforms for In-System Programming (ispLSI 1016)



2

Figure 7. Program, Verify & Bulk Erase Waveforms (ispLSI 1016)

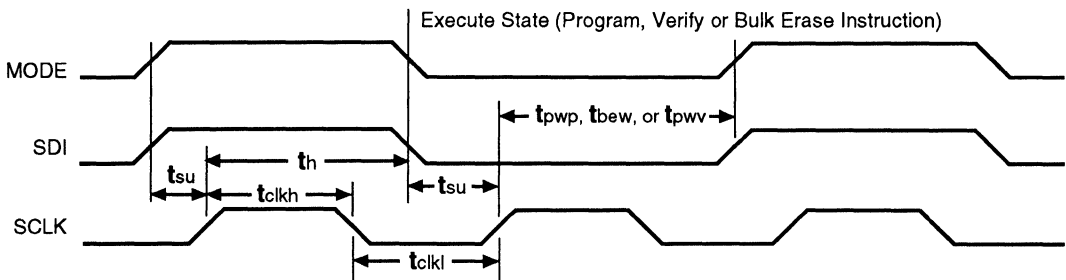
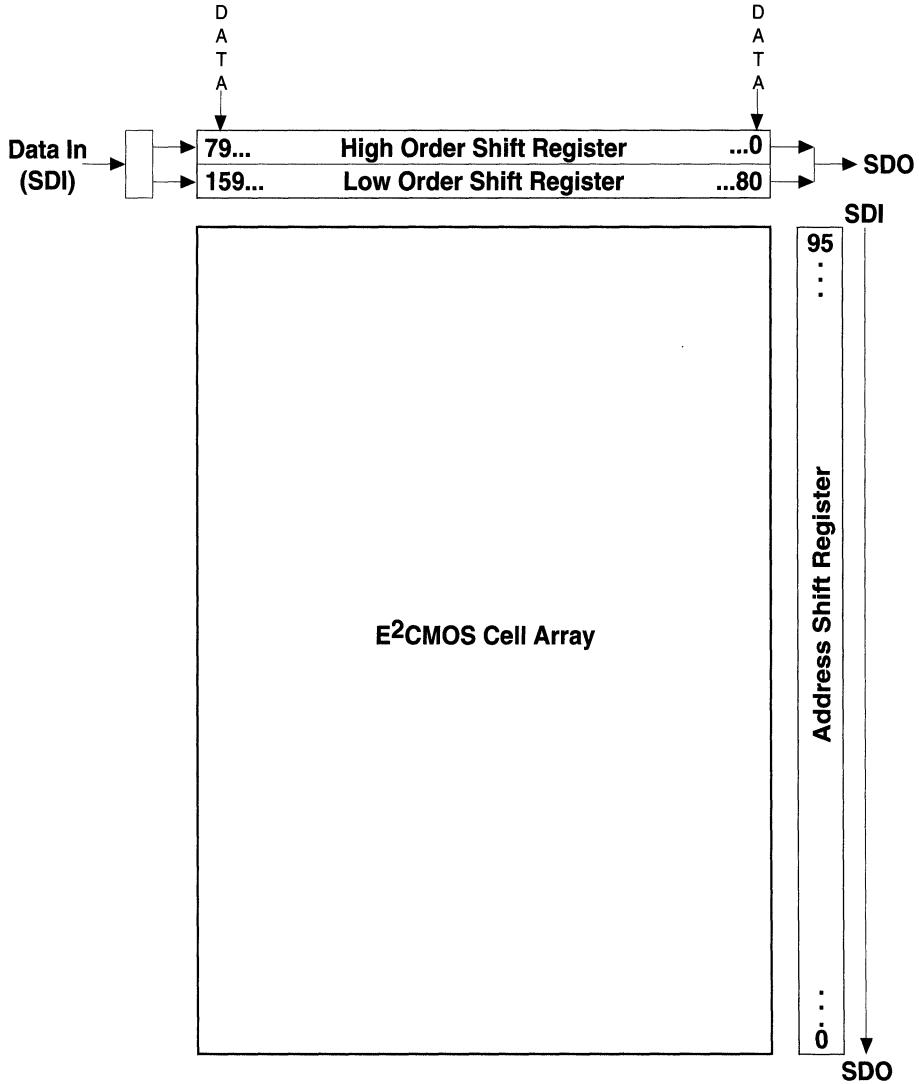


Figure 8 illustrates the address and data shift register bits for the ispLSI 1016. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book.

Figure 8. ispLSI 1016 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

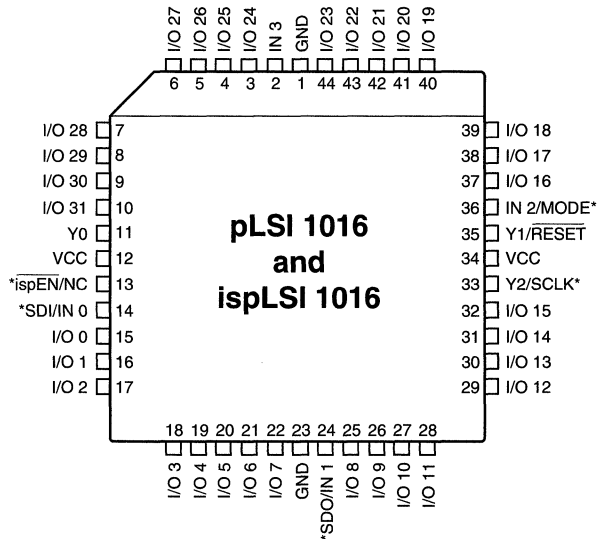
Name	TQFP Pin Numbers	PLCC Pin Numbers	JLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 3	40	2	2	Dedicated input pins to the device.
ispEN*	7	13	13	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	8	14	14	Input – This pin performs <u>two</u> functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 2	30	36	36	Input – This pin performs <u>two</u> functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 1	18	24	24	Input/Output – This pin performs <u>two</u> functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK*/Y2	27	33	33	Input – This pin performs <u>two</u> functions. It is a dedicated clock input when ispEN is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
Y0	5	11	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1/RESET	29	35	35	This pin performs two functions: <ul style="list-style-type: none"> – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
GND VCC	17, 39 6, 28	1, 23 12, 34	1, 23 12, 34	Ground (GND) V _{CC}

* For ispLSI 1016 Only

Table 2 - 0002C-16-isp

Pin Configuration

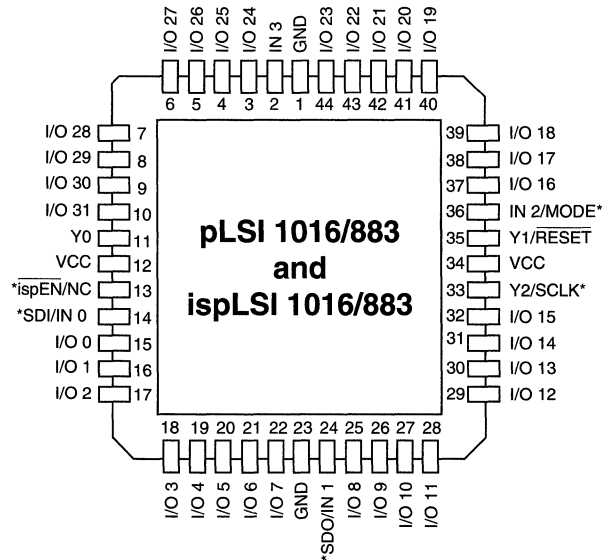
pLSI and ispLSI 1016 44-Pin PLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1016 only (except pin 13, which is $\overline{\text{ispEN}}$ only).

pLSI and ispLSI 1016 44-Pin JLCC Pinout Diagram

0123A-isp1016

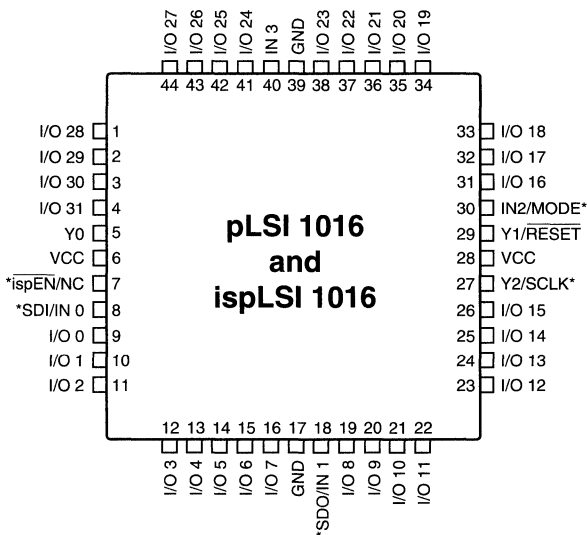


* Pins have dual function capability for ispLSI 1016 only (except pin 13, which is $\overline{\text{ispEN}}$ only).

0123-16-isp/JLCC

Pin Configuration

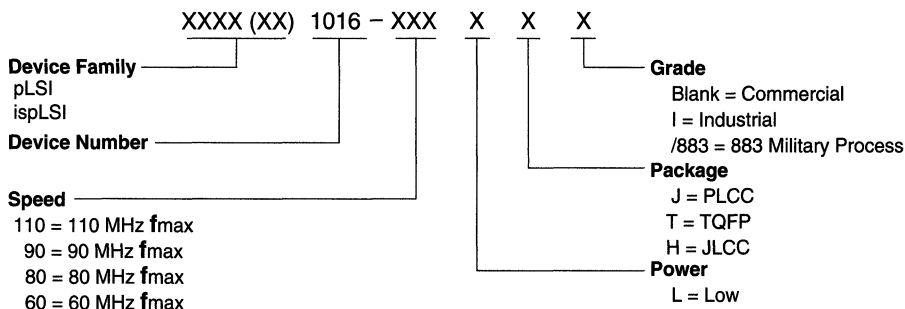
pLSI and ispLSI 1016 44-Pin TQFP Pinout Diagram



* Pins have dual function capability for ispLSI 1016 only (except pin 7, which is $\overline{\text{ispEN}}$ only).

0851-167QF

Part Number Description



00212-808-isp1016

pLSI and ispLSI 1016 Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	110	10	pLSI 1016-110LJ	44-Pin PLCC
	110	10	pLSI 1016-110LT	44-Pin TQFP
	90	12	pLSI 1016-90LJ	44-Pin PLCC
	90	12	pLSI 1016-90LT	44-Pin TQFP
	80	15	pLSI 1016-80LJ	44-Pin PLCC
	80	15	pLSI 1016-80LT	44-Pin TQFP
	60	20	pLSI 1016-60LJ	44-Pin PLCC
	60	20	pLSI 1016-60LT	44-Pin TQFP
ispLSI	110	10	ispLSI 1016-110LJ	44-Pin PLCC
	110	10	ispLSI 1016-110LT	44-Pin TQFP
	90	12	ispLSI 1016-90LJ	44-Pin PLCC
	90	12	ispLSI 1016-90LT	44-Pin TQFP
	80	15	ispLSI 1016-80LJ	44-Pin PLCC
	80	15	ispLSI 1016-80LT	44-Pin TQFP
	60	20	ispLSI 1016-60LJ	44-Pin PLCC
	60	20	ispLSI 1016-60LT	44-Pin TQFP

INDUSTRIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	60	20	pLSI 1016-60LJI	44-Pin PLCC
ispLSI	60	20	ispLSI 1016-60LJI	44-Pin PLCC

MILITARY/883

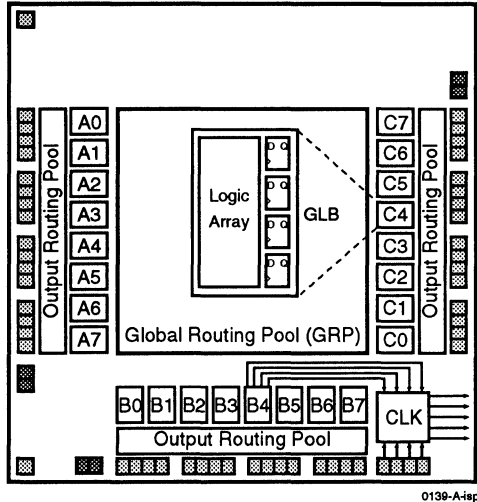
Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	60	20	pLSI 1016-60LH/883	44-Pin JLCC
ispLSI	60	20	ispLSI 1016-60LH/883	44-Pin JLCC

Table 2-0041-16-isp1016

Features

- **PROGRAMMABLE AND IN-SYSTEM PROGRAMMABLE HIGH DENSITY LOGIC**
 - High-Speed Global Interconnect
 - 4000 PLD Gates
 - 48 I/O Pins, Six Dedicated Inputs
 - 144 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Fast Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - f_{max} = 90 MHz Maximum Operating Frequency
 - f_{max} = 60 MHz for Industrial and Military/883 Devices
 - t_{pd} = 12 ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile E²CMOS Technology
 - 100% Tested
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System Programmable 5-Volt Only
 - Change Logic and Interconnects "On-the-Fly" in Seconds
 - Reprogram Soldered Device for Debugging
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Four Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS[®])**
 - pDS Software**
 - Easy to Use PC Windows[™] Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+[™] Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning and Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



2

Description

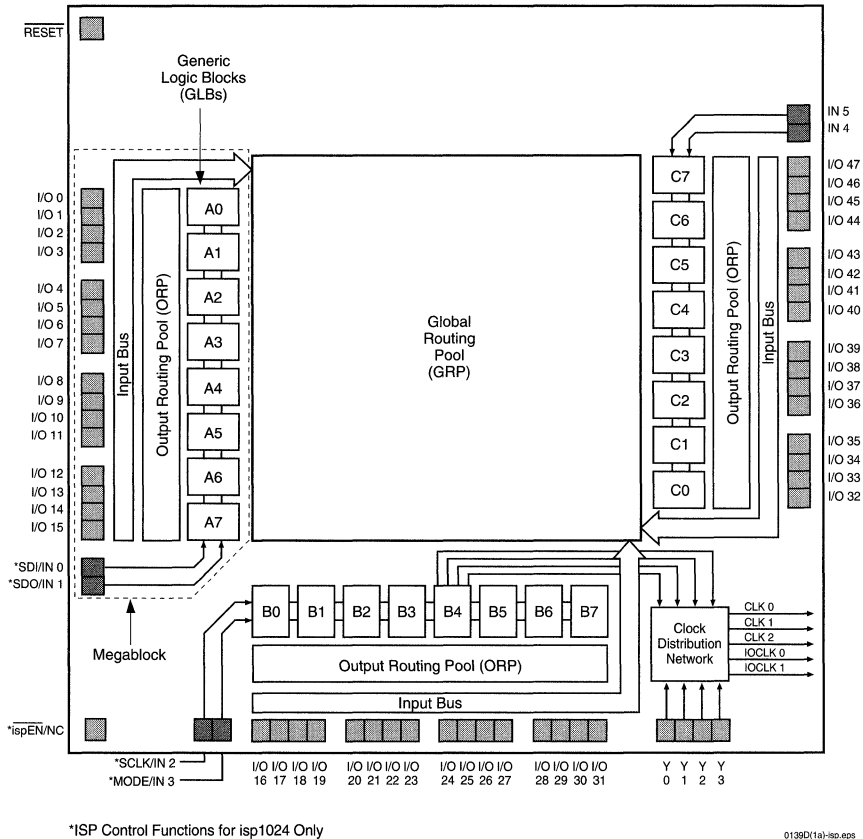
The Lattice pLSI and ispLSI 1024 are High-Density Programmable Logic Devices containing 144 Registers, 48 Universal I/O pins, six Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1024 features 5-Volt in-system programmability and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1024 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the pLSI and ispLSI 1024 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. C7 (see figure 1). There are a total of 24 GLBs in the pLSI and ispLSI 1024 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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Functional Block Diagram

Figure 1. pLSI and ispLSI 1024 Functional Block Diagram



The devices also have 48 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The pLSI and ispLSI 1024 devices contain three of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI and ispLSI 1024 devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B4 on the pLSI and ispLSI 1024 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings ¹

- Supply Voltage V_{CC} -0.5 to +7.0V
- Input Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Storage Temperature -65 to 150°C
- Case Temp. with Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
V_{CC}	Supply Voltage	Commercial $T_A = 0^\circ C$ to $+70^\circ C$	4.75	5.25	V
		Industrial $T_A = -40^\circ C$ to $+85^\circ C$	4.5	5.5	
		Military/883 $T_C = -55^\circ C$ to $+125^\circ C$	4.5	5.5	
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	

Table 2-0005Aisp w/mil.epc

Capacitance ($T_A=25^\circ C$, $f=1.0$ MHz)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS	
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	$V_{CC}=5.0V$, $V_{IN}=2.0V$
		Military	10	pf	$V_{CC}=5.0V$, $V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V$, V_{IO} , $V_V=2.0V$	

1. Guaranteed but not 100% tested.

Table 2-0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	-	YEARS
ispLSI Erase/Reprogram Cycles	1000	-	CYCLES
pLSI Erase/Reprogram Cycles	100	-	CYCLES

Table 2-0008A-isp

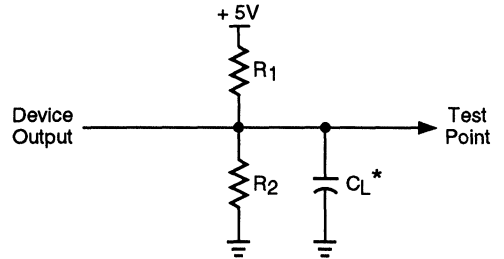
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



* C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition	R1	R2	CL
A	470Ω	390Ω	35pF
B	Active High	∞	390Ω
	Active Low	470Ω	390Ω
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω

Table 2- 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS	
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	-	-	0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	-	-	V	
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	-	-	-10	μA	
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	-	-	10	μA	
I_{IL-isp}	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	-	-	-150	μA	
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	-	-	-150	μA	
I_{OS1}	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	-60	-	-200	mA	
I_{CC2}	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$	Commercial	-	130	190	mA
		$f_{TOGGLE} = 1 \text{ MHz}$	Industrial/Military	-	135	220	mA

- One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- Measured using six 16-bit counters.
- Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Table 2-0007A-24 w/ml

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST ⁵ COND.	# ²	DESCRIPTION ¹	-90		-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	-	12	-	15	-	20	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	-	17	-	20	-	25	ns
f_{max}	A	3	Clock Frequency with Internal Feedback ³	90.9	-	80	-	60	-	MHz
f_{max} (Ext.)	-	4	Clock Frequency with External Feedback ($\frac{1}{t_{su2} + t_{co1}}$)	58.8	-	50	-	38	-	MHz
f_{max} (Tog.)	-	5	Clock Frequency, Max Toggle ⁴	125	-	100	-	83	-	MHz
t_{su1}	-	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	-	7	-	9	-	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	-	8	-	10	-	13	ns
t_{h1}	-	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	-	0	-	0	-	ns
t_{su2}	-	9	GLB Reg. Setup Time before Clock	9	-	10	-	13	-	ns
t_{co2}	-	10	GLB Reg. Clock to Output Delay	-	10	-	12	-	16	ns
t_{h2}	-	11	GLB Reg. Hold Time after Clock	0	-	0	-	0	-	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	-	15	-	17	-	22.5	ns
t_{rw1}	-	13	Ext. Reset Pulse Duration	10	-	10	-	13	-	ns
t_{en}	B	14	Input to Output Enable	-	15	-	18	-	24	ns
t_{dis}	C	15	Input to Output Disable	-	15	-	18	-	24	ns
t_{wh}	-	16	Ext. Sync. Clock Pulse Duration, High	4	-	5	-	6	-	ns
t_{wl}	-	17	Ext. Sync. Clock Pulse Duration, Low	4	-	5	-	6	-	ns
t_{su5}	-	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	-	2	-	2.5	-	ns
t_{h5}	-	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	-	6.5	-	8.5	-	ns

Table 2-0030-24/90,80,60C

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t _{iobp}	20	I/O Register Bypass	–	1.6	–	2.0	–	2.7	ns
t _{iolat}	21	I/O Latch Delay	–	2.4	–	3.0	–	4.0	ns
t _{iosu}	22	I/O Register Setup Time before Clock	4.8	–	5.5	–	7.3	–	ns
t _{ioh}	23	I/O Register Hold Time after Clock	2.1	–	1.0	–	1.3	–	ns
t _{ioco}	24	I/O Register Clock to Out Delay	–	2.4	–	3.0	–	4.0	ns
t _{ior}	25	I/O Register Reset to Out Delay	–	2.8	–	2.5	–	3.3	ns
t _{din}	26	Dedicated Input Delay	–	3.2	–	4.0	–	5.3	ns
GRP									
t _{grp1}	27	GRP Delay, 1 GLB Load	–	1.2	–	1.5	–	2.0	ns
t _{grp4}	28	GRP Delay, 4 GLB Loads	–	1.6	–	2.0	–	2.7	ns
t _{grp8}	29	GRP Delay, 8 GLB Loads	–	2.4	–	3.0	–	4.0	ns
t _{grp12}	30	GRP Delay, 12 GLB Loads	–	3.0	–	3.8	–	5.0	ns
t _{grp16}	31	GRP Delay, 16 GLB Loads	–	3.6	–	4.5	–	6.0	ns
t _{grp24}	32	GRP Delay, 24 GLB Loads	–	5.0	–	6.3	–	8.3	ns
GLB									
t _{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.2	–	6.5	–	8.6	ns
t _{1ptxor}	34	1 Product Term/XOR Path Delay	–	5.7	–	7.0	–	9.3	ns
t _{20ptxor}	35	20 Product Term/XOR Path Delay	–	7.0	–	8.0	–	10.6	ns
t _{xoradj}	36	XOR Adjacent Path Delay ³	–	8.2	–	9.5	–	12.7	ns
t _{gbp}	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
t _{gsu}	38	GLB Register Setup Time before Clock	1.2	–	1.0	–	1.3	–	ns
t _{gh}	39	GLB Register Hold Time after Clock	3.6	–	4.5	–	6.0	–	ns
t _{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	2.0	–	2.7	ns
t _{gr}	41	GLB Register Reset to Output Delay	–	2.0	–	2.5	–	3.3	ns
t _{ptre}	42	GLB Product Term Reset to Register Delay	–	8.0	–	10.0	–	13.3	ns
t _{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	7.8	–	9.0	–	12.0	ns
t _{ptck}	44	GLB Product Term Clock Delay	2.8	6.0	3.5	7.5	4.6	9.9	ns
ORP									
t _{orp}	45	ORP Delay	–	2.4	–	2.5	–	3.3	ns
t _{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

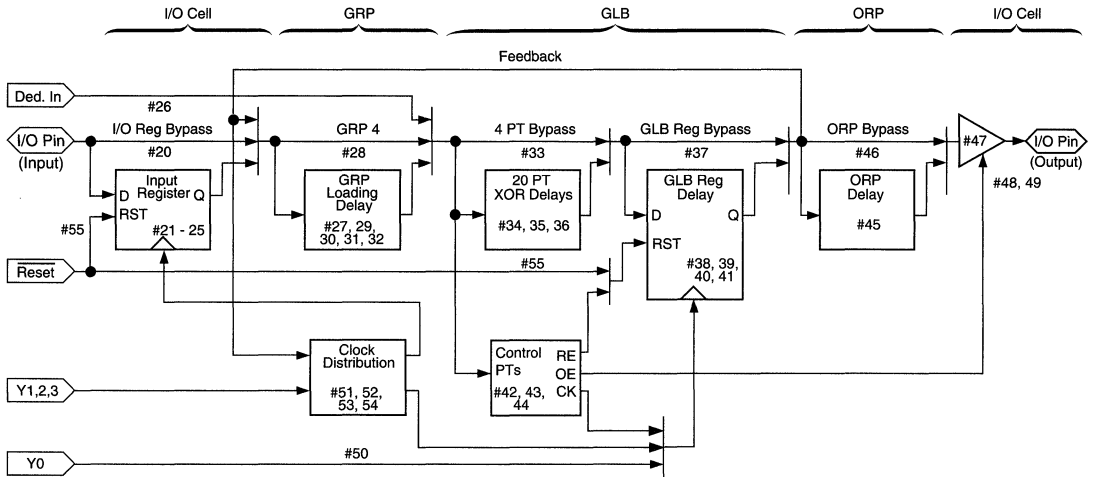
Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t _{ob}	47	Output Buffer Delay	–	2.4	–	3.0	–	4.0	ns
t _{oen}	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
t _{odis}	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
t _{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.6	3.6	4.5	4.5	6.0	6.0	ns
t _{gy1/2}	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t _{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
t _{ioy2/3}	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t _{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
Global Reset									
t _{gr}	55	Global Reset to GLB and I/O Registers	–	8.2	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

2

pLSI and ispLSI 1024 Timing Model

Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

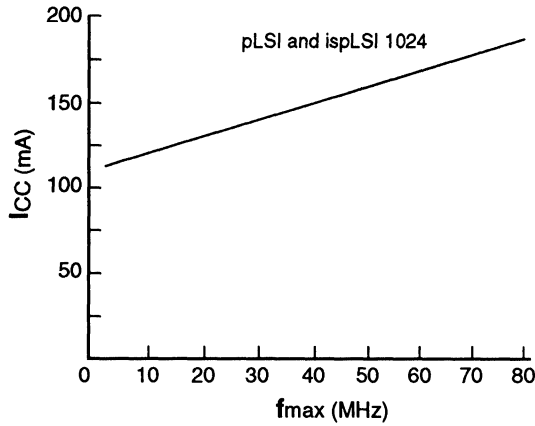
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 5.5 \text{ ns} &= (2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 4.0 \text{ ns} &= (2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 19.0 \text{ ns} &= (2.0 + 2.0 + 7.5) + (2.0) + (2.5 + 3.0)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
 5.5 \text{ ns} &= (2.0 + 2.0 + 8.0) + (1.0) - (4.5 + 2.0 + 1.0) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
 4.0 \text{ ns} &= (4.5 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
 19.0 \text{ ns} &= (4.5 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)
 \end{aligned}$$

1. Calculations are based upon timing specs for the pLSI and ispLSI 1024-80.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Six 16-bit Counters
Typical Current at 5V, 25°C

ICC can be estimated for the pLSI and ispLSI 1024 using the following equation:

$$I_{CC} = 42 + (\# \text{ of PTs} * 0.45) + (\# \text{ of nets} * \text{Max. freq} * 0.008) \text{ where:}$$

of PTs = Number of Product Terms used in design

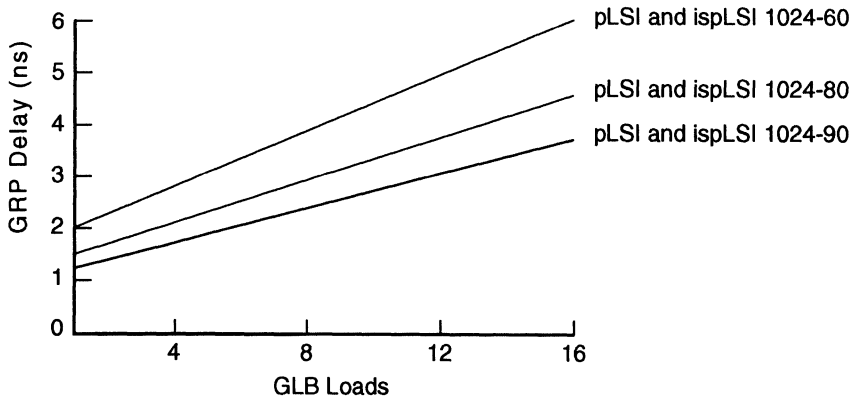
of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A-24-80-isp

Figure 4. Maximum GRP Delay vs GLB Loads



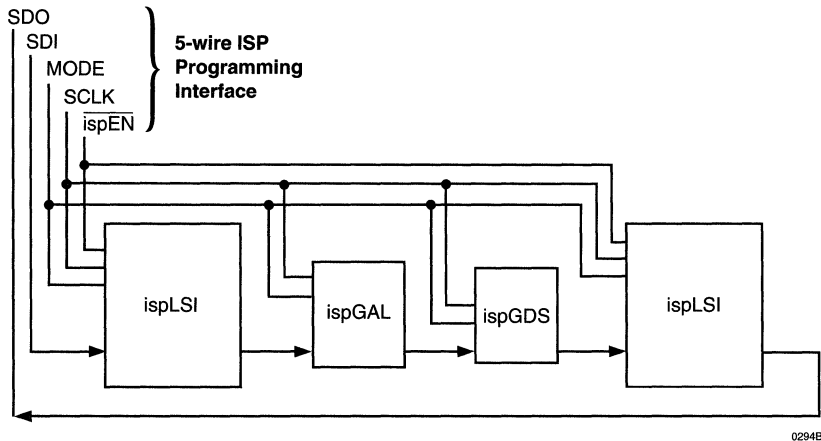
0126A-80-24-isp.eps

In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable (*ispEN*), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this Data Book.

Figure 5. ISP Programming Interface



ISP Programming Voltage/Timing Specifications¹

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.75	5	5.25	V
I_{CCP}	Programming Supply Current		–	50	100	mA
V_{IHP}	Input Voltage High	$\overline{\text{ispEN}} = \text{Low}$	2.0	–	V _{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	μA
V_{OHP}	Output Voltage High	I _{OH} = -3.2 mA	2.4	–	V _{CCP}	V
V_{OLP}	Output Voltage Low	I _{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	μs
t_{ispen}	$\overline{\text{ispEN}}$ to Output 3-State Enabled		–	2	10	μs
t_{ispdis}	$\overline{\text{ispEN}}$ to Output 3-State Disabled		–	2	10	μs
t_{su}	Setup Time		0.1	0.5	–	μs
t_{co}	Clock to Output		0.1	0.5	–	μs
t_h	Hold Time		0.1	0.5	–	μs
t_{clkh}, t_{ckl}	Clock Pulse Width, High and Low		0.5	1	–	μs
t_{pwv}	Verify Pulse Width		20	30	–	μs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V _{CCP}		45	–	–	μs

 1. ISP Programming is guaranteed for T_A = 0°C to 70°C Operation only.

Table 2- 0029 isp-C

Figure 6. Timing Waveforms for In-System Programming (ispLSI 1024)

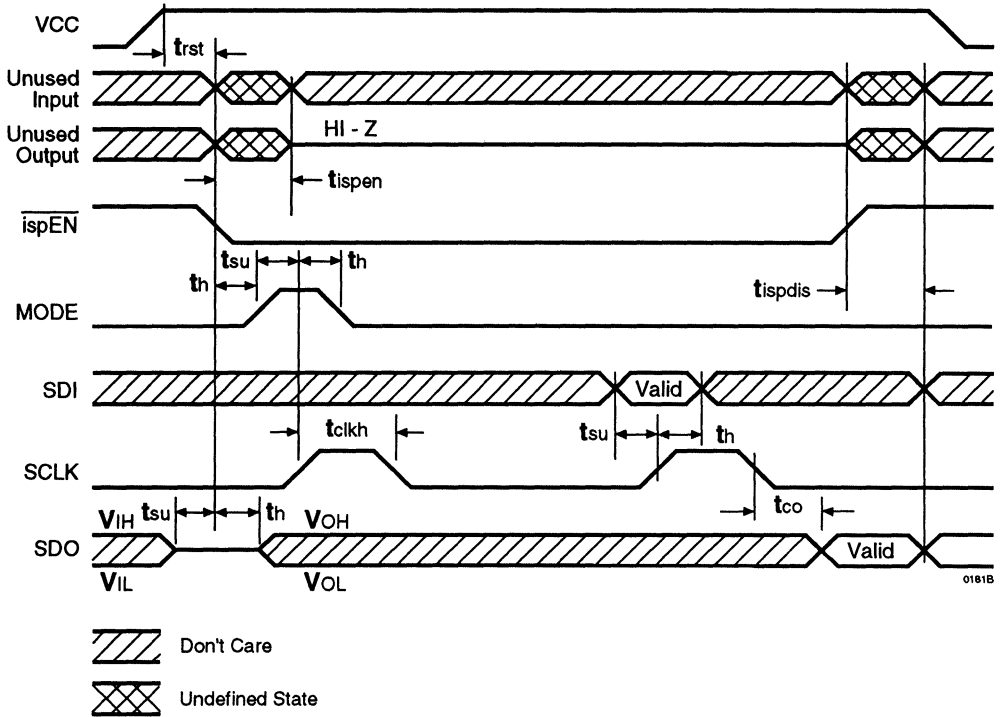


Figure 7. Program, Verify & Bulk Erase Waveforms (ispLSI 1024)

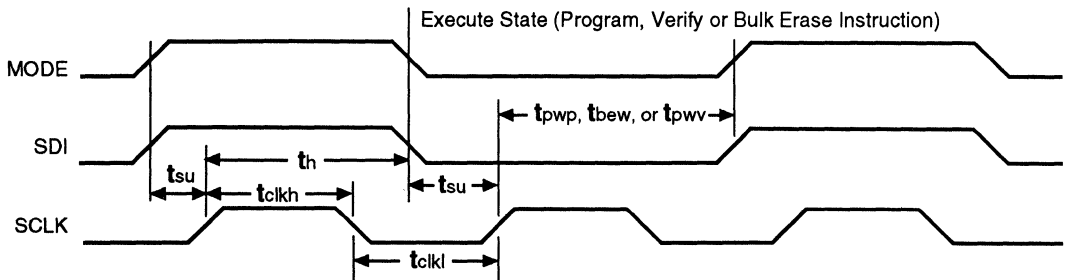
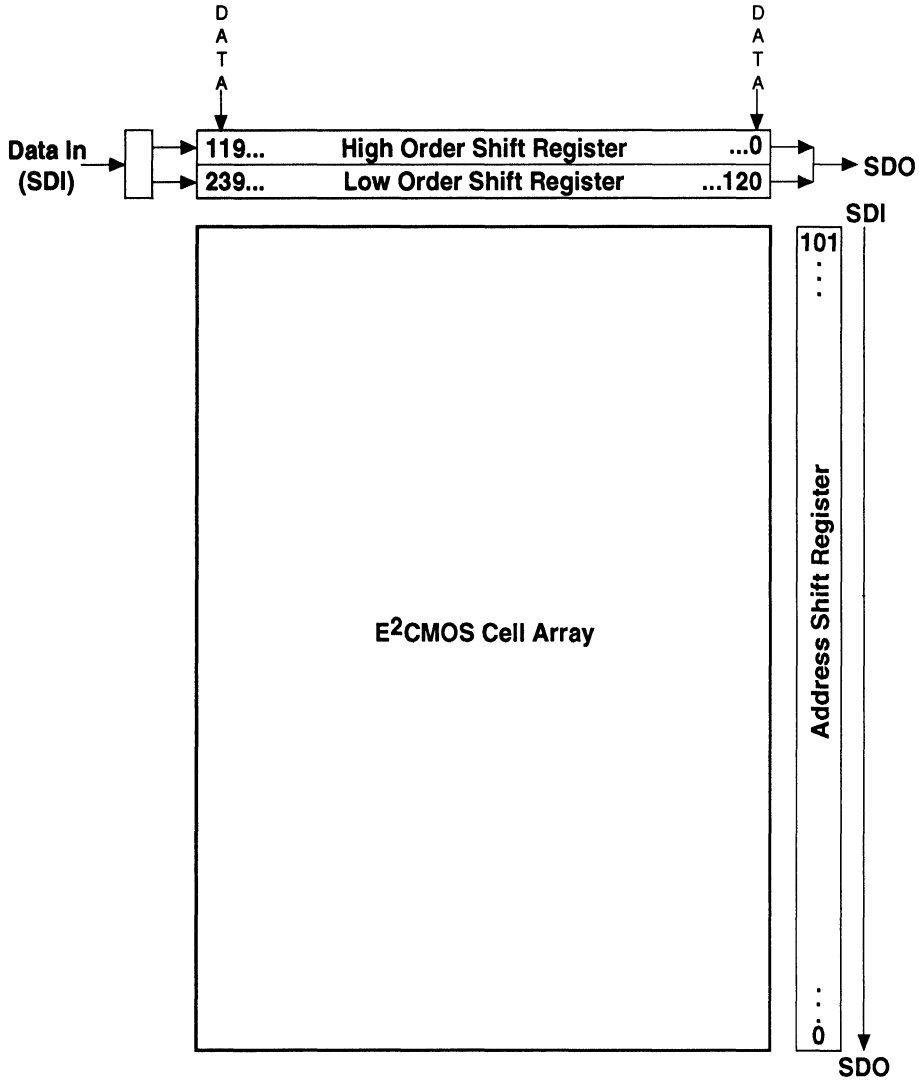


Figure 8 illustrates the address and data shift register bits for the ispLSI 1024. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book.

Figure 8. ispLSI 1024 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

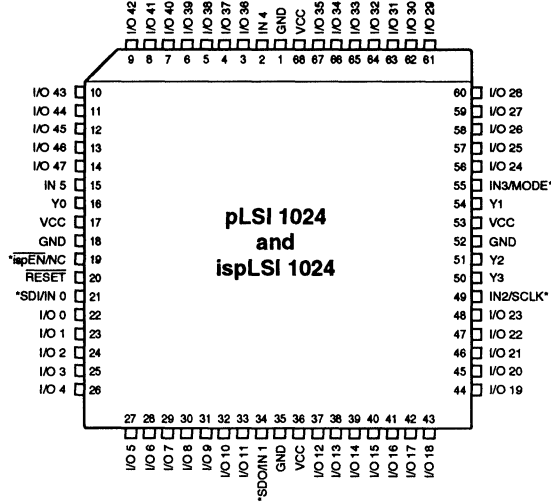
Pin Description

Name	PLCC and JLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47	22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 5	2, 15	Dedicated input pins to the device.
$\overline{\text{ispEN}}^*/\text{NC}$	19	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	21	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 3	55	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 1	34	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 2	49	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	20	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	16	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	54	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	51	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	50	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND VCC	1, 18, 35, 52 17, 36, 53, 68	Ground (GND) V _{cc}

*For ispLSI 1024 Only

Pin Configuration

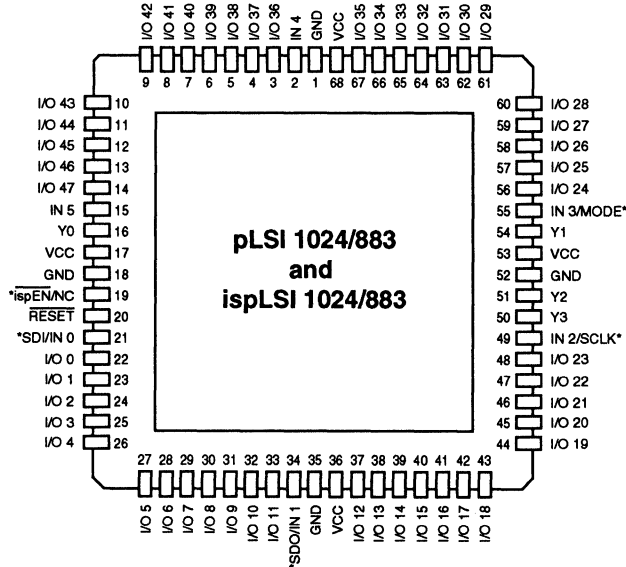
pLSI and ispLSI 1024 68-Pin PLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1024 only (except pin 19, which is $\overline{\text{ispEN}}$ only).

0123C-isp-1024

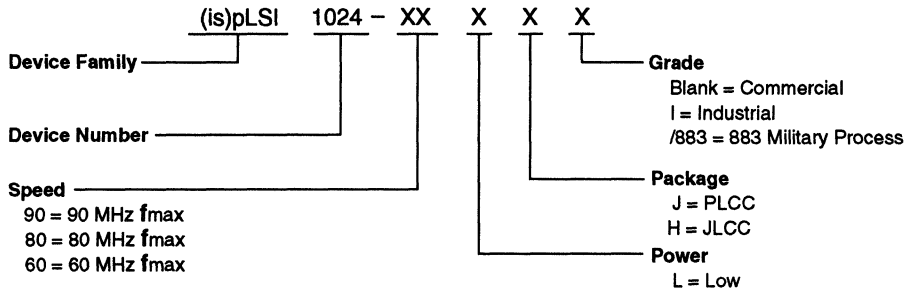
pLSI and ispLSI 1024 68-Pin JLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1024 only (except pin 19, which is $\overline{\text{ispEN}}$ only).

0123-24-ispJLCC

Part Number Description



00212-80B-isp1024

pLSI and ispLSI 1024 Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	90	12	pLSI 1024-90LJ	68-Pin PLCC
	80	15	pLSI 1024-80LJ	68-Pin PLCC
	60	20	pLSI 1024-60LJ	68-Pin PLCC
ispLSI	90	12	ispLSI 1024-90LJ	68-Pin PLCC
	80	15	ispLSI 1024-80LJ	68-Pin PLCC
	60	20	ispLSI 1024-60LJ	68-Pin PLCC

INDUSTRIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	60	20	pLSI 1024-60LJI	68-Pin PLCC
ispLSI	60	20	ispLSI 1024-60LJI	68-Pin PLCC

MILITARY/883

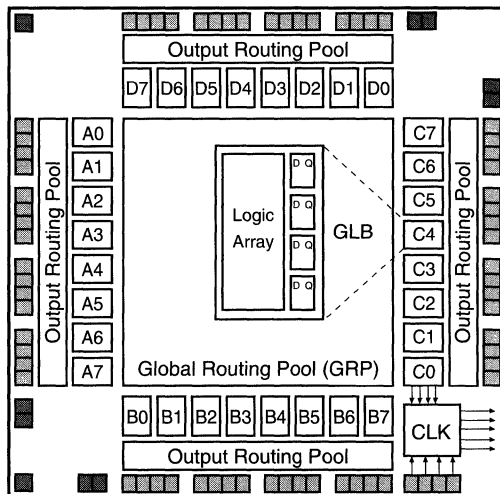
Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	60	20	pLSI 1024-60LH/883	68-Pin JLCC
ispLSI	60	20	ispLSI 1024-60LH/883	68-Pin JLCC

Table 2-0041A-24-isp

Features

- **PROGRAMMABLE AND IN-SYSTEM PROGRAMMABLE HIGH DENSITY LOGIC**
 - High Speed Global Interconnect
 - 6000 PLD Gates
 - 64 I/O Pins, Eight Dedicated Inputs
 - 192 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Fast Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - f_{max} = 90 MHz Maximum Operating Frequency
 - f_{max} = 60 MHz for Industrial and Military/883 Devices
 - t_{pd} = 12 ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile E²CMOS Technology
 - 100% Tested
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System Programmable 5-Volt Only
 - Change Logic and Interconnects "On-the-Fly" in Seconds
 - Reprogram Soldered Device for Debugging
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Four Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS[®])**
 - pDS Software**
 - Easy to Use PC Windows[™] Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+[™] Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning and Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



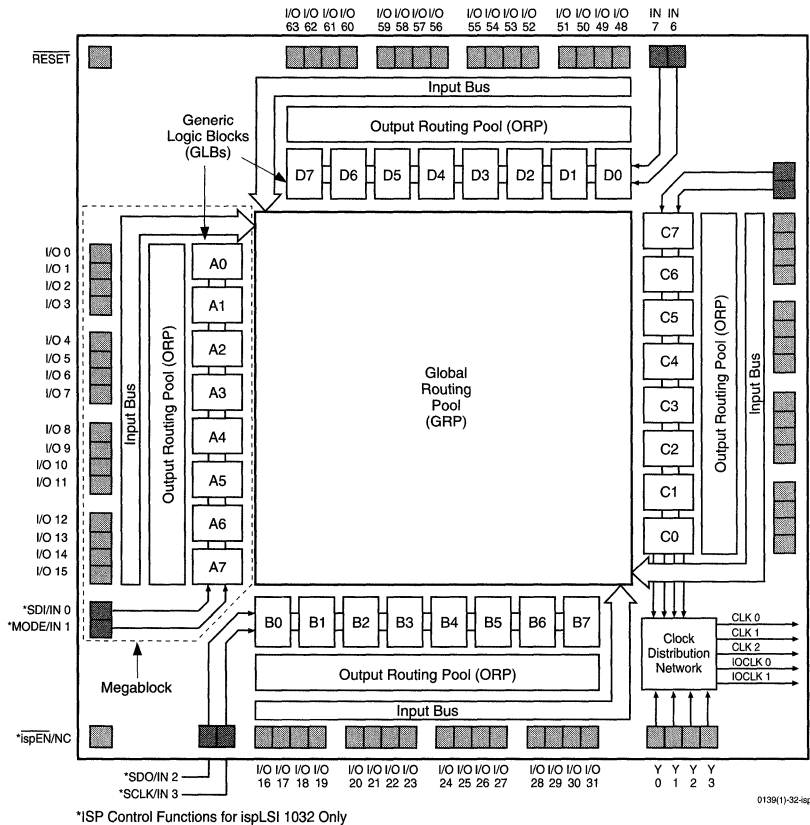
Description

The Lattice pLSI and ispLSI 1032 are High-Density Programmable Logic Devices containing 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1032 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the pLSI and ispLSI 1032 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the pLSI and ispLSI 1032 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. pLSI and ispLSI 1032 Functional Block Diagram



The devices also have 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The pLSI and ispLSI 1032 devices contain four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI and ispLSI 1032 devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the pLSI and ispLSI 1032 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings ¹

- Supply Voltage V_{CC} -0.5 to +7.0V
- Input Voltage Applied. -2.5 to $V_{CC} + 1.0V$
- Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Storage Temperature -65 to 150°C
- Case Temp. with Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
V_{CC}	Supply Voltage	Commercial $T_A = 0^\circ C$ to $+70^\circ C$	4.75	5.25	V
		Industrial $T_A = -40^\circ C$ to $+85^\circ C$	4.5	5.5	
		Military/883 $T_C = -55^\circ C$ to $+125^\circ C$	4.5	5.5	
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	

Table 2- 0005Aisp w/mil.eps

Capacitance ($T_A=25^\circ C, f=1.0$ MHz)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS	
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	$V_{CC}=5.0V, V_{IN}=2.0V$
		Military	10	pf	$V_{CC}=5.0V, V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V, V_{I/O}, V_V=2.0V$	

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	-	YEARS
ispLSI Erase/Reprogram Cycles	1000	-	CYCLES
pLSI Erase/Reprogram Cycles	100	-	CYCLES

Table 2-0008A-isp

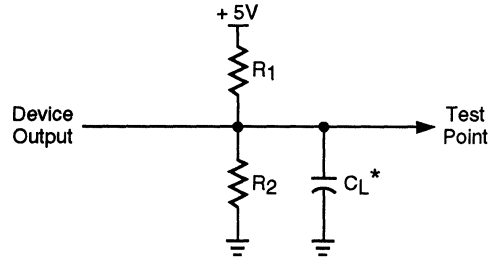
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2-0003

Figure 2. Test Load



* C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition	R1	R2	CL
A	470Ω	390Ω	35pF
B	Active High	∞	390Ω
	Active Low	470Ω	390Ω
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS	
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	-	-	0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	-	-	V	
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	-	-	-10	μA	
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	-	-	10	μA	
I_{IL-isp}	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	-	-	-150	μA	
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	-	-	-150	μA	
I_{OS1}	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	-60	-	-200	mA	
I_{CC2}	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$	Commercial	-	130	190	mA
		$f_{TOGGLE} = 1 \text{ MHz}$	Industrial	-	135	220	mA

1. One output at a time for a maximum duration of one second.
2. Measured using eight 16-bit counters.
3. Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Table 2-0007A-32-isp

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST ⁵ COND.	# ²	DESCRIPTION ¹	-90		-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	-	12	-	15	-	20	ns
t _{pd2}	A	2	Data Propagation Delay, Worst Case Path	-	17	-	20	-	25	ns
f _{max}	A	3	Clock Frequency with Internal Feedback ³	90.9	-	80	-	60	-	MHz
f _{max} (Ext.)	-	4	Clock Frequency with External Feedback ³ $(\frac{1}{t_{su2} + t_{co1}})$	58.8	-	50	-	38	-	MHz
f _{max} (Tog.)	-	5	Clock Frequency, Max Toggle ⁴	125	-	100	-	83	-	MHz
t _{su1}	-	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	-	7	-	9	-	ns
t _{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	-	8	-	10	-	13	ns
t _{h1}	-	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	-	0	-	0	-	ns
t _{su2}	-	9	GLB Reg. Setup Time before Clock	9	-	10	-	13	-	ns
t _{co2}	-	10	GLB Reg. Clock to Output Delay	-	10	-	12	-	16	ns
t _{h2}	-	11	GLB Reg. Hold Time after Clock	0	-	0	-	0	-	ns
t _{r1}	A	12	Ext. Reset Pin to Output Delay	-	15	-	17	-	22.5	ns
t _{rw1}	-	13	Ext. Reset Pulse Duration	10	-	10	-	13	-	ns
t _{en}	B	14	Input to Output Enable	-	15	-	18	-	24	ns
t _{dis}	C	15	Input to Output Disable	-	15	-	18	-	24	ns
t _{wh}	-	16	Ext. Sync. Clock Pulse Duration, High	4	-	5	-	6	-	ns
t _{wl}	-	17	Ext. Sync. Clock Pulse Duration, Low	4	-	5	-	6	-	ns
t _{su5}	-	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	-	2	-	2.5	-	ns
t _{h5}	-	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	-	6.5	-	8.5	-	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, ORP and Y0 clock.

Table 2-0030-32/90,80,60C

2. Refer to Timing Model in this data sheet for further details.

3. Standard 16-Bit counter using GRP feedback.

 4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.

5. Reference Switching Test Conditions Section.

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{iobp}	20	I/O Register Bypass	-	1.6	-	2.0	-	2.7	ns
t_{iolat}	21	I/O Latch Delay	-	2.4	-	3.0	-	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	4.8	-	5.5	-	7.3	-	ns
t_{iOh}	23	I/O Register Hold Time after Clock	2.1	-	1.0	-	1.3	-	ns
t_{ioco}	24	I/O Register Clock to Out Delay	-	2.4	-	3.0	-	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	-	2.8	-	2.5	-	3.3	ns
t_{din}	26	Dedicated Input Delay	-	3.2	-	4.0	-	5.3	ns
GRP									
t_{grp1}	27	GRP Delay, 1 GLB Load	-	1.2	-	1.5	-	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	-	1.6	-	2.0	-	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	-	2.4	-	3.0	-	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	-	3.0	-	3.8	-	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	-	3.6	-	4.5	-	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	-	6.4	-	8.0	-	10.6	ns
GLB									
t_{4ptbp}	33	4 Product Term Bypass Path Delay	-	5.2	-	6.5	-	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	-	5.7	-	7.0	-	9.3	ns
t_{20ptxor}	35	20 Product Term/XOR Path Delay	-	7.0	-	8.0	-	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay ³	-	8.2	-	9.5	-	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	-	0.8	-	1.0	-	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.2	-	1.0	-	1.3	-	ns
t_{gh}	39	GLB Register Hold Time after Clock	3.6	-	4.5	-	6.0	-	ns
t_{gco}	40	GLB Register Clock to Output Delay	-	1.6	-	2.0	-	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	-	2.0	-	2.5	-	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	-	8.0	-	10.0	-	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	-	7.8	-	9.0	-	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	2.8	6.0	3.5	7.5	4.6	9.9	ns
ORP									
t_{orp}	45	ORP Delay	-	2.4	-	2.5	-	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	-	0.4	-	0.5	-	0.7	ns

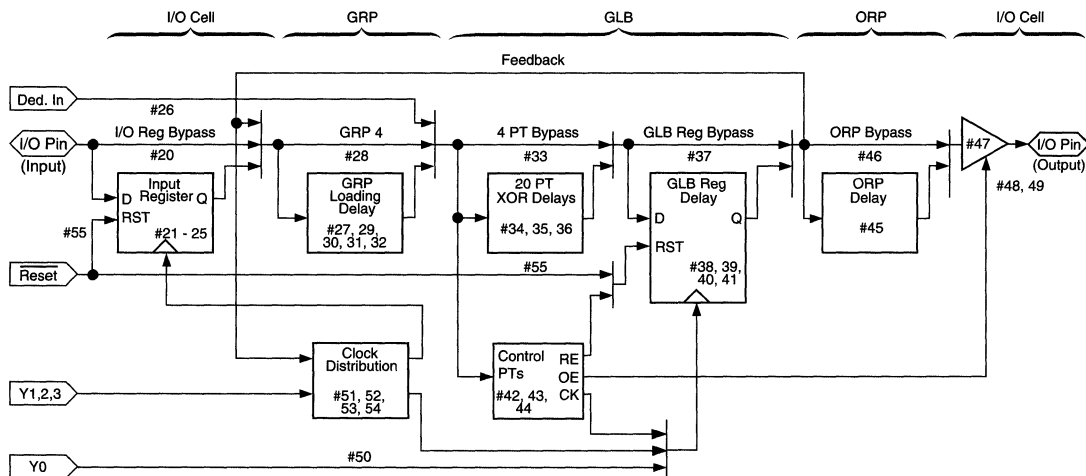
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	47	Output Buffer Delay	–	2.4	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.6	3.6	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
Global Reset									
t_{gr}	55	Global Reset to GLB and I/O Registers	–	8.2	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

pLSI and ispLSI 1032 Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

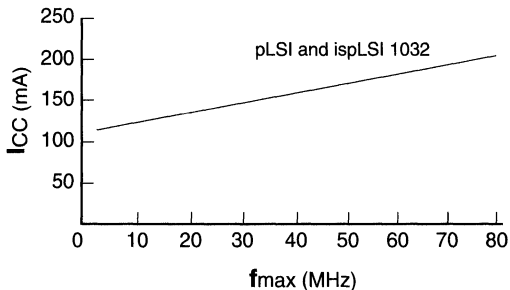
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 5.5 \text{ ns} &= (2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 4.0 \text{ ns} &= (2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 19.0 \text{ ns} &= (2.0 + 2.0 + 7.5) + (2.0) + (2.5 + 3.0)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
 5.5 \text{ ns} &= (2.0 + 2.0 + 8.0) + (1.0) - (4.5 + 2.0 + 1.0) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
 4.0 \text{ ns} &= (4.5 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
 19.0 \text{ ns} &= (4.5 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)
 \end{aligned}$$

1. Calculations are based upon timing specs for the pLSI and ispLSI 1032-80.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit Counters
Typical Current at 5V, 25°C

ICC can be estimated for the pLSI and ispLSI 1032 using the following equation:

$$I_{CC} = 52 + (\# \text{ of PTs} * 0.30) + (\# \text{ of nets} * \text{Max. freq} * 0.009) \text{ where:}$$

of PTs = Number of Product Terms used in design

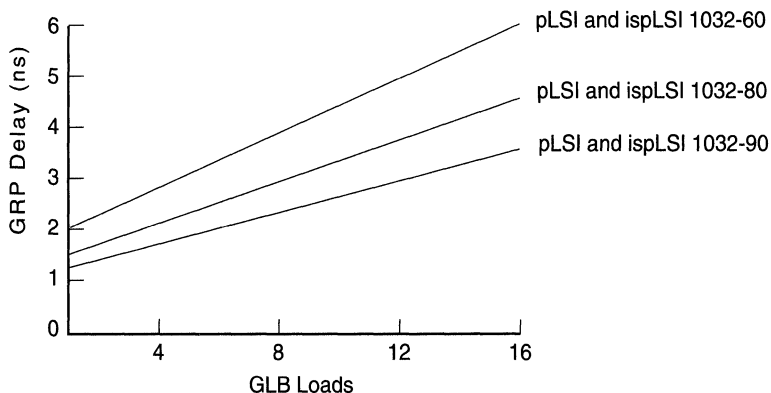
of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A-32-80-isp

Figure 4. Maximum GRP Delay vs GLB Loads



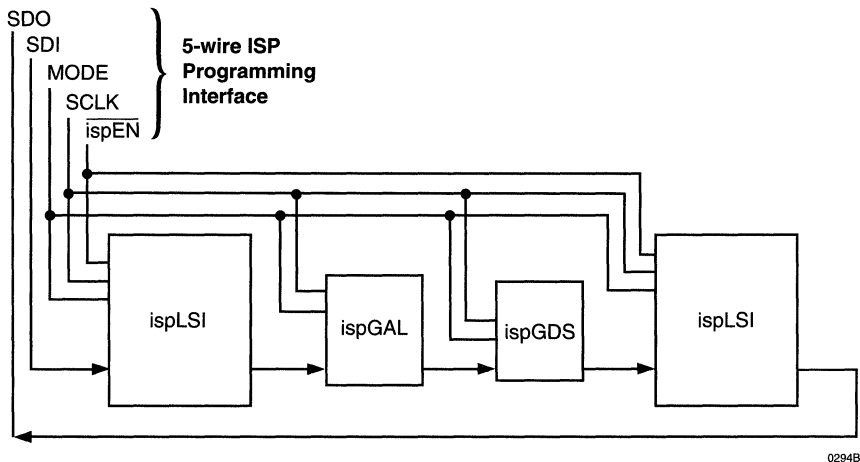
0126A-80-32-isp

In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this Data Book.

Figure 5. ISP Programming Interface



0294B

ISP Programming Voltage/Timing Specifications¹

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCP}	Programming Voltage		4.75	5	5.25	V
I _{CCP}	Programming Supply Current		–	50	100	mA
V _{IHP}	Input Voltage High	$\overline{\text{ispEN}} = \text{Low}$	2.0	–	V _{CCP}	V
V _{ILP}	Input Voltage Low		0	–	0.8	V
I _{IP}	Input Current		–	100	200	μA
V _{OHP}	Output Voltage High	I _{OH} = -3.2 mA	2.4	–	V _{CCP}	V
V _{OLP}	Output Voltage Low	I _{OL} = 5 mA	0	–	0.5	V
t _r , t _f	Input Rise and Fall		–	–	0.1	μs
t _{ispEN}	$\overline{\text{ispEN}}$ to Output 3-State Enabled		–	2	10	μs
t _{ispDIS}	$\overline{\text{ispEN}}$ to Output 3-State Disabled		–	2	10	μs
t _{su}	Setup Time		0.1	0.5	–	μs
t _{co}	Clock to Output		0.1	0.5	–	μs
t _h	Hold Time		0.1	0.5	–	μs
t _{clkh} , t _{ckl}	Clock Pulse Width, High and Low		0.5	1	–	μs
t _{pwv}	Verify Pulse Width		20	30	–	μs
t _{pwP}	Programming Pulse Width		40	–	100	ms
t _{bew}	Bulk Erase Pulse Width		200	–	–	ms
t _{rst}	Reset Time From Valid V _{CCP}		45	–	–	μs

1. ISP Programming is guaranteed for T_A = 0°C to 70°C Operation only.

Table 2- 0029 isp-C

Figure 6. Timing Waveforms for In-System Programming (ispLSI 1032)

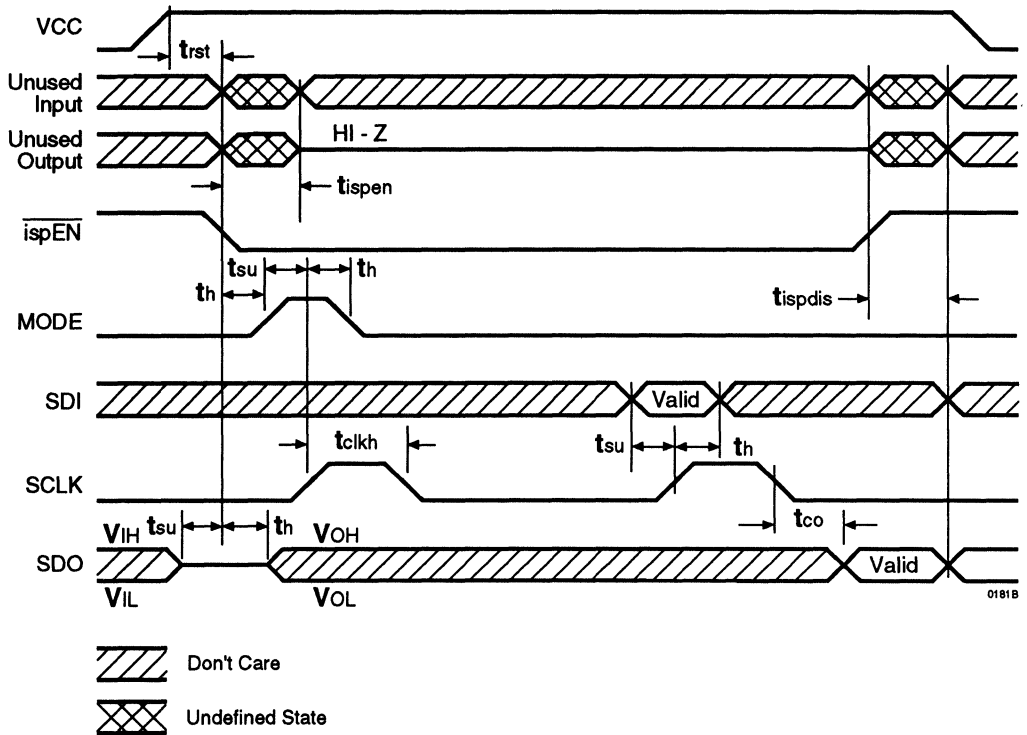


Figure 7. Program, Verify & Bulk Erase Waveforms (ispLSI 1032)

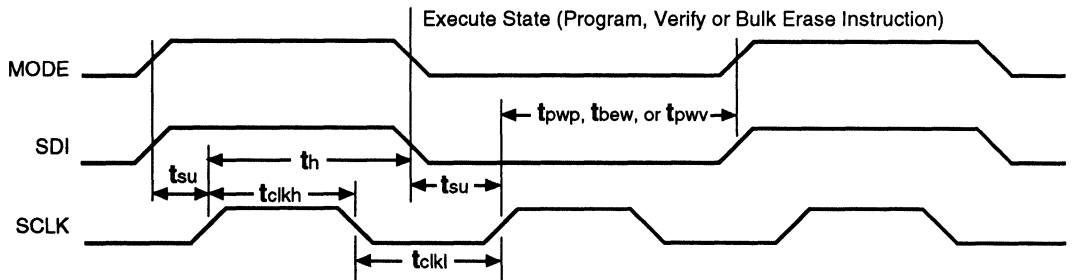
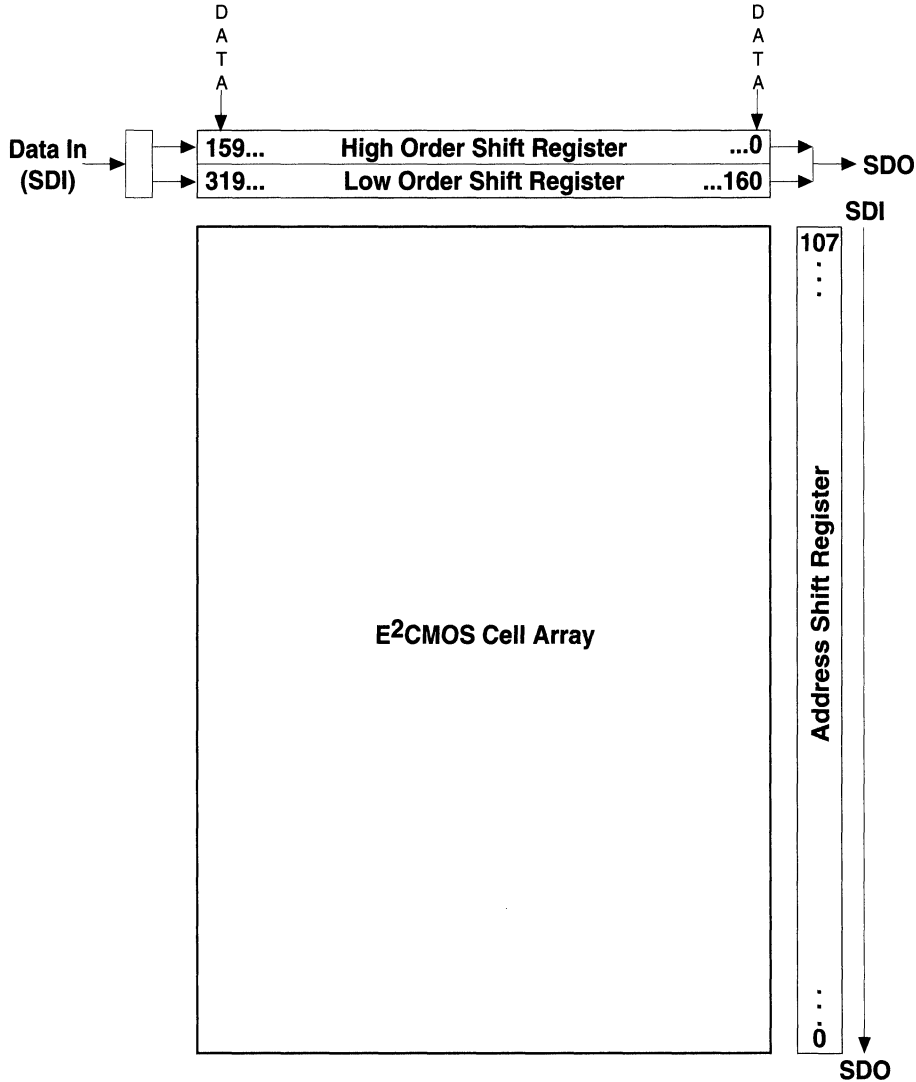


Figure 8 illustrates the address and data shift register bits for the ispLSI 1032. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book.

Figure 8. ispLSI 1032 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	67, 84, 2, 19	Dedicated input pins to the device.
$\overline{\text{ispEN}}$ */NC	23	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	25	<u>Input</u> – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	42	<u>Input</u> – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 2	44	<u>Input/Output</u> – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 3	61	<u>Input</u> – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	24	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	20	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	66	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	63	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND VCC	1, 22, 43, 64 21, 65	Ground (GND) V _{cc}

* For ispLSI 1032 Only

Table 2-0002A-32-isp

Pin Description

Name	TQFP Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 35, 36, 40, 41, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 58, 59, 67, 68, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 85, 86, 90, 91, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7, 8, 9	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	66, 87, 89, 10	Dedicated input pins to the device.
ispEN*/NC	14	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	16	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	37	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 2	39	Input/Output – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 3	60	Input – This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
NC	1, 2, 24, 25, 26, 27, 49, 50, 51, 52, 74, 75 76, 77, 99, 100	These pins are not used.
RESET	15	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	65	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	61	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	13, 38, 63, 88	Ground (GND)
V _{CC}	12, 64	V _{CC}

* For ispLSI 1032 Only

Table 2- 0002B-32-isp

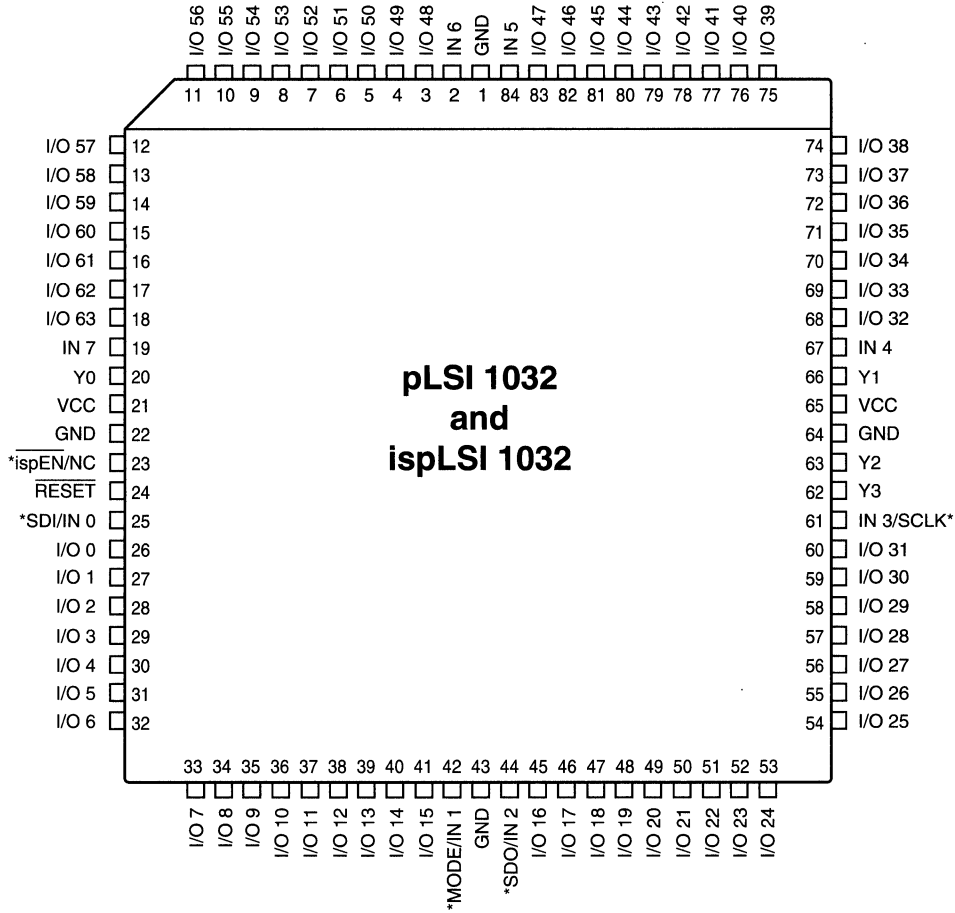
Pin Description

Name	CPGA Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	F1, H1, H2, J1, K1, J2, L1, K2, K3, L2, L3, K4, L4, J5, K5, L5, L7, K7, L6, L8, K8, L9, L10, K9, L11, K10, J10, K11, J11, H10, H11, F10, E9, D11, D10, C11, B11, C10, A11, B10, B9, A10, A9, B8, A8, B6, B7, A7, A5, B5, C5, A4, B4, A3, A2, B3, A1, B2, C2, B1, C1, D2, D1, E3	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	E10, C7, A6, E2	Dedicated input pins to the device.
$\overline{\text{ispEN}}^*/\text{NC}$	G3	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	G2	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	K6	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 2	J7	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 3	G10	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	G1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	E1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	E11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	G9	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	G11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC	G3	This pin should be left floating or tied to V_{cc} . This pin should never be tied to GND.
GND VCC	C6, F3, F9, J6 F2, F11	Ground (GND) V_{cc}

Table 2-0002-32/83

Pin Configuration

pLSI and ispLSI 1032 84-Pin PLCC Pinout Diagram

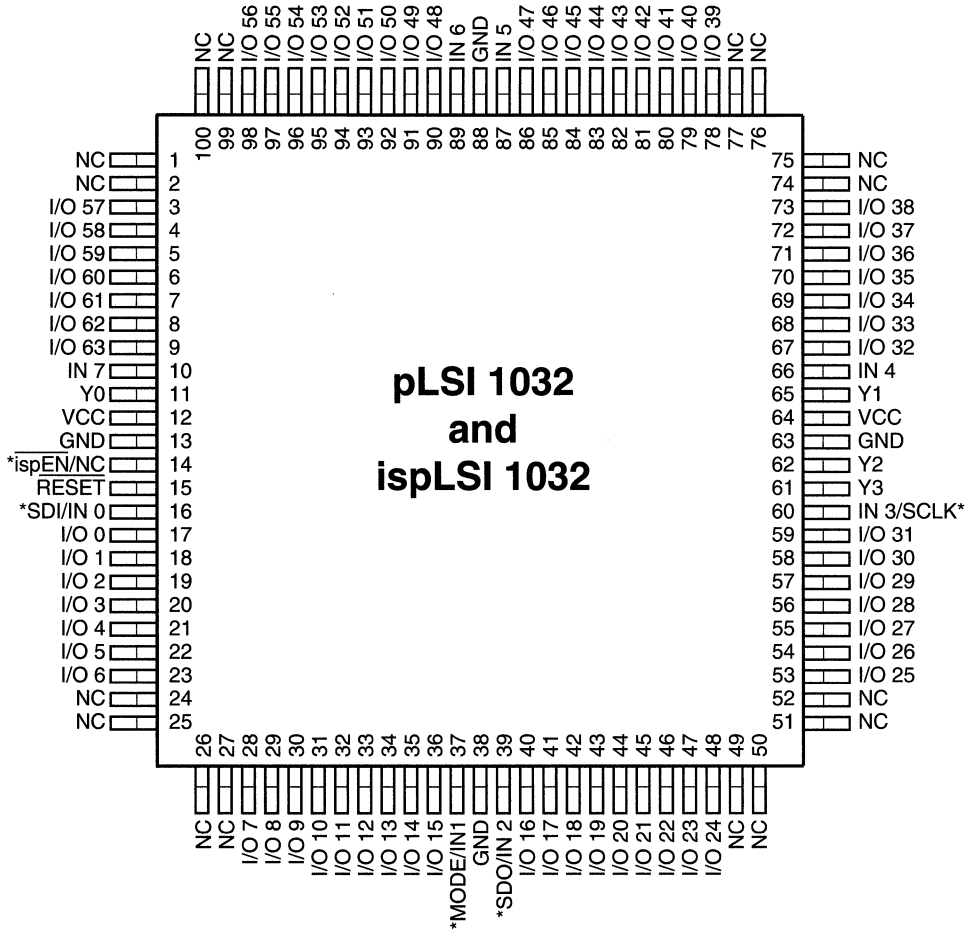


*Pins have dual function capability for ispLSI 1032 only (except pin 23, which is $\overline{\text{ispEN}}$ only).

0123-32-isp

Pin Configuration

pLSI and ispLSI 1032 100-pin TQFP Pinout Diagram

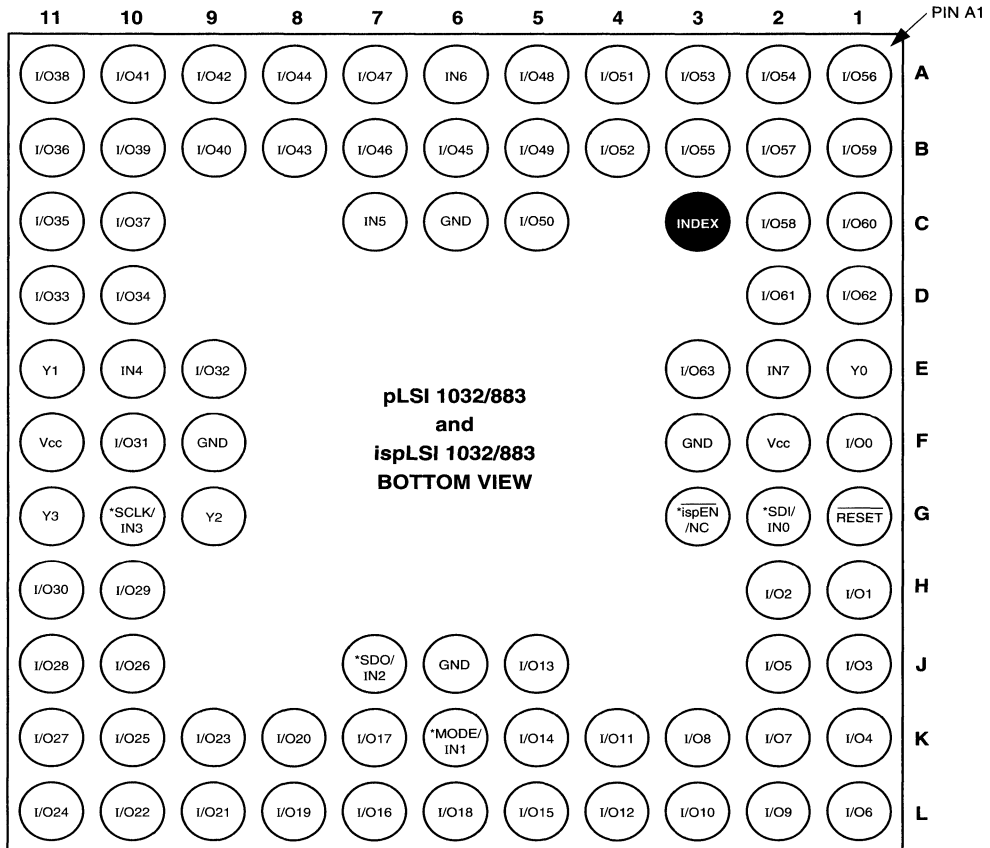


*Pins have dual function capability for ispLSI 1032 only (except pin 14, which is ispEN only).

0766A-32-isp

Pin Configuration

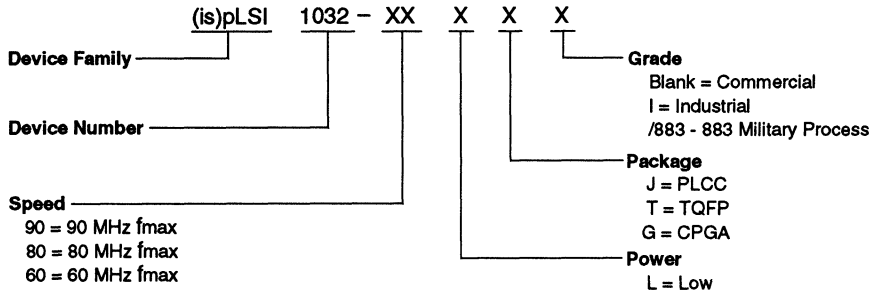
pLSI and ispLSI 1032/883 84-Pin CPGA Pinout Diagram



*Pins have dual function capability for ispLSI 1032/883 only (except pin 63, which is $\overline{\text{ispEN}}$ only).

0488A-32-isp/883

Part Number Description



00212-808-isp1032

pLSI and ispLSI 1032 Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	90	12	pLSI 1032-90LJ	84-Pin PLCC
	90	12	pLSI 1032-90LT	100-Pin TQFP
	80	15	pLSI 1032-80LJ	84-Pin PLCC
	80	15	pLSI 1032-80LT	100-Pin TQFP
	60	20	pLSI 1032-60LJ	84-Pin PLCC
	60	20	pLSI 1032-60LT	100-Pin TQFP
ispLSI	90	12	ispLSI 1032-90LJ	84-Pin PLCC
	90	12	ispLSI 1032-90LT	100-Pin TQFP
	80	15	ispLSI 1032-80LJ	84-Pin PLCC
	80	15	ispLSI 1032-80LT	100-Pin TQFP
	60	20	ispLSI 1032-60LJ	84-Pin PLCC
	60	20	ispLSI 1032-60LT	100-Pin TQFP

INDUSTRIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	60	20	pLSI 1032-60LJI	84-Pin PLCC
ispLSI	60	20	ispLSI 1032-60LJI	84-Pin PLCC

MILITARY/883

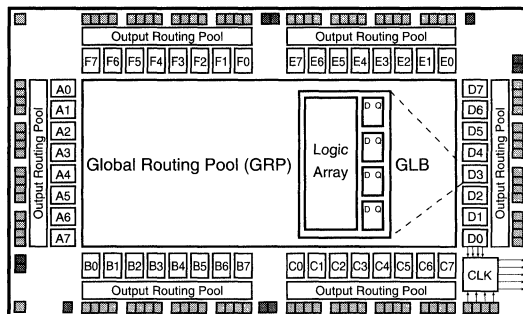
Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	SMD Number	Package
pLSI	60	20	pLSI 1032-60LG/883	5962-9466801MXC	84-Pin CPGA
ispLSI	60	20	ispLSI 1032-60LG/883	5962-9308501MXC	84-Pin CPGA

Table 2-0041A-32-isp

Features

- **PROGRAMMABLE AND IN-SYSTEM PROGRAMMABLE HIGH DENSITY LOGIC**
 - High-Speed Global Interconnects
 - 8000 PLD Gates
 - 96 I/O Pins, Ten Dedicated Inputs
 - 288 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - $f_{max} = 80$ MHz Maximum Operating Frequency
 - $f_{max} = 50$ MHz for Industrial Devices
 - $t_{pd} = 15$ ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile E²CMOS Technology
 - 100% Tested
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System Programmable 5-Volt Only
 - Change Logic and Interconnects "On-the-Fly" in Seconds
 - Reprogram Soldered Device for Debugging
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Four Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS[®])**
 - pDS Software**
 - Easy to Use PC Windows[™] Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+[™] Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning and Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



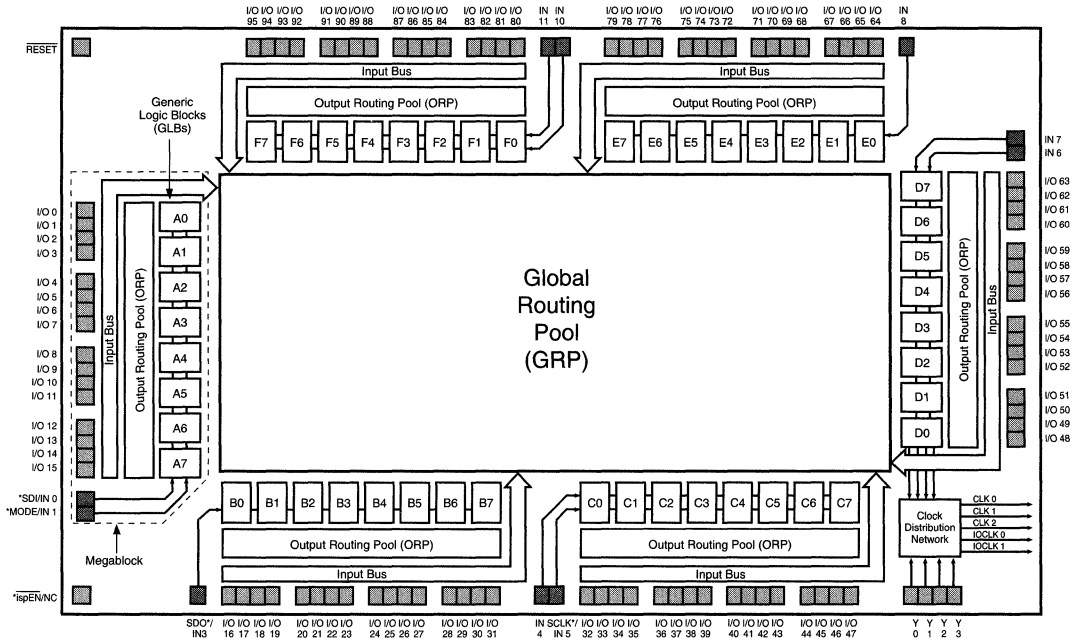
Description

The Lattice pLSI and ispLSI 1048 are High-Density Programmable Logic Devices which contain 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the pLSI and ispLSI 1048 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see figure 1). There are a total of 48 GLBs in the pLSI and ispLSI 1048 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. pLSI and ispLSI 1048 Functional Block Diagram



*ISP Control Functions for ispLSI 1048 Only

0139F(1)-48-isp

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs (one dedicated input in Megablock B and E) and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The pLSI and ispLSI 1048 devices contain six of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI and ispLSI 1048 devices are selected using the Clock Distribution Network. Four dedicated clockpins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the pLSI and ispLSI 1048 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings ¹

- Supply Voltage V_{CC} -0.5 to +7.0V
- Input Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Storage Temperature -65 to 150°C
- Case Temp. with Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
V_{CC}	Supply Voltage	Commercial $T_A = 0^\circ C$ to $+70^\circ C$	4.75	5.25	V
		Industrial $T_A = -40^\circ C$ to $+85^\circ C$	4.5	5.5	
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	

Capacitance ($T_A=25^\circ C$, $f=1.0$ MHz)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	$V_{CC}=5.0V$, $V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V$, V_{IO} , $V_Y=2.0V$

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	-	YEARS
ispLSI Erase/Reprogram Cycles	1000	-	CYCLES
pLSI Erase/Reprogram Cycles	100	-	CYCLES

Table 2-0008A-isp.eps

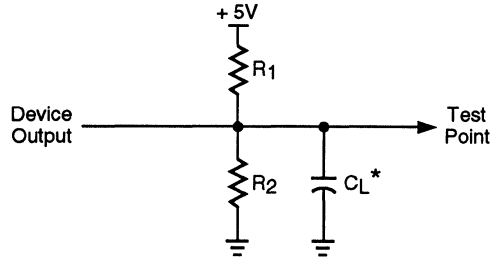
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



* C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition	R1	R2	CL
A	470Ω	390Ω	35pF
B	Active High	∞	390Ω
	Active Low	470Ω	390Ω
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
VOL	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	—	—	0.4	V
VOH	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	—	—	V
IIL	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	—	—	-10	μA
IiH	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
IIL-isp	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	—	—	-150	μA
IIL-PU	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	—	—	-150	μA
IOS1	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	-60	—	-200	mA
ICC²	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$	Commercial	165	235	mA
		$f_{TOGGLE} = 1 \text{ MHz}$	Industrial	165	260	mA

- One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- Measured using twelve 16-bit counters.
- Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Table 2- 0007A-48-isp

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND. ⁵	# ²	DESCRIPTION ¹	-80		-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	-	15	-	18	-	24	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	-	20	-	23	-	30.7	ns
f_{max}	A	3	Clock Frequency with Internal Feedback ³	80	-	71.4	-	53.6	-	MHz
f_{max} (Ext.)	-	4	Clock Frequency with External Feedback ($\frac{1}{t_{su2} + t_{co1}}$)	50	-	41.7	-	31.3	-	MHz
f_{max} (Tog.)	-	5	Clock Frequency, Max Toggle ⁴	100	-	83	-	71.4	-	MHz
t_{su1}	-	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	-	9	-	12	-	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	-	10	-	12	-	16	ns
t_{h1}	-	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	-	0	-	0	-	ns
t_{su2}	-	9	GLB Reg. Setup Time before Clock	10	-	12	-	16	-	ns
t_{co2}	-	10	GLB Reg. Clock to Output Delay	-	12	-	14	-	18.7	ns
t_{h2}	-	11	GLB Reg. Hold Time after Clock	0	-	0	-	0	-	ns
t_{tr1}	A	12	Ext. Reset Pin to Output Delay	-	17	-	17	-	22.7	ns
t_{rw1}	-	13	Ext. Reset Pulse Duration	10	-	10	-	13	-	ns
t_{en}	B	14	Input to Output Enable	-	18	-	20	-	26.7	ns
t_{dis}	C	15	Input to Output Disable	-	18	-	20	-	26.7	ns
t_{wh}	-	16	Ext. Sync. Clock Pulse Duration, High	5	-	6	-	7	-	ns
t_{wl}	-	17	Ext. Sync. Clock Pulse Duration, Low	5	-	6	-	7	-	ns
t_{su5}	-	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	-	2	-	2.7	-	ns
t_{h5}	-	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	-	6.5	-	8.7	-	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Table 2- 0030A-48/80,70,50

2

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-80		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t _{iobp}	20	I/O Register Bypass	–	2.5	–	3.0	–	4.0	ns
t _{iolat}	21	I/O Latch Delay	–	3.3	–	4.0	–	5.3	ns
t _{iosu}	22	I/O Register Setup Time before Clock	5.3	–	6.0	–	8.1	–	ns
t _{ioh}	23	I/O Register Hold Time after Clock	1.5	–	0.5	–	0.9	–	ns
t _{ioco}	24	I/O Register Clock to Out Delay	–	2.5	–	3.0	–	3.9	ns
t _{ior}	25	I/O Register Reset to Out Delay	–	2.9	–	3.5	–	4.6	ns
t _{din}	26	Dedicated Input Delay	–	5.0	–	6.0	–	8.0	ns
GRP									
t _{grp1}	27	GRP Delay, 1 GLB Load	–	2.1	–	2.5	–	3.3	ns
t _{grp4}	28	GRP Delay, 4 GLB Loads	–	2.5	–	3.0	–	4.0	ns
t _{grp8}	29	GRP Delay, 8 GLB Loads	–	3.3	–	4.0	–	5.3	ns
t _{grp12}	30	GRP Delay, 12 GLB Loads	–	4.2	–	5.0	–	6.7	ns
t _{grp16}	31	GRP Delay, 16 GLB Loads	–	5.0	–	6.0	–	8.0	ns
t _{grp48}	32	GRP Delay, 48 GLB Loads	–	13.3	–	16.0	–	21.3	ns
GLB									
t _{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.4	–	6.5	–	8.6	ns
t _{1ptxor}	34	1 Product Term/XOR Path Delay	–	6.5	–	7.0	–	9.3	ns
t _{20ptxor}	35	20 Product Term/XOR Path Delay	–	7.6	–	7.5	–	10.0	ns
t _{xoradj}	36	XOR Adjacent Path Delay ³	–	8.4	–	9.5	–	12.7	ns
t _{gbp}	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
t _{gsu}	38	GLB Register Setup Time before Clock	0.8	–	1.5	–	2.0	–	ns
t _{gh}	39	GLB Register Hold Time after Clock	5.0	–	6.0	–	8.0	–	ns
t _{gco}	40	GLB Register Clock to Output Delay	–	2.1	–	2.5	–	3.3	ns
t _{gr}	41	GLB Register Reset to Output Delay	–	2.1	–	2.5	–	3.3	ns
t _{ptre}	42	GLB Product Term Reset to Register Delay	–	8.3	–	10.0	–	13.3	ns
t _{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	8.8	–	9.0	–	11.9	ns
t _{ptck}	44	GLB Product Term Clock Delay	2.9	6.3	3.5	7.5	4.6	9.9	ns
ORP									
t _{orp}	45	ORP Delay	–	3.2	–	3.5	–	4.7	ns
t _{orpbp}	46	ORP Bypass Delay	–	1.3	–	1.5	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Table 2- 0036A-48/80,70,50.eps

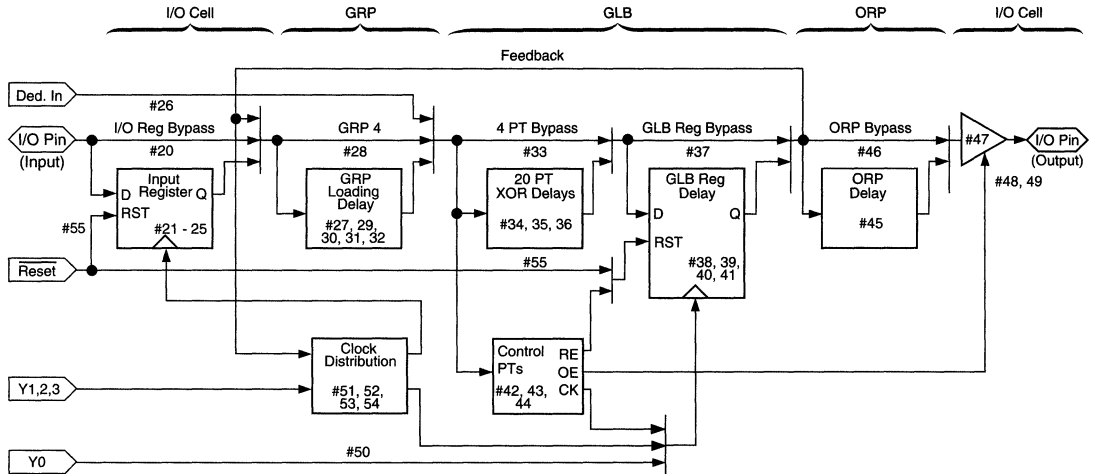
Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-80		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t _{ob}	47	Output Buffer Delay	-	2.5	-	3.0	-	4.0	ns
t _{oen}	48	I/O Cell OE to Output Enabled	-	4.2	-	5.0	-	6.7	ns
t _{odis}	49	I/O Cell OE to Output Disabled	-	4.2	-	5.0	-	6.7	ns
Clocks									
t _{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.2	4.2	5.0	5.0	6.7	6.7	ns
t _{gy1/2}	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.3	5.0	4.0	6.0	5.3	8.0	ns
t _{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.2	1.0	5.0	1.3	6.6	ns
t _{ioy2/3}	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	3.3	5.0	4.0	6.0	5.3	8.0	ns
t _{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.2	1.0	5.0	1.3	6.6	ns
Global Reset									
t _{gr}	55	Global Reset to GLB and I/O Registers	-	9.2	-	8.0	-	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

2

pLSI and ispLSI 1048 Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

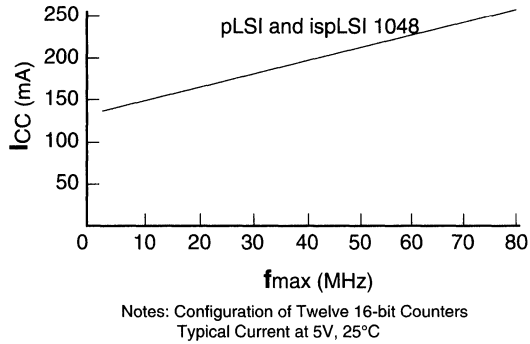
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 5.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (1.5) - (3.0 + 3.0 + 3.5) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 6.0 \text{ ns} &= (3.0 + 3.0 + 7.5) + (6.0) - (3.0 + 3.0 + 7.5) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 22.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (2.5) + (3.5 + 3.0)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
 6.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (1.5) - (5.0 + 2.5 + 1.0) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
 5.0 \text{ ns} &= (5.0 + 2.5 + 5.0) + (6.0) - (3.0 + 3.0 + 7.5) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
 21.5 \text{ ns} &= (5.0 + 2.5 + 5.0) + (2.5) + (3.5 + 3.0)
 \end{aligned}$$

1. Calculations are based upon timing specs for the pLSI and ispLSI 1048-70.

Figure 3. Typical Device Power Consumption vs fmax



2

ICC can be estimated for the pLSI and ispLSI 1048 using the following equation:

$$I_{CC} = 73 + (\# \text{ of PTs} * 0.23) + (\# \text{ of nets} * \text{Max. freq} * 0.010) \text{ where:}$$

of PTs = Number of Product Terms used in design

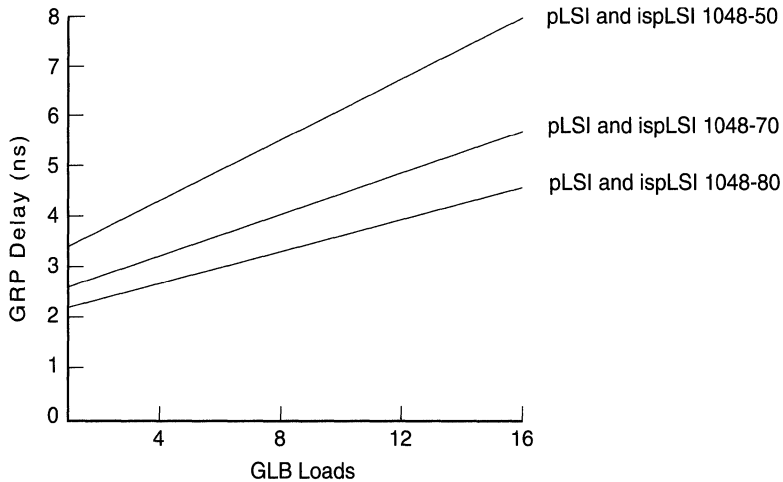
of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A-48-80-isp

Figure 4. Maximum GRP Delay vs GLB Loads



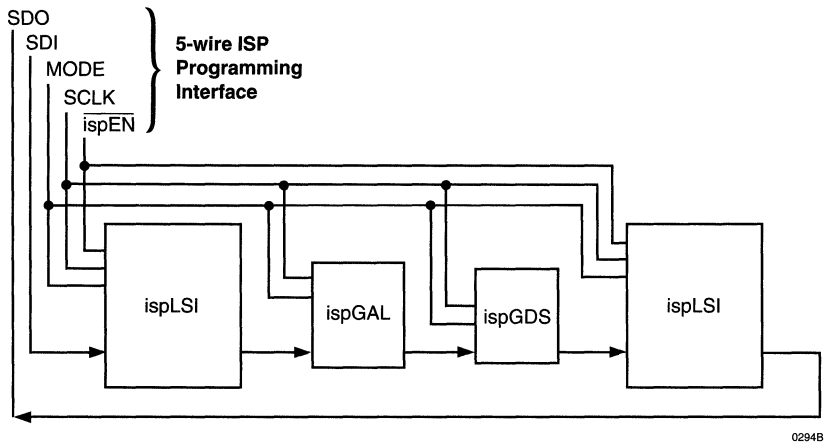
0126A-48-80-isp

In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this Data Book.

Figure 5. ISP Programming Interface



SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.75	5	5.25	V
I_{CCP}	Programming Supply Current		–	50	100	mA
V_{IHP}	Input Voltage High	$\overline{\text{ispEN}} = \text{Low}$	2.0	–	V _{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	μA
V_{OHP}	Output Voltage High	I _{OH} = -3.2 mA	2.4	–	V _{CCP}	V
V_{OLP}	Output Voltage Low	I _{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	μs
t_{ispEN}	$\overline{\text{ispEN}}$ to Output 3-State Enabled		–	2	10	μs
t_{ispDIS}	$\overline{\text{ispEN}}$ to Output 3-State Disabled		–	2	10	μs
t_{su}	Setup Time		0.1	0.5	–	μs
t_{co}	Clock to Output		0.1	0.5	–	μs
t_h	Hold Time		0.1	0.5	–	μs
t_{clkH}, t_{clkL}	Clock Pulse Width, High and Low		0.5	1	–	μs
t_{pwv}	Verify Pulse Width		20	30	–	μs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V _{CCP}		45	–	–	μs

 1. ISP Programming is guaranteed for T_A = 0°C to 70°C Operation only.

Table 2-0028 isp-C

Figure 6. Timing Waveforms for In-System Programming (ispLSI 1048)

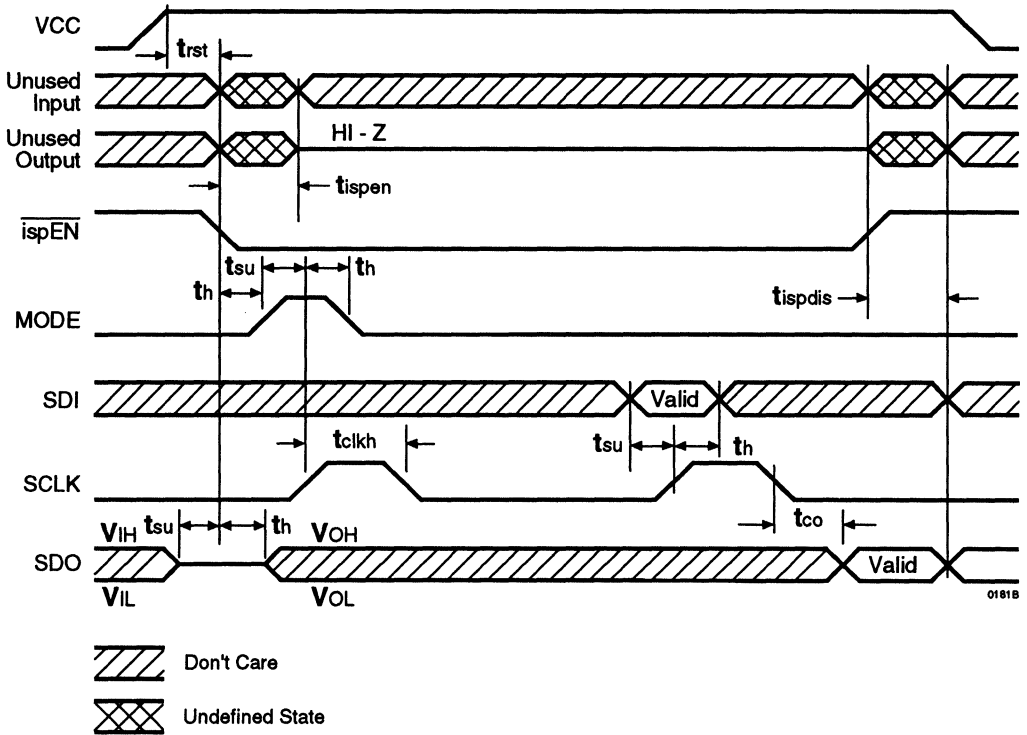


Figure 7. Program, Verify & Bulk Erase Waveforms (ispLSI 1048)

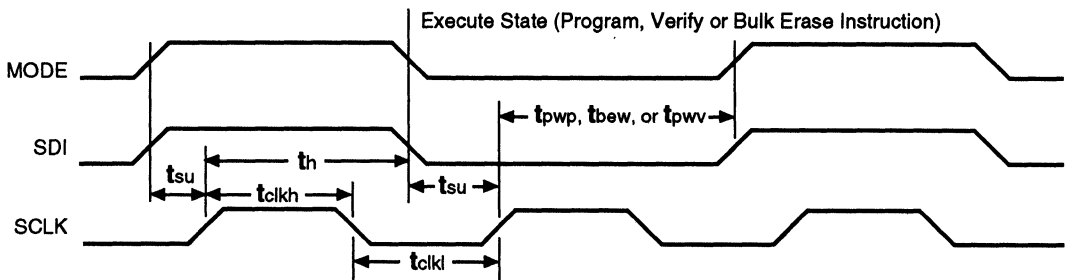
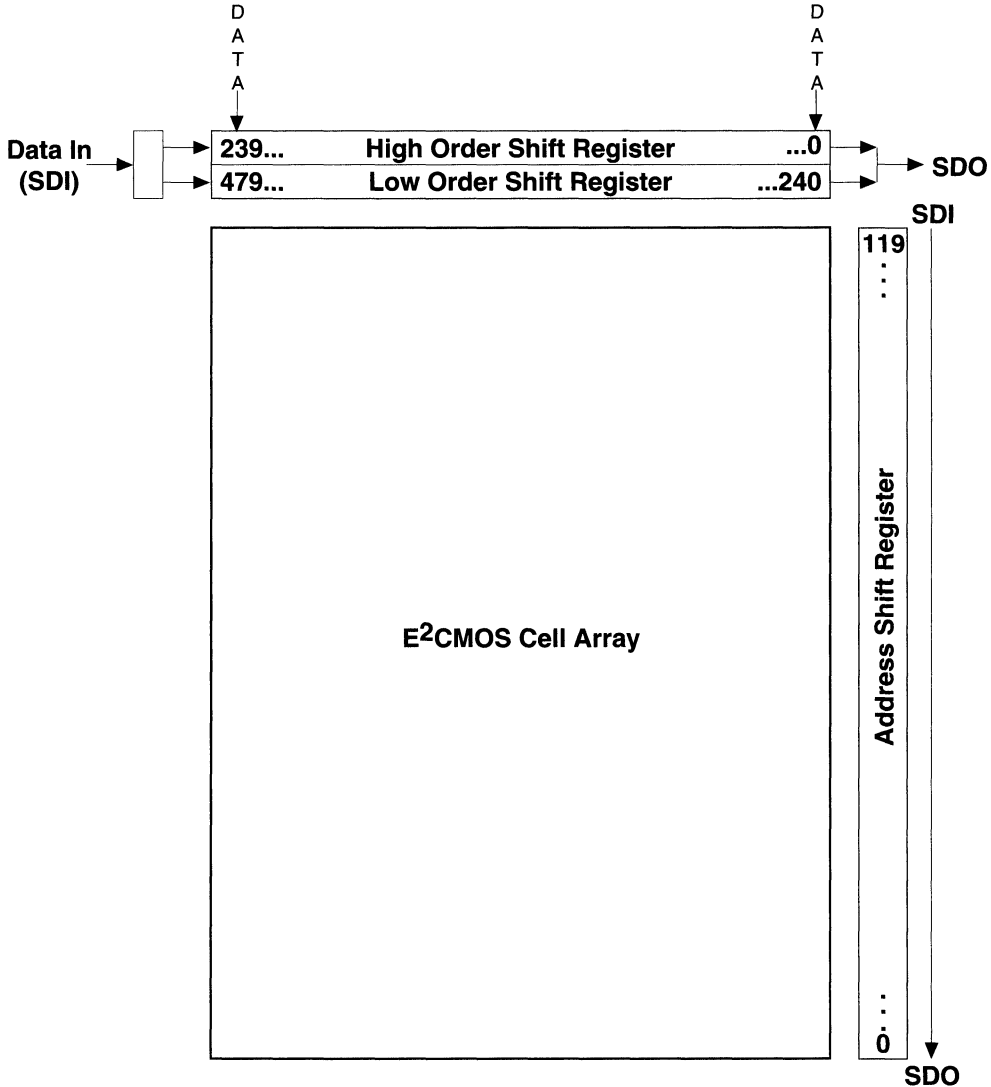


Figure 8 illustrates the address and data shift register bits for the ispLSI 1048. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book.

Figure 8. ispLSI 1048 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

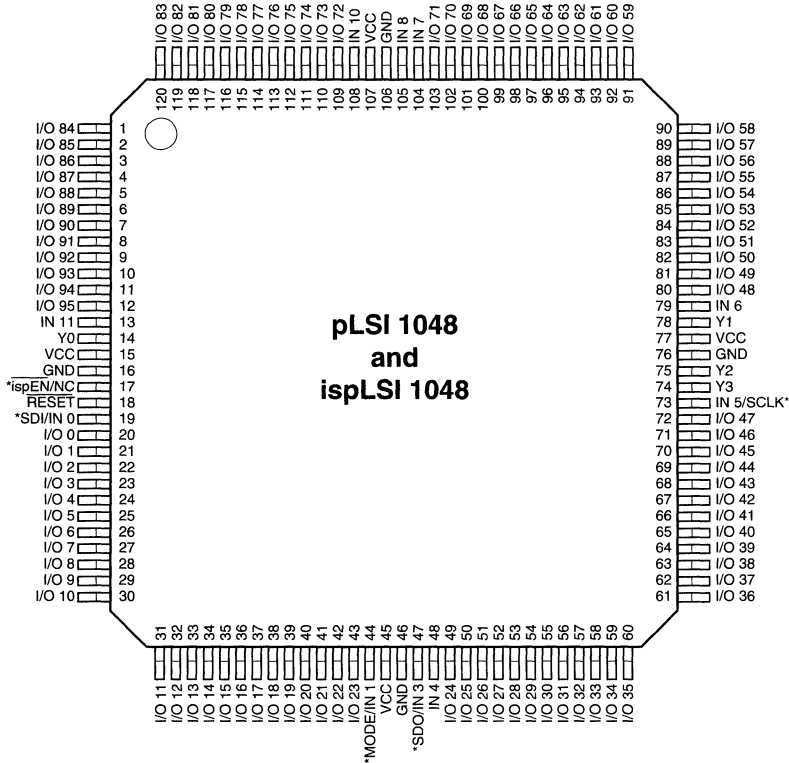
Name	PQFP Pin Numbers	Description
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 IN 6 - IN 11	48, 79, 104, 105, - 108, 13	Dedicated input pins to the device. (IN 2 and IN 9 not available)
$\overline{\text{ispEN}}^*/\text{NC}$ SDI*/IN 0 MODE*/IN 1 SDO*/IN 3 SCLK*/IN 5	17 19 44 47 73	<p>Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.</p> <p>Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.</p> <p>Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.</p> <p>Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.</p> <p>Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.</p>
$\overline{\text{RESET}}$ Y0 Y1 Y2 Y3	18 14 78 75 74	<p>Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.</p> <p>Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.</p> <p>Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.</p> <p>Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.</p> <p>Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.</p>
GND VCC	46, 76, 106, 16 15, 45, 77, 107	Ground (GND) V _{cc}

*For ispLSI 1048 Only

Table 2- 0002C-48-isp

Pin Configuration

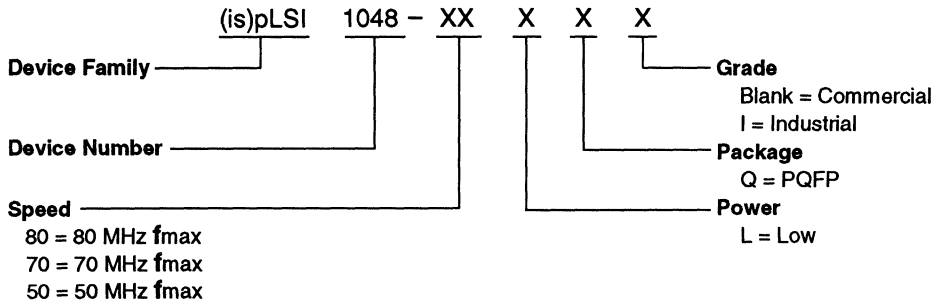
pLSI and ispLSI 1048 120-Pin PQFP Pinout Diagram



* Pins have dual function capability for ispLSI 1048 only (except pin 17, which is $\overline{\text{ispEN}}$ only).

0124-48-isp

Part Number Description



0212-80B-isp1048

pLSI and ispLSI 1048 Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	80	15	pLSI 1048-80LQ	120-Pin PQFP
	70	18	pLSI 1048-70LQ	120-Pin PQFP
	50	24	pLSI 1048-50LQ	120-Pin PQFP
ispLSI	80	15	pLSI 1048-80LQ	120-Pin PQFP
	70	18	ispLSI 1048-70LQ	120-Pin PQFP
	50	24	ispLSI 1048-50LQ	120-Pin PQFP

INDUSTRIAL

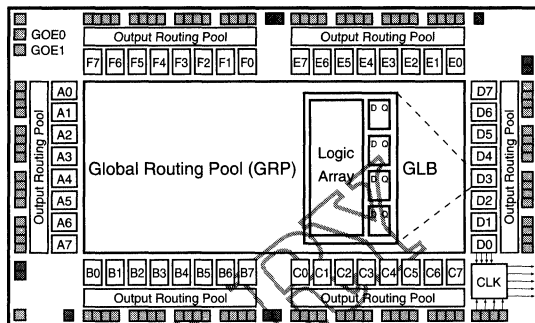
Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	50	24	pLSI 1048-50LQI	120-Pin PQFP
ispLSI	50	24	ispLSI 1048-50LQI	120-Pin PQFP

Table 2-0041A-48-isp

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
 - High-Speed Global Interconnects
 - 96 I/O Pins, 12 Dedicated Inputs, 2 Global Output Enables
 - 288 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - $f_{max} = 70$ MHz Maximum Operating Frequency
 - $f_{max} = 50$ MHz for Industrial Devices
 - $t_{pd} = 18$ ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile E²CMOS Technology
 - 100% Tested at Time of Manufacture
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System Programmable 5-Volt Only
 - Change Logic and Interconnects "On-the-Fly" in Seconds
 - Reprogram Soldered Device for Debugging
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Four Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS[®])**
 - pDS Software**
 - Easy to Use PC Windows[™] Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+[™] Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning and Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



0139G1A-isp

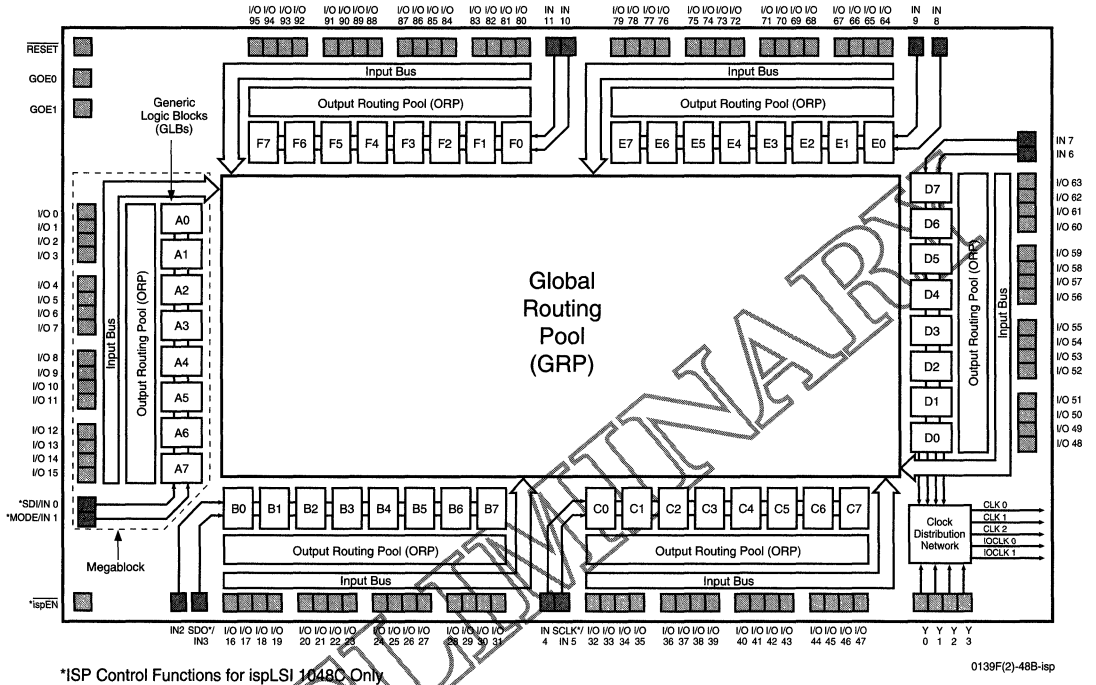
Description

The Lattice pLSI and ispLSI 1048C are High-Density Programmable Logic Devices containing 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, two global output enables (GOE), four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048C features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048C device, but multiplexes four of the dedicated input pins to control in-system programming. Compared to the pLSI and ispLSI 1048, the pLSI and ispLSI 1048C offers two additional dedicated inputs and two new global output enable pins.

The basic unit of logic on the pLSI and ispLSI 1048C devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see figure 1). There are a total of 48 GLBs in the pLSI and ispLSI 1048C devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. pLSI and ispLSI 1048C Functional Block Diagram



*ISP Control Functions for ispLSI 1048C Only

0139F(2)-48B-isp

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The pLSI and ispLSI 1048C devices contains six of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI and ispLSI 1048C devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the pLSI and ispLSI 1048C devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings ¹

- Supply Voltage V_{CC} -0.5 to +7.0V
- Input Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Storage Temperature -65 to 150°C
- Case Temp. with Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
V_{CC}	Supply Voltage	Commercial $T_A = 0^\circ C$ to $+70^\circ C$	4.75	5.25	V
		Industrial $T_A = -40^\circ C$ to $+85^\circ C$	4.5	5.5	
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	

Capacitance ($T_A=25^\circ C$, $f=1.0$ MHz)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	$V_{CC}=5.0V$, $V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V$, V_{IO} , $V_I=2.0V$

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	-	YEARS
ispLSI Erase/Reprogram Cycles	1000	-	CYCLES
pLSI Erase/Reprogram Cycles	100	-	CYCLES

Table 2-0008A-isp

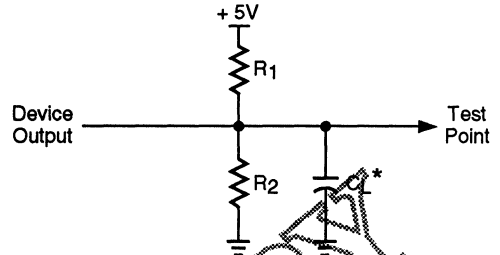
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



*CL includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition	R1	R2	CL
A	470Ω	390Ω	35pF
B	Active High	∞	390Ω
	Active Low	470Ω	390Ω
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω

Table 2- 0004

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS	
VOL	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	—	—	0.4	V	
VOH	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	—	—	V	
IIL	Input I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	—	—	-10	μA	
IIH	Input I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA	
IIL-isp	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	—	—	-150	μA	
IIL-PU	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	—	—	-150	μA	
IOS1	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	-60	—	-200	mA	
ICC ²	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$	Commercial	—	165	235	mA
		$f_{TOGGLE} = 1 \text{ MHz}$	Industrial	—	165	260	mA

1. One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.

2. Measured using twelve 16-bit counters.

3. Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Table 2- 0007A-48-isp

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST ⁵ COND.	# ²	DESCRIPTION ¹	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
t _{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	-	18.0	-	24.0	ns
t _{pd2}	A	2	Data Propagation Delay	-	20.5	-	27.0	ns
f _{max}	A	3	Clock Frequency with Internal Feedback ³	71.4	-	54.1	-	MHz
f _{max} (Ext.)	-	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	46.5	-	35.1	-	MHz
f _{max} (Tog.)	-	5	Clock Frequency, Max Toggle ⁴	83.3	-	62.5	-	MHz
t _{su1}	-	6	GLB Reg. Setup Time before Clock, 4PT bypass	9.0	-	12.0	-	ns
t _{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	-	11.0	-	14.5	ns
t _{h1}	-	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	-	0	-	ns
t _{su2}	-	9	GLB Reg. Setup Time before Clock	10.5	-	14.0	-	ns
t _{co2}	-	10	GLB Reg. Clock to Output Delay	-	12.0	-	15.5	ns
t _{h2}	-	11	GLB Reg. Hold Time after Clock	0	-	0	-	ns
t _{r1}	A	12	Ext. Reset Pin to Output Delay	-	15.0	-	20.0	ns
t _{rw1}	-	13	Ext. Reset Pulse Duration	10.0	-	13.0	-	ns
t _{ptoen}	B	14	Input to Output Enable	-	20.0	-	26.5	ns
t _{ptoedis}	C	15	Input to Output Disable	-	20.0	-	26.5	ns
t _{goen}	B	16	Global OE Output Enable	-	15.0	-	20.0	ns
t _{goedis}	C	17	Global OE Output Disable	-	15.0	-	20.0	ns
t _{wh}	-	20	Ext. Sync. Clock Pulse Duration, High	6.0	-	8.0	-	ns
t _{wl}	-	21	Ext. Sync. Clock Pulse Duration, Low	6.0	-	8.0	-	ns
t _{su3}	-	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.0	-	2.5	-	ns
t _{h3}	-	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	-	8.5	-	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Table 2- 0030-48B/70, 50

2

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t _{iobp}	24	I/O Register Bypass	–	3.1	–	4.1	ns
t _{iolat}	25	I/O Latch Delay	–	4.0	–	5.3	ns
t _{iosu}	26	I/O Register Setup Time before Clock	6.5	–	8.5	–	ns
t _{ioh}	27	I/O Register Hold Time after Clock	0.1	–	0.1	–	ns
t _{ioco}	28	I/O Register Clock to Out Delay	–	3.1	–	4.1	ns
t _{ior}	29	I/O Register Reset to Out Delay	–	3.4	–	4.5	ns
t _{din}	30	Dedicated Input Delay	–	5.4	–	7.2	ns
GRP							
t _{grp1}	31	GRP Delay, 1 GLB Load	–	4.5	–	6.0	ns
t _{grp4}	32	GRP Delay, 4 GLB Loads	–	4.9	–	6.5	ns
t _{grp8}	33	GRP Delay, 8 GLB Loads	–	5.8	–	7.7	ns
t _{grp12}	34	GRP Delay, 12 GLB Loads	–	6.7	–	8.9	ns
t _{grp16}	35	GRP Delay, 16 GLB Loads	–	7.6	–	10.1	ns
t _{grp48}	36	GRP Delay, 48 GLB Loads	–	16.5	–	22.0	ns
GLB							
t _{4ptbp}	37	4 Product Term Bypass Path Delay	–	5.0	–	6.7	ns
t _{1ptxor}	38	1 Product Term/XOR Path Delay	–	5.8	–	7.8	ns
t _{20ptxor}	39	20 Product Term/XOR Path Delay	–	6.5	–	8.7	ns
t _{xoradj}	40	XOR Adjacent Path Delay ³	–	8.0	–	10.7	ns
t _{gbp}	41	GLB Register Bypass Delay	–	0.9	–	1.2	ns
t _{gsu}	42	GLB Register Setup Time before Clock	1.4	–	1.9	–	ns
t _{gh}	43	GLB Register Hold Time after Clock	5.3	–	7.1	–	ns
t _{gco}	44	GLB Register Clock to Output Delay	–	1.5	–	1.8	ns
t _{gr}	45	GLB Register Reset to Output Delay	–	2.1	–	2.8	ns
t _{ptre}	46	GLB Product Term Reset to Register Delay	–	8.6	–	11.5	ns
t _{ptoe}	47	GLB Product Term Output Enable to I/O Cell Delay	–	7.0	–	9.2	ns
t _{ptck}	48	GLB Product Term Clock Delay	3.0	6.5	4.0	8.7	ns
ORP							
t _{orp}	49	ORP Delay	–	2.5	–	3.0	ns
t _{orpbp}	50	ORP Bypass Delay	–	1.5	–	1.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Table 2- 0036-48B/70, 50

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	51	Output Buffer Delay	–	2.6	–	3.5	ns
t_{oen}	52	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	53	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	5.4	5.4	7.2	7.2	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.5	6.4	6.0	8.6	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	1.9	5.5	2.5	7.3	ns
$t_{ioy2/3}$	57	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.5	6.4	6.0	8.6	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.9	5.5	2.5	7.3	ns
Global Reset							
t_{gr}	59	Global Reset to GLB and I/O Registers	–	7.8	–	10.3	ns

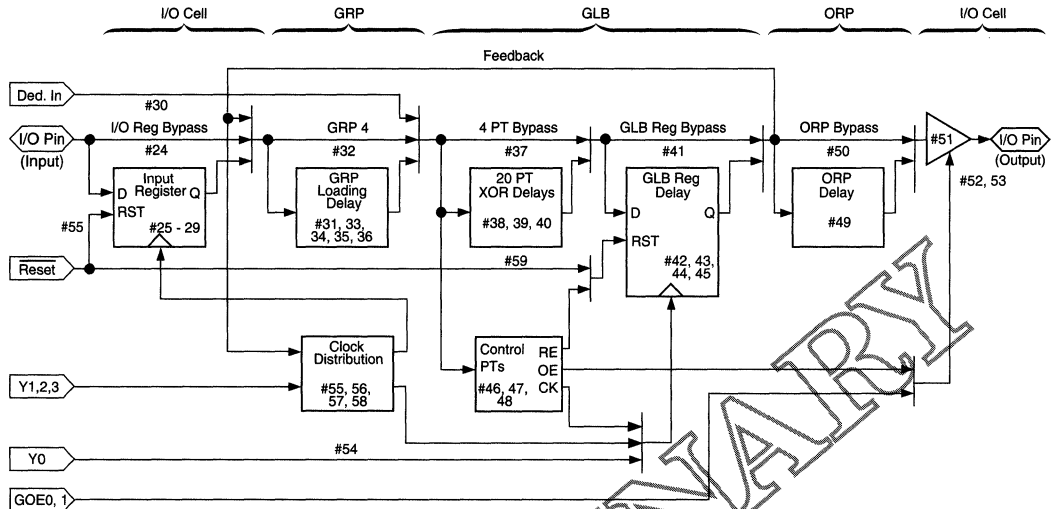
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Table 2-0037-48C/70, 50

PRELIMINARY

2

pLSI and ispLSI 1048C Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

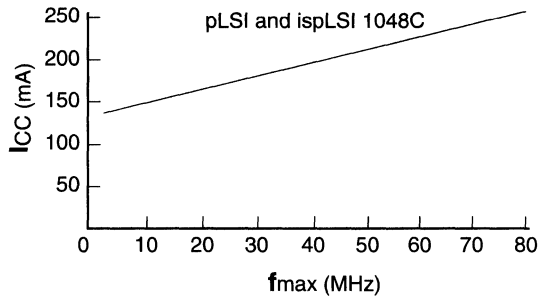
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#24 + \#32 + \#39) + (\#42) - (\#24 + \#32 + \#48) \\
 5.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (1.5) - (3.0 + 3.0 + 3.5) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#24 + \#32 + \#48) + (\#43) - (\#24 + \#32 + \#39) \\
 6.0 \text{ ns} &= (3.0 + 3.0 + 7.5) + (6.0) - (3.0 + 3.0 + 7.5) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#24 + \#32 + \#48) + (\#44) + (\#49 + \#51) \\
 22.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (2.5) + (3.5 + 3.0)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#24 + \#32 + \#39) + (\#42) - (\#54 + \#44 + \#56) \\
 6.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (1.5) - (5.0 + 2.5 + 1.0) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#54 + \#44 + \#56) + (\#43) - (\#24 + \#32 + \#39) \\
 5.0 \text{ ns} &= (5.0 + 2.5 + 5.0) + (6.0) - (3.0 + 3.0 + 7.5) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#54 + \#44 + \#56) + (\#44) + (\#49 + \#51) \\
 21.5 \text{ ns} &= (5.0 + 2.5 + 5.0) + (2.5) + (3.5 + 3.0)
 \end{aligned}$$

1. Calculations are based upon timing specs for the pLSI/ispLSI 1048C-70.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Twelve 16-bit Counters
Typical Current at 5V, 25°C

ICC can be estimated for the pLSI and ispLSI 1048C using the following equation:

$$I_{CC} = 73 + (\# \text{ of PTs} * 0.23) + (\# \text{ of nets} * \text{Max. freq} * 0.010) \text{ where:}$$

of PTs = Number of Product Terms used in design

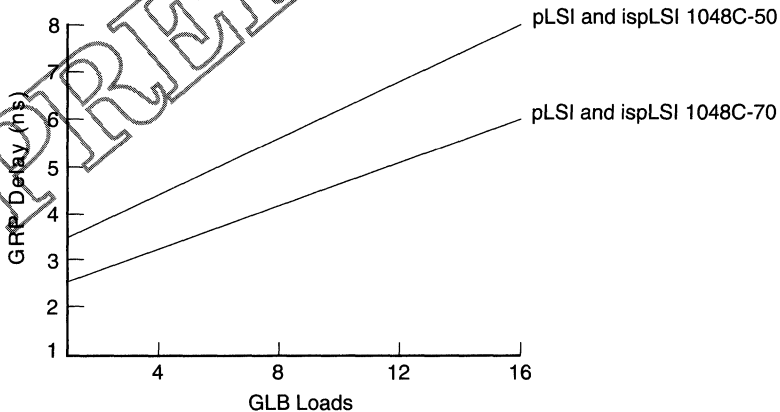
of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A-48C-80-isp

Figure 4. Maximum GRP Delay vs GLB Loads



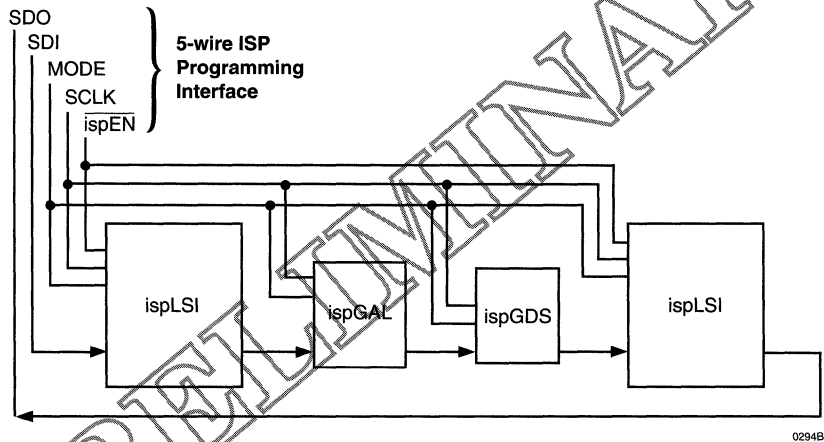
0126A-48B-80-isp

In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 5 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this Data Book.

Figure 5. ISP Programming Interface



ISP Programming Voltage/Timing Specifications¹

2

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCP}	Programming Voltage		4.75	5	5.25	V
I _{CCP}	Programming Supply Current		–	50	100	mA
V _{IHP}	Input Voltage High	ispEN = Low	2.0	–	V _{CCP}	V
V _{ILP}	Input Voltage Low		0	–	0.8	V
I _{IP}	Input Current		–	100	200	μA
V _{OHP}	Output Voltage High	I _{OH} = -3.2 mA	2.4	–	V _{CCP}	V
V _{OLP}	Output Voltage Low	I _{OL} = 5 mA	0	–	0.5	V
t _r , t _f	Input Rise and Fall		–	–	0.1	μs
t _{ispen}	ispEN to Output 3-State Enabled		–	2	10	μs
t _{ispdis}	ispEN to Output 3-State Disabled		–	2	10	μs
t _{su}	Setup Time		0.1	0.5	–	μs
t _{co}	Clock to Output		0.1	0.5	–	μs
t _h	Hold Time		0.1	0.5	–	μs
t _{clkh} , t _{cikl}	Clock Pulse Width, High and Low		0.5	1	–	μs
t _{pwv}	Verify Pulse Width		20	30	–	μs
t _{pwp}	Programming Pulse Width		40	–	100	ms
t _{bew}	Bulk Erase Pulse Width		200	–	–	ms
t _{rst}	Reset Time From Valid V _{CCP}		45	–	–	μs

1. ISP Programming is guaranteed for T_A = 0°C to 70°C Operation only.

Table 2-0029 isp-C

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Figure 6. Timing Waveforms for In-System Programming

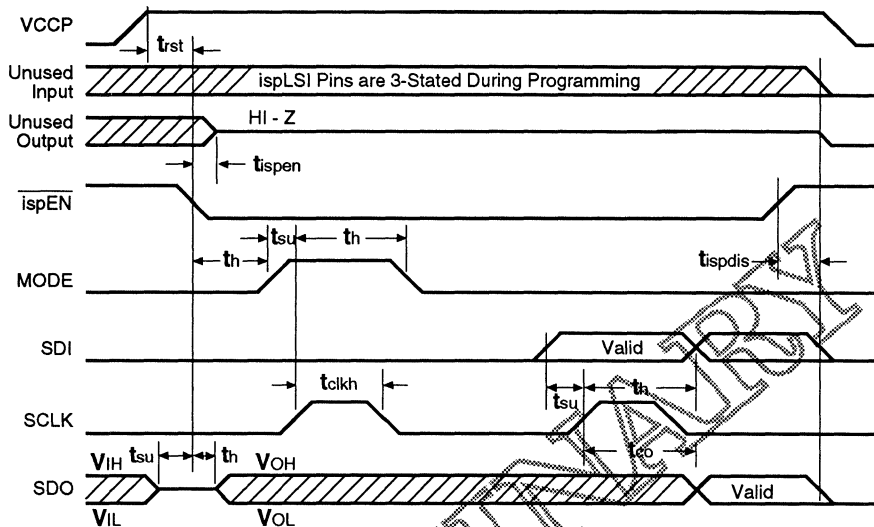


Figure 7. Program, Verify & Bulk Erase Waveforms

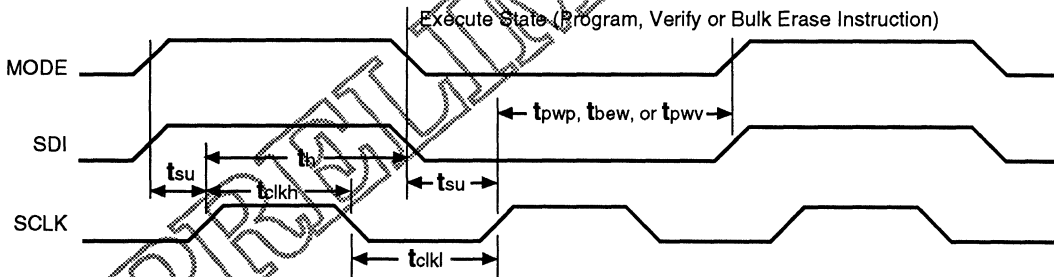
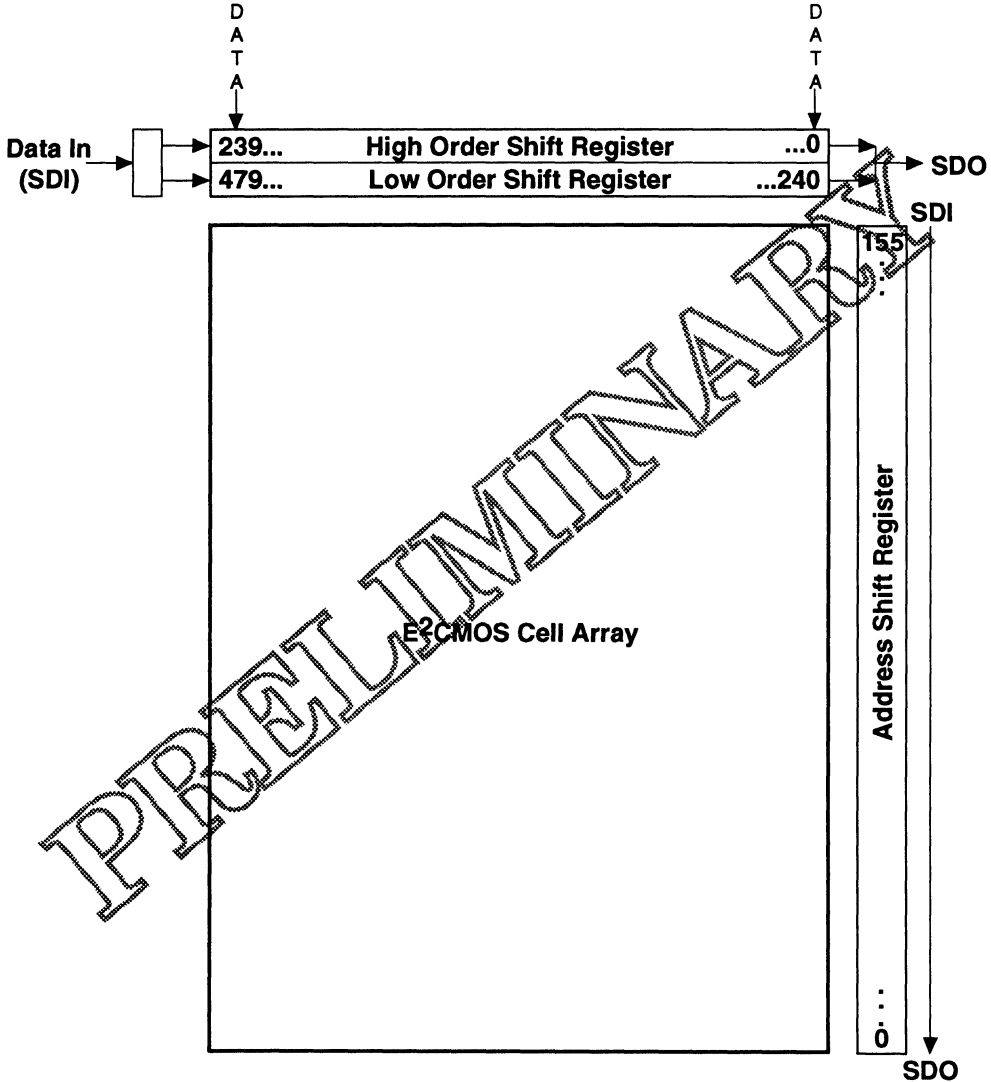


Figure 8 illustrates the address and data shift register bits for the ispLSI 1048C. For a detailed explanation refer to the Device Layout discussion in the pLSI and ispLSI Architectural Description section of this Data Book.

Figure 8. ispLSI 1048C Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

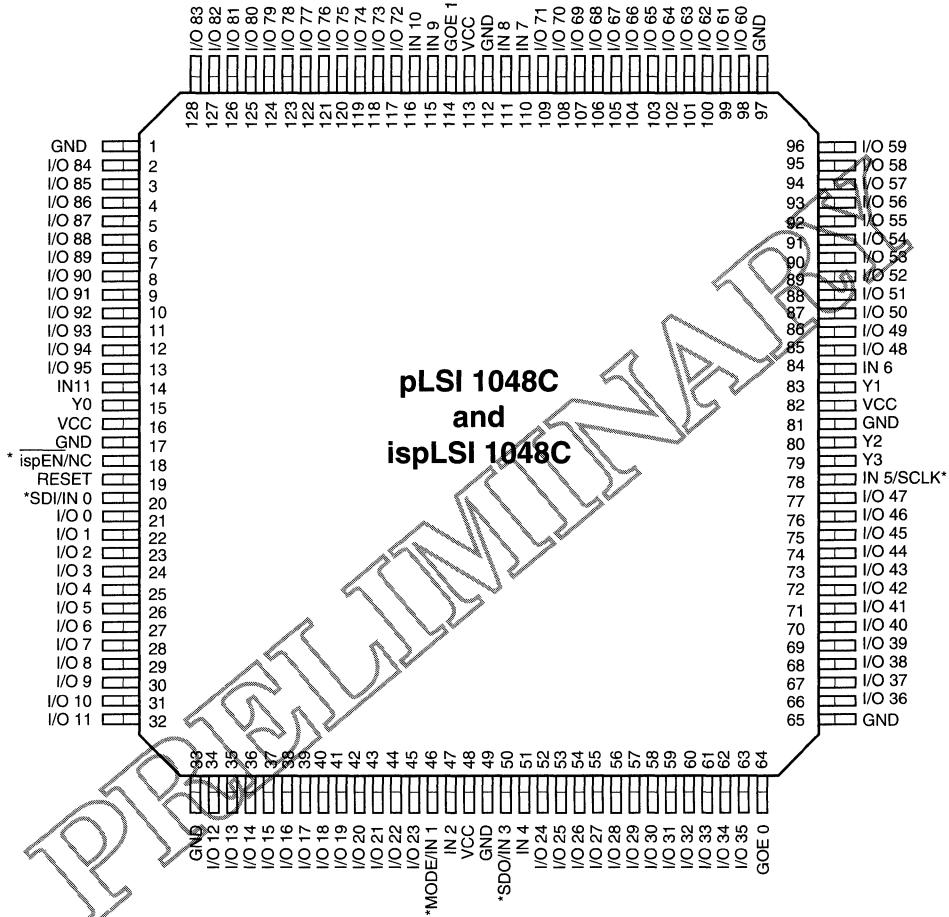
Name	PQFP Pin Numbers	Description
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 22, 23, 24, 25, 26 27, 28, 29, 30, 31, 32 34, 35, 36, 37, 38, 39 40, 41, 42, 43, 44, 45 52, 53, 54, 55, 56, 57 58, 59, 60, 61, 62, 63 66, 67, 68, 69, 70, 71 72, 73, 74, 75, 76, 77 85, 86, 87, 88, 89, 90 91, 92, 93, 94, 95, 96 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 117, 118, 119, 120, 121, 122 123, 124, 125, 126, 127, 128, 2, 3, 4, 5, 6, 7 8, 9, 10, 11, 12, 13	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	64, 114	Global output enables for all I/Os.
IN 2, IN 4 IN 6 - IN 11	47, 51 84, 110, 111, 115, 116, 14	Dedicated input pins to the device.
ispEN*	18	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	20	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	46	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 3	50	Input/Output – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 5	78	Input – This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
RESET	19	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	15	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	83	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	80	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	79	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1, 17, 33, 49, 65, 81, 97, 112	Ground (GND)
V _{CC}	16, 48, 82, 113	V _{CC}

*For ispLSI 1048C Only

Table 2- 0002C-48C

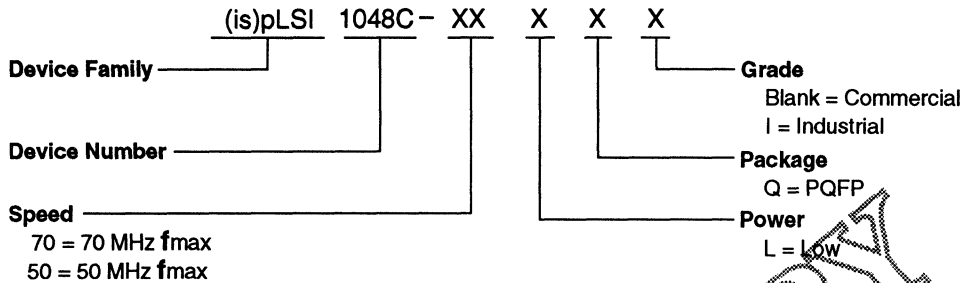
Pin Configuration

pLSI and ispLSI 1048C 128-Pin PQFP Pinout Diagram



*Pins have dual function capability for ispLSI 1048C only (except pin 18, which is ispEN only).

Part Number Description



1048C-50L-isp1048C

pLSI and ispLSI 1048C Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	70	18	pLSI 1048C-70LQ	128-Pin PQFP
	50	24	pLSI 1048C-50LQ	128-Pin PQFP
ispLSI	70	18	ispLSI 1048C-70LQ	128-Pin PQFP
	50	24	ispLSI 1048C-50LQ	128-Pin PQFP

INDUSTRIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	50	24	pLSI 1048C-50LQI	128-Pin PQFP
ispLSI	50	24	ispLSI 1048C-50LQI	128-Pin PQFP

Table 2: 0041A-48C-isp

Introduction to pLSI[®] and ispLSI[™] 2000 Family

Introduction to pLSI and ispLSI 2000 Family

Lattice Semiconductor's pLSI (programmable Large Scale Integration) and ispLSI (in-system programmable Large Scale Integration) are high-density and high-performance E²CMOS[®] programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The Lattice pLSI and ispLSI 2000 Families are I/O intensive, programmable logic devices that combine high performance and ease of use of PLDs with the density and flexibility of FPGAs.

The pLSI and ispLSI 2000 families are ideal for designs needing high performance in conjunction with high I/O requirements.

The ispLSI devices have also pioneered non-volatile, in-system programmability, a technology that allows real-time programming, less expensive manufacturing and end-user feature reconfiguration.

Lattice's E²CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from Lattice and third-party vendors. Development tools offered range from Lattice's low cost pDS[®] software, featuring Boolean entry in a graphical Windows[™] based environment, to the pDS+[™] family of fitters that interfaces with third party development software packages. Design systems interfacing with pDS+ Fitters feature schematic capture, state machine and HDL design entry. Designs can now be completed in hours as opposed to days or weeks.

pLSI and ispLSI Product 2000 Family

- 135 MHz System Performance
- 7.5 ns Pin-to-Pin Delay
- Deterministic Performance
- High Density (1,000-4,000 PLD Gates)
- 44 Pin to 128 Pin Package Options
- Flexible Architecture
- Easy-to-Use
- In-System Programmable (ispLSI)
- Ideal for I/O Intensive Designs

pLSI and ispLSI Technology

- UltraMOS E²CMOS — the PLD Technology of Choice
- Electrically Erasable/Programmable/Reprogrammable
- 100% Tested During Manufacture
- 100% Programming Yield
- Fast Programming

pLSI and ispLSI Development Tools

- Low Cost, Fully Integrated pDS Design System for the PC
- Boolean Equations and Macro Input
- HDL and Schematic Capture Entry
- pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- Timing and Functional Simulation
- PC and Workstation Platforms

Introduction to pLSI and ispLSI 2000 Family

2000 Family Overview

The pLSI and ispLSI 2000 families of high-density devices address high-performance system logic needs, implementing logic functions ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD density ranging from 1,000 to 4,000 gates, the pLSI and ispLSI 2000 Families provide a wide range of programmable logic solutions which meet tomorrow's design requirements today.

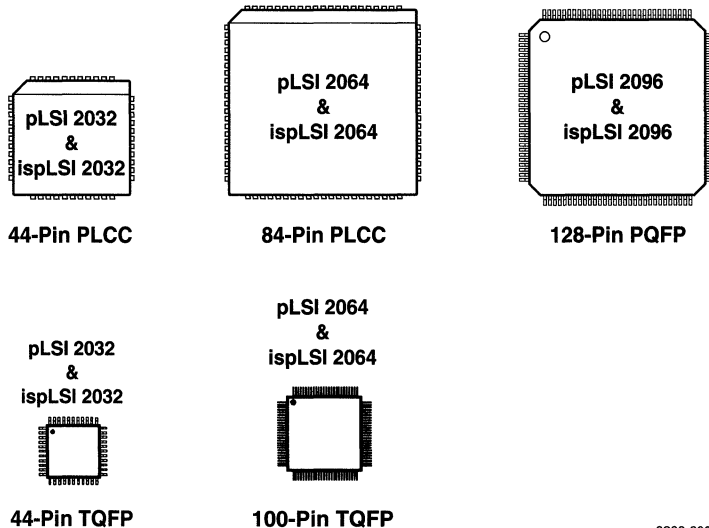
Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

Table 1. pLSI and ispLSI 2000 Family Attributes

Family Member	2032	2064	2096
Density (PLD Gates)	1,000	2,000	4,000
Speed: f_{max} (MHz)	135	135	110
Speed: t_{pd} (ns)	7.5	7.5	10
Macrocells	32	64	96
Registers	32	64	96
Inputs + I/O	34	68	102
Pin/Package	44-pin PLCC 44-pin TQFP	84-pin PLCC 100-pin TQFP	128-pin PQFP

Tab 1-0003A-2000

Figure 1. 2000 Family Packages

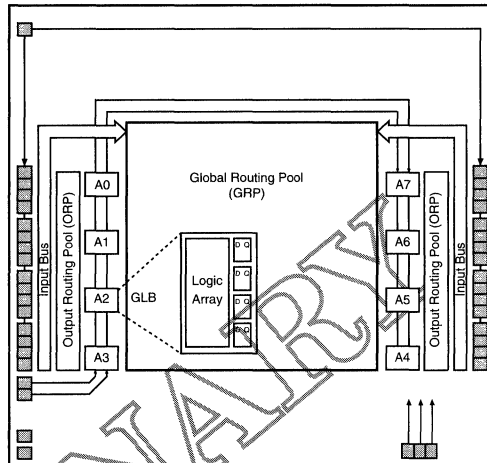


0288-2000

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
 - High Speed Global Interconnect
 - 1000 PLD Gates
 - 32 I/O Pins, Two Dedicated Inputs
 - 32 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - $f_{max} = 135$ MHz Maximum Operating Frequency
 - $t_{pd} = 7.5$ ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile
 - 100% Tested at Time of Manufacture
 - Unused Product Term Shutdown Saves Power
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System Programmable 5-Volt Only
 - Change Logic and Interconnects "On-the-Fly" in Seconds
 - Reprogram Soldered Devices for Debugging
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Three Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS®)**
 - pDS Software**
 - Easy to Use PC Windows™ Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+™ Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning and Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



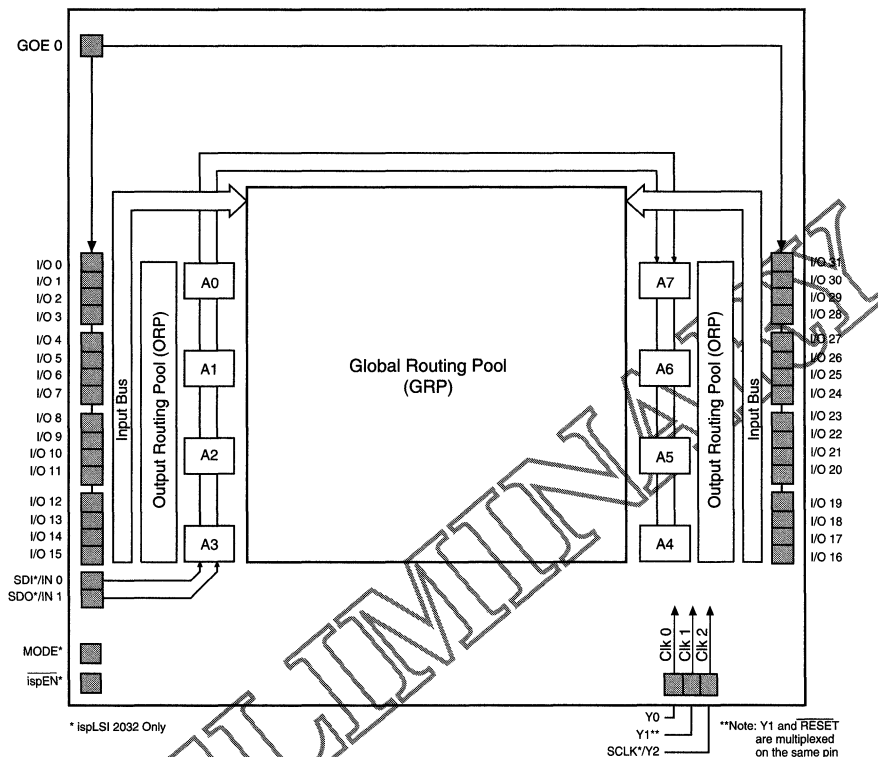
Description

The Lattice pLSI and ispLSI 2032 are High Density Programmable Logic Devices. The devices contain 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2032 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2032 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the pLSI and ispLSI 2032 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see figure 1). There are a total of eight GLBs in the pLSI and ispLSI 2032 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

Functional Block Diagram

Figure 1. pLSI and ispLSI 2032 Functional Block Diagram



The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each pLSI and ispLSI 2032 devices contain one Megablock.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the pLSI and ispLSI 2032 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings ¹

- Supply Voltage V_{CC} -0.5 to +7.0V
- Input Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
- Storage Temperature -65 to 125°C
- Ambient Temp. with Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V

Capacitance ($T_A=25^\circ\text{C}, f=1.0\text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	$V_{CC}=5.0V, V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V, V_{IO}, V_Y=2.0V$

1. Guaranteed but not 100% tested

Table 2-0006A

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
ispLSI Erase/Reprogram Cycles	1000	–	CYCLES
pLSI Erase/Reprogram Cycles	100	–	CYCLES

Table 2-0008A-2032-isp

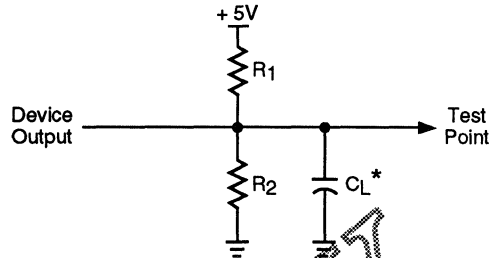
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



*CL includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition	R1	R2	CL
A	470Ω	390Ω	35pF
B	Active High	∞	390Ω
	Active Low	470Ω	390Ω
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω

Table 2- 0004

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
VOL	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	—	—	0.4	V
VOH	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	—	—	V
IIL	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	—	—	-10	μA
IIH	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
IIL-isp	isp/EN Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$	—	—	-150	μA
IIL-PU	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	—	—	-150	μA
IOS1	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	-60	—	-200	mA
ICC2	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$ $f_{TOGGLE} = 1 \text{ MHz}$	—	40	—	mA

- One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- Measured using two 16-bit counters.
- Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Table 2- 0007isp/2032

Over Recommended Operating Conditions

PARAMETER	TEST ⁵ COND.	# ²	DESCRIPTION ¹	-135		-110		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	-	7.5	-	10.0	-	15.0	ns
t _{pd2}	A	2	Data Propagation Delay	-	10.0	-	13.3	-	20.0	ns
f _{max}	A	3	Clock Frequency with Internal Feedback ³	137	-	110.7	-	80	-	MHz
f _{max} (Ext.)	-	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	100	-	79.2	-	50	-	MHz
f _{max} (Tog.)	-	5	Clock Frequency, Max Toggle ⁴	167	-	125	-	100	-	MHz
t _{su1}	-	6	GLB Reg. Setup Time before Clock, 4PT bypass	4	-	5.3	-	-	-	ns
t _{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	-	4.5	-	5.3	-	10.0	ns
t _{h1}	-	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	-	0	-	0	-	ns
t _{su2}	-	9	GLB Reg. Setup Time before Clock	5.5	-	7.4	-	10.0	-	ns
t _{co2}	-	10	GLB Reg. Clock to Output Delay	-	5.5	-	6.8	-	12.0	ns
t _{h2}	-	11	GLB Reg. Hold Time after Clock	0	-	0	-	0	-	ns
t _{r1}	A	12	Ext. Reset Pin to Output Delay	-	10.0	-	13.3	-	17.0	ns
t _{rw1}	-	13	Ext. Reset Pulse Duration	5.0	-	10.0	-	10.0	-	ns
t _{ptoen}	B	14	Input to Output Enable	-	12.0	-	14.5	-	18.0	ns
t _{ptoedis}	C	15	Input to Output Disable	-	12.0	-	14.5	-	18.0	ns
t _{goeen}	B	16	Global OE to Output Enable	-	6.0	-	6.7	-	9.5	ns
t _{goedis}	C	17	Global OE to Output Disable	-	6.0	-	6.7	-	9.5	ns
t _{wh}	-	18	External Synchronous Clock Pulse Duration, High	3.0	-	4.0	-	5.0	-	ns
t _{wl}	-	19	External Synchronous Clock Pulse Duration, Low	3.0	-	4.0	-	5.0	-	ns

1. Unless noted otherwise, all parameters use 20 P_{TXOR} path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using ORP feedback.
4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Table 2 - 0030A/2032-135

2

PROBATION

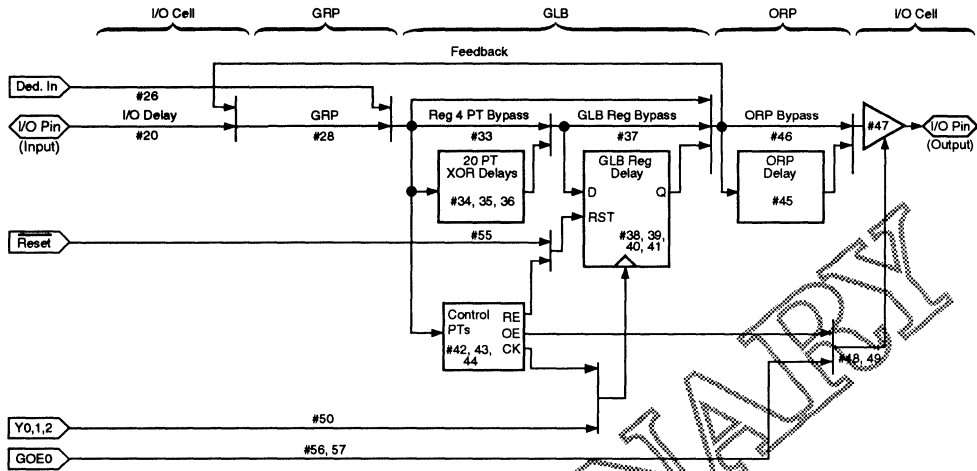
Internal Timing Parameters¹
Over Recommended Operating Conditions

PARAMETER	# ²	DESCRIPTION	-135		-110		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t _{iobp}	20	I/O Register Bypass	-	1.0	-	1.3	-	2.0	ns
t _{din}	26	Dedicated Input Delay	-	2.6	-	3.5	-	4.0	ns
GRP									
t _{grp}	28	GRP Delay	-	1.3	-	1.7	-	2.0	ns
GLB									
t _{4ptbp}	33	4 Product Term Bypass Path Delay	-	3.2	-	4.3	-	6.5	ns
t _{1ptxor}	34	1 Product Term/XOR Path Delay	-	4.0	-	5.3	-	7.0	ns
t _{20ptxor}	35	20 Product Term/XOR Path Delay	-	4.7	-	6.2	-	8.0	ns
t _{xoradj}	36	XOR Adjacent Path Delay ³	-	6.4	-	7.2	-	9.5	ns
t _{gbp}	37	GLB Register Bypass Delay	-	0.5	-	0.7	-	1.0	ns
t _{gsu}	38	GLB Register Setup Time before Clock	0.8	-	1.1	-	1.0	-	ns
t _{gh}	39	GLB Register Hold Time after Clock	3.0	-	4.5	-	4.5	-	ns
t _{gco}	40	GLB Register Clock to Output Delay	-	0.7	-	0.2	-	2.0	ns
t _{gr}	41	GLB Register Reset to Output Delay	-	1.1	-	1.5	-	2.5	ns
t _{ptre}	42	GLB Product Term Reset to Register Delay	-	4.4	-	5.9	-	10.0	ns
t _{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	-	6.5	-	7.2	-	9.0	ns
t _{ptck}	44	GLB Product Term Clock Delay	3.3	3.3	4.4	4.4	3.5	3.5	ns
ORP									
t _{orp}	45	ORP Delay	-	1.3	-	1.7	-	2.5	ns
t _{orpbp}	46	ORP Bypass Delay	-	0.3	-	0.4	-	0.5	ns
Outputs									
t _{ob}	47	Output Buffer Delay	-	1.2	-	1.6	-	3.0	ns
t _{oen}	48	I/O Cell OE to Output Enabled	-	2.2	-	4.3	-	5.0	ns
t _{odis}	49	I/O Cell OE to Output Disabled	-	2.2	-	4.3	-	5.0	ns
Clocks									
t _{gy0/172}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.3	2.3	3.1	3.1	4.5	4.5	ns
Global Reset									
t _{gr}	55	Global Reset to GLB	-	6.4	-	8.5	-	9.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Table 2- 0036A-16/135/110

pLSI and ispLSI 2032 Timing Model



*Note: Y1 and Y2 only for pLSI and ispLSI 1016

04910202

Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

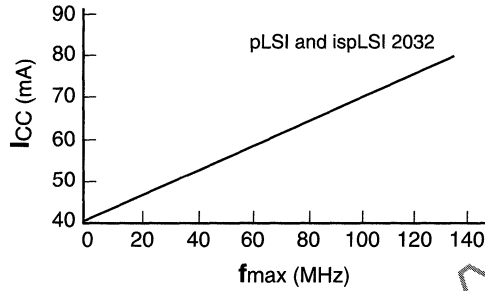
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg}_{su} - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp} + t_{ptck(min)}) \\
 &= (\#24 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 2.2 \text{ ns} &= (1.0 + 1.3 + 4.7) + (0.8) - (1.0 + 1.3 + 3.3) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 4.6 \text{ ns} &= (1.0 + 1.3 + 3.3) + (3.0) - (1.0 + 1.3 + 4.7) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{iobp} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 8.8 \text{ ns} &= (1.0 + 1.3 + 3.3) + (0.7) + (1.3 + 1.2)
 \end{aligned}$$

Note: Calculations are based upon timing specifications for the pLSI and ispLSI 2032-135L.

Power Consumption

Power Consumption in the pLSI and ispLSI 2032 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Two 16-bit Counters
Typical Current at 5V, 25° C

ICC can be estimated for the pLSI and ispLSI 2032 using the following equation:

$$I_{CC} = 23 + (\# \text{ of PTs} * 0.33) + (\# \text{ of nets} * \text{Max freq} * 0.011) \text{ where:}$$

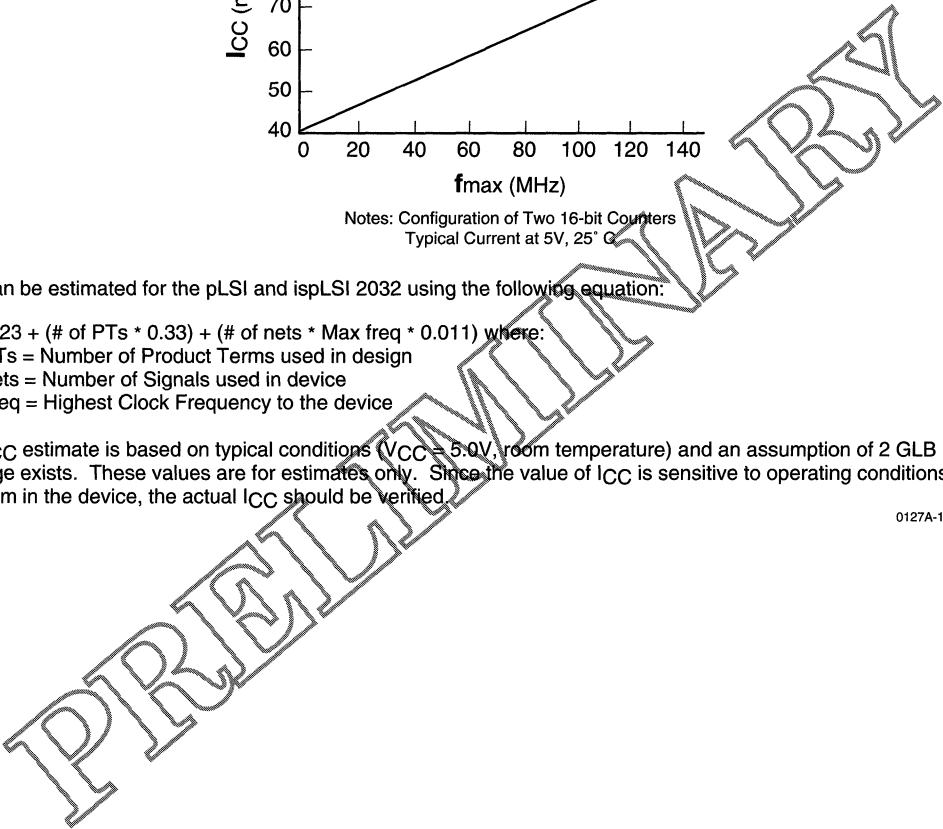
of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Max freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A-16-80-isp/2000

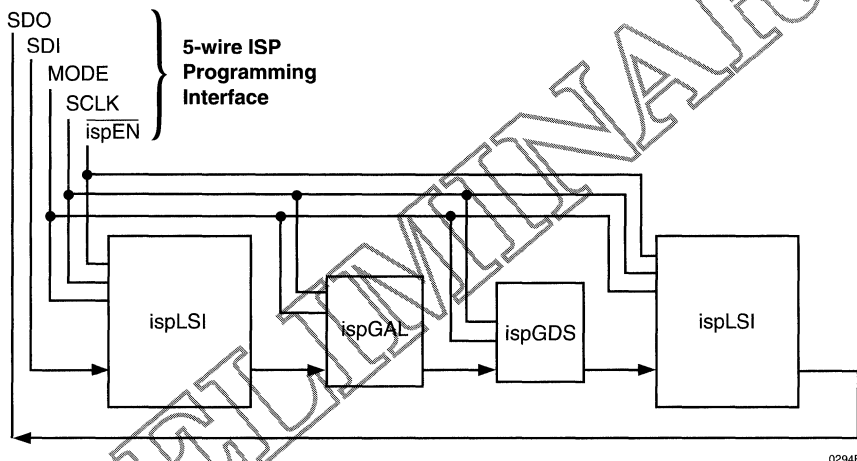


In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this Data Book.

Figure 4. ISP Programming Interface



ISP Programming Voltage/Timing Specifications¹

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCP}	Programming Voltage		4.75	5	5.25	V
I _{CCP}	Programming Supply Current		–	50	100	mA
V _{IHP}	Input Voltage High	ispEN = Low	2.0	–	V _{CCP}	V
V _{ILP}	Input Voltage Low		0	–	0.8	V
I _{IP}	Input Current		–	100	200	μA
V _{OHP}	Output Voltage High	I _{OH} = -3.2 mA	2.4	–	V _{CCP}	V
V _{OLP}	Output Voltage Low	I _{OL} = 5 mA	0	–	0.5	V
t _r , t _f	Input Rise and Fall		–	–	1	μs
t _{ispen}	ispEN to Output 3-State Enabled		–	2	10	μs
t _{ispdis}	ispEN to Output 3-State Disabled		–	2	10	μs
t _{su}	Setup Time		0.1	0.5	–	μs
t _{co}	Clock to Output		0.1	0.5	–	μs
t _h	Hold Time		0.1	0.5	–	μs
t _{clkh} , t _{ckl}	Clock Pulse Width, High and Low		0.5	1	–	μs
t _{pw}	Verify Pulse Width		20	30	–	μs
t _{pwp}	Programming Pulse Width		40	–	100	ms
t _{bew}	Bulk Erase Pulse Width		200	–	–	ms
t _{rst}	Reset Time From Valid V _{CCP}		45	–	–	μs

 1. ISP Programming is guaranteed for T_A = 0°C to 70°C operation only

Table 2-0029 isp-C

PRELIMINARY

Figure 5. Timing Waveform for In-System Programming

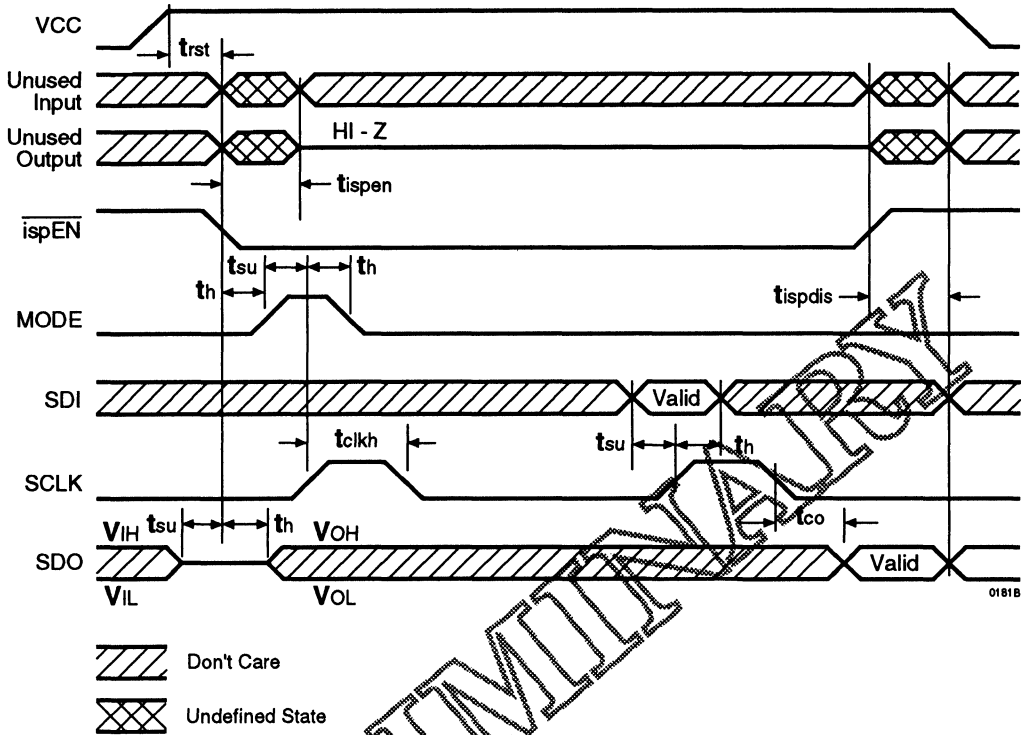


Figure 6. Program, Verify & Bulk Erase Waveform

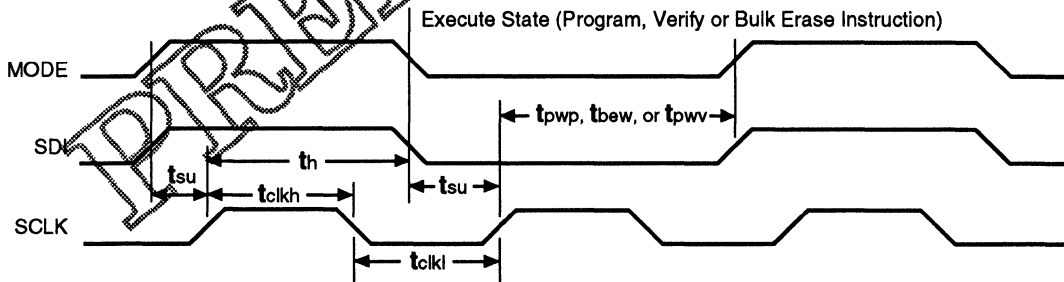
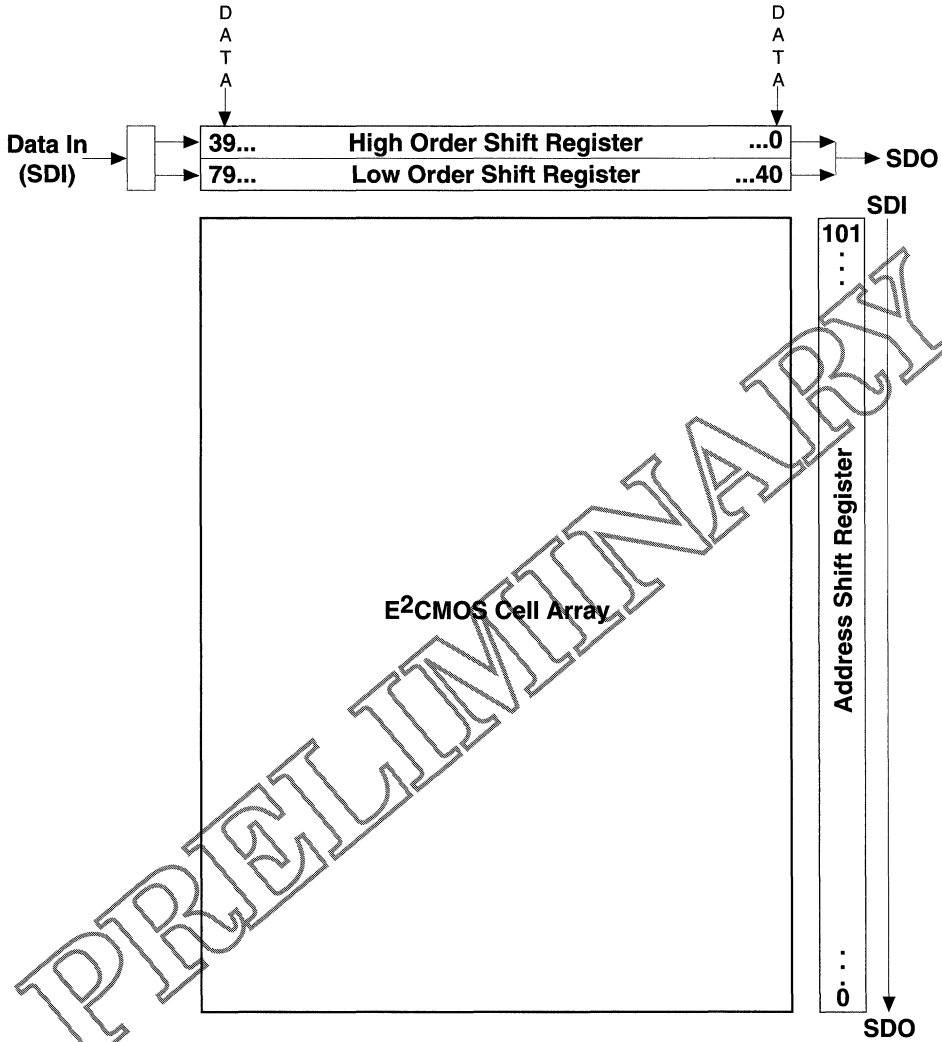


Figure 7. ispLSI 2032 Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	2	Global Output Enable input pin.
Y0 Y1/ $\overline{\text{RESET}}$	11 35	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device. This pin performs two functions: 1. Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device. 2. Active Low (0) Reset pin which resets all the registers in the device.
$\overline{\text{ispEN}}^*/\text{NC}$ MODE*/NC SDI*/INO SDO*/IN1 SCLK*/Y2	13 36 14 24 33	Input - Dedicated in-system programming enable pin. this pin is brought low to enable the programming mode. When low, the MODE, SDI and SDO controls become active. Input - When in ISP mode, controls operation of ISP state-machine. This pin has two functions: 1. Dedicated input pin when not in ISP mode. 2. Serial data input when in ISP mode. This pin performs two functions: 1. Dedicated input pin when not in ISP mode. 2. Serial data output when in isp mode. This pin performs two functions: 1. Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device. 2. Input - When in ISP mode, functions as a clock pin for the Serial Shift Register.
GND VCC	1, 23 12, 34	Ground (GND) V _{cc}

* ispLSI 2032 Only

Table 2- 0002A-08isp/2000

Pin Description

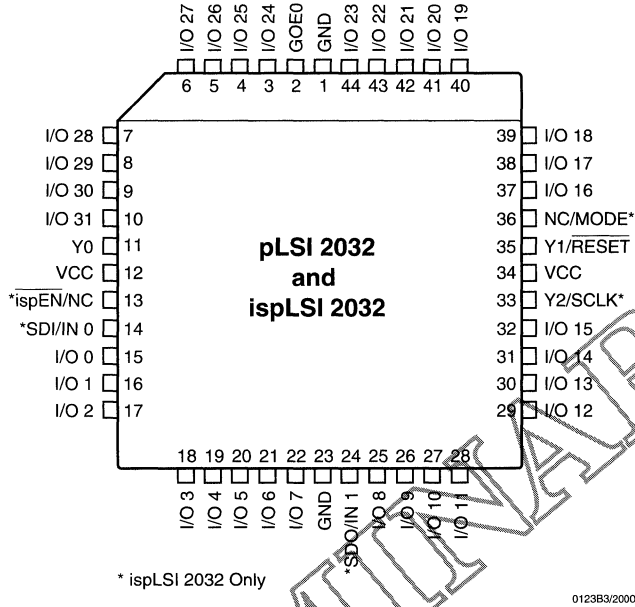
Name	TQFP Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	40	Global Output Enable Input Pin.
$\overline{\text{ispEN}}^*/\text{NC}$	7	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	8	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/NC	30	Input – When in ISP mode, controls operation of ISP state-machine.
SDO*/IN 1	18	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/Y2	27	Input – This pin performs two functions. It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
Y0 Y1/ $\overline{\text{RESET}}$	5 29	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device. This pin performs two functions: <ul style="list-style-type: none"> – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
GND V _{CC}	17, 39 6, 28	Ground (GND) V _{CC}

* For ispLSI 2032 Only

Table 2 - 0002B-2032

Pin Configuration

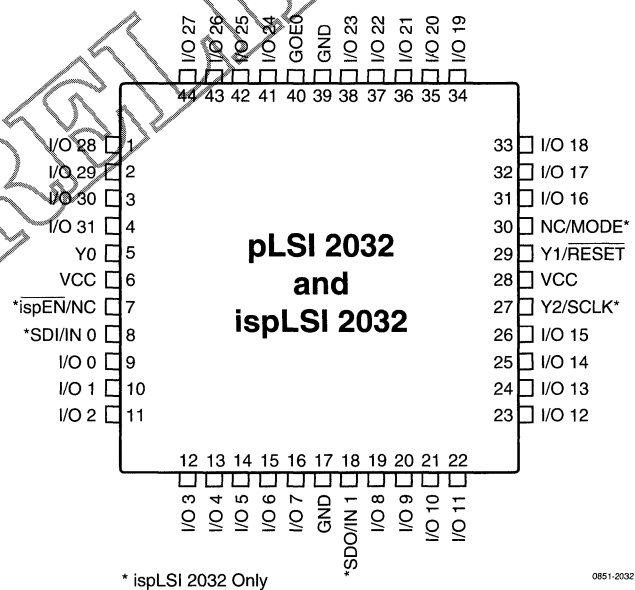
pLSI and ispLSI 2032 44-pin PLCC



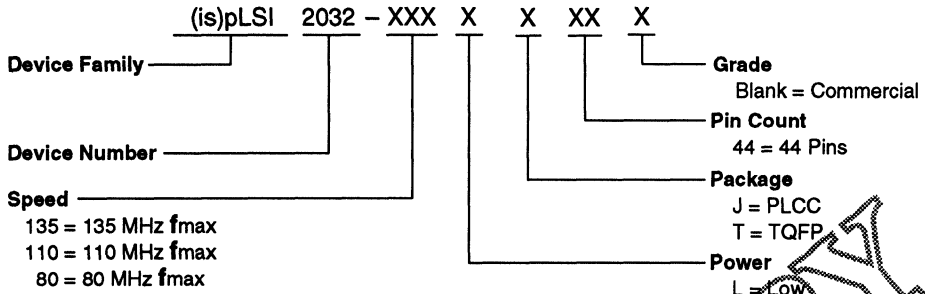
2

Pin Configuration

pLSI and ispLSI 2032 44-pin TQFP



Part Number Description



pLSI and ispLSI 2032 Ordering Information

COMMERCIAL

Device Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	135	7.5	pLSI 2032-135LJ44	44-Pin PLCC
	135	7.5	pLSI 2032-135LT44	44-Pin TQFP
	110	10	pLSI 2032-110LJ44	44-Pin PLCC
	110	10	pLSI 2032-110LT44	44-Pin TQFP
	80	15	pLSI 2032-80LJ44	44-Pin PLCC
	80	15	pLSI 2032-80LT44	44-Pin TQFP
ispLSI	135	7.5	ispLSI 2032-135LJ44	44-Pin PLCC
	135	7.5	ispLSI 2032-135LT44	44-Pin TQFP
	110	10	ispLSI 2032-110LJ44	44-Pin PLCC
	110	10	ispLSI 2032-110LT44	44-Pin TQFP
	80	15	ispLSI 2032-80LJ44	44-Pin PLCC
	80	15	ispLSI 2032-80LT44	44-Pin TQFP

Table 2- 0041A-08isp/2000

Introduction to pLSI[®] and ispLSI[™] 3000 Family

Introduction to pLSI and ispLSI 3000 Family

Lattice Semiconductor's pLSI (programmable Large Scale Integration) and ispLSI (in-system programmable Large Scale Integration) are high-density and high-performance E²CMOS[®] programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The Lattice pLSI and ispLSI 3000 Families are the third generation to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs.

The pLSI and ispLSI 3000 Family is ideal for high density designs, where integration of complete logic sub-systems into a single device is necessary.

The ispLSI devices have also pioneered non-volatile, in-system programmability, a technology that allows real-time programming, less expensive manufacturing and end-user feature reconfiguration.

Lattice's E²CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from Lattice and third-party vendors. Development tools offered range from Lattice's low cost pDS[®] software, featuring Boolean entry in a graphical Windows[™] based environment, to the pDS+[™] family of Fitters that interface with third party development software packages. pDS+ systems support schematic capture, state machine, Boolean, and HDL Design entry. Designs can now be completed in hours as opposed to days or weeks.

pLSI and ispLSI Product 3000 Family

- 110 MHz System Performance
- 10 ns Pin-to-Pin Delay
- Deterministic Performance
- High Density (8000 - 14,000 PLD Gates)
- Flexible Easy-to-Use Architecture
- In-System Programmable (ispLSI)
- Boundary Scan (IEEE 1149.1)

pLSI and ispLSI Technology

- UltraMOS E²CMOS — the PLD Technology of Choice
- Electrically Erasable/Programmable/Reprogrammable
- 100% Tested During Manufacture
- 100% Programming Yield
- Fast Programming

pLSI and ispLSI Development Tools

- Low Cost, Fully Integrated pDS Design System for the PC
- HDL Boolean Equation and Schematic Capture Entry
- pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- Timing and Functional Simulation
- PC and Workstation Platforms

Introduction to pLSI and ispLSI 3000 Family

3000 Family Overview

The pLSI and ispLSI 3000 family of high-density devices address high-performance system logic designs implementing logic functions, ranging from registers, to counters, to multiplexers, to complex state machines.

With up to 14,000 PLD gates density, the pLSI and ispLSI 3000 Family provides a wide range of programmable logic solutions which meet tomorrow's design requirements today.

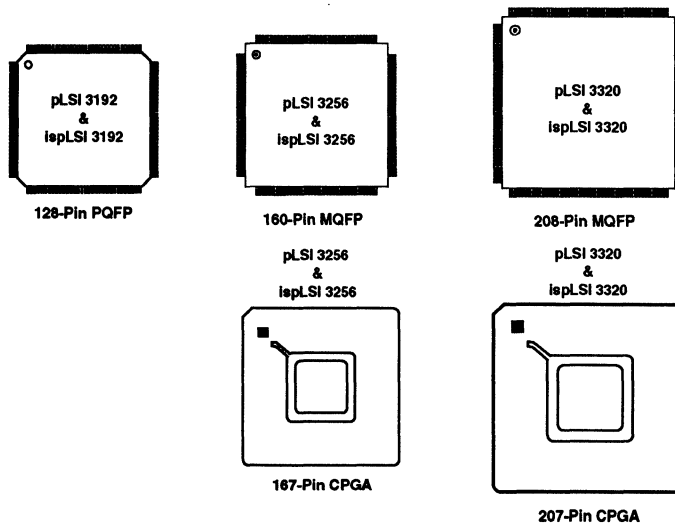
Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

Table 1. pLSI and ispLSI 3000 Family Attributes

Family Member	3192	3256	3320
Density (PLD Gates)	8,000	11,000	14,000
Speed: f_{max} (MHz)	110	80	80
Speed: t_{pd} (ns)	10	15	15
Macrocells	192	256	320
Registers	288	384	480
Inputs + I/O	96	128	160
Pin/Package	128-pin PQFP	160-pin MQFP 167-pin CPGA	208-pin MQFP 207-pin CPGA

Table 1-0003A-3000

Figure 1. 3000 Family Packages

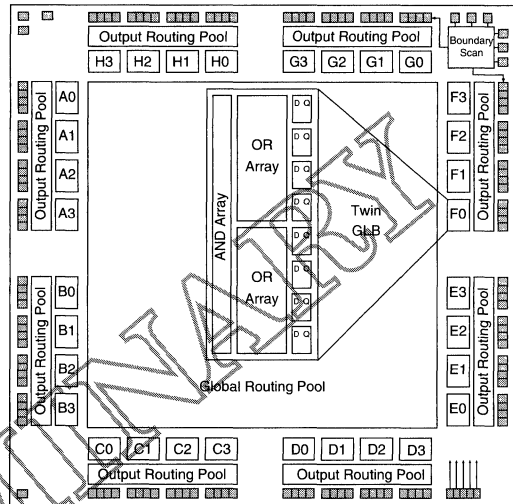


0288-1808-3000

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
 - High Speed Global Interconnect
 - 128 I/O Pins
 - 11000 PLD Gates
 - 384 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²C²MOS[®] TECHNOLOGY**
 - $f_{max} = 80$ MHz Maximum Operating Frequency
 - $t_{pd} = 15$ ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile
 - 100% Tested at Time of Manufacture
 - Unused Product Term Shutdown Saves Power
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System Programmable 5-Volt Only
 - Change Logic and Interconnects "On-the-Fly" in Seconds
 - Reprogram Soldered Devices for Debugging
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device can Combine Glue Logic and Structured Designs
 - Five Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS[®])**
 - pDS Software**
 - Easy to Use PC Windows[™] Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+[™] Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning and Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



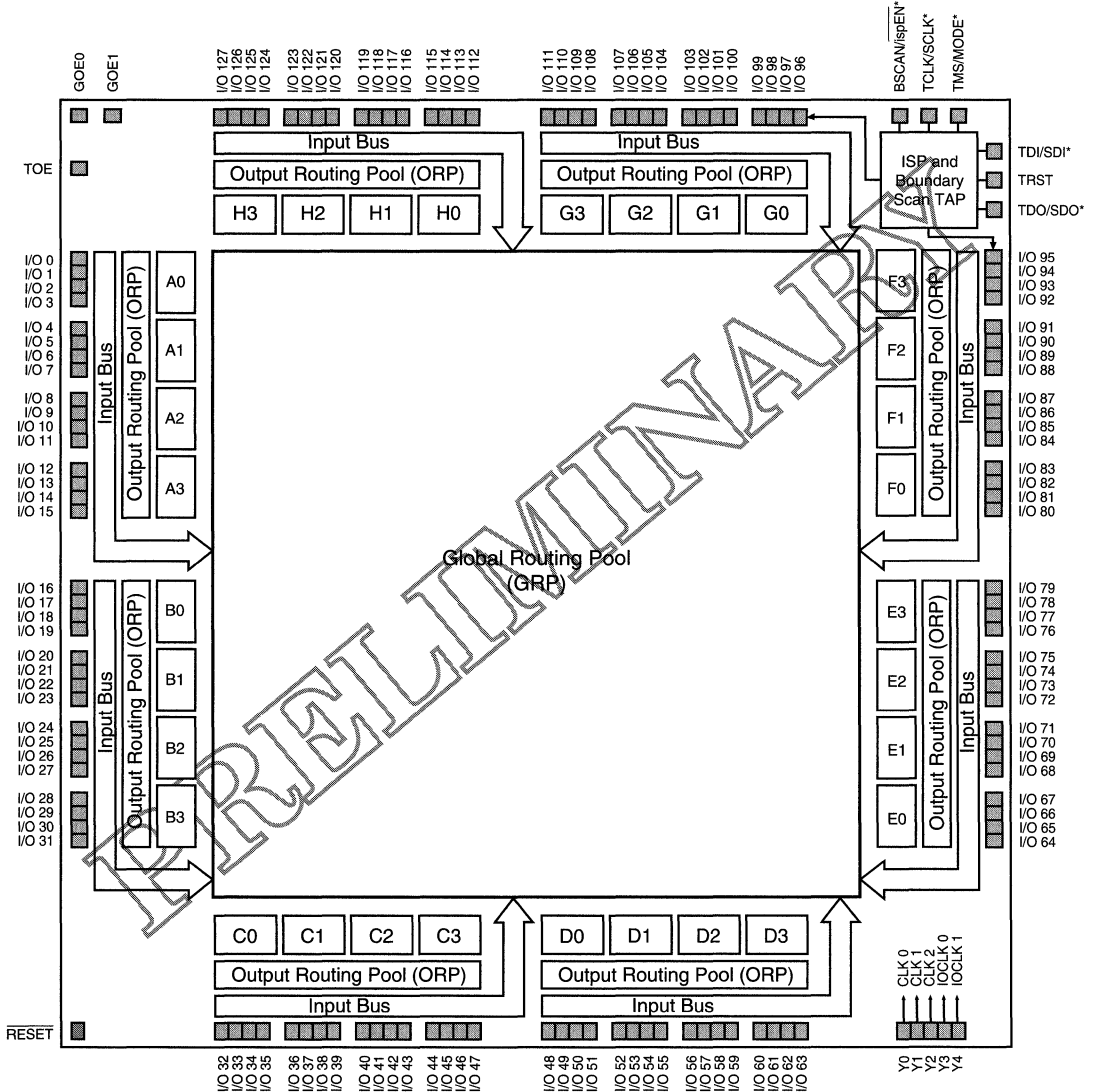
Description

The Lattice pLSI and ispLSI 3256 are High Density Programmable Logic Devices which contain 384 Registers, 128 Universal I/O pins, five Dedicated Clock Input Pins, eight Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3256 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3256 devices, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the pLSI and ispLSI 3256 devices is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3. There are a total of 32 of these Twin GLBs in the pLSI and ispLSI 3256 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

Functional Block Diagram

Figure 1. pLSI and ispLSI 3256 Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 128 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

The 128 I/O Cells are grouped into eight sets of 16 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. These groups of 16 I/O cells share one Product Term Output Enable and two Global Output Enable signals.

Four Twin GLBs, 16 I/O Cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The pLSI and ispLSI 3256 Device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the pLSI and ispLSI 3256 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the pLSI and ispLSI 3256 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The pLSI and ispLSI 3256 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the pLSI and ispLSI 3256

Device	pLSI and ispLSI 3256
Twin GLBs	32
Registers	384
I/O Pins	128
Global OE	2
Test OE	1

Table 1- 0003Aisp/3256

Absolute Maximum Ratings ¹

Supply Voltage V_{CC} -0.5 to +7.0V
 Input Voltage Applied. -2.5 to $V_{CC} + 1.0V$
 Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 125°C
 Ambient Temp. with Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V

Capacitance ($T_A=25^\circ\text{C}, f=1.0\text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	$V_{CC}=5.0V, V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V, V_{IO}, V_T=2.0V$

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
ispLSI Erase/Reprogram Cycles	1000	–	CYCLES
pLSI Erase/Reprogram Cycles	100	–	CYCLES

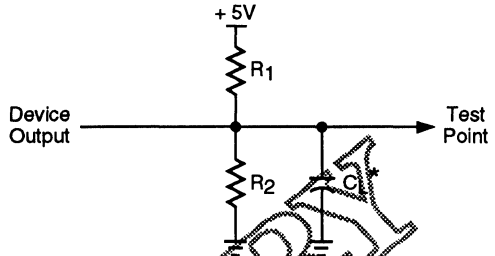
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



*CL includes Test Fixture and Probe Capacitance.

Output Load conditions (figure 2)

Test Condition	R1	R2	CL	
A	470Ω	390Ω	35pF	
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω	5pF
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω	5pF

Table 2- 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	-	-	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	-	-	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	-	-	-10	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	-	-	10	μA
I_{IL-isp}	Bscan/ispEN Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$	-	-	-150	μA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	-	-	-150	μA
I_{OS1}	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	-60	-	-200	mA
I_{CC2}	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$ $f_{TOGGLE} = 1 \text{ MHz}$	-	150	-	mA

- One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- Measured using sixteen 16-bit counters.
- Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Table 2- 0007isp/3256

External Switching Characteristics^{1, 2, 3}

Over Recommended Operating Conditions

PARAMETER	TEST 5 COND.	# ²	DESCRIPTION ¹	-80 ⁶		-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	-	15	-	17	-	23	ns
t _{pd2}	A	2	Data Propagation Delay	-	-	-	-	-	-	ns
f _{max}	A	3	Clock Frequency with Internal Feedback ³	80	-	70	-	50	-	MHz
f _{max} (Ext.)	-	4	Clock Frequency with External Feedback ($\frac{1}{(t_{su2} + t_{co1})}$)	-	-	-	-	-	-	MHz
f _{max} (Tog.)	-	5	Clock Frequency, Max Toggle ⁴	-	-	-	-	-	-	MHz
t _{su1}	-	6	GLB Reg. Setup Time before Clock, 4PT bypass	-	-	-	-	-	-	ns
t _{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	-	-	-	-	-	-	ns
t _{h1}	-	8	GLB Reg. Hold Time after Clock, 4 PT bypass	-	-	-	-	-	-	ns
t _{su2}	-	9	GLB Reg. Setup Time before Clock	-	-	-	-	-	-	ns
t _{co2}	-	10	GLB Reg. Clock to Output Delay	-	-	-	-	-	-	ns
t _{h2}	-	11	GLB Reg. Hold Time after Clock	-	-	-	-	-	-	ns
t _{r1}	A	12	Ext. Reset Pin to Output Delay	-	-	-	-	-	-	ns
t _{rw1}	-	13	Ext. Reset Pulse Duration	-	-	-	-	-	-	ns
t _{ptoen}	B	14	Input to Output Enable	-	-	-	-	-	-	ns
t _{ptoedis}	C	15	Input to Output Disable	-	-	-	-	-	-	ns
t _{goeen}	B	16	Global OE Output Enable	-	-	-	-	-	-	ns
t _{goedis}	C	17	Global OE Output Disable	-	-	-	-	-	-	ns
t _{toeen}	-	18	Test OE Output Enable	-	-	-	-	-	-	ns
t _{toedis}	-	19	Test OE Output Disable	-	-	-	-	-	-	ns
t _{wh}	-	20	Ext. Sync. Clock Pulse Duration, High	-	-	-	-	-	-	ns
t _{wl}	-	21	Ext. Sync. Clock Pulse Duration, Low	-	-	-	-	-	-	ns
t _{su3}	-	22	IO Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	-	-	-	-	-	-	ns
t _{h3}	-	23	IO Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	-	-	-	-	-	-	ns

Table 2 - 0030A/3256

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.
6. Contact factory for additional information.

Internal Timing Parameters¹

Over Recommended Operating Conditions

2

PARAMETER	# ²	DESCRIPTION	-80 ⁴		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t _{iobp}	24	I/O Register Bypass	-		-	2		2.7	ns
t _{iolat}	25	I/O Latch Delay	-		-	3		4.1	ns
t _{iosu}	26	I/O Register Setup Time before Clock		-	9		12.2	-	ns
t _{ioh}	27	I/O Register Hold Time after Clock		-			-1.4	-	ns
t _{ioco}	28	I/O Register Clock to Out Delay	-			2		2.7	ns
t _{ior}	29	I/O Register Reset to Out Delay	-		-	3.6		4.7	ns
GRP									
t _{grp}	31	GRP Delay			-	4		5.4	ns
GLB									
t _{4ptbp}	37	4 Product Term Bypass Path Delay			-	6.5		8.8	ns
t _{1ptxor}	38	1 Product Term/XOR Path Delay	-		-	7		9.5	ns
t _{20ptxor}	39	20 Product Term/XOR Path Delay	-		-	8.5		11.5	ns
t _{xoradj}	40	XOR Adjacent Path Delay ³	-		-	10		13.5	ns
t _{gbp}	41	GLB Register Bypass Delay	-		-	1		1.4	ns
t _{gsu}	42	GLB Register Setup Time before Clock		-	1.5		2		ns
t _{gh}	43	GLB Register Hold Time after Clock		-	9		12.2		ns
t _{gco}	44	GLB Register Clock to Output Delay	-		-	1.5		2	ns
t _{gr}	45	GLB Register Reset to Output Delay	-		-	2.5		3.4	ns
t _{ptre}	46	GLB Product Term Reset to Register Delay	-		-	10		13.5	ns
t _{ptoe}	47	GLB Product Term Output Enable to I/O Cell Delay	-		-	9		12.2	ns
t _{ptck}	48	GLB Product Term Clock Delay			3.5	7.5	4.7	10.1	ns
ORP									
t _{orp}	49	ORP Delay	-		-	2		2.7	ns
t _{orpbp}	50	ORP Bypass Delay	-		-	0.5		0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.
4. Contact factory for additional information.

Table 2- 0036A/3256

Internal Timing Parameters¹

Over Recommended Operating Conditions

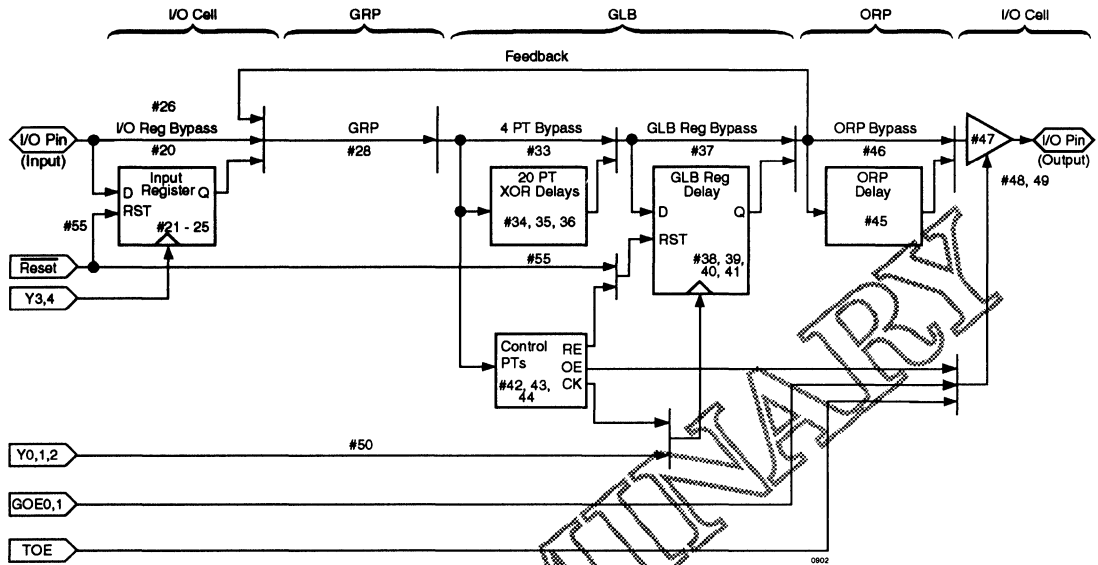
PARAMETER	# ²	DESCRIPTION	-80 ³		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t _{ob}	51	Output Buffer Delay	-	-	-	3	-	4.1	ns
t _{oen}	52	I/O Cell OE to Output Enabled	-	-	-	5	-	6.8	ns
t _{odis}	53	I/O Cell OE to Output Disabled	-	-	-	5	-	6.8	ns
Clocks									
t _{gy0/1/2}	54	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line (Ref. clock)	-	-	3	3	4.1	4.1	ns
t _{ioy3/4}	56	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	-	-	1	1	1.4	1.4	ns
Global Reset									
t _{gr}	57	Global Reset to GLB and I/O Registers	-	-	-	7.5	-	10.1	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. Contact factory for additional information.

Table 2- 0037A/3256

PRELIMINARY

pLSI and ispLSI 3256 Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg} - \text{Clock} (\text{min}) \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck}(\text{min})) \\
 &= (24 + 31 + 89) + (42) - (24 + 31 + 48) \\
 1.5 \text{ ns} &= (2 + 4 + 3.5) + (1.5) - (2 + 4 + 3.5) \\
 t_h &= \text{Clock}(\text{max}) + \text{Reg} - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck}(\text{max})) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (24 + 31 + 48) + (43) - (24 + 31 + 39) \\
 8 \text{ ns} &= (2 + 4 + 7.5) + (9) - (2 + 4 + 8.5) \\
 t_{co} &= \text{Clock}(\text{max}) + \text{Reg} - \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck}(\text{max})) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (24 + 31 + 48) + (44) + (49 + 51) \\
 20 \text{ ns} &= (2 + 4 + 7.5) + (1.5) + (2 + 3)
 \end{aligned}$$

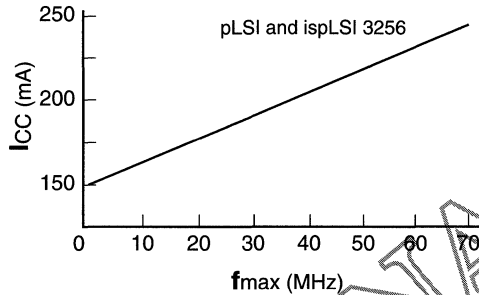
Note: Calculations are based on timing specs for the ispLSI 3256-70L.

Power Consumption

Power Consumption in the pLSI and ispLSI 3256 device depends on two primary factors: the speed at which the device is operating and the number of product terms

used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25°C

I_{CC} can be estimated for the pLSI and ispLSI 3256 using the following equation:

$$I_{CC} = 44 + (\# \text{ of PTs} * 0.18) + (\# \text{ of nets} * \text{Max. freq} * 0.013) \text{ Where:}$$

of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-16-80-isp/3000

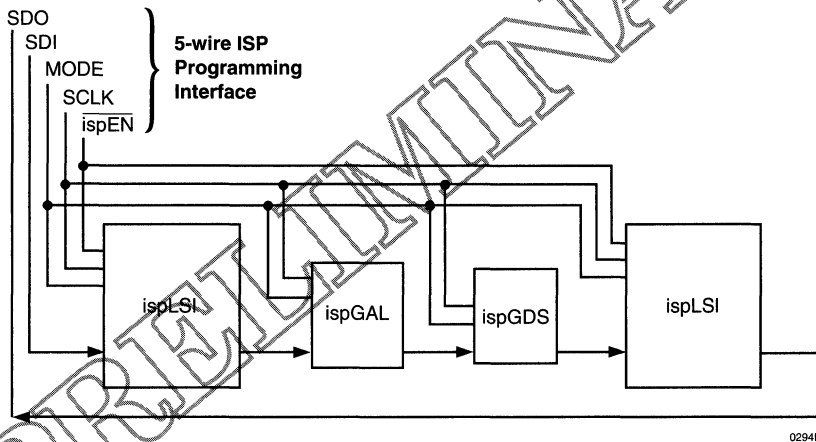
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the in-system programming section in this Data Book.

2

Figure 4. ISP Programming Interface



ISP Programming Voltage/Timing Specifications

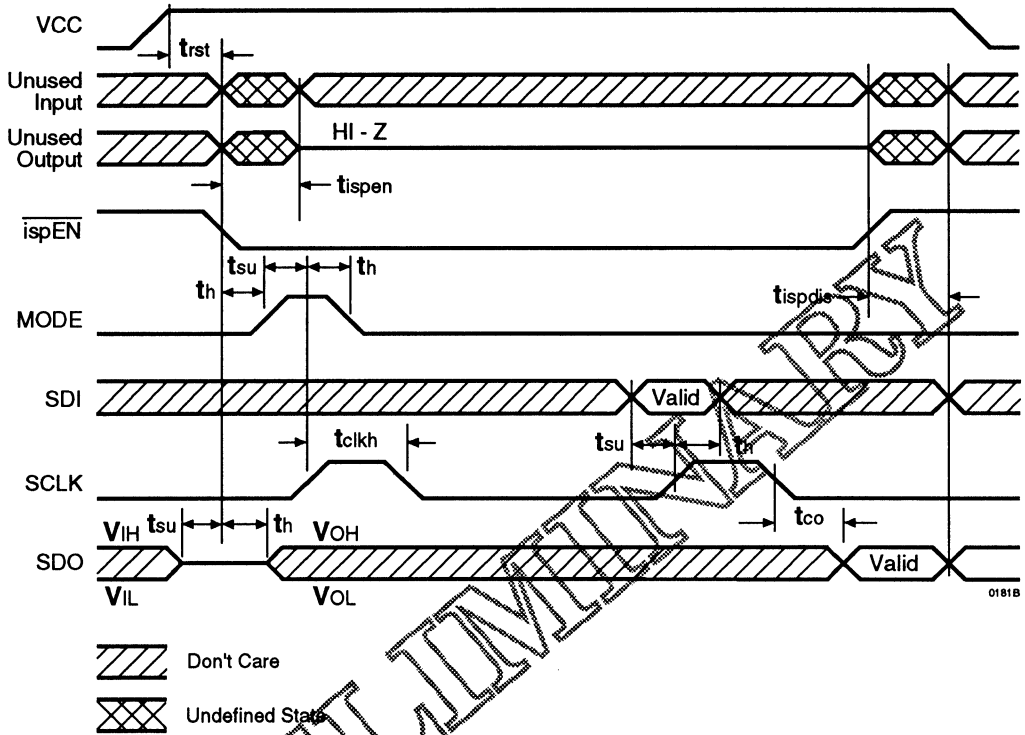
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCP}	Programming Voltage		4.75	5	5.25	V
I _{CCP}	Programming Supply Current		–	50	100	mA
V _{IHP}	Input Voltage High	ispEN = Low	2.0	–	V _{CCP}	V
V _{ILP}	Input Voltage Low		0	–	0.8	V
I _{IP}	Input Current		–	100	200	μA
V _{OHP}	Output Voltage High	I _{OH} = -3.2 mA	2.4	–	V _{CCP}	V
V _{OLP}	Output Voltage Low	I _{OL} = 5 mA	0	–	0.5	V
t _r , t _f	Input Rise and Fall		–	–	0.1	μs
t _{isp_{en}}	ispEN to Output 3-State Enabled		–	2	10	μs
t _{isp_{dis}}	ispEN to Output 3-State Disabled		–	2	10	μs
t _{su}	Setup Time		0.1	0.5	–	μs
t _{co}	Clock to Output		0.1	0.5	–	μs
t _h	Hold Time		0.1	0.5	–	μs
t _{cl_{kh}} , t _{cl_{kl}}	Clock Pulse Width, High and Low		0.5	1	–	μs
t _{pw}	Verify Pulse Width		20	30	–	μs
t _{p_w}	Programming Pulse Width		80	–	160	ms
t _{b_{ew}}	Bulk Erase Pulse Width		200	–	–	ms
t _{rst}	Reset Time From Valid V _{CCP}		45	–	–	μs

1. ISP Programming is guaranteed for T_A = 0°C to 70°C Operation only.

Table 2- 0029 isp-3256

PRELIMINARY

Figure 5. Timing Waveform for ISP Operation



2

Figure 6. Program, Verify & Bulk Erase Waveform

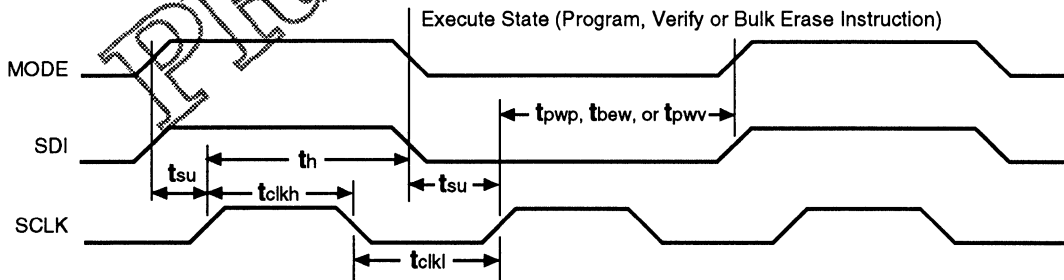
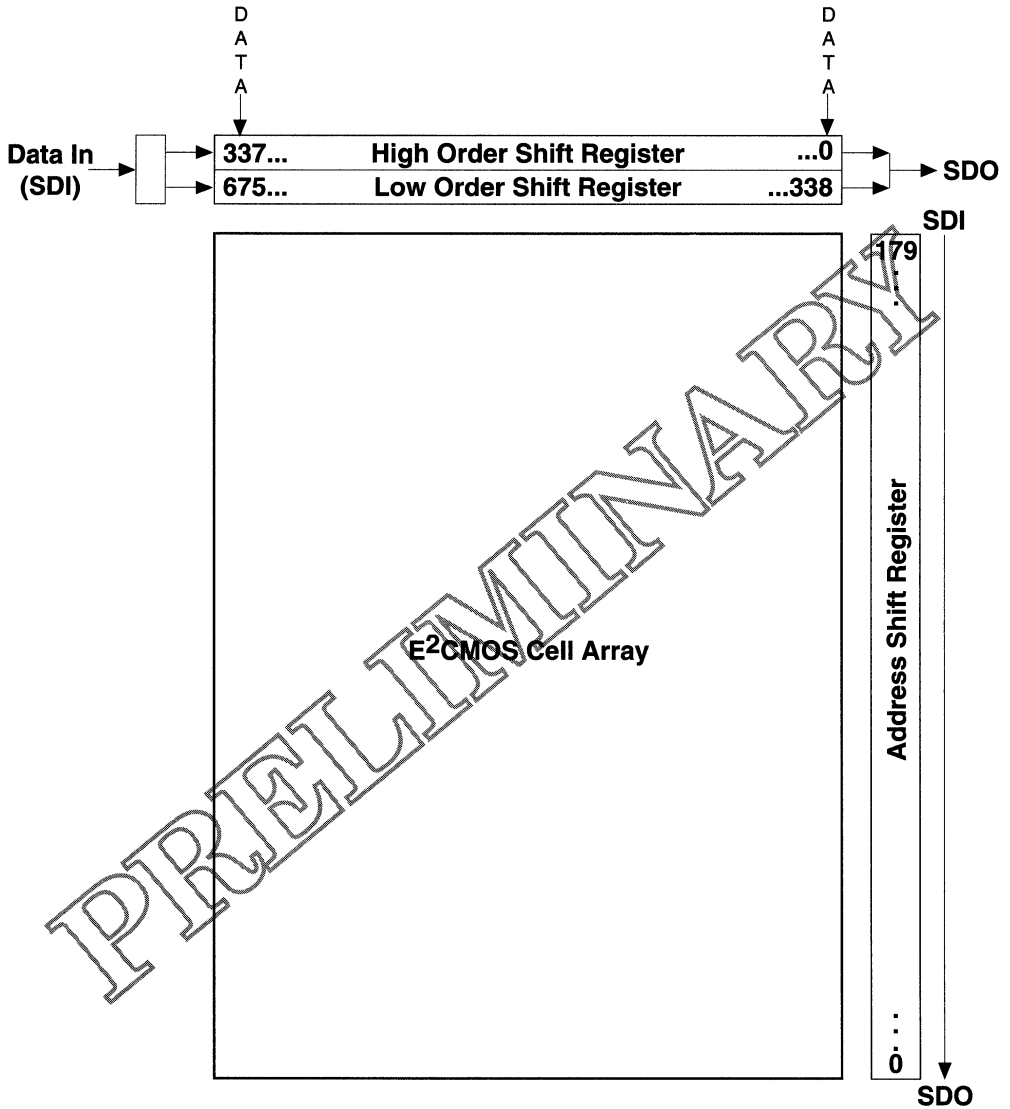


Figure 7. ispLSI 3256 Shift Register Layout



0182A/3256

Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Boundary Scan

Lattice offers support for the IEEE 1149.1 Boundary Scan specification on the 3000 Family of devices.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset (TRST) and Test Clock (TCK).

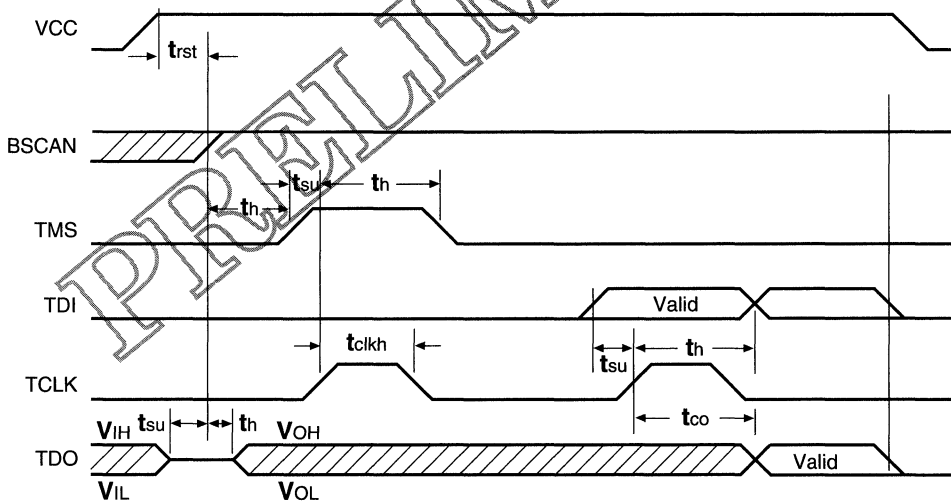
The timing specifications for Boundary Scan are listed below. The waveforms are shown in figure 9.

Boundary Scan Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CC}	Supply Voltage		4.75	5.0	5.25	V
t _{rst}	Reset Time from Valid V _{CC}		45	-	-	μs
t _{su}	Setup Time		0.1	0.5	-	μs
t _h	Hold Time		0.1	0.5	-	μs
t _{co}	Clock to Output		0.1	0.5	-	μs

Table 2 -0028Aisp/3256

Figure 8. Boundary Scan Waveforms



0181A.eps

Pin Description

Name	CPGA Pin Numbers	Description
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	G1, G2, G3, E1, F2, F3, C1, E2, E3, D2, D3, B2, C3, C4, B3, B1, B4, C5, A3, B5, C6, A4, B6, A5, C7, A6, A7, C8, B8, B9, C9, A9, A10, B10, A11, B11, A12, C11, A13, B12, A14, A15, A16, C13, B14, B15, C14, B16, C15, D15, A17, D16, E15, B17, C17, E16, F15, D17, E17, F17, G16, G17, H15, H16, L16, M17, N17, M16, P17, R17, N16, S17, N15, P16, P15, S16, R15, R14, S15, T17, S14, R13, T15, S13, R12, T14, S12, T13, R11, T12, T11, R10, S10, S9, R9, T9, T8, S8, T7, S7, T6, R7, T5, S6, T4, R3, T2, R5, S4, S3, R4, S2, R3, P3, T1, P2, N3, S1, R1, N2, M3, P1, N1, M1, L2, L1, K3, K2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	J17 and J15 J16	Global Output Enable input pins. Test output enable pin.
RESET	J3	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1 and Y2	K1, J2, K15	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3 and Y4	K16, K17	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/ $\overline{\text{ispEN}}^*$	J1	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
TDI/SDI*	H1	Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine.
TCLK/SCLK	H2	Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
TMS/MODE*	H3	Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine.
$\overline{\text{TRST}}$	H17	Input - Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO*	L17	Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND	F1, C2, A2, B7, C10, B13, C16, F16, L15, R16, T16, S11, S5, R8, R2, M2	Ground (GND)
VCC	D1, A8, G15, C12, M15, T10, L3, R6	V _{cc}

* ispLSI 3256 Only

Table 2- 0002isp/3256

Pin Description

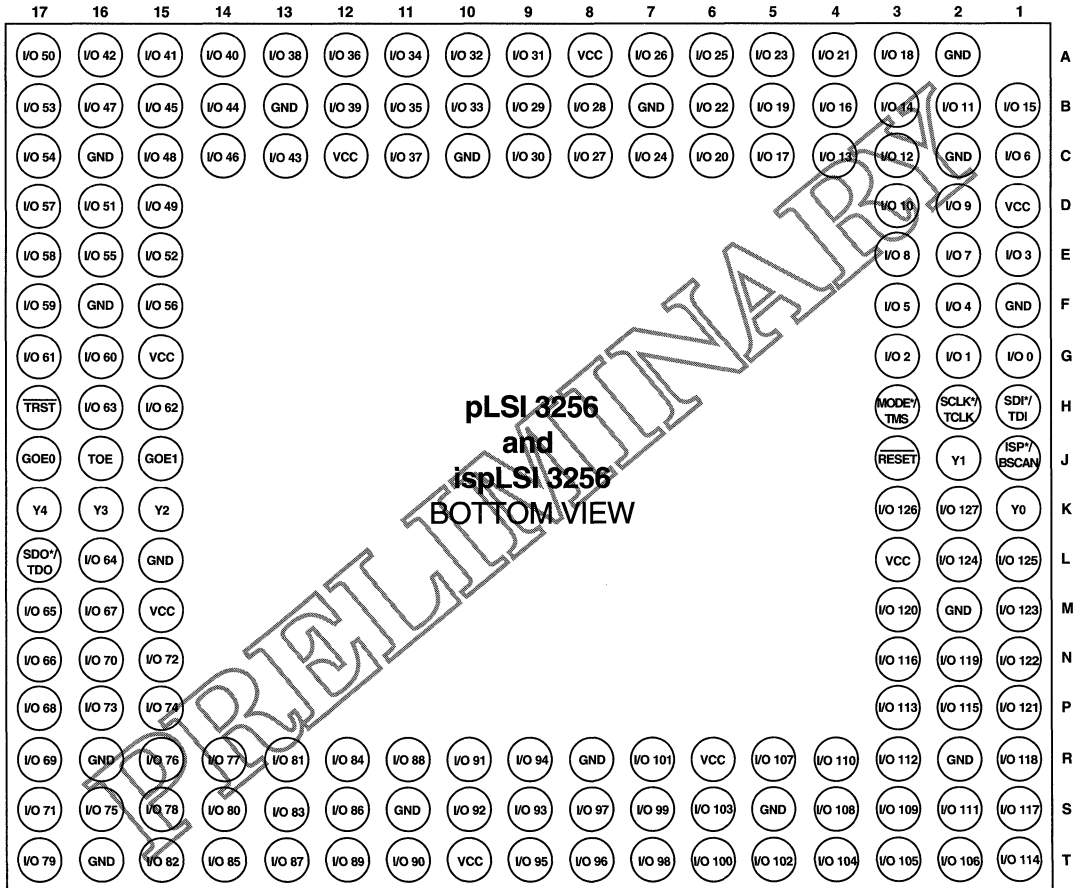
Name	MQUAD Pin Numbers	Description
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	25, 26, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 46, 47, 48, 49, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 70, 72, 73, 74, 75, 76, 77, 78, 79, 80 82, 83, 84, 85, 86, 87, 88, 89, 90, 92, 93, 94, 95, 96, 105, 106, 108, 109, 110, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 126, 127, 128, 129, 130, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 144, 145, 146, 147, 148, 149, 150, 152, 153, 154, 155, 156, 157, 158, 159, 160, 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15, 16, 17,	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	100 and 99 98	Global Output Enable input pins. Test output enable pin.
$\overline{\text{RESET}}$	20	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0 and Y1	18, 19	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y2, Y3 and Y4	103, 102, 101	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/ispEN*	21	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
TDI/SDI*	22	Input - This pin performs two functions. It is the Test Data input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine.
TCLK/SCLK*	23	Input - This pin performs two functions. It is the Test Clock input pin when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
TMS/MODE*	24	Input - This pin performs two functions. It is the Test Mode Select input pin when ispEN is logic high. When ispEN is logic low, it functions as pin to control the operation of the isp state machine.
TRST	97	Input - Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO*	104	Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When ispEN is high it functions as Test Data Out.
GND	1, 10, 27, 45, 63, 81, 107, 125, 143	Ground (GND)
VCC	12, 31, 51, 71, 91, 111, 131, 151	V _{cc}

* ispLSI 3256 Only

Table 2-0002Bisp/3256

Pin Configuration

pLSI and ispLSI 3256 167-pin CPGA Pinout Diagram

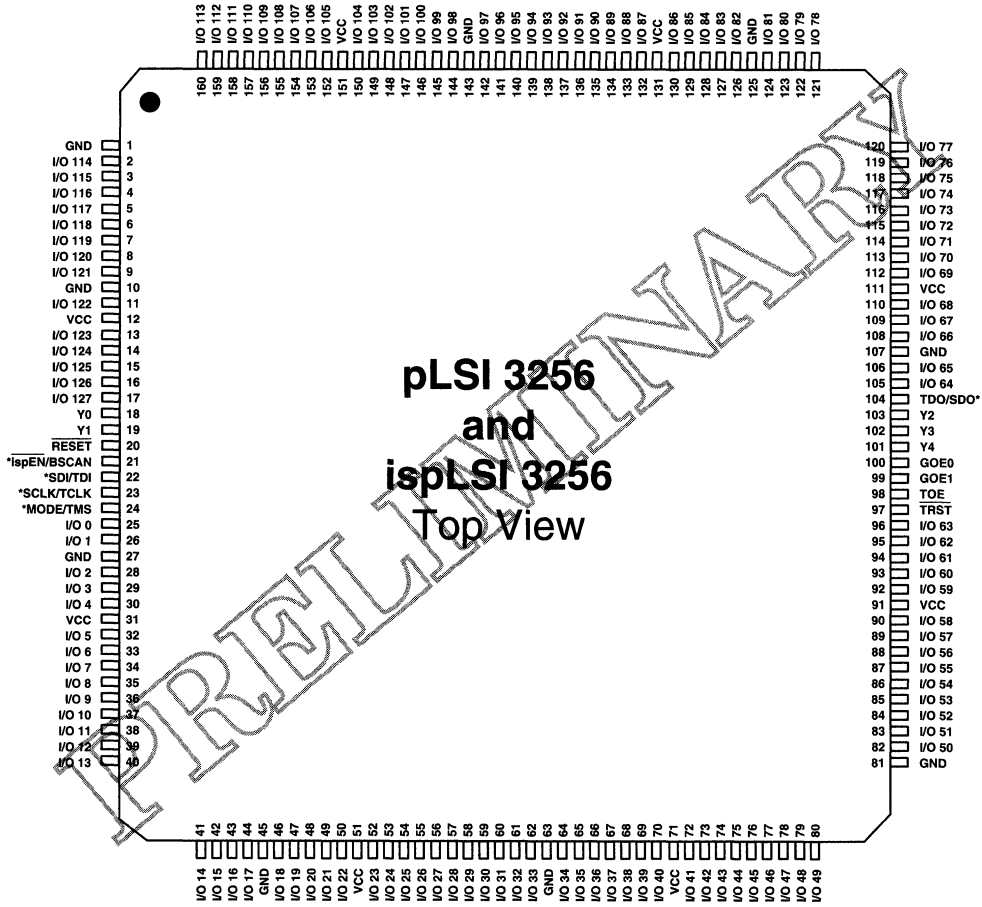


* ispLSI 3256 Only

0123Bisp

Pin Configuration

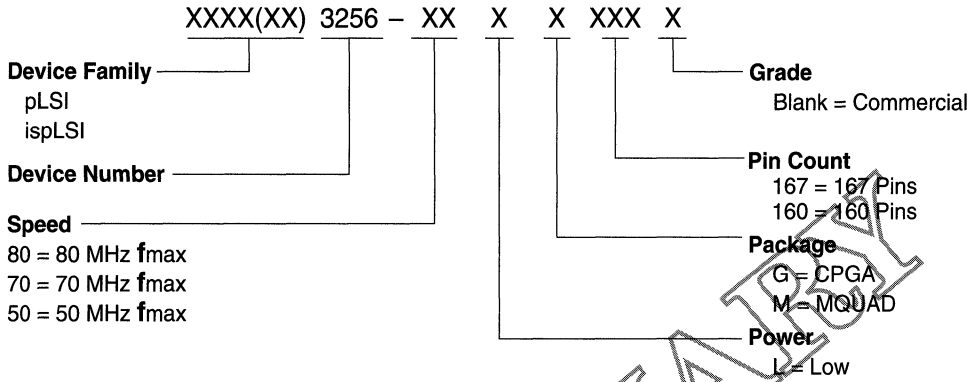
pLSI and ispLSI 3256 160-Pin MQUAD Pinout Diagram



*ispLSI 3256 Only

160-MQFP/3256

Part Number Description



0212Aisp/3256

Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
pLSI	80	15	pLSI 3256-80LM160	160-Pin MQUAD
	80	15	pLSI 3256-80LG167	167-Pin CPGA
	70	17	pLSI 3256-70LM160	160-Pin MQUAD
	70	17	pLSI 3256-70LG167	167-Pin CPGA
	50	23	pLSI 3256-50LM160	160-Pin MQUAD
	50	23	pLSI 3256-50LG160	167-Pin CPGA
ispLSI	80	15	ispLSI 3256-80LM160	160-Pin MQUAD
	80	15	ispLSI 3256-80LG167	167-Pin CPGA
	70	17	ispLSI 3256-70LM160	160-Pin MQUAD
	70	17	ispLSI 3256-70LG167	167-Pin CPGA
	50	23	ispLSI 3256-50LM160	160-Pin MQUAD
	50	23	ispLSI 3256-50LG167	167-Pin CPGA

Table 2- 0041A-08isp/3256

Section 1: Introduction

Section 2: High-Density Programmable Logic

Section 3: Low-Density Programmable Logic

Introduction to Generic Array Logic	3-1
Commercial / Industrial Product Datasheets	
GAL16V8	3-5
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GAL16VP8	3-49
GAL18V10	3-67
GAL20RA10	3-79
GAL20V8	3-97
GAL20V8Z/ZD	3-121
GAL20VP8	3-141
GAL20XV10	3-159
GAL22V10	3-173
ispGAL22V10	3-193
GAL26CV12	3-213
GAL6001	3-231
GAL6002	3-249

Section 4: In-System Programmable Generic Digital Switch (ispGDS) Devices

Section 5: Military Program

Section 6: Development Tools

Section 7: Quality and Reliability

Section 8: General Information

Introduction to Generic Array Logic

Overview

Lattice, the inventor of the Generic Array Logic (GAL[®]) family of low density, E²CMOS PLDs is the leading supplier of low density CMOS PLDs in the world. Features such as industry leading performance, low power E²CMOS technology, 100% testability and 100% programming yields make the GAL family the preferred choice among system designers.

The GAL family contains 14 product architectures with a variety of performance levels specified across commercial, industrial and military (MIL-STD-883) operating ranges to meet the demands of any system logic design.

These GAL products can be segmented into two broad categories:

Base Products — Aimed at providing a superior design alternative to the bipolar PLD, these five architectures replace over 98% of all bipolar PAL devices. The GAL16V8 and GAL20V8 replace 42 different PAL devices. The GAL22V10, GAL20RA10 and GAL20XV10 round out the Base products. These GAL devices meet, and in most cases beat bipolar PAL performance specifications while consuming significantly lower power and offering higher quality and reliability via Lattice's electrically reprogrammable E²CMOS technology.

Extension Products — These products build upon the Base GAL product features to provide enhanced functionality including innovative architectures (GAL18V10, GAL26CV12, GAL6001/6002), 64mA high output drive (GAL16VP8 & GAL20VP8), "Zero power" operation (GAL16V8Z/ZD & GAL20V8Z/ZD) and in-system programmability (ispGAL22V10).

A PRODUCT FOR ANY SYSTEM DESIGN NEED

Lattice GAL products have the performance, architectural features, low power, and high quality to meet the needs of the most demanding system designs.

The GAL16V8 and GAL20V8

- Performance ranges from the industry's fastest, at 5ns Tpd to popular 25ns versions
- Low power consumption with Low Power versions rated at 75mA typical and Quarter Power versions at 45mA typical
- 8 Powerful Output Logic Macrocells (OLMCs) with 8 Product Terms each
- Standard 20-pin (DIP and PLCC) and 24/28-pin (DIP/PLCC) packages

The GAL22V10

- Available in industry leading 5ns/200MHz versions through 25ns versions
- Low power consumption with Low Power versions at 90mA and Quarter Power versions at 45mA typical
- 10 OLMCS with variable Product Terms per OLMC ranging from 8 to 16 for increased logic capability
- Standard 24-pin DIP and 28-pin PLCC packages

The GAL18V10

10 Outputs in a 20-pin Package

- 20-pin space-saving subset of the popular GAL22V10
- 8-10 Product Terms per OLMC
- Ideal for p.c. board area constrained designs
- Only 10 output, 20-pin PLD in the market

The GAL26CV12

Expanded Logic Density in a 28-pin DIP/PLCC Package

- 28-pin superset of the popular GAL22V10
- World's fastest 28-pin PLD at 7.5ns
- 26 inputs, 12 outputs
- Flexible 22V10 OLMC
- Fully utilized 28-pin PLCC package give added functionality over the 22V10 at no space premium!

Introduction to Generic Array Logic

The GAL20RA10

High Performance Asynchronous Logic

- 10 OLMCs
- 10 Independently programmable clocks
- Each macrocell has an independent product term clock
- Fast 10ns Tpd performance
- Faster and lower power than bipolar PAL
- Available in 24/28-pin DIP/PLCC packages

The GAL16V8Z/ZD and GAL20V8Z/ZD

Zero Stand-by Power

- 50 μ A Icc typical stand-by power (100 μ A MAX)
- 12ns Tpd performance
- Two power-down modes
 - Input transition detection (Z)
 - Dedicated power-down pin (ZD)
- Available in 20-pin DIP/PLCC/SOIC and 24/28-pin DIP/PLCC packages

The GAL20XV10

Perfect for Fast Counters, Decoders or Comparators

- Utilizes powerful XOR function for efficient implementation of arithmetic functions
- Replaces: PAL20L10, 20X10, 20X8 and 20X4, 12L10
- 10ns/100MHz performance significantly outperforms bipolar PALs
- Perfect for video, multimedia and graphics applications
- Available in 24/28-pin DIP/PLCC packages

The GAL6001 and GAL6002

The Logic Density of an FPLA Architecture

- Unprecedented logic density in a 24/28-pin DIP/PLCC
- Functional equivalent of 2 GAL22V10s
- 38 Macrocells
 - 10 Input Macrocells
 - 10 Output Macrocells
 - 10 I/O Macrocells
 - 8 Buried Logic Macrocells
- 15ns/75MHz performance
- Ideal for register-intensive applications

The GAL16VP8 and GAL20VP8

Ideal for Bus Interface or Memory Control Logic

- High output drive versions of the GAL16V8 and GAL20V8
- IOL = 64mA vs standard 24mA
- Combines GAL architecture with high drive of 74XX244 buffer families
- Fast 15ns/80MHz performance
- Available in 20-pin DIP/PLCC and 24/28-pin DIP/PLCC packages

The ispGAL22V10

Offers In-System Programmability

- Popular 22V10 architecture
- In-system programmable
- Same 28-pin PLCC as GAL22V10
- Fast 7.5ns/111MHz performance
- Unprecedented design and manufacturing flexibility

Introduction to Generic Array Logic

Commercial/Industrial/Military Grades Available

The Lattice GAL family is available in a wide range of commercial, industrial and military Grade versions. In the military arena, Lattice offers a MIL-STD-883 family as well as a family of Standard Military Drawing (SMD) devices.

The following table summarizes the Lattice GAL product offering.

Table 1. Lattice GAL Product Offering

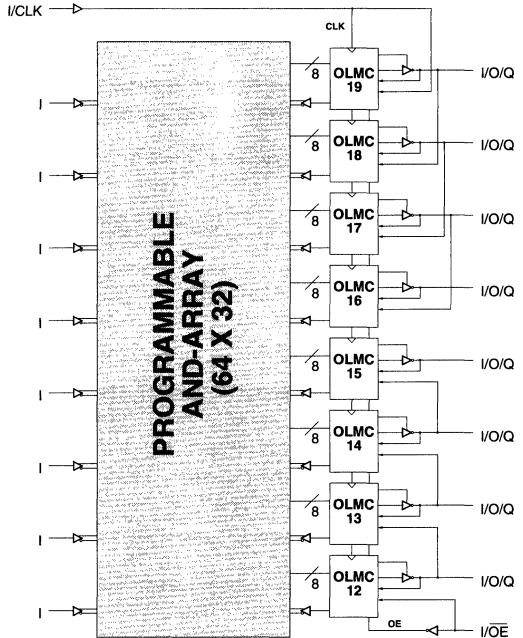
	Speed Options by Grade (Tpd in ns)		
	Commercial	Industrial	883 / Military
GAL16V8 Low Power	5, 7.5, 10, 15, 25	7.5, 10, 15, 25	10, 15, 20, 30
GAL16V8 Quarter Power	15, 25	20, 25	—
GAL16V8Z/ZD Zero Power	12, 15	—	—
GAL16VP8	15, 25	—	—
GAL18V10	15, 20	—	—
GAL20RA10	10, 15, 20, 30	20	—
GAL20V8 Low Power	5, 7.5, 10, 15, 25	10, 15, 25	10, 15, 20
GAL20V8 Quarter Power	15, 25	20, 25	—
GAL20V8Z/ZD Zero Power	12, 15	—	—
GAL20VP8	15, 25	—	—
GAL20XV10	10, 15, 20	—	—
GAL22V10 Low Power	5, 6, 7.5, 10, 15, 25	10, 15, 20, 25	15, 20, 25, 30
GAL22V10 Quarter Power	15, 25	—	—
ispGAL22V10	7.5, 10, 15	—	—
GAL26CV12	7.5, 10, 15, 20	10, 15, 20	—
GAL6001	30	—	—
GAL6002	15, 20	—	—
Vcc	5V ±5%	5V ±10%	5V ±10%
Temperature	0 to 75°C	-40 to 85°C	-55 to 125°C
Packaging	Plastic DIP, PLCC & SOIC	Plastic DIP & PLCC	CERDIP & LCC

Notes

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 5 ns Maximum Propagation Delay
 - F_{max} = 166 MHz
 - 4 ns Maximum from Clock Input to Data Output
 - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc} on Low Power Device
 - 45mA Typ I_{cc} on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



3

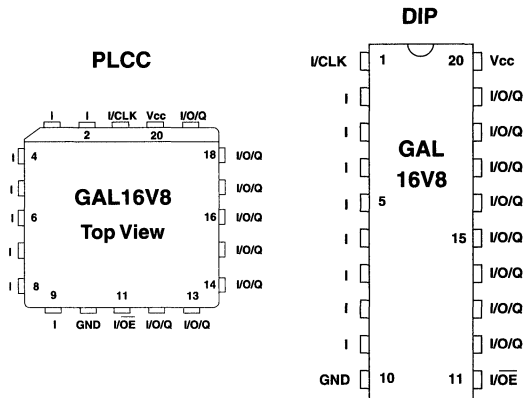
DESCRIPTION

The GAL16V8C, at 5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

PIN CONFIGURATION



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GAL16V8 ORDERING INFORMATION

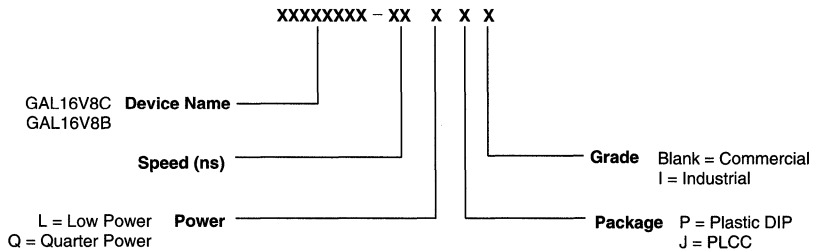
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL16V8C-5LP	20-Pin Plastic DIP
			115	GAL16V8C-5LJ	20-Lead PLCC
7.5	7	5	115	GAL16V8B-7LP	20-Pin Plastic DIP
			115	GAL16V8B-7LJ	20-Lead PLCC
10	10	7	115	GAL16V8B-10LP	20-Pin Plastic DIP
			115	GAL16V8B-10LJ	20-Lead PLCC
15	12	10	55	GAL16V8B-15QP	20-Pin Plastic DIP
			55	GAL16V8B-15QJ	20-Lead PLCC
			90	GAL16V8B-15LP	20-Pin Plastic DIP
			90	GAL16V8B-15LJ	20-Lead PLCC
25	15	12	55	GAL16V8B-25QP	20-Pin Plastic DIP
			55	GAL16V8B-25QJ	20-Lead PLCC
			90	GAL16V8B-25LP	20-Pin Plastic DIP
			90	GAL16V8B-25LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	130	GAL16V8C-7LPI	20-Pin Plastic DIP
			130	GAL16V8C-7LJI	20-Lead PLCC
10	10	7	130	GAL16V8B-10LPI	20-Pin Plastic DIP
			130	GAL16V8B-10LJI	20-Lead PLCC
15	12	10	130	GAL16V8B-15LPI	20-Pin Plastic DIP
			130	GAL16V8B-15LJI	20-Lead PLCC
20	13	11	65	GAL16V8B-20QPI	20-Pin Plastic DIP
			65	GAL16V8B-20QJI	20-Lead PLCC
25	15	12	65	GAL16V8B-25QPI	20-Pin Plastic DIP
			65	GAL16V8B-25QJI	20-Lead PLCC
			130	GAL16V8B-25LPI	20-Pin Plastic DIP
			130	GAL16V8B-25LJI	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and ACO, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8 can emulate. It also shows the OLMC mode under which the GAL16V8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8	GAL16V8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

3

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/IC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered" ¹	"Complex" ¹	"Simple" ¹	GAL16V8A
PLDesigner	P16V8R ²	P16V8C ²	P16V8C ²	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS ³	G16V8

1) Used with **Configuration** keyword.
 2) Prior to Version 2.0 support.
 3) Supported on Version 1.20 or later.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

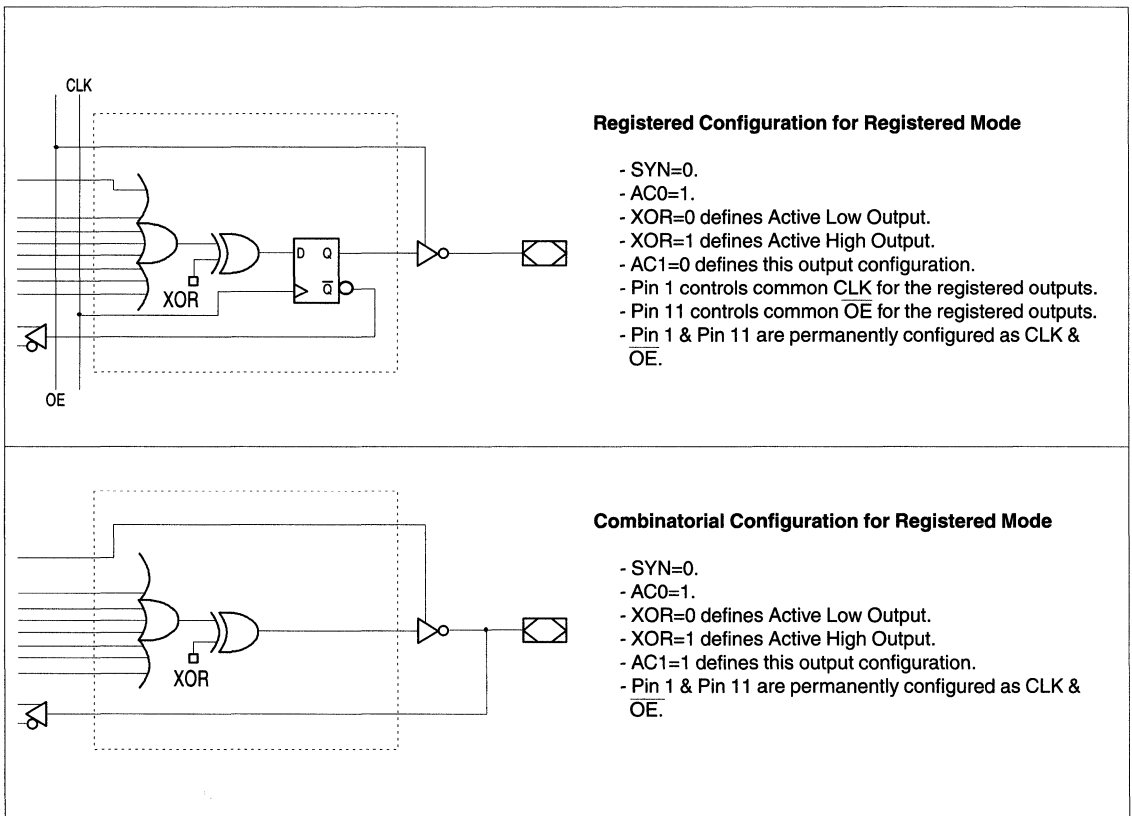
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this

mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

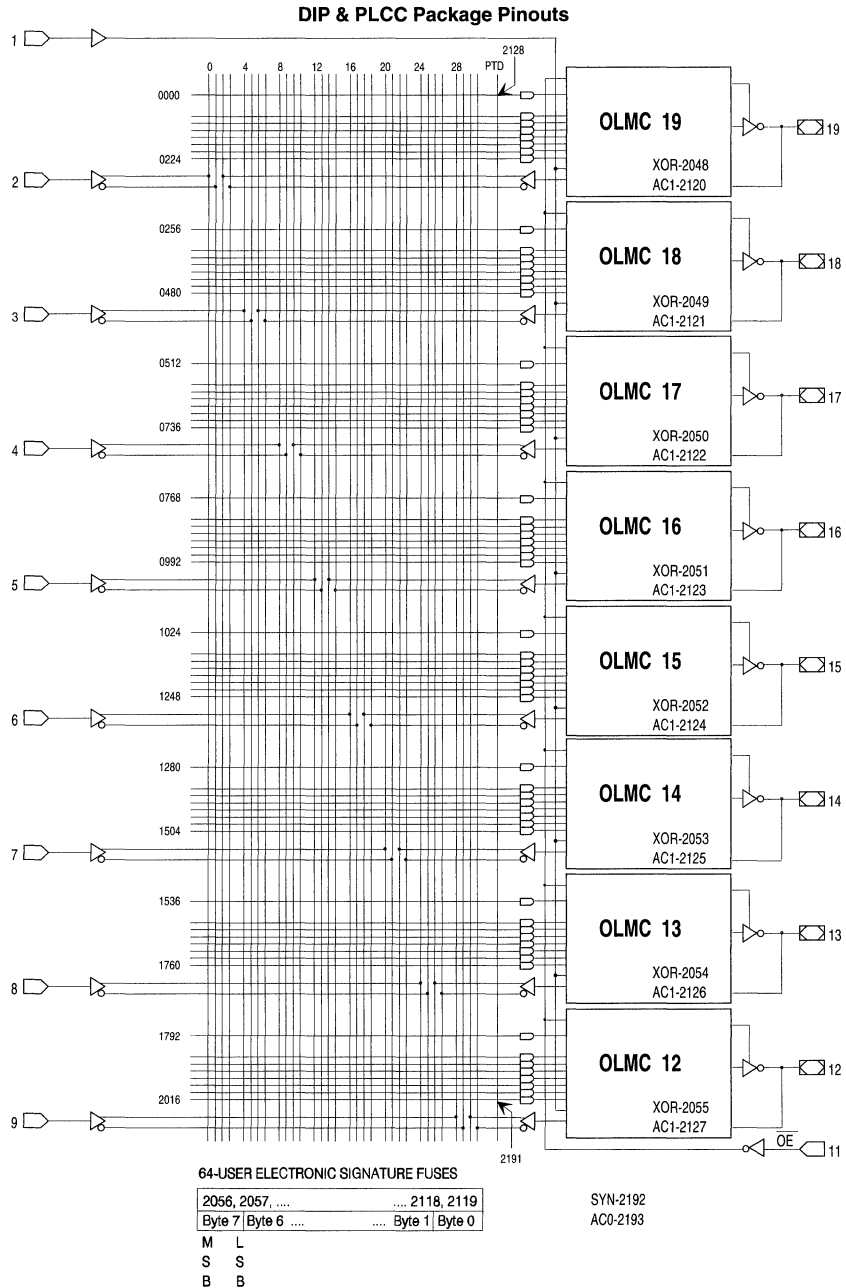
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM



COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

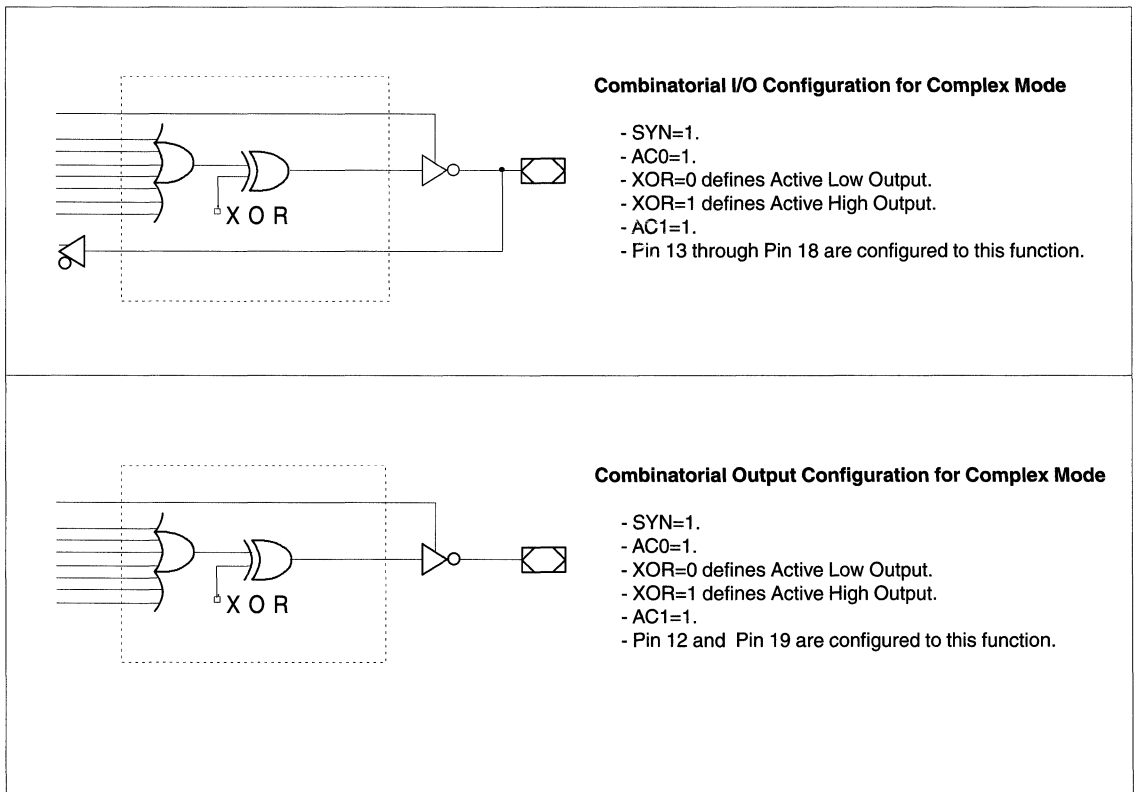
Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input ca-

pability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

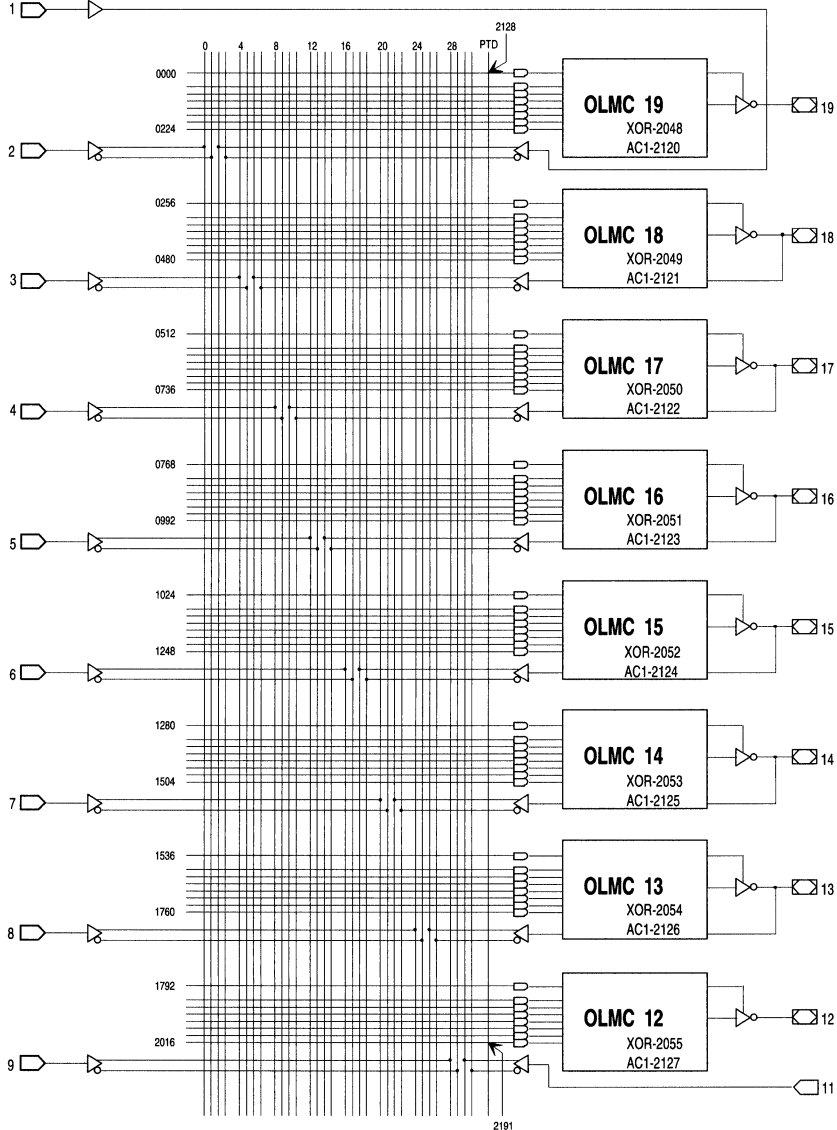
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, 2118, 2119
Byte 7 Byte 6 Byte 1 Byte 0
M	L
S	S
B	B

SYN-2192
AC0-2193

SIMPLE MODE

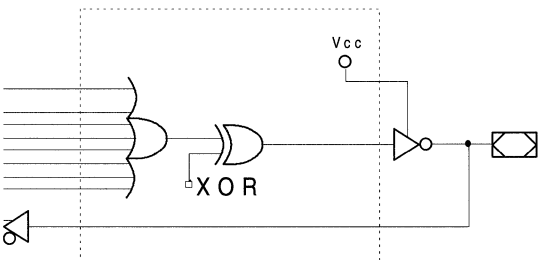
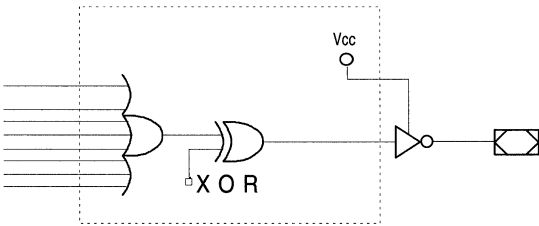
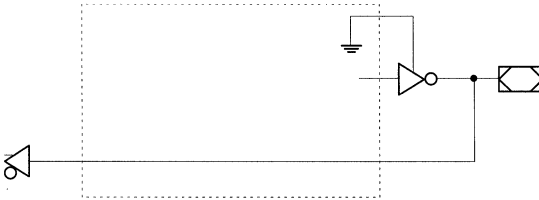
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

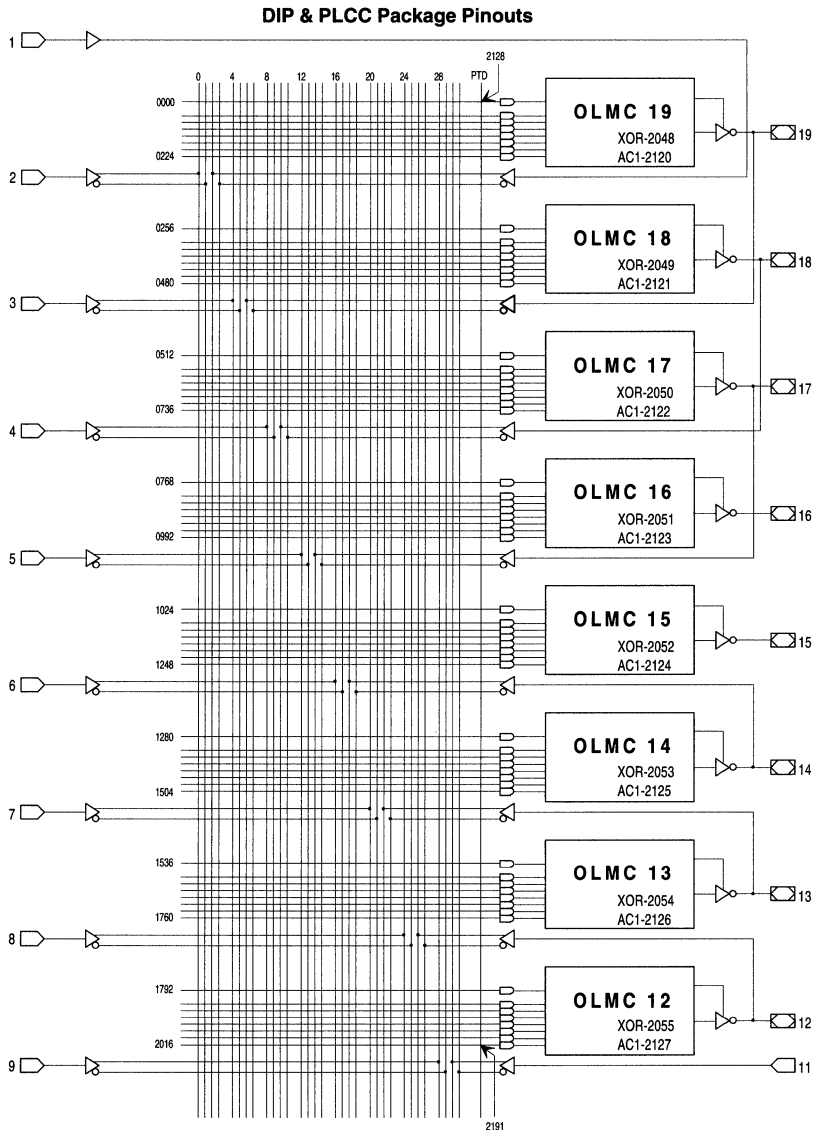
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - All OLMC except pins 15 & 16 can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - Pins 15 & 16 are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - All OLMC except pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, 2118, 2119
Byte 7 Byte 6 Byte 1 Byte 0

M L
S S
B B

SYN-2192
ACO-2193

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with

Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX.$ $V_{IN} = V_{IL}$ or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX.$ $V_{IN} = V_{IL}$ or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V$ $V_{OUT} = 0.5V$ $T_A = 25^\circ C$	-30	—	-150	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V$ $V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -5	—	75	115	mA
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INDUSTRIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V$ $V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -7	—	75	130	mA
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1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		IND		UNITS
			-5		-7		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	1	5	1	7.5	ns
t_{co}	A	Clock to Output Delay	1	4	1	5	ns
t_{cf}^2	—	Clock to Feedback Delay	—	3	—	3	ns
t_{su}	—	Setup Time, Input or Feedback before Clock \uparrow	3	—	7	—	ns
t_h	—	Hold Time, Input or Feedback after Clock \uparrow	0	—	0	—	ns
f_{max}^3	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	142.8	—	83.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	166	—	100	—	MHz
	A	Maximum Clock Frequency with No Feedback	166	—	100	—	MHz
t_{wh}	—	Clock Pulse Duration, High	3	—	5	—	ns
t_{wl}	—	Clock Pulse Duration, Low	3	—	5	—	ns
t_{en}	B	Input or I/O to Output Enabled	1	6	1	9	ns
	B	\overline{OE} to Output Enabled	1	6	1	6	ns
t_{dis}	C	Input or I/O to Output Disabled	1	5	1	9	ns
	C	\overline{OE} to Output Disabled	1	5	1	6	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

 3) Refer to **f_{max} Descriptions** section. Characterized initially and after any design or process changes that may affect these parameters.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{cc} = 5.0\text{V}$, $V_i = 2.0\text{V}$
$C_{i/o}$	I/O Capacitance	8	pF	$V_{cc} = 5.0\text{V}$, $V_{i/o} = 2.0\text{V}$

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{\text{toggle}} = 15\text{MHz}$ Outputs Open	L -7/-10	—	75	115	mA
			L -15/-25	—	75	90	mA
			Q -15/-25	—	45	55	mA

INDUSTRIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{\text{toggle}} = 15\text{MHz}$ Outputs Open	L -10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

- 1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND ¹ .	DESCRIPTION	COM		COM / IND		COM / IND		IND		COM / IND		UNITS
			-7		-10		-15		-20		-25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to	3	7.5	3	10	3	15	3	20	3	25	ns
		8 outputs switching											
		Comb. Output											
		1 output switching	—	7	—	—	—	—	—	—	—	—	ns
t_{co}	A	Clock to Output Delay	2	5	2	7	2	10	2	11	2	12	ns
t_{cf}^2	—	Clock to Feedback Delay	—	3	—	6	—	8	—	9	—	10	ns
t_{su}	—	Setup Time, Input or Fdbk before Clk \uparrow	7	—	10	—	12	—	13	—	15	—	ns
t_h	—	Hold Time, Input or Fdbk after Clk \uparrow	0	—	0	—	0	—	0	—	0	—	ns
f_{max}^3	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	83.3	—	58.8	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	100	—	62.5	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	62.5	—	62.5	—	50	—	41.6	—	MHz
t_{wh}	—	Clock Pulse Duration, High	5	—	8	—	8	—	10	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	5	—	8	—	8	—	10	—	12	—	ns
t_{en}	B	Input or I/O to Output Enabled	3	9	3	10	—	15	—	20	—	25	ns
	B	\overline{OE} to Output Enabled	2	6	2	10	—	15	—	18	—	20	ns
t_{dis}	C	Input or I/O to Output Disabled	2	9	2	10	—	15	—	20	—	25	ns
	C	\overline{OE} to Output Disabled	1.5	6	1.5	10	—	15	—	18	—	20	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

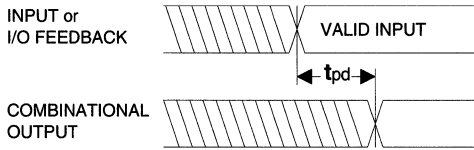
 3) Refer to **f_{max} Descriptions** section.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

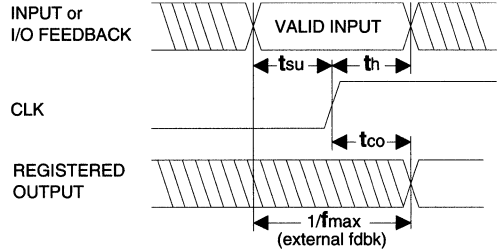
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{cc} = 5.0V$, $V_i = 2.0V$
$C_{i/o}$	I/O Capacitance	8	pF	$V_{cc} = 5.0V$, $V_{i/o} = 2.0V$

*Guaranteed but not 100% tested.

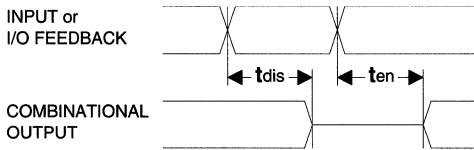
SWITCHING WAVEFORMS



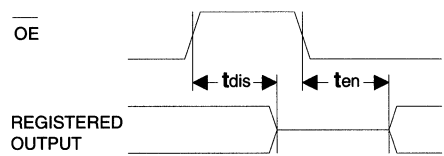
Combinatorial Output



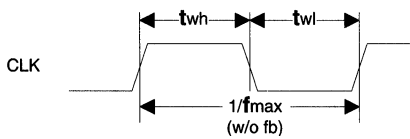
Registered Output



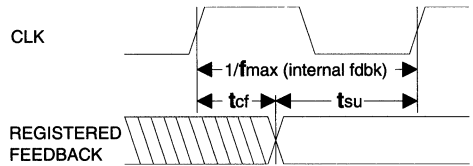
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

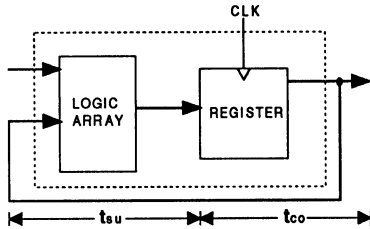


Clock Width



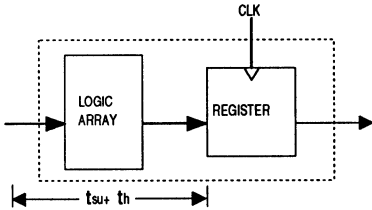
f_{max} with Feedback

f_{max} DESCRIPTIONS



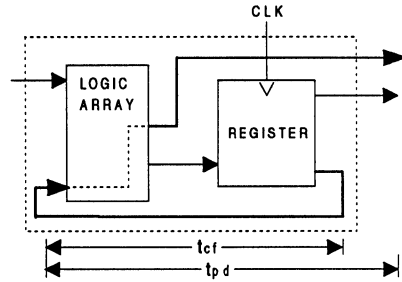
f_{max} with External Feedback 1/(t_{su}+t_{co})

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.



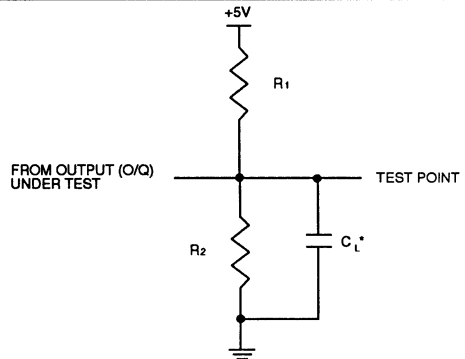
f_{max} with Internal Feedback 1/(t_{su}+t_{cf})

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback (t_{cf} = 1/f_{max} - t_{su}). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Times	GAL16V8B	2 – 3ns 10% – 90%
	GAL16V8C	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V	
Output Timing Reference Levels	1.5V	
Output Load	See Figure	

3-state levels are measured 0.5V from steady-state active level.



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL16V8B Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	200Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	200Ω	390Ω
C	Active High	∞	390Ω
	Active Low	200Ω	390Ω

GAL16V8C Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	200Ω	200Ω	50pF
B	Active High	∞	200Ω
	Active Low	200Ω	200Ω
C	Active High	∞	200Ω
	Active Low	200Ω	200Ω

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL16V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided in the GAL16V8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL16V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

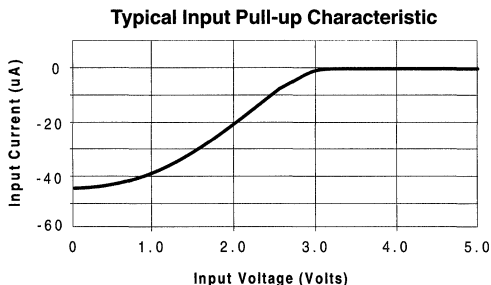
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL16V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

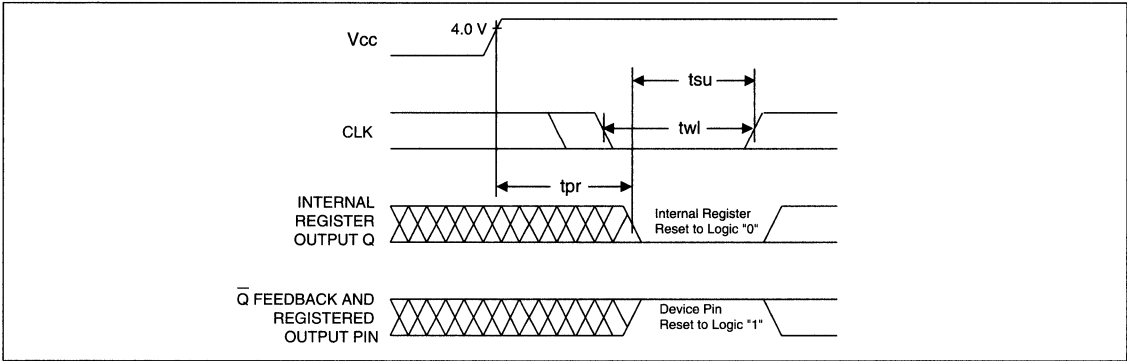
INPUT BUFFERS

GAL16V8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16V8 input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC} , or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.



POWER-UP RESET

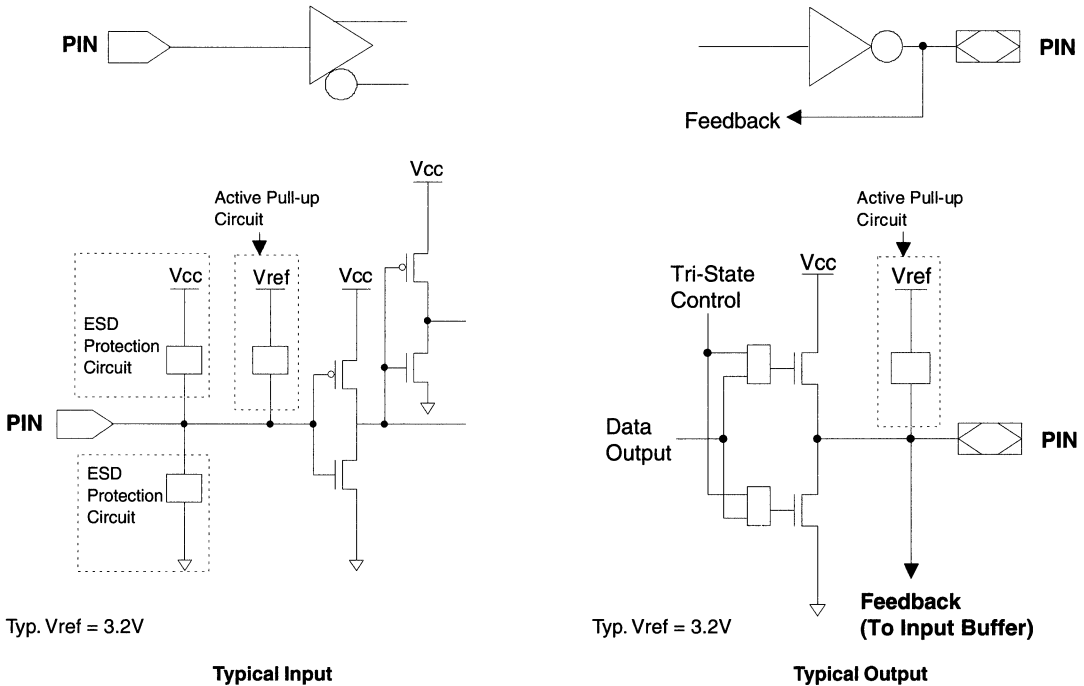


3

Circuitry within the GAL16V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

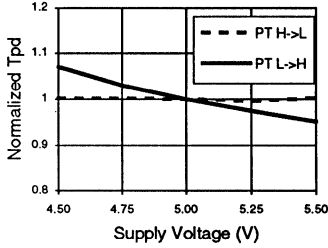
conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

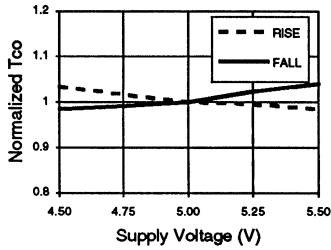


GAL 16V8C-5: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

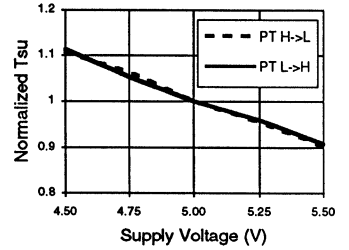
Normalized Tpd vs Vcc



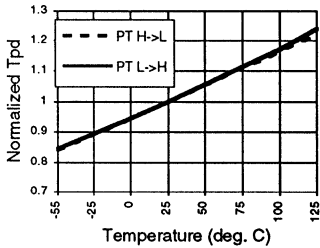
Normalized Tco vs Vcc



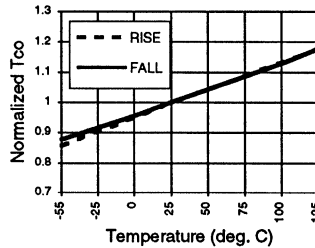
Normalized Tsu vs Vcc



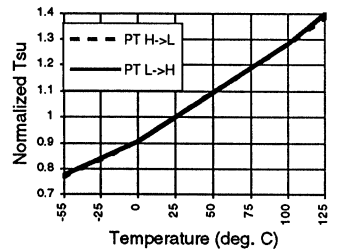
Normalized Tpd vs Temp



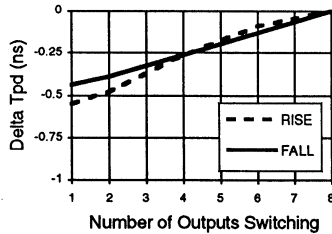
Normalized Tco vs Temp



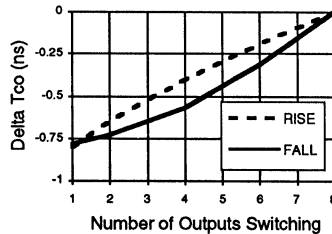
Normalized Tsu vs Temp



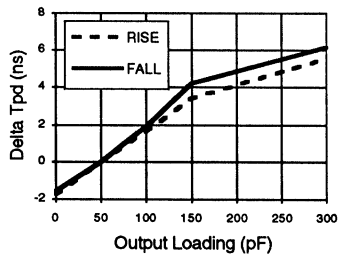
Delta Tpd vs # of Outputs Switching



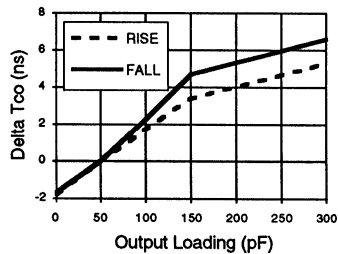
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

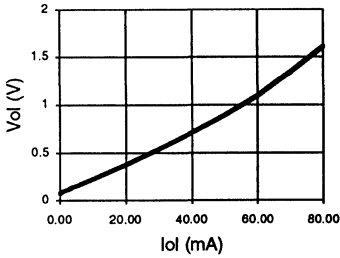


Delta Tco vs Output Loading

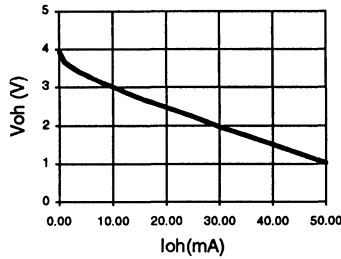


GAL 16V8C-5: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

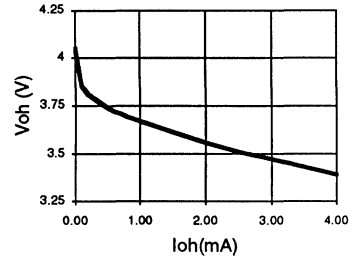
Vol vs Iol



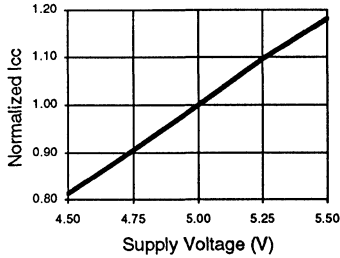
Voh vs Ioh



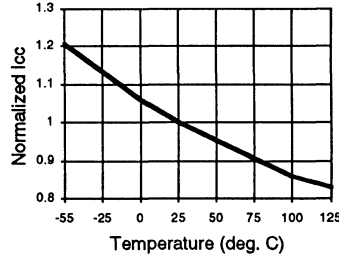
Voh vs Ioh



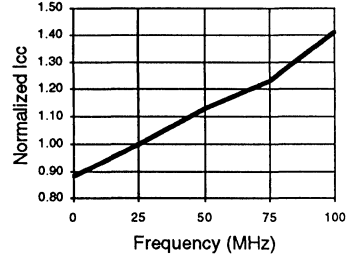
Normalized Icc vs Vcc



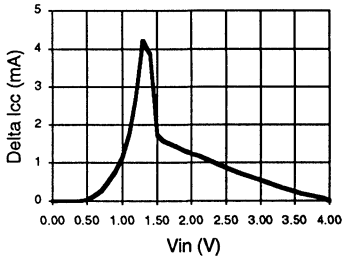
Normalized Icc vs Temp



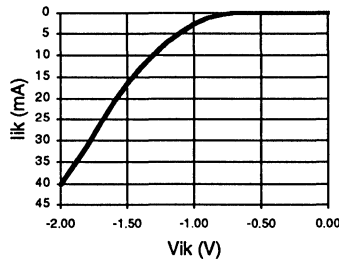
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

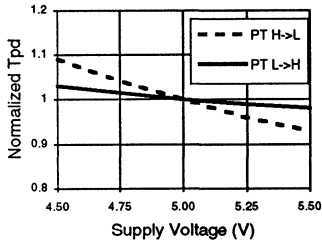


Input Clamp (Vik)

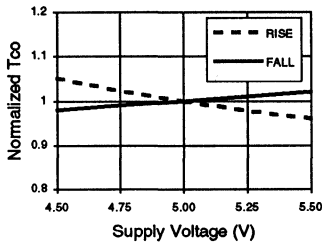


GAL 16V8B-7/10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

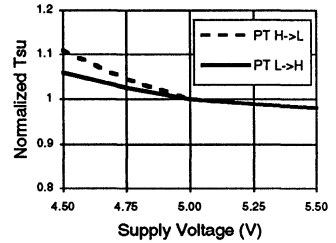
Normalized Tpd vs Vcc



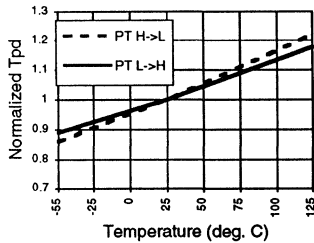
Normalized Tco vs Vcc



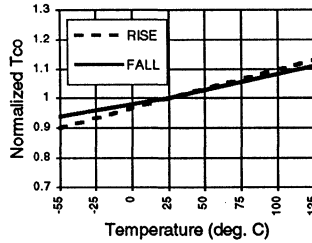
Normalized Tsu vs Vcc



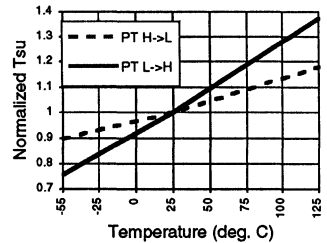
Normalized Tpd vs Temp



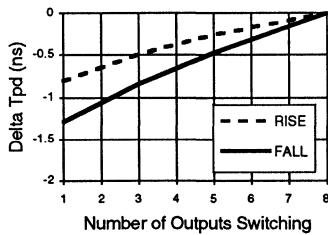
Normalized Tco vs Temp



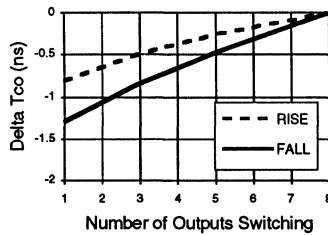
Normalized Tsu vs Temp



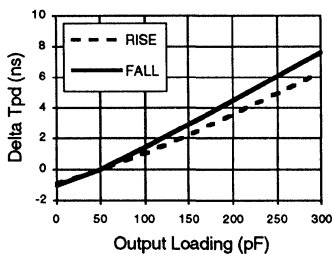
Delta Tpd vs # of Outputs Switching



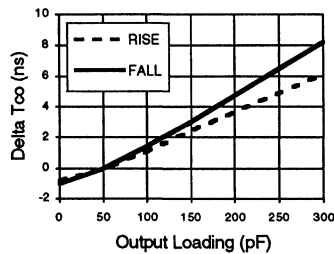
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

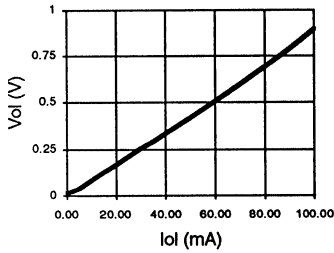


Delta Tco vs Output Loading

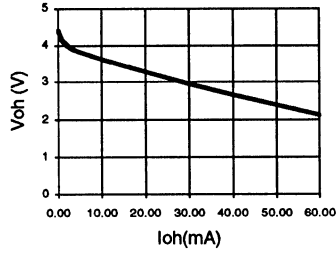


GAL 16V8B-7/10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

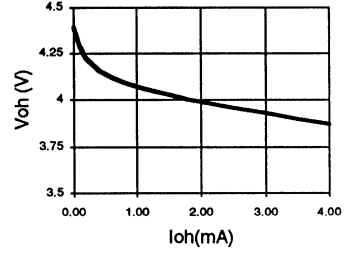
Vol vs Iol



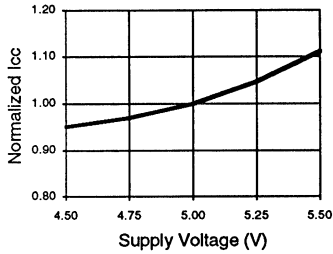
Voh vs Ioh



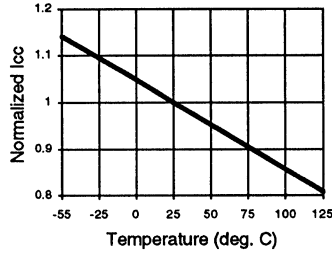
Voh vs Ioh



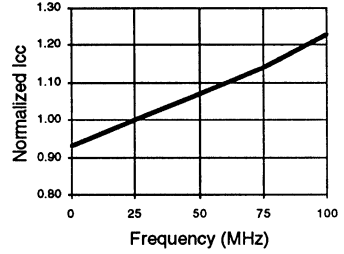
Normalized Icc vs Vcc



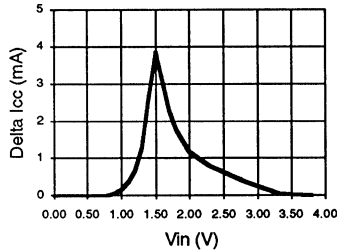
Normalized Icc vs Temp



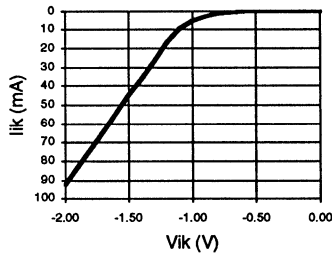
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)

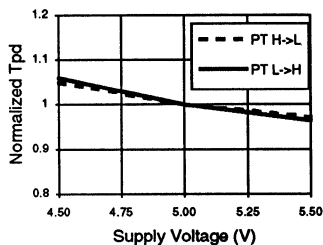


Input Clamp (Vik)

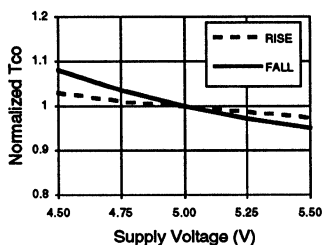


GAL 16V8B-15/25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

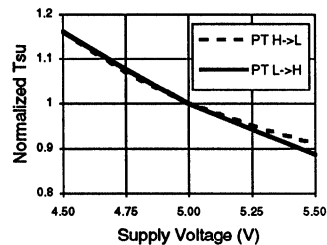
Normalized Tpd vs Vcc



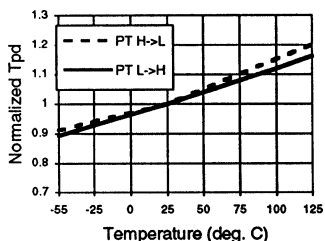
Normalized Tco vs Vcc



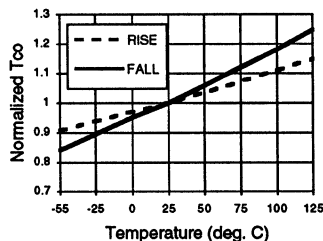
Normalized Tsu vs Vcc



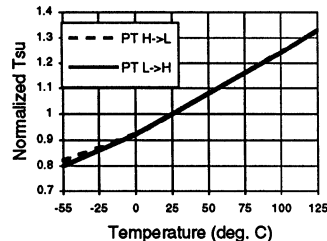
Normalized Tpd vs Temp



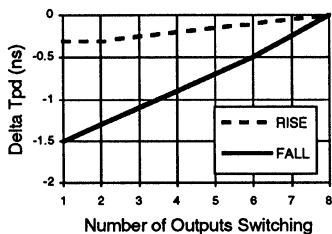
Normalized Tco vs Temp



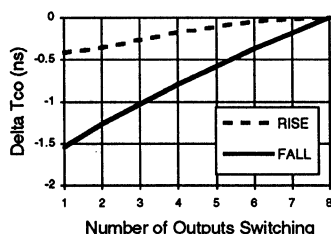
Normalized Tsu vs Temp



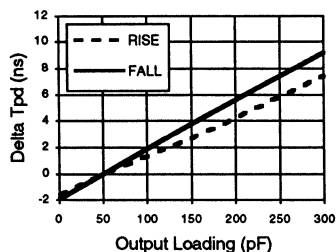
Delta Tpd vs # of Outputs Switching



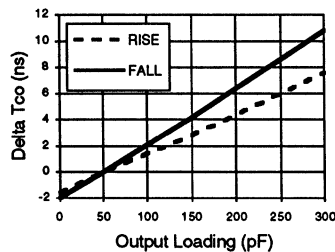
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

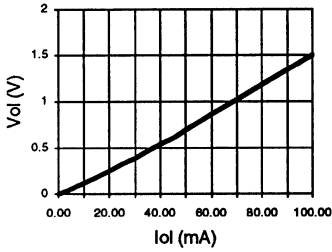


Delta Tco vs Output Loading

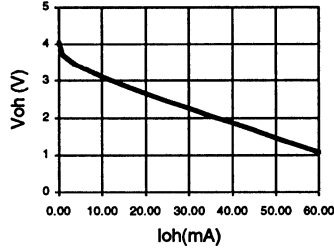


GAL 16V8B-15/25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

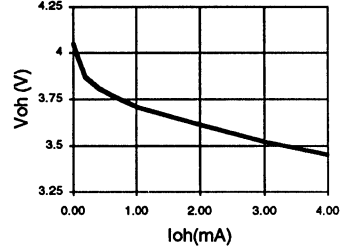
Vol vs Iol



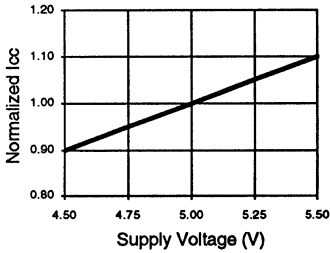
Voh vs Ioh



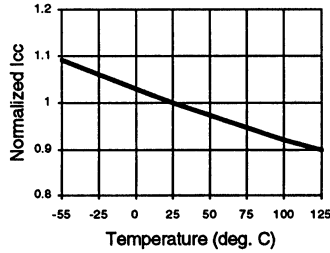
Voh vs Ioh



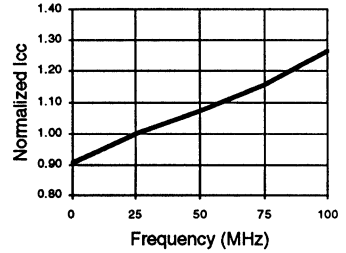
Normalized Icc vs Vcc



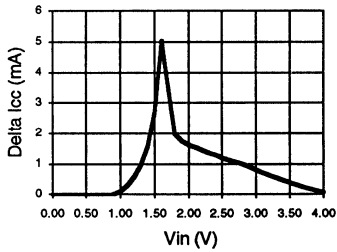
Normalized Icc vs Temp



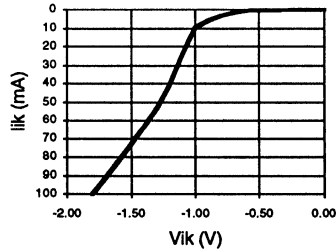
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)



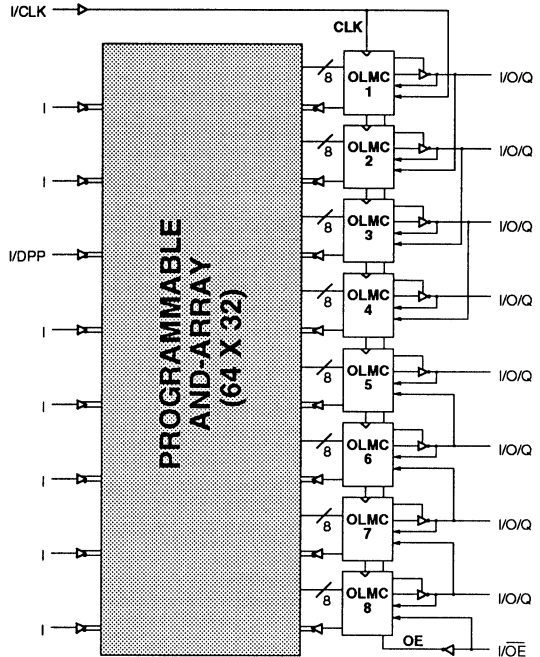
Input Clamp (Vik)



FEATURES

- **ZERO POWER E²CMOS TECHNOLOGY**
 - 100µA Standby Current
 - Input Transition Detection on GAL16V8Z
 - Dedicated Power-down Pin on GAL16V8ZD
 - Input and Output Latching During Power Down
- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
 - 12 ns Maximum Propagation Delay
 - F_{max} = 83.3 MHz
 - 8 ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Output Drive
 - UltraMOS® Advanced CMOS Technology
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Architecturally Similar to Standard GAL16V8
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - Battery Powered Systems
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



3

DESCRIPTION

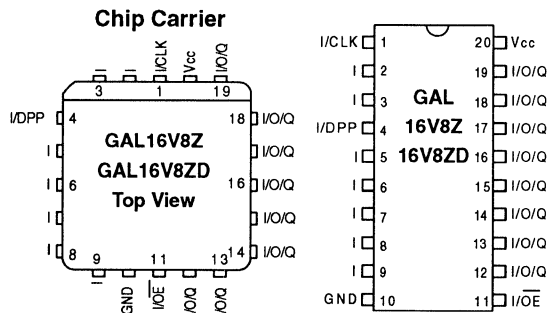
The GAL16V8Z and GAL16V8ZD, at 100 µA standby current and 12ns propagation delay provides the highest speed and lowest power combination PLD available in the market. The GAL16V8Z/D is manufactured using Lattice's advanced zero power E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology.

The GAL16V8Z uses Input Transition Detection (ITD) to put the device in standby mode and is capable of emulating the full functionality of the standard GAL16V8. The GAL16V8ZD utilizes a dedicated power-down pin (DPP) to put the device in standby mode. It has 15 inputs available to the AND array.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

PIN CONFIGURATION

DIP/SOIC



GAL16V8Z/ZD ORDERING INFORMATION

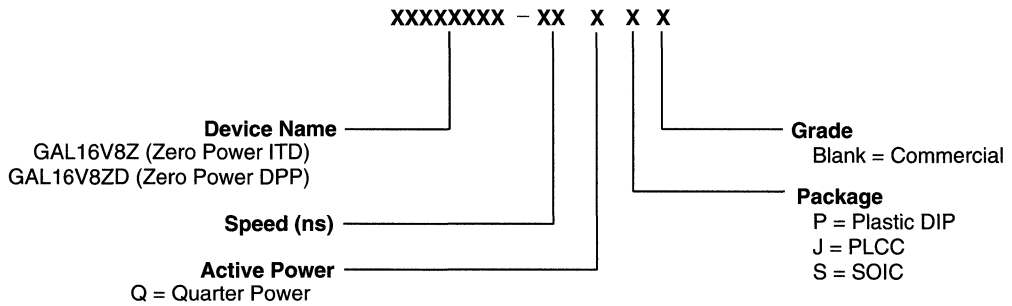
GAL16V8Z: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	I _{sb} (μA)	Ordering #	Package
12	10	8	55	100	GAL16V8Z-12QP	20-Pin Plastic DIP
			55	100	GAL16V8Z-12QJ	20-Lead PLCC
			55	100	GAL16V8Z-12QS	20-Lead SOIC
15	15	10	55	100	GAL16V8Z-15QP	20-Pin Plastic DIP
			55	100	GAL16V8Z-15QJ	20-Lead PLCC
			55	100	GAL16V8Z-15QS	20-Lead SOIC

GAL16V8ZD: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	I _{sb} (μA)	Ordering #	Package
12	10	8	55	100	GAL16V8ZD-12QP	20-Pin Plastic DIP
			55	100	GAL16V8ZD-12QJ	20-Lead PLCC
15	15	10	55	100	GAL16V8ZD-15QP	20-Pin Plastic DIP
			55	100	GAL16V8ZD-15QJ	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and ACO, control the mode configuration for all macrocells. The

XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8Z/D. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL16V8 JEDEC fuse pattern generated by the logic compilers for the GAL16V8Z/D, special attention must be given to pin 4 (DPP) to make sure that it is not used as one of the functional inputs.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

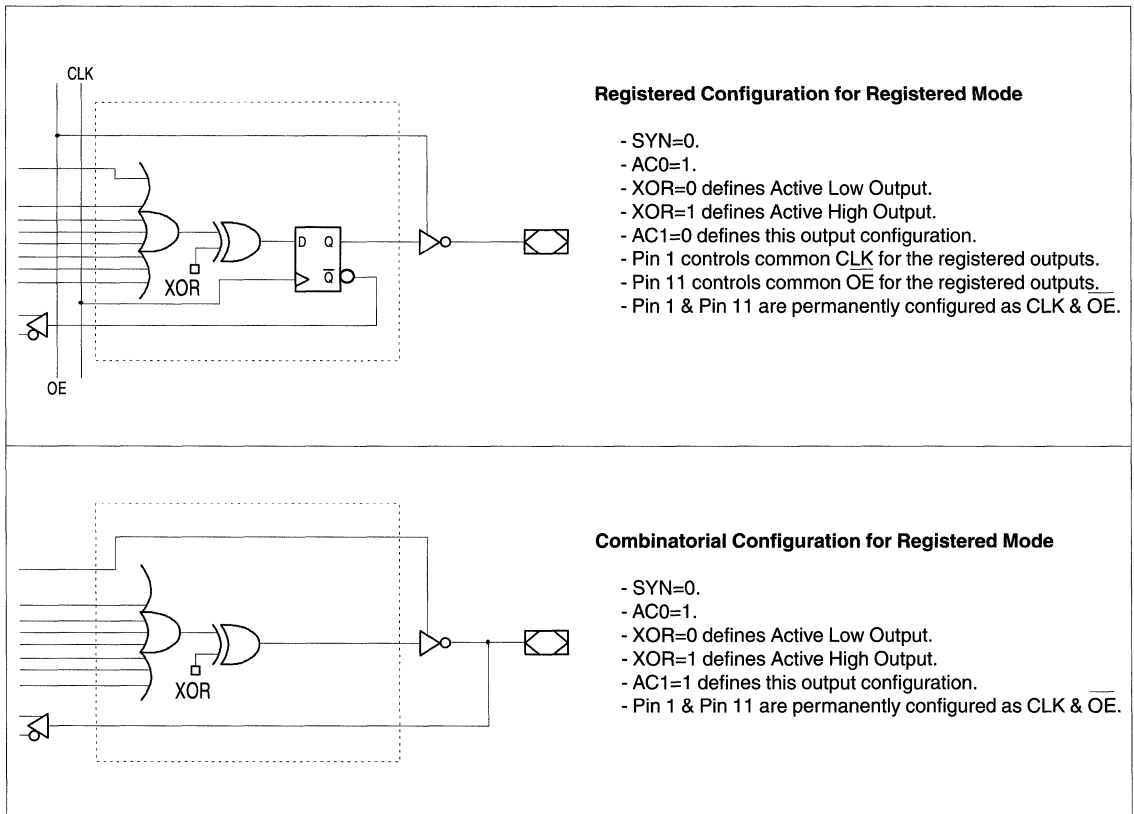
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

Pin 4 is used as dedicated power-down pin on GAL16V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

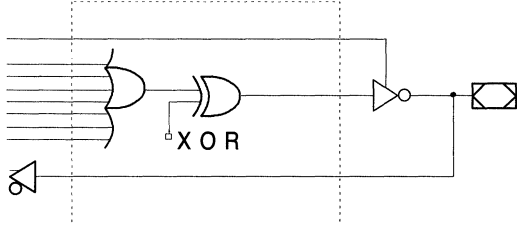
Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

Pin 4 is used as dedicated power-down pin on GAL16V8ZD. It cannot be used as functional input.

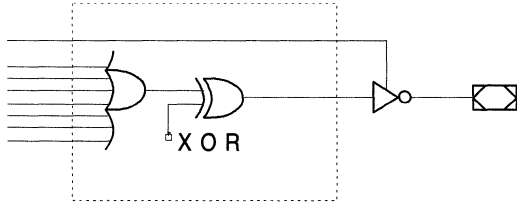
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



The diagram shows a macrocell with four inputs on the left. The top three inputs go to an OR gate. The bottom input goes to an AND gate. The output of the AND gate is labeled 'XOR'. The output of the OR gate goes to an AND gate. The output of this AND gate goes to an inverter. The output of the inverter goes to a multiplexer. The output of the multiplexer goes to an output pin.

Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 13 through Pin 18 are configured to this function.



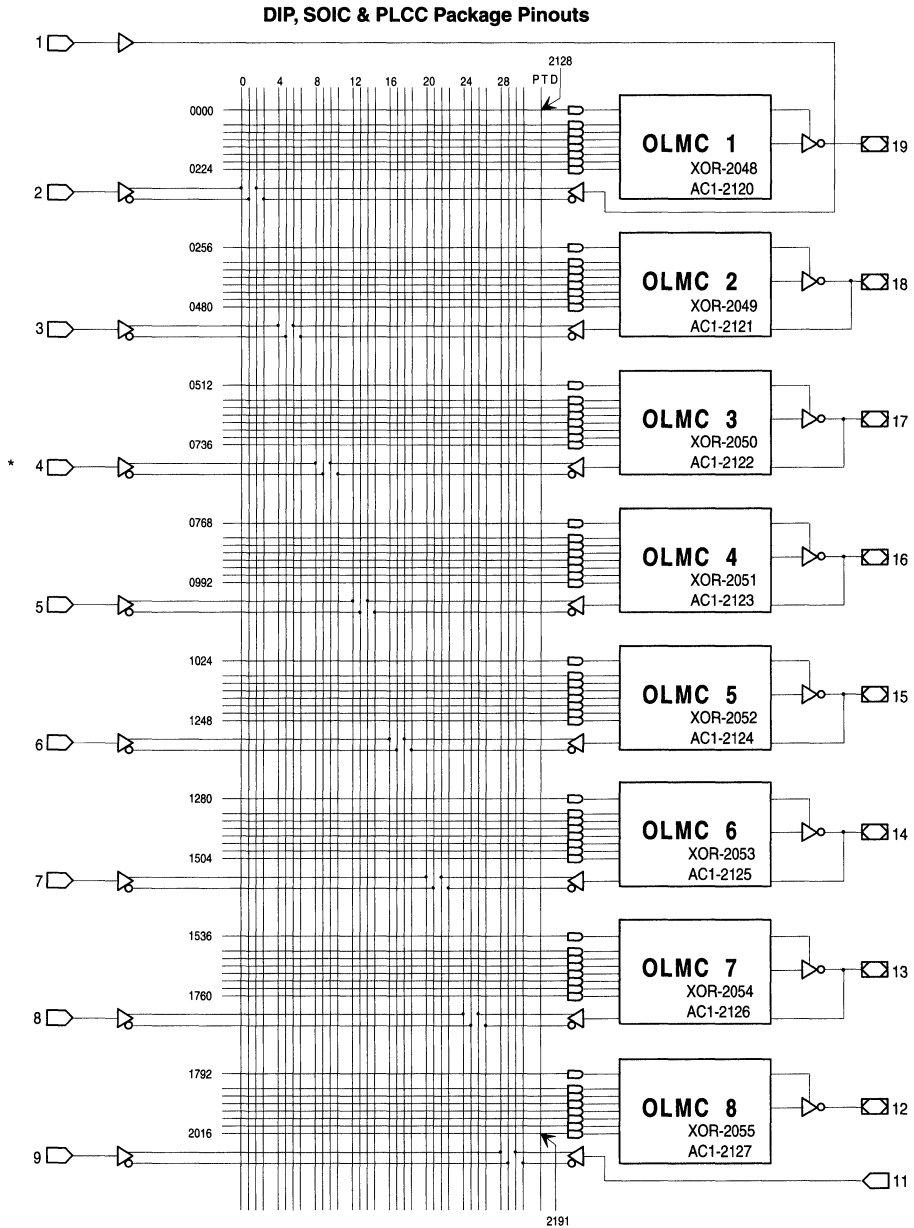
The diagram shows a macrocell with four inputs on the left. The top three inputs go to an OR gate. The bottom input goes to an AND gate. The output of the AND gate is labeled 'XOR'. The output of the OR gate goes to an AND gate. The output of this AND gate goes to an inverter. The output of the inverter goes to a multiplexer. The output of the multiplexer goes to an output pin.

Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES
 2056, 2057, 2118, 2119
 Byte7 Byte6 Byte1 Byte0

SYN-2192
AC0-2193

MSB LSB

* Note: Input not available on GAL16V8ZD

SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used in the input configuration.

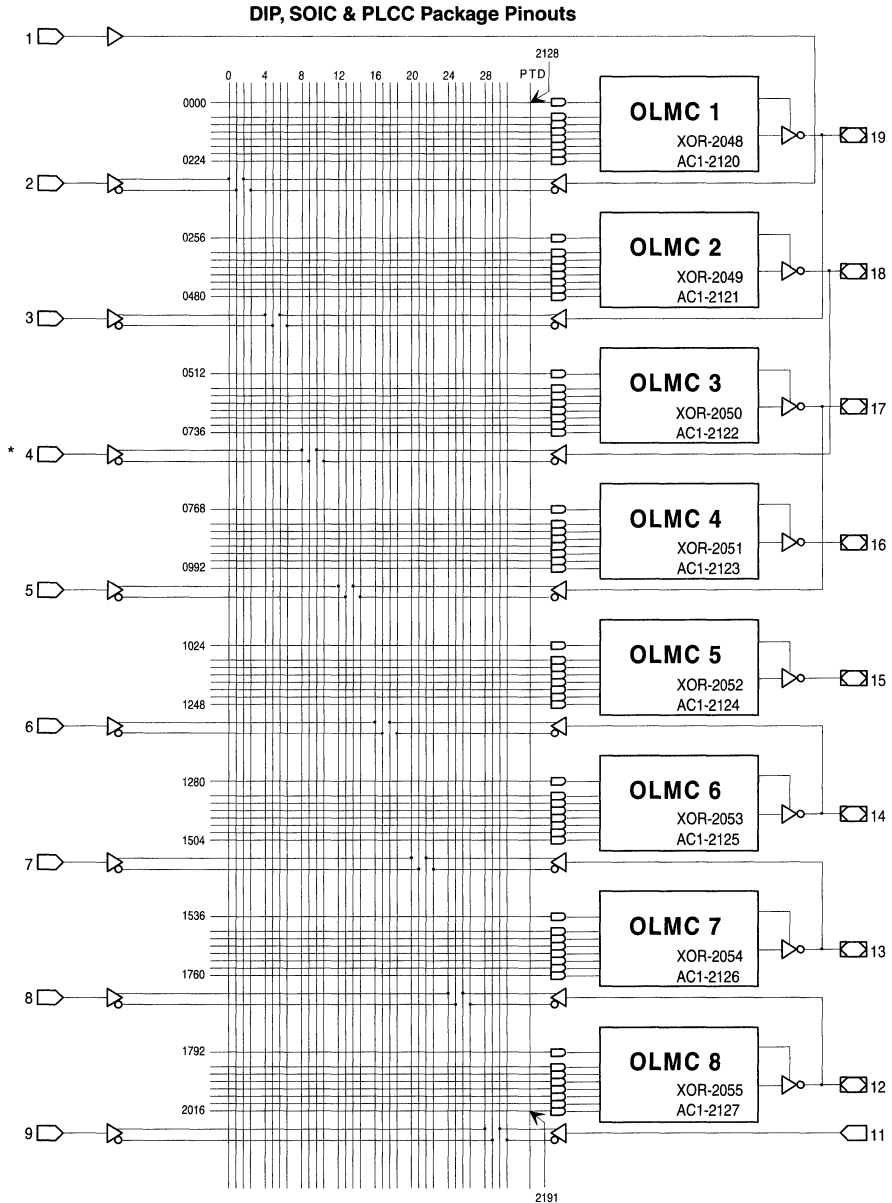
Pin 4 is used as dedicated power-down pin on GAL16V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - All OLMC except pins 15 & 16 can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - Pins 15 & 16 are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - All OLMC except pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES
 2056, 2057, 2118, 2119
 Byte7 | Byte6 | Byte1 | Byte0

SYN-2192
AC0-2193

MSB LSB

* Note: Input not available on GAL16V8ZD

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
 Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
		$I_{OH} = -100 \mu A V_{IN} = V_{IL} \text{ or } V_{IH}$	$V_{CC} - 1$	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}'	Output Short Circuit Current	$V_{CC} = 5V V_{OUT} = 0.5V T_A = 25^\circ C$	-30	—	-150	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	$V_{IL} = GND V_{IH} = V_{CC}$ Outputs Open	Z-12/-15 ZD-12/-15	—	50	100	μA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V V_{IH} = 3.0V$ $f_{toggle} = 15 \text{ MHz}$ Outputs Open	Z-12/-15 ZD-12/-15	—	—	55	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_I = 2.0V$
$C_{I/O}$	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

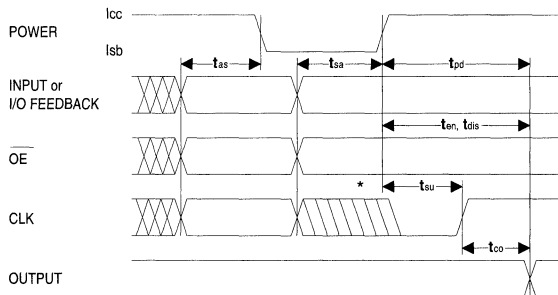
Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
			t_{pd}	A	Input or I/O to Combinational Output	3	
t_{co}	A	Clock to Output Delay	2	8	2	10	ns
t_{cf}²	—	Clock to Feedback Delay	—	6	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	OE to Output Enabled	—	12	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	OE to Output Disabled	—	12	—	15	ns
t_{as}	—	Last Active Input to Standby	60	140	50	150	ns
t_{sa}⁴	—	Standby to Active Output	6	13	5	15	ns

3

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.
- 3) Refer to **f_{max} Specification** section.
- 4) Add t_{sa} to t_{pd}, t_{su}, t_{en} and t_{dis} when the device is coming out of standby state.

STANDBY POWER TIMING WAVEFORMS



* Note: Rising clock edges are allowed during t_{sa} but outputs are not guaranteed.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		COM		UNITS
			-12		-15		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	3	12	3	15	ns
t_{co}	A	Clock to Output Delay	2	8	2	10	ns
t_{cf}²	—	Clock to Feedback Delay	—	6	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock [↑]	10	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock [↑]	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	\overline{OE} to Output Enabled	—	12	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	\overline{OE} to Output Disabled	—	12	—	15	ns

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.
- 3) Refer to **f_{max} Specification** section.

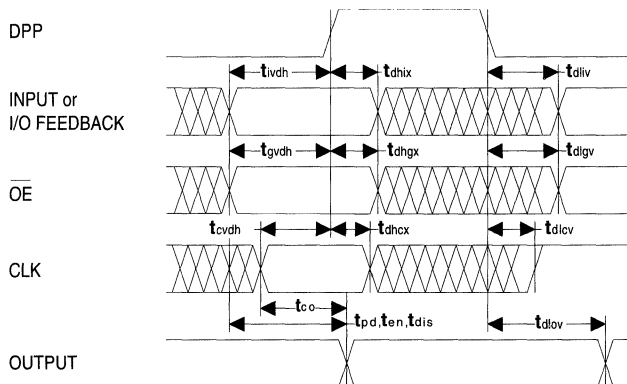
DEDICATED POWER-DOWN PIN SPECIFICATIONS

Over Recommended Operating Conditions

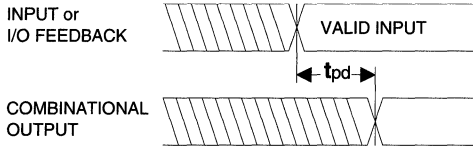
PARAMETER	TEST COND ¹ .	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
			t_{whd}	—	DPP Pulse Duration High	12	
t_{wld}	—	DPP Pulse Duration Low	25	—	30	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	5	—	8	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	2	—	5	ns
t_{dhgx}	—	\overline{OE} Don't Care after DPP High	—	6	—	9	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	8	—	11	ns
STANDBY TO ACTIVE							
t_{dliv}	—	DPP Low to Valid Input	12	—	15	—	ns
t_{dlgv}	—	DPP Low to Valid \overline{OE}	16	—	20	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	18	—	20	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	24	5	30	ns

1) Refer to **Switching Test Conditions** section.

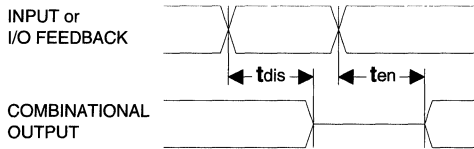
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



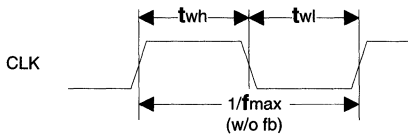
SWITCHING WAVEFORMS



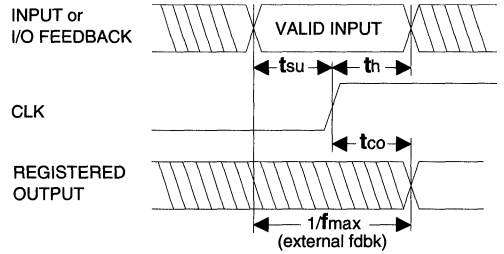
Combinatorial Output



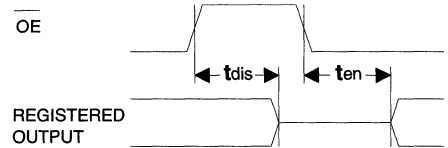
Input or I/O to Output Enable/Disable



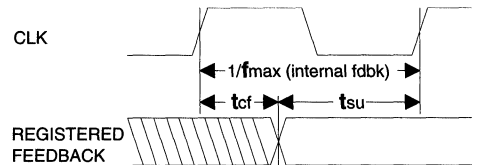
Clock Width



Registered Output

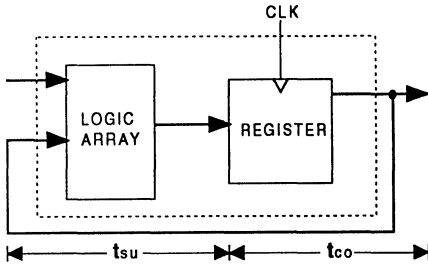


OE to Output Enable/Disable



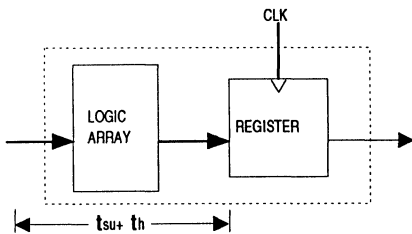
fmax with Feedback

f_{max} SPECIFICATIONS



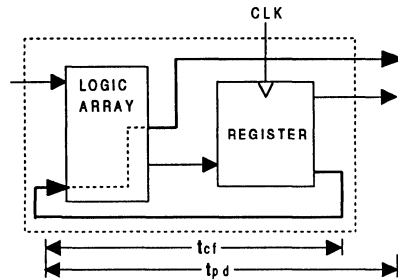
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

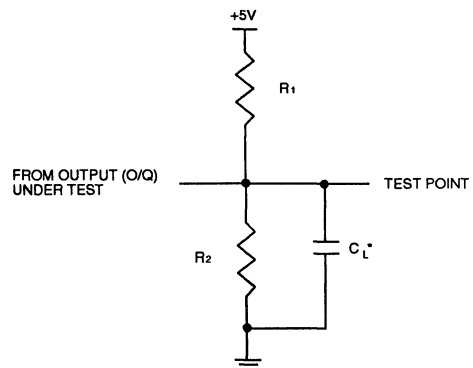
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R1	R2	CL
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	5pF
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL16V8Z/ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

A security cell is provided in the GAL16V8Z/ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the Development Tools Section of the Data Book). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

INPUT TRANSITION DETECTION (ITD)

The GAL16V8Z relies on its internal input detection circuitry to put the device in power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Any valid input transition will put the device back into the active state. The first rising clock transition from power-down state only acts as a wake up signal to the device and will not clock the data input through to the output (refer to standby power timing waveform for more detail). Any input pulse widths greater than 5ns at input voltage level of 1.5V will be detected as input transition. The device will not detect any input pulse widths less than 1ns measured at input voltage level of 1.5V as an input transition.

DEDICATED POWER-DOWN PIN (DPP)

The GAL16V8ZD uses pin 4 as the dedicated power-down signal to put the device in to the power-down state. DPP is an active high signal where a logic high driven on this signal puts the device into power-down state. Input pin 4 cannot be used as a functional input on this device.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

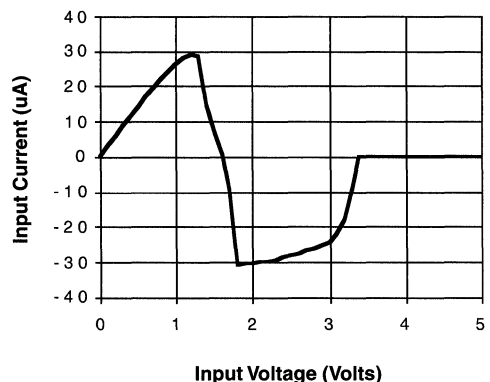
The GAL16V8Z/ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

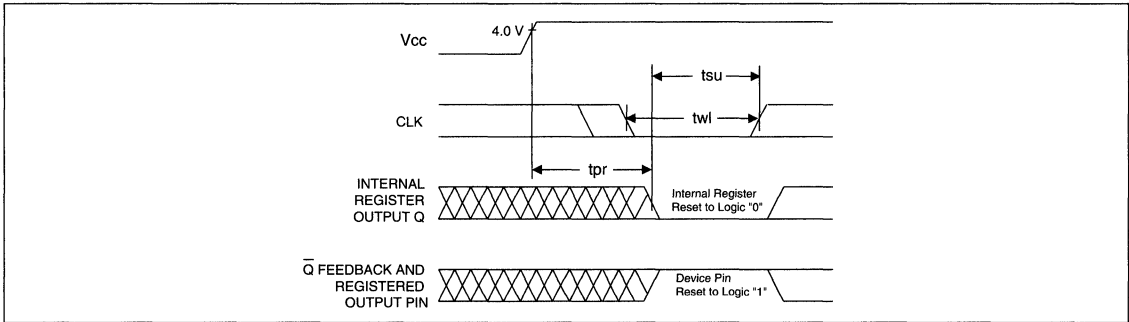
GAL16V8Z/ZD devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL16V8Z/ZD input buffers have latches within the buffers. As a result, when the device goes into standby mode the inputs will be latched to its values prior to standby. In order to overcome the input latches, they will have to be driven by an external source. Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC} , or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Characteristic



POWER-UP RESET

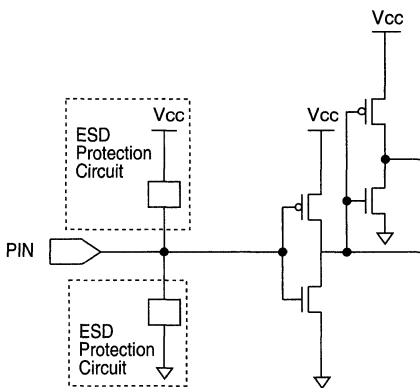
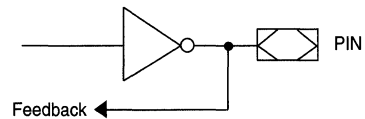
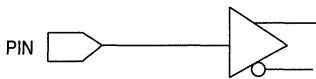


3

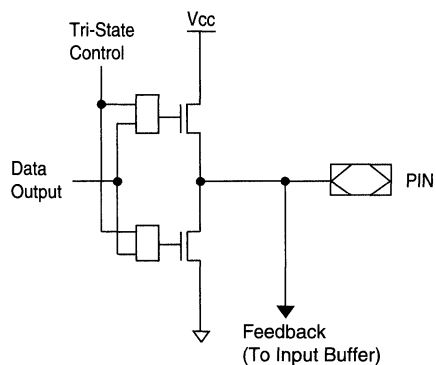
Circuitry within the GAL16V8Z/ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the

asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16V8Z/ZD. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



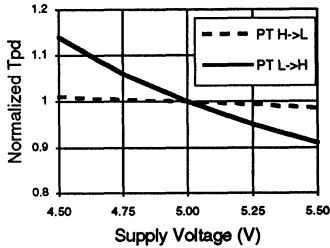
Typical Input



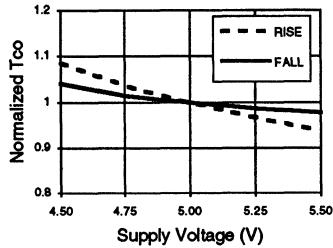
Typical Output

TYPICAL AC AND DC CHARACTERISTICS

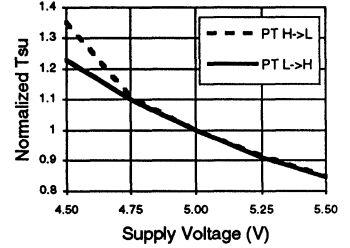
Normalized Tpd vs Vcc



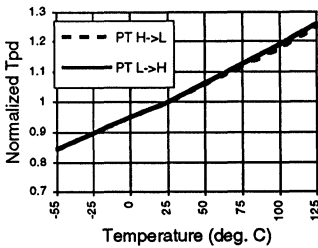
Normalized Tco vs Vcc



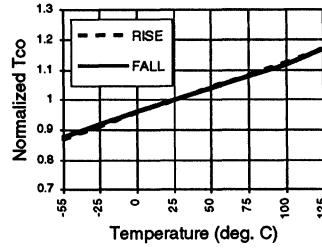
Normalized Tsu vs Vcc



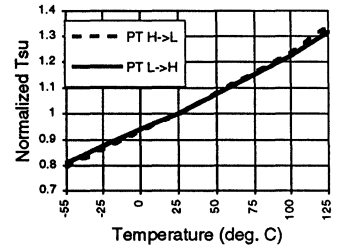
Normalized Tpd vs Temp



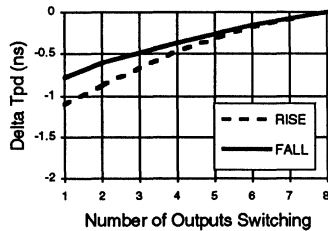
Normalized Tco vs Temp



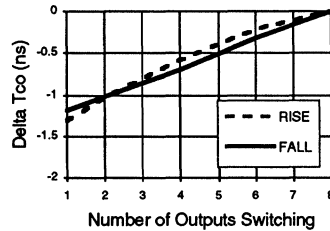
Normalized Tsu vs Temp



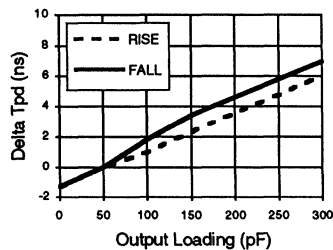
Delta Tpd vs # of Outputs Switching



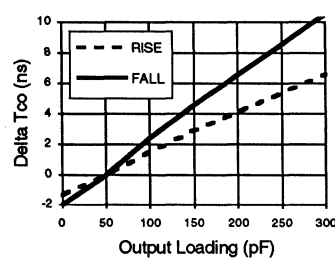
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading



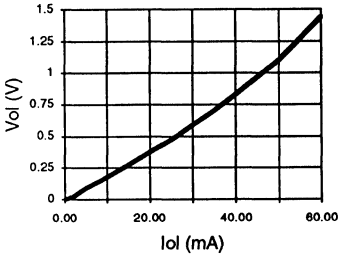
Delta Tco vs Output Loading



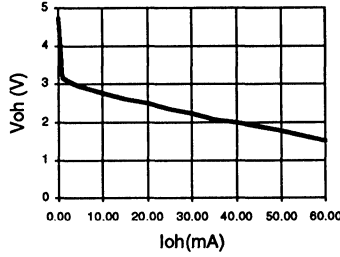
TYPICAL AC AND DC CHARACTERISTICS

3

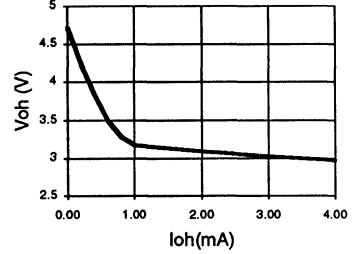
Vol vs Iol



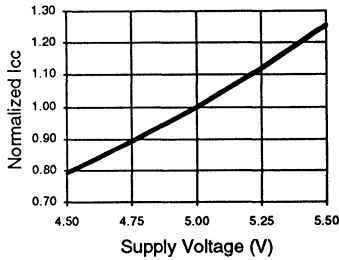
Voh vs Ioh



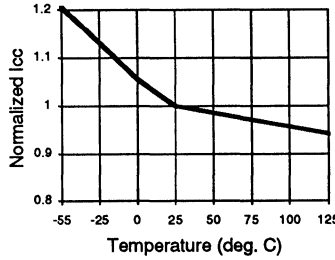
Voh vs Ioh



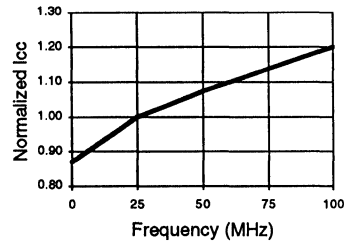
Normalized Icc vs Vcc



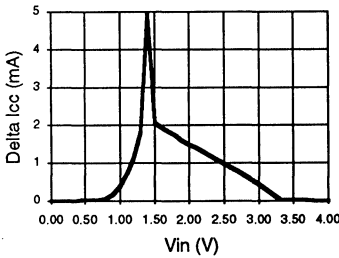
Normalized Icc vs Temp



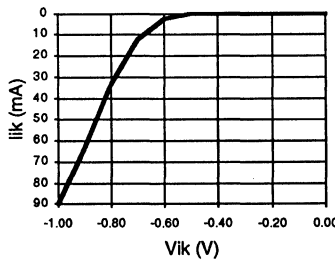
Normalized Icc vs Freq. (DPP & ITD > 10MHz)



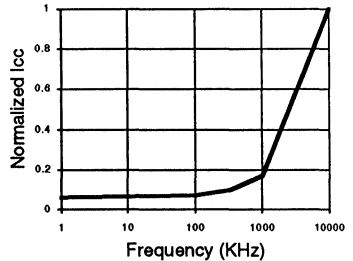
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)



FEATURES

- **HIGH DRIVE E²CMOS® GAL® DEVICE**
 - TTL Compatible 64 mA Output Drive
 - 15 ns Maximum Propagation Delay
 - F_{max} = 80 MHz
 - 10 ns Maximum from Clock Input to Data Output
 - UltraMOS® Advanced CMOS Technology
- **ENHANCED INPUT AND OUTPUT FEATURES**
 - Schmitt Trigger Inputs
 - Programmable Open-Drain or Totem-Pole Outputs
 - Active Pull-Ups on All Inputs and I/O pins
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Architecturally Compatible with Standard GAL16V8
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - Ideal for Bus Control & Bus Arbitration Logic
 - Bus Address Decode Logic
 - Memory Address, Data and Control Circuits
 - DMA Control
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

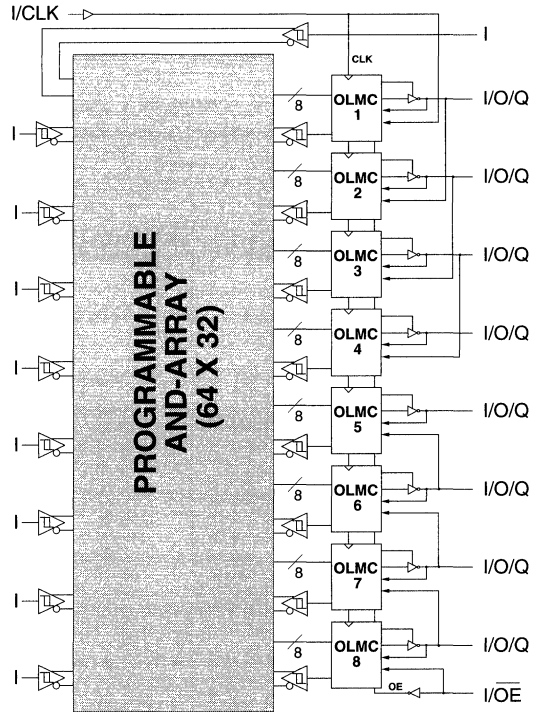
DESCRIPTION

The GAL16VP8, with 64 mA drive capability and 15 ns maximum propagation delay time is ideal for Bus and Memory control applications. The GAL16VP8 is manufactured using Lattice's advanced E²CMOS process which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

System bus and memory interfaces require control logic before driving the bus or memory interface signals. The GAL16VP8 combines the familiar GAL16V8 architecture with bus drivers as its outputs. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The 64mA output drive eliminates the need for additional devices to provide bus driving capability.

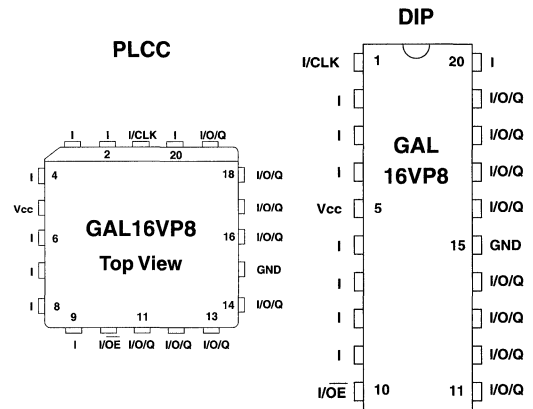
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



3

PIN CONFIGURATION



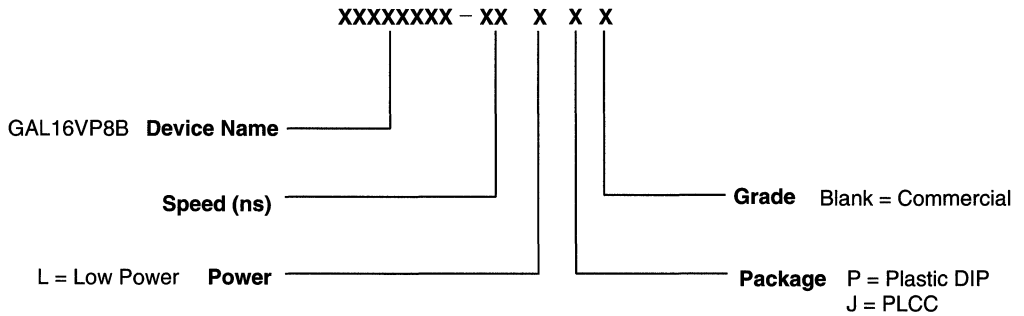
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GAL16VP8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	8	10	115	GAL16VP8B-15LP	20-Pin Plastic DIP
			115	GAL16VP8B-15LJ	20-Lead PLCC
25	10	15	115	GAL16VP8B-25LP	20-Pin Plastic DIP
			115	GAL16VP8B-25LJ	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in

any of the three modes, while the AC1 and AC2 bit of each of the macrocells controls the input/output and totem-pole/open-drain configuration. These two global and 24 individual architecture bits define all possible configurations in a GAL16VP8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

3

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 10 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 10 become dedicated inputs and use the feedback paths of pin 19 and pin 11 respectively. Because of this feedback path usage, pin 19 and pin 11 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 14 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

In addition to the architecture configurations, the logic compiler software also supports configuration of either totem-pole or open-drain outputs. The actual architecture bit configuration, again, is transparent to the user with the default configuration being the standard totem-pole output.

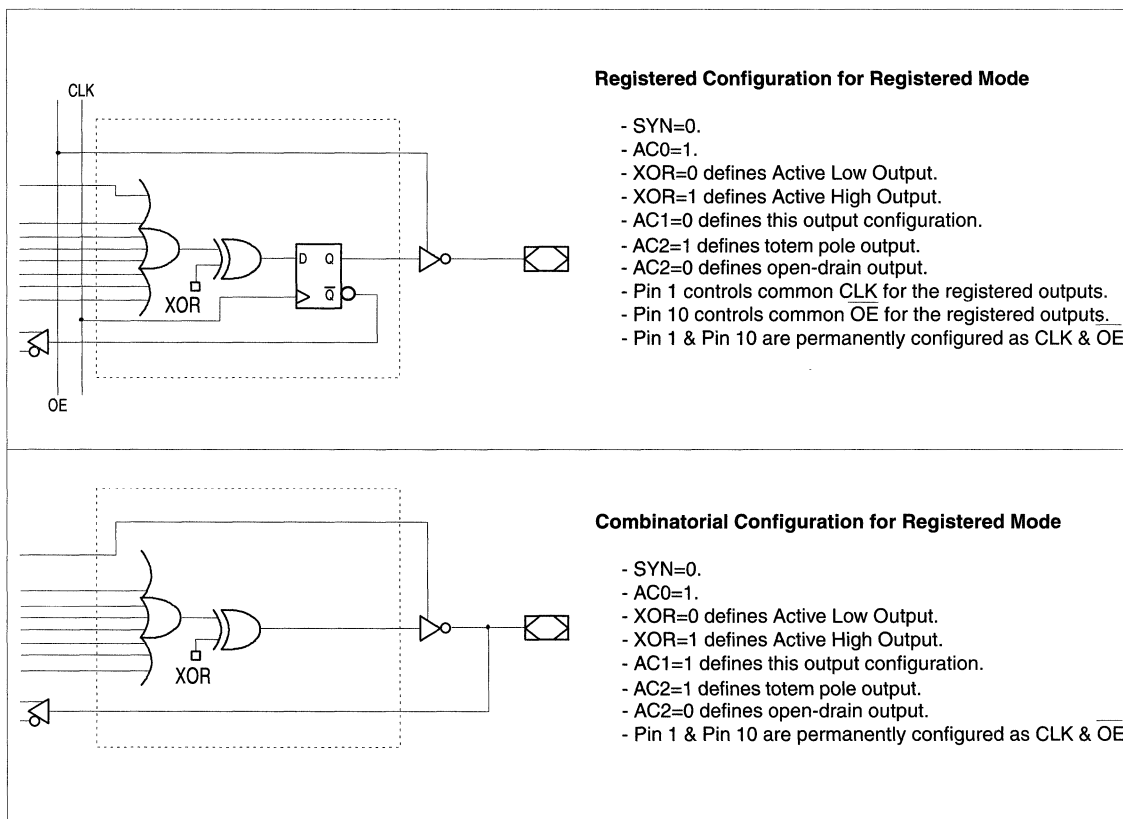
REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

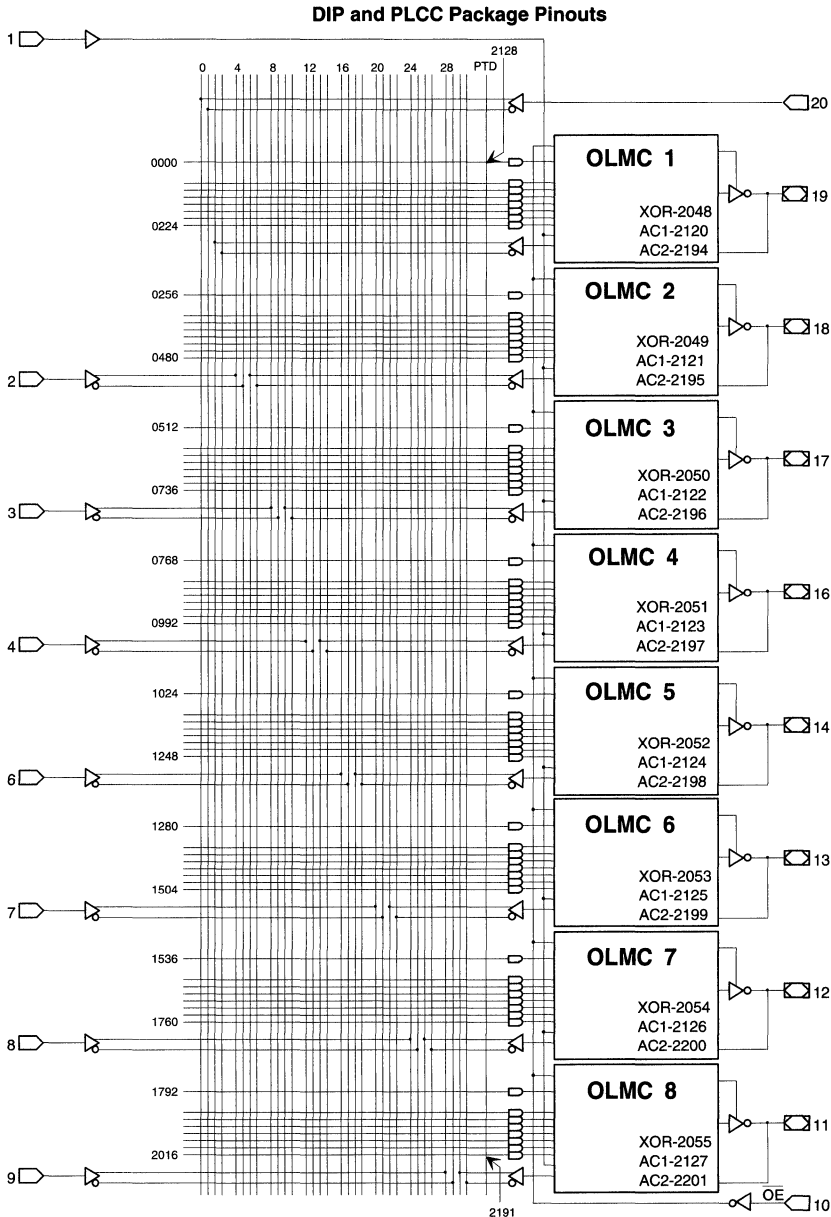
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2055, 2118, 2119
Byte7 Byte6 Byte1 Byte0

SYN-2192
AC0-2193

MSB — — LSB

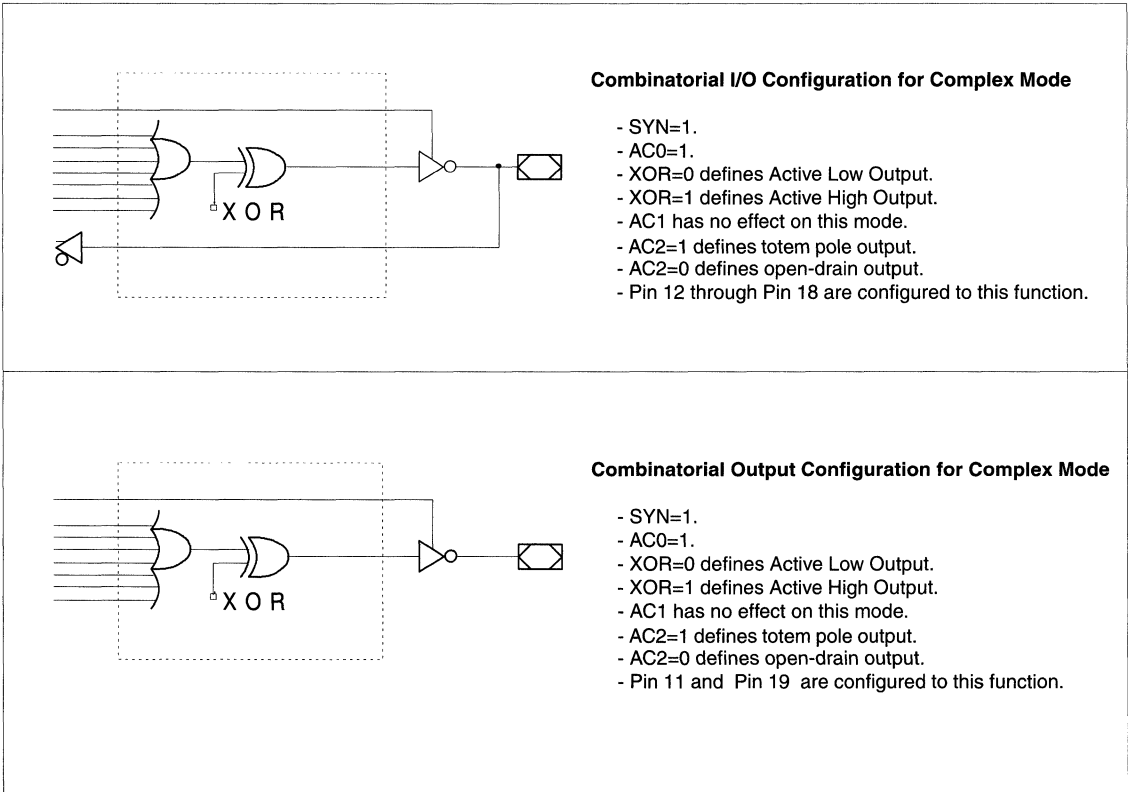
COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 11 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

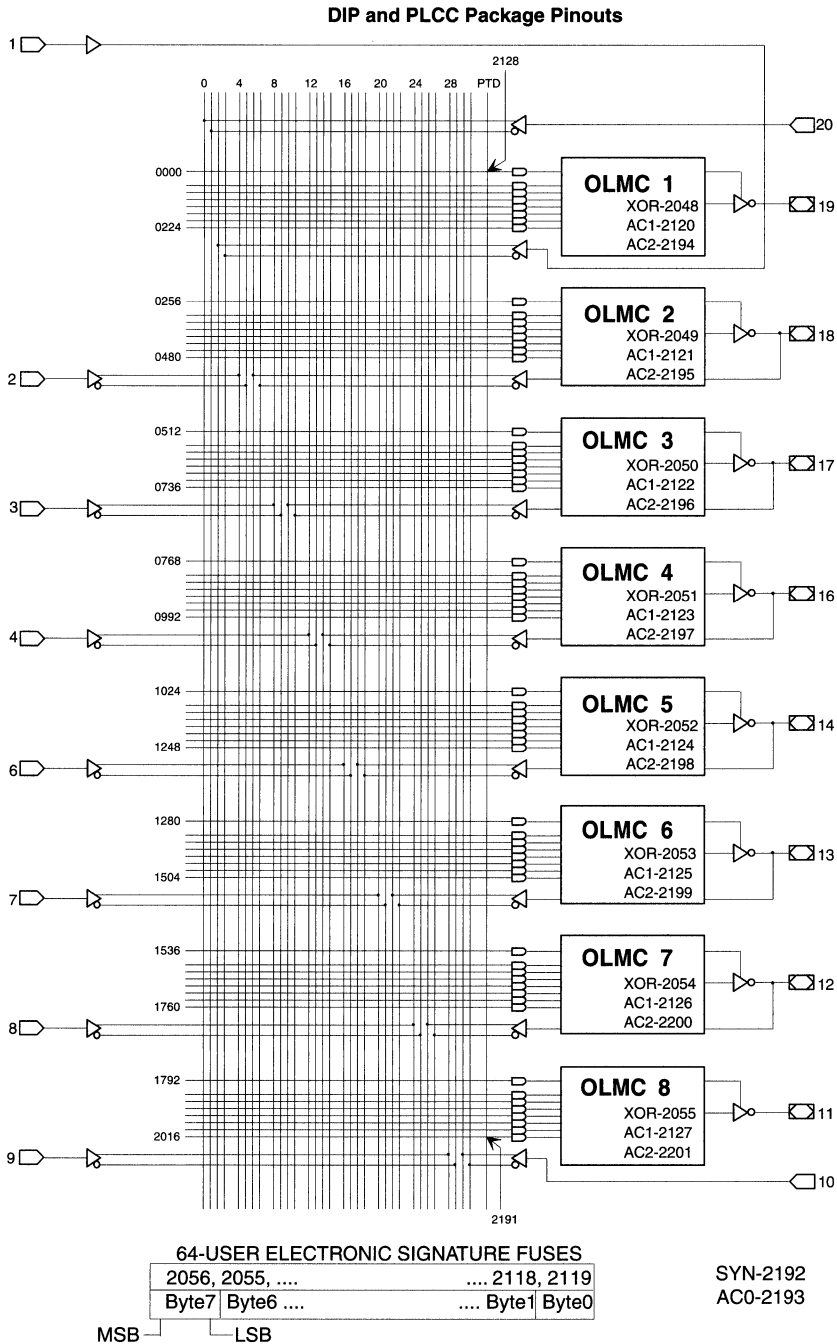
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 10 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM



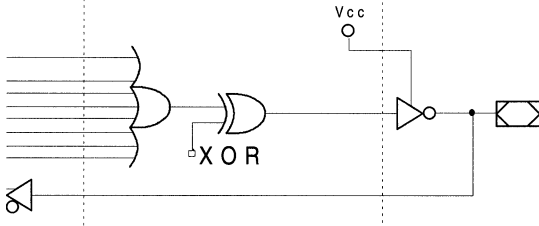
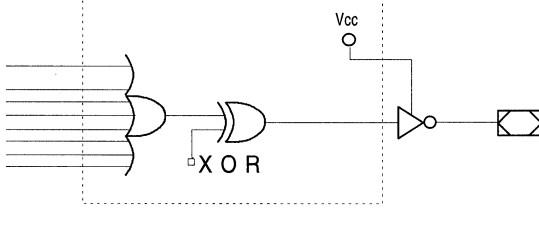
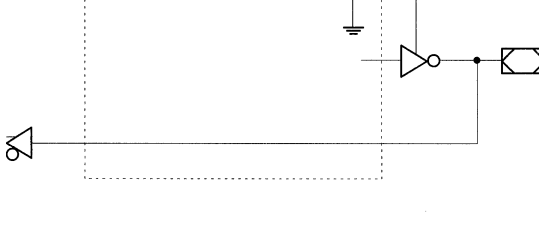
SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

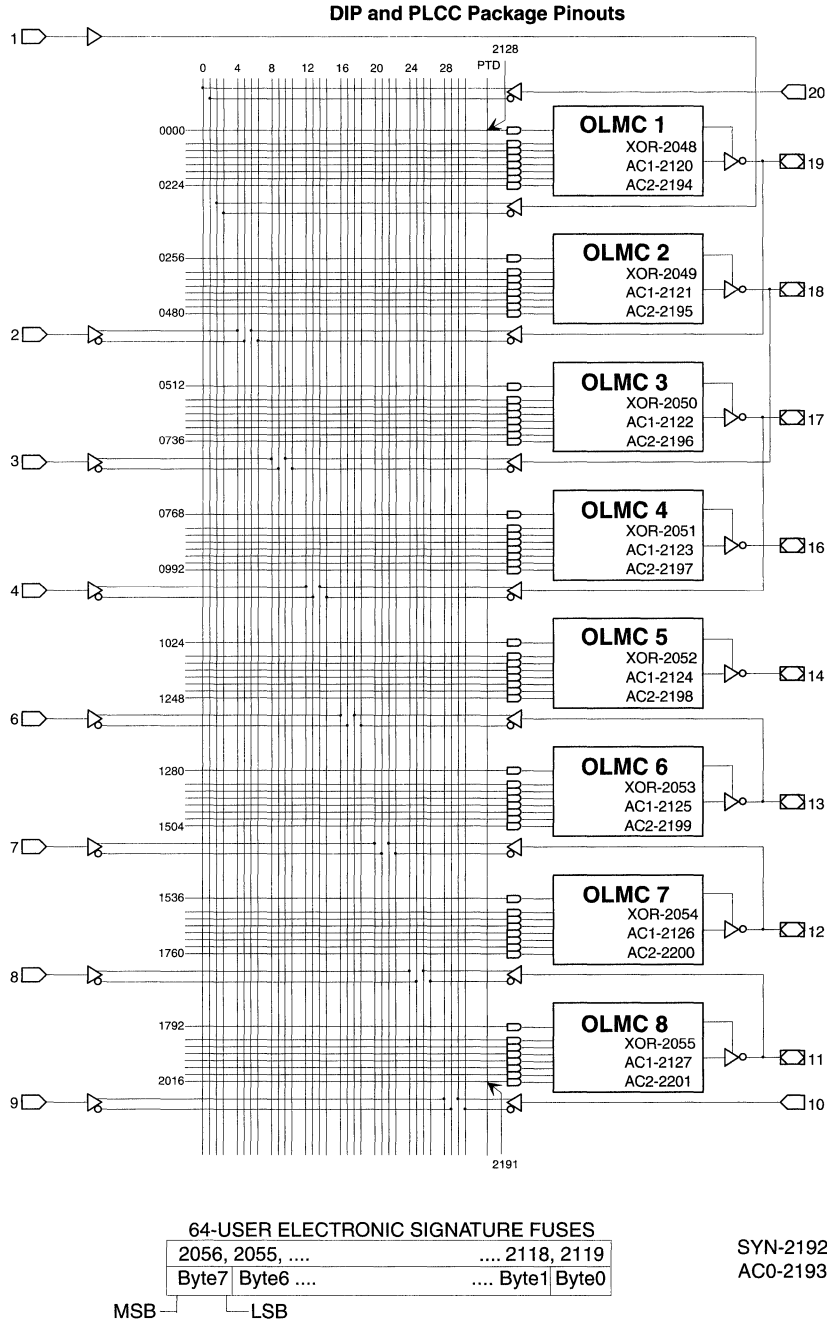
Pins 1 and 10 are always available as data inputs into the AND array. The center two macrocells (pins 14 & 16) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - AC2=1 defines totem pole output. - AC2=0 defines open-drain output. - All OLMC except pins 14 & 16 can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - AC2=1 defines totem pole output. - AC2=0 defines open-drain output. - Pins 14 & 16 are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - AC2=1 defines totem pole output. - AC2=0 defines open-drain output. - All OLMC except pins 14 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM



3

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ⁴	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
V_I^1	Input Clamp Voltage	$V_{CC} = \text{Min. } I_{IN} = -32\text{mA}$	—		-1.2	V
I_{IL}^2	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (\text{MAX.})$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = \text{MAX. } V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = \text{MAX. } V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	64	mA
I_{OH}	High Level Output Current		—	—	-32	mA
I_{OS}^3	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ\text{C}$	-60	—	-400	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{\text{toggle}} = 15\text{MHz}$ Outputs Open	L -15/-25	—	90	115	mA
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1) Guaranteed but not 100% tested.

2) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

3) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.

4) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		COM		UNITS
			-15		-25		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	3	15	3	25	ns
t_{co}	A	Clock to Output Delay	2	10	2	15	ns
t_{cf}²	—	Clock to Feedback Delay	—	4.5	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	8	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	55.5	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	80	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	80	—	50	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	10	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	10	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	ns
	B	$\overline{\text{OE}}$ to Output Enabled	—	12	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	ns
	C	$\overline{\text{OE}}$ to Output Disabled	—	12	—	15	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from **f_{max}** with internal feedback. Refer to **f_{max} Specification** section.

 3) Refer to **f_{max} Specification** section.

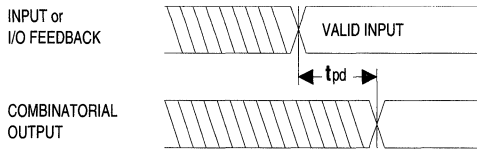
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _i	Input Capacitance	10	pF	V _{cc} = 5.0V, V _i = 2.0V
C _{i/o}	I/O Capacitance	15	pF	V _{cc} = 5.0V, V _{i/o} = 2.0V

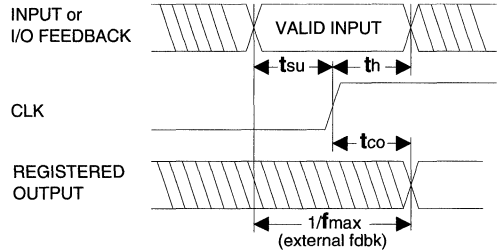
*Guaranteed but not 100% tested.

3

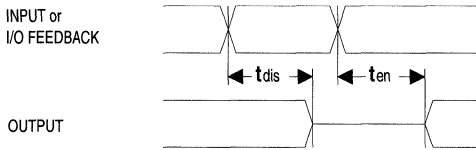
SWITCHING WAVEFORMS



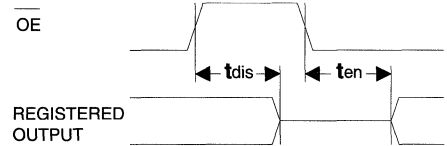
Combinatorial Output



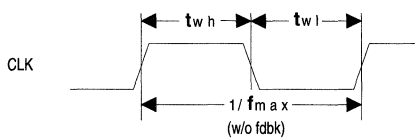
Registered Output



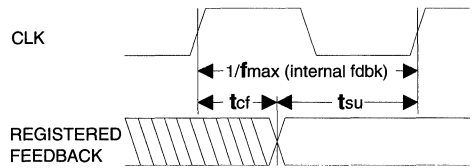
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

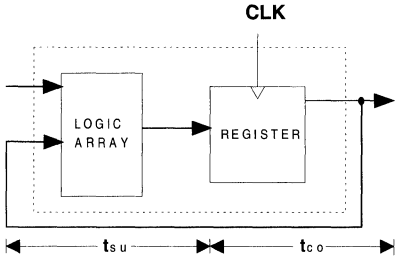


Clock Width



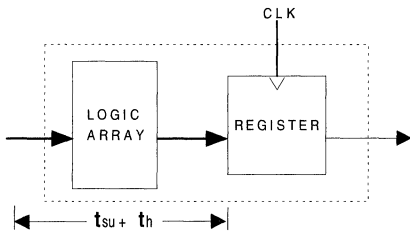
f_{max} with Feedback

f_{max} DESCRIPTIONS



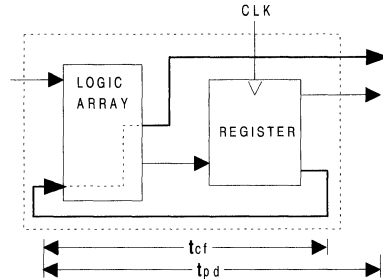
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to t_{cf} + t_{pd}.

3

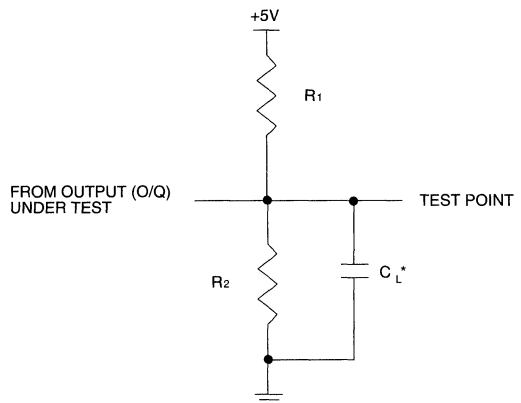
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	500Ω	500Ω	50pF
B	Active High	∞	500Ω
	Active Low	500Ω	500Ω
C	Active High	∞	500Ω
	Active Low	500Ω	500Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL16VP8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

The security cell is provided on all GAL16VP8 devices to prevent unauthorized copying of the array patterns. Once programmed, the circuitry enabling array is disabled, preventing further programming or verification of the array. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

GAL16VP8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

BULK ERASE MODE

During a programming cycle, a clear function performs a bulk erase of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its original state, which is all JEDEC ones.

SCHMITT TRIGGER INPUTS

One of the enhancements of the GAL16VP8 for bus interface logic implementation is input hysteresis. The threshold of the positive going edge is 1.5V, while the threshold of the negative going edge is 1.3V. This provides a typical hysteresis of 200mV between positive and negative transitions of the inputs.

HIGH DRIVE OUTPUTS

All eight outputs of the GAL16VP8 are capable of driving 64 mA loads when driving low and 32 mA loads when driving high. Near symmetrical high and low output drive capability provides small skews between high-to-low and low-to-high output transitions.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

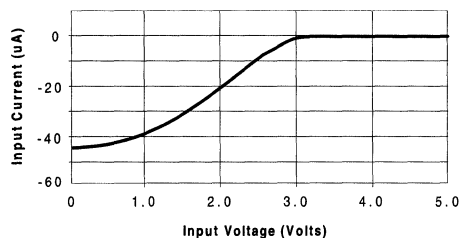
The GAL16VP8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors can perform output register preload automatically.

INPUT BUFFERS

GAL16VP8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL16VP8 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC} , or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

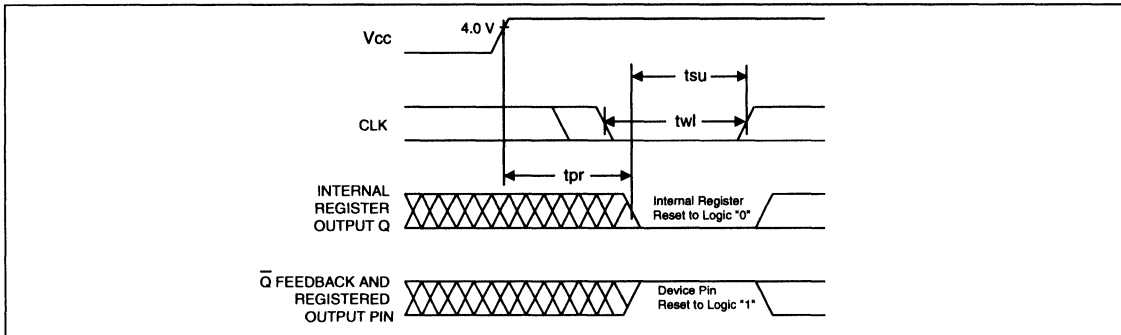
Typical Input Pull-up Characteristic



PROGRAMMABLE OPEN-DRAIN OUTPUTS

In addition to the standard GAL16V8 type configuration, the outputs of the GAL16VP8 are individually programmable either as a standard totempole output or an open-drain output. The totempole output drives the specified V_{OH} and V_{OL} levels whereas the open-drain output drives only the specified V_{OL} . The V_{OH} level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by the AC2 fuse. When AC2 cell is erased (JEDEC "1") the output is configured as a totempole output and when AC2 cell is programmed (JEDEC "0") the output is configured as an open-drain. The default configuration when the device is in bulk erased state is totempole configuration. The AC2 fuses associated with each of the outputs is included in all of the logic diagrams.

POWER-UP RESET

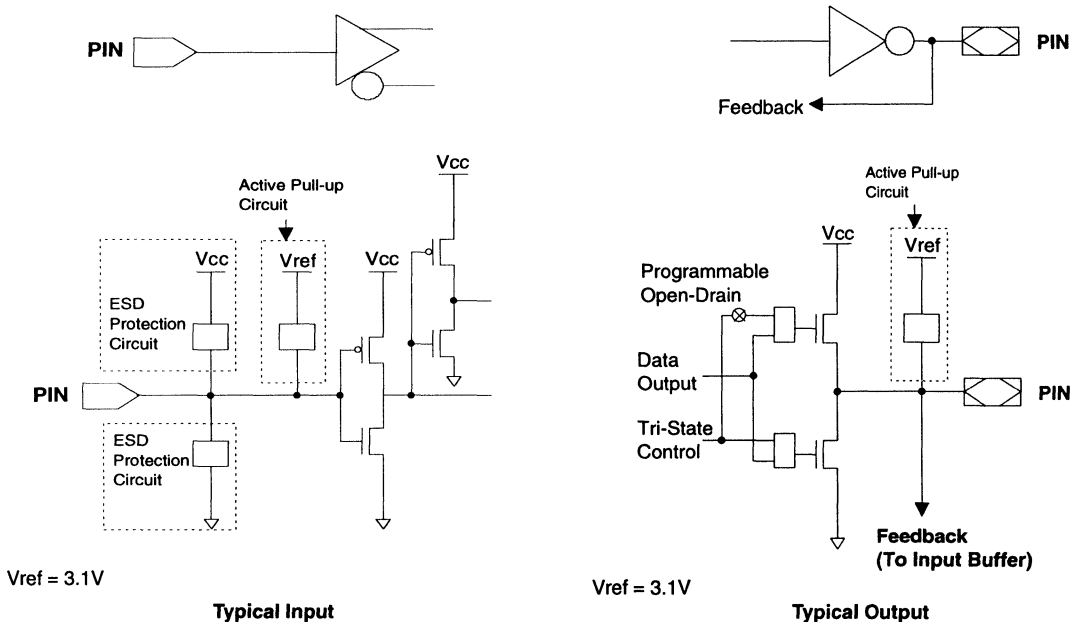


3

Circuitry within the GAL16VP8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown above. Because of the asynchro-

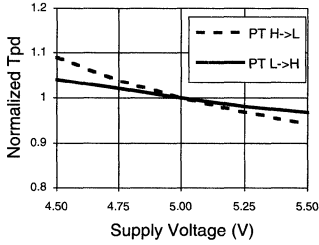
nous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16VP8. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

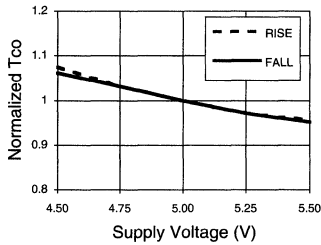


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

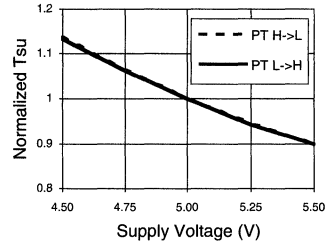
Normalized Tpd vs Vcc



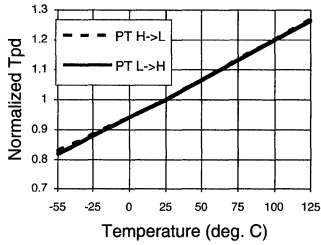
Normalized Tco vs Vcc



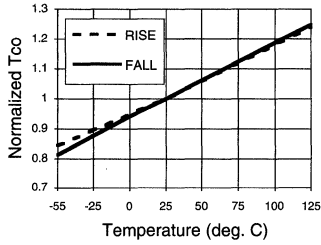
Normalized Tsu vs Vcc



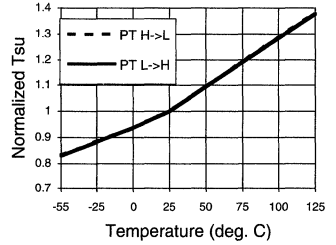
Normalized Tpd vs Temp



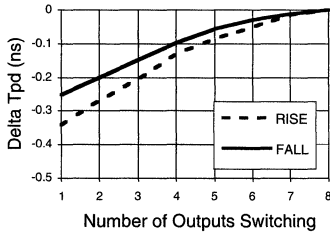
Normalized Tco vs Temp



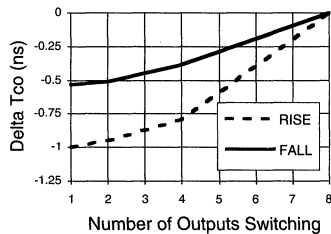
Normalized Tsu vs Temp



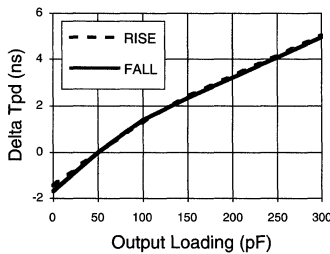
Delta Tpd vs # of Outputs Switching



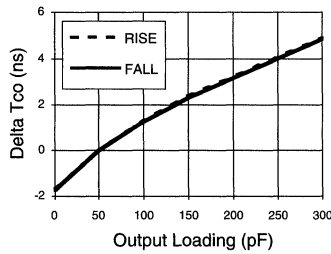
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

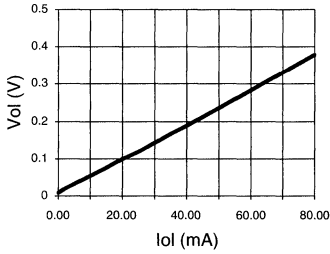


Delta Tco vs Output Loading

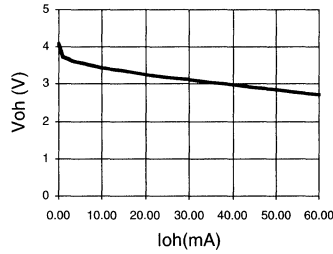


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

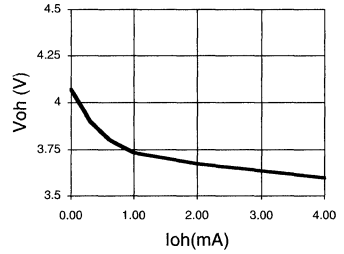
Vol vs Iol



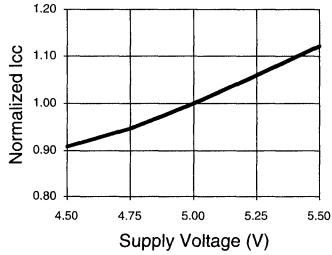
Voh vs Ioh



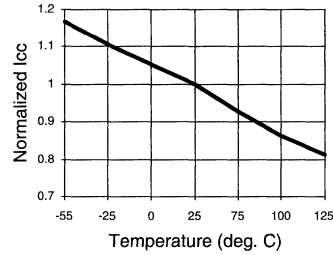
Voh vs Ioh



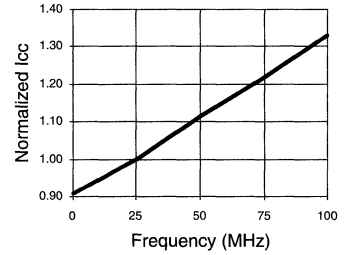
Normalized Icc vs Vcc



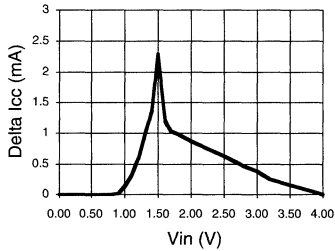
Normalized Icc vs Temp



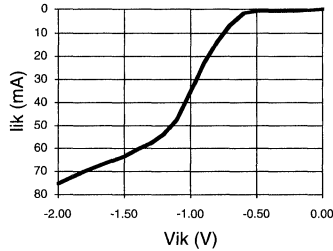
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Iik)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 15 ns Maximum Propagation Delay
 - Fmax = 62.5 MHz
 - 10ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **LOW POWER CMOS**
 - 75 mA Typical Icc
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Uses Standard 22V10 Macrocell Architecture
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

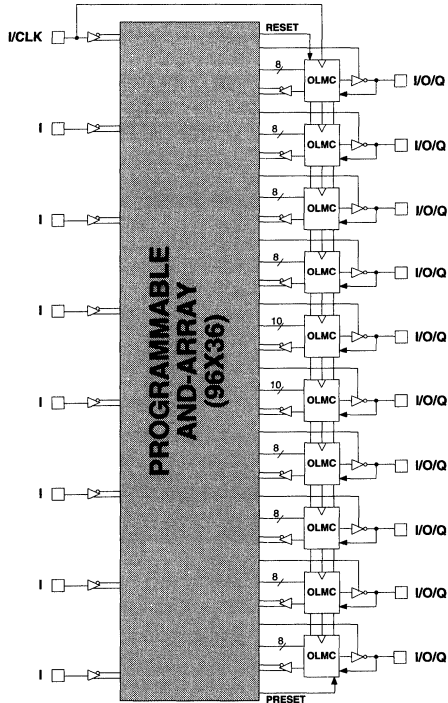
DESCRIPTION

The GAL 18V10, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide a very flexible 20-pin PLD. CMOS circuitry allows the GAL 18V10 to consume much less power when compared to its bipolar counterparts. The E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

By building on the popular 22V10 architecture, the GAL 18V10 eliminates the learning curve usually associated with using a new device architecture. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL 18V10 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

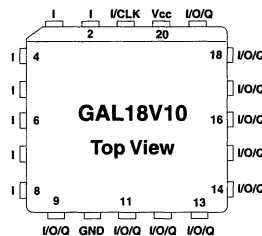
FUNCTIONAL BLOCK DIAGRAM



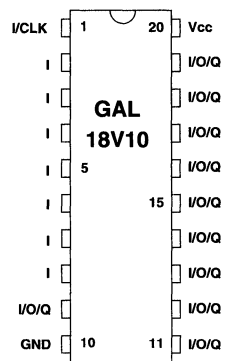
3

PACKAGE DIAGRAMS

PLCC



DIP



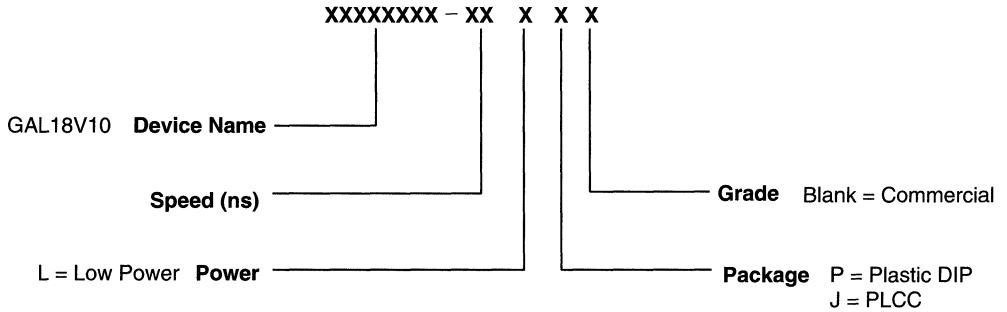
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GAL18V10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	10	115	GAL18V10-15LP	20-Pin Plastic DIP
			115	GAL18V10-15LJ	20-Lead PLCC
20	12	12	115	GAL18V10-20LP	20-Pin Plastic DIP
			115	GAL18V10-20LJ	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

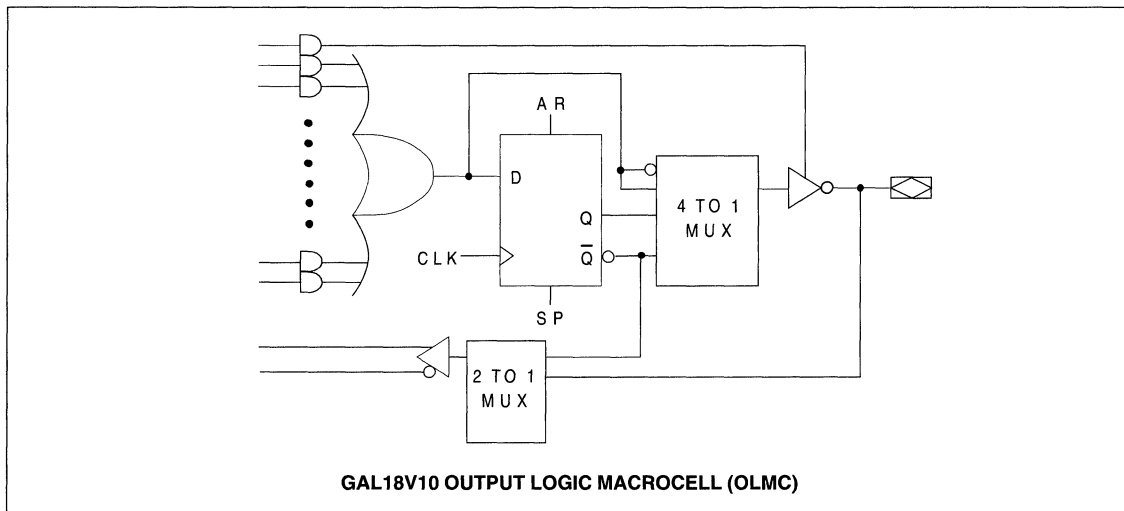
The GAL18V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to ten product terms (pins 14 and 15), and the other eight OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL18V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.

3



OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL18V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

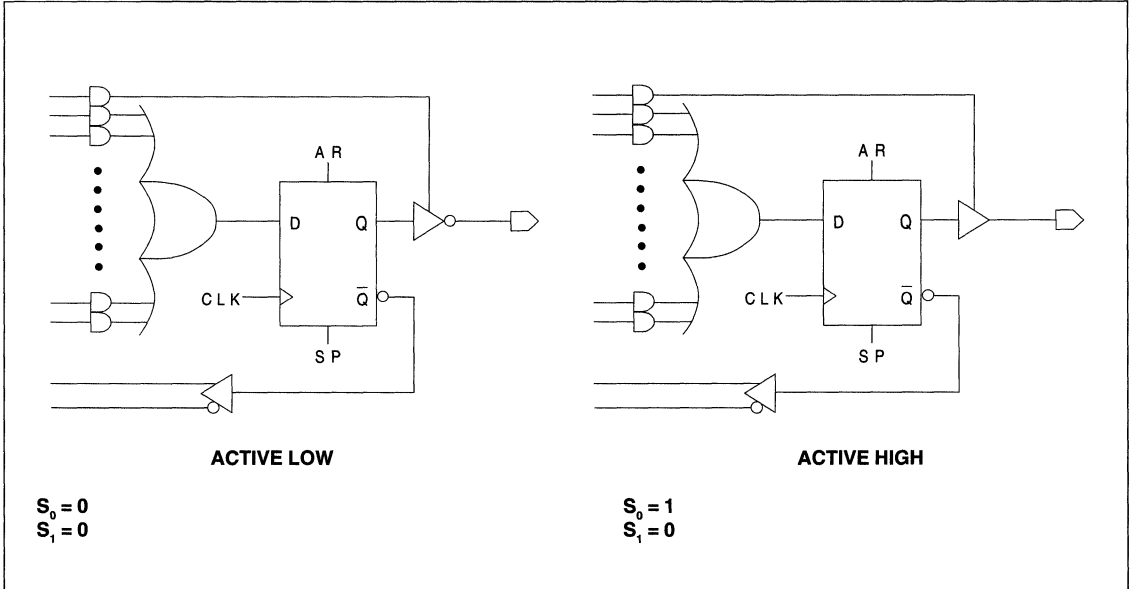
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

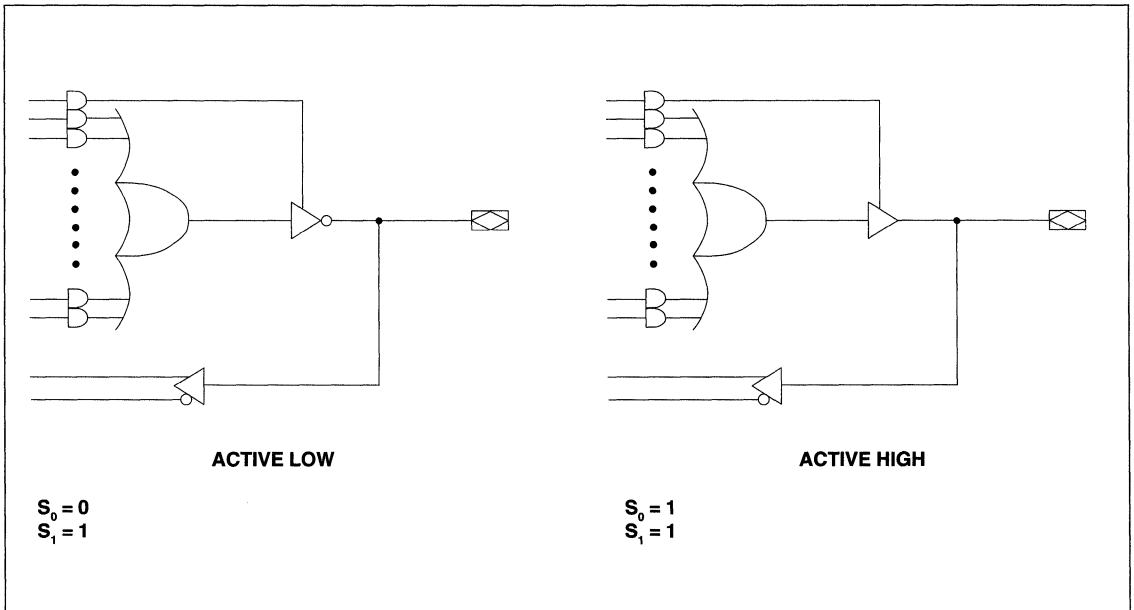
COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE

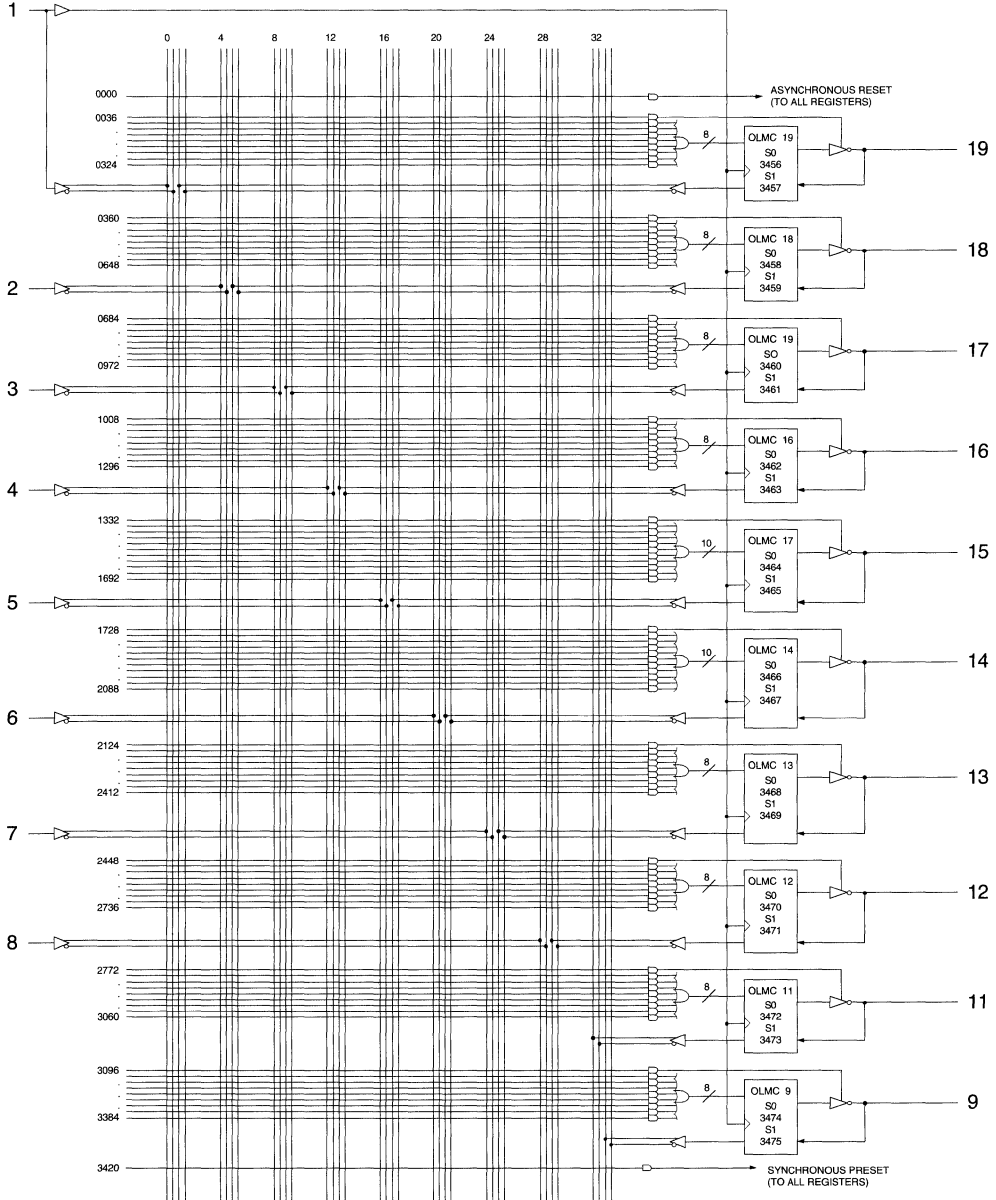


COMBINATORIAL MODE



GAL18V10 LOGIC DIAGRAM / JEDEC FUSE MAP

3



3476, 3477 ...	Electronic Signature	... 3536, 3539					
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
M	L	S	S	B	B	B	B

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \text{ Outputs Open}$	L -15/-20	—	75	115	mA
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- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	COM		COM		UNITS
			-15		-20		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	15	—	20	ns
t_{co}	A	Clock to Output Delay	—	10	—	12	ns
t_{cf}^2	—	Clock to Feedback Delay	—	7	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock \uparrow	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock \uparrow	0	—	0	—	ns
f_{max}^3	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	50	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	58.8	—	45.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	—	20	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	12	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

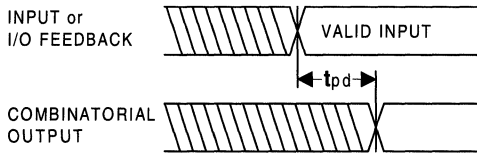
 3) Refer to **f_{max} Description** section.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

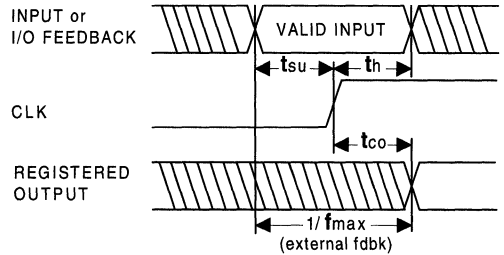
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V$, $V_i = 2.0V$
$C_{i/O}$	I/O Capacitance	10	pF	$V_{CC} = 5.0V$, $V_{i/O} = 2.0V$

*Guaranteed but not 100% tested.

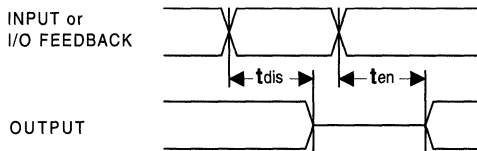
SWITCHING WAVEFORMS



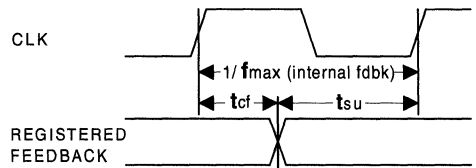
Combinatorial Output



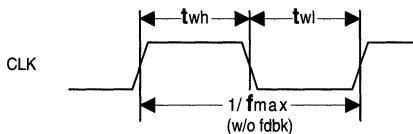
Registered Output



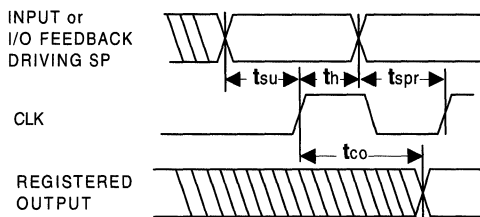
Input or I/O to Output Enable/Disable



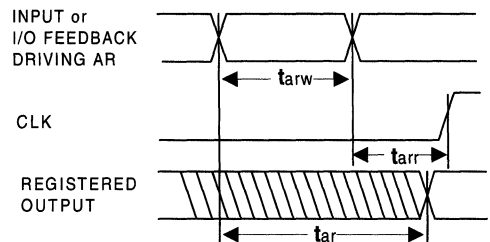
fmax with Feedback



Clock Width

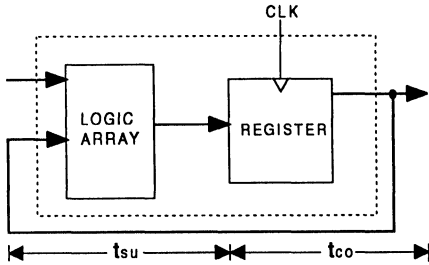


Synchronous Preset



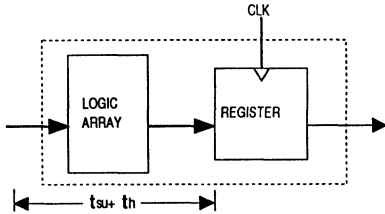
Asynchronous Reset

f_{max} DESCRIPTIONS



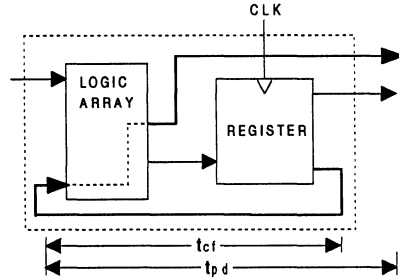
f_{max} with External Feedback $1/(t_{su} + t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su} + t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

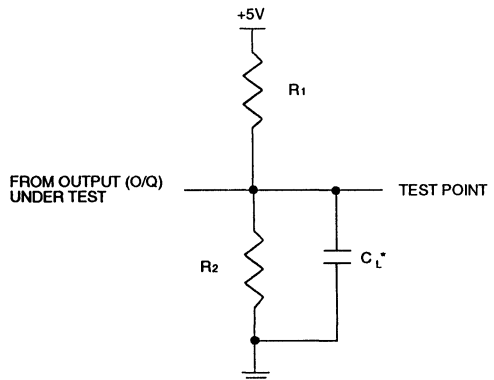
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	390Ω
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL18V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL18V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL18V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

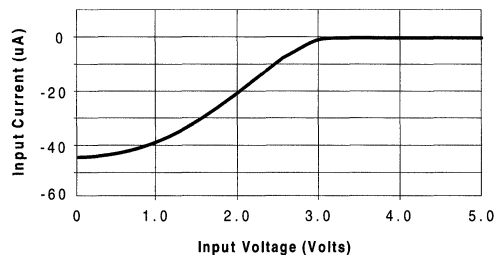
The GAL18V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

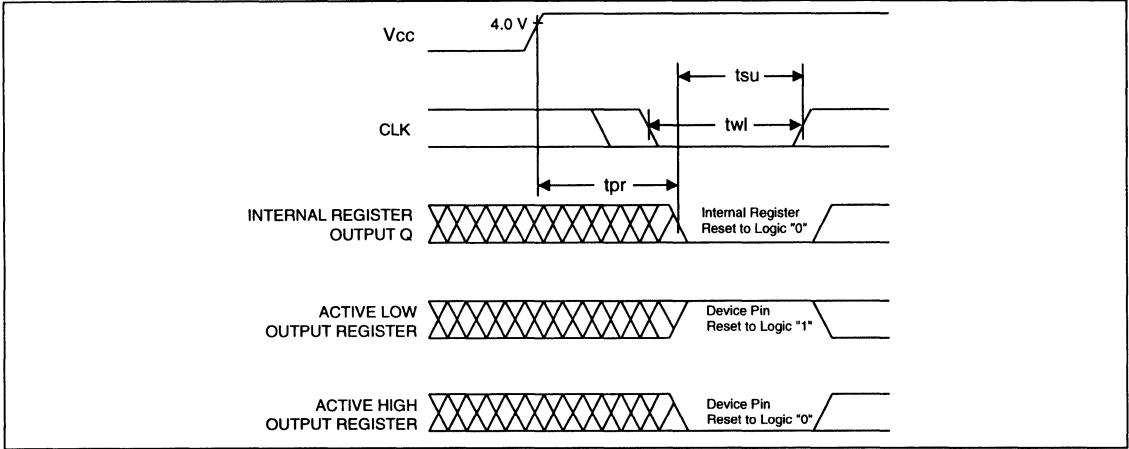
GAL18V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device.

Typical Input Current



POWER-UP RESET

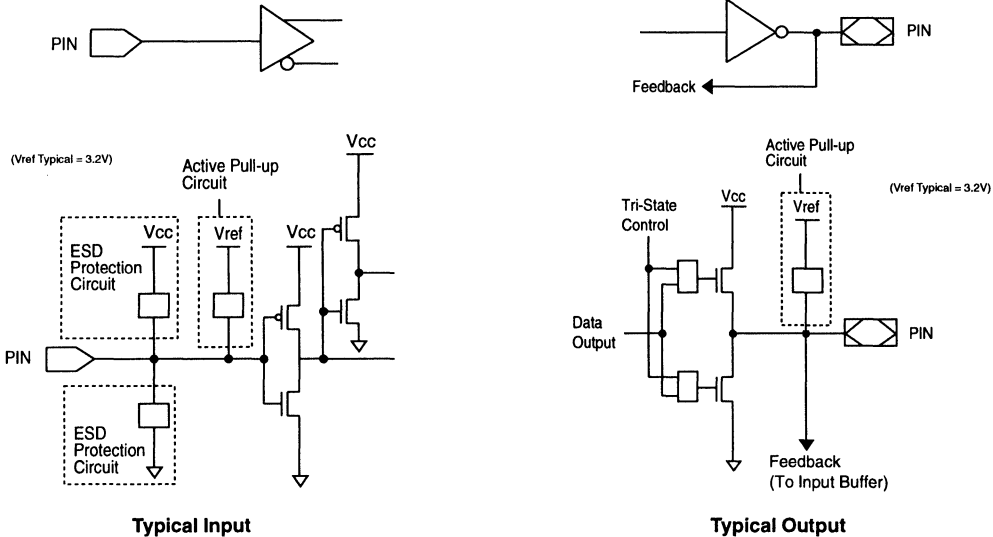


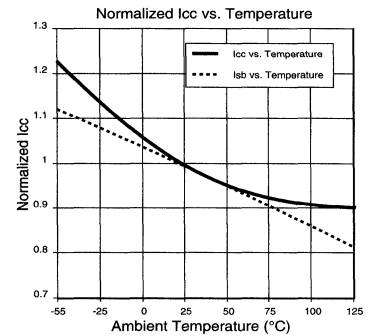
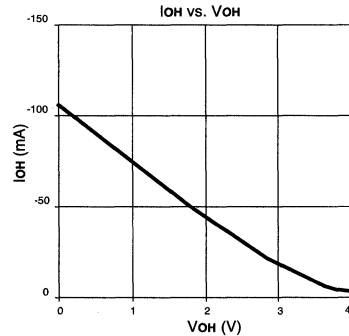
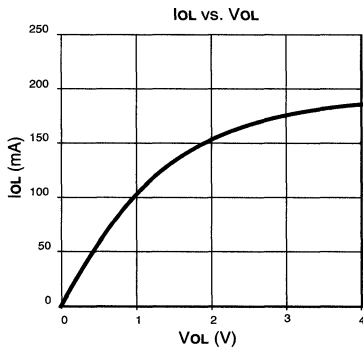
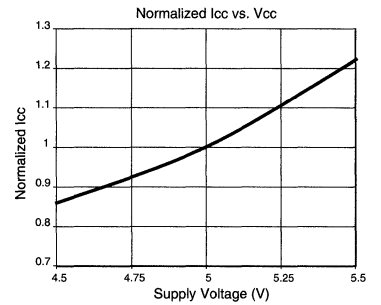
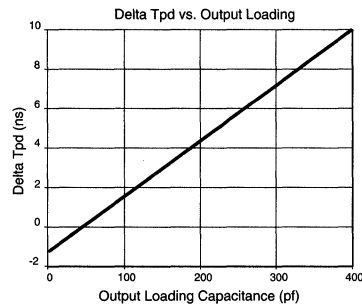
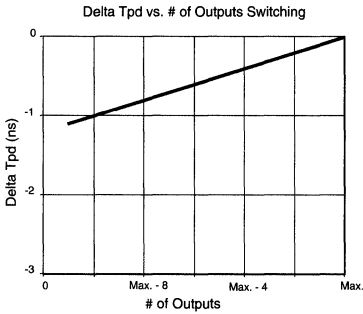
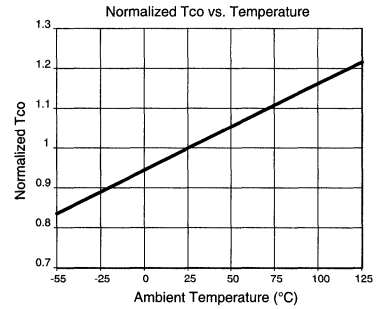
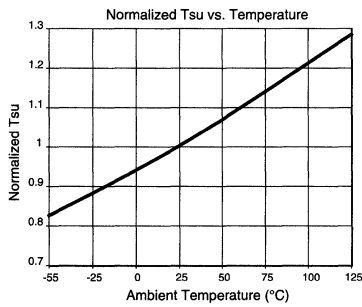
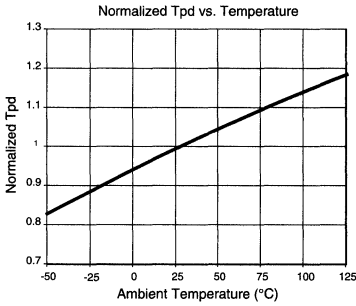
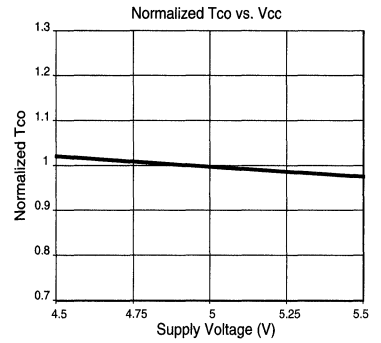
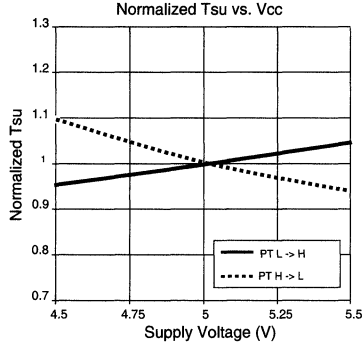
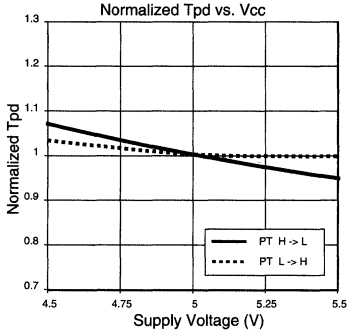
3

Circuitry within the GAL18V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS





FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 10 ns Maximum Propagation Delay
 - $F_{max} = 71.4$ MHz
 - 11 ns Maximum from Clock Input to Data Output
 - TTL Compatible 8 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc}
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erase (<100 ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Independent Programmable Clocks
 - Independent Asynchronous Reset and Preset
 - Registered or Combinatorial with Polarity
 - Full Function and Parametric Compatibility with PAL20RA10
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - State Machine Control
 - Standard Logic Consolidation
 - Multiple Clock Logic Designs
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

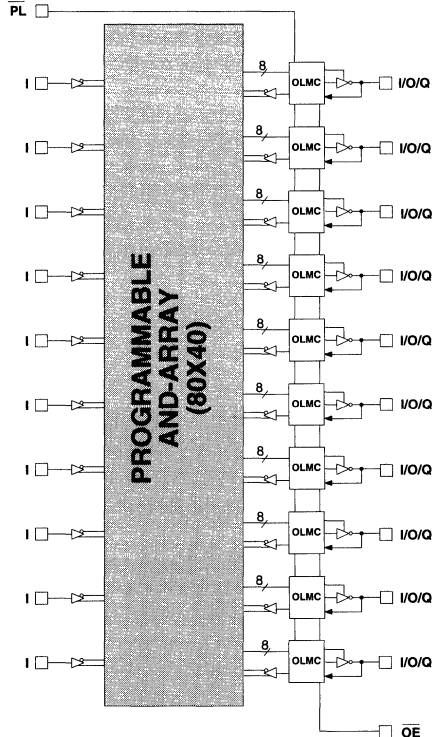
DESCRIPTION

The GAL20RA10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. Lattice's E²CMOS circuitry achieves power levels as low as 75mA typical I_{cc} which represents a substantial savings in power when compared to bipolar counterparts. E² technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

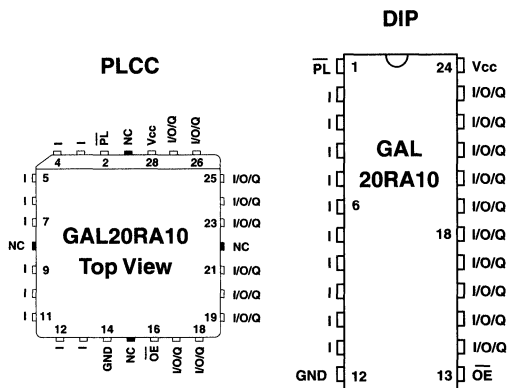
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



3

PIN CONFIGURATION



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GAL20RA10 ORDERING INFORMATION

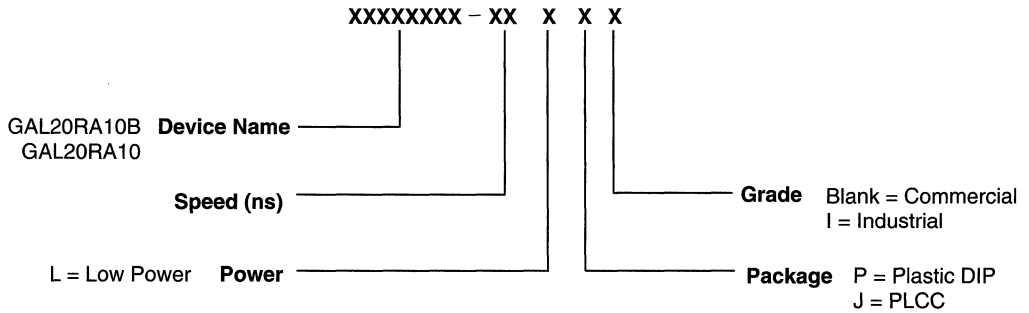
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	4	11	100	GAL20RA10B-10LP	24-Pin Plastic DIP
			100	GAL20RA10B-10LJ	28-Lead PLCC
15	7	15	100	GAL20RA10-15LP	24-Pin Plastic DIP
			100	GAL20RA10-15LJ	28-Lead PLCC
20	10	20	100	GAL20RA10-20LP	24-Pin Plastic DIP
			100	GAL20RA10-20LJ	28-Lead PLCC
30	20	30	100	GAL20RA10-30LP	24-Pin Plastic DIP
			100	GAL20RA10-30LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	10	20	120	GAL20RA10-20LPI	24-Pin Plastic DIP
			120	GAL20RA10-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The GAL20RA10 OLMC consists of 10 D flip-flops with individual asynchronous programmable reset, preset and clock product terms. The sum of four product terms and an Exclusive-OR provide a programmable polarity D-input to each flip-flop. An output enable term combined with the dedicated output enable pin provides tri-state control of each output. Each OLMC has a flip-flop bypass, allowing any combination of registered or combinatorial outputs.

The GAL20RA10 has 10 dedicated input pins and 10 programmable I/O pins, which can be either inputs, outputs, or dynamic I/O. Each pin has a unique path to the logic array. All macrocells have the same type and number of data and control product terms, allowing the user to exchange I/O pin assignments without restriction.

INDEPENDENT PROGRAMMABLE CLOCKS

An independent clock control product term is provided for each GAL20RA10 macrocell. Data is clocked into the flip-flop on the active edge of the clock product term. The use of individual clock control product terms allow up to ten separate clocks. These clocks can be derived from any pin or combination of pins and/or feedback from other flip-flops. Multiple clock sources allow a number of asynchronous register functions to be combined into a single GAL20RA10. This allows the designer to combine discrete logic functions into a single device.

PROGRAMMABLE POLARITY

The polarity of the D-input to each macrocell flip-flop is individually programmable to be active high or low. This is accomplished with a programmable Exclusive-OR gate on the D-input of each flip-flop. While any one of the four logic function product terms are active the D-input to the flip-flop will be low if the Exclusive-OR bit is set to zero(0) and high if the Exclusive-OR bit is set to one(1). It should be noted that the programmable polarity only affects the data latched into the flip-flop on the active edge of the clock product term. The reset, preset and preload will alter the state of the flip-flop independent of the state of programmable polarity bit. The ability to program the active polarity of the D-inputs can be used to reduce the total number of product terms used, by allowing the DeMorganization of the logic functions. This logic reduction is accomplished by the logic compiler, and does not require the designer to define the polarity.

OUTPUT ENABLE

The output of each GAL20RA10 macrocell is controlled by the "AND'ing" of an independent output enable product term and a common active low output enable pin(13). The output is enabled while the output enable product term is active and the output enable pin(13) is low. This output control structure allows several output enable alternatives.

ASYNCHRONOUS RESET AND PRESET

Each GAL20RA10 macrocell has an independent asynchronous reset and preset control product term. The reset and preset product terms are level sensitive, and will hold the flip-flop in the reset or preset state while the product term is active independent of the clock or D-inputs. It should be noted that the reset and preset term alter the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low.

RESET	PRESET	FUNCTION
0	0	Registered function of data product term
1	0	Reset register to "0" (device pin = "1")
0	1	Preset register to "1" (device pin = "0")
1	1	Register-bypass (combinatorial output)

COMBINATORIAL CONTROL

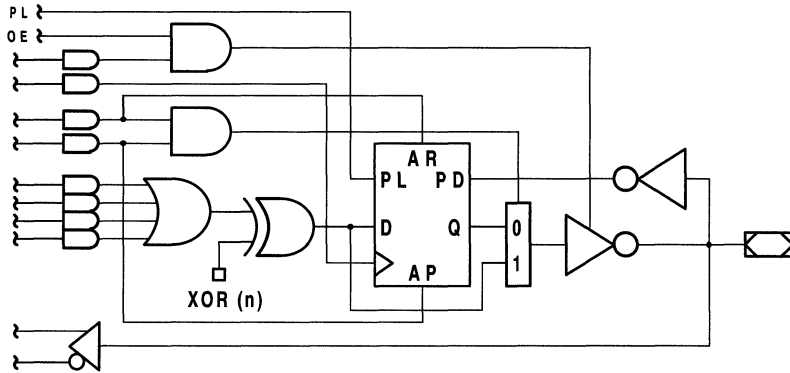
The register in each GAL20RA10 macrocell may be bypassed by asserting both the reset and preset product terms. While both product terms are active the flip-flop is bypassed and the D-input is presented directly to the inverting output buffer. This provides the designer the ability to dynamically configure any macrocell as a combinatorial output, or to fix the macrocell as combinatorial only by forcing both reset and preset product terms active. Some logic compilers will configure macrocells as registered or combinatorial based on the logic equations, others require the designer to force the reset and preset product terms active for combinatorial macrocells.

PARALLEL FLIP-FLOP PRELOAD

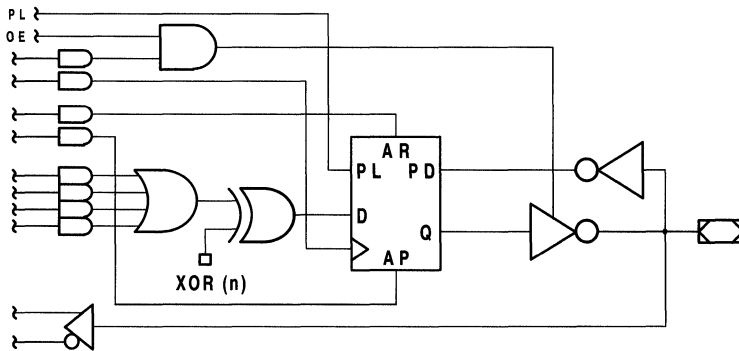
The flip-flops of a GAL20RA10 can be reset or preset from the I/O pins by applying a logic low to the preload pin (1) and applying the desired logic level to each I/O pin. The I/O pins must remain valid for the preload setup and hold time. All 10 flip-flops are reset or preset during preload, independent of all other OLMC inputs.

A logic low on an I/O pin during preload will preset the flip-flop, a logic high will reset the flip-flop. The output of any flip-flop to be preloaded must be disabled. Enabling the output during preload will maintain the current logic state. It should be noted that the preload alters the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low. Note that the common output enable pin (13) will disable all 10 outputs of the GAL20RA10 when held high.

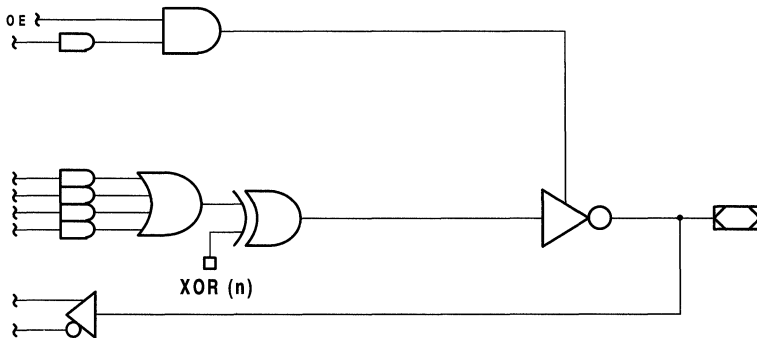
OUTPUT LOGIC MACROCELL DIAGRAM



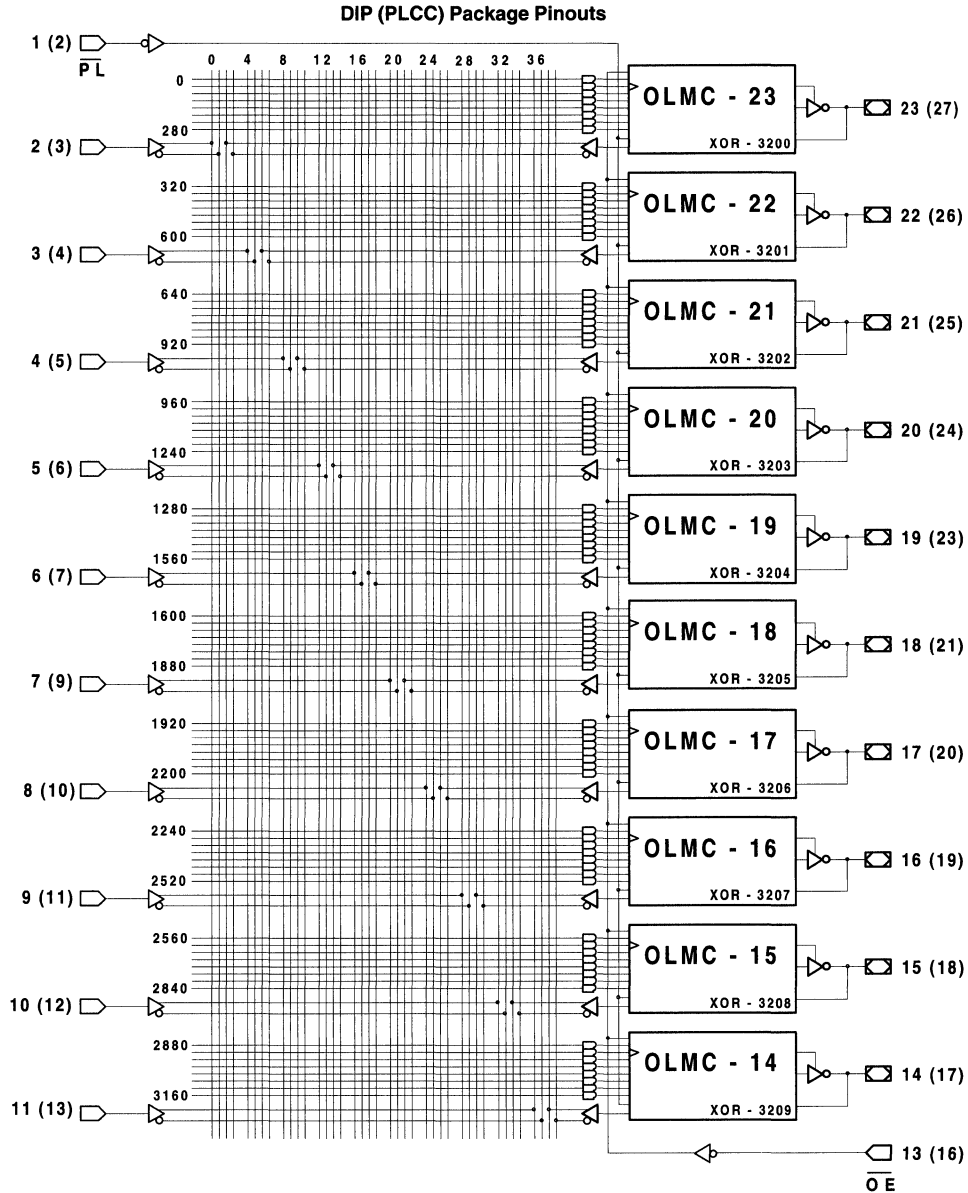
OUTPUT LOGIC MACROCELL CONFIGURATION (REGISTERED with POLARITY)



OUTPUT LOGIC MACROCELL CONFIGURATION (COMBINATORIAL with POLARITY)



GAL20RA10 LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

3210, 3211, 3272, 3273
Byte 7 Byte 6 Byte 1 Byte 0

M L
S S
B B

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to +85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -10	—	75	100	mA
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1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	COM		UNITS
			-10		
			MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	2	10	ns
t_{co}	A	Clock to Output Delay	2	11	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	4	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	3	—	ns
f_{max}²	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	66.7	—	MHz
	A	Maximum Clock Frequency without Feedback	71.4	—	MHz
t_{wh}	—	Clock Pulse Duration, High	7	—	ns
t_{wl}	—	Clock Pulse Duration, Low	7	—	ns
t_{en} / t_{dis}	B, C	Input or I/O to Output Enabled / Disabled	—	10	ns
t_{en} / t_{dis}	B, C	\overline{OE} to Output Enabled / Disabled	—	9	ns
t_{ar} / t_{ap}	A	Input or I/O to Asynchronous Reset / Preset	—	11	ns
t_{arw} / t_{apw}	—	Asynchronous Reset / Preset Pulse Duration	10	—	ns
t_{arr} / t_{apr}	—	Asynchronous Reset / Preset Recovery Time	7	—	ns
t_{wp}	—	Preload Pulse Duration	10	—	ns
t_{sp}	—	Preload Setup Time	7	—	ns
t_{hp}	—	Preload Hold Time	7	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Refer to **f_{max} Descriptions** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	8	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	10	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to +85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -15/-20/-30	—	75	100	mA
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INDUSTRIAL

I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -20	—	75	120	mA
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1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	COM		COM / IND		COM		UNITS
			-15		-20		-30		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	15	—	20	—	30	ns
t_{co}	A	Clock to Output Delay	—	15	—	20	—	30	ns
t_{su}	—	Setup Time, Input or Feedback before Clock \uparrow	7	—	10	—	20	—	ns
t_h	—	Hold Time, Input or Feedback after Clock \uparrow	3	—	3	—	10	—	ns
f_{max}^2	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	45.0	—	33.3	—	20.0	—	MHz
	A	Maximum Clock Frequency without Feedback	50.0	—	41.7	—	25.0	—	MHz
t_{wh}	—	Clock Pulse Duration, High	10	—	12	—	20	—	ns
t_{wl}	—	Clock Pulse Duration, Low	10	—	12	—	20	—	ns
t_{en} / t_{dis}	B,C	Input or I/O to Output Enabled / Disabled	—	15	—	20	—	30	ns
t_{en} / t_{dis}	B,C	\overline{OE} to Output Enabled / Disabled	—	12	—	15	—	20	ns
t_{ar} / t_{ap}	A	Input or I/O to Asynchronous Reset / Preset	—	15	—	20	—	30	ns
t_{arw} / t_{apw}	—	Asynchronous Reset / Preset Pulse Duration	15	—	20	—	20	—	ns
t_{arr} / t_{apr}	—	Asynchronous Reset / Preset Recovery Time	10	—	12	—	20	—	ns
t_{wp}	—	Preload Pulse Duration	15	—	20	—	30	—	ns
t_{sp}	—	Preload Setup Time	10	—	15	—	25	—	ns
t_{hp}	—	Preload Hold Time	10	—	15	—	25	—	ns

 1) Refer to **Switching Test Conditions** section.

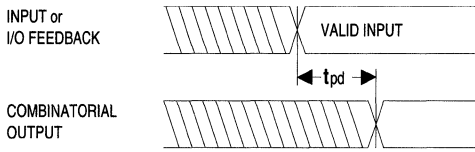
 2) Refer to **f_{max} Descriptions** section.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

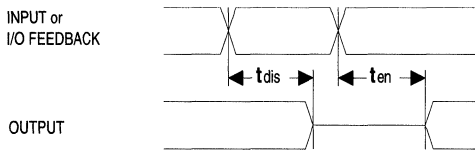
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V$, $V_i = 2.0V$
$C_{i/O}$	I/O Capacitance	10	pF	$V_{CC} = 5.0V$, $V_{i/O} = 2.0V$

*Guaranteed but not 100% tested.

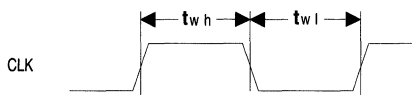
SWITCHING WAVEFORMS



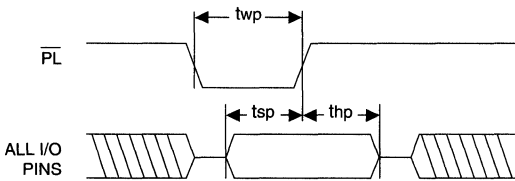
Combinatorial Output



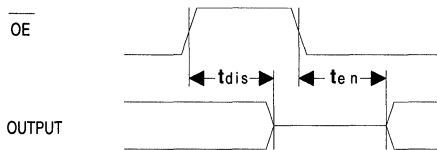
Input or I/O to Output Enable/Disable



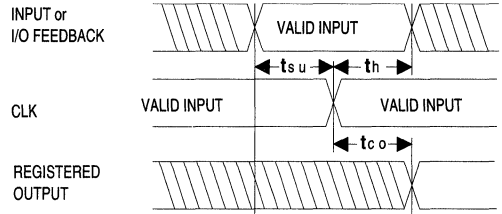
Clock Width



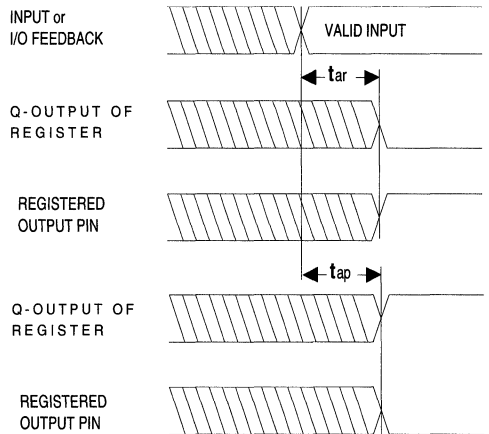
Parallel Preload



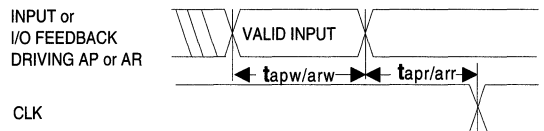
OE to Enable / Disable



Registered Output

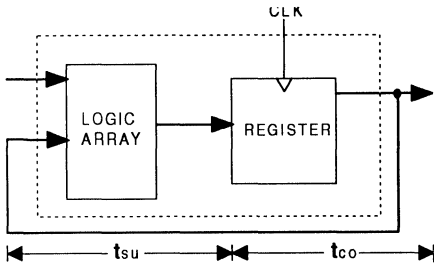


Asynchronous Reset and Preset



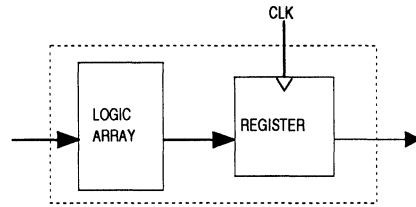
Asynchronous Reset and Preset Recovery

f_{max} DESCRIPTIONS



f_{max} with External Feedback $1/(t_{su} + t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

3

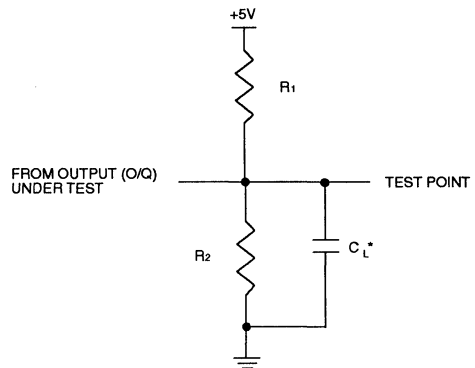
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L *
A	470Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	470Ω	390Ω
C	Active High	∞	390Ω
	Active Low	470Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20RA10 device. It contains 64 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits if programmed to any value other than zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20RA10 devices as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

LATCH-UP PROTECTION

GAL20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

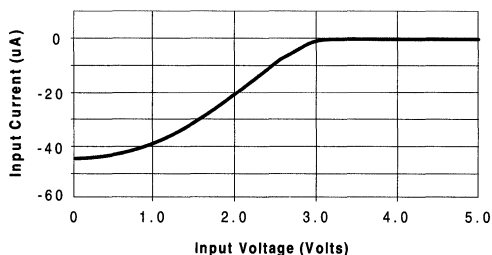
GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

INPUT BUFFERS

GAL20RA10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance and present a much lighter load to the driving logic than traditional bipolar devices.

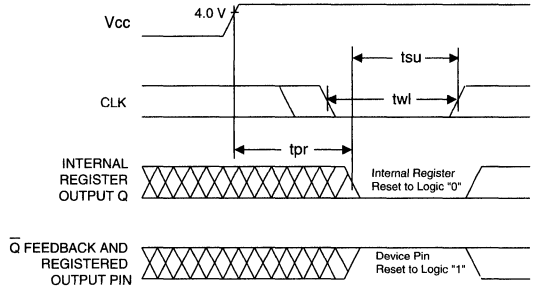
GAL20RA10 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic

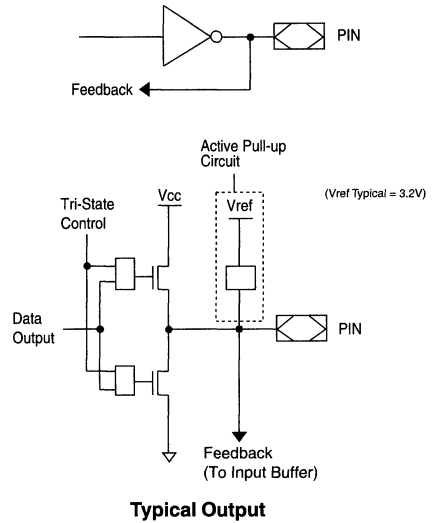
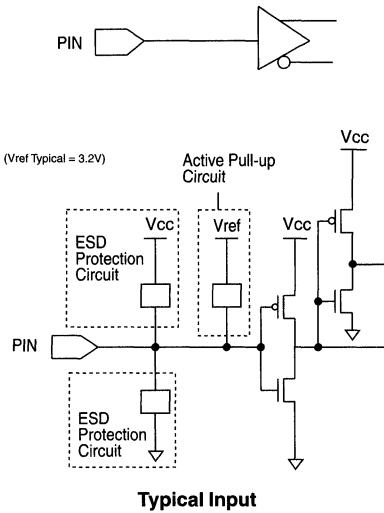


POWER-UP RESET

Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be high on power-up, because of the inverting buffer on the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown to the right. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20RA10. First, the V_{cc} rise must be monotonic. Second, the clock input must be at a static TTL level as shown in the diagram during power up. The registers will reset within a maximum of 1 μ s. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

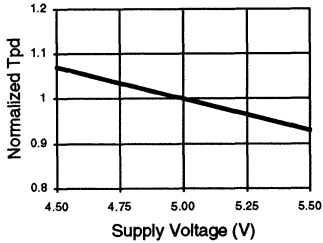


INPUT/OUTPUT EQUIVALENT SCHEMATICS

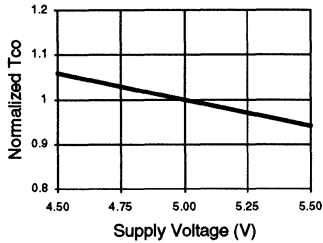


GAL20RA10B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

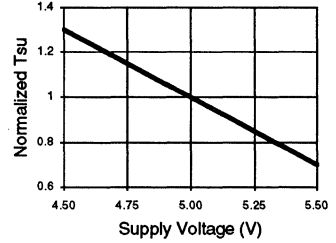
Normalized Tpd vs Vcc



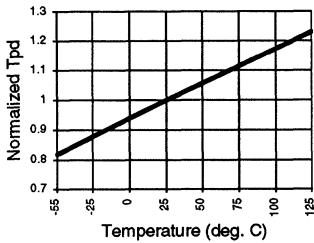
Normalized Tco vs Vcc



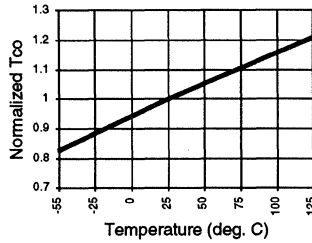
Normalized Tsu vs Vcc



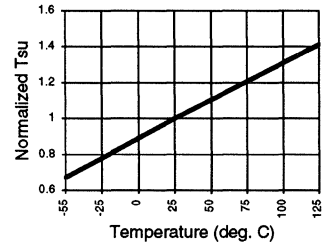
Normalized Tpd vs Temp



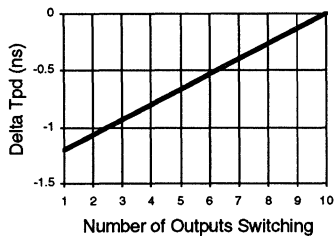
Normalized Tco vs Temp



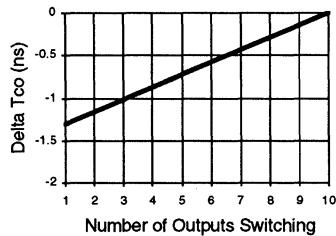
Normalized Tsu vs Temp



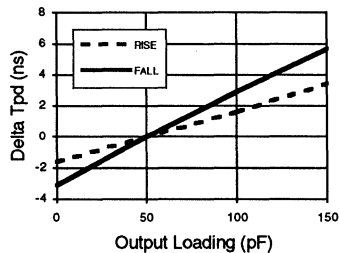
Delta Tpd vs # of Outputs Switching



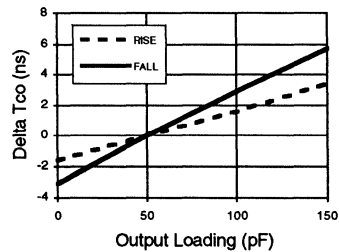
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading



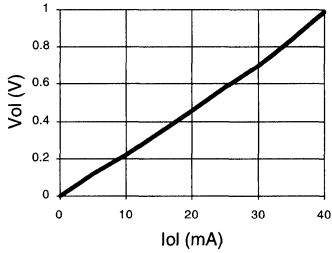
Delta Tco vs Output Loading



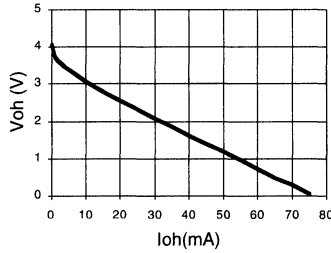
GAL20RA10B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

3

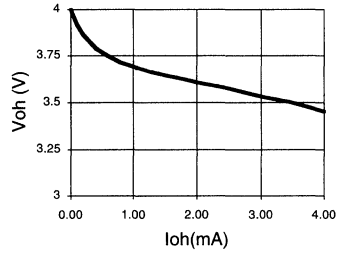
Vol vs Iol



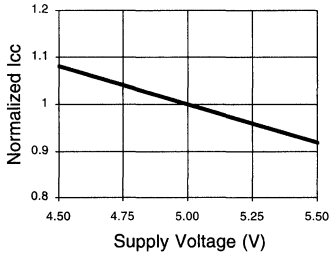
Voh vs Ioh



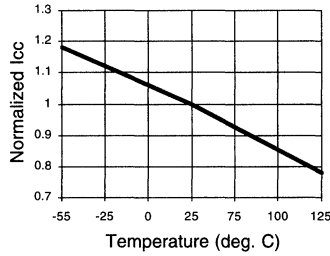
Voh vs Ioh



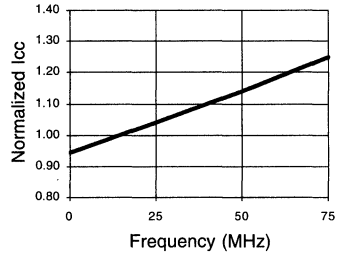
Normalized Icc vs Vcc



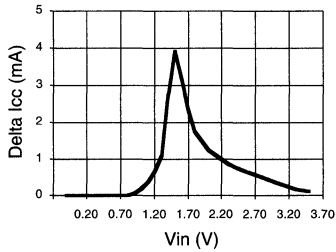
Normalized Icc vs Temp



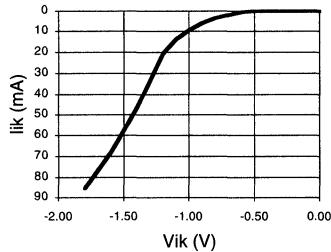
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

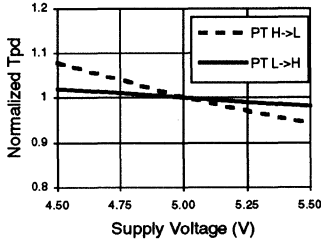


Input Clamp (Vik)

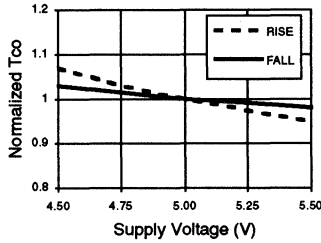


GAL20RA10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

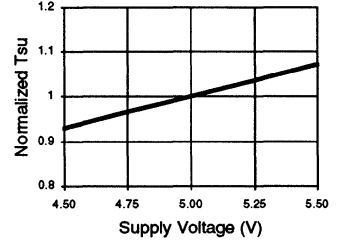
Normalized Tpd vs Vcc



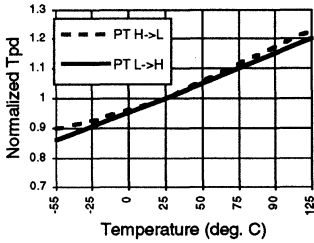
Normalized Tco vs Vcc



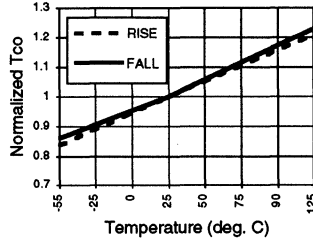
Normalized Tsu vs Vcc



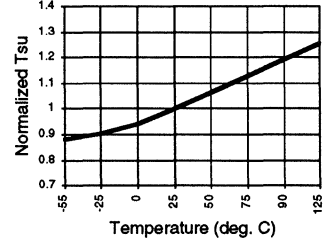
Normalized Tpd vs Temp



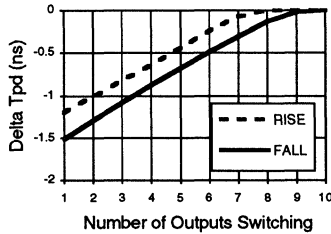
Normalized Tco vs Temp



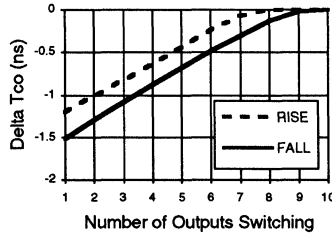
Normalized Tsu vs Temp



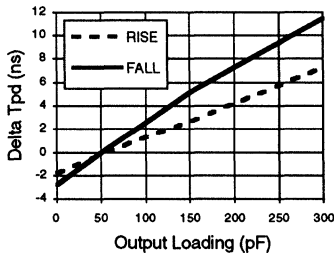
Delta Tpd vs # of Outputs Switching



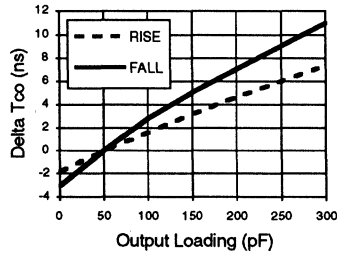
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

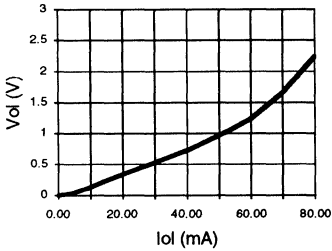


Delta Tco vs Output Loading

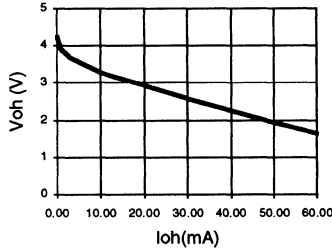


GAL20RA10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

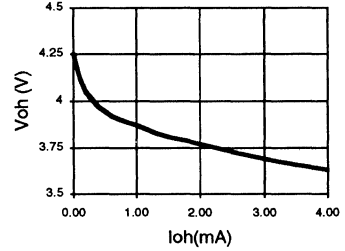
Vol vs Iol



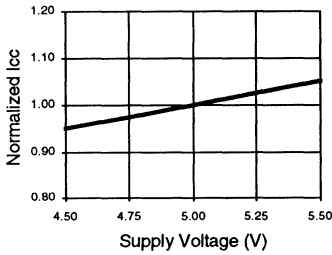
Voh vs Ioh



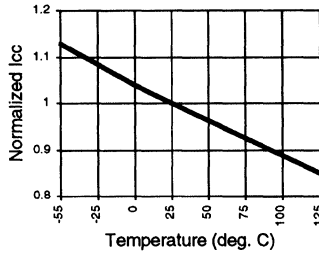
Voh vs Ioh



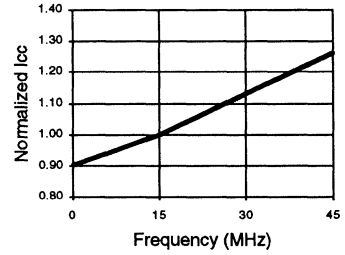
Normalized Icc vs Vcc



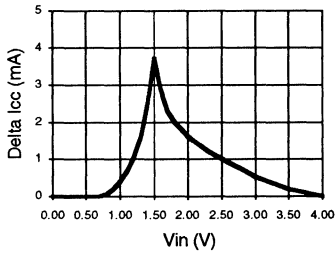
Normalized Icc vs Temp



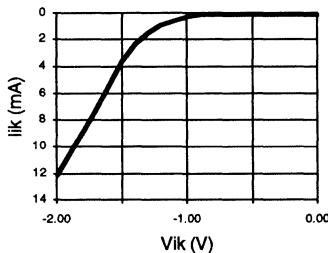
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)



Input Clamp (Vik)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 5 ns Maximum Propagation Delay
 - Fmax = 166 MHz
 - 4 ns Maximum from Clock Input to Data Output
 - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ Icc on Low Power Device
 - 45mA Typ Icc on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

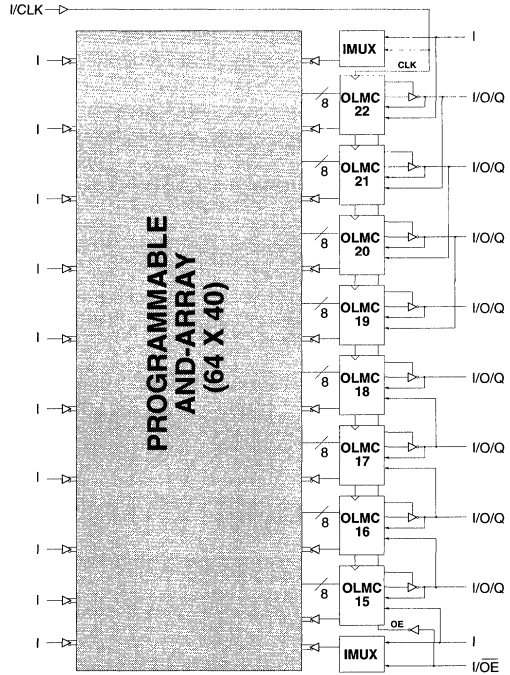
DESCRIPTION

The GAL20V8C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8 are the PAL architectures listed in the table of the macrocell description section. GAL20V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

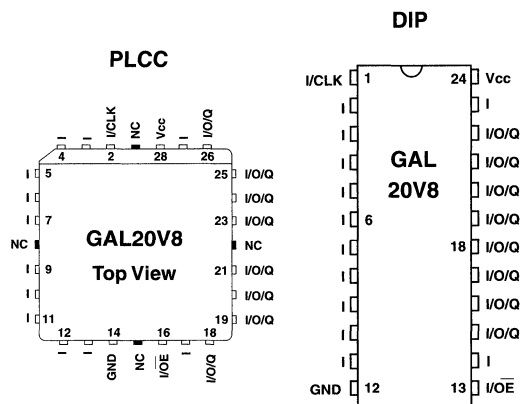
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



3

PIN CONFIGURATION



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GAL20V8 ORDERING INFORMATION

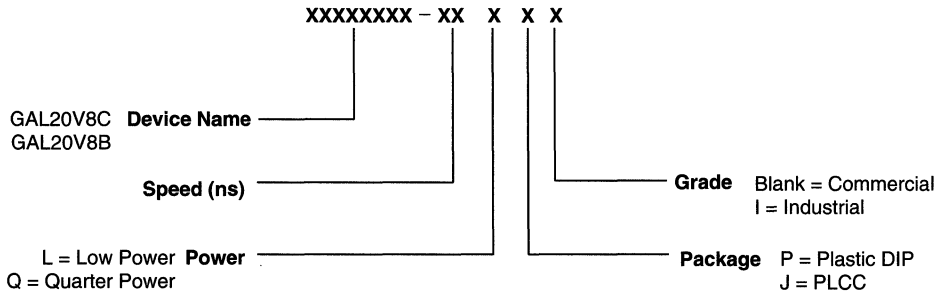
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJ	28-Lead PLCC
7.5	7	5	115	GAL20V8B-7LP	24-Pin Plastic DIP
			115	GAL20V8B-7LJ	28-Lead PLCC
10	10	7	115	GAL20V8B-10LP	24-Pin Plastic DIP
			115	GAL20V8B-10LJ	28-Lead PLCC
15	12	10	55	GAL20V8B-15QP	24-Pin Plastic DIP
			55	GAL20V8B-15QJ	28-Lead PLCC
			90	GAL20V8B-15LP	24-Pin Plastic DIP
			90	GAL20V8B-15LJ	28-Lead PLCC
25	15	12	55	GAL20V8B-25QP	24-Pin Plastic DIP
			55	GAL20V8B-25QJ	28-Lead PLCC
			90	GAL20V8B-25LP	24-Pin Plastic DIP
			90	GAL20V8B-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8B-10LPI	24-Pin Plastic DIP
			130	GAL20V8B-10LJI	28-Lead PLCC
15	12	10	130	GAL20V8B-15LPI	24-Pin Plastic DIP
			130	GAL20V8B-15LJI	28-Lead PLCC
20	13	11	65	GAL20V8B-20QPI	24-Pin Plastic DIP
			65	GAL20V8B-20QJI	28-Lead PLCC
25	15	12	65	GAL20V8B-25QPI	24-Pin Plastic DIP
			65	GAL20V8B-25QJI	28-Lead PLCC
			130	GAL20V8B-25LPI	24-Pin Plastic DIP
			130	GAL20V8B-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20V8 can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20V8	GAL20V8 Global OLMC Mode
20R8	Registered
20R6	Registered
20R4	Registered
20RP8	Registered
20RP6	Registered
20RP4	Registered
20L8	Complex
20H8	Complex
20P8	Complex
14L8	Simple
16L6	Simple
18L4	Simple
20L2	Simple
14H8	Simple
16H6	Simple
18H4	Simple
20H2	Simple
14P8	Simple
16P6	Simple
18P4	Simple
20P2	Simple

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 13 (DIP pinout) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 22 and pin 15 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pin 18 and 19) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered" ¹	"Complex" ¹	"Simple" ¹	GAL20V8A
PLDesigner	P20V8R ²	P20V8C ²	P20V8C ²	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS ³	G20V8

1) Used with **Configuration** keyword.
 2) Prior to Version 2.0 support.
 3) Supported on Version 1.20 or later.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

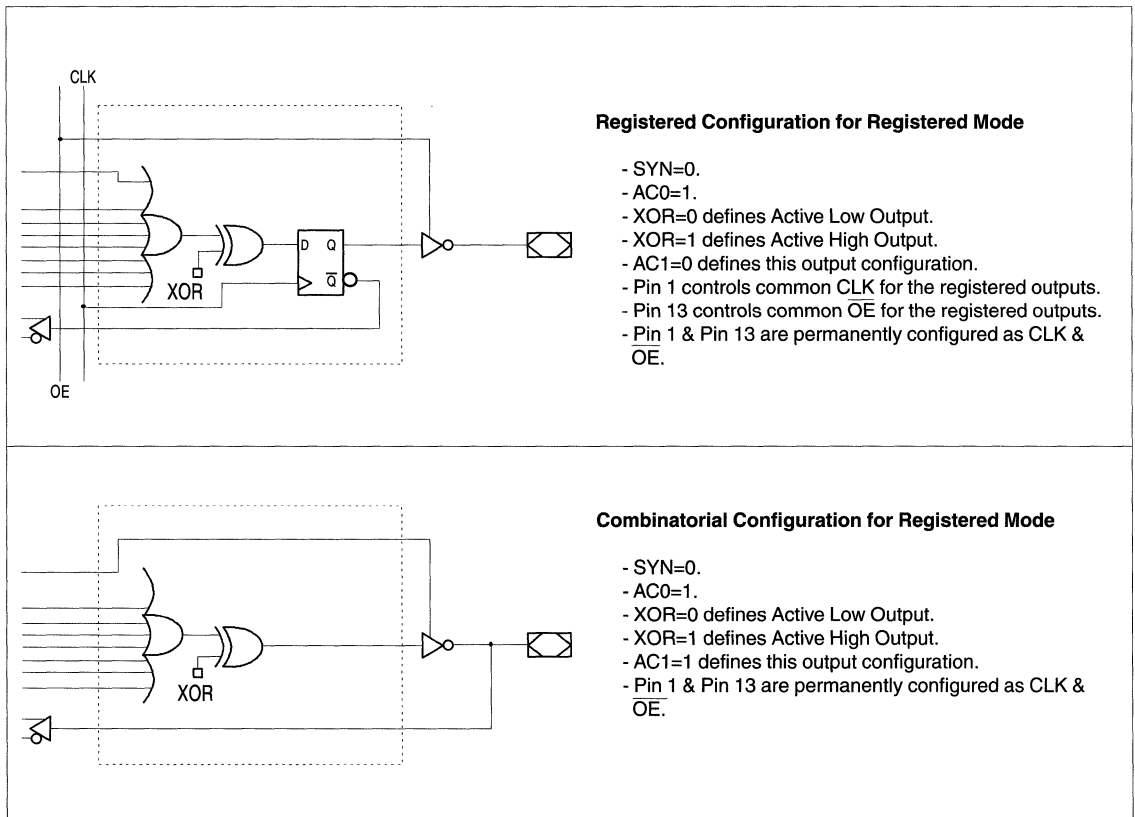
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this

mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

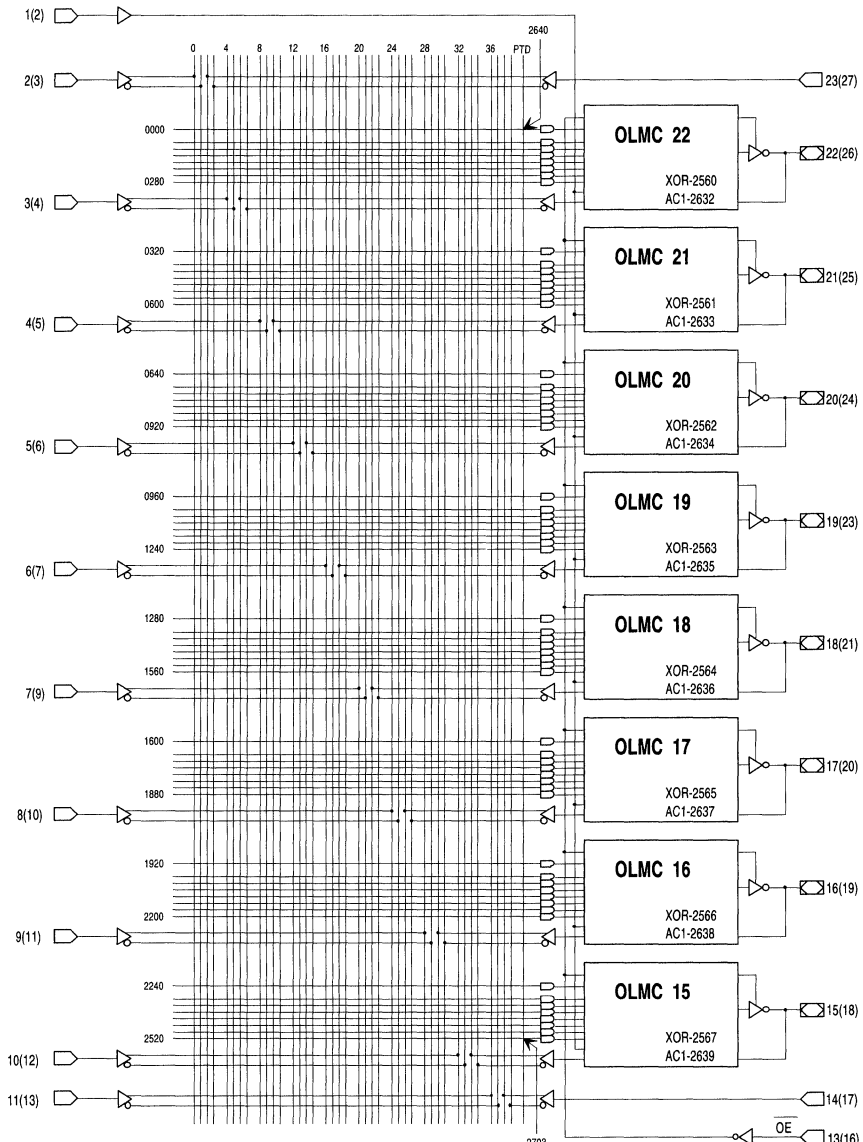
The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ..., 2630, 2631
 Byte 7 | Byte 6 | ... | Byte 1 | Byte 0

M L
 S S
 B B

SYN-2704
 ACO-2705

COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

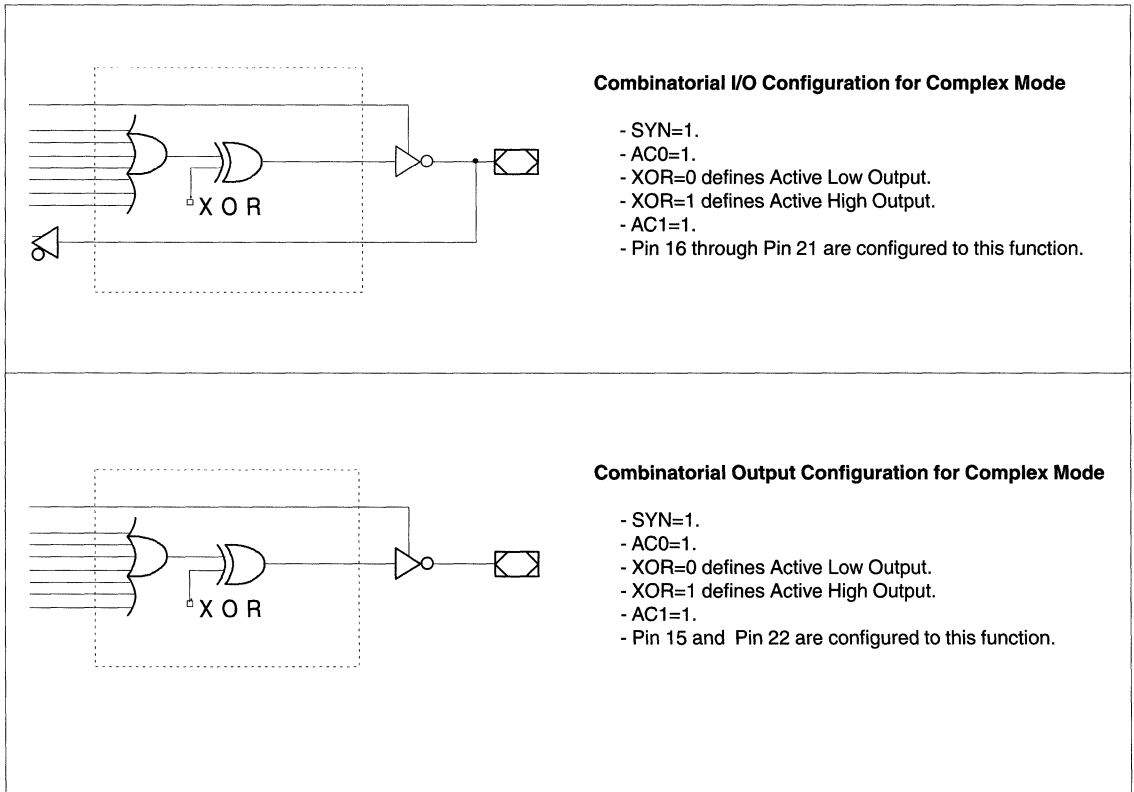
Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input ca-

patibility. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

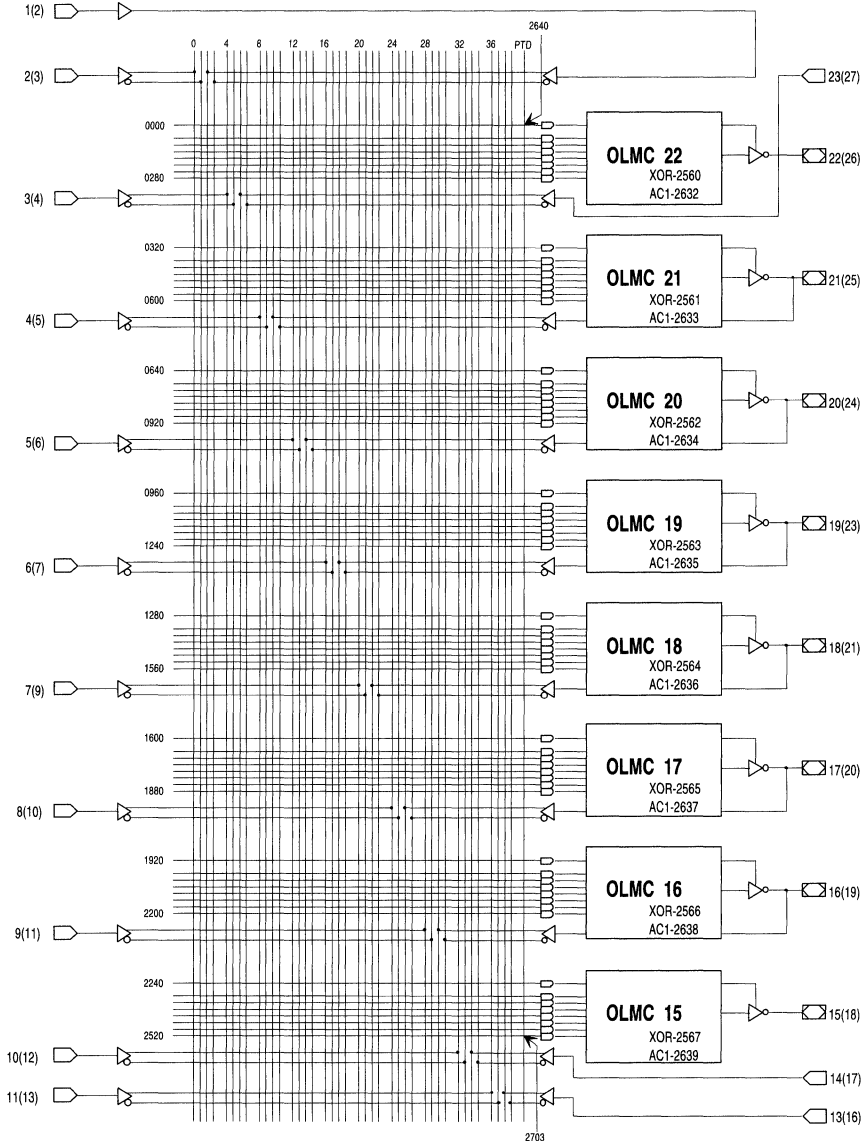
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	2630, 2631
Byte 7 Byte 6 ...	Byte 1 Byte 0

M L
S S
B B

SYN-2704
ACO-2705

SIMPLE MODE

In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 18 & 19) cannot be used in the input configuration.

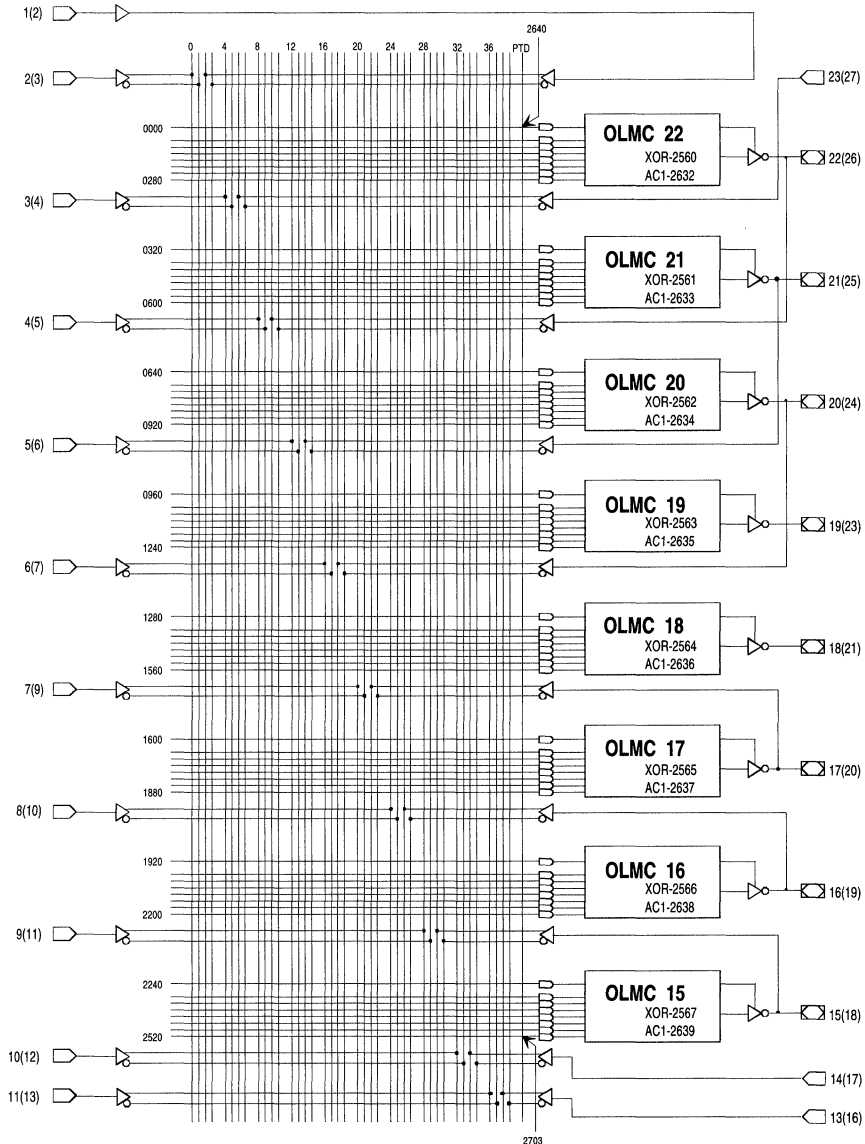
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - All OLMC except pins 18 & 19 can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - Pins 18 & 19 are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - All OLMC except pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569,	2630, 2631
Byte 7 Byte 6 	Byte 1 Byte 0

M L
S S
B B

SYN-2704
ACO-2705

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -5	—	75	115	mA
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- 1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		UNITS
			-5		
			MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	1	5	ns
t_{co}	A	Clock to Output Delay	1	4	ns
t_{cf}²	—	Clock to Feedback Delay	—	3	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	3	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	142.8	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	166	—	MHz
	A	Maximum Clock Frequency with No Feedback	166	—	MHz
t_{wh}	—	Clock Pulse Duration, High	3	—	ns
t_{wl}	—	Clock Pulse Duration, Low	3	—	ns
t_{en}	B	Input or I/O to Output Enabled	1	6	ns
	B	\overline{OE} to Output Enabled	1	6	ns
t_{dis}	C	Input or I/O to Output Disabled	1	5	ns
	C	\overline{OE} to Output Disabled	1	5	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

 3) Refer to **f_{max} Descriptions** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _i	Input Capacitance	8	pF	V _{cc} = 5.0V, V _i = 2.0V
C _{i/O}	I/O Capacitance	8	pF	V _{cc} = 5.0V, V _{i/O} = 2.0V

*Guaranteed but not 100% tested.

3

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -7/-10	—	75	115	mA
			L -15/-25	—	75	90	mA
			Q -15/-25	—	45	55	mA

INDUSTRIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND ¹ .	DESCRIPTION	COM		COM / IND		COM / IND		IND		COM / IND		UNITS
			-7		-10		-15		-20		-25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to 8 outputs switching	3	7.5	3	10	3	15	3	20	3	25	ns
		Comb. Output 1 output switching	—	7	—	—	—	—	—	—	—	—	ns
t_{co}	A	Clock to Output Delay	2	5	2	7	2	10	2	11	2	12	ns
t_{cf}²	—	Clock to Feedback Delay	—	3	—	6	—	8	—	9	—	10	ns
t_{su}	—	Setup Time, Input or Fdbk before Clk [↑]	7	—	10	—	12	—	13	—	15	—	ns
t_h	—	Hold Time, Input or Fdbk after Clk [↑]	0	—	0	—	0	—	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	83.3	—	58.8	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	100	—	62.5	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	62.5	—	62.5	—	50	—	41.7	—	MHz
t_{wh}	—	Clock Pulse Duration, High	5	—	8	—	8	—	10	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	5	—	8	—	8	—	10	—	12	—	ns
t_{en}	B	Input or I/O to Output Enabled	3	9	3	10	—	15	—	20	—	25	ns
	B	\overline{OE} to Output Enabled	2	6	2	10	—	15	—	18	—	20	ns
t_{dis}	C	Input or I/O to Output Disabled	2	9	2	10	—	15	—	20	—	25	ns
	C	\overline{OE} to Output Disabled	1.5	6	1.5	10	—	15	—	18	—	20	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

3) Refer to **f_{max} Descriptions** section.

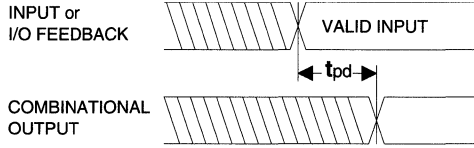
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _i	Input Capacitance	8	pF	V _{CC} = 5.0V, V _i = 2.0V
C _{i/o}	I/O Capacitance	8	pF	V _{CC} = 5.0V, V _{i/o} = 2.0V

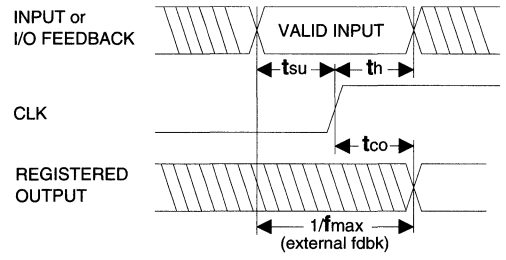
*Guaranteed but not 100% tested.

3

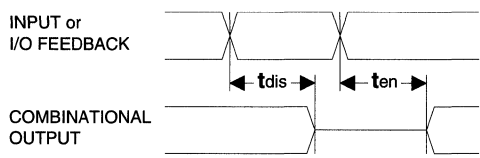
SWITCHING WAVEFORMS



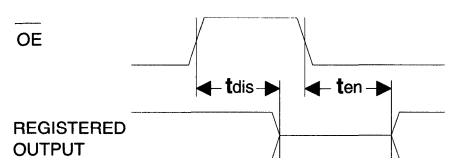
Combinatorial Output



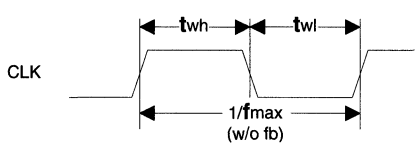
Registered Output



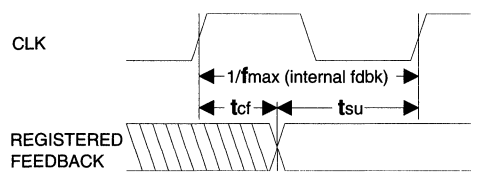
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

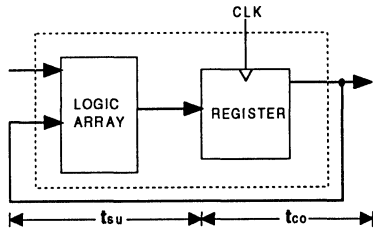


Clock Width



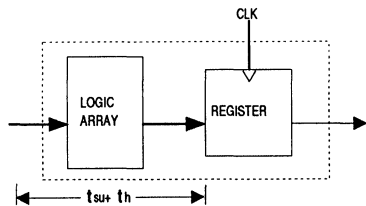
fmax with Feedback

f_{max} DESCRIPTIONS



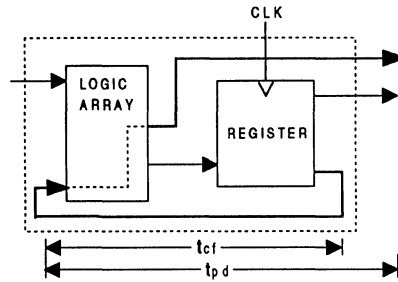
f_{max} with External Feedback 1/(tsu+tco)

Note: f_{max} with external feedback is calculated from measured tsu and tco.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback 1/(tsu+tcf)

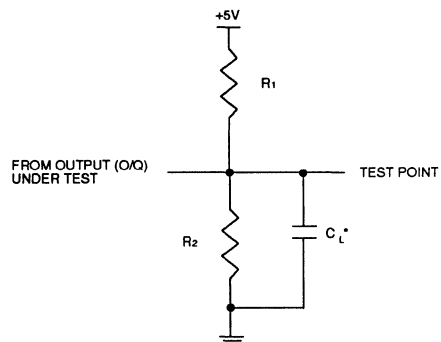
Note: tcf is a calculated value, derived by subtracting tsu from the period of f_{max} w/internal feedback (tcf = 1/f_{max} - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to tcf + tpd.

3

SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL20V8B	2 – 3ns 10% – 90%
	GAL20V8C	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.



*CL INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL20V8B Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	200Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	200Ω	390Ω
C	Active High	∞	390Ω
	Active Low	200Ω	390Ω

GAL20V8C Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	200Ω	200Ω	50pF
B	Active High	∞	200Ω
	Active Low	200Ω	200Ω
C	Active High	∞	200Ω
	Active Low	200Ω	200Ω

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL20V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided in the GAL20V8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL20V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

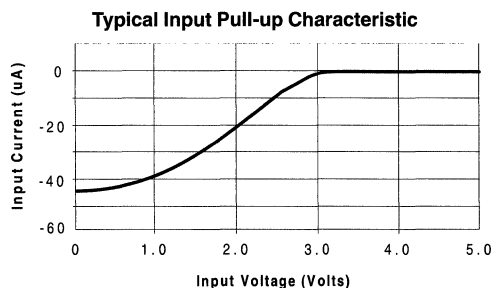
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL20V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

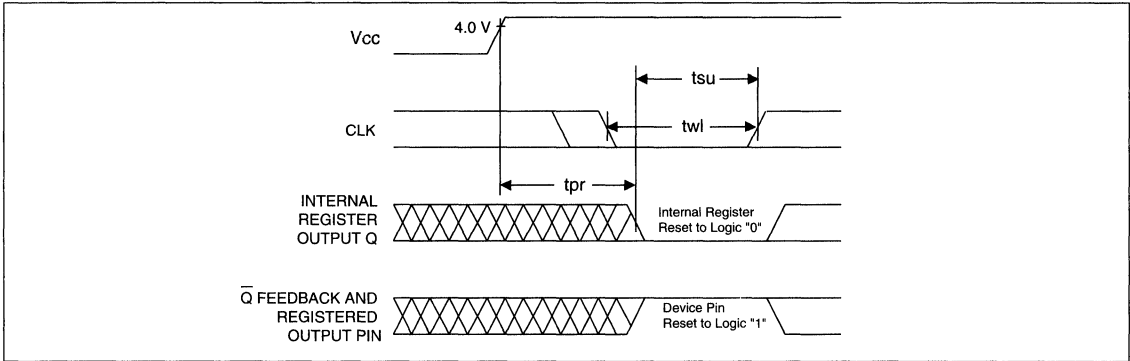
INPUT BUFFERS

GAL20V8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL20V8 input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC} , or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.



POWER-UP RESET

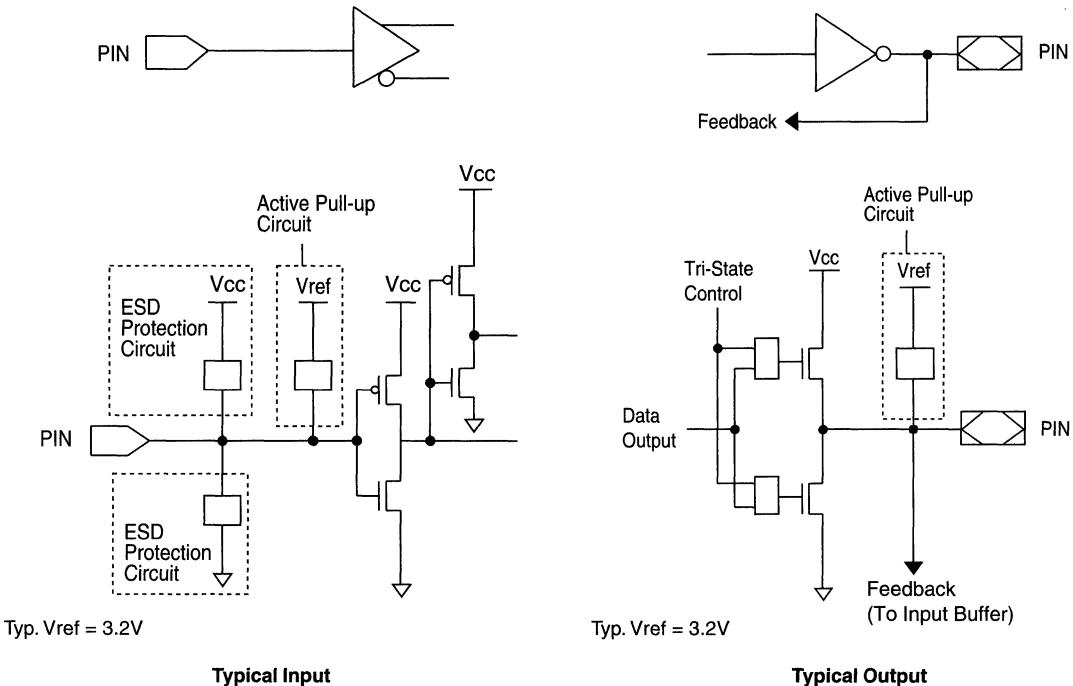


3

Circuitry within the GAL20V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

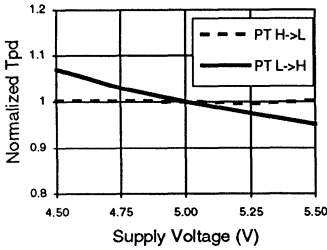
conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

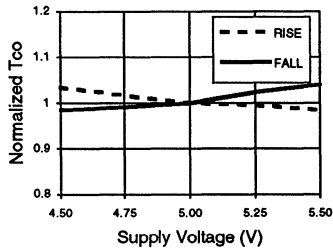


GAL 20V8C-5: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

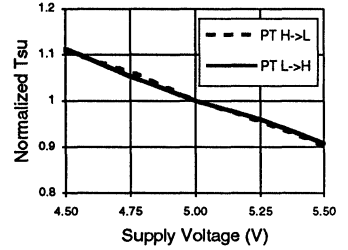
Normalized Tpd vs Vcc



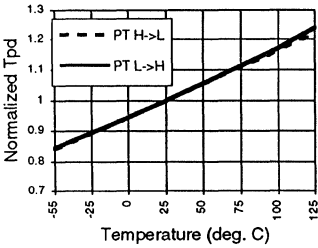
Normalized Tco vs Vcc



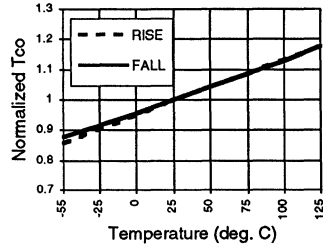
Normalized Tsu vs Vcc



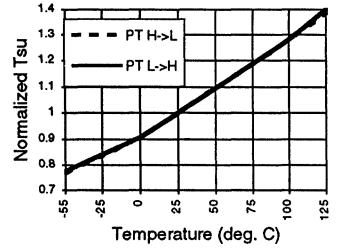
Normalized Tpd vs Temp



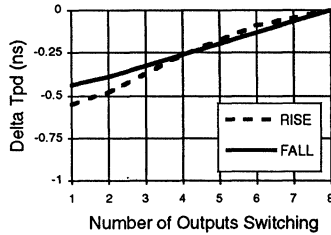
Normalized Tco vs Temp



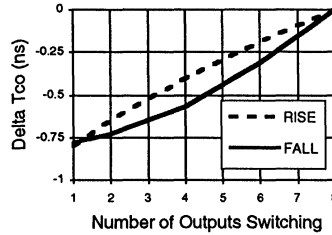
Normalized Tsu vs Temp



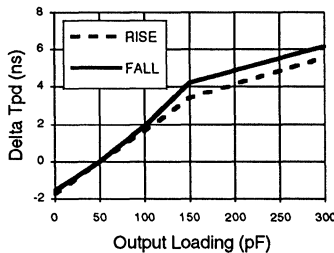
Delta Tpd vs # of Outputs Switching



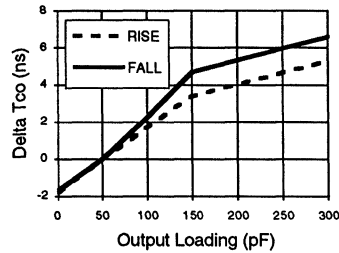
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

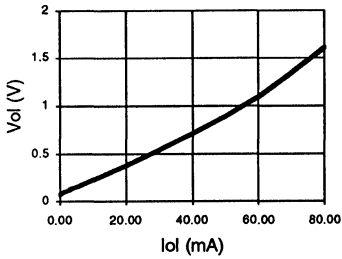


Delta Tco vs Output Loading

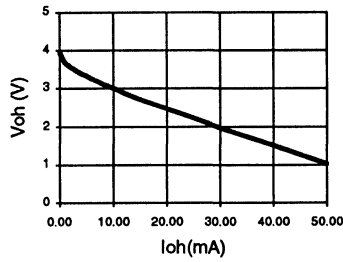


GAL 20V8C-5: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

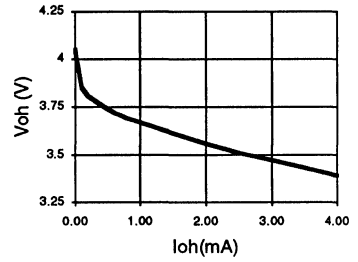
Vol vs Iol



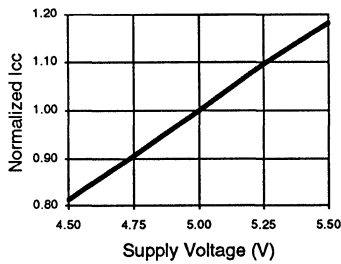
Voh vs Ioh



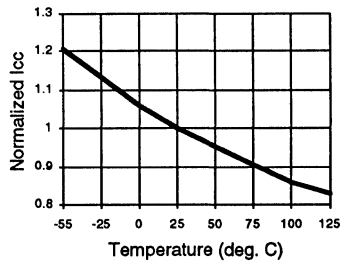
Voh vs Ioh



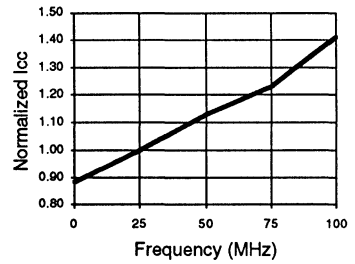
Normalized Icc vs Vcc



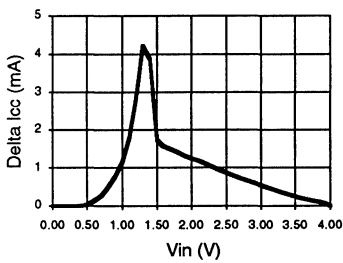
Normalized Icc vs Temp



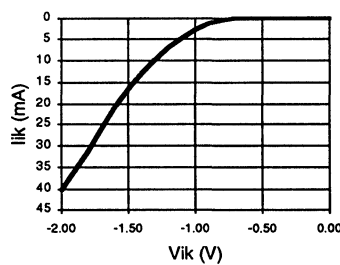
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

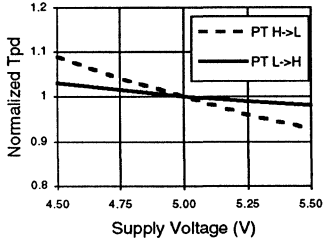


Input Clamp (Vik)

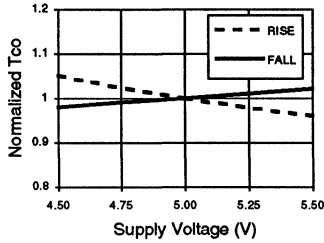


GAL 20V8B-7/10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

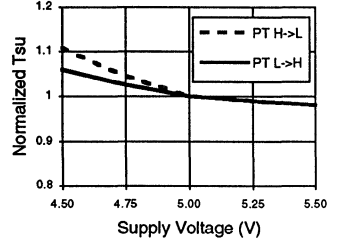
Normalized Tpd vs Vcc



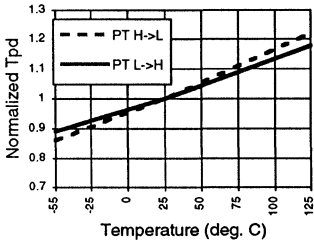
Normalized Tco vs Vcc



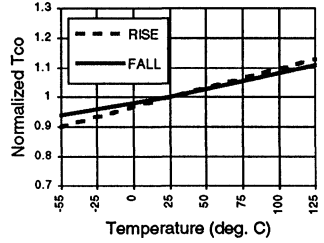
Normalized Tsu vs Vcc



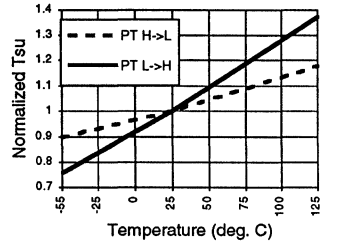
Normalized Tpd vs Temp



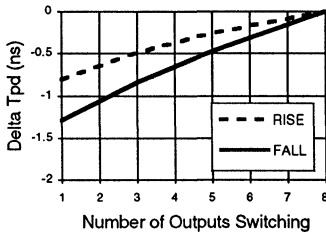
Normalized Tco vs Temp



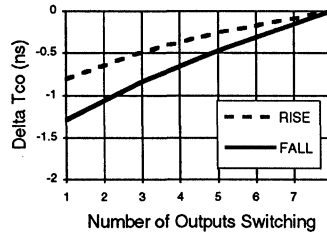
Normalized Tsu vs Temp



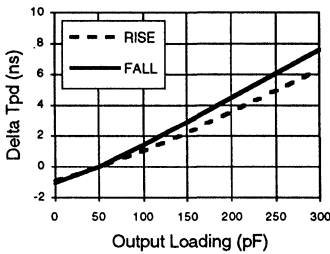
Delta Tpd vs # of Outputs Switching



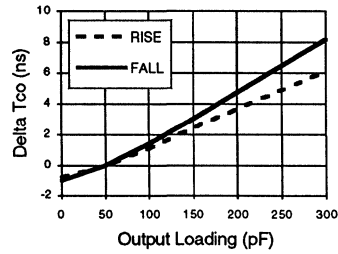
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

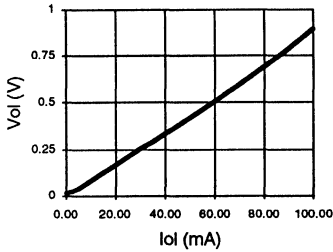


Delta Tco vs Output Loading

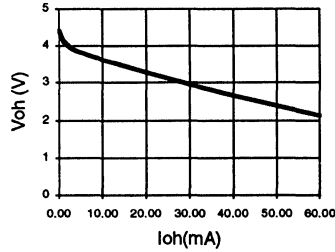


GAL 20V8B-7/10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

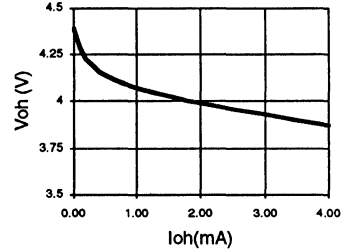
Vol vs Iol



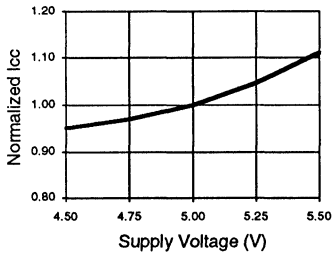
Voh vs Ioh



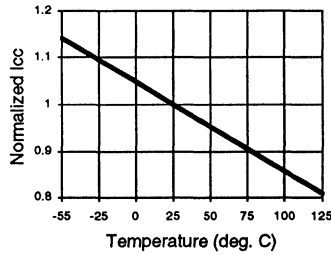
Voh vs Ioh



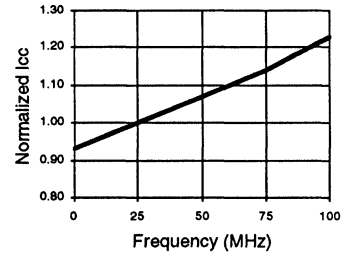
Normalized Icc vs Vcc



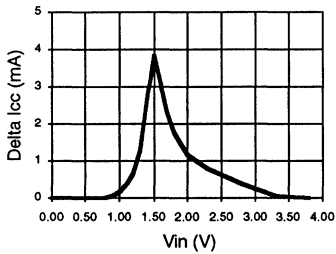
Normalized Icc vs Temp



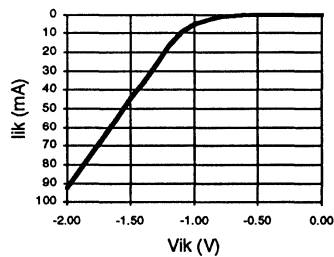
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

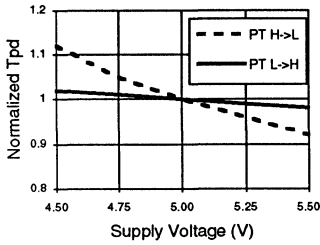


Input Clamp (Vik)

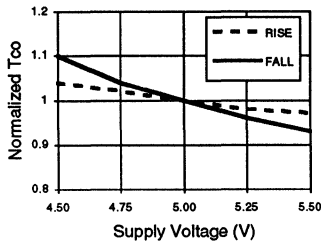


GAL 20V8B-15/25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

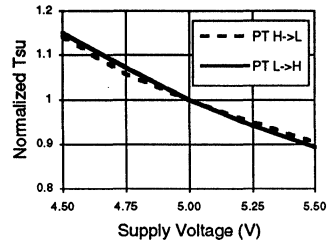
Normalized Tpd vs Vcc



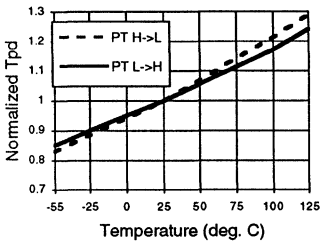
Normalized Tco vs Vcc



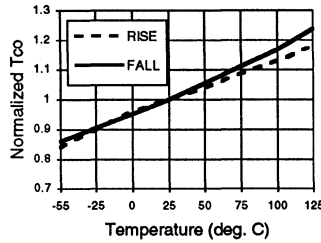
Normalized Tsu vs Vcc



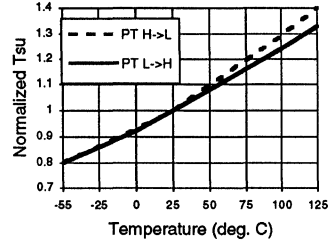
Normalized Tpd vs Temp



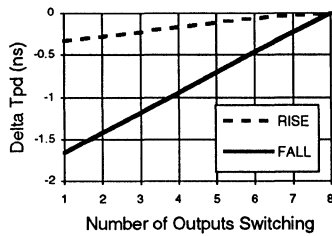
Normalized Tco vs Temp



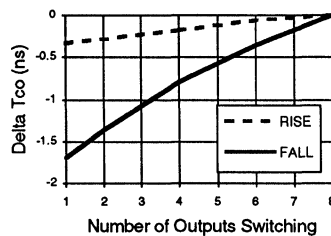
Normalized Tsu vs Temp



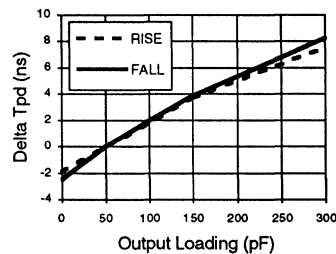
Delta Tpd vs # of Outputs Switching



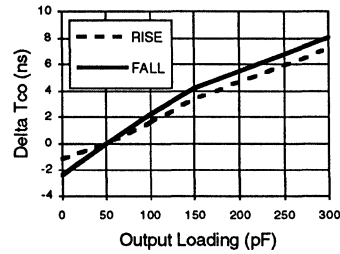
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

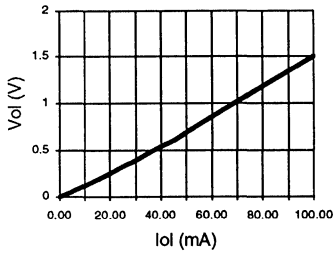


Delta Tco vs Output Loading

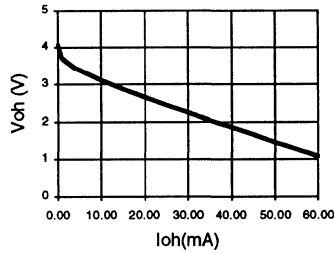


GAL 20V8B-15/25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

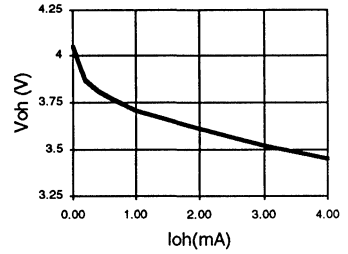
Vol vs Iol



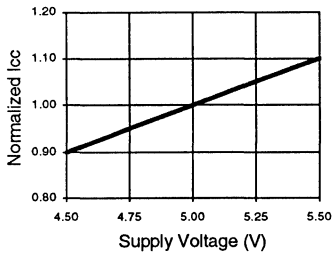
Voh vs Ioh



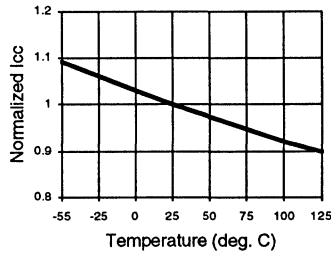
Voh vs Ioh



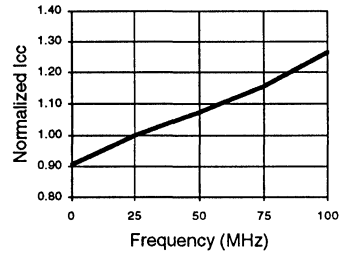
Normalized Icc vs Vcc



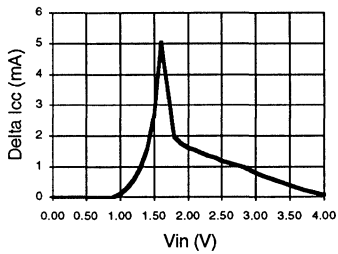
Normalized Icc vs Temp



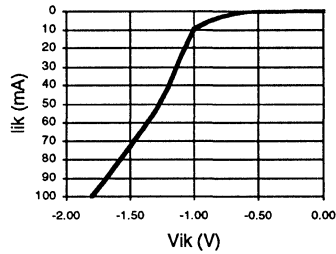
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)



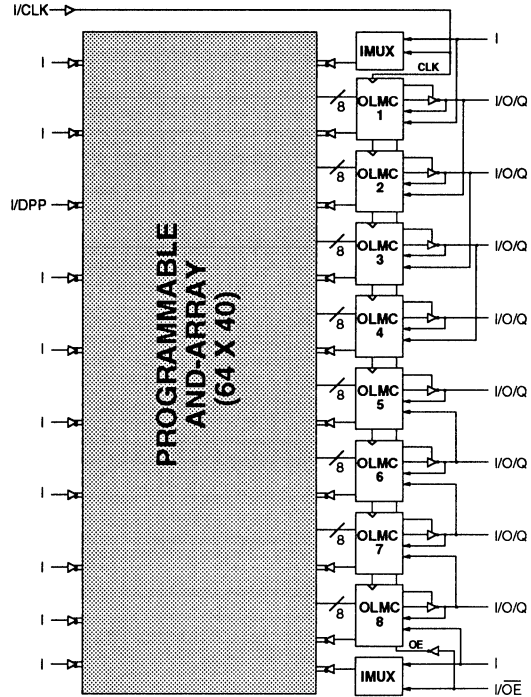
Input Clamp (Vik)



FEATURES

- ZERO POWER E²CMOS TECHNOLOGY
 - 100µA Standby Current
 - Input Transition Detection on GAL20V8Z
 - Dedicated Power-down Pin on GAL20V8ZD
 - Input and Output Latching During Power Down
- HIGH PERFORMANCE E²CMOS TECHNOLOGY
 - 12 ns Maximum Propagation Delay
 - F_{max} = 83.3 MHz
 - 8 ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Output Drive
 - UltraMOS[®] Advanced CMOS Technology
- E² CELL TECHNOLOGY
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Architecturally Similar to Standard GAL20V8
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
 - 100% Functional Testability
- APPLICATIONS INCLUDE:
 - Battery Powered Systems
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

FUNCTIONAL BLOCK DIAGRAM



3

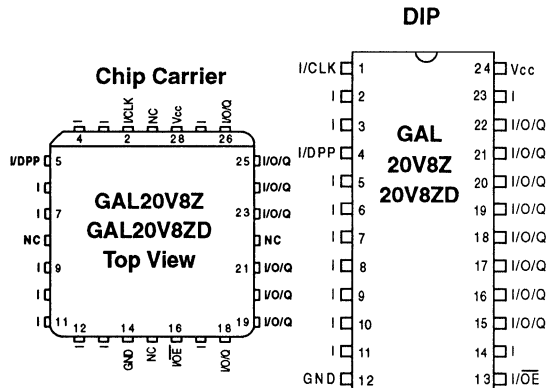
DESCRIPTION

The GAL20V8Z and GAL20V8ZD, at 100 µA standby current and 12ns propagation delay provides the highest speed and lowest power combination PLD available in the market. The GAL20V8Z/ZD is manufactured using Lattice's advanced zero power E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology.

The GAL20V8Z uses Input Transition Detection (ITD) to put the device in standby mode and is capable of emulating the full functionality of the standard GAL20V8. The GAL20V8ZD utilizes a dedicated power-down pin (DPP) to put the device in standby mode. It has 19 inputs available to the AND array.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

PIN CONFIGURATION



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GAL 20V8Z/ZD ORDERING INFORMATION

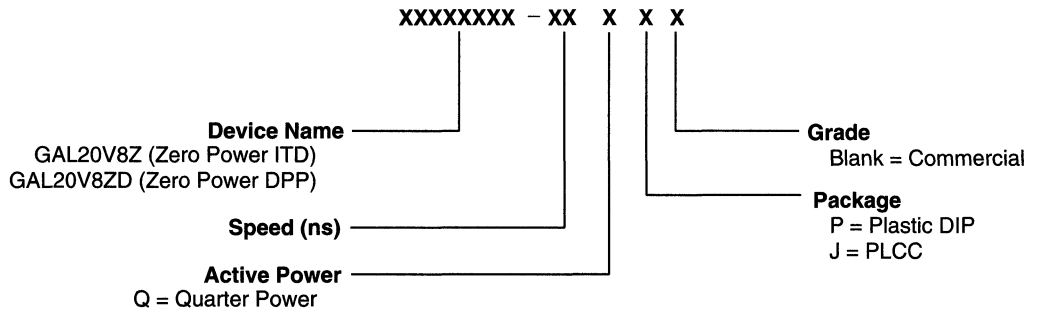
GAL20V8Z: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	ISB (µA)	Ordering #	Package
12	10	8	55	100	GAL20V8Z-12QP	24-Pin Plastic DIP
			55	100	GAL20V8Z-12QJ	28-Lead PLCC
15	15	10	55	100	GAL20V8Z-15QP	24-Pin Plastic DIP
			55	100	GAL20V8Z-15QJ	28-Lead PLCC

GAL20V8ZD: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	ISB (µA)	Ordering #	Package
12	10	8	55	100	GAL20V8ZD-12QP	24-Pin Plastic DIP
			55	100	GAL20V8ZD-12QJ	28-Lead PLCC
15	15	10	55	100	GAL20V8ZD-15QP	24-Pin Plastic DIP
			55	100	GAL20V8ZD-15QJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The

XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8Z/ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1(2) and pin 13(16) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1(2) and pin 13(16) become dedicated inputs and use the feedback paths of pin 22(26) and pin 15(18) respectively. Because of this feedback path usage, pin 22(26) and pin 15(18) do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18(21) and 19(23)) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL20V8 JEDEC fuse pattern generated by the logic compilers for the GAL20V8ZD, special attention must be given to pin 4(5) (DPP) to make sure that it is not used as one of the functional inputs.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

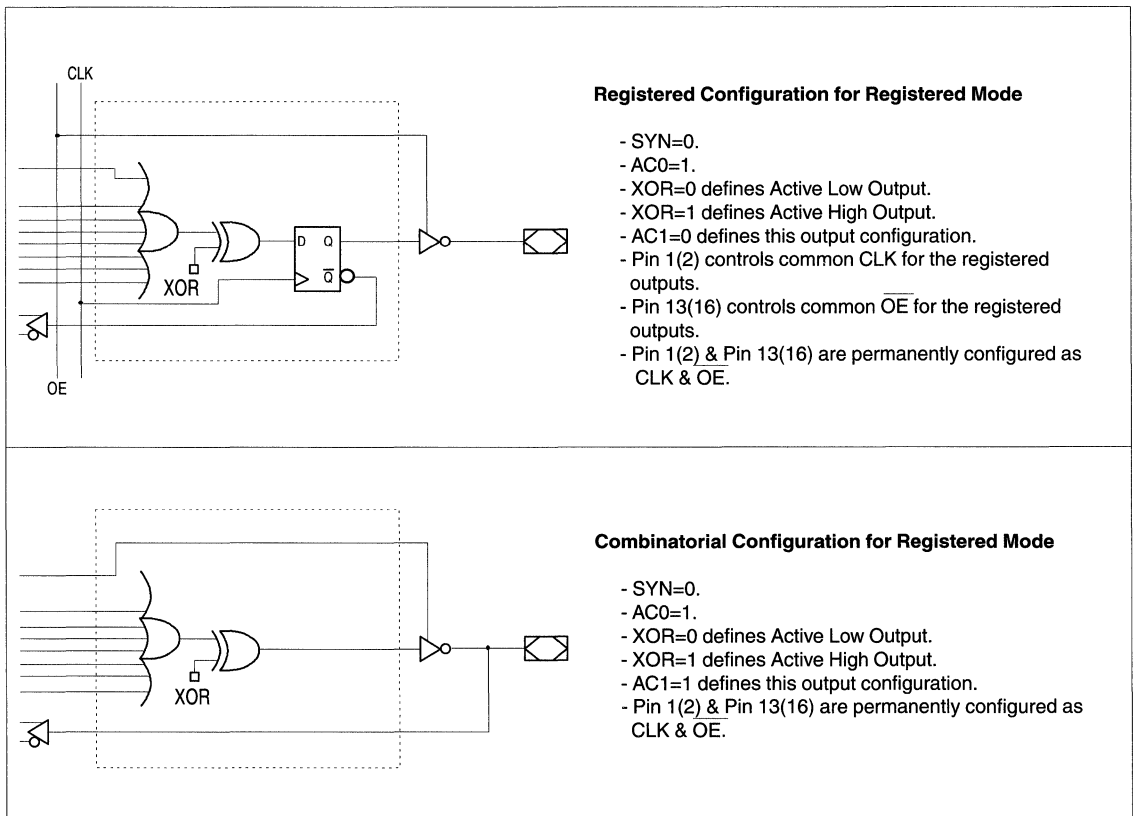
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

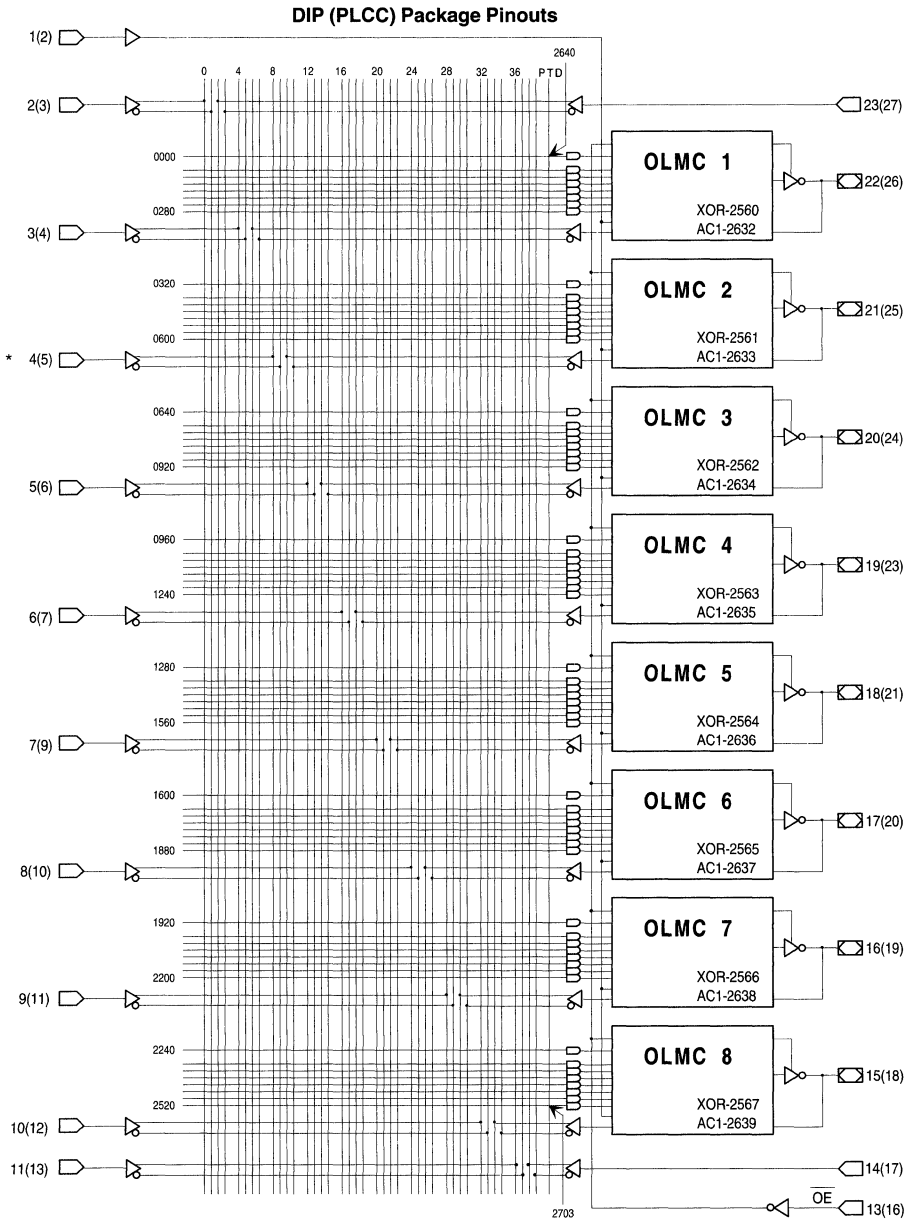
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, 2630, 2631
Byte7 Byte6 Byte1 Byte0

MSB LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

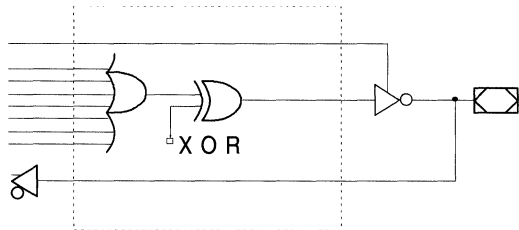
Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15(18) & 22(26)) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1(2) and 13(16) are always available as data inputs into the AND array.

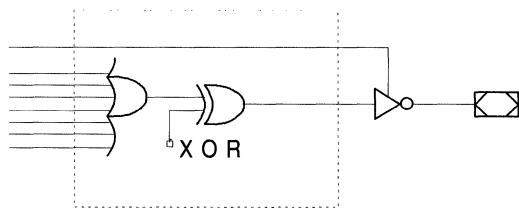
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 16(19) through Pin 21(25) are configured to this function.

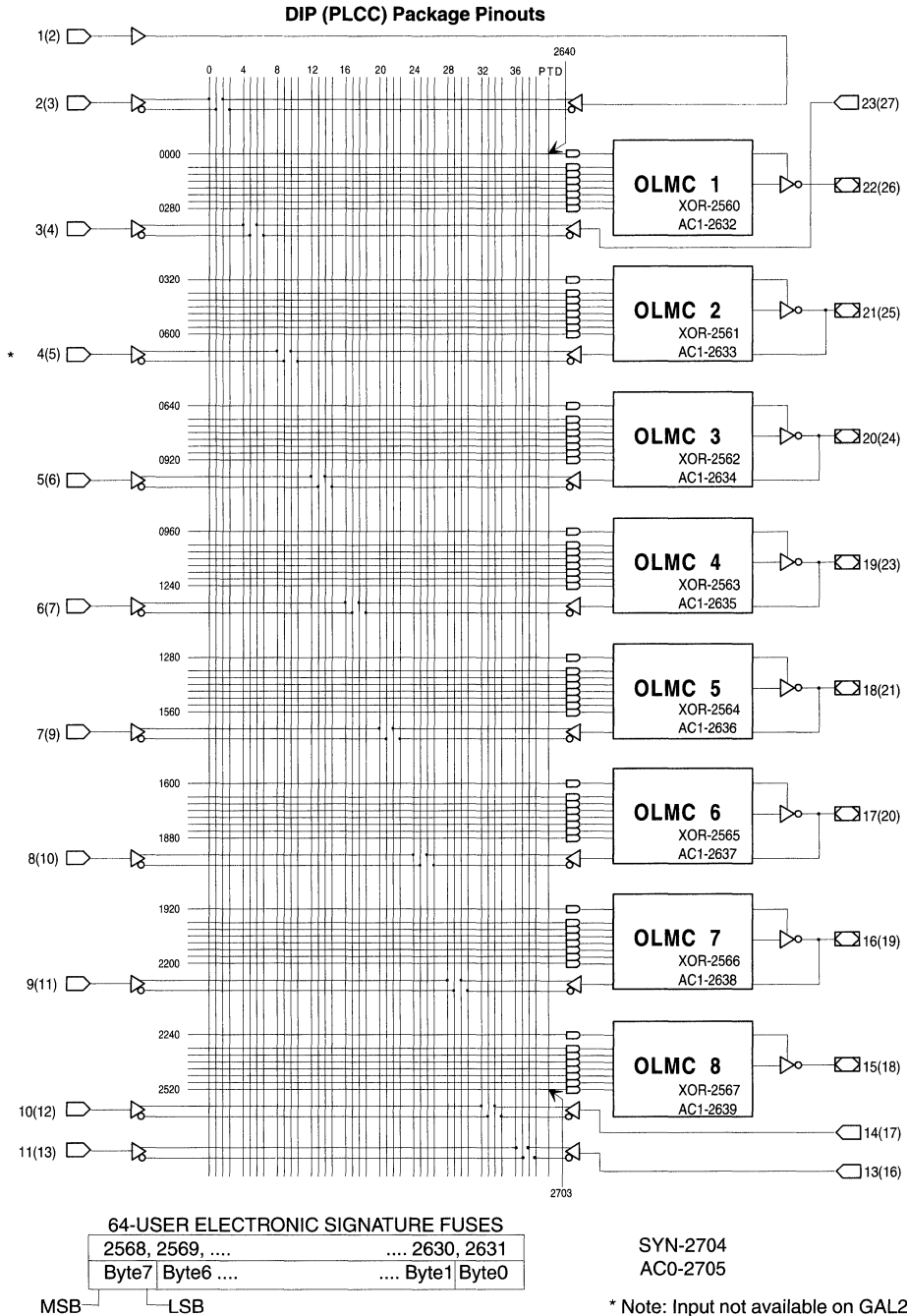


Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 15(18) and Pin 22(26) are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM



SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1(2) and 13(16) are always available as data inputs into the AND array. The center two macrocells (pins 18(21) & 19(23)) cannot be used in the input configuration.

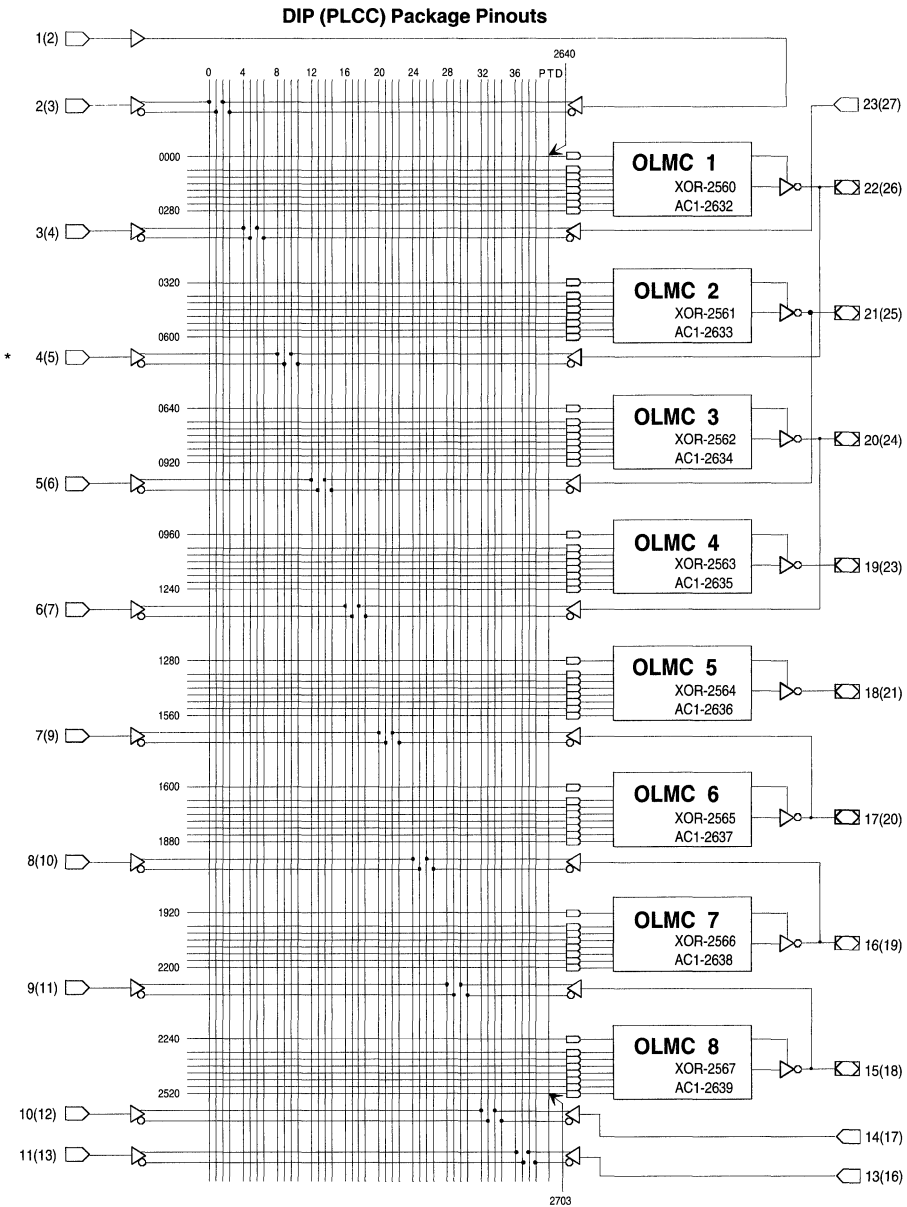
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - All OLMC except pins 18(21) & 19(23) can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - Pins 18(21) & 19(23) are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - All OLMC except pins 18(21) & 19(23) can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, 2630, 2631
Byte7 Byte6 Byte1 Byte0

MSB ———— LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
 Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
		$I_{OH} = -100 \mu A \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	$V_{CC} - 1$	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}¹	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA

COMMERCIAL

ISB	Stand-by Power Supply Current	$V_{IL} = GND \quad V_{IH} = V_{CC} \quad \text{Outputs Open}$	Z-12/-15 ZD-12/-15	—	50	100	μA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{\text{toggle}} = 15 \text{ MHz} \quad \text{Outputs Open}$	Z-12/-15 ZD-12/-15	—	—	55	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_I = 2.0V$
$C_{I/O}$	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

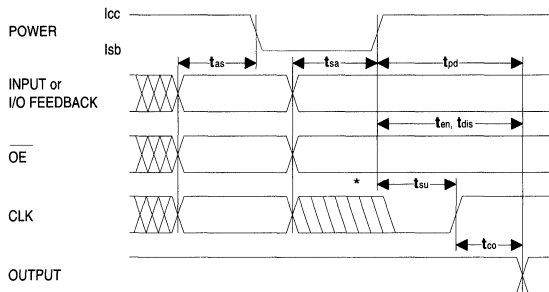
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
			t_{pd}	A	Input or I/O to Combinational Output	3	
t_{co}	A	Clock to Output Delay	2	8	2	10	ns
t_{cf}^2	—	Clock to Feedback Delay	—	6	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock \uparrow	10	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock \uparrow	0	—	0	—	ns
f_{max}^3	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	\overline{OE} to Output Enabled	—	12	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	\overline{OE} to Output Disabled	—	12	—	15	ns
t_{as}	—	Last Active Input to Standby	60	140	50	150	ns
t_{sa}^4	—	Standby to Active Output	6	13	5	15	ns

- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.
- 3) Refer to **f_{max} Specification** section.
- 4) Add t_{sa} to t_{pd} , t_{su} , t_{en} and t_{dis} when the device is coming out of standby state.

STANDBY POWER TIMING WAVEFORMS



* Note: Rising clock edges are allowed during t_{sa} but outputs are not guaranteed.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		COM		UNITS
			-12		-15		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	3	12	3	15	ns
t_{co}	A	Clock to Output Delay	2	8	2	10	ns
t_{cf}²	—	Clock to Feedback Delay	—	6	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock [↑]	10	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock [↑]	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	\overline{OE} to Output Enabled	—	12	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	\overline{OE} to Output Disabled	—	12	—	15	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.

 3) Refer to **f_{max} Specification** section.

DEDICATED POWER-DOWN PIN SPECIFICATIONS

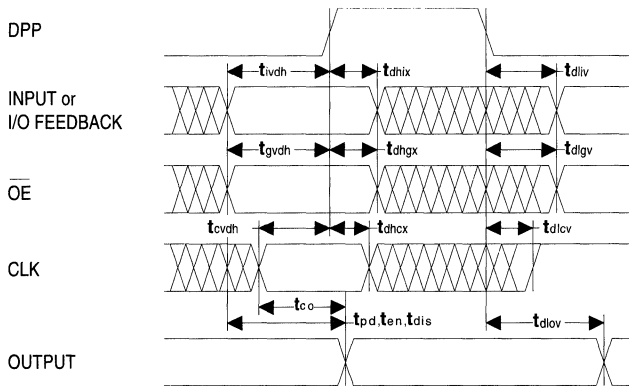
Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
			t_{whd}	—	DPP Pulse Duration High	12	
t_{wld}	—	DPP Pulse Duration Low	25	—	30	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	5	—	8	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	2	—	5	ns
t_{dhgx}	—	OE Don't Care after DPP High	—	6	—	9	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	8	—	11	ns
STANDBY TO ACTIVE							
t_{div}	—	DPP Low to Valid Input	12	—	15	—	ns
t_{dgv}	—	DPP Low to Valid OE	16	—	20	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	18	—	20	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	24	5	30	ns

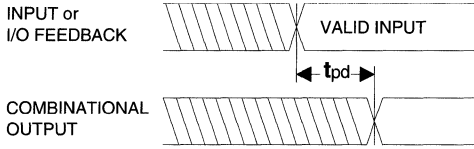
3

1) Refer to Switching Test Conditions section.

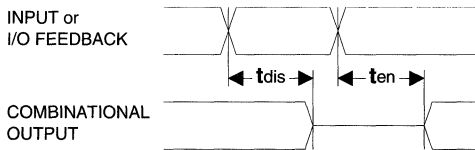
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



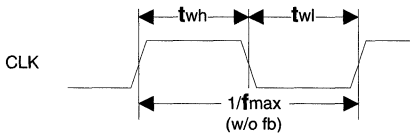
SWITCHING WAVEFORMS



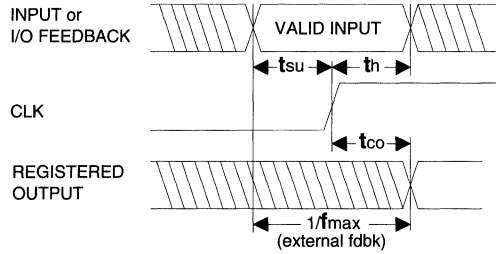
Combinatorial Output



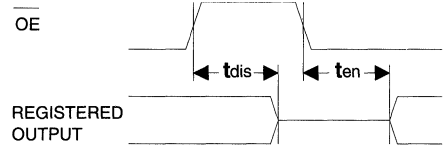
Input or I/O to Output Enable/Disable



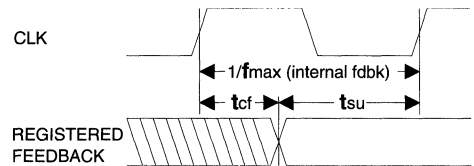
Clock Width



Registered Output

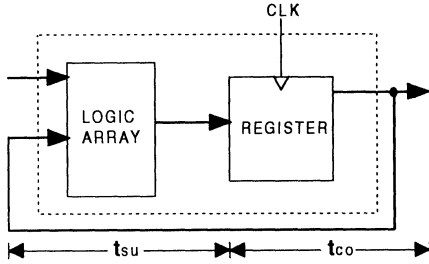


\overline{OE} to Output Enable/Disable



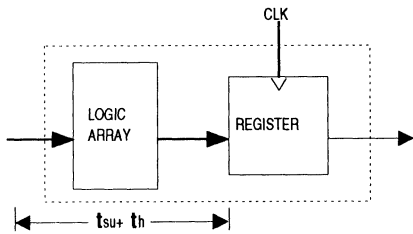
f_{max} with Feedback

f_{max} SPECIFICATIONS



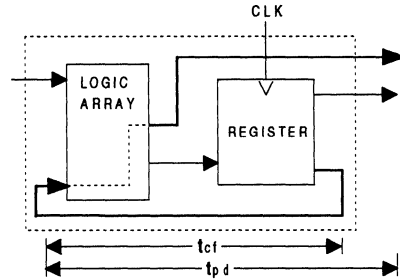
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

3

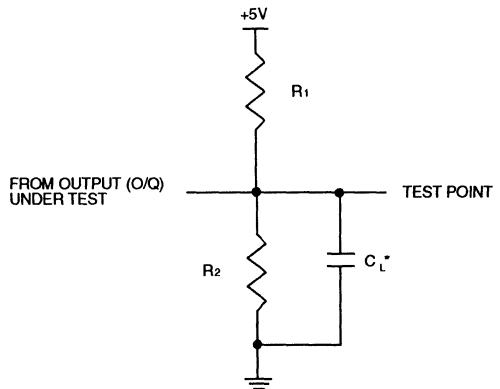
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	5pF
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20V8Z/ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

A security cell is provided in the GAL20V8Z/ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools Section of the Data Book). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

INPUT TRANSITION DETECTION (ITD)

The GAL20V8Z relies on its internal input detection circuitry to put the device in power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Any valid input transition will put the device back into active state. The first rising clock transition from power-down state only acts as a wake up signal into the device and will not clock the data input through to the output (refer to standby power timing waveform for more detail). Any input pulse widths greater than 5ns at input voltage level of 1.5V will be detected as input transition. The device will not detect any input pulse widths less than 1ns measured at input voltage level of 1.5V as input transition.

DEDICATED POWER-DOWN PIN (DPP)

The GAL20V8ZD uses pin 4 (pin 5 on PLCC) as the dedicated power-down signal to put the device in power-down state. DPP is an active high signal where logic high driven on this signal puts the device into power-down state. Input pin 4 (5) cannot be used as a functional input on this device.

OUTPUT REGISTER PRELOAD

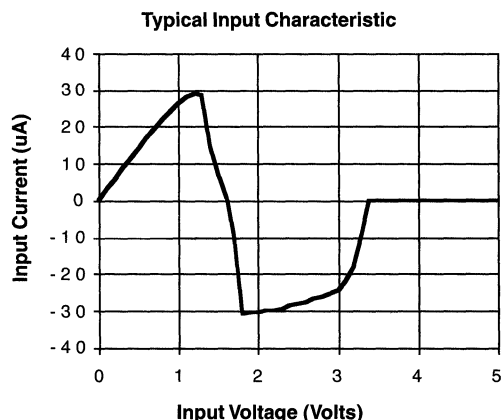
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL20V8Z/ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

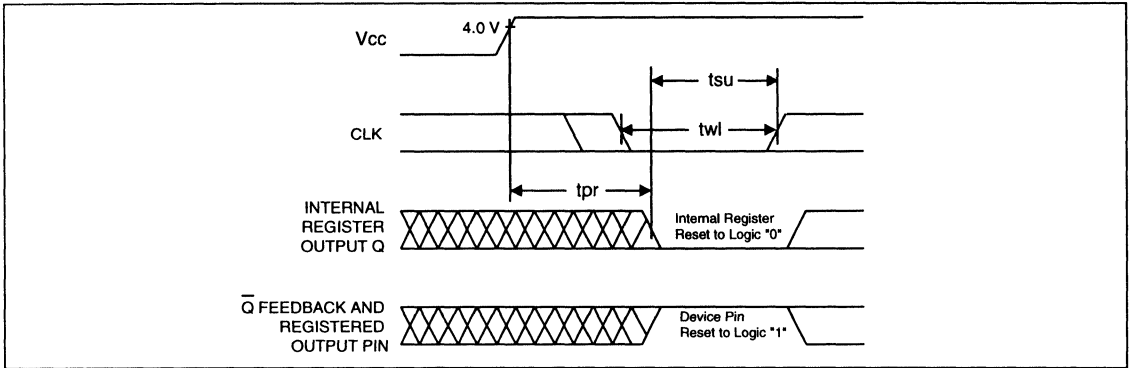
INPUT BUFFERS

GAL20V8Z/ZD devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL20V8Z/ZD input buffers have latches within the buffers. As a result, when the device goes into standby mode the inputs will be latched to its values prior to standby. In order to overcome the input latches, they will have to be driven by an external source. Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC} , or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.



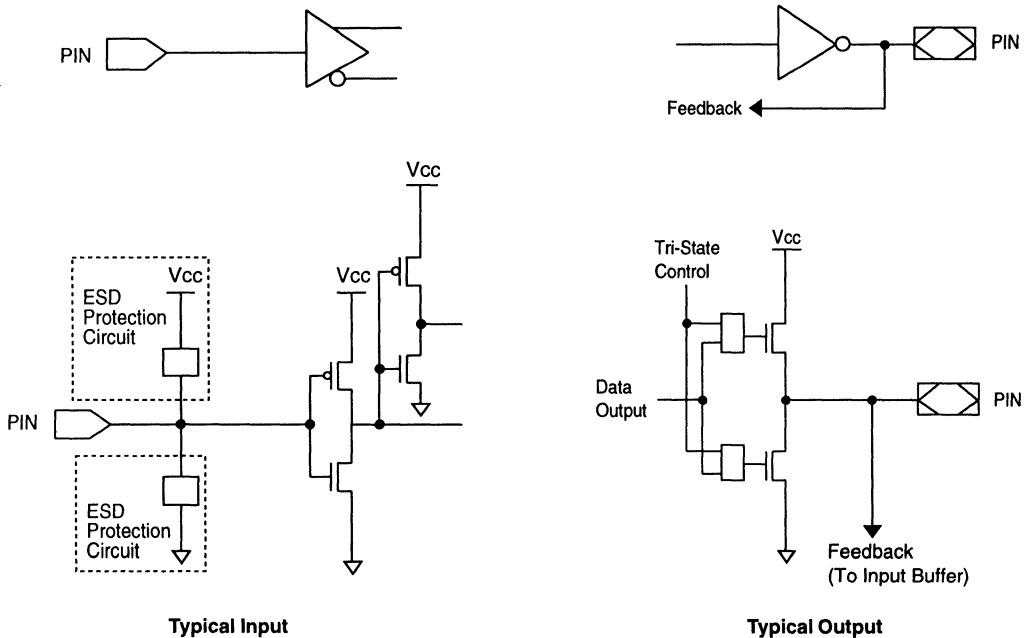
POWER-UP RESET



Circuitry within the GAL20V8Z/ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the

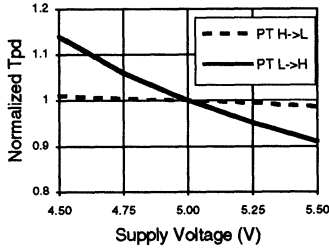
asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20V8Z/ZD. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

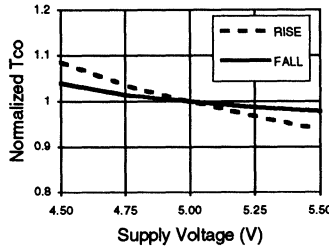


TYPICAL AC AND DC CHARACTERISTICS

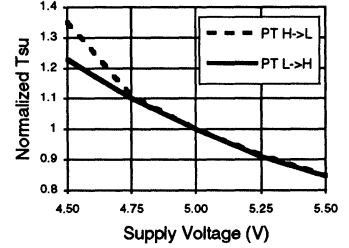
Normalized Tpd vs Vcc



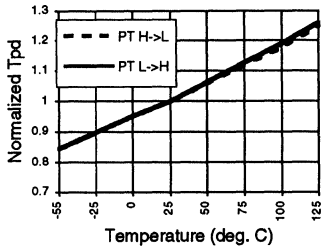
Normalized Tco vs Vcc



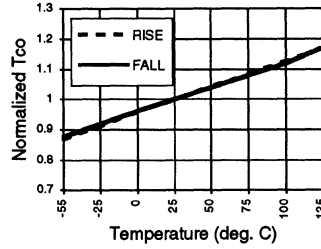
Normalized Tsu vs Vcc



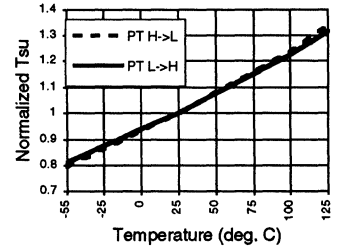
Normalized Tpd vs Temp



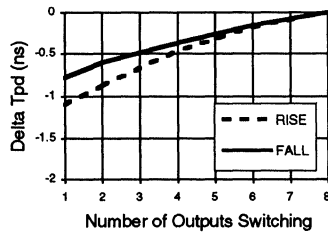
Normalized Tco vs Temp



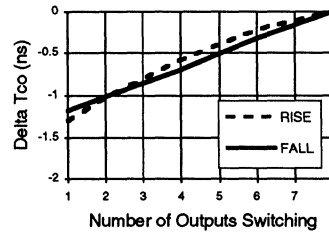
Normalized Tsu vs Temp



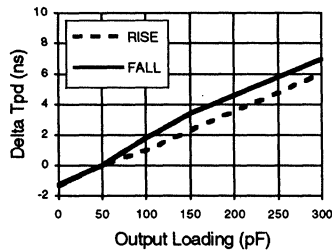
Delta Tpd vs # of Outputs Switching



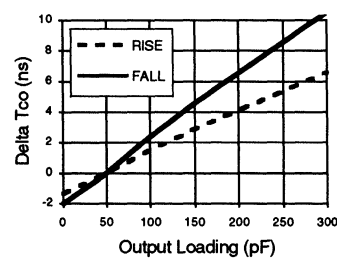
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

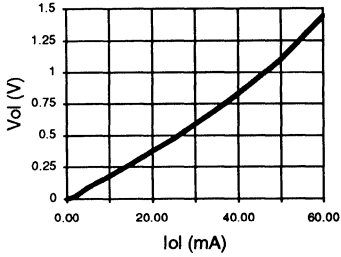


Delta Tco vs Output Loading

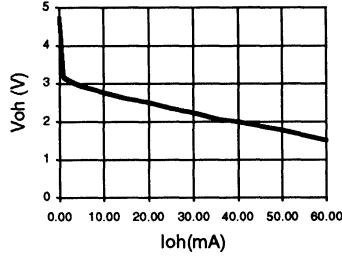


TYPICAL AC AND DC CHARACTERISTICS

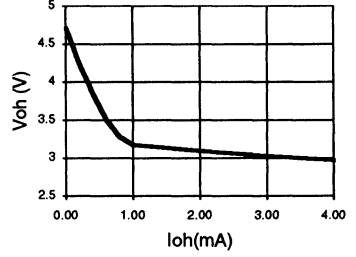
Vol vs Iol



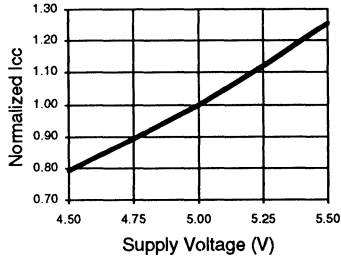
Voh vs Ioh



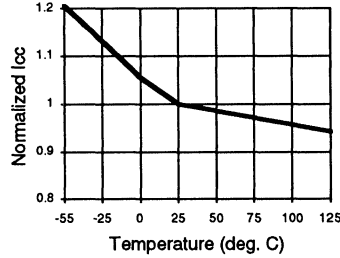
Voh vs Ioh



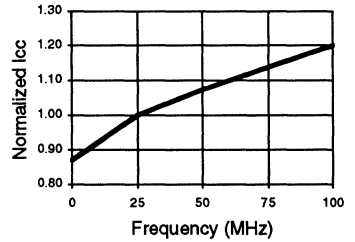
Normalized Icc vs Vcc



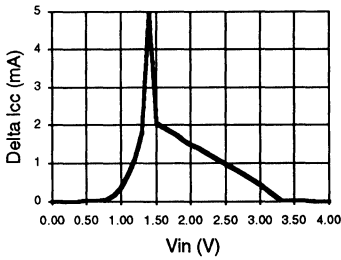
Normalized Icc vs Temp



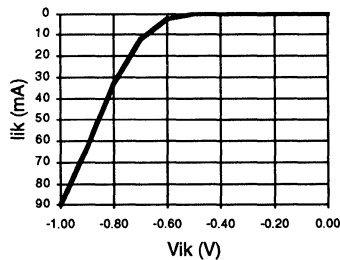
Normalized Icc vs Freq. (DPP & ITD > 10MHz)



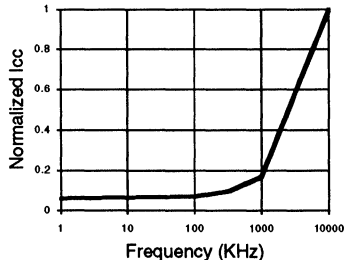
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)



FEATURES

- **HIGH DRIVE E²CMOS® GAL® DEVICE**
 - TTL Compatible 64 mA Output Drive
 - 15 ns Maximum Propagation Delay
 - F_{max} = 80 MHz
 - 10 ns Maximum from Clock Input to Data Output
 - UltraMOS® Advanced CMOS Technology
- **ENHANCED INPUT AND OUTPUT FEATURES**
 - Schmitt Trigger Inputs
 - Programmable Open-Drain or Totem-Pole Outputs
 - Active Pull-Ups on All Inputs and I/O pins
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Architecturally Compatible with Standard GAL20V8
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - Ideal for Bus Control & Bus Arbitration Logic
 - Bus Address Decode Logic
 - Memory Address, Data and Control Circuits
 - DMA Control
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

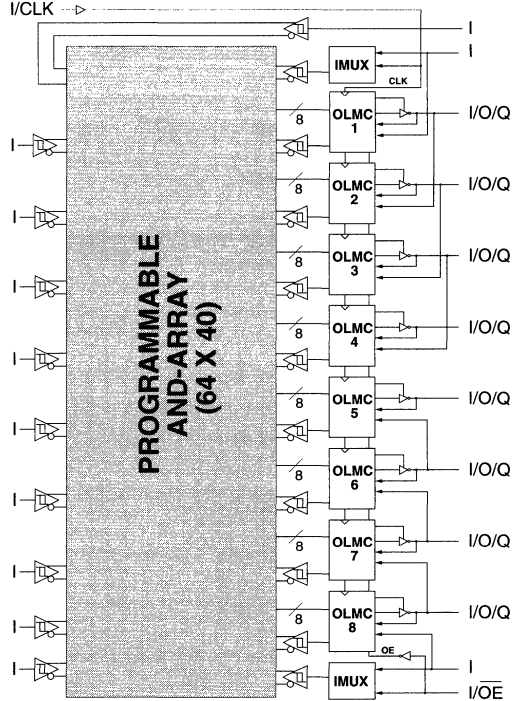
DESCRIPTION

The GAL20VP8, with 64 mA drive capability and 15 ns maximum propagation delay time is ideal for Bus and Memory control applications. The GAL20VP8 is manufactured using Lattice's advanced E²CMOS process which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

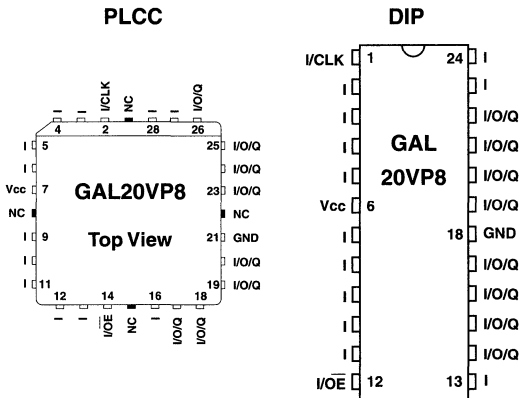
System bus and memory interfaces require control logic before driving the bus or memory interface signals. The GAL20VP8 combines the familiar GAL20V8 architecture with bus drivers as its outputs. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The 64mA output drive eliminates the need for additional devices to provide bus-driving capability.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



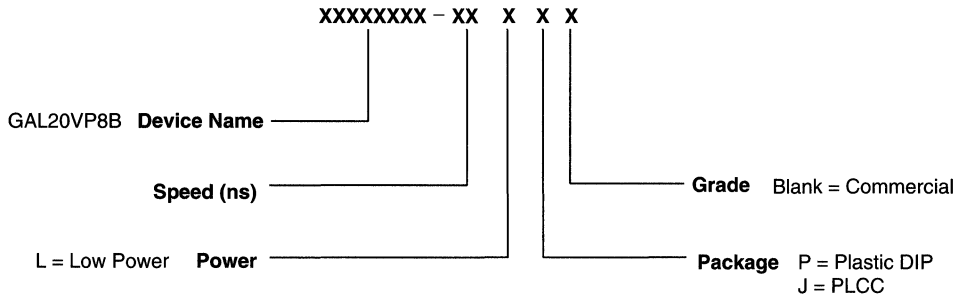
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GAL20VP8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	8	10	115	GAL20VP8B-15LP	24-Pin Plastic DIP
			115	GAL20VP8B-15LJ	28-Lead PLCC
25	10	15	115	GAL20VP8B-25LP	24-Pin Plastic DIP
			115	GAL20VP8B-25LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any

of the three modes, while the AC1 and AC2 bit of each of the macrocells controls the input/output and totem-pole/open-drain configuration. These two global and 24 individual architecture bits define all possible configurations in a GAL20VP8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

3

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1(2) and pin 12(14) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1(2) and pin 12(14) become dedicated inputs and use the feedback paths of pin 22(26) and pin 14(17) respectively. Because of this feedback path usage, pin 22(26) and pin 14(17) do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 17(20) and 19(23)) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

In addition to the architecture configurations, the logic compiler software also supports configuration of either totem-pole or open-drain outputs. The actual architecture bit configuration, again, is transparent to the user with the default configuration being the standard totem-pole output.

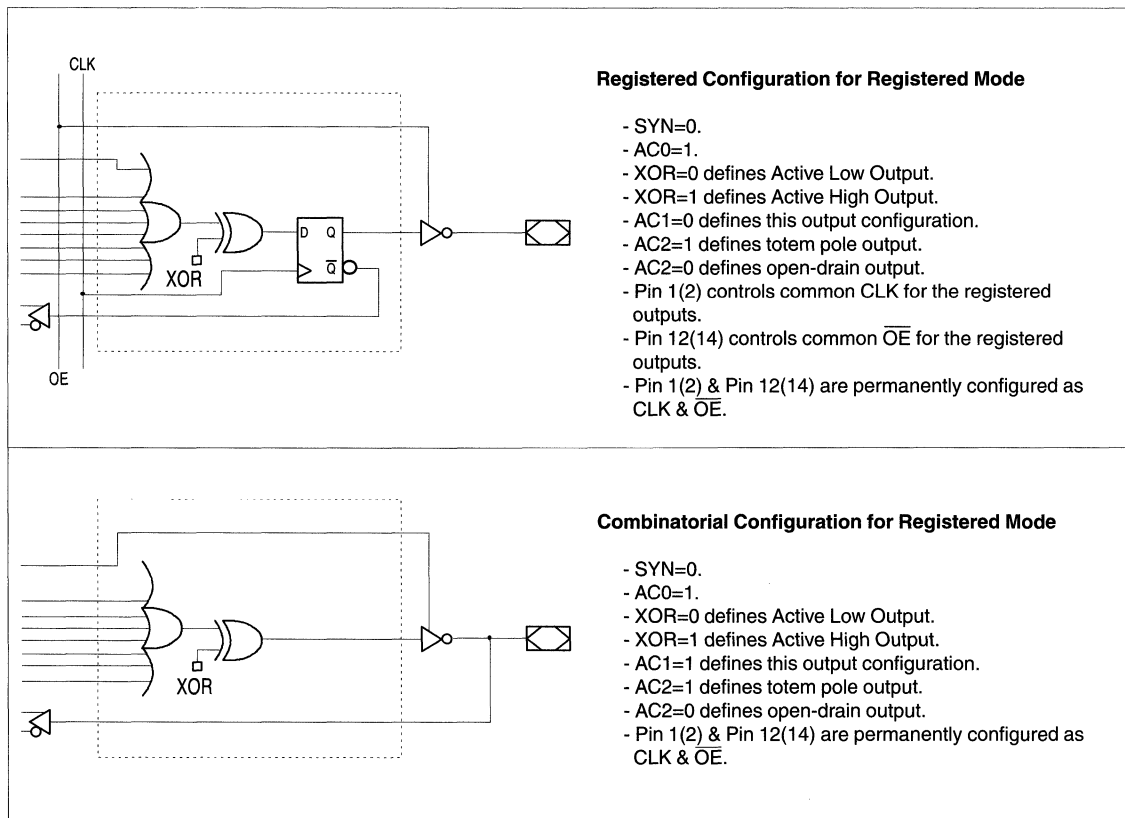
REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

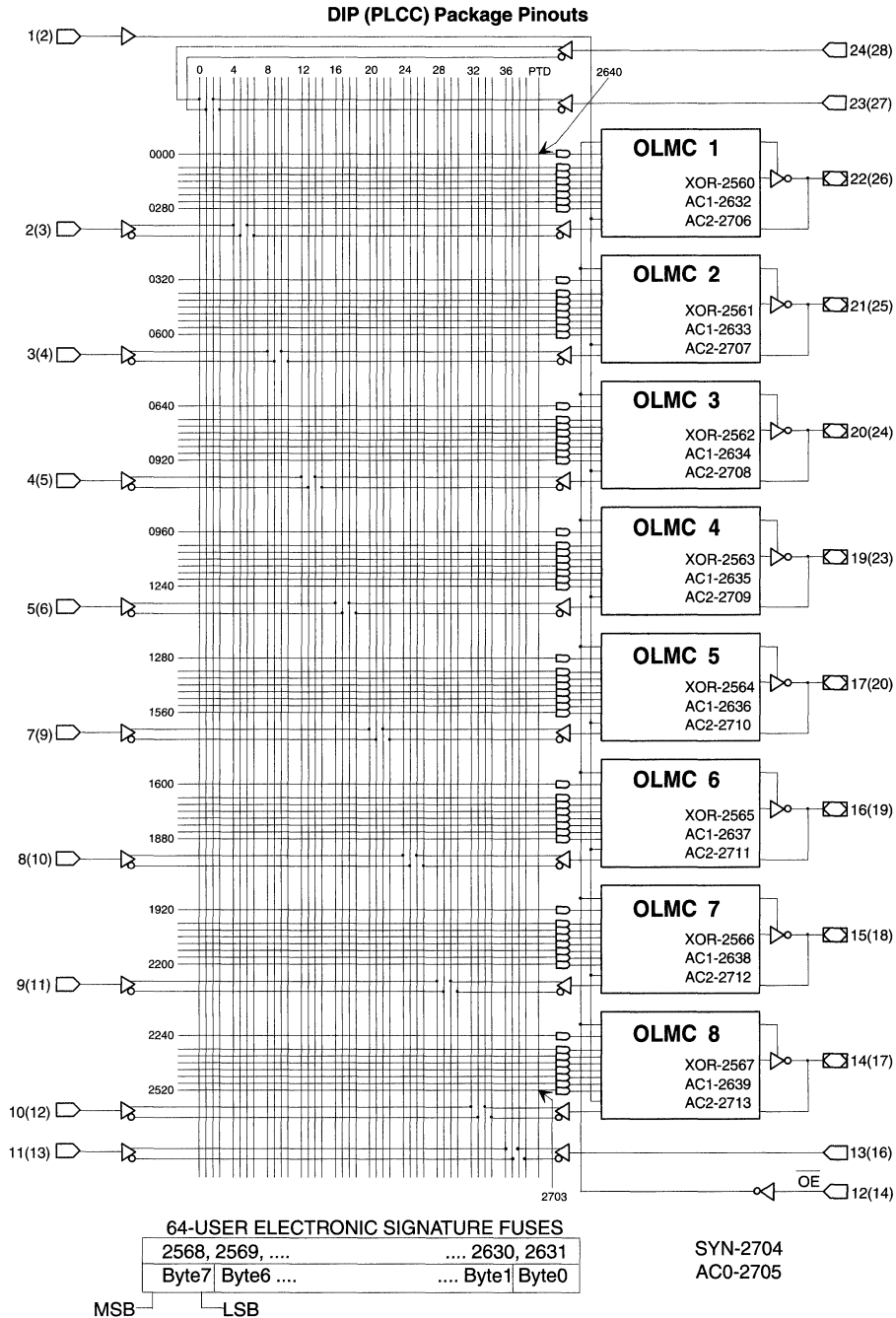
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM



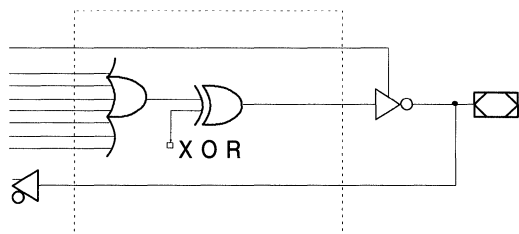
COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 14(17) & 22(26)) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

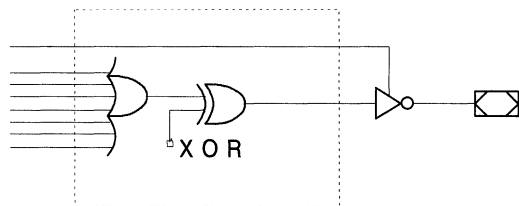
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1(2) and 12(14) are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 15(18) through Pin 21(25) are configured to this function.

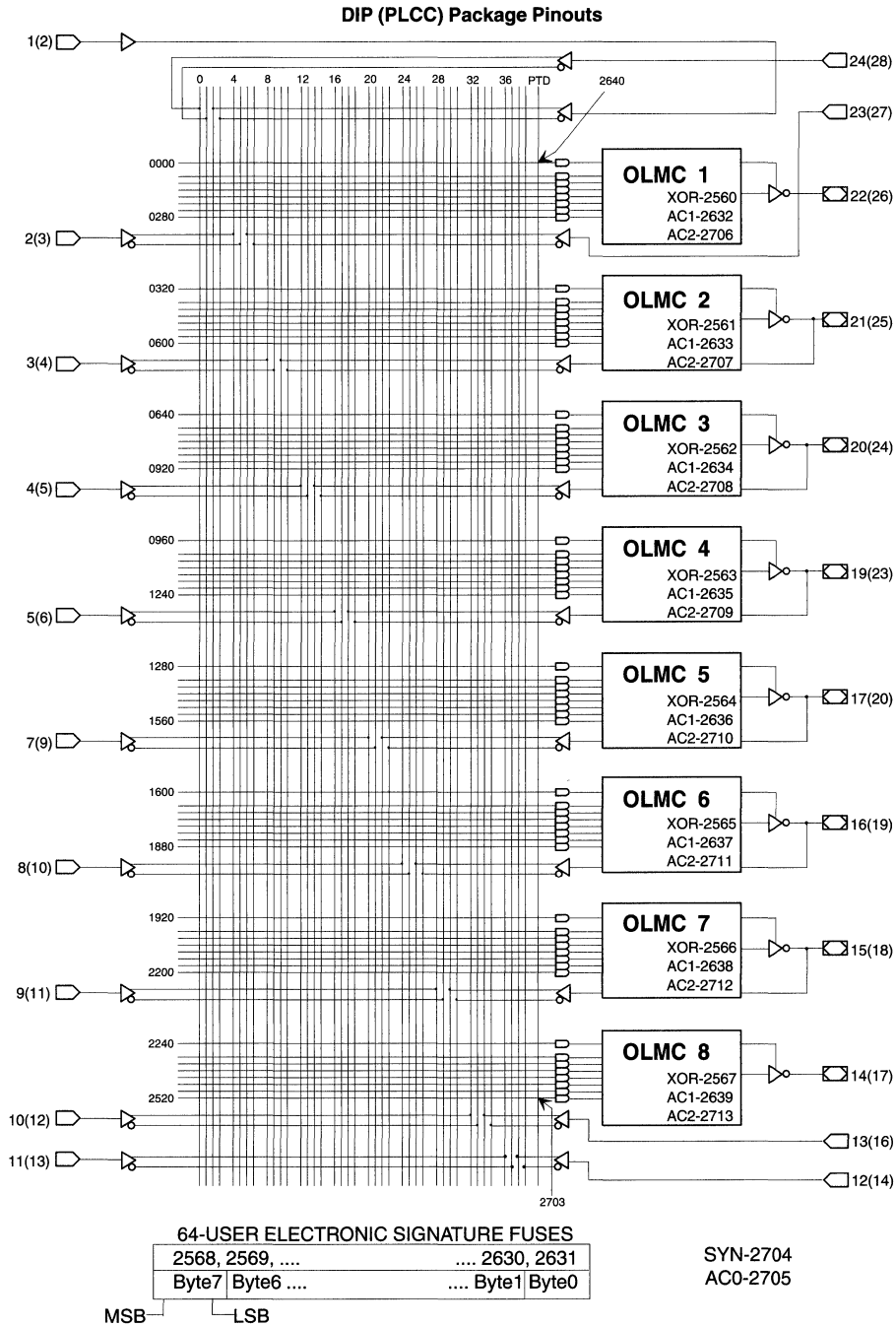


Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 14(17) and Pin 22(26) are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM



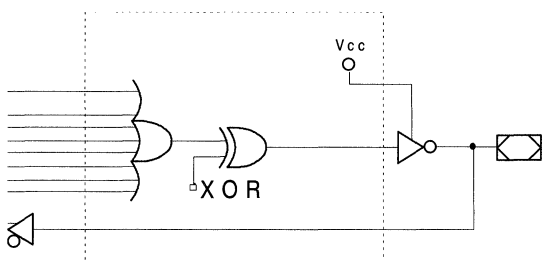
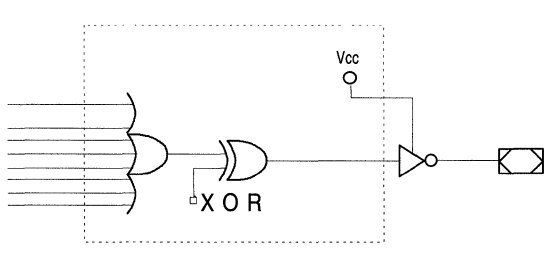
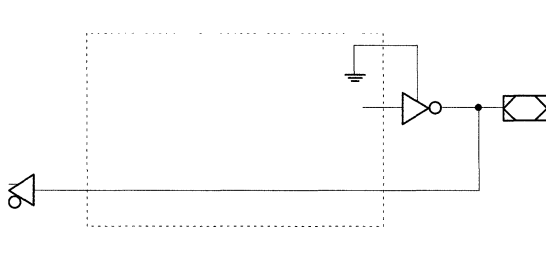
SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

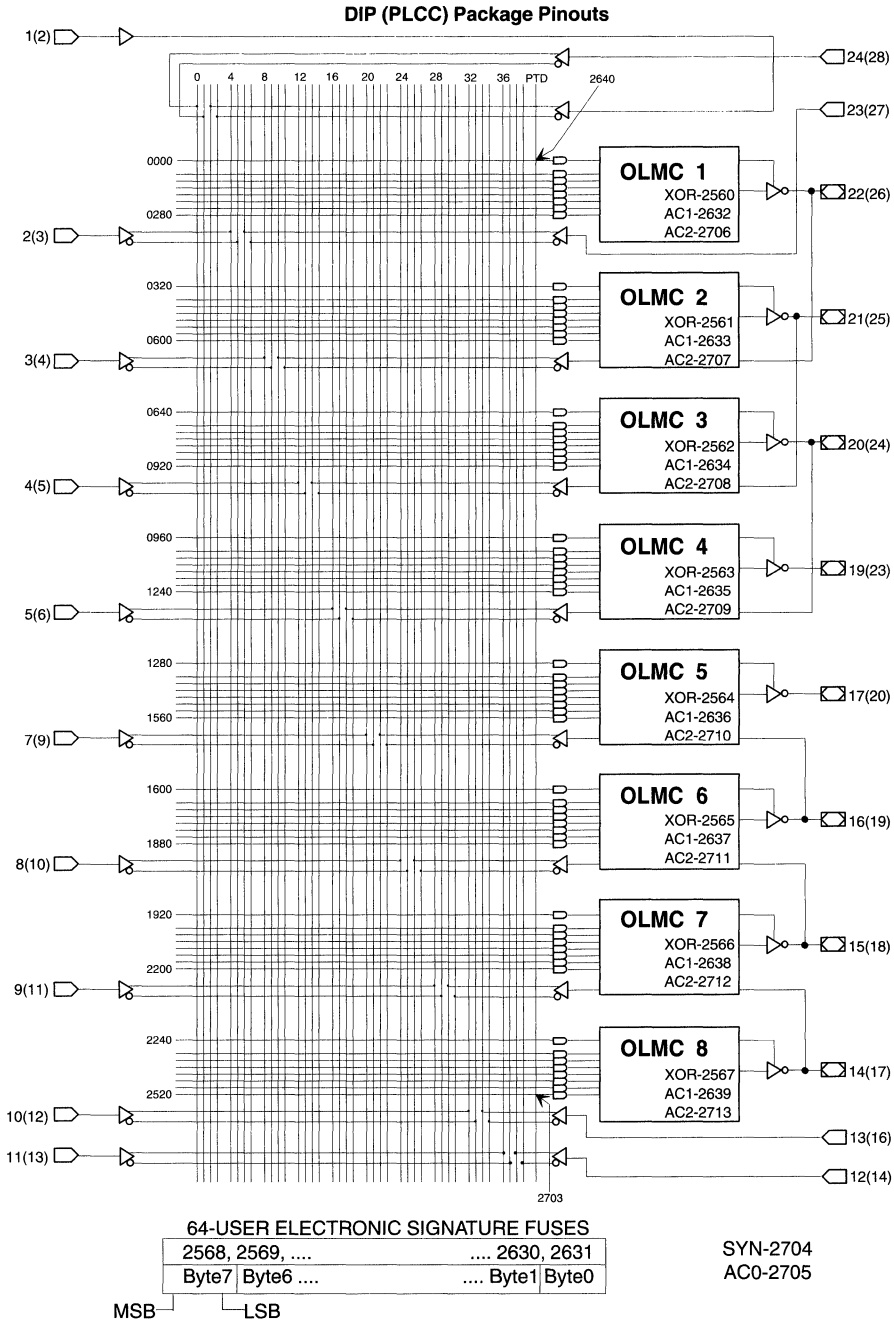
Pins 1(2) and 12(14) are always available as data inputs into the AND array. The center two macrocells (pins 17(20) & 19(23)) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - AC2=1 defines totem pole output. - AC2=0 defines open-drain output. - All OLMC except pins 17(20) & 19(23) can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - AC2=1 defines totem pole output. - AC2=0 defines open-drain output. - Pins 17(20) & 19(23) are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - AC2=1 defines totem pole output. - AC2=0 defines open-drain output. - All OLMC except pins 17(20) & 19(23) can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾ RECOMMENDED OPERATING COND.

Supply voltage V_{CC} -5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

Commercial Devices:
 Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ⁴	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
V_I¹	Input Clamp Voltage	$V_{CC} = \text{Min. } I_{IN} = -32\text{mA}$	—		-1.2	V
I_{IL}²	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (\text{MAX.})$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = \text{MAX. } V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = \text{MAX. } V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	64	mA
I_{OH}	High Level Output Current		—	—	-32	mA
I_{OS}³	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-60	—	-400	mA

COMMERCIAL

I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	L -15/-25	—	90	115	mA
	Supply Current	$f_{toggle} = 15\text{MHz}$ Outputs Open					

- 1) Guaranteed but not 100% tested.
- 2) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
- 3) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- 4) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		COM		UNITS
			-15		-25		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	3	15	3	25	ns
t_{co}	A	Clock to Output Delay	2	10	2	15	ns
t_{cf}²	—	Clock to Feedback Delay	—	4.5	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock ↑	8	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock ↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	55.5	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	80	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	80	—	50	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	10	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	10	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	ns
	B	$\overline{\text{OE}}$ to Output Enabled	—	12	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	ns
	C	$\overline{\text{OE}}$ to Output Disabled	—	12	—	15	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.

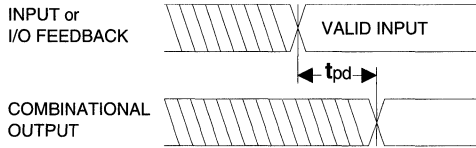
 3) Refer to **f_{max} Specification** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

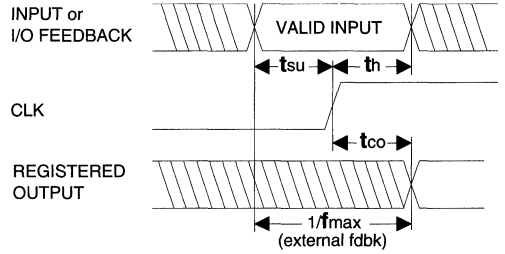
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _i	Input Capacitance	10	pF	V _{cc} = 5.0V, V _i = 2.0V
C _{i/o}	I/O Capacitance	15	pF	V _{cc} = 5.0V, V _{i/o} = 2.0V

*Guaranteed but not 100% tested.

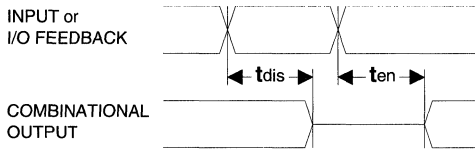
SWITCHING WAVEFORMS



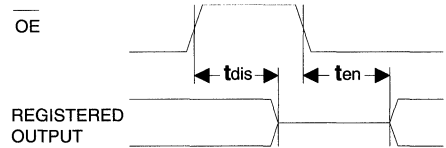
Combinatorial Output



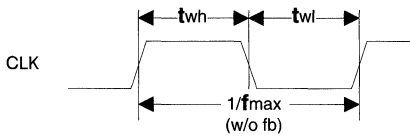
Registered Output



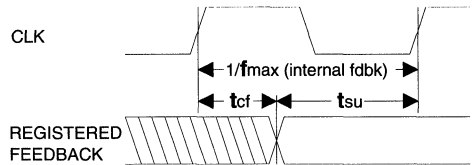
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

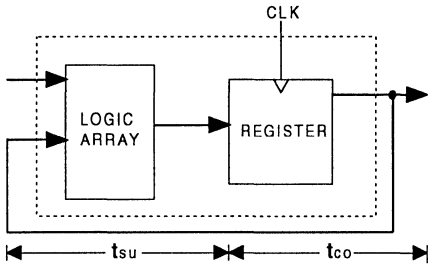


Clock Width



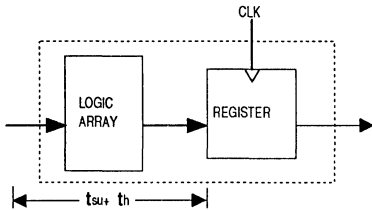
fmax with Feedback

f_{max} DESCRIPTIONS



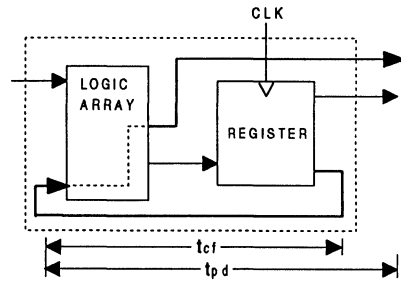
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured tsu and tco.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting tsu from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to t_{cf} + t_{pd}.

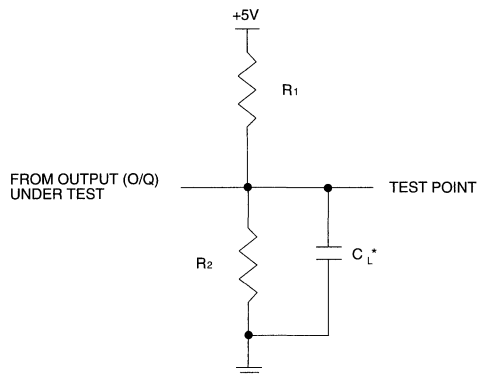
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L *
A	500Ω	500Ω	50pF
B	Active High	∞	500Ω
	Active Low	500Ω	500Ω
C	Active High	∞	500Ω
	Active Low	500Ω	500Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20VP8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

The security cell is provided on all GAL20VP8 devices to prevent unauthorized copying of the array patterns. Once programmed, the circuitry enabling array is disabled, preventing further programming or verification of the array. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

GAL20VP8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

BULK ERASE MODE

During a programming cycle, a clear function performs a bulk erase of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its original state, which is all JEDEC ones.

SCHMITT TRIGGER INPUTS

One of the enhancements of the GAL20VP8 for bus interface logic implementation is input hysteresis. The threshold of the positive going edge is 1.5V, while the threshold of the negative going edge is 1.3V. This provides a typical hysteresis of 200mV between positive and negative transitions of the inputs.

HIGH DRIVE OUTPUTS

All eight outputs of the GAL20VP8 are capable of driving 64 mA loads when driving low and 32 mA loads when driving high. Near symmetrical high and low output drive capability provides small skews between high-to-low and low-to-high output transitions.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

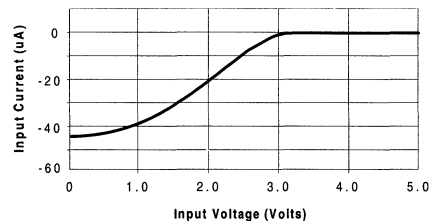
The GAL20VP8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors can perform output register preload automatically.

INPUT BUFFERS

The GAL20VP8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL20VP8 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC} , or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

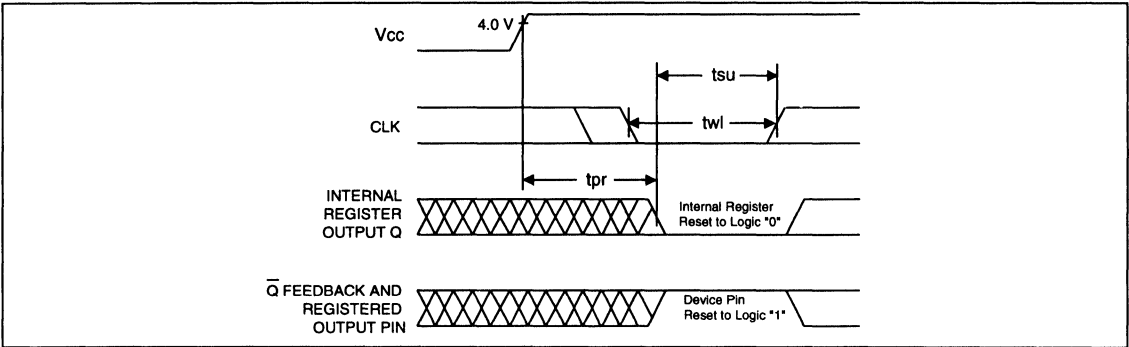
Typical Input Pull-up Characteristic



PROGRAMMABLE OPEN-DRAIN OUTPUTS

In addition to the standard GAL20V8 type configuration, the outputs of the GAL20VP8 are individually programmable either as a standard totempole output or an open-drain output. The totempole output drives the specified V_{OH} and V_{OL} levels whereas the open-drain output drives only the specified V_{OL} . The V_{OH} level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by the AC2 fuse. When AC2 cell is erased (JEDEC "1") the output is configured as a totempole output and when AC2 cell is programmed (JEDEC "0") the output is configured as an open-drain. The default configuration when the device is in bulk erased state is totempole configuration. The AC2 fuses associated with each of the outputs is included in all of the logic diagrams.

POWER-UP RESET

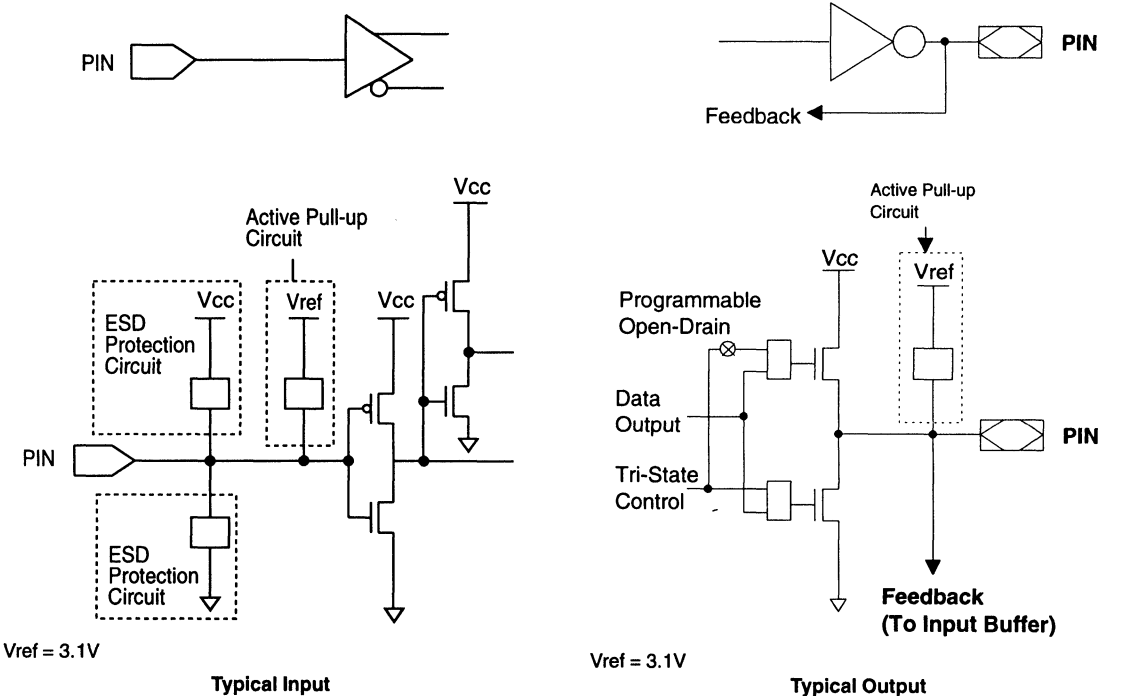


3

Circuitry within the GAL20VP8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown above. Because of the asynchro-

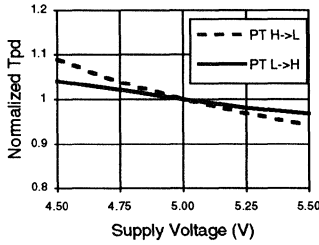
nous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20VP8. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

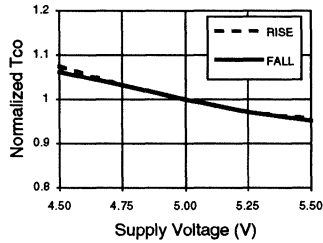


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

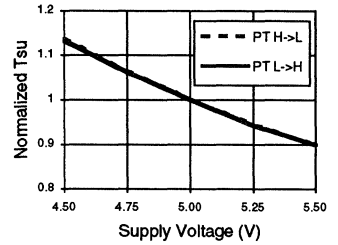
Normalized Tpd vs Vcc



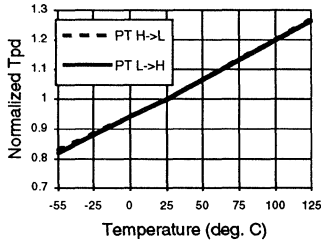
Normalized Tco vs Vcc



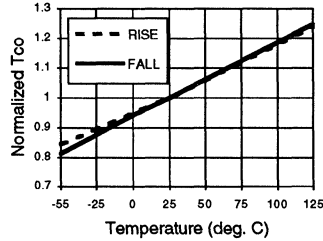
Normalized Tsu vs Vcc



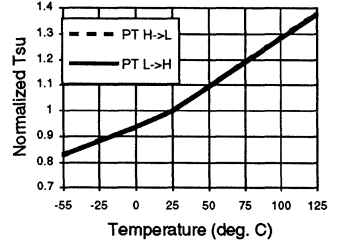
Normalized Tpd vs Temp



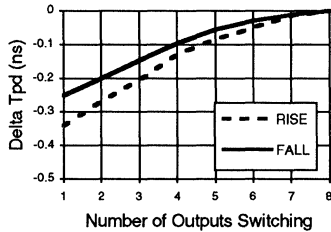
Normalized Tco vs Temp



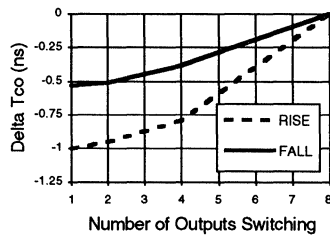
Normalized Tsu vs Temp



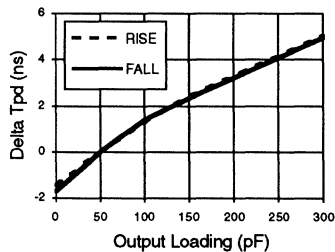
Delta Tpd vs # of Outputs Switching



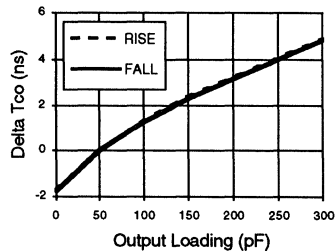
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

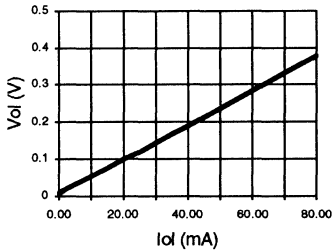


Delta Tco vs Output Loading

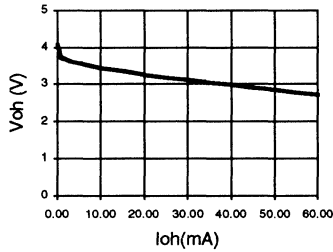


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

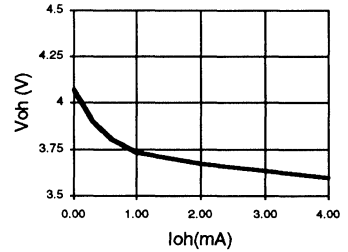
Vol vs Iol



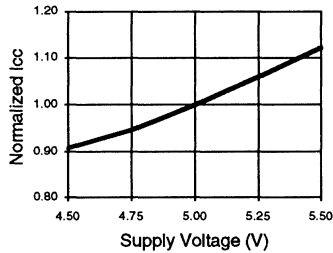
Voh vs Ioh



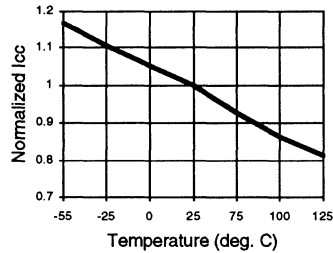
Voh vs Ioh



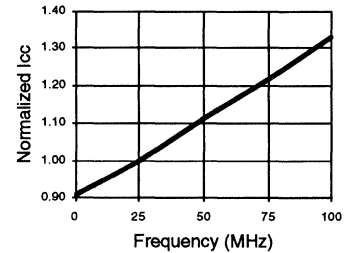
Normalized Icc vs Vcc



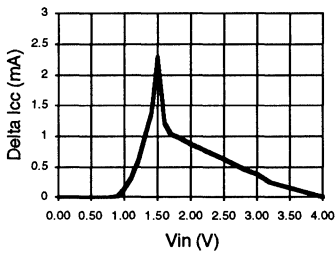
Normalized Icc vs Temp



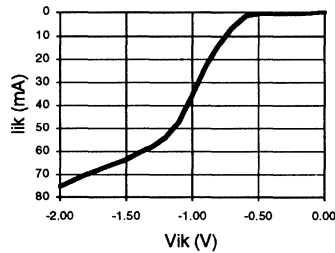
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 10 ns Maximum Propagation Delay
 - F_{max} = 100 MHz
 - 7 ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 90mA Max I_{cc}
 - 75mA Typ I_{cc}
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100 ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - XOR Gate Capability on all Outputs
 - Full Function and Parametric Compatibility with PAL12L10, 20L10, 20X10, 20X8, 20X4
 - Registered or Combinatorial with Polarity
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
- **APPLICATIONS INCLUDE:**
 - High Speed Counters
 - Graphics Processing
 - Comparators
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

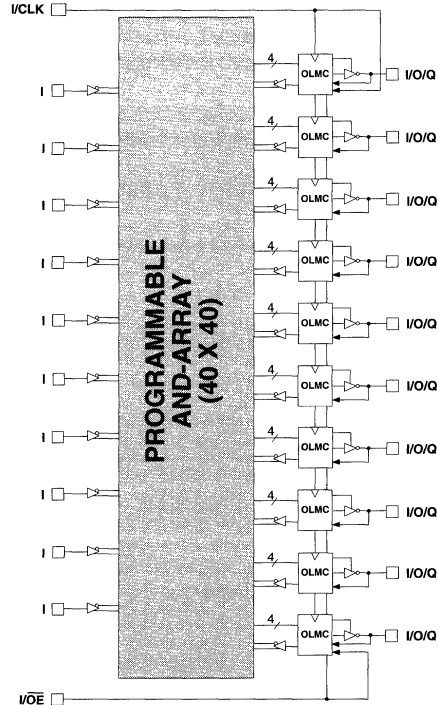
DESCRIPTION

The GAL20XV10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed Exclusive-OR PLD available in the market. At 90mA maximum I_{cc} (75mA typical I_{cc}), the GAL20XV10 provides a substantial savings in power when compared to bipolar counterparts. E²CMOS technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20XV10 are the PAL® architectures listed in the macrocell description section of this document. The GAL20XV10 is capable of emulating these PAL architectures with full function and parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

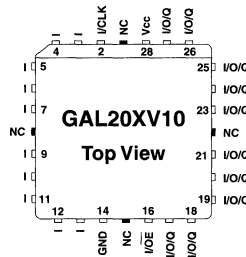
FUNCTIONAL BLOCK DIAGRAM



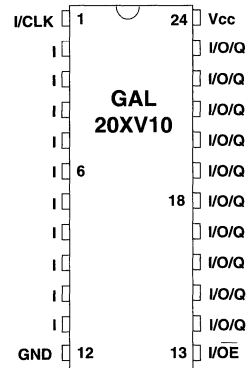
3

PACKAGE DIAGRAMS

PLCC



DIP



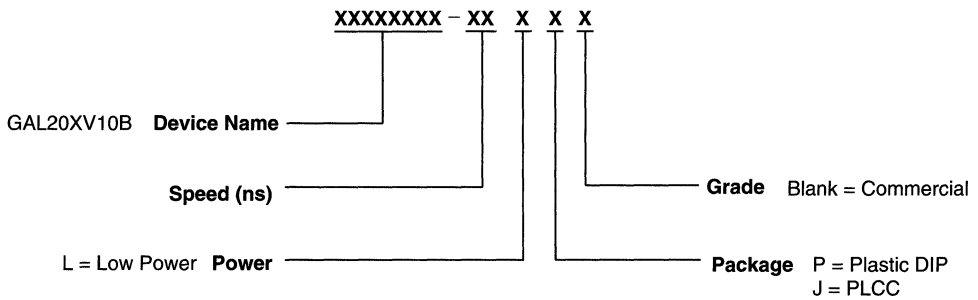
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GAL20XV10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	6	7	90	GAL20XV10B-10LP	24-Pin Plastic DIP
				GAL20XV10B-10LJ	28-Lead PLCC
15	8	8	90	GAL20XV10B-15LP	24-Pin Plastic DIP
				GAL20XV10B-15LJ	28-Lead PLCC
20	10	10	90	GAL20XV10B-20LP	24-Pin Plastic DIP
				GAL20XV10B-20LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the Output Logic Macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The GAL20XV10 has two global architecture configurations that allow it to emulate PAL architectures. The Input mode emulates combinatorial PAL devices, with the I/CLK and I/OE pins used as inputs. The Feedback mode emulates registered PAL devices with the I/CLK pin used as the register clock and the I/OE pin as an output enable for all registers. The following is a list of PAL architectures that the GAL20XV10 can emulate. It also shows the global architecture mode used to emulate the PAL architecture.

PAL Architectures Emulated by GAL20XV10	GAL20XV10 Global OLMC Mode
PAL12L10	Input Mode
PAL20L10	Input Mode
PAL20X10	Feedback Mode
PAL20X8	Feedback Mode
PAL20X4	Feedback Mode

INPUT MODE

The Input mode architecture is defined when the global architecture bit SYN = 1. In this mode, the I/CLK pin becomes an input to the AND array and also provides the clock source for all registers. The I/OE pin becomes an input into the AND array and provides the output enable control for any macrocell configured as an Exclusive-OR function. Feedback into the AND array is provided from macrocells 2 through 9 only. In this mode, macrocells 1 and 10 have no feedback into the AND array.

FEEDBACK MODE

The Feedback mode architecture is defined when the global architecture bit SYN = 0. In this mode the I/CLK pin becomes a dedicated clock source for all registers. The I/OE pin is a dedicated output enable control for any macrocell configured as an Exclusive-OR function. The I/CLK and I/OE pins are not available to the AND array in this mode. Feedback into the AND array is provided on all macrocells 1 through 10.

FEATURES

Each Output Logic Macrocell has four possible logic function configurations controlled by architecture control bits AC0 and AC1. Four product terms are fed into each macrocell.

XOR REGISTERED CONFIGURATION

The Macrocell is set to the Exclusive-OR Registered configuration when AC0 = 0 and AC1 = 0. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed into a D-type register. The register is clocked by the low-to-high transition of the I/CLK pin. The inverting output buffer is enabled by the I/OE pin, which is an active low output enable common to all

Exclusive-OR macrocells. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

REGISTERED CONFIGURATION

The Macrocell is set to Registered configuration when AC0 = 1 and AC1 = 0. Three of the four product terms are used as sum-of-product terms for the D input of the register. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. The XOR bit controls the polarity of the output. The register is clocked by the low-to-high transition of the I/CLK. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

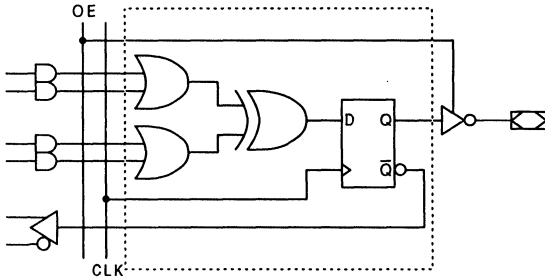
XOR COMBINATORIAL CONFIGURATION

The Macrocell is set to the Exclusive-OR Combinatorial configuration when AC0 = 0 and AC1 = 1. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed to an output buffer. The inverting output buffer is enabled by the I/OE pin, which is an active low output enable that is common to all XOR macrocells. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

COMBINATORIAL CONFIGURATION

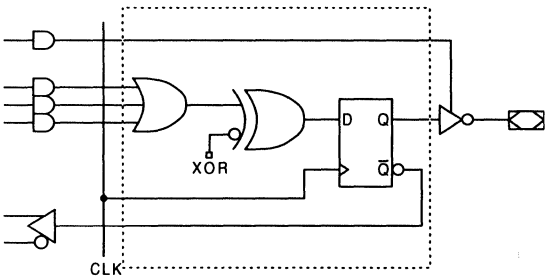
The Macrocell is set to Combinatorial mode when AC0 = 1 and AC1 = 1. Three of the four product terms are used as sum-of-product terms for the combinatorial output. The XOR bit controls the polarity of the output. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

INPUT MODE



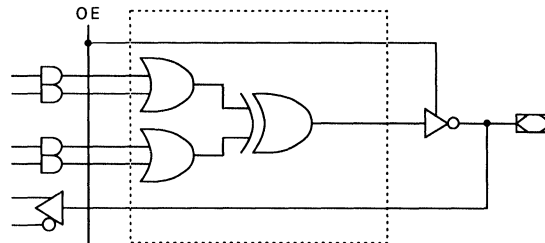
XOR Registered Configuration

- SYN = 1.
- AC0 = 0.
- AC1 = 0.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- Pin 13(16) can be OE and/or Input.



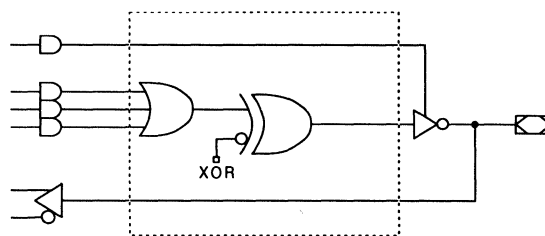
Registered Configuration

- SYN = 1.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- OE controlled by product term.



XOR Combinatorial Configuration

- SYN = 1.
- AC0 = 0.
- AC1 = 1.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 13(16) can be OE and/or Input.

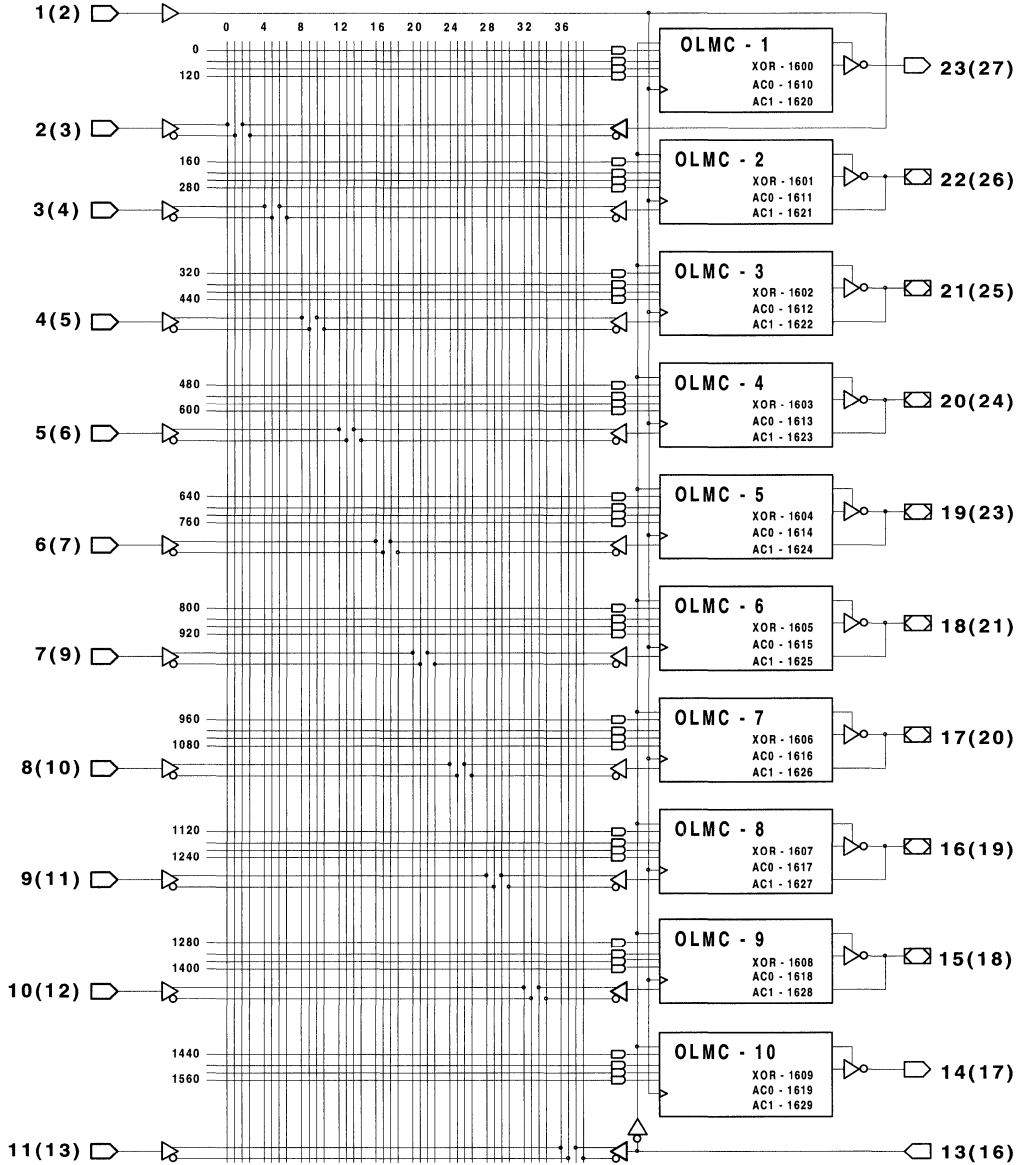


Combinatorial Configuration

- SYN = 1.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- OE controlled by product term.

INPUT MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinout



40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, 1669, 1670
Byte4 Byte3 Byte1 Byte0

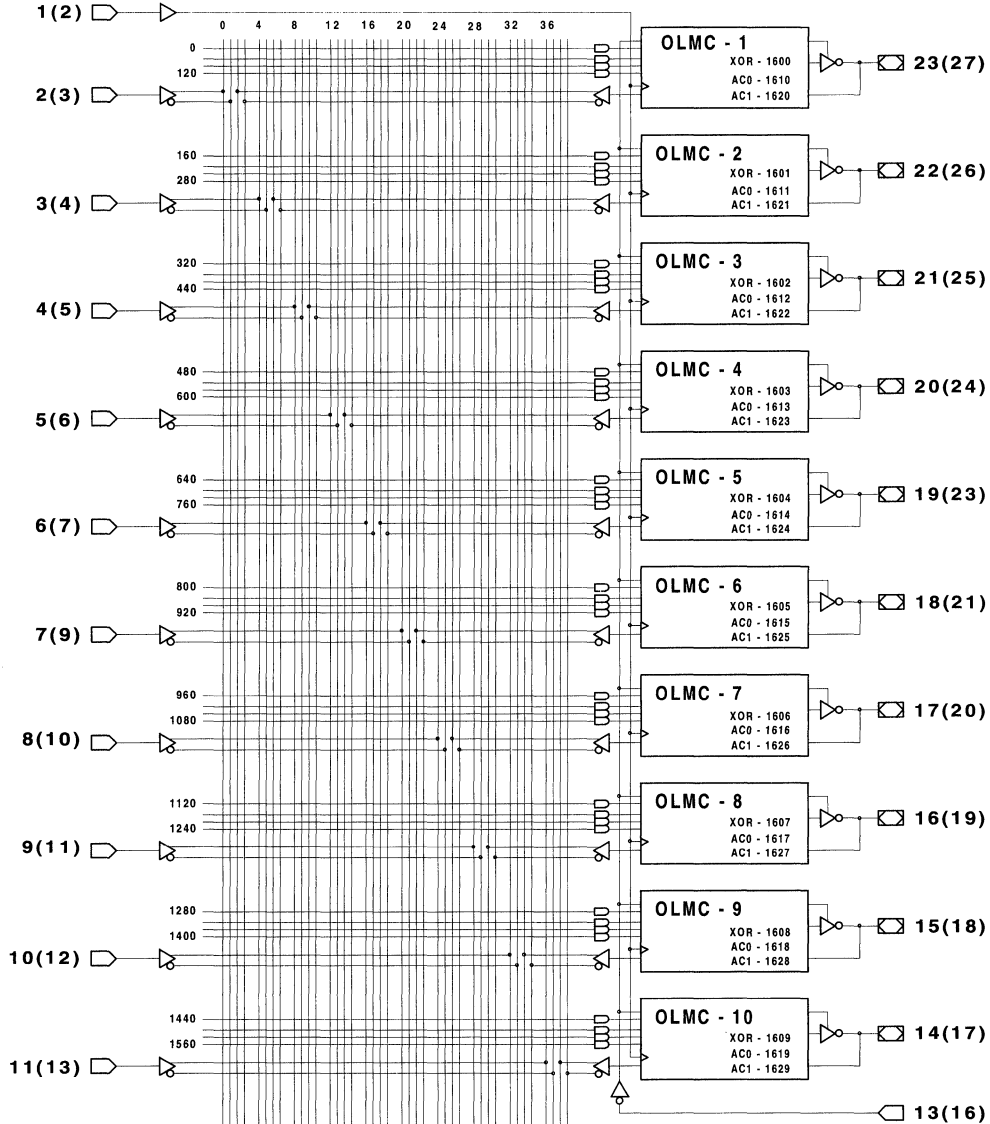
SYN - 1630

FEEDBACK MODE

	<p>XOR Registered Configuration</p> <ul style="list-style-type: none"> - SYN = 0. - AC0 = 0. - AC1 = 0. - Dedicated CLK input on Pin 1(2). - Dedicated \overline{OE} input on Pin 13(16).
	<p>Registered Configuration</p> <ul style="list-style-type: none"> - SYN = 0. - AC0 = 1. - AC1 = 0. - XOR = 1 defines Active Low Output. - XOR = 0 defines Active High Output. - Dedicated CLK input on Pin 1(2). - OE controlled by product term. - Pin 13(16) is not connected to this configuration.
	<p>XOR Combinatorial Configuration</p> <ul style="list-style-type: none"> - SYN = 0. - AC0 = 0. - AC1 = 1. - Dedicated \overline{OE} input on Pin 13(16). - Pin 1(2) is not connected to this configuration.
	<p>Combinatorial Configuration</p> <ul style="list-style-type: none"> - SYN = 0. - AC0 = 1. - AC1 = 1. - XOR = 1 defines Active Low Output. - XOR = 0 defines Active High Output. - OE controlled by product term. - Both pin1(2) and pin 13(16) are not connected to this configuration.

FEEDBACK MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinout



40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, 1669, 1670
Byte4 Byte3 Byte1 Byte0

SYN - 1630

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC}	-0.5 to +7V
Input voltage applied	-2.5 to $V_{CC} + 1.0V$
Off-state output voltage applied	-2.5 to $V_{CC} + 1.0V$
Storage Temperature	-65 to 150°C
Ambient Temperature with Power Applied	-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A)	0 to +75°C
Supply voltage (V_{CC}) with Respect to Ground	+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-150	mA

COMMERCIAL

I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	L -10/-15/-20	—	75	90	mA
	Supply Current	$f_{toggle} = 15MHz \text{ Outputs Open}$					

- 1) The leakage current is due to the internal pull-up on all input and I/O pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	COM		COM		COM		UNITS
			-10		-15		-20		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	3	10	3	15	3	20	ns
t_{co}	A	Clock to Output Delay	2	7	2	8	2	10	ns
t_{cf}²	—	Clock to Feedback Delay	—	4	—	4	—	4	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	6	—	8	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	76.9	—	62.5	—	50	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	100	—	83.3	—	71.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	83.3	—	71.4	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	6	—	7	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	6	—	7	—	ns
t_{en}	B	Input or I/O to Output Enabled	3	10	3	15	3	20	ns
	B	\overline{OE} to Output Enabled	2	9	2	10	2	15	ns
t_{dis}	C	Input or I/O to Output Disabled	3	9	3	15	3	20	ns
	C	\overline{OE} to Output Disabled	2	9	2	10	2	15	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

 3) Refer to **f_{max} Description** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

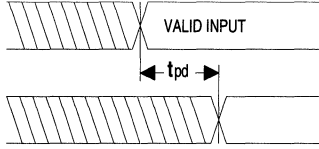
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V _{CC} = 5.0V, V _I = 2.0V
C_{I/O}	I/O Capacitance	8	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

3

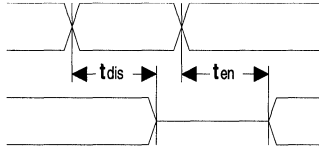
SWITCHING WAVEFORMS

INPUT or
I/O FEEDBACK



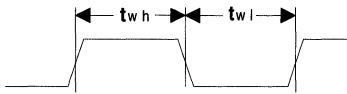
Combinatorial Output

INPUT or
I/O FEEDBACK



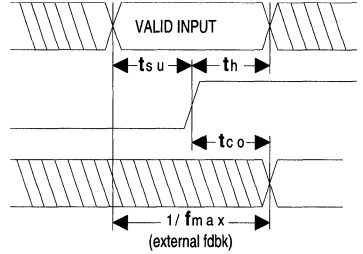
Input or I/O Feedback to Enable/Disable

CLK



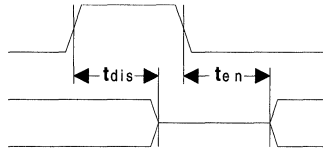
Clock Width

INPUT or
I/O FEEDBACK



Registered Output

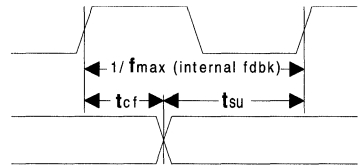
OE



OE to Output Enable/Disable

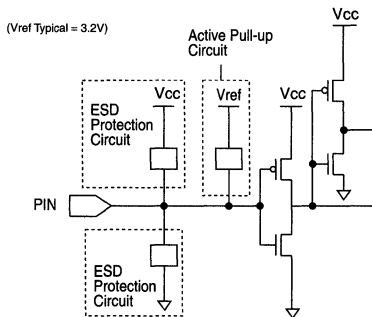
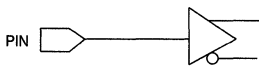
CLK

REGISTERED
FEEDBACK

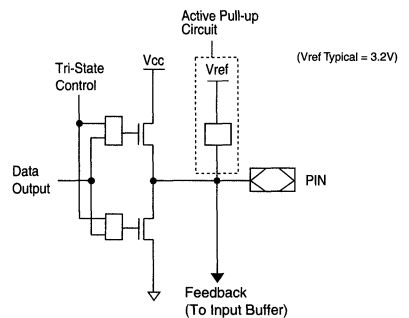
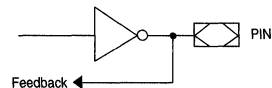


fmax with Feedback

INPUT/OUTPUT EQUIVALENT SCHEMATICS

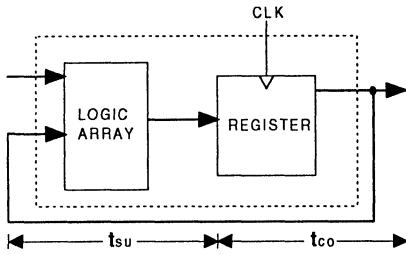


Typical Input



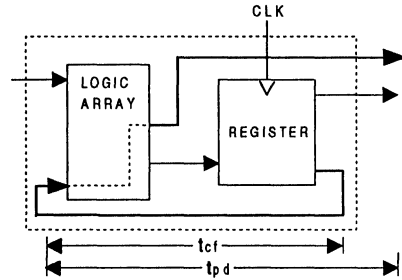
Typical Output

f_{max} DESCRIPTIONS



f_{max} with External Feedback $1/(t_{su} + t_{co})$

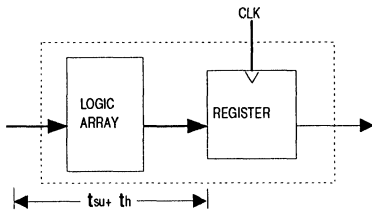
Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su} + t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

3



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

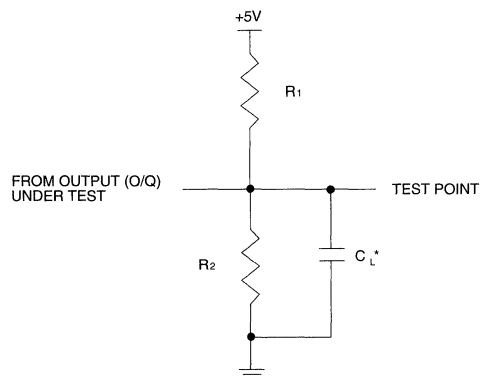
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	390Ω
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20XV10 device. It contains 40 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits, if programmed to any value other than zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20XV10 device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes less than a second. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

LATCH-UP PROTECTION

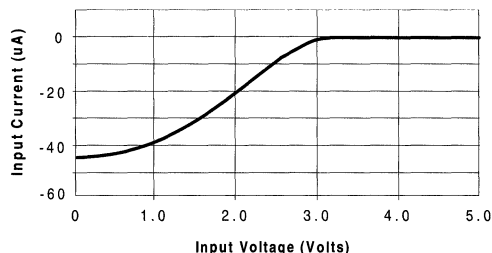
GAL20XV10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL20XV10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

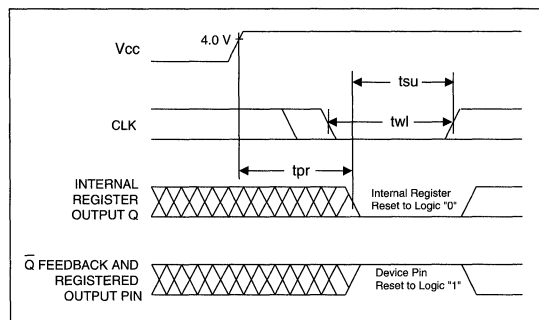
GAL20XV10 input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

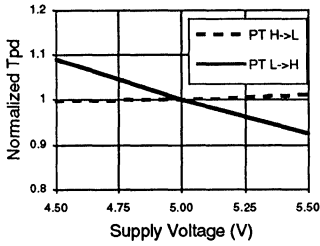
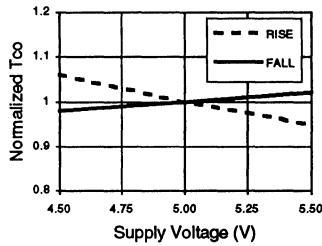
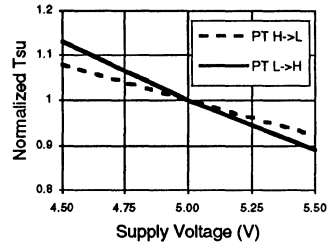
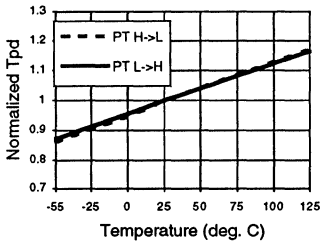
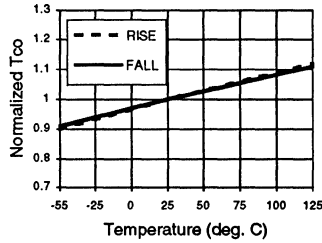
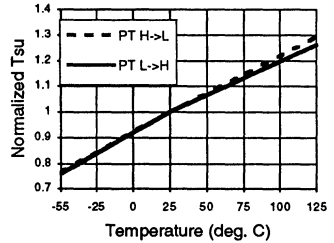
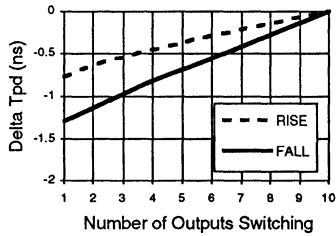
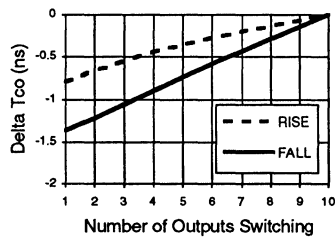
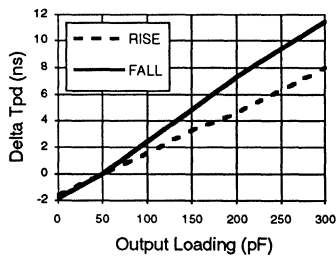
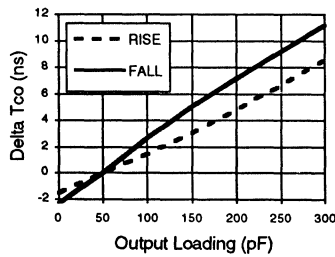
Typical Input Pull-up Characteristic



POWER-UP RESET

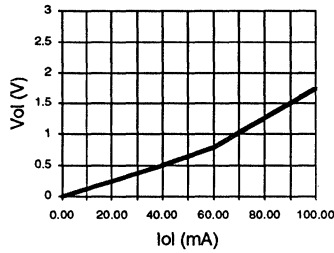
Circuitry within the GAL20XV10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , $1\mu s$ MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20XV10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.



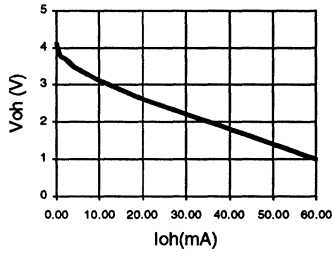
TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS
Normalized Tpd vs Vcc

Normalized Tco vs Vcc

Normalized Tsu vs Vcc

Normalized Tpd vs Temp

Normalized Tco vs Temp

Normalized Tsu vs Temp

Delta Tpd vs # of Outputs Switching

Delta Tco vs # of Outputs Switching

Delta Tpd vs Output Loading

Delta Tco vs Output Loading


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

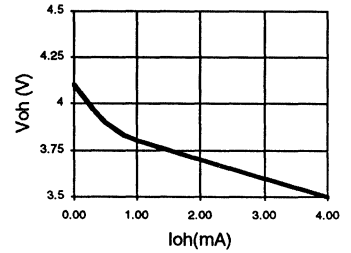
Vol vs Iol



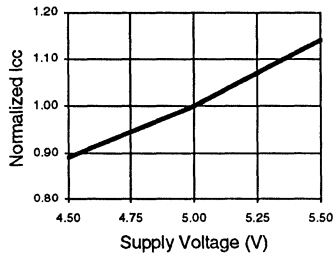
Voh vs Ioh



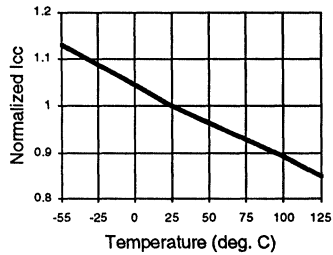
Voh vs Ioh



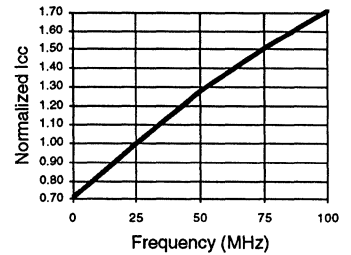
Normalized Icc vs Vcc



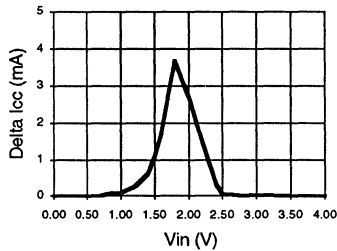
Normalized Icc vs Temp



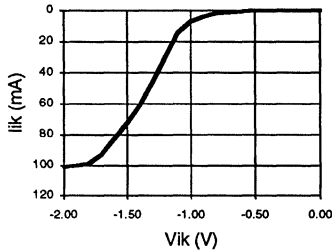
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (VIK)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 5 ns Maximum Propagation Delay
 - Fmax = 200 MHz
 - 4 ns Maximum from Clock Input to Data Output
 - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
 - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMS 22V10 Devices
- **50% to 75% REDUCTION IN POWER VERSUS BIPOLAR**
 - 90mA Typ Icc on Low Power Device
 - 45mA Typ Icc on Quarter Power Device
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

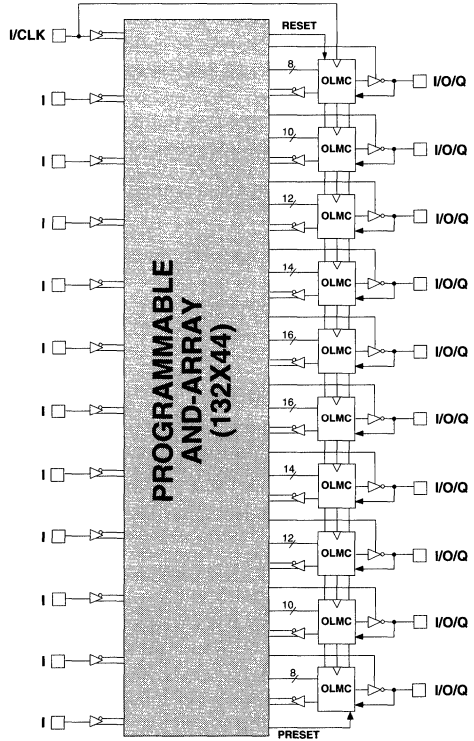
DESCRIPTION

The GAL22V10C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

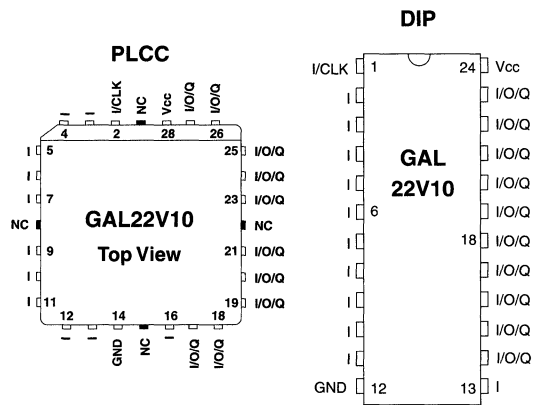
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



3

PACKAGE DIAGRAMS



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GAL22V10 ORDERING INFORMATION

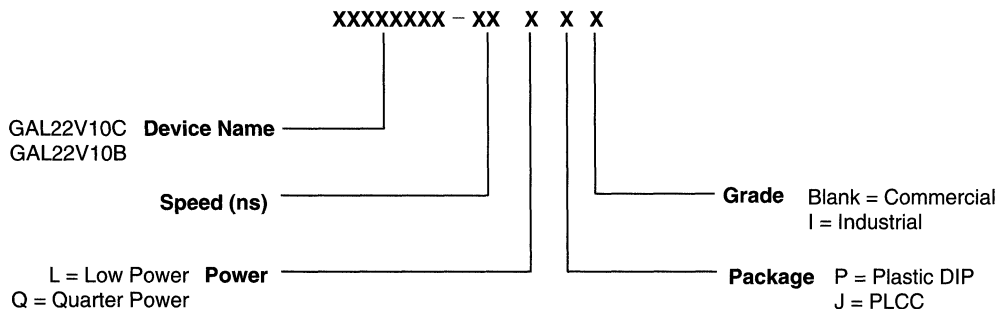
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	150	GAL22V10C-5LJ	28-Lead PLCC
6	4	4	140	GAL22V10C-6LJ	28-Lead PLCC
7.5	4.5	4.5	140	GAL22V10C-7LJ	28-Lead PLCC
			140	GAL22V10C-7LP	24-Pin Plastic DIP
	6.5	5	140	GAL22V10B-7LP	24-Pin Plastic DIP
			140	GAL22V10B-7LJ	28-Lead PLCC
10	7	7	130	GAL22V10B-10LP	24-Pin Plastic DIP
			130	GAL22V10B-10LJ	28-Lead PLCC
15	10	8	55	GAL22V10B-15QP	24-Pin Plastic DIP
			55	GAL22V10B-15QJ	28-Lead PLCC
			130	GAL22V10B-15LP	24-Pin Plastic DIP
			130	GAL22V10B-15LJ	28-Lead PLCC
25	15	15	55	GAL22V10B-25QP	24-Pin Plastic DIP
			55	GAL22V10B-25QJ	28-Lead PLCC
			90	GAL22V10B-25LP	24-Pin Plastic DIP
			90	GAL22V10B-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	7	7	160	GAL22V10C-10LPI	24-Pin Plastic DIP
			160	GAL22V10C-10LJI	28-Lead PLCC
15	10	8	150	GAL22V10B-15LPI	24-Pin Plastic DIP
			150	GAL22V10B-15LJI	28-Lead PLCC
20	14	10	150	GAL22V10B-20LPI	24-Pin Plastic DIP
			150	GAL22V10B-20LJI	28-Lead PLCC
25	15	15	150	GAL22V10B-25LPI	24-Pin Plastic DIP
			150	GAL22V10B-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

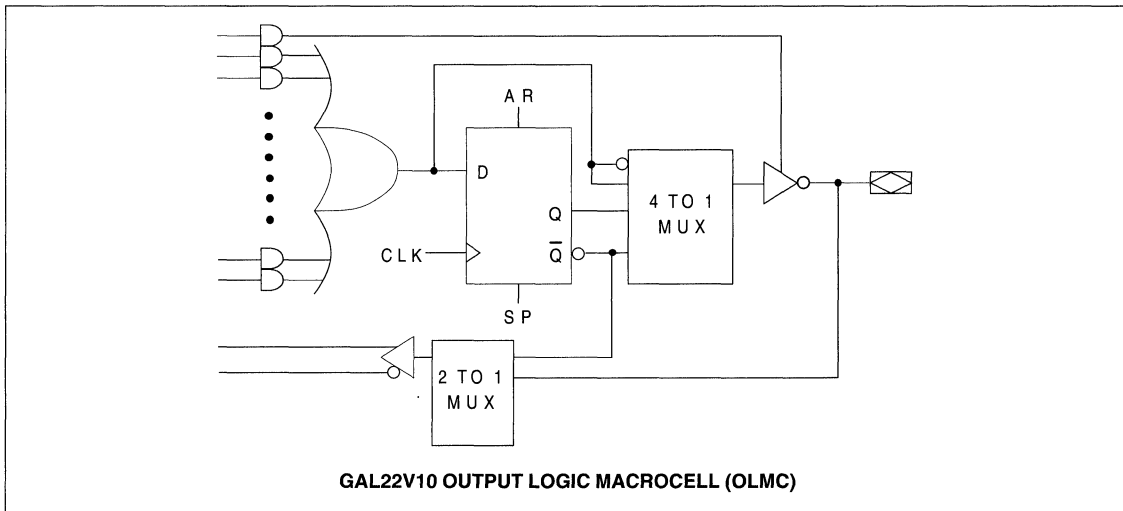
The GAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.

3



OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

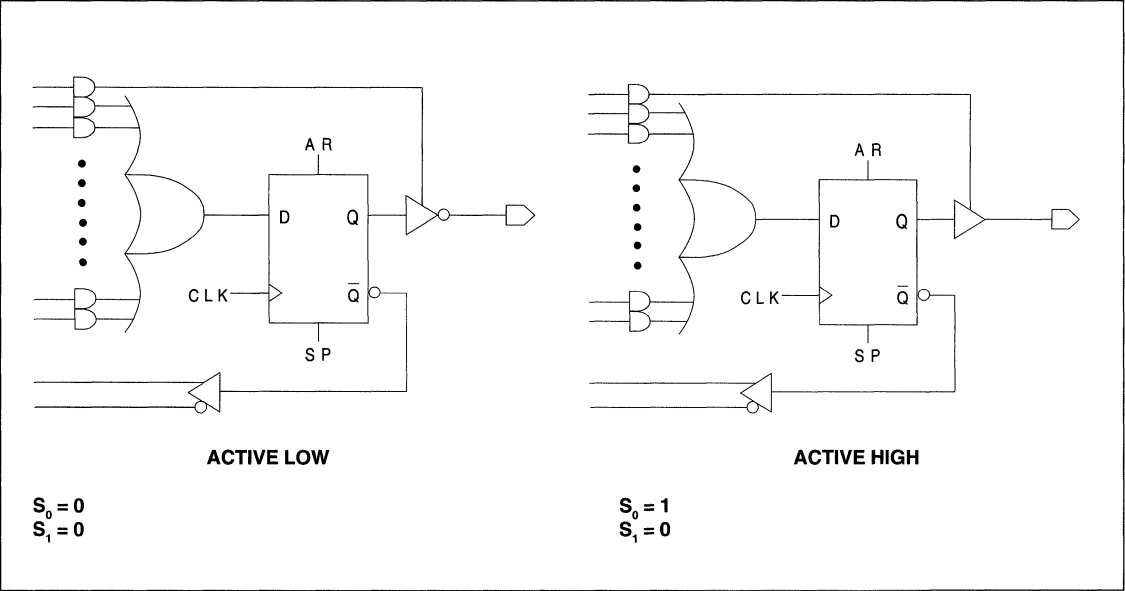
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

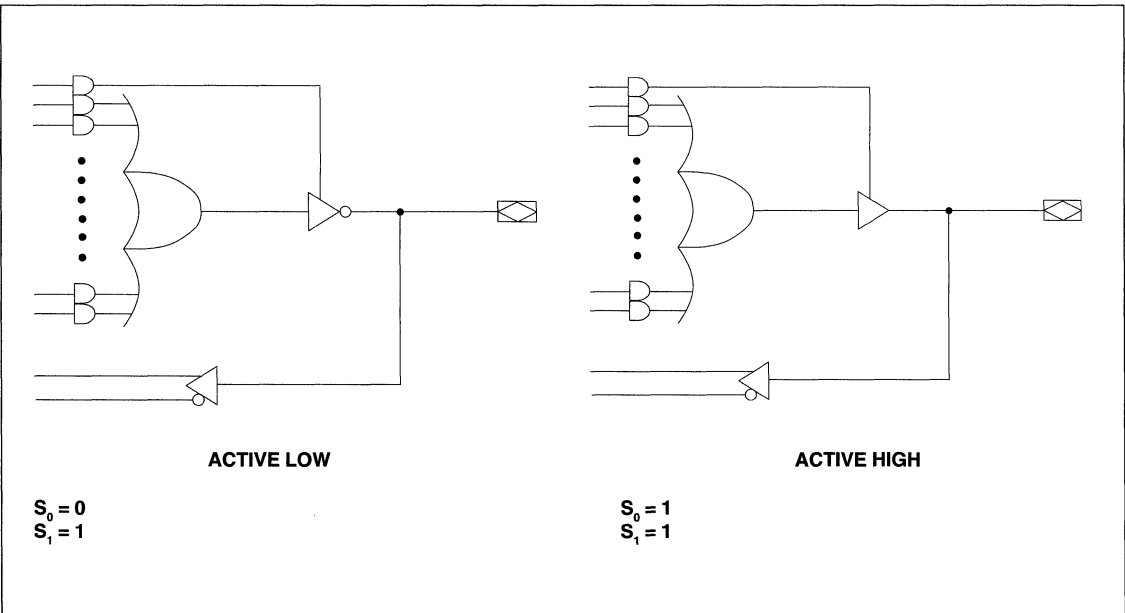
COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE

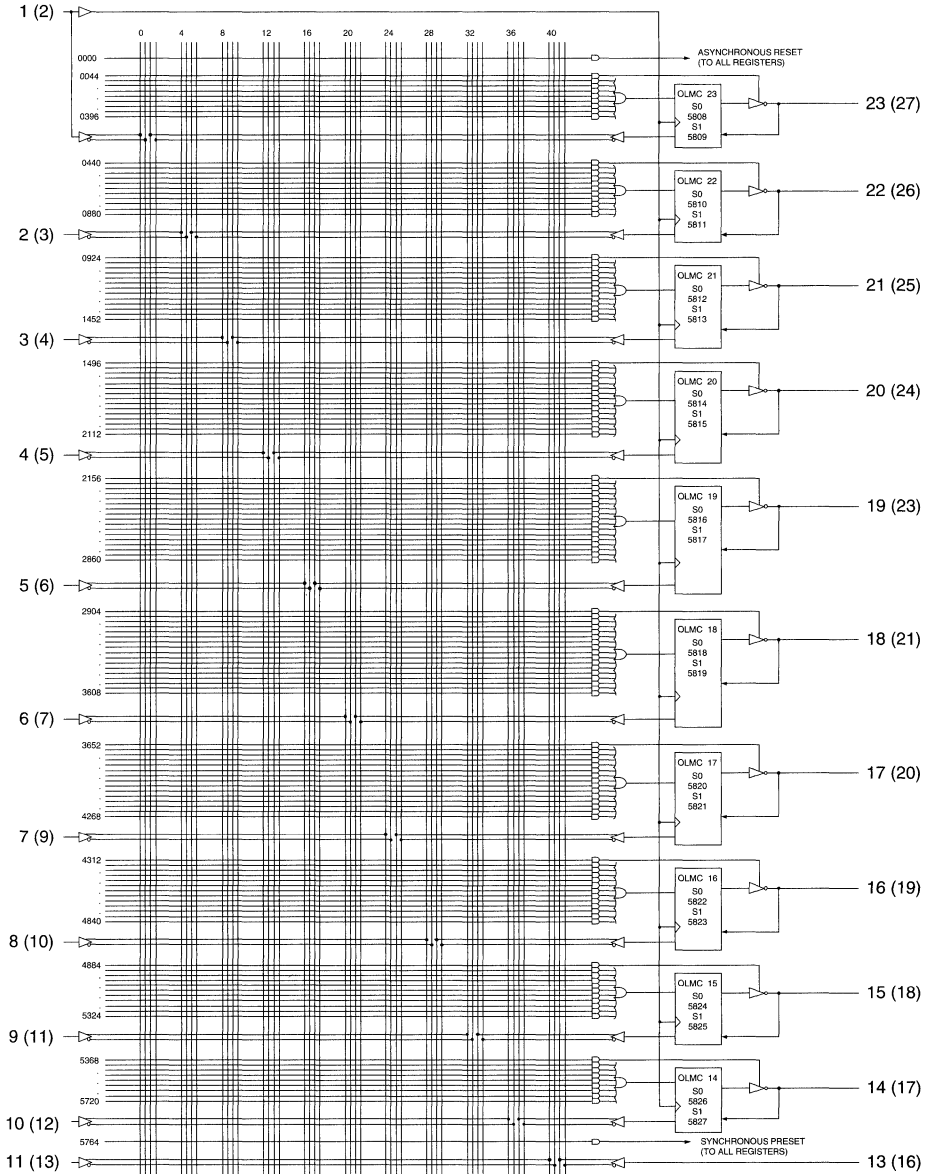


COMBINATORIAL MODE



GAL22V10 LOGIC DIAGRAM / JEDEC FUSE MAP

DIP (PLCC) Package Pinouts



5828, 5829 — Electronic Signature — 5890, 5891
 Byte 7 | Byte 6 | Byte 5 | Byte 4 | Byte 3 | Byte 2 | Byte 1 | Byte 0
 M L
 S S
 0 0

3

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with

Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \text{ Outputs Open}$	L-5	—	90	150	mA
			L-6/-7	—	90	140	mA

INDUSTRIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \text{ Outputs Open}$	L-10	—	90	160	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND. ¹	DESCRIPTION	COM		COM		COM		COM		IND		UNITS
			-5 (PLCC)		-6 (PLCC)		-7 (PLCC)		-7 (PDIP)		-10		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	1	5	1	6	1	7.5	1	7.5	1	10	ns
t_{co}	A	Clock to Output Delay	1	4	1	4	1	4.5	1	4.5	1	7	ns
t_{cf}^2	—	Clock to Feedback Delay	—	3	—	3	—	3	—	3	—	2.5	ns
t_{su}	—	Setup Time, Input or Fdbk before Clk \uparrow	3	—	4	—	4.5	—	5	—	7	—	ns
t_h	—	Hold Time, Input or Fdbk after Clk \uparrow	0	—	0	—	0	—	0	—	0	—	ns
f_{max}^3	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	142.8	—	125	—	111	—	105	—	71.4	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	166	—	142.8	—	133	—	125	—	105	—	MHz
	A	Maximum Clock Frequency with No Feedback	200	—	166	—	166	—	142.8	—	105	—	MHz
t_{wh}	—	Clock Pulse Duration, High	2.5	—	3	—	3	—	3.5	—	4	—	ns
t_{wl}	—	Clock Pulse Duration, Low	2.5	—	3	—	3	—	3.5	—	4	—	ns
t_{en}	B	Input or I/O to Output Enabled	1	6	6	6	1	7.5	1	7.5	1	10	ns
t_{dis}	C	Input or I/O to Output Disabled	1	6	1	6	1	7.5	1	7.5	1	9	ns
t_{ar}	A	Input or I/O to Asynch. Reset of Reg.	1	5.5	7.5	7.5	1	9	1	9	1	13	ns
t_{arw}	—	Asynch. Reset Pulse Duration	5.5	—	6.5	—	7	—	7	—	8	—	ns
t_{arr}	—	Asynch. Reset to Clk \uparrow Recovery Time	4	—	—	—	5	—	5	—	8	—	ns
t_{spr}	—	Synch. Preset to Clk \uparrow Recovery Time	4	—	4	—	5	—	5	—	10	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

 3) Refer to **f_{max} Description** section. Characterized initially and after any design or process changes that may affect these parameters.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{cc} = 5.0\text{V}$, $V_i = 2.0\text{V}$
$C_{i/o}$	I/O Capacitance	8	pF	$V_{cc} = 5.0\text{V}$, $V_{i/o} = 2.0\text{V}$

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	L-7	—	90	140	mA
			L-10/-15	—	90	130	mA
			L-25	—	75	90	mA
			Q-15/-25	—	45	55	mA

INDUSTRIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \quad \text{Outputs Open}$	L-15/-20/-25	—	90	150	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND. ¹	DESCRIPTION	COM		COM		COM / IND		IND		COM / IND		UNITS
			-7		-10		-15		-20		-25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Comb. Output	3	7.5	3	10	3	15	3	20	3	25	ns
t_{co}	A	Clock to Output Delay	2	5	2	7	2	8	2	10	2	15	ns
t_{cf}^2	—	Clock to Feedback Delay	—	2.5	—	2.5	—	2.5	—	8	—	13	ns
t_{su_1}	—	Setup Time, Input or Fdbk before Clk \uparrow	6.5	—	7	—	10	—	14	—	15	—	ns
t_{su_2}	—	Setup Time, SP before Clock \uparrow	10	—	10	—	10	—	14	—	15	—	ns
t_h	—	Hold Time, Input or Fdbk after Clk \uparrow	0	—	0	—	0	—	0	—	0	—	ns
f_{max}^3	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	87	—	71.4	—	55.5	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	111	—	105	—	80	—	45.4	—	35.7	—	MHz
	A	Maximum Clock Frequency with No Feedback	111	—	105	—	83.3	—	50	—	38.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	4	—	6	—	10	—	13	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	4	—	6	—	10	—	13	—	ns
t_{en}	B	Input or I/O to Output Enabled	3	8	3	10	3	15	3	20	3	25	ns
t_{dis}	C	Input or I/O to Output Disabled	3	8	3	9	3	15	3	20	3	25	ns
t_{ar}	A	Input or I/O to Asynch. Reset of Reg.	3	13	3	13	3	20	3	25	3	25	ns
t_{arw}	—	Asynch. Reset Pulse Duration	8	—	8	—	15	—	20	—	25	—	ns
t_{arr}	—	Asynch. Reset to Clk \uparrow Recovery Time	8	—	8	—	10	—	20	—	25	—	ns
t_{spr}	—	Synch. Preset to Clk \uparrow Recovery Time	10	—	10	—	10	—	14	—	15	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **fmax Description** section.

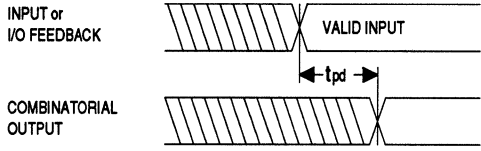
 3) Refer to **fmax Description** section.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

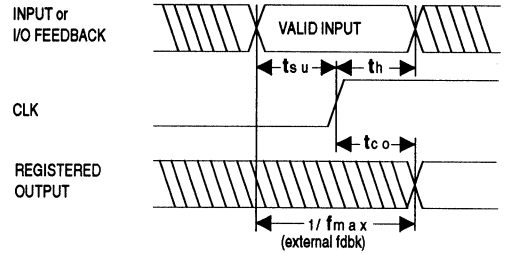
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{cc} = 5.0\text{V}$, $V_i = 2.0\text{V}$
$C_{i/o}$	I/O Capacitance	8	pF	$V_{cc} = 5.0\text{V}$, $V_{i/o} = 2.0\text{V}$

*Guaranteed but not 100% tested.

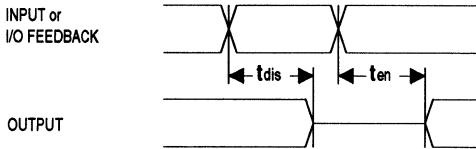
SWITCHING WAVEFORMS



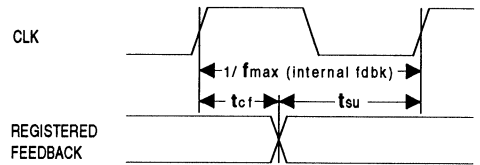
Combinatorial Output



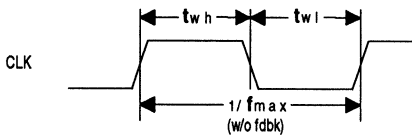
Registered Output



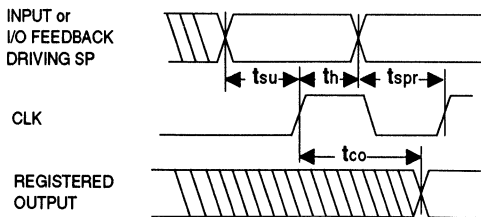
Input or I/O to Output Enable/Disable



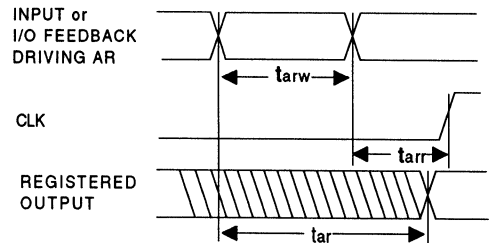
f_{max} with Feedback



Clock Width

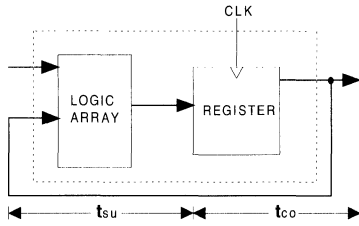


Synchronous Preset



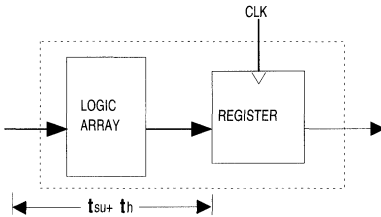
Asynchronous Reset

f_{max} DESCRIPTIONS



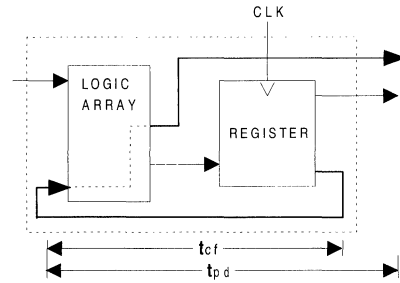
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to t_{cf} + t_{pd}.

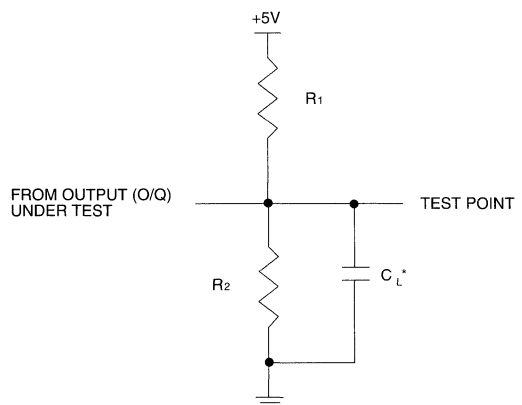
SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	-5/-6	1.5ns 10% – 90%
	-7/-10	2.0ns 10% – 90%
	-15/-20/-25	3ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	390Ω
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL22V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22V10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22V10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22V10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every GAL22V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

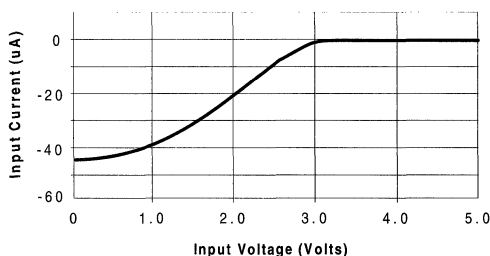
The GAL22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

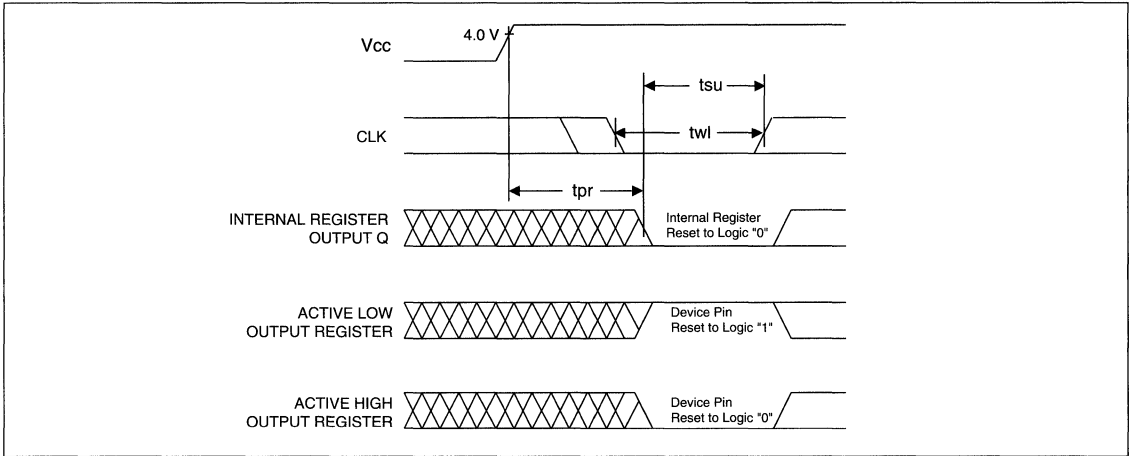
GAL22V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current



POWER-UP RESET

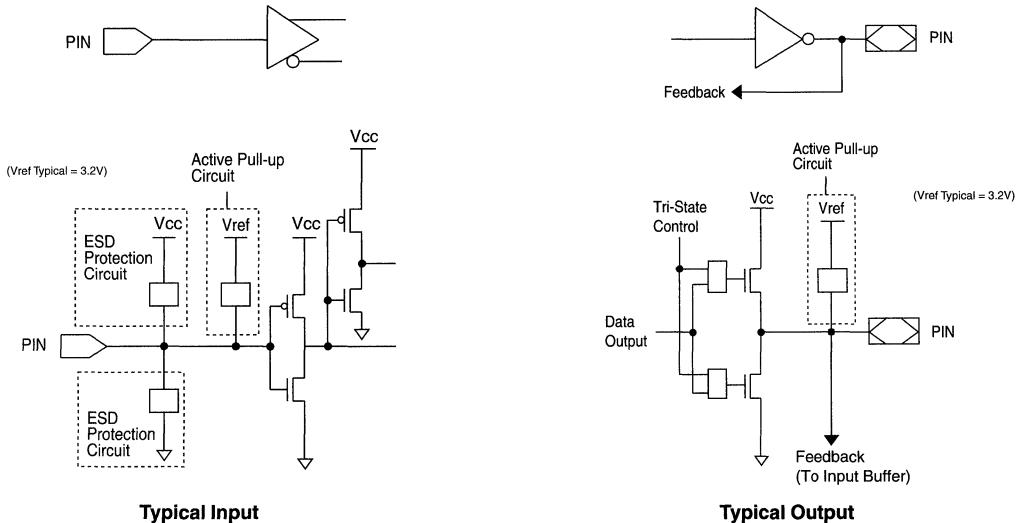


3

Circuitry within the GAL22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-

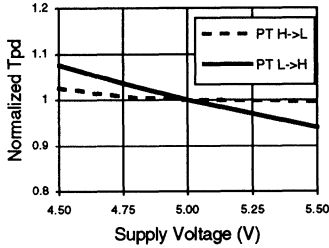
up, some conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

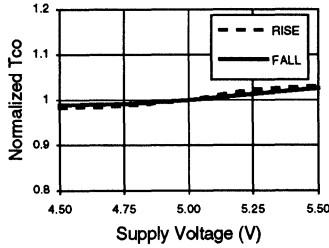


GAL22V10C-6/-7: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

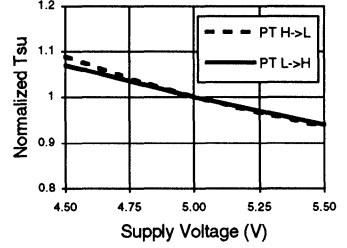
Normalized Tpd vs Vcc



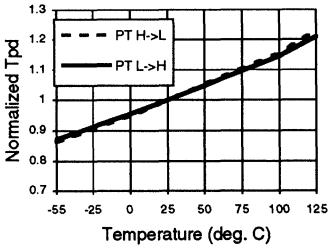
Normalized Tco vs Vcc



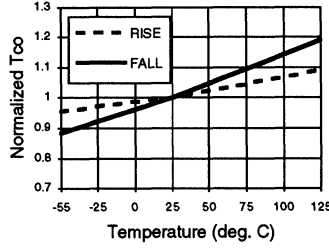
Normalized Tsu vs Vcc



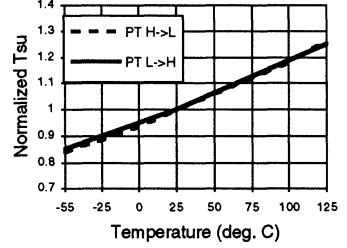
Normalized Tpd vs Temp



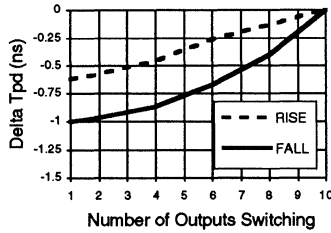
Normalized Tco vs Temp



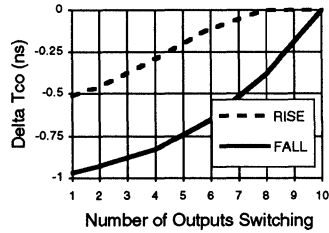
Normalized Tsu vs Temp



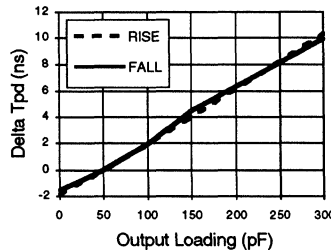
Delta Tpd vs # of Outputs Switching



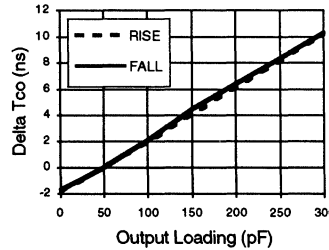
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

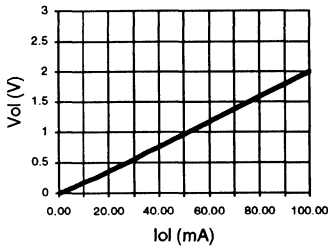


Delta Tco vs Output Loading

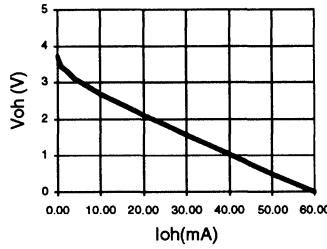


GAL22V10C-6/7: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

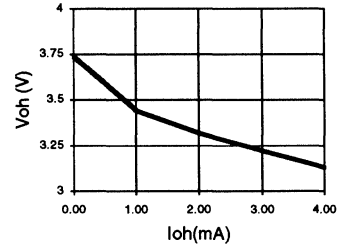
Vol vs Iol



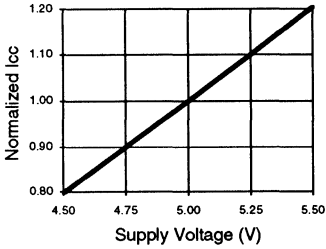
Voh vs Ioh



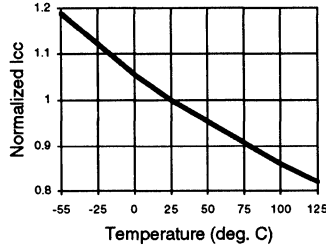
Voh vs Ioh



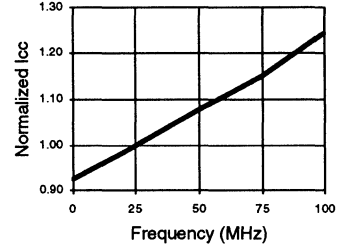
Normalized Icc vs Vcc



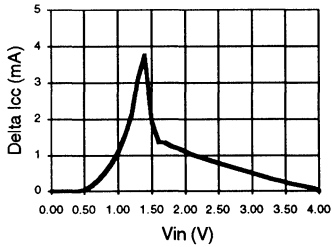
Normalized Icc vs Temp



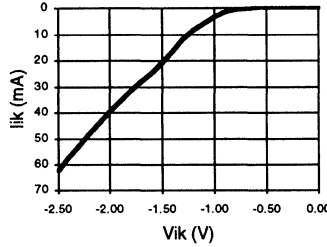
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)

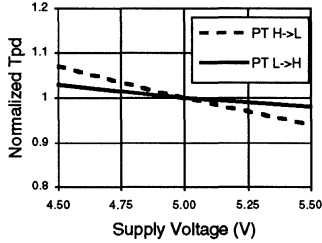


Input Clamp (Vik)

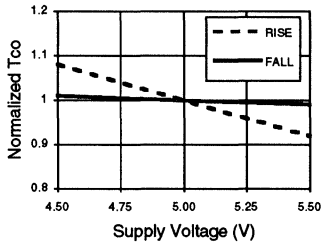


GAL22V10B-7/-10/-15/-25L: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

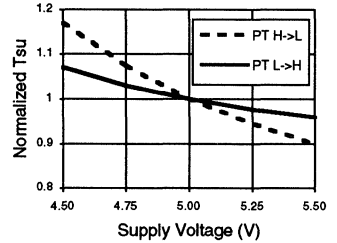
Normalized Tpd vs Vcc



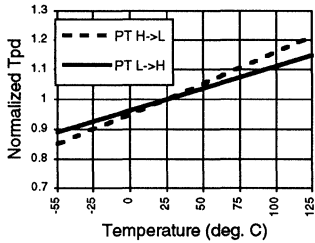
Normalized Tco vs Vcc



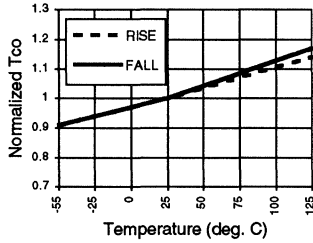
Normalized Tsu vs Vcc



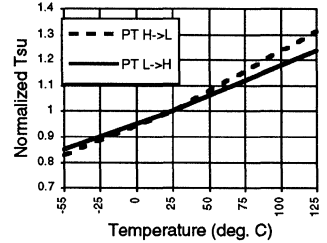
Normalized Tpd vs Temp



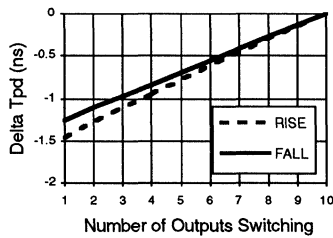
Normalized Tco vs Temp



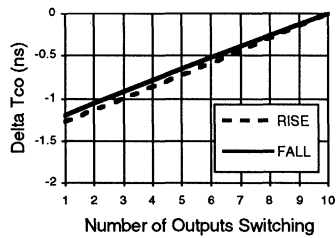
Normalized Tsu vs Temp



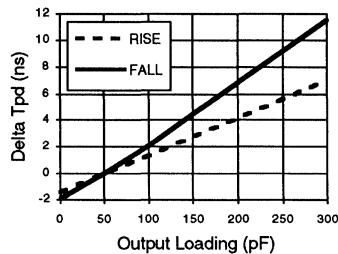
Delta Tpd vs # of Outputs Switching



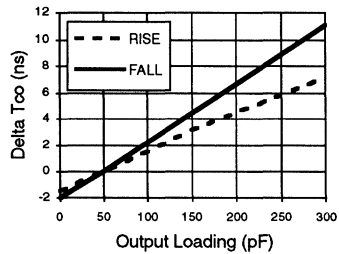
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

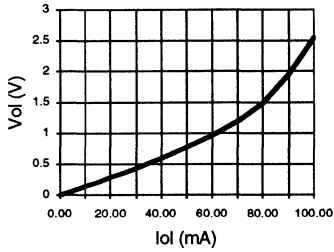


Delta Tco vs Output Loading

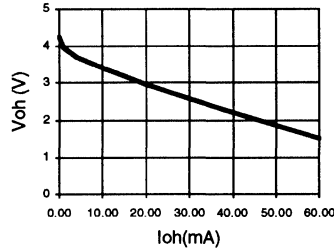


GAL22V10B-7/-10/-15/-25L: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

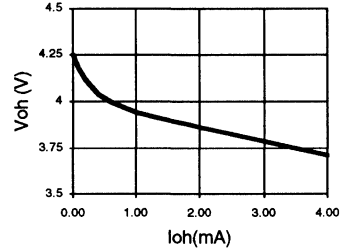
Vol vs Iol



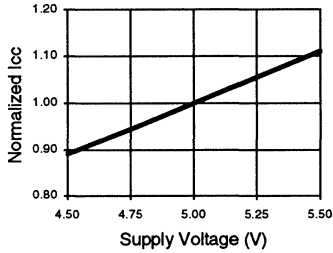
Voh vs Ioh



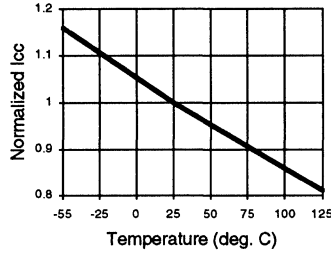
Voh vs Ioh



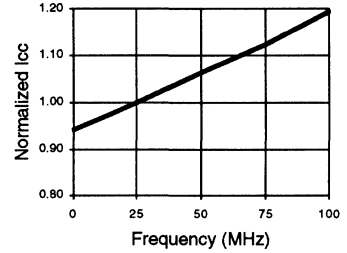
Normalized Icc vs Vcc



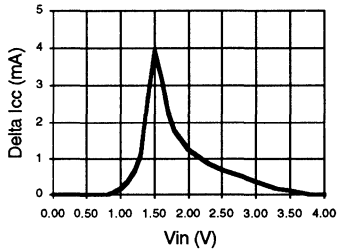
Normalized Icc vs Temp



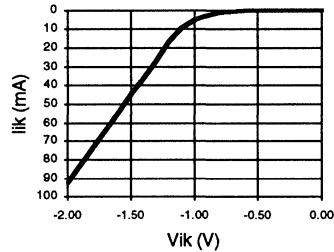
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)

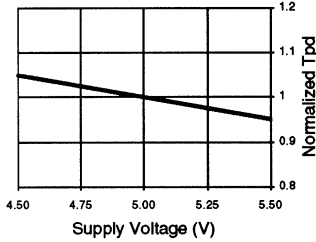


Input Clamp (VIK)

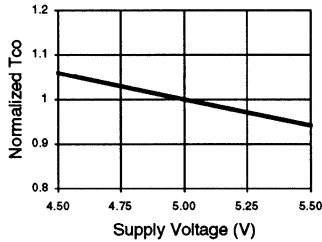


GAL22V10B-15/-25Q: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

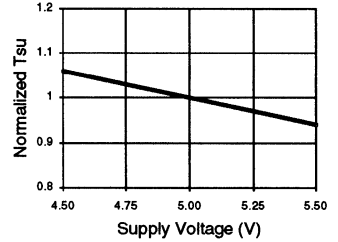
Normalized Tpd vs Vcc



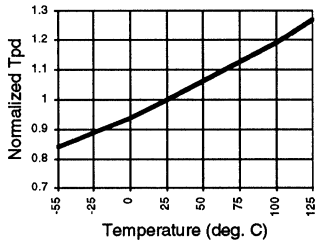
Normalized Tco vs Vcc



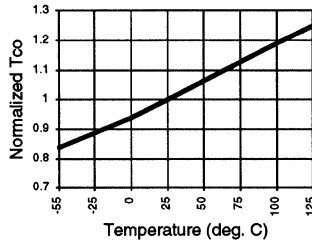
Normalized Tsu vs Vcc



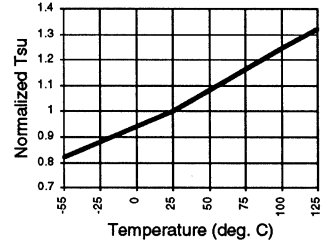
Normalized Tpd vs Temp



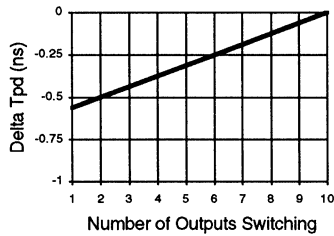
Normalized Tco vs Temp



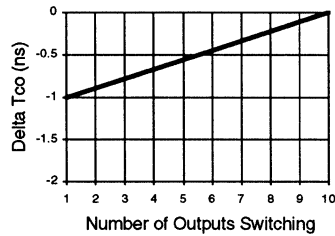
Normalized Tsu vs Temp



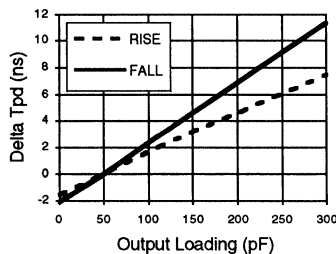
Delta Tpd vs # of Outputs Switching



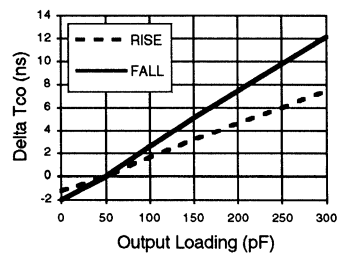
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

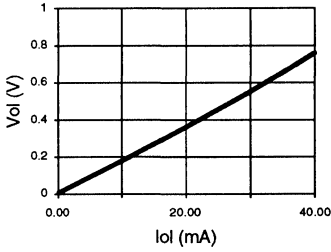


Delta Tco vs Output Loading

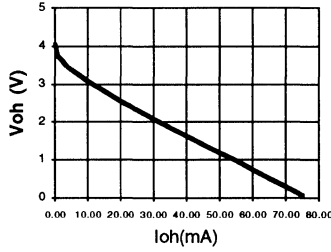


GAL22V10B-15/-25Q: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

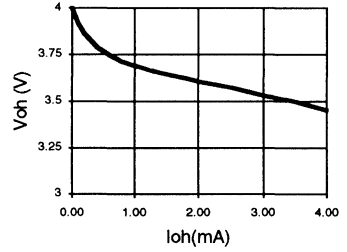
Vol vs Iol



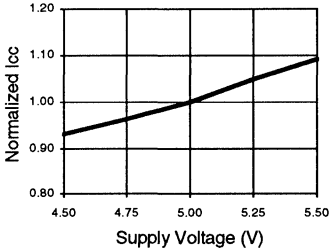
Voh vs Ioh



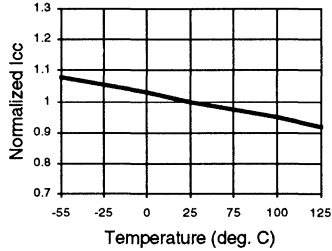
Voh vs Ioh



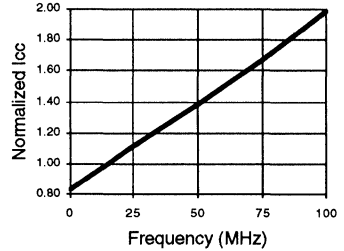
Normalized Icc vs Vcc



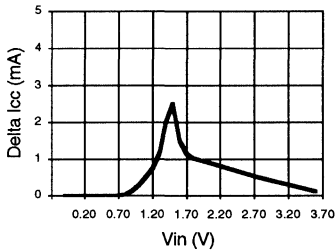
Normalized Icc vs Temp



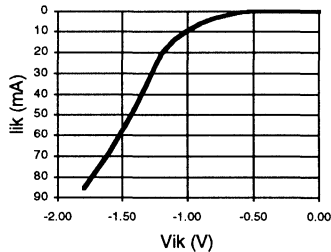
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



FEATURES

- **IN-SYSTEM PROGRAMMABLE (5-V ONLY)**
 - 4-Wire Serial Programming Interface
 - Minimum 10,000 Program/Erase Cycles
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 7.5 ns Maximum Propagation Delay
 - F_{max} = 111 MHz
 - 5 ns Maximum from Clock Input to Data Output
 - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
 - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and CMOS 22V10 Devices
- **E² CELL TECHNOLOGY**
 - In-System Programmable Logic
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Software-Driven Hardware Configuration
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

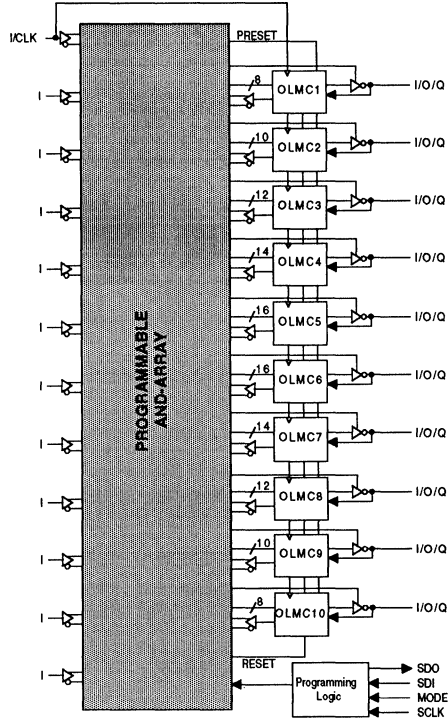
DESCRIPTION

The ispGAL22V10, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the industry's first in-system programmable 22V10 device. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The ispGAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices. The standard PLCC package provides the same functional pinout as the standard 22V10 PLCC package with No-Connect pins being used for ISP interface signals.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all products. LATTICE also guarantees 10,000 erase/rewrite cycles and data retention in excess of 20 years.

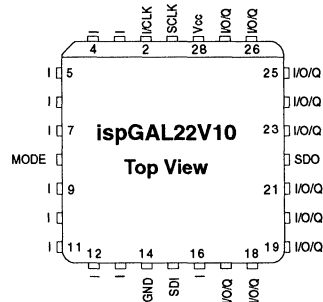
FUNCTIONAL BLOCK DIAGRAM



3

PACKAGE DIAGRAMS

PLCC



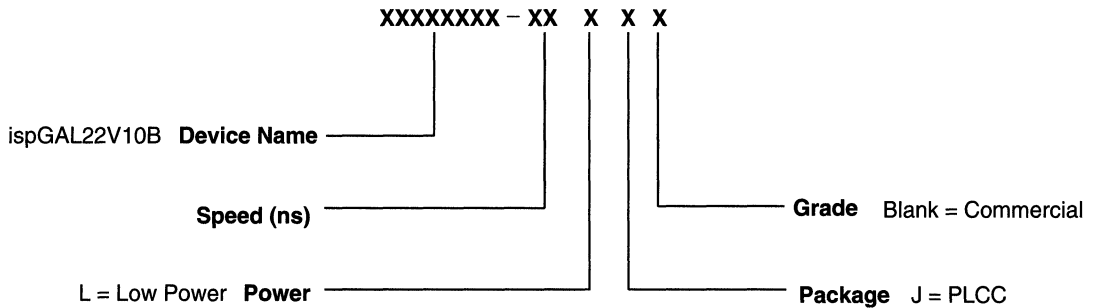
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ispGAL22V10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	6.5	5	140	ispGAL22V10B-7LJ	28-Lead PLCC
10	7	7	140	ispGAL22V10B-10LJ	28-Lead PLCC
15	10	8	140	ispGAL22V10B-15LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



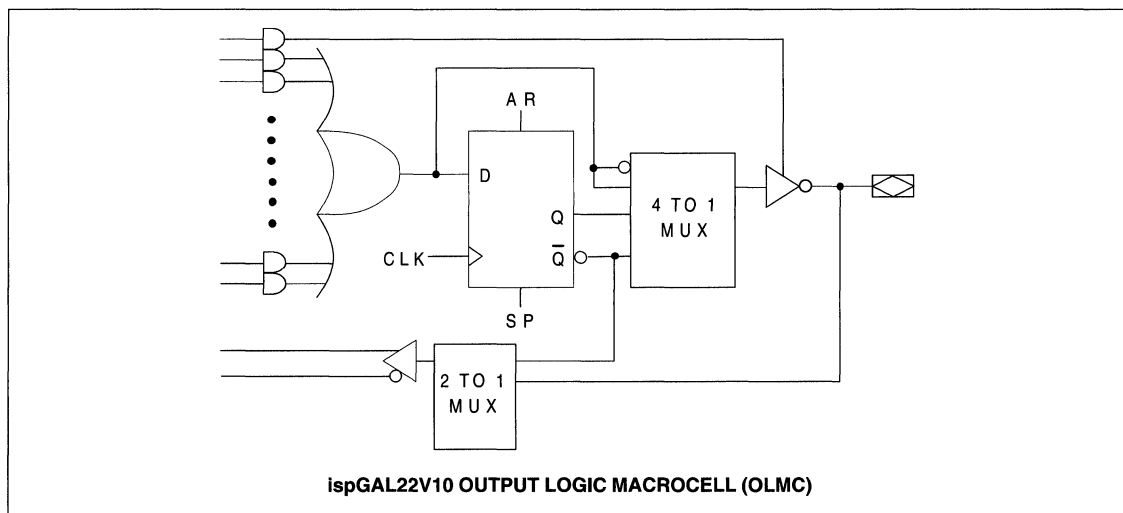
OUTPUT LOGIC MACROCELL (OLMC)

The *ispGAL22V10* has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (OLMC 1 and 10), two have ten product terms (OLMC 2 and 9), two have twelve product terms (OLMC 3 and 8), two have fourteen product terms (OLMC 4 and 7), and two OLMCs have sixteen product terms (OLMC 5 and 6). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The *ispGAL22V10* has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the *ispGAL22V10* has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

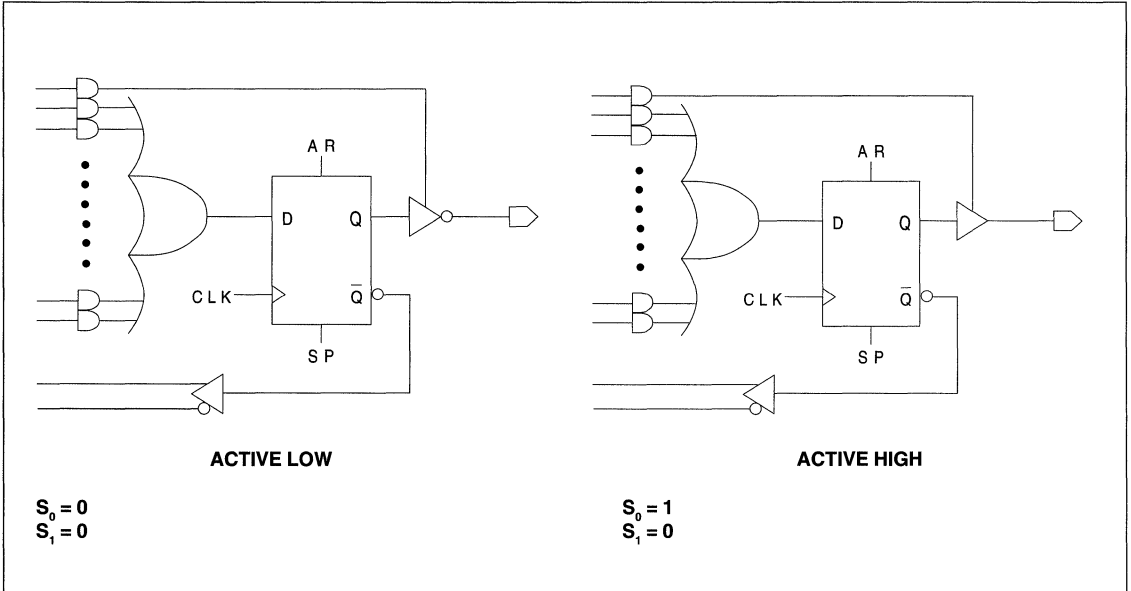
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

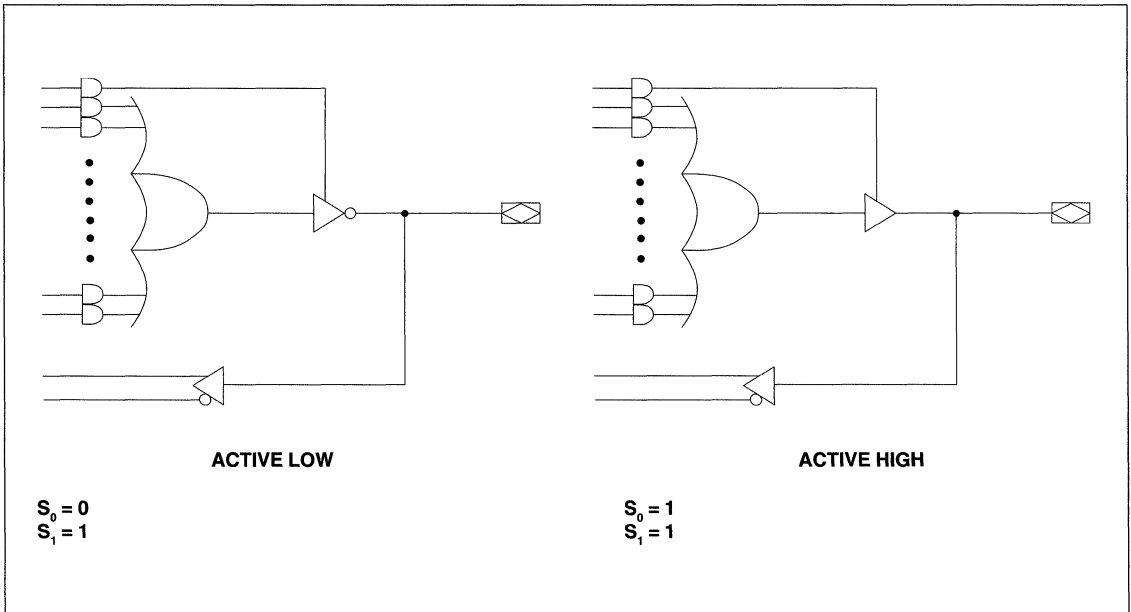
COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE

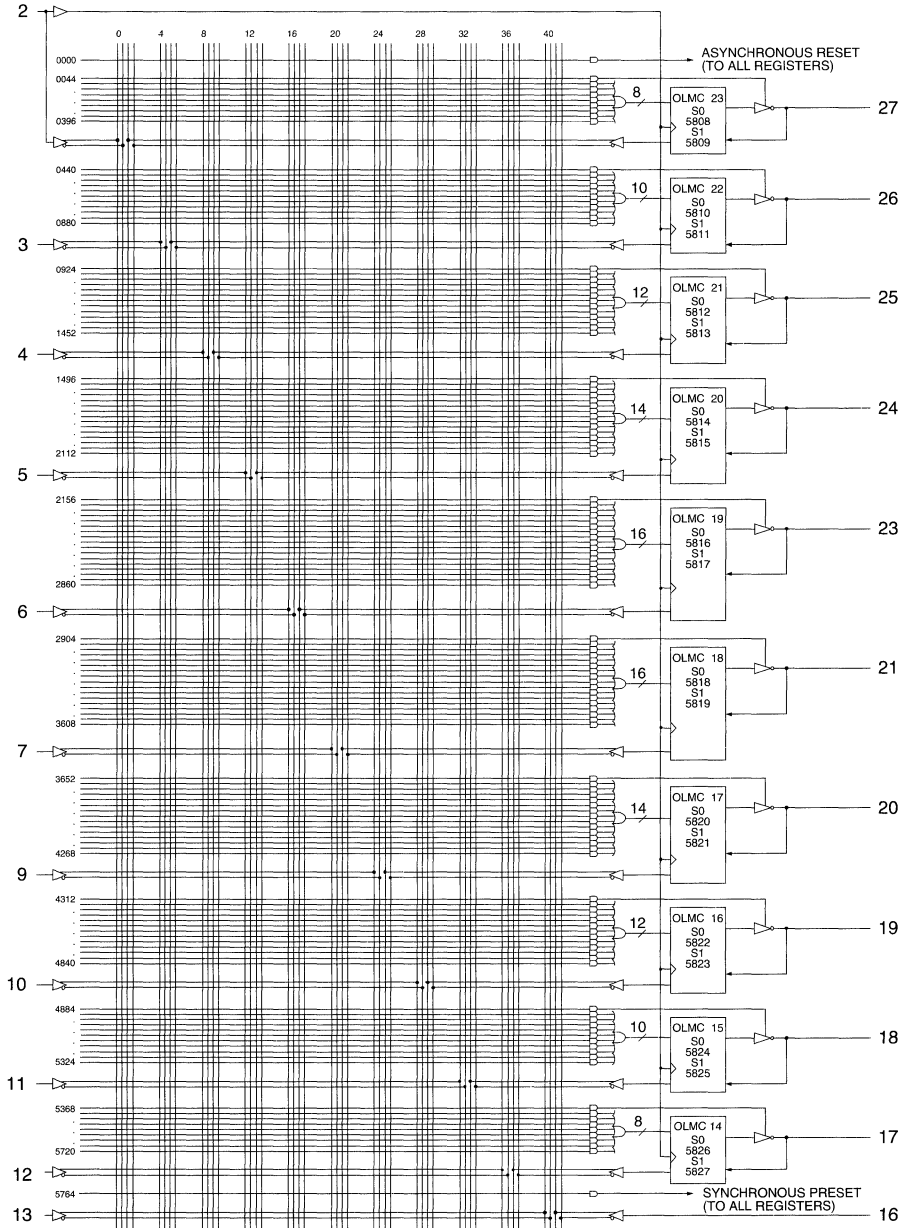


COMBINATORIAL MODE



ispGAL22V10 LOGIC DIAGRAM / JEDEC FUSE MAP

PLCC Package Pinouts



5828, 5829 ...	Electronic Signature	... 5890, 5891					
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
M	L						B
S	S						B
B	B						B

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC}	-0.5 to +7V
Input voltage applied	-2.5 to $V_{CC} + 1.0V$
Off-state output voltage applied	-2.5 to $V_{CC} + 1.0V$
Storage Temperature	-65 to 150°C
Ambient Temperature with Power Applied	-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A)	0 to +75°C
Supply voltage (V_{CC}) with Respect to Ground	+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

ICC	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	L -7/-10/-15	—	90	140	mA
	Supply Current	$f_{toggle} = 15MHz \text{ Outputs Open}$					

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$
$C_{I/O}$	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{I/O} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

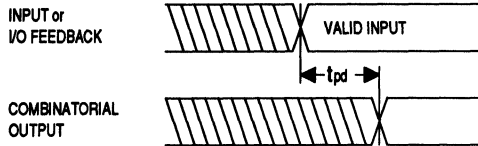
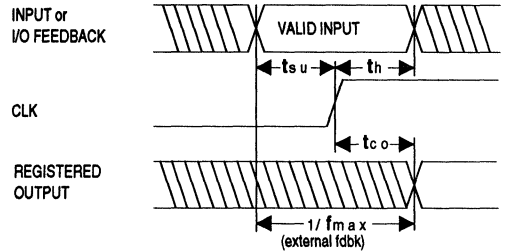
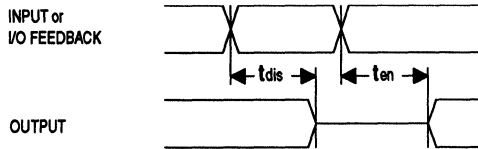
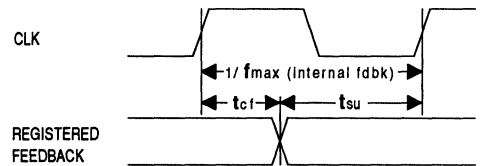
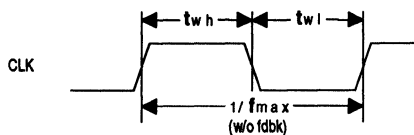
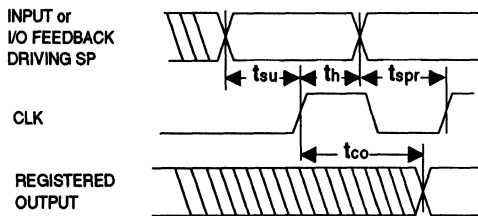
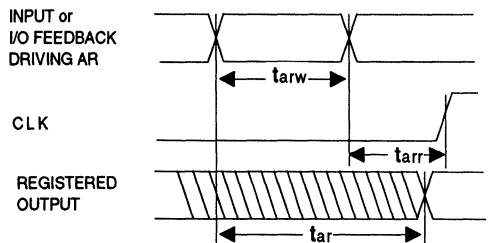
Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	COM		COM		COM		UNITS
			-7		-10		-15		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	7.5	—	10	—	15	ns
t_{co}	A	Clock to Output Delay	—	5	—	7	—	8	ns
t_{cf}²	—	Clock to Feedback Delay	—	2.5	—	2.5	—	2.5	ns
t_{su₁}	—	Setup Time, Input or Feedback before Clock↑	6.5	—	7	—	10	—	ns
t_{su₂}	—	Setup Time, SP before Clock↑	10	—	10	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	87	—	71.4	—	55.5	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	111	—	105	—	80	—	MHz
	A	Maximum Clock Frequency with No Feedback	111	—	105	—	83.3	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	4	—	6	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	4	—	6	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	8	—	10	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	8	—	10	—	15	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	—	13	—	13	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	8	—	8	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	8	—	8	—	10	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	10	—	10	—	ns

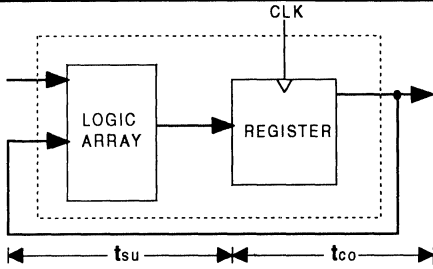
 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.

 3) Refer to **f_{max} Description** section.

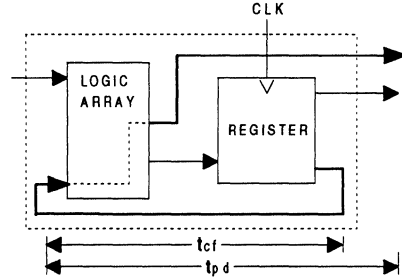
SWITCHING WAVEFORMS

Combinatorial Output

Registered Output

Input or I/O to Output Enable/Disable

fmax with Feedback

Clock Width

Synchronous Preset

Asynchronous Reset

f_{max} DESCRIPTIONS



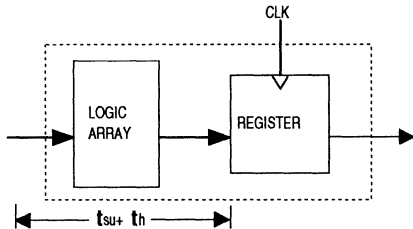
f_{max} with External Feedback 1/(t_{su}+t_{co})

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback 1/(t_{su}+t_{cf})

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback (t_{cf} = 1/f_{max} - t_{su}). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/t_{wh} + t_{wl}. This is to allow for a clock duty cycle of other than 50%.

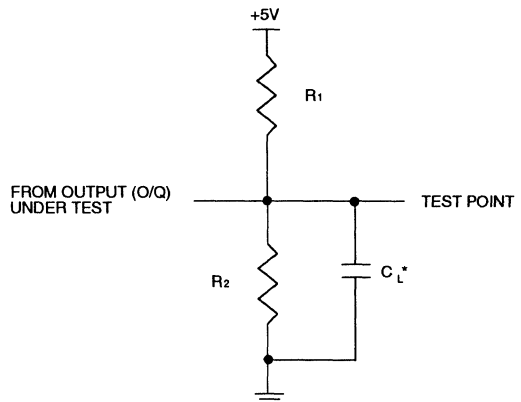
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	5pF
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every ispGAL22V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically an ispGAL22V10 and a ispGAL22V10-UES (UES = User Electronic Signature) or ispGAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the ispGAL22V10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the ispGAL22V10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every ispGAL22V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

ispGAL22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

The ispGAL22V10 device uses a standard 22V10 JEDEC fusemap file to describe the device programming information. Any third party logic compiler can produce the JEDEC file for this device.

The JEDEC file can be used to program the device using a standard PLD programmer or the in-system programming methods described later in this data sheet.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

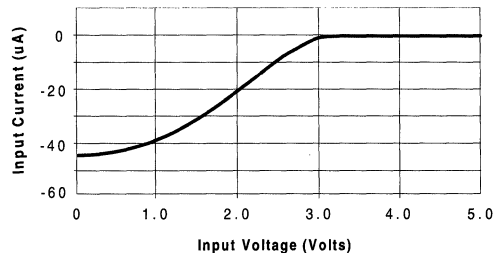
The ispGAL22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

ispGAL22V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

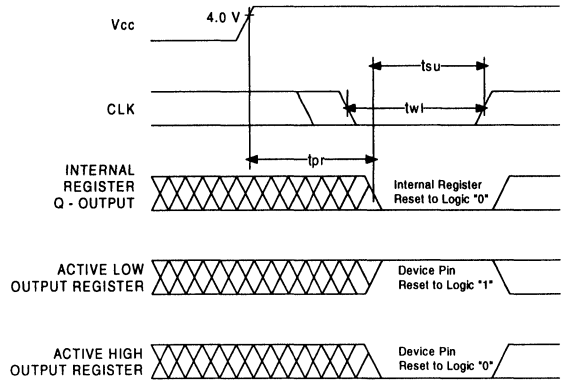
The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current

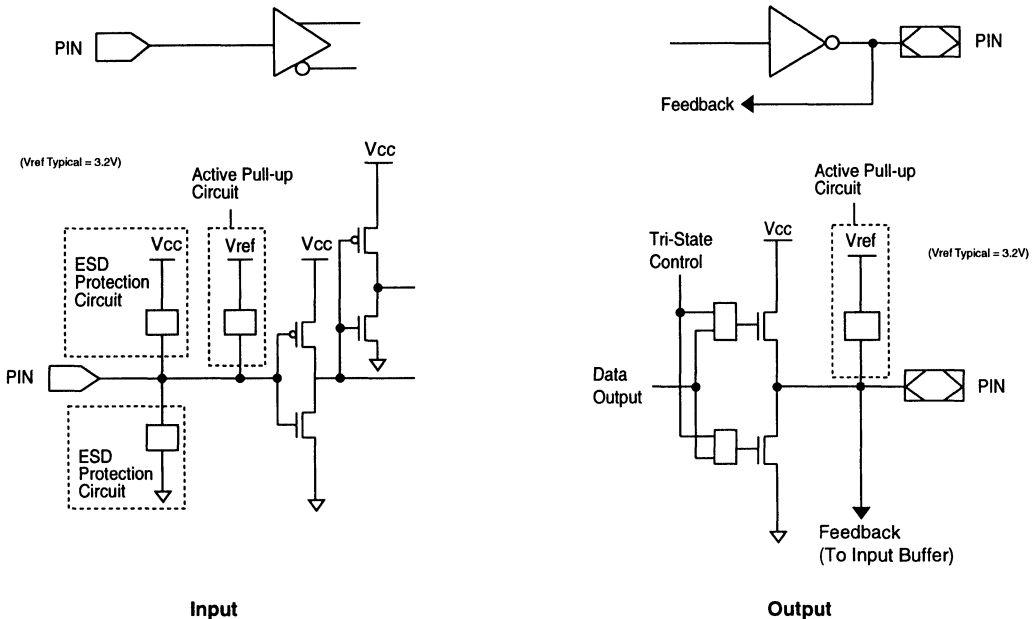


POWER-UP RESET

Circuitry within the *ispGAL22V10* provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the *ispGAL22V10*. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.



INPUT/OUTPUT EQUIVALENT SCHEMATICS



IN-SYSTEM PROGRAMMING OVERVIEW

The ispGAL22V10 device can be programmed in a number of ways. Two options are to build a custom cable to program devices on your board directly from the parallel port of a PC, or to build the programming capability right into your system. To support the software side of either of these solutions, Lattice provides the ispGAL Download library of programming routines. These routines are written in ANSI-standard C language, which can be used either to serve as detailed examples or to be integrated directly into your system. These routines include such common operations as Program, Read, and Verify. The routines are structured so that any hardware-dependent code is contained in a few well-documented functions, which can be easily modified for virtually any system. Example programs are included which use the parallel printer port of an IBM PC or compatible.

In addition, popular third-party programmers provide the ability to program the devices in a socket, just like conventionally programmed devices. This is especially useful for engineering

debug of programming circuitry you build into your own system. Many of the best applications for the ispGAL device use their ability to reconfigure a system in the field. In any system that uses a microprocessor, the microprocessor can often be used to program the ispGAL devices right in the system. The Lattice ispGAL Download software routines can be used to easily integrate ispGAL programming capability into your system software, or allow you to quickly create a custom program for configuring the system. A typical system is shown below in Figure 1. Note that the pattern information is normally stored in the Lattice ispSTREAM™ format, which is a bit-packed format providing device pattern storage in less than 1/8 that of a standard JEDEC file. The pattern information may reside either on-board in an EPROM or EEPROM, or be loaded from an external source such as a disk or across a network.

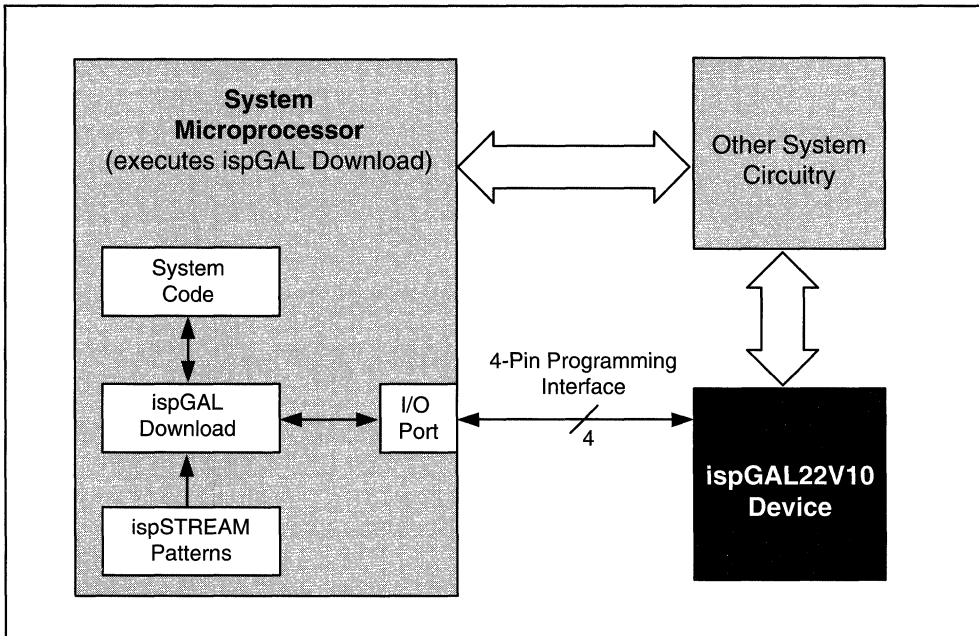


Figure 1. In-System Programming Using ispGAL Download Routines

IN-SYSTEM PROGRAMMING OVERVIEW

Another possibility is to use an external system, such as a portable PC, to change the configuration of a board by reprogramming an on-board ispGAL device (see figure 2 below). This can be useful for field service personnel to re-configure a board for testing or to enable optional features. The same method can be used during the design, test or manufacturing phase, before the board is put into a working system capable of reprogramming the devices.

Lattice provides a stand-alone utility program that uses the PC parallel port to program ispGAL devices through a cable. Also, the ispGAL software library can be used to easily create custom programs for programming the ispGAL devices through your own interface. Example programs using the PC parallel port are included in the ispGAL Download software.

When programming multiple ispGAL devices, the ISP serial interface allows the user to cascade multiple ISP devices in a serial daisy chain (see figure 3). This serial daisy chain interface provides the flexibility to program all daisy chained devices at once or one at a time through a 4-wire interface. To program the serial devices one at a time, the Lattice ISP FLOWTHRU instruction is provided to bypass the serial devices that are not to be programmed.

If you have any questions about programming the ispGAL devices, please contact Lattice Application Engineering at 800-327-8425 or 503-693-0201.

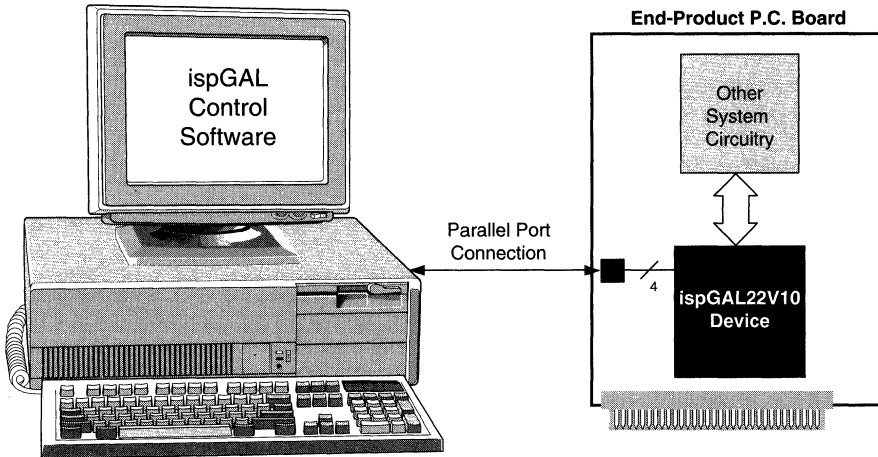


Figure 2. Configuring the ispGAL Device from a Remote System

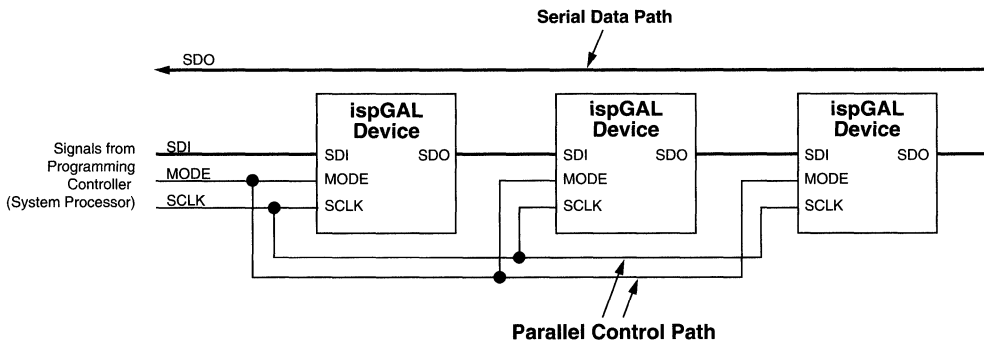


Figure 3. ISP Serial Daisy Chain

The ispGAL uses a similar programming algorithm and programming parameters to other Lattice ISP devices. The devices generate their own internal supervoltage for programming, and only require standard TTL signals to program. Programming the ispGAL device is centered around a 3-state state machine, with its state transitions controlled by two control signals. One of the states is the normal operation state, with the other two states controlling the programming process. The ISP programming state machine is controlled by four dedicated programming pins on each device, which are described below. During normal device operation the SDI, MODE and SCLK pins should be tied low.

SERIAL PROGRAMMING INTERFACE

The ispGAL devices are programmed using the four dedicated programming interface pins: SDI, MODE, SDO and SCLK.

Serial Data In (SDI) performs two different functions. First as the input to the serial shift register, and second as one of the two control pins for the programming state machine. Because of this dual role, the function of SDI is controlled by the MODE pin. When MODE is low, SDI is the serial input to the shift registers and when MODE is high, SDI becomes a control signal. Internal to the device, the SDI is multiplexed to various shift registers in the device. The different shift instructions of the state machine determine which of these shift registers gets the input from SDI.

The MODE signal, combined with the SDI signal, controls the programming state machine, as described in this section.

Serial Clock (SCLK) is the serial shift register clock used to clock

the internal serial shift registers and to clock the state machine between states. State changes and shifting data in is done on a low-to-high transition. When shifting data out, the data is available on SDO only after a subsequent high-to-low transition. When MODE is high, SCLK controls the programming state machine, and when MODE is low, SCLK acts as a shift register clock to shift data in or out or to start an operation.

Serial Data Out (SDO) is the output of the serial shift registers. The selection of shift register is again determined by the state machine's shift instruction. When MODE is driven high, SDO connects directly to the SDI, bypassing the device's shift registers.

PROGRAMMING STATE MACHINE OPERATION

The programming state machine controls which mode the device is in, and provides the means to read and write data to the device (see figure 4). The four dedicated control pins are used to load and unload data, and to control the state machine. The state machine is a 2 bit state machine, with three defined states: IDLE (00), SHIFT (01) and EXECUTE (10). Instruction codes are shifted into the device in the SHIFT state, and control which instruction is to be executed in the EXECUTE state. In the SHIFT and EXECUTE states all the I/O pins are tri-stated. To transition between states MODE is held high, SDI is set to the appropriate level, and SCLK is clocked.

The IDLE state is the default state of the state machine. In this state the device is in normal operation, and programming operations are disabled. Each device contains a hardwired eight bit ID code, which can be read from this state. The IDLE state may be reached from any other state by setting MODE high, SDI low, and clocking SCLK.

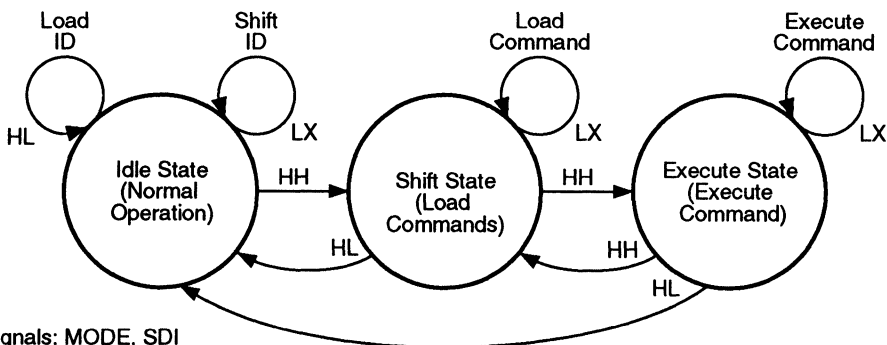


Figure 4. Programming State Machine

The SHIFT state provides the means to load an instruction into the state machine. A five bit instruction is loaded into the state machine by holding MODE low and clocking in the instruction, via SDI. The entire Instruction Set is shown below in Table 1. Once an instruction is loaded into the state machine, it may be executed in the EXECUTE state. The SHIFT state is reached from either of the other two states by setting MODE and SDI high, and clocking SCLK.

The EXECUTE state is where the instruction that was shifted in during the SHIFT state is actually executed. An individual instruction execution is started by taking MODE low and clocking SCLK.

Instruction	Operation	Description
00000	NOP	No operation performed.
00010	SHIFT_DATA	Clocks data into, or out of, the Data Shift Register.
00011	BULK_ERASE	Erases the entire device.
00101	ERASE_ARRAY	Erases everything except the Architecture rows.
00110	ERASE_ARCH	Erases the Architecture rows only
00111	PROGRAM	Programs the Serial Shift Register data into the addressed row
01010	VERIFY	Load data from the selected row into the Serial Shift Register.
01101	IOPRLD	Preload the I/O register with given data.
01110	FLOWTHRU	Disables the Shift Register (SDI=SDO).
10100	ARCH SHIFT	Enables the Architecture shift register for shifting data into or out of the register.

Table 1. Instruction Codes

SHIFT REGISTERS

The ispGAL device has four shift registers, the Device ID shift register, the Instruction shift register, the Data shift register, and the Architecture shift register. All shift registers operate on a First In First Out (FIFO) basis, and are chosen by which state the programming state machine is in.

The Device ID shift register is only accessible in the IDLE state. It is eight bits long, and is only used to shift out the device ID. For ispGAL22V10, the ID is defined to be 08 (hex). The Instruction shift register is only accessible in the SHIFT state. It is five bits long, and is only used to shift the Instruction Codes into the device. The Data and Instruction shift registers expect the LSB shifted in first. The Data shift register is 138 bits long, and is used to shift all addresses and data into or out of the device. The Data shift register is only accessible in the EXECUTE state when executing a SHIFT_DATA instruction. The architecture shift register is 20 bits long and the OLMC 1's S1 architecture bit is shifted in first and OLMC 10's S0 architecture bit is shifted in last. The architecture shift register is accessed during EXECUTE state when ARCH_SHIFT instruction is executed.

To program an ispGAL device, data is read from a serial bit stream and shifted into the shift registers. The data is read 138 bits at a time, shifted into the device, and then a programming operation is performed. The exact sequence, and the methods for converting a JEDEC map into a serial bit stream is explained in the Device Architecture section.

TIMING

Programming the ispGAL devices properly requires that a number of timing specifications be met. Most critical are the specifications relating to programming and erasing the E²CMOS cells. In addition to a minimum pulse width, there is also a maximum specification for these parameters. Table 2 lists the programming mode specifications for the ispGAL device. Diagrams for the programming mode specifications are shown in Figures 5, 6, and 7 on the following page.

INTERNAL ARCHITECTURE

This section explains the internal architecture of the device as it relates to programming. This section is not strictly necessary to the programming of the device if you are using the Lattice software tools provided.

The key to easy programming of the ispGAL device is the use of a bit-stream of all the data that needs to be shifted into a device to program it. Lattice calls this bit-stream format an ispSTREAM™ format. The ispSTREAM format uses one bit to represent the state of each of the programmable cells, instead of the byte value used in a JEDEC file. Considering the additional characters in a JEDEC file, this means a space savings of more than a factor of eight. In addition, the ispSTREAM does not require any parsing. The bits are simply read from the file and shifted into the device. Since 804 bytes are required to store the pattern for an ispGAL device, multiple patterns can be stored in a small space.

This section mainly concerns the details of constructing the ispSTREAM format. If you are using the supplied software tools, a conversion utility (complete with source code) is included to convert an industry-standard JEDEC file to an ispSTREAM format. All of the Lattice software routines read from and write to this ispSTREAM format.

The ispGAL device have three basic sections to their programming architecture (see figure 8). There are 44, 132-bit wide rows of AND array section, one 64-bit wide row of User Electronic Signature (UES) section and one 20-bit wide row of architecture information.

The AND array section of the physical layout is organized so that each column of JEDEC fuse numbers shown in the logic diagram of ispGAL22V10 corresponds to one row of shift register for the device layout. This translates to each physical row being 132 bits long. With each row of AND array data, there is a 6-bit row address associated with it. Including the row address bits makes the shift registers 138 bits long. These row

address bits must also be shifted into the shift register along with the AND array data. Executing a PROGRAM command following the combination of data and row address shift programs the row that is specified by the shift instruction. The UES row is unique from the AND array data rows in that it is only 64 bits long. When the row address bits are added to the row the total shift register length required to fully specify the UES row is 70 bits long. In other words only 70 bits out of 132 bit shift register is used for UES. The 20-bit long architecture shift register is selected when ARCH_SHIFT instruction is executed. The OLMC 0, S1: OLMC 0, S0; OLMC 1, S1: OLMC1, S0; etc. are shifted in order with the last bit of the shift register being OLMC 10, S0.

Param.	Description	Min.	Max.	Unit
t _{rst}	Time from power-up of device to any programming operation.	1	—	μs
t _{isp}	Time from leaving IDLE state to I/O pins tri-state, or entering IDLE state to I/O pins active.	—	10	μs
t _{su}	Setup time, from either MODE or SDI to rising edge of SCLK.	100	—	ns
t _h	Hold time, from rising edge of SCLK to MODE or SDI changing level.	100		ns
t _{co}	Time from falling edge of SCLK to data out on SDO.		150	ns
t _{clkh}	Clock pulse width of SCLK while high.	0.5		μs
t _{clkl}	Clock pulse width of SCLK while low.	0.5		μs
t _{pw}	Time for a programming operation.	40	100	ms
t _{pwe}	Time for an erase operation.	200		ms
t _{pwv}	Time for a verify operation.	5		μs

Table 2. Programming Mode Timing Specifications

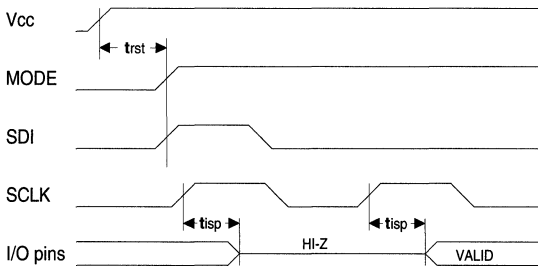


Figure 5. Programming Mode Timing

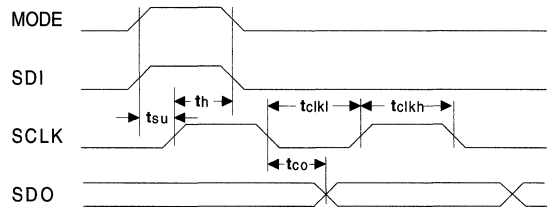


Figure 6. Shift Register Timing

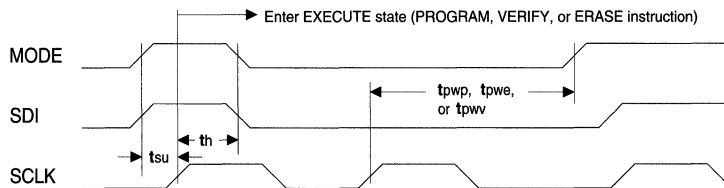


Figure 7. Program, Verify, & Erase Timing

ispStream Format

To convert the information in a standard JEDEC file into the ispSTREAM format, all of the addressing information is added, as well as the place-holding bits to fill to the next byte boundary. The objective is to have every bit that is shifted into the device for programming included in the ispSTREAM format. For the AND array rows, this means simply adding six bits to the end of each row. For the UES row, there are 2 bits to add. And for the architecture row 4 bits are added. These additional bits must be properly handled when data is shifted into the shift register. The proper number of bits must be incremented to forward the ispSTREAM bits to point to the next correct address bit.

The ispSTREAM uses one bit for each programmable cell. This means that each AND array row will take 138 bits. Similarly, 64 bits for the UES and 20 bits for the architecture. One extra byte is used at the front of the file to store the device ID code. This ID code is the same as the one hardwired into the device. The purpose of including this ID code is to be sure the ispSTREAM type matches that of the device to be programmed. All ispSTREAM formats, regardless of which Lattice In-System Programmable device they are for, will contain this ID code as the first byte. By reading this ID code, you can tell which device the ispSTREAM is for. If the ispSTREAMs are stored in EPROM for instance, they will be stacked end to end, and the ID code will help to determine not only which device type it belongs with, but how long it is, and thus where the next pattern starts.

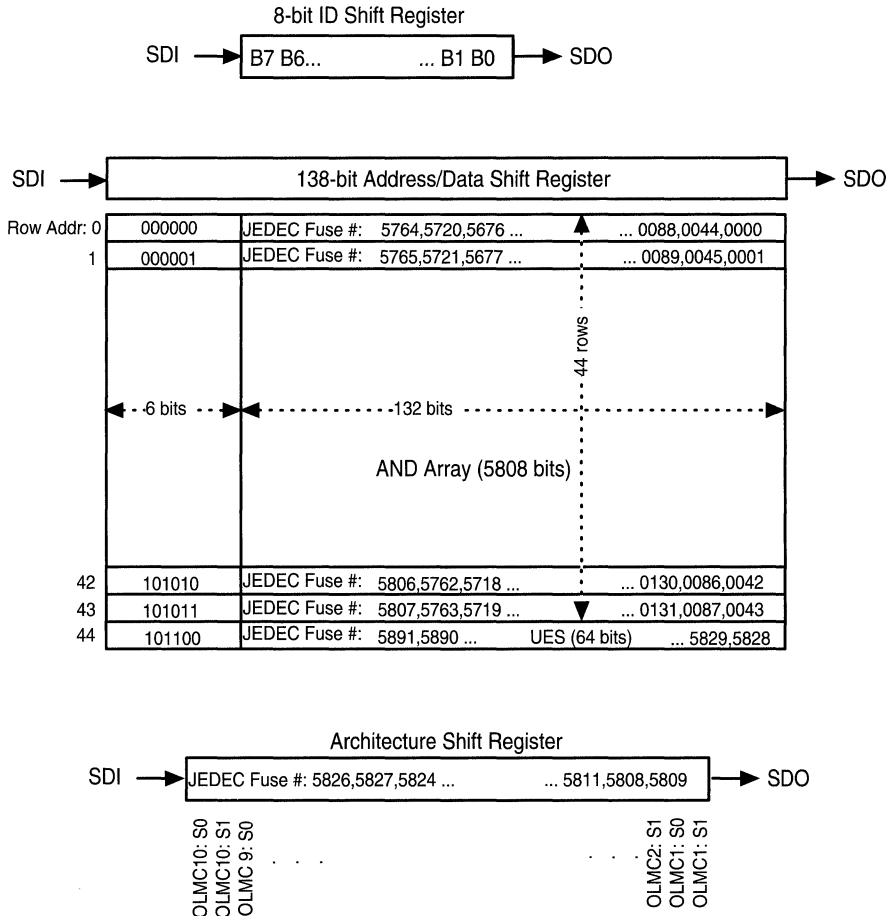


Figure 8. ispGAL Device Shift Register Layout

ISP PROGRAMMING TOOLS SUPPORT

To assist users in implementing ISP programming, Lattice provides ispGAL C language routines included with the ispGAL Download software which implement the basic ISP functions for programming through the PC parallel port. This section provides the details of the PC parallel port definition needed to program the ispGAL.

PC PARALLEL PORT DEFINITION

The PC parallel port must be properly defined in order to use the ispGAL software to program the devices. After defining the port, ispGAL Download software controls the read and write of data through the parallel port. To guarantee the signal integrity and drive capability, a 74HC367 (or equivalent) buffer should be directly connected at the parallel port's DB25 connector. Figure

9 below defines the parallel port DB25 pins and the associated programming signals. This hardware definition is identical to the Lattice ispLSI programming hardware with the exception of the ispEN and RESET signals which are defined only for the ispLSI devices.

The buffer at the parallel port drives the cable that connects the output of the buffer to the ISP programming signals of the device. It is important to keep the cable length to a minimum to reduce the loading on the signal drivers. The SDI, SCLK and MODE inputs to the ispGAL are driven by the buffer connected at the parallel port. The SDO output signal from the ispGAL is driven from the device back to the parallel port. If the load on the SDO signal is more than a minimum cable length and the parallel port input, it is recommended that the user provide a buffer on the circuit board to ensure good signal integrity.

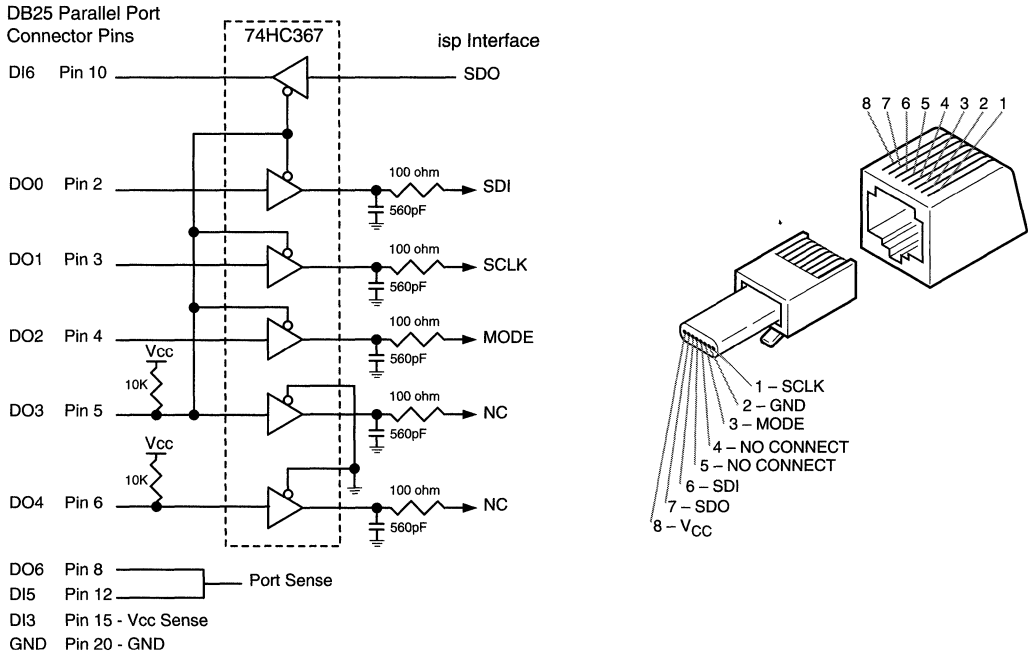
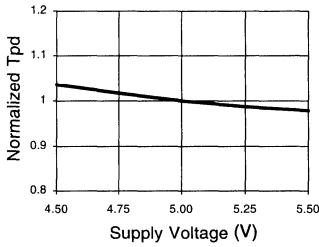
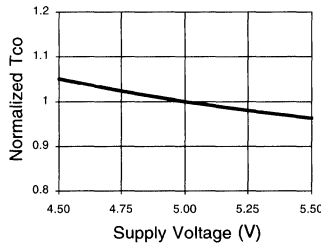
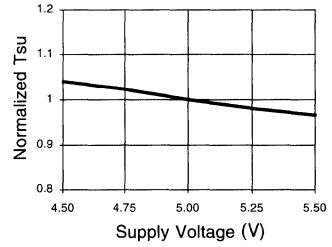
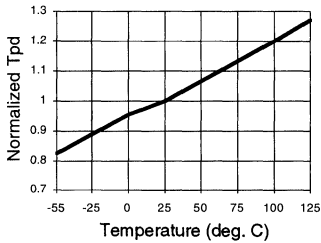
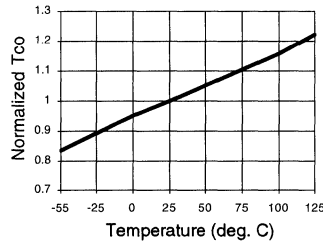
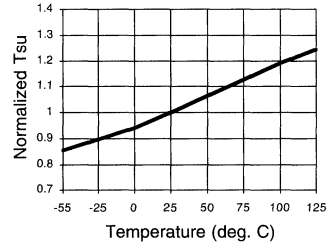
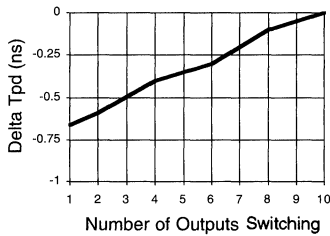
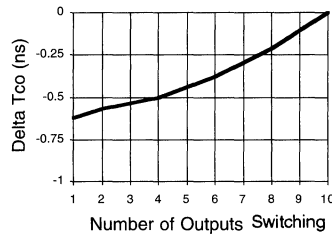
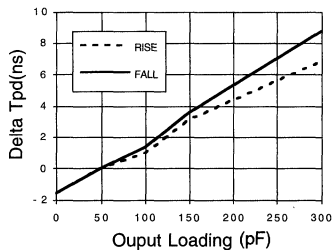
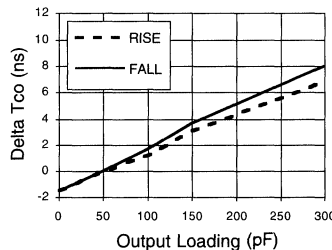
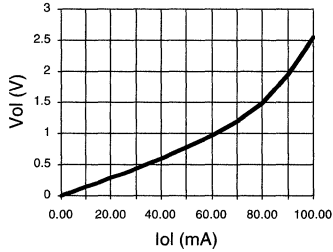


Figure 9. PC Parallel Port Buffer & RJ45 Connector Definition

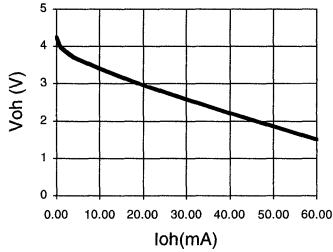
ispGAL22V10B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS
Normalized Tpd vs Vcc

Normalized Tco vs Vcc

Normalized Tsu vs Vcc

Normalized Tpd vs Temp

Normalized Tco vs Temp

Normalized Tsu vs Temp

Delta Tpd vs # of Outputs Switching

Delta Tco vs # of Outputs Switching

Delta Tpd vs Output Loading

Delta Tco vs Output Loading


ispGAL22V10B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

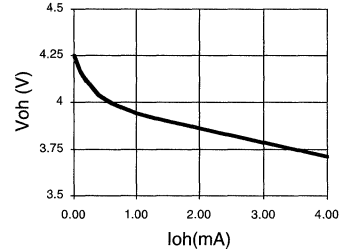
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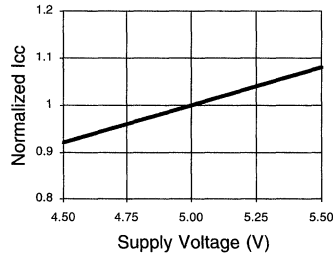
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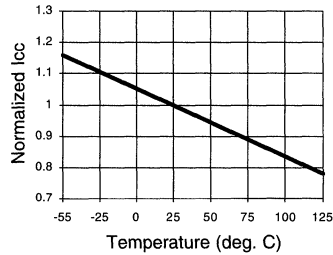
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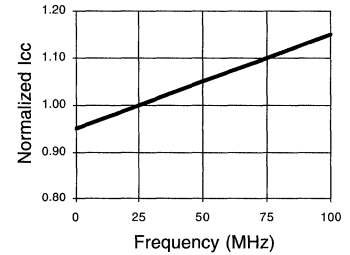
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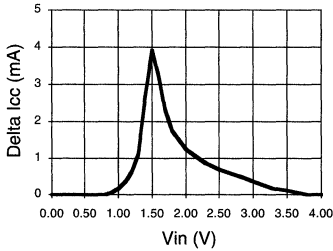
Normalized Icc vs Temp



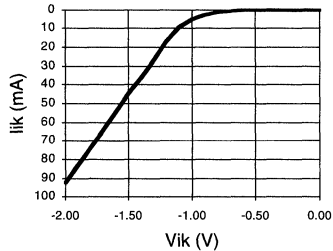
Normalized Icc vs Freq.



Delta Icc vs Vcc



Input Clamp (Vik)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 7.5 ns Maximum Propagation Delay
 - F_{max} = 142.8 MHz
 - 4.5ns Maximum from Clock Input to Data Output
 - TTL Compatible 16 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **LOW POWER CMOS**
 - 90 mA Typical I_{cc}
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TWELVE OUTPUT LOGIC MACROCELLS**
 - Uses Standard 22V10 Macrocells
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

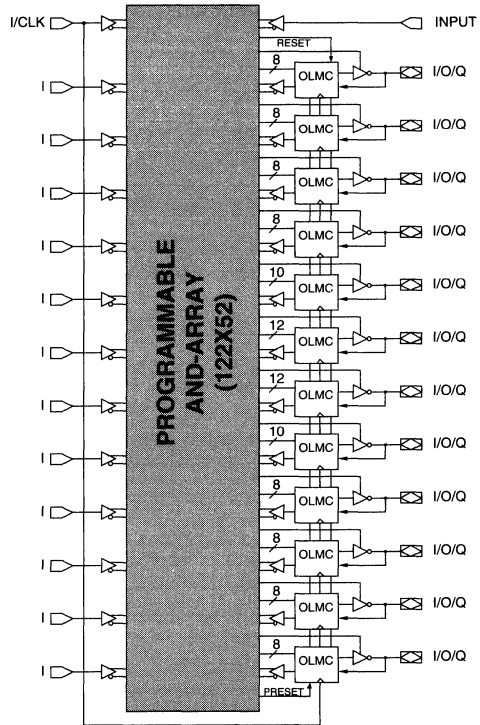
DESCRIPTION

The GAL26CV12, at 7.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance 28-pin PLD available on the market. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

Expanding upon the industry standard 22V10 architecture, the GAL26CV12 eliminates the learning curve typically associated with using a new device architecture. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL26CV12 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

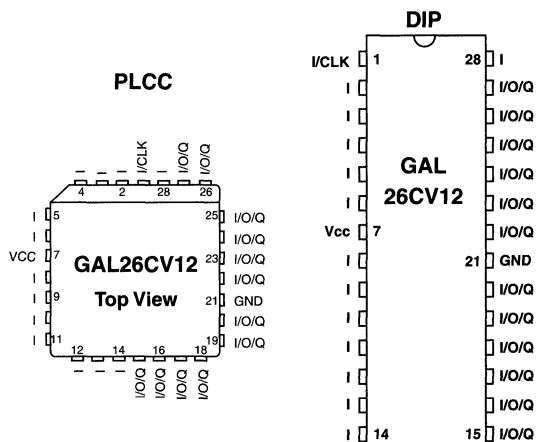
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



3

PACKAGE DIAGRAMS



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GAL26CV12 ORDERING INFORMATION

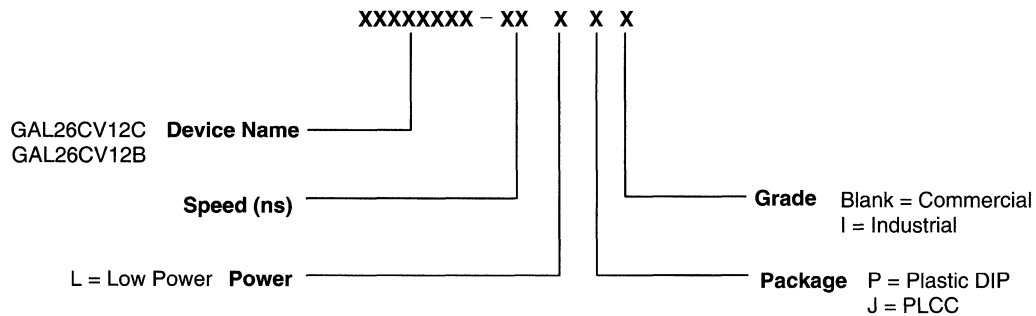
Commercial Grade Specifications

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			130	GAL26CV12C-7LJ	28-Lead PLCC
10	7	7	130	GAL26CV12B-10LP	28-Pin Plastic DIP
			130	GAL26CV12B-10LJ	28-Lead PLCC
15	10	8	130	GAL26CV12B-15LP	28-Pin Plastic DIP
			130	GAL26CV12B-15LJ	28-Lead PLCC
20	12	12	130	GAL26CV12B-20LP	28-Pin Plastic DIP
			130	GAL26CV12B-20LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	7	7	150	GAL26CV12C-10LPI	28-Pin Plastic DIP
			150	GAL26CV12C-10LJI	28-Lead PLCC
15	10	8	150	GAL26CV12B-15LPI	28-Pin Plastic DIP
			150	GAL26CV12B-15LJI	28-Lead PLCC
20	12	12	150	GAL26CV12B-20LPI	28-Pin Plastic DIP
			150	GAL26CV12B-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



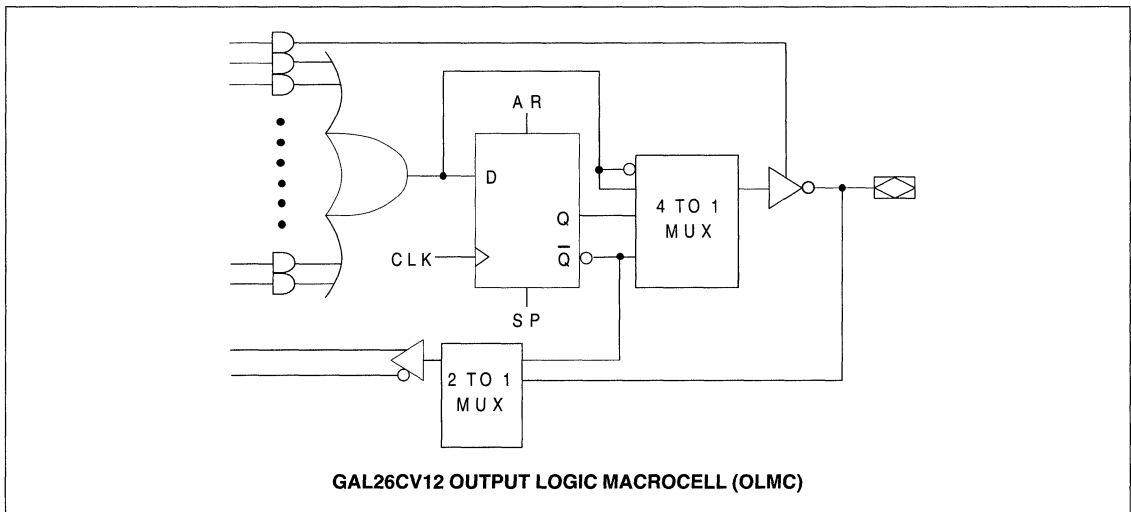
OUTPUT LOGIC MACROCELL (OLMC)

The GAL26CV12 has a variable number of product terms per OLMC. Of the twelve available OLMCs, two OLMCs have access to twelve product terms (pins 20 and 22), two have access to ten product terms (pins 19 and 23), and the other eight OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL26CV12 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL26CV12 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

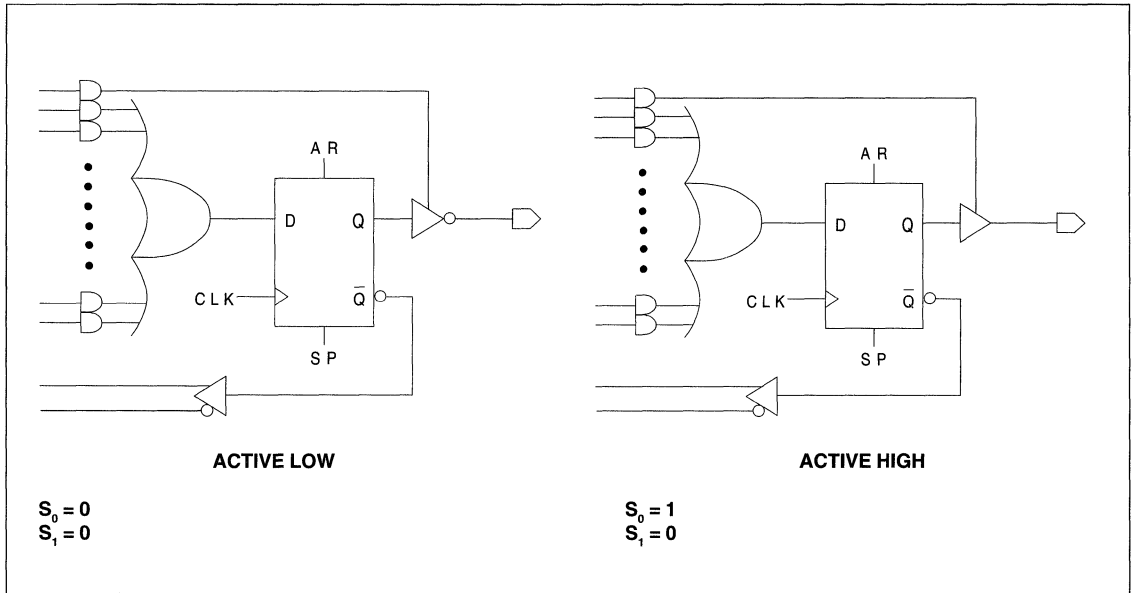
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

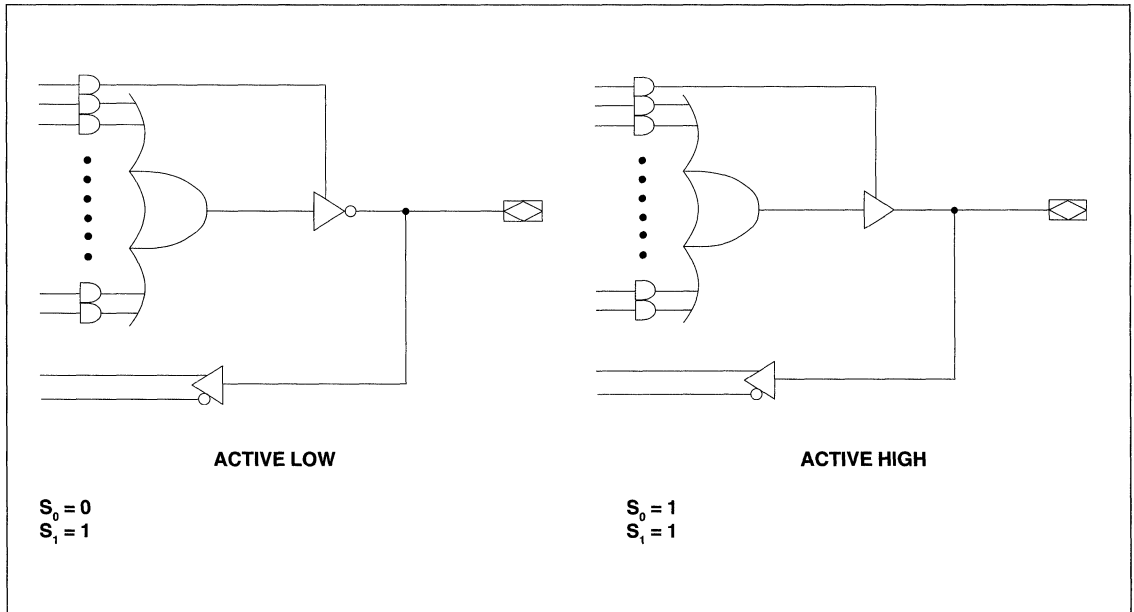
COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

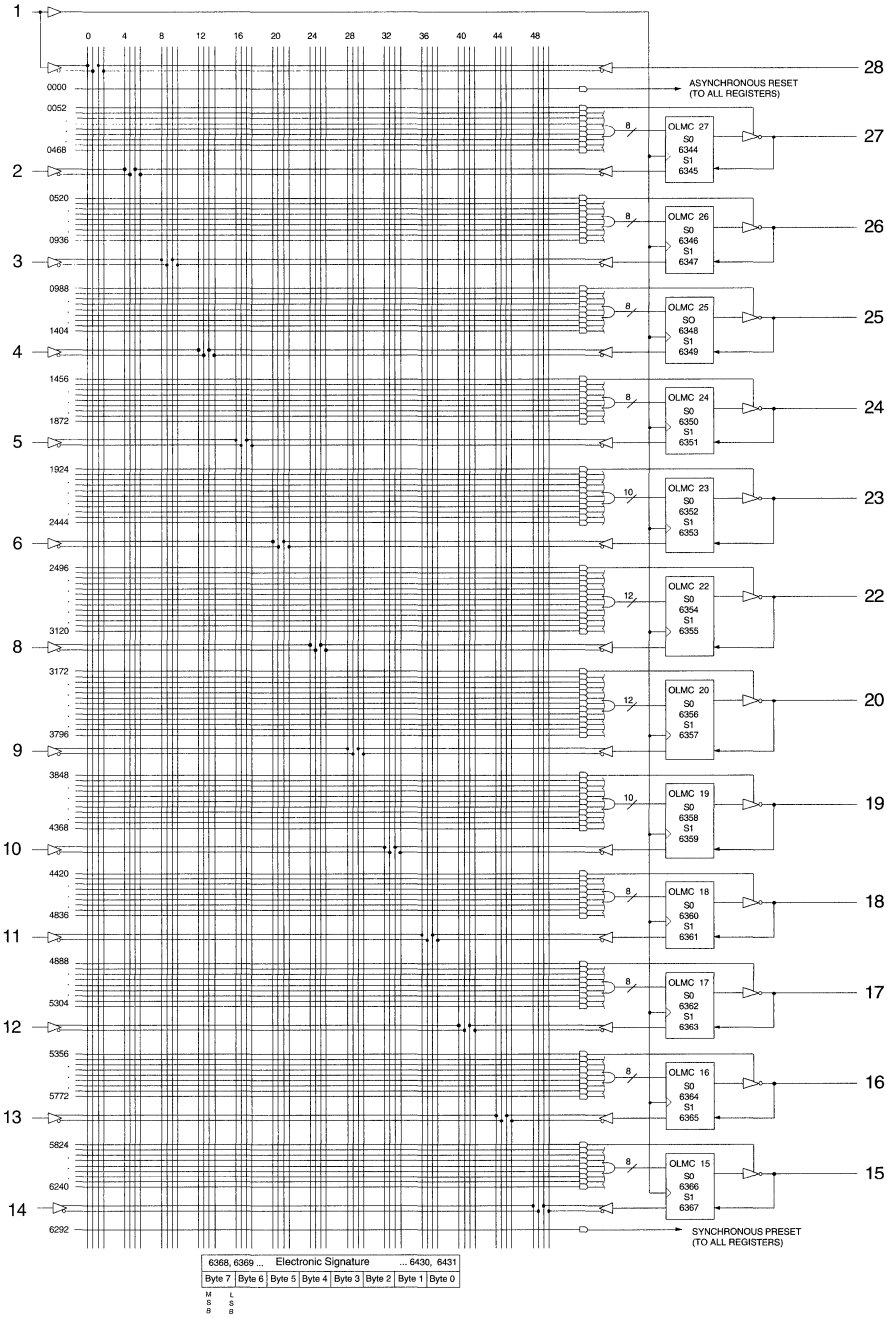
REGISTERED MODE



COMBINATORIAL MODE



GAL26CV12 LOGIC DIAGRAM / JEDEC FUSE MAP



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.5 to +5.5V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 15MHz$ Outputs Open	L-7	—	90	130	mA
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INDUSTRIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 15MHz$ Outputs Open	L-10	—	90	150	mA
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- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	COM		IND		UNITS
			-7		-10		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	1	7.5	1	10	ns
t_{co}	A	Clock to Output Delay	1	4.5	1	7	ns
t_{cf}²	—	Clock to Feedback Delay	—	2.5	—	2.5	ns
t_{su}	—	Setup Time, Input or Feedback before Clock ↑	6	—	7	—	ns
t_h	—	Hold Time, Input or Feedback after Clock ↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	95.2	—	71.4	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	117.6	—	105	—	MHz
	A	Maximum Clock Frequency with No Feedback	142.8	—	105	—	MHz
t_{wh}	—	Clock Pulse Duration, High	3.5	—	4	—	ns
t_{wl}	—	Clock Pulse Duration, Low	3.5	—	4	—	ns
t_{en}	B	Input or I/O to Output Enabled	1	7.5	1	10	ns
t_{dis}	C	Input or I/O to Output Disabled	1	7.5	1	9	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	1	9	1	13	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	7	—	8	—	ns
t_{arr}	—	Asynchronous Reset to Clock ↑ Recovery Time	5	—	8	—	ns
t_{spr}	—	Synchronous Preset to Clock ↑ Recovery Time	5	—	10	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.

 3) Refer to **f_{max} Specification** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	8	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	8	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to +75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

Industrial Devices:

Ambient Temperature (T_A) -40 to 85°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.5 to +5.5V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 15MHz$	L-10/-15/-20	—	90	130	mA
		Outputs Open					

INDUSTRIAL

ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V \quad f_{toggle} = 15MHz$	L-15/-20	—	90	150	mA
		Outputs Open					

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	COM		COM / IND		COM / IND		UNITS
			-10		-15		-20		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	3	10	3	15	3	20	ns
t_{co}	A	Clock to Output Delay	2	7	2	8	2	12	ns
t_{cf}²	—	Clock to Feedback Delay	—	2.5	—	2.5	—	10	ns
t_{su1}	—	Setup Time, Input or Feedback before Clock ↑	7	—	10	—	12	—	ns
t_{su2}	—	Setup Time, SP before Clock ↑	10	—	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock ↑	0	—	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	71.4	—	55.5	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	105	—	80	—	45.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	105	—	83.3	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	6	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	6	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	3	10	3	15	3	20	ns
t_{dis}	C	Input or I/O to Output Disabled	3	10	3	15	3	20	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	3	13	3	20	3	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	8	—	10	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	8	—	10	—	15	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	10	—	12	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Specification** section.

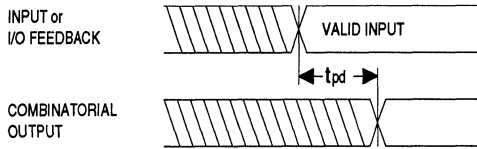
 3) Refer to **f_{max} Specification** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

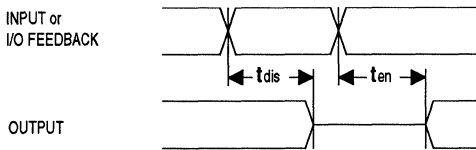
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	8	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	8	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

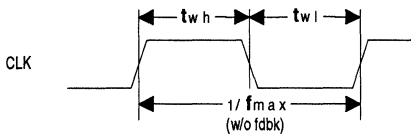
SWITCHING WAVEFORMS



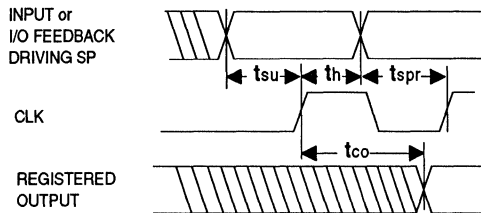
Combinatorial Output



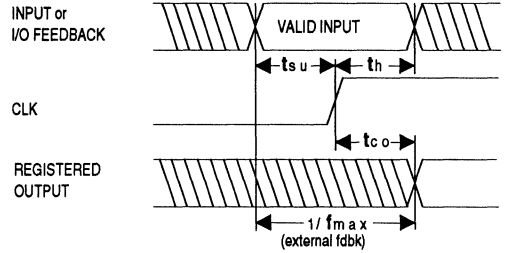
Input or I/O to Output Enable/Disable



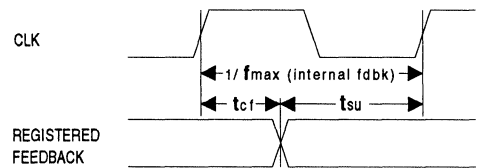
Clock Width



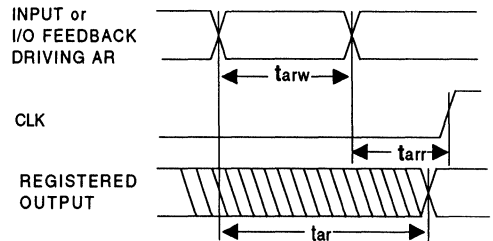
Synchronous Preset



Registered Output

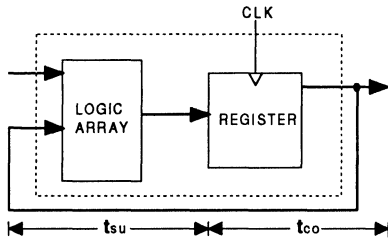


fmax with Feedback



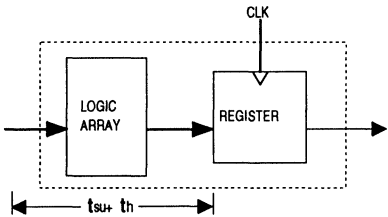
Asynchronous Reset

f_{max} SPECIFICATIONS



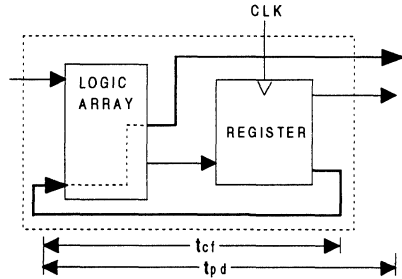
f_{max} with External Feedback 1/(t_{su}+t_{co})

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback 1/(t_{su}+t_{cf})

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback (t_{cf} = 1/f_{max} - t_{su}). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

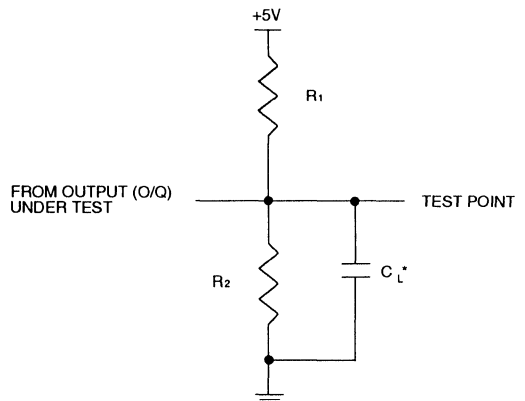
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Times	C-7/-10	1.5ns 10% – 90%
	B-10/-15/-20	3ns 10% – 90%
Input Timing Reference Levels	1.5V	
Output Timing Reference Levels	1.5V	
Output Load	See Figure	

3-state levels are measured 0.5V from steady-state active level.

GAL26CV12 Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	5pF
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL26CV12 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL26CV12 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL26CV12 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential for latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in normal machine operation. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

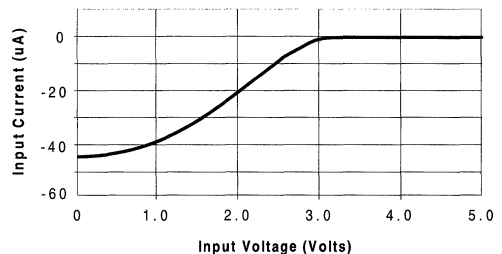
The GAL26CV12 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

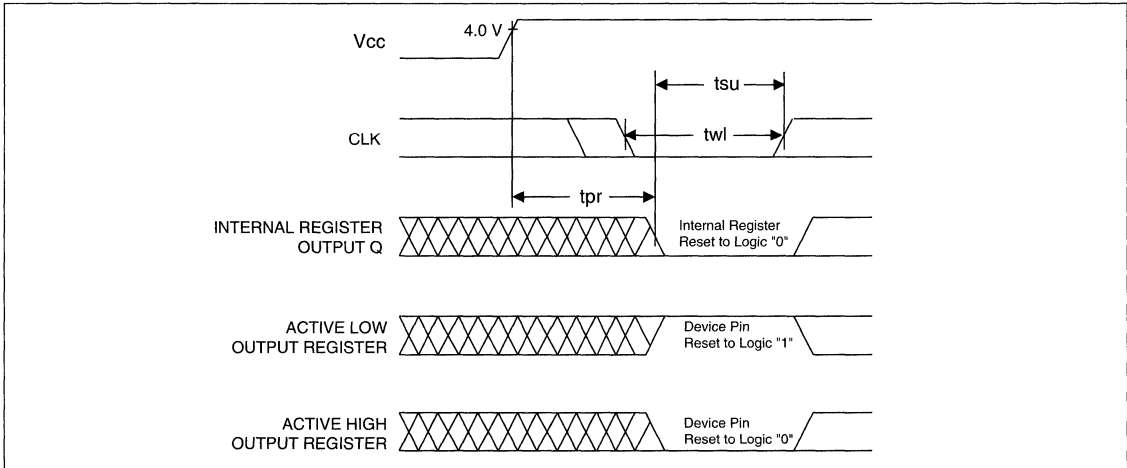
GAL26CV12 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL logic.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device.

Typical Input Current



POWER-UP RESET

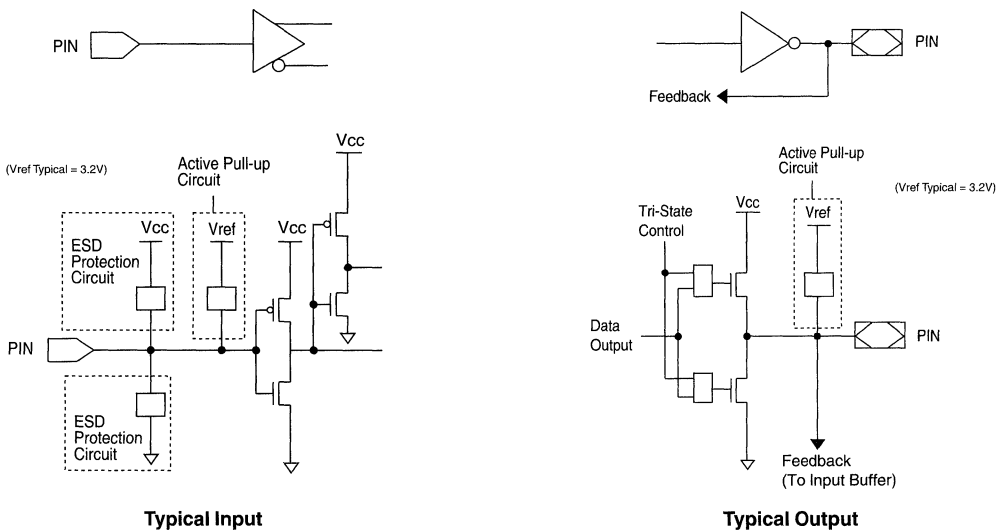


3

Circuitry within the GAL26CV12 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some

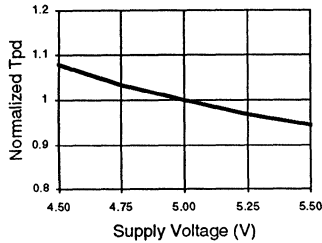
conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

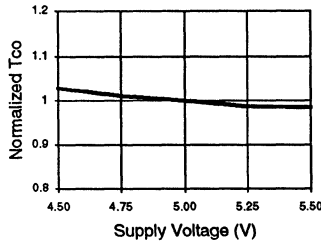


GAL26CV12C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

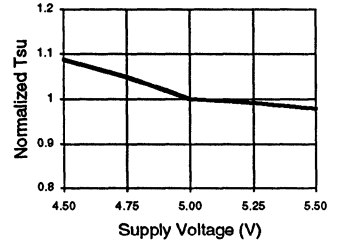
Normalized Tpd vs Vcc



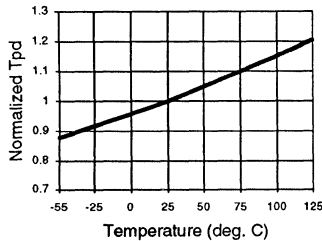
Normalized Tco vs Vcc



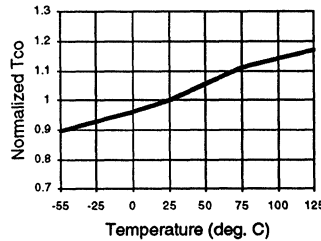
Normalized Tsu vs Vcc



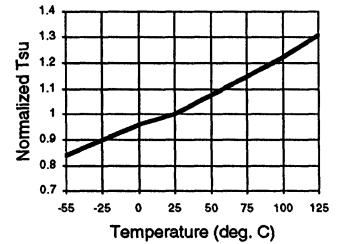
Normalized Tpd vs Temp



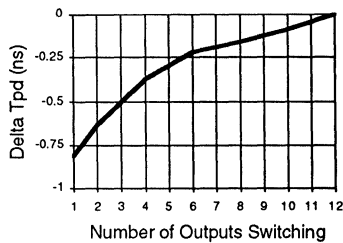
Normalized Tco vs Temp



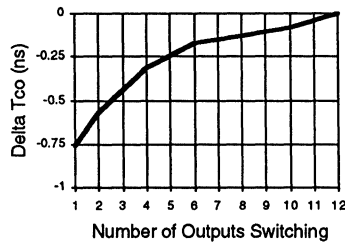
Normalized Tsu vs Temp



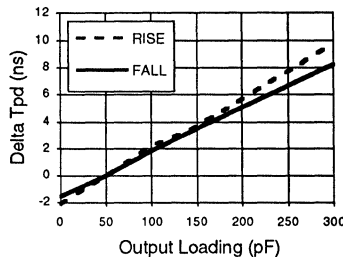
Delta Tpd vs # of Outputs Switching



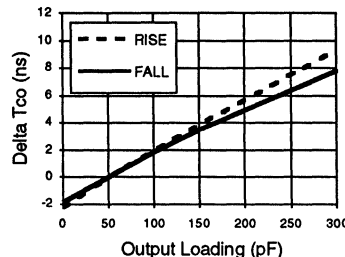
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

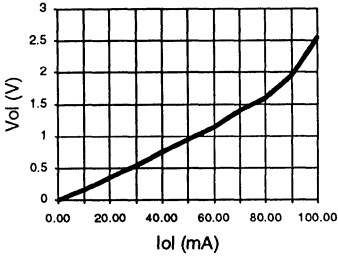


Delta Tco vs Output Loading

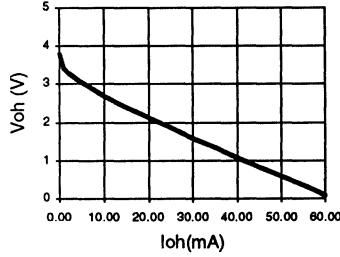


GAL26CV12C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

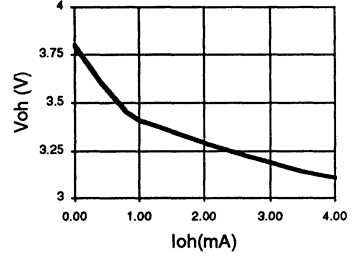
Vol vs Iol



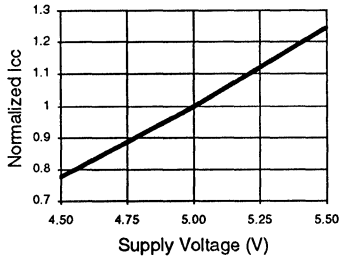
Voh vs Ioh



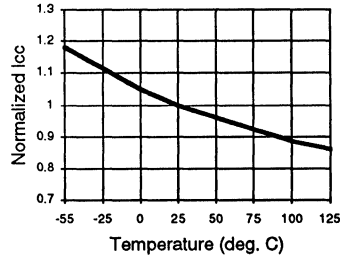
Voh vs Ioh



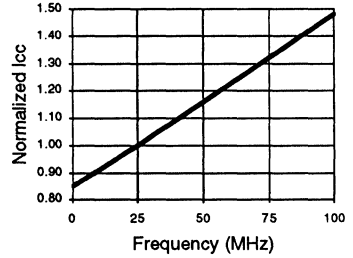
Normalized Icc vs Vcc



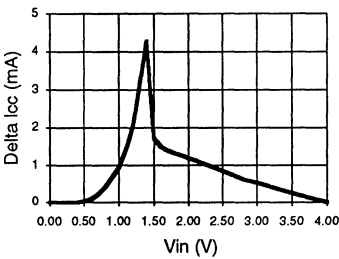
Normalized Icc vs Temp



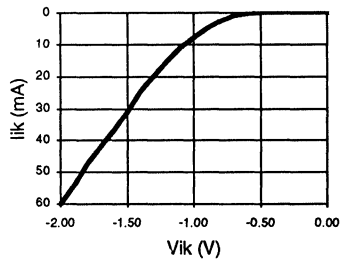
Normalized Icc vs Freq.



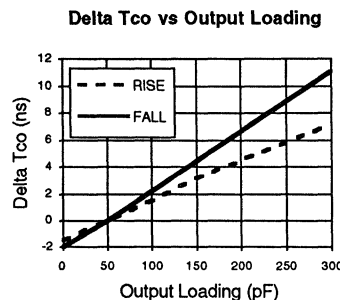
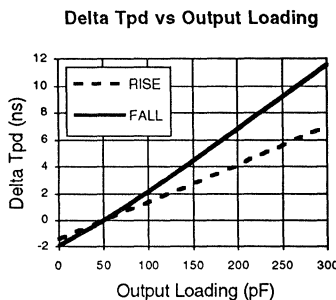
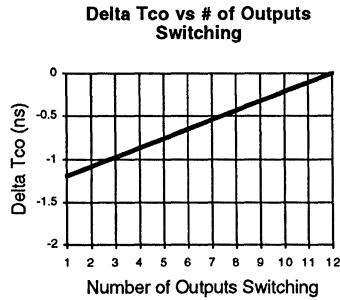
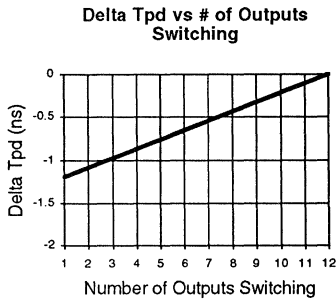
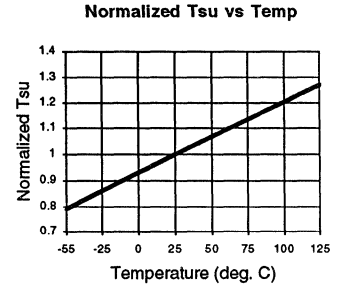
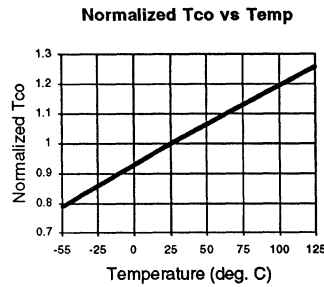
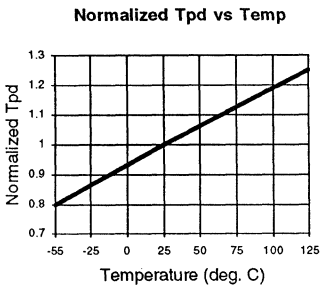
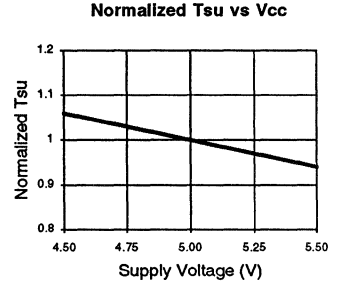
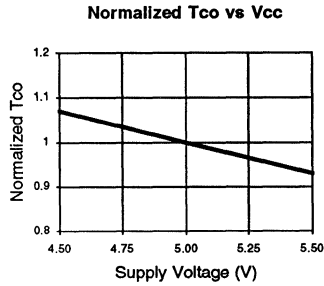
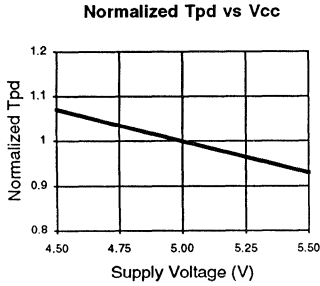
Delta Icc vs Vin (1 input)



Input Clamp (Vik)

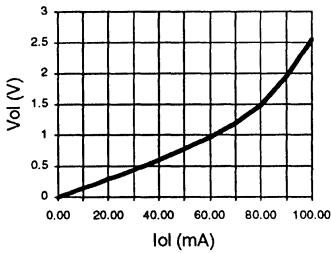


GAL26CV12B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

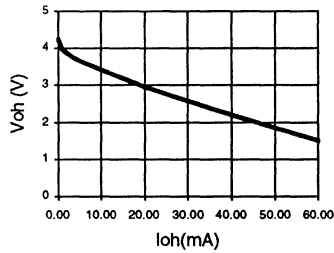


GAL26CV12B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

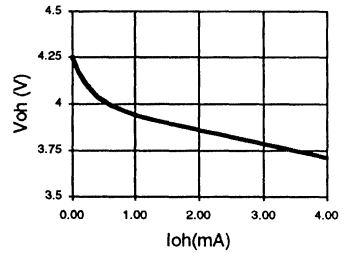
Vol vs Iol



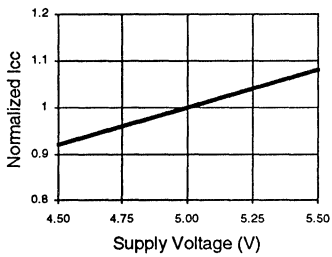
Voh vs Ioh



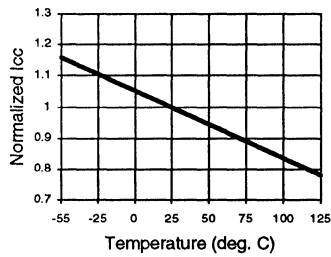
Voh vs Ioh



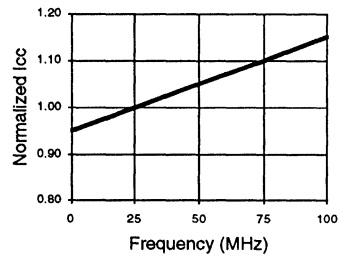
Normalized Icc vs Vcc



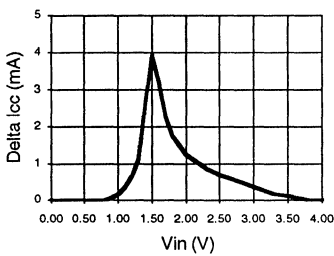
Normalized Icc vs Temp



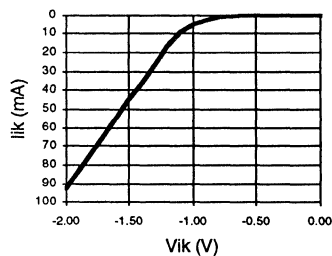
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 30ns Maximum Propagation Delay
 - 27MHz Maximum Frequency
 - 12ns Max. Clock to Output Delay
 - TTL Compatible 16mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **LOW POWER CMOS**
 - 90mA Typical Icc
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **UNPRECEDENTED FUNCTIONAL DENSITY**
 - 78 x 64 x 36 FPLA Architecture
 - 10 Output Logic Macrocells
 - 8 Buried Logic Macrocells
 - 20 Input and I/O Logic Macrocells
- **HIGH-LEVEL DESIGN FLEXIBILITY**
 - Asynchronous or Synchronous Cloning
 - Separate State Register and Input Clock Pins
 - Functional Superset of Existing 24-pin PAL® and FPLA Devices
- **APPLICATIONS INCLUDE:**
 - Sequencers
 - State Machine Control
 - Multiple PLD Device Integration

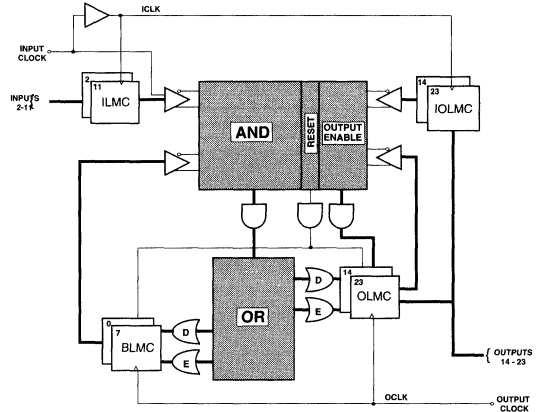
DESCRIPTION

Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers a high degree of functional integration and flexibility in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



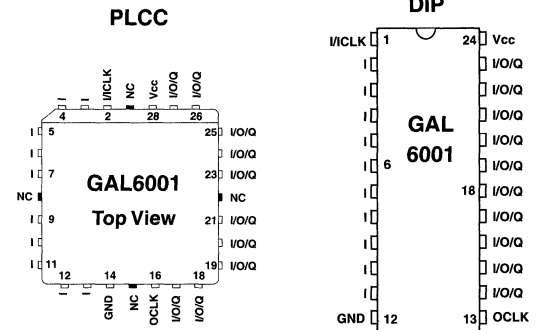
MACROCELL NAMES

ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

I ₀ - I ₁₀	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V _{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION

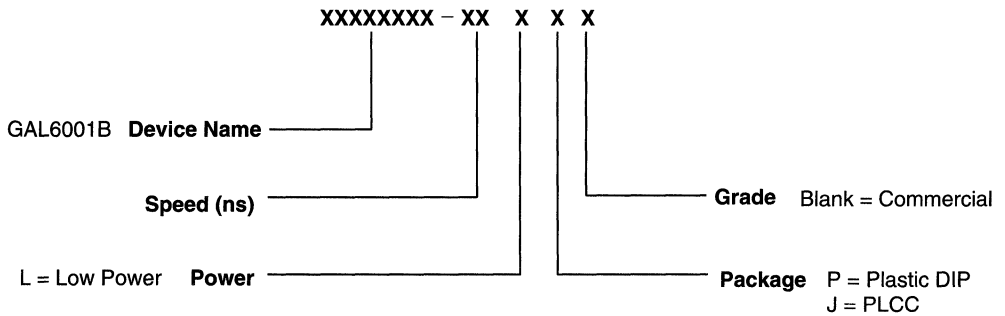


GAL6001 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Fclk (MHz)	Icc (mA)	Ordering #	Package
30	27	150	GAL6001B-30LP	24-Pin Plastic DIP
		150	GAL6001B-30LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide system designers with unparalleled design flexibility. With

the GAL6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinatorial, D-type register with sum term (asynchronous) clock, or D/E-type register. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the "D" XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selected through the "E" XOR.

When the macrocell is configured as a D/E type register, it is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a D-type register with a sum term clock, the register is always enabled and its "E" sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

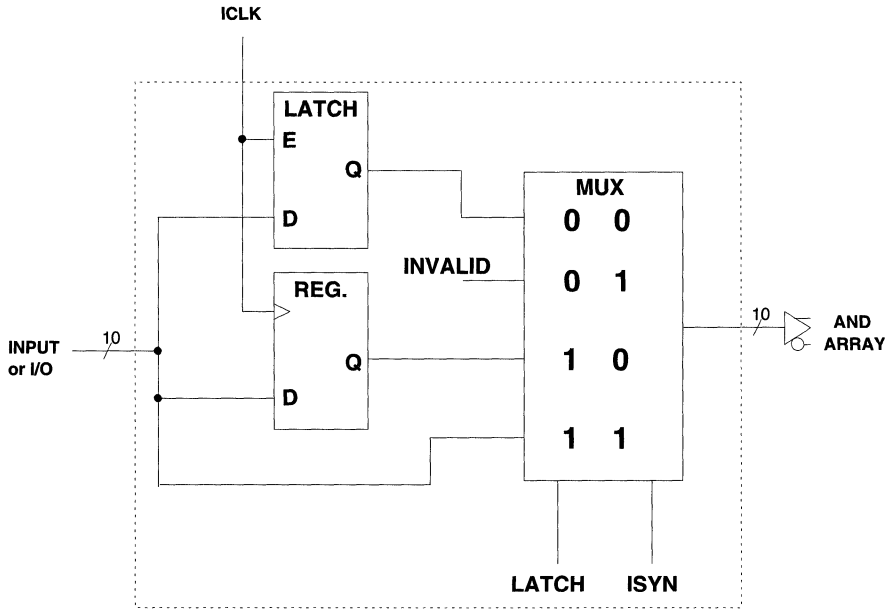
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an output pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

ILMC AND IOLMC CONFIGURATIONS



ILMC/IOLMC

Generic Logic Block Diagram

ILMC (Input Logic Macrocell)
JEDEC Fuse Numbers

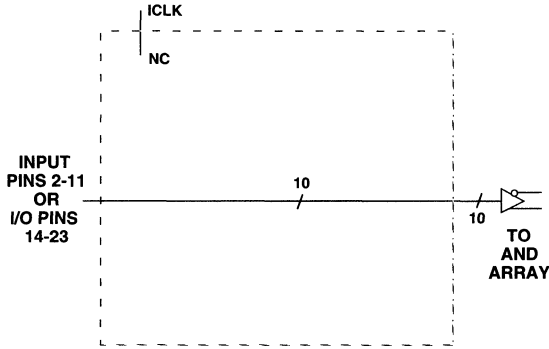
ISYN	LATCH
8218	8219

IOLMC (I/O Logic Macrocell)
JEDEC Fuse Numbers

ISYN	LATCH
8220	8221

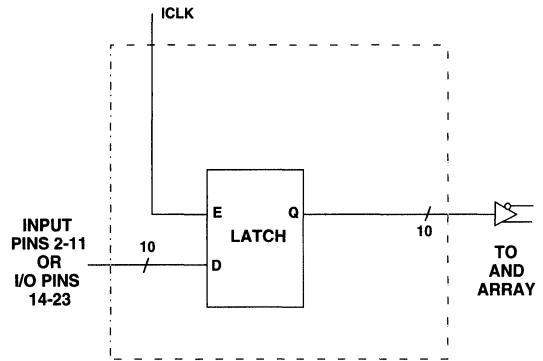
ILMC AND IOLMC CONFIGURATIONS

3



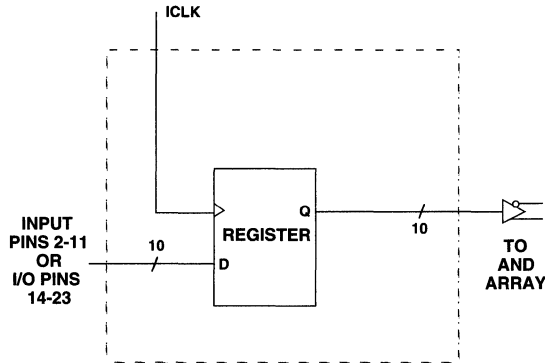
Asynchronous Input

ISYN	LATCH
1	1



Latched Input

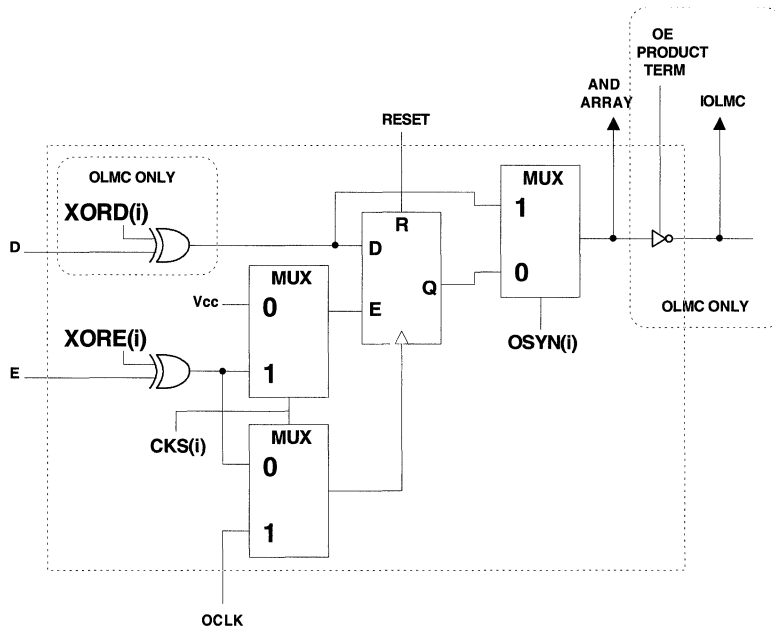
ISYN	LATCH
0	0



Registered Input

ISYN	LATCH
0	1

OLMC AND BLMC CONFIGURATIONS



OLMC/BLMC

Generic Logic Block Diagram

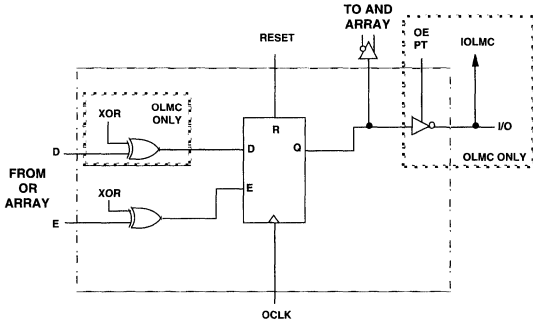
OLMC (Output Logic Macrocell)
JEDEC Fuse Numbers

OLMC	OCLK	OSYN	XORE	XORD
0	8178	8179	8180	8181
1	8182	8183	8184	8185
2	8186	8187	8188	8189
3	8190	8191	8192	8193
4	8194	8195	8196	8197
5	8198	8199	8200	8201
6	8202	8203	8204	8205
7	8206	8207	8208	8209
8	8210	8211	8212	8213
9	8214	8215	8216	8217

BLMC (Buried Logic Macrocell)
JEDEC Fuse Numbers

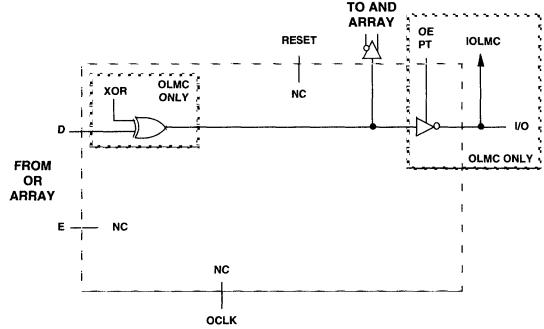
BLMC	OCLK	OSYN	XORE
7	8175	8176	8177
6	8172	8173	8174
5	8169	8170	8171
4	8166	8167	8168
3	8163	8164	8165
2	8160	8161	8162
1	8157	8158	8159
0	8154	8155	8156

OLMC AND BLMC CONFIGURATIONS



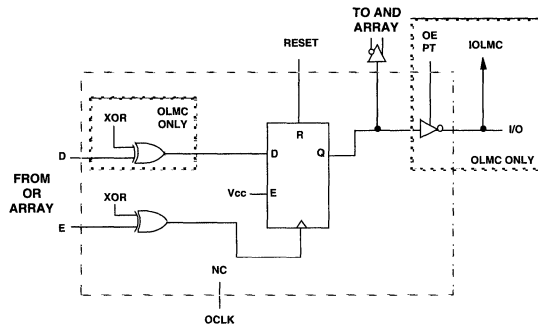
D/E Type Registered

OSYN(i)	OCKS(i)
0	1



Combinatorial

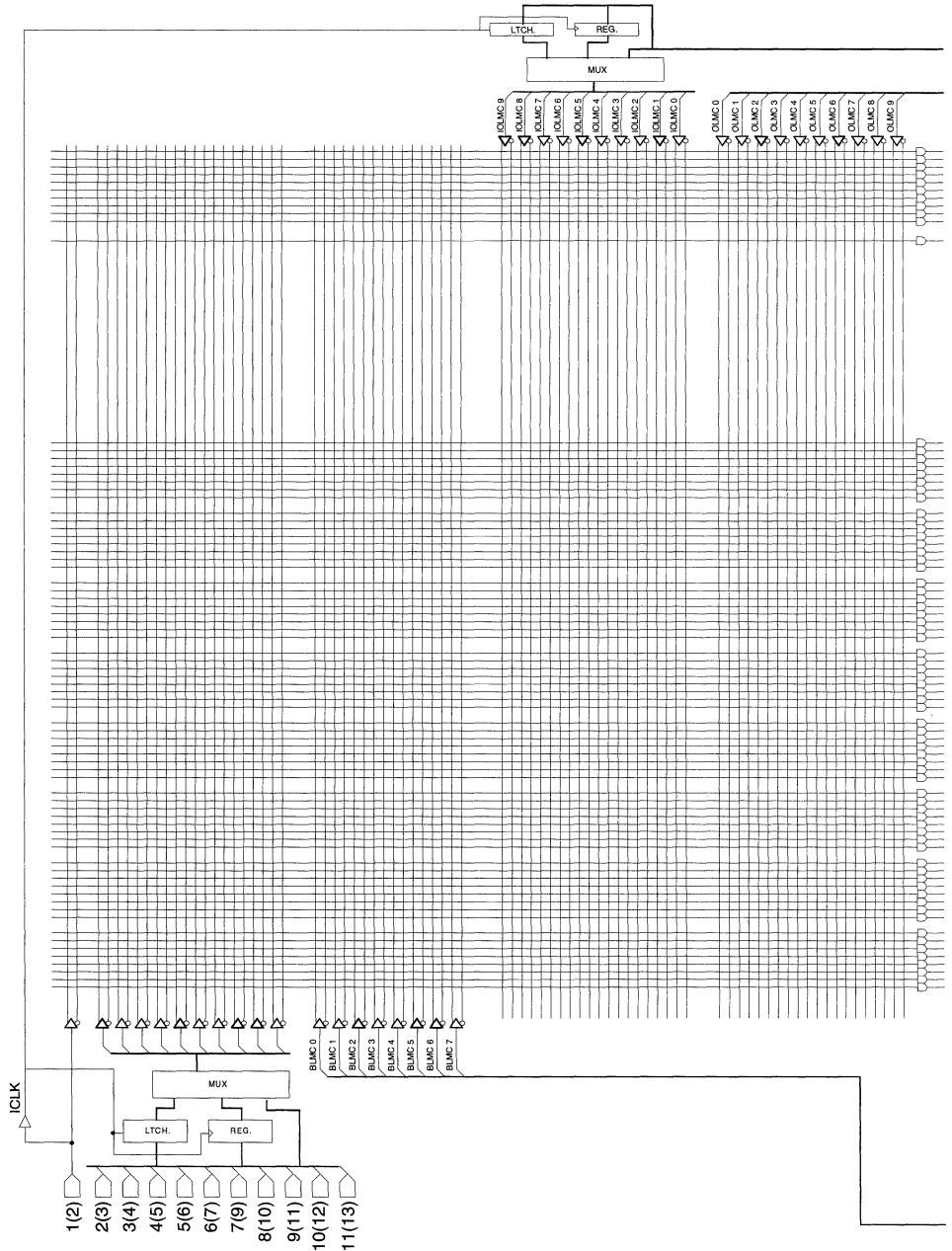
OSYN(i)	OCKS(i)
1	0



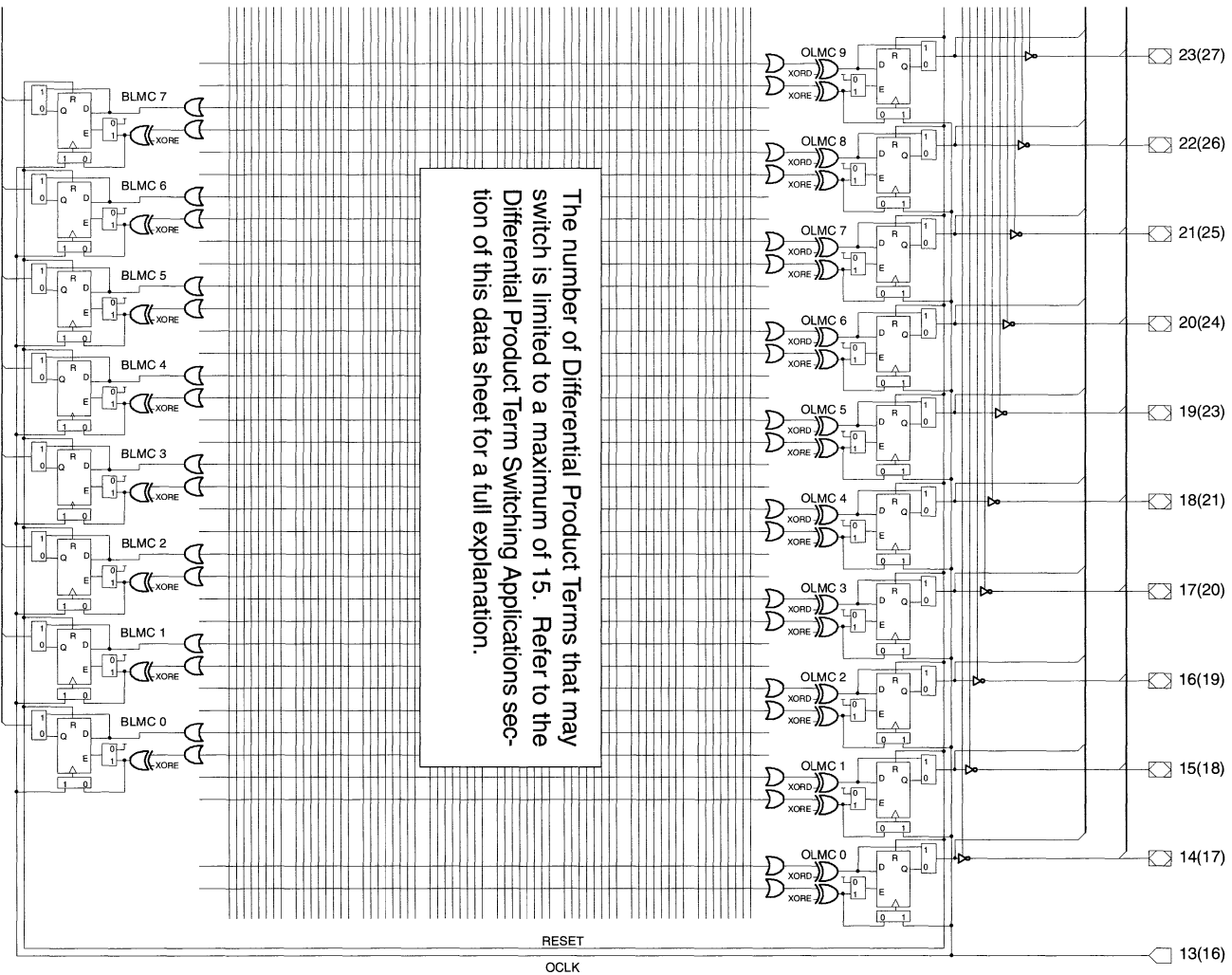
**D Type Register
with Sum Term
Asynchronous Clock**

OSYN(i)	OCKS(i)
0	0

GAL6001 LOGIC DIAGRAM



GAL6001 LOGIC DIAGRAM (Cont.)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V$	-30	—	-130	mA

COMMERCIAL

I_{CC}	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	L -30	—	90	150	mA
	Supply Current	$f_{toggle} = 15MHz$ Outputs Open					

1) The leakage current is due to the internal pull-up on all pins.

2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
$C_{i/O}$	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{i/O} = 2.0V$

*Guaranteed but not 100% tested.

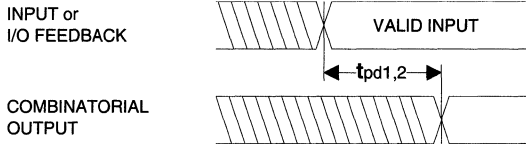
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

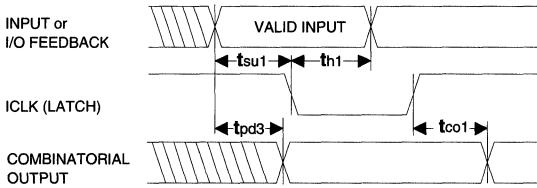
PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		UNITS
			-30		
			MIN.	MAX.	
t_{pd1}	A	Combinatorial Input to Combinatorial Output	—	30	ns
t_{pd2}	A	Feedback or I/O to Combinatorial Output	—	30	ns
t_{pd3}	A	Transparent Latch Input to Combinatorial Output	—	35	ns
t_{co1}	A	Input Latch ICLK to Combinatorial Output Delay	—	35	ns
t_{co2}	A	Input Reg. ICLK to Combinatorial Output Delay	—	35	ns
t_{co3}	A	Output D/E Reg. OCLK to Output Delay	—	12	ns
t_{co4}	A	Output D Reg. Sum Term CLK to Output Delay	—	35	ns
t_{su1}	—	Setup Time, Input before Input Latch ICLK	2.5	—	ns
t_{su2}	—	Setup Time, Input before Input Reg. ICLK	2.5	—	ns
t_{su3}	—	Setup Time, Input or Feedback before D/E Reg. OCLK	25	—	ns
t_{su4}	—	Setup Time, Input or Feedback before D Reg. Sum Term CLK	7.5	—	ns
t_{su5}	—	Setup Time, Input Reg. ICLK before D/E Reg. OCLK	30	—	ns
t_{su6}	—	Setup Time, Input Reg. ICLK before D Reg. Sum Term CLK	15	—	ns
t_{h1}	—	Hold Time, Input after Input Latch ICLK	5	—	ns
t_{h2}	—	Hold Time, Input after Input Reg. ICLK	5	—	ns
t_{h3}	—	Hold Time, Input or Feedback after D/E Reg. OCLK	0	—	ns
t_{h4}	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK	10	—	ns
f_{max}	—	Maximum Clock Frequency, OCLK	27	—	MHz
t_{wh1}	—	ICLK or OCLK Pulse Duration, High	10	—	ns
t_{wh2}	—	Sum Term CLK Pulse Duration, High	15	—	ns
t_{wl1}	—	ICLK or OCLK Pulse Duration, Low	10	—	ns
t_{wl2}	—	Sum Term CLK Pulse Duration, Low	15	—	ns
t_{arw}	—	Reset Pulse Duration	15	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	25	ns
t_{dis}	C	Input or I/O to Output Disabled	—	25	ns
t_{ar}	A	Input or I/O to Asynchronous Reg. Reset	—	35	ns
t_{arr1}	—	Asynchronous Reset to OCLK Recovery Time	20	—	ns
t_{arr2}	—	Asynchronous Reset to Sum Term CLK Recovery Time	10	—	ns

 1) Refer to **Switching Test Conditions** section.

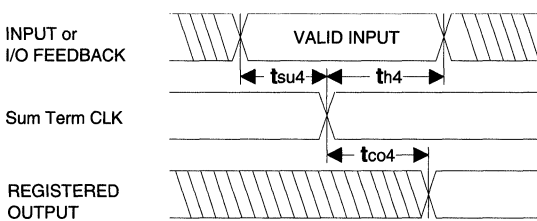
SWITCHING WAVEFORMS



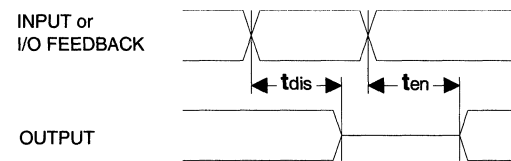
Combinatorial Output



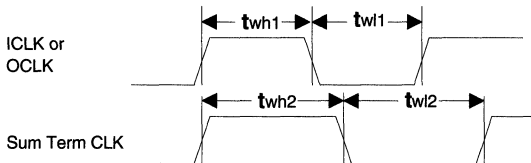
Latched Input



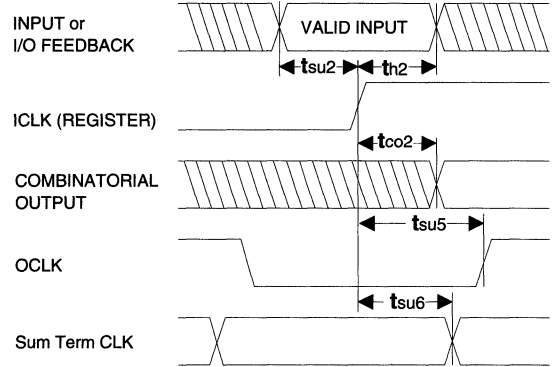
Registered Output (Sum Term CLK)



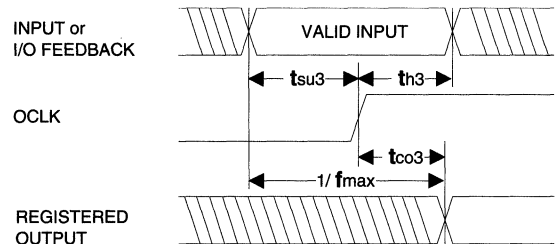
Input or I/O to Output Enable/Disable



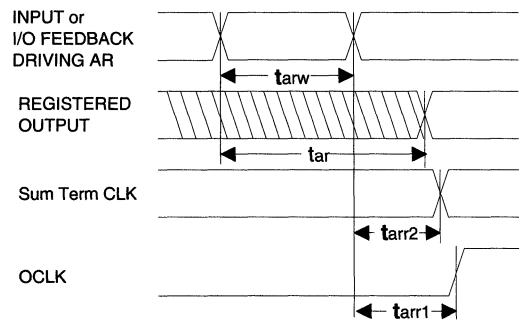
Clock Width



Registered Input

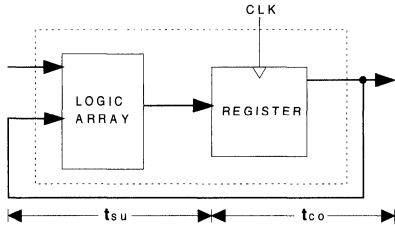


Registered Output (OCLK)



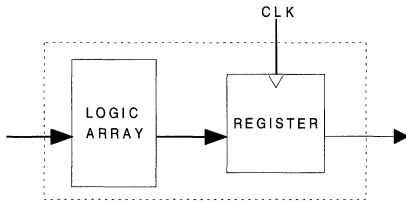
Asynchronous Reset

f_{max} DESCRIPTIONS



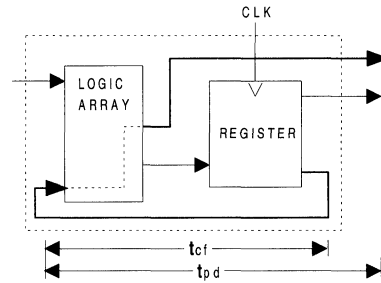
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

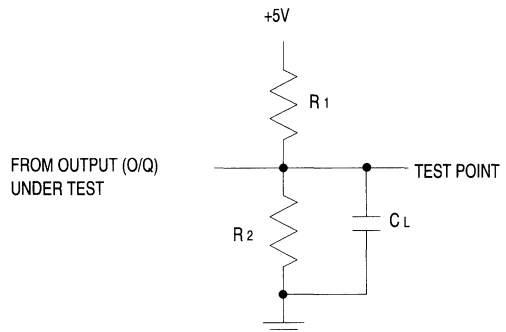
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	5pF
	Active Low	300Ω	390Ω



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ARRAY DESCRIPTION

The GAL6001 contains two E² reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device pins 14-23 to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided in every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

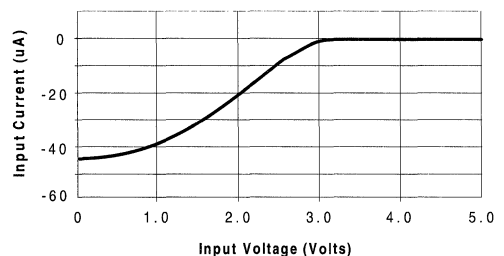
GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

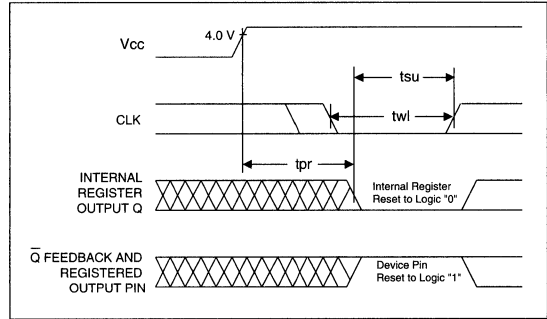
GAL6001 input buffers have active pull-ups within their input structure. This pull-up will cause any unterminated input or I/O to float to a TTL high (logical 1). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce ICC for the device.

Typical Input Pull-up Characteristic



POWER-UP RESET

Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.



DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = | (P\text{-Terms})_{LH} - (P\text{-Terms})_{HL} |$$

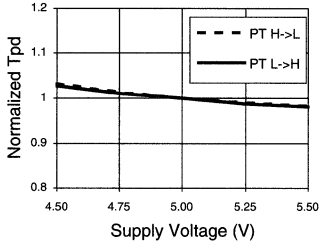
DPTS restricts the number of product terms that can be switched

simultaneously - there is no limit on the number of product terms that can be used.

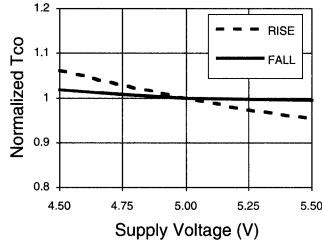
A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering Dept. (Tel: 503-681-0118 or 800-FASTGAL; FAX: 681-3037).

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

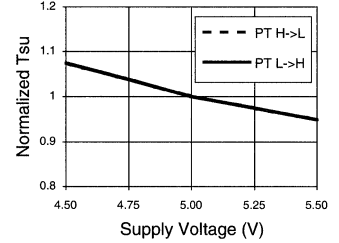
Normalized Tpd vs Vcc



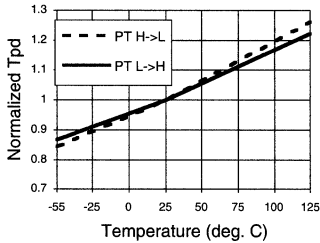
Normalized Tco vs Vcc



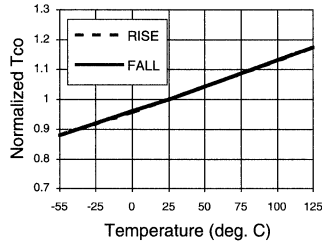
Normalized Tsu vs Vcc



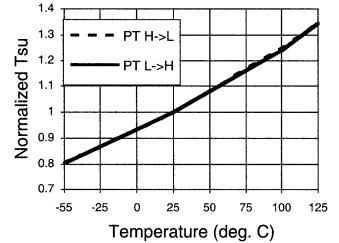
Normalized Tpd vs Temp



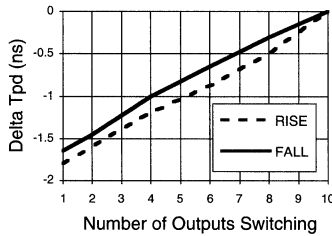
Normalized Tco vs Temp



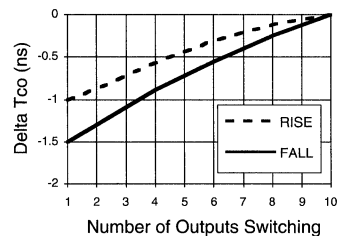
Normalized Tsu vs Temp



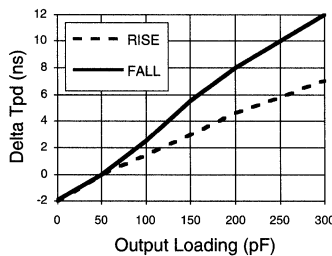
Delta Tpd vs # of Outputs Switching



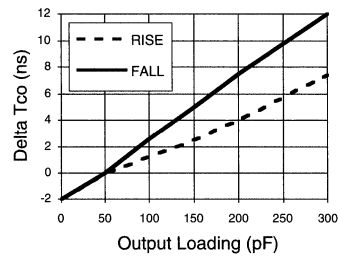
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

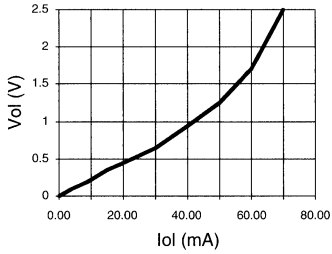


Delta Tco vs Output Loading

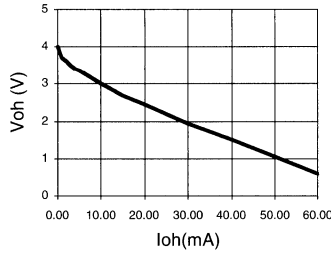


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

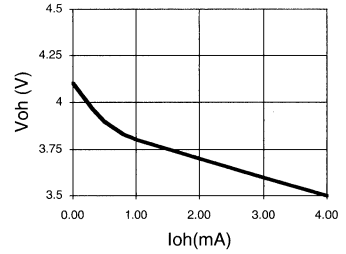
Vol vs Iol



Voh vs Ioh

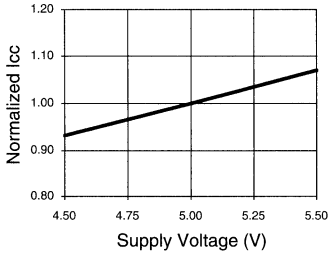


Voh vs Ioh

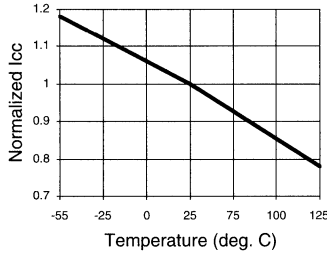


3

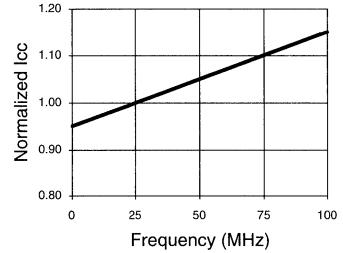
Normalized Icc vs Vcc



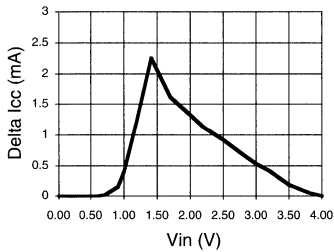
Normalized Icc vs Temp



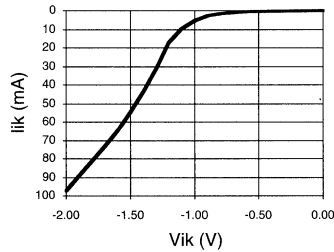
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 15ns Maximum Propagation Delay
 - 75MHz Maximum Frequency
 - 6.5ns Max. Clock to Output Delay
 - TTL Compatible 16mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **LOW POWER CMOS**
 - 90mA Typical I_{cc}
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **UNPRECEDENTED FUNCTIONAL DENSITY**
 - 78 x 64 x 36 FPLA Architecture
 - 10 Output Logic Macrocells
 - 8 Buried Logic Macrocells
 - 20 Input and I/O Logic Macrocells
- **HIGH-LEVEL DESIGN FLEXIBILITY**
 - Asynchronous or Synchronous Clocking
 - Separate State Register and Input Clock Pins
 - Functional Superset of Existing 24-pin PAL® and FPLA Devices
- **APPLICATIONS INCLUDE:**
 - Sequencers
 - State Machine Control
 - Multiple PLD Device Integration

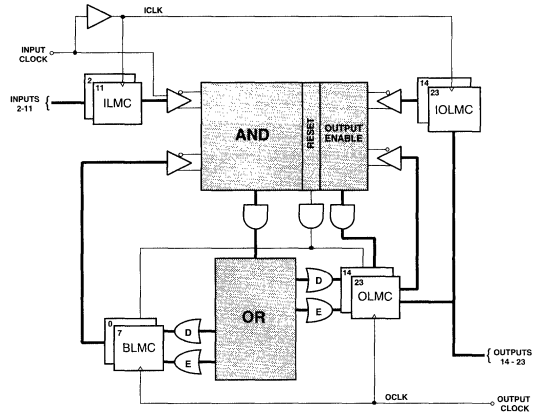
DESCRIPTION

Having an FPLA architecture, the GAL6002 provides superior flexibility in state-machine design. The GAL6002 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package. E²CMOS technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The GAL6002 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. As a result, Lattice is able to guarantee 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



MACROCELL NAMES

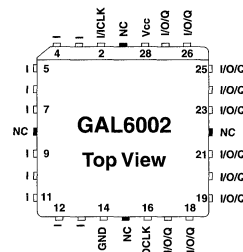
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

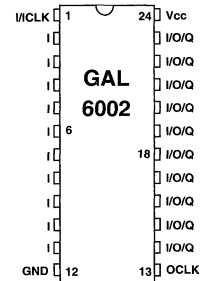
I ₀ - I ₁₀	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V _{CC}	POWER (+5V)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION

PLCC



DIP

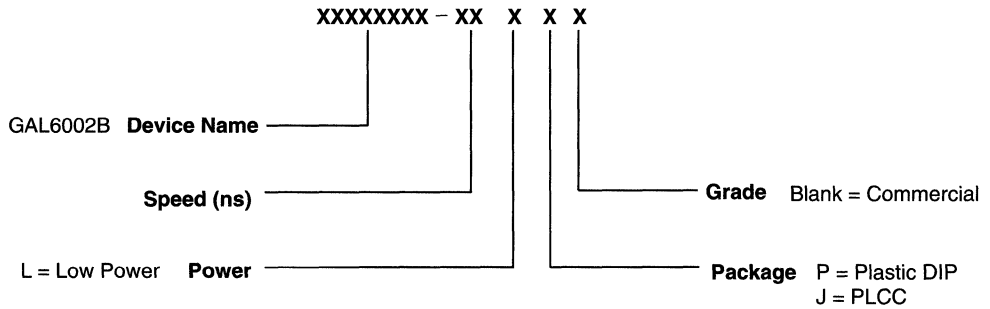


GAL6002 COMMERCIAL DEVICE ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Fclk (MHz)	Icc (mA)	Ordering #	Package
15	75	135	GAL6002B-15LP	24-Pin Plastic DIP
		135	GAL6002B-15LJ	28-Lead PLCC
20	60	135	GAL6002B-20LP	24-Pin Plastic DIP
		135	GAL6002B-20LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6002 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is individually configurable as asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Individually configurable inputs provide system designers with unparalleled design flexibility. With the GAL6002, external input registers and latches are not necessary.

Both the ILMC and the IOLMC are individually configurable and the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations and its associated fuse numbers are shown in the diagrams on the following pages. Note that these programmable cells are configured by the logic compiler software. The user does not need to manually manipulate these architecture bits.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, D-type register with sum term (asynchronous) clock, or D/E-type register. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the programmable polarity control cell called XOR. Polarity selection for BLMCs is selected through the true and complement forms of their feedbacks to the AND array. Polarity of all E (Enable) sum terms is selected through the XORE programmable cells.

When the output or buried logic macrocell is configured as a D/E type register, the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with count hold and state hold functions.

When the macrocell is configured as a D type register with a sum term clock, the register is always enabled and the associated "E"

sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

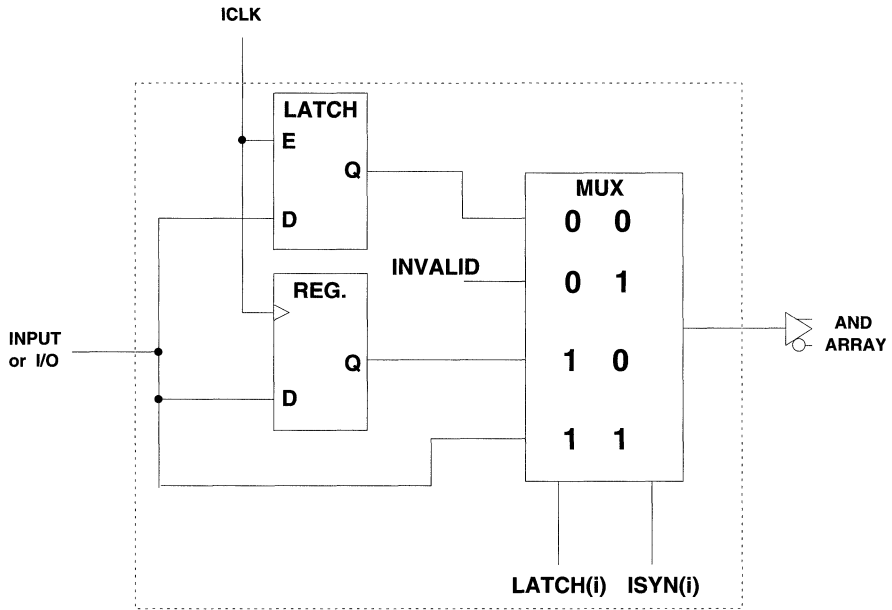
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. All registers reset to logic zero. With the inverting output buffers, the output pins will reset to logic one.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried without losing the use of the associated OLMC pin as an input, or dynamically buried with the use of the output enable product term.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS, JK, and T registers with the same efficiency as a dedicated RS, JK, or T registers.

The three macrocell configurations are shown in the diagrams on the following pages. These programmable cells are also configured by the logic compiler software. The user does not need to manually manipulate these architecture bits.

ILMC AND IOLMC CONFIGURATIONS



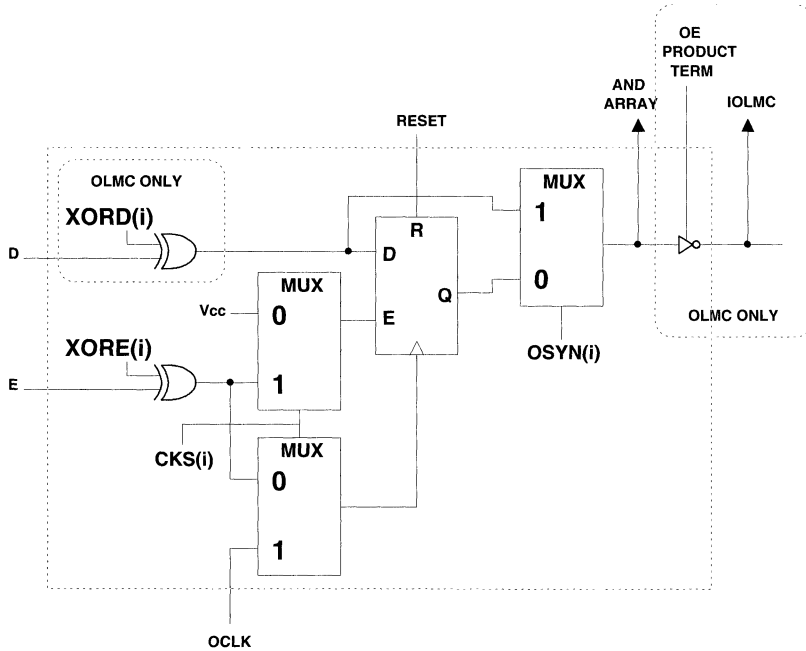
ILMC/IOLMC
Generic Logic Block Diagram

Input Macrocell JEDEC Fuse Numbers

INSYNC	INLATCH	ILMC
8218	8219	0
8220	8221	1
8222	8223	2
8224	8225	3
8226	8227	4
8228	8229	5
8230	8231	6
8232	8233	7
8234	8235	8
8236	8237	9

I/O Macrocell JEDEC Fuse Numbers

IOSYNC	IOLATCH	IOLMC
8238	8239	9
8240	8241	8
8242	8243	7
8244	8245	6
8246	8247	5
8248	8249	4
8250	8251	3
8252	8253	2
8254	8255	1
8256	8257	0

OLMC AND BLMC CONFIGURATIONS


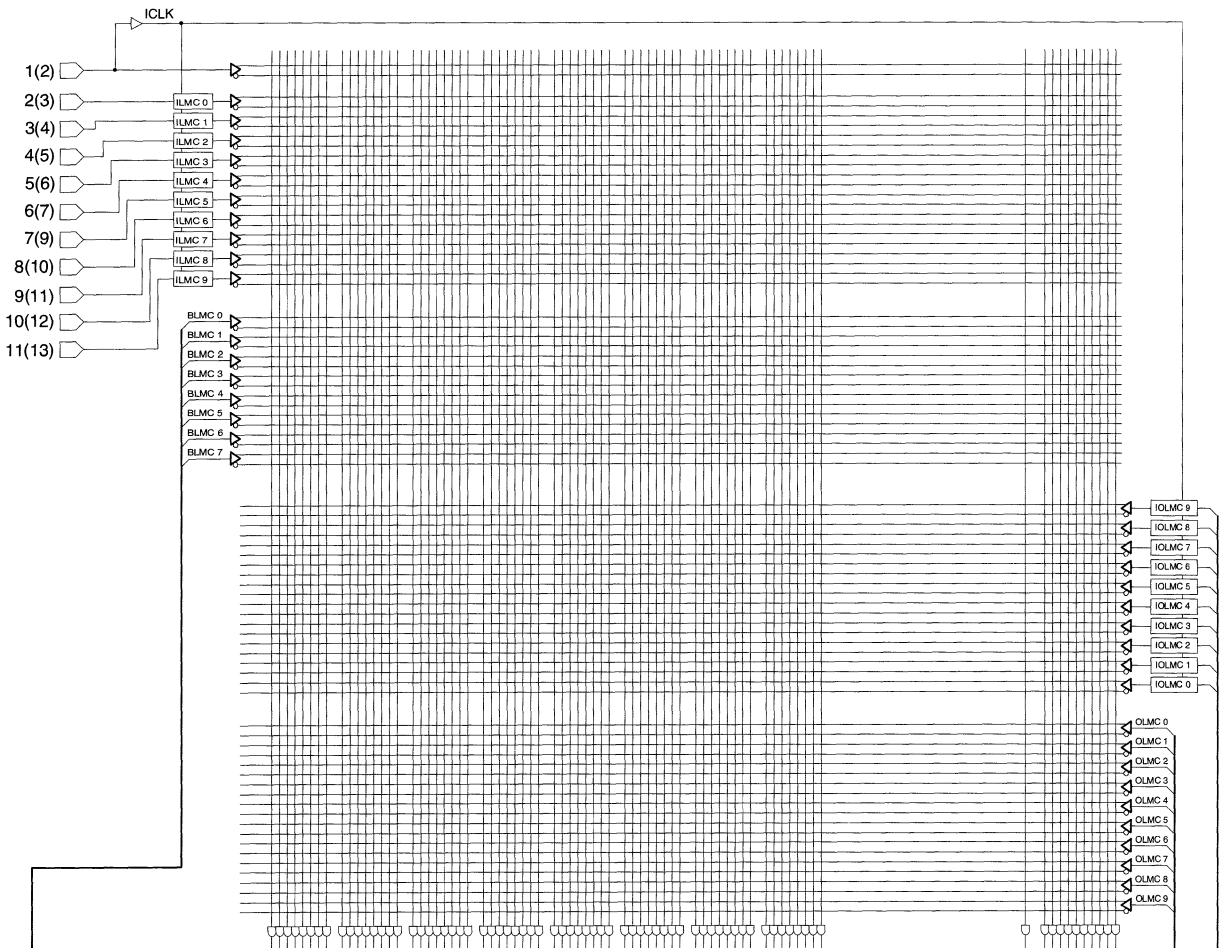
OLMC/BLMC
Generic Logic Block Diagram

OLMC JEDEC Fuse Numbers

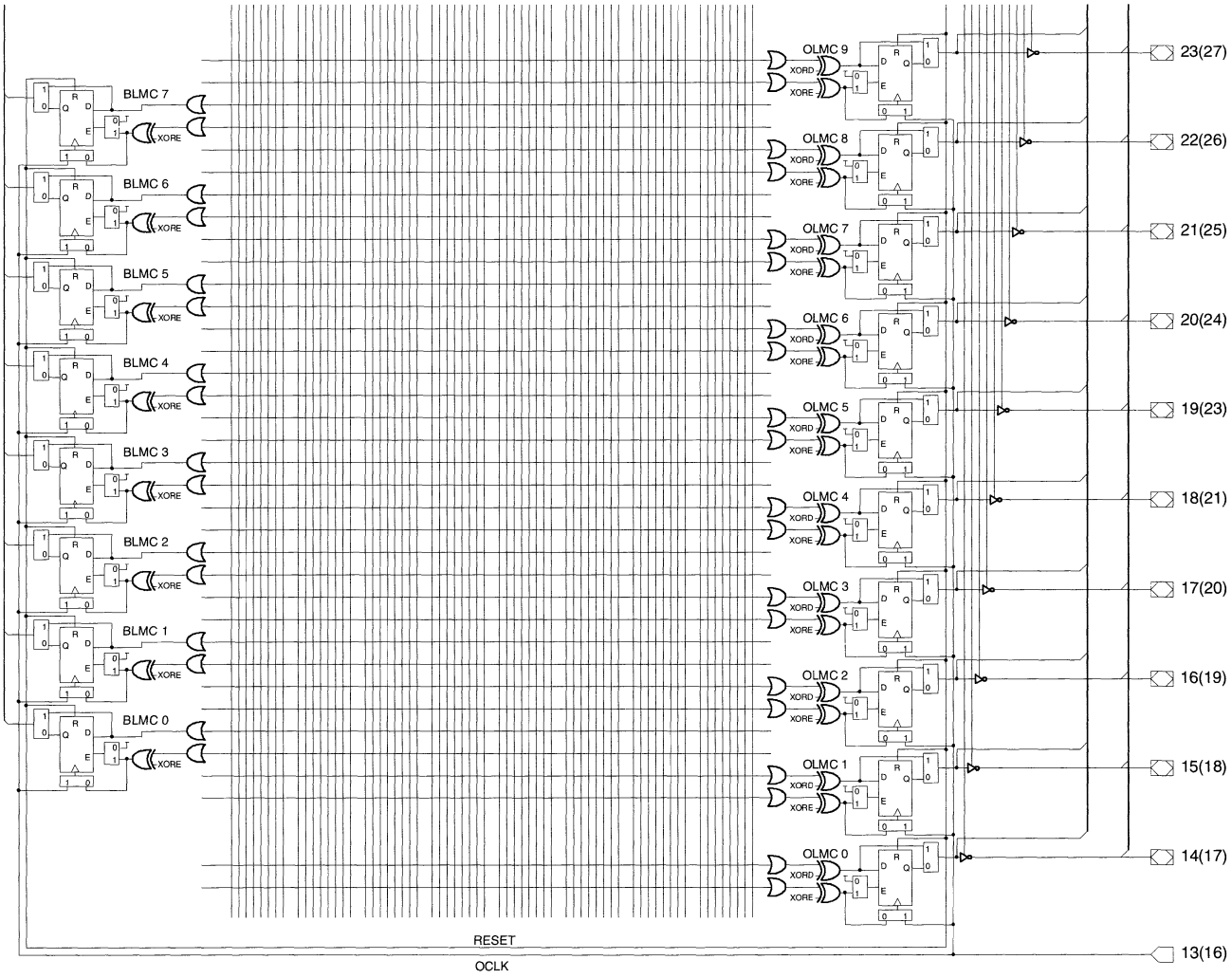
OLMC	CKS	OUTSYNC	XORE	XORD
0	8178	8179	8180	8181
1	8182	8183	8184	8185
2	8186	8187	8188	8189
3	8190	8191	8192	8193
4	8194	8195	8196	8197
5	8198	8199	8200	8201
6	8202	8203	8204	8205
7	8206	8207	8208	8209
8	8210	8211	8212	8213
9	8214	8215	8216	8217

BLMC JEDEC Fuse Numbers

BLMC	CKS	OUTSYNC	XORE
7	8175	8176	8177
6	8172	8173	8174
5	8169	8170	8171
4	8166	8167	8168
3	8163	8164	8165
2	8160	8161	8162
1	8157	8158	8159
0	8154	8155	8156

LOGIC DIAGRAM


LOGIC DIAGRAM (CONT.)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}^1	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \text{ Outputs Open}$	L -15/-20	—	90	135	mA
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- 1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
$C_{I/O}$	I/O Capacitance	8	pF	$V_{CC} = 5.0V, V_{IO} = 2.0V$

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND ¹ .	DESCRIPTION	COM		COM		UNITS
			-15		-20		
			MIN.	MAX.	MIN.	MAX.	
t pd1	A	Combinatorial Input to Combinatorial Output	—	15	—	20	ns
t pd2	A	Feedback or I/O to Combinational Output	—	15	—	20	ns
t pd3	A	Transparent Latch Input to Combinatorial Output	—	18	—	23	ns
t co1	A	Input Latch ICLK to Combinatorial Output Delay	—	20	—	25	ns
t co2	A	Input Reg. ICLK to Combinatorial Output Delay	—	20	—	25	ns
t co3	A	Output D/E Reg. OCLK to Output Delay	—	6.5	—	8	ns
t co4	A	Output D Reg. Sum Term CLK to Output Delay	—	18	—	20	ns
t cf1 ²	—	Output D/E Reg. OCLK to Buried Feedback Delay	—	3.6	—	7	ns
t cf2 ²	—	Output D Reg. STCLK to Buried Feedback Delay	—	10.1	—	13	ns
t su1	—	Setup Time, Input before Input Latch ICLK	1.5	—	2	—	ns
t su2	—	Setup Time, Input before Input Reg. ICLK	1.5	—	2	—	ns
t su3	—	Setup Time, Input or Fdbk before D/E Reg. OCLK	11.5	—	13	—	ns
t su4	—	Setup Time, Input or Fdbk before D Reg. Sum Term CLK	5	—	7	—	ns
t su5	—	Setup Time, Input Reg. ICLK before D/E Reg. OCLK	15	—	20	—	ns
t su6	—	Setup Time, Input Reg. ICLK before D Reg. Sum Term CLK	7	—	9	—	ns
t h1	—	Hold Time, Input after Input Latch ICLK	3	—	4	—	ns
t h2	—	Hold Time, Input after Input Reg. ICLK	3	—	4	—	ns
t h3	—	Hold Time, Input or Feedback after D/E Reg. OCLK	0	—	0	—	ns
t h4	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK	4	—	6	—	ns
f max1 ³	—	Max. Clock Frequency w/External Feedback, $1/(\mathbf{t}$ su3+ \mathbf{t} co3)	55.5	—	47.6	—	MHz
f max2 ³	—	Max. Clock Frequency w/External Feedback, $1/(\mathbf{t}$ su4+ \mathbf{t} co4)	43.4	—	37	—	MHz
f max3 ³	—	Max. Clock Frequency w/Internal Feedback, $1/(\mathbf{t}$ su3+ \mathbf{t} cf1)	66	—	50	—	MHz
f max4 ³	—	Max. Clock Frequency w/Internal Feedback, $1/(\mathbf{t}$ su4+ \mathbf{t} cf2)	66	—	50	—	MHz
f max5 ³	—	Max. Clock Frequency w/No Feedback, OCLK	75	—	60	—	MHz
f max6 ³	—	Max. Clock Frequency w/No Feedback, STCLK	70	—	60	—	MHz
t wh1	—	ICLK Pulse Duration, High	6	—	7	—	ns
t wh2	—	OCLK Pulse Duration, High	6	—	7	—	ns
t wh3	—	STCLK Pulse Duration, High	7	—	8	—	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.

 3) Refer to **fmax Description** section.

AC SWITCHING CHARACTERISTICS (CONT.)

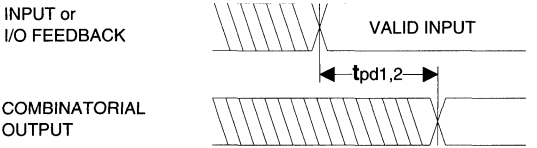
Over Recommended Operating Conditions

PARAMETER	TEST COND'.	DESCRIPTION	COM		COM		UNITS
			-15		-20		
			MIN.	MAX.	MIN.	MAX.	
t_{w1}	—	ICLK Pulse Duration, Low	6	—	7	—	ns
t_{w2}	—	OCLK Pulse Duration, Low	6	—	7	—	ns
t_{w3}	—	STCLK Pulse Duration, Low	7	—	8	—	ns
t_{arw}	—	Reset Pulse Duration	12	—	15	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	ns
t_{ar}	A	Input or I/O to Asynchronous Reg. Reset	—	16	—	20	ns
t_{arr1}	—	Asynchronous Reset to OCLK Recovery Time	11	—	14	—	ns
t_{arr2}	—	Asynchronous Reset to Sum Term CLK Recovery Time	4	—	6	—	ns

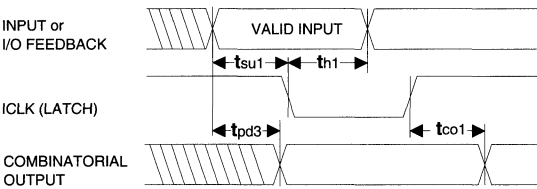
 1) Refer to **Switching Test Conditions** section.

SWITCHING WAVEFORMS

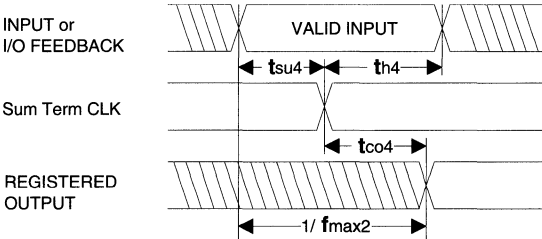
3



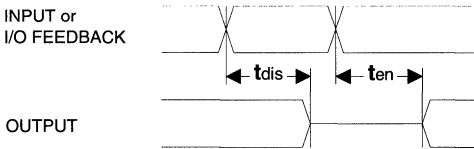
Combinatorial Output



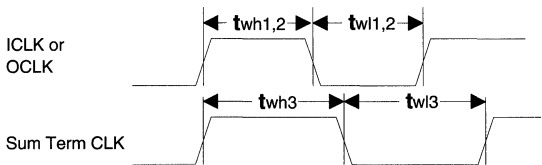
Latched Input



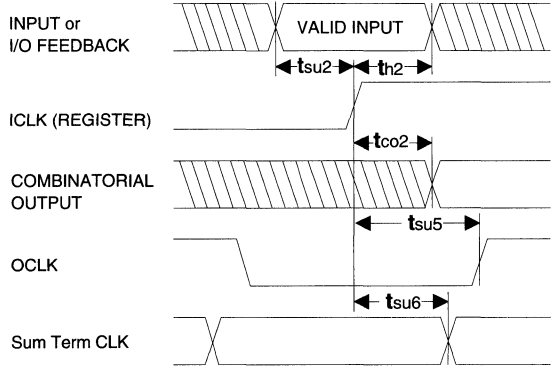
Registered Output (Sum Term CLK)



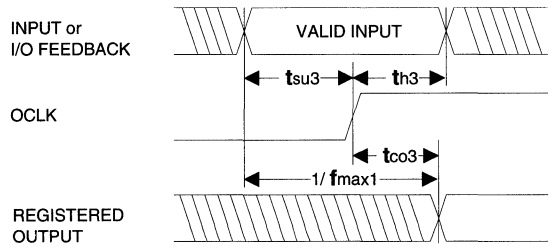
Input or I/O to Output Enable/Disable



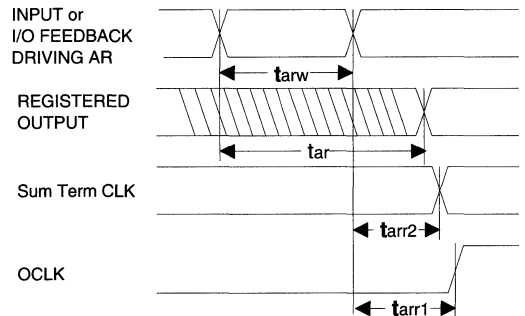
Clock Width



Registered Input

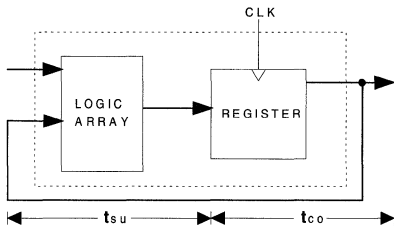


Registered Output (OCLK)



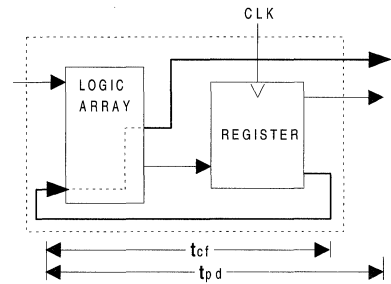
Asynchronous Reset

f_{max} DESCRIPTIONS



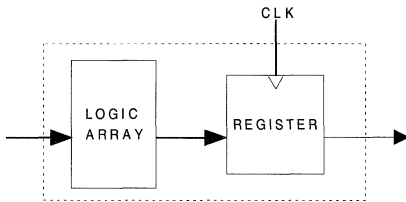
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

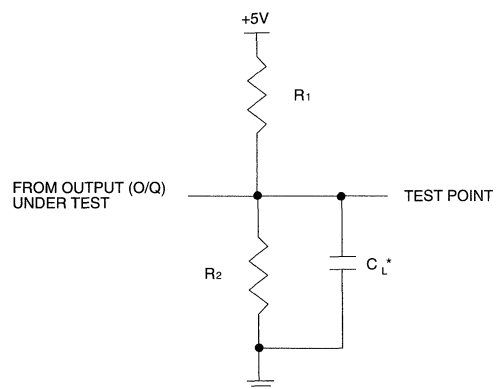
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	390Ω
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ARRAY DESCRIPTION

The GAL6002 contains two E² reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device I/O pins to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature is provided with every GAL6002 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6002 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because certain events may occur during system operation that cause the logic to be in an illegal state (power-up, line voltage glitches, brown-out, etc.). To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6002 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

3

LATCH-UP PROTECTION

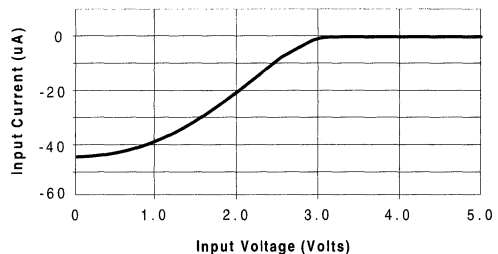
GAL6002 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

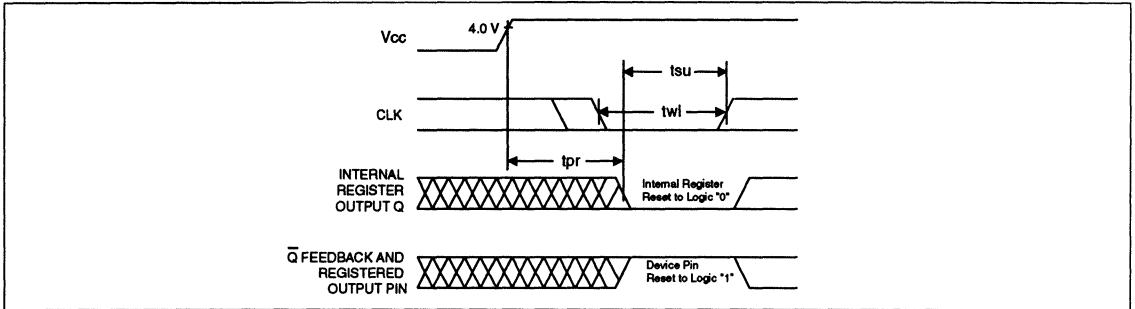
GAL6002 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL6002 input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce lcc for the device.

Typical Input Pull-up Characteristic



POWER-UP RESET



Circuitry within the GAL6002 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr} , 1 μ s MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature

of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6002. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = \left| (P\text{-Terms})_{LH} - (P\text{-Terms})_{HL} \right|$$

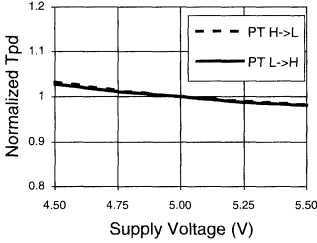
DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

The majority of designs fall below 15 DPTS, with the upper limit being approximately 25 DPTS. Lattice guarantees and tests the commercial grade GAL6002 for functionality at $DPTS \leq 30$.

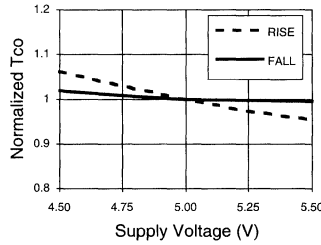
A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL6002 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering Dept. (Tel: 503-681-0118 or 1-800-FASTGAL; FAX: 681-3037).

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

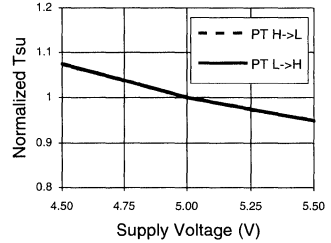
Normalized Tpd vs Vcc



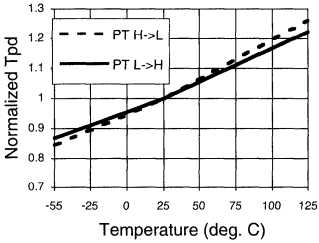
Normalized Tco vs Vcc



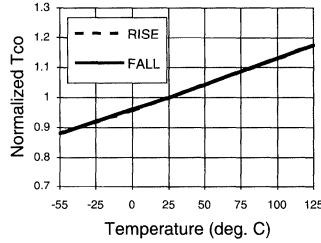
Normalized Tsu vs Vcc



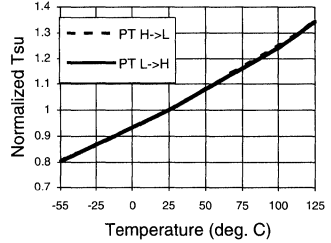
Normalized Tpd vs Temp



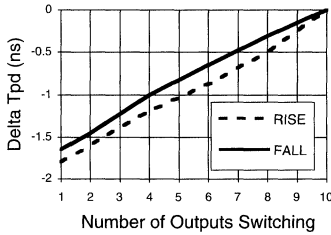
Normalized Tco vs Temp



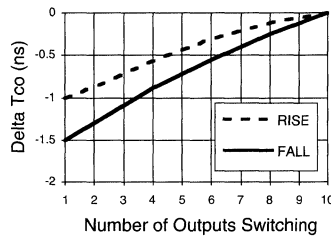
Normalized Tsu vs Temp



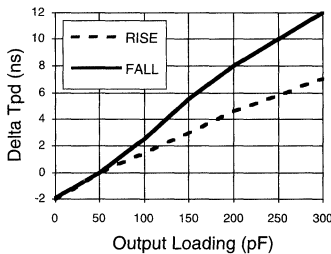
Delta Tpd vs # of Outputs Switching



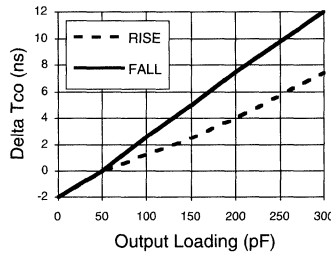
Delta Tco vs # of Outputs Switching

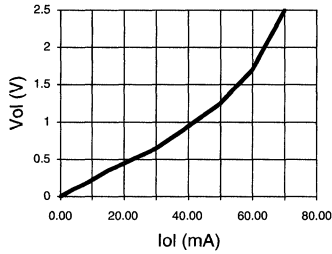
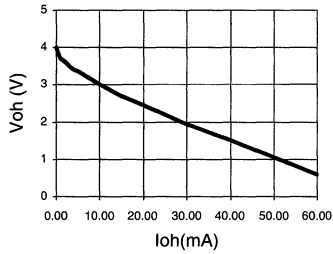
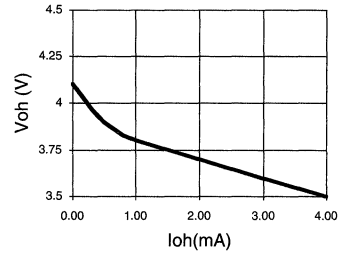
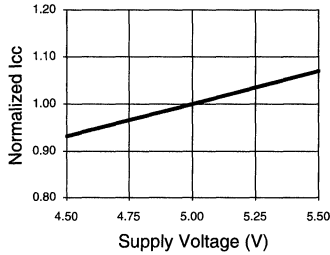
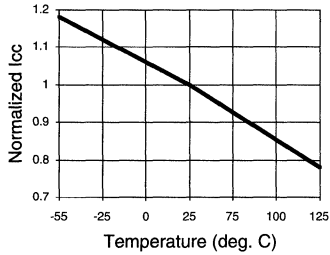
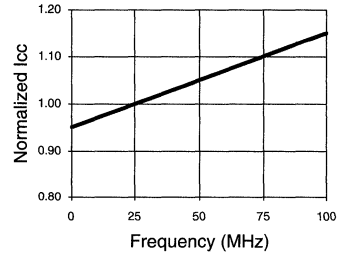
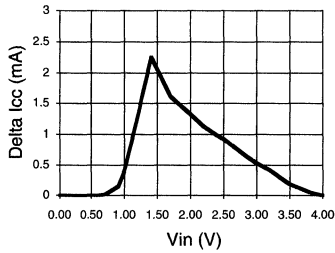
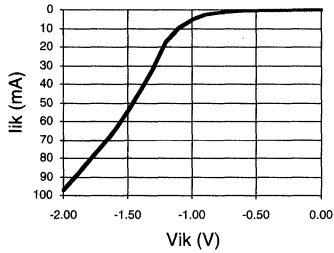


Delta Tpd vs Output Loading



Delta Tco vs Output Loading



TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS
Vol vs Iol

Voh vs Ioh

Voh vs Ioh

Normalized Icc vs Vcc

Normalized Icc vs Temp

Normalized Icc vs Freq.

Delta Icc vs Vin (1 input)

Input Clamp (Vik)


Section 1: Introduction

Section 2: High-Density Programmable Logic

Section 3: Low-Density Programmable Logic

Section 4: In-System Programmable Generic Digital Switch (ispGDS) Devices

Introduction to ispGDS	4-1
ispGDS22/18/14 Datasheet.....	4-5

Section 5: Military Program

Section 6: Development Tools

Section 7: Quality and Reliability

Section 8: General Information

Introduction to ispGDS™

Lattice, the pioneer of non-volatile in-system programmable (ISP™) logic has now expanded the application of ISP to include programmable system interconnect. The new ispGDS (Generic Digital Switch) family combines the in-system programmability, high performance and low power of Lattice's GAL programmable logic technology with a switch matrix architecture, resulting in an innovative programmable signal router. The ispGDS is a configurable switch matrix which provides the ability to quickly implement and change p.c. board connections without changing mechanical switches or other system hardware. ISP allows the connections to be reprogrammed without removal from the p. c. board via a simple 5V, 4 wire serial interface. This capability allows the system designer to define hardware which can be reconfigured in-system to meet a variety of applications. The ispGDS also conserves board real estate, providing up to 22 I/Os in about a quarter square inch of board space.

With today's demand for user-friendly systems, there is an increasing need for hardware which is easily reconfigured under software control without manual intervention. The Lattice ispGDS family is an ideal solution for end-system feature reconfiguration and signal routing applications. The fast 7.5ns propagation delay through the devices supports high-performance signal routing applications. Easier system upgrades, user feature selection and system manufacturing are the results.

The ispGDS also provides higher quality and reliability than other switch solutions due to the nature of E²CMOS technology. E²CMOS technology supports 100% testability which guarantees you 100% in-system programmability and functionality.

There are three members of the ispGDS family: the ispGDS22, ispGDS18, and ispGDS14. Each of the devices operate identically with the only difference being the number of I/O cells available.

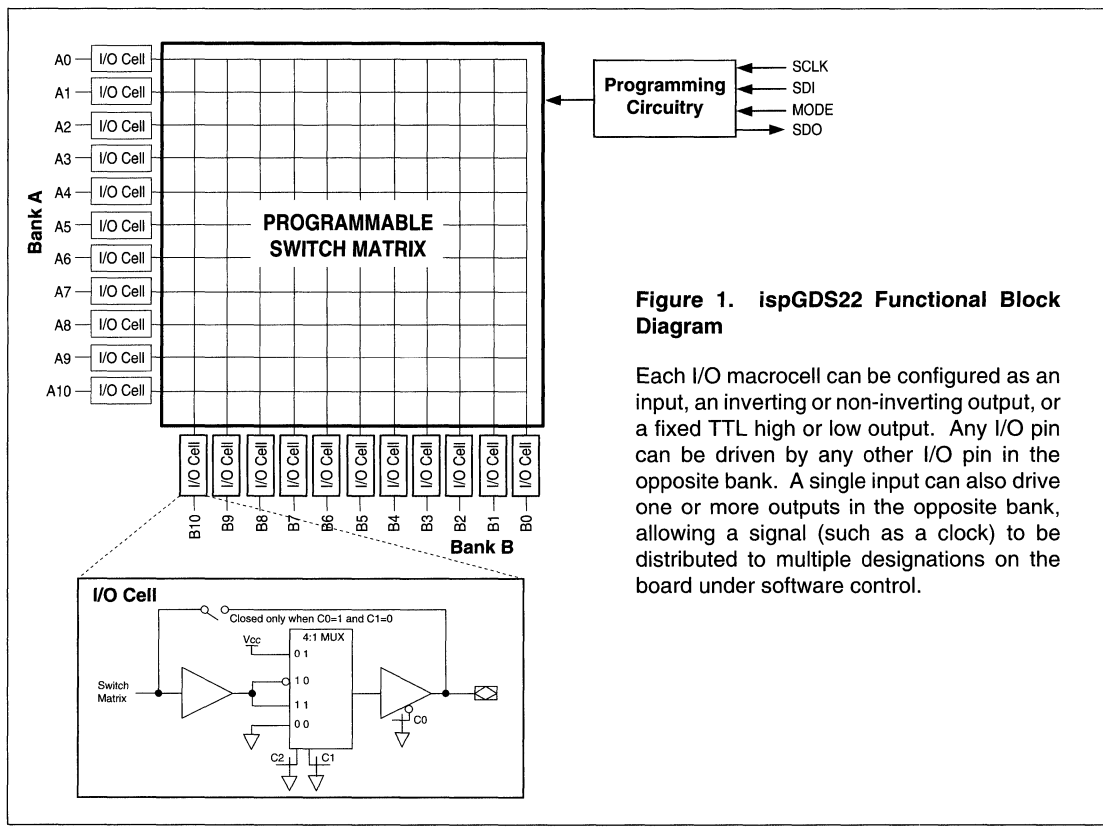


Figure 1. ispGDS22 Functional Block Diagram

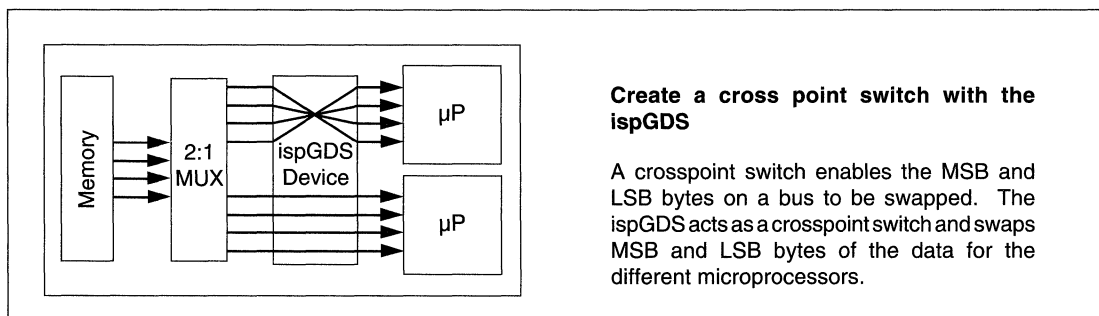
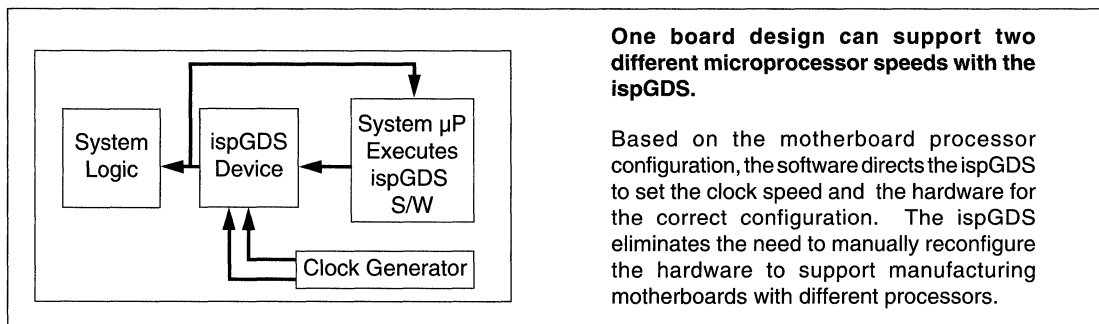
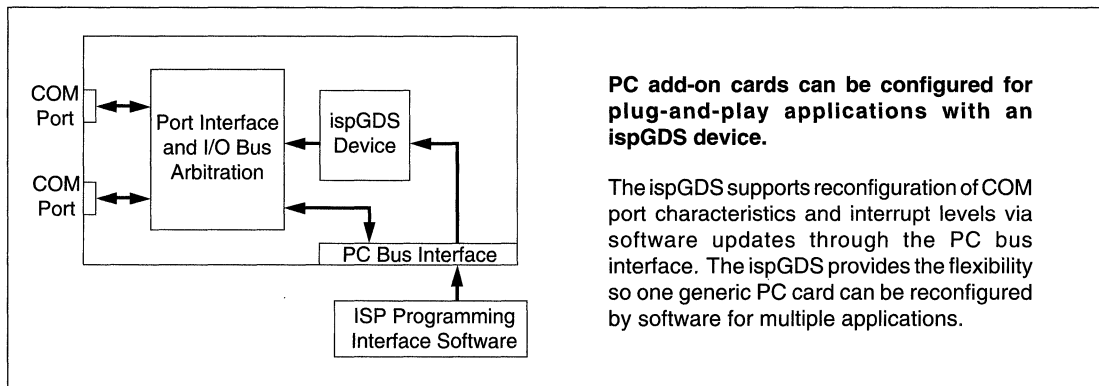
Each I/O macrocell can be configured as an input, an inverting or non-inverting output, or a fixed TTL high or low output. Any I/O pin can be driven by any other I/O pin in the opposite bank. A single input can also drive one or more outputs in the opposite bank, allowing a signal (such as a clock) to be distributed to multiple designations on the board under software control.

Introduction to ispGDS

ispGDS Applications

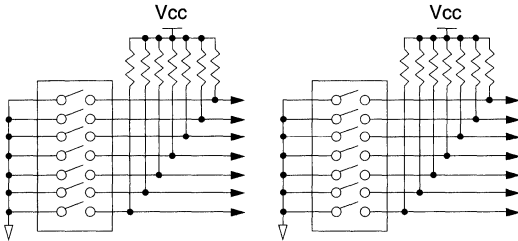
With the ispGDS, designs can be reconfigured without mechanical devices or user intervention. Provision for easier system upgrades and feature selection can now

be included in the system's original design. A few examples of actual ispGDS applications demonstrate the possibilities.



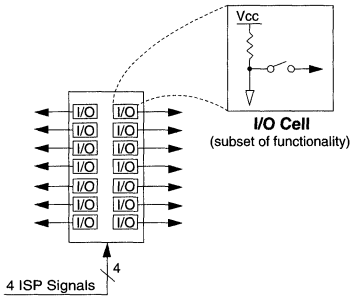
2 DIP Switches + 14 Resistors

14 pins which can be pulled high or low manually



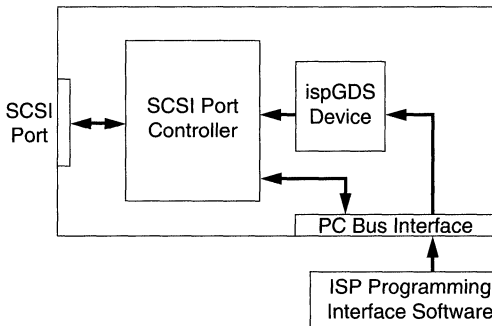
ispGDS14

14 pins which can be set high or low by SOFTWARE



Replace DIP switches with a software controlled switch alternative

The ispGDS can be configured as a programmable replacement for standard DIP switches, providing space savings, in-system reconfigurability, higher reliability as well as ease of use. The programmable nature of the ispGDS eliminates the need to manually select DIP switch settings.



SCSI port interface configurations can be set using the ispGDS

Software can reconfigure the ispGDS via the PC bus which in turn controls the SCSI port and interrupt level selection. Hardware changes become transparent to the user as the ispGDS is reconfigured by software while in-system eliminating the need for manual intervention.

Introduction to ispGDS

In-System Programming

The ispGDS devices can be programmed in-system using 5 volt only signals through a simple 4-wire programming interface using TTL level signals. Programming and erasure of the entire device can be done in less than one second.

In addition to third party programmers, the ispGDS can be programmed from your automatic test equipment (ATE) or even from a PC on your manufacturing line. For more flexibility, you can have your product's embedded microprocessor configure the ispGDS devices through one of its I/O ports, making a field upgrade a snap.

Lattice provides free compiler support and "ISP Download Software" to support the software side of these programming options. The ispGDS Download routines are written in ANSI-standard C language which can be integrated directly into your system.

Designing with the ispGDS will provide you with the flexibility to reconfigure your design while in-system. It will revolutionize the way systems are designed and maintained. Call 1-800-327-8425 for a data sheet and begin designing today!

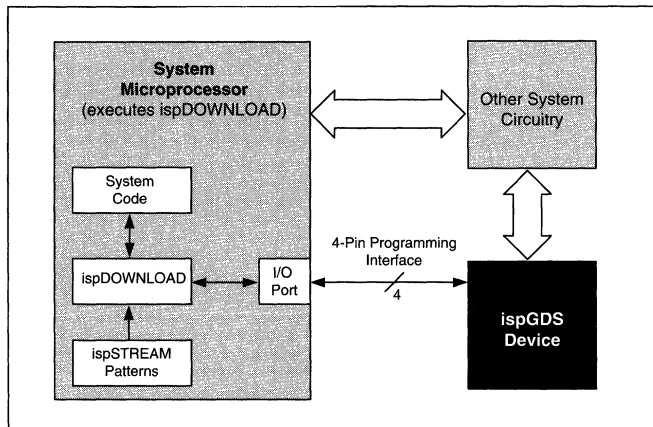


Figure 2. In-System Programming Using ispGDS Download Routines

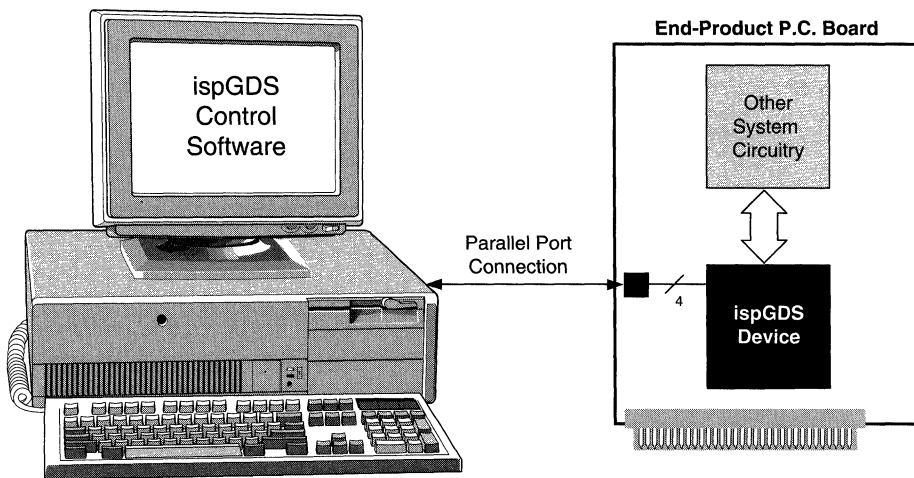
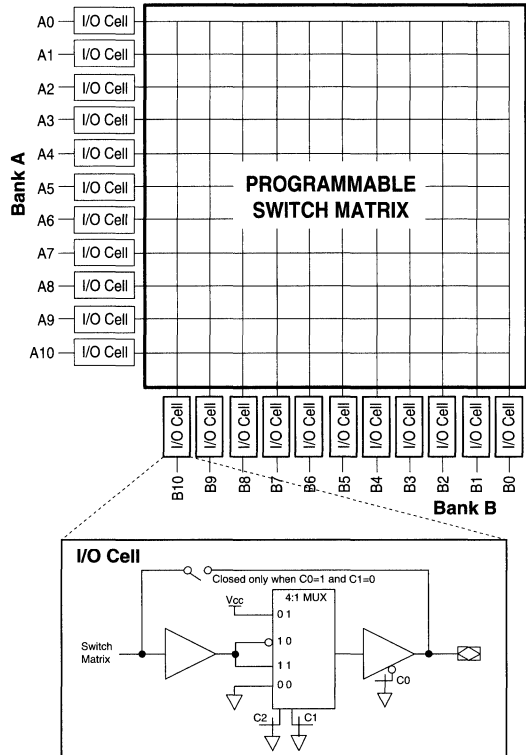


Figure 3. Configuring an ispGDS Device from a Remote System

FEATURES

- **HIGH-SPEED SWITCH MATRIX**
 - 7.5 ns Maximum Propagation Delay
 - Typical $I_{cc} = 25$ mA
 - UltraMOS® Advanced CMOS Technology
- **FLEXIBLE I/O MACROCELL**
 - Any I/O Pin Can be Input, Output, or Fixed TTL High or Low
 - Programmable Output Polarity
 - Multiple Outputs Can be Driven by One Input
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
 - Programming Time of Less Than One Second
 - 4-Wire Programming Interface
 - Minimum 10,000 Program/Erase Cycles
- **E² CELL TECHNOLOGY**
 - Non-Volatile Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **APPLICATIONS INCLUDE:**
 - Software-Driven Hardware Configuration
 - Multiple DIP Switch Replacement
 - Software Configuration of Add-In Boards
 - Configurable Addressing of I/O Boards
 - Multiple Clock Source Selection
 - Cross-Matrix Switch
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM (ispGDS22)



4

DESCRIPTION

The Lattice ispGDS™ family is an ideal solution for reconfiguring system signal routing or replacing DIP switches used for feature selection. With today's demands for customer ease of use, there is a need for hardware which is easily reconfigured electronically without dismantling the system. The ispGDS devices address this challenge by replacing conventional switches with a software configurable solution. Since each I/O pin can be set to an independent logic level, the ispGDS devices can replace most DIP switch functions with about half the pin count, and without the need for additional pull-up resistors. In addition to DIP switch replacement, the ispGDS devices are useful as signal routing cross-matrix switches. This is the only non-volatile device on the market which can provide this flexibility.

With a maximum tpd of 7.5ns, and a typical active I_{cc} of only 25 mA, these devices provide maximum performance at very low power levels. The ispGDS devices may be programmed in-system, using 5 volt only signals, through a simple 4-wire programming interface. The ispGDS devices are manufactured

using Lattice's advanced non-volatile E²CMOS process which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

Each I/O macrocell can be configured as an input, an inverting or non-inverting output, or a fixed TTL high or low output. Any I/O pin can be driven by any other I/O pin in the opposite bank. A single input can drive one or more outputs in the opposite bank, allowing a signal (such as a clock) to be distributed to multiple destinations on the board, under software control. The I/Os accept and drive TTL voltage levels.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all LATTICE products. LATTICE also guarantees 10,000 erase/rewrite cycles and data retention in excess of 20 years.

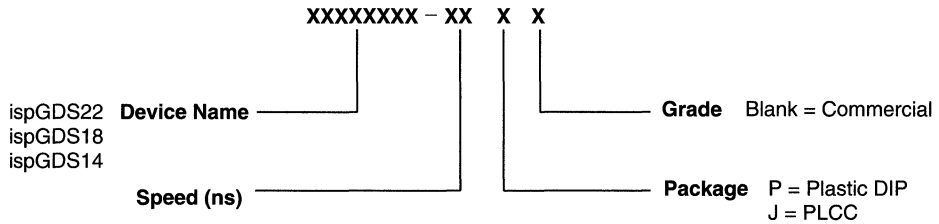
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ispGDS ORDERING INFORMATION

Commercial Grade Specifications

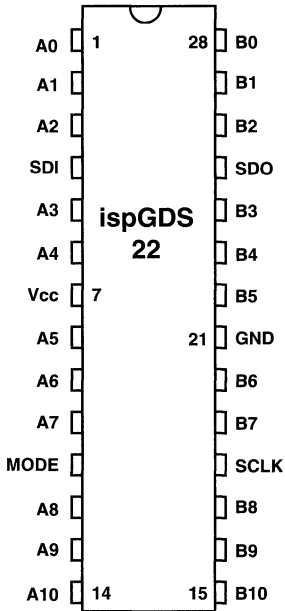
Matrix Size	I/O Pins	Tpd (ns)	Isb (mA)	Icc (mA)	Ordering #	Package
11 x 11	22	7.5	25	40	ispGDS22-7P	28-Pin Plastic DIP
					ispGDS22-7J	28-Lead PLCC
9 x 9	18	7.5	25	40	ispGDS18-7P	24-Pin Plastic DIP
7 x 7	14	7.5	25	40	ispGDS14-7P	20-Pin Plastic DIP
					ispGDS14-7J	20-Lead PLCC

PART NUMBER DESCRIPTION

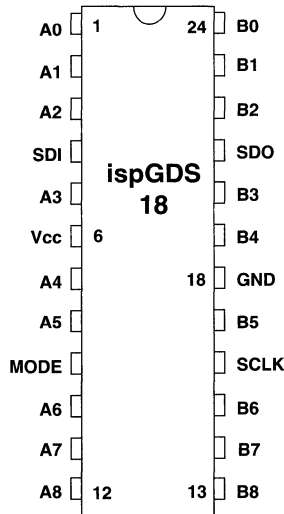


PACKAGE DIAGRAMS

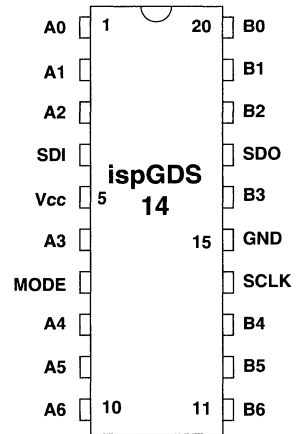
28-Pin DIP



24-Pin DIP

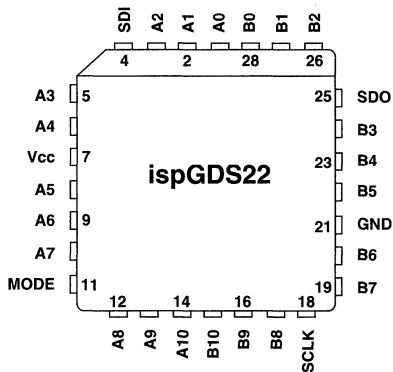


20-Pin DIP

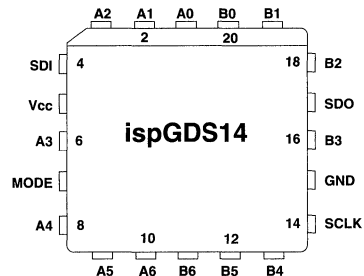


4

28-Pin PLCC



20-Pin PLCC



ispGDS FAMILY OVERVIEW

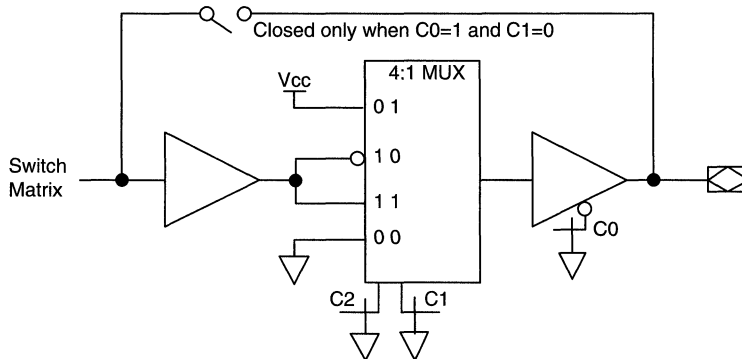
There are three members of the ispGDS family, the ispGDS22, ispGDS18, and ispGSD14. The numerical portion of the part name indicates the number of I/O cells available. All of the devices are available in a DIP package, with the ispGDS22 and ispGDS14 also available in a PLCC package. Each of the devices operate identically, with the only difference being the number of I/O cells available.

The ispGDS devices are all programmed through a four-pin interface, using TTL level signals. The four dedicated programming pins are named MODE, SDI, SDO, and SCLK. No high-voltage is needed, as the voltages needed for programming are generated internally. Programming of the entire device, including erasure, can be done in less than one second. During the programming operation, all I/O pins will be tri-stated. Further

details of the programming process can be found in the In-System Programming section later in this datasheet.

The I/O cells in each device are divided equally into two banks (Bank A and Bank B). Each I/O cell can be configured as an input, an inverting output, a non-inverting output, or set to a fixed TTL high or low. A switch matrix connects the I/O banks, allowing an I/O cell in one bank to be connected to any of the I/O cells in the other bank. A single I/O cell configured as an input can drive one or more I/O cells in the other bank. The full I/O macrocell, which is identical for each of the I/O pins, is shown below. The allowable configurations are shown on the following page.

I/O MACROCELL



DEVICE PROGRAMMING

The ispGDS family of devices uses a standard JEDEC file, as used for programmable logic devices, to describe device programming information. Popular logic compilers, such as ABEL and CUPL, can produce the JEDEC files for these devices.

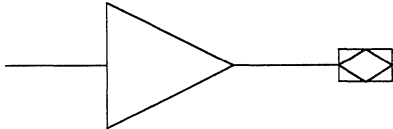
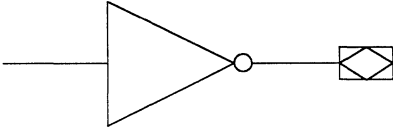
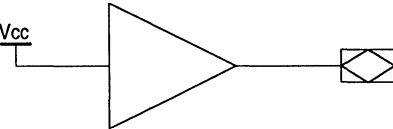
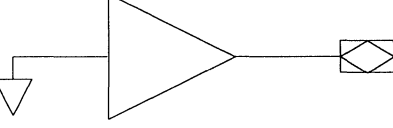
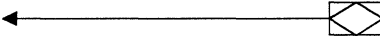
The JEDEC files can be used to program the ispGDS devices in a number of ways, which are shown in the In-System Programming Overview section later in this datasheet.

ELECTRONIC SIGNATURE

An electronic signature word is provided with every ispGDS device. It contains 32 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the fuse checksum in the JEDEC fusemap.

I/O MACROCELL CONFIGURATIONS

From Switch Matrix		<p>Configuration for Active High Output</p> <ul style="list-style-type: none"> - C0 = 0. - C1 = 1. - C2 = 1.
From Switch Matrix		<p>Configuration for Active Low Output</p> <ul style="list-style-type: none"> - C0 = 0. - C1 = 0. - C2 = 1.
Vcc		<p>Configuration for Fixed TTL High Output</p> <ul style="list-style-type: none"> - C0 = 0. - C1 = 1. - C2 = 0.
↓		<p>Configuration for Fixed TTL Low Output</p> <ul style="list-style-type: none"> - C0 = 0. - C1 = 0. - C2 = 0.
To Switch Matrix		<p>Configuration for Dedicated Input</p> <ul style="list-style-type: none"> - C0 = 1. - C1 = 0. - C2 = 1.

Note 1: The development software configures all of the architecture control bits and checks for proper pin usage automatically.
 Note 2: The default configuration for unused pins is for all configuration bits set to one, which produces a tri-stated output.

IN-SYSTEM PROGRAMMING OVERVIEW

The ispGDS family of devices can be programmed in a number of ways. Two options are to build a custom cable to program devices on your board directly from the parallel port of a PC, or to build the programming capability right into your system. To support the software side of either of these solutions, Lattice provides ispGDS Download programming routines. These routines are written in ANSI-standard C language, which can be used either to serve as detailed examples or to be integrated directly into your system. These routines include such common operations as Program, Read, and Verify. The routines are structured so that any hardware-dependent code is contained in a few well-documented functions, which can be easily modified for virtually any system. Example programs are included which use the parallel printer port of an IBM PC or compatible.

In addition, popular third-party programmers provide the ability to program the devices in a socket, just like conventionally programmed devices. This is especially useful for engineering debug of programming circuitry you build into your own system.

Many of the best uses for the ispGDS devices are to use them to reconfigure a system in the field. In any system that uses a microprocessor, the microprocessor can often be used to program the ispGDS devices right in the system. The Lattice ispGDS Download software routines can be used to easily integrate ispGDS programming capability into your system software, or allow you to quickly create a custom program for configuring the system. A typical system is shown below in Figure 1. Note that the pattern information is normally stored in the Lattice ispSTREAM™ format, which is a bit-packed format providing device pattern storage in less than 1/8 that of a standard JEDEC file. The pattern information may reside either on-board in an EPROM or EEPROM, or be loaded from an external source such as a disk or across a network.

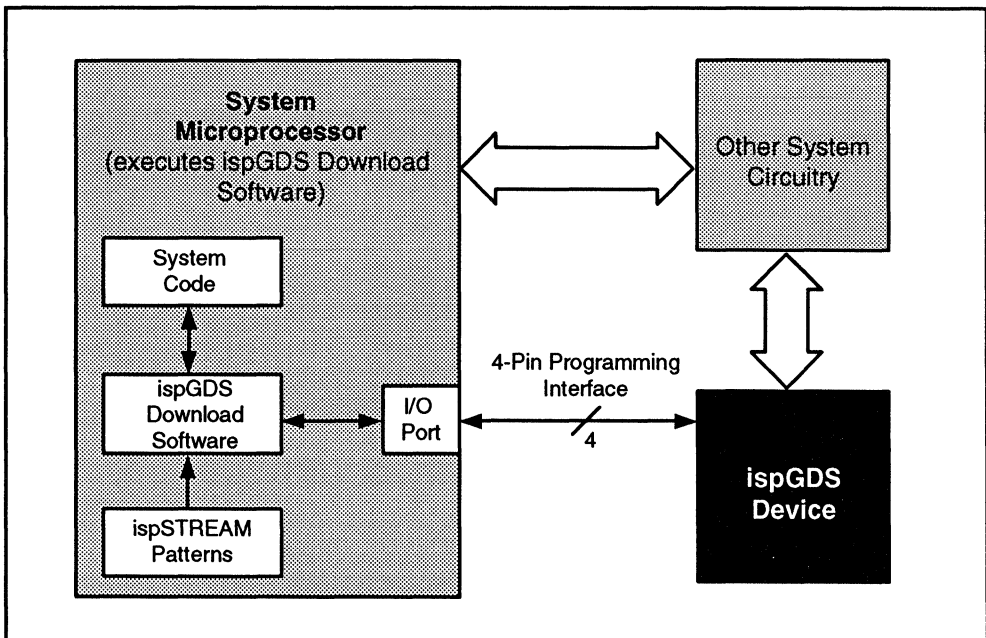


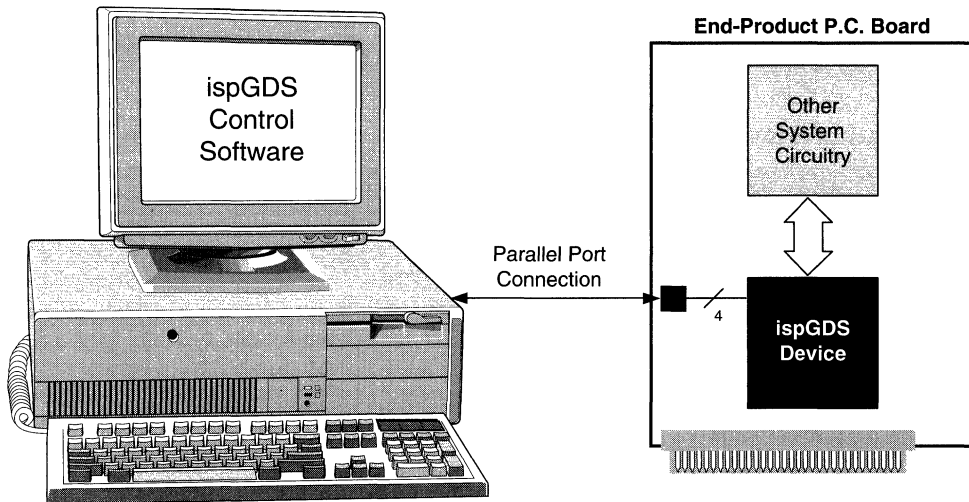
Figure 1 — In-System Programming Using ispGDS Download Software

IN-SYSTEM PROGRAMMING OVERVIEW

Another possibility is to use an external system, such as a portable PC, to change the configuration of a board by reprogramming an on-board ispGDS device (see figure 2 below). This can be useful for field service personnel to re-configure a board for testing or to enable optional features. The same method can be used during the design, test or manufacturing phase, before the board is put into a working system capable of reprogramming the devices.

Lattice provides a standalone utility program that uses the PC parallel port to program ispGDS devices through a cable. Also, the ispGDS Download software can be used to easily create custom programs for programming the ispGDS devices through your own interface. Example programs using the PC parallel port are included in the ispGDS Download software.

If you have any questions about programming the ispGDS devices, please contact Lattice Application Engineering at 800-327-8425 or 503-693-0201.



4

Figure 2 — Configuring the ispGDS from a Remote System

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC}	-5 to +7V
Input voltage applied	-2.5 to $V_{CC} + 1.0V$
Off-state output voltage applied	-2.5 to $V_{CC} + 1.0V$
Storage Temperature	-65 to 150°C
Ambient Temperature with Power Applied	-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:	
Ambient Temperature (T_A)	0 to 75°C
Supply voltage (V_{CC}) with Respect to Ground	+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}¹	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

I_{SB}	Standby Power Supply Current	Inputs = 0V Outputs open	L-7	—	15	25	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L-7	—	25	40	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
$C_{I/O}$	I/O Capacitance (as input or output)	8	pF	$V_{CC} = 5.0V, V_I = 2.0V$

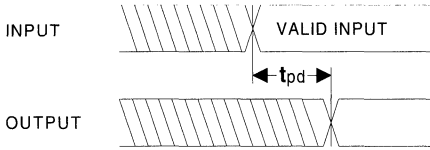
*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

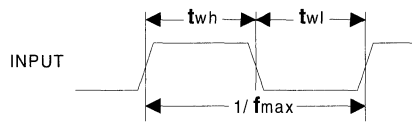
Over Recommended Operating Conditions

PARAMETER	TEST COND.	DESCRIPTION	COM		UNITS
			MIN.	MAX.	
t_{pd}	A	Input to Output Delay	One Input Driving One Output		ns
f_{max}	A	Maximum Input Frequency	One Output Switching		MHz
t_{wh}	A	Input Pulse Duration, High	10	—	ns
t_{wl}	A	Input Pulse Duration, Low	10	—	ns

SWITCHING WAVEFORMS



Input to Output Delay



Input Pulse Width/ Fmax

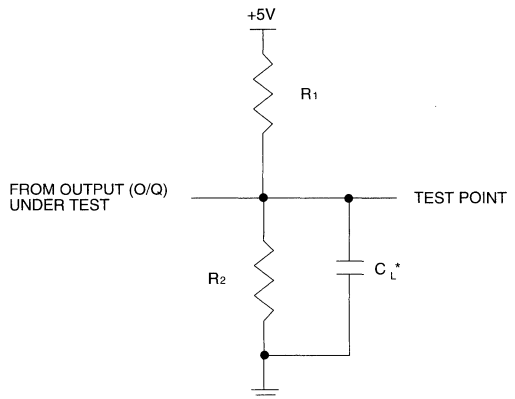
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	470Ω	390Ω	50pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

IN-SYSTEM PROGRAMMING

Each device in the ispGDS family uses the same programming algorithm and programming parameters. The devices generate their own internal supervoltage for programming, and only require standard TTL signals to program. Programming the ispGDS devices is centered around a 3-state state machine, with its state transitions controlled by two control signals. One of the states is the normal operation state, with the other two states controlling the programming process. The ISP programming state machine is controlled by four dedicated programming pins on each device, which are described below. During normal device operation the SDI, MODE and SCLK pins should be tied low.

SERIAL PROGRAMMING INTERFACE

The ispGDS devices are programmed using the four dedicated programming interface pins: SDI, MODE, SDO and SCLK.

Serial Data In (SDI) performs two different functions. First as the input to the serial shift register, and second as one of the two control pins for the programming state machine. Because of this dual role, the function of SDI is controlled by the MODE pin. When MODE is low, SDI is the serial input to the shift registers and when MODE is high, SDI becomes a control signal. Internal to the device, the SDI is multiplexed to various shift registers in the device. The different shift instructions of the state machine determine which of these shift registers gets the input from SDI.

The MODE signal, combined with the SDI signal, controls the programming state machine, as described in this section.

Serial Clock (SCLK) is the serial shift register clock used to clock the internal serial shift registers and to clock the state machine between states. State changes and shifting data in is done on

a low-to-high transition. When shifting data out, the data is available on SDO only after a subsequent high-to-low transition. When MODE is high, SCLK controls the programming state machine, and when MODE is low, SCLK acts as a shift register clock to shift data in or out or to start an operation.

Serial Data Out (SDO) is the output of the serial shift registers. The selection of shift register is again determined by the state machine's shift instruction. When MODE is driven high, SDO connects directly to the SDI, bypassing the device's shift registers.

PROGRAMMING STATE MACHINE OPERATION

The programming state machine controls which mode the device is in, and provides the means to read and write data to the device (see figure 3). The four dedicated control pins are used to load and unload data, and to control the state machine. The state machine is a 2 bit state machine, with three defined states: IDLE (00), SHIFT (01) and EXECUTE (10). Instruction codes are shifted into the device in the SHIFT state, and control which instruction is to be executed in the EXECUTE state. In the SHIFT and EXECUTE states all the I/O pins are tri-stated. To transition between states MODE is held high, SDI is set to the appropriate level, and SCLK is clocked.

The IDLE state is the default state of the state machine. In this state the device is in normal operation, and programming operations are disabled. Each device contains a hardwired eight bit ID code, which can be read from this state. The IDLE state may be reached from any other state by setting MODE high, SDI low, and clocking SCLK.

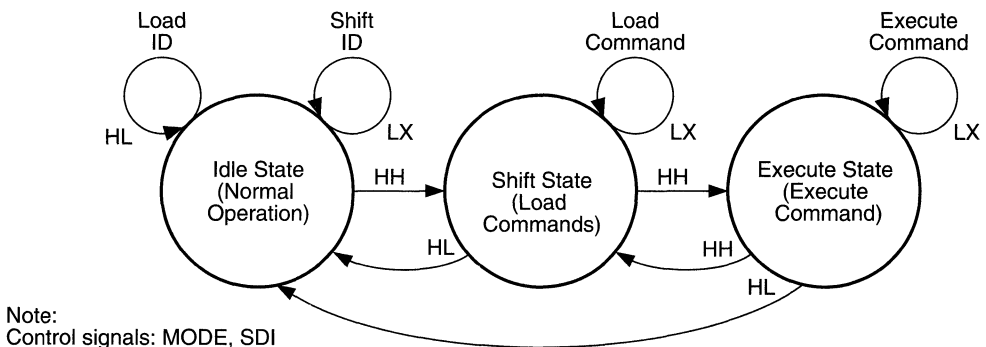


Figure 3. Programming State Machine

The SHIFT state provides the means to load an instruction into the state machine. A five bit instruction is loaded into the state machine by holding MODE low and clocking in the instruction, via SDI. The entire Instruction Set is shown below in Table 1. Once an instruction is loaded into the state machine, it may be executed in the EXECUTE state. The SHIFT state is reached from either of the other two states by setting MODE and SDI high, and clocking SCLK.

The EXECUTE state is where the instruction that was shifted in during the SHIFT state is actually executed. An individual instruction execution is started by taking MODE low and clocking SCLK.

Instruction	Operation	Description
00000	NOP	No operation performed.
00010	SHIFT_DATA	Clocks data into, or out of, the Data Shift Register.
00011	BULK_ERASE	Erases the entire device.
00101	ERASE_ARRAY	Erases everything except the Architecture rows.
00110	ERASE_ARCH	Erases the Architecture rows only
00111	PROGRAM	Programs the Shift Register data into the addressed row
01010	VERIFY	Load data from the selected row into the Serial Shift Register.
01110	FLOWTHRU	Disables the Shift Register (SDI=SDO).

Table 1. Instruction Codes

SHIFT REGISTERS

The ispGDS devices have three shift registers, the Device ID shift register, the Instruction shift register and the Data shift register. All shift registers operate on a First In First Out (FIFO) basis, and are chosen by which state the programming state machine is in.

The Device ID shift register is only accessible in the IDLE state. It is eight bits long, and is only used to shift out the device ID. The Instruction shift register is only accessible in the SHIFT state. It is five bits long, and is only used to shift the Instruction Codes

into the device. The Device ID and Instruction shift registers expect the LSB shifted in first. The Data shift register is 24 bits long, and is used to shift all addresses and data into or out of the device. The Data shift register is only accessible in the EXECUTE state when executing a SHIFT_DATA instruction.

To program an ispGDS device, data is read from a serial bit stream and shifted into the shift registers. Twenty four bits are read at a time, shifted into the device, and then a programming operation is performed. The exact sequence, and the methods for converting a JEDEC map into a serial bit stream is explained in the Device Architecture section.

TIMING

Programming the ispGDS devices properly requires that a number of timing specifications be met. Most critical are the specifications relating to programming and erasing the E²CMOS cells. In addition to a minimum pulse width, there is also a maximum specification for these parameters. Table 2 lists the programming mode specifications for the ispGDS family of devices. Diagrams for the programming mode specifications are shown in Figures 4, 5, and 6 on the following page.

INTERNAL ARCHITECTURE

This section explains the internal architecture of the device as it relates to programming. This section is not strictly necessary to the programming of the device if you are using the Lattice software tools provided.

The key to easy programming of the ispGDS device is the use of a bit-stream of all the data that needs to be shifted into a device to program it. Lattice calls this bit-stream format an ispStream format. The ispStream format uses one bit to represent the state of each of the programmable cells, instead of the byte value used in a JEDEC file. Considering the additional characters in a JEDEC file, this means a space savings of more than a factor of eight. In addition, the ispStream does not require any parsing. The bits are simply read from the file and shifted into the device. Since only 49 bytes are required to store the pattern for an ispGDS device, many different patterns can be stored in a small space.

This section mainly concerns the details of constructing the ispStream format. If you are using the supplied software tools, a conversion utility (complete with source code) is included to convert an industry-standard JEDEC file to an ispStream format. All of the Lattice software routines read from and write to this ispStream format.

The ispGDS devices have two basic sections to their programming architecture (see figure 7). There are three rows of architecture information, which contain the three bits that control the function of each I/O cell. The rows are 24 bits long; one bit for each I/O cell. (the ispGDS18 and ispGDS14 do not use all the bits) The other major area contains the cell data for the switch

Table 1. Programming Mode Timing Specifications

Param.	Description	Min.	Max.	Unit
t_{rst}	Time from power-up of device to any programming operation.	1	—	μ s
t_{isp}	Time from leaving IDLE state to I/O pins tri-state, or entering IDLE state to I/O pins active.	—	10	μ s
t_{su}	Setup time, from either MODE or SDI to rising edge of SCLK.	100	—	ns
t_h	Hold time, from rising edge of SCLK to MODE or SDI changing level.	100	—	ns
t_{co}	Time from falling edge of SCLK to data out on SDO.	—	150	ns
t_{clkh}	Clock pulse width of SCLK while high.	0.5	—	μ s
t_{clkl}	Clock pulse width of SCLK while low.	0.5	—	μ s
t_{pwp}	Time for a programming operation.	40	100	ms
t_{pwe}	Time for an erase operation.	200	—	ms
t_{pwv}	Time for a verify operation.	5	—	μ s

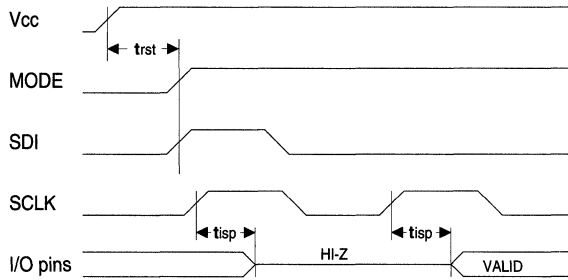


Figure 4. Programming Mode Timing

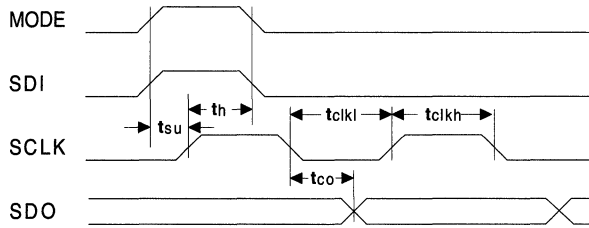


Figure 5. Shift Register Timing

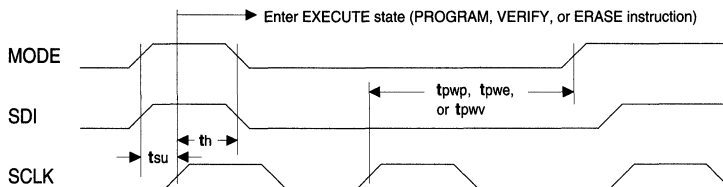


Figure 6. Program, Verify, & Erase Timing

matrix area of the device, and the User Electronic Signature (UES) data area. There are two UES rows of 24 bits each, and 11 switch matrix rows of 24 bits each.

Even though the shift register lengths are 24 bits long, all of the area is not a data area. In the Architecture section, two bits are used for addressing. In the matrix/UES area, there are six bits for addressing. In the switch matrix area, there are only 11 bits of actual data, and 7 dummy bits to make all the shift registers the same length. These 5 bits will always read as a one, or a logic High on SDO. For the UES, there are 16 bits of actual data in each row, and two dummy bits.

STREAM FORMAT

To convert the information in a standard JEDEC file into the ispStream format, all of the addressing information is added, as well as the place-holding bits (dummy bits). The objective is to

have every bit that is shifted into the device for programming included in the ispStream format. For the three architecture rows, this means simply adding the two bits for the addresses. For the UES and Switch Matrix rows, there are 8 bits to add. The first two bits are always 00 to distinguish this area from the Architecture row. Then there are 4 bits to address the specific row, and 2 bits as placeholders. In the Switch Matrix rows, there are also 5 bits for place-holding at the end of the rows. The various placeholder bits are built into the device so that all rows appear to be the same length, thus simplifying the programming operations.

The ispStream uses one bit for each programmable cell. This means that each row will take 24 bits, or 3 bytes of storage. With 3 bytes per row, and 16 rows per device, the ispStream would then take only 48 bytes of storage area. However, there is one extra byte used at the front of the file to store the device ID code,

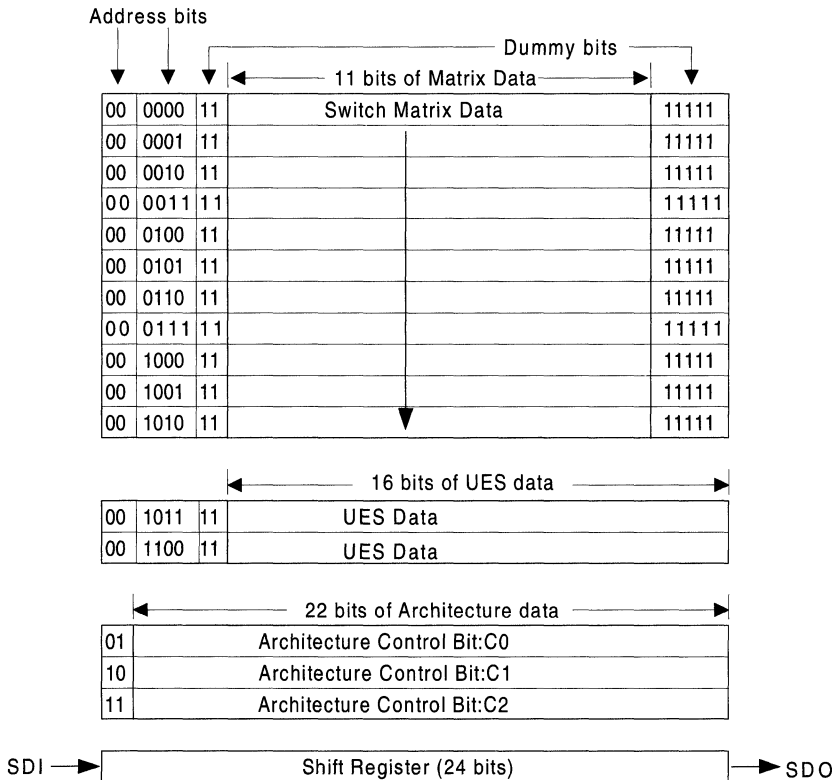


Figure 7. ispGDS Architecture

and a 32-bit checksum. This ID code is the same as the one hardwired into the device. The purpose of including this ID code is to be sure the ispStream type is the same as the device is to be programmed into. All ispStream formats, regardless of which Lattice In-System Programmable device they are for, will contain this ID code as the first byte. By reading this ID code, you can tell which device the ispStream is for. If the ispStreams are stored in EPROM for instance, they will be stacked end to end, and the ID code will help to determine not only which device type it belongs with, but how long it is, and thus where the next pattern starts. See Figure 8 for details of the ispStream format, and Figure 9 for the JEDEC map.

ALGORITHMS

The programming of the ispGDS devices will be described as a hierarchical set of algorithms and functions. This section contains the high level algorithms for erasing, programming, verifying and loading an ispGDS device. A universal set of functions is used to make up all the algorithms, and enable each of them to be written in a modular format. The individual functions are explained in the next section. Note that most procedures leave the device in the SHIFT state. These algorithms and functions closely follow the ispCODE source code library that Lattice provides.

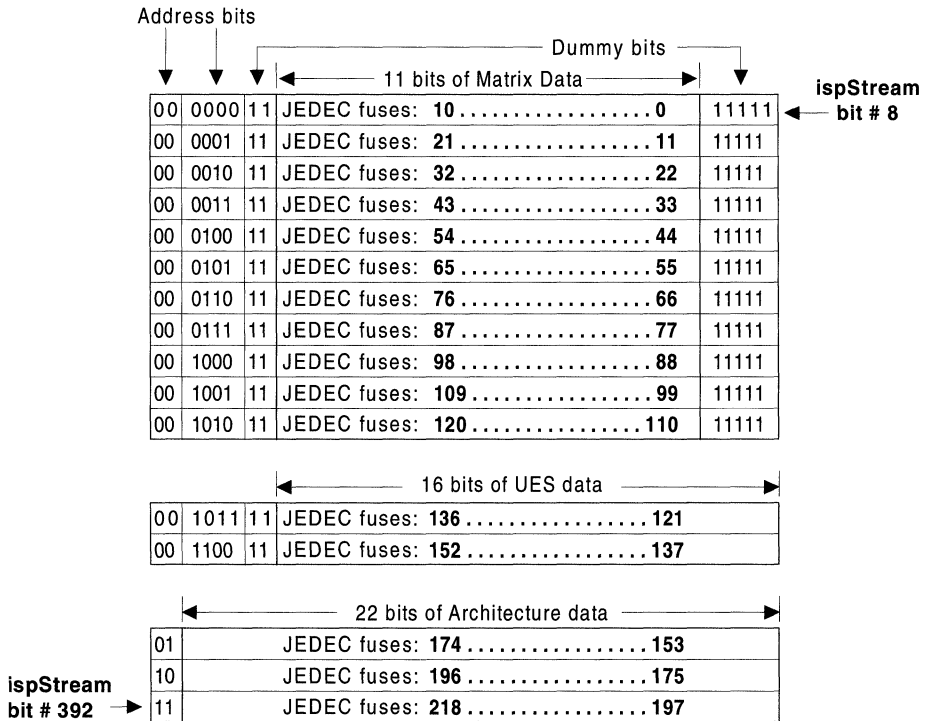
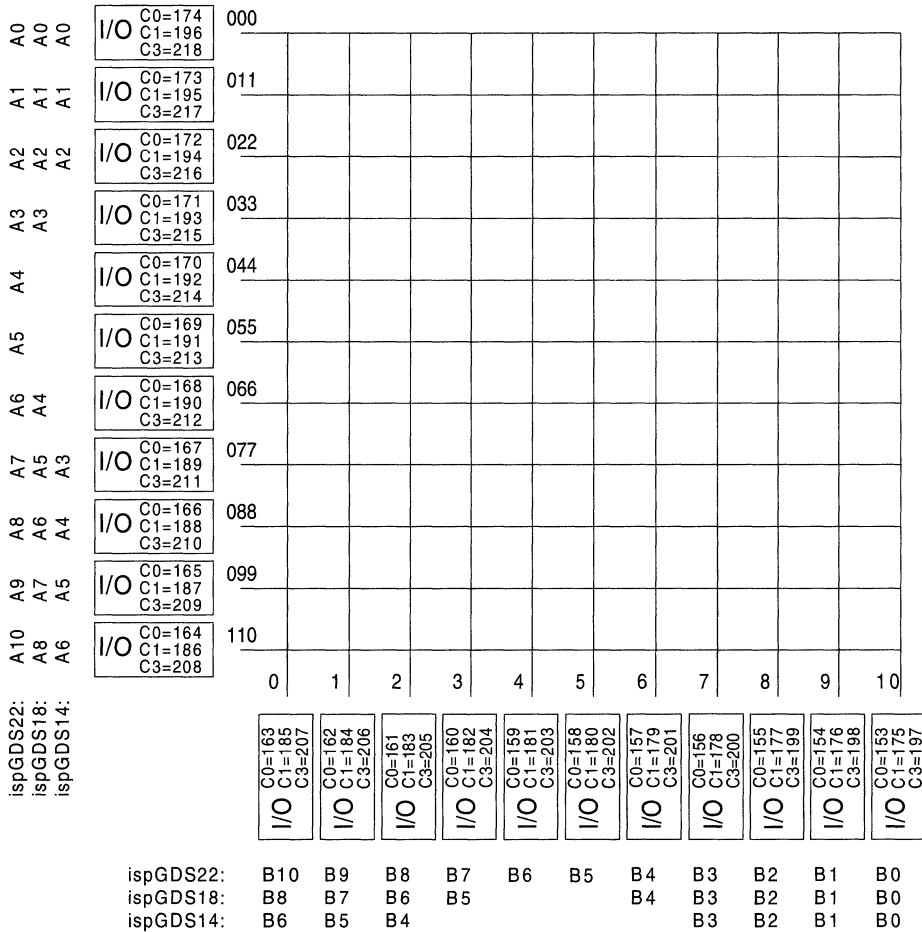


Figure 8. ispStream Format



User Electronic Signature

121, 122 151, 152			
Byte 3	Byte 2	Byte 1	Byte 0

M L
S S
B B

Figure 9. ispGDS JEDEC Fuse Map

To simplify the algorithms, all operations use an ispStream format as the data structure from which to read from and write to. The ispStream contains all the address information, and simplifies all the operations considerably. Working from the ispStream, the device appears as an array of 16 rows by 24 bits long.

Program Algorithm

Before programming a device, it must first be erased. Cells can be programmed (set to a JEDEC zero) using the programming command, but only an Erase procedure erase a cell (set a cell back to a JEDEC one). In this algorithm, the entire device is erased (Bulk Erased), and then the entire device is programmed.

To program a device:

- Call procedure: Get_ID (to check device type)
- Call procedure: Change_State (from IDLE to SHIFT state)
- (Erase entire device)
 - Call procedure: Shift_Command, with command: ERASE
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Execute_Command (starts operation)
 - Call procedure: Wait (Erase_Time)
 - Call procedure: Change_State (to SHIFT state)
- Set row_count =0
- Loop until row_count = 15
- (Program one row on each loop)
 - Call procedure: Shift_Command, with command: SHIFT_DATA
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Shift_Data_In, with data location in ispStream at (row_count x 24)
 - Call procedure: Change_State (to SHIFT state)
 - Call procedure: Shift_Command, with command: PROGRAM
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Execute_Command (starts operation)
 - Call procedure: Wait (Program_Time)
 - Call procedure: Change_State (to SHIFT state)
- End Loop

Load Algorithm

The load algorithm below is the same for all ispGDS devices. First the 13 rows of array data (11 rows for the array matrix, and 2 for the UES) is read, and then the 3 rows of Architecture information is read. After each row is read, it is stored in an ispStream format.

In order to load each row's data into the shift register, it is necessary to load the address of the row into the appropriate area of the shift register. Because of the unique way the different areas of the device are addressed, the simplest way to get the addresses into the device in the proper order is to use an existing ispStream to supply those addresses. In other words, the full data for each row is loaded from the ispStream into the device. When a VERIFY command is executed, the device's data for that same row is then loaded into the shift register to be shifted out. This method will be used in this algorithm.

When using an existing ispStream to supply the addresses, the data should not be the same as the expected data, or a failure to verify may not be detected. To cover this possibility, a pattern that contains all ones for data can be used (and is supplied with the software tools provided by Lattice). This ispStream still has the addresses intact, but all programmable cell data is set to a one (erased state).

To load a device:

- Call procedure: Get_ID (to check device)
- Call procedure: Change_State (from IDLE to SHIFT state)
- Set row_count =0
- Loop until row_count = 15
 - Call procedure: Shift_Command, with command: SHIFT_DATA
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Shift_Data_In, with data location in Source ispStream at (row_count x 24)
 - Call procedure: Change_State (to SHIFT state)
 - Call procedure: Shift_Command, with command: VERIFY
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Execute_Command (starts operation)
 - Call procedure: Wait (Verify_Time)
 - Call procedure: Change_State (to SHIFT state)
 - Call procedure: Shift_Command, with command: SHIFT_DATA
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Shift_Data_Out, with data location in Target ispStream at (row_count x 24)
 - Call procedure: Change_State (to SHIFT state)
- End Loop

Verify Algorithm

A row by row verification procedure is used to verify the ispGDS device, and is basically the same as the verify algorithm, except that each row is compared with (instead of stored in) an ispStream as the data is shifted out of the device. Note that the special pattern used for verifying is used to load the addresses, the same as in the Load algorithm. The

To load a device:

- Call procedure: Get_ID (to check device type)
- Call procedure: Change_State (from IDLE to SHIFT state)
- Set row_count =0
- Loop until row_count = 15
 - Call procedure: Shift_Command, with command: SHIFT_DATA
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Shift_Data_In, with data location in Source ispStream at (row_count x 24)
 - Call procedure: Change_State (to SHIFT state)
 - Call procedure: Shift_Command, with command: VERIFY
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Execute_Command (starts operation)
 - Call procedure: Wait (Verify_Time)
 - Call procedure: Change_State (to SHIFT state)
 - Call procedure: Shift_Command, with command: SHIFT_DATA
 - Call procedure: Change_State (to EXECUTE State)
 - Call procedure: Shift_Data_Out, with data location a 24 bit temporary buffer
 - Compare temp row buffer with data location in ispStream to be verified against, at (row_count x 24)
 - Verify Error if the 24 bits don't match
 - Call procedure: Change_State (to SHIFT state)
- End Loop

PROCEDURES

This section describes the procedures that make up the program, verify and load algorithms for the ispGDS family of devices. The procedures are written so each algorithm may be written in a high-level modular format, calling one of the following procedures to actually change pin levels and handle timing.

Important: Notice that most of the procedures are written so the state machine is left in the Shift State ready to perform the next operation. This point is important in keeping all the routines compatible.

Goto_IDLE Procedure

The Goto_IDLE procedure resets the programming state machine to the IDLE state, regardless of which state it is in.

Procedure Steps:

- set MODE pin High, and SDI pin Low
- wait Tsu
- bring SCLK pin High
- wait Tckh
- bring SCLK pin Low
- (END Procedure)

Get_ID Procedure

The 8 bit device ID code provides the means to identify the three different ispGDS devices. The ID is read in the IDLE state by first loading the ID into the shift register and then clocking the data out. The ID is loaded by holding MODE high and SDI low and clocking the device. The ID is clocked out of the device by holding MODE low and clocking DCLK. Only seven clock cycles are required, since the first bit is available at SDO after the ID is loaded.

8 bit ID codes:

Device	Pins	Device ID
ispGDS22	28	0111 0010 (72 hex)
ispGDS18	24	0111 0001 (71 hex)
ispGDS14	20	0111 0000 (70 hex)

Procedure Steps:

- set MODE pin High, and SDI pin Low
- wait Tsu
- Set SCLK pin High
- wait Tckh
- Set SCLK pin Low
- set count =0
- get value from SDO and store in temp_buffer[0]
- set count = 1
- loop until count == 7
 - bring SCLK pin High
 - wait Twh
 - bring SCLK pin Low
 - wait Twl
 - get value from SDO and store in temp_buffer[count]
- End loop
- (Device ID code is now stored in the temp_buffer array)
- (END procedure)

Change_State Procedure

The Change_State procedure changes the programming state machine to the next state, according to the state diagram.

Procedure Steps:

```
set MODE pin High, and SDI pin High
wait Tsu
bring SCLK pin High
wait Th
set MODE pin Low, and SDI pin Low
wait Tclkh
bring SCLK pin Low
(End Procedure)
```

Shift_Command Procedure

The Shift_Command procedure shifts a five bit command into the device's shift register. The various commands should be coded so the procedure can use a mnemonic (such as PROGRAM), and the controlling software will use the appropriate five bit sequence for that command.

Procedure Steps:

```
set MODE pin Low
set count =0
loop until count == 4
    get next bit of command code (count = bit number)
    set SDI pin to bit value
    wait Tsu
    bring SCLK pin High
    wait Tclkh
    bring SCLK pin Low
    count = count +1
```

End loop

(END Procedure)

Shift_Data_In Procedure

The Shift_Data_In procedure explains the steps to clock a row of data into the device, reading the data from an ispStream. This procedure shifts in 22 bits of data, and is used for all 16 rows.

Procedure Steps:

```
set MODE pin Low
set count =0
loop until count == 23
    get next bit from ispStream ( bit number = count x
row_number)
    set SDI pin to bit value
    wait Tsu
    bring SCLK pin High
```

wait Tclkh

bring SCLK pin Low

End loop

(END Procedure)

Shift_Data_Out Procedure

The Shift_Data_In procedure explains the steps to clock a row of data out of the device and store it in an ispStream. This procedure shifts out 22 bits of data, and is used for all 16 rows.

Procedure Steps:

```
set MODE pin Low
wait Tsu
set count =0
loop until count == 23
    bring SCLK pin High
    wait Tclkh
    bring SCLK pin Low
    get value of SDO pin and store as next bit in ispStream ( bit
number = count x row_number)
```

End loop

(END Procedure)

Execute_Command Procedure

The Execute_Command procedure causes many of the commands to begin executing after the state machine is in the EXECUTE state.

Procedure Steps:

```
set MODE pin Low, and SDI pin Low
wait Tsu
bring SCLK pin High
wait Twh
bring SCLK pin Low
(End Procedure)
```

Wait Procedure

The Wait procedure simply waits the indicated time period, to make sure various timing parameters are met. This procedure is most likely to be used when executing the PROGRAM and ERASE procedures, which need a long delay (tens of milliseconds). The other timing parameters may be able to be guaranteed by the system timing, although the wait procedure can also be used. The various timing parameters should be coded so that a mnemonic (such as PROGRAM_TIME) may be passed to the procedure. This procedure will be system (hardware) specific.

Procedure Steps:

```
wait the indicated time
(End Procedure)
```

ISP PROGRAMMING TOOLS SUPPORT

To assist users in implementing the ISP programming, Lattice provides ispGDS Download software C language routines which implement the basic ISP functions for programming through the PC parallel port. This section provides the details of the ispGDS C code and the PC parallel port definition needed to program the ispGDS.

PC PARALLEL PORT DEFINITION

The PC parallel port must be properly defined in order to use the ispGDS software to program the devices. After defining the port, it is just a matter of using the ispGDS software to read and write from the parallel port. To guarantee the signal integrity and drive capability, a 74HC367 (or equivalent) buffer should be directly connected at the parallel port's DB25 connector. Figure 10 below defines the parallel port DB25 pins and the associated programming signals. This hardware definition is identical to the Lattice ispLSI programming hardware with the exception of the ispEN and RESET signals which are defined only for the ispLSI devices.

The buffer at the parallel port drives the cable that connects the output of the buffer to the ISP programming signals of the

device. It is important to keep the cable length to a minimum to reduce the loading on the signal drivers. The SDI, SCLK and MODE inputs to the ispGDS are driven by the buffer connected at the parallel port. SDO output signal from the ispGDS is driven from the device back to the parallel port. If the load on the SDO signal is more than a minimum cable length and the parallel port input, it is recommended that the user provide a buffer on the circuit board to ensure signal integrity.

ISP SOFTWARE INTERFACE

In addition to the hardware interface, the ispGDS Download C language routines take care of the ispGDS programming software interface. The software interface must implement routines to read and write from the parallel port, to translate JEDEC fusemap to and from the stream file format, and to toggle the ISP hardware signals connected at the output port. Predefined routines for these functions such as `gds_program`, `gds_read`, `gds_verify`, etc. are provided with the ispGDS download software which is available on the Lattice BBS at (503) 693-0215 under the file name GDSPKG.ZIP.

Also available within the GDSPKG.ZIP file is a compiler that supports all the ispGDS devices. These utilities can also be obtained from your local Lattice sales representative.

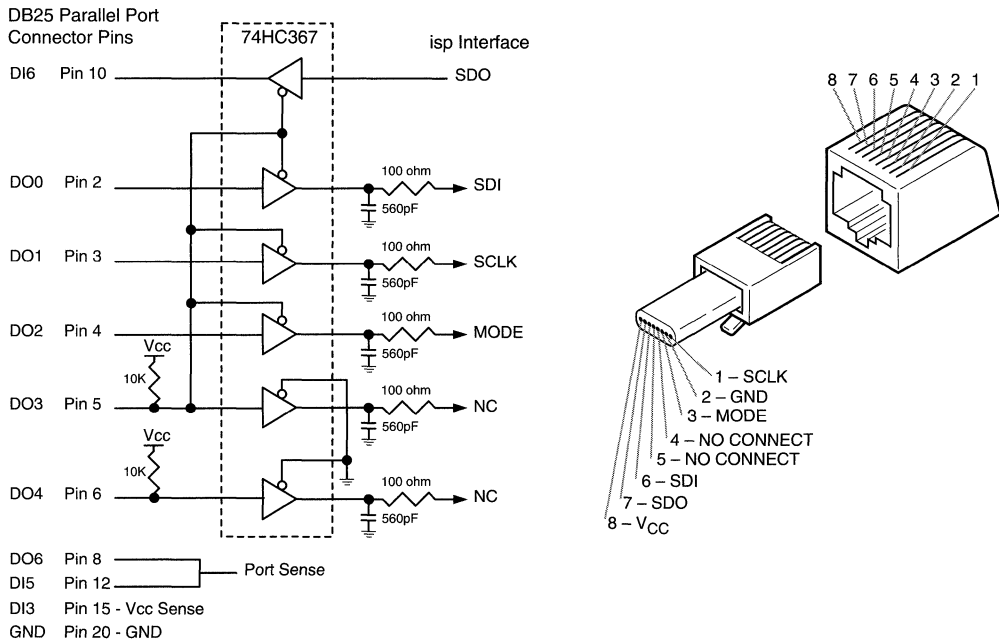
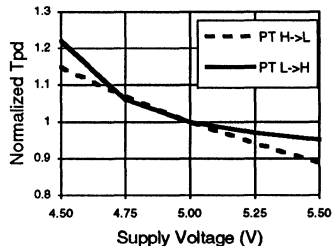


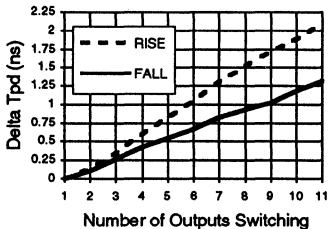
Figure 10. PC Parallel Port Buffer & RJ45 Connector Definition

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

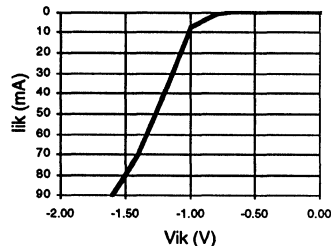
Normalized Tpd vs Vcc



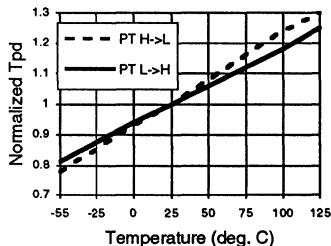
Delta Tpd vs # of Outputs Switching



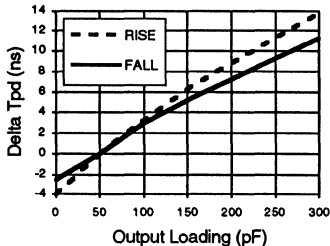
Input Clamp (Vik)



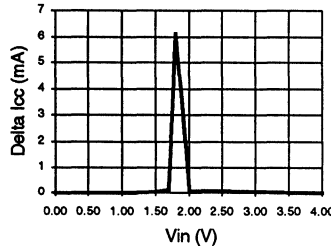
Normalized Tpd vs Temp



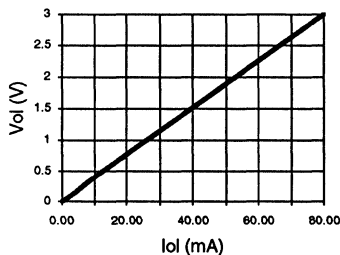
Delta Tpd vs Output Loading



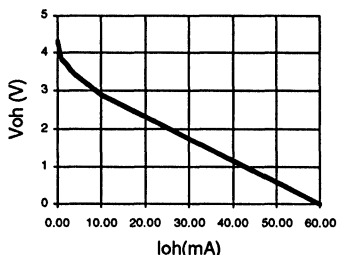
Delta Icc vs Vin (1 Input)



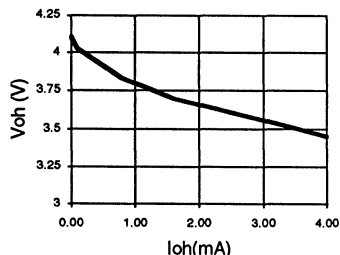
Vol vs Iol



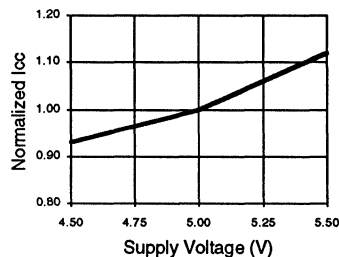
Voh vs Ioh



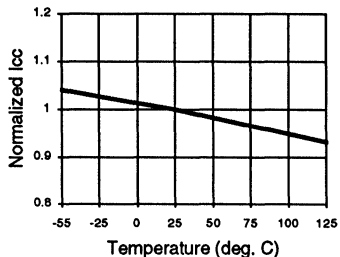
Voh vs Ioh



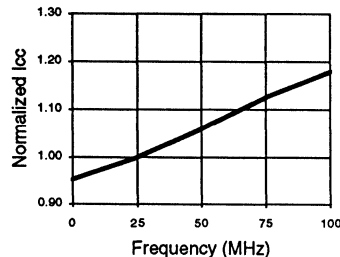
Normalized Icc vs Vcc



Normalized Icc vs Temp



Normalized Icc vs Freq.



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Section 2: High-Density Programmable Logic

Section 3: Low-Density Programmable Logic

Section 4: In-System Programmable Generic Digital Switch (ispGDS) Devices

Section 5: Military Program

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pLSI and ispLSI 1024 (See Commercial Datasheet)	
pLSI and ispLSI 1032 (See Commercial Datasheet)	

Section 6: Development Tools

Section 7: Quality and Reliability

Section 8: General Information



Military Program Overview

CORPORATE PHILOSOPHY

Lattice Semiconductor is committed to leadership in device performance and quality. Our family of Military GAL devices is a reflection of this philosophy. Lattice manufactures all devices under strict Quality Assurance guidelines. All grades, Commercial through Military 883, are monitored under a quality program conformant to MIL-I-38535 Appendix C with inspections conformant to MIL-I-45208.

Complete reviews of Lattice's procedures, documentation and technical data are welcomed and can be arranged at the Company's facility near Portland, Oregon.

QUALITY AND TESTABILITY

Lattice Semiconductor processes its devices to strict conformance with MIL-STD-883 Class B. In conjunction with the military flow, the inherent testability of E²CMOS technology allows Lattice to achieve a quality level superior to other PLD technologies.

All devices are patterned and tested dozens of times throughout the manufacturing flow. Every device is tested under worst case configurations to assure customers achieve 100% yields. Tests are performed using the same E² cell array that will be used for the final patterning of the devices. This 100% "actual test" philosophy does away with the correlated and simulated testing that is necessary with bipolar and UV (EPROM) based PLD devices.

RELIABILITY

Lattice Semiconductor performs extensive reliability testing prior to product release. This testing continues in the form of Reliability Monitors that are run on an ongoing basis to assure continued process integrity. A formal, written report of these test results is updated regularly and can be obtained from your local Lattice Sales Representative.

The reliability testing performed includes extensive analysis of fundamental design and process integrity. The reprogrammable nature of Lattice devices allows for an inherently more thorough reliability evaluation than other programmable alternatives.

MIL-STD-883 COMPLIANCE

MIL-STD-883 defines a uniform and precise method for environmental, mechanical and electrical testing which ensures the suitability of microelectronic devices for use in military and aerospace systems. Table I summarizes the MIL-STD-883, Class B flow. Table II summarizes the conformance testing required by MIL-STD-883, Method 5005, for quality conformance testing of Lattice military microcircuits.

MIL-I-38535

MIL-I-38535 Appendix A and C, when used in conjunction with MIL-STD-883, define design, packaging, material, marking, sampling, qualification and quality system requirements for Lattice military devices.

GROUP DATA

Group A and B data is taken on every inspection lot per MIL-STD-883, Class B requirements. This data, along with Generic Group C and D data can be supplied, upon written request, with your device shipment. Your Lattice sales representative can advise you of charges and leadtime necessary for providing this data.

STANDARD MILITARY DRAWINGS

Lattice actively supports the DESC Standard Military Drawing (SMD) Program. The SMD Program offers a cost effective alternative to source control drawings and provides standardized MIL-STD-883 product specifications to simplify military procurement.

A list of currently available SMD qualified devices is provided (see Military Ordering Information).

Military Program Overview

**MILITARY SCREENING FLOW
(TABLE I)**

Screen	Method	Requirement
Internal Visual	2010 Cond. B	100%
Temp. Cycling	1010 Cond. C	100%
Constant Acceleration	2001 Cond. E	100%
Hermeticity	1014	100%
Fine	Cond. A or B	
Gross	Cond. C	
Endurance Test	1033	100%
Retention Test	Unbiased Bake 24 HRS. T _A = 180°C	100%
Pre Burn-In Electrical	Applicable Device Specification T _c = 25°C	100%
Dynamic Burn-In	1015 Cond. D	100%
Post Burn-In Electrical	Applicable Device Specification T _c = 25°C PDA = 5%	100%
Final Electrical Test	Applicable Device Specification T _c = 125°C	100%
Final Electrical Test	Applicable Device Specification T _c = - 55°C	100%
Final Electrical Test	Applicable Device Specification T _c = 25°C	100%
External Visual	2009	100%
QCI Sample Selection	MIL-M-38535, Appendix A Sec. 4.5 and MIL-STD-883 Sec. 1.2	Sample

**MILITARY QUALITY CONFORMANCE
INSPECTIONS (TABLE II)**

Subgroup	Method	Sample
GROUP A: Electrical Tests		
<i>Subgroups 1, 7, 9</i> Electrical Test	Applicable Device Spec. 25°C	LTPD = 2
<i>Subgroups 2, 8A, 10</i> Electrical Test	Applicable Device Spec. Max. Operating Temp.	LTPD = 2
<i>Subgroups 3, 8B, 11</i> Electrical Test	Applicable Device Spec. Min. Operating Temp.	LTPD = 2
GROUP B: Mechanical Tests		
<i>Subgroup 2</i> Solvent Resistance	2015	4(0)
<i>Subgroup 3</i> Solderability	2003	LTPD = 10
<i>Subgroup 5</i> Bond Strength	2011	LTPD = 15
GROUP C: Chip Integrity Tests		
<i>Subgroup 1</i> Dynamic Life Test End Point Electrical	1005, 1,000 HRS. 125°C Applicable Device Spec.	LTPD = 5
<i>Subgroup 2</i> Unbiased Retention End Point Electrical	1,000 HRS. 150°C Applicable Device Spec.	LTPD = 5
GROUP D: Environmental Integrity		
<i>Subgroup 1</i> Physical Dimensions	2016	LTPD = 15
<i>Subgroup 2</i> Lead Integrity Hermeticity	2004, Cond. B 1014	LTPD = 5
<i>Subgroup 3</i> Thermal Shock Temp. Cycle Moisture Resistance Hermeticity Visual Examination Endpoint Electrical	1011, Cond. B, 15 Cycles 1010, Cond. C, 100 Cycles 1004 1014 1004, 1010 Applicable Device Spec.	LTPD = 15
<i>Subgroup 4</i> Mechanical Shock Vibration Constant Acceleration Hermeticity Visual Examination Endpoint Electrical	2002, Cond. B 2007, Cond. A 2001, Cond. E 1014 1010, 1011 Applicable Device Spec.	LTPD = 15
<i>Subgroup 5</i> Salt Atmosphere Hermeticity Visual Examination	1009, Cond. A 1014 1009	LTPD = 15
<i>Subgroup 6</i> Internal Water Vapor	1018 < 5,000 PPM, 100°C	3(0)
<i>Subgroup 7</i> Lead Finish Adhesion	2025	LTPD = 15
<i>Subgroup 8</i> Lid Torque	2024	5(0)

Military Ordering Information

Lattice offers the most comprehensive line of military E²CMOS Programmable Logic Devices. Lattice recognizes the trend in military device procurement towards using SMD compliant devices and encourages customers

to use the SMD number where it exists, when ordering parts. Listed below are Lattice's military qualified devices and their corresponding SMD numbers. Please contact your local Lattice representative for the latest product listing.

Military Products Selector Guide

Family	Part #	SMD #	Tpd (ns)	Fmax (MHz)	Icc		Package
					Typ (mA)	Max (mA)	
pLSI	pLSI 1016-60LH/883	Contact Factory	20	60	100	170	44-Pin JLCC
	pLSI 1024-60LH/883	Contact Factory	20	60	130	215	68-Pin JLCC
	pLSI 1032-60LG/883	5962-9466801MXC	20	60	135	220	84-Pin CPGA
ispLSI	ispLSI 1016-60LH/883	Contact Factory	20	60	100	170	44-Pin JLCC
	ispLSI 1024-60LH/883	Contact Factory	20	60	130	215	68-Pin JLCC
	ispLSI 1032-60LG/883	5962-9308501MXC	20	60	135	220	84-Pin CPGA
GAL16V8	GAL16V8B-10LD/883	5962-8983904RA	10	62.5	75	130	20-Pin CERDIP
	GAL16V8B-10LR/883	5962-89839042A	10	62.5	75	130	20-Pin LCC
	GAL16V8B-15LD/883	5962-8983903RA	15	50	75	130	20-Pin CERDIP
	GAL16V8B-15LR/883	5962-89839032A	15	50	75	130	20-Pin LCC
	GAL16V8A-20LD/883	5962-8983902RA	20	41.6	75	130	20-Pin CERDIP
	GAL16V8A-20LR/883	5962-89839022A	20	41.6	75	130	20-Pin LCC
	GAL16V8A-30LD/883	5962-8983901RA	30	33.3	75	130	20-Pin CERDIP
GAL20V8	GAL20V8B-10LD/883	5962-8984004LA	10	62.5	75	130	24-Pin CERDIP
	GAL20V8B-10LR/883	5962-89840043A	10	62.5	75	130	28-Pin LCC
	GAL20V8B-15LD/883	5962-8984003LA	15	50	75	130	24-Pin CERDIP
	GAL20V8A-15LR/883	5962-89840033A	15	50	75	130	28-Pin LCC
	GAL20V8B-20LD/883	5962-8984002LA	20	41.6	75	130	24-Pin CERDIP
	GAL20V8A-20LR/883	5962-89840023A	20	41.6	75	130	28-Pin LCC
GAL22V10	GAL22V10B-15LD/883	5962-8984103LA	15	62.5	90	150	24-Pin CERDIP
	GAL22V10B-15LR/883	5962-89841033A	15	62.5	90	150	28-Pin LCC
	GAL22V10B-20LD/883	5962-8984102LA	20	33	90	150	24-Pin CERDIP
	GAL22V10B-20LR/883	5962-89841023A	20	33	90	150	28-Pin LCC
	GAL22V10B-25LD/883	5962-8984104LA	25	33	90	150	24-Pin CERDIP
	GAL22V10B-30LD/883	5962-8984101LA	30	25	90	150	24-Pin CERDIP

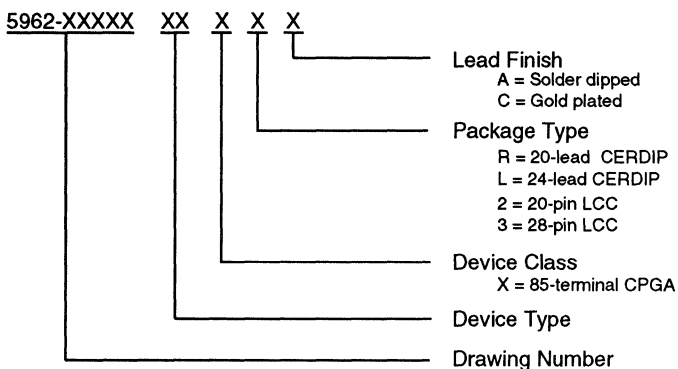
Military Ordering Information

DESC Standard Military Drawing Listing

SMD #	LATTICE PART #
5962-8983901FA	GAL16V8A-30LD/883
5962-89839022A	GAL16V8A-20LR/883
5962-8983902FA	GAL16V8A-20LD/883
5962-89839032A	GAL16V8B-15LR/883
5962-8983903FA	GAL16V8B-15LD/883
5962-89839042A	GAL16V8B-10LR/883
5962-8983904FA	GAL16V8B-10LD/883
5962-89840023A	GAL20V8A-20LR/883
5962-8984002LA	GAL20V8A-20LD/883
5962-89840033A	GAL20V8A-15LR/883
5962-8984003LA	GAL20V8A-15LD/883

SMD #	LATTICE PART #
5962-89840043A	GAL20V8B-10LR/883
5962-8984004LA	GAL20V8B-10LD/883
5962-8984101LA	GAL22V10B-30LD/883
5962-89841023A	GAL22V10B-20LR/883
5962-8984102LA	GAL22V10B-20LD/883
5962-89841033A	GAL22V10B-15LR/883
5962-8984103LA	GAL22V10B-15LD/883
5962-8984104LA	GAL22V10B-25LD/883
5962-9308501MXC	ispLSI 1032-60LG/883
5962-9466801MXC	pLSI 1032-60LG/883

Standard Military Drawing Number Description





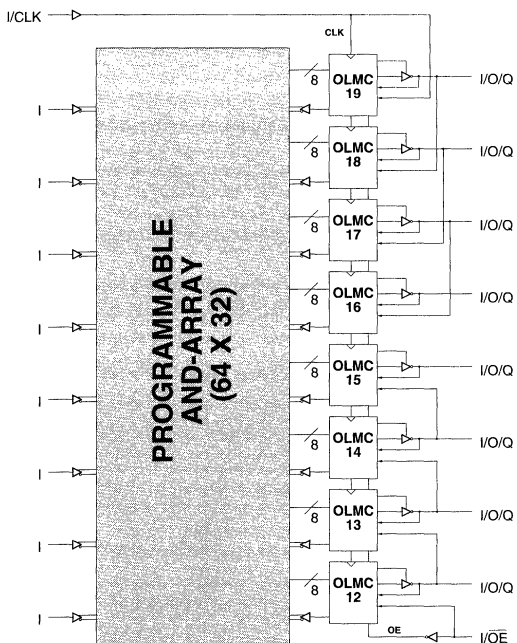
GAL16V8/883

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 10 ns Maximum Propagation Delay
 - Fmax = 62.5 MHz
 - 7 ns Maximum from Clock Input to Data Output
 - TTL Compatible 12 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **50% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ Icc
- **ACTIVE PULL-UPS ON ALL PINS (GAL16V8B-10)**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



5

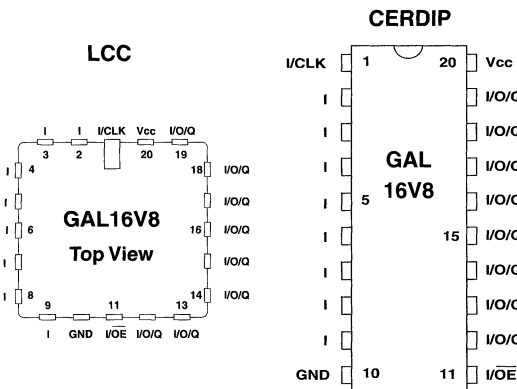
DESCRIPTION

The GAL16V8/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed/power performance available in the 883 qualified PLD market. The GAL16V8B/883, at 10ns maximum propagation delay time, is the world's fastest military qualified CMOS PLD.

The generic GAL architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8/883 is capable of emulating all standard 20-pin PAL® devices with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS	
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V	
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V	
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	L-10	—	—	-100	μA
			L-15	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA	
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V	
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V	
I_{OL}	Low Level Output Current		—	—	12	mA	
I_{OH}	High Level Output Current		—	—	-2	mA	
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA	
ICC	Operating Power	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$	—	75	130	mA	
	Supply Current	$f_{toggle} = 15MHz \text{ Outputs Open}$					

- 1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-10		-15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	2	10	3	15	ns
t_{co}	A	Clock to Output Delay	1	7	2	12	ns
t_{cf}²	—	Clock to Feedback Delay	—	7	—	12	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	58.8	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	58.8	—	41.6	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	50	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	10	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	10	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	10	—	15	ns
	B	\overline{OE} to Output Enabled	—	10	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	10	—	15	ns
	C	\overline{OE} to Output Disabled	—	10	—	15	ns

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 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

 3) Refer to **f_{max} Descriptions** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	10	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	10	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS	
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V	
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V	
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA	
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA	
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V	
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V	
I_{OL}	Low Level Output Current		—	—	12	mA	
I_{OH}	High Level Output Current		—	—	-2.0	mA	
I_{OS}¹	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA	
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 25MHz$ Outputs Open		L -20/-30	75	130	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹	DESCRIPTION	-20		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	3	20	3	30	ns
t_{co}	A	Clock to Output Delay	2	15	2	20	ns
t_{cf}²	—	Clock to Feedback Delay	—	15	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	15	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	33.3	—	22.2	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	33.3	—	22.2	—	MHz
	A	Maximum Clock Frequency with No Feedback	41.6	—	33.3	—	MHz
t_{wh}	—	Clock Pulse Duration, High	12	—	15	—	ns
t_{wl}	—	Clock Pulse Duration, Low	12	—	15	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	20	—	30	ns
	B	$\overline{\text{OE}}$ to Output Enabled	—	18	—	25	ns
t_{dis}	C	Input or I/O to Output Disabled	—	20	—	30	ns
	C	$\overline{\text{OE}}$ to Output Disabled	—	18	—	25	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from **f_{max}** with internal feedback. Refer to **f_{max} Descriptions** section.

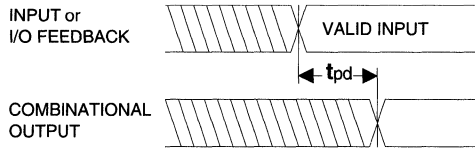
 3) Refer to **f_{max} Descriptions** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

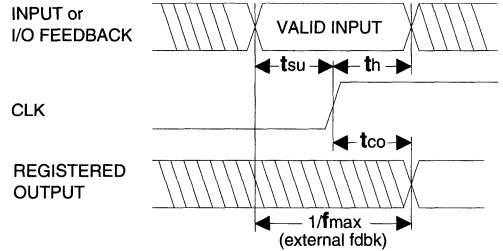
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	10	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	10	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

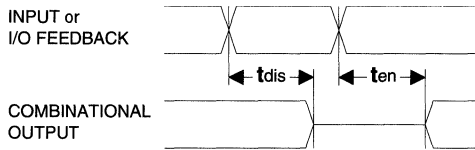
SWITCHING WAVEFORMS



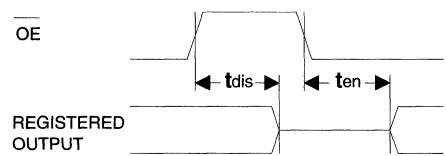
Combinatorial Output



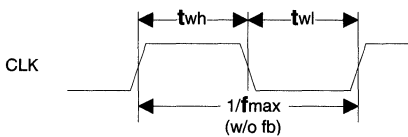
Registered Output



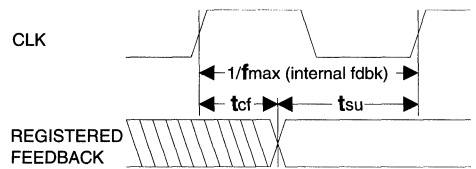
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

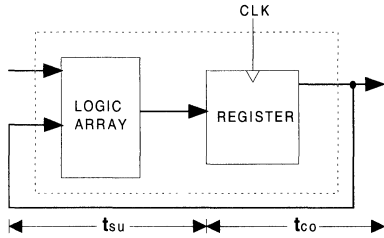


Clock Width



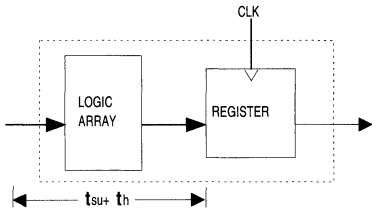
f_{max} with Feedback

f_{max} DESCRIPTIONS



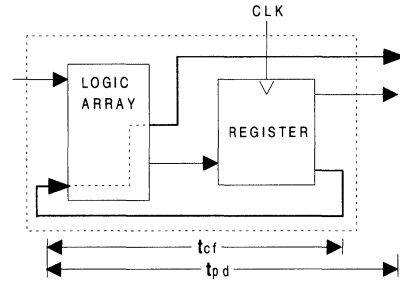
f_{max} with External Feedback 1/(t_{su}+t_{co})

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback 1/(t_{su}+t_{cf})

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback (t_{cf} = 1/f_{max} - t_{su}). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

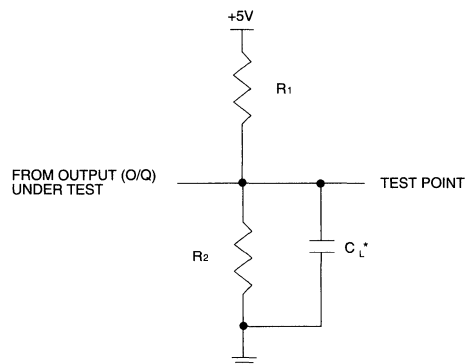
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	390Ω	750Ω	50pF
B	Active High	∞	750Ω
	Active Low	390Ω	750Ω
C	Active High	∞	5pF
	Active Low	390Ω	750Ω



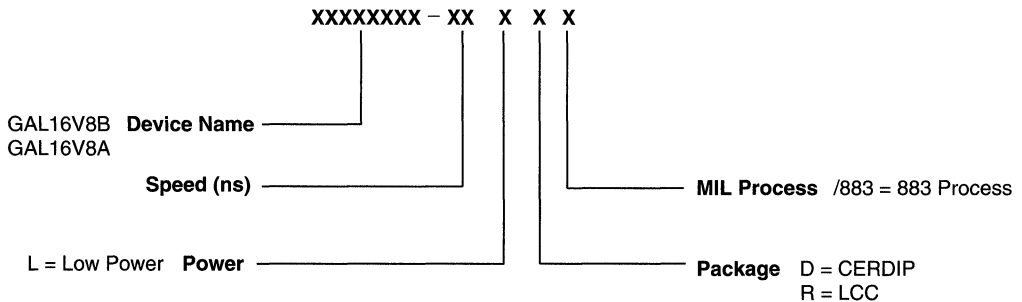
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL16V8 ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
10	10	7	130	20-Pin Cerdip	GAL16V8B-10LD/883	5962-8983904RA
			130	20-Pin LCC	GAL16V8B-10LR/883	5962-89839042A
15	12	12	130	20-Pin Cerdip	GAL16V8B-15LD/883	5962-8983903RA
			130	20-Pin LCC	GAL16V8B-15LR/883	5962-89839032A
20	15	15	130	20-Pin Cerdip	GAL16V8A-20LD/883	5962-8983902RA
			130	20-Pin LCC	GAL16V8A-20LR/883	5962-89839022A
30	25	20	130	20-Pin Cerdip	GAL16V8A-30LD/883	5962-8983901RA

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 10 ns Maximum Propagation Delay
 - Fmax = 62.5 MHz
 - 7 ns Maximum from Clock Input to Data Output
 - TTL Compatible 12 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **50% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ Icc on Low Power Device
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

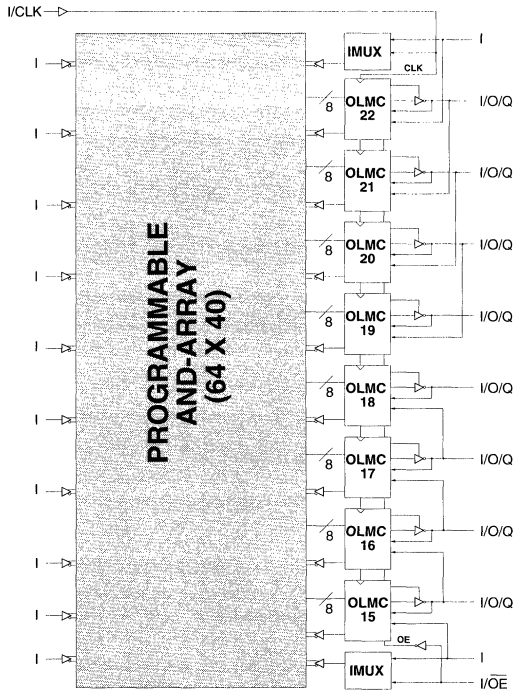
DESCRIPTION

The GAL20V8/883 is a high performance E²CMOS programmable logic devices processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed/power performance available in the 883 qualified PLD market.

The generic GAL architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20V8/883 is capable of emulating all standard 24-pin PAL® devices with full function/fuse map/parametric compatibility.

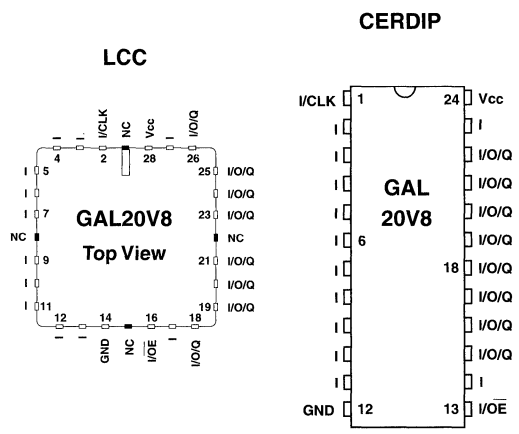
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



5

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}¹	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz \text{ Outputs Open}$		L -10	75 130	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	-10		UNITS
			MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	2	10	ns
t_{co}	A	Clock to Output Delay	1	7	ns
t_{cf}²	—	Clock to Feedback Delay	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock [↑]	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock [↑]	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	58.8	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	58.8	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	10	ns
	B	\overline{OE} to Output Enabled	—	10	ns
t_{dis}	C	Input or I/O to Output Disabled	—	10	ns
	C	\overline{OE} to Output Disabled	—	10	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

 3) Refer to **f_{max} Descriptions** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _I	Input Capacitance	10	pF	V _{cc} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	10	pF	V _{cc} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS	
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V	
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V	
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA	
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA	
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V	
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V	
I_{OL}	Low Level Output Current		—	—	12	mA	
I_{OH}	High Level Output Current		—	—	-2.0	mA	
I_{OS}'	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA	
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 25MHz$ Outputs Open		L -15/-20	75	130	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	3	15	3	20	ns
t_{co}	A	Clock to Output Delay	2	12	2	15	ns
t_{cf}^2	—	Clock to Feedback Delay	—	12	—	15	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
f_{max}^3	A	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with No Feedback	50	—	41.6	—	MHz
t_{wh}	—	Clock Pulse Duration, High	10	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	10	—	12	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	ns
	B	\overline{OE} to Output Enabled	—	15	—	18	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	ns
	C	\overline{OE} to Output Disabled	—	15	—	18	ns

 1) Refer to **Switching Test Conditions** section.

 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Descriptions** section.

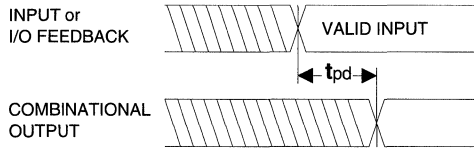
 3) Refer to **f_{max} Descriptions** section.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

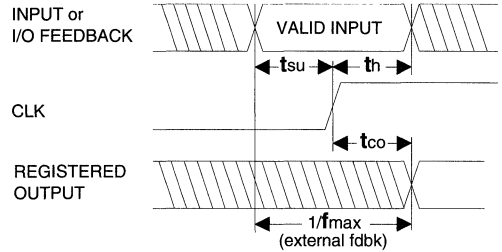
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	10	pF	$V_{CC} = 5.0V$, $V_I = 2.0V$
$C_{i/o}$	I/O Capacitance	10	pF	$V_{CC} = 5.0V$, $V_{i/o} = 2.0V$

*Guaranteed but not 100% tested.

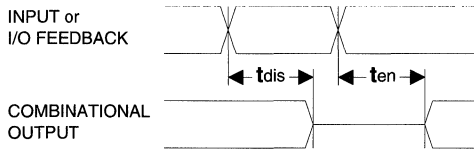
SWITCHING WAVEFORMS



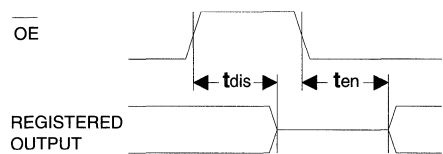
Combinatorial Output



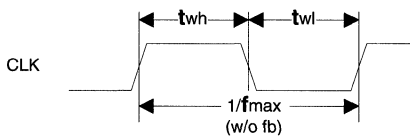
Registered Output



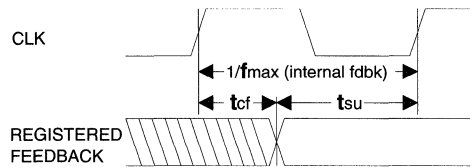
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

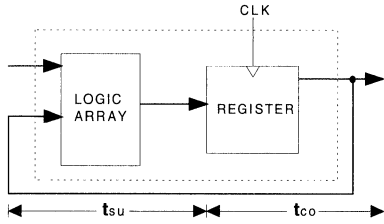


Clock Width



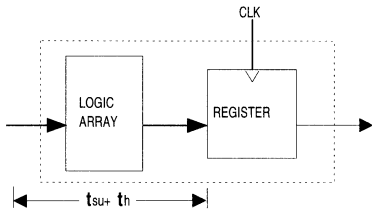
f_{max} with Feedback

f_{max} DESCRIPTIONS



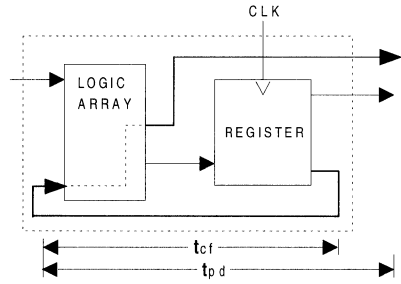
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

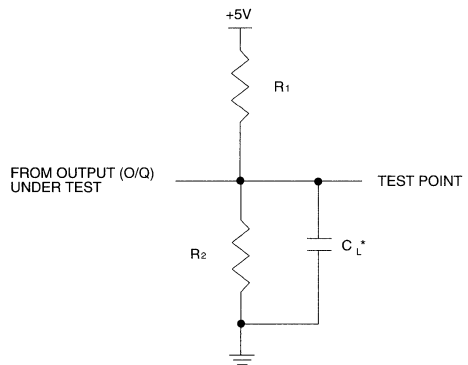
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	390Ω	750Ω	50pF
B	Active High	∞	750Ω
	Active Low	390Ω	750Ω
C	Active High	∞	750Ω
	Active Low	390Ω	750Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

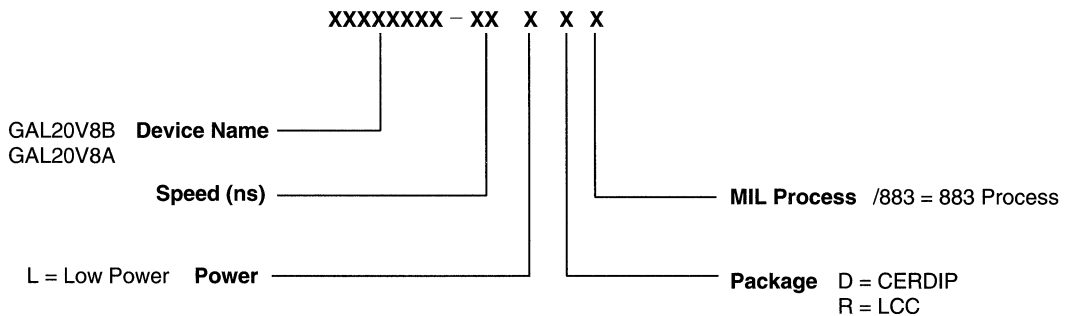
GAL20V8 ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
10	10	7	130	24-Pin Cerdip	GAL20V8B-10LD/883	5962-8984004LA*
			130	28-Pin LCC	GAL20V8B-10LR/883	5962-89840043A*
15	12	12	130	24-Pin Cerdip	GAL20V8A-15LD/883	5962-8984003LA
			130	28-Pin LCC	GAL20V8A-15LR/883	5962-89840033A
20	15	15	130	24-Pin Cerdip	GAL20V8A-20LD/883	5962-8984002LA
			130	28-Pin LCC	GAL20V8A-20LR/883	5962-89840023A

*Preliminary

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

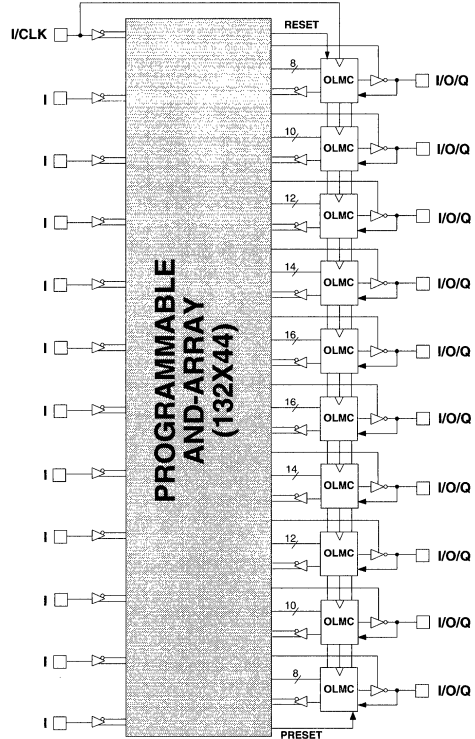
PART NUMBER DESCRIPTION



FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
 - 15 ns Maximum Propagation Delay
 - F_{max} = 62.5 MHz
 - 8ns Maximum from Clock Input to Data Output
 - TTL Compatible 12 mA Outputs
 - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
 - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMS 22V10 Devices
- **50% REDUCTION IN POWER VERSUS BIPOLAR**
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



5

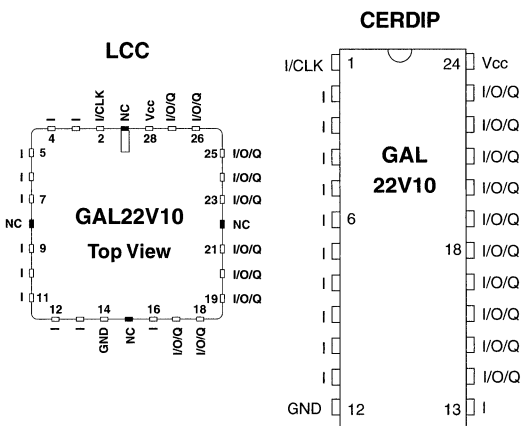
DESCRIPTION

The GAL22V10/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available of any military qualified 22V10 device. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.

PACKAGE DIAGRAMS



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply Voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}¹	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}²	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ $f_{toggle} = 15MHz$ Outputs Open	L -15/-20/-25/-30	—	90 150	mA

- 1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
- 3) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND. ¹	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	15	—	20	—	25	—	30	ns
t_{co}	A	Clock to Output Delay	—	8	—	15	—	20	—	20	ns
t_{cf}²	—	Clock to Feedback Delay	—	8	—	15	—	20	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	12	—	17	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	50	—	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	50	—	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	33	—	33	—	25	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	15	—	15	—	20	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	15	—	15	—	20	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	—	25	—	25	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	—	25	—	25	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	—	20	—	25	—	30	—	30	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	20	—	25	—	30	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	15	—	20	—	25	—	30	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	12	—	17	—	20	—	25	—	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from **f_{max}** with internal feedback. Refer to **f_{max} Description** section.

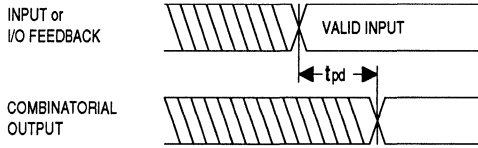
3) Refer to **f_{max} Description** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

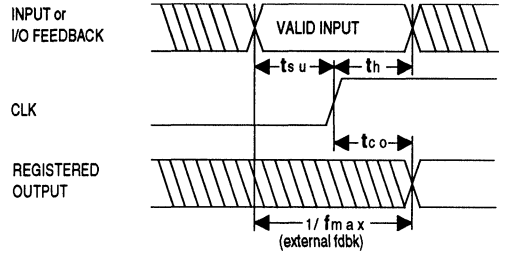
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C _i	Input Capacitance	10	pF	V _{CC} = 5.0V, V _I = 2.0V
C _{I/O}	I/O Capacitance	10	pF	V _{CC} = 5.0V, V _{I/O} = 2.0V

*Guaranteed but not 100% tested.

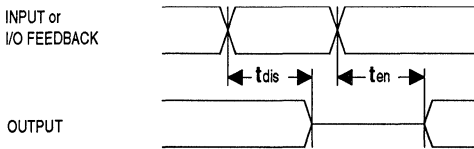
SWITCHING WAVEFORMS



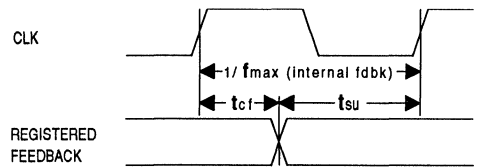
Combinatorial Output



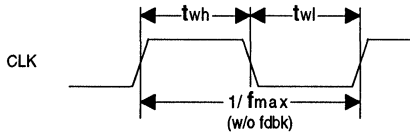
Registered Output



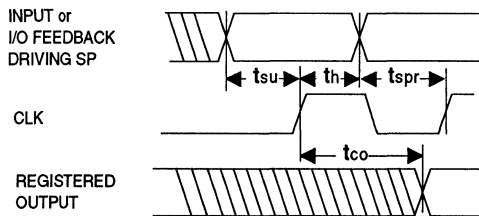
Input or I/O to Output Enable/Disable



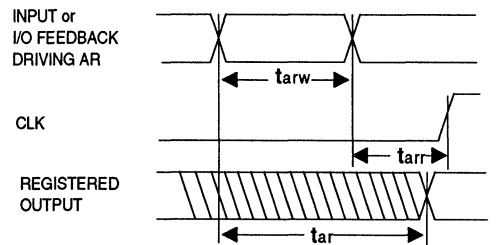
fmax with Feedback



Clock Width

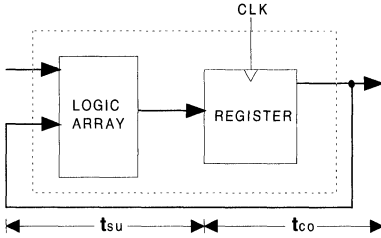


Synchronous Preset



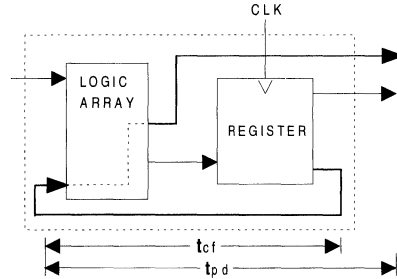
Asynchronous Reset

f_{max} DESCRIPTIONS



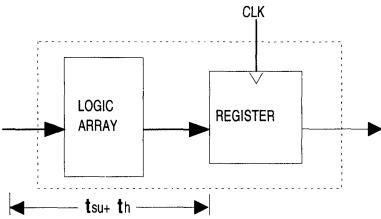
f_{max} with External Feedback $1/(t_{su}+t_{co})$

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.

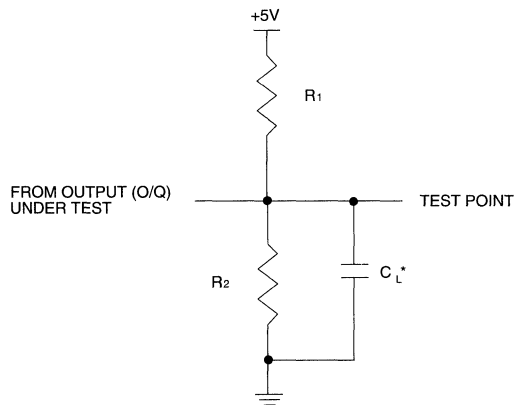
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	390Ω	750Ω	50pF
B	Active High	∞	750Ω
	Active Low	390Ω	750Ω
C	Active High	∞	5pF
	Active Low	390Ω	750Ω



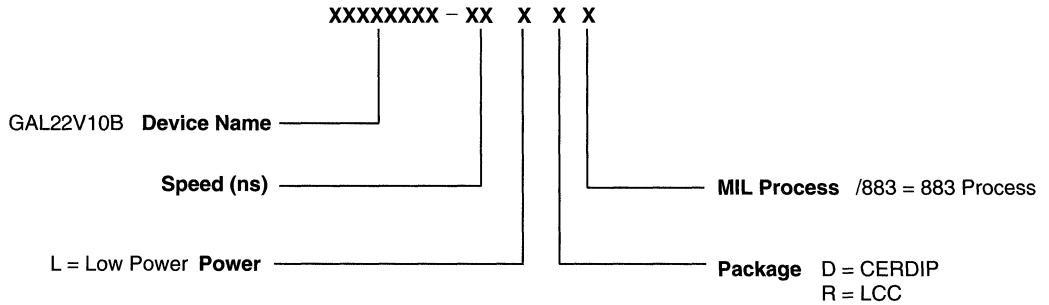
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL22V10 ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering #	
					MIL-STD-883	SMD #
15	12	8	150	24-Pin CERDIP	GAL22V10B-15LD/883	5962-8984103LA
			150	28-Pin LCC	GAL22V10B-15LR/883	5962-89841033A
20	17	15	150	24-Pin CERDIP	GAL22V10B-20LD/883	5962-8984102LA
			150	28-Pin LCC	GAL22V10B-20LR/883	5962-89841023A
25	20	20	150	24-Pin CERDIP	GAL22V10B-25LD/883	5962-8984104LA
30	25	20	150	24-Pin CERDIP	GAL22V10B-30LD/883	5962-8984101LA

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION



Section 1: Introduction

Section 2: High-Density Programmable Logic

Section 3: Low-Density Programmable Logic

Section 4: In-System Programmable Generic Digital Switch (ispGDS) Devices

Section 5: Military Program

Section 6: Development Tools

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Section 8: General Information

Lattice Design Tool Strategy

Introduction

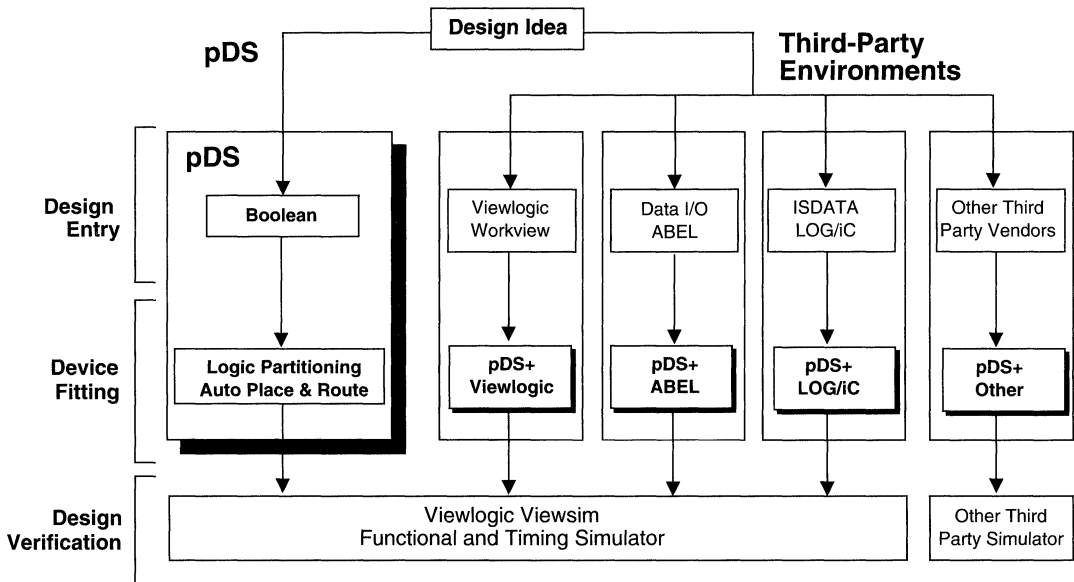
The Lattice design tool strategy for the pLSI and ispLSI families is to support a wide range of design environments. Lattice provides both a proprietary PC-based solution (pDS[®]) as well as third-party compatible CAE tools (pDS+[™] Fitters) that run on PC and Sun workstation platforms.

The Lattice pDS (pLSI and ispLSI Development System) software provides a comprehensive, high-performance, low-cost package for logic development. Developed and supported by Lattice, pDS provides an easy-to-use Windows-based graphical interface using a mouse and pull-down menus. Design entry includes Boolean equations and macros. For simulation, timing tables are included as a standard offering. Additionally, pDS interfaces with Viewlogic's Viewsim simulation package for full functional and timing simulation. pDS software generates industry standard JEDEC programming files and supports direct download into ispLSI devices.

Lattice's pDS+ (pDS Plus) solution supports multiple third-party CAE tools, providing designers with the capability to design in familiar CAE environments. These third-party CAE tools offer schematic capture, hardware description language (such as VHDL), state machine language, Boolean equation, and macro design entry as well as functional and timing simulators for design verification.

Lattice's pDS and pDS+ solutions give designers powerful, easy to use, cost-effective design tools to meet their development needs. Each third-party vendor must adhere to strict quality and certification requirements before becoming qualified, thus ensuring superior support. Additional support for popular third-party CAE tools is scheduled. Contact your local Lattice Sales Representative for availability.

Figure 1. pDS and pDS+ Design Flows



Lattice Design Tool Strategy

Lattice Design Flow

There are three steps in the Lattice pLSI and ispLSI design flow: design entry, device fitting (logic partitioning, place and route), and design verification. (See the pDS and pDS+ Design Flow). This section outlines the design flow of the pDS and pDS+ solutions.

Lattice pDS

Lattice's pDS solution is a comprehensive, self-contained design solution which operates on a PC under Microsoft Windows. pDS uses familiar ABEL-like Boolean equation and macro design entry, and provides manual partitioning, high speed automatic place and route, and simulation timing tables for design verification. Viewlogic's Viewsim simulation package is compatible with pDS for functional and timing simulation.

After the development work has been completed, the design is ready to be programmed into a device. For third-party programming support, the pDS package generates a JEDEC fusemap. Alternatively, the ispLSI devices can be programmed directly from the PC or Sun workstation with the Lattice isp Engineering Kit.

The pDS development systems are ideal for designers who desire a cost-effective, user friendly approach to pLSI and ispLSI design.

Lattice pDS+

The pDS+ solution combines third-party CAE tools for design entry and verification with the Lattice pDS+ Fitter for device fitting to offer a powerful and complete development solution. Initial Fitter products include the pDS+ ABEL Fitter, pDS+ Viewlogic Fitter, and pDS+ LOG/iC Fitter which interface with their respective third party design tools.

The design entry step is typically performed with schematic capture, Boolean equations, state machines, truth tables or a Hardware Description Language (HDL). Once design entry is complete, the design is ready to be implemented into a Lattice pLSI or ispLSI device.

The Lattice pDS+ Fitter uses architecture-specific algorithms to synthesize a logic description into a pLSI or ispLSI device. Steps in the device fitting process include logic optimization and minimization, automatic logic partitioning, and automatic place and route.

pDS+ also supports design verification. Design verification options include both functional and timing simulation. Various combinations of graphical and text-based functional and timing simulators are supported by third-party CAE vendors.

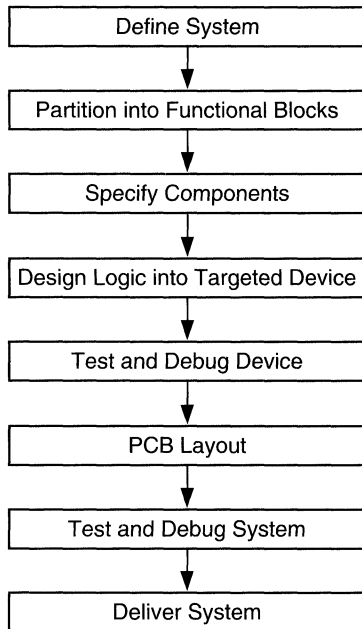
Following design verification, the Lattice pDS+ Fitter generates a JEDEC fusemap for device programming. The design can be programmed into a pLSI device using third-party programmers. In addition, the ispLSI devices can be programmed directly from the PC or Sun workstation system using Lattice's isp Engineering Kit, or from dedicated logic designed into the end-system.

System Design Process

Introduction

Conceptually, system definition is the first step in the design process. This involves visualizing the PLD's interaction with the rest of the electronic system and defining a general flow diagram to determine the design's basic sequential behavior. This organizational flow, used to integrate an entire subsystem into high density devices, is described in the following topics and shown in figure 1.

Figure 1. System Design Flow



Partitioning

After completing the conceptual design, the designer partitions the system into modules or functional blocks. These blocks can be a few components or multiple circuit boards with numerous components. The designer organizes these functional blocks to match the capabilities of the devices being targeted, for example, the number of I/O pins, flip-flops and gates needed. The user should also consider the frequency at which the targeted device must operate, the number of clocks required, and the timing relationships of signals (AC specifications).

Specifying Components

After the partitioning is defined, the designer chooses the components which will be used to implement the desired functions. The design should meet the system specifications using the least number of components in order to keep the system cost as low as possible while keeping the system reliability as high as possible.

System specifications calling for low weight, low power and reduced size also drive designers to higher levels of logic integration. These added requirements can adversely affect the design schedule and project completion. The pLSI and ispLSI high-density devices can meet such design requirements while delivering excellent performance. The pLSI and ispLSI family of high-speed, high-density PLDs supported by easy-to-use effective software for fast design implementation and verification.

Design Entry and Optimization

After the functional partitioning and component specifications are completed, the logic necessary to implement the functions is defined block by block. The logic may include standard TTL functions, CMOS logic functions, or functions from a library, such as the Lattice Macro Library. The implementation of logic into a high density device is optimized for the targeted device by the design software. The partitioning also affects the optimization. Optimization can be for speed, utilization or a combination of both.

Logic entry for a Lattice high density device is done with the pLSI/ispLSI Development System or with any of Lattice's pDS+ Fitter products (pDS+ Viewlogic, pDS+ ABEL, pDS+ LOG/iC, etc.). The pDS software utilizes the Graphical User Interface (GUI) of Microsoft's Windows™ to provide a complete design flow from logic entry to program-

System Design Process

ming pLSI/ispLSI devices within hours. The pDS+ ABEL software supports textual design entry using a Hardware Description Language (HDL). Standard CAE schematic design entry is supported by the pDS+ Viewlogic software. pDS+ LOG/iC supports Boolean, truth table and state machine entry.

Test and Debug

When designing a system, or a portion of a system, it is easier to test and debug pieces or modules rather than the entire system. In this manner, the designer can confirm module designs, or functional blocks, and find problems earlier in the design cycle.

Logic can be verified by either timing simulation or actual testing of the programmed device. Simulation can be accomplished using the Viewlogic Viewsim logic simulator (available from Lattice). Design errors detected by software simulation can be corrected by the designer before the printed circuit board is laid out and manufactured, which saves time and reduces cost. Board and system level simulation can be accomplished through behavioral simulation using Logic Modeling Corporation's models.

Reprogrammable devices allow the designer to test, debug, and modify logic right on the p.c. board. pLSI and ispLSI devices can be reprogrammed multiple times. This reprogrammability further assists the designers by allowing them to temporarily program the devices with diagnostic and design verification logic.

The designer should always attempt to design logic with testability in mind. Testability means different things to different designers. Key guidelines to be aware of are:

- Large counters should be segmented for quick and easy testing.
- Logic should be designed for controllability and observability.
- There should be no floating nets.
- All nets should be at a known state or are able to be set or reset.

To assist system testability, the ispLSI devices offer preload and verification features. These features allow register contents to be verified without using logic analyzers or other debugging tools.

Printed Circuit Board Layout

Once the logic has been verified, the Printed Circuit Board (PCB) is laid out and manufactured. Since the logic may be changed during design, this phase of the system design is usually executed after the logic has been validated. It is recommended that board design and layout be done after verifying designs using pLSI and ispLSI parts.

System Test and Debug

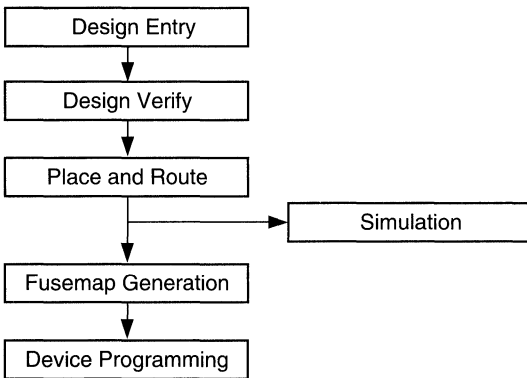
System test and debug is the final stage of the design process. The logic and the PCB are tested as a system and minor enhancements or bug fixes are implemented. Because of the flexibility of the pLSI and ispLSI devices, minor changes can be made without affecting the layout of the PCB or the pinout of the device.

pLSI and ispLSI Design Flow

Introduction

Once the system design has been organized into functional components, and the logic functions which need to be incorporated in the selected components defined, the logic design phase begins. The general design flow is shown in figure 1. A pLSI or ispLSI design may be implemented from a number of design environments: including pLSI/ispLSI Development System (pDS), pDS+ ABEL, pDS+ Viewlogic and pDS+ LOG/iC

Figure 1. General Design Flow



These design environments offer various levels of design implementation from logic entry through programming the device. They support a variety of user interfaces and entry methods including: MS Windows GUI, Data I/O ABEL HDL or VHDL, Viewlogic Viewdraw/Viewsynthesis and the ISDATA LOG/iC Design System. The design flows using these development software systems are shown in figures 2, 2a, 2b and 2c.

Design Entry

The pDS software allows the user to manually partition the logic to control design fit and performance. Using the MS Windows environment, logic functions are placed into Generic Logic Blocks (GLBs) and I/O Cells. This can be done by using the Edit, Cut, Copy, and Paste functions to enter Boolean equations and/or pre-defined functions from the Lattice Macro or user libraries.

In addition to Boolean design entry, the pDS+ABEL HDL format allows high-level descriptions of counters, adders, comparators, etc. The ABEL language also supports state machines, truth tables and case constructs for behavioral

design implementations. ABEL also accepts VHDL as a high level language input. The Lattice-ABEL interface allows many existing PLD designs to be easily integrated and converted into a pLSI or ispLSI devices.

For standard CAE schematic designs, the pDS+Viewlogic software provides support for graphical and hierarchical logic implementations using the Lattice library of primitives and macros. The Viewlogic interface also allows easy integration of system or user-created functions into a hierarchical schematic using a top-down or bottom-up design methodology. Additionally, Viewsynthesis offers VHDL capability to round out the design entry process.

Design Verification

Verification using the pDS software is accomplished in two steps after logic has been placed. First, each cell may be individually verified to ensure that the minimized logic will fit into the GLB architecture. After all GLB and I/O cells are incrementally checked, the entire design is then verified to ensure that all nets have proper sources and destinations.

Because the advanced pDS+ tools perform automatic partitioning, design verification is done at a higher-level (pre-partitioned). In the ABEL environment, the Compile (ahdl2pla) function performs the syntax and design rule checks. After the Compile phase, the Optimize (plaopt) function (optionally) minimizes the design.

In the pDS+Viewlogic environment, pre-partitioned design verification is performed by the Design Analyzer which ensures the logic conforms to the Lattice design rules.

Partitioning

Partitioning using the pDS software is done by the user as part of the design entry process. The advanced pDS+ABEL, pDS+ Viewlogic and pDS+ LOG/iC tools incorporate Lattice's automatic partitioner which accepts converted data from designs entered in ABEL, Viewlogic and LOG/iC respectively. Lattice specific attributes for design entry are available to guide the partitioner in order to optimize usage of device features and performance.

Place and Route

All Lattice design tools offer automatic place and route. This entails placement of GLB and IOC logic and then routing (or interconnecting) the source signals to their

pLSI and ispLSI Design Flow

destinations. In the pLSI and ispLSI devices, the Global Routing Pool (GRP) provides fast interconnects from external inputs and GLB feedbacks to the GLB inputs. The Output Routing Pool (ORP) provides flexible interconnects from GLB outputs to external pins. To take advantage of the architectural features, Lattice offers two different routers, Fast and Strong. The Fast router utilizes quick algorithms to route most designs. The more comprehensive Strong router is used to route more complex designs.

Post-route Simulation

After place and route, a netlist for full timing and function simulation may be passed to the Viewsim simulator. Viewsim supports simulation using both textual and graphical input and interfaces. Board and system level simulation models are also available from Logic Modeling Corporation.

Documentation

Report files, containing partitioned equations and pin-out information, may be generated for routed or un-routed designs. The pDS software can also generate reports with post-route maximum timing delays. In addition, the design can be exported in an Electronic Design Interchange Format (EDIF). This supports design interfaces to standard third-party CAE tools.

Device Programming

Programming information is generated on a routed design by the FuseMap Generator for a specific pLSI and ispLSI device. It is an ASCII file written in the JEDEC format. Using the pDS+ ABEL software, the user may optionally append test vectors onto the JEDEC file. This allows post-programming functional test on the actual device.

Two programming methods are used to program the pLSI and ispLSI devices. The first method uses the Device Programming Mode for both types of devices. This method facilitates device programming support from third-party vendors. The second method uses the Lattice In-System Programming Mode and applies to the ispLSI family of devices.

Both methods of device programming allow the user to program and read back the fuesmap from the programmed device for verification (if the security cell has not been set).

Figure 2. pDS Design Flow

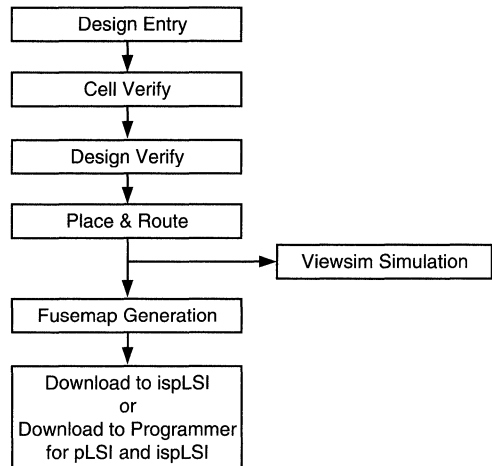


Figure 2a. pDS+ ABEL Design Flow

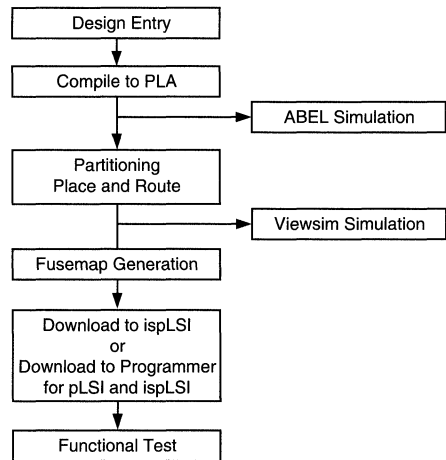


Figure 2b. pDS+ Viewlogic Design Flow

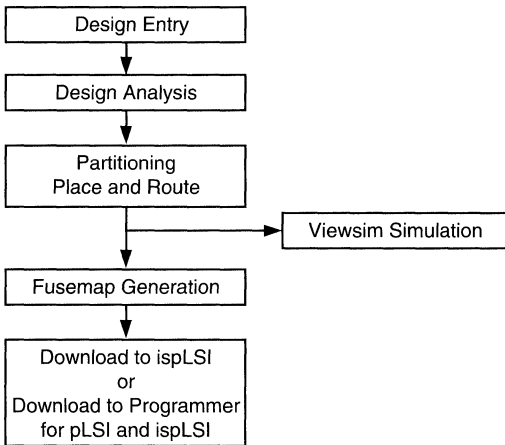
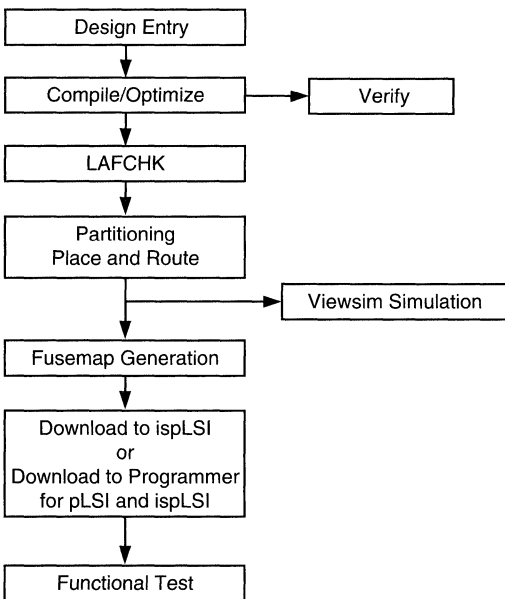


Figure 2c. pDS+ LOG/iC Design Flow



Notes

Features

- **pLSI[®] and ispLSI[™] Development System**
 - Supports pLSI and ispLSI 1000, 2000 and 3000 Families
- **Design Entry with Easy-to-Use Windows[™] Environment**
 - ABEL-Like Boolean Equation Entry
 - Logic Macro Entry with over 275 "TTL-Like" Macros
 - Manual Device Partitioning Ensures Tight Control of Performance and Utilization
- **Fast Design Compilation**
 - Efficient Design Optimization & Minimization
 - "Hands Free" Automatic Place and Route
 - Fast Route Option for Quick Turnaround
 - Strong Route Option for Comprehensive and Optimized Routing
 - Predictable Performance
- **Complete Design Verification**
 - Functional and Timing Simulation Option Using Viewsim
- **Industry Standard JEDEC Programming File Generation**
 - Standard JEDEC Device Fusemap
- **Optional isp Engineering Kit (Model 100)***
 - PC Compatible Programmer for Engineering Use
 - Supports Entire ispLSI Device Family
 - Download to Programmer Circuit Board
- **Runs on 386/486/Pentium IBM-Compatible PC Under Windows[™] Environment**

*Not intended for production programming

Introduction

The pDS software is a comprehensive design package for the Lattice pLSI and ispLSI device families giving full design entry and device implementation capabilities under the Windows design environment. The pDS software provides the best solution for high performance designs which require direct control of the logic implementation. It offers designers complete control over the performance and utilization of the device. The pDS software allows designers to quickly move from concept to a programmed logic device.

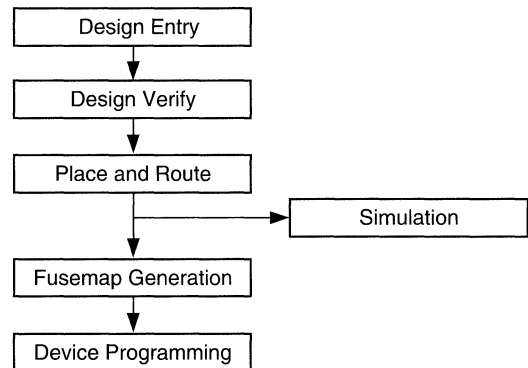
The pDS software also offers a simulation option for full functional and timing simulation of designs using Viewlogic's Viewsim software.

pDS Software

Using the pDS software, designs can be defined completely using simple Boolean equations and "TTL-like" logic macros. Automated design capabilities shorten design cycles allowing designers to explore several design solutions before deciding on the one that provides the best solution.

Designs can be entered in two ways: either through the integrated edit windows within the pDS software, or by using a standard ASCII text editor to create a design file that can be imported into the pDS environment. The Lattice Place and Route software automatically places the logic and routes the interconnections. The Fusemap program generates a fuse file which can then be downloaded into a device programmer or directly to a Lattice ispLSI device (see figure 1).

Figure 1. pDS Design Flow



Design Entry

pDS software offers an easy to use interface as shown in figure 2. Designers can quickly enter the design into

GLBs and I/O cells through this interface. An example of an edit window is shown in figure 3. Tables 1, 2 and 3 provide a condensed list of the different operations which are supported in the pDS software.

Figure 2. User Interface

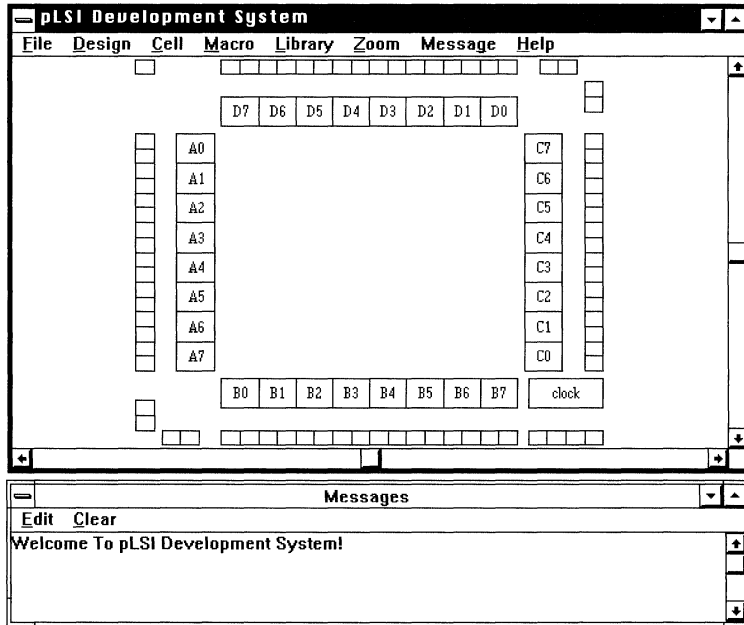


Figure 3. Sample Edit Window Illustrating Boolean Equations and Macros

```
SIGTYPE CO_P OUT;
SIGTYPE C1 REG OUT;
XOR4 (par, D1, D2, D3, D4)
EQUATIONS
    CO_P = CO_0 & CO_1 # CO_2;
    C1 = C1$$ C0;
    C1.CLK = SYSCLK;
END;
```

The following summarizes the pDS software keywords, operators and dot extensions used.

Table 1. Keywords

Keyword	Description
CONSTANT	Assigns a value to a signal
SET	Assigns a label to a group of signals
SIGTYPE	Assigns specific attributes to a GLB output
CRIT	Used for the 4 product term bypass
XPIN	Identifies external signal in the I/O cell
LOCK	Locks an I/O cell to a pin
EQUATIONS	Beginning of the Boolean description of the logic in a GLB
//	The text that follows is a comment

Table 2. Operators

Operator	Description
=	Assignment
!	Inversion
\$\$	Hardware exclusive OR
&	AND
#	OR
\$	Exclusive OR
!\$	Exclusive NOR

Table 3. Dot Extensions

Extension	Description
.D	Identifies the signal as the D input
.Q	Identifies the signal as the Q output
.RE	Identifies the product term reset signal for the GLB
.CLK	Identifies the system clock for the GLB
.PTCLK	Identifies the product term clock for the GLB
.OE	Identifies the output enable signal for the I/O cells within the megablock

The pDS software offers an extensive selection (over 275) of TTL-like macros. These macros enable the design engineer to use familiar pre-defined functions to build a design. Table 4 shows a summary of the available macros in the pDS software.

Table 4. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	11
I/Os	31
Flip-Flops	25
Arithmetic	28
Counters	66
Shift Registers	15
MUX/DEMUX	34
Miscellaneous	25

Logic Optimization

The pDS software provides extensive design rule checking during the optimization and fitting process. After the design has been checked, the software initiates logic minimization to reduce the number of product terms needed.

Automatic Place and Route

The pDS software provides an automatic place and route routine which eliminates the need for manual routing and provides a quicker design cycle time. The router automatically generates pinouts based on an optimal design implementation or it can use a user defined pinout. There are two routing options:

- Fast Route
- Strong Route

The Fast Route option performs quick place and route to reach the debugging stage sooner. The Strong Route option performs a comprehensive routing search to maximize device resource utilization and ensures efficient design implementation. With the Strong Route option, small design changes can generally be performed without expensive PC board rework.

Incremental place-and-route capability allows last-minute logic updates to be implemented without design pin-out changes.

Post Route Simulation

Complete post route design verification can be performed using the optional Viewsim timing simulator.

Fusemap Generation

The Lattice Fusemap generation module outputs the file containing the fuse pattern used to implement the logic in the device. A security feature offers protection of proprietary designs from unauthorized duplication.

Device Programming

The pDS software supports two ways of programming devices. The designer can program the parts themselves through the In-System Programming option or download the file to a third-party device programmer (shown in table 5).

In-System Programming allows the devices to be programmed without removing them from the system board. A download cable is used to transfer the bit stream and programming instructions (called ispSTREAM) from the pDS software to the target system.

Table 5. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

System Requirements

- 386/486/Pentium IBM Compatible PC
- MS DOS Version 3.3 or Later
- MS Windows Version 3.1 or Later
- 4 MB RAM and 10 MB Hard Disk Space
- Parallel Printer Port for Software Key
- VGA or Higher Resolution Display
- Mouse (Windows Compatible)

isp Engineering Kit Ordering Information

- Kit Contains Programming Module (Base Unit), Download Cable, A/C Adapter, Socket Adapters and
- One ispLSI Device Sample Included per Adapter

For more information on specific devices, please refer to the isp Engineering Kit data sheet.

Product Code	Description
pDS4102-PM	Model 100 Universal Programming Module

Technical Support Assistance

- Lattice Hotline: 1-800-LATTICE (Domestic)
- Lattice Hotline: 1-408-428-6414 (International)
- Lattice BBS: 1-408-980-9814
- email: applications@lattice.com

Warranty/Update Service

- 90 Day Warranty on Disk Media
- One year of Maintenance Support Included
- Annual Maintenance Agreement Available
- 90 Day Warranty on isp Engineering Kit

pDS Ordering Information

Product Code	Description
pDS1101-STD/PC1	pLSI and ispLSI Development System supports 1000 and 2000 Family devices
pDS1101-3UP/PC1	pLSI and ispLSI Development System Upgrade to add support fo 3000 Family devices
pDS1101-ULT/PC1	pLSI and ispLSI Development System supports 1000, 2000 and 3000 Family devices
pDS1101M-STD/PC1	pDS1101-STD/PC1 Annual Maintenance Renewal
pDS1101M-ULT/PC1	pDS1101-ULT/PC1 Annual Maintenance Renewal
pDS3302-PC1	Viewlogic Viewsim Timing & Functional Simulator
pDS1102-PC1	Viewlogic Viewsim Simulation Libraries and Interface Files

Features

- pLSI® and ispLSI™ Development System
 - Supports All pLSI and ispLSI 1000, 2000 and 3000 Families
- Design Entry Using ABEL and VHDL-Direct™
 - Design Verification Using ABEL Functional Simulation
 - Lattice Fitter for Design Synthesis
 - Optional Timing Simulation Using Viewlogic Viewsim
- Supports Viewlogic ViewPLD
- Integrated Development Environment for Mixed-Mode Design Entry
 - ABEL Hardware Description Language (AHDL) or VHDL Syntax Including Boolean Equations, Truth Tables and State Machines
 - Graphical Menu Driven User Interface
- Lattice pDS+ ABEL Fitter
 - Automatic Device Fitter Ensures High Utilization and Performance
 - Efficient Design Optimization & Minimization
 - Automatic Partitioning with High Utilization
 - "Hands Free" Automatic Place and Route
 - Fast Route Option for Quick Turnaround
 - Strong Route Option for Comprehensive and Optimized Routing
 - Predictable Performance
- Industry Standard Programming File Generation
 - Standard JEDEC Device Fusemap
 - Standard JEDEC Device Test Vectors
- Optional isp Engineering Kit*
 - Programmer for Engineering Use
 - Model 100 for PC
 - Model 200 for Sun Workstation
 - Supports All ispLSI Device Families
 - Download to Programmer or Circuit Board
- PC and Sun Workstation Design Platforms
 - PC - 386/486/Pentium IBM Compatible PC
 - Sun Workstation - Sun SPARC 4

*Not intended for production programming

Introduction

The pDS+ ABEL software from Lattice Semiconductor offers a powerful solution to fit high-density logic designs into Lattice's pLSI and ispLSI devices.

Design entry is made simple by using ABEL software from Data I/O together with the pDS+ ABEL Fitter for design implementation. The Lattice pDS+ ABEL software offers high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

Data I/O ABEL

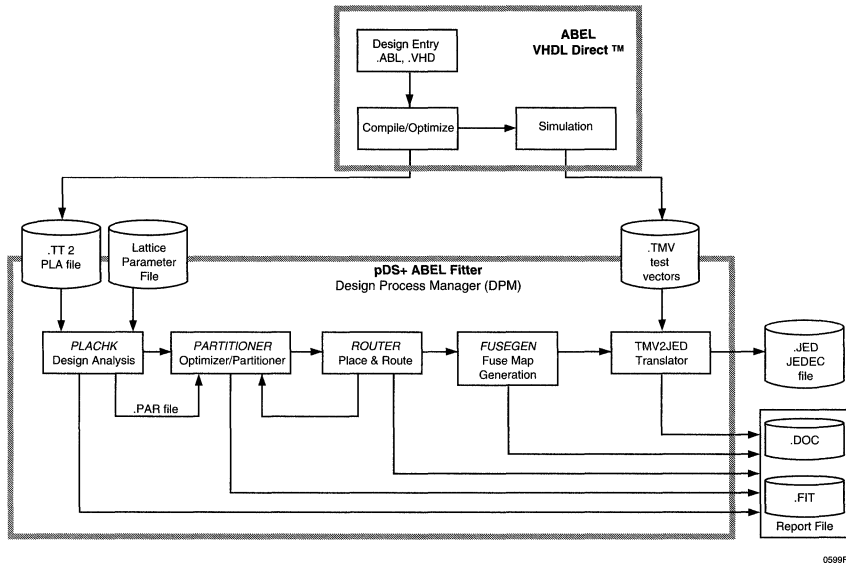
The easy-to-use, menu-driven ABEL software packages provide a complete pre-fit design environment. Using the ABEL Hardware Description Language (AHDL) from DATA I/O Corporation or the IEEE standard VHDL, complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or other HDL descriptions. The HDL syntax allows design creation without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation as easy as clicking a mouse button. Synario will support schematic entry and additional features.

pDS+ ABEL Software

The Lattice pDS+ ABEL Fitter for pLSI and ispLSI devices is completely integrated within the ABEL Software environment. The Lattice Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation with optional test vectors, in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization. The pDS+ ABEL Fitter performs the following functions during design synthesis:

- Design Optimization and Logic Minimization
- Automatic Partitioning
- Automatic Place and Route
- Design Parameter Control
- Fusemap Generation

Figure 3. pDS+ ABEL Fully Integrated Design Environment



Design Optimization and Logic Minimization

The pDS+ ABEL Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, compressing multiple level logic into two level logic, and utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ ABEL Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ ABEL Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or uses user assigned pinouts. It offers two routing options:

- Fast Route
- Strong Route

The Fast Route option allows quick place and route for fast debugging of designs. The Strong Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is small design changes don't result in expensive PC Board rework.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ ABEL Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using "Property" statements in the ABEL design file. These controls fall into two categories:

- Performance and Utilization Control
- Design Implementation Control

Performance and Utilization Control

Special properties can be passed to the pDS+ ABEL Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

- MAX_DELAY Specifies maximum level of (GLB's) delay
- PRESERVE Maintains a net as GLB output
- SCP/ECP Defines critical paths to reduce delays
- EFFORT Runs four optimization strategies and uses the best to implement the design
- CRIT Instructs router to use the faster Output Routing Pool Bypass
- SNP/ENP Defines logic paths for no logic minimization
- SAP/EAP Defines asynchronous paths to prevent signal duplication
- LXOR2 Defines nets to use the internal hard XOR for speed (Macro library element)

Design Implementation Control

pDS+ ABEL Design implementation controls are used for changing such design parameters as security, clocking, etc. Some of the implementation controls are:

- MAX_GLB_IN Controls maximum number of inputs to a GLB
- AVG_GLB_IN Specifies average number of inputs to a GLB
- FASTCLK Lets you assign a product term clock to use the Fast Clock Distribution network to clock all or desired sets of registers
- REGTYPE Specifies register placement either in an I/O Cell or GLB
- PULLUP Specifies internal pull-up resistors on all or unused I/Os
- SECURITY Sets the device security cell to prevent unauthorized fusemap read back
- ISP Instructs Router to reserve in-system programming pins

- ISP_EXCEPT_Y2 Reserves all ISP pins except Y2
- Y1_AS_RESET Uses Y1 clock pin on ispLSI 1016/pLSI 1016 as a global reset pin
- LOCK Lets you lock I/O signals to specific device pins.

Parameter File

The pDS+ ABEL Fitter provides a parameter file feature which helps designers eliminate guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ ABEL Fitter also provides post-route equations showing exactly how the design is implemented in the selected device.

Fusemap Generation

The pDS+ ABEL Fitter generates a device fusemap in standard JEDEC format. A security feature gives protection of proprietary designs from unauthorized duplication. The fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

Design Verification

The pDS+ ABEL software provides functional simulation of all pLSI and ispLSI designs using the built-in ABEL functional simulator. The simulation test vectors can be combined into the JEDEC file for device testing in a programmer.

Complete post route design verification can also be performed using the optional Viewsim timing simulator. The pDS+ ABEL software generates the "sim" file required for Viewsim simulation. Simulation libraries are available from Lattice for both PC and Sun platforms. The Viewlogic Viewsim simulation is available from Lattice for the PC platform.

System Requirements (PC Platform)

- 386/486/Pentium IBM Compatible PC
- MSDOS Version 3.3 or Later
- 16 MB RAM with 10MB Hard Disk Space
- ABEL 4.1 or Later
- Parallel Printer Port for Software Key

System Requirements (Sun Platform)

- Sun Sparc 4
- Sun OS Version 4.x
- Open Windows 3.0
- ABEL 4.1 or Later
- 16 MG RAM with 100 MB Hard Disk Space
- 3 Button Mouse

Technical Support Assistance

Lattice Hotline: 1-800-LATTICE (Domestic)
 Lattice Hotline: 1-408-428-6414 (International)
 Lattice BBS: 1-408-980-9814
 email: applications@lattice.com

pDS+ ABEL Ordering Information

Product Code	Description
pDS2102-PC1	pDS+ ABEL Fitter for PC
pDS2102-SN1	pDS+ ABEL Fitter for Sun Workstation
pDS2102M-PC1	pDS+ ABEL Fitter Maintenance
pDS2102M-SN1	pDS+ ABEL Fitter Maintenance
pDS3302-PC1	Viewlogic Viewsim Timing and Functional Simulator
pDS1102-PC1	Viewlogic Viewsim Timing and Functional Simulation Libraries and Interface Files (For customers who already own Viewlogic Viewsim)

Note: Contact Lattice for availability of pDS+ ABEL support for Synario and pLSI & ispLSI 2000 and 3000 Families.

Programmer Support

All devices in the Lattice ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed either via the isp Engineering Kit or by an on-board microprocessor.

All Lattice ispLSI and pLSI devices can be programmed using third-party PLD programmers. These devices are

currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

High Pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

isp Engineering Kit Ordering Information

- Kit Contains Programming Module (Base Unit), Download Cable, A/C Adapter, Socket Adapters and
- One ispLSI Device Sample Included per Adapter

Product Code	Description
pDS4102-PM	Model 100 Universal Programming Module (for PC)
pDS4102-WS	Model 200 Universal Programming Module (for Sun)

Warranty/Update Service

- 90 Day Warranty on Disk Media
- One year Maintenance Support Included with Purchase
- Annual Maintenance Agreement Available
- 90 Day Warranty on isp Engineering Kit



pDS+™ Viewlogic Software

Features

- **pLSI® and ispLSI™ Development System**
 - Supports All pLSI and ispLSI 1000 Devices
 - Support for 2000 and 3000 Families Under Development
- **Integrated Workview 4.x, Pro Series, Workview Plus or Powerview Development Environment for Design Entry**
 - Schematic Entry
 - Over 300 "TTL-like" Macros
 - Viewsynthesis VHDL Language Entry
 - Graphical Menu Driven User Interface
 - Command Line Driven User Interface
- **Lattice pDS+ Viewlogic Fitter**
 - Automatic Device Fitter Ensures High Utilization and Performance
 - Efficient Design Optimization & Minimization
 - Automatic Partitioning
 - "Hands Free" Automatic Place and Route
 - Fast Route Option for Quick Turnaround
 - Strong Route Options for Comprehensive and Optimized Routing
 - Predictable Performance
- **Complete Design Verification**
 - Using Viewsim Timing Simulator
- **Industry Standard Programming File Generation**
 - Standard JEDEC Device Fusemap
- **Optional isp Engineering Kit***
 - Programmer for Engineering Use
 - Model 100 for PC
 - Model 200 for Sun Workstation
 - Supports All ispLSI Device Families
 - Download to Programmer or Circuit Board
- **PC and Sun Workstation Design Platforms**
 - PC - 386/486/Pentium IBM Compatible PC
 - Sun Workstation - Sun Sparc 4

*Not intended for production programming

Introduction

The pDS+ Viewlogic Software from Lattice Semiconductor now offers a powerful solution to fit high density logic designs into Lattice's pLSI and ispLSI devices.

Design entry and implementation is made simple using the software environments from Viewlogic Corporation. Viewlogic has a number of software products of various names. The new Pro Series of products will be supported by Lattice in 1994. For simplicity the tools are referred to as Viewdraw, Viewsim and Viewsynthesis. The Lattice pDS+ Viewlogic software supports high level, device independent design entry together with efficient logic compilation, delivering the most complex designs in the shortest time possible.

Viewlogic's Software

Viewlogic supports schematic entry using Viewdraw. Viewdraw lets you create designs without regard to any specific device dependencies. Viewdraw offers advanced features such as cut and paste, unlimited zoom and pan functions, automatic symbol generation as well as many other features to streamline and speed-up the design and verification process. Viewsynthesis supports VHDL language entry as well. The integrated design environment supports an optional timing simulator (Viewsim) so designs can be fully simulated before device programming. The Menu-driven environment makes design implementations as easy as a single click of the mouse button. The pDS+ Viewlogic design environment also offers the user multi-window operation, allowing schematic, simulator and waveform (Viewwave) windows to be opened concurrently. Results can also be dynamically back annotated to the schematic for design verification.

The Viewwave software is a graphical editor for creating simulation input stimulus as well as analyzing waveforms. This graphical editor/analyzer also increases designer productivity through its speed and ease-of-use.

pDS+ Viewlogic Software

The Lattice pDS+ Viewlogic Fitter for pLSI and ispLSI devices is completely integrated within the Viewlogic

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pDS+ Viewlogic Software

environment. The Lattice pDS+ Viewlogic Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation. The pDS+ Viewlogic software comes complete with a library of over 300 TTL-like macros to simplify design entry. Extensive top level design control is provided for design implementation optimized for speed and/or high device resource utilization. The pDS+ Viewlogic Fitter performs the following functions during design synthesis:

- Design Optimization and Logic Minimization
- Automatic Partitioning
- Automatic Place and Route
- Design Parameter Control
- Fusemap Generation

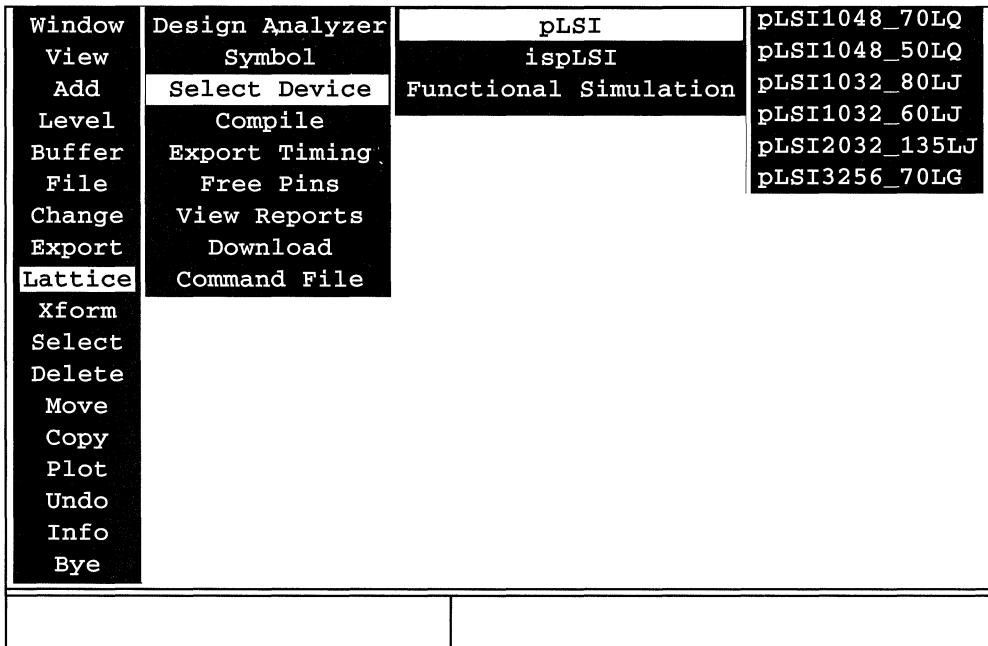
pDS+ Viewlogic Macro Library

The pDS+ Viewlogic software offers an extensive selection (over 300) of TTL-like macros. These macros enable the design engineer to use familiar predefined functions to build a design. Table 1 shows a summary of the available macros in the pDS+ software.

Table 1. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	22
Counters	65
Shift Registers	15
Miscellaneous	45

Figure 1. pDS+ Viewlogic PC Design Interface



0478E

Figure 2. pDS+ Viewlogic Integrated Design Environment

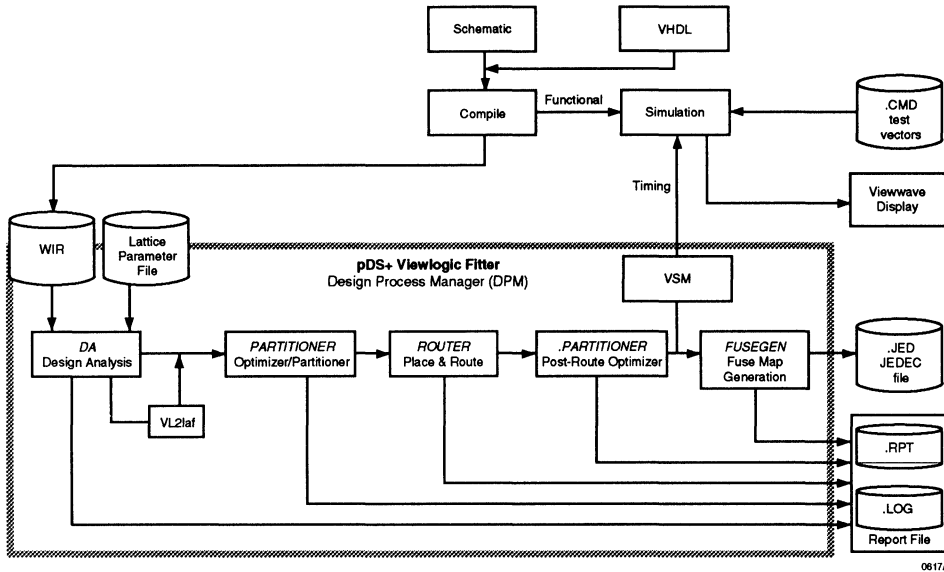
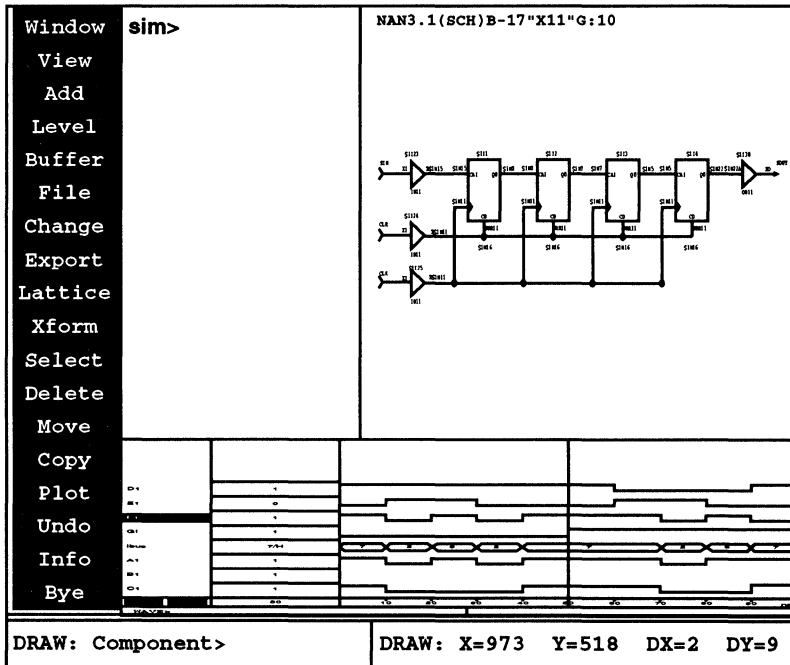


Figure 3. pDS+ Viewlogic Multi-Window PC Design Environment



pDS+ Viewlogic Software

Design Optimization and Logic Minimization

The pDS+ Viewlogic Fitter uses proprietary logic synthesis algorithms targeted for device-specific features. The fitter performs a thorough design optimization, compressing multiple level logic into two level logic, and utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ Viewlogic Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ Viewlogic Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on optimal design implementation or uses user-assigned pinouts. It offers two routing options:

- Fast Route
- Strong Route

The Fast Route option allows quick place and route for fast debugging of designs. The Strong Route option performs comprehensive routing to maximize device resource utilization and ensures efficient design implementation. The result is small design changes do not result in expensive PCB rework.

Design Parameter Control

The pDS+ Viewlogic Fitter offers extensive design parameter control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "Attributes" in the

Viewdraw design file. These controls fall into two categories:

- Performance and Utilization Control
- Design Implementation Control

Performance and Utilization Control

Special attributes can be passed to the pDS+ Viewlogic Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

MAX_DELAY	Specifies maximum levels of (GLBs) delay
PRESERVE	Maintains a net as GLB output
SCP/ECP	Defines critical paths to reduce delays
EFFORT	Runs four optimization strategies and uses the best to implement the design.
CRIT	Instructs router to use the faster Output Routing Pool Bypass
SNP/ENP	Defines logic paths for no logic minimization
SAP/EAP	Defines asynchronous paths to prevent signal duplication
LXOR2	Defines nets to use the internal hard XOR for speed (This is a macro library element)

Design Implementation Control

pDS+ Viewlogic Design implementation controls are used for changing such design parameters as security, clocking and pin locking. Some of the powerful implementation controls are:

MAX_GLB_IN	Controls maximum number of inputs to a GLB
AVG_GLB_IN	Specifies average number of inputs to a GLB
FASTCLK	Assigns a clock to the Fast Clock Distribution network to clock all or desired sets of registers
REGTYPE	Specifies register placement either in an I/O Cell or GLB
PULLUP	Specifies internal pull-up resistors on all or unused I/Os
SECURITY	Sets the device security cell to prevent unauthorized fusemap read back

- ISP Instructs Router to reserve device in-system programming pins
- ISP_EXCEPT_Y2 Reserves all ISP pins except Y2
- Y1_AS_RESET Uses Y1 clock pin on ispLSI and pLSI 1016 as a global reset pin
- LOCK Lets you lock I/O signals to specific device pins

Parameter File

The pDS+ Viewlogic Fitter provides a parameter file feature which helps designers eliminate the guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using all of the design implementation controls in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

The pDS+ Viewlogic Fitter also provides a post route design file for optional timing simulation.

Design Verification

The pDS+ Viewlogic software offers complete post route design verification using the optional Viewsim timing simulator. The pDS+ Viewlogic Fitter generates the "wire" file required for Viewsim simulations, and generates a "sim" file which can be used in the Viewsim simulator, or other design platforms. The Viewlogic simulation libraries and the Viewsim simulator are available from Lattice.

Fusemap Generation

The pDS+ Viewlogic software generates a device fusemap in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

- 386/486/Pentium IBM Compatible PC
- MS DOS Version 3.3 or Later
- 16 MB RAM with 40 MB Hard Disk Space
- Workview 4.1 or Later
- Serial Port for Mouse
- 3 Button Mouse (Mouse Systems Compatible)
- Parallel Printer Port for Software Key

System Requirements (Sun Platform)

- Sun Sparc 4
- Sun OS Version 4.x
- Open Windows 3.0
- Workview 4.1 or Powerview 5.0 or Later
- 16 MB RAM with 100 MB Hard Disk Space
- 3 Button Mouse

Technical Support Assistance

- Lattice Hotline 1-800-LATTICE (Domestic)
- Lattice Hotline 1-408-428-6414 (International)
- Lattice BBS 1-408-980-9814

Programmer Support

All devices in the Lattice ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed either via the isp Engineering Kit or by an on-board microprocessor.

All Lattice ispLSI and pLSI devices can be programmed using third-party programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

pDS+ Viewlogic Software

pDS+ Viewlogic Ordering Information

Software Products

pDS1102-PC1	Viewlogic Viewsim and Viewdraw Libraries and Interface Files (Direct Viewlogic Customers on the PC)
pDS1102-SN1	Viewlogic Viewsim and Viewdraw Libraries and Interface Files (Direct Viewlogic Customers on the Sun)
pDS1103-PC1	Viewlogic Viewsim and Viewdraw Libraries and Interface Files (Customers of Actel or Other FPGA Suppliers on the PC)
pDS1104-PC1	Viewlogic Viewsim and Viewdraw Libraries and Interface Files (Xilinx Customers on the PC)
pDS1301-PC1	Viewlogic Viewdraw Schematic Editor
pDS2101-PC1	pDS+ Viewlogic Fitter for (PC)
pDS2101-SN1	pDS+ Viewlogic Fitter for (Sun)
pDS3302A-PC1	pDS+ Viewlogic Viewsim Functional and Timing Simulator (PC) for Current Viewlogic Users
pDS3302-PC1	pDS+ Viewlogic Viewsim Functional and Timing Simulator (PC) for New Viewlogic Users

Maintenance Agreements

pDS1102M-PC1	Viewlogic Viewsim and Viewdraw Libraries and Interface Files (Lattice Viewsim Library Products) (pDS1102-PC1)
pDS1102M-SN1	Viewlogic Viewsim and Viewdraw Libraries and Interface files (pDS1102-SN1)
pDS1301M-PC1	Viewlogic Viewdraw Schematic Editor (pDS1301-PC1)
pDS2101M-PC1	pDS+ Viewlogic Fitter (pDS2101-PC1)
pDS2101M-SN1	pDS+ Viewlogic Fitter (pDS2101-SN1)
pDS3302M-PC1	pDS+ Viewlogic Viewsim Functional and Timing Simulator (For all Lattice Viewsim Simulation Products) (pDS3302-PC1)

isp Engineering Kit

pDS4102-PM	Model 100 Universal Programming Module for the PC: Universal Programming Module,(2) 8 wire Download cables, AC/DC Power Supply Converter, 25-Pin Parallel Port Adapter
pDS4102-WS	Model 200 Universal Programming Module for the Sun

Warranty / Update Service

- 90 Day Warranty on Disk Media
- One year of Maintenance Support Included with Purchase
- Annual Maintenance Agreement Available
- 90 Day Warranty on isp Engineering Kit

Features

- **pLSI® and ispLSI™ Development System Support**
 - pLSI 1016, 1024, 1032
 - ispLSI 1016, 1024, 1032
 - Support for 2000 Family Under Development
- **Design Entry Using ISDATA LOG/iC PLUS or PERFECT and LOG/iC ODC**
 - Design Verification Using LOG/iC Functional Simulation
 - Lattice Fitter for Design Synthesis
 - Optional Timing Simulator
- **Integrated Development Environment for Mixed-Mode Design Entry**
 - ISDATA LOG/iC Syntax Including Boolean Equations, Truth Tables and State Machines, Optional VHDL, Schematics or Graphical State Machine Entry
 - Graphical Menu Driven User Interface
- **Lattice pDS+ LOG/iC Fitter**
 - Automatic Device Fitter Ensures High Utilization and Performance
 - Efficient Design Optimization & Minimization
 - Automatic Partitioning with High Utilization
 - "Hands Free" Automatic Place and Route
 - Fast Route Option for Quick Turnaround
 - Strong Route Option for Comprehensive and Optimized Routing
 - Predictable Performance
- **Industry Standard Programming File Generation**
 - Standard JEDEC Device Fusemap
- **Optional isp Engineering Kit***
 - Programmer for Engineering Use
 - Supports ispLSI 1016, 1024, & 1032
 - Model 100 for PC
 - Download to Programmer or Circuit Board
- **Runs on 386/486/Pentium IBM Compatible PC**

*Not intended for production programming

Introduction

The pDS+ LOG/iC software from Lattice Semiconductor offers a powerful solution to fit high density logic designs into Lattice's pLSI and ispLSI devices.

Design entry is made simple by using LOG/iC software from ISDATA GmbH together with the pDS+ LOG/iC Fitter for design implementation. The Lattice pDS+ LOG/iC software offers high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

ISDATA LOG/iC

The easy to use, menu driven ISDATA LOG/iC software package provides a complete design environment. Using the LOG/iC program package, complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or other LOG/iC design. The LOG/iC syntax creates designs without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation simple to use.

pDS+ LOG/iC Software

The Lattice pDS+ LOG/iC Fitter for pLSI and ispLSI devices is completely integrated within the LOG/iC software environment. The Lattice Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation with optional test vectors in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization. The pDS+ LOG/iC Fitter performs the following functions during design synthesis:

- Design Optimization and Logic Minimization
- Automatic Partitioning
- Automatic Place and Route
- Design Parameter Control
- Fusemap Generation

Figure 1. pDS+ LOG/iC Design Interface

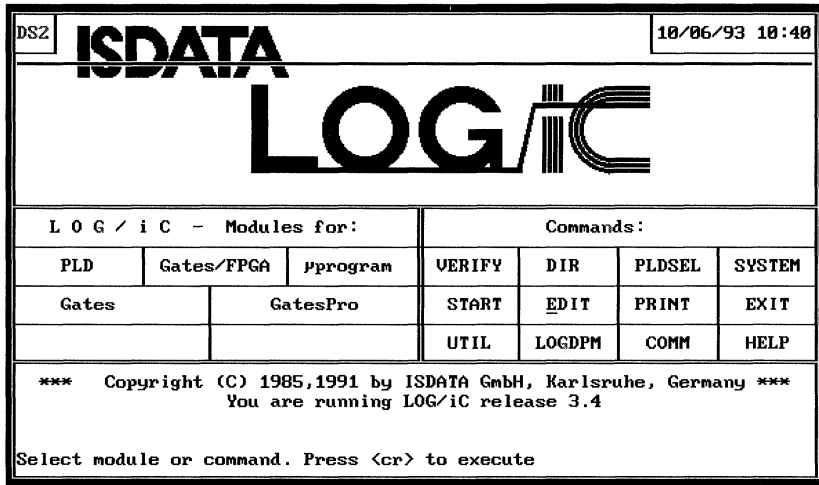
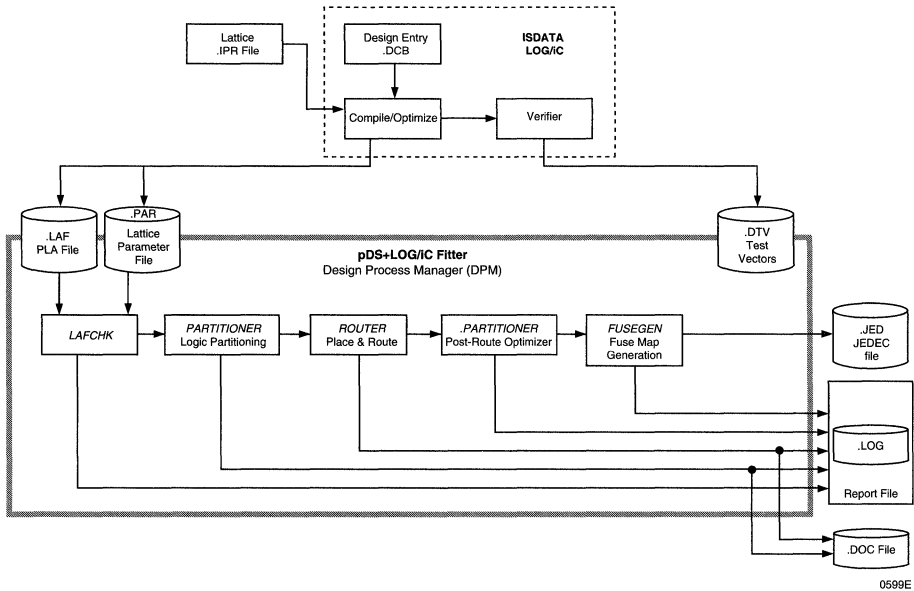


Figure 2. pDS+ LOG/iC Fully Integrated Design Environment



Design Optimization and Logic Minimization

The pDS+ LOG/iC Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, compressing multiple level logic into two level logic, and utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ LOG/iC Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ LOG/iC Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features, such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. Common sub-expressions are extracted, and unused registers are eliminated. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or uses user assigned pinouts. It offers two routing options:

- Fast Route
- Strong Route

The Fast Route option allows quick place and route for fast debugging of designs. The Strong Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is small design changes don't result in expensive p.c. board rework.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ LOG/iC Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using "Property" statements in the Lattice Property file (.IPR). These controls fall into five categories:

- Fitter Statements
- Option Statements
- Net Statements
- Path Statements
- Sym Statements

Fitter Statements

Special properties can be passed to the pDS+ LOG/iC Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

PART	Determines device type to be used
EFFORT/TRY	Runs four optimization strategies and uses the best to implement the design. TRY uses only one of the four strategies, and overrides EFFORT if both are specified
LOCK	Lets you lock I/O signals to specific device pins
MAX_DELAY	Specifies maximum level of (GLBs) delay
AVG_GLB_IN	Specifies average number of inputs to a GLB. Default is 16
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16
FAST/STRONG	Method of routing. Default is STRONG ROUTE Fixed

Option Statements

pDS+ LOG/iC Design implementation controls are used for changing such design parameters as security, pull-ups etc. Some of the implementation controls are:

ISP	Instructs Router to reserve in-system programming pins
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016 only)
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016 as a global reset pin
SECURITY	Sets the device security cell to prevent unauthorized fusemap read back
PULLUP	Specifies internal pull-up resistors on all (ON) or unused I/Os

Net Statements

These properties control how the design is mapped into the specified features of the target device:

CLK 0 - 2	Assigns GLB clock signals
IOCLK 0 - 1	Assigns I/O cell clock signals
FASTCLK	Assigns a product term clock to use any one of the dedicated clock inputs to clock all or desired sets of registers
SLOWCLK	Designate clock to use a product term clock within a GLB
PRESERVE	Prevents logic minimization on specified nodes
CRIT	Specifies Output Routing Pool Bypass Modes for selected duplication

Path Statements

The following properties specify paths in the design that have special fitting requirements:

SAP/EAP	Defines asynchronous paths to prevent signal duplication
SCP/ECP	Defines critical paths to reduce delays
SNP/ENP	Defines logic paths for no logic minimization

Sym Statements

These allow you to choose to place a register in a specific GLB or an I/O cell:

SYM IOC	Register in the I/O cell
SYM GLB	Register in the GLB

Parameter File

The pDS+ LOG/iC Fitter uses a parameter file (.IPR file) feature to help designers optimize the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ LOG/iC Fitter also provides post route equations showing exactly how the design is implemented in the selected device. An optional timing simulator is also available for detailed post route timing simulation of designs using the VERIFY section of the menu.

Fusemap Generation

The pDS+ LOG/iC Fitter generates a device fusemap in standard JEDEC format. The fusemap is automatically produced and inserted in the JEDEC file after a successful route. A security feature gives protection of proprietary designs from unauthorized duplication.

Design Verification

The pDS+ LOG/iC software provides functional simulation of pLSI and ispLSI designs using the optional LOG/iC Functional Design Verifier (FDV). The simulation test program file (.DTP) can be created for device simulation in the VERIFY menu, but the FDV can also be stimulated interactively on the screen.

Full timing simulation is also available using Viewlogic's Viewsim Simulation (available from Lattice).

System Requirements

- 386/486/Pentium IBM Compatible PC**
- MSDOS Version 3.3 or Later
 - 16 MB RAM with 40MB Hard Disk Space
 - 3 1/2" Floppy Disk Drive
 - ISDATA's LOG/iC PLUS or PERFECT and LOG/iC ODC SOFTWARE
 - Parallel Printer Port for Software Key
 - EGA Graphics Monitor or higher

Technical Support Assistance

- Lattice Hotline: 1-800-LATTICE (Domestic)
- Lattice Hotline: 1-408-428-6414 (International)
- Lattice BBS: 1-408-980-9814
- email: applications@lattice.com
- ISDATA Inc. 1-510-531-8553
1-800-777-1202
- ISDATA GmbH: 49-721-751087

Programmer Support

All devices in the Lattice ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed either via the isp Engineering Kit or by an on-board microprocessor.

All Lattice ispLSI and pLSI devices can be programmed using third-party PLD programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

High Pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

pDS+ LOG/iC Ordering Information

Product Code	Description
pDS2103-PC1	pDS+LOG/iC Fitter for PC
pDS2103M-PC1	pDS+LOG/iC Fitter Maintenance
pDS3302-PC1	Viewlogic Viewsim Simulator
pDS3302M-PC1	Viewsim Maintenance
pDS1102-PC1	Viewsim Library

isp Engineering Kit Ordering Information

- Kit Contains Programming Module (Base Unit), Download Cable and A/C Adapter
- One ispLSI Device Sample Included per Adapter

Product Code	Description
pDS4102-PM	Model 100 Universal Programming Module

Warranty/Update Service

- 90 Day Warranty on Disk Media
- One year Maintenance Support Included with Purchase
- Annual Maintenance Agreement Available
- 90 Day Warranty on isp Engineering Kit



isp™ Starter Kit

Starter Set of Software, Hardware, Datasheets and Samples for Lattice ISP Products

Includes

- **Software**
 - pDS1016-PC1 Design Development System for ispLSI 1016 Device
 - ispGAL® Download Software
 - ispGDS™ (Generic Digital Switch) Compiler and Download Software
 - ispCODE™ ANSI C Compiled and Source Programming Software
- **Datasheets**
 - ispLSI 1016 Device Datasheet
 - ispGAL22V10 Device Datasheet
 - ispGDS22/18/14 Device Datasheet
- **Samples**
 - ispLSI 1016-60LJ Device in 44 pin PLCC Package
 - ispGAL22V10B-15LJ Device in 28 pin PLCC Package
 - ispGDS14-7J Device in 20 pin PLCC Package
- **Hardware**
 - ispDOWNLOAD™ Cable

Features

- **Easy to Use Kit Contains Everything Needed for In-System Programmable Device Design-in**
- **Supports Lattice's ispLSI 1016 Device — the Industry's Fastest High Density Programmable Device at 110 MHz**
- **Supports Industry Standard 22V10 Architecture Coupled with Lattice's Innovative In-System Programmable Design Capability**
- **Supports Lattice's New isp Generic Digital Switch for Applications such as Software Driven Hardware Configuration and Multiple DIP Switch Replacement**
- **E²CMOS Technology**

Introduction

The isp Starter Kit is designed to make Lattice's innovative in-system programmable device technology available in a single, complete package. The isp Starter Kit contains all the software, hardware, device samples, and information you need to begin designing with Lattice's ISP products. The ispLSI devices are the fastest High Density Programmable Logic devices in the industry, at 110 MHz, as certified by PREP™ Benchmarks. Lattice's new 7.5ns ispGAL22V10 device has all the advantages of In-System Programmability and maintains the familiar 22V10 architecture and 28-pin PLCC pinout. The ispGDS is Lattice's latest in-system programmable innovation. This new family of devices offers the ability to configure its programmable switch matrix to connect signals arbitrarily between two banks of I/O pins or to force pins to fixed high or low logic states.

In-System Programmability (ISP)

ISP is a Lattice innovation that supports device function programming and reprogramming on the printed circuit board at 5 volts. There are several advantages to in-system programmability: First, it accelerates the system and board level debug process and enables you to define your board layout earlier in the design process. Second, ISP eliminates bent leads caused by extra handling and socket insertions made during the device programming process. Third, systems incorporating ISP are reconfigurable with the devices already soldered to the p.c. board, minimizing board rework time and expense. With this capability your system options are boundless and easier field updates are made possible by downloading a new configuration file via a floppy disk or modem.

ispLSI 1016 and pDS 1016 Software

The ispLSI 1016 device is a fast, high density programmable logic device containing 64 logic registers, 32 Universal I/O pins with input registers, four dedicated input pins, three dedicated clock input pins, and a programmable Global Routing Pool (GRP). The basic logic element of the device is the Generic Logic Block (GLB) which has 18 inputs, a programmable AND/OR/XOR array, and four outputs that may be configured as

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LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.

Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037

1994 Data Book

either combinatorial or registered. Lattice's pDS1016 Design Software is a high performance development environment that runs on IBM compatible 386/486/Pentium PCs. The software has a friendly, efficient, Microsoft Windows Interface which supports familiar Boolean equation entry. pDS1016 features automatic logic Place and Route for quick design implementation. To make designing even easier there is a library of over 200 Logic Macros for fast design entry.

ispGAL22V10 and Download Software

The ispGAL22V10 is the industry's first in-system programmable 22V10 device and offers a fast 7.5ns maximum propagation delay time. The generic architecture provides maximum flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The logic functionality, fusemap, and AC and DC parameters of the ispGAL22V10 are fully compatible with standard bipolar and CMOS 22V10 devices. The 28-pin PLCC package provides the same functional pinout as the standard 22V10 by using the four "No Connect" pins on the 28 pin PLCC for the ISP interface signals.

Designs for the ispGAL22V10 can be compiled by any logic compiler supporting the 22V10 architecture. The ispGAL Download Software takes any 22V10 JEDEC file as input and programs the device in-system, quickly and easily.

ispGDS and Compiler/Download Software

The Lattice ispGDS family is an ideal solution for reconfiguring system signal routing and replacing DIP switches used for feature selection. Each I/O cell can be configured as an input, an inverting or noninverting output, or a fixed TTL high or low output. Any I/O pin in the one bank can be driven by any I/O pin in the opposite bank. A single input can also drive one or more outputs in the opposite bank, allowing a signal, such as a clock, to be distributed to multiple destinations on the board.

The ispGDS Compiler and Download Software is a simple text entry and compilation design tool that produces a standard JEDEC file for device programming.

Ordering Information

Part Number	Description
isp-SK	Lattice isp Starter Kit



Features

- **C-LANGUAGE SOURCE CODE FOR IN-SYSTEM PROGRAMMING OF THE ispLSI FAMILY**
 - Simplifies In-System Programming
 - Pre-Defined Routines for Common Programming Functions
 - Extensively Commented Code Provides Complete Reference
 - Easy Modification Saves Valuable Time
 - Supports Programming of Multiple ispLSI Devices on Individual Boards
- **ACCEPTS PROGRAMMING FILES FROM THE pLSI AND ispLSI DEVELOPMENT SYSTEM (pDS®)**
 - Supports pDS and pDS+™ Software
 - Supports ispLSI 1000, 2000, and 3000 Families
- **PORTABLE TO ANY HARDWARE PLATFORM**
 - Adaptable to Any Hardware Interface
 - UNIX Systems, PCs, Testers, Embedded Systems
 - ANSI-Standard C for Portability
- **GENERATES ispSTREAM™ FORMAT FOR GREATER EFFICIENCY**
 - Bit-packed File Format for Storing JEDEC Fusemap
 - Requires Less Than 1/8 the Storage Space of a Standard JEDEC File
 - Ideal for Use in Embedded Systems, PROMs and EPROMs
 - Includes Checksum To Assure Data Integrity
- **USER ELECTRONIC SIGNATURE (UES) SUPPORTED**
 - Provides Data Storage Area In Device
 - Facilitates User Identification of Program for Secured Devices
 - Automatic Counter Records Number of Programming Cycles
- **EXTENSIVE EXAMPLE FILES**
 - Fast Learning Curve
 - 100% of Library Functions Demonstrated

Introduction

The ispCODE software from Lattice is designed to facilitate in-system programming of ispLSI devices on customer-specific hardware platforms. The ispCODE works with Lattice's pLSI and ispLSI Development System software to give users a powerful, fully integrated tool kit for developing logic designs and programming ispLSI devices "on-the-fly."

After completion of the logic design and creation of a JEDEC file by the pDS or pDS+ software (see figure 1), in-system programming can be accomplished on customer-specific hardware: UNIX systems, PCs, testers, embedded systems (see figure 2). The ispCODE software package supplies specific routines, with extensively commented code, for incorporation into user application programs. These routines provide users with flexible, easy-to-use program modules which support the programming of a single device or multiple devices on a board.

ispCODE Software

The ispCODE software consists of source files containing subroutines for performing all the functions needed to control the programming of Lattice in-system programmable devices (see Table 1). These routines are provided as fully-commented source code for easy inclusion with any software written in the industry-standard C language. This source code library was designed from the ground up to be easily portable to any system that has an ANSI-standard C compiler. The majority of the code is completely independent of the hardware platform and rarely requires modification. All hardware dependent portions of the code are in a separate file, and are easily modified for any hardware system. The code supports the programming of multiple ispLSI devices by controlling the ispEN pins of each device separately, or in a daisy chain configuration.

Example programs are provided to demonstrate the use of each routine. These example programs are designed to enhance readability and understanding. In addition, they provide a practical method of immediately programming devices. By making small changes to the hardware-specific source files and re-compiling the example programs, a complete set of command-line oriented

utilities are created that program, verify, read, and secure devices.

All of the example programs and the hardware-specific code are written to run on IBM PC or compatible microcomputers. The programs use the standard PC parallel printer port to provide the interface to the Lattice device's in-system programming pins (see figure 3). The pinout is compatible with the Lattice isp Engineering Kit Model 100.

Fusemap Storage

All of the ispCODE routines use a bit-packed file format for storing the device pattern information. This bit stream is called an ispSTREAM, and consists of one bit for each of the programmable cells in the devices, plus one byte at the front of the file for a device ID code, and four bytes at the end of the file for a 32-bit checksum. This format provides the most compact means possible for storing the pattern information, requiring less than 1/8 the storage space of a standard JEDEC file. This format is ideal for use in embedded systems, and the storage of ispLSI pattern information in PROMs or EPROMs. Also, using the ispSTREAM format simplifies the programming code, thus reducing the possibility of errors. The following are the ispSTREAM storage requirements for ispLSI 1000 family devices:

Device	Storage Requirement
ispLSI 1016	1933 bytes
ispLSI 1024	3078 bytes
ispLSI 1032	4343 bytes
ispLSI 1048	7233 bytes

There are ispCODE routines for converting JEDEC files to ispSTREAM files, and for converting back to JEDEC files. In addition, ispCODE software includes stand-alone programs called "jedtoisp" and "isptojed" which can be used for converting files. When using the ispCODE routines and the example programs, the JEDEC files are first converted to ispSTREAM format. The ispSTREAM files are then used to do the programming.

User Electronic Signature

The ispCODE library provides routines for accessing the UES (User Electronic Signature), which is a user-accessible data storage area present in all Lattice in-system programmable devices. This area can be used to store information relating to the current configuration of the device or system, and is always readable, even when the functional portions of the devices are secured.

The ispLSI 1000 family devices have the following UES areas available:

Device	UES Area
ispLSI 1016	8 bytes
ispLSI 1024	13 bytes
ispLSI 1032	18 bytes
ispLSI 1048	28 bytes

Figure 1. Using the ispCODE Software

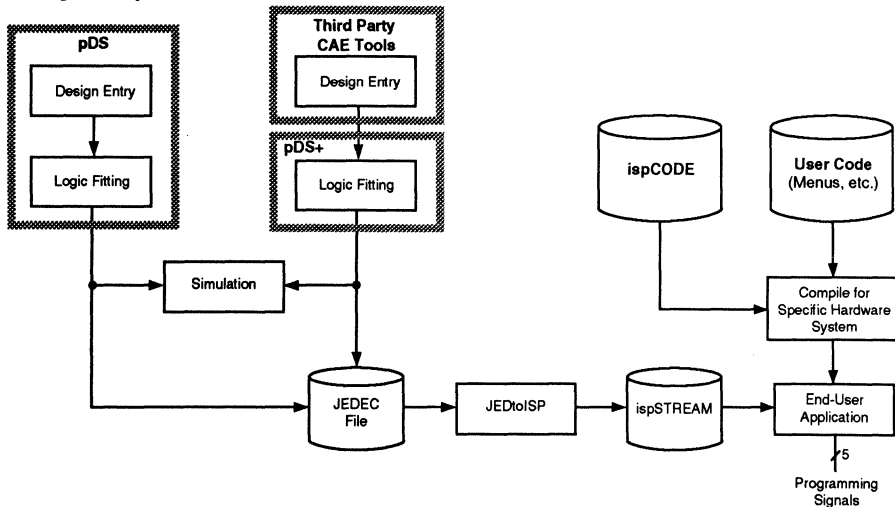
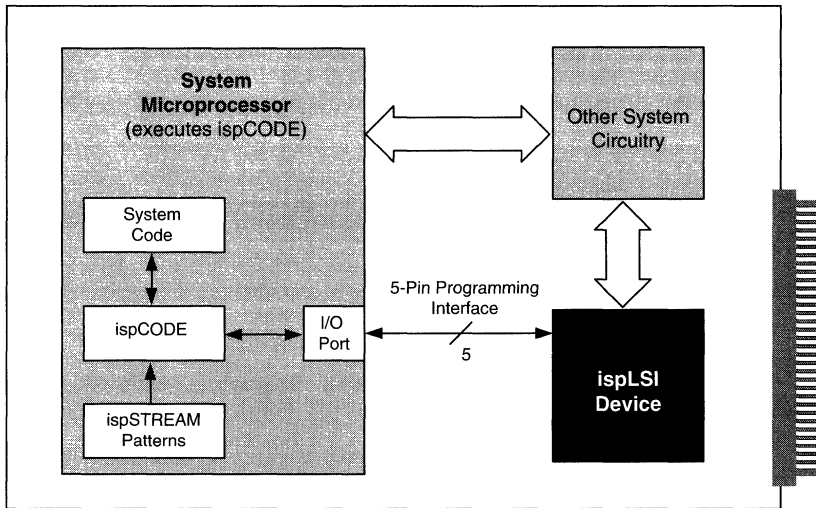
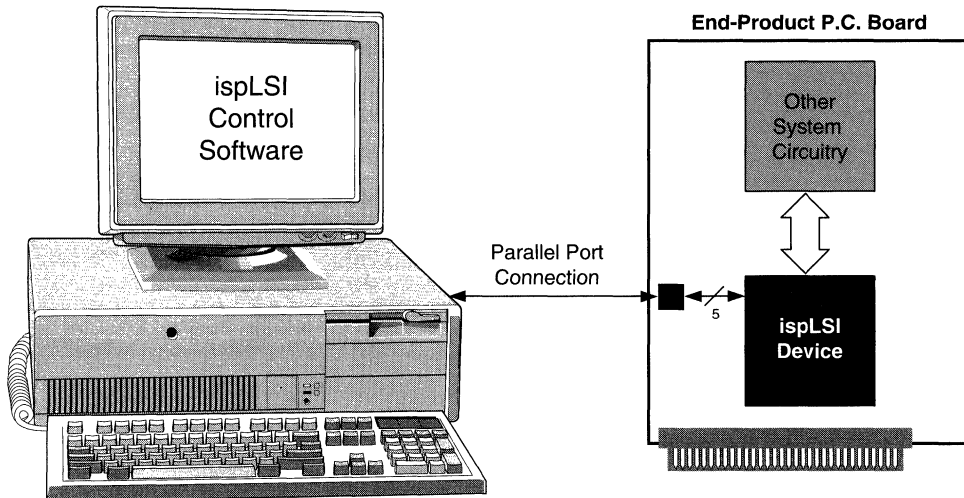


Figure 2. Configuring an ispLSI Device from an On-board Microprocessor



6

Figure 3. Configuring an ispLSI Device from a Remote System



Automatic Program Count

Another useful feature of ispCODE is the implementation of a program counter. A section of the same area in which the UES is stored is reserved for a 16-bit count of programming cycles. When the ispCODE routines are used exclusively for programming the device, an accurate count of programming cycles will be available to the user. The programming routine automatically increments the count after each programming cycle. There is also a routine which reads the count value from the device.

Table 1. High Level Routines

Routine	Purpose
isp_program()	program the entire device
isp_read()	read the entire device
isp_verify()	verify the entire device
isp_secure()	secure the device
isp_jedtoisp()	convert JEDEC file to ispSTREAM format
isp_isptojed()	convert ispSTREAM format to JEDEC file
isp_new()	initialize device data structure, including pattern data and address
isp_delete()	delete device data structure
isp_read_ues()	read the User Electronic Signature (UES) from the device
isp_ues_to_string()	convert an array of UES bits to a standard C string
isp_string_to_ues()	convert a standard C string to an array of UES bits
isp_compare_ues()	compare two arrays of UES bits
isp_get_count()	get the programming count
isp_get_id()	get the device ID from a device
isp_add_checksum()	calculate and add/update an ispSTREAM checksum
isp_check_stream()	verify the checksum of an ispSTREAM
isp_calc_checksum()	calculate the checksum of an ispSTREAM

Using the Routines

All the user-accessible routines use a data structure (isp_STRUCT) to hold all the data needed to do any ISP operation on a given device. This structure is defined in a header file, which must be included in any program that calls the Lattice routines. There are two routines, isp_new() and isp_delete(), which handle the memory allocation and freeing, as well as the data initialization for isp_STRUCT items.

Multiple isp_STRUCT structures may be allocated at once, since all the routines take a pointer to a single isp_STRUCT, and don't depend on any global variables. Each structure created holds a pointer to an ispSTREAM, as well as the I/O port address, for the device (and other device-specific data). Different devices could be located at different addresses and easily programmed by sequential calls to the isp_program() routine with a different isp_STRUCT pointer each time.

Devices Supported

The ispCODE library of routines will support all Lattice in-system programmable devices. As new devices are developed and released, the ispCODE library will be updated to include them.

Hardware Requirements

The ispCODE routines are designed to be portable to any hardware platform with an ANSI C compiler available. The code is written such that accessing the pins of the Lattice device is done by writing to a memory or I/O port address.

In addition to driving the pins, a method of controlling timing in the millisecond range is required. The best approach for this is a hardware-based method, such as a timer chip that can be read. Most micro controllers have a timer built in, and most other systems have some way of keeping time that may be used. The ispCODE source files include an example of reading the timer chip on a PC to accurately time the programming pulses.

ispCODE Ordering Information

Part Number	Description
pDS4103	ispCode Software - ANSI C Compiled and Source Files

Lattice includes a copy of the ispCODE with pDS and pDS+ software purchases.

Technical Support Assistance

Lattice Hotline: 1-800-LATTICE (Domestic)

Lattice Hotline: 1-408-428-6414 (International)

Lattice BBS: 1-408-980-9814

email: applications@lattice.com

ispCODE Example Program

Below is a sample program using the Lattice routines to program, verify, and secure a device from an ispSTREAM file. The usual error checking has been omitted for clarity, with the ispCODE specific sections in boldface type. This file would be compiled and linked with the ispCODE routines to produce the executable program.

```

#include      <stdio.h>
#include      <stdlib.h>
#include      "isplsi.h"

void main(int argc, char *argv[])
{
isp_STRUCT *device;
unsigned inport, outport;

FILE *source_file;
int verified = FALSE;
int i, dev_num;

/* Program device #1 */
dev_num = 1;

/* use LPT1 parallel port on PC */
inport = PORT1_IN;
outport = PORT1_OUT;

/* Initialize isp device structure, allocate memory for the
   ispSTREAM, and set device type and I/O ports */
device = isp_new(ispLSI1032, TRUE, FALSE, inport+1, outport, dev_num);

/* read file into ispSTREAM buffer allocated by isp_new()*/
source_file = fopen(argv[1],"rb");
for( i=0; i<device->stream_bits; i++)
    device->stream[i] = getc(source_file);

/* print status and program the device */
printf("Programming... Please wait. \n");
isp_program(device, FALSE);

/* print status and verify the device */
printf("Verifying... Please wait. \n");
verified = isp_verify(device, TRUE);

if( verified )
{
    printf("Device programmed and verified! \n");
    /* secure device if verified properly */
    isp_secure(device);
}
else
    printf("ERROR: Device did not verify \n");

/* free the memory allocated for the isp_STRUCT */
isp_delete(device);
} /*main()*/

```


Features

- Supports All ispLSI 1000, 2000 and 3000 Family Members
- Stand-alone Device Programmer
- Download Directly to an ISP™ Device on System Board
 - Only 5 Control/Data Pins Needed
- Quick Device Programming
- Inexpensive, Small and Compact
 - Eliminates Need For Expensive, Remote Programmer
- Excellent for Prototyping New Designs
 - Not Intended For Production Programming
- Easy to Use
- Connects Directly to Parallel Printer Port of Host PC

Description

The isp Engineering Kit Model 100 provides designers a quick and inexpensive means of evaluating and prototyping new designs using Lattice in-system programmable Large Scale Integration (ispLSI™) devices. This Kit is designed for engineering purposes only and is not intended for production use. The Kit programs devices from the parallel printer port of a host PC using the Lattice pLSI/ispLSI Development System (pDS®) or pLSI/ispLSI Development System Plus (pDS+™) PC-based designs tools. By connecting a system cable (included) from the host PC to the isp Engineering Kit, or connecting from the host PC to the target device on the system board, a JEDEC file can be easily downloaded into the ispLSI device(s).

Components

The isp Engineering Kit Model 100 consists of two primary components, each sold separately:

- Universal Programming Module (UPM)
- Socket Adapters

The adapters plug into the UPM base. The adapter provides the appropriate PLCC, PQFP, TQFP, or QFP socket for a particular ispLSI device package.



isp Engineering Kit - Model 100

UPM Description

The Model 100 Universal Programming Module (UPM) is designed to support all package types available from Lattice. It consists of the following components:

- Universal Programming Module Base Unit
- Power Supply Converter (110VAC/9VDC @ 200mA)
 - Included for North America and Asia Only
- 25-Pin Parallel Port Adapter
- 6' Universal Programming Module Download Cable with Modular Phone connectors (RJ45) on both ends
- 6' System Download Cable with a Modular Phone connector on one end and a AMP 1-87499-3 connector on other end

The connection between the host PC and the UPM base unit is shown in figure 1.

Electrical Characteristics

Power Supply

AC Input Voltage: 110 VAC
 DC Output Voltage: 9 VDC @ 200mA

UPM Physical Characteristics

Length: 3.75 inches
 Width: 2.625 inches
 Depth: 1.375 inches

Download Cables

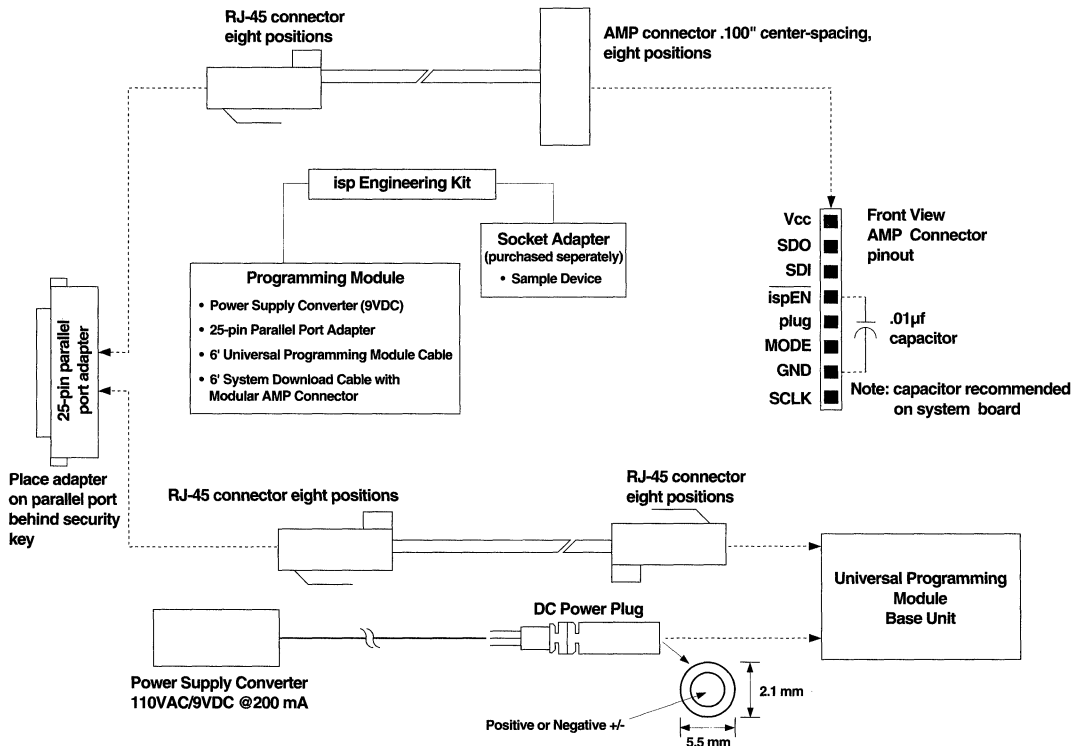
Download Cable with RJ-45 Phone Connectors on Both Ends

Length: 6.0 feet (192.8 cm)
 Connectors: RJ-45 with eight positions

System Download Cable with RJ-45 Phone and AMP 1-87499-3 Connectors

Length: 6.0 feet (192.8 cm)
 Connectors: RJ-45 with eight positions
 AMP single in-line 0.100" center spacing 8 positions

Figure 1. Universal Programming Module Description



0613A

Ordering Information

Order Code	Product Description
pDS4102-PM	isp Engineering Kit Model 100 for the PC: UPM programming module, (2) 8 wire Download cables, AC/DC Power Supply Converter, 25-Pin Parallel Port Adapter
pDS4102-J44	44-pin PLCC socket adapter, (1) ispLSI 1016 Engineering Sample
pDS4102-T44	44-pin TQFP socket adapter, (1) ispLSI 1016 Engineering Sample
pDS4102-J68	68-pin PLCC socket adapter, (1) ispLSI 1024 Engineering Sample
pDS4102-J84	84-pin PLCC socket adapter, (1) ispLSI 1032 Engineering Sample
pDS4102-T100	100-pin TQFP socket adapter, (1) ispLSI 1032 Engineering Sample
pDS4102-Q120	120-pin PQFP socket adapter, (1) ispLSI 1048 Engineering Sample
pDS4102-Q128	128-pin PQFP socket adapter, (1) ispLSI 1048C Engineering Sample
pDS4102-M160	160-pin MQFP socket adapter, (1) ispLSI 3256 Engineering Sample
pDS4102-G167	167-pin CPGA socket adapter, (1) ispLSI 3256 Engineering Sample

Features

- Supports All ispLSI 1000, 2000, and 3000 Family Members
- Stand-alone Device Programmer
- Download Directly to an ISP™ Device on System Board
 - Only 5 Control/Data Pins Needed
- Quick Device Programming
- Inexpensive, Small and Compact
 - Eliminates Need For Expensive, Remote Programmer
- All External isp Signals Optically Isolated from Workstation
 - Prevents Ground Loop Problems
- Excellent for Prototyping New Designs
 - Not Intended for Production Programming
- Easy to Use
- Connects Directly to Serial Port of Host Workstation

Description

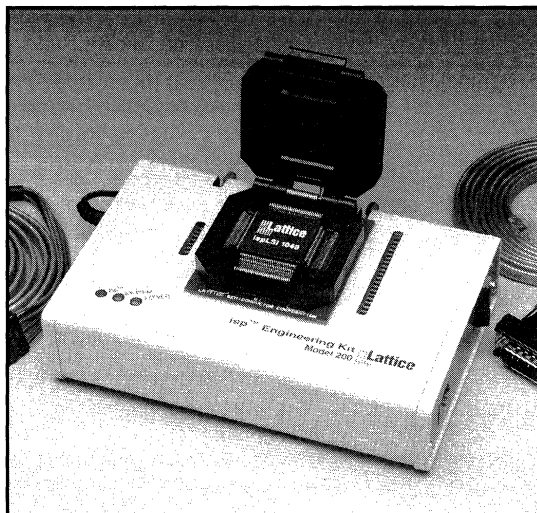
The isp Engineering Kit Model 200 provides designers a quick and inexpensive means of evaluating and prototyping new designs using Lattice in-systems programmable Large Scale Integration devices (ispLSI™). This Kit is designed for engineering purposes only and is not intended for production use. The Kit programs devices from the RS-232 serial port of a host workstation using the Lattice pLSI/ispLSI Development System Plus (pDS+™) workstation based design tools by connecting a system download cable (included) from the host workstation to the isp Engineering Kit.

Components

The isp Engineering Kit Model 200 consists of two primary components, each sold separately:

- Universal Programming Module (UPM)
- Socket Adapters

The adapters plug into the UPM base. The adapter provides the appropriate PLCC, PQFP, TQFP or QFP socket.



isp Engineering Kit - Model 200

Model 200 Description

The Model 200 Universal Programming Module (UPM) is designed to support all package types available from Lattice. It consists of the following components:

- Universal Programming Module Base Unit
- Power Supply Converter (110VAC/9VDC at 500mA)
 - Included for North America and Asia Only
- RS-232C (DB25P) Serial Port Adapter and cable
- 6' Universal Programming Module Download Cable with Modular Phone connectors (RJ45) on both ends
- 6' System Download Cable with a Modular Phone connector on one end and a AMP 1-87499-3 connector on other end

A drawing showing the connection between the workstation host and the UPM is shown in figure 1.

Detailed Functional Description

Top Panel

The top panel has three status indicator lights:

Power Indicator Light: Green illuminates when the power is turned ON and the correct input voltage is applied to the programming module.

System Indicator Light: Green or Red. When data is transmitted to or read from an isp device on the socket adapter board, the light becomes green. When any type of error is detected during programming, the light blinks red.

isp Indicator Light: Green illuminates when data is transmitted to or read from an isp device that is connected to the isp download cable. If the programming module detects the presence of a supply voltage on the isp download cable, it becomes active and programming to the socket adapter board is bypassed, regardless of the presence of a device on the socket adapter board.

Quick-Connect Interface for Socket Adapter Boards

Located at rear of the top panel are slots for the dual set of quick release contacts and the handles used to activate them. The inner or outer pair of contacts is chosen depending on type of socket adapter board used. The handles are flipped up when a socket adapter board is inserted in the proper contact slots. Push both handles down to lock the socket adapter board in place.

Left Panel

Power Input Jack

This jack is coaxial and accepts the power plug from the Power Supply Converter.

RS-232 RJ-11 Jack

This jack connects the RS-232C flat cable to the workstation's serial port.

BAUD

An eight position DIP switch that sets the serial port communications parameters. This switch is set at the factory for optimum performance.

Right Panel

ON/OFF Switch

This switch controls the input power supplied to the programming module.

RJ-45 Jack

If download is to be performed while an isp device is on board, the isp download cable is plugged into the RJ-45 jack.

Figure 2. isp Engineering Kit Model 200

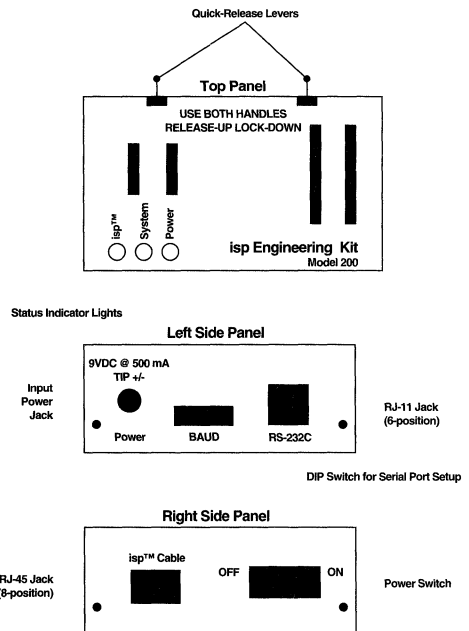
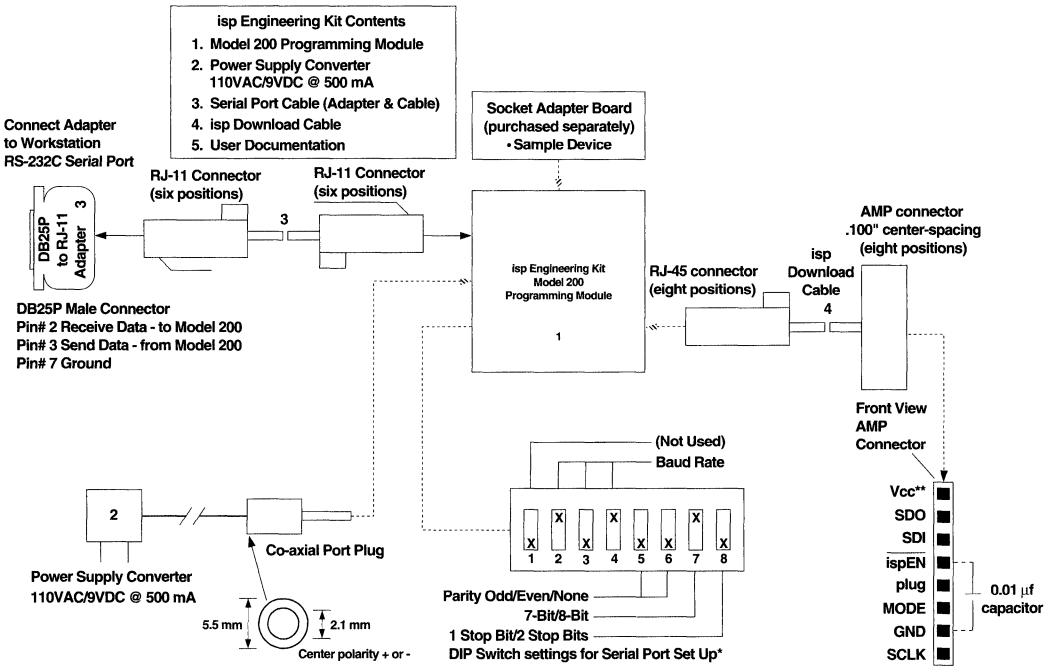


Figure 1. isp Engineering Kit Model 200



*Note: These are factory settings

**Note: User's system must supply 5VDC @ 30 mA

0814A

DIP Switch Settings

DIP switch settings for Model 200 are shown in Tables 1 to 4.

Note: SW1 is not used and asterisk following parameters are default factory settings

Table 1. RS-232C Baud Rate Selection

Baud Rate	SW2	SW3	SW4
38400*	UP	DOWN	UP
19200	UP	DOWN	DOWN
9600	DOWN	UP	UP
2400	DOWN	UP	DOWN
1200	DOWN	DOWN	UP
300	DOWN	DOWN	DOWN

Table 2. Parity Selection

Parity	SW5	SW6
None*	DOWN	DOWN
Odd	UP	DOWN
Even	UP	UP

Table 3. Word Length Selection

Word Length	SW7
7 Data Bits	DOWN
8 Data Bits*	UP

Table 4. Stop Bit Selection

Number of Stop Bits	SW8
1*	DOWN
2	UP

Electrical Characteristics

Power Supply

AC Input Voltage:	110 VAC
DC Output Voltage:	9 VDC @ 500mA

UPM Physical Characteristics

Length:	6.50 inches
Width:	4.125 inches
Depth:	1.50 inches

Download Cables

Serial Port Cable with RJ-11 Phone Connectors on Both Ends

Length:	6.0 feet (192.8 cm)
Connectors:	RJ-11 with 6 positions

System Download Cable with RJ-45 Phone and AMP 1-87499-3 Connectors

Length:	6.0 feet (192.8 cm)
Connectors:	RJ-45 with 8 positions AMP single in-line 0.100" center spacing 8 positions

Ordering Information

Order Code	Product Description
pDS4102-WS	isp Engineering Kit Model 200 for the Workstation: M200PM programming module, (1) 8 wire Download cable, (1) 6 wire Download cable, AC/DC Power Supply Converter
pDS4102-J44	44-pin PLCC socket adapter, (1) ispLSI 1016 Engineering Sample
pDS4102-T44	44-pin TQFP socket adapter, (1) ispLSI 1016 Engineering Sample
pDS4102-J68	68-pin PLCC socket adapter, (1) ispLSI 1024 Engineering Sample
pDS4102-J84	84-pin PLCC socket adapter, (1) ispLSI 1032 Engineering Sample
pDS4102-T100	100-pin TQFP socket adapter, (1) ispLSI 1032 Engineering Sample
pDS4102-Q120	120-pin PQFP socket adapter, (1) ispLSI 1048 Engineering Sample
pDS4102-Q128	128-pin PQFP socket adapter, (1) ispLSI 1048C Engineering Sample
pDS4102-M160	160-pin MQFP socket adapter, (1) ispLSI 3256 Engineering Sample
pDS4102-G167	167-pin CPGA socket adapter, (1) ispLSI 3256 Engineering Sample



ispDOWNLOAD™ Cable

Download Cable for In-System Programming of the Lattice ISP™ Family of Devices

Features

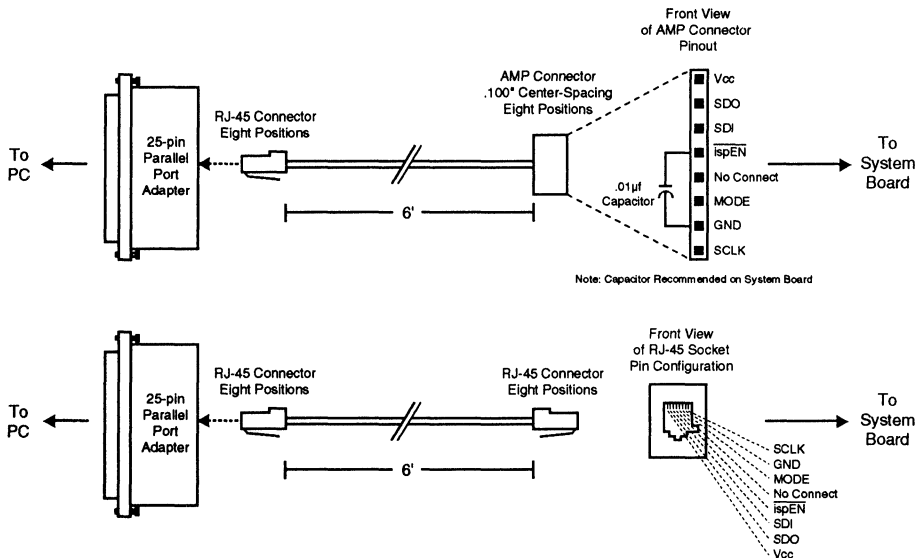
- **CABLE AND PARALLEL PORT ADAPTER FACILITATE IN-SYSTEM PROGRAMMING OF ISP FAMILY OF DEVICES**
 - Simplifies In-System Programming
 - Ideal for Design Prototyping and Debugging
- **SUPPORTS ALL ISP™ FAMILIES**
 - ispLSI™ Families (1000, 2000 and 3000)
 - ispGAL® Family
 - ispGDS™ Family
- **EASY-TO-USE CONNECTORS**
 - 25-Pin Adapter Connects to PC Parallel Printer Port
 - Two 6' Cables Offer P.C. Board Interface Options:
 - RJ-45 Connector
 - AMP Connector (8 Position, .100 Inch Center Spacing)

Introduction

The ispDOWNLOAD Cable product is designed to facilitate in-system programming of all Lattice ISP devices on a printed circuit board directly from the parallel port of a PC. With In-System Programming, hardware functions can be programmed and modified in real-time on the system board to give additional product features, shorten system design and debug cycle time, enhance product manufacturability and simplify field upgrades. After completion of the logic design and creation of a JEDEC file by a logic compiler such as the pDS®, pDS+™ Fitter or ispGDS Compiler software, Lattice's ispDOWNLOAD Software programs devices on the end-product p.c. board by generating programming signals directly from the parallel port of a PC which then pass through the ispDOWNLOAD Cable to the device. With this cable and a connector on the p.c. board, no additional components are required to program a device. The ispDOWNLOAD Software automatically generates the appropriate ISP command, programming address and data from the JEDEC fusemap information. ispDOWNLOAD Software is included with all Lattice pDS and pDS+ Fitter products. For the ispGDS, the ispDOWNLOAD Software can be obtained directly from the Lattice Literature Department.

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Figure 1. ispDOWNLOAD Cable Offers Two Types of In-System Programming Interfaces



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Figure 2. PC Parallel Port Connector

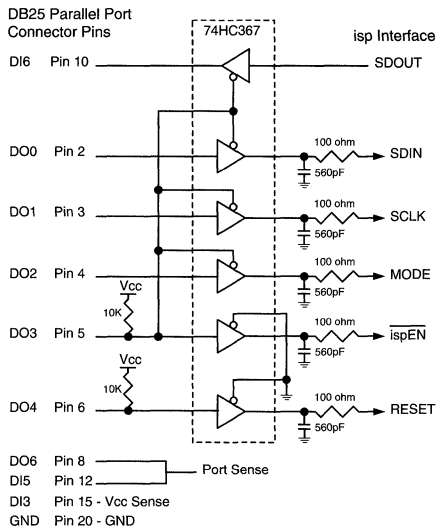
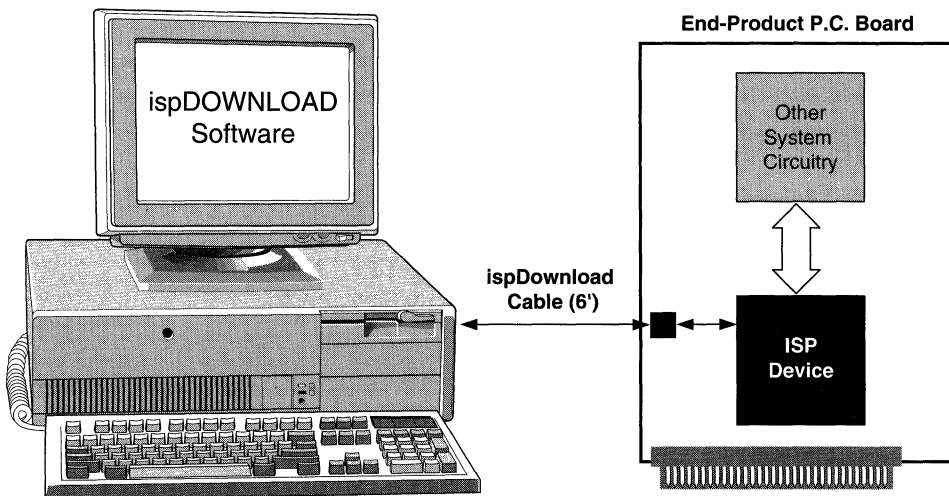


Figure 3. Configuring In-System Programming from a Remote System



Ordering Information

Part Number	Description
pDS4102-DL	ispDOWNLOAD Cable (For PC Only) Contains: Two 6' Cables with RJ45 and AMP Connectors Parallel Port Adapter Documentation

pLSI and ispLSI Design Tool Selector Guide

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DESIRED DESIGN ENVIRONMENT	DESIRED CAPABILITIES	pLSI and ispLSI DESIRED FAMILY SUPPORT			EXISTING TOOLS	DESIGN TOOL SOLUTION	PC ORDERING INFORMATION	SUN ORDERING INFORMATION
		1000	2000	3000				
LATTICE pLSI and ispLSI Development System (pDS)	Entry and Fitting	x	x		None	pDS-STD (Standard)	pDS1101-STD/PC1	N/A
				x	pDS1101	pDS 3000 Family Upgrade	pDS1101-3UP/PC1	N/A
		x	x	x	None	pDS-Ultra	pDS1101-ULT/PC1	N/A
	Entry, Fitting, and Simulation	x	x		None	pDS-STD (Standard) Viewlogic ViewSim Simulator	pDS1101-STD/PC1 pDS3302-PC1	N/A N/A
		x	x		ViewSim purchased from Viewlogic	pDS-STD (Standard) Viewlogic Interface/Library	pDS1101-STD/PC1 pDS1102-PC1	N/A N/A
		x	x		ViewSim purchased from Actel/TI/Other	pDS-STD (Standard) Viewlogic Interface/Library Upgrade	pDS1101-STD/PC1 pDS1103-PC1	N/A N/A
		x	x		ViewSim purchased from Xilinx	pDS-STD (Standard) Viewlogic Interface/Library Upgrade	pDS1101-STD/PC1 pDS1104-PC1	N/A N/A
		x	x	x	None	pDS-Ultra Viewlogic ViewSim Simulator	pDS1101-ULT/PC1 pDS3302-PC1	N/A N/A
		x	x	x	ViewSim purchased from Viewlogic	pDS-Ultra Viewlogic Interface/Library	pDS1101-ULT/PC1 pDS1102-PC1	N/A N/A
		x	x	x	ViewSim purchased from Actel/TI/Other	pDS-Ultra Viewlogic Interface/Library Upgrade	pDS1101-ULT/PC1 pDS1103-PC1	N/A N/A
x	x	x	ViewSim purchased from Xilinx	pDS-Ultra Viewlogic Interface/Library Upgrade	pDS1101-ULT/PC1 pDS1104-PC1	N/A N/A		
LATTICE In System Programmable isp-Starter Kit	isp-Starter Kit	x	and ispGAL22V10 and ispGDS		None	Lattice pDS Software to Support pLSH1016 and ispLSH1016, ispGDS, ispGAL22V10, Device Samples, Datasheets, and ispDownload Cable	isp-SK	N/A

pLSI and ispLSI Design Tool Selector Guide (Cont.)

DESIRED DESIGN ENVIRONMENT	DESIRED CAPABILITIES	pLSI and ispLSI DESIRED FAMILY SUPPORT			EXISTING TOOLS	DESIGN TOOL SOLUTION	PC ORDERING INFORMATION	SUN ORDERING INFORMATION
		1000	2000	3000				
DATA I/O ABEL	Entry and Fitting	x			None	ABEL 4.3 or Later Lattice pDS+ ABEL Fitter	From Data I/O pDS2102-PC1	From Data I/O pDS2102-SN1
		x			ABEL 4.3 or Later	Lattice pDS+ ABEL Fitter	pDS2102-PC1	pDS2102-SN1
	Entry, Fitting, and Simulation	x			None	ABEL 4.3 or Later Lattice pDS+ ABEL Fitter Viewlogic ViewSim Simulator Viewlogic Interface/Library	From Data I/O pDS2102-PC1 pDS3302-PC1 Included w/pDS3302	From Data I/O pDS2102-SN1 From Viewlogic pDS1102-SN1
		x			ABEL 4.3 or Later	Lattice pDS+ ABEL Fitter Viewlogic ViewSim Simulator Viewlogic Interface/Library	pDS2102-PC1 pDS3302-PC1 Included w/pDS3302	pDS2102-SN1 From Viewlogic pDS1102-SN1
		x			ViewSim purchased from Viewlogic	ABEL 4.3 or Later Lattice pDS+ ABEL Fitter Viewlogic Interface/Library	From Data I/O pDS2102-PC1 pDS1102-PC1	From Data I/O pDS2102-SN1 pDS1102-SN1
		x			ViewSim purchased from Actel/TI/Other (PC Only)	ABEL 4.3 or Later Lattice pDS+ ABEL Fitter Viewlogic Interface/Library Upgrade	From Data I/O pDS2102-PC1 pDS1103-PC1	N/A N/A N/A
		x			ViewSim purchased from Xilinx (PC Only)	ABEL 4.3 or Later Lattice pDS+ ABEL Fitter Viewlogic Interface/Library Upgrade	From Data I/O pDS2102-PC1 pDS1104-PC1	N/A N/A N/A
VIEWLOGIC Workview, PRO Series, Workview +, and Powerview	Capture and Fitting	x			None	Viewlogic ViewDraw Capture Lattice pDS+ Viewlogic Fitter Viewlogic Interface/Library	pDS1301-PC1 pDS2101-PC1 Included w/pDS1301	From Viewlogic pDS2101-SN1 pDS1102-SN1
		x			ViewDraw purchased from Viewlogic	Lattice pDS+ Viewlogic Fitter Viewlogic Interface/Library	pDS2101-PC1 pDS1102-PC1	pDS2101-SN1 pDS1102-SN1
		x			ViewDraw purchased from Actel/TI/Other (PC Only)	Lattice pDS+ Viewlogic Fitter Viewlogic Interface/Library	pDS2101-PC1 pDS1103-PC1	N/A N/A
		x			ViewDraw purchased	Lattice pDS+ Viewlogic Fitter	pDS2101-PC1	N/A

pLSI and ispLSI Design Tool Selector Guide (Cont.)

DESIRED DESIGN ENVIRONMENT	DESIRED CAPABILITIES	pLSI and ispLSI DESIRED FAMILY SUPPORT			EXISTING TOOLS	DESIGN TOOL SOLUTION	PC ORDERING INFORMATION	SUN ORDERING INFORMATION
		1000	2000	3000				
VIEWLOGIC Workview, PRO Series, Workview Plus, and Powerview	Capture, Fitting, and Simulation	x			None	Viewlogic ViewDraw Capture Viewlogic ViewSim Simulator Lattice pDS+ Viewlogic Fitter Viewlogic Interface/Library	pDS1301-PC1 pDS3302-PC1 pDS2101-PC1 Included w/pDS1301	From Viewlogic From Viewlogic pDS2101-SN1 pDS1102-SN1
		x			ViewDraw/ViewSim from Viewlogic	Lattice pDS+ Viewlogic Fitter Viewlogic Interface/Library	pDS2101-PC1 pDS1102-PC1	pDS2101-SN1 pDS1102-SN1
		x			ViewDraw/ViewSim from Actel/TI/Other (PC Only)	Lattice pDS+ Viewlogic Fitter Viewlogic Interface/Library Upgrade	pDS2101-PC1 pDS1103-PC1	N/A N/A
		x			ViewDraw/ViewSim from Xilinx (PC Only)	Lattice pDS+ Viewlogic Fitter Viewlogic Interface/Library Upgrade	pDS2101-PC1 pDS1104-PC1	N/A N/A
	Synthesis Option (VHDL Entry)	x			ViewSynthesis purchased from Viewlogic	Lattice Viewlogic Synthesis Library	pDS1105-PC1	pDS1105-SN1
ISDATA LOG/iC	Entry and Fitting	x			None	LOG/iC Lattice pDS+ LOG/iC Fitter	From ISDATA pDS2103-PC1	N/A N/A
		x			LOG/iC	Lattice pDS+ LOG/iC Fitter	pDS2103-PC1	N/A
	Entry, Fitting, and Simulation	x			None	LOG/iC Viewlogic ViewSim Simulator Lattice pDS+ LOG/iC Fitter	From ISDATA pDS3302-PC1 pDS2103-PC1	N/A N/A N/A
		x			ViewDraw/ViewSim from Viewlogic	Lattice pDS+ LOG/iC Fitter Viewlogic Interface/Library	pDS2103-PC1 pDS1102-PC1	N/A N/A
		x			ViewDraw/ViewSim from Actel/TI/Other (PC Only)	Lattice pDS+ LOG/iC Fitter Viewlogic Interface/Library Upgrade	pDS2103-PC1 pDS1103-PC1	N/A N/A
		x			ViewDraw/ViewSim from Xilinx (PC Only)	Lattice pDS+ LOG/iC Fitter Viewlogic Interface/Library Upgrade	pDS2103-PC1 pDS1104-PC1	N/A N/A



pLSI and ispLSI Design Tool Selector Guide (Cont.)

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DESIRED DESIGN ENVIRONMENT	DESIRED CAPABILITIES	pLSI and ispLSI DESIRED FAMILY SUPPORT			EXISTING TOOLS	DESIGN TOOL SOLUTION	PC ORDERING INFORMATION	SUN ORDERING INFORMATION	
		1000	2000	3000					
LOGIC MODELING	Board and System Level Simulation	x			None	SmartModel Library Subscription	Purchase from LMC	Purchase from LMC	
					Logic Modeling Library Subscription	Routine SmartModel Library Maintenance	Purchase from LMC	Purchase from LMC	
LATTICE ispCODE * * Included with pDS and pDS+ Fitter Software	Programming	x			pDS or pDS+ Software	ANSI C Source and Compiled In System Programming Routines	pDS4103	pDS4103	
LATTICE isp Engineering Kit and Socket Adapters	Programming	x	x	x		ispEngineering Kit Model 100	pDS4102-PM		pDS4102-WS
		x	x	x		ispEngineering Kit Model 200			
	Socket Adapter	x	x			44 Pin PLCC Socket Adapter	pDS4102-J44	pDS4102-J44	
	Socket Adapter	x	x			44 Pin TQFP Socket Adapter	pDS4102-T44	pDS4102-T44	
	Socket Adapter	x				68 Pin PLCC Socket Adapter	pDS4102-J68	pDS4102-J68	
	Socket Adapter	x	x			84 Pin PLCC Socket Adapter	pDS4102-J84	pDS4102-J84	
	Socket Adapter	x	x			100 Pin TQFP Socket Adapter	pDS4102-T100	pDS4102-T100	
	Socket Adapter	x				120 Pin PQFP Socket Adapter	pDS4102-Q120	pDS4102-Q120	
	Socket Adapter		x			128 Pin PQFP Socket Adapter	pDS4102-Q128	pDS4102-Q128	
	Socket Adapter			x		160 Pin MQUAD Socket Adapter	pDS4102-Q160	pDS4102-Q160	
Socket Adapter			x	167 Pin PGA Socket Adapter		pDS4102-G167	pDS4102-G167		

GAL Development Support

Lattice Semiconductor recommends the use of qualified programming equipment when programming Lattice devices. Lattice works with several programming manufacturers to insure that there is cost effective equipment available. We have approved programmers in each of the following categories:

- Low Cost GAL Only Programmers
- Mid Range 28-pin Programmers
- Full Universal Programmers
- Production Programming Equipment

Lattice conducts a very stringent qualification procedure, which includes a complete evaluation of the programming, verification and load algorithms; verification of critical pulse widths and voltage levels, along with a complete yield analysis. The result is the best programming yields in the industry and a guarantee of 100% programming yields to customers using qualified programming equipment. Below are the third-party programmers which are qualified to program Lattice devices.

For a current listing of Lattice qualified programmers, please call Lattice's Literature Distribution Department (Tel: 503-693-0287; FAX: 503-681-3037).

QUALIFIED PROGRAMMERS

Vendor	Programmer
Data I/O	Autosite
	Unisite
	3900
	2900
	29B
	60A/H
Logical Devices	Allpro 88
	Allpro 40
Stag	System 3000
	ZL30B & ZL30A
	Quasar-U84 & Quasar-U40
System General	TURPRO-1 & TURPRO-1/FX
	SGUP-85A
SMS Microcomputer	Sprint Expert
	Sprint Plus
BP-Microsystems	BP-1200
	PLD-1128 & CP-1128
	PLD-1100
Advin	Pilot-U84 & Pilot-U40
	Pilot-GL & Pilot-GCE

LOGIC COMPILER SUPPORT

Vendor	Logic Compiler
Accel Tech.	Tango PLD
Cadence	PIC Designer Composer
	PIC Designer Concept
Data I/O	ABEL
ISDATA	LOG/iC
Logical Devices	CUPL
Mentor Graphics	PLSynthesis II
Minc	PLDesigner-XL
OrCAD	OrCAD PLD
Omaton	Schema-PLD
Viewlogic	ViewPLD

GAL Development Support

PROGRAMMER/COMPILER VENDORS

Accel Technologies

6825 Flanders Dr.
San Diego, CA 92121
Tel: (619) 554-1000
FAX: (619) 554-1019

Advin Systems

1050-L Duane Ave
Sunnyvale, CA 94086
Tel: (408) 243-7000
FAX: (408) 736-2503

BP Microsystems

1000 N Post Oak Road
Houston, TX 77055-7237
Tel: (713) 688-4600
1-800-225-2102
FAX: (713) 688-0902
BBS: (713) 688-9283

Cadence Design Systems

555 River Oaks Parkway
San Jose, CA 95134
Tel: (408) 943-1234
FAX: (408) 943-0513

Data I/O Corp.

10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
Tel: (206) 881-6444
Tel: 1-800-247-5700
FAX: (206) 882-1043
In Europe contact:
Data I/O Corp.
Tel: +31 (0) 20-6622866
In Japan contact:
Data I/O Corp.
Tel: (03) 432-6991

ISDATA GmbH

Haid-und-Neu-Straße 7
7500 Karlsruhe 1
Germany
Tel: 0721-693092
FAX: 0721-174263

In the U.S. contact
ISDATA Inc.
Tel: (408) 373-7359
FAX: (408) 373-3622

Logical Devices

692 South Military Trail
Deerfield Beach, FL 33442
Tel: (305) 428-6868
FAX: (305) 428-1181

Mentor Graphics

8005 S.W. Boeckman Rd.
Wilsonville, OR 97070
Tel: (503) 685-7000
FAX: (503) 685-1204

Minc Incorporated

6755 Earl Dr.
Colorado Springs, CO 80918
Tel: (719) 590-1155
FAX: (719) 590-7330

Omaton

801 Presidential
Richardson, TX 75081
Tel: (214) 231-5167
FAX: (214) 783-9072

OrCAD Systems Corp.

3175 N.W. Alcoclek Dr.
Hillsboro, OR 97124
Tel: (503) 690-9881
FAX: (503) 690-9891

SMS Micro Systems

IM Grund 15
D-7988 Wangen
Germany
Tel: (49) 7522-5018
FAX: (49) 7522-8929
In the U.S. contact:
SMS North America, Inc.
16522 N.E. 135th Pl.
Redmond, WA 98052
Tel: (206) 883-8447
FAX: (206) 883-8601

Stag Microsystems

Martinfield
Welwyn Garden City
Herts AL7 1JT
United Kingdom
Tel: 011-44-707-332148
FAX: 011-44-707-371503
In the U.S. contact:
Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
Tel: (408) 988-1118
FAX: (408) 988-1232

System General

3Fl., No. 1, Alley 8, Lane 45
Bao Shing Rd.
Shin Dian
Taipei, Taiwan R.O.C.
Tel: 886-2-9173005
FAX: 886-2-9111283
In the U.S. contact:
System General
510 S. Park Victoria Dr.
Milpitas, CA 95035
Tel: (408) 263-6667
FAX: (408) 262-9220

Viewlogic Systems

293 Boston Post Rd. West
Marlboro, MA 01752
Tel: (508) 480-0881
FAX: (508) 480-0882

ispGDS

Compiler Support

Introduction

To simplify the development of ispGDS devices, Lattice offers an ispGDS assembler which processes the input ASCII files to generate the JEDEC compatible fusemap files required for the ispGDS devices. Free ispGDS assembler software is available from the Lattice BBS at 503-693-0215 under GDSPKG.ZIP file. This software is also available on diskette by calling the Lattice Hotline at 1-800-327-8425 (FASTGAL). For design engineers who are familiar with standard third party compiler software packages, ABEL from Data I/O and CUPL from Logical Devices also support all ispGDS devices.

Using the GDS Compiler

The compiler will accept an ASCII text file containing the GDS programming instructions, and will create JEDEC and .DOC files. Once a JEDEC file has been created, the ispGDS device can be programmed by either downloading the JEDEC file to a programmer, or by using the ispGDS Download utility to program the device using the parallel port of an IBM compatible PC.

Compiler Syntax

The basic compiler syntax supports inserting comments, title, device type, pin assignments and input/output assignments. The ispGDS compiler source file comment lines are denoted with quote marks at the beginning of the comment lines. The title is defined with the key word "title = ". Any text following the "title =" key word that are within single quotes are defined to be the title of the design. Similarly, the device type is defined by the key word "device =" followed by the three valid device types -- ispgds22, ispgds18, ispgds14. The compiler syntax also allow the user to assign pin names by typing in a 10 character pin name followed by at least a single space, the "pin" key word and the pin number. This pin assignment is optional since the compiler syntax allows the user to use the "pin" key word and the pin number directly in the input/output assignments.

The output pins are assigned on the left side of the equation and the input pins are assigned on the right side of the equation. To assign an output pin to either high or low, simply assign "H" or "L" respectively on the right side of the equation. If you need to assign an input pin to multiple output pins, use one line for each assignment, as

shown in the following example. In the example below, pin 28 is an input that is routed to three outputs — pin 1, pin 2 and pin 3. Further, each output's polarity can be individually defined. The example shows pin 3 as an active low polarity whereas pin 1 and pin 2 are defined to be active high polarity. An example source file is appended at the end of this document.

```
pin 1 = pin 28
pin 2 = pin 28
!pin 3 = pin 28
```

Assembling a File

To use the assembler, create an ASCII GDS source file, then invoke the assembler from the DOS command line. For example: `gasm <test.gds>`

where `test.gds` is the name of the GDS source file. GDS will create a JEDEC file with the same base name, and a .JED extension, like "test.jed," and a doc file with a .DOC extension, like "test.doc."

Submitting a New Problem Report

If you find problems with the assembler, please ZIP the following files together, and upload to the Lattice BBS at (503)693-0215:

1. the GDS source file
2. the JEDEC file
3. a description of the error

After the files are uploaded, please call the Lattice Hotline at (800) 327-8425 and inform them that the files have been uploaded.

Programming the ispGDS

You can either program the GDS using a JEDEC file output from the GDS assembler, or by using the GDS_PROG routines included in the GDSPKG software package. To program the GDS using a programmer, follow these steps:

1. Create an ASCII GDS source file
2. Assemble the GDS file using the GDS assembler (GASM).
3. Download the JEDEC file created by the assembler to the programmer and program the device. The

ispGDS Compiler Support

JEDEC file will have the same name as your GDS source file, but will have a .JED extension (for example, "test.jed").

Alternatively, you may want to program the ispGDS devices either through the parallel port of an IBM compatible PC, or through some custom hardware configuration. The routines included in the ispGDS compiler software package are configured to use the PC parallel port for programming. If you want to use a custom hardware configuration, read through the comments in GDS_PROG for information on which routines need to be modified. If you are programming using the PC, you will need an ispDOWNLOAD Cable and ISP programming interface signals on the circuit board which will plug into the printer port on your PC.

To program using the parallel port of the PC, follow these steps:

1. Create an ASCII GDS source file
2. Assemble the GDS file using the GDS assembler (GASM)
3. Convert the JEDEC file to ISP stream format by running JEDTOISP. See the documentation on JEDTOISP for further information.
4. Run GDS_PROG to program the device using the parallel port.

GDS Source Format

The following text is an example of a GDS source file.

```
"This is a comment (line begins with quote mark)
title = 'DIP SWITCH REPLACEMENT CONFIGURATION'

" the ispgds device type (ispgds22, ispgds18, ispgds14)
device = ispgds22

" pin names are defined as follows
pin_name pin 28

" pin 1 is an output connected to pin 28
pin 1 = pin_name
pin 2 = pin 27

" pin 3 is another output connected to pin 28
pin 3 = pin 28

" pin 5 is always high
pin 5 = h

"pin 6 is always low
pin 6 = l
pin 8 = pin 22

"! defines the inverted output for pin 9
!pin 9 = pin 20

pin 10 = pin 19
pin 12 = pin 17
pin 13 = pin 16
pin 14 = pin 15
```

Notes

If you get an error regarding "pin 0", you may have duplicated an output pin assignment (by assigning different input signals to the same output pin). Refer to the line number in the assembler error message to locate the source of the problem.

Section 1: Introduction

Section 2: High-Density Programmable Logic

Section 3: Low-Density Programmable Logic

Section 4: In-System Programmable Generic Digital Switch (ispGDS) Devices

Section 5: Military Program

Section 6: Development Tools

Section 7: Quality and Reliability

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Section 8: General Information

Quality Assurance Program

Introduction

Lattice views quality assurance as a corporate responsibility and an integral part of all operational activities. Lattice's Quality Assurance organization is independent from Manufacturing and has direct access to top management, assuring sufficient authority is afforded to quality issues.

Lattice's quality program is in full compliance to the quality assurance requirements of MIL-M-38510 Appendix A and all inspection system requirements of MIL-I-45208. Lattice is also fully certified to the ISO 9001 standard.

Reliability

All new products, processes and vendors must pass pre-defined evaluations before receiving initial qualification release. Major changes to products, processes or vendors require additional qualification before implementation. To assure continuing conformance to reliability goals, an ongoing monitor program is maintained on all products.

In-Process Control

Qualified product must be manufactured under strict quality controls that start with regulated procurement and documented inspection plans for all incoming materials. Sample testing and in-line monitoring as well as statistical process control charts provide constant feedback at each critical step of the manufacturing process.

Calibration

All equipment involved in determining product conformance to specifications through inspection, measurement or testing must be of the required accuracy. Equipment is calibrated and maintained on a defined interval against a nationally recognized standard. In addition, equipment must exhibit a suitable indicator showing calibration status as well as safeguards to disallow unauthorized adjustments.

Training

Key manufacturing personnel must complete a formal training program and obtain certification for each operation before they are allowed to perform activities affecting quality. Methods and records identifying the type and extent of training are maintained and recertification required on a yearly basis.

Subcontractor Control

All subcontracted manufacturing operations must be performed by sources exhibiting a quality program

commensurate to that of Lattice. These suppliers are audited at least once a year to monitor their compliance to Lattice's quality initiatives and goals. Incoming inspection is performed to provide feedback and continuous improvement of subcontractor performance with the main objective being to control quality at the source. Communications and in-line data are continuously exchanged to allow real-time monitoring of subcontractor manufacturing operations.

Document Control

Every product and process must have adequate written documentation released and available at the point of use before production begins. All information related to the definition, manufacturing, testing and support of Lattice products or services shall be maintained and controlled. Initial release as well as subsequent changes must be properly reviewed and approved before implemented.

Nonconforming Material

Material found to be nonconforming to specified requirements is identified, segregated, analyzed and dispositioned per documented procedures. Records are maintained denoting the nature of the discrepancy as well as the final disposition. All dispositions involve the applicable engineering section and Quality Assurance. Where applicable, the root cause of the discrepancy will be identified and a corrective action implemented using the CAR (Corrective Action Request) form.

Failure analysis

Failure modes discovered during qualification testing, inspections, customer returns or in-process screening are processed through Lattice's Failure Analysis group to determine the cause or relevancy of the failure. Verified failure modes are documented and corrective action initiated as required to eliminate the root cause.

Corrective action

All operational functions utilize a documented corrective action system coordinated, recorded and monitored by Quality Assurance. The system is designed to provide for proactive problem identification and resolution in a timely manner. Inputs include vendor, internal and customer related problems. Emphasis is placed on effective elimination of the root cause to prevent recurrence of the problem.

Management is responsible for ensuring that employees have sufficiently well defined responsibilities, authority and organizational freedom to identify potential quality related problems as well as initiate and implement solutions.

Quality Assurance Program

Self Audit

Internal self audits of the entire quality and delivery system are performed per written procedures and to a predefined schedule. The functional audits evaluate actual method to written procedure. The results of these audits are documented on a checklist and any discrepancies are brought to the attention of personnel responsible for the audited area. Deficiencies require corrective actions must be initiated and subsequently verified as to deployment and effectiveness. A periodic review of these functional audit results and corrective actions is performed by Quality Assurance.

Procurement

All direct materials and services affecting quality or reliability of end product must be purchased from qualified sources. Selection of these critical suppliers is based upon one of more of the following: quality system audits, product qualification testing, correlation studies, incoming inspection and demonstrated ability. A qualified supplier list is maintained by Quality Assurance and used by Purchasing to control procurement. Each purchase order must specify the applicable controlling requirements for all such direct materials or services.

Qualification Program

Introduction

Lattice has an intensive qualification program for examining and testing new products, processes, and vendors in order to insure the highest levels of quality. Lattice's Quality and Reliability Group is responsible for defining and implementing this qualification program.

The following table outlines the steps which must be performed before a new product, package or process is released. The requirements listed below are general guidelines. Detailed information on Lattice's qualification process is available to customers upon request.

Qualification Requirements

Test	# of Samples	Duration		
		New Product	New Wafer Process	New Package
125° C Operating Lifetest (5.25V)	300	1,000 Hours	2,000 Hours	2,000 Hours ¹
150° C Biased Retention Bake (5.25V)	450	1,000 Hours	2,000 Hours	2,000 Hours ¹
Endurance Cycling	75	10,000 Cycles	10,000 Cycles	N/A
ESD (CDM, HBM, MM)	216	End of Test	End of Test	N/A
Latch-Up Immunity	27	End of Test	End of Test	N/A
Temperature Cycling (-65 to 150° C)	150	1,000 Cycles	1,000 Cycles	1,000 Cycles
Biased 85/85 (5V)	225	N/A	1,000 Hours	1,000 Hours
Autoclave (121° C, 15psig)	150	N/A	336 Hours	336 Hours
Lead Integrity (DIP only)	9	N/A	N/A	End of Test
Solderability	9	N/A	N/A	End of Test
Physical Dimensions	6	N/A	N/A	End of Test

1. Required for new assembly technologies only.

Qualification Program

Reliability Monitor Program

The Reliability Monitor Program provides for a periodic reliability monitor of Lattice products. The program assures that all Lattice products comply on a continuing basis with established reliability and quality levels.

The Reliability Monitor Program is designed to monitor all fab and assembly facilities as well as each process technology in production. A summary of the program test and sampling plan is shown below.

Short Term Process Monitor (Bi-Weekly)

Test	# of Samples	Duration
125° C Operating Lifetest (6.50V)	70	160 Hours
150° C Biased Retention Bake (5.25V)	70	160 Hours
Autoclave (121° C, 15psig)	35	160 Hours

Long Term Process Monitor (Monthly)

Test	# of Samples	Duration
125° C Operating Lifetest (6.00V)	100	2000 Hours
150° C Biased Retention Bake (5.25V)	150	2000 Hours

Ongoing Package Monitor (Monthly)

Test	# of Samples	Duration
Temperature Cycling (-65 to 150° C)	50	1000 Cycles
85° C / 85% RH	75	2000 Hours

E²CMOS Testability Improves Quality

Introduction

The inherent testability of Lattice's E²CMOS PLDs significantly improves their quality and reliability. By using electrically erasable EEPROM technology to produce GAL, pLSI and ispLSI devices, Lattice is able to perform 100% AC/DC, functional, and parametric testing of every single device. In order to achieve the highest quality levels, Lattice programs and tests each device repeatedly throughout the manufacturing process.

Actual Test vs. Simulated Test

Why is "actual test" so significant? PLDs, unlike most other semiconductor devices, have a programmable element that determines the final device functionality and AC/DC performance. These programmable elements can be fabricated from metal link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or electrically erasable EEPROM cells. Each of these technologies carries a different variability of programming success and a variance in the impact of the programming success on the performance and reliability of the device.

The most common programmable elements are the metal fuse, EPROM cell and EEPROM cell. Of these element types, only the EEPROM cell can be thoroughly tested by the manufacturer prior to shipment to an end user OEM.

EEPROM Allows Actual Test

Each of the technologies identified above can be programmed. In this manner they are all the same. The differences become apparent when the erase times are analyzed. Metal link and One-Time Programmable (OTP) devices cannot be erased. UV EPROM devices can be erased, however the time required is 20-30 minutes (in an expensive windowed package). EEPROM devices, on the other hand, offer instant erasability on the order of 50 ms (thousandth's of a second). The advantage of this instant erase for manufacturing test is significant. Instant erase allows instant re-patterning for additional testing.

EEPROM technology has been used for PLD manufacturing by Lattice for more than a decade. Lattice refers to their high performance EEPROM technology as E²CMOS technology. Extensive reliability studies of the technology have been performed with industry-wide acceptance, including the military.

Other Methods Are Imprecise

All PLD devices must be tested to some degree to validate functionality and performance. Technologies that are not erasable or require lengthy erase times severely constrain

the test flexibility. Since the normal "user" programmable elements cannot be programmed during manufacture (all elements must be available for end-user programming) the manufacturers of one-time programmable PLDs resort to using simulated and correlated performance of test rows, test columns and phantom or dummy-test arrays. At best, this is a statistical measure of the actual device performance. One need only look at the "normal" programming yield fallout of 0.5 to 3% or the "acceptable" post-programming test vector and board yield fallout of 0.5 to 2% to know that this correlation is weak. The quality systems of today are measuring defects in parts per million (PPM). A six sigma program requires less than 3.4 PPM, four orders of magnitude less than that achievable with non-testable PLDs.

Actual Matrix Patterning

The unique capability of E²CMOS devices to be instantly electrically erased allows these devices to be patterned multiple times during Lattice's manufacturing test. Normal array cells in the programmable matrix are patterned, erased and tested again and again. The test rows or columns, phantom arrays, etc., that are used with other technologies are not necessary with E²CMOS devices. Programmability of every cell is checked dozens of times.

Historically, the checking of a successful programming operation consisted of no more than a pass/fail verification step. This digital, go/no go check is not adequate to assure that the cell is programmed properly with sufficient margin to guarantee long-term reliable performance of the device. Lattice E²CMOS devices are processed through a proprietary cell verification step that consists of an analog measure (to millivolt accuracy) of the actual cell threshold. This capability is used for extensive reliability and quality measurements and testing.

Worst Case AC/DC Testing

A PLD does not have a defined function until the engineer patterns the device with his custom pattern. The manufacturer, when considering the testing of a PLD, must consider the hundreds of different architecture and functional variations that can be created by the end user. Each configuration of architecture brings on a different set of worst case pattern and stimulus conditions. Quick application of a series of worst case patterns that cover all of the permutations of input combinations, array load and switching, and output configuration is required.

E²CMOS devices offer instant erasability to address this reconfiguration and test problem. Testing each additional

E²CMOS Testability Improves Quality

worst case configuration takes fractions of a second, allowing multiple patterns to be checked to assure performance to rated speeds. The final result is a device with defects reduced from PPH (parts per hundred) to PPM (parts per million).

ISO 9000 Program

Introduction

Lattice is the first major PLD manufacturer to complete ISO 9000 registration. Lattice Quality Systems have been certified, and the company is registered to the ISO 9000 standard. Lattice certification is for ISO 9001, the most comprehensive of the various ISO 9000 levels, covering the design, manufacturing, sales, and service functions.

ISO 9000 Certification

Certification to the ISO 9000 standard provides a recognized and standardized basis for the continued development of the quality and reliability of Lattice products. This certification assures Lattice's customers that its Quality Systems are well organized and embody a "Quality First" philosophy. It also reaffirms Lattice's promise to provide its customers with the highest quality and most reliable products in the industry.

What is ISO 9000?

The ISO 9000 series is an international version of British Standard BS 5750, intended to define the quality management systems for a wide range of an organization's

activities. The standard was initiated by the British Standards Institution, which over the last 80 years has certified over 9,000 Quality Systems. Today, both the CEN (European Committee for Standardization), which is commissioned to coordinate quality standards in Europe and remove potential trade restrictions within and outside the European Community, and the USA Standard ANSI/ASQC have adopted the ISO 9000 series.

Four quality standards make up the ISO 9000 series: ISO 9004, ISO 9003, ISO 9002, and ISO 9001. ISO 9004 is an informational document containing guidelines for Quality Management and Quality Systems. ISO 9003 guarantees quality in a product's final testing and inspection. ISO 9002 confirms quality in the production and installation of a product. ISO 9001 assures quality in a product's design, development, production, and installation. ISO 9001 is composed of 20 system sections, including the ISO 9002 and ISO 9003 subsets. Lattice is certified to the most comprehensive quality standard of the series, ISO 9001, and registered with the American Society for Quality Control's Registration Accreditation Board.



Lattice Semiconductor: First PLD Supplier to Achieve ISO 9000 Certification

Notes

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Section 2: High-Density Programmable Logic

Section 3: Low-Density Programmable Logic

Section 4: In-System Programmable Generic Digital Switch (ispGDS) Devices

Section 5: Military Program

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Copying PAL, EPLD & PEEL Patterns Into GAL Devices

INTRODUCTION

The generic/universal architectures of Lattice GAL devices are able to emulate a wide variety of PAL, EPLD and PEEL devices. GAL devices are direct functional and parametric replacements for most PLD device architectures. To use GAL devices in place of other PLD types, some conversion of the original device pattern may be needed. This conversion is not difficult, and can be accomplished at either the design or manufacturing level. The following sections describe several techniques available to convert PAL, EPLD and PEEL device patterns to Lattice GAL device patterns.

CROSS PROGRAMMING: GAL16V8 AND GAL20V8

The GAL16V8 and GAL20V8 devices replace most standard 20-pin and 24-pin PAL devices. To simplify the conversion process, Lattice has worked with programmer hardware manufacturers to provide the ability to program GAL devices directly from existing PAL JEDEC files, or master PAL devices. Lattice qualified programmers can automatically configure the architecture of a GAL device to emulate the source PAL device.

To provide a conceptual framework for the conversion from PAL devices to GAL devices, a mythical device known as a RAL device was created. A RAL device is simply a GAL device configured to emulate a PAL. There is a one-to-one correspondence between the name of a PAL device and that of a RAL device. For example, a RAL16L8 is simply a GAL16V8 configured as a PAL16L8. Some programmers list the RAL device types as choices for cross-programming, while others specifically state that a cross-programming operation is to be performed using a PAL device type as the architecture type. Other programmers list devices such as a Lattice 16L8. Even though Lattice does not make a 16L8 device, choosing this selection allows the programmer to accept a 16L8 JEDEC file, and will program a GAL16V8 device to emulate a PAL16L8.

To program a GAL16V8 or GAL20V8 device from an existing PAL JEDEC file, simply select the appropriate device code (either RAL type, or PAL type to cross-program from), then download the PAL JEDEC file to the programmer. Insert the appropriate GAL device that can directly emulate the PAL device (according to the chart in the GAL16V8 or GAL20V8 data sheets). The programmer will automatically configure the GAL device to emulate the PAL device during programming. The resulting GAL device is 100% compatible with the original PAL device.

A GAL device may also be programmed from a master PAL device by reading the pattern of the master PAL into the programmer memory, then selecting the appropriate RAL device or PAL type to cross-program from. The GAL device can then be programmed from the programmer memory.

CROSS PROGRAMMING: GAL22V10/GAL20RA10

The GAL22V10 and GAL20RA10 are direct replacements for bipolar PAL devices, and are JEDEC fuse map compatible with these industry standard devices. To program a GAL22V10 or GAL20RA10 device from an existing PAL JEDEC file, simply select the appropriate GAL device code, then download the PAL JEDEC file to the programmer. The resulting GAL device is 100% compatible with the original PAL.

GAL devices also may be programmed from Master PAL devices by reading the pattern of the Master PAL into the programmer memory, then selecting the appropriate GAL device code. The GAL device can then be programmed from the programmer memory.

The GAL22V10 and GAL20RA10 also can store a User Electronic Signature (see the data sheets on these devices for more information). To use this feature, the JEDEC file must contain this information. To add the signature data to the JEDEC map, use the PALtoGAL conversion utility (see next section) or recompile the source equations for a Lattice GAL device instead of a generic 22V10 type. Many programmers list two device types to differentiate between the two types of JEDEC files, and list both a GAL22V10 and a name such as GAL22V10-UES or GAL22V10-ES. Other programmers allow both types of JEDEC files to be accepted, and simply don't program the Signature fuses if they are not present in the file.

CROSS PROGRAMMING: GAL20XV10

The GAL20XV10 can be configured as a direct replacement for bipolar PAL20X10, 20X8, 20X4, and 20L10 devices. Many programmers provide cross-programming support similar to that provided for the GAL16V8/GAL20V8 devices. This allows the use of existing PAL device files to program the GAL20XV10 to emulate the PAL devices. The PALtoGAL conversion software (described below) also supports conversion of the PAL JEDEC files to a functionally equivalent GAL device file.

PALTOGAL CONVERSION UTILITY SOFTWARE

Lattice has created a software utility that will convert an existing PAL device JEDEC file to the appropriate GAL

Copying PAL Patterns Into GAL Devices

device JEDEC format. Called PALtoGAL, this software utility can be used to convert PAL device files to GAL device files, add/or change the User Electronic Signature without changing device functionality, and reformat existing GAL JEDEC files for readability.

Since a few programmable logic devices have features that a GAL device cannot exactly emulate, the PALtoGAL utility will clearly describe the incompatibility but will not create an output file. GAL devices programmed using files converted by PALtoGAL will be 100% compatible with the original logic device. PALtoGAL is just another method of cross-programming, and should produce the same results as using a programmer. The advantage is that a full GAL device JEDEC map is created, meaning that the appropriate GAL device may then be selected on the programmer, which may simplify the manufacturing flow. Also, the PALtoGAL conversion software provides conversions that programmers do not.

A copy of the PALtoGAL conversion utility software can be obtained through your local Lattice representative, or by

contacting the GAL Applications Hotline at 1-800-FASTGAL (327-8425) or (503) 693-0201. The software also may be downloaded from Lattice's Electronic Bulletin Board at (503) 693-0215; the file name is "PALTOGAL.EXE".

SOFTWARE COMPILER CONVERSION

If the equation source file is available for the PAL device, it can be converted by re-compiling using a suitable logic compiler that supports GAL devices. If there are any device incompatibilities (there shouldn't be in most cases), the compiler will describe the errors. The output of the compiler will be a GAL JEDEC file that can be used to program a GAL device directly. The resulting GAL device will be 100% functionally compatible with the original device.

Suitable logic compilers are listed in the Development Tools section. If additional questions arise, contact your compiler manufacturer or a Lattice Applications Engineer by calling the GAL Applications Hotline at 1-800-FASTGAL or (503) 693-0201.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LATTICE PART #
ALTERA	EP310 EP320 EP330	GAL16V8Z ¹ GAL16V8 ¹ or... GAL18V10
AMD	PAL10H8 PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8
	PAL16L8 PAL16R4 PAL16R6 PAL16R8 PALC16L8 PALC16R4 PALC16R6 PALC16R8 AmPAL16L8 AmPAL16R4 AmPAL16R6 AmPAL16R8 PAL16P8 PAL16RP4 PAL16RP6 PAL16RP8	GAL16V8
	PALCE16V8	GAL16V8
	PALCE16V8Z	GAL16V8Z
	AmPAL18P8 PALC18U8	GAL16V8 ¹ or... GAL18V10
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8
	PAL20L8 PAL20R4 PAL20R6 PAL20R8 AmPAL20RP4 AmPAL20RP6 AmPAL20RP8	GAL20V8
	PALCE20V8	GAL20V8
	PAL20RA10	GAL20RA10

MANUFACTURER	PART #	LATTICE PART #
AMD	AmPAL20RP10	GAL22V10
	PAL20S10 PAL20RS4 PAL20RS8 PAL20RS10	GAL6002 ¹ or... GAL22V10 ¹
	PAL12L10 AmPAL20L10 PAL20L10 PAL20X4 ² PAL20X8 ² PAL20X10 ²	GAL20XV10
	AmPAL22V10 PAL22V10 PALC22V10 PALCE22V10	GAL22V10
	PALCE24V10 PALCE26V12	GAL26CV12 ¹
	PLS167 PLS168	GAL6002 ¹
ATMEL	AT22V10	GAL22V10
CYPRESS	PALC16L8 PALC16R4 PALC16R6 PALC16R8	GAL16V8
	PLDC18G8	GAL16V8 ¹ or... GAL18V10
	PALC20CG10 PALC22V10 PAL22V10	GAL16V8 ¹ or... GAL22V10
	PLD20RA10	GAL20RA10
HARRIS	HPL16LC8 HPL16RC4 HPL16RC6 HPL16RC8	GAL16V8
ICT	PEEL18CV8	GAL16V8 ¹ or... GAL18V10
	PEEL153 PEEL253	GAL16V8 ¹ or... GAL18V10 ¹
	PEEL20CG10 PEEL22CV10A	GAL20V8 ¹ or... GAL22V10

1) Conversion possible but not 100% compatible with this device.

2) PLCC pin-out may not be 100% compatible.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LATTICE PART #	MANUFACTURER	PART #	LATTICE PART #
INTEL	5C031 5C032 85C220	GAL16V8' or... GAL16V8Z or... GAL18V10	SGS-THOMSON	GAL16V8	GAL16V8
	85C224	GAL20V8' or... GAL22V10		GAL20V8	GAL20V8
	85C22V10	GAL22V10		GAL39V18	GAL6001 or... GAL6002
NATIONAL	PAL10H8	GAL16V8	SIGNETICS	PLHS16L8 PLUS16L8 PLUS16R4 PLUS16R6 PLUS16R8	GAL16V8
	PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8		PLHS18P8	GAL16V8' or... GAL18V10
	PAL16L8 PAL16R4 PAL16R6 PAL16R8	GAL16V8		PLS153 PHD16N8	GAL16V8' or... GAL18V10'
	GAL16V8 GAL16V8A	GAL16V8		PLUS20L8 PLUS20R4 PLUS20R6 PLUS20R8	GAL20V8
	GAL18V10	GAL18V10		PLUS168 PLUS173	GAL6002'
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8		TI	TIBPAL16L8 TIBPAL16R4 TIBPAL16R6 TIBPAL16R8
	PAL20L8 PAL20P8 PAL20R4 PAL20RP4 PAL20R6 PAL20RP6 PAL20R8 PAL20RP8	GAL20V8	TICPAL16L8 TICPAL16R4 TICPAL16R6 TICPAL16R8		GAL16V8
	PAL20RA10	GAL20RA10	EP330 TIBPAD16N8		GAL16V8' or... GAL18V10'
	PAL20L10 PAL20X4 PAL20X8 PAL20X10	GAL20XV10	TIBPAL20L8 TIBPAL20R4 TIBPAL20R6 TIBPAL20R8		GAL20V8
	GAL22V10	GAL22V10	TIBPAL20L10 TIBPAL20X4 TIBPAL20X8 TIBPAL20X10		GAL20XV10
	GAL26CV12	GAL26CV12	TIBPAL22V10 TICPAL22V10		GAL22V10
	GAL6001	GAL6001 or... GAL6002	TIBPLS506C TIBPLS507C TIB82S105 TIB82S167		GAL6002'

1) Conversion possible but not 100% compatible with this device.

Package Thermal Resistance

The following table provides information on the package thermal resistance of Lattice commercial and industrial grade devices. For information on the package thermal resistance of Lattice military grade devices, please refer to "MIL-M-38510, Appendix C."

mounted on a thermal test board conforming to SEMI SPECIFICATION G42-88: "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages."

Test Conditions

Power Dissipation = 0.5watts (IC reverse biased)

Ambient Air Velocity = Zero (still air)

Ambient Temperature = 65°C

Measuring Current = 3mA

Testing was performed per SEMI TEST METHOD G38-87: "Still and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of IC Packages" with devices

PACKAGE THERMAL RESISTANCE

Package	Pin Count	θ_{JA}	θ_{JC}
Plastic DIP	20-pin	67°C/W	30°C/W
	24-pin	65°C/W	25°C/W
	28-pin	52°C/W	23°C/W
PLCC	20-pin	67°C/W	25°C/W
	28-pin	56°C/W	23°C/W
	44-pin	50°C/W	16°C/W
	68-pin	45°C/W	13°C/W
	84-pin	42°C/W	12°C/W
SOIC	20-pin	85°C/W	18°C/W
Ceramic DIP	20-pin	62°C/W	10°C/W
	24-pin	60°C/W	10°C/W
	28-pin	58°C/W	10°C/W
LCC	20-pin	65°C/W	8°C/W
	28-pin	62°C/W	7°C/W
JLCC	44-Pin	69°C/W	4°C/W
	68-pin	52°C/W	3°C/W
PQFP	120-pin	50°C/W	15°C/W
TQFP	44-pin	65°C/W	19°C/W
	100-pin	55°C/W	20°C/W
MQFP	160-pin	20°C/W	2°C/W
CPGA	84-pin	38°C/W	3°C/W
	167-PIN	25°C/W	2°C/W

Tape and Reel Specifications

A tape-and-reel packing container is available for plastic leaded chip carriers to protect the product from mechanical/ electrical damage and to provide an efficient method for handling. Lattice's tape-and-reel containers are shipped in full compliance to Electronics Industry Association Standard EIA-RS481.

The tape-and-reel packing system consists of a pocketed carrier tape loaded with one device per pocket. A protective cover tape seals the carrier tape and holds the devices in

the pockets. A full reel holds a maximum quantity of devices depending on the package size. Lattice requires ordering in full reel quantities. Once loaded, the tape is wound onto a plastic reel for labeling and packing.

Devices packaged in tape-and-reel containers must be factory programmed (pre-patterned). Custom marking of devices prior to mounting on tape-and-reel is available upon request. Contact your local Lattice sales office for more details on Lattice's tape-and reel packing system.

TAPE-AND-REEL QUANTITIES AND DIMENSIONS

Package	Pin Count	Carrier Tape Dimensions		Quantity Per 13 Inch Reel
		Width	Pitch	
PLCC	20-pin	16mm	12mm	1000
	28-pin	24mm	16mm	750
	44-pin	32mm	24mm	500
	68-pin	44mm	32mm	250
	84-pin	44mm	36mm	250

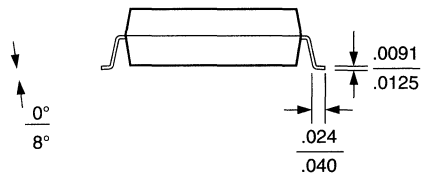
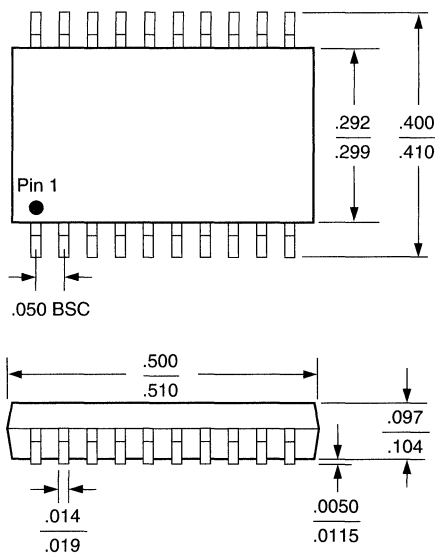
Package Diagrams

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28-Pin LCC	8-13
28-Pin CERDIP	8-14
44-Pin PLCC	8-14
44-Pin TQFP	8-15
44-Pin JLCC	8-15
68-Pin PLCC	8-16
68-Pin JLCC	8-16
84-Pin PLCC	8-17
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120-Pin PQFP	8-18
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20-Pin SOIC Package

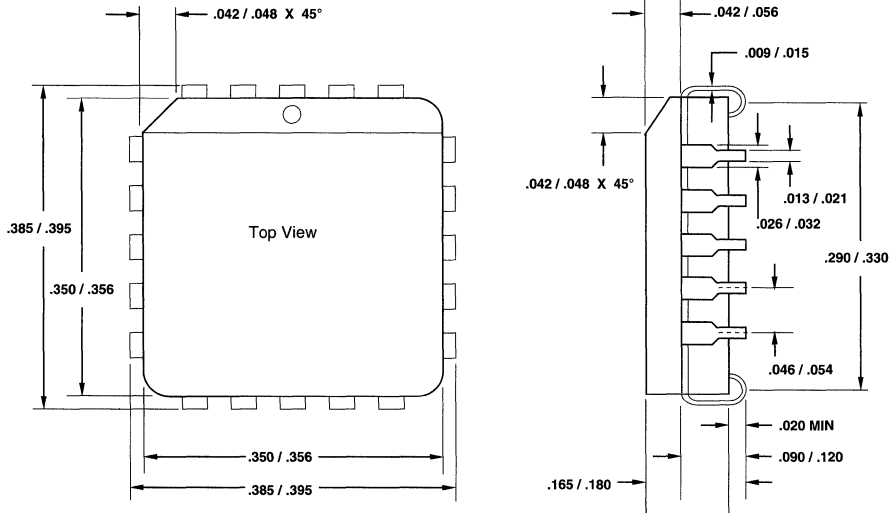
Dimensions in Inches MIN. / MAX.



Package Diagrams

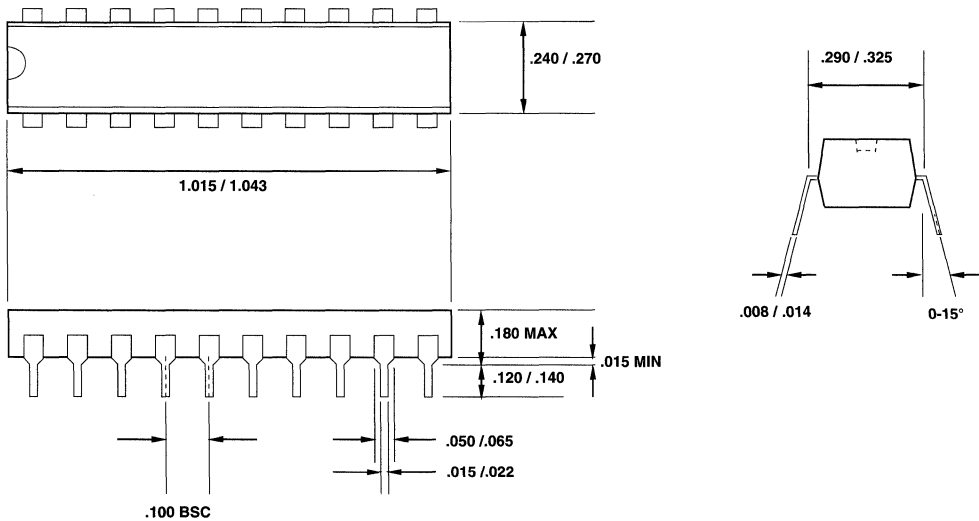
20-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



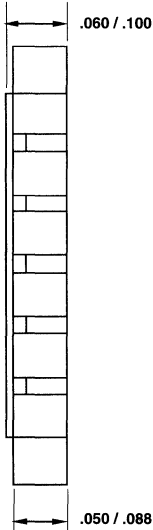
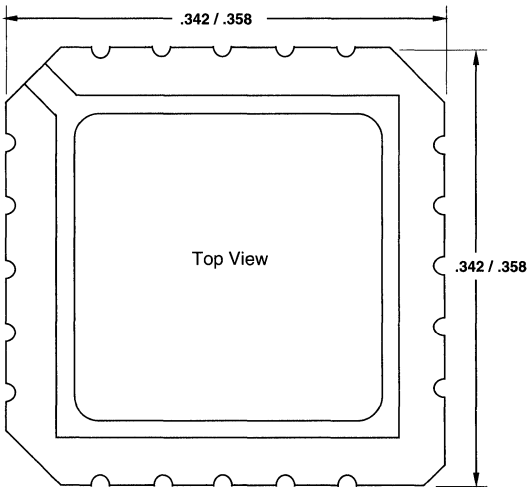
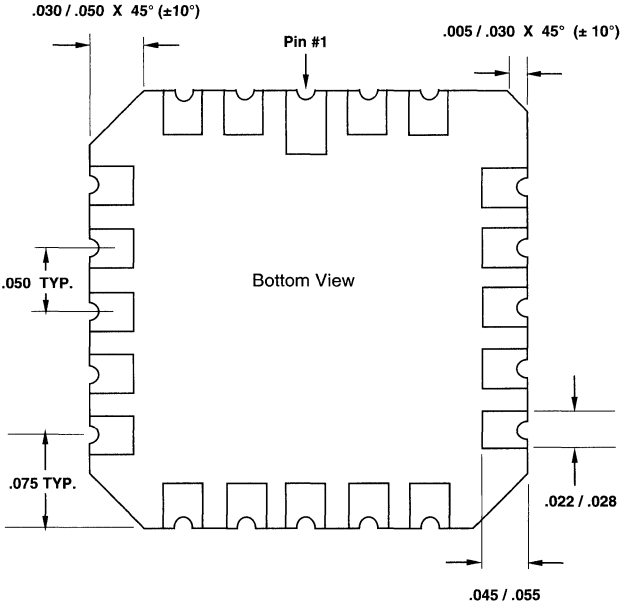
20-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



20-Pin LCC

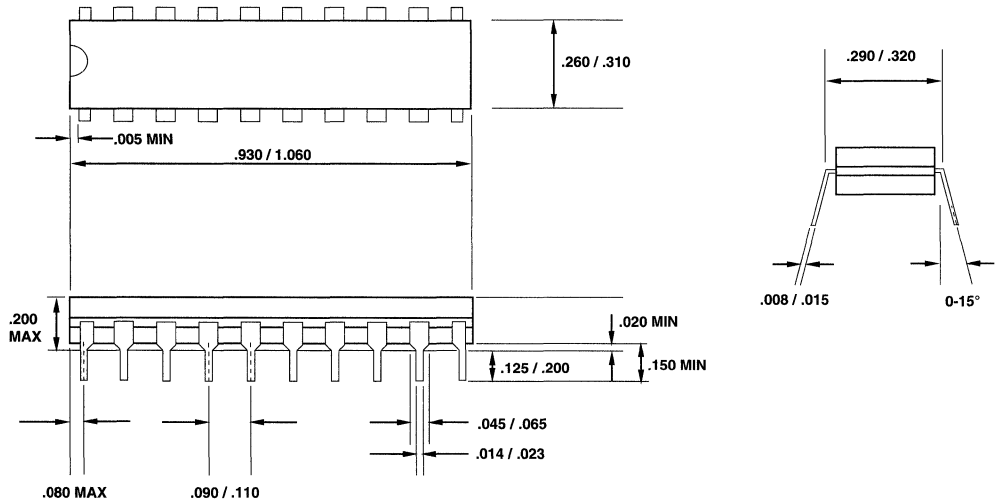
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Package Diagrams

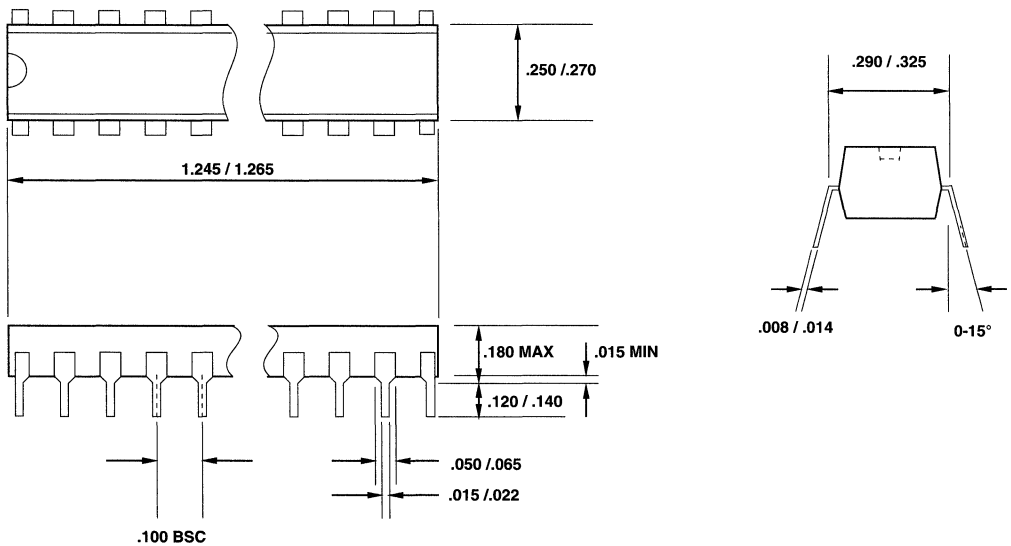
20-Pin (300-Mil) Cerdip

Dimensions in Inches MIN. / MAX.



24-Pin Plastic DIP

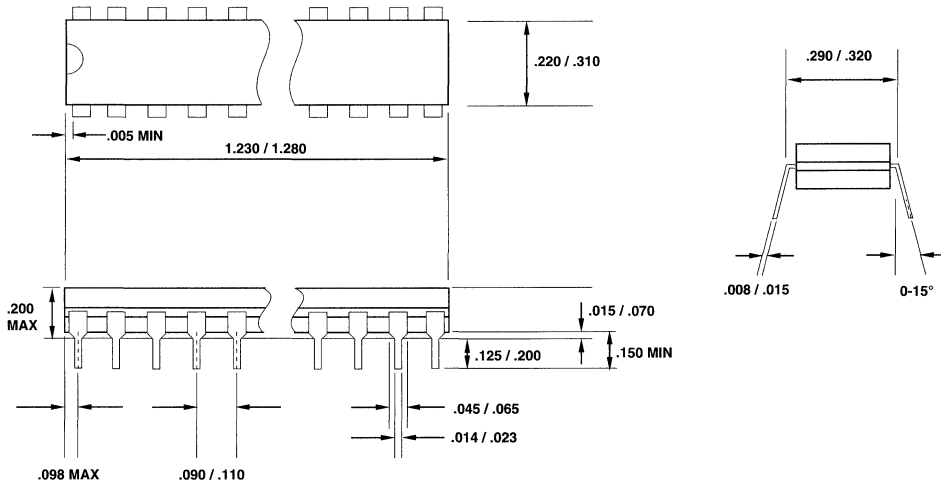
Dimensions in Inches MIN. / MAX.



Package Diagrams

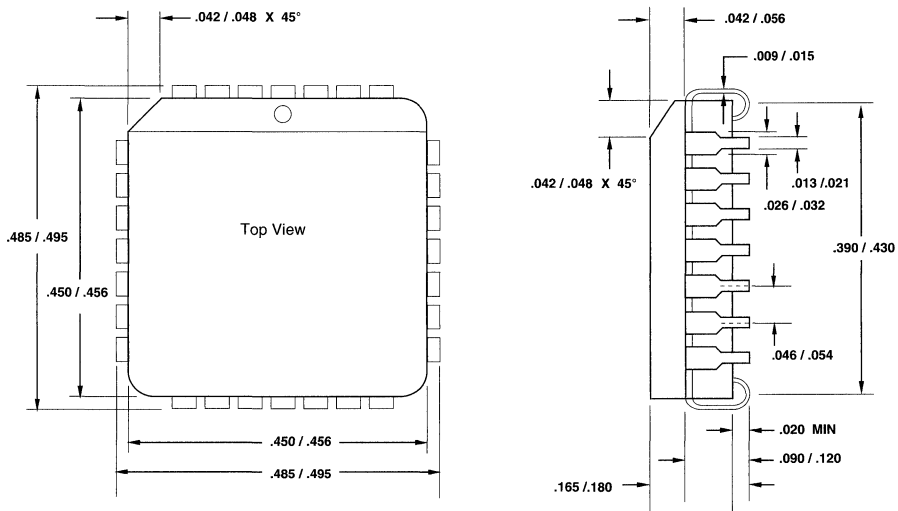
24-Pin (300-Mil) Cerdip

Dimensions in Inches MIN. / MAX.



28-Pin PLCC Package

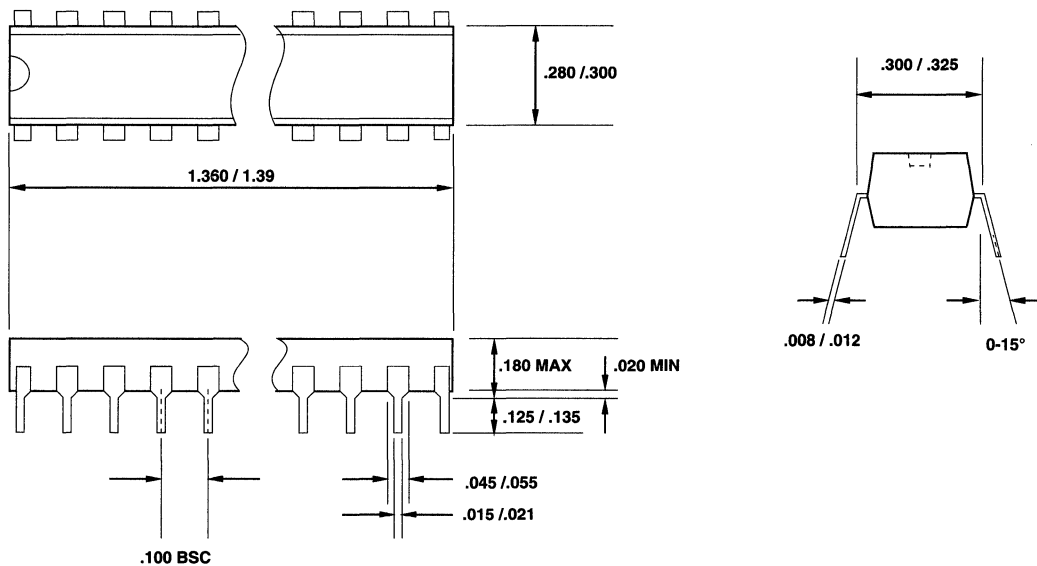
Dimensions in Inches MIN. / MAX.



Package Diagrams

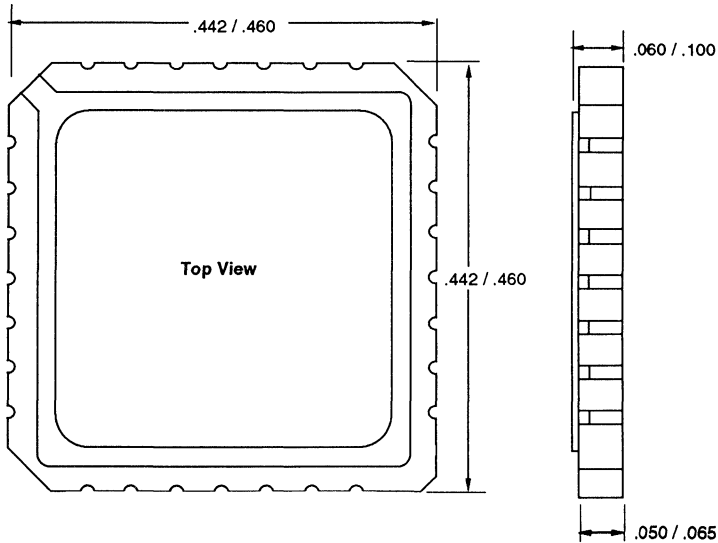
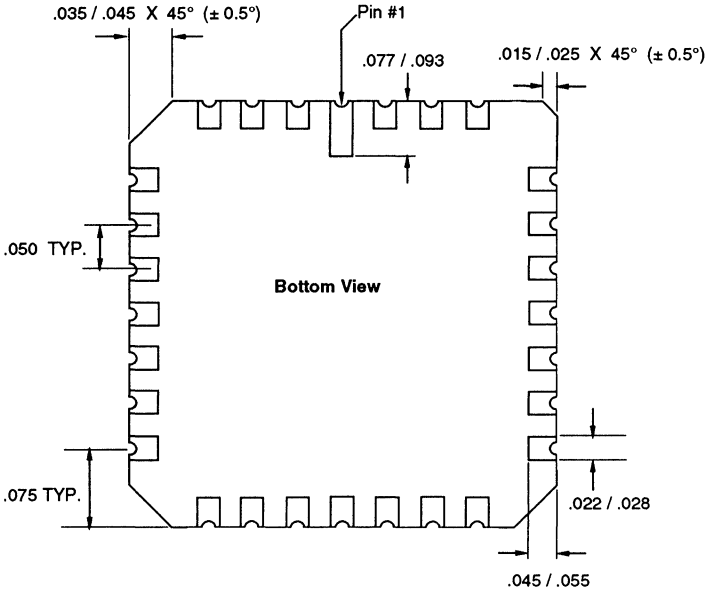
28-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



28-Pin LCC

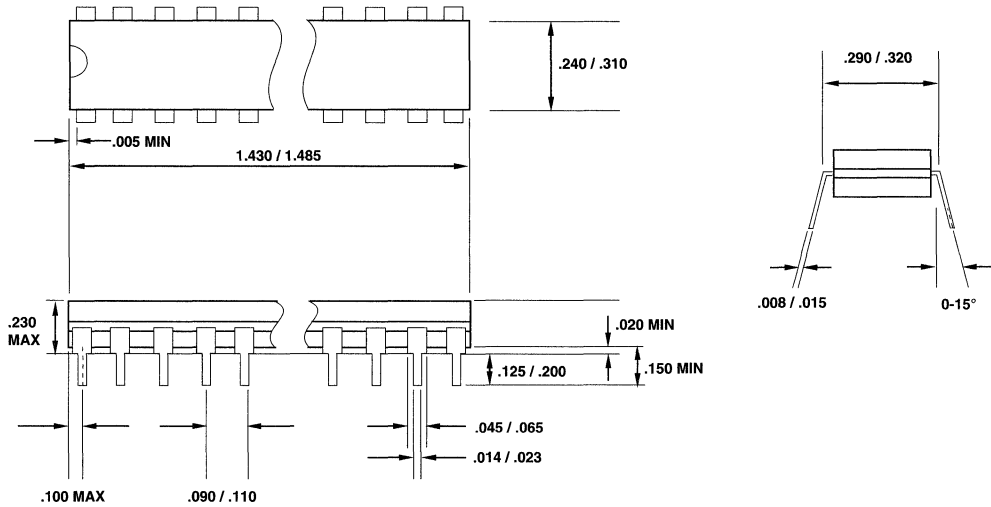
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Package Diagrams

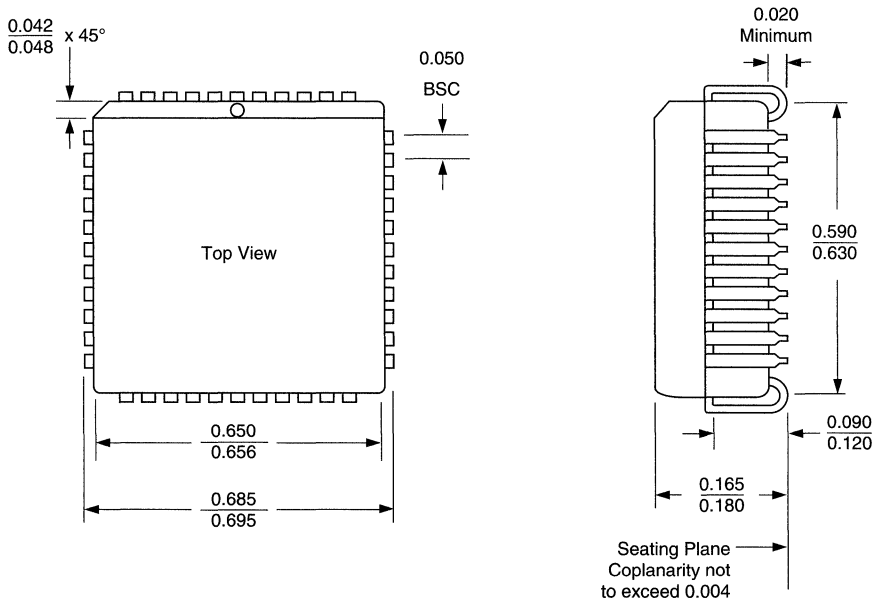
28-Pin (300 MIL) Cerdip

Dimensions in Inches MIN. / MAX.



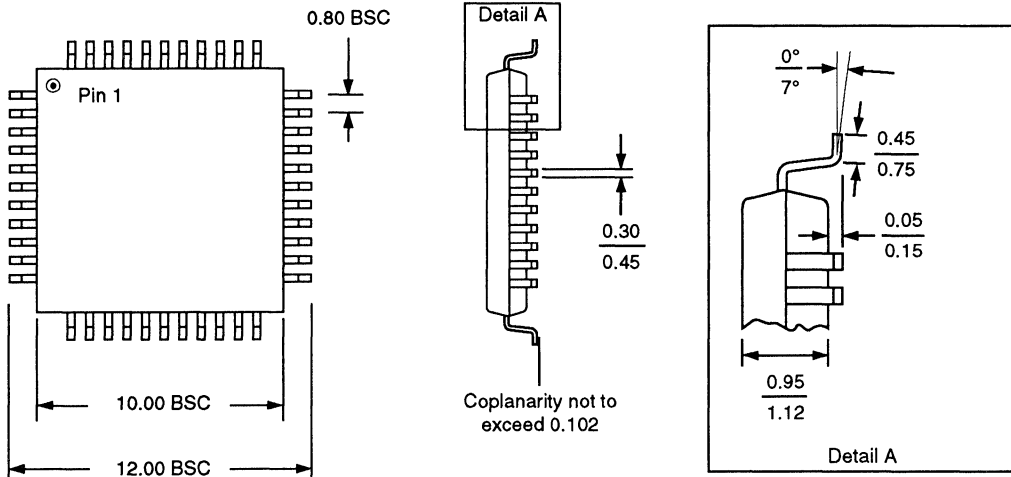
44-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



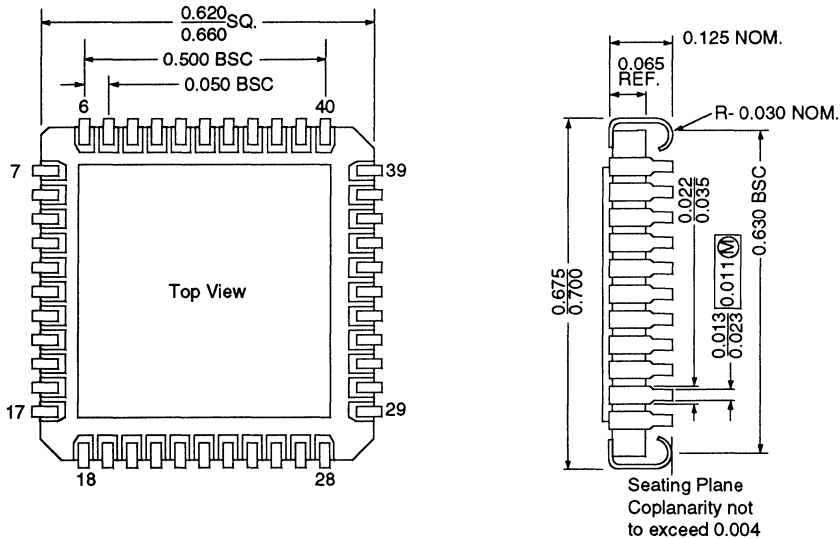
44-Pin TQFP Package

Dimensions in Millimeters MIN. / MAX.



44-Pin JLCC Package

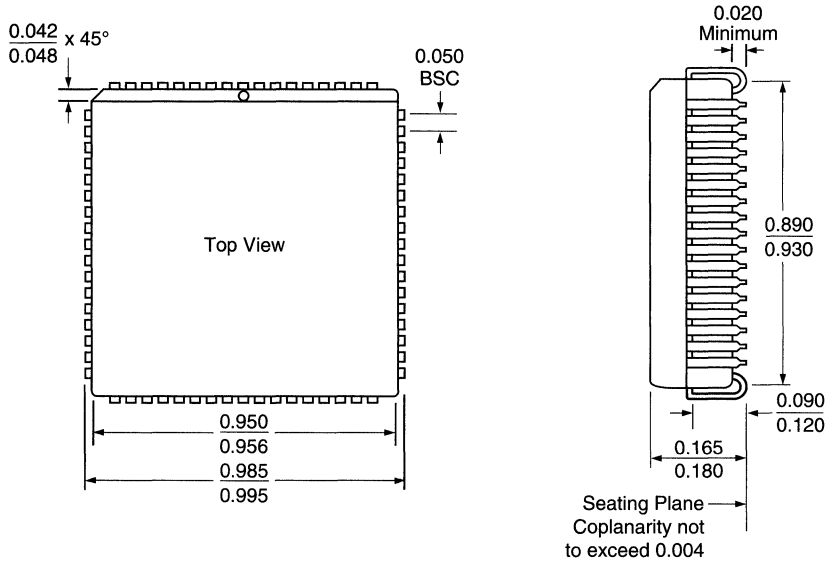
Dimensions in Inches MIN. / MAX.



Package Diagrams

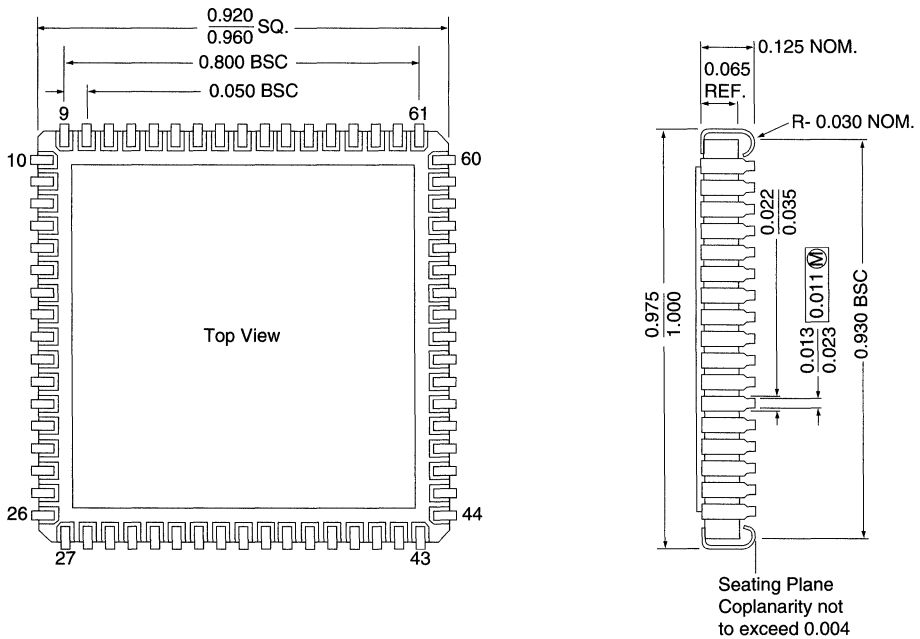
68-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



68-Pin JLCC Package

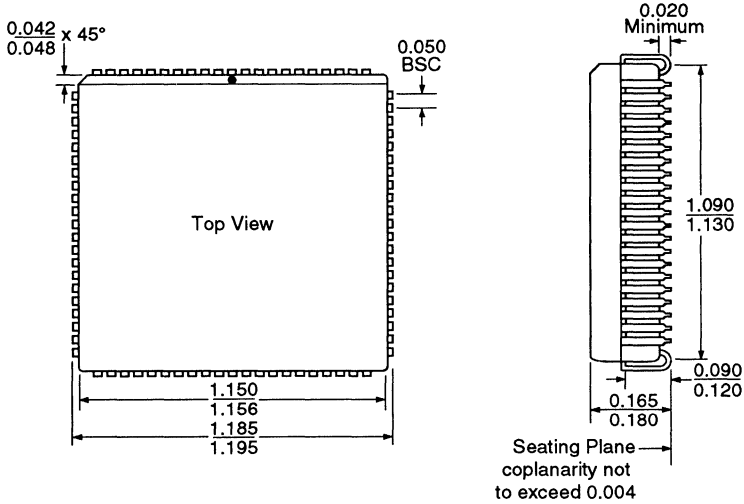
Dimensions in Inches MIN. / MAX.



Package Diagrams

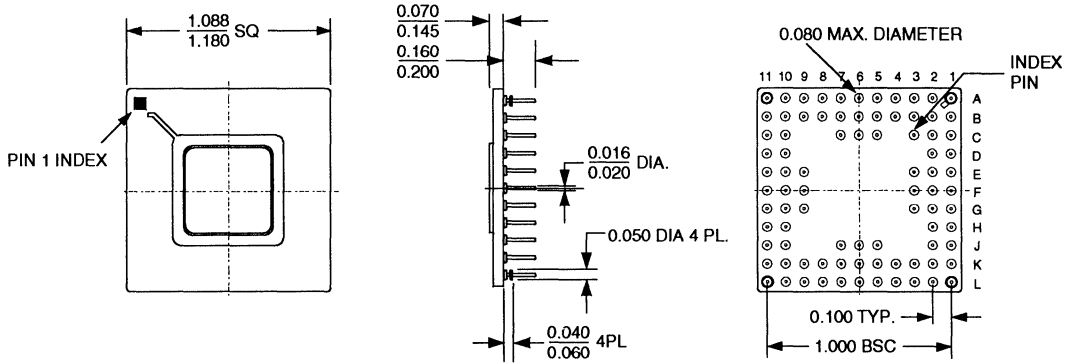
84-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



84-Pin CPGA Package

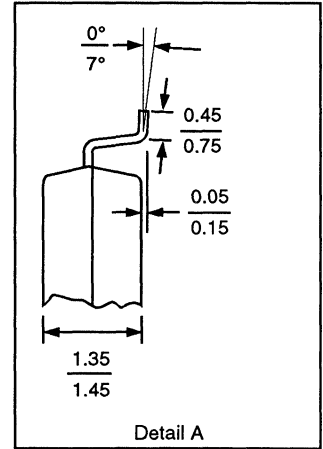
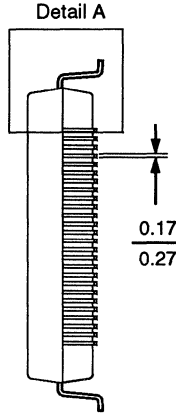
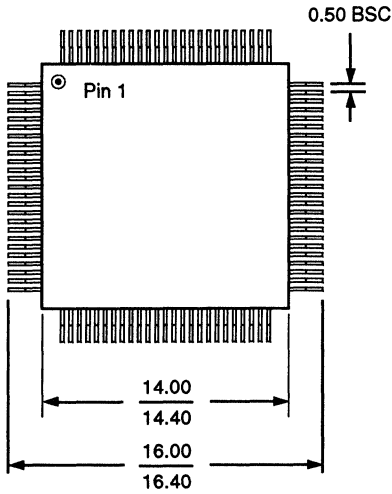
Dimensions in Inches MIN. / MAX.



Package Diagrams

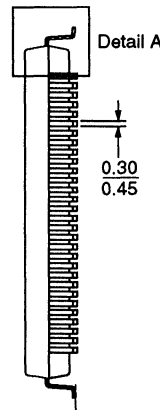
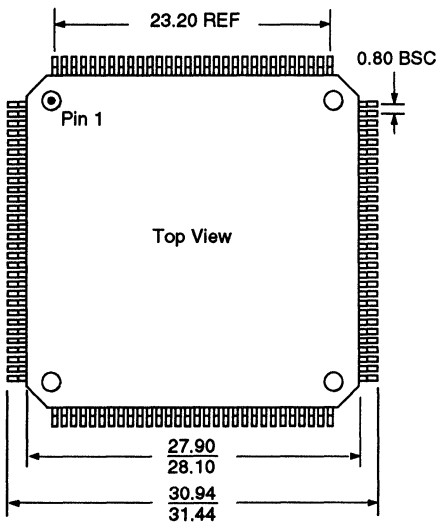
100-Pin TQFP Package

Dimensions in Millimeters MIN. / MAX.

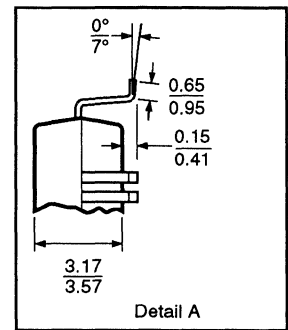


120-Pin PQFP Package

Dimensions in Millimeters MIN. / MAX.

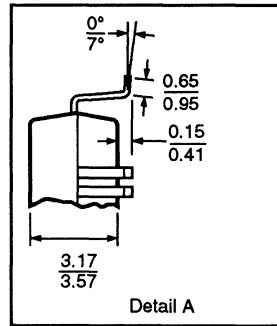
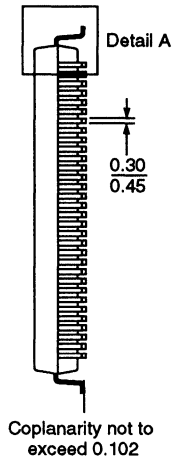
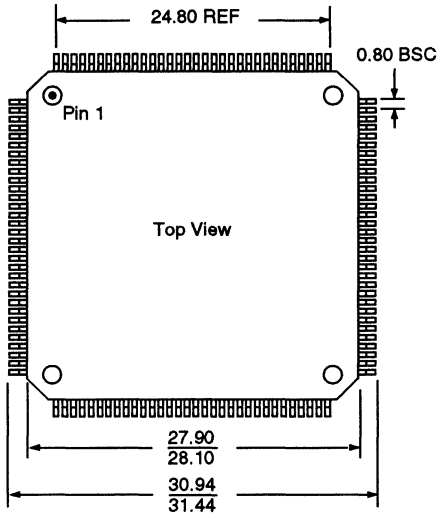


Coplanarity not to exceed 0.102



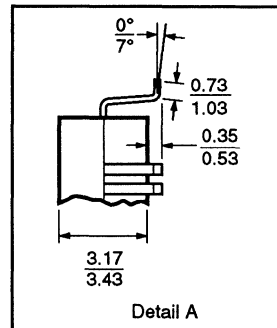
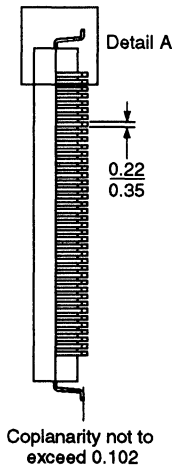
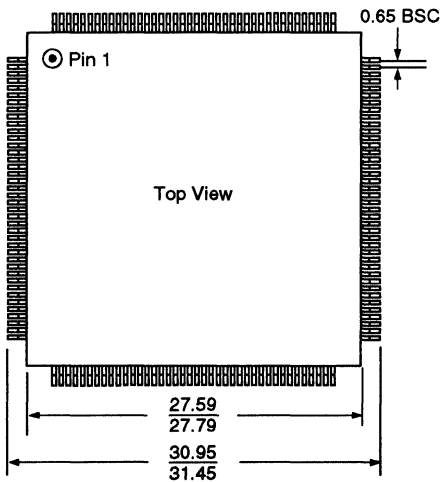
128-Pin PQFP Package

Dimensions in Millimeters MIN. / MAX.



160-Pin MQUAD Package

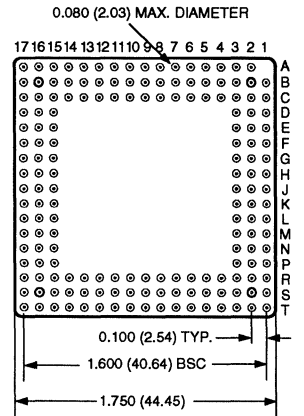
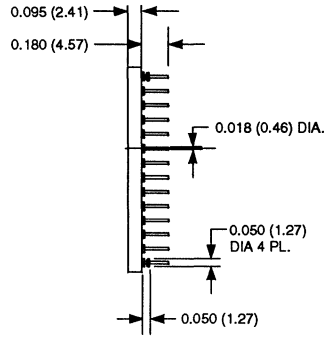
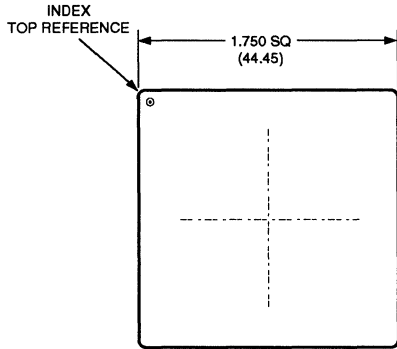
Dimensions in Millimeters MIN. / MAX.



Package Diagrams

167-Pin CPGA Package

Dimensions in Inches MIN. / MAX.



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