INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8152F / IT8152G

Advanced RISC-to-PCI Companion Chip

Preliminary Specification V0.3.4

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Revision History

Section	Revision	Page No.
1, 2	• Remove the next generation xScale CPU support.	1, 3
5	• The SDCLK attribute was revised from OD12 to OT24 in Table 5-2.	17
	• The OT24 description was added in I/O cell section.	22
7	• The PCICR default was revised to 00000168h in Table 7-1.	32
	• Bit 0 description was revised in section 7.2.1 SDRAM Control Register.	33
	• The default value of bit 7 was revised to 0 in section 7.2.2 PCI Slave Control Register. • The default value of bit 3 was revised to 1000 in section 7.2.2 PCI Slave Control Register.	34

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1. Features

- **CPU Interface**
  - Supports INTEL StrongArm Series SA1110 32-bit RISC microprocessor interface

- **Shared SDRAM Controller**
  - Supports 16Mb, 64Mb, 128Mb, 256Mb SDRAM
  - Supports up to 64MB Memory
  - 32-bit data bus interface
  - Supports one bank of SDRAM shared with SA1110 microprocessor interface SDRAM controller
  - Provides deep levels of PCI to SDRAM buffers for burst transfer
  - Up to 96 MHz bus operation

- **PCI Bus Controller**
  - 32-bit data bus interface
  - Supports PCI rev. 2.1 specification
  - Provides CPU to PCI buffers for burst transfer
  - PCI bus arbiter built in
  - Supports up to 4 individual external bus master devices
  - Supports CLKRUN# signal function
  - 33 MHz bus operation

- **Interrupt Controller**
  - Supports one maskable interrupt to RISC processor
  - Interrupt order is controlled by software
  - Registers support interrupts masking and unmasking

- **Chaining DMA Controller**
  - Four independent software DMA channels
  - Supports chaining mode and non-chaining mode
  - Supports both PCI memory address and I/O address
  - Supports rotating and fixed priority types
  - Supports DMA transfers of unaligned address

- **Timers**
  - 4-channel 24-bit auto-reloaded timer with pre-scale (1,1/16,1/256) for dividing CPU clock
  - Supports the interrupt generation whenever the timer's count reaches 0

- **Low Pin Count (LPC) Host Controller**
  - Compliant with Intel LPC Interface Specification Rev. 1.0 (Sept. 29, 1997)
  - Supports Serial IRQ Protocol
  - Shared with GPIO pins

- **Digital AC'97 Controller**
  - Directly interfaced to AC97 CODEC for controlling voice data to the speaker or from the microphone

- **USB Host Controller**
  - Supports two USB ports
  - Supports device bandwidth of 12 Mbps or 1.5 Mbps
  - Supports power management mode to protect USB Bus power, and overcurrent detector to protect USB bus from abnormal overcurrent load
  - Fully compatible with USB specification version 1.1 and register compatible with OHCI specification version 1.0 issued by Microsoft, Compaq and NS

- **UART**
  - Supports TXD and RXD signals for serial data transfer, it is 16550 mode compatible

- **General Purpose I/O (GPIO) Function**
  - GPIO pins can be programmed as inputs, outputs, or as interrupt inputs
  - Interrupt events can be independently programmed to rising edge or falling edge trigger
  - Maximum 8 bits for GPIO functions

- **Clock Generator and PLL**
  - Provides a PLL from 12 MHz to 96 MHz for SDRAM controller
  - Provides a PLL from 12 MHz to 33 MHz for PCI bus controller
  - Clock generator and PLL support STANDBY mode

- **Power Management**
  - Software controllable power management
  - Intelligent Power management to reduce power consumption
  - System wake up through interrupt, GPIO pins

- **Package: 208-pin PQFP**
  208-pin LBGA

2. General Description

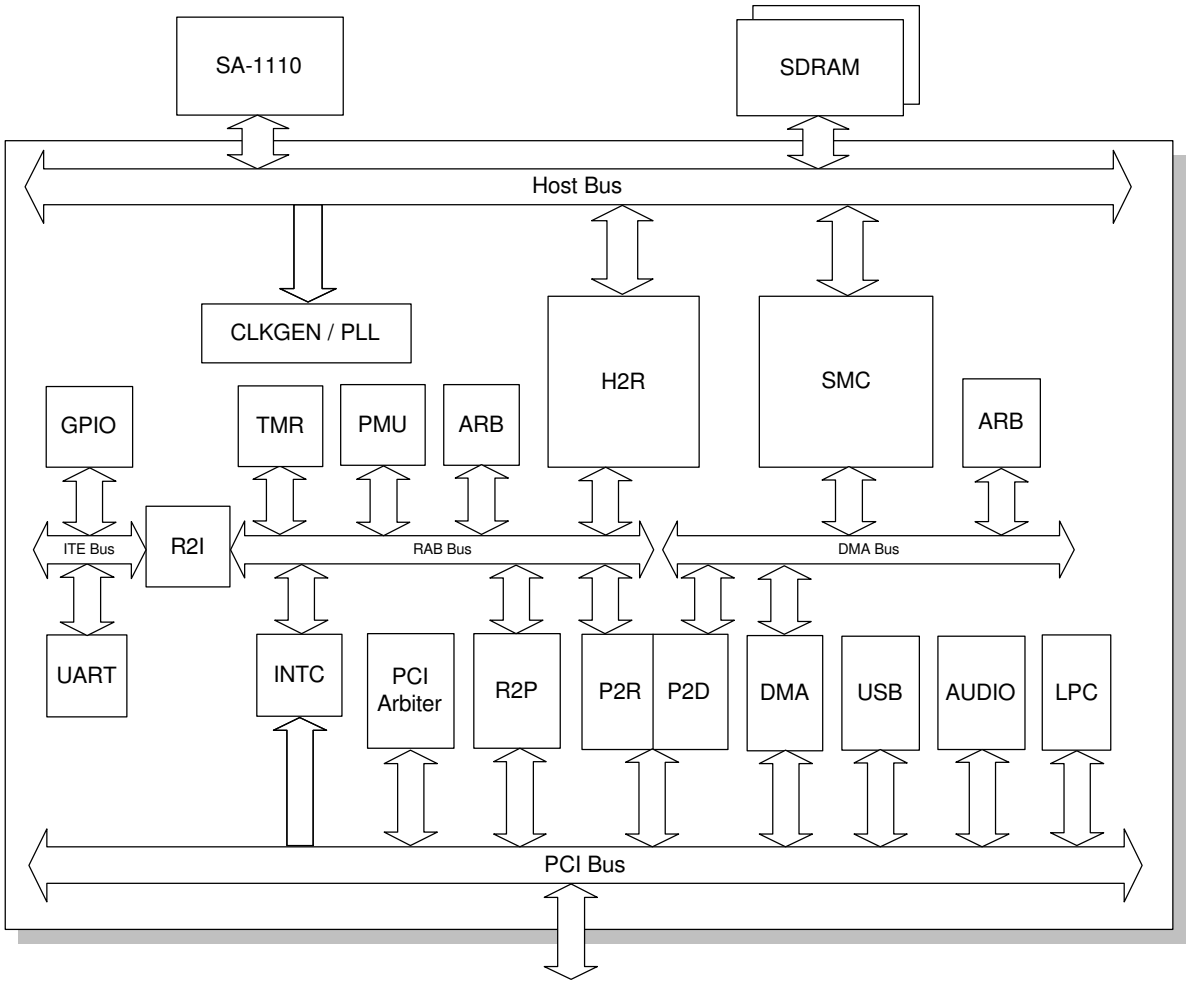
The IT8152, an advanced RISC-to-PCI companion chip that supports SA1110 32-bit RISC microprocessor interface, is especially designed for the main applications in Datacomm, Telecomm, and Internet Appliances and Networking devices. This companion chip interfaces directly to RISC processors, and provides a bridge to link host bus and PCI bus. It also provides a Shared Memory (SDRAM) Controller, Low Pin Count (LPC) Host Controller, Interrupt Controller, DMA Controller, Timers, USB Host Controller, Digital AC'97 Controller, GPIO Controller and Power Management.

Paired with Intel's SA1110 RISC microprocessor interface, the IT8152 provides a low cost, high performance host to PCI bridge function for any system applications in Datacomm/Telecomm products.

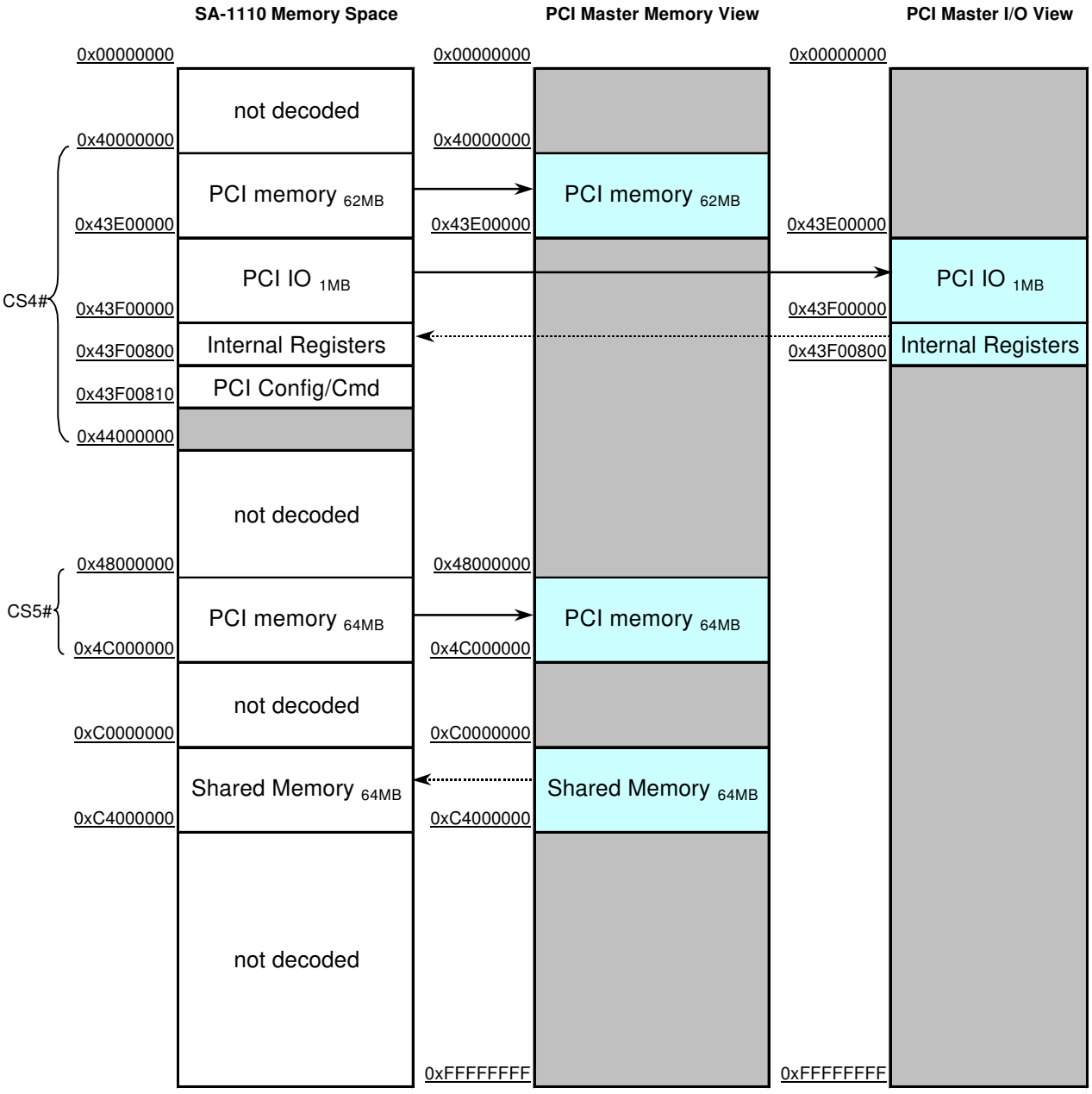
The IT8152 is available in two packages: 208-pin PQFP and 208-pin LBGA.

3. System Block Diagram

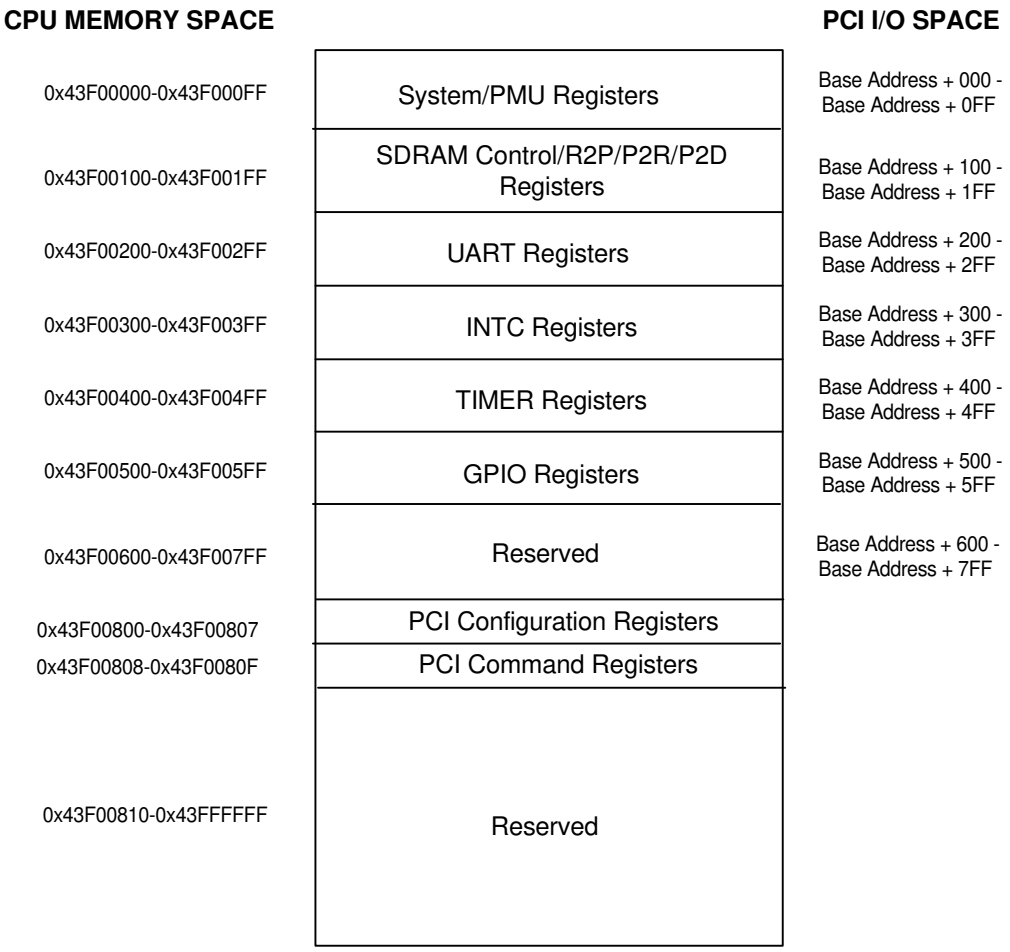
3.1 Block Diagram



3.2 System Address Space

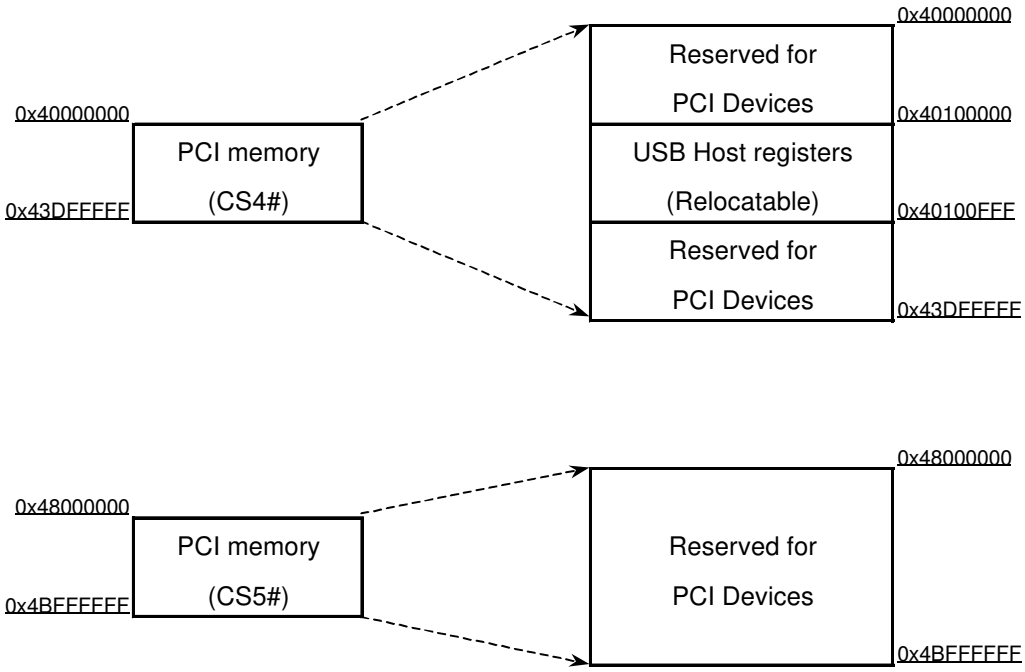


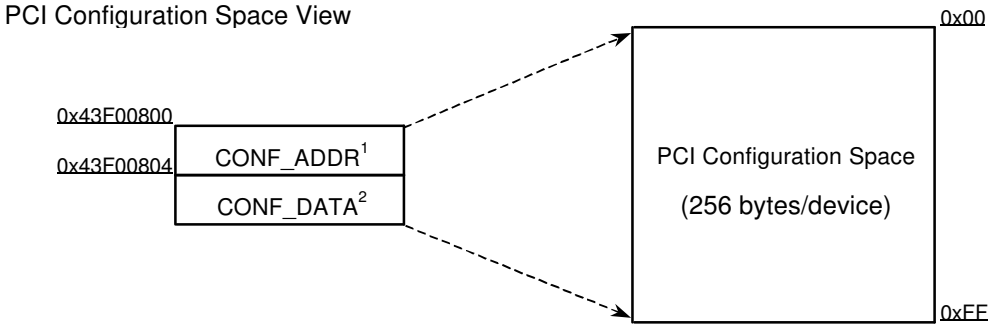
3.3 Internal Registers Address Map



Note : The default PCI I/O base address for internal registers is 0x43F00000.

3.4 PCI Memory Space and Configuration Space Map

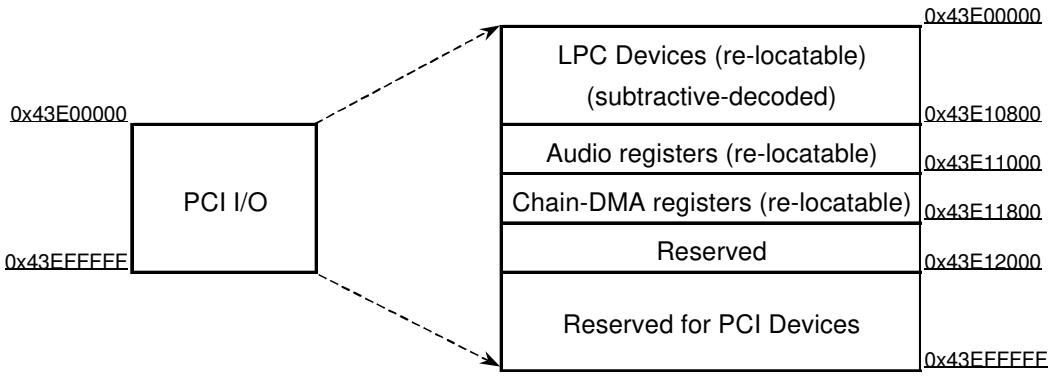




Notes:

1. PCI Configuration Address register
2. PCI Configuration Data register

3.5 PCI IO Space Map



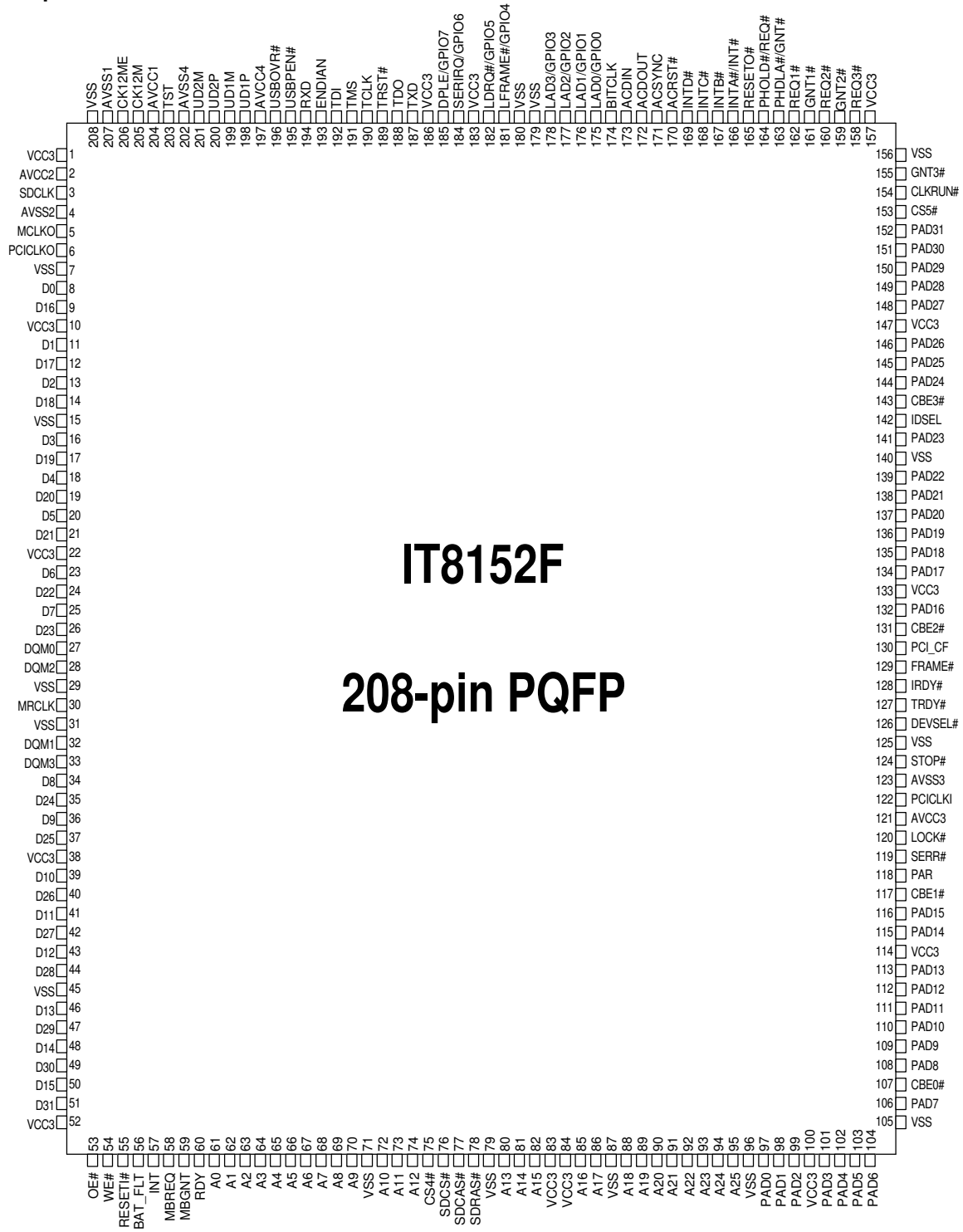
Notes:

The IT8152 is a multi-function (PCI) device, i.e., only one IDSEL is provided. Therefore, for a PCI configuration cycle, all functions in the PCI bus must decode the function numbers in addition to IDSEL. The function numbers are assigned as follows:

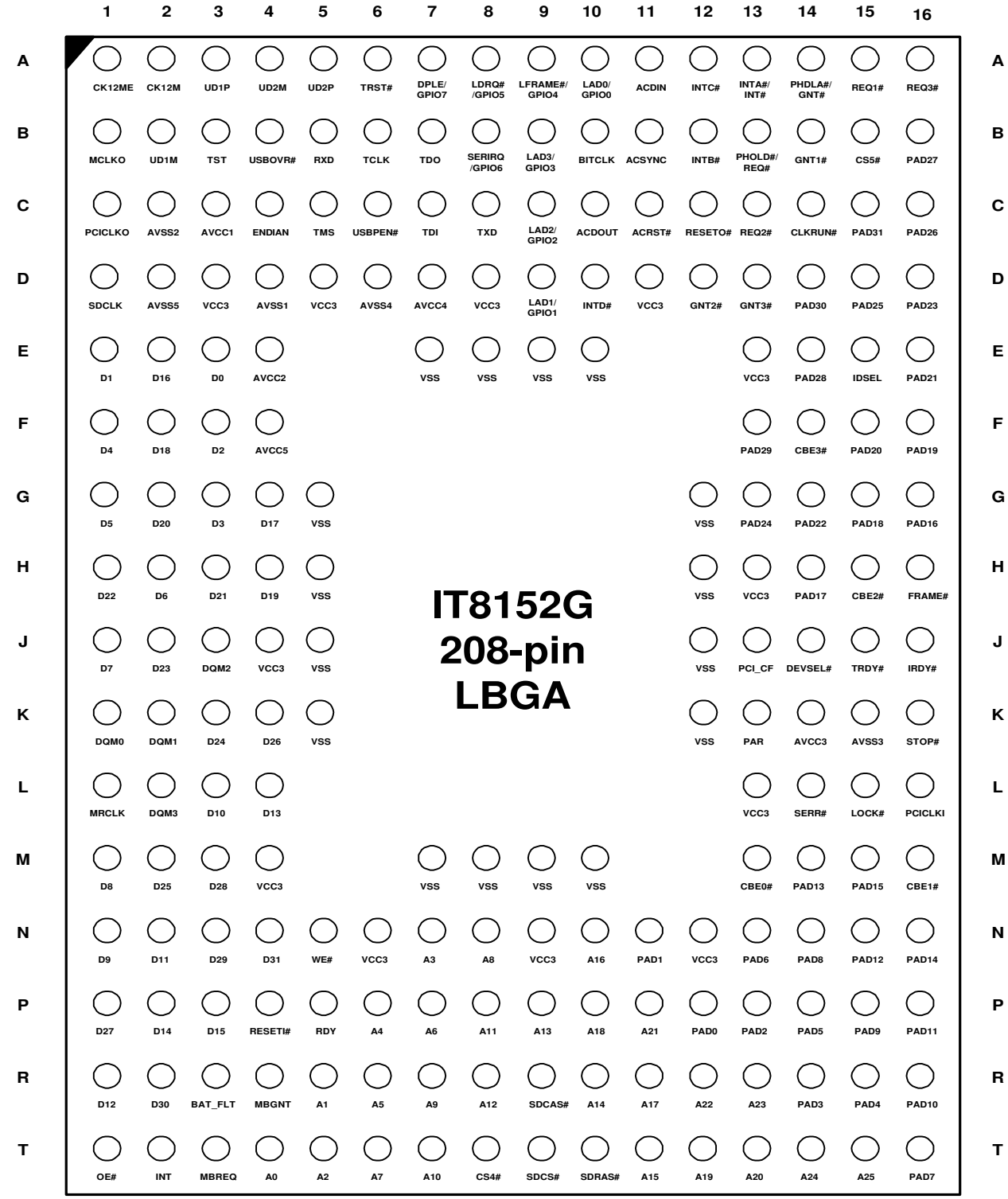
1. The internal registers (PCI bridge, UART, INTC, PMU, TIMER, GPIO that are hooked in the RAB bus) is function 0.
2. The CDMA Controller is function 1.
3. The PCI-to-LPC Bridge is function 2.
4. The Audio Digital Controller is function 3.
5. The USB Host Controller is function 4.

4. Pin Configuration

4.1 208-pin PQFP



4.2 208-pin LBGA (Top View)



4.3 208-pinLBGA (Bottom View)

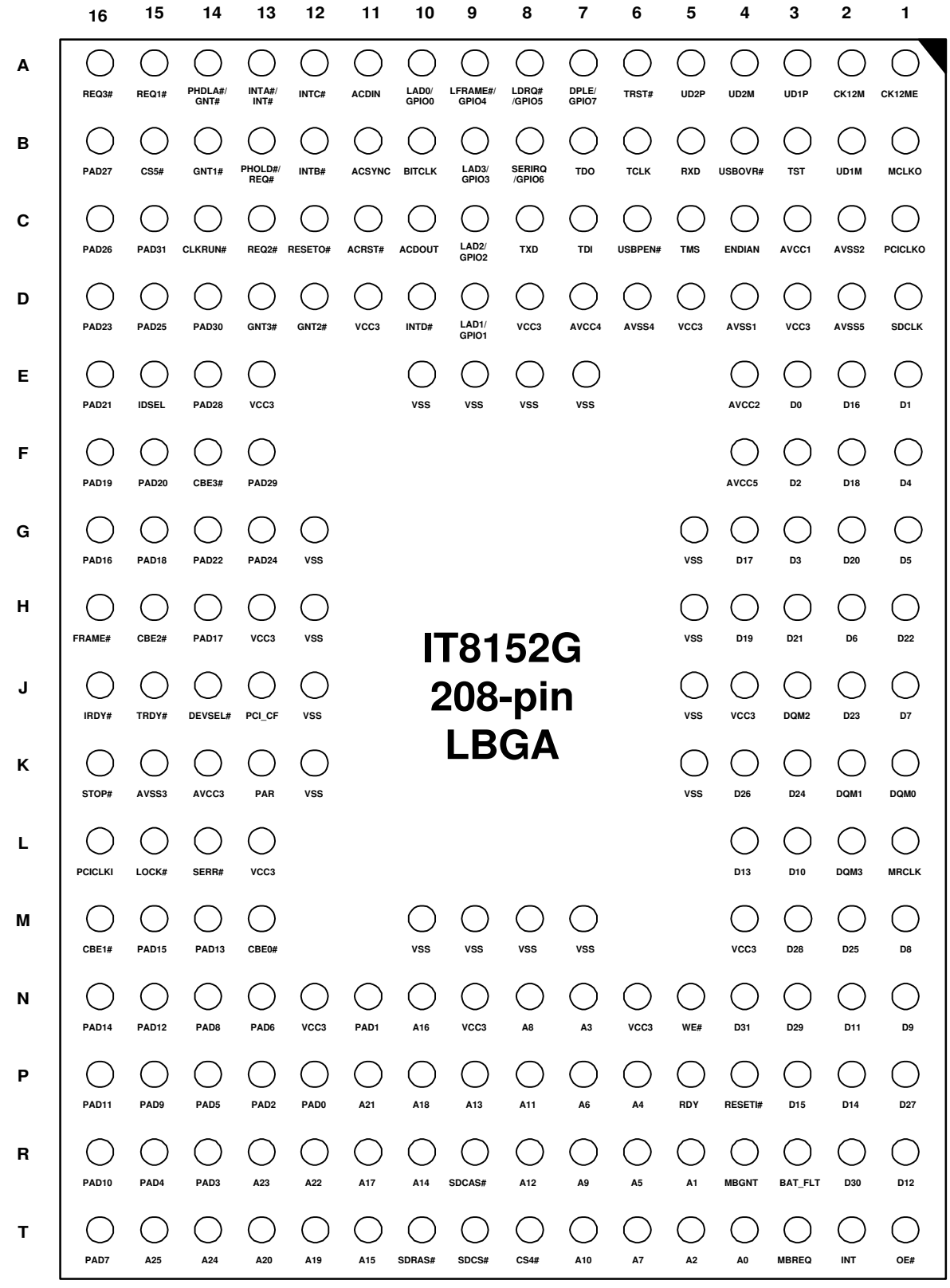


Table 4-1. Pins Listed in Numeric Order for 208-Pin PQFP (IT8152F)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC3	53	OE#	105	VSS	157	VCC3
2	AVCC2	54	WE#	106	PAD7	158	REQ3#
3	SDCLK	55	RESETI#	107	CBE0#	159	GNT2#
4	AVSS2	56	BAT_FLT	108	PAD8	160	REQ2#
5	MCLKO	57	INT	109	PAD9	161	GNT1#
6	PCICLKO	58	MBREQ	110	PAD10	162	REQ1#
7	VSS	59	MBGNT	111	PAD11	163	PHDLA#/GNT#
8	D0	60	RDY	112	PAD12	164	PHOLD#/REQ#
9	D16	61	A0	113	PAD13	165	RESETO#
10	VCC3	62	A1	114	VCC3	166	INTA#INT#
11	D1	63	A2	115	PAD14	167	INTB#
12	D17	64	A3	116	PAD15	168	INTC#
13	D2	65	A4	117	CBE1#	169	INTD#
14	D18	66	A5	118	PAR	170	ACRST#
15	VSS	67	A6	119	SERR#	171	ACSYNC
16	D3	68	A7	120	LOCK#	172	ACDOUT
17	D19	69	A8	121	AVCC3	173	ACDIN
18	D4	70	A9	122	PCICLKI	174	BITCLK
19	D20	71	VSS	123	AVSS3	175	LAD0/GPIO0
20	D5	72	A10	124	STOP#	176	LAD1/GPIO1
21	D21	73	A11	125	VSS	177	LAD2/GPIO2
22	VCC3	74	A12	126	DEVSEL#	178	LAD3/GPIO3
23	D6	75	CS4#	127	TRDY#	179	VSS
24	D22	76	SDCS#	128	IRDY#	180	VSS
25	D7	77	SDCAS#	129	FRAME#	181	LFRAME#/GPIO4
26	D23	78	SDRAS#	130	PCI_CF	182	LDRQ#/GPIO5
27	DQM0	79	VSS	131	CBE2#	183	VCC3
28	DQM2	80	A13	132	PAD16	184	SERIRQ/GPIO6
29	VSS	81	A14	133	VCC3	185	DPLE/GPIO7
30	MRCLK	82	A15	134	PAD17	186	VCC3
31	VSS	83	VCC3	135	PAD18	187	TXD
32	DQM1	84	VCC3	136	PAD19	188	TDO
33	DQM3	85	A16	137	PAD20	189	TRST#
34	D8	86	A17	138	PAD21	190	TCLK
35	D24	87	VSS	139	PAD22	191	TMS
36	D9	88	A18	140	VSS	192	TDI
37	D25	89	A19	141	PAD23	193	ENDIAN
38	VCC3	90	A20	142	IDSEL	194	RXD
39	D10	91	A21	143	CBE3#	195	USBPEN#
40	D26	92	A22	144	PAD24	196	USBOVR#
41	D11	93	A23	145	PAD25	197	AVCC4
42	D27	94	A24	146	PAD26	198	UD1P
43	D12	95	A25	147	VCC3	199	UD1M
44	D28	96	VSS	148	PAD27	200	UD2P
45	VSS	97	PAD0	149	PAD28	201	UD2M
46	D13	98	PAD1	150	PAD29	202	AVSS4
47	D29	99	PAD2	151	PAD30	203	TST
48	D14	100	VCC3	152	PAD31	204	AVCC1
49	D30	101	PAD3	153	CS5#	205	CK12M
50	D15	102	PAD4	154	CLKRUN#	206	CK12ME
51	D31	103	PAD5	155	GNT3#	207	AVSS1
52	VCC3	104	PAD6	156	VSS	208	VSS

Table 4-2. Pins Listed in Numeric Order for 208-Pin LBGA (IT8152G)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	CK12ME	D5	VCC3	J1	D7	N13	PAD6
A2	CK12M	D6	AVSS4	J2	D23	N14	PAD8
A3	UD1P	D7	AVCC4	J3	DQM2	N15	PAD12
A4	UD2M	D8	VCC3	J4	VCC3	N16	PAD14
A5	UD2P	D9	LAD1/GPIO1	J5	VSS	P1	D27
A6	TRST#	D10	INTD#	J12	VSS	P2	D14
A7	DPLE/GPIO7	D11	VCC3	J13	PCI_CF	P3	D15
A8	LDRQ#/GPIO5	D12	GNT2#	J14	DEVSEL#	P4	RESETI#
A9	LFRAME#/GPIO4	D13	GNT3#	J15	TRDY#	P5	RDY
A10	LAD0/GPIO0	D14	PAD30	J16	IRDY#	P6	A4
A11	ACDIN	D15	PAD25	K1	DQM0	P7	A6
A12	INTC#	D16	PAD23	K2	DQM1	P8	A11
A13	INTA#/INT#	E1	D1	K3	D24	P9	A13
A14	PHDLA#/GNT#	E2	D16	K4	D26	P10	A18
A15	REQ1#	E3	D0	K5	VSS	P11	A21
A16	REQ3#	E4	AVCC2	K12	VSS	P12	PAD0
B1	MCLKO	E7	VSS	K13	PAR	P13	PAD2
B2	UD1M	E8	VSS	K14	AVCC3	P14	PAD5
B3	TST	E9	VSS	K15	AVSS3	P15	PAD9
B4	USBOVR#	E10	VSS	K16	STOP#	P16	PAD11
B5	RXD	E13	VCC3	L1	MRCLK	R1	D12
B6	TCLK	E14	PAD28	L2	DQM3	R2	D30
B7	TDO	E15	IDSEL	L3	D10	R3	BAT_FLT
B8	SERIRQ/GPIO6	E16	PAD21	L4	D13	R4	MBGNT
B9	LAD3/GPIO3	F1	D4	L13	VCC3	R5	A1
B10	BITCLK	F2	D18	L14	SERR#	R6	A5
B11	ACSYNC	F3	D2	L15	LOCK#	R7	A9
B12	INTB#	F4	AVCC5	L16	PCICLKI	R8	A12
B13	PHOLD#/REQ#	F13	PAD29	M1	D8	R9	SDCAS#
B14	GNT1#	F14	CBE3#	M2	D25	R10	A14
B15	CS5#	F15	PAD20	M3	D28	R11	A17
B16	PAD27	F16	PAD19	M4	VCC3	R12	A22
C1	PCICLKO	G1	D5	M7	VSS	R13	A23
C2	AVSS2	G2	D20	M8	VSS	R14	PAD3
C3	AVCC1	G3	D3	M9	VSS	R15	PAD4
C4	ENDIAN	G4	D17	M10	VSS	R16	PAD10
C5	TMS	G5	VSS	M13	CBE0#	T1	OE#
C6	USBPEN#	G12	VSS	M14	PAD13	T2	INT
C7	TDI	G13	PAD24	M15	PAD15	T3	MBREQ
C8	TXD	G14	PAD22	M16	CBE1#	T4	A0
C9	LAD2/GPIO2	G15	PAD18	N1	D9	T5	A2
C10	ACDOUT	G16	PAD16	N2	D11	T6	A7
C11	ACRST#	H1	D22	N3	D29	T7	A10
C12	RESETO#	H2	D6	N4	D31	T8	CS4#
C13	REQ2#	H3	D21	N5	WE#	T9	SDCS#
C14	CLKRUN#	H4	D19	N6	VCC3	T10	SDRAS#
C15	PAD31	H5	VSS	N7	A3	T11	A15
C16	PAD26	H12	VSS	N8	A8	T12	A19
D1	SDCLK	H13	VCC3	N9	VCC3	T13	A20
D2	AVSS5	H14	PAD17	N10	A16	T14	A24
D3	VCC3	H15	CBE2#	N11	PAD1	T15	A25
D4	AVSS1	H16	FRAME#	N12	VCC3	T16	PAD7

5. IT8152F/IT8152G Pin Descriptions

Table 5-1. Pin Descriptions of Test Mode Select

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
Test Mode Select (3.3V CMOS I/F)				
TST	203	B3	I	***Test Mode Enable.*** 0: Disabled. 1: Enabled.

Table 5-2. Pin Descriptions of Host Bus Interface

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
Host Bus Interface (3.3V CMOS I/F)				
MRCLK	30	L1	I	***Memory Read Access Clock Reference Input.***
SDCLK	3	D1	OT24	***Shared Memory Clock Output to SDRAM.*** This clock will be floating, if the chip is not accessing SDRAM right now.
MCLKO	5	B1	O12	***Memory Clock Output for Adjusting Clock Skew.*** This clock is always running.
RESETI#	55	P4	IK	***Power On Reset.***
RESETO#	165	C12	O8	***System Reset Output for All System Reset.***
A[25:0]	95-88, 86, 85, 82-80, 74-72, 70-61	T15, T14, R13, R12, P11, T13, T12, P10, R11, N10, T11, R10, P9, R8, P8, T7, R7, N8, T6, P7, R6, P6, N7, T5, R5, T4	IO12	***26-bit System Address Bus.*** The A[24:10] will be as output pins when the internal DMA or external PCI master want to access the SDRAM.
D[31:0]	51, 49, 47, 44, 42, 40, 37, 35, 26, 24, 21, 19, 17, 14, 12, 9, 50, 48, 46, 43, 41, 39, 36, 34, 25, 23, 20, 18, 16, 13, 11, 8	N4, R2, N3, M3, P1, K4, M2, K3, J2, H1, H3, G2, H4, F2, G4, E2, P3, P2, L4, R1, N2, L3, N1, M1, J1, H2, G1, F1, G3, F3, E1, E3	IO12	***32-bit System Data Bus.***
OE#	53	T1	I	***Memory Output Enable of CPU.*** The output enable is active when the CPU read accesses right now.
WE#	54	N5	IO12	***Memory Write Enable.*** When the ASIC is the slave of CPU write transfer, the pin is input signal and it pairs with DQM[3:0] to specify byte write. On the other hand, when the ASIC writes data to SDRAM, the pin is output signal and is connected to WE# pin of SDRAM.
DQM[3:0]	33, 28, 32, 27	L2, J3, K2, K1	IO12	***Data Output Mask Enable for SDRAM Write Transfer.***
CS4#	75	T8	I	***Chip Select 4 for Enabling All Access.***
CS5#	153	B15	I	***Chip Select 5 for Enabling All Access.***
RDY	60	P5	OT12	***Ready Signal for CPU.***

Table 5-2. Pin Descriptions of Host Bus Interface (cont'd)

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
Host Bus Interface (3.3V CMOS I/F)				
MBREQ	58	T3	O8	***Bus Request to CPU.***
MBGNT	59	R4	I	***Bus Grant from CPU.***
SDCS#	76	T9	OT12	***SDRAM Chip Select.***
SDRAS#	78	T10	OT12	***SDRAM Row Address Strobe.***
SDCAS#	77	R9	OT12	***SDARM Column Address Strobe.***
INT	57	T2	O8	***Interrupt to Request to CPU.***
ENDIAN	193	C4	I	***Big Endian Enable*** Set the addressing mode of CPU interface to either Big Endian or Little Endian. 0: Little Endian. 1: Big Endian.

Table 5-3. Pin Descriptions of PCI Bus Interface

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
PCI Bus Interface (3.3V CMOS I/F, 5V tolerant)				
PCICLKI	122	L16	PI	***PCI Clock Input.***
PCICLKO	6	C1	O16	***PCI Clock Output.***
PAD[31:0]	152-148, 146-144, 141, 139-134, 132, 116,115, 113-108, 106, 104-101, 99-97	C15, D14, F13, E14, B16, C16, D15, G13, D16, G14, E16, F15, F16, G15, H14, G16, M15, N16, M14, N15, P16, R16, P15, N14, T16, N13, P14, R15, R14, P13, N11, P12	PIO	***PCI Address/Data Bus 31-0.***
CBE[3:0]#	143,131, 117,107	F14, H15, M16, M13	PIO	***PCI C/BE[3:0]# Signal.*** PCI C/BE# Bus 3-0 signals.
FRAME#	129	H16	PIO	***PCI Bus FRAME# Signal.***
LOCK#	120	L15	PIO	***PCI Bus LOCK# Signal.***
IRDY#	128	J16	PIO	***PCI Bus IRDY# Signal.***
TRDY#	127	J15	PIO	***PCI Bus TRDY# Signal.***
STOP#	124	K16	PIO	***PCI Bus STOP# Signal.***
DEVSEL#	126	J14	PIO	***PCI Bus DEVSEL# Signal.***
IDSEL	142	E15	PI	***PCI Bus Initialization Device Select.***
SERR#	119	L14	PI	***PCI Bus SERR# signal.***
PAR	118	K13	PIO	***PCI Bus Parity Bit.***

Table 5-3. Pin Descriptions of PCI Bus Interface (cont'd)

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
PCI Bus Interface (3.3V CMOS I/F, 5V tolerant)				
PHOLD#/ REQ#	164	B13	PI/ PO	***PCI HOLD for Intel Chipset/PCI Bus Request.*** When the PCI_CF is tied to high, the ASIC is active as PCI device, the pin is the PCI bus request output to PCI arbiter. Contrarily, the PCI CF is tied to low, the PCI arbiter is in the ASIC, the pin is the PCI HOLD input for bus request of Intel Chipset.
PHDLA#/ GNT#	163	A14	PO/ PI	***PCI HOLD Acknowledge for Intel Chipset/PCI Bus Grant.*** When the PCI_CF is tied to high, the ASIC is active as PCI device, the pin is the PCI bus grant input from PCI arbiter. Contrarily, the PCI_CF is tied to low, the PCI arbiter is in the ASIC, the pin is the PCI HOLD Acknowledge output to Intel Chipset.
REQ[3:1]#	158, 160, 162	A16, C13, A15	PI	***PCI Master Request [3:1].***
GNT[3:1]#	155, 159,161	D13, D12, B14	PO	***PCI Master Grant [3:1].***
INTA#/INT#	166	A13	PI/ PO	***PCI Bus Interrupt Request A/PCI Bus Interrupt Request.*** When the PCI_CF is tied to high, the ASIC is active as PCI device, the pin is the PCI bus interrupt request output to PCI master. Contrarily, the PCI_CF is tied to low, the PCI arbiter is in the ASIC, the pin is the PCI interrupt request A input from external PCI device.
INTB#	167	B12	PI	***PCI Bus Interrupt Request B.***
INTC#	168	A12	PI	***PCI Bus Interrupt Request C.***
INTD#	169	D10	PI	***PCI Bus Interrupt Request D.***
CLKRUN#	154	C14	IOD8	***PCI Bus CLKRUN# Signal.*** This pin does not support 5V tolerant. It only supports 3.3V CMOS I/F.
PCI_CF	130	J13	I	***PCI Device Function Enable.*** When the pin is tied to high, the ASIC is active as PCI device.

Table 5-4. Pin Descriptions of LPC Host Controller/GPIO Interface

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
LPC Host Controller/GPIO Interface (3.3V CMOS I/F, 5V tolerant)				
LAD3-0 /GPIO3-0	178-175	B9, C9, D9, A10	IO12 / IO12	***Multiplexed Command, Address and Data for LPC/GPIO Bits 3-0.*** These are multi-function pins. They can be controlled by Port Control Register (GPxCnR). Please refer to General Purpose I/O Port chapter for details. When the 'function 2"is set, the corresponding LAD3-0 function is enabled. It is used as multiplexed Command, Address and Data signals for LPC function. Otherwise, the bits 3-0 function of General Purpose I/O port register is enabled.

Table 5-4. Pin Descriptions of LPC Host Controller/GPIO Interface (cont'd)

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
LPC Host Controller/GPIO Interface (3.3V CMOS I/F, 5V tolerant)				
LFRAME#/ GPIO4	181	A9	O12/ IO12	***Frame Signal for LPC/GPIO Bit 4.*** This is a multi-function pin. It can be controlled by Port Control Register (GPxCnR). Please refer to General Purpose I/O Port chapter for details. When the 'function 2"is set, the corresponding LFRAME# function is enabled. It is used to indicate the start of a new cycle, and the termination of a broken cycle for LPC function. Otherwise, the bit 4 function of General Purpose I/O port register is enabled.
LDRQ#/ GPIO5	182	A8	I/ IO12	***Encoded DMA and Bus Master Request for LPC/GPIO Bit 5.*** This is a multi-function pin. It can be controlled by Port Control Register (GPxCnR). Please refer to General Purpose I/O Port chapter for details. When the 'function 2"is set, the corresponding LDRQ# function is enabled for LPC function. Otherwise, the bit 5 function of General Purpose I/O port register is enabled.
SERIRQ/ GPIO6	184	B8	IO12/ IO12	***Serialized IRQ for LPC/GPIO Bit 6.*** This is a multi-function pin. It can be controlled by Port Control Register (GPxCnR). Please refer to General Purpose I/O Port chapter for details. When the 'function 2"is set, the corresponding SERIRQ function is enabled for LPC function. Otherwise, the bit 6 function of General Purpose I/O port register is enabled.
DPLE/ GPIO7	185	A7	O12/ IO12	***Debug Port Latch Enable/GPIO Bit 7.*** This is a multi-function pin. It can be controlled by Port Control Register (GPxCnR). Please refer to General Purpose I/O Port chapter for details. When the 'function 2"is set, the corresponding DPLE function is enabled. Otherwise, the bit 7 function of General Purpose I/O port register is enabled.

Table 5-5. Pin Descriptions of UART Port Interface

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
UART Port Interface (3.3V CMOS I/F)				
TXD	187	C8	O8	***Data Output for UART.***
RXD	194	B5	I	***Data Input for UART.***

Table 5-6. Pin Descriptions of Digital AC Link Interface

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
AC-Link Interface (3.3V CMOS I/F)				
BITCLK	174	B10	I	***AC97 CODEC Serial Interface Clock.***
ACDIN	173	A11	I	***AC97 CODEC Seri al Interface Input Data.***
ACDOUT	172	C10	O8	***AC97 CODEC Serial Interface Output Data.***
ACSYNC	171	B11	O8	***AC97 CODEC Serial Interface Synchronous.***
ACRST#	170	C11	O8	***RESET# for AC97 CODEC.***

Table 5-7. Pin Descriptions of USB Host Controller Interface

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
USB Host Controller Interface (3.3V CMOS I/F)				
UD1P	198	A3	UIO	***USB Port 1 D+ Line.***
UD1M	199	B2	UIO	***USB Port 1 D- Line.***
UD2P	200	A5	UIO	***USB Port 2 D+ Line.***
UD2M	201	A4	UIO	***USB Port 2 Data D- Line.***
USBPEN#	195	C6	O8	***USB Power Enable.***
USBOVR#	196	B4	I	***Over Current Detection.*** This input is asserted when the downstream ports exceed their current limitation. This input is used to disable the USB power, and the over-current condition will be reported on the hub and port status register.

Table 5-8. Pin Descriptions of Miscellaneous Signals

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
Miscellaneous (MISC) Signals (3.3V CMOS I/F)				
BAT_FLT	56	R3	IK	***Battery Fault.*** When the signal is asserted, the all functions of this ASIC will be forced to stand-by mode.
CK12M	205	A2	OSCI	***12 MHz Crystal Oscillator Input.***
CK12ME	206	A1	OSCIO	***12 MHz Crystal Oscillator Output.***

Table 5-9. Pin Descriptions of JTAG Interface Signals

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
JTAG Interface Signals				
TDI	192	C7	I	***Test Data Input for JTAG.***
TMS	191	C5	I	***Test Mode Select for JTAG.***
TCLK	190	B6	I	***Test Clock Input for JTAG.***
TRST#	189	A6	I	***Test Reset Signal for JTAG.***
TDO	188	B7	O8	***Test Data Output for JTAG.***

Table 5-10. Pin Descriptions of Power/Ground Signals

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
Power Ground Signals				
VCC3	1, 10, 22, 38, 52, 83, 84, 100, 114, 133, 147, 157, 183, 186	D3, D5, D8, D11, E13, H13, J4, L13, M4, N6, N9, N12	I	***Power Supply of 3.3 V.***
VSS	7, 15, 29, 31, 45, 71, 79, 87, 96, 105, 125, 140, 156, 179, 180, 208	E7-E10, G5, G12, H5, H12, J5, J12, K5, K12, M7-M10	I	***Ground.***
AVCC1	204	C3	I	***Analog VCC for analog PLL.***
AVSS1	207	D4	I	***Analog Ground for analog PLL.***
AVCC2	2	E4	I	***Analog VCC for analog PLL.***
AVSS2	4	C2	I	***Analog Ground for analog PLL.***
AVCC3	121	K14	I	***Analog VCC for analog PLL.***

Table 5-10. Pin Descriptions of Power/Ground Signals (cont'd)

Signal	Pin(s) No. PQFP	Pin(s) No. LBGA	Attribute	Description
Power/Ground Signals				
AVSS3	123	K15	I	***Analog Ground for analog PLL.***
AVCC4	197	D7	I	***Analog VCC for USB Transceiver.***
AVSS4	202	D6	I	***Analog Ground for USB Transceiver.***
AVCC5	-	F4	I	***Analog VCC for analog PLL. (LBGA version only)***
AVSS5	-	D2	I	***Analog Ground for analog PLL. (LBGA version only)***

Notes: IO cell types are described as below:

I: Input PAD.
IK: Schmitt Trigger Input PAD.
PI: PCI Bus Specified Input PAD.
OSCI: Oscillator Input PAD.
O8: 8mA Output PAD.
O12: 12mA Output PAD.
O16: 16mA Output PAD.
OT12: 12mA Tri-State Output PAD.
OT24: 24mA Tri-State Output PAD.
OSCIO: Oscillator Input/Output PAD
PO: PCI Bus Specified Output PAD.
IO12: 12mA Input/Output PAD.
PIO: PCI Bus Specified Input/Output PAD.
UIO: USB Bus Specified Input/Output PAD.
IOD8: 8mA Open-Drain Input/Output PAD.

6. Power Management

6.1 Overview

The IT8152 power management policy is software-oriented. The power management is to provide the standby register to control the device power consumption. Some other registers are included in the power management to control the peripheral devices with ease.

6.2 Features

- Software-oriented power management
- Peripheral Devices Standby control
- Provides software reset mechanism for peripheral devices
- Provides peripheral device test control

6.3 Clock Tree Block Diagram

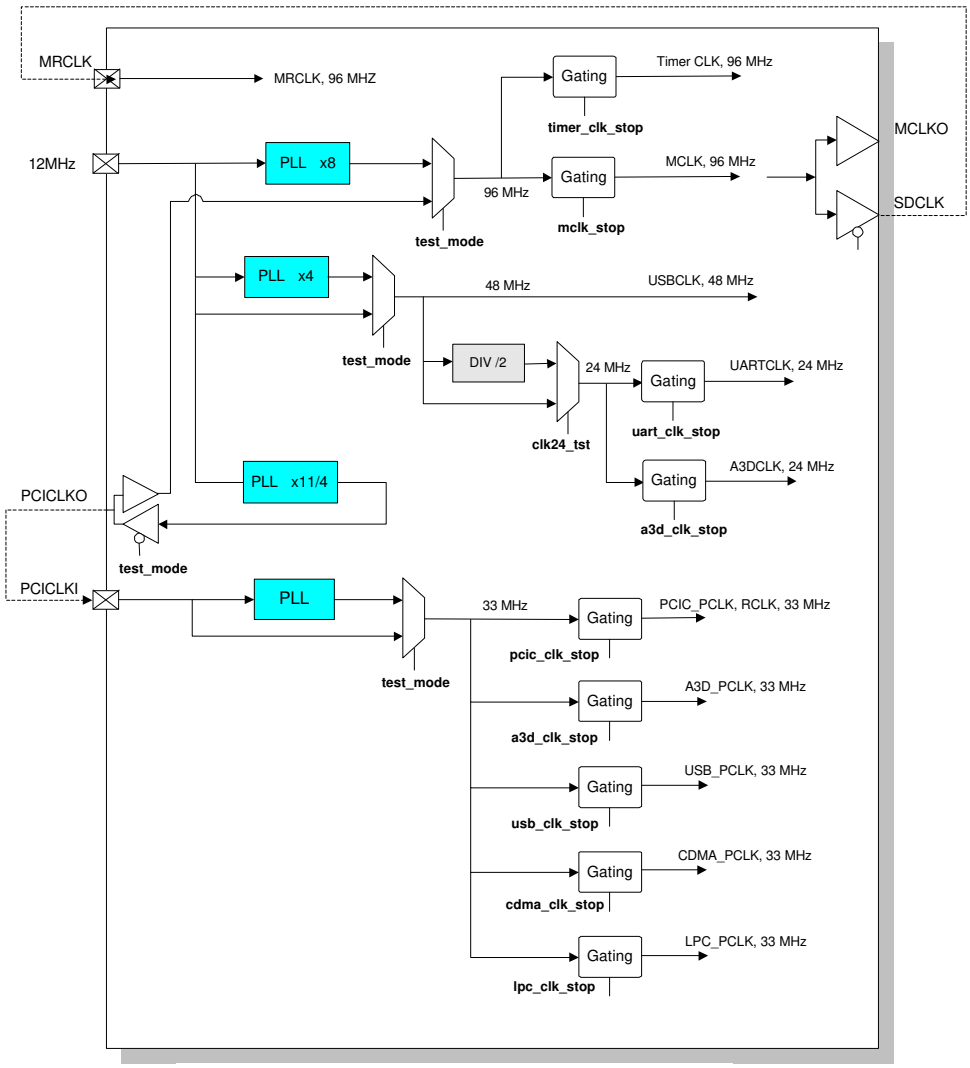


Figure 6-1. IT8152 Clock Tree Block Diagram

6.4 Register Descriptions

The following table lists all the registers in power management. The register size and access size are measured in the unit of byte. The register size is the actual size of register. The access size defines the word or byte, which is used to access each register or part of a power management register. The default value of the base address is **0x43F00000** in PCI I/O space.

Table 6-1. Register List of System Registers

Register Name	R/W	Offset	Default
Device Standby Register (DSR)	R/W	0x00	0000006Fh
Device Software Reset Register (DSRR)	R/W	0x04	00000000h
Device Test Mode Register (DTMR)	R/W	0x08	00000000h
PCI CLKRUN Option Register (PCOR)	R/W	0x0C	8000003Fh
PLL Control Register (PLLCR)	R/W	0x20	0000008Fh
MCLK Frequency Select Register (MFSR)	R/W	0x24	00000007h
Debug Port Register (DPR)	WO	0x40	-
Software Interrupt Port Register (SIPR)	WO	0x44	-

Definition of R/W Attributes:
WO **WRITE ONLY**. If a register is write only, reads from this register will have no effects.
R/W **READ/WRITE**. A register with this attribute can be read and written.

6.4.1 Device Standby Register (DSR) — Offset 0x00

This register is used to control the device to enter the standby mode or operation mode.

Bit	R/W	Default	Description
31-7	RO	0h	**Reserved**
6	R/W	1	**UART Standby Enable (UARTSB)** When this bit is set, the UART will enter the standby mode. When this bit is cleared, the UART will be in normal operation mode.
5	R/W	1	**Timer Standby (TMRSB)** This bit is used to force the Timer to enter the standby mode. When this bit is set, the Timer is in standby mode. If this bit is cleared, the Timer is in normal operation mode.
4	R/W	0	**PCI Controller Standby Enable (PCICSB)** When this bit is set, the PCI Controller will enter the standby mode. When this bit is cleared, the PCI Controller will be in normal operation mode.
3	R/W	1	**DMA Bus Standby Enable (DMABSB)** When this bit is set, the DMA Bus will enter the standby mode. When this bit is cleared, the DMA Bus will be in normal operation mode.
2	R/W	1	**CDMA Standby Enable (CDMASB)** When this bit is set, the Chaining DMA will enter the standby mode. When this bit is cleared, the Chaining DMA will be in normal operation mode.
1	R/W	1	**LPC Standby Enable (LPCSB)** When this bit is set, the LPC will enter the standby mode. When this bit is cleared, the LPC will be in normal operation mode.
0	R/W	1	**Audio Controller Standby Enable (ACSB)** When this bit is set, the Audio controller will enter the standby mode. When this bit is cleared, the Audio controller will be in normal operation mode.

6.4.2 Device Software Reset Register (DSRR) — Offset 0x04

The device software reset register can be used to reset the Device by software.

Bit	R/W	Default	Description
31-11	RO	0h	**Reserved**
10	R/W	0	**UART Software Reset (UARTSR)** When this bit is set, the UART will be reset. This reset is equivalent to the hardware reset. All UART registers are set to the reset default values. Note that this software reset bit is self-clearing when the reset is done.
9	R/W	0	**Timer #4 Software Reset (TMR4SR)** When this bit is set, the Timer #4 will be reset. This reset is equivalent to hardware reset. All the registers of Timer #4 are set to the reset default values. Note that this software reset bit is self-clearing.
8	R/W	0	**Timer #3 Software Reset (TMR3SR)** When this bit is set, the Timer #3 will be reset. This reset is equivalent to hardware reset. All the registers of Timer #3 are set to the reset default values. Note that this software reset bit is self-clearing.
7	R/W	0	**Timer #2 Software Reset (TMR2SR)** When this bit is set, the Timer #2 will be reset. This reset is equivalent to hardware reset. All the registers of Timer #2 are set to the reset default values. Note that this software reset bit is self-clearing.

Device Software Reset Register (DSRR) [cont'd]

Bit	R/W	Default	Description
6	R/W	0	**Timer #1 Software Reset (TMR1SR)** When this bit is set, the Timer #1 will be reset. This reset is equivalent to hardware reset. All the registers of Timer #1 are set to the reset default values. Note that this software reset bit is self-clearing.
5	R/W	0	**PCI Controller Software Reset (PCICSR)** When this bit is set, the PCI controller will be reset. This reset is equivalent to the hardware reset. All the registers of PCI controller are set to the reset default values. Note that this software reset bit is self-clearing.
4	R/W	0	**DMA Bus Software Reset (DMABSR)** When this bit is set, the DMA Bus will be reset. This reset is equivalent to the hardware reset. All DMA Bus registers are set to the reset default values. Note that this software reset bit is self-clearing when the reset is done.
3	R/W	0	**Chaining DMA Software Reset (CDMASR)** When this bit is set, the Chaining DMA will be reset. This reset is equivalent to the hardware reset. All Chaining DMA registers are set to the reset default values. Note that this software reset bit is self-clearing when the reset is done.
2	R/W	0	**LPC Software Reset (LPCSR)** When this bit is set, the LPC will be reset. This reset is equivalent to the hardware reset. All LPC registers are set to the reset default values. Note that this software reset bit is self-clearing when the reset is done.
1	R/W	0	**USB Software Reset (USBSR)** When this bit is set, the USB will be reset. This reset is equivalent to the hardware reset. All USB registers are set to the reset default values. Note that this software reset bit is self-clearing when the reset is done.
0	R/W	0	**Audio Controller Software Reset (ACSR)** When this bit is set, the Audio controller will be reset. This reset is equivalent to the hardware reset. All the registers of Audio controller are set to the reset default values. Note that this software reset bit is self-clearing.

6.4.3 Device Test Mode Register (DTMR) — Offset 0x08

This register is used to control the test mode of each Device.

Bit	R/W	Default	Description
31-11	RO	0h	**Reserved**
10	R/W	0	**UART Baud Rate Test (UARTTST)** This bit is used to test the UART baud rate.
9	RO	0	**RAB to Internal Bus Bridge Test (R2ITST)** This bit is used to enable the RAB to Internal Bus Bridge test mode.
8	R/W	0	**RAB Test (RABTST)** This bit is used to enable the RAB test mode.
7	R/W	0	**Host to PCI Bridge Test (H2PTST)** This bit is used to enable the Host to PCI Bridge test mode.
6	R/W	0	**DMA Bus Test (DMABTST)** This bit is used to control the DMA Bus test pin.

Device Test Mode Register (DTMR) [cont'd]

Bit	R/W	Default	Description
5	R/W	0	**Chaining DMA Test (CDMATST)** This bit is used to control the chaining DMA test pin.
4	R/W	0	**LPC Test (LPCTST)** This bit is used to enable the LPC test mode.
3	R/W	0	**USB Transceiver Test (USBTTST)** This bit is used to enable the USB transceiver test pin.
2	R/W	0	**USB Function Test (USBFTST)** This bit is used to enable the USB function test pin.
1	R/W	0	**USB Test (USBTST)** This bit is used to enable the USB test mode.
0	R/W	0	**Audio Controller Test (ACTST)** This bit is used to enable the Audio Controller test pin.

6.4.4 PCI CLKRUN Option Register (PCOR) — Offset 0x0C

This register is used to control the operation of PCI CLKRUN#. The most significant two bits PCICR and PCICS dominants the operation of PCICLK and these two bits should not be set at the same time. The relative CLKRUN mask bits from bit 5 to bit 0 are used to control the PCI CLKRUN# sources and valid only as PCICR and PCICS are both cleared to "0".

Bit	R/W	Default	Description
31	R/W	1	**PCICLK RUN (PCICR)** When this bit is set, the PCICLK is always running regardless the status of the signal PCI CLKRUN#.
30	R/W	0	**PCICLK STOP (PCICS)** When this bit is set, the PCICLK is forced to stop regardless the status of the signal PCI CLKRUN#.
29-6	-	0h	**Reserved**
5	R/W	1	**Memory Controller CLKRUN Mask (MEMCM)** When this bit is set, the CLKRUN# signal of the Memory controller is mask and then has no effect to the status of PCI CLKRUN#. When this bit is cleared, the CLKRUN# signal of the Memory controller is passed to the PCI CLKRUN#.
4	R/W	1	**Host to PCI Bridge CLKRUN Mask (H2PCM)** When this bit is set, the CLKRUN# signal of the Host to PCI Bridge is mask and then has no effect to the status of PCI CLKRUN#. When this bit is cleared, the CLKRUN# signal of the Host to PCI Bridge is passed to the PCI CLKRUN#.
3	R/W	1	**PCI to LPC Bridge CLKRUN Mask (P2LCM)** When this bit is set, the CLKRUN# signal of the PCI to LPC Bridge is mask and then has no effect to the status of PCI CLKRUN#. When this bit is cleared, the CLKRUN# signal of the PCI to LPC Bridge is passed to the PCI CLKRUN#.
2	R/W	1	**Chaining DMA CLKRUN Mask (CDMACM)** When this bit is set, the CLKRUN# signal of the chaining DMA is mask and then has no effect to the status of PCI CLKRUN#. When this bit is cleared, the CLKRUN# signal of the chaining DMA is passed to the PCI CLKRUN#.

PCI CLKRUN Option Register (PCOR) [cont'd]

Bit	R/W	Default	Description
1	R/W	1	**USB Host Controller CLKRUN Mask (USBCM)** When this bit is set, the CLKRUN# signal of the USB Host controller is mask and then has no effect to the status of PCI CLKRUN#. When this bit is cleared, the CLKRUN# signal of the USB Host controller is passed to the PCI CLKRUN#.
0	R/W	1	**Audio Controller CLKRUN Mask (ACCM)** When this bit is set, the CLKRUN# signal of the Audio controller is mask and then has no effect to the status of PCI CLKRUN#. When this bit is cleared, the CLKRUN# signal of the Audio controller is passed to the PCI CLKRUN#.

6.4.5 PLL Control Register (PLLCR) — Offset 0x20

This register is used to control the PLL power down and clock skew between internal and external clocks.

Bit	R/W	Default	Description
31-8	R/W	0h	**Reserved**
7	R/W	1	**12MHZ Clock Oscillator Power Down (12PDN)** This bit is used to control the power down mode of 12MHZ clock's oscillator. When this bit is set, the oscillator is in normal operation mode. When this bit is cleared, the oscillator is in power down mode.
6-4	R/W	000b	**PCI Clock Skew Control (PCICSC)** These bits are used to control the clock skew between the internal PCI clock and external PCI clock (PCICLK).
3	R/W	1	**48MHZ Clock PLL Power Down (48PDN)** This bit is used to control the power down mode of 48MHZ clock's P LL. When this bit is set, the PLL is in normal operation mode. When this bit is cleared, the PLL is in power down mode. Note that when the PLL is switched from the power down mode to the normal mode, at least 5 microseconds are needed to let the PLL lock the external 48MHZ clock.
2	R/W	1	**De-skew Clock PLL Power Down (DPDN)** This bit is used to control the power down mode of De-skew clock's PLL. When this bit is set, the PLL is in normal operation mode. When this bit is cleared, the PLL is in power down mode. Note that when the PLL is switched from the power down mode to the normal mode, at least 5 microseconds are needed to let the PLL lock the external De-skew clock.
1	R/W	1	**PCI Clock PLL Power Down (PPDN)** This bit is used to control the power down mode of PCI clock's PLL. When this bit is set, the PLL is in normal operation mode. When this bit is cleared, the PLL is in power down mode. Note that when the PLL is switched from the power down mode to the normal mode, at least 5 microseconds are needed to let the PLL lock the external PCI clock (PCICLK).
0	R/W	1	**Memory Clock PLL Power Down (MPDN)** This bit is used to control the power down mode of Memory clock's PLL. When this bit is set, the PLL is in normal operation mode. When this bit is cleared, the PLL is in power down mode. Note that when the PLL is switched from the power down mode to the normal mode, at least 5 microseconds are needed to let the PLL lock the external Memory clock (MCLK).

6.4.6 MCLK Frequency Select Register (MFSR) — Offset 0x24

This register is used to select the operating frequency of Memory Clock, MCLK. Be sure to put the MCLK PLL in power down mode before changing the operating frequency.

Bit	R/W	Default	Description
31-3	-	0h	**Reserved**
2-0	R/W	111b	**MCLK Frequency Select (MFS[2:0])** 000: 12 MHz 001: 24 MHz 010: 36 MHz 011: 48 MHz 100: 60 MHz 101: 72 MHz 110: 84 MHz 111: 96 MHz

6.4.7 Debug Port Register (DPR) — Offset 0x40

Writing a data to this address will generate a data latch signal output via DPLE pin. This signal is used to latch the data value to be written into this register.

6.4.8 Software Interrupt Port Register (SIPR) — Offset 0x44

Writing a data to this address will generate a software interrupt pulse to the interrupt controller.

7. Memory Controller

7.1 Overview

The Memory Controller includes PCI to memory interface, internal DMA bus arbiter, shared SDRAM controller, a PCI to internal RAB bus interface and the internal RAB bus arbiter.

7.1.1 Features

- Supports 96 MHz, 3.3 V SDRAM
- 32-bit SDRAM data bus width
- Supports16Mb, 64Mb, 128Mb, 256Mb SDRAM
- Supports up to 64MB Memory
- Supports 2-level 64-byte PCI to SDRAM post write FIFO
- Supports 2-level 64-byte PCI to SDRAM read FIFO
- Supports PCI read prefetch
- Supports PCI delayed transactions for IO cycles

7.1.2 Block Diagram

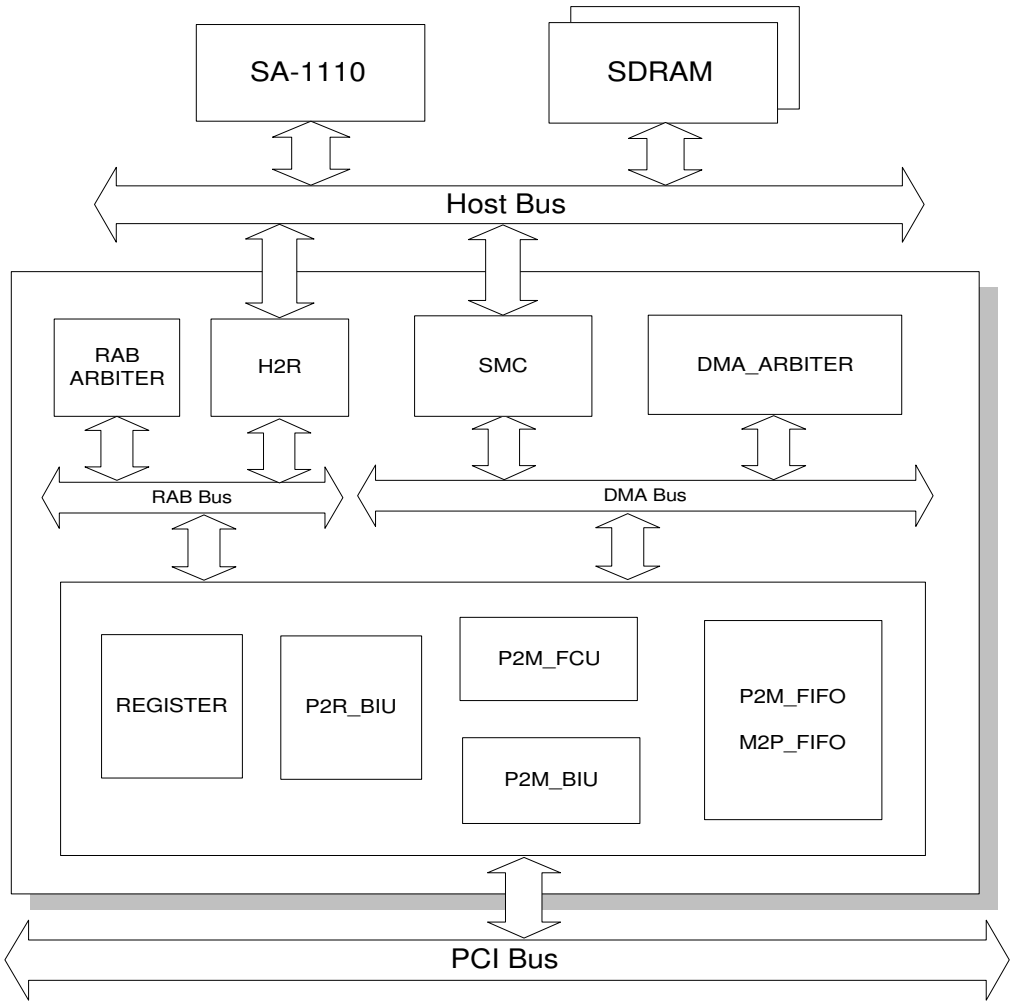


Figure 7-1. Memory Controller Block Diagram

7.1.3 Register Configuration

The following table lists the registers of the memory controller. All register size and access size are double word (32 bits). The base address (from CPU memory space) of all registers is **0x43F00100**. Note that these registers can also be accessed from PCI IO space. The base address for the Memory Controller registers is **0x43F00100** (PCI IO space base address plus **0x100**) and can be re-allocated by changing the PCI IO space base address register described at the PCI configuration space registers in the CPU to PCI bridge section. The device number is dependent on board connection and the function number is 0.

Table 7-1. Shared Memory Controller Registers

Register Name	R/W	Offset	Default
SDRAM Control Register (SDCR)	R/W[Note1]	0x00	0E050501h
PCI Slave Control Register (PCICR)	R/W[Note2]	0x04	00000168h

Definition of R/W Attribute:

R/W **READ/WRITE**. A register with this attribute can be read and written.

Note 1: Bits 27-24, 18-16, 10- 8 and 0 in the register are read/write. Other bits are reserved.
Note 2: Bits 8-5, 3-0 in the register are read/write. Other bits are reserved.

7.2 Register Descriptions

7.2.1 SDRAM Control Register (SDCR) —Offset 0x00

This register provides some control options to the shared memory controller, including memory clock PAD driving, memory signals (control and data) PAD driving, SDRAM type, and two timing parameters tRAS and tCAS (or tCL) which can be adjusted to comply various SDRAM.

Bit	R/W	Default	Description
31-26	-	000011	**Reserved**
25-24	R/W	10	**SDRAM Interface PAD Current (SDCUR[1:0])** 00: 4mA, 01: 8mA, 10: 12 mA, 11: 16mA
23-19	-	0	**Reserved**
18-16	R/W	101	**SDRAM Type (SDTYP[2:0])** 16 Mb: 001 1M x 16 10 x 10 011 1M x 16 12 x 8 010 2M x 8 11 x 10 011 2M x 8 12 x 9 010 4M x 4 11 x 11 011 4M x 4 12 x 10 64 Mb : 010 4M x 16 11 x 11 011 4M x 16 12 x 10 100 4M x 16 13 x 9 101 4M x 16 14 x 8 011 8M x 8 12 x 11 100 8M x 8 13 x 10 101 8M x 8 14 x 9 011 16M x 4 12 x 12 100 16M x 4 13 x 11 101 16M x 4 14 x 10 128 Mb: 101 8M x 16 14 x 9 101 16M x 8 14 x 10 256 Mb: 110 16M x 16 15 x 9 110 32M x 8 15 x 10
15-11	-	0	**Reserved**
10-8	R/W	101	**TRAS (TRAS[2:0])** The value of the SDRAM timing parameter tRAS.
7-1	-	0	**Reserved**
0	R/W	1	**TCAS (TCAS)** The value of the SDRAM timing parameter tCAS (or tCL). When this bit is set to 1, it represents tCAS=3; set to 0, represents tCAS=2. Note that this bit should be fixed at 1 for IT8152.

7.2.2 PCI Slave Control Register (PCICR) — Offset 0x04

This register provides control options to the PCI bus interface of the shared memory controller, including PCI memory read pre-fetch control, PCI delayed transaction control, PCI initial latency timer control and PCI memory space top bound (for address decoder).

Bit	R/W	Default	Description
31-9	-	0	**Reserved**
8	R/W	1	**PCI Memory Read Prefetch Enable (ENPRF)** Set this bit to 1 to enable the PCI slave memory read prefetch.
7	R/W	0	**PCI IO Delayed Transaction Enable (ENDLY)** Set this bit to 1 to enable the delayed transaction for PCI IO cycles. Note that PCI memory cycles do not implement delayed transaction since memory requests are generally completed within 16 PCI clocks.
6-5	R/W	11	**PCI Initial Latency Timer Period Selection (ITMR[1:0])** Set to 11 for 32 clocks of PCI initial latency timer, and set to 10 for 16 clocks. The default value is 32 clocks as in the PCI specification. Set to 0x disables the initial latency timer.
4	-	0	**Reserved**
3-0	R/W	1000	**PCI Memory Space Top Bound (TOPB[3:0])** This register is the register that shows the PCI slave memory space (decoding range, PCI address bit 25 to 22). Software is responsible for filling the correct value depends on the SDRAM size that was detected. The default value is 16MB.

7.3 Operations

The operation of the memory controller is divided into five parts, PCI to memory interface, DMA arbiter, shared SDRAM controller, PCI to internal RAB bus interface and RAB arbiter. Basic operations of each part are described below.

7.3.1 PCI to Memory Interface (P2M)

The PCI interface supports PCI memory read/write transactions. The supported PCI commands are write, write and invalidate, read, read line and read multiple. The write and write and invalidate commands are treated the same. The read command is handled in a different manner with read line and read multiple if read prefetch is disabled, the read command will not prefetch but read line and read multiple will prefetch in current line (32 bytes alignment). The decoding speed is always medium decoding. Retry, disconnect with/without data are supported. The Initial latency and subsequent latency timer are supported. CLKRUN# is asserted when the PCI bus is non-idle, the write FIFO is not empty or when the read prefetch FIFO is not empty to guarantee the operations of the PCI bus. PCI lock cycle (device lock) is also supported.

For PCI write transactions, all data are posted to write FIFO, then the data gathering mechanism will issue proper write commands to SDRAM controller. All write cycles issued to SDRAM controller are 32-byte alignment. The write FIFO is capable of containing 64 bytes write data, once the FIFO is full, the PCI state machines will insert wait states until the FIFO is capable of receiving more data or disconnect when subsequent latency timer is expired.

For PCI read transactions, if read prefetch is enabled, the prefetch mechanism will issue proper commands to prefetch data and queued in read FIFO. All read requests issued to SDRAM controller are 32-byte alignment. At the end of a read transaction, the prefetch FIFO will be flushed. If read data is not yet ready, wait states are inserted until data ready or the latency timers expire to retry or disconnect the current read cycle. For data consistency, PCI read cycles will push all write cycles (including CPU write cycles), i.e., previously posted write cycles must be completed before current read cycles.

7.3.2 DMA Arbiter

The DMA arbiter performs the arbitration between the P2M and CDMA and is a round robin arbiter. On receiving the request from P2M or CDMA, the DMA arbiter sends the request to SDRAM controller and also replies grant to the higher priority master. On receiving the grant from DMA arbiter, the P2M or CDMA is allowed to issue cycles to the DMA bus, the SDRAM controller will then transform the cycle to the SDRAM bus.

7.3.3 Shared SDRAM Controller

The SDRAM interface supports one bank of 16Mb, 64Mb, 128Mb or 256Mb asymmetric SDRAM with memory size from 8MB to 64MB. The shared SDRAM controller asserts MBREQ to request the host bus on receiving requests from the DMA arbiter. The CPU asserts MBGNT to release the host bus and the shared SDRAM controller is now allowed to issue SDRAM cycles to the host bus. On completion of every SDRAM cycle (at most a burst of eight), the MBREQ is negated by the shared SDRAM controller so that the CPU can do refresh or other cycles. The SDRAM controller do not support page mode operations, that is, every row should be pre-charged after READ or WRITE command. The MRCLK input is for latching the read data from the SDRAM, and it should be directly connected to SDCLK for optimum timing. To fine tune the relationship between the input data and clock, MRCLK can be connected to MCLKO on which a capacitor is placed to control the timing.

The SDRAM initialization process (precharge all banks, 8 auto refresh followed by a set mode register command) is executed after power-on reset by CPU. The refresh is also the responsibility of the CPU.

The supported SDRAM types are the same with SA-1110 CPU. The SDRAM type register should be programmed to be the same with the CPU and the tCAS parameter should be the same with which programmed to the mode register of the SDRAM during initialization.

7.3.4 PCI to Internal RAB Bus Interface

The PCI to Internal RAB bus interface translates PCI cycles targeted at internal registers that reside on the RAB bus to the RAB bus cycles. A RAB bus arbiter is responsible for arbitration between the CPU access and PCI access to the RAB bus. All PCI IO writes to the RAB bus will be posted to one level of write FIFO. Delayed transaction is supported for PCI IO read cycle that accesses the RAB bus.

To avoid deadlock, all CPU initiated PCI IO cycles that targeted at internal RAB bus or system memory will be terminated with target abort.

7.3.5 RAB Bus Arbiter

The RAB arbiter is for arbitration between P2R (PCI to RAB interface) and H2R (host to RAB interface). The grant is parked at H2R when there is no request to access the RAB bus. Once PCI side request is received, the arbiter will grant to P2R if there is no H2R request, that is, the H2R has higher priority than P2R. Once the P2R cycle is completed, the grant to P2R is de-asserted and parked to H2R again.

8. CPU to PCI Bridge

8.1 Overview

The CPU to PCI Bridge provides a 32-bit Host PCI Bus Interface, which supports PCI clock up to 33 MHz. Eight-level DWORD buffers are provided for CPU-to-PCI post writes to help maximize the bandwidth for memory and I/O writes to the PCI bus. It also allows concurrent transaction between CPU bus and PCI bus. For increasing the PCI memory access performance, memory pre-fetch function is implemented.

8.2 Features

- PCI Spec. version 2.1 compliant
- Provide 8-level DWORD posted write buffers for CPU-to-PCI write transactions
- Provide 8-level DWORD prefetch buffers for PCI Memory pre-fetch function,
- Support PCI clock speed up to 33 MHz
- Support Concurrent Transaction between the CPU and PCI bus

8.3 Block Diagram

The CPU to PCI Bridge is composed of CPU to RAB Bridge (H2R) and RAB to PCI Bridge (R2P), where the RAB Bus is provided as an internal 32-bit synchronous Register Access Bus.

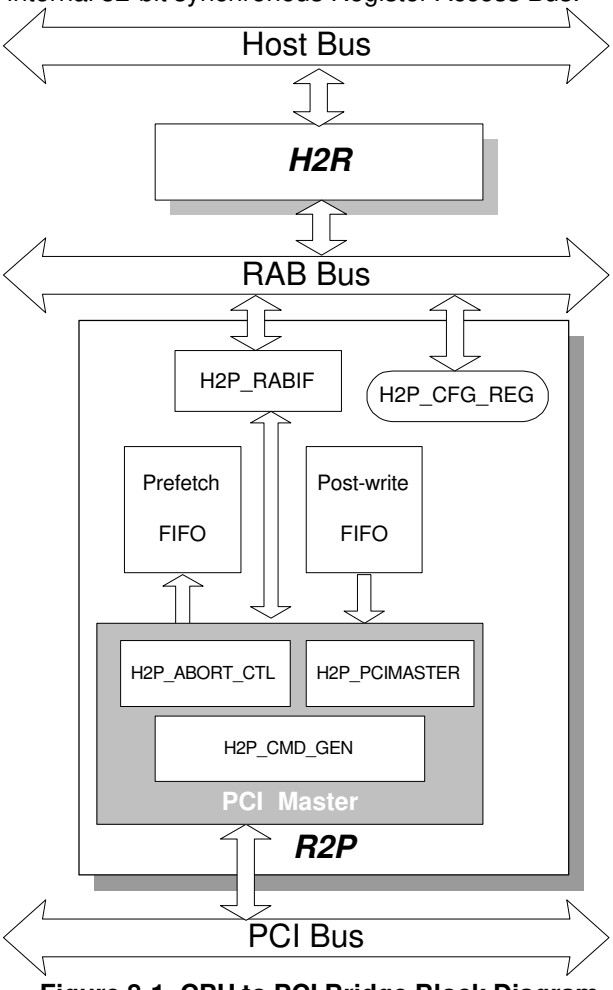


Figure 8-1. CPU to PCI Bridge Block Diagram

8.4 Register Description

Table 8-1. List of PCI Configuration Registers

Register Name	R/W	Address	Default
Configuration Address Register (CONFADDR)	R/W[Note1]	0x43F00800	00000000h
Configuration Data Register (CONFDATA)	R/W	0x43F00804	00000000h

Definition of R/W Attribute:

R/W **READ/WRITE**. A register with this attribute can be read and written.

Note 1: Bits 0 - 1, 24 - 31 in the register are read only. Other bits are read/write.

Table 8-2. List of PCI Command Registers

Register Name	R/W	Address	Default
PCI Interrupt Acknowledge Cycle (PIAC)	RO	0x43F00808	-
PCI Special Cycle (PSC)	WO	0x43F0080C	-

Definition of R/W Attributes:

RO **READ ONLY**. If a register is read only, writes to this register have no effects.
WO **WRITE ONLY**. If a register is written only, the data written to this register can not be read from this register.

Table 8-3. List of CPU/PCI Bridge Configuration Registers

Register Name	R/W	Offset	Default
Vendor Identification Register (VID)	RO	0x00	1283h
Device Identification Register (DID)	RO	0x02	8152h
PCI Command Register (PCICMD)	R/W [Note1]	0x04	0007h
PCI Status Register (PCISTS)	R/WC [Note2]	0x06	0200h
Revision ID Register (RID)	RO	0x08	20h
Class Code Register (CLASSC)	RO	0x09	060000h
Header Type Register (HEADT)	RO	0x0E	80h
PCI Memory Base Address Register (PMBAR)	R/W [Note3]	0x10	C0000008h
PCI I/O Base Address Register (PIOBAR)	R/W [Note4]	0x14	43F00001h
PCI Memory Address Prefix Register for Bank 4 (PMAPR4)	R/W [Note5]	0x40	40000000h
PCI Memory Address Prefix Register for Bank 5 (PMAPR5)	R/W [Note5]	0x44	48000000h
PCI I/O Address Prefix Register (PIOAPR)	R/W [Note6]	0x48	43E00000h
Prefetch Control Register (PCR)	R/W [Note7]	0x4C	0
Partial Read Base Address Register 0 (PRBAR0)	R/W [Note8]	0x50	0
Partial Read Control Register 0 (PRCR0)	R/W [Note9]	0x54	0
Partial Read Base Address Register 1 (PRBAR1)	R/W [Note8]	0x58	0
Partial Read Control Register 1 (PRCR1)	R/W [Note9]	0x5C	0

Table 8-3. List of CPU/PCI Bridge Configuration Registers (cont'd)

Register Name	R/W	Offset	Default
Partial Read Base Address Register 2 (PRBAR2)	R/W Note8	0x60	0
Partial Read Control Register 2 (PRCR2)	R/W Note9	0x64	0
Partial Read Base Address Register 3 (PRBAR3)	R/W Note8	0x68	0
Partial Read Control Register 3 (PRCR3)	R/W Note9	0x6C	0
Partial Read Base Address Register 4 (PRBAR4)	R/W Note8	0x70	0
Partial Read Control Register 4 (PRCR4)	R/W Note9	0x74	0
Partial Read Base Address Register 5 (PRBAR5)	R/W Note8	0x78	0
Partial Read Control Register 5 (PRCR5)	R/W Note9	0x7C	0
Partial Read Base Address Register 6 (PRBAR6)	R/W Note8	0x80	0
Partial Read Control Register 6 (PRCR6)	R/W Note10	0x84	0
Partial Read Base Address Register 7 (PRBAR7)	R/W Note8	0x88	0
Partial Read Control Register 7 (PRCR7)	R/W Note10	0x8C	0

Definition of R/W Attributes:

RO **READ ONLY**. If a register is read only, writes to this register have no effects.
R/W **READ/WRITE**. A register with this attribute can be read and written.
R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 will have no effects.

Note 1: Bits 2 - 5, 7 - 15 in the register are read only. Other bits are read/write.
Note 2: Bits 0 - 7, 9 - 10, 14 in the register are read only. Other bits are read/write clear.
Note 3: Bits 0 - 25 in the register are read only. Other bits are read/write.
Note 4: Bits 0 - 10 in the register are read only. Other bits are read/write.
Note 5: Bits 0 - 25 in the register are read only. Other bits are read/write.
Note 6: Bits 0 - 19 in the register are read only. Other bits are read/write.
Note 7: Bits 1 – 21, 27 - 31 in the register are read only. Other bits are read/write.
Note 8: Bits 27 - 31 in the register are read only. Other bits are read/write.
Note 9: Bits 10 - 29 in the register are read only. Other bits are read/write.
Note 10: Bits 26 - 29 in the register are read only. Other bits are read/write.

8.4.1 PCI Configuration Registers

The PCI specification defines two types of bus cycles to access the PCI configuration space – **Configuration Read** and **Configuration Write**. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The IT8152 only supports Mechanism #1 according to the PCI specification.

The configuration access mechanism involves using the CONFADDR Register and CONFDATA Register. To reference a configuration register, a DWORD write cycle is used to load a value into CONFADDR which specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of device function being accessed. CONFDATA becomes a window into four bytes of configuration space specified by the contents of CONFADDR. Any read or write to CONFDATA will result in translating the CONFADDR into a PCI configuration cycle.

Type 0 Configuration Access – If the Bus Number field of the CONFADDR is 0, a Type 0 Configuration cycle is performed on PCI bus. The content of CONFADDR[10:2] is mapped into AD[10:2]. The Device Number field of CONFADDR is decoded into AD[31:11]. For the Device Selection during configuration cycle, Device #0 will assert AD11, Device #1 will assert AD12, Device #2 will assert AD13 and so forth up to Device #20 which will assert AD31. According to the PCI specification, only one AD line will be asserted at a time. All device numbers greater than 20 will cause a type 0 configuration access without IDSEL being asserted, and consequently result a Master Abort.

Type 1 Configuration Access – If the Bus Number field of CONFADDR is not 0, a Type 1 Configuration is performed on PCI bus. The CONFADDR[23:2] is mapped directly to AD[23:2]. AD[1:0] are driven to "01" to indicate a Type 1 Configuration cycle. All other AD lines are driven to 0.

8.4.1.1 Configuration Address Register (CONFADDR) — Address 0x43F00800

The CONFADDR register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	R/W	Default	Description
31-24	RO	0h	**Reserved**
23-16	R/W	0h	**Bus Number (BUSN)** A Type 0 Configuration cycle is generated on PCI bus if the Bus Number is programmed to 0h and Host/PCI Bridge is not the target. If the Bus Number is programmed to a non-zero value, a Type 1 Configuration cycle is generated on PCI bus with the Bus Number mapped to PAD[23:16] during the address phase.
15-11	R/W	0h	**Device Number (DEVN)** This field selects one of the 21 devices on a given Bus Number. During a Type 0 Configuration cycle, this field is decoded, and one of PAD[31:11] is set to 1. During a Type 1 Configuration cycle, this field is mapped to PAD[15:11].
10-8	R/W	0h	**Function Number (FUNN)** This field is mapped to PAD[10:8] during PCI configuration cycles. This value is used to select one of eight possible functions on a multifunction device.
7-2	R/W	0h	**Register Number (REGN)** This field is mapped to PAD[7:2] during PCI Configuration cycles. This value is used to index a DWORD in Configuration Space of the intended target.
1-0	RO	0h	**Reserved**

8.4.1.2 Configuration Data Register (CONFDATA) — Address 0x43F00804

This register provides a 32-bit read/write window into configuration space. The address portion of the configuration space that is referenced by the CONFDATA register is determined by the contents of the CONFADDR register.

Bit	R/W	Default	Description
31-0	R/W	0h	**Configuration Data (CONFDATA)** Any access to this register will generate a Configuration cycle which address space uses the contents of the CONFADDR.

8.4.2 PCI Command Registers

8.4.2.1 PCI Interrupt Acknowledge Cycle (PIAC) — Address 0x43F00808

Bit	R/W	Default	Description
31-0	RO	-	**PCI Interrupt Acknowledge Cycle (PIAC)** Read this register will generate a PCI Interrupt Acknowledge Cycle on the PCI Bus. The PCI address is undefined. The PCI byte enables are derived from CPU byte enables.

8.4.2.2 PCI Special Cycle (PSC) — Address 0x43F0080C

Bit	R/W	Default	Description
31-0	WO	-	**PCI Special Cycle (PSC)** Write this register will generate a PCI Special Cycle on the PCI Bus. The PCI address is undefined. The PCI byte enables are derived from CPU byte enables.

8.4.3 CPU/PCI Bridge Configuration Registers (Function 0)

The CPU/PCI Bridge Configuration registers are contained in IT8152 function 0 and are used to specify the CPU/PCI bridge configuration and operating parameters.

8.4.3.1 Vendor Identification Register (VID) — Offset 0x00-01

Bit	R/W	Default	Description
15-0	RO	1283h	**Vendor ID (VID)** This is a 16-bit value assigned to ITE.

8.4.3.2 Device Identification Register (DID) — Offset 0x02-0x03

Bit	R/W	Default	Description
15-0	RO	8152h	**Device ID (DID)** This is a 16-bit value assigned to the IT8152.

8.4.3.3 PCI Command Register (PCICMD) — Offset 0x04-0x05

Bit	R/W	Default	Description
15-10	RO	0h	**Reserved**
9	RO	0	**Fast Back-to-Back Enable (FB2BE)** Not implemented. This bit is always 0.
8	RO	0	**SERR # Enable (SERRE)** Not implemented. This bit is always 0.
7	RO	0	**Address/Data Stepping (ADS)** Not implemented. This bit is always 0.
6	R/W	0	**Parity Error Response (PER)** When this bit is set to 1, the Data Parity Error Detected can be reported. When this bit is set to 0, the Data Parity Error Detected is ignored.
5	RO	0	**Video Pallet Snooping (VPS)** Not implemented. This bit is always 0.
4	RO	0	**Memory Write and Invalidate Enable (MWIE)** Not implemented. This bit is always 0.
3	RO	0	**Special Cycle Enable (SCE)** Not implemented. This bit is always 0.
2	RO	1	**Bus Master Enable (BME)** This bit is always 1. Disabling of bus master capability on PCI bus is not supported.
1	R/W	1	**Memory Access Enable (MAE)** When this bit is 1, the IT8152 permits other PCI masters to access main memory if the PCI address selects enabled Memory space. When this bit is 0, the IT8152 does not respond to any PCI memory cycle which accesses the main memory.
0	R/W	1	**I/O Access Enable (IOAE)** When this bit is 1, the IT8152 permits other PCI masters to access internal registers of IT8152. When this bit is 0, access to internal registers of IT8152 is disabled.

8.4.3.4 PCI Status Register (PCISTS) — Offset 0x06-0x07

Bit	R/W	Default	Description
15	R/WC	0	**Detected Parity Error (DPE)** When this bit is set to 1, it indicates that a parity error has been detected even if parity error enable (**PERRE**) bit is disabled. When this bit is 0, it indicates that no parity error is detected. This bit is cleared by writing a 1 to itself.
14	RO	0	**Signaled System Error (SSE)** This bit is not implemented.
13	R/WC	0	**Received Master Abort (RMA)** When the IT8152 terminates a CPU-to-PCI transaction with a master abort, this bit is set to 1. This bit is cleared by writing a 1 to itself.
12	R/WC	0	**Received Target Abort (RTA)** This bit is set to 1 when an IT8152-initiated PCI transaction is terminated with Target-Abort. This bit is cleared by writing a 1 to itself.
11	R/WC	0	**Signaled Target Abort (STA)** This bit is set to 1 when IT8152 terminates a PCI transaction with a Target-Abort. This bit is cleared by writing a 1 to itself.
10-9	RO	01	**DEVSEL Timing (DEVT)** These two bits are set to 01b (medium) to indicate the slowest time that DEVSEL# is asserted.
8	R/WC	0	**Data Parity Error Detected (DPED)** This bit is set only if the following conditions are met: 1) IT8152 asserts PERR# itself (during a read); 2) the Parity Error Response (**PER**) bit in command register is set to "1". This bit is cleared by writing a 1 to itself.
7	RO	0	**Fast Back-to-Back Capable (FB2BC)** This bit is always 0 when the Fast Back-to-Back is not implemented.
6	RO	0	**UDF Supported (UDF)** This bit is always 0 because UDF is not supported.
5	RO	0	**66 MHz Capable (66C)** The 66 MHz PCI is not supported. This bit is always 0.
4-0	RO	0h	**Reserved**

8.4.3.5 Revision ID Register (RID) — Offset 0x08

Bit	R/W	Default	Description
7-0	RO	20h	**Revision ID (RID)** This field contains the revision number of the IT8152. The current ASIC revision number is 2.0.

8.4.3.6 Class Code Register (CLASSC) — Offset 0x09-0x0B

Bit	R/W	Default	Description
23-16	RO	06h	**Base Class Code (BASEC)** 06h = Bridge Device.
15-8	RO	00h	**Sub-Class Code (SCC)** 00h = Host Bridge.
7-0	RO	00h	**Programming Interface (PI)** 00h = Host-to-PCI Bridge.

8.4.3.7 Header Type Register (HEADT) — Offset 0x0E

Bit	R/W	Default	Description
7-0	RO	80h	**Header Type (HEADT)** Header Type 80h identifies the IT8152 as a multi-function device.

8.4.3.8 PCI Memory Base Address Register (PMBAR) — Offset 0x10

Bit	R/W	Default	Description
31-26	R/W	30h	**PCI Memory Base Address (PMBA)** PCI slave memory base address is 0xc0000000.
25-4	RO	0	**PCI Memory Size (PMSZ)** PCI slave memory size, 64M Bytes is required. These bits are hardwired to '0'.
3	RO	1	**PCI Prefetchable Memory Area (PRF)** A "1" indicates that this is a prefetchable memory area.
2-1	RO	0	**Memory Type (MTYP)** A '00" means that this memory could be allocated anywh ere in 32-bit address space.
0	RO	0	**Memory Space Indicator (MEM)** A '0" indicates that this is a memory space base address register.

8.4.3.9 PCI I/O Base Address Register (PIOBAR) — Offset 0x14

Bit	R/W	Default	Description
31-11	R/W	87Eh	**PCI I/O Base Address (PIOBA)** PCI I/O base address is 0x43F00000.
10-2	RO	0	**PCI I/O Space Size (PIOSZ)** PCI I/O space size. These bits are hardwired to '0'.
1	-	0	**Reserved**
0	RO	1	**PCI I//O Indicator (IO)** PCI I/O Space Indicator.

8.4.3.10 PCI Memory Address Prefix Register for Bank 4 (PMAPR4) — Offset 0x40

Bit	R/W	Default	Description
31-26	R/W	10h	**PCI Memory Address Prefix (PMAP)** This field (6 bits) will be prefixed to CPU address (bits 25-0) to generate the 32-bit PCI MEM address.
25-0	RO	0	**Reserved**

8.4.3.11 PCI Memory Address Prefix Register for Bank 5 (PMAPR5) — Offset 0x44

Bit	R/W	Default	Description
31-26	R/W	12h	**PCI Memory Address Prefix (PMAP)** This field (6 bits) will be prefixed to CPU address (bits 25-0) to generate the 32-bit PCI MEM address.
25-0	RO	0	**Reserved**

8.4.3.12 PCI I/O Address Prefix Register (PIOAPR) — Offset 0x48

Bit	R/W	Default	Description
31-20	R/W	43Eh	**PCI I/O Address Prefix (PIOAP)** This field (12 bits) will be prefixed to CPU address (bits 19-0) to generate the 32-bit PCI I/O address.
19-0	RO	0	**Reserved**

8.4.3.13 Prefetch Control Register (PCR) — Offset 0x4C

Bit	R/W	Default	Description
31-27	RO	0	**Reserved**
26	R/W	0	**Prefetch Bank Select (PBS)** 1: Static bank 5 0: Static bank 4
25-22	R/W	0	**Prefetch Base Address (PBA)** CPU base address (bit 25-22) of PCI read prefetch function.
21-1	RO	0	**Reserved**
0	R/W	0	**Prefetch Enable (PEN)** Set this bit to 1 enables the prefetch function. When prefetch function is enabled and CPU address match prefetch base address, prefetch function will be performed to PCI memory read.

8.4.3.14 Partial Read Base Address Register n (PRBARn)

For PCI I/O device, byte enables must be consistent with address. However, SA-1110 asserts all byte enables on any read cycle. So, IT8152 has to infer accurate byte enables from the two LSBs of host address when SA-1110 issues a read cycle. For A[1:0] equal to 1 or 3, 8-bit data transfer is assumed. As for A[1:0] equal to 0 or 2, the following 8 sets of partial read registers are used to determine the transfer size.

Each set of partial read registers are composed of a base address register and a control register. Set 6 and set 7 have offset size up to 64M bytes (bit 25-0), while others have offset size up to 1K bytes (bit 9-0). When more than one set are addressed and enabled, set 0 always has the highest priority and set 7 has the lowest priority. When none of them are addressed or enabled, 16-bit data transfer is assumed for A[1:0] equal to 2, and 32-bit data transfer is assumed for A[1:0] equal to 0.

PRBAR0 — Offset 0x50
PRBAR1 — Offset 0x58
PRBAR2 — Offset 0x60
PRBAR3 — Offset 0x68
PRBAR4 — Offset 0x70
PRBAR5 — Offset 0x78
PRBAR6 — Offset 0x80
PRBAR7 — Offset 0x88

Bit	R/W	Default	Description
31-27	RO	0	**Reserved**
26	R/W	0	**Partial Read Bank Select (PRBS)** 1: Static bank 5 0: Static bank 4
25-0	R/W	0	**Partial Read Base Address (PRBA)** CPU base address of PCI partial read function.

8.4.3.15 Partial Read Control Register n (PRCRn)

PRCR0 — Offset 0x54
PRCR1 — Offset 0x5C
PRCR2 — Offset 0x64
PRCR3 — Offset 0x6C
PRCR4 — Offset 0x74
PRCR5 — Offset 0x7C

Bit	R/W	Default	Description
31	R/W	0	**Partial Read Enable (PREN)** 1: Enabled. 0: Disabled.
30	R/W	0	**Partial Read Transfer Size (PRTS)** 1: 16-bit transfer 0: 8-bit transfer
29-10	RO	0	**Reserved**
9-0	R/W	0	**Partial Read Offset Size (PROS)** Offset size of PCI partial read function.

PRCR6 — Offset 0x84
PRCR7 — Offset 0x8C

Bit	R/W	Default	Description
31	R/W	0	**Partial Read Enable (PREN)** 1: Enabled. 0: Disabled.
30	R/W	0	**Partial Read Transfer Size (PRTS)** 1: 16-bit transfer. 0: 8-bit transfer.
29-26	RO	0	**Reserved**
25-0	R/W	0	**Partial Read Offset Size (PROS)** Offset size of PCI partial read function.

9. PCI-to-LPC Bridge

9.1 Overview

The PCI-to-LPC Bridge provides a bus conversion from PCI bus to LPC bus so that system can access LPC devices.

The PCI-to-LPC Bridge is PCI function 2 in IT8152.

9.2 Features

PCI Interface features:

- Supports 32-bits PCI bus & up to 33 MHz PCI bus frequency
- Supports PCI Rev. 2.1 specification
- Supports programmable Delayed Transaction
- Supports PCI Configuration, Memory and I/O cycles
- Supports PCI Master and Slave

LPC Interface features:

- Supports LPC 1.0 specification
- Supports I/O Read, I/O Write cycles
- Supports SYNC Time-out abort report
- Supports SYNC Error report

Serial IRQ Interface features:

- Supports up to 21 programmable data frames
- Supports Quiet mode and Continuous mode
- Supports programmable 4-bit, 6-bit, 8-bit Start Frame width

9.3 Configuration Register Description

Register Name	R/W	Offset	Default
Vendor Identification Register (VID)	RO	0x00	1283h
Device Identification Register (DID)	RO	0x02	8152h
PCI Command Register (PCICMD)	R/W	0x04	0007h
PCI Status Register (PCISTS)	R/WC	0x06	0200h
Revision ID Register (RID)	RO	0x08	20h
Class Code Register (CLASSC)	RO	0x09	068000h
Header Type Register (HEADT)	RO	0x0E	00h
Base Address Register (BAR)	R/W	0x10	43E11801h
Serial IRQ Control Register (SERIRQC)	R/W	0x49	00h
Bridge Control Register (BCR)	R/W	0x4C	06h
Bridge Status Register (BSR)	R/WC	0x4D	00h
Discard Timer Register (DTR)	R/W	0x4F	3Fh
LPC I/O Space Base Address Register (LISBAR)	R/W	0x50	43E0h

Definition of R/W Attributes:

RO **READ ONLY**. If a register is read only, writes to this register will have no effects.
R/W **READ/WRITE**. A register with this attribute can be read and written.
R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 has no effects.

9.3.1 Vendor Identification Register (VID) — Offset 0x00-0x01

Bit	R/W	Default	Description
15-0	RO	1283h	**Vendor ID (VID)** This is a 16-bit value assigned to ITE.

9.3.2 Device Identification Register (DID) — Offset 0x02-0x03

Bit	R/W	Default	Description
15-0	RO	8152h	**Device ID (DID)** This is a 16-bit value assigned to the device ID.

9.3.3 PCI Command Register (PCICMD) — Offset 0x04-0x05

Bit	R/W	Default	Description
15-10	-	-	**Reserved**
9	RO	0	**Fast Back-to-Back Enable (FB2BE)** Not implemented. This bit is always 0.
8	R/W	0	**SERR # Enable (SERRE)** When this bit is set to 1 (and the bit **IOBLEE** or **LPCTOE** or **LPCERRE** or **DTTOE** in BCR register is set), The SERR# signal will be asserted when the condition is matched. When this bit is set to 0, no SERR# signal will be asserted.
7	RO	0	**Address/Data Stepping (ADS)** Not implemented. This bit is always 0.
6	RO	0	**Parity Error Response (PER)** Not implemented. This bit is always 0.
5	RO	0	**Video Palette Snooping (VPS)** Not implemented. This bit is always 0.
4	RO	0	**Memory Write and Invalidate Enable (MWIE)** Not implemented. This bit is always 0.
3	RO	0	**Special Cycle Enable (SCE)** Not implemented. This bit is always 0.
2	RO	1	**Bus Master Enable (BME)** This bit is hardwired to 1 so that Bus Master is always enabled.
1	RO	1	**Memory Access Enable (MAE)** This bit is hardwired to 1 so that Memory Access is always enabled.
0	RO	1	**I/O Access Enable (IOAE)** This bit is hardwired to 1 so that I/O Access is always enabled.

9.3.4 PCI Status Register (PCISTS) — Offset 0x06-0x07

Bit	R/W	Default	Description
15	RO	0	**Detected Parity Error (DPE)** Not implemented. This bit is always 0.
14	R/WC	0	**Signaled System Error (SSE)** When PCI to Internal Bus Bridge asserts the SERR# signal, this bit is set to 1. This bit can be cleared by writing a 1 to it.
13	RO	0	**Received Master Abort (RMA)** Not implemented. This bit is always 0.
12	RO	0	**Received Target Abort (RTA)** Not implemented. This bit is always 0.
11	R/WC	0	**Signaled Target Abort (STA)** This bit is set when PCI to Internal Bus bridge function is targeted with a transaction that terminates with a target abort. This bit can be cleared by writing a 1 to it.
10-9	RO	01	**DEVSEL Timing (DEVT)** These two bits are set to 01b (medium) to indicate the slowest time that DEVSEL# is asserted for all positive decode I/O spaces.
8	RO	0	**Data Parity Error Detected (DPED)** Not implemented. This bit is always 0.
7	RO	0	**Fast Back-to-Back Capable (FB2BC)** This bit is always 0 as the Fast Back-to-Back is not implemented.
6-0	-	-	**Reserved**

9.3.5 Revision ID Register (RID) — Offset 0x08

Bit	R/W	Default	Description
7-0	RO	20h	**Revision ID (RID)** This field contains the revision number of the IT8152. The current ASIC revision number is 2.0.

9.3.6 Class Code Register (CLASSC) — Offset 0x09-0x0B

Bit	R/W	Default	Description
23-16	RO	06h	**Base Class Code (BASEC)** 06h = Bridge Device.
15-8	RO	80h	**Sub Class Code (SCC)** 80h = Other Bridge Device.
7-0	RO	00h	**Programming Interface (PI)** 00h = No register level programming interface defined.

9.3.7 Header Type Register (HEADT) — Offset 0x0E

Bit	R/W	Default	Description
7-0	RO	00h	**Header Type (HEADT)** Header Type 00h indicates that the device's configuration space map follows the basic format.

9.3.8 Base Address Register (BAR) — Offset 0x10

Bit	R/W	Default	Description
31-8	R/W	43E118	**Reserved**
7-1	RO	0000000b	**Reserved**
0	RO	1	**Reserved**

9.3.9 Serial IRQ Control Register (SERIRQC) — Offset 0x49

Bit	R/W	Default	Description
7	R/W	0	**Serial IRQ Enable (SIRQEN)** This bit is used to enable the Serial IRQ Host. When this bit is set, the Serial IRQ Host is enabled. When this bit is cleared, the Serial IRQ Host is disabled.
6	R/W	0	**Serial IRQ Mode Select (SIRQMS)** This bit is used to select Quiet or Continuous Mode. When this bit is set, the Continuous mode is selected. When this bit is cleared, the Quiet mode is selected. Note that for system using the Quiet mode, this bit should be first set to 1 (Continuous mode) for at least one serial IRQ cycle (IRQ frame start to frame stop). Second, this bit is cleared to switch to the Quiet mode. These two steps must be performed before the SERIRQ pin will respond to the actual interrupt status.
5-4	R/W	00b	**Serial IRQ Frame Width (SIRQFW)** These two bits are used to specify the number of PCI clocks that Serial IRQ Host will assert SERIRQ pin low at the start frame. Note that when the Serial IRQ Host is in Quiet or Continuous mode, the start frame width is the same as observed at SERIRQ pin. 00: 4 clocks, 01: 6 clocks, 10: 8 clocks, 11: Reserved
3	-	-	**Reserved**
2-0	R/W	000b	**Serial IRQ Frame Number (SIRQFN)** These three bits are used to specify the number of Data Frame. The minimum is 17 frames. The maximum is 21 frames. 000: 17 frames, 001: 18 frames, 010: 19 frames, 011: 20 frames, 100: 21 frames, 101-111: Reserved

9.3.10 Bridge Control Register (BCR) — Offset 0x4C

Bit	R/W	Default	Description
7	R/W	0	**SERR# due to LPC SYNC Time-out Error Enable (LPCTOE)** This bit is used to enable the LPC SYNC Time-out error report to SERR#. When this bit is set, the LPC SYNC Time-out error report to SERR# is enabled. If this bit is cleared, the LPC SYNC Time-out error report to SERR# is disabled.
6	R/W	0	**SERR# due to PCI I/O Cycle Byte Lane Error Enable (IOBLEE)** This bit is used to enable the PCI I/O cycle byte lane error report to SERR#. When this bit is set, the PCI I/O cycle byte lane error report to SERR# is enabled. If this bit is cleared, the PCI I/O cycle byte lane error report to SERR# is disabled.
5	R/W	0	**SERR# due to LPC SYNC Error Report Enable (LPCERRE)** This bit is used to enable the LPC SYNC Error signal status report to SERR#. When this bit is set, the LPC SYNC Error signal status report to SERR# is enabled. If this bit is cleared, the LPC SYNC Error signal status report to SERR# is disabled.
4	R/W	0	**SERR# due to Delayed Transaction Time-out Enable (DTTOE)** This bit is used to enable the Delayed Transaction Time-out report to SERR# if the PCI master does not retry the same transaction when the discard timer is expired. When this bit is set, the Delayed Transaction Time-out report to SERR# is enabled. If this bit is cleared, the Delayed Transaction Time-out report to SERR# is disabled.
3	-	-	**Reserved**
2	R/W	1	**LPC I/O Single Byte Read Enable (LISBRE)** When this bit is set to 1, this bridge is allowed to issue a single byte read LPC I/O cycle no matter what the byte enables on PCI are. If this bit is 0, this bridge issues LPC I/O read cycle based on the byte enables on PCI.
1	R/W	1	**LPC I/O Space Decode Enable (LIODE)** 1: Enable. 0: Disable. Decoded space is limited to the 64KB I/O space which is assigned by LPC I/O Space Base Address Register. This space is subtractive decoded.
0	R/W	0	**Delayed Transaction Enable (DTE)** This bit is used to enable the delayed transaction. When this bit is set, the delayed transaction mechanism is enabled. If this bit is cleared, the delayed transaction mechanism is disabled.

9.3.11 Bridge Status Register (BSR) — Offset 0x4D

Bit	R/W	Default	Description
7	R/WC	0	**LPC SYNC Time-out Error (LPCTO)** When this bit is set, the LPC Time-out error occurred. Write a 1 to clear this bit
6	R/WC	0	**PCI I/O Cycle Byte Lane Error (IOBLE)** When this bit is set, the PCI I/O cycle byte lane error occurred. Write a 1 to clear this bit.
5	R/WC	0	**LPC SYNC Error Asserted (LPCERR)** When this bit is set, the LPC SYNC Error signal is asserted and latched. Write a 1 to clear this bit.
4	R/WC	0	**Delayed Transaction Time-out (DTTO)** When this bit is set, the Delayed Transaction Time-out occurred. Write a 1 to clear this bit.
3-0	-	-	**Reserved**

9.3.12 Discard Timer Register (DTR) — Offset 0x4F

Bit	R/W	Default	Description
7-0	R/W	3Fh	**Discard Timer (DT)** If the PCI master does not repeat the same transaction within the discard time after the Delayed Transaction is finished. The Delayed Transaction will time out. This causes the PCI target interface to discard the transaction and set the bit 4 (DTTO) in Bridge Status Register (BSR). The discard time is the discard timer value x 256 PCI clocks. 00h=Never Expired; 01h=256T; FFh=256x256T.

9.3.13 LPC I/O Space Base Address Register (LISBAR) — Offset 0x50

Bit	R/W	Default	Description
15-0	R/W	43E0h	**LPC I/O Space Base Address (LISBA)** The values of this register are bits 31-16 of the 64k PCI I/O space which is subtractive decoded by the PCI-to-LPC bridge and translated to LPC I/O space.

10. Chaining DMA Controller

10.1 Overview

The Chaining DMA (CDMA) controller is PCI function 1 in IT8152F. The CDMA is able to support four independent DMA channels which are capable of transferring data between SDRAM and PCI devices. Each channel supports both chaining and non-chaining transfers. Besides, both PCI memory device address and PCI I/O device address are supported.

The Chaining DMA (CDMA) controller also supports DMA transfer when bits 0 – 1 of the initial address of in PCI space are not equal to bits 0 – 1 of the initial address in SDRAM space (unaligned address).

10.2 Features

- Four independent software DMA channels
- Chaining mode and non-chaining mode are supported
- Both PCI memory address and PCI I/O address are supported
- Rotating and fixed priority types are supported
- DMA transfers of unaligned address are supported

10.3 Block Diagram

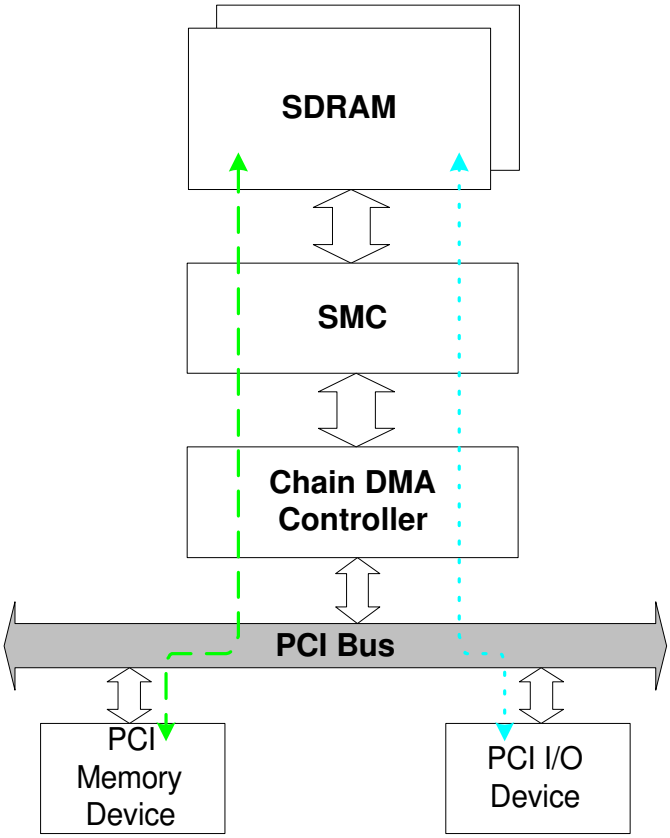


Figure 10-1. CDMA System Architecture

10.4 DMA Operation

Two DMA operation modes are supported in the CDMA controller: Non-Chaining Mode DMA and Chaining Mode DMA.

10.4.1 Non-Chaining Mode DMA

DMA mode can be set to the non-Chaining mode DMA through the Mode Register. Transfer parameters are set up through Memory Address Register, Device Address Register, Byte Count Register, and Descriptor Pointer Register (only the Direction of Transfer bit is needed in this mode). The Transfer Start bit in the Command/Status Register can be then set to initiate the transfer. The Transfer Done bit in the Command/Status Register can be polled to indicate the status of DMA transfer. Besides, the CDMA controller can be programmed to generate the interrupt request when the DMA transfer is completed.

In this mode, only consecutive data are transferred. Therefore, when the transfer of non-consecutive data is desired, Chaining Mode DMA is suggested.

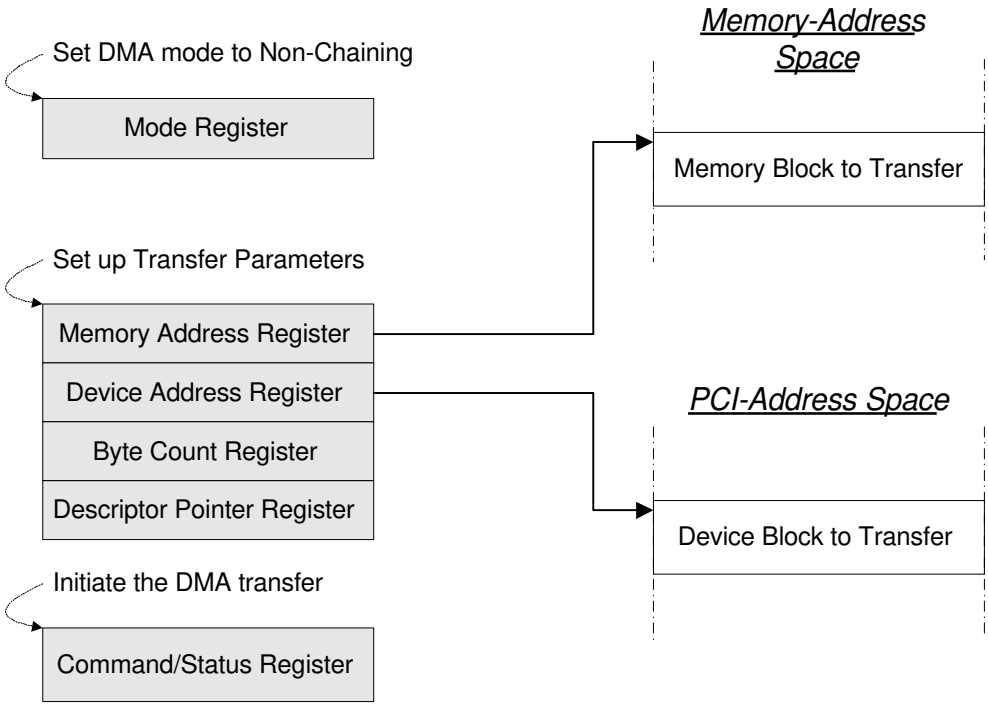


Figure 10-2. Non-Chaining Mode DMA Operation

10.4.2 Chaining Mode DMA

In this mode, transfer parameters are set up through descriptors resided in memory that must be able to be accessed with PCI memory address. They are composed of the contents of Memory Address Register, Device Address Register, Byte Count Register, and Descriptor Pointer Register.

Before the chaining mode DMA transfer can begin, the address of the initial descriptor must be set up in the Descriptor Pointer Register, and the Byte Count Register must be cleared, otherwise the initial descriptor can not be loaded correctly.

The transfer can be then initiated by setting the Transfer Start bit. The CDMA controller loads the initial descriptor and writes the content to Memory Address Register, Device Address Register, Byte Count Register, and Descriptor Pointer Register, and data is transferred until the desired byte count is reached, then next descriptor is loaded if necessary. The same steps are repeated (load a descriptor and transfer data) until the End of Chain bit is set in the Descriptor Pointer Register.

The CDMA controller can be programmed to generate the interrupt request when the transfer of current descriptor is done or when the overall DMA transfers are completed.

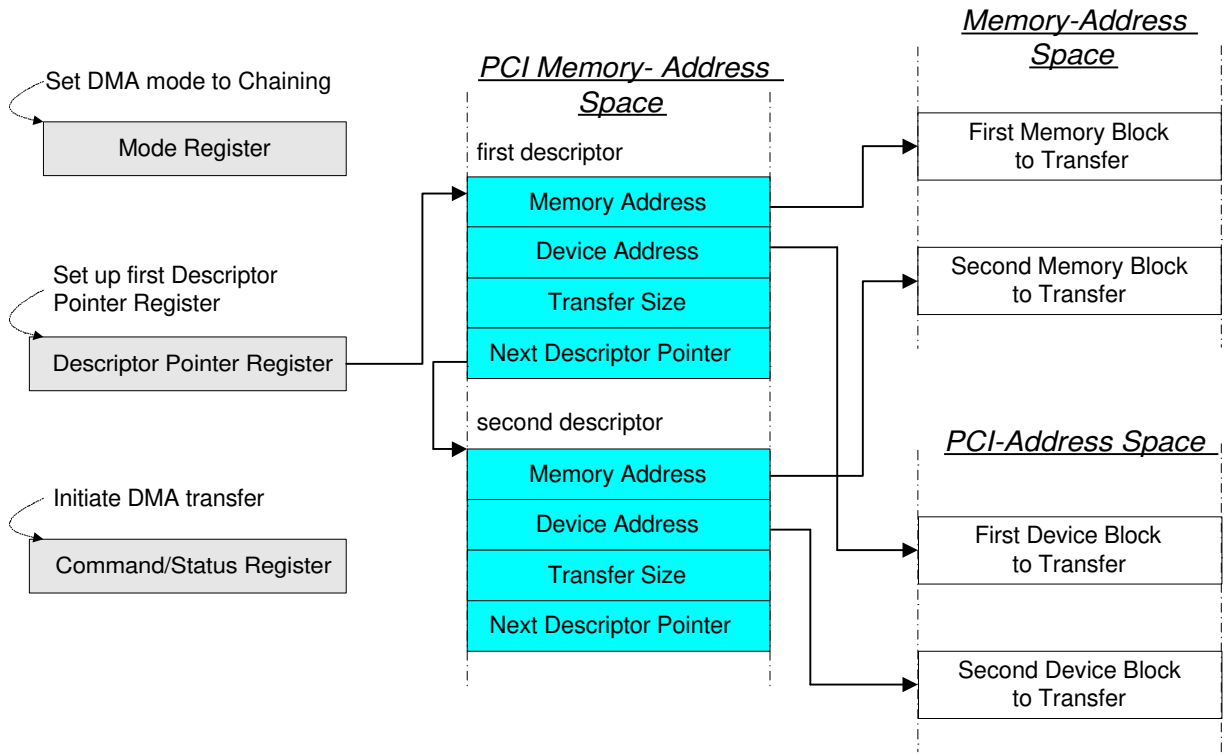


Figure 10-3. Chaining Mode DMA Operation

10.5 Register Description

Table 10-1. Configuration Register List of CDMA Controller

Register Name	R/W	Offset	Default
Vendor Identification Register (VID)	RO	0x00	1283h
Device Identification Register (DID)	RO	0x02	8152h
PCI Command Register (PCICMD)	R/W[Note1]	0x04	0005h
PCI Status Register (PCISTS)	R/WC[Note2]	0x06	0200h
Revision Register (RID)	RO	0x08	20h
Class Code Register (CLASSC)	RO	0x09	080103h
Latency Timer Register (LT)	R/W[Note3]	0x0D	80h
Base Address Register (BAR)	R/W[Note4]	0x10	43E11001h

The default value of the base address for the following registers is **0x43E11000**. Note that these registers can be re-allocated by changing the base address register.

Table 10-2. Operation Register List of CDMA Controller

Register Name	R/W	Offset	Default
Memory Address Register of Channel 0 (MAR0)	R/W	0x00	0h
Device Address Register of Channel 0 (DAR0)	R/W	0x04	0h
Byte Count Register of Channel 0 (BCR0)	R/W	0x08	0h
Descriptor Pointer Register of Channel 0 (DPR0)	R/W[Note5]	0x0C	0h
Memory Address Register of Channel 1 (MAR1)	R/W	0x10	0h
Device Address Register of Channel 1 (DAR1)	R/W	0x14	0h
Byte Count Register of Channel 1 (BCR1)	R/W	0x18	0h
Descriptor Pointer Register of Channel 1 (DPR1)	R/W[Note5]	0x1C	0h
Memory Address Register of Channel 2 (MAR2)	R/W	0x20	0h
Device Address Register of Channel 2 (DAR2)	R/W	0x24	0h
Byte Count Register of Channel 2 (BCR2)	R/W	0x28	0h
Descriptor Pointer Register of Channel 2 (DPR2)	R/W[Note5]	0x2C	0h
Memory Address Register of Channel 3 (MAR3)	R/W	0x30	0h
Device Address Register of Channel 3 (DAR3)	R/W	0x34	0h
Byte Count Register of Channel 3 (BCR3)	R/W	0x38	0h
Descriptor Pointer Register of Channel 3 (DPR3)	R/W[Note5]	0x3C	0h
Mode Register of Channel 0 (MR0)	R/W[Note6]	0x40	20h
Mode Register of Channel 1 (MR1)	R/W[Note6]	0x44	20h
Mode Register of Channel 2 (MR2)	R/W[Note6]	0x48	20h
Mode Register of Channel 3 (MR3)	R/W[Note6]	0x4C	20h
Command/Status Register of Channel 0 (CSR0)	R/W[Note7]	0x50	0h
Command/Status Register of Channel 1 (CSR1)	R/W[Note7]	0x54	0h

Table 10-2. Operation Register List of CDMA Controller (cont'd)

Register Name	R/W	Offset	Default
Command/Status Register of Channel 2 (CSR2)	R/W[Note7]	0x58	0h
Command/Status Register of Channel 3 (CSR3)	R/W[Note7]	0x5C	0h
Priority Type Register (PTR)	R/W[Note8]	0x60	0h

Definition of R/W Attributes:

RO **READ ONLY**. If a register is read only, writes to this register will have no effects.
R/W **READ/WRITE**. A register with this attribute can be read and written.
R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 has no effects.

Note 1: Bits 0, 6 in the register are read/write. Other bits are read only.
Note 2: Bits 11 - 13 in the register are read/write clear. Other bits are read only.
Note 3: Bits 0 - 2 in the register are read only. Other bits are read/write.
Note 4: Bits 0 - 7 in the register are read only. Other bits are read/write.
Note 5: Bit 0 in the register is read only. Other bits are read/write.
Note 6: Bits 7, 16 - 31 in the register are read only. Other bits are read/write.
Note 7: Bits 3 - 5 in the register are read/write clear. Bits 6 - 31 in the register are read only. Other bits are read/write.
Note 8: Bit 0 in the register is read/write. Other bits are read only.

10.5.1 CDMA Configuration Registers (Function 1)

The following registers are the standard PCI-specific configuration registers.

10.5.1.1 Vendor Identification Register (VID) — VID, Offset 0x00-0x11

Bit	R/W	Default	Description
15-0	RO	1283h	**Vendor ID (VID)** This is a 16-bit value assigned to ITE.

10.5.1.2 Device Identification Register (DID) — DID, Offset 0x02-0x03

Bit	R/W	Default	Description
15-0	RO	8152h	**Device ID (DID)** This is a 16-bit value assigned to the IT8152.

10.5.1.3 PCI Command Register (PCICMD) — PCICMD, Offset 0x04-0x05

Bit	R/W	Default	Description
15-10	RO	0h	**Reserved**
9	RO	0	**Fast Back-to-Back Enable (FB2BE)** Not implemented. This bit is always 0.
8	RO	0	**SERR # Enable (SERRE)** Not implemented. This bit is always 0.
7	RO	0	**Address/Data Stepping (ADS)** Not implemented. This bit is always 0.
6	R/W	0	**Parity Error Response (PER)** When this bit is set to 1, the Data Parity Error Detected can be reported. When this bit is set to 0, the Data Parity Error Detected is ignored.
5	RO	0	**Video Pallet Snooping (VPS)** Not implemented. This bit is always 0.
4	RO	0	**Memory Write and Invalidate Enable (MWIE)** Not implemented. This bit is always 0.
3	RO	0	**Special Cycle Enable (SCE)** Not implemented. This bit is always 0.
2	RO	1	**Bus Master Enable (BME)** This bit is always 1. Disabling of bus master capability on PCI bus is not supported.
1	RO	0	**Memory Access Enable (MAE)** This bit is hardwired to 0 for not allowing this device to respond to Memory Space accesses.
0	R/W	1	**I/O Access Enable (IOAE)** A value of 1 allows CDMA to respond to PCI I/O space accesses. A value of 0 disables it.

10.5.1.4 PCI Status Register (PCISTS) — PCISTS, Offset 0x06-0x07

Bit	R/W	Default	Description
15	RO	0	**Detected Parity Error (DPE)** This bit is not implemented.
14	RO	0	**Signaled System Error (SSE)** This bit is not implemented.
13	R/WC	0	**Received Master Abort (RMA)** When this device terminates a PCI transaction with a master abort, this bit is set to 1. This bit is cleared by writing a 1 to it.
12	R/WC	0	**Received Target Abort (RTA)** This bit is set to 1 when a PCI transaction issued by this master device is terminated with Target-Abort. This bit is cleared by writing a 1 to it.
11	R/WC	0	**Signaled Target Abort (STA)** This bit is set to 1 when this target terminates a transaction with Target-Abort. This bit is cleared by writing a 1 to it.
10-9	RO	01	**DEVSEL Timing (DEVT)** These two bits are set to 01b (medium) to indicate the slowest time that DEVSEL# is asserted.
8	RO	0	**Data Parity Error Detected (DPED)** This bit is not implemented.
7	RO	0	**Fast Back-to-Back Capable (FB2BC)** This bit is always 0 when the Fast Back-to-Back is not implemented.
6	RO	0	**UDF Supported (UDF)** This bit is always 0 because UDF is not supported.
5	RO	0	**66 MHz Capable (66C)** The 66 MHz PCI is not supported. This bit is always 0.
4-0	RO	0h	**Reserved**

10.5.1.5 Revision ID Register (RID) — RID, Offset 0x08

Bit	R/W	Default	Description
7-0	RO	**10h**	**Revision ID (RID)** This field contains the revision number of the device. The current ASIC revision number is **1.0**.

10.5.1.6 Class Code Register (CLASSC) — CLASSC, Offset 0x09-0x0B

Bit	R/W	Default	Description
23-16	RO	08h	**Base Class Code (BASEC)** 08h = Base system peripherals.
15-8	RO	01h	**Sub-Class Code (SCC)** 01h = DMA Controller.
7-0	RO	03h	**Programming Interface (PI)** 03h = PCI DMA Controller.

10.5.1.7 Latency Timer Register (LT) — LT, Offset 0x0D

Bit	R/W	Default	Description
7-0	R/W	80h	**Latency Timer (LT)** The number of clocks programmed represents the guaranteed time slice (measured in PCI clocks) allocated to this device, after which it must surrender the bus as soon as other PCI masters request the bus.

10.5.1.8 Base Address Register (BAR) — BAR, Offset 0x10

Bit	R/W	Default	Description
31-8	R/W	43E110h	**I/O Base Address (IOBA)** This field defines the I/O base address for the CDMA Operation Registers. The default PCI I/O base address is 43E11000h.
7-1	RO	0	**Reserved**
0	RO	1	**I/O Space Indicator (IOSI)** This bit always reads back a "1", indicating that this base address register defines a PCI I/O space.

10.5.2 CDMA Operation Registers

The following registers are the CDMA Operation Registers used to control the operation of the CDMA controller. Address space mentioned in the following registers (except MAR) is PCI address space.

10.5.2.1 Memory Address Register of Channel n (MARn)

A 26-bit address in SDRAM space (not in PCI space) is expected in this register.

MAR0, I/O Offset: 0x00
MAR1, I/O Offset: 0x10
MAR2, I/O Offset: 0x20
MAR3, I/O Offset: 0x30

Bit	R/W	Default	Description
31-26	RO	0	**Reserved**
25-0	R/W	0	**Memory Address (MA)** This field indicates the starting memory address of a DMA transfer.

10.5.2.2 Device Address Register of Channel n (DARn)

DAR0, I/O Offset: 0x04
DAR1, I/O Offset: 0x14
DAR2, I/O Offset: 0x24
DAR3, I/O Offset: 0x34

Bit	R/W	Default	Description
31-0	R/W	0	**Device Address (DA)** This field indicates the starting device address of a DMA transfer.

10.5.2.3 Byte Count Register of Channel n (BCRn)

BCR0, I/O Offset: 0x08
BCR1, I/O Offset: 0x18
BCR2, I/O Offset: 0x28
BCR3, I/O Offset: 0x38

Bit	R/W	Default	Description
31-0	R/W	0	**Byte Count (BC)** This field indicates the number of bytes to be transferred during a DMA transfer. It will be cleared by hardware when the transfer is finished normally.

10.5.2.4 Descriptor Pointer Register of Channel n (DPRn)

DPR0, I/O Offset: 0x0C
DPR1, I/O Offset: 0x1C
DPR2, I/O Offset: 0x2C
DPR3, I/O Offset: 0x3C

Bit	R/W	Default	Description
31-4	R/W	0	**Next Descriptor Address (NDA)** This field indicates the double word aligned address (Bit3-0 = 0000) of next descriptor.
3	R/W	0	**Direction of Transfer (DT)** A value of 1 indicates transfers from Memory to PCI Device. A value of 0 indicates transfers from PCI Device to Memory. 1: M2D. 0: D2M.
2	R/W	0	**Descriptor Done Interrupt Enable (DDIE)** A value of 1 causes an interrupt to be generated after the terminal count for this descriptor is reached. A value of 0 disables interrupts from being generated.
1	R/W	0	**End of Chain (EC)** A value of 1 indicates the end of chain.
0	-	0	**Reserved**

10.5.2.5 Mode Register of Channel n (MRn)

MR0, I/O Offset: 0x40
MR1, I/O Offset: 0x44
MR2, I/O Offset: 0x48
MR3, I/O Offset: 0x4C

Bit	R/W	Default	Description
31-16	RO	0	**Reserved**
15-8	R/W	0	**Transfer Limit of each PCI Transaction (TLPT)** This field is used to limit the data phase number of each PCI transaction. It is useful to control the time-sharing when rotating priority is selected. Only the five high-order bits are implemented, resulting in a granularity of eight. A value of 0 will disable this function.
7	RO	0	**Reserved**
6	R/W	0	**Transfer Error Interrupt Enable (TEIE)** A value of 1 enables the interrupt to be generated when a transfer error has occurred.
5-4	R/W	0	**Device Transfer Type (DTT)** This field is only meaningful when DAT is set to 1. It indicates the transfer size of each PCI I/O transaction and it must be consistent with Byte Count. 00: Byte access. 01: Word access. 1x: Double word access.
3	R/W	0	**Device Addressing Type (DAT)** A value of 1 indicates device address is within PCI I/O space. A value of 0 indicates device address is within PCI Memory space. 1: PCI I/O. 0: PCI Memory.
2	R/W	0	**Device Addressing Mode (DAM)** A value of 1 indicates device address will be held constant. A value of 0 indicates the device address is incremented. This bit can only be set when PCI I/O address is selected. 1: Fixed. 0: Incremented.
1	R/W	0	**Transfer Done Interrupt Enable (TDIE)** A value of 1 enables the interrupt to be generated when transfer is done.
0	R/W	0	**Chaining Mode (CM)** A value of 1 causes the DMA controller to operate in Chaining mode. 1: Chaining mode. 0: Non-chaining mode.

10.5.2.6 Command/Status Register of Channel n (CSRn)

CSR0, I/O Offset: 0x50
CSR1, I/O Offset: 0x54
CSR2, I/O Offset: 0x58
CSR3, I/O Offset: 0x5C

Bit	R/W	Default	Description
31-6	RO	0	**Reserved**
5	R/WC	0	**Transfer Error (TE)** A value of 1 indicates the controller encounters an error in the process of transfer. The error may be due to incorrect transfer parameters or PCI abort situation has happened. Writing a 1 will clear this bit and the interrupt due to this event when TEIE is set to 1.
4	R/WC	0	**Descriptor Done (DD)** A value of 1 indicates the transfer of current descriptor is complete. Writing a 1will clear this bit and the interrupt due to this event when DDIE is set to 1.
3	R/WC	0	**Transfer Done (TD)** A value of 1 indicates the transfer of this channel is complete. Writing a 1 will clear this bit and the interrupt due to this event when TDIE is set to 1.
2	R/W	0	**Transfer Abort (TA)** Writing a 1 to this bit causes the channel to abort the current transfer. The channel enable bit must be cleared. This channel transfer done bit is set when the abort is complete. Reading this bit always gets 0.
1	R/W	0	**Transfer Start (TS)** Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled. Reading this bit always gets 0.
0	R/W	0	**DMA Enable (DE)** A value of 1 enables this DMA channel.

10.5.2.7 Priority Type Register (PTR) — PTR, I/O Offset 0x60

Bit	R/W	Default	Description
31-1	-	-	**Reserved**
0	R/W	0	**Priority Type (PT)** A value of 1 indicates the priority type is rotating type. Channel will be arbitrated for each normally terminated PCI transaction. A value of 0 indicates the priority type is fixed type. When the fixed type is selected, channel 0 has the highest priority. 1: Rotating priority. 0: Fixed priority.

11. Audio Digital Controller

11.1 Overview

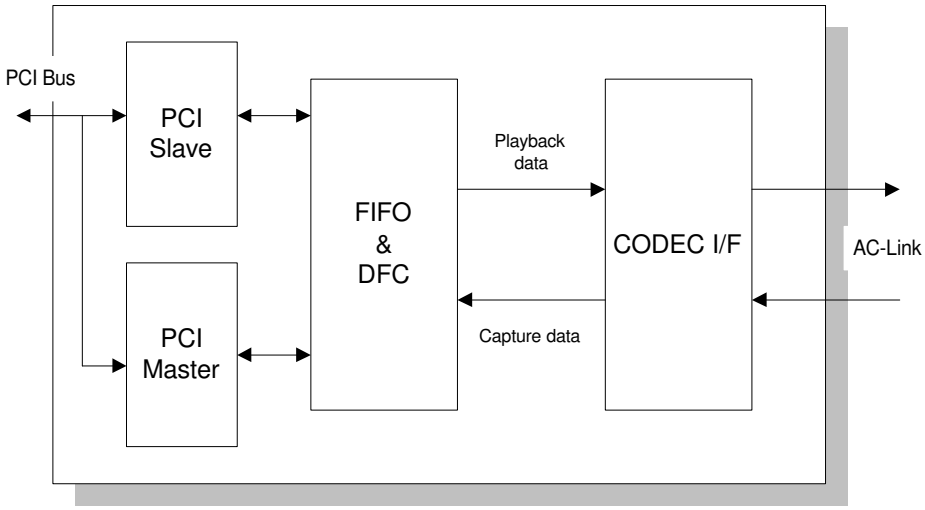
This module is a digital audio controller which supports full-duplex playback and recording. Combined with high-performance AC97 Codec, this controller provides the most cost -effective yet high quality audio experience to users.

The Audio Digital Controller is PCI function 3 in IT8152.

11.2 Features

- PCI v.2.1 compliant with bus master and scatter-and-gather capability
- 2 output channels and 2 input channels
- Support AC97 AC -link 2.0

11.3 Block Diagram



11.4 Configuration Register Descriptions

Register Name	R/W	Offset	Default
Vendor Identification Register (VID)	RO	0x00	1283h
Device Identification Register (DID)	RO	0x02	0801h
PCI Command Register (PCICMD)	R/W	0x04	0000h
PCI Status Register (PCISTS)	R/WC	0x06	0200h
Revision ID Register (RID)	RO	0x08	B1h
Class Code Register (CLASSC)	RO	0x09	040000h
Latency Timer Register (LT)	R/W	0x0D	00h
Header Type Register (HEADT)	RO	0x0E	00h
Base Address Register (BAR)	R/W	0x10	43E10801h
Sub-system Vendor ID Register(SVID) (shadow of 0x9C~9D)	RO	0x2C	1283h
Sub-system ID Register (SID) (shadow of 0x9E~9F)	RO	0x2E	1283h
Capability Pointer Register (CP)	RO	0x34	DCh
Interrupt Line Register (ILR)	R/W	0x3C	00h
Interrupt Pin Register (IPR) (INTA#)	RO	0x3D	01h
Min Grant Period PCI for Burst Period Register (MGPBP)	RO	0x3E	04h
Max Latency for PCI Grant Period Register (MLPGP)	RO	0x3F	28h
Vendor ID Writeable Register (VIDW)	R/W	0x98	1283h
Device ID Writeable Register (DIDW)	R/W	0x9A	0801h
Sub-system Vendor ID Writeable Register (SVIDW)	R/W	0x9C	1283h
Sub-system ID Writeable Register (SIDW)	R/W	0x9E	1283h
DFC Reset Control Register (DRC)	R/W	0xA0	00h
Capability ID Register (CID)	RO	0xDC	01h
Next Item Pointer Register (NIP)	RO	0xDD	00h
Power Management Capability Register (PMC)	RO	0xDE	0421h
Power Management Control/Status Register (PMCS)	R/W	0xE0	0000h

Definitions of R/W Attributes:

RO **READ ONLY**. If a register is read only, writes to this register will have no effects.
R/W **READ/WRITE**. A register with this attribute can be read and written.
R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 has no effects.

11.4.1 Device/Vendor Identification Register (DID/VID)

DID, Offset: 0x02-0x03
VID, Offset: 0x00-0x01

Bit	R/W	Default	Description
31-16	RO	0801h	**Device ID (DID)** This is a 16-bit value assigned to this device.
15-0	RO	1283h	**Vendor ID (VID)** This is a 16-bit value assigned to ITE.

11.4.2 PCI Status/Command Register (PCISTS/PCICMD)

PCISTS, Offset 0x06-0x07
PCICMD, Offset: 0x04-0x05

Bit	R/W	Default	Description
31	R/WC	0	**Detected Parity Error (DPE)** When this bit is set to 1, it indicates that a parity error is detected even if parity error enable (**PERRE**) bit is disabled. When this bit is 0, it indicates that no parity error is detected. This bit is cleared by writing a 1 to itself.
30	RO	0	**Reserved**
29	R/WC	0	**Received Master Abort (RMA)** When this device terminates a PCI transaction with a master abort, this bit is set to 1. This bit is cleared by writing a 1 to itself.
28	R/WC	0	**Received Target Abort (RTA)** This bit is set to 1 when a PCI transaction issued by this master device is terminated with Target-Abort. This bit is cleared by writing a 1 to itself.
27	R/WC	0	**Reserved**
26-25	RO	01	**DEVSEL Timing (DEVT)** These two bits are hardwired to 01b (medium) to indicate the slowest time that DEVSEL# is asserted.
24	R/WC	0	**Reserved**
23	RO	1	**Fast Back-to-Back Capable (FB2BC)** This bit is always "1".
22	RO	0	**UDF Supported (UDF)** This bit is always 0 because UDF is not supported.
21	RO	0	**66 MHz Capable (66C)** The 66 MHz PCI is not supported. This bit is always 0.
20	RO	1	**Power Management Features (PM)** PCI Power Management features appear in the standard configuration space header. **Read Only**.
19-10	-	0h	**Reserved**
9	R/W	0	**Fast Back-to-Back Enable (FB2BE)** A value of 1 enables Fast Back-to-Back. A value of 0 disables Fast Back-to-Back.
8	R/W	0	**SERR # Enable (SERRE)** A value of 0 disables this device to generate SERR#. A value of 1 enables this device to generate SERR#.
7	RO	0	**Address/Data Stepping (ADS)** Not implemented. This bit is always 0.
6	R/W	0	**Reserved**
5	RO	0	**Video Palette Snooping (VPS)** Not implemented. This bit is always 0.

PCI Status/Command Register (PCISTS/PCICMD) [cont'd]

Bit	R/W	Default	Description
4	RO	0	**Memory Write and Invalidate Enable (MWIE)** Not implemented. This bit is always 0.
3	RO	0	**Special Cycle Enable (SCE)** Not implemented. This bit is always 0.
2	R/W	0	**Bus Master Enable (BME)** A value of 0 disables this device from generating PCI accesses. A value of 1 allows this device to behave as a bus master.
1	R/W	0	**Memory Access Enable (MAE)** A value of 0 disables this device's response to memory access. A value of 1 enables this device's response to memory access.
0	R/W	0	**I/O Access Enable (IOAE)** A value of 0 disables this device's response to I/O access. A value of 1 enables this device's response to I/O access.

11.4.3 Class Code/Revision ID Registers (CLASSC/RID)

CLASSC, Offset: 0x09-0x0Bb
RID, Offset: 0x08

Bit	R/W	Default	Description
31-24	RO	04h	**Base Class Code (BASEC)** Multimedia device.
23-16	RO	01h	**Sub Class Code (SCC)** 01h = Audio device.
15-8	RO	00h	**Programming Interface (PI)** 00h = Specific register-level programming interface.
7-0	RO	B1h	**Revision ID (RID)** This field contains the revision number of the device. B1h indicates the 3rd version.

11.4.4 BIST/Header Type/Latency Timer/Cache Line Size Registers (BIST/HEADT/LT/CALS)

BIST, Offset: 0x0F
HEADT, Offset: 0x0E
LT, Offset: 0x0D
CALS, Offset: 0x0C

Bit	R/W	Default	Description
31-24	-	-	**BIST (BIST)** The Built in Self Test (BIST) function is not supported by the device.
23-16	RO	00h	**Header Type (HEADT)** Header Type 00h indicates that the device's configuration space map follows the basic format.
15-8	R/W	00h	**Latency Timer (LT)** The number of clocks programmed represents the guaranteed time slice (measured in PCI clocks) allocated to this device, after which it must surrender the bus to the other PCI masters requesting for the bus. The default value is 00h.
7-0	-	-	**Cache Line Size (CALS)** The Cache Line Size is not supported by this device.

11.4.5 Base Address Register (BAR) — Offset 0x10

Bit	R/W	Default	Description
31-8	R/W	43E108h	**Base Address (BA)** This address determines the starting address of Audio Controller's I/O registers.

11.4.6 Sub-system Vendor ID Register (SVID) — Offset 0x2C

Bit	R/W	Default	Description
15-0	RO	1283h	**Sub-system Vendor ID (SVID)** Subsystem Vendor ID. These bits can be written by being programmed through 0x9C~9D.

11.4.7 Sub-system ID Register (SID) — Offset 0x2E

Bit	R/W	Default	Description
15-0	RO	1283h	**Sub-system ID (SID)** Sub-system ID. These bits can be written by being programmed through 0x9E~9F.

11.4.8 Capability Pointer Register (CP) — Offset 0x34

Bit	R/W	Default	Description
7-0	RO	DCh	**Capabilities Pointer (CP)** This register indicates where the PCI Power Management features appear in the standard configuration space header.

11.4.9 Interrupt Line Register (ILR) — Offset 0x3C

Bit	R/W	Default	Description
7-0	R/W	00h	**Interrupt Line (IL)** This register is used to communicate the interrupt line routing information.

11.4.10 Interrupt Pin Register (IPR) — Offset 0x3D

Bit	R/W	Default	Description
7-0	RO	01h	**Interrupt Pin (IP)** This register is hardwired to 01h, which indicates that this device uses INTA# as the interrupt pin.

11.4.11 Min Grant Period for PCI Burst Period Register (MGPBP) — Offset 0x3E

Bit	R/W	Default	Description
7-0	RO	04h	**Min Grant Period (MGP)** This register is used to specify how long of a burst period the device needs (in 1/4 microsecond unit). This device will use 1 μs burst period.

11.4.12 Max Latency for PCI Grant Period Register (MLPGP) — Offset 0x3F

Bit	R/W	Default	Description
7-0	RO	28h	**Max Latency (ML)** This register is used to specify how often the device needs (in 1/4 microsecond unit) to gain the access to the PCI bus. This device needs the PCI bus grant every 10 μs.

11.4.13 Vendor ID Writeable Register (VIDW) — Offset 0x98

Bit	R/W	Default	Description
15-0	R/W	1283h	**Vendor ID (VID)** ITE Vendor ID. The value of this register will also show in 00~01h.

11.4.14 Device ID Writeable Register (DIDW) — Offset 0x9A

Bit	R/W	Default	Description
15-0	R/W	0801h	**Device ID (DID)** The value of this register will also show in 02~03h.

11.4.15 Sub-system Vendor ID Writeable Register (SVIDW) — Offset 0x9C

Bit	R/W	Default	Description
15-0	R/W	1283h	**Sub-system Vendor ID (SVID)** The value of this register will also show in 2C~2Dh.

11.4.16 Sub-system ID Writeable Register (SIDW) — Offset 0x9E

Bit	R/W	Default	Description
15-0	R/W	1283h	**Sub-system ID (SID)** The value of this register will also show in 2E~2Fh.

11.4.17 DFC Reset Control Register (DRC) — Offset 0xA0

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	R/W	0	**DC Test Enable (DTE)**
1	R/W	0	**Reset DFC Pointer Enable 1 (RDPE1)** When receiving PLAYBACK START command, DFC pointer is reset if this bit is set to 1.
0	R/W	0	**Reset DFC Pointer Enable 0 (RDPE0)** When receiving PLAYBACK STOP command, DFC pointer is reset if this bit is set to 1.

11.4.18 Capability ID Register (CID) — Offset 0xDC

Bit	R/W	Default	Description
7-0	RO	01h	**Capability ID (CID)** A "01" indicates that the linked list items are the PCI Power Management Registers.

11.4.19 Next Item Pointer Register (NIP) — Offset 0xDD

Bit	R/W	Default	Description
7-0	RO	00h	**Next Item Pointer (NIP)** A "00" indicates that there are no additional items in the Capability list.

11.4.20 Power Management Capability Register (PMC) — Offset 0xDE

Bit	R/W	Default	Description
15-11	RO	00000	**PME Support (PMES)** A "00000" indicates that there is no PME support.
10	RO	1	**D2 Support (D2S)** 1: Yes (Shutdown 24 MHz clock, AC97 DAC, ADC, and Mixer). 0: No.
9	RO	0	**D1 Support (D1S)** 1: Yes, 0: No.
8-6	-	-	**Reserved**
5	RO	1	**Device Specific Initialization (DSI)** A "1" indicates that the function requires that an initialization sequence specified by a device, following a transition from the non-D0 uninitialized state to the D0 uninitialized state.
4	-	-	**Reserved**
3	RO	0	**PME Clock (PMECK)** A "0" indicates that no PCI clock is required to generate PME#.
2-0	RO	001	**Version Number (VN)**

11.4.21 Power Management Control/Status Register (PMCS) — Offset 0xE0

Bit	R/W	Default	Description
15	R/WC	0	**PME Status (PMES)** Writing "1" to this bit will clear it and cause the function to stop asserting a PME#. The default value of 0 indicates the function does not support PME# generation from the D3 cold state.
14-13	RO	00	**Data Scale (DSC)**
12-9	RO	00000	**Data Select (DSEL)**
8	R/W	0	**PME Enable (PMEE)**
7-2	-	-	**Reserved**
1-0	R/W	00	**Power State (PS)** The change of power state from D3 to D0 will cause the software reset.

11.5 Operation Register Description

The default value of the base address for all registers is **0x43E10800**. Note that these registers can be re-allocated by changing the base address register.

Register Name	R/W	Offset	Default
Playback Channel Control Register (PCC)	R/W	0x08	CA01h
Playback Channel Data Length/Current Count Register (PCDL/CC)	R/W	0x0A	-
Playback Channel Buffer I System Starting Address Register (PCB1STA)	R/W	0x0C	-
Playback Channel Buffer II System Starting Address Register (PCB2STA)	R/W	0x10	-
Capture Channel Control Register (CAPCC)	R/W	0x14	CA00h
Capture Channel Data Length/Current Count Register (CAPCDL/CC)	R/W	0x16	-
Capture Channel Buffer I System Starting Address Register (CAPB1STA)	R/W	0x18	-
Capture Channel Buffer II System Starting Address Register (CAPB2STA)	R/W	0x1C	-
Codec Control Register (CODECC)	R/W	0x22	0000h
Codec Index Register Command Port (CIRCP)	R/W	0x2A	0000h
Codec Index Register Data Port (CIRDP)	R/W	0x2C	-
PCI FIFO Data Port Register (PFDP)	R/W	0x4C	-
General Control Register (GC)	R/W	0x54	00h
Interrupt Mask Control Register (IMC)	R/W	0x56	03h
Interrupt Status/Clear Register (ISC)	R/WC	0x5B	00h
Blocks Power Down Control Register (BPDC)	R/W	0x70	00h

Definitions of R/W Attributes:

RO **READ ONLY**. If a register is read only, writes to this register will have no effects.
R/W **READ/WRITE**. A register with this attribute can be read and written.
R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 has no effects.

11.5.1 Playback Channel Control Register (PCC) — Offset 0x08

Bit	R/W	Default	Description
15	R/W	1	**Stereo/Mono (SM)** 0: Mono, 1: Stereo.
14	R/W	1	**Data Format (DF)** 0: 8-bit unsigned, 1: 16-bit signed.
13-8	-	-	**Reserved**
7	R/W	0	**Channel Stop Point (CSP)** 0: At the end of the current buffer. 1: Immediately stop when receiving Stop command.
6	R/W	0	**Channel Pause (CP)** 0: Normal. 1: Transfer Pause. (To pause, bit 5 has to remain at "1".)
5	R/W	0	**Channel Action (CA)** 0: Stop Transfer. 1: Start Transfer.
4-3	-	-	**Reserved**
2	R/W	0	**Current buffer II transfer is the last transfer (CB2L)** 0: No, 1: Yes.
1	R/W	0	**Current buffer I transfer is the last transfer (CB1L)** 0: No, 1: Yes.
0	RO	1	**DFC/PFIFO Data Empty (DE)** 1: Empty. 0: Not empty.

11.5.2 Playback Channel Data Length/Current Count Register (PCDL/CC) — Offset 0x0A

Bit	R/W	Default	Description
15-0	R/W	-	**Data Length/Current Count (DL/CC)** (write) DS Channel Data Length for buffer I and II (Have to be the same size for both buffers). The actual transfer count will be this register value plus 1. (read) DS Channel Data Current Remaining Count.(not available until playback starts.)

11.5.3 Playback Channel Buffer I System Starting Address Register (PCB1STA) — Offset 0x0C

Bit	R/W	Default	Description
31-0	R/W	-	**Buffer 1 Starting Address (B1SA)** (write) DS Playback Channel Buffer I System Starting Address. (read) DS Playback Channel Buffer I current address.

11.5.4 Playback Channel Buffer II System Starting Address Register (PCB2STA) — Offset 0x10

Bit	R/W	Default	Description
31-0	R/W	-	**Buffer 2 Starting Address (B2SA)** (write) DS Playback Channel Buffer II System Starting Address. (read) DS Playback Channel Buffer II current address.

11.5.5 Capture Channel Control Register (CAPCC) — Offset 0x14

Bit	R/W	Default	Description
15	R/W	1	**Stereo/Mono (SM)** 0: Mono. 1: Stereo.
14	R/W	1	**Data Format (DF)** 0: 8-bit unsigned. 1: 16-bit signed.
13-8	-	-	**Reserved**
7	R/W	0	**Channel Stop Point (CSP)** 0: At the end of current buffer. 1: Immediately stop when receiving Stop command.
6	R/W	0	**Channel Pause (CP)** 0: Normal. 1: Transfer Pause. (To pause, the bit 5 has to remain at "1".)
5	R/W	0	**Channel Action (CA)** 0: Stop Transfer. 1: Start Transfer.
4-3	-	-	**Reserved**
2	R/W	0	**Current buffer II transfer is the last transfer (CB2L)** 0: No, 1: Yes.
1	R/W	0	**Current buffer I transfer is the last transfer (CB1L)** 0: No, 1:Yes.
0	-	-	**Reserved**

11.5.6 Capture Channel Data Length/Current Count Register (CAPCDL/CC) — Offset 0x16

Bit	R/W	Default	Description
15-0	R/W	-	**Data Length/Current Count (DL/CC)** (write) DS Channel Data Length for buffer I and II (Have to be the same size for both buffers). The actual transfer count will be this register value plus 1. (read) DS Channel Data Current Remaining Count.(not available until playback starts)

11.5.7 Capture Channel Buffer I System Starting Address Register (CAPB1STA) — Offset 0x18

Bit	R/W	Default	Description
31-0	R/W	-	**Buffer 1 Starting Address (B1SA)** (write) DS Capture Channel Buffer I System Starting Address. (read) DS Capture Channel Buffer I current address.

11.5.8 Capture Channel Buffer II System Starting Address Register (CAPB2STA) — Offset 0x1C

Bit	R/W	Default	Description
31-0	R/W	-	**Buffer 2 Starting Address (B2SA)** (write) DS Capture Channel Buffer II System Starting Address. (read) DS Capture Channel Buffer II current address.

11.5.9 Codec Control Register (CODECC) — Offset 0x22

Bit	R/W	Default	Description
15-9	-	-	**Reserved**
8	R/W	0	**AC'97 ATE Test Mode (ATM)** 1: ATE Test Mode On, 0: Normal.
7	-	-	**Reserved**
6	R/W	0	**AC'97 Warm Reset (WR)** 1: Warm Reset, 0: Normal.
5	R/W	0	**AC'97 Cold Reset (CR)** 1: Cold Reset, 0: Normal.
4-0	-	-	**Reserved**

11.5.10 Codec Index Register Command Port (CIRCP) — Offset 0x2A

Bit	R/W	Default	Description
15-10	-	-	**Reserved**
9	RO	0	**Command Port Status (CPS)** 0: Ready, 1: Busy.
8	RO	0	**Data Port Valid Flag (DPVF)** 0: Invalid, 1: Valid.
7	R/W	0	**Read/Write Command (RWC)** 0: Write, 1: Read.
6-0	R/W	-	**Codec Index Address (CIA)**

11.5.11 Codec Index Register Data Port (CIRDP) — Offset 0x2C

Bit	R/W	Default	Description
15-0	R/W	-	**Codec Register Data Port (CDP)**

11.5.12 PCI FIFO Data Port Register (PFDP) — Offset 0x4C

Bit	R/W	Default	Description
31-0	R/W	-	**PCI FIFO Data Port (PFDP)** Playback/Capture FIFO Data Port.

11.5.13 General Control Register (GC) — Offset 0x54

Bit	R/W	Default	Description
7-6	R/W	00	**Volume Division Control (VDC)** 00: No division, 01: All sources divided by 2, 10: Divided by 4.
5-2	-	-	**Reserved**
1	-	0	**Reserved**
0	R/W	0	**Software Warm Reset (SWR)** 1: Software Warm Reset, 0: Normal.

11.5.14 Interrupt Mask Control Register (IMC) — Offset 0x56

Bit	R/W	Default	Description
7	-	-	**Reserved** Note: Do not write 0 to this bit.
6-2	-	-	**Reserved**
1	R/W	1	**Capture Channel Interrupt Mask (CCIM)** 1: Mask, 0: Non-Mask.
0	R/W	1	**Playback Channel Interrupt Mask (PCIM)** 1": Mask, 0: Non -Mask.

11.5.15 Interrupt Status/Clear Register (ISC) — Offset 0x5B

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/WC	0	**Capture Channel Interrupt (CCI)** A write of "1" will clear the interrupt. A write of "0" will have no effects.
0	R/WC	0	**Playback Channel Interrupt (PCI)** A write of "1" will clear the interrupt. A write of "0" will have no effects.

11.5.16 Blocks Power Down Control Register (BPDC) — Offset 0x70-0x71

Bit	R/W	Default	Description
15-9	-	-	**Reserved**
8	R/W	0	**PCI Clock can be Turn Off (PCTF)** 1: Ready, 0: Not ready to power down.
7-0	-	-	**Reserved**

11.6 Protocol and Data Flow

11.6.1 Codec DAC and ADC Data Access

Codec I/F will read the DAC data (left and right channels) from DFC (Data Format Control) when slot request sent from CODEC is active. If the underrun condition occurs, the same DAC data have to remain in the buffer of the Digital Mixer for Codec I/F to access. Codec I/F will write the ADC data (left and right channels) to the DFC. When the overrun condition occurs, the new data will overwrite the previous data.

11.6.2 Codec Control Register Access

1. Host can access the Codec index registers through the control register (0x2A~2D). For register writes, the Host has to poll the bit 9 of the Codec Index Register Command Port (0x2A~2B) first until it is ready. After users make sure that Hw is ready to access the Codec registers, the host can program the data port (0x2C~2D) first, then it should issue the "write command" and the index address to register 0x2A to trigger the Hw to start programming Codec.

2. For register reads from Codec, the Host has to poll the bit 9 of the Codec Index Register Command Port (0x2A~2B) first until it is ready. The Host is then allowed to issue the "read command" and the address to register 0x2A. To read the data, Host starts to poll the bit 8 of the Codec Index Register Command Port until it is set before it can read the data from data port at 0x2C~2D.

11.6.3 DirectSound Playback

1. Program the Playback Channel Data Length Register (0x0A~0x0B) and Playback Buffer I & II System Starting Address Registers (0x0C~0x13) with the proper value.
2. Set playback WAVE format by setting Stereo or Mono, 8-bit or 16-bit and the sampling rate at the Playback Channel Control Register (0x08~09).
3. Fill the buffer 1 and buffer 2 with the playback data. Set the bit 5 of the Playback Channel Control Register (0x08~09) to "1" to start the PC I bus-master transfer for playback.
4. Playback current address can be read from the Playback Channel Buffer Address Register (0x0C~0x0F or 0x10~0x13). Playback current remaining count can be read from the Playback Channel Current Count Register (0x0A~0x0B) to determine where the Hw pointer is. The interrupt status will be generated when the current count reaches '0".
5. When the current count reaches '0", Hw will switch to buffer 2 starting address to transfer the data (ping-pong buffers scheme) and the current count will be re-loaded and start from data length again. In the meantime, the driver has to start filling the data in the buffer 1.
6. To pause the playback operations, set the bit 6 of the Playback Channel Control Register (0x08~09) to "1". To resume, just restore '0" to the bit 6.
7. To stop/finish playback, set the bit 7 of the Playback Channel Control Register (0x08~09) to "1" and the bit 5 to '0".

11.6.4 DirectSound Recording

1. Program the Capture Channel Data Length Register (0x16~0x17) and the Capture Channel Buffer I & II System Starting Address Registers (0x18~0x1F) with the proper value.
2. Set Recording WAVE format by setting Stereo or Mono, 8-bit or 16-bit and the sampling rate at the Capture Channel Control Register (0x14~15).
3. Set the bit 5 of the Capture Channel Control Register (0x14~15) to "1" to start the PCI bus -master transfer for Recording.
4. Capture current address can be read from the Capture Channel Buffer I or II System Starting Address Register (0x18~0x1B or 0x1C~0x1F). The Capture current remaining count can be read from the Capture Channel Current Count Register (0x16~0x17) to determine where the Hw pointer is. The interrupt status will be generated when the current count reaches '0".
5. When the current count reaches '0", Hw will switch to buffer 2 st arting address to transfer the data (ping-pong buffers scheme) and the current count will be re-loaded and start from the data length again. In the mean time, the driver has to move the data in the buffer 1 to the system.
6. To pause the recording, set the bit 6 of the Capture Channel Control Register (0x14~15) to "1". To resume, just restore '0" to the bit 6.
7. To stop/finish Recording, set the bit 7 of the Capture Channel Control Register (0x14~15) to "1" and the bit 5 to '0".