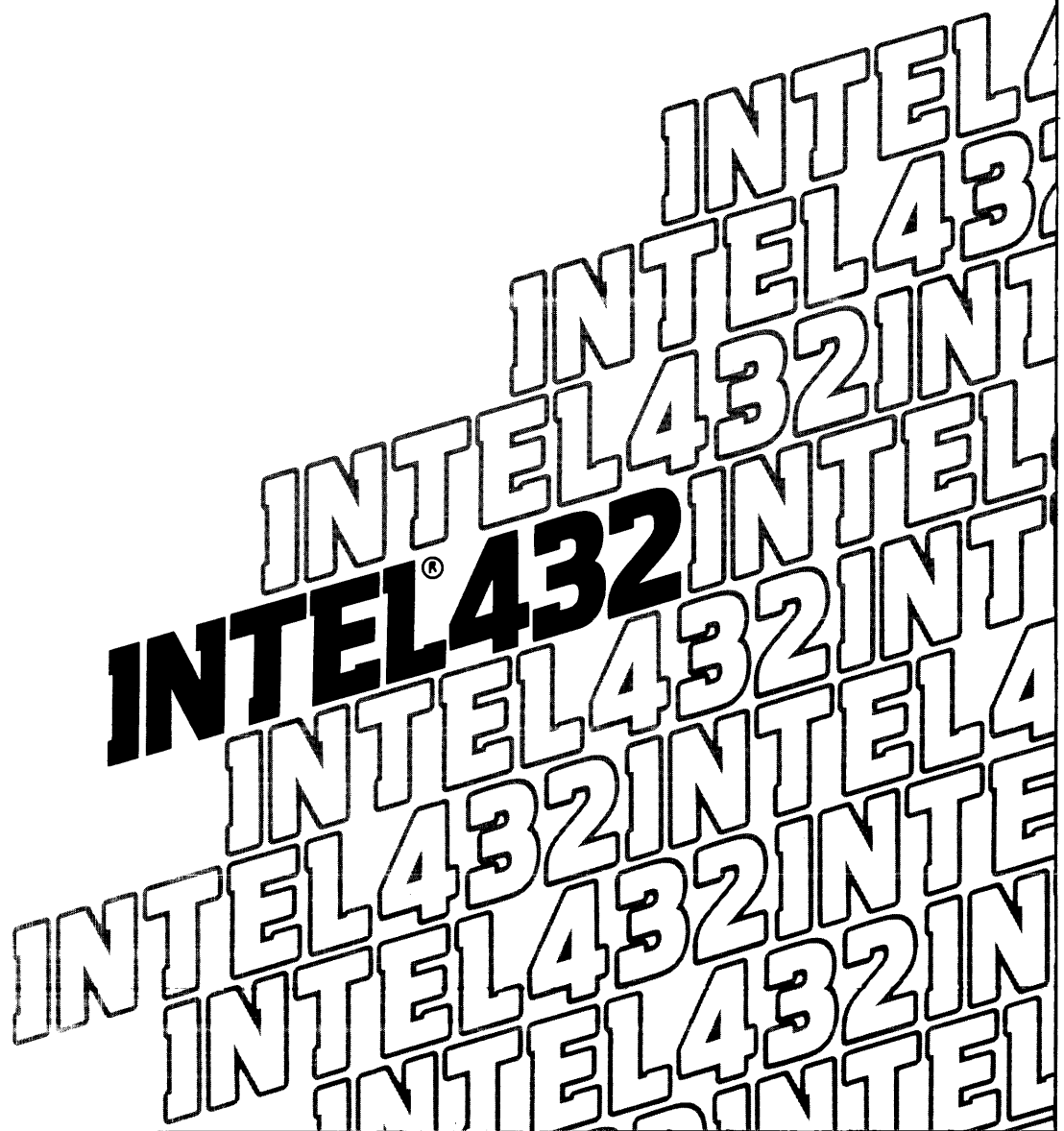# intel®

iSBC 432/100™
Processor Board
Hardware Reference Manual

INTEL432

iSBC 432/100™
PROCESSOR BOARD
HARDWARE REFERENCE MANUAL

Manual Order Number: 171820-001

Additional copies of this manual or other Intel literature may be obtained from:

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This manual contains general information, installation, programming information, and principles of operation for the Intel iSBC 432/100 Processor Board. Additional hardware/architectural information pertaining to the iSBC 432/100 board is available in the following documents:

* *iAPX 432 General Data Processor Architecture Reference Manual*, Order No. 171860-001.

* *Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter*, Application Note AP-16.

* *Intel Multibus Specification*, Order No 9800683.

* *Intel Multibus Interfacing*, Application Note AP-28.

Introductory iAPX 432 information, if required, is contained in the following documents:

* *The iAPX 432 Object Primer*, Order No. 171858-001.

* *Introduction to the iAPX 432 Architecture*, Order No. 171821-001.

* *Getting Started on the Intellec 432/100*, Order No. 171819-001.

* *Object Builder User's Guide*, Order No. 171859-001.

* *Object Programming Language User's Manual*, Order No. 171823-001.

CONTENTS

TABLES

ILLUSTRATIONS

1.1 INTRODUCTION

The iSBC 432/100 Processor Board is a Multibus-compatible implementation of the iAPX 432 Micro-mainframe, a 32-bit VLSI microprocessor. This board is designed to operate as a Multibus master in Intellec microcomputer systems. The iSBC 432/100 board contains an iAPX 432 microprocessor, a serial communications interface, programmable timers, Multibus control logic, and bus expansion drivers for interfacing with other Multibus-compatible boards.

1.2 DESCRIPTION

The iSBC 432/100 Processor Board (figure 1-1) is controlled by an iAPX 432 General Data Processor (GDP). The GDP consists of two VLSI components: the 43201 Instruction Decode Unit and the 43202 Instruction Execution Unit. The GDP's instruction set supports a wide range of data addressing modes and data manipulation operations, as well as highly efficient and secure protection mechanisms. The iSBC 432/100 board accesses the Multibus system bus for all memory and I/O operations.

An RS-232-C compatible serial I/O port, controlled by an Intel 8251A USART (Universal Synchronous/Asynchronous Receiver/Transmitter), operates with standard CRT terminals at baud rates from 110 to 19.2K bits/second. The USART is individually programmable for operation in many synchronous and asynchronous serial data transmission formats (including IBM Bi-sync). In operation, most transmission characteristics (e.g., character length, parity, and baud rate) are programmable.

In both the synchronous and asynchronous modes, the serial I/O port features half- or full-duplex, double buffered transmit and receive capability. In addition, USART error detection circuits can check for parity, overrun, and framing errors. The USART transmit and receive clocks are supplied by a programmable baud rate generator. The RS-232-C control lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector (in the upper right corner of the board) that mates with flat or round cable (through a standard board edge connector).
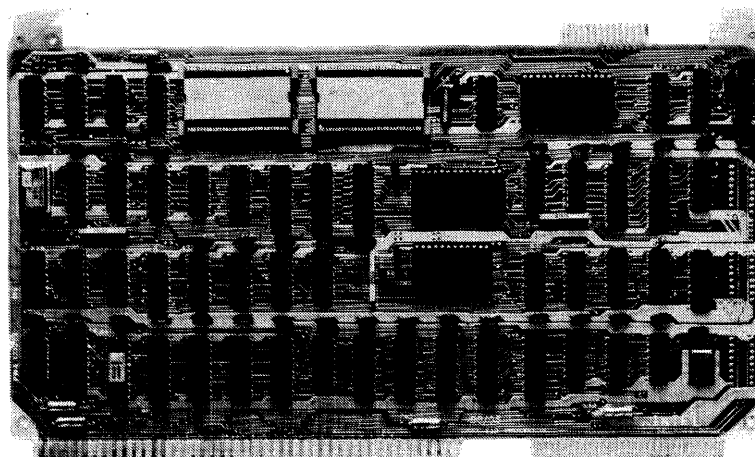
Figure 1-1. iSBC 432/100™ Processor Board

171820-1

Three programmable 16-bit interval timers are provided by an Intel 8253 Programmable Interval Timer (PIT). All three timers are reserved for processor time base generation and serial I/O baud rate generation. Additional on-board I/O registers, containing processor control and status information, may be accessed from the Multibus bus.

The iSBC 432/100 board provides full Multibus arbitration control logic. This control logic allows up to three bus masters to share the Multibus bus in serial (daisy-chain) fashion or up to 16 bus masters to share the Multibus bus using an external parallel priority resolution network. The Multibus aribtration logic operates synchronously with the bus clock, which is derived from another Multibus master or generated by customer supplied logic. (The iSBC 432/100 board does not generate the bus clock signal.) Data is transferred by means of a handshake between the controlling master and the addressed bus module. This arrangement allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. The transfer speed is dependent on the transmitting and receiving devices only. This design prevents slower master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data over the same bus.

1.3 EQUIPMENT SUPPLIED

The following items are supplied with the iSBC 432/100 Processor Board:

a.   Schematic diagram, drawing no. 171773

b.   Assembly drawing, drawing no. 171826

1.4 EQUIPMENT REQUIRED

The iSBC 432/100 Processor Board is designed to operate in an Intellec 800, Intellec Series II, or Intellec Series III Microcomputer Development System.

1.5 SPECIFICATIONS

Specifications of the iSBC 432/100 Processor Board are listed in table 1-1.

Table 1-1. iSBC 432/100™ Specifications

Word Size		
Instruction:	Variable, 6 bits to 271 bits.	
Data:	8, 16, 32, 64, or 80 bits.	

Memory Addressing		
Physical:	1 Megabyte RAM, ROM, or EPROM.	
Virtual:	2^{40} bytes	

Serial Communications			
Synchronous:	5-, 6-, 7-, or 8-bit characters. One or two sync characters. Automatic sync insertion.		
Asynchronous:	5-, 6-, 7-, or 8-bit characters. Break character generation. 1, 1½, or 2 stop bits. False start bit detection.		
Sample Baud Rate:	**Frequency**[1] **(kHz, software selectable)**	**Baud Rate (Hz)**[2] **Synchronous**	**Asynchronous**
			16 64
	307.2	—	19200 4800
	153.6	—	9600 2400
	76.8	—	4800 1200
	38.4	38400	2400 600
	19.2	19200	1200 300
	9.6	9600	600 150
	4.8	4800	300 75
	2.4	2400	150 —
	1.76	1760	110 —

Table 1-1. iSBC 432/100™ Specifications (Cont'd.)

	Notes:
	1. Frequency selected by I/O writes of appropriate 16-bit frequency factor into 8253 PIT registers.
	2. Baud rates shown here are only a sample subset of possible software programmable rates available. Any frequency from 37.5 to 614.4 kHz may be generated utilizing the on-board crystal oscillator and 16-bit PIT.
Interval Timer and Baud Rate Generator	
Input Frequency:	1.228 MHz ± 0.1% (.82 microsecond nominal period).
Output Frequencies:	Rate Generator: 37.5 Hz to 614.4 kHz Process Clock: 3.25 microseconds to 58.25 minutes. (cascaded timers)
I/O Addressing	On-board I/O devices recognize an 8-bit I/O address. iSBC 432/100 local accesses are translated to Multibus I/O accesses.
Interface Compatibility Serial I/O:	EIA standard RS-232-C signals provided and supported: Clear to Send Transmitted Data Request to Send Received Data Data Set Ready Data Terminal Ready
Interrupts:	The 432 CPU can generate a single interrupt on the Multibus INT5/, INT6/, or INT7/ lines.
Compatible Connectors/Cables:	Refer to Table 2-1 for compatible connector details. Refer to paragraph 2-15 for recommended types and lengths of I/O cables.
Environmental Requirements:	0° to 50° C (32° to 122° F)
Relative Humidity:	To 90% without condensation.
Physical Characteristics Width: Height: Thickness: Weight:	 30.48 cm (12.00 inches) 17.15 cm (6.75 inches) 1.52 cm (0.6 inches) 453.6 gm (16 ounces)
Power Requirements + 5V ± 5% at 4.5 A +12V ± 5% at 40 mA −12V ± 5% at 40 mA	

2.1 INTRODUCTION

This chapter provides instructions for configuring the iSBC 432/100 Processor Board for operation in a user-defined environment. It is advisable that the contents of Chapters 1 and 3 be fully understood before beginning the configuration and installation procedures described in this chapter.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the customer letter contained in the shipping carton. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

2.3 INSTALLATION CONSIDERATIONS

The iSBC 432/100 board is designed for use as a bus master in an Intellec 800, Intellec Series II, or Intellec Series III Microcomputer Development System. Important criteria for installing and interfacing the iSBC 432/100 board in this configuration are presented in the following paragraphs.

Table 2-1. Connector Details

Function	No. of Pairs/ Pins	Centers (inches)	Connector Type	Vendor	Vendor Part No.	Intel® Part No.
Serial I/O Connector	13/26	0.1	Flat Crimp	3M AMP ANSLEY SAE	3462-0001 88106-1 609-2615 SD6726 SERIES	iSBC 955 Cable Set
Serial I/O Connector	13/26	0.1	Soldered	TI AMP	H312113 1-583485-5	N/A
Serial I/O Connector	13/26	0.1	Wirewrap[1]	TI	H311113	N/A
Multibus Connector	43/86	0.156	Soldered[1]	CDC[3] MICRO PLASTICS ARCO VIKING	VPB01E43D00A1 MP-0156-43-BW-4 AE443WP1 LESS EARS 2VH43/1AV5	N/A
Multibus Connector	43/86	0.156	Wirewrap [1,2]	CDC[3] CDC[3] VIKING	VFB01E43D00A1 or VPB01E43A00A1 2VH43/1AV5	MDS 985*

NOTES:

1. Connector heights are not guaranteed to conform to OEM packaging requirements.

2. Wirewrap pin lengths are not guaranteed to conform to OEM packaging requirements.

3. CDC VPB01..., VPB02..., VPB04..., etc. are identical connectors with different electroplating thickness or metal surfaces.

*"MDS" is an ordering code only, and is not used as a product name or trademark. MDS® is a registered trademark of Mohawk Data Sciences Corp.

2.4 USER FURNISHED COMPONENTS

A serial I/O connector (see table 2-1) and RS-232-C cable must be installed to interface the processor board to a CRT terminal.

2.5 POWER REQUIREMENTS

The iSBC 432/100 board requires +5V, +12V, and −12V power supplies at the currents listed in table 1-1.

2.6 COOLING REQUIREMENTS

The iSBC 432/100 board dissipates 336.5 gram-calories/minute (1.33 BTU/minute), and adequate circulation must be provided to prevent a temperature rise above 50° C (122° F). Intellec systems include fans to provide adequate intake and exhaust of ventilating air.

2.7 PHYSICAL DIMENSIONS

Physical dimensions of the iSBC 432/100 board are as follows:

a. Width: 30.48 cm (12.00 inches)

b. Height: 17.15 cm (6.75 inches)

c. Thickness: 1.52 cm (0.6 inch)

2.8 JUMPER CONFIGURATION

The iSBC 432/100 design includes a variety of jumper-selectable options that allow the user to configure the board for his/her particular application. Table 2-2 summarizes these options and lists the grid reference locations of the jumpers as shown in figure 5-1 (parts location diagram) and figure 5-2 (schematic diagram).

Table 2-2. Jumper Selectable Options

Function	Fig. 5-1 Grid Ref.	Fig. 5-2 Grid Ref.	Description
I/O Base Address	1B6	2C5	Selects the Multibus base address for on-board I/O ports. The default jumper (79-80*) configures the I/O addresses to 1X. The value of X is determined by the I/O port to be addressed (refer to table 3-1). Other base addresses are selected as follows: address jumper 7X 67-68 6X 69-70 5X 71-72 4X 73-74 3X 75-76 2X 77-78 1X 79-80*
XACK/Timing	1B8	3A6	The factory default jumper 54-55* provides the correct XACK delay to read and write on-board I/O ports. This jumper should not be modified.
8/16-bit bus access	1B4	7C2	Selects 8- or 16-bit Multibus transfer mode. The default jumper configuration (46-47*) selects the 8-bit transfer mode. In this mode, all Multibus accesses are single-byte accesses. By jumpering 45-46, the 16-bit Multibus mode is selected.
Bus Lock	1B7	2A6	Default jumper 65-66* locks the Multibus bus during each GDP data transfer. A GDP initiated data transfer may require as many as ten Multibus transfers in the 8-bit mode. To allow other masters to acquire the bus during GDP transfers, remove this jumper and connect 64-65.
Processor ID	1C8	2C4	Default jumpr 33-34* permits the GDP to read its processor ID from an on-board register at I/O address 00H. This jumper should not be removed.
Interrupt Signals	1B7	4D1	A board generated interrupt may be routed to one of the Multibus interrupt lines (INT5/, INT6/, or INT7/). Default jumper 86-87* routes the interrupt signal to INT6/. If another interrupt line is desired, remove this jumper and connect 88-89 (INT7/) or 90-91 (INT5/).

*Default jumper configured at the factory.

Table 2-2. Jumper Selectable Options (Cont'd.)

Function	Fig. 5-1 Grid Ref.	Fig. 5-2 Grid Ref.	Description
Bus Arbitration	1B7	2A4	Default jumper 81-82* routes the Bus Priority Out signal BPRO/ to the Multibus bus. (Refer to table 2-4.) This jumper should always be connected when the processor board is inserted in an Intellec system or used with a serial priority bus resolution scheme. The Common Bus Request signal (CBRQ) from the Multibus bus is not presently used.
User Selectable Inputs	1B6	4C5	Three user selectable jumpers are available for system configuration inputs. These three inputs are read through the processor status port. These inputs appear on the three most significant data lines as follows:
GDP Initialization	1C5	4D6	In normal operation (default jumper 43-44*), the GDP is initialized when a Multibus master writes an initialization pattern to the processor control I/O port and also when the Multibus INIT/ signal is activated. The GDP is held in the initialized state until the Multibus master subsequently rewrites the I/O port.
Serial I/O Port	1C4	3C2	The serial I/O port has three jumper selectable options. Jumper 31-32 provides I/O loopback for testing. This jumper should not be connected in normal operation; 27-28* provides an automatic data set ready response when the data terminal ready signal is asserted; 29-30* provides an automatic clear-to-send response when the request-to-send signal is asserted. User configuration of these jumpers is terminal dependent.

Port Data Bit	Associated Jumper	= 0	= 1
D7	40-41*	remove jumper	install jumper*
D6	38-39*	remove jumper	install jumper*
D5	36-37*	remove jumper	install jumper*

*Default jumper configured at the factory.

Study table 2-2 carefully while making reference to figures 5-1 and 5-2. If the default (factory configured) jumper configuration is appropriate for a particular function, no further action is required for that function. If, however, a different configuration is required, remove the default jumper(s) and/or install optional jumper(s) as specified. For most options, the information in table 2-2 is sufficient for proper configuration. Additional information, where necessary, is contained in the following paragraphs.

2.9 I/O ACCESS

All on-board I/O devices are accessible only from the Multibus bus. The selection of an I/O base address is performed by the user as described in table 2-2. By moving the address selection jumper, the most significant four I/O address bits are fixed as:

A7	A6	A5	A4	Hex	Jumper
0	0	0	1	1	79-80
0	0	1	0	2	77-78
0	0	1	1	3	75-76
0	1	0	0	4	73-74
0	1	0	1	5	71-72
0	1	1	0	6	69-70
0	1	1	1	7	67-68

The least significant four bits of the I/O address are determined by the individual I/O port; a list of I/O addresses and corresponding I/O ports is given in table 3-1. The processor ID register always resides at Multibus I/O address 00H and cannot be relocated. Note that all Multibus I/O addresses generated by the iSBC 432/100 board are even, i.e., the least-significant address bit is always zero. In addition, all Multibus addresses (I/O or memory) are generated using the on-board offset register, as discussed in paragraph 4-5.

2.10 MULTIBUS BUS ACCESS

The iSBC 432/100 board contains no local memory. All system memory resides on separate Multibus modules. Both system memory and all I/O ports (including I/O ports contained on the processor board) must be accessed via the Multibus bus. Each GDP access specifies either a local address or a physical address (refer to the discussion in Chapter 3). Local address requests are translated into Multibus I/O commands; physical address requests are translated into Multibus memory commands.

The iSBC 432/100 board is designed to operate with either 8-bit or 16-bit memory modules. A user-selectable jumper (table 2-2) is provided to select the 8-bit or 16-bit Multibus transfer mode. (The board is factory-configured to operate in the 8-bit mode.) GDP memory accesses may require the transfer of one to ten data bytes over the Multibus bus. In the 8-bit mode, all GDP memory requests initiate a series of single-byte read or write accesses. In the 16-bit mode, all GDP multibyte memory requests that originate on even byte boundaries are satisfied by a series of double-byte (16-bit) read or write accesses. All other accesses are performed in the same manner as are accesses in the 8-bit mode.

CAUTION

When operating with iSBC/MDS* 016 16K RAM memory modules, the 8-bit mode must be used. The 16-bit mode may be used with iSBC/MDS 032/048/064 RAM memory modules.

As mentioned earlier, a single GDP memory request may require the transfer of ten data bytes over the Multibus bus. In order to shorten the overall time required for these data transfers, the bus may be locked from the beginning of the first transfer until the GDP memory transfer has been completed. Locking the bus eliminates the time required to acquire and release the bus for each byte data transfer. This "bus lock" feature, which results in higher processor throughput, is user selectable as described in table 2-2. The processor board is shipped with the "bus lock" feature enabled.

CAUTION

The bus lock provision cannot be enabled in systems with double-density diskette controllers and 8-bit memory if the diskette controller will operate simultaneously with the iSBC 432/100 board.

*"MDS" is an ordering code only, and is not used as a product name or trademark. MDS® is a registered trademark of Mohawk Data Sciences Corp.

2.11 MULTIBUS BUS CONFIGURATION

For system applications, the iSBC 432/100 board is designed for installation in a standard Multibus backplane (e.g., an Intellec Microcomputer Development System). Multibus signal characteristics and methods of implementing a serial or parallel priority resolution scheme for resolving bus contention in a multiple bus master system are described in the following paragraphs.

CAUTION

Always turn off the system power supply before installing or removing any board from the backplane. Failure to observe this precaution can cause damage to the board.

2.12 SIGNAL CHARACTERISTICS

As shown in figure 1-1, connector P1 interfaces the iSBC 432/100 board to the Multibus bus. The pin assignments for this 86-pin connector are listed in table 2-3 and descriptions of the signal functions are provided in table 2-4.

The dc characteristics of the iSBC 432/100 bus interface are provided in table 2-5. The ac characteristics of the iSBC 432/100 board when operating in the master mode and slave mode are provided in tables 2-6 and 2-7, respectively. Bus exchange timing diagrams are provided in figures 2-1 and 2-2.

2.13 SERIAL PRIORITY RESOLUTION

In a multiple bus master system, bus contention can be resolved by implementing a serial priority resolution scheme as shown in figure 2-3. Due to the propagation delay of the BPRO/ signal path, this scheme is limited to a maximum of three bus masters capable of acquiring and controlling the Multibus bus. In the configuration shown in figure 2-3, the bus master installed in slot J2 has the highest priority and is able to acquire control of the bus at any time because its BPRN/ input is always enabled (tied to ground).

If the bus master in slot J2 desires control of the Multibus bus, it drives its BPRO/ output high and inhibits the BPRN/ input to all lower-priority bus masters. When finished using the bus, the J2 bus master pulls its BPRO/ output low and gives the J3 bus master the opportunity to take control of the bus. If the J3 bus master does not desire to control the bus at this time, it pulls its BPRO/ output low and gives the lowest priority bus master in slot J4 the opportunity to assume control of the bus.

Table 2-3. Multibus™ Connector P1 Pin Assignments

Pin*	Signal	Function	Pin*	Signal	Function
1	GND	} Ground	44	ADRF/	
2	GND		45	ADRC/	
3	+5V		46	ADRD/	
4	+5V		47	ADRA/	
5	+5V		48	ADRB/	
6	+5V	} Power input	49	ADR8/	
7	+12V		50	ADR9/	
8	+12V		51	ADR6/	} Address bus
9	−5V		52	ADR7/	
10	−5V		53	ADR4/	
11	GND	} Ground	54	ADR5/	
12	GND		55	ADR2/	
13	BCLK/	Bus Clock	56	ADR3/	
14	INIT/	System Initialize	57	ADR0/	
15	BPRN/	Bus Priority In	58	ADR1/	
16	BPRO/	Bus Priority Out	59	DATE/	
17	BUSY/	Bus Busy	60	DATF/	
18	BREQ/	Bus Request	61	DATC/	
19	MRDC/	Memory Read Command	62	DATD/	
20	MWTC/	Memory Write Command	63	DATA/	
21	IORC/	I/O Read Command	64	DATB/	
22	IOWC/	I/O Write Command	65	DAT8/	
23	XACK/	Transfer Acknowledge	66	DAT9/	} Data Bus
24	INH1/	Inhibit RAM	67	DAT6/	
25			68	DAT7/	
26			69	DAT4/	
27	BHEN/	Byte High Enable	70	DAT5/	
28	ADR10/	Address bus bit 10	71	DAT2/	
29	CBRQ/	Common Bus Request	72	DAT3/	
30	ADR11/	Address bus bit 11	73	DAT0/	
31	CCLK/	Constant Clock	74	DAT1/	
32	ADR12/	Address bus bit 12	75	GND	} Ground
33	INTA/	Interrupt Acknowledge	76	GND	
34	ADR13/	Address bus bit 13	77		
35	INT6/	Interrupt request on level 6	78		
36	INT7/	Interrupt request on level 7	79	−12V	
37	INT4/	Interrupt request on level 4	80	−12V	
38	INT5/	Interrupt request on level 5	81	+5V	
39	INT2/	Interrupt request on level 2	82	+5V	} Power input
40	INT3/	Interrupt request on level 3	83	+5V	
41	INT0/	Interrupt request on level 0	84	+5V	
42	INT1/	Interrupt request on level 1	85	GND	} Ground
43	ADRE/		86	GND	

*All odd-numbered pins (1,3,5...85) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.

Table 2-4. Multibus™ Signal Functions

Signal	Functional Description
ADR0/ADRF/ ADR10/-ADR13/	Address. These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0/ (when active low) enables the even byte bank (DAT0/-DAT7/) on the Multibus bus; i.e., ADR0/ is active low for all even addresses. ADR13/ is the most significant address bit.
BCLK/	Bus Clock. Used to synchronize the bus contention logic on all bus masters. BCLK/ is approximately 10 MHz with a worst case 35/65 percent duty cycle.
BHEN/	Byte High Enable. When active low, enables the odd byte bank (DAT8/-DATF/) onto the Multibus bus.
BPRN/	Bus Priority In. Indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPR0/	Bus Priority Out. In serial (daisy chain) priority resolution schemes, BPR0/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	Bus Request. In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	Bus Busy. Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	Common Bus Request. Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
CCLK/	Constant Clock. Provides a clock signal of constant frequency for use by other system modules. CCLK/ is approximately 10 MHz with a worst case 35/65 percent duty cycle.
DAT0/-DATF/	Data. These 16 bidirectional data lines transmit data to, and receive data from, the addressed memory location or I/O port. DATF/ is the most-significant bit. For data byte operations, DAT0/-DAT7/ is the even byte and DAT8/-DATF/ is the odd byte.
INH1/	Inhibit RAM. For system applications, allows RAM addresses to be overlaid by ROM/PROM or memory mapped I/O devices.
INIT/	Initialize. Resets the entire system to known internal state.
INTA/	Interrupt Acknowledge. This signal is issued in response to an interrupt request.
INT0/-INT7/	Interrupt Request. These eight lines transmit Interrupt Requests to the appropriate interrupt handler. INT0 has the highest priority.
IORC/	I/O Read Command. Indicates that the address of an I/O port is on the Multibus address lines, and that the output of that port is to be read (placed) onto the Multibus data lines.
IOWC/	I/O Write Command. Indicates that the address of an I/O port is on the Multibus address lines, and that the contents on the Multibus data lines are to be accepted by the addressed port.
MRDC/	Memory Read Command. Indicates that the address of a memory location is on the Multibus address lines, and that the contents of that location are to be read (placed) on the Multibus data lines.
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the Multibus address lines, and that the contents on the Multibus data lines are to be written into that location.
XACK/	Transfer Acknowledge. Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto, or accepted from, the Multibus data lines.

Table 2-5. iSBC 432/100™ DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
XACK/	V_{OL}	Output Low Voltage	$I_{OL} = 16$ mA		0.4	V
	V_{OH}	Output High Voltage	$I_{OH} = -2.6$ mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.4$V		-0.4	mA
	I_{IH}	Input Current at High V	$V_{IN} = 2.7$V		20	μA
ADR0/-ADRF/ ADR10/-ADR13/ BHEN/	V_{OL}	Output Low Voltage	$I_{OL} = 32$ mA		0.45	V
	V_{OH}	Output High Voltage	$I_{OH} = -5$ mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.45$V		-2.2	mA
	I_{IH}	Input Current at High V	$V_{IN} = 2.7$V		100	μA
	I_{LH}	Output Leakage High	$V_O = 5.25$V		50	μA
	I_{LL}	Output Leakage Low	$V_O = 0.45$V		-50	μA
BCLK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.45$V		-0.5	mA
	I_{IH}	Input Current at High V	$V_{IN} = 5.5$V		60	μA
CCLK	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.4$V		-0.4	mA
	I_{IH}	Input Current at High V	$V_{IN} = 2.7$V		20	μA
BPRN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.45$V		-0.5	mA
	I_{IH}	Input Current at High V	$V_{IN} = 5.5$V		60	μA
BPR0/,BREQ/	V_{OL}	Output Low Voltage	$I_{OL} = 10$ mA		0.45	V
	V_{OH}	Output High Voltage	$I_{OH} = -0.4$ mA	2.4		V
BUSY/,CBRQ/, (OPEN COLLECTOR)	V_{OL}	Output Low Voltage	$I_{OL} = 20$ mA		0.45	V
DAT0/-DATF/	V_{OL}	Output Low Voltage	$I_{OL} = 32$ mA		0.45	V
	V_{OH}	Output High Voltage	$I_{OH} = -5$ mA	2.4		V
	V_{IL}	Input Low Voltage			0.90	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.45$V		-0.80	mA
	I_{IH}	Output Leakage High	$V_O = 5.25$V		200	μA
INIT/ (SYSTEM RESET)	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = 0.4$V		-0.9	mA
	I_{IH}	Input Current at High V	$V_{IN} = 2.4$V		80	μA
INT5/-INT7/	V_{OL}	Output Low Voltage	$I_{OL} = 16$ mA		0.4	V
IORC/,IOWC/	V_{OL}	Output Low Voltage	$I_{OL} = 32$ mA		0.5	V
	V_{OH}	Output High Voltage	$I_{OH} = -5$ mA	2.4		V
	I_{LH}	Output Leakage High	$V_O = 5.25$V		100	μA
	I_{LL}	Output Leakage Low	$V_O = 0.4$V		-100	μA
	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	$V_{IN} = .4$V		-.4	mA
	I_{IH}	Input Current at High V	$V_{IN} = 2.7$V		20	μA
MRDC/,MWTC/	V_{OL}	Output Low Voltage	$I_{OL} = 32$ mA		0.5	V
	V_{OH}	Output High Voltage	$I_{OH} = -5$ mA	2.4		V
	I_{LH}	Output Leakage High	$V_O = 5.25$V		100	μA
	I_{LL}	Output Leakage Low	$V_O = .4$V		-100	μA

Table 2-6. iSBC 432/100™ AC Characteristics (Master Mode)

Parameter	Minimum (ns)	Maximum (ns)	Description	Remarks
t_{AS}	50		Address setup time to command	
t_{AH}	50		Address hold time from command	
t_{DS}		50	Data setup to write CMD	
t_{DHW}	50		Data hold time from write CMD	
t_{CY}	198	202	CPU cycle time	
t_{CMDR}	594		Read command width	
t_{CMDW}	594		Write command width	
t_{CSWR}	396		Read-to-write command separation	In override mode
t_{CSRR}	396		Read-to-read command separation	In override mode
t_{CSWW}	594		Write-to-write command separation	In override mode
t_{CSRW}	594		Write-to-read command separation	In override mode
t_{SAM}	198	202	Time between XACK samples	
t_{DHR}	0		Read data hold time	
t_{DXL}	−400		Read data setup to XACK	
t_{XAH}	0		XACK hold time	
t_{BS}	23		BPRN to BCLK setup time	
t_{DBY}		55	BCLK to BUSY delay	
t_{NOD}		30	BPRN to BPRO delay	
t_{DBO}	40		BCLK/ to bus priority out	
t_{BCY}	100		Bus clock period (BCLK)	
t_{BW}	$.35t_{BCY}$	$.65t_{BCY}$	Bus clock low or high interval	Supplied by system
t_{INIT}	3000		Initialization width	After all voltages have stabilized

Table 2-7. iSBC 432/100™ I/O Access AC Characteristics

Parameter	Minimum (ns)	Maximum (ns)	Description	Remarks
t_{AS}	50		Address setup to command	From address to command
t_{DS}	−100		Write data setup to command	
t_{ACK}		$4t_{BCY}$	Command to XACK	
t_{CMD}	400		Command width	
t_{AH}	50		Address hold time	
t_{DHW}	50		Write data hold time	
t_{DHR}	25	125	Read data hold time	
t_{XAH}		50	Acknowledge hold time	Acknowledge turn-off delay
t_{ACC}		300	Read to data valid	
t_{DXL}	100		Read data setup to XACK	

Figure 2-1. Bus Exchange Timing (Master Mode)
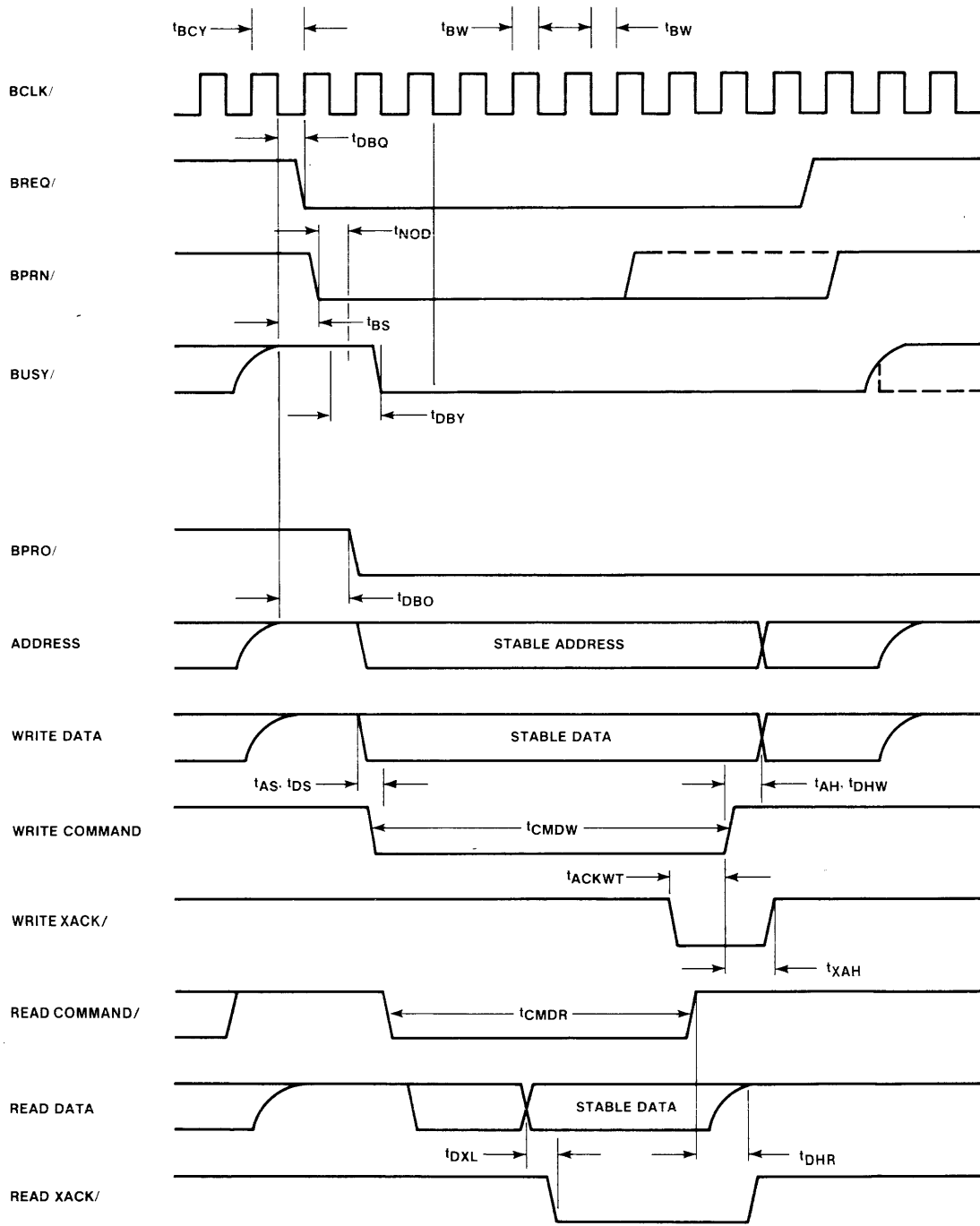
*CBRQ/ timing not shown relative to other bus signals other than BCLK/.
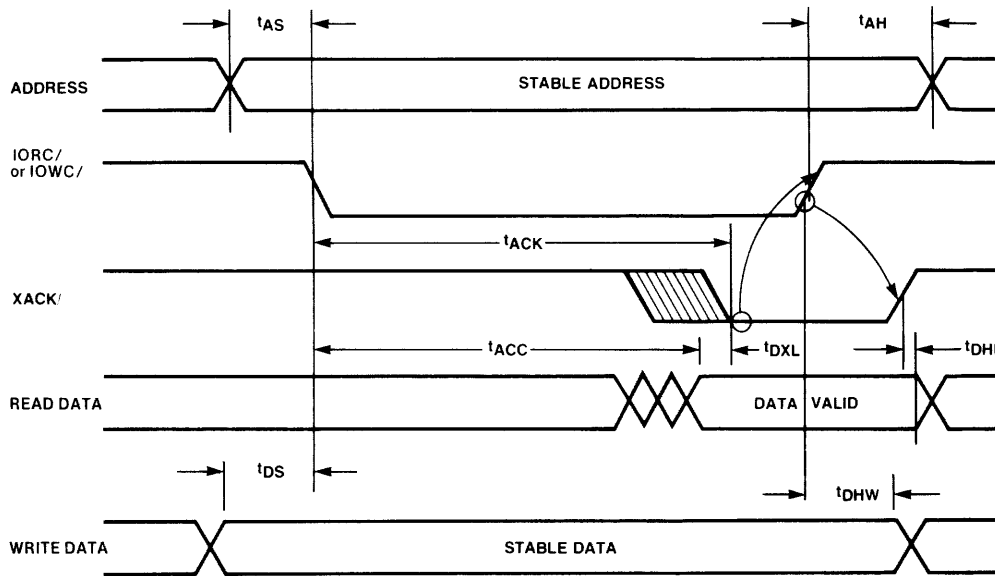
171820-2

Figure 2-2. I/O Access Timing (Read/Write)   171820-3
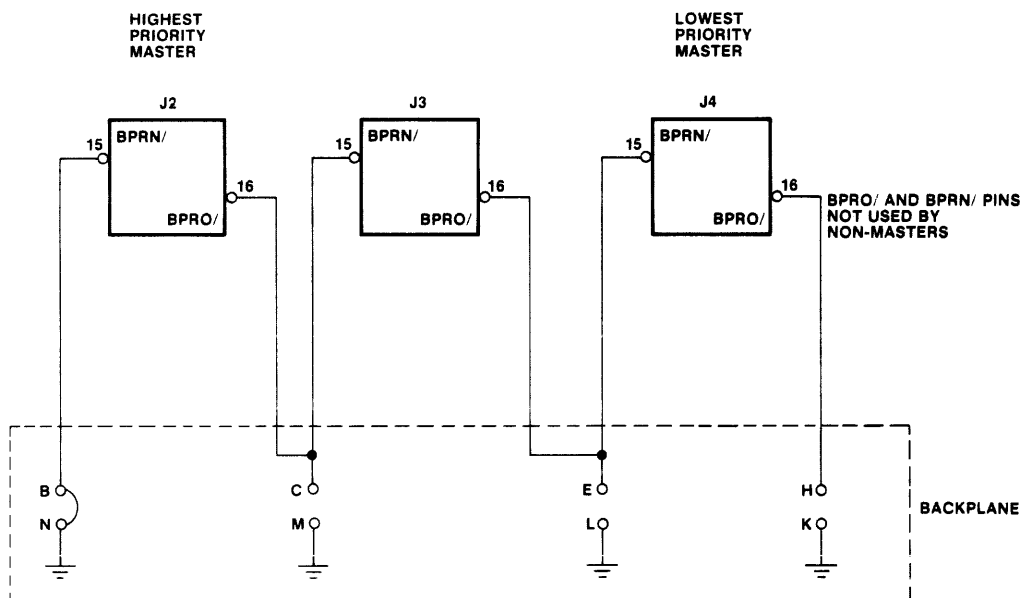
Figur 2-3. Serial Priority Resolution Scheme   171820-4
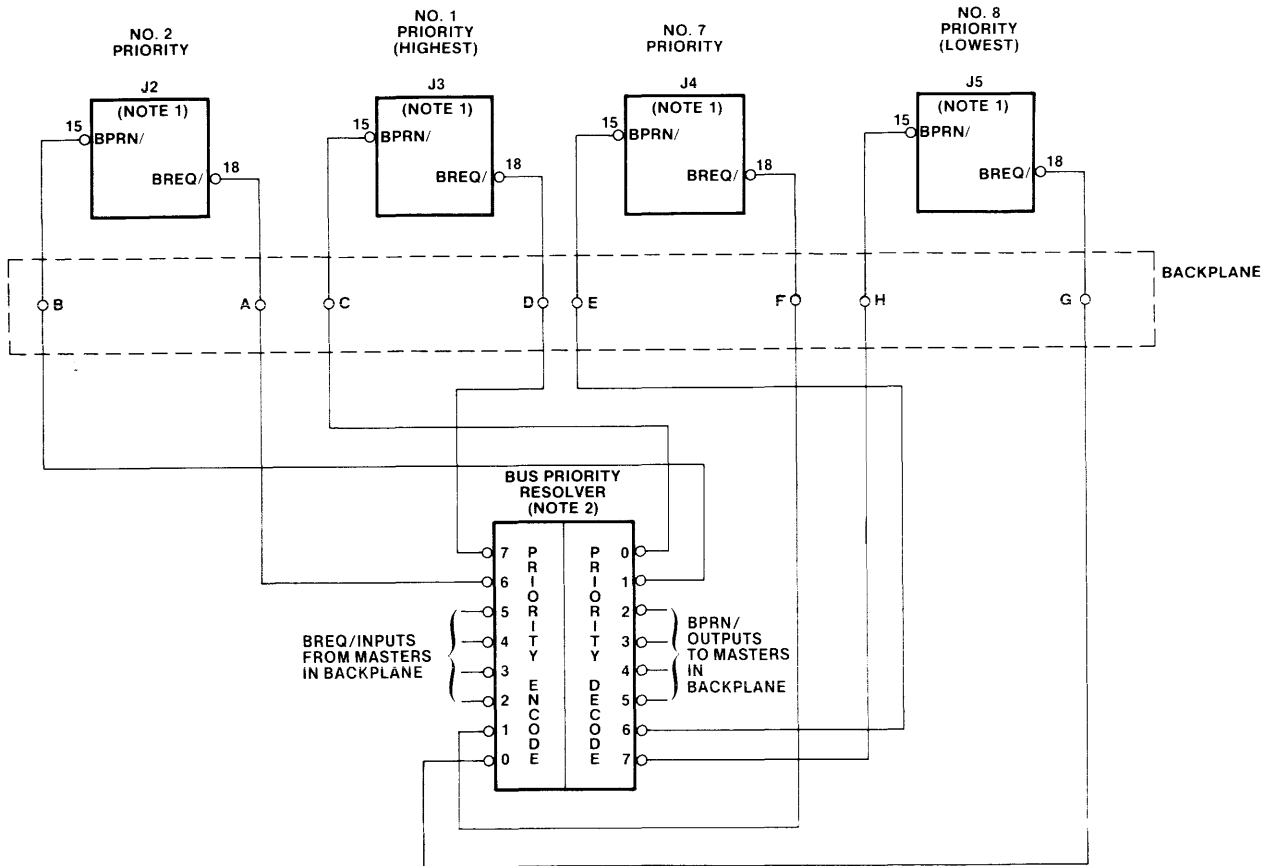
NOTE: REFER TO TEXT REGARDING THE
       DISABLING OF BPRO/ OUTPUT.

Figure 2-4. Parallel Priority Resolution Scheme   171820-5

2.14 PARALLEL PRIORITY RESOLUTION

A parallel priority resolution scheme allows up to 16 bus masters to acquire and control the Multibus bus. Figure 2-4 illustrates one method of implementing such a scheme for resolving bus contention in a system containing eight bus masters. Notice that the two highest and two lowest priority bus masters are shown installed in the system backplane.

In the scheme shown in figure 2-4, the priority encoder is a 74148 and the priority decoder is an Intel 8205. Input connections to the priority encoder determine the bus priority, with input 7 having the highest priority and input 0 having the lowest priority (the J5 bus master has the lowest priority).

IMPORTANT: In a parallel priority resolution scheme, the BPRO/ output must be disabled on all bus masters. On the iSBC 432/100 board, the BPRO/ output signal may be disabled by removing jumper 40-41.

2.15 SERIAL I/O CABLING

Pin assignments and signal definitions for the RS-232-C serial I/O interface are listed in table 2-8. An Intel iSBC 955 cable set may be used for interfacing. The serial cable assembly consists of a 25-conductor flat cable with a 26-pin printed circuit board edge connector at one end and a 25-pin RS-232-C interface connector at the other end.

Table 2-8. Serial I/O Connector J1 Pin Assignments

Pin[1]	Signal	Description
2	PROTECTIVE GND	Protective Chassis Ground
4	RXD	8251A receiver data input (RXD)
6	TXD	8251A transmitter data output (TXD)
8	CTS[2]	8251A Clear-to-send input (CTS)
10	RTS[2]	8251A Request-to-send output (RTS)
12	DTR[3]	8251A Data Terminal Ready output (DTR)
13	DSR[3]	8251A Data Set Ready input (DSR)
14	SIG GND	Signal Ground

NOTES:

1. All odd-numbered pins (1, 3, 5,..., 25) are on the component side of the board. Pin 1 is the right-most pin when viewed from the component side of the board with the extractors at the top.

2. For applications without CTS capability, connect jumper 5-6. This routes 8251A RTS output to 8251A CTS input.

3. For applications without DSR capability, connect jumper 3-4. This routes 8251A DTR output to 8251A DSR input.

For applications where cables may be made by the user for the iSBC 432/100 board, it is important to note that the mating connector for J1 has 26 pins whereas the RS-232-C connector has 25 pins. Consequently, when connecting the 26-pin mating connector to 25-conductor flat cable, be sure that the cable makes contact with pins 1 and 2 of the mating connector and not with pin 26. Table 2-9 provides pin correspondence between the board edge connector (J1) and an RS-232-C connector. When attaching the cable to J1, be sure that the PC connector is oriented properly with respect to pin 1 on the edge connector. (Refer to the footnote in table 2-8.)

2.16 BOARD INSTALLATION

{CAUTION}

Always turn off the computer system power supply before installing or removing the iSBC 432/100 board and before installing or removing device interface cables. Failure to take these precautions can result in damage to the board.

In an Intellec system, install the iSBC 432/100 board in any odd-numbered slot except slot 1 and attach the appropriate serial I/O cable assembly to the edge connector J1.

Table 2-9. Connector J1 Vs RS-232-C
Pin Correspondence

PC Conn. J1	RS232C Conn.	PC Conn. J1	RS232C Conn.
1	14	14	7
2	1	15	21
3	15	16	8
4	2	17	22
5	16	18	9
6	3	19	23
7	17	20	10
8	4	21	24
9	18	22	11
10	5	23	25
11	19	24	12
12	6	25	N/C
13	20	26	13

3.1 INTRODUCTION

This chapter lists I/O address assignments, describes the effects of hardware initialization, and provides programming information for the Intel 8251A USART (Universal Synchronous/Asynchronous Receiver/Transmitter), the Intel 8253 PIT (Programmable Interval Timer), and the on-board control and status registers.

A complete description of the Intel iAPX 432 General Data Processor (GDP)—its instruction set, programming, and protection mechanisms—may be found in the *iAPX 432 General Data Processor Architecture Reference Manual*, Order No. 171860-001.

3.2 MEMORY ADDRESSING AND ACCESS

The iSBC 432/100 Processor Board contains no local memory; all GDP memory accesses are processed over the Multibus architecture. GDP physical address references are translated into Multibus memory read/write commands. Physical addresses generated by the GDP are modified by an on-board offset register to permit an Intellec or iSBC system processor to share Multibus memory with the iSBC 432/100 processor.

When the GDP addresses memory (via the Multibus bus) each GDP access request is implemented as one or more 8/16-bit Multibus data transfers. Memory access mechanisms are described in detail beginning in paragraph 4-4. Briefly, to perform Multibus data transfers, the iSBC 432/100 board must first gain control of the bus. After addressing the correct memory location and issuing a Memory Read or Memory Write command, the processor board waits until a Transfer Acknowledge (XACK/) is received from the addressed memory module. When the data transfer is completed, the iSBC 432/100 board releases the bus to permit other masters to use it. When a GDP access request specifies a multibyte data transfer that must be translated into more than one Multibus transfer, a "bus lock" feature permits the processor board to retain Multibus control for the complete sequence of Multibus transfers. This feature eliminates the time required to release and regain bus control between data transfers, thereby increasing throughput and lowering Multibus bandwidth requirements.

3.3 I/O ADDRESSING AND ACCESS

GDP local address references are translated into Multibus I/O read/write commands. All I/O port accesses (including accesses to on-board devices) occur via the Multibus bus. I/O ports physically located on the iSBC 432/100 Processor Board are logically situated on the bus. Any bus master may access the board's I/O ports (listed in table 3-1). I/O address generation is performed in the same manner as memory address generation (described in paragraph 4-5).

3.4 INITIALIZATION

The Multibus initialization signal line (INIT/), when activated, resets the GDP and causes the 8251A USART to enter an "idle" state waiting for a set of Command Words to program the desired function. The 8253 PIT is not affected by the INIT/ signal.

In addition to the INIT/ reset sequence, another Multibus master may reset the GDP by writing the processor reset flag (contained within the processor control register—refer to table 3-1).

3.5 8251A USART PROGRAMMING

The USART converts parallel output data into a serial output data format (e.g., IBM Bi-Sync) for half- or full-duplex operation. The USART also converts serial input data into parallel data format.

Prior to the start of data transmission or data reception, the USART must be loaded with a set of control words. These control words, which define the complete functional operation of the USART, must immediately follow a reset (internal or external). The control words are either Mode instructions or Command instructions.

3.6 MODE INSTRUCTION FORMAT

The Mode instruction word defines the general characteristics of the USART and must follow a reset operation. Once the Mode instruction word has been

Table 3-1. iSBC 432/100™ I/O Address Assignments

I/O Address	R/W	Description
00	R	Processor ID Register

X0	R/W	8253 PIT
		Process Clock Timer
		  Read: Counter 0
		  Write: Counter 0 (load count)

X2	R/W	Process Clock Timer
		  Read: Counter 1
		  Write: Counter 1 (load count)

X4	R/W	Baud Rate Generator
		  Read: Counter 2
		  Write: Counter 2 (load count)

X6	R/W	Read: None Write: Control

X8	R/W	8251A USART
		  Read: Data (J1)
		  Write: Data (J1)

XA	R/W	Read: Status Write: Mode or Command
XC	W	Memory Address Offset Register (contains an 8-bit memory offset for all memory addressing operations)
XE	R	Processor Status Register bit # description 0 processor initialization hold 1 interrupt pending 2 GDP accesses stopped 3 stop command active 4 fatal error 5-7 user selectable jumpers
XE	W	Processor Control bit # description 0 release processor from initialized state 1 issue Multibus interrupt 2 issue interprocessor communication request 3 stop GDP accesses 4 issue alarm signal

Note: X is jumper selectable (1-7) as described in table 2-2.

written into the USART, sync characters or command instructions may be inserted. The Mode instruction word defines the following:

a. For Synchronous Mode:

(1) Character length

(2) Parity enable

(3) Even/odd parity generation and check

(4) External sync detect (not supported by the iSBC 432/100 board)

(5) Single- or double-character sync

b. For Asynchronous Mode:

(1) Baud rate factor (X1, X16, or X64)

(2) Character length

(3) Parity enable

(4) Even/odd parity generation and check

(5) Number of stop bits

Instruction word and data transmission formats for synchronous and asynchronous modes are shown in figures 3-1 through 3-4.
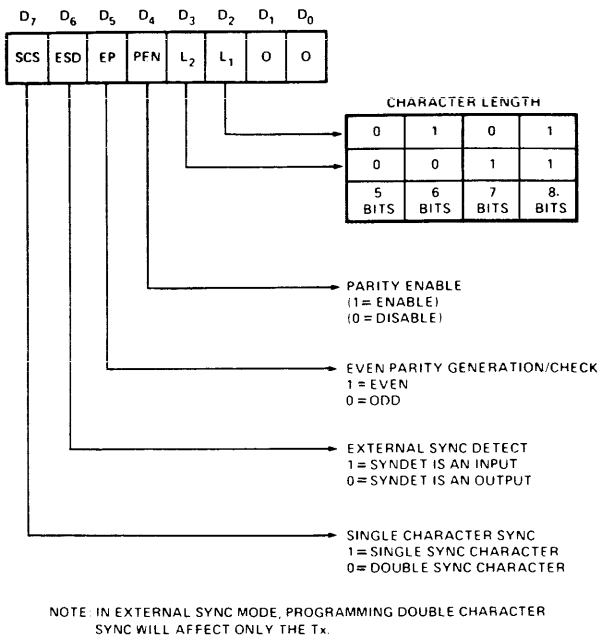
Figure 3-1. USART Synchronous Mode Instruction Word Format 171820-6
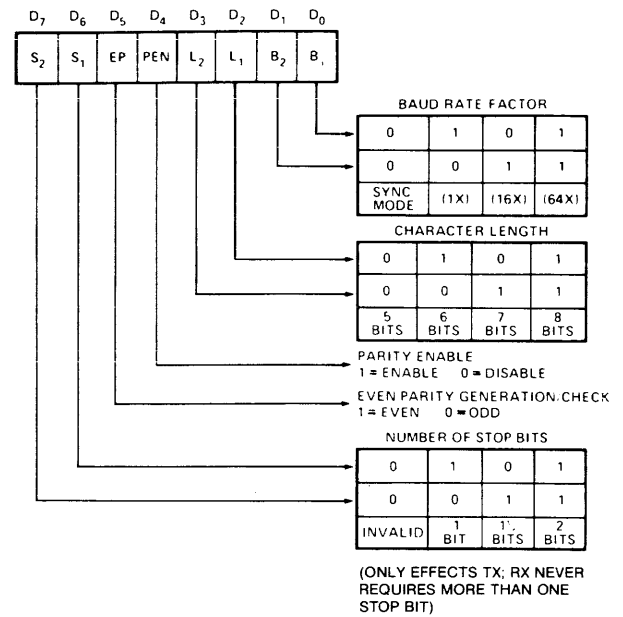
Figure 3-3. USART Asynchronous Mode Instruction Word Format 171820-8
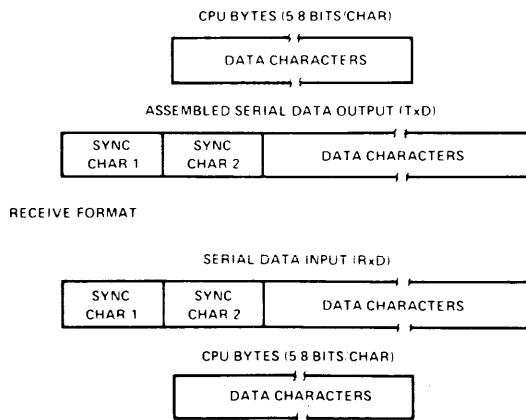
Figure 3-2. USART Synchronous Mode Transmission Format 171820-7
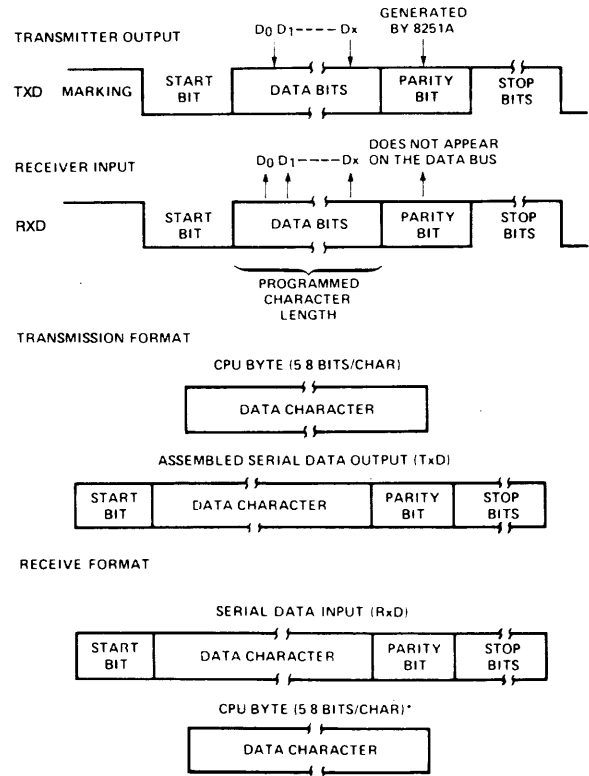
Figure 3-4. USART Asynchronous Mode Transmission Format 171820-9

3.7 SYNC CHARACTERS

Sync characters are written to the USART in the synchronous mode only. The USART can be programmed for either one or two sync characters; the format of the sync characters is at the option of the programmer.

3.8 COMMAND INSTRUCTION FORMAT

The Command instruction word shown in figure 3-5 controls the operation of the addressed USART. A Command instruction must follow the mode and/or sync words. Once the Command instruction has been written, data can be transmitted or received by the USART.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
EH	IR	RTS	ER	SBRK	RXE	DTR	TXEN

TRANSMIT ENABLE
1 = enable
0 = disable

DATA TERMINAL READY
"high" will force DTR output to zero

RECEIVE ENABLE
1 enable
0 disable

SEND BREAK CHARACTER
1 = forces TXD "low"
0 = normal operation

ERROR RESET
1 = reset error flags PE, OE, FE

REQUEST TO SEND
"high" will force RTS output to zero

INTERNAL RESET
"high" returns 8251A to Mode Instruction Format

ENTER HUNT MODE*
1 = enable search for Sync Characters

* (HAS NO EFFECT IN ASYNC MODE)

Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 3-5. USART Command Instruction Word Format 171820-10

It is not necessary for a Command instruction to precede all data transactions; only those transmissions that require a change in the Command instruction. An example is a change in the transmit enable or receive enable flag. Command instructions can be written to the USART at any time after one or more data operations.

After initialization, always read the chip status and check for the TXRDY bit prior to writing either data or command words to the USART. This ensures that any prior input is not overwritten and lost. Note that issuing a Command instruction with bit 6 (IR) set will return the USART to the Mode instruction format.

3.9 RESET

To change the Mode instruction word, the USART must receive a Reset command. The next word written to the USART after a Reset command is assumed to be a Mode instruction. Similarly, for sync mode, the next word after a mode instruction is assumed to be the first of one or more sync characters. All control words written into the USART after the Mode instruction (and/or the last sync character) are assumed to be Command instructions.

3.10 ADDRESSING

The USART chip uses address X8 to read and write I/O data; address XA is used to write mode and command words and read the USART status. (Refer to table 3-1.)

3.11 INITIALIZATION

A typical USART initialization and I/O data sequence is presented in figure 3-6. The USART chip is initialized in four steps:

a. Reset the USART to the Mode instruction format.

b. Write the Mode instruction word. One function of the mode word is to specify synchronous or asynchronous operation.

c. If synchronous mode is selected, write one or two sync characters as required.

d. Write the Command instruction word.

First, reset the USART chip by writing a Command instruction to location XA. The Command instruction must have bit 6 set (IR = 1); all other bits are immaterial.

ADDRESS	RESET
000A	MODE INSTRUCTION
000A	SYNC CHARACTER 1
000A	SYNC CHARACTER 2
000A	COMMAND INSTRUCTION
0008	DATA I/O
000A	COMMAND INSTRUCTION
0008	I/O DATA
000A	COMMAND INSTRUCTION

SYNC MODE ONLY*
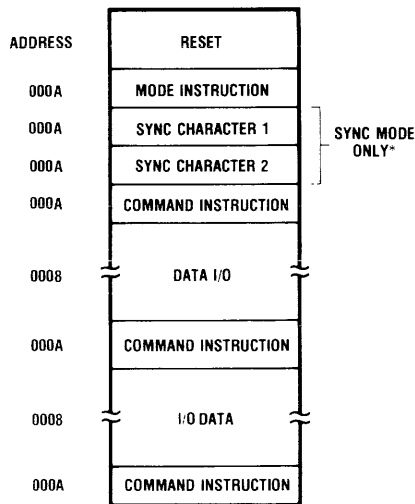
*The second sync character is skipped if Mode instruction has programmed USART to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed USART to async mode.

Figure 3-6. Typical USART Initialization and Data I/O Sequence   171820-11

NOTE

This reset procedure should be used only if the USART has been completely initialized, or the initialization procedure has reached the point that the USART is ready to receive a Command word. For example, if the reset command is written when the initialization sequence calls for a sync character, then subsequent programming will be in error.

Next write a Mode instruction word to the USART. (See figures 3-1 through 3-4.) If the USART is programmed for the synchronous mode, write one or two sync characters depending on the transmission format.

Finally, write a Command instruction word to the USART. Refer to figure 3-5.

IMPORTANT: During initialization, the 8251A USART requires a minimum recovery time of 2.4 microseconds (6 clock cycles) between back-to-back writes in order to set up its internal registers. This precaution applies only to the USART initialization and does not apply at any other time.

3.12 OPERATION

Normal operating procedures use data read and write, status read, and Command instruction write operations. Programming and addressing procedures for the above are summarized in the following paragraphs.

NOTE

After the USART has been initialized, always check the status of the TXRDY bit prior to writing data or writing a new command word to the USART. The TXRDY bit must be true to prevent overwriting and subsequent loss of command or data words. The TXRDY bit is inactive until initialization has been completed; do not check TXRDY until after the command word, which concludes the initialization procedure, has been written.

Prior to any operation change, a new command word must be written with command bits changed as appropriate. (Refer to figure 3-5.)

3.13 DATA INPUT/OUTPUT

For data receive or transmit operations, perform a GDP local read or write, respectively, to the USART. During normal transmit operation, the USART sets the Transmit Ready (TXRDY) flag. This flag indicates that the USART is ready to accept a data character for transmission. TXRDY is automatically reset when a character is loaded into the USART. Similarly, during normal receive operation, the USART sets the Receive Ready (RXRDY) flag. This flag indicates that a character has been received and is ready for input to the processor. RXRDY is automatically reset when a character is read from the USART. TXRDY and RXRDY are available in the status word. (Refer to paragraph 3-14.)

3.14 STATUS READ

Any Multibus master can determine the status of the serial I/O port by issuing an I/O Read Command to the upper address (XA) of the USART chip. The format of the status word is shown in figure 3-7.

3.15 8253 PIT PROGRAMMING

A 14.7456 MHz crystal oscillator supplies the master time base for GDP process timing and serial I/O. This basic frequency is divided by twelve to provide the 1.2288 MHz input clock for counter 0 and counter 2. The output of counter 0 is routed to the

clock input for counter 1. This cascaded arrangement permits the generation of time intervals from 3.25 microseconds to over 58 minutes. The output of counter 2 is used to supply the 8251A transmit (TXC) and receive (RXC) clocks.

3.16 MODE CONTROL WORD AND COUNT

All three counters must be initialized prior to their use. The initialization for each counter consists of two steps:

a. A mode control word (figure 3-8) is written to the control register for each individual counter.

b. A down-count number is loaded into each counter; the down-count number consists of one or two 8-bit bytes as determined by mode control word.

The mode control word (figure 3-8) does the following:

a. Selects the counter to be loaded.

b. Selects the counter operating mode.

c. Selects one of the following four counter read/load functions:

   (1) Counter latch (for stable read operation).

   (2) Read or load most-significant byte only.

   (3) Read or load least-significant byte only.

   (4) Read or load least-significant byte first, then most-significant byte.

d. Sets the counter for either binary or BCD count.

The mode control word and the count register bytes for any given counter must be entered in the following sequence:

a. Mode control word.

b. Least-significant count register byte.

c. Most-significant count register byte.
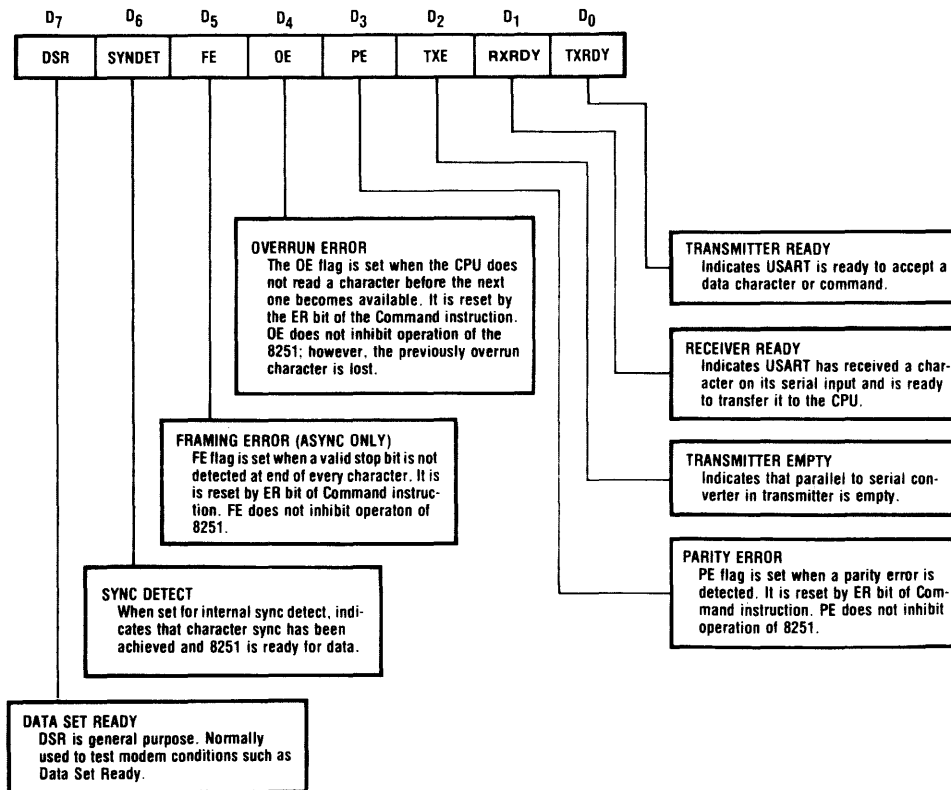
Figure 3-7. USART Status Read Format   171820-12

As long as the above procedure is followed for each counter, the chip can be programmed in any convenient sequence. For example, mode control words can be loaded first into each of three counters, followed by the least-significant byte, etc. Figure 3-9 shows two possible programming sequences.

Since all counters in the PIT chip are downcounters, the value loaded in the count registers is decremented. Loading all zeroes into a count register results in a maximum count of 2^{16} for binary numbers or 10^4 for BCD numbers. When a selected count register is to be loaded, it must be loaded with the number of bytes programmed in the mode control word. One or two bytes can be loaded,

depending on the appropriate down-count. These two bytes can be programmed at any time following the mode control word, as long as the correct number of bytes is loaded in order.

The count mode selected in the control word controls the counter output. As shown in figure 3-8, the PIT chip can operate in any of six modes:

a. mode 0—Interrupt on terminal count

b. mode 1—Programmable one-shot

c. mode 2—Rate generator

d. mode 3—Square wave generator

e. mode 4—Software-triggered strobe

f. mode 5—Hardware-triggered strobe

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

(BINARY/BCD)

0	Binary Counter (16-bits)
1	Binary Coded Decimal (BCD) Counter (4 Decades)

M2	M1	M0	(MODE)
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

← Use Mode 3 for Baud Rate Generator

RL1	RL0	(READ/LOAD)
0	0	Counter Latching operation (refer to paragraph 3-19).
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

SC1	SC0	(SELECT COUNTER)
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

Figure 3-8. PIT Mode Control Word Format   171820-13

3-7

PROGRAMMING FORMAT

Step

1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step

1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

Figure 3-9. PIT Programming Sequence Examples   171820-14

Mode 3, the primary operating mode for Counter 2, is used to generate Baud rate clock signals. In this mode, the counter output remains high until one-half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for $(N + 1)/2$ counts, and low for $(N - 1)/2$ counts.

Counter 0 and counter 1 normally operate in mode 2. In this mode, the output of each counter will be low for one period of the clock input. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the new value. When mode 2 is set, the output of the counter will remain high until after the count register is loaded.

3.17 ADDRESSING

As listed in table 3-1, the PIT uses four I/O addresses. Addresses X0, X2, and X4, respectively, are used in loading and reading the count in Counters 0, 1, and 2. Address X6 is used in writing the mode control word to the desired counter.

3.18 INITIALIZATION

To intialize the PIT chip, perform the following:

a. Write mode control word for Counter 0 to address X6. Note that all mode control words are written to X6, since the mode control word specifies which counter is being programmed. (Refer to figure 3-8.)

b. Assuming the mode control word has selected a 2-byte load, load the least-significant byte of count into Counter 0 at address X0.

c. Load the most-significant byte of count into Counter 0 at address X0.

NOTE

Be sure to enter the down-count in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly, enter the down count value in BCD if the counter was so programmed.

d. Repeat steps b, c, and d for Counters 1 and 2.

3.19 OPERATION

The following paragraphs describe operating procedures for counter reading, and for clock frequency/divide ratio selection.

3.20 COUNTER READ

Since the gates of all counters are constantly enabled, the 8253 counters can only be read "on the fly." The recommended procedure is to use a mode control word to latch the contents of the count register; this ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

If a counter is read during the down-count, it is mandatory to complete the read procedure; that is, if two bytes were programmed to the counter, then two bytes must be read before any other operations are performed with that counter.

To read the count of a particular counter, proceed as follows:

a. Write counter register latch control word (figure 3-10) to address X6. This control word specifies the desired counter and selects the counter latching operation.

b. Perform a read operation of the desired counter; refer to table 3-1 for counter addresses.

NOTE

Be sure to read one or two bytes, as specified in the initialization mode control word. For two bytes, read in the order specified.
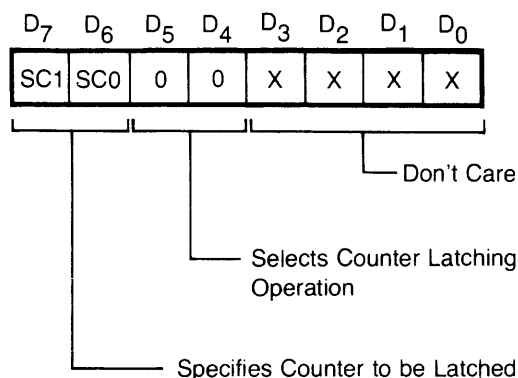
Figure 3-10. PIT Counter Register
Latch Control Word Format 171820-15

3.21 CLOCK FREQUENCY/DIVIDE RATIO SELECTION

To operate the 8251A serial I/O port, counter 2 must be loaded with a down-count value (N). When count value N is loaded into a counter, it becomes the clock divisor. To derive N for either synchronous or asynchronous RS-232-C operation, use the procedures described in following paragraphs.

3.22 SYNCHRONOUS MODE

In the synchronous mode, the TXC and/or RXC rates equal the Baud rate. Therefore, the count value is determined by:

$$N = CB$$

where N is the count value,
    B is the desired Baud rate, and
    C is 1.2288 MHz, the input clock frequency.

Thus, for a 4800 Baud rate, the required count value (N) is:

$$N = \frac{1.2288 \times 10^6}{4800} = \underline{256}.$$

If the binary equivalent of count value N = 256 is loaded into Counter 2, then the output frequency is 4800 Hz, which is the desired clock rate for synchronous mode operation.

3.23 ASYNCHRONOUS MODE

In the asynchronous mode, the TXC and/or RXC rates equal the Baud rate times one of the following multipliers: X1, X16, or X64. Therefore, the count value is determined by:

$$N = C/BM$$

where N is the count value,
    B is the desired Baud rate,
    M is the Baud rate multiplier (1, 16, or 64), and
    C is 1.2288 MHz, the input clock frequency.

Thus, for a 4800 Baud rate, the required count value (N) is:

$$N = \frac{1.23 \times 10^6}{4800 \times 16} = \underline{16}.$$

If the binary equivalent of count value N = 16 is loaded into Counter 2, then the output frequency is 4800 X 16 Hz, which is the desired clock rate for

asynchronous mode operation. Count values (N) versus rate multiplier (M) for each Baud rate are listed in table 3-2.

NOTE

During initialization, be sure to load the count value (N) into counter 2 and the Baud rate multiplier (M) into the 8251A USART.

Table 3-2. PIT Count Value vs. Rate Multiplier for Each Baud Rate

Baud Rate: (B)	M = 1	Count Value (N)* For	
		M = 16	M = 64
75	16384	1024	256
110	11171	698	175
150	8192	512	128
300	4096	256	64
600	2048	128	32
1200	1024	64	16
2400	512	32	8
4800	256	16	4
9600	128	8	2
19200	64	4	
38400	32		

*Count Values (N) assume clock is 1.2288 MHz. Count Values (N) and Rate Multipliers (M) are in decimal.

3.24 iSBC 432/100 CONTROL AND STATUS REGISTERS

In addition to the previously described I/O devices, the processor board also contains a write-only control register and a read-only status register as listed in table 3-1. The status register contains iSBC 432/100 operational information as follows when each bit is set:

Bit Number	Description
0	Processor Initialization Hold. The GDP is held in the initialized state. When this bit is reset, the GDP is executing instructions.
1	Interrupt Pending. A GDP interrupt request has been issued.
2	Processor Access Stopped. The iSBC 432/100 board has stopped Multibus accesses. The GDP may continue executing until the next Multibus access is attempted.
3	Stop Request. An access stop request has been issued. When the iSBC 432/100 board acknowledges this request, the Processor Access Stopped flag (bit 2 above) is set.

Bit Number	Description
4	Fatal Error. The GDP has entered a state from which it cannot continue executing. For example, a fatal error can be caused by the corruption of system data structures.
5-7	User Selectable Jumpers. Three flags that may be individually selected by the user.

IMPORTANT: The Fatal Error signal is connected to a red LED in the upper left corner of the processor board. When this LED is lit, a fatal error has occurred and the GDP has suspended execution. The iSBC 432/100 processor must be re-initialized to continue execution.

The processor control register contains five software controlled command flags that control processor initialization and interprocessor communication as follows:

Bit Number	Description
0	Initialize Processor. When reset, this command flag holds the GDP in the initialized state. When the flag is subsequently set, the GDP begins execution.
1	Issue Multibus Interrupt. When set, this flag sets the Interrupt Pending flag in the status register and generates an interrupt request on the appropriate Multibus level (see table 2-2).
2	Issue Interprocessor Communication Request. Reserved for future implementation. This flag should always be reset.
3	Stop Multibus Access Request. Setting this flag causes the iSBC 432/100 board to stop Multibus accesses. After stopping Multibus activity, the Processor Access Stopped flag (bit 2 in the status register) is set. When this flag is reset, the processor board continues with the next access. The GDP may continue executing while Multibus accesses are stopped.
4	Issue Alarm Signal. Activation of this signal causes a GDP ALARM condition. This command flag is automatically reset (by the iSBC 432/100 hardware) after the ALARM condition is initiated.

NOTE

When interfacing the iSBC 432/100 Processor Board to another system processor (e.g., in an Intellec Microcomputer Development System), the processor interrupt capabilities should be fully utilized for synchronization and communication. These interrupt capabilities greatly enhance system throughput by eliminating Multibus polling accesses and processor "busy wait" operations.

4.1 INTRODUCTION

The iSBC 432/100 Processor Board is designed to incorporate the advanced processing features of the iAPX 432 microprocessor into Multibus compatible systems. The 43201 Instruction Decode Unit and the 43202 Instruction Execution Unit comprise the iAPX 432 General Data Processor (GDP). These LSI devices form the heart of the iSBC 432/100 board. The GDP operates with a two-phase overlapped clock that is generated on-board.

The GDP address space is divided into two components: a local address space and a physical address space. On-board logic converts local address space references into Multibus I/O commands; physical address space references are converted into Multibus memory commands. To perform a memory or I/O access, the GDP outputs 24 address bits and 8 bits of control information (on the processor packet bus) in two 16-bit cycles. This 24-bit address is converted to a 20-bit Multibus address as described in paragraph 4-5. To perform this conversion, an address offset register is used, permitting the iSBC 432/100 board to share Intellec system memory with another processor. All iSBC 432/100 Multibus memory references are translated to addresses in upper memory (as specified by the offset value). In this manner, software for the system processor (e.g., the Intellec operating system) is protected from iSBC 432/100 accesses, allowing both processors to operate independently.

The iSBC 432/100 board is designed to operate within 8- or 16-bit wide Multibus systems; a single user selectable jumper option configures the board for the appropriate operating mode. For each data transfer, the GDP indicates the number of bytes to be transferred by means of a three-bit code embedded in the eight control bits (output by the GDP at the start of each transfer). This code specifies a one to ten byte transfer (1, 2, 4, 6, 8, or 10 bytes). In the 8-bit transfer mode, data reads and writes are performed one byte at a time over the Multibus bus. In the 16-bit mode, data reads and writes are performed as follows:

1. When a single byte transfer is requested, an 8-bit Multibus read or write is performed.

2. When a multibyte transfer is requested on an even byte boundary, the appropriate number of 16-bit Multibus transfers is performed.

3. When a multibyte transfer is requested on an odd byte boundary, the appropriate number of 8-bit Multibus transfers is performed.

In the 8-bit mode a single 80-bit (10 byte) processor requested read or write operation requires ten Multibus accesses. A jumper option is provided that permits the iSBC 432/100 processor to lock the bus during a complete data transaction. Using this "bus lock" provision results in faster overall processor operation.

CAUTION

The "bus lock" cannot be used in systems with double-density diskette controllers and 8-bit memory if the disk controller is required to operate simultaneously with the iSBC 432/100 Processor Board.

The actual data transfers in both the 8- and the 16-bit mode are controlled by a small FPLA state machine in conjunction with a memory transfer counter. The state machine determines whether the 8- or the 16-bit transfer mode is active and requests the correct number of Multibus accesses. All Multibus accesses are carried out by means of an 8288 bus controller and an 8289 bus arbiter.

The iSBC 432/100 board also contains a serial I/O port and three timers. One timer provides the baud rate clock for the serial I/O port. The other two timers are cascaded to generate a process clock (PCLK) for the 43202. The board also contains a number of miscellaneous I/O flags that can be read or written (from the bus) to control processor operation and monitor processor status. I/O port address assignments are detailed in paragraph 3-3.

4.2 FUNCTIONAL DESCRIPTION

The iSBC 432/100 Processor Board may be functionally subdivided into 6 units:

1. CPU and I/O Clock Generators
2. iAPX 432 Processor
3. Address Generator
4. Data Transfer State Machine
5. Multibus Interface
6. Input and Output

Figure 4-1 illustrates the approximate location of each functional unit on the iSBC 432/100 Processor Board; a block diagram of the board is shown in figure 4-2. The following paragraphs present a brief description of each functional unit. A circuit analysis of each unit is also given (beginning with paragraph 4-11).

4.3 CLOCK GENERATION

Two clocks are generated on the iSBC 432/100 board. One clock drives the GDP and all on-board logic that is synchronized with the processor. The second clock drives both the 8253 Programmable Interval Timer (PIT) and the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

GDP operation requires two clock phases, CLKA and CLKB, that differ by 90 degrees (refer to figure 4-3). These clock phases are generated from the output of a crystal oscillator and both are buffered by high-current line drivers and resistively terminated.

The second clock is derived from a 14.7456 MHz crystal attached to an 8284 clock generator. The divide-by-six output of the 8284 (2.4576 MHz) provides the 8251A master clock. This frequency is further divided by two, generating a 1.2288 MHz clock for the 8253 timers. The 8253 is programmed to provide the baud rate for the 8251A.

4.4 iAPX 432 PROCESSOR

The GDP is composed of two VLSI devices: the 43201 and the 43202. These devices are interconnected by means of a dedicated 16-bit bus and three dedicated status signals. Both devices operate with the same clock and are connected to a common 16-bit multiplexed address/data bus. The two clock phases (CLKA and CLKB) control the 43201/43202 timing. The GDP interfaces with external logic by means of the 16-bit multiplexed address/data bus (the packet bus or ACD bus). All external logic timing is synchronous with clock transitions. Most input signals are sampled by the processor on the rising edge of CLKA; inputs on the ACD bus are sampled on the falling edge of CLKA. Most CPU outputs may be sampled by external logic on the falling edge of CLKA.

Data read and write addressing information is output on the ACD bus by the GDP in two 16-bit information cycles. The first double-byte output contains an 8-bit operation code and the least significant 8 bits of the address. The next double-byte contains the most significant 16 bits of the address. The 8-bit operation code contains an operation specifier (1 bit), an access specifier (1 bit), and a length specifier (3 bits). The operation specifier indicates whether the procesor is executing a read or write operation. The access specifier indicates the issuance of a local address versus a physical memory address. Finally, the length specifier indicates the number of data bytes (1, 2, 4, 6, 8, or 10) affected by the data transfer. During processor transfer requests, the external circuitry handshakes with the GDP by means of the ISA and ISB control signals.
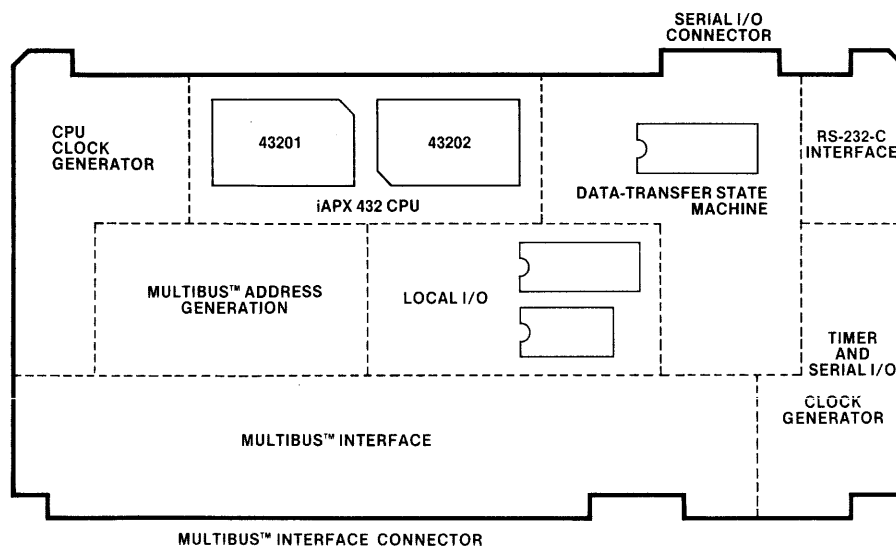
Figure 4-1. iSBC 432/100™ Processor Board Functional Areas

171820-16
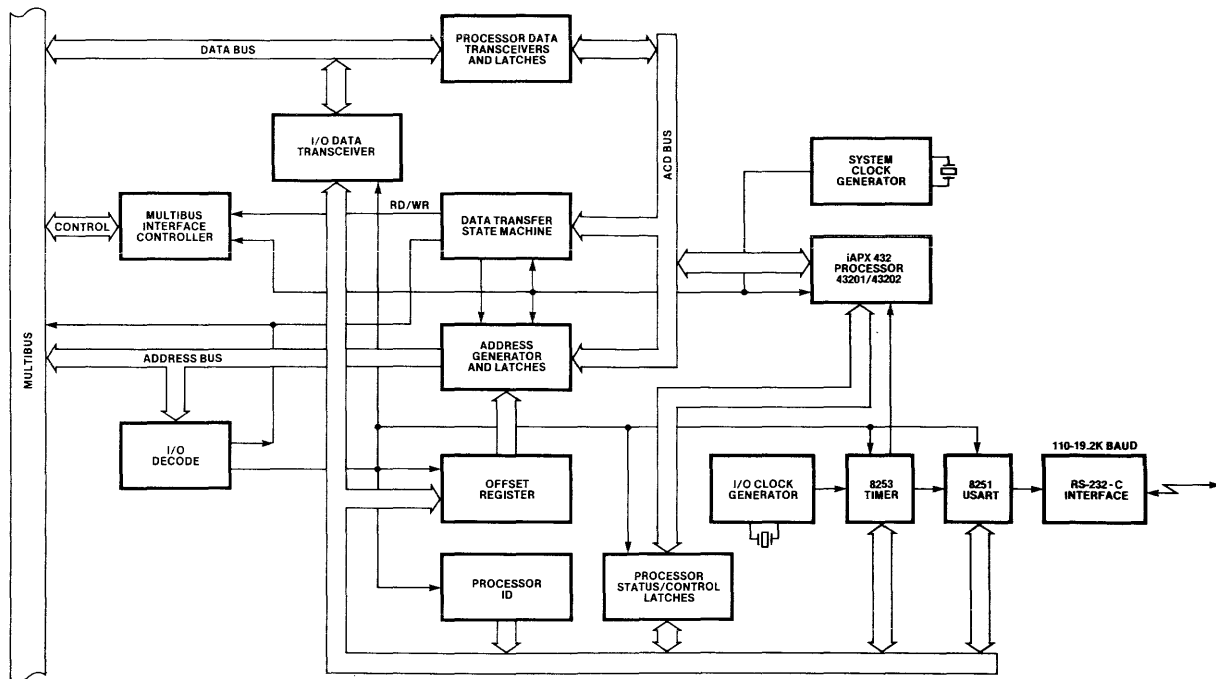
Figure 4-2. iSBC 432/100™ Processor Board Block Diagram   171820-17
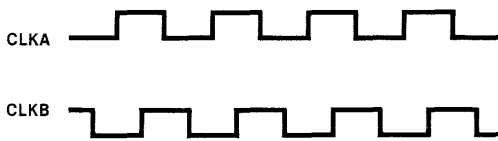
Figure 4-3. Two-Phase Overlapped Processor
Clock   171820-18

The ACD bus is also used to transfer data to and from the processor for read and write accesses. During a write access, the data is output as a sequence of up to five double-bytes (80 bits) immediately following the two initial addressing specification cycles; on a read request, the processor inputs the required number of double-bytes from the ACD bus. If the read or write data is a single 8-bit data element, it appears on the least significant bits of the 16-bit ACD bus.

The external circuitry may request that the processor hold (stretch) an access until the data is accepted (for a write access) or until the data is supplied (for a read access) by the external component(s). The ISB signal is used by the external circuitry to indicate this request to the processor. The stretch function may be requested on any double-byte of a read or write data transfer. After each double-byte transfer, the external circuitry must also indicate the success or failure of the transfer cycle by means of the ISB signal.

4.5 ADDRESS GENERATION

The 24-bit address issued by the iAPX 432 processor is converted into an initial 20-bit Multibus address as follows (refer to figure 4-4):

1. The upper four bits are discarded, leaving a 20-bit address.

2. The lower twelve address bits are directly loaded into three 4-bit counters.
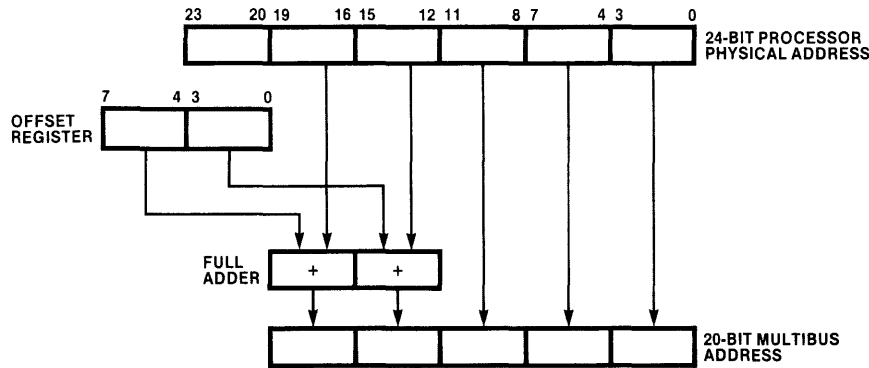
Figure 4-4. 24-Bit Processor Physical Address to 20-Bit Multibus™ Address Conversion   171820-19

3. The remaining eight bits are added to an address offset contained in an 8-bit offset register. The result of this calculation is loaded into two additional 4-bit counters. The offset register (an 8-bit I/O port on the board) may be loaded by a Multibus master as discussed in paragraph 4.18.

Once this initial address has been computed and latched into the five address counters, the data transfer state machine controls the actual data transfers between the bus and the GDP. As each 8- or 16-bit transfer is completed, the state machine updates (increments) the 20-bit address (stored in the counters) in order to correctly cycle through multibyte transfer requests.

4.6 DATA TRANSFER STATE MACHINE

The data transfer state machine is composed of a programmable logic array (PLA), a state register, a transfer counter, and a command decoder. The PLA, which is the heart of the state machine, generates the signals required to synchronize Multibus operations with processor data transfers. The state machine operates in either an 8-bit or 16-bit Multibus mode. A jumper option may be strapped by the user to force all operations to be performed in the 8-bit mode. Otherwise, in the 16-bit mode, all single byte transfers and all multibyte transfers initiated on odd addresses are forced into the 8-bit mode. The following descriptions of data transfer operations are graphically depicted in figure 4-5.

In the 8-bit mode, all Multibus operations are 8-bit (byte) transfers. If a single-byte read is requested by the processor, this byte is transferred from the least significant eight Multibus data lines (DAT0/-DAT7/) through a transparent latch (A54) to the

least significant byte of the ACD bus (ACD0-ACD7) as illustrated in figure 4-5a. When more than one byte is requested, two 8-bit Multibus operations are combined into a single 16-bit processor transfer. The first Multibus read latches DAT0/-DAT7/ into transparent latch A54, driving ACD0-ACD7. After incrementing the memory address, the second Multibus read operation transfers data from DAT0/-DAT7/ onto ACD8-ACDF (through transceiver A52). A double-byte read transfer is illustrated in figure 4-5b.

During a single-byte write transfer, data on ACD0-ACD7 is transferred to the DAT0/-DAT7/ data lines of the Multibus bus through transceiver A53 (refer to figure 4-5c). Multiple data byte transfers perform two Multibus write operations for each 16-bit ACD bus transfer. The first Multibus write transfers ACD0-ACD7 to the DAT0/-DAT7/ data lines (through transceiver A53). After incrementing the memory address, the second Multibus write operation transfers ACD8-ACDF to the DAT0/-DAT7/ Multibus data lines. This double-byte write transfer is shown in figure 4-5d.

In the 16-bit mode, a single byte read is performed through A54 (if the address is odd) or through A53 (if the address is even). A single-byte write transfers data through transceiver A53. In both a single-byte write and a single-byte read transfer, ACD0-ACD7 are connected to Multibus data lines DAT0/-DAT7/ (figure 4-5e to 4-5g). Multibyte transfers in the 16-bit mode are performed as a sequence of double-byte Multibus/processor operations. Each double-byte read transfers 16 bits of data from the multibus bus to the ACD bus by means of A53 (least significant byte) and A51 (most significant byte). Multibyte write operations utilize the same data path as used by the multibyte read transfers, but in the opposite direction. Multibyte transfers in the 16-bit mode are illustrated in figure 4-5h.

ACD$_{8-F}$ ——————— A51 ——————— DAT$_{8-F}$/

A52

A54

ACD$_{0-7}$ ◄——————— A53 ——————— DAT$_{0-7}$/

(A) SINGLE-BYTE READ TRANSFER, 8-BIT MODE

ACD$_{8-F}$ ——————— A51 ——————— DAT$_{8-F}$/

A52

FIRST MULTIBUS TRANSFER—
LOW BYTE IS LATCHED IN A54

A54

ACD$_{0-7}$ ——————— A53 ——————— DAT$_{0-7}$/

ACD$_{8-F}$ ◄——————— A51 ——————— DAT$_{8-F}$/

A52

SECOND MULTIBUS TRANSFER—
HIGH BYTE FROM BUS, LOW BYTE
FROM LATCH

A54

ACD$_{0-7}$ ◄——————— A53 ——————— DAT$_{0-7}$/

(B) DOUBLE-BYTE READ TRANSFER, 8-BIT MODE

ACD$_{8-F}$ ——————— A51 ——————— DAT$_{8-F}$/

A52

A54

ACD$_{0-7}$/ ——————— A53 ——————► DAT$_{0-7}$/

(C) SINGLE-BYTE WRITE TRANSFER, 8-BIT MODE

Figure 4-5. iSBC 432/100™ Data Transfer Routing to/from the Multibus™ Bus   171820-20

(D) DOUBLE-BYTE WRITE TRANSFER, 8-BIT MODE
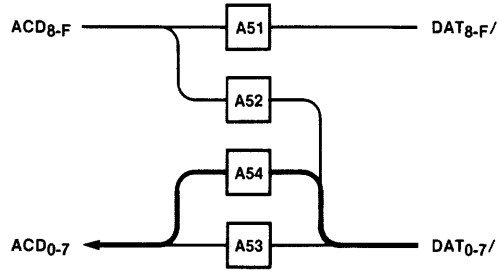
(E) SINGLE-BYTE READ TRANSFER (ODD ADDRESS), 16-BIT MODE
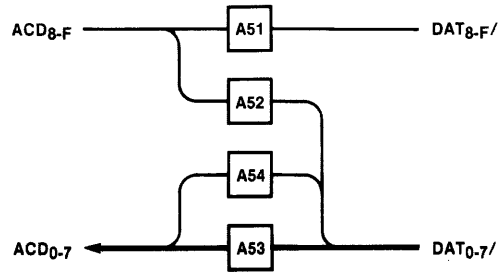
(F) SINGLE-BYTE READ TRANSFER (EVEN ADDRESS), 16-BIT MODE

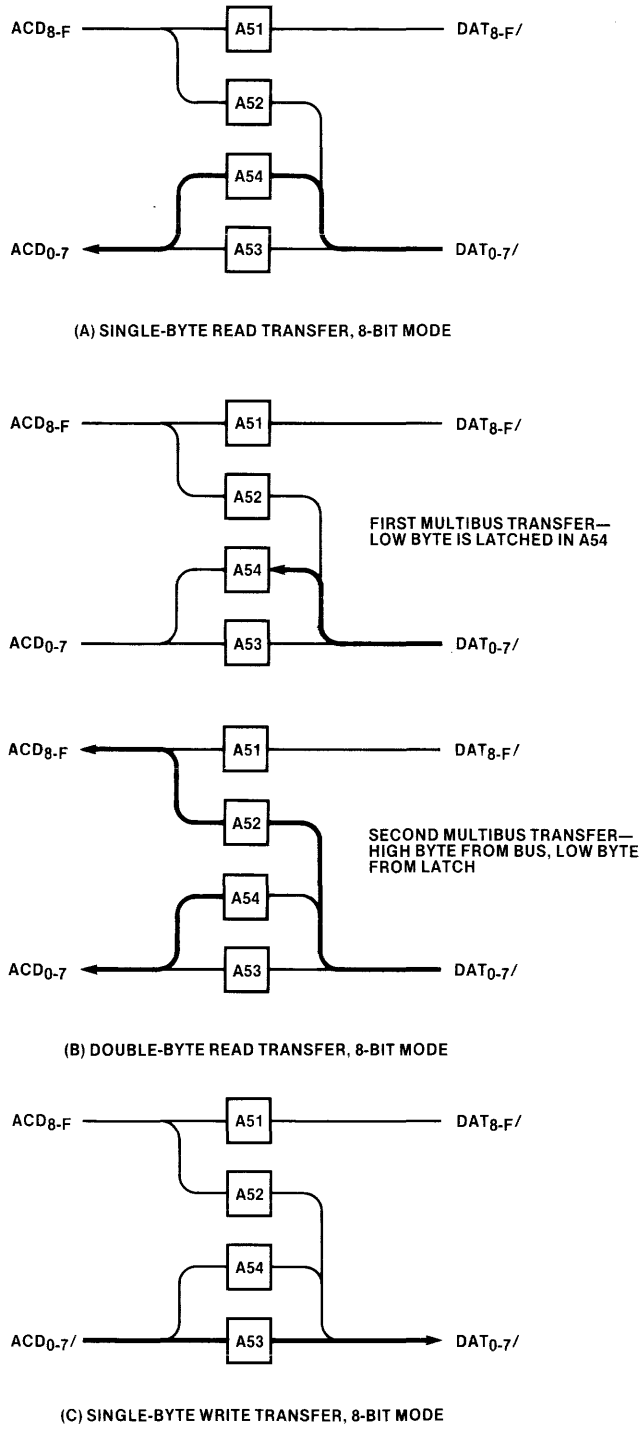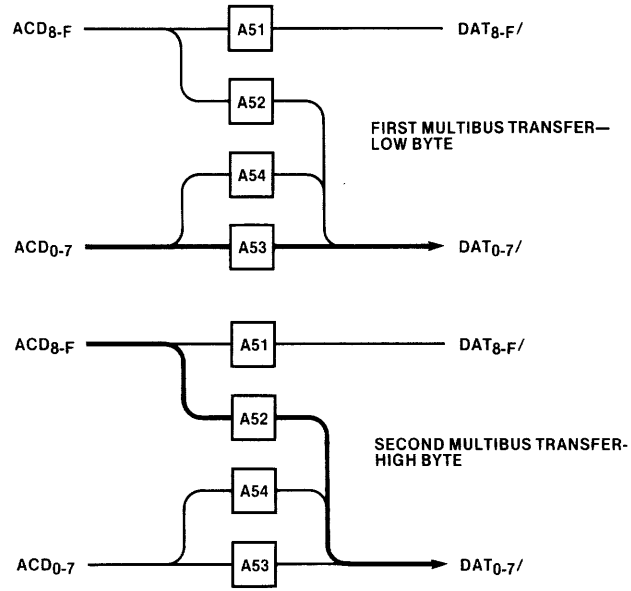Figure 4-5. iSBC 432/100™ Data Transfer Routing to/from the Multibus™ Bus (Cont'd.)   171820-20

(G) SINGLE-BYTE WRITE TRANSFER, 16-BIT MODE

(H) DOUBLE-BYTE READ/WRITE TRANSFER, 16-BIT MODE
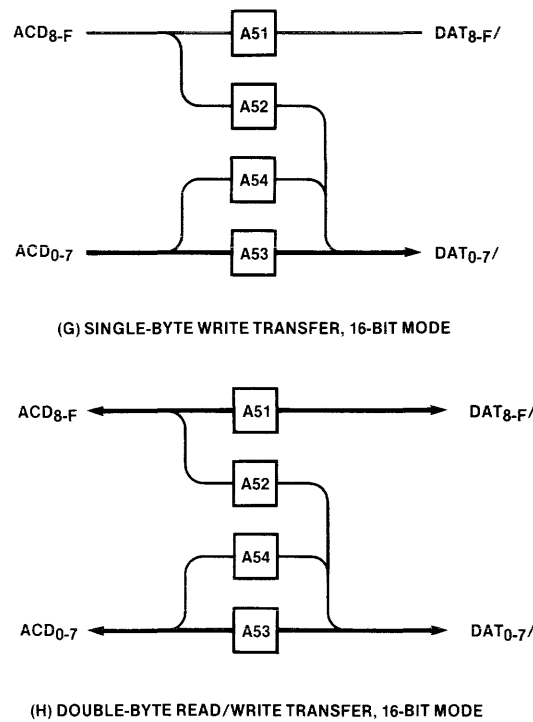
Figure 4-5. iSBC 432/100™ Data Transfer Routing to/from the Multibus™ Bus (Cont'd.)   171820-20

4.7 MULTIBUS INTERFACE

The iSBC 432/100 board is completely Multibus compatible and supports both 8-bit and 16-bit operations. The Multibus interface includes an 8288/8289 controller/arbiter pair that allows the iSBC 432/100 board to function as a Multibus master. Also included in the Multibus interface are address/data bus transceivers and latches and an I/O command decoder (discussed in paragraph 4-18). All I/O ports are directly accessible from the Multibus by any Multibus master.

4.8 INTERVAL TIMER

The 8253 PIT provides three 16-bit timers used on-board for serial I/O timing and for process timing. Counters 0 and 1 are cascaded to provide the process clock (PCLK) signal. Counter 2 generates a programmable baud rate for the 8251A serial I/O port. Baud rates from 110 to 19.2K are easily generated as discussed in paragraph 3-20 and table 3-2.

4.9 SERIAL I/O

The 8251A USART provides an RS-232-C compatible serial synchronous or asynchronous data link for CRT terminal operation. Character size, parity bits, stop bits, and baud rates are all programmable as discussed in paragraph 3-5.

4.10 PARALLEL I/O

Four parallel I/O ports are contained on the iSBC 432/100 board to support processor control and status reporting functions. An 8-bit offset register (write-only), used in addressing calculations (refer to paragraphs 4-5 and 4-18), may be set from the Multibus bus to translate processor addresses into Multibus addresses. A second write-only I/O port controls processor initialization and allows another Multibus master to start, stop, and alarm the iSBC 432/100 processor (see paragraph 3-23).

The third I/O port (read-only) may be interrogated by other Multibus masters to determine the processor status (see paragraph 3-23). In addition, three jumper selectable inputs are user configurable and may be read by any Multibus master, including the GDP. These inputs may be used to specify user-dependent configuration options (such as CRT model selection). The fourth I/O port (read-only) supplies the GDP with a unique processor ID. This processor ID is used by the GDP during initialization to determine processor dependent parameters.

4.11 CIRCUIT ANALYSIS

The schematic diagram for the iSBC 432/100 board is given in figure 5-2. The schematic diagram consists of 7 sheets, each of which includes grid coordinates. Signals that traverse from one sheet to another are assigned grid coordinates at both the signal source and the signal destination. For example, the grid coordinates 2B1 locate a signal source (or signal destination) on sheet 2 in zone B1.

Both active-high and acitve-low signals are used. A signal mnemonic that ends with a virgule (e.g., DAT7/) denotes that the signal is active-low ($\leq 0.4V$). Conversely, a signal mnemonic without a virgule (e.g., BYTOP) denotes that the signal is active-high ($\geq 2.0V$).

4.12 INITIALIZATION

When the Multibus INIT/ signal is activated, the iSBC 432/100 Processor Board is forced into the following state:

1. The GDP is initialized and held in the initialized state by pulling the PINIT/ signal low (through flip-flops A22 and A24 at 4D6 and 4D4).

2. The data transfer state machine is initialized to state zero (by the PINIT/ input to latch A25 at 4C4).

3. The bus interrupt flip-flop, A22 (4D6), is cleared.

4. The external "stop" command flip-flop, A26 (4C6), is cleared.

5. The bus arbiter is reset (outputs are 3-stated).

6. The serial I/O port is set to the "idle" mode.

4.13 CLOCK GENERATION

The CPU clock is generated by two flip-flops (in A1 at 5C6) from a master oscillator (A12 at 5D7). The resulting overlapped CPU clock phases (CLKA and CLKB) are driven through a resistive termination by 50-ohm line drivers (A2 at 5C5). In addition, CLKA/ is driven to various positions on the board by a

separate 50-ohm line driver (A3 at 5C5). CLKA/ controls the timing of the address counters, the transfer counter, and the data transfer state machine.

The I/O clock is developed by an 8284 clock generator (A41 at 3D6) and crystal Y1 (14.7456 MHz). This frequency is internally divided by six within the 8284 to provide a 2.4576 MHz master clock to the 8251A USART (A21 at 3C4). This clock is also divided by two by flip-flop A23 (3D4) to supply a 1.2288 MHz clock to the 8253 PIT (A36 at 3B4).

4.14 iAPX 432 GENERAL DATA PROCESSOR

As discussed previously, the GDP outputs the address and operation code on the ACD bus in two double-byte cycles (paragraph 4-1). During a write cycle, the write data immediately follows these two double-byte addressing specification cycles. The timing of a typical processor write cycle is illustrated in figure 4-6 while the timing of a typical read cycle is illustrated in figure 4-7. The information contained within the 8-bit operation code is shown in figure 4-8.

4.15 ADDRESS GENERATION

At the start of a data transfer operation, the complement of the transfer length is latched into the transfer up-counter (A57 at 7C3). The access type, operation type, and least-significant address bit (odd/even flag) are clocked into latch A38 (7C3). Discrete logic gates (A58 and A14 at 7B2) generate the CNT1 signal (from the output of the transfer counter) that is used by the data transfer state machine to determine when the last data byte is transferred. At the same time, the least significant address byte (output by the processor on ACD0-ACD7) is latched into two 4-bit up-counters, A33 and A34 (6B4).

The second double-byte issued by the procesor (upper 16 address bits) is divided into three portions. The upper four bits are discarded. The lower four bits are routed directly to a 4-bit up-counter, A17 (6B4). The remaining eight bits are routed to two 4-bit adders (A15 and A16 at 6C6) where they are combined with the address offset from A18 (4A6). The resulting address is latched into two 4-bit up-counters (A31 and A32 at 6C4) to complete the generation of a 20-bit Multibus address.

4.16 DATA TRANSFER STATE MACHINE

The heart of the data transfer state machine is an 82S100 PLA (A28 at 4C3). The eight output signals of the PLA are divided into three segments: a 4-bit

*INTERPROCESSOR COMMUNICATION REQUEST WINDOW
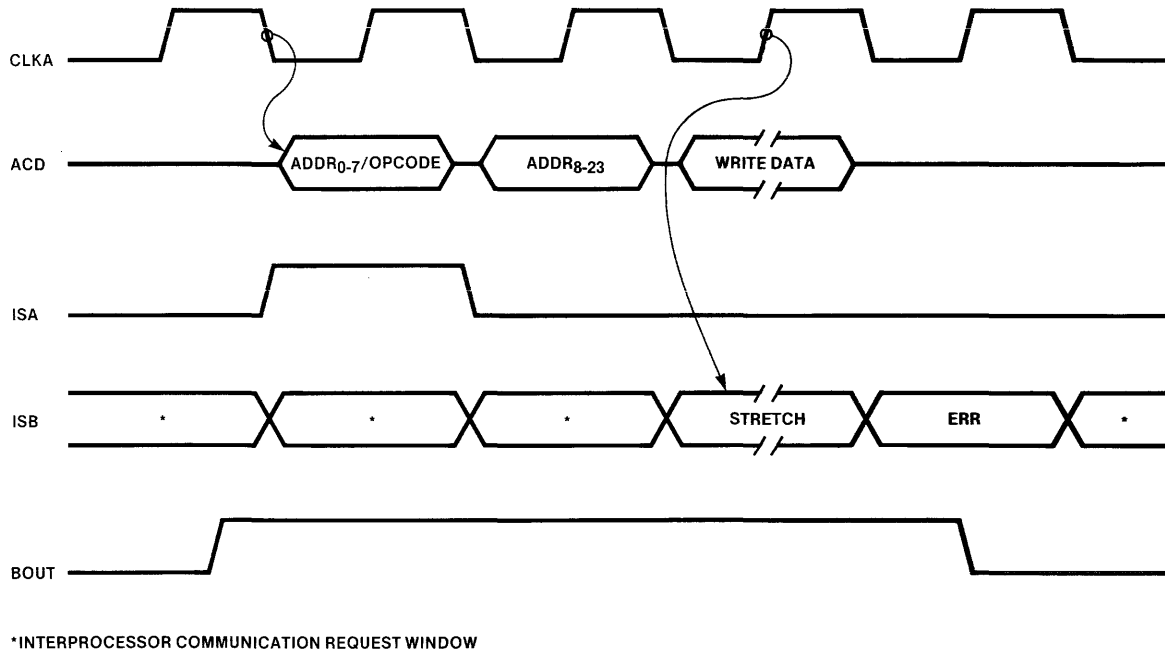
Figure 4-6. Typical Processor Write Cycle Timing   171820-21

*INTERPROCESSOR COMMUNICATION REQUEST WINDOW
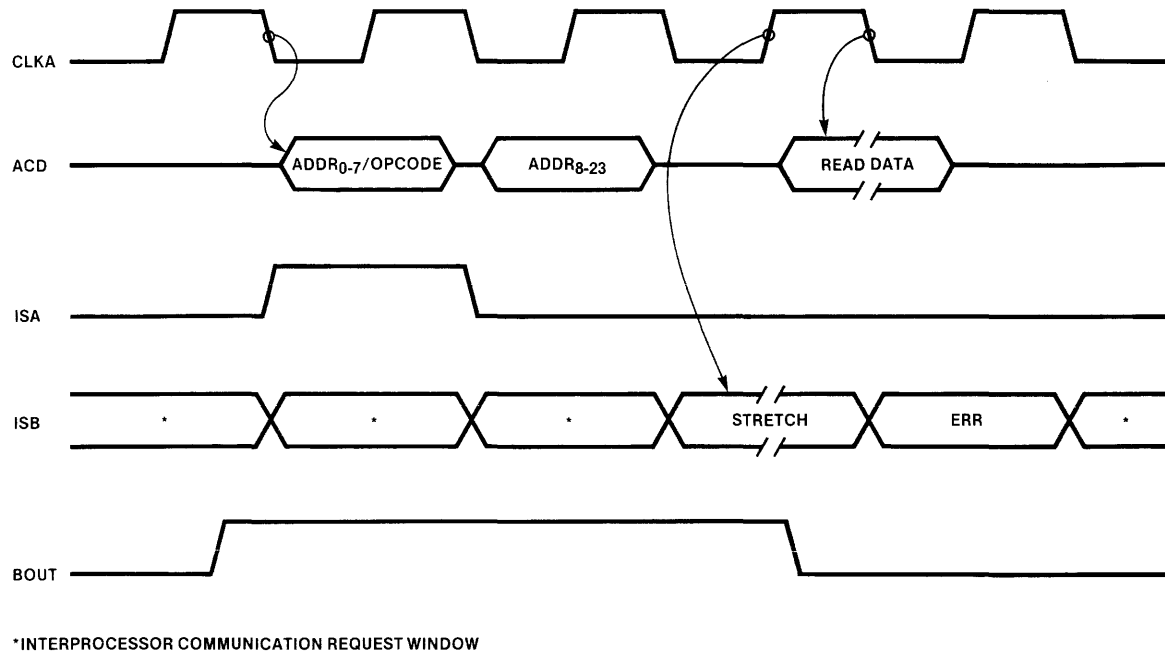
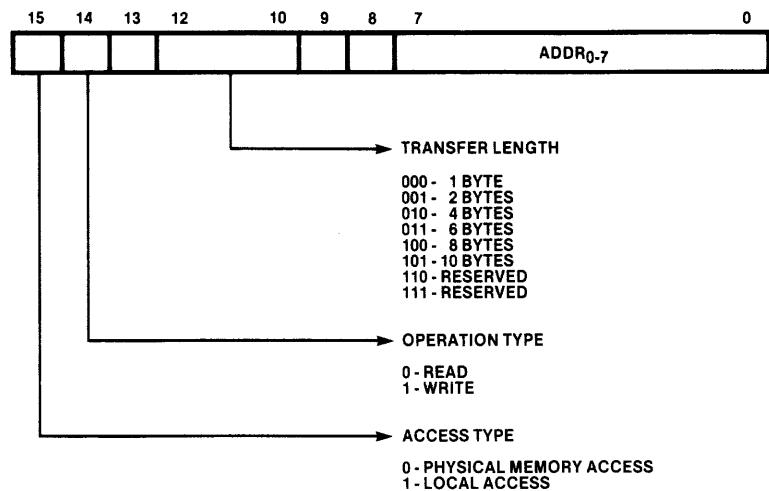Figure 4-7. Typical Processor Read Cycle Timing   171820-22

Figure 4-8. Eight-Bit Transfer Specification Opcode.

"next" state (recorded in latch A25 at 4C4), a 3-bit command code, and the processor ISB signal. The inputs to the PLA include the 4-bit current state (from latch A25), the processor ISA signal, the CNT1 signal from the transfer counter, the odd/even address flag (least significant address bit), and the operation type (read/write).

In addition, three synchronized signals are input to the PLA: the Multibus transfer acknowledge signal (XACK/), the interprocessor communication request (from flip-flop A23 at 4C6), and the processor "access stop" request (from flip-flop A26 at 4C6).

A transition from one PLA state to another state occurs as the result of an input signal change. The following twelve input signals (16 bits) completely control state transitions:

Input Signal	Description
STATE	4-bit current state number (from A25 at 4C4)
ISA	Processor generated data transfer request signal
IPCRQ	Interprocessor communication request (from A23 at 4C6)
BXACK	Synchronized Multibus XACK signal
STOPRQ	Processor "access stop" request (from A26 at 4C6)
PINIT/	Processor initialization signal
CNT1	Last-byte transfer indicator
A0	Odd/even address flag (least significant address bit)
WRITE	Processor write transfer indicator

During each state transition clock cycle, one of the following eight commands (specified by the 3-bit command code) is executed:

Command Code	Command Name	Description
0	COUNT	Increments the transfer counter.
1	CLRIPC	Clears pending interprocessor communication requests.
2	LDLOW	Latches the least-significant 8 bits of the initial Multibus address in the address counters (A33 and A34).
3	LDHIGH	Latches the most-significant 12 bits of the initial Multibus address into the address counters (A17, A31, and A32).
4	UNLOCK	Unlocks the Multibus bus (overrides the bus lock) at the completion of a processor-requested data transfer.
5	STOPPED	Signals that processor Multibus accesses have been stopped.
6	NOOP	No operation.
7	——	Not used.

The state diagram for the data transfer state machine is given in figure 4-9. To illustrate actual state machine operation, the following paragraphs describe a four byte memory write operation on an even byte boundary (in the 16-bit mode). While reading the discussion, follow the state transitions as depicted in figure 4-9.

After initialization and before the start of a transfer, the state machine idles in state 0, maintaining ISB high, and waiting for the processor to raise the ISA signal (indicating the beginning of a data transfer operation). When the state machine senses a high ISA signal, it enables the LDLOW/ signal and continues to maintain a high ISB signal. The state machine immediately enters state 8. Activation of the LDLOW/ signal causes the least-significant address byte and operation code information to be latched as described in paragraph 4.15. Shortly after the activation of the LDLOW/ signal, the CNT1 signal and A0 signal are both set low by the logic associated with A57 and A38 (7C3).

On the subsequent clock cycle, the processor lowers the ISA signal as it outputs the upper 16 bits of the address. The state machine recognizes this action and activates the LDHIGH/ signal, latching the upper address bits into the Multibus address latches. The state machine enters state 2 and waits until the BXACK input is inactive (from previous transfers) before proceeding with the actual data transfer). Instead of lowering ISA, the processor may cancel the current access by maintaining ISA high for an additional clock cycle.

As soon as BXACK is determined to be inactive, the state machine enters state 7, ISB is lowered (to begin stretch), and the ACCESS/ signal is enabled (A3 at 4C2) in order to begin the first Multibus operation. The state machine remains in state 7 until XACK/ has been activated by the addressed device on the Multibus (indicating "write data accepted") and until the XACK signal has propagated through the synchronizing flip-flops in A24 (4D4). At this point, when BXACK is sensed active, (CNT1=0, A0=0, and WRITE=1 in this example), the state machine increments the bus address (contained in the address counters), increments the transfer counter, and enters state 14. State 14 inserts a delay to satisfy the Multibus data hold time requirements. On the next cycle, the state machine exits state 14 and enters state 1, raising the ISB signal to end stretch.

Since the data transfer in this example is not yet complete (only two of the four bytes have been transferred and CNT1 is low), the Multibus address is again incremented. The state machine reenters state 2 and waits until BXACK has been removed (after the previous transfer). At the same time, ISB is lowered to indicate an error-free data transfer. Events for this second 16-bit data transfer proceed from state 2 to state 1 in the same manner as the events proceeded for the first transfer. During this second transfer, CNT1 changes from low to high immediately following the transfer counter incrementation (between state 14 and state 1). Once in

state 1, ISB is set to zero, indicating a second error free transfer, and the state machine reenters the idle state (state 0).

4.17 MULTIBUS INTERFACE

The Multibus interface consists of the 8288/8289 bus controller/arbiter pair (A45 and A46 at 2C5), bidirectional data bus transceivers (A51, A52, and A53 at 7B5 and A55 at 3B6), a data latch (A54 at 7B5), and address buffers (A47, A48, and A49 at 6C2).

The falling edge of BCLK/ provides the bus timing reference for the bus arbiter, which allows the iSBC 432/100 board to assume the role of a bus master. When the data transfer state machine enters one of the predefined Multibus transfer states (state 7 or state 15), the ACCESS/ signal is activated. This signal causes flip-flop A30 (2B7) to enable bus arbitration activity. Three output signals from the processor request status latch (A38 at 7C3) are used to indicate the type of Multibus activity required. The READ and WRITE signals specify data read and write cycles, respectively. The LOCAL/ signal indicates an I/O transfer when it is low (a local address read or write), and a memory transfer when the signal is high (a physical address read or write). READ, WRITE, and LOCAL/ are input to the S0-S3 pins of the bus arbiter to control Multibus activity.

When a Multibus transfer is initiated, the bus arbiter drives BREQ/ low and BPRO/ high. The BREQ/ output from each bus master in the system is used when bus priority is resolved in a parallel priority scheme as described in paragraph 2.14. The BPRO/ output is used when the bus priority is resolved in a serial priority scheme as described in paragraph 2.13.

The iSBC 432/100 gains control of the bus when the BPRN/ input to the bus arbiter is driven low and the bus is not busy (BUSY/ inactive). On the next falling edge of BCLK/, the bus arbiter activates the BUSY/ and AEN/ signals (driving them low). The BUSY/ output indicates that the bus is in use and that the current bus master (in control of the bus) has total bus control until the master releases the bus by deactivating its BUSY/ signal. The AEN/ output, which can be thought of as a "master bus control" signal, is applied to the bus address buffers (A47, A48, and A49 at 6B2) and to the input of gate A14-5 (3A5). With AEN/ enabled, the board is prepared to recognize the ensuing acknowledge signal (XACK/) transmitted by the addressed system device.
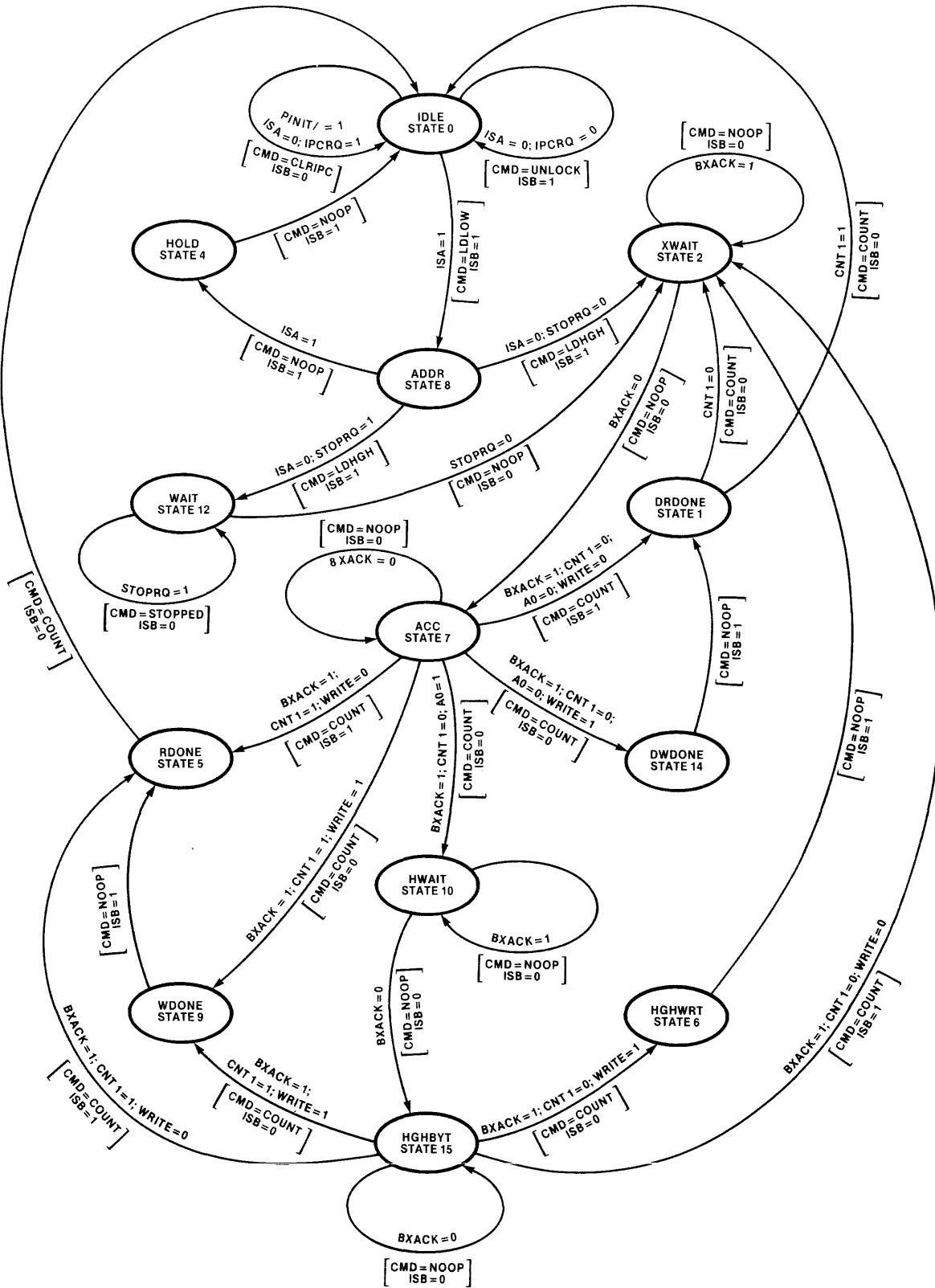
Figure 4-9. Data Transfer State Machine State Diagram

171820-24

Data Transfer State Machine Description

State (Number)	Activating Input(s)	Next State	ISB	Output Command	Comments
IDLE(0)	ISA=0 IPCRQ=0	IDLE	1	UNLOCK	Wait for something to happen
IDLE	ISA=0 IPCRQ=1 PINIT/=1	IDLE	0	CLRIPC	Issue pending IPC if no access
IDLE	ISA=1	ADDR	1	LDLOW	Access start, capture low address
ADDR(8)	ISA=1	HOLD	1	NOOP	Access cancelled
ADDR	ISA=0 STOPRQ=1	WAIT	1	LDHIGH	Load high address; stop accesses on stop request
ADDR	ISA=0 STOPRQ=0	XWAIT	1	LDHIGH	Load high address
HOLD(4)	——	IDLE	1	NOOP	Prevent an IPC after a cancel
WAIT(12)	STOPRQ=1	WAIT	0	STOPPED	Set stopped status and wait for the stop request to end
WAIT	STOPRQ=0	XWAIT	0	NOOP	Exit wait to continue access
XWAIT(2)	BXACK=1	XWAIT	0	NOOP	Wait for BXACK inactive to start access
XWAIT	BXACK=0	ACC	0	NOOP	Start the access
ACC(7)	BXACK=0	ACC	0	NOOP	Wait for access complete
ACC	BXACK=1 CNT1=1 WRITE=0	RDONE	1	COUNT	Byte read access complete
ACC	BXACK=1 CNT1=1 WRITE=1	WDONE	0	COUNT	Byte write, stretch write access to satisfy hold time
ACC	BXACK=1 CNT1=0 A0=0 WRITE=0	DRDONE	1	COUNT	Double-byte read access complete
ACC	BXACK=1 CNT1=0 A0=0 WRITE=1	DWDONE	0	COUNT	Double-byte write, stretch write access to satisfy hold time
ACC	BXACK=1 CNT1=0 A0=1	HWAIT	0	COUNT	Odd access boundary, perform one byte at a time
HWAIT(10)	BXACK=1	HWAIT	0	NOOP	Wait until BXACK done
HWAIT	BXACK=0	HGHBYT	0	NOOP	Start high byte access
HGHBYT(15)	BXACK=0	HGHBYT	0	NOOP	Wait for access to complete
HGHBYT	BXACK=1 CNT1=0 WRITE=0	XWAIT	1	COUNT	Start next double-byte
HGHBYT	BXACK=1 CNT1=0 WRITE=1	HGHWRT	0	COUNT	Stretch write data
HGHBYT	BXACK=1 CNT1=1 WRITE=0	RDONE	1	COUNT	Read access complete
HGHBYT	BXACK=1 CNT1=1 WRITE=1	WDONE	0	COUNT	Stretch write data
HGHWRT(6)	——	XWAIT	1	NOOP	Complete write operation
DWDONE(14)	——	DRDONE	1	NOOP	Complete write operation
DRDONE(1)	CNT1=0	XWAIT	0	COUNT	Get next double-byte
DRDONE	CNT1=1	IDLE	0	COUNT	Access complete, no errors
WDONE(9)	——	RDONE	1	NOOP	Complete write operation
RDONE(5)	——	IDLE	0	COUNT	Access complete, no errors

Figure 4-9. Data Transfer State Machine State Diagram (Cont'd.)   171820-24

When a Multibus transfer is initiated, the bus controller (A46 at 2B5) is also enabled, The controller decodes the S0-S2 control signals and drives the appropriate Multibus command lines low when AEN/ is activated by the bus arbiter. The bus controller also drives DEN high to selectively enable data bus drivers/receivers A51, A52, A53, and/or A54 (7B5) as described in paragraph 4.6. The data bus drivers are switched to the appropriate "transmit" or "receive" mode depending on the state of the READ, WRITE, and processor generated BOUT signals.

After the command is acknowledged (signified by the addressed device driving the Multibus XACK/ line low), the data transfer state machine terminates the command. The bus arbiter and bus controller, respectively, terminate AEN/ and DEN; the bus arbiter also relinquishes control of the bus by driving BREQ/ high and BPRO/ low and then raising BUSY/.

When gaining control of the bus, the iSBC 432/100 board can invoke a "bus lock" condition to prevent loss of bus control during Multibyte transfers (see paragraph 2.10 and table 2-2). The "bus lock" condition is invoked by driving the bus arbiter LOCK pin low. The "bus lock" capability is enabled by a user-selectable jumper option (A30 at 2A6).

4.18 I/O OPERATION

The following paragraphs describe on-board I/O operations. All on-board I/O devices are accessible only from the Multibus bus. The actual functions performed by specific read and write commands to on-board I/O devices are described in Chapter 3.

Multibus address bits ADR0/ through ADR7/ are applied to the I/O address decoder, which is composed of A50, A37, A13, and A28 (2D5). The board I/O base address is user-selected from the jumper matrix associated with the address decoder A50 (2C5). This address decoder decodes a portion of the incoming address bits (ADR3/ through ADR7/) from the bus. Addresses ADR0/ through ADR2/ further qualify the I/O address and are decoded by A37 to provide chip selects for the 8253 PIT, the 8251A USART, and the four parallel I/O ports:

Address*	Chip Select	I/O Device
00	PRID/	Processor ID Register
X2,X4,X6	53CS/	8253 PIT
XA	51CS/	8251A USART
XC	OFFCS/	Address Offset Register
XE	STATCS/	Processor Status/Control Register

*X may be 1 through 7 as selected from the base address jumper matrix.

5.1 INTRODUCTION

This chapter provides a list of replaceable parts, a schematic diagram, and a parts location diagram for the iSBC 432/100 Processor Board.

5.2 REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the iSBC 432/100 board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

5.3 SCHEMATIC AND PARTS LOCATION DIAGRAMS

The iSBC 432/100 parts location diagram and schematic diagram are provided in figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a virgule (e.g., IOWC/) is active low. Conversely, a signal mnemonic without a virgule (e.g., BYTOP) is active high.

5.4 SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacting the Intel Product Service Hotling in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other MCSD products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other MCSD products, the serial number is usually stamped on a label.

d. Shipping & billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following numbers for contacting the Intel Product Service Hotline:

All U.S. locations, except Alaska, Arizona, & Hawaii
Telephone:
    (800) 528-0595

All other locations telephone:
    (602) 869-4600

TWX Number:
    910-951-1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

Table 5-1. Replaceable Parts

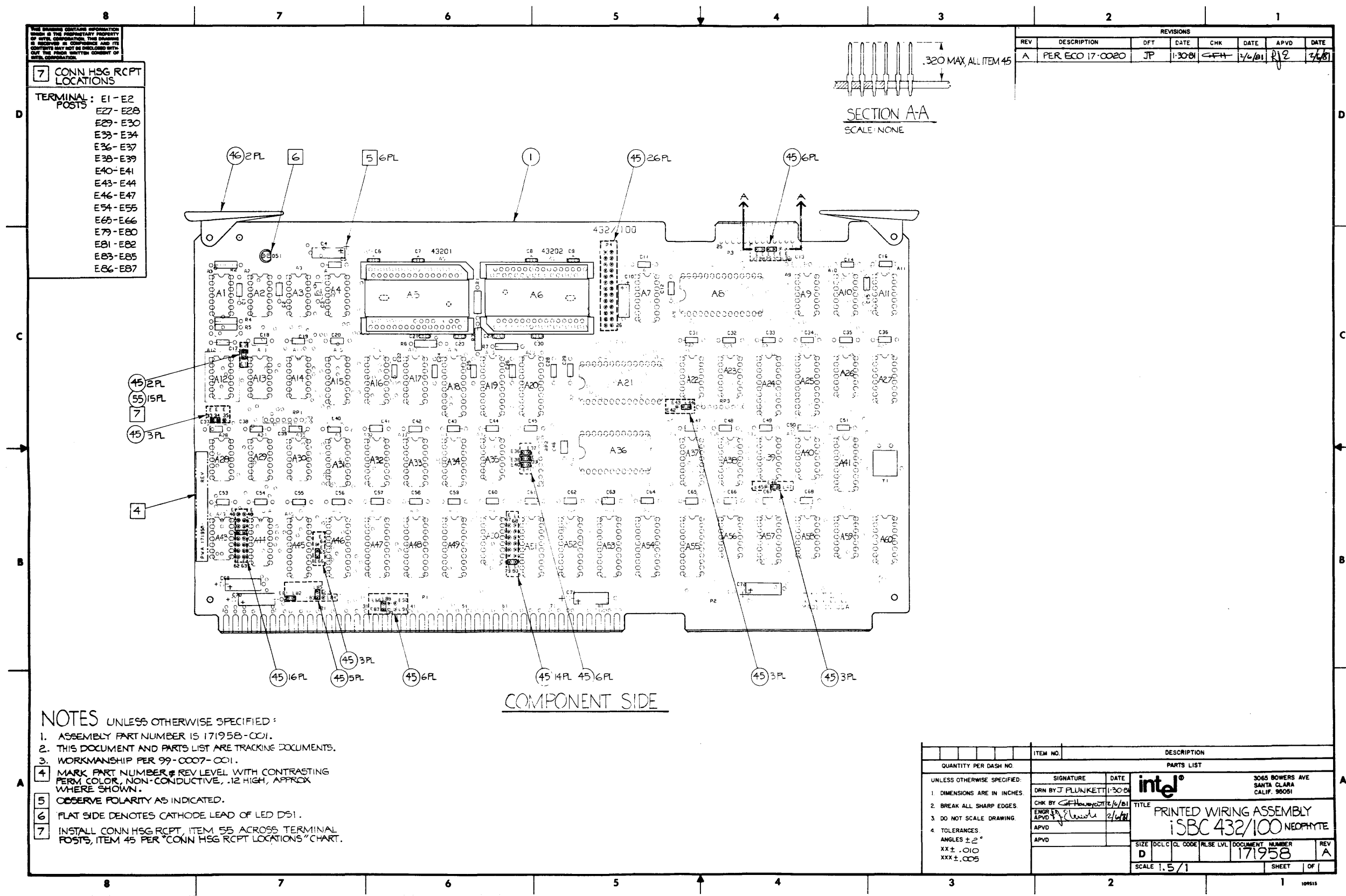| Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty
A7,50	IC, Intel 8205, 3-to-8 Decoder	8205	COML	2
A21	IC, Intel 8251A, USART	8251A	COML	1
A36	IC, Intel 8253, Programmable Interval Timer	8253	COML	1
A47,48,49,54	IC, Intel 8283, Octal Latch	8283	COML	4
A41	IC, Intel 8284, Clock Generator	8284	COML	1
A19,20,51,52, 53,55	IC, Intel 8287, Octal Transceiver	8287	COML	6
A46	IC, Intel 8288, Bus Controller	8288	COML	1
A45	IC, Intel 8289, Bus Arbiter	8289	COML	1
A5	IC, Intel 43201, General Data Processor	43201	COML	1
A6	IC, Intel 43202, General Data Processor	43202	COML	1
A14	IC, 74LS02, Quad 2-Input NOR Gates	SN74LS02	TI	1
A9,35	IC, 74LS04, Hex Inverters	SN74LS04	TI	2
A56,58	IC, 74LS10, Triple 3-Input NAND Gates	SN74LS10	TI	2
A22,23,26	IC, 74LS74, Dual D Flip-Flops	SN74LS74	TI	3
A29	IC, 74LS125, Quad Three-state Bus Buffers	SN74LS125	TI	1
A17,31,32,33 34,57	IC, 74LS163, Binary 4-Bit Counter	SN74LS163	TI	6
A43	IC, 74LS164, 8-Bit Shift Register	SN74LS164	TI	1
A38	IC, 74LS175, Quad D Flip-Flops	SN74LS175	TI	1
A18,24,25	IC, 74LS273, Octal D Flip-Flops	SN74LS273	TI	3
A15,16	IC, 74LS283, 4-Bit Full Adders	SN74LS283	TI	2
A44	IC, 74LS367, Hex Bus Drivers	SN74LS367	TI	1
A4,39	IC, 74S00, Quad 2-Input NAND Gates	SN74S00	TI	2
A13	IC, 74S08, Quad 2-Input AND Gates	SN74S08	TI	1
A28,40	IC, 74S32, Quad 2-Input OR Gates	SN74S32	TI	2
A1,30	IC, 74S74, Dual D Flip-Flops	SN74S74	TI	2
A37	IC, 74S139, Dual 2-to-4 Decoder	SN74S139	TI	1
A2,3	IC, 74S140, Dual 4-Input Line Driver	SN74S140	TI	2
A11	IC, 75188, Quad Line Driver	SN75188	TI	1
A10	IC, 75189A, Quad Line Receiver	SN75189A	TI	1
A8	IC, 82S100, FPLA	82S100	SIG	1
A12	Oscillator, Crystal, 20.000 MHz	K1100A	MOT	1
C52	Cap., mica, 10pF, 5%, 100V	OBD	COML	1
C15	Cap., cer, 330pF, 10%, 50V	OBD	COML	1
C1-3,12-14, 16,20,22, 24-26,28,29, 31-51,53-68	Cap., cer, .01µF, +80 −20%, 50V	OBD	COML	51
C5,11,18,19	Cap., cer, .1µF, +80 −20%, 50V	OBD	COML	4
C6-9,21,23, 27,30	Cap., cer, RDL, .1µF, +80 −20%, 50V	OBD	COML	8
C17	Cap., cer, 1µF, +80 −20%, 50V	OBD	COML	1
C70,71	Cap., tant, axial, 4.7µF, 20%, 15V	OBD	COML	2
C4,10	Cap., tant, axial, 22µF, 20%, 10V	OBD	COML	2
C69,72	Cap., tant, 22µF, 10%, 15V	OBD	COML	2
DS1	Diode, Red LED, 1.2 MCD	OBD	COML	1
R1,3	Res., fxd, comp, 100 ohm, 5%, ¼W	OBD	COML	2

Table 5-1. Replaceable Parts (Cont'd.)

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty
R2	Res., fxd, comp, 220 ohm, 5%, ¼WS	OBD	COML	1
R4,5	Res., fxd, comp, 1K ohm, 5%, ¼W	OBD	COML	2
RP1-3	Res., pack, 8 pin, 1K ohm, 2%, 2W	OBD	COML	3
XA12	Socket, 14-pin, DIP	514-AG19D	AUG	1
XA36	Socket, 24-pin, DIP	524-AG11D	AUG	1
XA8,21	Socket, 28-pin, DIP	528-AG11D	AUG	2
XA5,6	Socket Assembly, 64-pin Leadless	827-0067-00	INT	2
Y1	Crystal, 14.7456 MHz, Fundamental	CY14B	CRY	1
	Extractor, Card	105UL	CAL	2
	Post, Wire Wrap	89531-6	AMP	91
	Plug, Shorting, 2-Position	530153-2	AMP	15

Table 5-2. List of Manufacturers' Codes

Mfr. Code	Manufacturer	Address
AMP	AMP, Inc.	Harrisburg, PA
AUG	Augat, Inc.	Attleboro, MA
CAL	Calmark Corporation	San Gabriel, CA
CRY	Crystek	Fort Meyers, FL
INT	Intel Corporation	Santa Clara, CA
MOT	Motorola Semiconductor	Phoenix, AZ
SIG	Signetics	Sunnyvale, CA
TI	Texas Instruments	Dallas, TX
OBD	Order by Description; available from any commerical (COML) source	

7 CONN HSG RCPT LOCATIONS

TERMINAL POSTS:
E1 - E2
E27 - E28
E29 - E30
E33 - E34
E36 - E37
E38 - E39
E40 - E41
E43 - E44
E46 - E47
E54 - E55
E65 - E66
E79 - E80
E81 - E82
E83 - E85
E86 - E87

.320 MAX, ALL ITEM 45

SECTION A-A
SCALE: NONE

432/100

COMPONENT SIDE

NOTES UNLESS OTHERWISE SPECIFIED:
1. ASSEMBLY PART NUMBER IS 171958-001.
2. THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS.
3. WORKMANSHIP PER 99-0007-001.
4. MARK PART NUMBER & REV LEVEL WITH CONTRASTING PERM COLOR, NON-CONDUCTIVE, .12 HIGH, APPROX WHERE SHOWN.
5. OBSERVE POLARITY AS INDICATED.
6. FLAT SIDE DENOTES CATHODE LEAD OF LED DS1.
7. INSTALL CONN HSG RCPT, ITEM 55 ACROSS TERMINAL POSTS, ITEM 45 PER "CONN HSG RCPT LOCATIONS" CHART.

REVISIONS

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	PER ECO 17-0020	JP	1-30-81	GFH	2/6/81		2/6/81

PARTS LIST

ITEM NO.	DESCRIPTION
QUANTITY PER DASH NO.	

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES
ANGLES ± 2°
XX ± .010
XXX ± .005

DRN BY J. PLUNKETT 1-30-81
CHK BY GFH 2/6/81
ENGR APVD

intel
3065 BOWERS AVE
SANTA CLARA
CALIF. 95051

TITLE
PRINTED WIRING ASSEMBLY
iSBC 432/100 NEOPHYTE

SIZE D
DOCUMENT NUMBER 171958
REV A
SCALE 1.5/1
SHEET OF 1

Figure 5-1. iSBC 432/100™ Parts Location Diagram

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
ALL	A	PER ECO 17-0020	JP	GH	2-6-81	
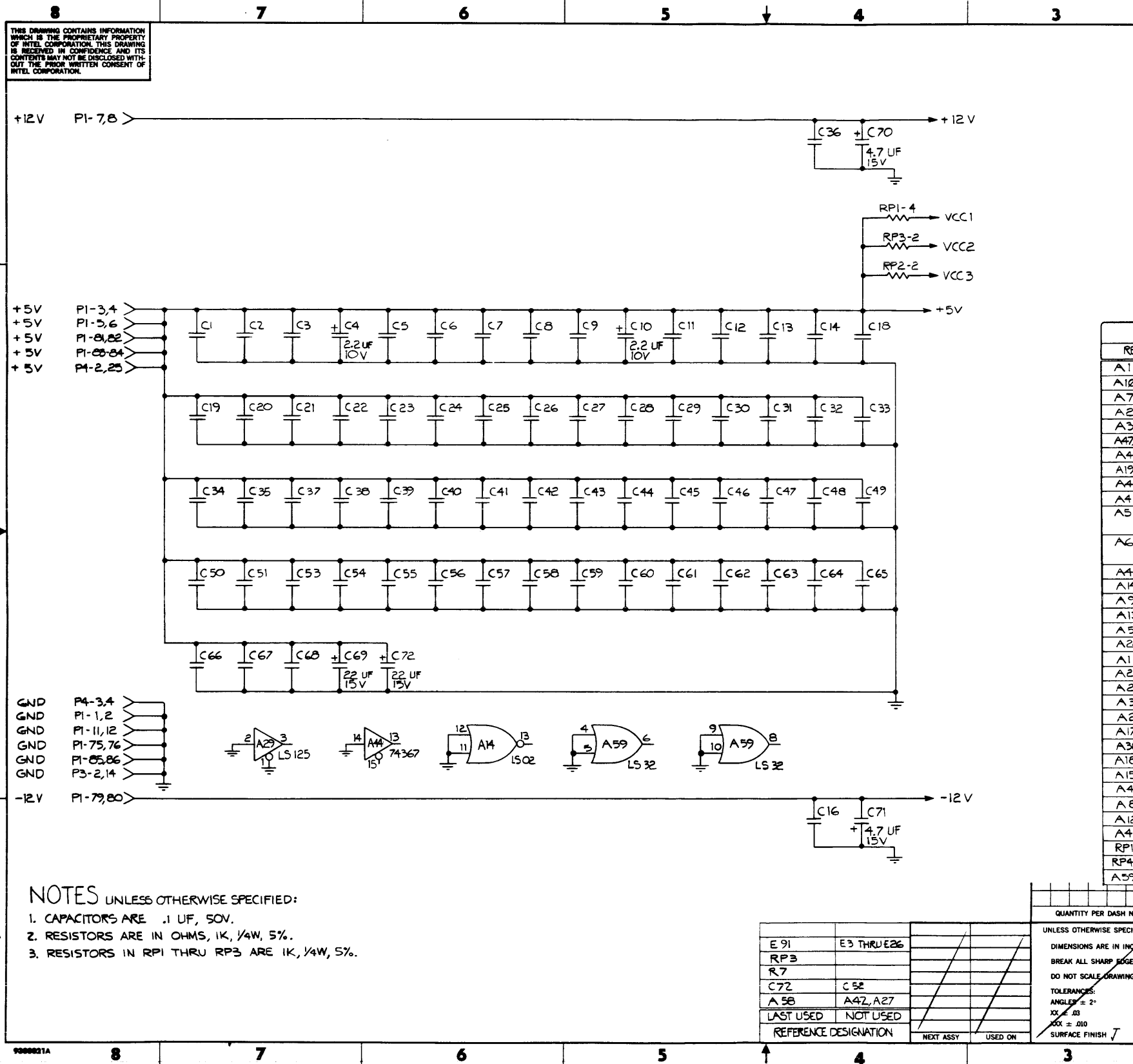
THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITH-OUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

+12V   P1-7,8

+5V   P1-3,4
+5V   P1-5,6
+5V   P1-81,82
+5V   P1-83,84
+5V   P4-2,25

RP1-4 → VCC1
RP3-2 → VCC2
RP2-2 → VCC3

C36 +C70 4.7 UF 15V +12V
+5V

GND P4-3,4
GND P1-1,2
GND P1-11,12
GND P1-75,76
GND P1-85,86
GND P3-2,14

-12V P1-79,80

C16 C71 4.7 UF 15V -12V

C69 22 UF 15V   C72 22 UF 15V

DEVICE TABLE

REFERENCE DESIGNATION	DEVICE TYPE	GND PIN	+5V PIN	+12V PIN	-12V PIN	UNUSED OUTPUT PINS
A11	75188	7		14	1	
A10	75189A	7	14			
A7, A50	8205	8	16			
A21	8251A	4	26			
A36	8253	12	24			
A47, A48, A49, A54	8283	10	20			
A41	8284	9	18			
A19, A20, A51, A52, A53, A55	8287	10	20			
A46	8288	10	20			
A45	8289	10	20			
A5	8801					
A6	8802					
A4, A39	74S00	7	14			
A14	74LS02	7	14			A14-13
A9, A35	74LS04	7	14			
A13	74S08	7	14			
A56, A58	74LS10	7	14			
A28, A40	74S32	7	14			
A1, A30	74S74	7	14			
A22, A23, A26	74LS74	7	14			
A29	74LS125	7	14			A29-3
A37	74S139	8	16			
A2, A3	74S140	7	14			
A17, A31, A32, A33, A34, A57	74LS163	8	16			
A38	74LS175	8	16			
A18, A24, A25	74LS273	10	20			A25-19
A15, A16	74LS283	8	16			
A44	74367	8	16			A44-13
A8	82S100	14	28			
A12	K1100A	7	14			
A43	74LS164	7	14			
RP1, RP2, RP3	R-PAK		1			RP1-2
RP4	R-PAK	1	8			
A59	74LS32	7	14			A59-6,8

A29 LS125   A44 74367   A14 LS02   A59 LS32   A59 LS32

NOTES UNLESS OTHERWISE SPECIFIED:
1. CAPACITORS ARE .1 UF, 50V.
2. RESISTORS ARE IN OHMS, 1K, 1/4W, 5%.
3. RESISTORS IN RP1 THRU RP3 ARE 1K, 1/4W, 5%.

E 91	E3 THRU E26	
RP3		
R7		
C72	C 52	
A 58	A42, A27	
LAST USED	NOT USED	
REFERENCE DESIGNATION		

PARTS LIST

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
BREAK ALL SHARP EDGES.
DO NOT SCALE DRAWING.
TOLERANCES:
ANGLES ± 2°
.XX ± .03
.XXX ± .010
SURFACE FINISH

DRN BY J PLUNKETT 2-5-81

intel
3065 BOWERS AVE.
SANTA CLARA, CALIF. 95051

TITLE: LOGIC DIAGRAM, PWA iSBC 432/100

SIZE D CODE DWG. NO. 171959 REV A

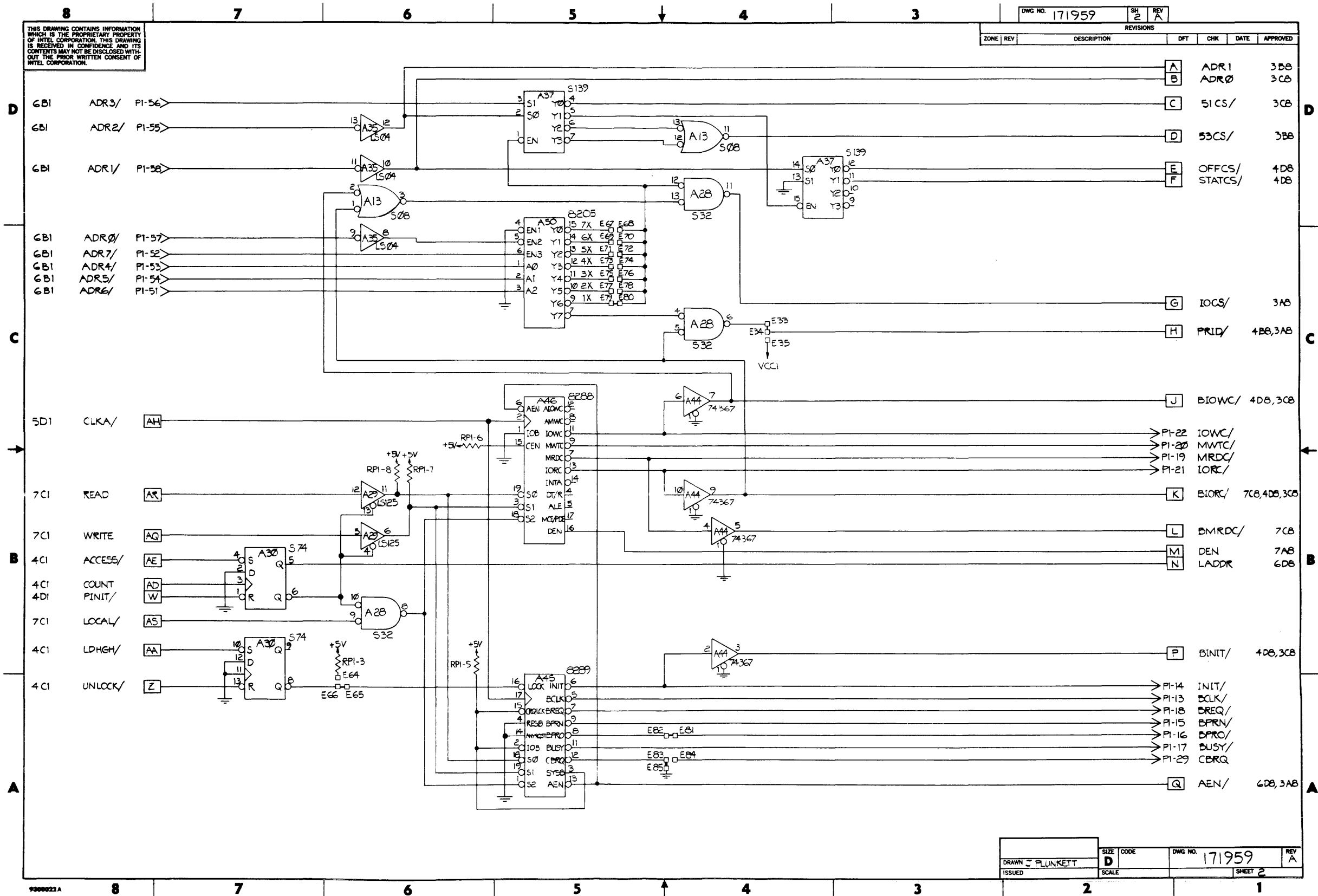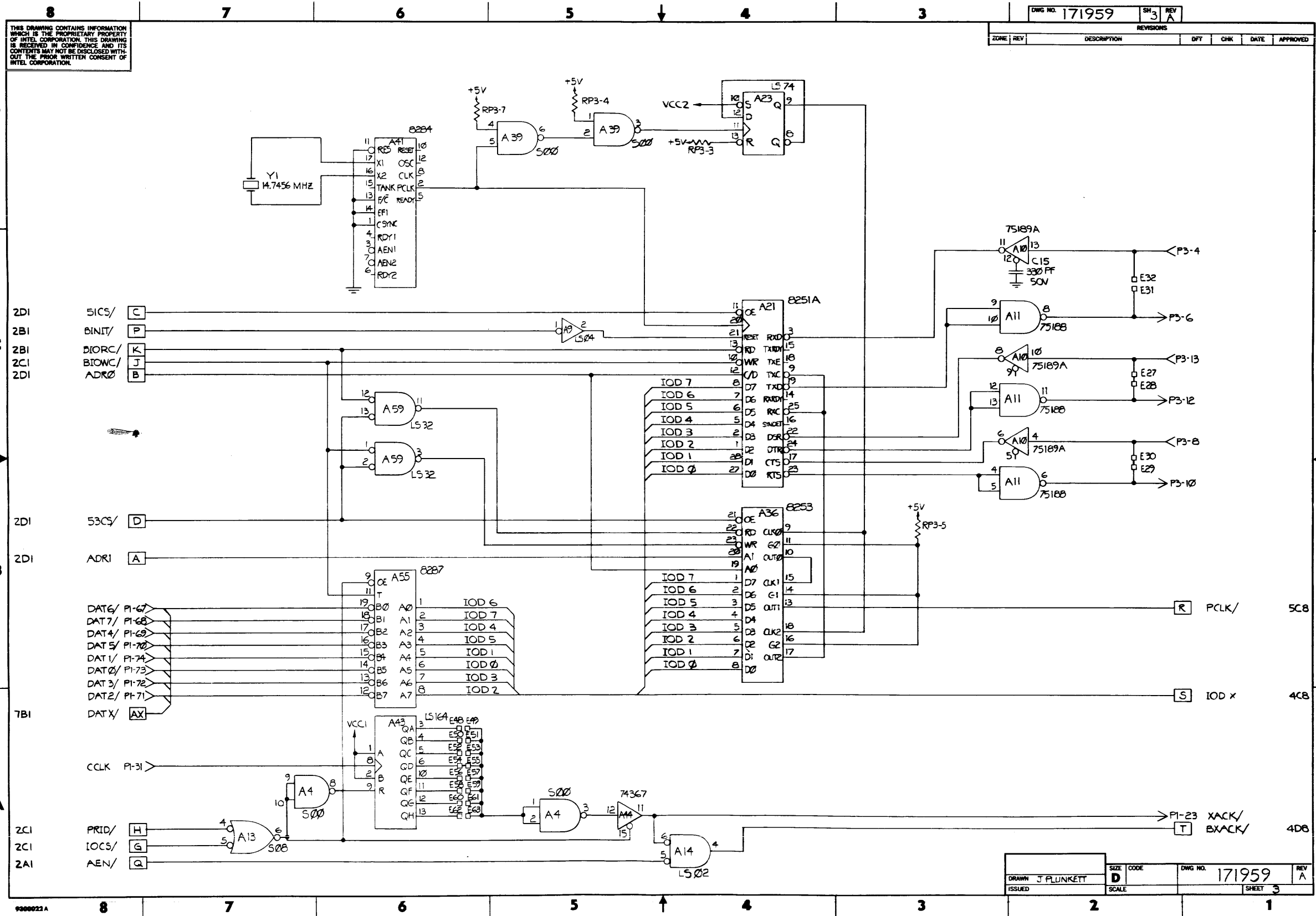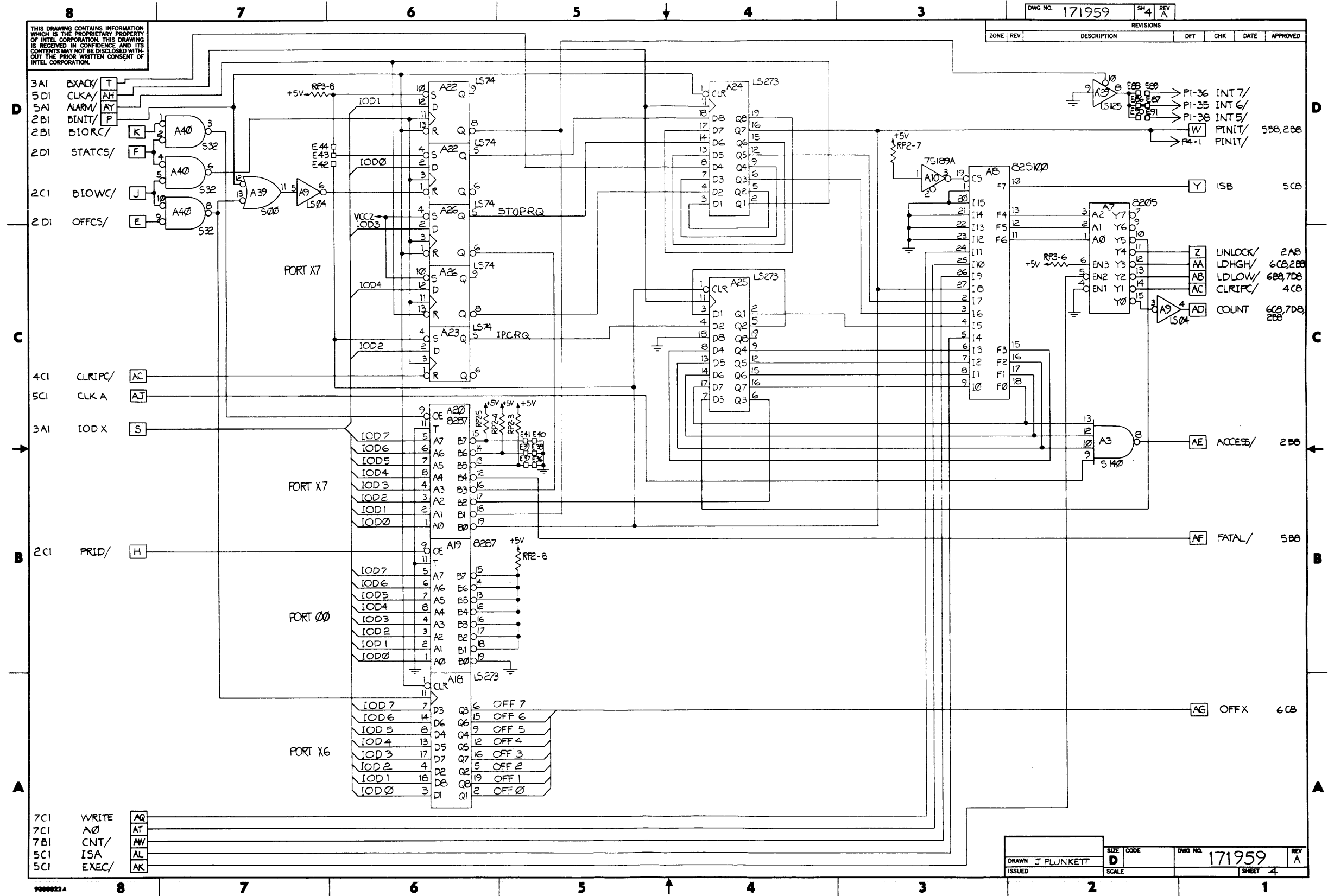SHEET 1 OF 7

Figure 5-2. Schematic Diagram

Figure 5-2. Schematic Diagram (Cont'd.)

Figure 5-2. Schematic Diagram (Cont'd.)
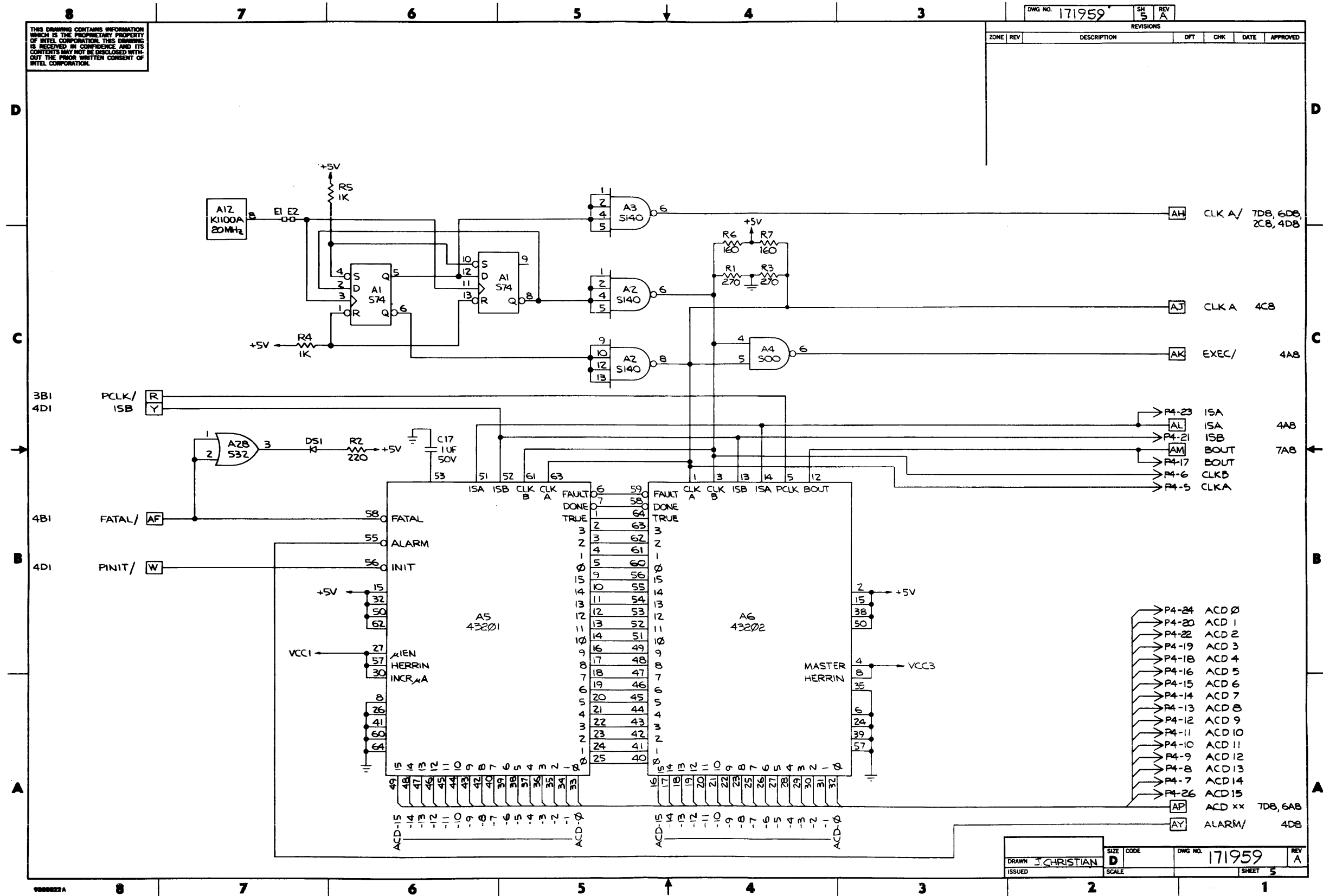
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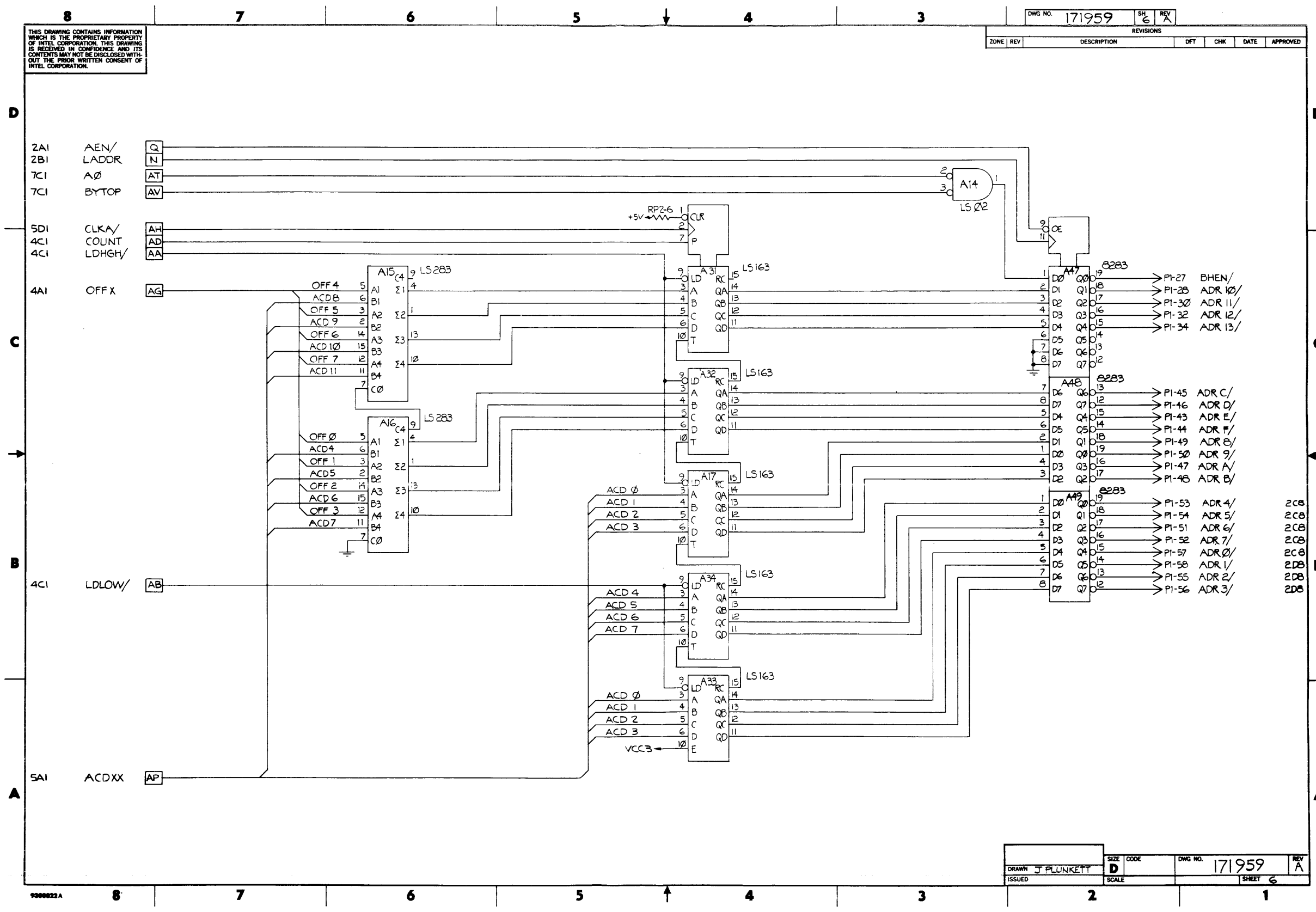
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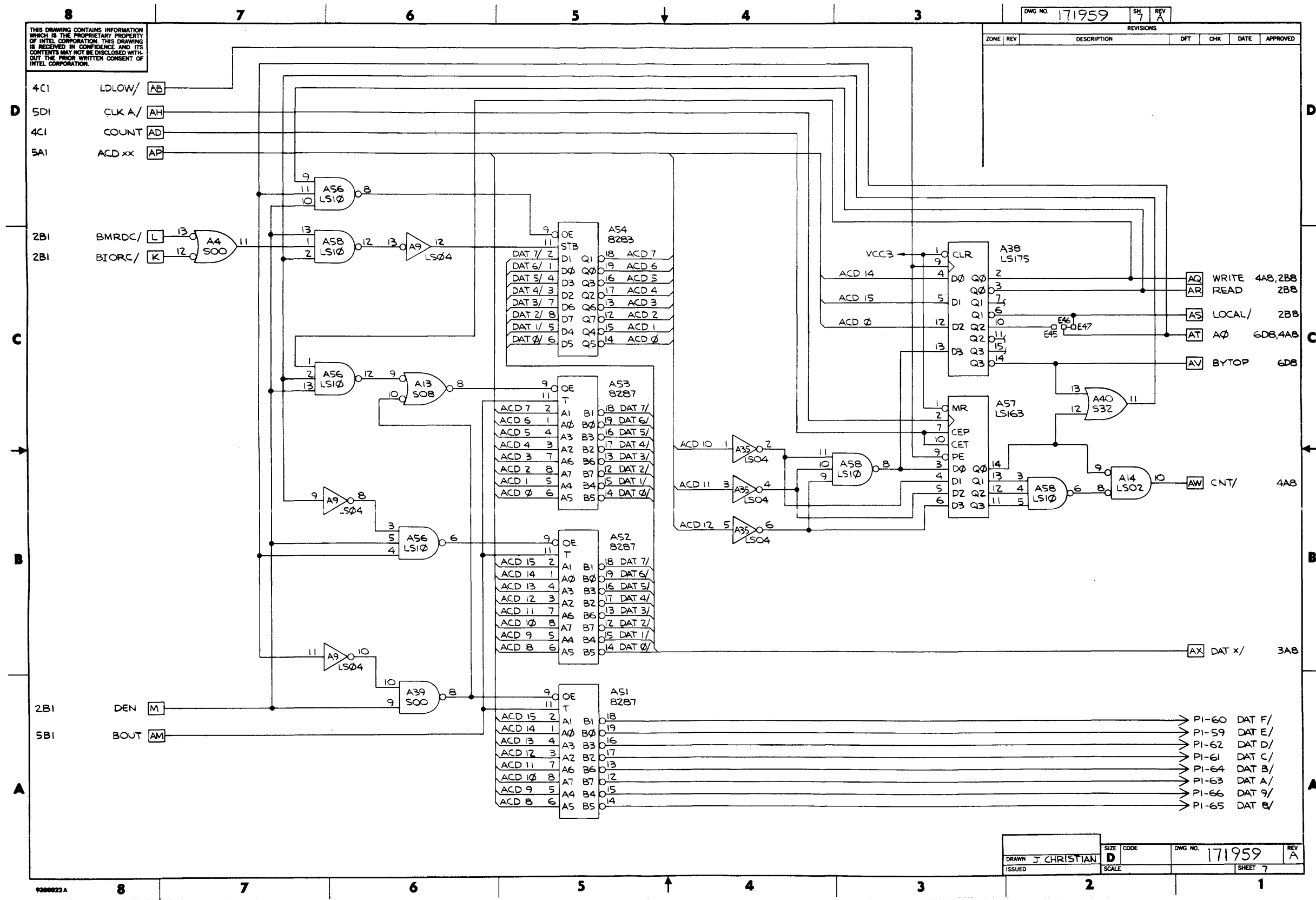
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Figure 5-2. Schematic Diagram (Cont'd.)

Figure 5-2. Schematic Diagram (Cont'd.)

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