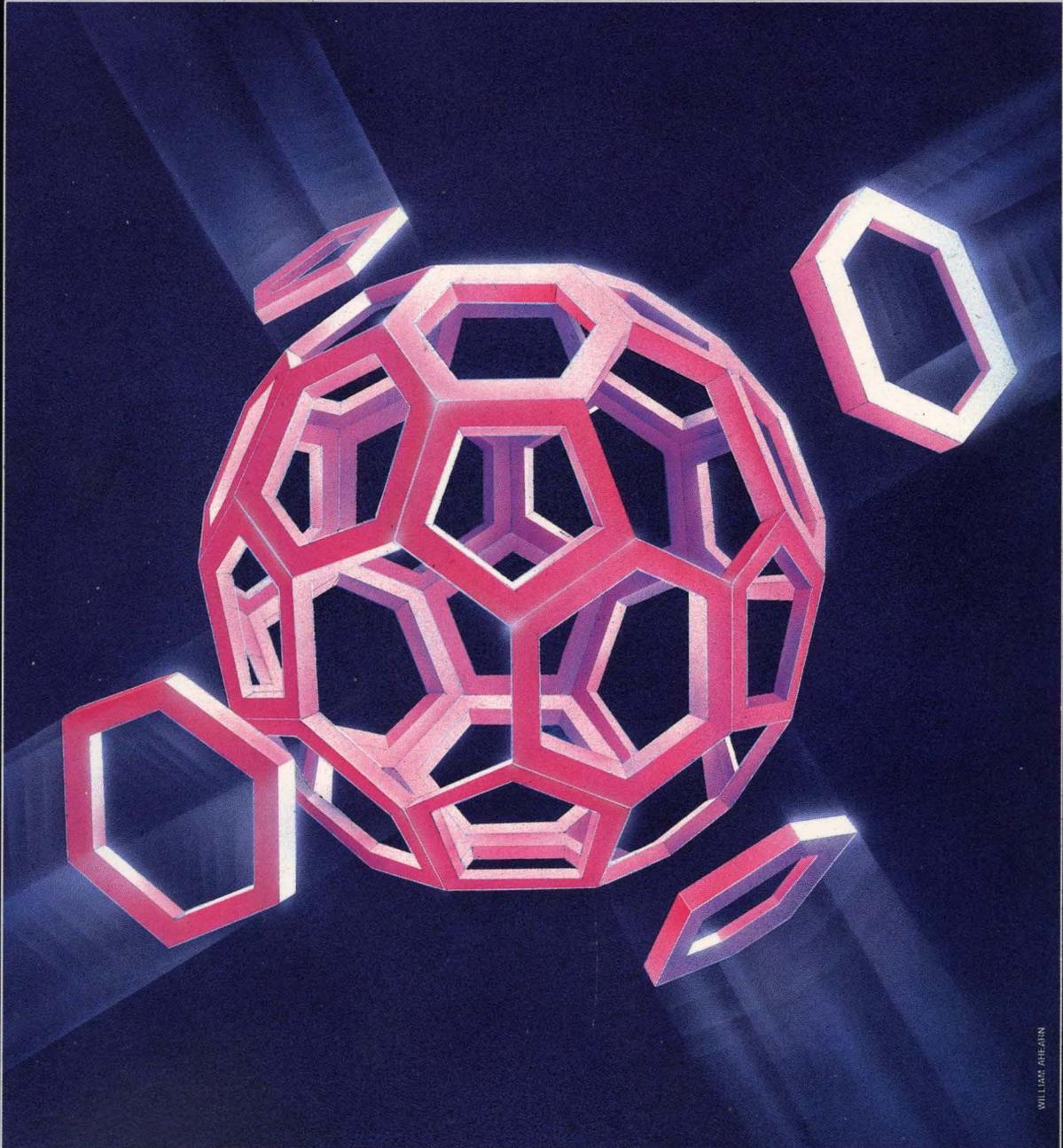


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CHMOS Components Handbook

CHMOS Components Handbook



WILLIAM AHEARN

1985

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CHMOS COMPONENTS HANDBOOK

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INTRODUCTION

This handbook introduces products on a new generation of VLSI semiconductor technology from Intel. CHMOS (Complementary High-performance Metal Oxide Semiconductor) combines the best processing techniques used on Intel's high performance HMOS processes with a new set of performance-oriented design rules. CHMOS improves the industry's best speed-power performance to achieve high-speed products with an order of magnitude less power usage. Additionally, on some products (like the new series of CHMOS Random Access Memories), CHMOS is utilized to attain higher speed versions than previously available.

These CHMOS product specifications are brought together to give designers a common reference for information on Intel's complete VLSI CHMOS product line. Represented are components from the microprocessor, peripheral, microcontroller, telecommunication, non-volatile memory, and volatile memory areas. In each case, optimized CHMOS versions of industry-standard architectures are included. This complete set of CHMOS products enables designers to utilize their software and hardware expertise gained with HMOS and quickly take advantage of CHMOS benefits for their systems.

USING THIS HANDBOOK:

Primarily, this book contains a compilation of Intel's CHMOS data sheets organized by product type.

Each data sheet highlights those aspects of each product which the designer will find most useful. Complete parametric specifications follow the product descriptions.

A summary of Intel's unique approach to building CHMOS product line has been inserted at the outset. The opening chapter discusses the key issues addressed in designing CHMOS — namely latchup prevention, soft-error prevention, interconnections, and logic design techniques. The approach used to resolve these issues and create a complete set of VLSI components is then outlined.

This handbook should be used in combination with other Intel design aids. Additional specifications, application materials, design support tools, or instructional classes are available to supplement design efforts. These items can be obtained from your local Intel representative.

ABOUT THE FUTURE:

Specifications of Intel's initial CHMOS products are contained in this handbook. More VLSI CHMOS components will be added as Intel continues to improve its technologies, the products they make up, and ultimately the systems they go into. With these new products will come an expanding set of documentation to keep designers abreast of advanced semiconductor capabilities and their applications.

CHMOS Technology Overview

Modular approach to C-MOS technology tailors process to application

Despite the proliferation of applications, a few C-MOS process variations can address the functional requirements of many different products

by Kim Kokkonen and Richard Pashley, *Intel Corp., Santa Clara, Calif.*

□ In the past few years, the interest in complementary-MOS technology and its applications to new products has exploded. Traditional arguments for C-MOS center on its low power dissipation, the large noise margins of complementary logic, and its simple ratioless design. With the advent of very large-scale integration, these arguments are taking on new meaning and importance.

As an example, Fig. 1 compares the performance of H-MOS (high-performance n-channel MOS) inverters with their equivalent in Intel's C-H-MOS (complementary high-performance MOS) technology. Though H-MOS's speed continues to improve with further scaling, its delay-power product is more than an order of magnitude higher than a C-H-MOS implementation with identical n-channel transistors. In a VLSI part with 50,000 gates, C-H-MOS could mean the difference between 1 and 10 watts of power dissipation, which might save the expense and difficulty of a sophisticated cooling system or extend a portable system's operating time by a factor of 10.

That C-MOS performance is now on a par with n-MOS technology has also accelerated its popularity. In addition, the density of C-MOS circuitry has improved dramatically with advances in technology. Finally, the number of process alternatives has grown so large that almost any integrated-circuit design can be supported with available C-MOS technology.

Unfortunately, the wave of enthusiasm for C-MOS and the needs of different applications have multiplied the number of approaches that C-MOS developers are taking. Several major issues remain in VLSI C-MOS design—namely latchup and soft-error prevention, interconnections, and logic-design techniques. A building-block approach with a limited number of basic process modules can be used to create a close-knit family of technologies that squarely addresses these issues and simultaneously supports a wide range of applications.

The basis for C-H-MOS

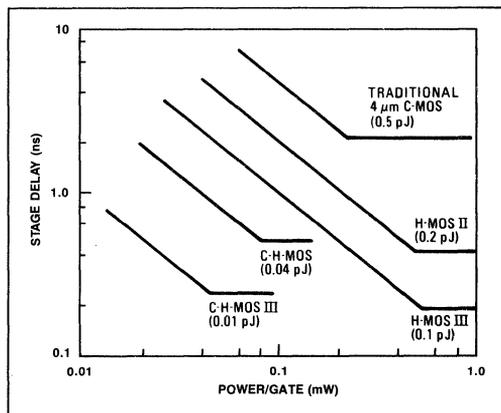
A firm foundation in n-MOS-transistor physics will support the advancement of C-MOS technology. As channel lengths approach 1 micrometer, n-channel transistors become more difficult to optimize because the standard 5-volt power supply causes problems with high-intensity fields. Improperly designed transistors may be unreliable as a result of hot-carrier injection into gate oxides, or they may cause less localized problems by injecting carri-

ers into the MOS substrate—there to bleed charge from storage nodes or even trigger a destructive latchup.

The resources to develop and verify the reliability of a 1- μm n-channel transistor are well established and substantial. In Intel's C-H-MOS process, the basic design of the n-channel transistor is identical to its H-MOS counterpart, as shown in the table. Even at the more detailed levels of doping profiles, the H-MOS and C-H-MOS transistors are nearly identical.

Thus a high-performance C-MOS technology may be born out of an established n-MOS line. The relatively simple addition of an n-well in the same high-resistivity substrate results in a C-MOS process that serves as the basis for several optimized technologies. This is just a start, however, as other important issues remain.

Latchup has been the traditional nemesis of C-MOS. Given the presence of parasitic silicon controlled rectifiers within every bulk C-MOS chip, a current pulse of sufficient magnitude either inside or outside the chip may cause a catastrophic latchup. Many schemes have been proposed to combat latchup, ranging from carefully scrutinizing the layout (which imposes no burden on the technology) to a buried layer (which significantly in-



1. Power down. Despite the continuous improvement of H-MOS (high-performance MOS) by scaling, the delay-power product for C-H-MOS (complementary-MOS H-MOS) is more than an order of magnitude lower in the typical integrated circuit.

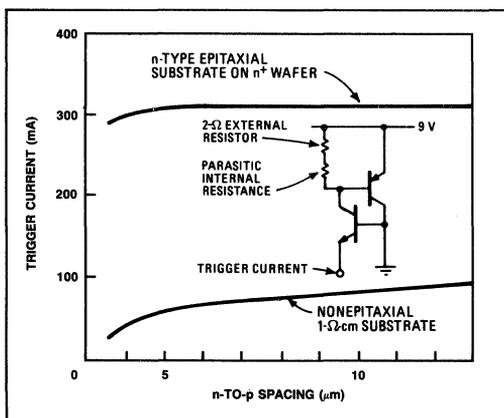
n-CHANNEL TRANSISTOR COMPARISON					
Technology		Gate-oxide thickness (Å)	Channel length (μm)	Threshold voltage (V)	Graded drain profile
n-MOS	C-MOS				
H-MOS I	—	700	3.0	0.7	no
H-MOS II	C-H-MOS	400	2.0	0.7	no
H-MOS II	C-H-MOS III	250	1.0	0.7	yes

increases complexity and processing cost). All have some degree of effectiveness.

A modular approach to a broad-based line of C-MOS technologies requires other measures besides mere physical latchup resistance. The latchup spoiler must be applicable to dynamic random-access memories, erasable programmable read-only memories, and static RAMs, as well as to microprocessors and controllers. In order to improve latchup resistance, it cannot increase the distance between n- and p-channel transistors (this constraint is most significant in random logic and full C-MOS six-transistor static-RAM cells). The technique must be compatible with low-cost and large-volume manufacturing. Finally, the approach must be consistent with the use of an automated checking algorithm, so that every gate of a large semirandom logic design need not be scrutinized for latchup susceptibility.

Epitaxial benefits

Figure 2 shows the margin gained in latchup trigger current when an epitaxial substrate is used. The epitaxial substrate brings the same latchup benefits to all product lines, and in many cases provides additional advantages such as improved surface lifetimes (for dynamic RAMs) and reduced dc resistance (for E-PROMs and logic). Epitaxial substrates are now available in volume from commercial silicon vendors, adding less than 5% to the cost of a finished wafer. No additional or exotic fabrication equipment needs to be installed. Because the epitaxial



2. Benefits. By raising the margin of latchup trigger current, an epitaxial substrate effects a dramatic improvement in combatting latchup, a major concern in complementary-MOS chip design.

substrate's heavily doped bulk effectively eliminates the vertically triggered latchup mode, it is possible to develop a set of computer-aided-design tools that can flag latchup-sensitive layouts on the largest VLSI chips.

Since grasping the phenomenon of upsets induced by alpha particles, in 1977, memory designers have taken care to ensure that enough charge is stored within each cell to minimize

the problem. As critical chip dimensions are reduced, this problem becomes more severe, however, since both parasitic and storage capacitances are naturally reduced. For the latest 1.5-μm n-MOS process, stored charge is low enough to caution even microprocessor designers to guard against random storage nodes suffering from soft errors. Fortunately, C-MOS provides a natural barrier against soft errors if the storage node is located within the C-MOS well.

The well junction is reverse-biased by the power-supply voltage. The electric field at this junction naturally repels any carriers generated outside the well that might otherwise diffuse up to surface storage nodes. The combination of the well structure and an epitaxial substrate is even more effective. Here the funneling mechanism that usually collapses local electric fields during the passage of an alpha particle is also minimized. By using epitaxial substrates and the protection of a C-MOS well, the amount of charge collected during an alpha event can be reduced by an order of magnitude.

Of course, the designer must arrange for the storage node to reside within the well. This constraint, combined with other performance issues, leads to different choices of well and substrate polarities, depending on application. For example, in a C-MOS technology that is optimized for dynamic RAM, the ideal memory cell should have a p-channel pass gate and a p-channel capacitor located within an n-well in a p-type substrate. The p-channel transistor is chosen because it injects far fewer spurious carriers into the substrate and thus does not by itself disturb the state of neighboring cells.

The conductance of the p-channel device, while lower than that of an n-channel device of the same size, does not degrade the RAM's performance, since dynamic-RAM sensing is limited primarily by the amount of stored charge. Experimental results with C-H-MOS dynamic RAMs based on these principles show a soft-error rate of less than 300 FIT (failures in time, or device failures per billion hours) at a power supply of only 3 V. This is an improvement of more than three orders of magnitude over traditional n-MOS dynamic-RAM technology and offers the possibility of dynamic-RAM systems that require no error correction and that are compatible with low-voltage battery backup.

High-density, high-performance static RAMs present the other side of the coin. The smallest static-RAM cells today are built using polysilicon-load resistors that sustain the stored-node voltage. On the time scale of an alpha event, however, these resistors in effect do not exist. Because the storage node's RC time constant is on the order of milliseconds and the alpha event's time scale

is nanoseconds, the cell appears dynamic. In this sense, polysilicon-load static-RAM cells are very similar to dynamic-RAM cells. The major difference arises in the way the cells sense the cell's information. The static-RAM cell provides a direct current, and to maximize the cell's performance, that current must be as large as possible while contained in a minimum area. Thus the chip designer must use high-gain n-channel transistors for the cell's pass gates and pulldowns. For good soft-error protection, then, the cell must be located in a p-well within an n-type substrate.

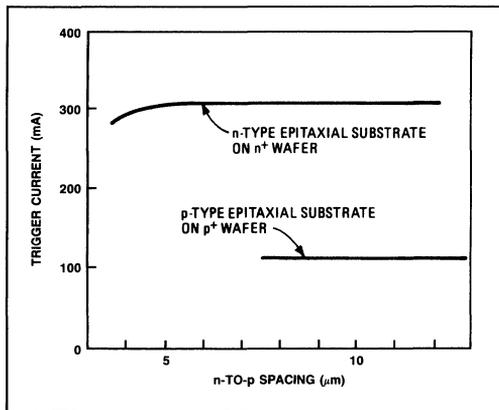
The p-well approach benefits even full C-MOS six-transistor static-RAM cells. The area of such cells depends strongly on the distance allowed between n- and p-channel devices. Using a straightforward implementation of epitaxial C-MOS, the p-well approach provides more margin against latchup at small n-to-p spacings (Fig. 3). This phenomenon occurs because of the differing diffusion properties of n- and p-type dopants. The heavy doping in the n-type substrate is less mobile than is the p-type dopant, resulting in less outdiffusion during thermal processing and thus minimizing the shunt resistance that controls latchup.

Hooking it up

One of the challenges of C-MOS in logic applications is interconnection. Designers of n-MOS chips are accustomed to buried contacts, which directly connect n-type polysilicon and n-type transistor source or drain regions. Because C-MOS requires contact to both p and n regions, the traditional n-type buried contact becomes much less useful, and a version suitable for both diffusion polarities is quite difficult to implement. This increases the burden on contact and metallization modules.

For high-density C-MOS logic, the first level of metal is all but consumed by local connections between p and n transistors. The payback from adding a second level of metal for longer-distance routing is very high. A good example exists for the six-transistor static-RAM cell commonly used by logic designers. Figure 4 compares single- and double-metal versions of this cell, both implemented with 1.5- μm design rules. Here the second-metal layer provides the bit lines for the cell. Similar arguments justify the use of second metal in global power, clock, and data routing in complex microprocessor chips.

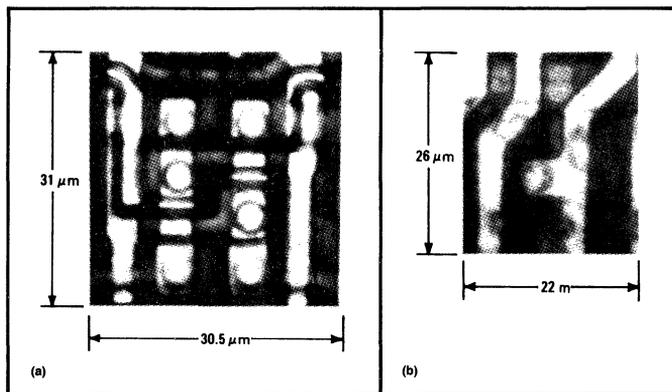
Contacts themselves are more difficult to build in C-MOS. N-MOS technology accustomed process engineers to adding a phosphorus contact plug after the contacts have been etched. This plug brought several advantages: the phosphorus gettered metallic contaminants from the wafer, reducing junction leakage; and the high-temperature diffusion rounded the profile of the contact sidewall, easing the step coverage of the metal subsequently deposited. Further, the plug had self-aligning features. If the



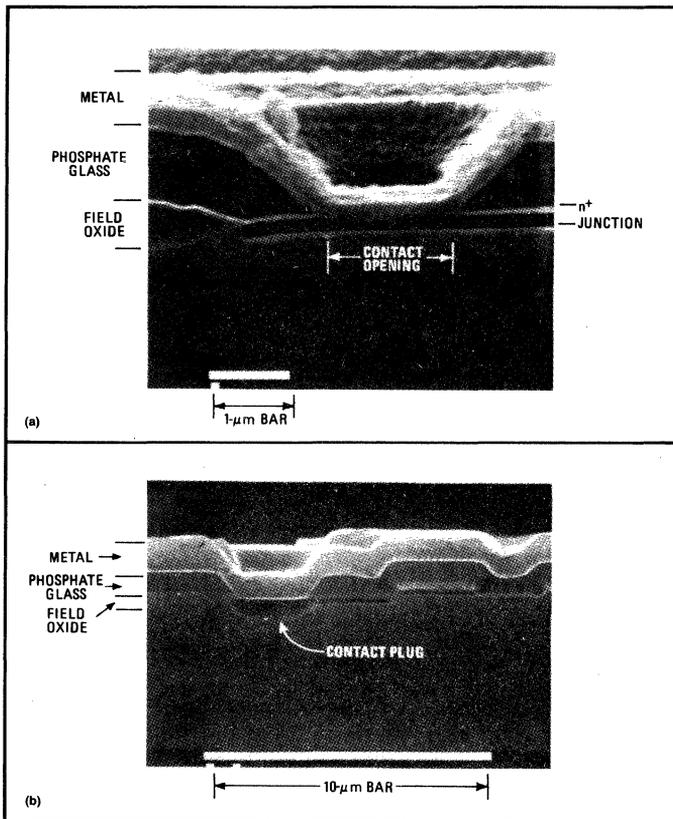
3. P-well margin. With an epitaxial substrate, a p-well structure (upper curve) yields a greater margin against latchup than n-well at smaller n- and p-device spacings.

contact etch attacked the silicon substrate or if the contact was misaligned toward the field-oxide edge, the plug would rejuvenate the resulting weakened junctions. In C-MOS, these same attributes must be obtained differently, through improved fabrication, cleanliness, new gettering techniques, improved dielectrics, and tightly controlled contact etching. Figure 5 shows the difference in implementing a 1.5- μm contact structure in n-MOS and C-MOS.

Along with the proliferation of C-MOS technologies has come a wave of innovation in C-MOS design techniques. For digital logic, the major contenders for broad use are full complementary design and domino logic, first proposed by AT&T Bell Laboratories (Fig. 6). For many applications, traditional C-MOS logic is a winner. It requires no clocks, has larger operating margins, and uses fewer transistors for simple gates. For more complex gates, however, domino logic uses fewer transistors and runs faster. The speed results from connecting fewer transistors in series and reducing gate-fanout loading by



4. Payback. The use of double-metal layers for a six-transistor static-RAM cell can produce a large savings in real-estate. In two cells implemented with a 1.5- μm design rules, the savings can amount to one third of the total area. The cell at right uses second-layer metal for bit lines.



5. Making contact. Contacts are more difficult to build in C-MOS than in conventional n-MOS. The phosphorous contact plug used in n-MOS after contact etching (a) adds desirable features such as reduced junction leakage and improved step coverage by the metal layer. To gain the same advantages in C-MOS requires greater process control (b).

and p-well construction show that the p-channel's conductance may be improved by as much as 10% with the proper well type.

By contrast, domino logic is at its best in an n-well technology. Here, the n-channel transistor dominates both performance and transistor count. Placing the n-channel device outside the well improves its conductance and reduces the dominant parasitic junction capacitance. Density also increases because no well contacts are required for the majority of the transistors.

The twin-well approach to C-MOS blurs these distinctions. In this approach, a high-resistivity epitaxial layer is grown on a heavily doped starting wafer. Then the doping for each transistor polarity may be independently optimized without need for doping compensation. Performance arguments based on mobility or junction capacitance thus become moot. Nonetheless, domino logic will still be best on a p-type substrate (equivalent to n-well) because it does

up to a factor of two compared with full C-MOS.

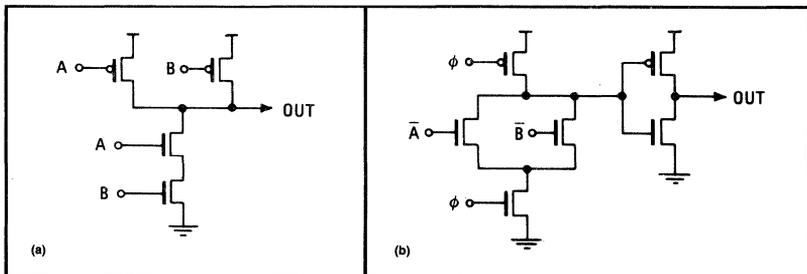
Interestingly, the choice of design style influences the optimal type of C-MOS well. The speed of full C-MOS is limited by the slower of the two transistor polarities. Since the trip point is quite close to half the power supply, the time required for either transistor type to discharge its load capacitance by about 2.5 V sets the gate's speed. Since the p-channel device is the weaker one, it pays to choose a well type that improves the p-channel's conductance. P-well does this because the p-device is fabricated in an uncompensated substrate and thus has maximum mobility. Comparisons between n-

not require well contacts to collect the large parasitic substrate currents from the n-channel transistors, thus improving packing density.

Matching process to product

These and other technical arguments may be combined into a consistent strategy (Fig. 7) for creating a line of C-MOS processes serving a broad marketplace. For at least the next several years, a complete technology line must include C-MOS based on both p- and n-type substrates. Fortunately, choosing epitaxial-latchup control minimizes the development cost of running both process-

6. Logic. Two major contenders for digital logic design are full complementary (a) and domino logic (b). The former requires no clocks and is simpler for many applications. Domino logic, which performs best in an n-well technology, is faster and simpler for more complex circuits.



es. Dynamic RAMs are supported on the n-well side to minimize pattern sensitivities induced by substrate currents while protecting the p-channel cell from soft errors. E-PROMs are built in a similar n-well C-H-MOS process. Placing Intel's n-MOS E-PROM cell in an epitaxial p-type substrate eliminates parasitic effects caused by high substrate currents flowing during cell programming.

Microcontrollers land on the n-well side also, so that they may incorporate on-chip E-PROM cells. Most microcontroller products come in two versions, one with on-chip E-PROM for system-development and manufacturing flexibility, and another with on-chip ROM for lowest cost. Using n-well C-MOS, a single core design can support both versions. Telecommunications and signal-processing products can also take advantage of the n-well E-PROM process, both for its high-quality polysilicon-polysilicon capacitors and for the E-PROM cell's programmable features. High-performance static RAMs, whether six-transistor or polysilicon-load, can take advantage of a p-well C-H-MOS process. High-end microprocessors can key off the dense n-to-p packing and double-metal capability offered by the six-transistor static-RAM process.

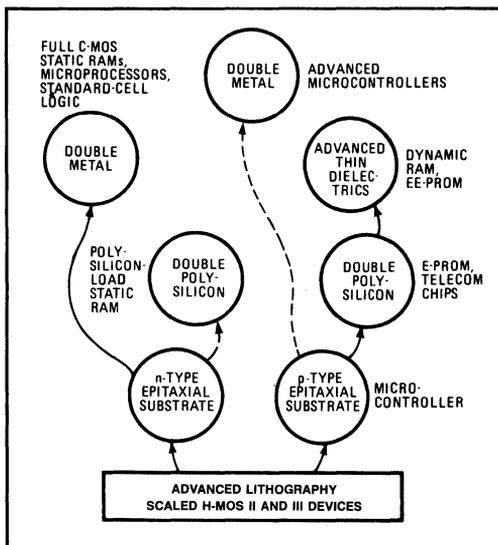
Because these processes are modular, development is simplified and manufacturing overhead is minimized. Just as all the 1.5- μm C-H-MOS III technologies share a common transistor module, the difficult contact module was developed once to be shared among all. Specialized features such as double polysilicon or double metal are extensions of the common base.

The future

C-MOS technology is still developing at a frenetic pace. Surprisingly, the application of some newer techniques and the demands of next-generation circuits may bring the various forms of C-MOS closer together, rather than further splitting the number of integrated processes.

One example of this trend is the development of a trench-isolation technique for separating n and p devices. When this module is perfected, there will be no reason to develop six-transistor static-RAM cells on p-well technology. The near-ideal trench isolation will prevent latchup on either substrate type. Similarly, if stacked C-MOS static-RAM cells can be perfected, there will be no need for polysilicon loads. The stacked C-MOS cell will have the same density but with improved performance and soft-error immunity. At that time, twin-well C-MOS on a p-type substrate, augmented by specialized features for specific product lines, will become the one approach to a broad line of C-MOS processes.

Another factor affecting future C-MOS integration is the continued scaling of transistors. It is well known that the weaker p-channel transistor is gradually catching up on the n-channel device as channel lengths enter the submicrometer region. Eventually, the performance differences may become so small that p- and n-channel devices will be used interchangeably. Before this level is reached, however, the 5-v power-supply standard must be reduced. Because of the large base of TTL-compatible designs and the impossibility of converting the world to a new standard overnight, components operating from the new reduced supply will need to maintain TTL compatibility and also be able to operate in a system that mixes



7. Technology tree. A relatively small line of C-MOS process variations, or modules, can be matched to a wide variety of products to serve a broad marketplace. The broken lines indicate directions of potential future growth.

older 5-v components with lower-voltage ones. An on-chip 5-to-3-v converter may be one way to solve the problem. This technique, however, will waste up to 40% of the total chip power within the voltage regulator.

C-MOS technology provides an elegant solution because it can drive TTL-compatible output levels from a system power supply as low as 3 v. Since TTL levels are referenced to the negative (ground) rail, the grounded substrate offered by n-well C-MOS is a much-preferred means of integrating submicrometer transistors into such a system. This will be a strong motive to standardize on p-substrate C-MOS.

A final factor that tends to drive future C-MOS processes toward commonality is the growing importance of RC delays in overall chip performance. The latest high-performance static RAMs use an aluminum strap in parallel with the polysilicon word line because the RC delay induced by even the best refractory metal polyicides is several nanoseconds too long. Studies of dynamic RAMs larger than 1 megabit similarly indicate that refractory word lines will probably be inadequate, forcing the technology to support two layers of metal. Combining these observations with those made previously regarding the evolution of static-RAM cells leads to the conclusion that most future C-MOS technologies will have two layers of polysilicon as well as two layers of metal.

The development of silicon-on-insulator technology is the one major factor that could renew the divergence of C-MOS approaches in the future. However, until the quality of SOI substrates is adequate to support dynamic RAM and E-PROM cells, and not just static logic, it will not play a major role in a broad-based and modular technology strategy. □

51C64H HIGH PERFORMANCE RIPPLEMODE™ 64K X 1 CHMOS DYNAMIC RAM

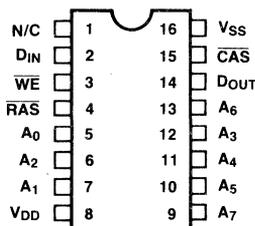
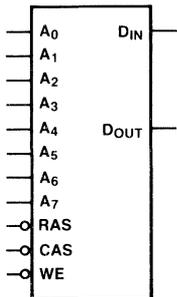
	51C64H-8	51C64H-10	51C64H-12
Maximum Access Time (ns)	80	100	120
Maximum Column Address Access Time (ns)	45	55	65
Ripplemode Cycle Time (ns)	55	65	75

- **Ripplemode Operation**
 - Continuous data rate over 18 MHz
 - Random access within a row
 - Flow through column latch for pipelining
- **Low Operating Current — 45 mA**
- **Low Input/Output Capacitance**
- **Fast “Usable Speed”**
 - $t_{RC} = 140$ ns
 - $t_{CAC} = 20$ ns
 - $t_{RCD} = 30$ ns min./60 max.
- **Fully TTL Compatible**
- **High Reliability Plastic — 16 Pin DIP**

The Intel® 51C64H is a high speed 65,536 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C64H offers features not provided by an NMOS dynamic RAM: Ripplemode for high data bandwidth and fast usable speed. All inputs and outputs are fully TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

Ripplemode operation allows random or sequential access of up to 256 bits within a row, with cycle times as fast as 55 ns. Because of static column circuitry, the \overline{CAS} clock is no longer in the critical timing path. The flow through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the 51C64H ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance microprocessor systems.

LOGIC SYMBOL PIN CONFIGURATION PIN NAMES



\overline{RAS}	ROW ADDRESS STROBE
\overline{CAS}	COLUMN ADDRESS STROBE
\overline{WE}	WRITE ENABLE
A ₀ -A ₇	ADDRESS INPUTS
D _{IN}	DATA IN
D _{OUT}	DATA OUT
V _{DD}	POWER (+ 5V)
V _{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias	-10°C to +80°C
Storage Temperature	Plastic -55 to +125°C
Voltage on Any Pin except V _{DD} and D _{OUT} Relative to V _{SS}	-2.0V to 7.5V
Voltage on V _{DD} Relative to V _{SS} ...	-1.0V to 7.5V
Voltage on D _{OUT} Relative to V _{SS}	-2.0V to V _{DD} + 1V
Data Out Current	50 mA
Power Dissipation	1.0W

†COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above or below those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C64H			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating		33	45	mA	t _{RC} = t _{RC} (min), for - 8 specification	3,4
			27	37	mA	t _{RC} = t _{RC} (min), for - 10 specification	
			23	35	mA	t _{RC} = t _{RC} (min), for - 12 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby			4	mA	\overline{RAS} and \overline{CAS} at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, TTL \overline{RAS} -Only Refresh		28	45	mA	t _{RC} = t _{RC} (min), for - 8 specification	4
			24	37	mA	t _{RC} = t _{RC} (min), for - 10 specification	
			20	35	mA	t _{RC} = t _{RC} (min), for - 12 specification	
I _{DD4}	V _{DD} Supply Current, Ripplemode™		20	45	mA	t _{PC} = t _{PC} (min), for - 8 specification	3,4
			18	37	mA	t _{PC} = t _{PC} (min), for - 10 specification	
			17	35	mA	t _{PC} = t _{PC} (min), for - 12 specification	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled		3	6	mA	\overline{RAS} at V _{IH} , \overline{CAS} at V _{IL} , all other inputs and output ≥ V _{SS}	3
I _{LI}	Input Load Current (any pin)			10	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current for High Impedance State			10	μA	\overline{RAS} and \overline{CAS} at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	6
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -5 mA	6

NOTES:

- All voltages referenced to V_{SS}.
- Typical values are at T_A = 25°C and V_{DD} = +5V.
- I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
- I_{DD} is dependent upon the number of address transitions while \overline{CAS} is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Ripplemode.
- Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
- Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†
 $T_A = 25^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Address, D_{IN}	3	4	pF
C_{IN2}	\overline{RAS} , \overline{CAS} , \overline{WE}	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

A.C. CHARACTERISTICS 1,2,3
 $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C64H-8		51C64H-10		51C64H-12		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	\overline{RAS} Pulse Width	80	75000	100	75000	120	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	140		160		190		ns	
3	t_{RH2RL2}	t_{RP}	\overline{RAS} Precharge Time	50		50		60		ns	
4	t_{RL1CH1}	t_{CSH}	\overline{CAS} Hold Time	80		100		120		ns	
5	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
6	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		15		ns	
7	t_{CH2CL2}	t_{CP}	\overline{CAS} Precharge Time	10		10		15		ns	
8	t_{CH2RL2}	t_{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	-20		-20		-20		ns	
9	t_{RL1CL2}	t_{RCD}	\overline{RAS} to \overline{CAS} Delay	30	60	30	80	35	95	ns	4
10	t_{AVCL2}	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10		10		15		ns	
12	t_{RL1AX}	t_{AR}	Column Address Hold Time From \overline{RAS}	40		40		50		ns	
	t_{RVRV}	t_{REF}	Time Between Refresh		4		4		4	ms	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	5
13	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0	20	0	20	0	25	ns	
14	t_{CH2QZ}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	25	ns	

NOTES:

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a \overline{RAS} clock such as \overline{RAS} -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).
- A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, $V_{IL}(\text{min}) \geq V_{SS}$ and $V_{IH}(\text{max}) \leq V_{DD}$.
- $t_{RCD}(\text{max})$ is specified for reference only.
- t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

A.C. CHARACTERISTICS (Con't.)

Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64H-8		51C64H-10		51C64H-12		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
15	t _{RL1QV}	t _{RAC}	Access Time From \overline{RAS}		80		100		120	ns	6
16	t _{CL1QV}	t _{CAC}	Access Time From \overline{CAS}		20		20		25	ns	7,8
17	t _{AVQV}	t _{CAA}	Access Time From Column Address		45		55		65	ns	8,9
18	t _{CL1CH1(R)}	t _{CAS(R)}	\overline{CAS} Pulse Width (Read Cycle)	15	75000	20	75000	25	75000	ns	
19	t _{CL1RH1(R)}	t _{RSH(R)}	\overline{RAS} Hold Time (Read Cycle)	10		10		10		ns	
20	t _{WH2CL2}	t _{RCS}	Read Command Set-up Time	0		0		0		ns	
21	t _{AVRH1}	t _{CAR}	Column Address to \overline{RAS} Set-up Time	45		55		65		ns	
22	t _{CH2WX}	t _{RCH}	Read Com. Hold Time Ref. to \overline{CAS}	0		0		0		ns	10
23	t _{RH2WX}	t _{RRH}	Read Com. Hold Time Ref. to \overline{RAS}	10		10		10		ns	10

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64H-8		51C64H-10		51C64H-12		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
24	t _{CL1RH1(W)}	t _{RSH(W)}	\overline{RAS} Hold Time (Write Cycle)	35		35		40		ns	
25	t _{CL1CH1(W)}	t _{CAS(W)}	\overline{CAS} Pulse Width (Write Cycle)	25	75000	30	75000	35	75000	ns	
26	t _{WL1RH1}	t _{RWL}	Write Command to \overline{RAS} Lead Time	25		30		35		ns	
27	t _{WL1CH1}	t _{CWL}	Write Command to \overline{CAS} Lead Time	25		30		35		ns	
28	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	20		20		25		ns	
29	t _{WL1CL2}	t _{WCS}	Write Command Set-up Time	0		0		0		ns	11
30	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	25		30		35		ns	
31	t _{DVCL2}	t _{DS}	Data-In Set-up Time	0		0		0		ns	
32	t _{CL1DX}	t _{DH}	Data-In Hold Time	20		20		25		ns	

NOTES:

6. Assumes that t_{RCD} ≤ t_{RCD} (max). If t_{RCD} > t_{RCD} (max), then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
7. Assumes t_{RCD} ≥ t_{RCD} (max).
8. If t_{ASC} < (t_{CAA} (max) - t_{CAC} (max) - t_T), then access time is defined by t_{CAA} rather than by t_{CAC}.
9. When a Ripplemode read cycle immediately follows a Ripplemode write cycle, the specification must be increased by 10 ns.
10. Either t_{RCH} or t_{RRH} must be satisfied.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS} (min), the cycle is a \overline{CAS} controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min) and t_{AWD} ≥ t_{AWD}(min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)

Read-Modify-Write Cycle 12

#	JEDEC Symbol	Symbol	Parameter	51C64H-8		51C64H-10		51C64H-12		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
33	t _{RL2RL2(RMW)}	t _{RWC}	Read-Modify-Write (RMW) Cycle Time	170		195		230		ns	
34	t _{RL1RH1(RMW)}	t _{RRW}	RMW Cycle $\overline{\text{RAS}}$ Pulse Width	110	75000	135	75000	160	75000	ns	
35	t _{CL1CH1(RMW)}	t _{CRW}	RMW Cycle $\overline{\text{CAS}}$ Pulse Width	50	75000	55	75000	65	75000	ns	
36	t _{RL1WL2}	t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	80		100		120		ns	13
37	t _{CL1WL2}	t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	20		20		25		ns	13
38	t _{AVWL2}	t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay	45		55		65		ns	13

Ripplemode Cycle 14

#	JEDEC Symbol	Symbol	Parameter	51C64H-8		51C64H-10		51C64H-12		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t _{CH2QV}	t _{CAP}	Access Time From Column Precharge		50		60		70	ns	15,16
40	t _{CL2CL2(R)}	t _{PC}	Ripplemode Read or Write Cycle	55		65		75		ns	15,16
41	t _{CL2CL2(RRMW)}	t _{PCM}	Ripplemode RMW Cycle Time	80		95		110		ns	

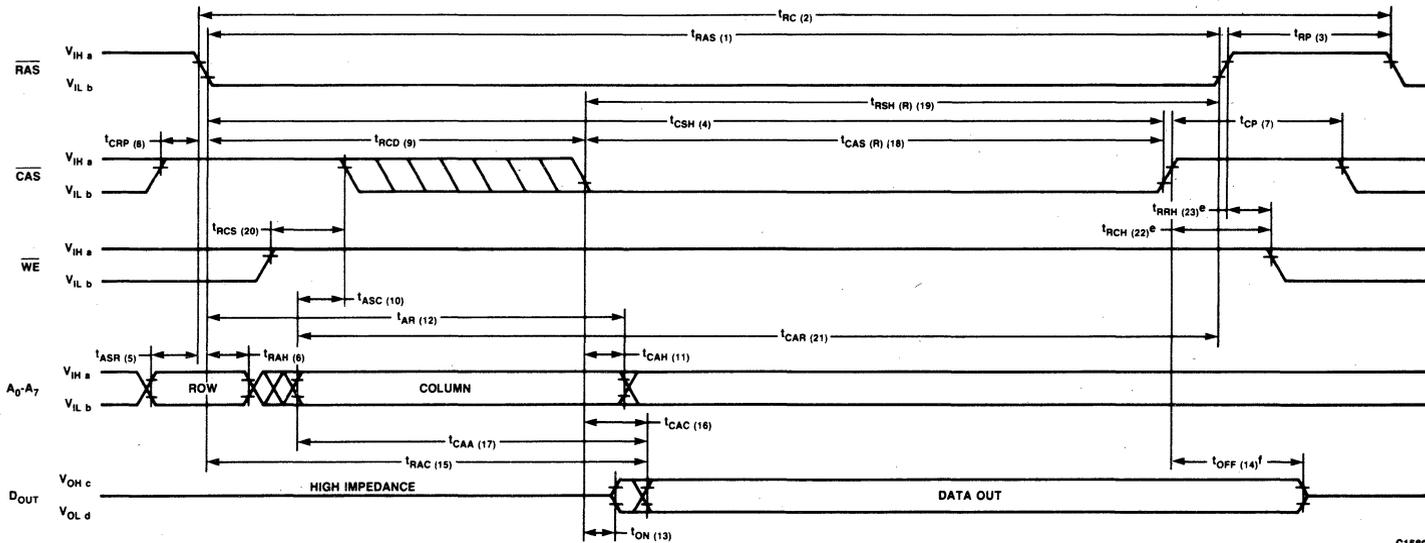
NOTES:

12. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS} (min), the cycle is a $\overline{\text{CAS}}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min) and t_{AWD} ≥ t_{AWD} (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.
14. All previously specified A.C. Characteristics are applicable.
15. Access time is determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.
16. When a Ripplemode read cycle immediately follows a Ripplemode write cycle, the specification must be increased by 10 ns.

WAVEFORMS

Read Cycle

2-6



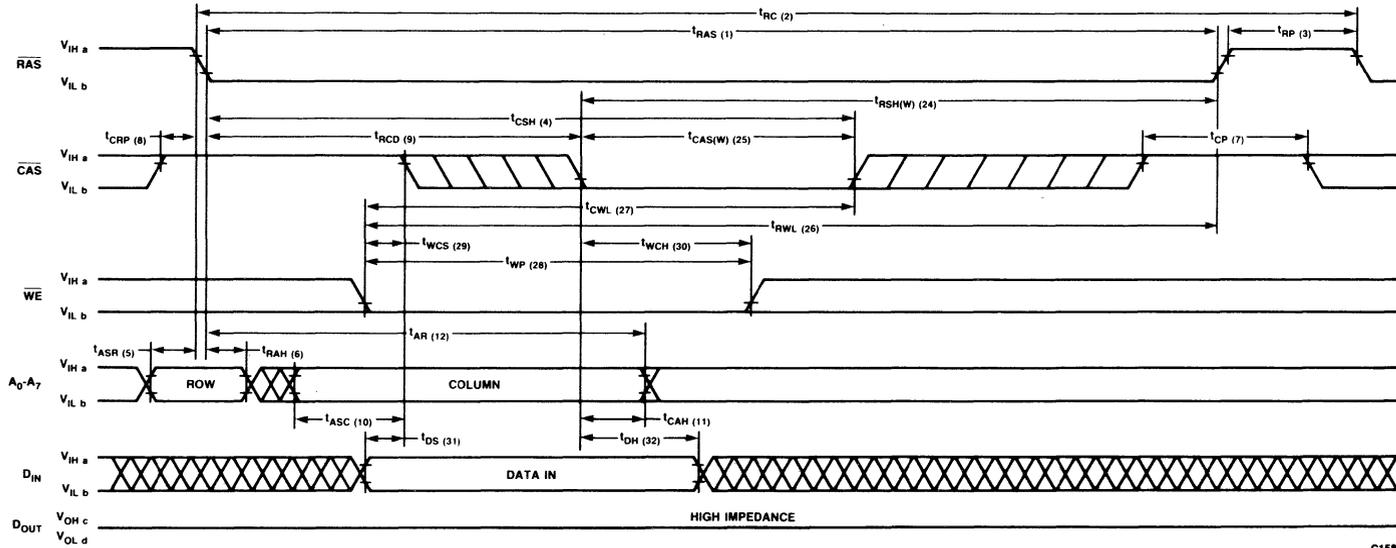
C1580

NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- Either t_{RCH} or t_{RRH} must be satisfied.
- t_{OFF} is measured to $|I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)

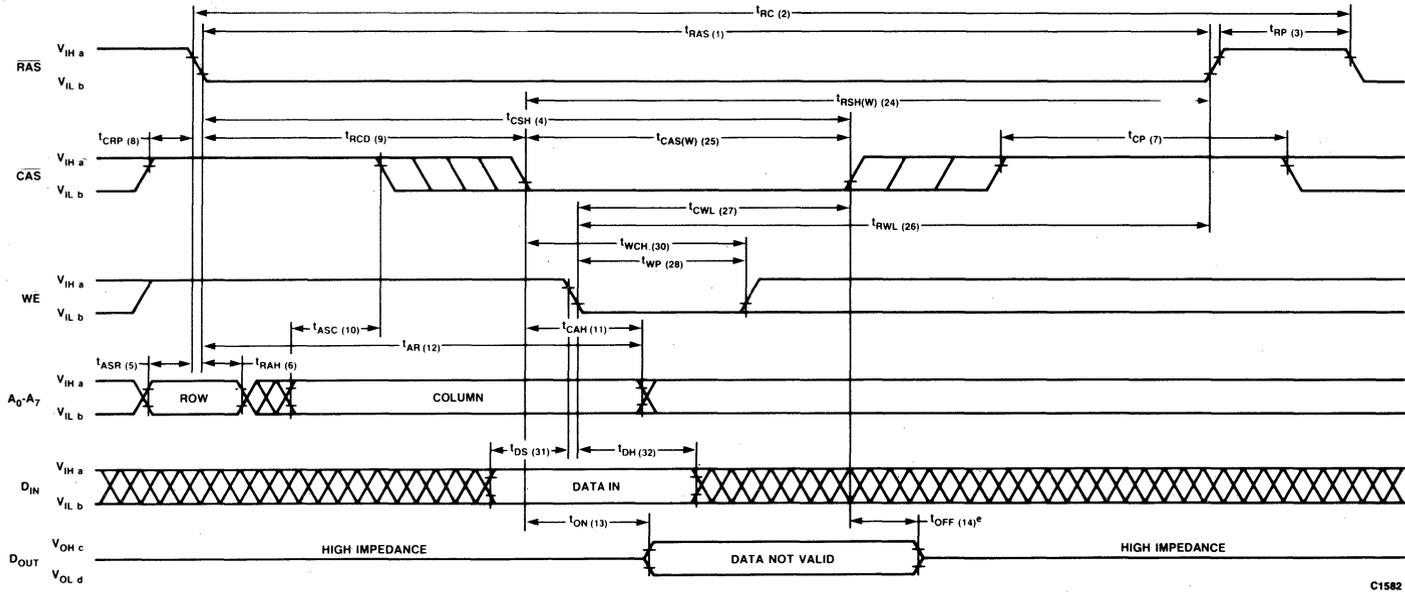
Write Cycle ($\overline{\text{CAS}}$ Controlled)^e



NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- WE is low prior to or simultaneously with CAS low transition. CAS latches column address and data-in.

WAVEFORMS (Cont.)
Write Cycle (WE Controlled)^f



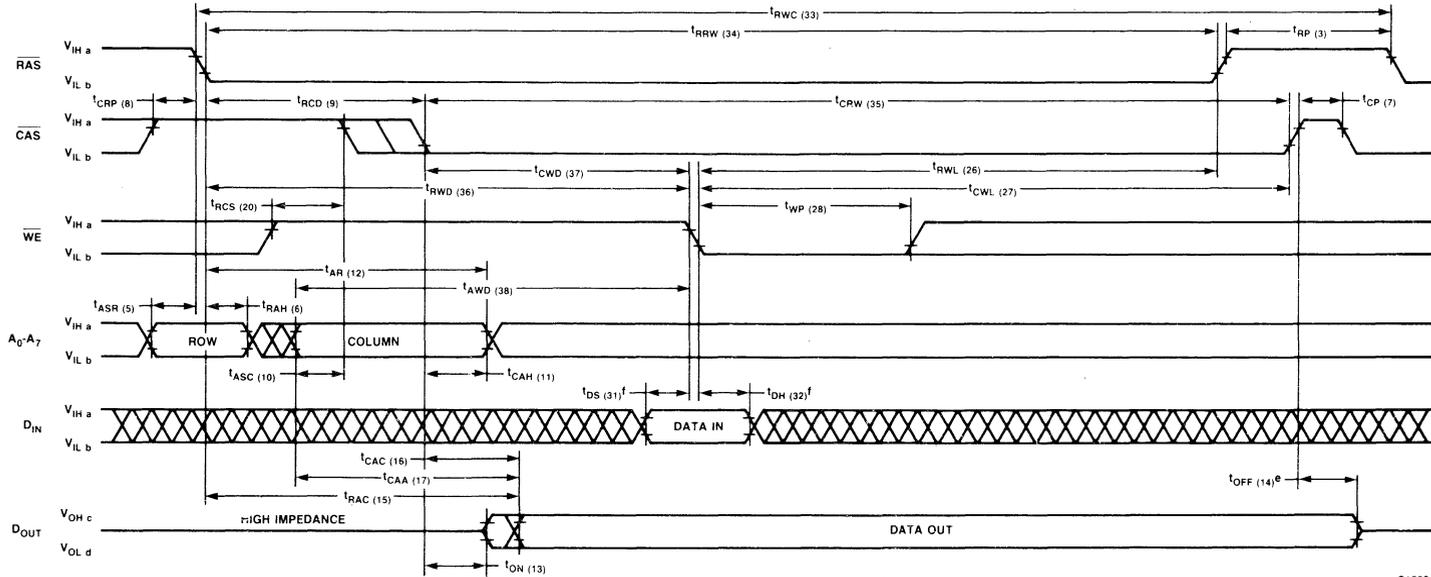
C1582

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
- f. CAS is low prior to the WE low transition. \overline{CAS} latches the column address while \overline{WE} latches the data-in.

WAVEFORMS (Cont.)

Read/Modify/Write Cycle

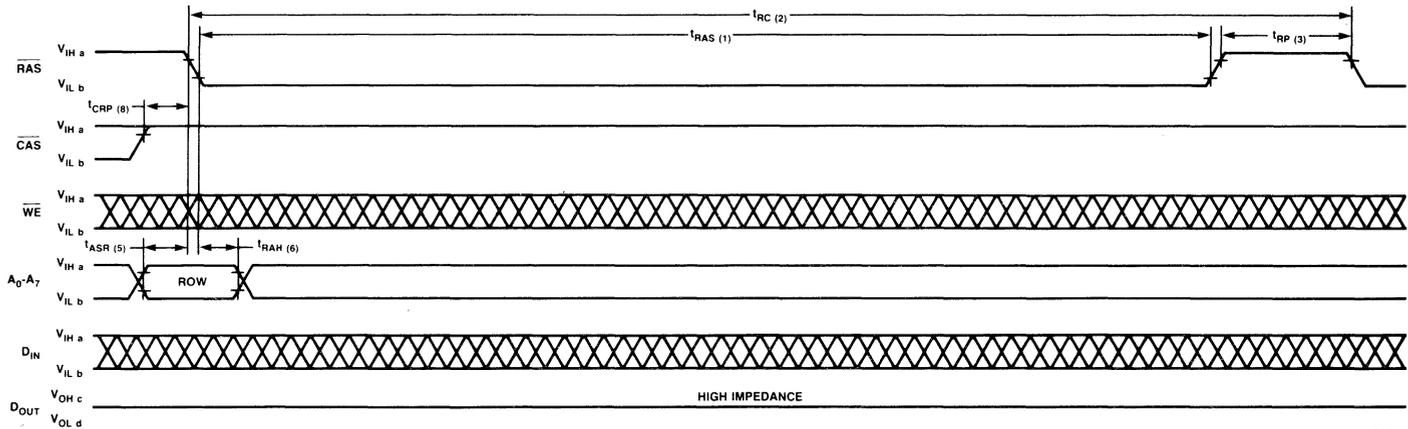


C1583

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
- f. t_{DS} and t_{DH} are referenced to \overline{CAS} or \overline{WE} , whichever occurs last.

WAVEFORMS (Cont.) RAS-Only Refresh Cycle



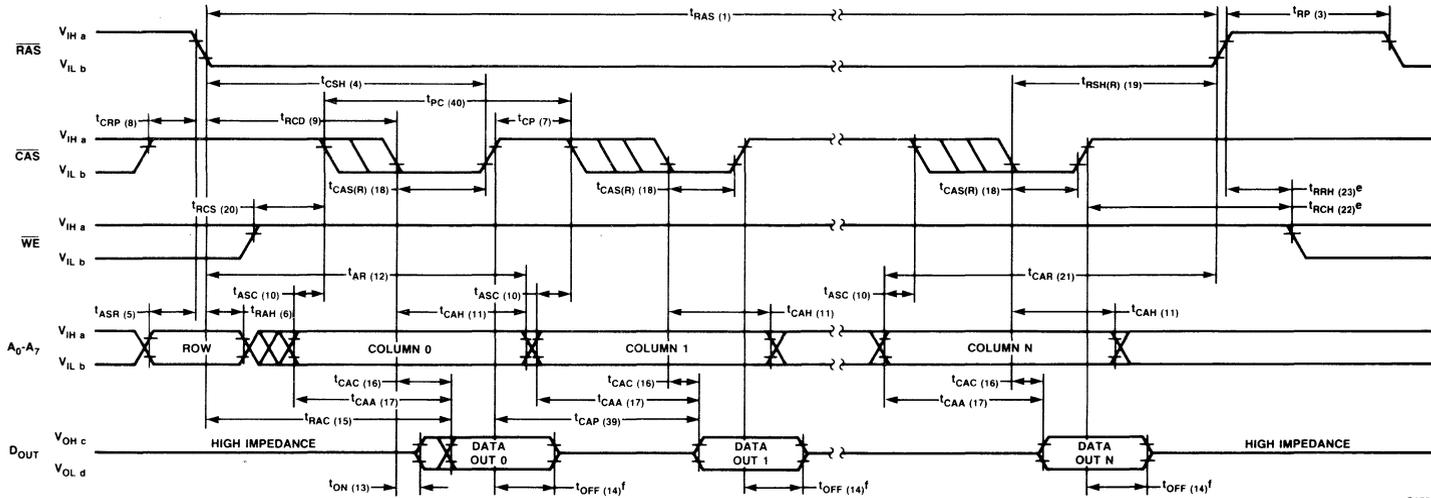
C1584

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

WAVEFORMS (Cont.)

Ripplemode Read Cycle



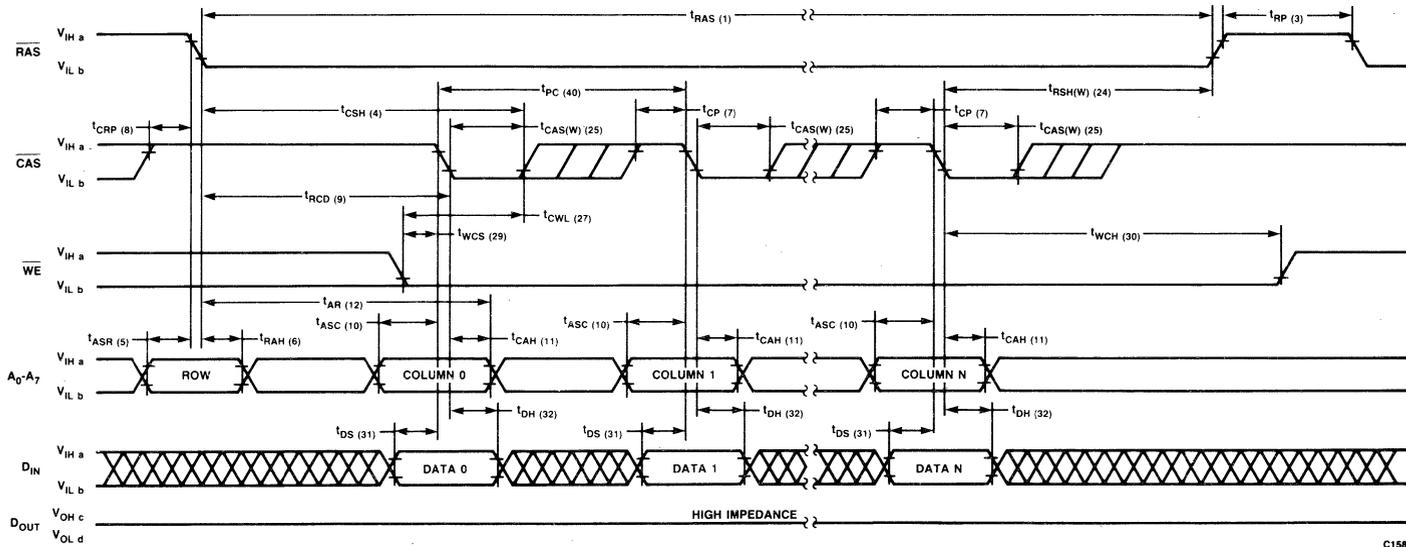
C1585

NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- Either t_{RCH} or t_{RRH} must be satisfied.
- t_{OFF} is measured to $|I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)

Ripplemode Write Cycle ($\overline{\text{CAS}}$ Controlled)^e



2-12

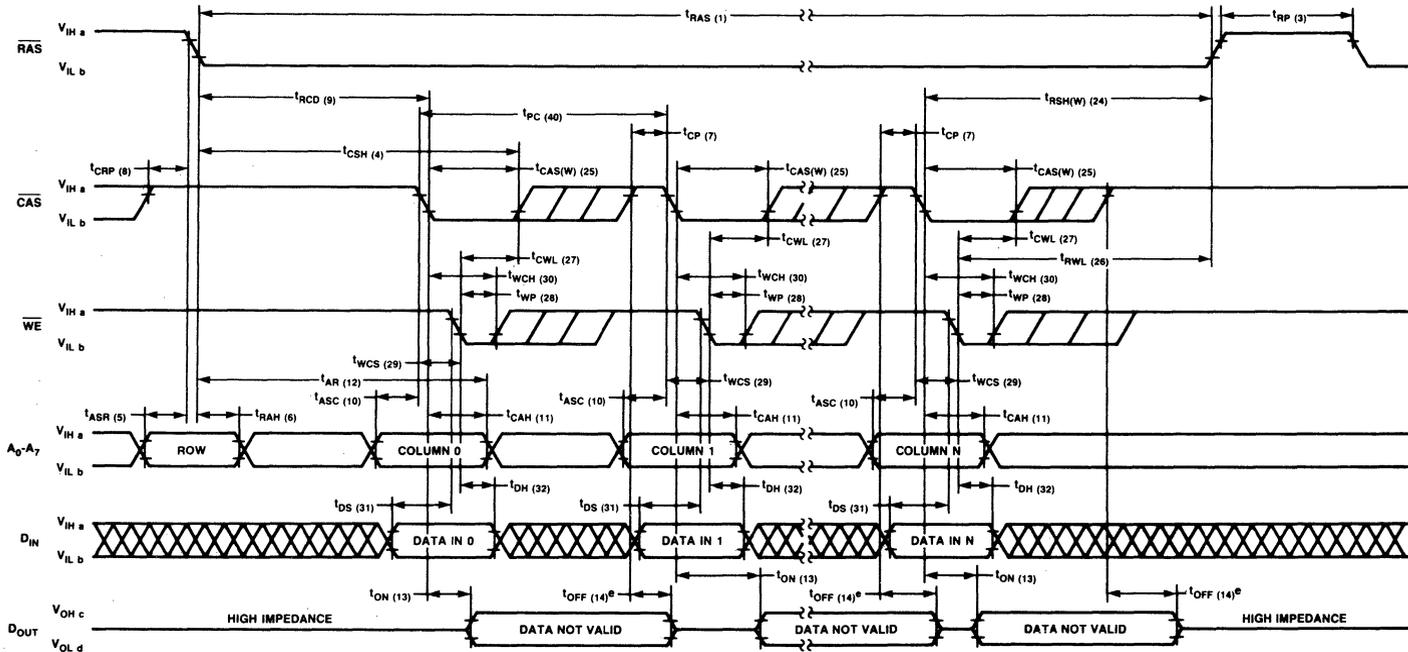
NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column addresses and data-in.

C1586

WAVEFORMS (Cont.)

Ripplemode Write Cycle (\overline{WE} Controlled)^f



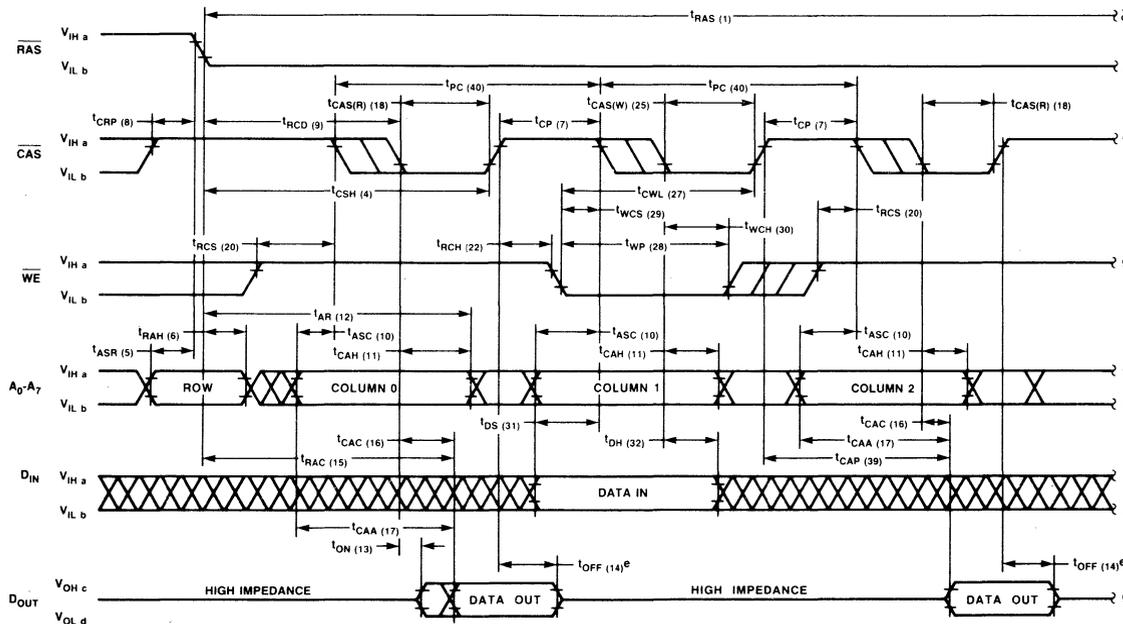
C1587

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{OL}|$.
- f. \overline{CAS} is low prior to or simultaneously with \overline{WE} low transition. \overline{CAS} latches the column addresses while \overline{WE} latches the data-in.

WAVEFORMS

Ripplemode Read/Write/Read. . . Cycle ($\overline{\text{CAS}}$ Controlled)^f



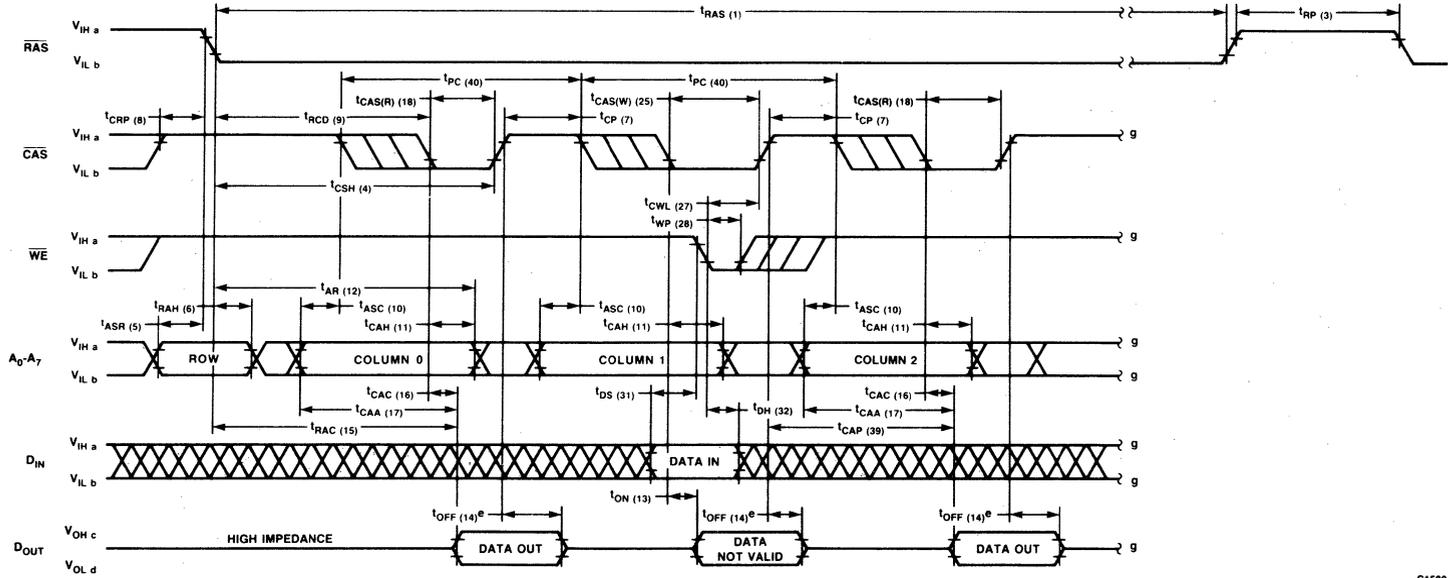
NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $I_{OUT} \leq I_{IO}$.
- f. $\overline{\text{WE}}$ is low prior to $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column addresses and data-in.
- g. The cycle can be terminated either by a read or a write operation followed by a $\overline{\text{RAS}}$ high transition. See page 11 or 12 for timings.

C1588

WAVEFORMS

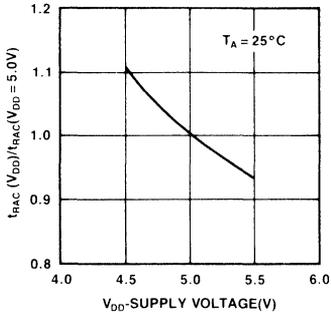
Ripplemode Read/Write/Read...Cycle (\overline{WE} Controlled)^f



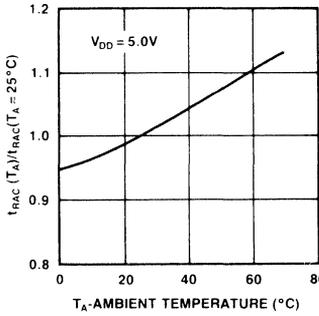
NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
- f. \overline{CAS} is low prior to \overline{WE} low transition. \overline{CAS} latches the column addresses while \overline{WE} latches data-in.
- g. The cycle can be terminated either by a read or a write operation followed by a \overline{RAS} high transition. See page 11 or 13 for timings.

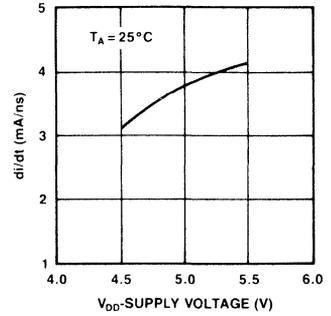
GRAPH 1
TYPICAL ACCESS TIME
 t_{RAC} (NORMALIZED) vs. V_{DD}



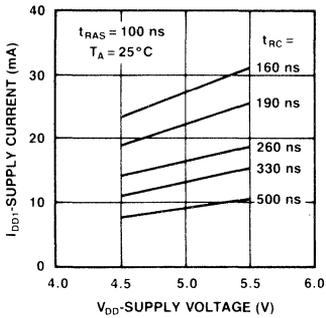
GRAPH 2
TYPICAL ACCESS TIME
 t_{RAC} (NORMALIZED) vs. T_A



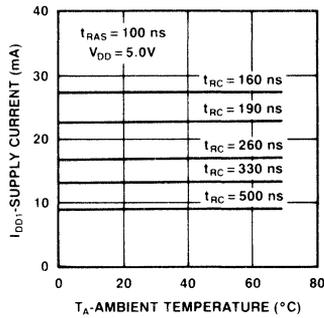
GRAPH 3
TYPICAL CURRENT TRANSIENTS
 di/dt vs. V_{DD}



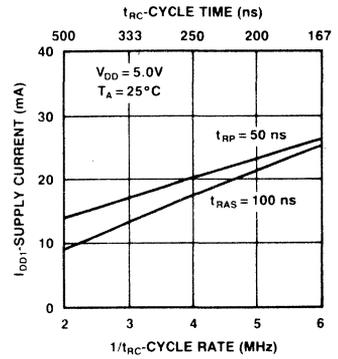
GRAPH 4
TYPICAL OPERATING CURRENT
 I_{DD1} vs. V_{DD}



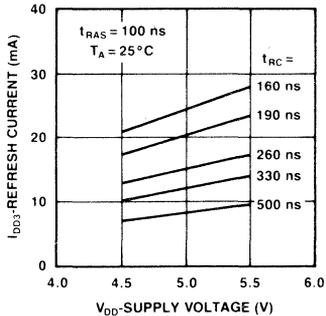
GRAPH 5
TYPICAL OPERATING CURRENT
 I_{DD1} vs. T_A



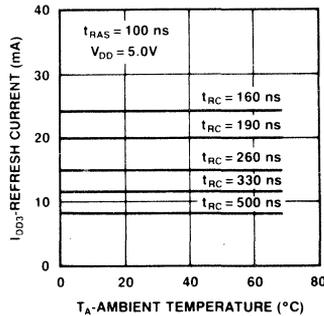
GRAPH 6
TYPICAL OPERATING CURRENT
 I_{DD1} vs. $1/t_{RC}$



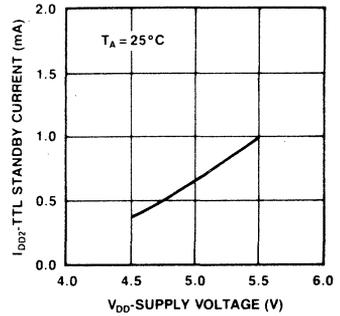
GRAPH 7
TYPICAL REFRESH CURRENT
 I_{DD3} vs. V_{DD}



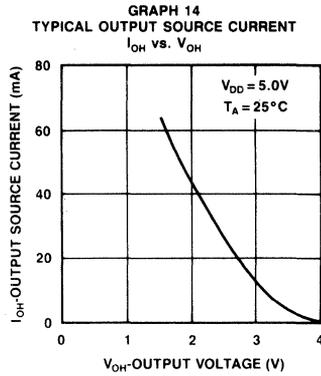
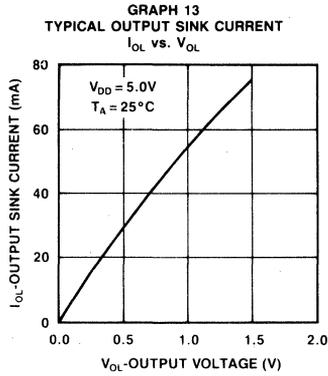
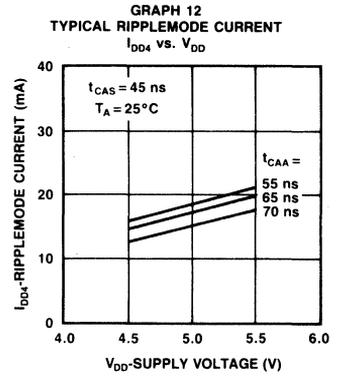
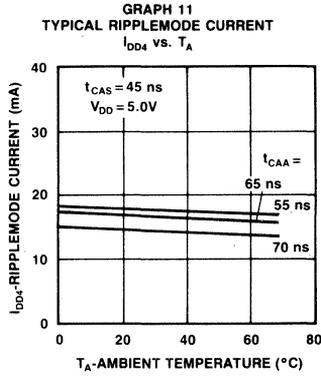
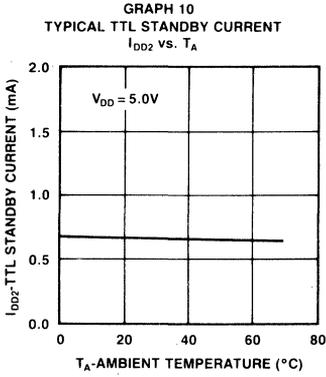
GRAPH 8
TYPICAL REFRESH CURRENT
 I_{DD3} vs. T_A



GRAPH 9
TYPICAL TTL STANDBY CURRENT
 I_{DD2} vs. V_{DD}



C14928-V
C14938-V



C1493B-V

FUNCTIONAL DESCRIPTIONS

The 51C64H is a CHMOS dynamic RAM optimized for high data bandwidth applications. The functionality is similar to a traditional dynamic RAM. The 51C64H reads and writes data by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe (\overline{RAS}). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe (\overline{CAS}). Because access time is primarily dependent upon a valid column address, the delay time between \overline{RAS} and \overline{CAS} can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing \overline{RAS} low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable (\overline{WE}) signal high during the $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR} . Data out becomes valid only when t_{RAC} , t_{CAA} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking \overline{WE} and \overline{CAS} low during a \overline{RAS} operation. The column address is latched in by \overline{CAS} . The write cycle can be \overline{WE} controlled or \overline{CAS} controlled depending upon the later of \overline{WE} or \overline{CAS} low transition. Consequently, the input data must be valid at or before the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. In a \overline{CAS} controlled write cycle (the leading edge of \overline{WE} occurs prior to or

coincident with the \overline{CAS} low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with \overline{CAS} will maintain the output in the high impedance state; terminating with \overline{WE} allows the output to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with \overline{RAS} at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or \overline{RAS} -Only cycle will perform refresh.

Ripplemode™ Operation

Ripplemode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining \overline{RAS} low while successive \overline{CAS} cycles are performed, retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while \overline{CAS} is high. Access begins from the valid column address rather than from \overline{CAS} , eliminating t_{ASC} and t_f from the critical timing path. \overline{CAS} latches the addresses into the column address buffer and acts as an output enable.

During this operation read, write, read-modify-write, or read-write-read cycles are possible at random or sequential addresses within a row. Following the entry cycle into Ripplemode operation, access time is t_{CAA} or t_{CAP} dependent. If the column address is valid prior to or coincident with the rising edge of \overline{CAS} , then the access time is determined by the rising edge of \overline{CAS} specified by t_{CAP} as shown in Figure 1. If the column address is valid after the rising edge of \overline{CAS} , then the access time is determined by the valid column address specified by t_{CAA} . For both cases, the falling edge of \overline{CAS} latches the address and enables the output.

Ripplemode operation provides a sustained data rate over 18 MHz for applications that require high data rate such as bit mapped graphics or high speed sig-

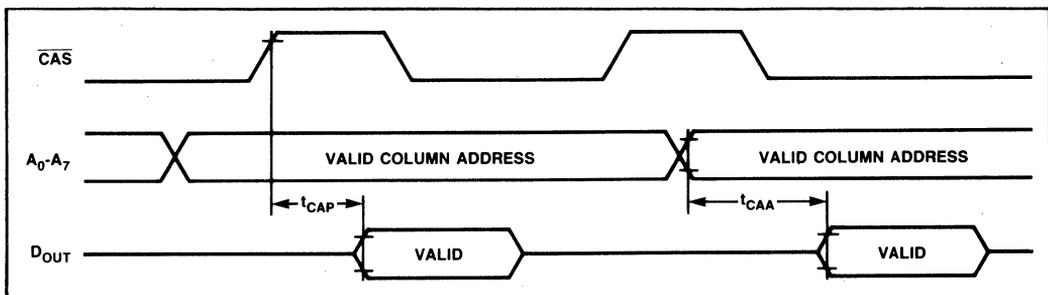


Figure 1. Ripplemode™ Access Time Determination

nal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255 t_{PC}}$$

Data Out Operation

The 51C64H data Output (D_{OUT}), which has three-state capability, is controlled by \overline{CAS} . During \overline{CAS} high state (\overline{CAS} at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles, containing a \overline{RAS} clock such as \overline{RAS} -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).

The V_{DD} current (I_{DD}) requirement of the 51C64H during power on is dependent upon the input levels of \overline{RAS} and \overline{CAS} . If $\overline{RAS} = V_{SS}$ during power on, the

device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that \overline{RAS} and \overline{CAS} track with V_{DD} or be held at a valid V_{IH} during power on.

Soft Error Rate

Soft errors are random, non-recurring changes in memory logic states caused by the impact of an ionizing particle, such as an alpha particle. For example, a logic "0" may change to a logic "1". The average soft error rate (SER) of the 51C64H is less than 10 FITs. This is determined by accelerated testing using an alpha particle source and is subsequently confirmed by system testing. The SER is a function of the operating voltage, cycle time, package, and the alpha particle source. Intel measures the SER at $V_{DD} = 4.75V$, and $t_{cycle} = 1\mu s$. A thorium source of $1.6 \times 10^5 \alpha/cm^2/hr.$ is used because it best matches the package energy spectra.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

Table 1. Intel 51C64H Data Output Operation for Various Types of Cycles

Type of Cycle	Data Out State
Read Cycle	Data from Addressed Memory Cell
\overline{CAS} Controlled Write Cycle (Early Write)	High Impedance
\overline{WE} Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Read-Write-Read Cycle (\overline{CAS} Controlled)	Data from Addressed Memory Cell
Read-Write-Read Cycle (\overline{WE} Controlled)	Data from Addr. Memory Cell and Active, Not Valid
\overline{RAS} -Only Refresh Cycle	High Impedance
\overline{CAS} -Only Cycle	High Impedance

51C64L

LOW POWER 64K X 1

CHMOS DYNAMIC RAM

	51C64L-10	51C64L-12
Maximum Access Time (ns)	100	120
Maximum CHMOS Standby Current (mA)	0.05	0.05

■ Low Power Data Retention

- Standby current, CHMOS — $50\mu\text{A}$ (max.)
- Refresh period, $\overline{\text{RAS}}$ -Only — 64 ms (max.)
- Data retention current — $80\mu\text{A}$ (max.)

■ Low Operating Current — 35mA (max.)

■ Fully TTL Compatible Inputs and Outputs

■ Low Input/Output Capacitance

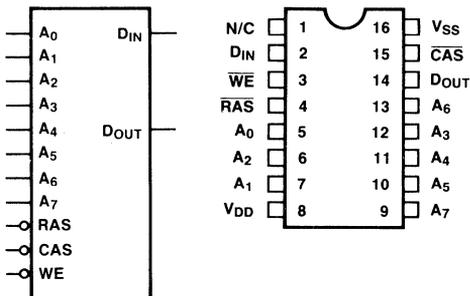
■ High Reliability Plastic — 16 Pin DIP

The Intel® 51C64L is a low power 65,536 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C64L offers features not provided by an NMOS dynamic RAM: CHMOS standby current and extended $\overline{\text{RAS}}$ -Only refresh for low data retention power. All inputs and outputs are fully TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

The 51C64L offers a maximum standby current of $50\mu\text{A}$ when $\overline{\text{RAS}} \geq V_{\text{DD}} - 0.5\text{V}$. During standby (i.e. refresh only cycles) the refresh period can be extended to 64 ms to reduce the total current required for data retention to less than $80\mu\text{A}$ (max). The 51C64L combines low power with high density for portable and battery backup applications.

LOGIC SYMBOL PIN CONFIGURATION

PIN NAMES



$\overline{\text{RAS}}$	ROW ADDRESS STROBE
$\overline{\text{CAS}}$	COLUMN ADDRESS STROBE
$\overline{\text{WE}}$	WRITE ENABLE
$\text{A}_0\text{-A}_7$	ADDRESS INPUTS
D_{IN}	DATA IN
D_{OUT}	DATA OUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under

- Bias.....-10°C to +80°C
- Storage Temperature... Plastic -55°C to +125°C
- Voltage on Any Pin except V_{DD} and D_{OUT}
 Relative to V_{SS}.....-2.0V to 7.5V
- Voltage on V_{DD} Relative to V_{SS}.....-1.0V to 7.5V
- Voltage on D_{OUT}
 Relative to V_{SS}.....-2.0V to V_{DD}+1V
- Data Out Current.....50 mA
- Power Dissipation.....1.0W

†COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C64L			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating		27	37	mA	t _{RC} = t _{RC} (min), for - 10 specification	3,4
			23	35	mA	t _{RC} = t _{RC} (min), for - 12 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby		0.7	2	mA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, RAS-Only Refresh		24	37	mA	t _{RC} = t _{RC} (min), for - 10 specification	4
			20	35	mA	t _{RC} = t _{RC} (min), for - 12 specification	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled		3	4	mA	$\overline{\text{RAS}}$ at V _{IH} , $\overline{\text{CAS}}$ at V _{IL} , all other inputs and output ≥ V _{SS}	3
I _{DD6}	V _{DD} Supply Current, CHMOS Standby		0.008	0.05	mA	$\overline{\text{RAS}} \geq V_{DD} - 0.5V$ and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{LI}	Input Load Current (any pin)			1	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current for High Impedance State			1	μA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	- 1.0		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} +1	V		5
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	6
V _{OH}	Output High Voltage	2.4			V	I _{OH} = - 5 mA	6

NOTES:

1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and V_{DD} = + 5V.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{\text{CAS}}$ is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†
 $T_A = 25^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Address, D_{IN}	3	4	pF
C_{IN2}	\overline{RAS} , \overline{CAS} , \overline{WE}	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

A.C. CHARACTERISTICS^{1, 2, 3}
 $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	\overline{RAS} Pulse Width	100	75000	120	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	160		190		ns	
3	t_{RH2RL2}	t_{RP}	\overline{RAS} Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}	\overline{CAS} Hold Time	100		120		ns	
5	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
6	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		ns	
7	t_{CH2CL2}	t_{CP}	\overline{CAS} Precharge Time	10		15		ns	
8	t_{CH2RL2}	t_{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	-20		-20		ns	
9	t_{RL1CL2}	t_{RCD}	\overline{RAS} to \overline{CAS} Delay	30	80	35	95	ns	4
10	t_{AVCL2}	t_{ASC}	Column Address Set-up Time	0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10		15		ns	
12	t_{RL1AX}	t_{AR}	Column Address Hold Time From \overline{RAS}	40		50		ns	
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4	ms	5
	t_{RVRV}	t_{REF2}	Time Between Refresh (\overline{RAS} -Only)		64		64	ms	5
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6
13	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0	20	0	25	ns	
14	t_{CH2QZ}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	ns	

NOTES:

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a \overline{RAS} clock such as \overline{RAS} -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).
- A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, $V_{IL}(\text{min}) \geq V_{SS}$ and $V_{IH}(\text{max}) \leq V_{DD}$.
- $t_{RCD}(\text{max})$ is specified for reference only.
- The 51C64L extends the refresh period to 64 ms during \overline{RAS} -Only refresh operation.
- t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

A.C. CHARACTERISTICS (Con't.)
Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
15	t _{RL1QV}	t _{RAC}	Access Time From $\overline{\text{RAS}}$		100		120	ns	7
16	t _{CL1QV}	t _{CAC}	Access Time From $\overline{\text{CAS}}$		20		25	ns	8,9
17	t _{AVQV}	t _{CAA}	Access Time From Column Address		55		65	ns	9
18	t _{CL1CH1(R)}	t _{CAS(R)}	$\overline{\text{CAS}}$ Pulse Width (Read Cycle)	20	75000	25	75000	ns	
19	t _{CL1RH1(R)}	t _{RSH(R)}	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	10		10		ns	
20	t _{WH2CL2}	t _{RCS}	Read Command Set-up Time	0		0		ns	
21	t _{AVRH1}	t _{CAR}	Column Address to $\overline{\text{RAS}}$ Set-up Time	55		65		ns	
22	t _{CH2WX}	t _{RCH}	Read Com. Hold Time Ref. to $\overline{\text{CAS}}$	0		0		ns	10
23	t _{RH2WX}	t _{RRH}	Read Com. Hold Time Ref. to $\overline{\text{RAS}}$	10		10		ns	10

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
24	t _{CL1RH1(W)}	t _{RSH(W)}	$\overline{\text{RAS}}$ Hold Time (Write Cycle)	35		40		ns	
25	t _{CL1CH1(W)}	t _{CAS(W)}	$\overline{\text{CAS}}$ Pulse Width (Write Cycle)	30	75000	35	75000	ns	
26	t _{WL1RH1}	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	30		35		ns	
27	t _{WL1CH1}	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	30		35		ns	
28	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	20		25		ns	
29	t _{WL1CL2}	t _{WCS}	Write Command Set-up Time	0		0		ns	11
30	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	30		35		ns	
31	t _{DVCL2}	t _{DS}	Data-In Set-up Time	0		0		ns	
32	t _{CL1DX}	t _{DH}	Data-In Hold Time	20		25		ns	

NOTES:

7. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$. If $t_{\text{RCD}} > t_{\text{RCD}}(\text{max})$ then t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{\text{RCD}}(\text{max})$.
8. Assumes $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
9. If $t_{\text{ASC}} < (t_{\text{CAA}}(\text{max}) - t_{\text{CAC}}(\text{max}) - t_{\text{T}})$, then access time is defined by t_{CAA} rather than by t_{CAC} .
10. Either t_{RCH} or t_{RRH} must be satisfied.
11. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are specified as reference points only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is a $\overline{\text{CAS}}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)

Read-Modify-Write Cycle 12

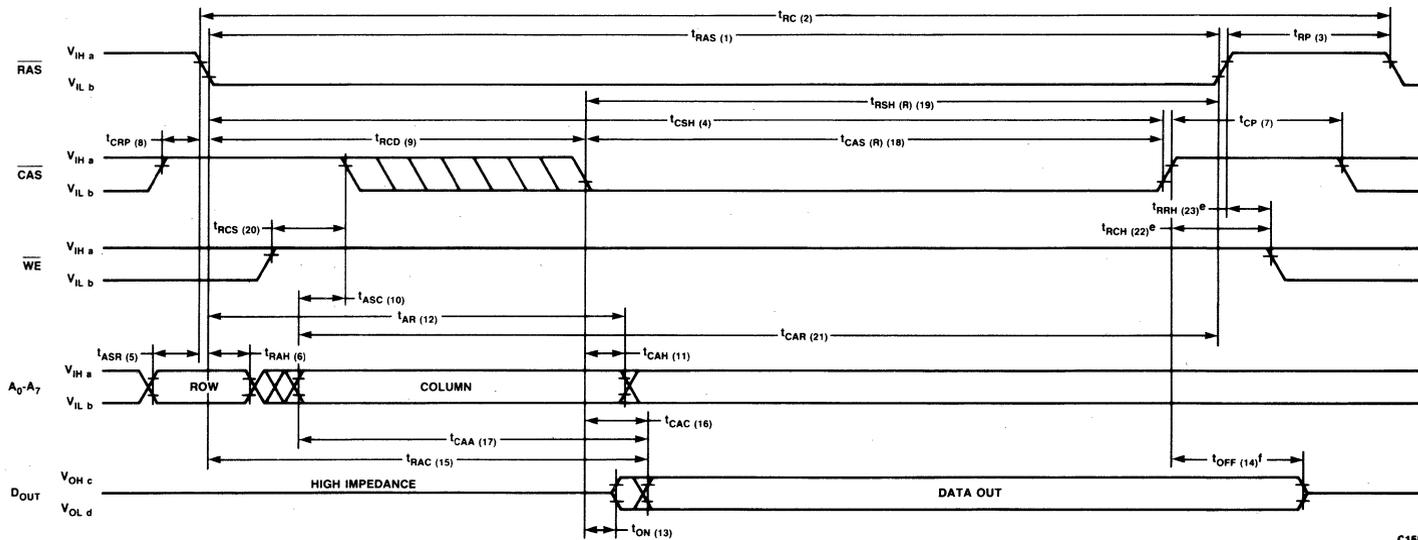
#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
33	t _{RL2RL2(RMW)}	t _{RWC}	Read-Modify-Write (RMW) Cycle Time	195		230		ns	
34	t _{RL1RH1(RMW)}	t _{RRW}	RMW Cycle \overline{RAS} Pulse Width	135	75000	160	75000	ns	
35	t _{CL1CH1(RMW)}	t _{CRW}	RMW Cycle \overline{CAS} Pulse Width	55	75000	65	75000	ns	
36	t _{RL1WL2}	t _{RWD}	\overline{RAS} to \overline{WE} Delay	100		120		ns	13
37	t _{CL1WL2}	t _{CWD}	\overline{CAS} to \overline{WE} Delay	20		25		ns	13
38	t _{AWL2}	t _{AWD}	Column Address to \overline{WE} Delay	55		65		ns	13

NOTES:

12. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS} (min), the cycle is a \overline{CAS} controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min) and t_{AWD} ≥ t_{AWD} (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.

WAVEFORMS

Read Cycle



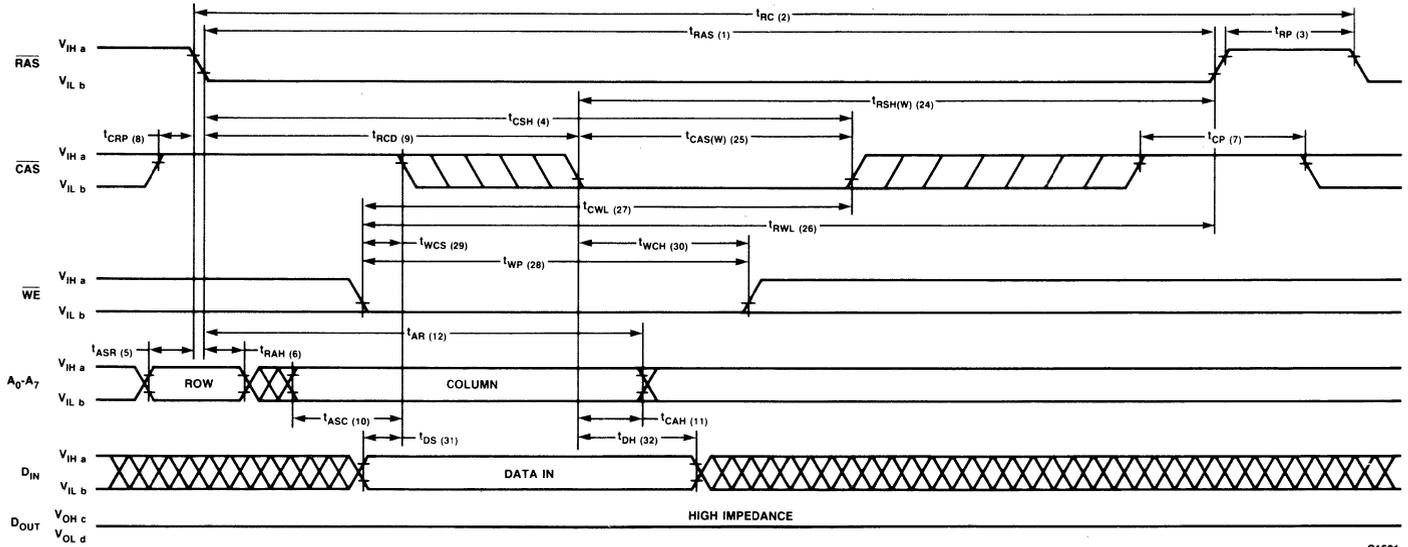
C1580

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. Either t_{RCH} or t_{RRH} must be satisfied.
- f. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)

Write Cycle ($\overline{\text{CAS}}$ Controlled)^e

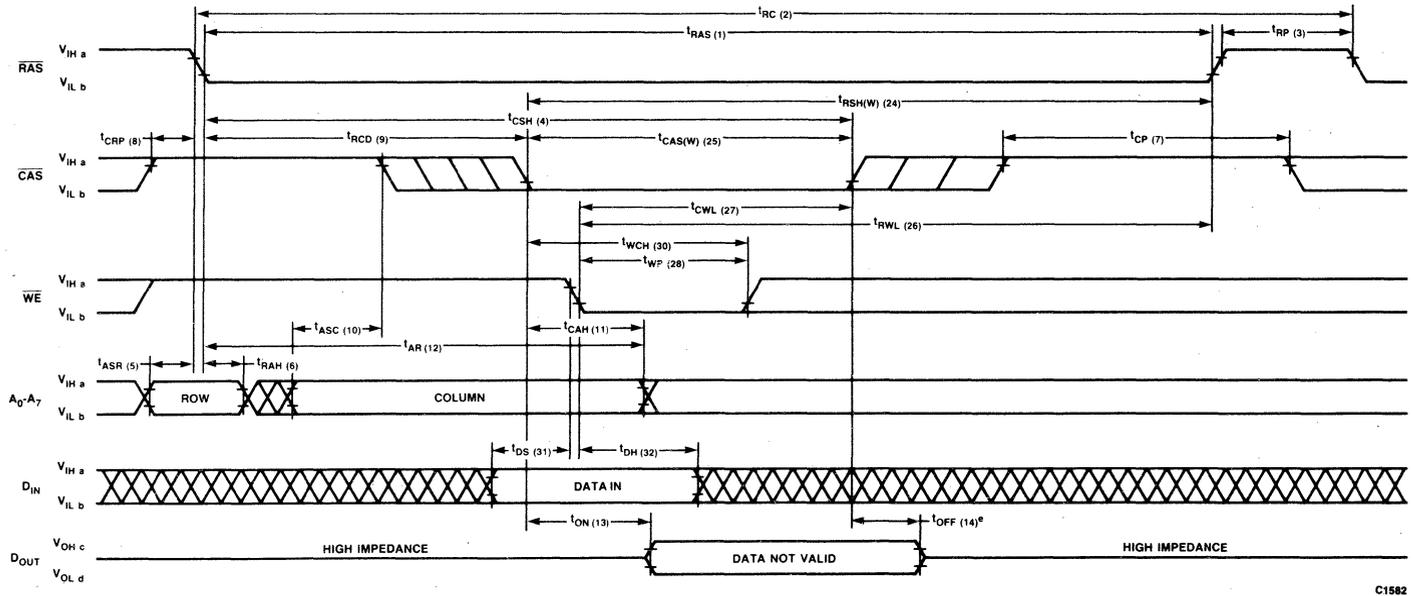


NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column address and data-in.

WAVEFORMS (Cont.)

Write Cycle (WE Controlled)^f

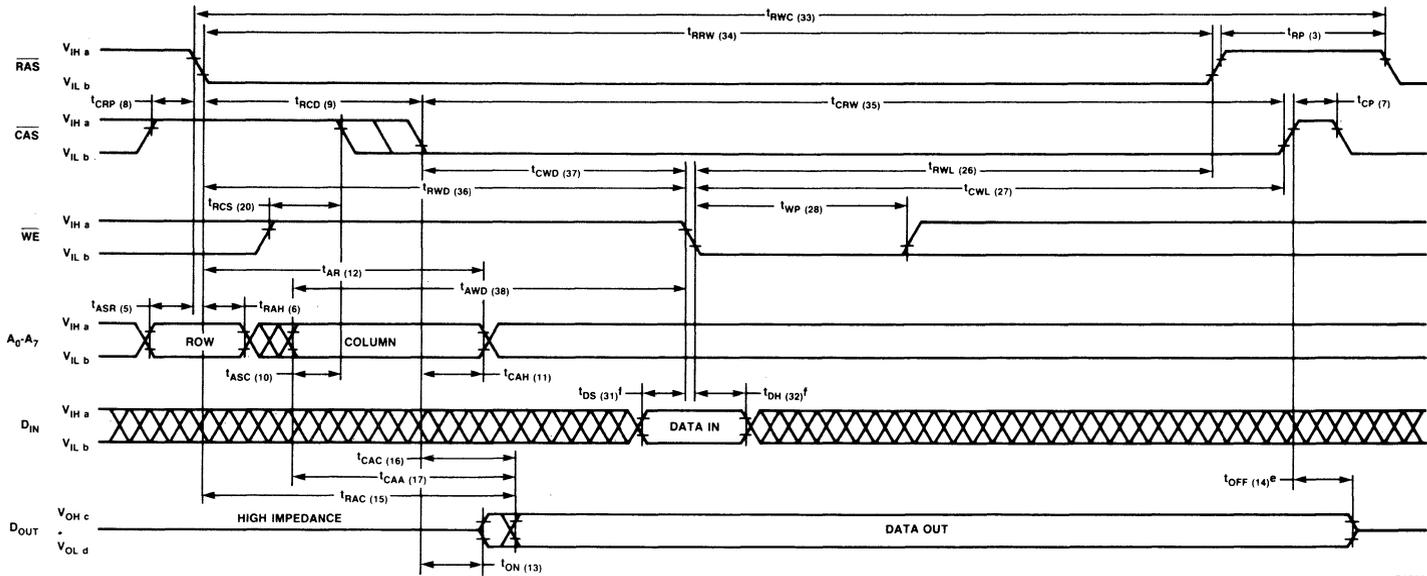


NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
- CAS is low prior to the WE low transition. CAS latches the column address while WE latches the data-in.

WAVEFORMS (Cont.)

Read/Modify/Write Cycle



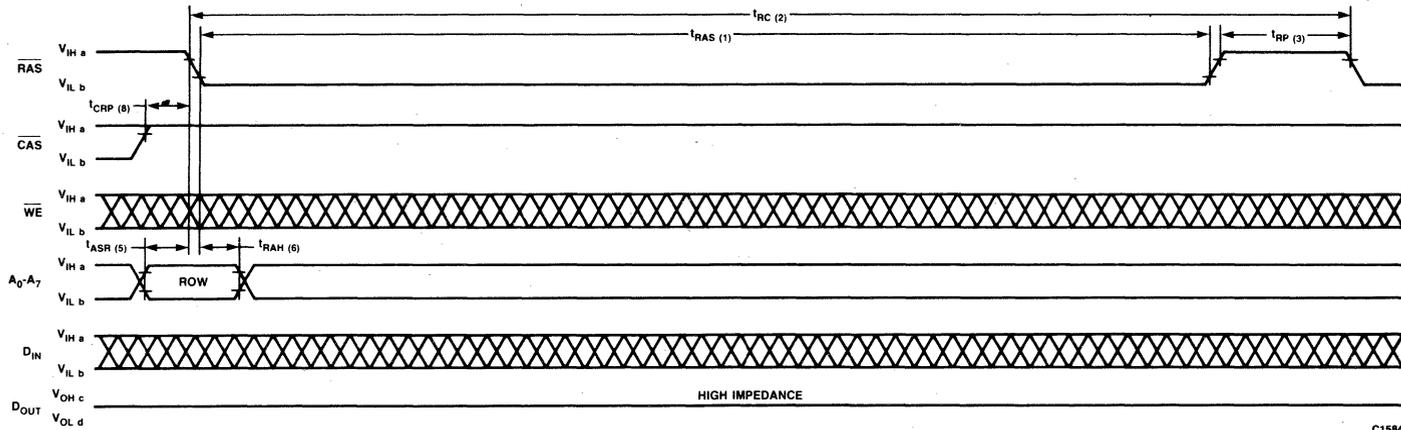
C1583

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $I_{OUT} \leq |I_{OL}|$.
- f. t_{DS} and t_{DH} are referenced to $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs last.

WAVEFORMS (Cont.)

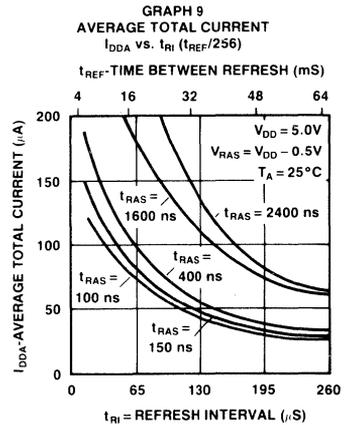
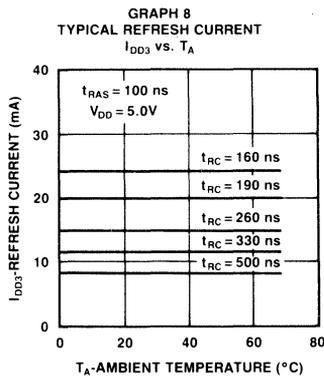
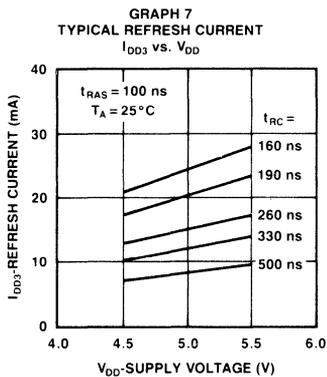
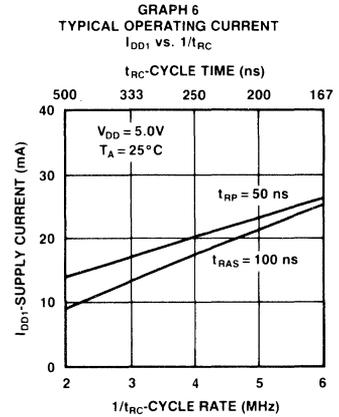
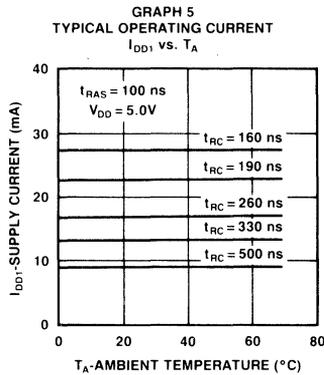
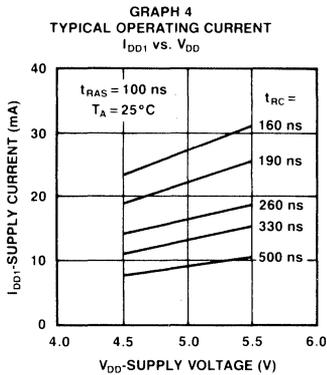
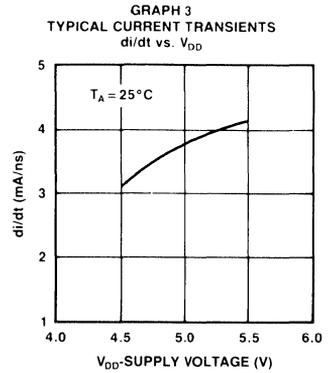
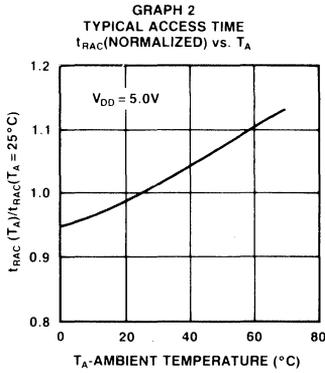
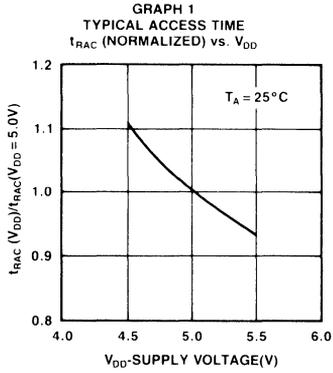
RAS-Only Refresh Cycle

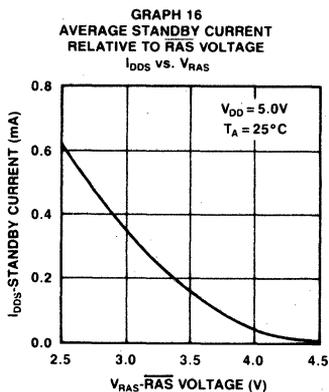
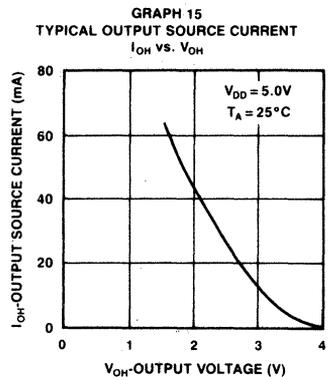
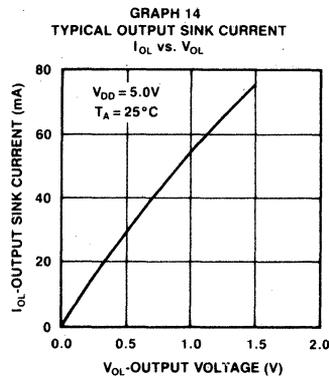
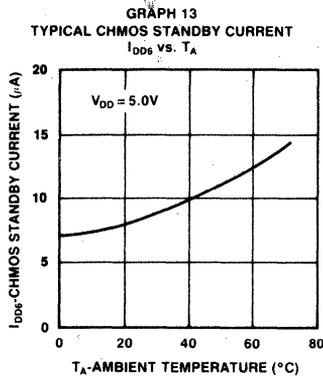
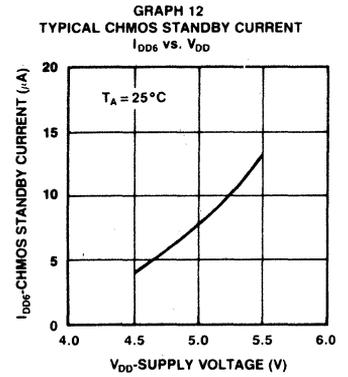
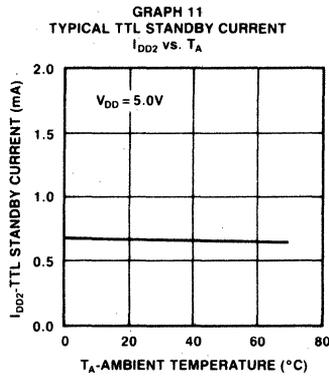
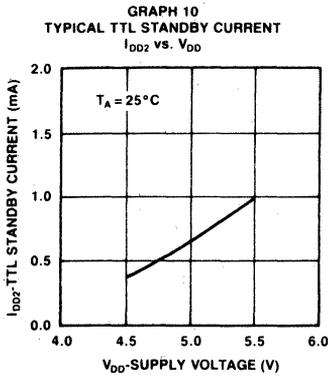


C1584

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .





FUNCTIONAL DESCRIPTIONS

The 51C64L is a CHMOS dynamic RAM optimized for low power applications. The functionality is similar to a traditional dynamic RAM. The 51C64L reads and writes data by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe ($\overline{\text{RAS}}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{\text{CAS}}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}/\overline{\text{CAS}}$ operation. The column address must be held for a minimum time specified by t_{AR} . Data out becomes valid only when t_{RAC} , t_{CAA} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ low during a $\overline{\text{RAS}}$ operation. The column address is latched in by $\overline{\text{CAS}}$. The write cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending upon the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. In a $\overline{\text{CAS}}$ controlled write cycle (the leading edge of $\overline{\text{WE}}$ occurs prior to or coincident with the $\overline{\text{CAS}}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the

beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ will maintain the output in the high impedance state; terminating with $\overline{\text{WE}}$ allows the output to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{\text{RAS}}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{\text{RAS}}$ -Only cycle will perform refresh.

Extended Refresh Cycle

The 51C64L extends the refresh cycle period to 64 milliseconds for $\overline{\text{RAS}}$ -Only refresh cycles. This feature reduces the total current consumption to a maximum of 80 micro Amperes, and typically 15 micro Amperes, for data retention ($\overline{\text{RAS}}$ -Only refresh operation for the 51C64L-12). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{\text{RC}} I_{\text{ACTIVE}}) + (t_{\text{RI}} - t_{\text{RC}}) (I_{\text{STANDBY}})}{t_{\text{RI}}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{\text{REF}}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Data Out Operation

The 51C64L Data Output (D_{OUT} , which has three-state capability, is controlled by $\overline{\text{CAS}}$. During $\overline{\text{CAS}}$ high state ($\overline{\text{CAS}}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles

Table 1. Intel 51C64L Data Output Operation for Various Types of Cycles

Type of Cycle	Data Out State
Read Cycle	Data from Addressed Memory Cell
$\overline{\text{CAS}}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{\text{WE}}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{\text{RAS}}$ -Only Refresh Cycle	High Impedance
$\overline{\text{CAS}}$ -Only Cycle	High Impedance

containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).

The V_{DD} current (I_{DD}) requirement of the 51C64L during power on is dependent upon the input levels of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. If $\overline{\text{RAS}} = V_{\text{ss}}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{DD} or be held at a valid V_{IH} during power on.

Soft Error Rate

Soft errors are random, non-recurring changes in memory logic states caused by the impact of an ionizing particle, such as an alpha particle. For example,

a logic "0" may change to a logic "1". The average soft error rate (SER) of the 51C64L is less than 10 FITs. This is determined by accelerated testing using an alpha particle source and is subsequently confirmed by system testing. The SER is a function of the operating voltage, cycle time, package, and the alpha particle source. Intel measures the SER at $V_{\text{DD}} = 4.75\text{V}$, and $t_{\text{cycle}} = 1\mu\text{s}$. A thorium source of $1.6 \times 10^5 \alpha/\text{cm}^2/\text{hr}$. is used because it best matches the package energy spectra.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

51C64HL

HIGH PERFORMANCE LOW POWER RIPPLEMODE™ 64K X1 CHMOS DYNAMIC RAM

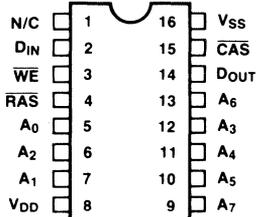
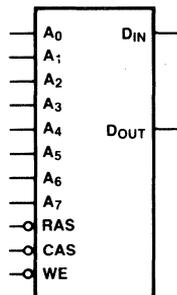
	51C64HL-10	51C64HL-12
Maximum Access Time (ns)	100	120
Maximum Column Address Access Time (ns)	55	65
Maximum CHMOS Standby Current (mA)	0.05	0.05

- **Ripplemode Operation**
 - Continuous data rate over 15 MHz
 - Random access within row
 - Flow through column latch for pipelining
 - t_{CAC} — 20, 25 ns
- **Low Input/Output Capacitance**
- **Fully TTL Compatible**
- **Low Power Data Retention**
 - Standby current, CHMOS — 50 μ A (max.)
 - Refresh period, \overline{RAS} -Only — 64 ms (max.)
 - Data Retention Current — 80 μ A (max.)
- **Low Operating Current — 37 mA (max.)**
- **High Reliability Plastic — 16 Pin DIP**

The Intel® 51C64HL is a high speed 65,536 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C64HL offers features not provided by an NMOS dynamic RAM: Ripplemode for high data bandwidth, fast usable speed, and CHMOS standby current and extended \overline{RAS} -Only refresh for low data retention power. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

Ripplemode operation allows random or sequential access of up to 256 bits within a row, with cycle times as fast as 65 ns. Because of static column circuitry, the \overline{CAS} clock is no longer in the critical timing path. The flow through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the 51C64HL ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance microprocessor systems.

The 51C64HL offers a maximum standby current of 50 μ A when $\overline{RAS} \geq V_{DD} - 0.5V$. During standby (i.e. refresh only cycles), the refresh period can be extended to 64 ms to reduce the total current required for data retention to less than 80 μ A (max). The 51C64HL combines low power with high density for portable and battery backup applications.

LOGIC SYMBOL
PIN CONFIGURATION
PIN NAMES


\overline{RAS}	ROW ADDRESS STROBE
\overline{CAS}	COLUMN ADDRESS STROBE
\overline{WE}	WRITE ENABLE
A ₀ -A ₇	ADDRESS INPUTS
D _{IN}	DATA IN
D _{OUT}	DATA OUT
V _{DD}	POWER (+ 5V)
V _{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias.....-10°C to +80°C
 Storage Temperature... Plastic -55°C to +125°C
 Voltage on Any Pin except V_{DD} and D_{OUT}
 Relative to V_{SS}.....-2.0V to 7.5V
 Voltage on V_{DD} Relative to V_{SS}.....-1.0V to 7.5V
 Voltage on D_{OUT}
 Relative to V_{SS}.....-2.0 to V_{DD} + 1V
 Data Out Current.....50 mA
 Power Dissipation.....1.0 W

†COMMENT

Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

t_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C64HL			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating		27	37	mA	t _{RC} = t _{RC} (min), for -10 A.C. spec	3,4
			23	35	mA	t _{RC} = t _{RC} (min), for -12 A.C. spec.	
I _{DD2}	V _{DD} Supply Current, TTL Standby		0.7	2	mA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, RAS-Only Cycle		24	37	mA	t _{RC} = t _{RC} (min), for -10 A.C. spec	4
			20	35	mA	t _{RC} = t _{RC} (min), for -12 A.C. spec	
I _{DD4}	V _{DD} Supply Current, Ripplemode™		18	37	mA	t _{PC} = t _{PC} (min), for -10 A.C. spec	3,4
			17	35	mA	t _{PC} = t _{PC} (min), for -12 A.C. spec	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled		3	4	mA	$\overline{\text{RAS}}$ at V _{IH} , $\overline{\text{CAS}}$ at V _{IL} , all other inputs and output ≥ V _{SS}	3
I _{DD6}	V _{DD} Supply Current, CHMOS Standby		0.008	0.05	mA	$\overline{\text{RAS}} \geq V_{DD} - 0.5V$ and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{LI}	Input Load Current (any pin)			1	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current for High Impedance State			1	μA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	6
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -5 mA	6

NOTES:

1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and V_{DD} = +5V.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{\text{CAS}}$ is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Ripplemode.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Address, D_{IN}	3	4	pF
C_{IN2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

A.C. CHARACTERISTICS 1, 2, 3

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C64HL-10		51C64HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	100	75000	120	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	160		190		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{\text{CAS}}$ Hold Time	100		120		ns	
5	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
6	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		ns	
7	t_{CH2CL2}	t_{CP}	$\overline{\text{CAS}}$ Precharge Time	10		15		ns	
8	t_{CH2RL2}	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	-20		-20		ns	
9	t_{RL1CL2}	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	30	80	35	95	ns	4
10	t_{AVCL2}	t_{ASC}	Column Address Set-up Time	0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10		15		ns	
12	t_{RL1AX}	t_{AR}	Column Address Hold Time From $\overline{\text{RAS}}$	40		50		ns	
	t_{RVRV}	$t_{REF 1}$	Time Between Refresh		4		4	ms	5
	t_{RVRV}	$t_{REF 2}$	Time Between Refresh ($\overline{\text{RAS}}$ -Only)		64		64	ms	5
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6
13	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0	20	0	25	ns	
14	t_{CH2OZ}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	ns	

NOTES:

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).
- A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, V_L (min) $\geq V_{SS}$ and V_H (max) $\leq V_{DD}$.
- t_{RCD} (max) is specified for reference only.
- The 51C64HL extends the refresh period to 64 ms during $\overline{\text{RAS}}$ -Only refresh operation.
- t_T is measured between V_H (min) and V_L (max).

A.C. CHARACTERISTICS (Con't.)

Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64HL-10		51C64HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
15	t _{RL1QV}	t _{RAC}	Access Time From $\overline{\text{RAS}}$		100		120	ns	7
16	t _{CL1QV}	t _{CAC}	Access Time From $\overline{\text{CAS}}$		20		25	ns	8,9
17	t _{AVQV}	t _{CAA}	Access Time From Column Address		55		65	ns	9,10
18	t _{CL1CH1(F)}	t _{CAS(F)}	$\overline{\text{CAS}}$ Pulse Width (Read Cycle)	20	75000	25	75000	ns	
19	t _{CL1RH1(F)}	t _{RSH(F)}	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	10		10		ns	
20	t _{WH2CL2}	t _{RCS}	Read Command Set-up Time	0		0		ns	
21	t _{AVRH1}	t _{CAR}	Column Address to $\overline{\text{RAS}}$ Set-up Time	55		65		ns	
22	t _{CH2WX}	t _{RCH}	Read Com. Hold Time Ref. to $\overline{\text{CAS}}$	0		0		ns	11
23	t _{RH2WX}	t _{RRH}	Read Com. Hold Time Ref. to $\overline{\text{RAS}}$	10		10		ns	11

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64HL-10		51C64HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
24	t _{CL1RH1(W)}	t _{RSH(W)}	$\overline{\text{RAS}}$ Hold Time (Write Cycle)	35		40		ns	
25	t _{CL1CH1(W)}	t _{CAS(W)}	$\overline{\text{CAS}}$ Pulse Width (Write Cycle)	30	75000	35	75000	ns	
26	t _{WL1RH1}	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	30		35		ns	
27	t _{WL1CH1}	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	30		35		ns	
28	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	20		25		ns	
29	t _{WL1CL2}	t _{WCS}	Write Command Set-up Time	0		0		ns	12
30	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	30		35		ns	
31	t _{DVCL2}	t _{DS}	Data-In Set-up Time	0		0		ns	
32	t _{CL1DX}	t _{DH}	Data-In Hold Time	20		25		ns	

NOTES:

7. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$. If $t_{\text{RCD}} > t_{\text{RCD}}(\text{max})$ then t_{RAC} will increase by the amount that $t_{\text{RCD}}(\text{max})$.
8. Assumes $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
9. If $t_{\text{ASC}} < (t_{\text{CAA}}(\text{max}) - t_{\text{CAC}}(\text{max}) - t_{\text{T}})$, then access time is defined by t_{CAA} rather than by t_{CAC} .
10. When a Ripplemode read cycle immediately follows a Ripplemode write cycle, the specification must be increased by 10 ns.
11. Either t_{RCH} or t_{RRH} must be satisfied.
12. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are specified as reference points only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is a $\overline{\text{CAS}}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)
Read-Modify-Write Cycle 13

#	JEDEC Symbol	Symbol	Parameter	51C64HL-10		51C64HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
33	t _{RL2RL2(RMW)}	t _{RWC}	Read-Modify-Write (RMW) Cycle Time	195		230		ns	
34	t _{RL1RH1(RMW)}	t _{RRW}	RMW Cycle \overline{RAS} Pulse Width	135	75000	160	75000	ns	
35	t _{CL1CH1(RMW)}	t _{CRW}	RMW Cycle \overline{CAS} Pulse Width	55	75000	65	75000	ns	
36	t _{RL1WL2}	t _{RWD}	\overline{RAS} to \overline{WE} Delay	100		120		ns	14
37	t _{CL1WL2}	t _{CWD}	\overline{CAS} to \overline{WE} Delay	20		25		ns	14
38	t _{AWWL2}	t _{AWD}	Column Address to \overline{WE} Delay	55		65		ns	14

Ripplemode Cycle 15

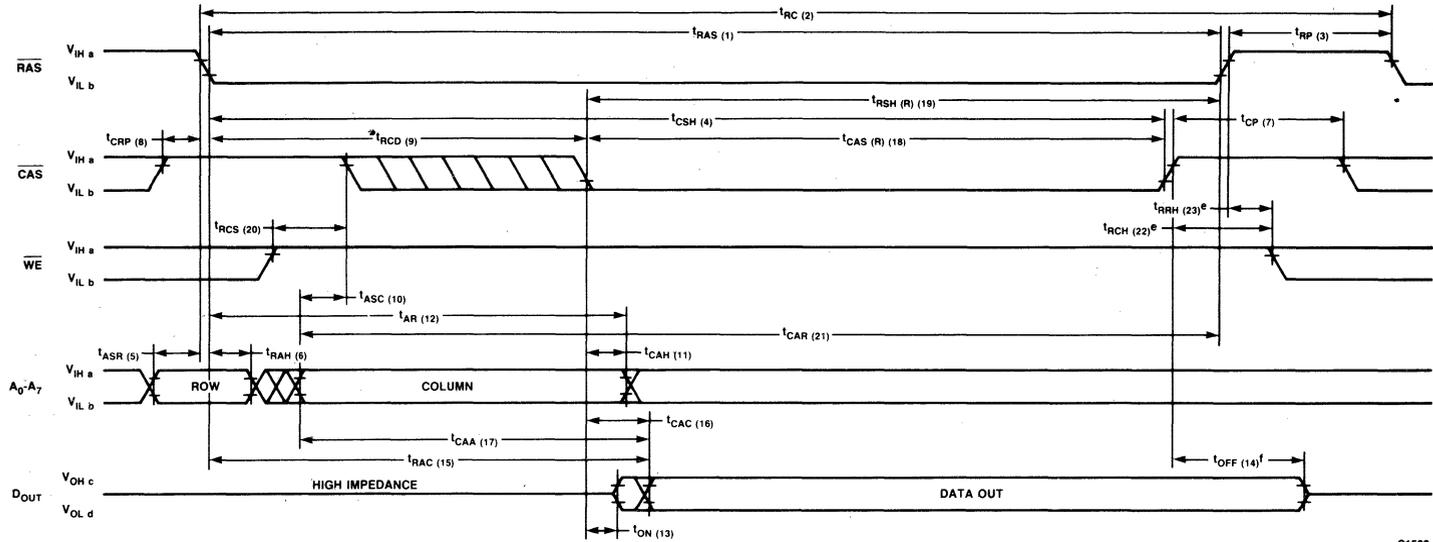
#	JEDEC Symbol	Symbol	Parameter	51C64HL-10		51C64HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
39	t _{CH2QV}	t _{CAP}	Access Time From Column Precharge		60		70	ns	16,17
40	t _{CL2CL2(R)}	t _{PC}	Ripplemode Read or Write Cycle	65		75		ns	16,17
41	t _{CL2CL2(RRMW)}	t _{PCM}	Ripplemode RMW Cycle Time	95		110		ns	

NOTES:

13. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
14. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS} (min), the cycle is a \overline{CAS} controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min) and t_{AWD} ≥ t_{AWD} (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.
15. All previously specified A.C. Characteristics are applicable.
16. Access time is determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.
17. When a Ripplemode read cycle immediately follows a Ripplemode write cycle, the specification must be increased by 10 ns.

WAVEFORMS

Read Cycle



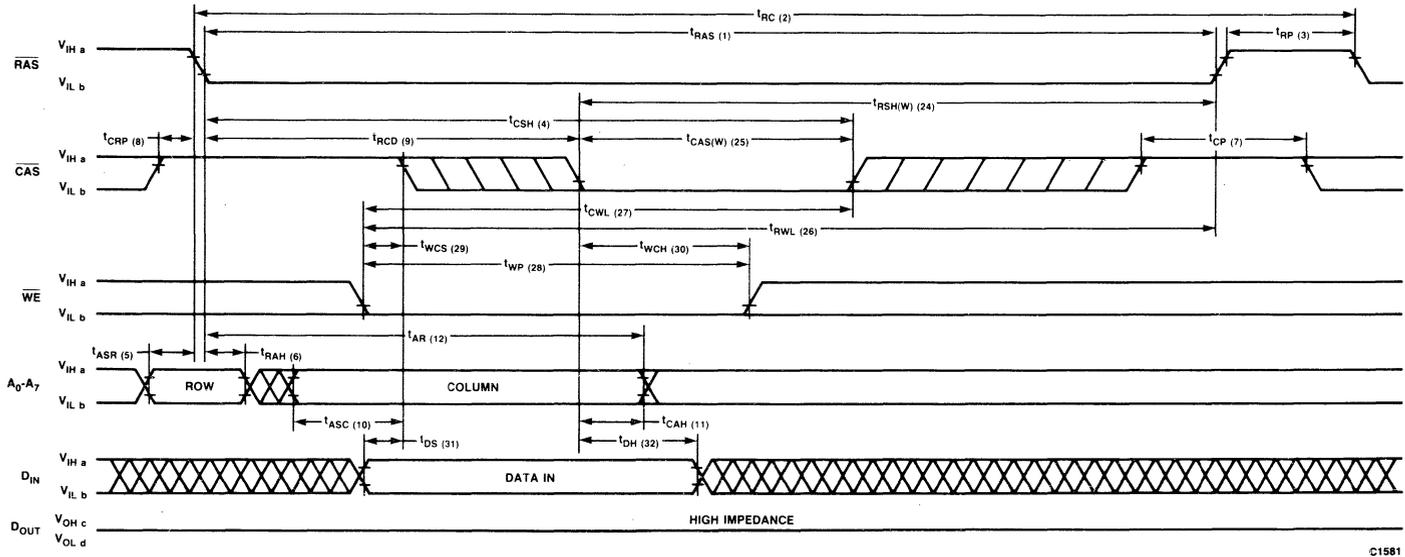
C1580

NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- Either t_{RCH} or t_{RRH} must be satisfied.
- t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)

Write Cycle ($\overline{\text{CAS}}$ Controlled)^e

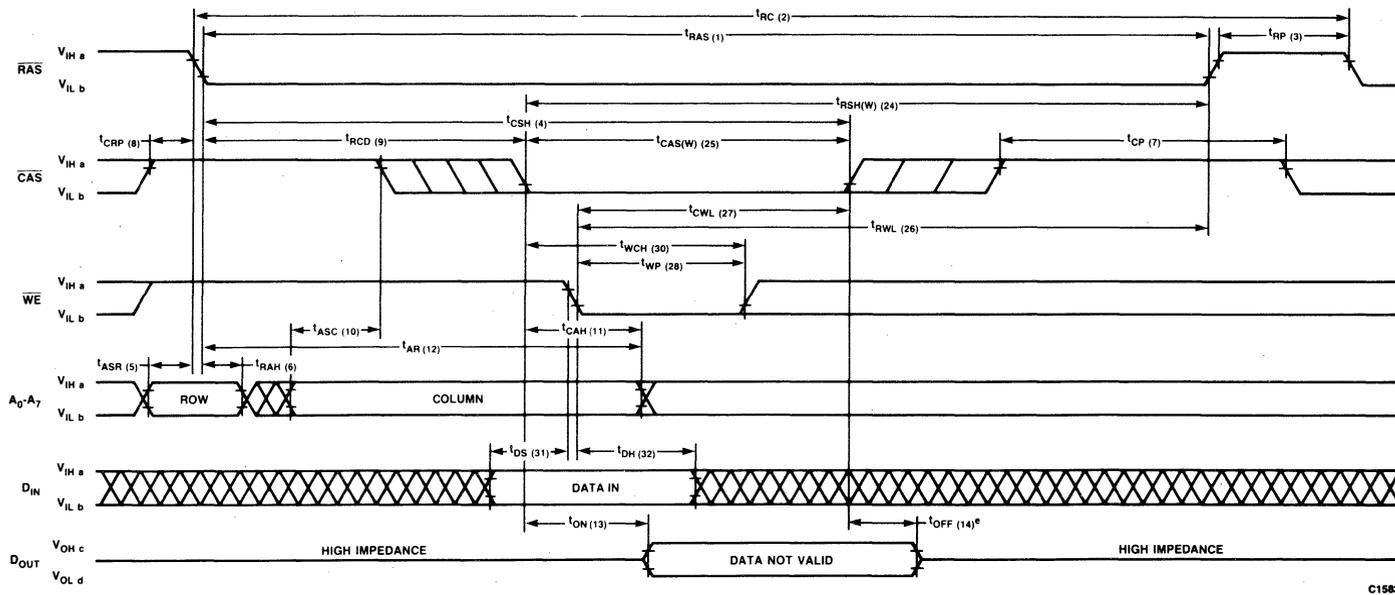


NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column address and data-in.

WAVEFORMS (Cont.)

Write Cycle (\overline{WE} Controlled)^f



2-42

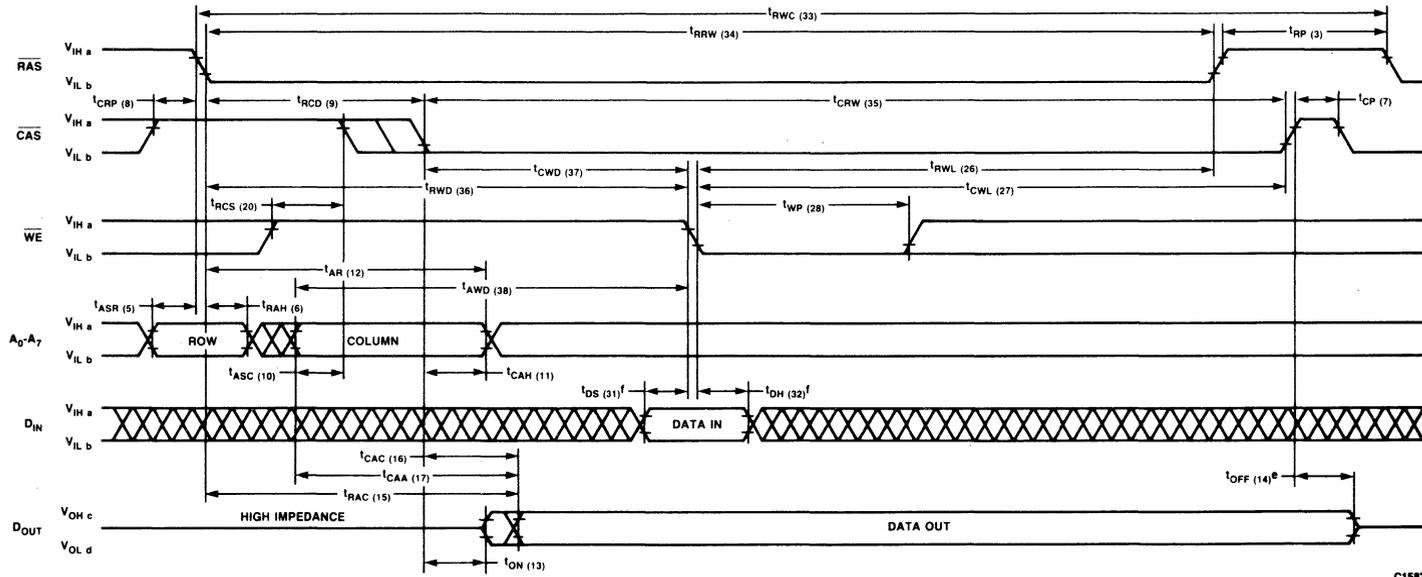
NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
- f. \overline{CAS} is low prior to the \overline{WE} low transition. \overline{CAS} latches the column address while \overline{WE} latches the data-in.

C1582

WAVEFORMS (Cont.)

Read/Modify/Write Cycle

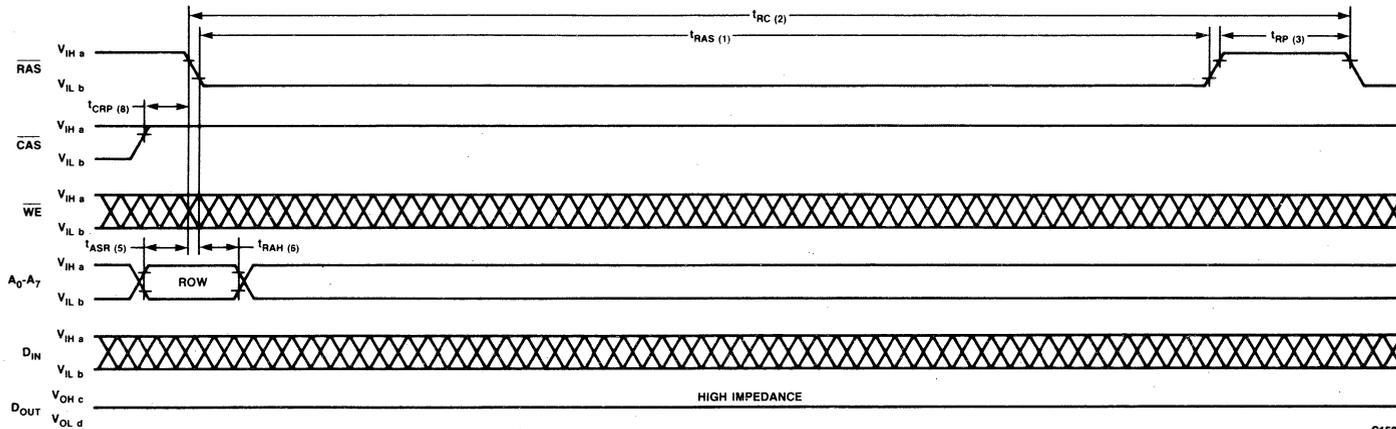


C1583

NOTES:

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- t_{OFF} is measured to $t_{OUT} \leq |t_{LO}|$.
- t_{DS} and t_{DH} are referenced to \overline{CAS} or \overline{WE} , whichever occurs last.

WAVEFORMS (Cont.)
RAS-Only Refresh Cycle



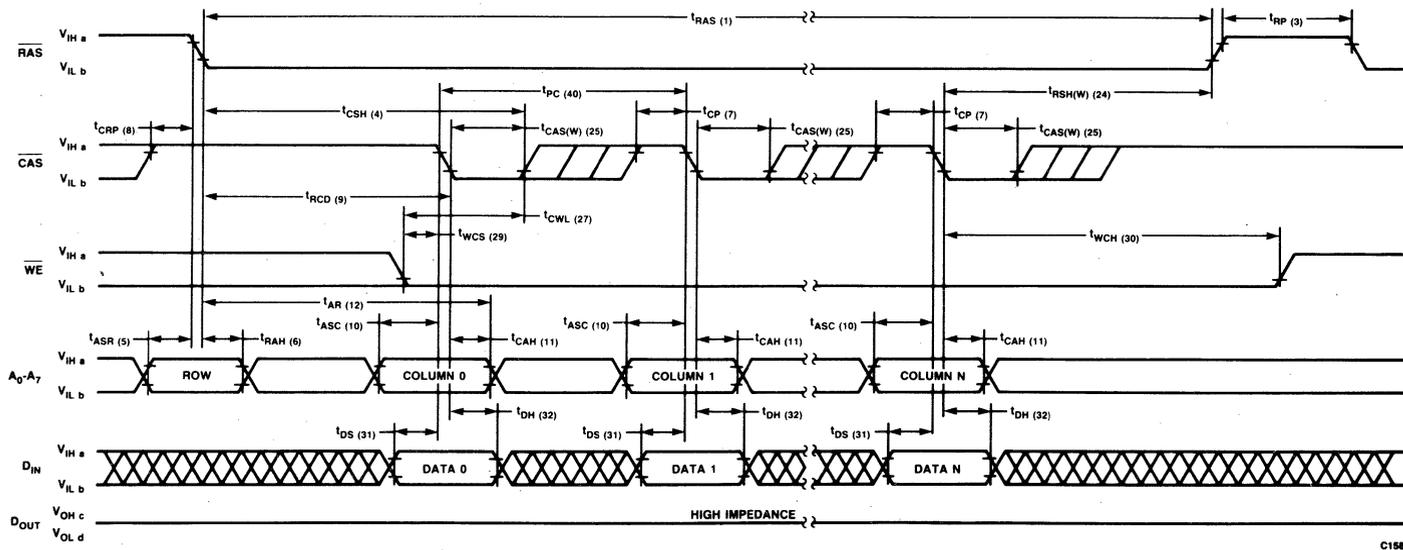
C1584

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

WAVEFORMS (Cont.)

Ripplemode Write Cycle (CAS Controlled)^e

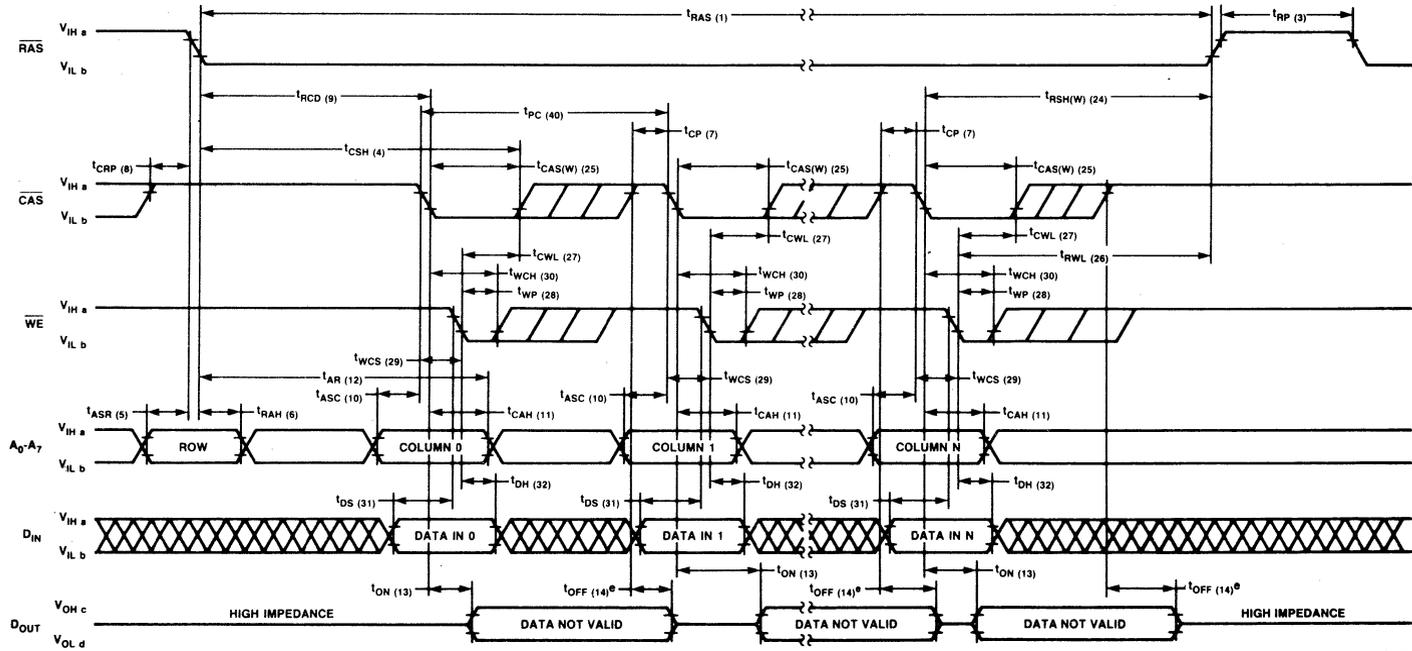


NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. \overline{WE} is low prior to or simultaneously with \overline{CAS} low transition. \overline{CAS} latches column address and data-in.

WAVEFORMS (Cont.)

Ripplemode Write Cycle (\overline{WE} Controlled)^f



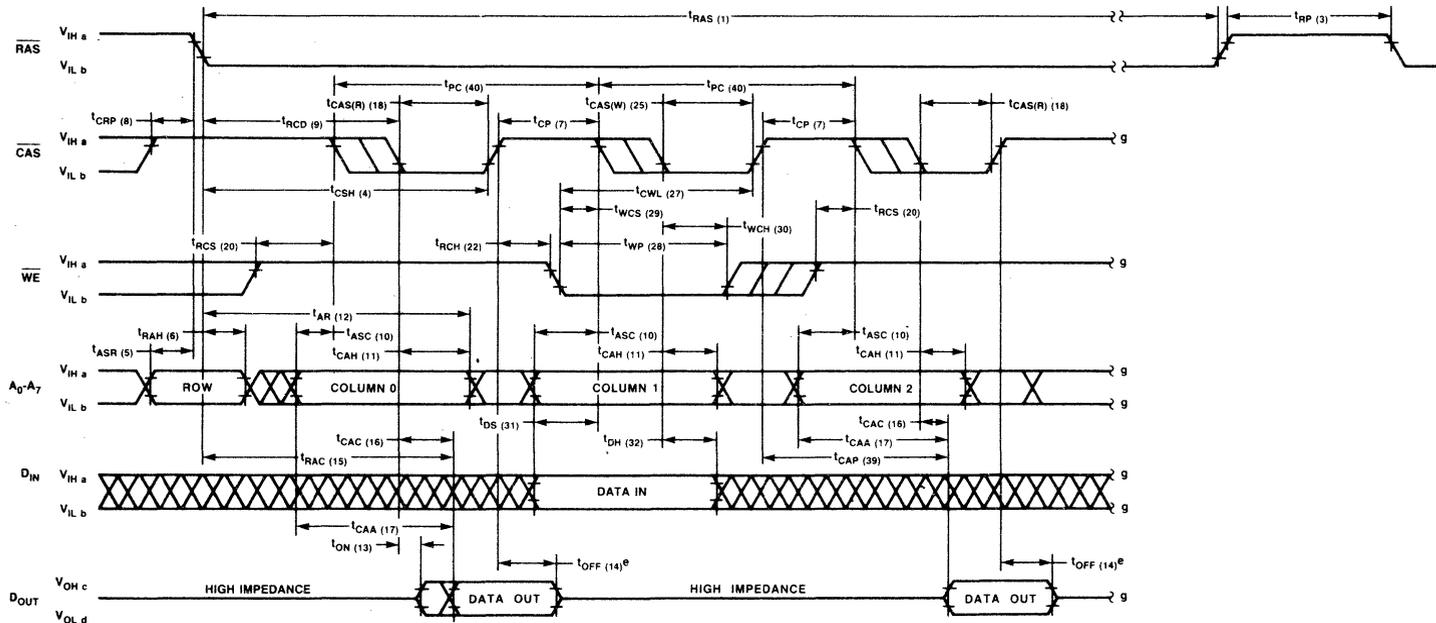
2-47

C1587

- NOTES:**
- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
 - f. \overline{CAS} is low prior to the \overline{WE} low transition. \overline{CAS} latches the column address while \overline{WE} latches the data-in.

WAVEFORMS

Ripplemode Read/Write/Read. . . Cycle ($\overline{\text{CAS}}$ Controlled)^f



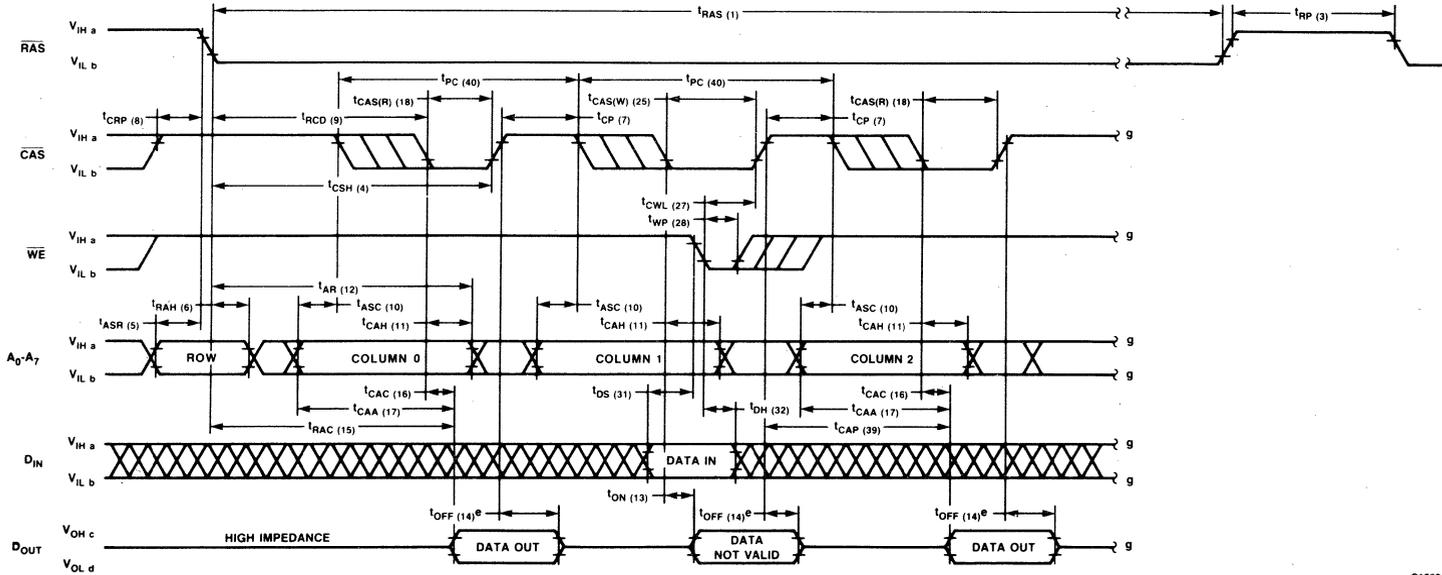
2-49

NOTES:

- a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
- c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
- e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
- f. $\overline{\text{WE}}$ is low prior to $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column addresses and data-in.
- g. The cycle can be terminated either by a read or a write operation followed by a $\overline{\text{RAS}}$ high transition. See page 11 or 12 for timings.

WAVEFORMS

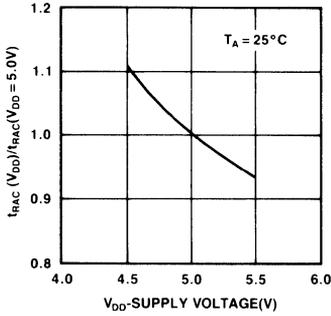
Ripplemode Read/Write/Read . . Cycle (\overline{WE} Controlled)^f



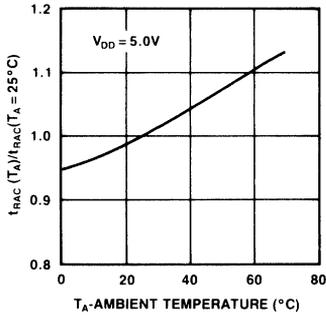
NOTES:

- $V_{IH} (min)$ and $V_{IL} (max)$ are reference levels for measuring timing of input signals.
- $V_{OH} (min)$ and $V_{OL} (max)$ are reference levels for measuring timing of D_{OUT} .
- t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
- CAS is low prior to WE low transition. CAS latches the column addresses while WE latches data-in.
- The cycle can be terminated either by a read or a write operation followed by a RAS high transition. See page 11 or 13 for timings.

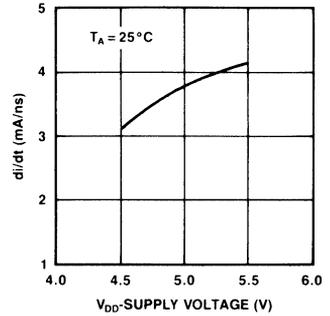
GRAPH 1
TYPICAL ACCESS TIME
 t_{RAC} (NORMALIZED) vs. V_{DD}



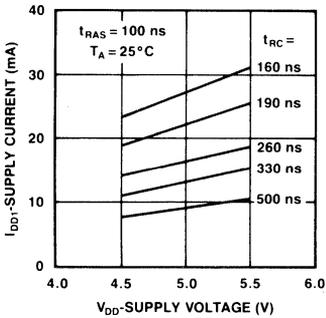
GRAPH 2
TYPICAL ACCESS TIME
 t_{RAC} (NORMALIZED) vs. T_A



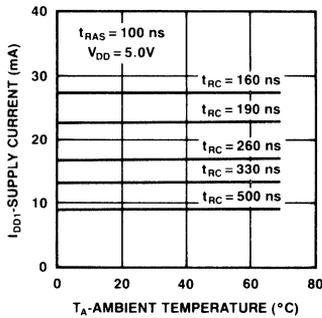
GRAPH 3
TYPICAL CURRENT TRANSIENTS
 di/dt vs. V_{DD}



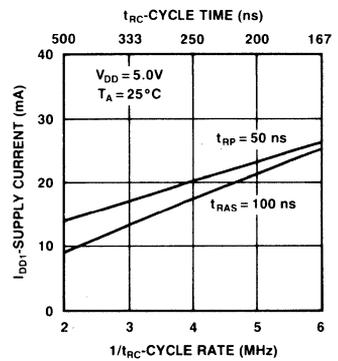
GRAPH 4
TYPICAL OPERATING CURRENT
 I_{DD1} vs. V_{DD}



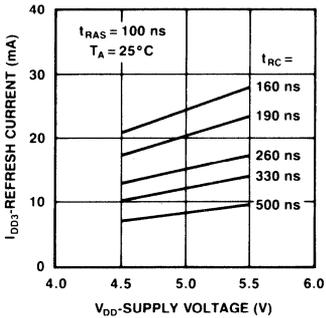
GRAPH 5
TYPICAL OPERATING CURRENT
 I_{DD1} vs. T_A



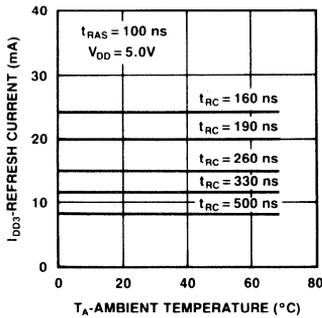
GRAPH 6
TYPICAL OPERATING CURRENT
 I_{DD1} vs. $1/t_{RC}$



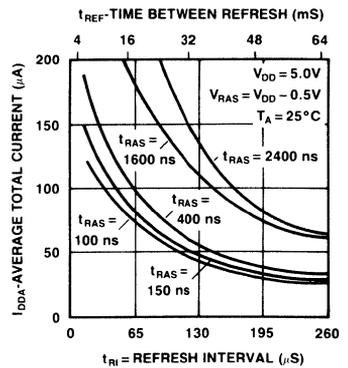
GRAPH 7
TYPICAL REFRESH CURRENT
 I_{DD3} vs. V_{DD}



GRAPH 8
TYPICAL REFRESH CURRENT
 I_{DD3} vs. T_A

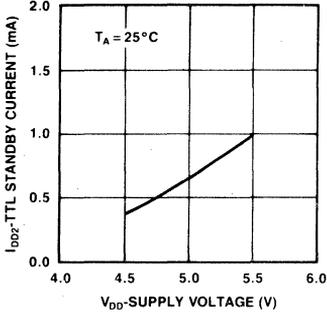


GRAPH 9
AVERAGE TOTAL CURRENT
 I_{DDA} vs. t_{RI} ($t_{REF}/256$)

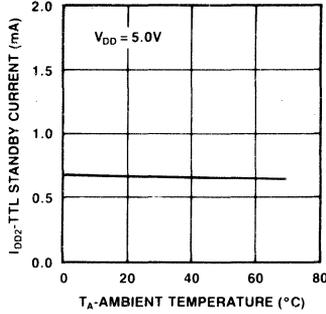


C14928

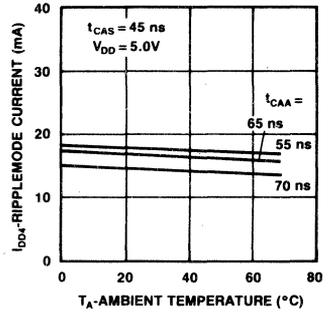
GRAPH 10
TYPICAL TTL STANDBY CURRENT
 I_{DD2} vs. V_{DD}



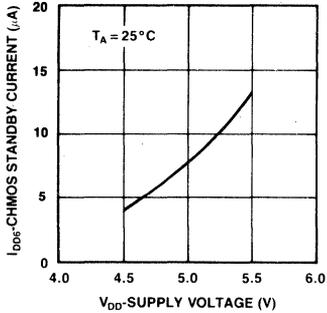
GRAPH 11
TYPICAL TTL STANDBY CURRENT
 I_{DD2} vs. T_A



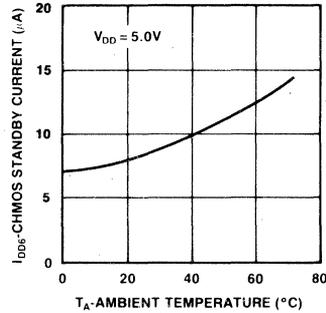
GRAPH 12
TYPICAL RIPPLEMODE CURRENT
 I_{DD4} vs. T_A



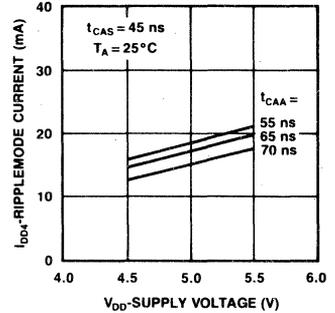
GRAPH 13
TYPICAL CHMOS STANDBY CURRENT
 I_{DD6} vs. V_{DD}



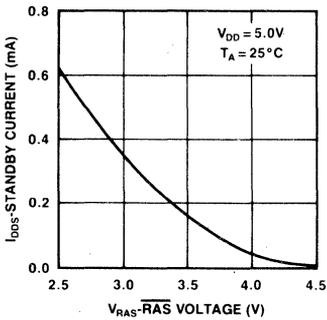
GRAPH 14
TYPICAL CHMOS STANDBY CURRENT
 I_{DD6} vs. T_A



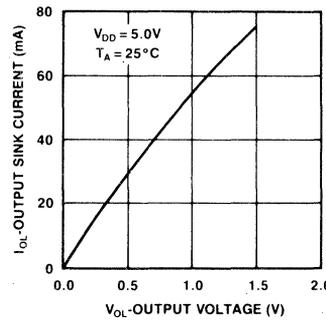
GRAPH 15
TYPICAL RIPPLEMODE CURRENT
 I_{DD4} vs. V_{DD}



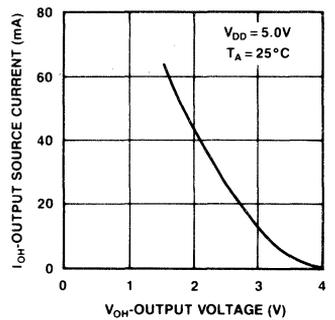
GRAPH 16
AVERAGE STANDBY CURRENT
RELATIVE TO RAS VOLTAGE
 I_{DD5} vs. V_{RAS}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
 I_{OL} vs. V_{OL}



GRAPH 18
TYPICAL OUTPUT SOURCE CURRENT
 I_{OH} vs. V_{OH}



FUNCTIONAL DESCRIPTION

The 51C64HL is a CHMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The 51C64HL reads and writes data by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe ($\overline{\text{RAS}}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{\text{CAS}}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ operation. The column address must be held for a minimum time specified by t_{AR} . Data out becomes valid only when t_{RAC} , t_{CAA} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ low during a $\overline{\text{RAS}}$ operation. The column address is latched in by $\overline{\text{CAS}}$. The write cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending upon the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. In a $\overline{\text{CAS}}$ controlled write cycle (the leading edge of $\overline{\text{WE}}$ occurs prior to or coincident with the $\overline{\text{CAS}}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ will maintain the output in the high impedance state; terminating with $\overline{\text{WE}}$ allows the output to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{\text{RAS}}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{\text{RAS}}$ -Only cycle will perform refresh.

Extended Refresh Cycle

The 51C64HL extends the refresh cycle period to 64 milliseconds for $\overline{\text{RAS}}$ -Only refresh cycles. This feature reduces the total current consumption to a maximum of 80 micro Amperes, and typically 15 micro Amperes, for data retention ($\overline{\text{RAS}}$ -Only refresh operation for the 51C64HL-12). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{\text{RC}} I_{\text{ACTIVE}}) + (t_{\text{RI}} - t_{\text{RC}}) I_{\text{STANDBY}}}{t_{\text{RI}}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{\text{REF}}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Ripplemode™ Operation

Ripplemode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{\text{RAS}}$ low while successive $\overline{\text{CAS}}$ cycles are performed, retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{\text{CAS}}$ is high. Access begins from the valid column address rather than from $\overline{\text{CAS}}$, eliminating t_{ASC} and t_{T} from the critical timing path. $\overline{\text{CAS}}$ latches the addresses into the column address buffer and acts as an output enable.

During this operation read, write, read-modify-write, or read-write-read cycles are possible at random or sequential addresses within a row. Following the entry cycle into Ripplemode operation, access time is t_{CAA} or t_{CAP} dependent. If the column address is valid prior to or coincident with the rising edge of $\overline{\text{CAS}}$, then the access time is determined by the rising edge of $\overline{\text{CAS}}$ specified by t_{CAP} as shown in Figure 1. If the column address is valid after the rising edge of $\overline{\text{CAS}}$, then the access time is determined by the valid column address specified by t_{CAA} . For both cases, the falling edge of $\overline{\text{CAS}}$ latches the address and enables the output.

Ripplemode operation provides a sustained data rate over 15 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{256}{t_{\text{RC}} + 255t_{\text{PC}}}$$

Data Out Operation

The 51C64HL Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{\text{CAS}}$. During $\overline{\text{CAS}}$ high

state ($\overline{\text{CAS}}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).

The V_{DD} current (I_{DD}) requirement of the 51C64HL during power on is dependent upon the input levels of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. If $\overline{\text{RAS}} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{DD} or be held at a valid V_{IH} during power on.

Soft Error Rate

Soft errors are random, non-recurring changes in memory logic states caused by the impact of an ionizing particle, such as an alpha particle. For example, a logic "0" may change to a logic "1." The average soft error rate (SER) of the 51C64HL is less than 10 FITs. This is determined by accelerated testing using an alpha particle source and is subsequently confirmed by system testing. The SER is a function of the operating voltage, cycle time, package, and the alpha particle source. Intel measures the SER at $V_{DD} = 4.75\text{V}$, and $t_{\text{cycle}} = 1\mu\text{s}$. A thorium source of $1.6 \times 10^5 \alpha/\text{cm}^2/\text{hr.}$ is used because it best matches the package energy spectra.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

Table 1. Intel 51C64HL Data Output Operation for Various Types of Cycles

Type of Cycle	Data Out State
Read Cycle	Data from Addressed Memory Cell
$\overline{\text{CAS}}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{\text{WE}}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{\text{CAS}}$ Controlled)	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{\text{WE}}$ Controlled)	Data from Addr. Memory Cell and Active, Not Valid
$\overline{\text{RAS}}$ -Only Refresh Cycle	High Impedance
$\overline{\text{CAS}}$ -Only Cycle	High Impedance

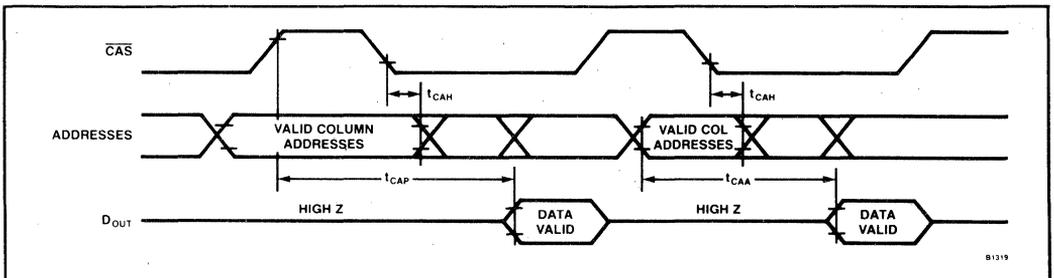


Figure 1. Ripplemode™ Access Time Determination

51C256H HIGH PERFORMANCE RIPPLEMODE™ 256K X 1 CHMOS DYNAMIC RAM

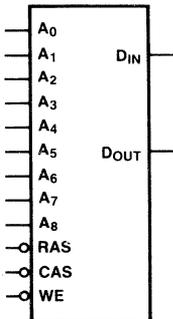
	51C256H-12†	51C256H-15	21C256H-20
Maximum Access Time (ns)	120	150	200
Maximum Column Address Access Time (ns)	55	70	90
Ripplemode Cycle Time (ns)	65	80	100

- **Ripplemode Operation**
 - Continuous data rate over 15 MHz
 - Random access within a row
 - Flow through column latch for pipelining
- **Fast “Usable Speed”**
 - $t_{RC} = 200$ ns
 - $t_{CAC} = 25$ ns
 - $t_{RCD} = 30$ ns min./95 ns max.
- **Low Operating Power – 70 mA**
- **Fully TTL Compatible**
- **Low Input/Output Capacitance**
- **High Reliability Plastic — 16 Pin DIP**

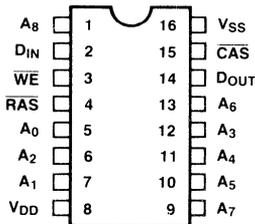
The Intel® 51C256H is a high speed 262,144 × 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C256H offers features not provided by an NMOS dynamic RAM: Ripplemode for high data bandwidth and fast usable speed. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

Ripplemode operation allows random or sequential access of up to 512 bits within a row, with cycle times as fast as 65 ns. Because of static column circuitry, the \overline{CAS} clock is no longer in the critical timing path. The flow through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the 51C256H ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance microprocessor systems.

LOGIC SYMBOL



PIN CONFIGURATION



PIN NAMES

\overline{RAS}	ROW ADDRESS STROBE
\overline{CAS}	COLUMN ADDRESS STROBE
\overline{WE}	WRITE ENABLE
A_0-A_8	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+ 5V)
V_{SS}	GROUND

†Available 1Q 1985

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under

Bias -10°C to +80°C

Storage Temperature . . Plastic -55°C to +125°C

 Voltage on Any Pin except V_{DD} and D_{OUT}

 Relative to V_{SS} -2.0V to 7.5V

 Voltage on V_{DD} Relative to V_{SS} . . . -1.0V to 7.5V

 Voltage on D_{OUT}

 Relative to V_{SS} -2.0V to V_{DD}+1V

Data Out Current 50 mA

Power Dissipation 1.0W

†COMMENT

Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

 T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C256H			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating		53	70	mA	t _{RC} = t _{RC} (min), for -12 specification	3,4
			48	65	mA	t _{RC} = t _{RC} (min), for -15 specification	
			35	50	mA	t _{RC} = t _{RC} (min), for -20 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby		1	4	mA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, RAS-Only Refresh		53	70	mA	t _{RC} = t _{RC} (min), for -12 specification	4
			45	65	mA	t _{RC} = t _{RC} (min), for -15 specification	
			35	50	mA	t _{RC} = t _{RC} (min), for -20 specification	
I _{DD4}	V _{DD} Supply Current, Ripplemode		26	70	mA	t _{PC} = t _{PC} (min), for -12 specification	3,4
			22	65	mA	t _{PC} = t _{PC} (min), for -15 specification	
			18	50	mA	t _{PC} = t _{PC} (min), for -20 specification	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled		3	6	mA	$\overline{\text{RAS}}$ at V _{IH} , $\overline{\text{CAS}}$ at V _{IL} , all other inputs and output ≥ V _{SS}	3
I _{LI}	Input Load Current (any pin)			10	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current for High Impedance State			10	μA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2mA	6
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -5mA	6

NOTES:

- All voltages referenced to V_{SS}.
- Typical values are at T_A = 25°C and V_{DD} = +5V.
- I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
- I_{DD} is dependent upon the number of address transitions while $\overline{\text{CAS}}$ is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Ripplemode.
- Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
- Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	5	pF
C_{IN2}	\overline{RAS} , \overline{CAS} , \overline{WE}	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS^{1,2,3}

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C256H-12		51C256H-15		51C256H-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	\overline{RAS} Pulse Width	120	75000	150	75000	200	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	200		245		315		ns	
3	t_{RH2RL2}	t_{RP}	\overline{RAS} Precharge Time	70		85		105		ns	
4	t_{RL1CH1}	t_{CSH}	\overline{CAS} Hold Time	120		150		200		ns	
5	t_{CL1CH1}	t_{CAS}	\overline{CAS} Pulse Width	25	75000	30	75000	35	75000	ns	
6	t_{WH2RL2}	t_{WRP}	Write to \overline{RAS} Precharge Time	10		10		10		ns	
7	t_{RL1WL2}	t_{RWH}	\overline{RAS} to Write Hold Time	15		20		25		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		20		25		ns	
10	t_{CH2CL2}	t_{CP}	\overline{CAS} Precharge Time	10		10		10		ns	
11	t_{CH2RL2}	t_{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	-20		-20		-20		ns	
12	t_{RL1CL1}	t_{RCD}	\overline{RAS} to \overline{CAS} Delay	30	95	35	120	40	165	ns	4
13	t_{AVCL2}	t_{ASC}	Column Address Set-up Time	5		5		5		ns	
14	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		20		25		ns	
15	t_{RL1AX}	t_{AR}	Col. Address Hold Time From \overline{RAS}	60		70		80		ns	
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4		4	ms	
	t_T	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	5
16	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0	25	0	30	0	35	ns	
17	t_{CH2QZ}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	0	30	ns	

NOTES:

1. All voltages referenced to V_{SS} .
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a \overline{RAS} clock such as \overline{RAS} -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).
3. A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, $V_{IL}(\text{min}) \geq V_{SS}$ and $V_{IH}(\text{max}) \leq V_{DD}$.
4. $t_{RCD}(\text{max})$ is specified for reference only.
5. t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

A.C. CHARACTERISTICS (Con't.)

Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256H-12		51C256H-15		51C256H-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
18	t _{RL1QV}	t _{RAC}	Access Time From $\overline{\text{RAS}}$		120		150		200	ns	6
19	t _{CL1QV}	t _{CAC}	Access Time From $\overline{\text{CAS}}$		25		30		35	ns	7,8
20	t _{AVQV}	t _{CAA}	Access Time From Column Address		55		70		90	ns	8
21	t _{CL1RH1(R)}	t _{RSH(R)}	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	10		10		10		ns	
22	t _{WH2CL2}	t _{RCS}	Read Command Set-up Time	0		0		0		ns	
23	t _{AVRH1}	t _{CAR}	Column Address to $\overline{\text{RAS}}$ Set-up Time	55		70		90		ns	
24	t _{CH2WX}	t _{RCH}	Read Com. Hold Time Referenced to $\overline{\text{CAS}}$	0		0		0		ns	9
25	t _{RH2WX}	t _{RRH}	Read Com. Hold Time Referenced to $\overline{\text{RAS}}$	10		10		10		ns	9

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256H-12		51C256H-15		51C256H-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
26	t _{CL1RH1(W)}	t _{RSH(W)}	$\overline{\text{RAS}}$ Hold Time (Write Cycle)	25		30		35		ns	
27	t _{WL1RH1}	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	25		30		35		ns	
28	t _{WL1CH1}	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	25		30		35		ns	
29	t _{WL1WH1}	t _{WHP}	Write Command Pulse Width	20		25		30		ns	
30	t _{WL1CL2}	t _{WCS}	Write Command Set-up Time	0		0		0		ns	10
31	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	25		30		35		ns	
32	t _{DVCL2}	t _{DS}	Data-In Set-up Time	0		0		0		ns	
33	t _{CL1DX}	t _{DH}	Data-In Hold Time	20		25		30		ns	

NOTES:

6. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If $t_{RCD} > t_{RCD}(\text{max})$, then t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{RCD}(\text{max})$.
7. Assumes $t_{RCD} \geq t_{RCD}(\text{max})$.
8. If $t_{ASC} < (t_{CAA}(\text{max}) - t_{CAC}(\text{max}) - t_r)$, then access time is defined by t_{CAA} rather than by t_{CAC} .
9. Either t_{RCH} or t_{RRH} must be satisfied.
10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is a $\overline{\text{CAS}}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)

Read-Modify-Write Cycle¹¹

#	JEDEC Symbol	Symbol	Parameter	51C256H-12		51C256H-15		51C256H-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
34	t _{RL2RL2} (RMW)	t _{RWC}	Read-Modify-Write (RMW) Cycle Time	230		280		355		ns	
35	t _{RL1RH1} (RMW)	t _{RRW}	RMW Cycle \overline{RAS} Pulse Width	150		185		240		ns	
36	t _{CL1CH1} (RMW)	t _{CRW}	RMW Cycle \overline{CAS} Pulse Width	55		65		75		ns	
37	t _{RL1WL2}	t _{RWD}	\overline{RAS} to \overline{WE} Delay	120		150		200		ns	12
38	t _{CL1WL2}	t _{CWD}	\overline{CAS} to \overline{WE} Delay	25		30		35		ns	12
39	t _{AVWL2}	t _{AWD}	Column Address to \overline{WE} Delay	55		70		90		ns	12

Ripplemode Cycle¹³

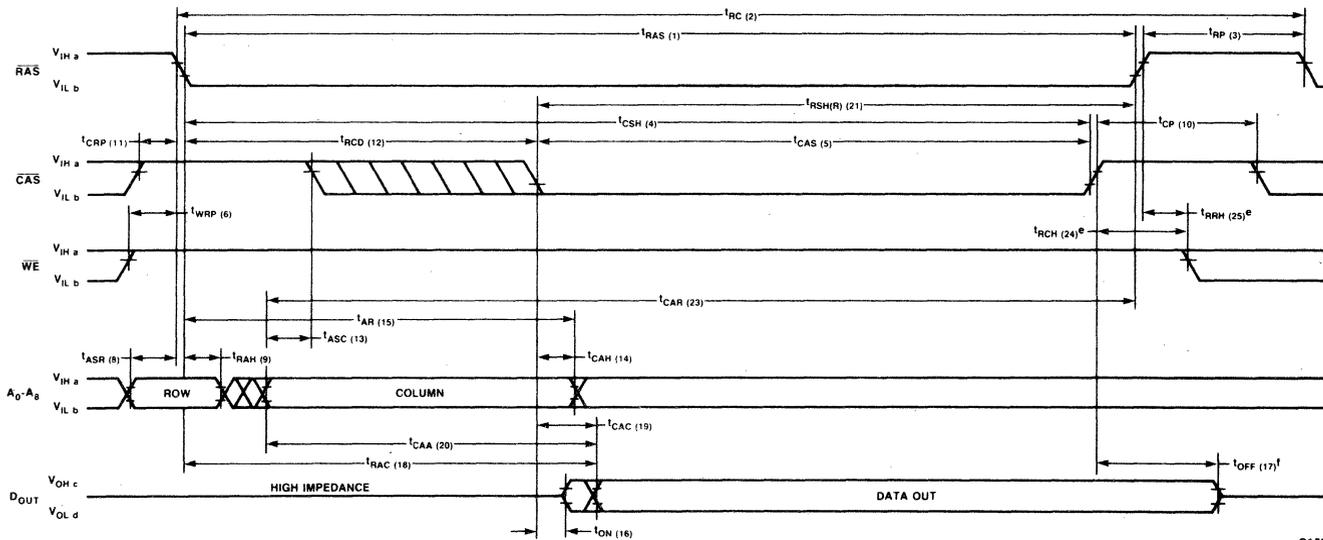
#	JEDEC Symbol	Symbol	Parameter	51C256H-12		51C256H-15		51C256H-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
40	t _{CH2QV}	t _{CAP}	Access Time From Column Precharge		60		75		95	ns	14
41	t _{CL2CL2(R)}	t _{PC}	Ripplemode Read or Write Cycle	65		80		100		ns	14
42	t _{CL2CL2(RRMW)}	t _{PCM}	Ripplemode RMW Cycle Time	90		110		135		ns	

NOTES:

11. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS} (min), the cycle is a \overline{CAS} controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min) and t_{AWD} ≥ t_{AWD} (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.
13. All previously specified A.C. Characteristics are applicable.
14. Access time is determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.

WAVEFORMS

Read Cycle



C1590

NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

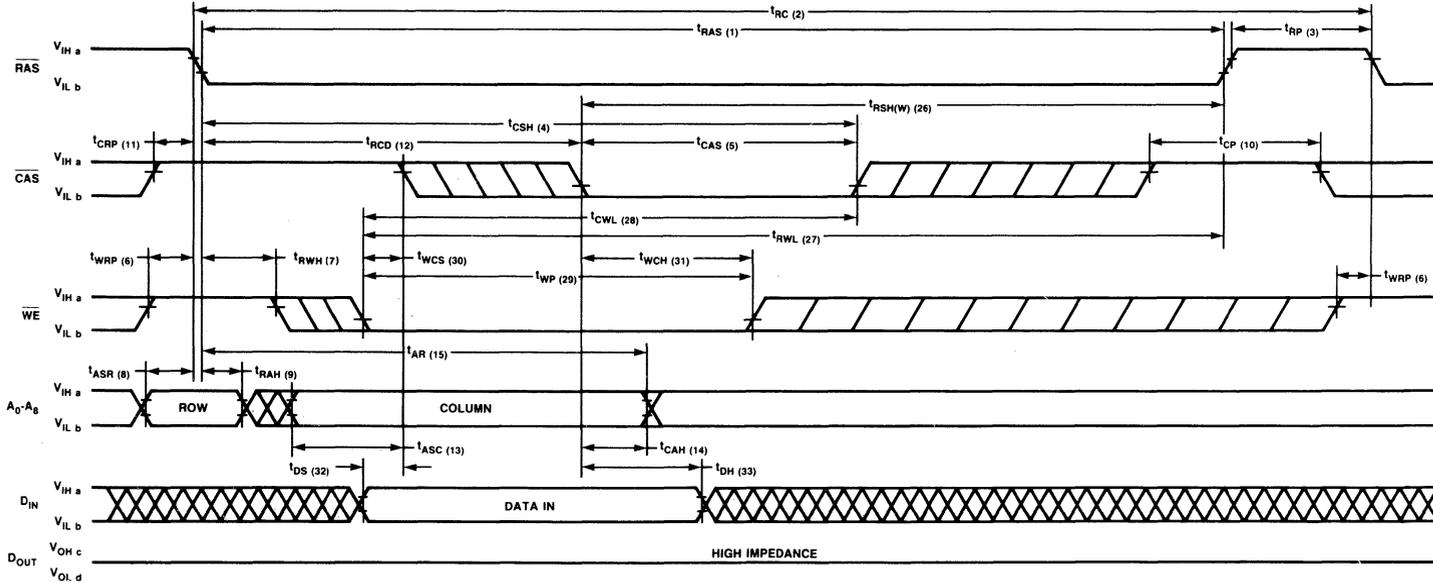
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

e. Either t_{RCH} or t_{RRH} must be satisfied.

f. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)

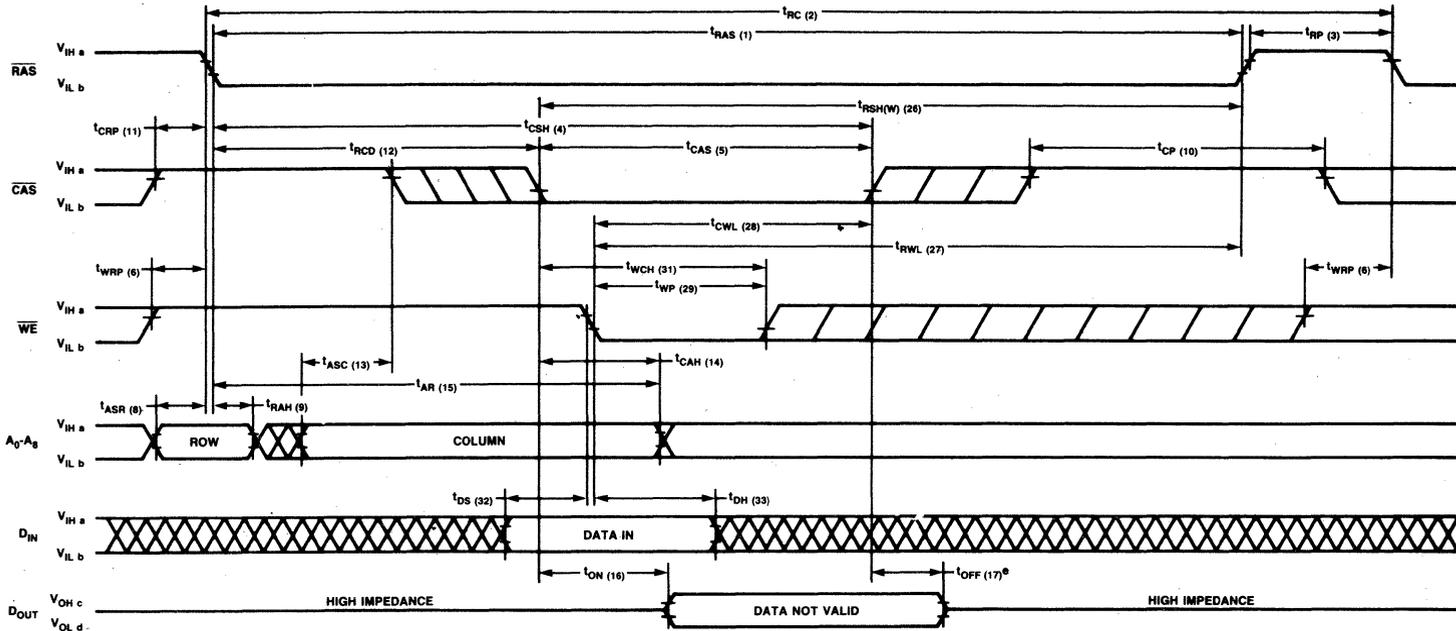
Write Cycle ($\overline{\text{CAS}}$ Controlled)^e



- NOTES:** a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column address and data-in.

WAVEFORMS (Cont.)

Write Cycle (WE Controlled)^f



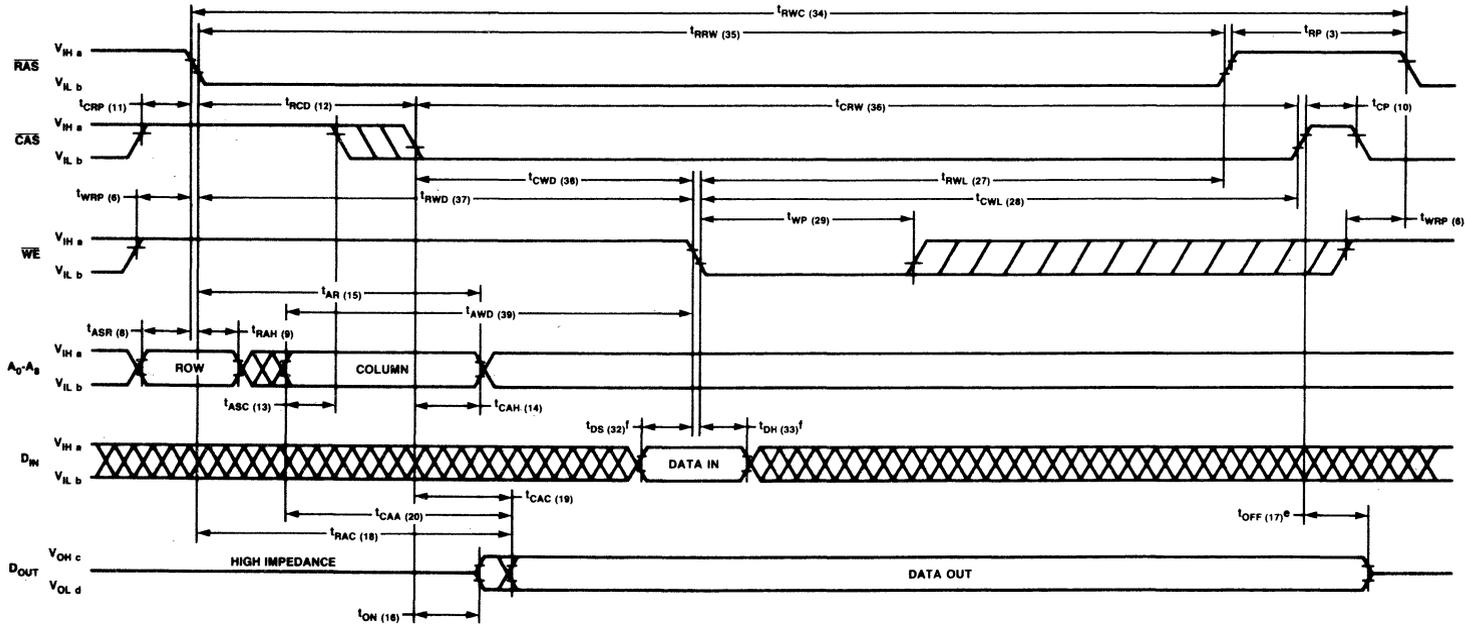
2-62

- NOTES:** a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{OL}|$.
 f. CAS is low prior to the WE low transition. CAS latches the column address while WE latches the data-in.

C1592

WAVEFORMS (Cont.)

Read/Modify/Write Cycle

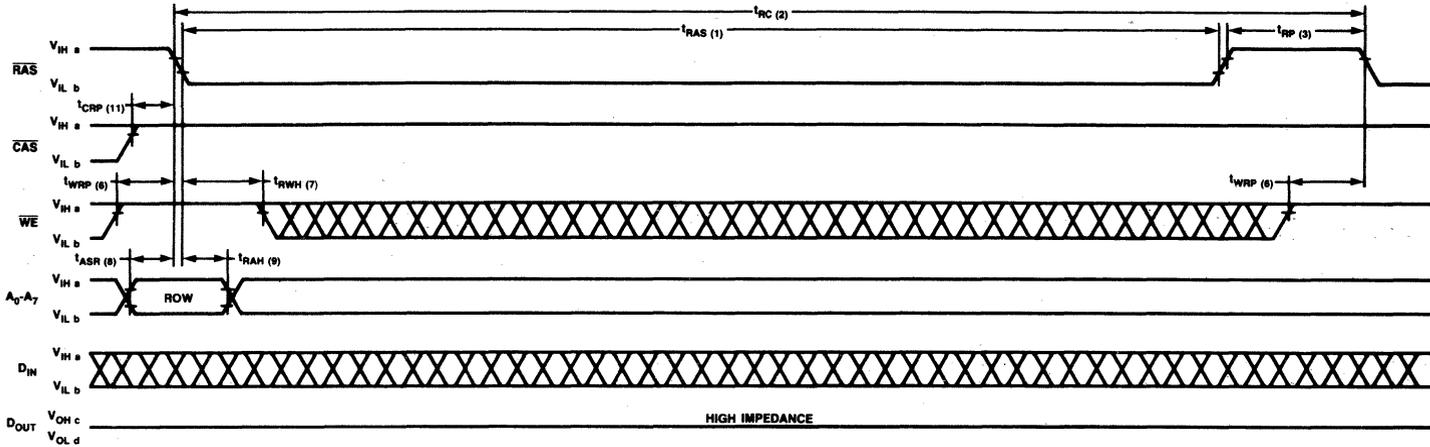


C1593

- NOTES:**
- a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
 - f. t_{DS} and t_{DH} are referenced to \overline{CAS} or \overline{WE} , whichever occurs last.

2-63

WAVEFORMS (Cont.)
RAS-Only Refresh Cycle



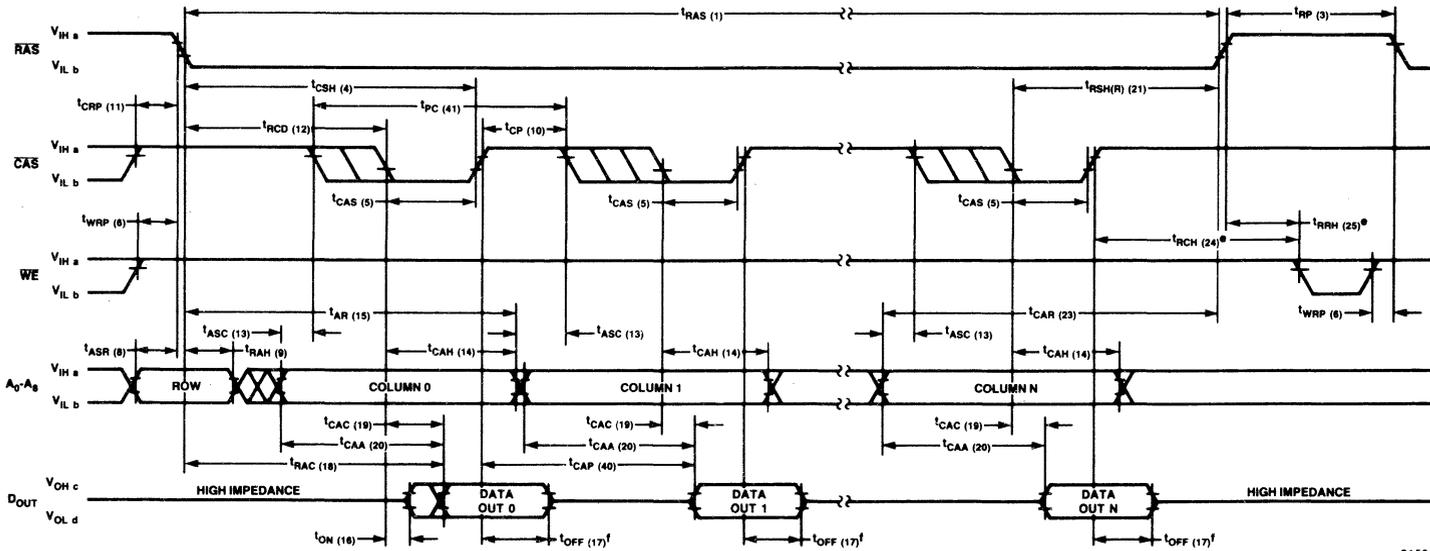
2-64

NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

C1594

WAVEFORMS (Cont.)

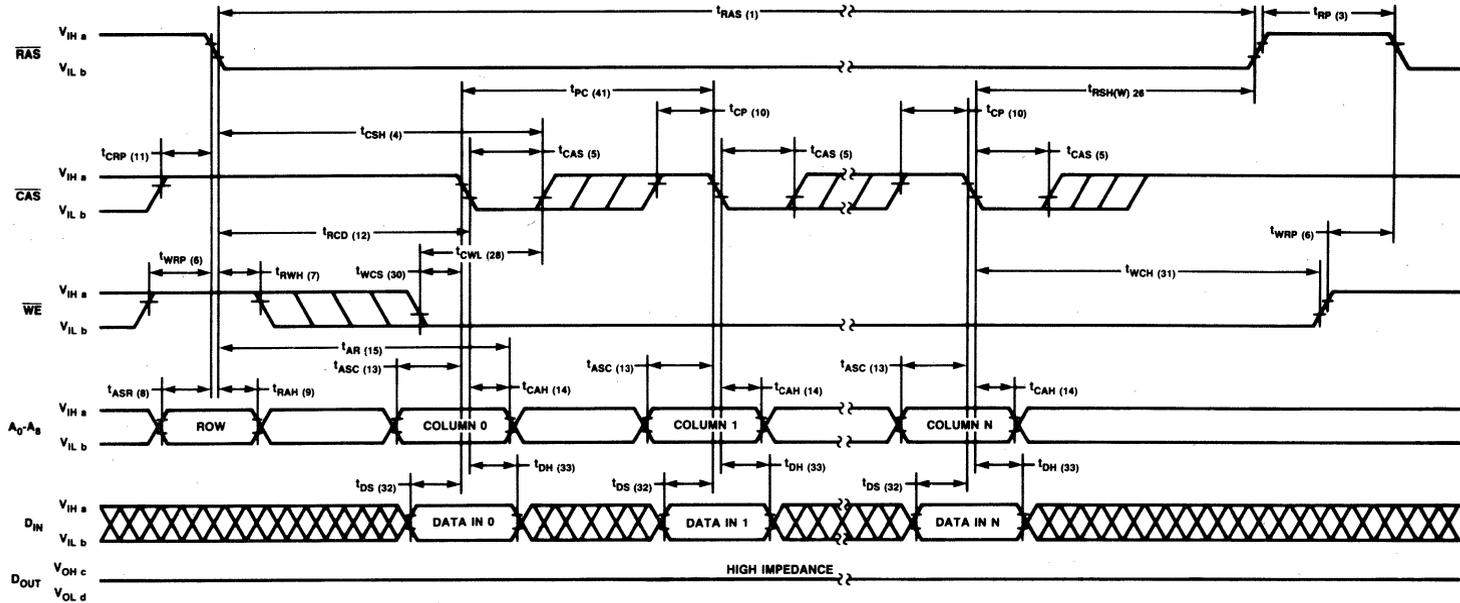
Ripplemode Read Cycle



- NOTES:**
- a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
 - e. Either t_{RCH} or t_{RRH} must be satisfied.
 - f. t_{OFF} is measured to t_{OUT} ≤ |L_O|.

WAVEFORMS (Cont.)

Ripplemode Write Cycle ($\overline{\text{CAS}}$ Controlled)^e



2-66

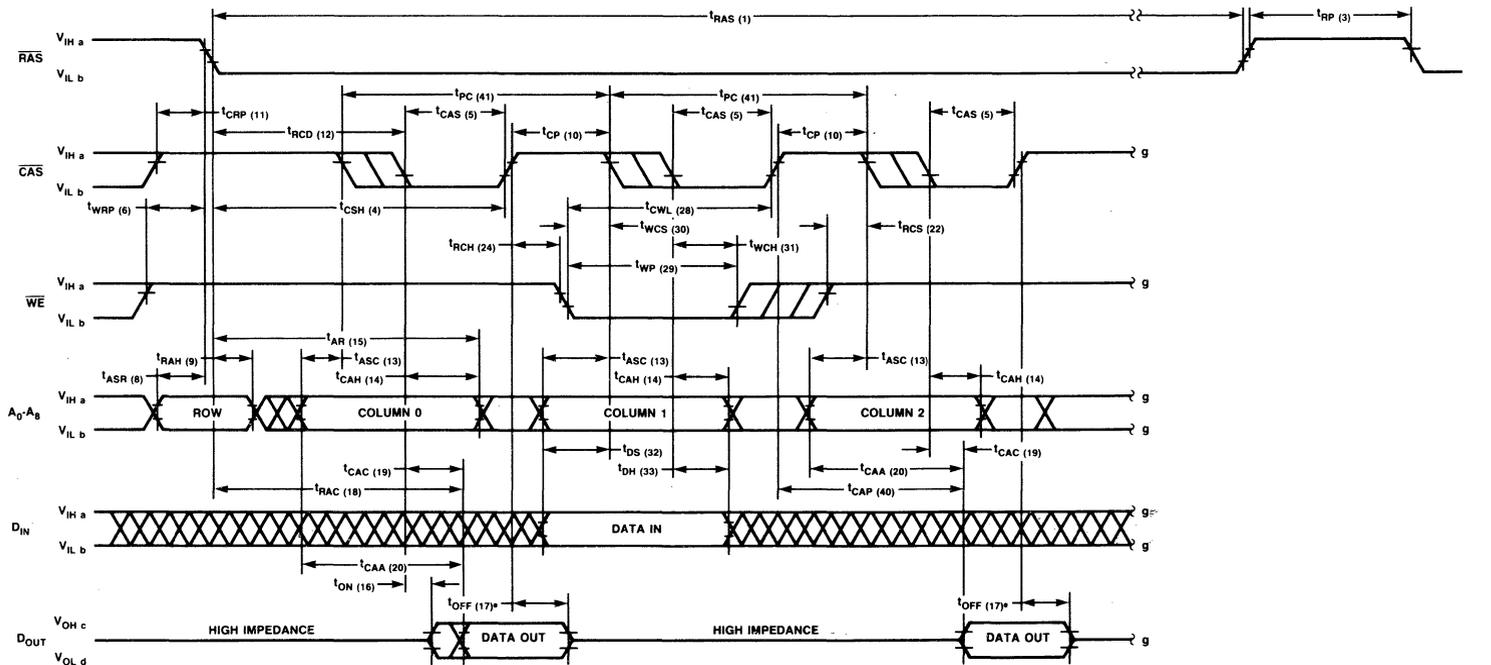
- NOTES:** a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column addresses and data-in.

C1596

WAVEFORMS (Cont.)

Ripplemode Read/Write/Read/. . . Cycle ($\overline{\text{CAS}}$ Controlled)^f

2-69



C1598

NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

e. t_{OFF} is measured to $I_{OUT} \leq |I_{OL}|$.

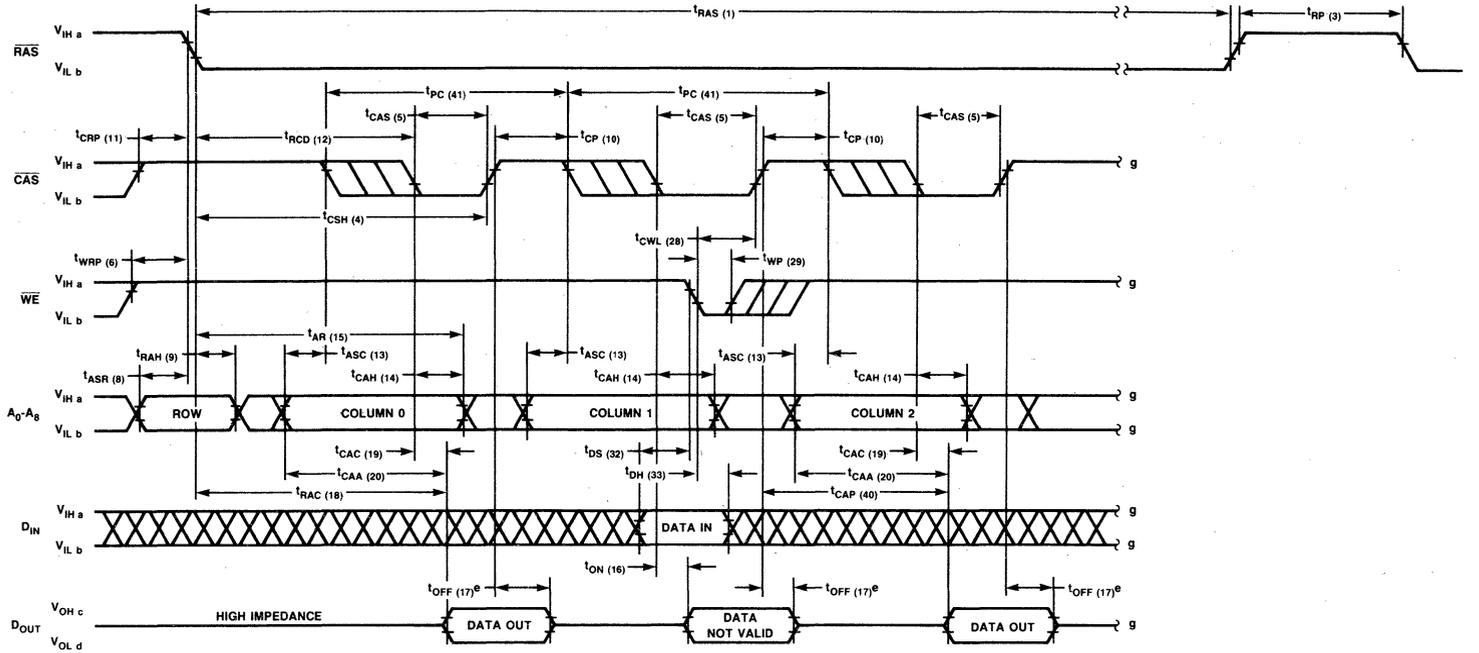
f. $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column addresses and data-in.

g. The cycle can be terminated either by a read or a write operation followed by a $\overline{\text{RAS}}$ high transition. See page 11 or 12 for timings.

WAVEFORMS (Cont.)

Ripplemode Read/Write/Read/. . . Cycle (\overline{WE} Controlled)^f

2-70



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

e. t_{OFF} is measured to $I_{OUT} \leq |I_{IO}|$.

f. CAS is low prior to WE low transition. CAS latches the column addresses while WE latches data-in.

g. The cycle can be terminated either by a read or a write operation followed by a RAS high transition. See page 11 or 13 for timings.

C1599

FUNCTIONAL DESCRIPTION

The 51C256H is a CHMOS dynamic RAM optimized for high data bandwidth applications. The functionality is similar to a traditional dynamic RAM. The 51C256H reads and writes data by multiplexing an 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched in by the Row Address Strobe ($\overline{\text{RAS}}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{\text{CAS}}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}/\overline{\text{CAS}}$ operation. The column address must be held for a minimum time specified by t_{AR} . Data out becomes valid only when t_{RAC} , t_{CAA} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ low during a $\overline{\text{RAS}}$ operation. The column address is latched in by $\overline{\text{CAS}}$. The write cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending upon the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. In a $\overline{\text{CAS}}$ controlled write cycle (the leading edge of $\overline{\text{WE}}$ occurs prior to or coincident with the $\overline{\text{CAS}}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ will maintain the output in the high impedance state; terminating with $\overline{\text{WE}}$ allows the output to go active.

The 51C256H incorporates a self-timed write feature which simplifies the system interface. The write function is internally timed on a write command which allows for a fast write pulse width and a fast write precharge time, thus eliminating the need for critical placement of transitions during the write cycle.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{\text{RAS}}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{\text{RAS}}$ -Only cycle will perform refresh.

Ripplemode™ Operation

Ripplemode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{\text{RAS}}$ low while successive $\overline{\text{CAS}}$ cycles are performed, retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{\text{CAS}}$ is high. Access begins from the valid column address rather than from $\overline{\text{CAS}}$, eliminating t_{ASC} and t_{r} from the critical timing path. $\overline{\text{CAS}}$ latches the addresses into the column address buffer and acts as an output enable.

During this operation read, write, read-modify-write, or read-write-read cycles are possible at random or sequential addresses within a row. Following the entry cycle into Ripplemode operation, access time is t_{CAA} or t_{CAP} dependent. If the column address is valid prior to or coincident with the rising edge of $\overline{\text{CAS}}$, then the access time is determined by the rising edge of $\overline{\text{CAS}}$ specified by t_{CAP} as shown in Figure 1. If the column address is valid after the rising edge of $\overline{\text{CAS}}$, then the access time is determined by the valid column address specified by t_{CAA} . For both cases, the falling edge of $\overline{\text{CAS}}$ latches the address and enables the output.

Ripplemode operation provides a sustained data rate over 15 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{512}{t_{\text{RC}} + 511 t_{\text{PC}}}$$

Data Out Operation

The 51C256H Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{\text{CAS}}$. During $\overline{\text{CAS}}$ high state ($\overline{\text{CAS}}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).

Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).

The V_{DD} current (I_{DD}) requirement of the 51C256H during power on is dependent upon the input levels of \overline{RAS} and \overline{CAS} . If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended

that \overline{RAS} and \overline{CAS} track with V_{DD} or be held at a valid V_{IH} during power on.

References

For further details see Application Note (A.P.) #171 *Low Power with CHMOS DRAMS*, and A.P. #172 *CHMOS DRAMS in Graphics Applications*.

Table 1. Intel 51C256H Data Output Operation for Various Types of Cycles

Cycle	Data Out of State
Read Cycle	Data from Addressed Memory Cell
\overline{CAS} Controlled Write Cycle (Early Write)	High Impedance
\overline{WE} Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Read-Write-Read Cycle (\overline{CAS} Controlled)	Data from Addressed Memory Cell
Read-Write-Read Cycle (\overline{WE} Controlled)	Data from Addressed Memory Cell and Active, Not Valid
\overline{RAS} -Only Refresh Cycle	High Impedance
\overline{CAS} -Only Cycle	High Impedance

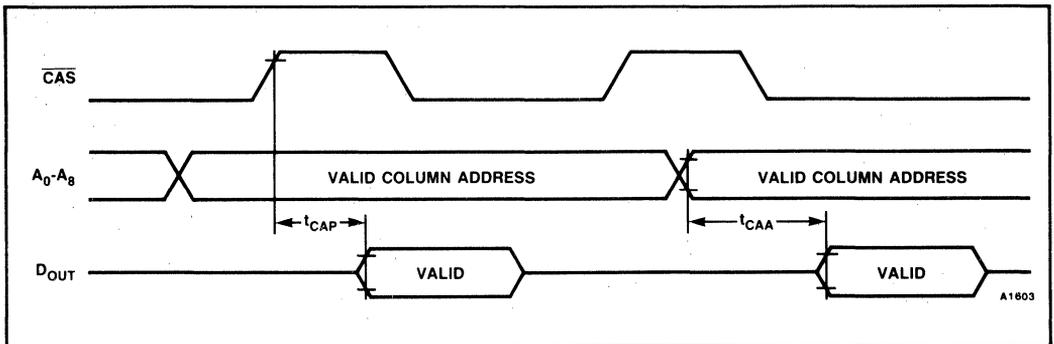


Figure 1. Ripplemode™ Access Time Determination

51C256L LOW POWER 256K X 1 CHMOS DYNAMIC RAM

	51C256L-15	51C256L-20
Maximum Access Time (ns)	150	200
Maximum CHMOS Standby Current (mA)	0.1	0.1

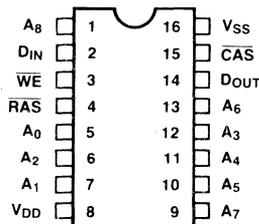
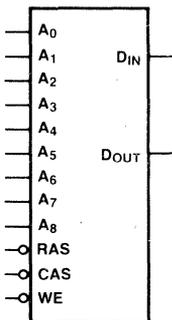
- Low Power Data Retention**
 - Standby current, CHMOS — 100 μ A (max.)
 - Refresh period, $\overline{\text{RAS}}$ -Only — 32 ms (max)
 - Data Retention Current — 230 μ A (max.)
- TTL and HCT Compatible**
- Low Input/Output Capacitance**
- High Reliability Plastic — 16 Pin DIP**

Intel® 51C256L is a low power 262,144 X 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C256L offers features not provided by an NMOS dynamic RAM: CHMOS standby current and extended $\overline{\text{RAS}}$ -Only refresh for low data retention power. All inputs and outputs are TTL and HCT compatible and the input and output capacitances are significantly lowered to allow increased system performance.

The 51C256L offers a maximum standby current of 100 μ A when $\overline{\text{RAS}} > V_{\text{DD}} - 0.5\text{V}$. During standby (i.e. refresh only cycles), the refresh period can be extended to 32 ms to reduce the total current required for data retention to less than 230 μ A (max). The 51C256L combines this low power with high density for portable and battery backup applications.

LOGIC SYMBOL PIN CONFIGURATION

PIN NAMES



$\overline{\text{RAS}}$	ROW ADDRESS STROBE
$\overline{\text{CAS}}$	COLUMN ADDRESS STROBE
$\overline{\text{WE}}$	WRITE ENABLE
$\text{A}_0\text{-A}_8$	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+ 5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under

- Bias..... -10°C to +80°C
- Storage Temperature... Plastic -55°C to +125°C
- Voltage on Any Pin except V_{DD} and D_{OUT}
 Relative to V_{SS}..... -2.0V to 7.5V
- Voltage on V_{DD} Relative to V_{SS}.... -1.0V to 7.5V
- Voltage on D_{OUT}
 Relative to V_{SS}..... -2.0V to V_{DD} + 1V
- Data Out Current..... 50 mA
- Power Dissipation..... 1.0W

†COMMENT:

Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C256L			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating		48	65	mA	t _{RC} = t _{RC} (min), for -15 specification	3,4
			35	50	mA	t _{RC} = t _{RC} (min), for -20 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby		1	2	mA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, RAS-only Refresh		45	65	mA	t _{RC} = t _{RC} (min), for -15 specification	4
			35	50	mA	t _{RC} = t _{RC} (min), for -20 specification	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled		3	4	mA	$\overline{\text{RAS}}$ at V _{IH} , $\overline{\text{CAS}}$ at V _{IL} , all other inputs and output ≥ V _{SS}	3
I _{DD6}	V _{DD} Supply Current, CHMOS Standby		0.01	0.1	mA	$\overline{\text{RAS}}$ ≥ V _{DD} - 0.5V and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{LI}	Input Load Current (any pin)			1	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current for High Impedance State			10	μA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	6
				0.1	V	I _{OL} = 100 μA ^{††}	
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -5 mA	6
				V _{DD} - .1	V	I _{OH} = -100 μA ^{††}	

NOTES: †† Available 1Q 1985

1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and V_{DD} = +5V.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{\text{CAS}}$ is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†
 $T_A = 25^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

Symbol	Parameter	Typ.	Max.	Unit
C _{IN1}	Address, D _{IN}	3	5	pF
C _{IN2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	4	5	pF
C _{OUT}	D _{OUT}	4	6	pF

A.C. CHARACTERISTICS^{1,2,3}
 $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t _{RL1RH1}	t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	150	75000	200	75000	ns	
2	t _{RL2RL2}	t _{RC}	Random Read or Write Cycle Time	245		315		ns	
3	t _{RH2RL2}	t _{RP}	$\overline{\text{RAS}}$ Precharge Time	85		105		ns	
4	t _{RL1CH1}	t _{CSH}	$\overline{\text{CAS}}$ Hold Time	150		200		ns	
5	t _{CL1CH1}	t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	30	75000	35	75000	ns	
6	t _{WH2RL2}	t _{WRP}	Write to $\overline{\text{RAS}}$ Precharge Time	10		10		ns	
7	t _{RL1WL2}	t _{RWH}	$\overline{\text{RAS}}$ to Write Hold Time	20		25		ns	
8	t _{AVRL}	t _{ASR}	Row Address Set-up Time	0		0		ns	
9	t _{RL1AX}	t _{RAH}	Row Address Hold Time	20		25		ns	
10	t _{CH2CL2}	t _{CP}	$\overline{\text{CAS}}$ Precharge Time	10		10		ns	
11	t _{CH2RL2}	t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	-20		-20		ns	
12	t _{RL1CL1}	t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	35	120	40	165	ns	4
13	t _{AVCL2}	t _{ASC}	Column Address Set-up Time	5		5		ns	
14	t _{CL1AX}	t _{CAH}	Column Address Hold Time	20		25		ns	
15	t _{RL1AX}	t _{AR}	Column Address Hold Time From $\overline{\text{RAS}}$	70		80		ns	
	t _{RVRV}	t _{REF1}	Time Between Refresh		4		4	ms	5
	t _{RVRV}	t _{REF2}	Time Between Refresh ($\overline{\text{RAS}}$ -Only)		32		32	ms	5
	t _T	t _T	Transition Time (Rise and Fall)	3	25	3	25	ns	6
16	t _{CL1QX}	t _{ON}	Output Buffer Turn On Delay	0	30	0	35	ns	
17	t _{CH2OZ}	t _{OFF}	Output Buffer Turn Off Delay	0	25	0	30	ns	

NOTES:

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).
- A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
- t_{RCD} (max) is specified for reference only.
- The 51C256L extends the refresh period to 32 ms during $\overline{\text{RAS}}$ -Only refresh operation.
- t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. CHARACTERISTICS (Con't.)

Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
18	t _{RL1QV}	t _{RAC}	Access Time From \overline{RAS}		150		200	ns	7
19	t _{CL1QV}	t _{CAC}	Access Time From \overline{CAS}		30		35	ns	8, 9
20	t _{AVQV}	t _{CAA}	Access Time From Column Address		70		90	ns	9
21	t _{CL1RH1(R)}	t _{RSH(R)}	\overline{RAS} Hold Time (Read Cycle)	10		10		ns	
22	t _{WH2CL2}	t _{RCS}	Read Command Set-up Time	0		0		ns	
23	t _{AVRH1}	t _{CAR}	Column Address \overline{RAS} Set-up Time	70		90		ns	
24	t _{CH2WX}	t _{RCH}	Read Com. Hold Time Referenced to \overline{CAS}	0		0		ns	10
25	t _{RH2WX}	t _{RRH}	Read Com. Hold Time Referenced to \overline{RAS}	10		10		ns	10

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
26	t _{CL1RH1(W)}	t _{RSH(W)}	\overline{RAS} Hold Time (Write Cycle)	30		35		ns	
27	t _{WL1RH1}	t _{RWL}	Write Command to \overline{RAS} Lead Time	30		35		ns	
28	t _{WL1CH1}	t _{CWL}	Write Command to \overline{CAS} Lead Time	30		35		ns	
29	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	25		30		ns	
30	t _{WL1CL2}	t _{WCS}	Write Command Set-up Time	0		0		ns	11
31	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	30		35		ns	
32	t _{DVCL2}	t _{DS}	Data-In Set-up Time	0		0		ns	
33	t _{CL1DX}	t _{DH}	Data-In Hold Time	25		30		ns	

NOTES:

7. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If $t_{RCD} \geq t_{RCD}(\text{max})$, then t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{RCD}(\text{max})$.
8. Assumes $t_{RCD} \geq t_{RCD}(\text{max})$.
9. If $t_{ASC} < (t_{CAA}(\text{max}) - t_{CAC}(\text{max}) - t_r)$, then access time is defined by t_{CAA} rather than by t_{CAC} .
10. Either t_{RCH} or t_{RRH} must be satisfied.
11. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is a \overline{CAS} controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)

Read-Modify-Write- Cycle¹²

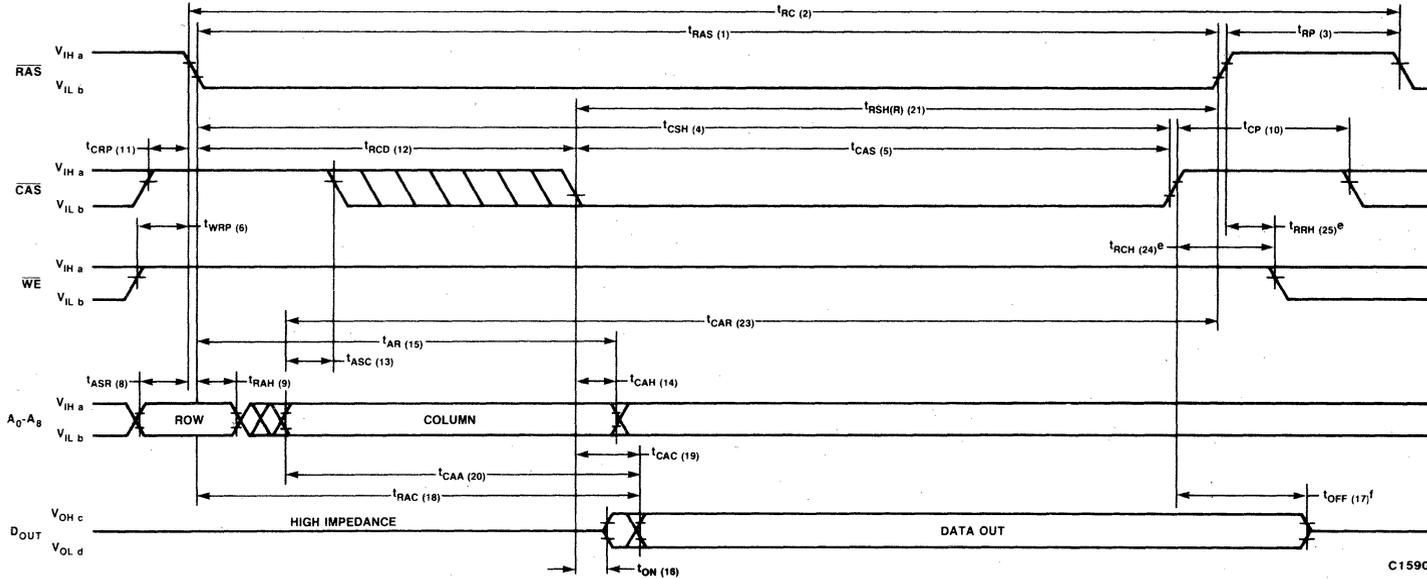
#	JEDEC Symbol	Symbol	Parameter	51C256L-15		51C256L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
34	t _{RL2RL2(RMW)}	t _{RWC}	Read-Modify-Write (RMW) Cycle Time	280		355		ns	
35	t _{RL1RH1(RMW)}	t _{RRW}	RMW Cycle \overline{RAS} Pulse Width	185		240		ns	
36	t _{CL1CH1(RMW)}	t _{CRW}	RMW Cycle \overline{CAS} Pulse Width	65		75		ns	
37	t _{RL1WL2}	t _{RWD}	\overline{RAS} to \overline{WE} Delay	150		200		ns	13
38	t _{CL1WL2}	t _{CWD}	\overline{CAS} to \overline{WE} Delay	30		35		ns	13
39	t _{AVWL2}	t _{AWD}	Column Address to \overline{WE} Delay	70		90		ns	13

NOTES:

12. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS} (min), the cycle is a \overline{CAS} controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min) and t_{AWD} ≥ t_{AWD} (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.

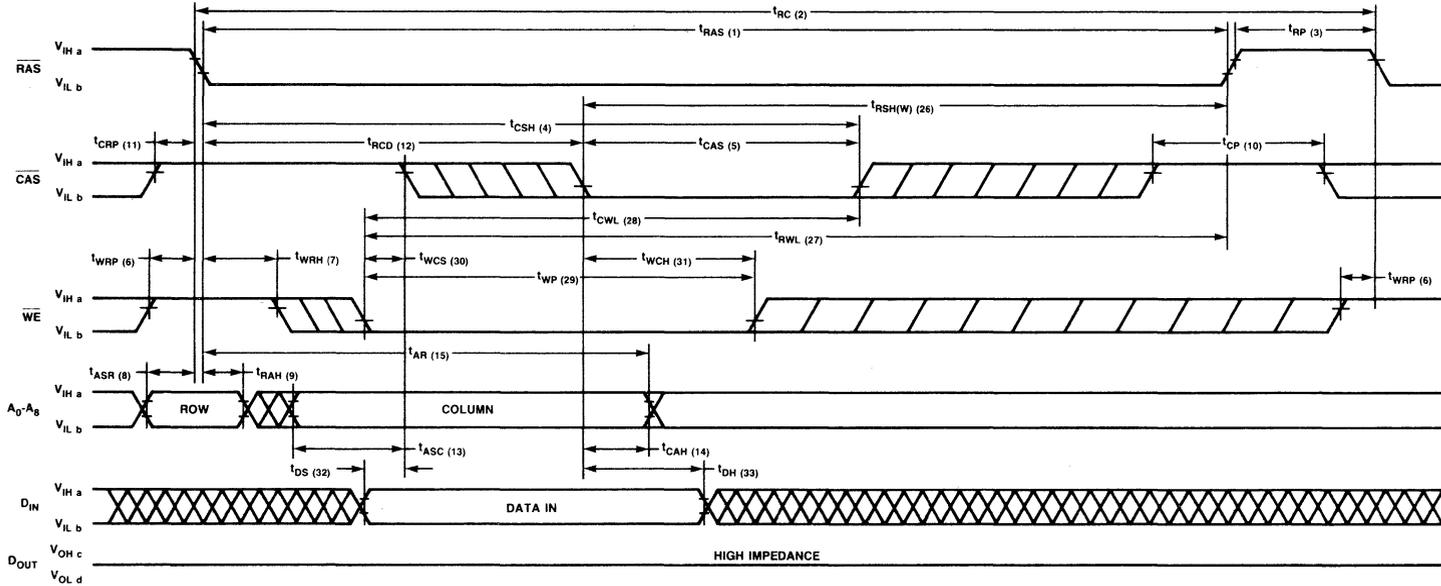
WAVEFORMS

Read Cycle



- NOTES:**
- a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
 - e. Either t_{RCH} or t_{RRH} must be satisfied.
 - f. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)
Write Cycle ($\overline{\text{CAS}}$ Controlled)^e



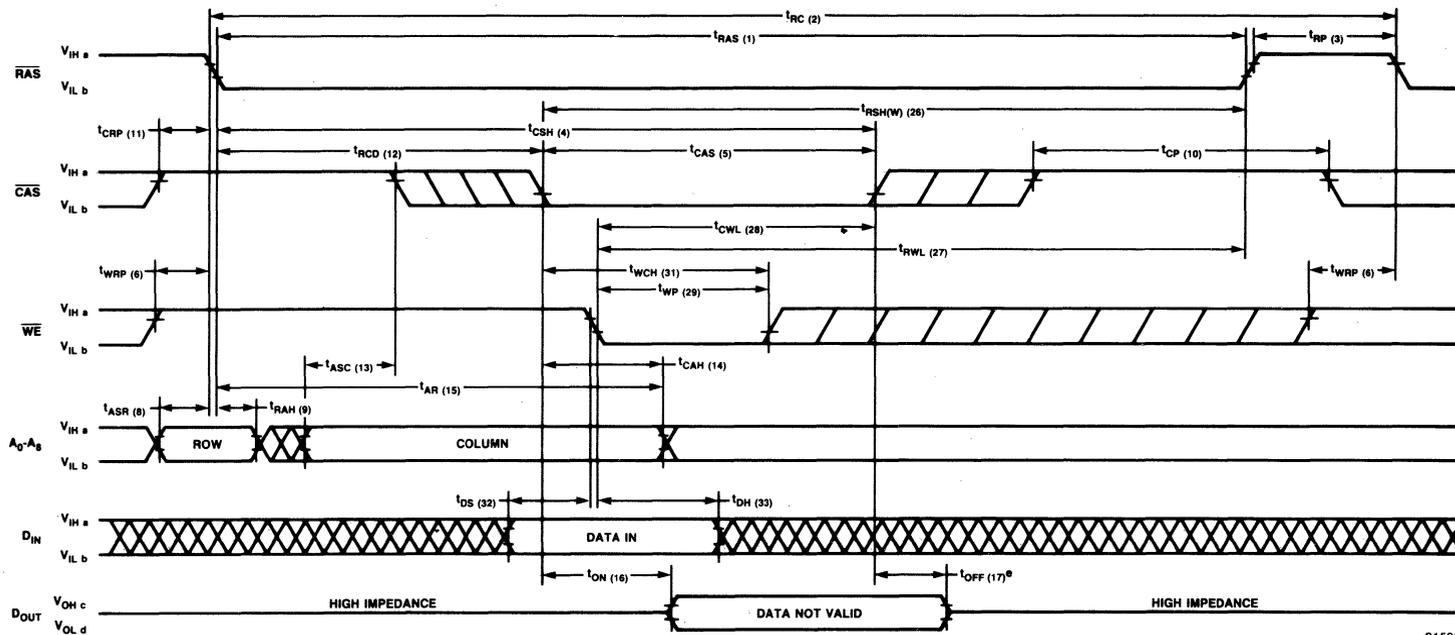
2-79

- NOTES:**
- a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - e. $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column address and data-in.

C1591

WAVEFORMS (Cont.)

Write Cycle (WE Controlled)^f

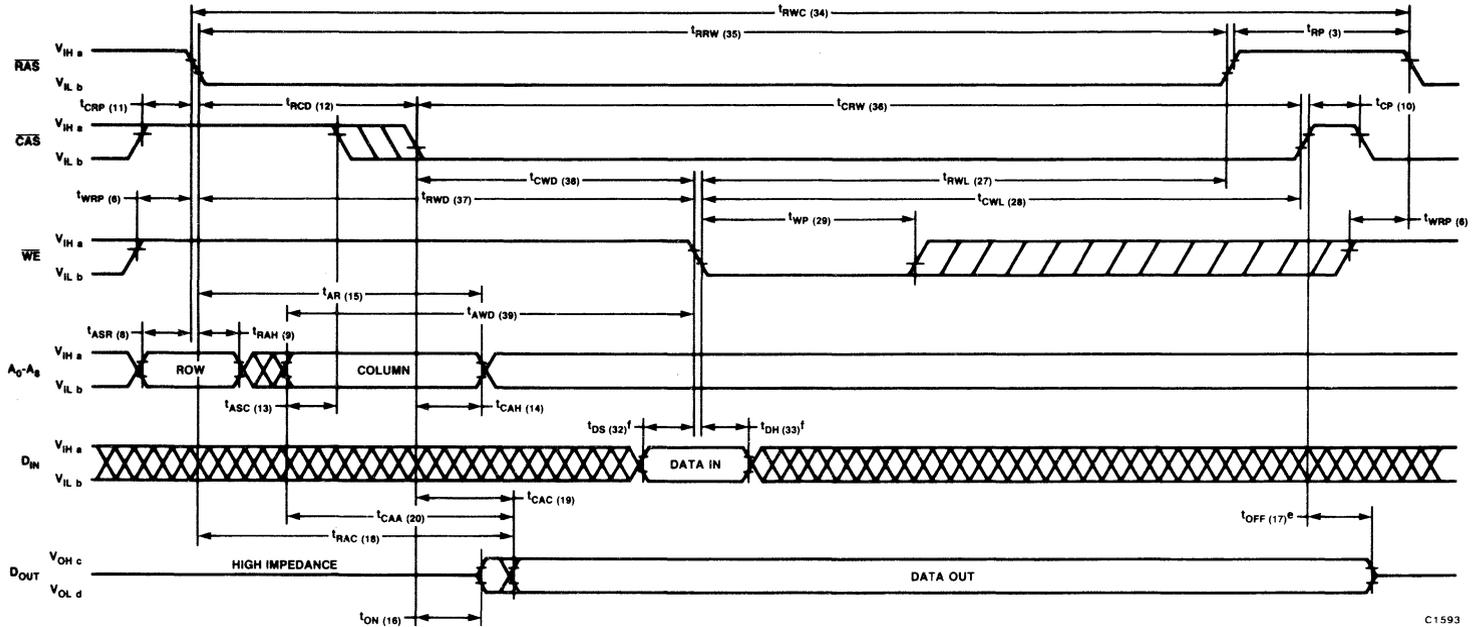


- NOTES:**
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
 - \overline{CAS} is low prior to the \overline{WE} low transition. \overline{CAS} latches the column address while \overline{WE} latches the data-in.

WAVEFORMS (Cont.)

Read/Modify/Write Cycle

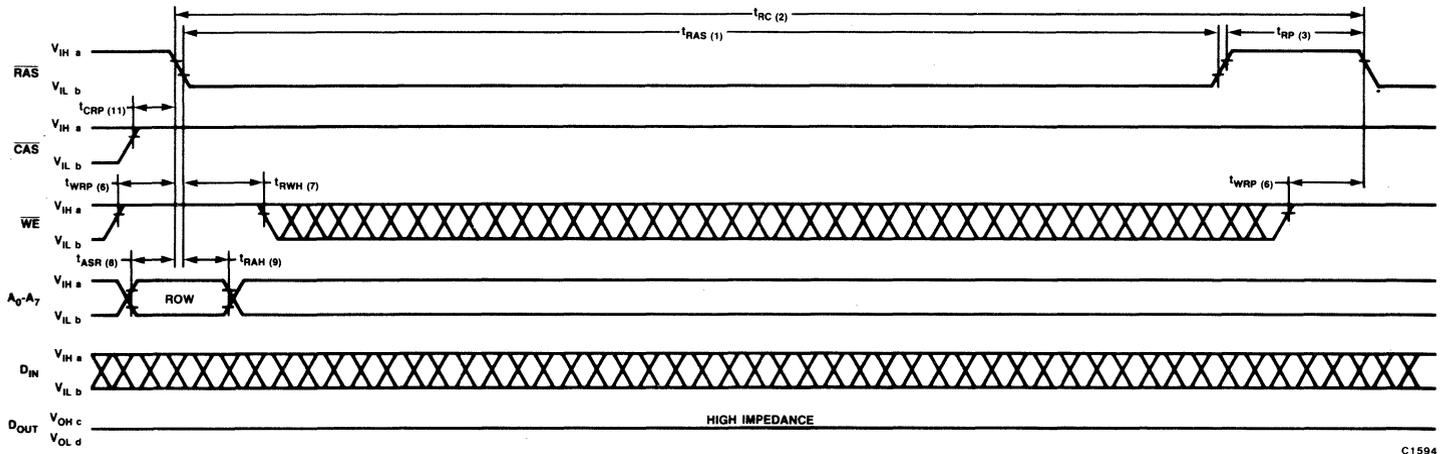
2-81



C1593

- NOTES:**
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
 - t_{DS} and t_{DH} are referenced to \overline{CAS} or \overline{WE} , whichever occurs last.

WAVEFORMS (Cont.)
RAS-Only Refresh Cycle



NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

FUNCTIONAL DESCRIPTIONS

The 51C256L is a CHMOS dynamic RAM optimized for low power applications. The functionality is similar to a traditional dynamic RAM. The 51C256L reads and writes data by multiplexing an 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched in by the Row Address Strobe ($\overline{\text{RAS}}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{\text{CAS}}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}/\overline{\text{CAS}}$ operation. The column address must be held for a minimum time specified by t_{AR} . Data out becomes valid only when t_{RAC} , t_{CAA} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ low during a $\overline{\text{RAS}}$ operation. The column address is latched in by $\overline{\text{CAS}}$. The write cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending upon the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. In a $\overline{\text{CAS}}$ controlled write cycle (the leading edge of $\overline{\text{WE}}$ occurs prior to or coincident with the $\overline{\text{CAS}}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ will maintain the output in the high impedance state; terminating with $\overline{\text{WE}}$ allows the output to go active.

The 51C256L incorporates a self-timed write feature which simplifies the system interface. The write function is internally timed on a write command which allows for a fast write pulse width and a fast write precharge time, thus eliminating the need for critical placement of transitions during the write cycle.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{\text{RAS}}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{\text{RAS}}$ -Only cycle will perform refresh.

Extended Refresh Cycle

The 51C256L extends the refresh cycle period to 32 milliseconds for $\overline{\text{RAS}}$ -Only refresh cycles. This feature reduces the total current consumption to a maximum of 230 micro Amperes, and typically 90 micro Amperes, for data retention ($\overline{\text{RAS}}$ -Only refresh operation for the 51C256L-20). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{\text{RC}})(I_{\text{Active}}) + (t_{\text{RC}} - t_{\text{RC}})(I_{\text{Standby}})}{t_{\text{RI}}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time of $t_{\text{REF}}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Data Out Operation

The 51C256L Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{\text{CAS}}$. During $\overline{\text{CAS}}$ high state ($\overline{\text{CAS}}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).

The V_{DD} current (I_{DD}) requirement of the 51C256L during power on is dependent upon the input levels of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. If $\overline{\text{RAS}} = V_{\text{SS}}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{DD} or be held at a valid V_{IH} during power on.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

Table 1. Intel 51C256L Data Output Operation for Various Types of Cycles

Cycle	Data Out State
Read Cycle	Data from Addressed Memory Cell
$\overline{\text{CAS}}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{\text{WE}}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{\text{RAS}}$ -Only Refresh Cycle	High Impedance
$\overline{\text{CAS}}$ -Only Cycle	High Impedance

51C256HL HIGH PERFORMANCE LOW POWER RIPPLEMODE™ 256K X 1 CHMOS DYNAMIC RAM

	51C256HL-15	51C256HL-20
Maximum Access Time (ns)	150	200
Maximum Column Address Access Time (ns)	70	90
Maximum CHMOS Standby Current (mA)	0.1	0.1

- **Ripplemode Operation**
 - Continuous data rate over 12 MHz
 - Random access within row
 - Flow through column latch for pipelining
- **Low Input/Output Capacitance**
- **TTL and HCT Compatible**
- **Low Power Data Retention**
 - Standby current, CHMOS — 100 μ A (max.)
 - Refresh period, $\overline{\text{RAS}}$ -Only — 32 ms (max.)
 - Data Retention Current — 230 μ A (max.)
- **Low Operating Current — 65 mA (max.)**
- **High Reliability Plastic — 16 Pin DIP**

The Intel® 51C256HL is a high speed 262,144 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C256HL offers features not provided by an NMOS dynamic RAM: Ripplemode for high data bandwidth, fast usable speed, and CHMOS standby current and extended $\overline{\text{RAS}}$ -Only refresh for low data retention power. All inputs and outputs are TTL and HCT compatible and the input and output capacitances are significantly lowered to allow increased system performance.

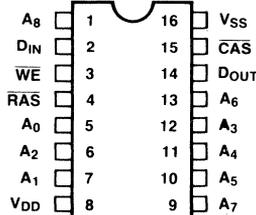
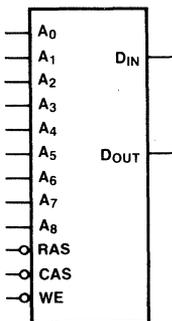
Ripplemode operation allows random or sequential access of up to 512 bits within a row, with cycle times as fast as 80 ns. Because of static column circuitry, the $\overline{\text{CAS}}$ clock is no longer in the critical timing path. The flow through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the 51C256HL ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance microprocessor systems.

The 51C256HL offers a maximum standby current of 100 μ A when $\overline{\text{RAS}} \geq V_{\text{DD}} - 0.5\text{V}$. During standby (i.e. refresh only cycles) the refresh period can be extended to 32 ms to reduce the total current required for data retention to less than 230 μ A (max). The 51C256HL combines low power with high density for portable and battery back-up applications.

LOGIC SYMBOL

PIN CONFIGURATION

PIN NAMES



$\overline{\text{RAS}}$	ROW ADDRESS STROBE
$\overline{\text{CAS}}$	COLUMN ADDRESS STROBE
$\overline{\text{WE}}$	WRITE ENABLE
A ₀ -A ₈	ADDRESS INPUTS
D _{IN}	DATA INPUT
D _{OUT}	DATA OUTPUT
V _{DD}	POWER (+ 5V)
V _{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under

- Bias -10°C to +80°C
- Storage Temperature... Plastic -55°C to +125°C
- Voltage on Any Pin except V_{DD} and D_{OUT}
Relative to V_{SS}.....-2.0V to 7.5V
- Voltage on V_{DD} Relative to V_{SS}.....-1.0V to 7.5V
- Voltage on D_{OUT}
Relative to V_{SS}.....-2.0V to V_{DD} + 1V
- Data Out Current..... 50 mA
- Power Dissipation..... 1.0W

†COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹ T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C256HL			Unit	Test Conditions	Note
		Min.	Typ ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating		48	65	mA	t _{RC} = t _{RC} (min), for - 15 specification	3,4
			35	50	mA	t _{RC} = t _{RC} (min), for - 20 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby		1	2	mA	\overline{RAS} and \overline{CAS} at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, \overline{RAS} -only Refresh		45	65	mA	t _{RC} = t _{RC} (min), for - 15 specification	4
			35	50	mA	t _{RC} = t _{RC} (min), for - 20 specification	
I _{DD4}	V _{DD} Supply Current, Ripplemode		22	65	mA	t _{PC} = t _{PC} (min), for - 15 specification	3,4
			18	50	mA	t _{PC} = t _{PC} (min), for - 20 specification	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled		3	4	mA	\overline{RAS} at V _{IH} , \overline{CAS} at V _{IL} , all other inputs and output ≥ V _{SS}	3
I _{DD6}	V _{DD} Supply Current, CMOS Standby		0.01	1	mA	\overline{RAS} ≥ V _{DD} - 0.5V and \overline{CAS} at V _{IH} , all other inputs and output ≥ V _{SS}	
I _{LI}	Input Load Current (any pin)			1	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current for High Impedance State			10	μA	\overline{RAS} and \overline{CAS} at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	- 1.0		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	6
				0.1	V	I _{OL} = 100μA ^{††}	
V _{OH}	Output High Voltage	2.4			V	I _{OH} = - 5 mA	6
				V _{DD} - .1	V	I _{OH} = - 100 μA ^{††}	

NOTES: †† Available 1Q 1985

1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and V_{DD} = + 5V.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while \overline{CAS} is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Ripplemode.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	5	pF
C_{IN2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS^{1,2,3}

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C256HL-15		51C256HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	150	75000	200	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	245		315		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	85		105		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{\text{CAS}}$ Hold Time	150		200		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	30	75000	35	75000	ns	
6	t_{WH2RL2}	t_{WRP}	Write to $\overline{\text{RAS}}$ Precharge Time	10		10		ns	
7	t_{RL1WL2}	t_{RWH}	$\overline{\text{RAS}}$ to Write Hold Time	20		25		ns	
8	t_{AVL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	20		25		ns	
10	t_{CH2CL2}	t_{CP}	$\overline{\text{CAS}}$ Precharge Time	10		10		ns	
11	t_{CH2RL2}	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	-20		-20		ns	
12	t_{RL1CL1}	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	35	120	40	165	ns	4
13	t_{AVL2}	t_{ASC}	Column Address Set-up Time	5		5		ns	
14	t_{CL1AX}	t_{CAH}	Column Address Hold Time	20		25		ns	
15	t_{RL1AX}	t_{AR}	Column Address Hold Time From $\overline{\text{RAS}}$	70		80		ns	
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4	ms	5
	t_{RVRV}	t_{REF2}	Time Between Refresh ($\overline{\text{RAS}}$ -Only)		32		32	ms	5
	t_T	t_T	Transition Time (Rise and Fall)	3	25	3	25	ns	6
16	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0	30	0	35	ns	
17	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	25	0	30	ns	

NOTES:

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).
- A.C. Characteristics assume $t_T = 5\text{ ns}$. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, $V_{IL}(\text{min}) \geq V_{SS}$ and $V_{IH}(\text{max}) \leq V_{DD}$.
- $t_{RCD}(\text{max})$ is specified for reference only.
- The 51C256HL extends the refresh period to 32 ms during $\overline{\text{RAS}}$ -Only refresh operation.
- t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

A.C. CHARACTERISTICS (Con't.)
Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256HL-15		51C256HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
18	t _{RL1QV}	t _{RAC}	Access Time From $\overline{\text{RAS}}$		150		200	ns	7
19	t _{CL1QV}	t _{CAC}	Access Time From $\overline{\text{CAS}}$		30		35	ns	8,9
20	t _{AVQV}	t _{CAA}	Access Time From Column Address		70		90	ns	9
21	t _{CL1RH1}	t _{RSH(R)}	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	10		10		ns	
22	t _{WH2CL2}	t _{RCS}	Read Command Set-up Time	0		0		ns	
23	t _{AVRH1}	t _{CAR}	Column Address to $\overline{\text{RAS}}$ Set-up Time	70		90		ns	
24	t _{CH2WX}	t _{RCH}	Read Com. Hold Time Referenced to $\overline{\text{CAS}}$	0		0		ns	10
25	t _{RH2WX}	t _{RRH}	Read Com. Hold Time Referenced to $\overline{\text{RAS}}$	10		10		ns	10

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C256HL-15		51C256HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
26	t _{CL1RH1(W)}	t _{RSH(W)}	$\overline{\text{RAS}}$ Hold Time (Write Cycle)	30		35		ns	
27	t _{WL1RH1}	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	30		35		ns	
28	t _{WL1CH1}	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	30		35		ns	
29	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	25		30		ns	
30	t _{WL1CL2}	t _{WCS}	Write Command Set-up Time	0		0		ns	11
31	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	30		35		ns	
32	t _{DVCL2}	t _{DS}	Data-In Set-up Time	0		0		ns	
33	t _{CL1DX}	t _{DH}	Data-In Hold Time	25		30		ns	

NOTES:

7. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$. If $t_{\text{RCD}} > t_{\text{RCD}}(\text{max})$, then t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{\text{RCD}}(\text{max})$.
8. Assumes $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
9. If $t_{\text{ASC}} < (t_{\text{CAA}}(\text{max}) - t_{\text{CAC}}(\text{max}) - t_{\text{T}})$, then access time is defined by t_{CAA} rather than by t_{CAC} .
10. Either t_{RCH} or t_{RRH} must be satisfied.
11. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are specified as reference points only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is a $\overline{\text{CAS}}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)
Read-Modify-Write- Cycle¹²

#	JEDEC Symbol	Symbol	Parameter	51C256HL-15		51C256HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
34	$t_{P, 2RL2(RMW)}$	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	280		355		ns	
35	$t_{RL1RH1(RMW)}$	t_{RRW}	RMW Cycle \overline{RAS} Pulse Width	185		240		ns	
36	$t_{CL1CH1(RMW)}$	t_{CRW}	RMW Cycle \overline{CAS} Pulse Width	65		75		ns	
37	t_{RL1WL2}	t_{RWD}	\overline{RAS} to \overline{WE} Delay	150		200		ns	13
38	t_{CL1WL2}	t_{CWD}	\overline{CAS} to \overline{WE} Delay	30		35		ns	13
39	t_{AVWL2}	t_{AWD}	Column Address to \overline{WE} Delay	70		90		ns	13

Ripplemode Cycle¹⁴

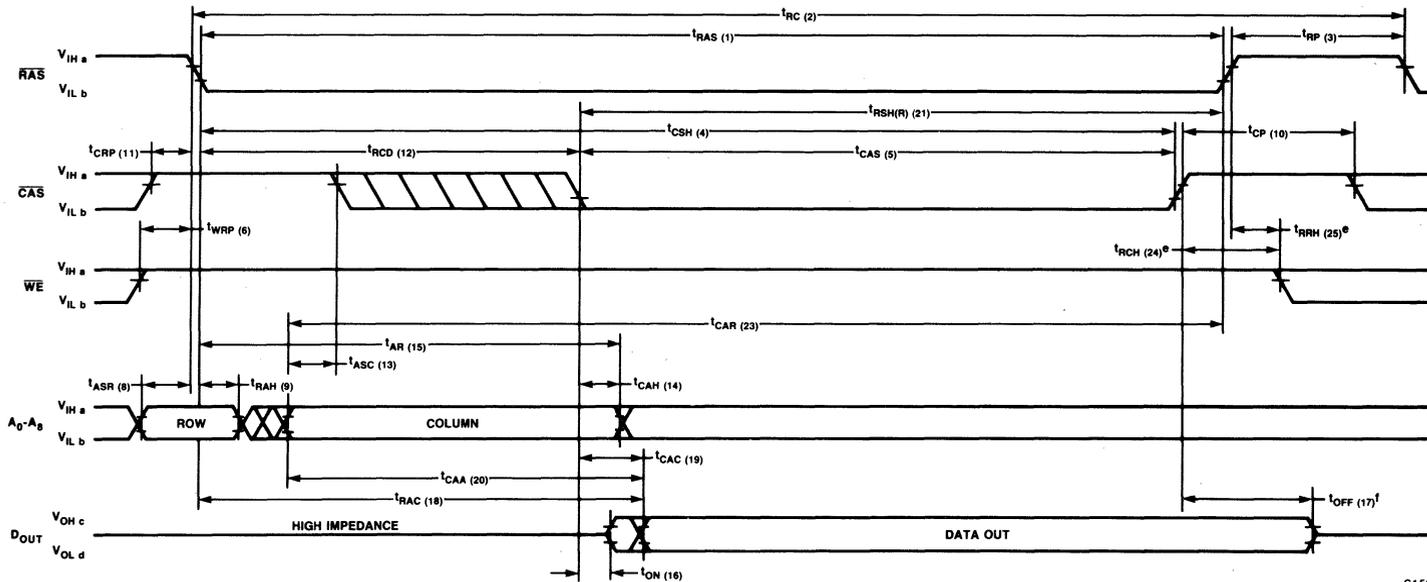
#	JEDEC Symbol	Symbol	Parameter	51C256HL-15		51C256HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
40	t_{CH2QV}	t_{CAP}	Access Time From Column Precharge		75		95	ns	15
41	$t_{CL2CL2 (R)}$	t_{PC}	Ripplemode Read or Write Cycle	80		100		ns	15
42	$t_{CL2CL2 (RRMW)}$	t_{PCM}	Ripplemode RMW Cycle Time	110		135		ns	

NOTES:

12. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
13. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is a \overline{CAS} controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.
14. All previously specified A.C. Characteristics are applicable.
15. Access time is determined by the longer of t_{CAA} or t_{CAC} or t_{CAP} .

WAVEFORMS

Read Cycle

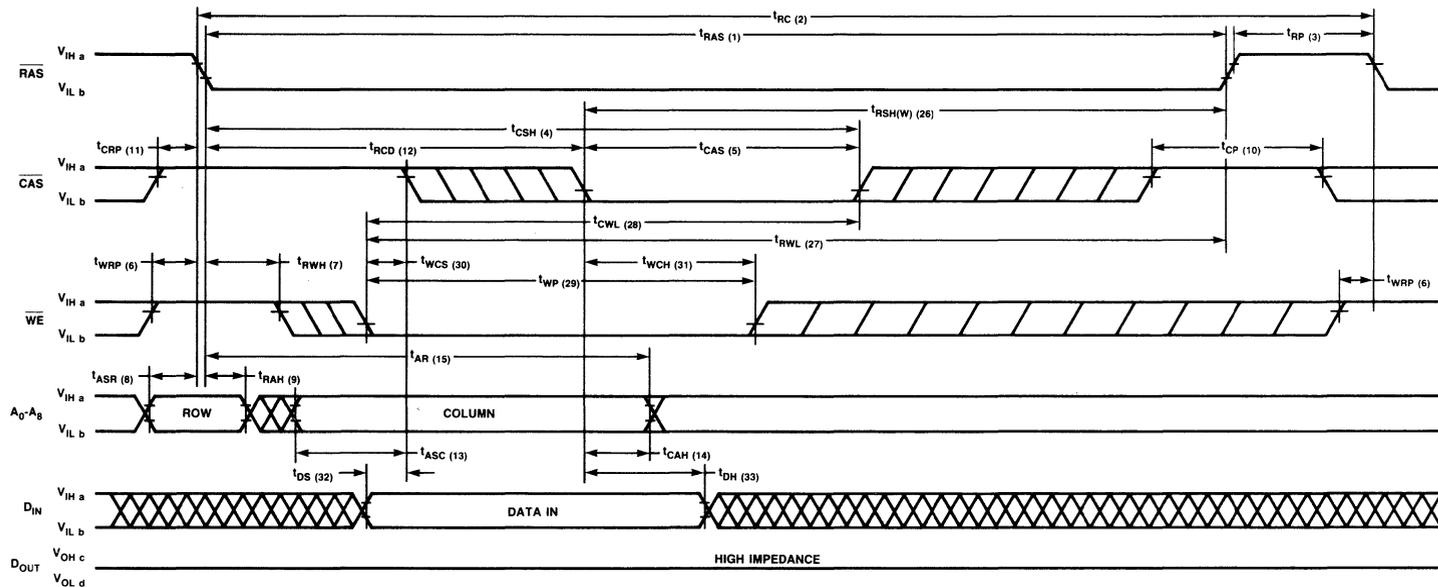


C1590

- NOTES:**
- a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - e. Either t_{RCH} or t_{RRH} must be satisfied.
 - f. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)

Write Cycle (CAS Controlled)^e



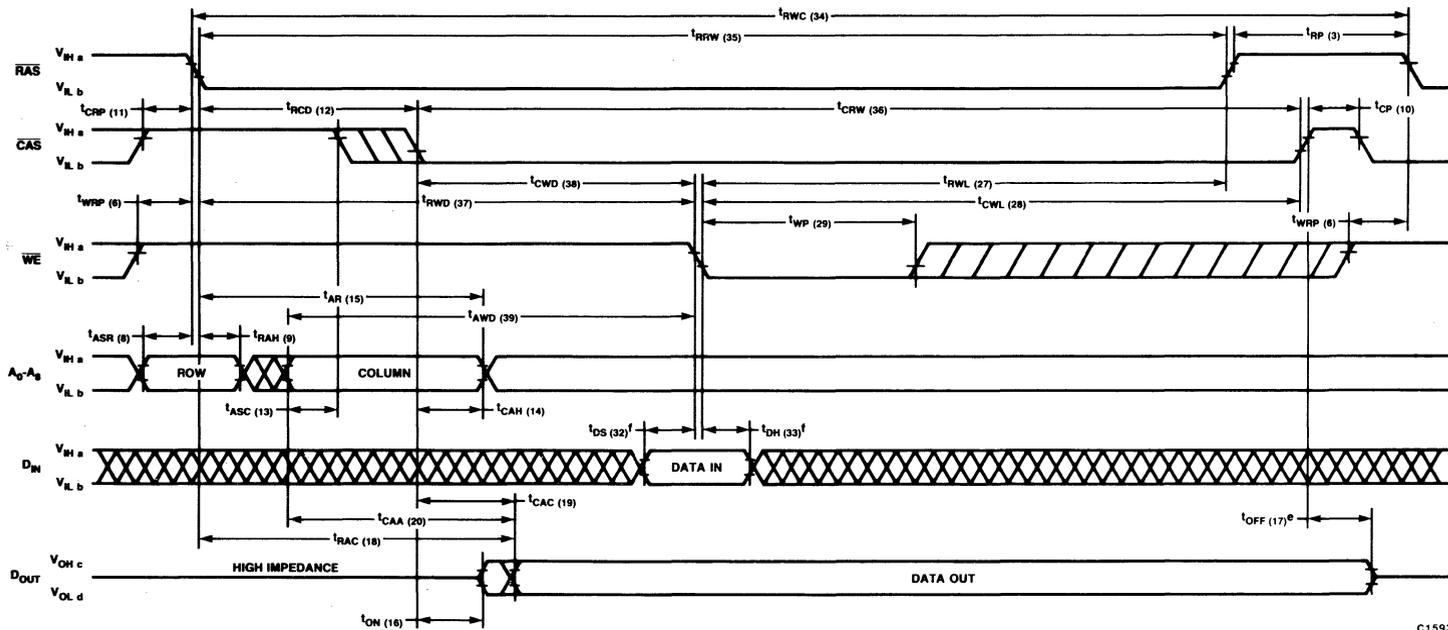
2-91

- NOTES:** a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. \overline{WE} is low prior to or simultaneously with \overline{CAS} low transition. \overline{CAS} latches column address and data-in.

C1591

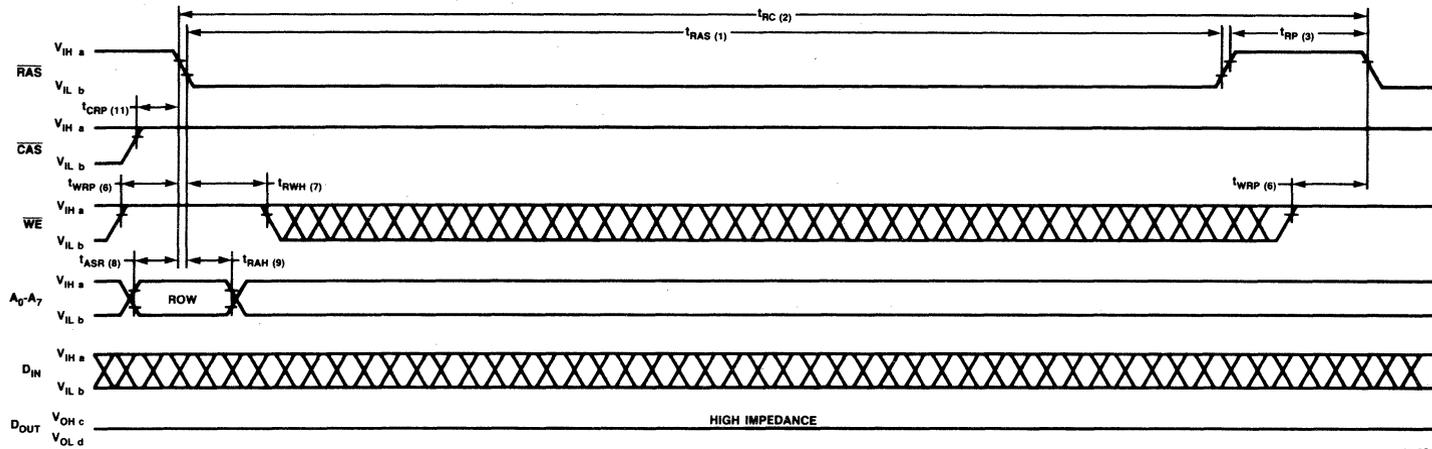
WAVEFORMS (Cont.)

Read/Modify/Write Cycle



- NOTES:**
- a,b. V_H (min) and V_L (max) are reference levels for measuring timing of input signals.
 - c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
 - e. t_{OFF} is measured to I_{OUT} ≤ |I_O|.
 - f. t_{DS} and t_{DH} are referenced to $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs last.

WAVEFORMS (Cont.)
RAS-Only Refresh Cycle

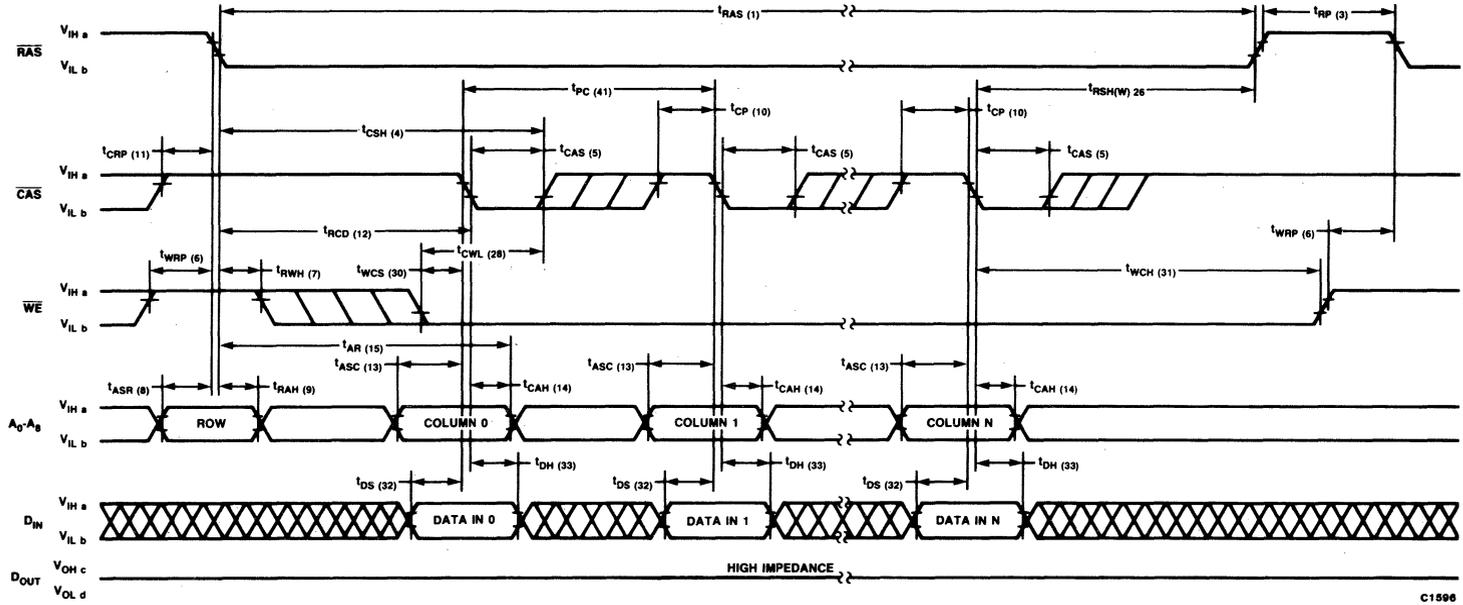


2-94

NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .

C1594

WAVEFORMS (Cont.)
Ripplemode Write Cycle ($\overline{\text{CAS}}$ Controlled)^e



2-96

- NOTES:** a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column addresses and data-in.

C1598

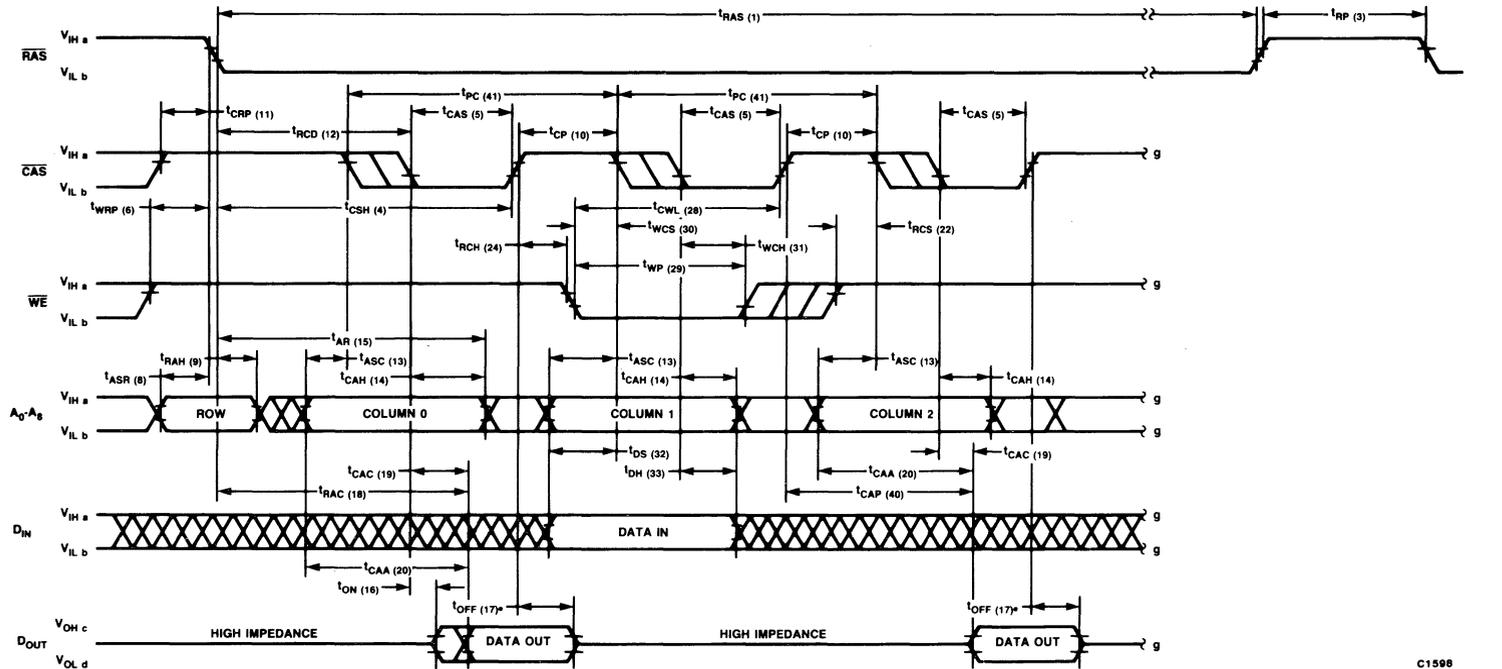


51C256HL

PRELIMINARY

WAVEFORMS (Cont.)

Ripplemode Read/Write/Read/. . . Cycle ($\overline{\text{CAS}}$ Controlled)

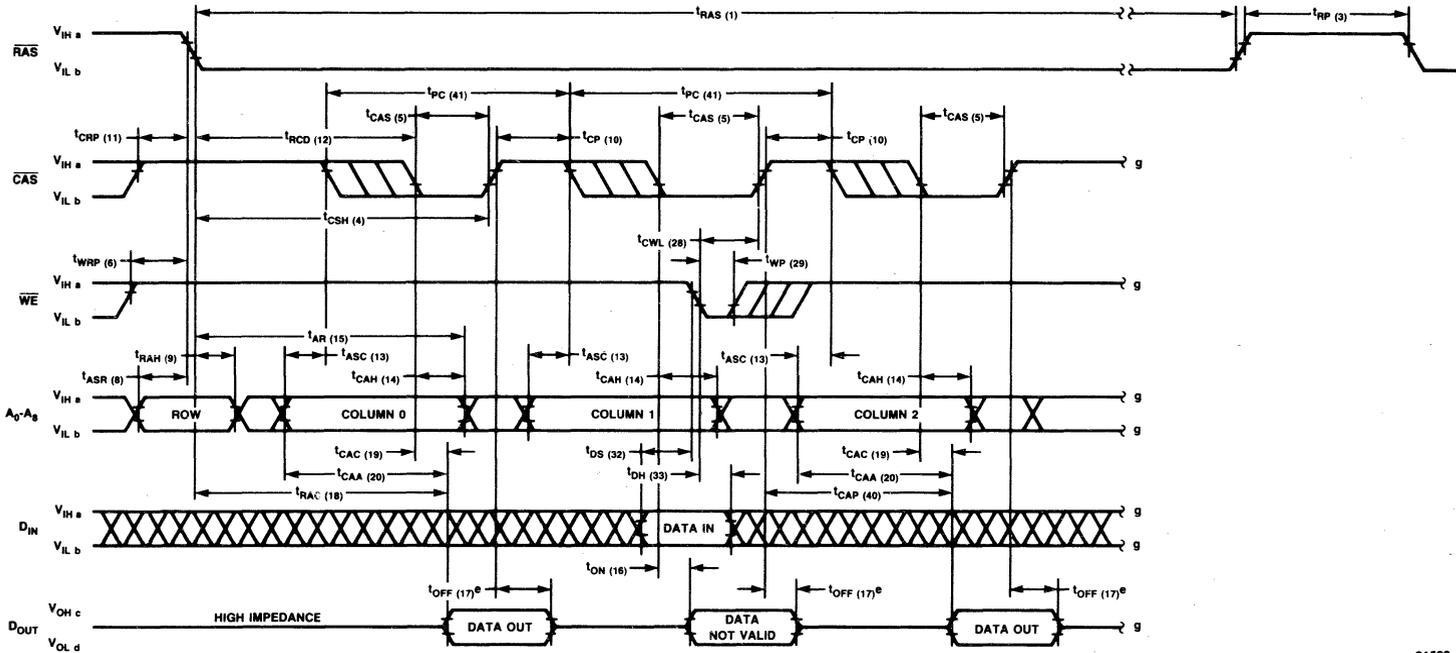


2-99

- NOTES: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. t_{OFF} is measured to $I_{OUT} \leq |I_{OL}|$.
 f. $\overline{\text{WE}}$ is low prior to or simultaneously with $\overline{\text{CAS}}$ low transition. $\overline{\text{CAS}}$ latches column addresses and data-in
 g. The cycle can be terminated either by a read or a write operation followed by a $\overline{\text{RAS}}$ high transition. See page 11 or 12 for timings.

C1598

WAVEFORMS (Cont.)
Ripplemode Read/Write/Read/. . . Cycle (\overline{WE} Controlled)^f



2-100

- NOTES:** a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
 f. \overline{CAS} is low prior to \overline{WE} low transition. \overline{CAS} latches the column addresses while \overline{WE} latches data-in.
 g. The cycle can be terminated either by a read or a write operation followed by a \overline{RAS} high transition. See page 11 or 13 for timings.

C1599

FUNCTIONAL DESCRIPTION

The 51C256HL is a CHMOS dynamic RAM optimized for both high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The 51C256HL reads and writes data by multiplexing an 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched in by the Row Address Strobe ($\overline{\text{RAS}}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe (CAS). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{\text{RAS}}$ and CAS can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}$ /CAS operation. The column address must be held for a minimum time specified by t_{AR} . Data out becomes valid only when t_{RAC} , t_{CAA} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ low during a $\overline{\text{RAS}}$ operation. The column address is latched in by CAS. The write cycle can be $\overline{\text{WE}}$ controlled or CAS controlled depending upon the later of $\overline{\text{WE}}$ or CAS low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or CAS, whichever occurs last. In a CAS controlled write cycle (the leading edge of $\overline{\text{WE}}$ occurs prior to or coincident with the CAS low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ will maintain the output in the high impedance state; terminating with $\overline{\text{WE}}$ allows the output to go active.

The 51C256HL incorporates a self-timed write feature which simplifies the system interface. The write function is internally timed on a write command which allows for a fast write pulse width and a fast write precharge time, thus eliminating the need for critical placement of transitions during the write cycle.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{\text{RAS}}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{\text{RAS}}$ -Only cycle will perform refresh.

Extended Refresh Cycle

The 51C256HL extends the refresh cycle period to 32 milliseconds for $\overline{\text{RAS}}$ -Only refresh cycles. This feature reduces the total current consumption to a maximum of 230 micro Amperes, and typically 90 micro Amperes, for data retention ($\overline{\text{RAS}}$ -Only refresh operation for the 51C256HL-20). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{\text{RC}} I_{\text{ACTIVE}}) + (t_{\text{RI}} - t_{\text{RC}}) (I_{\text{STANDBY}})}{t_{\text{RI}}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{\text{REF}}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Ripplemode™ Operation

Ripplemode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{\text{RAS}}$ low while successive CAS cycles are performed, retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while CAS is high. Access begins from the valid column address rather than from CAS, eliminating t_{ASC} and t_{T} from the critical timing path. CAS latches the addresses into the column address buffer and acts as an output enable.

During this operation read, write, read-modify-write, or read-write-read cycles are possible at random or sequential addresses within a row. Following the entry cycle into Ripplemode operation, access time is t_{CAA} or t_{CAP} dependent. If the column address is valid prior to or coincident with the rising edge of CAS, then the access time is determined by the rising edge of CAS specified by t_{CAP} as shown in Figure 1. If the column address is valid after the rising edge of $\overline{\text{CAS}}$, then the access time is determined by the valid column address specified by t_{CAA} . For both cases, the falling edge of CAS latches the address and enables the output.

Ripplemode operation provides a sustained data rate over 12 MHz for applications that require high data rate such as bit mapped graphics or high speed sig-

nal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 t_{PC}}$$

Data Out Operation

The 51C256HL Data Output (D_{OUT}), which has three-state capability, is controlled by \overline{CAS} . During \overline{CAS} high state (\overline{CAS} at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μ s is required after the application of the V_{DD} supply, followed by a minimum of

eight initialization cycles (any combination of cycles containing a \overline{RAS} clock such as \overline{RAS} -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).

The V_{DD} current (I_{DD}) requirement of the 51C256HL during power on is dependent upon the input levels of \overline{RAS} and \overline{CAS} . If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that \overline{RAS} and \overline{CAS} track with V_{DD} or be held at a valid V_{IH} during power on.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

Table 1. Intel 51C256HL Data Output Operation for Various Types of Cycles

Cycle	Data Out of State
Read Cycle	Data from Addressed Memory Cell
\overline{CAS} Controlled Write Cycle (Early Write)	High Impedance
\overline{WE} Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Read-Write-Read Cycle (\overline{CAS} Controlled)	Data from Addressed Memory Cell
Read-Write-Read Cycle (\overline{WE} Controlled)	Data from Addressed Memory Cell and Active, Not Valid
\overline{RAS} -Only Refresh Cycle	High Impedance
\overline{CAS} -Only Cycle	High Impedance

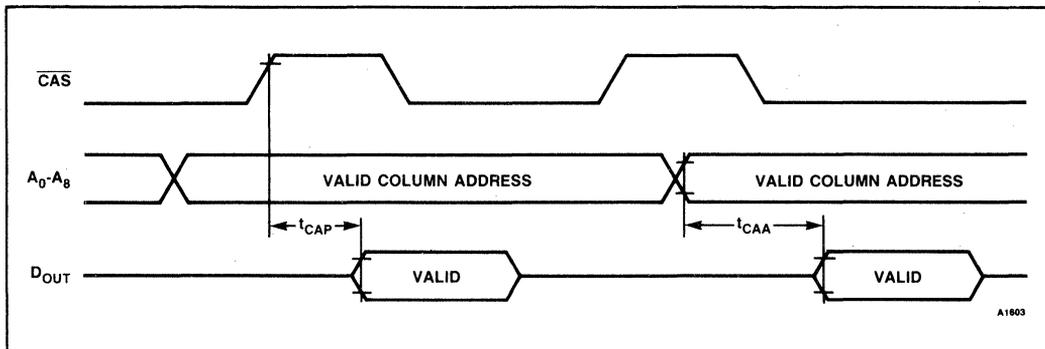


Figure 1. Ripplemode™ Access Time Determination



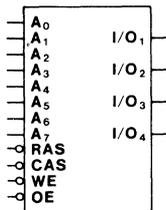
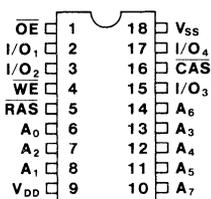
51C259H HIGH PERFORMANCE STATIC COLUMN 64K × 4 CHMOS DYNAMIC RAM

	51C259H-15	51C259H-20
Maximum Access Time (ns)	150	200
Maximum Column Address Access Time (ns)	70	90

- **Static Column Mode Operation**
 - Continuous data rate over 12 MHz
 - Random access from address within row
- **Low Input/Output Capacitance**
- **Low Operating Current - 65mA (max.)**
- **Fast "Usable Speed"**
 - $t_{CAC} = 30, 35 \text{ ns}$
 - $t_{OAC} = 25, 30 \text{ ns}$
- **Fully TTL Compatible**
- **High Reliability Plastic - 18 Pin DIP**

The Intel® 51C259H is a high speed 65,536 × 4 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C259H offers features not provided by an NMOS dynamic RAM: Static Column Mode for high data bandwidth and fast usable speed. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

Static Column Mode operation allows random or sequential access of all 256 bits within a row simply by changing the column address. Because column address access time is as fast as 70 ns, a continuous data rate of over 12 million 4 bit nibbles per second can be achieved. The 51C259H offers high performance while relaxing many critical system timing requirements for fast usable speed. These features make the 51C259H ideally suited for graphics, digital signal processing, and high performance systems.

LOGIC SYMBOL**PIN CONFIGURATION****PIN NAMES**

RAS	ROW ADDRESS STROBE
CAS	COLUMN ADDRESS STROBE
WE	WRITE ENABLE
OE	OUTPUT ENABLE
A ₀ -A ₇	ADDRESS INPUTS
I/O ₁ -I/O ₄	DATA IN/DATA OUT
V _{DD}	POWER (+5V)
V _{SS}	GROUND

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AUGUST, 1984
Order Number: 280033-001

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature	
Under Bias	-10°C to +80°C
Storage	
Temperature	Plastic -55°C to +125°C
Voltage on Any Pin except V _{DD} and D _{OUT}	
Relative to V _{SS}	-2.0V to 7.5V
Voltage on V _{DD}	
Relative to V _{SS}	-1.0V to 7.5V
Voltage on D _{OUT}	
Relative to V _{SS}	-2.0V to V _{DD} + 1V

Data Out Current	50 ma
Power Dissipation	1.0W

†COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C259H			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating			65	mA	t _{RC} = t _{RC(min)} , for -15 specification	3, 4
				50	mA	t _{RC} = t _{RC(min)} , for -20 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby			4	mA	RAS and CAS at V _{IH} , all other inputs and outputs ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, RAS-Only Refresh			65	mA	t _{RC} = t _{RC(min)} , for -15 specification	4
				50	mA	t _{RC} = t _{RC(min)} , for -20 specification	
I _{DD4}	V _{DD} Supply Current, Static Column Mode			65	mA	Minimum cycle for -15 specification	3, 4
				50	mA	Minimum cycle for -20 specification	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled			6	mA	RAS at V _{IH} , CAS and OE at V _{IL} , all other inputs and outputs ≥ V _{SS}	3
I _L	Input Load Current (any pin)			10	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current, High Impedance State			10	μA	RAS and CAS at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	-0.3		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage (all outputs)		0.4		V	I _{OL} = 4.2 mA	6
V _{OH}	Output High Voltage (all outputs)	2.4			V	I _{OH} = -5 mA	6

- NOTES:**
- All voltages referenced to V_{SS}.
 - Typical values are at T_A = 25°C and V_{DD} = +5V.
 - I_{DD} is dependent upon output loading when the device is selected. Specified I_{DD(max)} is measured with the output open.
 - I_{DD} is dependent upon the number of address transitions. Specified I_{DD(max)} is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Static Column Mode.
 - Specified V_{IL(min)} is steady state operation. During transitions, V_{IL} may undershoot to -1.0 V for periods not to exceed 20 ns. All A.C. parameters are measured with V_{IL(min)} ≥ V_{SS} and V_{IH(max)} ≤ V_{DD}.
 - Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured as noted in the A.C. Characteristics section.

CAPACITANCE†

$T_A = 25^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable Hewlett Packard capacitance meter.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	5	pF
C_{IN2}	RAS, \overline{CAS} , \overline{WE}	4	5	pF
$C_{I/O}$	Data In/Out	4	6	pF

A.C. CHARACTERISTICS^{1, 2, 3}

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write and Refresh Cycles

No.	JEDEC Symbol	Symbol	Parameter	51C259H-15		51C259H-20		Unit	Notes
				Min.	Max.	Min.	Max.		
1	tRL1RH1	tRAS	RAS Pulse Width	150	75000	200	75000	ns	
2	tRL2RL2	tRC	Random Read or Write Cycle Time	245		315		ns	
3	tRH2RL2	tRP	RAS Precharge Time	85		105		ns	
4	tRL1CH1	tCSH*	\overline{CAS} Hold Time	150		200		ns	
5	tCL1CH1	tCAS*	\overline{CAS} Pulse Width	30		35		ns	
6	tWH2RL2	tWRP	Write to RAS Precharge Time	10		10		ns	
7	tRL1WL2	tRWH	RAS to Write Hold Time	20		25		ns	
8	tAVRL2	tASR	Row Address Set-up Time	0		0		ns	
9	tRL1AX	tRAH	Row Address Hold Time	20		25		ns	
10	tCH2QZ	tHZ	\overline{OE} or \overline{CAS} to Output High Impedance		25		30	ns	4, 5
11	tCL2QX	tLZ	\overline{OE} or \overline{CAS} to Output Low Impedance	0		0		ns	4, 5
	tRVRV	tREF1	Time Between Refresh		4		4	ms	
	tT	tT	Transition Time (Rise and Fall)	3	25	3	25	ns	6

NOTES: * This parameter not applicable if operated with \overline{CAS} grounded.

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).
- A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with $V_{OL} = 0.8V$ at $I_{OL} = -2.2$ mA, $V_{OH} = 2.4V$ at $I_{OH} = -2.0$ mA with a 50 pF load, $V_{IL}(\text{min}) \geq V_{SS}$ and $V_{IH}(\text{max}) \leq V_{DD}$.
- Assumes three state test load (5 pF and a 380 Ohm Thevenin equivalent).
- At any given temperature and voltage combination, $t_{HZ}(\text{max}) \leq t_{LZ}(\text{min})$ from device to device.
- t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

A.C. CHARACTERISTICS (continued)

Read Cycle

No.	JEDEC Symbol	Symbol	Parameter	51C259H-15		51C259H-20		Unit	Notes
				Min.	Max.	Min.	Max.		
12	t _{RL1QV}	t _{RAC}	Access Time From \overline{RAS}		150		200	ns	7
13	t _{CL1QV}	t _{CAC}	Access Time From \overline{CAS}		30		35	ns	
14	t _{GL1QV}	t _{OAC}	Access Time From \overline{OE}		25		30	ns	
15	t _{AVQV}	t _{CAA}	Access Time From Column Address		70		90	ns	
16	t _{CL1RH1}	t _{RSH(R)*}	\overline{RAS} Hold Time (Read Cycle)	10		10		ns	
17	t _{WH2CL2}	t _{RCS*1}	Read Command Set-up Time	0		0		ns	
18	t _{AVRH1}	t _{CAR}	Column Address to \overline{RAS} Set-up Time	70		90		ns	
19	t _{RL1AX}	t _{ARR}	Column Address Hold Time From \overline{RAS} (Read)	140		190		ns	
20	t _{CH2WX}	t _{RCH*1}	Read Command Hold Time Referenced to \overline{CAS}	5		5		ns	
21	t _{RH2WX}	t _{RRH}	Read Command Hold Time Referenced to \overline{RAS}	10		10		ns	
22	t _{RH2AX}	t _{ARH}	Column Address Hold Time to \overline{RAS}	0		0		ns	
23	t _{RL1AV}	t _{RAD}	\overline{RAS} to Column Address Delay Time	25	80	30	110	ns	8
24	t _{AXQX}	t _{OHA}	Output Hold Time From Address Change	10		10		ns	
25	t _{GH1QX}	t _{OH}	Output Hold Time From \overline{OE} or \overline{CAS}	0		0		ns	

Write Cycle

26	t _{CL1RH1}	t _{RSH(W)}	\overline{RAS} Hold Time (Write Cycle)	35		40		ns	
27	t _{RL1WL2}	t _{WDR}	\overline{RAS} to Write Command Lead Time	30	115	35	160	ns	
28	t _{WL1RH1}	t _{RWL}	Write Command to \overline{RAS} Lead Time	30		35		ns	
29	t _{WL1CH1}	t _{CWL*}	Write Command to \overline{CAS} Lead Time	30		35		ns	
30	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	10		15		ns	
31	t _{WH2WL2}	t _{WCP}	Write Command Precharge Time	10		15		ns	
32	t _{WL1CL2}	t _{WCS*}	Write Command Set-up Time	0		0		ns	9
33	t _{CL1WH1}	t _{WCH*}	Write Command Hold Time	30		35		ns	
34	t _{RL1WH1}	t _{WCR}	Write Command Hold Time From \overline{RAS}	100		110		ns	
35	t _{AVWL2}	t _{AWS}	Column Address to Write Command Set-up Time	5		5		ns	
36	t _{WL1AX}	t _{AWH}	Column Address to Write Command Hold Time	25		30		ns	

- NOTES:**
- * This parameter not applicable if operated with \overline{CAS} grounded.
 - 7. Assumes that $t_{RAD} \leq t_{RAD(max)}$ if $t_{RAD} > t_{RAD(max)}$, then t_{RAC} will increase by the amount that t_{RAD} exceeds $t_{RAD(max)}$.
 - 8. t_{RAD} is specified for reference only.
 - 9. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{OWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is a \overline{CAS} controlled write cycle and the data out pin will remain in high impedance for the duration of \overline{WE} low. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{OWD} \geq t_{OWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.

A.C. CHARACTERISTICS (continued)

Write Cycle (Continued)

No.	JEDEC Symbol	Symbol	Parameter	51C259H-15		51C259H-20		Unit	Notes
				Min.	Max.	Min.	Max.		
37	tRL1AX	tARW	Column Address Hold Time From $\overline{\text{RAS}}$ (Write)	60		70		ns	
38	tDVWL2	tDS	Data-In Set-up Time	5		5		ns	
39	tWL1DX	tDH	Data-In Hold Time	25		30		ns	
40	tGH2WH1	tOWS	$\overline{\text{OE}}$ Set-up Time From End of Write	15		20		ns	
41	tCH2GL2	tCOH	$\overline{\text{OE}}$ Hold Time From $\overline{\text{CAS}}$	20		25		ns	

Read-Modify-Write Cycle ¹⁰

42	tR_2RL2	tRWC	Read-Modify-Write (RMW) Cycle Time	310		390		ns	
43	tRL1RH1	tRRW	$\overline{\text{RAS}}$ Pulse Width (RMW)	215	75000	275	75000	ns	
44	tCL1CH1	tCRW	$\overline{\text{CAS}}$ Pulse Width (RMW)	95		110		ns	
45	tRL1AX	tAR	Column Address Hold Time From $\overline{\text{RAS}}$ (RMW)	205		265		ns	
46	tRL1WL2	tRWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	180		235		ns	11
47	tAVWL2	tAWD	Column Address to $\overline{\text{WE}}$ Delay	100		115		ns	11
48	tCL1WL2	tCWD*	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	60		70		ns	11
49	tGH2WL2	tOWD	$\overline{\text{OE}}$ to $\overline{\text{WE}}$ Delay	30		35		ns	11

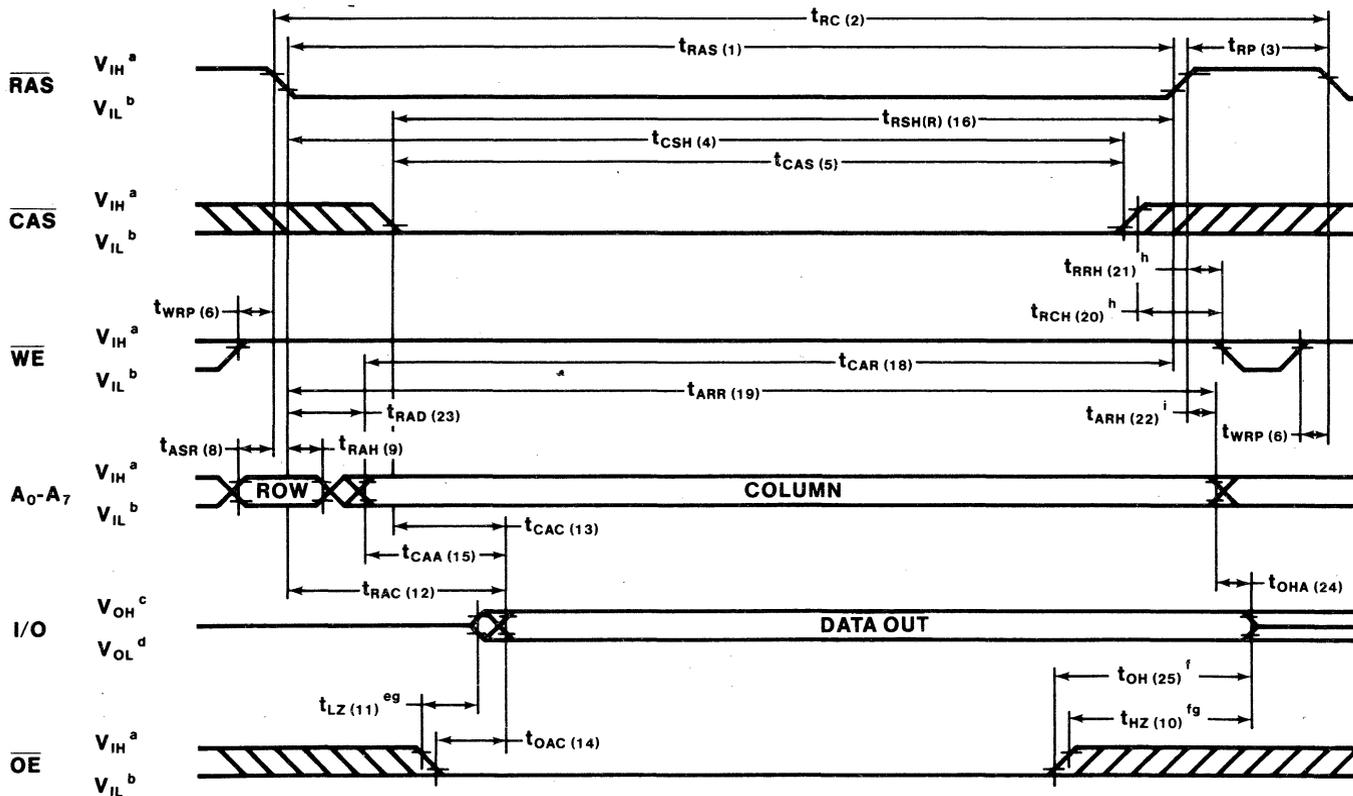
Static Column Mode ¹²

50	tWL2WL2	tSWC	Static Column Write Cycle Time	50		55		ns	
51	tWH2QV	tWPA	Write Precharge Access Time		30		35	ns	13
52	tWL1QV	tWRA	Write-Read Access Time		120		135	ns	13
53	tWL1GL2	tWOH	Write to $\overline{\text{OE}}$ Hold Time	30		35		ns	
54	tRL1WL1	tSWH	$\overline{\text{RAS}}$ to Write Command Hold Time	150		200		ns	

NOTES: * This parameter not applicable if operated with $\overline{\text{CAS}}$ grounded.

10. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
11. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{OWD} are specified as reference points only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is a $\overline{\text{CAS}}$ controlled write cycle and the data out pin will remain in high impedance for the duration of $\overline{\text{WE}}$ low. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{OWD}} \geq t_{\text{OWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition is of data out indeterminate.
12. All previously specified A.C. characteristics are applicable.
13. Access time from a write command to a read command is determined by the longer of t_{CAA} or t_{WPA} or t_{WRA} .

WAVEFORMS READ CYCLE



NOTE: a. b. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals.

c. d. $V_{OH}(\min)$ and $V_{OL}(\max)$ are reference levels for measuring timing of D_{OUT} .

e. t_{LZ} is referenced to the later of RAS, CAS, and OE low transition.

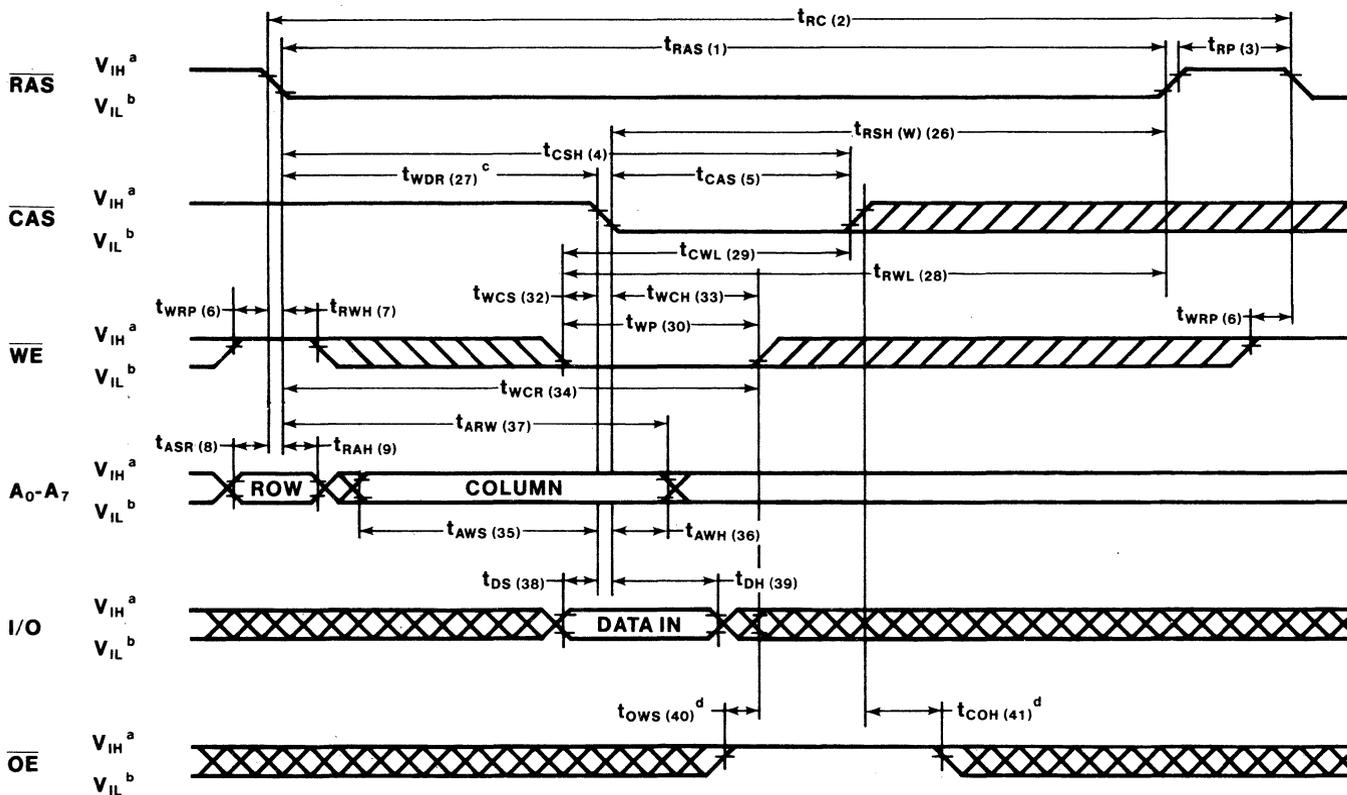
f. t_{HZ} and t_{OH} are referenced to the earlier of CAS or OE high transition.

g. Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

h. Either t_{RCH} or t_{RRH} must be satisfied.

i. If $t_{ARH} \geq t_{ARH}(\min)$, then data from the last address will be latched on D_{OUT} by a RAS high transition, until either a CAS or OE high transition releases the data.

WAVEFORMS (Cont'd.) WRITE CYCLE (CAS Controlled) ^e

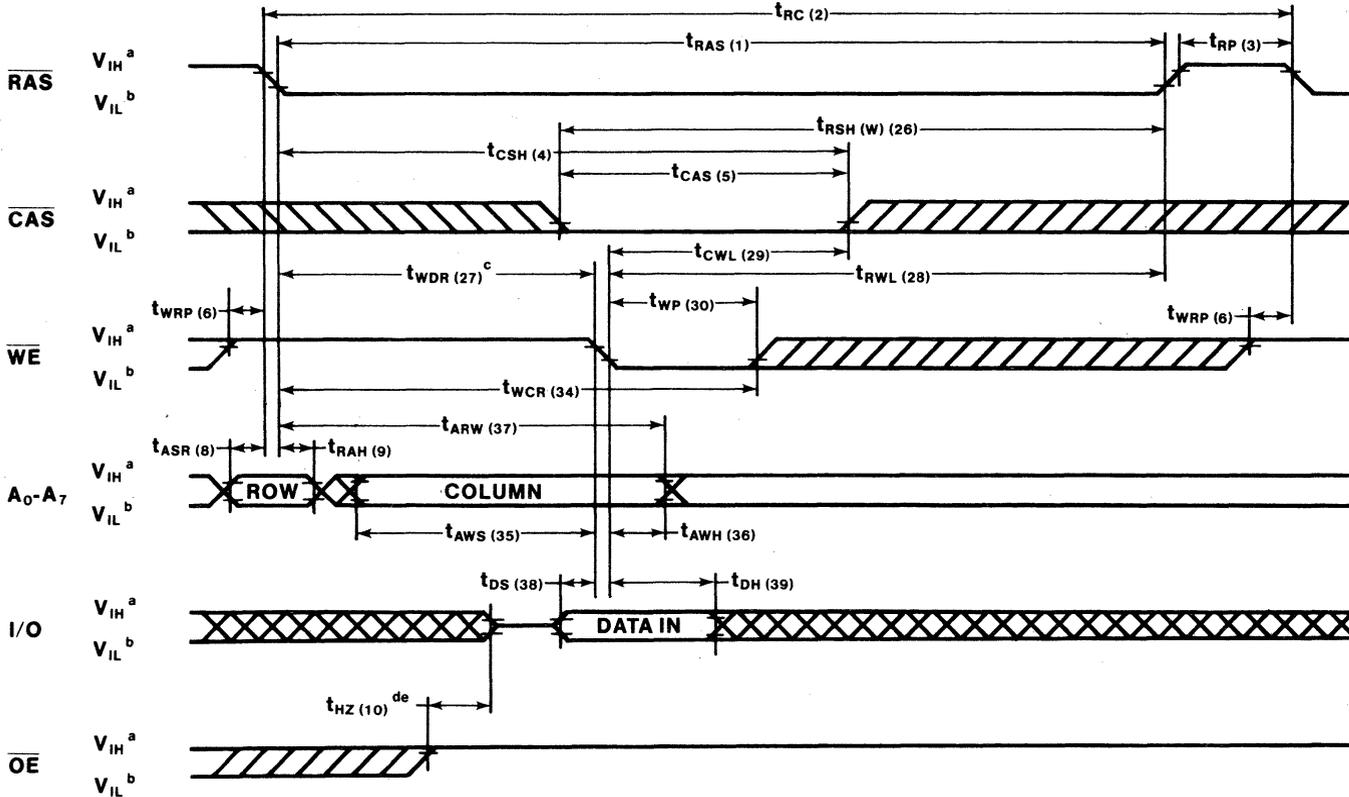


NOTE: a. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 b. t_{WDR} is reference to the later of the CAS or WE low transition.
 c. t_{WDR} is reference to the later of the CAS or WE low transition.
 d. If the low transition of WE occurs before or simultaneously with the low transition of CAS and the high transition of CAS or RAS occurs before the high transition of WE, then the outputs remain in a high impedance state (i.e., OE is a don't care).
 e. WE is low prior to or simultaneously with CAS low transition. CAS is high prior to RAS low transition.

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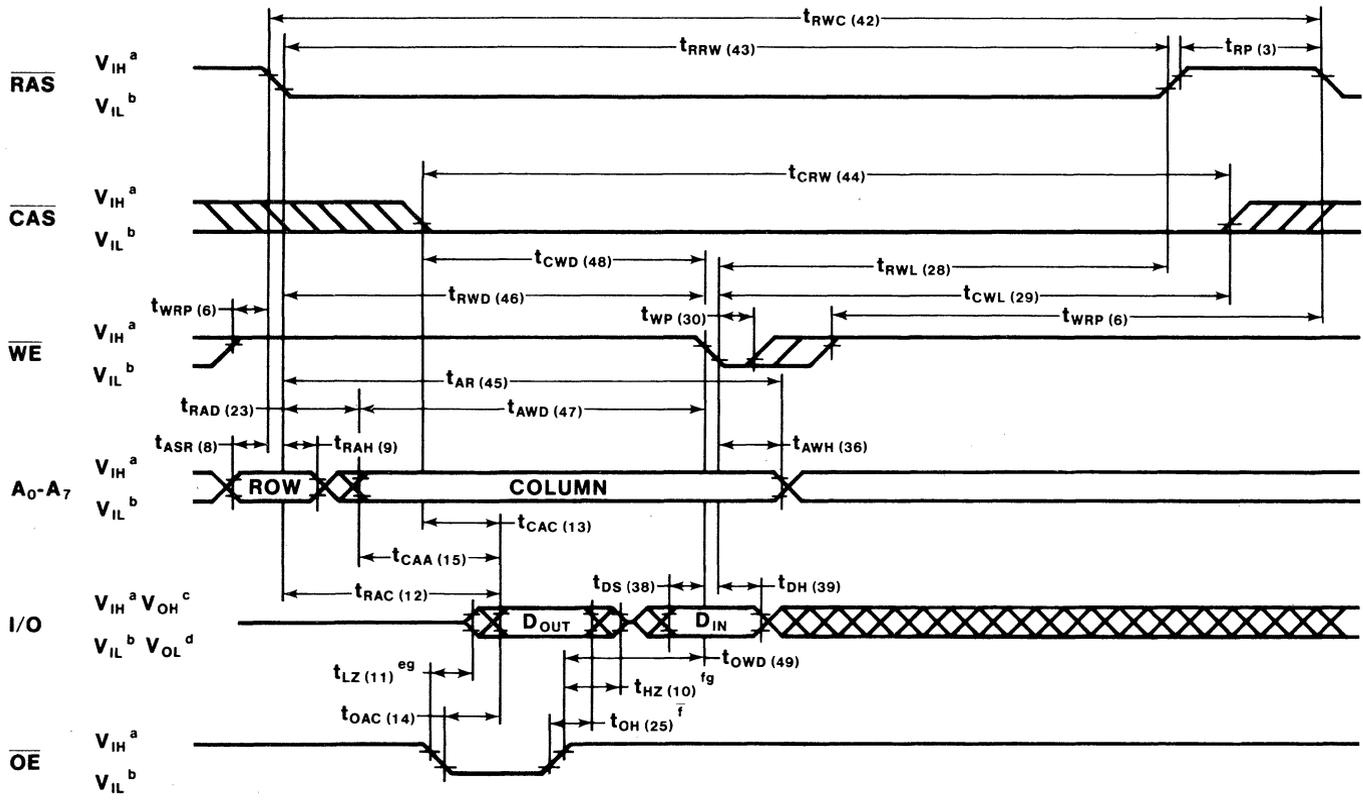
C1609

WAVEFORMS (Cont'd.) WRITE CYCLE (WE Controlled) ^f



- NOTE: a. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c. t_{WDR} is reference to the later of the CAS or WE low transition.
 d. t_{HZ} is referenced to the earlier of the CAS or OE high transition or WE low transition.
 e. Transition is measured + 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 f. CAS is low prior to the WE low transition.

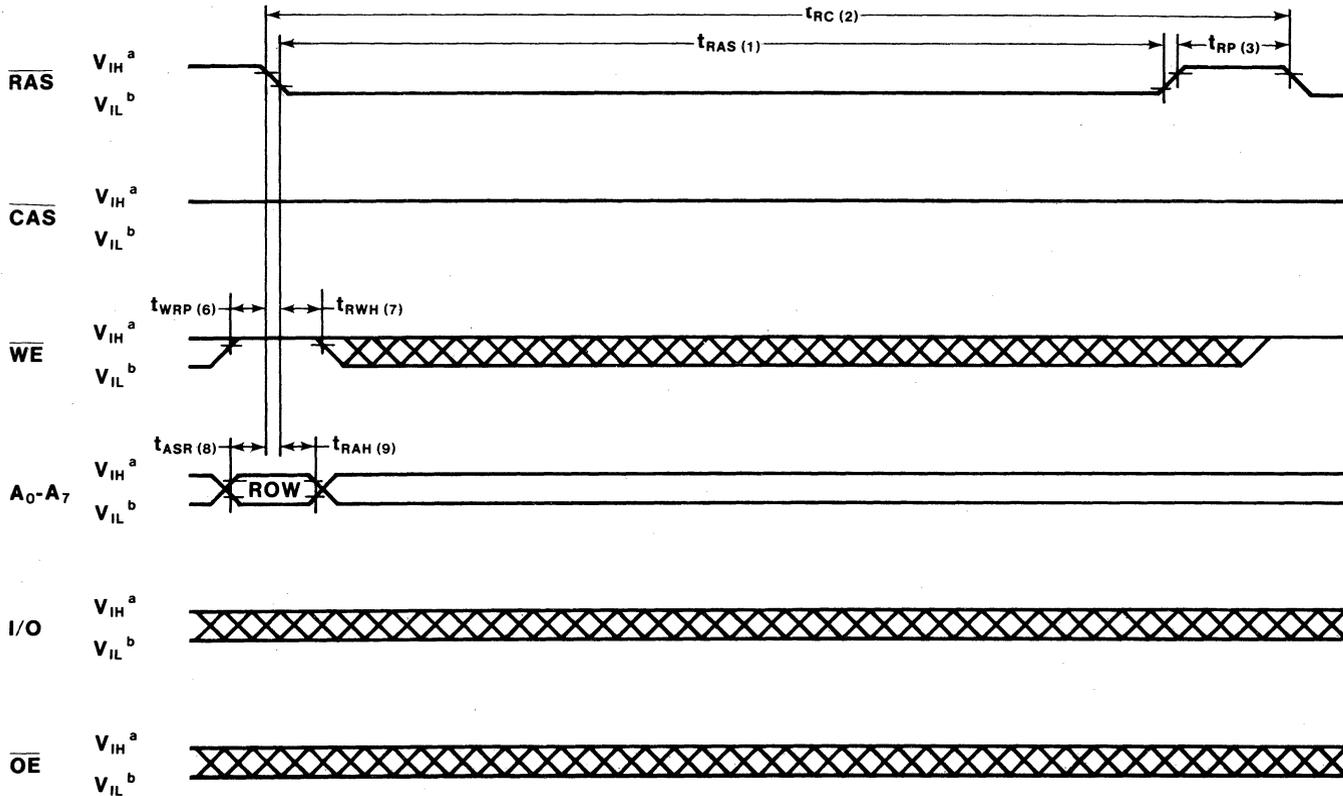
WAVEFORMS (Cont'd.) READ/MODIFY/WRITE CYCLE



2-111

- NOTE:**
- a.. b. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.
 - c.. d. $V_{OH}(\text{min})$ and $V_{OL}(\text{max})$ are reference levels for measuring timing of D_{OUT} .
 - e. t_{LZ} is referenced to the later of RAS, CAS, and OE low transition.
 - f. t_{HZ} and t_{OH} are referenced to the earlier of the CAS or OE high transition.
 - g. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

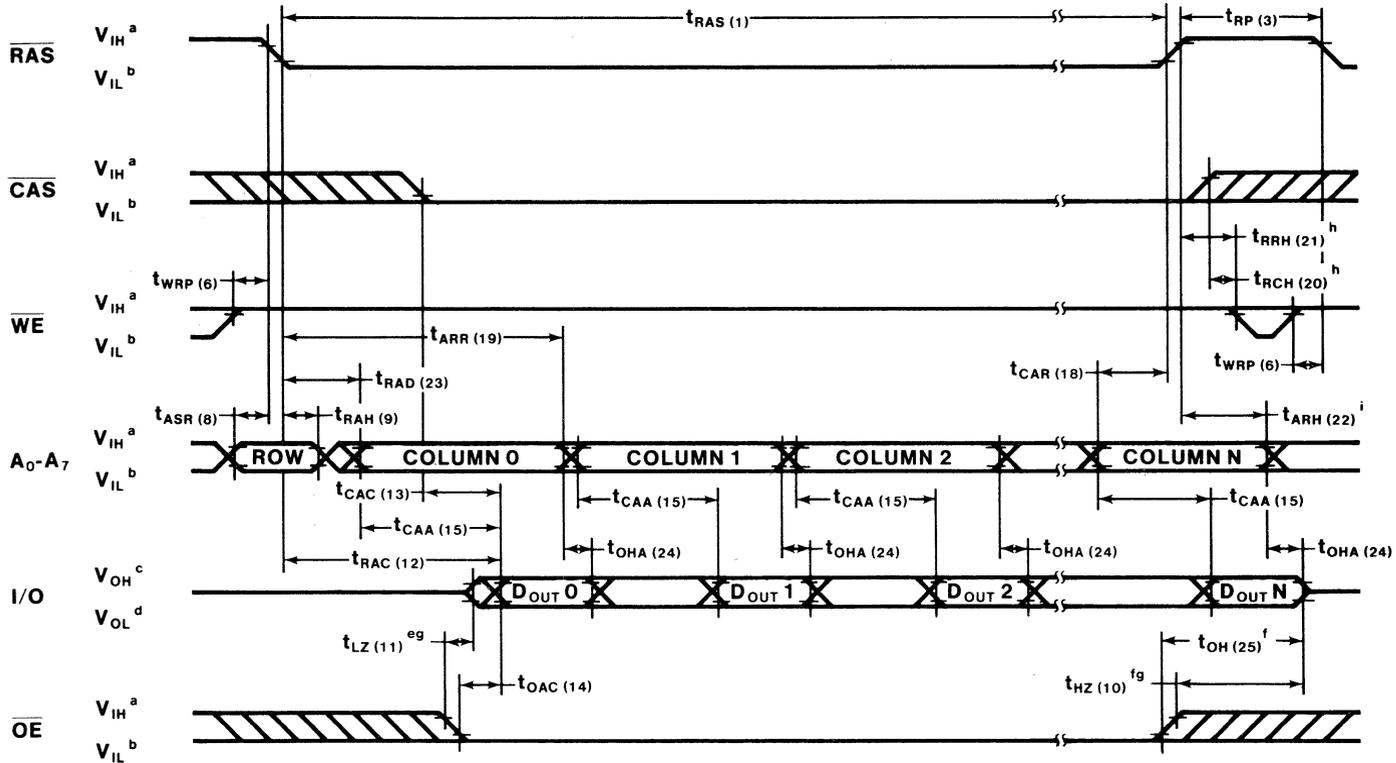
WAVEFORMS (Cont'd.) RAS-ONLY REFRESH CYCLE



NOTE: a.. b. $V_{IH} (min)$ and $V_{IL} (max)$ are reference levels for measuring timing of input signals.

C1612

WAVEFORMS (Cont'd.) STATIC COLUMN MODE READ CYCLE



NOTE: a. b. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals.

c. d. $V_{OH}(\min)$ and $V_{OL}(\max)$ are reference levels for measuring timing of D_{OUT} .

e. t_{LZ} is referenced to the later of RAS, CAS, and OE low transition.

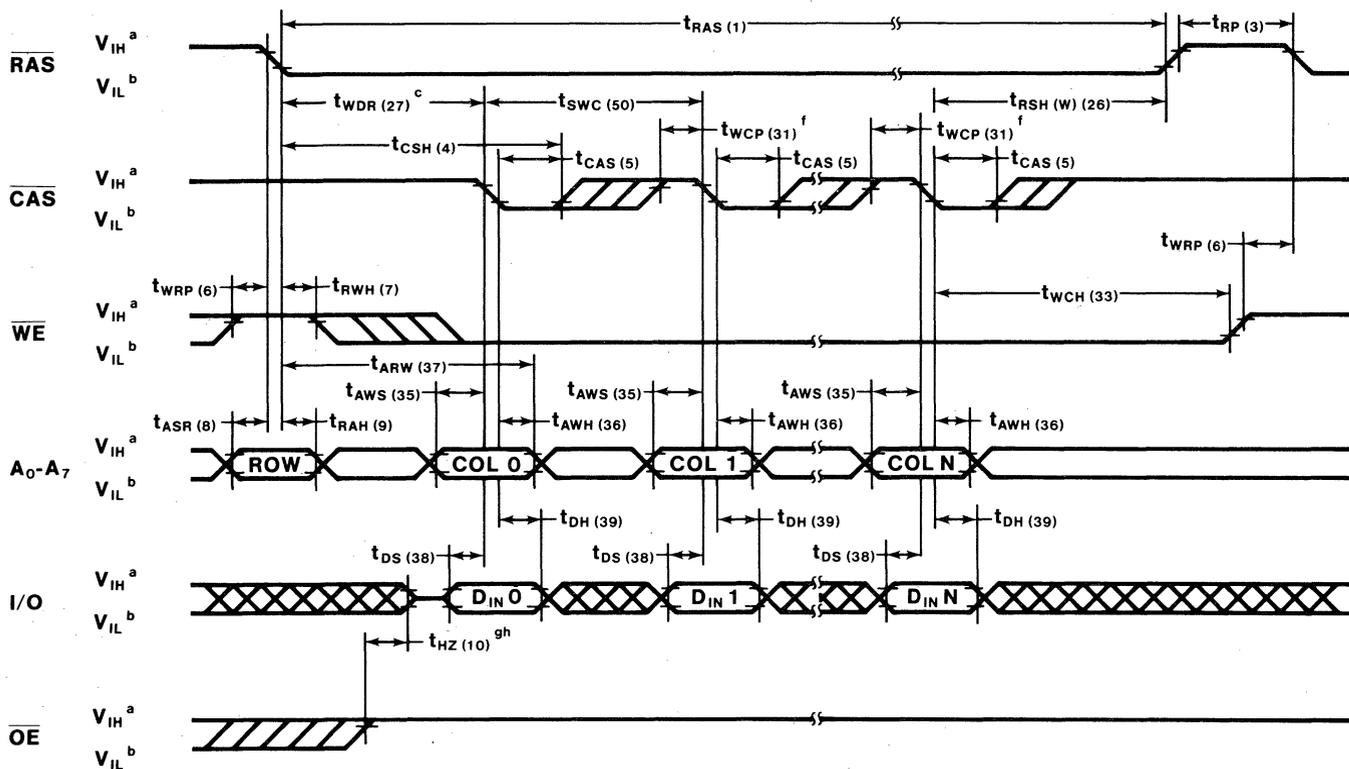
f. t_{HZ} and t_{OH} are referenced to the earlier of the CAS or OE high transition.

g. Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

h. Either t_{RCH} or t_{RRH} must be satisfied.

i. If $t_{ARR} > t_{ARR}(\min)$, then data from the last address will be latched on D_{OUT} by a \overline{RAS} high transition, until either a \overline{CAS} or \overline{OE} high transition releases the data.

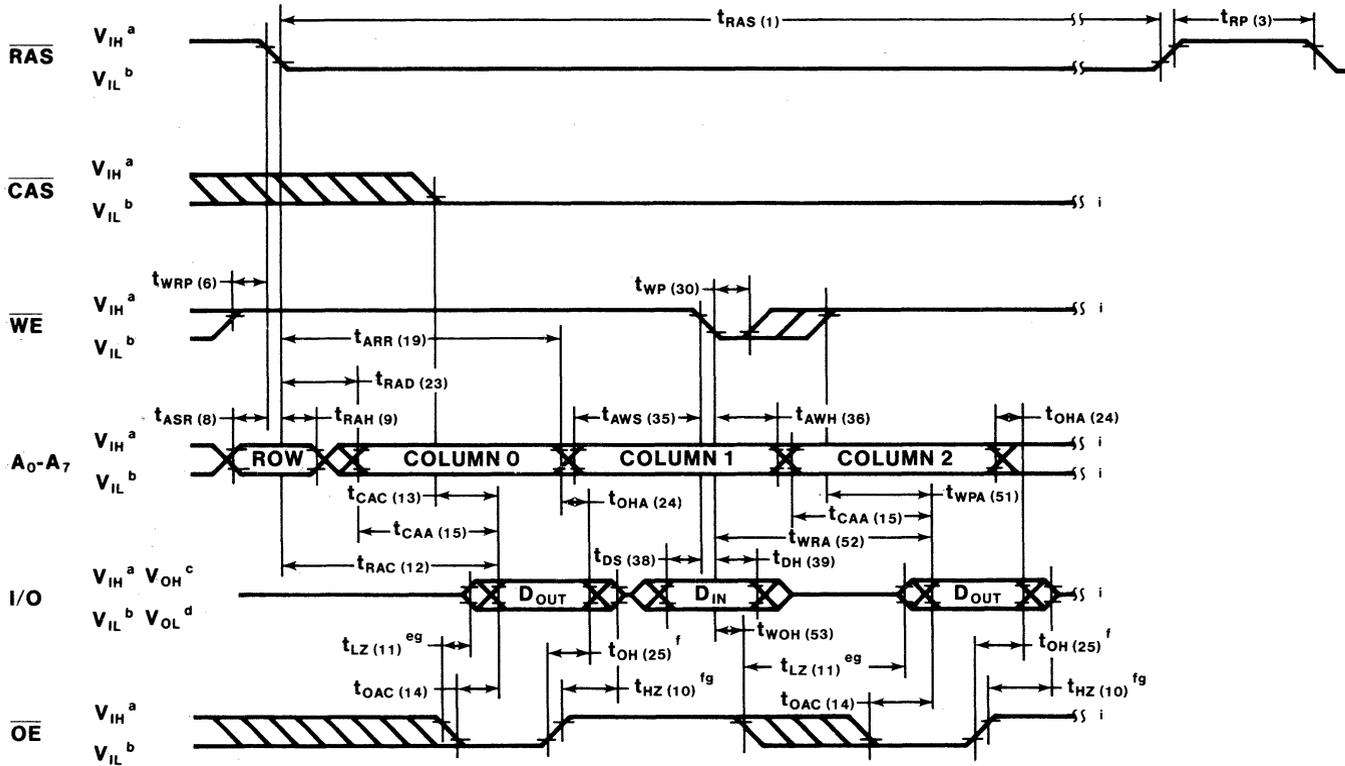
WAVEFORMS (Cont'd.) STATIC COLUMN MODE WRITE CYCLE (CAS Controlled) ⁹



- NOTE:** a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c. t_{WDR} is reference to the later of the CAS or WE low transition.
 d. t_{HZ} is referenced to the earlier of the CAS or OE high transition or WE low transition.
 e. Transition is measured + 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 f. t_{WCP} is measured from the earlier of CAS or WE high transition to the later of CAS or WE low transition.
 g. WE is low prior to or simultaneously with a CAS low transition. CAS is high prior to a RAS low transition.

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WAVEFORMS (Cont'd.) STATIC COLUMN MODE READ/WRITE/READ . . . CYCLE (\overline{WE} Controlled) ^h



- NOTE:** a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 e. t_{LZ} is referenced to the later of \overline{RAS} , \overline{CAS} , and \overline{OE} low transition if \overline{RAS} and \overline{CAS} and \overline{OE} are low.
 f. t_{LZ} and t_{OH} are referenced to the earlier of \overline{CAS} or \overline{OE} high transition.
 g. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 h. \overline{CAS} is low prior to a \overline{WE} low transition.
 i. The cycle can be terminated by either a read or a write operation followed by a \overline{RAS} high transition. See pages 11 or 13 for timings.

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FUNCTIONAL DESCRIPTION

The 51C259H is a CHMOS dynamic RAM optimized for high data bandwidth applications. The functionality is similar to a traditional dynamic RAM. The 51C259H reads and writes 4 bits of data at a time by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe ($\overline{\text{RAS}}$). The column address, however, is only latched during a write cycle by the later of either Column Address Strobe ($\overline{\text{CAS}}$) or Write Enable ($\overline{\text{WE}}$). During the read cycle, the column address is not latched and continuously flows through the internal input latches. Access time is primarily dependent upon a valid column address. $\overline{\text{CAS}}$ acts as chip select signal and can remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}$ operation. The column address must be held for a minimum time specified by t_{ARR} . $\overline{\text{CAS}}$ may either be held low or be pulsed similar to the traditional $\overline{\text{CAS}}$ operation. Data out is controlled by the Out Enable ($\overline{\text{OE}}$) and $\overline{\text{CAS}}$ which is discussed in the Data Out Operation.

For applications where $\overline{\text{CAS}}$ is held low, the data out becomes valid when t_{RAC} , t_{CAA} and t_{OAC} are all satisfied.

For applications where $\overline{\text{CAS}}$ is pulsed similar to the traditional $\overline{\text{CAS}}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. Data out becomes valid only when t_{RAC} , t_{CAA} , t_{OAC} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} , t_{OAC} , and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} , t_{OAC} , and t_{CAC} are all satisfied.

Write Cycle

A write cycle is performed by taking $\overline{\text{WE}}$ low during a $\overline{\text{RAS}}$ operation. The column address is

latched in by the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$. As in the read cycle, $\overline{\text{CAS}}$ may either be held low or be pulsed similar to the traditional $\overline{\text{CAS}}$ operation. For applications where $\overline{\text{CAS}}$ is held low, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$. For applications where $\overline{\text{CAS}}$ is pulsed similar to the traditional $\overline{\text{CAS}}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Consequently, the write cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending upon the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ low transition. In a $\overline{\text{CAS}}$ controlled write cycle (the leading edge of $\overline{\text{WE}}$ occurs prior to or coincident with the $\overline{\text{CAS}}$ low transition) the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ will maintain the I/O in the high impedance state; terminating with $\overline{\text{WE}}$ allows the output to go active, and the $\overline{\text{OE}}$ must be brought high to allow for inputs on the I/O.

The 51C259H incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write function has been initiated, the 51C259H internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{\text{RAS}}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or RAS-Only cycle will perform refresh.

Static Column Mode Operation

Static column mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Read, write, and read-write-read cycles can be performed during static column mode operation. The row address is internally retained by maintaining $\overline{\text{RAS}}$ active. Following the entry cycle into static column mode operation, the data is accessed simply by changing the column address. Because the column address buffer acts as a transparent or flow-through latch, access begins from a valid column address.

Thus, the 51C259H operates like a static RAM for multiple accesses within the same row. $\overline{\text{CAS}}$ acts as a chip select. Intel's Application Note 172, *CHMOS DRAMS in Graphics Applications*, provides more details on static column mode operation.

Data Out Operation

The 51C259H Input/Output (I/O) is controlled by $\overline{\text{OE}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and $\overline{\text{RAS}}$. A $\overline{\text{RAS}}$ low transition enables data to transfer into and from a selected row address. A $\overline{\text{RAS}}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{\text{RAS}}$ low transition, a $\overline{\text{CAS}}$ low transition or a $\overline{\text{CAS}}$ low level enables the internal I/O data path. A $\overline{\text{CAS}}$ high transition or a $\overline{\text{CAS}}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{\text{CAS}}$ low transition while $\overline{\text{RAS}}$ is high has no effect on the I/O data path, nor on the output driver. An $\overline{\text{OE}}$ low transition or an $\overline{\text{OE}}$ low level enables the output driver when the I/O data path is enabled. An $\overline{\text{OE}}$ high transition or an $\overline{\text{OE}}$ high level disables the output driver, but does not disable the data latch when it has been enabled. A $\overline{\text{WE}}$ low level disables the output driver when a $\overline{\text{CAS}}$ low level occurs. If the $\overline{\text{WE}}$ low transition occurs after the $\overline{\text{CAS}}$ low transition such that the output driver is enabled prior to the $\overline{\text{WE}}$ low transition, it

is necessary to use $\overline{\text{OE}}$ to disable the output driver prior to the $\overline{\text{WE}}$ low transition to allow data in set-up time (t_{DS}). A $\overline{\text{WE}}$ high transition passes control of the output drive to $\overline{\text{OE}}$.

Power On

An initial pause of 100 μS is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).

The V_{DD} current (I_{DD}) requirement of the 51C259H during power on is dependent upon the input levels of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. If $\overline{\text{RAS}} = V_{\text{SS}}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{DD} or be held at a valid V_{IH} during power on.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

51C259L LOW POWER 64K × 4 CHMOS DYNAMIC RAM

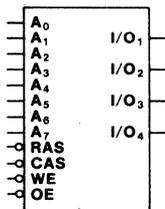
	51C259L-15	51C259L-20
Maximum Access Time (ns)	150	200
Maximum CHMOS Standby Current (mA)	0.1	0.1

- Low Power Data Retention
 - Standby current, CHMOS - 100 μ A (max.)
 - Refresh period, $\overline{\text{RAS}}$ -Only - 32 ms (max.)
 - Data retention current - 230 μ A (max.)
 - Low Operating Current - 65 mA (max.)
- TTL And HCT Compatible
 - Low Input/Output Capacitance
 - High Reliability Plastic - 18 Pin DIP
 - Column Address Not Latched During Read Cycle

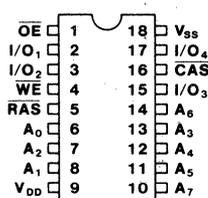
The Intel® 51C259L is a low power 65,536 × 4 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C259L offers features not provided by an NMOS dynamic RAM: CHMOS standby current and extended $\overline{\text{RAS}}$ -Only refresh for low standby power. All inputs and outputs are compatible to both TTL and HCT logic families while the input and output capacitances are significantly lowered to allow increased system performance.

The 51C259L offers a maximum standby current of 100 μ A when $\overline{\text{RAS}} \geq V_{\text{DD}} - 0.5\text{V}$. During standby (i.e. refresh only cycles), the refresh period can be extended to 32 ms to reduce the total current required to retain data to less than 230 μ A (max.). The 51C259L combines this low power with high density for portable and battery backup applications.

LOGIC SYMBOL



PIN CONFIGURATION



PIN NAMES

RAS	ROW ADDRESS STROBE
CAS	COLUMN ADDRESS STROBE
WE	WRITE ENABLE
OE	OUTPUT ENABLE
A ₀ -A ₇	ADDRESS INPUTS
I/O ₁ -I/O ₄	DATA IN/DATA OUT
V _{DD}	POWER (+5V)
V _{SS}	GROUND

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

ABSOLUTE MAXIMUM RATINGS†

Data Out Current 50 ma
 Power Dissipation 1.0W

Ambient Temperature
 Under Bias -10°C to + 80°C
 Storage
 Temperature ... Plastic -55°C to + 125°C
 Voltage on Any Pin except V_{DD} and D_{OUT}
 Relative to V_{SS} -2.0V to 7.5V
 Voltage on V_{DD}
 Relative to V_{SS} -1.0V to 7.5V
 Voltage on D_{OUT}
 Relative to V_{SS} -2.0V to V_{DD} + 1V

†COMMENT
 Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C259L			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating			65	mA	t _{RC} = t _{RC(min)} , for -15 specification	3, 4
				50	mA	t _{RC} = t _{RC(min)} , for -20 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby			4	mA	\overline{RAS} and \overline{CAS} at V _{IH} , all other inputs and outputs ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, RAS-Only Refresh			65	mA	t _{RC} = t _{RC(min)} , for -15 specification	4
				50	mA	t _{RC} = t _{RC(min)} , for -20 specification	
I _{DD5}	V _{DD} Supply Current Standby, Output Enabled			6	mA	\overline{RAS} at V _{IH} , \overline{CAS} and \overline{OE} at V _{IL} , all other inputs and outputs ≥ V _{SS}	3
I _{DD6}	V _{DD} Supply Current, CHMOS Standby		0.01	0.1	mA	\overline{RAS} and \overline{CAS} ≥ V _{DD} - 0.5V, all other inputs and output ≥ V _{SS}	
I _L	Input Load Current (any pin)			1	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current, High Impedance State			5	μA	\overline{RAS} and \overline{CAS} at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	-0.3		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage (all outputs)			0.4	V	I _{OL} = 4.2 mA	6
				0.1	V	I _{OL} = 100 μA	
V _{OH}	Output High Voltage (all outputs)	2.4			V	I _{OH} = -5 mA	6
		V _{DD} - 0.1			V	I _{OH} = -100 μA	

- NOTES:**
1. All voltages referenced to V_{SS}.
 2. Typical values are at T_A = 25°C and V_{DD} = +5V.
 3. I_{DD} is dependent upon output loading when the device is selected. Specified I_{DD(max)} is measured with the output open.
 4. I_{DD} is dependent upon the number of address transitions. Specified I_{DD(max)} is measured with a maximum of two transitions per address input per random cycle.
 5. Specified V_{IL(min)} is steady state operation. During transitions, V_{IL} may undershoot to -1.0V for periods not to exceed 20 ns. All A.C. parameters are measured with V_{IL(min)} ≥ V_{SS} and V_{IH(max)} ≤ V_{DD}.
 6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured as noted in the A.C. Characteristics section.

CAPACITANCE†
†NOTE:
 $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Capacitance is measured at worst case voltage levels with a programmable Hewlett Packard capacitance meter.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	5	pF
C_{IN2}	$\overline{\text{RAS}}$, CAS , $\overline{\text{WE}}$	4	5	pF
$C_{I/O}$	Data In/Out	4	6	pF

A.C. CHARACTERISTICS^{1, 2, 3}
 $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Read, Write and Refresh Cycles

No.	JEDEC Symbol	Symbol	Parameter	51C259L-15		51C259L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	150	75000	200	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	245		315		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	85		105		ns	
4	t_{RL1CH1}	t_{CSH}^*	$\overline{\text{CAS}}$ Hold Time	150		200		ns	
5	t_{CL1CH1}	t_{CAS}^*	$\overline{\text{CAS}}$ Pulse Width	30		35		ns	
6	t_{WH2RL2}	t_{WRP}	Write to $\overline{\text{RAS}}$ Precharge Time	10		10		ns	
7	t_{RL1WL2}	t_{RWH}	$\overline{\text{RAS}}$ to Write Hold Time	20		25		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	20		25		ns	
10	t_{CH2QZ}	t_{HZ}	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to Output High Impedance		25		30	ns	4, 5
11	t_{CL2QX}	t_{LZ}	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to Output Low Impedance	0		0		ns	4, 5
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4	ms	6
	t_{RVRV}	t_{REF2}	Time Between Refresh ($\overline{\text{RAS}}$ -Only)		32		32	ms	6
	t_T	t_T	Transition Time (Rise and Fall)	3	25	3	25	ns	7

NOTES: * This parameter not applicable if operated with $\overline{\text{CAS}}$ grounded.

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).
- A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with $V_{OL} = 0.8\text{V}$ at $I_{OL} = 2.2$ mA, $V_{OH} = 2.4\text{V}$ at $I_{OH} = -2.0$ mA with a 50 pF load, $V_{IL}(\text{min}) \geq V_{SS}$ and $V_{IH}(\text{max}) \leq V_{DD}$.
- Assumes three state test load (5 pF and a 380 Ohm Thevenin equivalent).
- At any given temperature and voltage combination, $t_{HZ}(\text{max}) \leq t_{LZ}(\text{min})$ from device to device.
- The 51C259L extends the refresh period to 32 ms during $\overline{\text{RAS}}$ -Only refresh periods.
- t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

A.C. CHARACTERISTICS (continued)

Read Cycle

No.	JEDEC Symbol	Symbol	Parameter	51C259L-15		51C259L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
12	t _{RL1QV}	t _{RAC}	Access Time From \overline{RAS}		150		200	ns	8
13	t _{CL1QV}	t _{CAC}	Access Time From \overline{CAS}		30		35	ns	
14	t _{GL1QV}	t _{OAC}	Access Time From \overline{OE}		25		30	ns	
15	t _{AVQV}	t _{CAA}	Access Time From Column Address		70		90	ns	
16	t _{CL1RH1}	t _{RSH(R)*}	\overline{RAS} Hold Time (Read Cycle)	10		10		ns	
17	t _{WH2CL2}	t _{RCS*}	Read Command Set-up Time	0		0		ns	
18	t _{AVRH1}	t _{CAR}	Column Address to \overline{RAS} Set-up Time	70		90		ns	
19	t _{RL1AX}	t _{ARR}	Column Address Hold Time From \overline{RAS} (Read)	140		190		ns	
20	t _{CH2WX}	t _{RCH*}	Read Command Hold Time Referenced to \overline{CAS}	5		5		ns	
21	t _{RH2WX}	t _{RRH}	Read Command Hold Time Referenced to \overline{RAS}	10		10		ns	
22	t _{RH2AX}	t _{ARH}	Column Address Hold Time to \overline{RAS}	0		0		ns	
23	t _{RL1AV}	t _{RAD}	\overline{RAS} to Column Address Delay Time	25	80	30	110	ns	9
24	t _{AXQX}	t _{OHA}	Output Hold Time From Address Change	10		10		ns	
25	t _{GH1QX}	t _{OH}	Output Hold Time From \overline{OE} or \overline{CAS}	0		0		ns	

Write Cycle

26	t _{CL1RH1}	t _{RSH(W)}	\overline{RAS} Hold Time (Write Cycle)	35		40		ns	
27	t _{RL1WL2}	t _{WDR}	\overline{RAS} to Write Command Lead Time	30	115	35	160	ns	
28	t _{WL1RH1}	t _{RWL}	Write Command to \overline{RAS} Lead Time	30		35		ns	
29	t _{WL1CH1}	t _{CWL*}	Write Command to \overline{CAS} Lead Time	30		35		ns	
30	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	10		15		ns	
31	t _{WH2WL2}	t _{WCP}	Write Command Precharge Time	10		15		ns	
32	t _{WL1CL2}	t _{WCS*}	Write Command Set-up Time	0		0		ns	10
33	t _{CL1WH1}	t _{WCH*}	Write Command Hold Time	30		35		ns	
34	t _{RL1WH1}	t _{WCR}	Write Command Hold Time From \overline{RAS}	100		110		ns	
35	t _{AVWL2}	t _{AWS}	Column Address to Write Command Set-up Time	5		5		ns	
36	t _{WL1AX}	t _{AWH}	Column Address to Write Command Hold Time	25		30		ns	

NOTES: * This parameter not applicable if operated with \overline{CAS} grounded.

8. Assumes that $t_{RAD} \leq t_{RAD(max)}$ if $t_{RAD} > t_{RAD(max)}$, then t_{RAC} will increase by the amount that t_{RAD} exceeds $t_{RAD(max)}$.

9. t_{RAD} is specified for reference only.

10. t_{WCS} , t_{RWd} , t_{CWd} , t_{AWd} and t_{OWd} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is a \overline{CAS} controlled write cycle and the data out pin will remain in high impedance for the duration of WE low. If $t_{CWd} \geq t_{CWd(min)}$ and $t_{RWd} \geq t_{RWd(min)}$ and $t_{OWd} \geq t_{OWd(min)}$ and $t_{AWd} \geq t_{AWd(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.

A.C. CHARACTERISTICS (continued)

Write Cycle (Continued)

No.	JEDEC Symbol	Symbol	Parameter	51C259L-15		51C259L-20		Unit	Notes
				Min.	Max.	Min.	Max.		
37	tRL1AX	tARW	Column Address Hold Time From $\overline{\text{RAS}}$ (Write)	60		70		ns	
38	tDVWL2	tDS	Data-In Set-up Time	5		5		ns	
39	tWL1DX	tDH	Data-In Hold Time	25		30		ns	
40	tGH2WH1	tOWS	$\overline{\text{OE}}$ Set-up Time From End of Write	15		20		ns	
41	tCH2GL2	tCOH	$\overline{\text{OE}}$ Hold Time From $\overline{\text{CAS}}$	20		25		ns	

Read-Modify-Write Cycle ¹¹

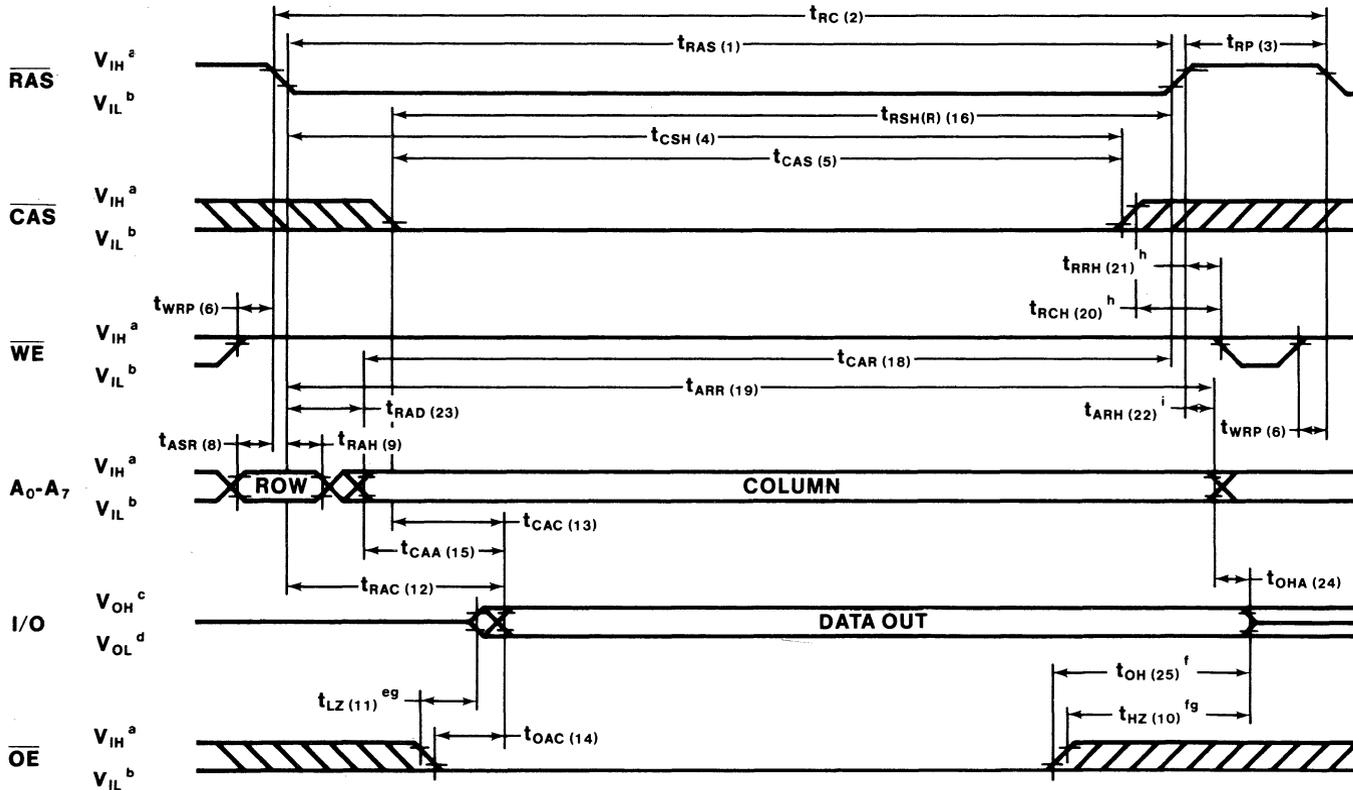
42	tRL2RL2	tRWC	Read-Modify-Write (RMW) Cycle Time	310		390		ns	
43	tRL1RH1	tRRW	$\overline{\text{RAS}}$ Pulse Width (RMW)	215	75000	275	75000	ns	
44	tCL1CH1	tCRW	$\overline{\text{CAS}}$ Pulse Width (RMW)	95		110		ns	
45	tRL1AX	tAR	Column Address Hold Time From $\overline{\text{RAS}}$ (RMW)	205		265		ns	
46	tRL1WL2	tRWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	180		235		ns	12
47	tAWL2	tAWD	Column Address to $\overline{\text{WE}}$ Delay	100		115		ns	12
48	tCL1WL2	tCWD*	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	60		70		ns	12
49	tGH2WL2	tOWD	$\overline{\text{OE}}$ to $\overline{\text{WE}}$ Delay	30		35		ns	12

NOTES: * This parameter not applicable if operated with $\overline{\text{CAS}}$ grounded.

11. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.

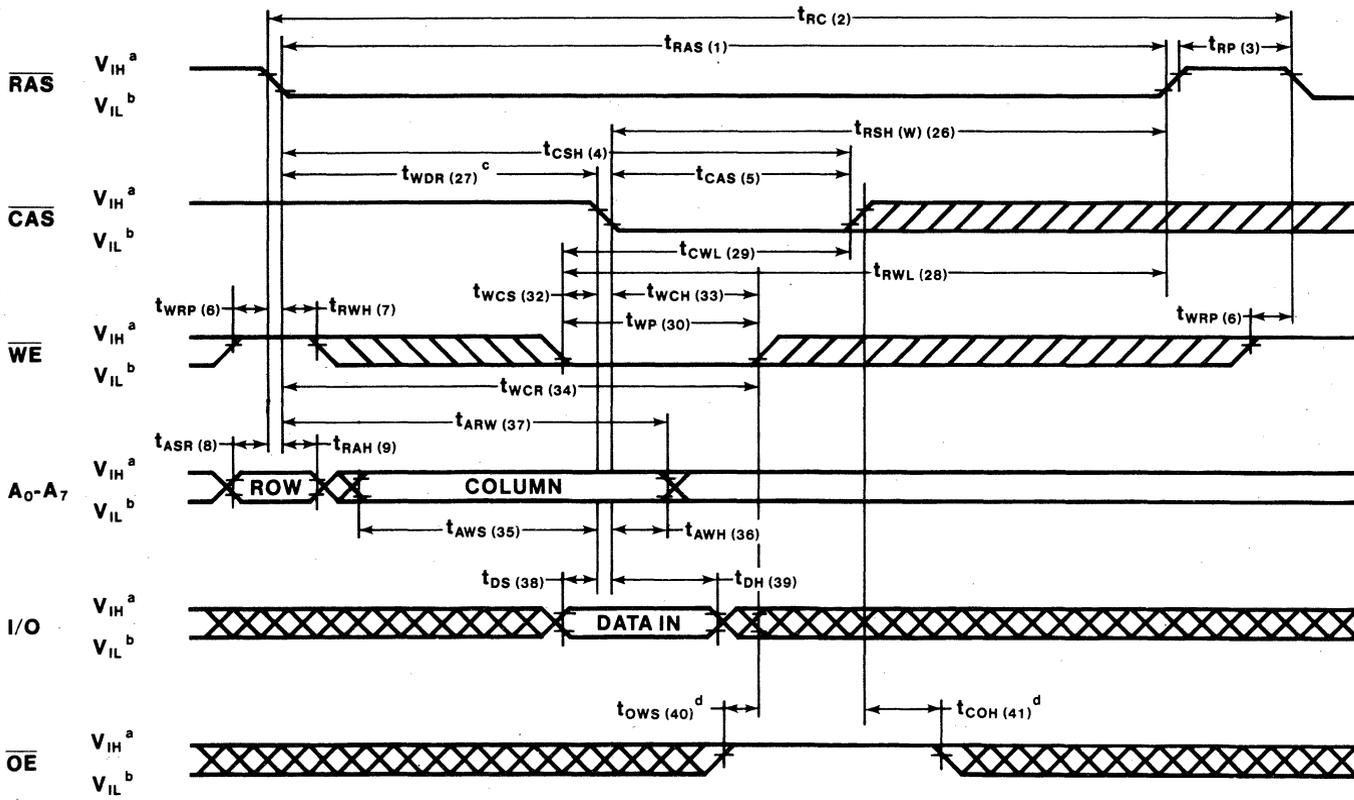
12. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{OWD} are specified as reference points only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is a $\overline{\text{CAS}}$ controlled write cycle and the data out pin will remain in high impedance for the duration of $\overline{\text{WE}}$ low. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{OWD}} \geq t_{\text{OWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition is of data out indeterminate.

WAVEFORMS READ CYCLE



- NOTE:**
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - t_{LZ} is referenced to the later of \overline{RAS} , \overline{CAS} , and \overline{OE} low transition.
 - t_{HZ} and t_{OH} are referenced to the earlier of \overline{CAS} or \overline{OE} high transition.
 - Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 - Either t_{RCH} or t_{RRH} must be satisfied.
 - If $t_{ARH} \geq t_{ARR}$ (min), then data from the last address will be latched on D_{OUT} by a \overline{RAS} high transition, until either a \overline{CAS} or \overline{OE} high transition releases the data.

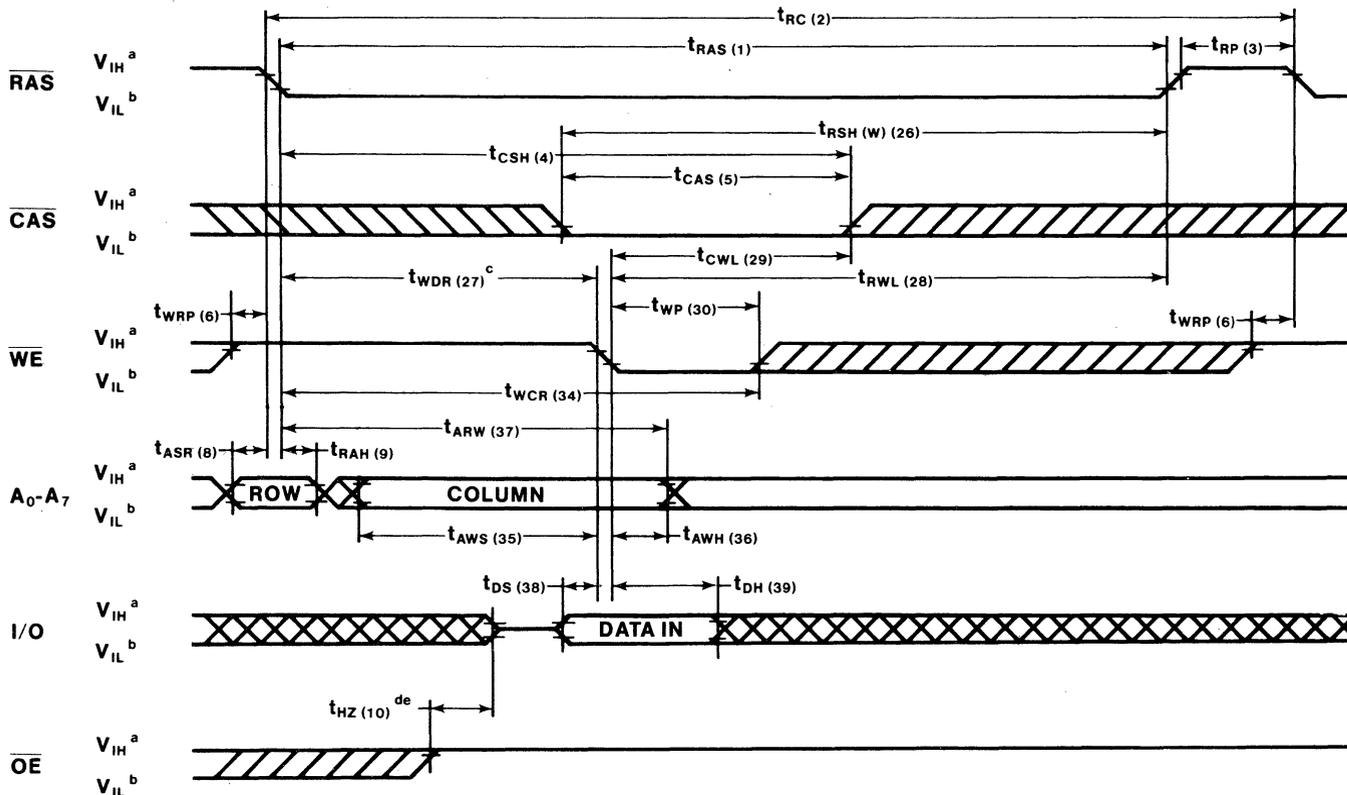
WAVEFORMS (Cont'd.) WRITE CYCLE (CAS Controlled) ^e



- NOTE:** a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 c. t_{WDR} is reference to the later of the CAS or WE low transition.
 d. If the low transition of WE occurs before or simultaneously with the low transition of CAS and the high transition of CAS or RAS occurs before the high transition of WE, then the outputs remain in a high impedance state (i.e., OE is a don't care).
 e. WE is low prior to or simultaneously with CAS low transition. CAS is high prior to RAS low transition.

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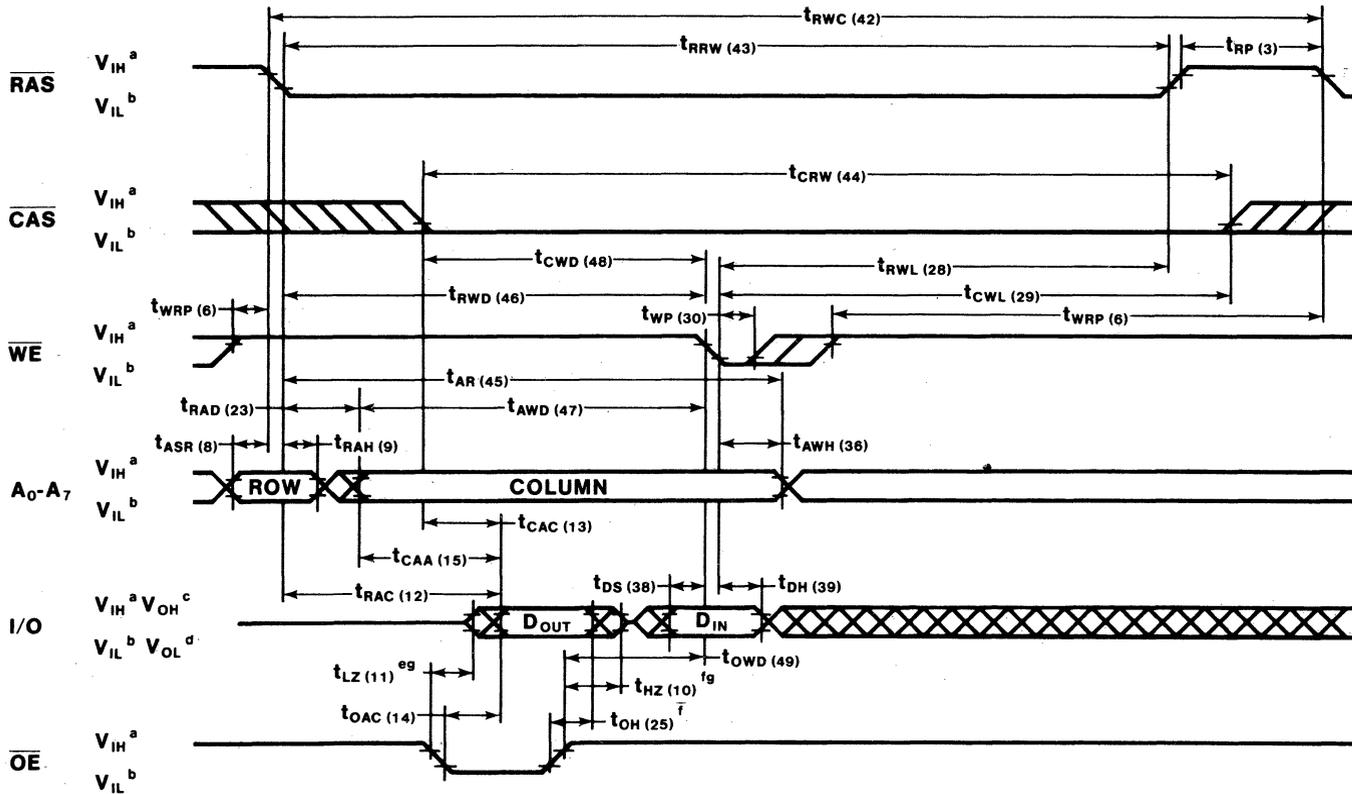
WAVEFORMS (Cont'd.) WRITE CYCLE (WE Controlled) ^f



- NOTE: a. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 b. t_{WDR} is reference to the later of the CAS or WE low transition.
 c. t_{HZ} is referenced to the earlier of the CAS or OE high transition or WE low transition.
 d. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 e. CAS is low prior to the WE low transition.

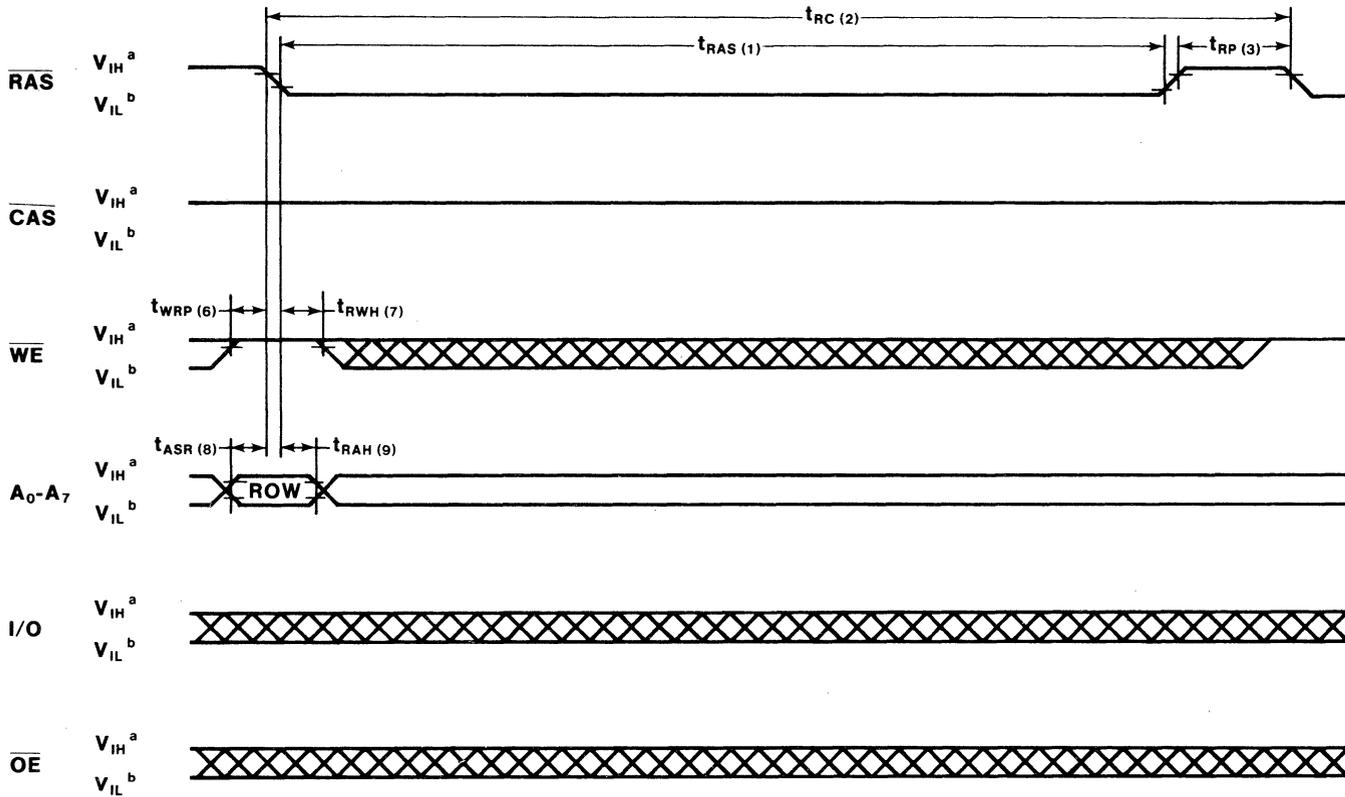
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WAVEFORMS (Cont'd.) READ/MODIFY/WRITE CYCLE



- NOTE:**
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 - V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT} .
 - t_{LZ} is referenced to the later of RAS, CAS, and OE low transition.
 - t_{HZ} and t_{OH} are referenced to the earlier of the CAS or OE high transition.
 - Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

**WAVEFORMS (Cont'd.)
RAS-ONLY REFRESH CYCLE**



NOTE: a., b. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.

C1612

FUNCTIONAL DESCRIPTION

The 51C259L is a CHMOS dynamic RAM optimized for low power applications. The functionality is similar to a traditional dynamic RAM. The 51C259L reads and writes 4 bits of data at a time by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe ($\overline{\text{RAS}}$). The column address, however, is only latched during a write cycle by the later of either Column Address Strobe ($\overline{\text{CAS}}$) or Write Enable ($\overline{\text{WE}}$). During the read cycle, the column address is not latched and continuously flows through the internal input latches. Access time is primarily dependent upon a valid column address. $\overline{\text{CAS}}$ acts as chip select signal and can remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}$ operation. The column address must be held for a minimum time specified by t_{ARR} . $\overline{\text{CAS}}$ may either be held low or be pulsed similar to the traditional $\overline{\text{CAS}}$ operation. Data out is controlled by the Out Enable ($\overline{\text{OE}}$) and $\overline{\text{CAS}}$ which is discussed in the Data Out Operation.

For applications where $\overline{\text{CAS}}$ is held low, the data out becomes valid when t_{RAC} , t_{CAA} and t_{OAC} are all satisfied.

For applications where $\overline{\text{CAS}}$ is pulsed similar to the traditional $\overline{\text{CAS}}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. Data out becomes valid only when t_{RAC} , t_{CAA} , t_{OAC} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} , t_{OAC} , and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} , t_{OAC} , and t_{CAC} are all satisfied.

Write Cycle

A write cycle is performed by taking $\overline{\text{WE}}$ low

during a $\overline{\text{RAS}}$ operation. To simplify the system design, the column address is latched in by the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$. As in the read cycle, $\overline{\text{CAS}}$ may either be held low or be pulsed similar to the traditional $\overline{\text{CAS}}$ operation. For applications where $\overline{\text{CAS}}$ is held low, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$. For applications where $\overline{\text{CAS}}$ is pulsed similar to the traditional $\overline{\text{CAS}}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Consequently, the write cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending upon the later of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ low transition. In a $\overline{\text{CAS}}$ controlled write cycle (the leading edge of $\overline{\text{WE}}$ occurs prior to or coincident with the $\overline{\text{CAS}}$ low transition) the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ will maintain the I/O in the high impedance state; terminating with $\overline{\text{WE}}$ allows the output to go active, and the $\overline{\text{OE}}$ must be brought high to allow for inputs on the I/O.

The 51C259L incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write function has been initiated, the 51C259L internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{\text{RAS}}$ at least every 4 milliseconds. Any Read, Write, Read-ModifyWrite, or $\overline{\text{RAS}}$ -Only cycle will perform refresh.

Extended Refresh Cycle

The 51C259L extends the refresh cycle period to 32 milliseconds for $\overline{\text{RAS}}$ -Only refresh cycles. This feature reduces the total current consumption to a maximum of 230 micro Amperes, and typically 90 micro Amperes, for data retention. The low standby current can significantly extend battery life in battery

back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})(I_{Active}) + (t_{RI} - t_{RC})(I_{Standby})}{t_{RI}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{REF}/256$

Data Out Operation

The 51C259L Input/Output (I/O) is controlled by \overline{OE} , \overline{CAS} , \overline{WE} and \overline{RAS} . A \overline{RAS} low transition enables data to transfer into and from a selected row address. A \overline{RAS} high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a \overline{RAS} low transition, a \overline{CAS} low transition or a \overline{CAS} low level enables the internal I/O data path. A \overline{CAS} high transition or a \overline{CAS} high level disables the I/O data path and disables the output driver if the driver was enabled. A \overline{CAS} low transition while \overline{RAS} is high has no effect on the I/O data path, nor on the output driver. An \overline{OE} low transition or an \overline{OE} low level enables the output driver when the I/O data path is enabled. An \overline{OE} high transition or an \overline{OE} high level disables the output driver, but does not disable the data latch when it has been enabled. A \overline{WE} low level disables the output driver when a \overline{CAS} low level occurs. If the \overline{WE} low transition occurs after the \overline{CAS} low transition such that the output

driver is enabled prior to the \overline{WE} low transition, it is necessary to use \overline{OE} to disable the output driver prior to the \overline{WE} low transition to allow data in set-up time (t_{DS}). A \overline{WE} high transition passes control of the output drive to \overline{OE} .

Power On

An initial pause of 100 μ S is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a \overline{RAS} clock such as \overline{RAS} -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).

The V_{DD} current (I_{DD}) requirement of the 51C259L during power on is dependent upon the input levels of \overline{RAS} and \overline{CAS} . If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that \overline{RAS} and \overline{CAS} track with V_{DD} or be held at a valid V_{IH} during power on.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*.



51C259HL

HIGH PERFORMANCE LOW POWER STATIC COLUMN 64K × 4 CHMOS DYNAMIC RAM

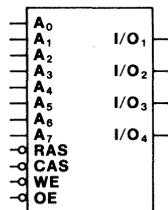
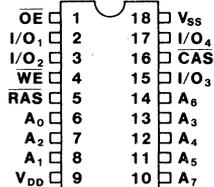
	51C259HL-15	51C259HL-20
Maximum Access Time (ns)	150	200
Maximum Column Address Access Time (ns)	70	90
Maximum CHMOS Standby Current (mA)	0.1	0.1

- **Static Column Mode Operation**
 - Continuous data rate over 12 MHz
 - Random access from address within row
 - $t_{CAC} = 30, 35 \text{ ns}$
 - $t_{OAC} = 25, 30 \text{ ns}$
- **Low Power Data Retention**
 - Standby current, CHMOS - 100 μA (max.)
 - Refresh period, $\overline{\text{RAS}}$ -Only - 32 ms (max.)
 - Data Retention Current - 230 μA (max.)
- **TTL And HCT Compatible**
- **High Reliability Plastic - 18 Pin DIP**
- **Low Input/Output Capacitance**

The Intel® 51C259HL is a high speed 65,536 × 4 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C259HL offers features not provided by an NMOS dynamic RAM: Static Column Mode for high data bandwidth, fast usable speed, and CHMOS standby current and extended $\overline{\text{RAS}}$ -Only refresh for low standby power. All inputs and outputs are compatible to both TTL and HCT logic families while the input and output capacitances are significantly lowered to allow increased system performance.

Static Column Mode operation allows random or sequential access of all 256 bits within a row simply by changing the column address. Because column address access time is as fast as 70 ns, a continuous data rate of over 12 million 4 bit nibbles per second can be achieved. The 51C259HL offers high performance while relaxing many critical system timing requirements for fast usable speed. These features make the 51C259HL ideally suited for graphics, digital signal processing, and high performance systems.

The 51C259HL offers a maximum standby current of 100 μA when $\overline{\text{RAS}} \geq V_{DD} - 0.5\text{V}$. During standby (i.e. refresh only cycles), the refresh period can be extended to 32 ms to reduce the total current required to retain data to less than 230 μA (max.). The 51C259HL combines this low power with high density for portable and battery backup applications.

LOGIC SYMBOL**PIN CONFIGURATION****PIN NAMES**

$\overline{\text{RAS}}$	ROW ADDRESS STROBE
$\overline{\text{CAS}}$	COLUMN ADDRESS STROBE
$\overline{\text{WE}}$	WRITE ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
A_0 - A_7	ADDRESS INPUTS
I/O_1 - I/O_4	DATA IN/DATA OUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

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ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature	
Under Bias	−10°C to +80°C
Storage	
Temperature	Plastic −55°C to +125°C
Voltage on Any Pin except V _{DD} and D _{OUT}	
Relative to V _{SS}	−2.0V to 7.5V
Voltage on V _{DD}	
Relative to V _{SS}	−1.0V to 7.5V
Voltage on D _{OUT}	
Relative to V _{SS}	−2.0V to V _{DD} + 1V

Data Out Current	50 ma
Power Dissipation	1.0W

†COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS¹

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	51C259HL			Unit	Test Conditions	Notes
		Min.	Typ. ²	Max.			
I _{DD1}	V _{DD} Supply Current, Operating			65	mA	t _{RC} = t _{RC} (min), for -15 specification	3, 4
				50	mA	t _{RC} = t _{RC} (min), for -20 specification	
I _{DD2}	V _{DD} Supply Current, TTL Standby			4	mA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , all other inputs and outputs ≥ V _{SS}	
I _{DD3}	V _{DD} Supply Current, RAS-Only Refresh			65	mA	t _{RC} = t _{RC} (min), for -15 specification	4
				50	mA	t _{RC} = t _{RC} (min), for -20 specification	
I _{DD4}	V _{DD} Supply Current, Static Column Mode			65	mA	Minimum cycle for -15 specification	3, 4
				50	mA	Minimum cycle for -20 specification	
I _{DD5}	V _{DD} Supply Current, Standby, Output Enabled			6	mA	$\overline{\text{RAS}}$ at V _{IH} , $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ at V _{IL} , all other inputs and outputs ≥ V _{SS}	3
I _{DD6}	V _{DD} Supply Current, CMOS Standby		0.01	0.1	mA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ ≥ V _{DD} - 0.5V, all other inputs and output ≥ V _{SS}	
I _L	Input Load Current (any pin)			1	μA	V _{IN} = V _{SS} to V _{DD}	
I _{LO}	Output Leakage Current, High Impedance State			5	μA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ at V _{IH} , D _{OUT} = V _{SS} to V _{DD}	
V _{IL}	Input Low Voltage (all inputs)	−0.3		0.8	V		5
V _{IH}	Input High Voltage (all inputs)	2.4		V _{DD} + 1	V		5
V _{OL}	Output Low Voltage (all outputs)			0.4	V	I _{OL} = 4.2 mA	6
				0.1	V	I _{OL} = 100 μA	
V _{OH}	Output High Voltage (all outputs)	2.4			V	I _{OH} = -5 mA	6
		V _{DD} - 0.1			V	I _{OH} = -100 μA	

- NOTES:**
- All voltages referenced to V_{SS}.
 - Typical values are at T_A = 25°C and V_{DD} = +5V.
 - I_{DD} is dependent upon output loading when the device is selected. Specified I_{DD(max)} is measured with the output open.
 - I_{DD} is dependent upon the number of address transitions. Specified I_{DD(max)} is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Static Column Mode.
 - Specified V_{IL(min)} is steady state operation. During transitions, V_{IL} may undershoot to -1.0 V for periods not to exceed 20 ns. All A.C. parameters are measured with V_{IL(min)} ≥ V_{SS} and V_{IH(max)} ≤ V_{DD}.
 - Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured as noted in the A.C. Characteristics section.

CAPACITANCE†

$T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

†NOTE:

Capacitance is measured at worst case voltage levels with a programmable Hewlett Packard capacitance meter.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	5	pF
C_{IN2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	4	5	pF
$C_{I/O}$	Data In/Out	4	6	pF

A.C. CHARACTERISTICS^{1, 2, 3}

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Read, Write and Refresh Cycles

No.	JEDEC Symbol	Symbol	Parameter	51C259HL-15		51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
1	tRL1RH1	tRAS	$\overline{\text{RAS}}$ Pulse Width	150	75000	200	75000	ns	
2	tRL2RL2	tRC	Random Read or Write Cycle Time	245		315		ns	
3	tRH2RL2	tRP	$\overline{\text{RAS}}$ Precharge Time	85		105		ns	
4	tRL1CH1	tCSH*	$\overline{\text{CAS}}$ Hold Time	150		200		ns	
5	tCL1CH1	tCAS*	$\overline{\text{CAS}}$ Pulse Width	30		35		ns	
6	tWH2RL2	tWRP	Write to $\overline{\text{RAS}}$ Precharge Time	10		10		ns	
7	tRL1WL2	tRWH	$\overline{\text{RAS}}$ to Write Hold Time	20		25		ns	
8	tAVRL2	tASR	Row Address Set-up Time	0		0		ns	
9	tRL1AX	tRAH	Row Address Hold Time	20		25		ns	
10	tCH2QZ	tHZ	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to Output High Impedance		25		30	ns	4, 5
11	tCL2QX	tLZ	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to Output Low Impedance	0		0		ns	4, 5
	tRVRV	tREF1	Time Between Refresh		4		4	ms	6
	tRVRV	tREF2	Time Between Refresh ($\overline{\text{RAS}}$ -Only)		32		32	ms	6
	tT	tT	Transition Time (Rise and Fall)	3	25	3	25	ns	7

NOTES: * This parameter not applicable if operated with $\overline{\text{CAS}}$ grounded.

- All voltages referenced to V_{SS} .
- An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).
- A.C. Characteristics assume $t_T = 5\text{ ns}$. All A.C. parameters are measured with $V_{OL} = 0.8\text{V}$ at $I_{OL} = 2.2\text{ mA}$, $V_{OH} = 2.4\text{V}$ at $I_{OH} = -2.0\text{ mA}$ with a 50 pF load, $V_{IL}(\text{min}) \geq V_{SS}$ and $V_{IH}(\text{max}) \leq V_{DD}$.
- Assumes three state test load (5 pF and a 380 Ohm Thevenin equivalent).
- At any given temperature and voltage combination, $t_{HZ}(\text{max}) \leq t_{LZ}(\text{min})$ from device to device.
- The 51C259HL extends the refresh period to 32 ms during $\overline{\text{RAS}}$ -Only refresh periods.
- t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

A.C. Characteristics (Continued)

Read Cycle

No.	JEDEC Symbol	Symbol	Parameter	51C259HL-15		51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
12	tRL1QV	tRAC	Access Time From $\overline{\text{RAS}}$		150		200	ns	8
13	tCL1QV	tCAC	Access Time From $\overline{\text{CAS}}$		30		35	ns	
14	tGL1QV	tOAC	Access Time From $\overline{\text{OE}}$		25		30	ns	
15	tAVQV	tCAA	Access Time From Column Address		70		90	ns	
16	tCL1RH1	tRSH(R)*	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	10		10		ns	
17	tWH2CL2	tRCS*	Read Command Set-up Time	0		0		ns	
18	tAVRH1	tCAR	Column Address to $\overline{\text{RAS}}$ Set-up Time	70		90		ns	
19	tRL1AX	tARR	Column Address Hold Time From $\overline{\text{RAS}}$ (Read)	140		190		ns	
20	tCH2WX	tRCH*	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	5		5		ns	
21	tRH2WX	tRRH	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	10		10		ns	
22	tRH2AX	tARH	Column Address Hold Time to $\overline{\text{RAS}}$	0		0		ns	
23	tRL1AV	tRAD	$\overline{\text{RAS}}$ to Column Address Delay Time	25	80	30	110	ns	9
24	tAXQX	tOHA	Output Hold Time From Address Change	10		10		ns	
25	tGH1QX	tOH	Output Hold Time From $\overline{\text{OE}}$ or $\overline{\text{CAS}}$	0		0		ns	

Write Cycle

26	tCL1RH1	tRSH(W)	$\overline{\text{RAS}}$ Hold Time (Write Cycle)	35		40		ns	
27	tRL1WL2	tWDR	$\overline{\text{RAS}}$ to Write Command Lead Time	30	115	35	160	ns	
28	tWL1RH1	tRWL	Write Command to $\overline{\text{RAS}}$ Lead Time	30		35		ns	
29	tWL1CH1	tCWL*	Write Command to $\overline{\text{CAS}}$ Lead Time	30		35		ns	
30	tWL1WH1	tWP	Write Command Pulse Width	10		15		ns	
31	tWH2WL2	tWCP	Write Command Precharge Time	10		15		ns	
32	tWL1CL2	tWCS*	Write Command Set-up Time	0		0		ns	10
33	tCL1WH1	tWCH*	Write Command Hold Time	30		35		ns	
34	tRL1WH1	tWCR	Write Command Hold Time From $\overline{\text{RAS}}$	100		110		ns	
35	tAVWL2	tAWS	Column Address to Write Command Set-up Time	5		5		ns	
36	tWL1AX	tAWH	Column Address to Write Command Hold Time	25		30		ns	

NOTES: * This parameter not applicable if operated with $\overline{\text{CAS}}$ grounded.

8. Assumes that $t_{\text{RAD}} \leq t_{\text{RAD(max)}}$ if $t_{\text{RAD}} > t_{\text{RAD(max)}}$, then t_{RAC} will increase by the amount that t_{RAD} exceeds $t_{\text{RAD(max)}}$.

9. t_{RAD} is specified for reference only.

10. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{OWD} are specified as reference points only. If $t_{\text{WCS}} \geq t_{\text{WCS(min)}}$, the cycle is a $\overline{\text{CAS}}$ controlled write cycle and the data out pin will remain in high impedance for the duration of $\overline{\text{WE}}$ low. If $t_{\text{CWD}} \geq t_{\text{CWD(min)}}$ and $t_{\text{RWD}} \geq t_{\text{RWD(min)}}$ and $t_{\text{OWD}} \geq t_{\text{OWD(min)}}$ and $t_{\text{AWD}} \geq t_{\text{AWD(min)}}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.

A.C. Characteristics (Continued)

Write Cycle (Continued)

No.	JEDEC Symbol	Symbol	Parameter	51C259HL-15		51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.		
37	tRL1AX	tARW	Column Address Hold Time From \overline{RAS} (Write)	60		70		ns	
38	tDVWL2	tDS	Data-In Set-up Time	5		5		ns	
39	tWL1DX	tdH	Data-In Hold Time	25		30		ns	
40	tGH2WH1	tOWS	\overline{OE} Set-up Time From End of Write	15		20		ns	
41	tCH2GL2	tCOH	\overline{OE} Hold Time From \overline{CAS}	20		25		ns	

Read-Modify-Write Cycle ¹¹

42	tRL2RL2	trWC	Read-Modify-Write (RMW) Cycle Time	310		390		ns	
43	tRL1RH1	tRRW	\overline{RAS} Pulse Width (RMW)	215	75000	275	75000	ns	
44	tCL1CH1	tCRW	\overline{CAS} Pulse Width (RMW)	95		110		ns	
45	tRL1AX	tAR	Column Address Hold Time From \overline{RAS} (RMW)	205		265		ns	
46	tRL1WL2	trWD	\overline{RAS} to \overline{WE} Delay	180		235		ns	12
47	tAVWL2	tAWD	Column Address to \overline{WE} Delay	100		115		ns	12
48	tCL1WL2	tcWD*	\overline{CAS} to \overline{WE} Delay	60		70		ns	12
49	tGH2WL2	tOWD	\overline{OE} to \overline{WE} Delay	30		35		ns	12

Static Column Mode ¹³

50	tWL2WL2	tSWC	Static Column Write Cycle Time	50		55		ns	
51	tWH2QV	tWPA	Write Precharge Access Time		30		35	ns	14
52	tWL1QV	tWRA	Write-Read Access Time		120		135	ns	14
53	tWL1GL2	tWOH	Write to \overline{OE} Hold Time	30		35		ns	
54	tRL1WL1	tSWH	\overline{RAS} to Write Command Hold Time	150		200		ns	

NOTES: * This parameter not applicable if operated with \overline{CAS} grounded.

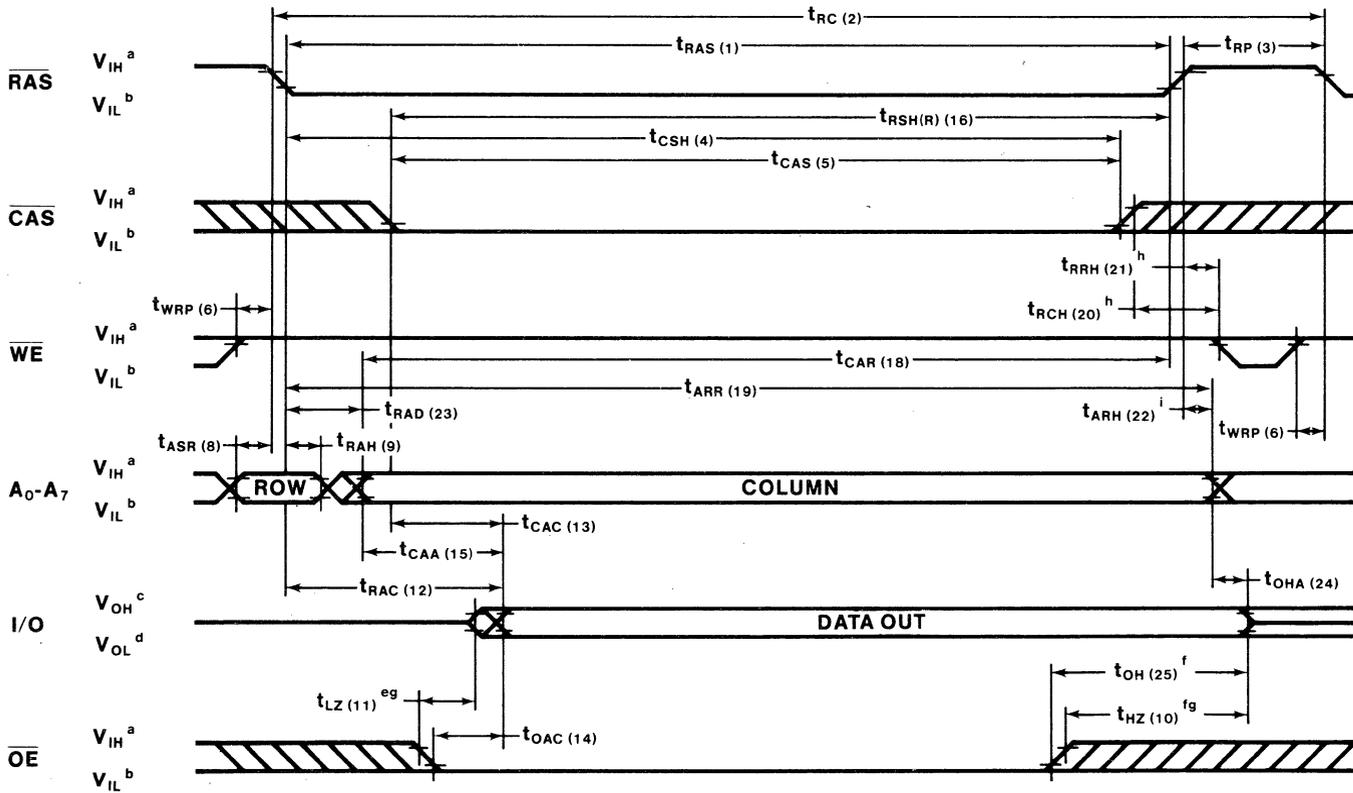
11. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.

12. twcs, trwd, tcwd, tawd and towd are specified as reference points only. If twcs \geq twcs(min), the cycle is a \overline{CAS} controlled write cycle and the data out pin will remain in high impedance for the duration of \overline{WE} low. If tcwd \geq tcwd(min) and trwd \geq trwd(min) and towd \geq towd(min) and tawd \geq tawd(min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition is of data out indeterminate.

13. All previously specified A.C. characteristics are applicable.

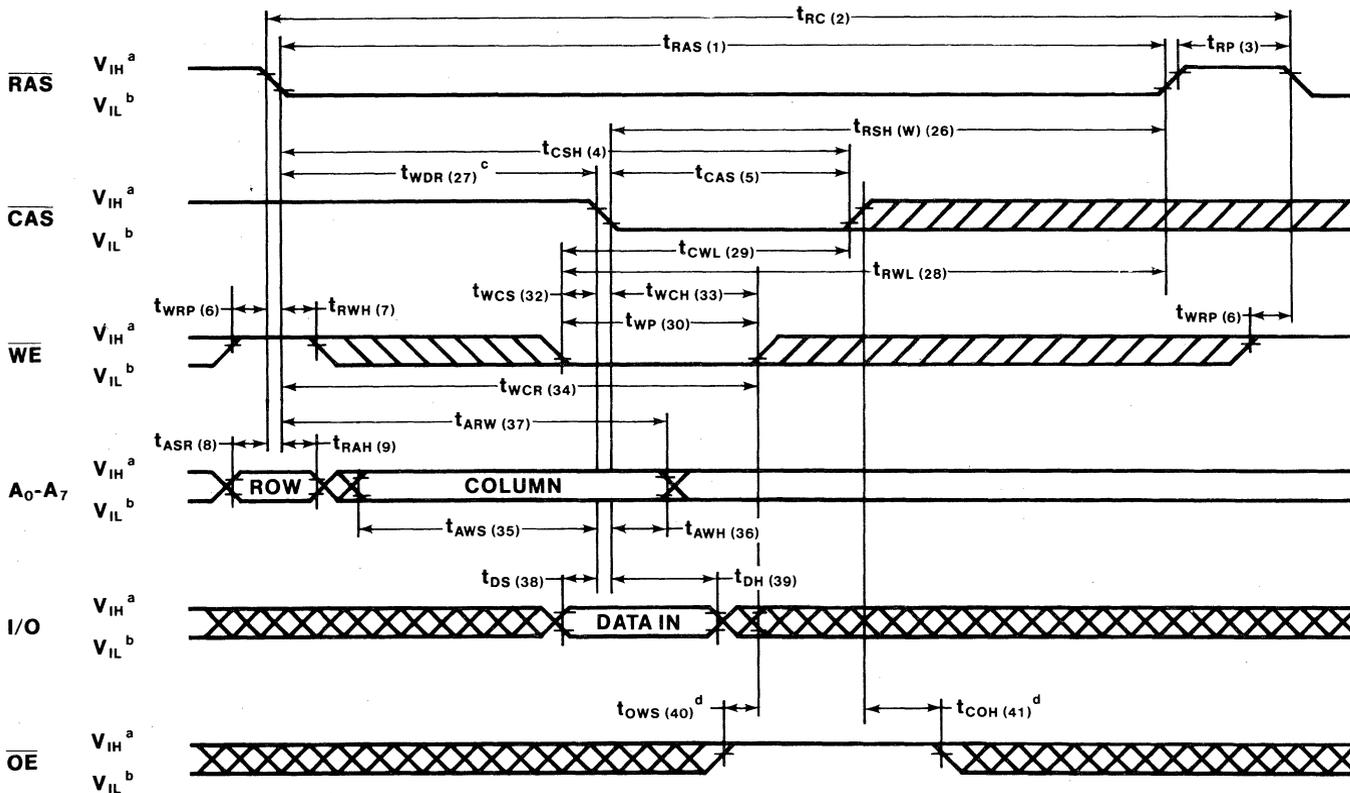
14. Access time from a write command to a read command is determined by the longer of tCAA or tWPA or tWRA.

WAVEFORMS READ CYCLE



- NOTE:**
- $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.
 - $V_{OH}(\text{min})$ and $V_{OL}(\text{max})$ are reference levels for measuring timing of D_{OUT} .
 - t_{LZ} is referenced to the later of RAS, CAS, and OE low transition.
 - t_{HZ} and t_{OH} are referenced to the earlier of CAS or OE high transition.
 - Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 - Either t_{RCH} or t_{RRH} must be satisfied.
 - If $t_{ARH} \geq t_{ARH}(\text{min})$, then data from the last address will be latched on D_{OUT} by a RAS high transition, until either a CAS or OE high transition releases the data.

WAVEFORMS (Cont'd.) WRITE CYCLE (CAS Controlled) ^e



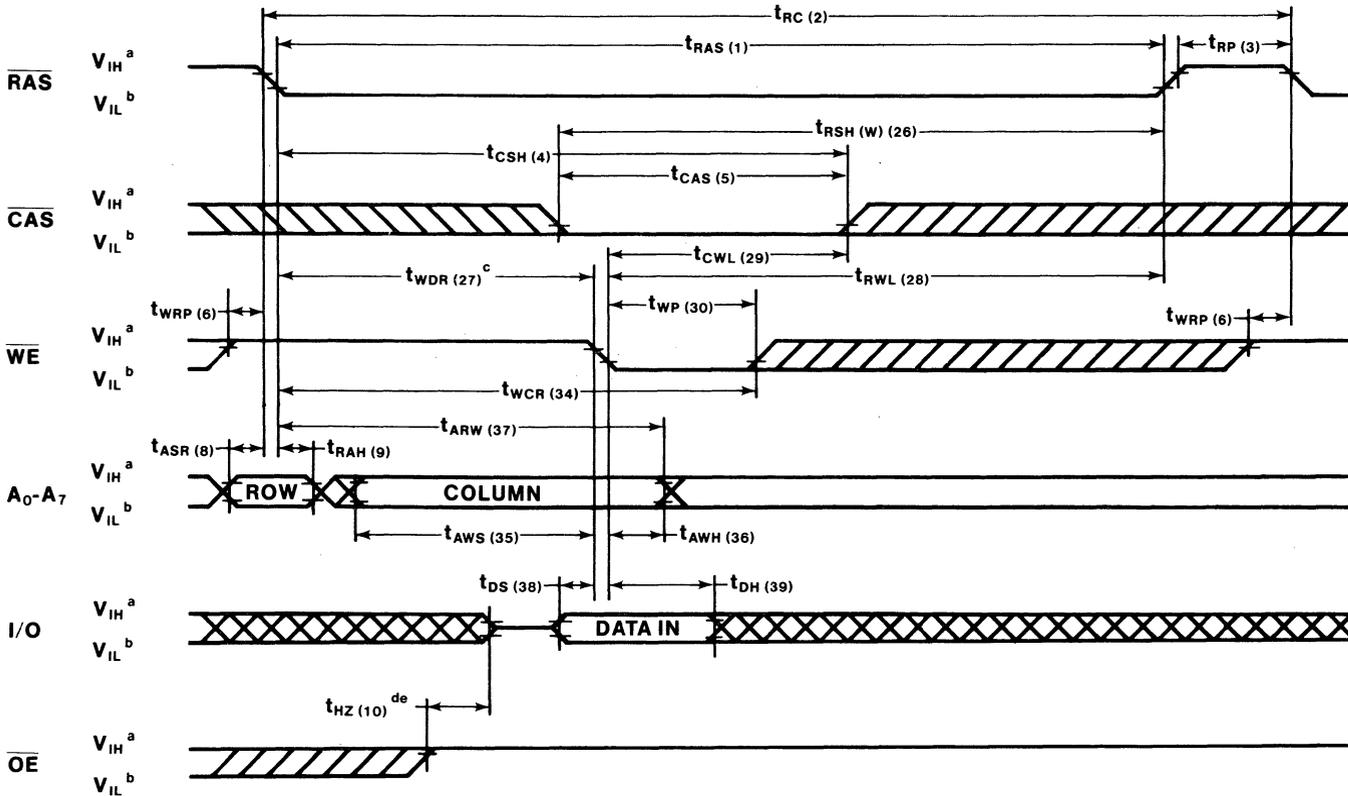
NOTE: a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c. t_{WDR} is reference to the later of the CAS or WE low transition.

d. If the low transition of WE occurs before or simultaneously with the low transition of CAS and the high transition of CAS or RAS occurs before the high transition of WE, then the outputs remain in a high impedance state (i.e., OE is a don't care).

e. WE is low prior to or simultaneously with CAS low transition. CAS is high prior to RAS low transition.

WAVEFORMS (Cont'd.) WRITE CYCLE (WE Controlled) ^f

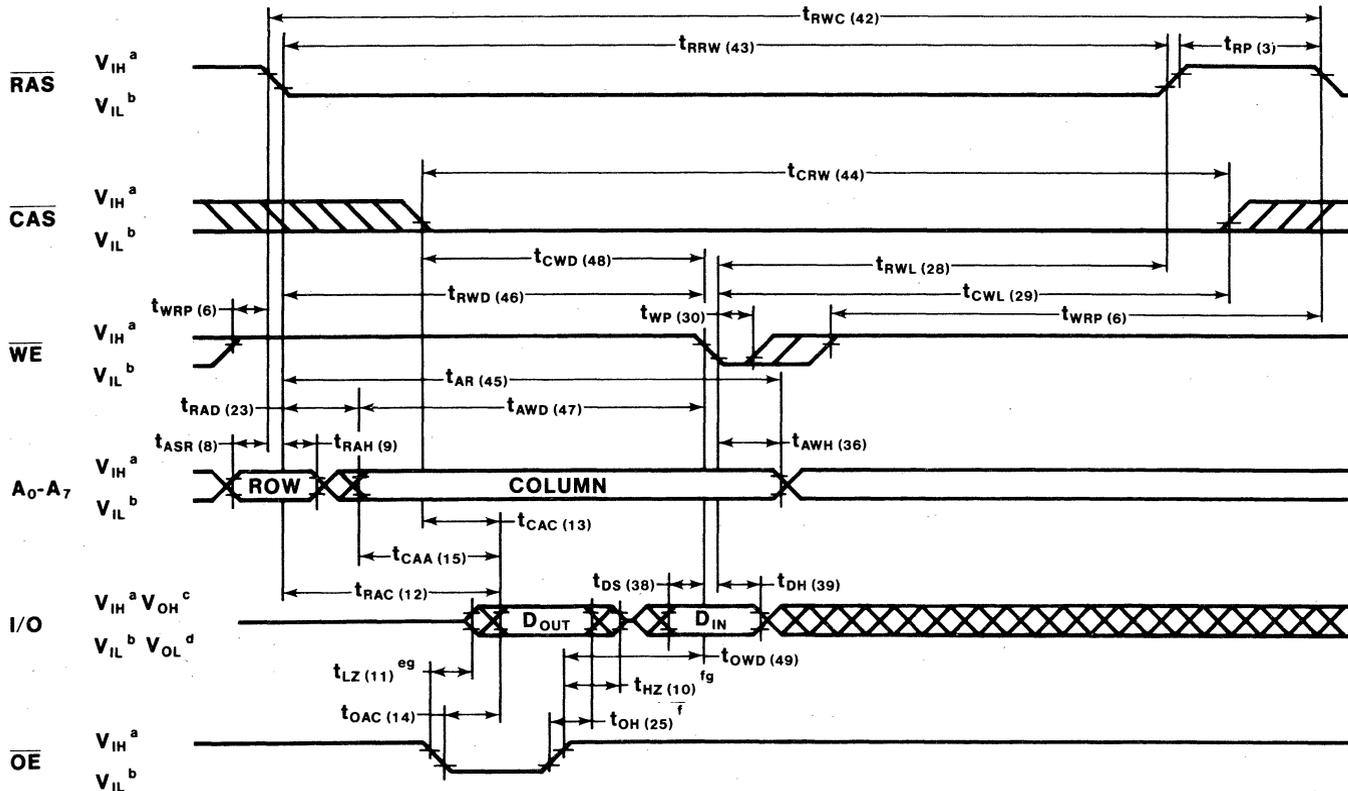


- NOTE: a. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 b. t_{WDR} is reference to the later of the CAS or WE low transition.
 c. t_{HZ} is referenced to the earlier of the CAS or OE high transition or WE low transition.
 d. Transition is measured + 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 e. CAS is low prior to the WE low transition.

2-139

C1610

WAVEFORMS (Cont'd.) READ/MODIFY/WRITE CYCLE



2-140

NOTE: a. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals.
 c. $V_{OH}(\min)$ and $V_{OL}(\max)$ are reference levels for measuring timing of D_{OUT} .
 d. t_{LZ} is referenced to the later of RAS, CAS, and OE low transition.
 e. t_{HZ} and t_{OH} are referenced to the earlier of the CAS or OE high transition.
 f. t_{HZ} and t_{OH} are referenced to the earlier of the CAS or OE high transition.
 g. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

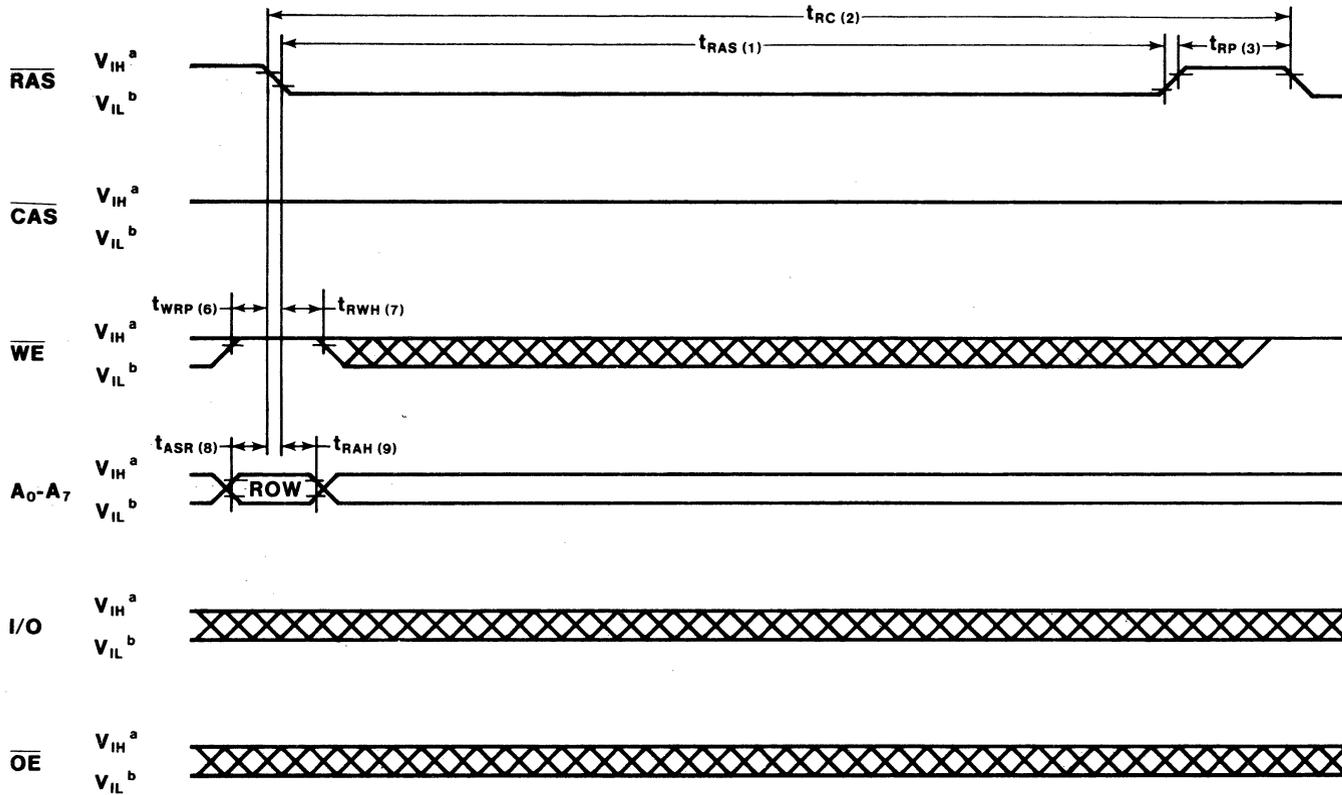
C1611



51C259HL

PRELIMINARY

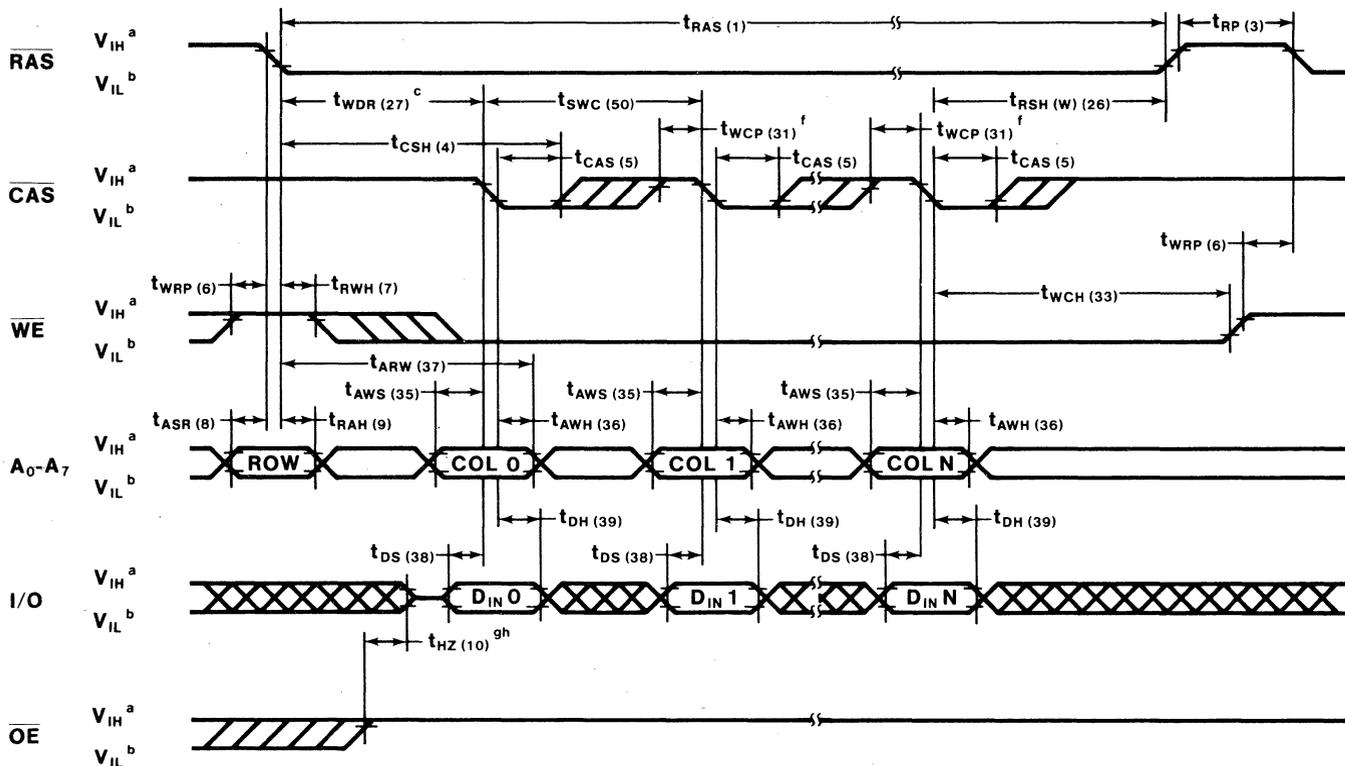
WAVEFORMS (Cont'd.) RAS-ONLY REFRESH CYCLE



NOTE: a., b. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals.

C1612

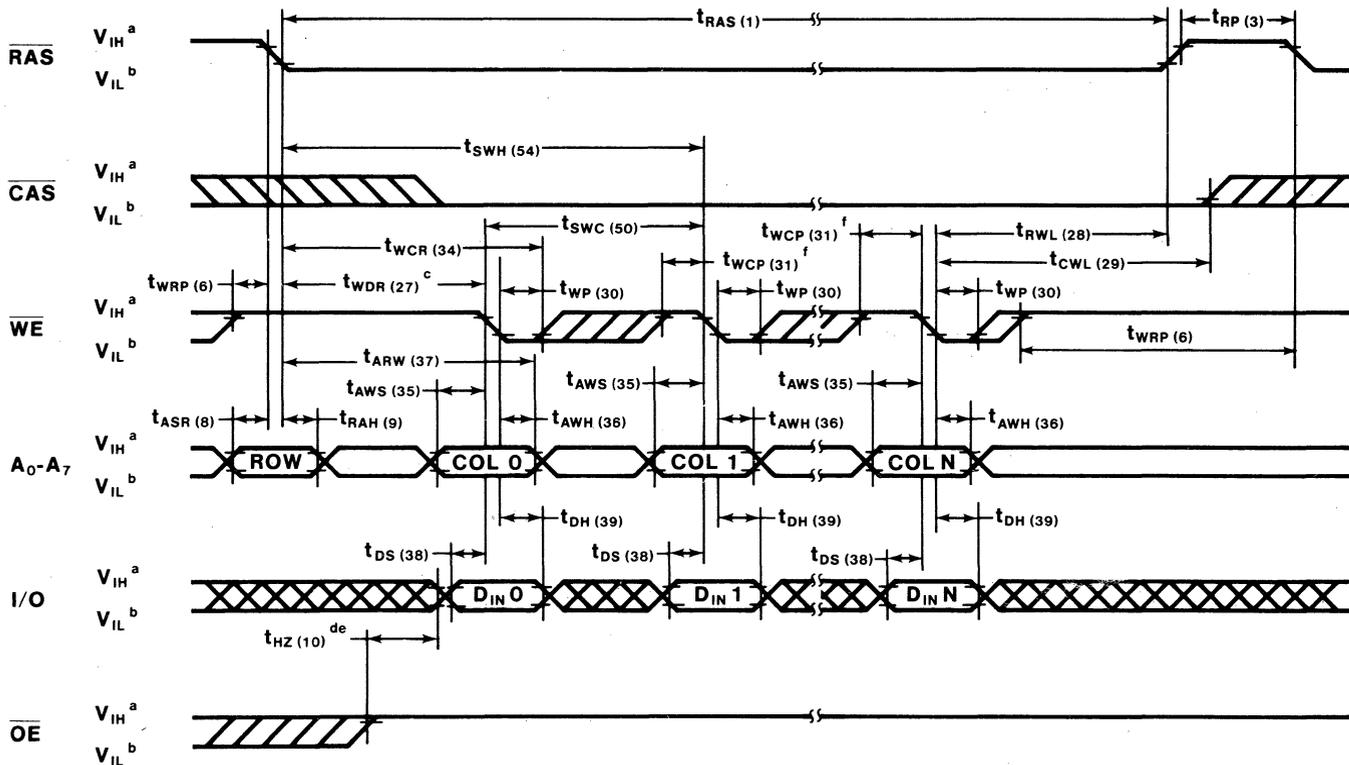
WAVEFORMS (Cont'd.) STATIC COLUMN MODE WRITE CYCLE (CAS Controlled) ^g



- NOTE:** a. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals.
 b. t_{WDR} is reference to the later of the CAS or WE low transition.
 c. t_{WDR} is reference to the later of the CAS or WE low transition.
 d. t_{HZ} is referenced to the earlier of the CAS or OE high transition or WE low transition.
 e. Transition is measured + 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 f. t_{WCP} is measured from the earlier of CAS or WE high transition to the later of CAS or WE low transition.
 g. WE is low prior to or simultaneously with a CAS low transition. CAS is high prior to a RAS low transition.

C1614

WAVEFORMS (Cont'd.) STATIC COLUMN MODE WRITE CYCLE (\overline{WE} Controlled) ⁹



- NOTE: a. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 b. t_{WDR} is reference to the later of the CAS or \overline{WE} low transition.
 c. t_{WDR} is reference to the later of the CAS or \overline{WE} low transition.
 d. t_{HZ} is referenced to the earlier of the RAS or CAS or \overline{OE} high transition.
 e. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
 f. t_{WCP} is measured from the earlier of CAS or \overline{WE} high transition to the later of CAS or \overline{WE} low transition.
 g. CAS is low prior to a \overline{WE} low transition.

FUNCTIONAL DESCRIPTION

The 51C259HL is a CMOS dynamic RAM optimized for the high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The 51C259HL reads and writes 4 bits of data at a time by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe (\overline{RAS}). The column address, however, is only latched during a write cycle by the later of either Column Address Strobe (\overline{CAS}) or Write Enable (\overline{WE}). During the read cycle, the column address is not latched and continuously flows through the internal input latches. Access time is primarily dependent upon a valid column address. \overline{CAS} acts as chip select signal and can remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing \overline{RAS} low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} , has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable (\overline{WE}) signal high during the \overline{RAS} operation. The column address must be held for a minimum time specified by t_{ARR} . \overline{CAS} may either be held low or be pulsed similar to the traditional \overline{CAS} operation. Data out is controlled by the Out Enable (\overline{OE}) and \overline{CAS} which is discussed in the Data Out Operation.

For applications where \overline{CAS} is held low, the data out becomes valid when t_{RAC} , t_{CAA} and t_{OAC} are all satisfied.

For applications where \overline{CAS} is pulsed similar to the traditional \overline{CAS} operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. Data out becomes valid only when t_{RAC} , t_{CAA} , t_{OAC} , and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC} , t_{CAA} , t_{OAC} , and t_{CAC} . For example, the access time is limited by t_{CAA} when t_{RAC} , t_{OAC} , and t_{CAC} are all satisfied.

Write Cycle

A write cycle is performed by taking \overline{WE} low during a \overline{RAS} operation. To simplify the system design, the column address is latched in by the later of \overline{WE} or \overline{CAS} . As in the read cycle, \overline{CAS} may either be held low or be pulsed similar to the traditional \overline{CAS} operation. For applications where \overline{CAS} is held low, the input data must be valid at or before the falling edge of \overline{WE} . For applications where \overline{CAS} is pulsed similar to the traditional \overline{CAS} operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Consequently, the write cycle can be \overline{WE} controlled or \overline{CAS} controlled depending upon the later of \overline{WE} or \overline{CAS} low transition. In a \overline{CAS} controlled write cycle (the leading edge of \overline{WE} occurs prior to or coincident with the \overline{CAS} low transition) the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with \overline{CAS} will maintain the I/O in the high impedance state; terminating with \overline{WE} allows the output to go active, and the \overline{OE} must be brought high to allow for inputs on the I/O.

The 51C259HL incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write function has been initiated, the 51C259HL internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with \overline{RAS} at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or \overline{RAS} -Only cycle will perform refresh.

Extended Refresh Cycle

The 51C259HL extends the refresh cycle period to 32 milliseconds for \overline{RAS} -Only refresh cycles. This feature reduces the total current

consumption to a maximum of 230 micro Amperes, and typically 90 micro Amperes, for data retention. The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{((t_{RC}) (I_{Active}) + (t_{RI} - t_{RC}) (I_{Standby}))}{t_{RI}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{REF}/256$

Static Column Mode Operation

Static column mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Read, write, and read-write-read cycles can be performed during static column mode operation. The row address is internally retained by maintaining \overline{RAS} active. Following the entry cycle into static column mode operation, the data is accessed simply by changing the column address. Because the column address buffer acts as a transparent or flow-through latch, access begins from a valid column address. Thus, the 51C259HL operates like a static RAM for multiple accesses within the same row. \overline{CAS} acts as a chip select. Intel's Application Note 172, *CHMOS DRAMS in Graphics Applications*, provides more details on static column mode operation.

Data Out Operation

The 51C259HL Input/Output (I/O) is controlled by \overline{OE} , \overline{CAS} , \overline{WE} and \overline{RAS} . A \overline{RAS} low transition enables data to transfer into and from a selected row address. A \overline{RAS} high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a \overline{RAS} low transition, a \overline{CAS} low transition or a \overline{CAS} low level enables the internal I/O data path. A \overline{CAS} high transition or a \overline{CAS} high level

disables the I/O data path and disables the output driver if the driver was enabled. A \overline{CAS} low transition while \overline{RAS} is high has no effect on the I/O data path, nor on the output driver. An \overline{OE} low transition or an \overline{OE} low level enables the output driver when the I/O data path is enabled. An \overline{OE} high transition or an \overline{OE} high level disables the output driver, but does not disable the data latch when it has been enabled. A \overline{WE} low level disables the output driver when a \overline{CAS} low level occurs. If the \overline{WE} low transition occurs after the \overline{CAS} low transition such that the output driver is enabled prior to the \overline{WE} low transition, it is necessary to use \overline{OE} to disable the output driver prior to the \overline{WE} low transition to allow data in set-up time (t_{DS}). A \overline{WE} high transition passes control of the output drive to \overline{OE} .

Power On

An initial pause of 100 μ S is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a \overline{RAS} clock such as \overline{RAS} -Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).

The V_{DD} current (I_{DD}) requirement of the 51C259HL during power on is dependent upon the input levels of \overline{RAS} and \overline{CAS} . If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that \overline{RAS} and \overline{CAS} track with V_{DD} or be held at a valid V_{IH} during power on.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS*, and A.P. #172, *CHMOS DRAMS in Graphics Applications*.

51C67 HIGH SPEED CHMOS 16,384 x 1 BIT STATIC RAM

	51C67-35
Max Access Time (ns)	35
Max Active Current (mA)	100
Max Standby Current (mA)	10

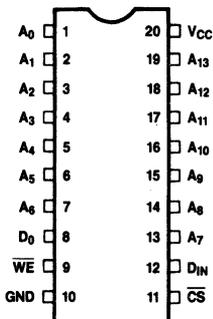
- Double Metal CHMOS III Technology
- Completely Static Memory—No Clock
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power Down
- 0.8–2.0V Output Timing Reference
- High Density 20-Pin Package
- Directly TTL Compatible—All Inputs and Output
- Separate Data Input and Output
- Three-State Output
- 2147H Upgrade

The Intel 51C67 is a 16,384-bit static random access memory organized as 16,384 words by 1 bit. This memory is fabricated using Intel's high performance double metal CHMOS III technology, with a full CHMOS 6T cell. This state of the art technology with HMOS III scaled transistors brings high performance to CMOS Static RAMs. The design of the 51C67 offers a 4× density improvement over the industry standard 2147H with compatible performance. The 51C67 offers the automatic power-down feature pioneered by the Intel 2147H.

\overline{CS} controls the power-down feature. In no more than a cycle time after \overline{CS} goes high (deselecting the 51C67), the part automatically reduces its power requirements and remains in this low power standby mode as long as \overline{CS} remains high. This device feature results in system power savings as great as 90% in larger systems where the majority of devices are deselected.

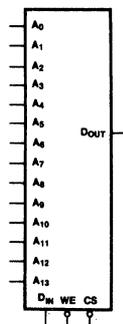
The 51C67 is placed in a 20-pin 300 mil package configured with the industry standard 16K x 1 pinout. It is directly TTL compatible in all respects: inputs, output; and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

Pin Configuration

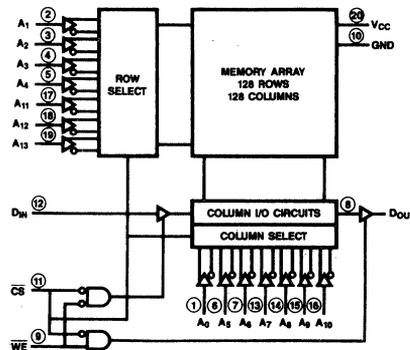


231094-2

Logic Symbol



231094-1



231094-3

Figure 1. 51C67 Block Diagram

Pin Names

A_0 – A_{13}	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output

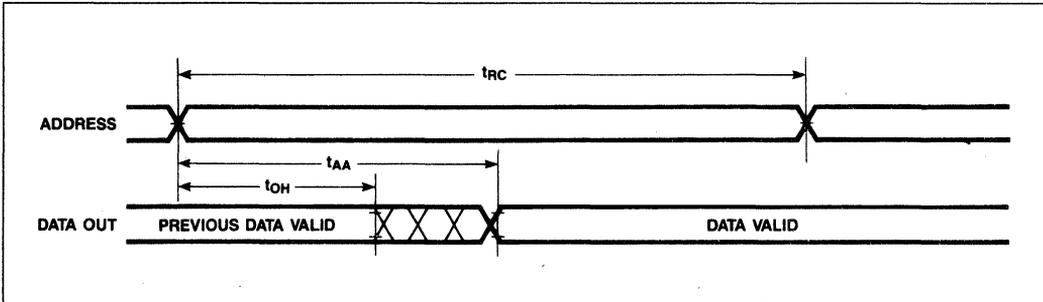
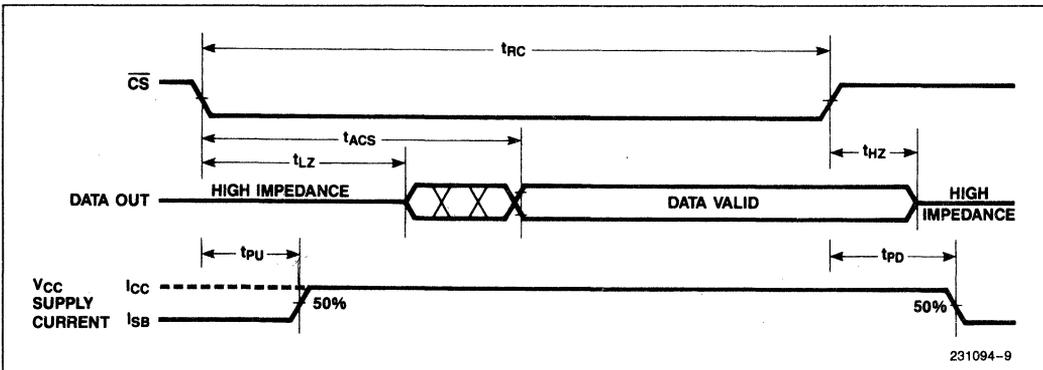
Truth Table

\overline{CS}	\overline{WE}	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

A. C. CHARACTERISTICS
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC} = +5 \pm 10\%$ Unless otherwise noted

READ CYCLE

Symbol	Parameter	Min	Max	Unit
$t_{RC}^{(1)}$	Read Cycle Time	35		ns
t_{AA}	Address Access Time		35	ns
$t_{ACS}^{(7)}$	Chip Select Access Time		35	ns
t_{OH}	Output Hold from Address Change	0		ns
$t_{LZ}^{(2,3)}$	Chip Selection to Output in Low Z	3		ns
$t_{HZ}^{(2,3)}$	Chip Deselection to Output in High Z	0	25	ns
t_{PU}	Chip Selection to Power Up Time	0		ns
t_{PD}	Chip Deselection to Power Down Time		35	ns

READ CYCLE NO. 1 (4, 5)

READ CYCLE NO. 2 (4,6,7)

NOTES ON READ OPERATION:

1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured at ± 500 mV from steady state voltage with specified loading in Figure 3.
4. \overline{WE} is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with \overline{CS} transition low.
7. Chip deselected for a finite time prior to selection. If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.

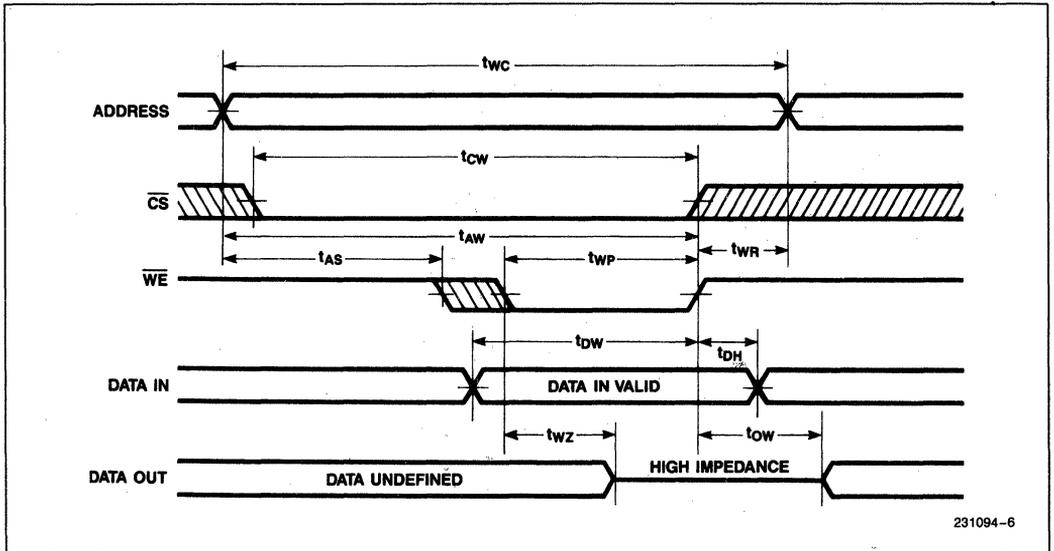
A. C. CHARACTERISTICS

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5 \pm 10\%$ unless otherwise noted

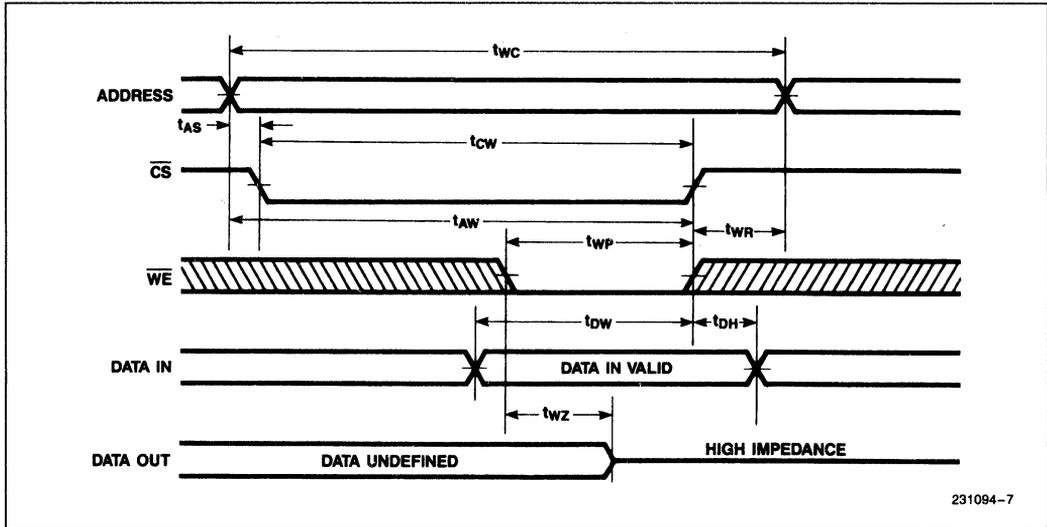
WRITE CYCLE

Symbol	Parameter	Min	Max	Unit
$t_{WC}^{(2)}$	Write Cycle Time	35		ns
t_{CW}	Chip Selection to End of Write	30		ns
t_{AW}	Address Valid to End of Write	30		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	20		ns
t_{WR}	Write Recovery Time	5		ns
t_{DW}	Data Valid to End of Write	15		ns
t_{DH}	Data Hold Time	3		ns
$t_{WZ}^{(3)}$	Write Enabled to Output in High Z	0	20	ns
$t_{OW}^{(3)}$	Output Active from End of Write	0		ns

WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)⁽⁴⁾



WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED)(4)



231094-7

NOTES ON WRITE OPERATION:

1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured = 500 mV from steady state voltage with specified loading in Figure 3.
4. \overline{CS} or \overline{WE} must be high during address transitions.

81C28 FAMILY

2048 x 8 Bit Ultra Low Power, High Integration Static RAM

	LOW POWER	STANDARD
	81C28L-200	81C28-200
Max Access Time	200 ns	200 ns
Max Active Current-CMOS Inputs	10 mA	10 mA
Max Standby Current-CMOS Inputs	50 μ A	100 μ A

- Integrated Address Latch
- Double Metal CHMOS III Technology
- Low Active and Microwatt Standby Power Allow Battery Operation/Backup
- Compatible with 80C51-BH, 80C31-BH, 80C49-BH for High Integration CMOS Systems
- Single +5V \pm 20% Supply
- High Reliability Plastic or CERDIP Package
- Common Data Input and Output with Three State Output Buffers

The Intel 81C28 is a 16,384 bit static random access memory organized as 2048 words by 8 bits using CHMOS III, an ultra low power CMOS technology. The 81C28 has been specially designed to eliminate the need of a latch to separate address and data in multiplexed address/data microprocessor and microcontroller applications. An OE pin is also provided for read cycles to eliminate the problem of Bus contention.

The address latch function allows for high integration systems where 2k bytes of external RAM are required. On the falling edge of the ALE input (ALE/ \overline{CS}) the address information is latched in. This pin also controls the power down feature. In less than a cycle time after ALE/ \overline{CS} goes high, disabling the 81C28, the part automatically reduces its power requirements and remains in this low power standby mode as long as ALE/ \overline{CS} remains high.

The 81C28 is assembled in a 24-pin 600 Mil dual-in-line plastic or CERDIP package, configured with the industry standard 2k x 8 pinout. It is directly compatible with TTL or CMOS in all respects—inputs, outputs and single power supply. The data is read out nondestructively and has the same polarity as the input data.

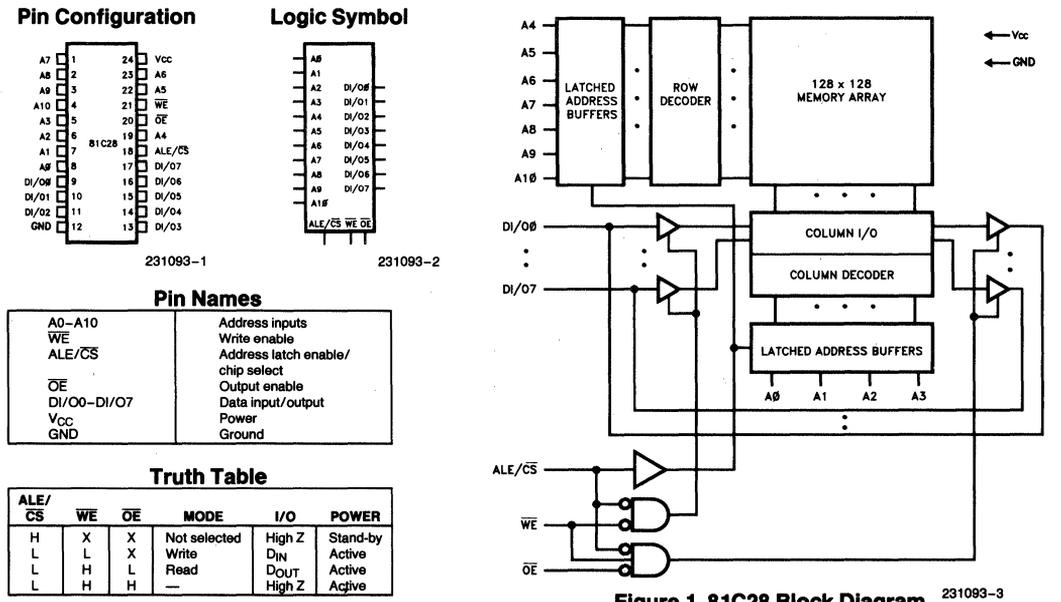


Figure 1. 81C28 Block Diagram 231093-3

A.C. Testing Conditions

Input pulse levels 0.4 to 2.4V
 Input rise and fall times 5 ns
 Input timing reference level 1.5V
 Output timing reference level 0.8 to 2.0V
 Output load see Figures 2, 3, 4

Capacitance^[1] $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	5	pf	$V_{IN} = 0V$
C_{IO}	Input/Output Capacitance	7	pf	$V_{OUT} = 0V$

NOTE:

1. This parameter is sampled and not 100% tested.

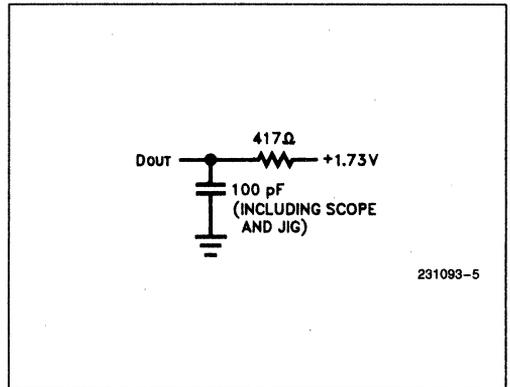


Figure 2. Test Load Configuration

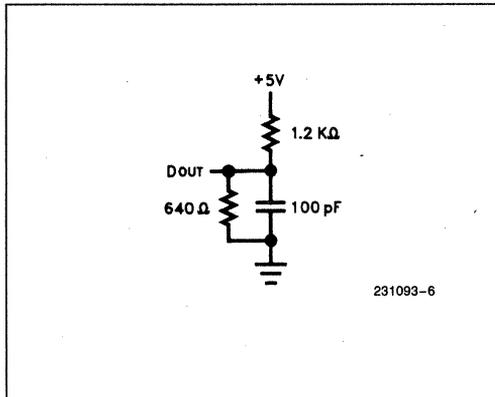


Figure 3. Equivalent Load Configuration

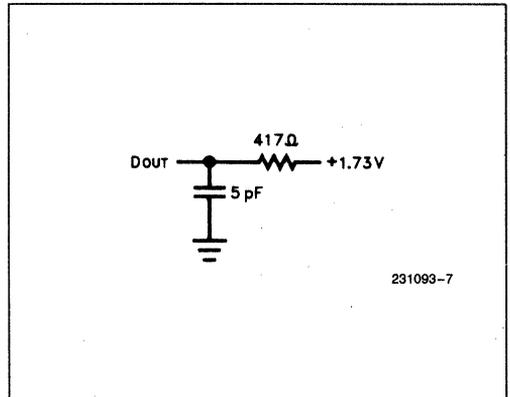


Figure 4. Test Load Configuration for High Impedance Measurements only

A.C. CHARACTERISTICS

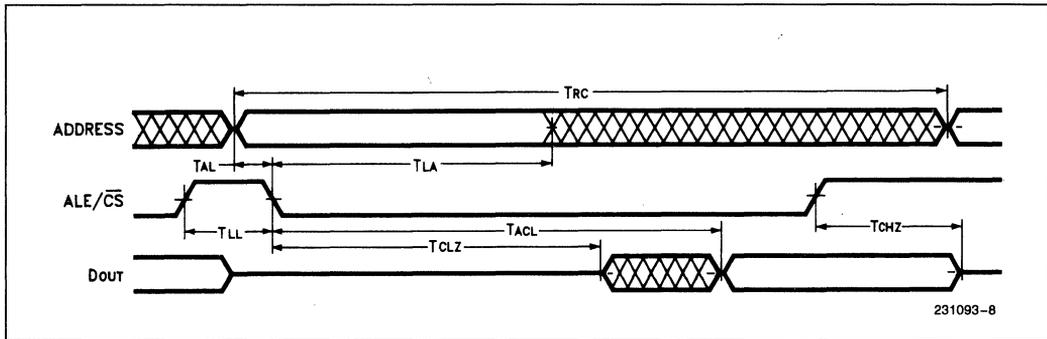
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 20\%$ unless otherwise noted.

READ CYCLE

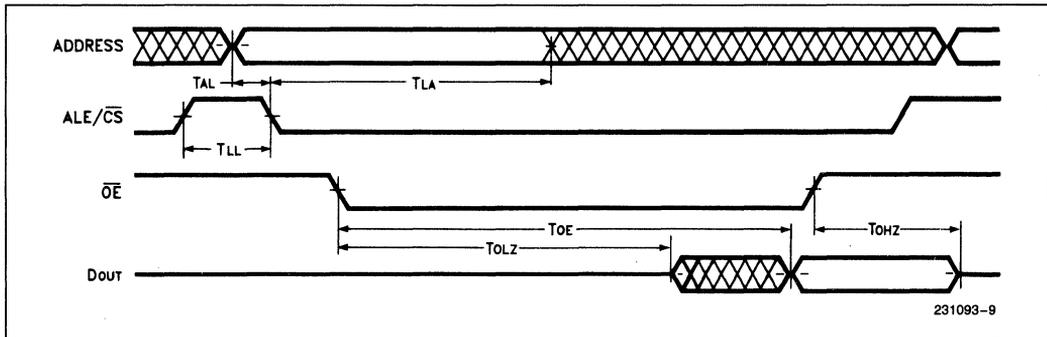
Symbol	Parameter	81C28/L-200 ^[1]		Unit	Notes
		Min	Max		
T_{RC}	Read Cycle Time	250		ns	2
T_{LL}	Chip Deselect Width	25		ns	
T_{AL}	Address to CS-Latch Set Up Time	0		ns	
T_{LA}	Address Hold Time from CS-Latch	40		ns	
T_{ACL}	CS-Latch Access Time		200	ns	
T_{OE}	Output Enable to Output Valid		65	ns	
T_{CLZ}	Chip Selection to Output in Low Z	15		ns	3
T_{OLZ}	Output Enable to Output in Low Z	0		ns	3
T_{CHZ}	Chip Deselection to Output in High Z	0	50	ns	3
T_{OHZ}	Output Disable to Output in High Z	0	50	ns	3

WAVEFORMS

READ CYCLE 1: ALE/ $\overline{\text{CS}}$ Controlled



READ CYCLE 2: $\overline{\text{OE}}$ Controlled



NOTES:

1. Compatible with 12 MHz 80C51-BH/80C31-BH.
2. Cycle Time = Access time (T_{ACL}) + chip deselect width (T_{LL}) + 25 nS output hold.
3. Transition is measured ± 500 mV from steady state voltage with load shown in Figure 4.

A.C. CHARACTERISTICS

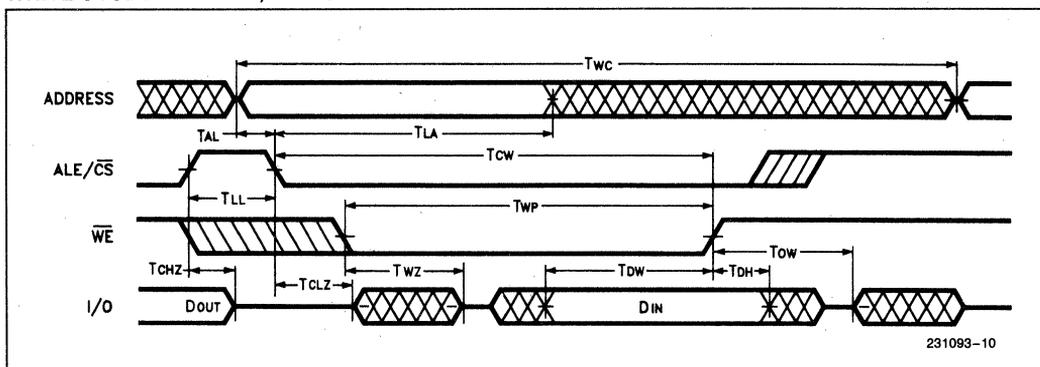
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 20\%$ unless otherwise noted.

WRITE CYCLE

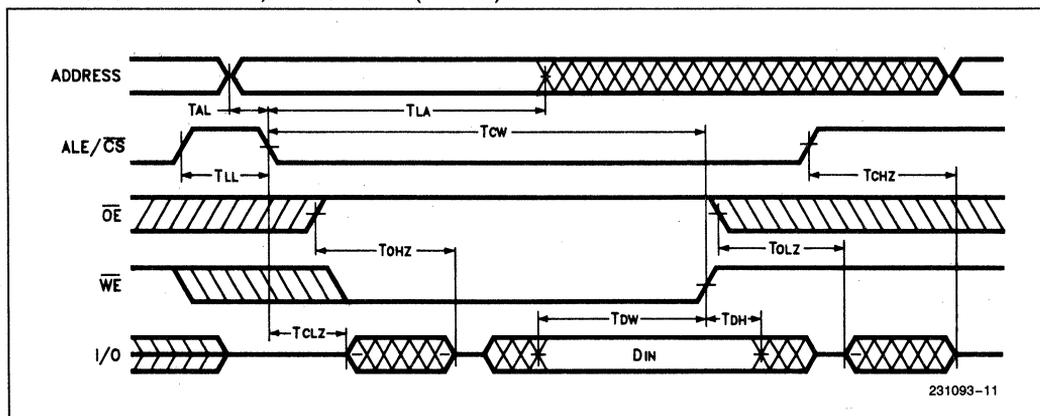
Symbol	Parameter	81C28/L-200		Unit	Notes
		Min	Max		
T_{WC}	Write Cycle Time	250		ns	2
T_{CW}	CS-latch to End of Write	160		ns	2
T_{WP}	Write Pulse Width	100		ns	2
T_{DW}	Data to Write Time Overlap	65		ns	2
T_{DH}	Data Hold from Write Time	0		ns	2
T_{WZ}	Write to Output in High Z	0	50	ns	1
T_{OW}	Output Active from End of Write	15		ns	1

WAVEFORMS

WRITE CYCLE 1: ALE/ $\overline{\text{CS}}$, $\overline{\text{WE}}$ Controlled



WRITE CYCLE 2: ALE/ $\overline{\text{CS}}$, $\overline{\text{WE}}$ Controlled (with $\overline{\text{OE}}$)



NOTES:

1. Transition is measured ± 500 mV from steady state voltage with load shown in Figure 4.
2. Can terminate write cycle with either $\overline{\text{CS}}$ or $\overline{\text{WE}}$.

Application Information

The 81C28 is perfectly compatible with the 80C51-BH timings, so that absolutely no wait states are necessary. When accessing external memory, the 80C51-BH emits the upper address byte from port 2 and the lower address byte as well as the data from port 0. The lower address and data are time multiplexed on P0 and are connected to both the A0-A7 and DI/O0-7 pins of the 81C28. ALE provides the signal necessary to separate in time the address from data for the 81C28 and is connected to the ALE/ \overline{CS} input pin. Two pins on port 3 (P3.6 and P3.7) provide the necessary read and write signals for proper control of the 81C28. The \overline{RD} signal is connected directly to the 81C28 \overline{OE} to allow data to be transferred to the 80C51-BH. External data memory is accessed from the 80C51-BH through the use of MOVX instructions. At 12 MHz, the 80C51-BH has a 1 μ sec cycle time which substantially reduces power consumption when using CMOS input levels (See Figure 6). The 80C51-BH also emits a \overline{PSEN} pulse which is for program storage. This can be used for an additional 64k of program memory space.

With CMOS input levels, the 81C28 FAMILY features very low standby currents of 50 μ A for the low power version and 100 μ A for the standard version. With μ watt standby power, battery backup operation can be accommodated. With the very low active current of 10 mA for CMOS inputs, full battery operation can also be designed. When coupled with the 80C51 at 12 MHz, active power consumption is even lower.

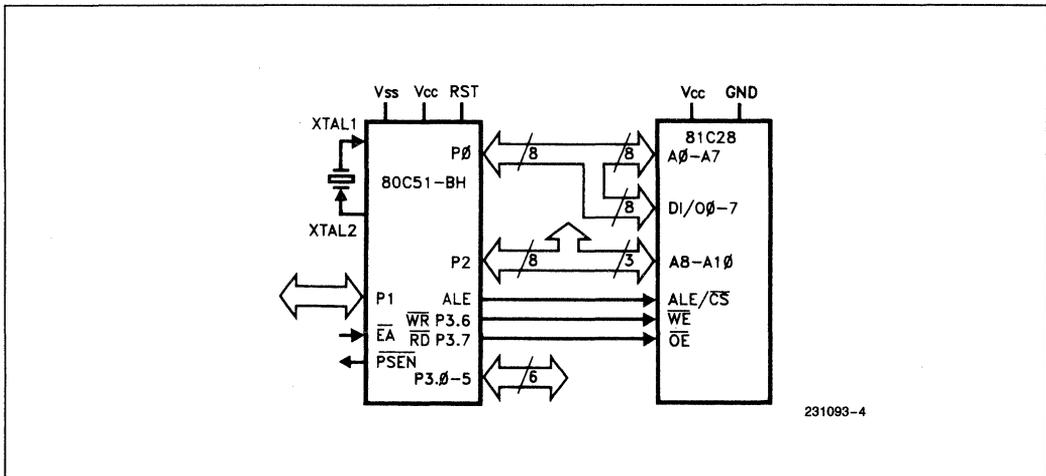


Figure 5. Hardware Interfacing of 81C28 to 80C51

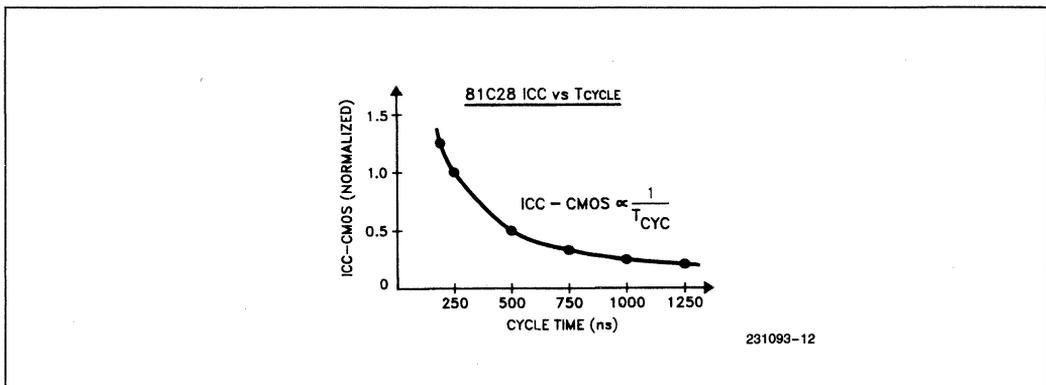


Figure 6. 81C28 ICC vs TCYCLE

27C64/87C64 64K (8K x 8) CHMOS UV ERASABLE PROM

- **CHMOS Microcontroller and Microprocessor Compatible**
 - 87C64-Integrated Address Latch
 - Universal 28 Pin Memory Site, 2-line Control
- **Low Power Consumption**
 - 10 mA Maximum Active Current
 - 100 μ A Maximum Standby Current
- **High Performance Speeds**
 - 200 ns Maximum Access Time
- **Noise Immunity Features**
 - $\pm 20\%$ V_{CC} Tolerance
 - Maximum Latch-up Immunity Through EPI Processing
- **Fast, Reliable intelligent Programming™**
 - Programs in Under 1 Minute
 - 12.5V V_{pp} , HMOS II-E Compatible

Intel's 27C64 and 87C64 CHMOS EPROMs are 64K bit 5V only memories organized as 8192 words of 8 bits. They employ advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 87C64 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C64 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 2764A (HMOS II-E).

The 27C64 and 87C64 achieve both high performance (200 ns access times) and low power consumption (10 mA active current maximum CMOS inputs) making them ideal for high performance, portable equipment. Special EPI processing also reduces these devices' susceptibility to latch-up, a common CMOS quality problem, and enables wide V_{CC} tolerances (20%) in CMOS systems. These features simplify the design of electronic equipment which is subject to high noise environments.

The 87C64 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can tie combined (multiplexed) address-data processor busses directly into both the A0-A7 and O0-O7 pins of the 87C64. During ALE high (ALE/ \overline{CS}) the address information is allowed to flow into the EPROM and begin accessing the stored code. On the falling edge of the ALE input (ALE/ \overline{CS}), address information at the address inputs is latched internally. The A0-A7 inputs are then ignored as data information is passed on the same bus from the EPROM O0-O7 Pins (ALE/ \overline{CS} remains low).

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from -1V to $V_{CC} + 1V$.

*HMOS and CHMOS are patented processes of Intel Corporation.

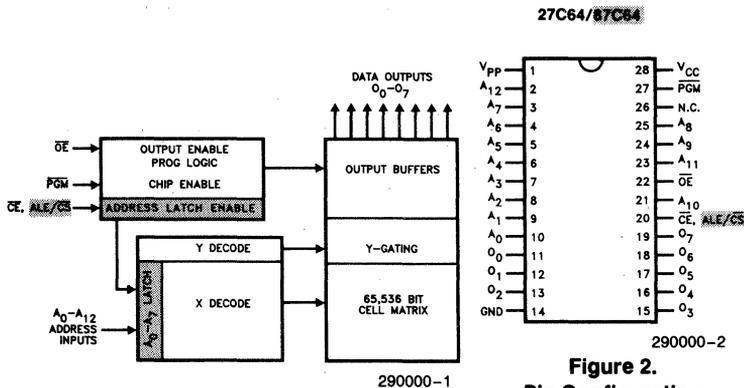


Figure 1. Block Diagram

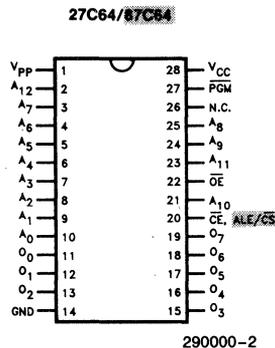


Figure 2.
Pin Configuration

Table 1. Pin Names

A ₀ -A ₁₂	ADDRESSES
O ₀ -O ₇	OUTPUTS
OE	OUTPUT ENABLE
CE	CHIP ENABLE
ALE/ \overline{CS}	ADDRESS LATCH ENABLE /CHIP SELECT
PGM	PROGRAM STROBE
N.C.	NO CONNECT

Shaded Areas represent the 87C64 version

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to +65°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to 7V(1)
Voltage on Pin 24 with Respect to Ground	-2.0V to +13.5V(1)
V _{PP} supply Voltage with Respect to Ground during programming	-2.0V to +14V(1)
Operating Temperature During Read ..	0°C - 70°C(2)

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION D.C. CHARACTERISTICS

Symbol	Parameter	Notes	Min	Typ ³	Max	Unit	Test Condition
I _{LI}	Input Load Current			0.01	1.0	μA	V _{IN} = 5.5V
I _{LO}	Output Leakage Current			0.01	1.0	μA	V _{OUT} = 5.5V
I _{CC} TTL	Operating Current TTL inputs	4			20, 30	mA	$\overline{CE} = \overline{OE} = V_{IL}$ V _{PP} = V _{CC} , O ₀₋₇ = 0 mA
I _{CC} CMOS	Operating Current	4			10.0	mA	$\overline{CE} = \overline{OE} = V_{IL}$ V _{PP} = V _{CC} , O ₀₋₇ = 0 mA
I _{SB} TTL	Standby Current TTL Inputs	4			1.0	mA	$\overline{CE} = V_{IH}$
I _{SB} CMOS	Standby Current CMOS Inputs	5			100.0	μA	$\overline{CE} = V_{IH}$
I _{PP}	V _{PP} Read Current	6			100.0	μA	V _{PP} = V _{CC}
V _{IL}	Input Low Voltage (±10% supply) (±20% supply)		-0.5 -0.5		0.8 0.5	V	V _{PP} = V _{CC}
V _{IH}	Input High Voltage (±10% supply) (±20% supply)		2.0 2.5		V _{CC} +0.5 V _{CC} +0.5		V _{PP} = V _{CC}
V _{OL}	Output Low Voltage				0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage		2.4			V	I _{OH} = -400 μA
I _{OS}	Output Short Circuit Current	7			+100	mA	
V _{PP}	V _{PP} Read Voltage	8	V _{CC} -0.7		V _{CC}	V	

NOTES:

- Minimum D.C. input voltage is -0.5V. During transitions, the inputs may undershoot to -2.0V for periods less than 20 ns.
- Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
- Typical limits are at V_{CC} = 5V, T_A = +25°C
- 20 mA for STD and -3 versions; 30 mA for -2 versions
TTL inputs: spec V_{IL}, V_{IH} levels
CMOS inputs: GND ± 0.2 to V_{CC} ± 0.2

- ALE/ \overline{CS} or \overline{CE} is V_{CC} ± 0.2V. All other inputs can have any value within spec.
- Maximum Active power usage is the sum I_{PP} + I_{CC}.
- Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
- V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.

CAPACITANCE¹ T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C _{IN}	Address/control capacitance	6	pF	V _{IN} = 0V
C _{OUT}	Output Capacitance	12	pF	V _{OUT} = 0V

NOTE:

1. Sampled. Not 100% tested.

A.C. Testing Load Circuit

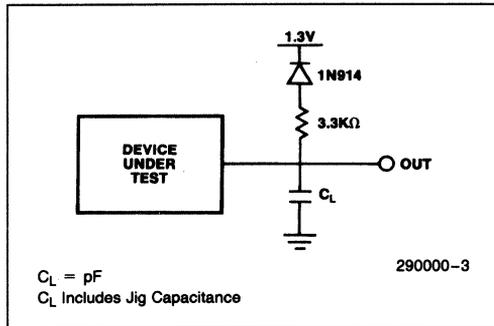


Figure 3. Test Configuration

READ MODE: 27C64

The 27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output enable (\overline{OE}) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

READ MODE: 87C64

The 87C64 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C64 is designed as shown in Figure 4. The processor's multiplexed bus (AD₀₋₇) is tied to both address and data pins of the 87C64. A separate address latch is eliminated.

The 87C64 internal address latch is directly enabled through the use of the ALE/ \overline{CS} line. While the ALE/ \overline{CS} is in the high state, the internal latch is enabled for address flow through. As the transition occurs on the ALE/ \overline{CS} from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM via the \overline{OE} pin.

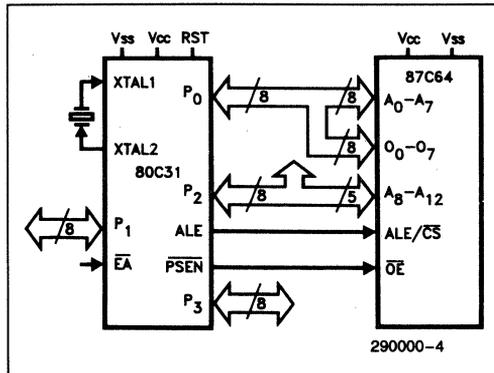


Figure 4. 80C31 with 87C64 System Configuration

Table 2. Read Modes for 27C64 / 87C64

Pins	ALE/ \overline{CS}	\overline{OE}	\overline{PGM}	V_{pp}	Outputs
	CE (20)	(22)	(27)	(1)	(11-13, 15-19)
READ	V _{IL}	V _{IL}	V _{IH}	V _{CC}	D _{OUT}
OUTPUT DISABLE	V _{IL}	V _{IH}	V _{IH}	V _{CC}	High Z
STANDBY	V _{IH}	X	X	V _{CC}	High Z

NOTE:

X can be V_{IH} or V_{IL}.

STANDBY MODE

The 27C64 and 87C64 have Standby modes which reduce the maximum V_{CC} current to 100 μA . Both are placed in the Standby mode when pin 20 is

in the TTL-high state. When in the Standby mode, the outputs are in a high impedance state, independent of the OE input.

READ OPERATION

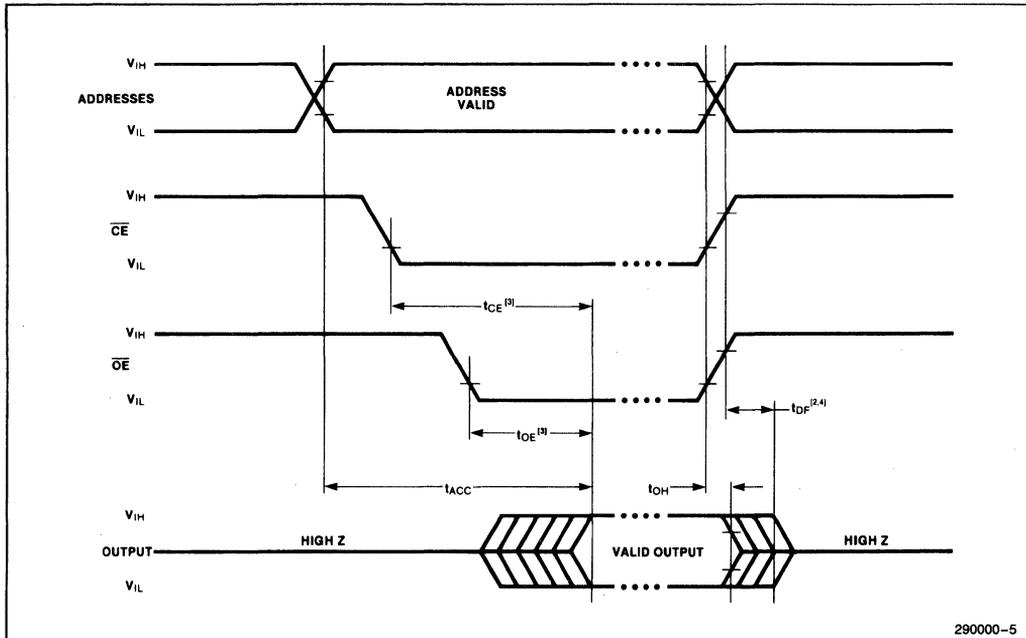
A.C. CHARACTERISTICS: 27C64¹

Versions	$V_{CC} \pm 5\%$	-2	-STD	-3	Unit				
	$V_{CC} \pm 10\%$	-20	-25	-30					
	$V_{CC} \pm 20\%^2$	-200	-250	-300					
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			200		250		300	ns
t_{CE}	\overline{CE} to Output Delay			200		250		300	ns
t_{OE}	\overline{OE} to Output Delay			75		100		120	ns
t_{DF}^3	\overline{OE} or \overline{CE} High to Output High Z			55		60		105	ns
t_{OH}^3	Output Hold from Addresses, \overline{CE} or \overline{OE} Change-Whichever is First.		0		0		0		ns

NOTES:

1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. $\pm 20\%$ V_{CC} versions available in 1985.
3. Guaranteed and sampled.

A.C. WAVEFORMS: 27C64



290000-5

READ OPERATION

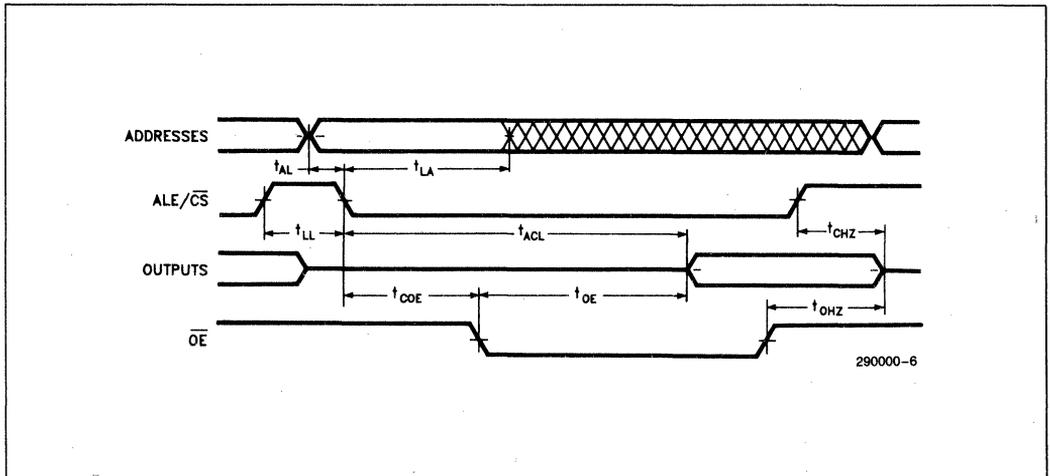
A.C. CHARACTERISTICS: 87C64¹

Versions		$V_{CC} \pm 5\%$		-2		-3		Unit
		$V_{CC} \pm 10\%$		-20		-30		
		$V_{CC} \pm 20\%^2$		-200		-300		
Symbol	Parameter	Min	Max	Min	Max			
t_{LL}	Chip Deselect Width	50		75				
t_{AL}	Address to CS-Latch Set-up	20		30				
t_{LA}	Address Hold from CS-LATCH	45		60				
t_{ACL}	CS-Latch Access Time		200		300			
t_{OE}	Output Enable to Output Valid		75		120			
t_{COE}	\overline{CS} to Output Enable	45		60				
t_{CHZ}^3	Chip Deselect to Output in High Z		50		75			
t_{OHZ}^3	Output Disable to Output in High Z		50		75			

NOTES:

1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. $\pm 20\% V_{CC}$ versions available in 1985.
3. Guaranteed and sampled.

A.C. WAVEFORMS: 87C64



ERASURE CHARACTERISTICS

The erasure characteristics of the 27C64 and 87C64 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C64 or 87C64 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C64 or 87C64 are to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C64 and 87C64 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity \times exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μ W/cm² power rating. The 27C64 or 87C64 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C64 or 87C64 can be exposed to without damage is 7258 Wsec/cm² (1 week @ 12000 μ W/cm²). Exposure of these CHMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from -1V to $V_{CC} + 1V$.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

PROGRAMMING

Caution: Exceeding 14.0V on pin 1 (V_{PP}) may permanently damage the 27C64 or 87C64.

Initially, and after each erasure, all bits of the 27C64 or 87C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27C64 or 87C64 are in the programming mode when the V_{PP} input is at 12.5V and \overline{CE} is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

intelligent Programming™ Algorithm

The 27C64 and 87C64 intelligent Programming Algorithms rapidly program Intel CHMOS II-E EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of one minute. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27C64 or 87C64 intelligent Programming Algorithm is shown in Figure 5.

The intelligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial \overline{CE} pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular 27C64 or 87C64 location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6.0V$ and $V_{PP} = 12.5V$.

When the intelligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = 5.0V$.

PROGRAM INHIBIT

Programming of multiple 27C64 or 87C64 EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level \overline{CE} or ALE/ \overline{CS} input inhibits other 27C64 or 87C64 EPROMs from being programmed.

Except for \overline{CE} or ALE/ \overline{CS} all inputs of the parallel 27C64s or 87C64s may be common. A TTL low-level pulse applied to the PGM and \overline{CE} or ALE/ \overline{CS} input with V_{PP} at 12.5V will program the selected 27C64 or 87C64.

VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with OE and CE or ALE/CS at V_{IL} . Data should be verified a minimum of t_{OE} after the falling edge of OE.

intelligent Identifier™ Mode

The intelligent identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for

use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the 27C64 or 87C64.

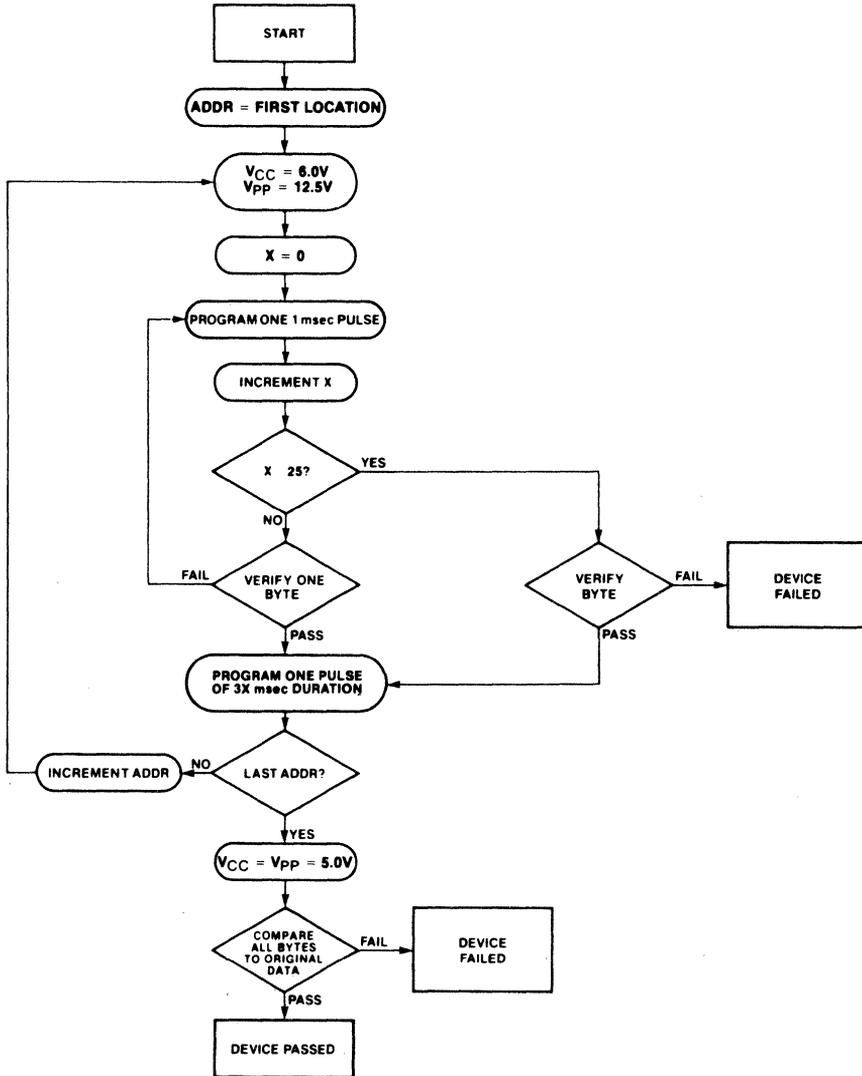
To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the 27C64 or 87C64. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during intelligent identifier Mode.

Table 3. Programming Modes for 27C64 and 87C64

Pins	ALE/CS CE (20)	OE (22)	PGM (27)	A ₉ (24)	A ₀ (10)	V _{PP} (1)	V _{CC} (28)	Outputs (11-13, 15-19)
Mode								
intelligent Programming	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	$6.0V^4$	D _{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	$6.0V^4$	D _{OUT}
Program Inhibit	V_{IH}	X	X	X	X	V_{PP}	$6.0V^4$	HIGH Z
intelligent Identifier ³ -Manufacturer	V_{IL}	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	V_{CC}	89 H
intelligent Identifier ³ -27C64	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IH}	V_{CC}	V_{CC}	07 H
intelligent Identifier ^{3,5} -87C64	V_{IL}	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	37 H

NOTES:

1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. $A_1-A_8, A_{10-12} = V_{IL}$
4. $V_{CC} = 6.0V \pm 0.25V$
5. Available in 1985



290000-7

Figure 5. 27C64 and 87C64 intelligent Programming™ Flowchart

intelligent Programming™ ALGORITHM
D.C. PROGRAMMING CHARACTERISTICS:
 $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6.0\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.5\text{V}$

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1\text{ mA}$
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400\ \mu\text{A}$
I_{CC2}	V_{CC} Supply Current		30	mA	
I_{PP2}	V_{PP} Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$

A.C. PROGRAMMING CHARACTERISTICS: 27C64

Symbol	Parameter	Limits				Test Conditions
		Min	Typ	Max	Unit	
t_{CES}	\overline{CE} Setup Time	2			μs	
t_{DS}	Address Setup Time	2			μs	
t_{OES}	\overline{OE} Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}^3	\overline{OE} High to Output Float Delay	0		130	ns	
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{PW}	PGM Initial Program Pulse Width	0.95	1.0	1.05	ms	(See Note 1)
t_{OPW}	PGM Overprogram Pulse Width	2.85		78.75	ms	(See Note 2)
t_{OE}	Data Valid from \overline{OE}			150	ns	

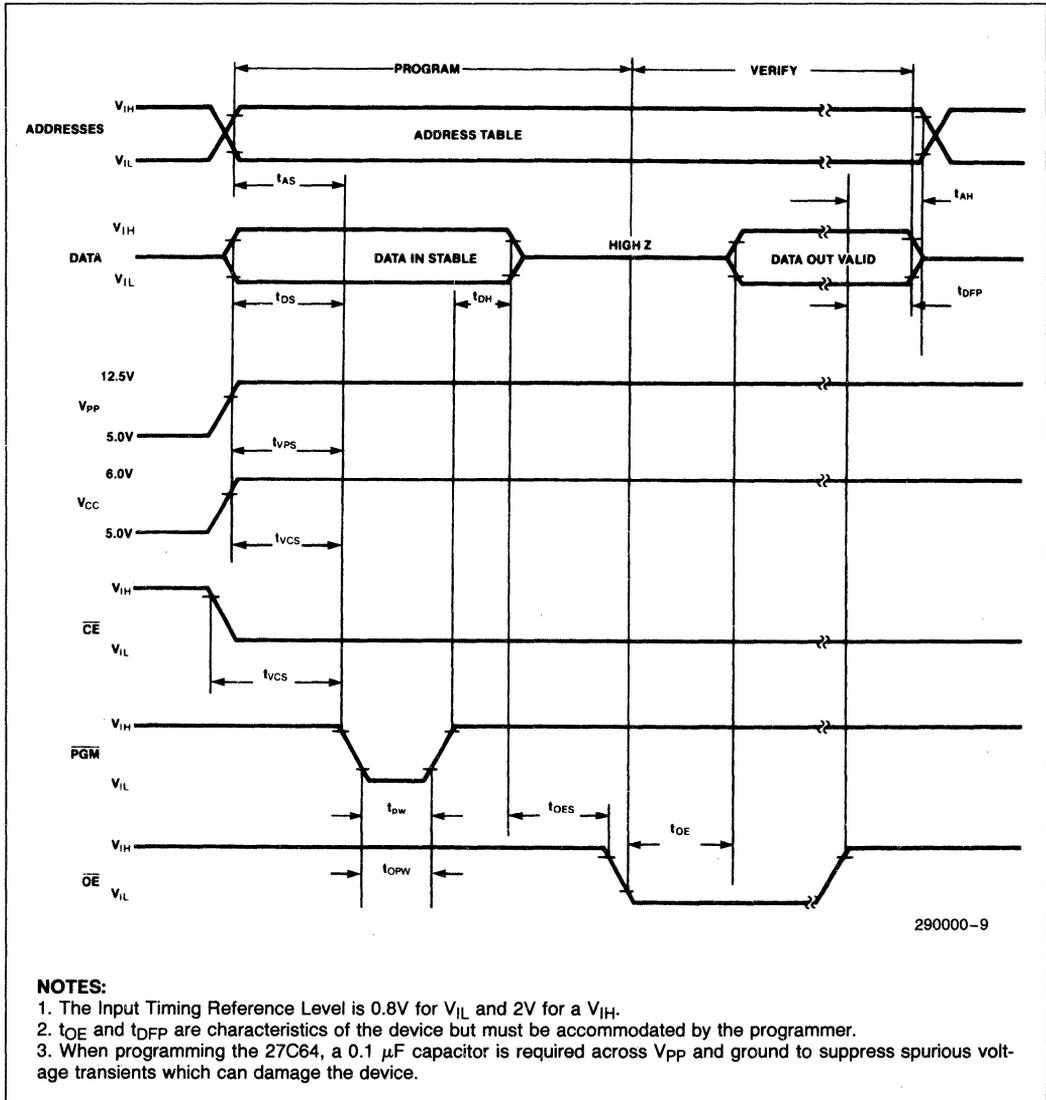
A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20 ns
 Input Pulse Levels 0.45V to 2.4V
 Input Timing Reference Level 0.8V and 2.0V
 Output Timing Reference Level 0.8V and 2.0V

NOTES:

1. Initial Program Pulse width tolerance is 1 msec \pm 5%.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

intelligent Programming™ Waveforms: 27C64



NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH} .
2. t_{OE} and t_{DFF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C64, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

A.C. PROGRAMMING CHARACTERISTICS: 87C64

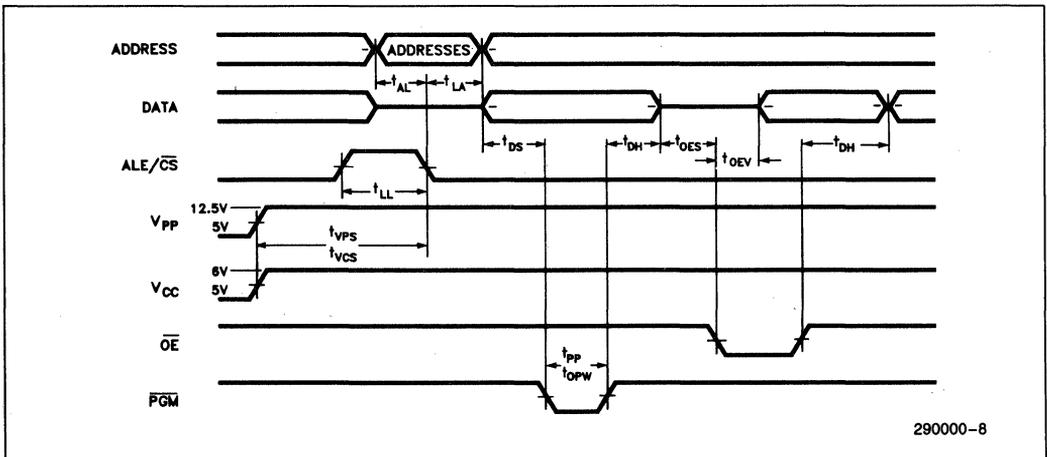
$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6.0 \pm 2.5\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.5\text{V}$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{LL}	Chip Deselect Width	2			μs	
t_{AL}	Address to Chip Select Setup	1			μs	
t_{LA}	Address Hold from Chip Select	1			μs	
t_{PP}	$\overline{\text{PGM}}$ Initial Pulse Width	0.95	1.0	1.05	μs	
t_{OPW}	$\overline{\text{PGM}}$ Overprogram Pulse Width	2.85		78.75	μs	
t_{DS}	Data Setup Time	2			μs	
t_{DH}	$\overline{\text{OE}}$ High to Data Float			150	ns	
t_{OES}	Output Enable Setup Time	2			μs	
t_{OEV}	Data Valid from Output Enable			150	ns	

NOTE:

Programming tolerances and test conditions are the same as 27C64

Intelligent Programming™ WAVEFORMS: 87C64



Telecommunications Components

3

iATC 29C50 and 29C51 FEATURE CONTROL COMBO

- 29C50 22-pin, 7 signaling channels
 - 29C51 28-pin, 10 signaling channels, secondary analog inputs and outputs
- | | |
|---|---|
| <ul style="list-style-type: none"> ■ External and User Programmable Transmit and Receive Gain ■ Programmable Internal and External Hybrid Balance Network Select ■ Programmable Analog, Digital, and Subscriber Loopback | <ul style="list-style-type: none"> ■ Programmable μ/A-Law Select ■ Flexible Signaling Interface ■ Secondary Analog Channel ■ Three-Party Conferencing ■ Low Power Consumption |
|---|---|

The Intel iATC 29C50/29C51 Feature Control Combo is an advanced user-programmable, fully integrated PCM Codec with transmit/receive filters fabricated in a CMOS technology. This technology is built on CHMOS and will allow the 29C50 and 29C51 to realize the same excellent transmission performance as in the Intel 2913/2914 combo while achieving the low power consumption typical of CMOS circuits.

The 29C50/29C51 are the first members of Intel's third generation advanced telecommunication components. The Feature Control Combo supports the analog subscriber with a variety of added per-line features to the normal BORSCHT functions associated with the analog line circuit. Some of these features include secondary analog channels, programmable transmit and receive gain, on-chip or custom hybrid balancing network selection, a flexible signaling interface, and programmable μ or A-law conversions.

The 29C50/29C51 is intended for use with the 2952 Integrated Line Card Controller in digital switching environments. These components allow the system transmit and receive backplane highways to operate at different frequencies from that of the subscriber interface data channels. The 2952 handles the transfer of primary voice, secondary analog data, feature control, and signaling information between the backplane and up to 8 29C50/29C51's.

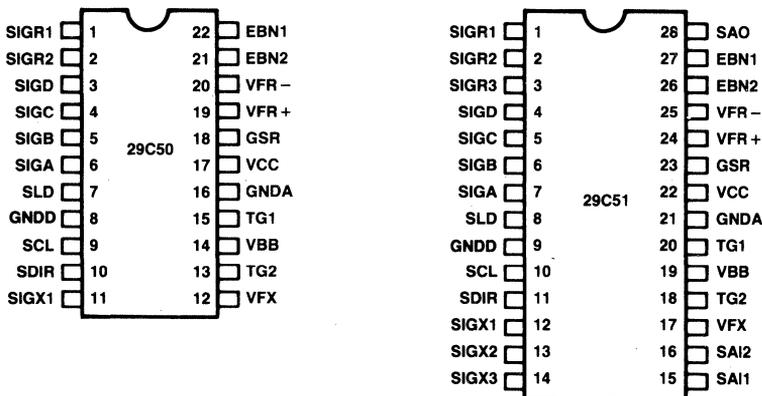


Figure 1. Pin Configuration

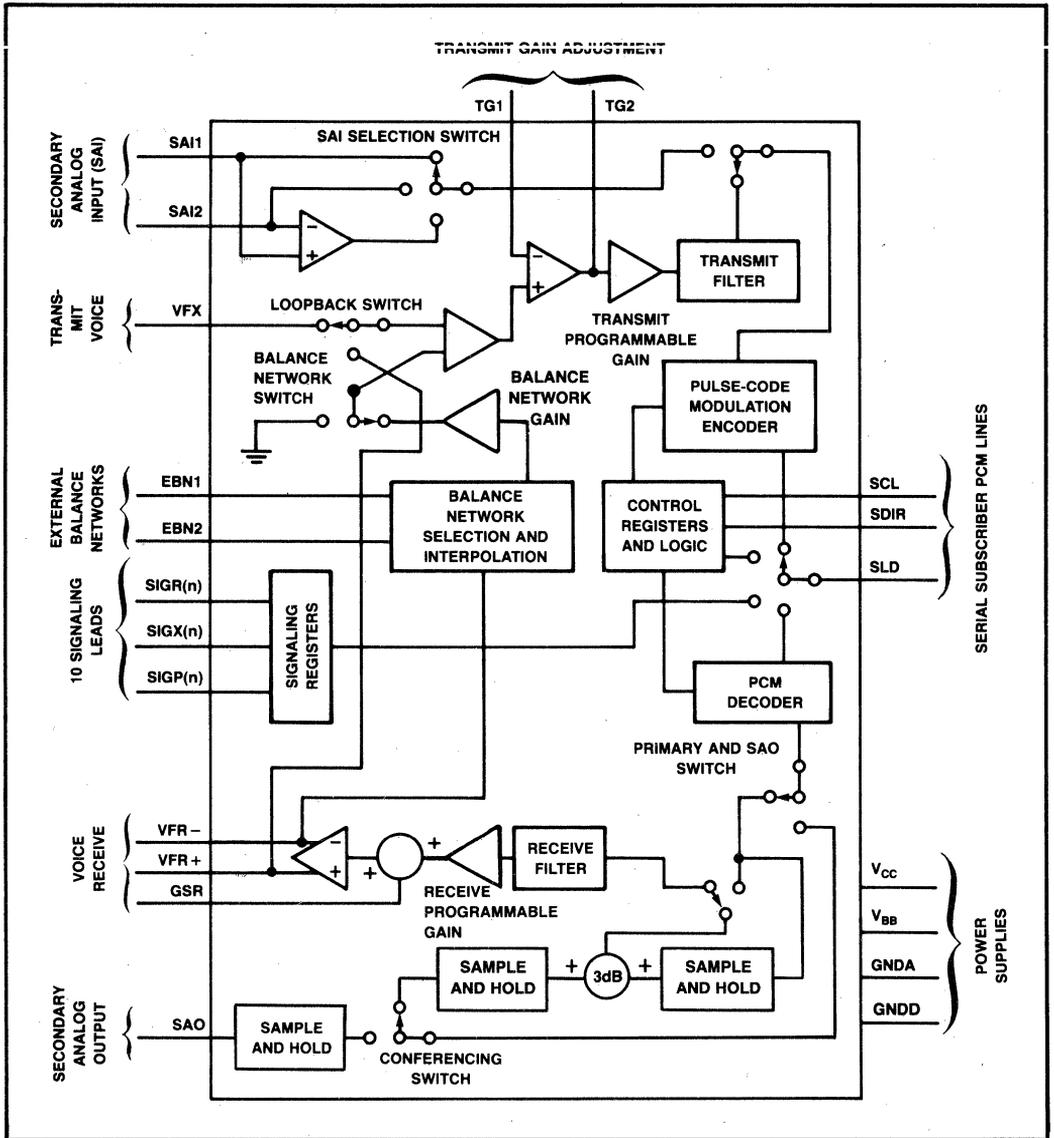


Figure 2. Block Diagram

Table 1. Pin Names

VFX	Analog Input	SCL	Subscriber Clock
VFR +, VFR –	Analog Output	SLD	Subscriber Data Link
SAI1, SAI2	Secondary Analog Inputs	SDIR	Subscriber Direction
SAO	Secondary Analog Output	TG1, TG2	Transmit Gain Adjust
GNDD	Digital Ground	GSR	Receive Gain Adjust
GNDA	Analog Ground	EBN1, EBN2	External Balance Network
V _{CC}	Power (+5V)	SIGX1, X2, X3	Transmit Signaling Input
V _{BB}	Power (–5V)	SIGR1, R2, R3	Receive Signaling Output
		SIGA, B, C, D	Programmable Transmit/ Receive Signaling Lead

Table 2. Pin Description

Symbol	Function	Symbol	Function
VCC	Most positive supply; input voltage is +5V ± 5%.	SAO	Secondary analog output, capable of driving loads of a least 10kΩ.
VBB	Most negative supply; input voltage is –5V ± 5%.	SCL	Subscriber clock. Supplied by the 2952 line card controller, this is a 512 kHz, 50% or 33% duty cycle clock. Input will accept TTL levels.
GNDA	Analog ground return line. Not internally connected to GNDD.	SDIR	Subscriber direction signal and frame sync. When high, SLD becomes an input and data is transferred from the 2952 to the 29C51. When low, the output buffer on the 29C51 SLD pin is enabled and data is transferred from the 29C51 to the 2952. Input will accept TTL levels.
GNDD	Digital ground return line. Not internally connected to GNDA.	SLD	Subscriber data link. A 512kbps bi-directional serial data port, which is clocked by SCL. SLD becomes a TTL compatible input when SDIR is high and an output capable of driving one TTL load when SDIR is low.
VFX	Analog voice input to transmit channel.	SIGX1 SIGX2 SIGX3	Transmit signaling inputs. Data present at SIGX(n) is latched by an internal signal preceding the falling edge of SDIR and is serially transferred on SLD during the transmit signaling byte. TTL compatible.
TG1	Inverting input to transmit gain adjusting op-amp. Feedback point for external gain adjusting resistor network up to 10k ohm.	SIGR1 SIGR2 SIGR3	Receive signaling outputs. Data received serially on SLD during the receive signaling byte is latched on these outputs during the following byte. Capable of driving one TTL load.
TG2	Output of the transmit gain adjusting op-amp. Will drive external gain adjusting resistor network up to 10k ohm.	SIGA SIGB SIGC SIGD	Programmable signaling pins. If the appropriate bit in the feature control memory is set high (either SIGDA, SIGDB, SIGDC, or SIGDD), the corresponding pin will become a receive signaling output, like SIGR(n). If the bit in the feature control memory is set low, the corresponding pin will become a transmit signaling input, like SIGX(n). Inputs will accept TTL level inputs, and outputs can drive one TTL load.
VFR +	Non-inverting output of the power amplifier. Capable of directly driving transformer hybrids or high impedance loads either single ended or differentially.		
VFR –	Inverting output of power amplifier. Capable of directly driving transformer hybrids or high impedance loads either single ended or differentially.		
GSR	Input to receive gain setting circuit. An external resistor network connected between VFR – and VFR +, and GSR sets the receive channel gain from 0dB to –9.54dB. Connecting GSR to GNDA will set the gain at –6.02dB.		
EBN1	Input for the first external balance network.		
EBN2	Input for the second external balance network.		
SAI1	First secondary analog input, also the non-inverting input if differential secondary analog input mode is selected.		
SAI2	Second secondary analog input, also the inverting input if differential secondary analog input mode is selected.		

FUNCTIONAL DESCRIPTION

The 29C50/29C51 is a combined channel filter and PCM codec for use on analog line interface circuit boards in a digital telecommunications switching system. This device resides between the circuitry which provides the "BORSHT" functions for a given line, and the shared line board controller. It provides the transmit and receive voice-path filtering and compressed analog-to-digital and digital-to-analog conversions necessary to interface a full duplex (4-wire) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system.

All features of the 22-lead device (29C50) are identical to that of the 28-lead device (29C51) except for the number of signaling pins and the secondary channel capabilities. There are 10 signaling channels available on the 29C51 configured as three transmit, three receive, and four programmable for either direction. Seven signaling leads are located on the 29C50 providing one transmit, two receive, and four programmable. There are no secondary analog inputs or outputs on the 29C50; however, three-party conferencing is still available.

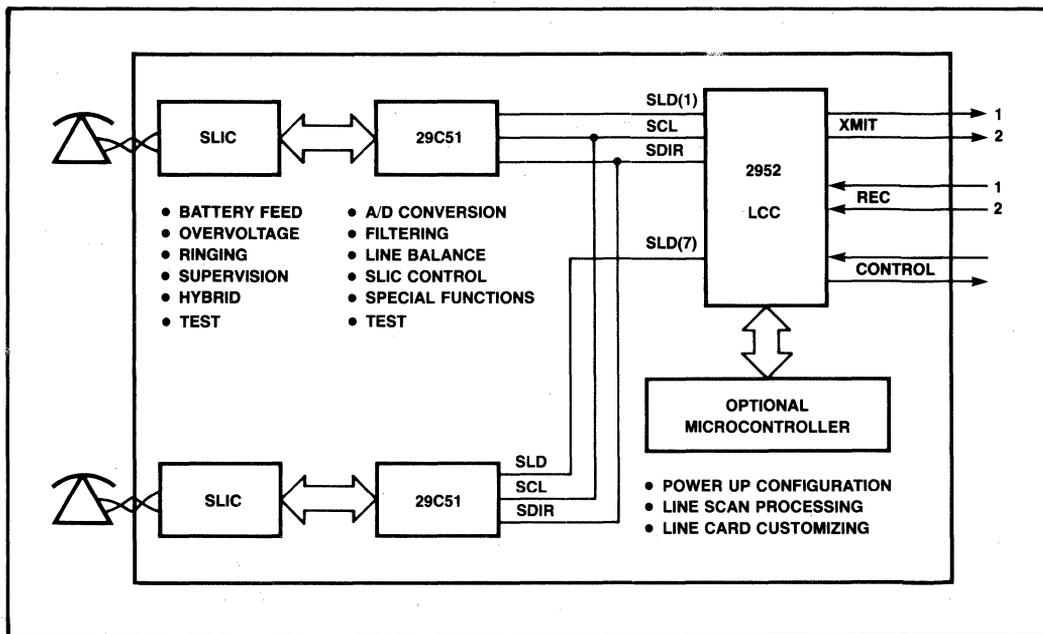


Figure 3. Analog Linecard

TRANSMIT AND RECEIVE OPERATION

Transmit Filter

A low pass anti-aliasing section is included on chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stop-band attenuation which fulfills the AT&T D3/D4 specification and the CCITT G.712 recommendation. The 29C50 and 29C51 specifications meet the digital

class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 10.

A high pass section configuration rejects low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Gain of up to 20dB can be set without degrading the performance of the filter.

Encoding

The output of the transmit filter is internally sampled by the encoder and held on an internal sample and hold capacitor. DC offset is corrected by an on-chip auto zero circuit. The signal is then encoded and presented as PCM data on the SLD lead on the first 8 bits of the XMIT half frame (fifth byte). Secondary analog input signals are routed directly to the encoder and output in the sixth byte on the SLD.

Decoding

The PCM words received on the SLD are demultiplexed and sent to the decoder. The decoded value is held on an internal sample and hold capacitor. If the secondary analog channel is being used, the PCM word received in the second byte on the SLD is decoded, then held on another sample and hold capacitor before appearing on the secondary analog output (SAO). If, however, conferencing has been selected, the two converted signals will be added and subsequently passed to the receive filter.

Receive Filter

The receive section of the filter provides a passband flatness and stopband rejection which fulfills the AT&T D3/D4 specification and the CCITT G.712 recommendation. The receive filter transfer characteristics and specifications will be within the limits shown in Figure 11.

GENERAL OPERATION

External Gain Setting

Both transmit and receive gain levels are factory trimmed, but can be modified by external resistors during line card assembly. The value of transmit gain is adjusted by connecting resistors RT1 and RT2 (see Figure 4) at the two external gain setting control pins, TG1 and TG2. These two pins are the input and output of an on-board gain amplifier stage, and the resistors provide the necessary input and feedback for gain control. The value of external gain is given by:

$$A = 1 + RT1/RT2$$

For unity gain, pins TG1 and TG2 are tied together. Similarly, for the receive section, external resistors RR1 and RR2 at pins VFR+, GSR, and VFR- set the external gain given by:

$$A = (RR1 + RR2)/(RR1 + 3RR2)$$

A value greater than 10k ohms and less than 100k ohms for R1 + R2 is recommended. The output is capable of driving loads of 300 ohms at 3.2Vp single ended or 600 ohms at 6.4Vp differentially.

Three additional gain settings of 0dB, -6dB, and -9.54dB can be realized without using any external

components by strapping pin GSR to VFR-, GNDA, and VFR+, respectively.

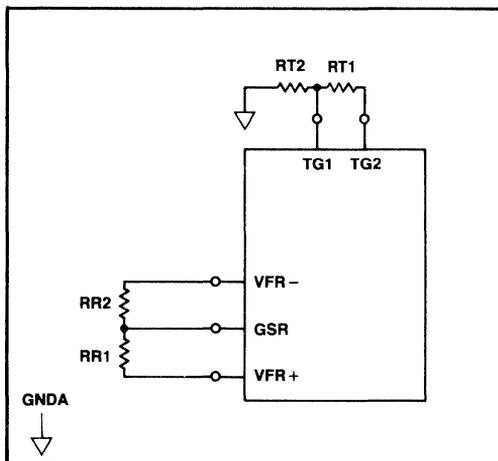


Figure 4. External Gain Connections

Hybrid Balancing Network

The 2- to 4-wire conversion necessary for subscriber interface is partially integrated on-chip. Network line balancing needed to minimize the trans-hybrid loss from the receive to transmit direction analog signals is handled internally. The three internal networks shown in Figure 6 may be selected by programming the appropriate feature control byte. These networks are integrated in a switched capacitor configuration and have single pole-zero characteristics in the 200 Hz to 3200 Hz range. They were chosen to serve a wide base of U.S. and European requirements, and can be used as standard line balancing networks or as test networks.

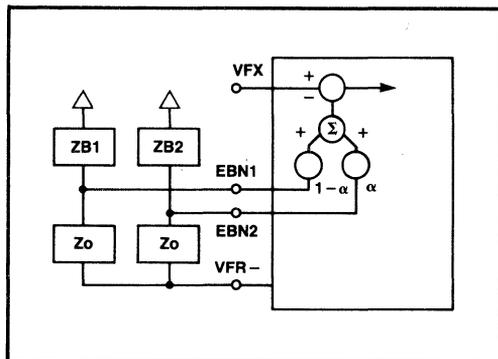


Figure 5. External Balance Network and Interpolation Configuration

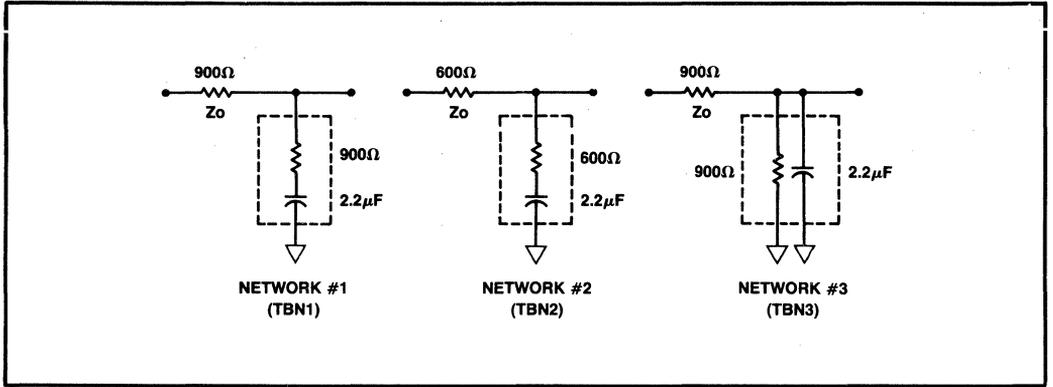


Figure 6. Internal Balance Networks

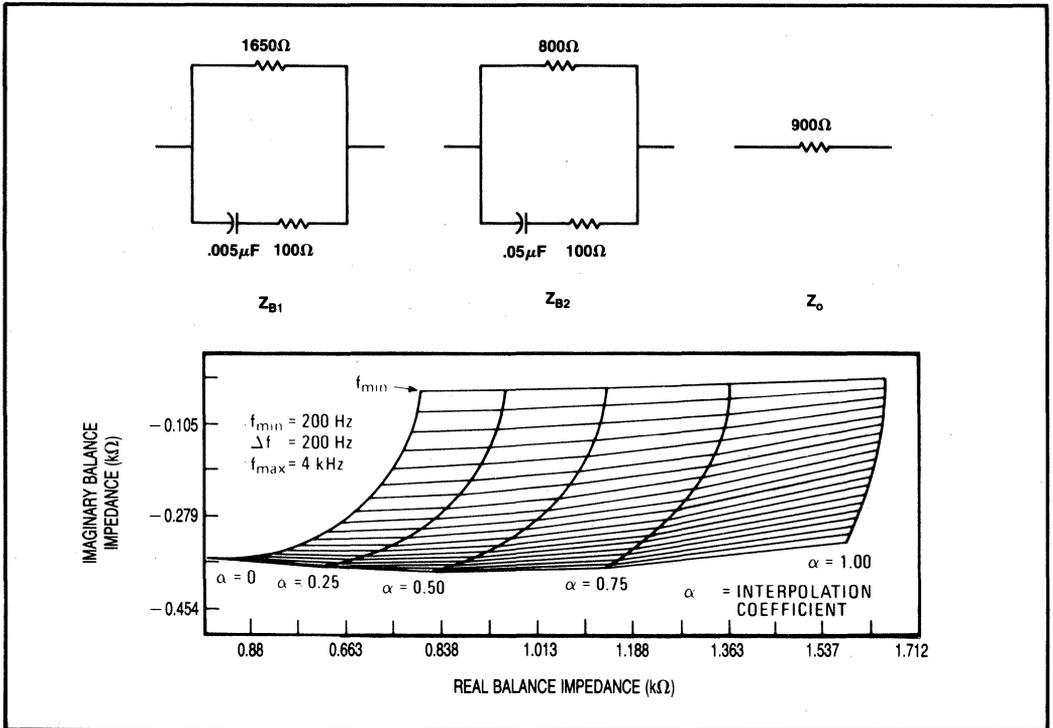


Figure 7. Typical External Balance Networks and Complex Impedance Plot

Additionally, the user may apply two external balance networks to accommodate varying subscriber loop characteristics (See Figure 5 for external connections). Presumably, these two networks can represent the two extremes of line conditions in different applications such as long or short loops and loaded or unloaded lines. To serve typical lines with characteristics in between the two extremes, the interpolation capability provides a weighted average of the network frequency characteristics. If the external network at EBN1 produces a transfer function $H1(f) = ZB1 (Z_o + ZB1)$ and the network at EBN2 produces $H2(f) = ZB2 (Z_o + ZB2)$, the balance signal can be programmed to have the transfer function $H(f)$:

$$H(f) = \alpha H1(f) + (1 - \alpha) H2(f)$$

where " α " is the interpolation coefficient programmed to have any of the five values of 0, .25, .50, .75, or 1.0. Figure 5 displays how the subtraction of the coupling signal is implemented inside the device.

As an example, the two external networks shown in Figure 7 represent typical hybrid balance networks for loaded (ZB1) and unloaded (ZB2) analog loops. The graph in Figure 7 shows the real and imaginary components of the equivalent impedance of these two networks as a function of frequency and the interpolation coefficient.

Secondary Analog Channel/Conferencing

The 29C51 offers two simultaneous unfiltered information channels beyond the primary channel. Narrow band analog signals can be supplied for such applications as telemetry, teleconferencing, remote loop testing, or various control uses.

The secondary analog channel is accessed through two inputs, SAI1 and SAI2, sampled either single ended or differentially. The unfiltered secondary analog output, SAO, is a stair-step signal with the inherent \sin^2/x frequency rolloff following D/A conversion.

To allow three-party conferencing, the third party voice information can be transmitted and received during the data bytes carrying the secondary analog channel information. In the receive direction the primary and secondary voice signals are held on separate internal capacitors following D/A conversion, then passed through a -3dB attenuator and summed together. The combined signal is smoothed in the receive filter and passed onto the output power amplifier. In the transmit direction, the pulse-code modulation encoder inserts the primary voice into both the fifth and sixth SLD bytes.

Precision Voltage References

Voltage references are generated on-chip and are trimmed during the manufacturing process. Separate

references are supplied for both the transmit and receive sections of the chip, each trimmed independently. These references determine the gain and dynamic range of the device and provide the user a significant margin for error in other board components.

SLD Interface

The 29C50 and 29C51 are intended for use with the 2952 Line Card Controller which manages the transfer of all voice, feature control and signaling data to and from the Feature Control Combo and the system backplane. The interface between the two consists of just three leads, two of which are clock signals and the third a unique serial bus for communication. Up to eight 29C50/29C51 feature control combos per line card can be controlled by one 2952, all sharing common clock signals, SCL and SDIR.

The subscriber direction (SDIR) lead provides an 8 kHz signal which divides each frame into transmit and receive halves. During the first half when SDIR is high (RCV half-cycle), data is transmitted from the 2952 to the 29C51 and in the second (XMIT half-cycle) transfer is from the 29C51 back to the 2952. Frame synchronization and all internal timing for the digital circuitry is derived from the rising edge of the SDIR signal.

The subscriber clock (SCL) input generated by the 2952 is a fixed 512 kHz clock signal allowing 64 bits (8 bytes) of data to be transferred on the SLD lead during each 125 μsec frame. Depending on 2952 master clock frequency, the SCL duty cycle can be either 50% or 33%.

The subscriber data link (SLD) is a bidirectional serial bus that transfers eight bytes of serial data to and from the 29C51 each frame. During the first half of each frame, RCV channel information is transferred to the 29C51 in four bytes consisting of primary voice, secondary analog, feature control, and signaling information. (The data byte actually contains the secondary analog channel information.) Similarly during the second half-cycle, four bytes of XMIT channel information are sent to the 2952. The MSB (bit 7) of each byte is sent first on the SLD. After the last valid signaling bit is transmitted to the 2952, the bus is placed in a high impedance state for at least one SCL clock cycle to prevent data contention on the bus. (See FCB#6 — Signaling Register.)

Upon power supply application and clocks SCL and SDIR applied, the 29C51 will automatically enter the power down state. During the transmit half cycle (29C51 talking to the 2952) a code of all ones will be sent to the controller during the VOX and DAX bytes.

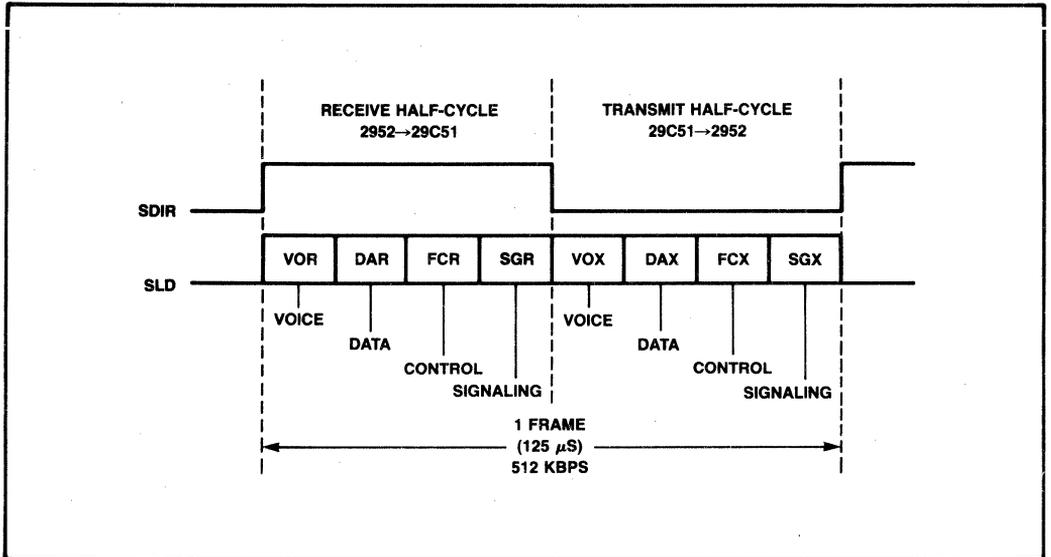


Figure 8. 29C51/2952 Interface

PROGRAMMABLE FEATURES

The 29C51 is configured by the 2952 line card controller by a set of six feature control bytes (FCB). These bytes of information are stored in internal registers which are serially multiplexed to and from the SLD interface in the third and seventh byte locations. The first two bits of each byte consist of a multiframe synchronization and write enable code. The framing bit (bit 7, MSB) establishes the beginning of a feature control frame when set to a logical zero, and increments the feature control counter when set to one. The second (bit 6) enables the writing to the 29C51 when it is the logical complement of the framing bit.

When writing new feature control information to the 29C51, the first byte should contain a framing (F) and write enable (WE) header of 01 (F=0 and WE=1). This designates a new frame of information to trans-

fer. The subsequent bytes should each have F=1 to advance the counter, and WE=0 to enable the write operation.

The controller can also request to verify the feature control register contents by sending a 00 or 11 at the beginning of the byte to be read. To read the first byte, a 00 F/WE code should be sent while each subsequent byte should have a 11 header. An internal six-stage counter is set on the first byte verified then incremented once each 125µs frame. It is reset only upon detection of a 01 or 00 F/WE. Once the counter is greater than six, neither read nor write modes may be selected by sending the 29C51 a 11 framing and write enable code. The 29C51 will then echo in byte 7 the data it received in byte 3.

FCB #1 — Power Up/Down, Loop Back Mode, µA-Law Select Register

POWER UP AND DOWN

The 29C50/29C51 can be instructed to go into the power down or standby mode for reduced power consumption. In this mode, all analog inputs and outputs are placed in a high impedance state, inhibiting all primary voice and secondary data signals. A code of all ones will be output in the voice and data bytes on the SLD. Signaling and feature control information will continue to be processed to allow the 29C51 to be read or reprogramed, and to allow the backplane to monitor the subscriber line.

The 2952 can change the state of the feature control combo from standby to active by sending the first feature control byte only. All other register contents will be preserved during power down provided the power supplies remain connected.

LOOP BACK MODE SELECT

Three modes of remote testing are incorporated in the 29C50/51 and can be selected by appropriate coding in this register. The loopback features allow a number of tests to be performed to determine line quality and balancing. These include digital loop back, analog loop back, and subscriber loop back.

In the digital loopback mode, the combo retransmits the PCM words it receives in the voice and data bytes of the SLD back to the line card controller in the same frame. This feature allows path verification and testing of the circuit up to the slave device.

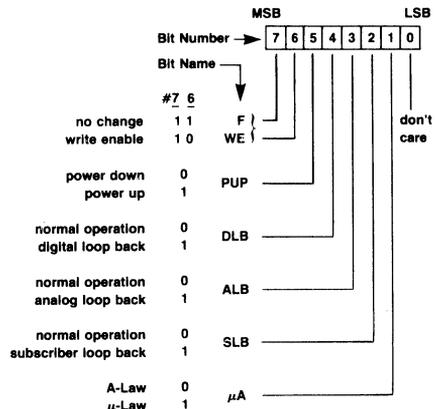
When the analog loopback mode is selected, the analog output VFR+ is internally connected to the analog input VFX. This feature allows functional testing of the combo as well as gain adjustment. The sec-

ondary analog channel is unaffected during this operation.

In the third test mode, subscriber loopback, the digital output of the A/D converter is internally connected to the input of the D/A converter. The analog signal input to VFX is sent through the transmit filter, encoded, then decoded, filtered and output to VFR+ and VFR-. This mode is used primarily for simplifying analog to analog testing from the subscriber side of the line card. If the secondary analog inputs and output are being used, they will be looped back in the same manner.

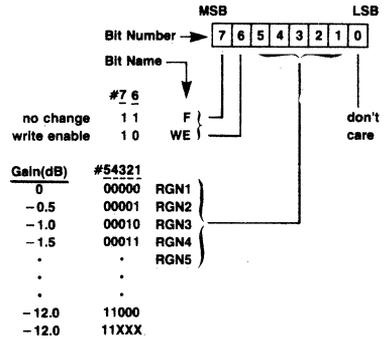
CONVERSION LAWS

The 29C50 and 29C51 can be selected for either µ-law or A-law operations. A user can select either conversion law by assigning the corresponding bit. A logical 1 in bit 1 would select µ-law while a logical 0 would select A-law conversions. Both conversions follow CCITT recommendation G.711.



FCB #2 — Receive Programmable Gain Register

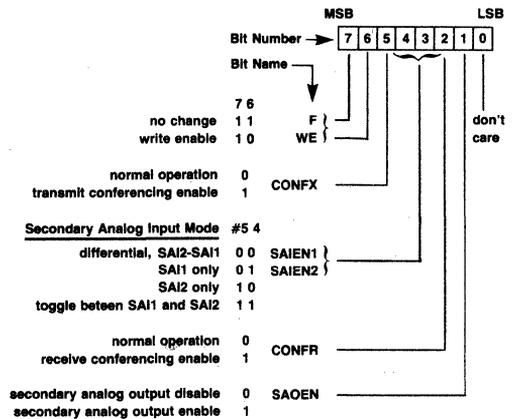
The receive gain levels can be adjusted by applying external resistors as mentioned earlier, or by selective programming of this register. A range from 0 to -12dB in 0.5dB increments can be realized for the receive channel.



FCB #3 — Secondary Analog Channel Register

SECONDARY ANALOG INPUTS AND OUTPUTS

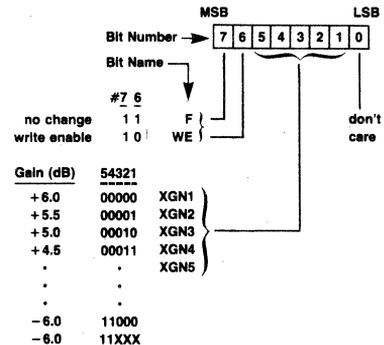
The two inputs to the secondary analog channel, SAI1 and SAI2, can be programmed to be encoded either single ended or differentially. An analog signal applied at the selected input may be encoded once every 125 μsec in addition to the primary voice channel. Alternatively, both SAI1 and SAI2 may be selected in which case each signal would be encoded in alternating frames at an effective sampling rate of 4 kHz. The LSB of the encoded word would toggle between 0 and 1 to designate which input it was encoded from. A "1" in the LSB represents SAI1 and a "0" for SAI2. The two inputs may also be used in a differential mode, resulting in SAI2 subtracted from SAI1.



The receive section of the secondary analog channel can be programmed to direct the data byte output onto SAO, or to add the analog signal to the primary voice channel for conferencing.

FCB #4 — Transmit Programmable Gain Register

The gain setting of the transmit section of the chip operates in the same manner as the receive gain register. A 12dB range from -6.0dB to +6.0dB in 0.5dB increments is available.



FCB #5 — Balance Network Select and Gain Register

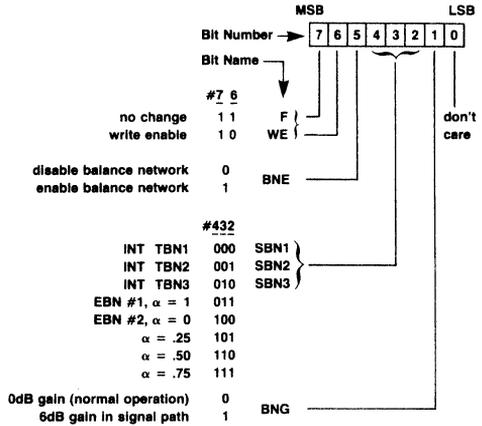
BALANCE NETWORKS

The 29C51 offers a choice of internal or external hybrid balancing. Externally, two balance networks connected to pins EBN1 and EBN2 can be used independently, or as a weighted average of the two. The weighting factor, or interpolation coefficient, can range from 0 to 1 in steps of .25. Setting "α" to be 1 or 0 results in selecting either EBN1 or EBN2 respectively.

Three additional balance network configurations consisting of either a series or parallel RC circuit are located internal to the device. (See Figure 6).

GAIN SETTING

An additional 6dB gain in the balance signal path can be realized by coding this bit with a logical one. A logical zero provides unity gain.



FCB #6 — Signaling Register

Four pins are provided on both the 29C50 and 29C51 chips to be used as selectable transmit or receive signaling inputs. A code of one in the respective bit commits the pin to receive signal information and a zero to transmit. The signaling field format as it appears on the SLD bus is shown in Figure 9 for both the 29C50 and 29C51. R1, R2, and R3 correspond to signaling information received on SIGR1, SIGR2, and SIGR3 respectively. Similarly, programmable pins SIGA, SIGB, SIGC, SIGD, and transmit pins SIGX1, SIGX2, SIGX3 are coded into the bit location as shown below.

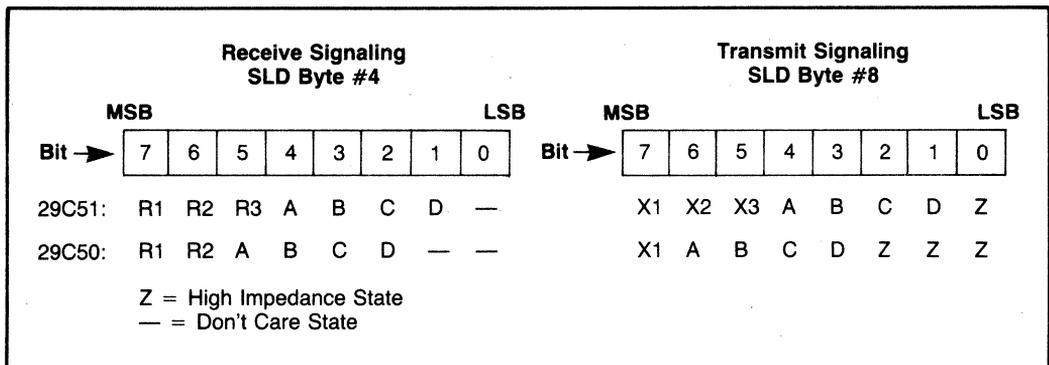
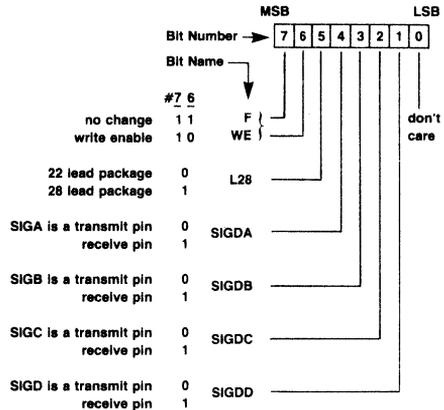


Figure 9. Signaling Field Format

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias -10°C to +80°C
 Storage Temperature -65°C to +150°C
 All Input and Output Voltages
 with Respect to V_{BB} -0.3V to 13V
 All Input and Output Voltages
 with Respect to V_{CC} -13V to 0.3V
 Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{BB} = -5v ± 5%; SCL (50% duty), SDIR, SLD applied GNDD = 0v, GNDA = 0V.) Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I _{IL}	Input Leakage Current	-0.3		± 10	µA	V _{BB} ≤ Vin ≤ V _{CC}
V _{IL}	Input Low Voltage			0.8	V	
V _{IH}	Input High Voltage	2.2		V _{CC} + .3	V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} ≥ -1.6mA, 1 TTL load
V _{OH}	Output High Voltage	2.4			V	I _{OH} ≤ 50µA, 1 TTL load

POWER DISSIPATION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I _{CCL}	V _{CC} Operating Current		9		mA	
I _{BBL}	V _{BB} Operating Current		9		mA	
I _{CCO}	V _{CC} Standby Current		0.8		mA	
I _{BBO}	V _{BB} Standby Current		0.8		mA	
P _{DO}	Standby Power Dissipation		8		mW	
P _{DI}	Operating Power Dissipation		90		mW	

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

(TG1 = TG2, Transmit Programmable Gain = 6dB; GSR = VFR -, Receive Programmable Gain = 0dB)

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response		± 0.1		dB	Signal input of 0dBm0 f = 1.02KHz
DmW	Digital Milliwatt Response		± 0.1		dB	f = 1.02KHz
DmW _{µV}	Digital Milliwatt Response VFR +, VFR -, µ-law		6.14		dBm	VFR + single-ended output R _L = 600Ω Receive input per CCITT G.711
DmW _{AV}	Digital Milliwatt Response VFR +, VFR -, A-law		6.17		dBm	
DMW _{µS}	Digital Milliwatt Response at SAO, µ-law		3.70		dBVrms	No load; no sin x/x correction
DmW _{AS}	Digital Milliwatt Response at SAO, A-law		3.73		dBVrms	No load; no sin x/x correction
OTLP _X	Zero Transmission Level Point Transmit Channel (0dBm0)		.788 .785		Vrms Vrms	A-law µ-law

GAIN TRACKING

Reference level = 0dBm0 for μ -law, -10 dBm0 A-law at 1.02KHz, TG1 = TG2, GSR = VFR-, Transmit Programmable Gain = 6dB, Receive Programmable Gain = 0dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
GT _T	Transmit Gain Tracking Error Sinusoidal Input; μ or A-law		$\pm .25$		dB	+3 to -40dBm0
			$\pm .50$		dB	-40 to -50dBm0
			± 1.2		dB	-50 to -55dBm0
GT _R	Receive Gain Tracking Error Sinusoidal Input; μ or A-law		$\pm .25$		dB	+3 to -40dBm0
			$\pm .50$		dB	-40 to -50dBm0
			± 1.2		dB	-50 to -55dBm0
						AT&T PUB43801 and CCITT G.712 — Method 2

ANALOG INTERFACE, RECEIVE PRIMARY AND SECONDARY CHANNELS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
R _{OR}	Output Resistance, VFR+ VFR-		1		Ω	
V _{OSR1}	Output Offset, VFR+ or VFR-, single ended		50		mV	Relative to GNDA
V _{OSR2}	Output Offset, VFR+ to VFR-, Differential		75		mV	
C _{LR}	Load Capacitance, VFR+, VFR-			100	pF	
V _{OR1}	Max Output Voltage Swing across R _L , VFR+, VFR-, single-ended connection	± 3.2			Vp	R _L \geq 300 Ω
V _{OR2}	Max Differential Output Voltage Swing, VFR+, VFR-	± 6.4			Vp	R _L \geq 600 Ω
P _{OR}	Differential Output Power, VFR+, VFR-			15.3	dBm	R _L = 600 Ω
R _{ORS}	Output Resistance, SAO		25		Ω	
V _{OSR}	Output Offset, SAO		50		mV	
C _{LRS}	Load Capacitance, SAO			20	pF	
R _{LRS}	Load Resistance, SAO	10			K Ω	
V _{ORS}	Output Voltage Swing SAO	± 3.2			Vp	R _L \geq 10K Ω

ANALOG INTERFACE, TRANSMIT PRIMARY AND SECONDARY CHANNELS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I _{BX}	Input Leakage Current, EBN1, EBN2, TG1		100		nA	-1.6V < VFX < 1.6V
R _{IX1}	Input Resistance, VFX		500		K Ω	-1.6V < VFX < 1.6V
R _{IX2}	Input Resistance, EBN1, EBN2, TG1		10		M Ω	-1.6V < VFX < 1.6V
CMRR _S	Common Mode Rejection, SAI1, SAI2		40		dB	Differential SAI conversion
TGmax	Max Transmit Gain Adjust			20	dB	
V _{OTG}	Max Output Voltage Swing TG2	± 1.6			v	R _L \geq 10K Ω
C _{LX}	Load Capacitance, TG2			20	pF	
R _{LX}	Load Resistance, TG2	10			K Ω	

DISTORTION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
SD _X , SD _R	Signal to Distortion, μ or A-law Sinusoidal input; CCITT G.712 — Method 2 Half Channel	35 29 25			dB dB dB	0 to -30dBm0 -30 to -40dBm0 -40 to -45dBm0
DP _X , DP _R	Single Frequency Distortion Products In Band (2nd or 3rd Harmonic Half Channel)		-50	-47	dB	Input = 1.02kHz 0dBm0 AT&T Advisory #64 (3.8)
IMD ₁	Intermodulation Distortion, End to End Measurement			-40	dBm0	CCITT G.712(7.1)
IMD ₂	Intermodulation Distortion, End to End Measurement			-50	dBm0	CCITT G.712(7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			-27	dBm0	CCITT G.712(6.1)
SIS	Spurious In Band Signals, End to End Measurement			-40	dBm0	CCITT G.712(9)
D _{AX}	Transmit Absolute Delay		180		μ s	0dBm0, 1.02kHz Includes delay through A/D
D _{DX}	Transmit Differential Envelope Delay; Relative to minimum envelope delay (1.4kHz)		170 95 45 105		μ s μ s μ s μ s	f = 500-600 Hz f = 600-1000 Hz f = 1000-2600 Hz f = 2600-2800 Hz
D _{AR}	Receive Absolute Delay		125		μ s	0dBm0, 1.02kHz Includes delay through D/A
D _{DR}	Receive Differential Envelope Delay; Relative to minimum envelope delay (300 Hz)		45 35 85 110		μ s μ s μ s μ s	f = 500-600 Hz f = 600-1000 Hz f = 1000-2600 Hz f = 2600-2800 Hz

NOISE (Primary Channel)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
N _{XC1}	Transmit Noise, C-Message Weighted		12		dBrnC0	Transmit Gain Adjust = 0dB
N _{XP1}	Transmit Noise, Psophometrically Weighted		-78		dBm0p	Transmit Gain Adjust = 0dB
N _{RC1}	Receive Noise, C-Message Weighted		10		dBrnC0	Unity Gain; Idle Code
N _{RP1}	Receive Noise, Psophometrically Weighted		-80		dBm0p	Unity Gain; Idle Code
PSRR ₁	V _{CC} Power Supply Rejection, Transmit Channel		-35		dB	Idle channel; 200mV P-P signal on supply DC to 50 KHz; Note 1.
PSRR ₂	V _{BB} Power Supply Rejection Transmit Channel		-30		dB	Idle Channel; 200mV P-P signal on supply DC to 50 KHz; Note 1.
PSRR ₃	V _{CC} Power Supply Rejection, Receive Channel		-35		dB	Idle channel, 200mV P-P signal on supply DC to 50 KHz; Note 1.
PSRR ₄	V _{BB} Power Supply Rejection Receive Channel		-30		dB	Idle channel, 200mV P-P signal on supply DC to 50 KHz; Note 1.

CROSSTALK

Symbol	Parameter	Min	Type	Max	Units	Test Conditions
CT _{TR}	Crosstalk, Transmit Primary Voice to Receive Primary Voice		-75		dB	Input = 0dBm0, unity gain 1.02KHz; idle code on SLD voice and data bytes
CT _{RT}	Crosstalk, Receive Primary Voice to Transmit Primary Voice		-75		dB	0dBm0, 1.02 KHz signal at SLD receive voice byte; VFX = GNDA; secondary channels off
CT _{ST}	Crosstalk, Transmit Secondary Channels to Transmit Primary Voice		-70		dB	SAI = 0dBm0, 1.02 KHz; VFX = GNDA idle code on SLD voice and data bytes
CT _{SR}	Crosstalk, Receive Secondary Channel to Receive Primary Voice		-70		dB	0dBm0, 1.02 KHz at SLD data byte VFX = SAI = GNDA

NOTES:

1. Measured at SLD Voice bytes for transmit channel. Measured at V_{FR+} for receive channel.

TRANSMIT VOICE FREQUENCY CHARACTERISTICS

TG1 = TG2, Transmit Programmable Gain = 6dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02kHz					0dBm0 Signal Input at VFX
	16.67Hz			-30	dB	
	50Hz			-25	dB	
	60Hz			-22	dB	
	200Hz	-1.8		-0.125	dB	
	300 to 3000Hz	-0.125		+0.125	dB	
	3300Hz	-0.35		+0.03	dB	
	3400Hz	-0.70		-0.10	dB	
	4600Hz and Above			-32	dB	
ΔG_{PX}	Programmable Gain Accuracy (Commulative Error)		$\pm .25$		dB	freq. = 1.02kHz for all steps

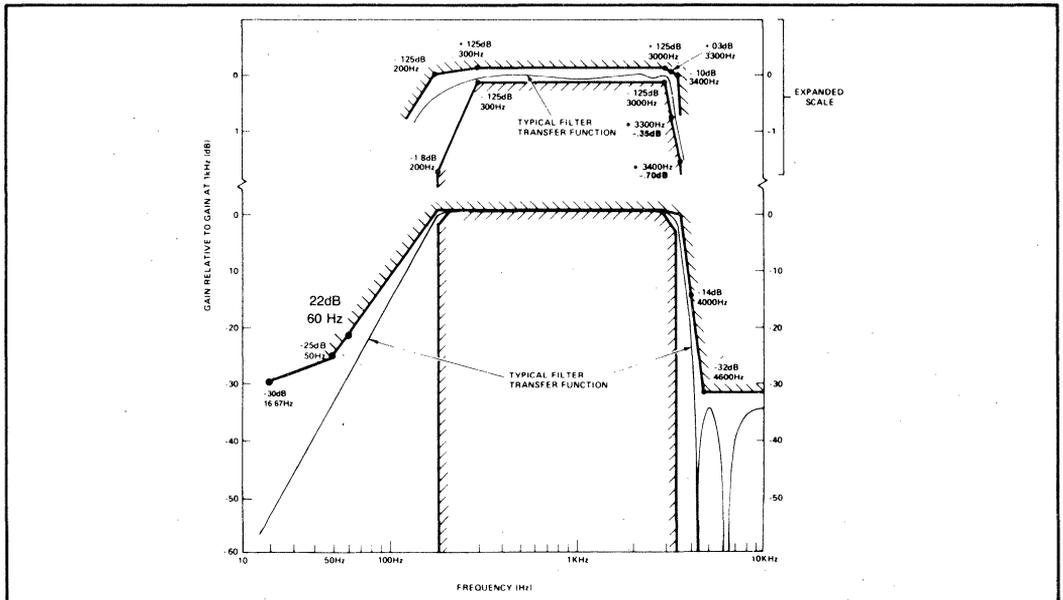


Figure 10. Transmit Voice Frequency Characteristics

RECEIVE VOICE FREQUENCY CHARACTERISTICS

GSR = VFR-, Receive Programmable Gain = 0dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G _{RR}	Gain Relative to gain at 1.02kHz					0dBm0 input on SLD
	Below 200Hz			+ 0.125	dB	
	200Hz	- 0.5		+ 0.125	dB	
	300 to 3000Hz	- 0.125		+ 0.125	dB	
	3300Hz	- 0.35		+ 0.03	dB	
	3400Hz	- 0.70		- 0.1	dB	
	4000Hz 4600Hz & Above			- 14 - 30	dB dB	
ΔG _{PR}	Programmable Gain Accuracy (Commulative Error)		+ .25		dB	f = 1.02kHz all steps

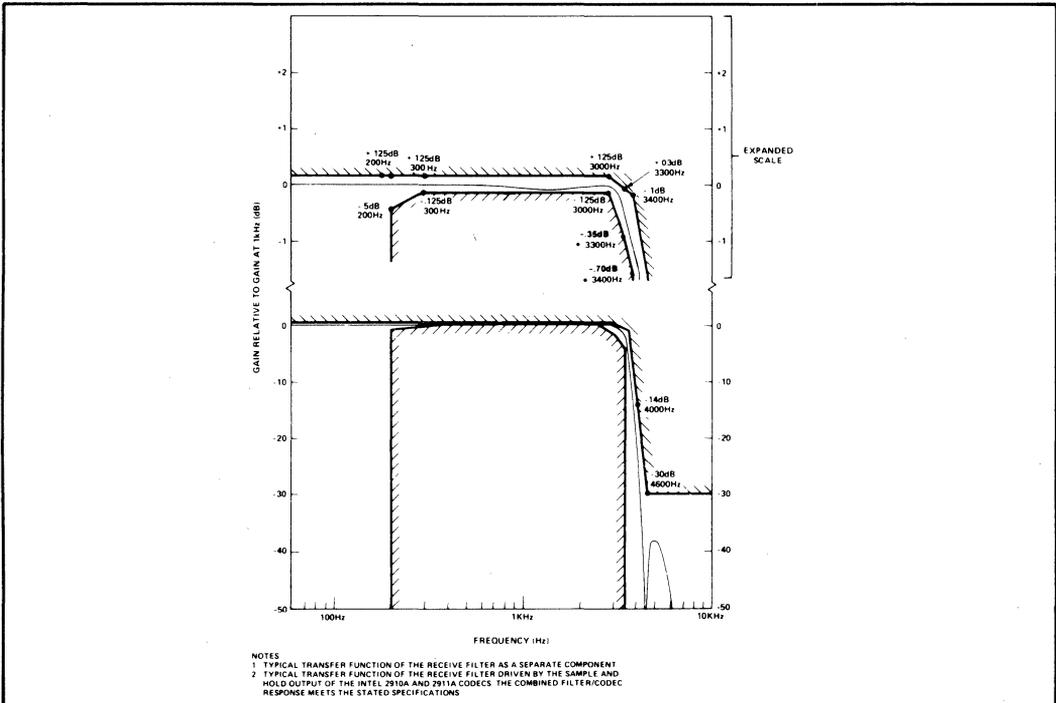


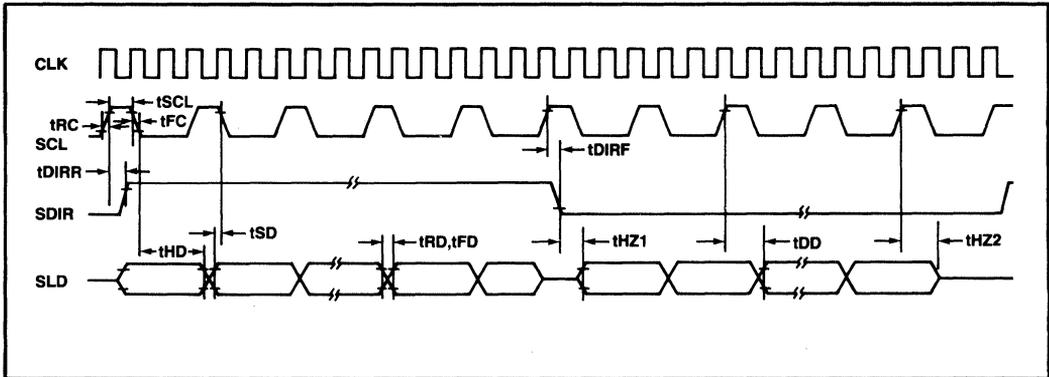
Figure 11. Receive Voice Frequency Characteristics

A.C. CHARACTERISTICS — TIMING PARAMETERS

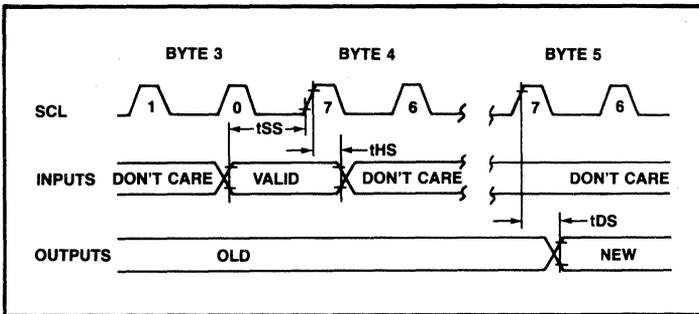
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
T _{DC}	SCL Duty Cycle	28 45	33 50	38 55	% %	2952 CLK Clock = 1.544 or 1.536MHz 2952 CLK CLock ≥ 2.048MHz
t _{RC} T _{FC}	Rise, Fall Times, SCL			50	ns	
T _{RD} T _{FD}	Rise, Fall Times, SLD			50	ns	
T _{DIRR}	SCL to SDIR Delay	- 100		100	ns	
T _{DIRF}	SCL to SDIR Delay	- 100		+ 420	ns	
T _{DD}	SCL to SLD Delay	0		200	ns	29C51 Transmitting*
T _{SD}	Set-up Time, SLD to SCL	100			ns	2952 Transmitting
T _{HD}	Hold Time, SCL to SLD	100			ns	
T _{HZ1}	SDIR to SLD Active	0		100	ns	Byte 1, Bit 1 29C51 Transmitting
T _{HZ2}	SCL to SLD High Impedence	0		100	ns	After last SIGX bit
T _{SS}	Set-up time, signaling inputs to SLD Byte #4, Bit 7	1			μs	
T _{HS}	Hold time, SLD Byte 4 Bit 7 for all signaling inputs	1			μs	
T _{DS}	Delay SLD Byte 5 to signaling outputs			1	μs	

*In cases where the T_{DIF} is positive, T_{DD} is to be measured from the SDIR edge.

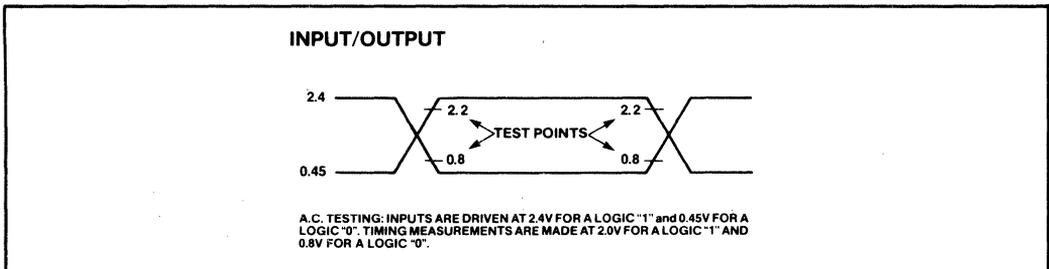
TIMING PARAMETERS (CLK = 1.544 MHz, 33% duty cycle)



SIGNALING TIMING



A.C. TESTING INPUT, OUTPUT WAVEFORM



29C13 AND 29C14 CHMOS COMBINED SINGLE-CHIP PCM CODEC AND FILTER

- 29C14 Asynchronous clocks, 8th bit signaling, loop back test capability
- 29C13 Synchronous clocks only, 300 mil package
- Low-Power Pin Compatible Version of Intel's 2913 and 2914
- AT&T D3/D4 and CCITT Compatible
- 28-Pin Plastic Leaded Chip Carrier (PLCC) for Higher Integration
- 3 Low-Power Modes
 - 5 mW Typical Power Down
 - 8 mW Typical Standby
 - 70 mW Typical Operating
- Direct Interface with Transformer or Electronic Hybrids
- TTL and CMOS Compatible

Intel's 29C13 and 29C14 are CHMOS versions of Intel's HMOS 2913 and 2914 family members. CHMOS is a technology built on HMOS-II, thus realizing the high performance and density obtained in that process while achieving the low power consumption typical of CMOS circuits.

The 29C13 and 29C14 retain all the features of the 2913 and 2914: push/pull power amplifiers, μ A law pin select, on-chip auto zero, sample and hold and precision voltage references, power up clear and tri-state on clock interrupt, two timing modes and two power down modes.

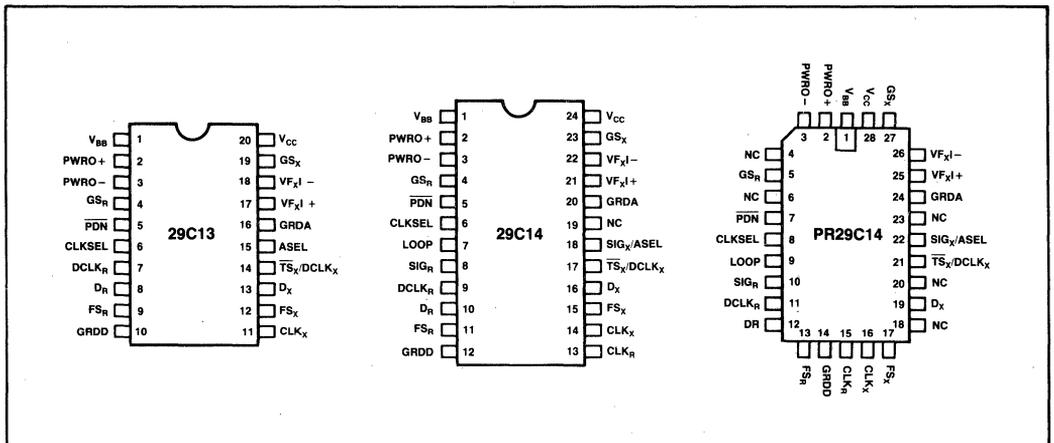


Figure 1. Pin Configurations

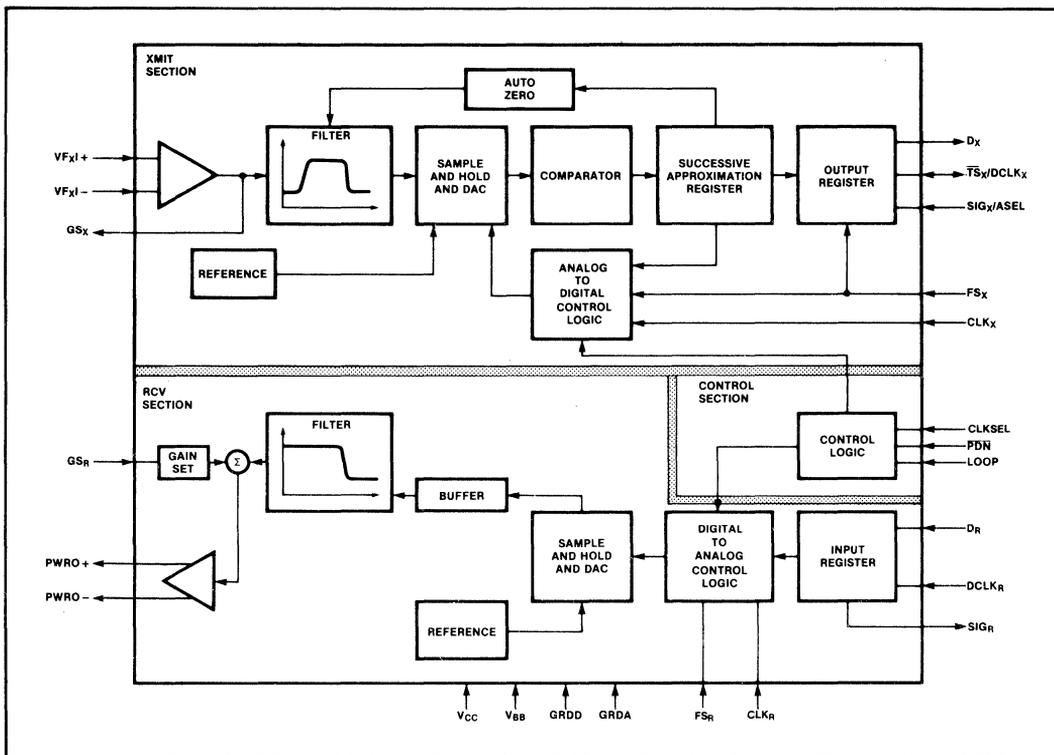


Figure 2. Block Diagram

Table 1. Pin Names

V _{BB}	Power (-5V)	GS _x	Transmit Gain Control
PWRO+, PWRO-	Power Amplifier Outputs	VFXI-, VFXI+	Analog Inputs
GS _r	Receive Gain Control	GRDA	Analog Ground
PDN	Power Down Select	NC	No Connect
CLKSEL	Master Clock Frequency Select	SIG _x	Transmit Signaling Input
LOOP	Analog Loop Back	ASEL	μ- or A-law Select
SIG _r	Receive Signaling Bit Output	TS _x	Timeslot Strobe/Buffer Enable
DCLK _r	Receive Variable Data Clock	DCLK _x	Transmit Variable Data Clock
D _r	Receive PCM Input	D _x	Transmit PCM Output
FS _r	Receive Frame Synchronization Clock	FS _x	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK _x	Transmit Master Clock
V _{CC}	Power (+5V)	CLK _r	Receive Master Clock (29C14 only, internally connected to CLK _x on 29C13)

Table 2. Pin Description

Symbol	Function
V _{BB}	Most negative supply; input voltage is -5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO-	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
GS _R	Input to the gain setting network on the output power amplifier. Transmission level can be adjusted over a 12dB range depending on the voltage at GS _R .
PDN	Power down select. When PDN is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK _X , CLK _R . CLKSEL = V _{BB} 2.048 MHz CLKSEL = GRDD 1.544 MHz CLKSEL = V _{CC} 1.536 MHz
LOOP	Analog loopback. When this pin is TTL high, the analog output (PWRO+) is internally connected to the analog input (VF _X I+), GS _R is internally connected to PWRO-, and VF _X I- is internally connected to GS _X . A 0dBm0 digital signal input at D _R is returned as a +3dBm0 digital signal output at D _X .
SIG _R	Signaling bit output, receive channel. In fixed data rate mode, SIG _R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
DCLK _R	Selects the fixed or variable data rate mode. When DCLK _R is connected to V _{BB} , the fixed data rate mode is selected. In this mode, the device is fully compatible with Intel 2910A and 2911A direct mode timing. When DCLK _R is not connected to V _{BB} , the device operates in the variable data rate mode. In this mode DCLK _R becomes the receive data clock which operates at TTL levels from 64Kb to 2.048 Mb data rates.
D _R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK _R in the fixed data rate mode and DCLK _R in variable data rate mode.
FS _R	8KHz frame synchronization clock input/ timeslot enable, receive channel. A multi-function input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS _R is TTL low for 300 milliseconds.

Symbol	Function
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK _R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK _X	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS _X	8 KHz frame synchronization clock input/ timeslot enable, transmit channel. Operates independently but in an analogous manner to FS _R . The transmit channel enters the standby state whenever FS _X is TTL low for 300 milliseconds.
D _X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock; CLK _X in fixed data rate mode and DCLK _X in variable data rate mode.
TS _X /DCLK _X	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer as in 2910A and 2911A direct mode timing. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64Kb to 2.048 Mb data rates.
SIG _X /ASEL	A dual purpose pin. When connected to V _{BB} , A-law operation is selected. When it is not connected to V _{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D _X lead. If not used as an input pin, ASEL should be strapped to either V _{CC} or GRDD.
NC	No connect
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF _X I+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF _X I-	Inverting analog input to uncommitted transmit operational amplifier.
GS _X	Output terminal of transmit input channel op amp. Internally, this is the voice signal input to the transmit filter.
V _{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 2913 and 2914 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line or trunk.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

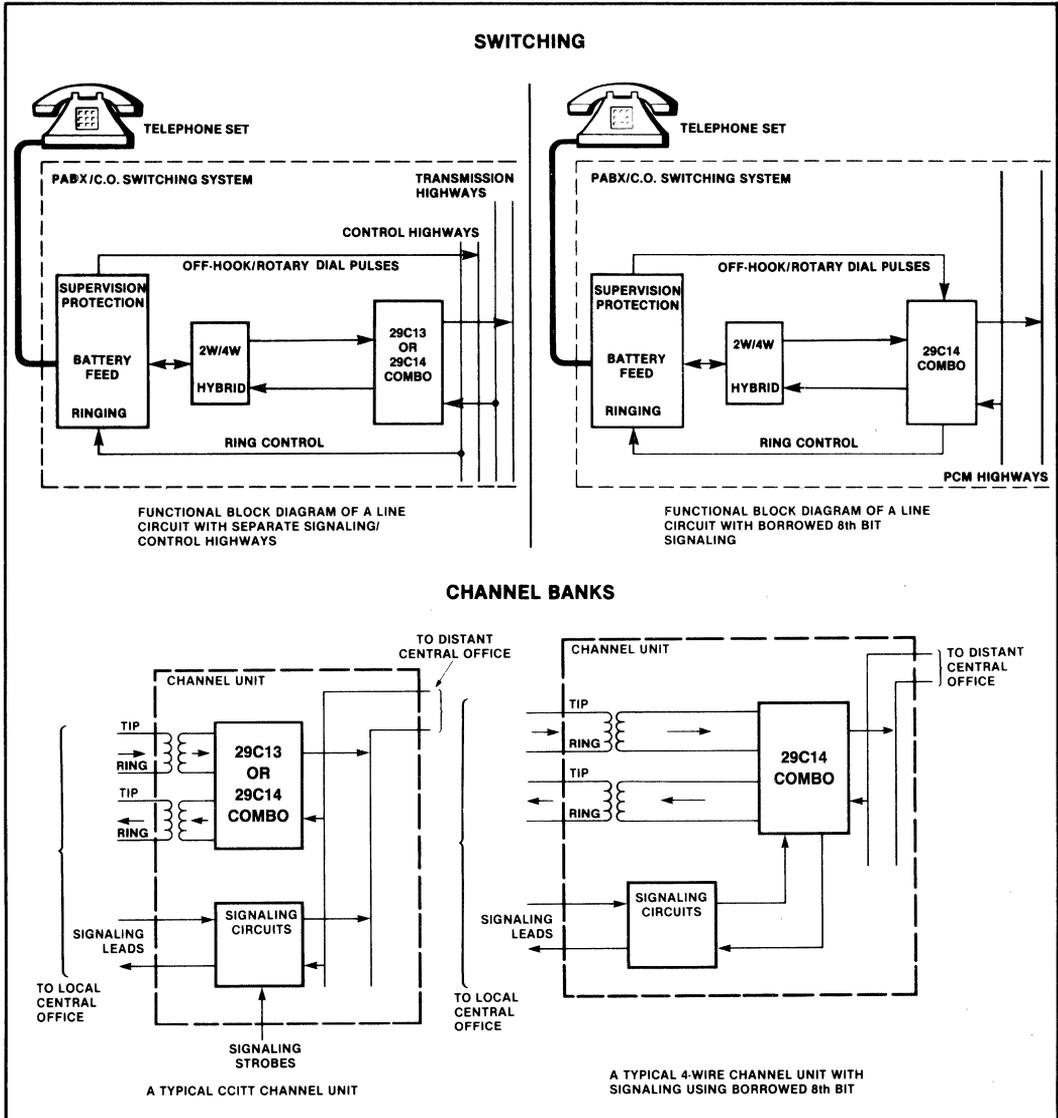


Figure 3. Typical Line Terminations

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to \overline{PDN} , provided that all clocks and supplies are connected. The 29C13 and 29C14 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and \overline{TS}_X are held in a high impedance state for approximately four frames (500 μ s) after power up or application of V_{BB} or V_{CC} . After this delay, D_X , \overline{TS}_X , and signaling will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the autozero circuit settling time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC} . SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, \overline{TS}_X and D_X will be placed in a high impedance state approximately 30 μ s after an interruption of CLK_X . Similarly, SIG_R will be held low approximately 30 μ s after an interruption of CLK_R . These interruptions could possibly occur with some kind of fault condition.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 29C13/C14 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up

the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the \overline{PDN} pin. In this mode, power consumption is reduced to the value shown in Table 3. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the \overline{PDN} pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R . With both channels in the standby state, power consumption is reduced to the value shown in Table 3. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A compatible, is selected by connecting $DCLK_R$ to V_{BB} . It employs master clocks CLK_X and CLK_R , frame synchronization clocks FS_X and FS_R , and output \overline{TS}_X .

CLK_X and CLK_R serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. \overline{TS}_X is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN} = \text{TTL low}$	5 mW	\overline{TS}_X and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10 μ s
Standby Mode	FS_X and FS_R are TTL low	8 mW	\overline{TS}_X and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state 300 milliseconds after FS_X and FS_R are removed.
Only transmit is on standby	FS_X is TTL low	50 mW	\overline{TS}_X and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FS_R is TTL low	50 mW	SIG_R is placed in a TTL low state within 300 milliseconds.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X . Similarly, on the receive side, data is received on the first eight falling edges of CLK_R . The frequency of CLK_X and CLK_R is selected by the $CLKSEL$ pin to be either 1.536, 1.544, or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB} . It employs master clocks CLK_X and CLK_R , bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X .

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the 29C14, synchronous in the case of the 29C13, from 64 kHz to 2.048 MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the $125\mu s$ frame as long

as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

Signaling

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode ($DCLK_R = V_{BB}$). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG_X for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG_R lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in Figure 4.

Asynchronous Operation

The 29C14 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special interrupt circuitry, the design of the Intel 29C13/C14 combochip includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow independent operation of the two channels.

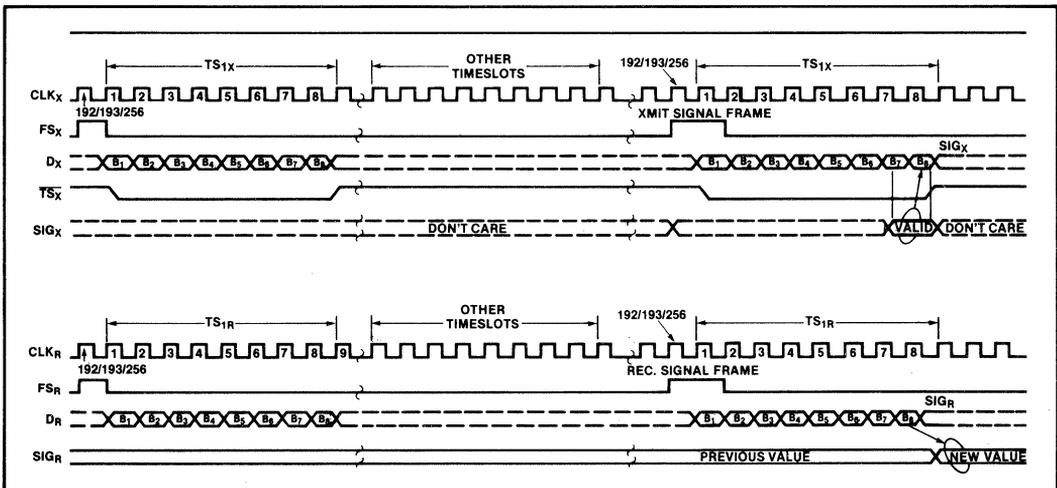


Figure 4. Signaling Timing (Used Only with Fixed Data Rate Mode)

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. CLK_X and $DCLK_X$ are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (refer to Variable Data Rate Timing Diagrams). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

Analog Loopback

A distinctive feature of the 29C14 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in Figure 5, when LOOP is TTL high the analog output ($PWRO+$) is internally connected to the analog input (VF_XI+), GS_R is internally connected to $PWRO-$, and VF_XI- is internally connected to GS_X .

With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel (D_R) with those generated on the transmit channel (D_X). Due to the difference in transmission levels between the transmit and receive sides, a 0 dBm0 code sent into D_R will emerge from D_X as a +3dBm0 code, an implicit gain of 3 dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are cali-

brated during the manufacturing process. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve the extremely accurate Digital Milliwatt Responses specified in the TRANSMISSION PARAMETERS, providing the user a significant margin for error in other board components.

Conversion Laws

The 29C13 and 29C14 are designed to operate in both μ -law and A-law systems. The user can select either conversion law according to the voltage present on the $SIG_X/ASEL$ pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for μ -law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB} . Thus, signaling is not allowed during A-law operation. If $\mu = 255$ -law operation is selected, then SIG_X is a TTL level input which modifies the LSB of the PCM output in signaling frames.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of ± 2.17 volts, a DC offset of 25 mV, and a typical voltage gain of 20,000. Gain of

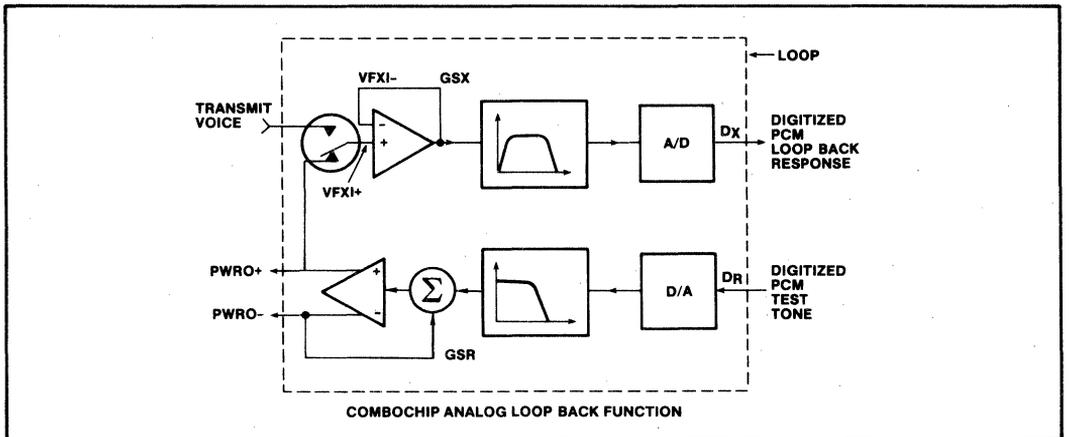


Figure 5. Simplified Block Diagram of 29C14 Combochip in the Analog Loopback Configuration

up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_x) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_xI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see Figure 6).

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The 29C13 and 29C14 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 8.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

Encoding

The encoder internally samples the output of the

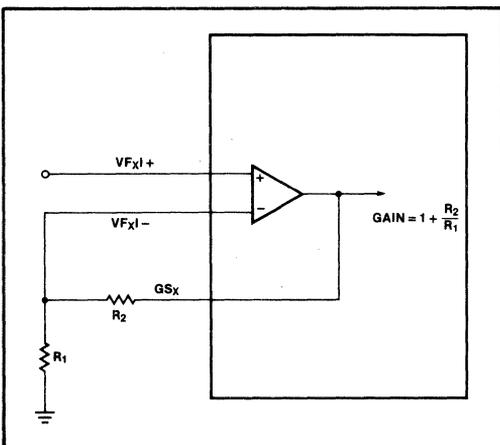


Figure 6. Transmit Filter Gain Adjustment

transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the $(\sin x)/x$ response of such decoders. The receive filter characteristics and specifications are shown in Figure 9.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended or 600 ohms differentially.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO-, the receive level is unattenuated; when it is tied to PWRO+, the level is attenuated by 12 dB. The output transmission level interpolates between 0 and -12 dB as GS_R is interpolated (with a potentiometer) between PWRO+ and PWRO-. The use of the output gain set is illustrated in Figure 7.

Transmission levels are specified relative to the re-

Table 4. Zero Transmission Level Points

Symbol	Parameter	Value	Units	Test Conditions
0TLP1 _x	Zero Transmission Level Point Transmit Channel (0dBm0) μ -law	+2.76 +1.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP2 _x	Zero Transmission Level Point Transmit Channel (0dBm0) A-law	+2.79 +1.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP1 _r	Zero Transmission Level Point Receive Channel (0dBm0) μ -law	+5.76 +4.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP2 _r	Zero Transmission Level Point Receive Channel (0dBm0) A-law	+5.79 +4.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω

ceive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

OUTPUT GAIN SET: DESIGN CONSIDERATIONS

(Refer to Figure 7.)

PWRO+ and PWRO- are low impedance complementary outputs. The voltages at the nodes are:

- Vo+ at PWRO+
- Vo- at PWRO-
- Vo = (Vo+) - (Vo-)(total differential response)

R₁ and R₂ are a gain setting resistor network with the center tap connected to the GS_R input.

A value greater than 10K ohms for R₁ + R₂ and less than 100K ohms for R₁ in parallel with R₂ is recommended because:

- (a) The parallel combination of R₁ + R₂ and R_L sets the total loading.
- (b) The total capacitance at the GS_R input and the parallel combination of R₁ and R₂ define a time constant which has to be minimized to avoid inaccuracies.

A is the gain of the power amplifiers,

$$\text{where } A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$$

For design purposes, a useful form is R₁/R₂ as a function of A.

$$R_1/R_2 = \frac{4A - 1}{1 - A}$$

(Allowable values for A are those which make R₁/R₂ positive.)

Examples are:

If A = 1 (maximum output), then

R₁/R₂ = ∞ or V(GS_R) = Vo-; i.e., GS_R is tied to PWRO-

If A = 1/2, then

$$R_1/R_2 = 2$$

If A = 1/4, (minimum output) then

R₁/R₂ = 0 or V(GS_R) = Vo+; i.e., GS_R is tied to PWRO+

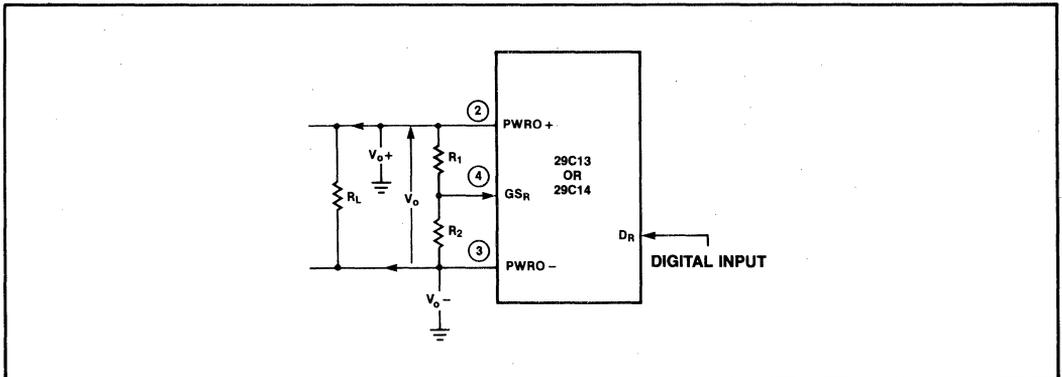


Figure 7. Gain Setting Configuration

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias -10°C to +80°C
 Storage Temperature -65°C to +150°C
 V_{CC} and GRDD with Respect to V_{BB} -0.3V to 15V
 All Input and Output Voltages
 with Respect to V_{BB} -0.3V to 15V
 All Input and Output Voltages
 with Respect to V_{CC} -15V to +0.3V
 Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified)
 Typical values are for $T_A = 25^\circ\text{C}$ and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	μA	$\text{GRDD} \leq V_{IN} \leq V_{IL}$ (Note 1)
I_{IH}	High Level Input Current			10	μA	$V_{IH} \leq V_{IN} \leq V_{CC}$
V_{IL}	Input Low Voltage, except CLKSEL			0.8	V	
V_{IH}	Input High Voltage, except CLKSEL	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 3.2 \text{ mA}$ at D_X , $\overline{\text{TS}}_X$ and SIG_R
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = 80 \mu\text{A}$ at D_X , SIG_R $I_{OH} = 1.2 \text{ mA}$ at SIG_R
V_{ILO}	Input Low Voltage, CLKSEL ²	V_{BB}		$V_{BB} + 0.5$	V	
V_{IIO}	Input intermediate Voltage, CLKSEL	GRDD - 0.5		0.5	V	
V_{IHO}	Input High Voltage, CLKSEL	$V_{CC} - 0.5$		V_{CC}	V	
C_{OX}	Digital Output Capacitance ³		5		pF	
C_{IN}	Digital Input Capacitance		5	10	pF	

POWER DISSIPATION

All measurements made at $f_{DCLK} = 2.048 \text{ MHz}$, outputs unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC1}	V_{CC} Operating Current		6.8		mA	
I_{BB1}	V_{BB} Operating Current		7.2		mA	
I_{CC0}	V_{CC} Power Down Current		0.5		mA	$\overline{\text{PDN}} \leq V_{IL}$; after 10 μs
I_{BB0}	V_{BB} Power Down Current		0.5		mA	$\overline{\text{PDN}} \leq V_{IL}$; after 10 μs
I_{CCS}	V_{CC} Standby Current		0.8		mA	$\text{FS}_X, \text{FS}_R \leq V_{IL}$; after 300 ms
I_{BBS}	V_{BB} Standby Current		0.8		mA	$\text{FS}_X, \text{FS}_R \leq V_{IL}$; after 300 ms
P_{D1}	Operating Power Dissipation ⁴		70		mW	
P_{D0}	Power Down Dissipation ⁴		5		mW	$\overline{\text{PDN}} \leq V_{IL}$; after 10 μs
P_{ST}	Standby Power Dissipation ⁴		8		mW	$\text{FS}_X, \text{FS}_R \leq V_{IL}$

NOTES:

- V_{IN} is the voltage on any digital pin.
- SIG_X and DCLK_R are TTL level inputs between GRDD and V_{CC} ; they are also pinstraps for mode selection when tied to V_{BB} . Under these conditions V_{ILO} is the input low voltage requirement.
- Timing parameters are guaranteed based on a 100 pf load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pf.
- With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, V_{FX1+} , V_{FX1-}			100	nA	$-2.17V \leq V_{IN} \leq 2.17V$
R_{IX1}	Input Resistance, V_{FX1+} , V_{FX1-}	10			M Ω	
V_{OSXI}	Input Offset Voltage, V_{FX1+} , V_{FX1-}			25	mV	
CMRR	Common Mode Rejection, V_{FX1+} , V_{FX1-}	55			dB	$-2.17 \leq V_{IN} \leq 2.17V$
A_{VOL}	DC Open Loop Voltage Gain, GS_X	5000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		300		KHz	
C_{LXI}	Load Capacitance, GS_X			50	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			k Ω	

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, $PWRO+$, $PWRO-$		1		Ω	
V_{OSRA}	Single-Ended Output DC Offset, $PWRO+$, $PWRO-$		75	± 150	mV	Relative to GRDA
C_{LRA}	Load Capacitance, $PWRO+$, $PWRO-$			100	pF	

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm₀, 1020 Hz sine wave.¹ Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm₀, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration.² All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response (Transmit gain tolerance)	-0.18	± 0.04	+0.18	dBm ₀	Signal input of 1.064 V _{rms} μ -law Signal input of 1.068 V _{rms} A-law $T_A = 25^\circ C$, $V_{BB} = -5V$, $V_{CC} = +5V$
EmW _{TS}	EmW variation with Temperature and supplies	-0.07	± 0.02	+0.12	dB	$\pm 5\%$ supplies, 0 to 70°C Relative to nominal conditions
DmW	Digital Milliwatt Response (Receive gain tolerance)	-0.18	± 0.04	+0.18	dBm ₀	Measure relative to 0TLP _R . Signal input per CCITT Recommendation G.711. Output signal of 1000 Hz. $T_A = 25^\circ C$; $V_{BB} = -5V$, $V_{CC} = +5V$.
DmW _{TS}	DmW variation with temperature and supplies	-0.07	± 0.02	+0.07	dB	$\pm 5\%$ supplies, 0 to 70°C

NOTES:

- 0dBm₀ is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 volts rms or an output of 1.503 volts rms for μ law.
- Unity gain input amplifier: GS_X is connected to V_{FX1-} , Signal input V_{FX1+} ; Maximum gain output amplifier; GS_R is connected to $PWRO-$, output to $PWRO+$.

GAIN TRACKING

Reference Level = -10dBm0

Symbol	Parameter	Min	Max	Unit	Test Conditions
GT1 _x	Transmit Gain Tracking Error Sinusoidal Input; μ -law		± 0.25 ± 0.5 ± 1.2	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, $R_L = 300\Omega$
GT2 _x	Transmit Gain Tracking Error Sinusoidal Input; A-law		± 0.25 ± 0.5 ± 1.2	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, $R_L = 300\Omega$
GT1 _R	Receive Gain Tracking Error Sinusoidal Input; μ -law		± 0.25 ± 0.5 ± 1.2	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, $R_L = 300\Omega$
GT2 _R	Receive Gain Tracking Error Sinusoidal Input; A-law		± 0.25 ± 0.5 ± 1.2	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, $R_L = 300\Omega$

NOISE (All receive channel measurements are single ended)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
N _{XC1}	Transmit Noise, C-Message Weighted			15	dBrc0	$V_{F_X +} = GRDA, V_{F_X -} = GS_X$
N _{XC2}	Transmit Noise, C-Message Weighted with Eighth Bit Signaling			18	dBrc0	$V_{F_X +} = GRDA, V_{F_X -} = GS_X$; 6th frame signaling
N _{XP}	Transmit Noise, Psophometrically Weighted			-75	dBm0p	$V_{F_X +} = GRDA, V_{F_X -} = GS_X$
N _{RC1}	Receive Noise, C-Message Weighted: Quiet Code			11	dBrc0	$D_R = 11111111$
N _{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle			12	dBrc0	Input to D_R is zero code with sign bit toggle at 1 kHz rate
N _{RP}	Receive Noise, Psophometrically Weighted			-79	dBm0p	$D_R =$ lowest positive decode level
N _{SF}	Single Frequency Noise End to End Measurement			-50	dBm0	CCITT G.712.4.2 Measure at PWRO+
PSRR ₁	V_{CC} Power Supply Rejection, Transmit Channel		-30		dB	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D_X
PSRR ₂	V_{BB} Power Supply Rejection, Transmit Channel		-30		dB	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D_X
PSRR ₃	V_{CC} Power Supply Rejection, Receive Channel		-25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+, 0 to 50 kHz
PSRR ₄	V_{BB} Power Supply Rejection, Receive Channel		-25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+, 0 to 50 kHz
CT _{TR}	Crosstalk, Transmit to Receive			-71	dB	$V_{F_X +} = 0dBm0, 1.02$ kHz, $D_R =$ lowest positive decode level, measure at PWRO+
CT _{RT}	Crosstalk, Receive to Transmit			-71	dB	$D_R = 0dBm0, 1.02$ kHz, $V_{F_X +} = GRDA$, measure at D_X

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SD1 _X	Transmit Signal to Distortion, μ -Law Sinusoidal Input; CCITT G.712-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD2 _X	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD1 _R	Receive Signal to Distortion, μ -Law Sinusoidal Input; CCITT G.712-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD2 _R	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
DP _X	Transmit Single Frequency Distortion Products			-46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP _R	Receive Single Frequency Distortion Products			-46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD ₁	Intermodulation Distortion, End to End Measurement			-35	dB	CCITT G.712 (7.1)
IMD ₂	Intermodulation Distortion, End to End Measurement			-49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			-25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			-40	dBm0	CCITT G. 712 (9)
D _{AX}	Transmit Absolute Delay		245		μ s	Fixed Data Rate. CLK _X = 2.048 MHz; 0 dBm0, 1.02 kHz signal at VF _{X1} + .. Measure at D _X .
D _{DX}	Transmit Differential Envelope Delay Relative to D _{AX}		170		μ s	f = 500 - 600 Hz
			95		μ s	f = 600 - 1000 Hz
			45		μ s	f = 1000 - 2600 Hz
			105		μ s	f = 2600 - 2800 Hz
D _{AR}	Receive Absolute Delay		190		μ s	Fixed Data Rate, CLK _R = 2.048 MHz; Digital input is DMW codes. Measure at PWRO +.
D _{DR}	Receive Differential Envelope Delay Relative to D _{AR}		45		μ s	f = 500 - 600 Hz
			35		μ s	f = 600 - 1000 Hz
			85		μ s	f = 1000 - 2600 Hz
			110		μ s	f = 2600 - 2800 Hz

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, noninverting; maximum gain output.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at $V_{FX}I+$
	16.67 Hz			-30	dB	
	50 Hz			-25	dB	
	60 Hz			-23	dB	
	200 Hz	-1.8		-0.125	dB	
	300 to 3000 Hz	-0.125		+ 0.125	dB	
	3300 Hz	-0.35		+ 0.03	dB	
	3400 Hz	-0.7		-0.10	dB	
	4000 Hz			-14	dB	
	4600 Hz and Above			-32	dB	

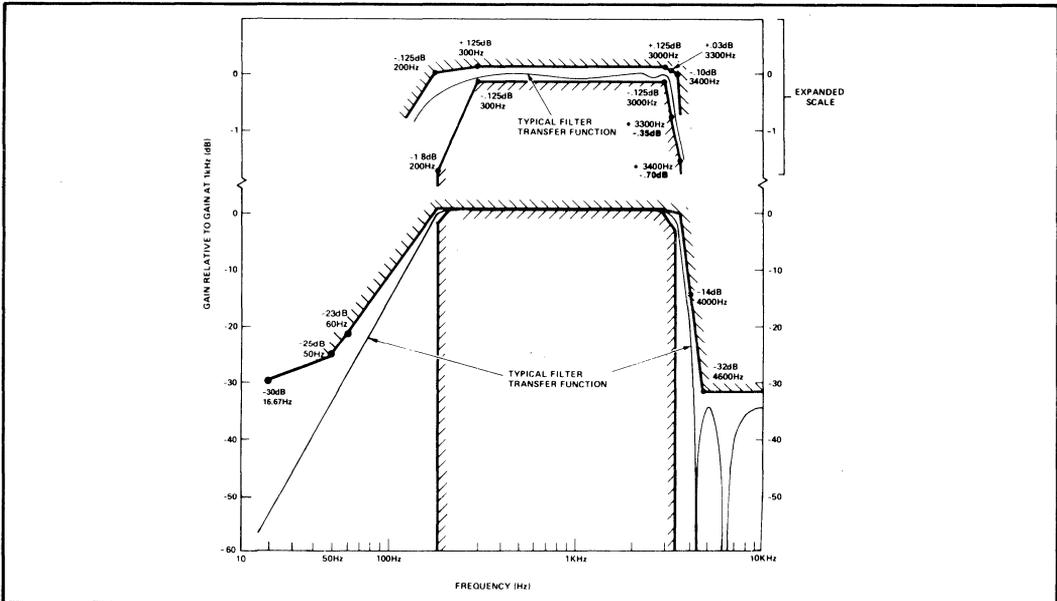


Figure 8. Transmit Channel

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at D_R
	Below 200 Hz			+0.125	dB	
	200 Hz	-0.5		+0.125	dB	
	300 to 3000 Hz	-0.125		+0.125	dB	
	3300 Hz	-0.35		+0.03	dB	
	3400 Hz	-0.7		-0.1	dB	
	4000 Hz			-14	dB	
	4600 Hz and Above			-30	dB	

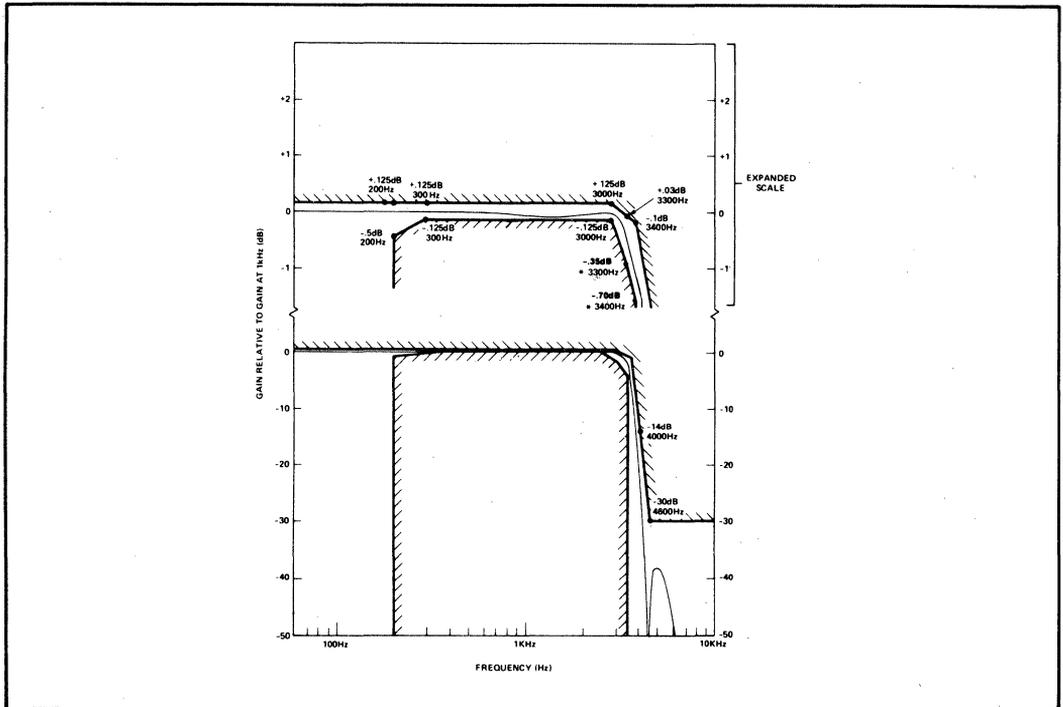


Figure 9. Receive Channel

A.C. CHARACTERISTICS — TIMING PARAMETERS
CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CY}	Clock Period, CLK_X , CLK_R	488			ns	$f_{CLKX} = f_{CLKR} = 2.048$ MHz
t_{CLK}	Clock Pulse Width, CLK_X , CLK_R	220			ns	
t_{DCLK}	Data Clock Pulse Width	220			ns	64 kHz $\leq f_{DCLK} \leq 2.048$ MHz
t_{CDC}	Clock Duty Cycle, CLK_X , CLK_R	45	50	55	%	
t_r , t_f	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE¹

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DZX}	Data Enabled on TS Entry	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{DDX}	Data Delay from CLK_X	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{HZX}	Data Float on TS Exit	60		215	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{SOFF}	Timeslot X to Disable	60		190	ns	$C_{LOAD} = 0$
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	
t_{SS}	Signal Setup Time	0			ns	
t_{SH}	Signal Hold Time	0			ns	

RECEIVE SECTION, FIXED DATA RATE MODE

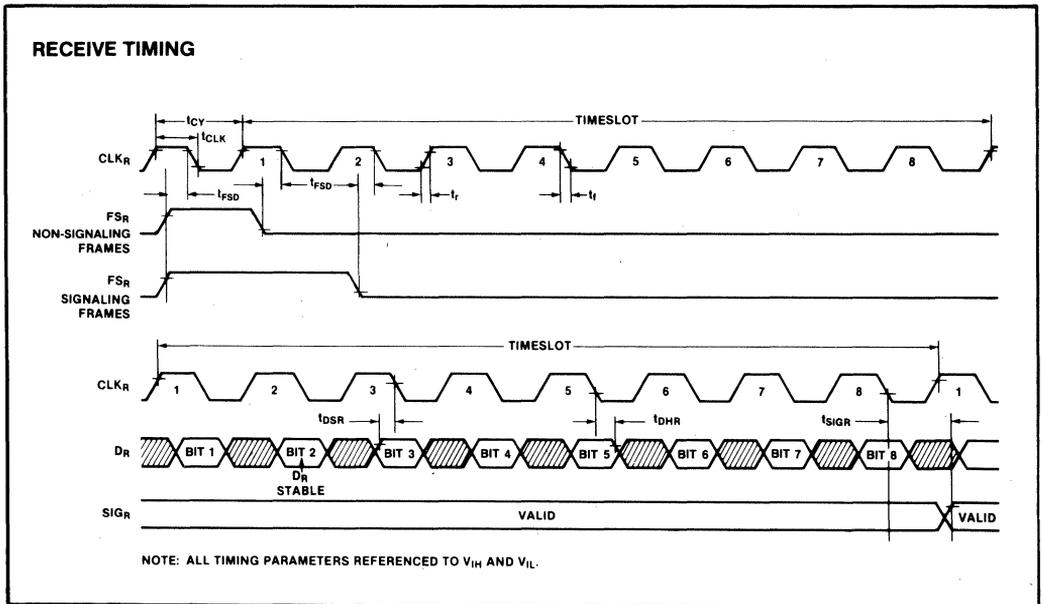
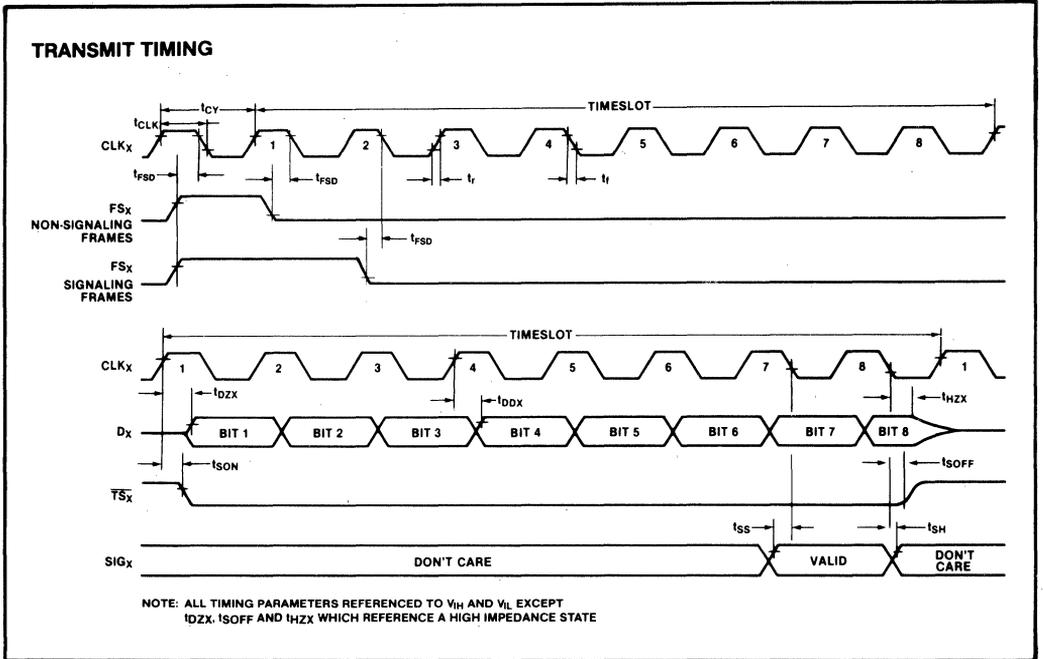
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DSR}	Receive Data Setup	10			ns	
t_{DHR}	Receive Data Hold	60			ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	
t_{SIGR}	SIG_R Update	0		2	μ s	

NOTES:

1. Timing parameters t_{DZX} , t_{HZX} , and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

Fixed Data Rate Timing



TRANSMIT SECTION, VARIABLE DATA RATE MODE¹

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X^2$	140		$t_{DX} - 140$	ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pf
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pf
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pf
t_{DX}	Data Clock Period	488		1562	ns	
t_{DFSX}	Data Delay from FS_X	0		140	ns	

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R^3$	140		$t_{DR} - 140$	ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
t_{DR}	Data Clock Period	488		1562	ns	
t_{SER}	Timeslot End Receive Time	0			ns	

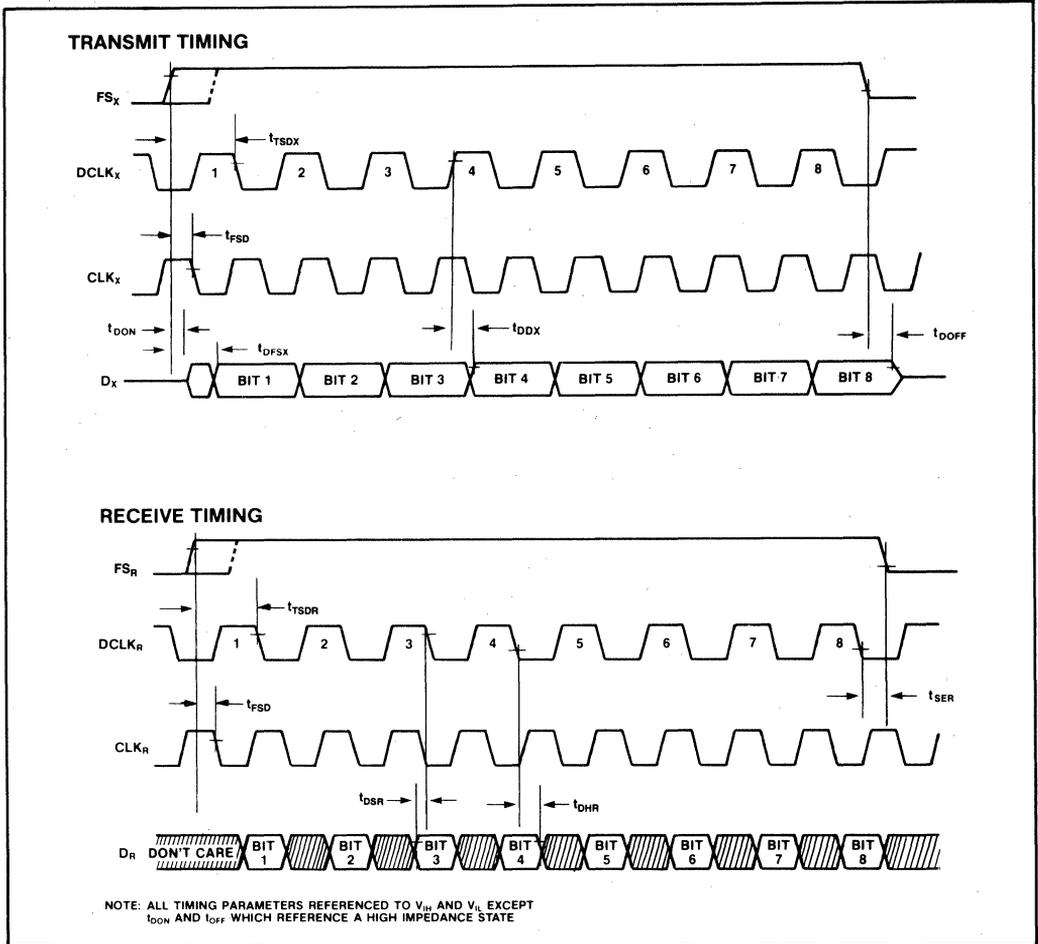
64 KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	1952			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	μ S	

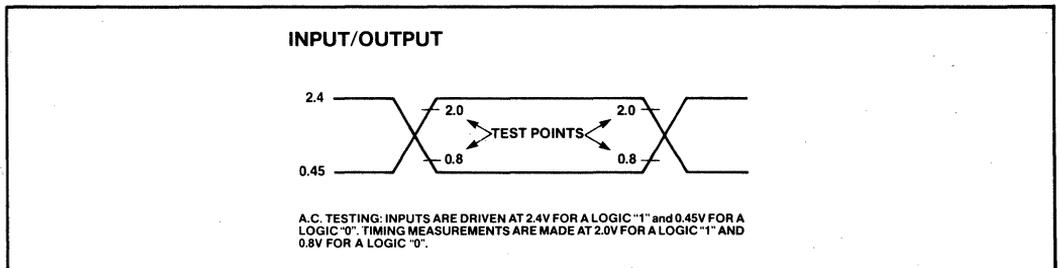
NOTES:

1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. t_{FSLX} minimum requirements overrides t_{TSDX} maximum spec for 64 kHz operation.
3. t_{FSLR} minimum requirements overrides t_{TSDR} maximum spec for 64 kHz operation.

VARIABLE DATA RATE TIMING



A.C. TESTING INPUT, OUTPUT WAVEFORM



29C16 AND 29C17 16 PIN CHMOS SINGLE-CHIP PCM CODEC AND FILTER

- 29C16 μ -Law, 2.048 MHz Master Clock
- 29C17 A-Law, 2.048 MHz Master Clock

- Low-Power Pin Compatible Version of Intel's 2916 and 2917
- AT&T D3/D4 and CCITT Compatible
- 16-Pin Package for Higher Linecard Densities
- Ideal for Digital Handset Applications

- 3 Low-Power Modes
 - 5mW Typical Power Down
 - 8mW Typical Standby
 - 70mW Typical Operating
- TTL and CMOS Compatible
- Two Timing Modes
 - 64 KHz to 2 MHz Variable
 - 2 MHz Direct

Intel's 29C16 and 29C17 are CHMOS versions of Intel's NMOS 2916 and 2917 family members. CHMOS is a technology built on HMOS-II, thus realizing the high performance and density obtained in that process while achieving the low power consumption typical of CMOS circuits.

The 29C16 and 29C17 are limited feature versions of the 29C13 and 29C14. The inherent low-power and small package size make these devices ideal for digital handset and cellular telephones where small size and low power are especially desirable.

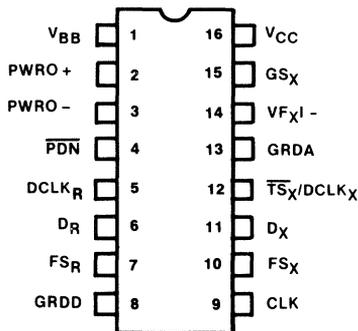


Figure 1. Pin Configuration

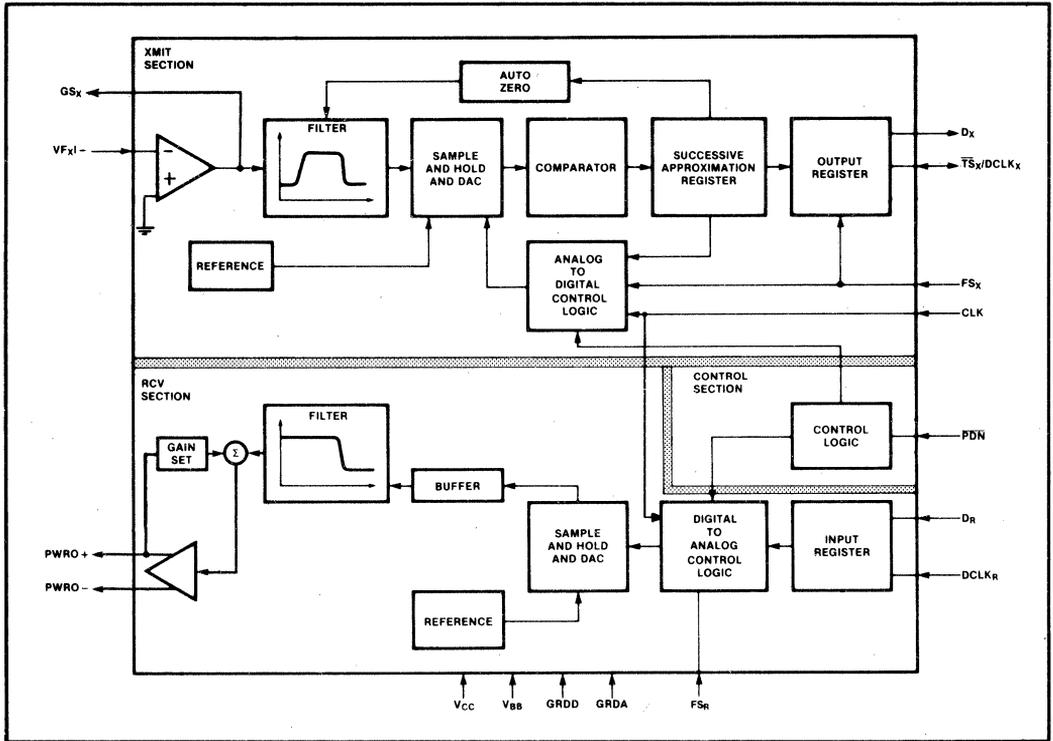


Figure 2. Block Diagram

Table 1. Pin Names

V_{BB}	Power (-5V)	GS_x	Transmit Gain Control
$PWRO+$, $PWRO-$	Power Amplifier Outputs	VF_{xI-}	Analog Input
\overline{PDN}	Power Down Select	$GRDA$	Analog Ground
$DCLK_R$	Receive Variable Data Clock	\overline{TS}_x	Timeslot Strobe/Buffer Enable
D_R	Receive PCM Input	$DCLK_x$	Transmit Variable Data Clock
FS_R	Receive Frame Synchronization Clock	D_x	Transmit PCM Output
$GRDD$	Digital Ground	FS_x	Transmit Frame Synchronization Clock
V_{CC}	Power (+5V)	CLK	Master Clock

Table 2. Pin Description

Symbol	Function
V _{BB}	Most negative supply; input voltage is -5 volts ±5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO-	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
PDN	Power down select. When PDN is TTL high, the device is active. When low, the device is powered down.
DCLK _R	Selects the fixed or variable data rate mode. When DCLK _R is connected to V _{BB} , the fixed data rate mode is selected. In this mode, the device is fully compatible with Intel 2910A and 2911A direct mode timing. When DCLK _R is not connected to V _{BB} , the device operates in the variable data rate mode. In this mode DCLK _R becomes the receive data clock which operates at TTL levels from 64Kb to 2.048 Mb data rates.
D _R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK in the fixed data rate mode and DCLK _R in variable data rate mode.
FS _R	8KHz frame synchronization clock input/ timeslot enable, receive channel. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS _R is TTL low for 300 milliseconds.

Symbol	Function
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK	Master and data clock for the fixed data rate mode; master clock only in variable data rate mode.
FS _X	8 KHz frame synchronization clock input/ timeslot enable, transmit channel. Operates independently but in an analogous manner to FS _R . The transmit channel enters the standby state whenever FS _X is TTL low for 300 milliseconds.
D _X	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock; CLK in fixed data rate mode and DCLK _X in variable data rate mode.
$\overline{TS}_X/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer as in 2910A and 2911A direct mode timing. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64Kb to 2.048 Mb data rates.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF _X I-	Inverting analog input to uncommitted transmit operational amplifier.
GS _X	Output terminal of on-chip transmit channel input op amp. Internally, this is the voice signal input to the transmit filter.
V _{CC}	Most positive supply; input voltage is +5 volts ±5%.

FUNCTIONAL DESCRIPTION

The 29C16 and 29C17 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to PDN, provided that all clocks and supplies are connected. The 29C16 and 29C17 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and \overline{TS}_X are held in a high impedance state for approximately four frames (500 μ s) after power up or application of V_{BB} or V_{CC} . After this delay, D_X and \overline{TS}_X will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60

milliseconds to reach their equilibrium value due to the autozero circuit settling time.

To enhance system reliability, \overline{TS}_X and D_X will be placed in a high impedance state approximately 30 μ s after an interruption of CLK.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 29C16/C17 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the PDN pin. In this mode, power consumption is reduced to the value shown in Table 3. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the PDN pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R . With both channels in the standby state, power consumption is reduced to the value shown in Table 3. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A

Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	\overline{PDN} = TTL low	5 mW	\overline{TS}_X and D_X are placed in a high impedance state within 10 μ s.
Standby Mode	FS_X and FS_R are TTL low	8 mW	\overline{TS}_X and D_X are placed in a high impedance state within 300 milliseconds.
Only transmit is on standby	FS_X is TTL low	50 mW	\overline{TS}_X and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FS_R is TTL low	50 mW	

compatible, is selected by connecting $DCLK_R$ to V_{BB} . It employs master clock CLK, frame synchronization clocks FS_X and FS_R , and output \overline{TS}_X .

CLK serves as the master clock to operate the codec and filter sections and as the bit clock to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency. \overline{TS}_X is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK following the rising edge of FS_X . Similarly, on the receive side, data is received on the first eight falling edges of CLK. The frequency of CLK must be 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB} . It employs master clock CLK, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X .

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64 kHz to 2.048 MHz. The master clock is still restricted to 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 μ s frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. These

references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve the extremely accurate Digital Milliwatt Responses specified in the TRANSMISSION PARAMETERS, providing the user a significant margin for error in other board components.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip operational amplifier. This operational amplifier has a common mode range of ± 2.17 volts, a maximum DC offset of 25 mV, and a typical open loop voltage gain of 20,000. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_XI- can be either AC or DC coupled. The input op amp can only be used in the inverting mode as shown in Figure 3.

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stop-band attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The 29C16 and 29C17 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 4.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

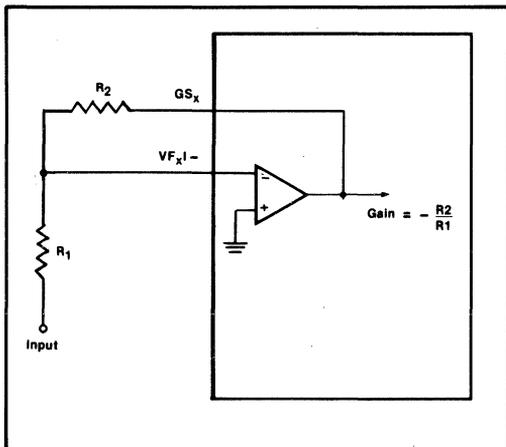


Figure 3. Transmit Filter Gain Adjustment

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way,

all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications will be within the limits shown in Figure 5.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended or 600 ohms differentially.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

Table 4. Zero Transmission Level Points

Symbol	Parameter	Typ	Units	Test Conditions
OTLP1 _x	Zero Transmission Level Point Transmit Channel (0dBm0) μ -law	+2.76 +1.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
OTLP2 _x	Zero Transmission Level Point Transmit Channel (0dBm0) A-law	+2.79 +1.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
OTLP1 _R	Zero Transmission Level Point Receive Channel (0dBm0) μ -law	+5.76 +4.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
OTLP2 _R	Zero Transmission Level Point Receive Channel (0dBm0) A-law	+5.79 +4.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
V _{CC} and GRDD with Respect to V _{BB}	-0.3V to 15V
All Input and Output Voltages with Respect to V _{BB}	-0.3V to 15V
All Input and Output Voltages with Respect to V _{CC}	-15V to +0.3V
Power Dissipation	1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)

Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I _{IL}	Low Level Input Current			10	μA	GRDD ≤ V _{IN} ≤ V _{IL} (Note 1)
I _{IH}	High Level Input Current			10	μA	V _{IH} ≤ V _{IN} ≤ V _{CC}
V _{IL}	Input Low Voltage			0.8	V	
V _{IH}	Input High Voltage	2.0			V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 3.2 mA at D _X , \overline{TS}_X
V _{OH}	Output High Voltage	2.4			V	I _{OH} = 80 μA at D _X
C _{OX}	Digital Output Capacitance ²		5		pF	
C _{IN}	Digital Input Capacitance		5	10	pF	

POWER DISSIPATION

All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I _{CC1}	V _{CC} Operating Current ⁴		6.8		mA	
I _{BB1}	V _{BB} Operating Current		7.2		mA	
I _{CC0}	V _{CC} Power Down Current		0.5		mA	$\overline{PDN} \leq V_{IL}$; after 10μs
I _{BB0}	V _{BB} Power Down Current		0.5		mA	$\overline{PDN} \leq V_{IL}$; after 10μs
I _{CCS}	V _{CC} Standby Current		0.8		mA	FS _X , FS _R ≤ V _{IL} ; after 300 ms
I _{BBS}	V _{BB} Standby Current		0.8		mA	FS _X , FS _R ≤ V _{IL} ; after 300 ms
P _{D1}	Operating Power Dissipation ³		70		mW	
P _{D0}	Power Down Dissipation ³		5		mW	$\overline{PDN} \leq V_{IL}$; after 10μs
P _{ST}	Standby Power Dissipation ³		8		mW	FS _X , FS _R ≤ V _{IL} ; after 300 ms

NOTES:

- V_{IN} is the voltage on any digital pin.
- Timing parameters are guaranteed based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM high-way without buffering, assuming a board capacitance of 60 pF.
- With nominal power supply values.
- V_{CC} applied last or simultaneously with V_{BB}.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input Leakage Current, $V_{F_{X1}} -$			100	nA	$-2.17V \leq V_{IN} \leq 2.17V$
R_{IX1}	Input Resistance, $V_{F_{X1}} -$	10			M Ω	
V_{OSX1}	Input Offset Voltage, $V_{F_{X1}} -$			25	mV	
A_{VOL}	DC Open Loop Voltage Gain, GS_x	5000				
f_c	Open Loop Unity Gain Bandwidth, GS_x		300		KHz	
C_{LX1}	Load Capacitance, GS_x			50	pF	
R_{LX1}	Minimum Load Resistance, GS_x	10			k Ω	

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output Resistance, PWRO+, PWRO-		1		Ω	
V_{OSRA}	Single-Ended Output DC Offset, PWRO+, PWRO-		75		mV	Relative to GRDA
C_{LRA}	Load Capacitance, PWRO+, PWRO-			100	pF	

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave.¹ Input amplifier is set for unity gain, inverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended. All output levels are (sin x)/x corrected. Typical values are for $T_A = 25^\circ\text{C}$ and nominal power supply values. ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; GRDA = 0; GRDD = 0; unless otherwise specified).

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response (Transmit gain tolerance)	-0.18	± 0.04	+0.18	dBm0	Signal input of 1.064 Vrms μ -law Signal input of 1.068 Vrms A-law $T_A = 25^\circ\text{C}$, $V_{BB} = -5V$, $V_{CC} = +5V$
EmW _{TS}	EmW variation with Temperature and supplies	-0.07	± 0.02	+0.07	dB	$\pm 5\%$ supplies, 0 to 70°C Relative to nominal conditions
DmW	Digital Milliwatt Response (Receive gain tolerance)	-0.18	± 0.04	+0.18	dBm0	Measure relative to 0TLP _R . Signal input per CCITT Recommendation G.711. Output signal of 1000 Hz. $R_L = \infty$ $T_A = 25^\circ\text{C}$; $V_{BB} = -5V$, $V_{CC} = +5V$.
DmW _{TS}	DmW variation with temperature and supplies	-0.07	± 0.02	+0.07	dB	$\pm 5\%$ supplies, 0 to 70°C

NOTES:

1. 0dBm0 is defined as the zero reference point of the channel for μ law under test (0TLP). This corresponds to an analog signal input of 1.064 volts rms or an output of 1.503 volts rms.

GAIN TRACKING

Reference Level = -10dBm0

Symbol	Parameter	2916		2917		Unit	Test Conditions
		Min	Max	Min	Max		
GT1 _x	Transmit Gain Tracking Error Sinusoidal Input; μ -law		± 0.25 ± 0.5 ± 1.2			dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, R _L = 300 Ω
GT2 _x	Transmit Gain Tracking Error Sinusoidal Input; A-law				± 0.25 ± 0.5 ± 1.2	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, R _L = 300 Ω
GT1 _r	Receive Gain Tracking Error Sinusoidal Input; μ -law		± 0.25 ± 0.5 ± 1.2			dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, R _L = 300 Ω
GT2 _r	Receive Gain Tracking Error Sinusoidal Input; A-law				± 0.25 ± 0.5 ± 1.2	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0 Measured at PWRO+, R _L = 300 Ω

NOISE (All receive channel measurements are single ended)

Symbol	Parameter	2916			2917			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
N _{XC1}	Transmit Noise, C-Message Weighted			15				dBrncO	Unity Gain
N _{XP}	Transmit Noise, Psophometrically Weighted						-75	dBm0p	Unity Gain
N _{RC1}	Receive Noise, C-Message Weighted: Quiet Code			11				dBrncO	D _R = 11111111
N _{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle			12				dBrncO	Input to D _R is zero code with sign bit toggle at 1 kHz rate
N _{RP}	Receive Noise, Psophometrically Weighted						-79	dBm0p	D _R = lowest positive decode level
N _{SF}	Single Frequency Noise End to End Measurement			-50			-50	dBm0	CCITT G.712.4.2
PSRR ₁	V _{CC} Power Supply Rejection, Transmit Channel		-30			-30		dB	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D _x
PSRR ₂	V _{BB} Power Supply Rejection, Transmit Channel		-30			-30		dB	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D _x
PSRR ₃	V _{CC} Power Supply Rejection, Receive Channel		-25			-25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+, 0 to 50 kHz

NOISE (All receive channel measurements are single ended)

Symbol	Parameter	2916			2917			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
PSRR ₄	V _{BB} Power Supply Rejection, Receive Channel		-25			-25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+, 0 to 50 kHz
CT _{TR}	Crosstalk, Transmit to Receive			-71			-71	dB	Input = 0dBm0, Unity Gain, 1.02 kHz, D _R = lowest positive decode level, measure at PWRO+
CT _{RT}	Crosstalk, Receive to Transmit			-71			-71	dB	D _R = 0dBm0, 1.02 kHz, measure at D _X

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SD1 _X	Transmit Signal to Distortion, μ -Law Sinusoidal Input; CCITT G.712-Method 2 (2916)	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD2 _X	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2 (2917)	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD1 _R	Receive Signal to Distortion, μ -Law Sinusoidal Input; CCITT G.712-Method 2 (2916)	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD2 _R	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2 (2917)	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
DP _X	Transmit Single Frequency Distortion Products (29C16)			-46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP _R	Receive Single Frequency Distortion Products (29C16)			-46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD ₁	Intermodulation Distortion, End to End Measurement			-35	dB	CCITT G.712 (7.1)
IMD ₂	Intermodulation Distortion, End to End Measurement			-49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			-25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			-40	dBm0	CCITT G. 712 (9)
D _{AX}	Transmit Absolute Delay		245		μ s	Fixed Data Rate. CLK _X = 2.048 MHz; 0 dBm0, 1.02 kHz input Signal, Unity Gain. Measure at D _X .
D _{DX}	Transmit Differential Envelope Delay Relative to D _{AX}		170		μ s	f = 500 - 600 Hz
			95		μ s	f = 600 - 1000 Hz
			45		μ s	f = 1000 - 2600 Hz
			105		μ s	f = 2600 - 2800 Hz

DISTORTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
D _{AR}	Receive Absolute Delay		190		µs	Fixed Data Rate, CLK = 2.048 MHz; Digital Input is DMW codes. Measure at PWRO + .
D _{DR}	Receive Differential Envelope Delay Relative to D _{AR}		45		µs	f = 500 – 600 Hz
			35		µs	f = 600 – 1000 Hz
			85		µs	f = 1000 – 2600 Hz
			110		µs	f = 2600 – 2800 Hz

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, inverting.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G _{RX}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at VFx1-
	16.67 Hz			-30	dB	
	50 Hz			-25	dB	
	60 Hz			-23	dB	
	200 Hz	-1.8		-0.125	dB	
	300 to 3000 Hz	-0.125		+0.125	dB	
	3300 Hz	-0.35		+0.03	dB	
	3400 Hz	-0.7		-0.10	dB	
	4000 Hz			-14	dB	
	4600 Hz and Above			-32	dB	

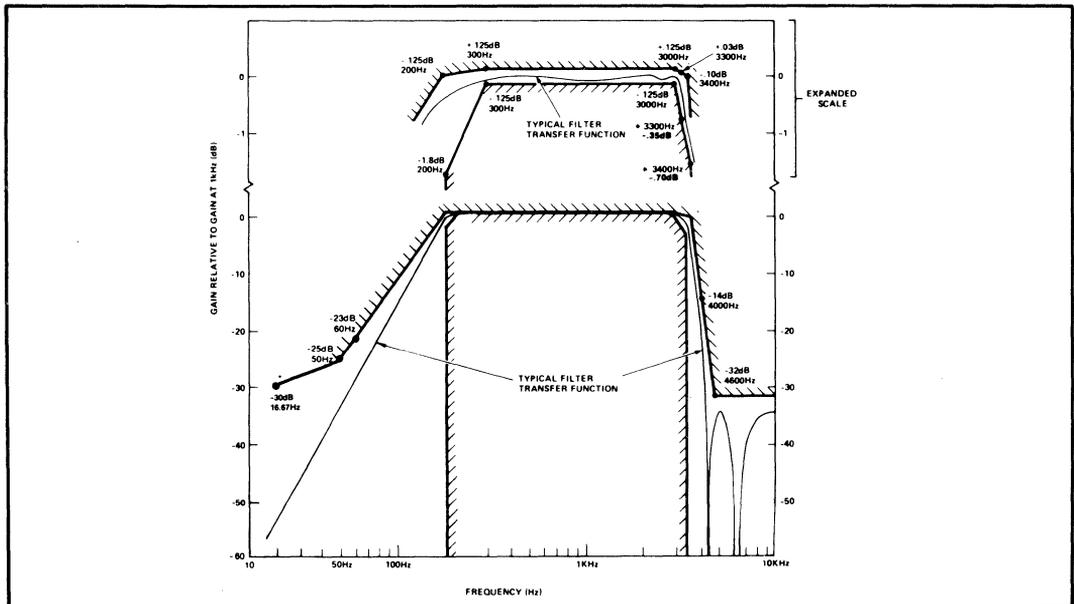


Figure 4. Transmit Channel

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_{RR}	Gain Relative to Gain at 1.02 kHz					0 dBm0 Signal input at D_R
	Below 200 Hz			+0.125	dB	
	200 Hz	-0.5		+0.125	dB	
	300 to 3000 Hz	-0.125		+0.125	dB	
	3300 Hz	-0.35		+0.03	dB	
	3400 Hz	-0.7		-0.1	dB	
	4000 Hz			-14	dB	
	4600 Hz and Above			-30	dB	

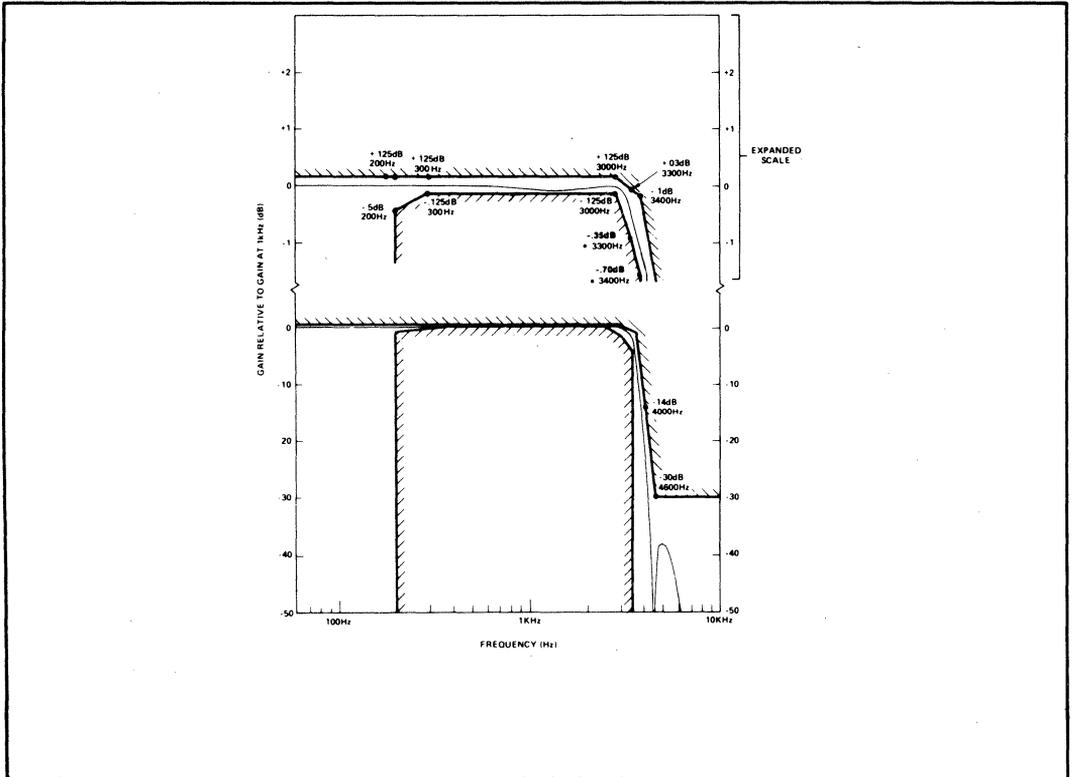


Figure 5. Receive Channel

A.C. CHARACTERISTICS — TIMING PARAMETERS
CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CY}	Clock Period, CLK	488			ns	$f_{CLK} = 2.048$ MHz
t_{CLK}	Clock Pulse Width, CLK	220			ns	
t_{DCLK}	Data Clock Pulse Width	220			ns	64 kHz $\leq f_{DCLK} \leq 2.048$ MHz
t_{CDC}	Clock Duty Cycle, CLK	45	50	55	%	
t_r, t_f	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE¹

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DZX}	Data Enabled on TS Entry	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{DDX}	Data Delay from CLK	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{HZX}	Data Float on TS Exit	60		215	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	0		145	ns	$0 < C_{LOAD} < 100$ pf
t_{SOFF}	Timeslot X to Disable	60		190	ns	$C_{LOAD} = 0$
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	

RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DSR}	Receive Data Setup	10			ns	
t_{DHR}	Receive Data Hold	60			ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	

NOTES:

- Timing parameters t_{DZX} , t_{HZX} , and t_{SOFF} are referenced to a high impedance state.

TRANSMIT SECTION, VARIABLE DATA RATE MODE¹

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDX}	Timeslot Delay from $DCLK_X^2$	140		$t_{DX} - 140$	ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	
t_{DDX}	Data Delay from $DCLK_X$	0		100	ns	$0 < C_{LOAD} < 100$ pf
t_{DON}	Timeslot to D_X Active	0		50	ns	$0 < C_{LOAD} < 100$ pf
t_{DOFF}	Timeslot to D_X Inactive	0		80	ns	$0 < C_{LOAD} < 100$ pf
t_{DX}	Data Clock Period	488		1562	ns	
t_{DFSX}	Data Delay from FS_X	0		140	ns	

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{TSDR}	Timeslot Delay from $DCLK_R^3$	140		$t_{DR} - 140$	ns	
t_{FSD}	Frame Sync Delay	100		$t_{CY} - 100$	ns	
t_{DSR}	Data Setup Time	10			ns	
t_{DHR}	Data Hold Time	60			ns	
t_{DR}	Data Clock Period	488		1562	ns	
t_{SER}	Timeslot End Receive Time	0			ns	

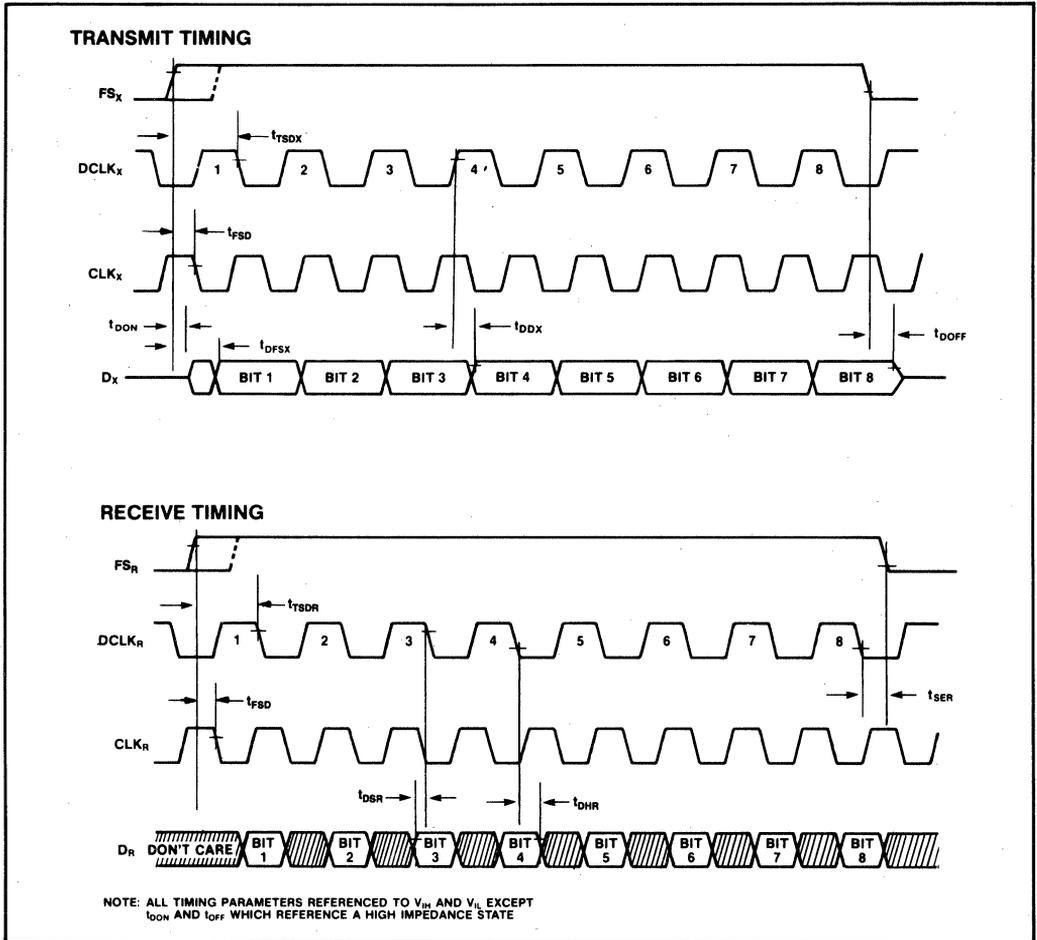
64 KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{FSLX}	Transmit Frame Sync Minimum Downtime	488			ns	FS_X is TTL high for remainder of frame
t_{FSLR}	Receive Frame Sync Minimum Downtime	1952			ns	FS_R is TTL high for remainder of frame
t_{DCLK}	Data Clock Pulse Width			10	μ s	

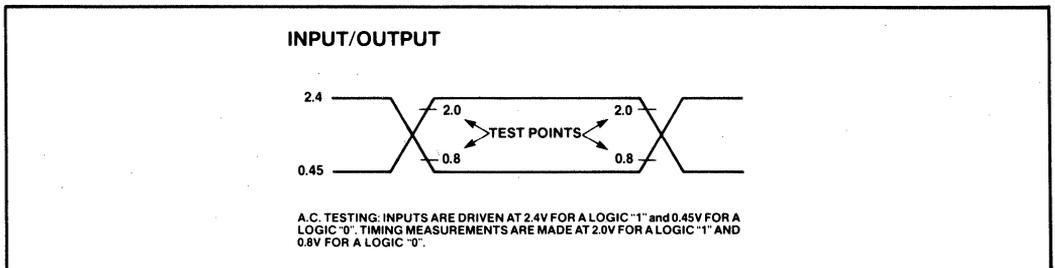
NOTES:

1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. t_{FSLX} minimum requirements overrides t_{TSDX} maximum spec for 64 kHz operation.
3. t_{FSLR} minimum requirements overrides t_{TSDR} maximum spec for 64 kHz operation.

VARIABLE DATA RATE TIMING



A.C. TESTING INPUT, OUTPUT WAVEFORM



80C49-7/80C39-7 CHMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

- 80C49-7 Low Power Mask Programmable ROM
- 80C39-7 Low Power, CPU only
- Pin-to-pin Compatible with Intel's 8049AH/8039AHL
- 1.36 μ sec Instruction Cycle. All Instructions 1 or 2 Cycles
- Ability to Maintain Operation during AC Power Line Interruptions
- Exit Idle Mode with an External or Internal Interrupt Signal
- Battery Operation
- 3 Power Consumption Selections
 - Normal Operation: 12 mA @ 11 MHz @ 5V
 - Idle Mode: 5 mA @ 11 MHz @ 5V
 - Power Down: 2 μ A @ 2.0V
- 11 MHz, TTL Compatible Operation:
 - $V_{CC} = 5V \pm 10\%$
 - CMOS Compatible Operation;
 - $V_{CC} = 5V \pm 20\%$

Intel's 80C49-7/80C39-7 are low power, CHMOS versions of the popular MCS[®]-48 HMOS family members. CHMOS is a technology built on HMOS II and features high resistivity P substrate, diffused N well, and scaled N and P channel devices. The 80C49-7/80C39-7 have been designed to provide low power consumption and high performance.

The 80C49-7 contains a 2K x 8 program memory, a 128 x 8 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to an on-board oscillator and clock circuits. For systems that require extra capability, the 80C49-7 can be expanded using CMOS external memories and MCS[®]-80 and MCS[®]-85 peripherals. The 80C39-7 is the equivalent of the 80C49-7 without program memory on-board.

The CHMOS design of the 80C49-7 opens new application areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during AC power line interruptions. These applications include portable and hand-held instruments, telecommunications, consumer, and automotive.

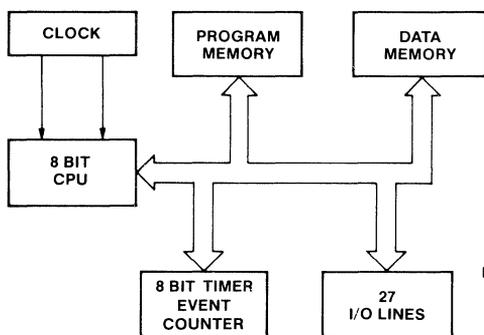


Figure 1.
Block Diagram

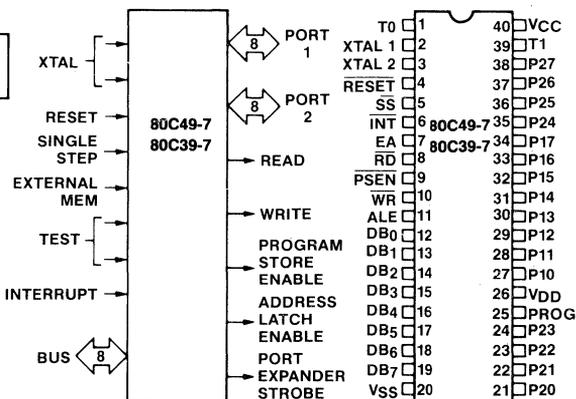


Figure 2:
Logic Symbol

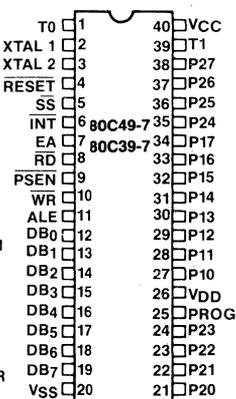


Figure 3.
Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Function	Symbol	Pin No.	Function
VSS	20	Circuit GND potential			Can be designated the timer/counter input using the STRT CNT instruction.
VDD	26	Low Power standby pin			
VCC	40	Main power supply; +5V during operation.	INT	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) Interrupt must remain low for at least 3 machine cycles for proper operation.
PROG	25	Output strobe for 82C43 I/O expander.			
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.	RD	8	Output strobe activated during a BUS read. Can be used to enable data onto toe bus from an external device. Used as a read strobe to external data memory. (Active low)
P20-P23	21-24	8-bit quasi-bidirectional port.	RESET	4	Input which is used to initialize the processor. (Active low) (Non TTL V _{IH})
P24-P27 Port 2	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.	WR	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.	ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.	PSEN	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
T1	39	Input pin testable using the JT1, and JNT1 instructions.	SS	5	Single step input can be used in conjunction with

Table 1. Pin Description (Continued)

Symbol	Pin No.	Function
SS (Con't)		ALE to "single step" the processor through each instruction (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing

Symbol	Pin No.	Function
		and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

IDLE MODE DESCRIPTION

The 80C49-7, when placed into Idle mode, keeps the oscillator, the internal timer and the external interrupt and counter pins functioning and maintains the internal register and RAM status.

To place the 80C49-7 in Idle mode, a command instruction (op code 01H) is executed. To terminate Idle mode, a reset must be performed or interrupts must be enabled and an interrupt signal generated. There are two interrupt sources that can restore normal operation. One is an external signal applied to the interrupt pin. The other is from the overflow of the timer/counter. When either interrupt is invoked, the CPU is taken out of Idle mode and vectors to the interrupt's service routine address. Along with the Idle mode, the standard MCS[®]-48 power-down mode is still maintained.

Table 2. Instruction Set

Accumulator			
Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output			
Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers			
Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch			
Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JNI addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine			
Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2

Flags			
Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Table 2. Instruction Set (Continued)

Data Moves			
Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, # data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2

Timer/Counter			
Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control			
Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1
IDL	Select Idle Operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to 70°C
 Storage Temperature -65°C to +150°C
 Voltage On Any Pin With Respect to Ground -0.5V to V_{CC}+1V
 Maximum Voltage On Any Pin With Respect to Ground 7V
 Power Dissipation 1.0 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

D.C. CHARACTERISTICS: ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = V_{DD} = 5\text{V} \pm 20\%$; $|V_{CC} - V_{DD}| \leq 1.5\text{V}$; $V_{SS} = 0\text{V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IL}	Input Low Voltage (All Except X1, RESET)	- .5		.18 V_{CC}	V	
V_{IL1}	Input Low Voltage X1, RESET	- 5		.13 V_{CC}	V	
V_{IH}	Input High Voltage (All Except XTAL1, RESET)	0.2 V_{CC} + 1.2		V_{CC}	V	
V_{IH1}	Input High Voltage (X1, RESET)	.7 V_{CC}		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS)			.6	V	$I_{OL} = 2.0\text{ mA}$
V_{OL1}	Output Low Voltage (RD, WR, PSEN, ALE)			.6	V	$I_{OL} = 1.8\text{ mA}$
V_{OL2}	Output Low Voltage (PROG)			.6	V	$I_{OL} = 1.0\text{ mA}$
V_{OL3}	Output Low Voltage (All Other Outputs)			.6	V	$I_{OL} = 1.6\text{ mA}$
V_{OH}	Output High Voltage (BUS)	.75 V_{CC}			V	$I_{OH} = -400\ \mu\text{A}$
V_{OH1}	Output High Voltage (RD, WR, PSEN, ALE)	.75 V_{CC}			V	$I_{OH} = -100\ \mu\text{A}$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4 3.0			V	$I_{OH} = -40\ \mu\text{A}$ $I_{OH} = -20\ \mu\text{A}$
I_{L1}	Input Leakage Current (T1, INT, EA)			± 5	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{L11}	Input Leakage Current (P10-P17, P20-P27, SS)			-500	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{L0}	Output Leakage Current (BUS, TO) (High Impedance State)			± 5	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LR}	Input Leakage Current (RESET)	-10		-300	μA	$V_{SS} \leq V_{IN} \leq V_{IH1}$
I_{PD}	Power Down Standby Current			2	μA	$V_{DD} = 2.0\text{V}$ RESET $\leq V_{IL}$

 I_{CC} Active Current (mA)

V_{CC}	4V	5V	6V
1 MHz	2.5	3.3	4.0
6 MHz	5	6.8	8.5
11 MHz	9	12	15

 I_{CC} Idle Current (mA)

V_{CC}	4V	5V	6V
1 MHz	1.7	2.0	2.2
6 MHz	2	3	4
11 MHz	3.5	4.8	6

Absolute Maximum Unloaded Current

 I_{CC} Test Conditions:
 I_{CC} Active

All outputs disconnected
 T1, INT, SS, T0 connected to HIGH (V_{IH})
 EA, RST connected to LOW (V_{IL})
 XTAL1 External Drive
 Rise Time = 10 ns, Fall Time = 10 ns
 XTAL2 No connection
 $V_{IH} = V_{CC} - 0.5\text{V}$
 $V_{IL} = V_{SS} + 0.5\text{V}$

 I_{CC} Idle

All outputs disconnected
 XTAL1 External Drive
 Rise Time = 10 ns, Fall Time = 10 ns
 XTAL2 No connection
 $V_{IH} = V_{CC} - 0.5\text{V}$
 $V_{IL} = V_{SS} + 0.5\text{V}$

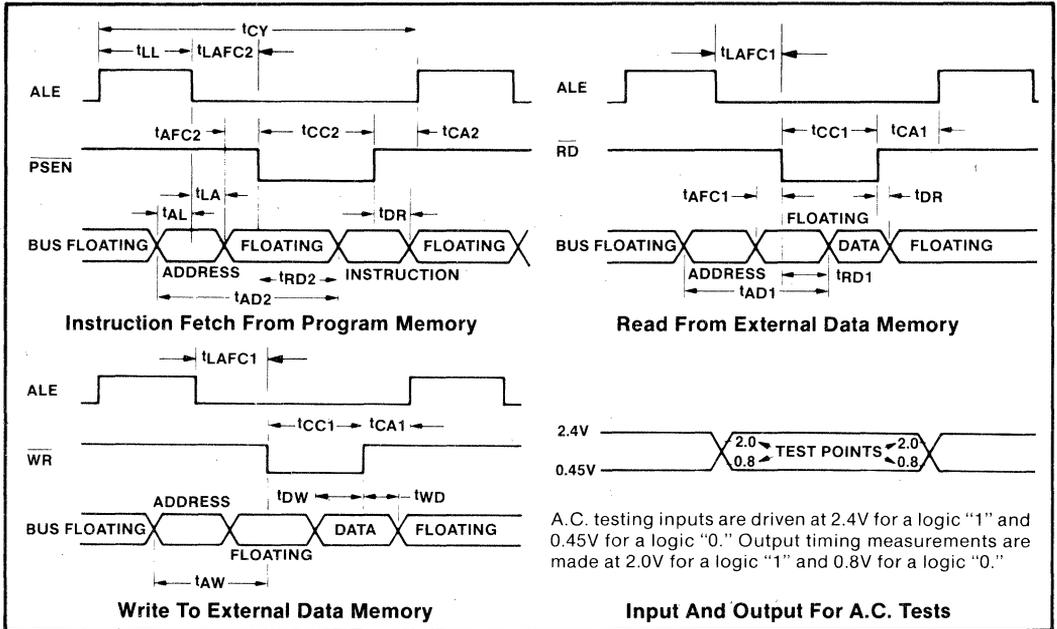
A.C. CHARACTERISTICS: ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = V_{DD} = 5V \pm 20\%$; $|V_{CC} - V_{DD}| \leq 1.5V$; $V_{SS} = 0V$)

Symbol	Parameter	f (t) (Note 3)	11 MHz		Unit	Conditions (Note 1)
			Min	Max		
t	Clock Period	1/xtal freq	90.9	1000	ns	(Note 3)
t _{LL}	ALE Pulse Width	3.5t-170	150		ns	
t _{AL}	Addr Setup to ALE	2t-110	70		ns	(Note 2)
t _{LA}	Addr Hold from ALE	t-40	50		ns	
t _{CC1}	Control Pulse Width (\overline{RD} , \overline{WR})	7.5t-200	480		ns	
t _{CC2}	Control Pulse Width (\overline{PSEN})	6t-200	350		ns	
t _{DW}	Data Setup before \overline{WR}	6.5t-200	390		ns	
t _{WD}	Data Hold after \overline{WR}	t-50	40		ns	
t _{DR}	Data Hold (\overline{RD} , \overline{PSEN})	1.5t-30	0	110	ns	
t _{RD1}	\overline{RD} to Data in	6t-170		350	ns	
t _{RD2}	\overline{PSEN} to Data in	4.5t-170		190	ns	
t _{AW}	Addr Setup to \overline{WR}	5t-150	300		ns	
t _{AD1}	Addr Setup to Data (\overline{RD})	10.5t-220		730	ns	
t _{AD2}	Addr Setup to Data (\overline{PSEN})	7.5t-220		460	ns	
t _{AFC1}	Addr Float to \overline{RD} , \overline{WR}	2t-40	140		ns	(Note 2)
t _{AFC2}	Addr Float to \overline{PSEN}	.5t-40	10		ns	(Note 2)
t _{LAFC1}	ALE to Control (\overline{RD} , \overline{WR})	3t-75	200		ns	
t _{LAFC2}	ALE to Control (\overline{PSEN})	1.5t-75	60		ns	
t _{CA1}	Control to ALE (\overline{RD} , \overline{WR} , \overline{PROG})	t-65	25		ns	
t _{CA2}	Control to ALE (\overline{PSEN})	4t-70	290		ns	
t _{CP}	Port Control Setup to \overline{PROG}	1.5t-80	50		ns	
t _{PC}	Port Control Hold to \overline{PROG}	4t-260	100		ns	
t _{PR}	\overline{PROG} to P2 Input Valid	8.5t-120		650	ns	
t _{PF}	Input Data Hold from \overline{PROG}	1.5t	0	140	ns	
t _{DP}	Output Data Setup	6t-290	250		ns	
t _{PD}	Output Data Hold	1.5t-90	40		ns	
t _{PP}	\overline{PROG} Pulse Width	10.5t-250	700		ns	
t _{PL}	Port 2 I/O Setup to ALE	4t-200	160		ns	
t _{LP}	Port 2 I/O Hold to ALE	1.5t-120	15		ns	
t _{PV}	Port Output from ALE	4.5t+100		510	ns	
t _{0PRR}	T0 Rep Rate	3t	270		ns	
t _{CY}	Cycle Time	15t	1.36	15.0	μs	

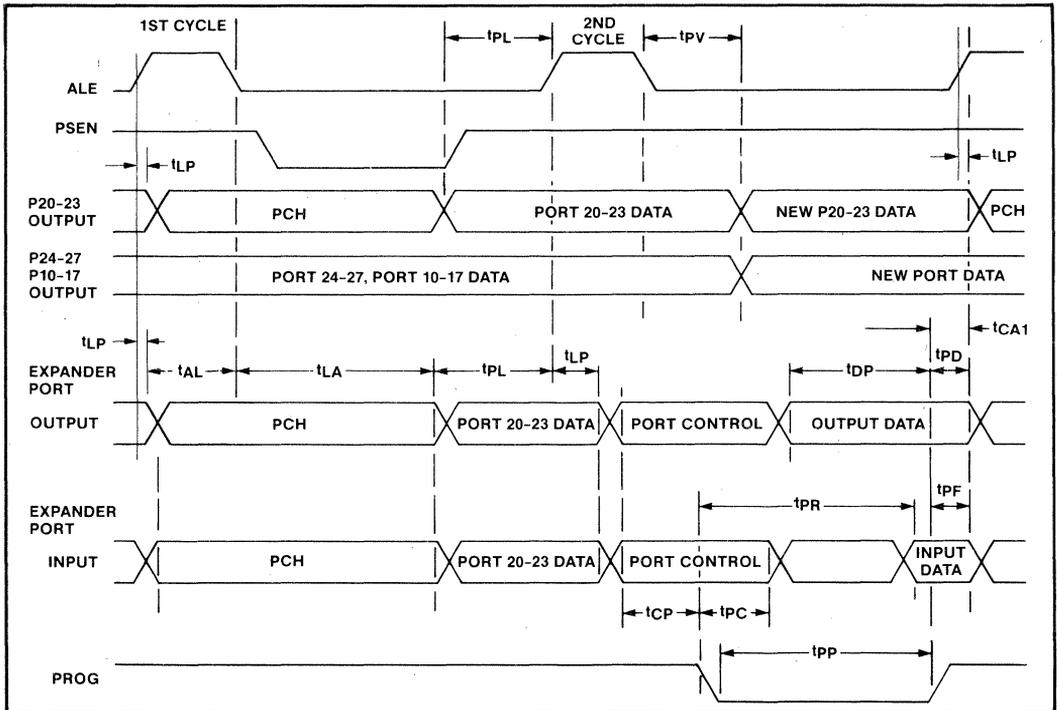
Notes:

- Control Outputs CL = 80pF
BUS Outputs CL = 150pF
- BUS High Impedance Load 20pF
- f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.

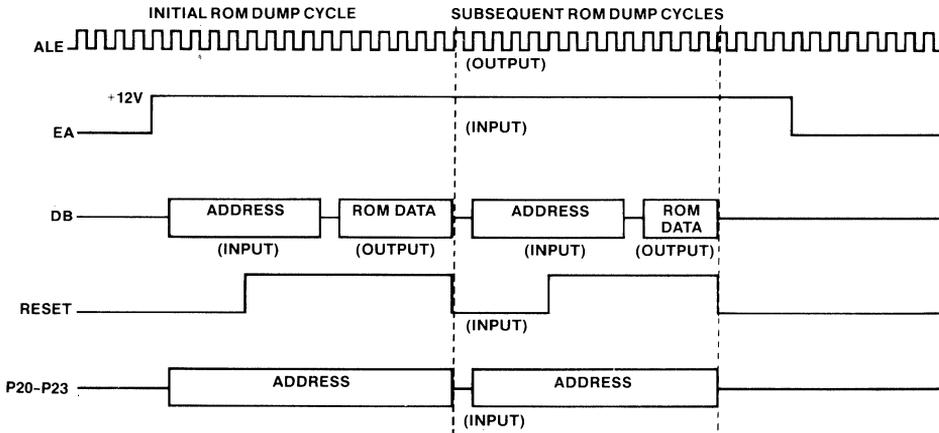
WAVEFORMS



PORT 1/PORT 2 TIMING



SUGGESTED ROM VERIFICATION ALGORITHM FOR CHMOS DEVICES ONLY



	C48	C49	C50
A10	0	ADDR	ADDR
A11	0	0	ADDR

VCC = VDD = + 5V

VSS = 0V

80C51BH/80C51BH-2 CHMOS SINGLE COMPONENT 8-BIT MICROCONTROLLER with Factory Mask-Programmable ROM

80C31BH/80C31BH-2 CHMOS SINGLE COMPONENT 8-BIT CONTROL-ORIENTED CPU WITH RAM AND I/O

80C51BH/80C31BH — 3.5 to 12 MHz $V_{CC} = 5V \pm 20\%$

80C51BH-2/80C31BH-2 — 0.5 to 12 MHz $V_{CC} = 5V \pm 20\%$

- 128 X 8 RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 64K Program Memory Space
- Boolean Processor
- 5 Interrupt Sources
- Programmable Serial Port
- 64K Data Memory Space

The MCS[®]-51 CHMOS products are fabricated on Intel's advanced CHMOS III process and are functionally compatible with the standard MCS-51 HMOS and EPROM products. CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. This combination expands the effectiveness of the powerful MCS-51 architecture and instruction set.

Like the MCS-51 EPROM and HMOS, the MCS-51 CHMOS products have the following features: 4K of ROM (80C51BH/80C51BH-2 only); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS-51 CHMOS products have two software selectable modes of reduced activity for further power reduction — Idle and Power Down.

Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. Power Down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

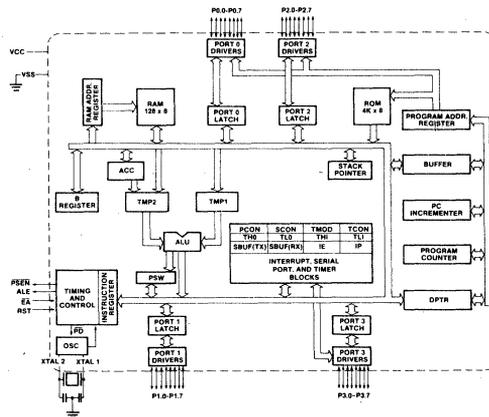


Figure 1. Block Diagram

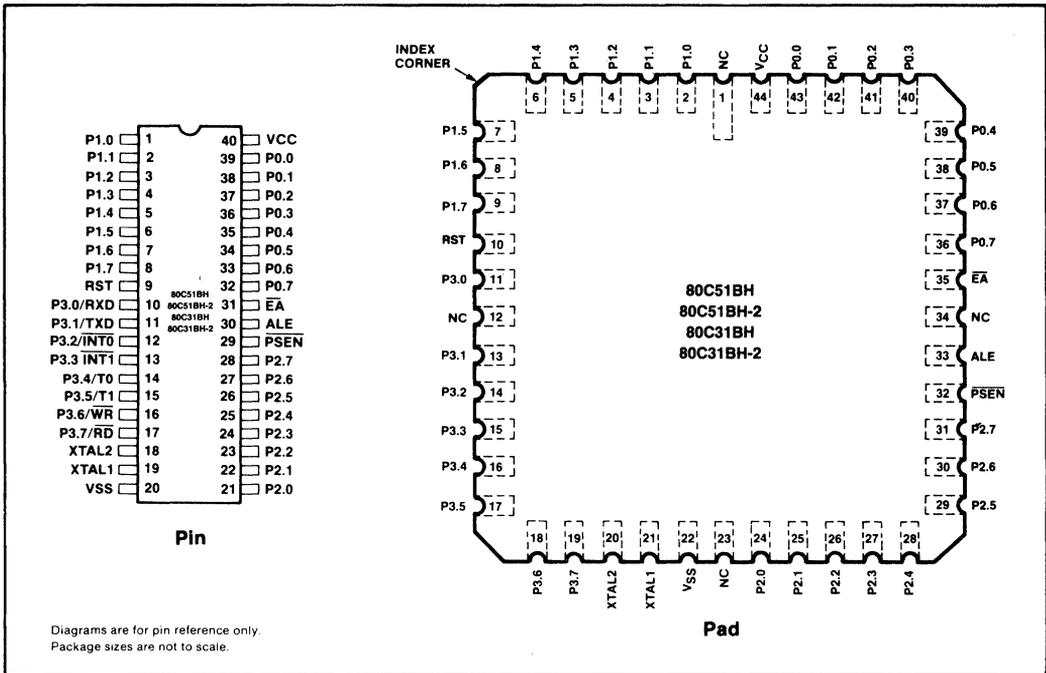


Figure 2. Configurations

IDLE AND POWER DOWN OPERATION

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation freezes the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is halted.

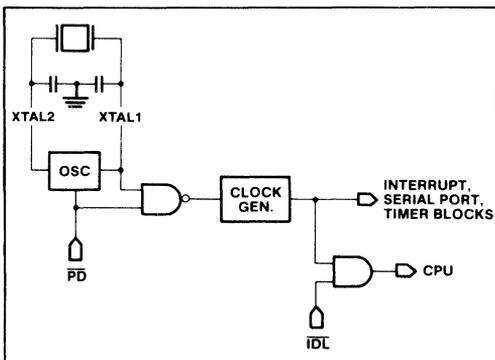


Figure 3. Idle and Power Down Hardware

These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

PCON: Power Control Register

(MSB)							(LSB)
SMOD	—	—	—	GF1	GF0	PD	IDL

Symbol Position Name and Function

SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
—	PCON.6 (Reserved)	
—	PCON.5 (Reserved)	
—	PCON.4 (Reserved)	
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XXX0000).

Idle Mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other registers maintain their data during Idle. Table 1 describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote a 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to going into power down. Once in power down, the oscillator is stopped. Only the contents of the on-chip RAM is preserved. The Special Function Registers are not saved. A hardware reset is the only way of exiting the power down mode.

In the Power Down mode, V_{CC} may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the

power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, p1, shown in figure 4.

80C51BH I/O Ports

The I/O port drive of the 80C51BH is similar to the 8051. The I/O buffers for Ports 1, 2, and 3 are implemented as shown in figure 4.

When the port latch contains a 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, p1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET p3 turns on through the inverter to supply the I_{OH} source current. This inverter and p3 form a latch which holds the 1 and is supported by p2.

When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have its strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as I_{TL} under the D.C. Specifications. When the input goes below approximately 2V, p3 turns off to save ICC current. Note, when returning to a logical 1, p2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input

Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

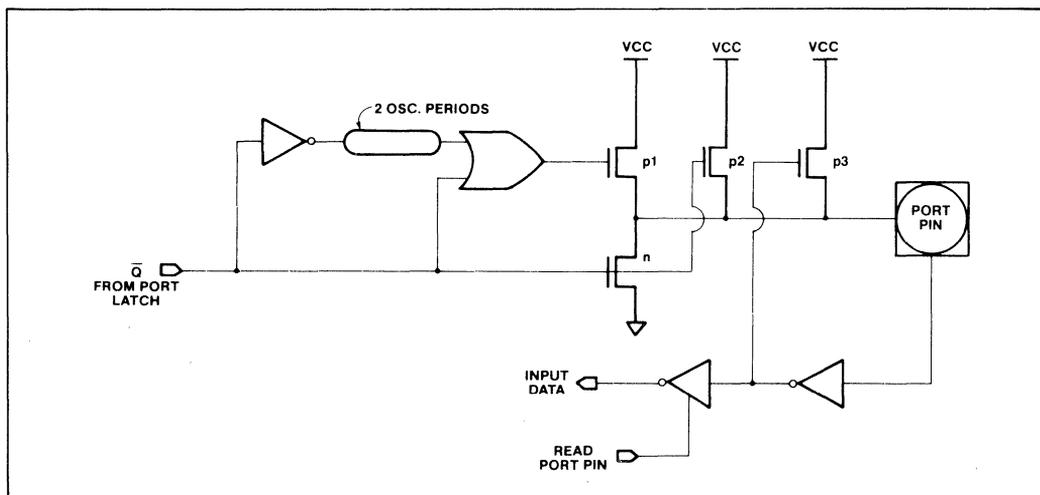


Figure 4. I/O Buffers in the 80C51BH (Ports 1, 2, 3)

line high. For additional information, refer to the chapter entitled "Design Considerations When Using CHMOS" in the 1984 Intel Microcontroller Handbook.

PIN DESCRIPTIONS

V_{CC}

Supply voltage during normal, Idle, and Power Down operations.

V_{SS}

Circuit ground.

Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 80C51BH. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are

pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during program verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits Power-On reset using only an external capacitor to V_{CC} .

ALE

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of $\frac{1}{6}$ the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

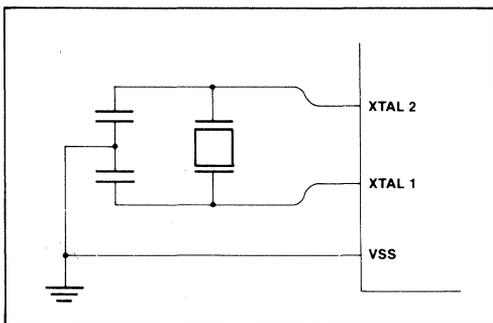


Figure 5. Crystal Oscillator

PSEN

Program Store Enable is the read strobe to external Program Memory.

When the 80C51BH is executing code from external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external Data Memory.

EA

External Access enable. $\overline{\text{EA}}$ must be externally held low in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock generator circuits.

XTAL2

Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in Figure 5. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in figure 6. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

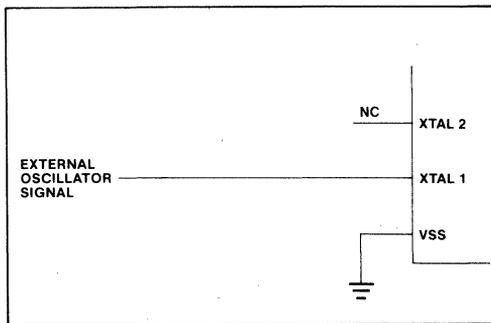


Figure 6. External Drive Configuration

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to 70°C
 Storage Temperature -65°C to +150°C
 Voltage on Any Pin to V_{SS} -0.5V to $V_{CC}+1V$
 Voltage on V_{CC} to V_{SS} -0.5V to +7V
 Power Dissipation 1.0W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS: ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{SS} = 0V$; $V_{CC} = 5V \pm 20\%$)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	$0.2V_{CC} - .1$	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	$0.2V_{CC} + .9$	$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage to XTAL1, RST	$0.7V_{CC}$	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)		0.45	V	$I_{OL} = 1.6 \text{ mA}$
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	$I_{OL} = 3.2 \text{ mA}$ (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2, 3)	2.4		V	$I_{OH} = -80\mu\text{A}$ $V_{CC} = 5V \pm 10\%$
		$0.75V_{CC}$		V	$I_{OH} = -30\mu\text{A}$
		$0.9V_{CC}$		V	$I_{OH} = -10\mu\text{A}$
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, PSEN)	2.4		V	$I_{OH} = -400\mu\text{A}$ $V_{CC} = 5V \pm 10\%$
		$0.75V_{CC}$		V	$I_{OH} = -150\mu\text{A}$
		$0.9V_{CC}$		V	$I_{OH} = -40\mu\text{A}$ (Note 2)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)		-50	μA	$V_{in} = 0.45V$
I_{TL}	Logical 1 to 0 transition Current (Ports 1, 2, 3)		-500	μA	$V_{in} = 2.0V$
I_{LI}	Input Leakage Current (Port 0, EA)		± 10	μA	$0.45 < V_{in} < V_{CC}$
R_{RST}	RST Pulldown Resistor	40	125	Kohm	
C_{IO}	Pin Capacitance		10	pF	test freq = 1 MHz, $T_A = 25^\circ\text{C}$
I_{PD}	Power Down Current		50	μA	$V_{CC} = 2$ to $6V$ (Note 3)

Maximum Operating I_{CC} (mA) (note 4)

V_{CC}	4V	5V	6V
Freq.			
0.5 MHz	1.6	2.2	3
3.5 MHz	4.3	5.7	7.5
8 MHz	8.3	11	14
12 MHz	12	16	20

Maximum Idle I_{CC} (mA) (note 5)

V_{CC}	4V	5V	6V
Freq.			
0.5 MHz	0.6	0.9	1.2
3.5 MHz	1.1	1.6	2.2
8 MHz	1.8	2.7	3.7
12 MHz	2.5	3.7	5

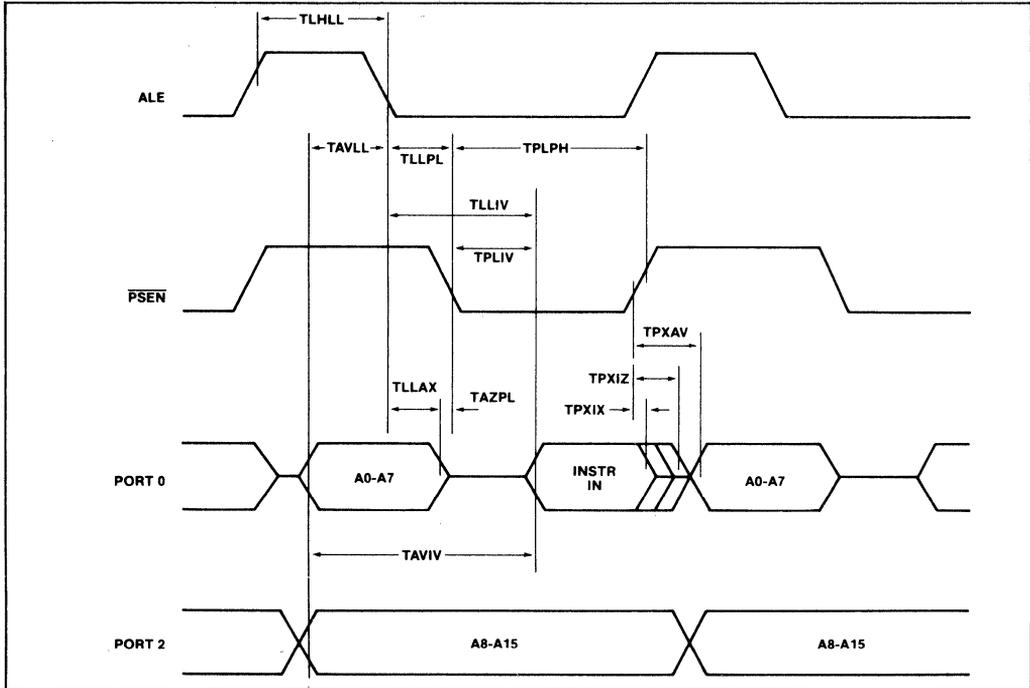
- Note 1:** Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE, and Ports 1 and 3. The noise is due to the external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
- Note 2:** Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $.9V_{CC}$ specification when the address bits are stabilizing.
- Note 3:** Power Down I_{CC} is measured with all output pins disconnected; EA = PORT0 = V_{CC} ; XTAL2 N.C.; RST = V_{SS} .
- Note 4:** I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 10 ns, $V_{ij} = V_{SS} + .5v$, $V_{ih} = V_{CC} - .5v$; XTAL2 N.C.; EA = RST = PORT0 = V_{CC} .
- Note 5:** Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 10 ns, $V_{ij} = V_{SS} + .5v$, $V_{ih} = V_{CC} - .5v$; XTAL2 N.C.; EA = PORT0 = V_{CC} ; RST = V_{SS} .

A.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{SS} = 0V$; $V_{CC} = 5V \pm 20\%$;
 Load Capacitance for Port 0, ALE, and PSEN = 100 pF, Load Capacitance for
 All Other Outputs = 80 pF)

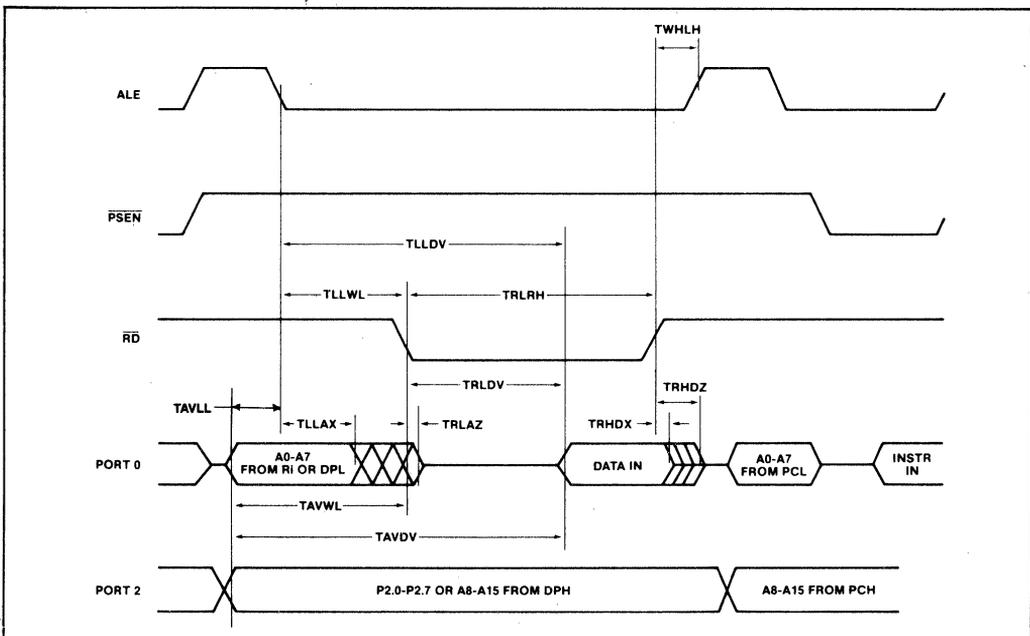
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Freq (80C51BH)	3.5	12	MHz
	Oscillator Freq (80C51BH-2)	0.5	12	MHz
TLHLL	ALE Pulse Width	2TCLCL - 40		ns
TAVLL	Address Valid to ALE Low	TCLCL - 40		ns
TLLAX	Address Hold After ALE Low	TCLCL - 35		ns
TLLIV	ALE Low to Valid Instr In		4TCLCL - 150	ns
TLLPL	ALE Low to PSEN Low	TCLCL - 25		ns
TPLPH	PSEN Pulse Width	3TCLCL - 35		ns
TPLIV	PSEN Low to Valid Instr In		3TCLCL - 150	ns
TPXIX	Input Instr Hold After PSEN	0		ns
TPXIZ	Input Instr Float After PSEN		TCLCL - 20	ns
TPXAV	PSEN to Address Valid	TCLCL - 8		ns
TAVIV	Address to Valid Instr In		5TCLCL - 150	ns
TPLAZ	PSEN Low to Address Float		0	ns
TRLRH	RD Pulse Width	6TCLCL - 100		ns
TWLWH	WR Pulse Width	6TCLCL - 100		ns
TRLDV	RD Low to Valid Data In		5TCLCL - 165	ns
TRHDX	Data Hold After RD	0		ns
TRHDZ	Data Float After RD		2TCLCL - 70	ns
TLLDV	ALE Low to Valid Data In		8TCLCL - 150	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



A.C. CHARACTERISTICS

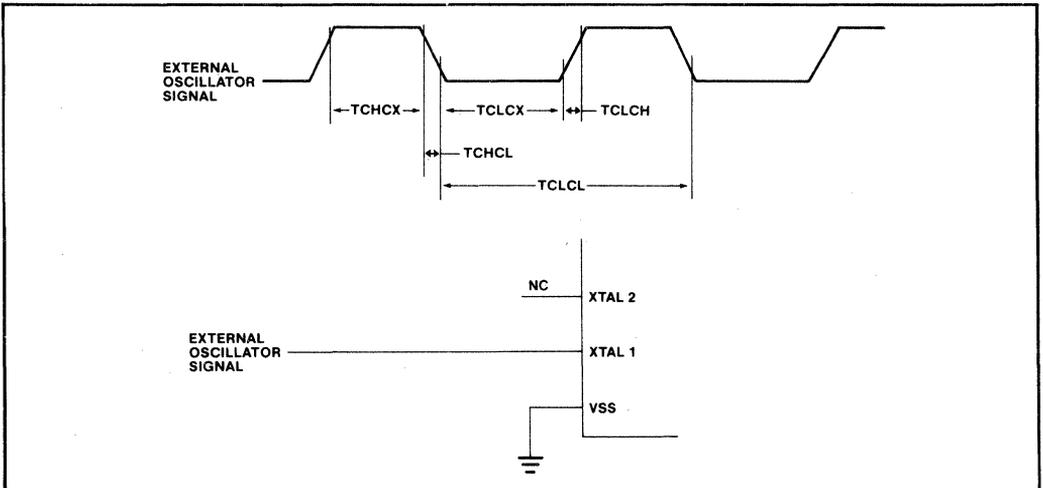
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units
TAVDV	Address to Valid Data In		9TCLCL - 165	ns
TLLWL	ALE Low to \overline{RD} or \overline{WR} Low	3TCLCL - 50	3TCLCL + 50	ns
TAVWL	Address to \overline{RD} or \overline{WR} Low	4TCLCL - 130		ns
TQVWX	Data Valid to \overline{WR} Transition	TCLCL - 60		ns
TQVWH	Data Valid to \overline{WR} High	7TCLCL - 150		ns
TWHQX	Data Held After \overline{WR}	TCLCL - 50		ns
TRLAZ	\overline{RD} Low to Address Float		0	ns
TWHLH	\overline{RD} or \overline{WR} High to ALE High	TCLCL - 40	TCLCL + 50	ns

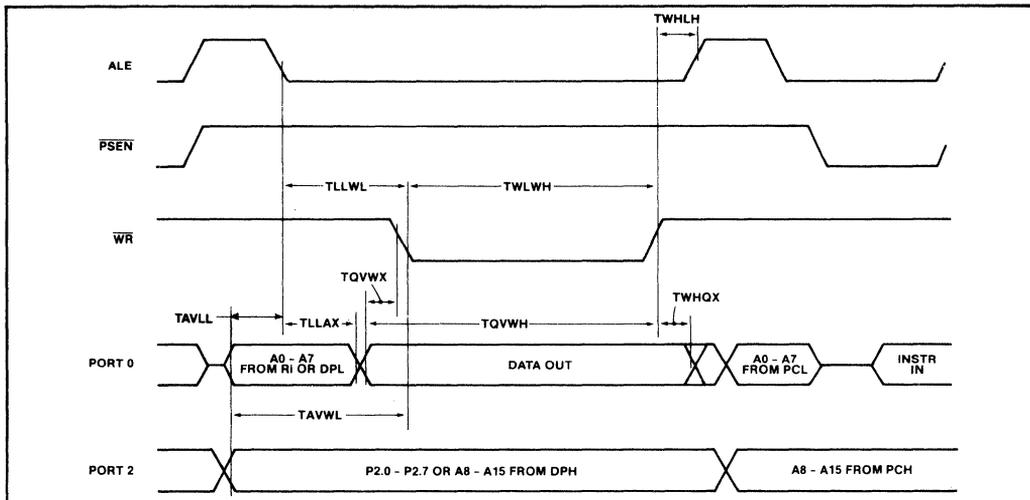
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Freq (80C51BH)	3.5	12	MHz
	Oscillator Freq (80C51BH-2)	0.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE



EXTERNAL DATA MEMORY WRITE CYCLE



SERIAL PORT TIMING — SHIFT REGISTER MODE

A.C. CHARACTERISTICS: ($T_A = 0^{\circ}\text{C}$ to 70°C ; $V_{SS} = 0\text{V}$; $V_{CC} = 5\text{V} \pm 20\%$;
Load Capacitance = 80 pF)

Symbol	Parameter	Min	Max	Units
TXLXL	Serial Port Clock Cycle Time	12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	10TCLCL - 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	2TCLCL - 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		10TCLCL - 133	ns

SHIFT REGISTER TIMING WAVEFORMS

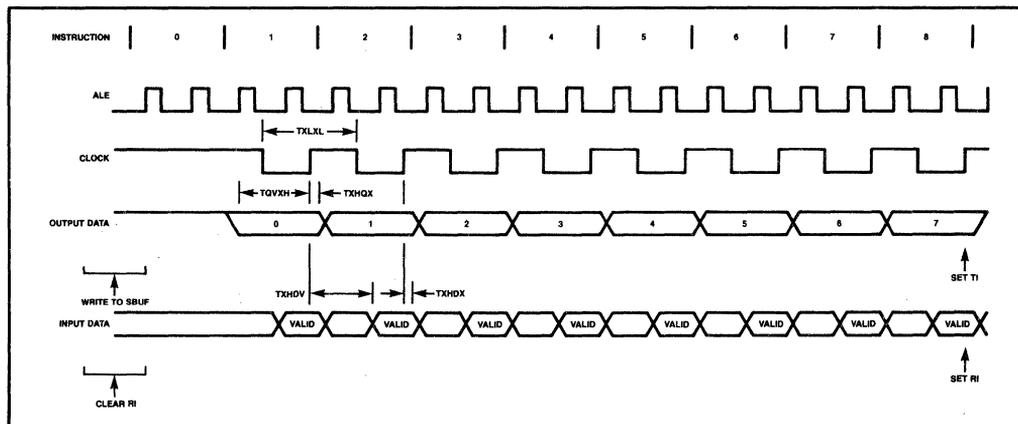


Table 2. MCS[®]-51 Instruction Set Description

ARITHMETIC OPERATIONS				LOGICAL OPERATIONS (CONTINUED)			
Mnemonic	Description	Byte	Cyc	Mnemonic	Destination	Byte	Cyc
ADD A,Rn	Add register to Accumulator	1	1	ORL A,@Ri	OR indirect RAM to Accumulator	1	1
ADD A,direct	Add direct byte to Accumulator	2	1	ORL A,#data	OR immediate data to Accumulator	2	1
ADD A,@Ri	Add indirect RAM to Accumulator	1	1	ORL direct,A	OR Accumulator to direct byte	2	1
ADD A,#data	Add immediate data to Accumulator	2	1	ORL direct,#data	OR immediate data to direct byte	3	2
ADDC A,Rn	Add register to Accumulator with Carry	1	1	XRL A,Rn	Exclusive-OR register to Accumulator	1	1
ADDC A,direct	Add direct byte to A with Carry flag	2	1	XRL A,direct	Exclusive-OR direct byte to Accumulator	2	1
ADDC A,@Ri	Add indirect RAM to A with Carry flag	1	1	XRL A,@Ri	Exclusive-OR indirect RAM to A	1	1
ADDC A,#data	Add immediate data to A with Carry flag	2	1	XRL A,#data	Exclusive-OR immediate data to A	2	1
SUBB A,Rn	Subtract register from A with Borrow	1	1	XRL direct,A	Exclusive-OR Accumulator to direct byte	2	1
SUBB A,direct	Subtract direct byte from A with Borrow	2	1	XRL direct,#data	Exclusive-OR immediate data to direct	3	2
SUBB A,@Ri	Subtract indirect RAM from A with Borrow	1	1	CLR A	Clear Accumulator	1	1
SUBB A,#data	Subtract immed data from A with Borrow	2	1	CPL A	Complement Accumulator	1	1
INC A	Increment Accumulator	1	1	RL A	Rotate Accumulator Left	1	1
INC Rn	Increment register	1	1	RLC A	Rotate A Left through the Carry flag	1	1
INC direct	Increment direct byte	2	1	RR A	Rotate Accumulator Right	1	1
INC @Ri	Increment indirect RAM	1	1	RRC A	Rotate A Right through Carry flag	1	1
INC DPTR	Increment Data Pointer	1	2	SWAP A	Swap nibbles within the Accumulator	1	1
DEC A	Decrement Accumulator	1	1				
DEC Rn	Decrement register	1	1				
DEC direct	Decrement direct byte	2	1				
DEC @Ri	Decrement indirect RAM	1	1				
MUL AB	Multiply A & B	1	4				
DIV AB	Divide A by B	1	4				
DA A	Decimal Adjust Accumulator	1	1				
LOGICAL OPERATIONS				DATA TRANSFER			
Mnemonic	Destination	Byte	Cyc	Mnemonic	Description	Byte	Cyc
ANL A,Rn	AND register to Accumulator	1	1	MOV A,Rn	Move register to Accumulator	1	1
ANL A,direct	AND direct byte to Accumulator	2	1	MOV A,direct	Move direct byte to Accumulator	2	1
ANL A,@Ri	AND indirect RAM to Accumulator	1	1	MOV A,@Ri	Move indirect RAM to Accumulator	1	1
ANL A,#data	AND immediate data to Accumulator	2	1	MOV A,#data	Mov immediate data to Accumulator	2	1
ANL direct,A	AND Accumulator to direct byte	2	1	MOV Rn,A	Move Accumulator to register	1	1
ANL direct,#data	AND immediate data to direct byte	3	2	MOV Rn,direct	Move direct byte to register	2	2
ORL A,Rn	OR register to Accumulator	1	1	MOV Rn,#data	Move immediate data to register	2	1
ORL A,direct	OR direct byte to Accumulator	2	1	MOV direct,A	Move Accumulator to direct byte	2	1
				MOV direct,Rn	Move register to direct byte	2	2
				MOV direct,direct	Move direct byte to direct	3	2
				MOV direct,@Ri	Move indirect RAM to direct byte	2	2

Table 2. MCS[®]-51 Instruction Set Description (Continued)

DATA TRANSFER (CONTINUED)			
Mnemonic	Description	Byte	Cyc
MOV direct,#data	Move immediate data to direct byte	3	2
MOV @Ri,A	Move Accumulator to indirect RAM	1	1
MOV @Ri,direct	Move direct byte to indirect RAM	2	2
MOV @Ri,#data	Move immediate data to indirect RAM	2	1
MOV DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2
MOVC A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX @Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX @DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A,Rn	Exchange register with Accumulator	1	1
XCH A,direct	Exchange direct byte with Accumulator	2	1
XCH A,@Ri	Exchange indirect RAM with A	1	1
XCHD A,@Ri	Exchange low-order Digit ind RAM w A	1	1
BOOLEAN VARIABLE MANIPULATION			
Mnemonic	Description	Byte	Cyc
CLR C	Clear Carry flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry flag	1	1
SETB bit	Set direct Bit	2	1
CPL C	Complement Carry flag	1	1
CPL bit	Complement direct bit	2	1
ANL C,bit	AND direct bit to Carry flag	2	2
ANL C,/bit	AND complement of direct bit to Carry	2	2
ORL C/bit	OR direct bit to Carry flag	2	2
ORL C,/bit	OR complement of direct bit to Carry	2	2
MOV C,/bit	Move direct bit to Carry flag	2	1
MOV bit,C	Move Carry flag to direct bit	2	2

PROGRAM AND MACHINE CONTROL			
Mnemonic	Description	Byte	Cyc
ACALL addr11	Absolute Subroutine Call	2	2
LCALL addr16	Long Subroutine Call	3	2
RET	Return from subroutine	1	2
RETI	Return from interrupt	1	2
AJMP addr11	Absolute Jump	2	2
LJMP addr16	Long Jump	3	2
SJMP rel	Short Jump (relative addr)	2	2
JMP @A+DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is Zero	2	2
JNZ rel	Jump if Accumulator is Not Zero	2	2
JC rel	Jump if Carry flag is set	2	2
JNC rei	Jump if No Carry flag	2	2
JB bit,rel	Jump if direct Bit set	3	2
JNB bit,rel	Jump if direct Bit Not set	3	2
JBC bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE A,#data,rel	Comp, immed, to A & Jump if Not Equal	3	2
CJNE Rn,#data,rel	Comp, immed, to reg & Jump if Not Equal	3	2
CJNE @Ri,#data,rel	Comp, immed, to ind, & Jump if Not Equal	3	2
DJNZ Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP	No operation	1	1
Notes on data addressing modes:			
Rn	—Working register R0–R7		
direct	—128 internal RAM locations, any I/O port, control or status register		
@Ri	—Indirect internal RAM location addressed by register R0 or R1		
#data	—8-bit constant included in instruction		
#data16	—16-bit constant included as bytes 2 & 3 of instruction		
bit	—128 software flags, any I/O pin, control or status bit		
Notes on program addressing modes:			
addr16	—Destination address for LCALL & LJMP may be anywhere within the 64-K program memory address space		
Addr11	—Destination address for ACALL & AJMP will be within the same 2-K page of program memory as the first byte of the following instruction		
rel	—SJMP and all conditional jumps include an 8-bit offset byte. Range is +127–128 bytes relative to first byte of the following instruction		
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Table 3. Instruction Opcodes in Hexidecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	code addr
02	3	LJMP	code addr
03	1	RR	A
04	1	INC	A
05	2	INC	data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	bit addr, code addr
11	2	ACALL	code addr
12	3	LCALL	code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	bit addr, code addr
21	2	AJMP	code addr
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,data addr
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	bit addr, code addr
31	2	ACALL	code addr
32	1	RETI	

Hex Code	Number of Bytes	Mnemonic	Operands
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,data addr
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	code addr
41	2	AJMP	code addr
42	2	ORL	data addr,A
43	3	ORL	data addr,#data
44	2	ORL	A,#data
45	2	ORL	A,data addr
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	code addr
51	2	ACALL	code addr
52	2	ANL	data addr,A
53	3	ANL	data addr,#data
54	2	ANL	A,#data
55	2	ANL	A,data addr
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	code addr
61	2	AJMP	code addr
62	2	XRL	data addr,A
63	3	XRL	data addr,#data
64	2	XRL	A,#data
65	2	XRL	A,data addr

Table 3. Instruction Opcodes in Hexidecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C,bit addr
73	1	JMP	@A+DPTR
74	2	MOV	A,#data
75	3	MOV	data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	data addr, data addr
86	2	MOV	data addr,@R0
87	2	MOV	data addr,@R1
88	2	MOV	data addr,R0
89	2	MOV	data addr,R1
8A	2	MOV	data addr,R2
8B	2	MOV	data addr,R3
8C	2	MOV	data addr,R4
8D	2	MOV	data addr,R5
8E	2	MOV	data addr,R6
8F	2	MOV	data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	code addr
92	2	MOV	bit addr,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0

Hex Code	Number of Bytes	Mnemonic	Operands
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/bit addr
A1	2	AJMP	code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,/bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Table 3. Instruction Opcodes in Hexidecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr

Hex Code	Number of Bytes	Mnemonic	Operands
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

80C86/80C86-2

16-Bit CHMOS Microprocessor

- Pin-for-Pin and Functionally Compatible to Industry Standard HMOS 8086
- Fully Static Design with Frequency Range from D.C. to:
 - 5 MHz for 80C86
 - 8 MHz for 80C86-2
- Low Power Operation
 - Operating $I_{CC} = 10 \text{ mA/MHz}$
 - Standby $I_{CCS} = 500 \mu\text{A max}$
- Bus-Hold Circuitry Eliminates Pull-Up Resistors
- Direct Addressing Capability of 1 MByte of Memory
- Architecture Designed for Powerful Assembly Language and Efficient High Level Languages
- 24 Operand Addressing Modes
- Byte, Word and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic
 - Binary or Decimal
 - Multiply and Divide

The Intel 80C86 is a high performance, CHMOS version of the industry standard HMOS 8086 16-bit CPU. It is available in 5 MHz clock rate and will be available in 8 MHz clock rate in the 2nd half of 1985. The 80C86 offers two modes of operation: MINimum for small systems and MAXimum for larger applications such as multi-processing. It is available in 40-pin DIP and will be available in 44-pin plastic leaded chip carrier (PLCC) package in the 2nd half of 1985.

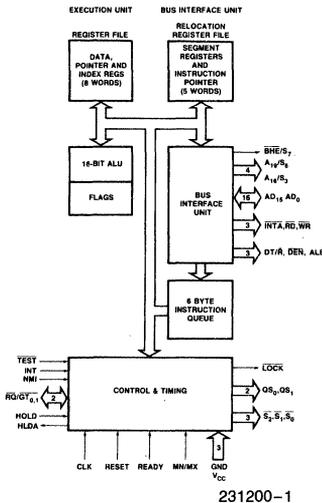


Figure 1. 80C86 CPU Block Diagram

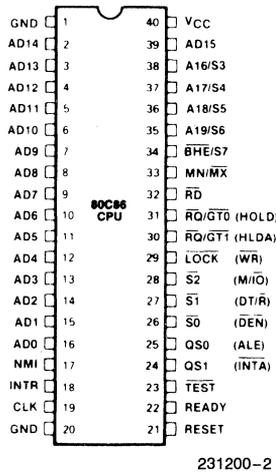


Figure 2a. 80C86 40-Lead DIP Configuration

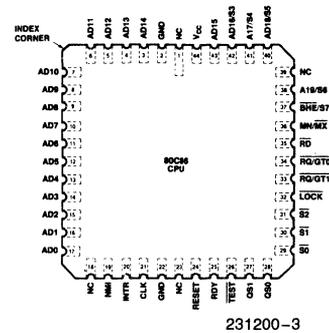


Figure 2b. 80C86 44-Lead PLCC Configuration

Table 1. Pin Description

The following pin function descriptions are for 80C86 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 80C86 (without regard to additional bus buffers).

Symbol	Pin No.	Type	Name and Function																		
AD ₁₅ -AD ₀	2-16, 39	I/O	<p>ADDRESS DATA BUS: These lines constitute the time multiplexed memory/I/O address (T₁) and data (T₂, T₃, T_W, T₄) bus. A₀ is analogous to BHE for the lower byte of the data bus, pins D₇-D₀. It is LOW during T₁ when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A₀ to condition chip select functions. (See BHE.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge."</p>																		
A ₁₉ /S ₆ , A ₁₈ /S ₅ , A ₁₇ /S ₄ , A ₁₆ /S ₃	35-38	O	<p>ADDRESS/STATUS: During T₁ these are the four most significant address lines for memory/operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T₂, T₃, T_W, and T₄. The status of the interrupt enable FLAG bit (S₅) is updated at the beginning of each CLK cycle. A₁₇/S₄ and A₁₆/S₃ are encoded as shown.</p> <p>This information indicates which relocation register is presently being used for data accessing.</p> <p>These lines float to 3-state OFF during local bus "hold acknowledge."</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%;">A₁₇/S₄</th> <th style="width: 33%;">A₁₆/S₃</th> <th style="width: 33%;">Characteristics</th> </tr> </thead> <tbody> <tr> <td>0 (LOW)</td> <td>0</td> <td>Alternate Data</td> </tr> <tr> <td>0</td> <td>1</td> <td>Stack</td> </tr> <tr> <td>1 (HIGH)</td> <td>0</td> <td>Code or None</td> </tr> <tr> <td>1</td> <td>1</td> <td>Data</td> </tr> <tr> <td colspan="3">S₆ is 0 (LOW)</td> </tr> </tbody> </table>	A ₁₇ /S ₄	A ₁₆ /S ₃	Characteristics	0 (LOW)	0	Alternate Data	0	1	Stack	1 (HIGH)	0	Code or None	1	1	Data	S ₆ is 0 (LOW)		
A ₁₇ /S ₄	A ₁₆ /S ₃	Characteristics																			
0 (LOW)	0	Alternate Data																			
0	1	Stack																			
1 (HIGH)	0	Code or None																			
1	1	Data																			
S ₆ is 0 (LOW)																					
BHE/S ₇	34	O	<p>BUS HIGH ENABLE/STATUS: During T₁ the bus high enable signal (BHE) should be used to enable data onto the most significant half of the data bus, pins D₁₅-D₈. Eight-bit oriented devices tied to the upper half of the bus would normally use BHE to condition chip select functions. BHE is LOW during T₁ for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S₇ status information is available during T₂, T₃, and T₄. The signal is active LOW, and floats to 3-state OFF in "hold." It is LOW during T₁ for the first interrupt acknowledge cycle.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%;">BHE</th> <th style="width: 33%;">A₀</th> <th style="width: 33%;">Characteristics</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Whole word</td> </tr> <tr> <td>0</td> <td>1</td> <td>Upper byte from/ to odd address</td> </tr> <tr> <td>1</td> <td>0</td> <td>Lower byte from/ to even address</td> </tr> <tr> <td>1</td> <td>1</td> <td>None</td> </tr> </tbody> </table>	BHE	A ₀	Characteristics	0	0	Whole word	0	1	Upper byte from/ to odd address	1	0	Lower byte from/ to even address	1	1	None			
BHE	A ₀	Characteristics																			
0	0	Whole word																			
0	1	Upper byte from/ to odd address																			
1	0	Lower byte from/ to even address																			
1	1	None																			

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
\overline{RD}	32	O	<p>READ: Read strobe indicates that the processor is performing a memory of I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the 80C86 local bus. \overline{RD} is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 80C86 local bus has floated.</p> <p>This floats to 3-state OFF in "hold acknowledge."</p>
READY	22	I	<p>READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/IO is synchronized by the 82C84A Clock Generator to form READY. This signal is active HIGH. The 80C86 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.</p>
INTR	18	I	<p>INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</p>
\overline{TEST}	23	I	<p>TEST: input is examined by the "Wait" instruction. If the \overline{TEST} input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.</p>
NMI	17	I	<p>NON-MASKABLE INTERRUPT: an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.</p>
RESET	21	I	<p>RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.</p>
CLK	19	I	<p>CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.</p>
V_{CC}	40		<p>V_{CC}: +5V power supply pin.</p>
GND	1, 20		<p>GROUND</p>
MN/\overline{MX}	33	I	<p>MINIMUM/MAXIMUM: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.</p>

Table 1. Pin Description (Continued)

The following pin function descriptions are for the 80C86/82C88 system in maximum mode (i.e., $MN/\overline{MX} = V_{SS}$). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

Symbol	Pin No.	Type	Name and Function																																	
$\overline{S_2}, \overline{S_1}, \overline{S_0}$	26-28	O	<p>STATUS: active during T_4, T_1, and T_2 and is returned to the passive state (1,1,1) during T_3 or during T_W when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}, \overline{S_1}, \overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.</p> <p>These signals float to 3-state OFF in "hold acknowledge." These status lines are encoded as shown.</p>																																	
			<table border="1"> <thead> <tr> <th>$\overline{S_2}$</th> <th>$\overline{S_1}$</th> <th>$\overline{S_0}$</th> <th>Characteristics</th> </tr> </thead> <tbody> <tr> <td>0 (LOW)</td> <td>0</td> <td>0</td> <td>Interrupt Acknowledge</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Read I/O Port</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Write I/O Port</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Halt</td> </tr> <tr> <td>1 (HIGH)</td> <td>0</td> <td>0</td> <td>Code Access</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Read Memory</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Write Memory</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Passive</td> </tr> </tbody> </table>	$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics	0 (LOW)	0	0	Interrupt Acknowledge	0	0	1	Read I/O Port	0	1	0	Write I/O Port	0	1	1	Halt	1 (HIGH)	0	0	Code Access	1	0	1	Read Memory	1	1	0	Write Memory	1
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics																																	
0 (LOW)	0	0	Interrupt Acknowledge																																	
0	0	1	Read I/O Port																																	
0	1	0	Write I/O Port																																	
0	1	1	Halt																																	
1 (HIGH)	0	0	Code Access																																	
1	0	1	Read Memory																																	
1	1	0	Write Memory																																	
1	1	1	Passive																																	
$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$	30, 31	I/O	<p>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see Figure 9):</p> <ol style="list-style-type: none"> 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 80C86 (pulse 1). 2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the 80C86 to the requesting master (pulse 2), indicates that the 80C86 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge." 3. A pulse 1 CLK wide from the requesting master indicates to the 80C86 (pulse 3) that the "hold" request is about to end and that 80C86 can reclaim the local bus at the next CLK. <p>Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> 1. Request occurs on or before T_2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. 																																	

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function															
			<p>If the local bus is idle when the request is made the two possible events will follow:</p> <ol style="list-style-type: none"> 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied. 															
$\overline{\text{LOCK}}$	29	O	<p>LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active LOW. The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge."</p>															
QS ₁ , QS ₀	24, 25	O	<p>QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS₁ and QS₀ provide status to allow external tracking of the internal 80C86 instruction queue.</p> <table border="1"> <thead> <tr> <th>QS₁</th> <th>QS₀</th> <th>Characteristics</th> </tr> </thead> <tbody> <tr> <td>0 (LOW)</td> <td>0</td> <td>No Operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>First Byte of Op Code from Queue</td> </tr> <tr> <td>1 (HIGH)</td> <td>0</td> <td>Empty the Queue</td> </tr> <tr> <td>1</td> <td>1</td> <td>Subsequent Byte from Queue</td> </tr> </tbody> </table>	QS ₁	QS ₀	Characteristics	0 (LOW)	0	No Operation	0	1	First Byte of Op Code from Queue	1 (HIGH)	0	Empty the Queue	1	1	Subsequent Byte from Queue
QS ₁	QS ₀	Characteristics																
0 (LOW)	0	No Operation																
0	1	First Byte of Op Code from Queue																
1 (HIGH)	0	Empty the Queue																
1	1	Subsequent Byte from Queue																

The following pin function descriptions are for the 80C86 in minimum mode (i.e., $MN/\overline{MX} = V_{CC}$). Only the pin functions which are unique to minimum mode are described; all other pin functions are described above.

$M/\overline{\text{IO}}$	28	O	<p>STATUS LINE: logically equivalent to S₂ in the maximum mode. It is used to distinguish a memory access from an I/O access. $M/\overline{\text{IO}}$ becomes valid in the T₄ preceding a bus cycle and remains valid until the final T₄ of the cycle (M = HIGH, IO = LOW). $M/\overline{\text{IO}}$ floats to 3-state OFF in local bus "hold acknowledge."</p>
$\overline{\text{WR}}$	29	O	<p>WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the $M/\overline{\text{IO}}$ signal. $\overline{\text{WR}}$ is active for T₂, T₃ and T_W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge."</p>
$\overline{\text{INTA}}$	24	O	<p>$\overline{\text{INTA}}$ is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T₂, T₃ and T_W of each interrupt acknowledge cycle.</p>
ALE	25	O	<p>ADDRESS LATCH ENABLE: provided by the processor to latch the address into an address latch. It is a HIGH pulse active during T₁ of any bus cycle. Note that ALE is never floated.</p>
DT/ $\overline{\text{R}}$	27	O	<p>DATA TRANSMIT/RECEIVE: needed in minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{\text{R}}$ is equivalent to S₁ in the maximum mode, and its timing is the same as for $M/\overline{\text{IO}}$. (T = HIGH, R = LOW.) This signal floats to 3-state OFF in local bus "hold acknowledge."</p>

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{\text{DEN}}$	26	O	DATA ENABLE: provided as an output enable for the transceiver in a minimum system which uses the transceiver. $\overline{\text{DEN}}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T_2 until the middle of T_4 , while for a write cycle it is active from the beginning of T_2 until the middle of T_4 . $\overline{\text{DEN}}$ floats to 3-state OFF in local bus "hold acknowledge."
HOLD, HLDA	31, 30	I/O	HOLD: indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T_1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWER the HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. The same rules as for $\overline{\text{RQ}}/\overline{\text{GT}}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

FUNCTIONAL DESCRIPTION

STATIC OPERATION

All 80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C86 can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the 80C86 power requirement is the standby current (500 μA maximum).

INTERNAL ARCHITECTURE

The internal functions of the 80C86 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte in the queue immediately becomes available to

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

The execution units receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description for further register set and architectural descriptions.

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64k bytes each, with each segment falling on 16-byte boundaries. (See Figure 3a.)

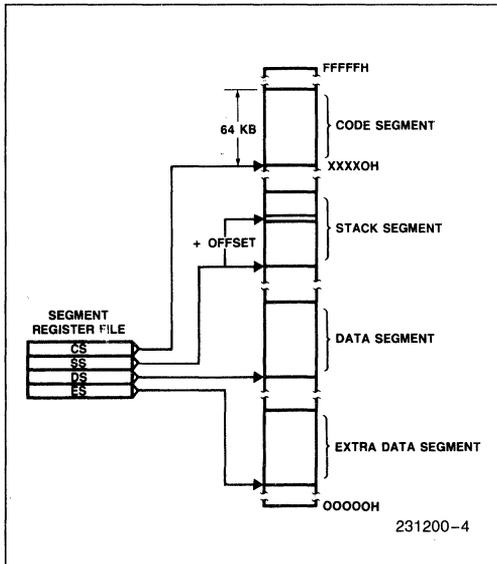


Figure 3a. Memory Organization

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands.

Physically, the memory is organized as a high bank (D₁₅-D₈) and a low bank (D₇-D₀) of 512k 8-bit bytes addressed in parallel by the processor's address lines.

A₁₉-A₁. Byte data with even addresses is transferred on the D₇-D₀ bus lines while odd addressed byte data (A₀ HIGH) is transferred on the D₁₅-D₈ bus lines. The processor provides two enable signals, \overline{BHE} and A₀, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

In referencing word data the BIU requires one or two memory cycles depending on whether or not the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing

word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (see Figure 3b.) Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

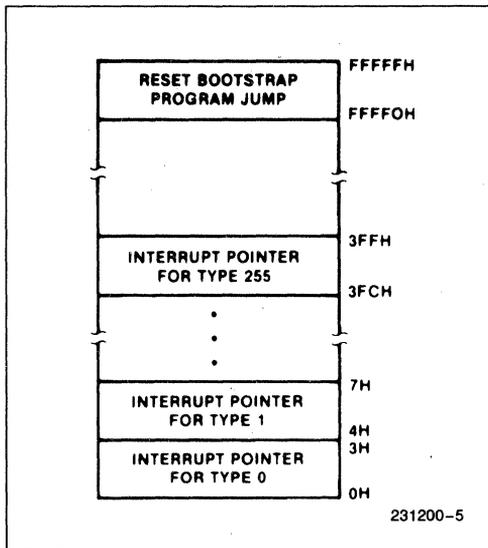


Figure 3b. Reserved Memory Locations

MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum 80C86 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 80C86 is equipped with a strap pin (MN/MX) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When MN/MX pin is strapped to GND, the 80C86 treats pins 24 through 31 in maximum mode. An 82C88 bus controller interprets status information coded into \overline{S}_0 , \overline{S}_1 , \overline{S}_2 to generate bus timing and control signals compatible with the MULTIBUS[®] architecture. When the MN/MX pin is strapped to V_{CC}, the 80C86 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 2. Examples of minimum mode and maximum mode systems are shown in Figure 4.

BUS OPERATION

The 80C86 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T₁, T₂, T₃ and T₄ (see Figure 5). The address is emitted from the processor during T₁ and data transfer occurs on the bus during T₃ and T₄. T₂ is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_W) are inserted between T₃ and T₄. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods can occur between 80C86 bus cycles. These are referred to as "Idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T₁ of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/MX strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

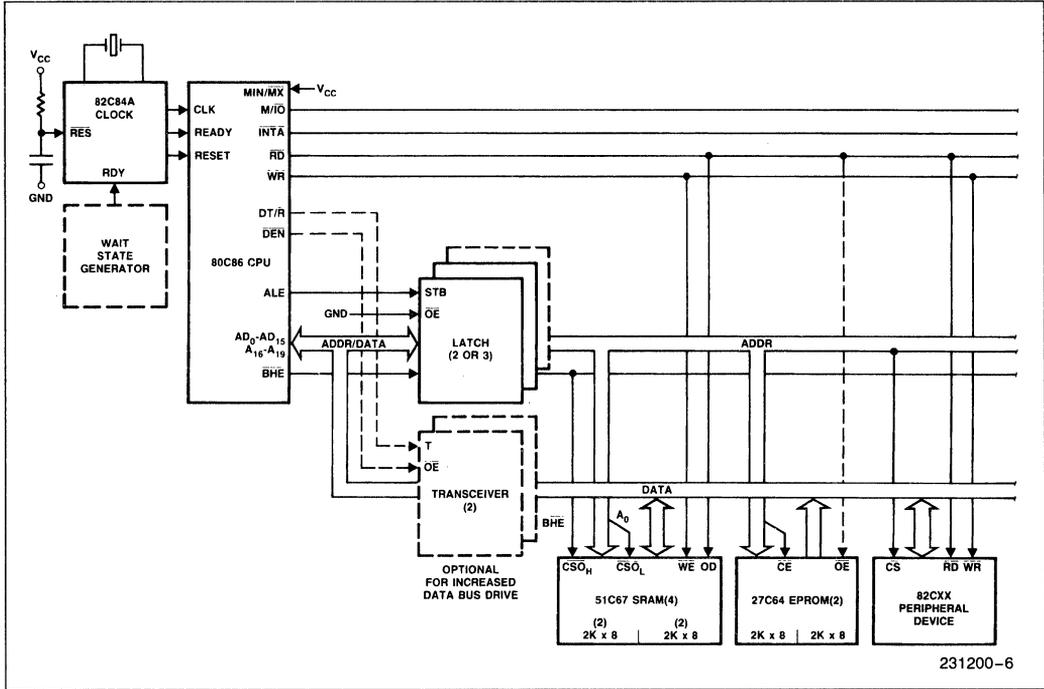


Figure 4a. Minimum Mode iAPX 80C86 Typical Configuration

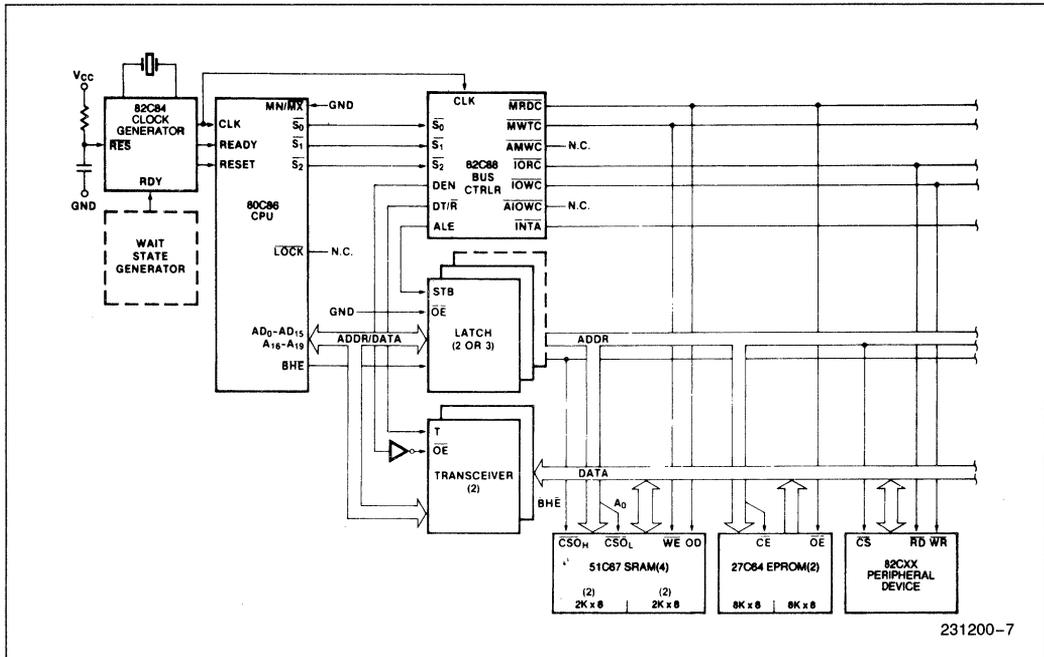
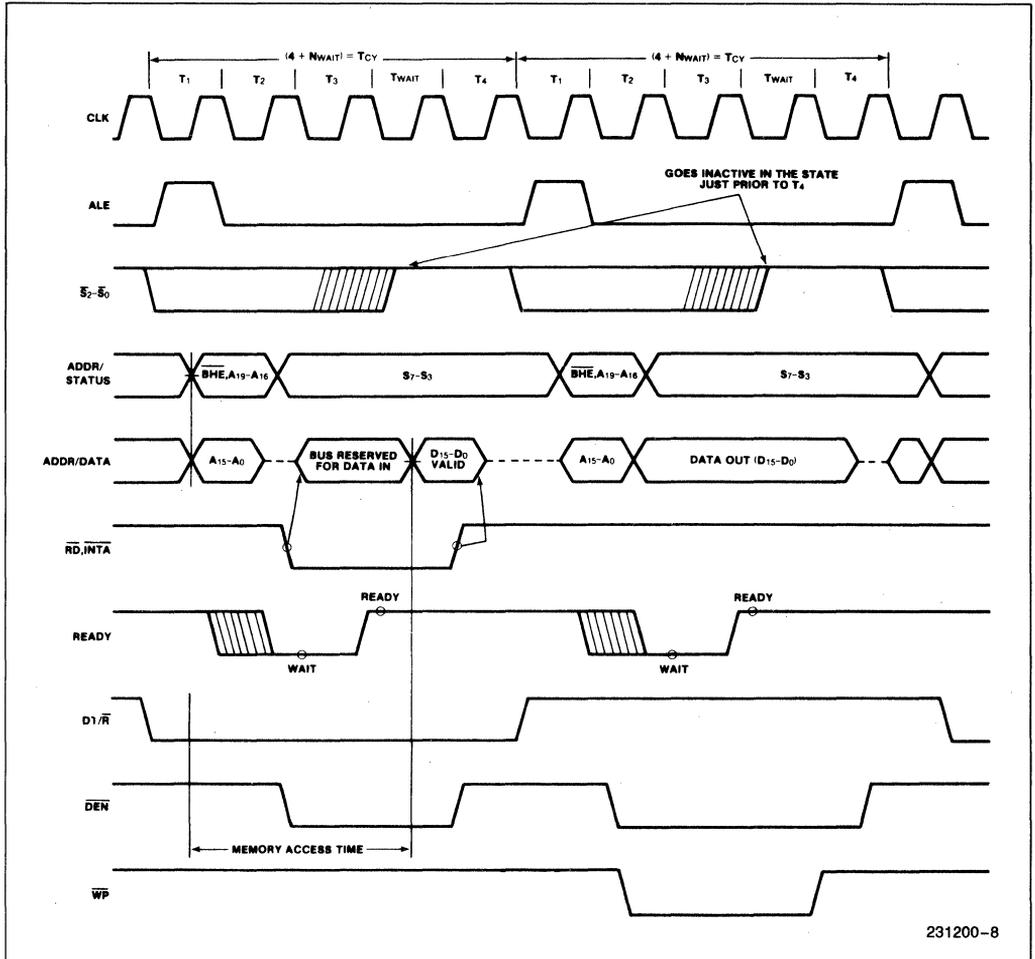


Figure 4b. Maximum Mode 80C86 Typical Configuration



231200-8

Figure 5. Basic System Timing

Status bits $\bar{S}_0, \bar{S}_1,$ and \bar{S}_2 are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

\bar{S}_2	\bar{S}_1	\bar{S}_0	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

therefore valid during T_2 through T_4 . S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

S_4	S_3	Characteristics
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. $S_6 = 0$ and S_7 is a space status bit.

Status bits S_3 through S_7 are multiplexed with high-order address bits and the \overline{BHE} signal, and are

I/O ADDRESSING

In the 80C86, I/O operations can address up to a maximum of 64k I/O byte registers or 32k I/O word registers. The I/O address appears in the same format as the memory address on bus lines A₁₅-A₀. The address lines A₁₉-A₁₆ are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D₇-D₀ bus lines and odd addressed bytes on D₁₅-D₈. Care must be taken to assure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

EXTERNAL INTERFACE

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C86 RESET is required to be HIGH for greater than 4 CLK cycles. The 80C86 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset se-

quence for approximately 10 CLK cycles. After this interval the 80C86 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 3b). The details of this operation are specified in the Instruction Set description of the MCS[®]-86 Family User's Manual. The RESET input is internally synchronized to the processor clock. At initialization the HIGH-to-LOW transition of RESET must occur no sooner than 50 μs after power-up, to allow complete initialization of the 80C86.

NMI may not be asserted prior to the 2nd CLK cycle following the end of RESET.

BUS HOLD CIRCUITRY

To avoid high current conditions caused by floating inputs to CMOS devices and eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on the 80C86 pins 2-16, 26-32, and 34-39 (Figures 6a, 6b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400 μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

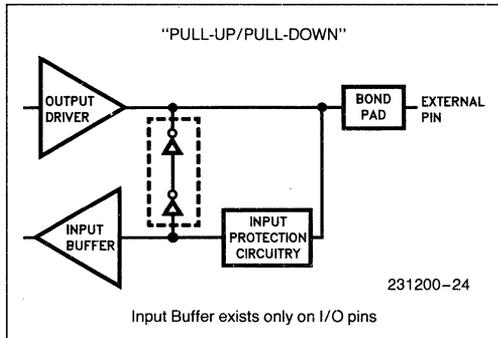


Figure 6a. Bus hold circuitry pin 2-16, 34-39.

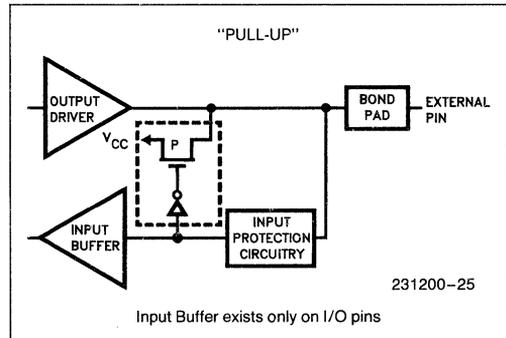


Figure 6b. Bus hold circuitry pin 26-32.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 3b), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. (See Instruction Set description.) NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs af-

ter the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The 80C86 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 7) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C86 emits the LOCK signal from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle a byte is fetched from the external interrupt system (e.g., 82C59 PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

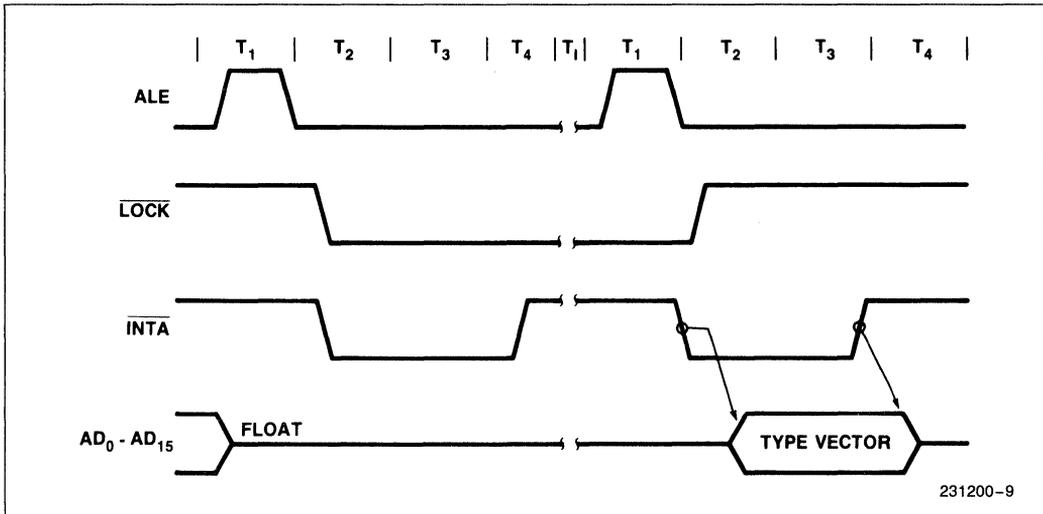


Figure 7. Interrupt Acknowledge Sequence

HALT

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In Maximum Mode, the processor issues appropriate HALT status on \overline{S}_2 , \overline{S}_1 and \overline{S}_0 and the 82C88 bus controller issues one ALE. The 80C86 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An interrupt request or RESET will force the 80C86 out of the "HALT" state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The \overline{LOCK} status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This provides the processor with the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The \overline{LOCK} signal is activated (forced LOW) in the clock bus cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While \overline{LOCK} is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.

EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to the interrupts and general I/O capabilities, the 80C86 provides a single software-testable input known as the \overline{TEST} signal. At any time the program may execute a WAIT instruction. If at that time the \overline{TEST} signal is inactive (HIGH), program execution becomes suspended while the processor waits for \overline{TEST} to become active. It must remain active for at least 5 CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in an idle state while waiting. All 80C86 drivers go to 3-state OFF if bus "Hold" is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction one extra time, processes the interrupt, and then re-fetches and re-executes the WAIT instruction upon returning from the interrupt.

BASIC SYSTEM TIMING

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 4a and 4b, respectively. In minimum mode, the MN/MX pin is strapped to V_{CC} and the processor emits bus control signals in a manner similar to the 8085. In maximum mode, the MN/MX pin is strapped to V_{SS} and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS compatible bus control signals. Figure 5 illustrates the signal timing relationships.

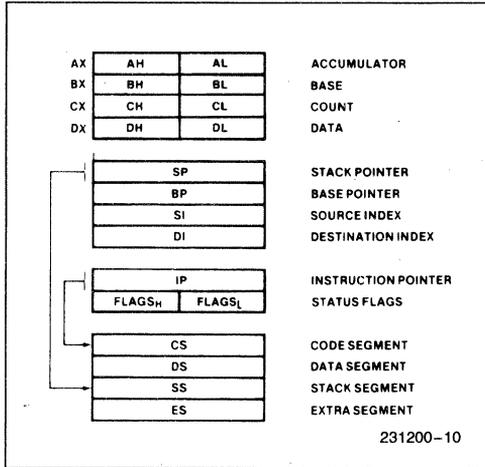


Figure 8. iAPX 80C86 Register Model

SYSTEM TIMING—MINIMUM SYSTEM

The read cycle begins in T_1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into a latch. The \overline{BHE} and A_0 signals address the low, high, or both bytes. From T_1 to T_4 the M/\overline{IO} signal indicates a memory or I/O operation. At T_2 the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at T_2 . The read (\overline{RD}) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later valid data will be available on the bus and the addressed device will drive the \overline{READY} line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver is required to buffer the 80C86 local bus, signals $\overline{DT}/\overline{R}$ and \overline{DEN} are provided by the 80C86.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/\overline{IO} signal is again asserted to indicate a memory or I/O write operation. In the T_2 immediately following the address emission the processor emits the data to be written into the addressed location. This data remains valid until the middle of T_4 . During T_2 , T_3 , and T_4 the processor asserts the write control signal. The write (\overline{WR}) signal becomes active at the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for the bus to float.

The \overline{BHE} and A_0 signals are used to select the proper byte(s) of the memory/I/O word to be read or written according to the following table:

\overline{BHE}	A_0	Characteristics
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D_7 - D_0 bus lines and odd addressed bytes on D_{15} - D_8 .

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal (\overline{INTA}) is asserted in place of the read (\overline{RD}) signal and the address bus is floated. (See Figure 7.) In the second of two successive \overline{INTA} cycles, a byte of information is read from bus lines D_7 - D_0 as supplied by the interrupt system logic (i.e., 82C59A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

BUS TIMING—MEDIUM SIZE SYSTEMS

For medium size systems the MN/\overline{MX} pin is connected to V_{SS} and the 82C88 Bus Controller is added to the system as well as a latch for latching the system address, and a transceiver to allow for bus loading greater than the 80C86 is capable of handling. Signals ALE, \overline{DEN} , and $\overline{DT}/\overline{R}$ are generated by the 82C88 instead of the processor in this configuration although their timing remains relatively the same. The 80C86 status outputs (\overline{S}_2 , \overline{S}_1 , and \overline{S}_0) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence data isn't valid at the leading edge of write. The transceiver receives the usual T and OE inputs from the 82C88 $\overline{DT}/\overline{R}$ and \overline{DEN} .

The pointer into the interrupt vector table, which is passed during the second \overline{INTA} cycle, can derive from an 82C59A located on either the local bus or the system bus. If the master 82C59A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the transceiver when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (With respect to ground)	-0.5 to 8.0V
Operating Supply Voltage (w.r.t. ground)	4.0 to 7.0V
Input Voltage Applied (w.r.t. ground)	-2.0 to $V_{CC} + 0.5V$
Output Voltage Applied (w.r.t. ground)	-0.5 to $V_{CC} + 0.5V$
Power Dissipation	1.0W
Storage Temperature	-65°C to 150°C
Ambient Temperature Under Bias	0°C to 70°C

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS (80C86: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 10\%$)
 (80C86-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.5 \text{ mA}$
V_{OH}	Output High Voltage	3.0 $V_{CC} - 0.4$		V	$I_{OH} = -2.5 \text{ mA}$ $I_{OH} = -100 \mu\text{A}$
I_{CC}	Power Supply Current		10 mA/MHz		$V_{IH} = \text{GND}$, $V_{IL} = V_{CC}$ $T_A = 25^\circ\text{C}$ $V_{CC} = 5.5V$
I_{CCS}	Standby Supply Current		500	μA	$V_{CC} = 5.5V$ $V_{IN}(\text{max}) = V_{CC}$ or GND Outputs Unloaded CLK = GND or V_{CC}
I_{LI}	Input Leakage Current		± 1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
I_{BHL}	Input Leakage Current (Bus Hold Low)	50	400	μA	$V_{IN} = 0.8V$ (Note 1)
I_{BHH}	Input Leakage Current (Bus Hold High)	-50	-400	μA	$V_{IN} = 3.0V$ (Note 2)
I_{BHLO}	Bus Hold Low Overdrive		600	μA	(Note 4)
I_{BHHO}	Bus Hold High Overdrive		-600	μA	(Note 5)
I_{LO}	Output Leakage Current		± 10	μA	$0V \leq V_{OUT} \leq V_{CC}$
V_{CL}	Clock Input Low Voltage	-0.5	+0.8	V	
V_{CH}	Clock Input High Voltage	$V_{CC} - 0.8$	$V_{CC} + 0.5$	V	
C_{IN}	Capacitance of Input Buffer (All input except AD ₀ -AD ₁₅ , RQ/GT)		5	pF	(Note 3)
C_{IO}	Capacitance of I/O Buffer (AD ₀ -AD ₁₅ , RQ/GT)		20	pF	(Note 3)
C_{OUT}	Output Capacitance		15	pF	(Note 3)

NOTES:

- Test condition is to lower V_{IN} to GND and then raise V_{IN} to 0.8V on pins 2-16, 26-32, and 34-39.
- Test condition is to raise V_{IN} to V_{CC} and then lower V_{IN} to 3.0V on pins 2-16, 26-32, and 34-39.
- Test conditions are a) Frequency = 1 MHz
b) Unmeasured pins at GND
c) V_{IN} at +5.0V or GND.
- An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.
- An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.

A.C. CHARACTERISTICS (80C86: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$)
 (80C86-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	80C86		80C86-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	D.C.	125	D.C.	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	$C_L = 20\text{--}100\text{ pF}$
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84A (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84A (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C86	118		68		ns	
TCHRYX	READY Hold Time into 80C86	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		-8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, TEST Setup Time (See Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V

A.C. CHARACTERISTICS (Continued)

Timing Responses

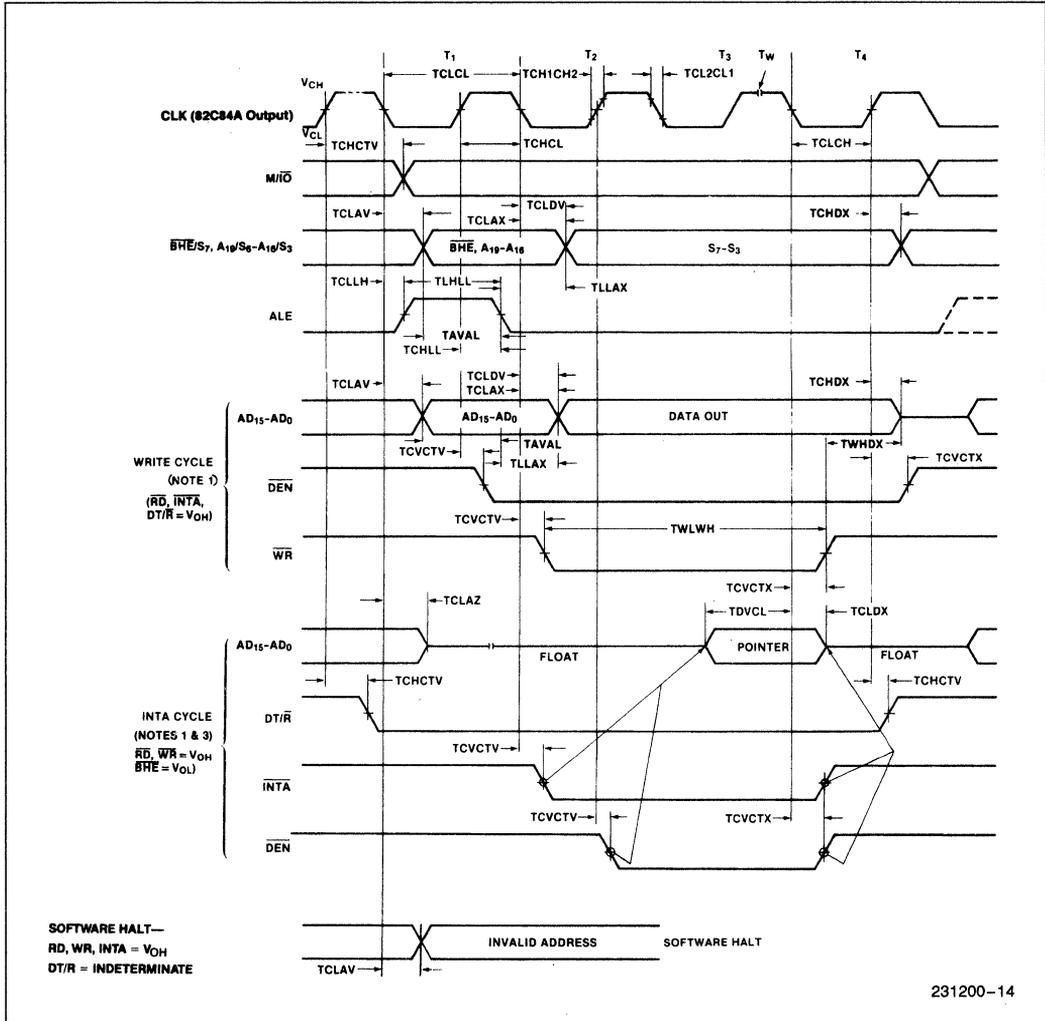
Symbol	Parameter	80C86		80C86-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLAV	Address Valid Delay	10	110	10	60	ns	*C _L = 20–100 pF for all 80C86 Outputs (in addition to 80C86 self-load)
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH – 20		TCLCH – 10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL – 10		TCHCL – 10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After WR	TCLCH – 30		TCLCH – 30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	\overline{RD} Active Delay	10	165	10	100	ns	
TCLRH	\overline{RD} Inactive Delay	10	150	10	80	ns	
TRHAV	\overline{RD} Inactive to Next Address Active	TCLCL – 45		TCLCL – 40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	\overline{RD} Width	2TCLCL – 75		2TCLCL – 50		ns	
TWLWH	WR Width	2TCLCL – 60		2TCLCL – 40		ns	
TAVAL	Address Valid to ALE Low	TCLCH – 60		TCLCH – 40		ns	
TOLOH	Output Rise Time		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns	From 2.0V to 0.8V

NOTES:

- Signal at 82C84A shown for reference only.
- Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
- Applies only to T2 state. (8 ns into T3).

WAVEFORMS (Continued)

MINIMUM MODE (Continued)



NOTES:

1. All timing measurements are made at V_{OH} and V_{OL} .
2. \overline{RDY} is sampled near the end of T_2, T_3, T_w to determine if T_w machine states are to be inserted.
3. Two \overline{INTA} cycles run back-to-back. The 80C86 LOCAL ADDR/DATA BUS is floating during both \overline{INTA} cycles. Control signals shown for second \overline{INTA} cycle.
4. Signals at 82C84A are shown for reference only.

A.C. CHARACTERISTICS
**MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)
TIMING REQUIREMENTS**

Symbol	Parameter	80C86		80C86-2		Units	Test Conditions	
		Min	Max	Min	Max			
TCLCL	CLK Cycle Period	200	D.C.	125	D.C.	ns		
TCLCH	CLK Low Time	118		68		ns		
TCHCL	CLK High Time	69		44		ns		
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V	
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V	
TDVCL	Data in Setup Time	30		20		ns	$C_L = 20-100 \text{ pF}$	
TCLDX	Data in Hold Time	10		10		ns		
TR1VCL	RDY Setup Time into 82C84A (Notes 1, 2)	35		35		ns		
TCLR1X	RDY Hold Time into 82C84A (Notes 1, 2)	0		0		ns		
TRYHCH	READY Setup Time into 80C86	118		68		ns		
TCHRYX	READY Hold Time into 80C86	30		20		ns		
TRYLCL	READY Inactive to CLK (Note 4)	-8		-8		ns		
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (Note 2)	30		15		ns		
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	30		15		ns		
TCHGX	\overline{RQ} Hold Time into 80C86	40		30		ns		
TILIH	Input Rise Time (Except CLK)		15		15	ns		From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns		From 2.0V to 0.8V

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	80C86		80C86-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLML	Command Active Delay (Note 1)	5	35	5	35	ns	C _L = 20–100 pF for all 80C86 Outputs (in addition to 80C86 self-load)
TCLMH	Command Inactive Delay (Note 1)	5	35	5	35	ns	
TRYHSH	READY Active to Status Passive (Note 3)		110		65	ns	
TCHSV	Status Active Delay	10	110	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (Note 1)		20		20	ns	
TSVMCH	Status Valid to MCE High (Note 1)		30		30	ns	
TCLLH	CLK Low to ALE Valid (Note 1)		15		15	ns	
TCLMCH	CLK Low to MCE High (Note 1)		25		25	ns	
TCHLL	ALE Inactive Delay (Note 1)	4	18	4	18	ns	
TCLMCL	MCE Inactive Delay (Note 1)		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (Note 1)	5	45	5	45	ns	
TCVNX	Control Inactive Delay (Note 1)	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		ns	
TCLRL	RD Active Delay	10	165	10	100	ns	
TCLRH	RD Inactive Delay	10	150	10	80	ns	

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES (Continued)

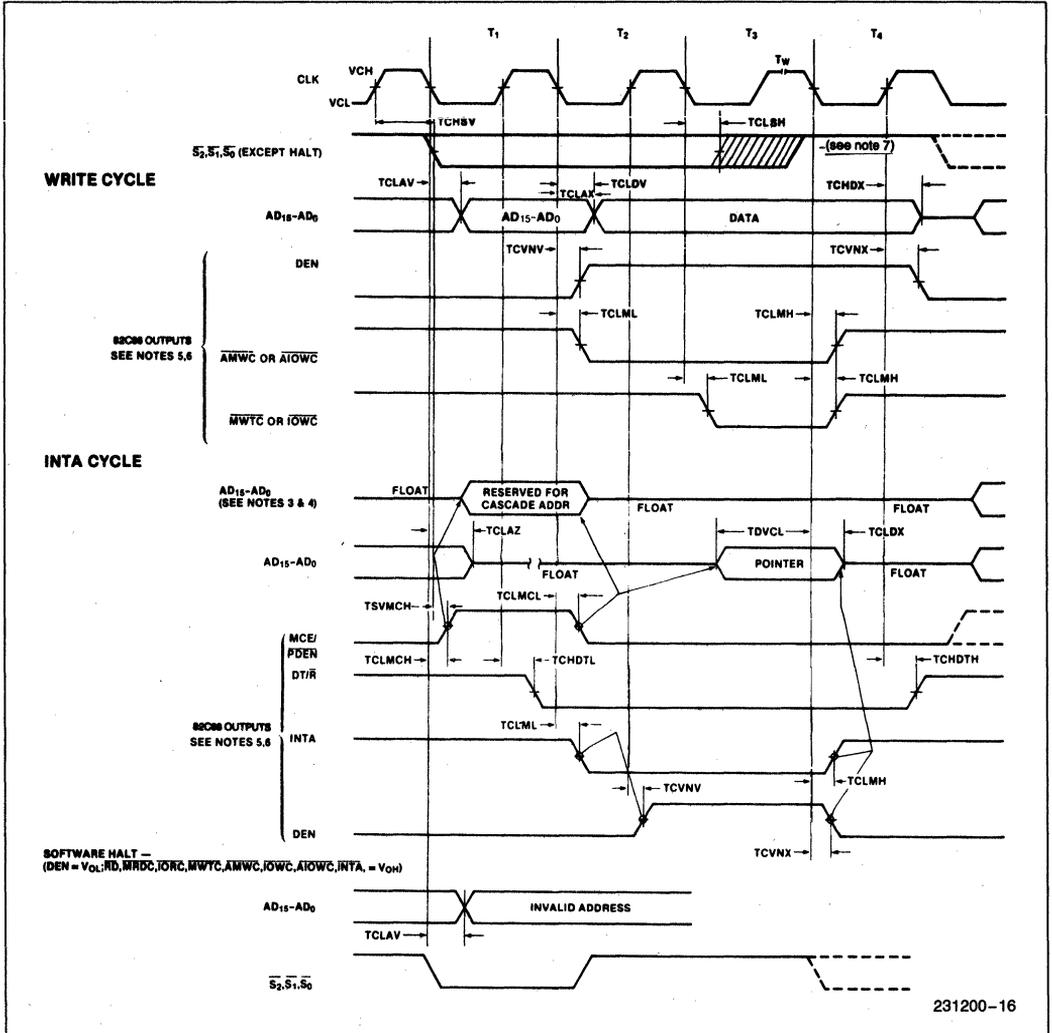
Symbol	Parameter	80C86		80C86-2		Units	Test Conditions
		Min	Max	Min	Max		
TRHAV	RD Inactive to Next Address Active	TCLCL - 45		TCLCL - 40		ns	C _L = 20-100 pF for all 80C86 Outputs (in addition to 80C86 self-load)
TCHDTL	Direction Control Active Delay (Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (Note 1)		30		30	ns	
TCLGL	GT Active Delay	0	85	0	50	ns	
TCLGH	GT Inactive Delay	0	85	0	50	ns	
TRLRH	RD Width	2TCLCL - 75		2TCLCL - 50		ns	
TOLOH	Output Rise Time		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns	From 2.0V to 0.8V

NOTES:

1. Signal at 82C84A or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).

WAVEFORMS (Continued)

MAXIMUM MODE (Continued)

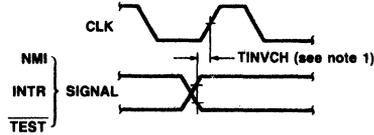


NOTES:

1. All timing measurements are made at V_{OH} and V_{OL} .
2. RDY is sampled near the end of T_2 , T_3 , T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The 80C86 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 82C88 CEN.
7. Status inactive in state just prior to T_4 .

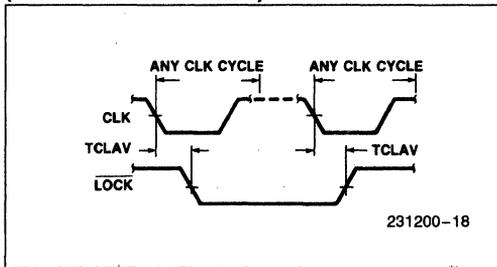
WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION

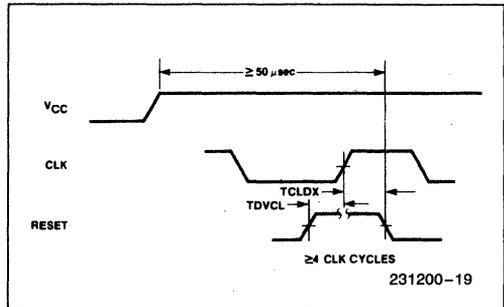


NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

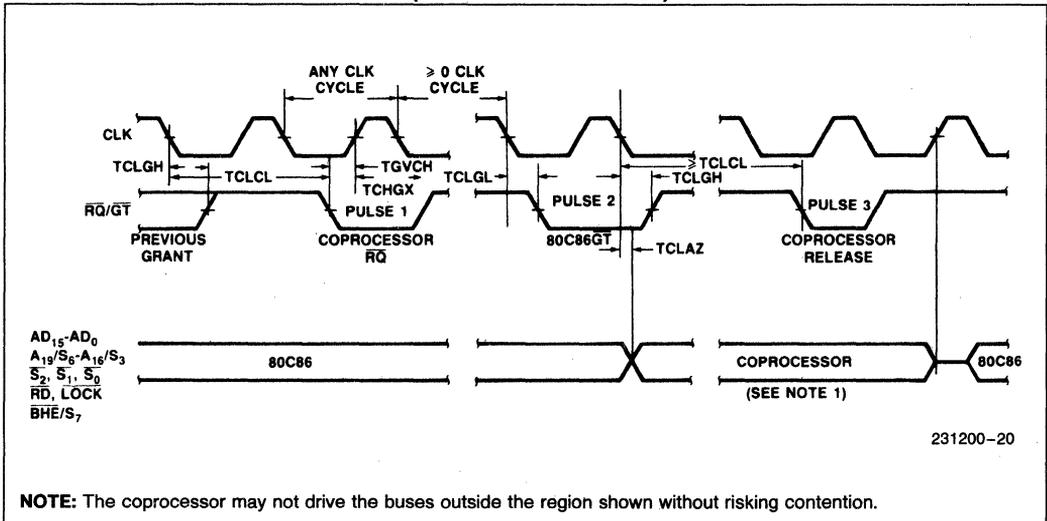
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING



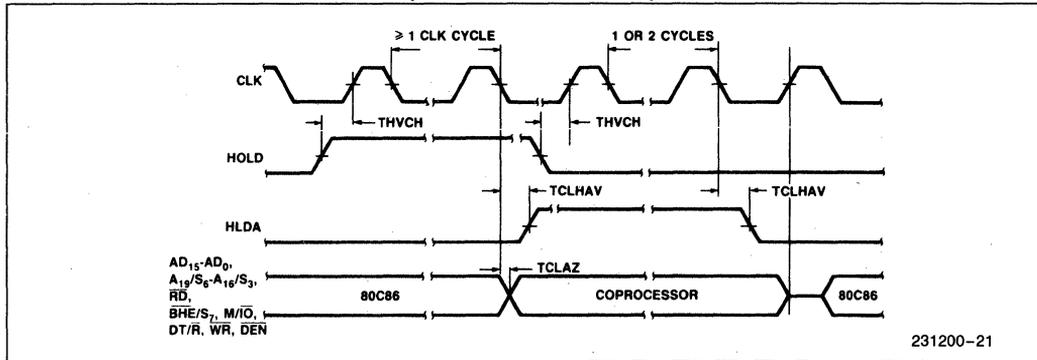
REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE: The coprocessor may not drive the buses outside the region shown without risking contention.

WAVEFORMS (Continued)

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



231200-21

Table 2. Instruction Set Summary

	76543210	76543210	76543210	76543210		76543210	76543210	76543210	76543210
DATA TRANSFER					DEC Decrement:				
MOV = Move:					Register/memory	1111101w	mod 000 r/m		
Register/memory to/from register	100010dw	mod reg r/m			Register	01001reg			
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	NEG Change sign	1111011w	mod 011 r/m		
Immediate to register	1011w reg	data	data if w=1		CMP Compare:				
Memory to accumulator	1110000w	addr=low	addr=high		Register/memory and register	001110dw	mod reg r/m		
Accumulator to memory	11010001w	addr=low	addr=high		Immediate with register/memory	100000sw	mod 111 r/m	data	data if s=w=01
Segment register to segment register	10001110	mod 0 reg r/m			Immediate with accumulator	0011110w	data	data if w=1	
Segment register to register/memory	10001100	mod 0 reg r/m			ABS ASCII adjust for subtract	00111111			
PUSH = Push:					DAS Decimal adjust for subtract	00101111			
Register/memory	11111111	mod 110 r/m			MUL Multiply (unsigned)	1111011w	mod 100 r/m		
Register	01010reg				IMUL Integer multiply (signed)	1111011w	mod 101 r/m		
Segment register	000reg 110				AAM ASCII adjust for multiply	11010100	00001010		
POP = Pop:					DIV Divide (unsigned)	1111011w	mod 110 r/m		
Register/memory	10001111	mod 000 r/m			IDIV Integer divide (signed)	1111011w	mod 000 r/m		
Register	01011reg				AAD ASCII adjust for divide	11010101	00001010		
Segment register	000reg 111				CBW Convert byte to word	10011000			
XCHG = Exchange:					CWD Convert word to double word	10011001			
Register/memory with register	1000011w	mod reg r/m			LOGIC				
Register with accumulator	10010reg				NOT Invert	1111011w	mod 010 r/m		
IN = Input from:					SHL/SAL Shift logical/arithmetic left	110100vw	mod 100 r/m		
Fixed port	1110010w	port			SHR Shift logical right	110100vw	mod 101 r/m		
Variable port	1110110w				SAR Shift arithmetic right	110100vw	mod 111 r/m		
OUT = Output to:					ROL Rotate left	110100vw	mod 000 r/m		
Fixed port	1110011w	port			ROR Rotate right	110100vw	mod 001 r/m		
Variable port	1110111w				RCL Rotate through carry flag left	110100vw	mod 010 r/m		
XLAT = Translate byte to AL	11010111				RCR Rotate through carry flag right	110100vw	mod 011 r/m		
LEA = Load EA to register	10001101	mod reg r/m			AND And:				
LDS = Load pointer to DS	11000101	mod reg r/m			Reg./memory and register to either	001000dw	mod reg r/m		
LFS = Load pointer to FS	11000100	mod reg r/m			Immediate to register/memory	100000dw	mod 100 r/m	data	data if w=1
LAFH = Load AH with flags	10011111				Immediate to accumulator	0010010w	data	data if w=1	
SAHF = Store AH into flags	10011110				TEST And function to flags, no result:				
PUSHF = Push flags	10011100				Register/memory and register	1000010w	mod reg r/m		
POPF = Pop flags	10011101				Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1
ARITHMETIC					Immediate data and accumulator	1010100w	data	data if w=1	
ADD = Add:					OR Or:				
Reg./memory with register to either	000000dw	mod reg r/m			Reg./memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s=w=01	Immediate to register/memory	100000dw	mod 001 r/m	data	data if w=1
Immediate to accumulator	0000010w	data	data if w=1		Immediate to accumulator	0000110w	data	data if w=1	
ADC = Add with carry:					XOR = Exclusive or:				
Reg./memory with register to either	000100dw	mod reg r/m			Reg./memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s=w=01	Immediate to register/memory	100000dw	mod 110 r/m	data	data if w=1
Immediate to accumulator	0001010w	data	data if w=1		Immediate to accumulator	0011010w	data	data if w=1	
INC = Increment:					STRING MANIPULATION				
Register/memory	1111111w	mod 000 r/m			REP = Repeat	1111001z			
Register	01000reg				MOVSB = Move byte/word	1010010w			
AAA = ASCII adjust for add	00110111				CMPS = Compare byte/word	1010011w			
DA A = Decimal adjust for add	00100111				SCAS = Scan byte/word	1010111w			
SUB = Subtract:					LODS = Load byte/word to AL/AX	1010110w			
Reg./memory and register to either	001010dw	mod reg r/m			STOS = Store byte/word from AL/A	1010101w			
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s=w=01					
Immediate from accumulator	001110w	data	data if w=1						
SBB = Subtract with borrow									
Reg./memory and register to either	000110dw	mod reg r/m							
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s=w=01					
Immediate from accumulator	0001110w	data	data if w=1						
Mnemonics Intel 1982									

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Table 2. Instruction Set Summary (Continued)

CONTROL TRANSFER

CALL = Call:

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m	
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	

JMP = Unconditional Jump:

Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	

RET = Return from CALL:

Within segment	1 1 0 0 0 0 1 1		
Within seg. adding immed to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high

JE/JZ = Jump on equal/zero

JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 0 1 0	disp	
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	

JBE/JNAE = Jump on below/not above or equal

JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 0 1 0	disp	
JBP/JNAE = Jump on parity/parity even	0 1 1 1 0 1 1 0	disp	

JO = Jump on overflow

JS = Jump on sign	0 1 1 1 0 0 0 0	disp	
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	

JNL/JGGE = Jump on not less/greater or equal

JNL/JG = Jump on not less or equal/greater	0 1 1 1 1 1 0 1	disp	
	0 1 1 1 1 1 1 1	disp	

JNB/JAE = Jump on not below/above or equal

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNB/JAE	0 1 1 1 0 0 1 1	disp
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPE Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ Jump on CX zero	1 1 1 0 0 0 1 1	disp

INT Interrupt

Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET Interrupt return	1 1 0 0 1 1 1 1	

PROCESSOR CONTROL

CLC Clear carry	1 1 1 1 1 0 0 0	
CMC Complement carry	1 1 1 1 0 1 0 1	
STC Set carry	1 1 1 1 1 0 0 1	
CLD Clear direction	1 1 1 1 1 1 0 0	
STD Set direction	1 1 1 1 1 0 0 1	
CLI Clear interrupt	1 1 1 1 1 0 1 0	
STI Set interrupt	1 1 1 1 0 1 1 1	
HLT Halt	1 1 0 1 0 1 0 0	
WAIT Wait	1 0 0 1 1 0 1 1	
ESC Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK Bus lock prefix	1 1 1 1 0 0 0 0	

Footnotes:

AL = 8-bit accumulator
 AX = 16-bit accumulator
 CX = Count register
 DS = Data segment
 ES = Extra segment
 Above/below refers to unsigned value.
 Greater = more positive.
 Less = less positive (more negative) signed values
 If d = 1 then "to" seg; if d = 0 then "from" seg
 If w = 1 then word instruction, if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
 if mod = 00 then DISP = 0*, disp-low and disp-high are absent
 if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
 if mod = 10 then DISP = disp-high, disp-low
 if r/m = 000 then EA = (BX) + (SI) + DISP
 if r/m = 001 then EA = (BX) + (DI) + DISP
 if r/m = 010 then EA = (BP) + (SI) + DISP
 if r/m = 011 then EA = (BP) + (DI) + DISP
 if r/m = 100 then EA = (SI) + DISP
 if r/m = 101 then EA = (DI) + DISP
 if r/m = 110 then EA = (BP) + DISP*
 if r/m = 111 then EA = (BX) + DISP
 DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high, disp-low.

if s/w = 01 then 16 bits of immediate data form the operand.
 if s/w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
 if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
 x = don't care
 z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-bit [w = 1]	8-bit [w = 0]	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file.

FLAGS = X:X:X:(CF):(DF):(IF):(SF):(ZF):(AF):X:(PF):X:(CF)

80C88/80C88-2 8-BIT CHMOS MICROPROCESSOR

- Pin-for-Pin and Functionally Compatible to Industry Standard HMOS 8088
- Direct Software Compatibility with 80C86, 8086, 8088
- Fully Static Design with Frequency Range from D.C. to:
 - 5 MHz for 80C88
 - 8 MHz for 80C88-2
- Low Power Operation
 - Operating $I_{CC} = 10 \text{ mA/MHz}$
 - Standby $I_{CCs} = 500 \mu\text{A max}$
- Bus-Hold Circuitry Eliminates Pull-Up Resistors
- Direct Addressing Capability of 1 MByte of Memory
- Architecture Designed for Powerful Assembly Language and Efficient High Level Languages
- 24 Operand Addressing Modes
- Byte, Word and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic
 - Binary or Decimal
 - Multiply and Divide

The Intel 80C88 is a high performance, CHMOS version of the industry standard HMOS 8088 8-bit CPU. The processor has attributes of both 8 and 16-bit microprocessors. It is available in 5 MHz clock rate and will be available in 8 MHz clock rate in 2nd half of 1985. The 80C88 offers two modes of operation: MINimum for small systems and MAXimum for larger applications such as multi-processing. It is available in 40-pin DIP and will be available in 44-pin plastic leaded chip carrier (PLCC) package in 2nd half of 1985.

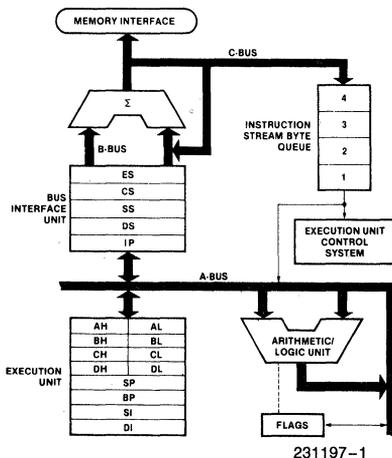


Figure 1. iAPX 80C88 CPU Functional Block Diagram

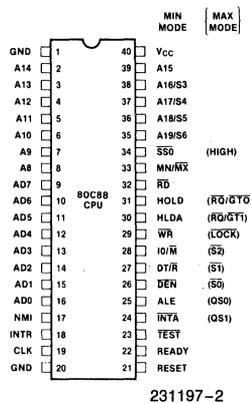


Figure 2. 80C88 40-lead Configuration

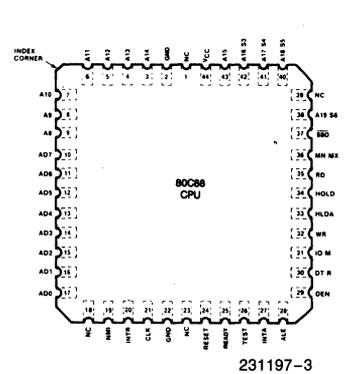


Figure 2b. 80C88 44-lead PLCC Configuration

Table 1. Pin Description

The following pin function descriptions are for 80C88 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 80C88 (without regard to additional bus buffers).

Symbol	Pin No.	Type	Name and Function																		
AD7-AD0	9-16	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/I/O address (T1) and data (T2, T3, Tw, and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".																		
A15-A8	2-8, 39	O	ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1-T4). These lines do not have to be latched by ALE to remain valid. A15-A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".																		
A19/S6, A18/S5, A17/S4, A16/S3	35-38	O	<p>ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.</p> <p>This information indicates which segment register is presently being used for data accessing.</p> <p>These lines float to 3-state OFF during local bus "hold acknowledge".</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">S4</th> <th style="width: 25%;">S3</th> <th style="width: 50%;">CHARACTERISTICS</th> </tr> </thead> <tbody> <tr> <td>0 (LOW)</td> <td>0</td> <td>Alternate Data</td> </tr> <tr> <td>0</td> <td>1</td> <td>Stack</td> </tr> <tr> <td>1 (HIGH)</td> <td>0</td> <td>Code or None</td> </tr> <tr> <td>1</td> <td>1</td> <td>Data</td> </tr> <tr> <td colspan="3">S6 is 0 (LOW)</td> </tr> </tbody> </table>	S4	S3	CHARACTERISTICS	0 (LOW)	0	Alternate Data	0	1	Stack	1 (HIGH)	0	Code or None	1	1	Data	S6 is 0 (LOW)		
S4	S3	CHARACTERISTICS																			
0 (LOW)	0	Alternate Data																			
0	1	Stack																			
1 (HIGH)	0	Code or None																			
1	1	Data																			
S6 is 0 (LOW)																					
\overline{RD}	32	O	<p>READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/\overline{M} pin or S2. This signal is used to read devices which reside on the 80C88 local bus. \overline{RD} is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C88 local bus has floated.</p> <p>This signal floats to 3-state OFF in "hold acknowledge".</p>																		
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A clock generator to form READY. This signal is active HIGH. The 80C88 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.																		

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{\text{TEST}}$	23	I	$\overline{\text{TEST}}$: input is examined by the "wait for test" instruction. If the $\overline{\text{TEST}}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V _{CC}	40		V_{CC}: is the +5V \pm 10% power supply pin.
GND	1, 20		GND: are the ground pins.
MN/ $\overline{\text{MX}}$	33	I	MINIMUM/MAXIMUM: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 80C88 minimum mode (i.e., MN/MX = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

IO/ $\overline{\text{M}}$	28	O	STATUS LINE: is an inverted maximum mode $\overline{\text{S}}_2$. It is used to distinguish a memory access from an I/O access. IO/ $\overline{\text{M}}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/ $\overline{\text{M}}$ floats to 3-state OFF in local bus "hold acknowledge".
WR	29	O	WRITE: strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/ $\overline{\text{M}}$ signal. WR is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{\text{INTA}}$	24	O	$\overline{\text{INTA}}$: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle.

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function			
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into an address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.			
DT/ \bar{R}	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/ \bar{R} is equivalent to $\bar{S1}$ in the maximum mode, and its timing is the same as for IO/ \bar{M} (T = HIGH, R = LOW). This signal floats to 3-state OFF in local "hold acknowledge".			
\bar{DEN}	26	O	DATA ENABLE: is provided as an output enable for the transceiver in a minimum system which uses the transceiver. \bar{DEN} is active LOW during each memory and I/O access, and for \bar{INTA} cycles. For a read or \bar{INTA} cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. \bar{DEN} floats to 3-state OFF during local bus "hold acknowledge".			
HOLD, HLDA	30, 31	I, O	HOLD: indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.			
\bar{SSO}	34	O	STATUS LINE: is logically equivalent to $\bar{S0}$ in the maximum mode. The combination of \bar{SSO} , IO/ \bar{M} and DT/ \bar{R} allows the system to completely decode the current bus cycle status.			
			IO/ \bar{M}	DT/ \bar{R}	\bar{SSO}	CHARACTERISTICS
			1(HIGH)	0	0	Interrupt Acknowledge
			1	0	1	Read I/O port
			1	1	0	Write I/O port
			1	1	1	Halt
			0(LOW)	0	0	Code access
			0	0	1	Read memory
			0	1	0	Write memory
			0	1	1	Passive

Table 1. Pin Description (Continued)

The following pin function descriptions are for the 80C88/82C88 system in maximum mode (i.e., MN/MX = GND.) Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

Symbol	Pin No.	Type	Name and Function			
$\overline{S2}, \overline{S1}, \overline{S0}$	26-28	O	<p>STATUS: is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}, \overline{S1},$ or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle.</p> <p>These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF.</p>			
			$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
			0(LOW)	0	0	Interrupt Acknowledge
			0	0	1	Read I/O port
			0	1	0	Write I/O port
0	1	1	Halt			
1(HIGH)	0	0	Code access			
1	0	1	Read memory			
1	1	0	Write memory			
1	1	1	Passive			
$\overline{RQ}/\overline{GT0},$ $\overline{RQ}/\overline{GT1}$	30, 31	I/O	<p>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor, so may be left unconnected. The request/grant sequence is as follows (See Figure 8):</p> <ol style="list-style-type: none"> 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 80C88 (pulse 1). 2. During a T4 or T1 clock cycle, a pulse one clock wide from the 80C88 to the requesting master (pulse 2), indicates that the 80C88 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released. 3. A pulse one CLK wide from the requesting master indicates to the 80C88 (pulse 3) that the "hold" request is about to end and that the 80C88 can reclaim the local bus at the next CLK. The CPU then enters T4. 			

Table 1. Pin Descriptions (Continued)

Symbol	Pin No.	Type	Name and Function															
$\overline{RQ}/\overline{GT0}$, $\overline{RQ}/\overline{GT1}$	30, 31	I/O	<p>Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> 1. Request occurs on or before T2. 2. Current cycle is not the low bit of a word. 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. <p>If the local bus is idle when the request is made the two possible events will follow:</p> <ol style="list-style-type: none"> 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied. 															
\overline{LOCK}	29	O	<p>\overline{LOCK}: indicates that other system bus masters are not to gain control of the system bus while \overline{LOCK} is active (LOW). The \overline{LOCK} signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state off in "hold acknowledge".</p>															
QS1, QS0	24, 25	O	<p>QUEUE STATUS: provide status to allow external tracking of the internal 80C88 instruction queue.</p> <p>The queue status is valid during the CLK cycle after which the queue operation is performed.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>QS1</th> <th>QS0</th> <th>CHARACTERISTICS</th> </tr> </thead> <tbody> <tr> <td>0(LOW)</td> <td>0</td> <td>No operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>First byte of opcode from queue</td> </tr> <tr> <td>1(HIGH)</td> <td>0</td> <td>Empty the queue</td> </tr> <tr> <td>1</td> <td>1</td> <td>Subsequent byte from queue</td> </tr> </tbody> </table>	QS1	QS0	CHARACTERISTICS	0(LOW)	0	No operation	0	1	First byte of opcode from queue	1(HIGH)	0	Empty the queue	1	1	Subsequent byte from queue
QS1	QS0	CHARACTERISTICS																
0(LOW)	0	No operation																
0	1	First byte of opcode from queue																
1(HIGH)	0	Empty the queue																
1	1	Subsequent byte from queue																
—	34	O	Pin 34 is always high in the maximum mode.															

FUNCTIONAL DESCRIPTION

STATIC OPERATION

All 80C88 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C88 can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C88 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C88 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until ultimately, at a DC input frequency, the 80C88 power requirement is the standby current (500 μ A maximum).

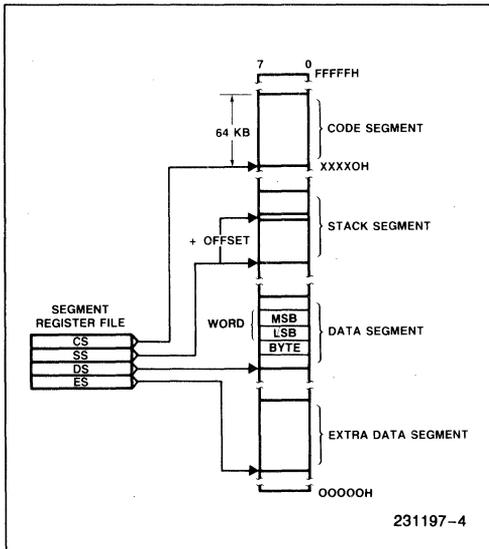


Figure 3. Memory Organization

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. (See Figure 4.) Locations from addresses FFFF0H through FFFFH are reserved for operations including a jump to the initial system

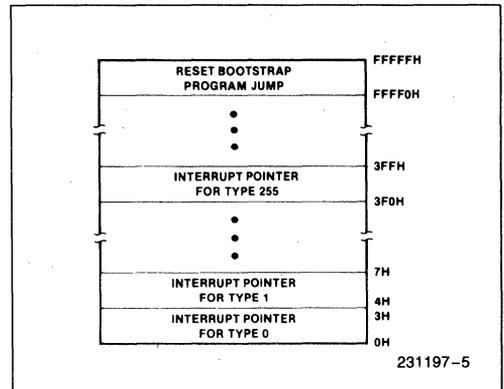


Figure 4. Reserved Memory Locations

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Four-byte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum 80C88 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 80C88 is equipped with a strap pin (MN/MX) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/MX pin is strapped to GND, the 80C88 defines pins 24 through 31 and 34 in maximum mode. When the MN/MX pin is strapped to V_{CC}, the 80C88 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C88 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the MCS®-85

multiplexed bus peripherals (8155, 8156, 8355, 8755A, and 8185). This configuration (See Figure 5) provides the user with a minimum chip count system. This architecture provides the 80C88 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64k addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it. A transceiver can also be used if data bus buffering is required. (See Figure 6.) The 80C88 provides DEN and DT/R to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller. (See Figure 7.) The 82C88 decodes status lines S₀, S₁, and S₂, and provides the system with all bus control signals. Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C88 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C88 in maximum mode. These features allow co-processors in local bus and remote bus configurations.

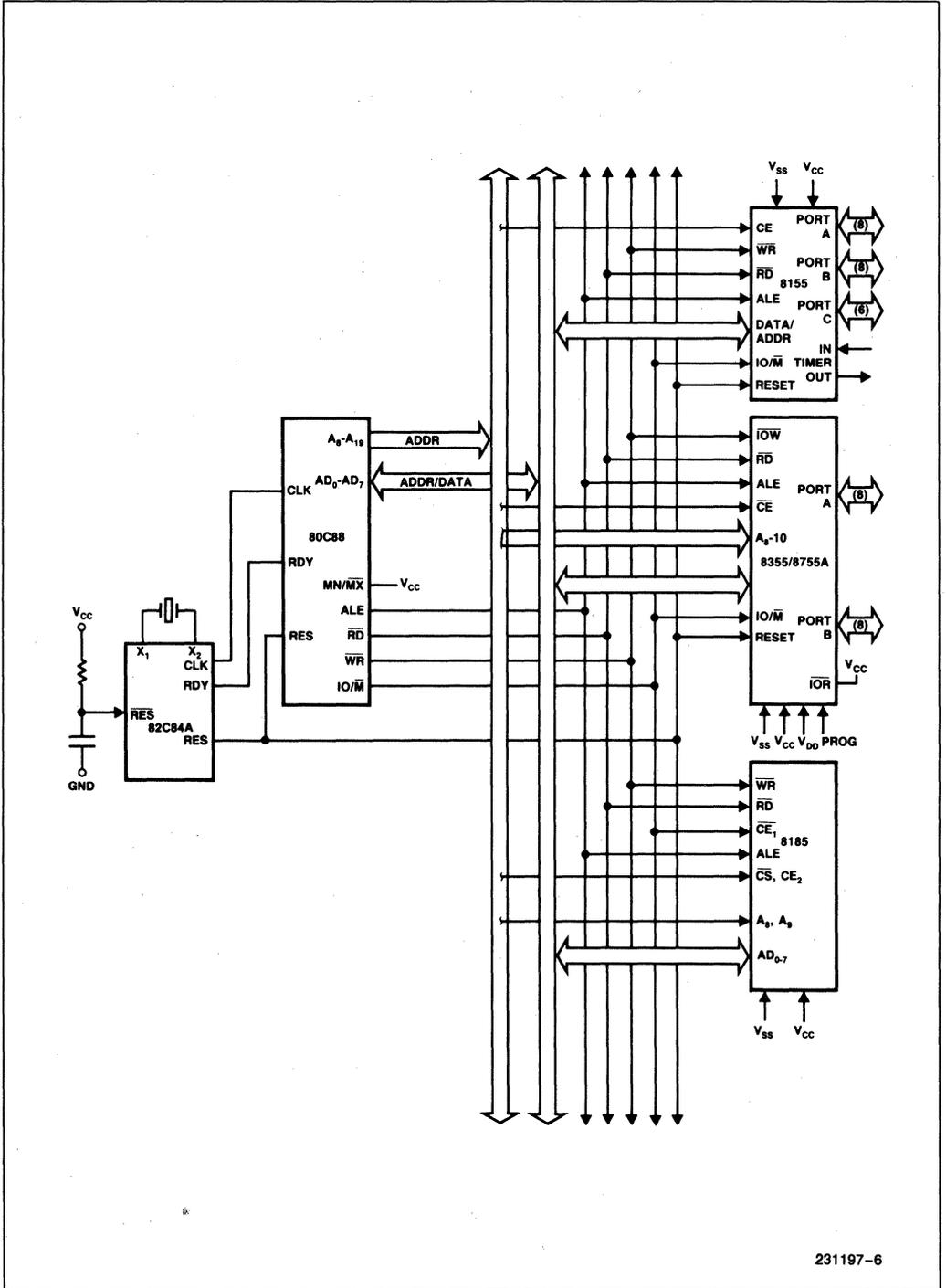


Figure 5. Multiplexed Bus Configuration

Bus Operation

The 80C88 address/data bus is broken into three parts—the lower eight address/data bits (A0–A7), the middle eight address bits (A8–A15), and the upper four address bits (A16–A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3, and T4. (See Figure 8). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a “NOT READY” indication is given by the addressed device, “wait” states (Tw) are inserted between T3 and T4. Each inserted “wait” state is of the same duration as a CLK cycle. Periods can occur between 80C88 driven bus cycles. These are referred to as “idle” states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

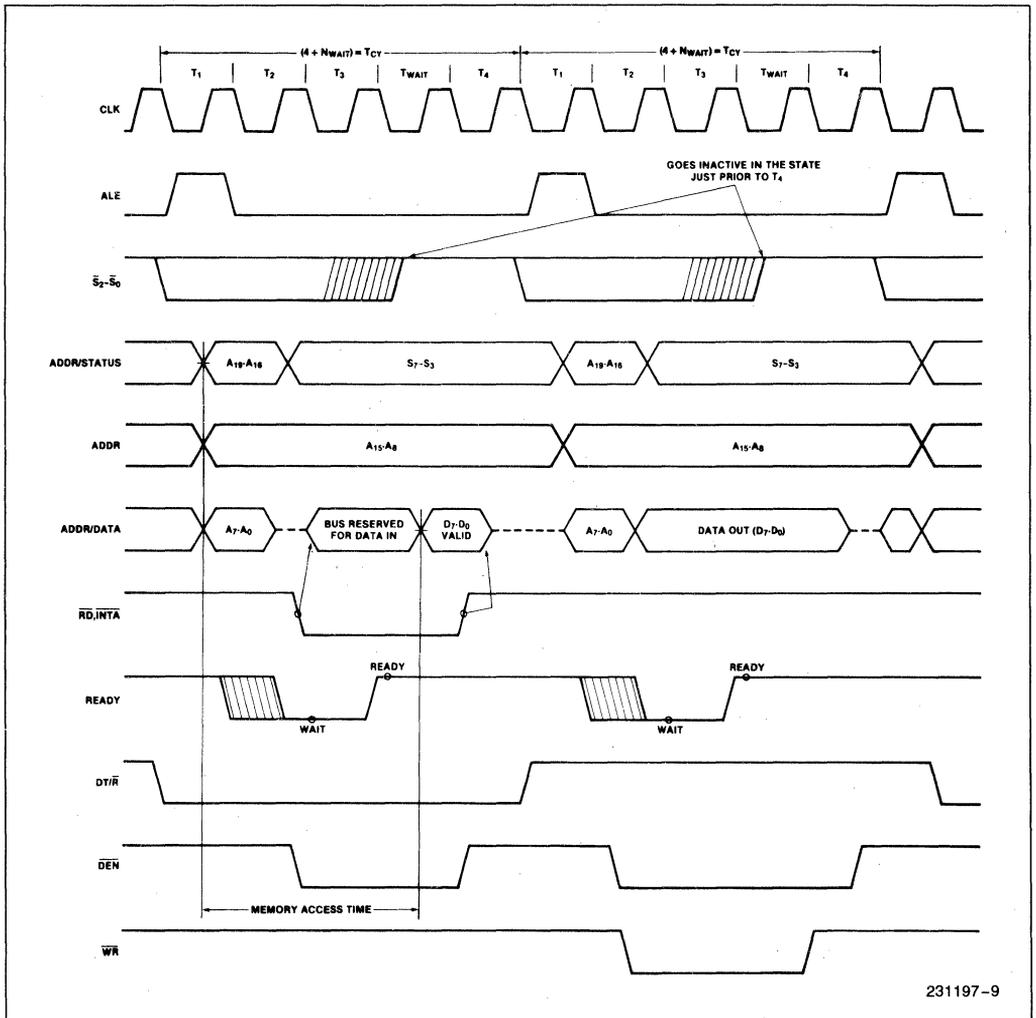


Figure 8. Basic System Timing

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/MX strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S6 are multiplexed with high order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S4	S3	CHARACTERISTICS
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

I/O ADDRESSING

In the 80C88, I/O operations can address up to a maximum of 64k I/O registers. The I/O address appears in the same format as the memory address on

bus lines A15–A0. The address lines A19–A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The 80C88 uses a full 16-bit address on its lower 16 address lines.

EXTERNAL INTERFACE

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C88 RESET is required to be HIGH for greater than four clock cycles. The 80C88 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 80C88 operates normally, beginning with the instruction in absolute location FFFF0H. (See Figure 4.) The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50 μ s after power up, to allow complete initialization of the 80C88.

If INTR is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

All 3-state outputs float to 3-state OFF during RESET. Status is active in the idle state for the first clock after RESET becomes active and then floats to 3-state OFF.

BUS HOLD CIRCUITRY

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on the 80C88 pins 2-16, 26-32, and 34-39 (Figure 9a, 9b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400 μ A minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply cur-

rent is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description in the iAPX 88 book or the iAPX 86,88 User's Manual. Hardware interrupts can be classified as nonmaskable or maskable.

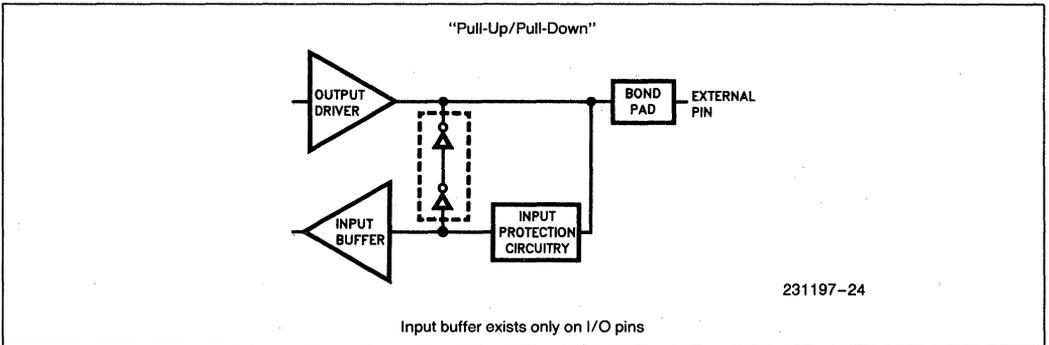


Figure 9a. Bus hold circuitry pin 2-16, 35-39.

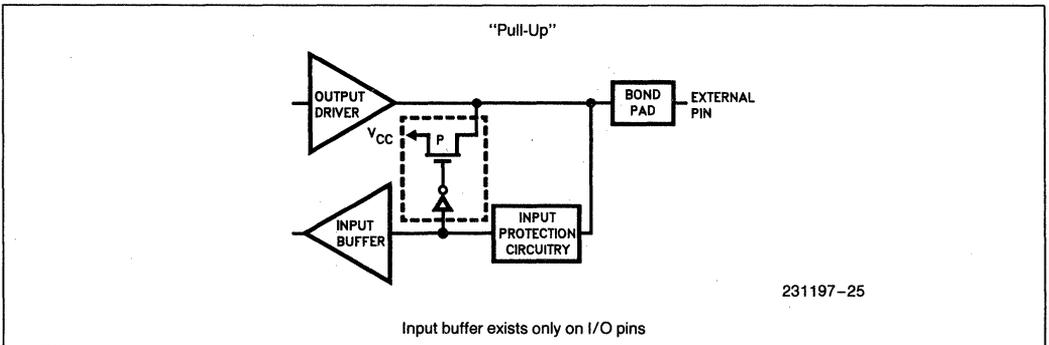


Figure 9b. Bus hold circuitry pin 26-32, 34.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (See Figure 4), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type." An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. Any higher going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must

be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The 80C88 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored, the enable bit will be zero unless specifically set by an instruction.

During the response sequence (See Figure 10), the processor executes two successive (back to back) interrupt acknowledge cycles. The 80C88 emits the LOCK signal (maximum mode only) from T₂ of the first bus cycle until T₂ of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a

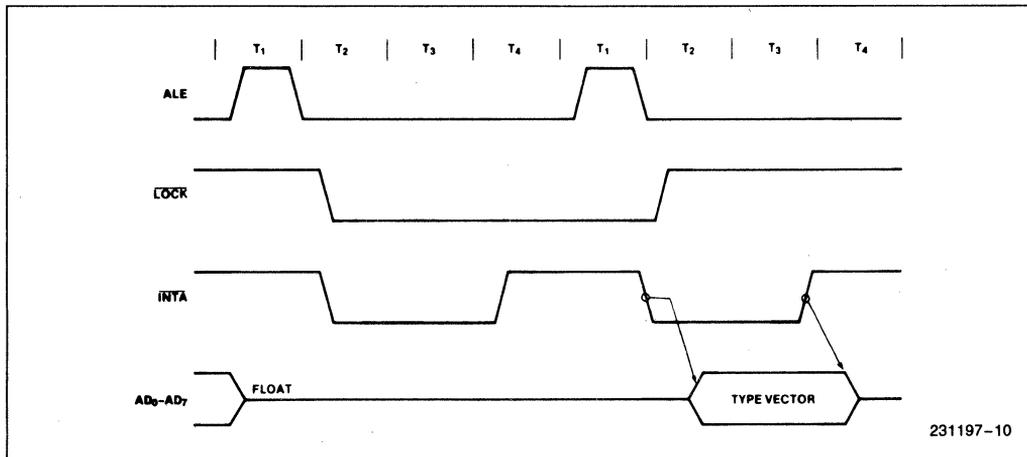


Figure 10. Interrupt Acknowledge Sequence

byte is fetched from the external interrupt system (e.g., 82C59A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

HALT

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/M, DT/R, and SSO. In maximum mode, the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, and $\overline{S0}$, and the 82C88 bus controller issues one ALE. The 80C88 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 80C88 out of the HALT state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The LOCK signal is activated (LOW) in the clock cycle following decoding of the LOCK prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the LOCK prefix. While LOCK is active, a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded, and then honored at the end of the LOCK.

EXTERNAL SYNCHRONIZATION VIA \overline{TEST}

As an alternative to interrupts, the 80C88 provides a single software-testable input pin (\overline{TEST}). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the \overline{TEST} input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C88 3-states all output drivers. If interrupts are enabled, the 80C88 will recognize interrupts and process them. The WAIT instruction is then re-fetched, and reexecuted.

BASIC SYSTEM TIMING

In minimum mode, the $\overline{MN}/\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals compatible with the 8085 bus structure. In maximum mode, the $\overline{MN}/\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS compatible bus control signals.

System Timing — Minimum System

(See Figure 8.)

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal. The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD7) at this time, into a latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/M signal indicates a memory or I/O operation. At T2 the address is removed from the address/data bus and the bus goes to a high impedance state. The read control signal is also asserted at T2. The read (\overline{RD}) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver is required to buffer the 80C88 local bus, signals DT/R and \overline{DEN} are provided by the 80C88.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/M signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3, and T_W , the processor asserts the write control signal. The write (\overline{WR}) signal becomes active at the beginning of T2, as opposed to the read, which is delayed somewhat into T2 to provide time for the bus to float.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge (\overline{INTA}) signal is asserted in place of the read (\overline{RD}) signal and the address bus is floated. (See Figure 10.) In the second of two successive \overline{INTA} cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e. 82C59A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

BUS TIMING — MEDIUM COMPLEXITY SYSTEMS

(See Figure 11.)

For medium complexity systems, the $\overline{MN}/\overline{MX}$ pin is connected to GND and the 82C88 bus controller is added to the system, as well as a latch for latching the system address, and a transceiver to allow for bus loading greater than the 80C88 is capable of handling. Signals \overline{ALE} , \overline{DEN} , and $\overline{DT}/\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C88 status outputs ($\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) provide type of cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The transceiver receives the usual \overline{T} and \overline{OE} inputs from the 82C88's $\overline{DT}/\overline{R}$ and \overline{DEN} outputs.

The pointer into the interrupt vector table, which is passed during the second \overline{INTA} cycle, can derive from an 82C59A located on either the local bus or the system bus. If the master 82C59A priority interrupt controller is positioned on the local bus, a TTL gate is required to disable the transceiver when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

THE 80C88 COMPARED TO THE 80C86

The 80C88 CPU is an 8-bit processor designed around the 80C86 internal structure. Most internal functions of the 80C88 are identical to the equiva-

lent 80C86 functions. The 80C88 handles the external bus the same way the 80C86 does with the distinction of handling only 8 bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the 80C88 and 80C86 are outlined below. The engineer who is unfamiliar with the 80C86 is referred to the iAPX 86, 88 User's Manual, Chapters 2 and 4, for function description and instruction set information. Internally, there are three differences between the 80C88 and the 80C86. All changes are related to the 8-bit bus interface.

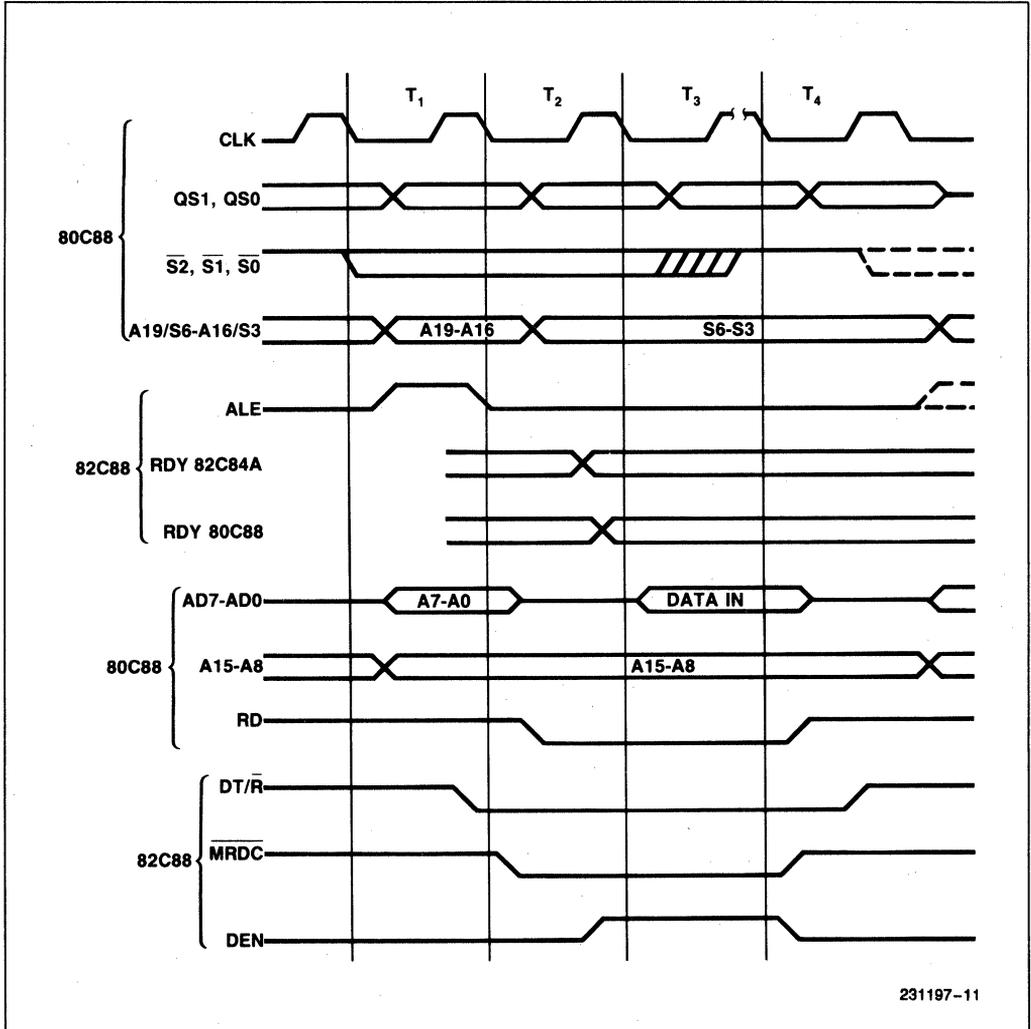
- The queue length is 4 bytes in the 80C88, whereas the 80C86 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 80C88 BIU will fetch a new instruction to load into the queue each time there is a 1 byte hole (space available) in the queue. The 80C86 waits until a 2-byte space is available.
- The internal execution time of the instruction set is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the 80C88 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 80C88 and 80C86 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an 80C88 or an 80C86.

The hardware interface of the 80C88 contains the major differences between the two CPUs. The pin assignments are nearly identical, however with the following functional changes:

- A8-A15 — These pins are only address outputs on the 80C88. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.

- \overline{BHE} has no meaning on the 80C88 and has been eliminated.
- \overline{SSO} provides the \overline{SO} status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/\overline{R} , IO/\overline{M} , and \overline{SSO} provide the complete bus status in minimum mode.
- IO/\overline{M} has been inverted to be compatible with the MCS-85 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.



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Figure 11. Medium Complexity System Timing

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage
 (With respect to ground) -0.5 to 8.0V
 Operating Supply Voltage
 (w.r.t. ground) 4.0 to 7.0V
 Input Voltage Applied
 (w.r.t. ground) -2.0 to $V_{CC} + 0.5V$
 Output Voltage Applied
 (w.r.t. ground) -0.5 to $V_{CC} + 0.5V$
 Power Dissipation 1.0W
 Storage Temperature -65°C to +150°C
 Ambient Temperature Under Bias 0°C to +70°C

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS (80C88: $T_A = 0^\circ C$ to $70^\circ C$, $V_{CC} = 5V \pm 10\%$)
 (80C88-2: $T_A = 0^\circ C$ to $70^\circ C$, $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage (All input except RQ/GT0, RQ/GT1)	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.0\text{ mA}$
V_{OH}	Output High Voltage	3.0 $V_{CC} - 0.4$		V	$I_{OH} = -2.5\text{ mA}$ $I_{OH} = -100\text{ }\mu\text{A}$
I_{CC}	Power Supply Current		10 mA/MHz		$T_A = 25^\circ C$, $V_{CC} = 5.5V$ $V_{IH} = GND$, $V_{IL} = V_{CC}$
I_{CCS}	Standby Supply Current		500	μA	$V_{IN(max)} = V_{CC}$ or GND $V_{CC} = 5.5V$ Outputs Unloaded CLK = GND or V_{CC}
I_{LI}	Input Leakage Current		± 1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
I_{BHL}	Input Leakage Current (Bus Hold Low)	50	400	μA	$V_{IN} = 0.8V$ (Note 1)
I_{BHH}	Input Leakage Current (Bus Hold High)	-50	-400	μA	$V_{IN} = 3.0V$ (Note 2)
I_{BHLO}	Bus Hold Low Overdrive		600	μA	(Note 4)
I_{BHHO}	Bus Hold High Overdrive		-600	μA	(Note 5)
I_{LO}	Output Leakage Current		± 10	μA	$0 \leq V_{OUT} \leq V_{CC}$
V_{CL}	Clock Input Low Voltage	-0.5	+0.8	V	
V_{CH}	Clock Input High Voltage	$V_{CC} - 0.8$	$V_{CC} + 0.5$	V	
C_{IN}	Capacitance of Input Buffer (All input except AD ₀ -AD ₇ , RQ/GT)		5	pF	(Note 3)
C_{IO}	Capacitance of I/O Buffer (AD ₀ -AD ₇ , RQ/GT)		20	pF	(Note 3)
C_{OUT}	Output Capacitance		15	pF	(Note 3)

NOTES:

1. Test condition is to lower V_{IN} to GND and then raise V_{IN} to 0.8V on pins 2-16, 26-32, and 34-39.
2. Test condition is to raise V_{IN} to V_{CC} and then lower V_{IN} to 3.0V on pins 2-16, 26-32, and 34-39.
3. Test conditions are a) Frequency = 1 MHz.
 b) Unmeasured pins at GND
 c) V_{IN} at +5.0V or GND.
4. An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.
5. An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.

A.C. CHARACTERISTICS (80C88: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 10\%$)
 (80C88-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	80C88		80C88-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	D.C.	125	D.C.	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	CL = 20 – 100 pF
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84A (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84A (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C88	118		68		ns	
TCHRYX	READY Hold Time into 80C88	30		20		ns	
TRYLCL	READY Inactive to CLK (Note 3)	-8		-8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, TEST Setup Time (Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V

NOTES:

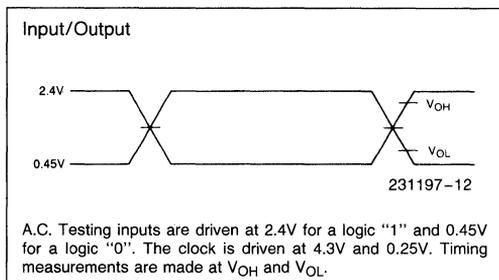
- Signal at 82C84A or 82C88 shown for reference only.
- Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
- Applies only to T2 state (8 ns into T3 state).

A.C. CHARACTERISTICS (Continued)

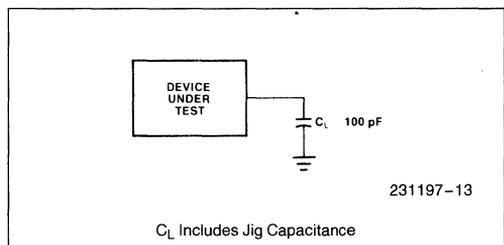
TIMING RESPONSES

Symbol	Parameter	80C88		80C88-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLAV	Address Valid Delay	10	110	10	60	ns	$C_L = 20\text{--}100\text{ pF}$ for all 80C88 Outputs in addition to internal loads
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH-20		TCLCH-10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		TCHCL-10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After WR	TCLCH-30		TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	\overline{RD} Active Delay	10	165	10	100	ns	
TCLRH	\overline{RD} Inactive Delay	10	150	10	80	ns	
TRHAV	\overline{RD} Inactive to Next Address Active	TCLCL-45		TCLCL-40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	\overline{RD} Width	2TCLCL-75		2TCLCL-50		ns	
TWLWH	\overline{WR} Width	2TCLCL-60		2TCLCL-40		ns	
TAVAL	Address Valid to ALE Low	TCLCH-60		TCLCH-40		ns	
TOLOH	Output Rise Time		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns	From 2.0V to 0.8V

A.C. TESTING INPUT, OUTPUT WAVEFORM

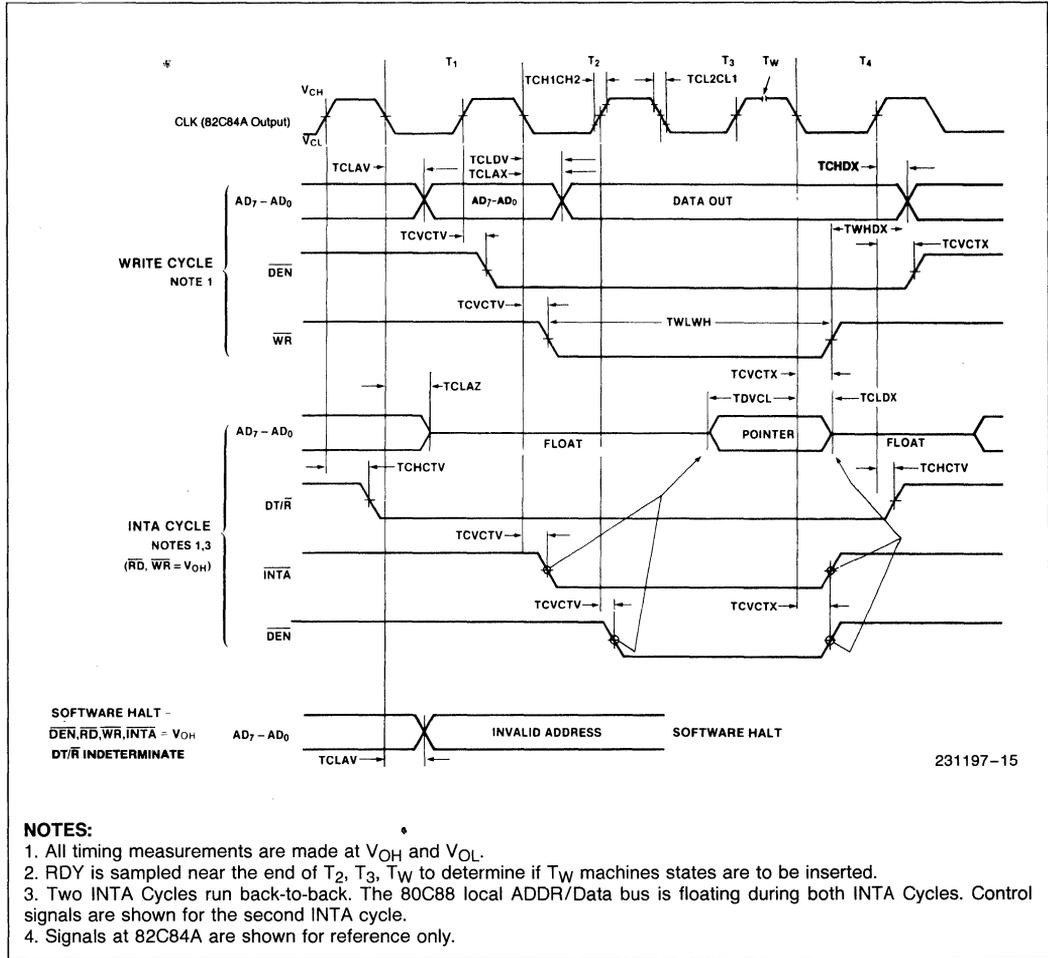


A.C. TESTING LOAD CIRCUIT



WAVEFORMS (Continued)

BUS TIMING — MINIMUM MODE SYSTEM (Continued)



NOTES:

1. All timing measurements are made at V_{OH} and V_{OL}.
2. RDY is sampled near the end of T₂, T₃, T_w to determine if T_w machines states are to be inserted.
3. Two INTA Cycles run back-to-back. The 80C88 local ADDR/Data bus is floating during both INTA Cycles. Control signals are shown for the second INTA cycle.
4. Signals at 82C84A are shown for reference only.

A.C. CHARACTERISTICS
**MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)
TIMING REQUIREMENTS**

Symbol	Parameter	80C88		80C88-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	D.C.	125	D.C.	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data In Setup Time	30		20		ns	CL = 20 – 100 pF
TCLDX	Data In Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C88	118		68		ns	
TCHRYX	READY Hold Time into 80C88	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	-8		-8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (See Note 2)	30		15		ns	
TGVCH	RQ/GT Setup Time	30		15		ns	
TCHGX	RQ Hold Time into 80C88	40		30		ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V

NOTES:

1. Signal at 82C84A or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states (8 ns into T3 state).
4. Applies only to T2 state (8 ns into T3 state).

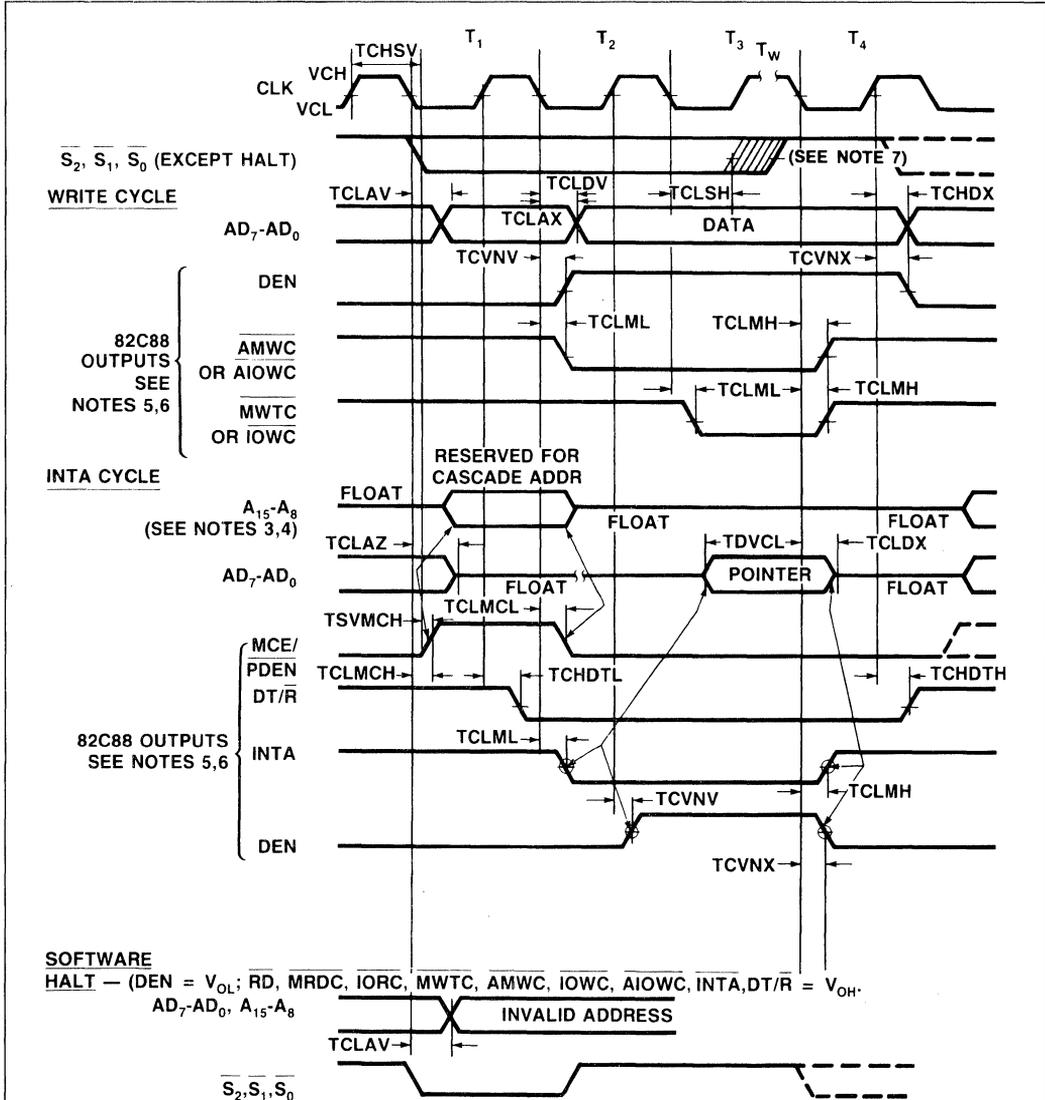
A.C. CHARACTERISTICS

TIMING RESPONSES

Symbol	Parameter	80C88		80C88-2		Units	Test Conditions	
		Min	Max	Min	Max			
TCLML	Command Active Delay (Note 1)	5	35	5	35	ns	C _L = 20–100 pF for all 80C88 Outputs in addition to internal loads	
TCLMH	Command Inactive Delay (Note 1)	5	35	5	35	ns		
TRYHSH	READY Active to Status Passive (Note 3)		110		65	ns		
TCHSV	Status Active Delay	10	110	10	60	ns		
TCLSH	Status Inactive Delay	10	130	10	70	ns		
TCLAV	Address Valid Delay	10	110	10	60	ns		
TCLAX	Address Hold Time	10		10		ns		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns		
TSVLH	Status Valid to ALE High (Note 1)		20		20	ns		
TSVMCH	Status Valid to MCE High (Note 1)		30		30	ns		
TCLLH	CLK Low to ALE Valid (Note 1)		15		15	ns		
TCLMCH	CLK Low to MCE High (Note 1)		25		25	ns		
TCHLL	ALE Inactive Delay (Note 1)	4	18	4	18	ns		
TCLMCL	MCE Inactive Delay (Note 1)		15		15	ns		
TCLDV	Data Valid Delay	10	110	10	60	ns		
TCHDX	Data Hold Time	10		10		ns		
TCVNV	Control Active Delay (Note 1)	5	45	5	45	ns		
TCVNX	Control Inactive Delay (Note 1)	10	45	10	45	ns		
TAZRL	Address Float to Read Active	0		0		ns		
TCLRL	RD Active Delay	10	165	10	100	ns		
TCLRH	RD Inactive Delay	10	150	10	80	ns		
TRHAV	RD Inactive to Next Address Active	TCLCL-45		TCLCL-40		ns		
TCHDTL	Direction Control Active Delay (Note 1)		50		50	ns		
TCHDTH	Direction Control Inactive Delay (Note 1)		30		30	ns		
TCLGL	GT Active Delay		85		50	ns		
TCLGH	GT Inactive Delay		85		50	ns		
TRLRH	RD Width	2TCLCL-75		2TCLCL-50		ns		
TOLOH	Output Rise Time		15		15	ns		From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns		From 2.0V to 0.8V

WAVEFORMS (Continued)

BUS TIMING — MAXIMUM MODE SYSTEM (USING 82C88)



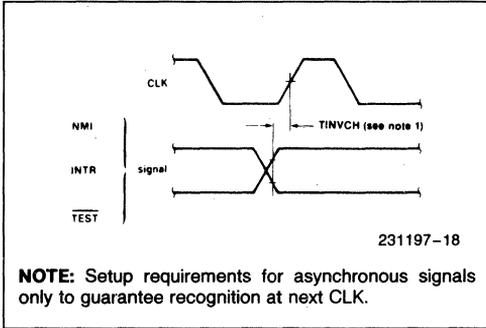
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NOTES:

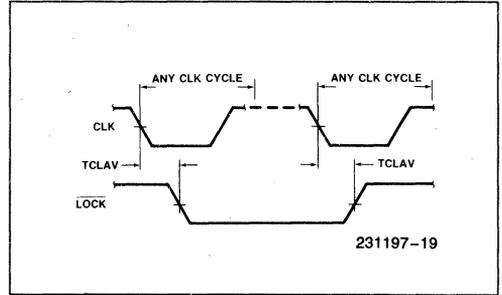
1. All timing measurements are made at V_{OH} and V_{OL} .
2. RDY is sampled near the end of T_2 , T_3 , T_w to determine if T_w machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycles.
4. Two INTA cycles run back-to-back. The 80C88 local ADDR/Data bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals (\overline{MRDC} , \overline{MWTC} , \overline{AMWC} , \overline{IORC} , \overline{IOWC} , \overline{AIOWC} , \overline{INTA} , $\overline{DT/R}$ and \overline{DEN}) lags the active high 82C88 CEN.
7. Status inactive in state just prior to T_4 .

WAVEFORMS (Continued)

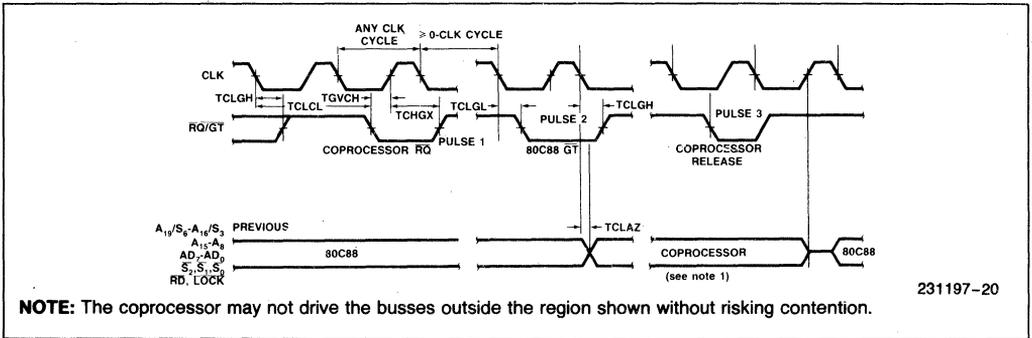
ASYNCHRONOUS SIGNAL RECOGNITION



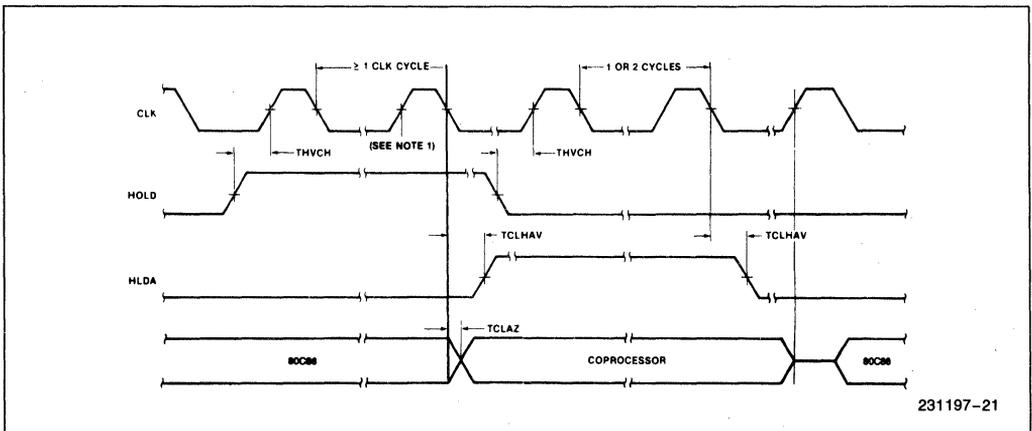
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



INSTRUCTION SET SUMMARY (Continued)

CONTROL TRANSFER			76543210			76543210			76543210			76543210		
CALL = Call:			11101000	disp-low	disp-high							01110011	disp	
Direct within segment			11111111	mod 0 10 r/m								01110111	disp	
Indirect within segment			10011010	offset-low	offset-high									
Direct intersegment				seg-low	seg-high									
Indirect intersegment			11111111	mod 0 11 r/m										
JMP = Unconditional Jump:														
Direct within segment			11101001	disp-low	disp-high									
Direct within segment-short			11101011	disp										
Indirect within segment			11111111	mod 1 0 0 r/m										
Direct intersegment			11101010	offset-low	offset-high									
Indirect intersegment			11111111	mod 1 0 1 r/m										
RET = Return from CALL:														
Within segment			11000011											
Within seg. adding immmed to SP			11000010	data-low	data-high									
Intersegment			11001011											
Intersegment adding immediate to SP			11001010	data-low	data-high									
JBE/JZ = Jump on equal/zero			01110100	disp										
JL/JNGE = Jump on less/not greater or equal			01111100	disp										
JLE/JNG = Jump on less or equal/not greater			01111110	disp										
JBI/JNAE = Jump on below/not above or equal			01110010	disp										
JBE/JNA = Jump on below or equal/not above			01110110	disp										
JPI/JPE = Jump on parity/parity even			01111010	disp										
JO = Jump on overflow			01110000	disp										
JS = Jump on sign			01111000	disp										
JNE/JNZ = Jump on not equal/not zero			01110101	disp										
JNL/JSGE = Jump on not less/greater or equal			01111101	disp										
JNLE/JG = Jump on not less or equal/greater			01111111	disp										
JNB/JAE Jump on not below/above or equal			01110011	disp										
JNBE/JA Jump on not below or equal/above			01110111	disp										
JNP/JPO = Jump on not par/par odd			01111011	disp										
JNO = Jump on not overflow			01110001	disp										
JNS Jump on not sign			01111001	disp										
LOOP Loop CX times			11100010	disp										
LOOPNZ/LOOPE Loop while zero/equal			11100011	disp										
LOOPNZ/LOOPE Loop while not zero/equal			11100000	disp										
JCXZ Jump on CX zero			11100011	disp										
INT Interrupt														
Type specified			11001101	type										
Type 3			11001100											
INTO = Interrupt on overflow			11001110											
IRET Interrupt return			11001111											
PROCESSOR CONTROL														
CLC Clear carry			11111000											
CMC Complement carry			11110101											
STC Set carry			11111001											
CLD Clear direction			11111100											
STD Set direction			11111101											
CLI Clear interrupt			11111010											
STI Set interrupt			11111011											
HLT Halt			11110100											
WAIT Wait			10011011											
ESC Escape (to external device)			11011xxx	mod x x x r/m										
LOCK Bus lock prefix			11110000											

Footnotes:

AL = 8-bit accumulator
 AX = 16-bit accumulator
 CX = Count register
 DS = Data segment
 ES = Extra segment
 Above/below refers to unsigned value.
 Greater = more positive.
 Less = less positive (more negative) signed values
 if $d = 1$ then "to" reg if $d = 0$ then "from" reg
 if $w = 1$ then word instruction; if $w = 0$ then byte instruction

if mod = 11 then r/m is treated as a REG field
 if mod = 00 then DISP = 0, disp-low and disp-high are absent
 if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
 if mod = 10 then DISP = disp-high; disp-low
 if r/m = 000 then EA = (BX) + (SI) + DISP
 if r/m = 001 then EA = (BX) + (DI) + DISP
 if r/m = 010 then EA = (BP) + (SI) + DISP
 if r/m = 011 then EA = (BP) + (DI) + DISP
 if r/m = 100 then EA = (SI) + DISP
 if r/m = 101 then EA = (DI) + DISP
 if r/m = 110 then EA = (BP) + DISP
 if r/m = 111 then EA = (BX) + DISP
 DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high; disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
 if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
 if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
 x = don't care
 z is used for string primitives for comparison with ZF FLAG.
SEGMENT OVERRIDE PREFIX
 0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-bit [w = 1]	8-bit [w = 0]	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X.X.X.X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

82C37A-5 CHMOS HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER

- Pin Compatible with NMOS 8237A-5
- Enable/Disable Control of Individual DMA Requests
- Four Independent DMA Channels
- Independent Autoinitialization of all Channels
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- High performance: 5 MHz Speed Transfers up to 1.6 MBytes/Second
- Directly Expandable to any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals

The Intel 82C37A-5 Multimode Direct Memory Access (DMA) Controller is a CHMOS peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 82C37A-5 offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 82C37A-5 is designed to be used in conjunction with an external 8-bit address register. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process (EOP).

Each channel has a full 64K address and word count capability.

The 82C37A-5 will not be available from Intel until late 1985.

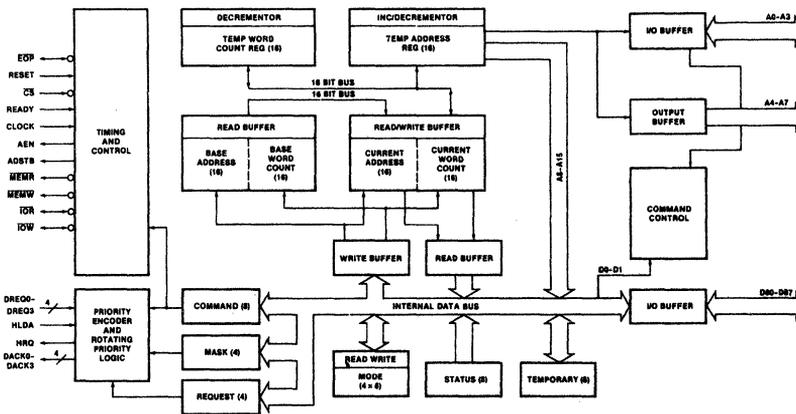


Figure 1. Block Diagram

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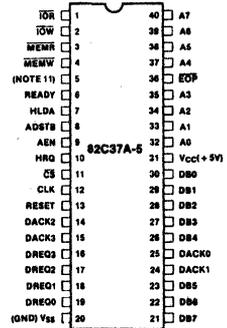


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
V _{CC}		POWER: +5 volt supply.
V _{SS}		GROUND: Ground.
CLK	I	CLOCK INPUT: Clock Input controls the internal operations of the 82C37A-5 and its rate of data transfers. The input may be driven at up to 5 MHz for the 82C37A-5.
\overline{CS}	I	CHIP SELECT: Chip Select is an active low input used to select the 82C37A-5 as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	RESET: Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip-flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	READY: Ready is an input used to extend the memory read and write pulses from the 82C37A-5 to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0–DREQ3	I	DMA REQUEST: The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0–DB7	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 82C37A-5 control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 82C37A-5 on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
\overline{IOR}	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 82C37A-5 to access data from a peripheral during a DMA Write transfer.
\overline{IOW}	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 82C37A-5. In the Active cycle, it is an output control signal used by the 82C37A-5 to load data to the peripheral during a DMA Read transfer.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
\overline{EOP}	I/O	END OF PROCESS: End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional \overline{EOP} pin. The 82C37A-5 allows an external signal to terminate an active DMA service. This is accomplished by pulling the \overline{EOP} input low with an external \overline{EOP} signal. The 82C37A-5 also generates a pulse when the terminal count (TC) for any channel is reached. This generates an \overline{EOP} signal which is output through the \overline{EOP} Line. The reception of \overline{EOP} , either internal or external, will cause the 82C37A-5 to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by \overline{EOP} unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, \overline{EOP} will be output when the TC for channel 1 occurs. \overline{EOP} should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
A0–A3	I/O	ADDRESS: The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4–A7	O	ADDRESS: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	HOLD REQUEST: This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 82C37A-5 to issue the HRQ. After HRQ goes active at least one clock cycle (TCY) must occur before HLDA goes active.
DACK0–DACK3	O	DMA ACKNOWLEDGE: DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	ADDRESS ENABLE: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	ADDRESS STROBE: The active high, Address Strobe is used to strobe the upper address byte into an external latch.
\overline{MEMR}	O	MEMORY READ: The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
\overline{MEMW}	O	MEMORY WRITE: The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

FUNCTIONAL DESCRIPTION

The 82C37A-5 block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The 82C37A-5 contains 344 bits of internal memory in the form of registers. Figure 3 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 3. 82C37A-5 Internal Registers

The 82C37A-5 contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 82C37A-5. The Program Command Control block decodes the various commands given to the 82C37A-5 by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In 82C37A-5 systems this input will usually be the $\phi 2$ TTL clock from an 8224 or CLK from an 8085AH or 82C84A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) does not satisfy 82C37A-5 clock LOW and HIGH time requirements. In this case, an external clock should be used to drive the 82C37A-5.

DMA Operation

The 82C37A-5 is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 82C37A-5 can assume seven separate states, each composed of one full clock period. State 1 (S1) is the inactive state. It is entered when the 82C37A-5 has no valid DMA requests pending. While in S1, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 82C37A-5 has requested a hold but the processor has not yet returned an acknowl-

edge. The 82C37A-5 may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 82C37A-5. Note that the data is transferred directly from the I/O device to memory (or vice versa) with \overline{IOR} and \overline{MEMW} (or \overline{MEMR} and \overline{IOW}) being active at the same time. The data is not read into or driven out of the 82C37A-5 in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

IDLE CYCLE

When no channel is requesting service, the 82C37A-5 will enter the Idle cycle and perform "S1" states. In this cycle the 82C37A-5 will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample \overline{CS} , looking for an attempt by the microprocessor to write or read the internal registers of the 82C37A-5. When \overline{CS} is low and HLDA is low, the 82C37A-5 enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The \overline{IOR} and \overline{IOW} lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 82C37A-5 in the Program Condition. These commands are decoded as sets of addresses with the \overline{CS} and \overline{IOW} . The commands do not make use of the data bus. Instructions include Clear First/Last Flip-Flop and Master Clear.

ACTIVE CYCLE

When the 82C37A-5 is in the Idle cycle and a non-masked channel requests a DMA service, the device

will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode — In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count “rolls over” from zero to FFFFH, a Terminal Count (TC) will cause an Auto-initialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, in 8080A, 8085AH, 80C88, or 80C86 system this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 82C37A-5 and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode — In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process (EOP) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode — In Demand Transfer mode the device is programmed to continue making transfers until a TC or external EOP is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 82C37A-5 Current Address and Current Word Count registers. Only an EOP can cause an Autoinitialize at the end of the service. EOP is generated either by TC or by an external signal.

Cascade Mode — This mode is used to cascade more than one 82C37A-5 together for simple system expansion. The HRQ and HLDA signals from the additional 82C37A-5 are connected to the DREQ and DACK signals of a channel of the initial 82C37A-5. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 82C37A-5 is used only for prioritizing the additional device, it does not output any address

or control signals of its own. These could conflict with the outputs of the active channel in the added device. The 82C37A-5 will respond to DREQ and DACK but all other outputs except HRQ will be disabled. The ready input is ignored.

Figure 4 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More 82C37A-5s could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

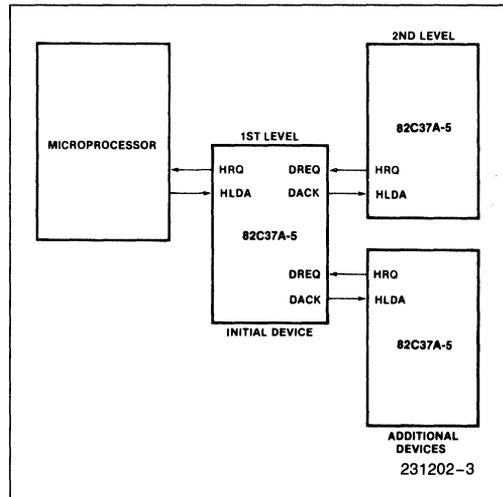


Figure 4. Cascaded 82C37A-5s

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from and I/O device to the memory by activating MEMW and IOR. Read transfers move data from memory to an I/O device by activating MEMR and IOW. Verify transfers are pseudo transfers. The 82C37A-5 operates as in Read or Write transfers generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. The ready input is ignored in verify mode.

Memory-to-Memory — To perform block moves of data from one memory address space to another with a minimum of program effort and time, the 82C37A-5 includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 to 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The

82C37A-5 requests a DMA service in the normal manner. After HLDA is true, the device, using four state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 82C37A-5 internal Temporary register. Channel 1 then performs a four-state transfer of the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an EOP output terminating the service.

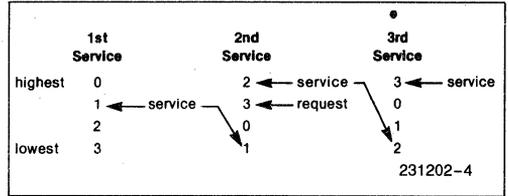
Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

The 82C37A-5 will respond to external \overline{EOP} signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 12. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Autoinitialize — By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following \overline{EOP} . The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not altered when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected. In order to Autoinitialize both channels in a memory-to-memory transfer, both word counts should be programmed identically. If interrupted externally, \overline{EOP} pulses should be applied in both bus cycles.

Priority — The 82C37A-5 has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing — In order to achieve even greater throughput where system characteristics permit, the 82C37A-5 can compress the transfer time to two clock cycles. From Figure 11 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 14.

Address Generation — In order to reduce pin count, the 82C37A-5 multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits into the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 82C37A-5 directly. Lines A0-A7 should be connected to the address bus. Figure 11 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 82C37A-5 executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register — Each channel has a 16-bit Current Address register. This register holds

the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an EOP.

Current Word Register — Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an EOP occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

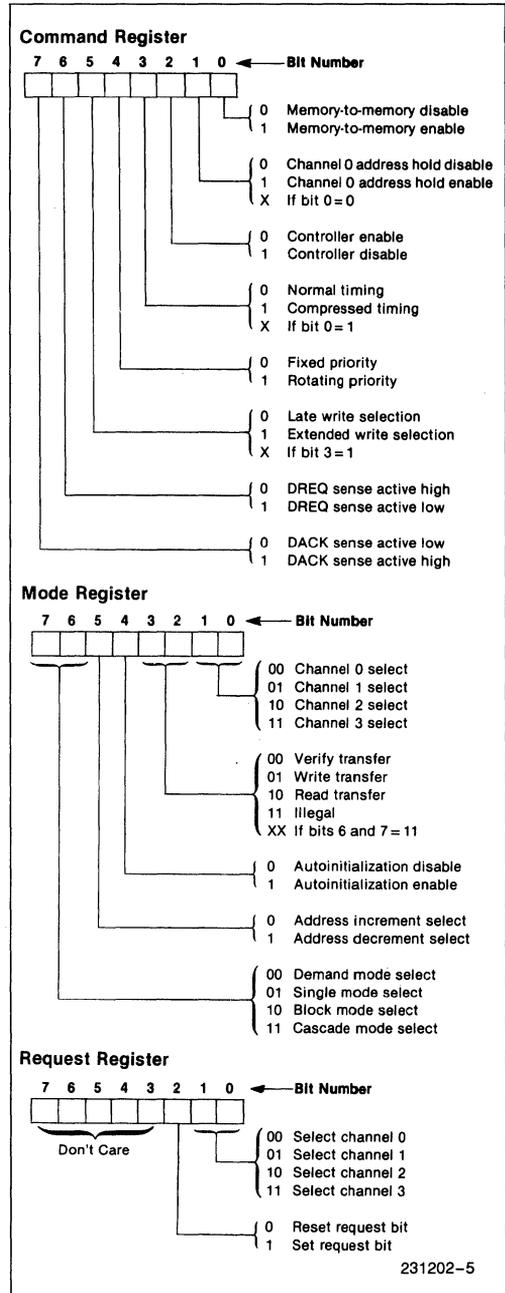
Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register — This 8-bit register controls the operation of the 82C37A-5. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 6 for address coding.

Mode Register — Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

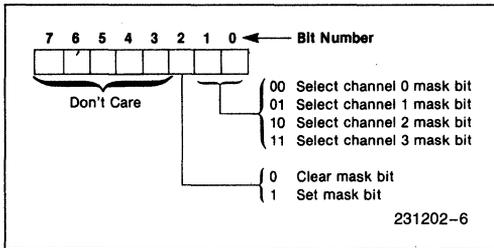
Request Register — The 82C37A-5 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each

register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register ad-

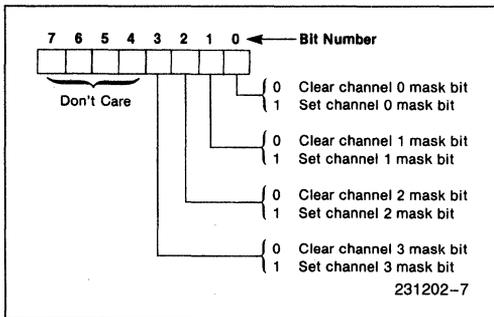


dress coding. In order to make a software request, the channel must be in Block Mode.

Mask Register — Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an \overline{EOP} if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 5 for instruction addressing.



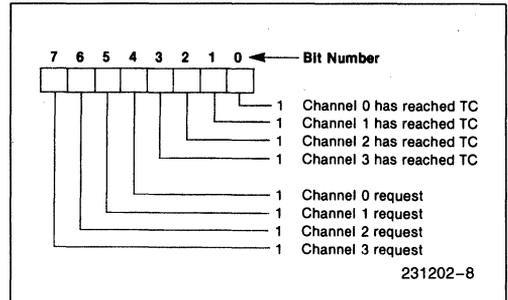
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		CS	IOR	IOW	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 5. Definition of Register Codes

Status Register — The Status register is available to be read out of the 82C37A-5 by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0–3 are set every time a TC is reached by that channel or an external \overline{EOP} is applied. These bits are cleared upon Reset and on each Status Read. Bits 4–7 are set whenever their corresponding channel is requesting service.



Temporary Register — The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands — These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The three software commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 82C37A-5. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 82C37A-5 will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 6 lists the address codes for the software commands:

Signals						Operation
A3	A2	A1	A0	IOR	IOW	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip-Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 6. Software Command Codes

PROGRAMMING

The 82C37A-5 will accept programming from the host processor any time that HLDA is inactive; this is true even if HRQ is active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the 82C37A-5 is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 82C37A-5 is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

Channel	Register	Operation	Signals						Internal Flip-Flop	Data Bus DB0-DB7	
			CS	IOR	IOW	A3	A2	A1			A0
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
	Current Address	Read	0	1	0	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	0	1	0	0	0	0	0	A0-A7
	Current Word Count	Read	0	0	1	0	0	0	0	1	A8-A15
1	Base and Current Address	Write	0	1	0	0	0	0	1	0	W0-W7
	Current Address	Read	0	1	0	0	0	0	1	1	W8-W15
	Base and Current Word Count	Write	0	0	1	0	0	1	0	0	W0-W7
	Current Word Count	Read	0	0	1	0	0	1	1	0	W8-W15
2	Base and Current Address	Write	0	0	1	0	0	1	0	1	W0-W7
	Current Address	Read	0	0	1	0	1	0	0	0	W8-W15
	Base and Current Word Count	Write	0	0	1	0	1	0	0	1	W0-W7
	Current Word Count	Read	0	0	1	0	1	0	1	0	W8-W15
3	Base and Current Address	Write	0	0	1	0	1	0	1	0	W0-W7
	Current Address	Read	0	0	1	0	1	1	0	1	W8-W15
	Base and Current Word Count	Write	0	0	1	0	1	1	0	0	W0-W7
	Current Word Count	Read	0	0	1	0	1	1	1	0	W8-W15

Figure 7. Word Count and Address Register Command Codes

After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

APPLICATION INFORMATION

Figure 8 shows a convenient method for configuring a DMA system with the 82C37A-5 controller and an 8080A/8085AH microprocessor system. The multi-mode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request

from a peripheral device. When the processor replies with a HLDA signal, the 82C37A-5 takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes — the least significant 8 bits on the eight address outputs and the most significant 8 bits on the data bus. The contents of the data bus are then latched into the 8-bit latch to complete the full 16 bits of the address bus. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one 82C37A-5 is used.

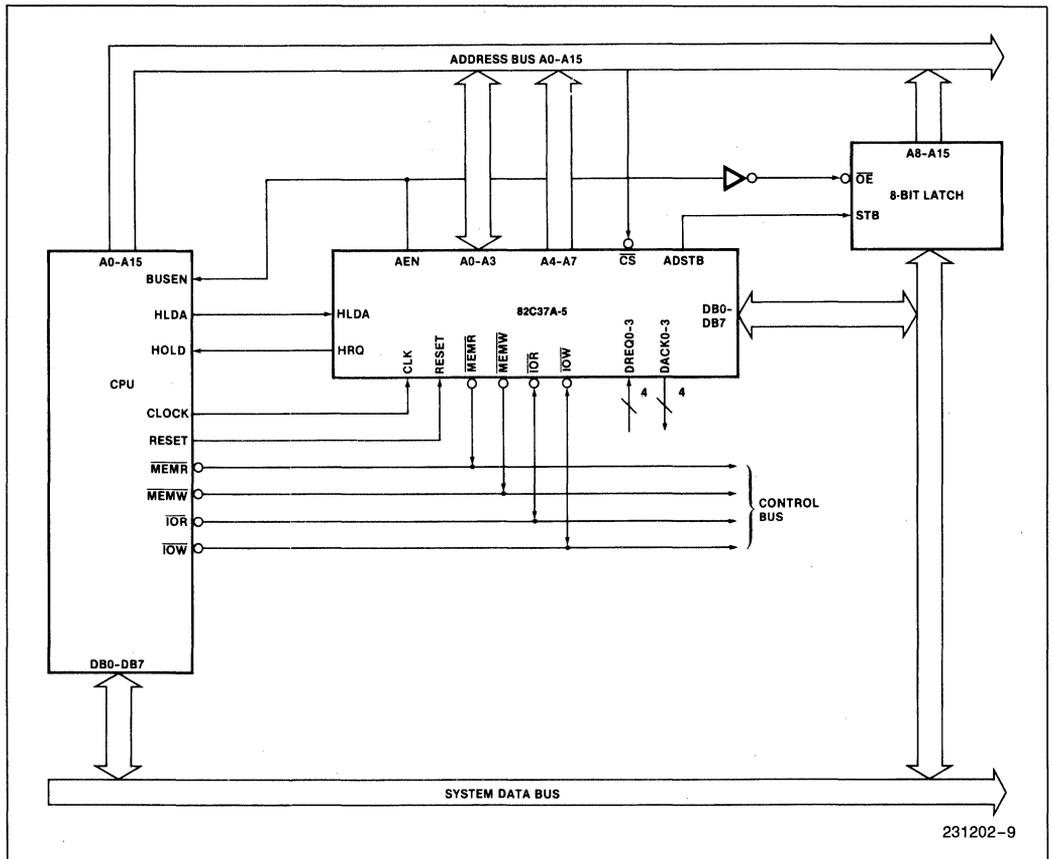


Figure 8. 82C37A-5 System Interface

82C59A-2 CMOS Programmable Interrupt Controller

- Pin Compatible with NMOS 8259A-2
- Eight-Level Priority Controller
- Expandable to 64 levels
- Programmable Interrupt Modes
- Low Standby Power—10 μ A
- Individual Request Mask Capability
- 80C86/88 and 8080/85/86/88 Compatible
- Fully Static Design
- Single 5V Power Supply

The Intel 82C59A-2 is a high performance CMOS Version of the NMOS 8259A-2 Priority Interrupt Controller. The 82C59A is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The high speed and industry standard configuration of the 82C59A-2, make it compatible with microprocessors such as the 80C86/88, 8086/88 and 8080/85.

The 82C59A-2 can handle up to 8 vectored priority interrupts for the CPU and is cascadable to 64 without additional circuitry. It is designed to minimize the software and real time overhead in handling multi-level priority interrupts. Two modes of operation make the 82C59A-2 optimal for a variety of system requirements. Static CMOS circuit design, requiring no clock input, insures low operating power. It is packaged in a 28-pin plastic DIP.

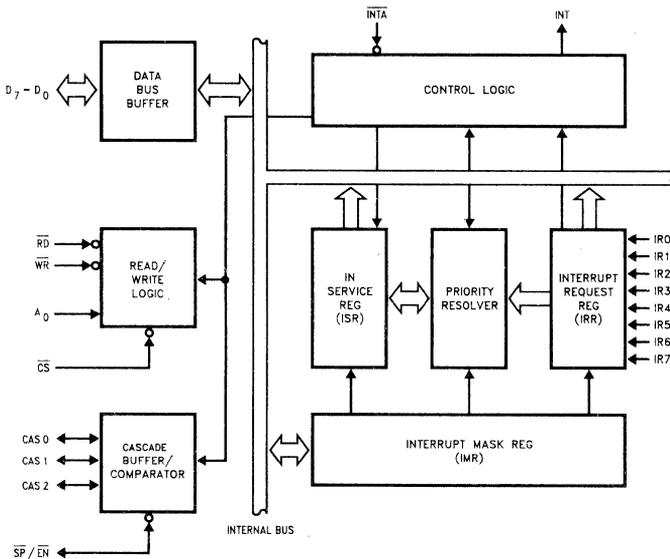


Figure 1. Block Diagram

231201-1

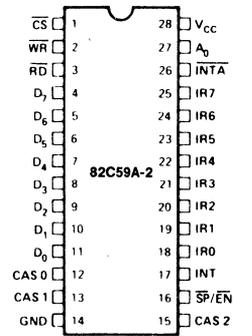


Figure 2. Pin Configuration

231201-2

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V _{CC}	28	I	SUPPLY: +5V Supply.
GND	14	I	GROUND.
\overline{CS}	1	I	CHIP SELECT: A low on this pin enables \overline{RD} and \overline{WR} communication between the CPU and the 82C59A-2. INTA functions are independent of CS.
\overline{WR}	2	I	WRITE: A low on this pin when \overline{CS} is low enables the 82C59A-2 to accept command words from the CPU.
\overline{RD}	3	I	READ: A low on this pin when \overline{CS} is low enables the 82C59A-2 to release status onto the data bus for the CPU.
D ₇ -D ₀	4-11	I/O	BIDIRECTIONAL DATA BUS: Control, status and interrupt-vector information is transferred via this bus.
CAS ₀ -CAS ₂	12, 13, 15	I/O	CASCADE LINES: The CAS lines form a private 82C59A-2 bus to control a multiple 82C59A-2 structure. These pins are outputs for a master 82C59A-2 and inputs for a slave 82C59A-2.
$\overline{SP}/\overline{EN}$	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR ₀ -IR ₇	18-25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
\overline{INTA}	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 82C59A-2 interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A ₀	27	I	AO ADDRESS LINE: This pin acts in conjunction with the \overline{CS} , \overline{WR} , and \overline{RD} pins. It is used by the 82C59A-2 to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 80C86, 80C88).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The 82C59A-2

The 82C59A-2 is a device specifically designed for use in real time, interrupt driven microcomputer sys-

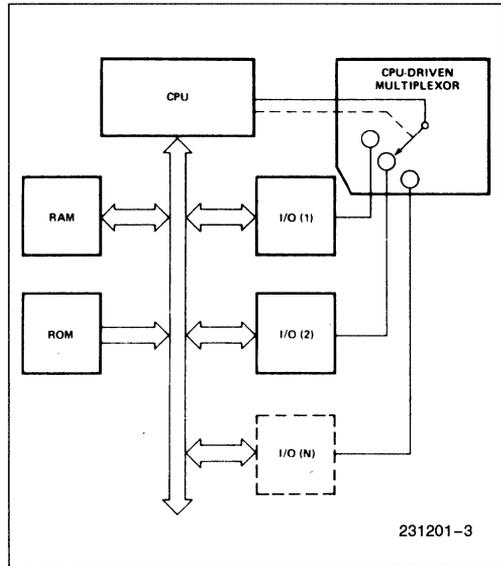


Figure 3a. Polled Method

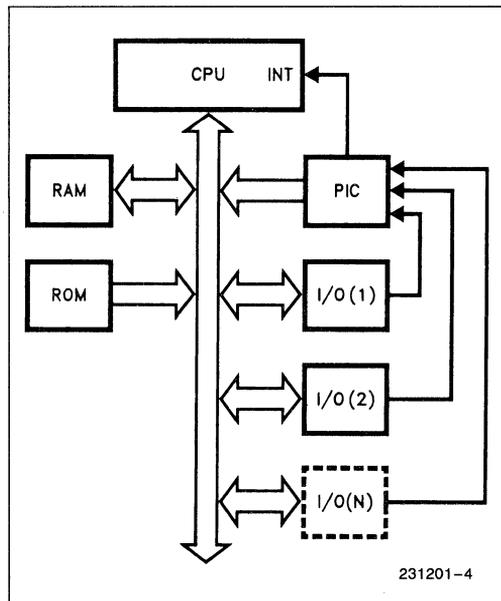


Figure 3b. Interrupt Method

tems. It manages eight levels or requests and has built-in features for expandability to other 82C59A-2's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 82C59A-2 can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{\text{INTA}}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A, 80C88 and 80C86 input levels.

$\overline{\text{INTA}}$ (INTERRUPT ACKNOWLEDGE)

$\overline{\text{INTA}}$ pulses will cause the 82C59A-2 to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 82C59A-2.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 82C59A-2 to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 82C59A-2 to be transferred onto the Data Bus.

$\overline{\text{CS}}$ (CHIP SELECT)

A LOW on this input enables the 82C59A-2. No reading or writing of the chip will occur unless the device is selected.

$\overline{\text{WR}}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 82C59A-2.

$\overline{\text{RD}}$ (READ)

A LOW on this input enables the 82C59A-2 to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 82C59A-2's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 82C59A-2 is used as a master and are inputs when the 82C59A-2 is used as a slave. As a master, the 82C59A-2 sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses. (See section "Cascading the 82C59A-2".)

INTERRUPT SEQUENCE

The powerful features of the 82C59A-2 in a micro-computer system are its programmability and the interrupt routine addressing capability. The latter al-

lows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

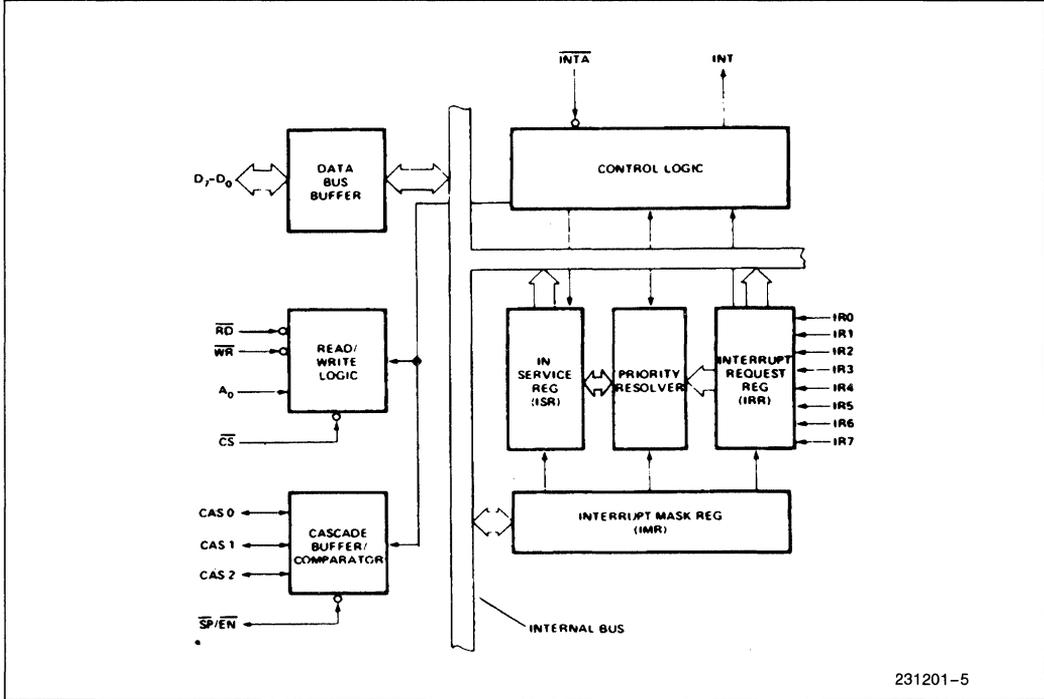


Figure 4. 82C59A-2 Block Diagram

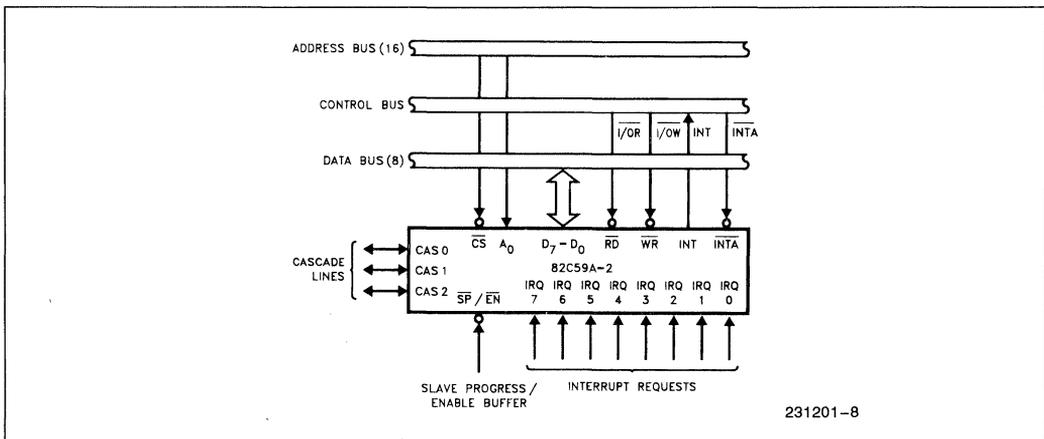


Figure 5. 82C59A-2 Interface to Standard System Bus

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST Lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 82C59A-2 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an \overline{INTA} pulse.
4. Upon receiving an \overline{INTA} from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A-2 will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more \overline{INTA} pulses to be sent to the 82C59A-2 from the CPU group.
6. These two \overline{INTA} pulses allow the 82C59A-2 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first \overline{INTA} pulse and the higher 8-bit address is released at the second \overline{INTA} pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A-2. In the AEOI mode the ISR bit is reset at the end of the third \overline{INTA} pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86 system are the same until step 4.

4. Upon receiving an \overline{INTA} from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 82C59A-2 does not drive the Data Bus during this cycle.
5. The 80C86 will initiate a second \overline{INTA} pulse. During this pulse, the 82C59A-2 releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second \overline{INTA} pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt is present at step 4 of either sequence (i.e., the request was too short in duration) the 82C59A-2 will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

INTERRUPT SEQUENCE OUTPUTS

MCS®-80, MCS-85

This sequence is timed by three \overline{INTA} pulses. During the first \overline{INTA} pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second \overline{INTA} pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A₅-A₇ are programmed, while A₀-A₄ are automatically inserted by the 82C59A-2. When Interval = 8 only A₆ and A₇ are programmed, while A₀-A₅ are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third \overline{INTA} pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A₈ - A₁₅), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 80C88

80C86, 80C88 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 82C59A-2 uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 80C86, 80C88 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A₅-A₁₁ are unused in 80C86, 80C88 mode):

Content of Interrupt Vector Byte for 80C86, 80C88 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 82C59A-2

The 82C59A-2 accepts two types of command words generated by the CPU:

- 1. Initialization Command Words (ICWs):** Before normal operation can begin, each 82C59A-2 in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by WR pulses.
- 2. Operation Command Words (OCWs):** These are the command words which command the 82C59A-2 to operate in various interrupt modes. These modes are:
 - a. Fully nested mode
 - b. Rotating priority mode
 - c. Special mask mode
 - d. Polled mode

The OCWs can be written into the 82C59A-2 any-time after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

GENERAL

Whenever a command is issued with A₀ = 0 and D₄ = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

- a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
- b. The Interrupt Mask Register is cleared.
- c. IR7 input is assigned priority 7.
- d. The slave mode address is set to 7.
- e. Special Mask Mode is cleared and Status Read is set to IRR.
- f. If IC₄ = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

***NOTE:**

Master/Slave in ICW4 is only used in the buffered mode.

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

A₅-A₁₅: *Page starting address of service routines.* In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A₀-A₁₅). When the routine interval is 4, A₀-A₄ are automatically inserted by the 82C59A-2, while A₅-A₁₅ are programmed externally. When the routine interval is 8, A₀-A₅ are automatically inserted by the 82C59A-2, while A₆-A₁₅ are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 80C86, 80C88 system A₁₅-A₁₁ are inserted in the five most significant bits of the vectoring

byte and the 82C59A-2 sets the three least significant bits according to the interrupt level. A₁₀-A₅ are ignored and ADI (Address Interval) has no effect:

LTIM: If LTIM = 1, then the 82C59A-2 will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SINGL: Single. Means that this is the only 82C59A-2 in the system. If SINGL = 1 no ICW3 will be issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 82C59A-2 in the system and cascading is used, in which case SINGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86, 80C88 only byte 2) through the cascade lines.

b. In the slave mode (either when \overline{SP} = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86, 80C88 are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

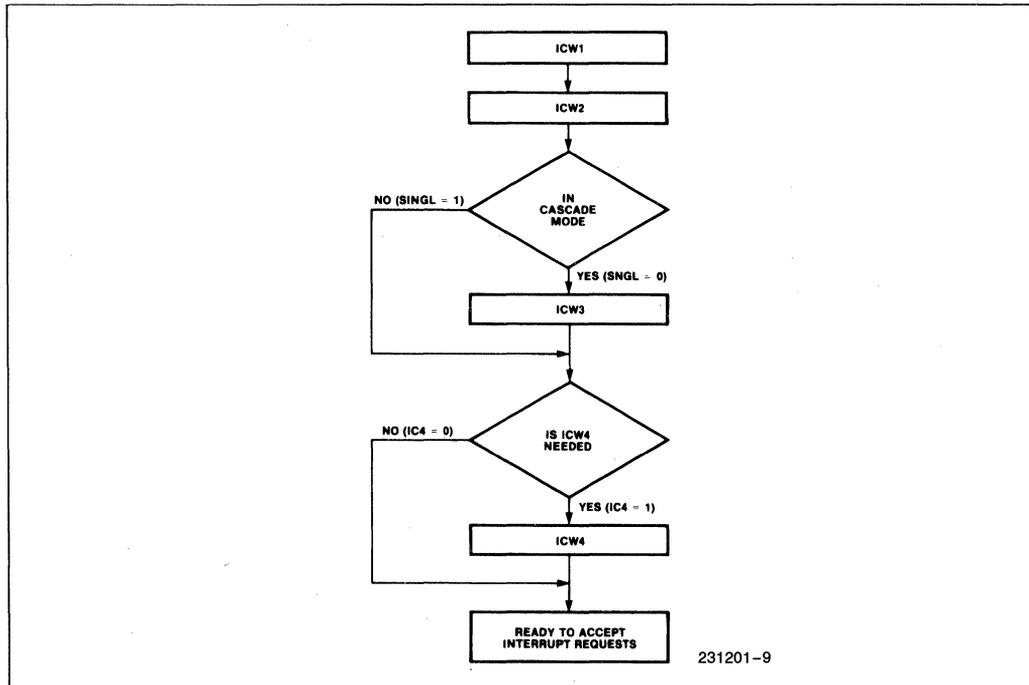
SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A-2 is programmed to be a master, M/S = 0 means the 82C59A-2 is programmed to be a slave. If BUF = 0, M/S has no function.

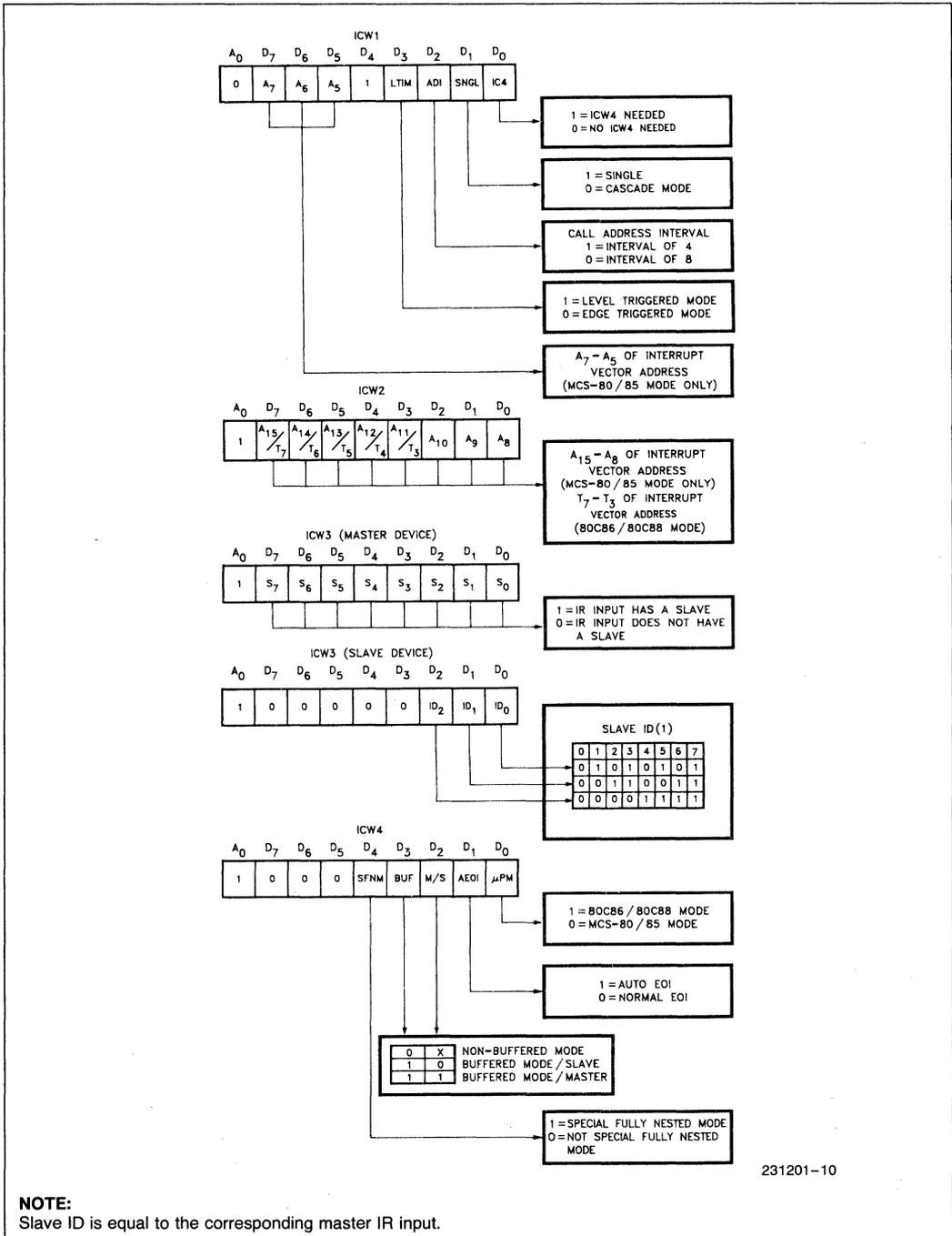
AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μ PM: Microprocessor mode: μ PM = 0 sets the 82C59A-2 for MCS-80, 85 system operation, μ PM = 1 sets the 82C59A-2 for 80C86 system operation.



231201-9

Figure 6. Initialization Sequence



231201-10

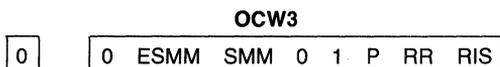
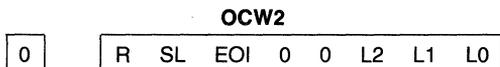
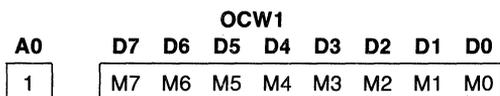
NOTE:
Slave ID is equal to the corresponding master IR input.

Figure 7. Initialization Command Word Format

OPERATION COMMAND WORDS (OCWs)

After the initialization Command Words (ICWs) are programmed into the 82C59A-2, the chip is ready to accept interrupt requests at its input lines. However, during the 82C59A-2 operation, a selection of algorithms can command the 82C59A-2 to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)



OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M₇–M₀ represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L₂, L₁, L₀—These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)

ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a “don’t care”.

SMM — Special Mask Mode. If ESMM = 1 and SMM = 1 the 82C59A-2 will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 82C59A-2 will revert to normal mask mode. When ESMM = 0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR₀ has the highest priority and IR₇ the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

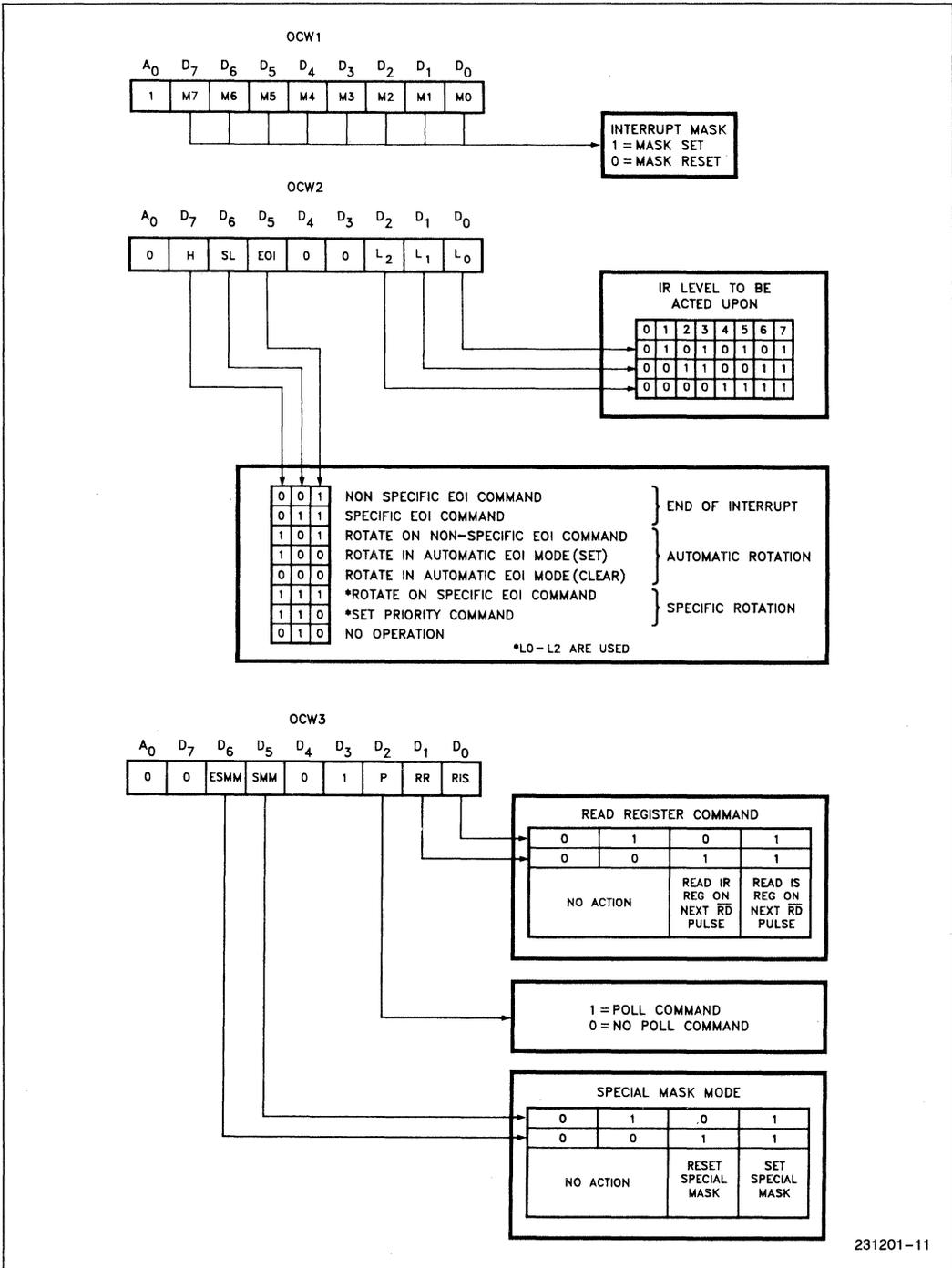
END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence INTA pulse (when AEOI bit in ICW4 is set) or by a command word that must be issued to the 82C59A-2 before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 82C59A-2 is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 82C59A-2 will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 82C59A-2 may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L₀-L₂ is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 82C59A-2 is in the Special Mask Mode.



231201-11

Figure 8. Operation Command Word Format

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI = 1 in ICW4, then the 82C59A-2 will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 82C59A-2 will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in 80C86/88). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 82C59A.

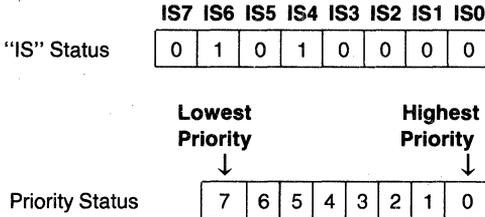
The AEOI mode can only be used in a master 82C59A and not a slave.

AUTOMATIC ROTATION

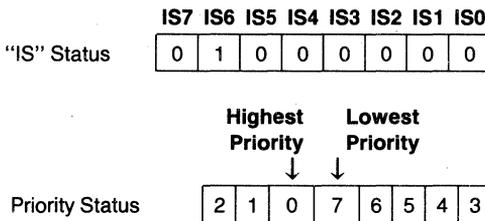
(Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)



After Rotate (IR4 was serviced, all other priorities rotated correspondingly)



There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Ro-

tate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

SPECIFIC ROTATION

(Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; LO-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and LO-L2 = IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 82C59A-2 would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

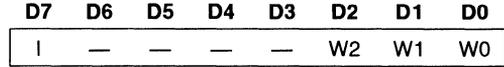
POLL COMMAND

In this mode the INT output is not used or the micro-processor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = "1" in OCW3. The 82C59A-2 treats the next RD pulse to the 82C59A-2 (i.e., RD = 0, CS = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a

request, and reads the priority level. Interrupt is frozen from WR to RD.

The word enabled onto the data bus during RD is:



WO-W2:

Binary code of the highest priority level requesting service.

1: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the INTA sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

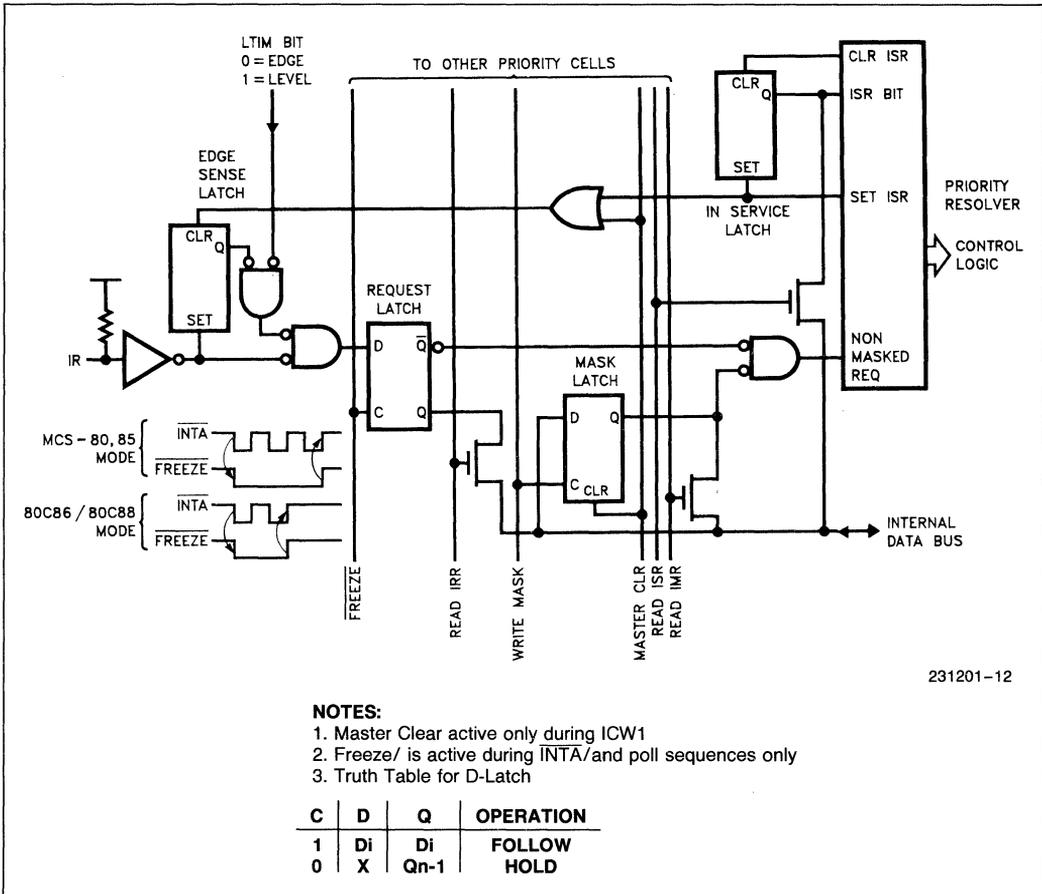


Figure 9. Priority Cell—Simplified Logic Diagram

READING THE 82C59A-2 STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1):

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 82C59A-2 "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 82C59A-2 is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever \overline{RD} is active and AO = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EO1 command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 82C59A-2. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

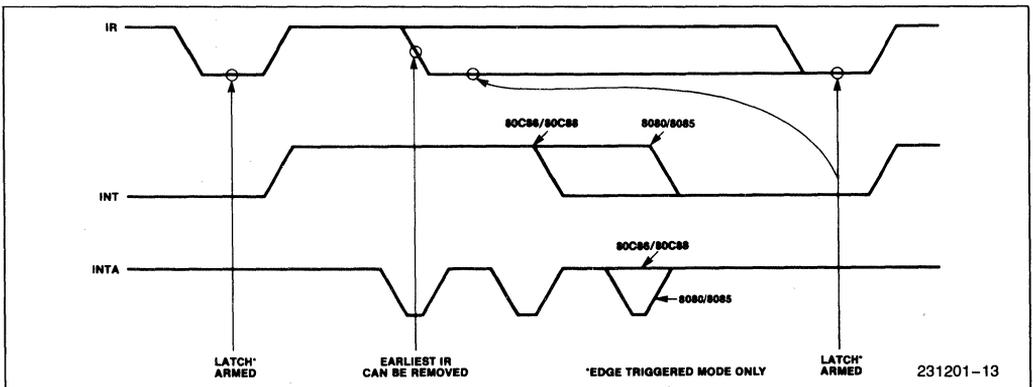


Figure 10. IR Triggering Timing Requirements

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

- a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)
- b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the 82C59A-2 is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 82C59A-2 to send an enable signal on SP/EN to enable the buffers. In this mode, whenever the 82C59A-2's data bus outputs are enabled, the SP/EN output becomes active.

This modification forces the use of software programming to determine whether the 82C59A-2 is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW3 determines whether it is a master or a slave.

CASCADE MODE

The 82C59A-2 can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the INTA sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 80C86/80C88).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 82C59A-2 in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 82C59A-2.

The cascade lines of the Master 82C59A-2 are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

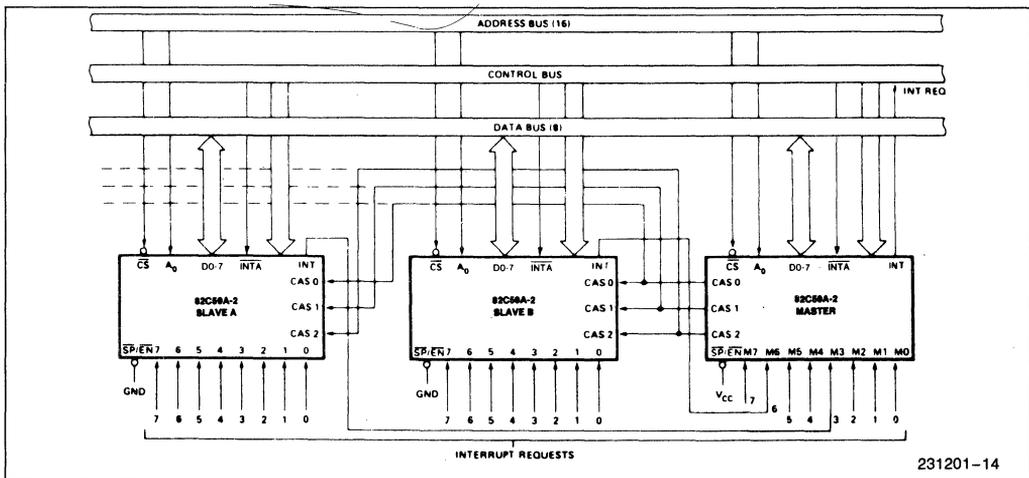


Figure 11. Cascading the 82C59A-2

231201-14

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to 70°C
 Storage Temperature -65°C to + 150°C
 Supply Voltage (w.r.t. ground) -0.5 to 8.0V
 Operating Supply Voltage (w.r.t. ground) . 4.0 to 7.0V
 Input Voltage (w.r.t. ground) . . . -2.0 to V_{CC} + 0.5V
 Output Voltage (w.r.t. ground) . . -0.5 to V_{CC} + 0.5V
 Power Dissipation 1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS [T_A = 0°C to 70°C, V_{CC} = 5V ± 10%]

Symbol	Parameter	Min	Max	Units	Test Conditions
I _{CCS}	Standby Supply Current		10	μA	V _{IN} = V _{CC} or GND Outputs Unloaded V _{CC} = 5.5V
I _{CC}	Operating Supply Current		5	mA	(Note)
V _{IH}	Input High Voltage	2.0		V	
V _{IL}	Input Low Voltage		0.8	V	
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 2.5 mA
V _{OH}	Output High Voltage	3.0 V _{CC} - 0.4		V	I _{OH} = -2.5 mA I _{OH} = -100 μA
I _{LI}	Input Leakage Current		± 1.0	μA	0V ≤ V _{IN} ≤ V _{CC}
I _{LO}	Output Leakage Current		± 10	μA	0V ≤ V _{OUT} ≤ V _{CC}
I _{LIR}	IR Input Leakage Current		-300 + 10	μA	V _{IN} = 0 V _{IN} = V _{CC}

NOTE: Repeated data input with 80C86-2 timings.

CAPACITANCE (T_A = 25°C; V_{CC} = GND = 0V)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C _{IN}	Input Capacitance			5	pF	f _c = 1 MHz
C _{I/O}	I/O Capacitance			20	pF	Unmeasured pins at GND
C _{OUT}	Output Capacitance			15	pF	

A.C. CHARACTERISTICS [$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 10\%$]

TIMING REQUIREMENTS

Symbol	Parameter	82C59A-2		Units	Test Conditions
		Min	Max		
TAHRL	AO/\overline{CS} Setup to $\overline{RD}/\overline{INTA} \downarrow$	10		ns	
TRHAX	AO/\overline{CS} Hold after $\overline{RD}/\overline{INTA} \uparrow$	5		ns	
TRLRH	$\overline{RD}/\overline{INTA}$ Pulse Width	160		ns	
TAHWL	AO/\overline{CS} Setup to $\overline{WR} \downarrow$	0		ns	
TWHAX	AO/\overline{CS} Hold after $\overline{WR} \uparrow$	0		ns	
TWLWH	\overline{WR} Pulse Width	190		ns	
TDVWH	Data Setup to $\overline{WR} \uparrow$	160		ns	
TWHDX	Data Hold after $\overline{WR} \uparrow$	0		ns	
TJLJH	Interrupt Request Width (Low)	100		ns	(See Note)
TCVIAL	Cascade Setup to Second or Third $\overline{INTA} \downarrow$ (Slave Only)	40		ns	
TRHRL	End of \overline{RD} to next \overline{RD} End of \overline{INTA} to next \overline{INTA} within an \overline{INTA} sequence only	160		ns	
TWHWL	End of \overline{WR} to next \overline{WR}	190		ns	
*TCHCL	End of Command to next Command (Not same command type) End of \overline{INTA} sequence to next \overline{INTA} sequence.	400		ns	

*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6 μs , 8085-A2 = 1 μs , 80C86 = 1 μs , 80C86-2 = 625 ns)

NOTE:

This is the low time required to clear the input latch in the edge triggered mode.

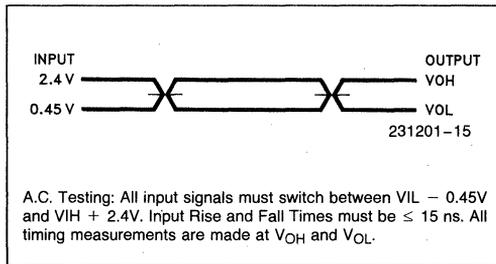
TIMING RESPONSES

Symbol	Parameter	8259A-2		Units	Test Conditions**
		Min	Max		
TRLDV	Data Valid from $\overline{RD}/\overline{INTA} \downarrow$		120	ns	1
TRHDZ	Data Float after $\overline{RD}/\overline{INTA} \uparrow$	10	85	ns	2
TJHIH	Interrupt Output Delay		300	ns	1
TIALCV	Cascade Valid from First $\overline{INTA} \downarrow$ (Master Only)		360	ns	1
TRLEL	Enable Active from $\overline{RD} \downarrow$ or $\overline{INTA} \downarrow$		100	ns	1
TRHEH	Enable Inactive from $\overline{RD} \uparrow$ or $\overline{INTA} \uparrow$		150	ns	1
TAHDV	Data Valid from Stable Address		200	ns	1
TCVDV	Cascade Valid to Valid Data		200	ns	1

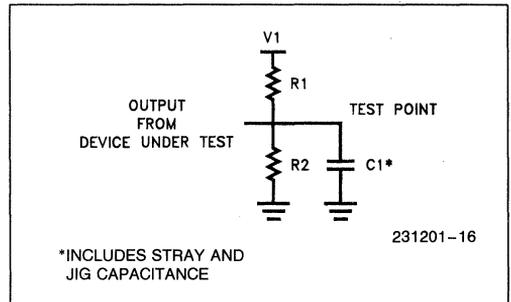
****Test Condition Definition Table**

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	100 pf
2	4.5V	1.8 kΩ	1.8 kΩ	30 pf

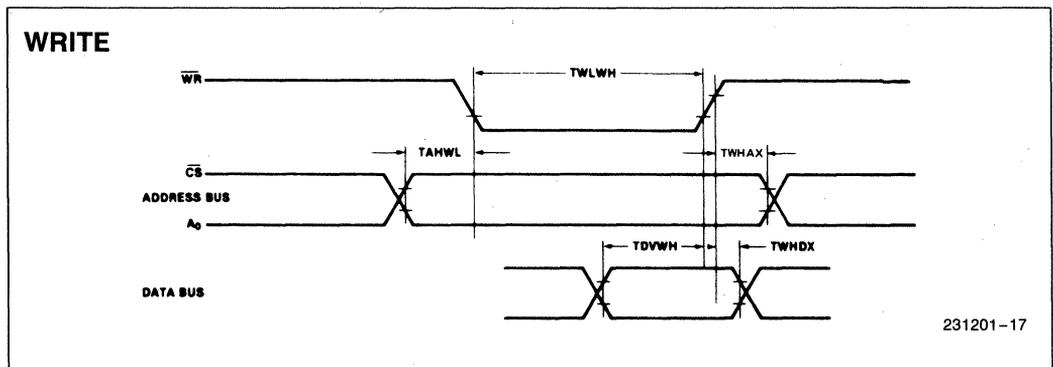
A.C. TESTING INPUT, OUTPUT WAVEFORM



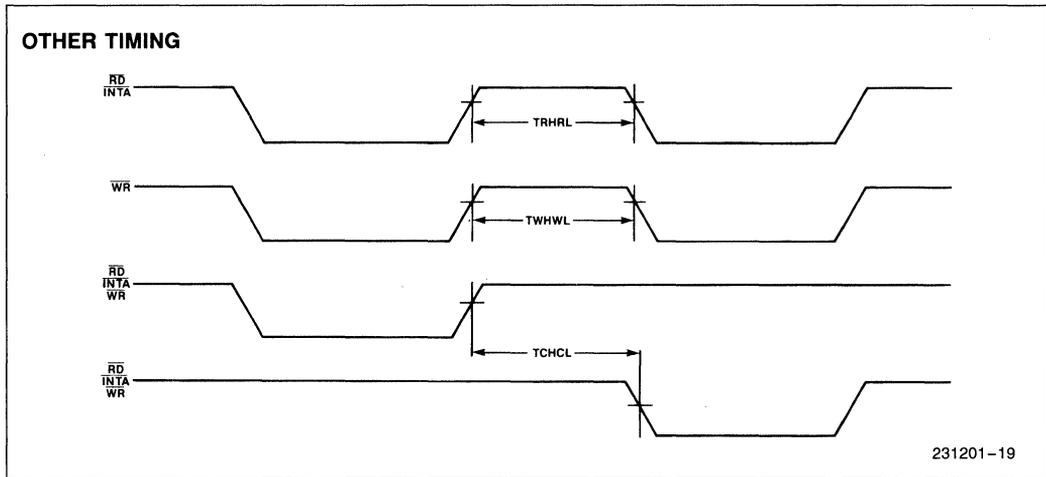
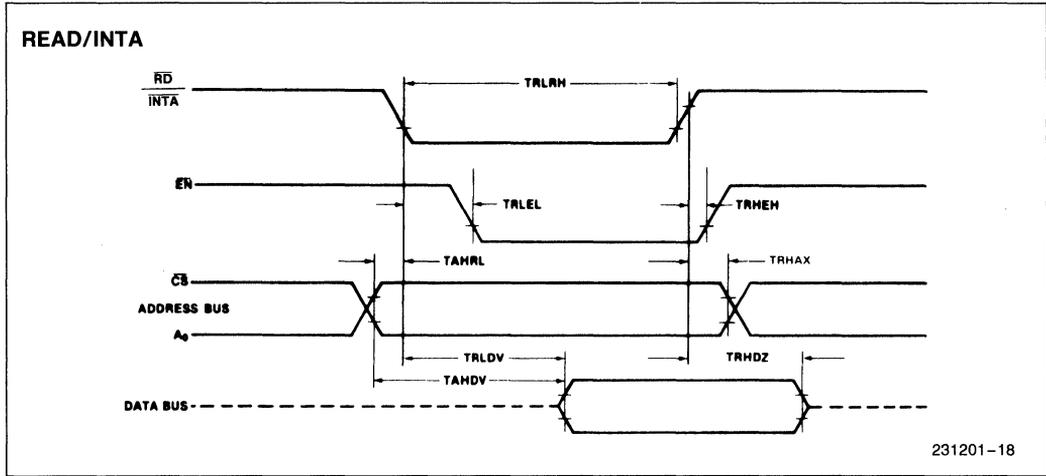
A.C. TESTING LOAD CIRCUIT



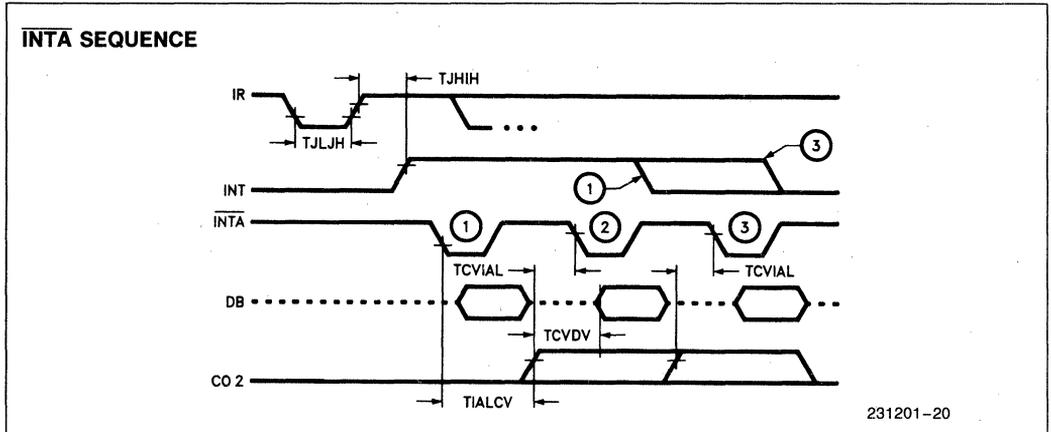
WAVEFORMS



WAVEFORMS (Continued)



WAVEFORMS (Continued)



NOTES:

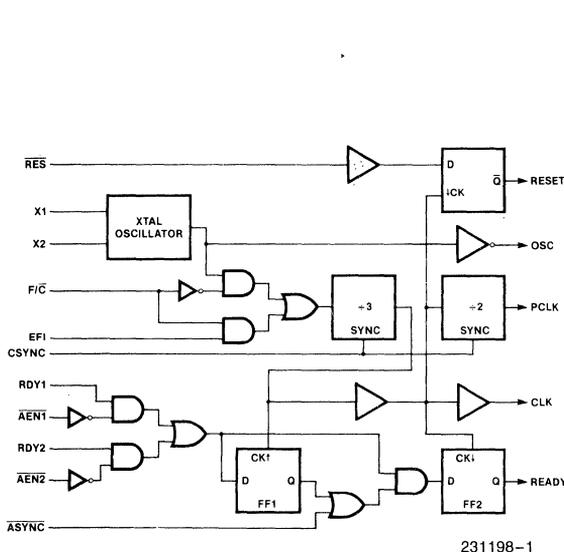
Interrupt output must remain HIGH at least until leading edge of first INTA.

1. Cycle 1 in 80C86 and 80C88 systems, the Data Bus is not active.

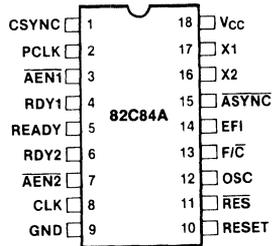
82C84A/82C84A-5 CHMOS CLOCK GENERATOR AND DRIVER FOR 80C86, 80C88 PROCESSORS

- Generates the System Clock for the 80C86, 80C88 Processors:
82C84A-5 for 5 MHz
82C84A for 8 MHz
- Pin Compatible with Bipolar 8284A
- Uses a Crystal or an External Frequency Source
- Provides Local READY and MULTIBUS® READY Synchronization
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with other 82C84As
- Low Power Consumption
- Single 5V Power Supply
- TTL Compatible Inputs/Outputs
- 18-Pin Plastic Package

The Intel 82C84A is a high performance CHMOS clock generator-driver designed to service the requirements of the 80C86/88 and 8086/88. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete READY synchronization and reset logic. Crystal controlled operation up to 15, 25 MHz utilizes a parallel, fundamental mode crystal and two small load capacitors. Power consumption is a fraction of that of equivalent bipolar circuits.



82C84A/82C84A-5 Block Diagram



231198-2

82C84A/82C84A-5 Pin Configuration

Control Pin	Logical 1	Logical 0
F/C	External Clock	Crystal Drive
RES	Normal	Reset
RDY 1 RDY 2	Bus Ready	Bus not ready
AEN 1 AEN 2	Address Disabled	Address Enabled
ASYNC	2 Stage Ready Synchronization	1 Stage Ready Synchronization

**82C84A/82C84A-5
Pin Description**

Table 1. Pin Description

Symbol	Type	Name and Function
AEN1, AEN2	I	ADDRESS ENABLE: $\overline{\text{AEN}}$ is an active LOW signal. AEN serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{\text{AEN1}}$ validates RDY1 while $\overline{\text{AEN2}}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the AEN signal inputs are tied true (LOW).
RDY1, RDY2	I	BUS READY: (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{\text{AEN1}}$ while RDY2 is qualified by $\overline{\text{AEN2}}$.
ASYNC	I	READY SYNCHRONIZATION SELECT: $\overline{\text{ASYNC}}$ is an input which defines the synchronization mode of the READY logic. When $\overline{\text{ASYNC}}$ is LOW, two stages of READY synchronization are provided. When $\overline{\text{ASYNC}}$ is HIGH a single stage of READY synchronization is provided. ($\overline{\text{ASYNC}}$ should never be left open).
READY	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency. (If no crystal is attached, then X1 should be tied to V_{CC} or GND and X2 should be left open.)
F/ \overline{C}	I	FREQUENCY/CRYSTAL SELECT: F/ \overline{C} is a strapping option. When strapped LOW, F/ \overline{C} permits the processor's clock to be generated by the crystal. When F/ \overline{C} is strapped HIGH, CLK is generated from the EFI input.
EFI	I	EXTERNAL FREQUENCY: When F/ \overline{C} is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output. When F/ \overline{C} is strapped LOW, EFI should be tied HIGH or LOW.
CLK	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is $\frac{1}{3}$ of the crystal or EFI input frequency and a $\frac{1}{3}$ duty cycle.
PCLK	O	PERIPHERAL CLOCK: PCLK is a TTL level peripheral clock signal whose output frequency is $\frac{1}{2}$ that of CLK and has a 50% duty cycle.
OSC	O	OSCILLATOR OUTPUT: OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
RES	I	RESET IN: $\overline{\text{RES}}$ is an active LOW signal which is used to generate RESET. The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
RESET	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86/88 family processors. Its timing characteristics are determined by \overline{RES} .
CSYNC	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84A's to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		GROUND.
V _{CC}		POWER: +5V supply.

FUNCTIONAL DESCRIPTION

Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \cdot C2}{C1 + C2} \quad (\text{Including stray capacitance})$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accom-

plished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/\overline{C} input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle MOS clock driver designed to drive the 80C86/88 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input (\overline{RES}) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A.

READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The \overline{AEN} signals validate their respective RDY signals. If a Multi-Master system is not being used the \overline{AEN} pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{\text{ASYNC}}$ input defines two modes of READY synchronization operation.

When $\overline{\text{ASYNC}}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized

directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, T_{R1VCL} , on each bus cycle.

When $\overline{\text{ASYNC}}$ is HIGH, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{\text{ASYNC}}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

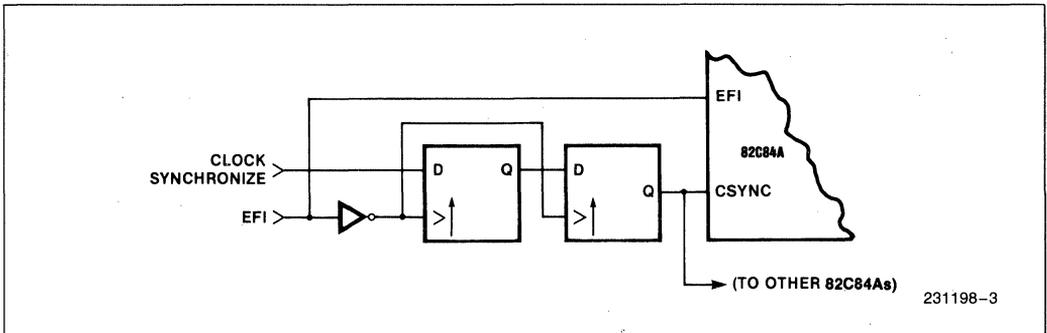


Figure 3. CSYNC Synchronization

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	-0.5V to 7.0V
Operating Supply Voltage	4.0V to 6.0V
Input Voltage Applied	-0.5V to $V_{CC} + 0.5V$
Output Voltage Applied	-0.5V to $V_{CC} + 0.5V$
Storage Temperature	-65°C to +150°C
Ambient Temp. Under Bias	0°C to +70°C
Power Dissipation	1 Watt

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter		Min	Max	Units	Test Conditions
I_{CC}	Operating Supply Current:	82C84A 82C84A-5		40 25	mA	25 MHz xtal, $C_L = 0$ 15 MHz xtal, $C_L = 0$
I_{CCS}	Stand by Supply Current			100	μA	X1 at V_{CC} or GND EF1 at V_{CC} or GND
I_{LI}	Input Leakage Current			± 1.0	μA	$0V \leq V_{IN} \leq V_{CC}$

D.C. CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
V _{IL}	Input LOW Voltage		0.8	V	
V _{IH}	Input HIGH Voltage	2.0		V	
V _{IHR}	Reset Input HIGH Voltage	0.6 V _{CC}		V	
V _{OL}	Output LOW Voltage		0.4	V	CLK: I _{OL} = 4 mA (Note) Others: I _{OL} = 2.5 mA (Note)
V _{OH}	Output HIGH Voltage	V _{CC} - 0.4		V	CLK: I _{OH} = -4 mA Others: I _{OH} = -2.5 mA
V _{IHR} -V _{ILR}	\overline{RES} Input Hysteresis	0.2 V _{CC}		V	
C _{IN}	Input Capacitance		7	pF	freq = 1 MHz

NOTE:

 All I_{OL} = 5 mA for 82C84A-5

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	82C84A		82C84A-5		Units	Test Conditions
		Min	Max	Min	Max		
t _{EHEL}	External Frequency HIGH Time	13		20		ns	90%–90% V _{IN}
t _{ELEH}	External Frequency LOW Time	13		20		ns	10%–10% V _{IN}
t _{ELEL}	EFI Period	36		66		ns	(Note 1)
	XTAL Frequency	2.4	25	6.0	15	MHz	
t _{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		35		ns	\overline{ASYNC} = HIGH
t _{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		35		ns	\overline{ASYNC} = LOW
t _{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		35		ns	
t _{CLR1X}	RDY1, RDY2 Hold to CLK	0		0		ns	
t _{AYVCL}	\overline{ASYNC} Setup to CLK	50		50		ns	
t _{CLAYX}	\overline{ASYNC} Hold to CLK	0		0		ns	
t _{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		15		ns	
t _{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		0		ns	
t _{YHEH}	CSYNC Setup to EFI	20		20		ns	
t _{EHYL}	CSYNC Hold to EFI	20		20		ns	
t _{YHYL}	CSYNC Width	2 • t _{ELEL}		2 • t _{ELEL}		ns	
t _{I1HCL}	\overline{RES} Setup to CLK	65		65		ns	(Note 2)
t _{CL11H}	\overline{RES} Hold to CLK	20		20		ns	(Note 2)
t _{LIH}	Input Rise Time	15		20		ns	(Note 1)
t _{LIH}	Input Fall Time	15		20		ns	(Note 1)

A.C. CHARACTERISTICS (Continued)

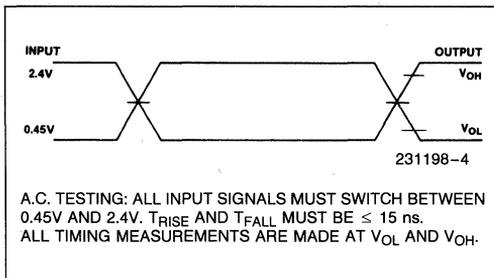
TIMING RESPONSES

Symbol	Parameter	Min 82C84A	Min 82C84A-5	Max	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125	200		ns	
t_{CHCL}	CLK HIGH Time	$(\frac{1}{3} t_{CLCL}) + 2$	69		ns	
t_{CLCH}	CLK LOW Time	$(\frac{2}{3} t_{CLCL}) - 15$	119		ns	
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time			10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL} - 20$	180		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL} - 20$	180		ns	
t_{RYLCL}	Ready Inactive to CLK (See Note 4)	-8	-8		ns	
t_{RYHCH}	Ready Active to CLK (See Note 3)	$(\frac{2}{3} t_{CLCL}) - 15$	119		ns	
t_{CLIL}	CLK to Reset Delay			40	ns	
t_{CLPH}	CLK to PCLK HIGH DELAY			22	ns	
t_{CLPL}	CLK to PCLK LOW Delay			22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	-5	-5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	2	35	ns	
t_{OLOH}	Output Rise Time (except CLK)			15	ns	From 0.8V to 2.0V
t_{OHOL}	Output Fall Time (except CLK)			15	ns	From 2.0V to 0.8V

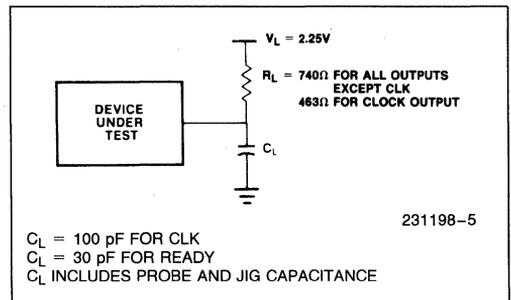
NOTES:

1. Transition between $V_{IL}(\max) - 0.4V$ and $V_{IH}(\min) + 0.4V$.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 and TW states.
4. Applies only to T2 states.

A.C. TESTING INPUT, OUTPUT WAVEFORM

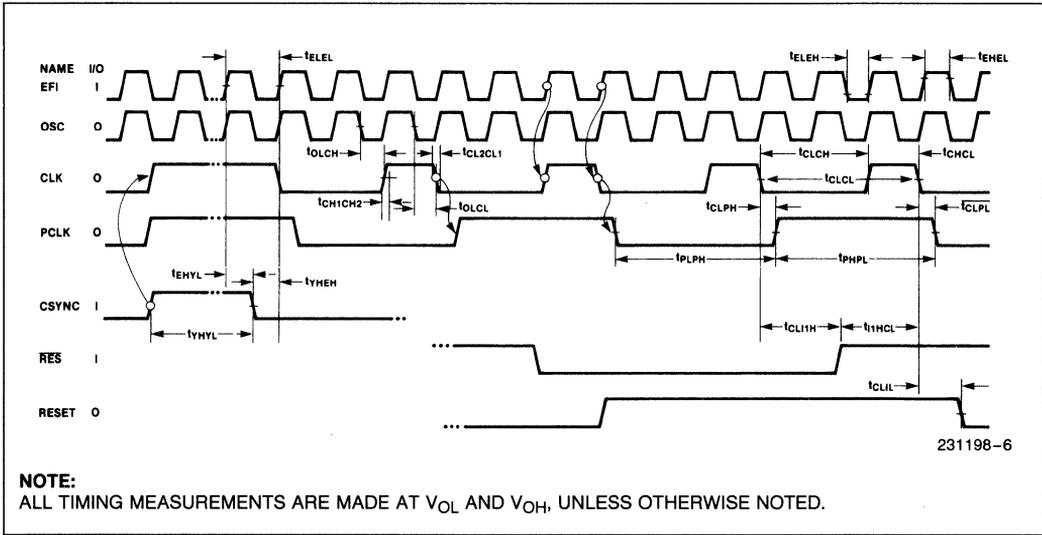


A.C. TESTING LOAD CIRCUIT

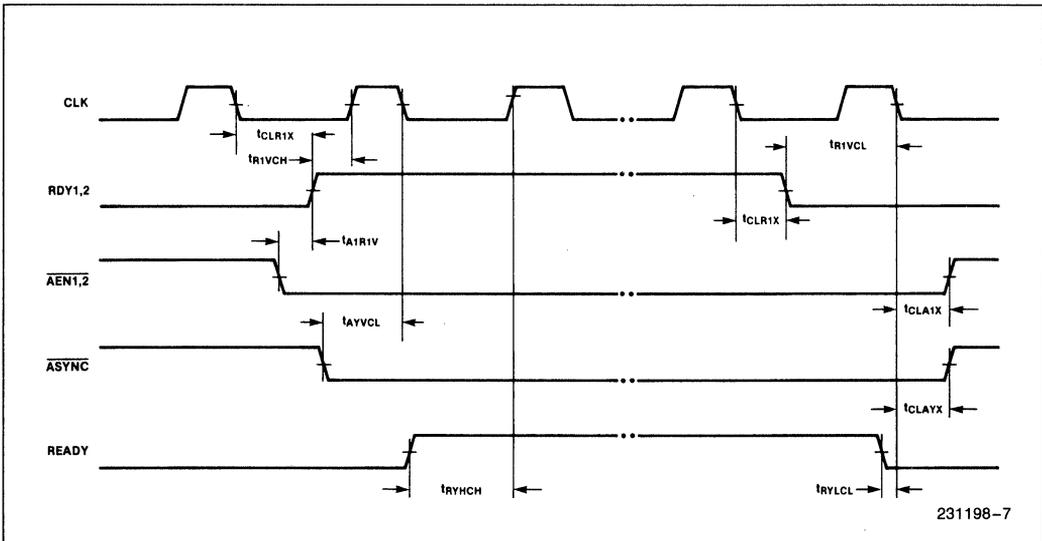


WAVEFORMS

CLOCKS AND RESET SIGNALS

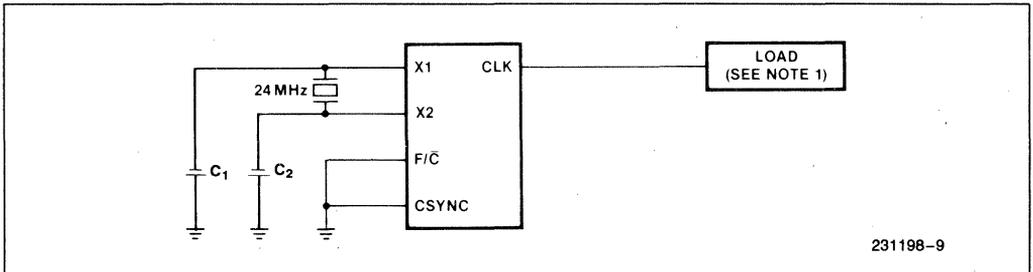
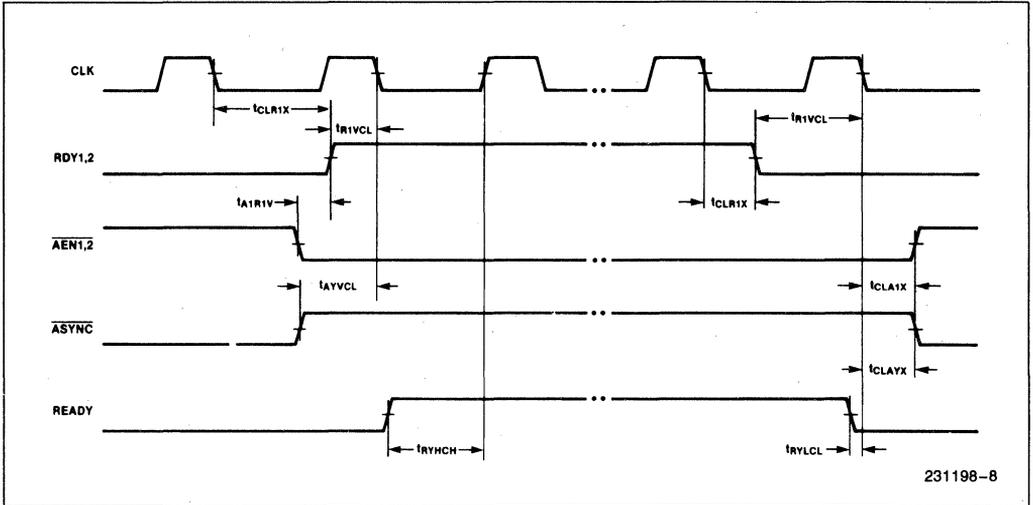


READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

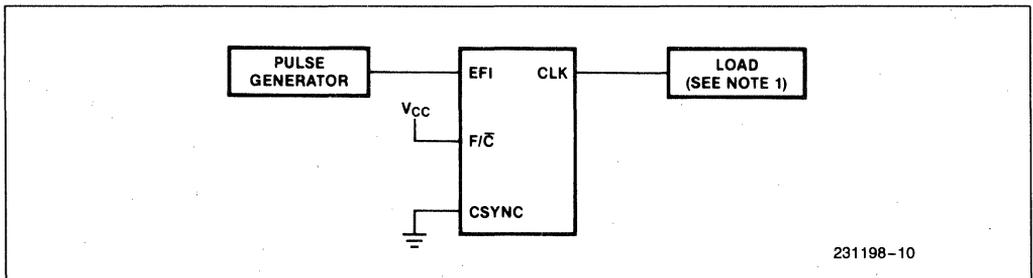


WAVEFORMS (Continued)

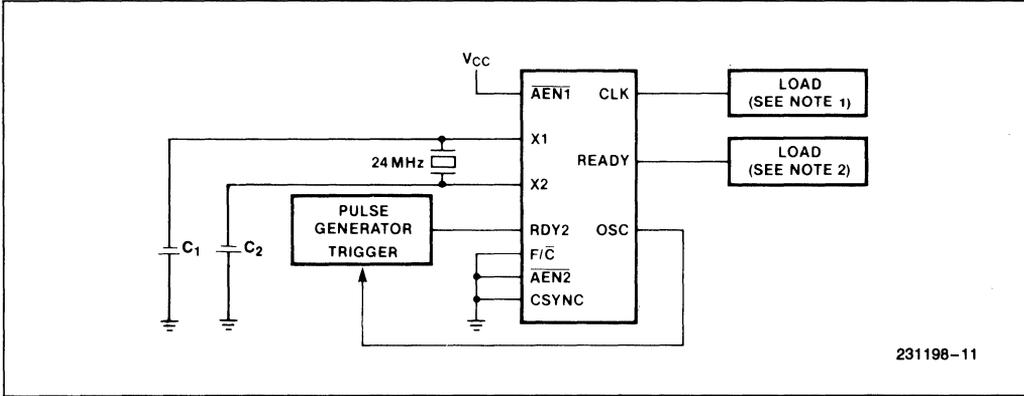
READY SIGNALS (FOR SYNCHRONOUS DEVICES)



Clock High and Low Time (Using X1, X2)

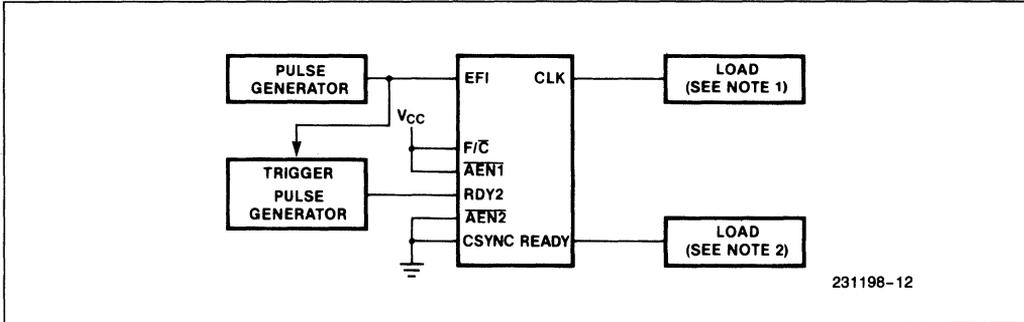


Clock High and Low Time (Using EFI)



231198-11

Ready to Clock (Using X1, X2)



231198-12

Ready to Clock (Using EFI)

- NOTES:**
 1. $C_L = 100 \text{ pF}$
 2. $C_L = 30 \text{ pF}$

82C88 CHMOS BUS CONTROLLER FOR 80C86, 80C88 PROCESSORS

- Pin Compatible with Bipolar 8288
- Low Power Operation
 - $I_{CCS} = 10 \mu A$
 - $I_{CC} = 1 mA/MHz$
- Provides Advanced Commands for Multi-Master Busses
- 3-State Command Output Drivers
- High Drive Capability
- Configurable for Use with an I/O Bus
- Single 5V Power Supply

The Intel 82C88 is a high performance CHMOS version of the 8288 bipolar bus controller. The 82C88 provides command and control timing generation for 80C86/88, 8086/88 and iAPX 186 systems. Static CHMOS circuit design insures low operating power. 8 MHz speed optimizes system performance and the 82C88 high output drive capability eliminates the need for additional bus drivers.

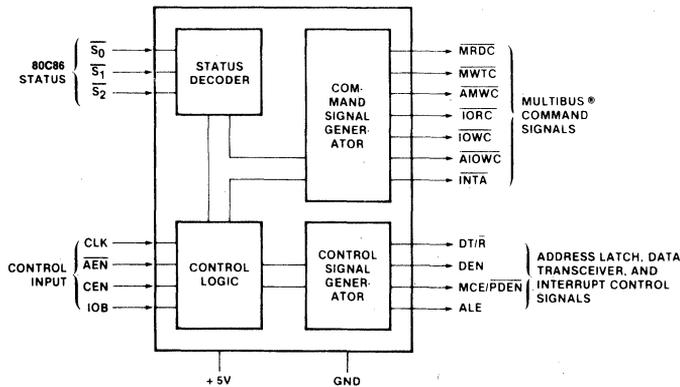
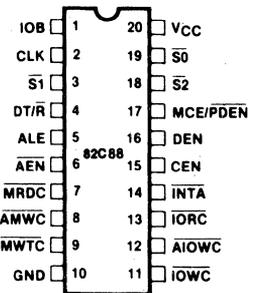


Figure 1. Block Diagram

231199-1



231199-2

Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
V _{CC}		POWER: +5V supply.
GND		GROUND.
$\overline{S_0}, \overline{S_1}, \overline{S_2}$	I	STATUS INPUT PINS: These pins are the status input pins from the 80C86, 80C88 or 80889 processors. The 82C88 decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Command and Control Logic.) Active "Bus Hold" circuits hold these lines HIGH when no other driving source is present.
CLK	I	CLOCK: This is a clock signal from the 82C84 clock generator and serves to establish when command and control signals are generated.
ALE	O	ADDRESS LATCH ENABLE: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
DEN	O	DATA ENABLE: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/ \overline{R}	O	DATA TRANSMIT/RECEIVE: This signal establishes the direction of data flow through the transceivers. A HIGH on this lines indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
\overline{AEN}	I	ADDRESS ENABLE: \overline{AEN} enables command outputs of the 82C88 Bus Controller at least 100 ns after it becomes active (LOW). \overline{AEN} going inactive immediately 3-states the command output drivers. \overline{AEN} does not affect the I/O command lines if the 82C88 is in the I/O Bus mode (IOB tied HIGH).
CEN	I	COMMAND ENABLE: When this signal is LOW all 82C88 command outputs and the DEN and \overline{PDEN} control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	I	INPUT/OUTPUT BUS MODE: When the IOB is strapped HIGH the 82C88 functions in the I/O Bus mode. When it is strapped LOW, the 82C88 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes).
\overline{AIOWC}	O	ADVANCED I/O WRITE COMMAND: The \overline{AIOWC} issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. \overline{AIOWC} is active LOW.
\overline{IOWC}	O	I/O WRITE COMMAND: This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.
\overline{IORC}	O	I/O READ COMMAND: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
\overline{AMWC}	O	ADVANCED MEMORY WRITE COMMAND: The \overline{AMWC} issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as read command signal. \overline{AMWC} is active LOW.
\overline{MWTC}	O	MEMORY WRITE COMMAND: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
\overline{MRDC}	O	MEMORY READ COMMAND: This command line instructs the memory to drive its data onto the data bus. This signal is active LOW.
\overline{INTA}	O	INTERRUPT ACKNOWLEDGE: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/ \overline{PDEN}	O	This is a dual function pin. MCE (IOB IS TIED LOW): Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. \overline{PDEN} (IOB IS TIED HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. \overline{PDEN} is active LOW.

FUNCTIONAL DESCRIPTION

Command and Control Logic

The command logic decodes the three 80C86, 80C88 or 8089 CPU status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued.

This chart shows the meaning of each status "word".

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State	82C88 Command
0	0	0	Interrupt Acknowledge	\overline{INTA}
0	0	1	Read I/O Port	\overline{IORC}
0	1	0	Write I/O Port	\overline{IOWC} , \overline{AIOWC}
0	1	1	Halt	None
1	0	0	Code Access	\overline{MRDC}
1	0	1	Read Memory	\overline{MRDC}
1	1	0	Write Memory	\overline{MWTC} , \overline{AMWC}
1	1	1	Passive	None

The command is issued in one of two ways dependent on the mode of the 82C88 Bus Controller.

I/O Bus Mode — The 82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines (\overline{IORC} , \overline{IOWC} , \overline{AIOWC} , \overline{INTA}) are always enabled (i.e., not dependent on \overline{AEN}). When an I/O command is initiated by the processor, the 82C88 immediately activates the command lines, using \overline{PDEN} and $\overline{DT/\overline{R}}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal (\overline{AEN} LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode — The 82C88 in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 115 ns after the \overline{AEN} Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the \overline{AEN} line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

COMMAND OUTPUTS

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command outputs are:

- \overline{MRDC} — Memory Read Command
- \overline{MWTC} — Memory Write Command
- \overline{IORC} — I/O Read Command
- \overline{IOWC} — I/O Write Command
- \overline{AMWC} — Advanced Memory Write Command
- \overline{AIOWC} — Advanced I/O Write Command
- \overline{INTA} — Interrupt Acknowledge

\overline{INTA} (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

CONTROL OUTPUTS

The control outputs of the 82C88 are Data Enable (DEN), Data Transmit/Receive ($\overline{DT/\overline{R}}$) and Master Cascade Enable/Peripheral Data Enable ($\overline{MCE/\overline{PDEN}}$). The DEN signal determines when the external bus should be enabled onto the local bus and the $\overline{DT/\overline{R}}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The $\overline{MCE/\overline{PDEN}}$ pin changes function with the two modes of the 82C88. When the 82C88 is in the IOB mode (IOB HIGH) the \overline{PDEN} signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

INTERRUPT ACKNOWLEDGE AND MCE

The MCE signal is used during an interrupt acknowledge cycle if the 82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second interrupt Ac-

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5V to 8.0V
Operating Supply Voltage	4.0V to 7.0V
All Input Voltages	-2.0V to V _{CC} + 0.5V
All Output Voltages	-0.5V to V _{CC} + 0.5V
Power Dissipation	1.0 Watt

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min	Max	Unit	Test Conditions
I _{CC}	Operating Supply Current		8	mA	V _{IN} = V _{CC} or GND V _{CC} = 5.5V Outputs Unloaded
I _{CCS}	Standby Supply Current		10	μA	V _{IN} = V _{CC} or GND V _{CC} = 5.5V Outputs Unloaded
V _{IH}	Input High Voltage	2.0		V	
V _{IL}	Input Low Voltage		0.8	V	
V _{CH}	V _{IH} for Clock	0.7 V _{CC}		V	
V _{CL}	V _{IL} for Clock		0.2 V _{CC}	V	
I _{LI}	Input Leakage Current		± 1.0	μA	0V ≤ V _{IN} ≤ V _{CC} (Note 1)
I _{BHH}	Input Leakage Current (Bus Hold High)	- 50	- 300	μA	V _{IN} = 2.0V (Notes 2, 3)
I _{BHHO}	Bus Hold High Overdrive	- 600		μA	(Notes 2, 4)
I _{LO}	Output Leakage Current		± 10	μA	0V ≤ V _{OUT} ≤ V _{CC}
V _{OL}	Output Low Voltage: Command Outputs Control Outputs		0.5 0.4	V	I _{OL} = 20 mA I _{OL} = 8 mA
V _{OH}	Output High Voltage: Command Outputs Control Outputs	3.0 V _{CC} - 0.4 3.0 V _{CC} - 0.4		V	I _{OH} = - 8 mA I _{OH} = - 2.5 mA I _{OH} = - 4 mA I _{OH} = - 2.5 mA
C _{IN}	Input Capacitance		5	pF	Freq. = 1 MHz Unmeasured pins at GND
C _{OUT}	Output Capacitance		15	pF	Freq. = 1 MHz Unmeasured pins at GND

NOTES:

1. Except $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$.
2. $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ only.
3. Raise inputs to V_{CC}, then lower to 2.0V.
4. An external driver must sink at least I_{BHHO} to toggle a status line from HIGH to LOW.

knowledge signal gates the interrupt vector onto the processor bus.

ADDRESS LATCH ENABLE AND HALT

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) into a latch for halt state decoding.

COMMAND ENABLE

The Command Enable (CEN) input acts as a command qualifier for the 82C88. If the CEN pin is high the 82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

A.C. CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$)*

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Units	Test Conditions
fc	CLK Frequency		8	MHz	
TCLCL	CLK Cycle Period	125		ns	
TCLCH	CLK Low Time	66		ns	
TCHCL	CLK High Time	40		ns	
TSVCH	Status Active Setup Time	35		ns	
TCHSV	Status Inactive Hold Time	10		ns	
TSHCL	Status Inactive Setup Time	35		ns	
TCLSH	Status Active Hold Time	10		ns	

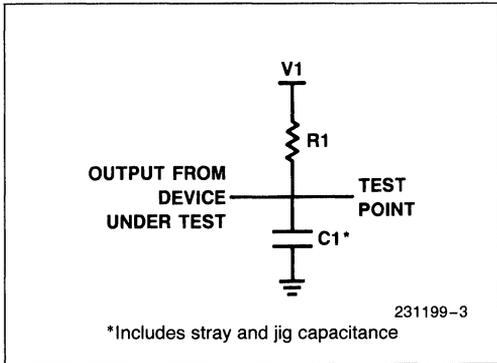
TIMING RESPONSES

Symbol	Parameter	Min	Max	Units	Test Conditions**
TCVNV	Control Active Delay	5	45	ns	a
TCVNX	Control Inactive Delay	10	45	ns	a
TCLLH	ALE Active Delay (from CLK)		20	ns	a
TCLMCH	MCE Active Delay (from CLK)		25	ns	a
TSVLH	ALE Active Delay (from Status)		20	ns	a
TSVMCH	MCE Active Delay (from Status)		30	ns	a
TCHLL	ALE Inactive Delay	4	18	ns	a
TMHNL	Command Inactive to DEN Low Delay	TCLCH-5		ns	Command: a, DEN: e
TCLML	Command Active Delay	5	35	ns	b
TCLMH	Command Inactive Delay	5	35	ns	b
TCHDTL	Direction Control Active Delay		50	ns	a
TCHDTH	Direction Control Inactive Delay		30	ns	a
TAELCH	Command Enable Time		40	ns	c(Note 1)
TAEHCZ	Command Disable Time		40	ns	d(Note 2)
TAELCV	Enable Delay Time	110	250	ns	b
TAEVNV	\overline{AEN} to DEN		25	ns	a
TCEVNV	CEN to DEN, \overline{PDEN}		25	ns	a
TCELRH	CEN to Command		TCLML + 10	ns	b
TLHLL	ALE High Time		TCLCL - 10	ns	a
TOLOH	Output, Rise Time		15	ns	From 0.8V to 2.0V
TOHOL	Output, Fall Time		15	ns	From 2.0V to 0.8V

NOTES:

1. TAELCH measurement is between 1.5V and 2.5V.
2. TAEHCZ measured at 0.5V change in V_{OUT} .

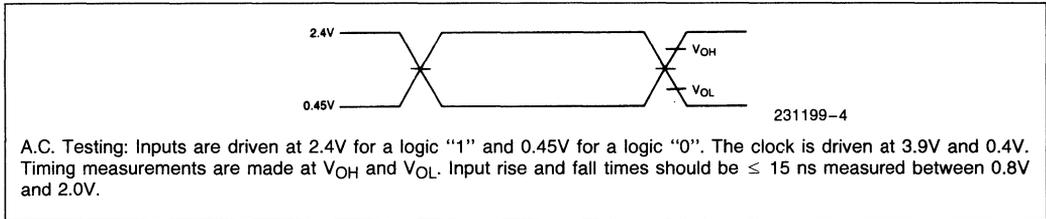
TEST LOAD CIRCUITS—3-STATE COMMAND OUTPUT TEST LOAD



****Test Condition Definition Table**

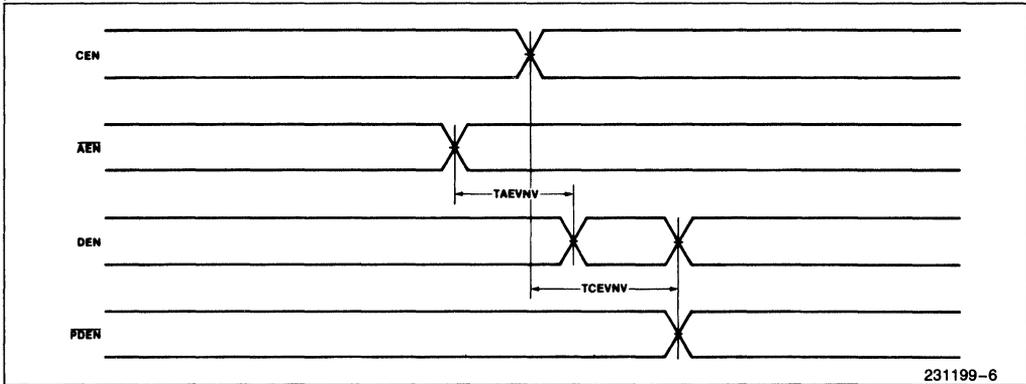
Test Condition	I_{OH}	I_{OL}	V1	R1	C1
a	-4.0 mA	+8.0 mA	2.13V	220Ω	80 pf
b	-8.0 mA	+20.0 mA	2.29V	91Ω	300 pf
c	-8.0 mA		1.5V	187Ω	300 pf
d	-8.0 mA		1.5V	187Ω	50 pf
e	-4.0 mA		2.28V	114Ω	5 pf

A.C. TESTING INPUT, OUTPUT WAVEFORM

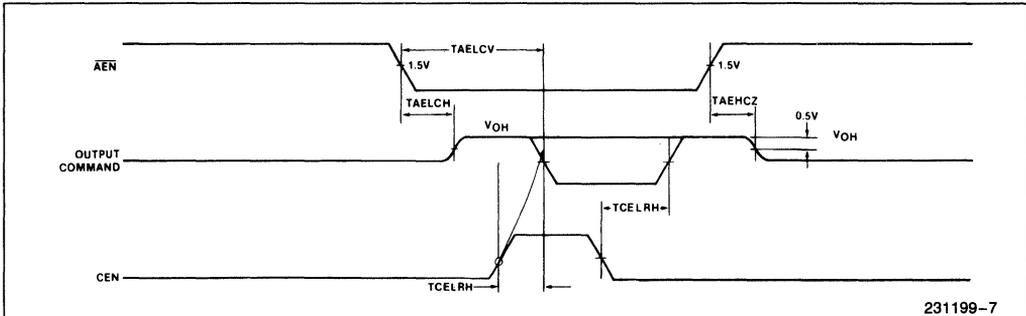


WAVEFORMS (Continued)

DEN, PDEN QUALIFICATION TIMING



ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)



NOTE:

CEN must be low or valid prior to T2 to prevent the command from being generated.

82C08 CHMOS DYNAMIC RAM CONTROLLER

- 0 Wait State, 8 MHz iAPX 286, iAPX 186/188, and iAPX 86/88
- Provides all Signals necessary to Control 64K (51C64) and 256K (51C256) Dynamic RAMs
- Pin-Compatible with 8208
- Automatic RAM Warm-up
- Directly Addresses and Drives up to 1 Megabyte without External Drivers
- Power Down Mode with Programmable Memory Refresh
- Microprocessor Data Transfer and Advance Acknowledge Signals
- Four Programmable Refresh Modes

The Intel 82C08 Dynamic RAM Controller is a CMOS, high performance, systems oriented, Dynamic RAM controller that is designed to easily interface 64K and 256K Dynamic RAMs to Intel and other microprocessors. The 82C08 also has a power down mode where only the refresh logic is activated.

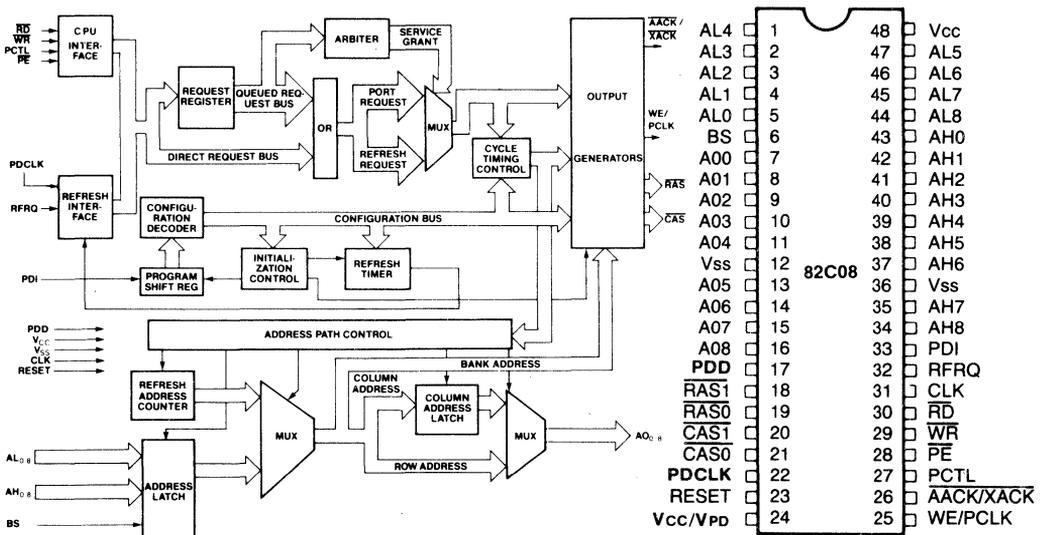


Figure 1. Block Diagram and Pinout Diagram

Intel Corporation Assumes No Responsibility for the Use of Any Circuitry Other Than Circuitry Embodied in an Intel Product. No Other Circuit Patent Licenses are Implied. Information Contained Herein Supersedes Previously Published Specifications On These Devices From Intel.

Table 1. Pin Description

Symbol	Pin	Type	Name and Function
AL0 AL1 AL2 AL3 AL4 AL5 AL6 AL7 AL8	5 4 3 2 1 47 46 45 44	 	ADDRESS LOW: These lower order address inputs are used to generate the row address for the internal address multiplexer. In iAPX 286 mode (CFS = 1), these addresses are latched internally.
AH0 AH1 AH2 AH3 AH4 AH5 AH6 AH7 AH8	43 42 41 40 39 38 37 35 34	 	ADDRESS HIGH: These higher order address inputs are used to generate the column address for the internal address multiplexer. In iAPX 286 mode, these addresses are latched internally.
BS	6		BANK SELECT: This input is used to select one of the two banks of the dynamic RAM array as defined by the program-bit RB.
AO0 AO1 AO2 AO3 AO4 AO5 AO6 AO7 AO8	7 8 9 10 11 13 14 15 16	○ ○ ○ ○ ○ ○ ○ ○ ○	ADDRESS OUTPUTS: These outputs are designed to provide the row and column addresses, of either the CPU or the refresh counter, to the dynamic RAM array. These outputs drive the dynamic RAM array directly and need no external drivers. However, they typically need series resistors to match impedances.
RAS0 RAS1	19 18	○ ○	ROW ADDRESS STROBE: These outputs are used by the dynamic RAM array to latch the row address, present on the A00-8 pins. These outputs are selected by the BS pin as programmed by program-bit RB. These outputs drive the dynamic RAM array directly and need no external drivers.
CAS0 CAS1	21 20	○ ○	COLUMN ADDRESS STROBE: These outputs are used by the dynamic RAM array to latch the column address, present on the A00-8 pins. These outputs are selected by the BS pin as programmed by program-bit RB. These outputs drive the dynamic RAM array directly and need no external drivers.
RESET	23		RESET: This active high signal causes all internal counters to be reset. Upon release of RESET, data appearing at the PDI pin is clocked-in by the PCLK output. The states of the PDI, PCTL and RFRQ pins are sampled by RESET going inactive and are used to program the 82C08. An 8-cycle dynamic RAM warm-up is performed after clocking PDI bits into the 82C08. Activation of RESET will terminate the power down mode.
WE/ PCLK	25	○	WRITE ENABLE/PROGRAMMING CLOCK: Immediately after a RESET this pin becomes PCLK and is used to clock serial programming data into the PDI pin. After the 82C08 is programmed this active high signal provides the dynamic RAM array the write enable input for a write operation.
AACK/ XACK	26	○	ADVANCE ACKNOWLEDGE/TRANSFER ACKNOWLEDGE: When the X programming bit is set to logic 0 this pin is AACK and indicates that the processor may continue processing and that data will be available when required. This signal is optimized for the system by programming the S program-bit for synchronous or asynchronous operation. The S programming bit determines whether this strobe will be early or late. If another dynamic RAM cycle is in progress at the time of the new request, the AACK is delayed. When the X programming bit is set to logic 1 this pin is XACK and indicates that data on the bus is valid during a read cycle or that data may be removed from the bus during a write cycle. XACK is a MULTIBUS compatible signal.

Table 1. Pin Description (continued)

Symbol	Pin	Type	Name and Function
PCTL	27	I	PORT CONTROL: This pin is sampled on the falling edge of RESET. It configures the 8208 to accept command inputs or processor status inputs. If PCTL is low after RESET the 8208 is programmed to accept bus/multibus command inputs or iAPX 286 status inputs. If PCTL is high after RESET the 8208 is programmed to accept status inputs from iAPX 86 or iAPX 186 type processors. The S2 status line should be connected to this input if programmed to accept iAPX 86 or iAPX 186 status inputs. When programmed to accept bus commands or iAPX 286 status inputs, it should be tied low or it may be connected to INHIBIT when operating with MULTIBUS.
$\overline{\text{PE}}$	28	I	PORT ENABLE: This pin serves to enable a RAM cycle request. It is generally decoded from the address bus.
$\overline{\text{WR}}$	29	I	WRITE: This pin is the write memory request command input. This input also directly accepts the S0 status line from Intel processors.
$\overline{\text{RD}}$	30	I	READ: This pin is the read memory request command input. This input also directly accepts the S1 status line from Intel processors.
CLK	31	I	CLOCK: This input provides the basic timing for sequencing the internal logic.
RFRQ	32	I	REFRESH REQUEST: This input is sampled on the falling edge of RESET. If RFRQ is high at RESET then the 82C08 is programmed for internal-refresh request or external-refresh request with failsafe protection. If RFRQ is low at RESET then the 82C08 is programmed for external-refresh without failsafe protection or burst-refresh. Once programmed the RFRQ pin accepts signals to start an external-refresh with failsafe protection or external-refresh without failsafe protection or a burst-refresh.
PDI	33	I	PROGRAM DATA INPUT: This input is sampled by RESET going low. It programs the various user selectable options in the 82C08. The PCLK pin shifts programming data into the PDI input from an external shift register. This pin may be strapped low to a default iAPX 186 mode configuration or high to a default iAPX 286 mode configuration.
*PDD	17	I	POWER DOWN DETECT: This input is sampled before every memory cycle to inform the 82C08 of system detection of power failure. When active, the 82C08 remains in power down mode and performs memory refresh only (RAS-only refresh). In power down mode the 82C08 uses PDCLK for timing and VPD for power.
*PDCLK	22	I	POWER DOWN CLOCK: This pin is used as a clock for internal refresh circuits during power down. The input can be asynchronous to pin 31. Extended refresh is achieved by slowing down this clock. This pin should be grounded if not used.
*V _{CC} /V _{PD}	24	I	POWER: During power down mode this is the only active power pin.
V _{CC}	48	I	POWER: +5V. Not active during power down.
V _{SS}	12	I	GROUND
	36	I	GROUND

*Different function than the HMOS 8208.

GENERAL DESCRIPTION: 8208 vs. 82C08

The Intel 82C08 Dynamic RAM Controller is a micro-computer peripheral device which provides the necessary signals to address, refresh and directly drive 64K and 256K dynamic RAMs.

The 8208 supports several microprocessor interface options including synchronous and asynchronous operations for iAPX 86, iAPX 186, iAPX 286 and MULTIBUS. The 82C08 will also interface to non-Intel microprocessors.

The 82C08 is a CHMOS version of the 8208 and is pin compatible with it. Three pins—17, 22, and 24—of the 82C08 are different from the 8208. They provide a power down mode that allows the system to run at much lower ICC. A separate refresh clock,

pin 22, allows the designer to take advantage of RAMs like Intel's 51C64L and 51C256L that permit extended memory refresh.

The 82C08 also has some timing changes versus the 8208. In order to eliminate the external bus latches, both WE and CAS timings are shortened. These timing changes are backwards-compatible for 8208 designs.

FUNCTIONAL DESCRIPTION

Processor Interface

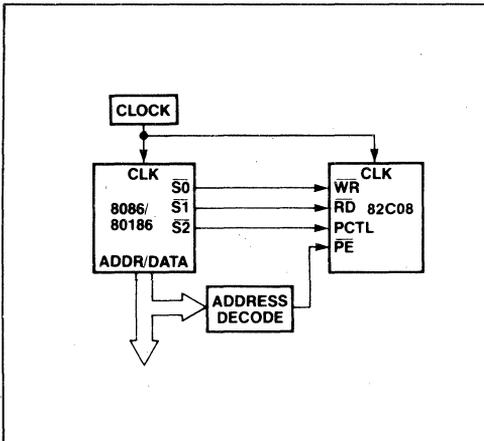
The 82C08 has control circuitry capable of supporting one of several possible bus structures. The 82C08 may be programmed to run synchronous or

asynchronous to the processor clock. The 82C08 has been optimized to run synchronously with Intel's iAPX 86, iAPX 88, iAPX 186/188 and iAPX 286. When the 82C08 is programmed to run in asynchronous mode, the 82C08 inserts the necessary synchronization circuitry for the RD, WR, PE, and PCTL inputs.

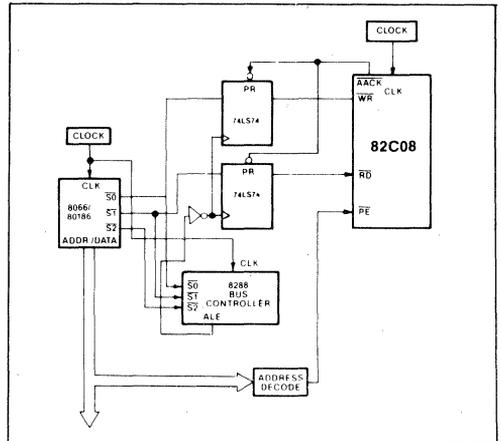
The 82C08 achieves high performance (i.e. no wait states) by decoding the status lines directly from the processor. The 82C08 can also be programmed to receive read or write MULTIBUS commands or commands from a bus controller.

The 82C08 may be programmed to accept the clock of the processor. The 82C08 adjusts its internal timing to allow for different clock frequencies of these microprocessors. (See Microprocessor Clock Frequency Option.)

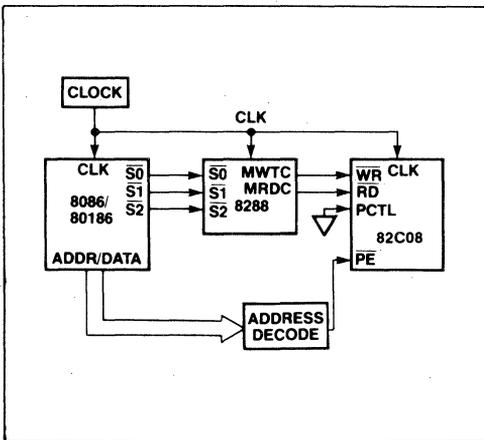
Figure 2 shows the different processor interfaces to the 82C08 using the synchronous or asynchronous mode and status or command interface. Figure 3 shows detailed interfaces to the iAPX 186 and iAPX 286 processors.



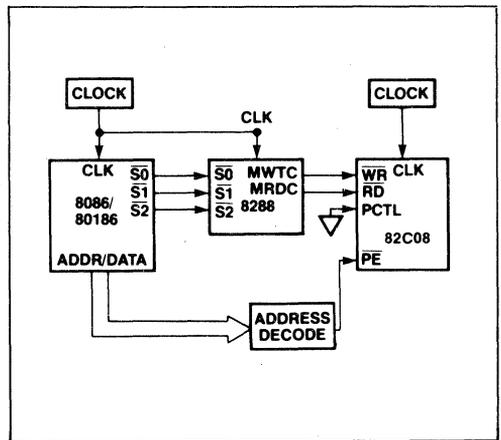
Slow-Cycle Synchronous-Status Interface



Slow-Cycle Asynchronous-Status Interface



Slow-Cycle Synchronous-Command Interface



Slow-Cycle Asynchronous-Command Interface

Figure 2A. Slow-cycle (CFS=0) Port Interfaces Supported by the 82C08

82C54 CHMOS PROGRAMMABLE INTERVAL TIMER

- **Compatible with all Intel and most other microprocessors**
- **High Speed, "Zero Wait State"**
Operation with 8 MHz 8086/88 and 80186/188
- **Three independent 16-bit counters**
- **Handles Inputs from DC to 8 MHz**
— 10 MHz for 82C54-2
- **Low Power CHMOS**
— $I_{CC} = 10 \text{ mA @ 8 MHz Count frequency}$
- **Completely TTL Compatible**
- **Six Programmable Counter Modes**
- **Binary or BCD counting**
- **Status Read Back Command**

The Intel 82C54 is a high-performance, CHMOS version of the industry standard 8254 counter/timer which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 82C54 is pin compatible with the HMOS 8254, and is a superset of the 8253.

Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications.

The 82C54 is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent HMOS product. The 82C54 is available in 24-pin DIP and 28-pin plastic leaded chip carrier (PLCC) packages.

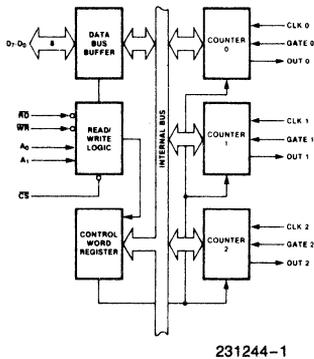
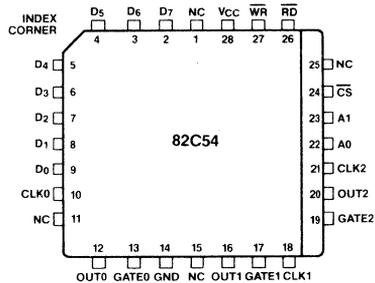
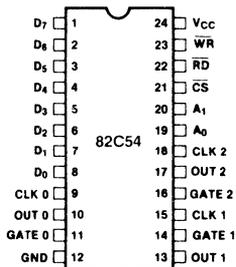


Figure 1. 82C54 Block Diagram



PLASTIC LEADED CHIP CARRIER



231244-2

Diagrams are for pin reference only.
Package sizes are not to scale.

Figure 2. 82C54 Pinout

Table 1. Pin Description

Symbol	Pin Number		Type	Function															
	DIP	PLCC																	
D ₇ -D ₀	1-8	2-9	I/O	Data: Bidirectional tri-state data bus lines, connected to system data bus.															
CLK 0	9	10	I	Clock 0: Clock input of Counter 0.															
OUT 0	10	12	O	Output 0: Output of Counter 0.															
GATE 0	11	13	I	Gate 0: Gate input of Counter 0.															
GND	12	14		Ground: Power supply connection.															
OUT 1	13	16	O	Out 1: Output of Counter 1.															
GATE 1	14	17	I	Gate 1: Gate input of Counter 1.															
CLK 1	15	18	I	Clock 1: Clock input of Counter 1.															
GATE 2	16	19	I	Gate 2: Gate input of Counter 2.															
OUT 2	17	20	O	Out 2: Output of Counter 2.															
CLK 2	18	21	I	Clock 2: Clock input of Counter 2.															
A ₁ , A ₀	20-19	23-22	I	Address: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.															
				<table border="1"> <thead> <tr> <th>A₁</th> <th>A₀</th> <th>Selects</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Counter 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>Counter 1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Counter 2</td> </tr> <tr> <td>1</td> <td>1</td> <td>Control Word Register</td> </tr> </tbody> </table>	A ₁	A ₀	Selects	0	0	Counter 0	0	1	Counter 1	1	0	Counter 2	1	1	Control Word Register
A ₁	A ₀	Selects																	
0	0	Counter 0																	
0	1	Counter 1																	
1	0	Counter 2																	
1	1	Control Word Register																	
\overline{CS}	21	24	I	Chip Select: A low on this input enables the 82C54 to respond to \overline{RD} and \overline{WR} signals. \overline{RD} and \overline{WR} are ignored otherwise.															
\overline{RD}	22	26	I	Read Control: This input is low during CPU read operations.															
\overline{WR}	23	27	I	Write Control: This input is low during CPU write operations.															
V _{CC}	24	28		Power: +5V power supply connection.															
NC		1, 11, 15, 25		No Connect															

FUNCTIONAL DESCRIPTION

General

The 82C54 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the de-

sired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Even counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 3).

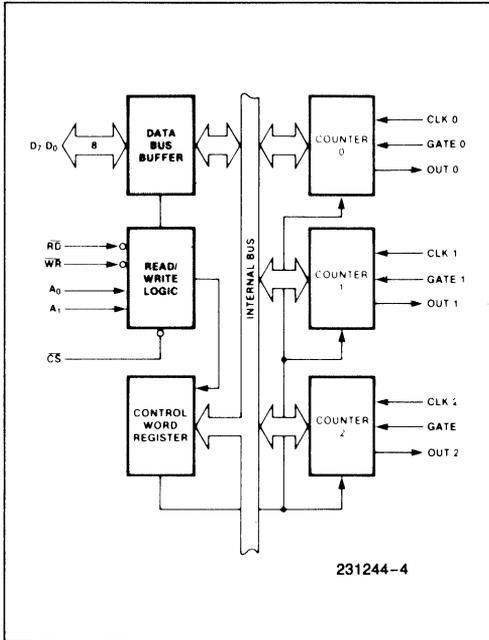


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

READ/WRITE LOGIC

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A₁ and A₀ select one of the three counters or the Control Word Register to be read from/written into. A "low" on the RD input tells the 82C54 that the CPU is reading one of the counters. A "low" on the WR input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both RD and WR are qualified by CS; RD and WR are ignored unless the 82C54 has been selected by holding CS low.

CONTROL WORD REGISTER

The Control Word Register (see Figure 4) is selected by the Read/Write Logic when A₁, A₀ = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

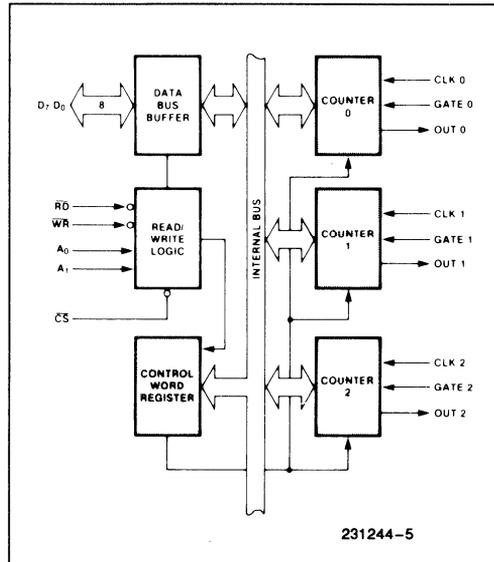


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

COUNTER 0, COUNTER 1, COUNTER 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

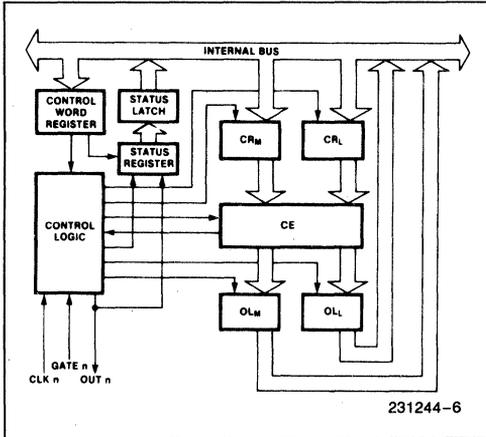


Figure 5. Internal Block Diagram of a Counter

The status register, shown in the Figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presetable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is

stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK_n, GATE_n, and OUT_n are all connected to the outside world through the Control Logic.

82C54 SYSTEM INTERFACE

The 82C54 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A₀, A₁ connect to the A₀, A₁ address bus signals of the CPU. The CS̄ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

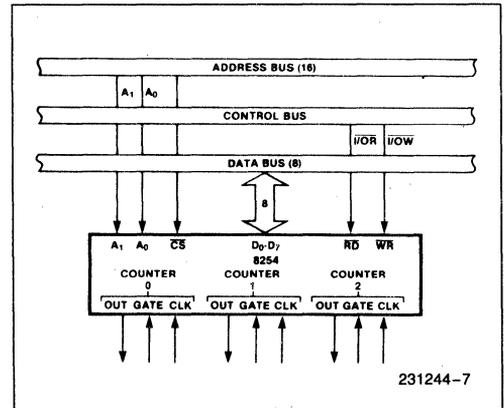


Figure 6. 82C54 System Interface

OPERATIONAL DESCRIPTION

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count. The control word format is shown in Figure 7.

All Control Words are written into the Control Word Register, which is selected when $A_1, A_0 = 11$. The Control Word itself specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Control Word Format

$A_1, A_0 = 11 \quad \overline{CS} = 0 \quad \overline{RD} = 1 \quad \overline{WR} = 0$

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 7. Control Word Format

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

- 1) For each Counter, the Control Word must be written before the initial count is written.
- 2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A₁, A₀ inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special in-

struction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

		A₁	A₀			A₁	A₀
Control Word —	Counter 0	1	1	Control Word —	Counter 2	1	1
LSB of count —	Counter 0	0	0	Control Word —	Counter 1	1	1
MSB of count —	Counter 0	0	0	Control Word —	Counter 0	1	1
Control Word —	Counter 1	1	1	LSB of count —	Counter 2	1	0
LSB of count —	Counter 1	0	1	MSB of count —	Counter 2	1	0
MSB of count —	Counter 1	0	1	LSB of count —	Counter 1	0	1
Control Word —	Counter 2	1	1	MSB of count —	Counter 1	0	1
LSB of count —	Counter 2	1	0	LSB of count —	Counter 0	0	0
MSB of count —	Counter 2	1	0	MSB of count —	Counter 0	0	0
		A₁	A₀			A₁	A₀
Control Word —	Counter 0	1	1	Control Word —	Counter 1	1	1
Counter Word —	Counter 1	1	1	Control Word —	Counter 0	1	1
Control Word —	Counter 2	1	1	LSB of count —	Counter 1	0	1
LSB of count —	Counter 2	1	0	Control Word —	Counter 2	1	1
LSB of count —	Counter 1	0	1	LSB of count —	Counter 0	0	0
LSB of count —	Counter 0	0	0	MSB of count —	Counter 1	0	1
MSB of count —	Counter 0	0	0	LSB of count —	Counter 2	1	0
MSB of count —	Counter 1	0	1	MSB of count —	Counter 0	0	0
MSB of count —	Counter 2	1	0	MSB of count —	Counter 2	1	0

NOTE:
In all four examples, all counters are programmed to read/write two-byte counts. These are only four of many possible programming sequences.

Figure 8. A Few Possible Programming Sequences

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the counters: a simple read operation, the Counter

Latch Command, and the Read-Back Command. Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A₁, A₀ inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

COUNTER LATCH COMMAND

The second method uses the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when $A_1, A_0 = 11$. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

$A_1, A_0 = 11; \overline{CS} = 0; \overline{RD} = 1; \overline{WR} = 0$

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4 - 00 designates Counter Latch Command

X - don't care

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 9. Counter Latching Command Format

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or pro-

gramming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies; A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

READ-BACK COMMAND

The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 10. The command applies to the counters selected by setting their corresponding bits D3,D2,D1 = 1.

$A_0, A_1 = 11 \quad \overline{CS} = 0 \quad \overline{RD} = 1 \quad \overline{WR} = 0$

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	COUNT	STATUS	CNT 2	CNT 1	CNT 0	0

D₅: 0 = Latch count of selected counter(s)
 D₄: 0 = Latch status of selected counter(s)
 D₃: 1 = Select counter 2
 D₂: 1 = Select counter 1
 D₁: 1 = Select counter 0
 D₀: Reserved for future expansion; must be 0

Figure 10. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5=0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the

count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4=0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 11. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

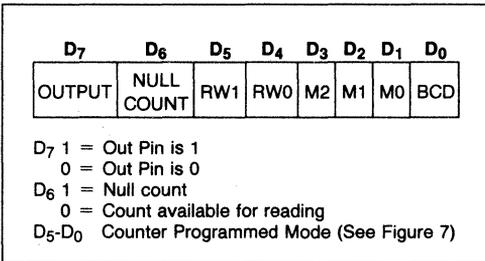


Figure 11. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 12.

THIS ACTION:	CAUSES:
A. Write to the control word register:[1] B. Write to the count register (CR);[2] C. New count is loaded into CE (CR → CE);	Null count = 1 • Null count = 1 Null count = 0
[1] Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected. [2] If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.	

Figure 12. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5,D4=0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 13.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

Command								Description	Results
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 13. Read-Back Command Example

CS	RD	WR	A ₁	A ₀	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER: a rising edge of a Counter's GATE input.

COUNTER LOADING: the transfer of a count from the CR to the CE (refer to the "Functional Description")

MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

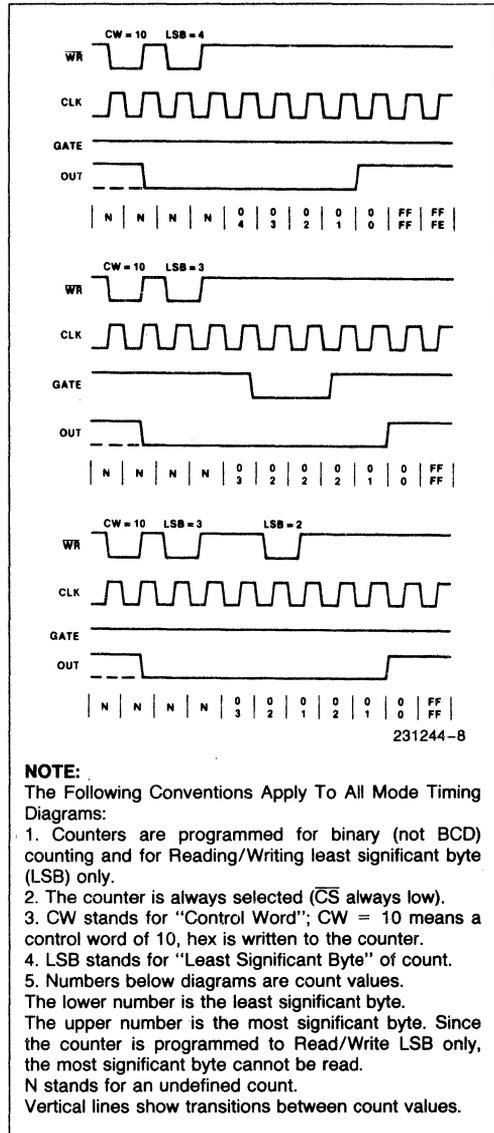
After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

- 1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
- 2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.



NOTE:

The Following Conventions Apply To All Mode Timing Diagrams:

1. Counters are programmed for binary (not BCD) counting and for Reading/Writing least significant byte (LSB) only.
2. The counter is always selected (\overline{CS} always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to Read/Write LSB only, the most significant byte cannot be read. N stands for an undefined count. Vertical lines show transitions between count values.

Figure 15. Mode 0

MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

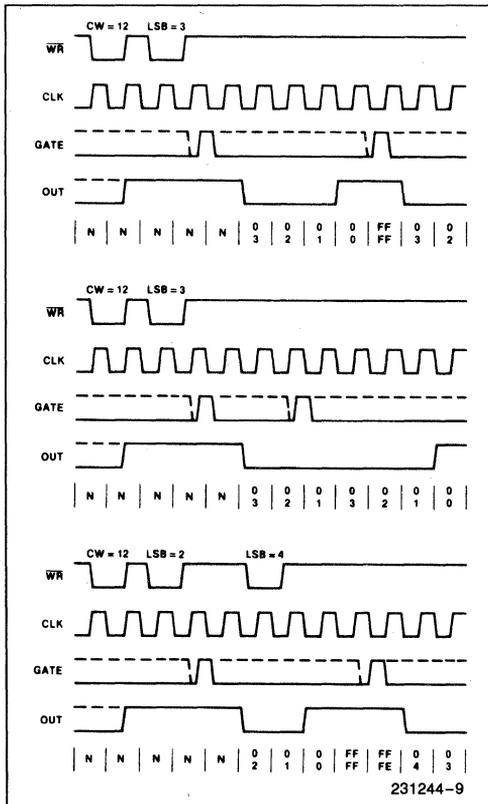


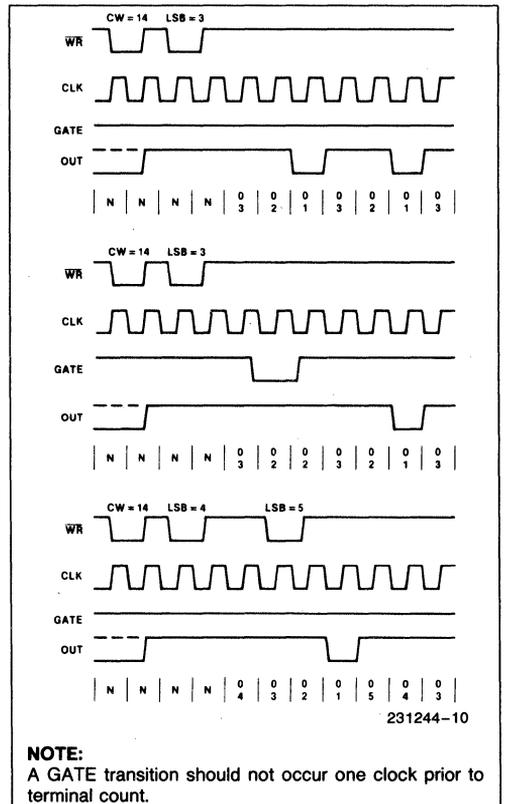
Figure 16. Mode 1

MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.



NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 17. Mode 2

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse *after* the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts,

OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

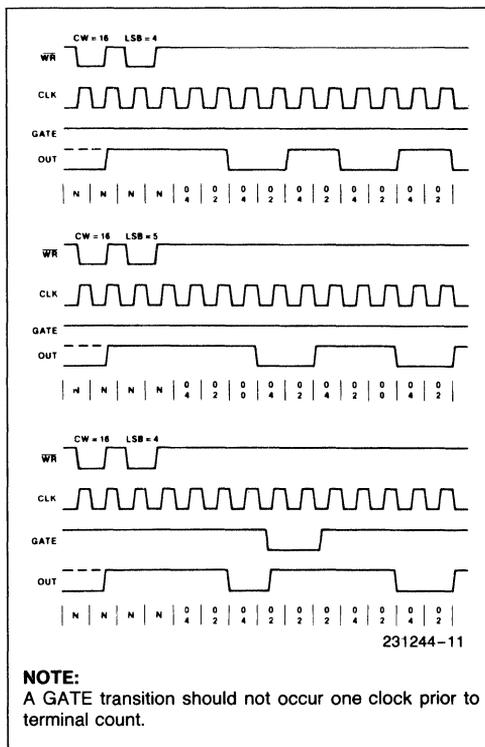


Figure 18. Mode 3

MODE 4: SOFTWARE TRIGGERED STROBE

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

- 1) Writing the first byte has no effect on counting.
- 2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

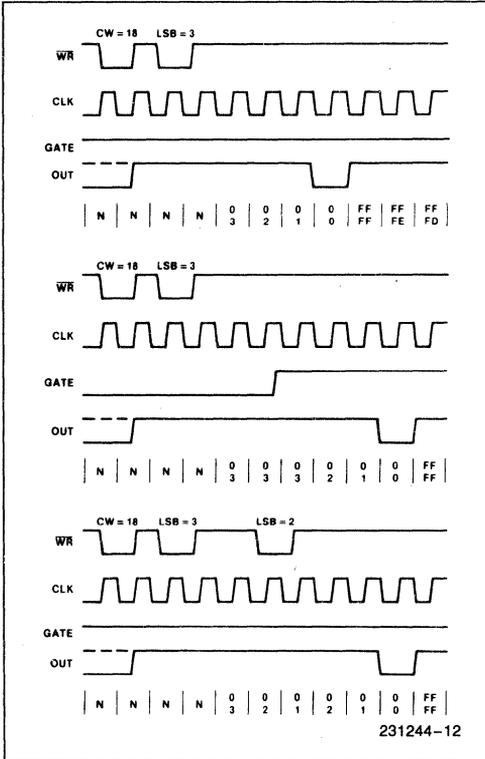


Figure 19. Mode 4

MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

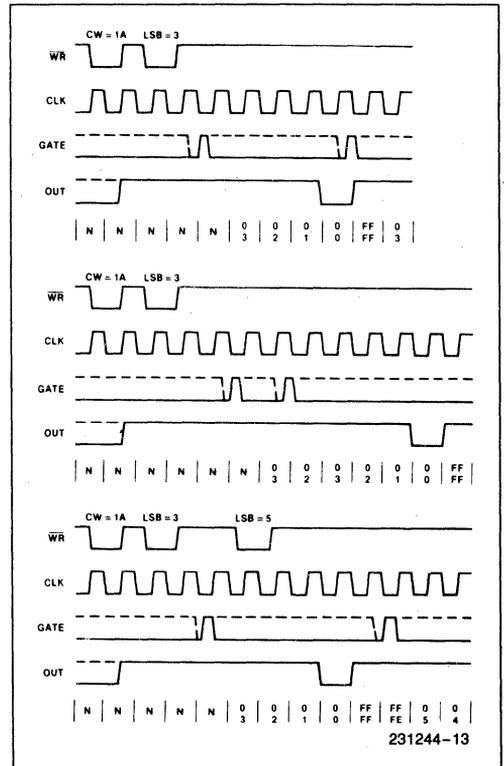


Figure 20. Mode 5

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 21. Gate Pin Operations Summary

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

NOTE:
0 is equivalent to 2¹⁶ for binary counting and 10⁴ for BCD counting

Figure 22. Minimum and Maximun initial Counts

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs—a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following \overline{WR} of a new count value.

COUNTER

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2¹⁶ for binary counting and 10⁴ for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter “wraps around” to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to 70°C
 Storage Temperature -65° to +150°C
 Supply Voltage -0.5 to +8.0V
 Operating Voltage +4V to +7V
 Voltage on any Input GND -2V to +6.5V
 Voltage on any Output GND -0.5V to V_{CC} + 0.5V
 Power Dissipation 1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	Min	Max	Units	Test Conditions
V _{IL}	Input Low Voltage	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.5V	V	
V _{OL}	Output Low Voltage		0.45	V	I _{OL} = 2.0 mA
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -400 μA
I _{IL}	Input Load Current		±10	μA	V _{IN} = V _{CC} to 0V
I _{OFL}	Output Float Leakage Current		±10	μA	V _{OUT} = V _{CC} to 0.45V
I _{CC}	V _{CC} Supply Current		10	mA	Clk Freq = 8MHz 82C54 10MHz 82C54-2
I _{CCSB}	V _{CC} Supply Current-Standby		10	μA	CLK Freq = DC

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min	Max	Units	Test Conditions
C _{IN}	Input Capacitance		10	pF	f _c = 1 MHz Unmeasured pins returned to GND
C _{I/O}	I/O Capacitance		20	pF	
C _{OUT}	Output Capacitance		20	pF	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V)

BUS PARAMETERS (Note 1)

READ CYCLE

Symbol	Parameter	82C54		82C54-2		Units
		Min	Max	Min	Max	
t _{AR}	Address Stable Before $\overline{RD} \downarrow$	45		30		ns
t _{SR}	\overline{CS} Stable Before $\overline{RD} \downarrow$	0		0		ns
t _{RA}	Address Hold Time After $\overline{RD} \downarrow$	0		0		ns
t _{RR}	\overline{RD} Pulse Width	150		95		ns
t _{RD}	Data Delay from $\overline{RD} \downarrow$		120		85	ns
t _{AD}	Data Delay from Address		220		185	ns
t _{DF}	$\overline{RD} \uparrow$ to Data Floating	5	90	5	65	ns
t _{RV}	Command Recovery Time	200		165		ns

NOTE:

1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V.

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	82C54		82C54-2		Units
		Min	Max	Min	Max	
t _{AW}	Address Stable Before \overline{WR} ↓	0		0		ns
t _{SW}	\overline{CS} Stable Before \overline{WR} ↓	0		0		ns
t _{WA}	Address Hold Time After \overline{WR} ↑	0		0		ns
t _{WW}	\overline{WR} Pulse Width	150		95		ns
t _{DW}	Data Setup Time Before \overline{WR} ↑	120		95		ns
t _{WD}	Data Hold Time After \overline{WR} ↑	0		0		ns
t _{RV}	Command Recovery Time	200		165		ns

CLOCK AND GATE

Symbol	Parameter	82C54		82C54-2		Units
		Min	Max	Min	Max	
t _{CLK}	Clock Period	125	DC	100	DC	ns
t _{PWH}	High Pulse Width	60 ^[3]		30 ^[3]		ns
t _{PWL}	Low Pulse Width	60 ^[3]		50 ^[3]		ns
T _R	Clock Rise Time		25		25	ns
t _F	Clock Fall Time		25		25	ns
t _{GW}	Gate Width High	50		50		ns
t _{GL}	Gate Width Low	50		50		ns
t _{GS}	Gate Setup Time to CLK ↑	50		40		ns
t _{GH}	Gate Hold Time After CLK ↑	50 ^[2]		50 ^[2]		ns
T _{OD}	Output Delay from CLK ↓		150		100	ns
t _{ODG}	Output Delay from Gate ↓		120		100	ns
t _{WC}	CLK Delay for Loading	0	55	0	55	ns
t _{WG}	Gate Delay for Sampling	-5	50	-5	40	ns
t _{WO}	OUT Delay from Mode Write		260		240	ns
t _{CL}	CLK Set Up for Count Latch	-4	45	-40	40	ns

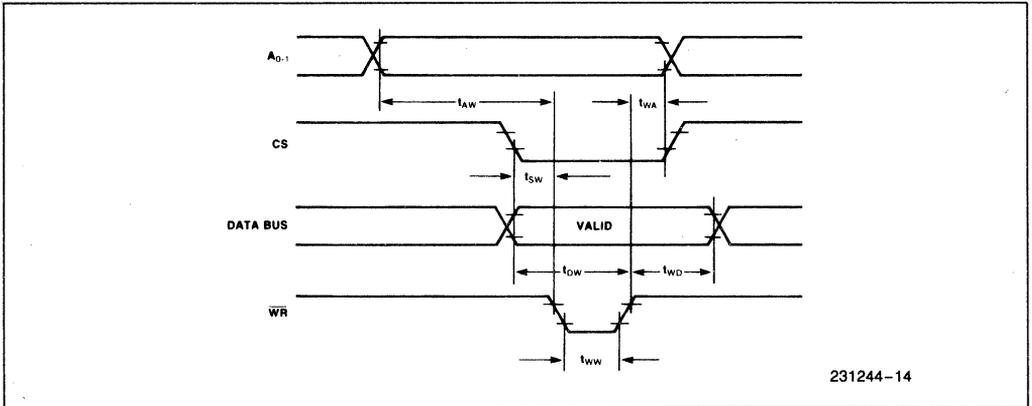
NOTES:

2. In Modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the 8254-2) of the rising clock edge may not be detected.

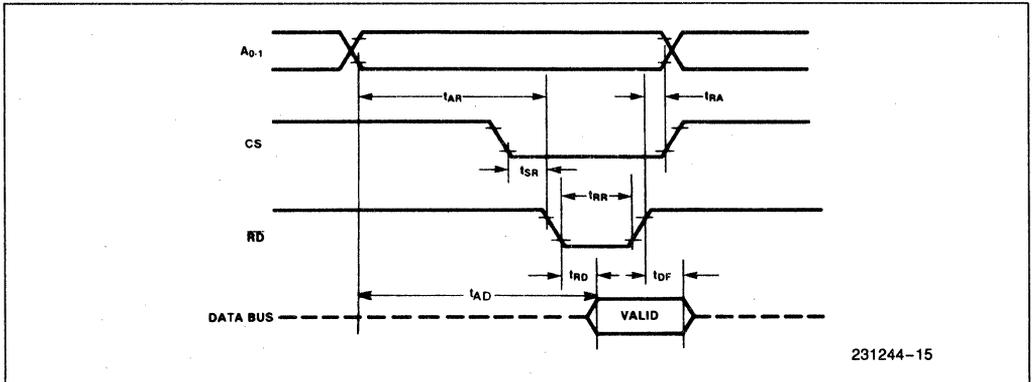
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

WAVEFORMS

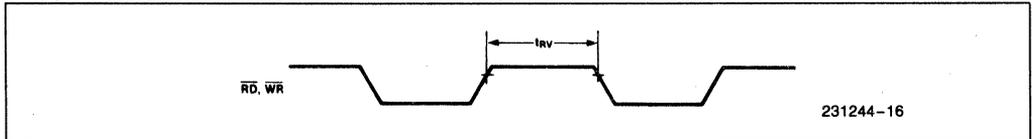
WRITE



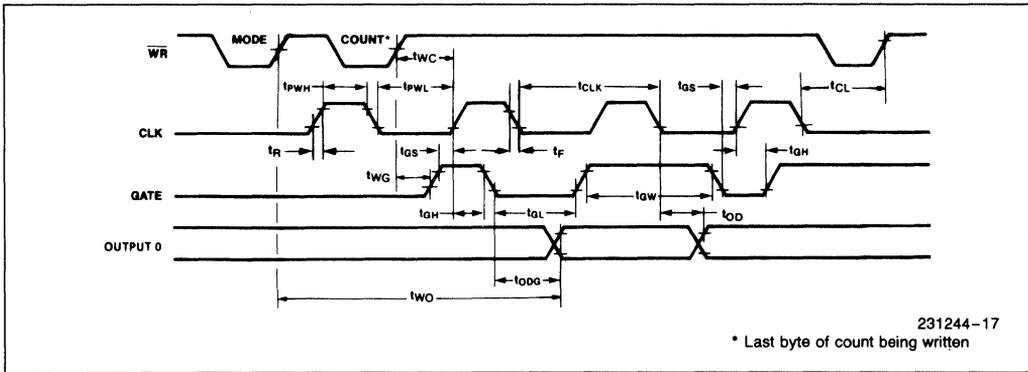
READ



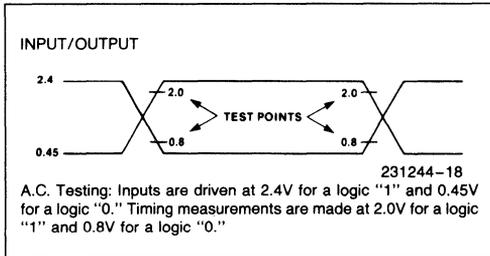
RECOVERY



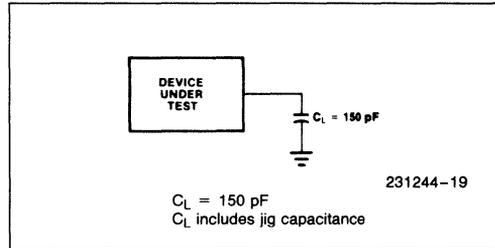
CLOCK AND GATE



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



82C55A CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- Compatible with all Intel and most other microprocessors
- High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188
- 24 Programmable I/O Pins
- Bus-hold circuitry on all I/O Ports Eliminates Pull-up Resistors
- Low Power CHMOS — $I_{CC} < 10 \text{ mA}$
- Completely TTL Compatible
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- 2.5 mA DC Drive Capability on all I/O Port Outputs

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a bi-directional bus, and 5 lines, borrowing one from the other group, for handshaking.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

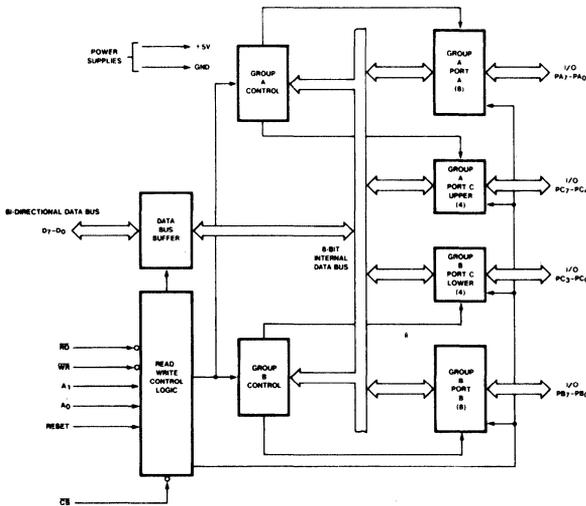


Figure 1. 82C55A Block Diagram

231256-1

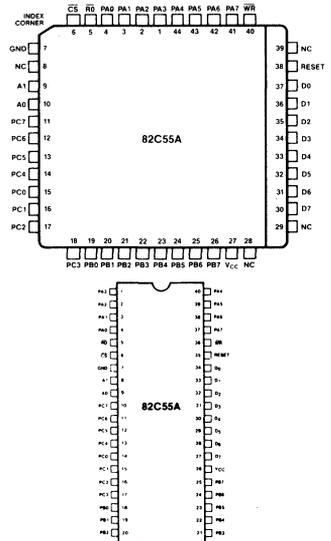


Figure 2. 82C55A Pinout
Diagrams are for pin reference only. Package sizes are not to scale.

231256-2

Table 1. Pin Description

Symbol	Pin Number		Type	Name and Function					
	Dip	PLCC							
PA ₃₋₀	1-4	1-4	I/O	PORT A, PINS 0-3: Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.					
\overline{RD}	5	5	I	READ CONTROL: This input is low during CPU read operations.					
\overline{CS}	6	6	I	CHIP SELECT: A low on this input enables the 82C55A to respond to \overline{RD} and \overline{WR} signals. \overline{RD} and \overline{WR} are ignored otherwise.					
GND	7	7		System Ground					
A ₁₋₀	8-9	9-10	I	ADDRESS: These input signals, in conjunction \overline{RD} and \overline{WR} , control the selection of one of the three ports or the control word registers.					
				A₁	A₀	\overline{RD}	\overline{WR}	\overline{CS}	Input Operation (Read)
				0	0	0	1	0	Port A - Data Bus
				0	1	0	1	0	Port B - Data Bus
				1	0	0	1	0	Port C - Data Bus
				1	1	0	1	0	Control Word - Data Bus
				Output Operation (Write)					
				0	0	1	0	0	Data Bus - Port A
				0	1	1	0	0	Data Bus - Port B
				1	0	1	0	0	Data Bus - Port C
				1	1	1	0	0	Data Bus - Control
				Disable Function					
				X	X	X	X	1	Data Bus - 3 - State
				X	X	1	1	0	Data Bus - 3 - State
PC ₇₋₄	10-13	11-14	I/O	PORT C, PINS 4-7: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.					
PC ₀₋₃	14-17	15-18	I/O	PORT C, PINS 0-3: Lower nibble of Port C.					
PB ₀₋₇	18-25	19-26	I/O	PORT B, PINS 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer.					
V _{CC}	26	27		SYSTEM POWER: + 5V Power Supply.					
D ₇₋₀	27-34	30-37	I/O	DATA BUS: Bi-directional, tri-state data bus lines, connected to system data bus.					
RESET	35	38	I	RESET: A high on this input clears the control register and all ports are set to the input mode.					
\overline{WR}	36	40	I	WRITE CONTROL: This input is low during CPU write operations.					
PA ₇₋₄	37-40	41-44	I/O	PORT A, PINS 4-7: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.					
NC		8, 28, 29, 39		No Connect					

82C55A FUNCTIONAL DESCRIPTION

General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7-C4)
Control Group B - Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

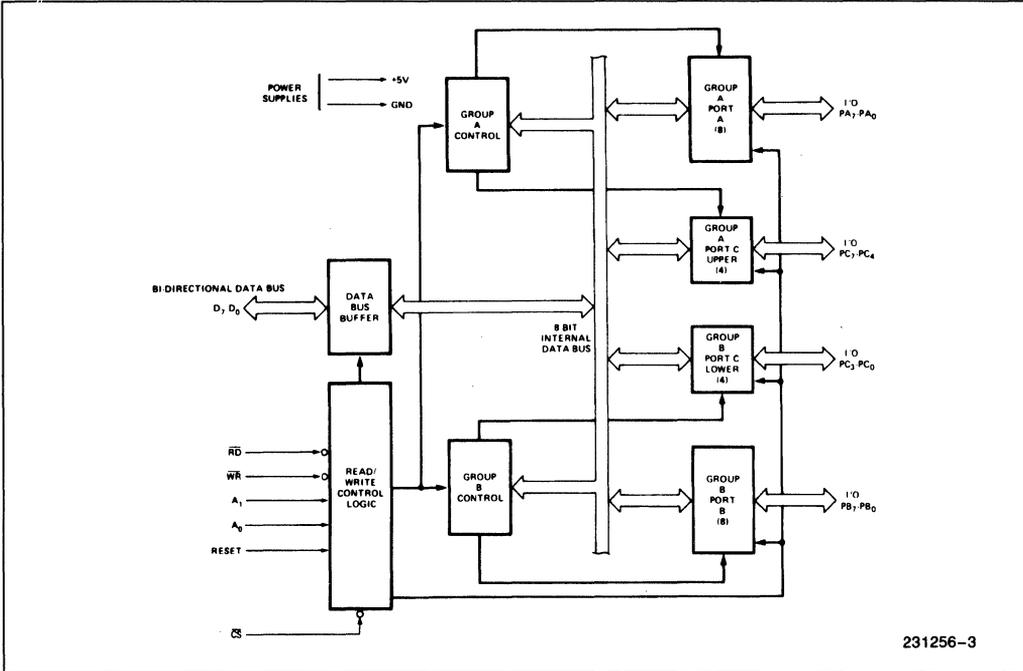
The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer. Only "pull-up" bus hold devices are present on Port B.

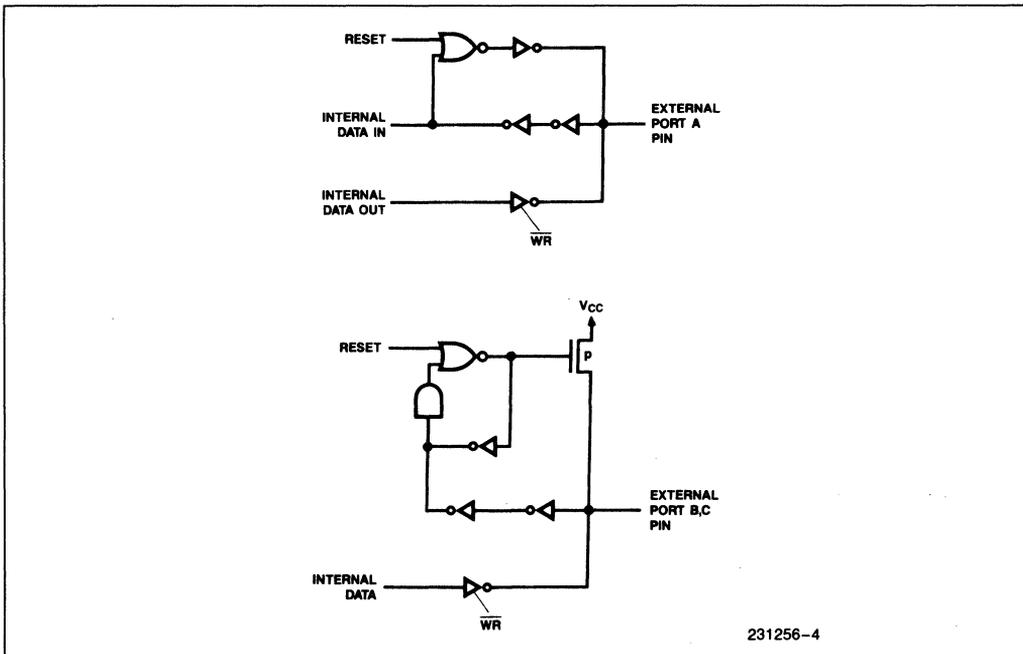
Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.



231256-3

Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions



231256-4

Figure 4. Port A, B, C, Bus-hold Configuration

82C55A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 — Basic input/output
- Mode 1 — Strobed Input/output
- Mode 2 — Bi-directional Bus

When the reset input goes "high" all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus hold devices. After the reset is removed the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

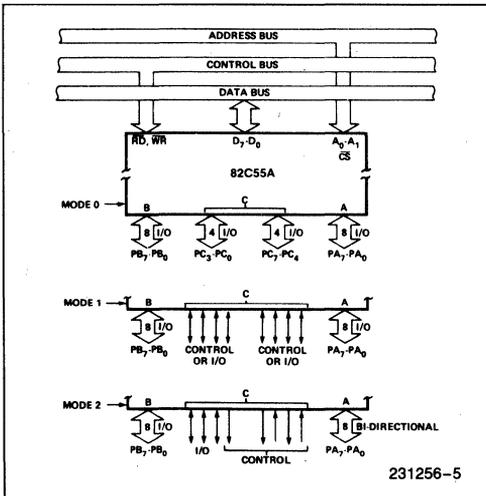


Figure 5. Basic Mode Definitions and Bus Interface

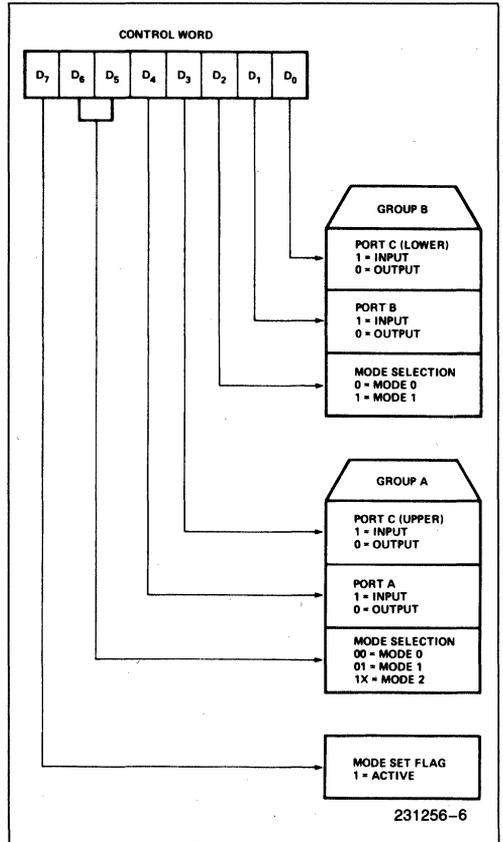


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTPUT instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

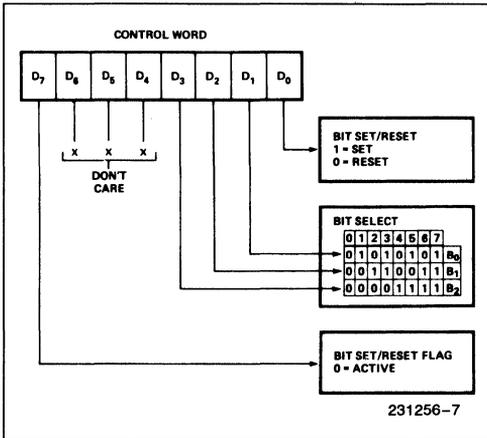


Figure 7. Bit Set/Reset Format

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

- (BIT-SET)—INTE is SET—Interrupt enable
- (BIT-RESET)—INTE is RESET—Interrupt disable

Note:

All Mask flip-flops are automatically reset during mode selection and device Reset.

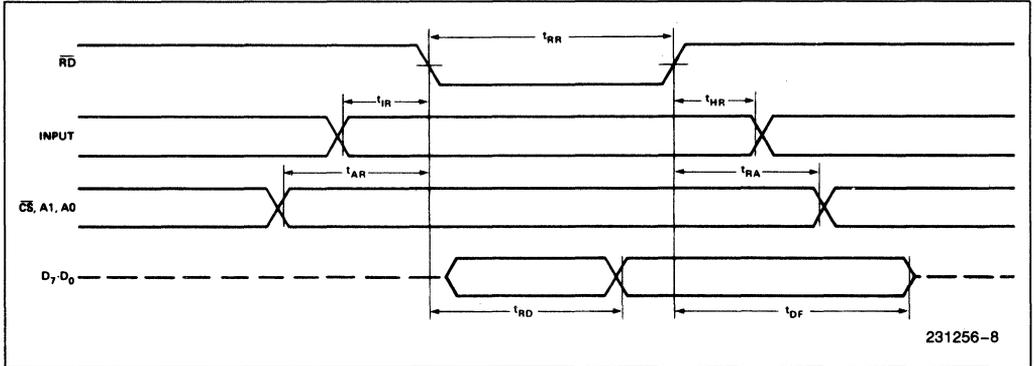
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

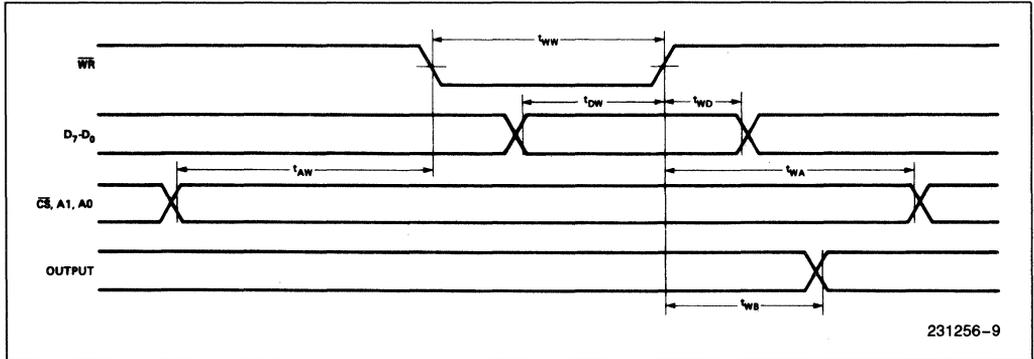
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



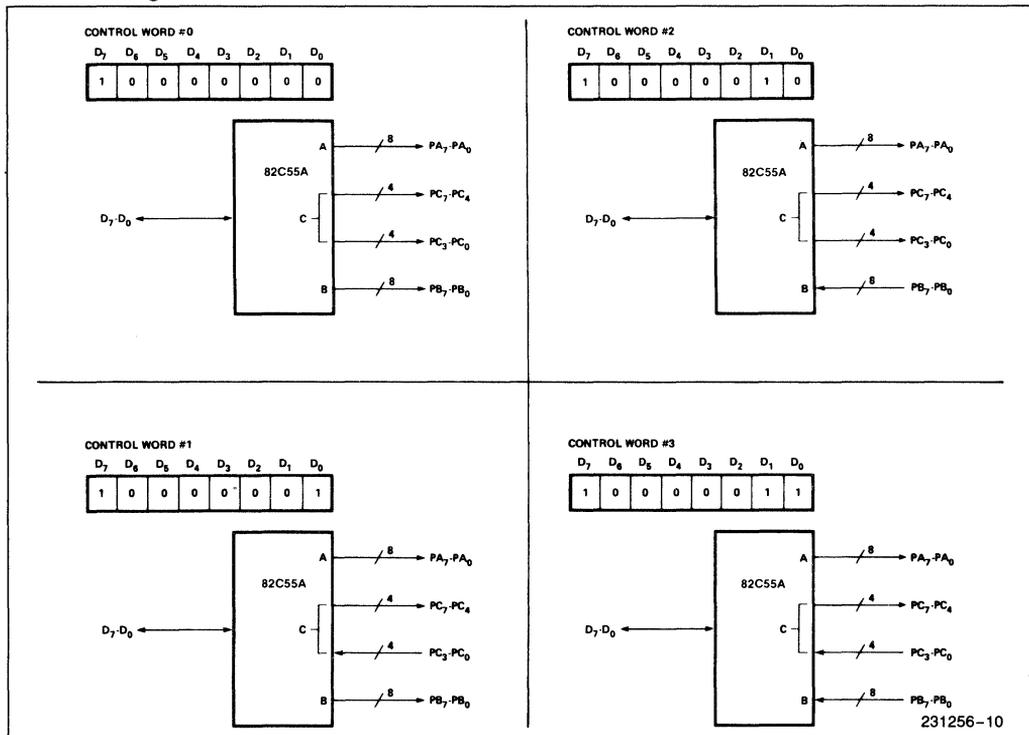
MODE 0 (BASIC OUTPUT)



MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D ₄	D ₃	D ₁	D ₀	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

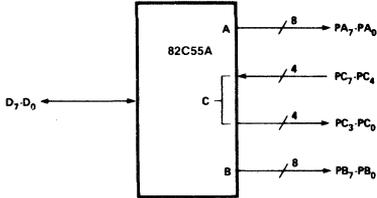


231256-10

MODE 0 Configurations (Continued)

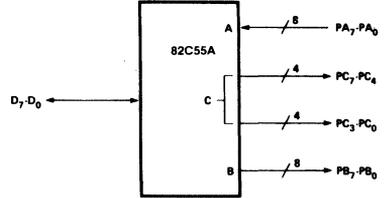
CONTROL WORD #4

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	0	0



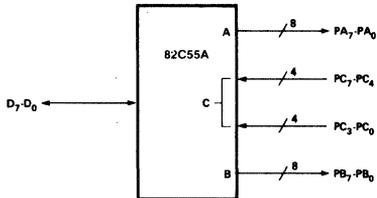
CONTROL WORD #8

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	0	0



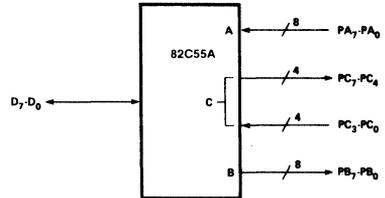
CONTROL WORD #5

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	0	1



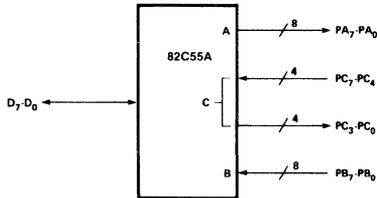
CONTROL WORD #9

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	0	1



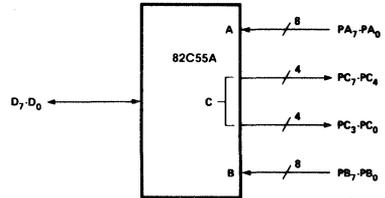
CONTROL WORD #6

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	1	0



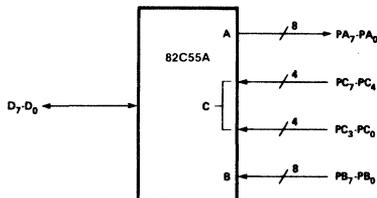
CONTROL WORD #10

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	1	0



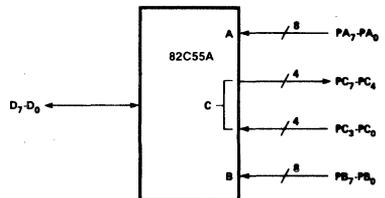
CONTROL WORD #7

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	1	1



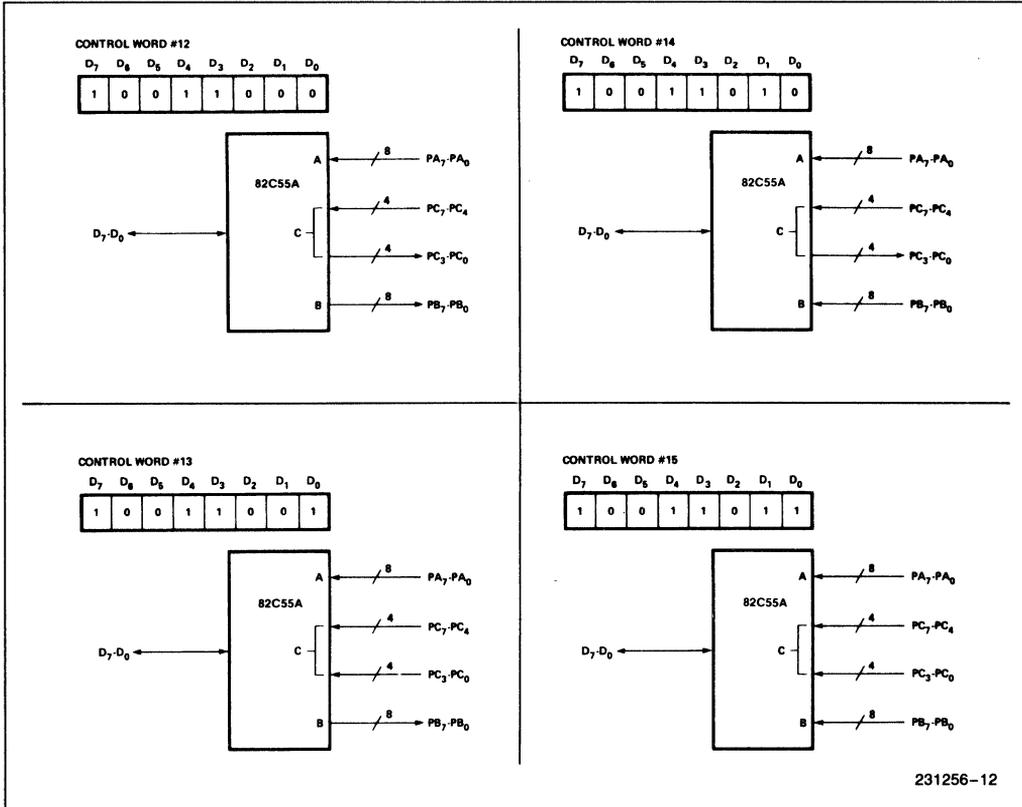
CONTROL WORD #11

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	1	1



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MODE 0 Configurations (Continued)



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Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC₄.

INTE B

Controlled by bit set/reset of PC₂.

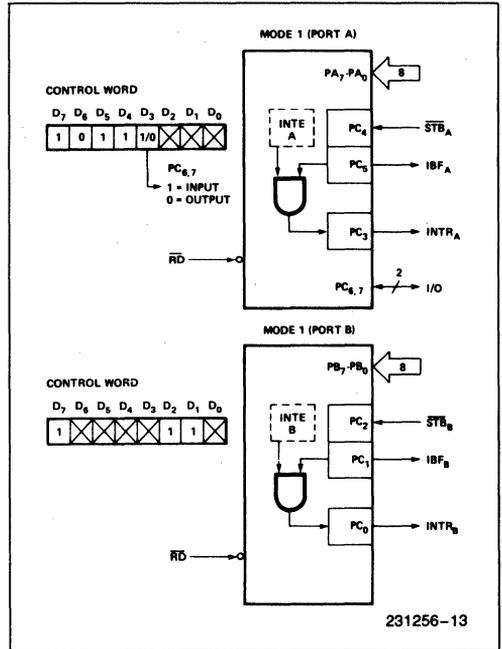


Figure 8. MODE 1 Input

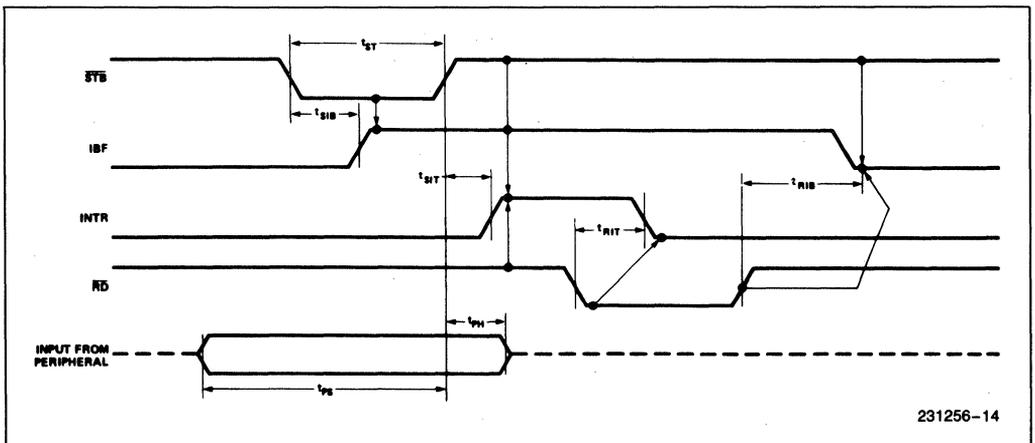


Figure 9. MODE 1 (Strobed Input)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

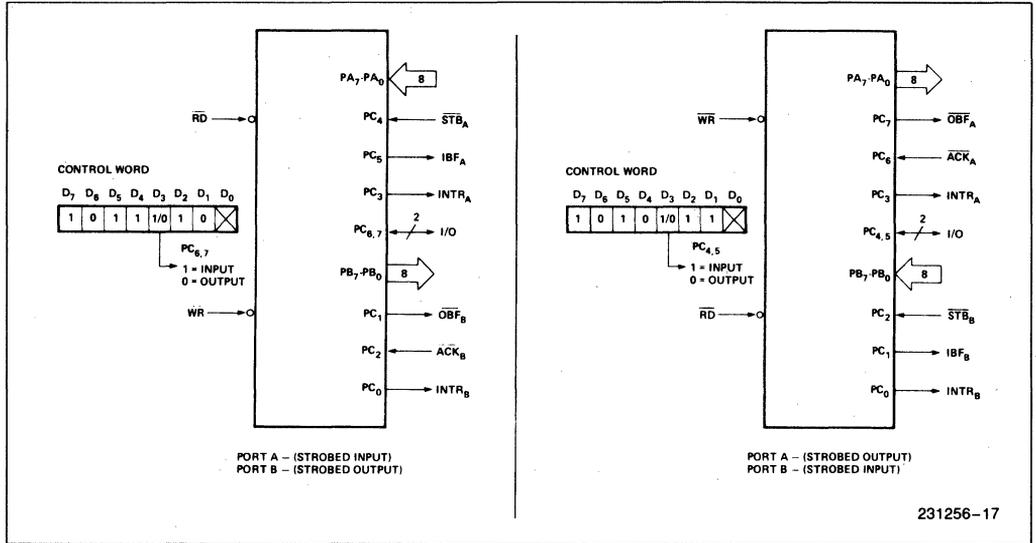


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A **only**.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for input or output operations.

Output Operations

OBF (Output Buffer Full). The OBF output will go "low" to indicate that the CPU has written data out to port A.

ACK (Acknowledge). A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC₆.

Input Operations

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC₄.

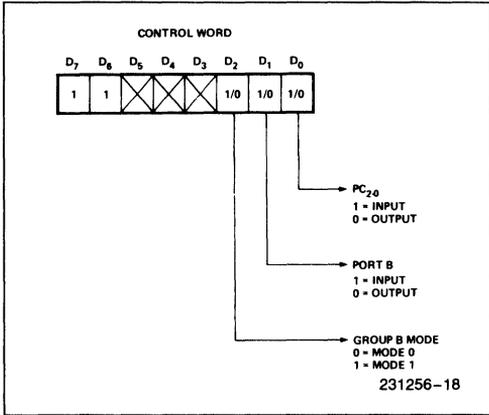


Figure 13. MODE Control Word

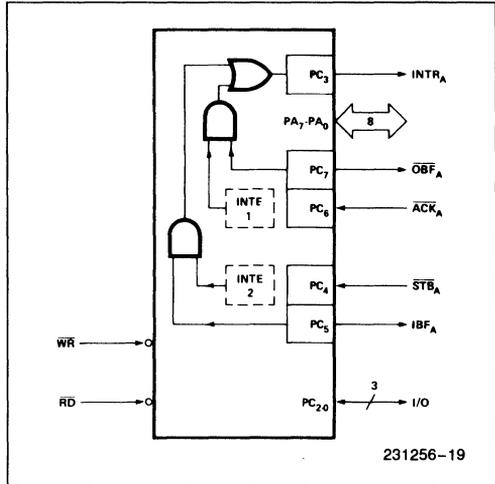


Figure 14. MODE 2

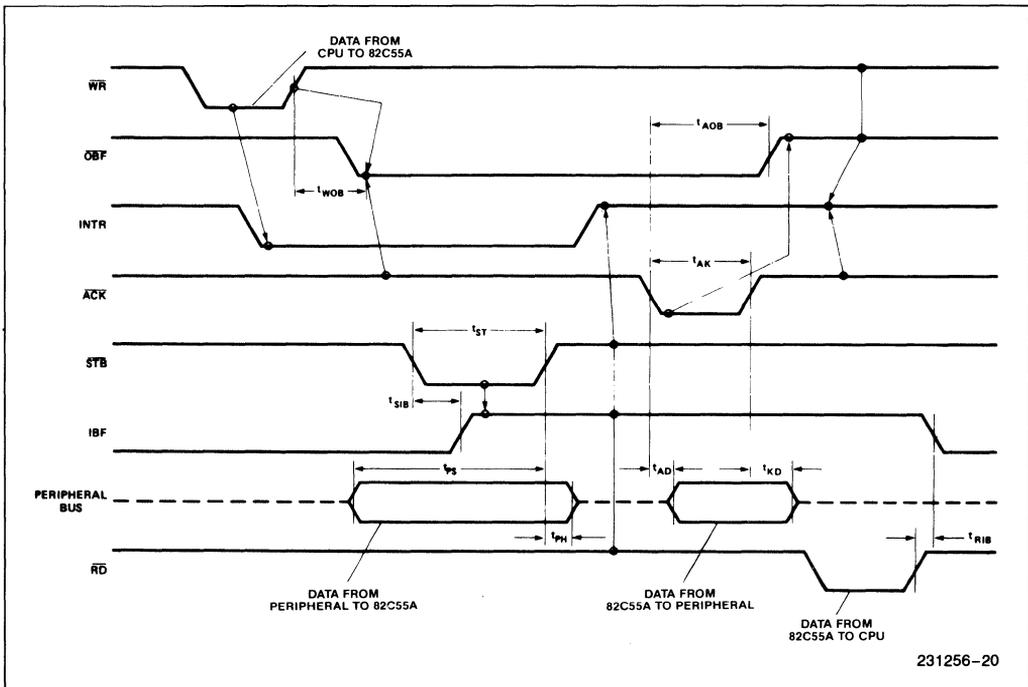
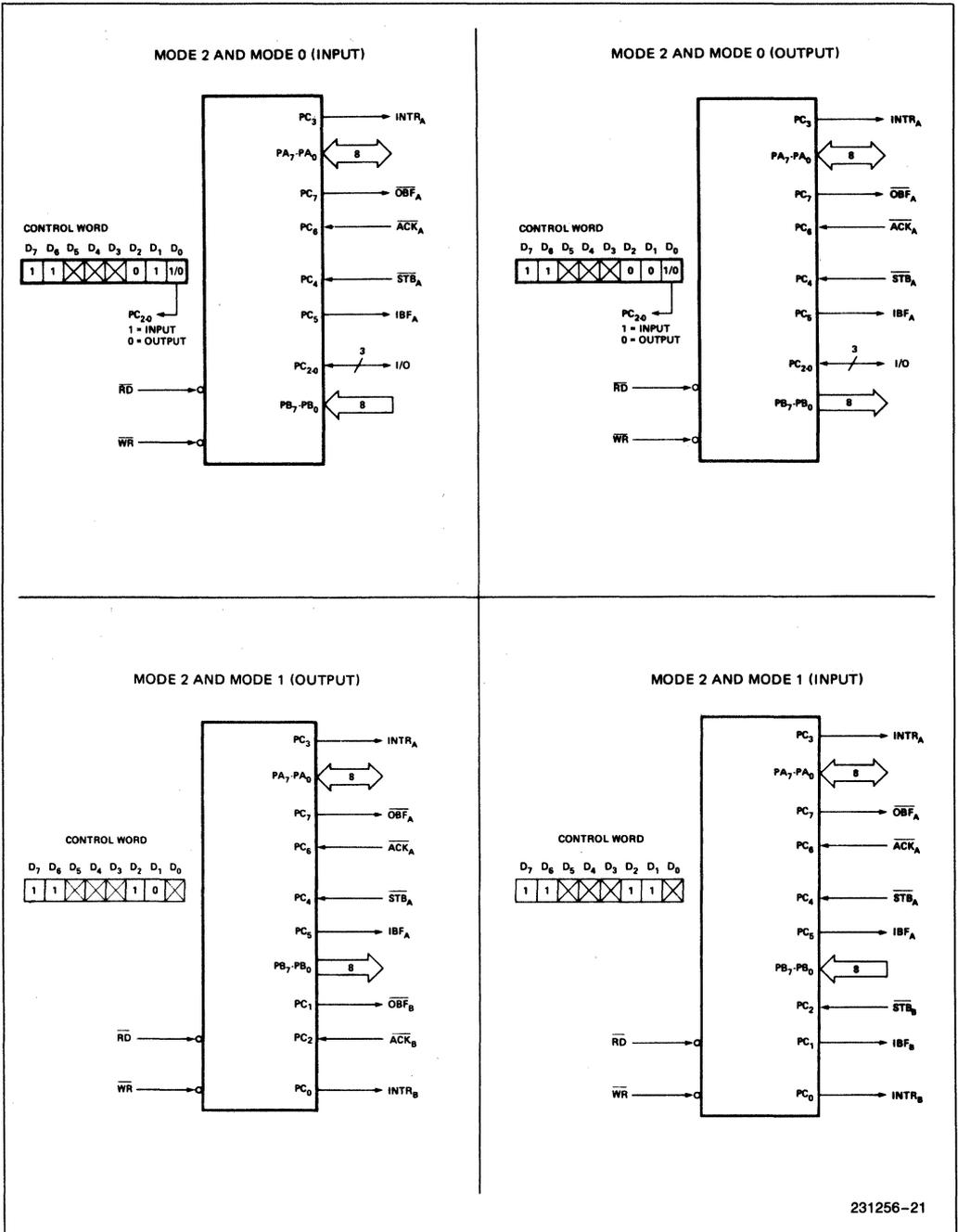


Figure 15. MODE 2 (Bidirectional)

NOTE:

Any sequence where \overline{WR} occurs before \overline{ACK} , and \overline{STB} occurs before \overline{RD} is permissible.
 $(INTR = IBF \cdot MASK \cdot STB \cdot RD + OBF \cdot MASK \cdot ACK \cdot WR)$



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Figure 16. MODE 1/4 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA ₀	IN	OUT	IN	OUT	↔	
PA ₁	IN	OUT	IN	OUT	↔	
PA ₂	IN	OUT	IN	OUT	↔	
PA ₃	IN	OUT	IN	OUT	↔	
PA ₄	IN	OUT	IN	OUT	↔	
PA ₅	IN	OUT	IN	OUT	↔	
PA ₆	IN	OUT	IN	OUT	↔	
PA ₇	IN	OUT	IN	OUT	↔	
PB ₀	IN	OUT	IN	OUT	—	
PB ₁	IN	OUT	IN	OUT	—	
PB ₂	IN	OUT	IN	OUT	—	
PB ₃	IN	OUT	IN	OUT	—	
PB ₄	IN	OUT	IN	OUT	—	
PB ₅	IN	OUT	IN	OUT	—	
PB ₆	IN	OUT	IN	OUT	—	
PB ₇	IN	OUT	IN	OUT	—	
PC ₀	IN	OUT	INTR _B	INTR _B	I/O	
PC ₁	IN	OUT	IBF _B	OBFB _B	I/O	
PC ₂	IN	OUT	STB _B	ACK _B	I/O	
PC ₃	IN	OUT	INTR _A	INTR _A	INTR _A	
PC ₄	IN	OUT	STB _A	I/O	STB _A	
PC ₅	IN	OUT	IBF _A	I/O	IBF _A	
PC ₆	IN	OUT	I/O	ACK _A	ACK _A	
PC ₇	IN	OUT	I/O	OBFA _A	OBFA _A	

MODE 0
OR MODE 1
ONLY

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the ACK and STB lines, will be placed on the data bus. In place of the ACK and STB line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to

change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBFB) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including ACK and STB lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the ACK and STB lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 18.

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5 mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

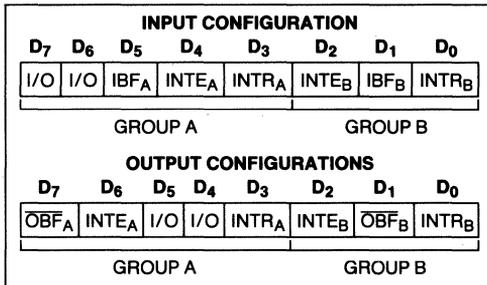


Figure 17a. MODE 1 Status Word Format

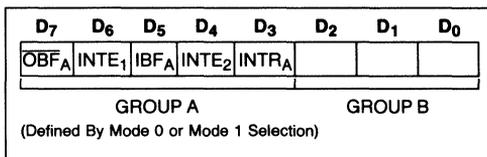


Figure 17b. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	\overline{ACK}_B (Output Mode 1) or \overline{STB}_B (Input Mode 1)
INTE A2	PC4	\overline{STB}_A (Input Mode 1 or Mode 2)
INTE A1	PC6	\overline{ACK}_A (Output Mode 1 or Mode 2)

Figure 18. Interrupt Enable Flags in Modes 1 and 2

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias0°C to + 70°C
 Storage Temperature - 65°C to + 150°C
 Supply Voltage - 0.5 to + 8.0V
 Operating Voltage + 4V to + 7V
 Voltage on any Input GND - 2V to + 6.5V
 Voltage on any Output GND - 0.5V to V_{CC} + 0.5V
 Power Dissipation 1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
V _{IL}	Input Low Voltage	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 2.5 mA
V _{OH}	Output High Voltage	3.0 V _{CC} - 0.4		V V	I _{OH} = -2.5 mA I _{OH} = -100 μA
I _{IL}	Input Leakage Current		± 10	μA	V _{IN} = V _{CC} to 0V
I _{OL}	Output Float Leakage Current		± 10	μA	V _{IN} = V _{CC} to 0V
I _{DAR}	Darlington Drive Current	-2.0		mA	Ports A, B, C R _{ext} = 750 Ω V _{ext} = 1.5V
I _{BHL}	Bus Hold Low Leakage Current	+ 50	+ 300	μA	V _{OUT} = 1.0V Port A only
I _{BHH}	Bus Hold High Leakage Current	- 50	- 300	μA	V _{OUT} = 3.0V Ports A, B, C
I _{CC}	V _{CC} Supply Current		10	mA	Outputs Open See Note
I _{CCSB}	V _{CC} Supply Current-Standby		10	μA	V _{CC} = 5.5V V _{IN} = V _{CC} or GND Outputs Open

Note:

Average I_{CC} with all outputs open is 100 μA.

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to GND
$C_{I/O}$	I/O Capacitance		20	pF	

A.C. CHARACTERISTICS

$T_A = 0^\circ$ to 70°C , $V_{CC} = +5\text{V} \pm 10\%$, $\text{GND} = 0\text{V}$

BUS PARAMETERS

READ CYCLE

Symbol	Parameter	82C55A		82C55A-2		Units	Test Conditions
		Min	Max	Min	Max		
t_{AR}	Address Stable Before $\overline{\text{RD}} \downarrow$	0		0		ns	
t_{RA}	Address Hold Time After $\overline{\text{RD}} \uparrow$	0		0		ns	
t_{RR}	$\overline{\text{RD}}$ Pulse Width	150		150		ns	
t_{RD}	Data Delay from $\overline{\text{RD}} \downarrow$		120		120	ns	
t_{DF}	$\overline{\text{RD}} \uparrow$ to Data Floating	10	75	10	75	ns	
t_{RV}	Recovery Time between $\overline{\text{RD}}/\overline{\text{WR}}$	300		300		ns	

WRITE CYCLE

Symbol	Parameter	82C55A		82C55A-2		Units	Test Conditions
		Min	Max	Min	Max		
t_{AW}	Address Stable Before $\overline{\text{WR}} \downarrow$	0		0		ns	
t_{WA}	Address Hold Time After $\overline{\text{WR}} \uparrow$	20		20		ns	Ports A & B
		100		20		ns	Port C
t_{WW}	$\overline{\text{WR}}$ Pulse Width	100		100		ns	
t_{DW}	Data Setup Time Before $\overline{\text{WR}} \uparrow$	100		100		ns	
t_{WD}	Data Hold Time After $\overline{\text{WR}} \uparrow$	30		30		ns	Ports A & B
		100		30		ns	Port C

OTHER TIMINGS

Symbol	Parameter	82C55A		82C55A-2		Units	Test Conditions
		Min	Max	Min	Max		
t _{WB}	$\overline{WR} = 1$ to Output		350		350	ns	
t _{IR}	Peripheral Data Before \overline{RD}	0		0		ns	
t _{HR}	Peripheral Data After \overline{RD}	0		0		ns	
t _{AK}	\overline{ACK} Pulse Width	100		100		ns	
t _{ST}	\overline{STB} Pulse Width	100		100		ns	
t _{PS}	Per. Data Before \overline{STB} High	20		20		ns	
t _{PH}	Per. Data After \overline{STB} High	50		50		ns	
t _{AD}	$\overline{ACK} = 0$ to Output		175		175	ns	
t _{KD}	$\overline{ACK} = 1$ to Output Float	20	250	20	250	ns	
t _{WOB}	$\overline{WR} = 1$ to $\overline{OBF} = 0$		150		150	ns	
t _{AOB}	$\overline{ACK} = 0$ to $\overline{OBF} = 1$		150		150	ns	
t _{SIB}	$\overline{STB} = 0$ to $IBF = 1$		150		150	ns	
t _{RIB}	$\overline{RD} = 1$ to $IBF = 0$		150		150	ns	
t _{RIT}	$\overline{RD} = 0$ to $INTR = 0$		200		200	ns	
t _{SIT}	$\overline{STB} = 1$ to $INTR = 1$		150		150	ns	
t _{AIT}	$\overline{ACK} = 1$ to $INTR = 1$		150		150	ns	
t _{WIT}	$\overline{WR} = 0$ to $INTR = 0$		200		200	ns	see note 1
t _{RES}	Reset Pulse Width.	500		500		ns	see note 2

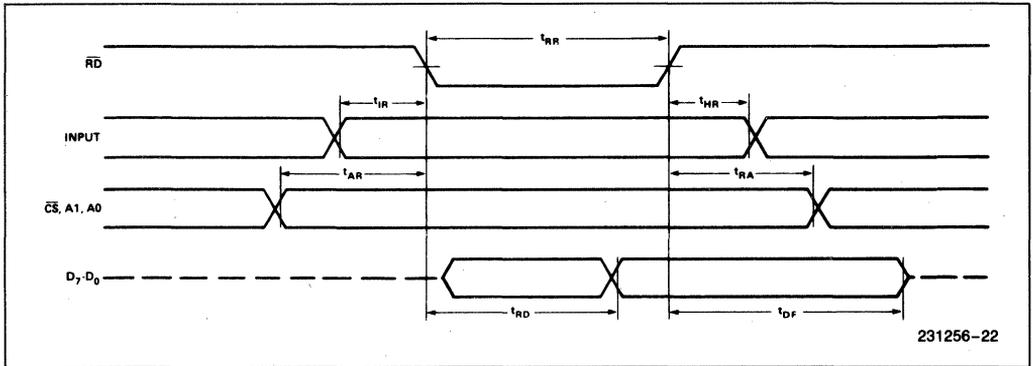
NOTE:

1. $INTR \uparrow$ may occur as early as $\overline{WR} \downarrow$.

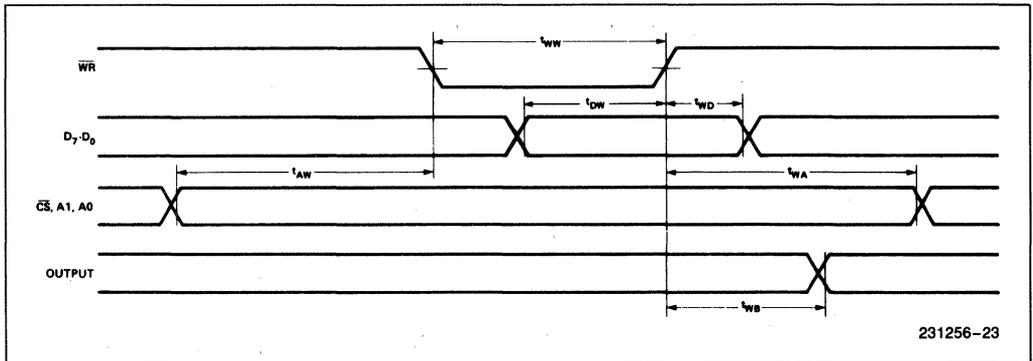
2. Pulse width of initial Reset pulse after power on must be at least 50 μ Sec. Subsequent Reset pulses may be 500 ns minimum.

WAVEFORMS

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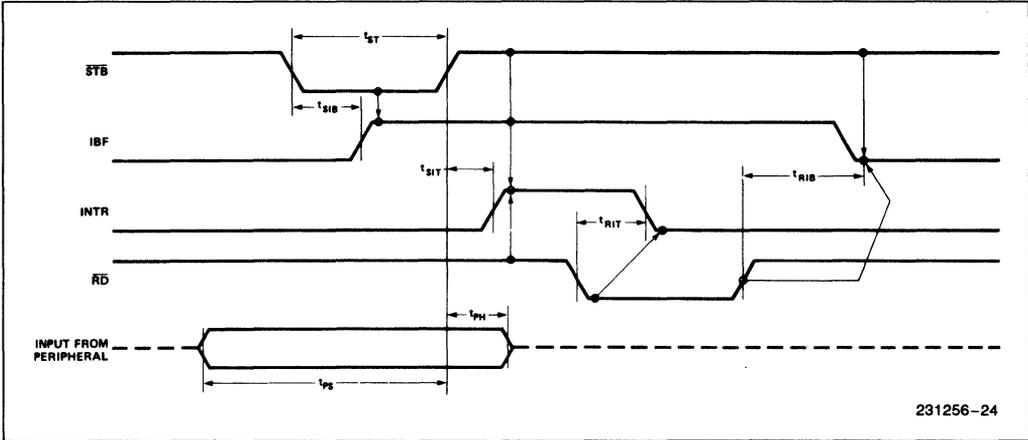


MODE 0 (BASIC OUTPUT)

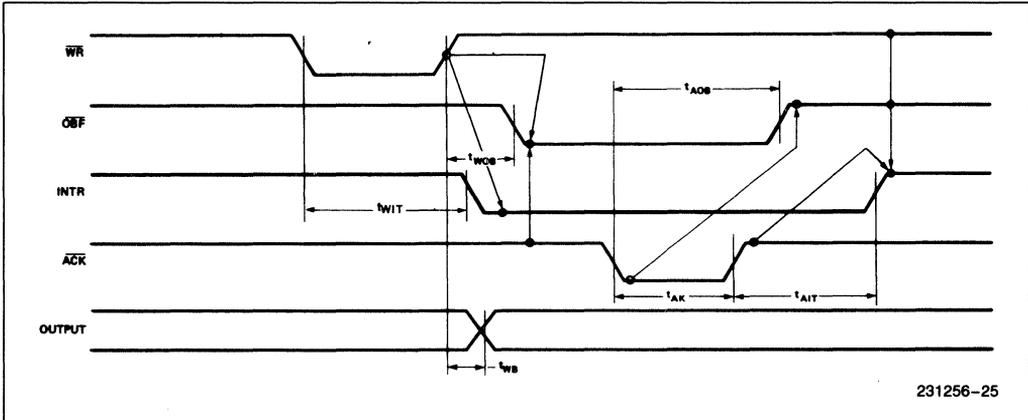


WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

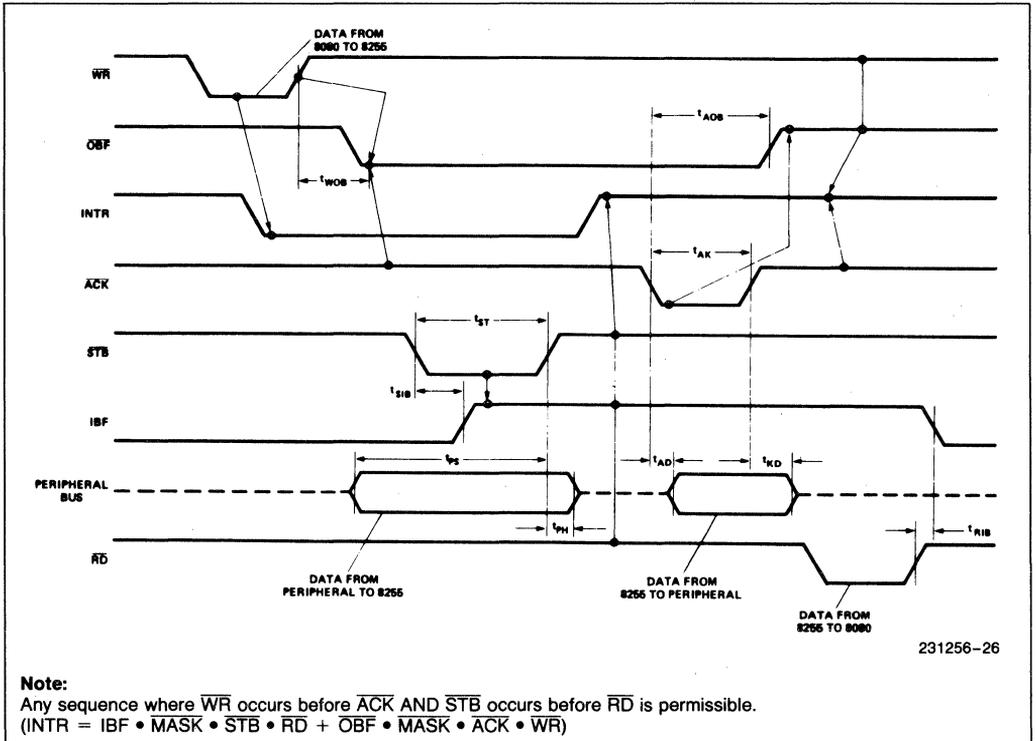


MODE 1 (STROBED OUTPUT)

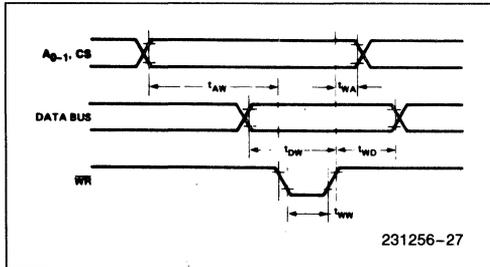


WAVEFORMS (Continued)

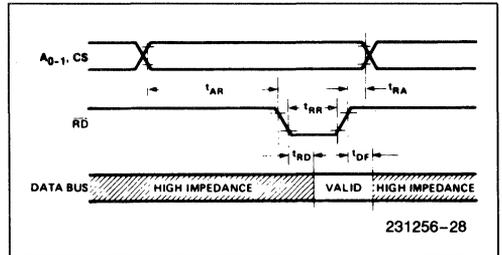
MODE 2 (BIDIRECTIONAL)



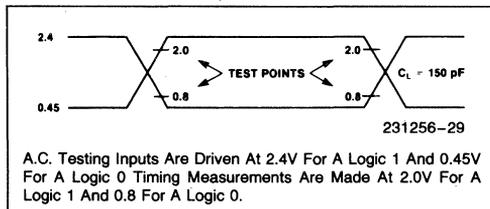
WRITE TIMING



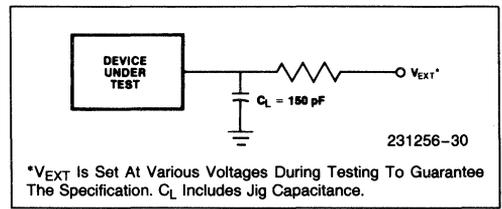
READ TIMING



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



Additional References

For additional information, the following documents appear in the appropriate product line handbook.

Memory Components

APPLICATION NOTES

- AP-171 Low Power with CHMOS DRAMs
- AP-172 CHMOS DRAMs In Graphics Applications

ARTICLE REPRINTS

- AR-311 System Implications of CHMOS Dynamic RAMs
- AR-312 Static Column Architecture in CHMOS Dynamic RAMs — A Graphics Memory Solution
- AR-313 CMOS vs. NMOS Comparisons In Dynamic RAM Design
- AR-332 Modular Approach to C-MOS Technology Tailors Process To Application
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- AR-302 Inside CMOS Technologies



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