USER'S MANUAL

Hitachi 8-Bit Microcomputer
HD63265 FDC
Floppy Disk Controller

◉ HITACHI

2nd Edition

Hitachi 8-Bit Microcomputer

HD63265
Floppy Disk Controller (FDC)
User's Manual

◎ HITACHI

CONTENTS

SECTION 1. GENERAL DESCRIPTION

1.1 INTRODUCTION

Recently, floppy disc drives (FDDs) have taken on the following features:

. Smaller size

. Larger capacity

. Higher speed

. Lower power dissipation

. Lower cost

To control and manage data transfers to and from such FDDs, Hitachi has developed a new Floppy Disk Controller (FDC). This FDC has the following major features.

1. Built-in VFO and write precompensation circuits: Since this FDC contains a built-in VFO circuit and a write precompensation circuit, which previously had to be externally installed, a compact system and lower system construction cost can be achieved. The VFO circuit is an analog PLL type to meet the high accuracy requirements for controlling large-capacity, high-speed FDDs.

2. CMOS process plus SLEEP command: Low power dissipation is achieved utilizing CMOS process. Furthermore, a SLEEP command which enables the FDC to enter a very low power dissipation mode is provided for use in FDD systems requiring or having a standby mode.

3. Command code compatible with standard FDCs: This FDC is command code compatible with standard FDCs, making it easy to be integrated into an existing design. Furthermore, for easy use in existing systems, the FDC has various modes to include control of all types of FDDs, and interfaces for both 68- and 80- series microprocessors.

1.2 NOTES ON USAGE

. Stepping rate is programmable from 1 ms to 16 ms by 1 ms increments in both 5" and 8" modes. In 5" mode, the stepping rate is also programmable from 2 ms to 32 ms by 2 ms increments.

. There is no read skip area around the Index.

. Requires no write clock.

. Stepping rate is always exact as specified.

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. The delay from the detection of US0, US1 signals to read the FDD status is 3 μs.
. The delay is 2 ms (8" mode) or 4 ms (5" mode) from WGATE signal's falling edge to HSEL signal's rising edge in multitrack write mode.
. Recalibrate operation is based on 255 step pulses.
. WDATA signal is always at low level when WGATE signal is at low level.
. $\overline{\text{IRQ}}$ and $\overline{\text{DREQ}}$ become inactive (high level) automatically when a data overrun error is detected.

1.3 FEATURES

. On-chip high accuracy data separator (adjustment-free analog VFO system)
  - No adjustment required
. On-chip write precompensation circuit
  - Delay times programmable from 0 to 750 ns in 62.5 ns increments
  - Different delay times for inner and outer tracks
  - Outer to inner switchover track programmable from 1 to 254
. Low power dissipation
  - CMOS circuit plus SLEEP command
. Command code compatible with standard FDCs
. Selectable recording codes
  - FM and MFM
. Serial data transfer rate
  - FM mode: 125, 150, 250 Kbps
  - MFM mode: 250, 300, 500 Kbps
. Selectable DMA and Non-DMA host data transfers
. Compatible with both 68- and 80- series microprocessors
. Formatting
  - Both IBM and ECMA (ISO) track formats supported
. Error checking
  - 16-bit CRC generator and checker incorporated
    CRC polynomial: $x^{16}+x^{12}+x^5+1$
. Multi-sector and multi-track read/write capability
. Data scan capability
  - Scans a single sector or an entire cylinder comparing the disk data byte-by-byte with the host memory data
. Multi-drive parallel seek capability
. Stepping rate, head load time, and head unload time programmable
  - Stepping rate programmable in 1 ms increments in 5" mode

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. Maximum drive control range:

  - Number of drives: 4

  - Number of cylinders: 255 cylinders/drive

  - Number of sectors: 255 sectors/track

  - Number of heads: 2 heads/drive

. Sector length programmable

  - 128, 256, 512, 1024, 2048, 4096, 8192 bytes/sector

1.4 COMMAND DESCRIPTION LIST

This FDC supports 20 commands listed in Table 1-1. READ LONG and WRITE LONG commands become valid only after command SPECIFY 2 has been issued.

Table 1-1. FDC Commands

Commands	Functions
READ DATA	Reads data from any specified sector(s) except the deleted sector(s)
READ DELETED DATA	Reads data from any specified sector(s) containing a data address mark of F8
READ ERRONEOUS DATA	Reads data from the first sector immediately after the index to the end of track regardless whether there are errors or not
READ ID	Reads the first errorfree ID encountered on a track
WRITE DATA	Writes data to any specified sector(s) using a data address mark of FB
WRITE DELETED DATA	Writes data to any specified sector(s) using a data address mark of F8
WRITE FORMAT	Formats the track where the head is currently positioned
SEEK	Moves the selected FDD's head to a specified track
RECALIBRATE	Moves the selected FDD's head to track 0
COMPARE EQUAL	Compares the data read from the selected FDD with the data sent from the host according to the chosen command
COMPARE LOW OR EQUAL	
COMPARE HIGH OR EQUAL	
CHECK DEVICE STATUS	Reads the selected FDD's status
CHECK INTERRUPT STATUS	Reads the interrupt causes

Table 1-1.   FDC Commands (cont)

Commands	Functions
SPECIFY 1	Specifies the FDC operating mode and sets up the various timers in the FDC
SPECIFY 2*	
SLEEP *	Sets the FDC to the low power dissipation mode
ABORT *	Software reset command
READ LONG *	Reads the CRC bytes as well as the data from a sector to the host
WRITE LONG *	Writes the CRC bytes as well as the data to a sector from the host

Note: Commands marked with * are newly added commands which are unique to this FDC. Rest of the commands are identical to other standard FDC commands.

SECTION 2. PIN DESCRIPTION

2.1 PIN CONFIGURATION

Figure 2-1 shows the pin configuration. Table 2-1 describes the pin functions.

```
        Vcc1  | 1 O           48 | LCT
        NUM1  | 2             47 | FRES
        NUM2  | 3             46 | HLOAD
       SFORM  | 4             45 | HSEL
         IFS  | 5             44 | HDIR
       8"/5"  | 6             43 | STEP
       RESET  | 7             42 | READY
       E,RD   | 8             41 | WPRT
      R/W,WR  | 9             40 | DSIDE
          CS  | 10            39 | FAULT
        DACK  | 11            38 | TRKO
          RS  | 12            37 | INDEX
        Vss1  | 13            36 | US0
          D0  | 14            35 | US1
          D1  | 15            34 | EARLY
          D2  | 16            33 | LATE
          D3  | 17            32 | WDATA
          D4  | 18            31 | WGATE
          D5  | 19            30 | RDATA
          D6  | 20            29 | Vcc2
          D7  | 21            28 | NC
        DREQ  | 22            27 | NC
         IRQ  | 23            26 | Vss2
        DEND  | 24            25 | CLK
```
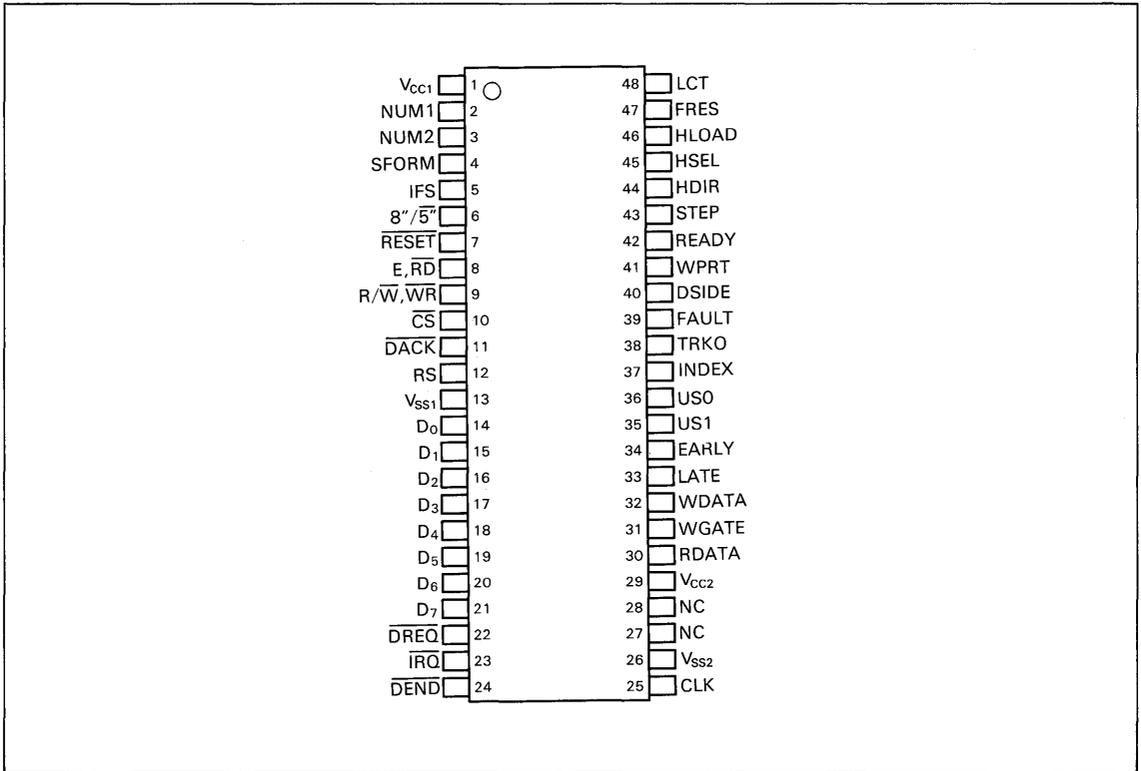
Figure 2-1. Pin Configuration

$V_{CC1}-V_{CC4}$	+5 V
$V_{SS1}-V_{SS3}$	Ground
NUM1	Not User Mode 1
NUM2	Not User Mode 2
SFORM	Select Format
IFS	Interface Select
8"/5"	8"/5" Mode Select
$\overline{RESET}$	Reset
E, $\overline{RD}$	Enable, Read
R/$\overline{W}$, $\overline{WR}$	Read/Write, Write
$\overline{CS}$	Chip Select
$\overline{DACK}$	DMA Acknowledge
RS	Register Select
D_0	
D_1	
D_2	
D_3	
D_4	Data Bus 0−7
D_5	
D_6	
D_7	
$\overline{DREQ}$	DMA Request
$\overline{IRQ}$	Interrupt Request
$\overline{DEND}$	DMA End

LCT	Low Current
FRES	Fault Reset
HLOAD	Head Load
HSEL	Head Select
HDIR	Head Direction
STEP	Step
READY	Ready
WPRT	Write Protected
DSIDE	Double Sided
FAULT	Fault
TRKO	Track 00
INDEX	Index
US0	Unit Select 0
US1	Unit Select 1
EARLY	Early
LATE	Late
WDATA	Write Data
WGATE	Write Gate
RDATA	Read Data
NC	No Connection
CLK	Clock
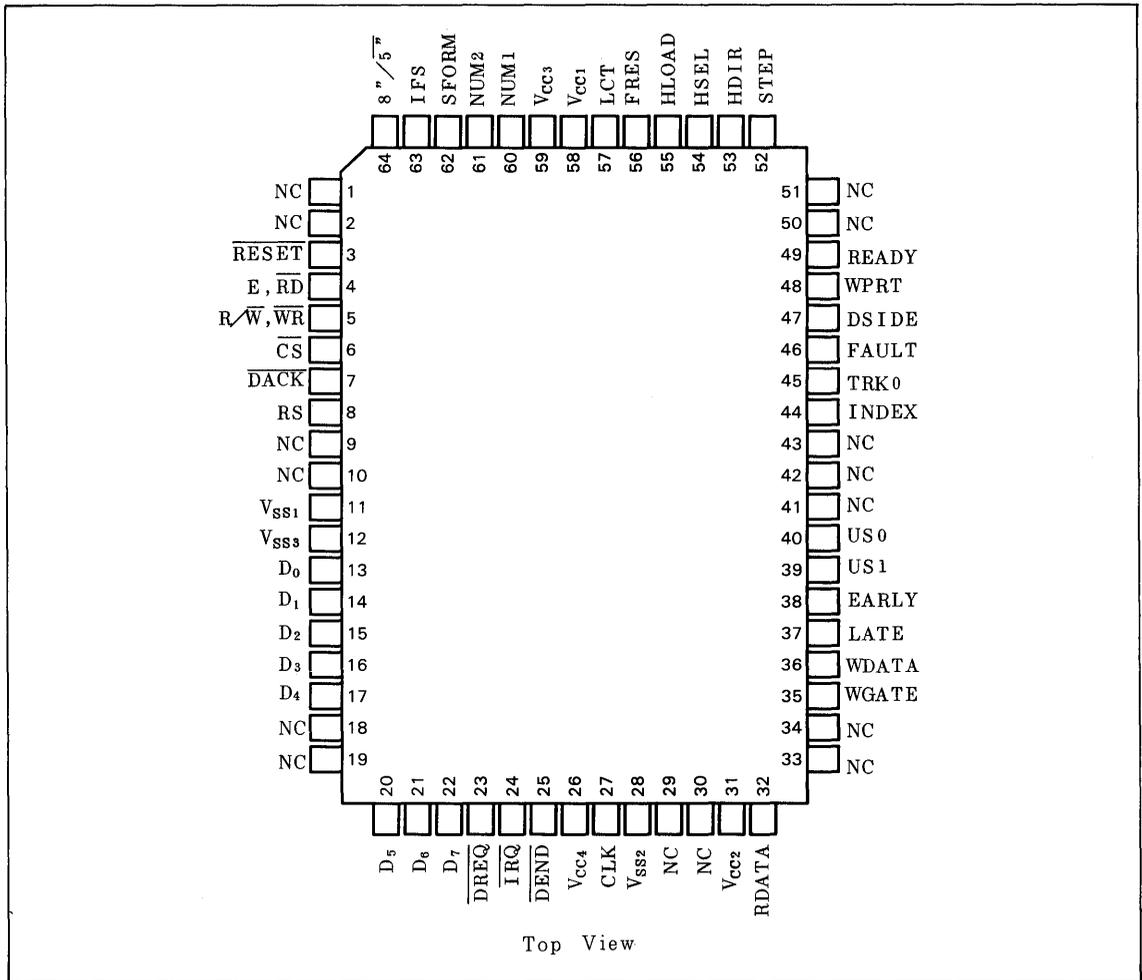
Figure 2-2. Pin Arrangement (FP-64)

Table 2-1. Pin Functions

Type	Pin No. DP-48	Pin No. FP-64	Symbol	Pin Name	Input/Output
Power	1	58	V_{CC1}	V_{CC1}	–
Supply,	13	11	V_{SS1}	V_{SS1}	–
Clock	29	31	V_{CC2}	V_{CC2}	–
	26	28	V_{SS2}	V_{SS2}	–
	25	27	CLK	Clock	Input
		59	V_{CC3}	V_{CC3}	–
		26	V_{CC4}	V_{CC4}	–
		12	V_{SS3}	V_{SS3}	–
MPU	7	3	$\overline{RESET}$	Reset	Input
Interface	8	4	E, $\overline{RD}$	Enable, Read	Input
	9	5	R/$\overline{W}$, $\overline{WR}$	Read/write, Write	Input
	10	6	$\overline{CS}$	Chip select	Input
	12	8	RS	Register select	Input
	14-21	13-22	D0-D7	Data bus, bits 0-7	Input/Output
	23	24	$\overline{IRQ}$	Interrupt request	Output
DMA	11	7	$\overline{DACK}$	DMA acknowledge	Input
Control	22	23	$\overline{DREQ}$	DMA request	Output
	24	25	$\overline{DEND}$	DMA end	Input
FDD	30	32	RDATA	Read data	Input
Interface	31	35	WGATE	Write gate	Output
	32	36	WDATA	Write data	Output
	33	37	LATE	Late	Output
	34	38	EARLY	Early	Output
	35	39	US1	Unit select 1	Output
	36	40	US0	Unit select 0	Output
	37	44	INDEX	Index	Input
	38	45	TRK0	Track 0	Input
	39	46	FAULT	Fault	Input
	40	47	DSIDE	Double sided	Input
	41	48	WPRT	Write protect	Input
	42	49	READY	Ready	Input
	43	52	STEP	Step	Output
	44	53	HDIR	Head direction	Output
	45	54	HSEL	Head select	Output
	46	55	HLOAD	Head load	Output
	47	56	FRES	Fault reset	Output
	48	57	LCT	Low current	Output

Table 2-1. Pin Functions (cont)

Type	Pin No. DP-48	FP-64	Symbol	Pin Name	Input/Output
FDC	4	62	SFORM	Select format	Input
Function	5	63	IFS	Interface select	Input
Switching	6	64	8"/$\overline{5}$"	8"/5" mode select	Input
Others	2	60	NUM1	Not-user mode 1	Input
	3	61	NUM2	Not-user mode 2	Input
	27 28	1,2 9,10 18,19 29,30 33,34 41-43 50,51	NC	No Connection	

2.2 SIGNAL DESCRIPTION

2.2.1 Power Supply, Clock

V_{CC1}, V_{CC2}, V_{CC3}, V_{CC4}, V_{SS1}, V_{SS2}, V_{SS3} (power Supply): V_{CC1}, V_{CC3}, V_{CC4}, V_{SS1}, and V_{SS3} are the power and ground for the logic area (+5 V ±5%). V_{SS1} and V_{SS3} are connected to ground. V_{CC2} and V_{SS2} are the power and ground for the internal VFO (+5 V ±5%). V_{SS2} is connected to ground.

CLK (Clock): CLK is the 16 MHz clock input (19.2 MHz for 150 and 300 kbps).

2.2.2 MPU Interface

$\overline{RESET}$ (Reset): $\overline{RESET}$ sets the $\overline{DREQ}$ and $\overline{IRQ}$ signals high and sets all the other output signals low. It forces D0-D7 into the input state.

E, $\overline{RD}$ (Enable, Read), R/$\overline{W}$, $\overline{WR}$ (Read/Write, Write): The functions of E, $\overline{RD}$ and R/$\overline{W}$, $\overline{WR}$ depend on the IFS input (table 2-2).

Table 2-2. E, $\overline{RD}$ and R/$\overline{W}$, $\overline{WR}$ Function

Signal	IFS		Function
E, $\overline{RD}$	0	$\overline{RD}$	Accepts the 80-series Read signal
	1	E	Accepts the 68-series Enable signal
R/$\overline{W}$, $\overline{WR}$	0	$\overline{WR}$	Accepts the 80-series Write signal
	1	R/$\overline{W}$	Accepts the 68-series Read/Write signal

$\overline{CS}$ (Chip Select): $\overline{CS}$ selects the chip and enables the read/write of the internal registers.

RS (Register Select): RS selects the internal register on which an MPU read/write is performed (table 2-3).

Table 2-3. RS Function

RS	Register Selected	Conditions
0	Status Register	Read
	Abort Register	Write
1	Data Register	Read/Write

D0-D7 (Data Bus): D0-D7 form the bidirectional 8-bit data bus, enabled by read/write.

$\overline{IRQ}$ (Interrupt Request): $\overline{IRQ}$ requests data transfer with the MPU in Non-DMA mode. It informs the MPU that a READ, WRITE, or SEEK command has been completed. When IFS is high, $\overline{IRQ}$ becomes an open drain output.

2.2.3 DMA Control

$\overline{DACK}$ (DMA Acknowledge): $\overline{DACK}$ receives the DMA acknowledge signal from the DMAC during a DMA transfer.

$\overline{DREQ}$ (DMA Request): $\overline{DREQ}$ requests the DMAC to perform a DMA transfer.

$\overline{DEND}$ (DMA End): $\overline{DEND}$ receives the DMA end signal from the DMAC and terminates the DMA transfer.

2.2.4 FDD Interface

RDATA (Read Data): RDATA inputs the read data signal from the FDD.

WGATE (Write Gate): WGATE outputs the write control signal to the FDD.

WDATA (Write Data): WDATA outputs the write data signal to the FDD.

LATE, EARLY (Late, Early): The LATE and EARLY output the write precompensation control signals used to advance or delay the write data before sending it to the FDD.

US1, US0 (Unit Select 1, 0): The US1 and US0 unit select outputs select the FDD. A maximum of 4 FDDs can be selected by decoding US1 and US0 (table 2-4).

Table 2-4 FDD Selection

US1	US0	FDD
0	0	FDD 0
0	1	FDD 1
1	0	FDD 2
1	1	FDD 3

INDEX (Index): INDEX inputs the index signal from the FDD.

TRK0 (Track 0): TRK0 inputs the track 00 signal from the FDD.

FAULT (Fault): FAULT inputs the fault signal from the FDD.

DSIDE (Double Sided): DSIDE inputs the double sided signal from the FDD.

WPRT (Write Protect): WPRT inputs the write protected signal from the FDD.

READY (Ready): READY inputs the ready signal from the FDD.

STEP (Step): The STEP output moves the FDD head.

HDIR (Head Direction): The HDIR output controls the direction of FDD head movement. HDIR = 0 indicates outward direction (towards track 0), while HDIR = 1 indicates inward direction.

HSEL (Head Select): The HSEL output selects the FDD head.
HSEL = 0 selects head 0, while HSEL = 1 selects head 1.

HLOAD (Head Load): The HLOAD output directs the FDD to load the heads onto the disk.

FRES (Fault Reset): The FRES output resets the FDD fault status FF.

LCT (Low Current): The LCT output reduces the FDD write current for inner tracks. After the SPECIFY 1 command is issued, the most outer position of the low current tracks is specified as track 43. For tracks $\geq$ this track, LCT = 1. A different most outer track position can be specified by the SPECIFY 2 command.

2.2.5 FDC Function Switching

SFORM (Select Format): The SFORM input selects the track format for formatting. SFORM high selects IBM format, SFORM low selects ECMA (ISO) format. SFORM is needed for formatting only. The FDC can read or write in either format regardless of the SFORM input level.

IFS (Interface Select): The IFS input specifies the host interface. IFS defines the functions of pins 8 and 9 (E, $\overline{RD}$ and R/$\overline{W}$, $\overline{WR}$) as shown in table 2-2. IFS = 0 for 80-series interface, IFS = 1 for 68-series interface.

8"/$\overline{5"}$ (8"/5" Mode Select): The 8"/$\overline{5"}$ input selects the FDD type. It specifies the drive data rate depending on the modulation method selected (table 2-5).

Table 2-5. Drive Data Rate

8"/$\overline{5"}$	FM	MFM
0	125 kbits/s	250 kbits/s
	150 kbits/s (Note)	300 kbits/s (Note)
1	250 kbits/s	500 kbits/s

Note: When CLK = 19.2 MHz

2.2.6 Others

NUM1, NUM2 (Not-User Mode 1, 2): NUM1 and NUM2 are not for user applications.

They must be tied to low.

<u>NC (No Connection)</u>: NC pins require no connection.

SECTION 3.   INTERNAL REGISTERS

3.1   INTERNAL REGISTER ACCESS

The host can access three registers: Data register (DTR), status register (STR), and abort register (ATR).   These registers are selected by the RS signal and read/write operations (table 3-1).

Table 3-1.   Register Selection

RS	Read/Write	Selected Register
0	Read	Status Register (STR)
	Write	Abort Register (ATR)
1	Read/Write	Data Register (DTR)

3.2   INTERNAL REGISTER FUNCTIONS

3.2.1   Status Register

The status register (figure 3-1) is a read-only register which indicates the FDC status and also whether each FDD selected by signals US0 and US1 is currently performing a seek or recalibrate operation.

STR								
Bit	7	6	5	4	3	2	1	0
Symbols	T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
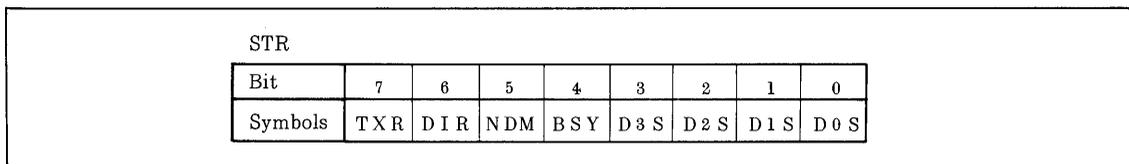
Figure 3-1.   Status Register

Bit 7   TXR (Transfer Ready): Bit 7 is set to 1 when DTR is in the read/write enabled state and it is cleared to 0 when data starts to be read or written by the host.

Bit 6   DIR (Data Direction): Bit 6 indicates the data transfer direction between the host and the FDC.

   DIR = 0: The host writes data to the FDC.

   DIR = 1: The host reads data from the FDC.

Bit 5   NDM (Non-DMA Mode): Bit 5 set to 1 indicates that the FDC transfers data in Non-DMA mode.   When Non-DMA mode is selected by commands SPECIFY 1 and SPECIFY 2, this bit is cleared to 0, except during the execution of read/write related commands.

Bit 4 BSY (Controller Busy): Bit 4 is set to 1 when the FDC cannot accept the next command because it is decoding or executing a command. A new command, except for the ABORT command, must be issued only when BSY = 0.

Bit 0-3 D0S-D3S (Drives 0-3 Seek): Bits 0-3 are set to 1 when the FDD selected by signals US0 and US1 is executing a SEEK or RECALIBRATE command. Bit 0 corresponds to FDD0 and bit 3 to FDD3. Bits D0S to D3S are 1's when the seek or recalibrate command is issued. Even if all of the step pulses are output, these bits stay as 1's until the SEEK and RECALIBRATE end status information is accepted by the CHECK INTERRUPT STATUS command.

3.2.2 Abort Register

Abort register is a write-only register used exclusively for the ABORT command.
ABORT command is issued by writing HEX FF into this register. This command is valid when the $\overline{\text{RESET}}$ signal is inactive regardless of the state of the FDC.
Values other than HEX FF written into this register are ignored by the FDC.

3.2.3 Data Register

Data register is a read/write register (actually a stack of registers with only one connected to the data bus at a time) which is used to receive commands and command parameters, transfer data, and read out result parameters.

This FDC can easily be interfaced to the 68- as well as the 80-series 8-bit devices.   IFS (pin 5) is used for selecting between 68-and 80-series interfaces.

4.1   68 SERIES INTERFACE (IFS = 1)

```
QFP     DIP
Pin 4  Pin 8:  E
Pin 5  Pin 9:  R/W̄
Pin 24 Pin 23 (ĪRQ):  Open-drain output
```

For the 68-series interface only, the data flow direction controlled by R/W̄ input (pin 9) is reversed between DMA and Non-DMA transfers (table 4-1). Here, DMA FDC access is by DĀCK̄ signal (pin 11), and Non-DMA FDC access is by C̄S̄ signal (pin 10).

Table 4-1.   Data Transfer 68-Series

Mode	DĀCK̄	C̄S̄	R/W̄	E	Data Transfer Direction	
DMA	0	1	0	1	FDC ⟶	Main memory
	0	1	1	1	Main memory ⟶	FDC
Non-	1	0	0	1	Host ⟶	FDC
DMA	1	0	1	1	FDC ⟶	Host

When the FDC is accessed by the DĀCK̄ signal, the RS signal (pin 12) is ignored, and DTR (data register) is always accessed.

4.2   80 SERIES INTERFACE (IFS = 0)

```
QFP     DIP
Pin 4  Pin 8   R̄D̄
Pin 5  Pin 9   W̄R̄
Pin 24 Pin 23 ĪRQ:  CMOS output the same as the other output pins
```

Table 4-2 shows the data transfer signals.

Table 4-2.   Data Transfer, 80-Series

Mode	DĀCK̄	C̄S̄	R̄D̄	W̄R̄	Data Transfer Direction	
DMA	0	1	1	0	Main memory ⟶	FDC
	0	1	0	1	FDC ⟶	Main memory
Non-	1	0	1	0	Host ⟶	FDC
DMA	1	0	0	1	FDC ⟶	Host

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During DMA transfer, in which the FDC is accessed by the $\overline{\text{DACK}}$ signal, the RS signal (pin 12) is ignored and DTR (data register) is always accessed.

SECTION 5.   DRIVE POLLING

This FDC performs drive polling every 1 ms (actually 1.024 ms) in 8" mode
and every 2 ms (2.048 ms) in 5" mode during command waiting.   During sleep
and head loading, no polling is performed.   Polling and seek operation
(step pulse output) are performed concurrently.
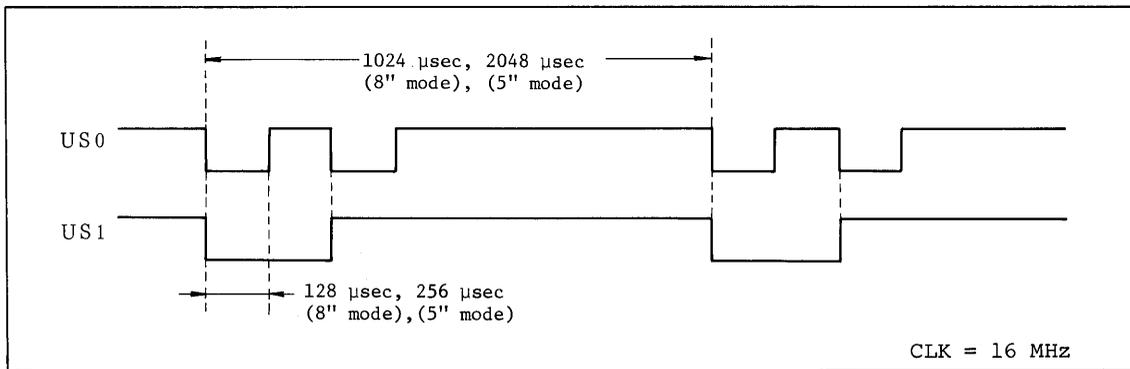
Figure 5-1.   Drive Selection Timing during Polling

US0 and US1 signals are changed (Figure 5-1) and the Ready signals of all
four drives are polled (Figure 5-2).   During this time, a step pulse is
issued to the drive requiring it (Figure 5-2).   When high speed seek mode is
specified using SPECIFY 2 command, 1 ms polling is performed even in 5" mode.
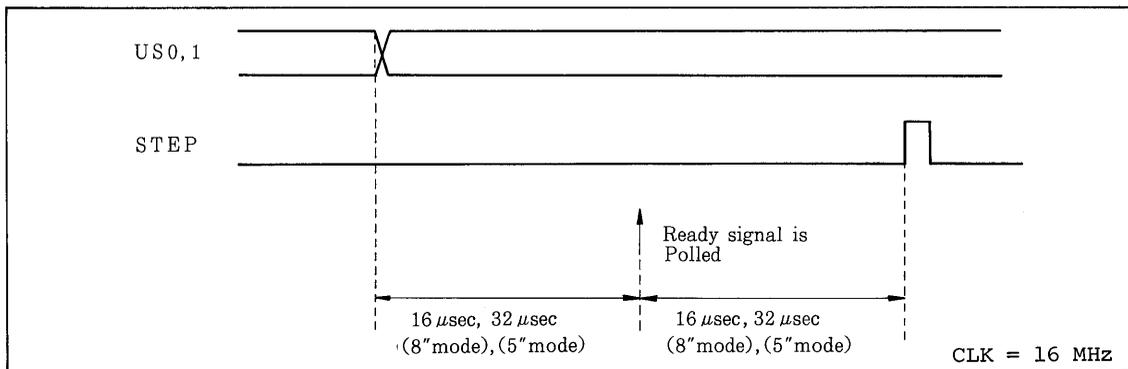

Figure 5-2.   Ready Signal Polling and Step Pulse Output Timing

During polling, if the ready signal level is inverted compared to the last time it was polled:

. INC (interrupt code) bits of SSB0 are set to CDS (Change in Drive Status) code,

. US1 and US0 bits of SSB0 are updated to the drive number whose ready signal is inverted, and

. $\overline{IRQ}$ signal is set active to request the host to issue CHECK INTERRUPT STATUS command.

Also, when a drive completes a seek operation, $\overline{IRQ}$ is set active to make a request for CHECK INTERRUPT STATUS command.

When a CHECK INTERRUPT STATUS command request source is accepted from the FDC by the CHECK INTERRUPT STATUS command, if there is no Seek-End status information in .the FDC, the next command request is not generated even if the Ready Signal Inversion status information is present.

However, when the CHECK INTERRUPT STATUS command is issued, the command is not treated as the INVALID command; the Ready Signal Inversion status information can be accepted. When Ready Signal Inversion is detected while the $\overline{IRQ}$ signal is inactive, the CHECK INTERRUPT STATUS command is requested by activating the $\overline{IRQ}$ signal.

FDC internal status	FDD0	READY inversion	—		
	FDD1	SEEK end		—	
	FDD2	READY inversion			—
	FDD3	—		READY inversion	—

$\overline{IRQ}$ does not become active⌐

┌ $\overline{IRQ}$ set by FDD3's READY inversion

$\overline{IRQ}$

CIS   FDD0 status return   CIS   FDD1 status return   CIS   FDD2 status return   CIS   FDD3 status return
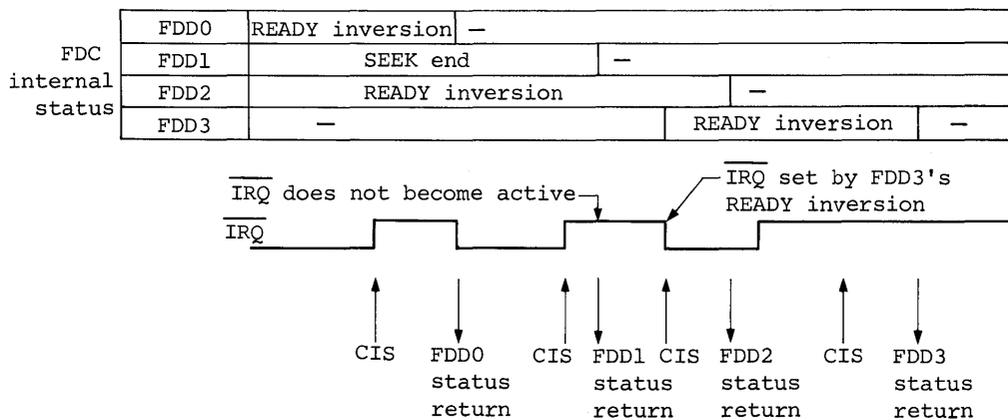
CIS: CHECK INTERRUPT STATUS command

If the FDC has statuses for more than one CIS command request, it returns FDD statuses to the host each time a CIS command is issued, starting at the lowest-numbered FDD's status.

6.1 COMMAND CODE LIST

Table 6-1 lists the FDC commands and the corresponding command codes.

Table 6-1. Command Codes

Commands	Command Codes							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
READ DATA	MT	MM	SD	0	0	1	1	0
READ DELETED DATA	MT	MM	SD	0	1	1	0	0
READ ERRONEOUS DATA	0	MM	0	0	0	0	1	0
READ ID	0	MM	0	0	1	0	1	0
WRITE DATA	MT	MM	0	0	0	1	0	1
WRITE DELETED DATA	MT	MM	0	0	1	0	0	1
WRITE FORMAT	0	MM	0	0	1	1	0	1
SEEK	0	0	0	0	1	1	1	1
RECALIBRATE	0	0	0	0	0	1	1	1
COMPARE EQUAL	MT	MM	SD	1	0	0	0	1
COMPARE LOW OR EQUAL	MT	MM	SD	1	1	0	0	1
COMPARE HIGH OR EQUAL	MT	MM	SD	1	1	1	0	1
CHECK DEVICE STATUS	0	0	0	0	0	1	0	0
CHECK INTERRUPT STATUS	0	0	0	0	1	0	0	0
SPECIFY 1	0	0	0	0	0	0	1	1
SPECIFY 2	0	A	H	0	1	0	1	1
SLEEP	0	0	0	0	1	1	1	0
ABORT	1	1	1	1	1	1	1	1
READ LONG	MT	MM	SD	1	0	0	1	0
WRITE LONG	MT	MM	0	1	0	1	1	0

MT: Multi Track

   MT = 1 specifies read/write of multi tracks.

MM: MFM Mode

   MM = 0 selects FM mode

   MM = 1 selects MFM mode

SD: Skip DDAM

   Sector with DDAM (deleted data address mark) is read or skipped depending

   on whether SD = 0 or 1. When SD = 1, the sector with DDAM is skipped.

A: Auto precompensation

   When A = 1, auto write precompensation is performed.

H: High speed seek

   H = 1 selects high speed seek mode.

6.2 COMMAND PARAMETERS

6.2.1 HSL-US: Head Select-Unit Select

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
×	×	×	×	×	H S L	U S 1	U S 0

× : Don't care

H S L : Head Select

U S 1 : Unit Select 1

U S 0 : Unit Select 0

Figure 6-1. Head Select-Unit Select

US0 and US1 bits (figure 6-1) specify the FDD that performs the command.
HSL specifies the read/write head to be used. When SEEK and RECALIBRATE
commands are issued, HSL has no meaning.


6.2.2 CA: Cylinder Address

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
←			Cylinder Address				→
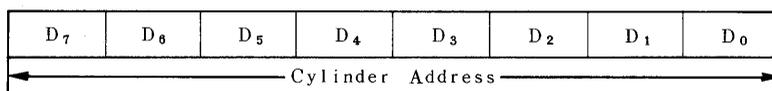
Figure 6-2. Cylinder Address

CA (figure 6-2) specifies a sector's or track's cylinder address.
CA range: 0 to 255

6.2.3 HA: Head Address

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	H A

Figure 6-3. Head Address

HA (figure 6-3) specifies a sector's or track's head address as 0 or 1.

6.2.4 SA: Sector Address

| D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
◄─────────────────────── Sector Address ───────────────────────►
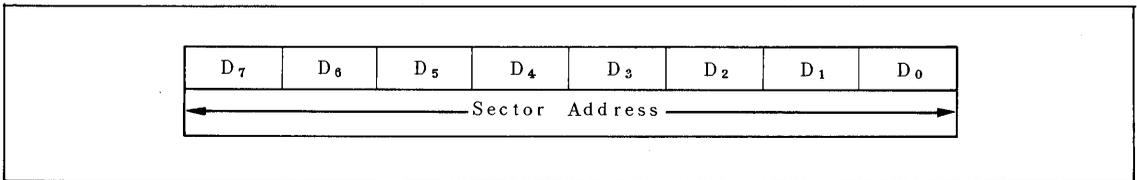
Figure 6-4. Sector Address

SA (Figure 6-4) specifies a sector's address (sector number).

SA range: 1 to 255

6.2.5 RL: Record Length

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	◄──── Record Length ────►
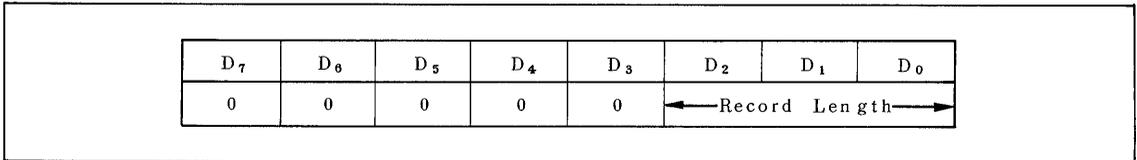
Figure 6-5. Record Length

RL (figure 6-5) specifies the sector length using a 3-bit binary code.

Using values 0 to 6, different sector lengths are specified as in table 6-2.

Table 6-2. Record Length

RL	Sector Length
0	128 Bytes/sector
1	256 Bytes/sector
2	512 Bytes/sector
3	1024 Bytes/sector
4	2048 Bytes/sector
5	4096 Bytes/sector
6	8192 Bytes/sector

6.2.6 ESN: End Sector Number

| D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
			End Sector Number				
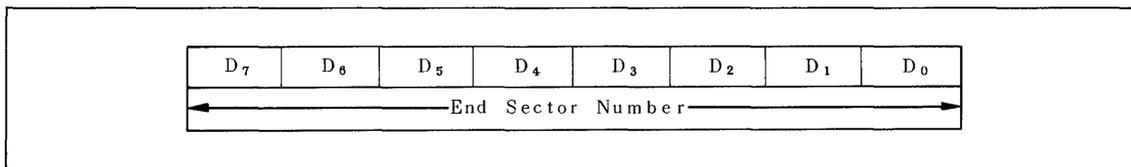
Figure 6-6. End Sector Number

ESN (figure 6-6) specifies the sector number of the last sector on the track. This number need not be the same as the actual (physical) last sector number. Read/Write access starts from the sector specified by SA, continues to and ends with the sector specified by ESN on the same track. However, if $\overline{DEND}$ signal is received during this time, the access terminates immediately. ESN range: 1 to 255. However, for COMPARE commands, the range is 1 to 253.

6.2.7 GSL: Gap Skip Length

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
			Gap Skip Length				
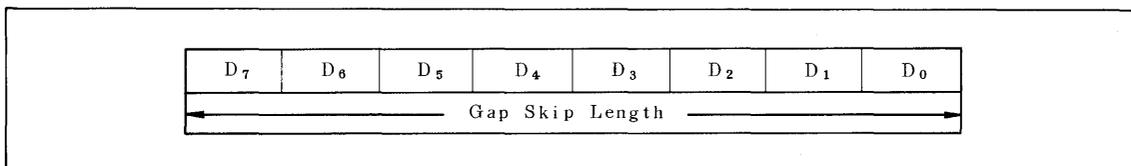
Figure 6-7. Gap Skip Length

GSL (figure 6-7) specifies the number of bytes skipped in between sectors as GAP3.

6.2.8 MNL: Meaning Length

| D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
			Meaning Length				
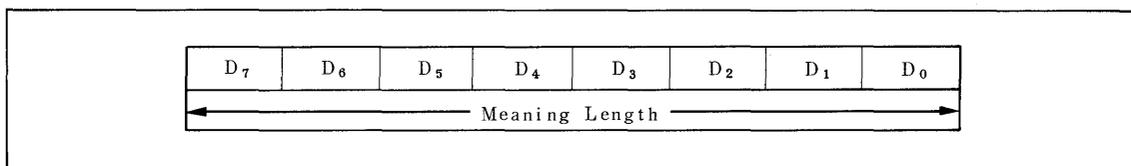
Figure 6-8. Meaning Length

To access part of a sector, MNL (Figure 6-8) specifies the byte count of data to be accessed. This function is valid only for sectors with RL = 0 (128 bytes/ sector).

Values from 0 to 255 can be set for MNL. If a value exceeding 128 (HEX 80) is specified, it is treated as 128, and the entire sector is accessed. When sectors with RL ≠ 0 are accessed, MNL has no effect.

6.2.9   SCNT: Sector Count

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
◄──────────────────── Sector Count ────────────────────►
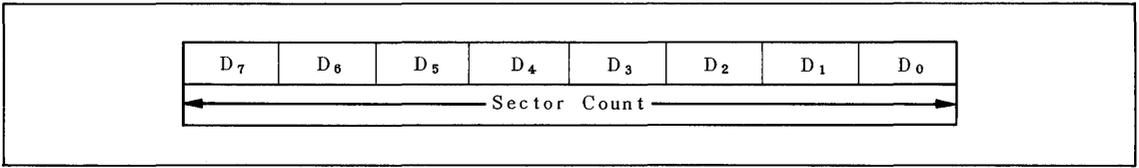
Figure 6-9.   Sector Count

SCNT (figure 6-9) specifies the sector count for formatting a track.

SCNT range: 1 to 255

6.2.10   GP3L: Gap 3 Length

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
◄──────────────────── Gap 3 Length ────────────────────►
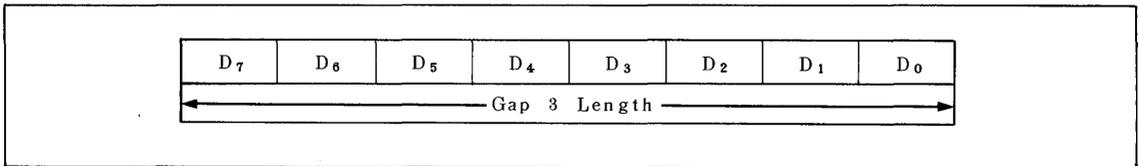
Figure 6-10.   Gap 3 Length

GP3L (figure 6-10) specifies in bytes the GAP3 length used in formatting a track.

GP3L range: 1 to 255

6.2.11   DUD: Dummy Data

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
◄──────────────────── Dummy Data ────────────────────►
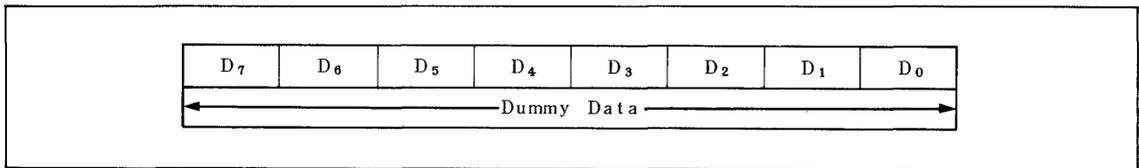
Figure 6-11.   Dummy Data

DUD (figure 6-11) specifies the dummy data pattern to be written into a sector's data area when formatting.

DUD range: 0 to 255

6.2.12   STEP: Step

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
0	0	0	0	0	0	S T E P	
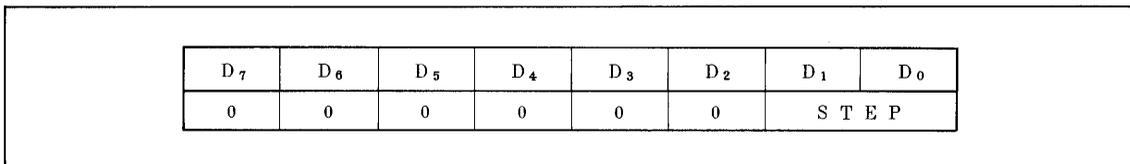
Figure 6-12.   Step

STEP (figure 6-12) specifies the sector increment for incrementing the sectors
whose data is to be compared byte-by-byte with the data sent from the host using
a COMPARE command.

   STEP = 1: Data from contiguous sectors is used for comparison.

   STEP = 2: Data from alternate sectors is used for comparison.

6.2.13   NCN: New Cylinder Number

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
←———————————— New Cylinder Number ————————————→							
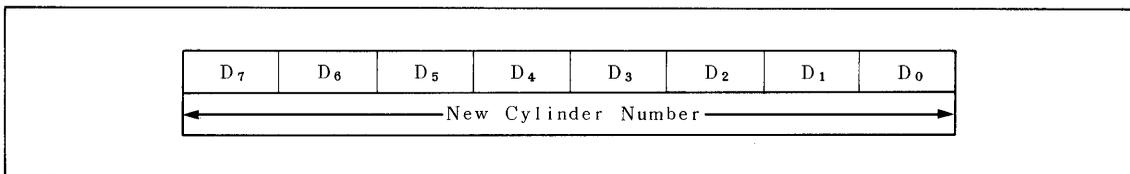
Figure 6-13.   New Cylinder Number

NCN (figure 6-13) specifies the cylinder number to which the head is to be moved.
NCN range: 0 to 255.

6.2.14   STR-HDUT: Stepping Rate-Head Unload Time

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
←———— Stepping Rate ————→				←—— Head Unload Time ——→			
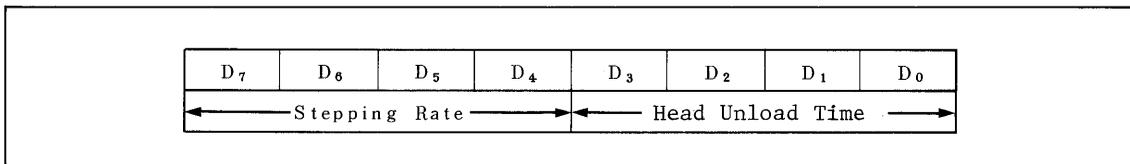
Figure 6-14.   Stepping Rate-Head Unload Time

STR-HDUT (figure 6-14) is a one-byte code in which the upper 4 bits represent
STR (stepping rate) and the lower 4 bits represent HDUT (head unload time).
STR: STR specifies the step pulse interval (stepping rate) for the seek and
recalibrate operations. Using values 1 to 15, different stepping rates are

specified as in table 6-3.

Table 6-3. Stepping Rates

Values (Decimal)	Stepping Rate (ms)	
	8"/$\overline{5"}$ = 1 or high-speed seek mode is selected	8"/$\overline{5"}$ = 0 and high-speed seek mode is not selected
0	16	32
1	15	30
2	14	28
3	13	26
4	12	24
5	11	22
6	10	20
7	9	18
8	8	16
9	7	14
10	6	12
11	5	10
12	4	8
13	3	6
14	2	4
15	1	2

CLK = 16 MHz

<u>HDUT</u>: HDUT specifies the time to wait from the completion of the head-load associated command execution before deactivating the head load signal. Using values 0 to 15, different head unload times are specified as in table 6-4.

Table 6-4.   Head Unload Times

Set Values	Head Unload Time (ms)	
(Decimal)	$8"/\overline{5"} = 1$	$8"/\overline{5"} = 0$
0	0	0
1	16	32
2	32	64
3	48	96
4	64	128
5	80	160
6	96	192
7	112	224
8	128	256
9	144	288
10	160	320
11	176	352
12	192	384
13	208	416
14	224	448
15	240	480

CLK = 16 MHz

6.2.15   HDLT-NDM: Head Load Time-Non-DMA Mode

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
←————————— Head Load Time —————————→							NDM
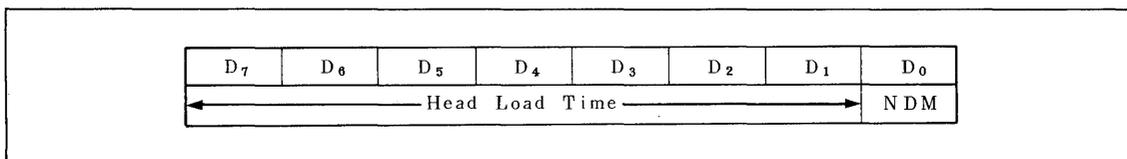
Figure 6-15.   Head Load Time-Non-DMA Mode

The upper 7 bits of HDLT-NDM (figure 6-15) denote HDLT (head load time) while the lowest bit denotes NDM (Non-DMA mode).

<u>HDLT</u>: HDLT specifies the time to wait from setting the head load signal active to start the command execution. When specifying HDLT, an allowance for head settle waiting time should be made also. Using values 0 to 127, different head load times are specified as in table 6-5.

Table 6-5. Head Load Times

Set Values (Decimal)	Head Load Time (ms)	
	8"/5" = 1	8"/5" = 0
0	0	0
1	2	4
2	4	8
3	6	12
4	8	16
5	10	20
6	12	24
7	14	28
8	16	32
↓	↓	↓
124	248	496
125	250	500
126	252	504
127	254	508

CLK = 16 MHz

NDM: NDM specifies if DMA or Non-DMA mode is used for transferring data between the FDC and the host.

NDM = 0: DMA mode

NDM = 1: Non-DMA mode

6.2.16   LCTK: Low Current Track

D $_7$	D $_6$	D $_5$	D $_4$	D $_3$	D $_2$	D $_1$	D $_0$
◄─────────────── Low Current Track ───────────────►							
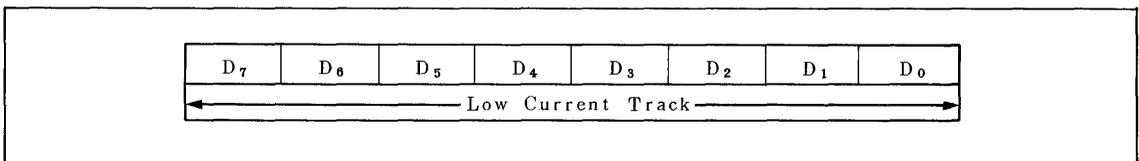
Figure 6-16.   Low Current Track

LCTK (figure 6-16) specifies the cross-over track number beyond which the LCT signal (pin 48) becomes active in SPECIFY2 mode. With LCTK set to a value ranging from 1 to 255, the LCT signal becomes active for tracks exceeding the LCTK value. With LCTK set to 0, the LCT signal is inactive at every track.

6.2.17 PC1, PC0: Precompensation Delay 1, 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
←	— P C 1 —	→	←	— P C 0 —	→		
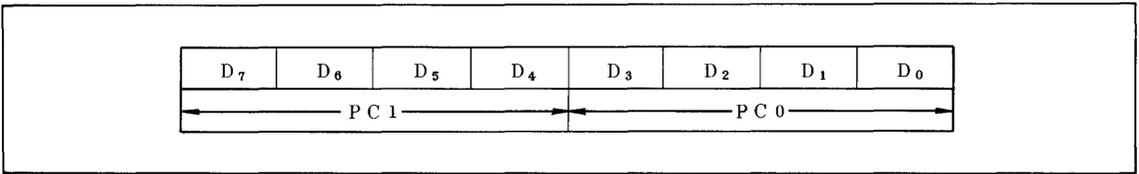
Figure 6-17. Precompensation Delay 1, 0

PC1 and PC0 (figure 6-17) specify the amount of precompensation delays for the auto precompensation mode (table 6-6). PC0 specifies the delay for the outer tracks (smaller track numbers) and PC1 specifies the delay for the inner tracks (larger track numbers). The FDC switches between PC0 and PC1 automatically depending on the head position. The switch-over track position is specified by PCDCT.

Maximum programmable values for PC1 and PC0 are

. HEX C in 5" mode

. HEX 6 in 8" mode

Values exceeding the above limits may cause malfunction.

Table 6-6. Precompensation Delay

PC1, PC0	Delay (ns)	
	CLK=16 MHz	CLK=19.2 MHz
HEX 0	0	0
HEX 1	62.5	52.1
HEX 2	125	104.2
|	|	|
HEX 6	375	312.5
|	|	|
HEX B	687.5	572.9
HEX C	750	625

6.2.18 PCDCT: Precompensation Delay Change Track

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
←			P C D C T				→
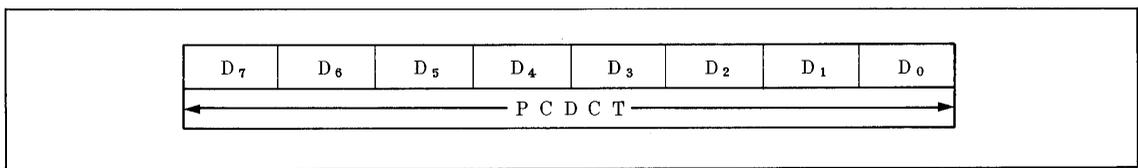
Figure 6-18.   Precompensation Delay Change Track

PCDCT (figure 6-18) specifies the track where the precompensation delay amount is changed in the auto precompensation mode.   For tracks with a number equal to or larger than PCDCT, the delay amount is specified by PC1, and for tracks with a smaller number, the delay is specified by PC0.

PCDCT range: 1 to 255

6.3   RESULT PARAMETERS

6.3.1   CA, HA, SA, and RL: Cylinder Address, Head Address, Sector Address, Record Length

CA, HA, SA, and RL are provided as command execution results and their values depend on the command type and how the command execution ended, with or without errors.   See section 6.5, "Command Functions".

6.3.2   SSB0: Sense Status Byte 0

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
I N C		S E D	D E R	D N R	H S L	U S 1	U S 0
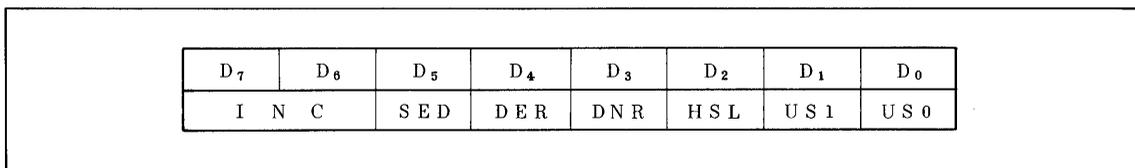
Figure 6-19.   Sense Status Byte 0

INC (Interrupt Code): INC (figure 6-19) indicates the cause of an interrupt request (table 6-7).

Table 6-7. Interrupt Code

D7	D6	Code Symbol	Code Name	Meaning
0	0	NOR	Normal End	Command normally ended
0	1	ABE	Abnormal End	Command abnormally ended
1	0	IVC	Invalid Command	Issued command is invalid
1	1	CDS	Change in Drive Status	Ready signal level from a drive is inverted compared to the last time it was polled

SED (Seek End): SED is set to 1 at the completion of SEEK and RECALIBRATE commands.

DER (Drive Error): DER is set to 1 when the fault signal is active during or at the completion of write related command execution, and when the track 0 signal cannot be detected from a drive to which 255 step pulses were applied during a RECALIBRATE command execution.

DNR (Drive Not Ready): DNR is set to 1 when a low level ready signal is detected from a drive at the start of or during the execution of drive access commands other than the CHECK DEVICE STATUS command.

HSL (Head Select): HSL indicates the head selected at the completion of command execution. In response to the CHECK INTERRUPT STATUS command, a zero is returned.

US1, US0 (Unit Select 1, 0): US1 and US0 indicate the drive number selected at the completion of a command execution or the one that caused an interrupt request.

6.3.3 SSB1: Sense Status Byte 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
NDE	0	CER	DOR	0	INF	WPM	ANF

Figure 6-20. Sense Status Byte 1

NDE (No DMA End): NDE (figure 6-20) is set to 1 if the $\overline{DEND}$ signal is not received active even after the last sector data has been transferred with a read/write related command. The last sector is determined depending on the MT (multi track) bit value as follows:

. MT = 0: The last sector is specified by the ESN (end sector number) byte on the track of the side specified as part of the command parameters.

. MT = 1: The last sector is specified by the ESN byte but always corresponds to the track on side 1.

CER (CRC Error): CER is set to 1 when a CRC error is detected in the ID or data field. READ ID command does not have any effect on this bit. For CRC errors in the ID field, only the CER bit is set to 1. For CRC errors in the data field, the CDF bit of SSB2 as well as the CER bit are set to 1.

DOR (Data Overrun): DOR is set to 1 if the host cannot complete data transfer requested by the FDC within a specified time to satisfy the FDC data throughput requirements. For details, see section 6.5, "Command Functions".

INF (ID Not Found): The meaning of INF depends on its context.

1. In READ DATA, READ DELETED DATA, READ LONG, WRITE DATA, WRITE DELETED DATA, WRITE LONG, and COMPARE commands: INF is set to 1 if the sector number (CA, HA, SA, RL) specified by a command parameter or updated during a multisector read/write operation cannot be found by the time three index pulses are detected.

2. In READ ID command: INF is set to 1 when an address mark in the ID field was detected but a CRC error-free ID was not found by the time three index pulses were detected.

3. In READ ERRONEOUS DATA command: INF is set to 1 if ID data in the FDC does not match the ID found.

WPM (Write Protected Medium): WPM is set to 1 when an active write protected signal is detected at the start of write related command execution.

ANF (AM Not Found): ANF is set to 1 if no ID address mark is detected by the time three index pulses are detected. ANF as well as the NAM bit of SSB2 are set to 1 when no address mark (data address mark or deleted data address mark) is detected in the data field within 1 ms after the desired ID was found, or when the first data other than HEX 00 found after the desired ID and at least 4 bytes (FM mode) or 5 bytes (MFM mode) of HEX 00 were detected is not AM.

6.3.4 SSB2: Sense Status Byte 2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	DDA	CDF	CAU	CCS	CNS	BDC	NAM

Figure 6-21. Sense Status Byte 2

DDA (Deleted Data Address Mark): DDA (figure 6-21) is set to 1 when a deleted data address mark is detected. In executing the READ DELETED DATA command, however, it is set to 1 when a normal data address mark is detected.

CDF (CRC Error in Data Field): CDF is set to 1 if a CRC error is detected in the data field.

CAU (Cylinder Address Unmatch): CAU is set to 1 when the disk ID's CA byte does not match the command parameter's CA byte, except when the disk ID's CA byte is HEX FF. However, CAU is not set by the READ ERRONEOUS DATA command.

CCS (Compare Condition Satisfied): CCS is set to 1 when the equal condition is satisfied while executing a COMPARE command.

CNS (Compare Condition Not Satisfied): CNS is set to 1 when the specified compare condition is not satisfied while executing a COMPARE command.

BDC (Bad Cylinder): BDC is set to 1 when the CA byte read from the disk does not match the command parameter's CA byte and also when the read CA byte is HEX FF. However, BDC is not set by the READ ERRONEOUS DATA command.

NAM (No Data Address Mark): NAM is set to 1 if no address mark (data address mark or deleted data address mark) is detected in the data field within 1 ms after the desired ID was found, or when the first data other than HEX 00 found after the desired ID and at least 4 bytes (FM mode) or 5 bytes (MFM mode) of HEX 00 were detected is not AM.

6.3.5 SSB3: Sense Status Byte 3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
FLT	WPT	RDY	TRZ	DSD	HSL	US1	US0

FLT : Fault   DSD : Double Sided
WPT : Write Protected   HSL : Head Select
RDY : Ready   US1 : Unit Select 1
TRZ : Track 0   US0 : Unit Select 0

Figure 6-22. Sense Status Byte 3

1) FLT, WPT, RDY, TRZ, and DSD: Sense bits FLT, WPT, RDY, TRZ, and DSD indicate the status of the drive specified in the CHECK DEVICE STATUS command.

2) HSL, US1, and US0: Sense bits HSL, US1, and US0 have the same values as HSL, US1, and US0 of the command parameters.

6.3.6 PCN: Physical Cylinder Number

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
←——————————— Physical Cylinder Number ———————————→							

Figure 6-23. Physical Cylinder Number

PCN (figure 6-23) represents the physical address of the drive head position
stored in the FDC (physical number of the track where a head is currently
placed). If a SEEK or RECALIBRATE command ends abnormally, the PCN value may
not match the head's current physical address. When the FDC is reset, the
PCN values for all four drives are set to HEX 00. Accordingly, drives with
an auto-recalibrate function (a function which automatically moves the heads
onto track 0 at power on) do not require the RECALIBRATE command to be
issued after the power on reset. The lower two bits of SSB0 read last
indicate which drive the PCN value belongs to.

6.4 ISSUING COMMANDS

6.4.1 Writing Command Codes

Commands can be issued by writing the desired command codes into the FDC. The
status register must be read before issuing a command.

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	0	0	0	×	×	×	×

Figure 6-24. Status Register Before Issuing a Command

The FDC is ready to accept commands when the status register bits are as shown
in figure 6-24.
When any of the D0S to D3S bits are set to 1:
1. CHECK DEVICE STATUS command and CHECK INTERRUPT STATUS command can be
    issued for all four drives. However, CHECK INTERRUPT STATUS command is
    treated as an invalid command when the FDC has no SEEK end and no READY
    inversion status.
2. SEEK and RECALIBRATE commands can be issued only for drives whose corres-
    ponding D0S to D3S bits are zeros.

Commands other than CHECK related and SEEK related commands can be issued when the status register value equals HEX 80.

An ABORT command can be issued independent of the status register value. When a command code is written, the status register is set as shown in figure 6-25 and the FDC begins to decode the command.

If the Data Register is read in the command waiting state, the FDC will malfunction since the FDC considers it as a command issue. So, during command waiting state, do not attempt to read the Data Register.

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
0	0	0	1	×	×	×	×

Figure 6-25. Status Register After Issuing a Command

6.4.2 Writing Command Parameters

At the completion of command code decoding, for commands requiring command parameters, the FDC sets the status register as shown in figure 6-26 and wait for command parameters.

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	0	0	1	×	×	×	×

Figure 6-26. Status Register Waiting for Command Parameters

TXR bit is cleared to zero every time a command parameter byte is received. When the FDC is ready to receive the next command parameter byte the TXR bit is again set to one and the next byte is transferred. After all the command parameter bytes have been received, no more transfer requests are made.

6.4.3 Transferring Data

Data transfer is performed during command execution in response to an FDC request. Data transfer requests are made by setting the $\overline{IRQ}$ signal active in Non-DMA mode or the $\overline{DREQ}$ signal active in DMA mode. Status register contents for both types of data transfer requests are shown in figure 6-27.

Read request in Non-DMA mode

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	1	1	1	0	0	0	0

Write request in Non-DMA mode

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	0	1	1	0	0	0	0

Read request in DMA mode

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	1	0	1	0	0	0	0

Write request in DMA mode

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	0	0	1	0	0	0	0

Figure 6-27. Status Register Contents for Various Data Transfer Requests

6.4.4 Transferring Result Status

For commands having a result status, the FDC requests the host to accept the
result parameter bytes at the completion of the command execution. Commands
which have no result status are SEEK, RECALIBRATE, SPECIFY1, SPECIFY2, SLEEP,
and ABORT. Commands which cause the status register to be set up as shown in
figure 6-28 and request the host to accept the result parameters are: CHECK
DEVICE STATUS, CHECK INTERRUPT STATUS, and INVALID.

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	1	0	1	×	×	×	×

Figure 6-28. Status Register Requesting Result Parameter Transfer (No $\overline{\text{IRQ}}$)

The above commands do not activate the $\overline{\text{IRQ}}$ signal in order to transfer the result parameters.

After one byte of the result parameters has been transferred, TXR and DIR are cleared to zero. When the next byte of the result parameters is ready to be transferred, it is loaded into the data register. Then both the DIR and TXR bits of the status register are set to 1 requesting the host to accept the new parameter byte. After the last byte of the result parameters has been transferred, some dummy data is loaded into the data register, TXR is set to 1 and BSY is cleared to 0 to enter the command waiting state (DIR remains zero). For all the other commands, the result status transfer is performed by setting the $\overline{\text{IRQ}}$ signal active and the status register as shown in figure 6-29. The $\overline{\text{IRQ}}$ signal is active only when the first byte of the result parameters is transferred, and becomes inactive after that.

T X R	D I R	N D M	B S Y	D 3 S	D 2 S	D 1 S	D 0 S
1	1	0	1	0	0	0	0

Figure 6-29.   Status Register Requesting Result Parameter Transfer (with $\overline{\text{IRQ}}$)

The first byte of the result parameters is transferred according to the following sequence of operations.
. $\overline{\text{IRQ}}$ signal is set active
. DIR bit is set to 1
. Result parameter byte is loaded into the data register
. TXR bit is set to 1
. FDC waits for the result parameter byte to be transferred
. Host reads the result parameter byte and TXR bit is reset to 0.
. DIR bit is reset to 0.
. $\overline{\text{IRQ}}$ signal is set inactive.

The remaining bytes are transferred in the same way except that the $\overline{\text{IRQ}}$ signal is not activated again. After the last byte of the result parameters is transferred, some dummy data is loaded into the data register, TXR is set to 1 and BSY is cleared to 0 to enter the command waiting state (DIR remains zero).

```
        ╭─────────────────╮
        │    Power on      │
        ╰─────────────────╯
                 │
                 ▼
        ┌─────────────────┐
        │   Reset FDC      │        Input low level to R̄E̅S̅E̅T̅ pin
        └─────────────────┘
                 │
                 ▼
        ┌─────────────────┐
        │   Issue          │
        │   SPECIFY         │        SPECIFY 1 or SPECIFY 2 command
        │   command         │
        └─────────────────┘
                 │
                 ▼
        ┌─────────────────┐
        │   Issue          │
        │   RECALIBRATE     │        Move FDD's heads to track 0
        │   command         │
        └─────────────────┘
                 │
                 ▼
        ┌─────────────────┐
        │   Issue          │
        │   CHECK           │
        │   INTERRUPT       │        Correctly end the RECALIBRATE command
        │   STATUS          │
        │   command         │
        └─────────────────┘
                 │
                 ▼
        ╭─────────────────╮
        │    Next          │
        │    process       │
        ╰─────────────────╯
```
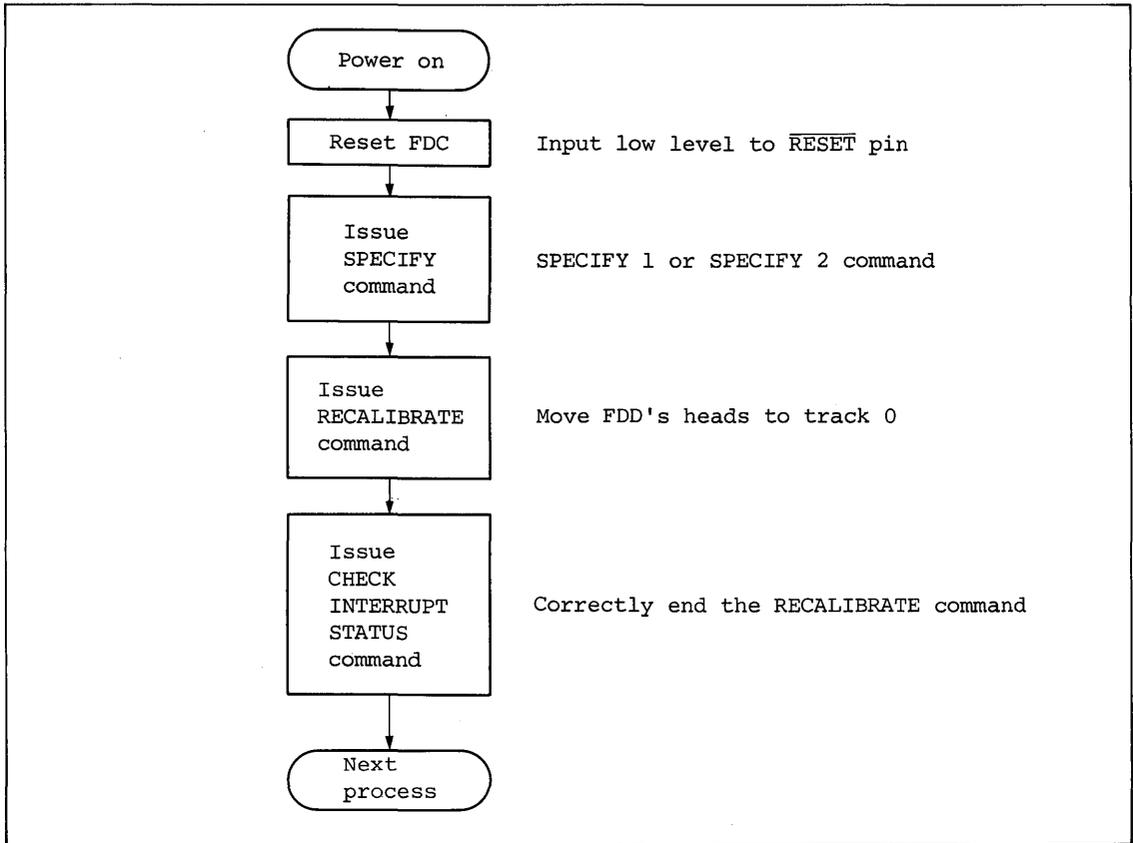
Figure 6-30. FDC Initial Setup Flowchart
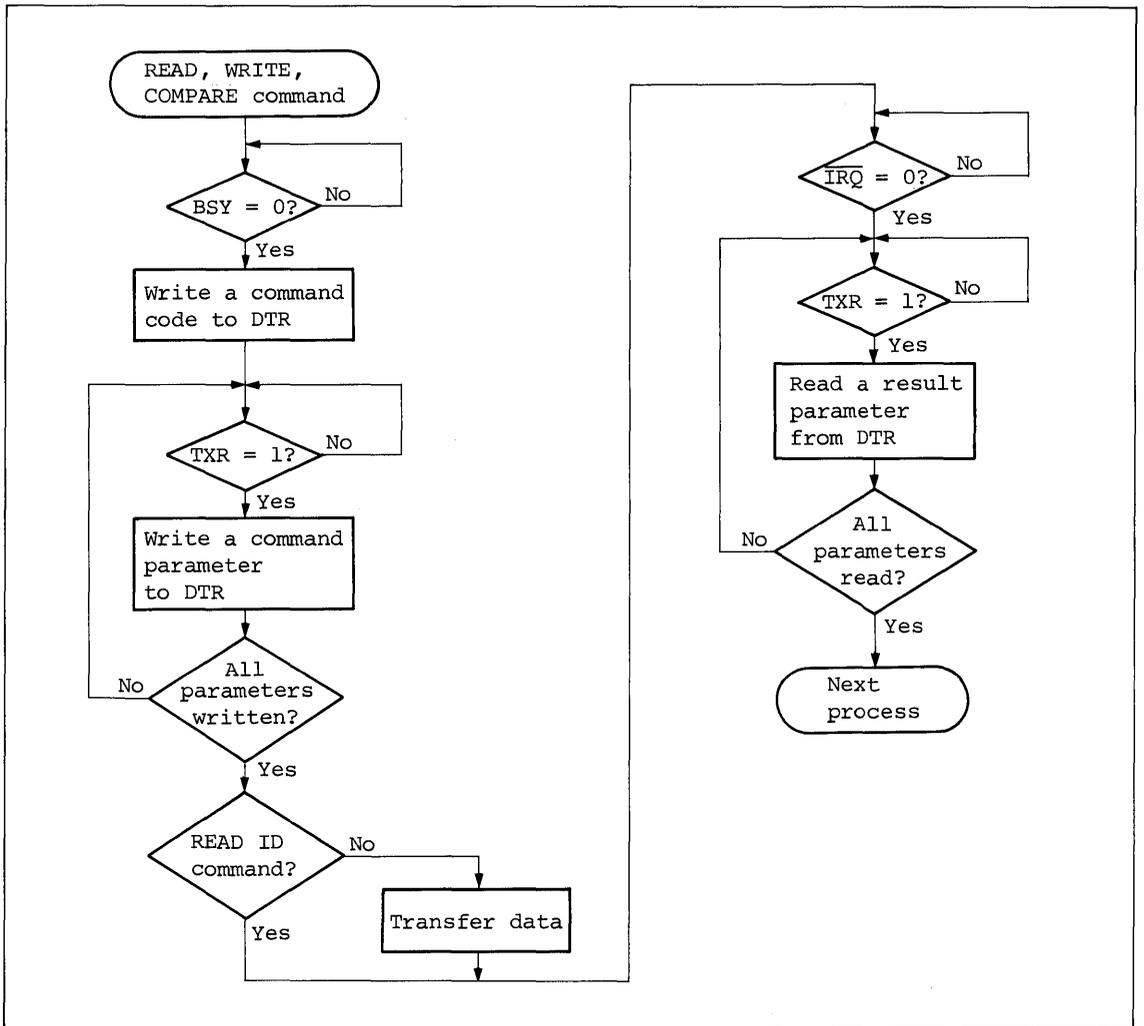
Figure 6-31. READ, WRITE, COMPARE Command Execution Flowchart
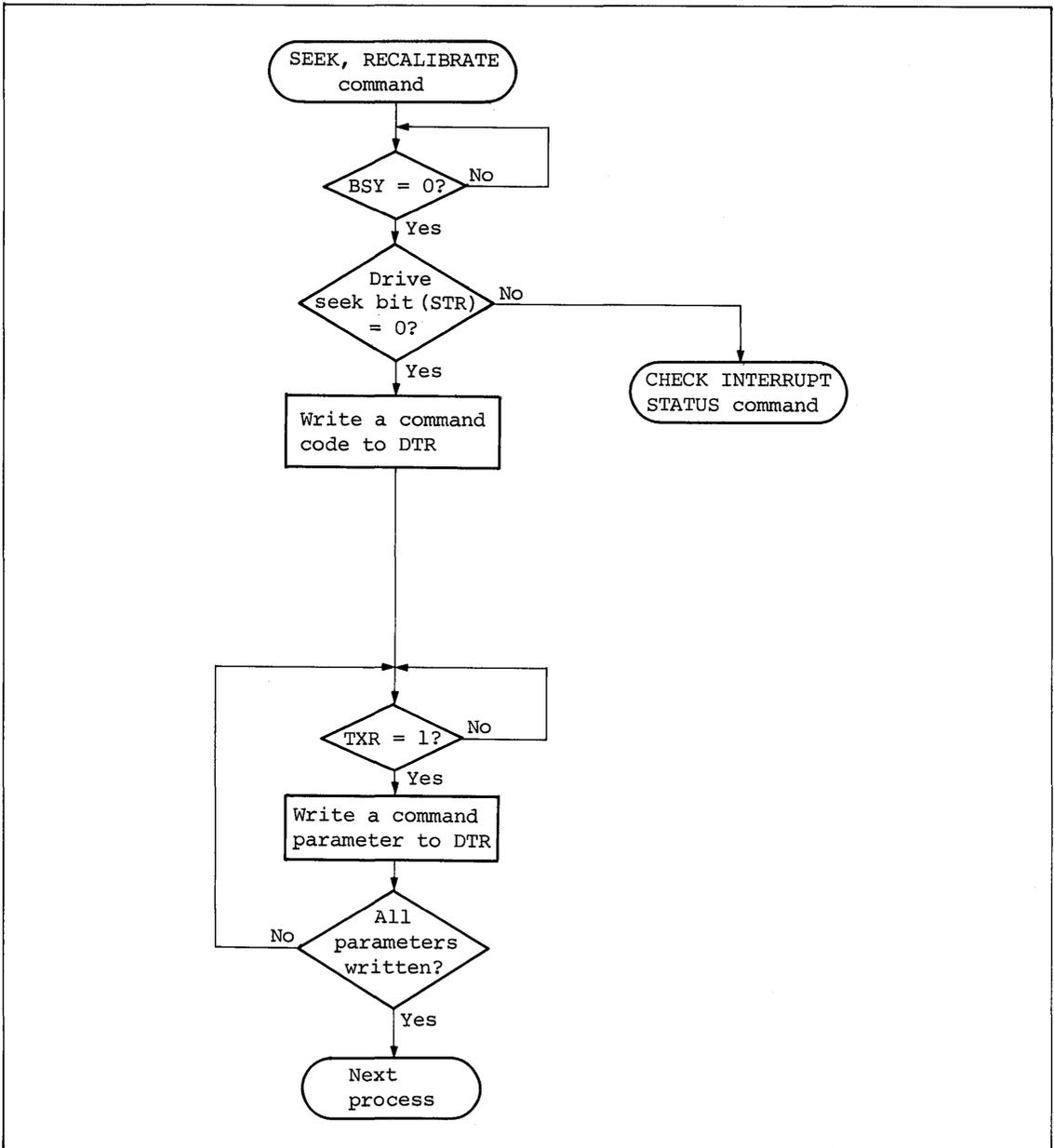
Figure 6-32.   SEEK, RECALIBRATE Command Execution Flowchart
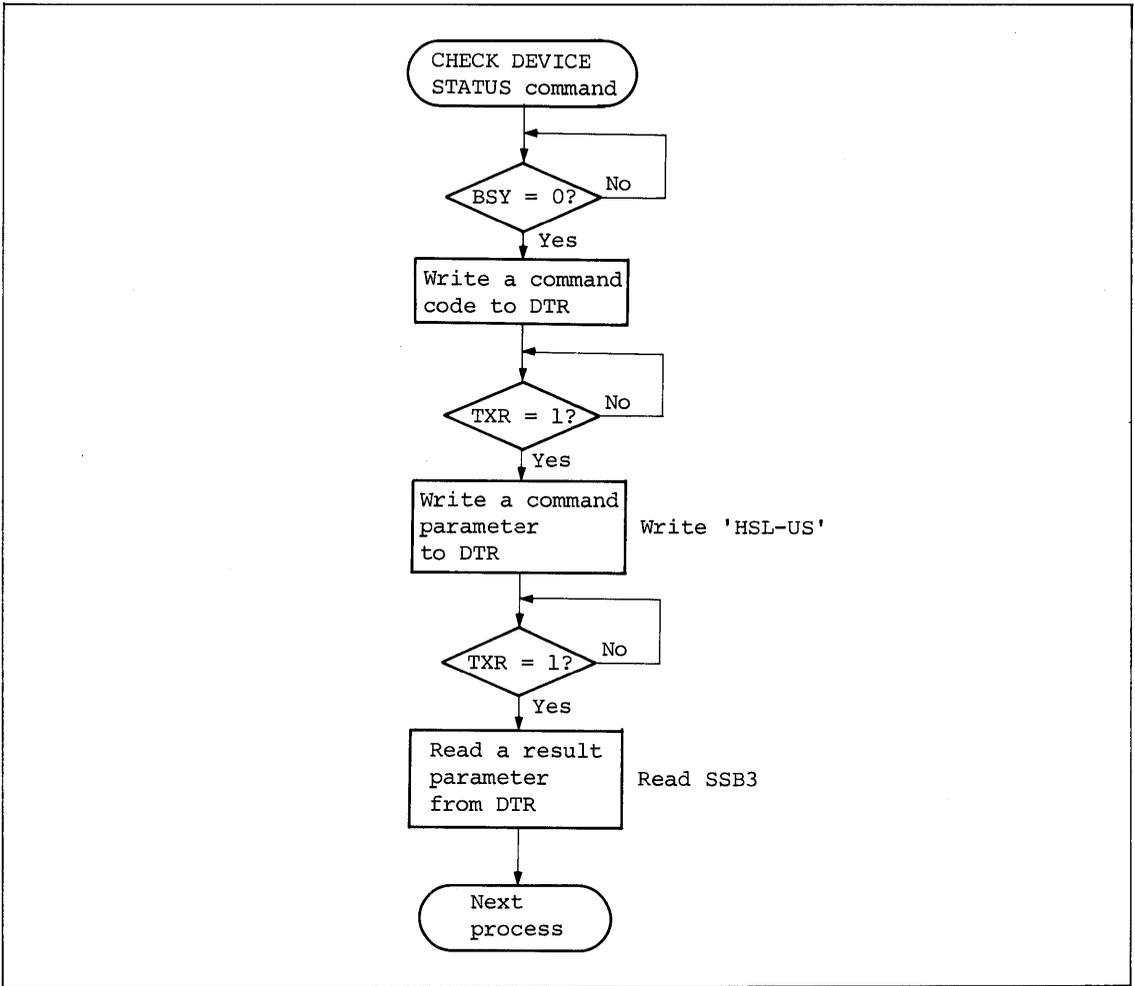
Figure 6-33. CHECK DEVICE STATUS Command Execution Flowchart
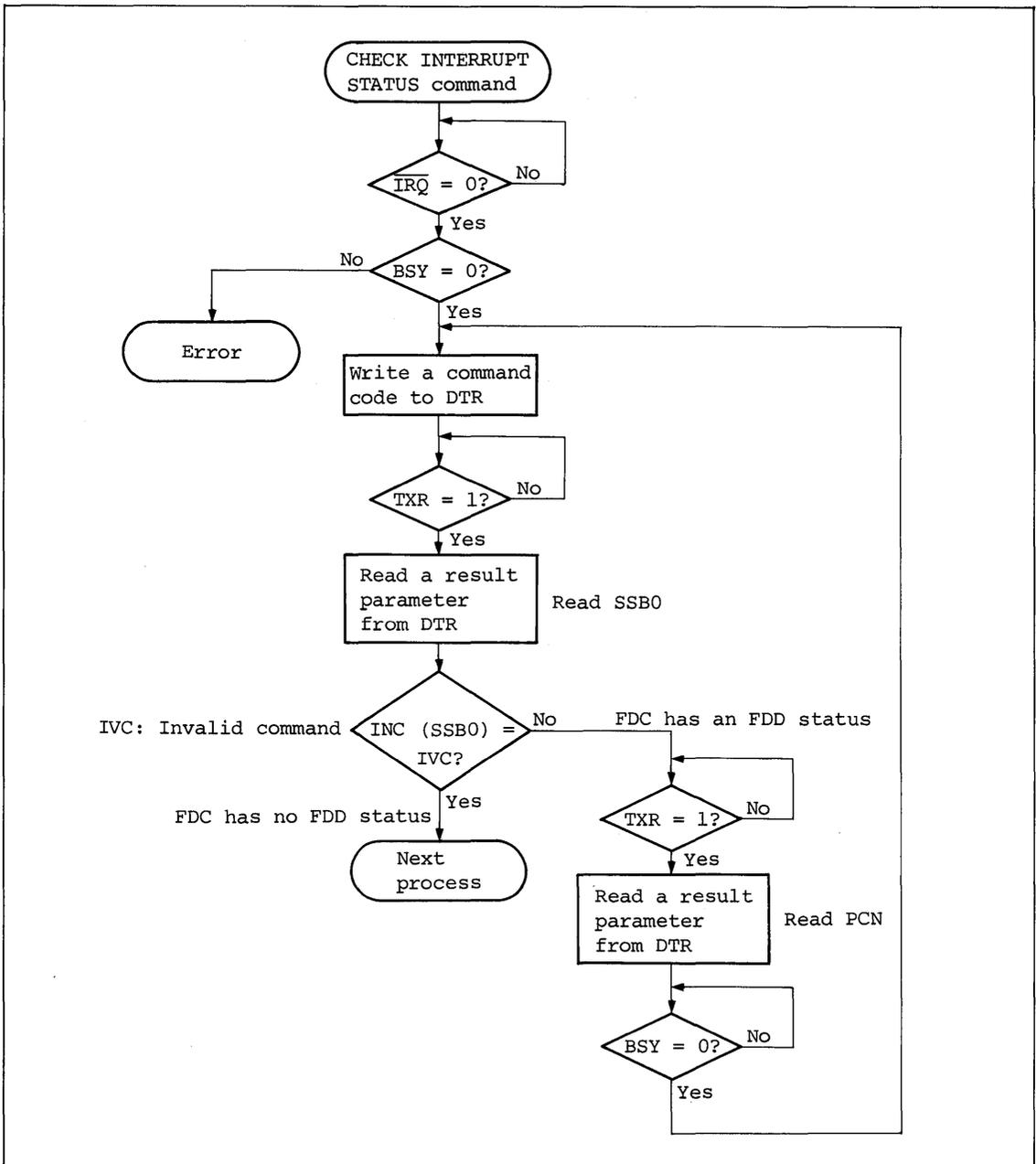
Figure 6-34. CHECK INTERRUPT STATUS Command Execution Flowchart
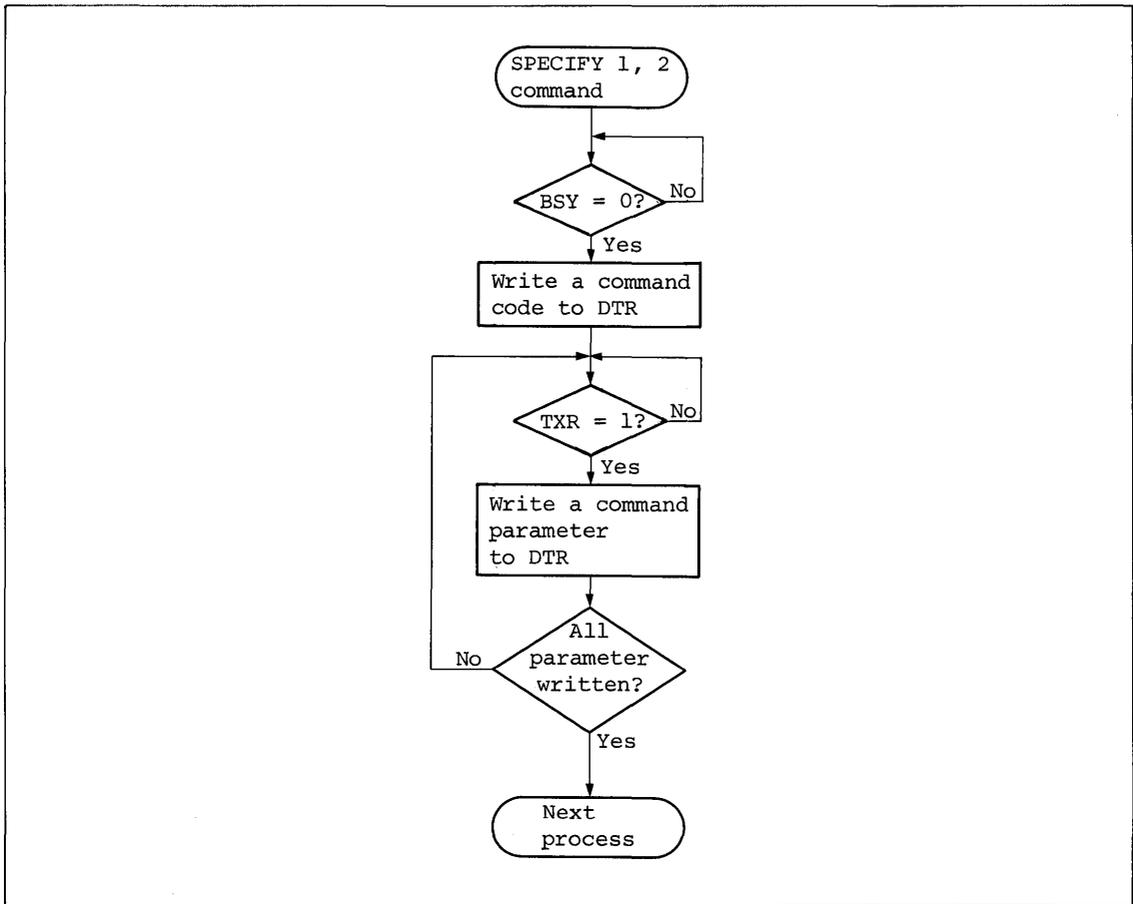
Figure 6-35. SPECIFY 1, SPECIFY 2 Command Execution Flowchart
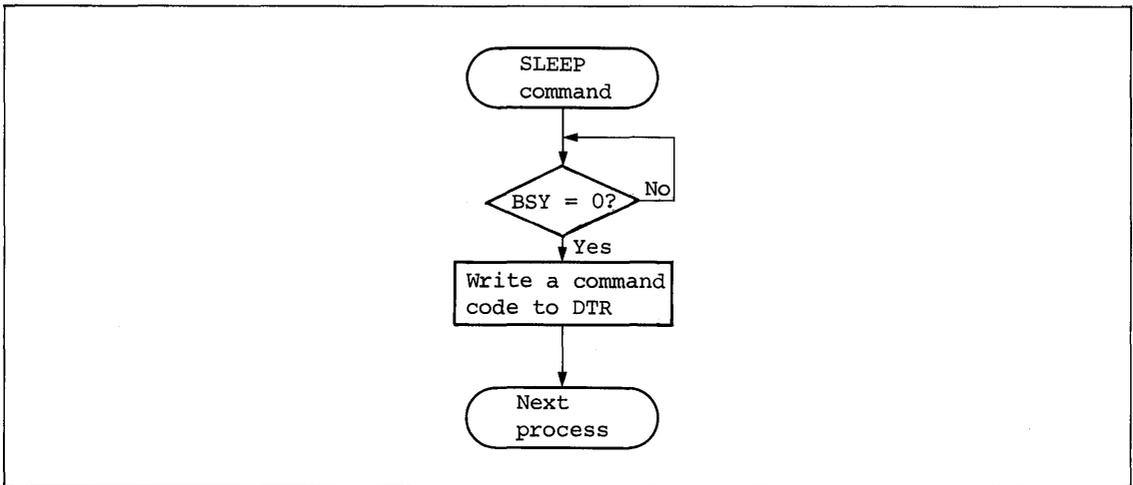
Figure 6-36.   SLEEP Command Issue Flowchart
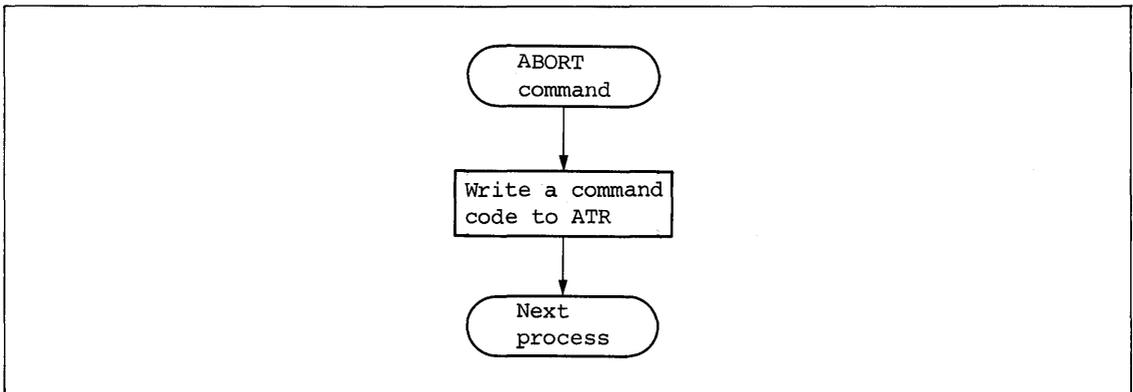
Figure 6-37.   ABORT Command Issue Flowchart

6.5 COMMAND FUNCTIONS

6.5.1 READ DATA

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	M T	M M	S D	0	0	1	1	0
Command Parameters	×	×	×	×	×	H S L	U S 1	U S 0
	C A							
	H A							
	S A							
	R L							
	E S N							
	G S L							
	M N L							
Result Parameters	S S B 0							
	S S B 1							
	S S B 2							
	C A							
	H A							
	S A							
	R L							
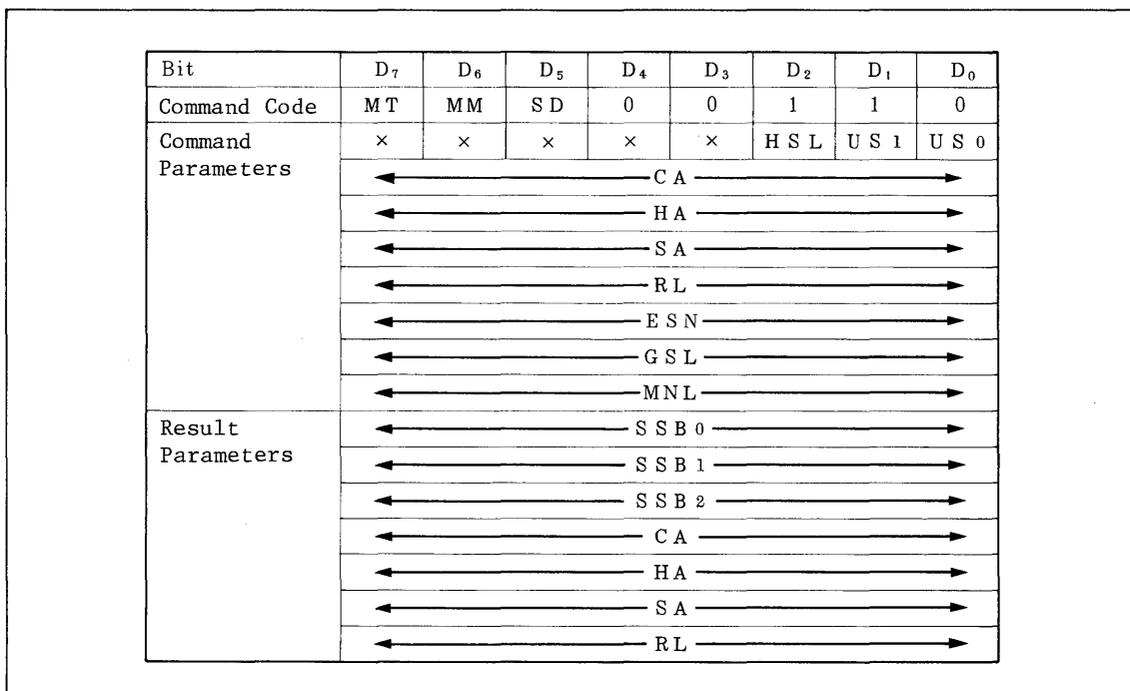
Figure 6-38. READ DATA Command

The READ DATA command (figure 6-38) transfers data to the host from the disk. The command parameters specify the location of the data on the disk. Multi-sector read is automatically performed. Multitrack read can also be performed if specified.

Selection of Unit and Head: When the command execution begins, a unit (drive) and a head are selected according to the command parameters.

Ready Check: The ready signal from the drive is checked after waiting for more than 3 µs following the drive selection. If the drive is not ready, the DNR (drive not ready) bit of SSB0 is set and the command execution is abnormally terminated. The ready check is also performed during an ID search.

Head Load: If the heads of a selected drive are not already loaded, they are automatically loaded on the disk and the command is executed after waiting for the head load time specified by the SPECIFY command. If the heads are already loaded, the FDC does not wait for the head load time.

ID Search: The FDC searches for the ID specified in the command parameters. If an ID different from the specified ID is found, a CRC check is performed for

the ID.   If the ID address mark cannot be found by the time three index pulses are detected, the ANF (AM not found) bit of SSB1 is set and the command execution is abnormally terminated.   Even after an ID address mark is found, if the specified ID cannot be found by the time three index pulses are detected, the INF (ID not found) bit of SSB1 is set and the command execution is abnormally terminated.   If the found ID's CA (cylinder address) byte does not match the desired ID's CA byte, the result parameters are set as follows depending on the contents of the command parameter CA byte.

. The loaded CA = HEX FF: BDC (bad cylinder) bit of SSB2 as well as the INF bit are set and the command execution is abnormally terminated.

. The loaded CA ≠ HEX FF: CAU (cylinder address unmatch) bit of SSB2 as well as the INF bit are set and the command execution is abnormally terminated.

CRC Check: CRC check is performed every time an ID and data are read.

When a CRC error is detected in an ID field, the CER (CRC error) bit of SSB1 is set and the command execution is abnormally terminated.

When a CRC error is detected in a data field, the CDF (CRC error in data field) bit of SSB2 as well as the CER bit of SSB1 are set and the command execution is abnormally terminated.

Detection of Data Address Mark: The NAM (no data address mark) bit of SSB2 as well as the ANF (AM not found) bit of SSB1 are set and the command execution is abnormally terminated in the following two conditions: a data address mark is not found within 1 ms after a CRC check on the specified read ID, or the first data other than HEX 00 found after the desired ID and at least 4 bytes (FM mode) or 5 bytes (MFM mode) of HEX 00 were detected is not AM.

Detection of Deleted Data Address Mark: When a deleted data address mark (data address mark: HEX FB   deleted data address mark: HEX F8) is detected, the DDA (deleted data address mark) bit of SSB2 is set.   If the SD (skip DDAM) bit of the command code is 0, the data in the sector is transmitted and the command execution is normally terminated.   If the SD bit is 1, the data in the sector is skipped (not transmitted, not CRC checked in the data field) and the FDC starts to process the next sector.

Data Transmission: The FDC requests the host to accept the data read from a disk in one of two ways depending on the NDM bit of the SPECIFY command. Data transmission is requested by the $\overline{\text{DREQ}}$ signal in DMA mode or by the $\overline{\text{IRQ}}$ signal in Non-DMA mode.   If the host does not access the data in the data

register within the periods shown in table 6-8 after the data transmission request, the DOR (data overrun) bit of SSB1 is set, a CRC check is performed on the sector data read and the command is abnormally terminated.

Table 6-8. Read Data Transfer Request Wait Times

8"/5" (pin 6)	FM mode	MFM mode
Low	54 μs	22 μs
High	27 μs	11 μs

Multisector/Multitrack Read: If the $\overline{\text{DEND}}$ signal is not received even after the last byte of a sector has been transmitted to the host, SA is incremented and the FDC starts to process the next sector (multisector read).
However, if SA of the processed sector is ESN, the following operations are performed depending on the Head Address HA and the MT bit of the command code.

. MT bit = 1 and HA = HEX 00: SA and HA are set to HEX 01 and a multitrack read is performed.

. MT bit = 0 or HA = HEX 01: The NDE (No DMA end) bit of SSB1 is set and the command execution is abnormally terminated.

When the $\overline{\text{DEND}}$ signal is received in the middle of a sector data transfer, the data transmission to the host stops immediately. However, the rest of the sector data is read from the drive and its CRC bytes are checked. If there exists no CRC error, the command execution is terminated normally. Also, when the $\overline{\text{DEND}}$ signal is received during the transmission of the last byte of a sector, access of the next sector is not performed and the command execution is terminated normally. If the $\overline{\text{DEND}}$ signal is received within the time shown below after a data transmission request, transmission of the next data byte is not performed.

For $\overline{\text{DEND}}$ signal received during the transmission of a byte in the middle of a sector, see table 6-9.

Table 6-9. $\overline{\text{DEND}}$ in the Middle of a Sector

8"/5" (pin 6)	FM mode	MFM mode
Low	59 μs	27 μs
High	27 μs	11 μs

For $\overline{\text{DEND}}$ signal received during the transmission of the last byte of a sector, see table 6-10.

Table 6-10. $\overline{\text{DEND}}$ at the Last Byte of a Sector

8"/$\overline{5"}$ (pin 6)	FM mode	MFM mode
Low	128 µsec	64 µsec
High	64 µsec	32 µsec

Head Unload Time: The head loaded state is maintained for the period specified by the head unload time after the command execution is terminated. Consequently, during this period if a command is issued for the same cylinder of the same drive, it can be executed before the head load wait time.

Transmitting Only the Number of Bytes Specified by MNL from a Sector: With command parameter's RL byte = HEX 00 and MNL byte < HEX 80, only the bytes specified by the MNL byte are transmitted from each sector. Remaining bytes are checked for a CRC error, but they are not transmitted to the host.
Until the $\overline{\text{DEND}}$ signal is received, a multisector read is performed with only MNL bytes being transmitted from each sector.

Result Parameters CA, HA, SA, and RL after Normal Termination with $\overline{\text{DEND}}$ Signal:
When the command execution is normally terminated by the $\overline{\text{DEND}}$ signal, the result parameters CA, HA, SA, and RL take on the values shown in table 6-11 depending on the values of the MT bit in the command code, ESN of the command parameters, and SA of the sector to which the $\overline{\text{DEND}}$ signal was applied.
CAd, HAd, SAd, and RLd represent the ID of the sector, the $\overline{\text{DEND}}$ signal was applied to.

Table 6-11. Result of $\overline{\text{DEND}}$ Termination

SAd	MT	HAd	Result parameters			
			CA	HA	SA	RL
SAd < ESN	×	×	CAd	HAd	SAd + 1	RLd
SAd $\geq$ ESN	0	×	CAd + 1	HAd	HEX 01	RLd
	1	HEX 00	CAd	HEX 01	HEX 01	RLd
		HEX 01	CAd + 1	HEX 00	HEX 01	RLd

Note: × = Don't care

6.5.2 READ DELETED DATA

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	SD	0	1	1	0	0
Command Parameters	×	×	×	×	×	HSL	US 1	US 0
	← CA →							
	← HA →							
	← SA →							
	← RL →							
	← ESN →							
	← GSL →							
	← MNL →							
Result Parameters	← SSB 0 →							
	← SSB 1 →							
	← SSB 2 →							
	← CA →							
	← HA →							
	← SA →							
	← RL →							

Figure 6-39. READ DELETED DATA Command

The READ DELETED DATA command (figure 6-39) is identical to the READ DATA command except that HEX FB and HEX F8 are regarded as the deleted data address mark and the data address mark, respectively.

6.5.3 READ ERRONEOUS DATA

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	MM	0	0	0	0	1	0
Command Parameters	×	×	×	×	×	H S L	U S 1	U S 0
	← C A →							
	← H A →							
	← S A →							
	← R L →							
	← E S N →							
	← G S L →							
	← M N L →							
Result Parameters	← S S B 0 →							
	← S S B 1 →							
	← S S B 2 →							
	← C A →							
	← H A →							
	← S A →							
	← R L →							

Figure 6-40.   READ ERRONEOUS DATA Command

The READ ERRONEOUS DATA command (Figure 6-40) reads the data starting from the first sector detected after the index to the end of the track regardless whether there are errors present or not.   Sectors are read in the order, they occur after index pulse detection, independent of CA, HA, SA and RL.   The SA byte of the command parameters is ignored and HEX 01 is specified in the FDC at the start of the command execution.   Multisector read is performed by incrementing SA by 1.   Multitrack read cannot be specified.

Selection of Unit and Head: Same as in the READ DATA command.

Ready Check: Same as in the READ.DATA command.

Head Load: Same as in the READ DATA command.

ID Search: An ID following the index pulse is searched independent of the command parameters.
The FDC uses CA, HA, and RL just as set in the command parameters but ignores SA and sets it to HEX 01 to begin the ID search.   If the contents of an ID field following the index pulse do not match the specified CA, HA, SA, and RL, the INF bit of SSB1 is set.   Simultaneously, the data in the sector is read and SA is incremented to search for an ID in the next sector.   If the

CA byte does not match, only the INF bit of SSB1 is set. Although an ID mismatch is detected, the command execution is not abnormally terminated. If an ID address mark cannot be found by the time three index pulses are detected, the ANF bit of SSB1 is set and the command execution is abnormally terminated.

CRC Check: CRC check is performed every time an ID and data are read. When a CRC error is detected, the CER bit of SSB1 and the CDF bit of SSB2 are set in the same way as in the READ DATA command. CRC error detection does not cause abnormal end of the command execution.

Detection of Data Address Mark: Same as in the READ DATA command.

Detection of Deleted Data Address Mark: When a deleted data address mark is detected, the DDA bit of SSB2 is set. Data on a sector containing a deleted data address mark is also accessed. Detection of a deleted data address mark does not cause the command execution to terminate.

Data Transmission: Same as in the READ DATA command.

Multisector Read: Multisector read is performed in a sequential order as they physically occur after the index pulse. When the DEND signal is received, the read operation stops. SA is initially set to HEX 01 independent of the contents of any ID read and is incremented by 1 for every sector read.
All other operations are the same as in the READ DATA command.
The READ ERRONEOUS DATA command has no multi-track read function.

Head Unload Timing: Same as in the READ DATA command.

Transmitting Only the Number of Bytes Specified by the MNL from a Sector: Same as in the READ DATA command.

Result Parameters CA, HA, SA, and RL after Normal Termination by $\overline{\text{DEND}}$ Signal: Same as in the READ DATA command.

6.5.4 READ ID

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	MM	0	0	1	0	1	0
Command Parameters	×	×	×	×	×	H S L	U S 1	U S 0
Result Parameters	←————————— S S B 0 —————————→							
	←————————— S S B 1 —————————→							
	←————————— S S B 2 —————————→							
	←————————— C A —————————→							
	←————————— H A —————————→							
	←————————— S A —————————→							
	←————————— R L —————————→							

Figure 6-41. READ ID Command

The READ ID command (figure 6-41) transmits the first error-free ID detected after the command execution has started to the host as result parameters CA, HA, SA, and RL.

Selection of Unit and Head: Same as in the READ DATA command.

Ready Check: Same as in the READ DATA command.

Head Load: Same as in the READ DATA command.

ID Search: The FDC searches for a CRC error-free ID.

If an ID address mark cannot be found by the time three index pulses are detected, the ANF bit of SSB1 is set and the command execution in abnormally terminated. If a CRC-error-free ID cannot be found by the time three index pulses are detected, even if an ID address mark has been found, the INF (ID Not Found) of SSB1 is set and the command execution is abnormally terminated.

CRC Check: A CRC check is performed on the read ID. If an error exists the SSB0 byte is not modified, but the next ID is searched.

Head Unload Timing: Same as in the READ DATA command.

6.5.5 WRITE DATA

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	0	0	0	1	0	1
Command Parameters	×	×	×	×	×	HSL	US1	US0
	← CA →							
	← HA →							
	← SA →							
	← RL →							
	← ESN →							
	← GSL →							
	← MNL →							
Result Parameters	← SSB0 →							
	← SSB1 →							
	← SSB2 →							
	← CA →							
	← HA →							
	← SA →							
	← RL →							
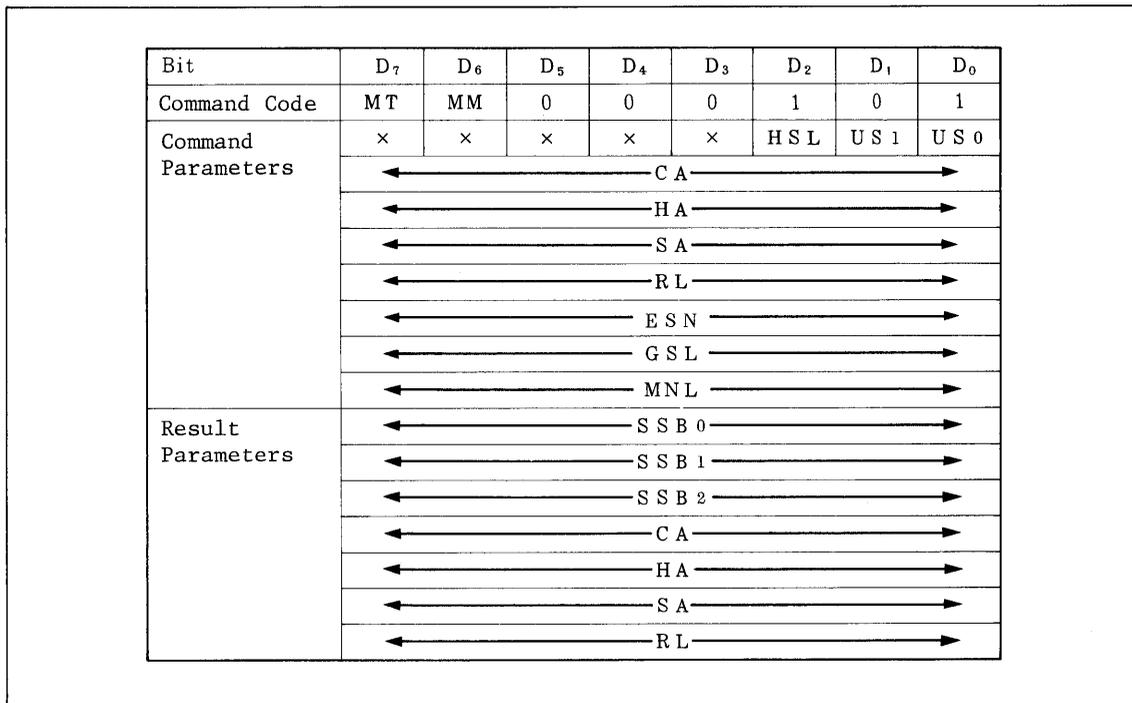
Figure 6-42. WRITE DATA Command

The WRITE DATA command (figure 6-42) requests the data transfer from the host and writes it to a sector on a track specified by the command parameters at the current head position. Multisector write is automatically performed. Multitrack write can also be performed if specified.

Selection of Unit and Head: Same as in the READ DATA command.

Ready Check: Same as in the READ DATA command.

Head Load: Same as in the READ DATA command.

ID Search: Same as in the READ DATA command.

CRC Check: CRC is checked every time an ID is read. If a CRC error is detected, the CER bit of SSB1 is set and the command execution is abnormally terminated.

Writing a Data Address Mark: One-byte and four-byte data address marks are written in the FM and MFM modes respectively.

FM mode

Data: HEX FB

Clock: HEX C7

MFM mode

Data: HEX A1 HEX A1 HEX A1 HEX FB

Clock: HEX 0A HEX 0A HEX 0A HEX 00

Transmitting Data: According to the NDM bit of the SPECIFY command, data transmission is requested from the host by the $\overline{\text{DREQ}}$ (DMA mode) or $\overline{\text{IRQ}}$ signal (Non-DMA mode). The data from the host are written to the disk in order of upper bits to lower bits. If the host does not transmit the data within the times shown in table 6-12 after a transmission request by the $\overline{\text{DREQ}}$ or $\overline{\text{IRQ}}$ signal, the DOR bit of SSB1 is set and the command execution is abnormally terminated.

Table 6-12. Write Data Transfer Request Wait Times

8"/$\overline{5}$" (Pin 6)	FM Mode	MFM mode
Low	52 μs	20 μs
High	26 μs	10 μs

Multisector/Multitrack Write: If the $\overline{\text{DEND}}$ signal is not received after all the data for one sector has been transmitted from the host, SA is incremented by 1 and processing of the next sector begins (multisector write). However, if

SA of the last sector processed is ESN, the following operations are performed depending on the Head Address HA and the MT bit of the command code:

. MT bit = 1 and HA = HEX 00

  Multitrack write is performed with SA = HEX 01, HD = HEX 01.

. MT bit = 0 or HA = HEX 01

  The NDE bit of SSB1 is set and the command execution is abnormally terminated.

If the $\overline{\text{DEND}}$ signal is received during the transmission of the data bytes for a sector, the data transmission request to the host ends immediately and HEX 00 is written for the remaining data bytes; the command execution is normally terminated. Also, when the $\overline{\text{DEND}}$ signal is received during the transmission of the last byte for a sector, access of the next sector is not performed and the command execution is normally terminated. Valid input timing of the $\overline{\text{DEND}}$ signal is the same as in the READ DATA command.

Head Unload Timing: Same as in the READ DATA command.

Transmitting Only the Number of Bytes Specified by MNL to a Sector: With the command parameter RL byte = HEX 00 and MNL byte < HEX 80, only the number of bytes specified by the MNL byte is requested to be transmitted to a sector.

HEX 00 is written for the remaining bytes. Until the $\overline{\text{DEND}}$ signal is received, a multisector write is performed with only MNL bytes being transmitted for each sector.

Result Parameters CA, HA, SA, and RL after Normal Termination with DEND Signal: Same as in the READ DATA command.

Checking Write Protected Signal: The write protected signal is checked immediately after the ready signal check. If a write protected signal is active, the WPM (write protected medium) bit of SSB1 is set and the command execution is abnormally terminated.

Checking Write Fault Signal: The write Fault signal is checked when the write gate signal is deactivated after the data has been written into a sector. If the write fault signal is active, the DER (drive error) bit of SSB0 is set and the command execution is abnormally terminated.

Writing CRC and Data Gap: A data field write is completed by writing a 2-byte CRC and a 1-byte data gap at the end of the data field. Then the write gate signal is deactivated. The contents of the CRC bytes are calculated based on the data transmitted from the host.
The contents of the data gap are:
FM mode: HEX FF
MFM mode: HEX 4E

6.5.6 WRITE DELETED DATA

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	0	0	1	0	0	1
Command Parameters	×	×	×	×	×	HSL	US1	US0
	← CA →							
	← HA →							
	← SA →							
	← RL →							
	← ESN →							
	← GSL →							
	← MNL →							
Result Parameters	← SSB0 →							
	← SSB1 →							
	← SSB2 →							
	← CA →							
	← HA →							
	← SA →							
	← RL →							

Figure 6-43. WRITE DELETED DATA Command

The WRITE DELETED DATA command (figure 6-43) is identical to the WRITE DATA command except that the following 1-byte and 4-byte deleted data address marks are written in the FM and MFM mode, respectively.

In FM mode
  Data : HEX F8
  Clock: HEX C7

In MFM mode
  Data : HEX Al, HEX Al, HEX Al, HEX F8
  Clock: HEX OA, HEX OA, HEX OA, HEX O3

6.5.7 WRITE FORMAT

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	M M	0	0	1	1	0	1
Command Parameters	×	×	×	×	×	H S L	U S 1	U S 0
	←————————— R L —————————→							
	←————————— S C N T —————————→							
	←————————— G P 3 L —————————→							
	←————————— D U D —————————→							
Result Parameters	←————————— S S B 0 —————————→							
	←————————— S S B 1 —————————→							
	←————————— S S B 2 —————————→							
	←————————— C A —————————→							
	←————————— H A —————————→							
	←————————— S A —————————→							
	←————————— R L —————————→							

Figure 6-44. WRITE FORMAT Command

The WRITE FORMAT command (figure 6-44) formats a single track where the head is currently positioned depending on the SFORM input (pin 4).

SFORM = 1: IBM format

SFORM = 0: ECMA (ISO) format

See section 6.6, "Track Format". When an index pulse is detected, the write gate signal is activated to begin the formatting operation.

Drive and Head Select: Same as in the READ DATA command.

Ready Check: Same as in the READ DATA command.

Head Load: Same as in the READ DATA command.

Head Unload Timing: Same as in the READ DATA command.

Write Protected Signal Check: Same as in the WRITE DATA command.

Write Fault Signal Check: A write fault signal check is performed immediately after the write gate signal is deactivated at the end of each track formatting. At this time if the write fault signal is active, the DER bit of SSB0 is set and the command is abnormally terminated.

Formatting Start and End: Formatting begins when the index pulse is detected. After the last sector has been written, the gap is written continually until

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the next index pulse is detected. When the next index pulse is detected, the formatting operation ends by deactivating the write gate signal.

Note: When the second index pulse is detected, the write gate signal is deactivated even if the last sector write has not yet been completed and the command is normally terminated.

Data Transfer: During formating, ID field's CA, HA, SA, and RL bytes must be transferred as data for each sector. Both DMA and Non-DMA transfers are possible. Data transfer timing is the same as in the WRITE DATA command. If the data transfer from the host is delayed and cannot meet the transfer request made by the FDC's $\overline{IRQ}$ or $\overline{DREQ}$ signal, the DOR bit of SSB1 is set and the command is abnormally terminated. The FDC continues to write the gap from the time an overrun error occurred (in the middle of an ID field) until the next index pulse is detected. The CA, HA, SA, and RL bytes from the transferred data are written intact into the ID field. Therefore, even if command parameter's RL byte value is different from the transferred data's, the transferred data's RL value is written in the ID field. The actual sector length, however, complies with command parameter's RL byte rather than the RL byte on the disk.

Format: Format conforms to section 6.6, "Track Format". Sector length is specified by the command parameter's RL byte. The number of sectors to be written is specified by the SCNT (sector count) byte. The DUD (dummy data) byte's contents are written into all data fields. Length of the gap between the adjacent sectors (GAP3) is specified by the GP3L (gap 3 length) byte.

6.5.8 SEEK

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	1	1	1	1
Command parameter	×	×	×	×	×	×	U S 1	U S 0
	← —————————————— N C N —————————————→							
Result parameter	———							

Figure 6-45. SEEK Command

In the SEEK operation (figure 6-45), a drive's head is moved onto the track specified by the command parameter's NCN (New Cylinder Number) byte. The stepping rate (step pulse interval) is specified by the SPECIFY command.

Ready Checking: Timing for the ready check conforms to section 5, "Polling". If the ready signal of the drive selected is inactive at the start or during the command execution, the step pulse output is halted immediately, and the SED (seek end) and DNR (drive not ready) bits of SSBO are set. The command is terminated abnormally and a request for issuing the CHECK INTERRUPT STATUS command is made by setting the $\overline{\text{IRQ}}$ signal active.

Drive Seek Bits Setting: After the ready signal has been checked, the drive seek bit (D0S-D3S) of the status register (STR) corresponding to the drive for which the command was issued is set. The drive seek bits can be reset only by issuing the CHECK INTERRUPT STATUS or ABORT command after the seek operation.

Direction Signal (HDIR) Setting: Command parameter's NCN and FDC's PCN (physical cylinder number) bytes are compared:

    If NCN > PCN, HDIR is set
    If NCN < PCN, HDIR is reset
    HDIR is undefined (1 or 0) when NCN=PCN

PCN Setting: Step pulse count is calculated from the PCN and NCN values after which the NCN value is substituted for PCN. Accordingly, the head's actual physical address will differ from the PCN value if a command ends (abnormal end due to change in state of ready signal, or end by ABORT command) before all step pulses are issued. The head's physical address will also differ from the PCN value if a second SEEK command is issued to a drive while it is seeking. When issuing the SEEK command, make sure that the drive seek bit of the status register corresponding to the drive to which the command is issued is zero.

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Seek Completion: After all the calculated number of step pulses have been output, SSB0's SED (seek end) bit is set after the step rate time specified by the SPECIFY command following the last step pulse output. The number of the drive which terminates the seek is then set in US0 and US1 of SSB0. Following this, the command terminates normally and the CHECK INTERRUPT STATUS command is requested by setting the $\overline{IRQ}$ signal active. Additionally, when HDIR = 0, if TRK0 becomes active, the step pulse output is halted prematurely. Following this, as described in the previous paragraph, the SED, US0, and US1 bits of SSB0 are modified and the command normally ends with an interrupt request to the host for issuing a CHECK INTERRUPT STATUS command. At this time, the result parameter PCN of the CHECK INTERRUPT STATUS command is the same as the command parameter NCN value of the SEEK command, and is not always HEX 00. The TRK0 signal is latched 500 ns (8" mode) or 1 µs (5" mode) before the step pulse output.

Parallel Seek: The FDC is placed into the command waiting state when the step pulse output begins after receiving the SEEK or RECALIBRATE command. At this time, another SEEK or RECALIBRATE command can be issued for a new drive whose drive seek bit in the status register is zero.

Head Unload: The head must be unloaded (HLOAD = 0) immediately after the SEEK command is issued. However, if the SEEK command is issued for a drive whose head is loading and parameter NCN is equal to PCN, the command is terminated without head unload.

Note: If the SEEK command is issued to a drive which is not ready, the status register's drive seek bit is not set.

6.5.9 RECALIBRATE

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	0	1	1	1
Command Parameter	×	×	×	×	×	×	US 1	US 0
Result Parameter				——				

Figure 6-46. RECALIBRATE Command

The RECALIBRATE command (figure 6-46) moves a drive's head to track 0. Head movement speed is the stepping rate (step pulse interval) specified by the SPECIFY command.

Ready Checking: Same as in the SEEK command.

Drive Seek Bit Setting: Same as in the SEEK command.

Direction Signal Setting: Resets HDIR.

PCN Setting: Step pulse count is 255, and PCN = HEX 00. However, if the system is in the drive-not-ready state, the PCN value does not change.

End of Recalibration: If the TRK0 signal becomes active during recalibration or after the step rate period specified by the SPECIFY command following the 255th step pulse, SSB0's SED bit is set and the recalibrated drive number is set in US0 and US1 and the command ends normally. Following this, a request for the CHECK INTERRUPT STATUS command is made to the host by setting the $\overline{IRQ}$ signal active. If the TRK0 signal does not become active following the step rate time specified by the SPECIFY command after 255 step pulses, SSB0's SED and DER (drive error) bits are set, US0 and US1 are set to the recalibrated drive number, and a CHECK INTERRUPT STATUS command is requested by setting the $\overline{IRQ}$ signal active.

Parallel Seek: Same as in the SEEK command.

Head Unload: Head unload state (HLOAD = 0) is specified immediately after the RECALIBRATE command is issued.

Note: If the RECALIBRATE command is issued to a drive which is not ready, the status register's drive seek bit is not set.

6.5.10 COMPARE EQUAL

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	M T	M M	S D	1	0	0	0	1
Command Parameters	×	×	×	×	×	H S L	U S 1	U S 0
	← C A →							
	← H A →							
	← S A →							
	← R L →							
	← E S N →							
	← G S L →							
	← S T E P →							
Result Parameters	← S S B 0 →							
	← S S B 1 →							
	← S S B 2 →							
	← C A →							
	← H A →							
	← S A →							
	← R L →							

Figure 6-47. COMPARE EQUAL Command

The COMPARE EQUAL command (figure 6-47) compares data from the host with the data read from a disk.

Drive and Head Select: Same as in the READ DATA command

Ready Check: Same as in the READ DATA command

Head Load: Same as in the READ DATA command

ID Search: Same as in the READ DATA command

CRC Check: Same as in the READ DATA command

Data Address Mark Detect: Same as in the READ DATA command

Deleted Data Address Mark Detect: Same as in the READ DATA command

Data Transfer: Same as in the WRITE DATA command except for the values of the time from the data transfer requests made by the $\overline{DREQ}$ or $\overline{IRQ}$ signal to the data overrun shown in table 6-13.

Table 6-13. Data Overrun Times

8"/$\overline{5}$" (Pin 6)	FM mode	MFM mode
Low	43 μs	15 μs
High	21 μs	7 μs

Multisector/Multitrack Compare: SA is updated by SA + STEP (command parameter's STEP byte) to locate the next sector which may satisfy the compare condition; the sector is then processed in multisector comparison. However, if the processed sector's SA is ESN, or SA + STEP > ESN, the following is performed depending on HA and the command code MT bit:

When MT bit = 1 and HA = HEX 00
Multitrack comparison is performed with SA = HEX 01, and HA = HEX 01.

When MT bit = 1 or HA = HEX 01
CNS (compare condition not satisfied) bit of SSB2 is set and the command ends normally. In COMPARE commands, ESN ≤ HEX FD.

If the $\overline{DEND}$ signal is received in the middle of sector processing, obtained data comparison results are checked whether or not they satisfy the specified condition. If the condition is not satisfied, the comparison data for the remaining sector data are not requested by the host to be transferred. Still, the data from the drive is read and the CRC check is performed. However, the transfer of the comparison data for the next sector indicated by the SA increment is requested. That is, the $\overline{DEND}$ signal is not a command execution termination condition, so the $\overline{DEND}$ signal need not be activated at the end of a sector processing.

A multisector comparison requires that all sector comparison data for all sector comparison results is to be transferred to the host.

$\overline{DEND}$ signal valid timing is shown in table 6-14.

Table 6-14 $\overline{DEND}$ in the Middle of a Sector

8"/$\overline{5}$" (Pin 6)	FM mode	MFM mode
Low	45 μs	15 μs
High	21 μs	7 μs

Head Unload Timing: Same as in the READ DATA command

Result Parameter's CA, HA, SA and RL Bytes after a Normal End: Sector ID contents which determined a normal end are output to the host.

Comparison Condition: When the data sent from the host matches the data read from the drive, the compare condition is considered to be satisfied. HEX FF data from the host is considered to match any data from the drive, so the compare condition is always satisfied. When a specified condition is satisfied, CCS (compare condition satisfied) bit of SSB2 is set and the command normally ends. If no sector satisfying the specified conditions is detected, even if comparison is performed as far as the sector specified by the ESN byte, the command is completed normally by setting the SSB2's CNS (Compare Condition Not Satisfied).

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	SD	1	1	0	0	1
Command Parameters	×	×	×	×	×	HSL	US1	US0
	◄————————————— C A —————————————►							
	◄————————————— H A —————————————►							
	◄————————————— S A —————————————►							
	◄————————————— R L —————————————►							
	◄————————————— E S N —————————————►							
	◄————————————— G S L —————————————►							
	◄————————————— S T E P —————————————►							
Result Parameters	◄————————————— S S B 0 —————————————►							
	◄————————————— S S B 1 —————————————►							
	◄————————————— S S B 2 —————————————►							
	◄————————————— C A —————————————►							
	◄————————————— H A —————————————►							
	◄————————————— S A —————————————►							
	◄————————————— R L —————————————►							
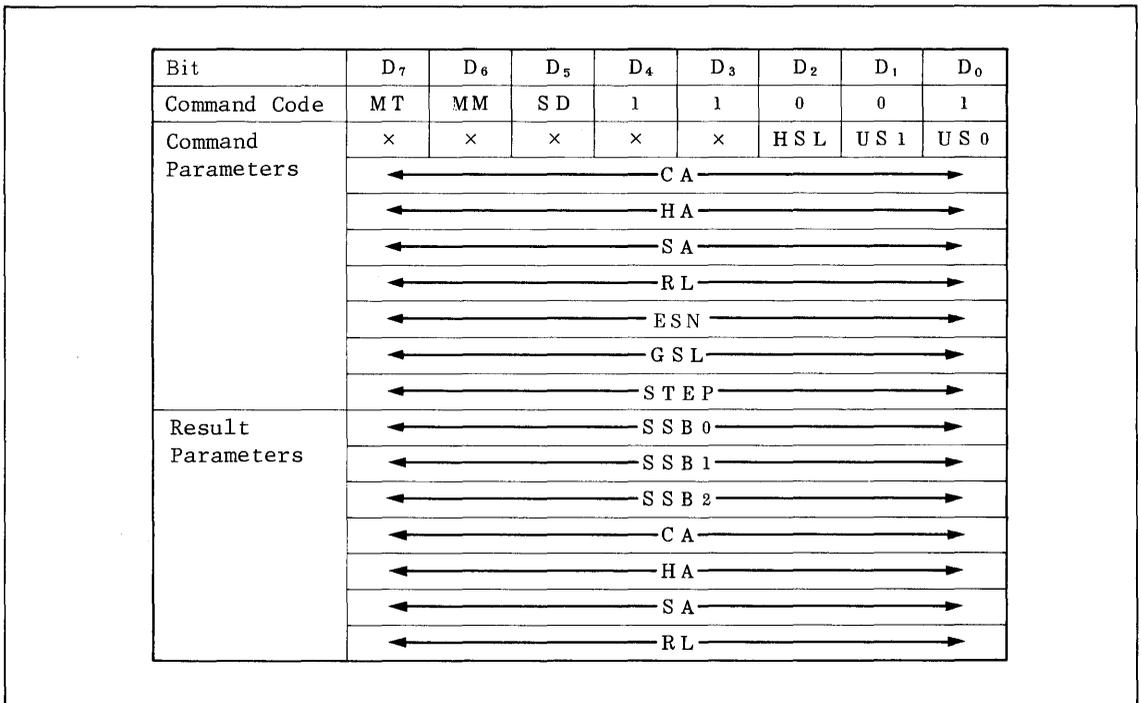
Figure 6-48.   COMPARE LOW OR EQUAL Command

The COMPARE LOW OR EQUAL command (figure 6-48) is identical to the COMPARE EQUAL command except for the comparison condition.

Comparison Condition: When the data from the host matches the data from the drive, the same processing as in the case of COMPARE EQUAL command is performed. If the data from the host is HEX FF, any data from the drive is considered to match.   If the first pair of bytes which do not match satisfied the following condition:

     host data > drive data,

the CRC check is performed before ending the command normally.   In this case, the CCS bit of SSB2 is not set.   If no sector satisfying the specified conditions is detected, even if comparison is performed as far as the sector specified by the ESN byte, the command is completed normally by setting the SSB2's CNS (Compare Condition Not Satisfied).

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	M T	M M	S D	1	1	1	0	1
Command Parameters	×	×	×	×	×	H S L	U S 1	U S 0
	←——————— C A ———————→							
	←——————— H A ———————→							
	←——————— S A ———————→							
	←——————— R L ———————→							
	←——————— E S N ———————→							
	←——————— G S L ———————→							
	←——————— S T E P ———————→							
Result Parameters	←——————— S S B 0 ———————→							
	←——————— S S B 1 ———————→							
	←——————— S S B 2 ———————→							
	←——————— C A ———————→							
	←——————— H A ———————→							
	←——————— S A ———————→							
	←——————— R L ———————→							
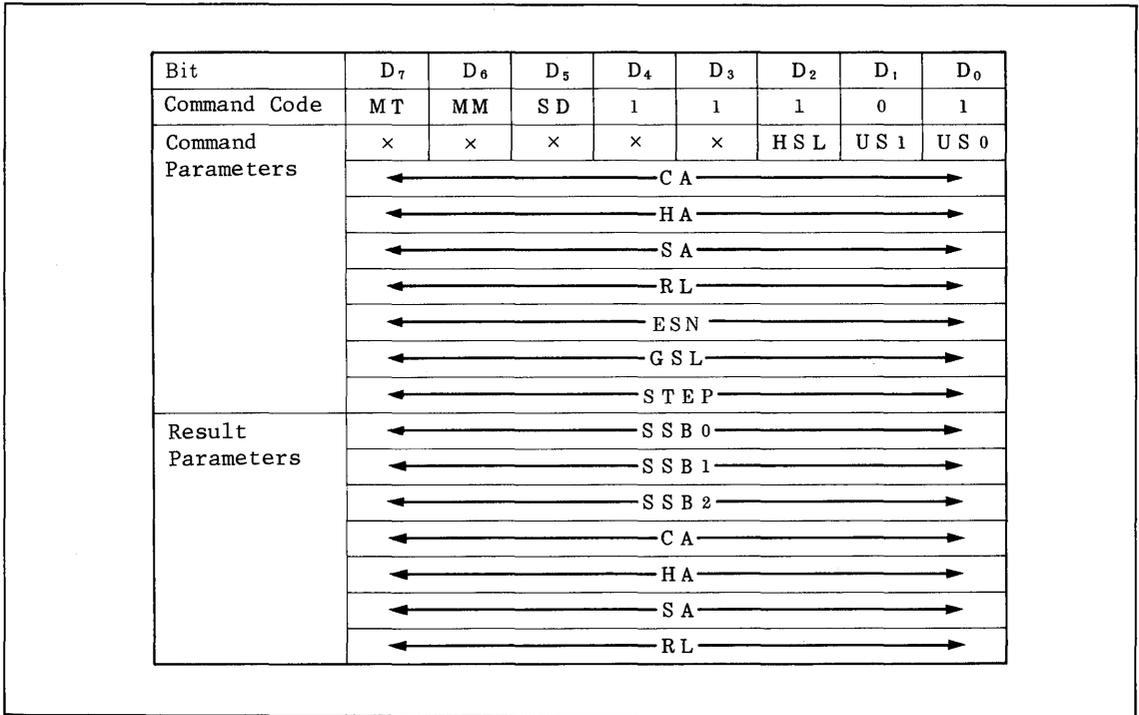
Figure 6-49. COMPARE HIGH OR EQUAL Command

The COMPARE HIGH OR EQUAL command (figure 6-49) is identical to the COMPARE EQUAL command except for the comparison condition.

Comparison Condition: When the data from the host matches the data from the drive, the same processing as in the case of COMPARE EQUAL command is performed. If the data from the host is HEX FF, any data from the drive is considered to match. It the first pair of bytes which do not match satisfies the following condition:

> host data < drive data,

the CRC check is performed before ending the command normally. In this case, the CCS bit of SSB2 is not set. If no sector satisfying the specified conditions is detected, even if comparison is performed as far as the sector specified by the ESN byte, the command is completed normally by setting the SSB2's CNS (Compare Condition Not Satisfied).

6.5.13   CHECK DEVICE STATUS

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	0	1	0	0
Command Parameters	×	×	×	×	×	H S L	U S 1	U S 0
Result Parameters	←				S S B 3			→

Figure 6-50.   CHECK DEVICE STATUS Command

The CHECK DEVICE STATUS command (figure 6-50) reads the status of a drive and sets it up in SSB3 transfer to the host. HSL, US1 and US0 bits of SSB3 are updated to contain exactly the same values as the respective command para-meter values. This command can also be issued for a drive which is performing a seek or recalibrate operation. If the command is issued for a different drive than the one currently selected, then its heads must be immediately unloaded (HLOAD = 0).

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	1	0	0	0
Command Parameters				———				
Result Parameters	◄———————— S S B 0 ————————►							
	◄———————— P C N ————————►							
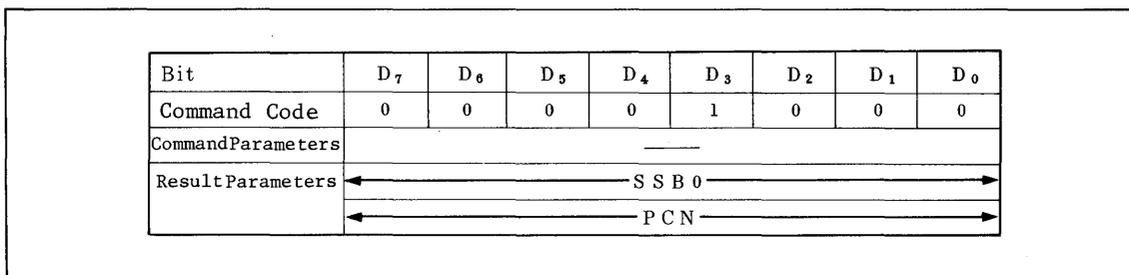
Figure 6-51. CHECK INTERRUPT STATUS Command

The CHECK INTERRUPT STATUS command (figure 6-51) transfers to the host the causes of the interrupt request made by the FDC, when the status register value is HEX 8X (command waiting state).

There are two types of interrupt causes:

· SEEK or RECALIBRATE command has ended normally or abnormally

· Ready signal has changed state since last polling

When the FDC does not have the Seek End (SED) or Ready Inversion (CDS) status, issuance of the CHECK INTERRUPT STATUS command is treated as an INVALID command.

6.5.15   SPECIFY 1

Bit	D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
Command Code	0	0	0	0	0	0	1	1
Command Parameters	S T R				H D U T			
	H D L T							N D M
Result Parameters	——							

Figure 6-52.   SPECIFY 1 Command

The SPECIFY 1 command (figure 6-52) specifies the stepping rate, head unload time, head load time, and Non-DMA mode (or DMA mode).

If a SPECIFY 1 command is issued after a SPECIFY 2 command, the auto-precompensation and high-speed seek modes specified under SPECIFY 2 command are reset, and the track position activating the LCT signal is specified as track 43.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	A	H	0	1	0	1	1
Command Parameter 1	S T R				H D U T			
	H D L T							N D M
	L C T K							
Command Parameter 2	P C 1				P C 0			
	P C D C T							
Result Parameter	——							

Figure 6-53. SPECIFY 2

The SPECIFY 2 command (figure 6-53) specifies the stepping rate, head unload time, head load time, Non-DMA mode, low write current starting track position, auto-precompensation mode, high-speed seek mode, precompensation delays for auto precompensation, and precompensation delay change track number. Command parameter 1 is required whenever this command is issued. Command parameter 2 is needed only when command code bit A = 1. When A = 0, the FDC cannot accept this parameter.

Auto-Precompensation Mode: When A = 1, the auto-precompensation mode is selected. In this mode, the write data which has been adjusted for the PC1 or PC0 specified precompensation delays is output (only in MFM mode), with the EARLY (pin 34) and LATE (pin 33) outputs fixed at low level. When A = 0, autoprecompensation is not performed, but the EARLY and LATE precompensation control signals are output (only in MFM mode).

High-Speed Seek Mode: When H = 1, the high-speed seek mode is selected. This mode allows the stepping rate to be set to a value ranging from 1 to 16 ms in 1 ms increments in the 5" mode (8"/$\overline{5}$" = low). In the 8" mode (8"/$\overline{5}$" = high), H has no meaning.

6.5.17   SLEEP

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	1	1	1	0
Command Parameters				───				
Result Parameters				───				

Figure 6-54.   SLEEP Command

The SLEEP command (figure 6-54) allows the FDC to dissipate lower power. When the FDC receives this command,

1.   HLOAD (Head Load) is set low,

2.   US0 and US1 are set high,

and the SLEEP mode is entered. In this mode, no drive polling is performed. In the SLEEP mode, the FDC's status register is set to HEX 80 indicating that the FDC is in the command waiting state. When the FDC receives a command in the SLEEP mode, it automatically releases the SLEEP mode and executes the command.

Power dissipation can be reduced by halting the FDC clock after saving the status conditions gathered immediately before the SLEEP mode is entered.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	1	1	1	1	1	1	1	1
Command Parameters				——				
Result Parameters				——				

Figure 6-55. ABORT Command

The ABORT command (figure 6-55) resets the FDC by software.

Note: This command is issued by writing it into the abort register (ATR), and holding RS = 0.

The abort register can be accessed at any time, irrespective of the FDC state, except when the $\overline{RESET}$ input signal is active.

When the FDC receives the ABORT command:

1. FRES, HLOAD, STEP, EARLY, LATE, WDATA, and WGATE signals are set to low level.

2. $\overline{DREQ}$ and $\overline{IRQ}$ signals are set to high level

3. Status register (STR) is set to HEX 80 and the drive polling starts.

This command cannot reset FDC's cylinder numbers or the values specified by the SPECIFY command. However, when the ABORT command is issued during the execution of a SEEK or RECALIBRATE command, the cylinder number is the value set by the SEEK or RECALIBRATE command, although the remaining step pulses are no longer generated. Thus, in such a case, a RECALIBRATE command must be be issued before the next command is issued.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	SD	1	0	0	1	0
Command Parameters	×	×	×	×	×	HSL	US 1	US 0
	←————————— CA —————————→							
	←————————— HA —————————→							
	←————————— SA —————————→							
	←————————— RL —————————→							
	←————————— ESN —————————→							
	←————————— GSL —————————→							
	←————————— MNL —————————→							
Result Parameters	←————————— SSB 0 —————————→							
	←————————— SSB 1 —————————→							
	←————————— SSB 2 —————————→							
	←————————— CA —————————→							
	←————————— HA —————————→							
	←————————— SA —————————→							
	←————————— RL —————————→							
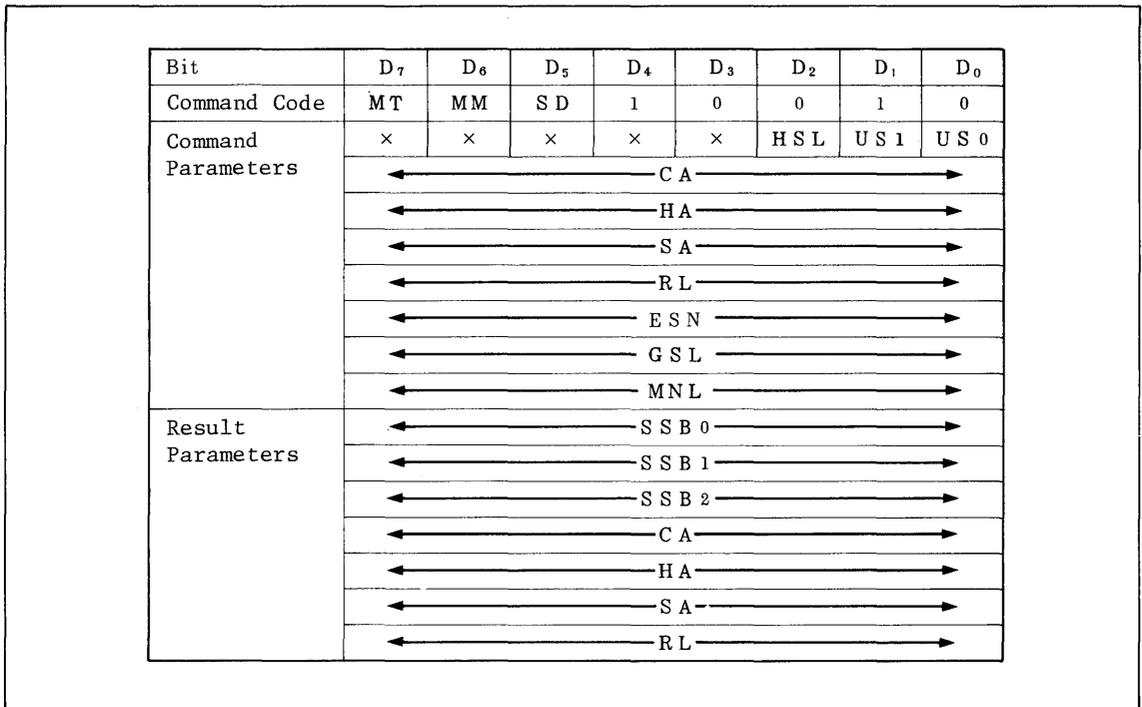
Figure 6-56.   READ LONG Command

The READ LONG command (figure 6-56) transfers the 2-byte CRC information as well as the data read from a sector to the host. This command is valid only after a SPECIFY 2 command has been issued. Otherwise it is invalid. This command is identical to the READ DATA command with the following two exceptions:

.   The CRC bytes of the sector whose data has been just transferred are also transferred to the host computer.

.   Data transfer of the type requiring only the number of bytes specified by MNL from a sector is ignored. With the $\overline{DEND}$ signal, however, the data transfer can be terminated even in the middle of a sector data or CRC byte transfer.

This command also performs a CRC check for the sector from which the data was transferred.

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Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	MT	MM	0	1	0	1	1	0
Command Parameters	×	×	×	×	×	HSL	US1	US0
	←————————————— C A —————————————→							
	←————————————— H A —————————————→							
	←————————————— S A —————————————→							
	←————————————— R L —————————————→							
	←————————————— E S N —————————————→							
	←————————————— G S L —————————————→							
	←————————————— M N L —————————————→							
Result Parameters	←————————————— S S B 0 —————————————→							
	←————————————— S S B 1 —————————————→							
	←————————————— S S B 2 —————————————→							
	←————————————— C A —————————————→							
	←————————————— H A —————————————→							
	←————————————— S A —————————————→							
	←————————————— R L —————————————→							
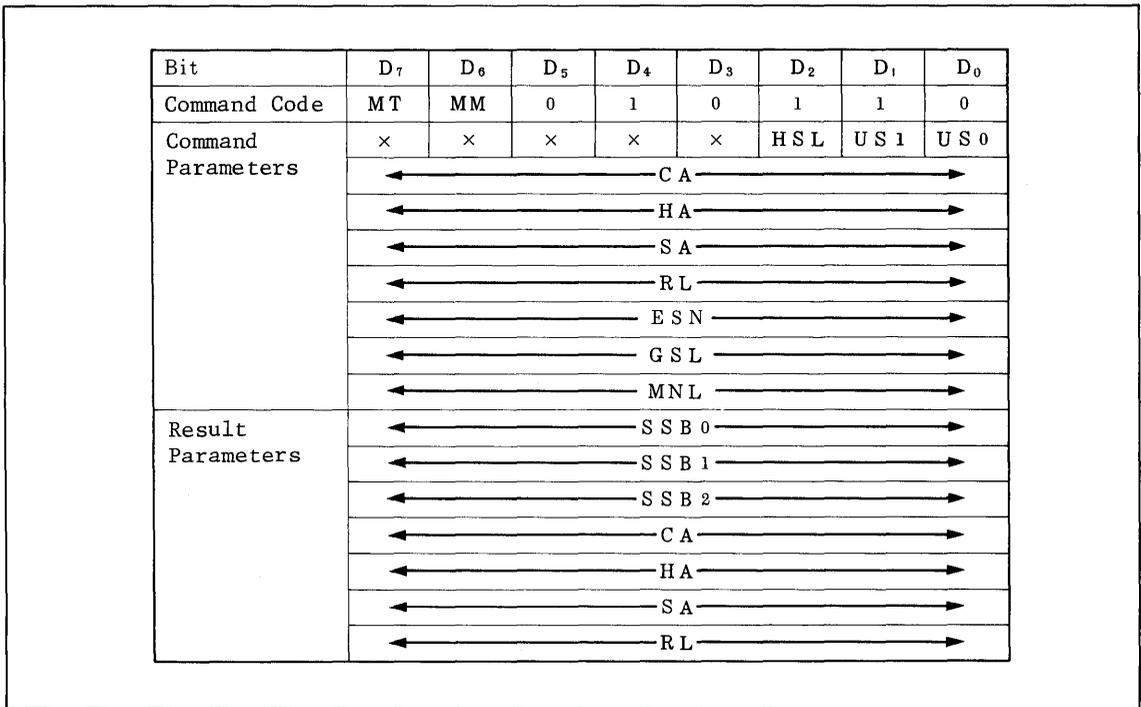
Figure 6-57.   WRITE LONG Command

The WRITE LONG command (figure 6-57) writes to a disk the 2-byte CRC information as well as the data sent from the host. This command is valid only after SPECIFY 2 command has been issued. Otherwise it is invalid. This command is identical to the WRITE DATA command except for the following:

. The host sends the 2-byte CRC information also for the sector whole data has just been sent.

. Only the number of bytes specified by the MNL byte can be written to a sector. The CRC byte also must be sent.

. If the data transfer is halted in the middle of a sector by the $\overline{\text{DEND}}$ signal, HEX 00 is written into the remaining sector including the CRC bytes.

6.5.21 INVALID

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	←——————————— INVALID Code ———————————→							
Command Parameters	———							
Result Parameters	←——————————— SSB0 ———————————→							
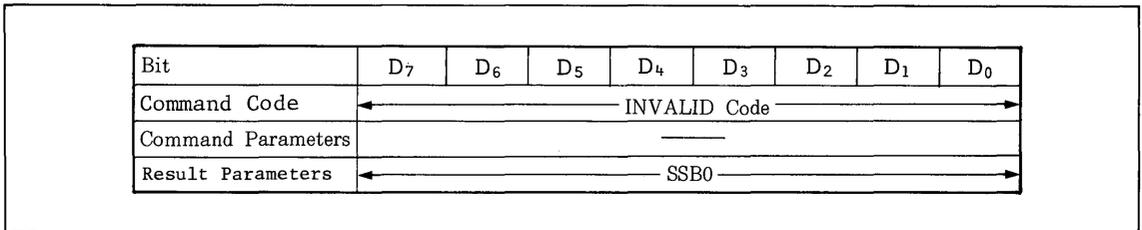
Figure 6-58. INVALID Command

The FDC processes the following cases as an INVALID command (Figure 6-58):

. Undefined command codes are written into the data register (DTR).

. HEX FF is written into DTR as a command.

. Issuing the CHECK INTERRUPT STATUS command when FDC has no Seek-end or
  Ready Inversion status informations.

SSB0 of the result parameter is HEX 80.

The following codes are not considered as INVALID commands after the SPECIFY 2
command has been issued:

HEX 10, 13, 14, 15, 17, 18, 1A, 1B, 1C, 1F, 57, 58

Consequently, if any of these codes is written into the FDC as a command, the
FDC will malfunction. The ABORT command can be used to bring the FDC to the
command waiting state, but the internal RAM contents may be destroyed.

To prevent this a SPECIFY command followed by the RECALIBRATE command must be
issued before any other command is issued. Do not write these codes into
FDC as a command at SPECIFY 2 mode.

6.6 TRACK FORMAT

Figure 6-59 shows the IBM and ISO track formats

Figure 6-59. Track Format

6.7 Command Code Rejection

6.7.1 Phenomenon

The FDC rejects command codes under the following timing conditions: (1) within the period 2.25 μs before to 1.75 μs after the $\overline{\text{IRQ}}$ signal is asserted to request a CIS command caused by READY signal inversion in 8-inch mode (or 4.5 μs before to 3.5 μs after $\overline{\text{IRQ}}$ assertion in 5-inch mode); or (2) if the $\overline{\text{IRQ}}$ signal has been asserted to request a CIS command when READY signal inversion is detected. This malfunction is described below for each timing condition.

Command Rejection Timing Condition 1: From 2.25 μs before to 1.75 μs after the $\overline{\text{IRQ}}$ signal is asserted to request a CIS command initiated by the READY signal in 8-inch mode (or 4.5 μs before to 3.5 μs after $\overline{\text{IRQ}}$ assertion in 5-inch mode)

In 8-inch mode, the FDC rejects all commands except ABORT if those commands are issued within the period 2.25 μs before to 1.75 μs after (or 4.5 μs before to 3.5 μs after in 5-inch mode) the IRQ signal is asserted to request a CIS command initiated by READY signal inversion, as shown in figure 6-60. The time during which commands are rejected is indicated by period A. In addition, for 0.5 μs (1.0 μs in 5-inch mode)(period B) after period A, the FDC accepts commands but the BSY bit of the status register (STR) remains cleared. The BSY bit of the STR is set when the host system writes the first-byte parameter to the FDC. Changes in the STR according to the timing of each issued command are summarized in table 6-15. Note that the FDC will not reject a command if the $\overline{\text{IRQ}}$ signal is asserted to request a CIS command initiated by SEEK or RECALIBRATE command completion.
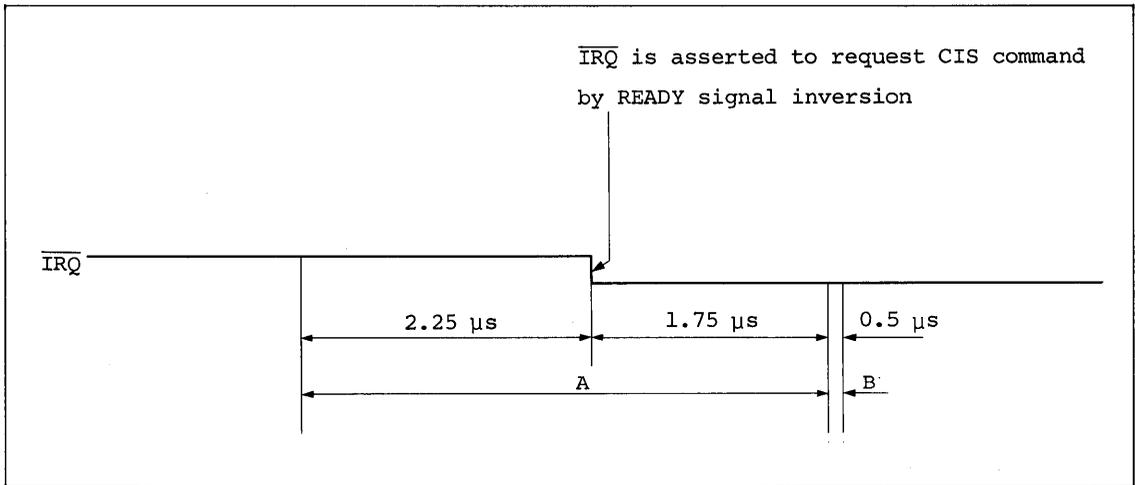
Figure 6-60.   Command Rejection Timing 1

Notes: 1. Figure 6-60 is the timing chart for 8-inch mode. For 5-inch mode,
           the periods must be doubled (2.25 μs → 4.5 μs, 1.75 μs → 3.5 μs,
           and 0.5 μs → 1.0 μs).
       2. A: If a command is issued during this period, the FDC rejects it.
           B: If a command is issued during this period, the FDC accepts it,
              but the BSY bit of the STR remains cleared.

Command Rejection Timing Condition 2: The $\overline{\text{IRQ}}$ signal has been asserted to request a CIS command when READY signal inversion is detected

The FDC rejects commands other than ABORT if those commands are issued when READY signal inversion has been detected while $\overline{\text{IRQ}}$ is asserted to request a CIS command initiated by SEEK or RECALIBRATE command completion or by a READY signal change. As shown by period A in figure 6-61, such commands are ignored for 20 µs in 8-inch mode (40 µs in 5-inch mode). In addition, during period B, which is the 0.5 µs (1.0 µs in 5-inch mode) after period A, the FDC accepts commands, but the BSY bit of the STR remains cleared. The BSY bit of the STR is set when the first-byte command parameter is written by the host system.
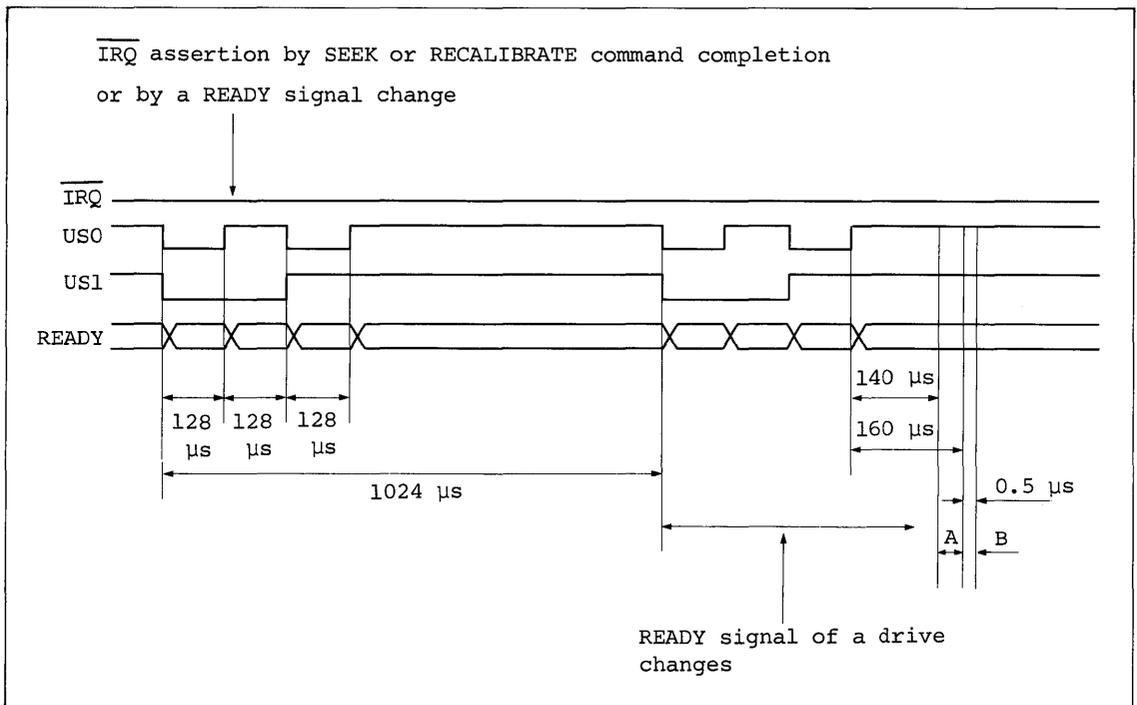
Figure 6-61. Command Rejection Timing 2

Notes: 1. Figure 6-61 is the timing chart for 8-inch mode. For 5-inch mode, the periods must be doubled (e.g., 128 µs → 256 µs, 1024 µs → 2048 µs, and 0.5 µs → 1.0 µs).

2. A: If a command is issued during this period, the FDC rejects it.
   B: If a command is issued during this period, the FDC accepts it, but the BSY bit of the STR remains cleared.

Table 6-15. STR Changes for Each Command

Command	Issue Timing	STR Change
All commands except CHECK INTERRUPT STATUS, SLEEP, and ABORT	Normal	Write command code ↓ HEX 8X -------- HEX 1X -------- HEX 9X -------- HEX 1X Wait for command / FDC busy / Request command parameter / Write parameter
	During period A	Write command code ↓ HEX 8X -------- HEX 1X -------- HEX 8X Ignore command code
	During period B	Write command code ↓ HEX 8X -------- HEX 1X -------- HEX 0X -------- HEX 8X Reset BSY / Request parameter
CHECK INTERRUPT STATUS	Normal	Write command code ↓ HEX 8X -------- HEX 1X -------- HEX DX -------- HEX 1X Request parameter acceptance / Accept parameter ↑
	During period A	Write command code ↓ HEX 8X -------- HEX 1X -------- HEX 8X Ignore command code
	During period B	Write command code ↓ HEX 8X -------- HEX 1X -------- HEX 0X -------- HEX CX Reset BSY / Request parameter acceptance
SLEEP	Normal	Write command code ↓ HEX 80 -------- HEX 10 -------- HEX 80 SLEEP
	During period A	Write command code ↓ HEX 80 -------- HEX 10 -------- HEX 80 (Ignore command code) Do not enter sleep mode
	During period B	Write command code ↓ HEX 80 -------- HEX 10 -------- HEX 00 -------- HEX 80 Reset BSY / Enter SLEEP mode

Notes: 1. ABORT is always accepted.
       2. X indicates HEX 0 - HEX F.

6.7.2 Countermeasures

Hitachi recommends implementing one of the following three countermeasures to prevent the above malfunctions: (1) check the $\overline{\text{IRQ}}$ signal level (valid for all commands); (2) check the STR status (valid for all commands except SLEEP); or (3) issue the ABORT command (valid for all command except SLEEP). These countermeasures are described in detail below.

$\overline{\text{IRQ}}$ Signal Level Check (valid for all commands)

Whether or not the FDC accepts a command code can be determined by checking the $\overline{\text{IRQ}}$ signal level after the TXR bit of the STR has been set to 1. If the FDC accepts a command code, the $\overline{\text{IRQ}}$ signal is negated high at least 5.5 μs before the TXR bit is set to 1. (TXR = 1 indicates command parameter request, result parameter accept request, or command wait state.) On the other hand, if the FDC rejects a command code, the $\overline{\text{IRQ}}$ remains asserted low when the TXR bit is set to 1. Therefore, if $\overline{\text{IRQ}}$ is negated high, the next process, such as a parameter transfer, can be performed correctly; but if $\overline{\text{IRQ}}$ remains asserted low, the command must be written to the FDC again. Figure 6-62 shows this $\overline{\text{IRQ}}$ signal level checking procedure.
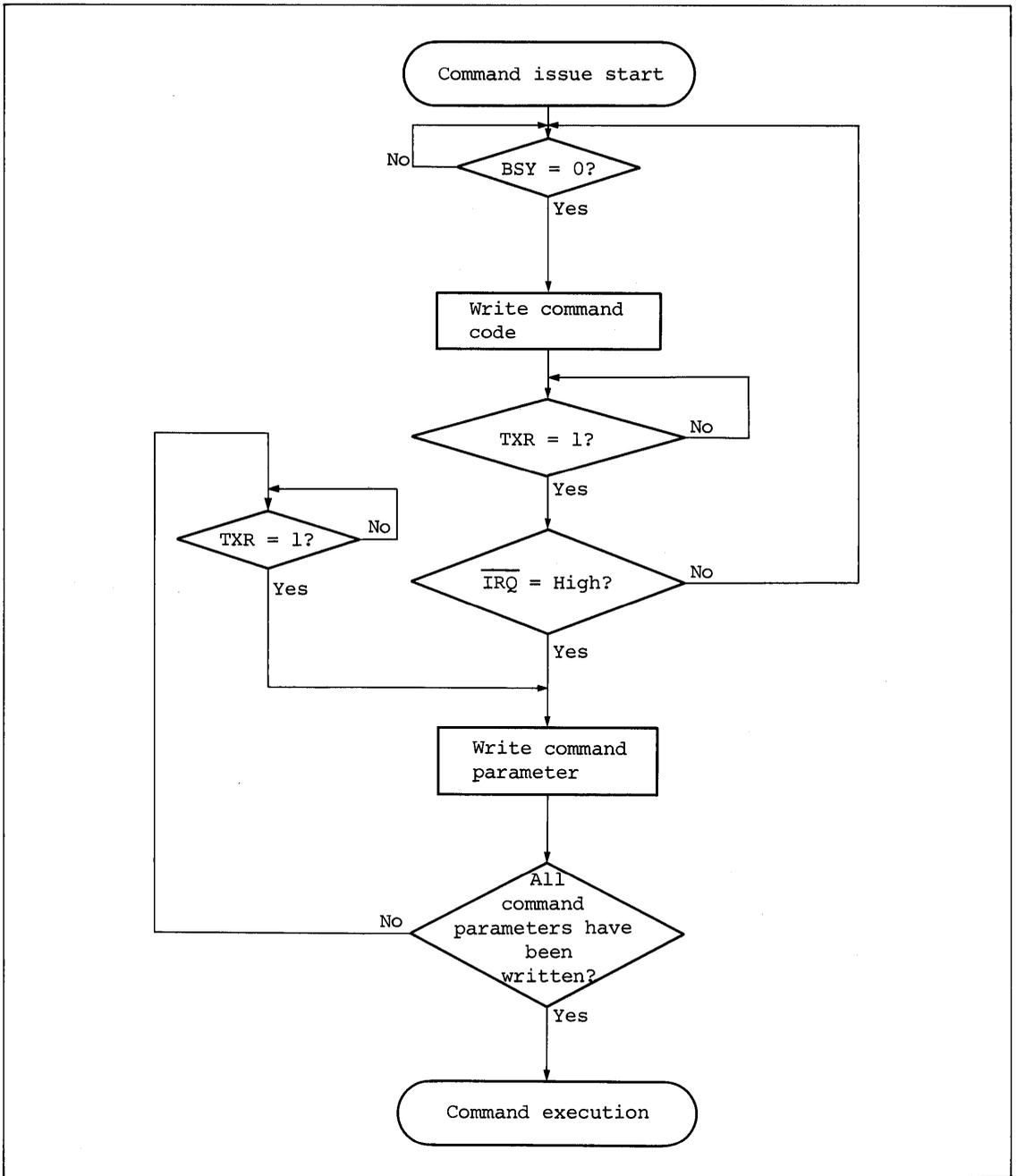
Figure 6-62. $\overline{\text{IRQ}}$ Signal Level Checking Procedure

STR Check (valid for all commands except SLEEP)

Whether or not the FDC accepts a command code can be determined by checking the contents of the STR during the T2 state, as shown in figure 6-63.

If the contents of the STR are HEX 00, a command code was issued during period B shown in figures 6-60 and 6-61. In this case, the FDC has accepted the command code and the next process, such as a parameter transfer, can be performed after the TXR bit of the STR is checked.

On the other hand, if the contents of the STR are HEX 10, a command code may be issued during period A or a period other than A and B shown in figures 6-60 and 6-61. In this case, whether or not the FDC has accepted the command code can be determined by the BSY bit of the STR as follows. If BSY is set 0.6 μs (8-inch mode) or 1.2 μs (5-inch mode) after the TXR bit has been set, the FDC has accepted the command correctly and the next process, such as parameter transfer, can be performed. If BSY is cleared, the FDC has rejected the command and the command code must be issued again.

The STR check procedure is summarized in figure 6-64.
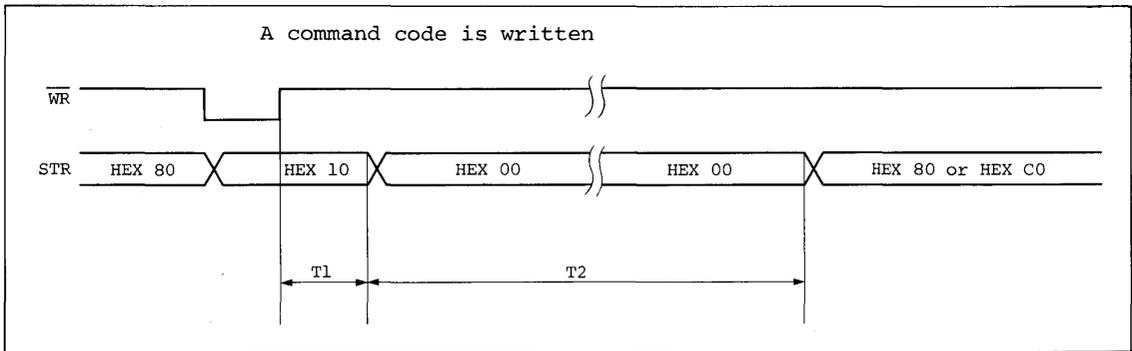
T1 State					T2 State				
8-inch mode		5-inch mode			8-inch mode		5-inch mode		
Min	Max	Min	Max	Unit	Min	Max	Min	Max	Unit
0	350	0	600	ns	9.5	18.0	19.0	36.0	μs

Note: STR is HEX 00 during the T2 state if a command code is issued during period B shown in figures 6-60 and 6-61.

Figure 6-63.   Timing Diagram When STR is HEX 00
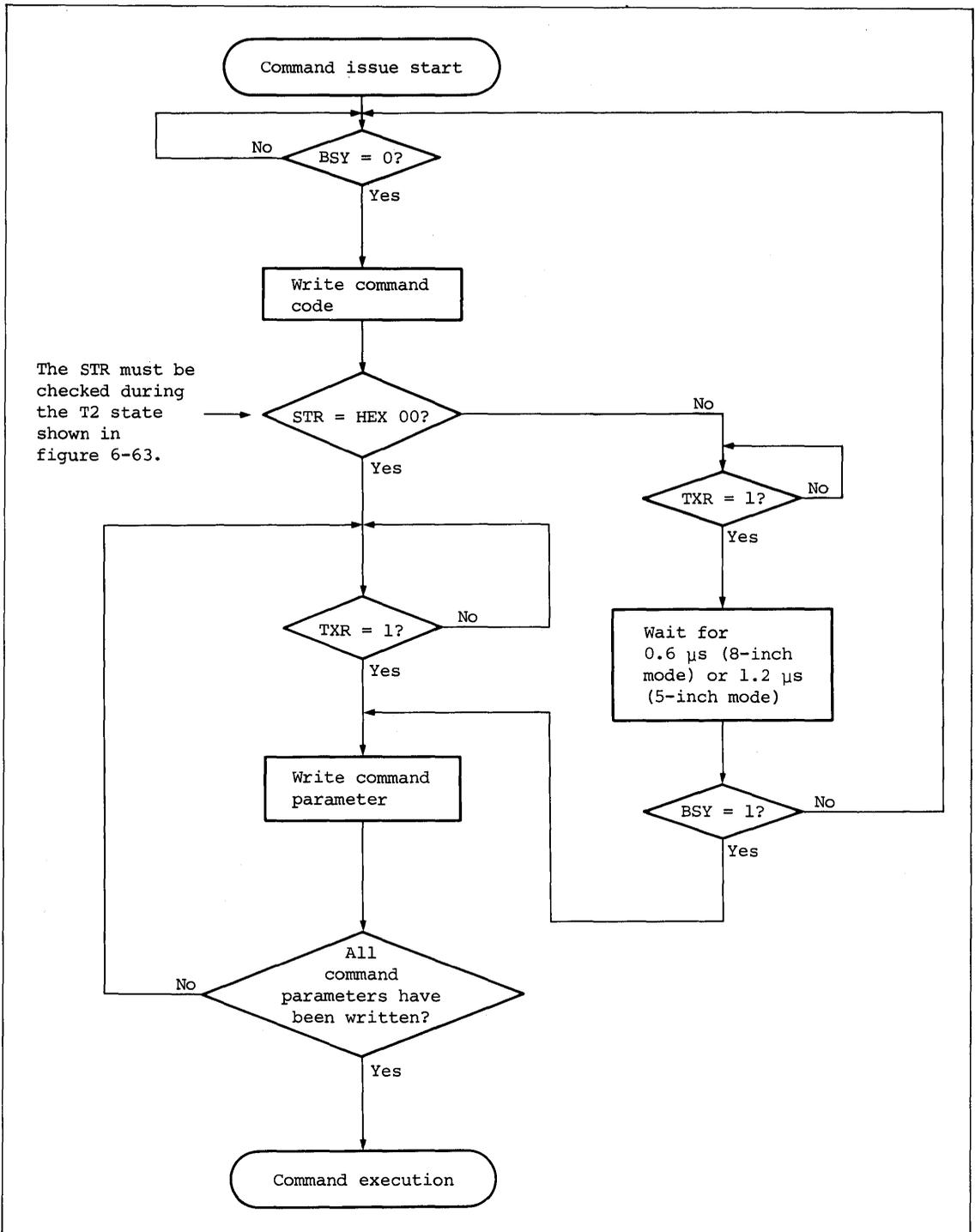
Figure 6-64. STR Checking Procedure

ABORT Command Issue (valid for all commands except SLEEP)

Whether or not the FDC accepts a command can be determined by checking the BSY bit of the STR 0.6 µs (8-inch mode) or 1.2 µs (5-inch mode) after the TXR bit has been set.

If a command is issued during period A shown in figures 6-60 and 6-61, the BSY bit is cleared 0.6 µs (8-inch mode) or 1.2 µs (5-inch mode) after the TXR bit has been set. In addition, if a command is issued during period B shown in figures 6-60 and 6-61, the BSY bit is always cleared after the TXR bit has been set.

Therefore, if the BSY bit is cleared 0.6 µs (8-inch mode) or 1.2 µs (5-inch mode) after the TXR bit has been set, the command must be issued again after the ABORT command has been issued.

If BSY is set 0.6 µs (8-inch mode) or 1.2 µs (5-inch mode) after the TXR bit has been set, the FDC has accepted a command correctly and the next process, such as parameter transfer, can be performed.

Figure 6-65 shows the ABORT command issue procedure.
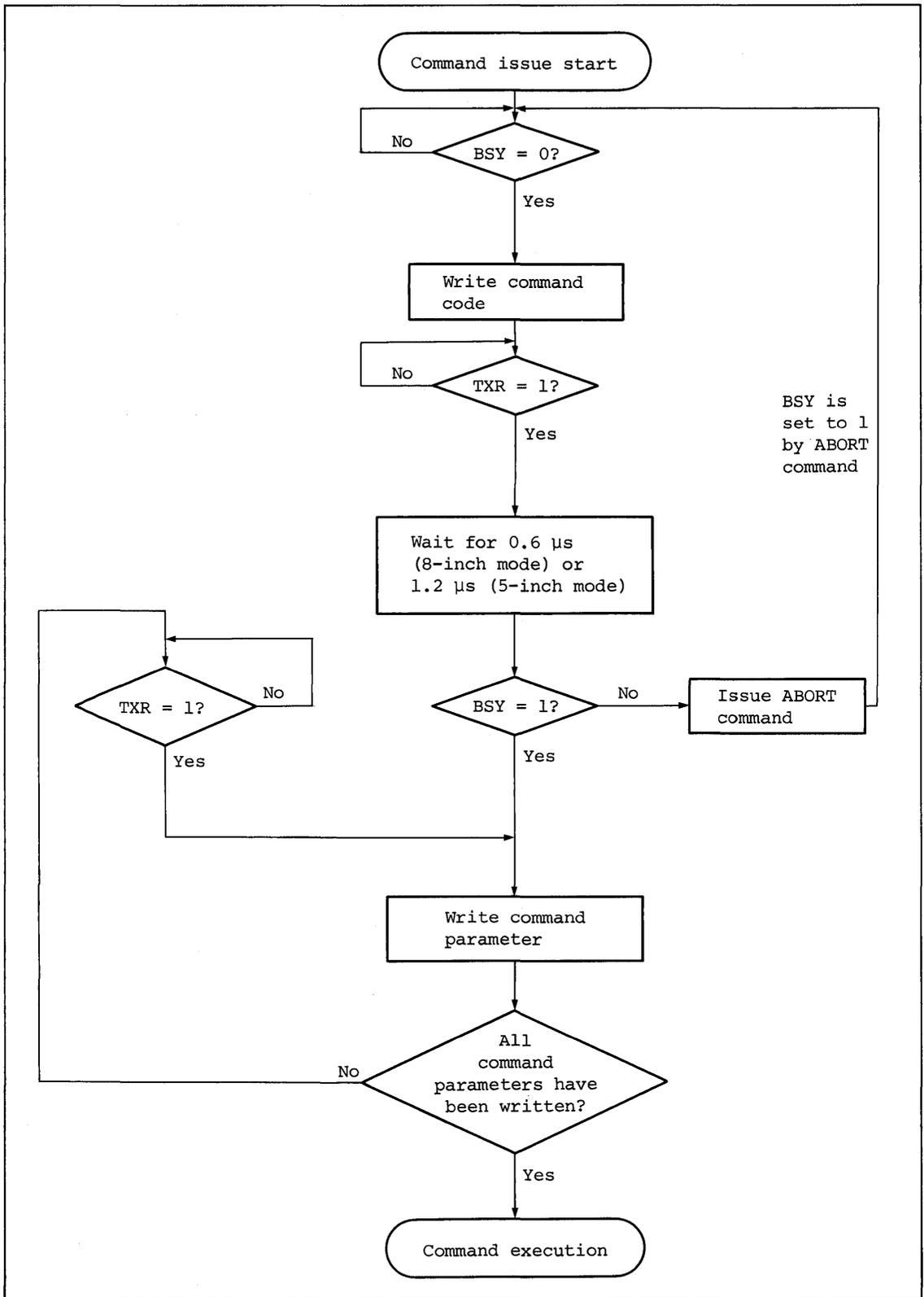
Figure 6-65. ABORT Command Issue Procedure

SECTION 7. VFO CIRCUIT

The VFO circuit (figure 7-1) uses an analog PLL and requires no adjustment and no external components.

7.1 VFO SYNCHRONIZATION

The VFO synchronizes with the following serial data rates:

    FM : 125, 150, 250 kbps
    MFM: 250, 300, 500 kbps

To synchronize to the data transferred at 150 kbps in FM or 300 kbps in MFM, a 19.2 MHz clock must be input to CLK (pin 25) with 8"/$\overline{5}$" (pin 6) tied low.

7.2 CONTROLLING THE VFO

The VFO changes the loop gain of the PLL (phase locked loop) while synchronizing to the SYNC field. It starts with a high gain to achieve fast synchronization and switches to a low gain to reduce bit jitter (figure 7-2). While not performing a read operation the VFO synchronizes to the FDC's clock, eliminating the need for a multiplexed reference clock input on the RDATA pin (pin 30).

During a read operation, when an internally generated SYNC signal becomes active, the VFO begins to detect an FM/MFM zero pattern on the RDATA (pin 30) input. Until detecting a zero, the VFO synchronizes with the FDC's clock. After detecting one byte of zeros, the VFO starts to synchronize to the RDATA input with high loop gain. Synchronization is completed within 3 bytes in FM mode and 4 bytes in MFM mode, and then the PLL switches to low loop gain. Now the FDC determines whether it should read the data or inform the VFO to resynchronize depending on whether the first non-zero pattern encountered is an address mark or not.
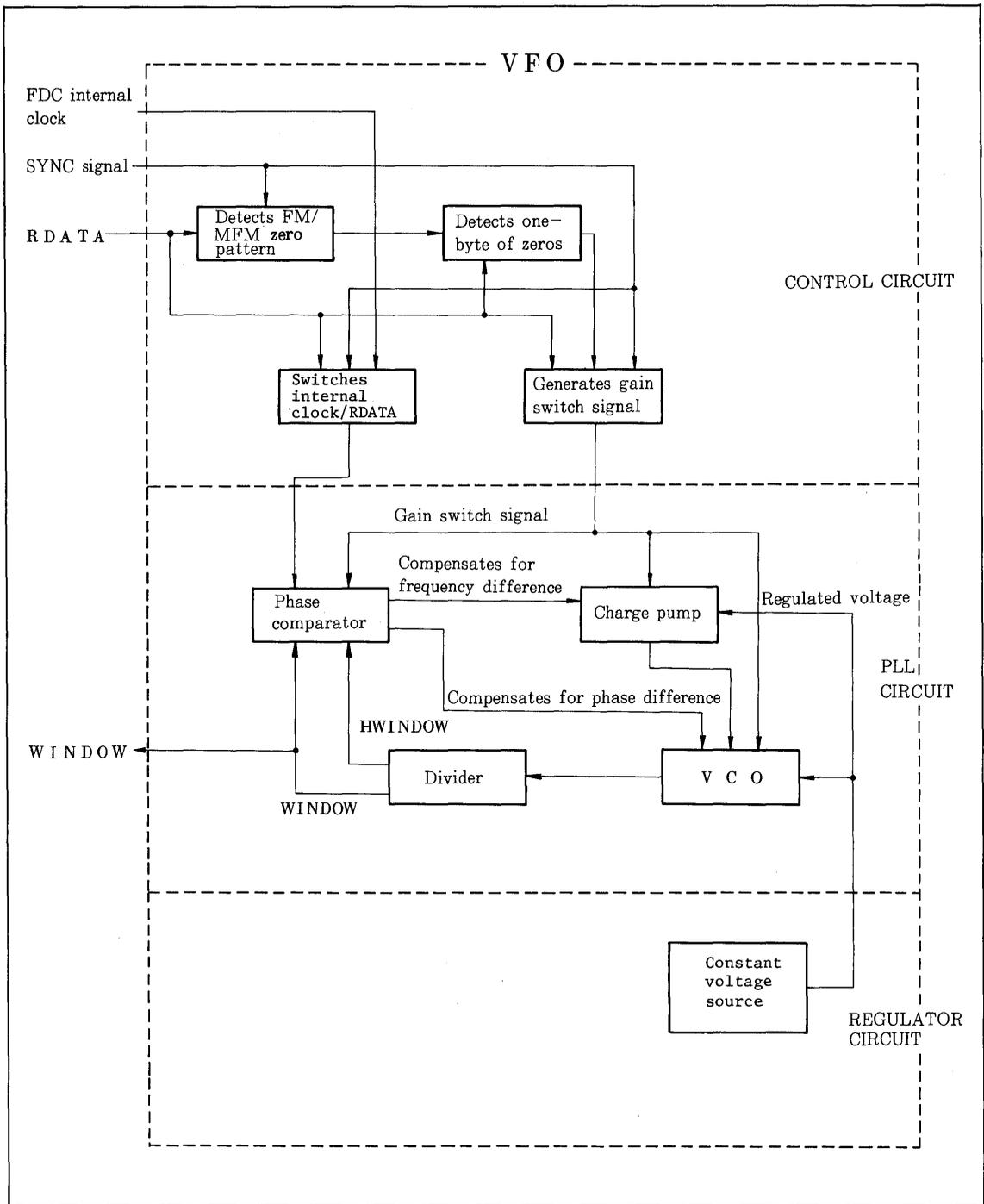
Figure 7-1.   VFO Circuit Block Diagram
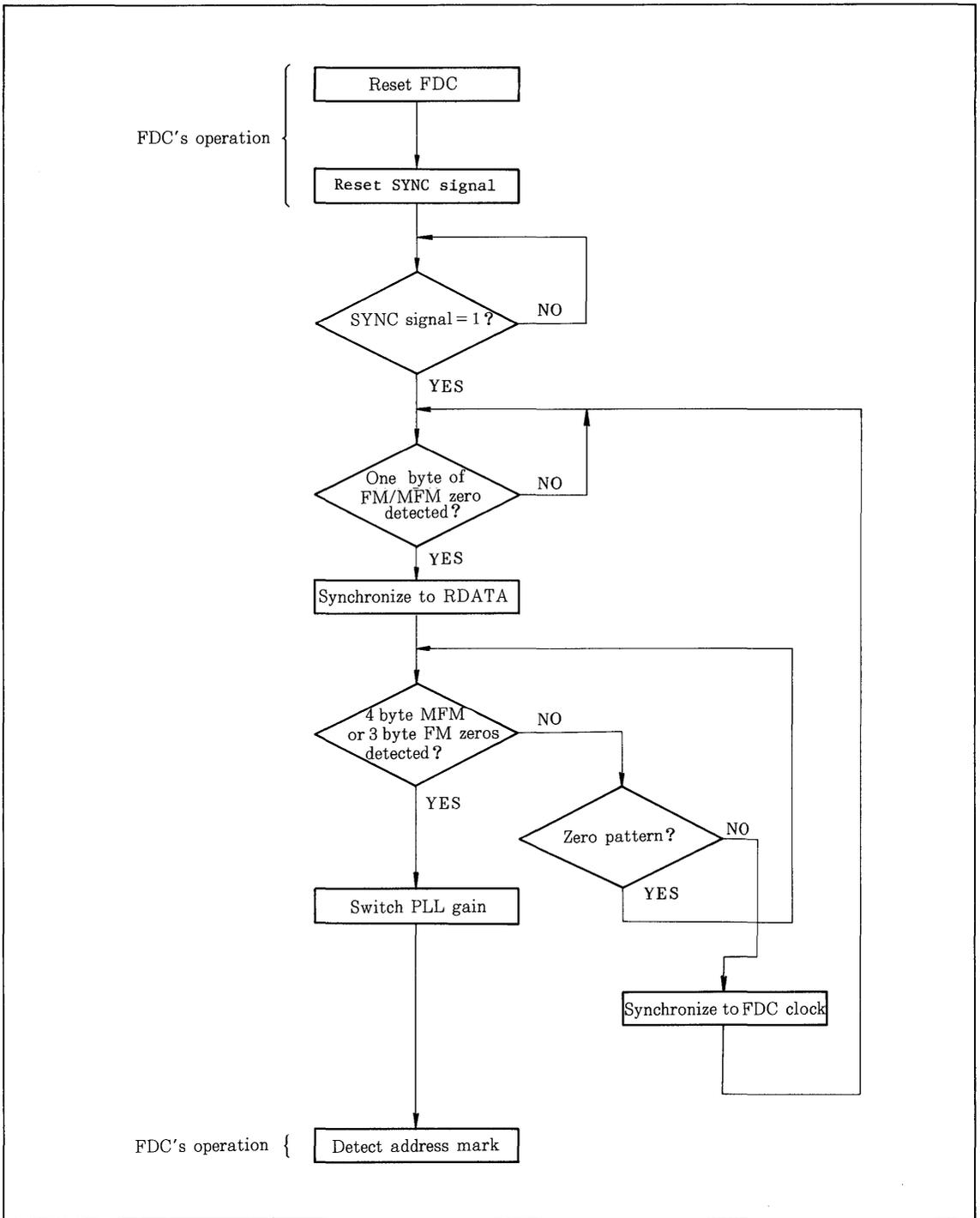
Figure 7-2. VFO Control Flow

7.3   PLL CIRCUIT

This PLL circuit, eliminates the need for a noise-sensitive, lag-lead type
filter and instead employs a new system to compensate for phase and frequency
differences.   In this method, frequency differences are compensated using
phase difference measurements.   A constant current source circuit is used
with the charge pump and the VCO (voltage controlled oscillator) circuits
so that supply voltage variations and noise will not influence the PLL.   The
center frequency of the VCO is 4 MHz.   Separate phase comparators are used
for the SYNC and DATA sections to perform the phase comparisons.   Two clocks
are applied to the phase comparators.   One is a WINDOW clock necessary to
separate the data.   The other is a HWINDOW clock with double the WINDOW
frequency which is generated in the process of generating the WINDOW by
dividing the VCO output.   Phase comparison is performed between the center
of the WINDOW and the RDATA input (figure 7-3).
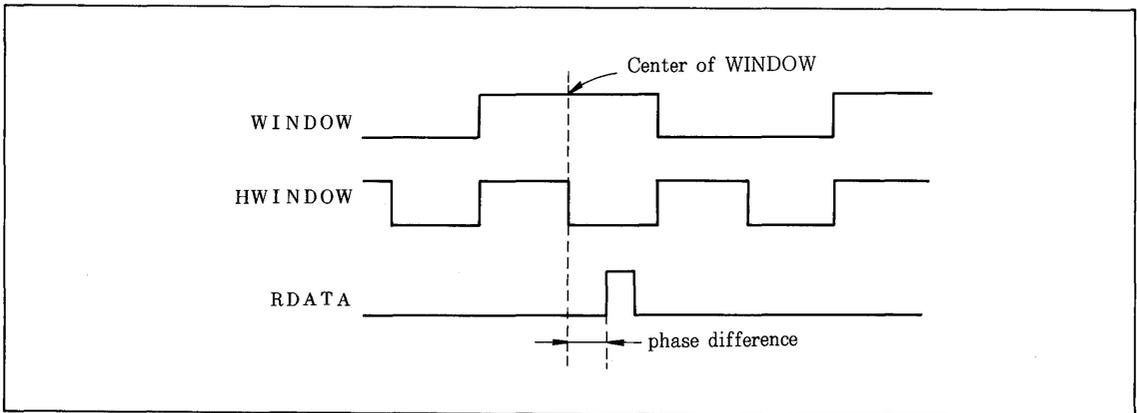
Figure 7-3.   Phase Comparison

SECTION 8. WRITE PRECOMPENSATION CIRCUIT

. Digital precompensation circuit

. Delay time programmable by software

. Delay time independently selectable for inner and outer tracks

. Outer to inner switchover track specifiable

. When auto-precompensation mode is not selected by command SPECIFY 2, the
  precompensation control signals (EARLY, LATE) are output. When auto-
  precompensation mode is selected, the control signals are not output;
  EARLY and LATE are fixed at low level.

. Delay time programmable by 62.5 ns increments (Note)

. Auto-precompensation and precompensation control signals are output in MFM
  mode only

. Range of delay time programmable (in MFM mode)

    250 kbps: 0 - 750 ns

    300 kbps: 0 - 625 ns (Note)

    500 kbps: 0 - 375 ns

When a value beyond this range is specified, FDC may malfunction.

Note: CLK = 19.2 MHz, delay time programmable by 52.1 ns increments at 300 kbps.

SECTION 9.　SYSTEM APPLICATION

9.1　SYSTEM CONFIGURATION

Figure 9-1 shows a typical system configuration using the HD63265 FDC.　By tying
the IFS pin of HD63265 to high or low, the host interface can be directly
connected respectively to a 68- or 80- series 8-bit system bus. A DMAC is used
for data transfer in the DMA mode.　Since the HD63265 has on-chip VFO and
write precompensation circuits, the FDD interface requires an oscillator,
a multiplex decoder circuit for decoding the unit select signals, and a
driver/receiver circuit as external circuits.　All signals other than the
unit select and ready signals can be directly connected to the driver/receiver
circuit.
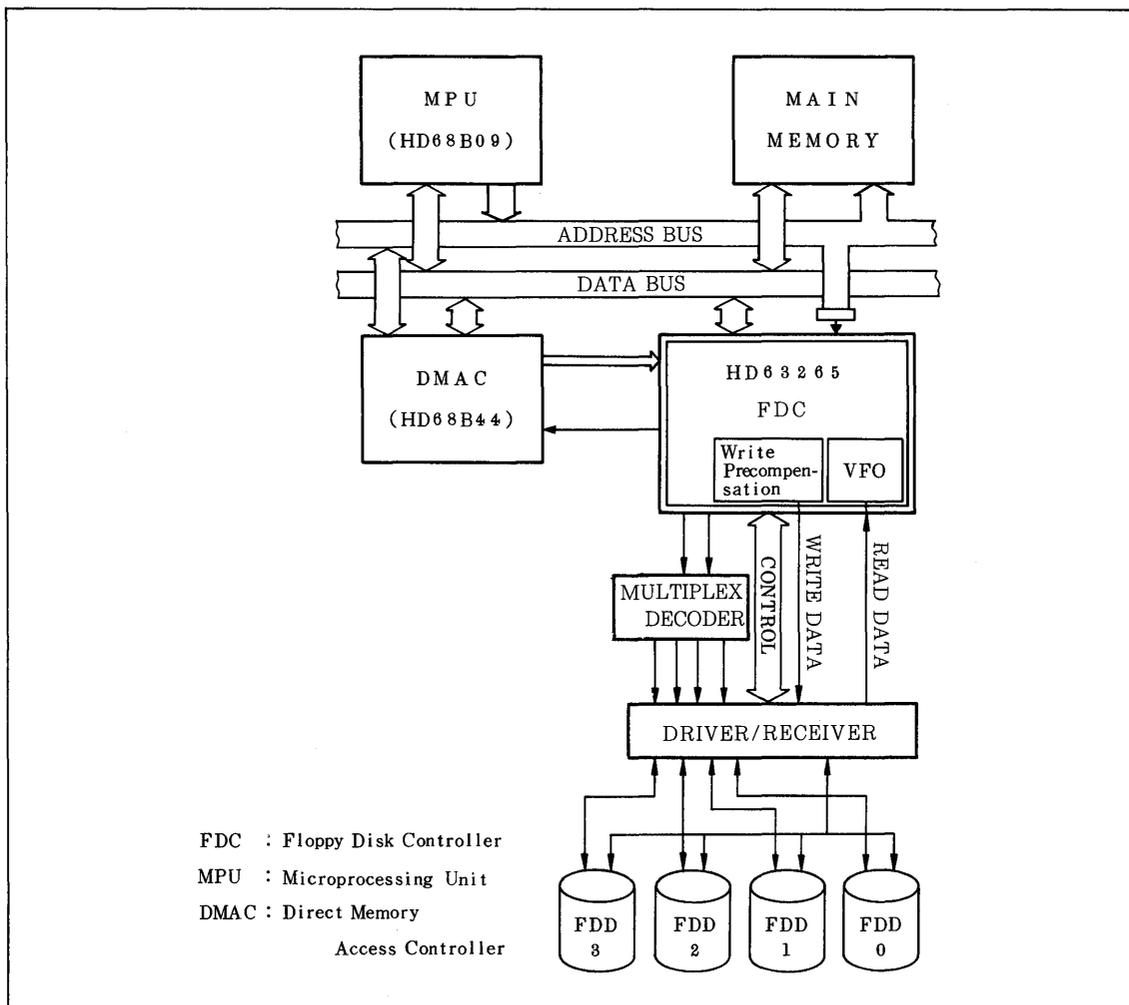
Figure 9-1.　Typical Configuration of a System Using the HD63265

9.2 SYSTEM OPERATION SEQUENCE

Figure 9-2 shows the operation sequence of a system using the HD63265 FDC.
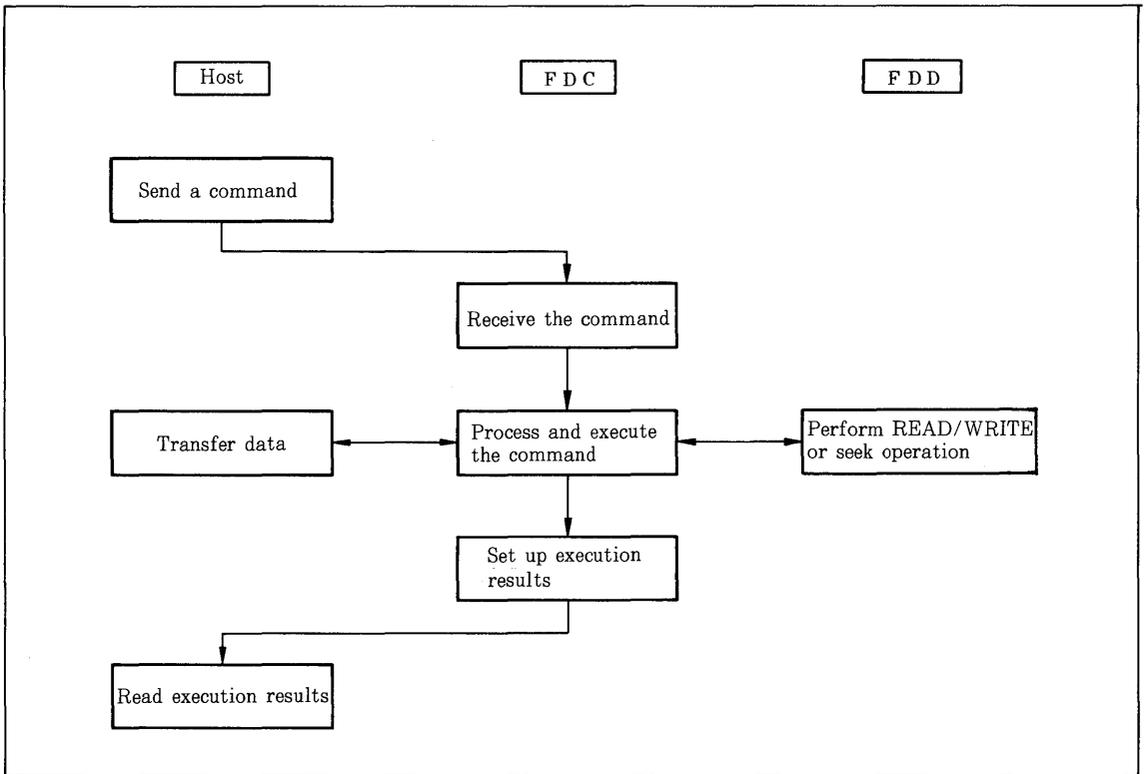
Figure 9-2. Operation Sequence of a System Using the HD63265 FDC

When READ/WRITE commands are executed, data transfer between a host computer and the FDC can be performed in the following two modes.

. DMA mode in which the DMAC transfers data as a bus master

. Non-DMA (PIO) mode in which the CPU transfers data

For operation sequence between the host computer CPU, the DMAC, and the FDC, refer to section 9.6, "Host Interface".

9.3 DATA TRANSFER TIMING

The FDC performs two types of data transfer operations to a floppy disk: one is a WRITE operation which converts 8-bit parallel data from the host memory to serial data for writing to a floppy disk, and the other is a READ operation which converts serial data from a floppy disk to parallel data for transferring to the host memory. Therefore, when designing a system with the FDC, the data transfer timing of the FDD and the data transfer timing of the system must be coordinated.

9.3.1 READ Operation

Figure 9-3 shows the READ operation timing.
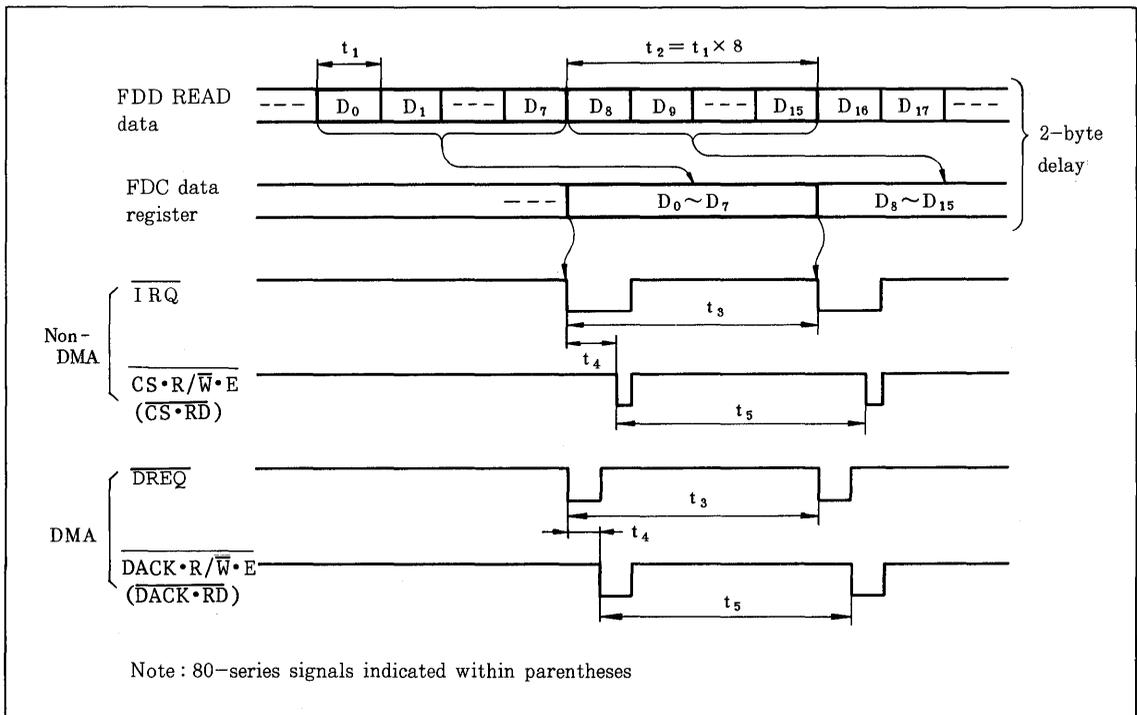
Figure 9-3. READ Operation Timing

The serial data transfer rate is selected by the input level of the 8"/5" pin and also by the FM/MFM mode. The above timings, t_1 through t_5, vary depending on the serial data rate. Table 9-1 shows their variations.

9.3.2   WRITE Operation

Figure 9-4 shows the WRITE operation timing.
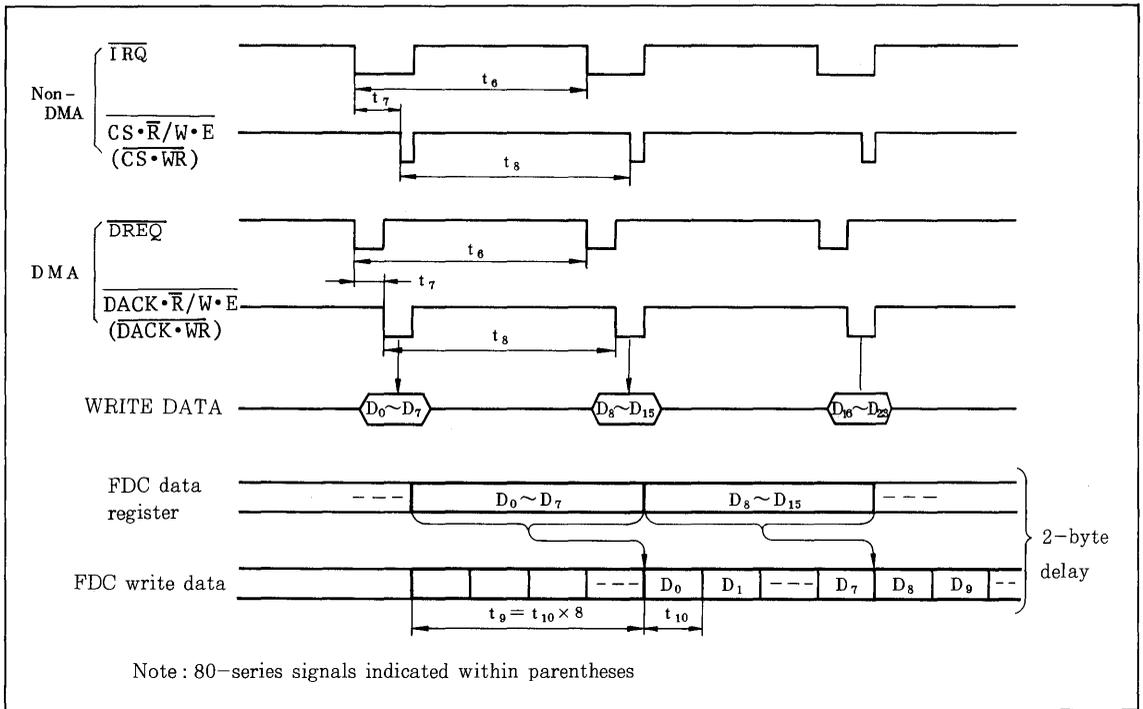
Figure 9-4.   WRITE Operation Timing

As in the case of the READ operation, the above timings t_6 through t_{10} vary depending on the serial data rate.   Table 9-1 show their variations, also.

9.4   DATA TRANSFER COMPLETION TIMING

During data transfer, the data transfer is completed by asserting the $\overline{DEND}$ (transfer completion) signal.   The requirement on the $\overline{DEND}$ assertion timing varies depending on whether it is a READ or WRITE operation, whether $\overline{DEND}$ is asserted in the middle or at the end of a sector, and what the data transfer rate is.   The following shows the $\overline{DEND}$ signal assertion timing for each case.

9.4.1 $\overline{DEND}$ Signal for READ

$\overline{DEND}$ Signal in the Middle of a Sector: Figure 9-5 shows the $\overline{DEND}$ signal assertion timing in the middle of a sector.   If the $\overline{DEND}$ signal is asserted within t_{11} of a data transfer request made by $\overline{IRQ}$ or $\overline{DREQ}$, further transfer requests do not occur after transferring the data requested by $\overline{IRQ}$ or $\overline{DREQ}$. Table 9-2 shows the range of t_{11} depending on the data transfer rate.
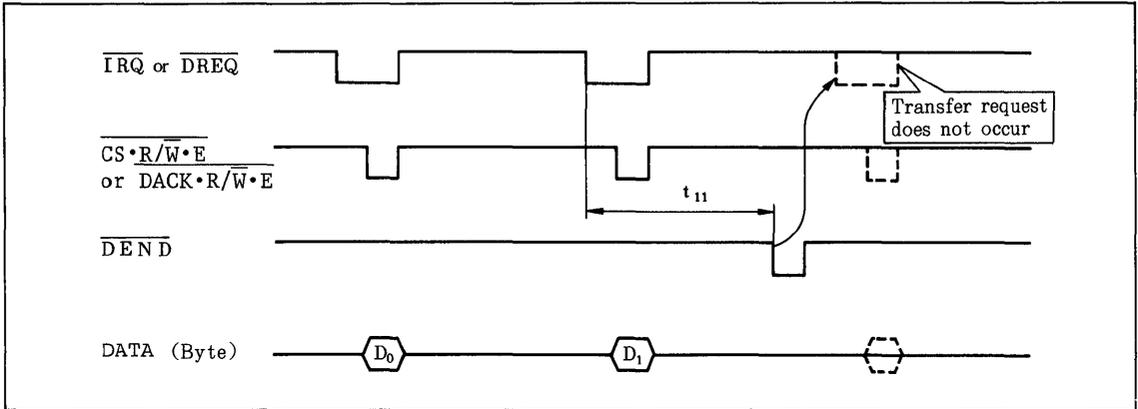
Figure 9-5. $\overline{\text{DEND}}$ Signal Assertion Timing in the Middle of a Sector

$\overline{\text{DEND}}$ Signal at the End of a Sector: Figure 9-6 shows the $\overline{\text{DEND}}$ signal assertion timing at the last byte of a sector.   For transfer request of the last byte of a sector, asserting the $\overline{\text{DEND}}$ signal within t_{12} (see Table 9-2) completes command execution for the sector.
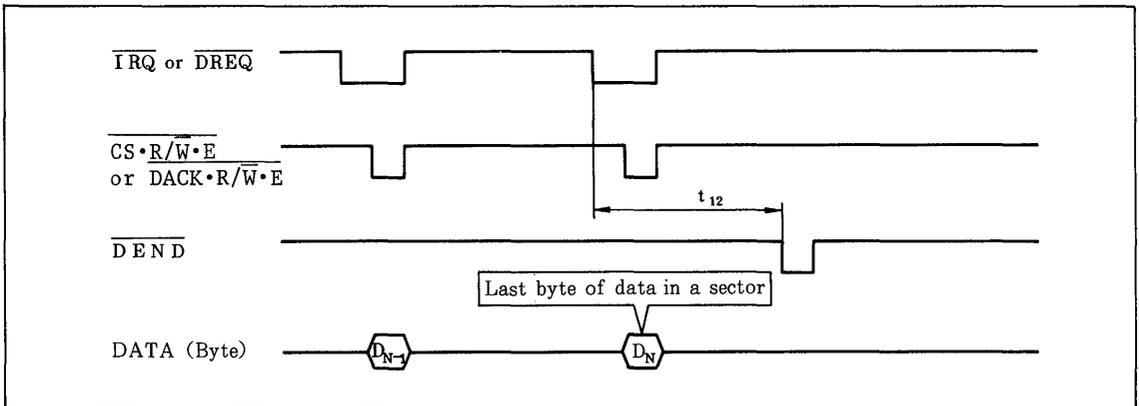
Figure 9-6. $\overline{\text{DEND}}$ Signal Assertion Timing at the Last Byte of a Sector

Table 9-1. FDC Data Transfer Timing

	t	8"/5̄" = 1		8"/5̄" = 0		Notes
		MFM	FM	MFM	FM	
Read	t1	2 μs	4 μs	4 μs	8 μs	1
	t2	16 μs	32 μs	32 μs	64 μs	1
	t3	16 μs	32 μs	32 μs	64 μs	1
	t4	≤11 μs	≤27 μs	≤22 μs	≤54 μs	2
		≤7 μs	≤21 μs	≤15 μs	≤43 μs	3
	t5	16 μs	32 μs	32 μs	64 μs	1
Write	t6	16 μs	32 μs	32 μs	64 μs	4
	t7	≤10 μs	≤26 μs	≤20 μs	≤52 μs	4
	t8	16 μs	32 μs	32 μs	64 μs	4
	t9	16 μs	32 μs	32 μs	64 μs	4
	t10	2 μs	4 μs	4 μs	8 μs	4

Notes 1. For commands READ DATA, READ DELETED DATA, READ ERRONEOUS DATA, READ LONG, COMPARE EQUAL, COMPARE LOW OR EQUAL, and COMPARE HIGH OR EQUAL.

   2. For commands READ DATA, READ DELETED DATA, READ ERRONEOUS DATA, and READ LONG.

   3. For commands COMPARE EQUAL, COMPARE LOW OR EQUAL, and COMPARE HIGH OR EQUAL.

   4. For commands WRITE DATA, WRITE DELETED DATA, and WRITE LONG.

Table 9-2. $\overline{\text{DEND}}$ Signal Assertion Timing

		t	8"/5̄" = 1		8"/5̄" = 0		Notes
			MFM	FM	MFM	FM	
Read	Middle of a sector	t11	≤11 μs	≤27 μs	≤27 μs	≤59 μs	2
	Middle of a sector	t11	≤7 μs	≤21 μs	≤15 μs	≤45 μs	3
	End of a sector	t12	≤32 μs	≤64 μs	≤64 μs	≤128 μs	2
Write	Middle of a sector	t13	≤11 μs	≤27 μs	≤27 μs	≤59 μs	4
	End of a sector	t14	≤32 μs	≤64 μs	≤64 μs	≤128 μs	4

Notes: See table 9-1.

$\overline{\text{DEND}}$ signal assertion at the end of a sector has no effect on COMPARE commands.

9.4.2 $\overline{\text{DEND}}$ Signal for WRITE

$\overline{\text{DEND}}$ Signal in the Middle of a Sector: If $\overline{\text{DEND}}$ is asserted in the middle of a sector during a write data transfer, HEX 00 is written in the remaining data area. Figure 9-7 shows the $\overline{\text{DEND}}$ signal assertion timing in the middle of a sector. If the $\overline{\text{DEND}}$ signal is asserted within t_{13} of a data transfer request made by $\overline{\text{IRQ}}$ or $\overline{\text{DREQ}}$, further transfer requests do not occur after the data transfer requested by $\overline{\text{IRQ}}$ or $\overline{\text{DREQ}}$. The variation of t_{13} with respect to the different data transfer rates is shown in table 9-2.
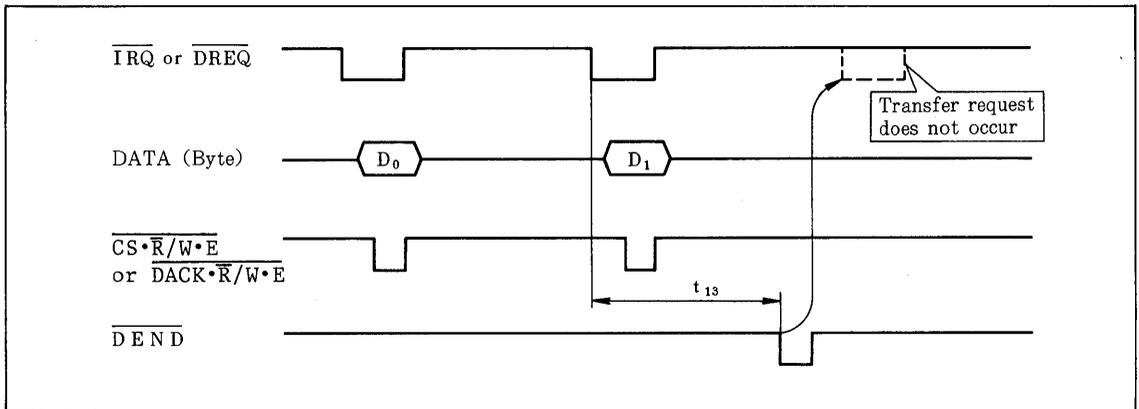
Figure 9-7. $\overline{\text{DEND}}$ Signal Assertion Timing in the Middle of a Sector

$\overline{\text{DEND}}$ Signal at the End of a Sector: Figure 9-8 shows the $\overline{\text{DEND}}$ signal assertion timing at the last byte of a sector. For transfer request of the last byte of a sector, asserting the $\overline{\text{DEND}}$ signal within t_{14} completes command execution for the sector. The variation of t_{14} with respect to the different data transfer rates is shown in Table 9-2.
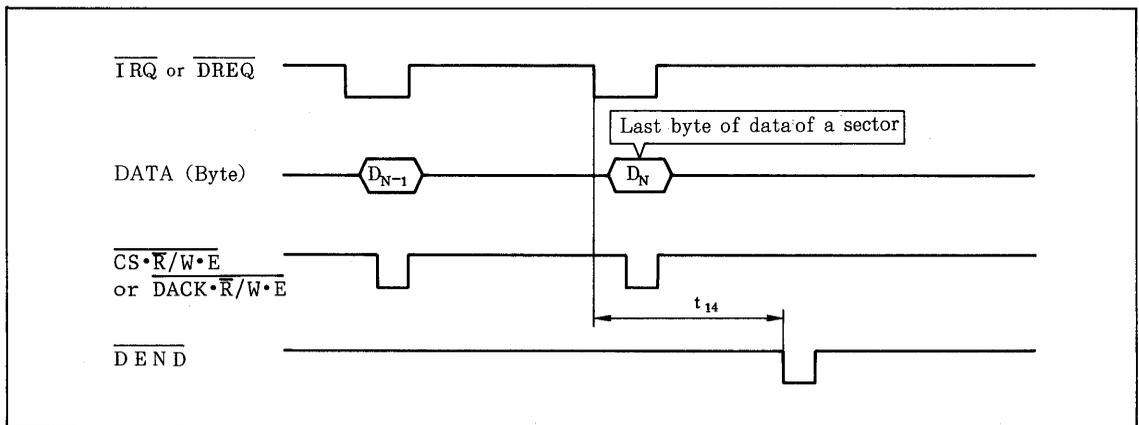
Figure 9-8. $\overline{\text{DEND}}$ signal Assertion Timing at the Last Byte of a Sector

9.5 FDC CONTROL

9.5.1 FDC Operating States

The FDC has three operating states as follows.

1. IDLE state: Usual command wait state

2. SLEEP mode: Low power dissipation mode, and also command wait state

3. Execution state: State during command execution

9.5.2 Interrupt Servicing

The FDC generates the $\overline{IRQ}$ signal in the following four cases:

1. Data read/write request in Non-DMA (PIO) mode

2. Result status read request at the termination of READ/WRITE commands

3. Starting request of CHECK INTERRUPT STATUS command at the termination of a
   SEEK or RECALIBRATE operation

4. Starting request of CHECK INTERRUPT STATUS command when the READY signal
   from an FDD has changed state since it was polled last time.

Thus, a host computer detects $\overline{IRQ}$ of the FDC, reads the status register,
identifies which of the above cases caused the interrupt, and then services
the request, accordingly.

9.6 HOST INTERFACE

The following examples show how to connect the FDC to the 80-series and
68-series 8-bit bus systems.

9.6.1 80-Series 8-Bit Bus System

Figure 9-9 shows a typical FDC interface circuit for a HD64B180-based
80-series 8-bit bus system.
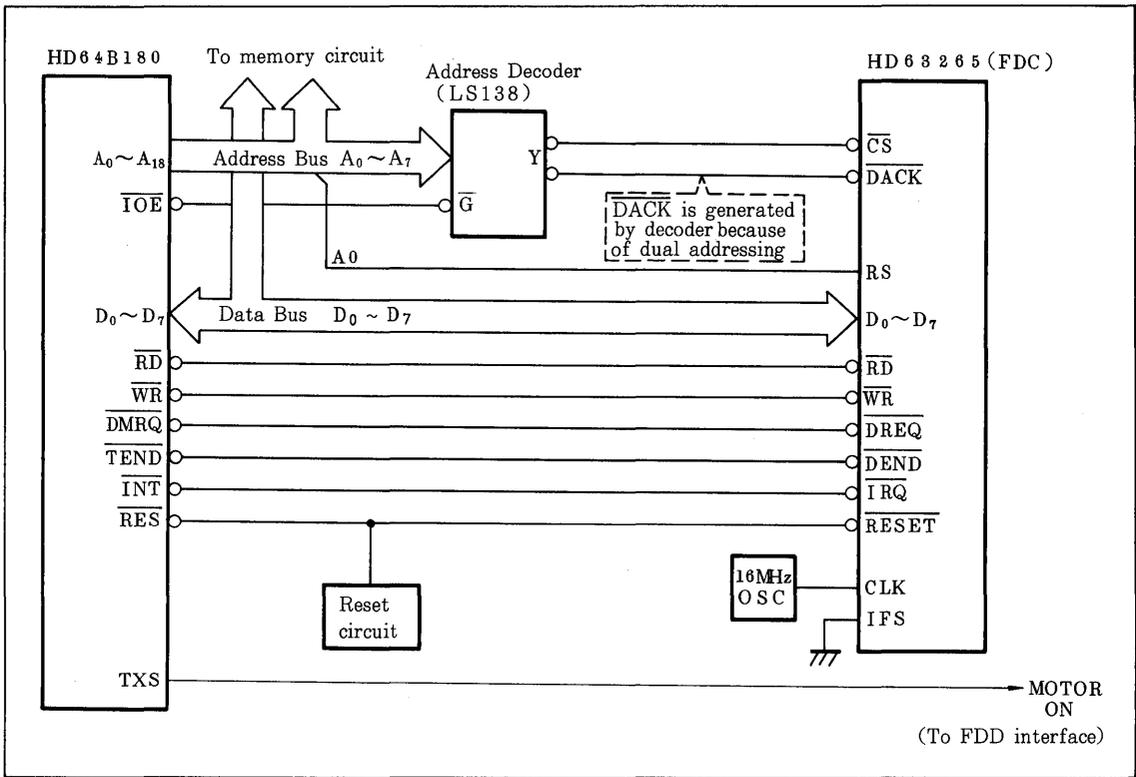
Figure 9-9.   A Typical FDC Interface Circuit Using HD64180 (80-series)

The HD64180 is a CMOS high integration 8-bit microprocessor consisting of a high-speed CPU, memory management unit (MMU), DMA controller, timer, asynchronous serial communication interface (ASCI), and serial I/O port. The MPU interface is based on the 8080 family (Intel) interface; an E clock is provided to enable interface with a 6800 family (Motorola) MPU. In this example, the FDC host interface is set to the 8080 family type by tying the IFS pin to low.

HD64180 Address Space: The HD64180 divides its address space into memory space (512 kbytes) and I/O space (64 bytes). The FDC is assigned to the I/O space by connecting the HD64180 $\overline{IOE}$ pin to the enable ($\overline{G}$) pin of the address decode circuit.

HD64180 I/O Access Timing: Read/Write operations to the internal registers of the HD63265 FDC are synchronized with the $\overline{RD}$, $\overline{WR}$ signals of the 80 series. Therefore, the HD64180 interface should be performed within the specified setup and hold times of the address, $\overline{CS}$ and DATA signals.

Figure 9-10 shows the 80-series Non-DMA (MPU) read/write timing of the HD63265.
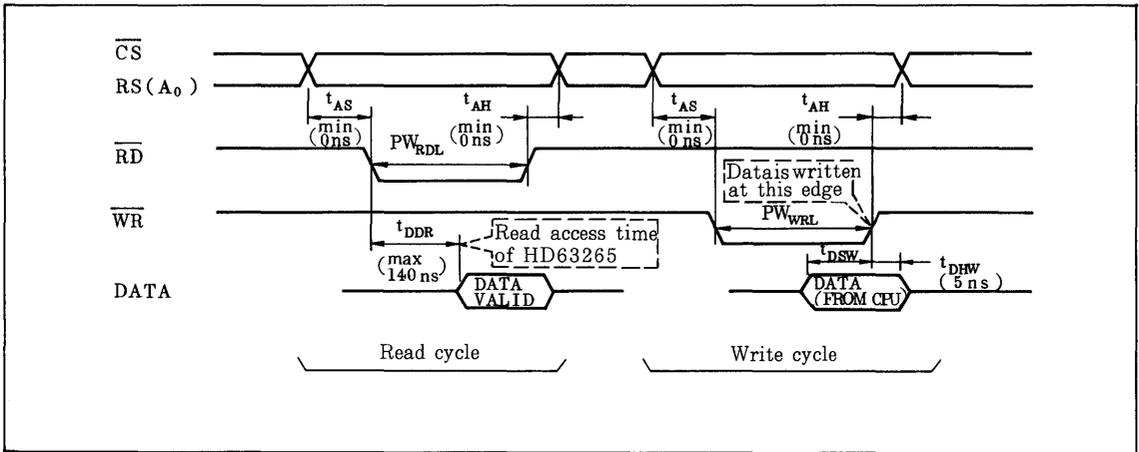
Figure 9-10.   80-Series Non-DMA Read/Write Timing of the HD63265

HD63265 timing specifications require minimum setup and hold times of 0 ns for $\overline{CS}$ with respect to $\overline{RD}$ and $\overline{WR}$. However, the HD64180 may not be able to meet this requirement since the memory and I/O access addresses are decoded externally, respectively enabled by $\overline{ME}$ and $\overline{IOE}$.

For I/O address decoding, since the address signals (A0 to A7) are controlled by $\overline{IOE}$, the resulting I/O access timing of the HD64180 is as shown in figure 9-11. In the I/O read cycle, since $\overline{IOE}$ and $\overline{RD}$ are asserted simultaneously at the falling edge of $\emptyset$ in state T_1, $\overline{CS}$ cannot provide setup time for $\overline{RD}$. However, in the read cycle of the HD63265, even if $\overline{CS}$ is delayed, access time t_{DDR} is only prolonged up to the $\overline{CS}$ delay time. Thus, a sufficient margin between t_{DDR} and PW_{RDL} enables access.
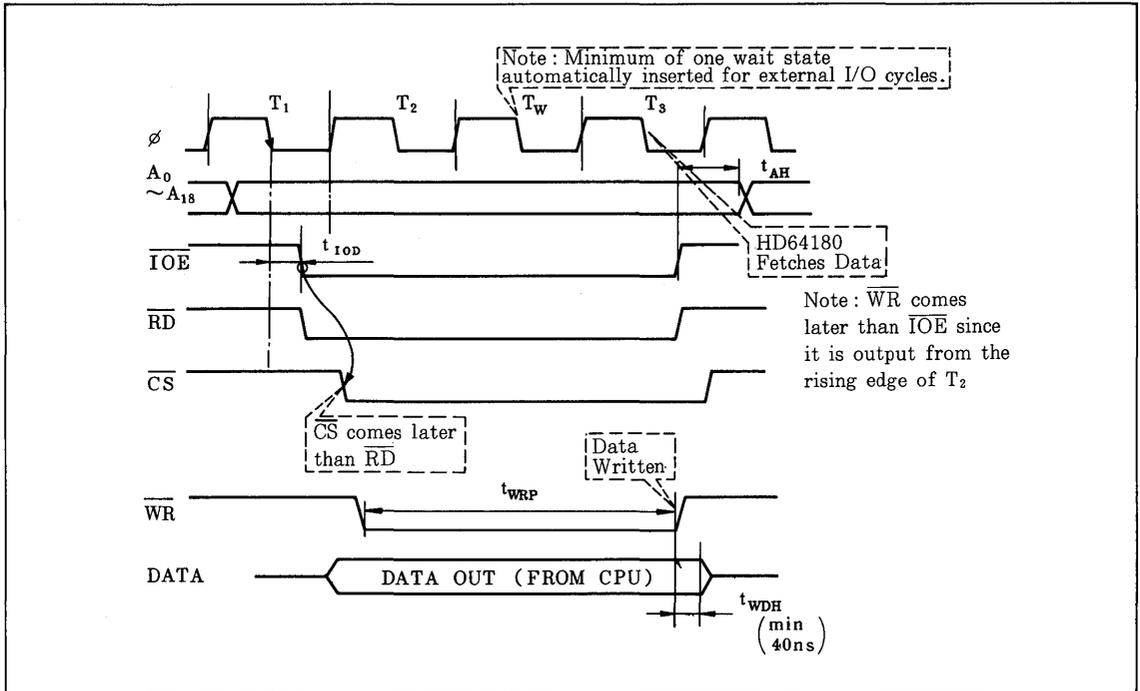
Figure 9-11. HD64180 I/O Access Timing

Moreover, since data is written to the HD63265 at the rising edge of the $\overline{WR}$ pulse, sufficient margin of t_{WRP} enables write as well as read cycles.   (For details, see HD64180 Hardware Application Note.)

DMA Transfer Mode: Since the HD63265 has $\overline{DACK}$ (implicit access), DMA transfer is possible in single addressing mode. However, DMA transfer in the case of HD64180 employs dual addressing mode in which both the I/O and memory addresses are generated respectively in an I/O (FDC) read cycle and memory write cycle. Thus, in response to a DMA request from the FDC, the $\overline{DACK}$ signal is generated by I/O address decoding. Figure 9-12 shows the DMA transfer timing in dual addressing mode.
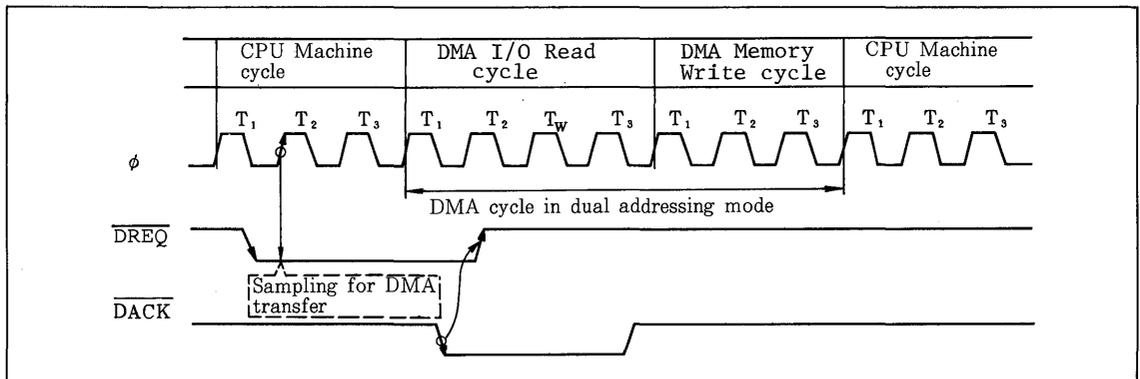
Figure 9-12. DMA Transfer Timing in Dual Addressing Mode

Since the $\overline{\text{DACK}}$ signal of the FDC can replace the $\overline{\text{CS}}$ signal in DMA operation, T_W (wait) state should be inserted to maintain the FDC read or write access time, depending on the frequency of ϕ employed. (For details, refer to HD64180 User's Manual.)

DMA Transfer Sequence: Figure 9-13 and 9-14 show the basic sequences of DMA transfer between the host (HD64180), DMAC (HD64180 built-in DMAC), and FDC (HD63265).
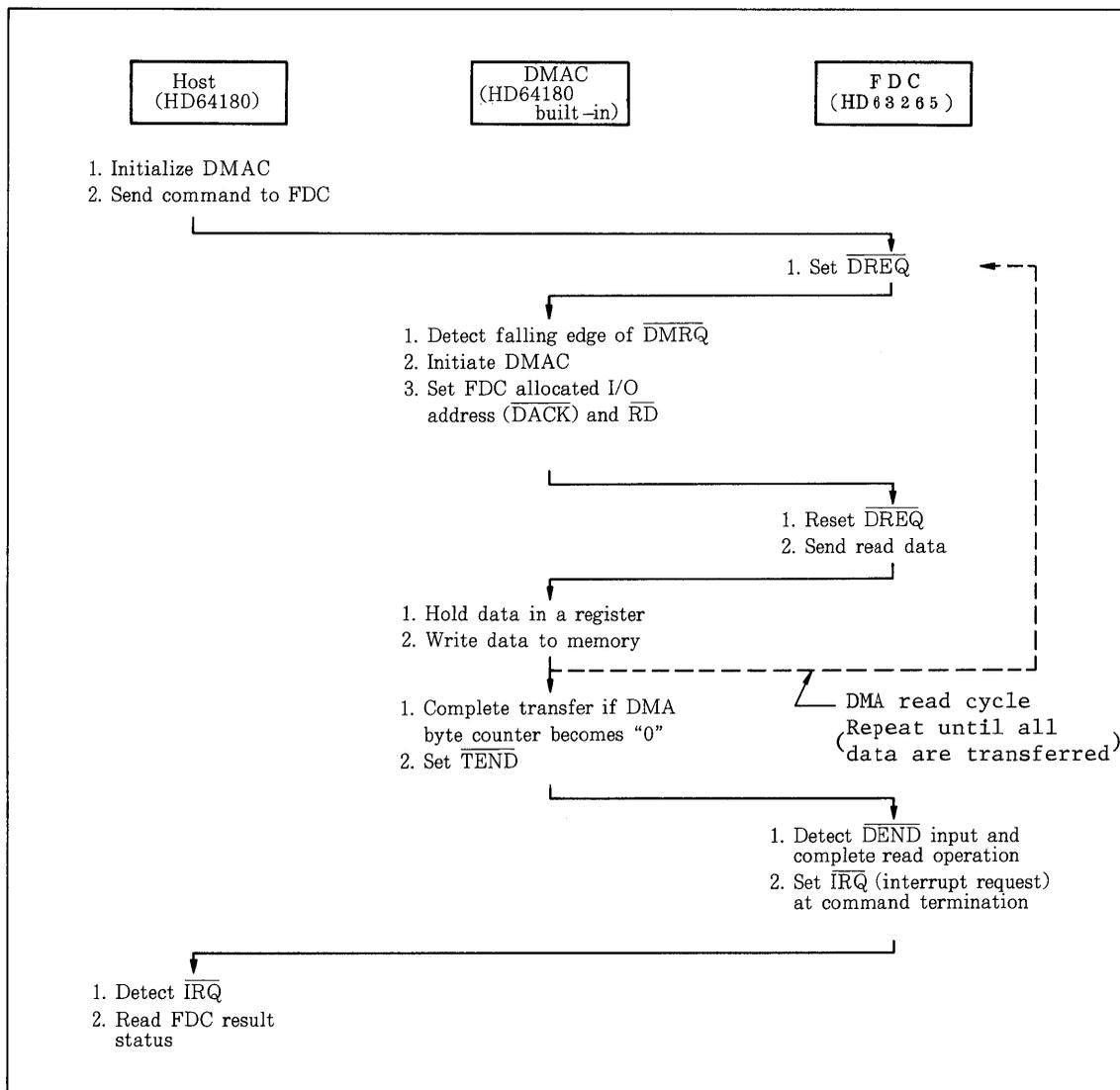
Figure 9-13. DMA Read (FDC → Memory) Sequence
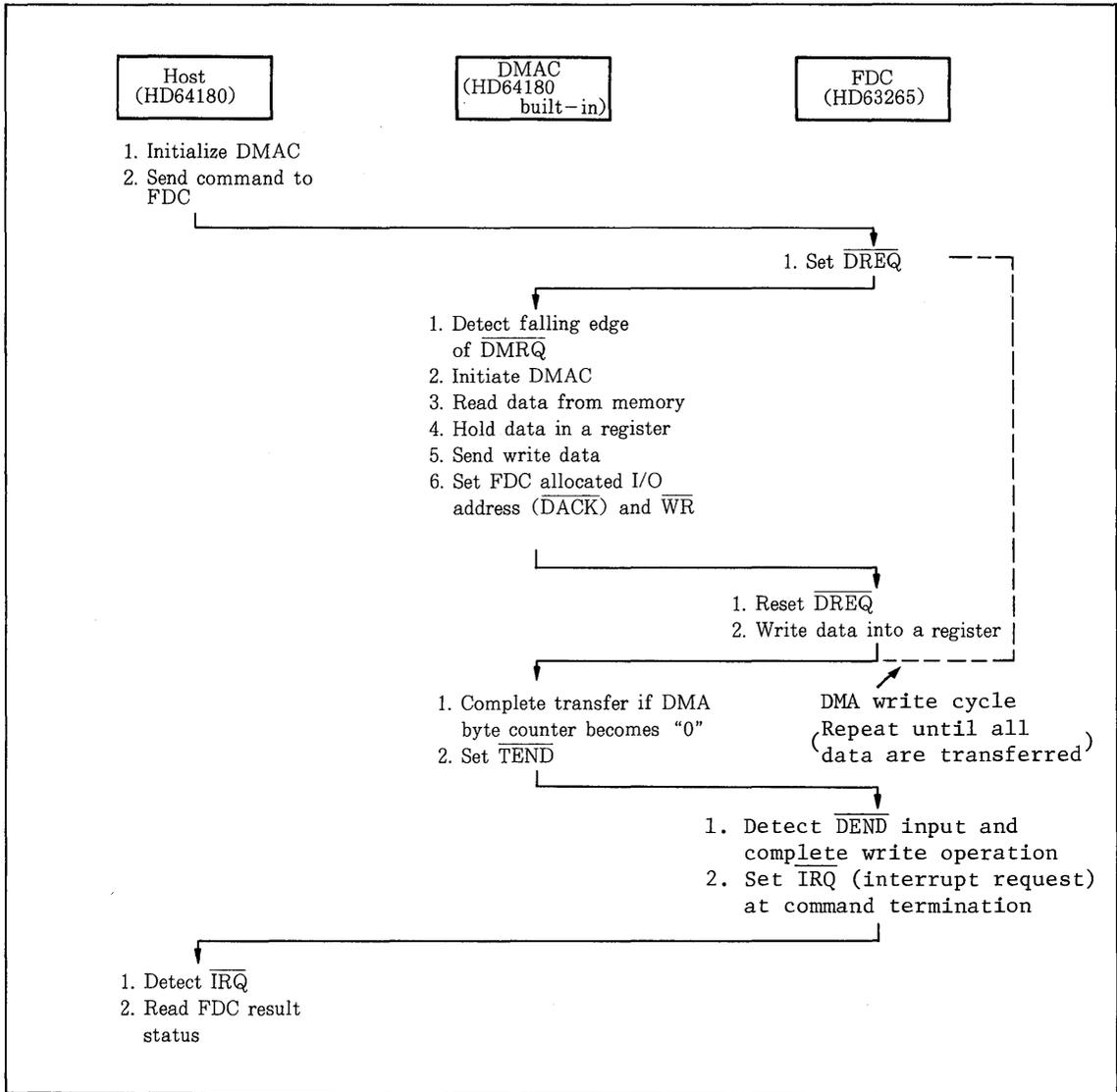
Figure 9-14.   DMA Write (Memory → FDC) Sequence

9.6.2 68-Series 8-Bit Bus System

Figure 9-15 shows a typical FDC interface circuit for a HD64B180-based 68-series 8-bit bus system.

Figure 9-15. A Typical FDC Interface Circuit Using HD64180 (68-series)

Using the E clock of the HD64180 with the IFS pin of the HD63265 tied to high, the FDC host interface is set to the 6800 family type.

The following points should be noted when the host interface of the HD63265 is set to a 6800 interface.

1. $\overline{\text{IRQ}}$ pin of the·HD63265 is an open-drain output in 68-series.

2. R/$\overline{\text{W}}$ logic is inverted between the MPU and DMA modes in 68-series.
    . MPU mode --- R/$\overline{\text{W}}$
    . DMA mode --- W/$\overline{\text{R}}$

Therefore the $\overline{\text{IRQ}}$ output should be tied to a pull-up resistance. A typical circuit for the R/$\overline{\text{W}}$ selection is illustrated in Figure 9-16.

Note: $\overline{ST(DMA)}$ must be generated from ST, $\overline{HALT}$, $\overline{LIR}$ of the HD64180, to indicate the HD64180 operating state (low level indicates DMA transfer operation).

Figure 9-16.   A Typical 68-Series R/$\overline{W}$ Selection Circuit

68-Series Non-DMA Read/Write Timing: For the 68-series, read/write operations to the internal registers of the HD63265 are all synchronized with the E clock. Thus, to interface with the HD64180, the setup and hold times for the Address, $\overline{CS}$, R/$\overline{W}$ and Data signals must be within the specified time limits with respect to the E clock timing.

Figure 9-17 shows the 68-series Non-DMA (MPU) read/write timing of the HD63265.
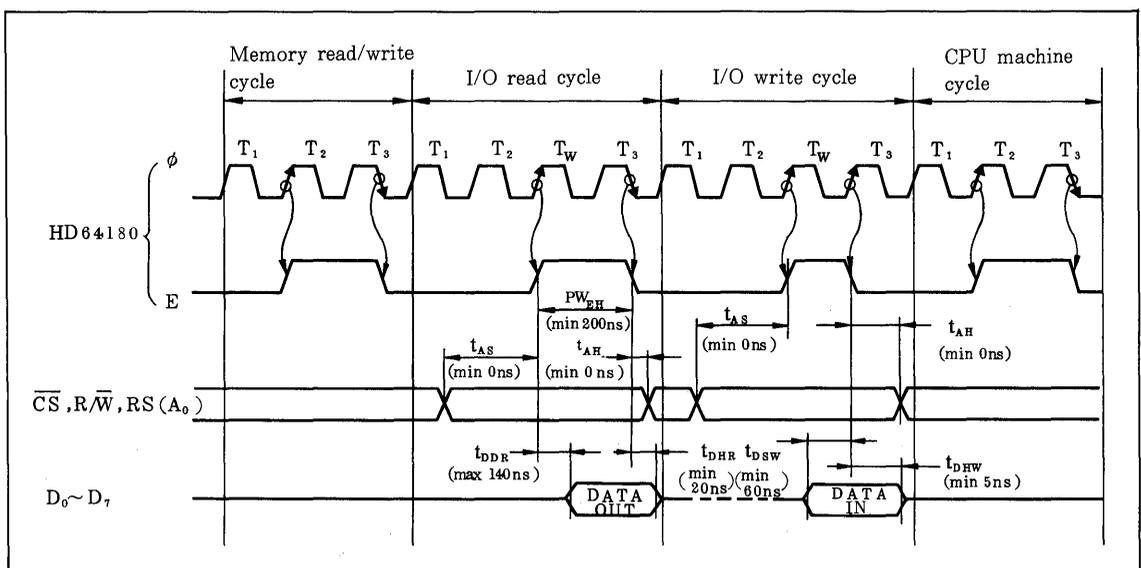
Figure 9-17.   68-Series Non-DMA Read/Write Timing of the HD63265

R/$\overline{\text{W}}$, $\overline{\text{CS}}$ and RS are sampled at the rising edge of the E clock, and a read or write operation is performed depending on their states (if t_{AS} is satisfied). Although hold times (t_{AH}, t_{DHW}) for $\overline{\text{CS}}$ and DATA are required with respect to the E clock falling edge, since the E clock is negated a half cycle earlier than in the I/O read than in the I/O write cycle, the hold time for $\overline{\text{CS}}$ and DATA can be satisfied. Since R/$\overline{\text{W}}$ is a status signal, either $\overline{\text{RD}}$ or $\overline{\text{WR}}$ of the HD64180 should be used to generate R/$\overline{\text{W}}$.

During a HD64180 I/O access, the E clock pulse width (PW_{EH}) can be calculated from the following expression.

$$PW_{EH} = n \cdot T_W + T3/2$$

n: Number of wait states

T_W, T_3: ϕ cycles

HD64B180 requires a 6.0 MHz clock for the ϕ input and PW_{EH} of the HD63265 must be 200 ns minimum. Since PW_{EH} is 250 ns with n = 1, HD63265 requirements are satisfied.

DMA transfer mode: DMA transfer in the 68-series employs a dual addressing mode as in the case of 80-series. Moreover, I/O read/write timing of the 68-series DMA transfer is basically the same as that of the 68-series Non-DMA mode. Note that $\overline{\text{CS}}$ in Non-DMA mode is $\overline{\text{DACK}}$ in DMA mode and both of them have identical timing.

9.7 FDD INTERFACE

Examples of a 5"/3.5" FDD interface and an 8" FDD interface are described below.

9.7.1 5"/3.5" FDD Interface

A typical 5"/3.5" FDD interface circuit requires a driver/receiver circuit and a decoding circuit to decode US0 and US1 of the HD63265 into DRIVE SELECT 0 to DRIVE SELECT 3.

Figure 9-18 shows such a 5"/3.5" FDD interface circuit.
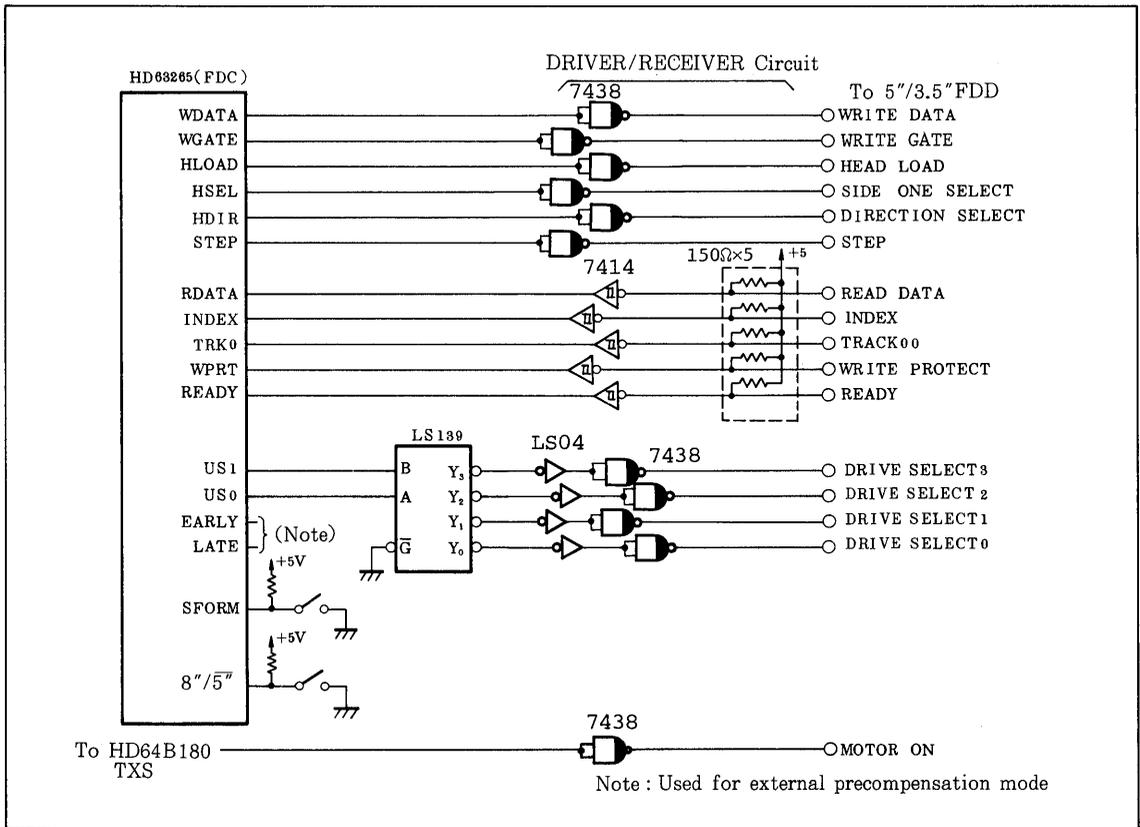
Figure 9-18. A Typical 5"/3.5" FDD Interface Circuit

Selection of Data Transfer Speed: Data can be transferred to the FDD at different data transfer rates as shown in table 9-3, depending on the 8"/5" pin input level and CLK input frequency.

Table 9-3 Data Transfer Rate Selection

CLK input	8"/$\overline{5}$"	FM	MFM
16 MHz	1	250 kbps	500 kbps
	0	125 kbps	250 kbps
19.2 MHZ	0	150 kbps	300 kbps

Data Format Selection: Data format can be selected during the WRITE FORMAT command execution, depending on the SFORM pin input level.

        SFORM = 1   →   IBM Format
        SFORM = 0   →   ECMA (ISO) Format

Disk read/write operations except for formatting can be performed in either format regardless of the SFORM input level.

Decoding of Drive Select Signals: To control 4 FDDs, the drive select signals US0 and US1 of the HD63265 must be decoded into DRIVE SELECT 0 to DRIVE SELECT3 signals. The interface circuit uses an LS139 decoder for this purpose.

MOTOR ON Signal: To interface to 5" and 3.5" FDDs, the MOTOR ON signal is required. Since the HD63265 does not support this signal it must be generated by an external circuit. The circuit uses the HD64B180 TXS (transfer data for serial I/O port) serial I/O port to generate the signal. Alternatively, the MOTOR ON signal can be generated using a dedicated port such as a flip-flop or latch.

Applicable Floppy Disk Drives: The interface circuit design is based on, but not restricted to, the following floppy disk drives.

        5" FDD --- FD-55GFV (TEAC)
      3.5" FDD --- FD-35F-20 (TEAC)

External Precompensation Circuit: In figure 9-18, the FDD interface circuit uses the internal precompensation circuit of the HD63265 where the EARLY and LATE pins are left unconnected. The EARLY and LATE signals are not output in the auto precompensation mode selected by issuing the SPECIFY 2 command. When the SPECIFY 1 command is issued or auto precompensation mode is not selected by the issue of the SPECIFY 2 command, the EARLY and LATE signals of the HD63265 are output (MFM mode only) and the external precompensation mode is selected. A typical external precompensation circuit is shown in figure 10-19.
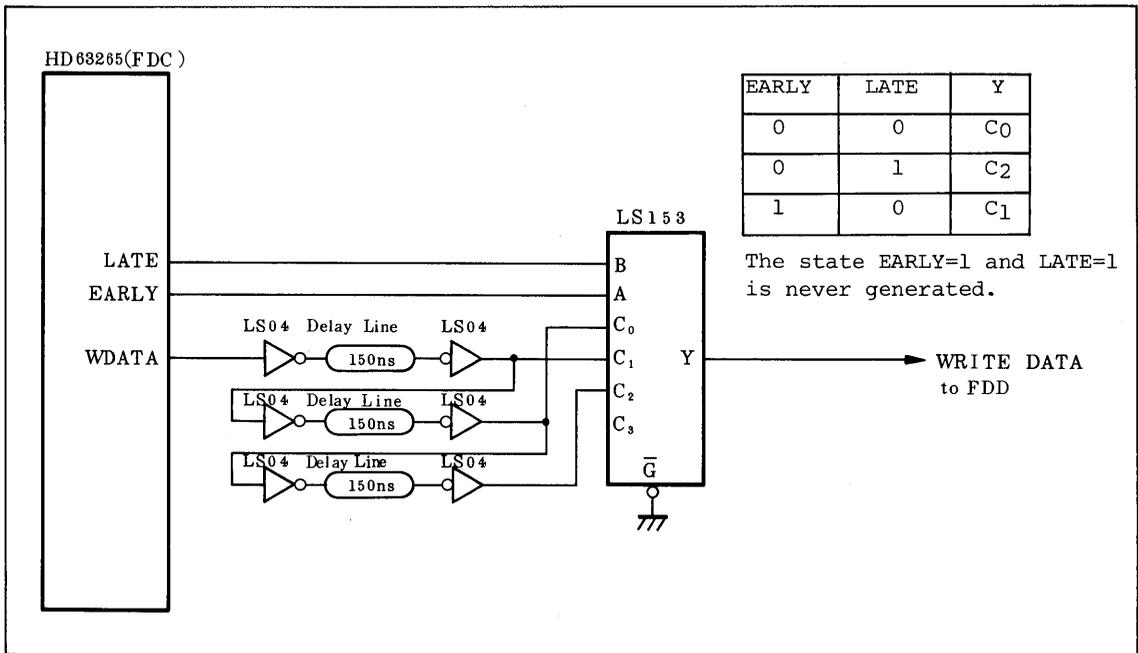
Figure 9-19. A Typical External Precompensation Circuit

The state EARLY=1 and LATE=1 is never generated.

EARLY	LATE	Y
0	0	C_0
0	1	C_2
1	0	C_1

9.7.2 8" FDD Interface

A typical 8" FDD interface circuit requires a driver/receiver circuit and a selector circuit to select READY 0 to READY 3 from a floppy disk drive and generate the READY signal input to the HD63265. Decoding US0 and US1 is not necessary since they interface to 8" floppy disk drives directly. Figure 9-20 shows such an 8" FDD interface circuit.
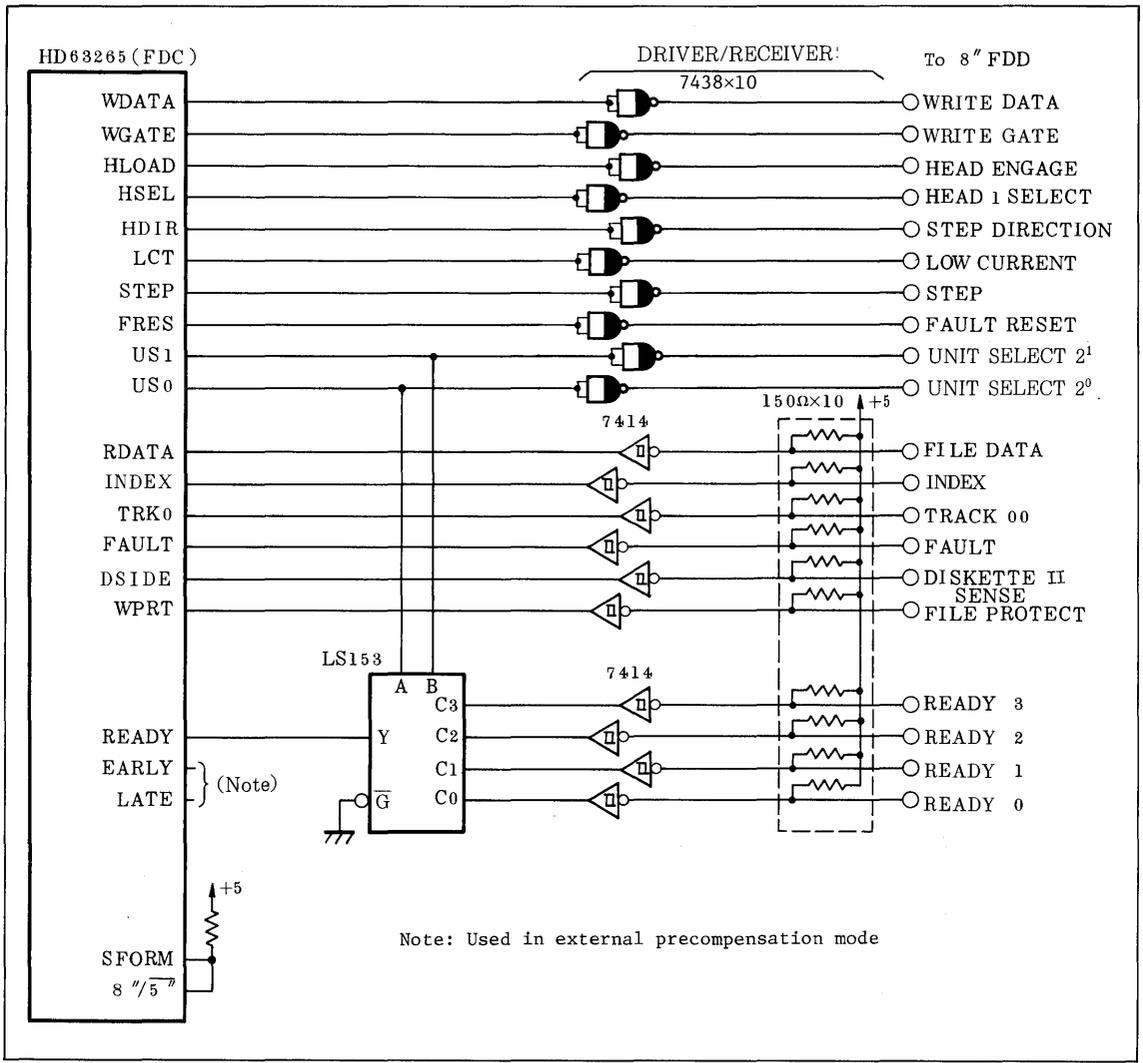
Figure 9-20. A Typical 8" FDD Interface Circuit

Data Transfer Rate Setting: Data transfer rate is set to 250 kbps for FM and 500 kbps for MFM with 8"/5" = 1 and CLK = 16 MHz.

Data Format Selection: IBM format is selected when SFORM = 1. Disk read/write operations other than formatting can be performed regardless of the SFORM input level.

READY Signal Selection: When interfacing four floppy disk drives to the FDC, one of the four drive READY signals (READY 0 to READY 3) is selected by the drive select signals (US0 and US1) and input to the FDC. The interface circuit uses an LS153 multiplexer for this purpose.

Applicable Floppy Disk Drives: The interface circuit design is based on, but not restricted to, the following floppy disk drive:

8" FDD --- YD-180 (Y. E. Data)

9.7.3 FDD Interface Specifications

The following interface specifications should be followed for the 8", 5" and 3.5" FDDs. Table 9-4 lists the driver/receiver and terminator specifications. Figure 9-21 shows the circuit connection to floppy disk drives.

Table 9-4. Driver/Receiver and Terminator Specifications

	Controller	Drive
Line driver	7438 or equivalent	7438 or equivalent
Line receiver	7414 or equivalent	7414 or equivalent
Terminator	150 or 220/330 Ω (input $\leftrightarrow$ +5V)	150 or 220/330 Ω (input $\leftrightarrow$ +5V by the drive furthest from the controller)
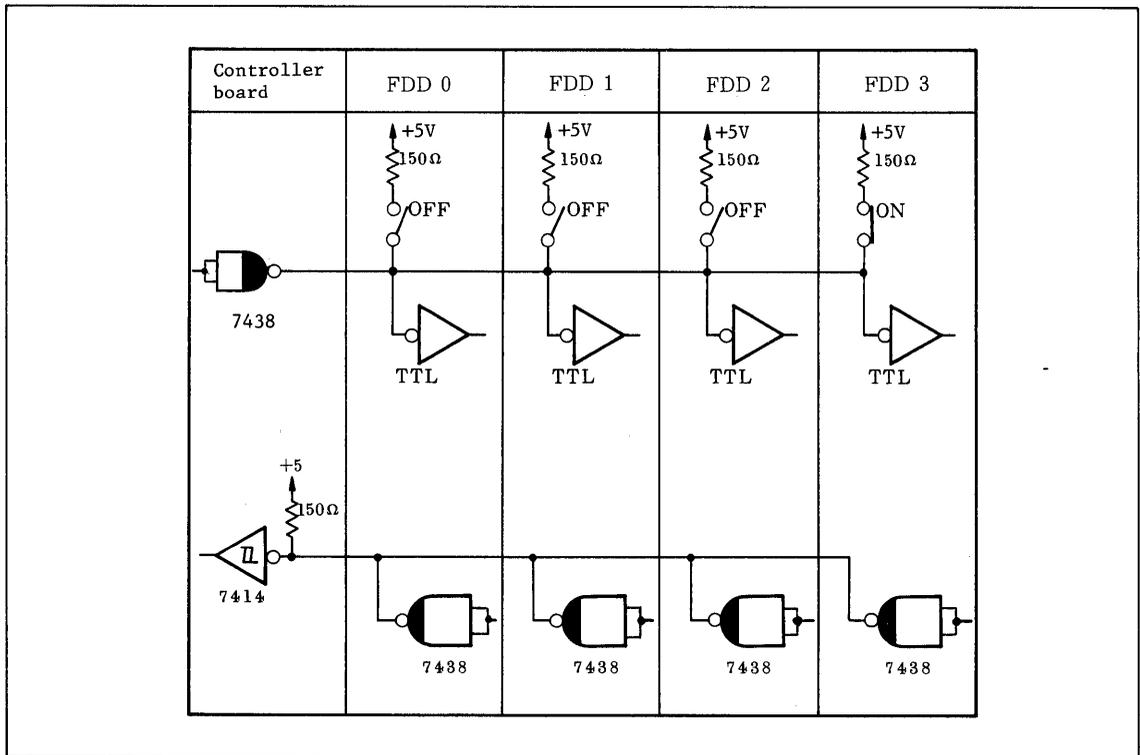
Figure 9-21. Circuit Connection to Floppy Disk Drives (FDDs)

FDD Interface Signals: Tables 9-5 through 9-7 list the 8", 5", and 3.5" FDD interface signals, respectively.

Table 9-5. 8" FDD Interface Signals (YD-180; Y. E. Data)

Pin #	Signal Name	Pin #	Signal Name
1	GND	2	UNIT SELECT 2^1 − N
3	UNIT SELECT 2^0 − N	4	GND
5	DISKETTE II SENSE − N	6	GND
7	INDEX − N	8	GND
9	STEP − N	10	GND
11	LOW CURRENT − N	12	GND
13	WRITE GATE − N	14	GND
15	HEAD 1 SELECT − N	16	GND
17	WRITE DATA − N	18	GND
19	READY 0 − N	20	GND
21	READY 1 − N	22	GND
23	READY 2 − N	24	GND
25	READY 3 − N	26	GND
27	TRACK 00 − N	28	GND
29	FILE PROTECT − N	30	GND
31	STEP DIRECTION − N	32	GND
33	VFO CLOCK − N	34	GND
35	SEPARATED DATA − N (Note)	36	GND
37	DATA AREA − N	38	GND
39	SEPARATED CLOCK − N	40	GND
41	MFM GATE − N	42	GND
43	RESERVED	44	GND
45	RESERVED	46	GND
47	FAULT − N	48	FAULT RESET − N
49	HEAD ENGAGE − N	50	KEY (No pin)

Note: Used as FILE DATA − N by selecting short plug.

Table 9-6. 5" FDD Interface Signals (FD-55GFV, TEAC)

Signal Name	Input/Output	Pin Number		
		Signal	0 V	Notes
HIGH/NORMAL DENSITY	I	2	1	1
IN USE/HEAD LOAD/OPEN	I	4	3	2
DRIVE SELECT 3	I	6	5	
INDEX	O	8	7	
DRIVE SELECT 0	I	10	9	
DRIVE SELECT 1	I	12	11	
DRIVE SELECT 2	I	14	13	
MOTOR ON	I	16	15	
DIRECTION SELECT	I	18	17	
STEP	I	20	19	
WRITE DATA	I	22	21	
WRITE GATE	I	24	23	
TRACK 00	O	26	25	
WRITE PROTECT	O	28	27	
READ DATA	O	30	29	
SIDE ONE SELECT	I	32	31	
READY/DISK CHANGE	O	34	33	3

Notes: 1. For details, refer to the TEAC FD-55GFV manual.
2. This signal is used as the HEAD LOAD signal by setting a jumper switch in the drive.
3. This signal is used as the READY signal by setting a jumper switch in the drive.

Table 9-7. 3.5" FDD Interface Signals (FD-35F; TEAC)

Signal Name	Input/Output	Pin Number Signal	Pin Number 0 V	Notes
DISK CHANGE RESET	I	1	–	1
DISK CHANGE	O	2	–	1
IN USE (or MOTOR ON 2)	I	4	3	2
DRIVE SELECT 3 (or MOTOR ON 1)	I	6	5	
INDEX	O	8	7	
DRIVE SELECT 0	I	10	9	
DRIVE SELECT 1	I	12	11	
DRIVE SELECT 2	I	14	13	
MOTOR ON (0)	I	16	15	
DIRECTION SELECT	I	18	17	
STEP	I	20	19	
WRITE DATA	I	22	21	
WRITE GATE	I	24	23	
TRACK 00	O	26	25	
WRITE PROTECT	O	28	27	
READ DATA	O	30	29	
SIDE ONE SELECT	I	32	31	
READY	O	34	33	

Notes: 1 DISK CHANGE RESET is set to low by connecting to GND. DISK CHANGE
          should be open (For details, refer to the TEAC FD-35F manual).
       2 The HEAD LOAD signal of the controller is used as the IN USE signal.

SECTION 10. CHARACTERISTICS

10.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} (Note 1)	-0.3 to $+7.0$	V
Input Voltage	V_{in} (Note 1)	-0.3 to $V_{CC} + 0.3$	V
Allowable Output Current	$|I_o|$ (Note 2)	5	mA
Total Allowable Output Current	$|\Sigma I_o|$ (Note 3)	80	mA
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to $+150$	°C

Notes: 1. This value is in reference to $V_{SS} = 0$ V

2. The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.

3. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.

4. Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be used under recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

10.2 RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} (Note)	4.75	5.0	5.25	V
Input Low Level Voltage	V_{IL} (Note)	0	–	0.8	V
Input High Level Voltage	V_{IH} (Note)	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

Note: This value is in reference to $V_{SS} = 0$ V

10.3 ELECTRICAL CHARACTERISTICS

10.3.1 DC Characteristics

(V_{CC} = 5.0 V $\pm$5%, V_{SS} = 0 V, T_a = 0 to +70°C unless otherwise noted)

Item		Symbol	Measuring Conditions	Limits Min	Limits Max	Unit
Supply Voltage	V_{CC}, $V_{CC}2$	V_{CC}		4.75	5.25	V
Input High Level Voltage	All Inputs	V_{IH}		2.2	V_{CC}	V
Input Low Level Voltage	All Inputs	V_{IL}		-0.3	0.8	V
Input Leak Current	All Inputs except D0 – D7	I_{in}	V_{in} = 0 to V_{CC}	-2.5	2.5	μA
Three State (Off State) Input Current	D0 – D7	I_{TSI}	V_{in} = 0.4 to V_{CC}	-10	10	μA
Output High Level Voltage	All Outputs except $\overline{IRQ}$ when IFS = 1	V_{OH}	I_{OH} = -400 μA	2.4	–	V
Output Low Level Voltage	All Outputs	V_{OL}	I_{OL} = 1.6 mA	–	0.5	V
Output Leak Current (Off State)	$\overline{IRQ}$ when IFS = 1	I_{LOH}	V_{OH} = V_{CC}	–	10	μA
Input Capacitance	All inputs and outputs	C_{in}	V_{in} = 0 V, T_a = 25°C f = 1.0 MHz	–	15	pF
Current Consumption		I_{CC}	FDC unselected and Disk operation with data transfer in progress	–	40	mA
			FDC in sleep mode	–	10	mA

10.3.2 AC Timing Specification

No.	Item	Symbol	Min	Typ	Max	Unit
1	Clock cycle time	$t_{cyc}C$	50	62.5	80	ns
2	Clock high level width	PW_{HC}	15			ns
3	Clock low level width	PW_{LC}	15			ns
4	Clock falling time	t_{Cf}			20	ns
5	Clock rising time	t_{Cr}			20	ns
6	Read data high level width	PW_{HRDT}	40			ns
7	Read data low level width	PW_{LRDT}	40			ns
8	Write data high level width	PW_{HWDT}		4		$t_{cyc}C$ [2]
9	Index signal high level width	PW_{IDX}	6 [1]			$t_{cyc}C$
10	Fault reset signal high level width	PW_{FRS}	136 [1]		140 [1]	$t_{cyc}C$
11	$\overline{DEND}$ signal low level width	PW_{DEND}	40			ns
12	$\overline{RESET}$ signal low level width	PW_{RES}	28 [1]			$t_{cyc}C$
13	Enable signal cycle time	$t_{cyc}E$	410			ns
14	Enable signal low level width	PW_{EL}	200			ns
15	Enable signal high level width	PW_{EH}	200			ns
16	Enable signal rising time	t_{Er}			20	ns
17	Enable signal falling time	t_{Ef}			20	ns
18	Address setup time	t_{AS}	0			ns
19	Address hold time	t_{AH}	0			ns
20	Data delay time	t_{DDR}			140	ns
21	Data hold time	t_{DHR}	20			ns
22	$\overline{IRQ}$ release time	t_{IRQ}			200	ns
23	Data setup time	t_{DSW}	60			ns
24	Data hold time	t_{DHW}	5			ns
25	$\overline{DREQ}$ signal release time	t_{DRQ}			200	ns
26	$\overline{RD}$ signal low level width	PW_{RDL}	200		1200 [1]	ns
27	$\overline{WR}$ signal low level width	PW_{WRL}	200		1200 [1]	ns
28	$\overline{DACK}$ signal low level width	t_{AA}	200			ns
29	$\overline{DACK}$ signal response time	t_{RA}	0			ns
30	$\overline{RD}$ signal response time 1	t_{RR}	0			ns
31	$\overline{WR}$ signal response time 1	t_{RW}	0			ns
32	Unit selection time	t_{US}		128 [1]		μs
33	STEP signal timing	t_{UP}		32 [1]		μs

AC Specification (cont)

No.	Item	Symbol	Min	Typ	Max	Unit
34	STEP signal high level width	PW_{HSTP}		7^1		μs
35	US0 signal switching time	t_{US0}		128^1		μs
36	US1 signal low level width	t_{US1}		256^1		μs
37	Polling cycle time	$t_{cyc}US$		1024^1		μs
38	Head selection signal switching time	t_{HSL}		2^1		ms
39	FDD selection time	t_{SFD}			3^1	μs
40	EARLY, LATE signal high level width	PW_{ELH}		1^1		μs

Notes: 1. These numbers are doubled for 5.25 inch mode.

2. $t_{cyc}C$ refers to a clock period of the input clock (CLK).
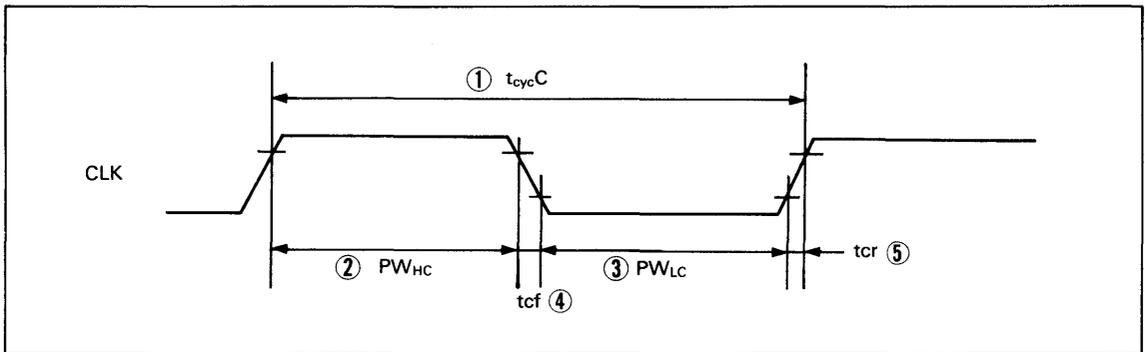
Figure 10-1. Clock Timing
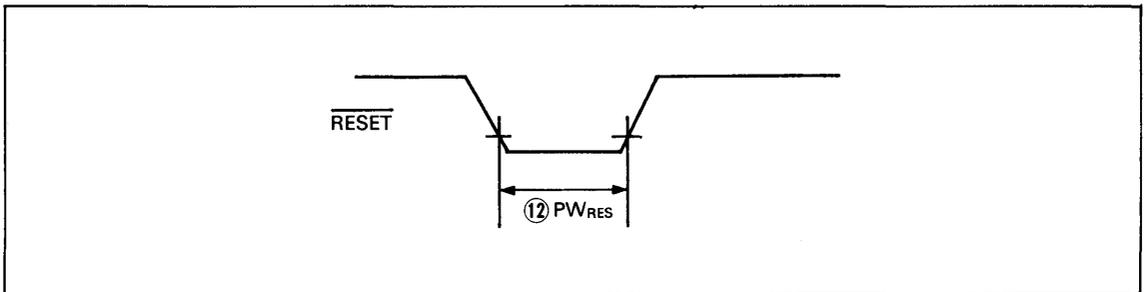
Figure 10-2. Reset Timing
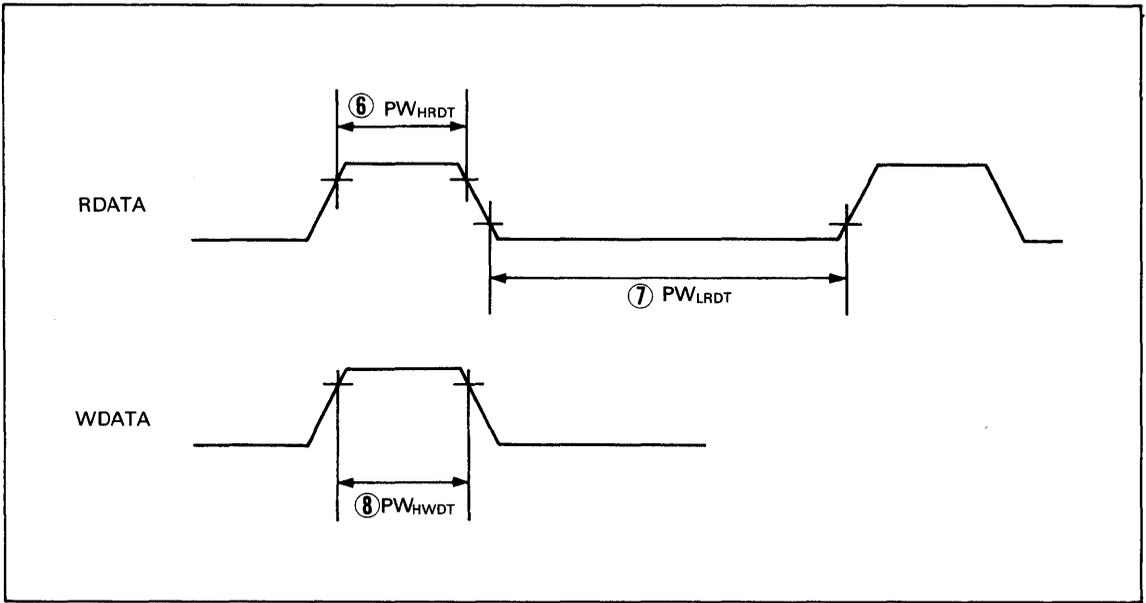
Figure 10-3.   FDD Data Timing
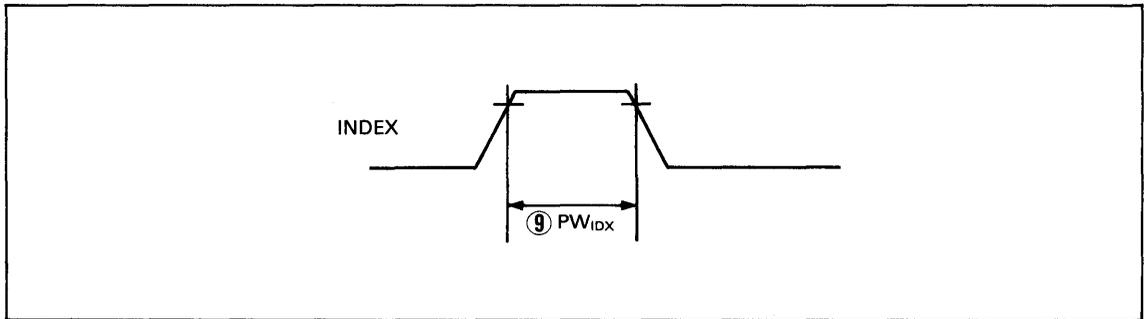
Figure 10-4.   Index Timing
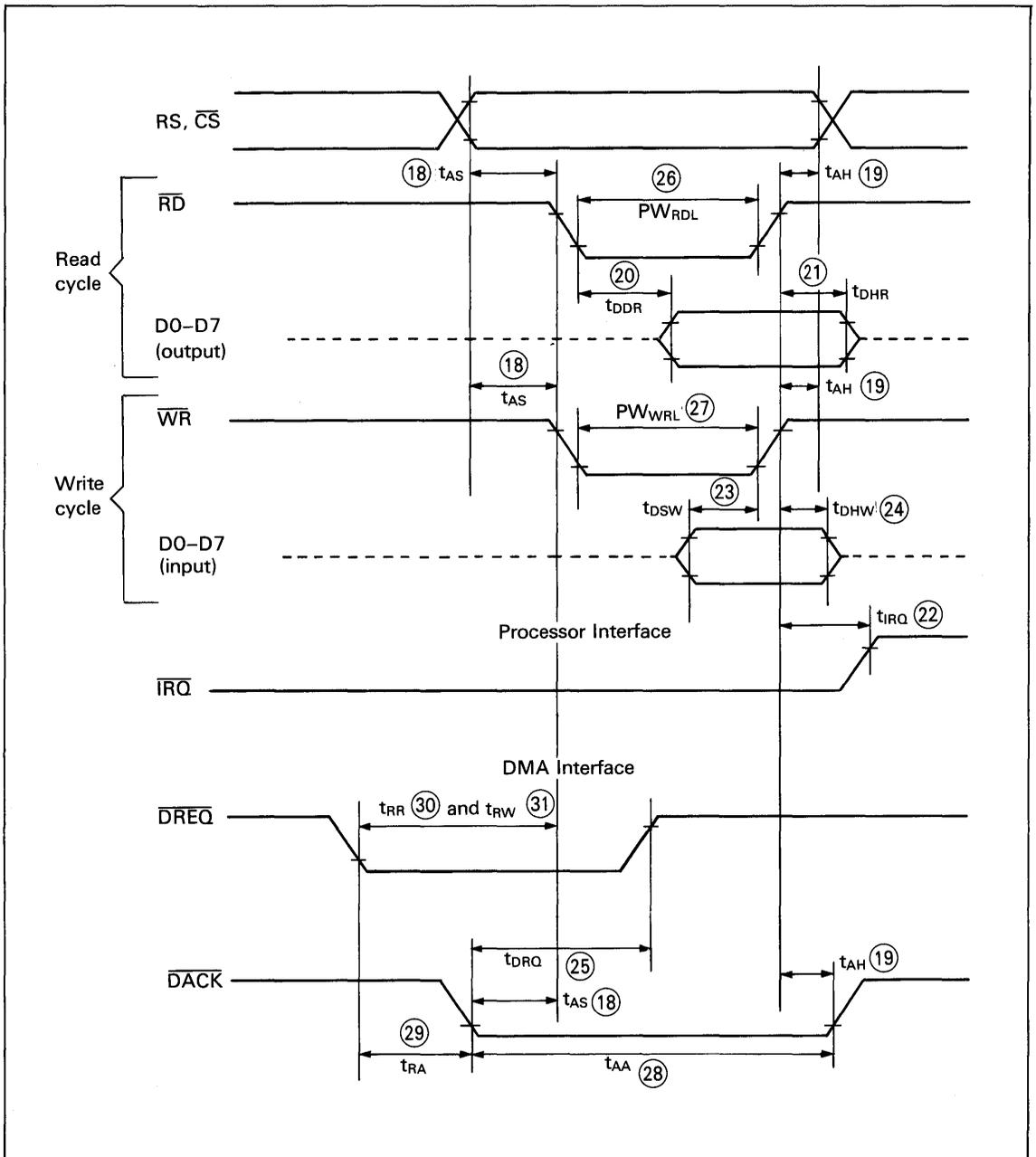
Figure 10-5. Data Transfer Timings for 80XX Interface
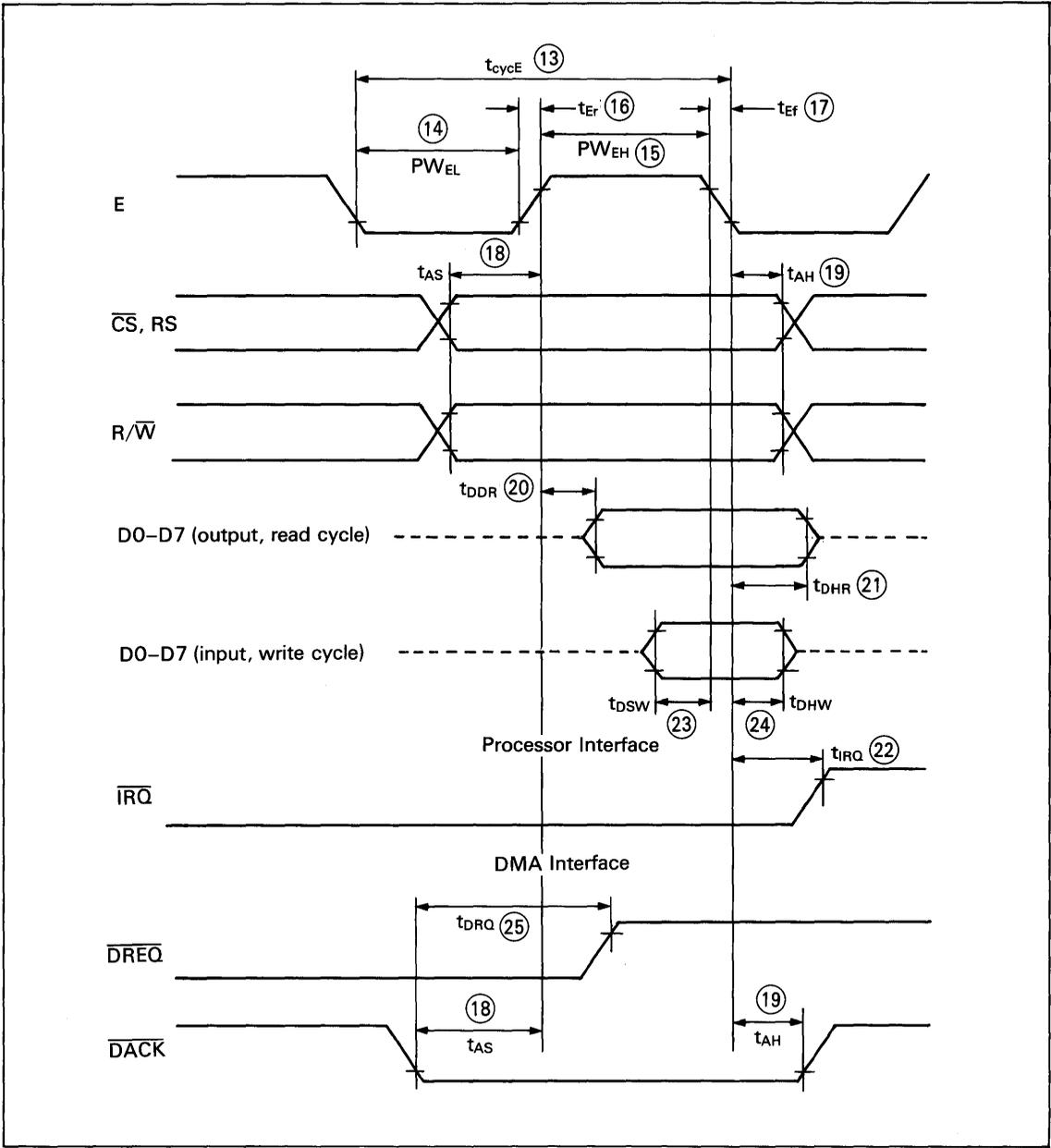
Figure 10-6. Data Transfer Timings for 68XX Interface
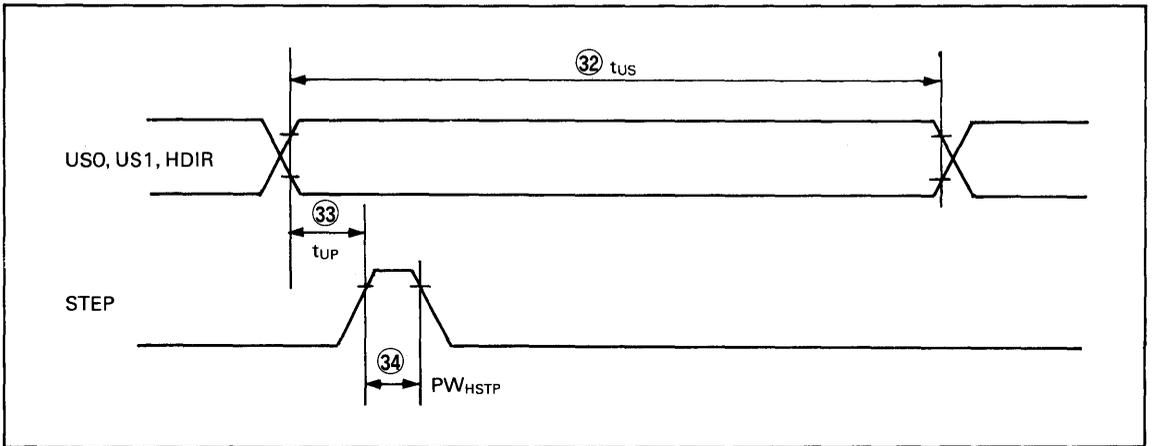
Figure 10-7. Seek, Recalibrate Timing
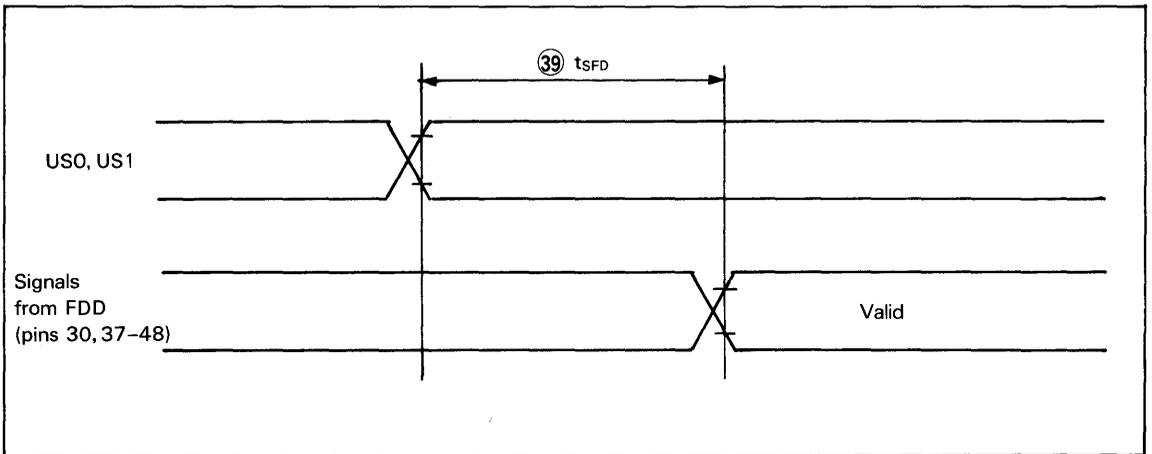
Figure 10-8. Drive Select Timing
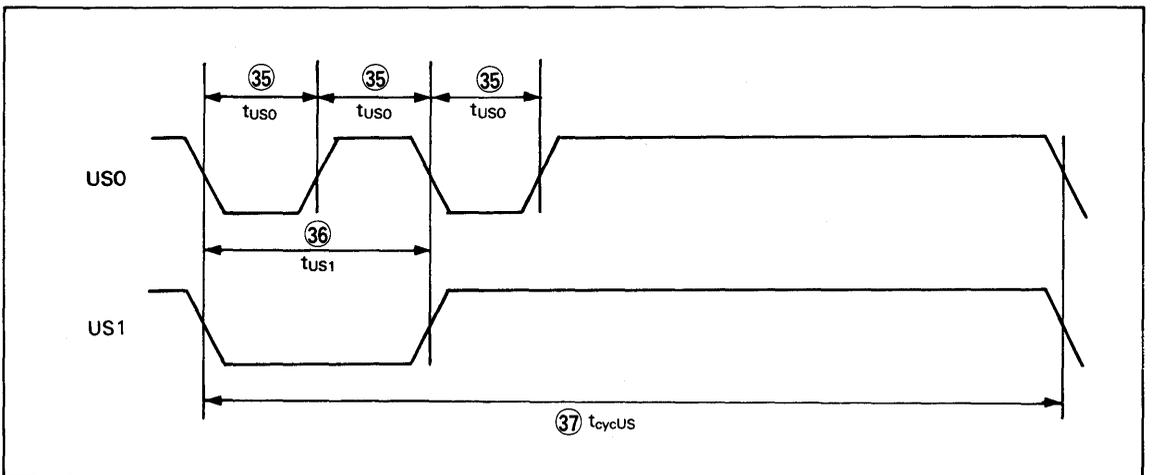


Figure 10-9. Automatic Polling Timing
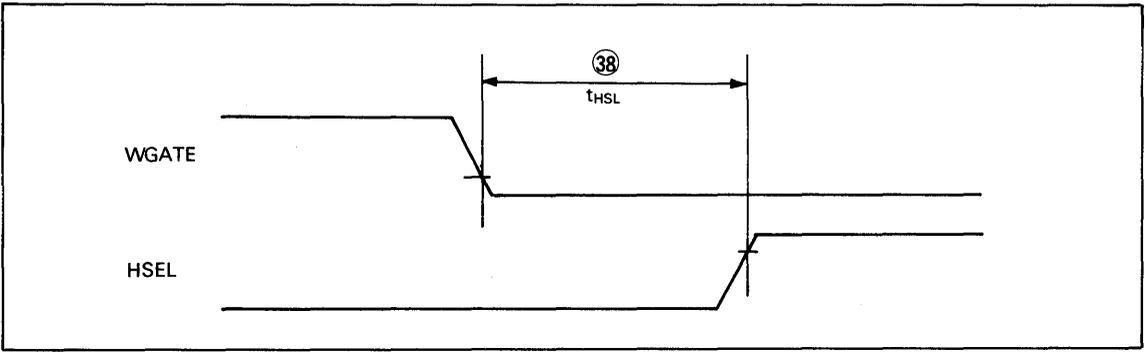
Figure 10-10.   Multitrack Write Timing
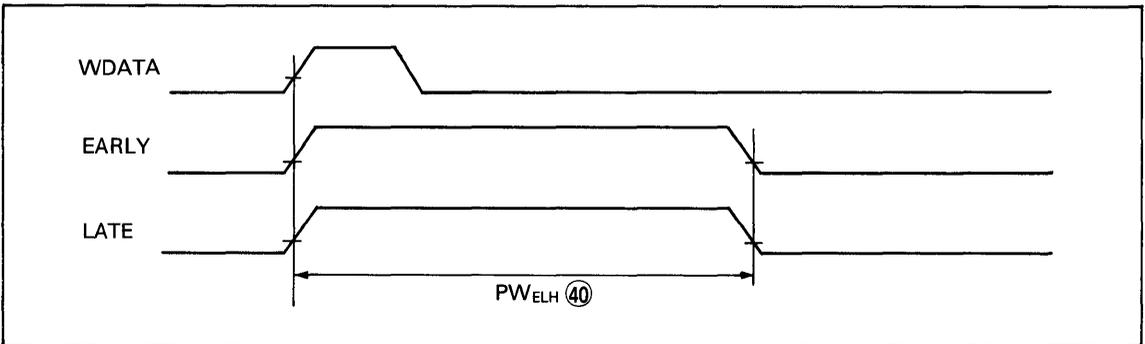
Figure 10-11.   Precompensation Timing
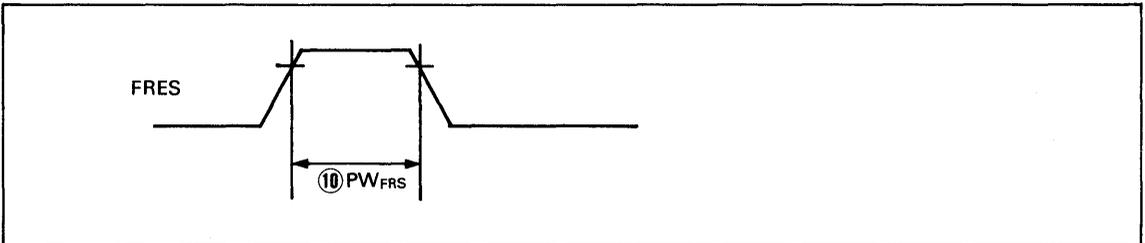
Figure 10-12.   Fault Reset Timing
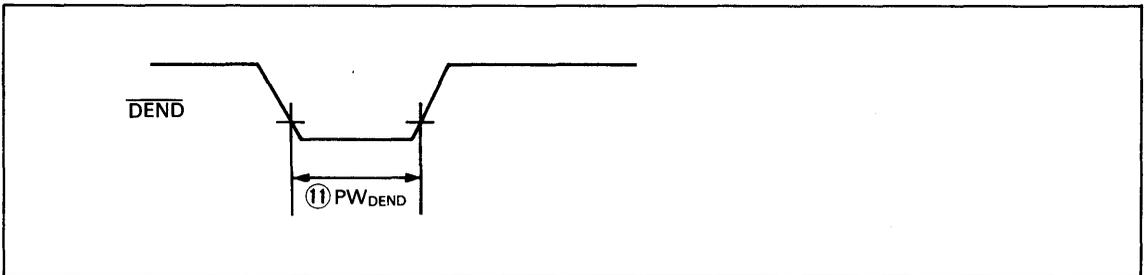
Figure 10-13.   DMA End Timing

| Signal	Load
D0–D7	C = 130 pF R = 10 kΩ
All other output pins except $\overline{IRQ}$ when IFS = 1	C = 40 pF R = 10 kΩ
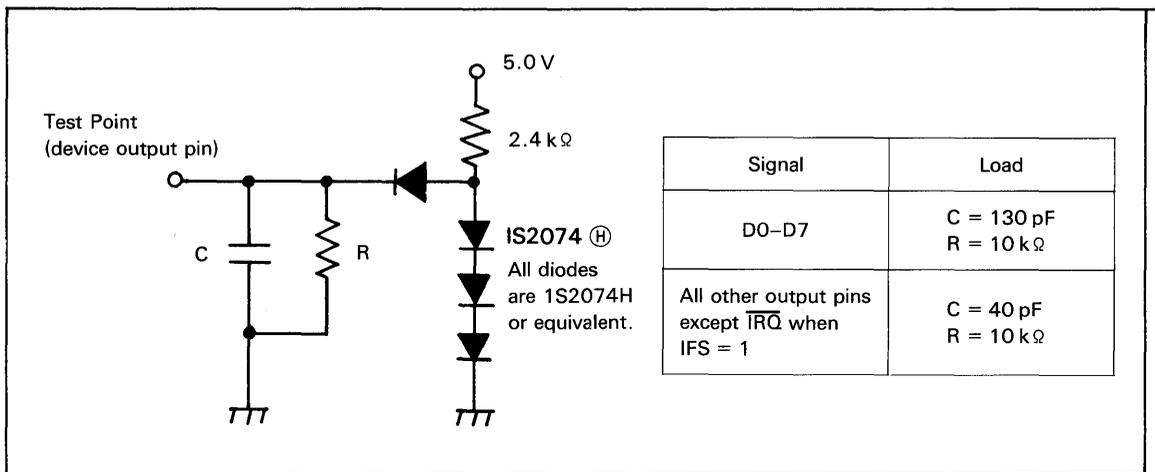
Figure 10-14.　Output Load Circuit for AC Testing
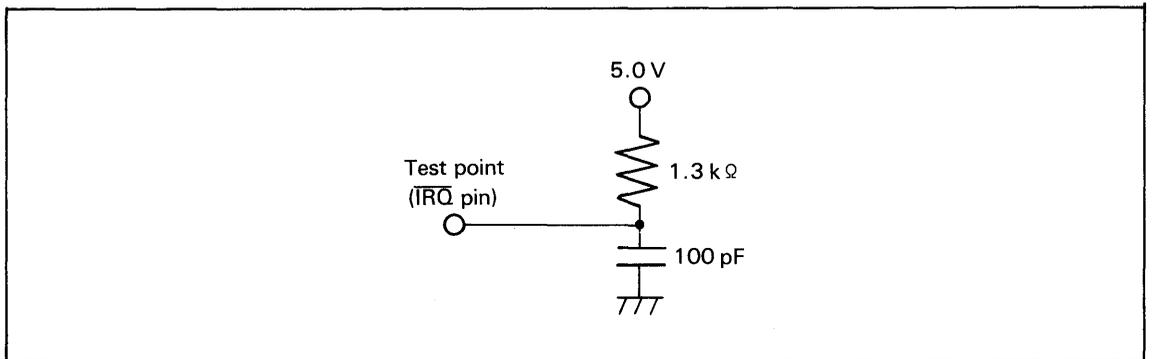
Figure 10-15.　$\overline{IRQ}$ Load Circuit for AC Testing When IFS = 1

$V_{CC} = 5V \pm 5\%$
$V_{SS} = 0V$
$T_a = 0$ to $\pm 70°C$
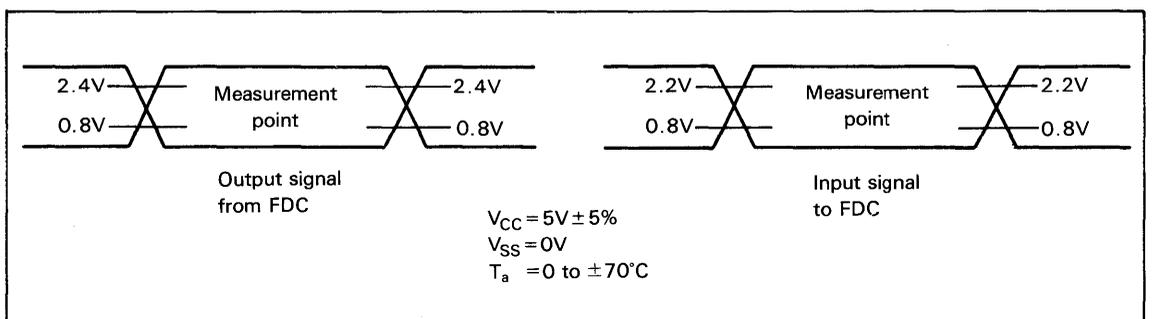
Figure 10-16.　AC Testing Measurement Conditions

● DP-48   (Unit: mm (inch))
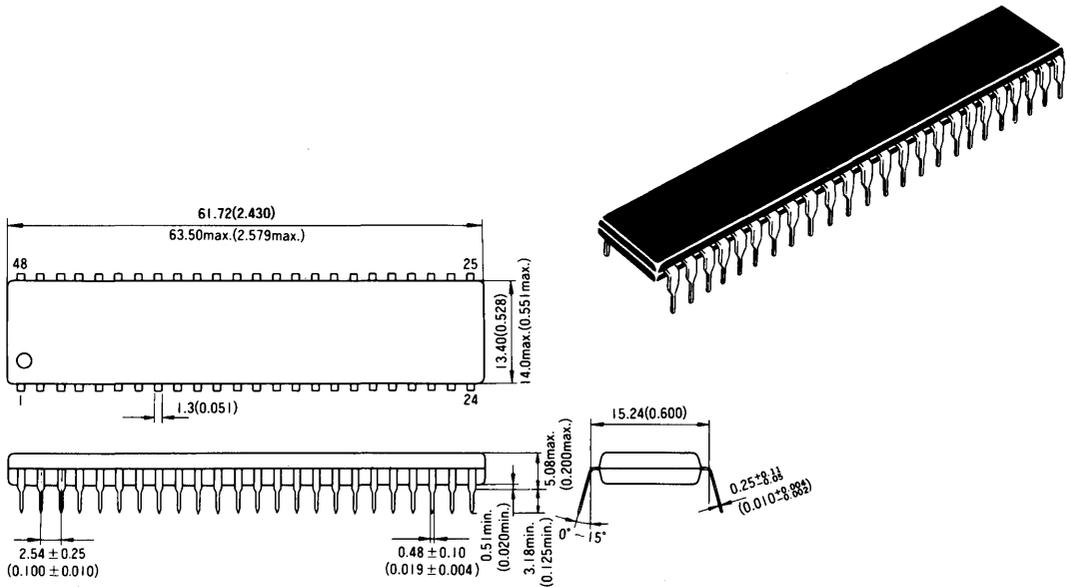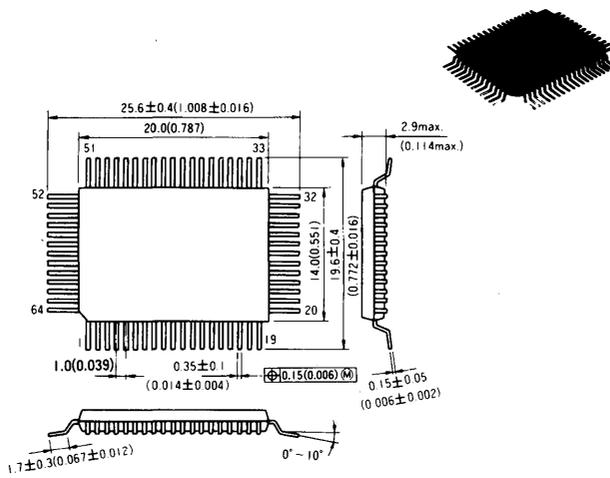
61.72(2.430)
63.50max.(2.579max.)
48
25
13.40(0.528)
14.0max.(0.551max.)
1
24
1.3(0.051)

15.24(0.600)
5.08max.
(0.200max.)
2.54±0.25
(0.100±0.010)
0.48±0.10
(0.019±0.004)
0.51min.
(0.020min.)
3.18min.
(0.125min.)
0.25$^{+0.11}_{-0.05}$
(0.010$^{+0.004}_{-0.002}$)
0°~15°

●FP-64   (Unit: mm (inch))

25.6±0.4(1.008±0.016)
20.0(0.787)
51
33
52
32
64
19
20
14.0(0.55)
19.6±0.4
(0.772±0.016)
2.9max.
(0.114max.)
1.0(0.039)
0.35±0.1
(0.014±0.004)
⊕ 0.15(0.006) Ⓜ
0.15±0.05
(0.006±0.002)
1.7±0.3(0.067±0.012)
0°~10°

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Branch Offices
Hitachi Europe GmbH Electronic Components Division
Central European Headquarters
Breslauer Straße 6,4040 Neuss 1, West Germany
Tel: 02101-15027~29
Telex: 8-518039 (HIEC D)
Fax: 02101-10513

Hitachi Europe GmbH Electronic Components Division
Central European Headquarters
Verkaufsbüro Stuttgart
Fabrikstraße 17,7024 Filderstadt 4, West Germany
Tel: 0711-772011
Telex: 7-255267 (HIES D)
Fax: 0711-77751·16

Hitachi Europe GmbH Electronic Components Division
Central European Headquarters
Bureau de Représentation en France
95-101, Rue Charles-Michels
93200 Saint Denis, France
Tel: 01-821-6015
Telex: 611387 (HITACHI F)
Fax: 01-2436997

Hitachi Europe GmbH Electronic Components Division
Central European Headquarters
Via B. Davanzati, 27
20158 Milano, Italy
Tel: 02-3763024
Telex: 323377 (HITEC I)
Fax: 02-3453006

EUROPEAN SALES OFFICES
Hitachi Europe Ltd. Electronic Components Division
Northern Europe Headquarters
21 Upton Road
Watford, Herts WD17TB England
Tel: 0923-24-6488
Telex: 936293 (HITEC G)
Fax: 0923-53610

Branch office
Hitachi Europe Ltd. Electronic Components Division
Northern Europe Headquarters
Box 1062, 163 11 Spanga, Sweden
Tel: 08-751-0035
Telex: 14106 (HITECST S)

ASIAN SALES OFFICES
Hitachi Electronic Components (Asia), Ltd.
Unit 512-513, 5/F North Tower
World Finance Centre
Harbour City, Canton Road, Tsim sha tsui
Kowloon, Hong Kong
Tel: 3-7219218~9, 7220698~9
Telex: 40815 (HISAL HX)

Branch offices
Hitachi Electronic Components (Asia), Ltd.
Taipei Branch Office
No. 64-1 9th Fl. Tun Hwa N. RD.
Taipei Financiai Center
Taipei, Taiwan R.O.C.
Tel: 02-773-2162~3
Telex: 23222 (HITEC TP 02 7414021)

Hitachi Electronic Components (Asia), Ltd.
Singapore Branch Office
75 Bukit Timah Road, 303-06 Boon Siew Bldg.
Singapore 0922
Tel: 3371200
Telex: 35534 (HISEKS RS)

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