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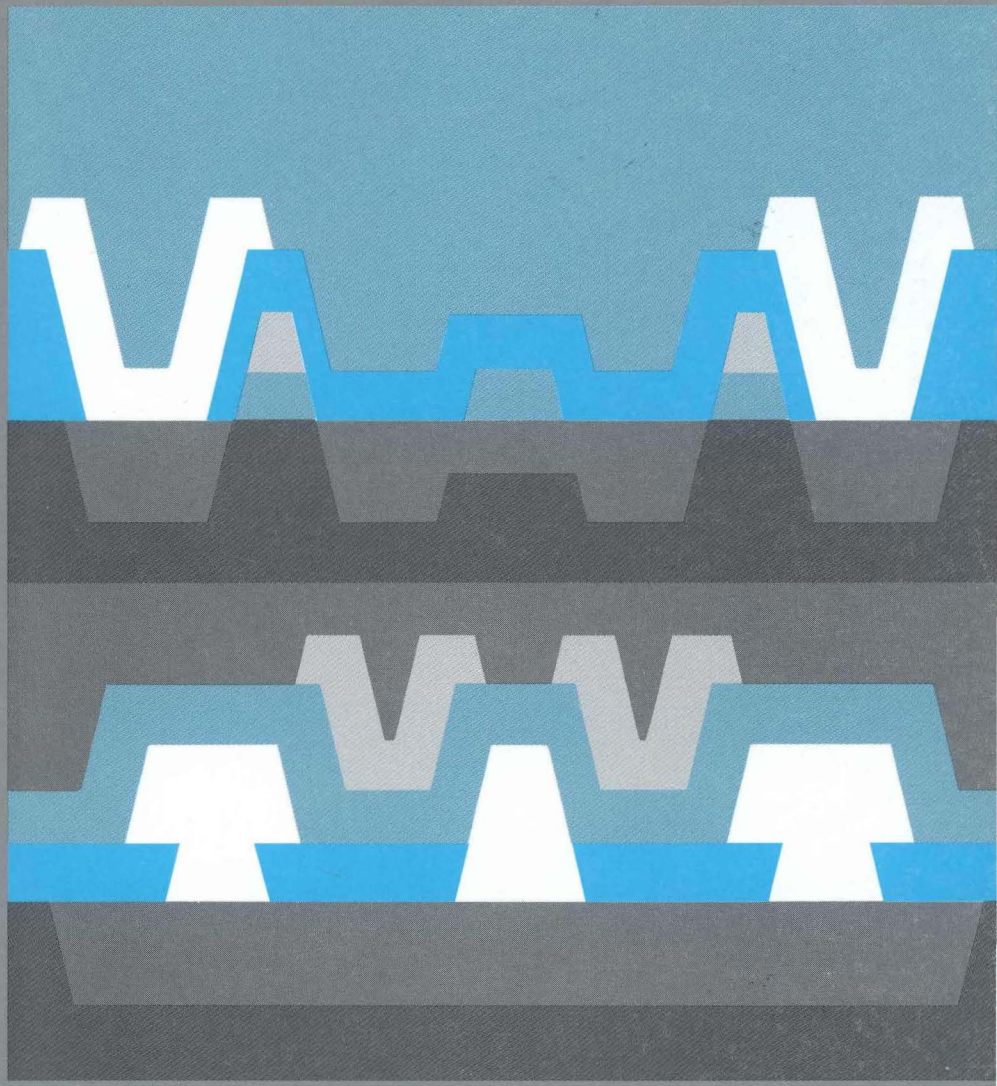

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*Legend

BiCMOS = BiCMOS Fast Static RAMs
CMOS = CMOS Fast Static RAMs
SRAM = Application Specific Static RAMs
MSBWSR = Medium Speed, Byte Wide Static RAMs
PRAM = Pseudo Static RAMs
SRM = Static RAM Modules

ALPHA-NUMERIC INDEX (CONT'D.)

*Legend

BiCMOS = BiCMOS Fast Static RAMs
CMOS = CMOS Fast Static RAMs
SRAM = Application Specific Static RAMs
MSBWSR = Medium Speed, Byte Wide Static RAMs
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- Package Information
- Reliability of Hitachi IC Memories
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Quick Reference Guide

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	HM6207HL-25		25	25		●								●	3-3
	HM6207HL-35		35	35		●								●	3-2
	HM6207HL-45		45	45		●								●	3-2
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	HM621664HL-25		25	25						●			●		3-78
	HM621864H Series	64Kx18													3-78
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	HM621864H-20		20	20						●			●		3-78
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	HM621864HL-20		20	20						●			●		3-78
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	HM62W8127H-30		30	30									●		3-91
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	HM62W8127HL-25		25	25									●		3-91
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	HM62W9127H-30		30	30									●		3-91
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	HM62W1664HL-30		30	30						●			●		3-102
	HM62W1664HL-35		35	35						●			●		3-102
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	HM62W1864H-35		35	35						●			●		3-102
	HM62W1864H-45		45	45						●			●		3-102
	HM62W1864HL-25		25	25						●			●		3-102
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	HM62A9128-20		10	20										●	4-9
	HM62A8128-17		8	17										●	4-9
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	HM62256-10		100	100		●	●								5-13
	HM62256-12		120	120		●	●								5-13
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	HM62256A-15		150	150		●	●					●			5-27
	HM62256AL-8		85	85		●	●	●	●			●			5-27
	HM62256AL-10		100	100		●	●	●	●			●			5-27
	HM62256AL-12		120	120		●	●	●	●			●			5-27
	HM62256AL-15		150	150		●	●	●	●			●			5-27
	HM62256AL-8SL		85	85		●	●	●	●			●			5-27
	HM62256AL-10SL		100	100		●	●	●	●			●			5-27
	HM62256AL-12SL		120	120		●	●	●	●			●			5-27
	HM62256AL-15SL		150	150		●	●	●	●			●			5-27

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1 M-bit	HM628128 Series	128Kx8			32										5-39
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	HM628128-8		85	85		●	●	●	●						5-39
	HM628128-10		100	100		●	●	●	●						5-39
	HM628128-12		120	120		●	●	●	●						5-39
	HM628128L-7		70	70		●	●	●	●						5-39
	HM628128L-8		85	85		●	●	●	●						5-39
	HM628128L-10		100	100		●	●	●	●						5-39
	HM628128L-12		120	120		●	●	●	●						5-39
	HM628128L-7SL		70	70		●	●	●	●						5-39
	HM628128L-8SL		85	85		●	●	●	●						5-39
	HM628128L-10SL		100	100		●	●	●	●						5-39
	HM628128L-12SL		120	120		●	●	●	●						5-39
	HM628128L-7L		70	70				●	●						5-39
	HM628128L-8L		85	85				●	●						5-39
	HM628128L-10L		100	100				●	●						5-39
	HM628128L-12L		120	120				●	●						5-39
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	HM628128AL-5		55	55		●								●	5-55
	HM628128AL-7		70	70		●								●	5-55
	HM628128AL-8		85	85		●								●	5-55
	HM628128AL-10		100	100		●								●	5-55
	HM628128AL-5L		55	55		●		●	●					●	5-55
	HM628128AL-7L		70	70		●		●	●					●	5-55
	HM628128AL-8L		85	85		●		●	●					●	5-55
	HM628128AL-10L		100	100		●		●	●					●	5-55
	HM628128AL-5SL		55	55		●	●	●	●						5-55
	HM628128AL-7SL		70	70		●	●	●	●						5-55
	HM628128AL-8SL		85	85		●	●	●	●						5-55
	HM628128AL-10SL		100	100		●	●	●	●						5-55
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	HM629128-7		70	70		●	●	●							5-66
	HM629128-8		85	85		●	●	●							5-66
	HM629128-10		100	100		●	●	●							5-66
	HM629128-7L		70	70		●	●	●							5-66
	HM629128-8L		85	85		●	●	●							5-66
	HM629128-10L		100	100		●	●	●							5-66
	HM629128-7SL		70	70		●	●	●							5-66
	HM629128-8SL		85	85		●	●	●							5-66
	HM629128-10SL		100	100		●	●	●							5-66
4 M-bit	HM628512 Series	512Kx8			32										5-78
	HM628512-5		55	55		●	●								5-78
	HM628512-7		70	70		●	●								5-78
	HM628512-8		85	85		●	●								5-78
	HM628512-10		100	100		●	●								5-78
	HM628512L-5		55	55		●	●			●	●				5-78
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	HM628512L-8SL		85	85		●	●			●	●				5-78
	HM628512L-10SL		100	100		●	●			●	●				5-78

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256 K-bit	HM62W256 Series	32Kx8			28										5-89
	HM62W256L-7		70	70			●	●							5-89
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	HM62W256L-8SL		85	85			●	●							5-89
	HM62W8128 Series	128Kx8			32										5-100
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	HM62W8128L-12		120	120		●	●	●							5-100
	HM62W8128L-10L		100	100		●	●	●							5-100
	HM62W8128L-12L		120	120		●	●	●							5-100
	HM62W8128L-10SL		100	100		●	●	●							5-100
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1 M-bit	HM62V8128 Series														5-111
	HM62V8128L-12		120	120		●	●	●							5-111
	HM62V8128L-15		150	150		●	●	●							5-111
	HM62V8128L-12L		120	120		●	●	●	●						5-111
	HM62V8128L-15L		150	150		●	●	●	●						5-111
	HM62V8128L-12SL		120	120		●	●	●	●						5-111
	HM62V8128L-15SL		150	150		●	●	●	●						5-111
	HM62W9128 Series	128Kx9													5-122
	HM62W9128L-10		100	100			●	●							5-122
	HM62W9128L-12		120	120			●	●							5-122
	HM62W9128L-10L		100	100			●	●							5-122
	HM62W9128L-12L		120	120			●	●							5-122
	HM62W9128L-10SL		100	100			●	●							5-122
	HM62W9128L-12SL		120	120			●	●							5-122
	HM62V9128 Series														5-132
	HM62V9128L-15		150	150			●	●							5-132
	HM62V9128L-15L		150	150			●	●							5-132
	HM62V9128L-15SL		150	150			●	●							5-132
Pseudo Static RAMs															6-1
	5.0v Supply														6-1
256 K-bit	HM65256B Series	32Kx8			28										6-3
	HM65256B-10		100	160		●	●								6-3
	HM65256B-12		120	190		●	●								6-3
	HM65256B-15		150	235		●	●								6-3
	HM65256B-20		200	310		●	●								6-3
	HM65256BL-10		100	160		●	●								6-3
	HM65256BL-12		120	190		●	●								6-3
	HM65256BL-15		150	235		●	●								6-3
	HM65256BL-20		200	310		●	●								6-3
1 M-bit	HM658128A Series	128Kx8			32										6-15
	HM658128AD-8		80	130		●	●	●	●						6-15
	HM658128AD-10		100	160		●	●	●	●						6-15
	HM658128AD-12		120	190		●	●	●	●						6-15
	HM658128AL-8		80	130		●	●	●	●						6-15
	HM658128AL-10		100	160		●	●	●	●						6-15
	HM658128AL-12		120	190		●	●	●	●						6-15
	HM658128AL-8L		80	130		●	●	●	●						6-15
	HM658128AL-10L		100	160		●	●	●	●						6-15
	HM658128AL-12L		120	190		●	●	●	●						6-15

Quick Reference Guide

Total bit	Type No.	Organization	Access time (ns) max	Cycle time (ns) min	Package Pin No.	P	FP	T	R	TT	RR	SP	CP	JP	Page
Pseudo Static RAMs (Cont'd.)															
	5.0v Supply (Cont'd.)														
4 M-bit	HM658512 Series	512Kx8			32										6-28
	HM658512L-8		80	130		●	●			●	●				6-28
	HM658512L-85		85	115		●	●			●	●				6-28
	HM658512L-10		100	160		●	●			●	●				6-28
	HM658512L-12		120	190		●	●			●	●				6-28
	HM658512L-8V		80	130		●	●			●	●				6-28
	HM658512L-85V		85	115			●			●	●				6-28
	HM658512L-10V		100	160		●	●			●	●				6-28
	HM658512L-12V		120	190		●	●			●	●				6-28
	HM658512D-8		80	130		●	●			●	●				6-28
	HM658512D-10		100	160		●	●			●	●				6-28
	HM658512D-12		120	190		●	●			●	●				6-28
	3.0v & 3.3v Supply														6-40
4 M-bit	HM65V8512 Series														6-40
	HM65V8512-12		120	190		●		●	●						6-40
	HM65V8512-15		150	230		●		●	●						6-40
	HM65V8512L-12		120	190		●		●	●						6-40
	HM65V8512L-15		150	230		●		●	●						6-40
	HM65V8512L-12V		120	190		●		●	●						6-40
	HM65V8512L-12V		150	130		●		●	●						6-40
	HM65W8512 Series														6-51
	HM65W8512D-12		120	120			●		●	●					6-51
	HM65W8512D-15		150	150			●		●	●					6-51
	HM65W8512L-12		120	120			●		●	●					6-51
	HM65W8512L-15		150	150			●		●	●					6-51
	HM65W8512L-12V		120	120			●		●	●					6-51
	HM65W8512L-15V		150	150			●		●	●					6-51

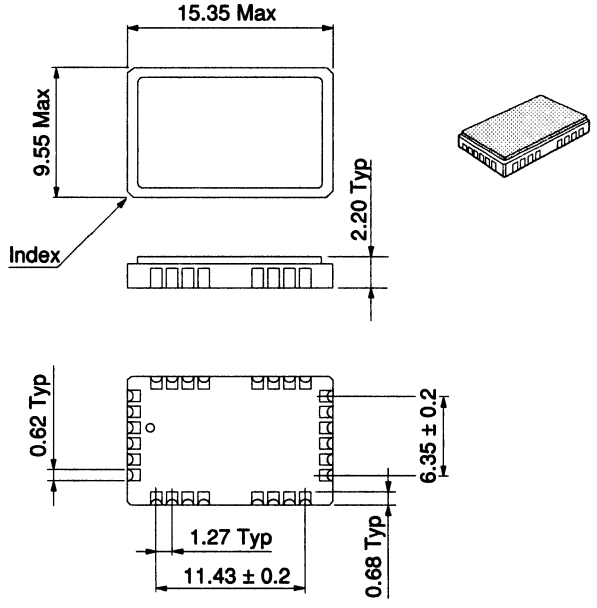
Total bit	Type No.	Organization	Access time (ns) max	Cycle time (ns) min	Package Pin No.	M	Page
Static RAM Modules							
	Medium Speed Static RAM Modules						7-1
4 M-bit	HM66205L Series	512Kx8			32		7-3
	HM66205L-85		85	85		●	7-3
	HM66205L-10		100	100		●	7-3
	HM66205L-12		120	120		●	7-3

Package Information

Chip Carrier

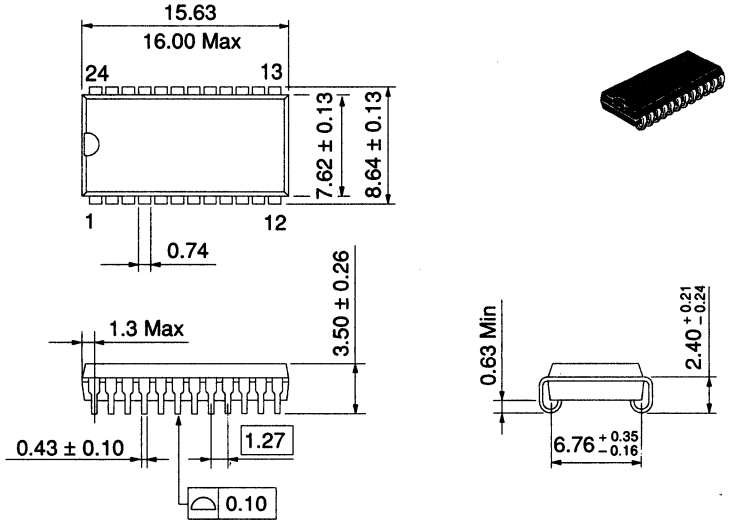
Unit: mm

• CG-28B



Flat Package (J-bend Leads)

• CP-24D

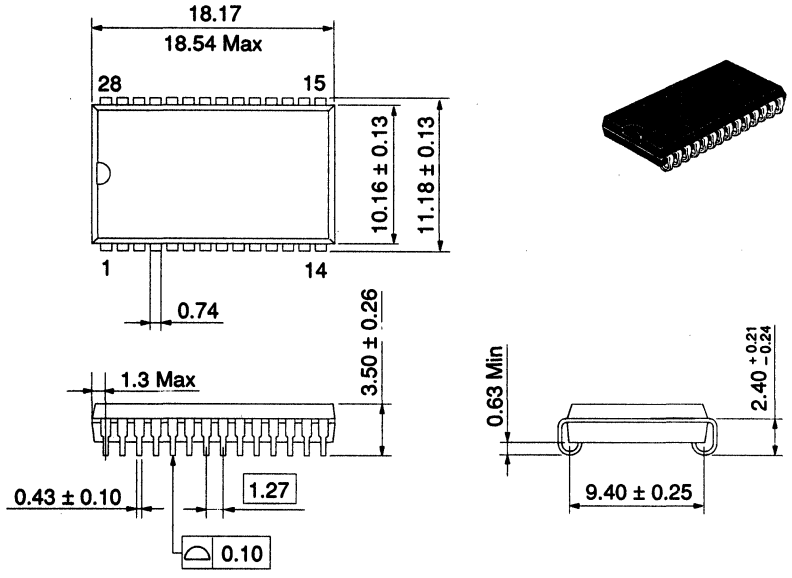


Package Information

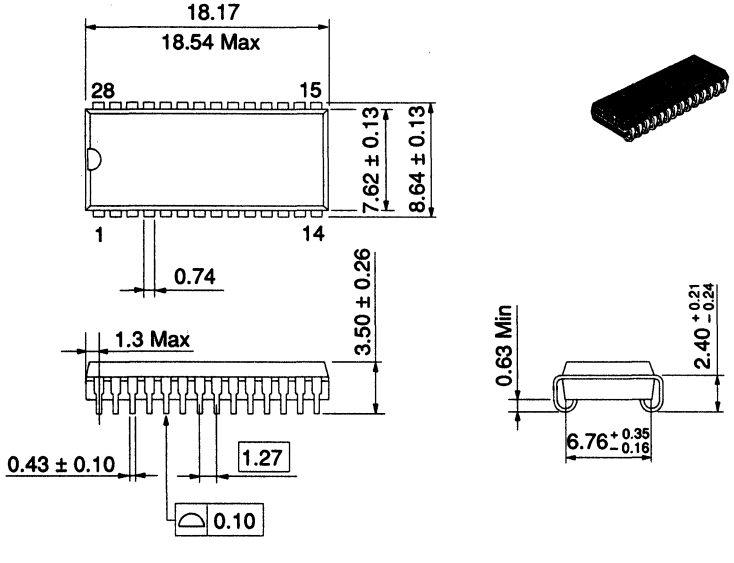
Flat Package (J-bend Leads)

Unit: mm

• CP-28D



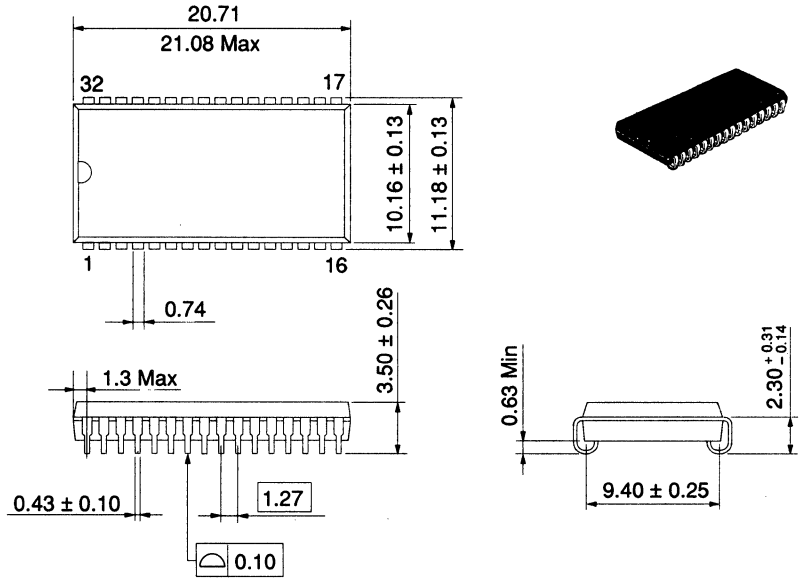
• CP-28DN



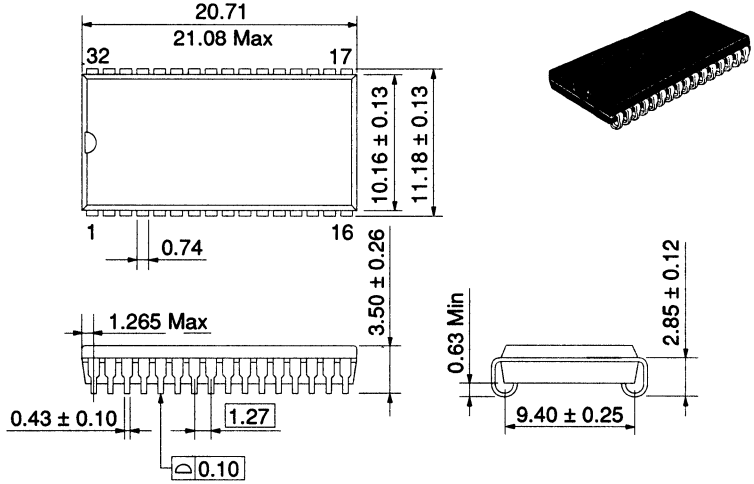
Flat Package (J-bend Leads)

Unit: mm

• CP-32D



• CP-32DB

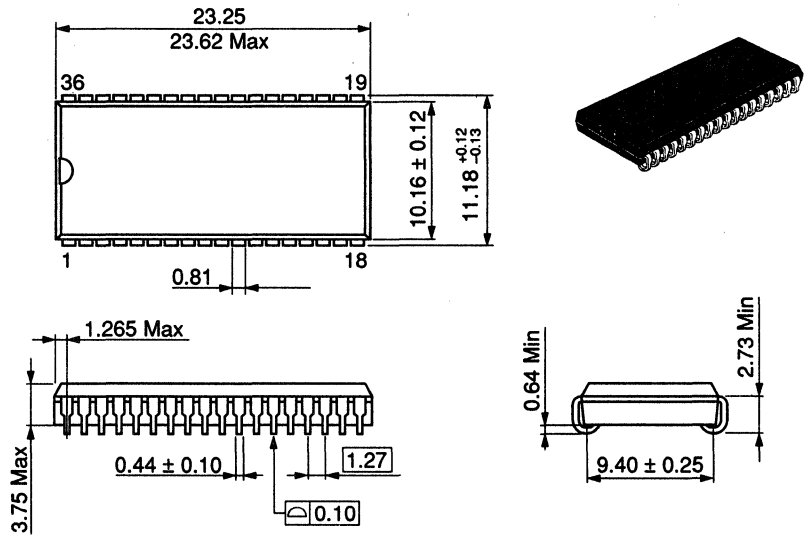


Package Information

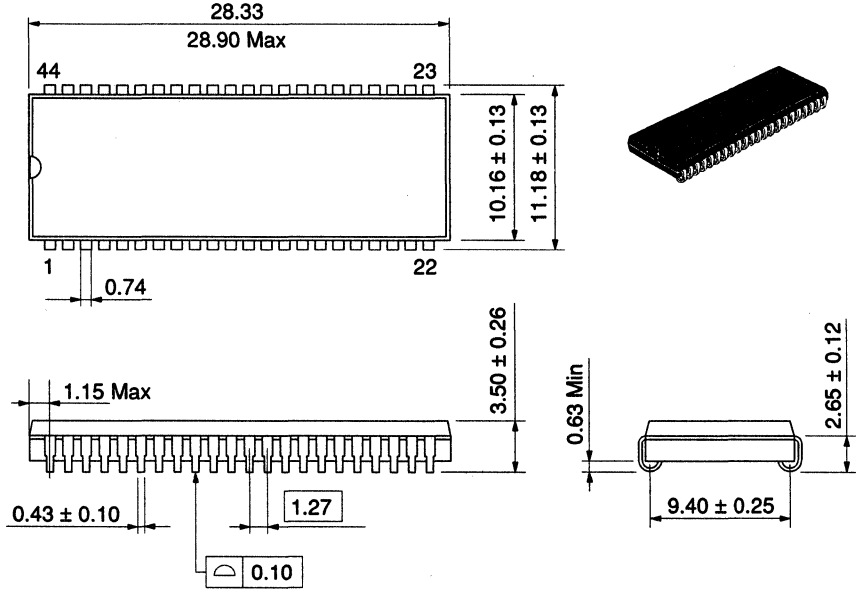
Flat Package (J-bend Leads)

Unit: mm

• CP-36D



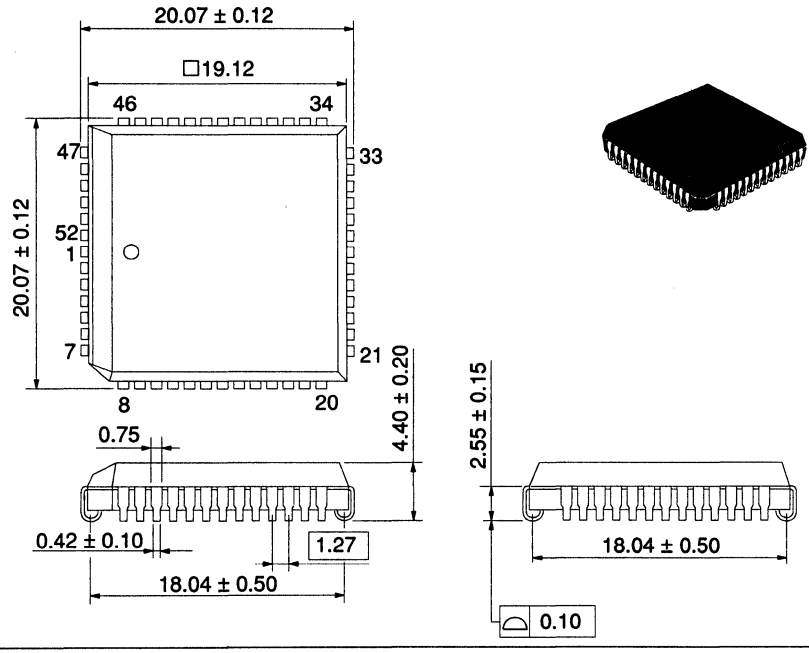
• CP-44D



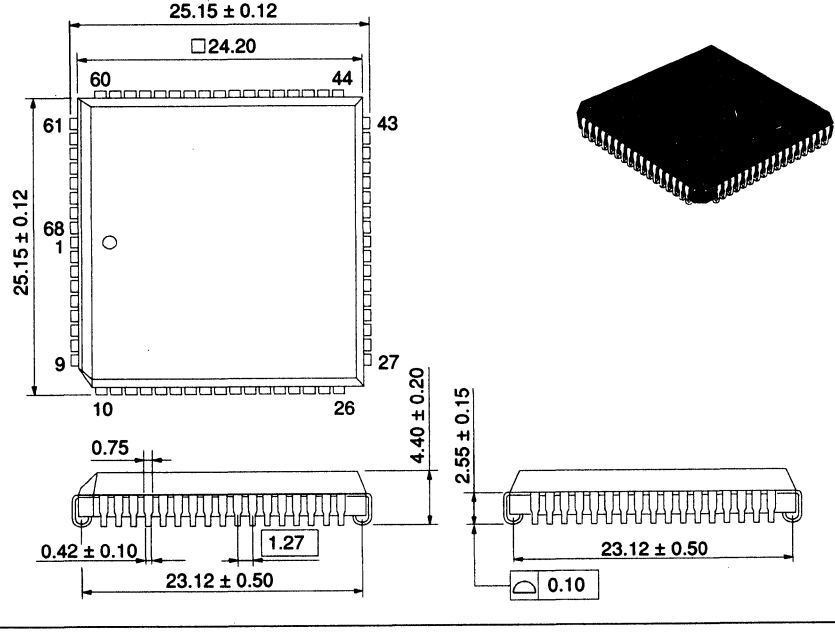
Flat Package (J-bend Leads)

Unit: mm

• CP-52



• CP-68



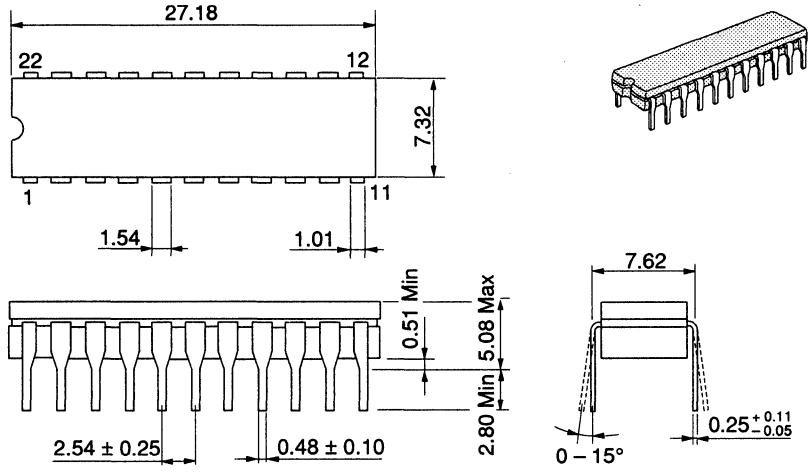
Applicable ICs

CG-28B	HM100500CG Series
CP-24D	HM6289JP Series, HM6289LJP Series, HM6789HAJP Series, HM6288JP Series, HM6288LJP Series, HM6287HJP Series, HM6287HLJP Series, HM6208HJP Series, HM6208HLJP Series, HM6708SHJP Series, HM6708AJP Series, HM6207HJP Series, HM6207HLJP Series, HM6707AJP Series, HM101490JP Series, HM6787HAJP Series
CP-28D	HM624256AJP Series, HM624256ALJP Series, HM621100AJP Series, HM621100ALJP Series
CP-28DN	HM62832HJP Series, HM62832HLJP Series, HM62832UHJP Series, HM62832UHLJP Series, HM67832SHJP Series, HM6709AJP Series, HM6209SHJP Series, HM100494JP Series, HM101494JP Series, HM6709SHJP Series, HM10494JP Series, HM101514JP Series
CP-32D	HM624257AJP Series, HM624257ALJP Series, HM100504JP Series, HM101504JP Series, HM62A9128JP Series, HM62A8128JP Series
CP-32DB	HM628127HJP Series, HM628127HLJP Series, HM62W8127HJP Series, HM62W8127HLJP Series, HM678127UHJ Series, HM674256UHJ Series, HM671400LJP Series, HM674100LJP Series, HM671400JP Series, HM674100JP Series
CP-36D	HM629127HJP Series, HM629127HLJP Series, HM62W9127HJP Series, HM62W9127HLJP Series, HM67A4101JP Series
CP-44D	HM621664HJP Series, HM621664HLJP Series, HM621864HJP Series, HM621864HLJP Series, HM62W1664HJP Series, HM62W1664HLJP Series, HM62W1864HJP Series, HM62W1864HLJP Series
CP-52	HM62B168CP Series, HM62B188CP Series, HM62A2016CP Series
CP-68	HM62A2017CP Series

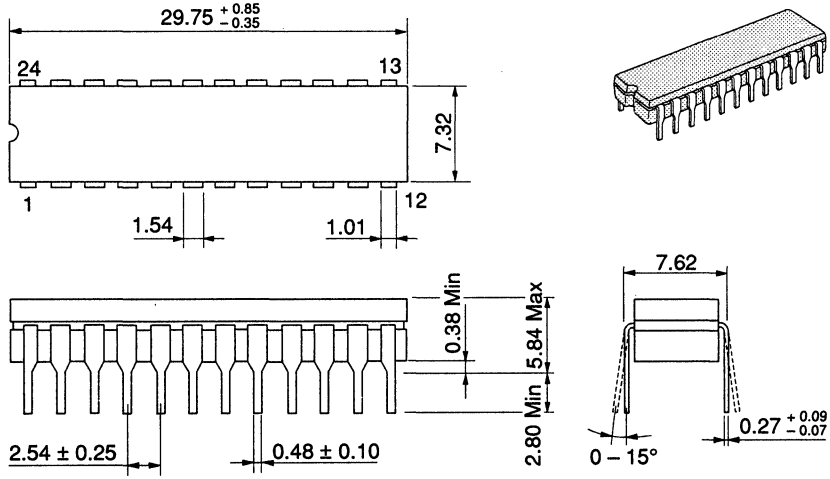
CERDIP

Unit: mm

• DG-22N



• DG-24V

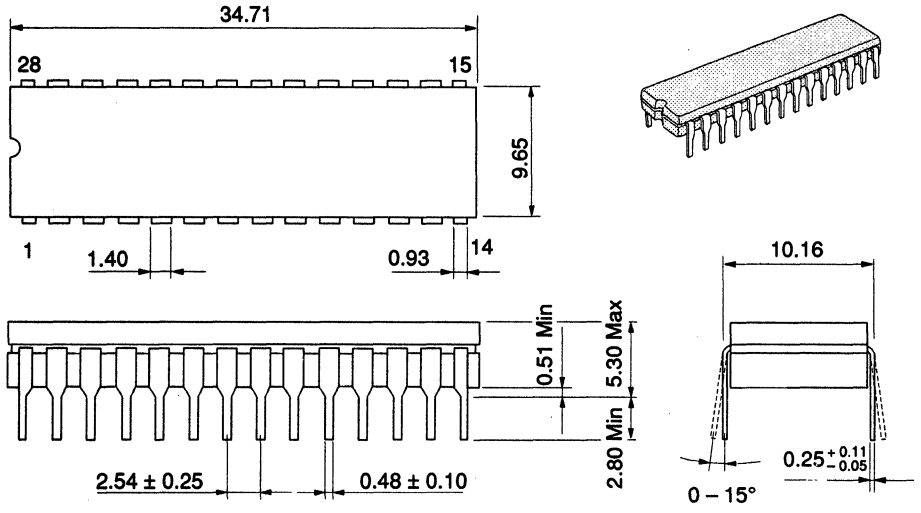


Package Information

CERDIP

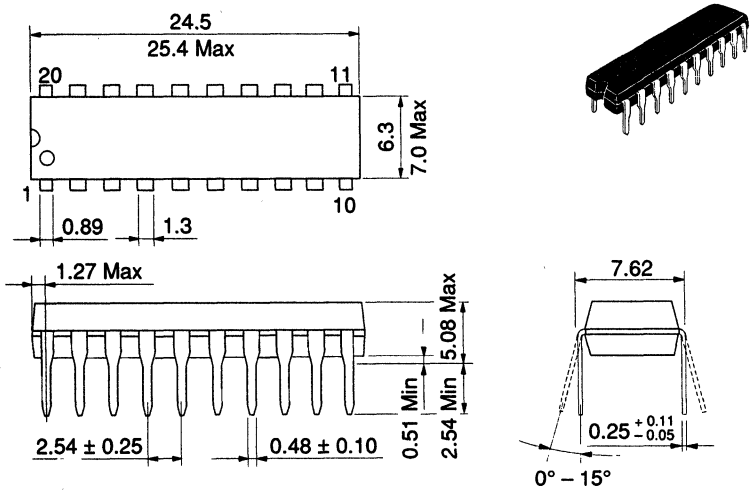
Unit: mm

- DG-28N



Dual-in-line Plastic

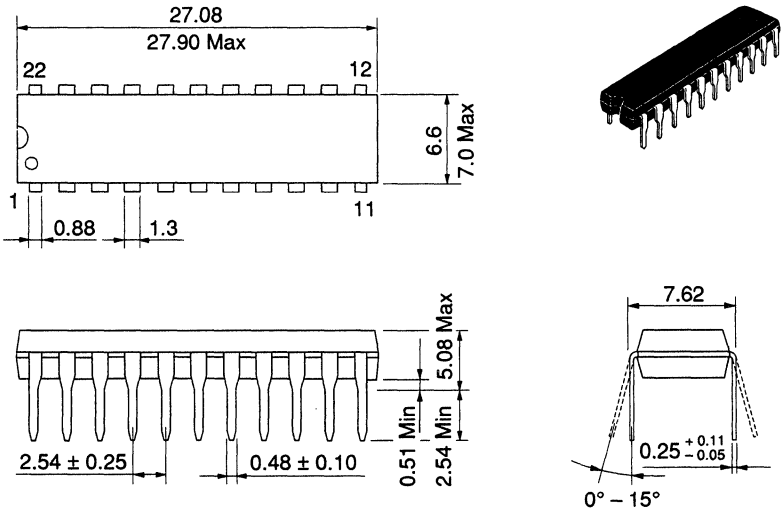
- DP-20N



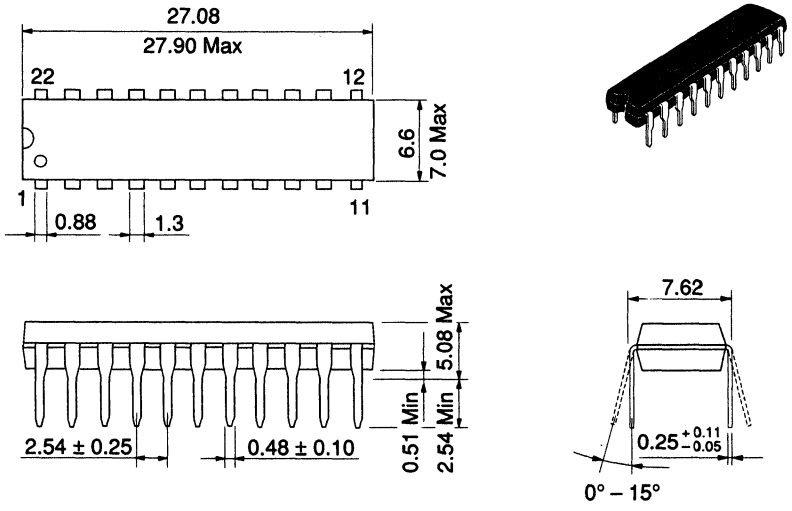
Dual-in-line Plastic

Unit: mm

- DP-22N



- DP-22NB

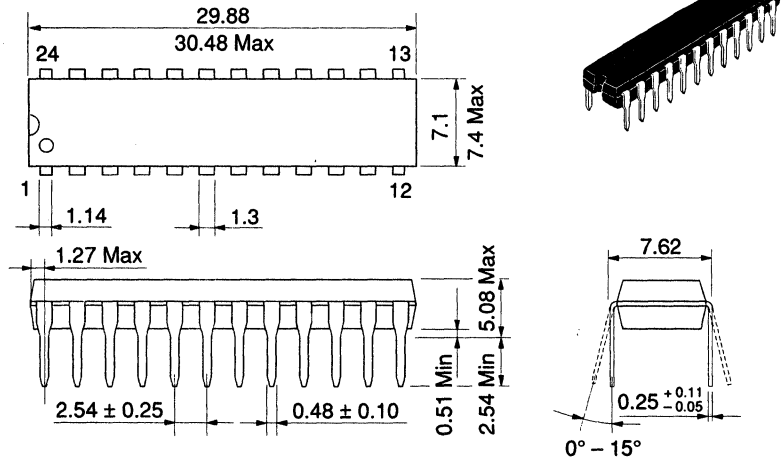


Package Information

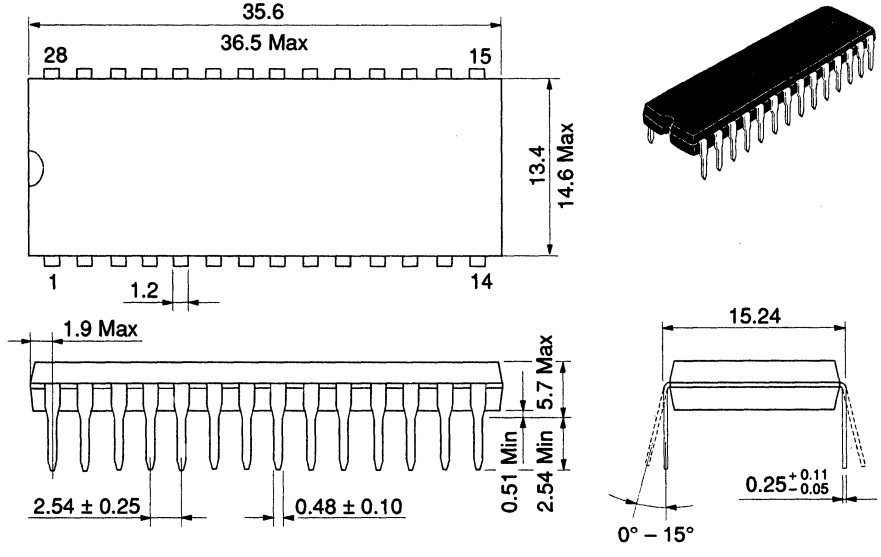
Dual-in-line Plastic

Unit: mm

- DP-24NC



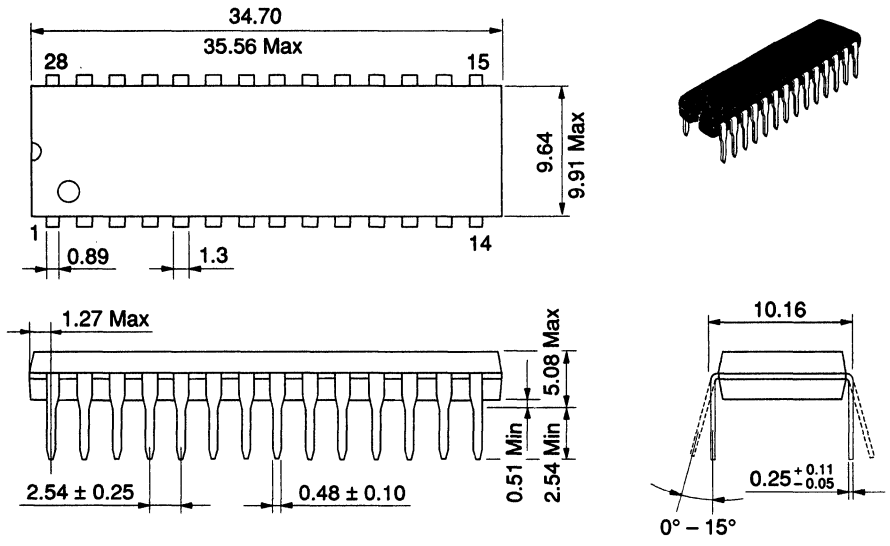
- DP-28



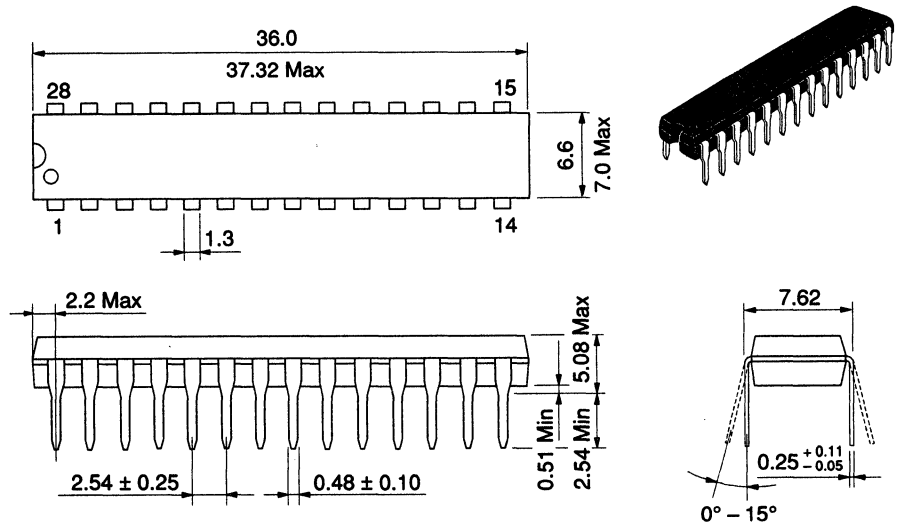
Dual-in-line Plastic

Unit: mm

• DP-28C



• DP-28N

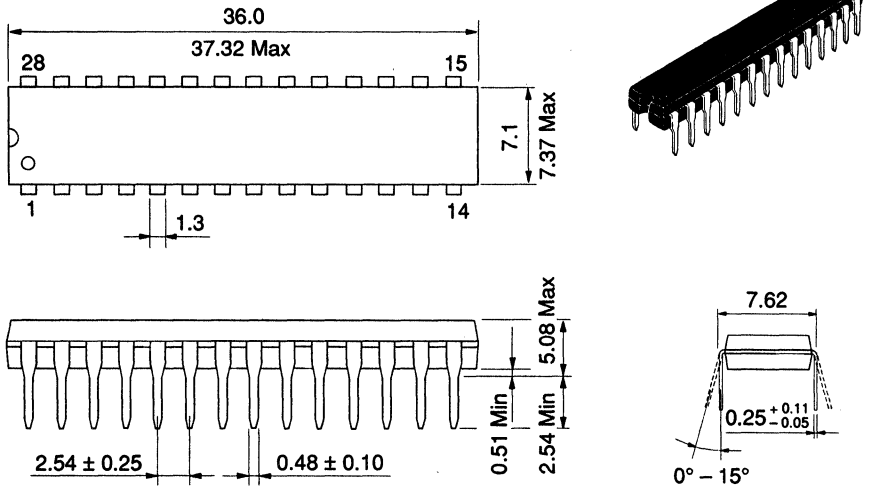


Package Information

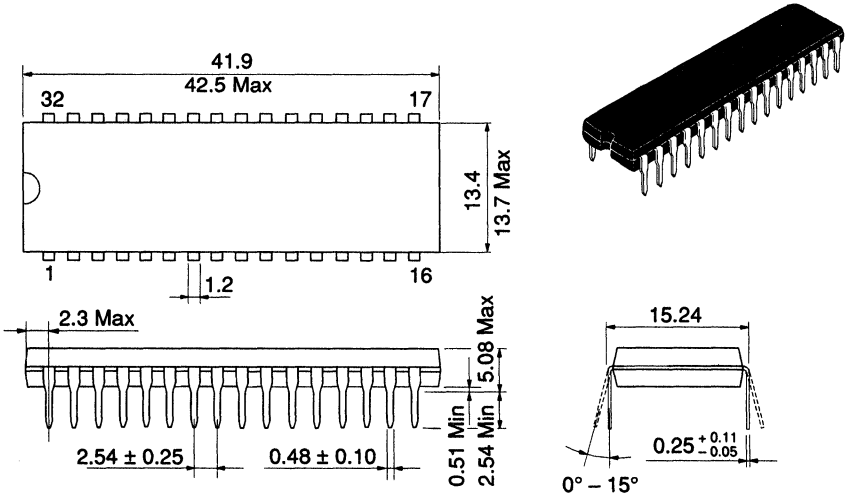
Dual-in-line Plastic

Unit: mm

- DP-28NA



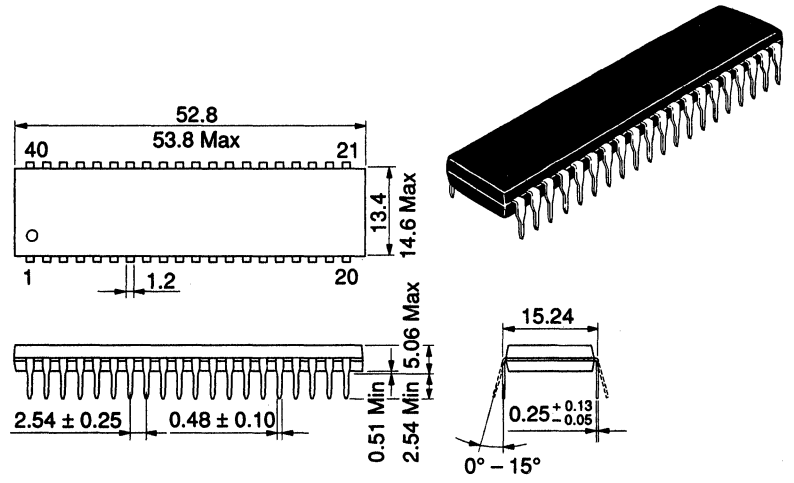
- DP-32



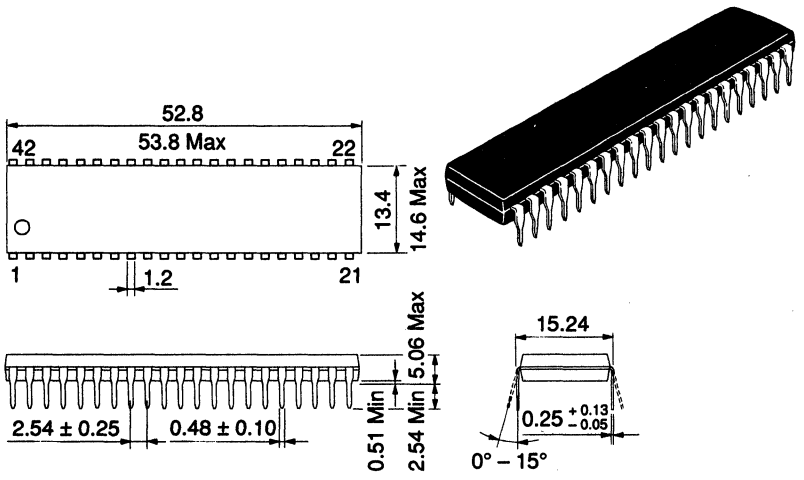
Dual-in-line Plastic

Unit: mm

- DP-40



- DP-42



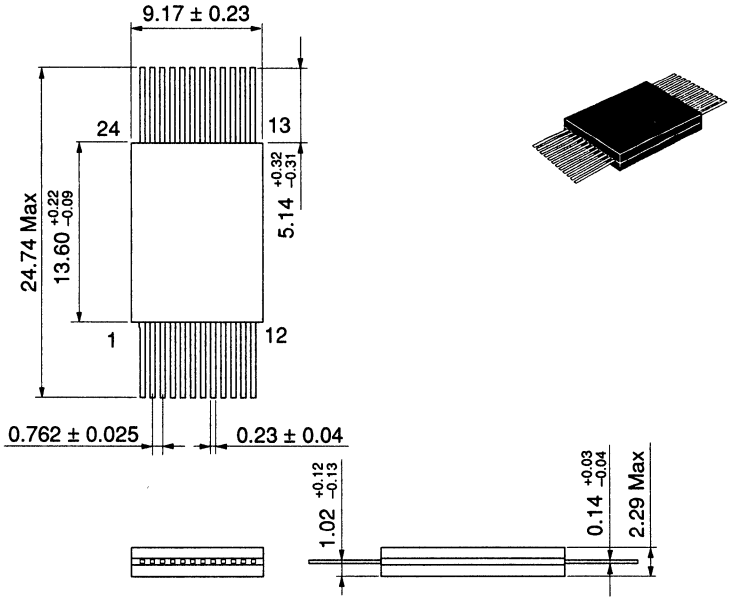
Applicable ICs

DG-22N	HM10490 Series, HM101490 Series
DG-24V	HM10500 Series, HM100500 Series, HM101500 Series
DG-28N	HM10494 Series, HM101494 Series
DP-20N	HM6268P Series, HM6268LP Series, HM6267P Series, HM6267LP Series
DP-22N	HM6287P Series, HM6287LP Series
DP-22NB	HM6288P Series, HM6288LP Series, HM6287HP Series, HM6287HLP Series, HM6787HAP Series, HM6788HAP Series
DP-24NC	HM6716P Series, HM6719P Series, HM6789HAP Series, HM6208HP Series, HM6208HLP Series, HM6708AP Series, HM6207HP Series, HM6207HLP Series, HM6707AP Series
DP-28	HM6264AP Series, HM6264ALP Series, HM6264ALP-L Series, HM62256P Series, HM62256LP Series, HM62256LP-SL Series, HM62256AP Series, HM62256ALP Series, HM62256ALP-SL Series, HM65256BP Series, HM65256BLP Series
DP-28C	HM624256P Series, HM624256LP Series, HM624256AP Series, HM624256ALP Series, HM621100AP Series, HM621100ALP Series
DP-28N	HM6264ASP Series, HM6264ALSP Series, HM6264ALSP-L Series, HM65256BSP Series, HM65256BLSP Series
DP-28NA	HM62256ASP Series, HM62256ALSP Series, HM62256ALSP-SL Series, HM62832HP Series, HM62832HLP Series, HM62832UHP Series, HM62832UHLP Series
DP-32	HM628128P Series, HM628128LP Series, HM628128LP-SL Series, HM628512P Series, HM628512LP Series, HM628512LP-SL Series, HM658128ADP Series, HM658128ALP Series, HM658128ALP-L Series, HM658512DP Series, HM658512LP Series, HM658512LP-V Series, HM628128ALP Series, HM628128ALP-L Series, HM628128ALP-SL Series, HM629128LP Series, HM629128LP-L Series, HM629128LP-SL Series, HM62V8128LP Series, HM62V8128LP-L Series, HM62V8128LP-SL Series
DP-40	HN62412P, HN62422P, HN62444P, HN62444BP, HN62442BP, HN62414P, HN62434P, HN62444BNP
DP-42	HN62428P, HN62418P, HN624116P, HN62W428P, HN62W4116P, HN62438P, HN62438NP, HN624316P, HN624316NP

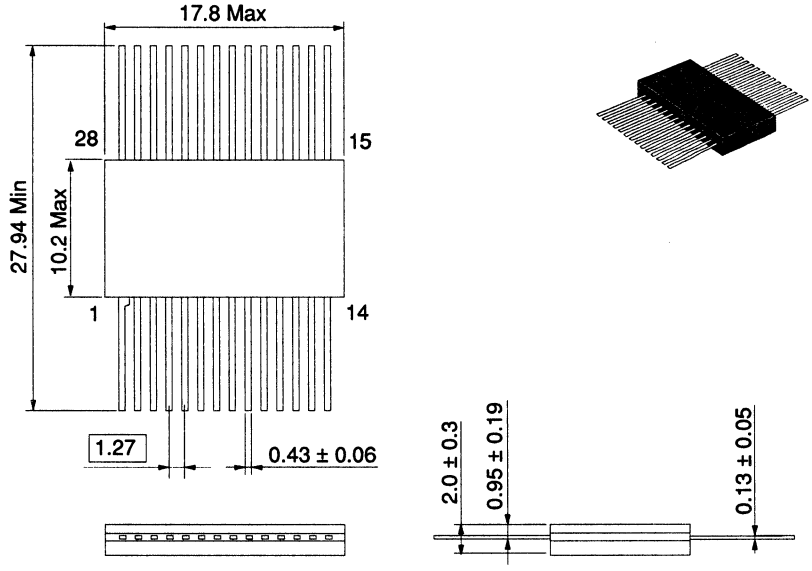
Flat Package

Unit: mm

• FG-24D



• FG-28D

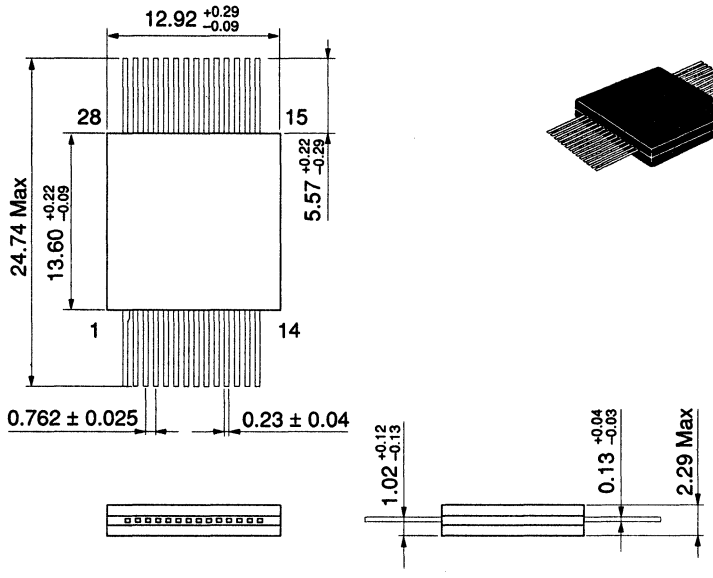


Package Information

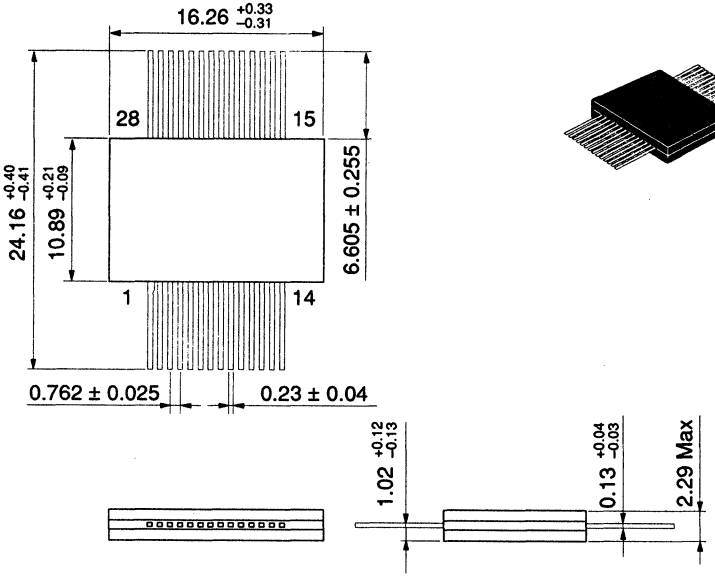
Flat Package

Unit: mm

• FG-28DA



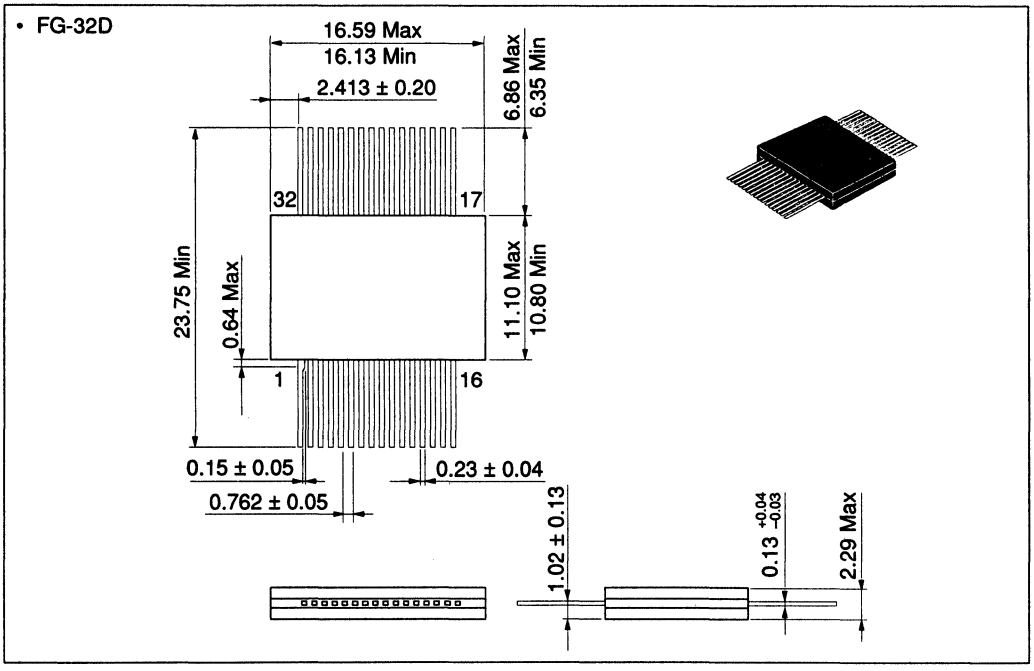
• FG-28DB



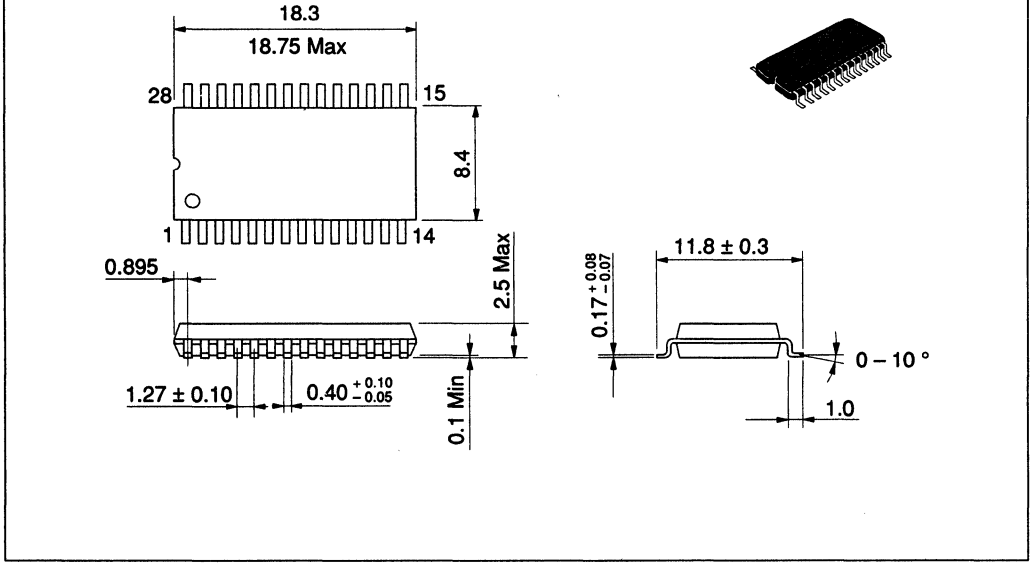
Flat Package

Unit: mm

• FG-32D



• FP-28D

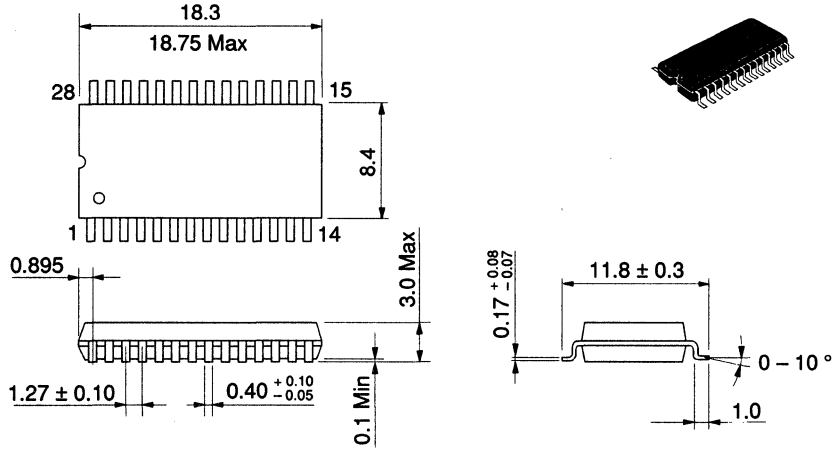


Package Information

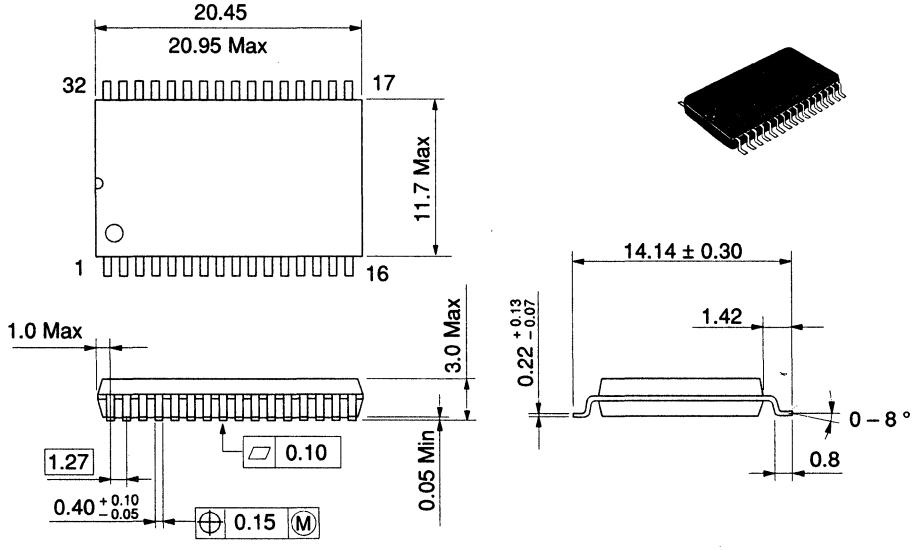
Flat Package

Unit: mm

• FP-28DA



• FP-32D



Applicable ICs

FG-24D	HM100500F Series, HM101500F Series
FG-28D	HM101494F Series, HM101484F Series
FG-28DA	HM100504F Series, HM101504F Series
FG-28DB	HM101510F Series
FG-32D	HM101514F Series, HM101513F Series, HM101515F Series

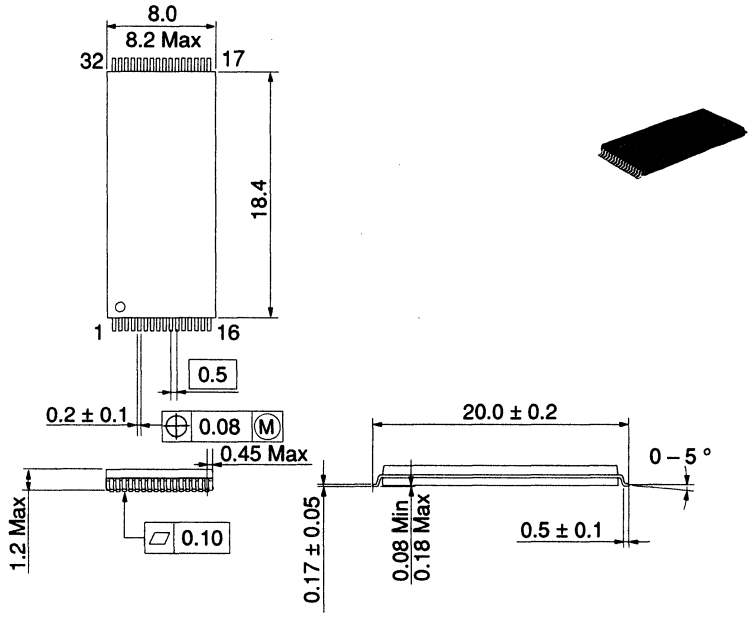
FP-28D	HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series
FP-28DA	HM6264AFP Series, HM 6264ALFP Series, HM6264ALFP-L Series, HM62256FP Series, HM62256LFP Series, HM62256LFP-SL Series, HM62256AFP Series, HM62256ALFP Series, HM62256ALFP-SL Series, HM65256BFP Series, HM65256BLFP Series
FP-32D	HM628128FP Series, HM628128LFP Series, HM628128LFP-SL Series, HM628512FP Series, HM628512LFP Series, HM628512LFP-SL Series, HM658128ADFP Series, HM658128ALFP Series, HM658128ALFP-L Series, HM658512DFP Series, HM658512LFP Series, HM658512LFP-V Series, HM628128ALFP Series, HM628128ALFP-L Series, HM628128ALFP-SL Series, HM62V8128LFP Series, HM62V8128LFP-L Series, HM62V8128LFP-SL Series, HM629128LFP Series, HM629128LFP-L Series, HM629128LFP-SL Series, HM65V8512DFP Series, HM65V8512LFP Series, HM65V8512LFP-V Series, HM62V9128LFP Series, HM62V9128LFP-L Series, HM62V9128LFP-SL Series HM65W8512DFP Series, HM65W8512LFP Series, HM65W8512LFP-V Series

Package Information

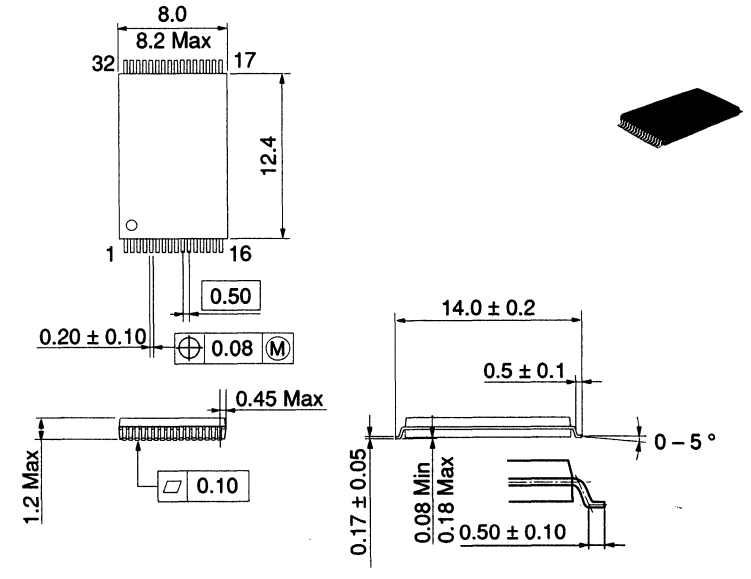
Flat Package

Unit: mm

• TFP-32D



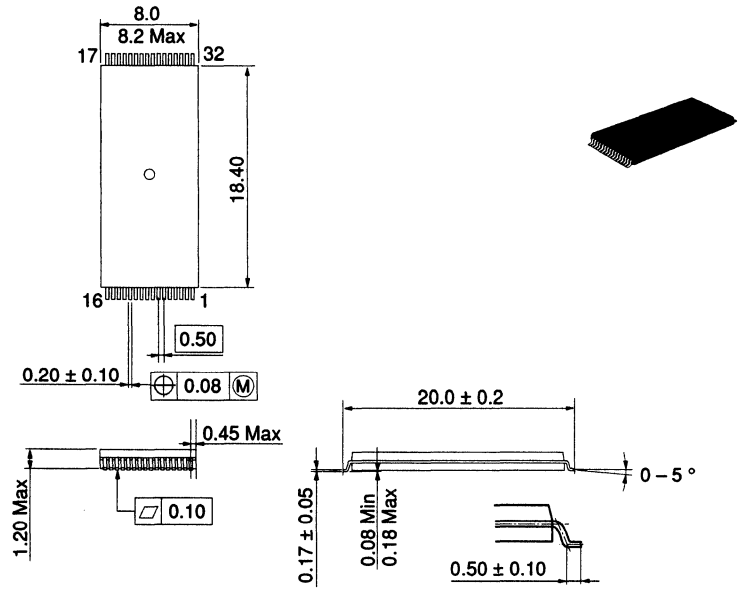
• TFP-32DA



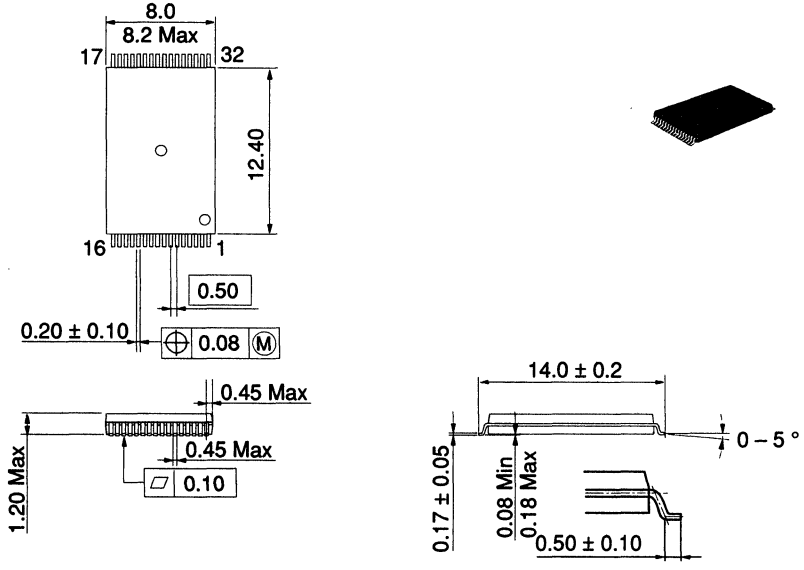
Flat Package

Unit: mm

• TFP-32DR



• TFP-32DAR

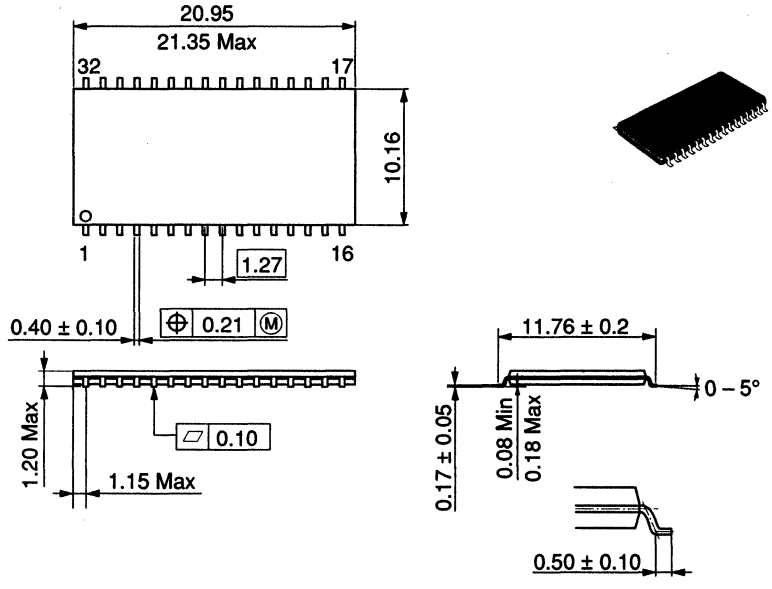


Package Information

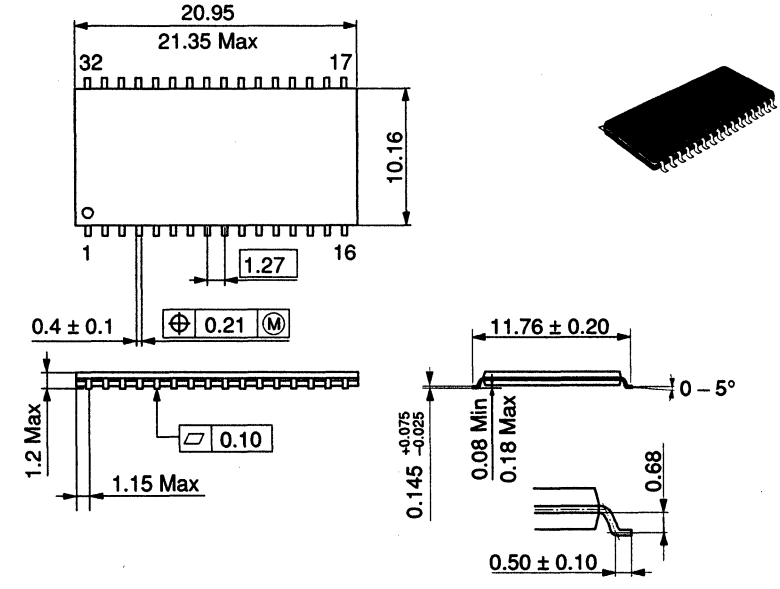
Thin Small-Outline Package

Unit: mm

• TTP-32D



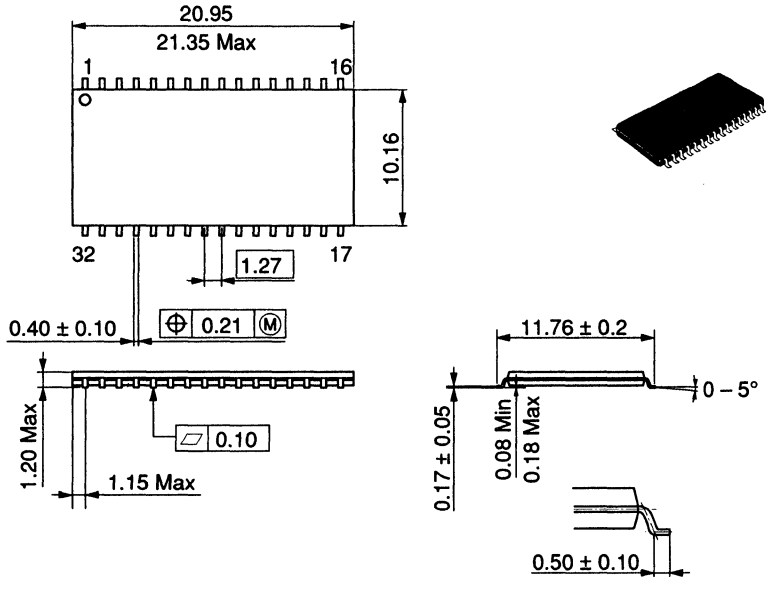
• TTP-32DA



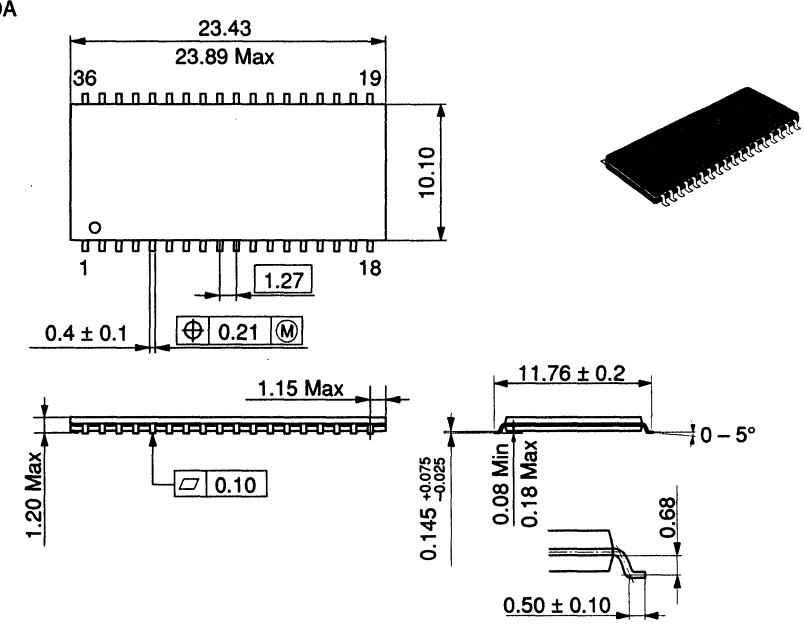
Thin Small-Outline Package

Unit: mm

• TTP-32DR



• TTP-36DA

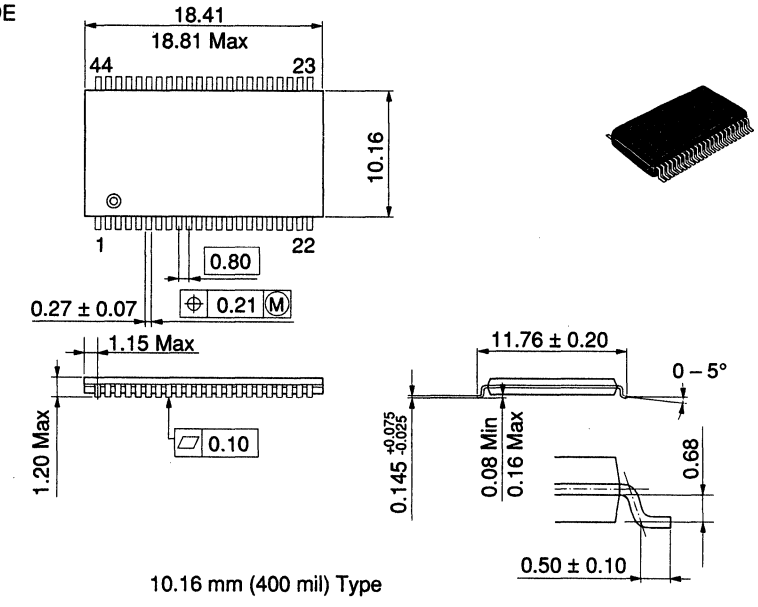


Package Information

Thin Small-Outline Package

Unit: mm

• TTP-44DE



10.16 mm (400 mil) Type

Applicable ICs

TFP-32D	HM628128T Series, HM628128LT Series, HM628128LT-L Series, HM658128ADT Series, HM658128ALT Series, HM658128ALT-L Series, HN28F4001T Series, HM628128ALT Series, HM628128ALT-L Series, HM629128LT Series, HM629128LTL-L Series, HM629128LT-SL Series, HM62V8128LT Series, HM62V8128LT-L Series, HM62V9128LT Series, HM62V9128LT-L Series, HM62V9128LT-SL Series
TFP-32DA	HM62256ALT Series, HM62256ALT-SL Series
TFP-32DR	HM628128R Series, HM628128LR Series, HM628128LR-L Series, HM658128ADR Series, HM658128ALR Series, HM658128ALR-L Series, HN28F4001R Series, HM628128ALR Series, HM628128ALR-L Series, HM62V8128LR Series, HM62V8128LR-L Series
TFP-32DAR	HM62256ALR Series, HM62256ALR-SL Series
TTP-32D	HM658512DTT Series, HM658512LTT Series, HM658512LTT-V Series, HM628512LTT Series, HM628512LTT-SL Series, HN27V101ATT Series, HM65V8512DTT Series, HM65V8512LTT Series, HM65V8512LTT-V Series, HM65W8512DTT Series, HM65W8512LTT Series, HM65W8512LTT-V Series
TTP-32DA	HM671400TT Series, HM671400LTT Series, HM674100TT Series, HM674100LTT Series
TTP-32DR	HM658512DRR Series, HM658512LRR Series, HM658512LRR-V Series, HM65V8512DRR Series, HM65V8512LRR Series, HM65V8512LRR-V Series, HM65W8512DRR Series, HM65W8512LRR Series, HM65W8512LRR-V Series
TTP-36DA	HM101524TT Series, HM67A4101TT Series
TTP-44DE	HM621664HTT Series, HM621664HLTT Series, HM621864HTT Series, HM621864HLTT Series, HM62W1664HTT Series, HM62W1664HLTT Series, HM62W1864HTT Series, HM62W1864HLTT Series

Reliability of Hitachi IC Memories

1. Structure

IC memory devices are classified as NMOS type, CMOS type, and Bi-CMOS type. There are advantages to it's circuit design, layout pattern, degree of integration, and manufacturing process.

All Hitachi memories are produced using standardized design, manufacturing, and inspection techniques. Reliability, a key factor in Hitachi IC design and usage, is enhanced by Test Element Group (TEG) evaluation. This approach ensures the best possible application of our experience and knowledge at every step of IC development.

IC memories consist of memory cells which are circuit patterns arranged within a device at very high density. Examples of memory cell circuitry of MOS memories are shown in Table 1.

The dies of IC memories are encapsulated in various packages. The most common packages are plastic and cerdip. Plastic packages are widely used in many different types of equipment. Cerdip packaging is especially suitable in equipment requiring high reliability. Surface mount packages, such as the plastic leaded chip carrier (PLCC) and small outline package (SOP) have been developed for high density applications.

Hitachi has developed new techniques of IC packaging, thus achieving high levels of reliability. Hitachi plastic IC packages have been improved to match the performance of other hermetically sealed packages.

Table 2 illustrates the appearance and relative sizes of various Hitachi IC packages.

Table 1 Basic Memory Cell Circuit of IC Memories

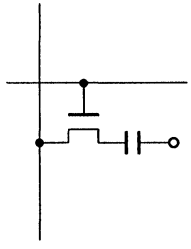
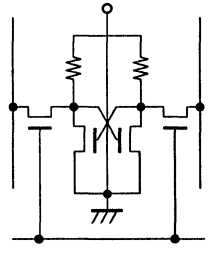
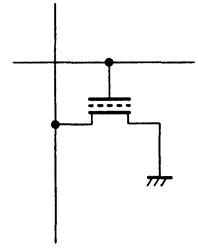
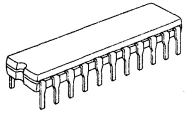
Classification	Dynamic RAM	Static RAM	EPROM
Example of basic cell circuit			

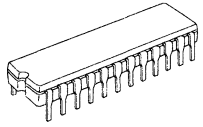
Table 2 IC Memory Package Outline

■ Cerdip

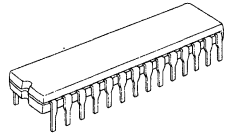
● 22 pin



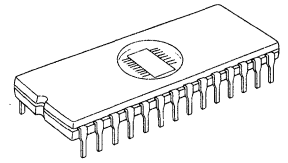
● 24 pin



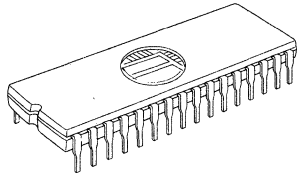
● 28 pin



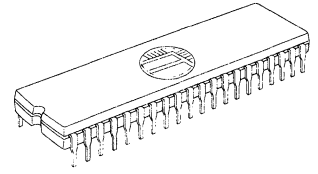
● 28 pin with Lid



● 32 pin with Lid

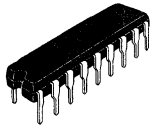


● 40 pin with Lid

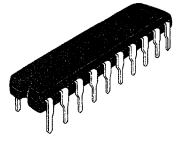


■ Plastic DIP

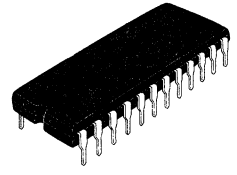
● 18 pin



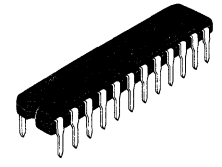
● 20 pin



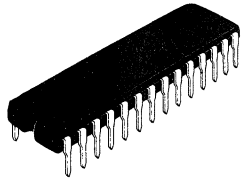
● 24 pin



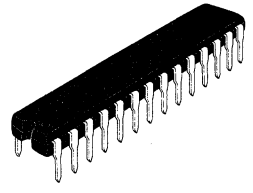
● 24 pin



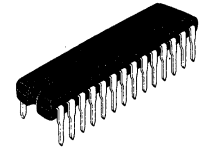
● 28 pin



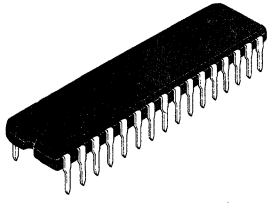
● 28 pin



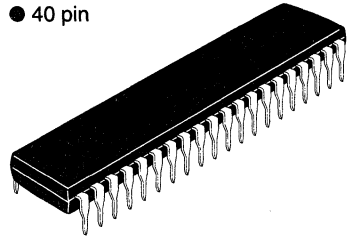
● 28 pin



● 32 pin



● 40 pin



● 42 pin

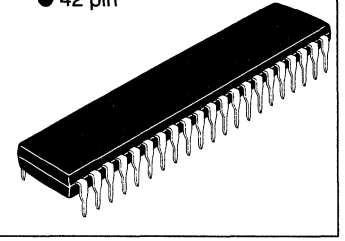
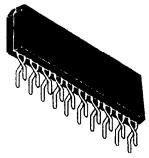


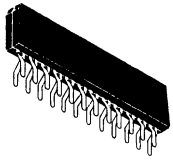
Table 2 IC Memory Package Outline (cont)

■ Zigzag-in-line Plastic

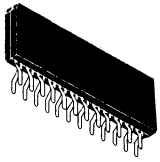
● 20 pin



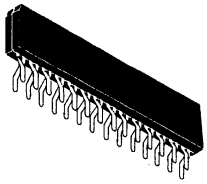
● 24 pin



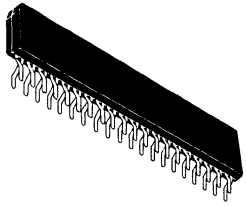
● 24 pin



● 28 pin

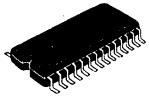


● 40 pin



■ SOP

● 28/32 pin

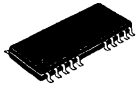


● 48 pin

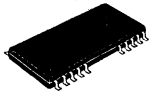
● 20 pin

● 32 pin

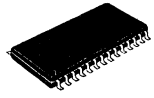
● 20 pin



● 24 pin

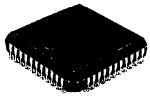


● 28 pin

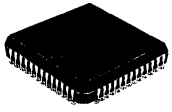


● 32 pin

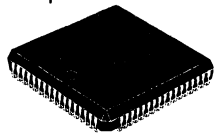
● 44 pin



● 52 pin

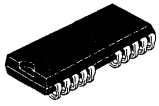


● 68 pin

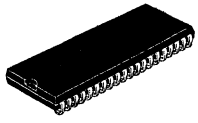


■ SOJ

● 20/26/28/32 pin



● 40 pin



2. Reliability

Hitachi IC memory reliability test results are listed below.

2.1 Reliability Test Data of Hi-BiCMOS Memory

Hi-BiCMOS memory is a recently developed design, based on the latest fine process technologies. Hi-BiCMOS memory offers a combination of the best features of other, earlier devices—the low power consumption and high integrity of CMOS devices, plus the high speed and high drive capability of bipolar (ECL) circuits. Hi-BiCMOS memory also supports the input and output levels of both ECL and TTL devices, which allows interfacing with other devices.
The reliability test data for HM101510F-15 (1M × 1 bit) and HM6708AJP-20 (64k × 4 bits) is listed in Tables 3 and 4.

In normal use, Hi-BiCMOS memory reliability is affected by some limitations based on the circuit composition. Besides the normal constraints of CMOS and bipolar device design, Hi-BiCMOS memory should not be used in applications involving deformed or slow signal waveforms that may cause latch-up or other malfunctions. For further information, refer to the detailed specifications on the data sheet for each Hi-BiCMOS device.

Table 3 Results of Hi-BiCMOS Memory Reliability Tests (1)

	HM101510F-15 (FPG)						HM6709SHJP-10 (SOJ)					
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate	Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate	Remarks
High-temperature pulse operation	Ta = 125°C V_{EE} = –5.2V	328	C.H. 3.28×10^5	0	1/h 3.3×10^{-6}	High-temperature pulse operation	Ta = 125°C/7V V_{CC} = 125°C/7V	280	C.H. 2.8×10^5	0	1/h 3.3×10^{-6}	
								9800	2.4×10^5	1	8.4×10^{-6}	oxide film failure × 1
	Ta = 100°C V_{EE} = –7.0V	32	C.H. 3.2×10^4	0	1/h 2.9×10^{-5}	Moisture endurance	85°C 85% RH 5.5V	210	2.1×10^5	0	4.4×10^{-6}	
High-temperature storage	Ta = 200°C	235	2.35×10^5	0	3.9×10^{-6}	Pressure cooker	121°C 100% RH	80	0.16×10^5	0	5.8×10^{-5}	

Table 4 Results of Hi-BiCMOS Memory Reliability Tests (2)

		HM101510F-15 (FPG)		HM6709SHJP-10 (SOJ)	
Test Item	Test Condition	Samples	Failures	Samples	Failures
Temperature cycling	–55° to +150°C, 100 cycles	180	0	180	0
Soldering heat	260°C, 10 seconds	22	0	22	0
Thermal shock	0° to +100°C, 10 cycles	50	0	50	0
Mechanical shock	1500 G, 0.5 ms, three times each for X, Y, and Z axes	22	0	—	—
Variable frequency vibration	100 to 200 Hz, 20 G, three times each for X, Y, and Z axes	22	0	—	—
Constant acceleration	20000 G, 1 minute, each for X, Y, and Z axes	22	0	—	—

2.2 Reliability Test Data of MOS Memory

2.2.1 MOS DRAM and SRAM Tests

Tables 5, 6, and 7 show the reliability test data on 1-Mbit DRAMs (HM511000, HM514256), 4-Mbit DRAMs (HM514100/HM514400), 16-Mbit DRAMs (HM5116100/HM5116400), 256-kbit SRAM (HM62256), and 1-Mbit SRAM (HM628128FP). The life test is performed at high temperature and high voltage to evaluate product reliability using many samples. For all failures identified in the manufacturing process, the data is analyzed in great detail to improve the quality and reliability of both the process and the finished product.

Table 5 Reliability Data on 1M MOS DRAM

		HM511000P/HM514256P Series (DIP)				HM511000JP/HM514256JP Series (SOJ)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	300	6.00×10^5	0	1.53×10^{-6}	200	4.00×10^5	0	2.30×10^{-6}	* Oxide film failure ×1
	125°C/7 V	1252	4.50×10^5	1*	4.49×10^{-6}	3186	9.34×10^5	0	9.85×10^{-7}	
	150°C/7 V	200	4.00×10^5	0	2.30×10^{-6}	200	4.00×10^5	0	2.30×10^{-6}	
Moisture endurance	85°C 85% RH 5.5 V	420	8.40×10^5	0	1.10×10^{-6}	682	1.36×10^6	0	6.74×10^{-7}	
Pressure cooker	121°C/100% RH	150	4.50×10^4	0	2.04×10^{-5}	200	6.00×10^4	0	1.53×10^{-5}	

Note: Confidence level 60%

		HM511000ZP/HM514256ZP Series (ZIP)				HM511000ATS/HM514256ATS Series (TSOP)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	300	6.0×10^5	0	1.53×10^{-6}	—	—	—	—	
	125°C/7 V	4368	6.0×10^5	0	1.53×10^{-6}	1100	1.5×10^5	0	6.22×10^{-6}	
	150°C/7 V	180	3.6×10^5	0	2.56×10^{-6}	—	—	—	—	
Moisture endurance	85°C 85% RH 5.5 V	426	8.5×10^5	0	1.08×10^{-6}	200	2.0×10^5	0	4.60×10^{-6}	
Pressure cooker	121°C/100% RH	125	3.7×10^4	0	2.70×10^{-5}	100	3.0×10^4	0	3.07×10^{-5}	

Note: Confidence level 60%

Table 6 Reliability Data on 4M and 16M DRAM

Test Item	Test Condition	HM514100AS/HM514400AS Series (SOJ) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	HM514100AZ/HM514400AZ Series (ZIP) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	823	8.2×10^5	0	1.12×10^{-6}	—	—	—	—	*
	125°C/7 V	2514	8.3×10^5	1*	2.43×10^{-6}	1100	1.5×10^5	0	6.22×10^{-6}	Oxide film failure ×1
	150°C/7 V	151	1.5×10^5	0	6.09×10^{-6}	—	—	—	—	
Moisture endurance	85°C 85% RH 5.5 V	317	3.2×10^5	0	2.90×10^{-6}	300	3×10^5	0	3.07×10^{-6}	
Pressure cooker	121°C/100% RH	100	3×10^4	0	3.07×10^{-5}	100	3×10^4	0	3.07×10^{-5}	

Note: Confidence level 60%

Test Item	Test Condition	HM514100AT/HM514400AT Series (TSOP) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)
High-temperature operation	125°C/5.5 V	—	—	—	—
	125°C/7 V	1100	1.5×10^5	0	6.22×10^{-6}
	150°C/7 V	—	—	—	—
Moisture endurance	85°C 85% RH 5.5 V	300	3.0×10^5	0	3.07×10^{-6}
Pressure cooker	121°C/100% RH	100	3.0×10^4	0	3.07×10^{-5}

Note: Confidence level 60%

Test Item	Test Condition	HM5116100J/HM5116400J Series (SOJ) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	HM5116100TT/HM5116400TT Series (TSOP) Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/7.0 V	12436	5.97×10^5	0	1.68×10^{-6}	22	4.40×10^4	0	2.27×10^{-5}	*
	125°C/7.5 V	5235	2.51×10^5	1*	3.98×10^{-6}	—	—	—	—	Oxide film failure ×1
	125°C/7 V	500	1.00×10^6	0	1.00×10^{-6}	—	—	—	—	
Moisture endurance	85°C 85% RH 5.5 V	306	6.12×10^5	0	1.63×10^{-6}	129	2.58×10^6	0	3.88×10^{-6}	
Pressure cooker	121°C/100% RH	130	3.90×10^4	0	2.56×10^{-5}	38	1.14×10^4	0	8.77×10^{-5}	

Note: Confidence level 60%

Table 6 Reliability Data on 4M and 16M DRAM (cont)

		HM5116100Z/HM5116400Z Series (ZIP)			
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)
High-temperature operation	125°C/7.0 V	—	—	—	—
	125°C/7.5 V	—	—	—	—
	125°C/7 V	129	2.58×10^{5}	0	3.88×10^{-6}
Moisture endurance	85°C 85% RH 5.5 V	129	2.58×10^{5}	0	3.88×10^{-6}
Pressure cooker	121°C/100% RH	38	1.14×10^{4}	0	8.77×10^{-5}

Note: Confidence level 60%

Table 7 Reliability Data on 256k and 1M MOS SRAM

		HM62256FP (SOP)				HM628128FP (SOP)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	3088	3.11×10^{6}	0	2.96×10^{-7}	1946	1.08×10^{6}	0	8.52×10^{-7}	*1
	125°C/7 V	455	4.55×10^{5}	0	2.02×10^{-6}	1096	6.78×10^{5}	1*1	2.98×10^{-6}	Foreign ×2
	150°C/7 V	103	1.00×10^{5}	1*1	2.02×10^{-5}	125	2.05×10^{5}	0	4.49×10^{-6}	
Moisture endurance	85°C/85% RH 7 V	680	6.80×10^{5}	0	1.35×10^{-6}	287	4.14×10^{5}	0	2.22×10^{-6}	*2 Leak ×1
Pressure cooker	121°C/100% RH	320	6.40×10^{4}	1*2	3.16×10^{-5}	150	3.90×10^{4}	0	2.36×10^{-5}	

Note: Confidence level 60%

2.2.2 Reliability Test Data on EPROM

There are two types of EPROM: the conventional EPROM with a transparent window over the active device area; and the one-time-programmable ROM (OTPROM) packaged in plastic. Table 8 shows the reliability test data on the 1-Mbit EPROM (HN27C101A, HN27C301A) and 4-Mbit EPROM (HN27C4096).

The high temperature failures shown in Table 8 are due to data dissipation in the memory cells. By absorbing thermal energy, the electrons in the floating gates are activated and dissipated. In actual usage, however, this is not a significant problem since this phenomenon is highly dependent on temperature (about 1.0 eV of activated energy) that should not appear during normal operation.

The moisture resistance of the OTPROM is satisfactory.

Table 9 shows an example of PROM derating. The primary derating parameter is generally temperature since other operating parameters are specified. The maintaining of low junction temperature during device mounting is especially important for a stable application operation (relative to access time, refresh time, and other characteristics).

Table 8 Reliability Data on 1-Mbit and 4-Mbit MOS EPROMs

		HN27C101A/HN27C301A (Cerdip/Plastic)				HN27C4096 (Cerdip)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	240	4.52×10^{5}	0	2.03×10^{-6}	220	4.18×10^{5}	0	2.20×10^{-6}	*
	125°C/7 V	570	9.55×10^{5}	0	0.96×10^{-6}	445	8.45×10^{5}	0	1.09×10^{-6}	Data dissipation×43
High-temperature bake	175°C	290	5.51×10^{5}	0	1.67×10^{-6}	180	3.60×10^{5}	0	2.56×10^{-6}	
	200°C	260	4.02×10^{5}	0*	2.29×10^{-6}	130	2.60×10^{5}	1*	7.77×10^{-6}	
	250°C	200	2.09×10^{5}	2*	1.48×10^{-5}	110	1.10×10^{5}	40*	3.64×10^{-4}	
Moisture endurance	85°C/85% RH 5.5 V	300	5.42×10^{5}	0	1.70×10^{-6}	—	—	—	—	Data of 1M OTPROM
Pressure cooker	121°C/100% RH	50	0.10×10^{5}	0	9.20×10^{-5}	—	—	—	—	

Note: Confidence level 60%

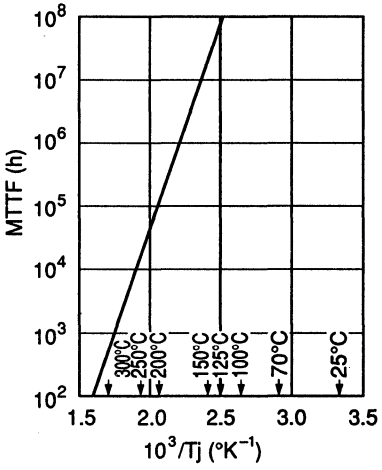
2.2.3 Reliability Test Data on MASK ROM

Table 10 shows the reliability test data for the 16-Mbit and 8-Mbit MASK ROMs. The MASK ROM is patterned in the manufacturing process, so data dissipation is not generated during high temperature operations, unlike EPROM and EEPROM devices.

Table 9 Example of HN27C101/HN27C301 Derating

Factor	Temperature
Failure criteria	Electrical characteristics, function test
Failure mechanism	Increase of leakage current, and others

Results:
The result of high temperature baking of the PROM is shown in the figure at right.



Note: As shown in the figure, decreasing junction temperature will improve reliability. The junction temperature can be calculated by the formula: $Tj = Ta + \theta ja \cdot Pd$ where θja is about 100°C/W with no air flow and about 60° to 70°C/W with 2.5 m/s air flow.

Table 10 Reliability Data on 16-Mbit and 8-Mbit MASK ROMs

		HN624016P (Plastic)				HN62408P (Plastic)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/h)	Remarks
High-temperature operation	125°C/5.5 V	140	1.4×10^5	0	6.6×10^{-6}	200	4.0×10^5	0	2.3×10^{-6}	
	125°C/7 V	100	1.0×10^5	0	9.2×10^{-6}	130	1.3×10^5	0	7.1×10^{-6}	
Moisture endurance	85°C/85% RH 5.5 V	100	1.0×10^5	0	9.2×10^{-6}	150	1.5×10^5	0	6.1×10^{-6}	
Pressure cooker	121°C/100% RH	60	3.0×10^4	0	3.1×10^{-5}	90	4.5×10^4	0	2.0×10^{-5}	

Note: Confidence level 60%

2.2.4 Reliability Test Data on MOS Memory (environmental testing)

Tables 11 and 12 list MOS memory environmental test data, showing excellent results without any failures, even in severe environments.

In MOS transistor operations, V_{TH} is a basic process parameter. While in use, MOS memory exhibits almost no change in V_{TH}, largely due to designed-in surface stabilization technology and extremely clean production processes.

Figure 3 shows examples of time dependent degradation for minimum V_{CC} and access time t_{RAC} for 4-Mbit DRAM under high temperature operation test conditions.

2.3 Change of Electrical Characteristics on IC Memories

The degradation of I_{CBO} and h_{FE} are the main factors of performance degradation for inner cell transistors in bipolar memory. The actual element design, however, specifies the operation in a range at which no degradation occurs. In this normal situation, no changes in the operating characteristics, including access time, will arise. Time dependencies in the access time for the HM100500 and HM6708P are shown in Figures 1 and 2.

Table 11 Reliability Data on MOS Memory (1)

		HM511000P (DIP)		HM511000JP (SOJ)		HM511000ZP (ZIP)		HM511000ATS (TSOP)		HM62256FP (SOP)		HM628128FP (SOP)		EPROM (Cerdip)	
Test Item	Test Condition	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures
Temperature cycling	–55° to 150°C 10 cycles	3755	0	2786	0	1500	0	900	0	3328	0	1215	0	2850	0
Temperature cycling	–55° to 150°C 500 cycles	150	0	200	0	175	0	250	0	482	0	210	0	520	0
Thermal shock	–65° to 150°C 15 cycles	77	0	100	0	50	0	22	0	76	0	77	0	100	0
Soldering heat	260°C, 10 sec	22	0	22	0	22	0	22	0	22	0	35	0	22	0
Mechanical shock	1500 G, 0.5 ms	—	—	—	—	—	—	—	—	—	—	—	—	38	0
Variable frequency vibration	100 to 2000 Hz 20 G	—	—	—	—	—	—	—	—	—	—	—	—	38	0
Constant acceleration	6000 G	—	—	—	—	—	—	—	—	—	—	—	—	38	0

Table 12 Reliability Data on MOS Memory (2)

		HM514400AS (SOJ)		HM514400AZ (ZIP)		HM514400AT (TSOP)		HM5116400J (SOJ)		HM5116400TT (TSOP)		HN624016P (DIP)		HN62408P (DIP)	
Test Item	**Test Condition**	**Samples**	**Failures**	**Samples**	**Failures**	**Samples**	**Failures**	**Samples**	**Failures**	**Samples**	**Failures**	**Samples**	**Failures**	**Samples**	**Failures**
Temperature cycling	–55° to 150°C 10 cycles	949	0	1000	0	900	0	1438	0	350	0	330	0	370	0
Temperature cycling	–55° to 150°C 500 cycles	200	0	200	0	100	0	141	0	129	0	70	0	12	0
Thermal shock	–65° to 150°C 15 cycles	22	0	22	0	22	0	32	0	22	0	22	0	22	0
Soldering heat	260°C, 10 sec	22	0	600	0	22	0	22	0	22	0	22	0	22	0

Example	
Device name	HM101510F-15
Test condition	Ta = 125°C, V_{EE} = –5.2 V all bit scanning
Failure criteria	t_{AA} = 15 ns
Failure mechanism	Surface degradation
Results: Access time is stabilized.	

Example of Time Dependent Degradation in Access Time for Hi-BiCMOS Memory

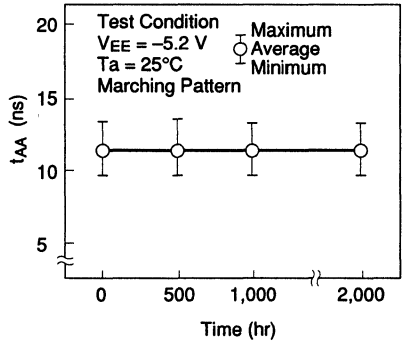


Figure 1 Time Dependent Degradation in Access Time for Hi-BiCMOS Memory

Example	
Device name	HM6709SHJP-10
Test condition	Ta = 125°C, V_{CC} = 7.0 V all bit scanning
Failure criteria	V_{CC} = 4.5 V, t_{AA} = 10 ns
Failure mechanism	Surface degradation

Results:
Both V_{CC} (min) and t_{AA} are stabilized.

Examples of Time Dependent Degradation in V_{CC} min and t_{AA} for Hi-BiCMOS Memory

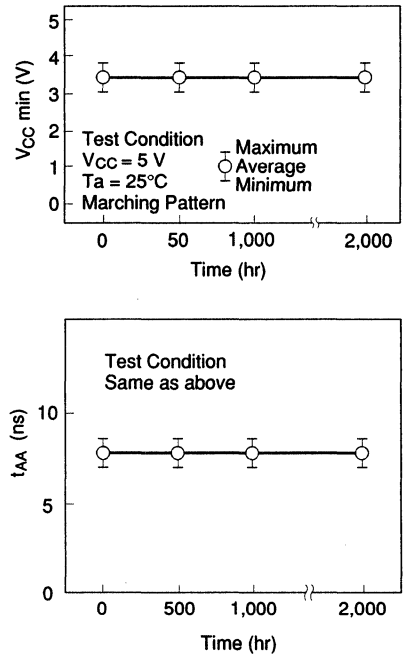


Figure 2 Time Dependent Degradation in Minimum V_{CC} and t_{AA} for Hi-BiCMOS Memory

Example	
Device name	HM514400AS
Test condition	Ta = 125°C, V_{CC} = 7 V all bit scanning
Failure criteria	ΔV_{CC} = 1.0 V, Δt_{RAC} = 6 ns
Failure mechanism	Surface degradation

Results:
V_{CC} margin and access time (t_{AA}) are stabilized and are within the failure criteria.

Note: Test accuracy is 0.2 V, 2 ns.

Example of Time Dependent Degradation in V_{CC} min and t_{RAC} for MOS Memory

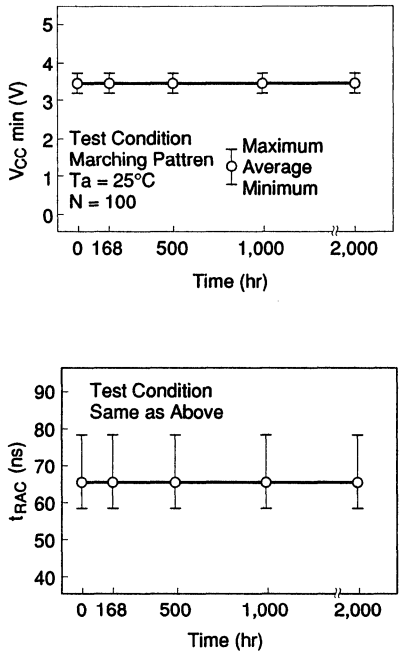


Figure 3 Time Dependent Degradation in Minimum V_{CC} and t_{RAC} for MOS Memory

2.4 Failure Mode Rate

Figures 4 and 5 show examples of failure modes identified in user applications. Since IC memories require the finest pattern process technology, the percentage of failures due to factors such as pinholes, photoresist defects, and foreign materials tends to increase along with product complexity. Hitachi has continued to improve its fabrication process technology, and performs 100% high temperature "burn-in" screening as a standard part of manufacturing.

Hitachi collects and analyzes customer usage data as part of a program designed to achieve higher product reliability. This analysis is a very useful feature of the program.

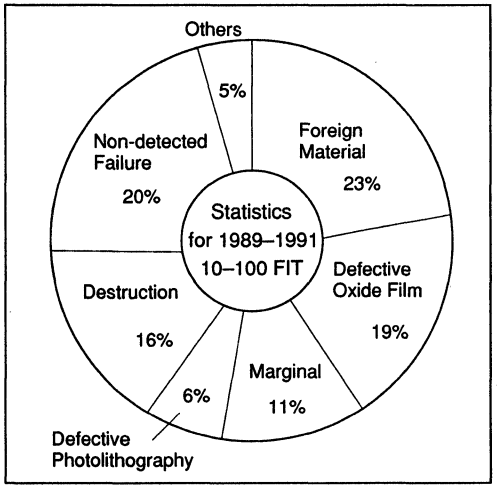


Figure 4 Failure Mode Rates for Hi-BiCMOSMemory

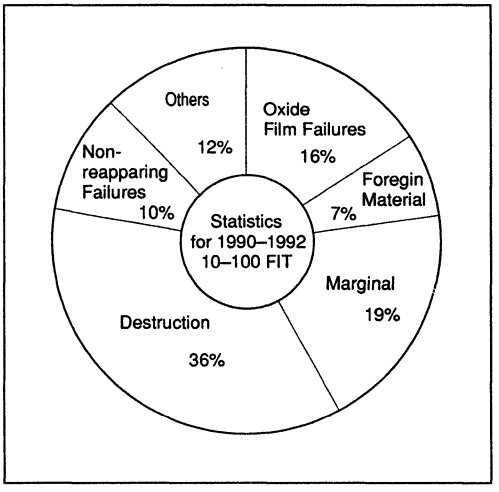


Figure 5 Failure Mode Rates for MOS Memory

3. Reliability of Semiconductor Devices

3.1 Reliability Characteristics for Semiconductor Devices

Hitachi semiconductor devices are designed, manufactured, and inspected to achieve a high level of reliability. System reliability is improved by combining highly reliable components with the proper environmental conditions. This section describes the reliability characteristics, failure types, and their mechanisms in terms of devices. First, the semiconductor device characteristics are examined in light of their reliability.

1. Semiconductor devices are essentially structure sensitive as seen in surface phenomena. Fabricating devices requires precise control of a large number of process steps.

2. Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

3. Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin-film surfaces sometimes exhibit different physical characteristics from the bulk quantities of identical materials.

4. Semiconductor device technology advances very quickly, and therefore many new devices have been developed using new processes over a short period of time. Hence, conventional device reliability data cannot always be used for comparisons.

5. Semiconductor devices are characterized by volume production. Therefore, manufacturing variation is an important consideration.

6. Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially semipermanently operable. However, failures caused by worn or aged materials and migration should also be reviewed when electrode and package materials are not suited for particular environmental conditions.

7. Component reliability may depend on the device mounting, conditions used, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength. Device reliability is generally represented by a failure rate. "Failure" implies that a device has lost its function, and includes intermittent degradation or complete destruction.

   Generally, the failure rate of electrical components and equipment is represented by the "bathtub" curve as shown in Figure 6. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which indicates an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be represented physically as well as statistically. Both failure aspects have been thoroughly analyzed to establish a high level of reliability.

3.2 Failure Types and Their Mechanisms

3.2.1 Failure Physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering." It is used to examine the physical mechanism of failures, in terms of atoms and molecules, to improve device reliability. This physical approach was introduced to the reliability field to answer the demand for minimized developmental cost and time. These conditions were derived from the development of solid-state physics (semiconductor physics) since the 1940's and from other associated device development. Failure physics has been employed to do the following:

1. Detect failed devices as soon as possible.
2. Establish models and equations used for failure prediction.
3. Evaluate the reliability in short time periods by accelerated life testing.

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage, and usage, by including physics as a basic technology to conventional experimental and statistical approaches.

3.2.2 Failure Types and Their Mechanisms

The physical aspects of device failures are covered in this section. Semiconductor device failures are basically categorized as open, short circuit, deterioration, and miscellaneous failures. These failures and their causes are summarized in Table 13. Typical failure mechanisms are as follows:

1. Surface deterioration

The pn junction has a charge density of 10^{14} to 10^{20} cm^{-3}. If charges exceeding the above density are accumulated on the pn junction surface, the electrical characteristics of the junction will tend to vary. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by the surface channels still exists. Surface deterioration depends heavily on the applied temperature and voltage and is often handled by the reaction model.

An example of a recent failure is the surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS}, thus raising the internal voltage and establishing a strong electric field near the drain of the MOS device. This may be a result from reduced device geometry (from 2 µm to 0.8 µm) as technological advances have occurred in production methods. Generated hot carriers may affect the surface boundary characteristics on a section of the gate oxide film, resulting in the degradation of the threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have consistently employed improved designs and process techniques to prevent these problems. However, as processes become even finer, surface deterioration may become a serious problem.

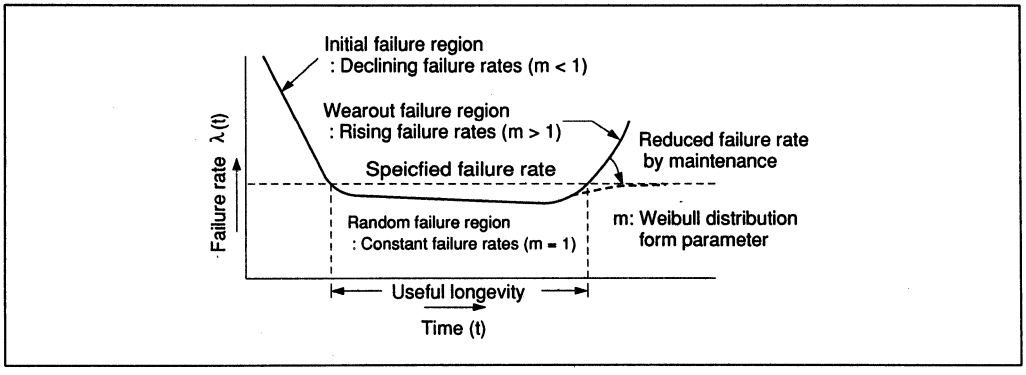


Figure 6 Typical Failure Rate Curve

2. Electrode-related failures
The concern for electrode-related failures has increased as multilayer metallization has become more complex. Noticeable failures include electromigration and Al metallization corrosion in plastic sealed packages.

a. Electromigration
This phenomenon takes place when metal atoms are moved by a large current of about 10^6 A/cm^2 that is supplied to the metal. When ionized atoms collide with the current of electrons, an "electron wind" is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at the opposite side. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause short circuits in multimetal lines.

b. Multimetal line related failures
Major failures associated with multimetal lines include increased leakage currents, short circuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

c. Al line corrosion and disconnection
When plastic encapsulated devices are subjected to high temperatures, high humidity, or a bias-applied condition, the Al electrodes in the devices can cause corrosion or disconnection (Figure 7). Under high temperature and high humidity, corrosion is randomly generated over the element surface.
However, after an extended period of time, such corrosion does not significantly increase. This type of failure is possibly due to initial failures associated with manufacturing variances. It is also known that such failures can be generated when the adhesion surface between an element

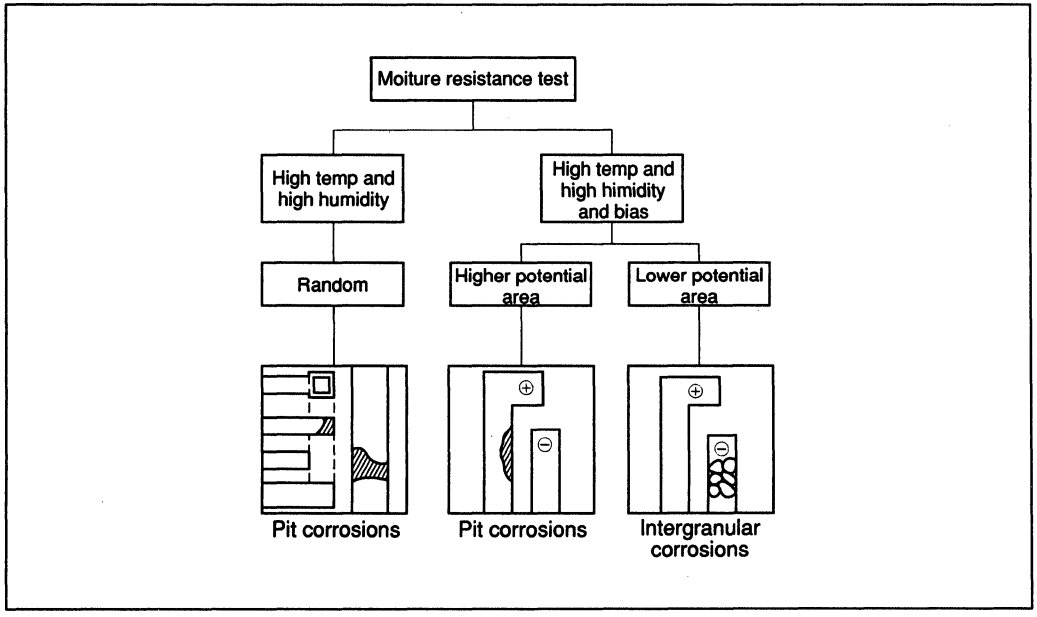


Figure 7 Categorized Al Corrosions

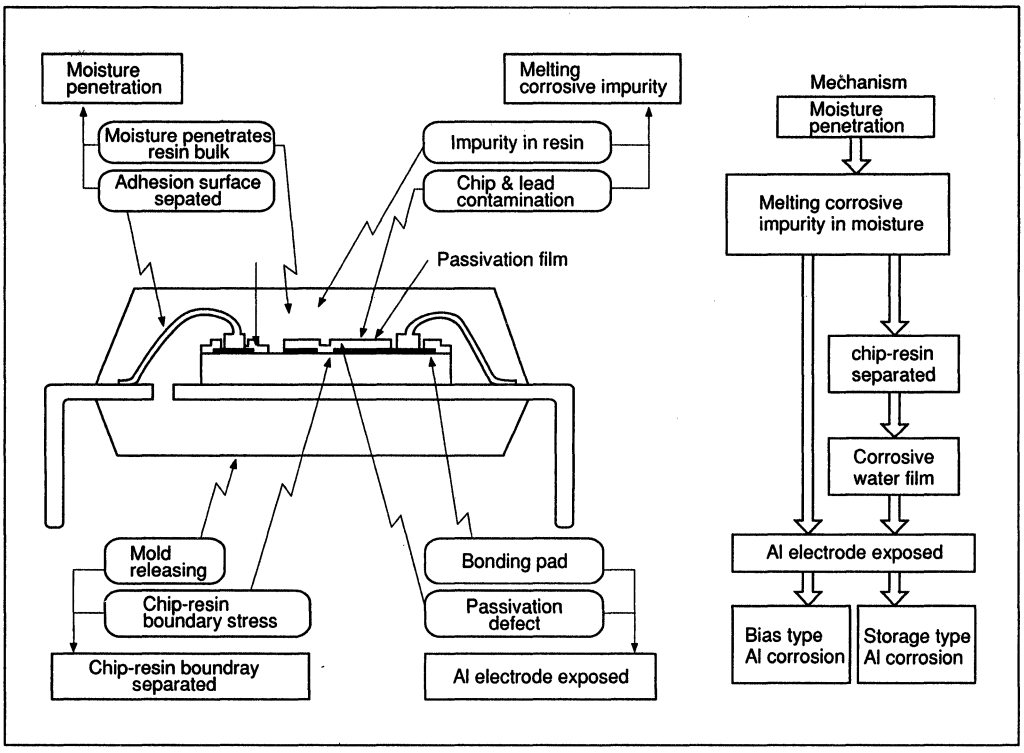


Figure 8 Plastic Package Cross Section and Al Corrosion Mechanism

and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high temperature, high humidity condition, on the other hand, pit corrosion is generated in higher potential areas while in lower potential areas, intergranular corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Figure 8.

3. Bonding related failures

   a. Degradation caused by intermetallic formation

   Bonding strength degradation and contact resistance increase are caused by compounds formed in the connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

b. Wire creep
Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introduced to the intergranular system. Bonding under usual conditions with no abnormal loop configuration failures does not cause this failure, unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

c. Chip crack
With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element method and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

d. Reduced maximum power dissipation
For power devices, heat fatigue due to thermal expansion coefficient mismatches among different materials deteriorates thermal resistance. This results in decreased maximum power dissipation.

4. Sealing related failures
Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

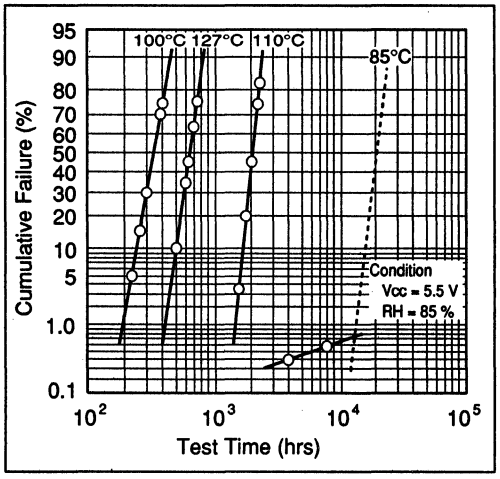


Figure 9 An Example of Moisture Resistance by High Temperature, High Humidity, and High Bias

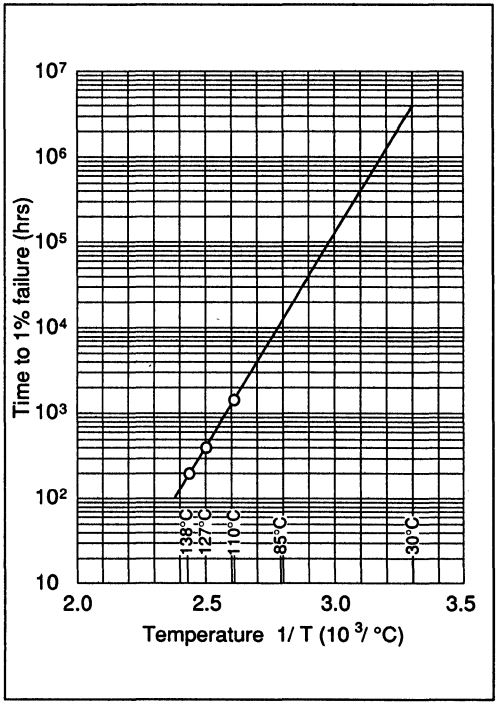


Figure 10 Relationship Between Temperature and Time to 1% Failure (RH = 85%)

— Al line corrosion on the chip surface due to slight moisture and reactions between different ionized materials.
— Intermittent moving foreign metals causing short circuiting.
— Al line corrosion due to extraneous H_20 caused by hermetic failure.

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parasitic effects and metal shorts. The foreign matter detection method is specified by the MIL-STD-883C, PIND (particle impact noise detection) test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying it.

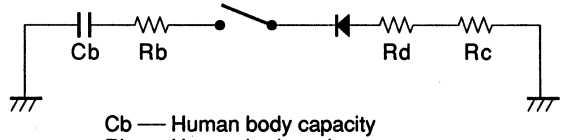
5. Disturbance

a. Electrostatic discharge destruction
Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure: the human body model, a charged device model, and a field induced model.
The human body is easily charged. A person just walking across a carpet can be charged up to 15,000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Figure 11. The human body's capacitance C_b and resistance R_b are 100 to 200 pF and 1000 to 2000 Ω, respectively. Assuming a body is charged with 2000 V, the dissipated energy is obtained as follows: With a time constant of 10^{-7}s, the dissipated energy is 2 kW, which is enough to destroy a small area of a chip.

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Figure 12. Device size and device position relative to ground are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by nearby high voltage. Since the capacitors or leads of a device act like antennas, the following cases will possibly cause its destruction.
— A device is incorporated into a high electric field such as a CRT.
— A device is left under a high-frequency electric field.
— A device is moved within a container charged at high voltage, such as a tube.

b. Latch-up
Latch-up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply, or noise is



Cb — Human body capacity
Rb — Human body resistance
Rd — Device resistance
Rc — Resistance between device and ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} J$$

Figure 11 Equivalent Circuit of the Human Body Model

applied, or when a device is operated from two sources having different setup voltages. These cases can cause input or output current to flow in the opposite direction from the usual flow, which triggers parasitic thyristors. This results in an excessive current flowing between a power supply and ground. This phenomenon continues until the power is removed or the current flow is reduced to a certain level. Once latch-up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch-up. Input or output currents that trigger latch-up start to flow under the following conditions.

$V_{in} > V_{CC}$ or $V_{in} < GND$ for input level
$V_{out} > V_{CC}$ or $V_{out} < GND$ for input level

Circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

c. Soft errors

When α-particles are generated from uranium or thorium on or near the silicon surface of an LSI chip and bombard the Si substrate, electron-hole pairs are formed. They act as noise to memory cell nodes and data lines, which results in data errors. This type of error occurs temporarily and is called a soft error. This phenomenon is shown in Figure 13. Only electrons from among the electron-hole pairs are collected into a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, an organic material, PIQ, is applied to the surface of the device.

6. Fine Geometry Related Problems

LSI circuit geometry has been reduced down to 0.8 μm, and further reductions are expected. However, while transmission line dimensions have undergone this substantial reduction in size, power supplies have not been correspondingly adjusted for 5 V use. Problems associated with finer geometries are shown in Table 14.

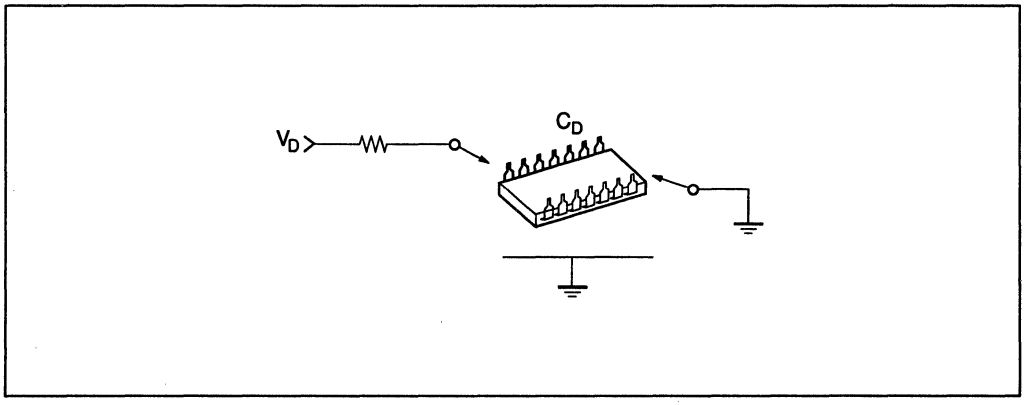


Figure 12 Equivalent Circuit of a Charged Model

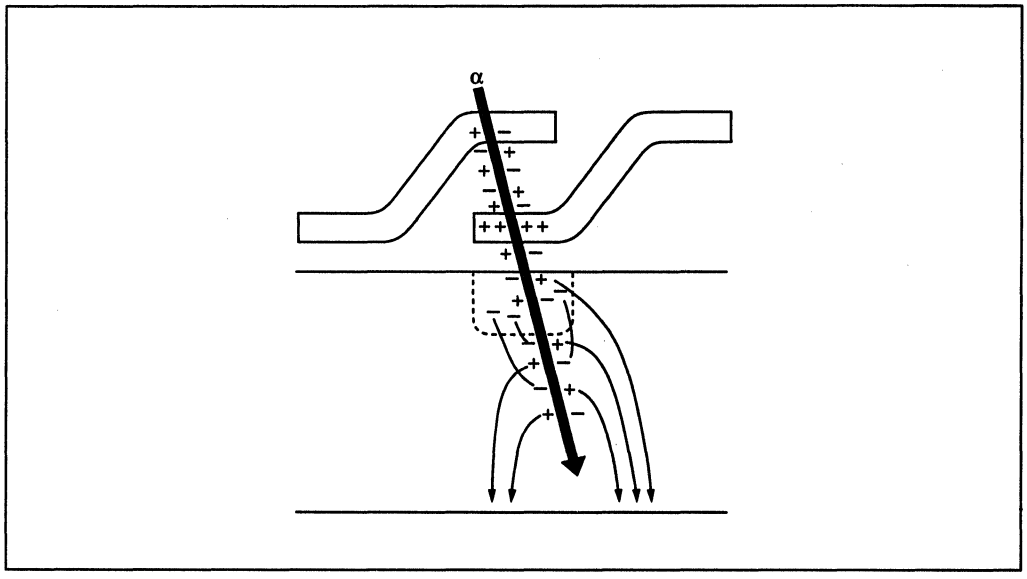


Figure 13 Soft Errors Caused by α-Particles in Dynamic Memory

Table 13 Failure Causes and Mechanisms

Failure Related Causes		Failure Mechanisms	Failure Modes
Passivation	Surface oxide film, insulating film between metallizations	Pin hole, crack, uneven thickness, contamination, surface inversion, hot carrier injected	Degradation of breakdown voltage, short, leak current increased, h_{FE} degraded, threshold voltage variation, noise
Metallization	Interconnection, contact, through hole	Flaw, void, mechanical damage, break due to uneven surface, non-ohmic contact, insufficient adhesion strength, improper thickness, electromigration, corrosion	Open, short, resistance increased
Connection	Wire bonding, ball bonding	Bonding runout, compounds between metals, bonding position mismatch, bonding damaged	Open, short resistance increased
Wire lead	Internal connection	Disconnection, sagging, short	Open, short
Diffusion, junction	Junction diffusion, isolation	Crystal defect, crystallized impurity, photo resist mismatching	Degradation of breakdown voltage, short

Table 13 Failure Causes and Mechanisms (cont)

Failure Related Causes		Failure Mechanisms	Failure Modes
Die bonding	Connection between die and package	Peeling chip, crack	Open, short, unstable operation, thermal resistance increased
Package sealing	Package, hermetic seal, lead plating, hermetic package and plastic package, filler gas	Integrity, moisture ingress, impurity gas, high temperature, surface contamination, lead rust, lead bend, break	Short, leakage current increased, open, corrosion soldering failure
Foreign matter	Foreign matter in package	Dirt, conducting foreign matter, organic carbide	Short, leakage current increased
Input/output pin	Electrostatistics, excessive voltage, surge	Human body charged device	Short, open, fusing
Disturbance	α particle	Electron hole generated	Soft error
	High electric field	Surface inversion	Leakage current increased

Table 14 Finer Geometry Related Problems

Item	Problems	Countermeasure
5 V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering • Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability • CMOS latch up • Mask alignment margin • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical and horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

Quality Assurance of IC Memories

1. Views on Quality and Reliability

Hitachi products should always meet individual users' purposes and required quality levels, maintaining satisfactory performance for general applications. Hitachi works continuously to assure high reliability standards for our IC memories in actual usage. To meet user needs and to cover expanding applications, Hitachi has defined these goals:

1. Establish reliability by design during new product development.
2. Establish quality at all steps in the manufacturing process.
3. Strengthen the inspection process at all points.
4. Improve product quality based on user data.

Furthermore, to reach the highest quality and performance levels, development and production teams cooperate very closely with Hitachi research laboratories. All these methods together make it possible for Hitachi to meet and exceed user requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

The establishment of reliability targets is important in manufacturing and marketing, as well as in determining function and price. Practically, the reliability targets cannot be determined from failure rates produced by any single common test condition; they are based on many factors such as equipment characteristics, target system purposes, derating applied during design, operating conditions, and maintenance requirements.

2.2 Reliability Design Factors

Timely analysis and execution are essential to achieve performance based on reliability targets. The primary design items of interest are design standardization, device process and structural design, design review, and reliability testing.

1. Design standardization
   Design standardization requires the establishment of design rules and the specification of parts, materials, and processes. When design rules are being established for the circuit, cell, and layout designs, critical quality and reliability features should also be examined. By doing this effectively, the use of standardized processes or materials, even in newly developed products, should generate much higher reliability (with the possible exception of special requirements or functions).

2. Device process and structural design
   It is important during device design to consider the total balance of process design, structural design, and circuit and layout design. Especially in the case of applying new processes or new materials, at Hitachi we study the technology in depth prior to any detailed device development.

3. Reliability testing by test site
   The test site is also called the test pattern. It is a useful method for evaluating the reliability of complex ICs and complicated functions.

   a. The purposes for the test site are:
   — To make clear definitions about fundamental failure modes
   — To analyze relationships between failure modes and manufacturing processes and/or conditions
   — To analyze failure mechanisms
   — To establish QC points in manufacturing

   b. The effects of the test site are:
   — Evaluation of common fundamental failure modes and failure mechanisms
   — Determination of predominant failure modes, and comparisons with field experiences
   — Analysis of relationships between failure causes and manufacturing factors
   — Simplification of testing

2.3 Design Review

Design review is a method to systematically confirm whether or not a design satisfies the performance required by users, whether it meets all specifications, and whether the technical items accumulated in test data and application data are effectively utilized.

In addition, from the standpoint of comparisons to competitive products, a major focus of the design review is to insure the quality and reliability of the product. At Hitachi, the design review is performed as a part of new product development, and when changing existing products.

The following items are considered in design review.

1. Describing the product based on specified design documents.

2. Planning and executing each product function and program (such as calculations) by considering the product and its documentation from the standpoint of each participant. Experiments and further investigations are indicated if any results are not exactly as expected.

3. Determining the contents and methods of reliability testing based on design documents and drawings.

4. Checking manufacturing process ability to achieve design goals.

5. Arranging preparations for production.

6. Planning and executing each product function and program of all design changes proposed by individual specialists. Generating tests, experiments, and calculations as needed to confirm the results of each design change.

7. Refering to past performance and failure experiences with similar devices. Confirming the prevention of any repetition of such experience, and planning and executing a test program to prove this level of performance.

At Hitachi, design reviews including these steps of analysis and decision are made using individual check lists according to each objective.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

At Hitachi, these are the general purposes of quality assurance:

1. Problems are resolved within each step, so that by the final stage of production even very small potential failure factors will be removed.
2. Information developed at every step is used in other steps, as indicated, to improve quality in the entire production sequence, and therefore achieve satisfactory levels of reliability and performance.

3.2 Qualification

For maximum product quality and reliability, qualification tests are done at each stage of trial production and mass production, based on design reliability as described in Section 2 "Reliability Design of Semiconductor Devices."

These are the purposes of qualification at Hitachi.

1. Qualify the product objectively from a customer standpoint (as by a third party).
2. Consider the failure experiences and data provided by customers.
3. Qualify every change in design and process.
4. Qualify, with special emphasis, all final choices of parts, materials, and processes.
5. Establish control points within the production procedure by considering the process ability and factors of manufacturing variance.

Figure 1 shows the general outline of design qualification at Hitachi.

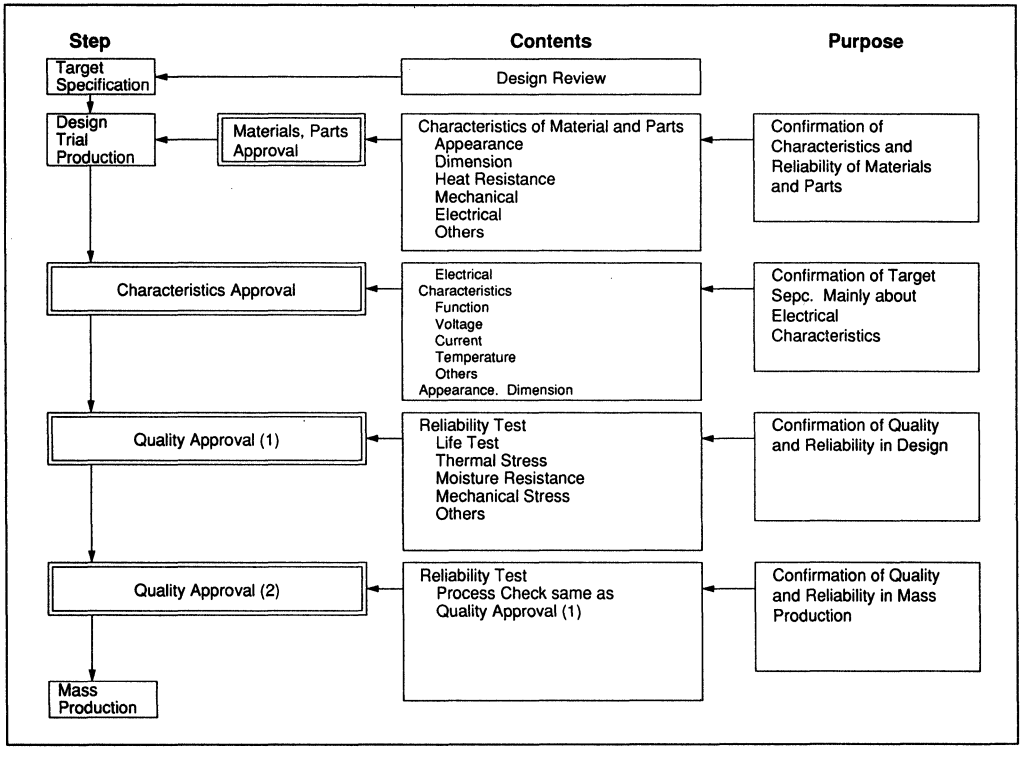


Figure 1 Flowchart of Device Design Qualification

3.3 Quality and Reliability Control in Mass Production

In mass production, quality is the functional responsibility of each department, primarily as defined by the manufacturing department and the quality assurance department. The total function flow is shown in Figure 2.

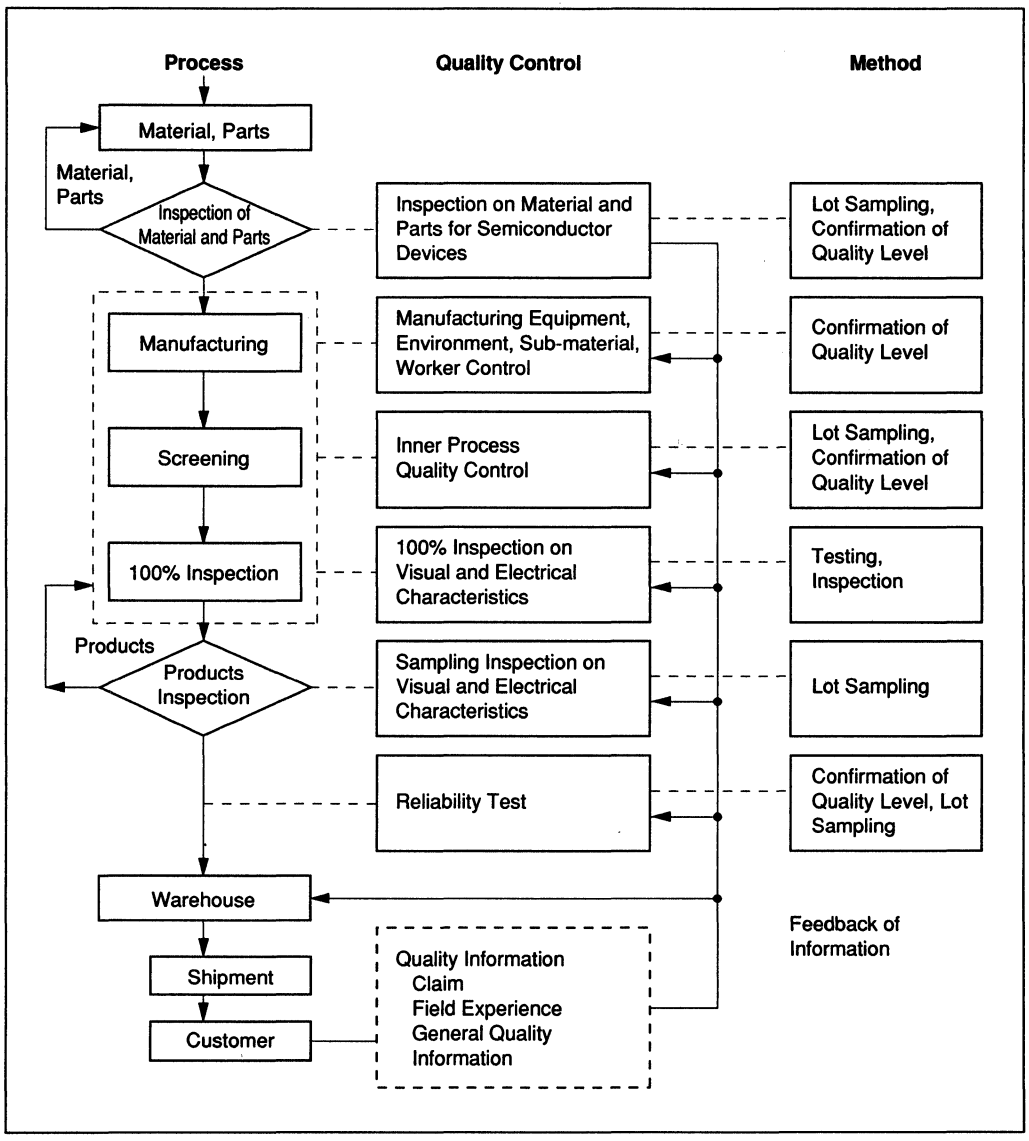


Figure 2 Flowchart of Quality Control in the Manufacturing Process

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, the quality control of parts and materials becomes more important. Items such as crystals, lead frames, fine wire for wire bonding, and packages and materials required in manufacturing processes like mask patterns and chemicals are all subject to inspection and control. Besides the qualification of parts and materials as stated in Section 3.2, the quality control of parts and materials begins at incoming inspection, which is performed based on purchase specifications, drawings and (mainly) sampling tests based on MIL-STD-105D. Other activities related to quality assurance are as follows.

1. Technology meetings with vendors.
2. Approval and guidance of vendors.
3. Analysis and test of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

Table 1 Quality Control Check Points of Parts and Materials (example)

Material parts	Important control items	Check points
Water	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratches
	Dimension	Dimension level
	Resistoration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratches, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratches
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratches
	Dimension	Dimension level
	Leakage resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechnical strength
Plastic	Composition	Characteristics of plastic material
	Electrical charactristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

3.3.2 Process Quality Control

Control of process quality is extremely significant in the overall process of device quality assurance. Quality control functions at every stage of production are described below. Figure 3 lists specific process quality control factors.

1. Quality control of products in every stage of production
   Potential device failure factors should be removed as soon as possible in the manufacturing process. To do this, check points are set up within each process to prevent products exhibiting failure factors to move onto any following process. Especially for devices designed for high reliability, manufacturing lines are rigidly monitored to control process quality. Additionally, we perform very stringent checks on some processes and/or lots, and even 100% inspections in certain critical processes to remove potentially failing items related to unavoidable manufacturing variances. Screening based on high temperature aging or temperature cycling are also part of quality assurance procedures. Controlling quality during processing includes these items:

   a. Control of conditions of equipment and workers
   b. Sampling test of uncompleted products
   c. Proposal and implementation of improvements in working conditions
   d. Continuous worker education
   e. Maintenance and improvement of yields
   f. Identification of quality problems, and implementation of countermeasures to eliminate them
   g. Communication of quality-related information

2. Quality control of manufacturing facilities and measuring equipment
   Manufacturing facilities have been developed to answer the need for higher device performance and automated production. It is also important to define and accurately measure quality and reliability.

   At Hitachi, automated manufacturing is used to reduce manufacturing variances. The operation of high performance equipment requires automated control to function properly.

   Maintenance inspections are carried out daily to ensure proper quality control, and in some instances at other more frequent intervals according to specifications, at every check point.

   The adjustment and maintenance of measuring equipment is done according to specifications and past experience, and is vigorously monitored to maintain and improve the quality of our products.

3. Quality control of the manufacturing environment and submaterial
   Final quality and reliability of devices are especially affected by manufacturing processes. We therefore thoroughly control factors of the manufacturing environment, such as gases or pure water.

   Dust control is critical to achieve higher integration and higher device reliability. To maintain and improve the cleanliness of the manufacturing site, we take great care to keep buildings, facilities, air-conditioning systems, materials, clothes, and all possible elements associated with production as clean and dust-free as we can. We extend this effort to periodically check the ambient air in the manufacturing facility for floating dust, and we check for any minute amounts which might have accumulated on the floor, other surfaces, or on any equipment.

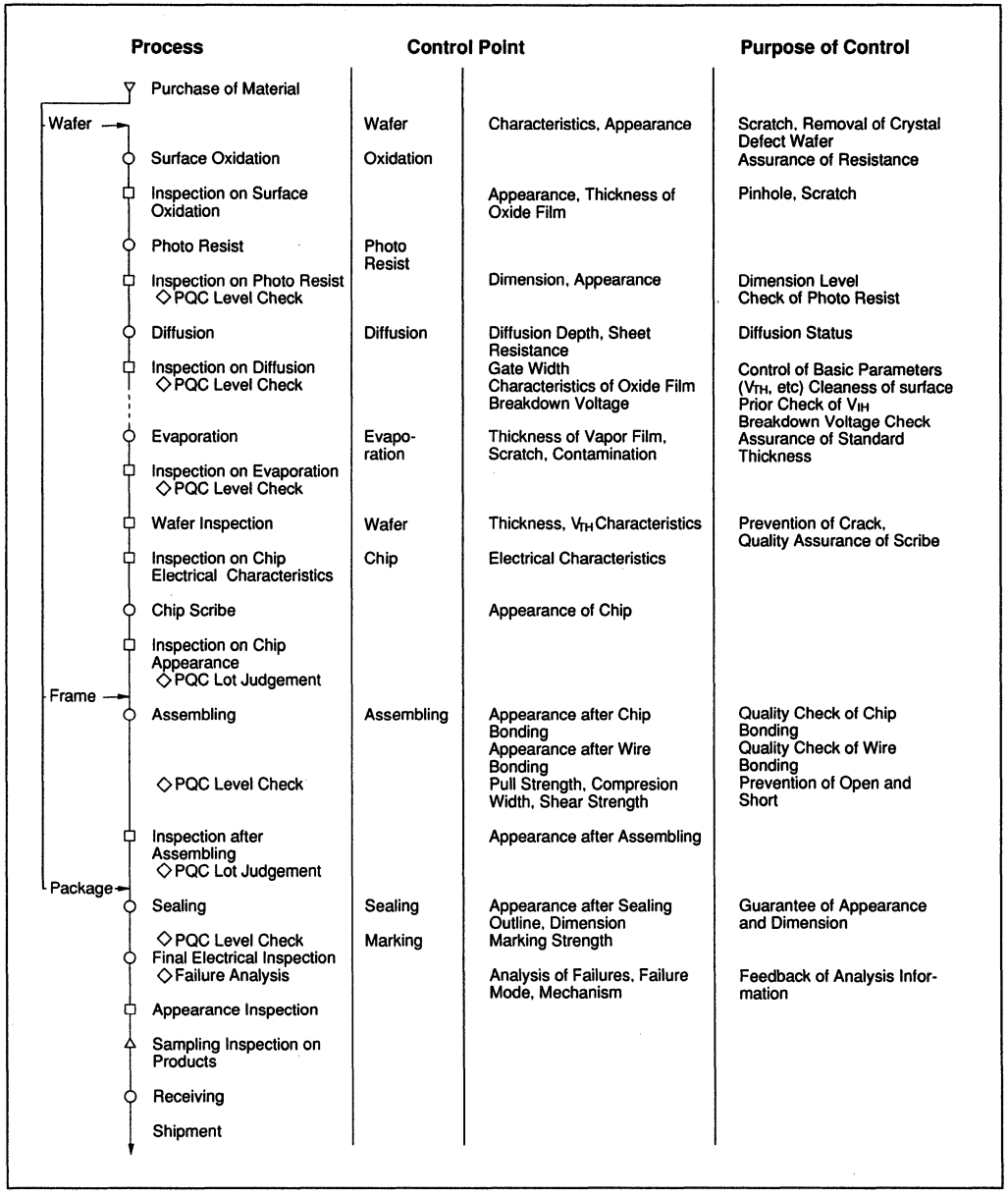


Figure 3 Example of Process Quality Control Factors

3.3.3 Final Tests and Reliability Assurance Tests

1. Final tests
   Lot inspection is done by the quality assurance department for products already passed in 100% testing during the manufacturing process. Although 100% performance is expected, sample lot inspection is also carried out to prevent any possible accidental mixture of failed products with regular, satisfactory devices.
   The extra lot inspection not only confirms that all products meet all user requirements, but considers any other potential factors. Our lot inspection is based on MIL-STD-105D.

2. Reliability assurance tests
   To assure reliability, appropriate tests are performed periodically on each manufacturing lot if the user requires such a high level of examination.

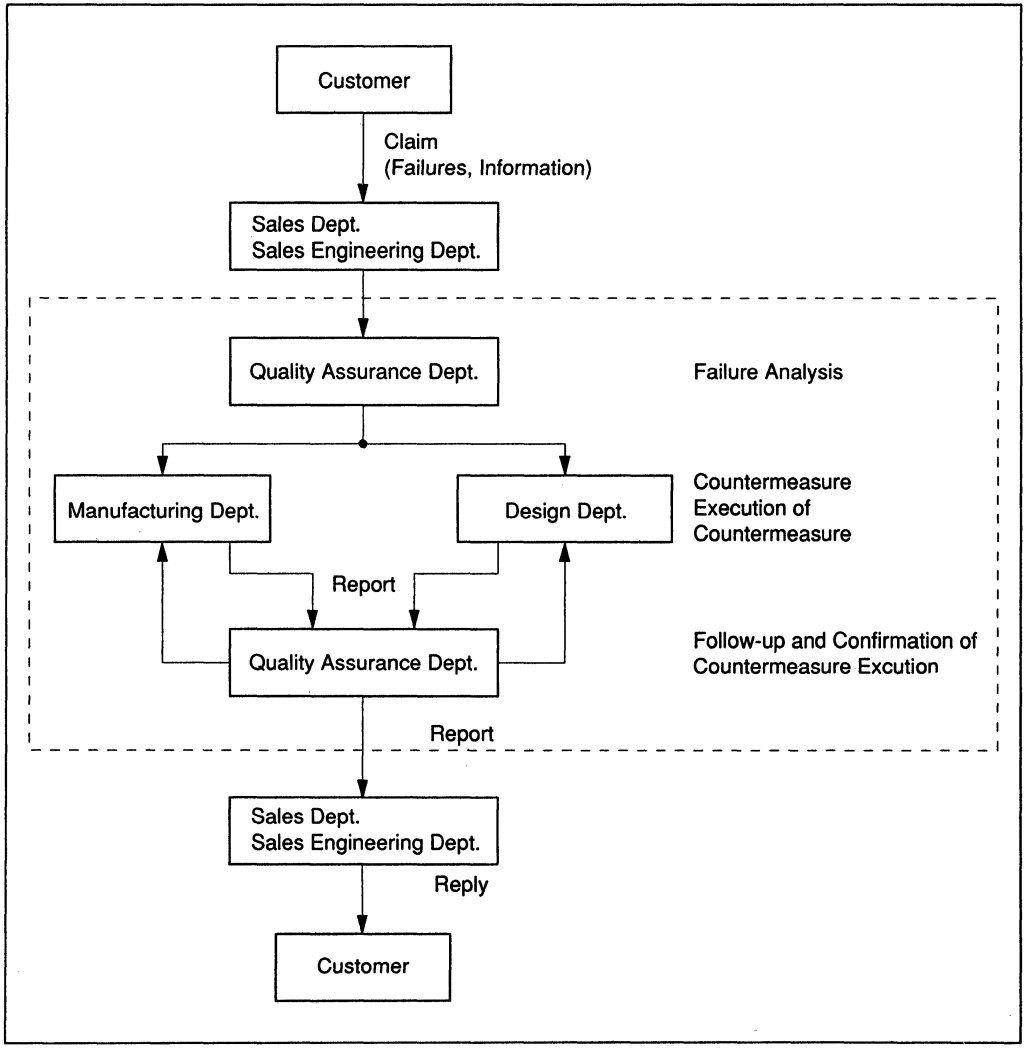


Figure 4 Process Flowchart for Customer-Reported Failure

Outline of Testing Method

1. Inspection Method

In memory IC inspection, the quality cannot be judged solely by a DC test on the external pins. The number of elements such as transistors which can be judged in a DC test is a very small part of all elements. The proposed address patterns listed below inspect whether internal circuits are functioning correctly.

1. All low, all high
2. Checker flag
3. Stripe pattern
4. Marching pattern
5. Galloping
6. Walking
7. Ping-pong

These are only a few representative samples of the testing options. There are also patterns to check the mutual interference of bits and the maximum power dissipation. Among the listing, 1 through 4 are called N patterns, which can check one sequence of N-bit IC memory with several consecutive cycles of N patterns. 5 through 7 are called N^2 patterns, which need several cycles of N^2 patterns to check one sequence of N-bit IC memory. Serious problems arise using N^2 patterns in large-capacity memory. For example, the inspection of 1-Mbit memory with the galloping pattern takes considerable time—about 120 hours. 1, 2, and 3 are rather simple and effective methods, but these patterns will not find all the failures in decoder circuits. Marching is the most simple and powerful pattern to check the functions of IC memories.

2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which 1s sequentially replace 0s throughout the device. The 1s "march" into all bits of 0. For example, a simple addressing of 16-bit memory is described below.

1. Clear all bits (see Figure 1 a).
2. Read 0 from the 0th address and check that read data is 0. Hereafter, to read means "checking and judging data."
3. Write 1 on the 0th address (see Figure 1 b).
4. Read 0 from the 1st address.
5. Write 1 on the 1st address.

   .
   .
   .
6. Read 0 from the nth address.
7. Write 1 on the nth address (see Figure 1 c).
8. Repeat 6 and 7 to the last address. Finally all data will be 1.
9. After all data has become 1, repeat from 2 through 8 replacing 0 with 1.

In this method, 5N address patterns are necessary for the N-bit memory.

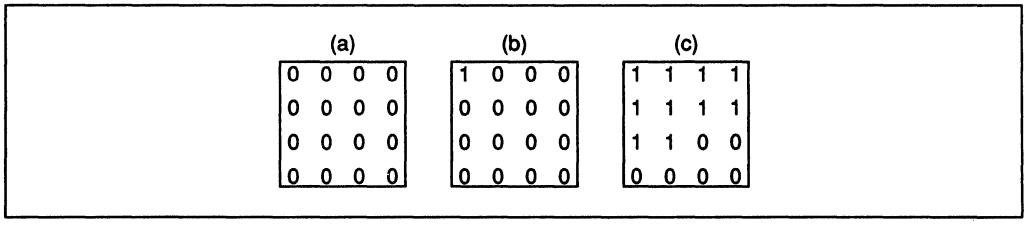


Figure 1 Addressing Method of 16-Bit Memory in the Marching Pattern

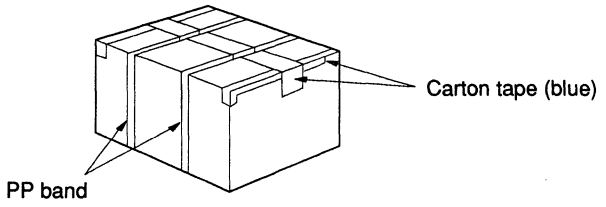
Packing Specifications

1. Forms of Package Packing

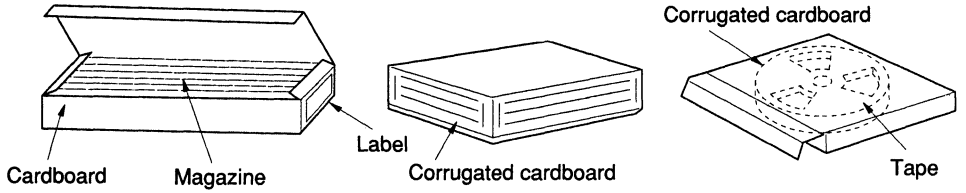
The forms of IC delivery include, as shown below, leaving the IC unsealed in a packing box and using an inside box in which there is a magazine, a tray, or tape, with the IC being housed inside. In the unsealed mode, the order of operations should be (1) corrugated cardboard packing box → (2) inside box → (3) magazine (or tray or tape).

The magazine, tray, or tape is designed so that the package is not subjected to damage during transport. When the seal is opened, the package should be handled with great care so that it is not damaged.

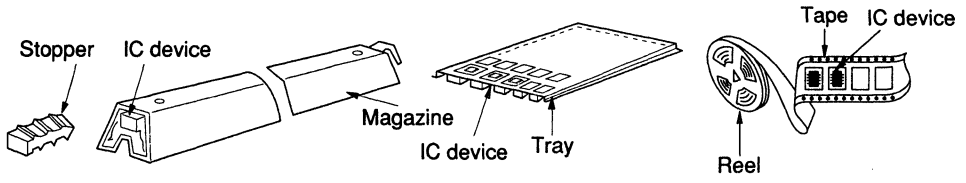
1. Cardboard packing box



2. Inside box

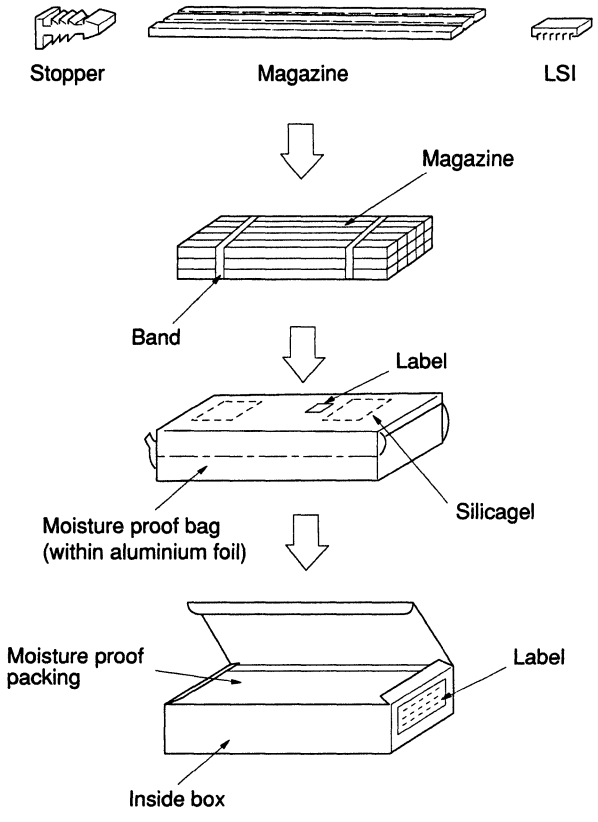


3. Magazine, tray or tape



2. Moistureproof Packing

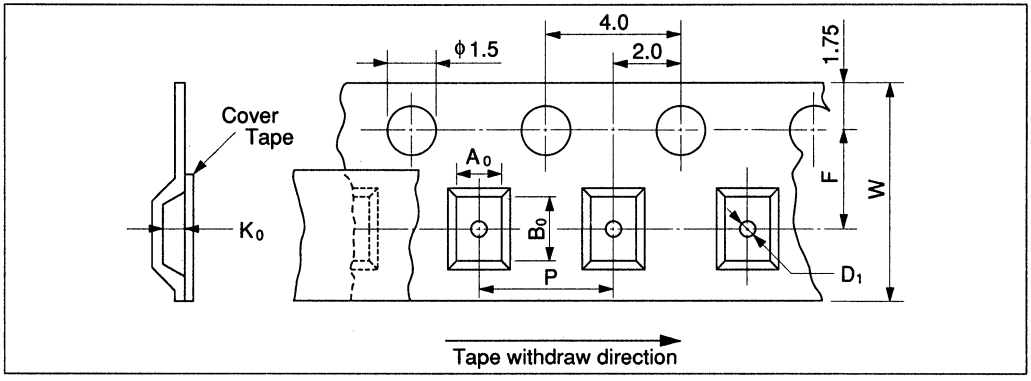
When a surface mount product is subjected to solder reflow mounting after the package has absorbed moisture, cracking of the package occurs during mounting. For this reason, moistureproof packing is carried out for plastic surface mount packages which carry large chips for the purpose of preventing moisture absorption during transport and storage. The specifications are shown below.



3. Taping for IC

Emboss tape: Tape width 16 to 24 mm

Unit: mm

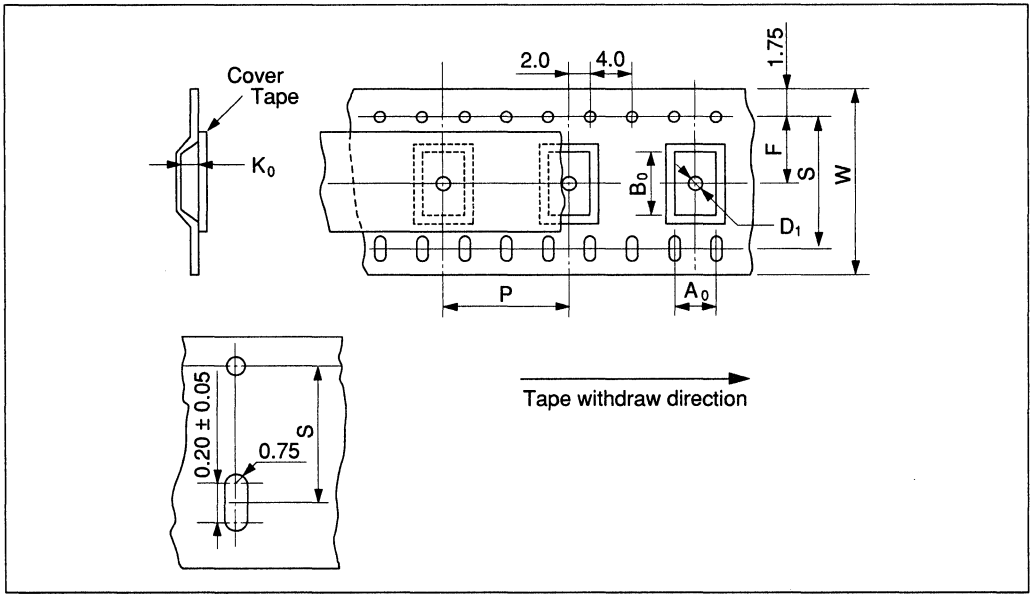


Package	Package Code	W	P	Ao	Bo	Ko	F	D_1	Maximum Storage No.
SOP	FP-24D	24	16	12.5	16.3	3.2	11.5	2	1000 IC/reel
	FP-28DA	24	16	12.4	18.5	3.1	11.5	2	1000 IC/reel
TSOP II	TTP-20DA	16	12	6.9	10.6	2 max	7.5	1.6 min	2000 IC/reel
SOJ	CP-20D	24	12	8.8	17.8	3.7	11.5	2.05	1000 IC/reel
	CP-20DA	24	12	10.35	17.7	4.3	11.5	2	1000 IC/reel
	CP-24D	24	12	8.9	16.3	4.15	11.5	2	1000 IC/reel
	CP-28DN	24	12	9.0	18.6	4.2	11.5	2	1000 IC/reel
	CP-28D, 28DA	24	16	11.6	18.65	4.2	11.5	2.05	1000 IC/reel

4. Taping for IC Memorys

Emboss tape: Tape width 32 to 44 mm

Unit: mm



Package	Package Code	W	P	Ao	Bo	Ko	F	S	D_1	Maximum Storage No.
SOP	FP-32D	32	16	14.65	21.15	3.55	14.2	28.4	2.05	1000 IC/reel
	FP-40D	44	24	14.7	26.3	3.1	20.2	40.4	2.0	750 IC/reel
	FP-44D	44	24	16.6	28.8	3.5	20.2	40.4	2.0	750 IC/reel
SOJ	CP-32D	32	16	11.45	21.5	4.05	14.2	28.4	2.05	1000 IC/reel
	CP-40D	44	16	11.7	26.75	4.2	20.2	40.4	2.05	750 IC/reel
PLCC	CP-44	32	24	17.85	17.85	4.95	14.2	28.4	2.05	500 IC/reel
	CP-52	32	24	20.55	20.5	5.35	14.2	28.4	2.05	500 IC/reel
	CP-68	44	32	26.0	25.9	4.9	20.2	40.4	2.05	250 IC/reel
	CP-84	44	36	30.9	30.8	4.9	20.2	40.4	2.05	250 IC/reel
TSOP (I)	TFP-20DA TFP-20DAR TFP-32D TFP-32DR	32	12	(8.5)	(20.4)	1.75	14.2	28.4	2.05	1000 IC/reel

4. Taping for IC Memorys (cont)

Package	Package Code	W	P	Ao	Bo	Ko	F	S	D_1	Maximum Storage No.
TSOP (II)	TTP-24D TTP-24DR TTP-28D TTP-28DR TTP-40DA TTP-40DAR TTP-44D TTP-44DA TTP-44DB TTP-44DBR	32	16	12.05	18.95	1.65	14.2	28.4	2.05	1000 IC/reel
	TTP-32D TTP-32DR TTP-32DA TTP-32DB	32	16	12.2	21.75	1.85	14.2	28.4	2.05	1000 IC/reel
	TTP-48D	32	24	(15.95)*1	(20.30)*1	1.65	14.2	28.4	2.05	1000 IC/reel

Note: 1. Subject to change without notice.

1. Static RAM

1.1 Static RAM Memory Cell

A memory cell used in Hitachi static RAM consists of 4 NMOS transistors and 2 load resistors as shown in Figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

1.2 Data Retention Mode and Battery Backup System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. This enables a battery backup system to retain the data during power failure.

Data Retention Mode: The important point in designing a battery backup system is the timing relationship between the memory power supply and the chip select signal during a change from the ordinal power source and battery power. If proper timing for the change is missed, memory data might be destroyed.

Figure 1-2 shows the timing for switching the power supply. The definitions for the technical terms related to the data retention mode are as follows.

Data retention mode: The period during which the supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS}$ = V_{DR} – 0.2 V).

t_{CDR} (time from chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (operation recovery time): The minimum time needed to change from data retention mode to operating mode.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally the minimum supply voltage needed to retain memory data is 2 V.

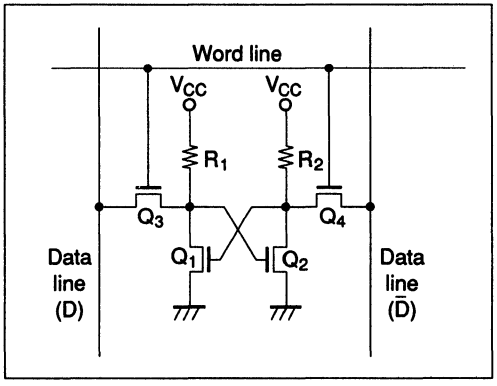


Figure 1-1 Static RAM Memory Cell

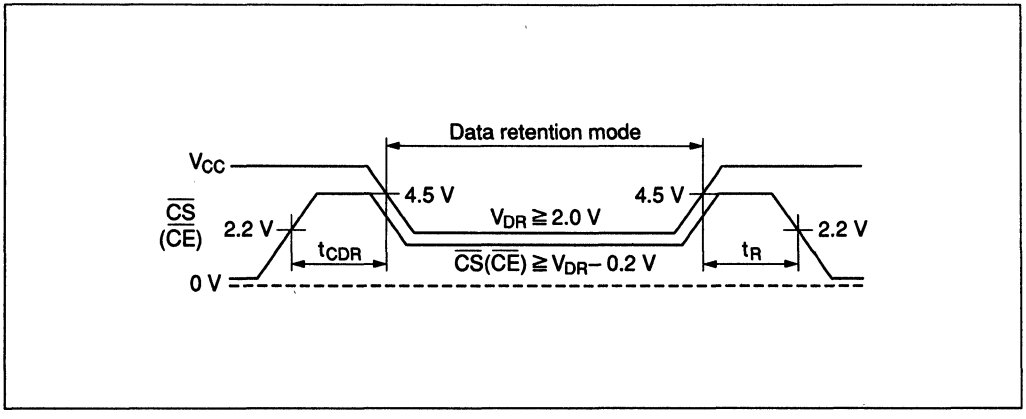


Figure 1-2 Timing for Battery Backup Application

I_{CCDR} (data retention current): The current consumption in the data retention mode depends on the memory power supply voltage and ambient temperature. It is specified as supply voltage, V_{DR} = 3.0 V.

Battery Backup System: The sequence of activities required to switch to battery backup is as follows.

1. External circuit detects a failure in the system power supply.
2. External circuit switches the RAM to standby mode.
3. External circuit separates the RAM from the system power supply.
4. External circuit switches to the backup power supply.

The control circuit detects the power failure and disconnects the power source after switching memory to the standby mode. On recovery, it confirms the power supply availability and, after some delay, returns memory to the operating mode. Memory control signals depend on the types of memory used in the system.

1. Using memory with only one $\overline{CS}$:
   The NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. Since the level of $\overline{CS}$ in the data retention mode must be higher than V_{DR} – 0.2 V, the power supply for this NAND gate must either be shared with the memory power supply or be pulled up to the memory power supply.

2. Using memory with two $\overline{CS}$:
   Basically, the signals are the same as above. In general use, two pins should be used for the control signal and the chip select signal, respectively. When the $\overline{CS}$ intercepts the current path of other pins in the input buffers, it is used as control signal input for the data retention mode.

3. Using memory with $\overline{CS}$ and CS:
   Since CS selects the chips at high level, it is preferable to use CS rather than $\overline{CS}$ as a control signal input for the data retention mode. As soon as power down is detected, the signals should be brought low. Therefore, a pull-up to the memory power supply level is not needed, thus simplifying the circuit organization.

Figure 1-4 shows an example of a battery backup system circuit. Hitachi recommends using CMOS logic for gate G1 in a control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch the regulating circuit from system power supply to backup power supply.

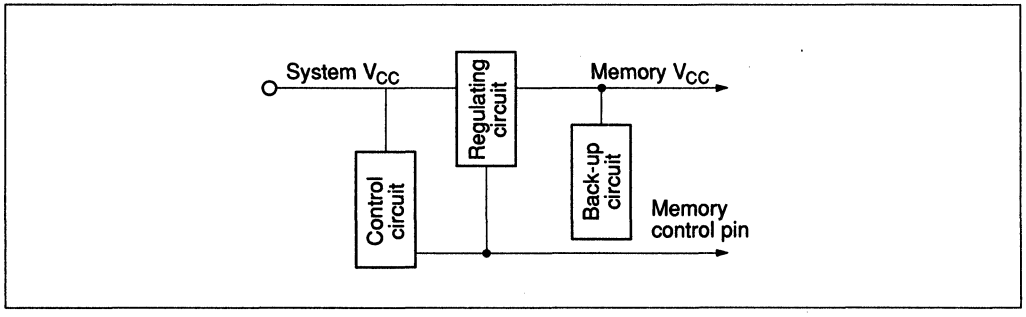


Figure 1-3 Example of Battery Backup System

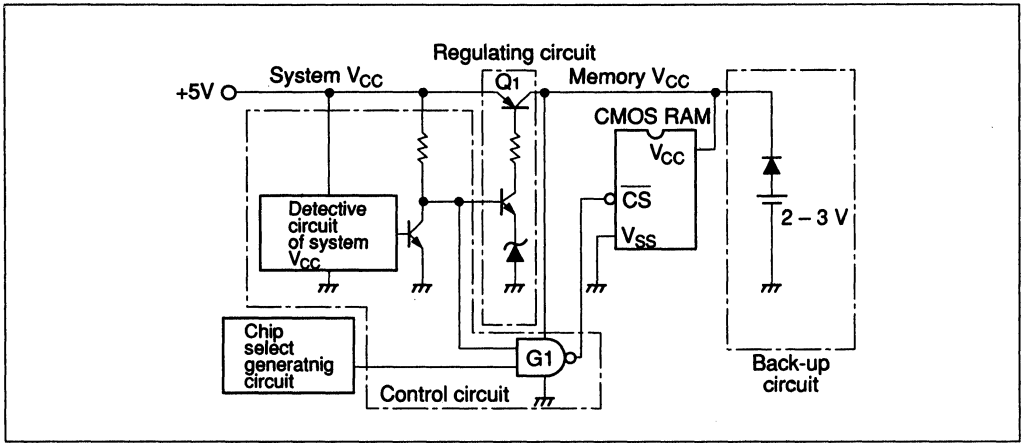


Figure 1-4 Example of a Battery Backup System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

PSRAM is a new type of IC memory designed to meet the demands for lower power consumption and lower cost.

RAMs (random access memory) are roughly classified into DRAMs (dynamic RAM) and SRAMs (static RAM). These memories vary in characteristics such as density, cost, and control method because of differences of their memory cell structures. By understanding the advantages and disadvantages of each device, a system designer can choose the best product for his application.

The advantages of DRAM are high density and low cost. These features are a result of the simple and small structure of its memory cell, which consists of one transistor and one capacitor. However, DRAM requires refresh (periodic charging) along with external control signals for refresh. In addition, the address multiplex method of decreasing the number of pins to obtain high density requires external circuits, such as an address multiplexer for generating addresses in a time-shared manner. Thus, a system timing design using DRAMs becomes complicated.

SRAM, on the other hand, does not require refresh and uses a non-address multiplex approach. Thus, SRAM can be interfaced to the MPU easily while keeping its external circuitry simple. However, SRAM requires a larger cell area and has lower density than DRAM because its memory cell is organized with 4 transistors and 2 resistors based on flip-flop circuits.

PSRAM has been developed as a new type of RAM providing the low cost per bit of DRAM and easy usage of SRAM. PSRAM offers the simple look of SRAM by providing part of the external circuits necessary with DRAM.

Table 2-1 lists the features of PSRAM, DRAM, and SRAM. PSRAM requires refresh like DRAM. One of three PSRAM refresh modes can be selected to match its system: address refresh, automatic refresh, and self refresh.

Figure 2-1 shows a comparison between systems using PSRAM and DRAM. By using PSRAM, many of the external circuits necessary for interfacing the MPU with DRAM can be eliminated.

Table 2-1 Comparison of SRAM, PSRAM, and DRAM Features

	SRAM	PSRAM	DRAM
Memory cell	4 transistors and 2 resistors	1 transistor and 1 capacitor	1 transistor and 1 capacitor
Density (same manufacturing process)	1 Mbits	4 Mbits	4 Mbits
Address	Non-address multiplex	Non-address multiplex	Address multiplex
Refresh	Not necessary	Necessary	Necessary
External circuit	Simple ◄——————————►		Complexed

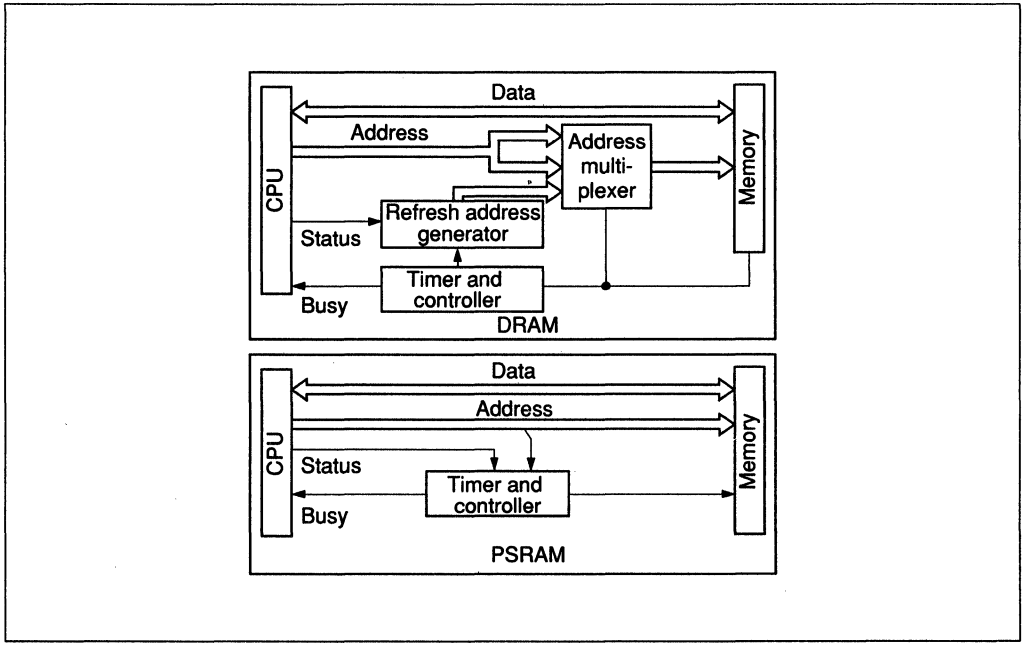


Figure 2-1 System Organization of DRAM and PSRAM

2.2 Pseudo-Static RAM Data Retention

PSRAM is useful in relatively small systems. Small systems require low current consumption since they often retain data with batteries. PSRAM with self-refresh retains data by internal refresh operation. Table 2-2 shows data retention characteristics.

Power supply voltage of data retention of PSRAM are different from that of SRAM. This is due to the use of different memory cell types. PSRAM uses an one-transistor type memory cell as used in DRAM. Refresh is internally done in order to retain data. This refresh operation is almost same operation as normal read/write, and it determines the low limit of the supply voltage. Though power supply voltage of standard PSRAM is 4.5 V – 5.5 V, some special parts retain data to 3.0 V. Please check the low limit of power supply in each data sheet.

2.3 Operation of 4M PSRAM HM658512

The operation of HM658512 is explained here for understanding of PSRAM function.

2.3.1 Read/Write Cycle

Figure 2-2 and figure 2-3 show the timing chart for the read and write cycle of the HM658512. The HM658512 can execute 2 types of accesses in the read cycle, a $\overline{CE}$ access (figure 2-2a) and an $\overline{OE}$ access (figure 2-2b). It writes data at the rising edge of $\overline{WE}$ (figure 2-3a) or at the rising edge of $\overline{CE}$ (figure 2-3b).

2.3.2 Refresh Cycle

Address refresh: This mode refreshes data by inputting row addresses 0-2047 through pins A0-A10 in sequence every 32 ms. Figure 2-4 shows the timing chart of distributed refresh.

Automatic refresh: This mode refreshes data with an internal refresh address which is generated by setting $\overline{OE}/\overline{RFSH}$ low with $\overline{CE}$ high. It is not requried to input a refresh address from address pins since it is generated internally. Figure 2-5 shows the timing chart for distributed automatic refresh.

Self refresh: This mode refreshes data automatically at fixed periods with the internal refresh timer. The self refresh mode is enabled by keeping $\overline{OE}/\overline{RFSH}$ low for more than 8 µs with $\overline{CE}$ high. This mode reduces the number of external circuits necessary for refresh since both refresh addresses and refresh request signals are generated internally. Figure 2-6 shows the timing chart for self refresh. The width of the $\overline{OE}/\overline{RFSH}$ pulse while $\overline{CE}$ is high determines whether automatic refresh or self refresh is performed. When the pulse width exceeds 8 µs, the PSRAM enters self refresh mode. Self refresh mode is useful when retaining RAM data with batteries.

Table 2-2 Data Retention of SRAM, PSRAM, and DRAM

	SRAM	PSRAM	DRAM
Density (same manufacturing process)	1 Mbits	4 Mbits	4 Mbits
Data retention voltage	2 V to 5.5 V	4.5 V to 5.5 V*1	4.5 V to 5.5 V
Current consumption (when saving data)	1 µA (typ)	70 µA (typ)*2	150 µA (typ)*2
Refresh	Not necessary	Necessary (internal control)	Necessary (external control)

Notes: 1. Some of PSRAMs retain data at 3.0 V.
2. Including refresh current. The typical values of HM658512 and HM514400A.

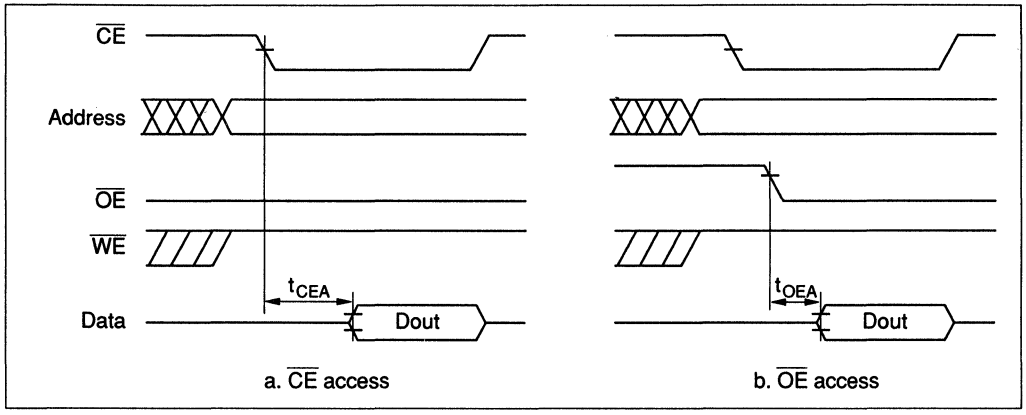


Figure 2-2 Read Cycle

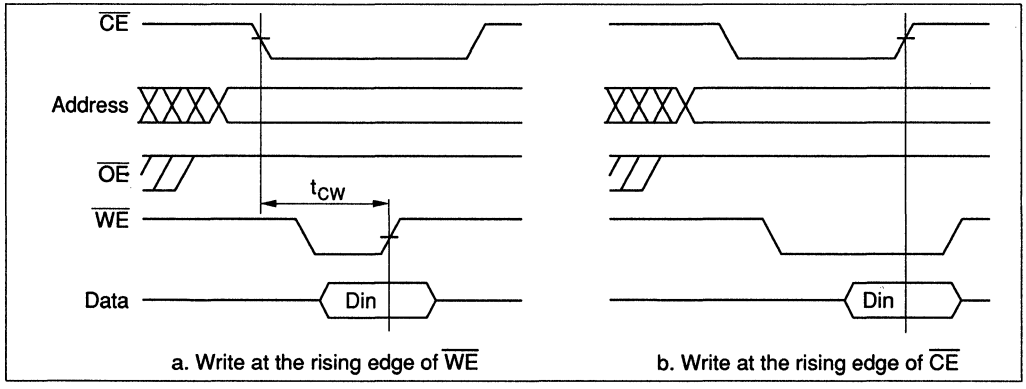


Figure 2-3 Write Cycle

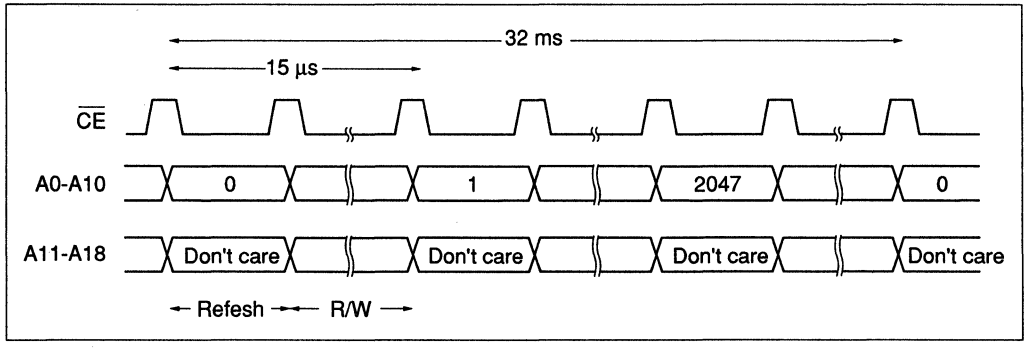


Figure 2-4 Address Refresh

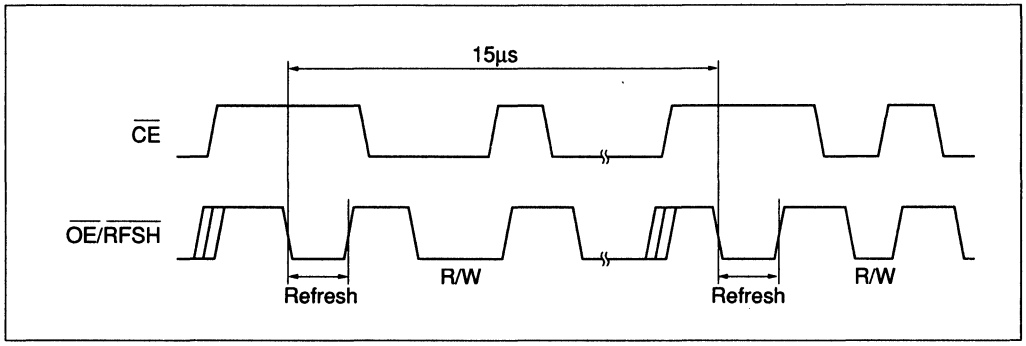


Figure 2-5 Automatic Refresh

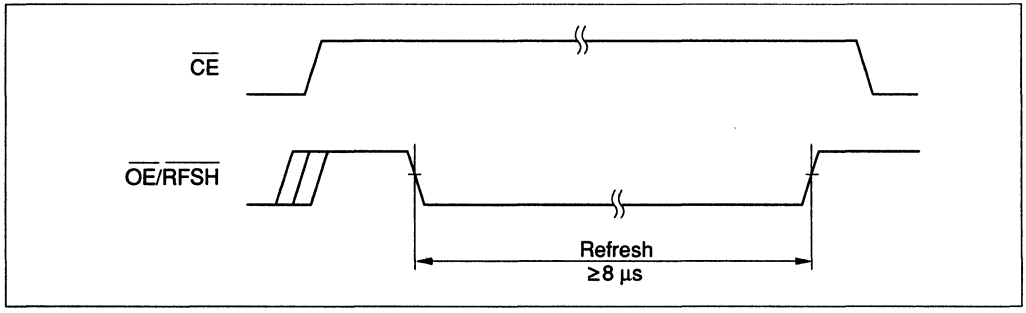


Figure 2-6 Self Refresh

2.3.3 Switching from Self Refresh Mode to Read/Write Mode

- After a self refresh is completed, the specification for t_{RFS} must be followed. t_{RFS} is defined as the time from a $\overline{OE}/\overline{RFSH}$ rising edge to the $\overline{CE}$ falling edge in the next cycle (see figure 2-7).
- When using address refresh cycles in read/write cycles, an address refresh must be started within 15 µs of completion of a self refresh, and the specified number of refresh cycles in the data sheet must be executed in succession.

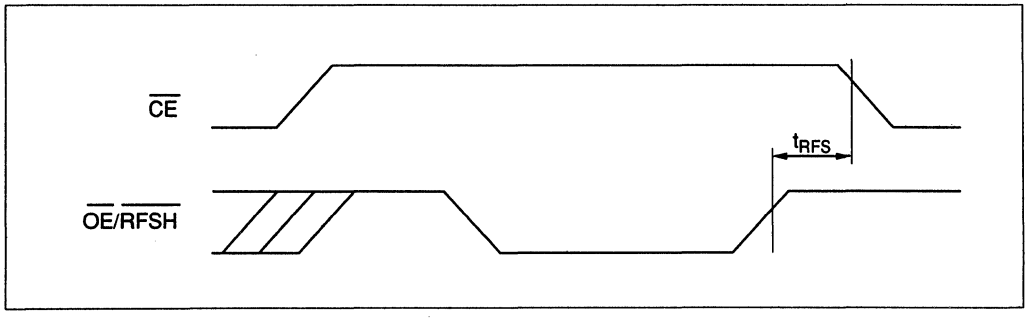


Figure 2-7 t_{RFS} (Refresh Reset Time)

- When using distributed automatic refresh cycles in read/write cycles, the first cycle of a distributed refresh must be executed within 15 µs of completion of a refresh.

- When using burst automatic refresh cycles in read/write cycles, the first cycle of automatic refresh must be started within 15 µs of completion of self refresh, and the specified number of refresh cycles in the data sheet must be executed in succession.

2.3.4 Initialization

Hitachi's PSRAM can start operation by executing eight or more initialization cycles (dummy cycles) at least 100 µs after the power voltage reaches 4.5 V – 5.5 V after power-on. An automatic refresh cycle can be used for initialization, where one automatic refresh cycle is equivalent to one initialization cycle.

2.3.5 Miscellaneous Notes

- If a short $\overline{CE}$ pulse of a width less than t_{CE} min is applied to RAM, an incomplete read occurs and stored data may be destroyed. Make sure that $\overline{CE}$ low pulses of less than t_{CE} min are inhibited. Note that a 10-ns $\overline{CE}$ low pulse may sometimes occur owing to the gate delay on the board if the $\overline{CE}$ signal is generated by the decoding of higher address signals on the board. Avoid these short pulses. One way to this $\overline{CE}$ short pulse is by gating the decoded addresses with an address strobe input.

- $\overline{OE}/\overline{RFSH}$ works as refresh control in standby mode. A short $\overline{OE}/\overline{RFSH}$ low pulse in standby mode may cause an incomplete refresh that will destroy data. Make sure that $\overline{OE}/\overline{RFSH}$ low pulse of less than t_{FAP} min are also inhibited. The definitions of t_{CE} and t_{FAP} are shown in the pages of HM658512.

- PSRAM is more sensitive to noise than normal SRAM since it executes dynamic operation internally like DRAM. It is recommended to insert one bypass condenser per RAM.

- The $\overline{OE}/\overline{RFSH}$ pin has two functions, $\overline{OE}$ for output enable and $\overline{RFSH}$ for refresh control. The specifications for parameters such as t_{OHC} and t_{OCD} must be followed to distinguish $\overline{OE}$ and $\overline{RFSH}$.

3. Instructions for Using Memory Devices

3.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled with these precautions:

1. In transporting and storing memory devices, place them in a conductive magazine or wrapper, or put all pins of each device into a conductive mat, so that they are kept at the same potential. Manufacturers should give sufficient consideration on proper packing when shipping their products.

2. When the devices are to be touched during mounting or inspection, the handler must be grounded. Do not forget to connect a resistor (1 MΩ approximately is desirable) in series for protect 10 n against electrical shock.

3. Keep the relative ambient humidity at about 50% during processing.

4. For working clothes, cotton is preferable to synthetic fabrics.

5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.

6. When transporting a board with memory devices mounted on it, enclose it with conductive materials.

7. Use conductive materials of high resistance (about 10^9 ohms) to protect the devices from electrostatic discharge. Otherwise, if accidentally put in contact with conductive materials such as a metal sheet, the devices may deteriorate or even breakdown, owing to the sudden release of charge stored on the surface.

8. Never set a system in which memory devices are used near anything that generates high voltage (e.g., a CRT anode electrode, etc.).

3.2 Using CMOS Memories

As shown in Figure 3-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 3-2 shows the relationship between the input voltage and current within the inverter. The top and bottom transistors turn on and create a current flow when the input voltage reaches an intermediate level. Therefore it is necessary to keep the input voltage below 0.2 V or above V_{CC} – 0.2 V in order to minimize power consumption. The data sheet specifies the standby current for two cases of input level (with minimum V_{IH} and maximum V_{IL}, and with 0.2 V or V_{CC} – 0.2 V), and the difference in values as being remarkably great. Some memory devices are designed to cut off such current flow in the standby mode by the control of input signals, but this depends on the

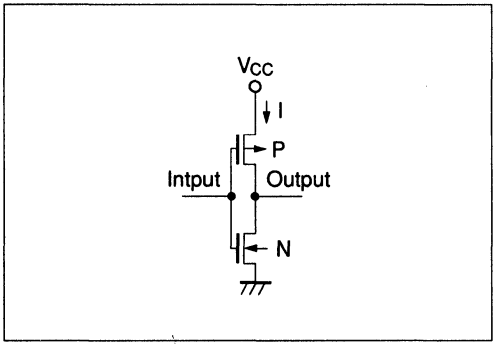


Figure 3-1 CMOS Inverter

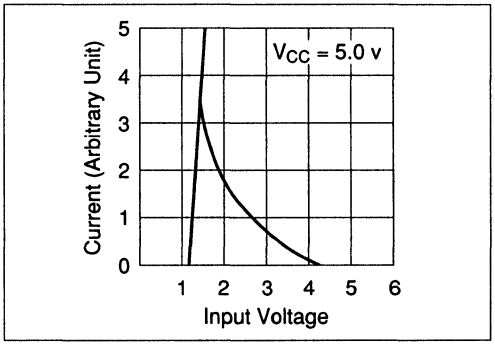


Figure 3-2 Relationship Between Input Voltage and Current in a CMOS Inverter

specific device type. This should be confirmed in data sheets for each device type.

Another problem peculiar to CMOS devices is latch up. Figure 3-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in Figure 3-4. When positive DC current or pulse noise is applied (Figure 3-4a), T_{R3} is turned on owing to the bias voltage generated between the base and emitter. Also, trigger current flows to ground through R_P, the base resistance of T_{R2}. As a result, T_{R2} becomes conductive and the current flows from power supply (V_{CC}) through the base resistance of T_{R1} (R_N), which also puts T_{R1} into conduction. Then as the base of T_{R2} is rebiased by the collector current from T_{R1}, the closed loop consisting of T_{R1} and T_{R2} reacts. Thus, current flows constantly between the power supply (V_{CC}) and ground even without the trigger current caused by outside noise.

Latch up can also be caused by a negative pulse (Figure 3-4 b). Most semiconductor memory

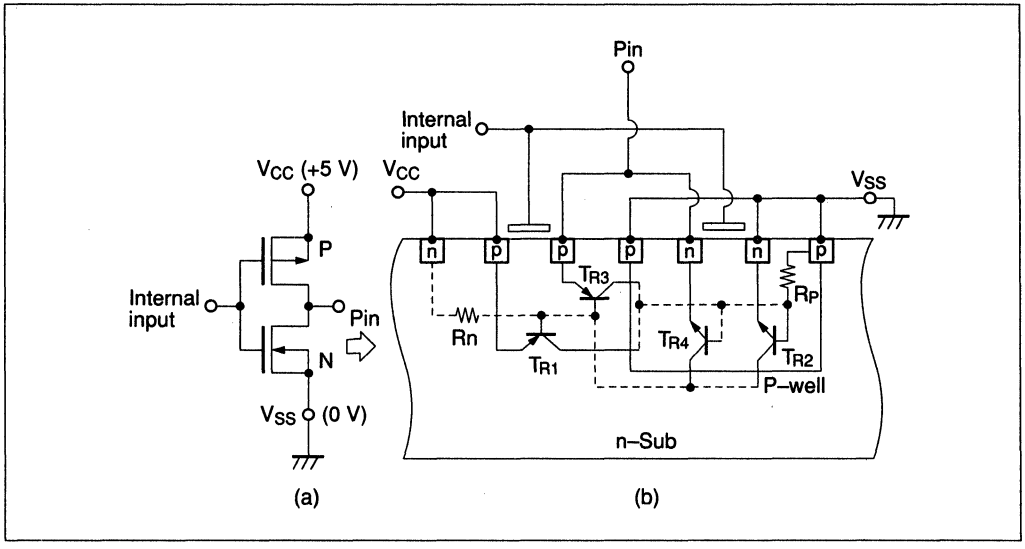


Figure 3-3 Cross Section Structure of CMOS Inverter

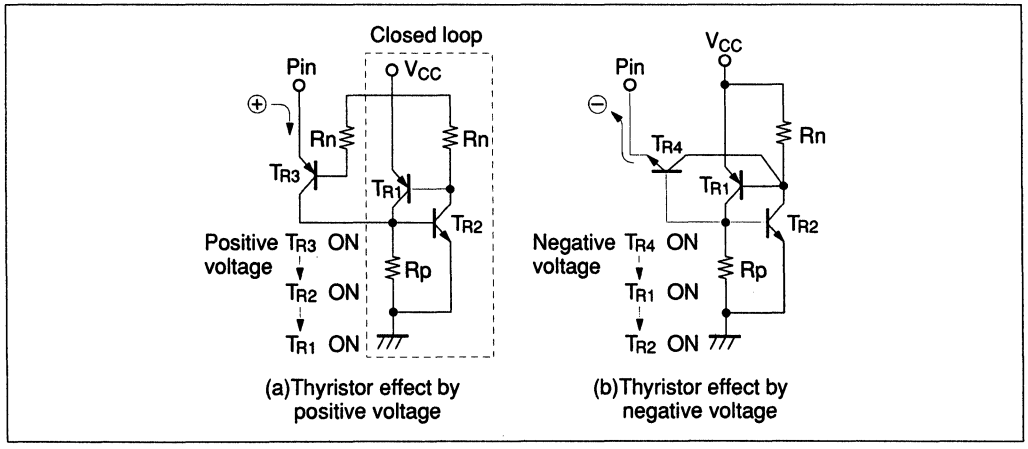


Figure 3-4 Equivalent Circuit of Parasitic Thyristor

manufacturers are trying to improve latch up immunity in their products. Hitachi provides a broad enough guard band by applying a diffusion layer around the inputs and outputs, taking care not to connect the input to the p^+ diffusion layer. The input voltage for the 64-kbit static RAM HM62256, for example, is specified as follows:

V_{IH} max 6.0 V (not dependent on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
–0.5 V (DC level)

Thus almost no consideration for latch up is required in system designs using these devices.

3.3 Noise Prevention

Noise in semiconductor memories is roughly classified as input signal noise and power supply noise.

Input Signal Noise: Input signal noise is caused by overshoot and undershoot. If either of them exceeds the recommended DC operating conditions, normal operation is hindered, and a voltage over the absolute maximum rating will break the device. When operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohms into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because the noise is often caused by an unstable reference voltage (ground level).

Power Supply Noise: Power supply noise can be classed as low-frequency and high-frequency as shown in Figure 3-5. To assure a stable memory operation, combined low- and high-frequency noise should be held below 10 percent of the standard level of the peak-to-peak power supply voltage.

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during the transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, the voltage drops. And if the

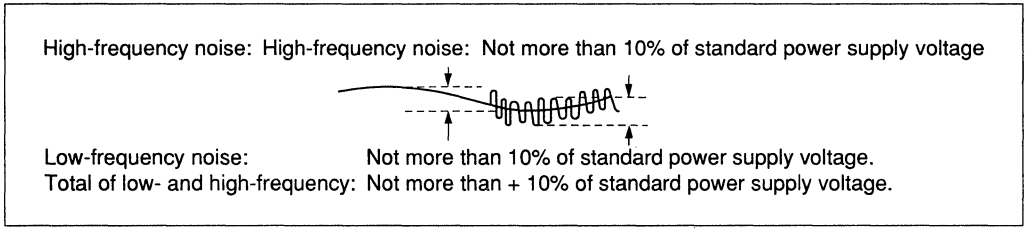


Figure 3-5 Power Supply Noise

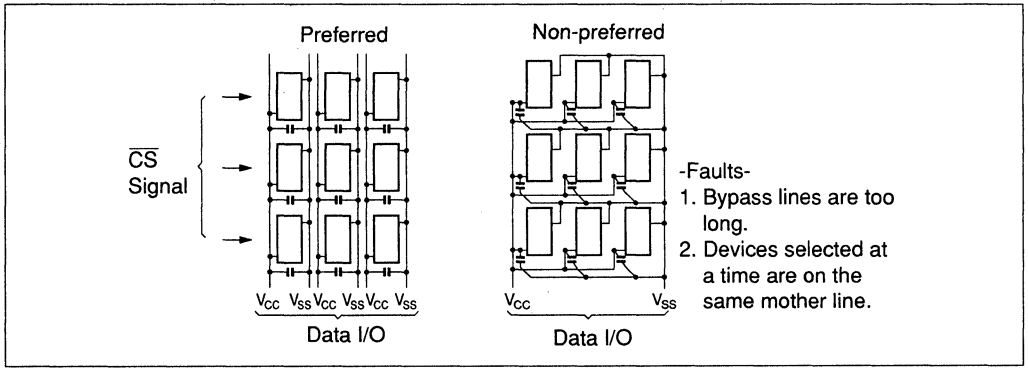


Figure 3-6 Examples of a Power Supply Board Pattern

recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1–0.01 µF should be inserted near the device. The following points must be considered in designing the layout of a board:

1. For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.

2. Bypass capacitors must be applied to the power supply pins of memory devices as near as possible, and inductance in the path from the V_{CC} pin to V_{SS} pin through the bypass capacitor must be kept as low as possible.

3. The line connected to the power supply on the board should be as wide as possible.

4. It is preferable for the power supply line to be at right angles to devices selected at the same time, otherwise too much peak current will flow through one power supply line at a time.

3.4 Address Input Waveform of Hi-BiCMOS Memory

Data stored in memory might be destroyed in a case where the address input of a HM6716, HM6719, HM6787, HM6788, or HM6789 series device floats and sticks near threshold voltage (e.g., CPU sets the address bus to off state in Figure 3-7). Consequently, the following three methods are recommended to prevent malfunctions of a Hi-BiCMOS memory device.

A: Insert the latch as shown in Figure 3-7 to keep the address input from floating.
B: Set $\overline{CS}$ high while the address input floats.
C: Insert a pull-up resistor (R) to hold the time constant of the rising edge waveform on the address input pin ($t_r = R \times C$) below 150 ns.

Stable operation can be assured if the above three methods (A, B, C) have been adopted. Should any further problems arise, please contact one of our sales offices.

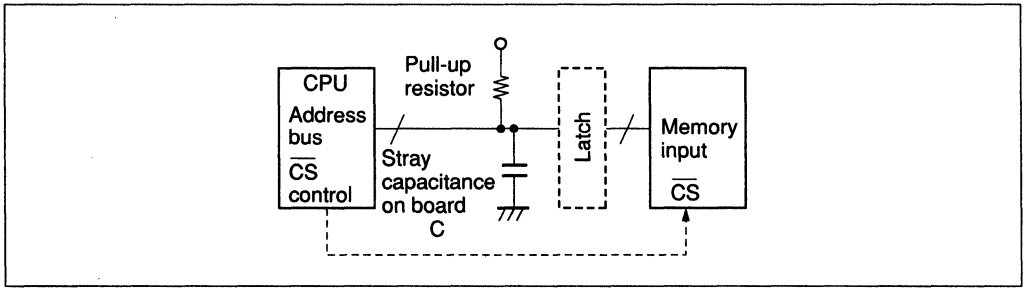


Figure 3-7

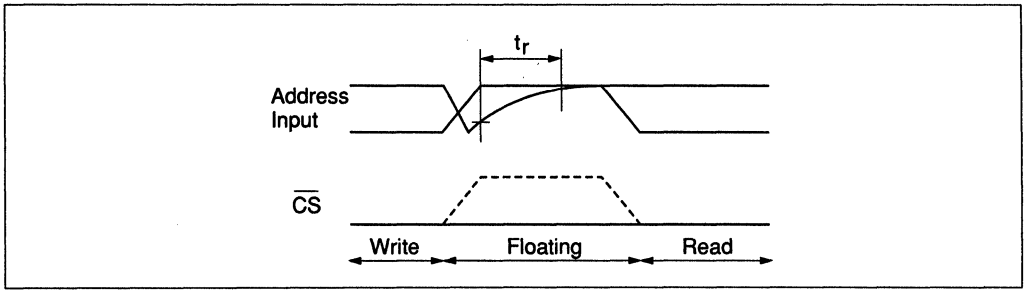


Figure 3-8

SECTION 2

BiCMOS FAST STATIC RAMs

- TTL I/O
- ECL I/O

HM6708SH/HM6709SH Series — TTL I/O

65,536-words × 4-bits High Speed Static Random Access Memory

Features

- 65,536 words × 4 bits organization
- Fully compatible with TTL input and output
- 0.8 µm Hi-BiCMOS process
- +5 V single power supply
- Completely static memory: No clock or timing strobe required
- Low power dissipation (DC) operating: 400 mW typ
- Super fast access time: 10/12 ns max

Ordering Information

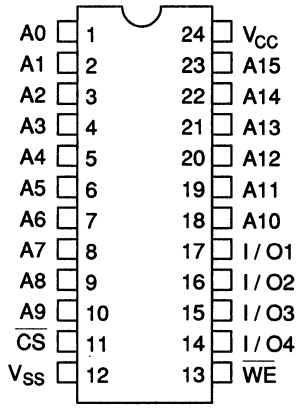
Type No.	Access time	Package
HM6708SHJP-10	10 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6708SHJP-12	12 ns	
HM6709SHJP-10	10 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM6709SHJP-12	12 ns	

Pin Description

Pin name	Function
A0–A15	Address input
I/O1–I/O4	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$ (for HM6709SH only)	Output enable
V_{SS}	Ground
V_{CC}	Power supply
NC	No connection

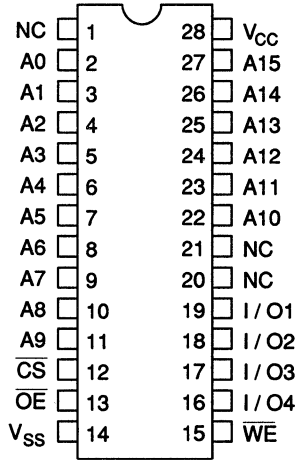
Pin Arrangement

HM6708SH Series



(Top View)

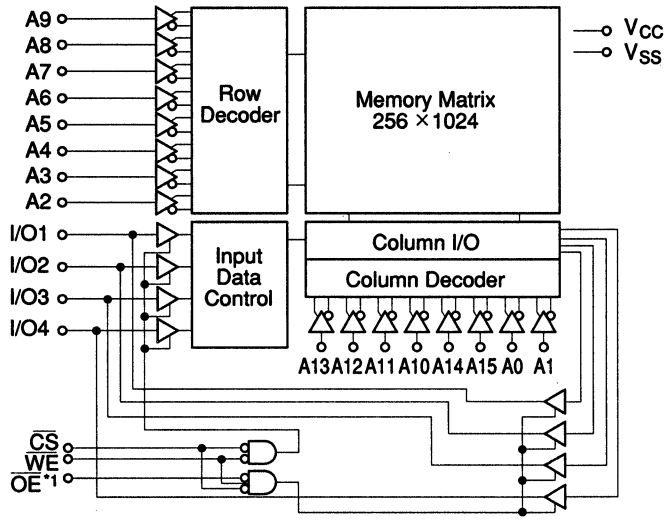
HM6709SH Series



(Top View)

2

Block Diagram



Note: 1. HM6709SH only

Function Table (HM6708SH)

Input

$\overline{CS}$	$\overline{WE}$	Mode	I/O pin	V_{CC} current	Reference cycle
H	X	Not selected	High Z	I_{SB}, I_{SB1}	—
L	H	Read	Data out	I_{CC}, I_{CC1}	Read cycle (2), (3)
L	L	Write	Data in	I_{CC}, I_{CC1}	Write cycle (1), (2)

Function Table (HM6709SH)

Input						
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	V_{CC} current	Reference cycle
H	X	X	Not selected	High Z	I_{SB}, I_{SB1}	—
L	H	H	Output disable	High Z	I_{CC}, I_{CC1}	—
L	H	L	Read	Data out	I_{CC}, I_{CC1}	Read cycle (1), (2), (3)
L	L	H	Write	Data in	I_{CC}, I_{CC1}	Write cycle (1), (2), (3), (4)
L	L	L	Write	Data in	I_{CC}, I_{CC1}	Write cycle (5), (6)

2

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage with respect to V_{SS} pin	V_{CC}	–0.5 to +7.0	V
Terminal voltage with respect to V_{SS} pin	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

For the AC and DC specifications shown in these tables, the devices were tested with a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (0°C≤ Ta ≤ 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: 1. Pulse width 10 ns, DC: –0.5 V

DC Characteristics (V_{CC} = 5.0 V ± 10%, Ta = 0 to +70°C)

		HM6708SH/HM6709SH							
		-10			-12				
Parameter	**Symbol**	**Min**	**Typ*1**	**Max**	**Min**	**Typ*1**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	—	2	—	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$=V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CC}
Operating power supply current	I_{CC}	—	60	100	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	130	180	—	120	175	mA	Min. cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	40	—	—	40	mA	$\overline{CS}$ =V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	—	—	30	—	—	30	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Note: 1. Typical limits are: V_{CC} = 5.0 V, Ta = 25°C, and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

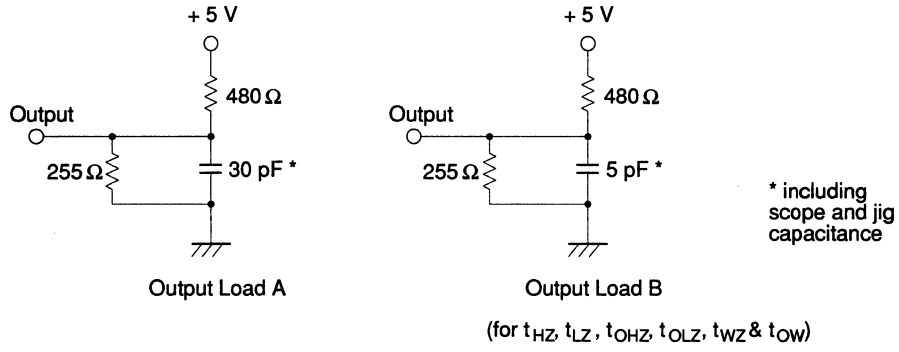
Parameter	**Symbol**	**Max**	**Unit**	**Test condition**
Input capacitance	C_{in}*1	6	pF	Vin = 0 V
Output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and is not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0°C to +70°C unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



Read Cycle

		HM6708SH/HM6709SH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Chip selection to output in low Z	t_{LZ}*1, *2	3	—	3	—	ns
Output enable to output valid	t_{OE}*3	—	5	—	6	ns

Read Cycle (cont)

		HM6708SH/HM6709SH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Output enable to output in low Z	t_{OLZ}*1, *2, *3	0	—	0	—	ns
Chip deselection to output in high Z	t_{HZ}*1, *2	0	5	0	5	ns
Output hold from address change	t_{OH}	3	—	3	—	ns

Notes: 1. This parameter is sampled and is not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).
3. These parameters are for HM6709SH.

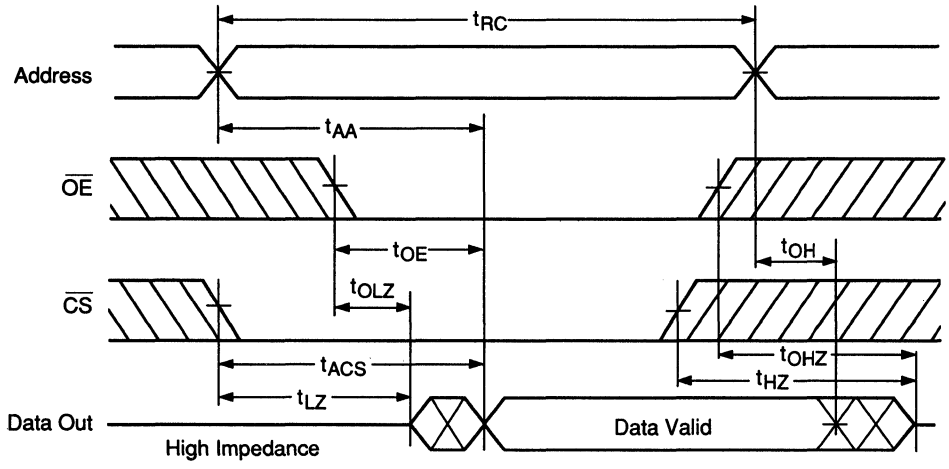
Write Cycle

		HM6708SH/HM6709SH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}*1	10	—	12	—	ns
Chip selection to end of write	t_{CW}	8	—	9	—	ns
Address valid to end of write	t_{AW}	10	—	11	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	8	—	9	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	6	—	6	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enable to output in high Z	t_{WZ}*2, *3	0	5	0	6	ns
Output disable to output in high Z	t_{OHZ}*2, *3, *4	0	6	0	6	ns
Output active from end of write	t_{OW}*2, *3	3	—	3	—	ns

Notes: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and is not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with loading specified in Load (B).
4. These parameters are for HM6709SH.

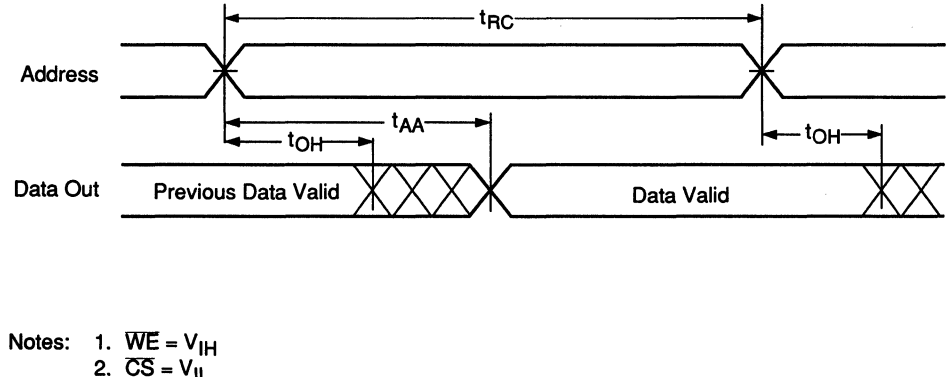
Timing Waveforms

Read Cycle 1



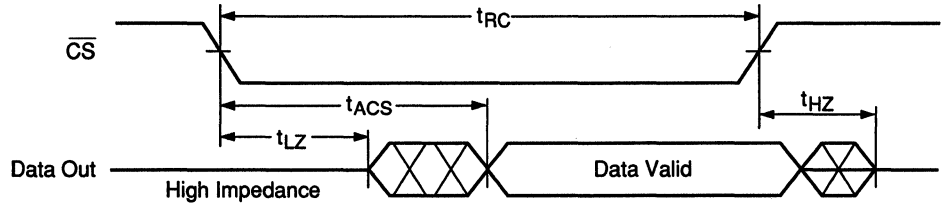
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle 2



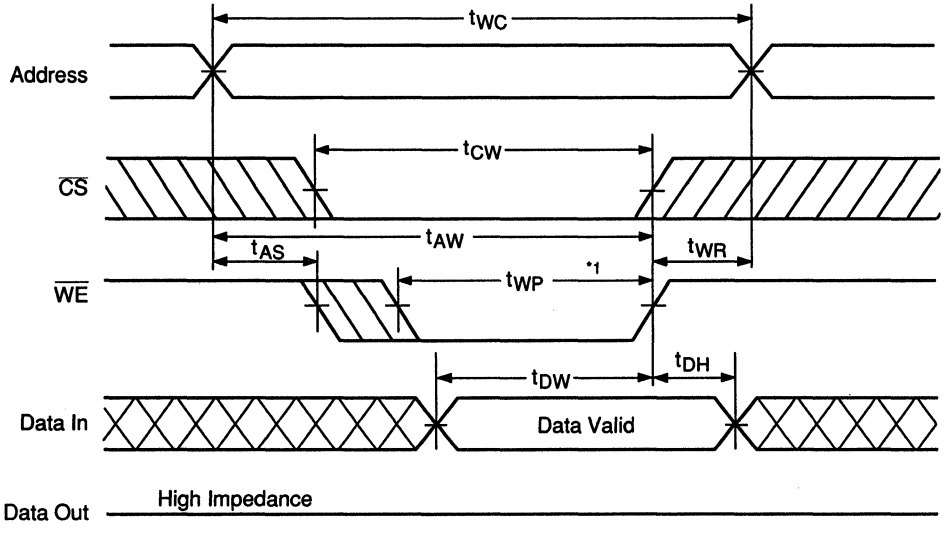
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle 3



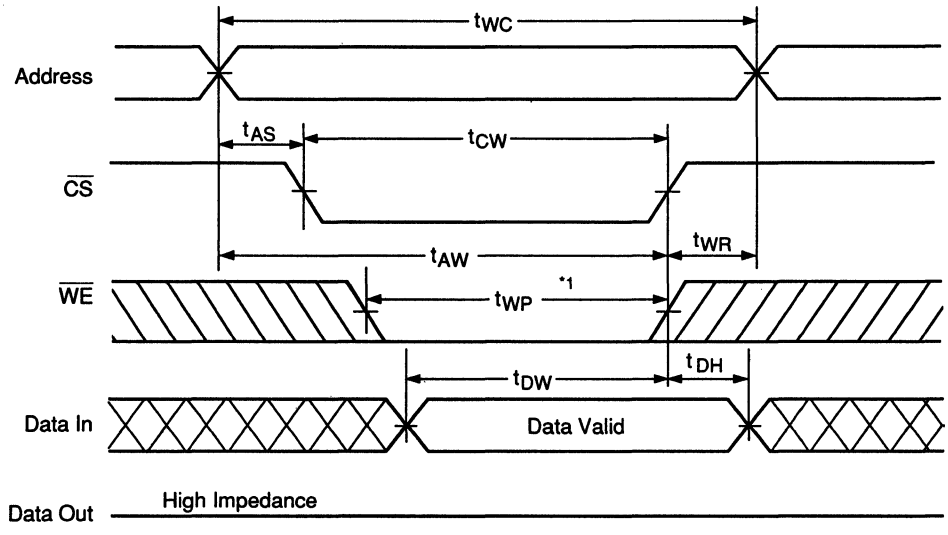
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE}$ = H, $\overline{WE}$ controlled)



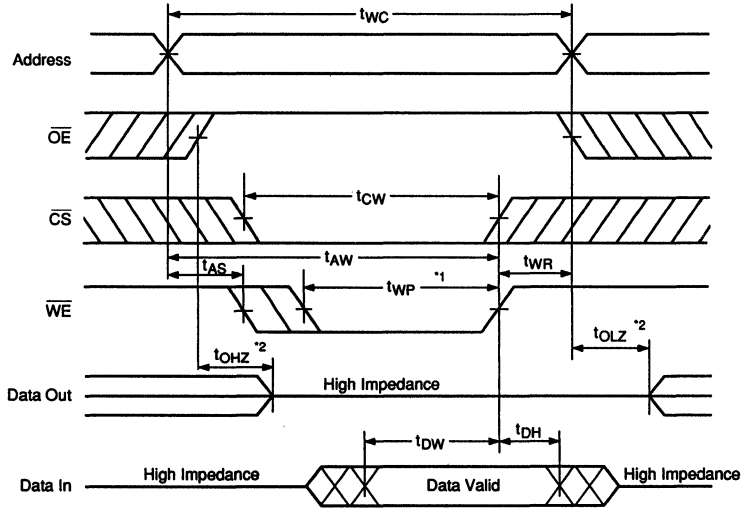
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE}$ = H, $\overline{CS}$ controlled)



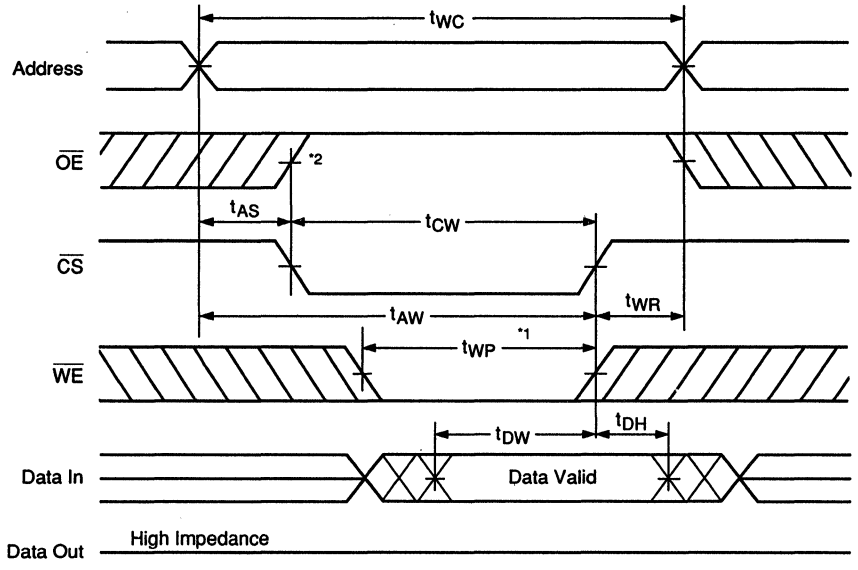
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



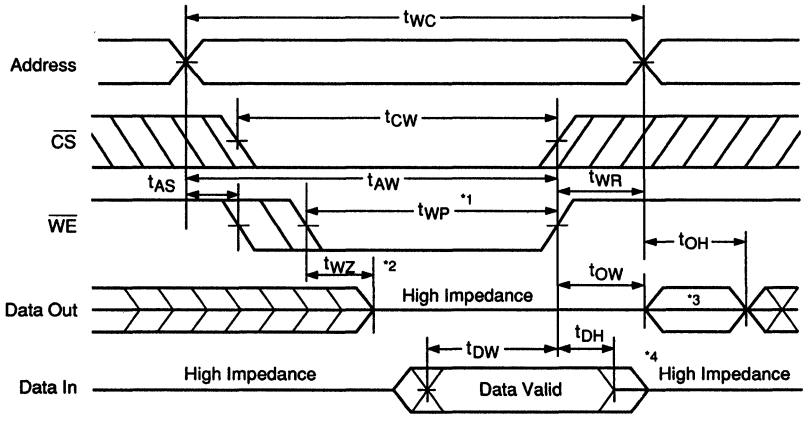
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



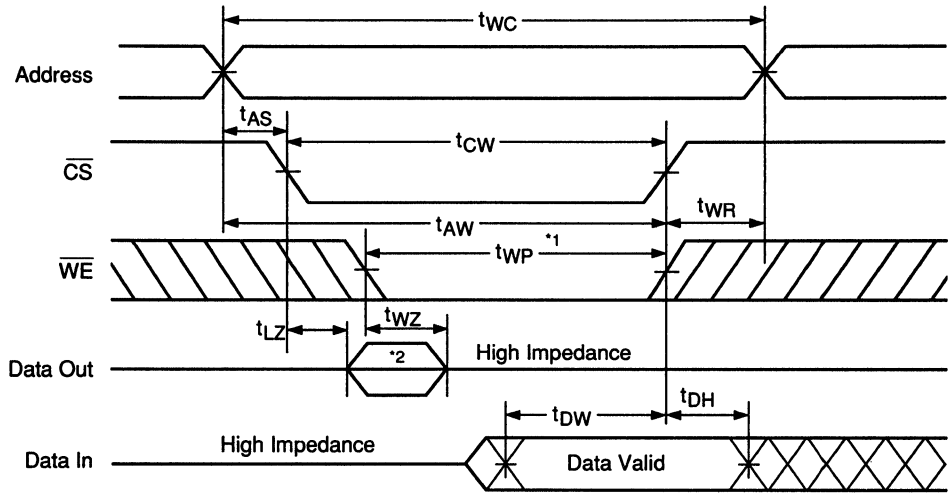
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle 6 ($\overline{OE}$ = L, $\overline{CS}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM67832SH Series

32,768-word × 8-bit High Speed Static Random Access Memory

Features

- 32,768 words × 8 bits organization
- Directly TTL compatible input and output
- 0.8 µm Hi-BiCMOS process
- +5 V single power supply
- Completely static memory: No clock or timing strobe required
- Low power dissipation (DC)
  operating: 400 mW typ
- Super fast access time: 10/12 ns (max)

Ordering Information

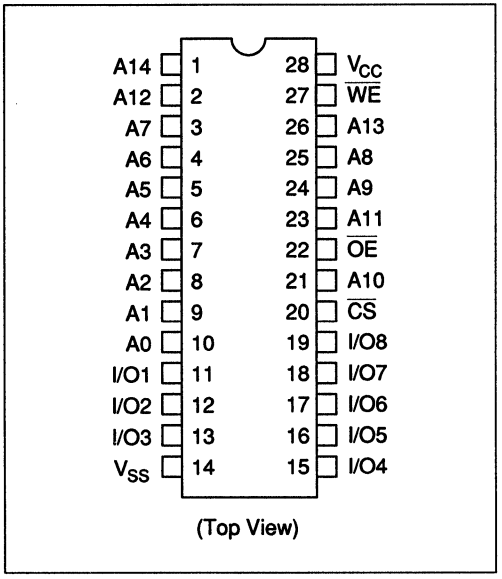
Type No.	Access time	Package
HM67832SHJP-10*	10 ns	300 mil 28 pin plastic SOJ (CP-28DN)
HM67832SHJP-12*	12 ns	

*Organization: 32k × 8

Pin Description

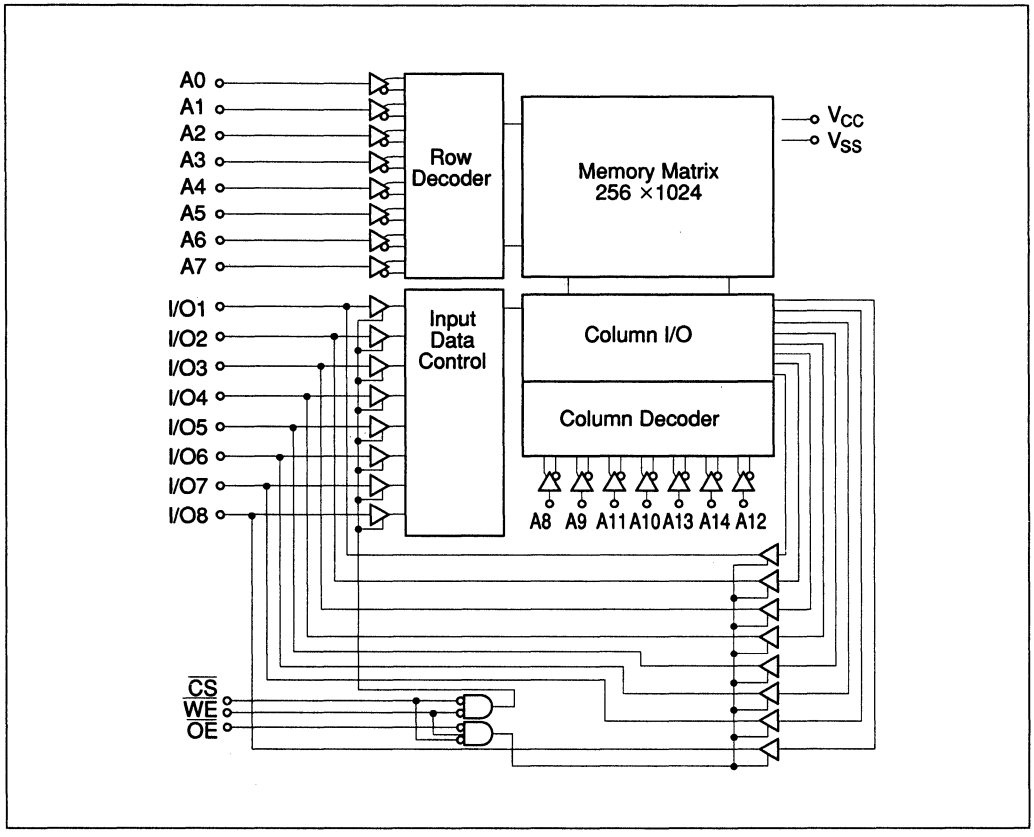
Pin name	Function
A0–A14	Address input
I/O1–I/O8	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{SS}	Ground
V_{CC}	Power supply

Pin Arrangement



(Top View)

Block Diagram



Function Table

Input						
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Output	Mode	V_{CC} current	Reference cycle
H	X	X	High Z	Not selected	I_{SB}, I_{SB1}	—
L	H	H	High Z	Output disable	I_{CC1}	—
L	H	L	Data out	Read	I_{CC1}	Read cycle 1, 2, 3
L	L	H	Data in	Write	I_{CC1}	Write cycle 1, 2, 3, 4
L	L	L	Data in	Write	I_{CC1}	Write cycle 5, 6

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage with respect to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin with respect to V_{SS}	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range (with bias)	T_{stg}(bias)	–10 to +85	°C
Storage temperature range	T_{stg}	–55 to +125	°C

For the DC and AC specifications shown in these tables, this device was tested under a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: 1. Pulse width 10 ns, DC: –0.5 V

DC Characteristics (V_{CC} = 5.0 V ± 10%, Ta = 0 to +70°C)

		HM67832SH							
		-10			-12				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	—	2	—	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CC}
Average operating current	I_{CC1}	—	150	200	—	140	195	mA	Min. cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	40	—	—	40	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	—	—	30	—	—	30	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Note: 1. Typical limits are at V_{CC} = 5.0 V, Ta = 25°C, and specified loading.

Capacitance (Ta =25°C, f=1 MHz)

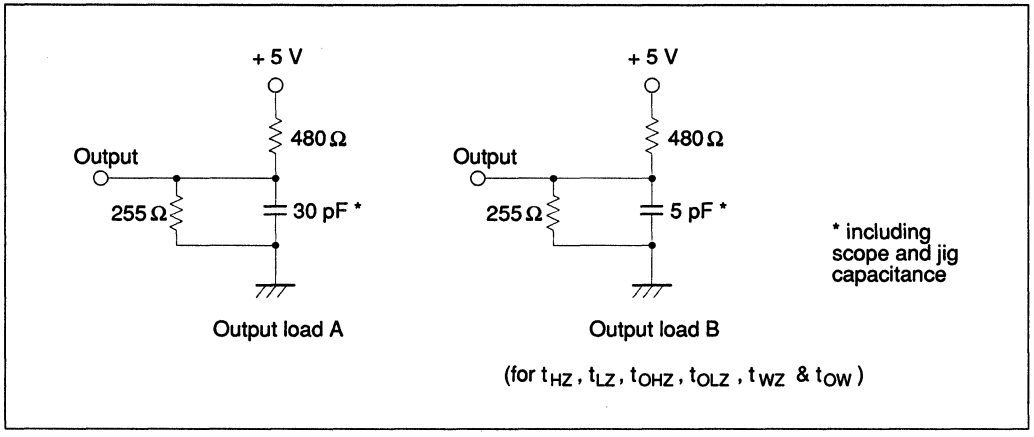
Parameter	**Symbol**	**Max**	**Unit**	**Test condition**
Input capacitance	Cin*1	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and has not been 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C, unless otherwise noted)

Test conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure
- Input rise and fall time: 4 ns
- Output reference level: 1.5 V



Read Cycle

		HM67832SH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Chip selection to output low Z	t_{LZ}*1, *2	3	—	3	—	ns
Output enable to output valid	t_{OE}	—	5	—	6	ns
Output enable to output low Z	t_{OLZ}*1, *2	0	—	0	—	ns
Chip deselection to output high Z	t_{HZ}*1, *2	0	5	0	5	ns
Output hold from address change	t_{OH}	3	—	3	—	ns

Notes: 1. This parameter is sampled and has not been 100% tested.
2. Transition is measured ±200 mV from steady state voltage with loading specified in Load (B).

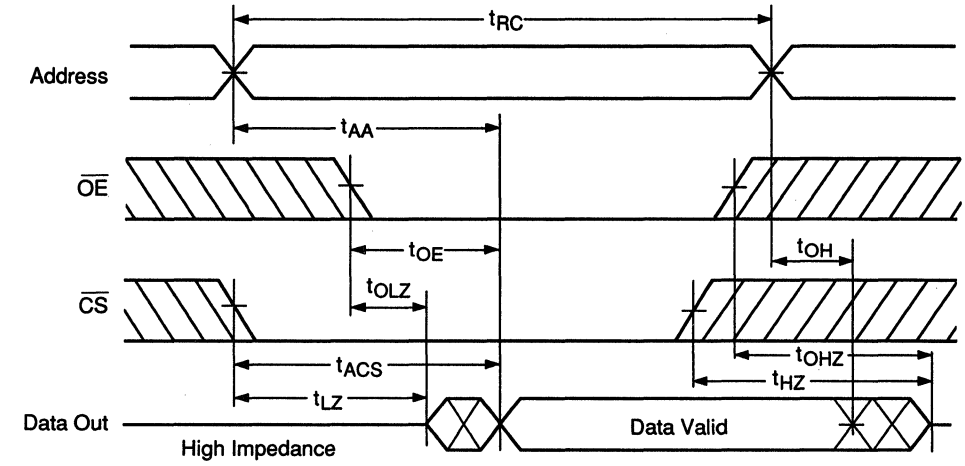
Write Cycle

		HM67832SH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}*1	10	–	12	–	ns
Chip selection to end of write	t_{CW}	8	–	9	–	ns
Address valid to end of write	t_{AW}	10	–	11	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	8	–	9	–	ns
Write recovery time	t_{WR}	0	–	0	–	ns
Data valid to end of write	t_{DW}	6	–	6	–	ns
Data hold time	t_{DH}	0	–	0	–	ns
Write enable to output high Z	t_{WZ}*2, *3	0	5	0	6	ns
Output disable to output high Z	t_{OHZ}*2, *3	0	6	0	6	ns
Output active from end of write	t_{OW}*2, *3	3	–	3	–	ns

Notes: 1. All write cycle timings are referenced from the last valid address to the first changing address.
2. This parameter is sampled and has not been 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

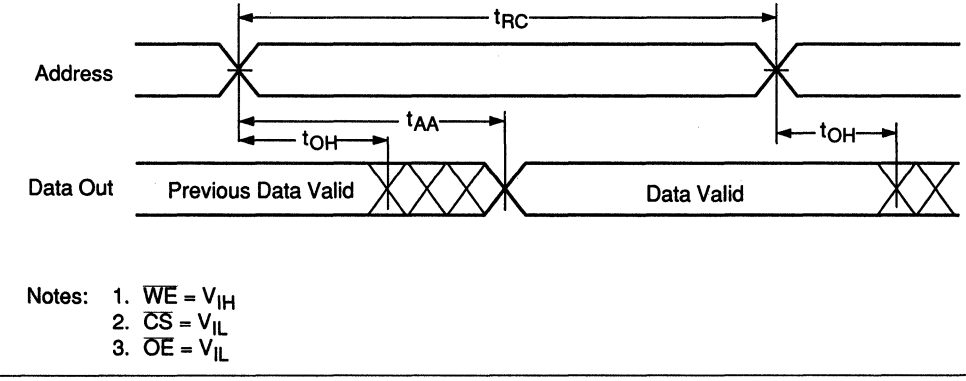
Timing Waveforms

Read Cycle 1



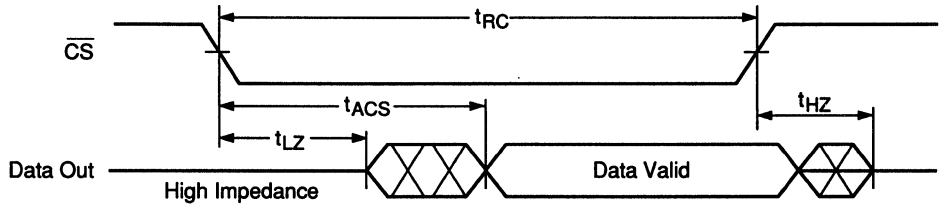
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle 2



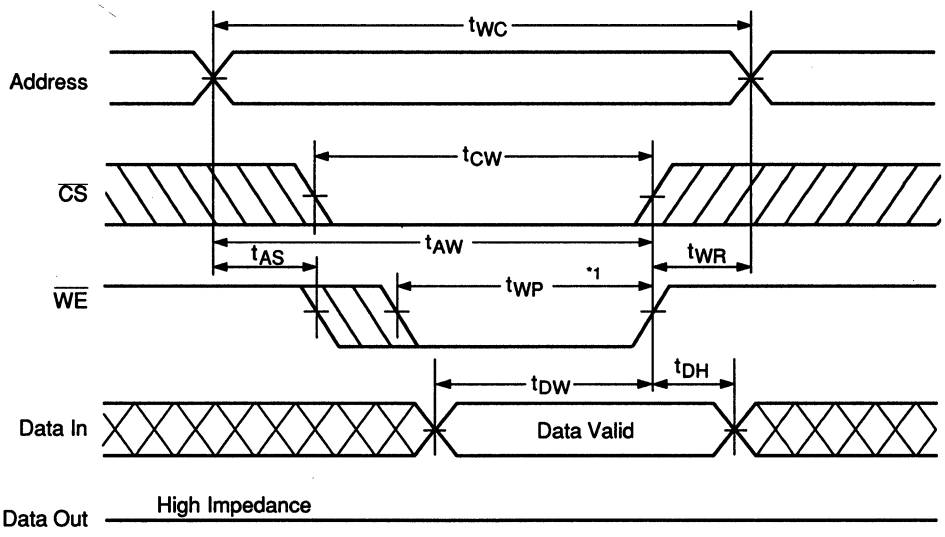
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle 3



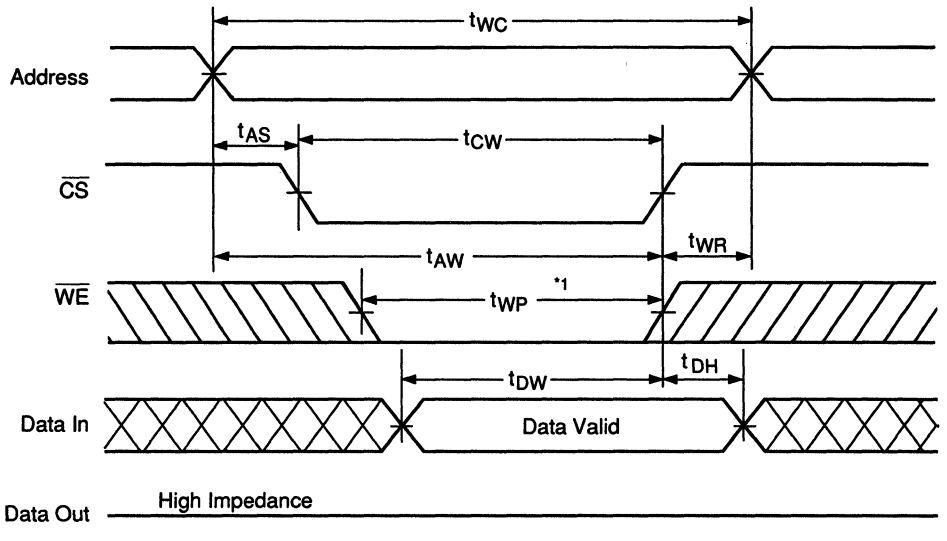
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



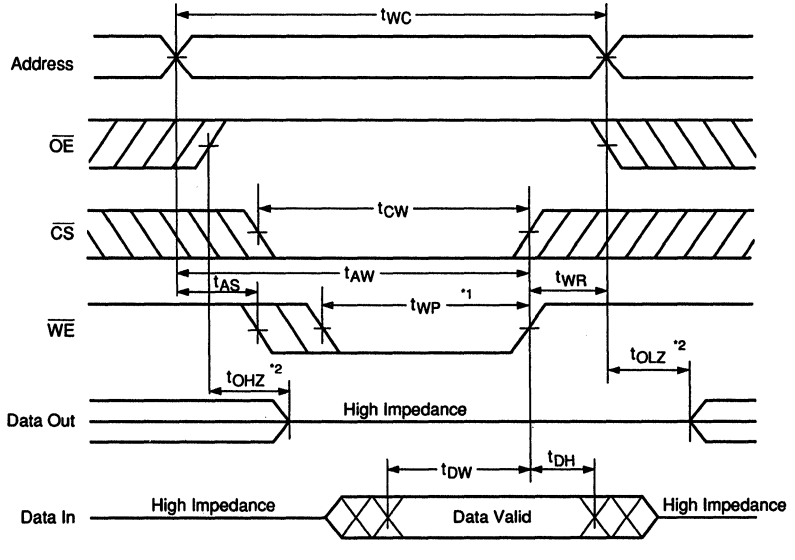
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



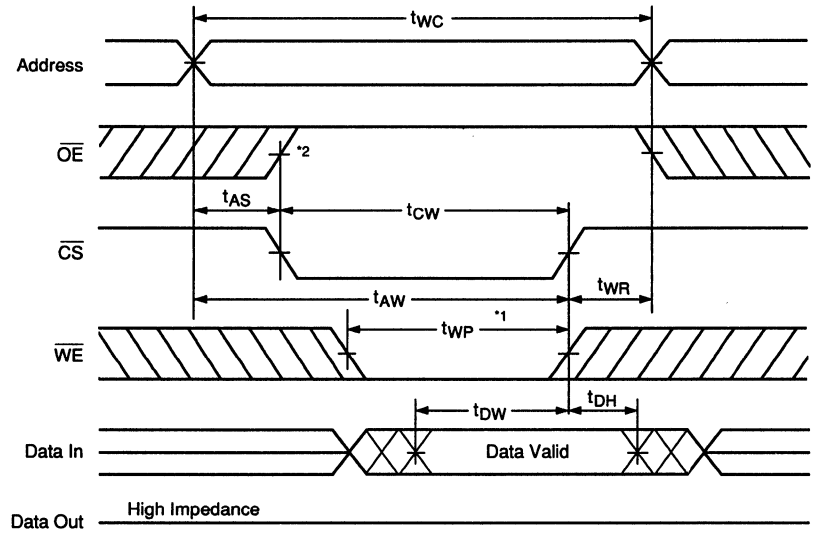
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



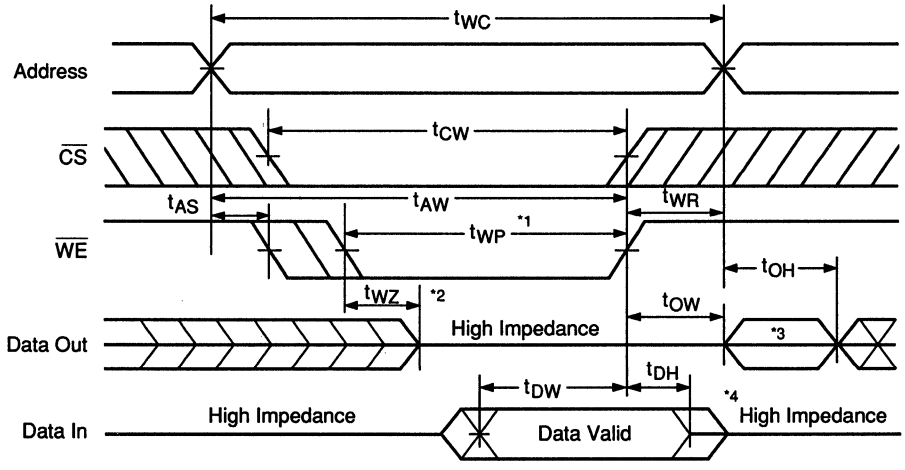
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



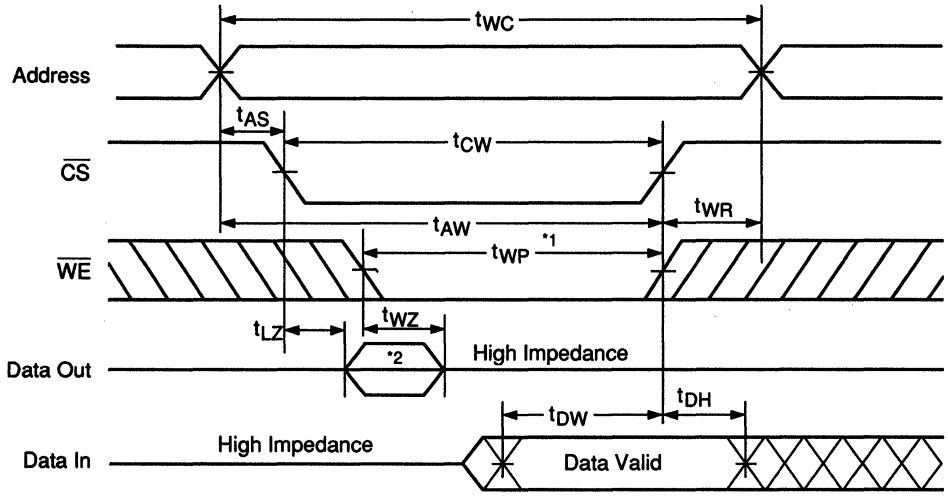
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle 6 ($\overline{OE}$ = L, $\overline{CS}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM674256UH Series — Under development

262144-words × 4-bits High Speed Static Random Access Memory

Features

- 262144-words × 4-bits organization
- Directly TTL compatible input and output
- Choice of 5.0 V or 3.3 V power supplies for output buffers
- Completely static memory
- No clock or timing strobe required
- Super fast access time: 10/12 ns (max)
- Revolutional pin arrangement

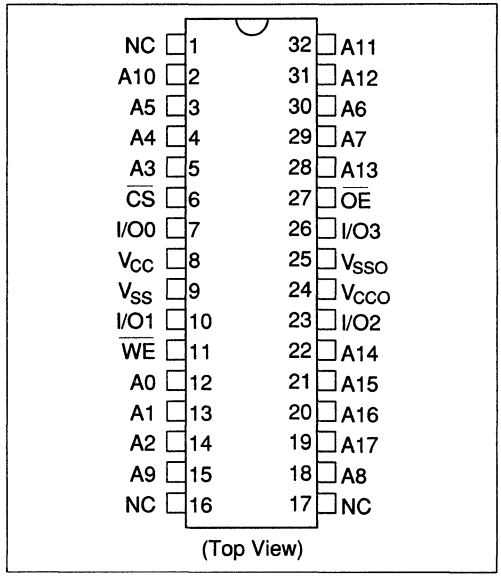
Ordering Information

Type No.	Access time	Package
HM674256UHJ-10	10 ns	400 mil 32pin Plastic SOJ (CP-32DB)
HM674256UHJ-12	12 ns	

Pin Description

Pin name	Function
A0 – A17	Address input
I/O0 – I/O3	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{CC}	+5 V power supply
V_{CCO}	Output buffer power supply
V_{SSO}	Output buffer ground
V_{SS}	Ground
NC	No connection

Pin Arrangement

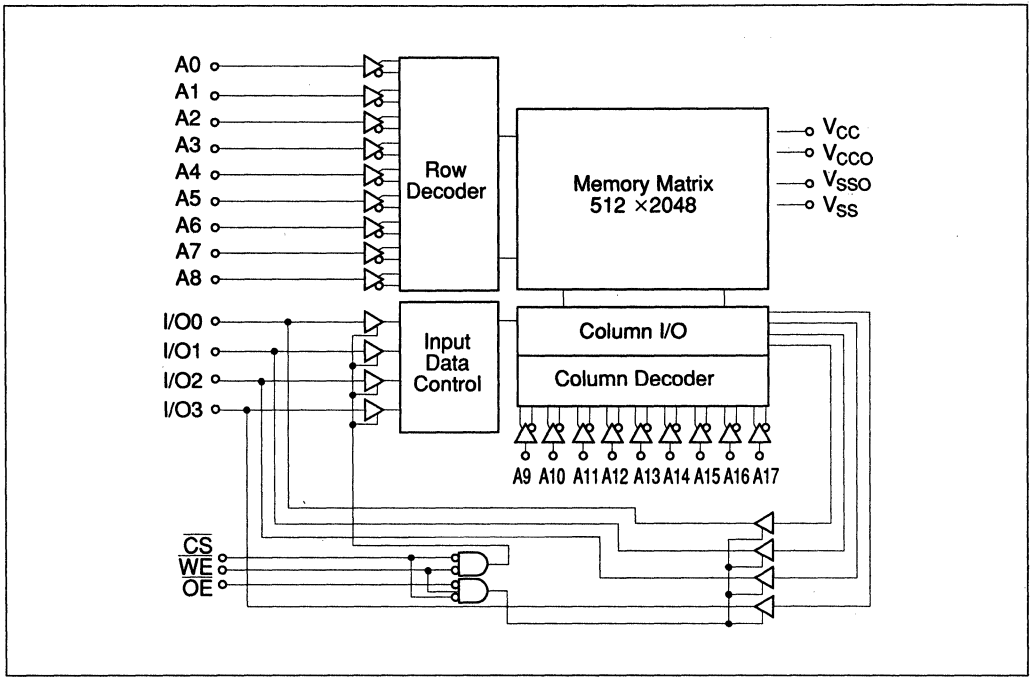


(Top View)

2

Note: This document contains information on a product under development.
Hitachi reserves the right to change or discontinue the product without notice.

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Output	Mode	V_{CC} current	Reference cycle
H	X	X	High-Z	Not selected	I_{SB}, I_{SB1}	—
L	H	H	High-Z	Output disable	I_{CC}, I_{CC1}	—
L	H	L	Data out	Read	I_{CC}, I_{CC1}	Read cycle 1, 2, 3
L	L	H	Data in	Write	I_{CC}, I_{CC1}	Write cycle 1, 2, 3, 4
L	L	L	Data in	Write	I_{CC}, I_{CC1}	Write cycle 5, 6

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}*1	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg(bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Note: 1. With respect to $V_{SS} = V_{SSO}$

For the DC and AC specifications shown in these tables, this device was tested under a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (0°C ≤ Ta ≤ 70°C)

Parameter		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.5	5.0	5.5	V
	5 V TTL compatible	V_{CCO}	4.5	5.0	5.5	V
	3.3 V TTL compatible		3.0	3.3	3.6	V
		V_{SS}, V_{SSO}	0.0	0.0	0.0	V
Input high voltage		V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage		V_{IL}	–0.5	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{CCO} = 5.0 V ± 10% or 3.3 V ± 0.3 V, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C)

		HM674256UH					
		-10		-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	2	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	10	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CCO}
Operating power supply current	I_{CC}	—	120	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	170	—	160	mA	Min. cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	40	—	40	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	30	—	30	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = –4 mA

Capacitance (Ta =25°C, f=1 MHz)

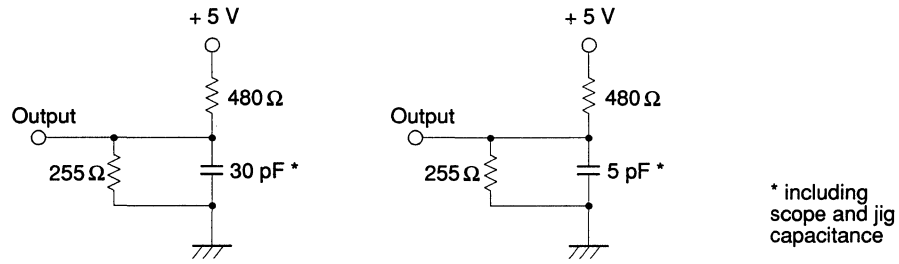
Parameter	**Symbol**	**Max**	**Unit**	**Test condition**
Input capacitance	C_{IN}*1	6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and has not been 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{CCO} = 5.0 V ± 10% or 3.3 V ± 0.3 V, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C, unless otherwise noted)

Test conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure
- Input rise and fall time: 4 ns
- Output reference level: 1.5 V



Read Cycle

		HM674256UH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Chip selection to output in low-Z	t_{LZ}*1, *2	3	—	4	—	ns
Output enable to output valid	t_{OE}	—	5	—	6	ns
Output enable to output in low-Z	t_{OLZ}*1, *2	0	—	0	—	ns
Chip deselection to output in high-Z	t_{HZ}*1, *2	0	5	0	6	ns
Output hold from address change	t_{OH}	3	—	4	—	ns

Notes: 1. This parameter is sampled and has not been 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

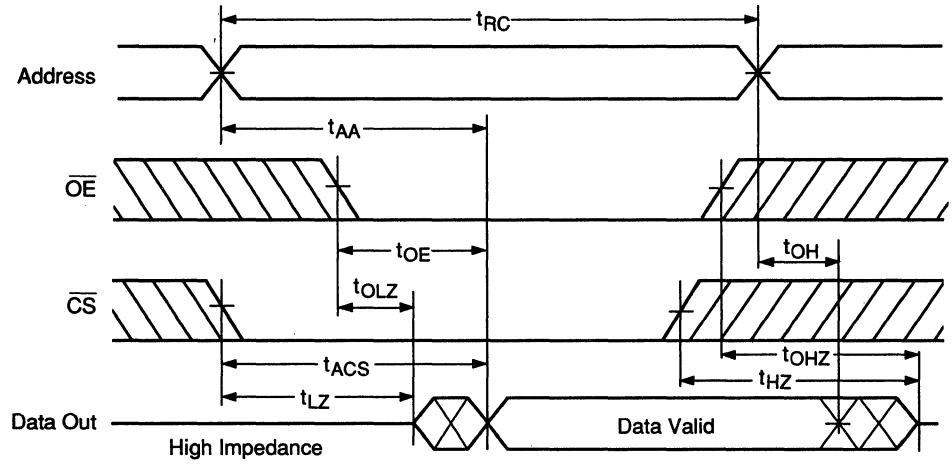
Write Cycle

		HM674256UH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}*1	10	–	12	–	ns
Chip selection to end of write	t_{CW}	8	–	10	–	ns
Address valid to end of write	t_{AW}	8	–	10	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	8	–	10	–	ns
Write recovery time	t_{WR}	0	–	0	–	ns
Data valid to end of write	t_{DW}	5	–	6	–	ns
Data hold time	t_{DH}	0	–	0	–	ns
Write enable to output in high-Z	t_{WZ}*2, *3	0	5	0	6	ns
Output disable to output in high-Z	t_{OHZ}*2, *3	0	5	0	6	ns
Output active from end of write	t_{OW}*2, *3	0	–	0	–	ns

Notes: 1. All write cycle timings are referred from the last valid address to the first transitioning address.
2. This parameter is sampled and has not been 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

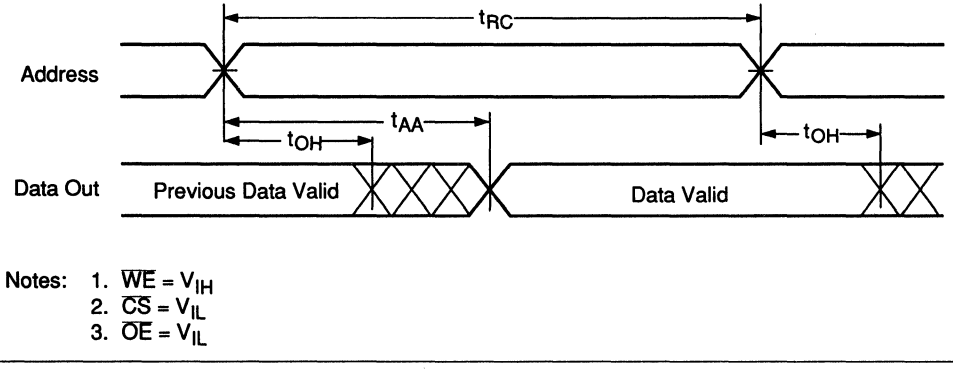
Timing Waveforms

Read Cycle 1



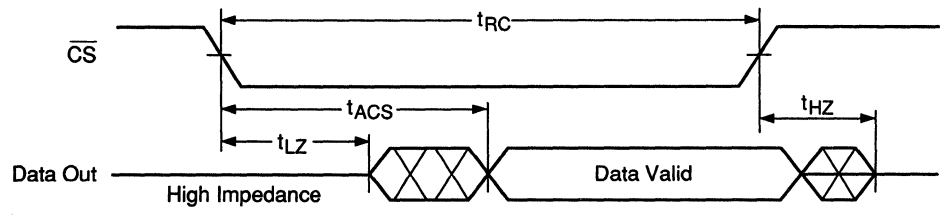
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle 2



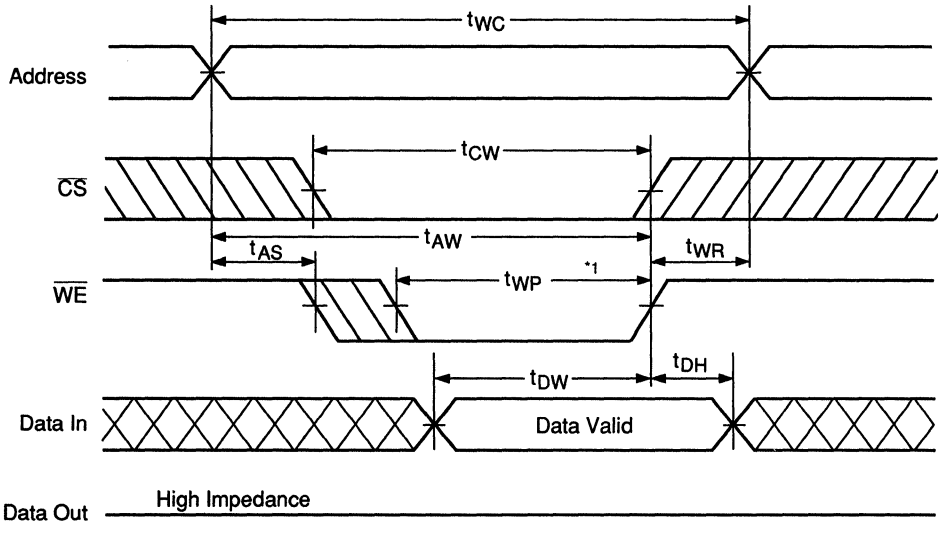
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle 3



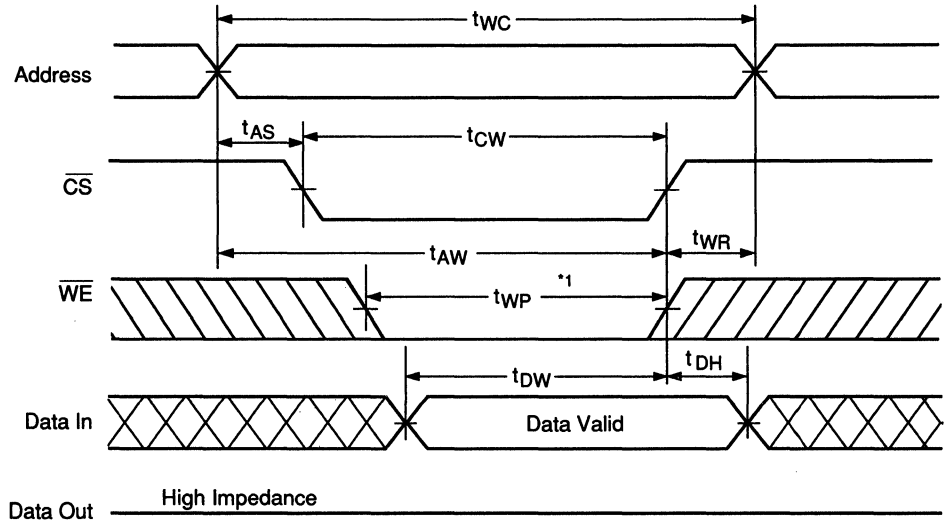
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



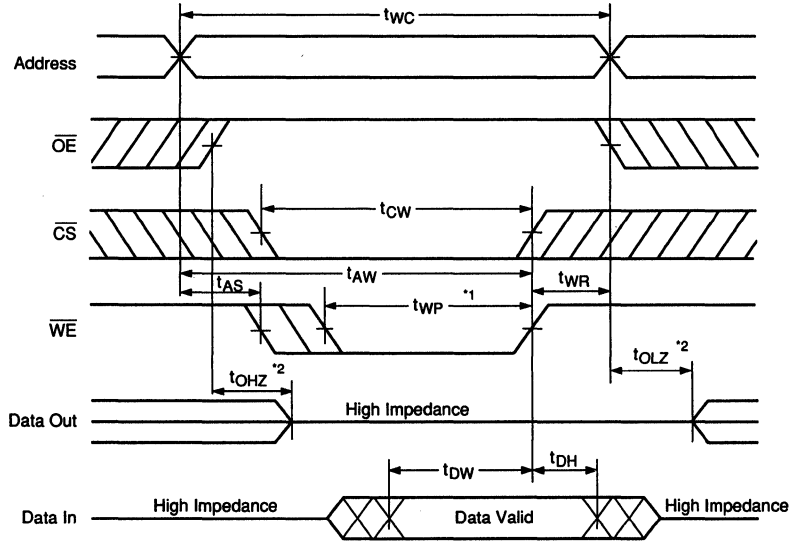
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



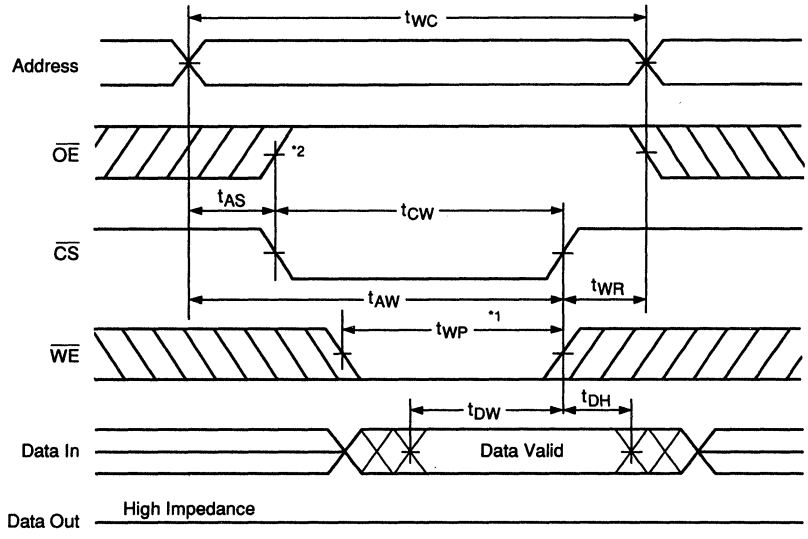
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



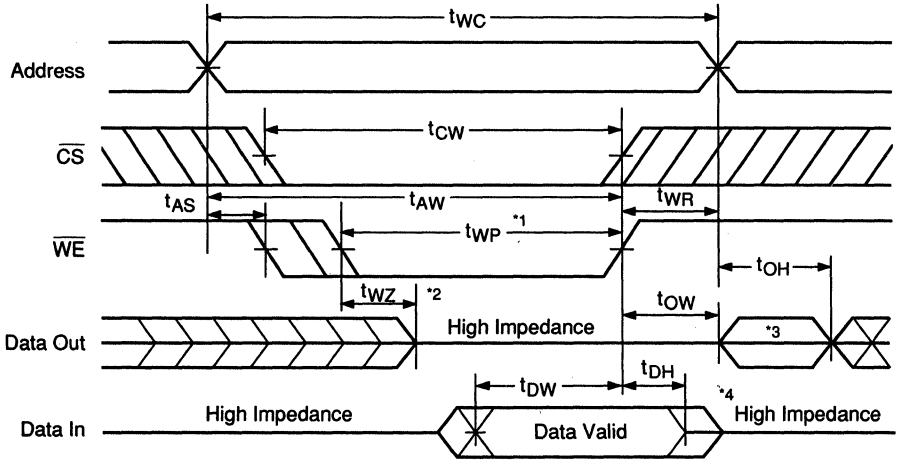
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



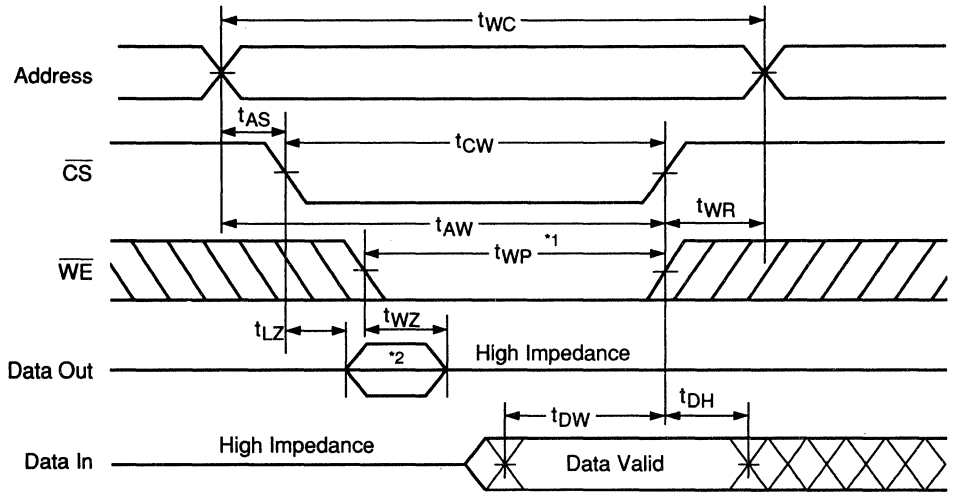
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle 6 ($\overline{OE}$ = L, $\overline{CS}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM678127UH Series — Under development

131072-words × 8-bits High Speed Static Access Memory

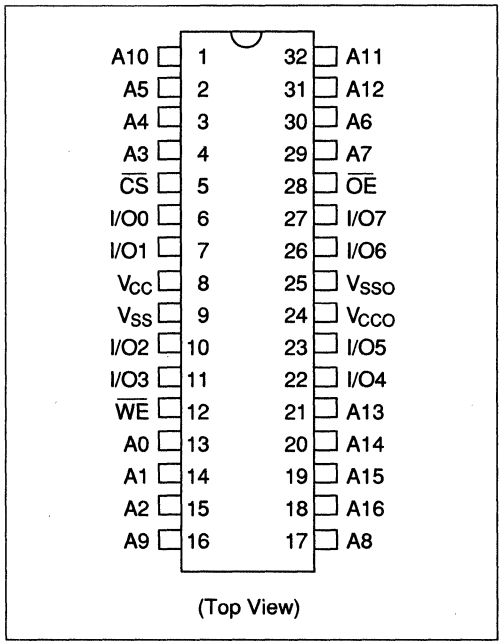
Features

- 131072-words × 8-bits organization
- Directly TTL compatible input and output
- Choice of 5.0 V or 3.3 V power supplies for output buffers
- Completely static memory
- No clock or timing strobe required
- Super fast access time: 10/12 ns (max)
- Revolutional pin arrangement

Ordering Information

Type No.	Access time	Package
HM678127UHJ-10	10 ns	400 mil 32 pin Plastic SOJ (CP-32DB)
HM678127UHJ-12	12 ns	

Pin Arrangement



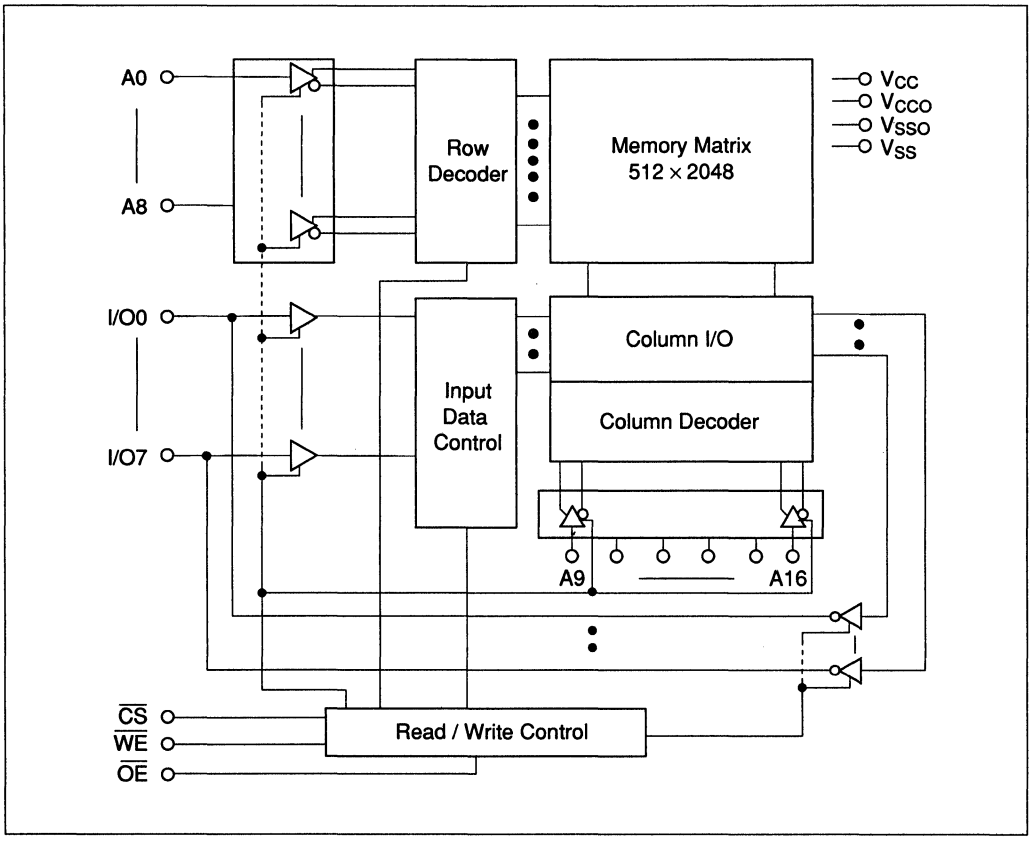
(Top View)

Pin Description

Pin name	Function
A0 – A16	Address input
I/O0 – I/O7	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{CC}	+5 V power supply
V_{CCO}	Output buffer power supply
V_{SSO}	Output buffer ground
V_{SS}	Ground
NC	No connection

Note: This document contains information on a product under development.
Hitachi reserves the right to change or discontinue the product without notice.

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Output	Mode	V_{CC} current	Reference cycle
H	X	X	High-Z	Not selected	I_{SB}, I_{SB1}	—
L	H	H	High-Z	Output disable	I_{CC}, I_{CC1}	—
L	H	L	Data out	Read	I_{CC}, I_{CC1}	Read cycle 1, 2, 3
L	L	H	Data in	Write	I_{CC}, I_{CC1}	Write cycle 1, 2, 3, 4
L	L	L	Data in	Write	I_{CC}, I_{CC1}	Write cycle 5, 6

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}*1	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg(bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Note: 1. With respect to $V_{SS} = V_{SSO}$

For the DC and AC specifications shown in these tables, this device was tested under a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions ($0°C \leq Ta \leq +70°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
5 V TTL compatible	V_{CCO}	4.5	5.0	5.5	V
3.3 V TTL compatible		3.0	3.3	3.6	V
	V_{SS}, V_{SSO}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage	V_{IL}	–0.5	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{CCO} = 5.0 V ± 10 % or 3.3 V ± 0.3 V, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C)

		HM678127UH					
		-10		-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	2	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	10	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CCO}
Operating power supply current	I_{CC}	—	120	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	200	—	190	mA	Min. cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	40	—	40	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	30	—	30	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = –4 mA

Capacitance (Ta =25°C, f=1 MHz)

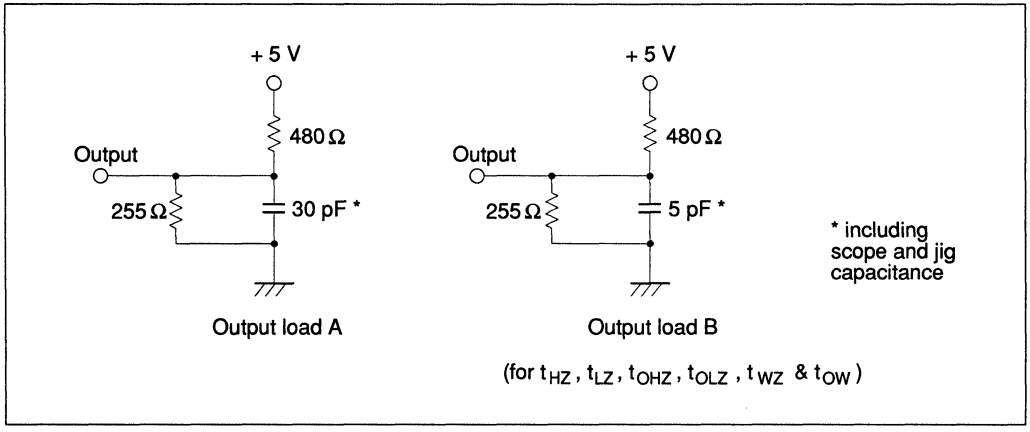
Parameter	**Symbol**	**Max**	**Unit**	**Test condition**
Input capacitance	C_{IN}*1	6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and has not been 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{CCO} = 5.0 V ± 10 % or 3.3 V ± 0.3 V, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C, unless otherwise noted)

Test conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure
- Input rise and fall time: 4 ns
- Output reference level: 1.5 V



Read Cycle

		HM678127UH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Chip selection to output in low-Z	t_{LZ}*1, *2	3	—	4	—	ns
Output enable to output valid	t_{OE}	—	5	—	6	ns
Output enable to output in low-Z	t_{OLZ}*1, *2	0	—	0	—	ns
Chip deselection to output in high-Z	t_{HZ}*1, *2	0	5	0	6	ns
Output hold from address change	t_{OH}	3	—	4	—	ns

Notes: 1. This parameter is sampled and has not been 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

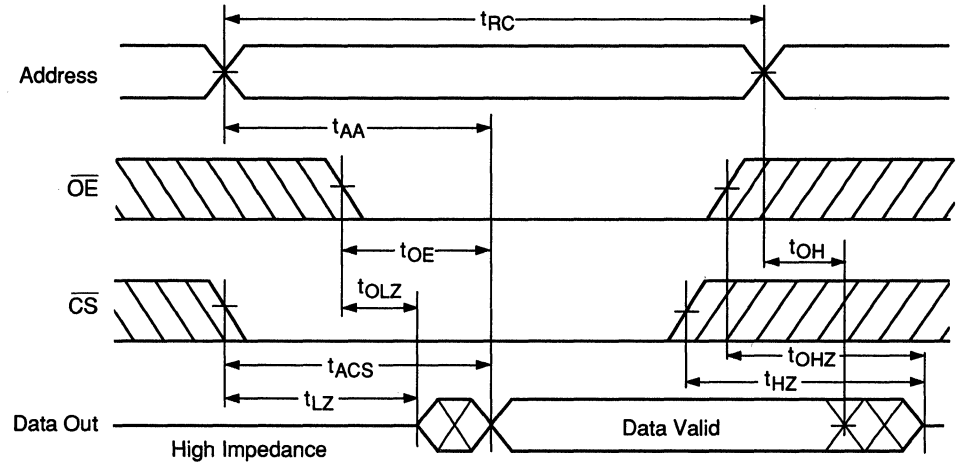
Write Cycle

		HM678127UH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}*1	10	–	12	–	ns
Chip selection to end of write	t_{CW}	8	–	10	–	ns
Address valid to end of write	t_{AW}	8	–	10	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	8	–	10	–	ns
Write recovery time	t_{WR}	0	–	0	–	ns
Data valid to end of write	t_{DW}	5	–	6	–	ns
Data hold time	t_{DH}	0	–	0	–	ns
Write enable to output in high-Z	t_{WZ}*2, *3	0	5	0	6	ns
Output disable to output in high-Z	t_{OHZ}*2, *3	0	5	0	6	ns
Output active from end of write	t_{OW}*2, *3	0	–	0	–	ns

Notes: 1. All write cycle timings are referred from the last valid address to the first transitioning address.
2. This parameter is sampled and has not been 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

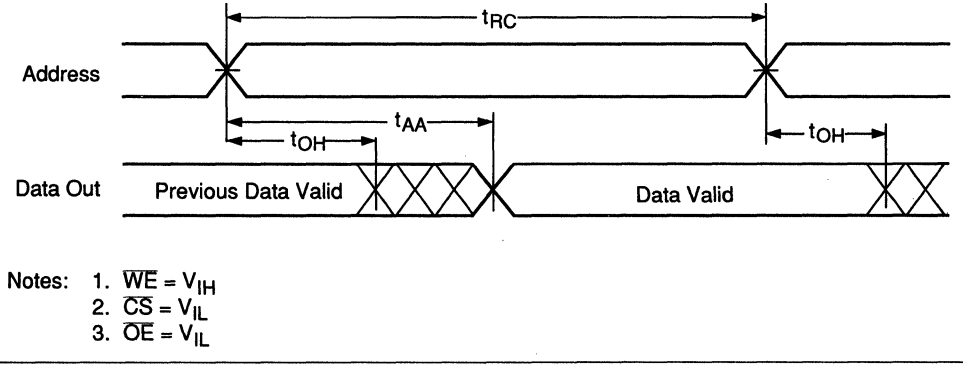
Timing Waveforms

Read Cycle 1



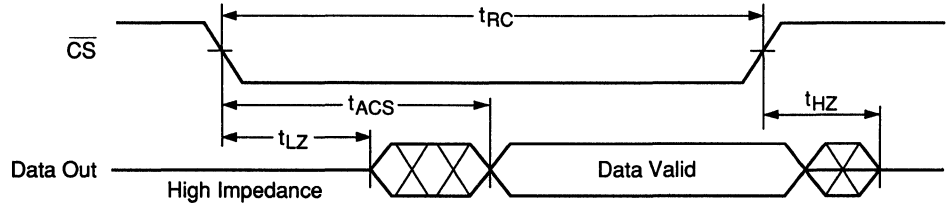
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle 2



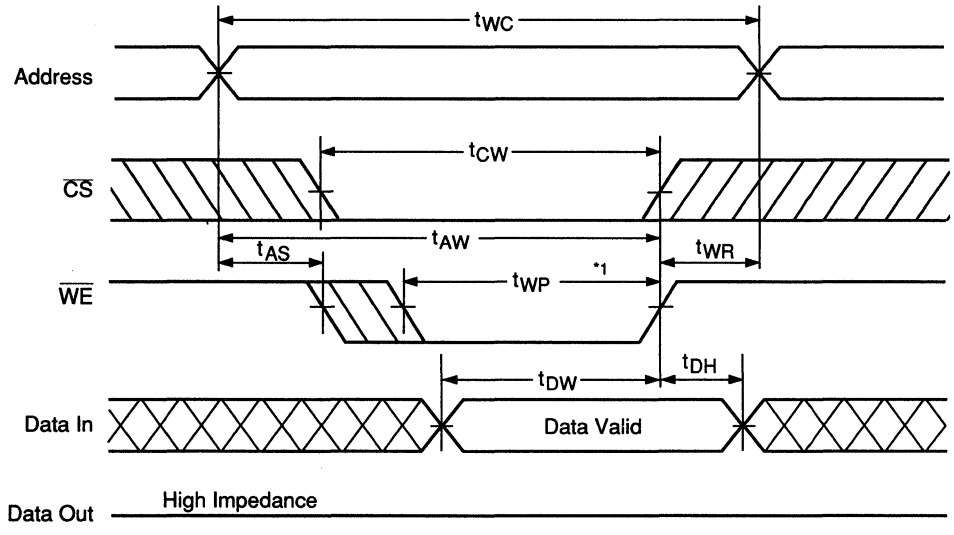
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle 3



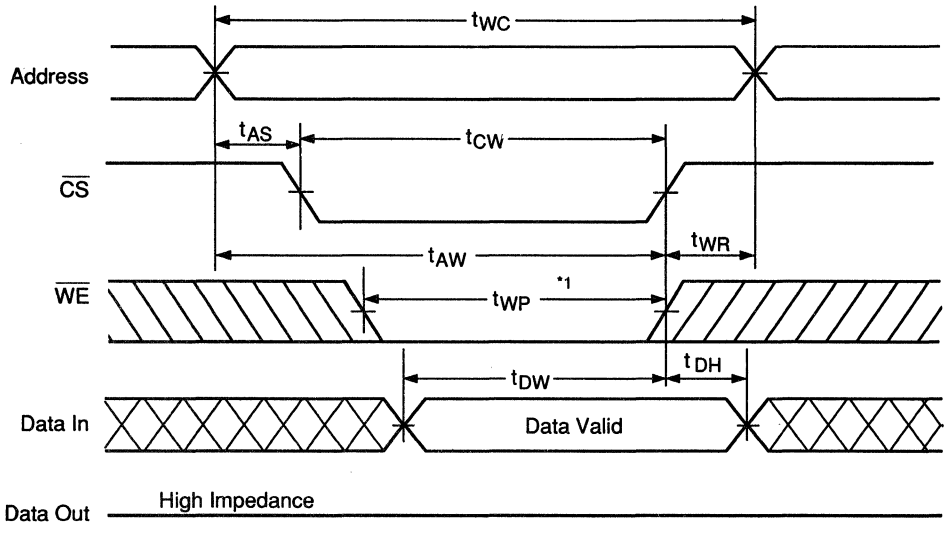
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



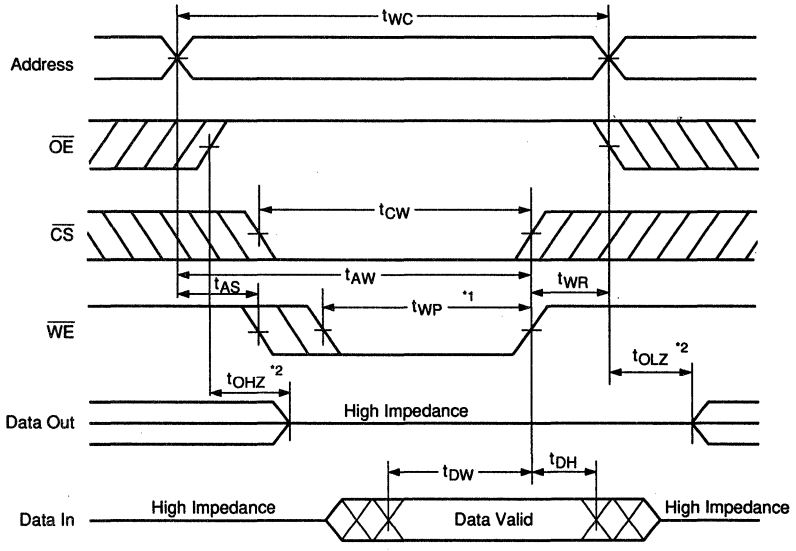
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



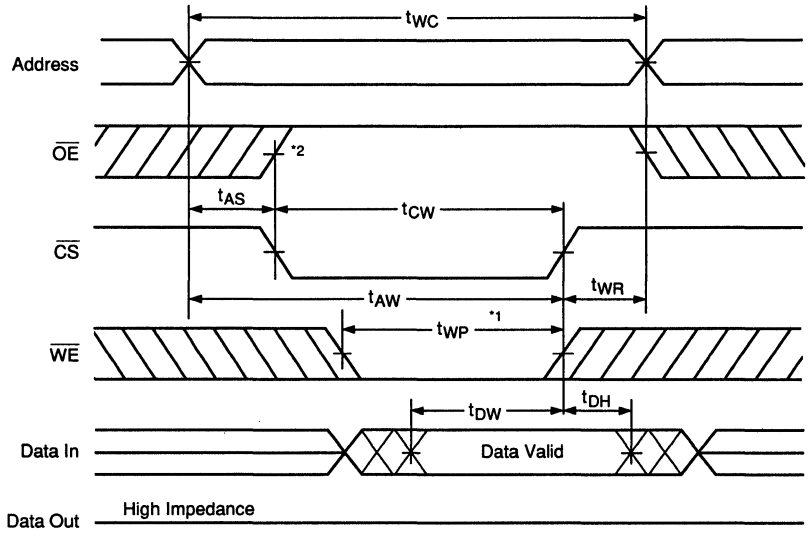
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



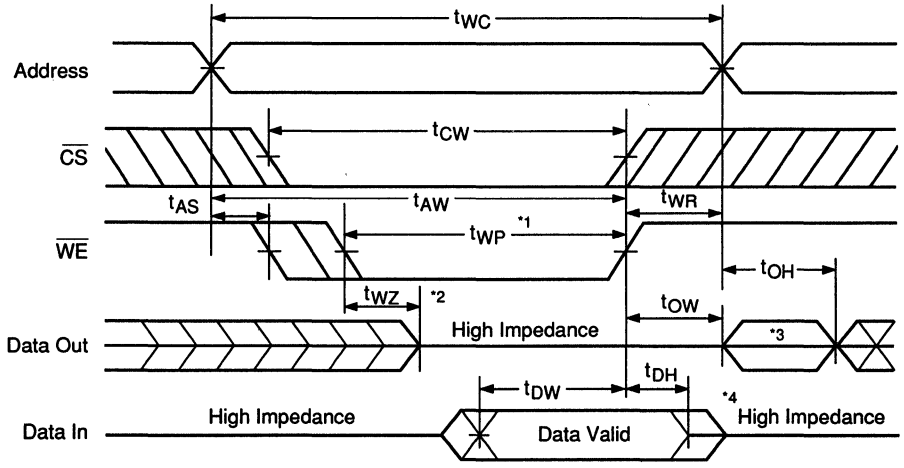
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle 4 ($\overline{OE}$ = clocked, $\overline{CS}$ controlled)



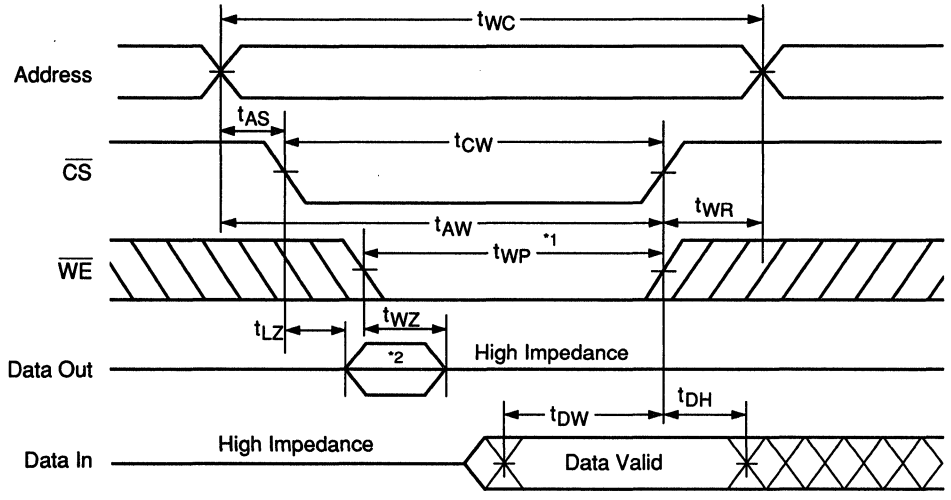
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle 6 ($\overline{OE}$ = L, $\overline{CS}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

1048576-word × 4 bit High Speed Static Random Access Memory

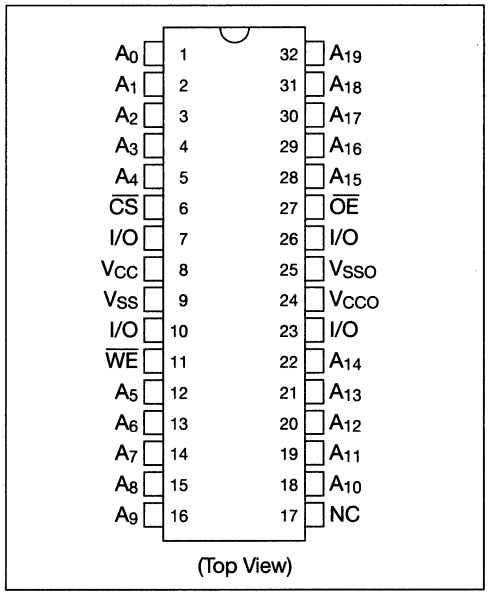
Features

- 1048576-word × 4-bit organization
- Directly TTL compatible input and output
- +5V Single Supply
- Completely static memory
- No clock or timing strobe required
- Super fast access time: 15/20/25ns (max)
- Revolutional Pin Arrangement

Ordering Information

Type No.	Organization	Access time	Package
HM674100HJP-15	1M×4	15ns	400mil 32 pin Plastic SOJ (CP-32DB)
HM674100HJP-20		20ns	
HM674100HJP-25		25ns	
HM674100HTT-15	1M×4	15ns	400mil 32 pin Plastic TSOPII (TTP-32DA)
HM674100HTT-20		20ns	
HM674100HTT-25		25ns	

Pin Arrangement



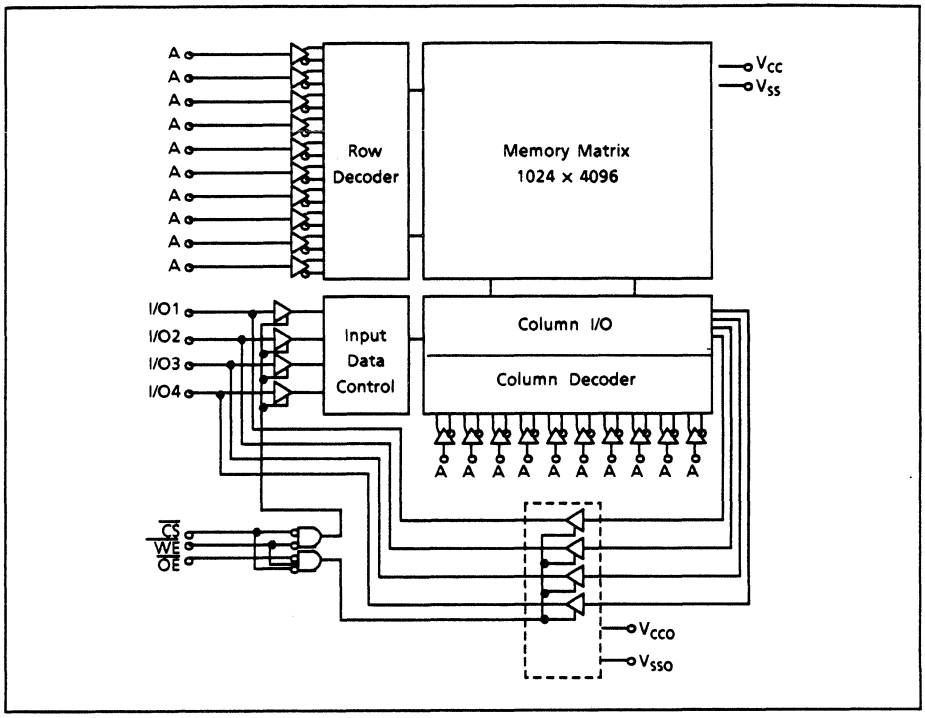
(Top View)

Pin Description

Pin Name	Function
A_0–A_{19}	Address Input
I/O_0–I/O_3	Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
V_{CC}	+5V Power Supply
V_{CCO}	Output Buffer Power Supply
V_{SSO}	Output Buffer Ground
V_{SS}	Ground
NC	Not Connect

Note: Product Preview: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

Block Diagram



Function Table

Input			Mode	I/O Pin	V_{CC} Current	Ref. Cycle
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$				
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}	-
L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	-
L	H	L	Read	Data Out	I_{CC}, I_{CC1}	Read Cycle (1), (2), (3)
L	L	H	Write	Data In	I_{CC}, I_{CC1}	Write Cycle (1), (2), (3), (4)
L	L	L	Write	Data Out	I_{CC}, I_{CC1}	Write Cycle (5), (6)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage [1]	V_{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V_{SS} [1]	V_T	−0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg}(Bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Notes 1) With respect to $V_{SS} = V_{SSO}$

Under the dc and ac specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

2

Recommended DC Operating Conditions (0°C ≦ Ta ≦ 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}, V_{CCO}	4.5	5.0	5.5	V
	V_{SS}, V_{SSO}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	TBD	-	0.8	V

DC and Operating Characteristics

($V_{CC} = V_{CCO} = 5.0\ V \pm 10\%$, $V_{SS} = V_{SSO} = 0\ V$, $Ta = 0$ to $+70°C$)

Item	Symbol	Test Conditions	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ to V_{CC}	-	2	-	2	-	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$ $V_{I/O} = 0\ V$ to V_{CC}	-	10	-	10	-	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O} = 0\ mA$	-	120	-	120	-	120	mA
Average Operating Current	I_{CC1}	min cycle, $I_{I/O} = 0\ mA$	-	220	-	200	-	160	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}	-	100	-	80	-	60	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2\ V$ $V_{IN} \leq 0.2\ V$ or $V_{IN} \geq V_{CC} - 0.2\ V$	-	20	-	20	-	20	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8\ mA$	-	0.4	-	0.4	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4\ mA$	2.4	-	2.4	-	2.4	-	V

AC Characteristics

($V_{CC} = V_{CCO} = 5\ V \pm 10\%$, $V_{SS} = V_{SSO} = 0\ V$, $Ta = 0°C$ to $70°C$, unless otherwise noted.)

• Read Cycle

Item	Symbol	-15		-20		-25		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	15	-	20	-	25	-	ns
Address Access Time	t_{AA}	-	15	-	20	-	25	ns
Chip Select Access Time	t_{ACS}	-	15	-	20	-	25	ns
Chip Selection to Output in Low Z	t_{LZ} 1), 2)	5	-	5	-	5	-	ns
Output Enable to Output Valid	t_{OE}	-	8	-	10	-	15	ns
Output Enable to Output in Low Z	t_{OLZ} 1), 2)	2	-	2	-	2	-	ns
Chip Deselection to Output in High Z	t_{HZ} 1), 2)	0	6	0	8	0	15	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns

Notes 1) This parameter is sampled and not 100% tested.
2) Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

• Write Cycle

Item	Symbol	-15		-20		-25		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC} 1)	15	-	20	-	25	-	ns
Chip Selection to End of Write	t_{CW}	12	-	15	-	17	-	ns
Address Valid to End of Write	t_{AW}	12	-	15	-	17	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	12	-	15	-	17	-	ns
Write Recovery Time	t_{WR}	3	-	3	-	3	-	ns
Data Valid to End of Write	t_{DW}	8	-	10	-	15	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	ns
Write Enable to Output in High Z	t_{WZ} 2), 3)	0	6	0	8	0	12	ns
Output Disable to Output in High Z	t_{OHZ} 2), 3)	0	6	0	8	0	10	ns
Output Active from End of Write	t_{OW} 2), 3)	2	-	2	-	2	-	ns

Notes 1) All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2) This parameter is sampled and not 100% tested.
3) Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

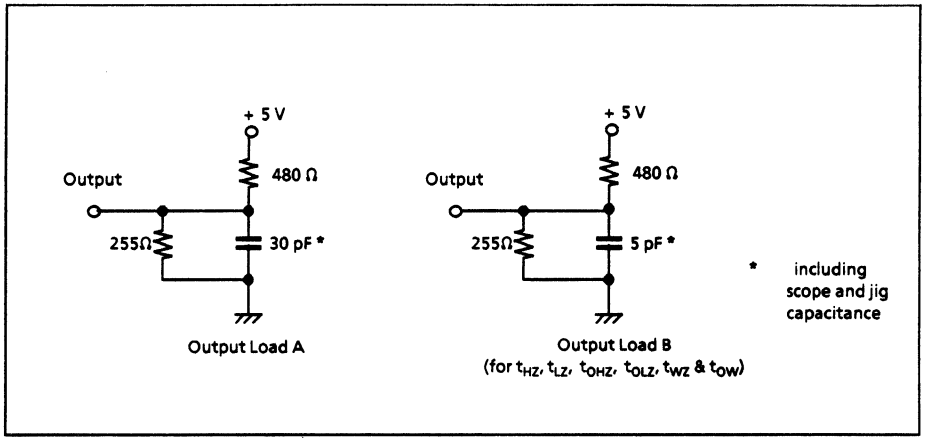
Capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	max	Unit	Test Condition
Input Capacitance	C_{IN} 1)	6	pF	V_{IN} = 0 V
Input/Output Capacitance	$C_{I/O}$ 1)	10	pF	$V_{I/O}$ = 0 V

Notes 1) This parameter is sampled and not 100% tested.

AC Test Conditions

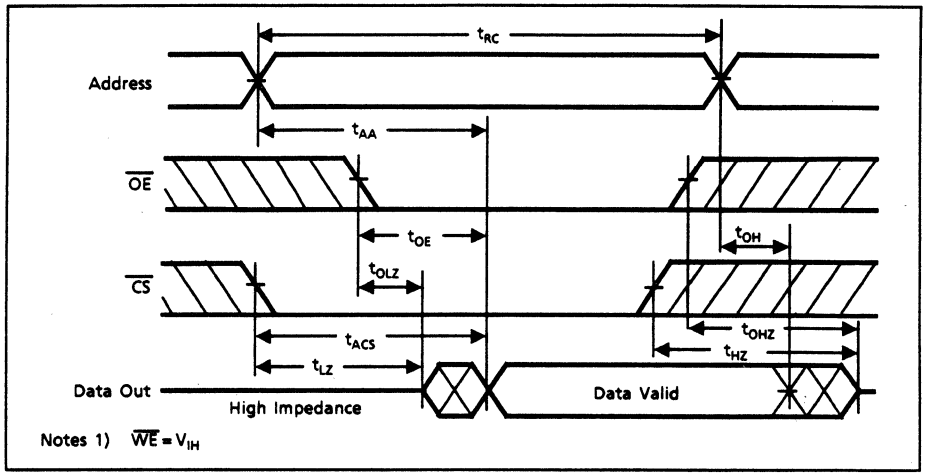
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5 V



2

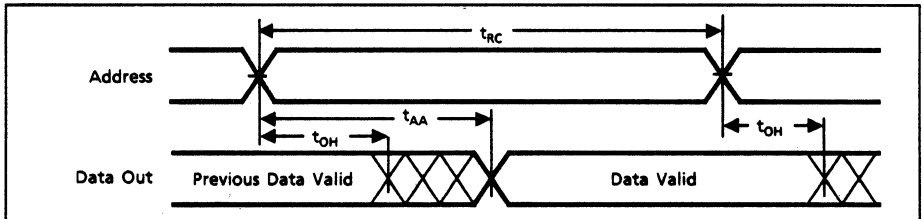
Timing Waveforms

Read Cycle – 1 [1]



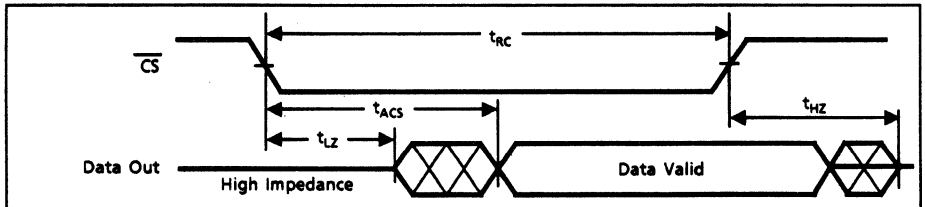
Notes 1) $\overline{WE} = V_{IH}$

Read Cycle – 2 [1], [2], [3]



Notes 1) $\overline{WE} = V_{IH}$
2) $\overline{CS} = V_{IL}$
3) $\overline{OE} = V_{IL}$

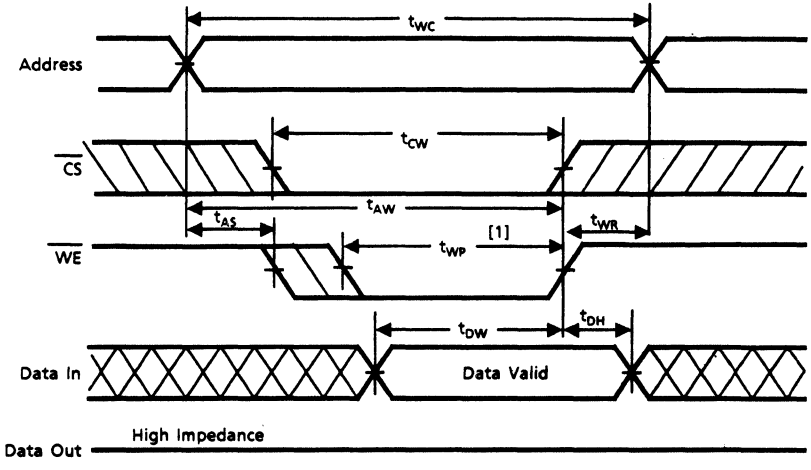
Read Cycle – 3 [1], [2], [3]



Notes 1) $\overline{WE} = V_{IH}$
2) $\overline{OE} = V_{IL}$
3) Address valid prior to or coincident with $\overline{CS}$ transition low.

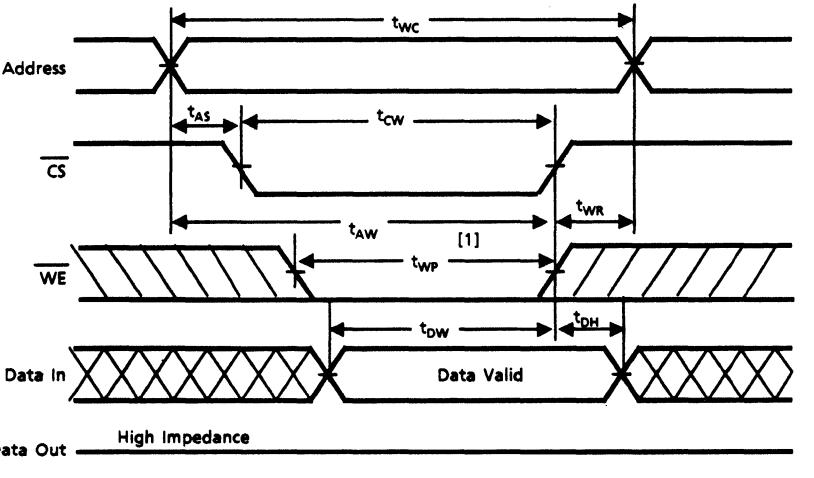
Timing Waveforms

Write Cycle – 1 [1] ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



Notes 1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$(t_{WP}).

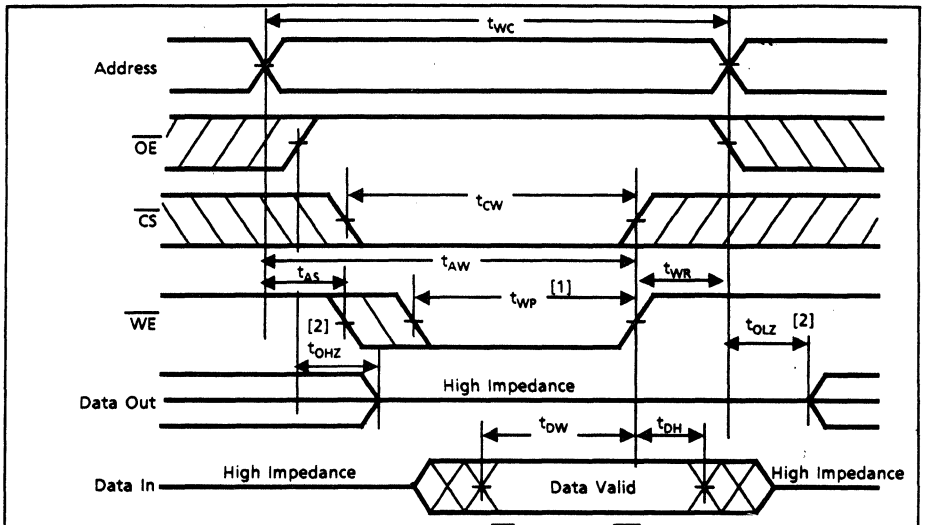
Write Cycle – 2 [1] ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



Notes 1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$(t_{WP}).

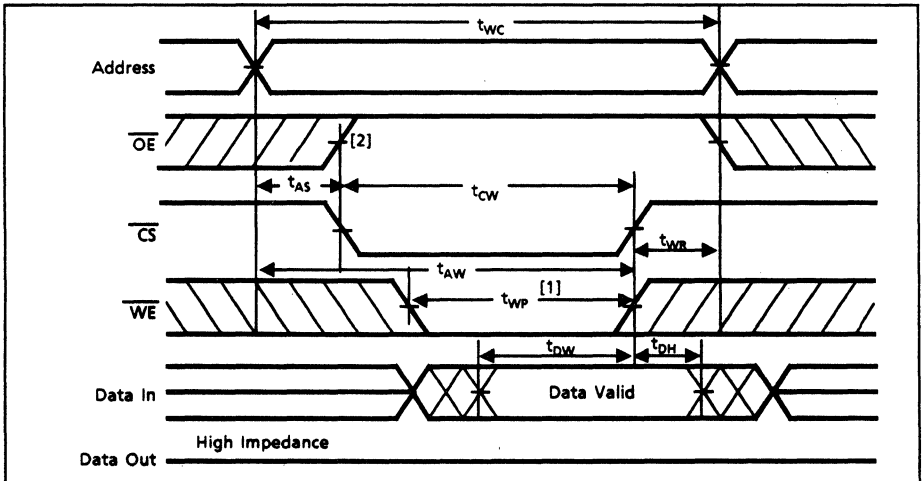
Timing Waveforms

Write Cycle – 3 [1],[2] ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



Notes 1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$(t_{WP}).
2) During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

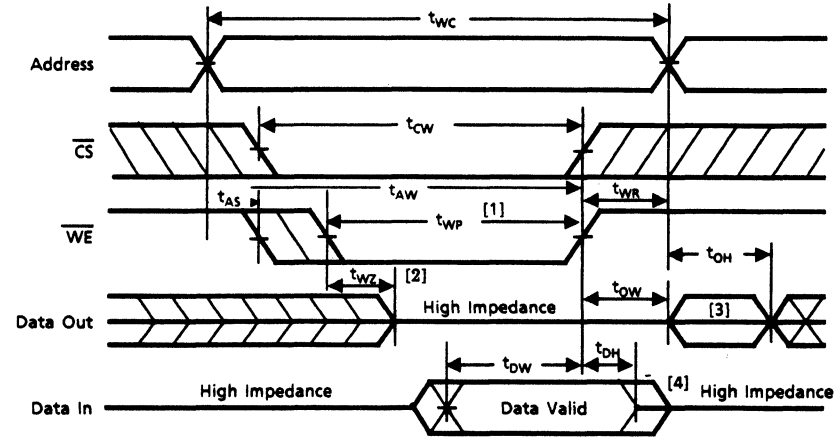
Write Cycle – 4 [1], [2] ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Notes 1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$(t_{WP}).
2) If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

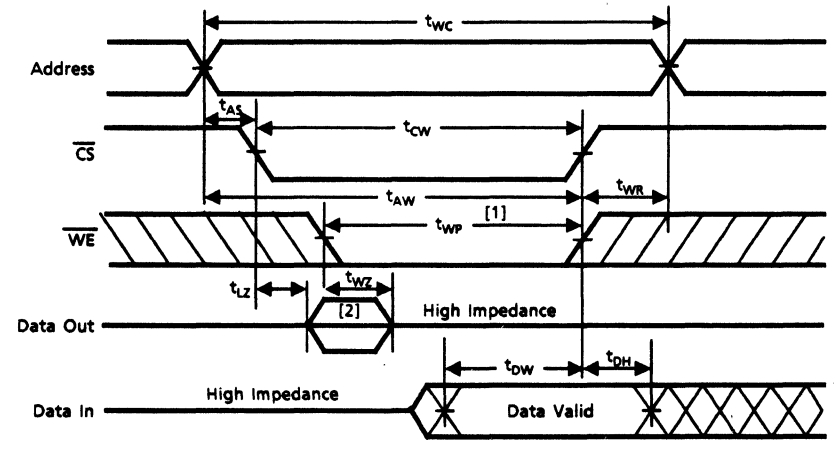
Timing Waveforms

Write Cycle – 5 [1], [2], [3], [4] ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Notes 1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$(t_{WP}).
2) During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must nit be applied.
3) Output data is the same phase of write data of this write cycle.
4) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle – 6 [1], [2] ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes 1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$(t_{WP}).
2) If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM101484HF-4/4.5

Preliminary

4096-word × 4 bit Fully Decoded Random Access Memory

ECL I/O

Description

The HM101484H is ECL 100k compatible, 4096-word by 4-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

- 4096 × 4-bit organization
- Fully compatible with 100k ECL level
- Address access time: 4/4.5 ns (max)
- Write pulse width: 5ns (min)
- Low power dissipation: 1000mW (typ)

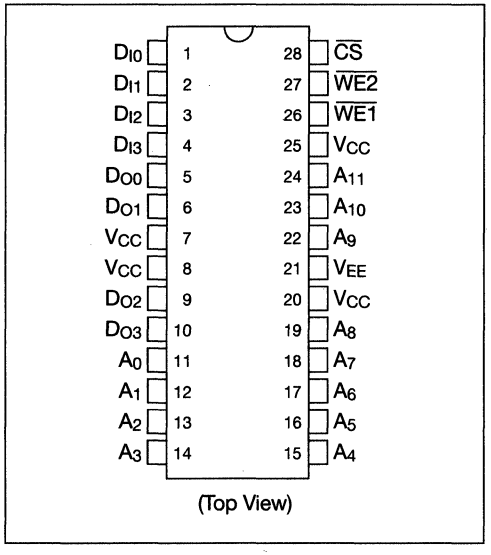
Ordering Information

Type No.	Access time	Package
HM101484HF-4	4 ns	28pin Ceramic Flat (FG-28D)
HM101484HF-4.5	4.5 ns	

Pin Description

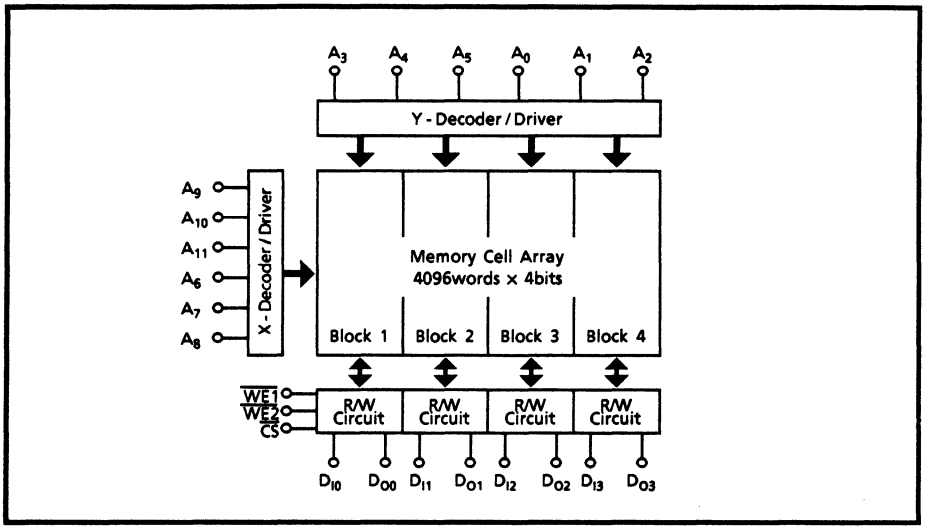
Pin Name	Function
A_0–A_{11}	Address Input
D_{10}–D_{13}	Data Input
D_{O0}–D_{O3}	Data Output
$\overline{WE1}$, $\overline{WE2}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

Pin Arrangement



(Top View)

Block Diagram



Function Table

Input				Output	Mode
$\overline{CS}$	$\overline{WE1}$	$\overline{WE2}$	Din		
H	X 1)	X	X 1)	L	Not Selected
L	L	L	L	L	Write "0"
L	L	L	H	L	Write "1"
L	X	H	X 1)	Dout 2)	Read
L	H	X	X 1)	Dout 2)	Read

Note 1) Don't Care
2) Read Out Noninvent

Absolute Maximum Rating (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+ 0.5 to − 7.0	V
Input Voltage	V_{in}	+ 0.5 to V_{EE}	V
Output Current	I_{out}	− 30	mA
Storage Temperature	T_{stg}	− 65 to + 150	°C
Storage Temperature	T_{stg}(Bias) 1)	− 55 to + 125	°C

Note 1) Under Bias, (V_{EE} = − 6.0V min)

Electrical Characteristics

• DC Characteristics (V_{EE} = −5.2 V, R_L = 50Ω to −2.0 V, Tc = 0 to +75°C)

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	$V_{in} = V_{IHA}$ or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035			mV	$V_{in} = V_{IHB}$ or V_{ILA}
	V_{OLC}			−1610	mV	
Input Voltage	V_{IH}	−1165		−880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	−1810		−1475	mV	
Input Current	I_{IH}			220	μA	$V_{in} = V_{IHA}$
	I_{IL}	0.5		170	μA	$V_{in} = V_{ILB}$ $\overline{CS}$
		−50			μA	Others
Supply Current	I_{EE}	−300			mA	All Outputs Open t_{CYC} = 8ns

• AC Characteristics (V_{EE} = −5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

		HM101484HF-4			HM101484HF-4.5				
Item	Symbol	min	typ	max	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}			4			4.5	ns	
Chip Select Recovery Time	t_{RCS}			3			3	ns	
Address Access Time	t_{AA}			4			4.5	ns	

Write Mode

		HM101484HF-4			HM101484HF-4.5				
Item	Symbol	min	typ	max	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	5			5			ns	$t_{WSA} = t_{WSA}$ min
Data Setup Time	t_{WSD}	1.5			1.5			ns	
Data Hold	t_{WHD}	1.5			1.5			ns	
Address Setup Time	t_{WSA}	1.5			1.5			ns	$t_W = t_W$ min
Address Hold Time	t_{WHA}	1.5			1.5			ns	
Chip Select Setup Time	t_{WSCS}	1.5			1.5			ns	
Chip Select Hold Time	t_{WHCS}	1.5			1.5			ns	
Write Disable Time	t_{WS}			3			3	ns	
Write Recovery Time	t_{WR}			5.5			6	ns	

Rise/Fall Time

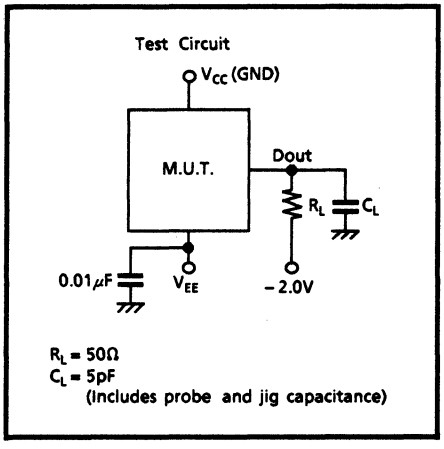
Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r		1		ns	
Output Fall Time	t_f		1		ns	

Capacitance

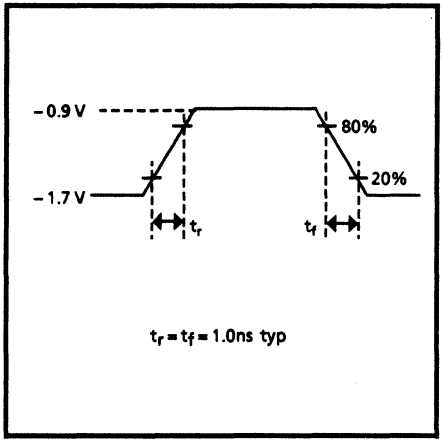
Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	Cin		2		pF	
Output Capacitance	Cout		3		pF	

Test Condition

- **Loading Condition**

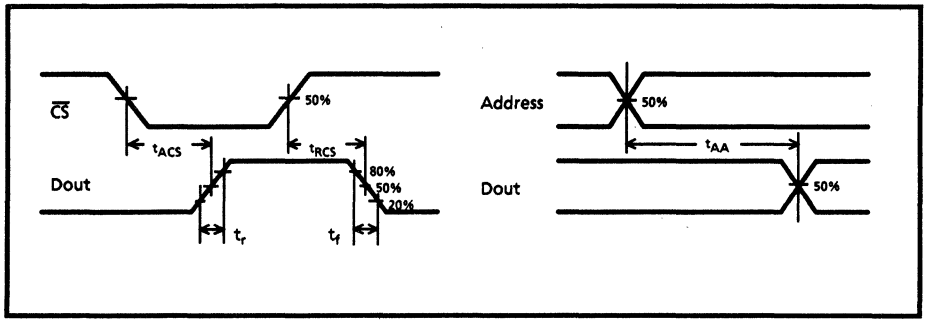


- **Input Pulse**

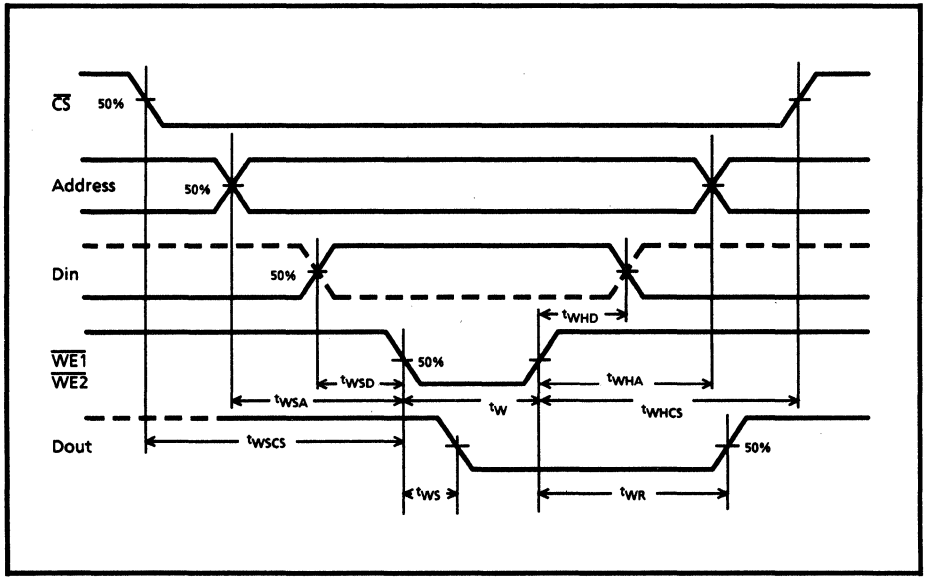


Timing Waveforms

• Read Mode



• Write Mode



HM101514 Series

262,144-word × 4-bit Random Access Memory

The Hitachi HM101514 is ECL 100 K compatible, 262,144 words by 4 bits read/write random access memory developed for high speed systems.

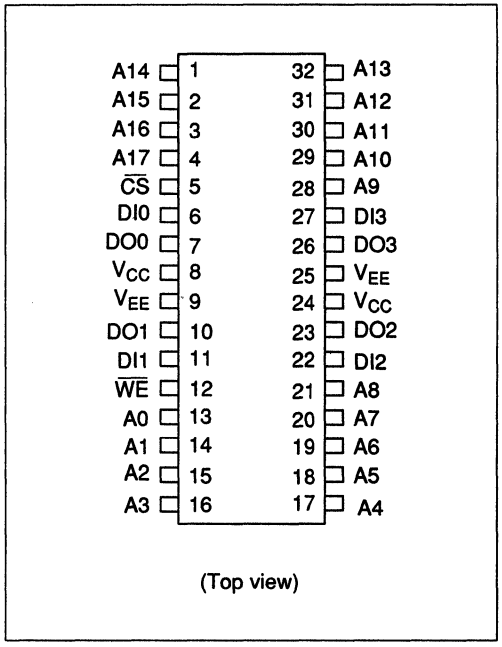
Features

- 262,144-words × 4 bit organization
- Fully compatible with 100 K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time : 13/15 ns max
- Write pulse width : 8/9 ns min
- Low power dissipation: 800 mW typ
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM101514JP-13	13 ns	400-mil 32-pin plastic SOJ (CP-32D)
HM101514JP-15	15 ns	

Pin Arrangement

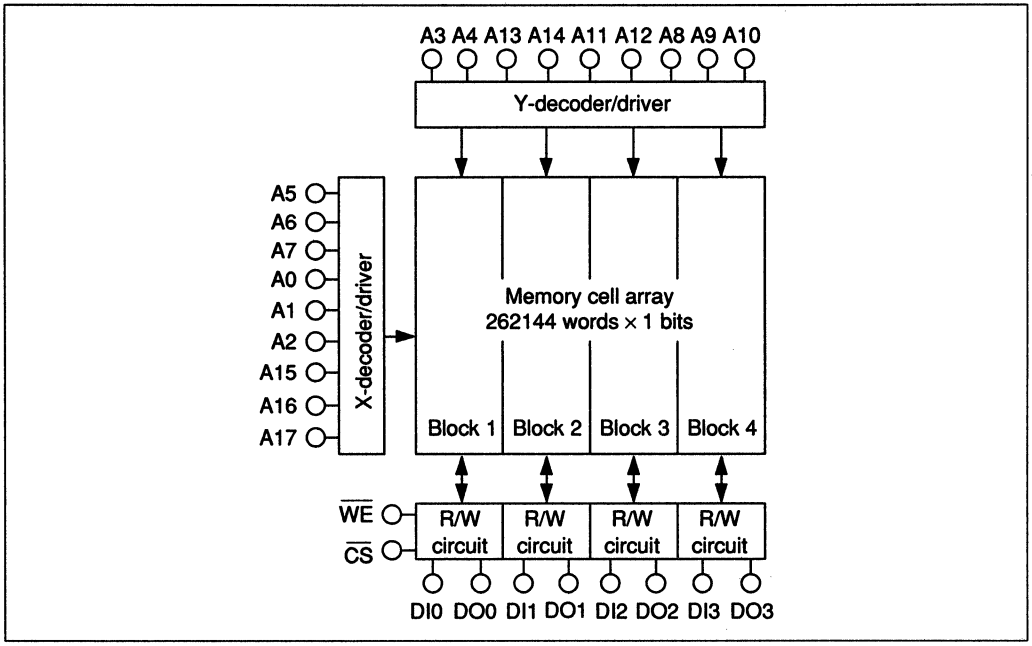


(Top view)

Pin Description

Pin name	Function
A0 – A17	Address input
DI0 – DI3	Data input
DO0 – DO3	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	X*1	X*1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X*1	Dout*2	Read

Notes: 1. Irrelevant.
2. Read out noninvert.

Absolute Maximum Rating (Tj = 125°C max)

Parameter	Symbol	SOJ Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Power dissipation	P_T	1.2	W
Operating temperature	Topr	0 to +85 *2	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature	Tstg (Bias) *1	–10 to +85 *2	°C

Notes: 1. Under bias (V_{EE} = –6.0 V min)
2. Case temperature

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Parameter	Symbol	Min (B)	Typ	Max (A)	Unit	Test condition	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–200	—	—	mA	All outputs open	

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

		HM101514-13			HM101514-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test condition**
Chip select access time	t_{ACS}	—	—	10	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	—	—	10	ns	
Address access time	t_{AA}	—	—	13	—	—	15	ns	

Write Mode

		HM101514-13			HM101514-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test condition**
Write pulse width	t_W	8	—	—	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	2	—	—	3	—	—	ns	
Data hold	t_{WHD}	3	—	—	3	—	—	ns	
Address setup time	t_{WSA}	2	—	—	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	3	—	—	ns	
Chip select setup time	t_{WSCS}	2	—	—	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	3	—	—	ns	
Write disable time	t_{WS}	—	—	13	—	—	15	ns	
Write recovery time	t_{WR}	—	—	16	—	—	18	ns	

Rise/Fall Time

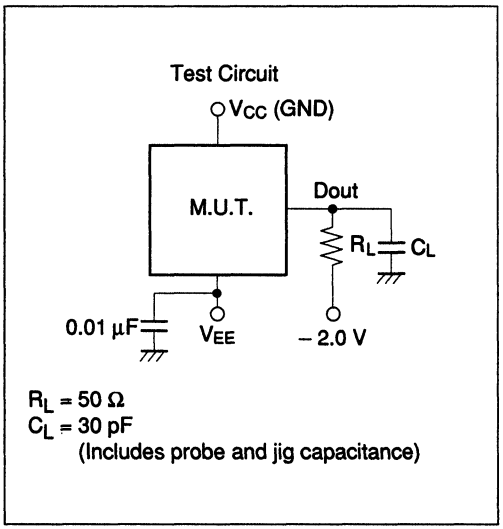
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test condition**
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

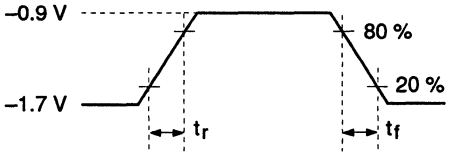
Test Circuit and Waveforms

Loading Condition



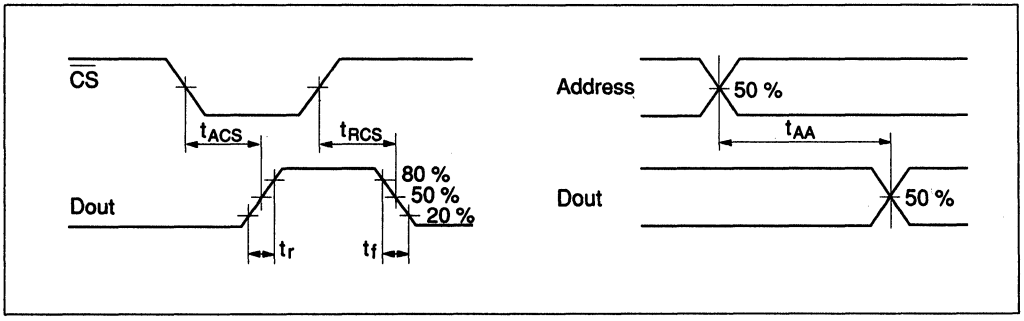
R_L = 50 Ω
C_L = 30 pF
(Includes probe and jig capacitance)

Input Pulse

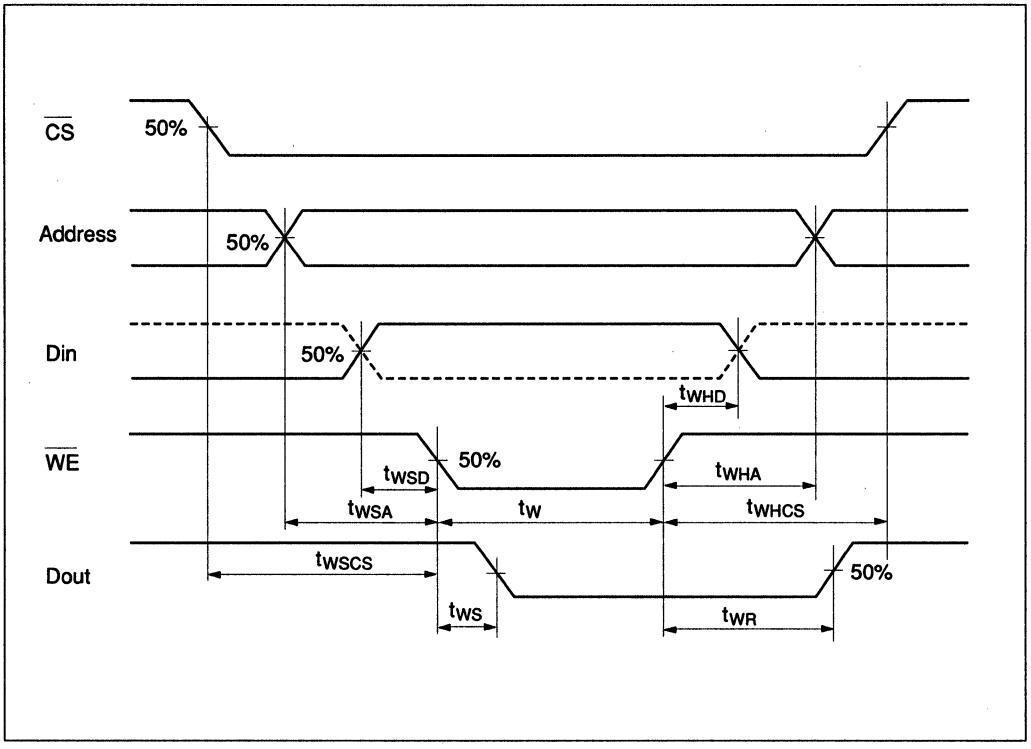


$t_r = t_f$ = 2.0 ns typ

Read Mode



Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101510 Series

1,048,576-word × 1-bit Random Access Memory

The Hitachi HM101510 is ECL 100 K compatible, 1,048,576 words by 1 bits read/write random access memory developed for high speed systems.

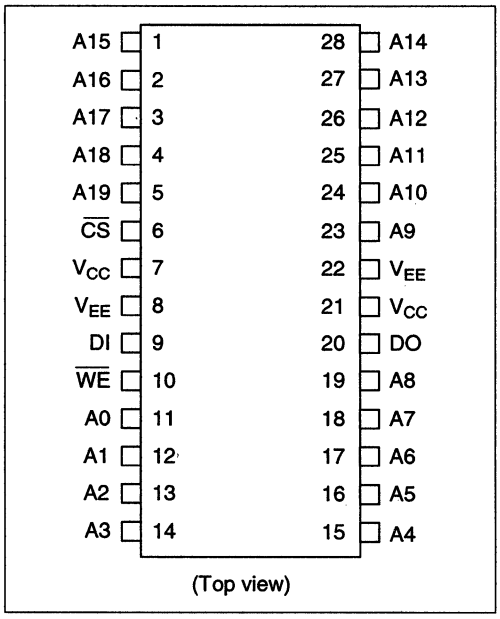
Features

- 1,048,576-words × 1 bit organization
- Fully compatible with 100 K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access Time: 15 ns max
- Write pulse width: 9 ns min
- Low power dissipation: 700 mW typ
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM101510F-15	15 ns	28 pin ceramic flat (30 mil lead pitch) (FG-28DB)

Pin Arrangement



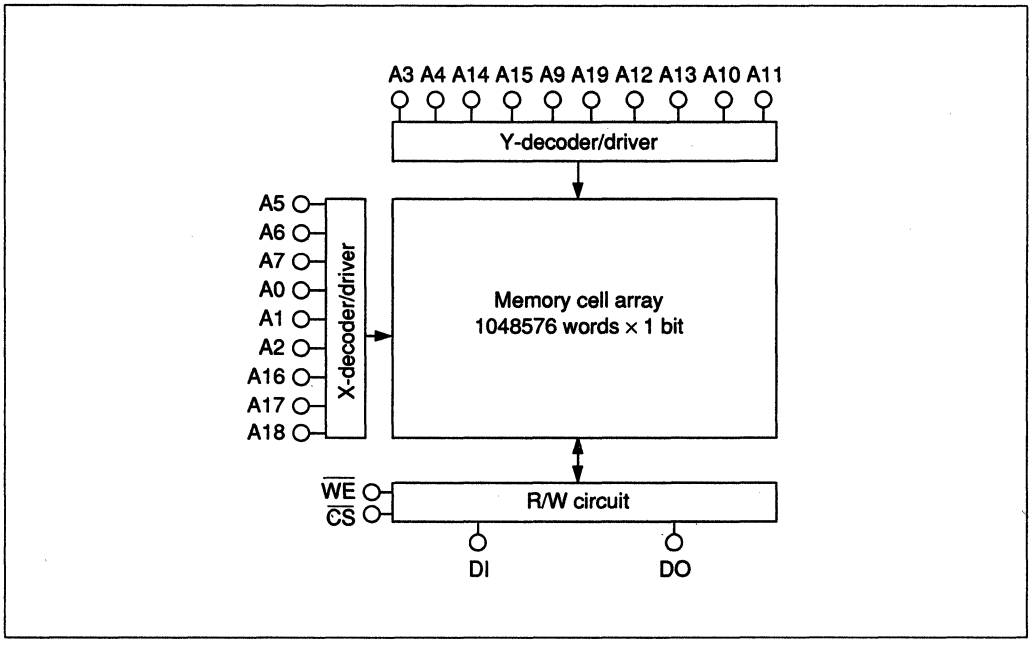
(Top view)

Pin Description

Pin name	Function
A0 – A19	Address input
DI	Data input
DO	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

2

Block Diagram



Function Table

Input				
$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	X*1	X*1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X*1	Dout*2	Read

Notes: 1. Irrelevant
2. Read out noninvert

Absolute Maximum Rating (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0 V min)

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Parameter	Symbol	Min (B)	Typ	Max (A)	Unit	Test condition
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all input
	V_{IL}	–1810	—	–1475	mV	
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		–50	—	—	µA	Others
Supply current	I_{EE}	–180	—	—	mA	All outputs open

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	

Write Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	3	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	

Rise/Fall Time

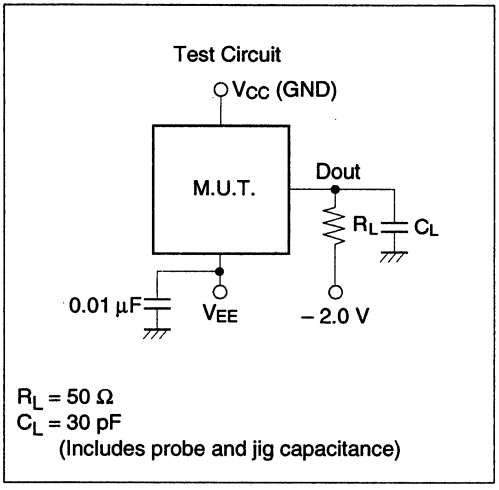
Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

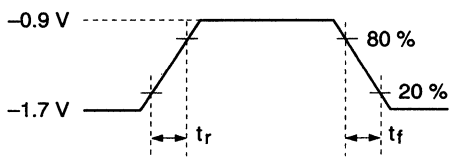
Test Circuit and Waveforms

Loading Condition



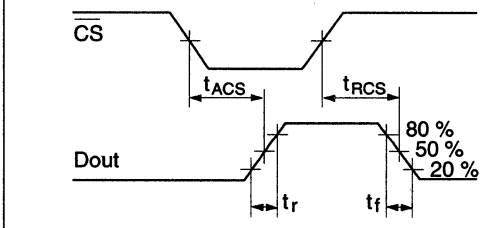
R_L = 50 Ω
C_L = 30 pF
(Includes probe and jig capacitance)

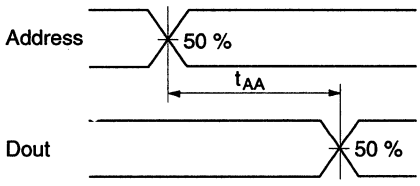
Input Pulse



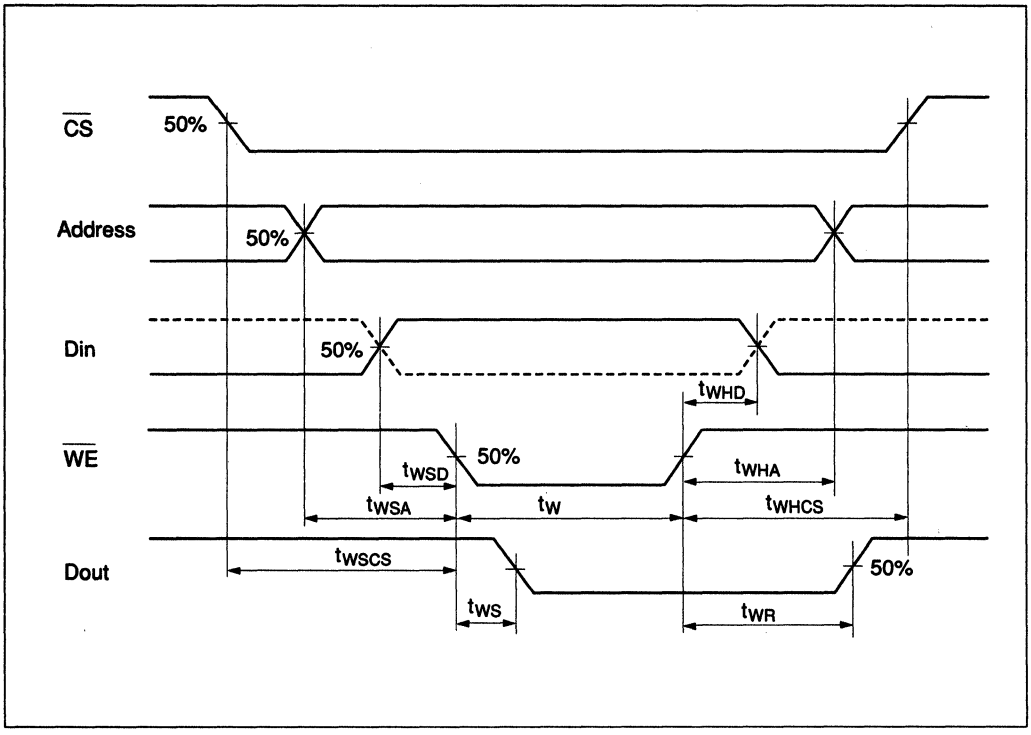
$t_r = t_f$ = 2.0 ns typ

Read Mode





Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101513 Series

262,144-word × 4-bit / 524,288-word × 2-bit Random Access Memory

The Hitachi HM101513 is ECL 100 K compatible, reconfigarable 262,144 words by 4 bits or 524,288 words by 2 bits read/write random access memory developed for high speed systems. With the DI1/MODE pin held at V_{EE}, the organization becomes from 256 k × 4 to 512 k × 2.

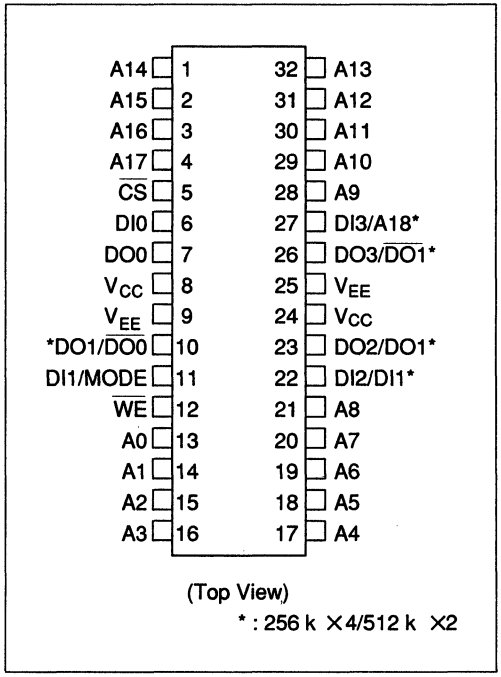
Features

- Reconfigaratible 262,144-words × 4 bit/524,288-words × 2 bit organization
- Fully compatible with 100 K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 15 ns max
- Write pulse width: 9 ns min
- Low power dissipation: 800 mW typ

Ordering Information

Type No.	Access time	Package
HM101513F-15	15 ns	32-pin ceramic flat (30 mil lead pitch)

Pin Arrangement



(Top View)

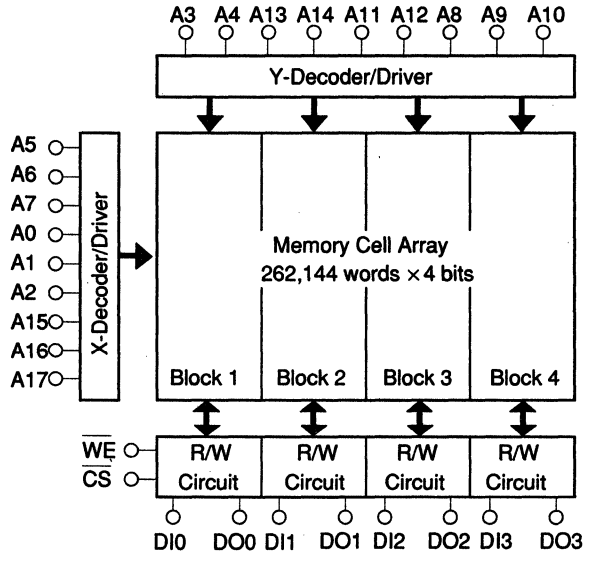
* : 256 k × 4/512 k × 2

Pin Description

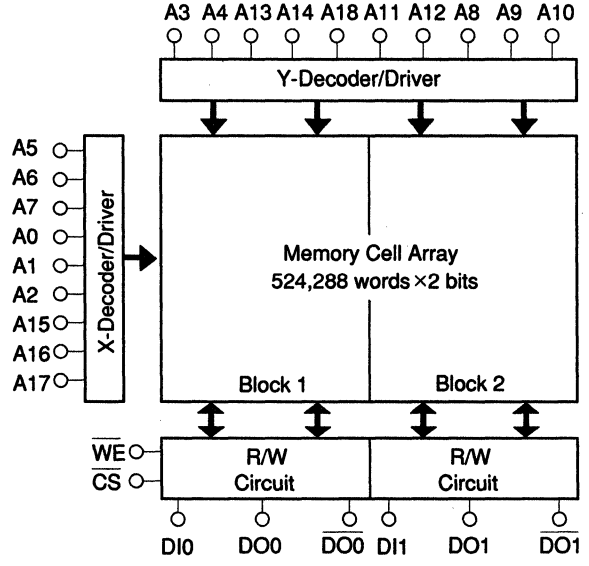
Pin name	Function
A0 – A18	Address input
DI0 – DI3	Data input
DO0 – DO3, $\overline{DO0}$ – $\overline{DO1}$	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage
MODE	Mode select

Block Diagram

• 256 k × 4 Organization



• 512 k × 2 Organization



Function Table

Input

$\overline{CS}$	$\overline{WE}$	Din	Output	$\overline{Output}$	Mode
H	X*1	X*1	L	H	Not selected
L	L	L	L	H	Write "0"
L	L	H	L	H	Write "1"
L	H	X*1	Dout*2	$\overline{Dout}$*3	Read

Notes: 1. Irrelevant.
2. Read out noninvert.
3. Read out invert.

Absolute Maximum Rating (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0 V min).

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Parameter	Symbol	Min (B)	Typ	Max (A)	Unit	Test condition	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–200	—	—	mA	All outputs open	

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	

Write Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	3	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	

Rise/Fall Time

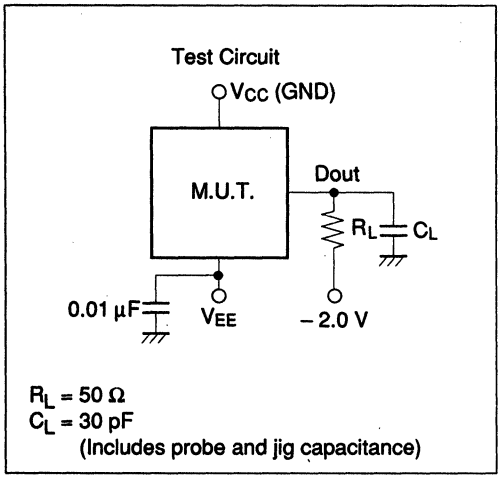
Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

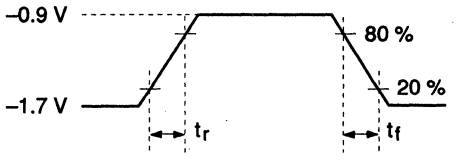
Test Circuit and Waveforms

Loading Condition



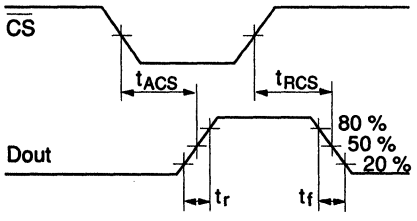
R_L = 50 Ω
C_L = 30 pF
(Includes probe and jig capacitance)

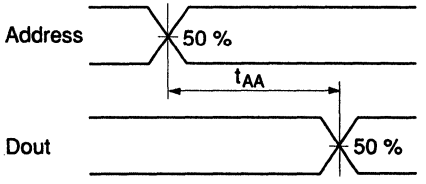
Input Pulse



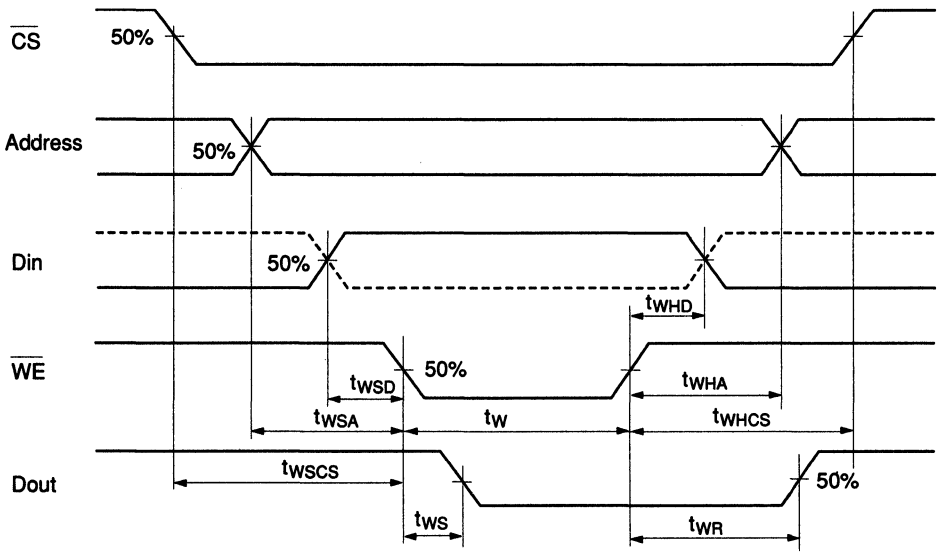
$t_r = t_f$ = 2.0 ns typ

Read Mode





Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101515 Series

262,144-words × 4-bits Fully Decoded Random Access Memory

Description

The HM101515 is ECL 100K compatible, 262,144-word by 4-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

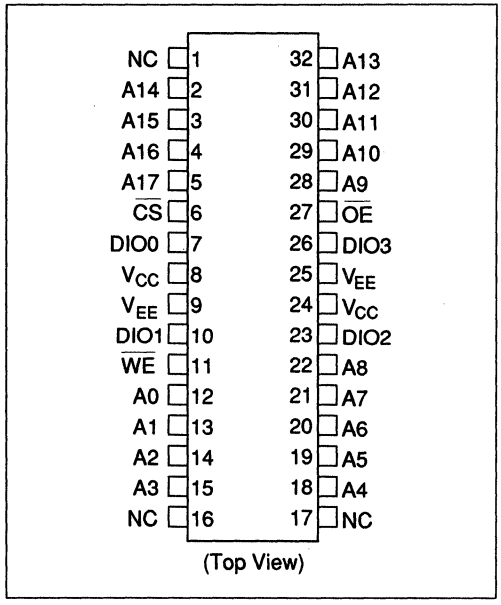
Features

- 262,144 × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 15 ns (max)
- Write pulse width: 9 ns
- Low power dissipation: 800 mW (typ)
- Common I/O

Ordering Information

Type No.	Access time	Package
HM101515F-15	15 ns	32-pin ceramic flat (30-mil lead pitch) (FG-32D)

Pin Arrangement

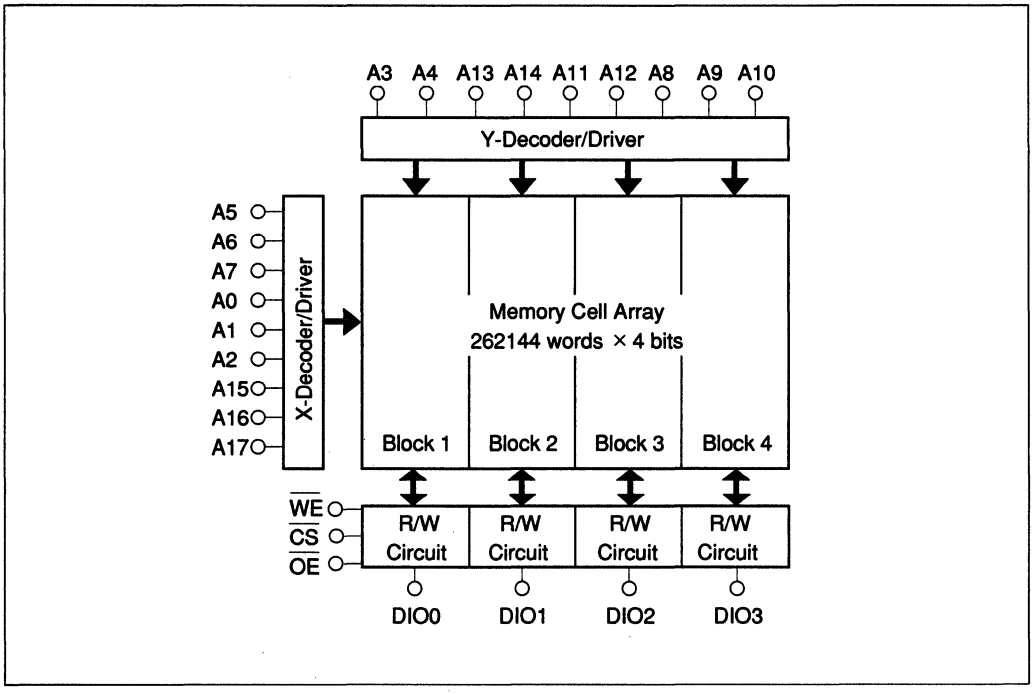


(Top View)

Pin Description

Pin Name	Function
A0–A17	Address input
DI/O0–DI/O3	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{CC}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input			I/O		
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	DI	DO	Mode
H	x	x	x	L	Not selected
L	L	x	L	L	Write 0
L	L	x	H	L	Write 1
L	H	L	L	DI*1	Read
L	H	H	x	L	Output disable

x: Don't care

Note: 1. Write data = Read data

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature (bias)	Tstg (Bias)*1	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0 V min.)

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IH}(max) or V_{IL}(min)	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IH}(min) or V_{IL}(max)	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage high/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IH}(max)	
	I_{IL}	0.5	—	170	µA	Vin = V_{IL}(min)	$\overline{CS}$, $\overline{OE}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–200	—	—	mA	All outputs open	

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	
Output enable access time	t_{AOE}	—	—	10	ns	
Output enable recovery time	t_{ROE}	—	—	10	ns	

Write Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	9	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	
Address setup time	t_{CSA}	3	—	—	ns	$\overline{CS}$ control
Address hold time	t_{CHA}	3	—	—	ns	$\overline{CS}$ control
Write pulse width	t_{CW}	9	—	—	ns	$\overline{CS}$ control

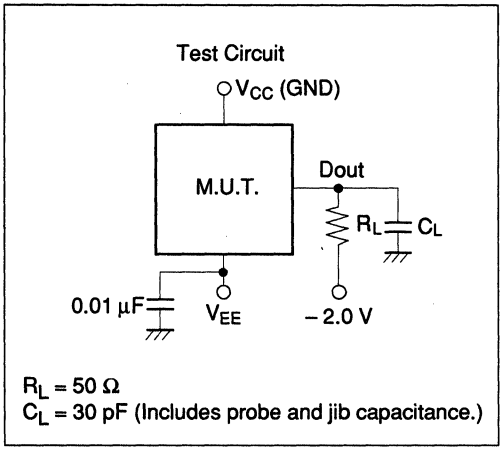
Rise/Fall Time

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

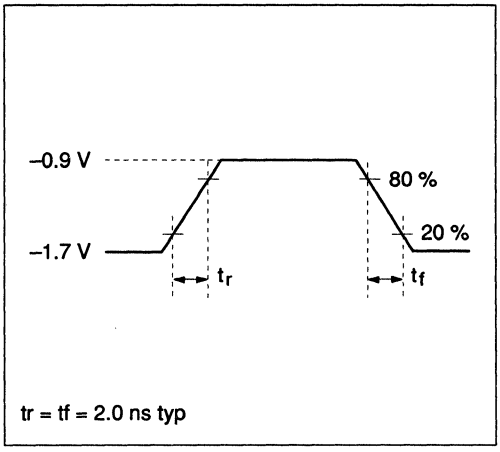
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

AC Test Condition



R_L = 50 Ω
C_L = 30 pF (Includes probe and jib capacitance.)

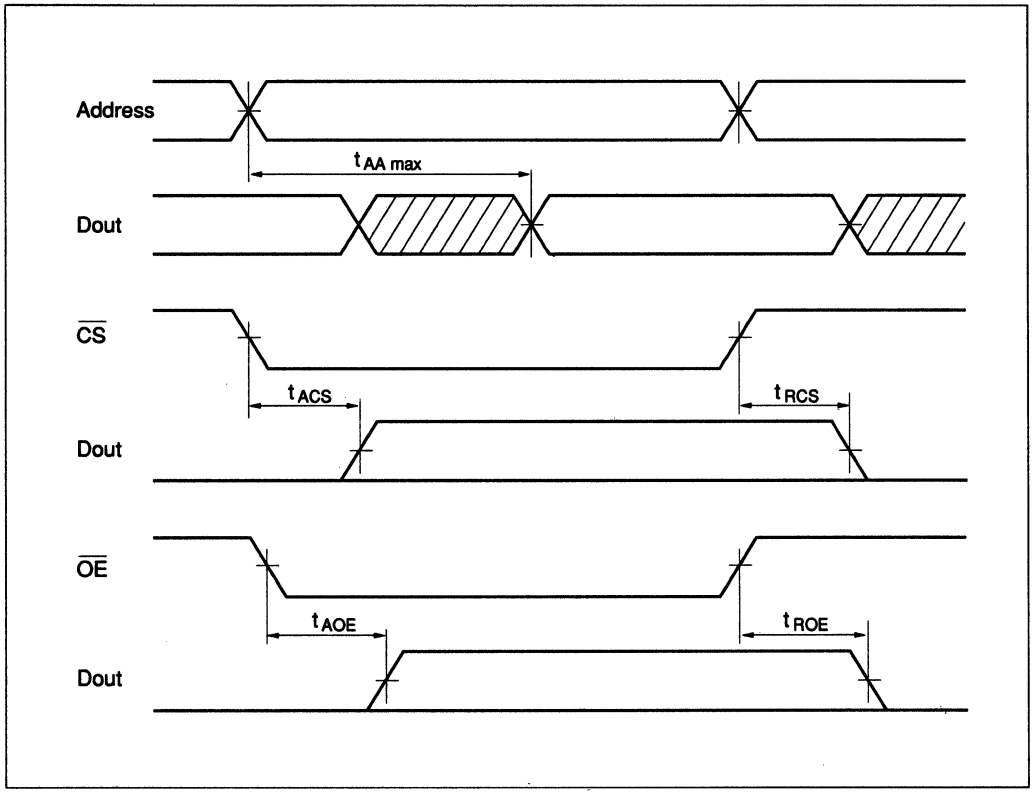
Input Pulse



tr = tf = 2.0 ns typ

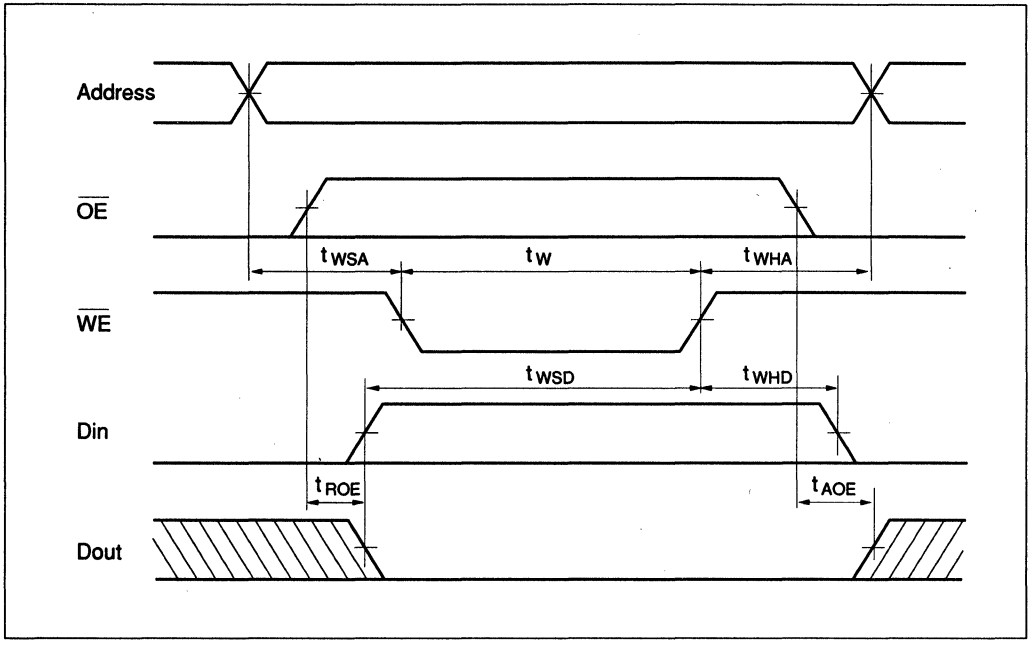
Timing Waveforms

Read Mode

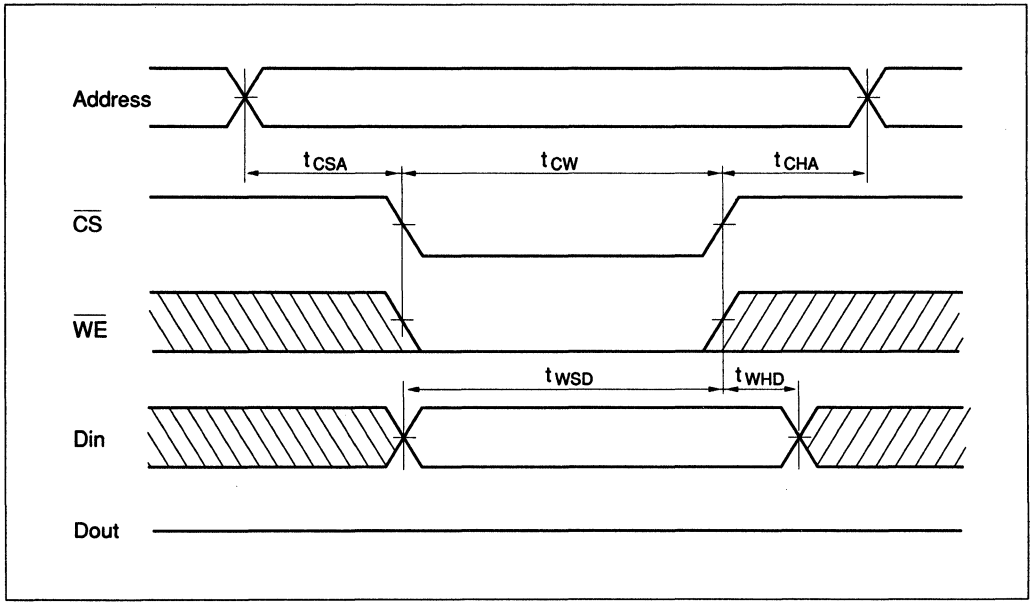


Write Mode

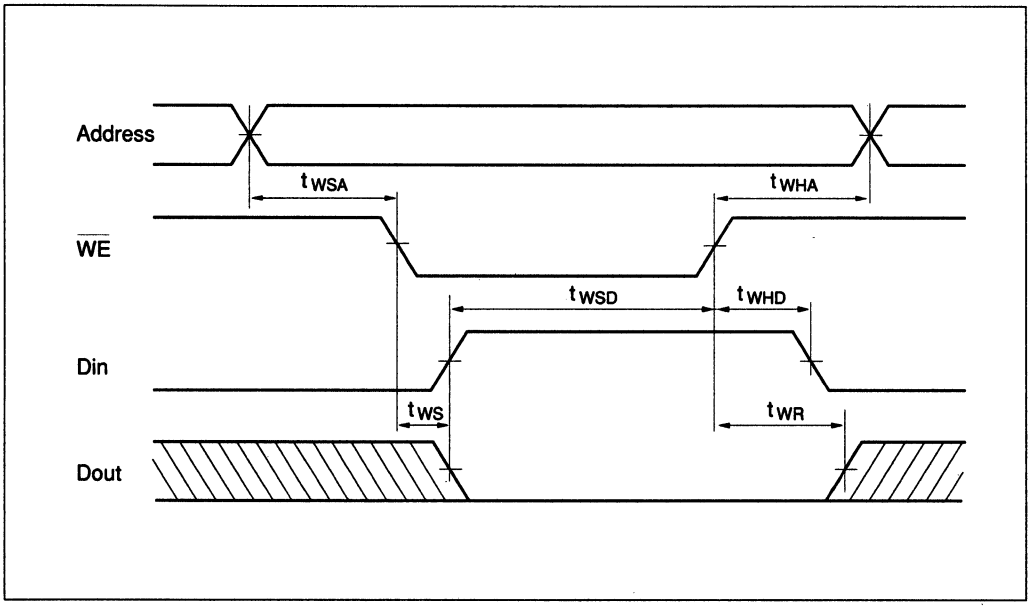
$\overline{OE}$ Control



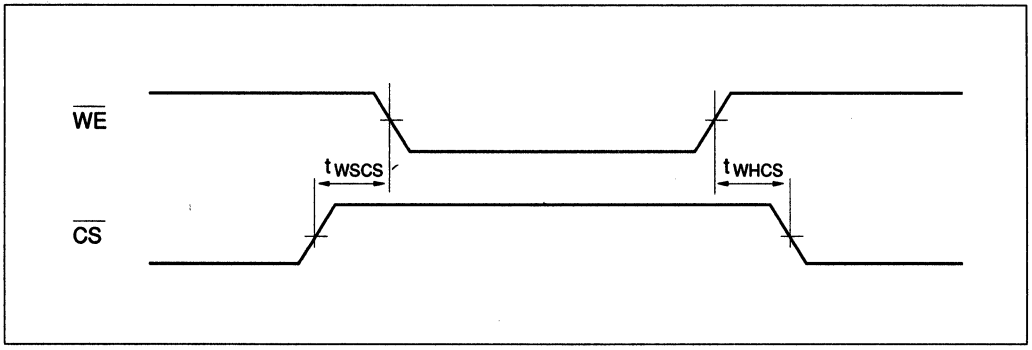
$\overline{CS}$ Control



$\overline{WE}$ Control



Write Disable Mode



1048576-word × 4-bit Random Access Memory

Description

The Hitachi HM101524 is ECL 101k compatible, 1048576 word by 4 bit read/write random access memory developed for high speed systems.

Features

- 1048576-word × 4-bit organization
- Fully compatible with 101k ECL level
- 0.5 μm Hi-BiCMOS process
- Address access Time: 15/18ns max
- Write pulse width: 9/12ns min
- Low power dissipation: 700mW typ
- Output obtainable by wired-OR (open emitter)

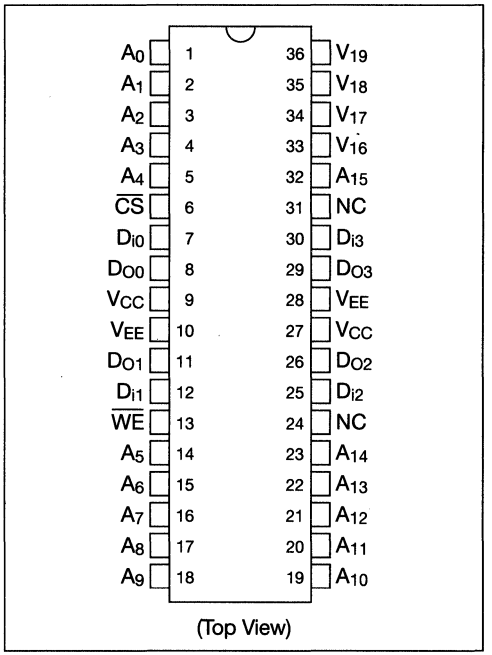
Ordering Information

Type No.	Access time	Package
HM101524JP-15 HM101524JP-18	15 ns 18 ns	400 mil 36 pin Plastic SOJ (50mil lead pitch)
HM101524TT-15 HM101524TT-18	15 ns 18 ns	400 mil 36 pin Plastic TSOP (50mil lead pitch) (TTP-36DA)

Pin Description

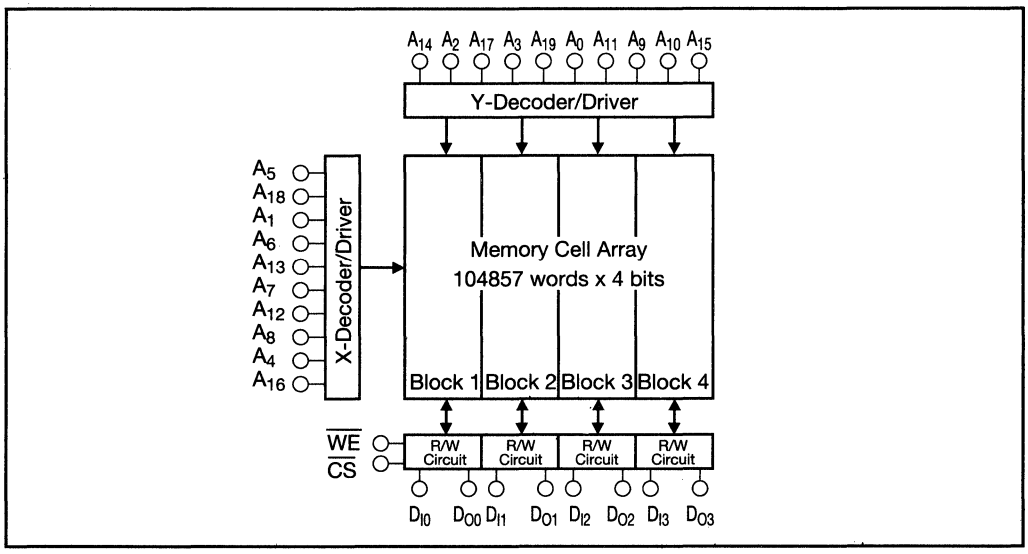
Pin Name	Function
A_0–A_{19}	Address Input
D_{i0}–D_{i3}	Data Input
D_{O0}–D_{03}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

Pin Arrangement



(Top View)

Block Diagram



Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	X[1]	X[1]	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X[1]	Dout[2]	Read

Notes 1) Don't Care 2) Read Out Noninvert

Absolute Maximum Rating (T_j = 125°C max)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}[2]	0 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature	T_{stg}(bias) 1, 2	−10 to +85	°C

Notes 1) Under Bias (V_{EE} = −6.0V min) 2) Case Temperature

Electrical Characteristics

• **DC Characteristics (V_{EE} = –5.2 V ± 5%, R_L = 50Ω to –2.0 V, T_c = 0 to +75°C)**

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	V_{in} = V_{iH} or V_{IL}
	V_{OL}	–1810	–1715	–1620	mV	
Input Voltage	V_{IH}	–1165		–880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	–1810		–1475	mV	
Input Current	I_{IH}			220	µA	V_{in} = V_{iHA}
	I_{IL}	0.5		170	µA	V_{in} = V_{iLS} $\overline{CS}$
		–50			µA	V_{in} = V_{iLS} Others
Supply Current	I_{EE}	–200			mA	Outputs Open 20ns cycle Address Increment Pattern

• **AC Characteristics (V_{EE} = –5.2 V ± 5%, T_c = 0 to +75°C)**

Read Mode

		HM101524-15			HM101524-18				
Item	**Symbol**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Test Condition**
Chip Select Access Time	t_{ACS}	1.5		15	1.5		18	ns	
Chip Select Recovery Time	t_{RCS}	1.5		15	1.5		18	ns	
Address Access Time	t_{AA}	3		15	3		18	ns	

Write Mode

		HM101524-15			HM101524-18				
Item	**Symbol**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Test Condition**
Write Pulse Width	t_W	9			12			ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	0			0			ns	
Data Hold Time	t_{WHD}	1			1			ns	
Address Setup Time	t_{WSA}	1			1			ns	t_W = t_W min
Address Hold Time	t_{WHA}	2			2			ns	
Chip Select Setup Time	t_{WSCS}	0			0			ns	
Chip Select Hold Time	t_{WHCS}	0			0			ns	
Write Disable Time	t_{WS}			15			18	ns	
Write Recovery Time	t_{WR}			17			20	ns	

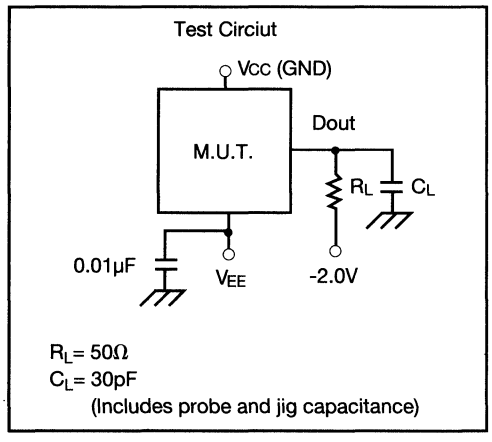
Rise/Fall Time

Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r		2		ns	
Output Fall Time	t_f		2		ns	

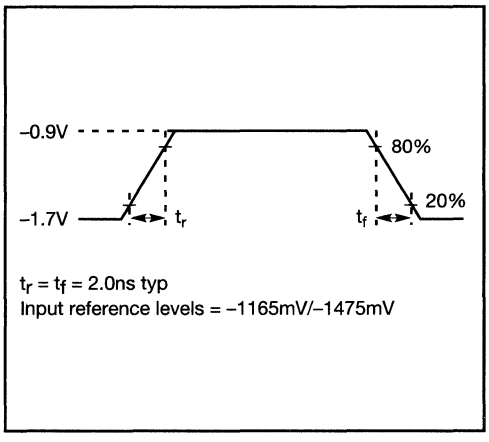
Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	C_{in}		3		pF	
Output Capacitance	C_{out}		5		pF	

AC Test Conditon

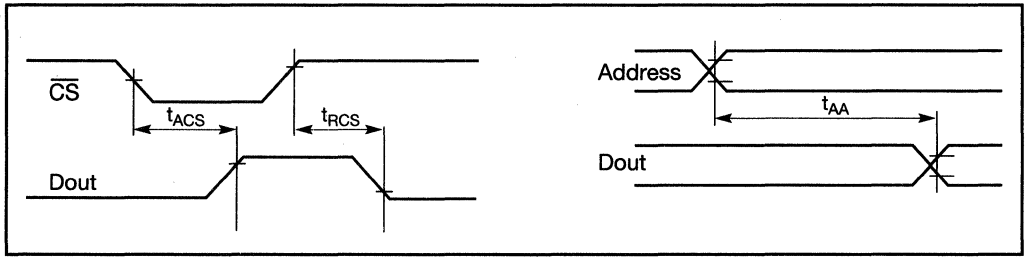


Input Pulse



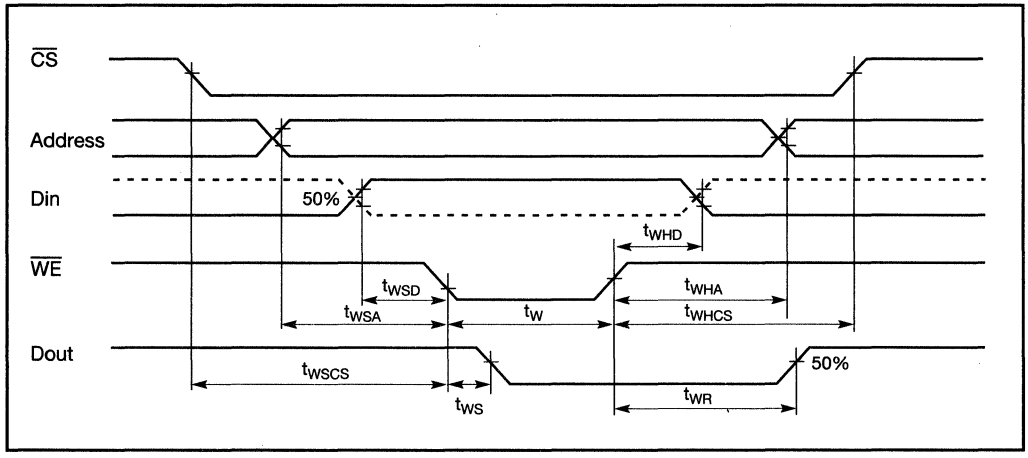
Timing Waveform

Read



Notes: Input and Output Reference Levels = –1165mV/–1475mV

Write



Notes: Input and Output Reference Levels = –1165mV/–1475mV

SECTION 3

CMOS FAST STATIC RAMs

- 5.0 V Supply
- 3.3 V Supply

HM6207H Series

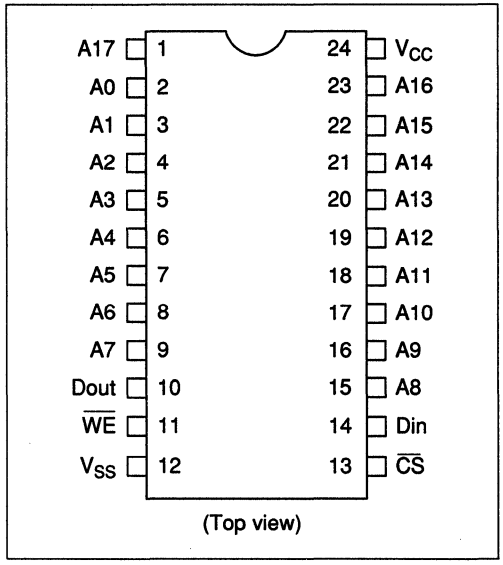
5.0 V Supply

262,144-word × 1-bit High Speed CMOS Static RAM

Features

- Single 5 V supply and high density 24-pin package
- High speed
  Access time: 25/35/45 ns (max)
- Low power
  — Operation: 300 mW (typ)
  — Standby: 100 µW (typ)
  30 µW (typ) (L-version)
- Completely static memory required, no clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible, all inputs and outputs
- Battery back-up operation capability (L-version)

Pin Arrangement



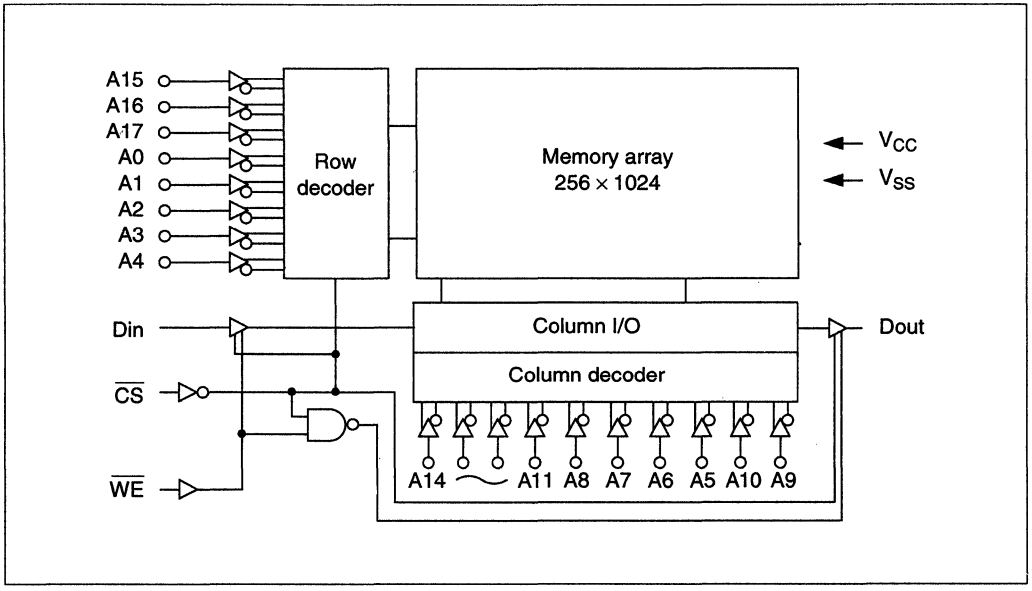
Ordering Information

Type No.	Access time	Package
HM6207HP-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6207HP-35	35 ns	
HM6207HP-45	45 ns	
HM6207HLP-25	25 ns	
HM6207HLP-35	35 ns	
HM6207HLP-45	45 ns	
HM6207HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6207HJP-35	35 ns	
HM6207HJP-45	45 ns	
HM6207HLJP-25	25 ns	
HM6207HLJP-35	35 ns	
HM6207HLJP-45	45 ns	

Pin Description

Pin name	Function
A0–AI7	Address
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



3

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	High-Z	Write cycle

Note: × = Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	Vin	−0.5* to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: Vin min = −2.5 V for pulse width < 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

		HM6207H-25			HM6207H-35/45				
Parameter	**Symbol**	**Min**	**Typ*1**	**Max**	**Min**	**Typ*1**	**Max**	**Unit**	**Test conditions**
Input leakage current	I_{LI}	—	—	2.0	—	—	2.0	µA	V_{CC} = Max, Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	—	—	10.0	—	—	10.0	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	60	120	—	50	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle, duty = 100%
	I_{CC1}	—	40	80	—	40	80	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, t cycle = 50 ns, duty = 100%
Standby power supply current	I_{SB}	—	20	40	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin < 0.2, or Vin ≥ V_{CC} – 0.2 V
	L-Version	—	0.006	0.1	—	0.006	0.1		
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4.0 mA

Note: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)*1

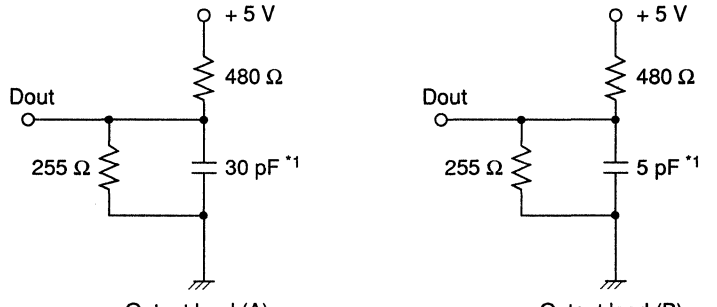
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	Vout = 0 V

Note: 1. This parameter is sampled and is not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10% unless otherwise noted)

AC Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: See figures



Note: 1. Including scope and jig

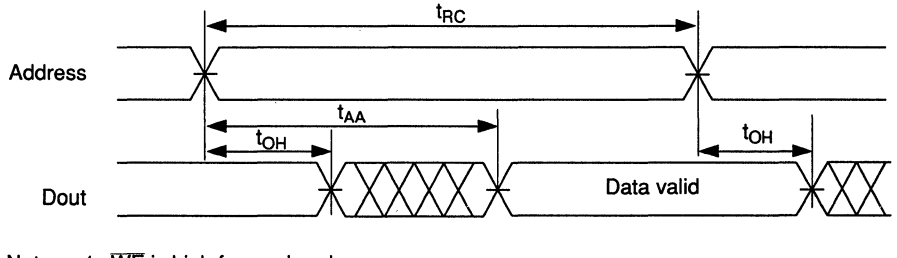
Read Cycle

Parameter	Symbol	HM6207H-25 Min	HM6207H-25 Max	HM6207H-35 Min	HM6207H-35 Max	HM6207H-45 Min	HM6207H-45 Max	Unit
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	tPD	—	15	—	25	—	30	ns

Note: 1. Transition is measured ± 200 mV from steady-state voltage with Load (B).
These parameters are sampled and not 100% tested.

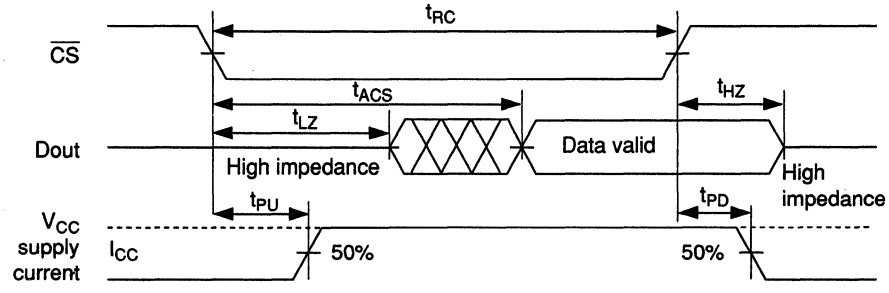
3

Read Timing Waveform (1)



Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

Read Timing Waveform (2)



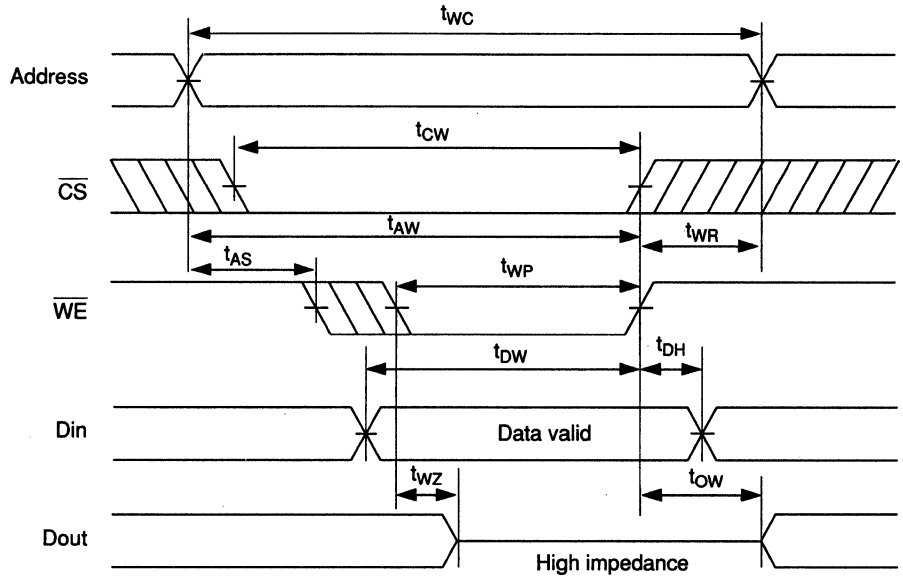
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to coincident with $\overline{CS}$ transition low.

Write Cycle

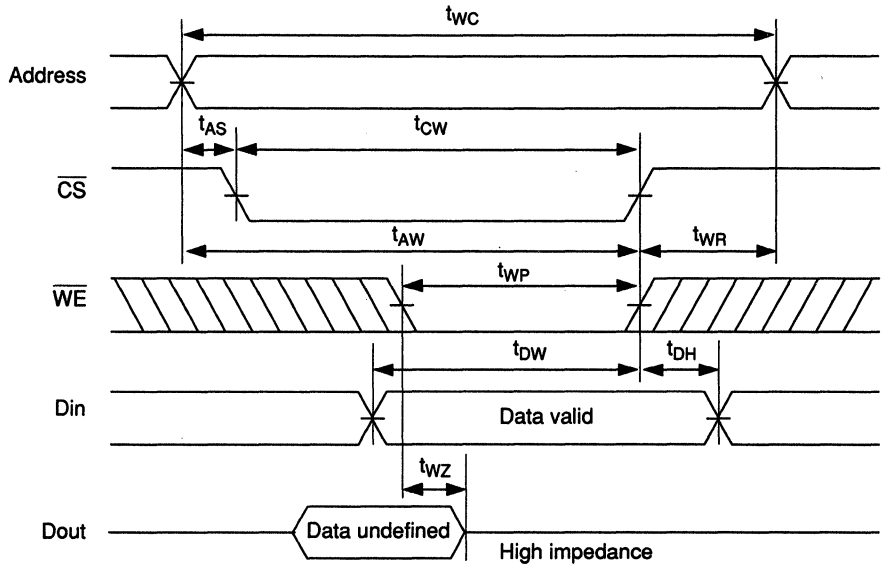
		HM6207H-25		HM6207H-35		HM6207H-45		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	40	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	25	—	ns
Write recovery time	t_{WR}	3	—	3	—	3	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ} *1	0	15	0	20	0	25	ns
Output active from end of write	t_{OW} *1	0	—	0	—	0	—	ns

Note: 1. Transition is measured ± 200 mV from high-impedance voltage with Load (B).
This parameter is sampled and is not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
3. If the CS low transition occurs simultaneously with the WE low transition, the output buffers remain in a high impedence state.
4. Dout has the same phase as write data in this write cycle, if t_{WR} is long enough.

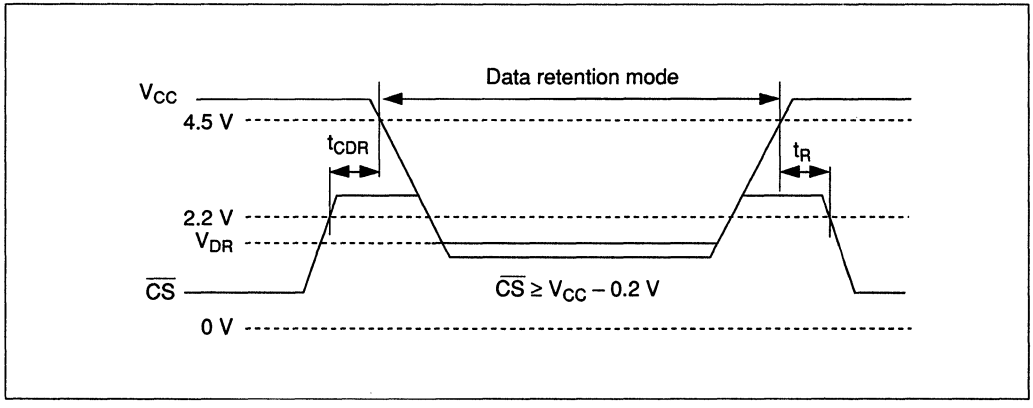
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

These characteristics are guaranteed for the L-version only.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V, or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



3

HM6208H Series

65,536-word × 4-bit High Speed CMOS Static RAM

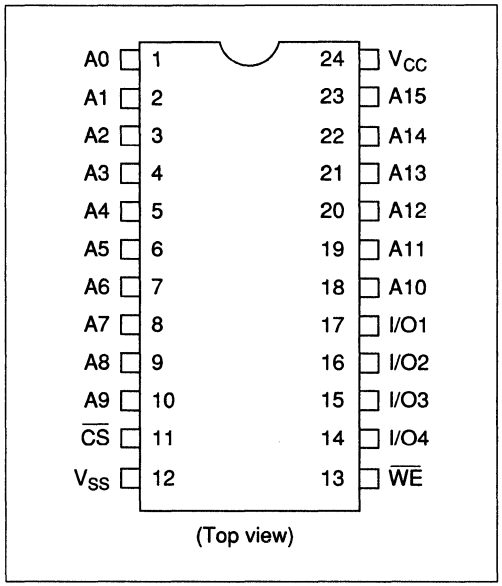
Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max)
- Low power
  - — Operation: 300 mW (typ)
  - — Standby: 100 µW (typ)
    30 µW (typ) (L-version)
- Completely static memory required
  - — No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs
- Battery back up operation capability (L-version)

Ordering Information

Type No.	Access time	Package
HM6208HP-25	25 ns	300-mil, 24-pin plastic DIP (DP-24NC)
HM6208HP-35	35 ns	
HM6208HP-45	45 ns	
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208HLP-45	45 ns	
HM6208HJP-25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HJP-45	45 ns	
HM6208HLJP-25	25 ns	
HM6208HLJP-35	35 ns	
HM6208HLJP-45	45 ns	

Pin Arrangement



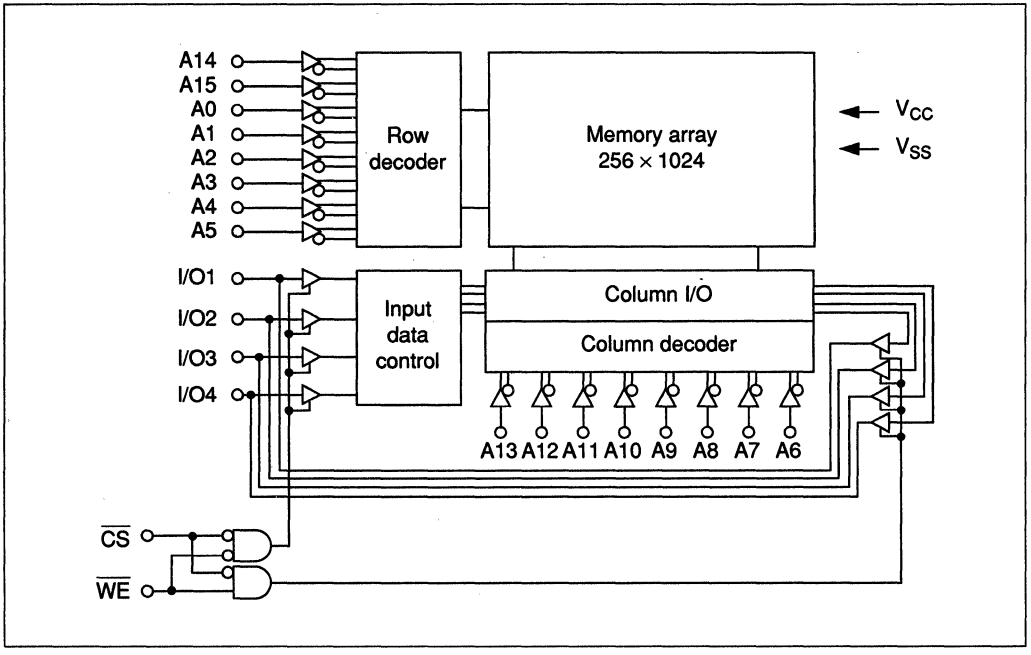
(Top view)

Pin Description

Pin name	Function
A0–A15	Address
I/O1–I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

3

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	Din	Write cycle

Note: × = Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5* to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: Vin min = –2.5 V for pulse widths ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*	—	0.8	V

Note: V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM6208H-25			HM6208H-35/45				
Parameter	**Symbol**	**Min**	**Typ*2**	**Max**	**Min**	**Typ*2**	**Max**	**Unit**	**Test conditions**
Input leakage current	I_{LI}	—	—	2.0	—	—	2.0	µA	V_{CC} = Max Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	—	—	10.0	—	—	10.0	µA	$\overline{CS}$ = V_{IH}, V_{IO} = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	60	120	—	50	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle, duty = 100%
	I_{CC1}	—	40	80	—	40	80	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, t cycle = 50 ns, duty = 100%
Standby power supply current	I_{SB}	—	20	40	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin < 0.2 V, or Vin ≥ V_{CC} – 0.2 V
		—	0.006	0.1	—	0.006	0.1*1		
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: 1. L version
2. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	11	pF	$V_{I/O}$ = 0 V

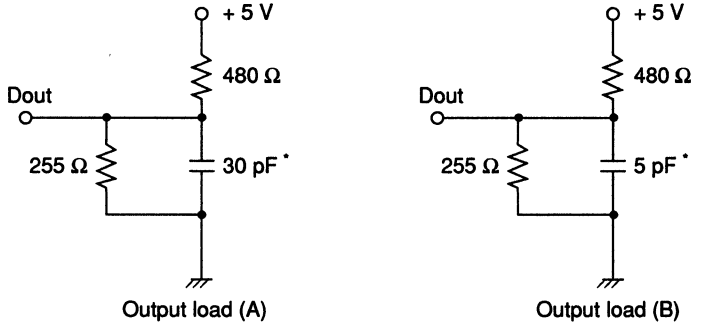
Note: These parameters are sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted)

AC Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figure

Output Load



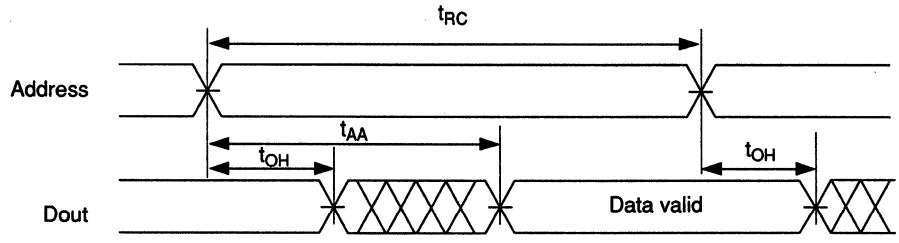
Note: Including scope and jig

Read Cycle

Parameter	Symbol	HM6208H-25 Min	HM6208H-25 Max	HM6208H-35 Min	HM6208H-35 Max	HM6208H-45 Min	HM6208H-45 Max	Unit
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*	0	15	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	25	—	30	ns

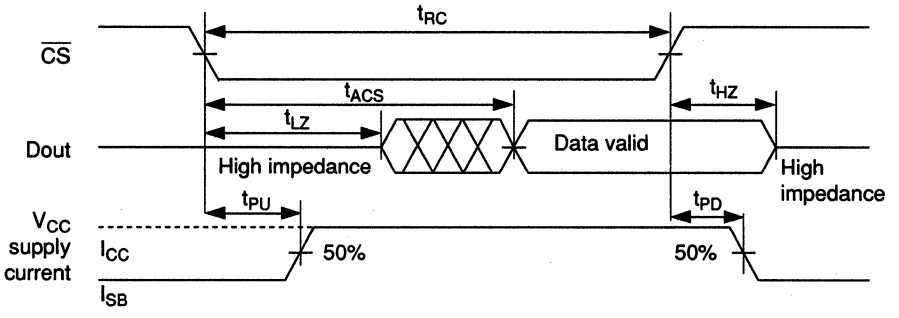
Note: Transition is measured ±200 mV from steady state voltage with load (B).
These parameters are sampled and not 100% tested.

Read Timing Waveform (1)



Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected.

Read Timing Waveform (2)



Notes: 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with the $\overline{CS}$ transition to low.

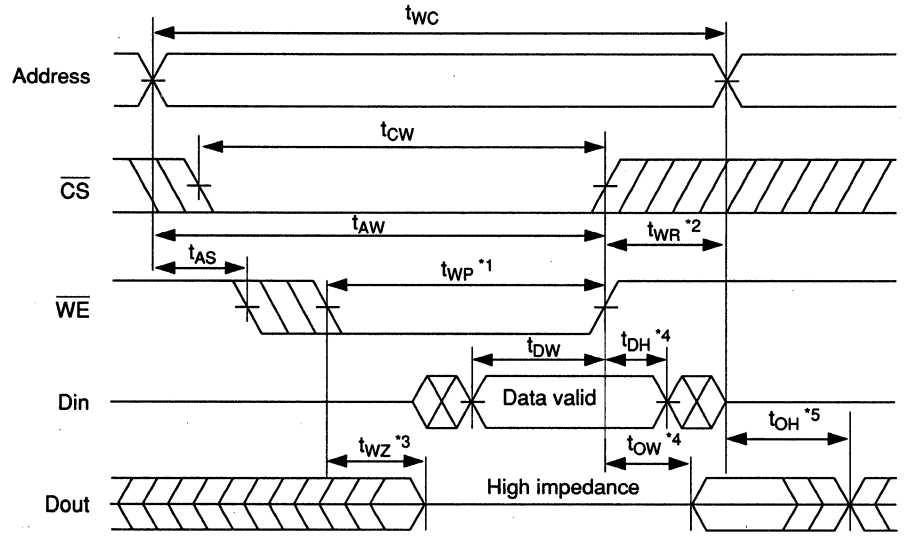
Write Cycle

Parameter	Symbol	HM6208H-25 Min	HM6208H-25 Max	HM6208H-35 Min	HM6208H-35 Max	HM6208H-45 Min	HM6208H-45 Max	Unit
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	40	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Write recovery time	t_{WR}	3	—	3	—	3	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}^*	0	8	0	10	0	15	ns
Output active from end of write	t_{OW}^*	0	—	0	—	0	—	ns

Note: Transition is measured ±200 mV from high impedance voltage with load (B).
These parameters are sampled and not 100% tested.

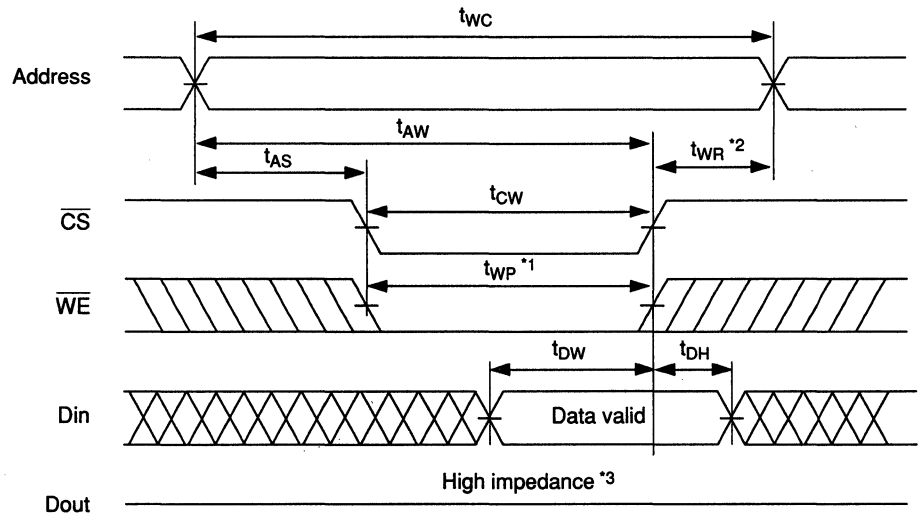
3

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
3. During this period, I/O pins are in the output state. The input signals of the opposite phase to the outputs must not be applied.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to them.
5. Dout is the same phase of write data of this write cycle.

Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high-impedance state.

3

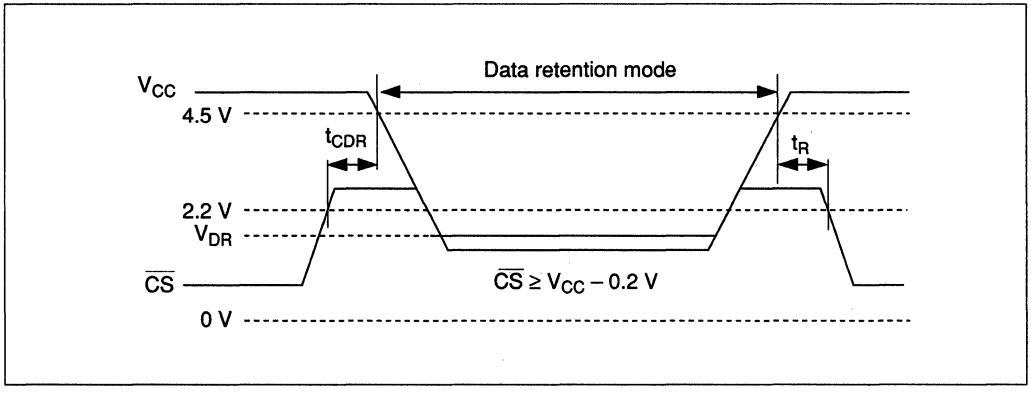
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

These characteristics are guaranteed for the L-version only.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V, or 0 V $\leq$ Vin < 0.2 V, or
Data retention current	I_{CCDR}	—	2	50*	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



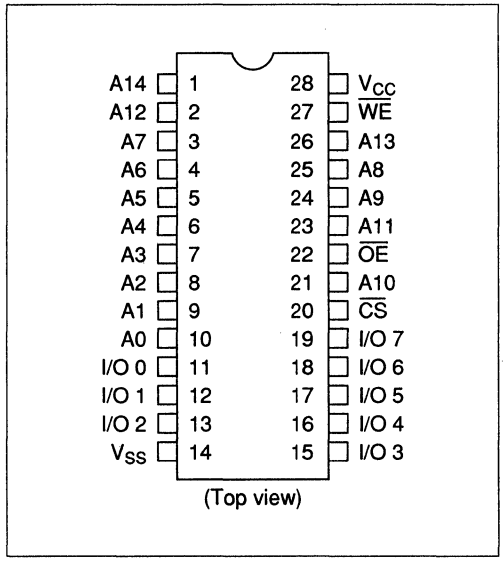
HM62832H Series

32768-Word × 8-Bit High Speed CMOS Static RAM

Features

- High speed: Fast access time 25/35/45 ns (max)
- Low power
  Active: 300 mW (typ)
  Standby: 10 µW (typ) (L-version)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output – Three state output
- Directly TTL compatible – All inputs and outputs

Pin Arrangement



Ordering Information

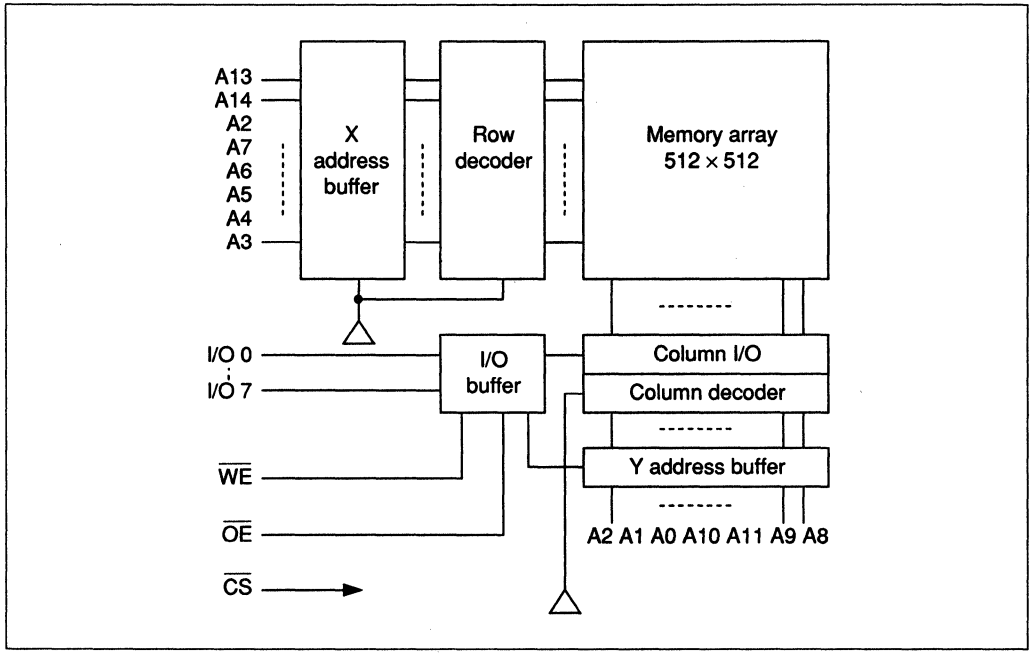
Type No.	Access time	Package
HM62832HP-25	25 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832HP-35	35 ns	
HM62832HP-45	45 ns	
HM62832HLP-25	25 ns	
HM62832HLP-35	35 ns	
HM62832HLP-45	45 ns	
HM62832HJP-25	25 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832HJP-35	35 ns	
HM62832HJP-45	45 ns	
HM62832HLJP-25	25 ns	
HM62832HLJP-35	35 ns	
HM62832HLJP-45	45 ns	

Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

3

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −2.5 V for pulse width ≤ 10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L		I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5 *1	—	0.8	V

Note: 1. −2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current	I_{CC}	—	60	120	mA	Min cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby power supply current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
Standby power supply current	I_{SB1}	—	0.02	2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} − 0.2 V	
		—	0.002	0.1	mA		L-version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)

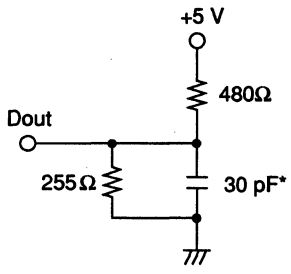
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

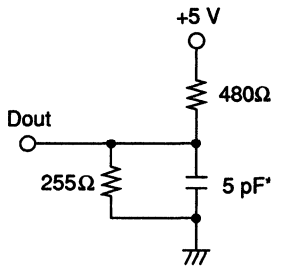
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig

Read Cycle

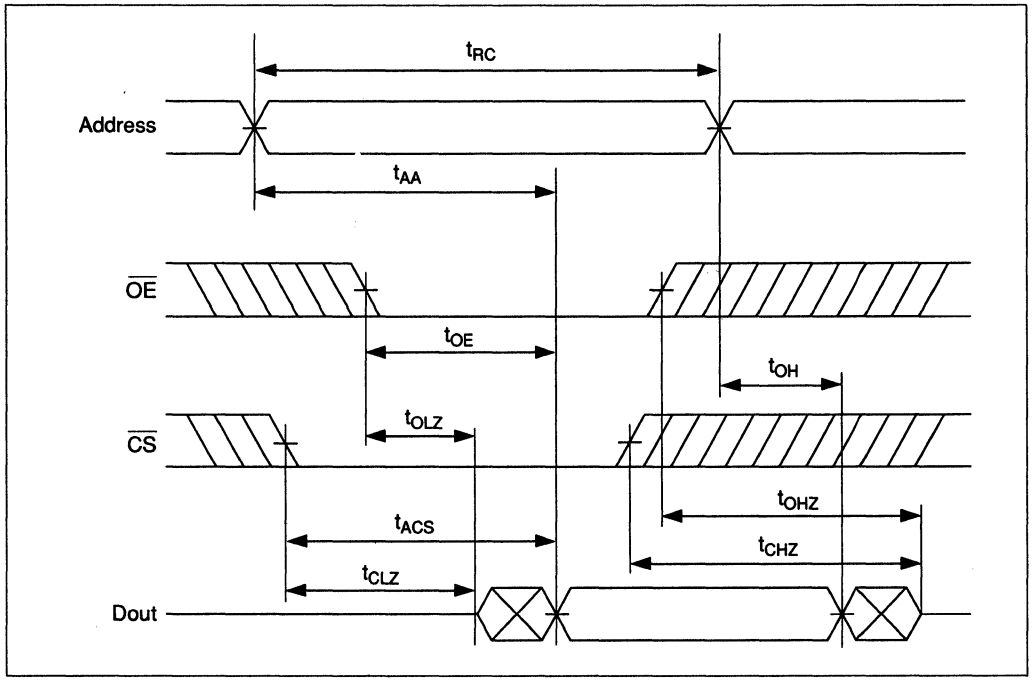
		HM62832H-25		HM62832H-35		HM62832H-45		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output enable to output valid	t_{OE}	—	12	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{CLZ}	5	—	5	—	5	—	ns
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}	0	12	0	15	0	20	ns
Output enable to output in high-Z	t_{OHZ}	0	12	0	15	0	20	ns

Write Cycle

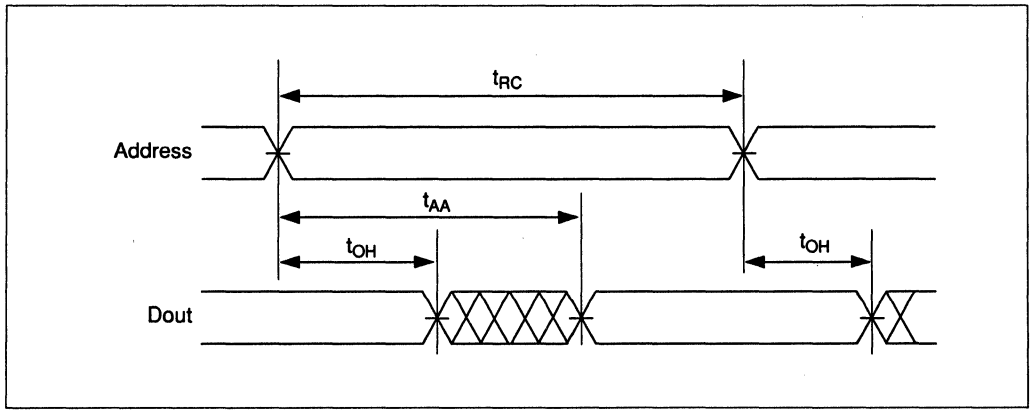
		HM62832H-25		HM62832H-35		HM62832H-45		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	15	—	20	—	25	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	20	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Write to output in high-Z	t_{WHZ}	0	12	0	15	0	20	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output disable to output in high-Z	t_{OHZ}	0	12	0	15	0	20	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns

Timing Waveforms

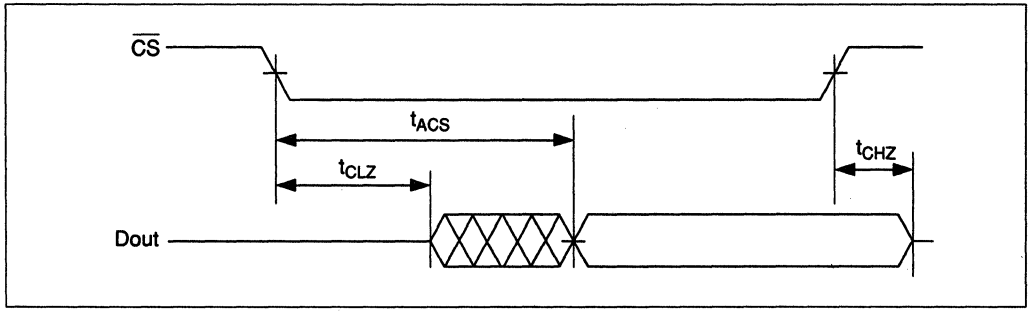
Read Cycle Timing–1*1, *2



Read Cycle Timing–2*2, *3, *5

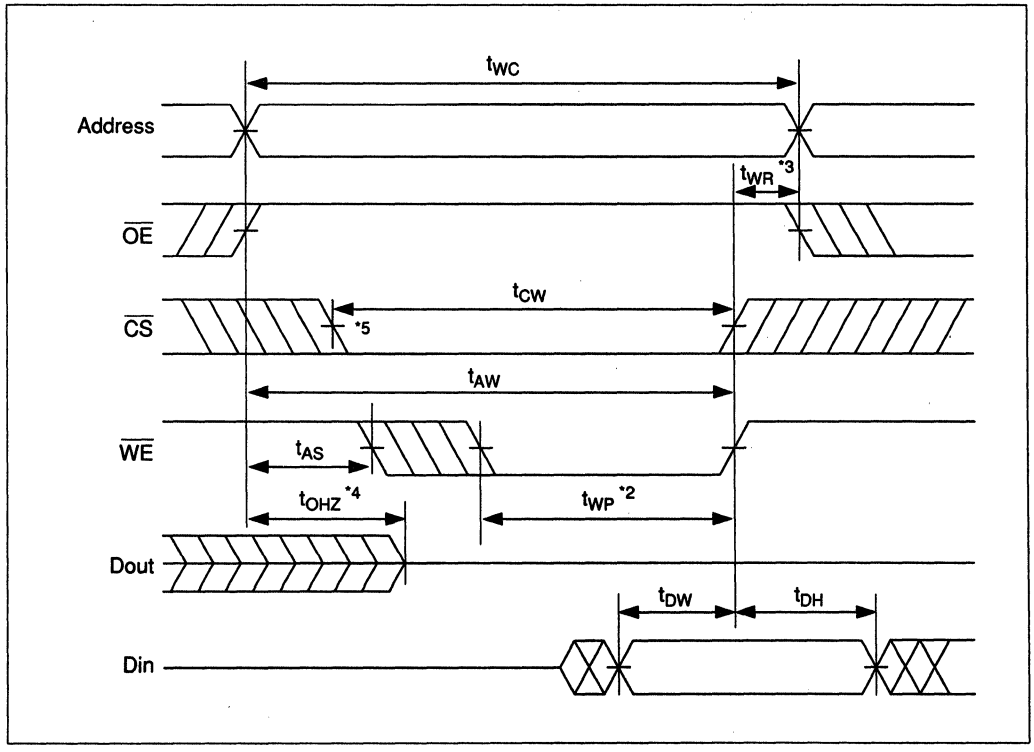


Read Cycle Timing–3*1, *2, *4, *5

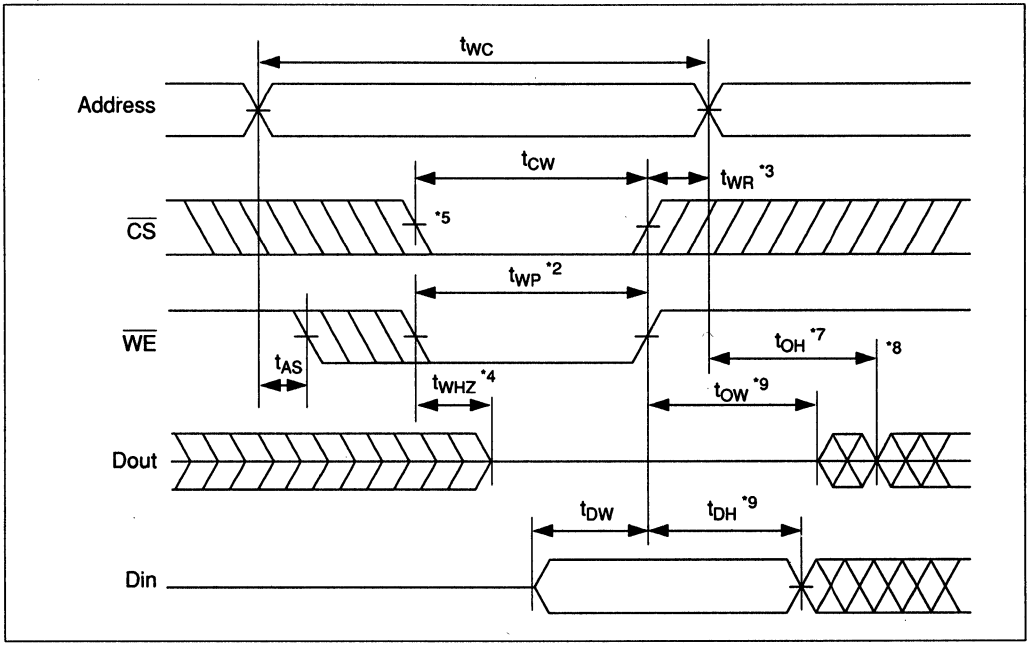


Notes: 1. Transition is measured ±200 mV from steady state voltage with load (B).
This parameter is sampled and not 100% tested.
2. WE is high for read cycle.
3. Device is continuously selected, CS = V_{IL}.
4. Address should be valid prior to or coincident with CS transition low.
5. OE = V_{IL}

Write Cycle Timing–1*10



Write Cycle Timing–2*6, *10



Notes: 1. Transition is measured ±200 mV from high impedance voltage with load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the ealier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. Dout is in the same phase of written data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.
10. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

3

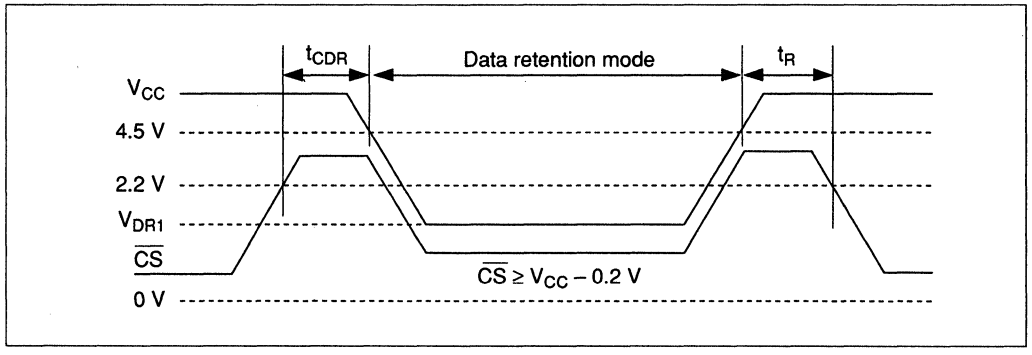
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

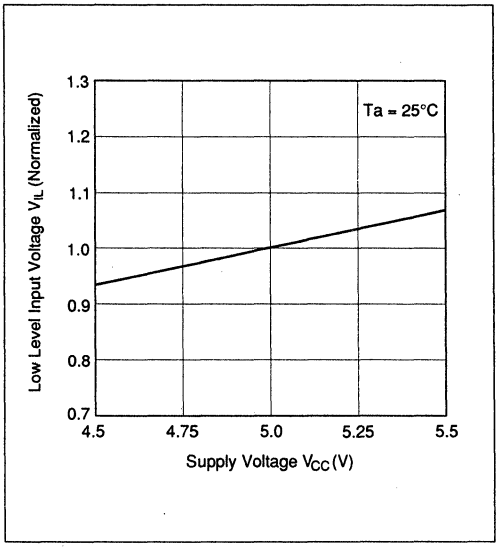
This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V $\leq$ Vin $\leq$ 0.2 V
Data retention current	I_{CCDR}	—	1	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

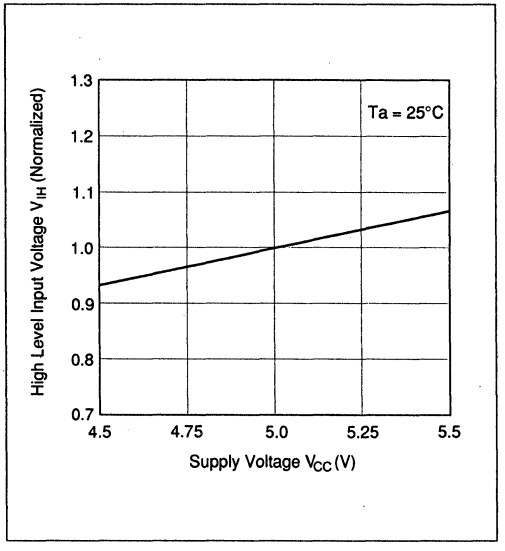
Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform

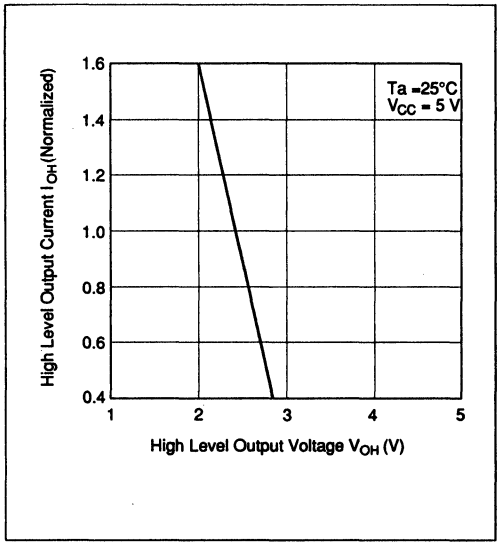




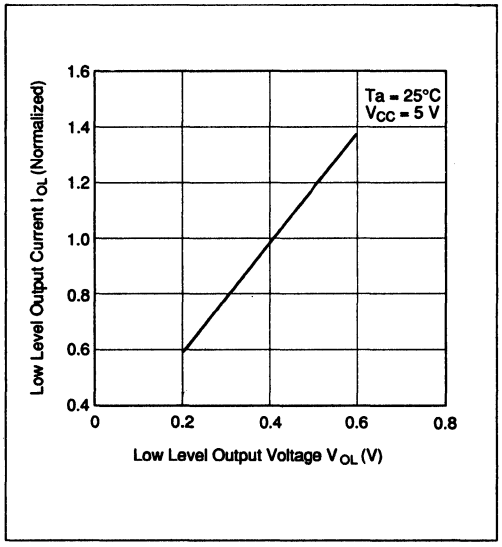
Low Level Input Voltage vs. Supply Voltage



High Level Input Voltage vs. Supply Voltage

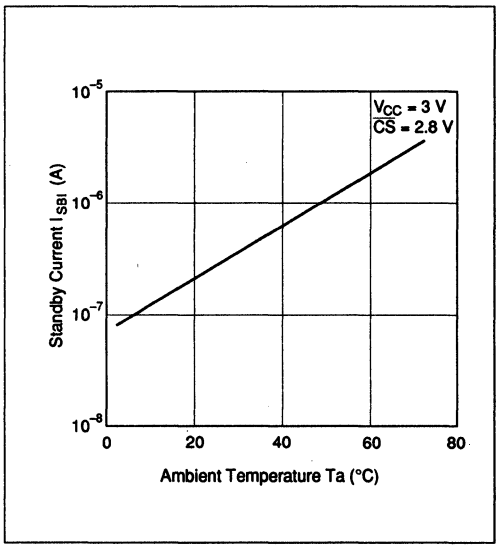


High Level Output Current vs. High Level Output Voltage

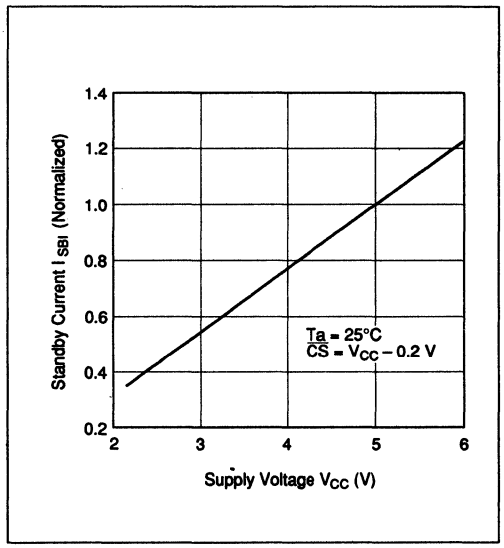


Low Level Output Current vs. Low Level Output Voltage

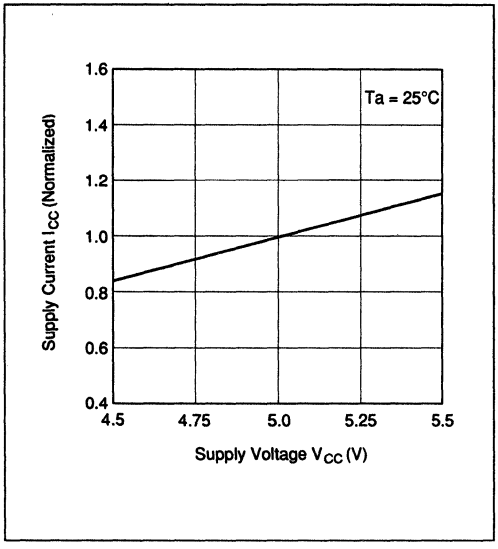
3



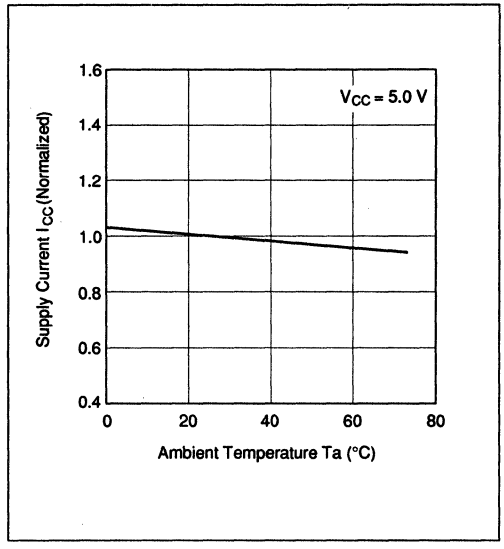
Standby Current vs. Ambient Temperature



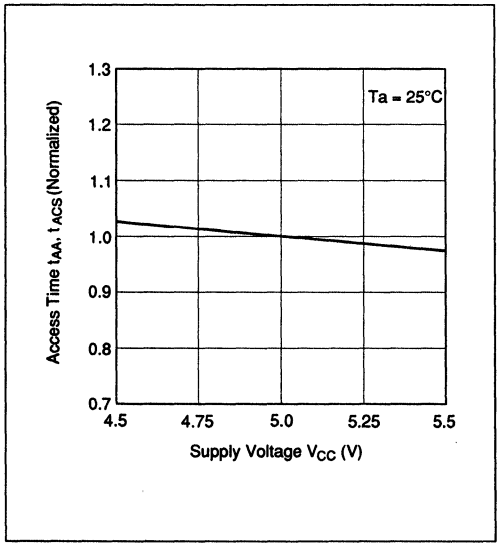
Standby Current vs. Supply Voltage



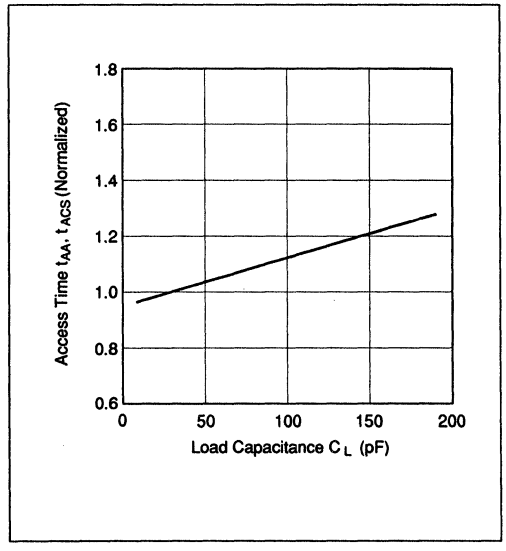
Supply Current vs. Supply Voltage



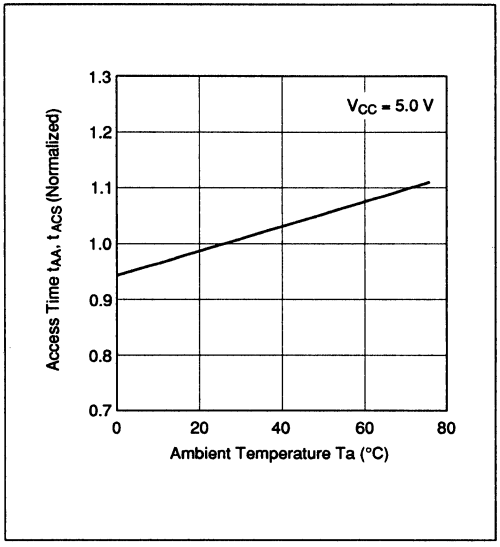
Supply Current vs. Ambient Temperature



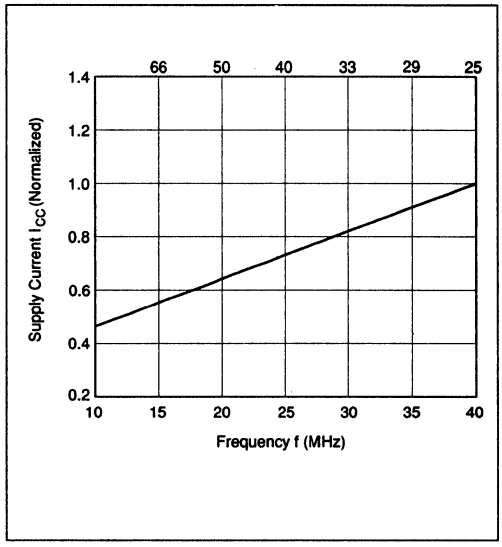
Access Time vs. Supply Voltage



Access Time vs. Load Capacitance



Access Time vs. Ambient Temperature



Supply Current vs. Frequency

3

HM62832UH Series

32768-word × 8-bit High Speed CMOS Static RAM

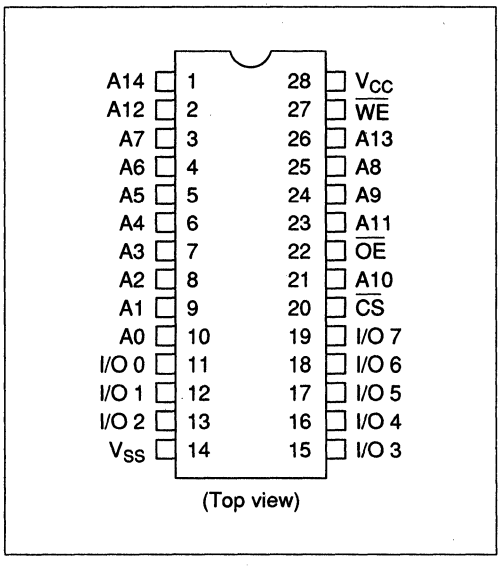
Features

- High speed: Fast access time 15/20 ns (max)
- Low Power
  Standby: 15 µW (typ) (L-version)
  Operation: 675/600 mW (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM62832UHP-15	15 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832UHP-20	20 ns	
HM62832UHLP-15	15 ns	
HM62832UHLP-20	20 ns	
HM62832UHJP-15	15 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832UHJP-20	20 ns	
HM62832UHLJP-15	15 ns	
HM62832UHLJP-20	20 ns	

Pin Arrangement

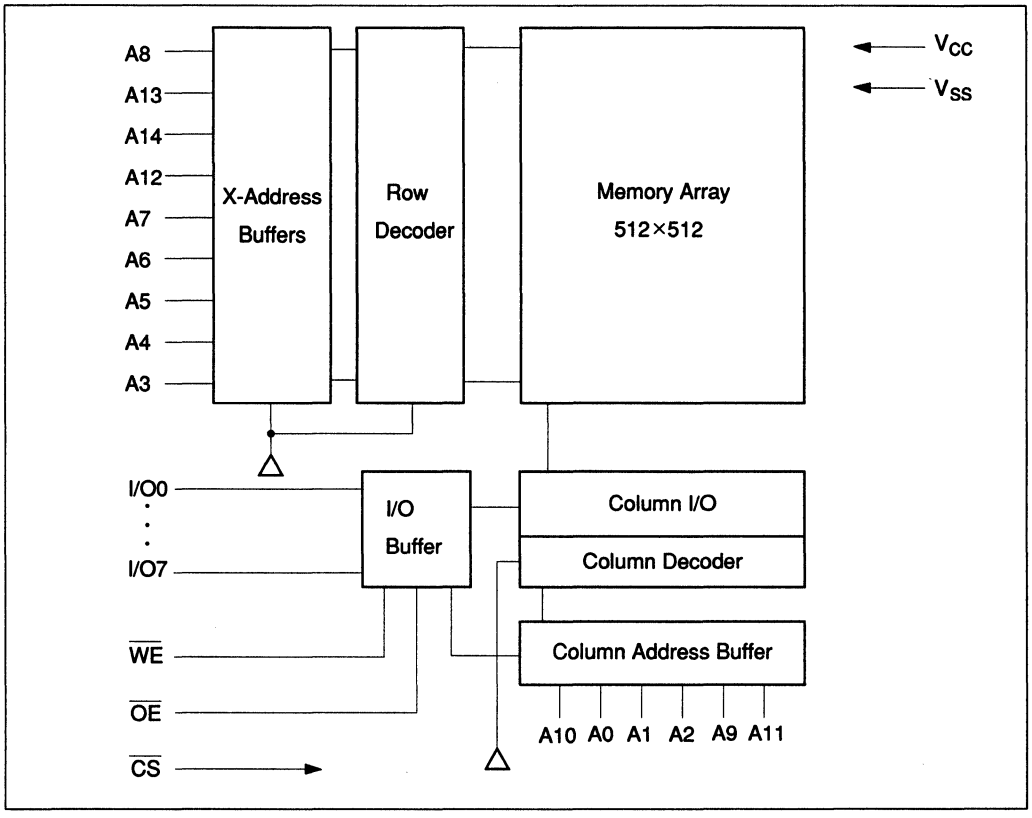


(Top view)

Pin Description

Symbol	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle 1, 2, 3
L	H	L	Write	I_{CC}	Din	Write cycle 1
L	L	L	Write	I_{CC}	Din	Write cycle 2

Note: X : H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	−0.5*2 to +7.0	V
Voltage on any pin relative to V_{SS}*1	V_T	−0.5*2 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. With respect to V_{SS}
2. V_{CC} and V_T min = −2.5 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse with ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} current	I_{CC1} (-15) *3	—	135	170	mA	min cycle *2
	I_{CC2} (-15)	—	100	120	mA	2x min cycle
	I_{CC1} (-20)	—	120	150	mA	min cycle
	I_{CC2} (-20)	—	90	110	mA	2x min cycle
Standby V_{CC} current	I_{SB} (-15)	—	40	60	mA	$\overline{CS}$ = V_{IH}, min cycle
	I_{SB} (-20)	—	30	50		
Standby V_{CC} current (1)	I_{SB1} (L-version)	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ Vin ≤ 0.2 V or V_{CC} – 0.2 V ≤ Vin
		—	0.003	0.1		
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, Ta = 25°C and specified loading.
2. $\overline{CS}$ = V_{IL}, Iout = 0 mA
3. Access time version

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

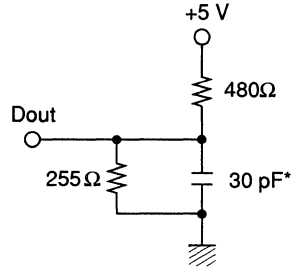
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

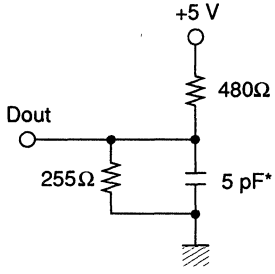
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 4 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



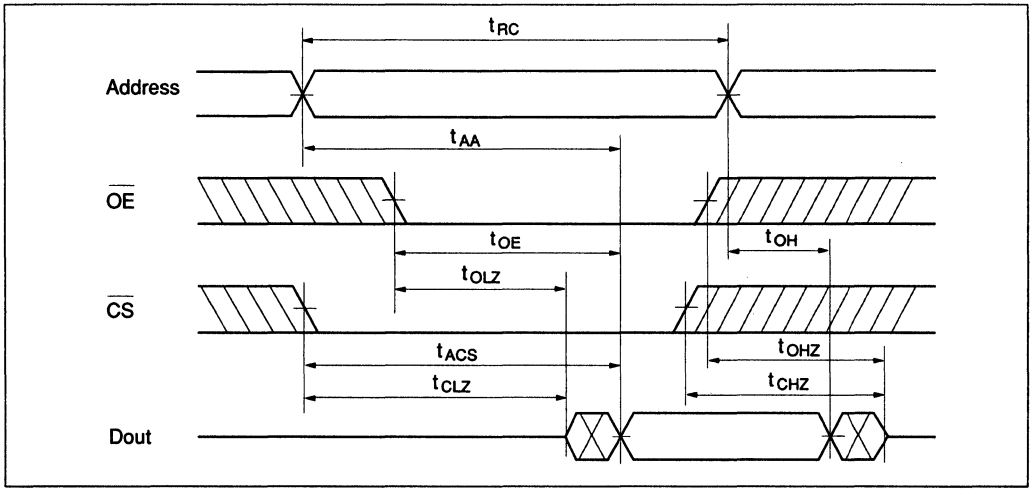
Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig

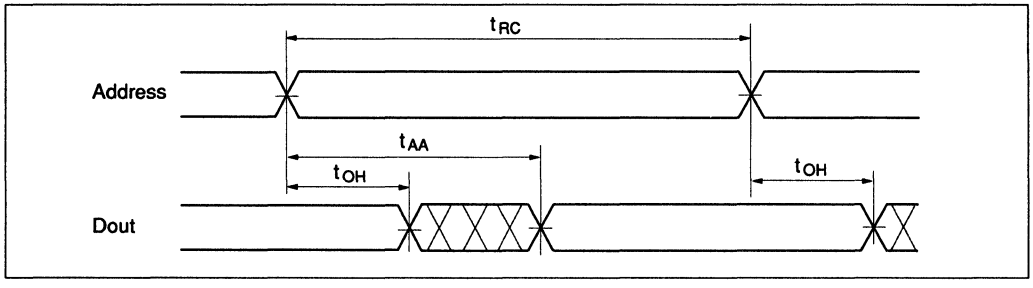
Read Cycle

		HM62832UH-15		HM62832UH-20		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip select access time	t_{ACS}	—	15	—	20	ns
Chip selection to output in low-Z	t_{CLZ}*1	3	—	3	—	ns
Output enable to output valid	t_{OE}	—	8	—	10	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	7	0	10	ns
Chip disable to output in high-Z	t_{OHZ}*1	0	7	0	10	ns
Output hold from address change	t_{OH}	3	—	3	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	20	ns

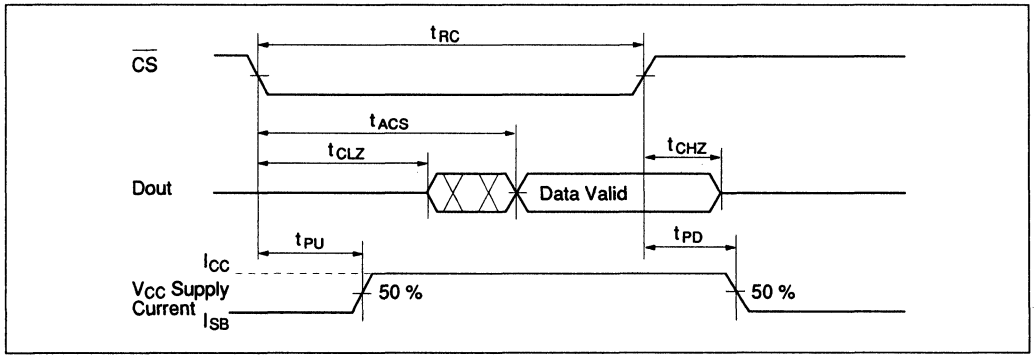
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *2, *3, *5



Read Timing Waveform (3) *1, *2 *4, *5

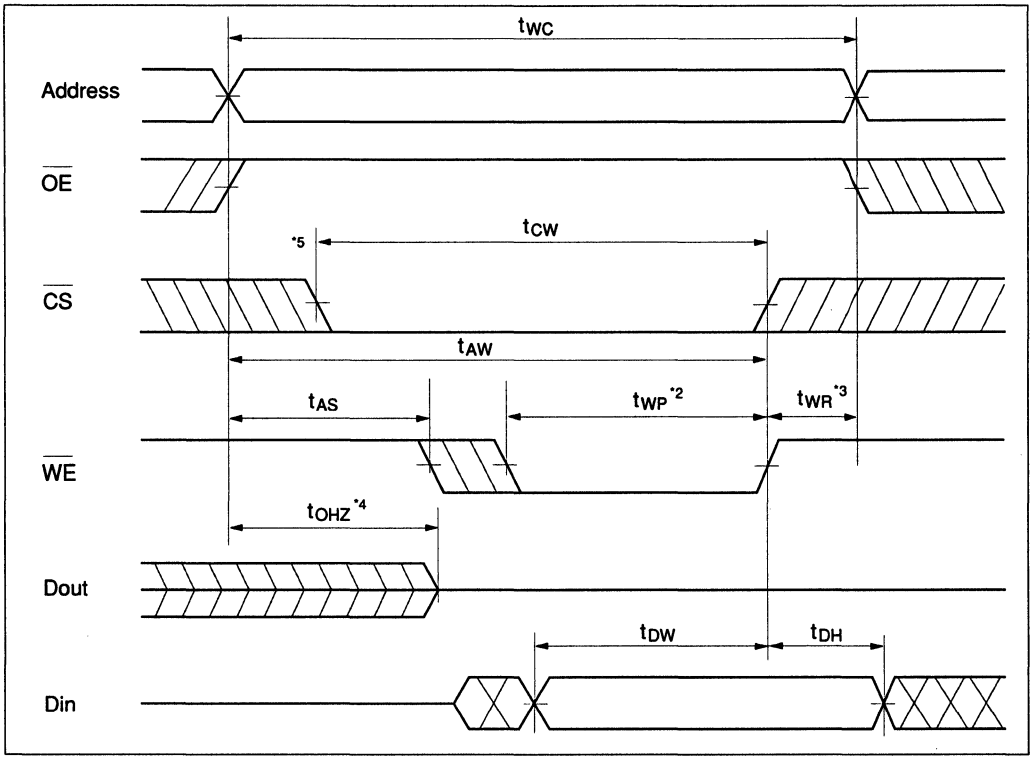


Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE} = V_{IL}$

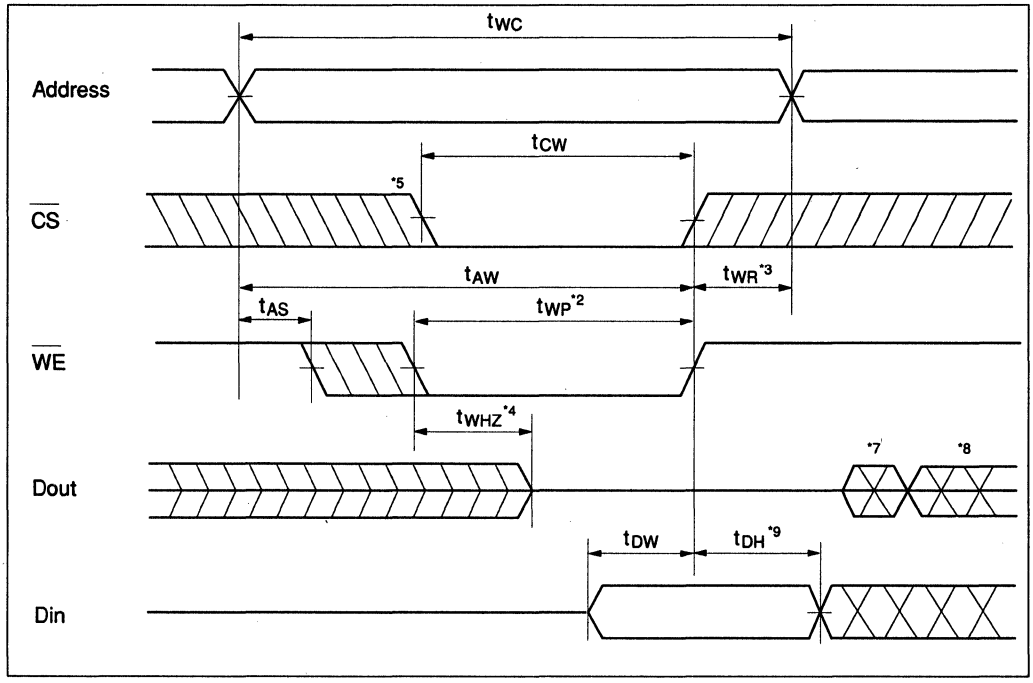
Write Cycle

Parameter	Symbol	HM62832UH-15		HM62832UH-20		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	15	—	20	—	ns
Chip selection to end of write	t_{CW}	10	—	12	—	ns
Address valid to end of write	t_{AW}	13	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	12	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	7	0	10	ns
Write to output in high-Z*1	t_{WHZ}	0	7	0	10	ns
Data to write time overlap	t_{DW}	8	—	10	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write*1	t_{OW}	3	—	3	—	ns

Write Timing Waveform (1)



Write Timing Waveform (2) *6



Notes:
1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$)
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. $\overline{WE}$ must be high during all address transition except when device is disable with $\overline{CS}$.

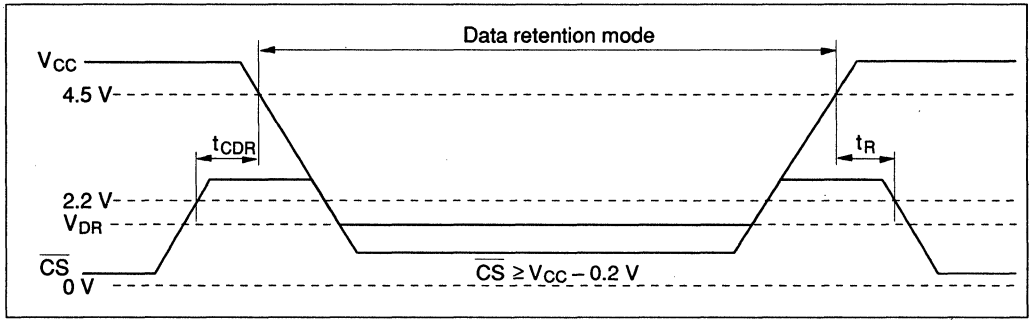
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2V$, Vin ≥ V_{CC} – 0.2 V or 0 V < Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



HM621100A Series

1048576-word × 1-bit High Speed CMOS Static RAM

The Hitachi HM621100A is a high speed 1M Static RAM organized as 1048576-word × 1-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM621100A, packaged in a 400-mil plastic SOJ is available for high density mounting.

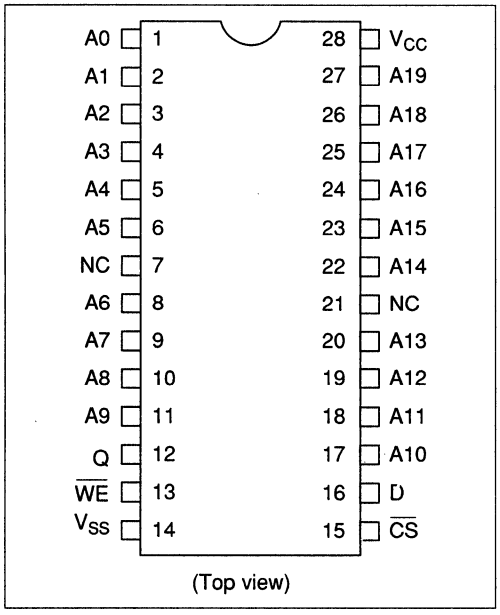
Features

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed
  Access time: 20/25/35 ns (max)
- Low power dissipation
  Active mode: 350 mW (typ)
  Standby mode: 100 µW (typ)
- Completely static memory required
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM621100AP-20	20 ns	400-mil 28-pin plastic DIP (DP-28C)
HM621100AP-25	25 ns	
HM621100AP-35	35 ns	
HM621100ALP-20	20 ns	
HM621100ALP-25	25 ns	
HM621100ALP-35	35 ns	
HM621100AJP-20	20 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM621100AJP-25	25 ns	
HM621100AJP-35	35 ns	
HM621100ALJP-20	20 ns	
HM621100ALJP-25	25 ns	
HM621100ALJP-35	35 ns	

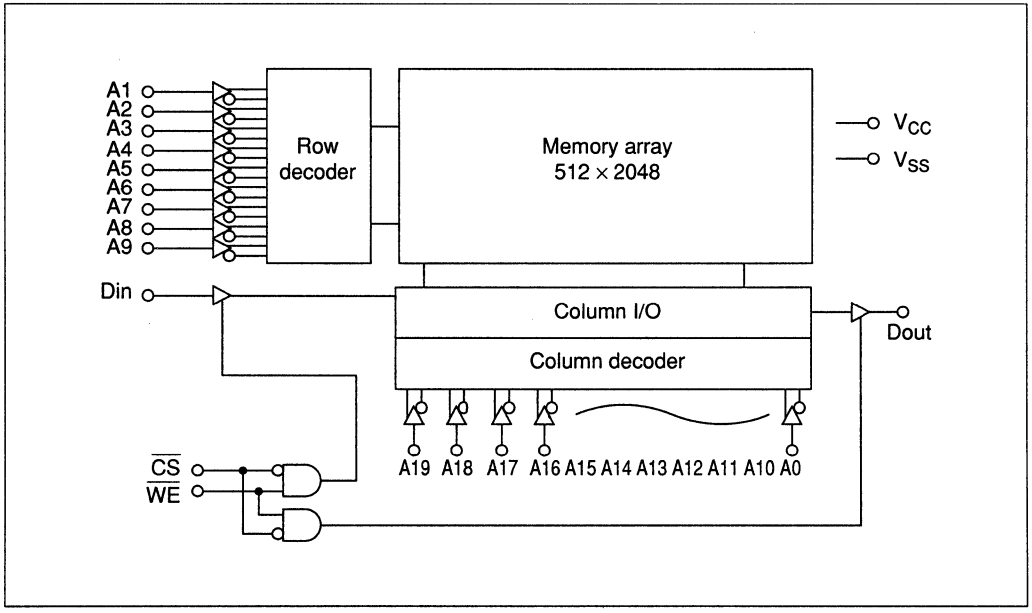
Pin Arrangement



Pin Description

Pin Name	Function
A0 – A19	Address
D	Input
Q	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} current	Output pin	Ref. cycle
H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle
L	L	Write	I_{CC}	High-Z	Write cycle

Note: 1. X : H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: 1. Vin min = −2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM621100A-20			HM621100A-25/35				
Parameter	**Symbol**	**Min**	**Typ*1**	**Max**	**Min**	**Typ*1**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle
Standby power supply current	I_{SB}	—	—	60	—	—	40	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}*2	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
	I_{SB1}*3	—	—	100	—	—	100	µA	
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
2. P and JP version
3. LP and LJP version

Capacitance (Ta = 25°C, f = 1 MHz)

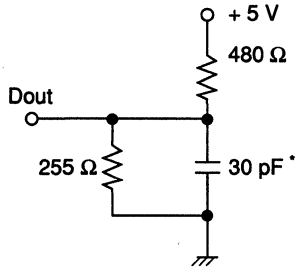
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Input capacitance	Cin	—	5*2	pF	Vin = 0 V
			6*3		
Output capacitance	Cout	—	8	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.
2. SOJ package
3. DIP package

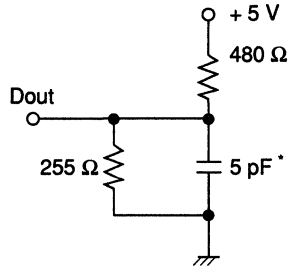
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall times: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)
Note: Including scope and jig

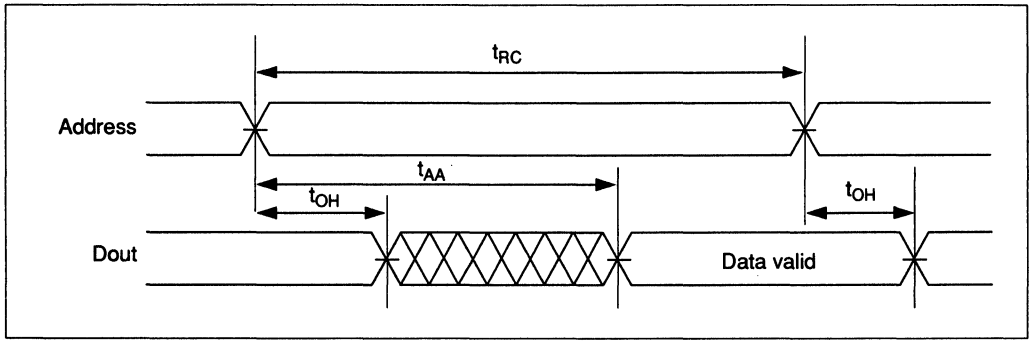


Output load (B)
(For t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

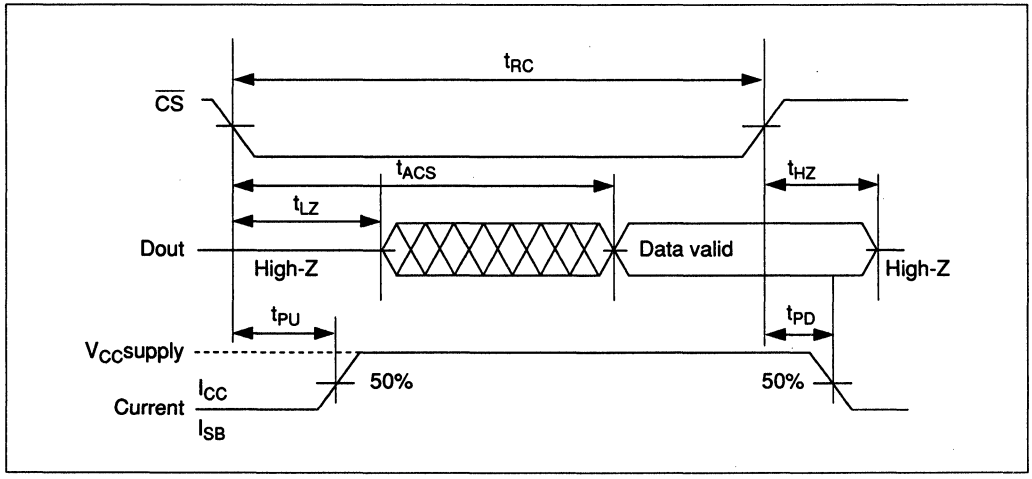
Read Cycle

		HM621100A-20		HM621100A-25		HM621100A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip select access time	t_{ACS}	—	20	—	25	—	35	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	10	0	12	0	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	12	—	15	—	25	ns

Read Timing Waveform (1) *2, *3



Read Timing Waveform (2) *2, *4

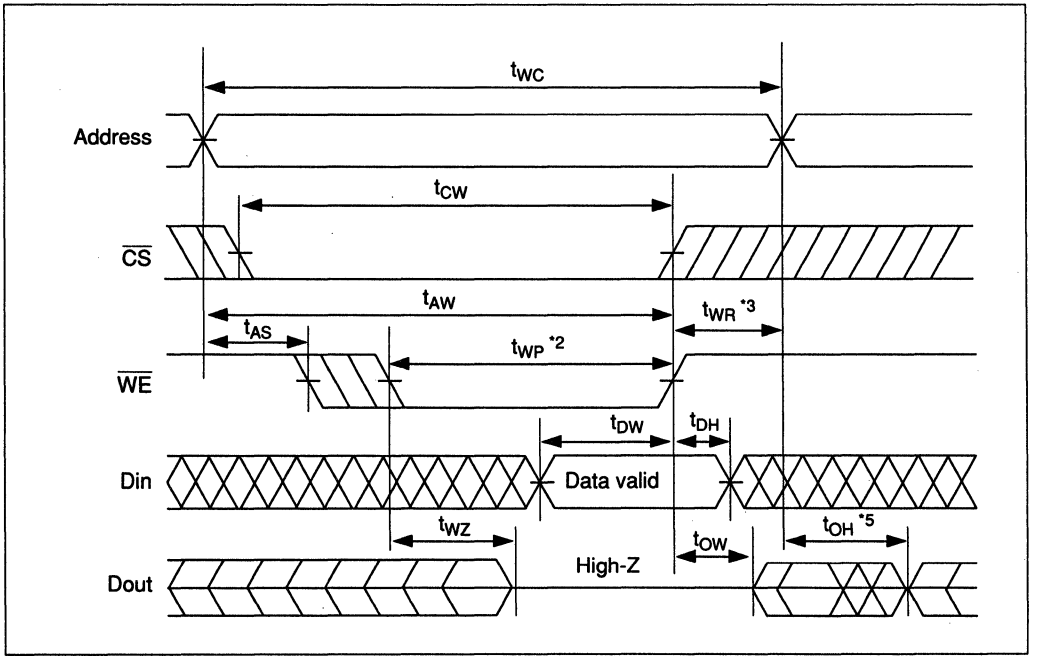


Notes: 1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

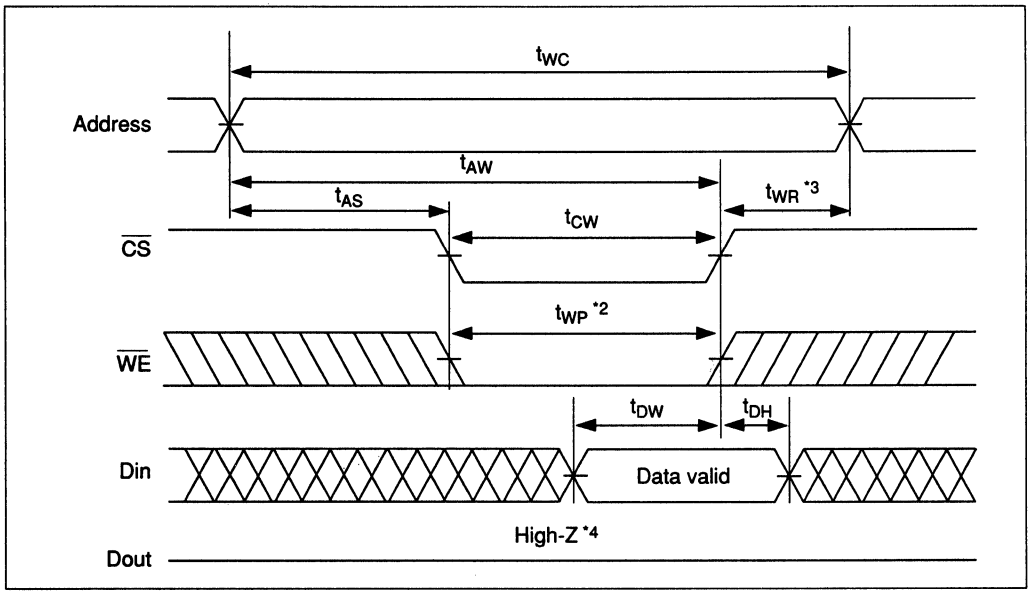
Write Cycle

Parameter	Symbol	HM621100A-20 Min	HM621100A-20 Max	HM621100A-25 Min	HM621100A-25 Max	HM621100A-35 Min	HM621100A-35 Max	Unit
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Chip selection to end of write	t_{CW}	15	—	17	—	25	—	ns
Address valid to end of write	t_{AW}	16	—	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	17	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Write to output in high-Z	t_{WZ}*1	0	12	0	15	0	15	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*1	0	—	0	—	0	—	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes:
1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

3

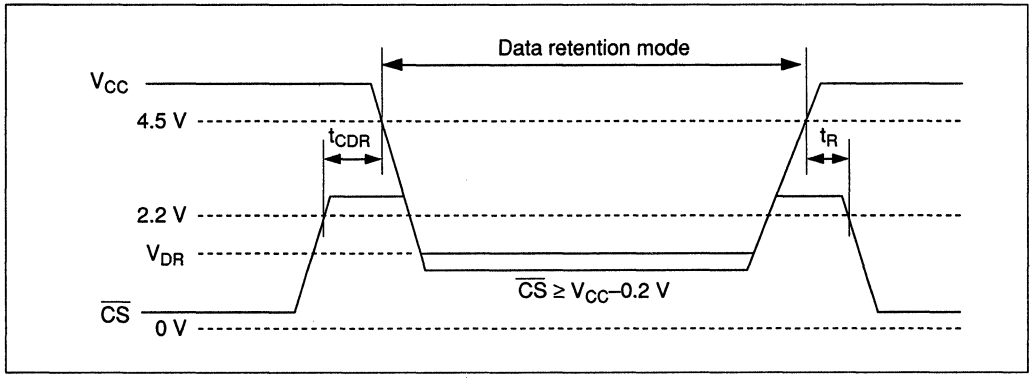
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

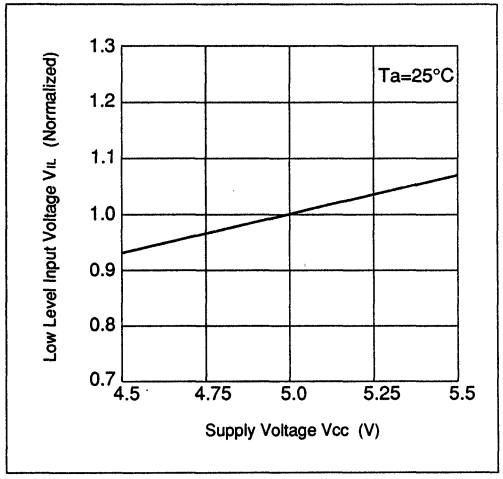
This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

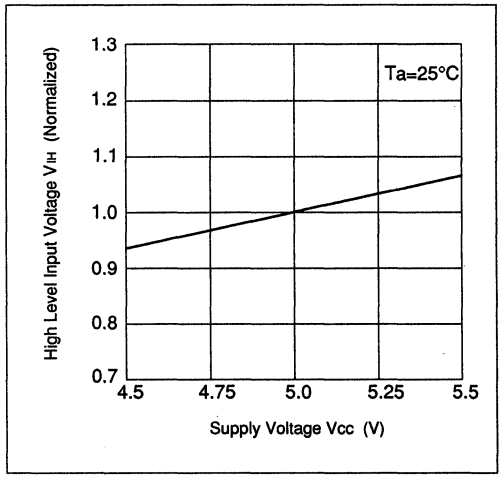
Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform

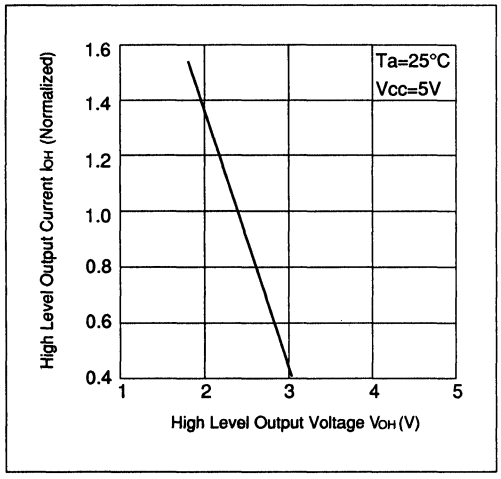




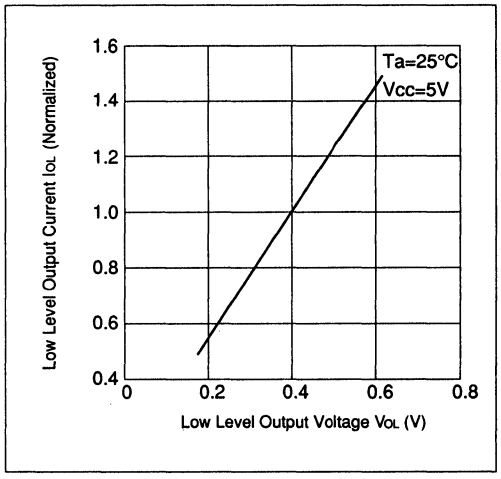
Low Level Input Voltage vs. Supply Voltage



High Level Input Voltage vs. Supply Voltage

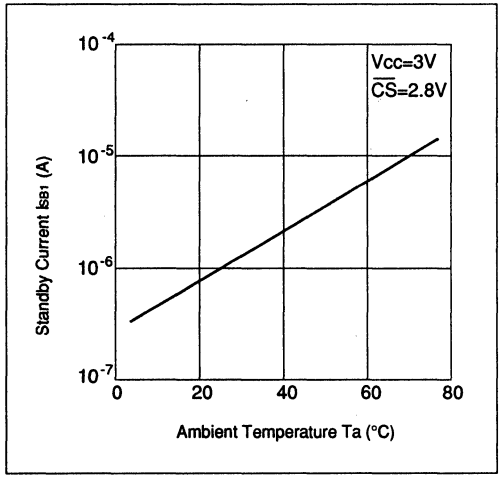


High Level Output Current vs. High Level Output Voltage

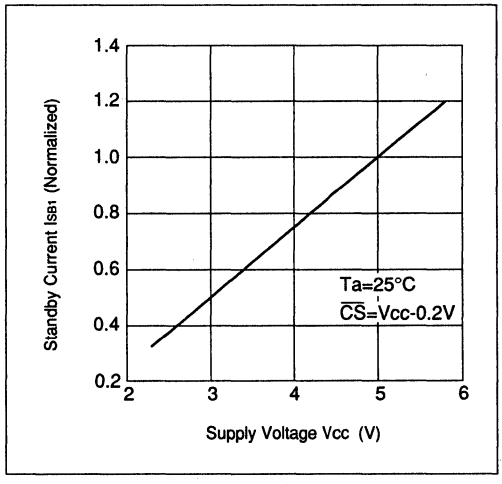


Low Level Output Current vs. Low Level Output Voltage

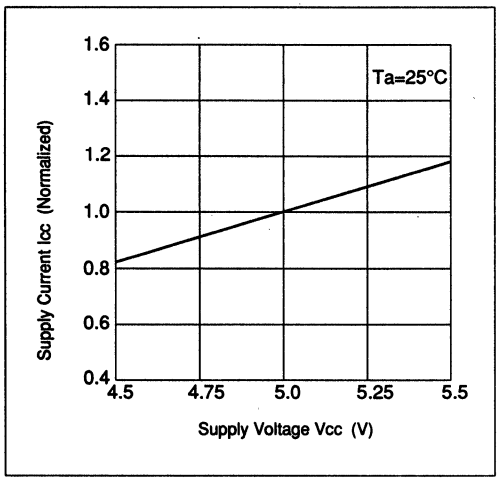
3



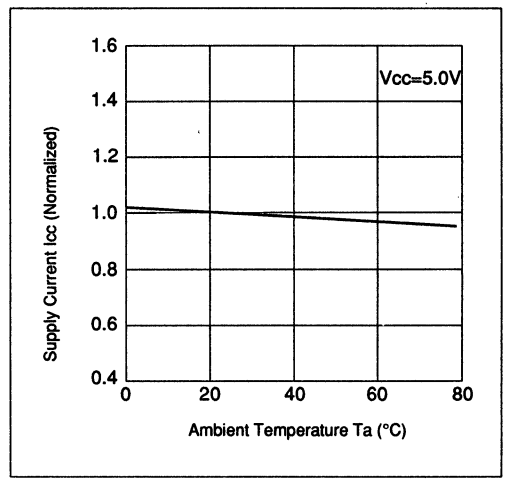
Standby Current vs. Ambient Temperature



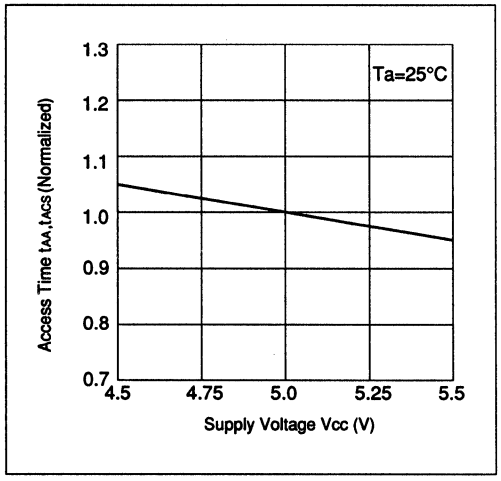
Standby Current vs. Supply Voltage



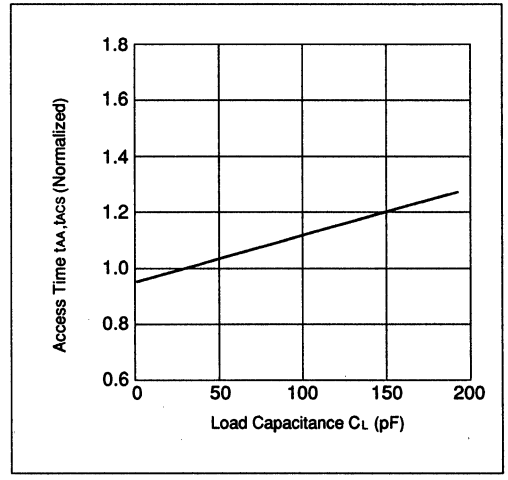
Supply Current vs. Supply Voltage



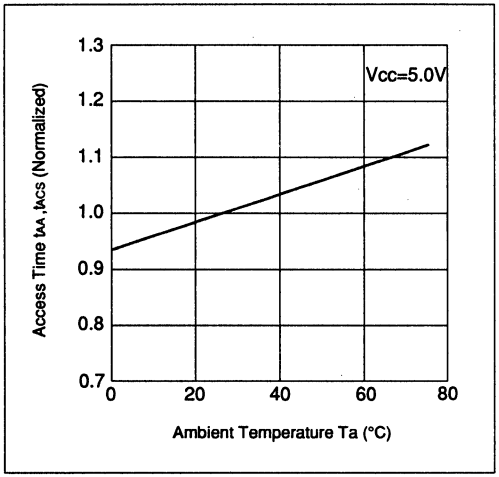
Supply Current vs. Ambient Temperature



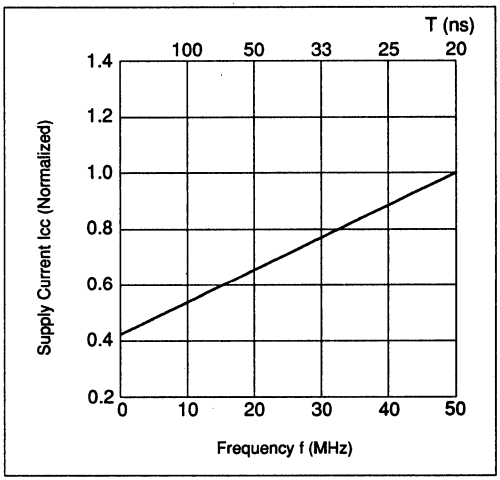
Access Time vs. Supply Voltage



Access Time vs. Load Capacitance



Access Time vs. Ambient Temperature



Supply Current vs. Frequency

3

HM624256A Series

262144-word × 4-bit High Speed CMOS Static RAM

The Hitachi HM624256A is a high speed 1M Static RAM organized as 256-kword × 4-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624256A, packaged in a 400-mil plastic SOJ is available for high density mounting.

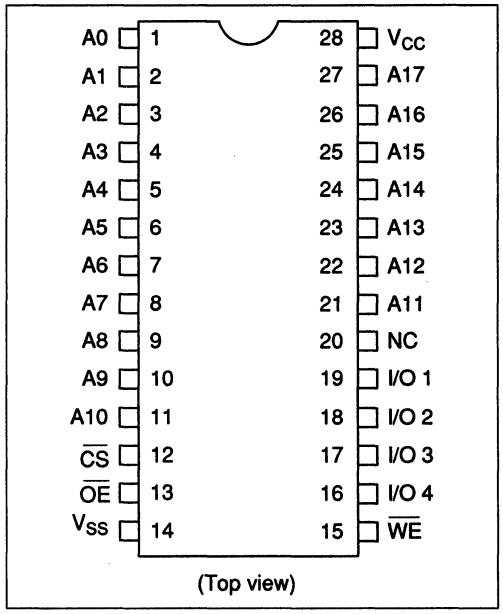
Features

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed
  Access time: 20/25/35 ns (maximum)
- Low power dissipation
  Active mode: 350 mW (typical)
  Standby mode: 100 µW (typical)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM624256AP-20	20 ns	400 mil 28-pin plastic DIP (DP-28C)
HM624256AP-25	25 ns	
HM624256AP-35	35 ns	
HM624256ALP-20	20 ns	
HM624256ALP-25	25 ns	
HM624256ALP-35	35 ns	
HM624256AJP-20	20 ns	400 mil 28-pin plastic SOJ (CP-28D)
HM624256AJP-25	25 ns	
HM624256AJP-35	35 ns	
HM624256ALJP-20	20 ns	
HM624256ALJP-25	25 ns	
HM624256ALJP-35	35 ns	

Pin Arrangement

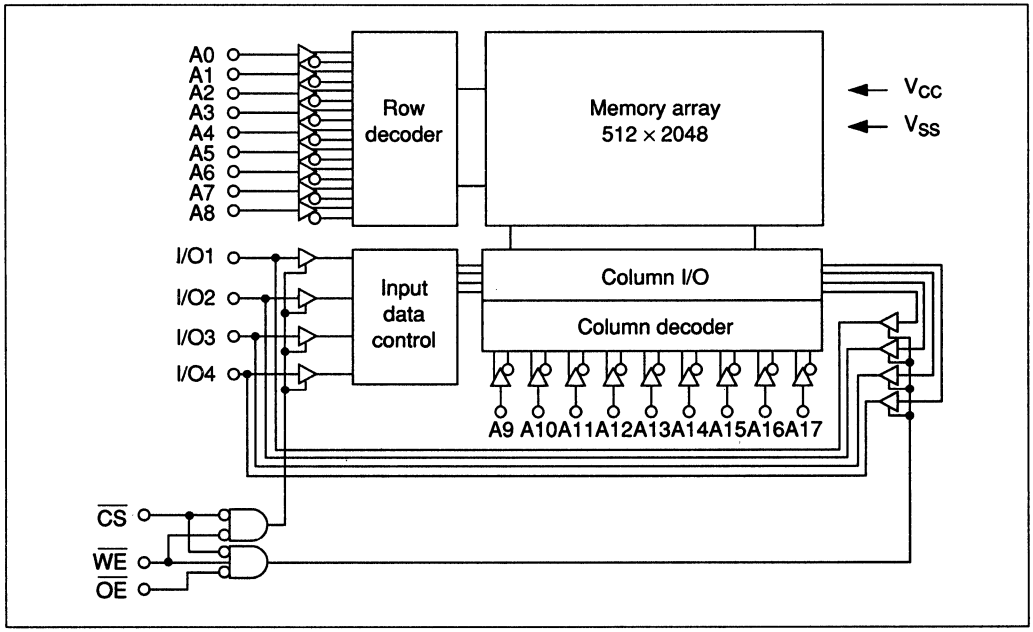


(Top view)

Pin Description

Pin name	Function
A0 – A17	Address
I/O1 – I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Not selected	I_{SB}, I_{SB1}	High-Z *	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) – (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: 1. Vin min = –2.0 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM624256A-20			HM624256A-25/35				
Parameter	Symbol	Min	Typ*1	Max	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle
Standby power supply current	I_{SB}	—	—	60	—	—	40	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V
	I_{SB1}*2	—	—	100*2	—	—	100*2	µA	
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4 mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
2. LP and LJP version

Capacitance (Ta = 25°C, f = 1 MHz)

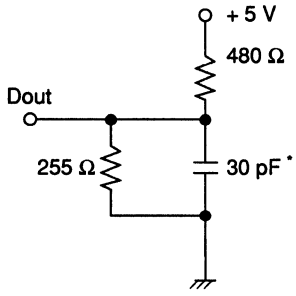
Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance	Cin	—	5*2	pF	Vin = 0 V
			6*3		
Input/output capacitance	$C_{I/O}$	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.
2. SOJ package
3. DIP package

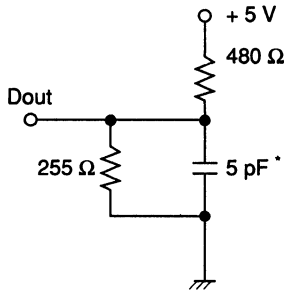
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0V to 3.0 V
- Input rise and fall times: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



Output load (B)
(For t_{CHZ}, t_{OHZ}, t_{CLZ}, t_{OLZ}, t_{WHZ} and t_{OW})

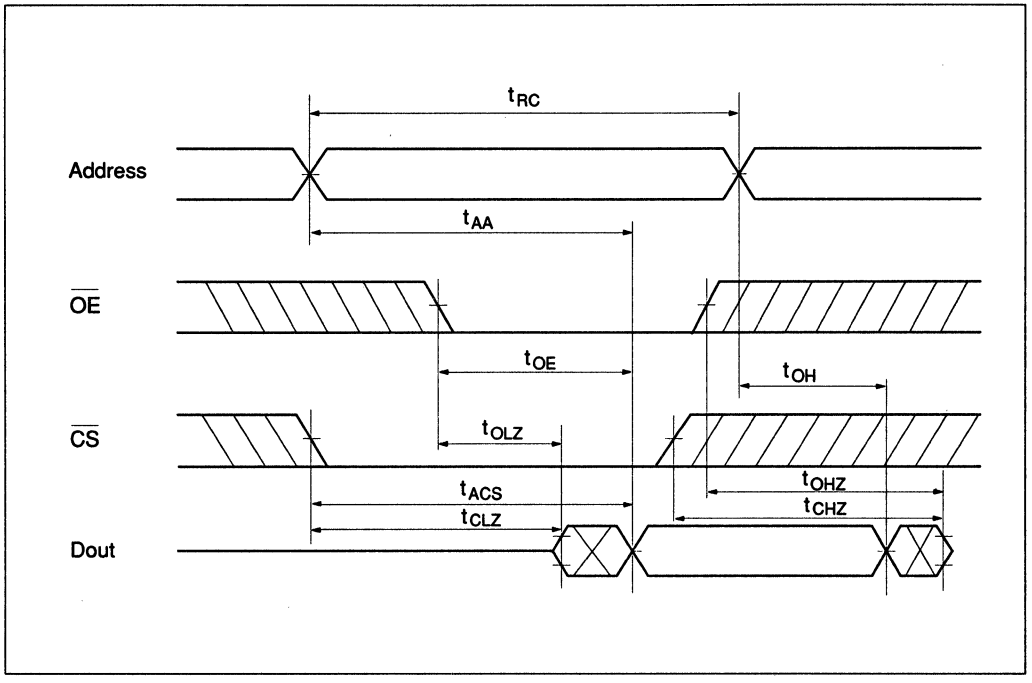
Note: Including scope and jig

3

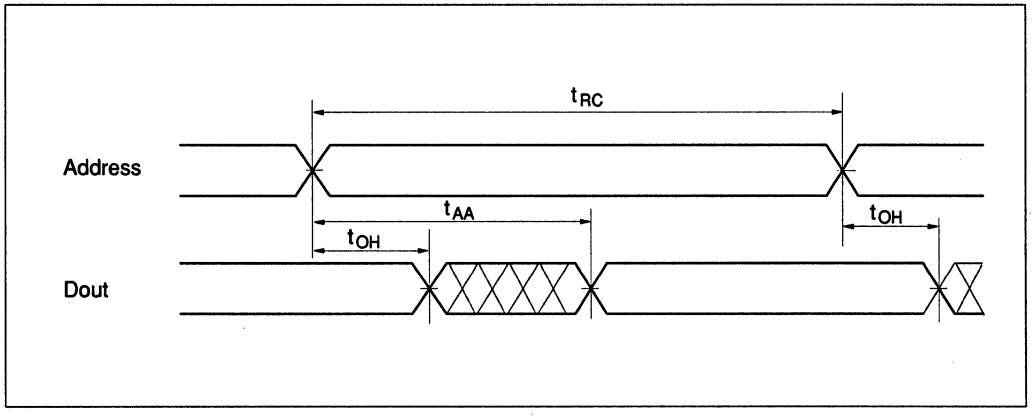
Read Cycle

		HM624256A-20		HM624256A-25		HM624256A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip select access time	t_{ACS}	—	20	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	10	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	10	0	12	0	15	ns
Chip disable to output in high-Z	t_{OHZ}*1	0	10	0	10	0	10	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	12	—	15	—	25	ns

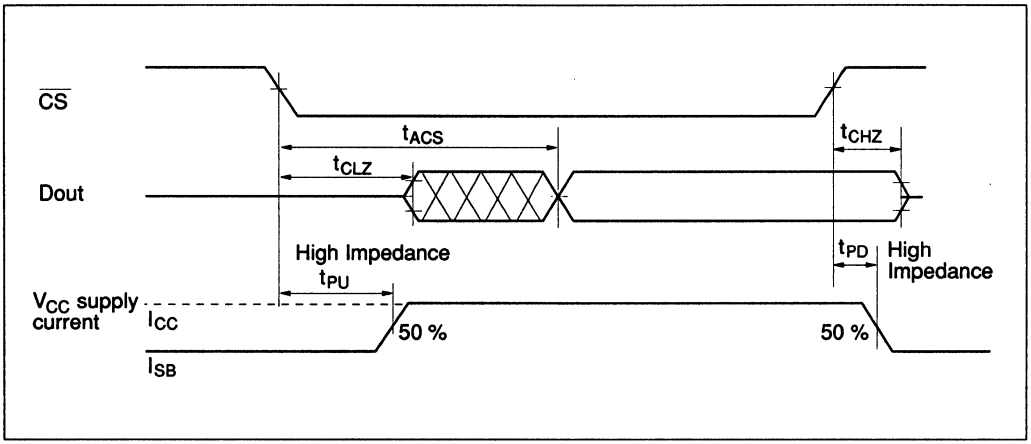
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *2, *3, *5



Read Timing Waveform (3) *1, *2, *4, *5



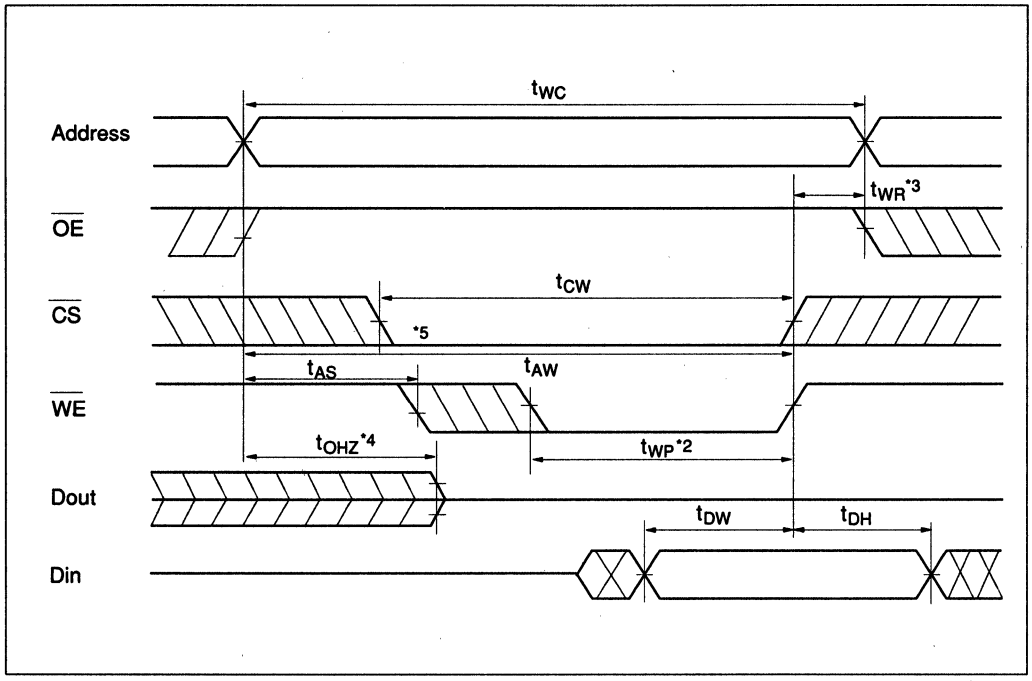
Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE} = V_{IL}$

3

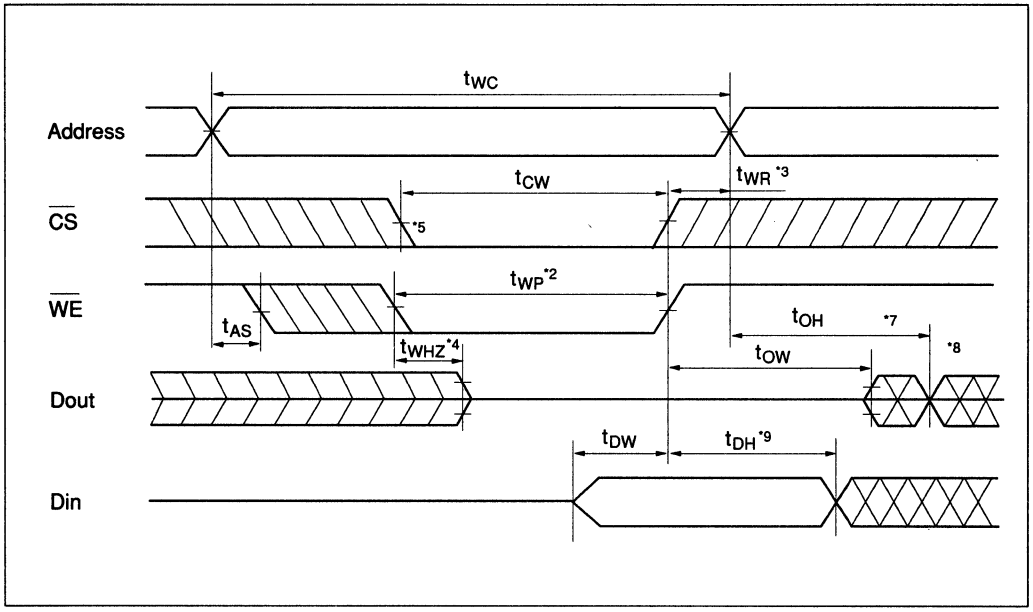
Write Cycle

		HM624256A-20		HM624256A-25		HM624256A-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Chip selection to end of write	t_{CW}	15	—	17	—	25	—	ns
Address valid to end of write	t_{AW}	16	—	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	17	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output disable to output in high-Z	t_{OHZ}*1	0	10	0	10	0	10	ns
Write to output in high-Z	t_{WHZ}*1	0	12	0	15	0	15	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*1	0	—	0	—	0	—	ns

Write Timing Waveform (1)



Write Timing Waveform (2) *6



Notes:
1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

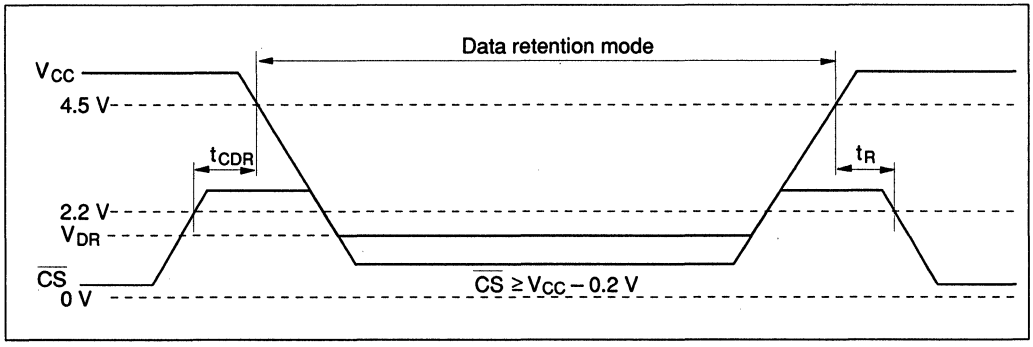
Low V_{CC} Date Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V $\leq$ Vin $\leq$ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



HM628127H/HM629127H Series — Preliminary

131072-word × 8/9-bit High Speed CMOS Static RAM

The HM628127H/HM629127H is an asyncronous high speed static RAM organized as 128 kword x 8/9 bit. It realize high speed access time (15/17/20/25 ns) with employing 0.8 µm CMOS process and high speed circuit designing technology.

It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.

The HM628127H/HM629127H is packaged in 400-mil 32/36-pin SOJ for high density surface mounting.

Features

- Single 5 V supply: 5 V ± 10%
- Access time 15/17/20/25 ns (max)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - All inputs and outputs
- 400-mil 32/36-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

Ordering Information

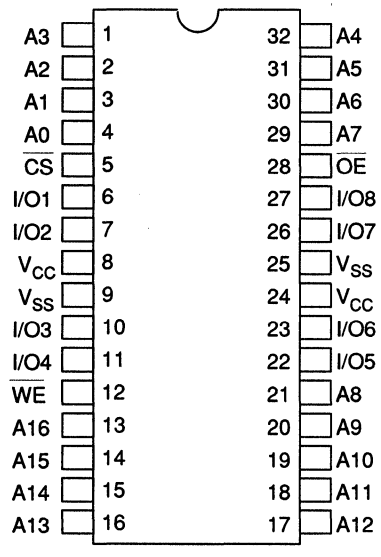
Type No.	Access time	Package
HM628127HJP-15	15 ns	400-mil 32-pin plastic SOJ (CP-32DB)
HM628127HJP-17	17 ns	
HM628127HJP-20	20 ns	
HM628127HJP-25	25 ns	
HM628127HLJP-15	15 ns	
HM628127HLJP-17	17 ns	
HM628127HLJP-20	20 ns	
HM628127HLJP-25	25 ns	
HM629127HJP-15	15 ns	400-mil 36-pin Plastic SOP (CP-36D)
HM629127HJP-17	17 ns	
HM629127HJP-20	20 ns	
HM629127HJP-25	25 ns	
HM629127HLJP-15	15 ns	
HM629127HLJP-17	17 ns	
HM629127HLJP-20	20 ns	
HM629127HLJP-25	25 ns	

3

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

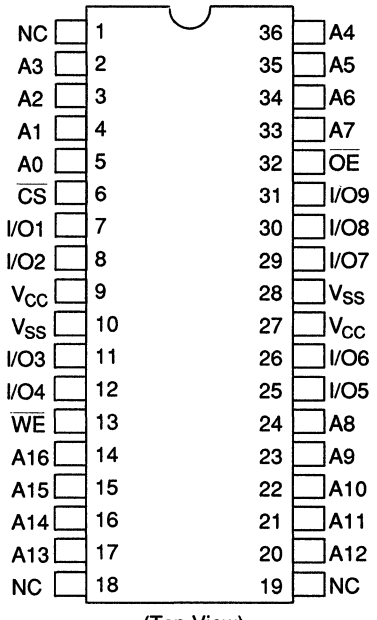
Pin Arrangement

HM628127H Series



(Top View)

HM629127H Series



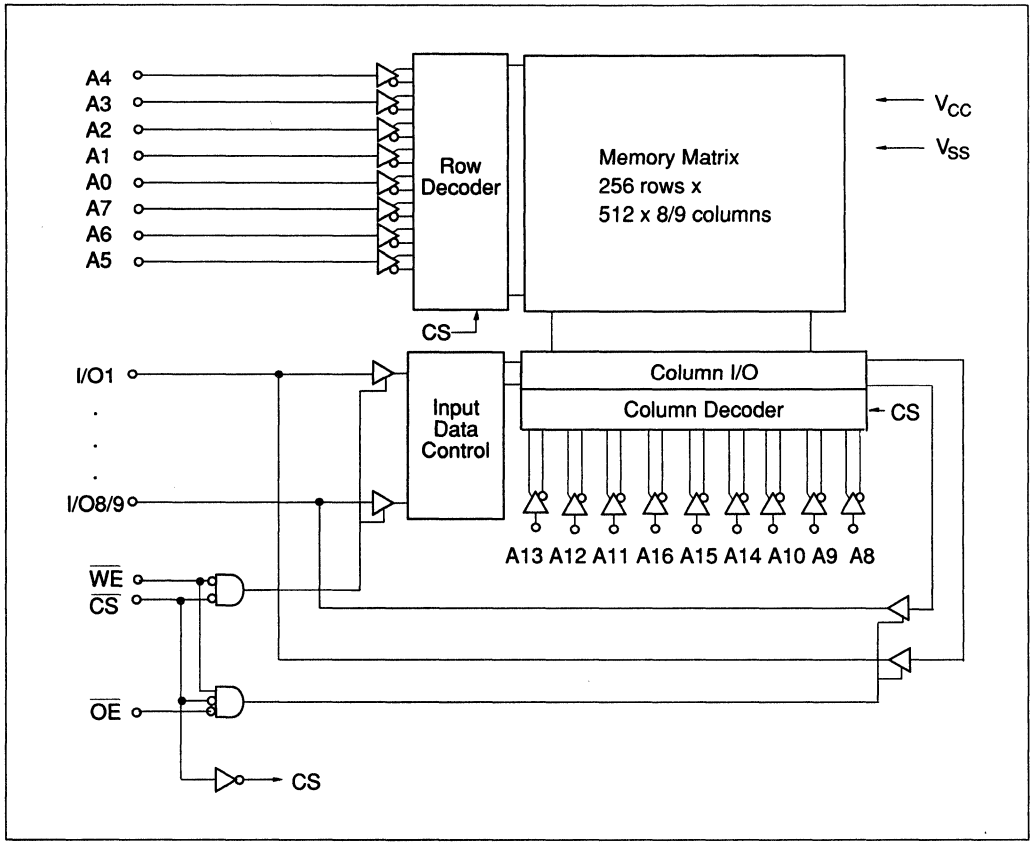
(Top View)

Pin Description

Pin name

HM628127H	HM629127H	Function
A0 – A16	A0 – A16	Address
I/O1 – I/O8	I/O1 – I/O9	Data input/output
$\overline{CS}$	$\overline{CS}$	Chip select
$\overline{WE}$	$\overline{WE}$	Write enable
$\overline{OE}$	$\overline{OE}$	Output enable
V_{CC}	V_{CC}	Power supply
V_{SS}	V_{SS}	Ground
—	NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5 *1 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0*2 / 1.5*3	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –2.5 V for pulse width (under shoot) ≤ 10 ns
2. at still air condition
3. at air flow ≥ 1.0 m/s

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	V_{CC} current	I/O	Ref. cycle
H	X	X	I_{SB}, I_{SB1}	High-Z	—
L	H	H	I_{CC}	High-Z	—
L	L	H	I_{CC}	Output	Read cycle
L	X	L	I_{CC}	Input	Write cycle

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*2	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	−0.5 *1	—	0.8	V

Note: 1. −2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$V_{I/O}$ = V_{SS} to V_{CC}	1
Operating power supply current	I_{CC}	—	160	220	mA	15 ns cycle	$\overline{CS}$ = V_{IL}, Iout = 0 mA, Other inputs = V_{IH}/V_{IL}	
		—	140	200	mA	17 ns cycle	
		—	130	180	mA	20 ns cycle	
		—	100	160	mA	25 ns cycle	
Standby power supply current	I_{SB}	—	70	100	mA	15 ns cycle	$\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}	
		—	60	95	mA	17 ns cycle	
		—	50	90	mA	20 ns cycle	
		—	40	85	mA	25 ns cycle	
Standby power supply current (1)	I_{SB1}	—	—	2	mA	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, 0 V ≤ Vin ≤ 0.2 V or $V_{CC} \geq$ Vin ≥ $V_{CC} - 0.2$ V	
		—	—	0.1	mA		L-version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

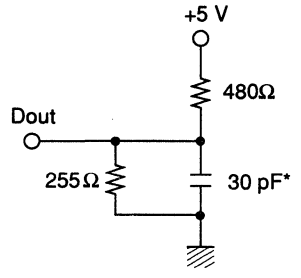
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

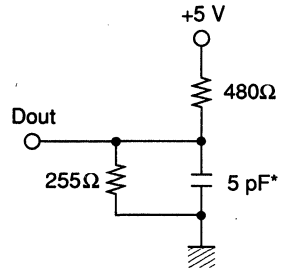
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



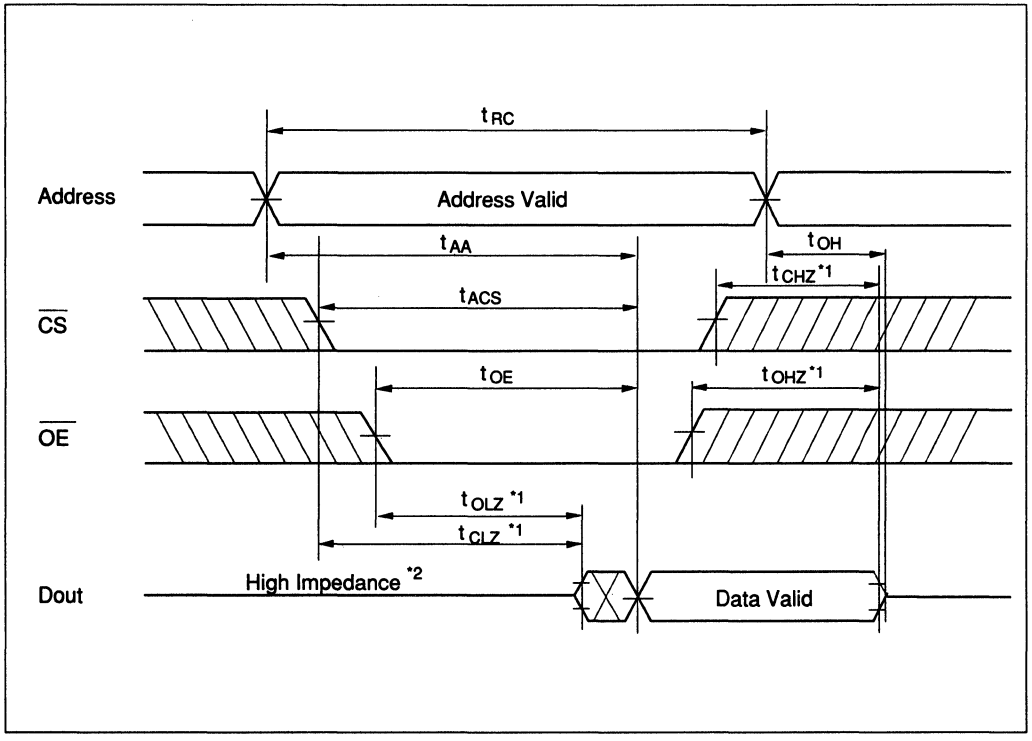
Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW})

* Including scope and jig

Read Cycle

		HM628127H/HM629127H								
		-15		-17		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	15	—	17	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	17	—	20	—	25	ns
Chip select access time	t_{ACS}	—	15	—	17	—	20	—	25	ns
Output enable to output valid	t_{OE}	—	8	—	8	—	10	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	3	—	3	—	ns
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	1	—	1	—	ns
Chip deselect to output in high-Z	t_{CHZ}	—	7	—	7	—	7	—	7	ns
Output disable to output in high-Z	t_{OHZ}	—	7	—	7	—	7	—	7	ns

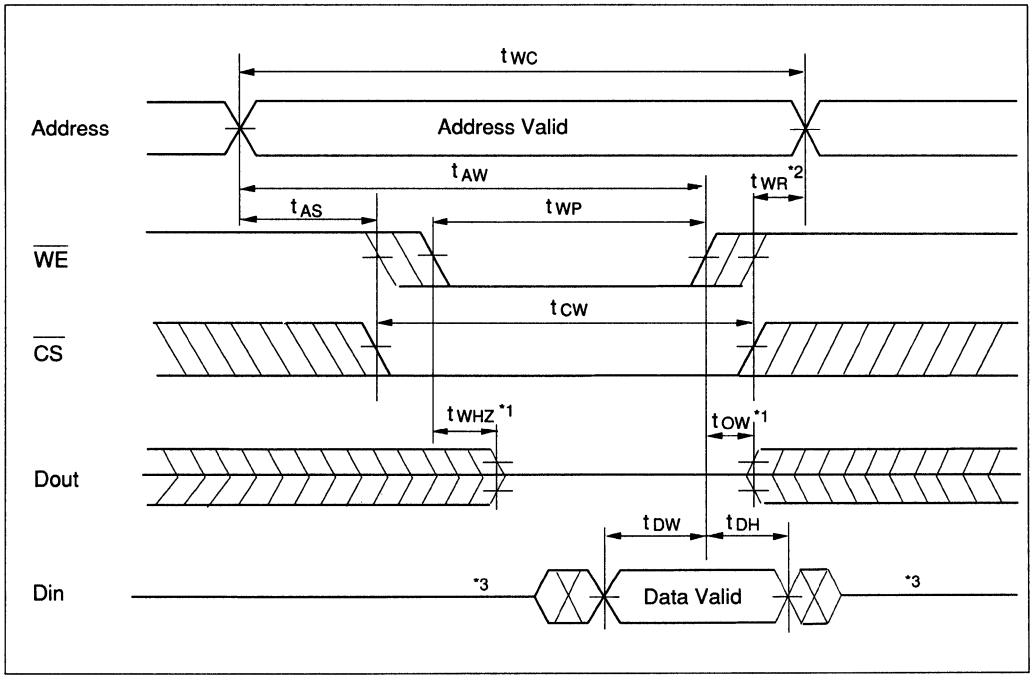
Read Timing Waveform*3



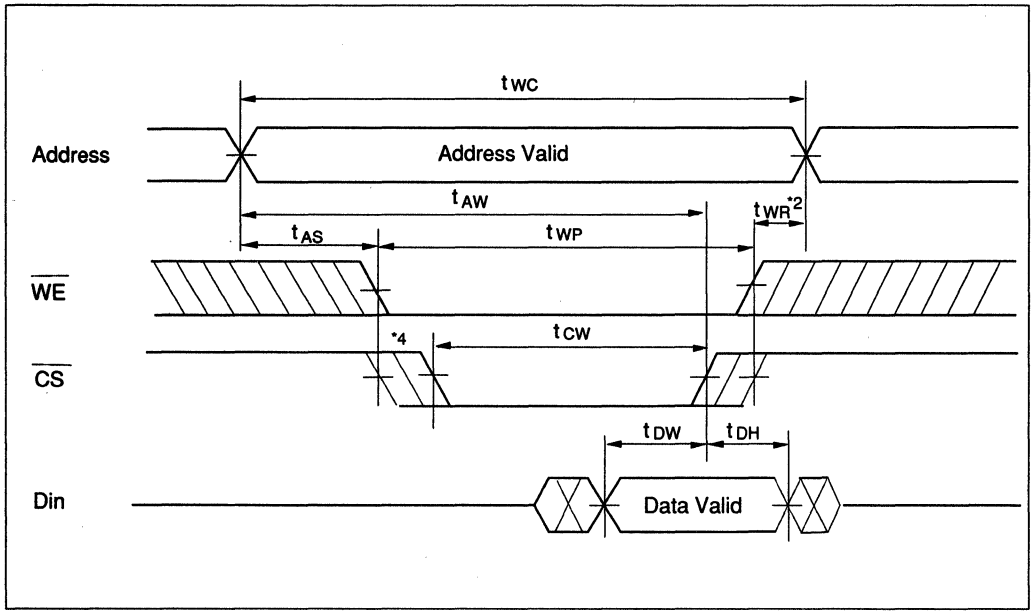
Notes: 1. Transition is measured ±200 mV from steady state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$ and $\overline{OE}$ are low, Dout is low impedance.
3. $\overline{WE}$ is high for read cycle.

Write Cycle

		HM628127H/HM629127H								
		-15		-17		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t_{WC}	15	—	17	—	20	—	25	—	ns
Address valid to end of write	t_{AW}	12	—	12	—	15	—	20	—	ns
Chip select to end of write	t_{CW}	10	—	10	—	12	—	15	—	ns
Write pulse width	t_{WP}	10	—	10	—	12	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns
Data to write time overlap	t_{DW}	8	—	8	—	10	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write disable to output in low-Z	t_{OW}	3	—	3	—	3	—	3	—	ns
Write enable to output in high-Z	t_{WHZ}	—	7	—	7	—	7	—	7	ns


tWC
Address
Address Valid
tAW
tWR*2
tAS
tWP
WE
tCW
CS
tWHZ*1
tOW*1
Dout
tDW
tDH
Din
*3
Data Valid
*3

Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: 1. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampeld and not 100% tested.
2. $\overline{WE}$ must be high during transition except when the device is disabled with $\overline{CS}$.
3. If $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.

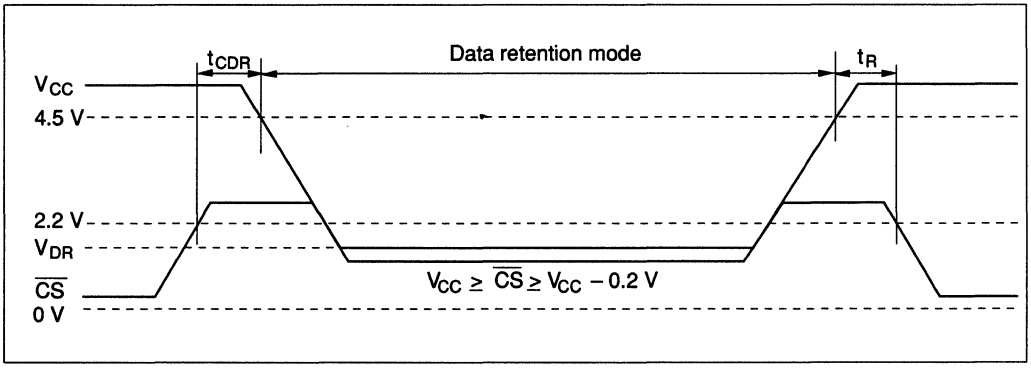
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0\ V \leq Vin \leq 0.2$ V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



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HM621664H/HM621864H Series — Preliminary

65536-word × 16/18-bit High Speed CMOS Static RAM

The HM621664H/HM621864H is an asyncronous high speed static RAM organized as 64 kword × 16/18 bit. It realize high speed access time (15/17/20/25 ns) with employing 0.8 µm CMOS process and high speed circuit designing technology.

It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.

The HM621664H/HM621864H is packaged in 400-mil 44-pin SOJ & TSOP-II for high density surface mounting.

Features

- Single 5 V supply: 5 V ± 10%
- Access time 15/17/20/25 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- 400-mil 44-pin SOJ & TSOP-II package
- Center V_{CC} and V_{SS} type pinout

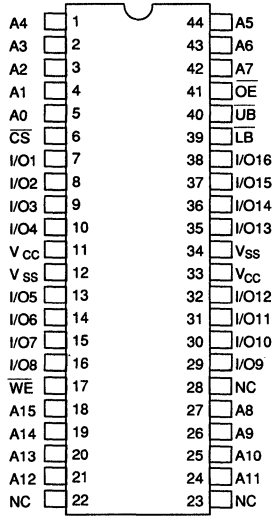
Ordering Information

Type No.	Access time	Package
HM621664HJP-15	15 ns	400-mil 44-pin plastic SOJ (CP-44D)
HM621664HJP-17	17 ns	
HM621664HJP-20	20 ns	
HM621664HJP-25	25 ns	
HM621664HLJP-15	15 ns	
HM621664HLJP-17	17 ns	
HM621664HLJP-20	20 ns	
HM621664HLJP-25	25 ns	
HM621864HJP-15	15 ns	
HM621864HJP-17	17 ns	
HM621864HJP-20	20 ns	
HM621864HJP-25	25 ns	
HM621864HLJP-15	15 ns	
HM621864HLJP-17	17 ns	
HM621864HLJP-20	20 ns	
HM621864HLJP-25	25 ns	
HM621664HTT-15	15 ns	400-mil 44-pin plastic TSOP-II normal bend type (TTP-44DE)
HM621664HTT-17	17 ns	
HM621664HTT-20	20 ns	
HM621664HTT-25	25 ns	
HM621664HLTT-15	15 ns	
HM621664HLTT-17	17 ns	
HM621664HLTT-20	20 ns	
HM621664HLTT-25	25 ns	
HM621864HTT-15	15 ns	
HM621864HTT-17	17 ns	
HM621864HTT-20	20 ns	
HM621864HTT-25	25 ns	
HM621864HLTT-15	15 ns	
HM621864HLTT-17	17 ns	
HM621864HLTT-20	20 ns	
HM621864HLTT-25	25 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

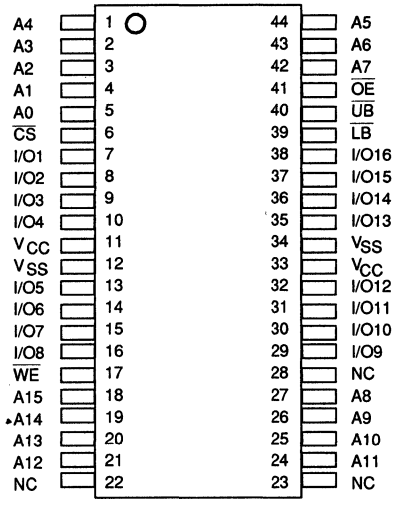
Pin Arrangement

HM621664HJP (SOJ)



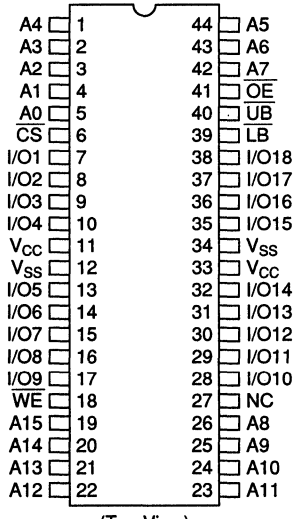
(Top View)

HM621664HTT
(Normal Bend TSOP-II)



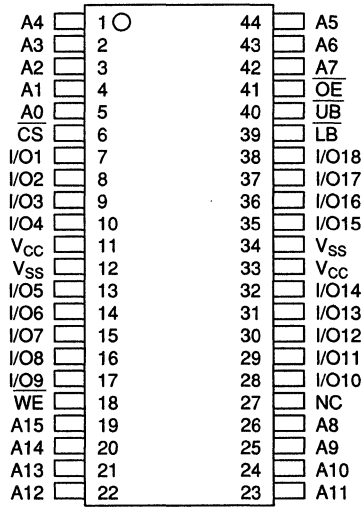
(Top View)

HM621864HJP (SOJ)



(Top View)

HM621864HTT
(Normal Bend TSOP-II)



(Top View)

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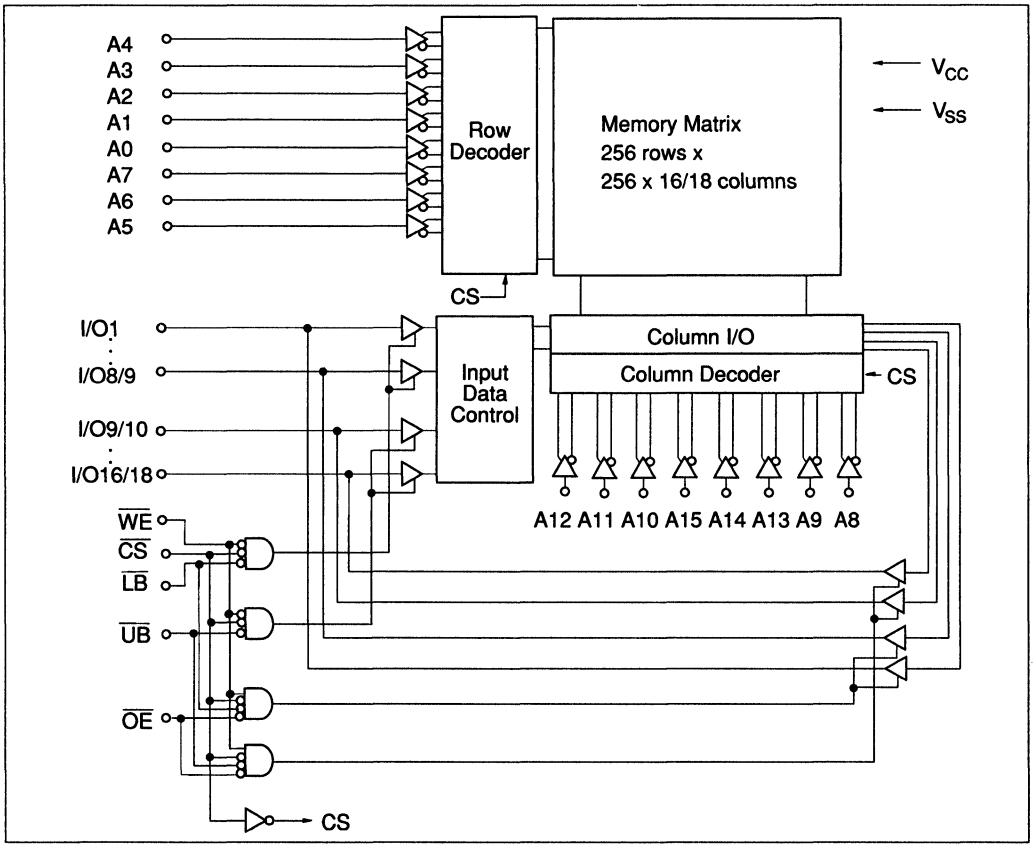
Pin Description

Pin name

HM621664H	HM621864H	Function
A0 – A15	A0 – A15	Address
I/O1 – I/O8	I/O1 – I/O9	Input/output (lower byte)
I/O9 – I/O16	I/O10 – I/O18	Input/output (upper byte)
$\overline{CS}$	$\overline{CS}$	Chip select
$\overline{LB}$	$\overline{LB}$	Lower byte select
$\overline{UB}$	$\overline{UB}$	Upper byte select
$\overline{WE}$	$\overline{WE}$	Write enable
$\overline{OE}$	$\overline{OE}$	Output enable
V_{CC}	V_{CC}	Power supply
V_{SS}	V_{SS}	Ground
NC	NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5 *1 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0*2 / 1.5*3	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –2.5 V for pulse width (under shoot) ≤ 10 ns
2. at still air condition
3. at air flow ≥ 1.0 m/s

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	V_{CC} current	I/O (Lower byte)	I/O (Upper byte)	Ref. cycle
H	X	X	X	X	I_{SB}, I_{SB1}	High-Z	High-Z	—
L	H	H	X	X	I_{CC}	High-Z	High-Z	—
L	L	H	L	L	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	I_{CC}	High-Z	High-Z	—
L	X	L	L	L	I_{CC}	Input	Input	Write cycle
L	X	L	L	H	I_{CC}	Input	High-Z	Write cycle
L	X	L	H	L	I_{CC}	High-Z	Input	Write cycle
L	X	L	H	H	I_{CC}	High-Z	High-Z	—

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*2	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	–0.5 *1	—	0.8	V

Note: 1. –2.0 V for pulse width (under stoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$V_{I/O}$ = V_{SS} to V_{CC}	1
Operating power supply current	I_{CC}	—	190	260	mA	15 ns cycle	$\overline{CS}$ = V_{IL}, Iout = 0 mA, Other inputs = V_{IH}/V_{IL}	
		—	175	240	mA	17 ns cycle		
		—	160	220	mA	20 ns cycle		
		—	145	200	mA	25 ns cycle		
Standby power supply current	I_{SB}	—	70	100	mA	15 ns cycle	$\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}	
		—	60	95	mA	17 ns cycle		
		—	50	90	mA	20 ns cycle		
		—	40	85	mA	25 ns cycle		
Standby power supply current (1)	I_{SB1}	—	—	2	mA	V_{CC} ≥ $\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or V_{CC} ≥ Vin ≥ V_{CC} – 0.2 V	
		—	—	0.1	mA		L-version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

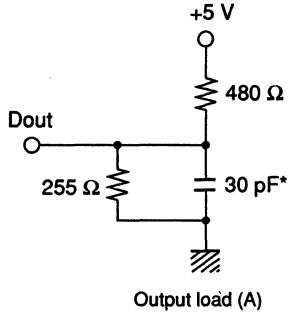
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

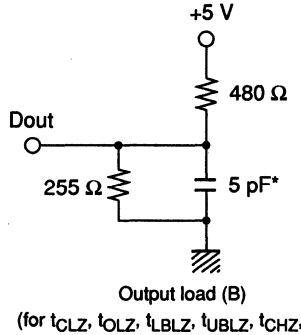
Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)

* Including scope and jig



Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{LBLZ}, t_{UBLZ}, t_{CHZ}, t_{OHZ}, t_{LBHZ}, t_{UBHZ}, t_{WHZ}, and t_{OW})

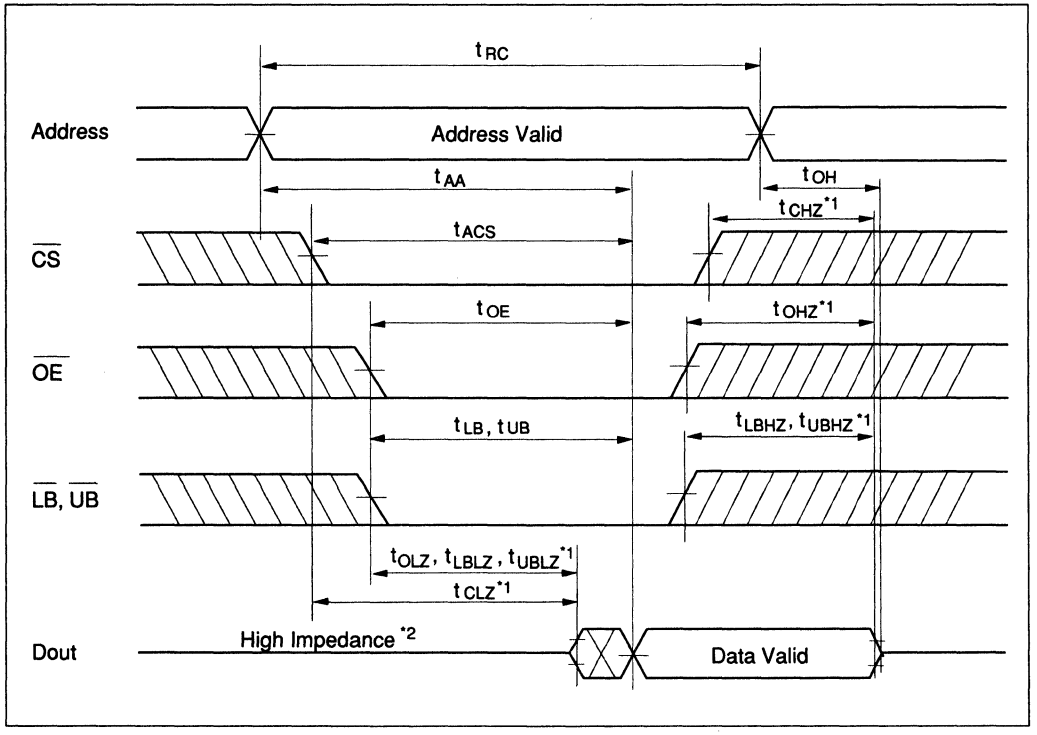
Read Cycle

		HM621664H/HM621864H								
		-15		-17		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	15	—	17	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	17	—	20	—	25	ns
Chip select access time	t_{ACS}	—	15	—	17	—	20	—	25	ns
Output enable to output valid	t_{OE}	—	8	—	8	—	10	—	12	ns
Byte select to output valid	t_{LB}, t_{UB}	—	8	—	8	—	10	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	3	—	3	—	ns
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	1	—	1	—	ns
Byte select to output in low-Z	t_{LBLZ}, t_{UBLZ}	1	—	1	—	1	—	1	—	ns
Chip deselect to output in high-Z	t_{CHZ}	—	7	—	7	—	7	—	7	ns

Read Cycle (cont)

		HM621664H/HM621864H								
		-15		-17		-20		-25		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Output disable to output in high-Z	t_{OHZ}	—	7	—	7	—	7	—	7	ns
Byte deselect to output in high-Z	t_{LBHZ}, t_{UBHZ}	—	7	—	7	—	7	—	7	ns

Read Timing Waveform *3

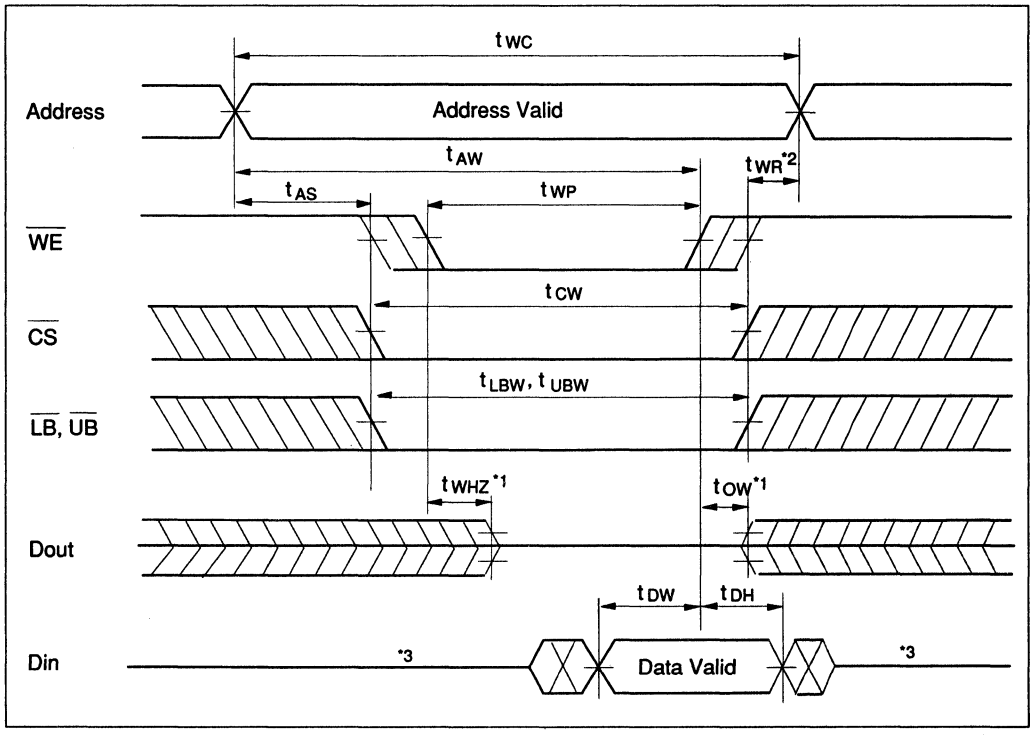


Notes: 1. Transition is measured ±200 mV from steady state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$, $\overline{OE}$, and $\overline{LB}$ are low, Dout (lower byte) is low impedance.
When $\overline{CS}$, $\overline{OE}$, and $\overline{UB}$ are low, Dout (upper byte) is low impedance.
3. $\overline{WE}$ is high for read cycle.

Write Cycle

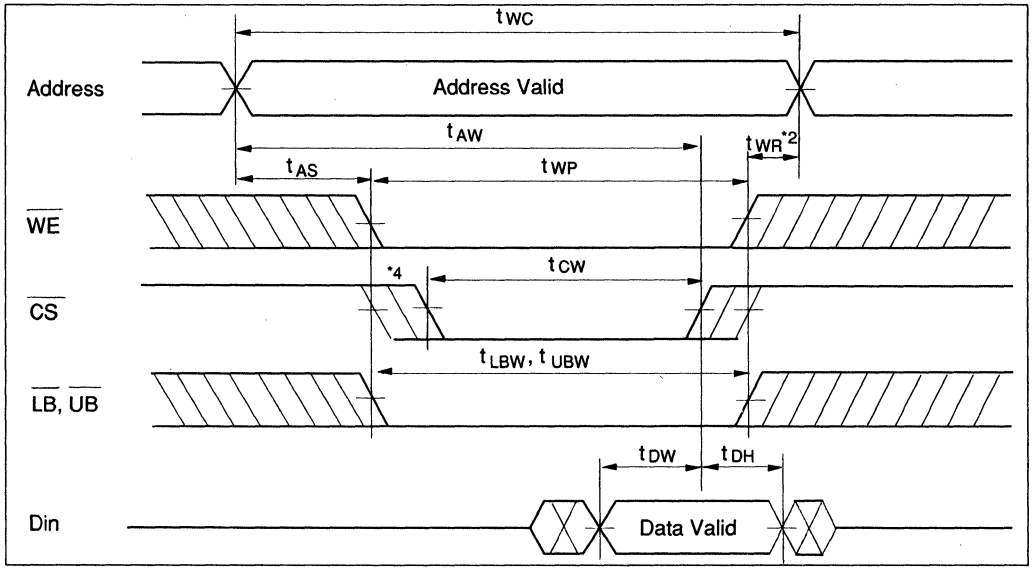
		HM621664H/HM621864H								
		-15		-17		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t_{WC}	15	—	17	—	20	—	25	—	ns
Address valid to end of write	t_{AW}	12	—	12	—	15	—	20	—	ns
Chip select to end of write	t_{CW}	10	—	10	—	12	—	15	—	ns
Write pulse width	t_{WP}	10	—	10	—	12	—	15	—	ns
Byte select to end of write	t_{LBW}, t_{UBW}	10	—	10	—	12	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns
Data to write time overlap	t_{DW}	8	—	8	—	10	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write disable to output in low-Z	t_{OW}	3	—	3	—	3	—	3	—	ns
Write enable to output in high-Z	t_{WHZ}	—	7	—	7	—	7	—	7	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)

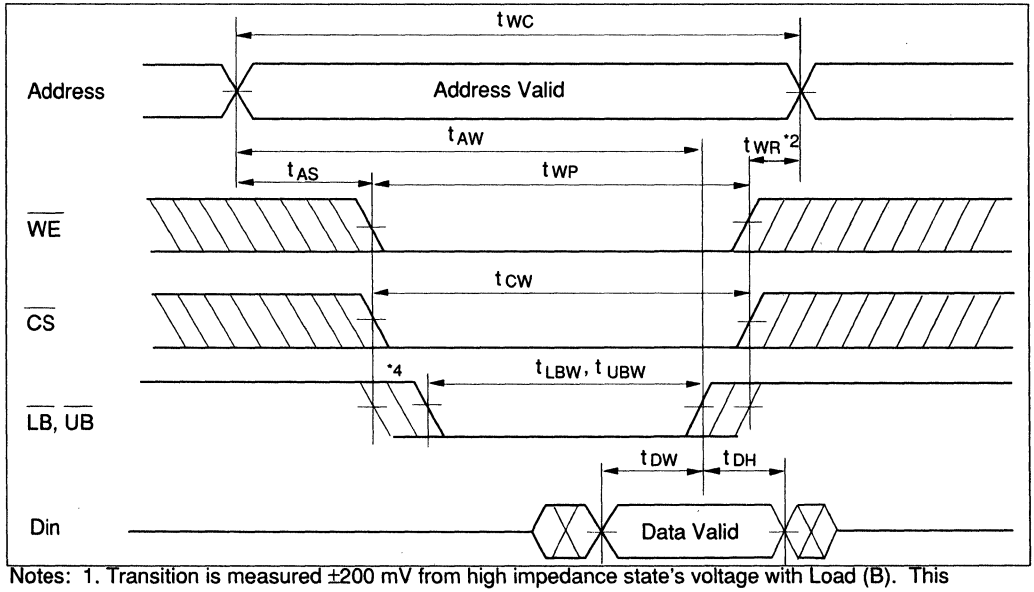


3

Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Write Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes: 1. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampeld and not 100% tested.
2. $\overline{WE}$ must be high during address transition except when the device is disabled with $\overline{CS}$, $\overline{LB}$, or $\overline{UB}$.
3. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$ or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.

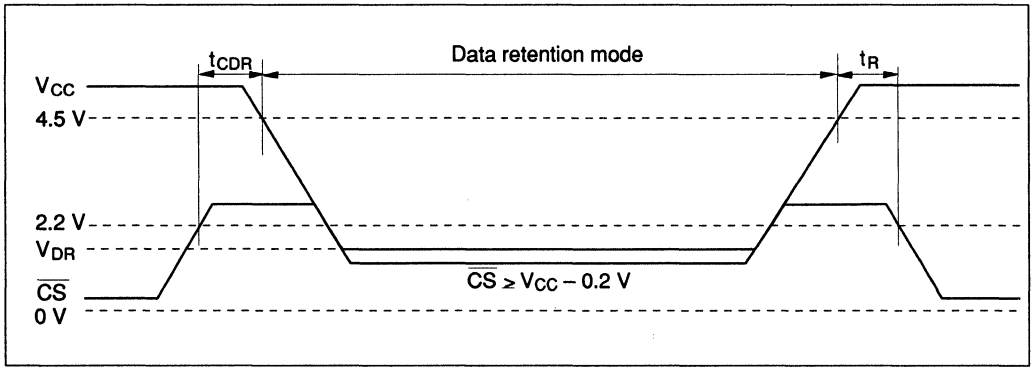
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0\ V \leq Vin \leq 0.2$ V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



HM62W832

Preliminary

32,768-word × 8-bit High Speed Static Access Memory

3.3 V Supply

Description

The HM62W832 series is Hitachi's new 256K Fast Static RAM with a 32,768-word × 8 bit organization, with an access time of 20 and 25 ns. This 3.3 volt part has low power dissipation which makes it ideal for portable applications. The HM62W832 series will be manufactured on Hitachi's advanced production lines using CMOS technology.

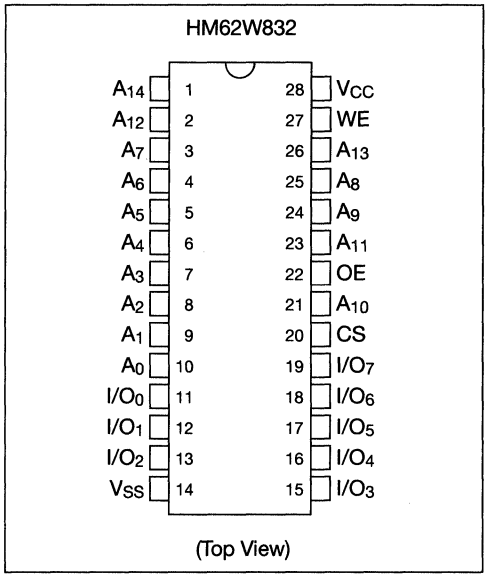
Features

- 32,768-word × 8-bit organization
- Fast access times 20/25 ns
- Single 3.3V power supply
- Low power dissipation
- Completely static memory—no timing strobe needed

Ordering Information

32K × 8 Type No.	Access time	Package
HM62W832-20	20 ns	300mil
HM62W832-25	25 ns	28 pin SOJ

Pin Arrangement



Pin Description

Pin Name	Function
A	Address Input
I/O	Data Input/Output
WE	Byte Write Enable
CS	Chip Select
OE	Output Enable
V_{CC}	+3.3V Power Supply
V_{SS}	Ground

Note: Product Preview: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

HM62W8127H Series
HM62W9127H Series

Preliminary

131072-word × 8/9-bit High Speed CMOS Static RAM

The HM62W8127H/HM62W9127H is an asyncronous 3.3 V operation high speed static RAM organized as 128 kword × 8/9 bit. It realize high speed access time (25/30/35/45 ns) with employing 0.8 µm CMOS process and high speed circuit designing technology.

It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.

The HM62W8127H/HM62W9127H is packaged in 400-mil 32/36-pin SOJ for high density surface mounting.

Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time 25/30/35/45 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly CMOS compatible
  - — All inputs and outputs
- 400-mil 32/36-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

Ordering Information

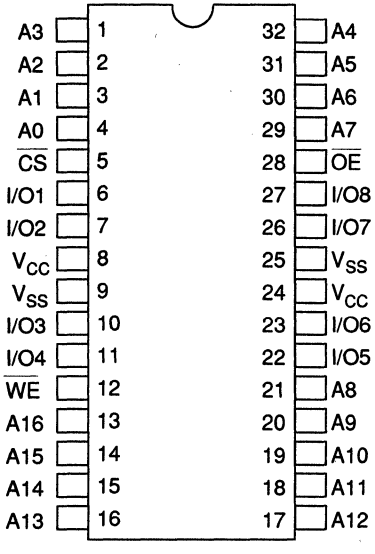
Type No.	Access time	Package
HM62W8127HJP-25	25 ns	400-mil 32-pin plastic SOJ (CP-32DB)
HM62W8127HJP-30	30 ns	
HM62W8127HJP-35	35 ns	
HM62W8127HJP-45	45 ns	
HM62W8127HLJP-25	25 ns	
HM62W8127HLJP-30	30 ns	
HM62W8127HLJP-35	35 ns	
HM62W8127HLJP-45	45 ns	
HM62W9127HJP-25	25 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM62W9127HJP-30	30 ns	
HM62W9127HJP-35	35 ns	
HM62W9127HJP-45	45 ns	
HM62W9127HLJP-25	25 ns	
HM62W9127HLJP-30	30 ns	
HM62W9127HLJP-35	35 ns	
HM62W9127HLJP-45	45 ns	

3

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

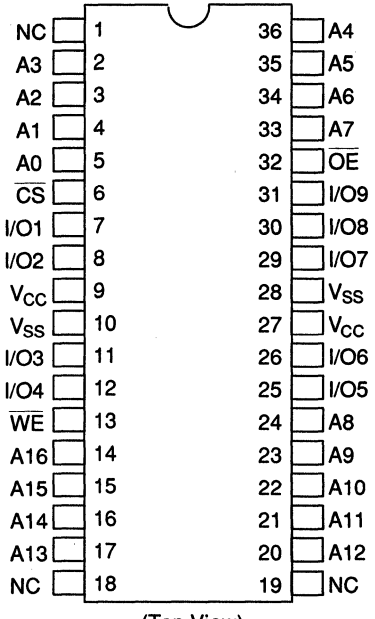
Pin Arrangement

HM62W8127H Series



(Top View)

HM62W9127H Series



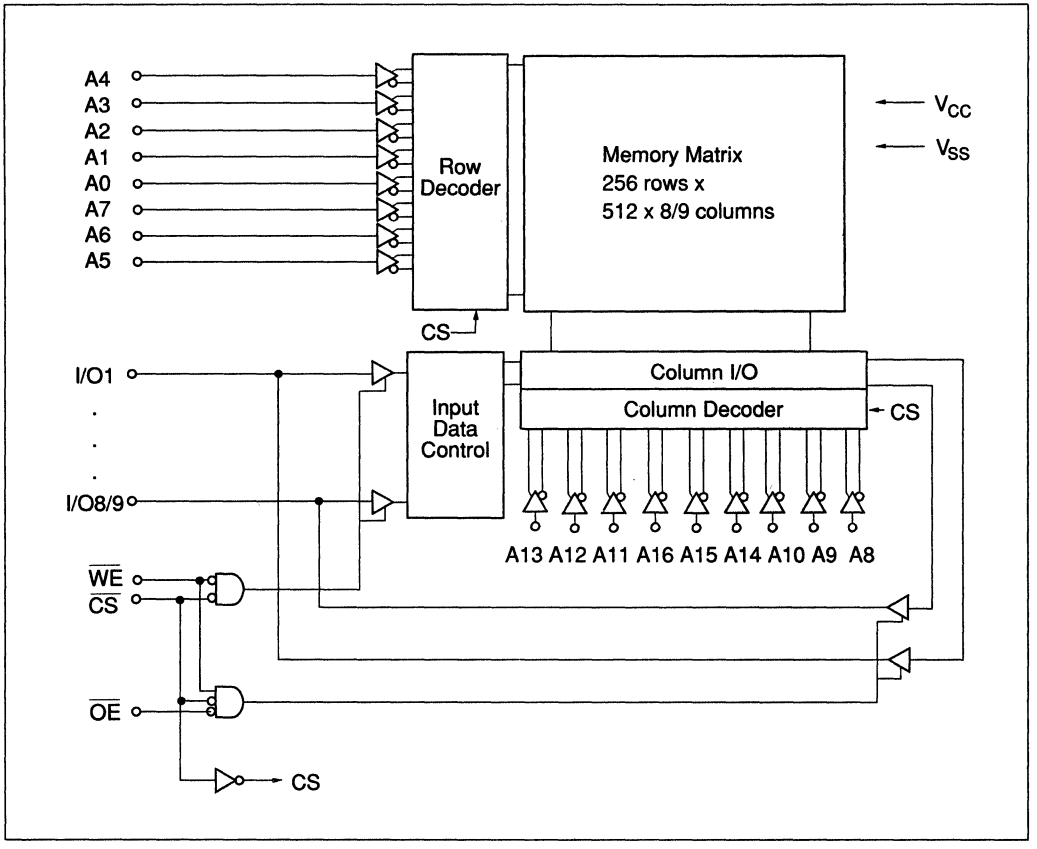
(Top View)

Pin Description

Pin name

HM62W8127H	HM62W9127H	Function
A0 – A16	A0 – A16	Address
I/O1 – I/O8	I/O1 – I/O9	Data input/output
$\overline{CS}$	$\overline{CS}$	Chip select
$\overline{WE}$	$\overline{WE}$	Write enable
$\overline{OE}$	$\overline{OE}$	Output enable
V_{CC}	V_{CC}	Power supply
V_{SS}	V_{SS}	Ground
—	NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	–0.5 *1 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –2.5 V for pulse width (under shoot) ≤ 10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{VE}$	V_{CC} current	I/O	Ref. cycle
H	X	X	I_{SB}, I_{SB1}	High-Z	—
L	H	H	I_{CC}	High-Z	—
L	L	H	I_{CC}	Output	Read cycle
L	X	L	I_{CC}	Input	Write cycle

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*2	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
	V_{IL}	–0.3 *1	—	0.8	V

Note: 1. –2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$V_{I/O}$ = V_{SS} to V_{CC}	1
Operating power supply current	I_{CC}	—	60	100	mA	25 ns cycle $\overline{CS}$ = V_{IL}, Iout = 0 mA Other inputs = V_{IH}/V_{IL}	
		—	50	90	mA	30 ns cycle	
		—	45	85	mA	35 ns cycle	
		—	40	80	mA	45 ns cycle	
Standby power supply current	I_{SB}	—	20	40	mA	25 ns cycle $\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}	
		—	18	35	mA	30 ns cycle	
		—	15	30	mA	35 ns cycle	
		—	13	25	mA	45 ns cycle	
Standby power supply current (1)	I_{SB1}	—	—	1	mA	$V_{CC} \geq \overline{CS} \geq V_{CC}$ – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or $V_{CC} \geq$ Vin ≥ V_{CC} – 0.2 V	
		—	—	0.06	mA		L-version
Output voltage	V_{OL1}	—	—	0.2	V	I_{OL1} = 0.1 mA	
	V_{OL2}	—	—	0.4	V	I_{OL2} = 2 mA	
	V_{OH1}	V_{CC} – 0.2	—	—	V	I_{OH1} = –0.1 mA	
	V_{OH2}	2.4	—	—	V	I_{OH2} = –2 mA	

Note: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

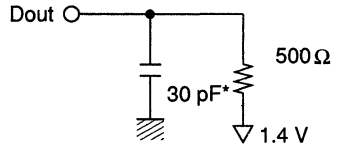
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

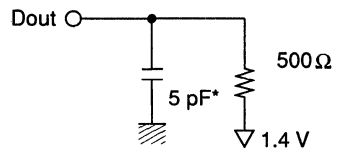
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 2.4 V/0.4 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures



Output load (A)



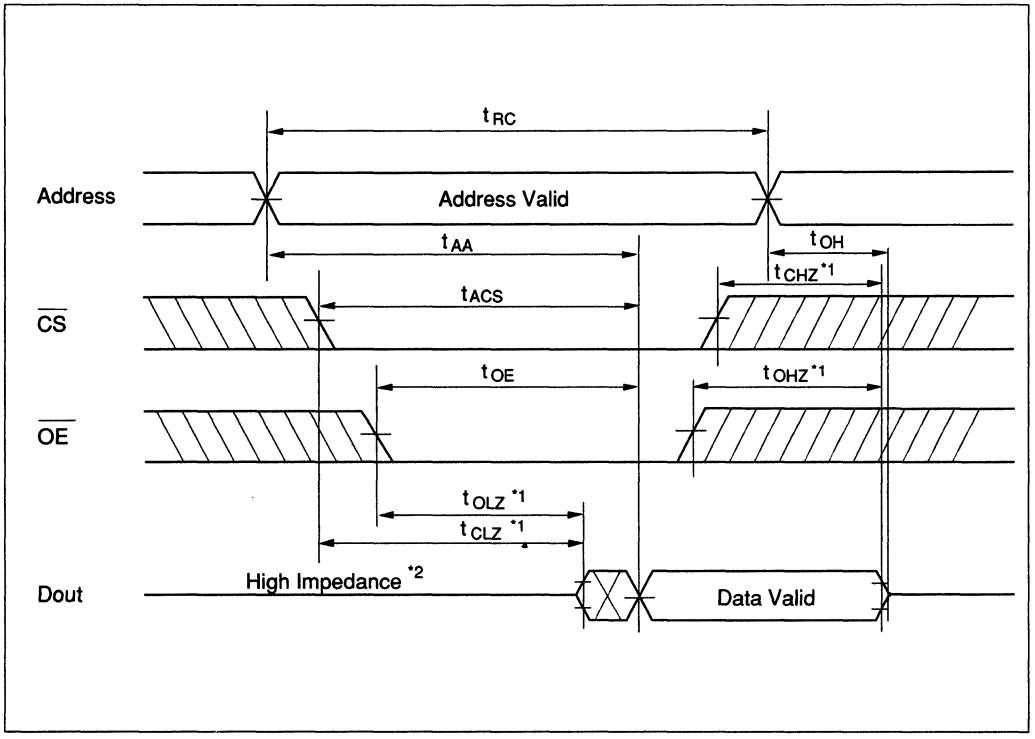
Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW})

* Including scope and jig

Read Cycle

		HM62W8127H/HM62W9127H								
		-25		-30		-35		-45		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Output enable to output valid	t_{OE}	—	15	—	15	—	20	—	25	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip select to output in low-Z	t_{CLZ}	5	—	5	—	5	—	5	—	ns
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	1	—	1	—	ns
Chip deselect to output in high-Z	t_{CHZ}	—	12	—	12	—	12	—	12	ns
Output disable to output in high-Z	t_{OHZ}	—	12	—	12	—	12	—	12	ns

Read Timing Waveform*3

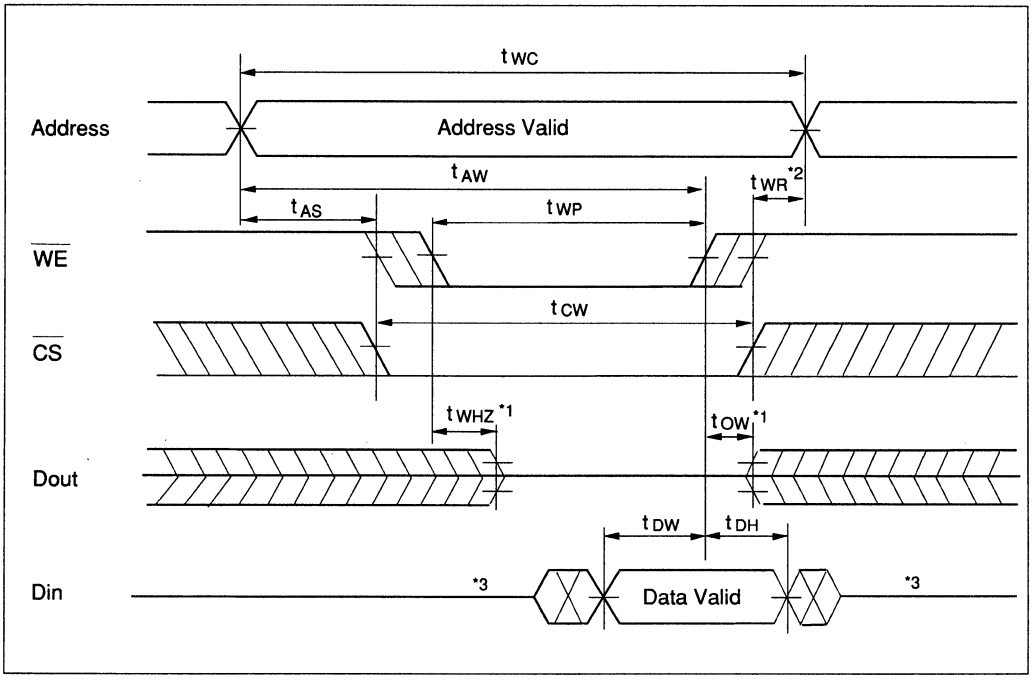


Notes: 1. Transition is measured ±200 mV from steady state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$ and $\overline{OE}$ are low, Dout is low impedance.
3. $\overline{WE}$ is high for read cycle.

Write Cycle

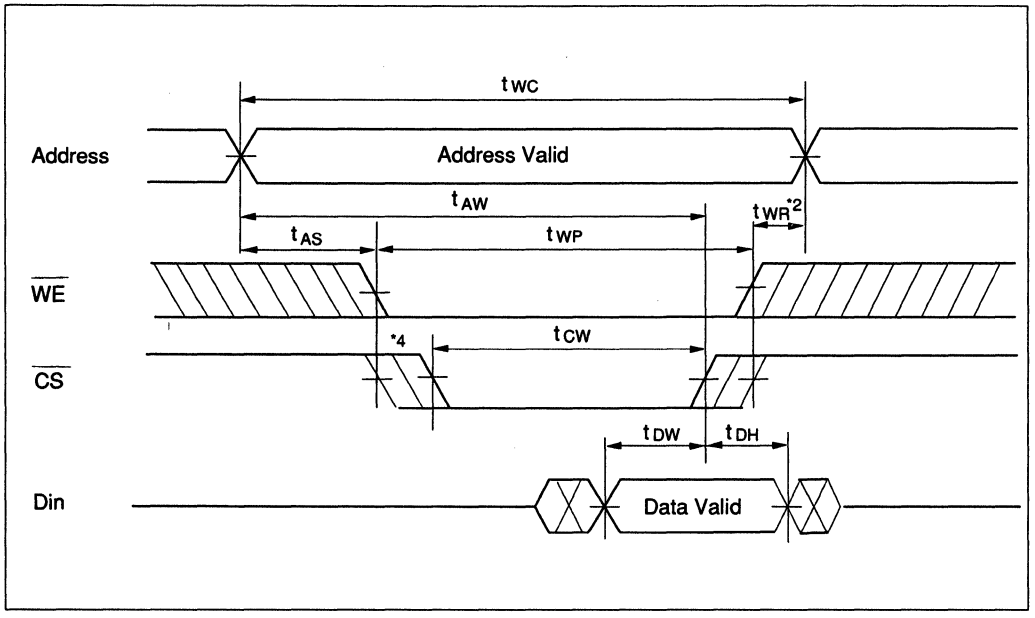
		HM62W8127H/HM62W9127H								
		-25		-30		-35		-45		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	25	—	30	—	35	—	45	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	25	—	30	—	ns
Chip select to end of write	t_{CW}	20	—	20	—	25	—	30	—	ns
Write pulse width	t_{WP}	20	—	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns
Data to write time overlap	t_{DW}	15	—	15	—	20	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write disable to output in low-Z	t_{OW}	5	—	5	—	5	—	5	—	ns
Write enable to output in high-Z	t_{WHZ}	—	12	—	12	—	12	—	12	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



3

Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes:
1. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampeld and not 100% tested.
2. $\overline{WE}$ must be high during transition except when the device is disabled with $\overline{CS}$.
3. If $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.

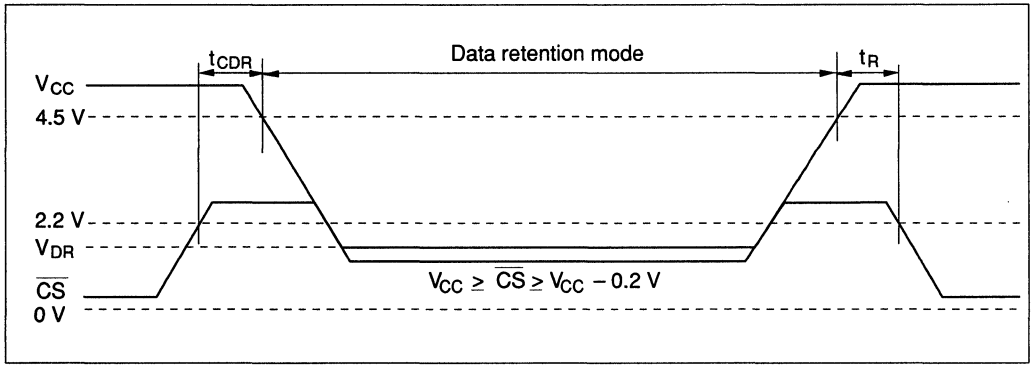
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0\ V \leq Vin \leq 0.2$ V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



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HM62W1664H Series
HM62W1864H Series

Preliminary

65536-word x 16/18-bit High Speed CMOS Static RAM

The HM62W1664H/HM62W1864H is an asyncronous 3.3 V operation high speed static RAM organized as 64 kword × 16/18 bit. It realize high speed access time (25/30/35/45 ns) with employing 0.8 µm CMOS process and high speed circuit designing technology.

It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.

The HM62W1664H/HM62W1864H is packaged in 400-mil 44-pin SOJ & TSOP-II for high density surface mounting.

Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time 25/30/35/45 ns (max)
- Completely static memory
  — No clock or timing strobe required
- Equal access and cycle times
- Directly CMOS compatible
  — All inputs and outputs
- 400-mil 44-pin SOJ & TSOP-II package
- Center V_{CC} and V_{SS} type pinout

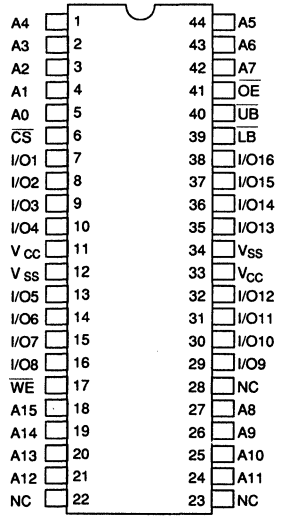
Ordering Information

Type No.	Access time	Package
HM62W1664HJP-25	25 ns	400-mil 44-pin plastic SOJ (CP-44D)
HM62W1664HJP-30	30 ns	
HM62W1664HJP-35	35 ns	
HM62W1664HJP-45	45 ns	
HM62W1664HLJP-25	25 ns	
HM62W1664HLJP-30	30 ns	
HM62W1664HLJP-35	35 ns	
HM62W1664HLJP-45	45 ns	
HM62W1864HJP-25	25 ns	
HM62W1864HJP-30	30 ns	
HM62W1864HJP-35	35 ns	
HM62W1864HJP-45	45 ns	
HM62W1864HLJP-25	25 ns	
HM62W1864HLJP-30	30 ns	
HM62W1864HLJP-35	35 ns	
HM62W1864HLJP-45	45 ns	
HM62W1664HTT-25	25 ns	400-mil 44-pin plastic TSOP-II normal bend type (TTP-44DE)
HM62W1664HTT-30	30 ns	
HM62W1664HTT-35	35 ns	
HM62W1664HTT-45	45 ns	
HM62W1664HLTT-25	25 ns	
HM62W1664HLTT-30	30 ns	
HM62W1664HLTT-35	35 ns	
HM62W1664HLTT-45	45 ns	
HM62W1864HTT-25	25 ns	
HM62W1864HTT-30	30 ns	
HM62W1864HTT-35	35 ns	
HM62W1864HTT-45	45 ns	
HM62W1864HLTT-25	25 ns	
HM62W1864HLTT-30	30 ns	
HM62W1864HLTT-35	35 ns	
HM62W1864HLTT-45	45 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

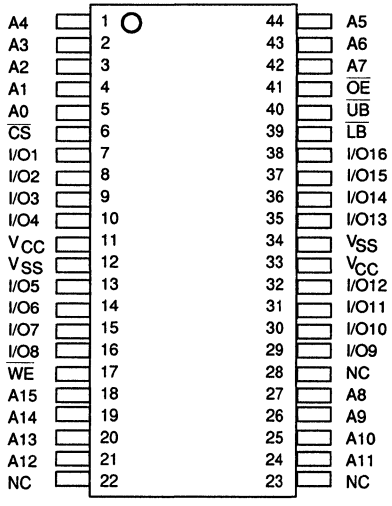
Pin Arrangement

HM62W1664HJP (SOJ)



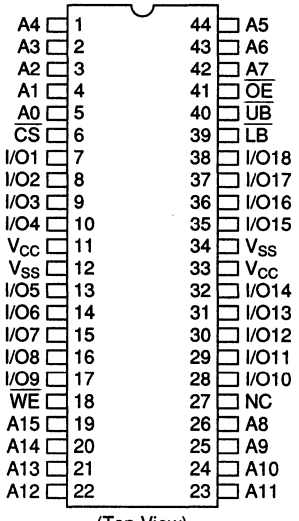
(Top View)

HM62W1664HTT
(Normal Bend TSOP-II)



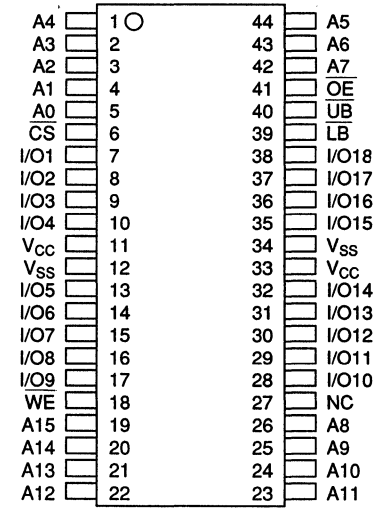
(Top View)

HM62W1864HJP (SOJ)



(Top View)

HM62W1864HTT
(Normal Bend TSOP-II)



(Top View)

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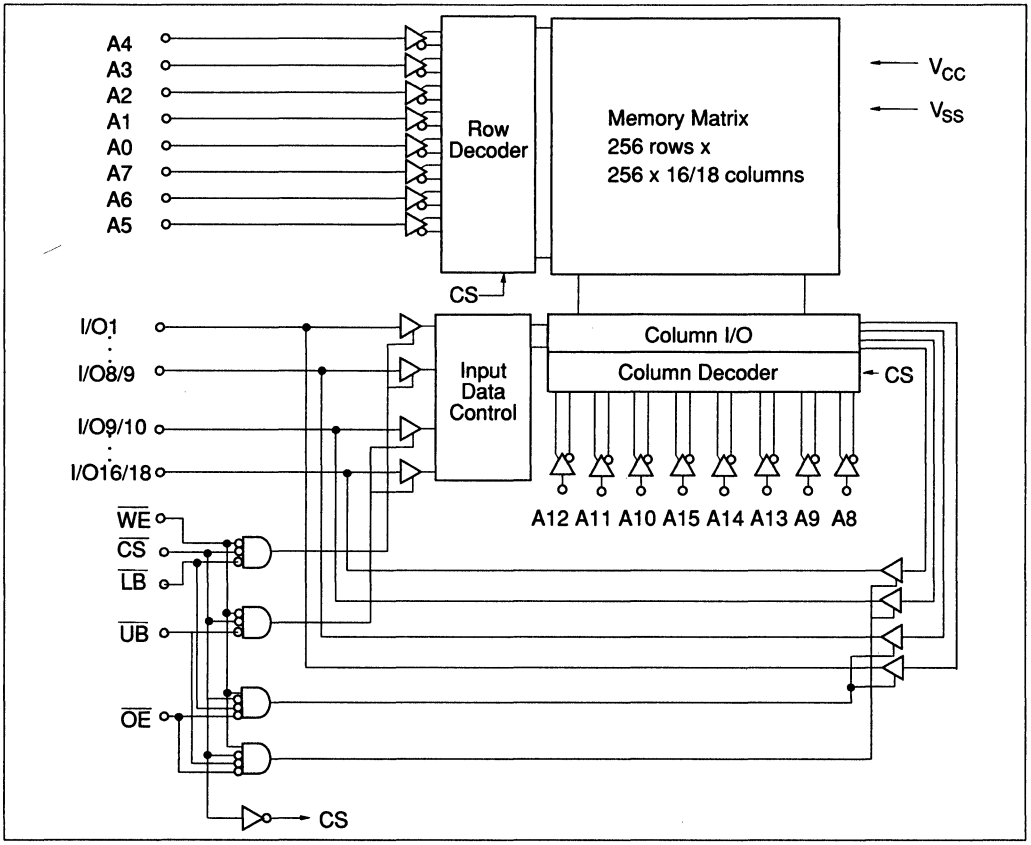
Pin Description

Pin name		
HM62W1664H	**HM62W1864H**	**Function**
A0 – A15	A0 – A15	Address
I/O1 – I/O8	I/O1 – I/O9	Input/output (lower byte)
I/O9 – I/O16	I/O10 – I/O18	Input/output (upper byte)
$\overline{CS}$	$\overline{CS}$	Chip select
$\overline{LB}$	$\overline{LB}$	Lower byte select
$\overline{UB}$	$\overline{UB}$	Upper byte select
$\overline{WE}$	$\overline{WE}$	Write enable
$\overline{OE}$	$\overline{OE}$	Output enable
V_{CC}	V_{CC}	Power supply
V_{SS}	V_{SS}	Ground
NC	NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	–0.5 *1 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –2.5 V for pulse width (under stoot) ≤ 10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	V_{CC} current	I/O (Lower byte)	I/O (Upper byte)	Ref. cycle
H	X	X	X	X	I_{SB}, I_{SB1}	High-Z	High-Z	—
L	H	H	X	X	I_{CC}	High-Z	High-Z	—
L	L	H	L	L	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	I_{CC}	High-Z	High-Z	—
L	X	L	L	L	I_{CC}	Input	Input	Write cycle
L	X	L	L	H	I_{CC}	Input	High-Z	Write cycle
L	X	L	H	L	I_{CC}	High-Z	Input	Write cycle
L	X	L	H	H	I_{CC}	High-Z	High-Z	—

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*2	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
	V_{IL}	–0.3 *1	—	0.8	V

Note: 1. –2.0 V for pulse width (under stoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$V_{I/O}$ = V_{SS} to V_{CC}	1
Operating power supply current	I_{CC}	—	90	120	mA	25 ns cycle	$\overline{CS}$ = V_{IL}, Iout = 0 mA, Other inputs = V_{IH}/V_{IL}
		—	80	110	mA	30 ns cycle	
		—	70	100	mA	35 ns cycle	
		—	60	90	mA	45 ns cycle	
Standby power supply current	I_{SB}	—	20	40	mA	25 ns cycle	$\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}
		—	18	35	mA	30 ns cycle	
		—	15	30	mA	35 ns cycle	
		—	13	25	mA	45 ns cycle	
Standby power supply current (1)	I_{SB1}	—	—	1	mA	V_{CC} ≥ $\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or	
		—	—	0.06	mA	V_{CC} ≥ Vin ≥ V_{CC} – 0.2 V	L-version
Output voltage	V_{OL1}	—	—	0.2	V	I_{OL1} = 0.1 mA	
	V_{OL2}	—	—	0.4	V	I_{OL2} = 2 mA	
	V_{OH1}	V_{CC} – 0.2	—	—	V	I_{OH1} = –0.1 mA	
	V_{OH2}	2.4	—	—	V	I_{OH2} = –2 mA	

Note: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

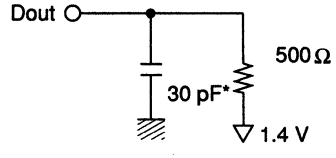
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

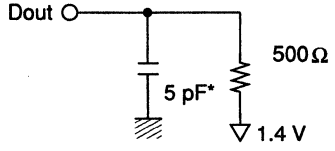
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 2.4 V / 0.4 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures



Output load (A)



Output load (B)

(for t_{CLZ}, t_{OLZ}, t_{LBLZ}, t_{UBLZ}, t_{CHZ}, t_{OHZ}, t_{LBHZ}, t_{UBHZ}, t_{WHZ}, and t_{OW})

* Including scope and jig

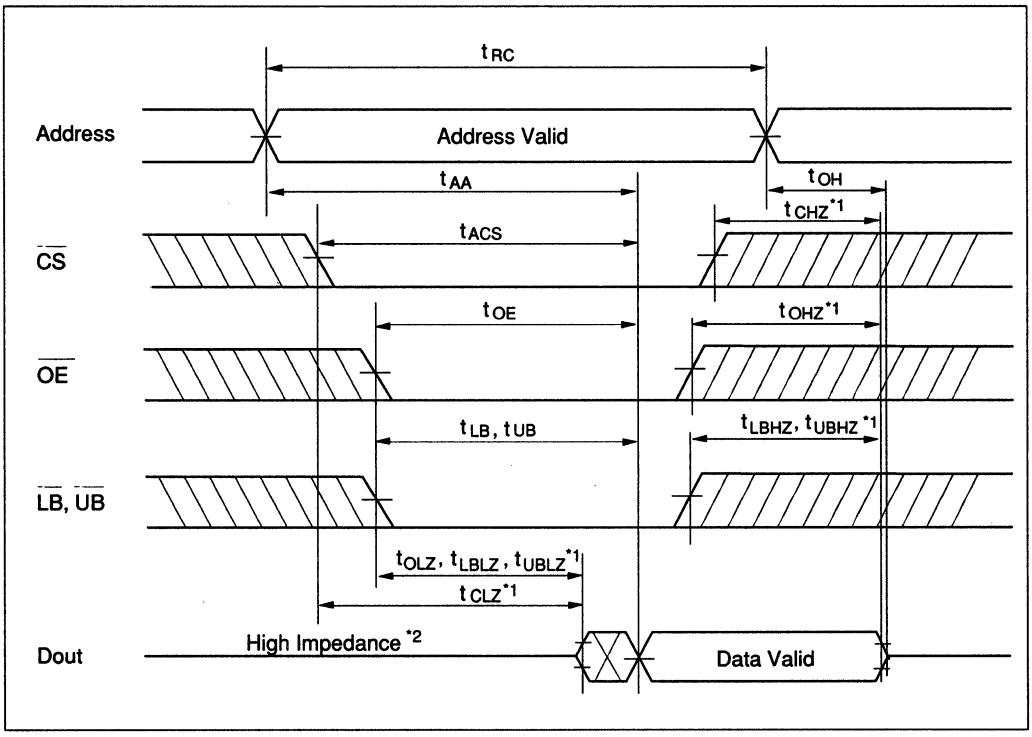
Read Cycle

		HM62W1664H/HM62W1864H								
		-25		-30		-35		-45		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Output enable to output valid	t_{OE}	—	15	—	15	—	20	—	25	ns
Byte select to output valid	t_{LB}, t_{UB}	—	15	—	15	—	20	—	25	ns
Output hold from address change	t_{OH}	5	—	5	—	—	5	—	ns	
Chip select to output in low-Z	t_{CLZ}	5	—	5	—	5	—	5	—	ns
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	1	—	1	—	ns
Byte select to output in low-Z	t_{LBLZ}, t_{UBLZ}	1	—	1	—	1	—	1	—	ns
Chip deselect to output in high-Z	t_{CHZ}	—	12	—	12	—	12	—	12	ns

Read Cycle (cont)

Parameter	Symbol	HM62W1664H/HM62W1864H								Unit
		-25		-30		-35		-45		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output disable to output in high-Z	t_{OHZ}	—	12	—	12	—	12	—	12	ns
Byte deselect to output in high-Z	t_{LBHZ}, t_{UBHZ}	—	12	—	12	—	12	—	12	ns

Read Timing Waveform *3

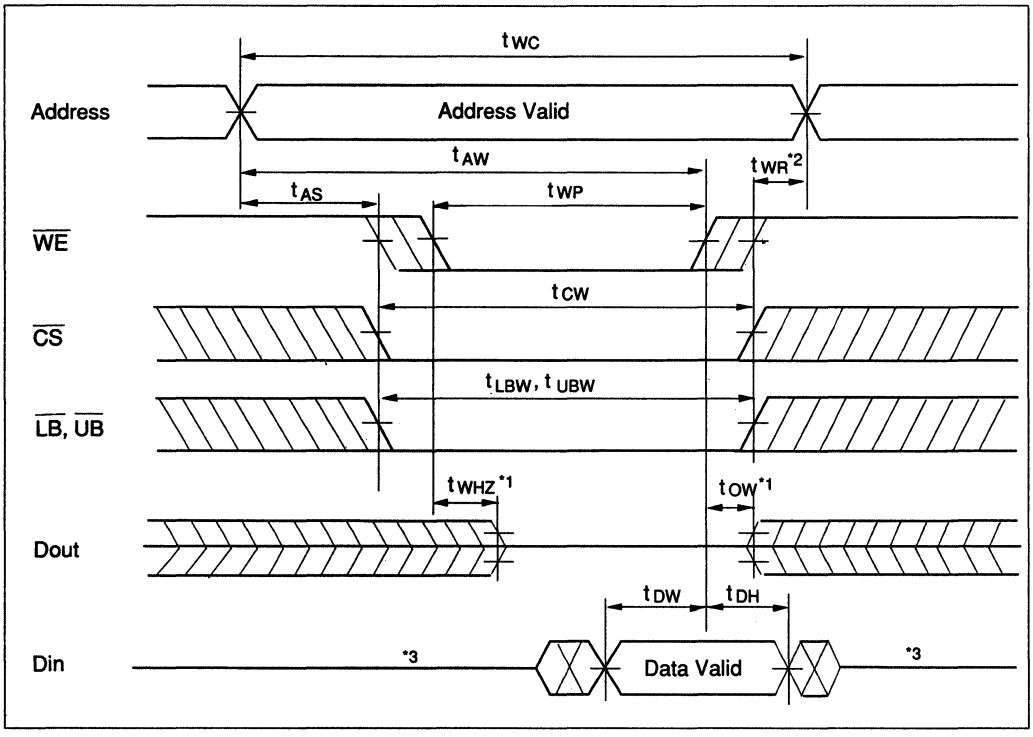


Notes: 1. Transition is measured ±200 mV from steady state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$, $\overline{OE}$, and $\overline{LB}$ are low, Dout (lower byte) is low impedance.
When $\overline{CS}$, $\overline{OE}$, and $\overline{UB}$ are low, Dout (upper byte) is low impedance.
3. $\overline{WE}$ is high for read cycle.

Write Cycle

		HM62W1664H/HM62W1864H								
		-25		-30		-35		-45		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t_{WC}	25	—	30	—	35	—	45	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	25	—	30	—	ns
Chip select to end of write	t_{CW}	20	—	20	—	25	—	30	—	ns
Write pulse width	t_{WP}	20	—	20	—	25	—	30	—	ns
Byte select to end of write	t_{LBW}, t_{UBW}	20	—	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns
Data to write time overlap	t_{DW}	15	—	15	—	20	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write disable to output in low-Z	t_{OW}	5	—	5	—	5	—	5	—	ns
Write enable to output in high-Z	t_{WHZ}	—	12	—	12	—	12	—	12	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



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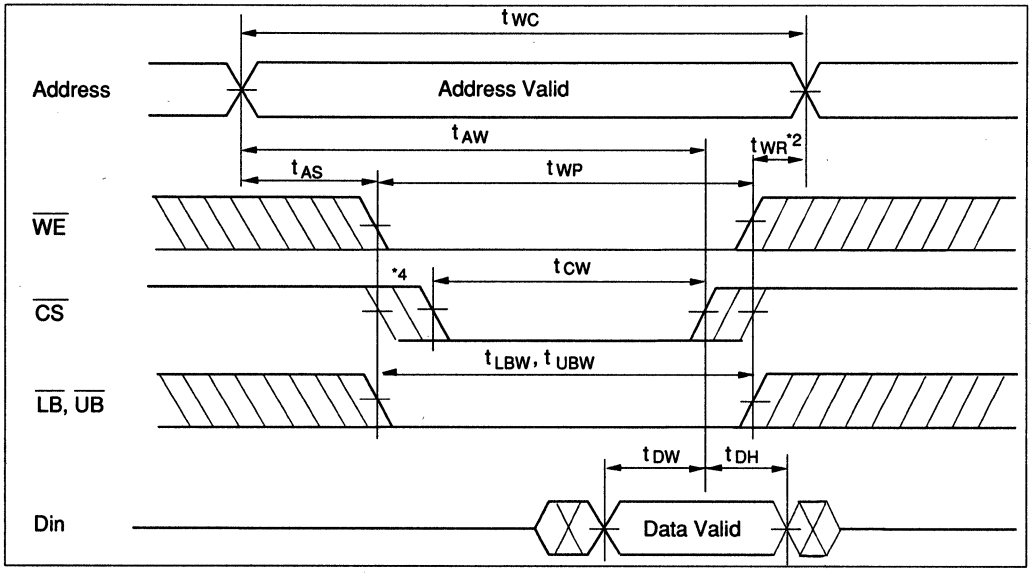
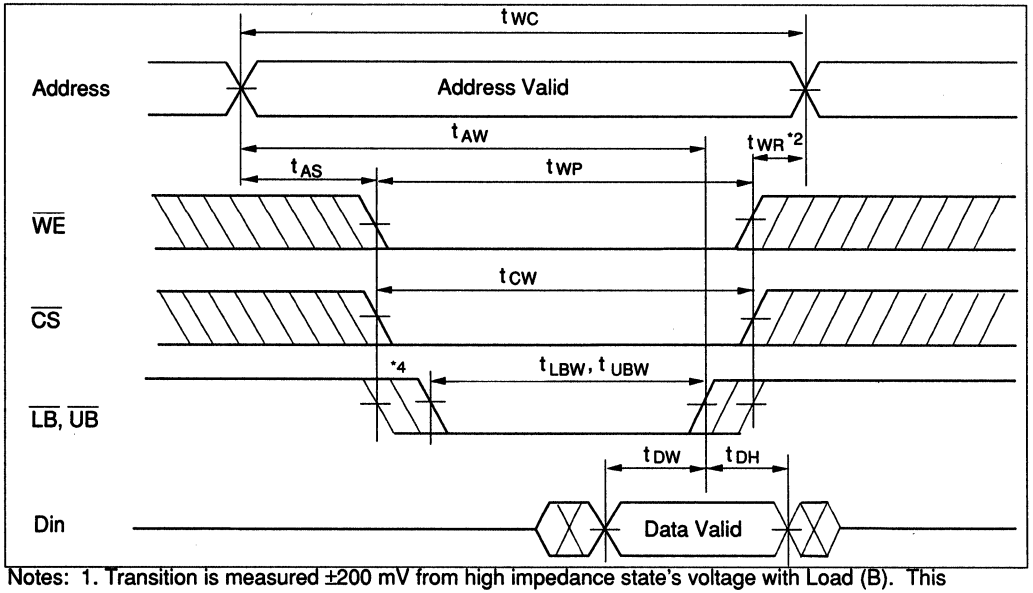
Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Write Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes: 1. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ must be high during address transition except when the device is disabled with $\overline{CS}$, $\overline{LB}$, or $\overline{UB}$.
3. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$ or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.

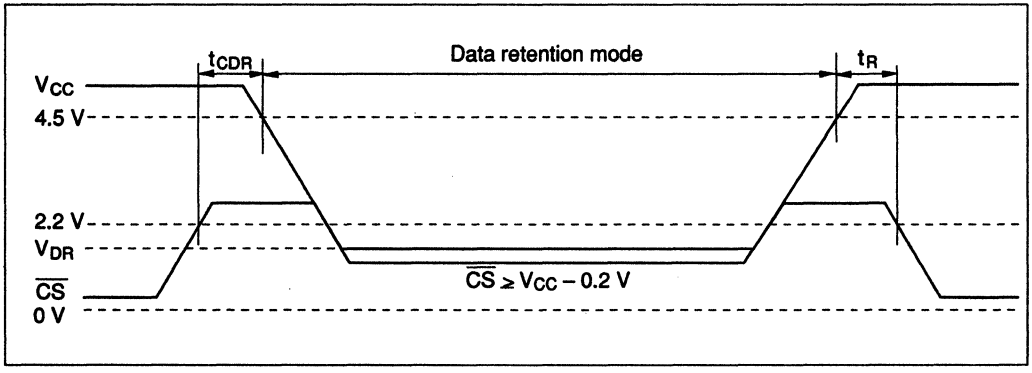
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0 V \leq Vin \leq 0.2$ V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



SECTION 4

APPLICATION SPECIFIC STATIC RAMs

HM67A4257 Series — Preliminary

262144-word × 4-bit I/O Separate Clocked Random Access Memory

Features

- 262144-word × 4-bit organization
- Directly TTL compatible input and output
- Choice of 5.0V or 3.3V power supply for output buffers
- Completely static memory
- Access time: from clock: 5/6ns (max)
- Cycle time: 10/12ns (min)
- Inputs registered on chip
- Outputs registed on chip
- Revolutional pin arrangement
- 400mil 36pin Plastic SOJ

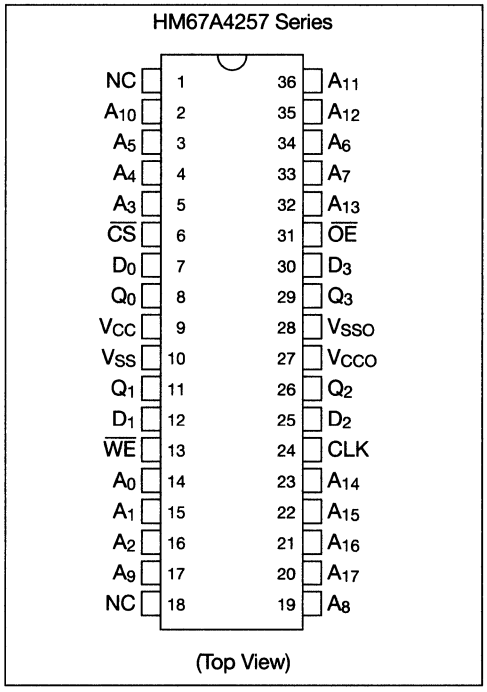
Ordering Information

Type No.	Organization	Access time	Package
HM67A4257JP-10 HM67A4257JP-12	256K×4	10ns 12ns	400mil 36pin Plastic SOJ) (CP-36DB)

Pin Description

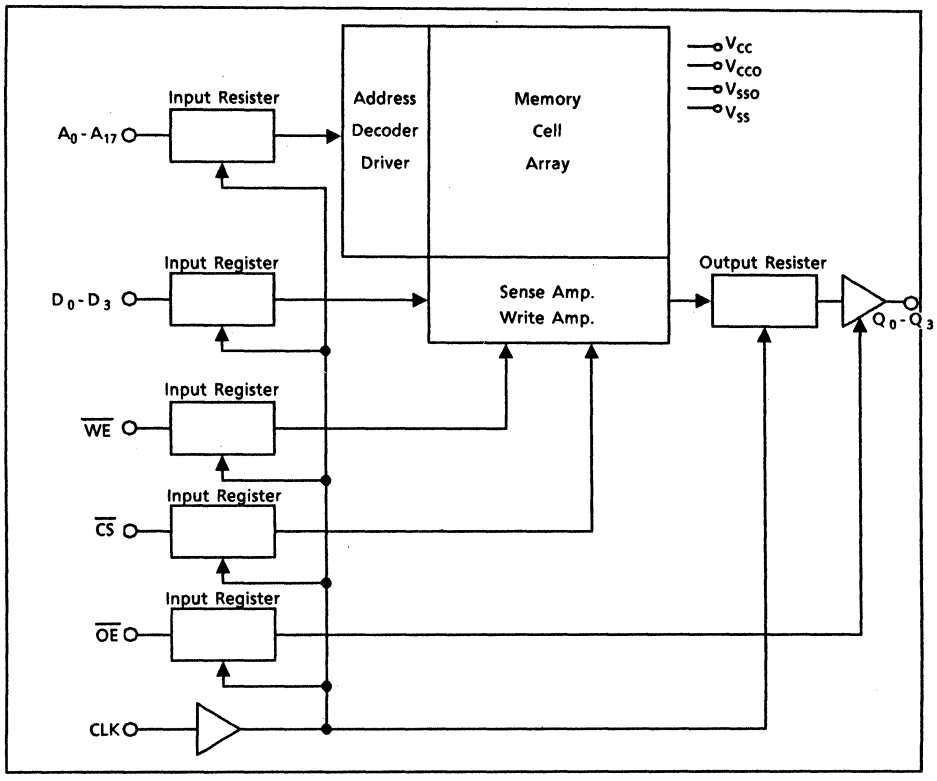
Pin Name	Function
A	Address Input
D	Data Input
Q	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
CLK	Clock Input
V_{CC}	+5V Power Supply
V_{CCO}	Output Buffer Power Supply
V_{SSO}	Output Buffer Ground
V_{SS}	Ground
NC	Not Connect

Pin Arrangement



Note: Product Preview: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

Block Diagram



Truth Table

Input			CLK	Mode	V_{CC} Current	Output	Ref. Cycle
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$					
H	X	X	⊓	Not Selected	I_{SB}, I_{SB1}	High Z	-
L	H	H	⊓	Output Disable	I_{CC}, I_{CC1}	High Z	-
L	H	L	⊓	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle
L	L	H	⊓	Write	I_{CC}, I_{CC1}	High Z	Write Cycle
L	L	L	⊓				

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage [1]	V_{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V_{SS} [1]	V_T	−0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg}(Bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Notes 1) With respect to $V_{SS} = V_{SSO}$

Under the dc and ac specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (0°C ≦ Ta ≦ 70°C)

Item		Symbol	min	typ	max	Unit
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
	5V TTL Compatible	V_{CCO}	4.5	5.0	5.5	V
	3.3V TTL Compatible		3.0	3.3	3.6	V
		V_{SS}, V_{SSI}	0.0	0.0	0.0	V
Input High Voltage		V_{IH}	2.2	-	V_{CC} + 0.5	V
Input Low Voltage		V_{IL}	-1.0	-	0.8	V

DC and Operating Characteristics

(V_{CC} = 5.0 V ±10%, V_{CCO} = 5.0V ±10% or 3.3 V ±0.3V, $V_{SS} = V_{SSO}$ = 0 V, Ta = 0 to +70°C)

Item	Symbol	Test Conditions	-10		-12		Unit
			min	max	min	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	-	2	-	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 V to V_{CCO}	-	10	-	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	-	120	-	120	mA
Average Operating Current	I_{CC1}	min. cycle, $I_{I/O}$ = 0 mA	-	200	-	190	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	-	40	-	40	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} - 0.2 V V_{IN} ≦ 0.2 V or V_{IN} ≧ V_{CC} - 0.2 V	-	30	-	30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	-	0.4	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = - 4 mA	2.4	-	2.4	-	V

4

AC Characteristics

(V_{CC} = 5.0 V ± 10%, V_{CCO} = 5.0V ± 10% or 3.3V ± 0.3V, V_{SS} = V_{SSO} = 0 V, Ta = 0°C to 70°C, unless otherwise noted.)

- **Read and Write Cycle**

Item	Symbol	-10		-12		Unit
		min	max	min	max	
Clock Pulse Width "H"	t_{WH}	4	-	5	-	ns
Clock Pulse Width "L"	t_{WL}	4	-	5	-	ns
Cycle Time	t_{CYC}	10	-	12	-	ns
Address Setup Time	t_{SA}	2	-	2	-	ns
Address Hold Time	t_{HA}	2	-	2	-	ns
Chip Select Setup Time	t_{SCS}	2	-	2	-	ns
Chip Select Hold Time	t_{HCS}	2	-	2	-	ns
Write Enable Setup Time	t_{SWE}	2	-	2	-	ns
Write Enable Hold Time	t_{HWE}	2	-	2	-	ns
Output Enable Setup Time	t_{SOE}	2	-	2	-	ns
Output Enable Hold Time	t_{HOE}	2	-	2	-	ns
Clock to Output in High Z	t_{CHZ} [1]	-	5	-	6	ns
Data Setup Time	t_{SDI}	2	-	2	-	ns
Data Hold Time	t_{HDI}	2	-	2	-	ns
Output Delay Time	t_{DR}	-	5	-	6	ns

Notes 1) Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

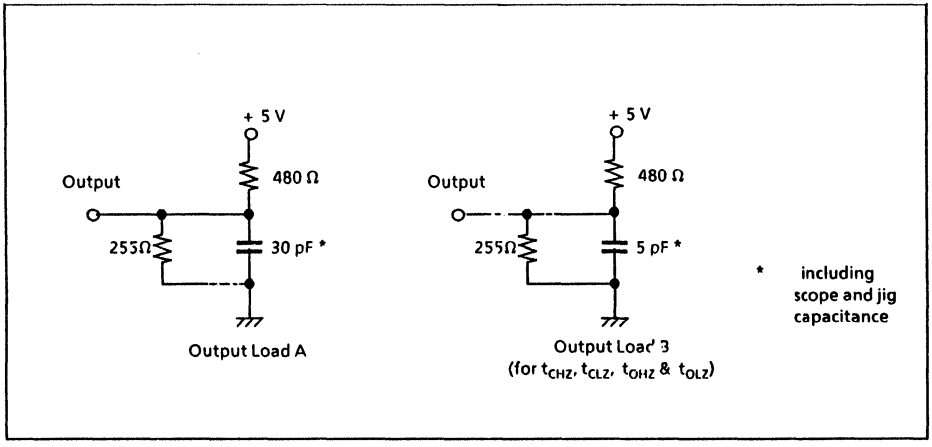
Capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	max	Unit	Test Condition
Input Capacitance	C_{IN} 1)	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT} 1)	10	pF	V = 0 V

Notes 1) This parameter is sampled and not 100% tested.

AC Test Conditions

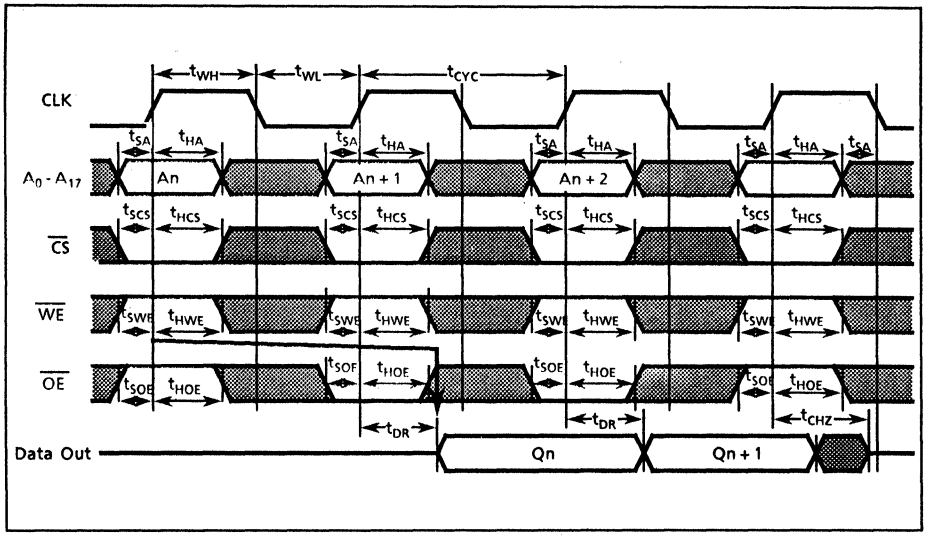
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5 V



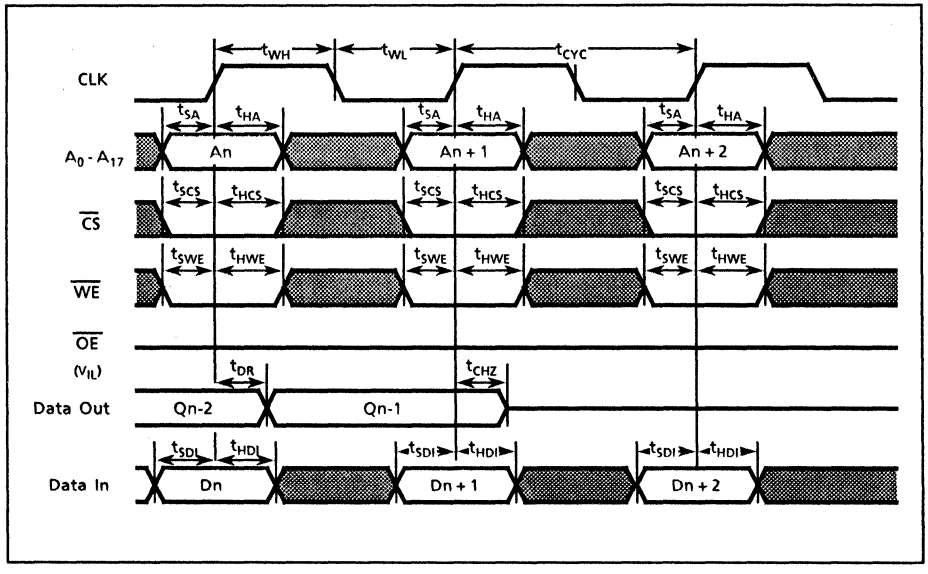
4

Timing Waveforms

Read Cycle



Write Cycle



HM62A9128/8128 Series

131072-word × 9 (8)-bit Synchronous Cache SRAM

Features

- For high speed cache memory applications
- Pipeline access capability with on-chip address, strobe and I/O resisters
- Organization: 128 kword × 9(8) bit
- SOJ - 32-pin
- TTL I/O

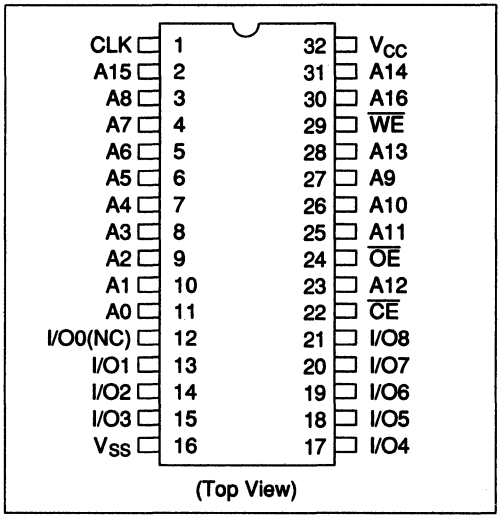
Main Characteristics

Item	Spec.	Remarks
Clock cycle time	20 ns (min)	
Clock to data valid	10 ns (max)	
Power dissipation	825 mW (max)	50 MHz

Ordering Information

Type No.	Clock cycle time	Package
HM62A9128JP–20	20 ns	32-pin SOJ (CP-32D)
HM62A8128JP–20	20 ns	

Pin Arrangement



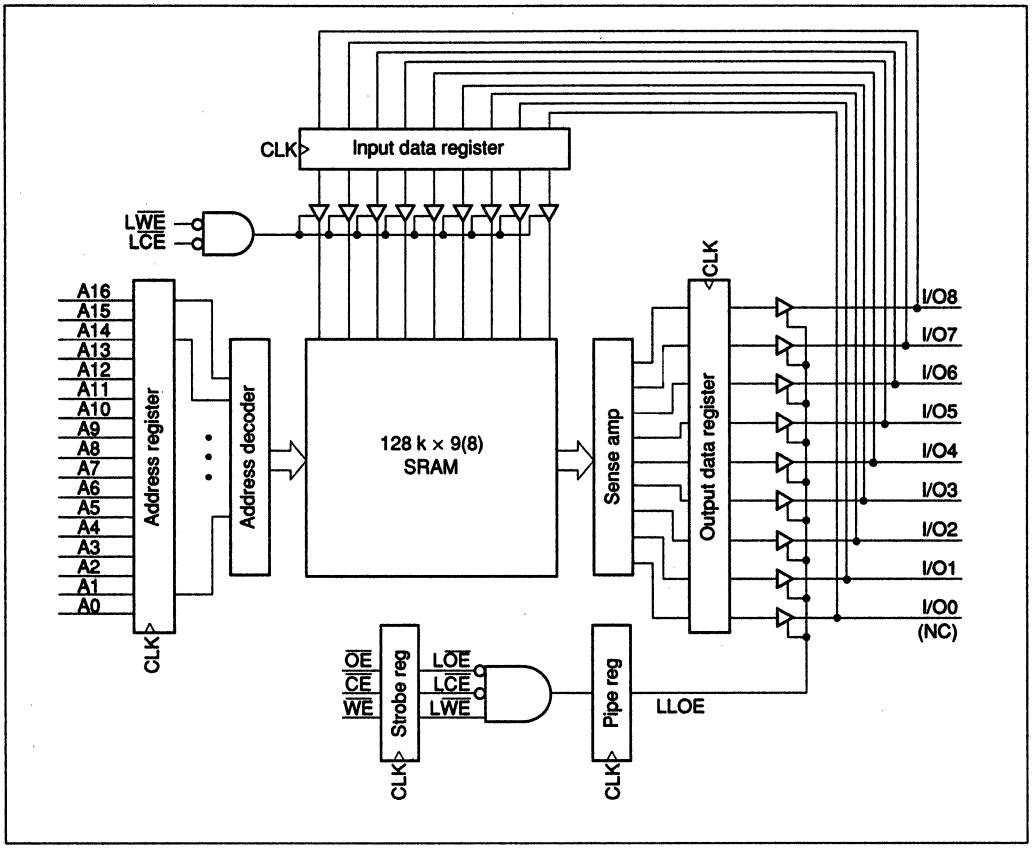
(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O8	Input/output
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
CLK	Clock input
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection (for × 8)

4

Block Diagram



Function Table

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Din	CLK	SRAM mode	Next cycle Dout	Ref. cycle
H	X	X	X	↗	Not selected	High-Z	Read cycle
L	H	H	X	↗	Not selected	High-Z	
L	L	H	X	↗	Read	Read data	Read cycle
L	H	L	Data	↗	Write	High-Z	Write cycle
L	L	L	Data	↗	Write	High-Z	

Note: 1. After power-on (V_{CC} in specification),CLK will be active for 10 cycles before any operation starts.
2. $\overline{CE}$,$\overline{OE}$ and $\overline{WE}$ will be in specification for at least 2 cycles before the first operation starts.
3. When the write after the read, the wait status more than 2cycles should be inserted due to the avoidance of data collision.

Registers

CLK	Mode	Register output
↗	Load	Register input
L or H	Hold	Not changed

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.2	—	6.0	V	
	V_{IL}	–0.5	—	0.8	V	1

Note: 1. –2.0 V for pulse width ≤ 10 ns

4

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	µA	Dout High-Z state $V_{I/O}$ = V_{SS} to V_{CC}
Average operating current	I_{CC1}	—	—	150	mA	Min. cycle, $\overline{CE}$= V_{IL} Duty: 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	110	mA	CLK ≤ V_{IL}, Min. cycle
	I_{SB1}	—	—	10	mA	Power standby, CLK ≤ 0.2 V, $\overline{CE}$≥V_{CC} – 0.2 V Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1.0 MHz)

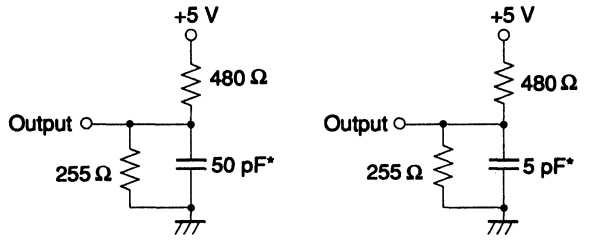
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 2 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figure



Output Load (A)

Output Load (B) (for t_{HZ}, t_{LZ})

*Including scope and jig capacitance

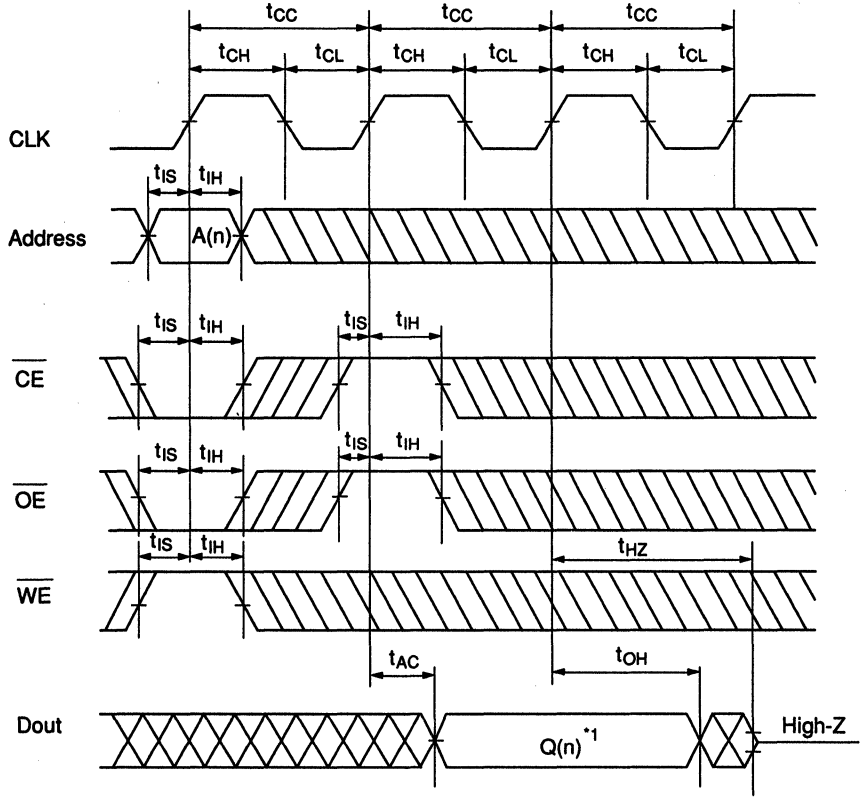
Read and Write Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Clock cycle time	t_{CC}	20	—	ns	3
Clock high pulse width	t_{CH}	5	—	ns	
Clock low pulse width	t_{CL}	5	—	ns	
Input setup time (address, data, strobes)	t_{IS}	3	—	ns	
Input hold time (address, data, strobes)	t_{IH}	1	—	ns	
Clock to output data valid	t_{AC}	—	10	ns	
Output data hold from clock	t_{OH}	3	—	ns	
Clock to output in Low-Z	t_{LZ}	0	—	ns	1, 2
Clock to output in High-Z	t_{HZ}	—	10	ns	1, 2

Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.
3. The rise time and fall time of CLK: 10 ns(max.)

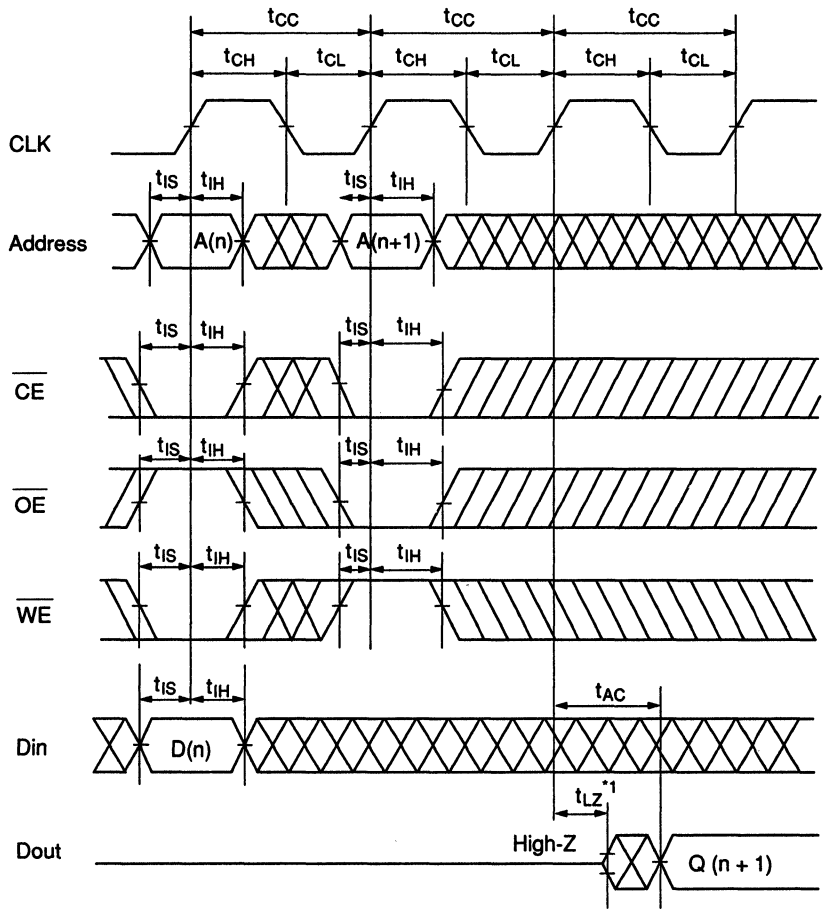
Timing Waveforms

Read Cycle



Notes: 1. Read data is valid on next cycle.
2. High impedance state is obtained on next cycle from $\overline{CE}$ = H, $\overline{OE}$ = H, or $\overline{WE}$ = L

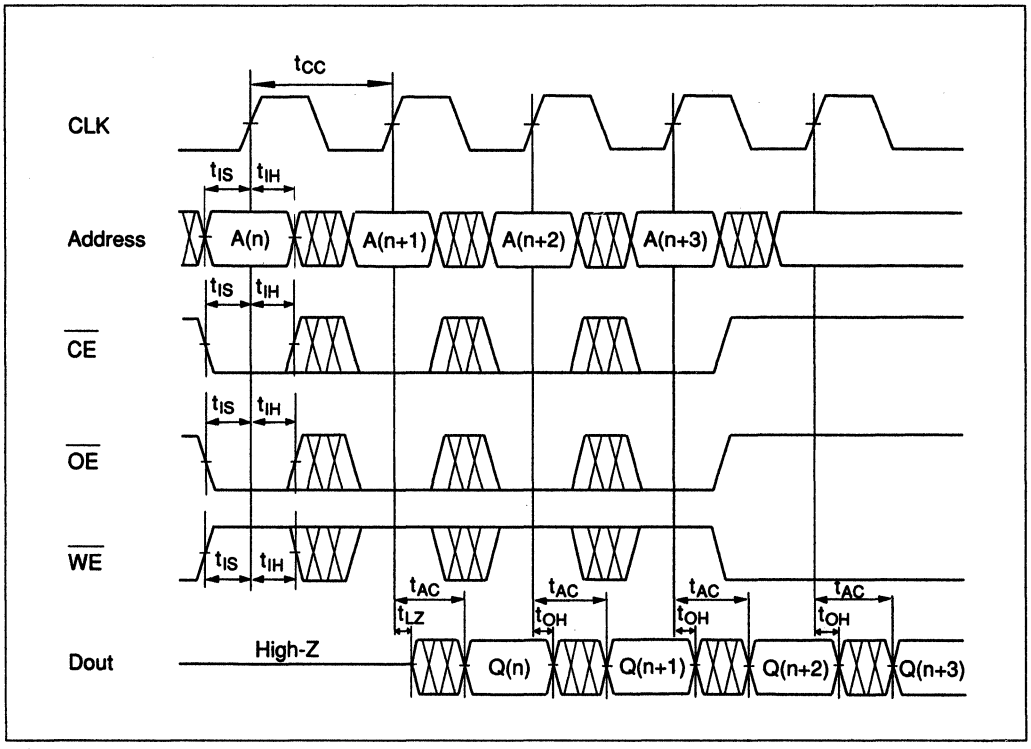
Write/Read Cycle



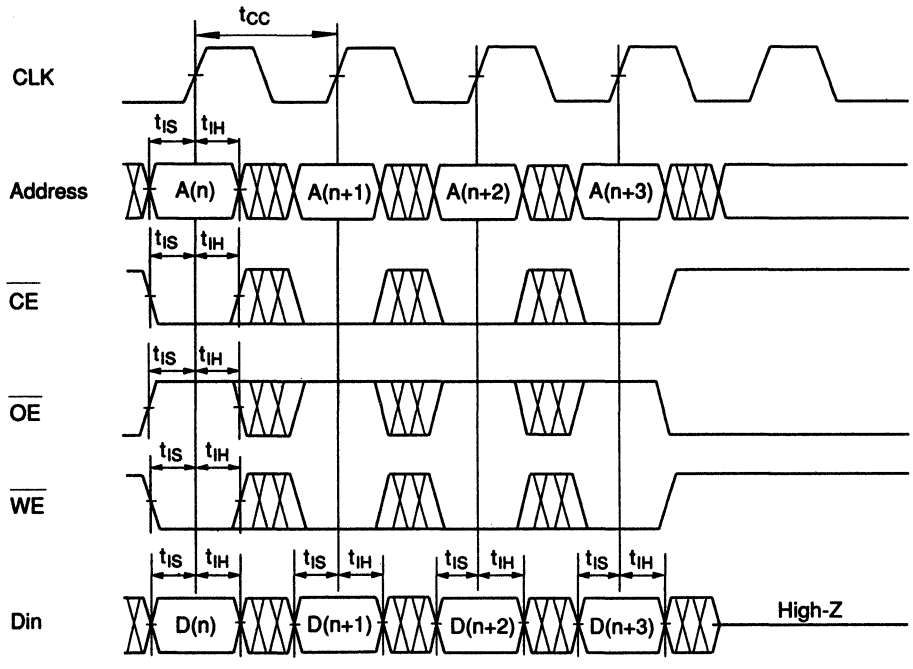
Notes: 1. Low impedance state is obtained on next cycle from $\overline{OE}$ = L, $\overline{CE}$ = L, and $\overline{WE}$ = H.

4

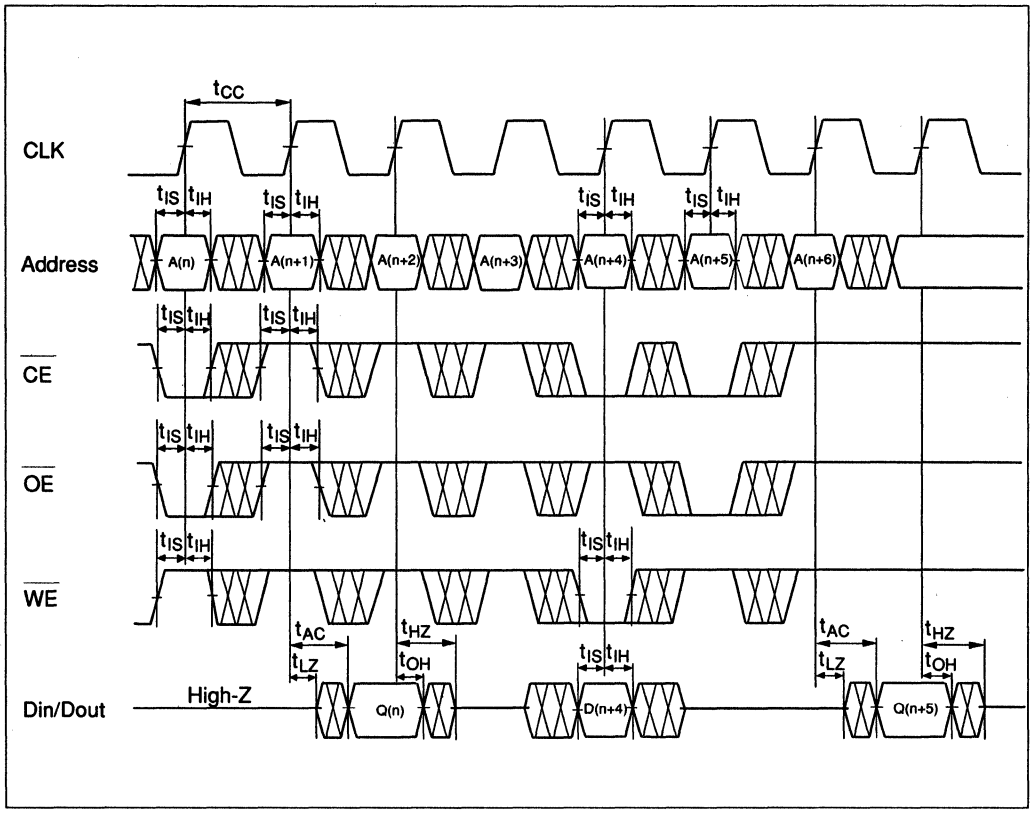
Pipelined Read Cycle



Pipelined Write Cycle



Alternate Read/Write/Read Cycle



HM67A4101 Series — Under development

1048576-words x 4-bits I/O Separate Clocked Random Access Memory

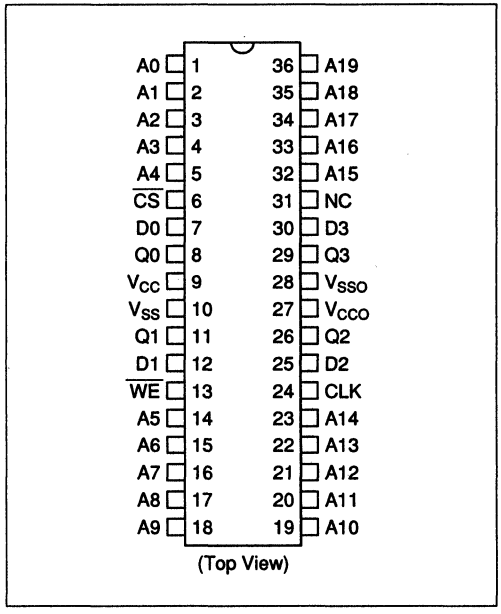
Features

- 1048576-words x 4-bits organization
- Directly TTL compatible input and output
- Choice of 5.0 V or 3.3 V power supplies for output buffers
- Completely static memory
- Access time from clock: 8 ns (max)
- Cycle time: 15 ns/18 ns (min)
- Inputs registered on chip
- Outputs registered on chip
- Revolutional pin arrangement
- 400 mil 36 pin Plastic SOJ or TSOP (II)

Ordering Informations

Type No.	Cycle time	Package
HM67A4101JP-15	15 ns	400 mil 36-pin SOJ (CP-36DB)
HM67A4101JP-18	18 ns	
HM67A4101TT-15	15 ns	400 mil 36-pin TSOP (II) (TTP-36DA)
HM67A4101TT-18	18 ns	

Pin Arrangement



4

Note: This document contains information on a product under development.
Hitachi reserves the right to change or discontinue the product without notice.

Pin Description

Pin name	Function
A0–A19	Address input
D0–D3	Data input
Q0–Q3	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
NC	No connection
CLK	Clock input
V_{CC}	+5 V power supply
V_{CCO}	Output buffer power supply
V_{SSO}	Output buffer ground
V_{SS}	Ground

524,288-word × 8/9-bit High Speed Synchronous Static Access Memory

Description

The HM67A8/9512 series is Hitachi's new 4Mb synchronous Fast Static RAM with a 524,288-word × 8/9 bit organization. The HM67A8/9512 has a super fast access time of 10/12ns. This series is manufactured on Hitachi's advanced 0.5μm production lines using Bi-CMOS technology.

Features

- 524,288-word × 8/9-bit organization
- Super fast cycle time 10/12ns
- Single 5.0V power supply
- V_{CCO}: 5.0V or 3.3V option
- Low power dissipation
- 0.5 μm Bi-CMOS technology
- Surface mount package

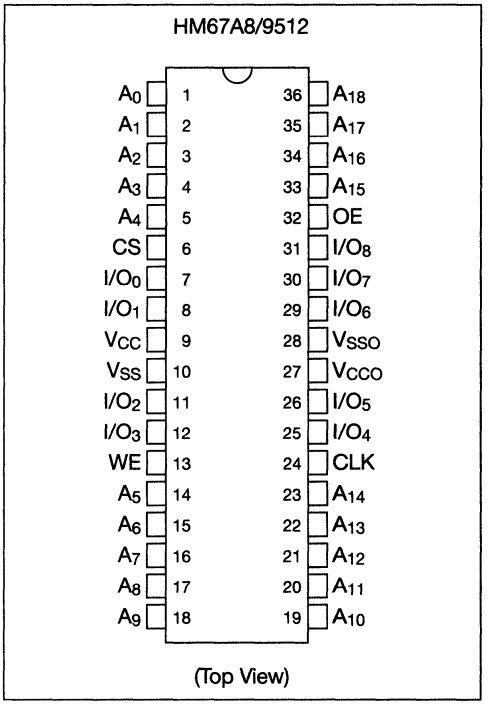
Ordering Information

512K × 8 Type No.	Access time	Package
HM67A8512-10	10ns	400mil 36 pin SOJ
HM67A8512-12	12ns	
HM67A8512-15	15ns	
HM67A9512-10	10ns	400mil 36 pin SOJ
HM67A9512-12	12ns	
HM67A9512-15	15ns	

Pin Description

Pin Name	Function
A	Address Input
I/O	Data Input/Output
WE	Byte Write Enable
CS	Chip Select
CLK	Clock
OE	Output Enable
V_{CC}, V_{CCO}	+3.3V power supply
V_{SS}, V_{SSO}	Ground

Pin Arrangement



Note: Product Preview: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

SECTION 5

MEDIUM SPEED
BYTE WIDE STATIC RAMs

- 5.0 V Supply
- 3.0 V & 3.3 V Supply

HM6264A Series

5.0 V Supply

8192-word × 8-bit High Speed CMOS Static RAM

Features

- Low-power standby
  - 0.1 mW (typ)
  - 10 µW (typ) L-/LL-version
- Low power operation
  - 15 mW/MHz (typ)
- Fast access time
  - 100/120/150 ns (max)
- Single +5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle time
- Common data input and output, three-state output
- Directly TTL compatible
  - All inputs and outputs
- Battery back up operation capability (L-/LL-version)

Ordering Information

Type No.	Access time	Package
HM6264AP-10	100 ns	600-mil, 28-pin plastic DIP (DP-28)
HM6264AP-12	120 ns	
HM6264AP-15	150 ns	
HM6264ALP-10	100 ns	
HM6264ALP-12	120 ns	
HM6264ALP-15	150 ns	
HM6264ALP-10L	100 ns	
HM6264ALP-12L	120 ns	
HM6264ALP-15L	150 ns	
HM6264ASP-10	100 ns	300-mil, 28-pin plastic DIP (DP-28N)
HM6264ASP-12	120 ns	
HM6264ASP-15	150 ns	
HM6264ALSP-10	100 ns	
HM6264ALSP-12	120 ns	
HM6264ALSP-15	150 ns	
HM6264ALSP-10L	100 ns	
HM6264ALSP-12L	120 ns	
HM6264ALSP-15L	150 ns	
HM6264AFP-10	100 ns	28-pin plastic SOP *1 (FP-28D/DA)
HM6264AFP-12	120 ns	
HM6264AFP-15	150 ns	
HM6264ALFP-10	100 ns	
HM6264ALFP-12	120 ns	
HM6264ALFP-15	150 ns	
HM6264ALFP-10L	100 ns	
HM6264ALFP-12L	120 ns	
HM6264ALFP-15L	150 ns	

Note: 1. T is added to the end of the type number for a SOP of 3.00 mm (max) thickness.

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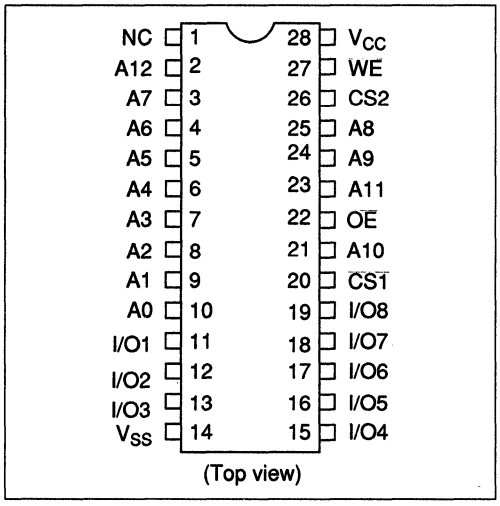
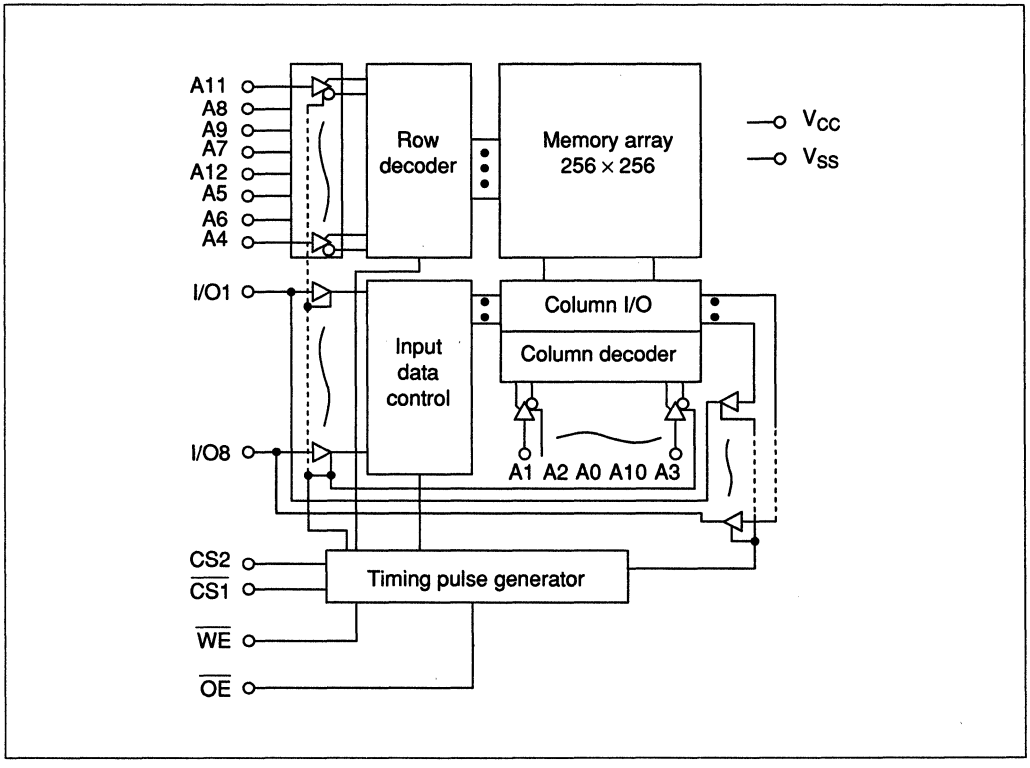
Pin Arrangement



Block Diagram



Truth Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	I/O pin	V_{CC} current	Note
×	H	×	×	Not selected (power down)	High Z	I_{SB}, I_{SB1}	
×	×	L	×		High Z	I_{SB}, I_{SB1}	
H	L	H	H	Output disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read cycle
L	L	H	H	Write	Din	I_{CC}	Write cycle 1
L	L	H	L	Write	Din	I_{CC}	Write cycle 2

×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage *1	V_T	–0.5 *2 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature (under bias)	Tbias	–10 to +85	°C

Notes: 1. With respect to V_{SS}.
2. –3.0 V for pulse width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.3 *1	—	0.8	V

Note: 1. –3.0 V for pulse width ≤ 50 ns

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DC and Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CCDC}	—	7	15	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	30	45*5	mA	Min. cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA
		—	30	55*6		
	I_{CC2}	—	3	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}
	I_{SB1} *2	—	0.02	2	mA	$\overline{CS1}$ ≥ Vcc – 0.2 V, CS2 ≥ Vcc – 0.2 V or
		—	2*3	100*3	µA	0 V ≤ CS2 ≤ 0.2 V, 0 V ≤ Vin
		—	2*4	50*4		
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes:
1. Typical values are at V_{CC} = 5.0 V, Ta = 25°C and not guaranteed.
2. V_{IL} min = –0.3 V
3. These characteristics are guaranteed only for the L-version.
4. These characteristics are guaranteed only for the LL-version.
5. For 120 ns/150 ns version.
6. For 100 ns version.

Capacitance (f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	5	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	7	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and is not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

AC Test Conditions:

- Input pulse levels: 0.8 V/2.4 V
- Input rise and fall time: 10 ns
- Input timing reference level: 1.5 V
- Output timing reference level
  - — HM6264A-10: 1.5 V
  - — HM6264A-12/15: 0.8 V/2.0 V
- Output load: 1 TTL gate and C_L (100 pF) (including scope and jig)

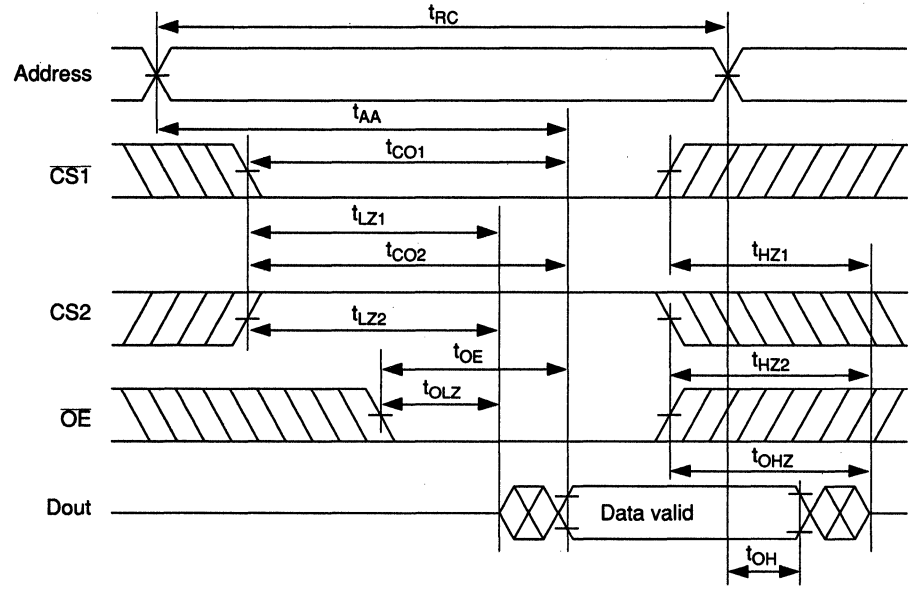
Read Cycle

			HM6264A-10		HM6264A-12		HM6264A-15		
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time		t_{RC}	100	—	120	—	150	—	ns
Address access time		t_{AA}	—	100	—	120	—	150	ns
Chip selection to output	$\overline{CS1}$	t_{CO1}	—	100	—	120	—	150	ns
	CS2	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid		t_{OE}	—	50	—	60	—	70	ns
Chip selection to output in low Z	$\overline{CS1}$	t_{LZ1}	10	—	10	—	15	—	ns
	CS2	t_{LZ2}	10	—	10	—	15	—	ns
Output enable to output in low Z		t_{OLZ}	5	—	5	—	5	—	ns
Chip deselection to output in high Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output disable to output in high Z		t_{OHZ}	0	35	0	40	0	50	ns
Output hold from address change		t_{OH}	10	—	10	—	10	—	ns

Notes
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs to achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.

5

Read Timing Waveform

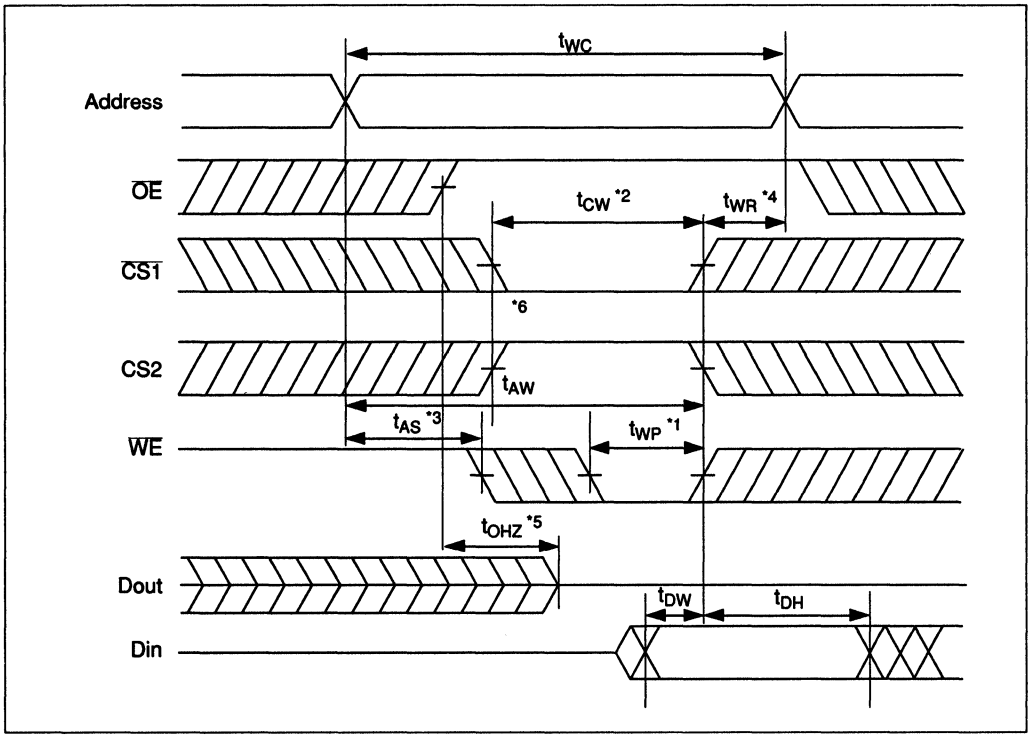


Note: $\overline{WE}$ is high for read cycle.

Write Cycle

		HM6264A-10		HM6264A-12		HM6264A-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Chip selection to end of write	t_{CW}	80	—	85	—	100	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address valid to end of write	t_{AW}	80	—	85	—	100	—	ns
Write pulse width	t_{WP}	60	—	70	—	90	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Write to output in high Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to write time overlap	t_{DW}	40	—	40	—	50	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output enable to output in high Z	t_{OHZ}	0	35	0	40	0	50	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{OE}$ Clock)



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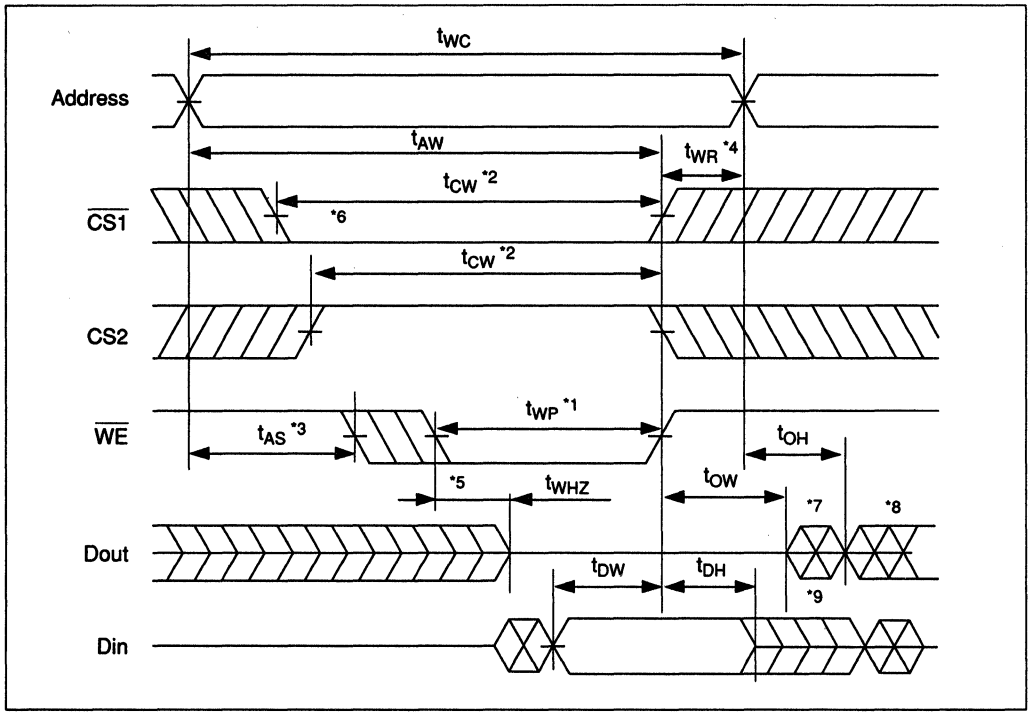
Write Timing Waveform (2) ($\overline{OE}$ Low Fix)



Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. Time t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of the write cycle.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ goes low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of the next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Input signals of opposite phase to the outputs must not be applied to I/O pins

Low V_{CC} Data Retention

In data retention mode, CS2 controls the address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$, and the Din buffer. If CS2 controls data retention mode, Vin (for these inputs) can be in the high impedance state. If CS1 controls the data retention mode, CS2 must satisfy either CS2 ≥ V_{CC} – 0.2 V or CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

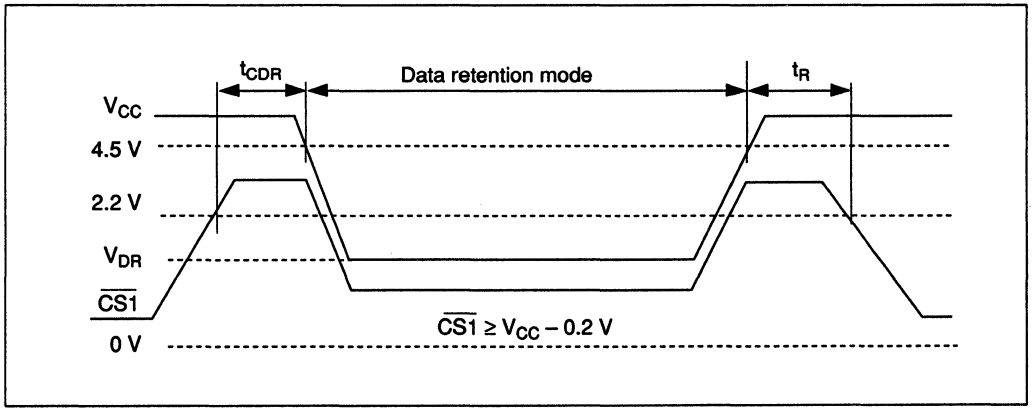
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only L/LL-version.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	$\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC}– 0.2 V, or CS2 ≤ 0.2 V	2.0	—	—	V
Data retention current	I_{CCDR}	V_{CC} = 3.0 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V, or 0 V ≤ CS2 ≤ 0.2 V, 0 V ≤ Vin	—	1*1	50*1	µA
			—	1*2	25*2	
Chip deselect to data retention time	t_{CDR}	See retention waveform	0	—	—	ns
Operation recovery time	t_R	See retention waveform	t_{RC}*3	—	—	ns

Notes: 1. V_{IL} min = –0.3 V, 20 µA max at Ta = 0 to 40°C. These characteristics are guaranteed only for the L-version.
2. V_{IL} min = –0.3 V, 10 µA max at Ta = 0 to 40°C. These characteristics are guaranteed only for the LL-version.
3. t_{RC} = Read cycle time.

Low V_{CC} Data Retention Waveform (1) ($\overline{CS1}$ Controlled)



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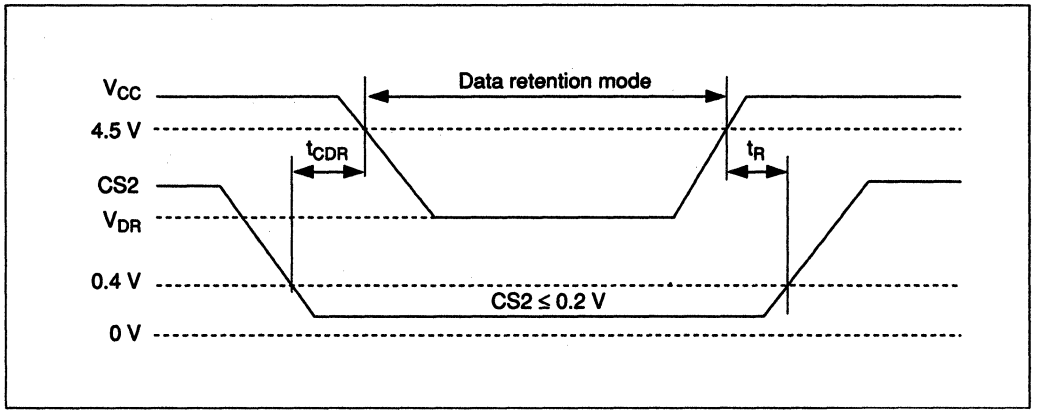
Low V_{CC} Data Retention Waveform (2) ($\overline{CS2}$ Controlled)



HM62256 Series — Maintenance only

32768-word × 8-bit High Speed CMOS Static RAM

Features

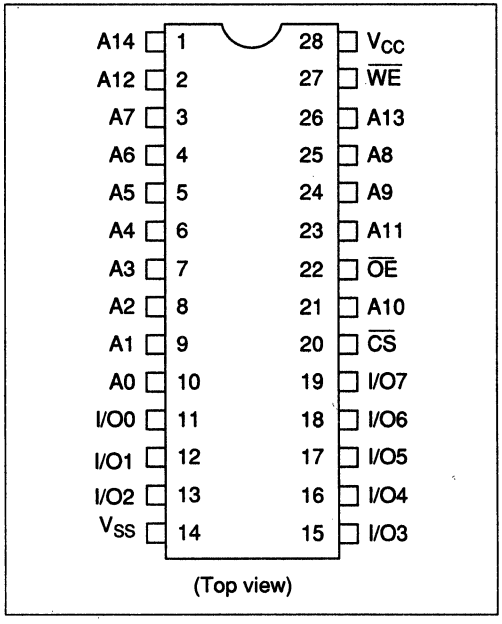
- High speed: Fast access time 85/100/120/150 ns (max)
- Low power standby and low power operation
  - — Standby: 200 µW (typ)/ 10 µW (typ) (L-/L-SL-version)
  - — Operation: 40 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static RAM: No clock or timing strobe required
- Equal access and cycle time
- Common data input and output, three-state output
- Directly TTL compatible—all inputs and outputs
- Battery back up operation capability (L-/L-SL-version)

Ordering Information

Type No.	Access time	Package
HM62256P-8	85 ns	600-mil 28-pin plastic DIP (DP-28)
HM62256P-10	100 ns	
HM62256P-12	120 ns	
HM62256P-15	150 ns	
HM62256LP-8	85 ns	
HM62256LP-10	100 ns	
HM62256LP-12	120 ns	
HM62256LP-15	150 ns	
HM62256LP-10SL	100 ns	
HM62256LP-12SL	120 ns	
HM62256LP-15SL	150 ns	

Type No.	Access time	Package
HM62256FP-8T	85 ns	28-pin plastic SOP (FP-28DA)
HM62256FP-10T	100 ns	
HM62256FP-12T	120 ns	
HM62256FP-15T	150 ns	
HM62256LFP-8T	85 ns	
HM62256LFP-10T	100 ns	
HM62256LFP-12T	120 ns	
HM62256LFP-15T	150 ns	
HM62256LFP-10SLT	100 ns	
HM62256LFP-12SLT	120 ns	
HM62256LFP-15SLT	150 ns	

Pin Arrangement



(Top view)

Note: This device is not available for new application.

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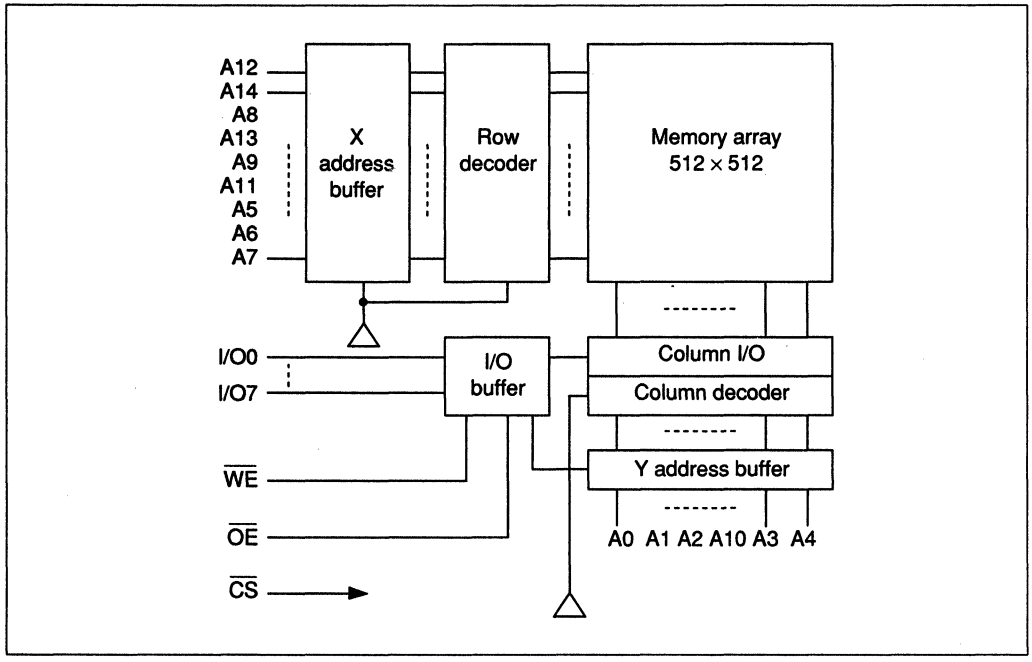
Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Reference cycle
H	x	x	Not selected	I_{SB}, I_{SB1}	High Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle No. 1–3
L	H	L	Write	I_{CC}	Din	Write cycle No. 1
L	L	L	Write	I_{CC}	Din	Write cycle No. 2

Note: x means H or L

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5* to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Temperature under bias	T_{bias}	−10 to +85	°C

Note: −3.0 V min for pulse width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5*	—	0.8	V

Note: −3.0 V min for pulse width ≤ 50 ns

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ *1	Max	Unit	Test condition
Input leakage current		$\|I_{LI}\|$	—	—	2	µA	$V_{IN} = V_{SS}$ to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	2	µA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current		I_{CC}	—	8	15	mA	$\overline{CS} = V_{IL}$, $I_{I/O}$ = 0 mA
Average operating power supply current	HM62256-8	I_{CC1}	—	50	70	mA	Min. cycle, duty = 100%, $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0 mA
	HM62256-10		—	40	70	mA	
	HM62256-12		—	35	70	mA	
	HM62256-15		—	33	70	mA	
		I_{CC2}	—	8	15	mA	$\overline{CS} = V_{IL}$, VIH = V_{CC}, V_{IL} = 0V, $I_{I/O}$ = 0 mA f = 1 MHz

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DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C) (cont)

Parameter	Symbol	Min	Typ *1	Max	Unit	Test condition
Standby power supply current	I_{SB}	—	0.5	3	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	0.04	2	mA	$\overline{CS} \geq V_{CC} - 0.2V$, $0V \leq V_{IN}$
		—	2*2	100*2	µA	
		—	2*3	50*3		
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = 25°C and specified loading.
2. These characterisitcs are guaranteed only for L-version.
3. These characterisitcs are guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f= 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test Condition
Input capacitance	C_{IN}	—	6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$	—	8	pF	$V_{I/O}$ = 0 V

Note: These parameters are sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C unless otherwise noted)

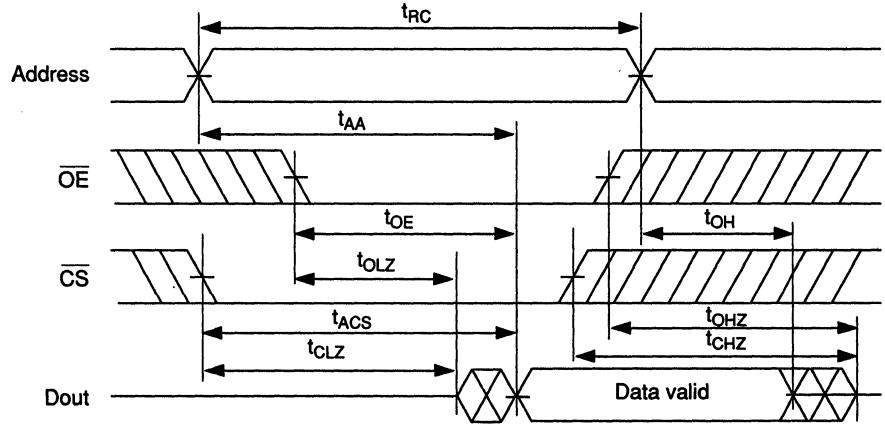
AC Test Conditions:

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1TTL gate and C_L = 100 pF (including scope and jig)

Read Cycle

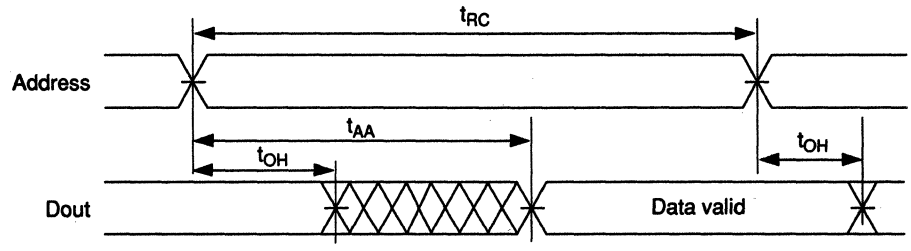
		HM62256-8		HM62256-10		HM62256-12		HM62256-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	85	—	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	85	—	100	—	120	—	150	ns
Chip select access time	t_{ACS}	—	85	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	45	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns
Chip selection to output in low Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip deselection to output in high Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

Read Timing Waveform (1)



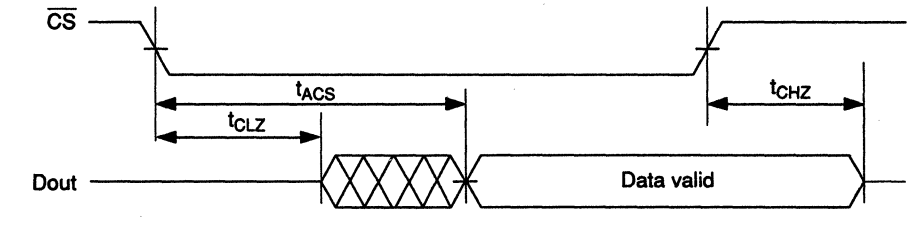
Note: $\overline{WE}$ is high during the read cycle.

Read Timing Waveform (2)



Notes: 1. $\overline{WE}$ is high during the read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. $\overline{OE}$ = V_{IL}.

Read Timing Waveform (3)

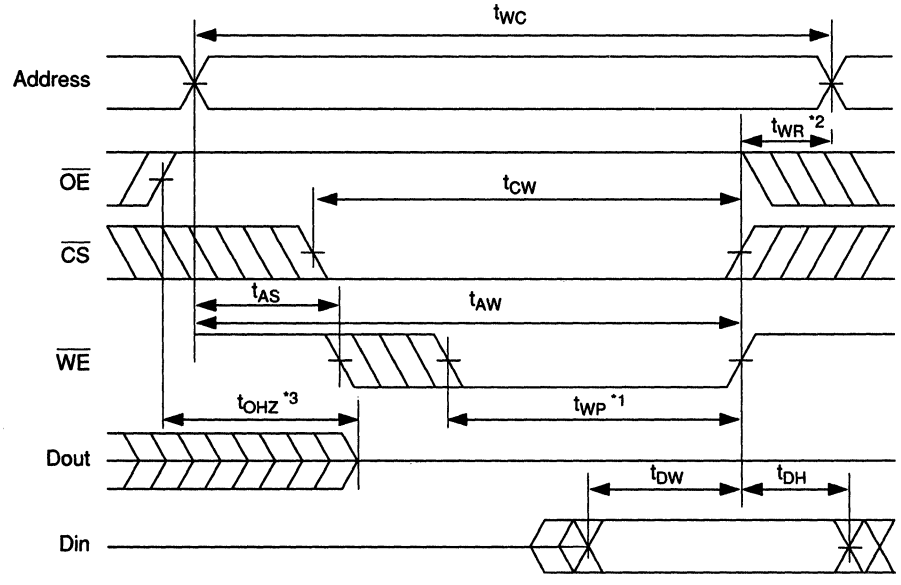


Notes: 1. $\overline{WE}$ is high during the read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.

Write Cycle

		HM62256-8		HM62256-10		HM62256-12		HM62256-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	85	—	100	—	120	—	150	—	ns
Chip selection to end of write	t_{CW}	75	—	80	—	85	—	100	—	ns
Address valid to end of write	t_{AW}	75	—	80	—	85	—	100	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	60	—	60	—	70	—	90	—	ns
Write recovery time	t_{WR}	10	—	0	—	0	—	0	—	ns
Write to output in high Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to write time overlap	t_{DW}	40	—	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output disable to output in high Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Out of phase input signals must not be applied.

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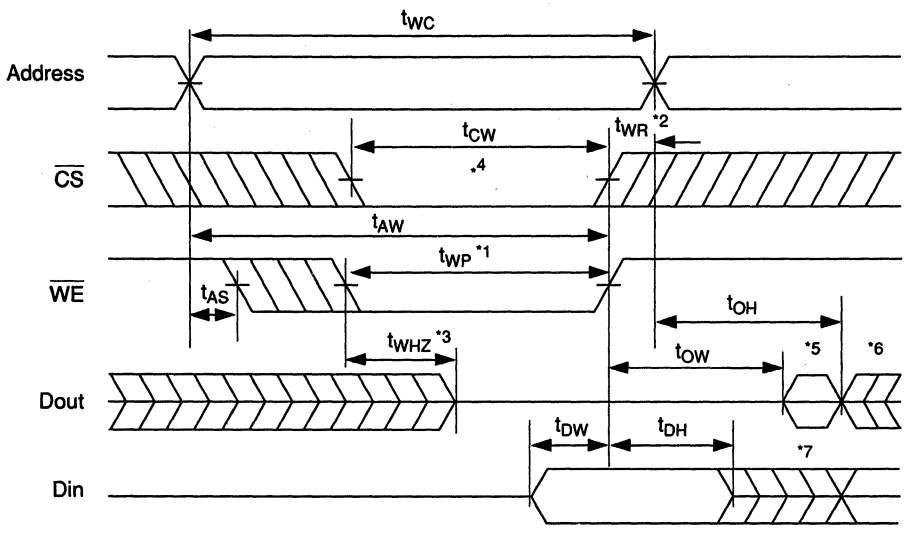
Write Timing Waveform (2) ($\overline{OE}$ Fixed Low)



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transistion occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. Dout is in the same phase of written data of this write cycle.
6. Dout is the read data of next address.
7. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Out of phase input signals must not be appplied to I/O pins.

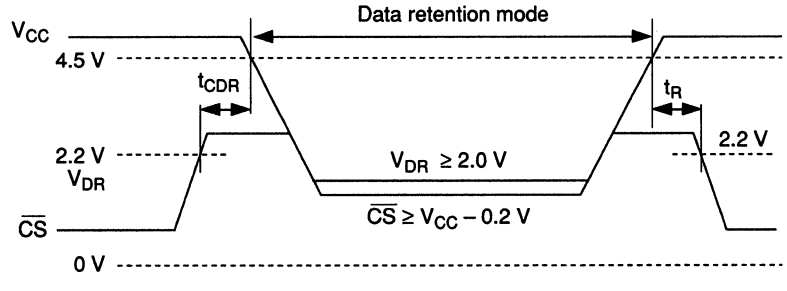
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

These characteristics are guaranteed only for L- and L-SL version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2$ V	2.0	—	—	V
Data retention current	I_{CCDR}	V_{CC} = 3.0 V, $\overline{CS} \geq 2.8$ V 0 V ≤ V_{IN}	—	—	50 *2	µA
			—	—	10 *3	
Chip deselect to data retention time	t_{CDR}	See retention waveform	0	—	—	ns
Operation recovery time	t_R	See retention waveform	t_{RC} *1	—	—	ns

Notes: 1. t_{RC} = read cycle time
2. These characteristics are guaranteed only for L-version, V_{IL} = –0.3 V min, 20 µA max. at Ta = 0 to 40°C.
3. These characteristics are guaranteed only for L-SL version, V_{IL} = –0.3 V min, 3 µA max. at Ta = 0 to 40°C.

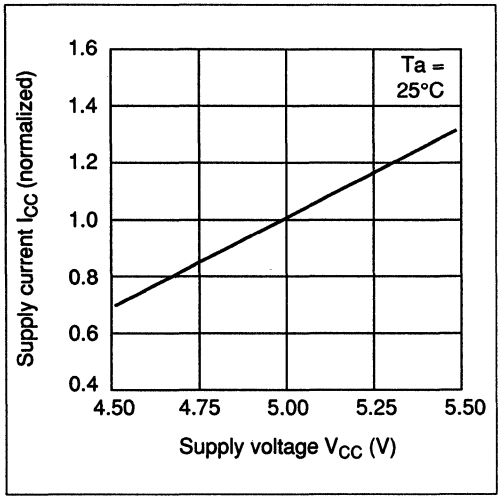
Low V_{CC} Data Retention Waveform



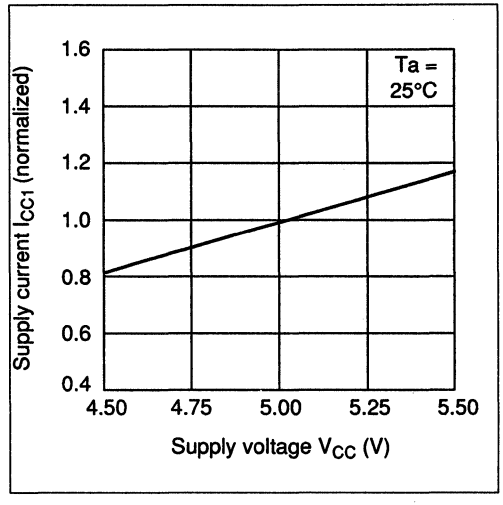
Note: In data retention mode, $\overline{CS}$ controls the address, $\overline{WE}$, $\overline{OE}$, and Din buffers. V_{in} for these inputs can be in high impedance state in data retention mode.

5

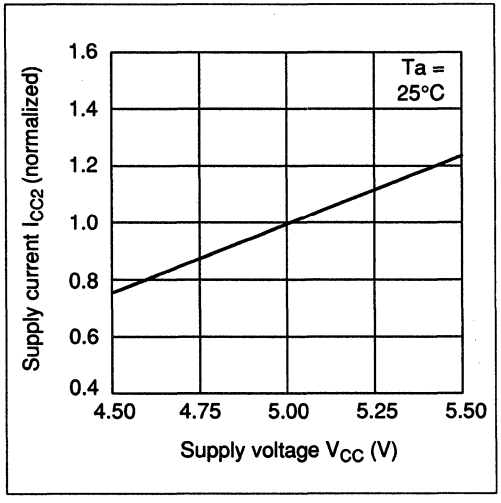
Characteristic Curves



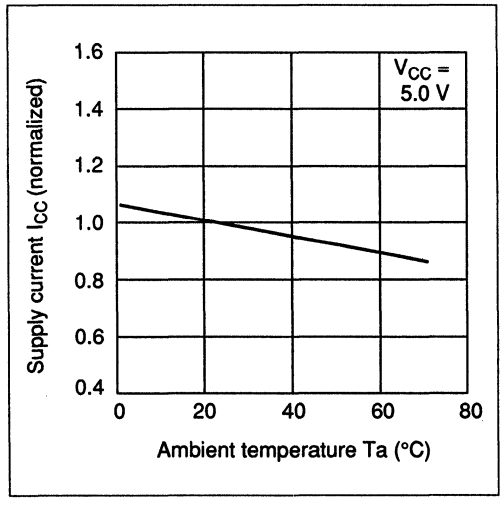
Supply Current vs. Supply Voltage (1)



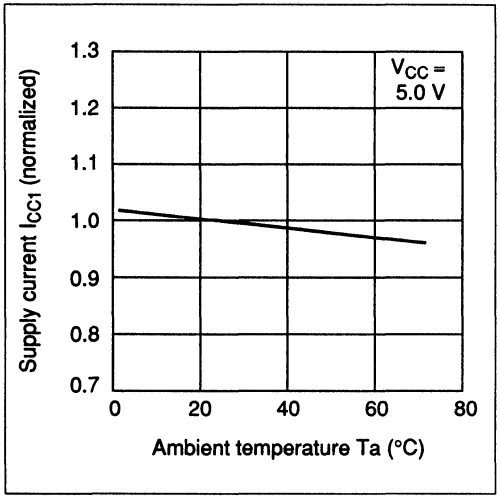
Supply Current vs. Supply Voltage (2)



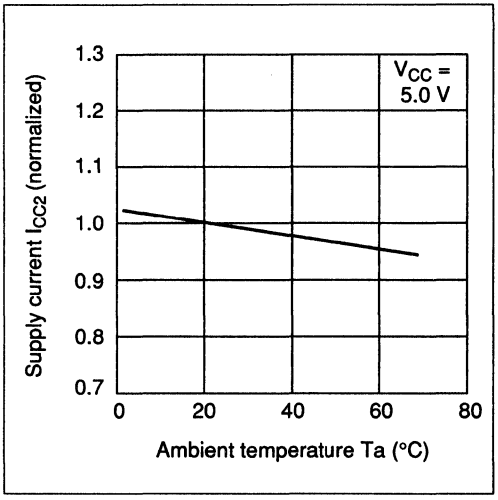
Supply Current vs. Supply Voltage (3)



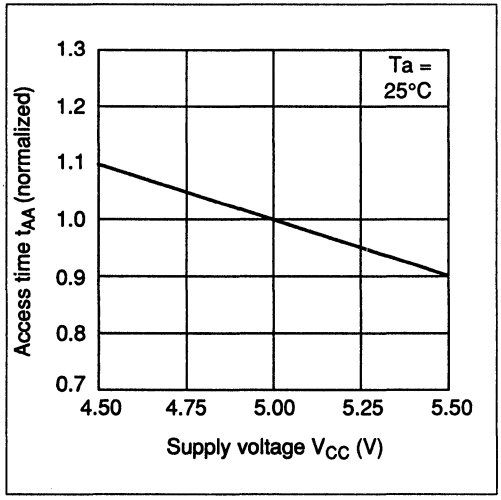
Supply Current vs. Ambient Temperature (1)



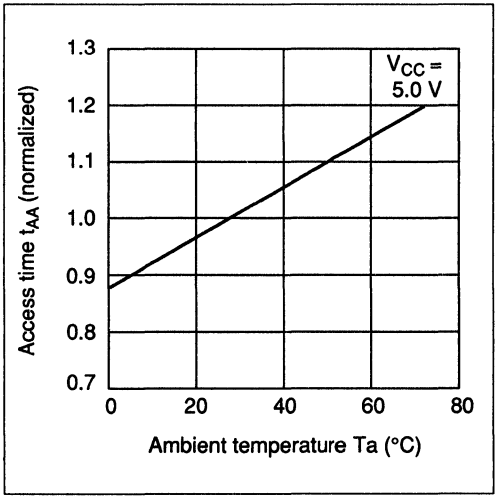
Supply Current vs. Ambient Temperature (2)



Supply Current vs. Ambient Temperature (3)

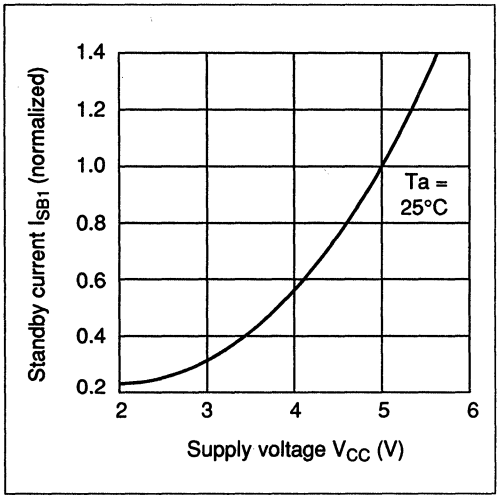


Access Time vs. Supply Voltage

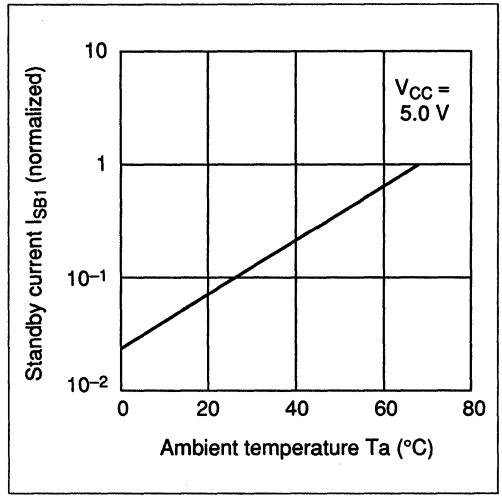


Access Time vs. Ambient Temperature

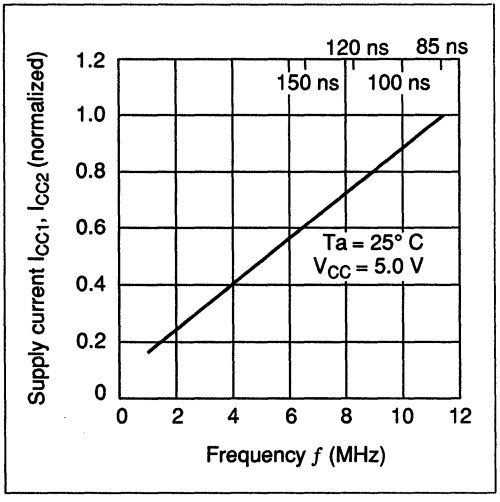
5



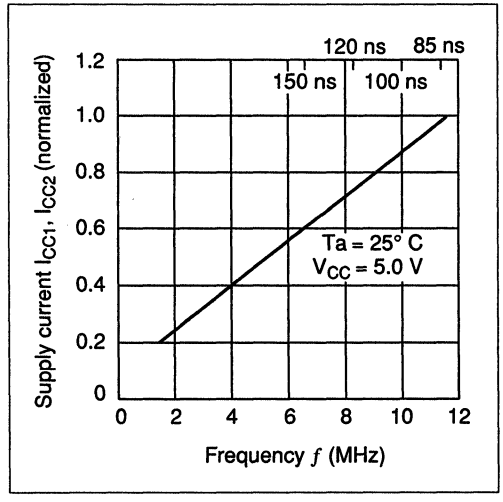
Standby Current vs. Supply Voltage



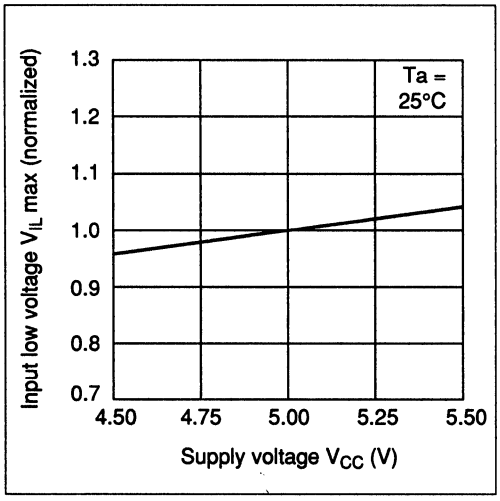
Standby Current vs. Ambient Temperature



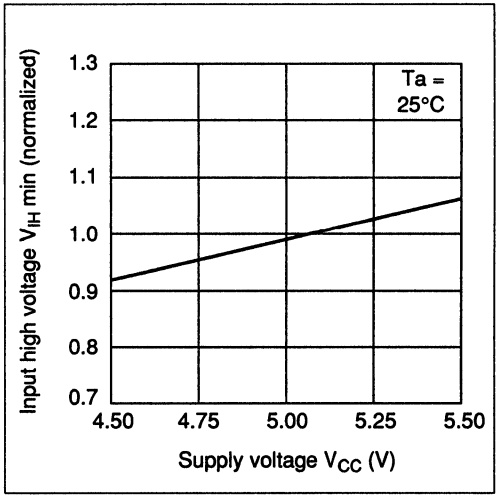
Supply Current vs. Frequency (Read)



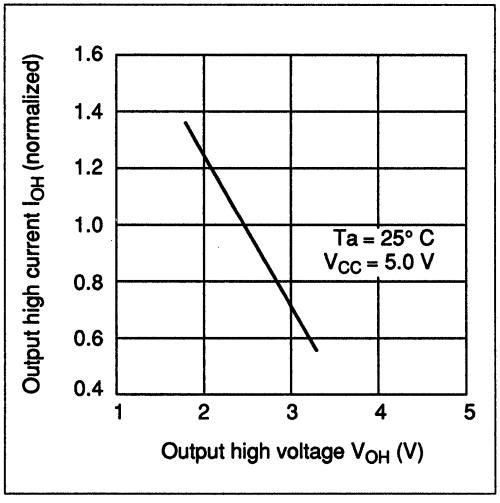
Supply Current vs. Frequency (Write)



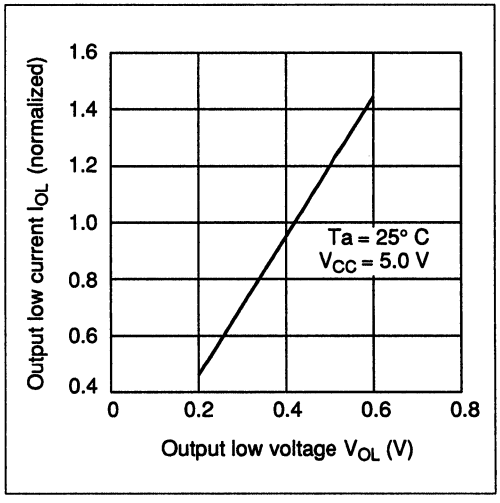
Input Low Voltage vs. Supply Voltage



Input High Voltage vs. Supply Voltage

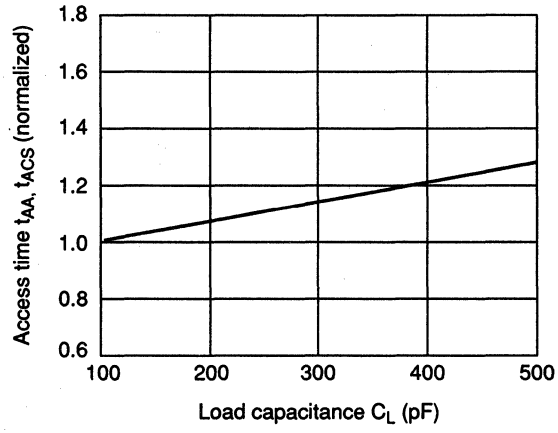


Output Current vs. Output Voltage (High)



Output Current vs. Output Voltage (Low)

5



Access Time vs. Load Capacitance

HM62256A Series

32,768-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM62256A is a CMOS static RAM organized 32-kword × 8-bit. It realizes higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology. The device, packaged in a 8 × 14 mm TSOP with thickness of 1.2 mm, 450-mil SOP (foot print pitch width), 600-mil plastic DIP, or 300-mil plastic DIP, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided. It offers low power standby power dissipation; therefore, it is suitable for battery back up system.

Features

- High speed: Fast Access time 85/100/120/150 ns (max)
- Low Power
  Standby: 5 µW (typ) (L/L-SL version)
  Operation: 40 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation

Ordering Information

Type No.	Access time	Package
HM62256AP-8	85 ns	600-mil 28-pin plastic DIP (DP-28)
HM62256AP-10	100 ns	
HM62256AP-12	120 ns	
HM62256AP-15	150 ns	
HM62256ALP-8	85 ns	
HM62256ALP-10	100 ns	
HM62256ALP-12	120 ns	
HM62256ALP-15	150 ns	
HM62256ALP-8SL	85 ns	
HM62256ALP-10SL	100 ns	
HM62256ALP-12SL	120 ns	
HM62256ALP-15SL	150 ns	
HM62256ASP-8	85 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62256ASP-10	100 ns	
HM62256ASP-12	120 ns	
HM62256ASP-15	150 ns	
HM62256ALSP-8	85 ns	
HM62256ALSP-10	100 ns	
HM62256ALSP-12	120 ns	
HM62256ALSP-15	150 ns	
HM62256ALSP-8SL	85 ns	
HM62256ALSP-10SL	100 ns	
HM62256ALSP-12SL	120 ns	
HM62256ALSP-15SL	150 ns	
HM62256AFP-8T	85 ns	450-mil 28-pin plastic SOP (FP-28DA)
HM62256AFP-10T	100 ns	
HM62256AFP-12T	120 ns	
HM62256AFP-15T	150 ns	
HM62256ALFP-8T	85 ns	
HM62256ALFP-10T	100 ns	
HM62256ALFP-12T	120 ns	
HM62256ALFP-15T	150 ns	
HM62256ALFP-8SLT	85 ns	
HM62256ALFP-10SLT	100 ns	
HM62256ALFP-12SLT	120 ns	
HM62256ALFP-15SLT	150 ns	

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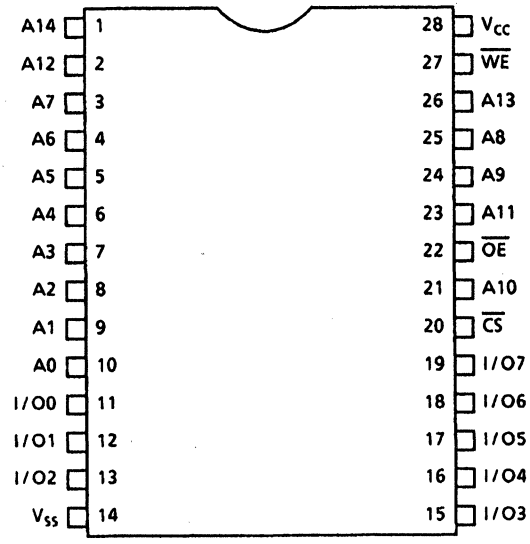
TSOP Series

Type No.	Access time	Package
HM62256ALT-8	85 ns	8 mm × 14 mm
HM62256ALT-10	100 ns	32-pin TSOP
HM62256ALT-12	120 ns	(normal type)
HM62256ALT-15	150 ns	(TFP-32DA)
HM62256ALT-8SL	85 ns	
HM62256ALT-10SL	100 ns	
HM62256ALT-12SL	120 ns	
HM62256ALT-15SL	150 ns	

Type No.	Access time	Package
HM62256ALR-8	85 ns	8 mm × 14 mm
HM62256ALR-10	100 ns	32-pin TSOP
HM62256ALR-12	120 ns	(reverse type)
HM62256ALR-15	150 ns	(TFP-32DAR)
HM62256ALR-8SL	85 ns	
HM62256ALR-10SL	100 ns	
HM62256ALR-12SL	120 ns	
HM62256ALR-15SL	150 ns	

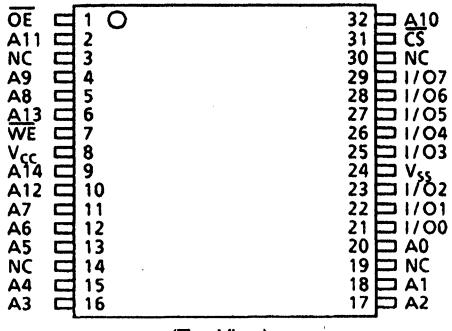
Pin Arrangement

HM62256AP/AFP/ASP Series



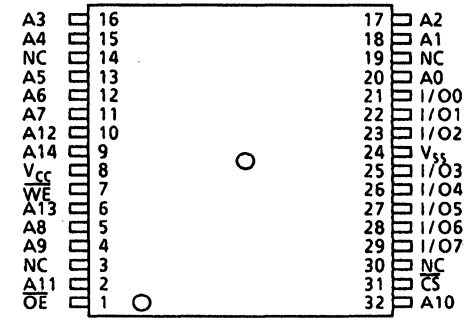
(Top View)

HM62256AT Series



(Top View)

HM62256AR Series

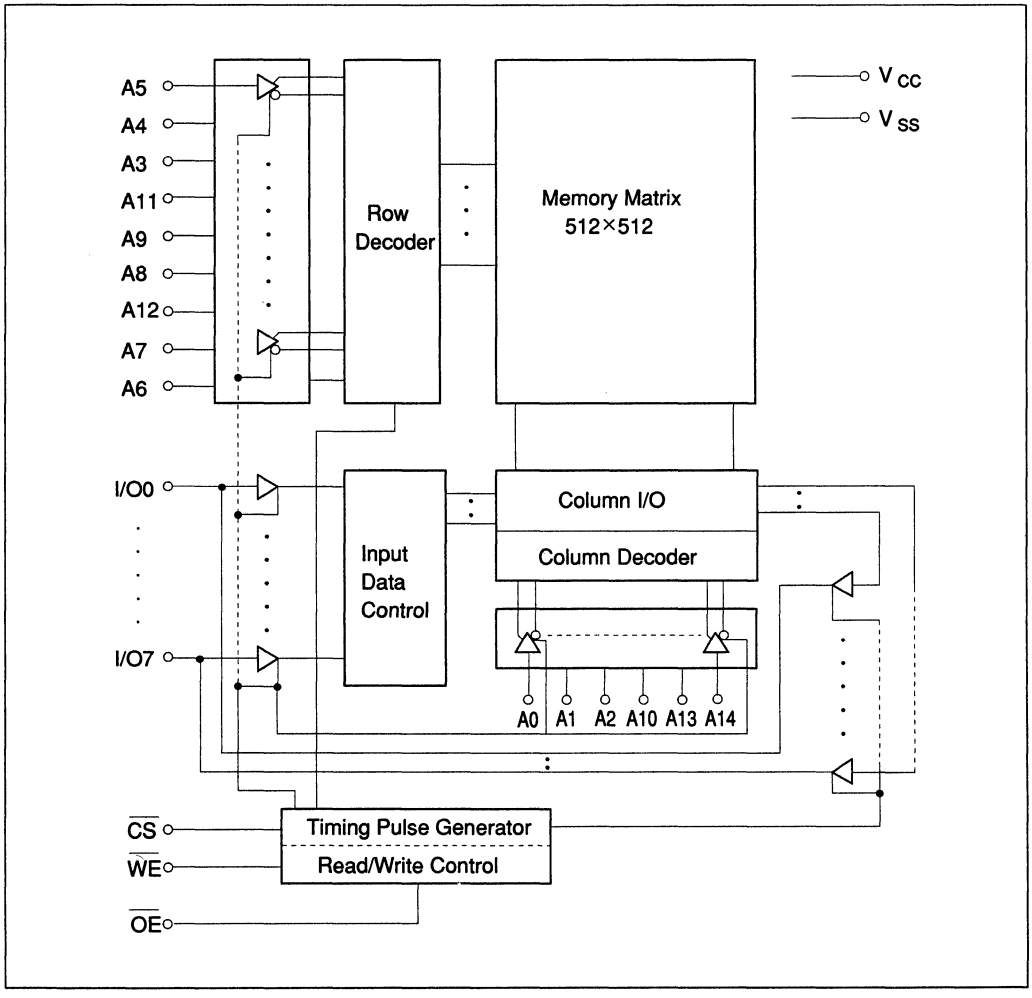


(Top View)

Pin Description

Symbol	Function	Symbol	Function
A0 – A14	Address	$\overline{OE}$	Output enable
I/O0 – I/O7	Input/output	NC	No connection
$\overline{CS}$	Chip select	V_{CC}	Power supply
$\overline{WE}$	Write enable	V_{SS}	Ground

Block Diagram



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Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5[*1] to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. V_T min = –3.0 V for pulse half-width ≤ 50 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5[*1]	—	0.8	V

Note: 1. V_{IL} min = –3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} current	I_{CC}	—	6	15	mA	$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} Iout = 0 mA
HM62256A-8	I_{CC1}	—	33	50	mA	min cycle, duty = 100%, $I_{I/O}$ = 0 mA
HM62256A-10		—	30	50		$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL}
HM62256A-12		—	27	45		
HM62256A-15		—	24	40		
	I_{CC2}	—	5	15	mA	Cycle time = 1µs, $I_{I/O}$ = 0 mA $\overline{CS}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0
Standby V_{CC} current	I_{SB}	—	0.3	2	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	0.01	1	mA	Vin ≥ 0 V $\overline{CS}$ ≥ V_{CC} – 0.2 V
		—	0.3*2	100*2	µA	
		—	0.3*3	50*3	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

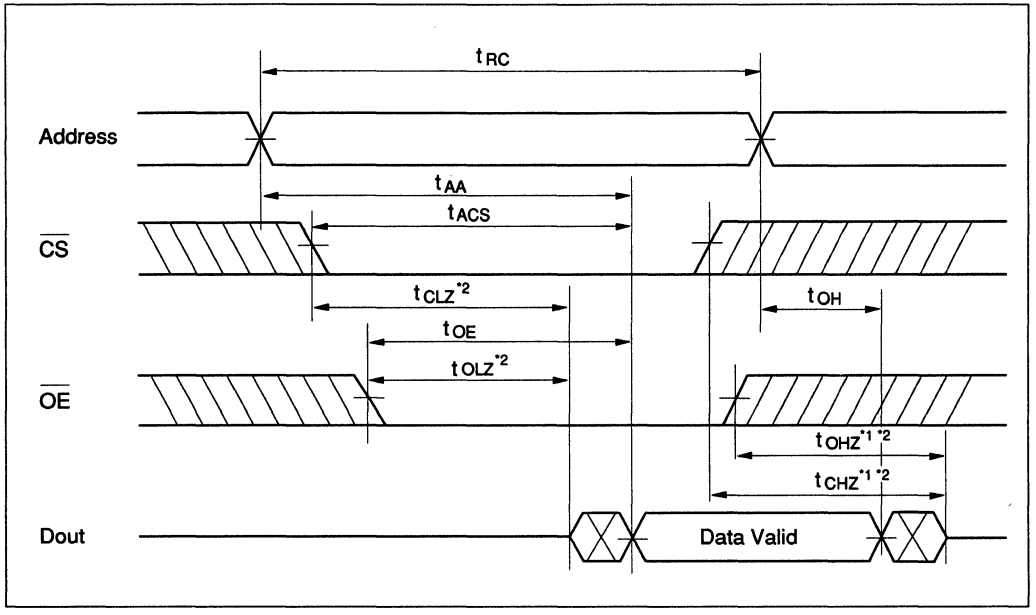
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing refernce levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

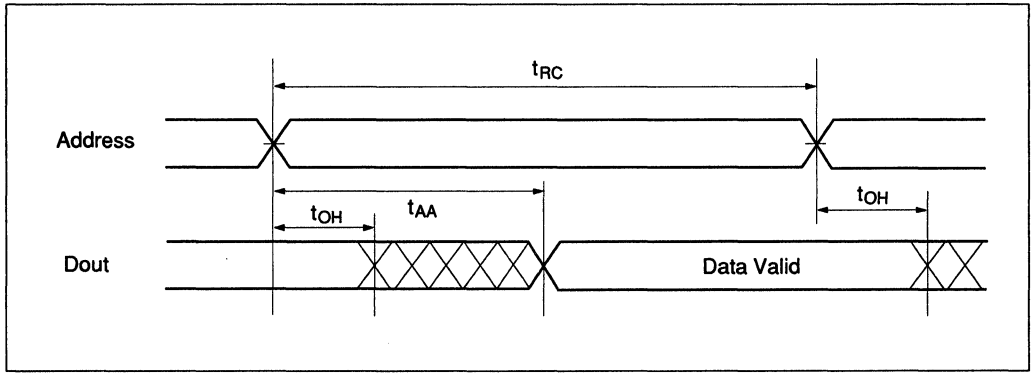
Read Cycle

		HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	85	—	100	—	120	—	150	—	ns	
Address access time	t_{AA}	—	85	—	100	—	120	—	150	ns	
Chip select access time	t_{ACS}	—	85	—	100	—	120	—	150	ns	
Output enable to output valid	t_{OE}	—	45	—	50	—	60	—	70	ns	
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	1, 2
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns	

Read Timing Waveform (1) *3



Read Timing Waveform (2) *3 *4 *6



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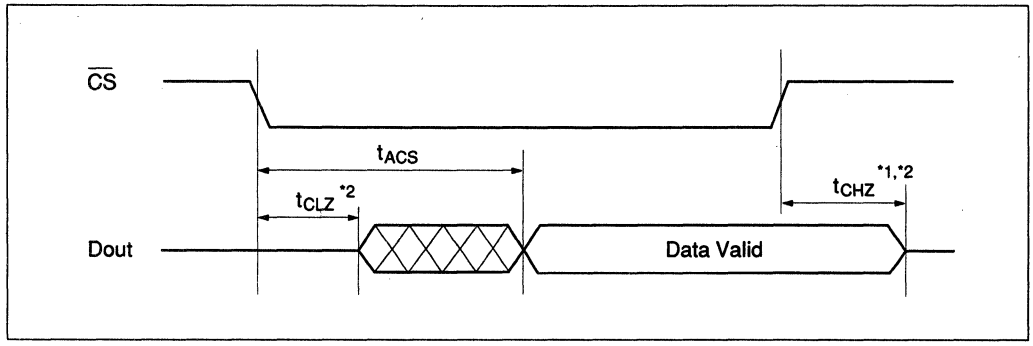
Read Timing Waveform (3) *3 *5 *6

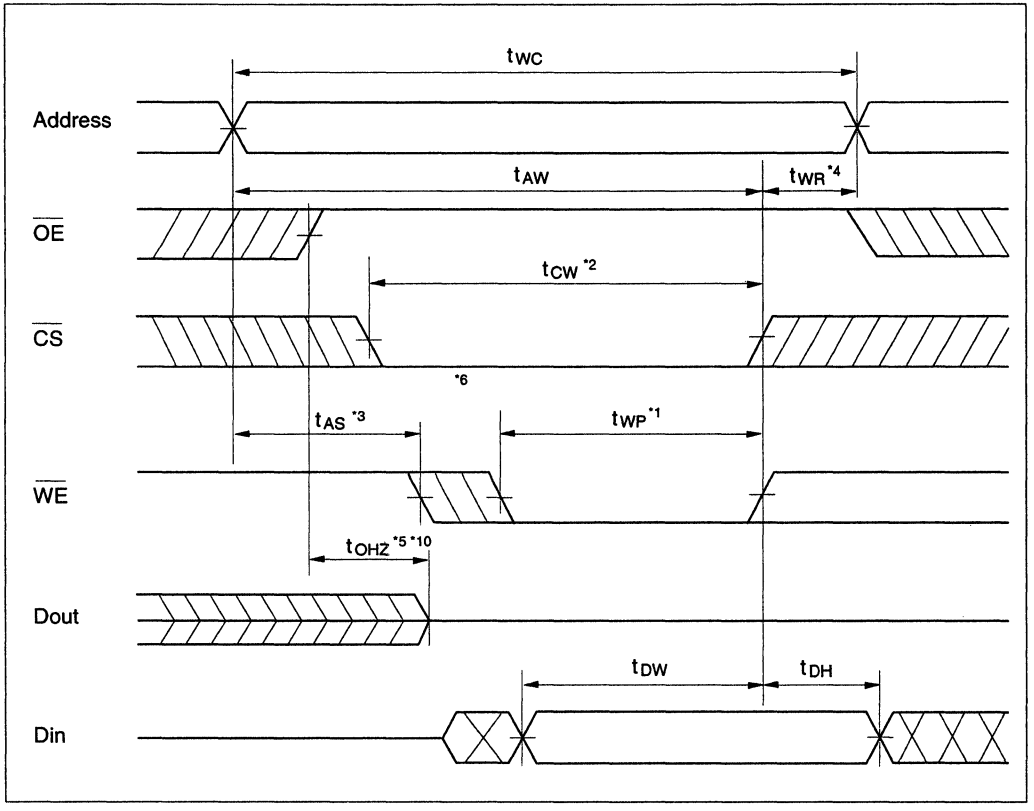


Notes: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
6. $\overline{OE} = V_{IL}$.

Write Cycle

		HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Write cycle time	t_{WC}	85	—	100	—	120	—	150	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	85	—	100	—	ns	2
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	75	—	80	—	85	—	100	—	ns	
Write pulse width	t_{WP}	55	—	60	—	70	—	90	—	ns	1
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns	4
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns	10
Data to write time overlap	t_{DW}	40	—	40	—	50	—	60	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	10, 11

Write Timing Waveform (1) ($\overline{OE}$ Clock)



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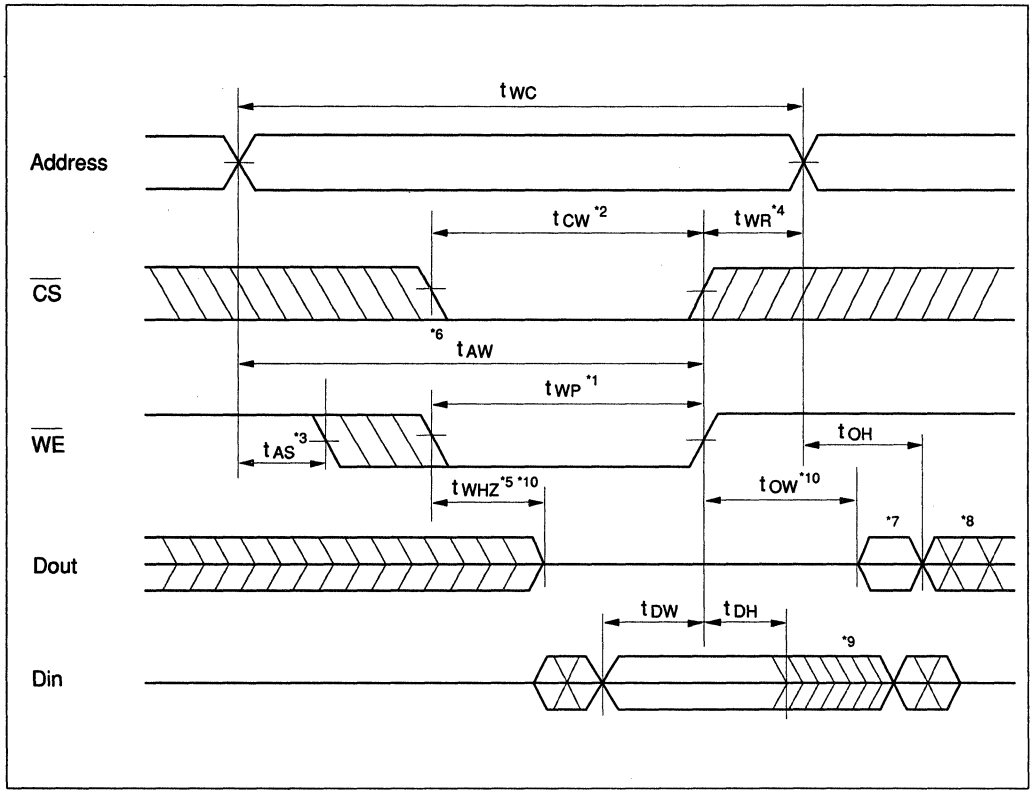
Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



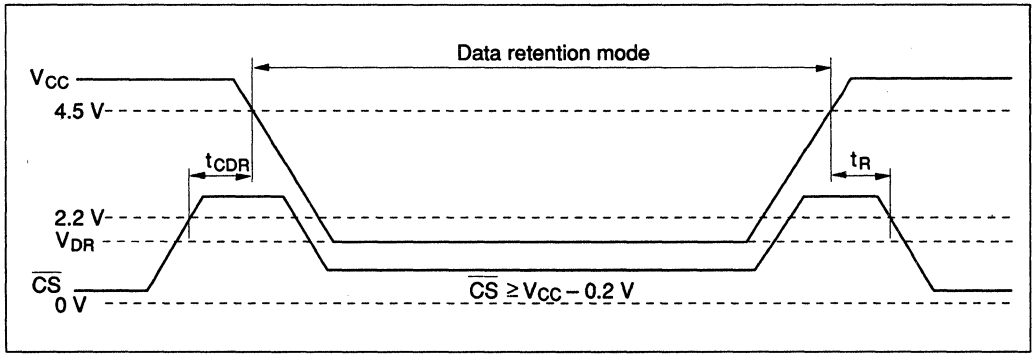
Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
7. Dout is the same phase of the write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the output must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L/L-SL version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	0.2	30*2	µA	V_{CC} = 3.0 V, Vin ≥ 0 V
		—	0.2	10*3	µA	$\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*4	—	—	ns	

Low V_{CC} Data Retention Timing Waveform



Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. 20 µA max at Ta = 0 to +40°C. (only for L-version)
3. 3 µA max at Ta = 0 to +40°C. (only for L-SL version)
4. t_{RC} = read cycle time.
5. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS}$ controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

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HM628128 Series

131072-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM628128 is a CMOS static RAM organized 128-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. The TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- High speed: fast access time 70/85/100/120 ns (max)
- Low power
  - —Standby: 10 μW (typ) (L/L-L/L-SL version)
  - —Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - —No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L/L-L/L-SL version) (2 chip selection for battery back up)

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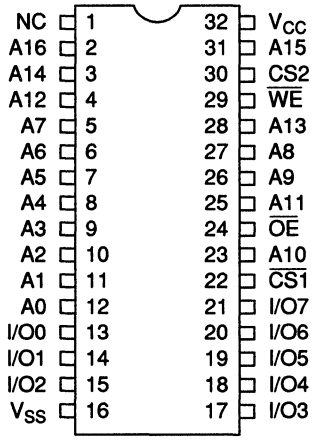
Ordering Information

Type No.	Access time	Package
HM628128P-7	70 ns	600-mil, 32-pin plastic DIP (DP-32)
HM628128P-8	85 ns	
HM628128P-10	100 ns	
HM628128P-12	120 ns	
HM628128LP-7	70 ns	
HM628128LP-8	85 ns	
HM628128LP-10	100 ns	
HM628128LP-12	120 ns	
HM628128LP-7SL	70 ns	
HM628128LP-8SL	85 ns	
HM628128LP-10SL	100 ns	
HM628128LP-12SL	120 ns	
HM628128T-7	70 ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
HM628128T-8	85 ns	
HM628128T- 10	100 ns	
HM628128T- 12	120 ns	
HM628128LT-7	70 ns	
HM628128LT-8	85 ns	
HM628128LT-10	100 ns	
HM628128LT-12	120 ns	
HM628128LT-7L	70 ns	
HM628128LT-8L	85 ns	
HM628128LT-10L	100 ns	
HM628128LT-12L	120 ns	
HM628128LT-7SL	70 ns	
HM628128LT-8SL	85 ns	
HM628128LT-10SL	100 ns	
HM628128LT-12SL	120 ns	

Type No.	Access time	Package
HM628128FP-7	70 ns	525 mil, 32-pin plastic SOP (FP-32D)
HM628128FP-8	85 ns	
HM628128FP-10	100 ns	
HM628128FP-12	120 ns	
HM628128LFP-7	70 ns	
HM628128LFP-8	85 ns	
HM628128LFP-10	100 ns	
HM628128LFP-12	120 ns	
HM628128LFP-7SL	70 ns	
HM628128LFP-8SL	85 ns	
HM628128LFP-10SL	100 ns	
HM628128LFP-12SL	120 ns	
HM628128R-7	70 ns	8mm × 20 mm 32-pin TSOP (reverse type) (TFP-32DR)
HM628128R-8	85 ns	
HM628128R-10	100 ns	
HM628128R- 12	120 ns	
HM628128LR-7	70 ns	
HM628128LR-8	85 ns	
HM628128LR-10	100 ns	
HM628128LR-12	120 ns	
HM628128LR-7L	70 ns	
HM628128LR-8L	85 ns	
HM628128LR-10L	100 ns	
HM628128LR-12L	120 ns	
HM628128LR-7SL	70 ns	
HM628128LR-8SL	85 ns	
HM628128LR-10SL	100 ns	
HM628128LR-12SL	120 ns	

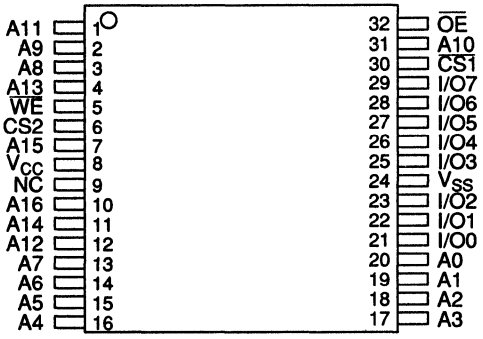
Pin Arrangement

HM628128P/LP/FP/LFP series



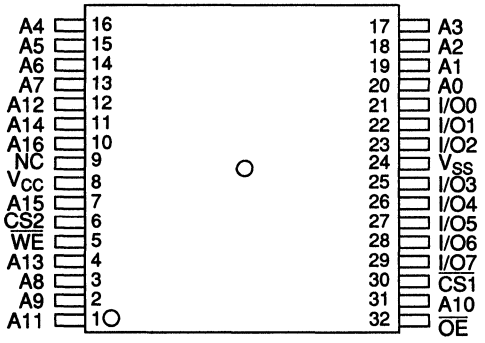
(Top view)

HM628128T series (normal type TSOP)



(Top view)

HM628128R series (reverse type TSOP)

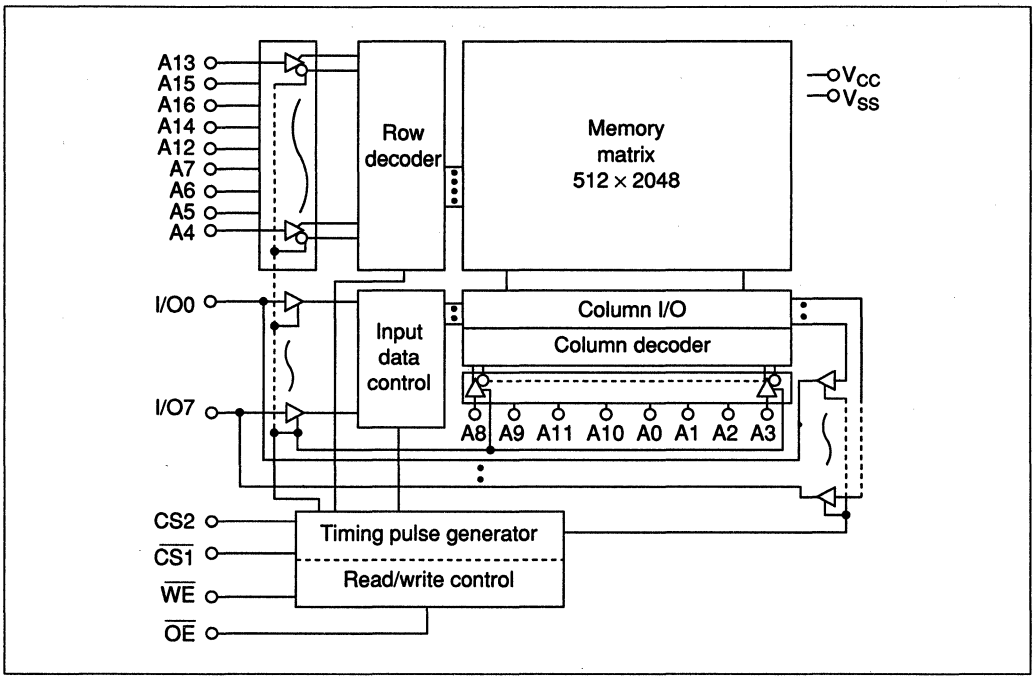


(Top view)

Pin Description

Pin name	Function	Pin name	Function
A0–A16	Address	$\overline{OE}$	Output enable
I/O0–I/O7	Input/output	NC	Not connected
$\overline{CS1}$	Chip select 1	V_{CC}	Power supply
CS2	Chip select 2	V_{SS}	Ground
$\overline{WE}$	Write enable		

Block Diagram



Truth Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	V_{CC} current	Dout pin	Cycle
x	H	x	x	Not selected	I_{SB}, I_{SB1}	High-Z	—
x	x	L	x		I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	D_{IN}	Write cycle (1)
L	L	H	L		I_{CC}	D_{IN}	Write cycle (2)

Note: x: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5* to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: −3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.3*	—	0.8	V

Note: −3.0 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\lvert I_{LI} \rvert$	—	—	2	µA	$V_{IN} = V_{SS}$ to V_{CC}
Output leakage current	$\lvert I_{LO} \rvert$	—	—	2	µA	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL} or $\overline{OE} = V_{IH}$ or WE = V_{IL}, $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current: DC	I_{CC}	—	15	35	mA	$\overline{CS1} = V_{IL}$, CS2 = V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating power supply current	I_{CC1}	—	45	70	mA	Min. cycle, duty = 100%, $\overline{CS1} = V_{IL}$, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	I_{CC2}	—	15	30	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1} \leq$ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, $V_{IH} \geq V_{CC}$ – 0.2 V, $V_{IL} \leq$ 0.2 V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS1} = V_{IH}$, CS2 = V_{IH} or CS2 = V_{IL}
Standby power supply current (1): DC	I_{SB1}	—	0.02	2	mA	$V_{IN} \geq$ 0 V, $\overline{CS1} \geq V_{CC}$ – 0.2 V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ CS2 = V_{IL}
		—	2*2	100*2	µA	
		—	2*3	50*3	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
2. These characteristics are guaranteed only for L-version.
3. These characteristics are guaranteed only for L-L/L-SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: These parameters are sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted)

Test Conditions:

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL gate and C_L (100 pF) (Including scope and jig)

Read Cycle

		HM628128-7		HM628128-8		HM628128-10		HM628128-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip selection ($\overline{CS1}$) to output valid	t_{CO1}	—	70	—	85	—	100	—	120	ns
Chip selection (CS2) to output valid	t_{CO2}	—	70	—	85	—	100	—	120	ns
Output enable ($\overline{OE}$) output valid	t_{OE}	—	35	—	45	—	50	—	60	ns
Chip selection ($\overline{CS1}$) to output in low-Z*[1,2,3]	t_{LZ1}	10	—	10	—	10	—	10	—	ns
Chip selection (CS2) to output in low-Z*[1,2,3]	t_{LZ2}	10	—	10	—	10	—	10	—	ns
Output enable ($\overline{OE}$) to output in low-Z*[1,2,3]	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip deselection ($\overline{CS1}$) to output in high-Z*[1,2,3]	t_{HZ1}	0	25	0	30	0	35	0	45	ns
Chip deselection (CS2) to output in high-Z*[1,2,3]	t_{HZ2}	0	25	0	30	0	35	0	45	ns
Output disable ($\overline{OE}$) to output in high-Z*[1,2,3]	t_{OHZ}	0	25	0	30	0	35	0	45	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns

Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. These parameters are sampled and not 100% tested.

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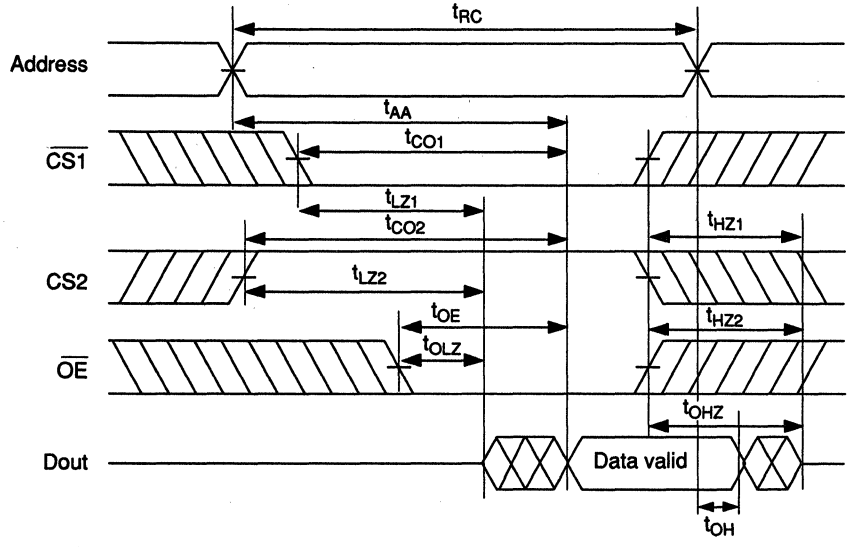
Read Timing Waveform



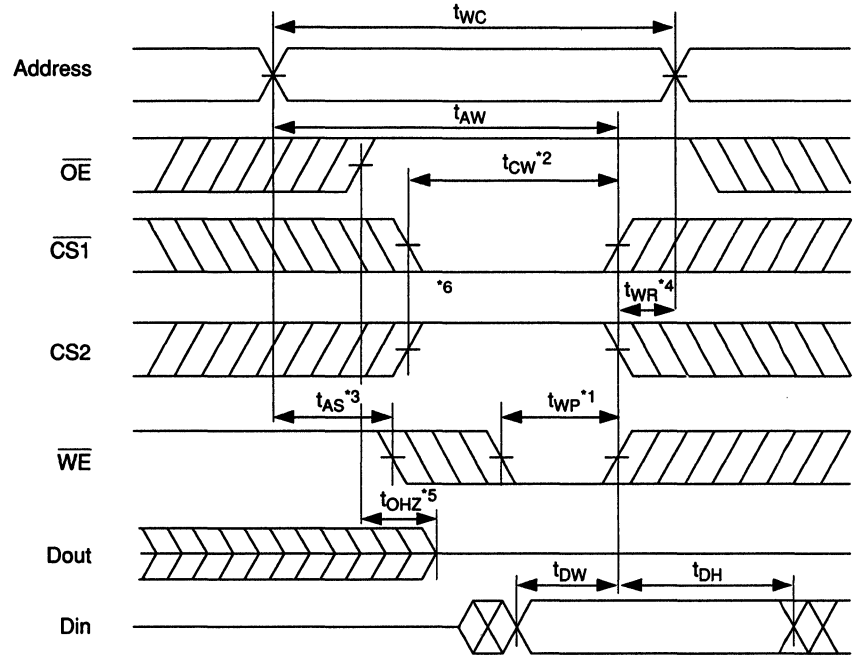
Note: $\overline{WE}$ is high for read cycle.

Write Cycle

		HM628128-7		HM628128-8		HM628128-10		HM628128-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Chip selection to end of write	t_{CW}	60	—	75	—	80	—	85	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Address valid to end of write	t_{AW}	60	—	75	—	80	—	85	—	ns
Write pulse width	t_{WP}	50	—	55	—	60	—	70	—	ns
Write recovery time*1	t_{WR}	5	—	5	—	5	—	10	—	ns
		10	—	10	—	10	—	15	—	ns*1
Write to output in high-Z*2	t_{WHZ}	0	25	0	30	0	35	0	40	ns
Data to write time overlap	t_{DW}	30	—	35	—	40	—	45	—	ns
Write hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output active from end of write*1	t_{OW}	5	—	5	—	5	—	5	—	ns

Notes: 1. This value is measured from CS2 going low to the end of write cycle.
2. This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Notes: 1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begin at the latest transtion among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write end at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

2. t_{CW} is measure from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

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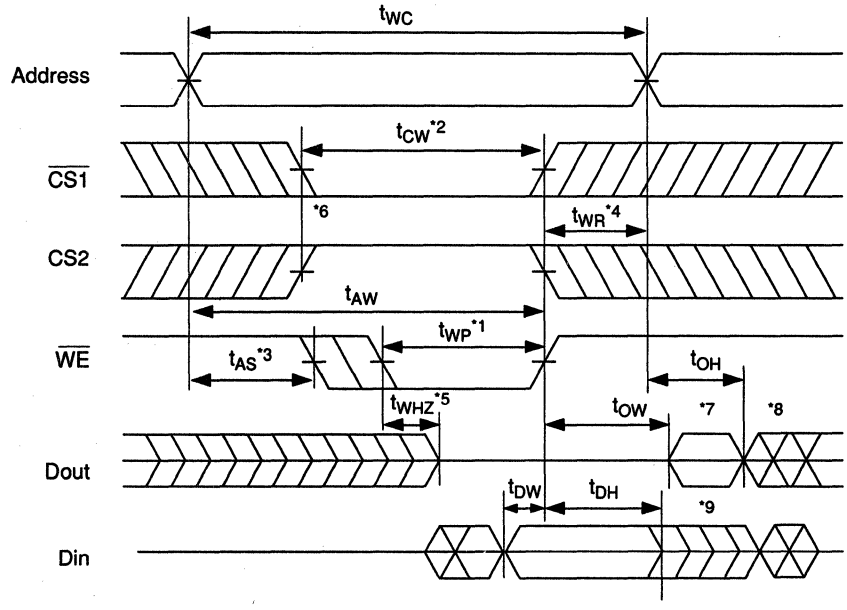
Write Timing Waveform (2) ($\overline{OE}$ Fixed Low)



Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transtiion amon $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write. t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max
2. t_{CW} is measure from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore,the input signals of the opposite phase to the outputs must not be applied to them.

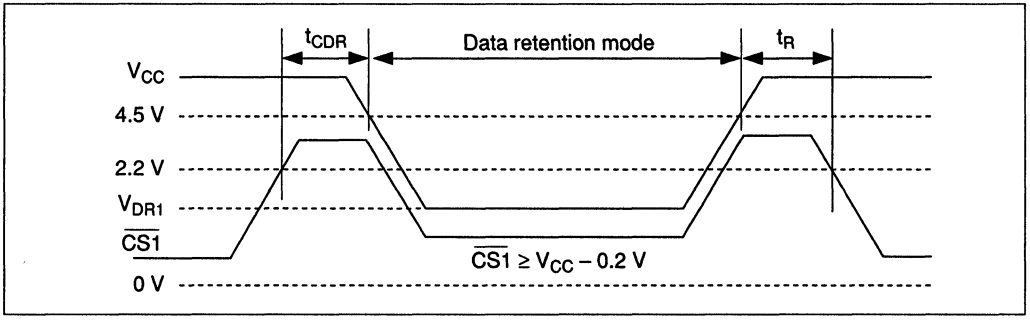
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

(These characteristics are guaranteed only for L, L-L, and L-SL version.)

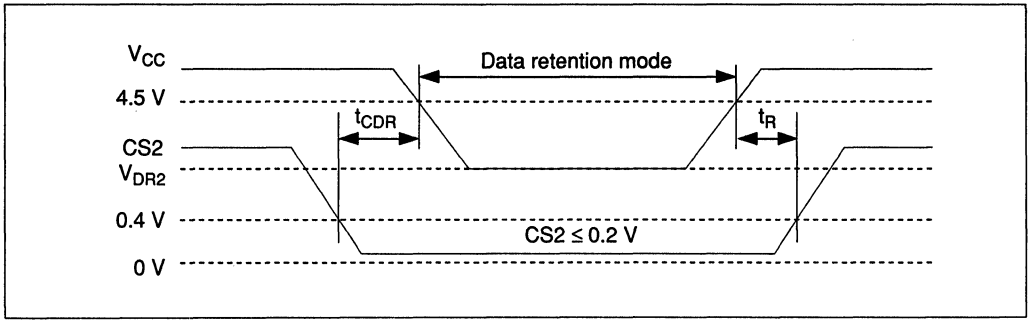
Parameter	Symbol		Min	Typ	Max	Unit	Test conditions*4
V_{CC} for data retention	V_{DR}		2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2$ V, or 0 V ≤ CS2 ≤ 0.2 V, $V_{in} \geq$
Data retention current	I_{CCDR}	L	—	1	50*1	µA	V_{CC} = 3.0 V, $V_{in} \geq$ 0 V, $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ $V_{CC} - 0.2$ V, or 0 V ≤ CS2 ≤ 0.2 V
		L-L	—	1	30*2	µA	
		L-SL	—	1	15*3	µA	
Chip deselect to data retention time	t_{CDR}		0	—	—	ns	See retention waveform
Operation recovery time	t_R		5	—	—	ms	

Notes: 1. 20 µA max at Ta = 0 to 40°C
2. 6 µA max at Ta = 0 to 40°C
3. 3 µA max at Ta = 0 to 40°C
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. if $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ $V_{CC} - 0.2$ V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



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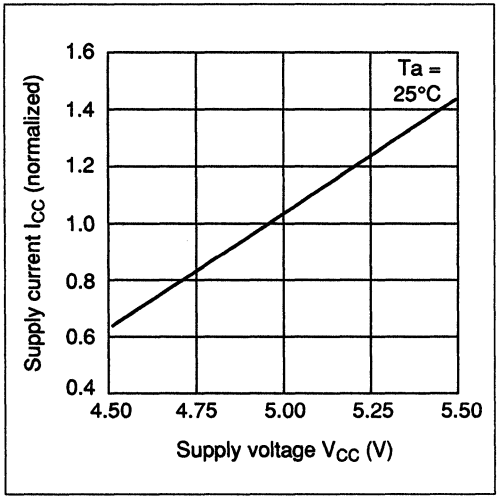
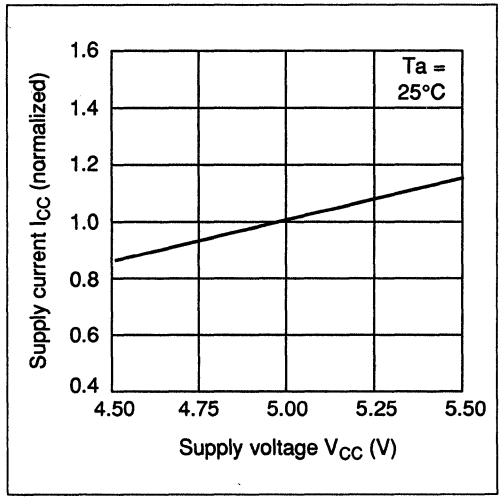
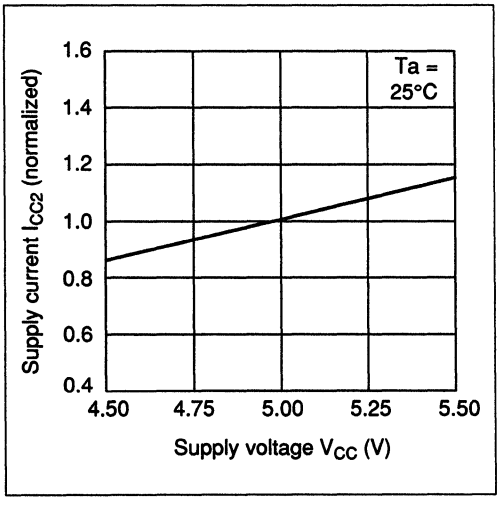


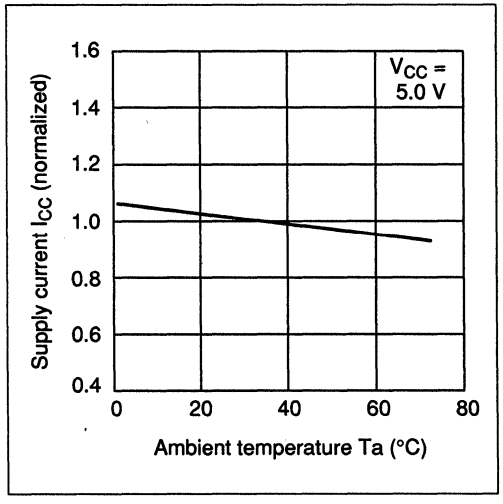
Supply Current vs. Supply Voltage (1)



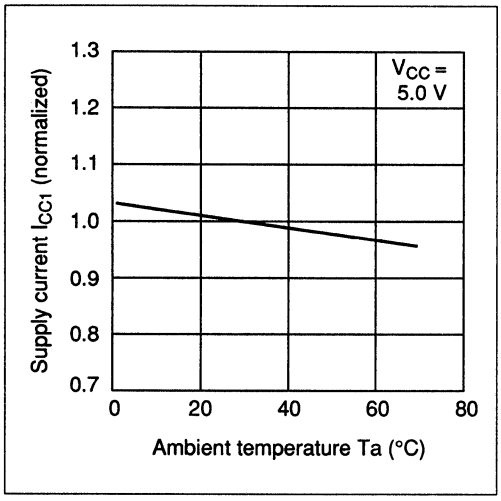
Supply Current vs. Supply Voltage (2)



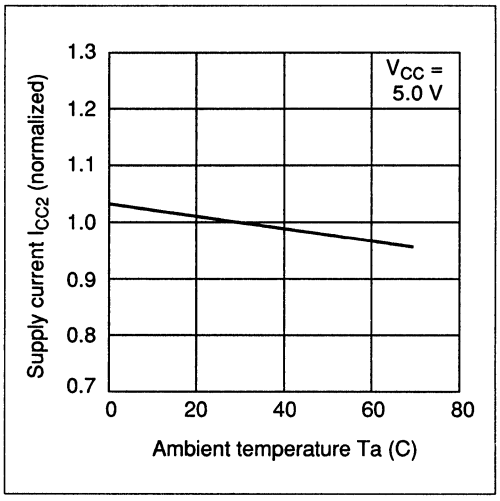
Supply Current vs. Supply Voltage (3)



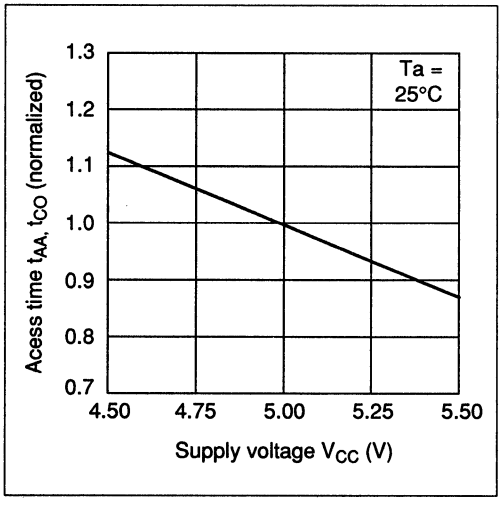
Supply Current vs. Ambient Temperature (1)



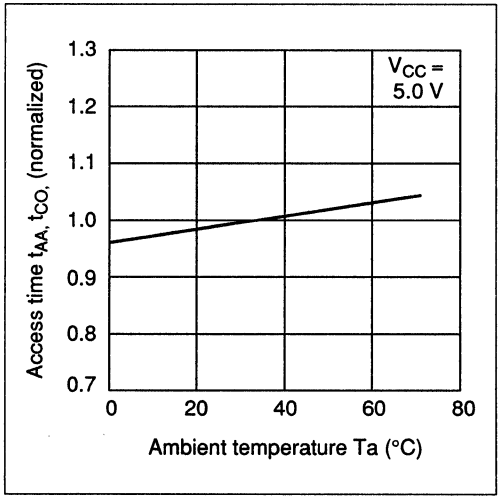
Supply Current vs. Ambient Temperature (2)



Supply Current vs. Ambient Temperature (3)

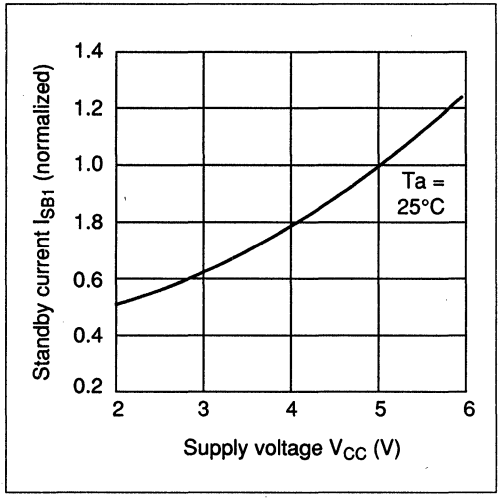


Access Time vs. Supply Voltage

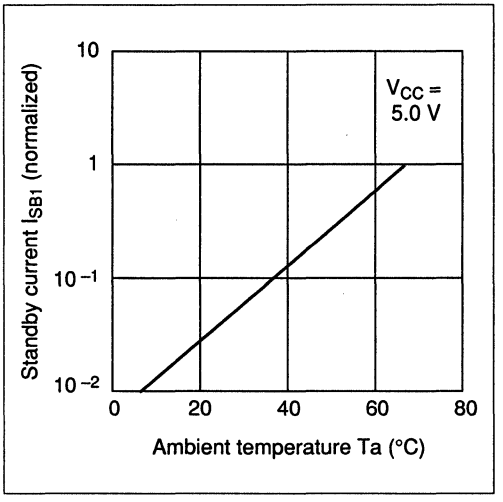


Access Time vs. Ambient Temperature

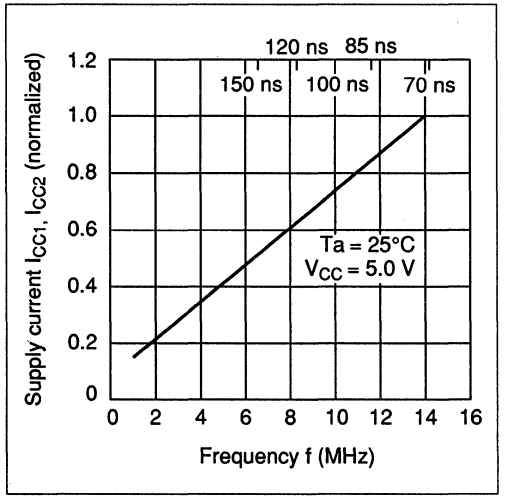
5



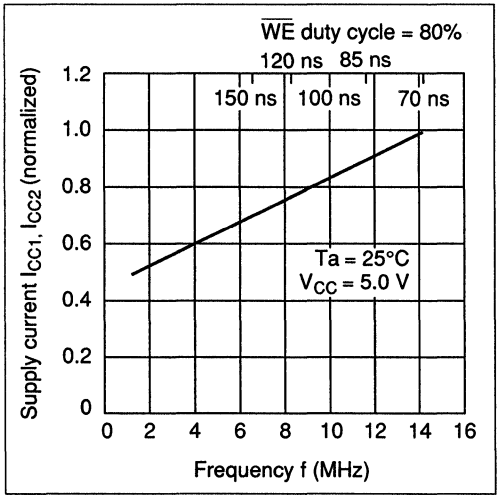
Standby Current vs. Supply Voltage



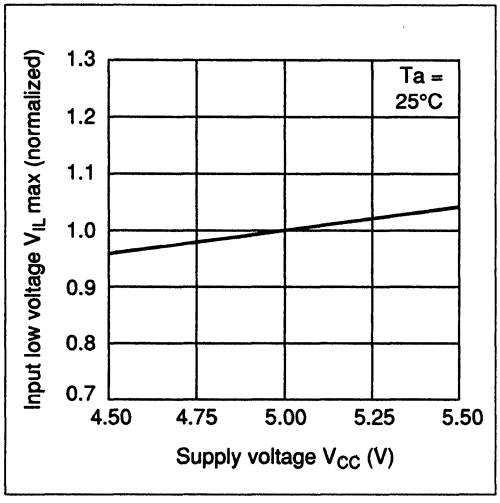
Standby Current vs. Ambient Temperature



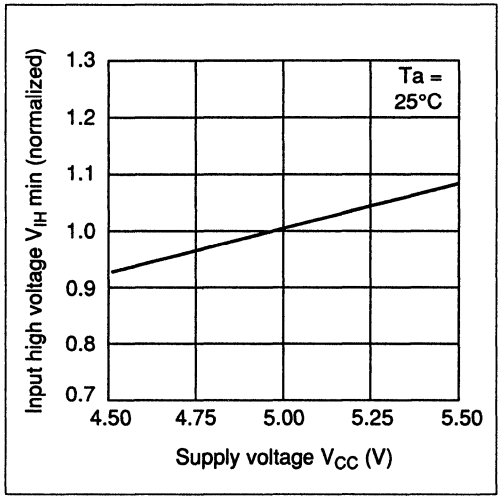
Supply Current vs. Frequency (Read)



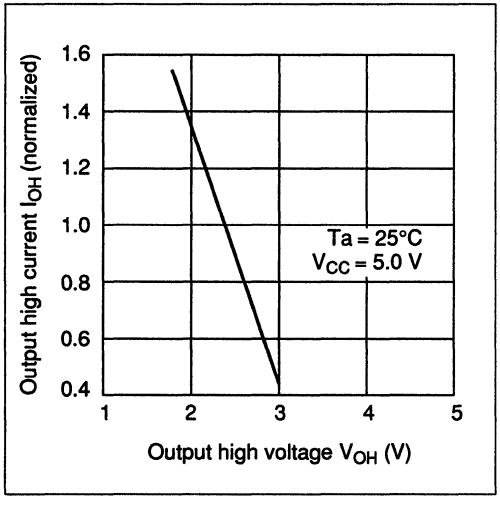
Supply Current vs. Frequency (Write)



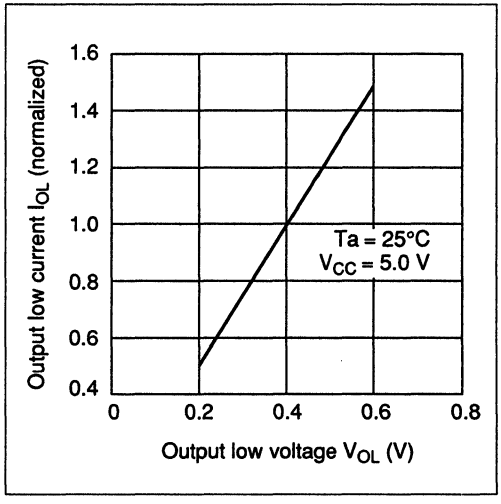
Input Low Voltage vs. Supply Voltage



Input High Voltage vs. Supply Voltage

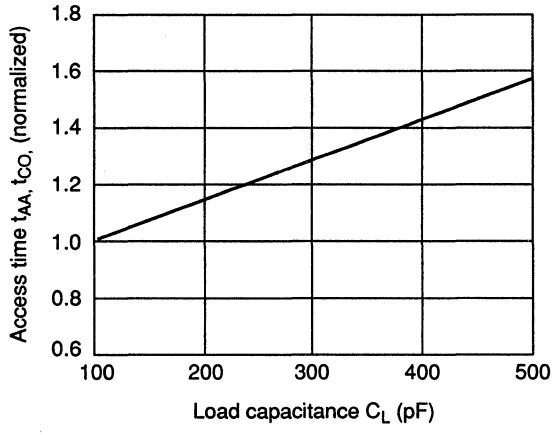


Output Higet vs. Output High Voltage



Output Low Current vs. Output Low Voltage

5



Access Time vs. Load Capacitance

HM628128A Series

131,072-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM628128A is a CMOS static RAM organized 128 kword × 8 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- High speed
  - Fast access time: 55/70/85/100 ns (max)
- Low power
  - Active: 75 mW (typ)
  - Standby: 10 µW (typ) (L/L-L/L-SL version)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery back up operation (L/L-L/L-SL version)
  - 2 chip selection for battery back up

Ordering Information

Type No.	Access time	Package
HM628128ALP–5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628128ALP–7	70 ns	
HM628128ALP–8	85 ns	
HM628128ALP–10	100 ns	
HM628128ALP–5L	55 ns	
HM628128ALP–7L	70 ns	
HM628128ALP–8L	85 ns	
HM628128ALP–10L	100 ns	
HM628128ALFP–5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628128ALFP–7	70 ns	
HM628128ALFP–8	85 ns	
HM628128ALFP–10	100 ns	
HM628128ALFP–5L	55 ns	
HM628128ALFP–7L	70 ns	
HM628128ALFP–8L	85 ns	
HM628128ALFP–10L	100 ns	
HM628128ALFP–5SL	55 ns	
HM628128ALFP–7SL	70 ns	
HM628128ALFP–8SL	85 ns	
HM628128ALFP–10SL	100 ns	
HM628128ALT–5	55 ns	8 mm × 20 mm 32-pin TSOP (normal type) (TFP-32D)
HM628128ALT–7	70 ns	
HM628128ALT–8	85 ns	
HM628128ALT–10	100 ns	
HM628128ALT–5L	55 ns	
HM628128ALT–7L	70 ns	
HM628128ALT–8L	85 ns	
HM628128ALT–10L	100 ns	
HM628128ALR–5	55 ns	8 mm × 20 mm 32-pin TSOP (reverse type) (TFP-32DR)
HM628128ALR–7	70 ns	
HM628128ALR–8	85 ns	
HM628128ALR–10	100 ns	
HM628128ALR–5L	55 ns	
HM628128ALR–7L	70 ns	
HM628128ALR–8L	85 ns	
HM628128ALR–10L	100 ns	

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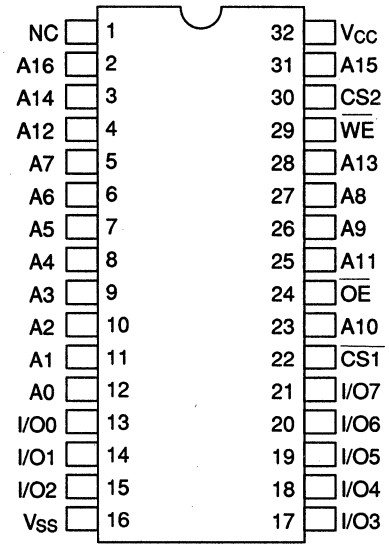
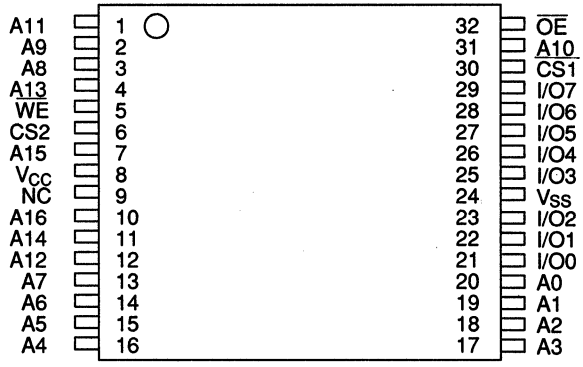
Pin Arrangement

HM628128ALP/ALFP Series



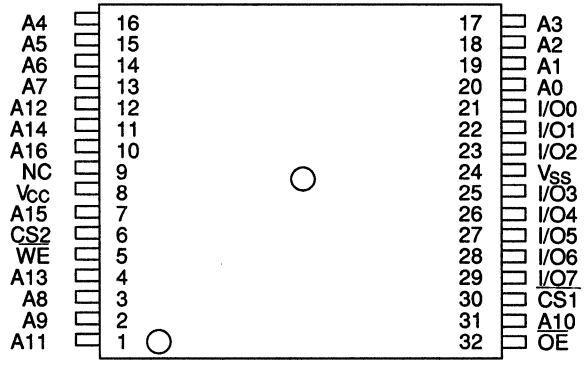
(Top View)

HM628128ALT Series



(Top View)

HM628128ALR Series



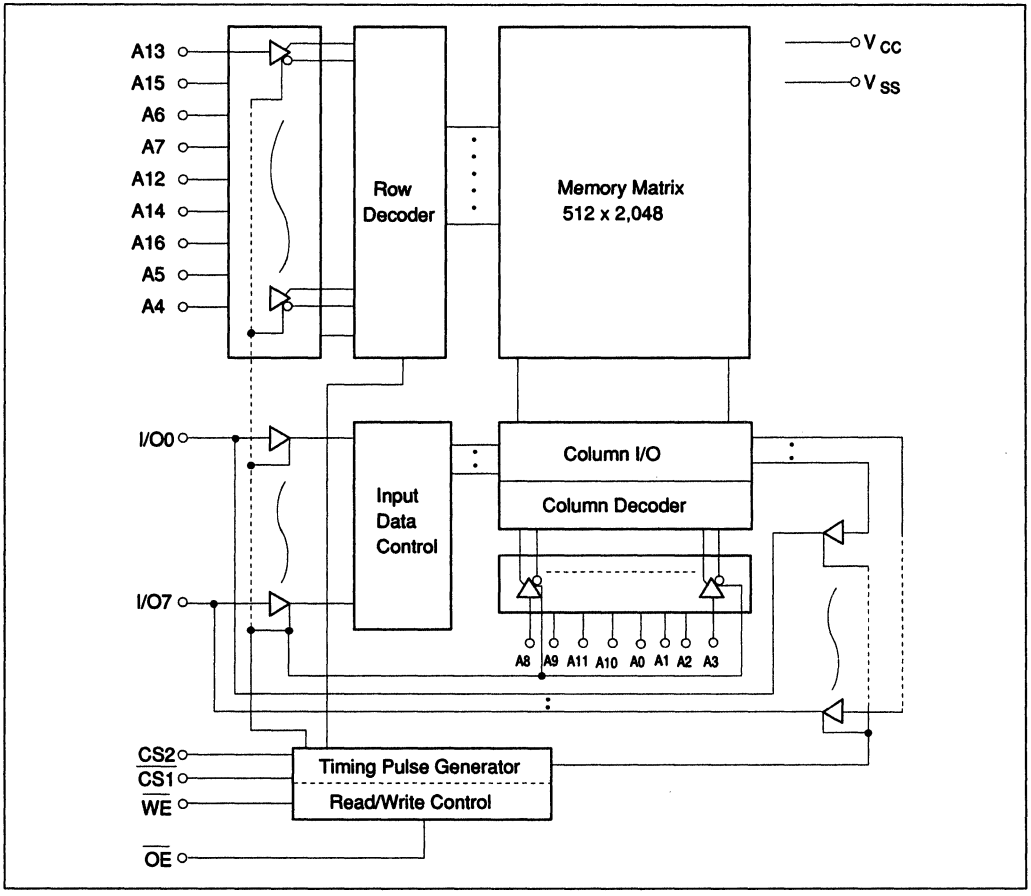
(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable

Pin name	Function
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5 *1 to V_{CC} + 0.3*2	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –3.0 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 7.0V.

5

Function Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage (HM628128A-7/8/10)	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3 *1	—	0.8	V
Input voltage (HM628128A-5)	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	–0.3 *1	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	1.0	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1.0	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC}	—	15	30	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	HM628128A -7/8/10
		—	50	80	mA		HM628128A -5
	I_{CC2}	—	15	25	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 > VCC – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V	
Standby power supply current: DC	I_{SB}	—	1	2	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}	
Standby power supply current (1): DC	I_{SB1}	—	0.02	2	mA	0 V ≤ Vin ≤ V_{CC}, $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V	
		—	2	100	µA		L-version
		—	2	50	µA		L-L/L-SL version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

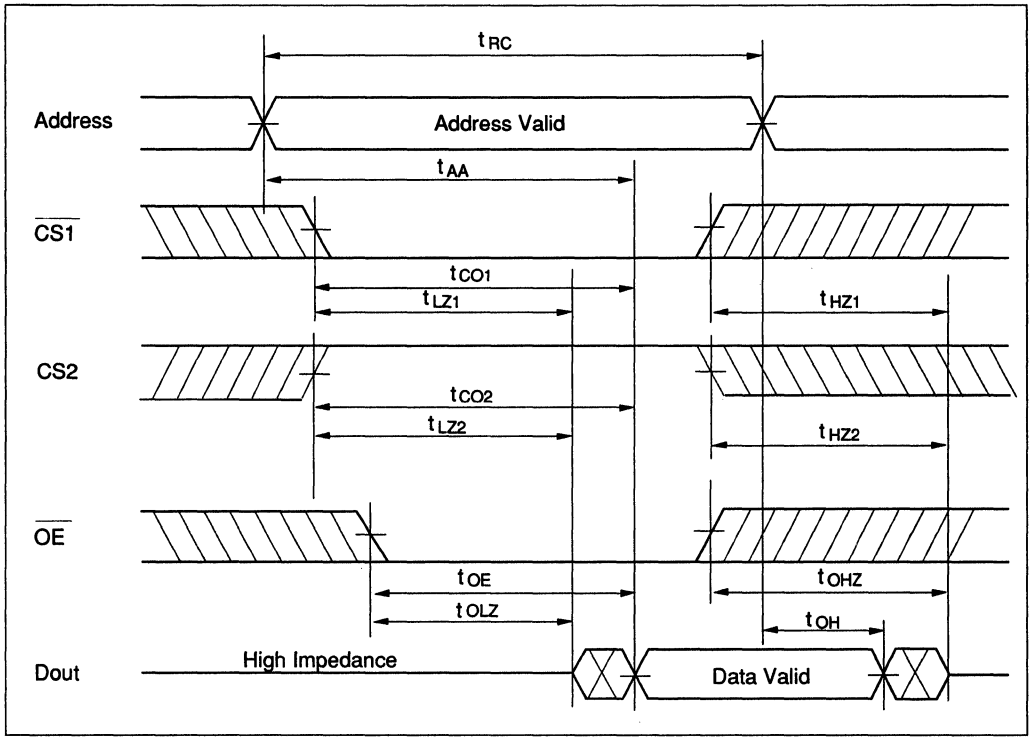
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V (HM628128A-7/8/10)
  0 V to 3 V (HM628128A-5)
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100 pF) (HM628128A-7/8/10)
  1 TTL Gate and CL (30 pF) (HM628128A-5)
  (Including scope & jig)

Read Cycle

		HM628128A									
		-5		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	55	—	70	—	85	—	100	—	ns	
Address access time	t_{AA}	—	55	—	70	—	85	—	100	ns	
Chip selection to output valid	t_{CO1}	—	55	—	70	—	85	—	100	ns	
	t_{CO2}	—	55	—	70	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	30	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	t_{LZ1}	5	—	10	—	10	—	10	—	ns	1, 2, 3
	t_{LZ2}	5	—	10	—	10	—	10	—	ns	1, 2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	1, 2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	20	0	25	0	30	0	35	ns	1, 2, 3
	t_{HZ2}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns	

Read Timing Waveform *4



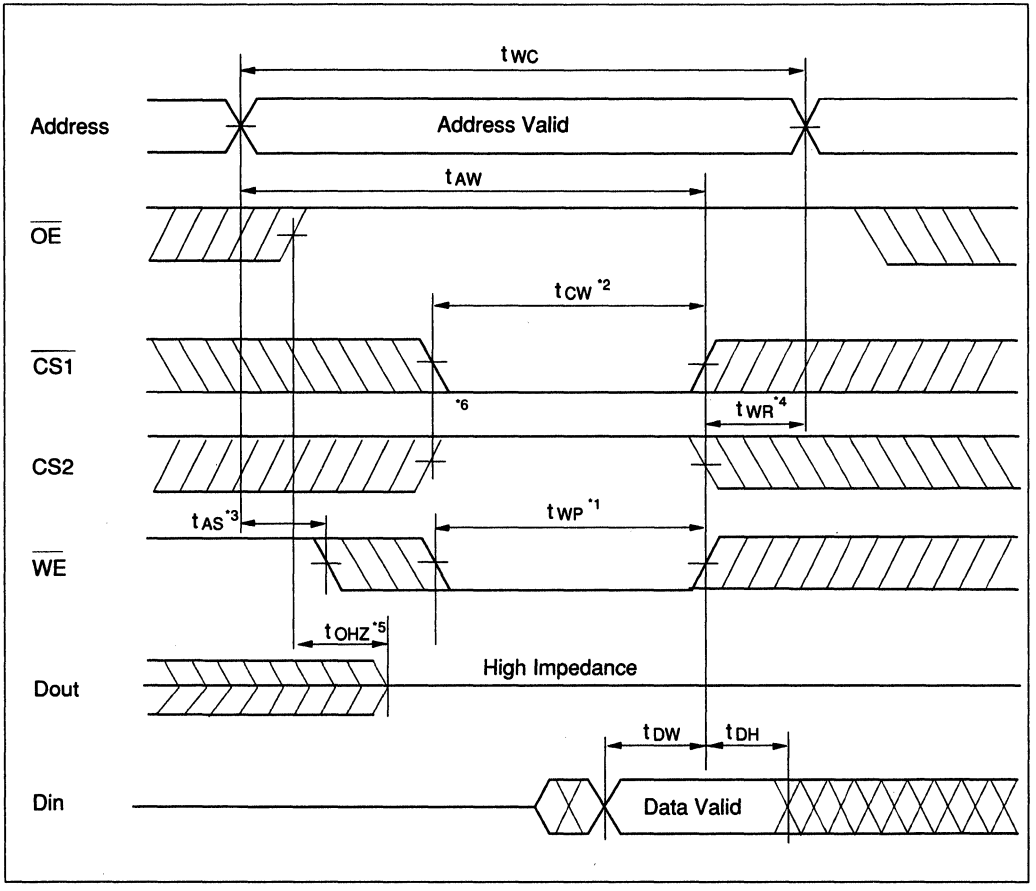
Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for read cycle.

5

Write Cycle

		HM628128A									
		-5		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	55	—	70	—	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	75	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	t_{AW}	50	—	60	—	75	—	80	—	ns	
Write pulse width	t_{WP}	40	—	50	—	55	—	60	—	ns	
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns	
		0	—	0	—	0	—	0	—	ns	11
Write to output in high-Z	t_{WHZ}	0	20	0	25	0	30	0	35	ns	10
Data to write time overlap	t_{DW}	25	—	30	—	35	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



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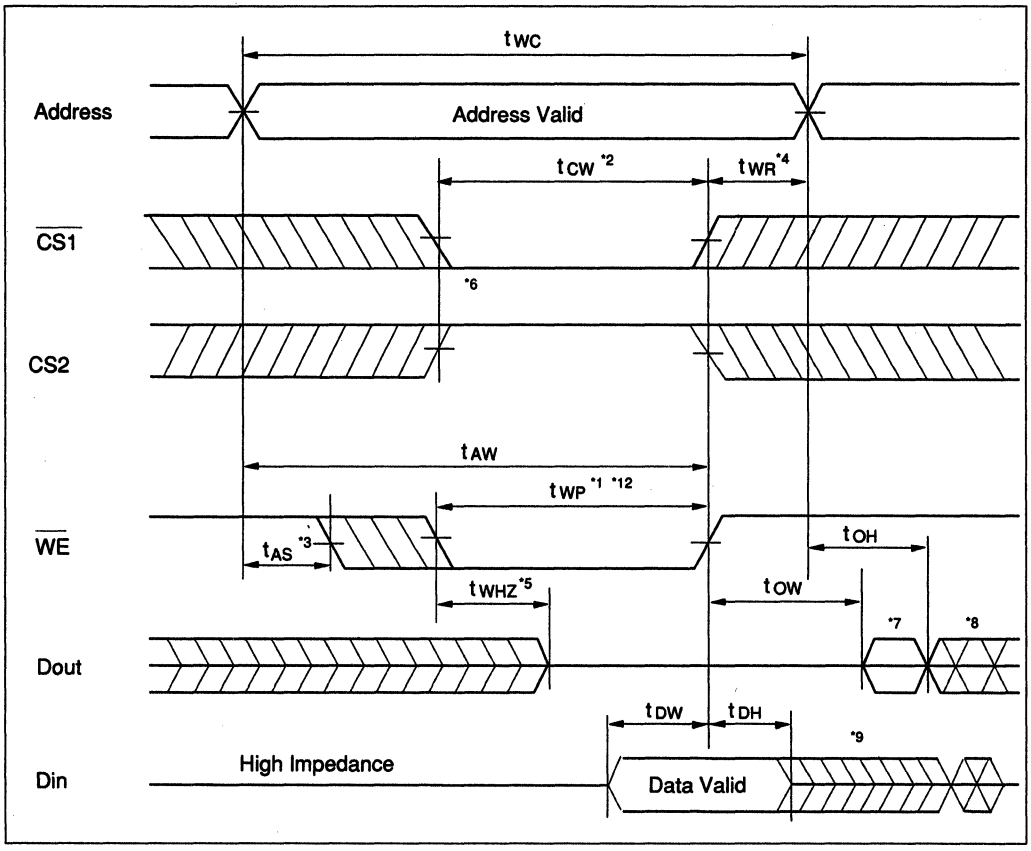
Write Timing Waveform (2) ($\overline{OE}$ low Fixed)



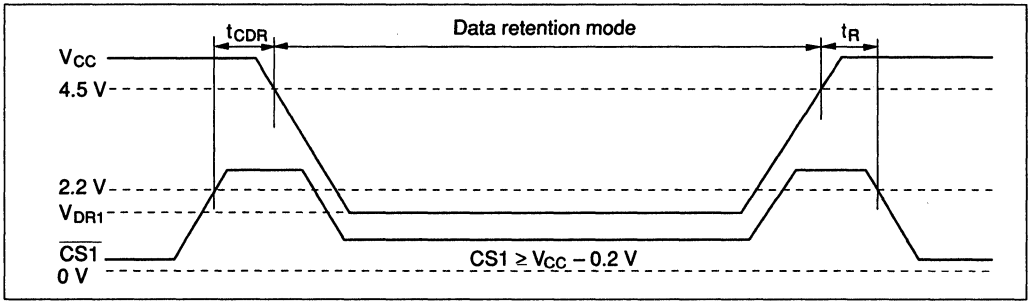
Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after the $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. This value is measured from CS2 going low to the end of write cycle.
12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.
    $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

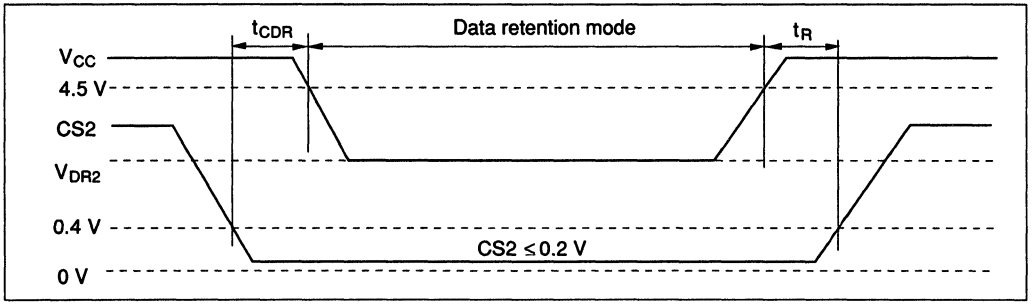
This characteristics is guaranteed only for L, L-L, and L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V or $0\ V \leq CS2 \leq 0.2$ V, $Vin \geq 0$ V	
Data retention current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3.0 V, $Vin \geq 0$ V, $\overline{CS1} \geq V_{CC} - 0.2$V	L version
		—	1	30*2	µA	$CS2 \geq V_{CC} - 0.2$ V or $0\ V \leq CS2 \leq 0.2$ V	L-L version
		—	1	15*3	µA		L-S version
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform	
Operation recovery time	t_R	5	—	—	ms		

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: 1. 20 µA max at Ta = 0 to 40°C (L version).
2. 6 µA max at Ta = 0 to 40°C (L-L version).
3. 3 µA max at Ta = 0 to 40°C (L-SL version).
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2$ V or $0\ V \leq CS2 \leq 0.2$ V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM629128 Series — Preliminary

131,072-word × 9-bit High Speed CMOS Static RAM

The Hitachi HM629128 is a CMOS static RAM organized 128 kword × 9 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards.

Features

- High speed
  - Fast access time: 70/85/100 ns (max)
- Low power
  - Active: 75 mW (typ)
  - Standby: 10 µW (typ) (L-/L-L/L-SL version)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery back up operation (L-/L-L/L-SL version)

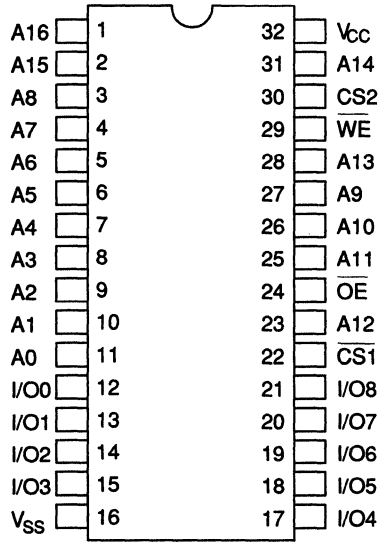
Ordering Information

Type No.	Access time	Package
HM629128LP–7	70 ns	600-mil 32-pin plastic DIP (DP-32)
HM629128LP–8	85 ns	
HM629128LP–10	100 ns	
HM629128LP–7L	70 ns	
HM629128LP–8L	85 ns	
HM629128LP–10L	100 ns	
HM629128LP–7SL	70 ns	
HM629128LP–8SL	85 ns	
HM629128LP–10SL	100 ns	
HM629128LFP–7	70 ns	525-mil 32-pin plastic SOP (FP-32D)
HM629128LFP–8	85 ns	
HM629128LFP–10	100 ns	
HM629128LFP–7L	70 ns	
HM629128LFP–8L	85 ns	
HM629128LFP–10L	100 ns	
HM629128LFP–7SL	70 ns	
HM629128LFP–8SL	85 ns	
HM629128LFP–10SL	100 ns	
HM629128LT–7	70 ns	8 mm x 20 mm 32-pin TSOP (normal type) (TFP-32D)
HM629128LT–8	85 ns	
HM629128LT–10	100 ns	
HM629128LT–7L	70 ns	
HM629128LT–8L	85 ns	
HM629128LT–10L	100 ns	
HM629128LT–7SL	70 ns	
HM629128LT–8SL	85 ns	
HM629128LT–10SL	100 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

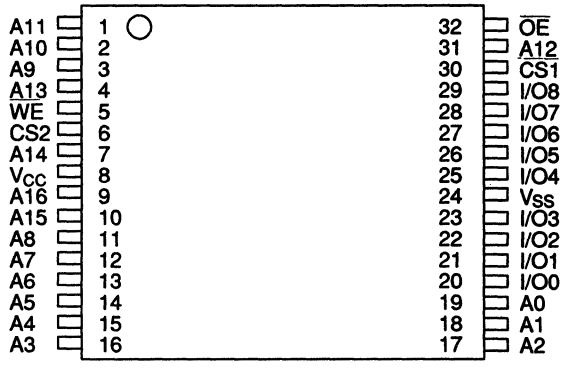
Pin Arrangement

HM629128LP/LFP Series



(Top view)

HM629128LT Series



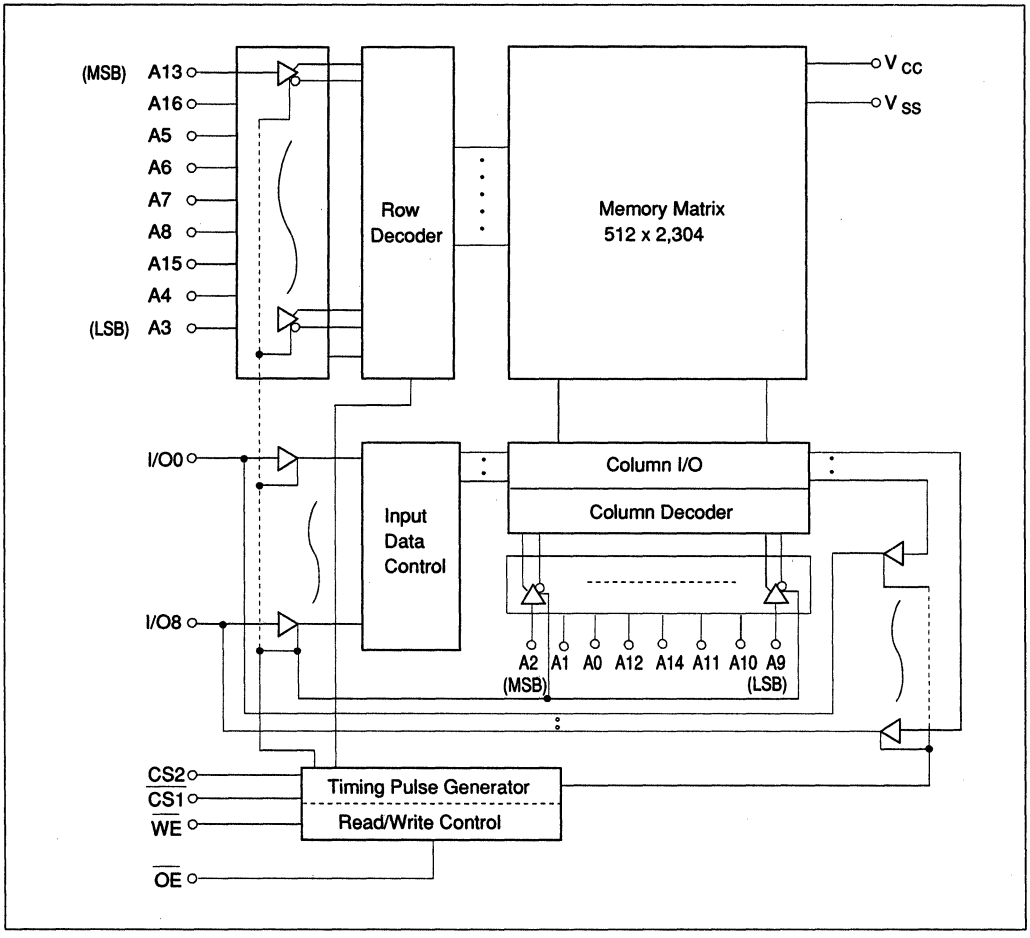
(Top view)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O8	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

5

Block Diagram



Function Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5 *1 to V_{CC} + 0.3*2	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –3.0 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 7.0V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage (HM629128-7/8/10)	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3 *1	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC}	—	15	35	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA	
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA	
	I_{CC2}	—	15	30	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 > VCC − 0.2 V V_{IH} ≥ V_{CC} − 0.2 V, V_{IL} ≤ 0.2 V	
Standby power supply current: DC	I_{SB}	—	1	3	mA	(1) $\overline{CS1}$ = V_{IH}, CS2 = V_{IH} (2) CS2 = V_{IL}	
Standby power supply current (1): DC	I_{SB1}	—	2	115	µA	(1) Vcc ≥ Vin ≥ 0 V $\overline{CS1}$ ≥ V_{CC} − 0.2 V, CS2 ≥ V_{CC} − 0.2 V	L-version
		—	2	60	µA	(2) V_{CC} ≥ Vin ≥ 0 V 0.2 V ≥ CS2 ≥ 0 V	L-L/L-SL version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8V to 2.4V (HM629128-7/8/10)
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100pF) (HM629128-7/8/10)
  (Including scope & jig)

Read Cycle

		HM629128							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	70	—	85	—	100	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	ns	
Chip selection to output valid	t_{CO1}	—	70	—	85	—	100	ns	
	t_{CO2}	—	70	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	40	—	45	—	50	ns	
Chip selection to output in low-Z	t_{LZ1}	10	—	10	—	10	—	ns	2
	t_{LZ2}	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{HZ1}	0	25	0	30	0	35	ns	1, 2
	t_{HZ2}	0	25	0	30	0	35	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	0	35	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns	

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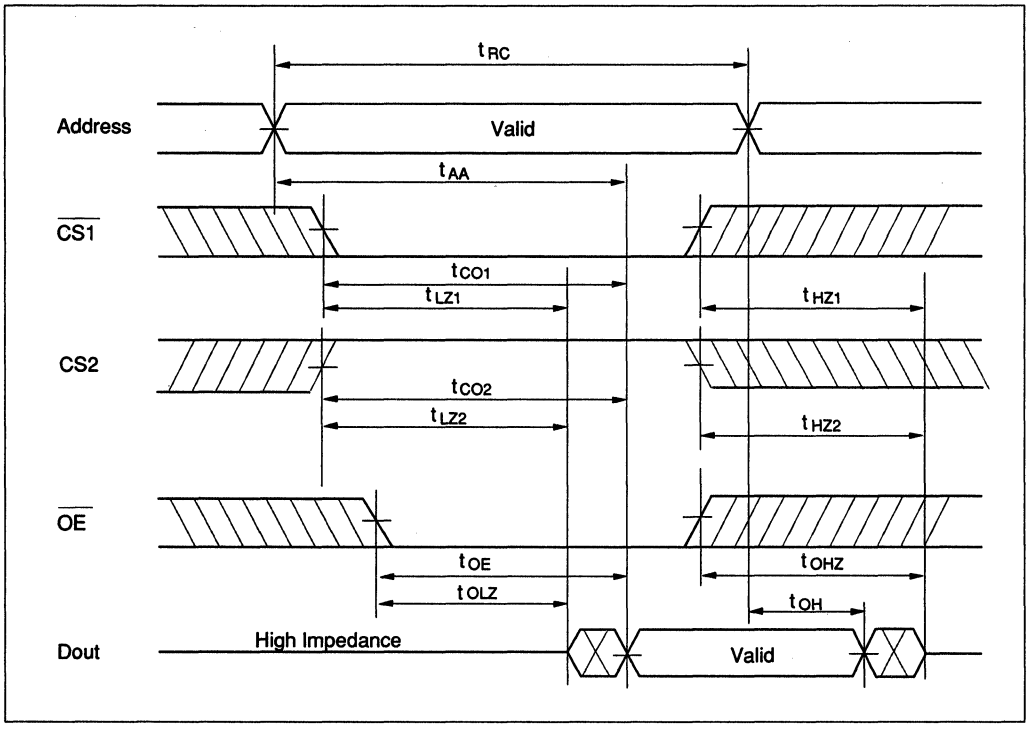
Read Timing Waveform *3



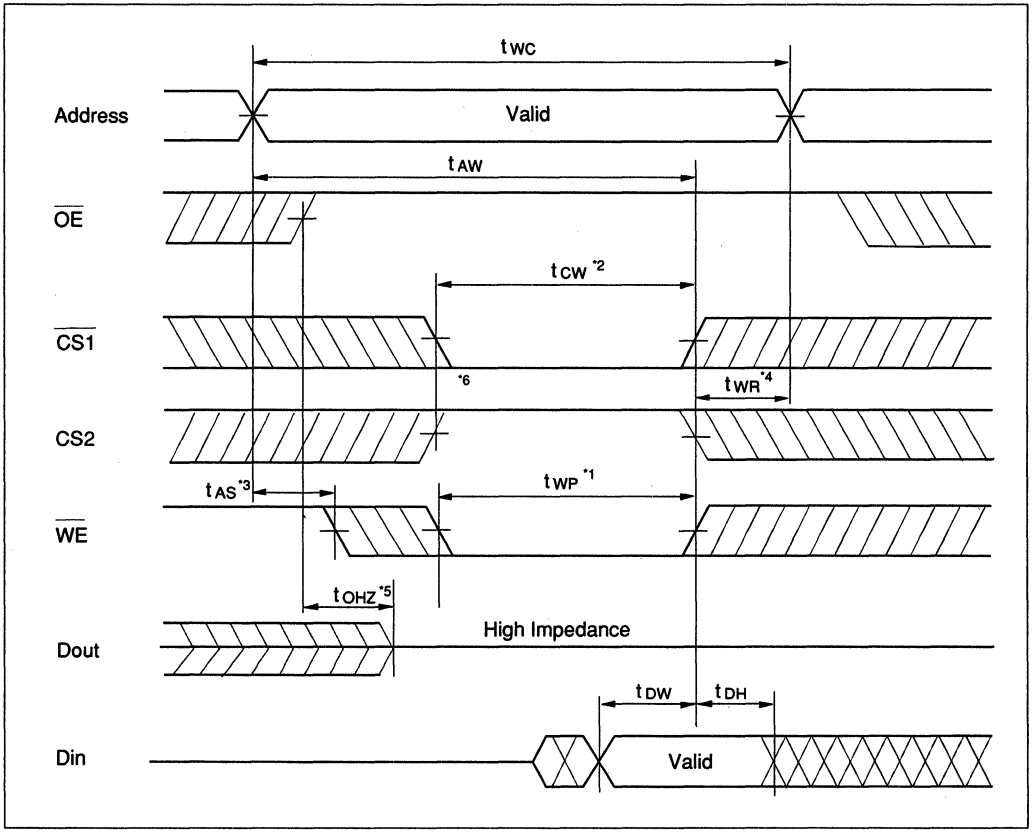
Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.

Write Cycle

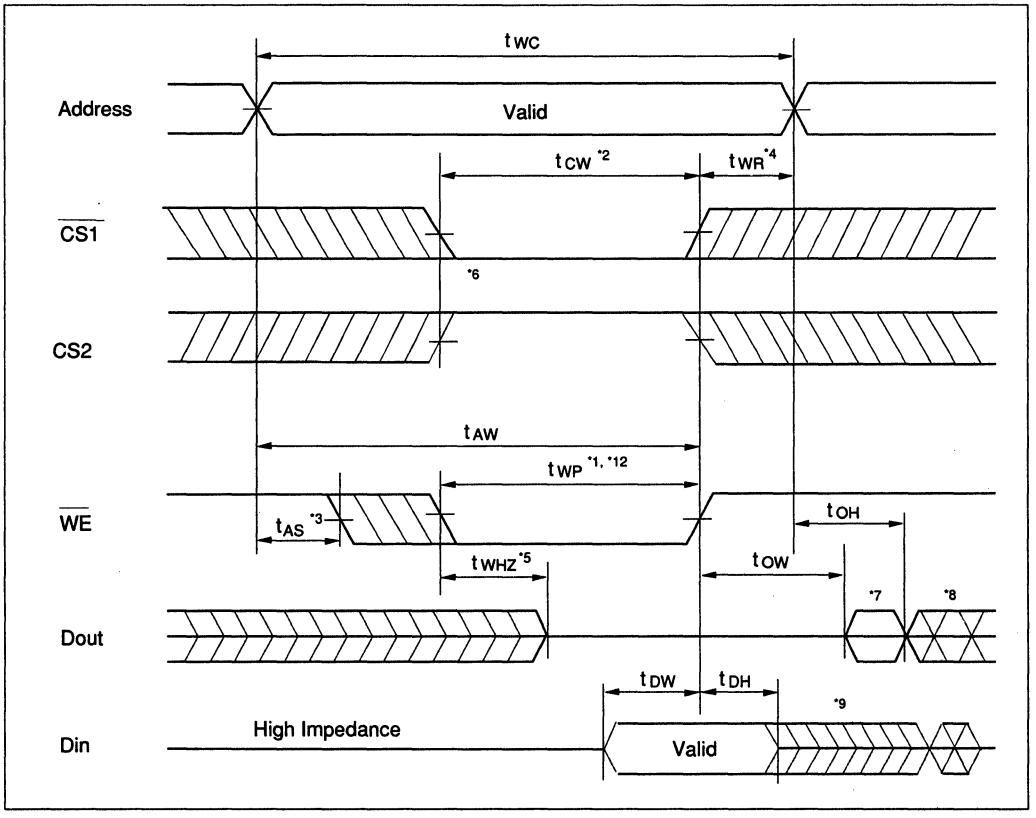
		HM629128							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	70	—	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	
Address valid to end of write	t_{AW}	60	—	75	—	80	—	ns	
Write pulse width	t_{WP}	50	—	55	—	60	—	ns	
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	
		0	—	0	—	0	—	ns	11
Write to output in high-Z	t_{WHZ}	0	25	0	30	0	35	ns	10
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns	10

5

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



Notes:
1. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after the $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. This value is measured from CS2 going low to the end of write cycle.
12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.

    $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

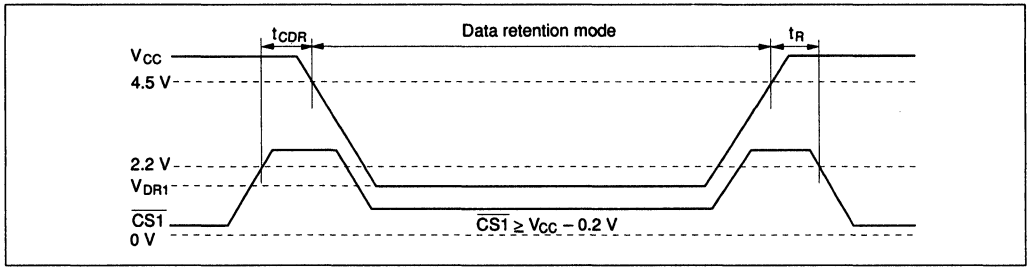
5

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

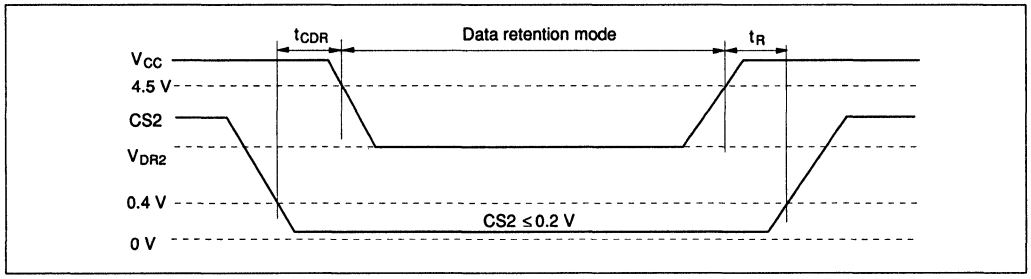
This characteristics is guaranteed only for L, L-L, and L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
V_{CC} for data retention	V_{DR}	2.0	—	—	V	(1) $\overline{CS1} \geq V_{CC} - 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V, $Vin \geq 0$V or (2) 0 V $\leq CS2 \leq$ 0.2 V, $Vin \geq 0$ V	
Data retention current	I_{CCDR}	—	1	60*1	µA	V_{CC} = 3.0 V, $V_{CC} \geq Vin \geq 0$V	Lversion
		—	1	40*2	µA	(1) $\overline{CS1} \geq V_{CC} - 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V or (2) 0 V $\leq CS2 \leq$ 0.2 V	L-Lversion
		—	1	20*3	µA		L-SLversion
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform	
Operation recovery time	t_R	5	—	—	ms		

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: 1. 25 µA max at Ta = 0 to 40°C (Lversion).
2. 8 µA max at Ta = 0 to 40°C (L-Lversion).
3. 5 µA max at Ta = 0 to 40°C (L-SLversion).
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 > V_{CC} – 0.2 V or 0 V < CS2 < 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

5

HM628512 Series

524288-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM628512 is a 4M-bit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5 µm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400 mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. LP-version is suitable for battery back up system.

Features

- High speed: Fast access time 55/70/85/100 ns (max)
- Low power
  Standby: 10 µW (typ) (L/L-SL version)
  Operation: 75 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L/L-SL version)

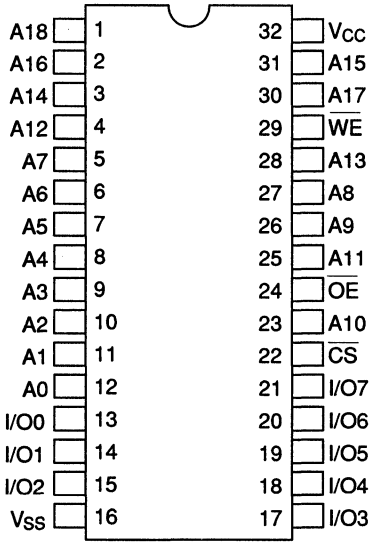
Ordering Information

Type No.	Access time	Package
HM628512P-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512P-7	70 ns	
HM628512P-8	85 ns	
HM628512P-10	100 ns	
HM628512LP-5	55 ns	
HM628512LP-7	70 ns	
HM628512LP-8	85 ns	
HM628512LP-10	100 ns	
HM628512LP-5SL	55 ns	
HM628512LP-7SL	70 ns	
HM628512LP-8SL	85 ns	
HM628512LP-10SL	100 ns	
HM628512FP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512FP-7	70 ns	
HM628512FP-8	85 ns	
HM628512FP-10	100 ns	
HM628512LFP-5	55 ns	
HM628512LFP-7	70 ns	
HM628512LFP-8	85 ns	
HM628512LFP-10	100 ns	
HM628512LFP-5SL	55 ns	
HM628512LFP-7SL	70 ns	
HM628512LFP-8SL	85 ns	
HM628512LFP-10SL	100 ns	
HM628512LTT-5*1	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512LTT-7*1	70 ns	
HM628512LTT-8*1	85 ns	
HM628512LTT-10*1	100 ns	
HM628512LTT-5SL*1	55 ns	
HM628512LTT-7SL*1	70 ns	
HM628512LTT-8SL*1	85 ns	
HM628512LTT-10SL*1	100 ns	
HM628512LRR-5*1	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512LRR-7*1	70 ns	
HM628512LRR-8*1	85 ns	
HM628512LRR-10*1	100 ns	
HM628512LRR-5SL*1	55 ns	
HM628512LRR-7SL*1	70 ns	
HM628512LRR-8SL*1	85 ns	
HM628512LRR-10SL*1	100 ns	

Note: 1. Preliminary

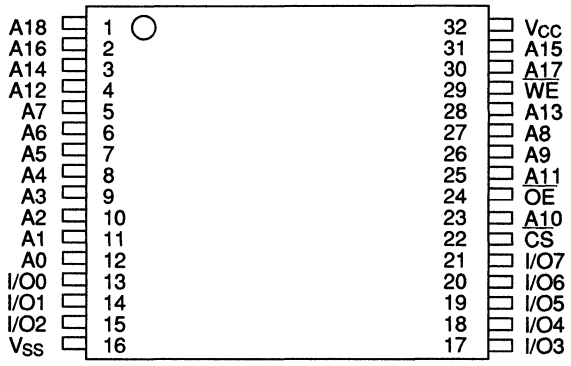
Pin Arrangement

HM628512P/FP Series



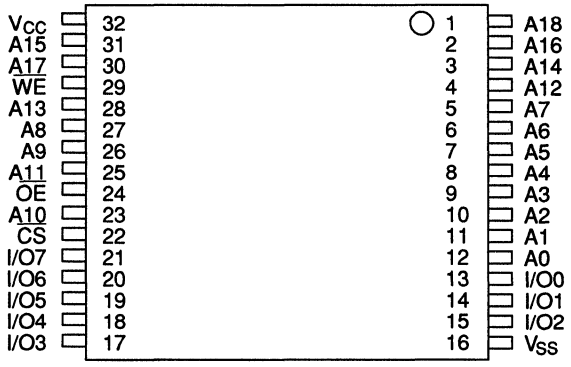
(Top View)

HM628512TT Series



(Top View)

HM628512RR Series



(Top View)

Pin Description

Symbol	Function	Symbol	Function
A0 – A18	Address	$\overline{OE}$	Output enable
I/O0 – I/O7	Input/output	V_{CC}	Power supply
$\overline{CS}$	Chip select	V_{SS}	Ground
$\overline{WE}$	Write enable		

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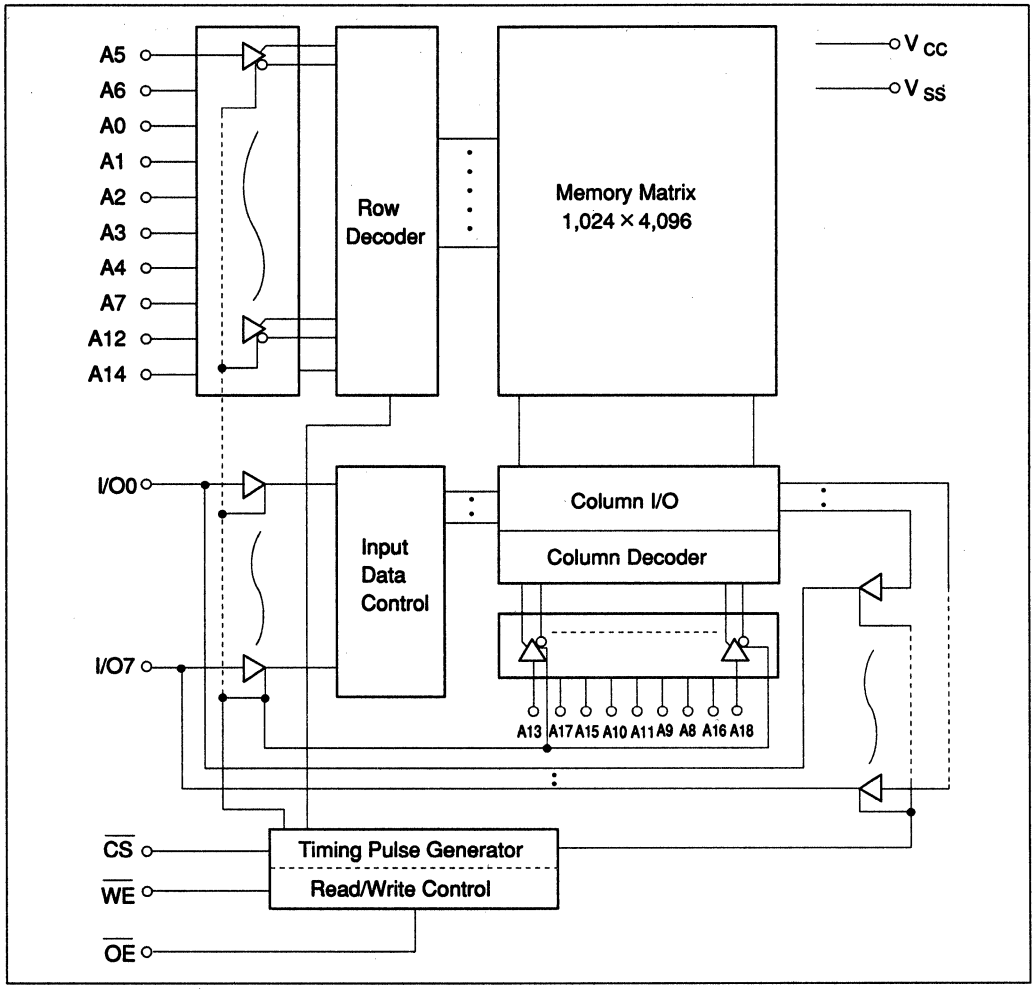
Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	Dout pin	Ref. cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5^{*1} to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	-0.3^{*1}	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC		I_{CCREAD}	—	15	25	mA	$\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
		$I_{CCWRITE}$	—	20	45	mA	$\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IL}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating power supply current	–5	I_{CC1}	—	70	100	mA	Min cycle, duty = 100% $\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	–7		—	60	90	mA	
	–8/10		—	55	80	mA	
		I_{CC2}	—	15	35	mA	Cycle time = 1 µs, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC		I_{SB}	—	1	3	mA	$\overline{CS}$ = V_{IH}
Standby power supply current (1): DC		I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V, $\overline{CS}$ ≥ V_{CC} – 0.2 V
			—	2	100*2	µA	
			—	2	50*3	µA	
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage		V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1 MHz)*1

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

		HM628512-5		HM628512-7		HM628512-8		HM628512-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	55	—	70	—	85	—	100	—	ns	
Address access time	t_{AA}	—	55	—	70	—	85	—	100	ns	
Chip select access time	t_{CO}	—	55	—	70	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	25	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	t_{LZ}	10	—	10	—	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{HZ}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

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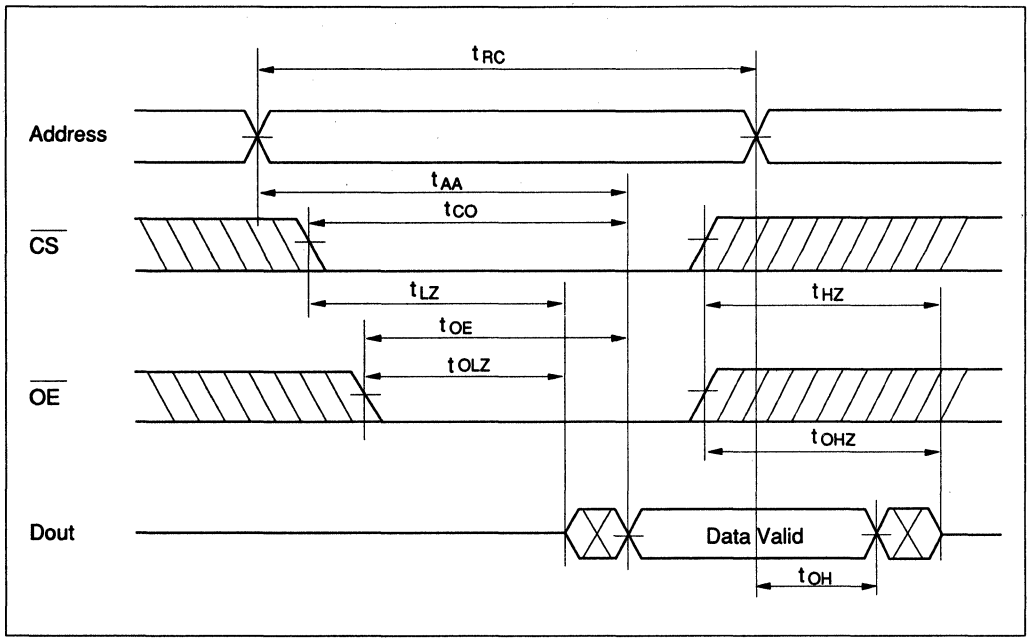
Read Timing Waveform[*4]



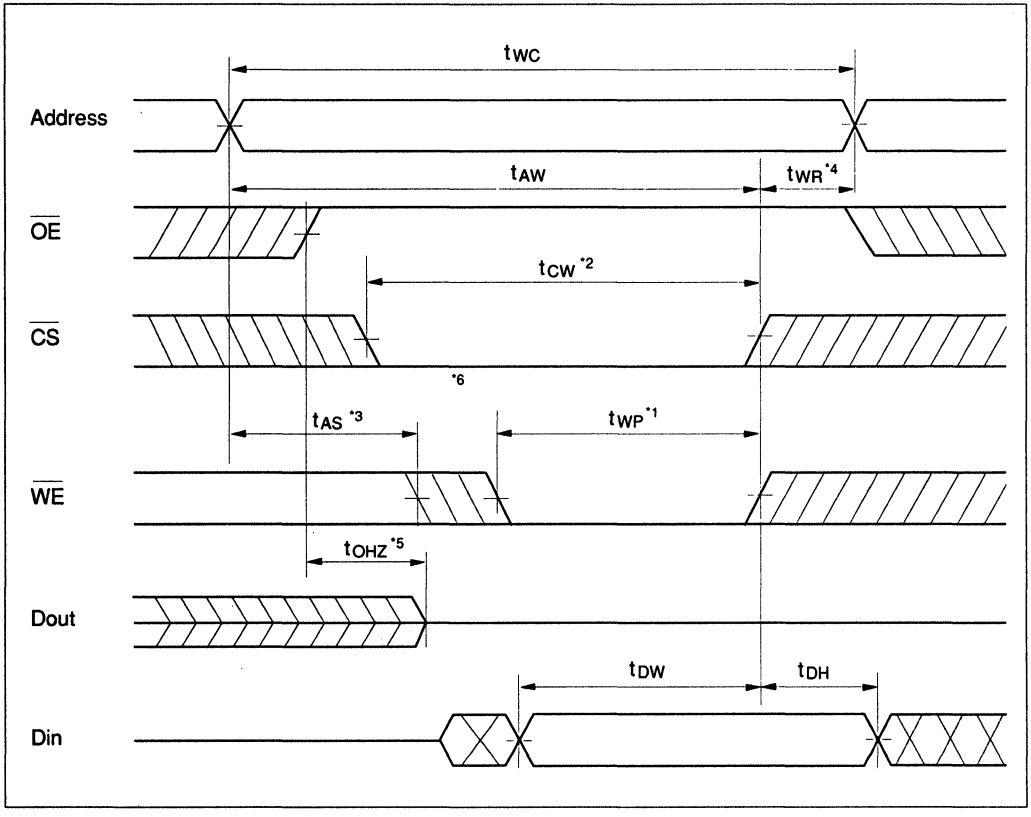
Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min.
3. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for read cycle.

Write Cycle

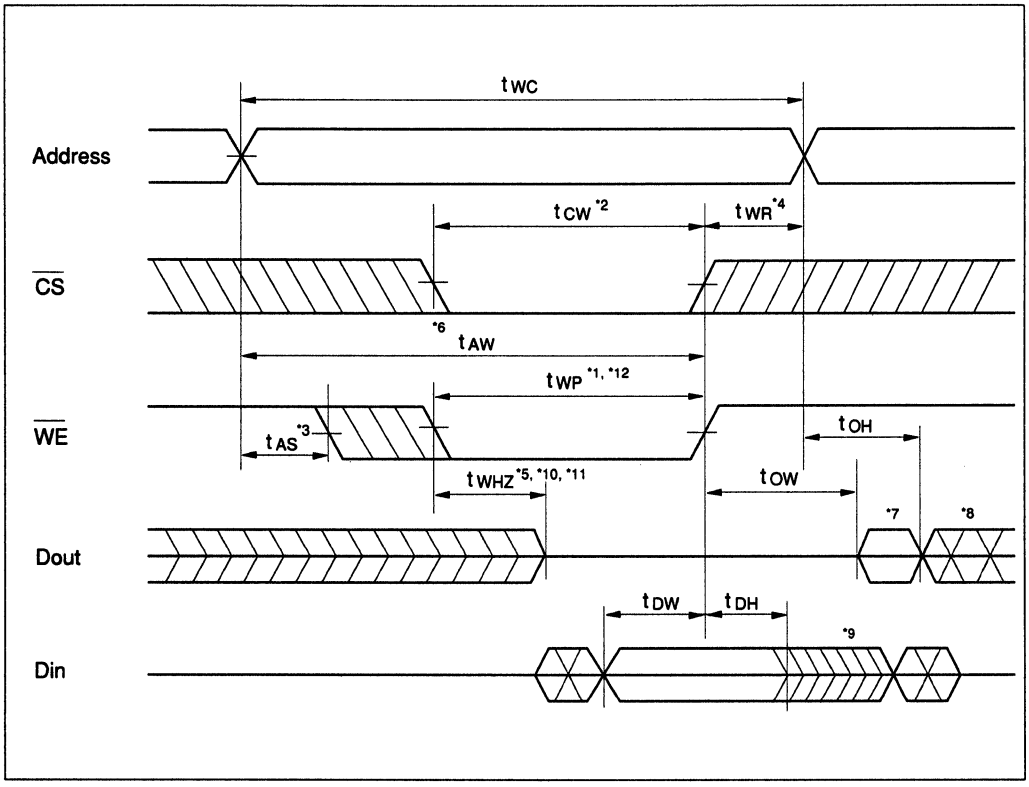
		HM628512-5		HM628512-7		HM628512-8		HM628512-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Write cycle time	t_{WC}	55	—	70	—	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	75	—	80	—	ns	2
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	50	—	60	—	75	—	80	—	ns	
Write pulse width	t_{WP}	40	—	50	—	55	—	60	—	ns	1, 12
Write recovery time	t_{WR}	5	—	5	—	5	—	5	—	ns	4
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	20	0	25	0	30	0	35	ns	10, 11
Data to write time overlap	t_{DW}	25	—	30	—	35	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10

5

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
7. Dout is the same phase of the write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not refered to output voltage levels.
12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.

    $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

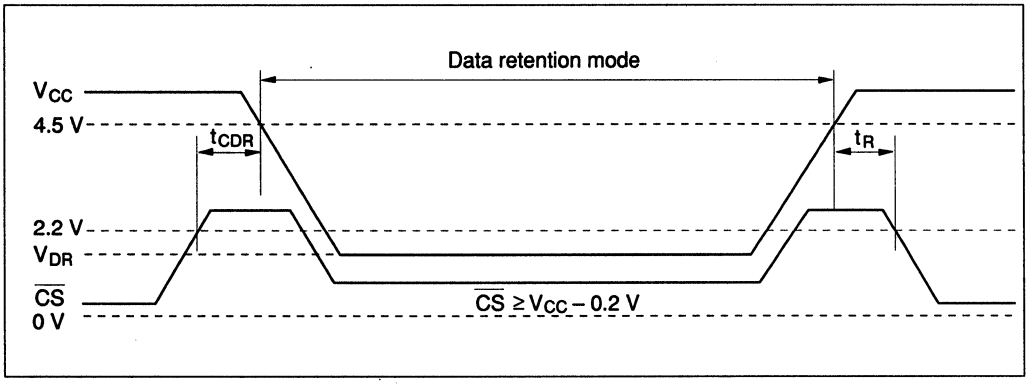
5

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L/L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*3
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3.0 V, Vin ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	1	15*2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Low V_{CC} Data Retention Timing Waveform ($\overline{CS}$ Controlled)



Notes: 1. For L-version and 20 µA max. at Ta = 0 to 40°C.
2. For SL-version and 3 µA max. at Ta = 0 to 40°C.
3. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. In data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM62W256 Series

3.0 V & 3.3 V Supply

32,768-Word × 8-Bit Low Voltage Operation CMOS Static RAM

Features

- Low voltage operation SRAM
  Single 3.3 V Supply
- 0.8 μm Hi-CMOS process
- High speed
  Access time: 70/85 ns (max)
- Low power
  Standby: 0.66 μW (typ)
  Operation: 17 mW (typ) (f = 1 MHz)
- Completely static memory
  No clock or timing strobe required
- Directly LVTTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM62W256LFP-7T	70 ns	450 mil 28-pin plastic SOP (FP-28DA)
HM62W256LFP-8T	85 ns	
HM62W256LFP-7SLT	70 ns	
HM62W256LFP-8SLT	85 ns	
HM62W256LT-7	70 ns	8 mm × 14 mm 32-pin TSOP (normal type) (TFP-32DA)
HM62W256LT-8	85 ns	
HM62W256LT-7SL	70 ns	
HM62W256LT-8SL	85 ns	

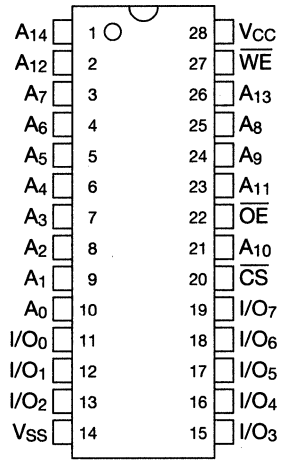
Pin Description

Symbol	Function
A_0–A_{14}	Address
I/O_0–I/O_7	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

5

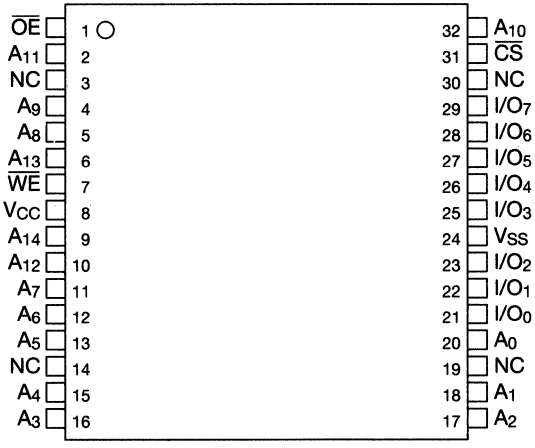
Pin Arrangement

HM62W256LFP Series



(Top View)

HM62W256LT Series



(Top View)

Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
X	H	X	Standby	I_{SB}, I_{SB1}	High-Z	—
H	L	X	Output Disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	D_{out}	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	D_{in}	Write cycle (1)
L	L	L	Write	I_{CC}	D_{in}	Write cycle (2)

Note 1. X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power Supply Voltage[1]	V_{CC}	–0.5 to 4.6	V
Terminal Voltage[1]	V_T	–0.5[2] to +V_{CC} +0.5	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature Under Bias	T_{bias}	–10 to +85	°C

Note 1. Relative to V_{SS}
2. V_T (min) = –3.0V for pulse half-width ≤ 50 ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low (Logic 0) Voltage	V_{IL}	–0.3[1]	—	0.8	V

Note 1. V_{IL} (min) = –3.0 V for pulse half-width ≤ 50 ns

5

DC Characteristics (T_a = 0 to +70°C, V_{CC} = 3.3 V ±0.3V, V_{SS} = 0 V)

Parameter		Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input Leakage Current		$\|I_{LI}\|$	—	—	1	µA	V_{in} = V_{SS} to V_{CC}
Output Leakage Current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current (DC)		I_{CCDC1}	—	1.5	5.0	mA	$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
		I_{CCDC2}	—	0.5	2.5	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, V_{IH} ≤ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V $I_{I/O}$ = 0 mA
Operating Power Supply Current	HM62W256-7	I_{CCAC1}	—	—	30	mA	min cycle, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL}
	HM62W256-8	I_{CCAC1}	—	—	27	mA	
		I_{CCAC2}	—	5	10	mA	Cycle time ≥ 1 µs, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby V_{CC} Current		I_{SB}	—	—	1	mA	$\overline{CS}$ = V_{IH}
		I_{SB1}	—	0.2	50	µA	V_{IN} ≥ 0 V, $\overline{CS}$ ≥ V_{CC} – 0.2 V
			—	0.2	10[2]	µA	
Output Low Voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2.0 mA
		V_{OL}	—	—	0.2	V	I_{OL} = 100 µA
Output High Voltage		V_{OH}	2.4	—	—	V	I_{OH} = –2.0 mA
		V_{OH}	V_{CC} –2.0	—	—	V	I_{OH} = –100 µA

Note 1. Typical values are at V_{CC} = 3.3 V, T_a = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L-SL version.

Capacitance (T_a = 25°C, f = 1.0 MHz)[1]

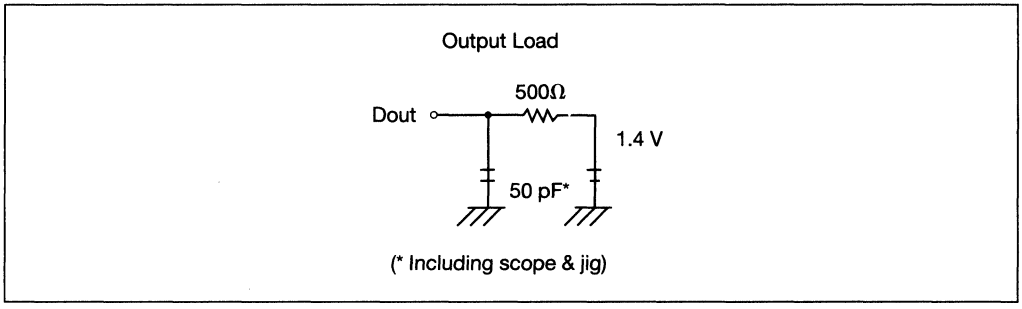
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	8	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note 1. This parameter is sampled and not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Condition

- Input pulse levels: 0.4 V to 2.4 V
- Input timing reference level: 1.4 V
- Input rise and fall times: 5ns
- Output timing reference level: 0.8 V/2.0 V

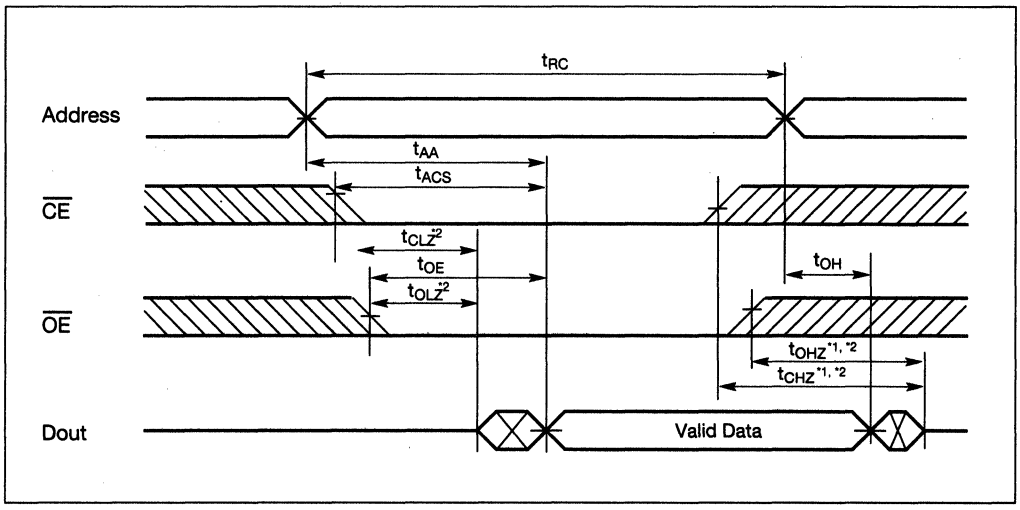


Read Cycle

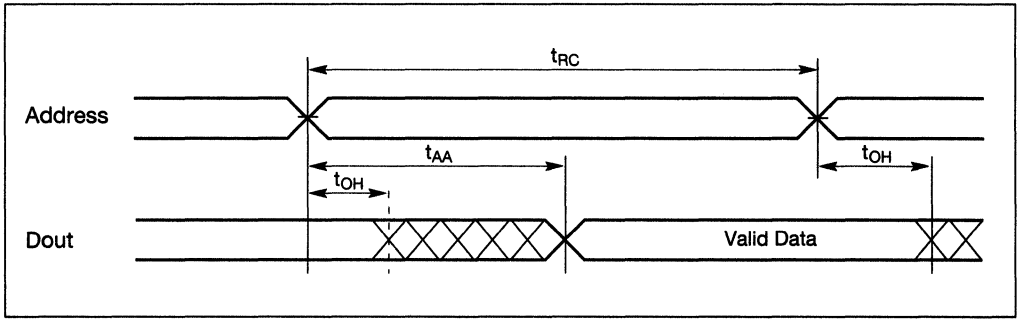
		HM62W256-7		HM62W256-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Cycle Time	t_{RC}	70	—	85	—	ns	
Address Access Time	t_{AA}	—	70	—	85	ns	
Chip Select Access Time	t_{ACS}	—	70	—	85	ns	
Output Enable to Output Valid	t_{OE}	—	35	—	45	ns	
Chip Selection to Output in Low-Z	t_{CLZ}	10	—	10	—	ns	2
Output Enable to Output in Low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip Deselection to Output in High-Z	t_{CHZ}	0	25	0	30	ns	1, 2
Output Disable to Output in High-Z	t_{OHZ}	0	25	0	30	ns	1, 2
Output Hold From Address Change	t_{OH}	10	—	10	—	ns	

5

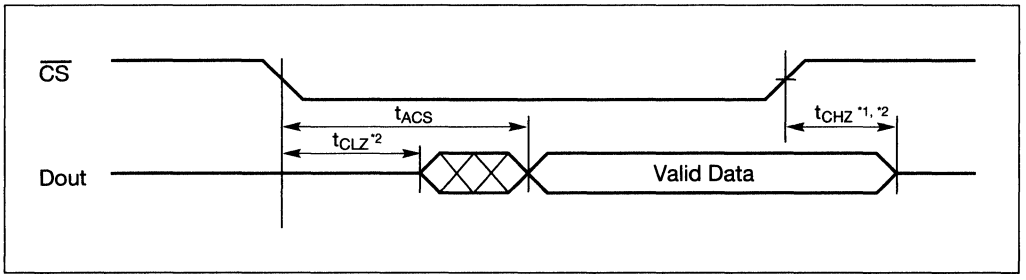
Read Timing Waveform (1) [3]



Read Timing Waveform (2) [3, 4, 6]



Read Timing Waveform (3) [3, 5, 6]



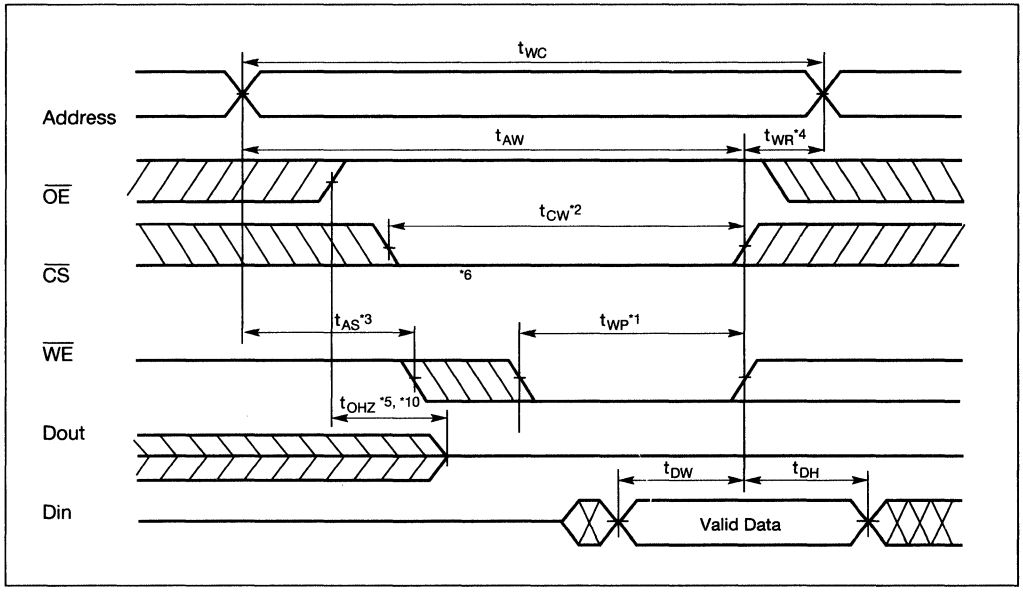
Notes:
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not refered to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.
4. Device is continuously selected, $\overline{CS} = V_{IL}$
5. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
6. $\overline{OE} = V_{IL}$

5

Write Cycle

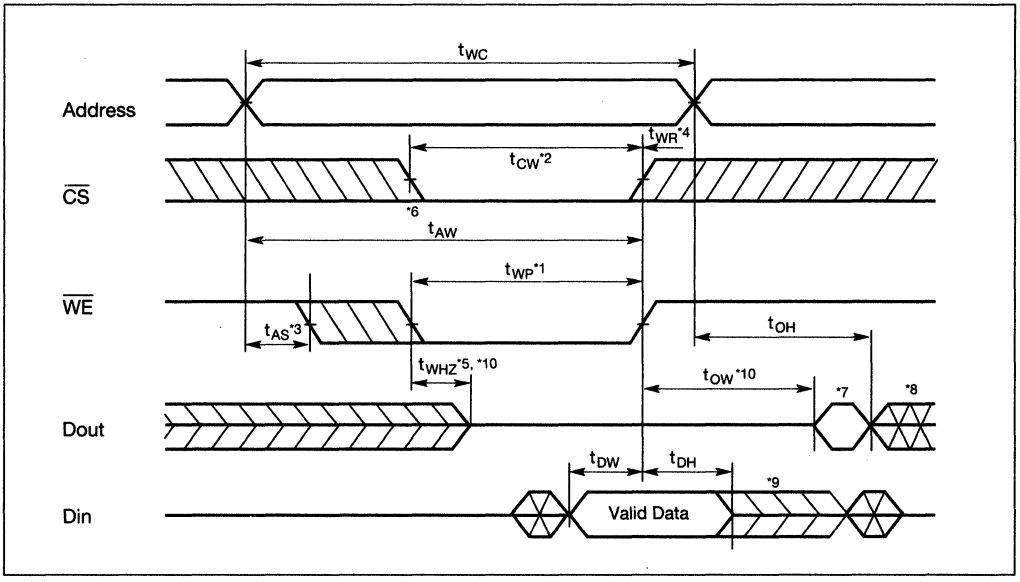
Parameter	Symbol	HM62W256-7 Min	HM62W256-7 Max	HM62W256-8 Min	HM62W256-8 Max	Unit	Notes
Write Cycle Time	t_{WC}	70	—	85	—	ns	
Chip Selection to End of Write	t_{CW}	60	—	75	—	ns	2
Address Setup Time	t_{AS}	0	—	0	—	ns	3
Address Valid to End of Write	t_{AW}	80	—	75	—	ns	
Write Pulse Width	t_{WP}	50	—	55	—	ns	1
Write Recovery Time	t_{WR}	0	—	0	—	ns	4
Write to Output in High-Z	t_{WHZ}	0	25	0	30	ns	10, 11
Data to Write Time Overlap	t_{DW}	30	—	40	—	ns	
Data Hold From Write Time	t_{DH}	0	—	0	—	ns	
Output Active From End of Write	t_{OW}	10	—	10	—	ns	10
Output Disable to Output in High-Z	t_{OHZ}	0	25	0	30	ns	10, 11

Write Timing Waveform (1) ($\overline{OE}$ Clock)



5

Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)*2

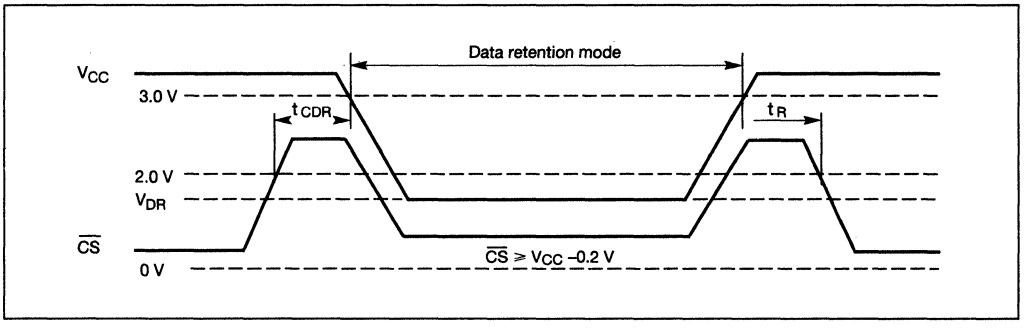


Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
7. D_{out} is the same phase of the write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the output must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not refered to output voltage levels.
12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, t_{WP} min = t_{WHZ} max + t_{DW} min.

Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	3.6	V	$\overline{CS} \geq V_{CC}$ –0.2 V, $V_{in} \geq 0$ V
Data Retention Current	I_{CCDR}	—	—	T.B.D.	µA	V_{CC} = T.B.D., $V_{in} \geq 0$ V $\overline{CS} \geq V_{CC}$ –0.2 V
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation Recovery Time	t_R	t_{RC}*1	—	—	ns	See Retention Waveform

Low V_{CC} Data Retention Timing Waveform



Notes: 1. t_{RC} = read cycle time.
2. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and D_{in} buffer. If $\overline{CS}$ controls data retention mode, other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

5

HM62W8128 Series — Product Preview

131072-Word × 8-Bit High Speed CMOS Static RAM

Description

The Hitachi HM62W8128 is a CMOS static RAM organized 128 kword × 8 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

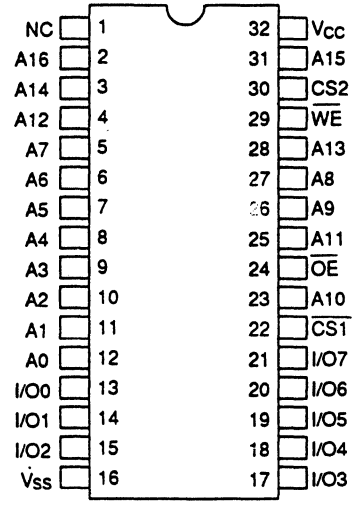
- High Speed
  Fast access time: 100/120 ns (max)
- Low power
  Active: 23 mW (typ)
  Standby: 4 μW (typ) (L-/L-L/L-SL version)
- Single 3.3 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- All inputs and outputs CMOS compatible.
- Capability of battery back up operation (L-/L-L/L-SL version)
  2 chip selection for battery back up

Ordering Information

Type No.	Access time	Package
HM62W8128LP-10	100 ns	600-mil 32-pin plastic DIP (DP-32)
HM62W8128LP-12	120 ns	
HM62W8128LP-10L	100 ns	
HM62W8128LP-12L	120 ns	
HM62W8128LP-10SL	100 ns	
HM62W8128LP-12SL	120 ns	
HM62W8128LFP-10	100 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62W8128LFP-12	120 ns	
HM62W8128LFP-10L	100 ns	
HM62W8128LFP-12L	120 ns	
HM62W8128LFP-10SL	100 ns	
HM62W8128LFP-12SL	120 ns	
HM62W8128LT-10	100 ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
HM62W8128LT-12	120 ns	
HM62W8128LT-10L	100 ns	
HM62W8128LT-12L	120 ns	
HM62W8128LR-10	100 ns	8mm × 20mm 32-pin TSOP (reverse type) (TFP-32DR)
HM62W8128LR-12	120 ns	
HM62W8128LR-10L	100 ns	
HM62W8128LR-12L	120 ns	

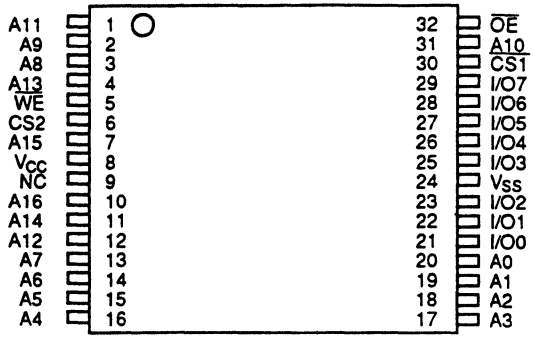
Pin Arrangement

HM62W8128P/FP Series



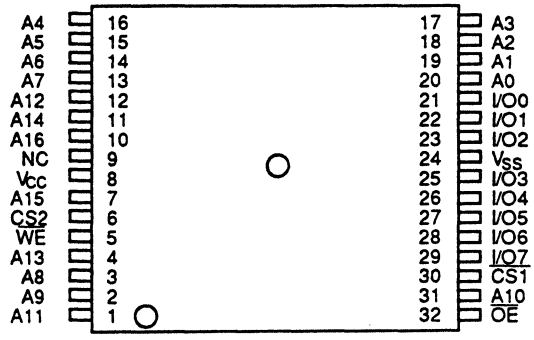
(Top View)

HM62W8128T Series



(Top View)

HM62W8128R Series



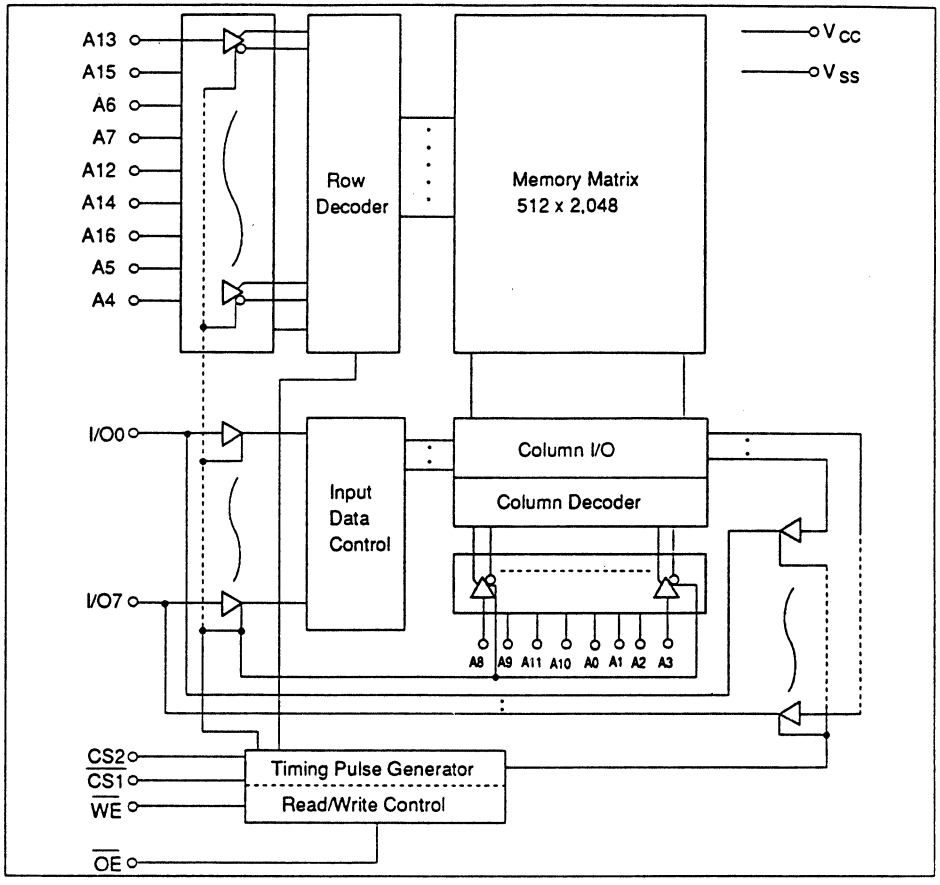
(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

5

Block Diagram



Function Table

$\overline{CS}_1$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to + 5.5	V
Voltave on any pin relative to V_{SS}	V_T	−0.5*1 to V_{CC}+0.3	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	−55 to + 125	°C
Storage tremperature under bias	Tbias	−10 to 85	°C

Notes: 1. −1.2 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	−0.3*1	—	0.4	V

Note: 1. −1.2 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC}	—	6	10	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
Operating power supply current	I_{CC1}	—	20	25	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
	I_{CC2}	—	7	10	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} - 0.2 V, V_{IH} ≥ V_{CC} - 0.2 V, V_{IL} ≤ 0.2 V	
Standby power supply current: DC	I_{SB}	—	0.5	2	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}	
Standby power supply current (1): DC	I_{SB1}	—	0.01	1	mA	0 V ≤ Vin ≤ V_{CC}, $\overline{CS1}$ ≥ V_{CC} - 0.2 V, CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V	
		—	1.2	70	µA		L-version
		—	1.2	50	µA		L-L version
		—	1.2	30	µA		L-SL version
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA	
	V_{OH}	2.9	—	—	V	I_{OH} = −100 µA	

Note: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and C_L (50 pF)
  (Including scope & jig)

Read Cycle

		HM62W8128–10		HM62W8128–12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
Chip selection to output valid	t_{CO1}	—	100	—	120	ns	
	t_{CO2}	—	100	—	120	ns	
Output enable to output valid	t_{OE}	—	80	—	100	ns	
Chip selection to output in low-Z	t_{LZ1}	15	—	15	—	ns	1, 2, 3
	t_{LZ2}	15	—	15	—	ns	1, 2, 3
Output enable to output in low-Z	t_{OLZ}	10	—	10	—	ns	1, 2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	40	0	50	ns	1, 2, 3
	t_{HZ2}	0	40	0	50	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	40	0	50	ns	1, 2, 3
Output hold from address change	t_{OH}	15	—	15	—	ns	1, 2, 3

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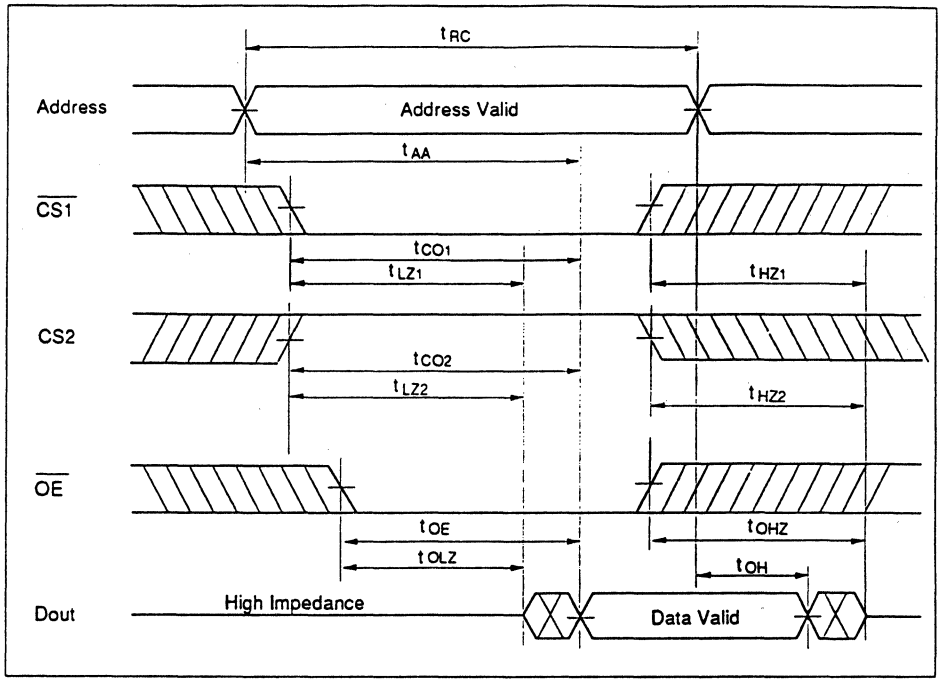
Read Timing Waveform *4



Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for read cycle.

Write Cycle

Parameter	Symbol	HM62W8128-10 Min	HM62W8128-10 Max	HM62W8128-12 Min	HM62W8128-12 Max	Unit	Notes
Write cycle time	t_{WC}	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	90	—	110	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address valid to end of write	t_{AW}	90	—	110	—	ns	
Write pulse width	t_{WP}	80	—	100	—	ns	
Write recovery time	t_{WR}	0	—	0	—	ns	
		0	—	0	—	ns	11
Write to output in high-Z	t_{WHZ}	0	40	0	50	ns	10
Data to write time overlap	t_{DW}	50	—	60	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	10	—	10	—	ns	10

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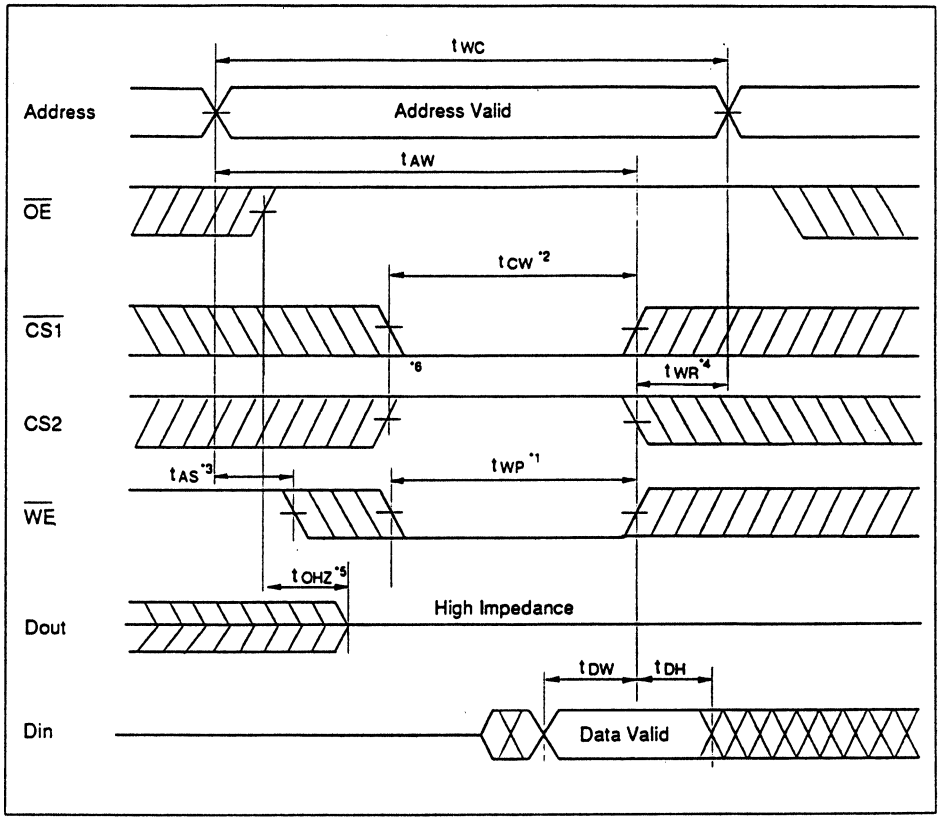
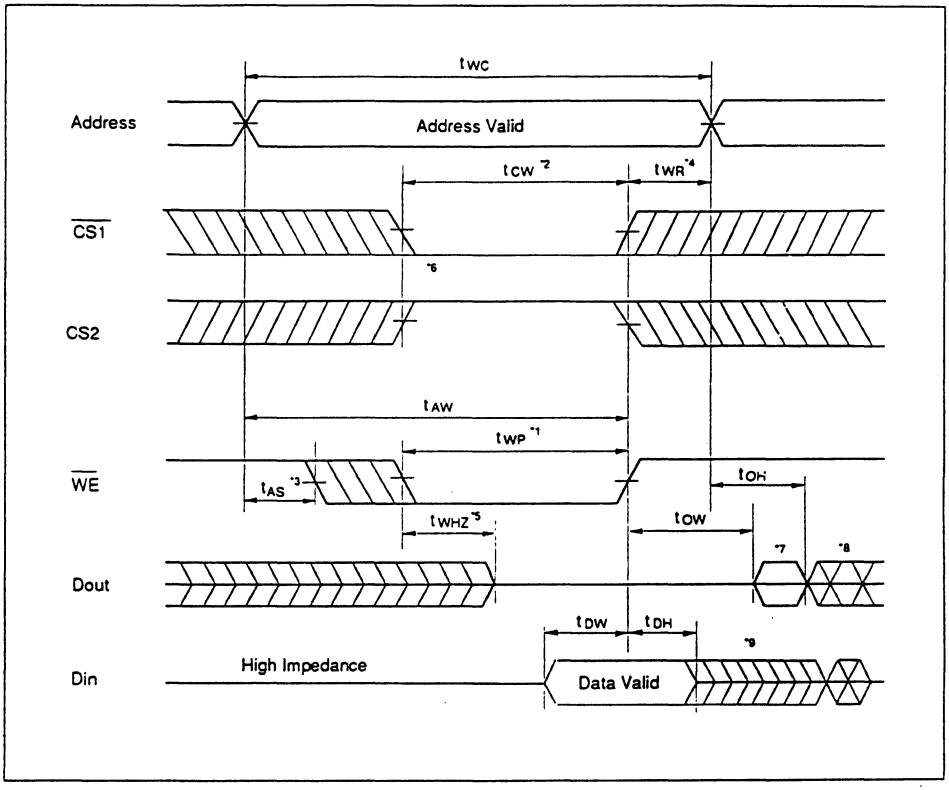
Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



Notes:
1. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. This value is measured from CS2 going low to the end of write cycle.

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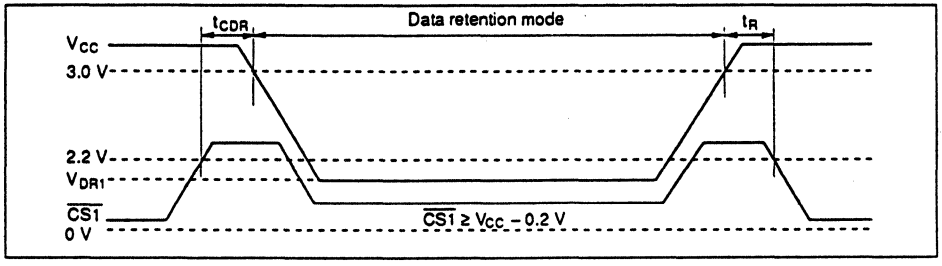
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

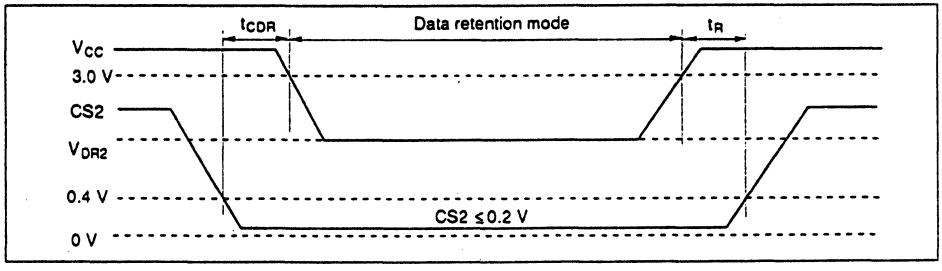
This characteristics is guaranteed only for L-, L-L, and L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or 0 V ≤ CS2 ≤ 0.2 V, Vin ≥ 0 V	
Data retention current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3.0 V, Vin ≥ 0V, $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or 0 V ≤ CS2 ≤ 0.2 V	Lversion
		—	1	30*2	µA		L-Lversion
		—	1	15*3	µA		L-SLversion
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform	
Operation recovery time	t_R	5	—	—	ms		

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: 1. 20 µA max at Ta = 0 to 40°C (Lversion).
2. 6 µA max at Ta = 0 to 40°C (L-Lversion).
3. 3 µA max at Ta = 0 to 40°C (L-SLversion).
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} − 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM62V8128 Series — Product Preview

131072-Word × 8-Bit High Speed CMOS Static RAM

Description

The Hitachi HM62V8128 is a CMOS static RAM organized 128 kword × 8 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- High Speed
  Fast access time: 120/150 ns (max)
- Low power
  Active: 18 mW (typ)
  Standby: 3 μW (typ) (L-/L-L/L-SL version)
- Single 3 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- All inputs and outputs CMOS compatible.
- Capability of battery back up operation (L-/L-L/L-SL version)
  2 chip selection for battery back up

Ordering Information

Type No.	Access time	Package
HM62V8128P-12	120 ns	600-mil 32-pin plastic DIP (DP-32)
HM62V8128P-15	150 ns	
HM62V8128LP-12	120 ns	
HM62V8128LP-15	150 ns	
HM62V8128LP-12SL	120 ns	
HM62V8128LP-15SL	150 ns	
HM62V8128FP-12	120 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8128FP-15	150 ns	
HM62V8128LFP-12	120 ns	
HM62V8128LFP-15	150 ns	
HM62V8128LFP-12SL	120 ns	
HM62V8128LFP-15SL	150 ns	
HM62V8128T-12	120 ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
HM62V8128T-15	150 ns	
HM62V8128LT-12	120 ns	
HM62V8128LT-15	150 ns	
HM62V8128LT-12L	120 ns	
HM62V8128LT-15L	150 ns	

Note: Product Preview: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

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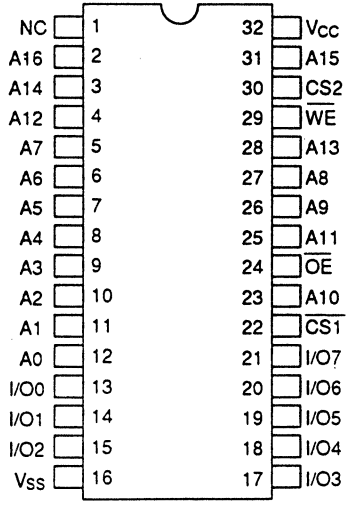
Ordering Information (cont)

Type No.	Access time	Package
HM62V8128R–12	120ns	
HM62V8128R–15	150ns	
HM62V8128LR–12	120 ns	8mm X 20mm 32-pin TSOP (reverse type) (TFP-32DR)
HM62V8128LR–15	150 ns	
HM62V8128LR–12L	120 ns	
HM62V8128LR–15L	150 ns	

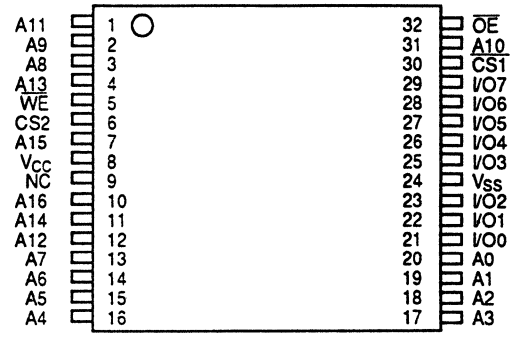
Pin Arrangement

HM62V8128P/FP Series



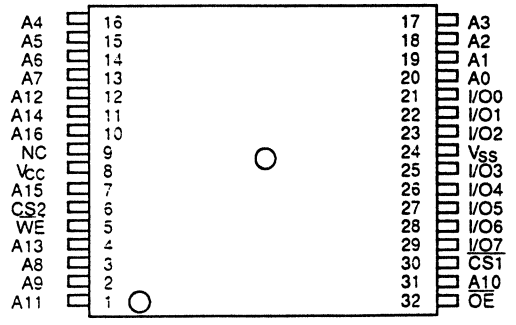
(Top View)

HM62V8128T Series



(Top View)

HM62V8128R Series

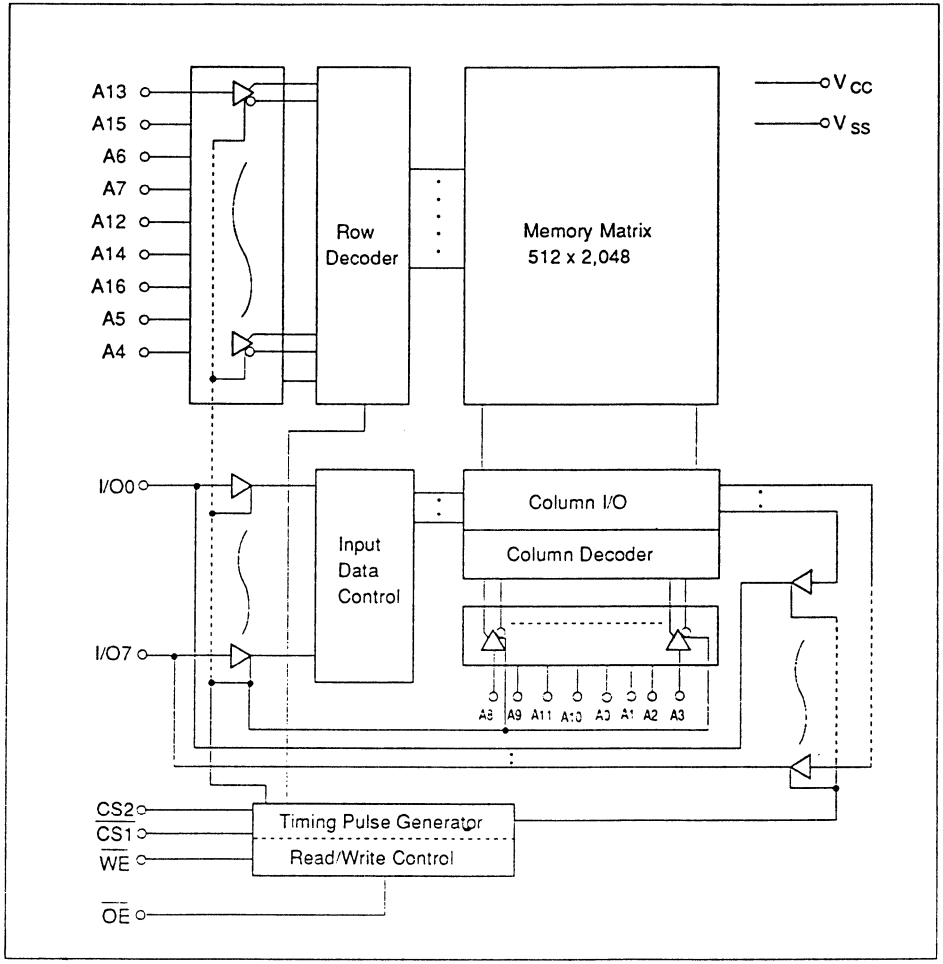


(Top View)

Pin Description

Pin name	Function	Pin name	Function
A0 – A16	Address	$\overline{WE}$	Write enable
I/O0 – I/O7	Input/output	$\overline{OE}$	Output enable
$\overline{CS1}$	Chip select 1	NC	No connection
CS2	Chip select 2	V_{CC}	Power supply
		V_{SS}	Ground

Block Diagram



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Function Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to + 5.5	V
Voltave on any pin relative to V_{SS}	V_T	−0.5*1 to V_{CC}+0.3	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	−55 to + 125	°C
Storage tremperature under bias	Tbias	−10 to 85	°C

Notes: 1. −1.2 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.3	—	V_{CC}+0.3	V
	V_{IL}	−0.3 *1	—	0.4	V

Note: 1. −1.2 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC}	—	5	10	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
Operating power supply current	I_{CC1}	—	15	20	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
	I_{CC2}	—	6	10	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} - 0.2 V, V_{IH} ≥ V_{CC} - 0.2 V, V_{IL} ≤ 0.2 V	
Standby power supply current: DC	I_{SB}	—	0.5	2	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}	
Standby power supply current (1): DC	I_{SB1}	—	0.01	1	mA	0 V ≤ Vin ≤ V_{CC}, $\overline{CS1}$ ≥ V_{CC} - 0.2 V, CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V	
		—	1	60	µA		L-version
		—	1	40	µA		L-L version
		—	1	20	µA		L-SL version
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA	
	V_{OH}	2.6	—	—	V	I_{OH} = –100 µA	

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

5

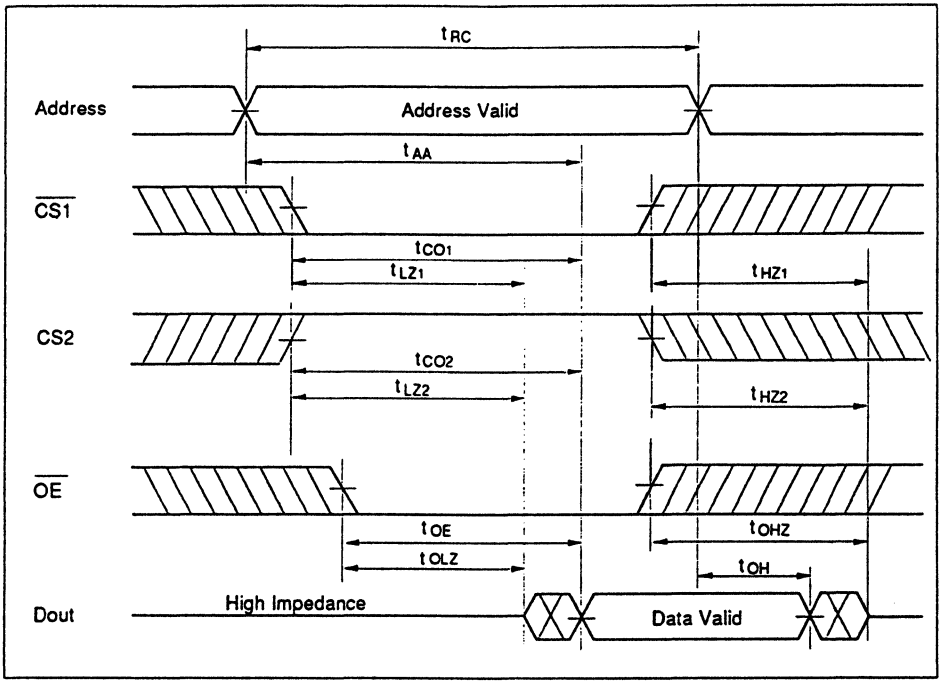
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%, unless otherwise noted.)

Test Conditions
- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load:
  HM62V8128-12 1 TTL Gate and C_L (50 pF)
  HM62V8128-15 1 TTL Gate and C_L (100 pF)
  (Including scope & jig)

Read Cycle

		HM62V8128–12		HM62V8128–15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
Chip selection to output valid	t_{CO1}	—	120	—	150	ns	
	t_{CO2}	—	120	—	150	ns	
Output enable to output valid	t_{OE}	—	90	—	100	ns	
Chip selection to output in low-Z	t_{LZ1}	15	—	20	—	ns	1, 2, 3
	t_{LZ2}	15	—	20	—	ns	1, 2, 3
Output enable to output in low-Z	t_{OLZ}	10	—	10	—	ns	1, 2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	50	0	60	ns	1, 2, 3
	t_{HZ2}	0	50	0	60	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	50	0	60	ns	1, 2, 3
Output hold from address change	t_{OH}	15	—	20	—	ns	1, 2, 3

Read Timing Waveform *4



Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for read cycle.

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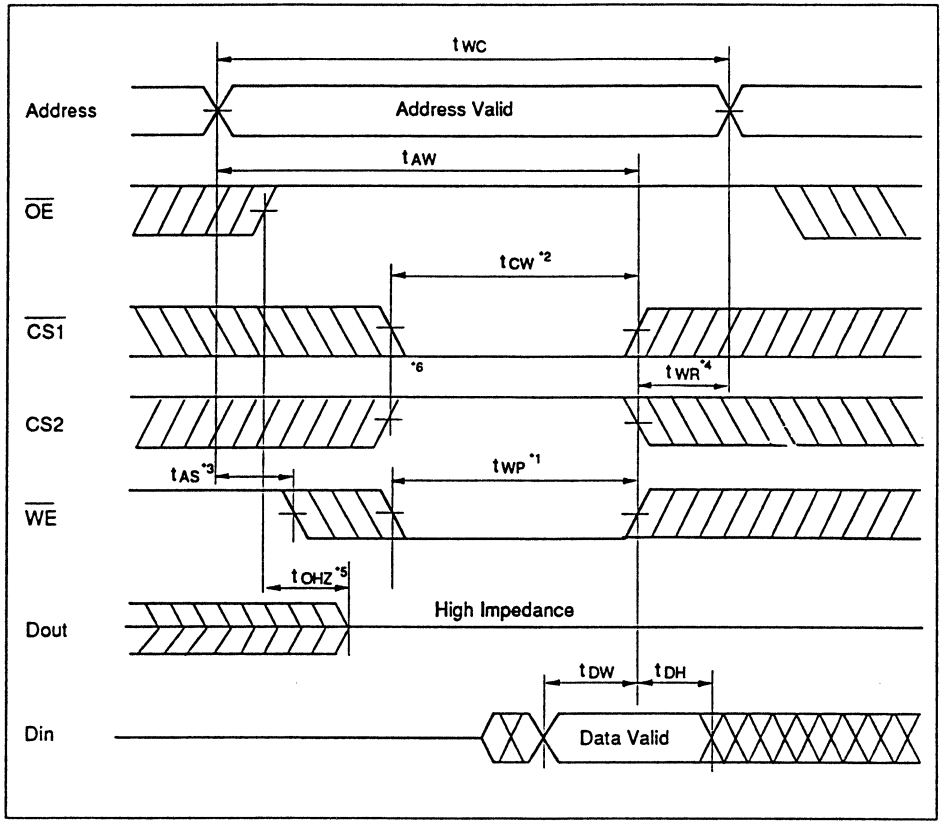
Write Cycle

Parameter	Symbol	HM62V8128-12 Min	HM62V8128-12 Max	HM62V8128-15 Min	HM62V8128-15 Max	Unit	Notes
Write cycle time	t_{WC}	120	—	150	—	ns	
Chip selection to end of write	t_{CW}	110	—	140	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address valid to end of write	t_{AW}	110	—	140	—	ns	
Write pulse width	t_{WP}	100	—	130	—	ns	
Write recovery time	t_{WR}	0	—	0	—	ns	
		0	—	0	—	ns	11
Write to output in high-Z	t_{WHZ}	0	50	0	60	ns	10
Data to write time overlap	t_{DW}	60	—	80	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	15	—	20	—	ns	10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



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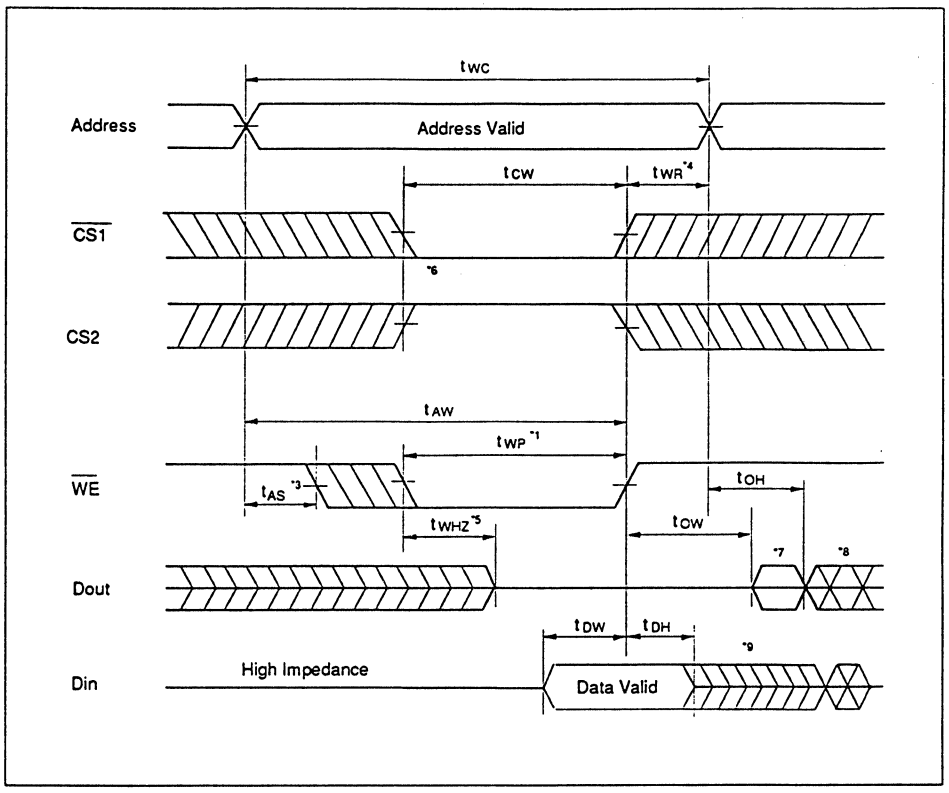
Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



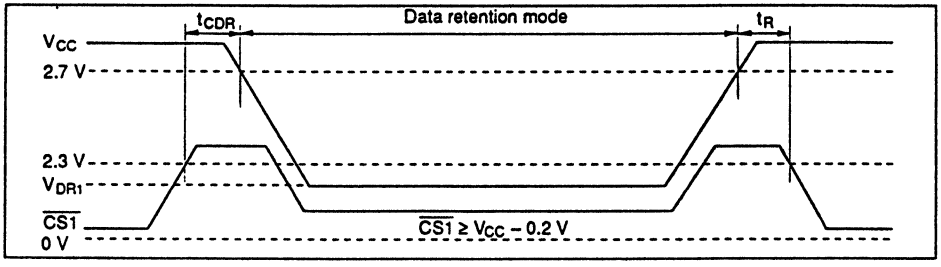
Notes:
1. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. This value is measured from CS2 going low to the end of write cycle.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

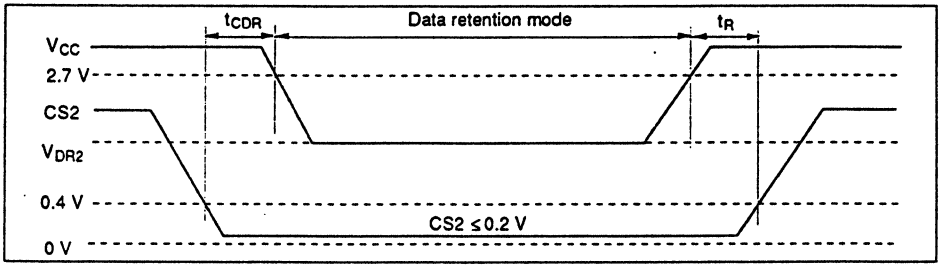
This characteristics is guaranteed only for L-, L-L, and L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or 0 V ≤ CS2 ≤ 0.2 V, Vin ≥ 0 V	
Data retention current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3.0 V, Vin ≥ 0V, $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or 0 V ≤ CS2 ≤ 0.2 V	Lversion
		—	1	30*2	µA		L-Lversion
		—	1	15*3	µA		L-SLversion
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform	
Operation recovery time	t_R	5	—	—	ms		

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: 1. 20 µA max at Ta = 0 to 40°C (Lversion).
2. 6 µA max at Ta = 0 to 40°C (L-Lversion).
3. 3 µA max at Ta = 0 to 40°C (L-SLversion).
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} − 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

5

HM62W9128 Series — Preliminary

131072-Word × 9-Bit High Speed CMOS Static RAM

Description

The Hitachi HM62W9128 is a CMOS static RAM organized 128 kword × 9 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards.

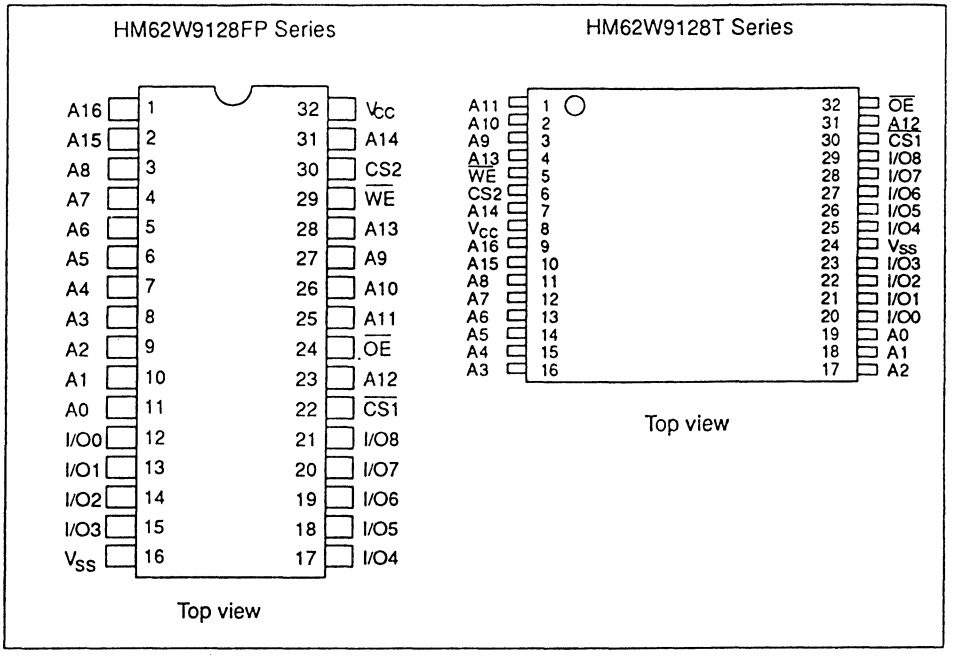
Features

- High Speed
  Fast access time: 100 ns/120 ns (max)
- Low power
  Active: 33 mW (typ)
  Standby: 4 μW (typ) (L-/L-L/L-SL version)
- Single 3.3 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- All inputs and outputs CMOS compatible.
- Capability of battery back up operation
  (L-/L-L/L-SL version)
  2 chip selection for battery back up

Ordering Information

Type No.	Access time	Package
HM62W9128LFP-10	100 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62W9128LFP-12	120 ns	
HM62W9128LFP-10L	100 ns	
HM62W9128LFP-12L	120 ns	
HM62W9128LFP-10SL	100 ns	
HM62W9128LFP-12SL	120 ns	
HM62W9128LT-10	100 ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
HM62W9128LT-12	120 ns	
HM62W9128LT-10L	100 ns	
HM62W9128LT-12L	120 ns	
HM62W9128LT-10SL	100 ns	
HM62W9128LT-12SL	120 ns	

Pin Arrangement



Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O8	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

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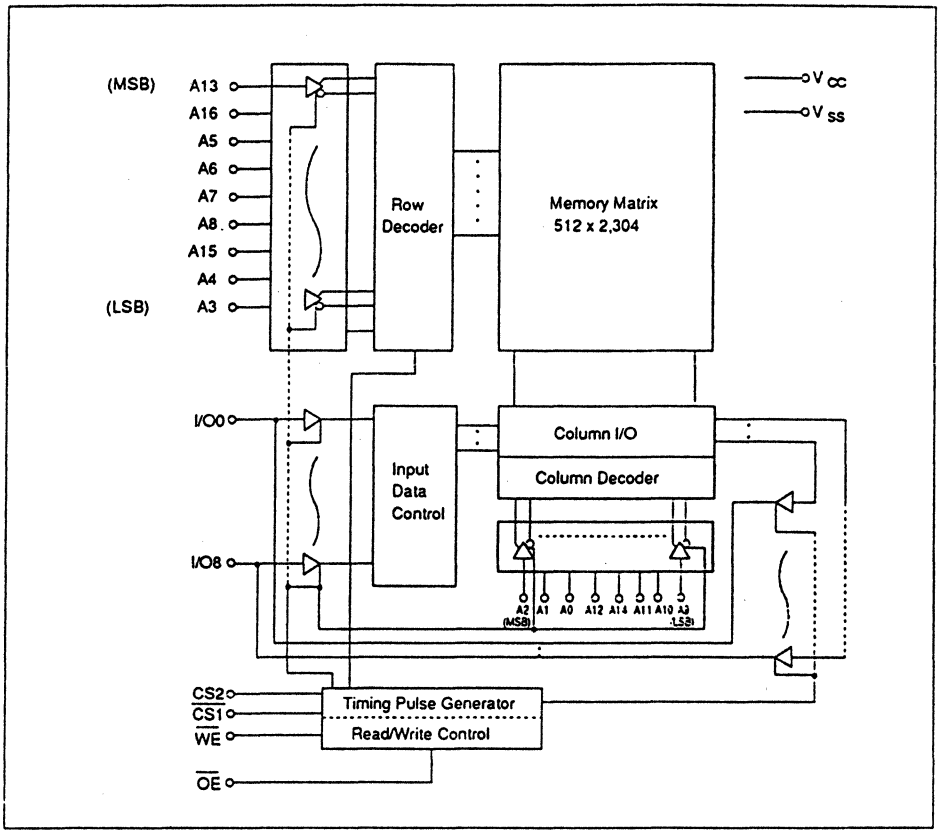
Block Diagram



Function Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to + 5.5	V
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to V_{CC}+0.3 *2	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	−55 to + 125	°C
Storage temperature under bias	Tbias	−10 to 85	°C

Notes: 1. −1.2 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 5.5V.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	−0.3 *1	—	0.4	V

Note: 1. −1.2 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC}	—	6	10	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
Operating power supply current	I_{CC1}	—	20	30	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
	I_{CC2}	—	10	15	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} − 0.2 V, V_{IH} ≥ V_{CC} − 0.2 V, V_{IL} ≤ 0.2 V	
Standby power supply current: DC	I_{SB}	—	0.5	2	mA	(1) $\overline{CS1}$ = V_{IH}, CS2 = V_{IH} (2) CS2 = V_{IL}	
Standby power supply current (1): DC	I_{SB1}	—	1.2	80	µA	(1) 0 V ≤ Vin ≤ V_{CC}, $\overline{CS1}$ ≥ V_{CC} − 0.2 V, CS2 ≥ V_{CC} − 0.2 V (2) 0 V ≤ Vin ≤ V_{CC}, $\overline{CS1}$ ≥ V_{CC} − 0.2 V, 0 V ≤ CS2 ≤ 0.2 V (3) 0 V ≤ Vin ≤ V_{CC}, 0 V ≤ CS2 ≤ 0.2 V	L-version
		—	1.2	60	µA		L-L version
		—	1.2	40	µA		L-SLversion
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA	
	V_{OH}	2.9	—	—	V	I_{OH} = −100 µA	

Note: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions
- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and C_L (50 pF)
  (Including scope & jig)

Read Cycle

		HM62W9128-10		HM62W9128-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
Chip selection to output valid	t_{CO1}	—	100	—	120	ns	
	t_{CO2}	—	100	—	120	ns	
Output enable to output valid	t_{OE}	—	80	—	100	ns	
Chip selection to output in low-Z	t_{LZ1}	15	—	15	—	ns	2
	t_{LZ2}	15	—	15	—	ns	2
Output enable to output in low-Z	t_{OLZ}	10	—	10	—	ns	2
Chip deselection to output in high-Z	t_{HZ1}	0	40	0	50	ns	1, 2
	t_{HZ2}	0	40	0	50	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	40	0	50	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

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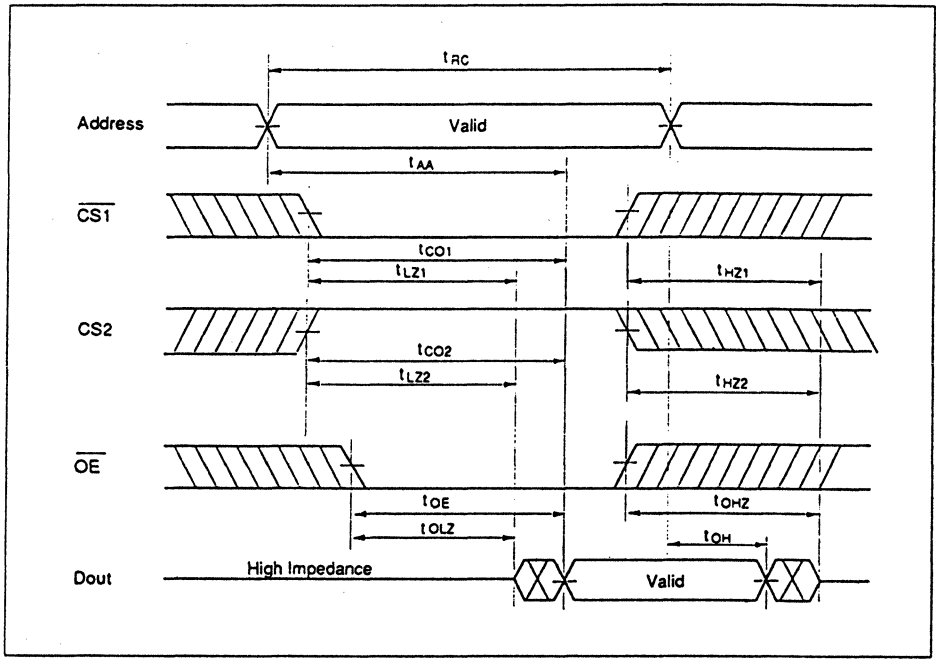
Read Timing Waveform *3

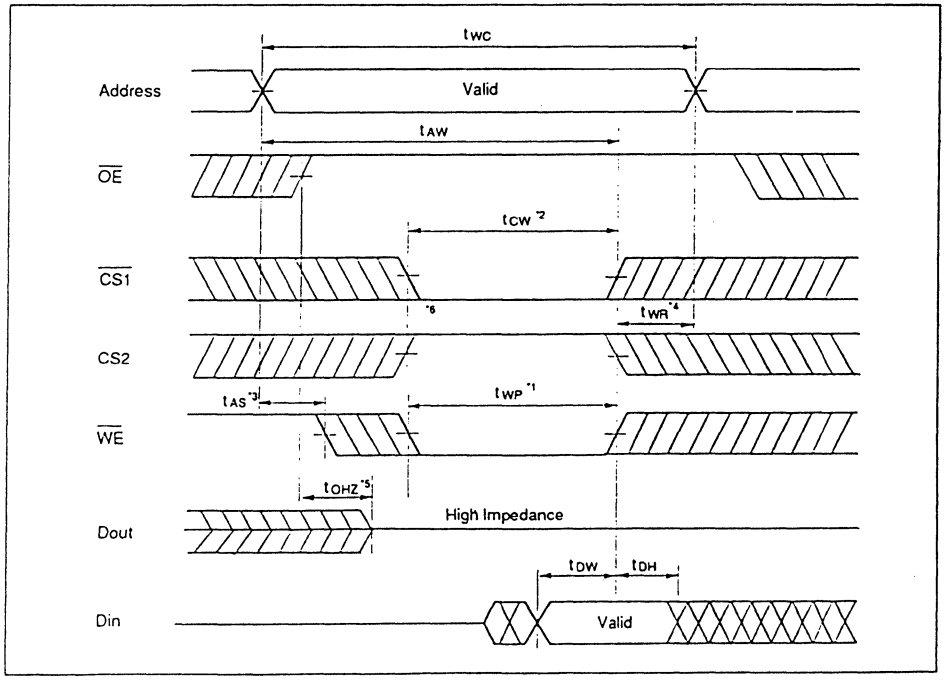


Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.

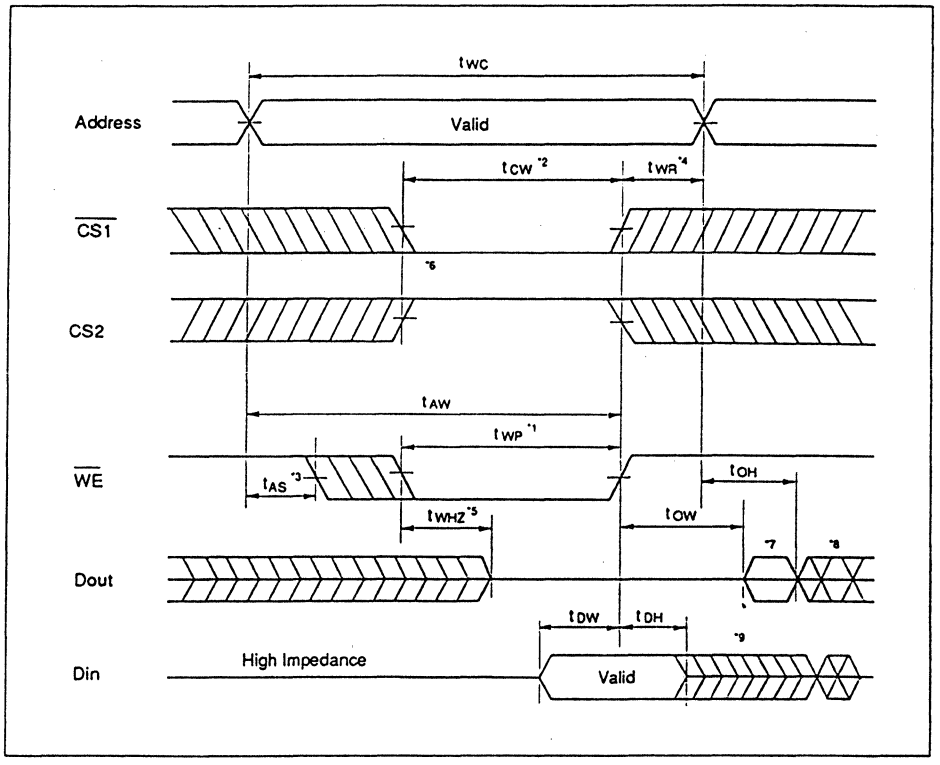
Write Cycle

Parameter	Symbol	HM62W9128-10 Min	HM62W9128-10 Max	HM62W9128-12 Min	HM62W9128-12 Max	Unit	Notes
Write cycle time	t_{WC}	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	90	—	110	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address valid to end of write	t_{AW}	90	—	110	—	ns	
Write pulse width	t_{WP}	80	—	100	—	ns	
Write recovery time	t_{WR}	0	—	0	—	ns	
Write to output in high-Z	t_{WHZ}	0	40	0	50	ns	10
Data to write time overlap	t_{DW}	50	—	60	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	10	—	10	—	ns	10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



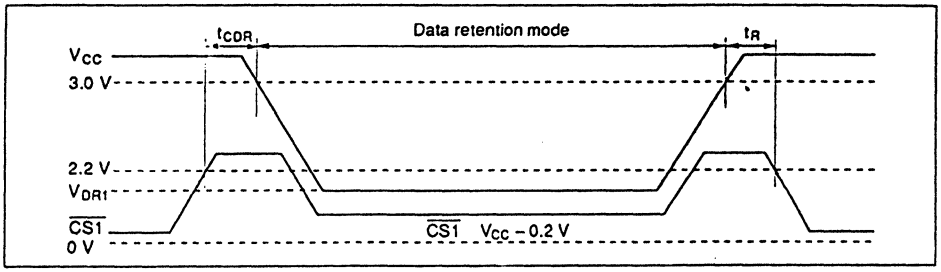
Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
   In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

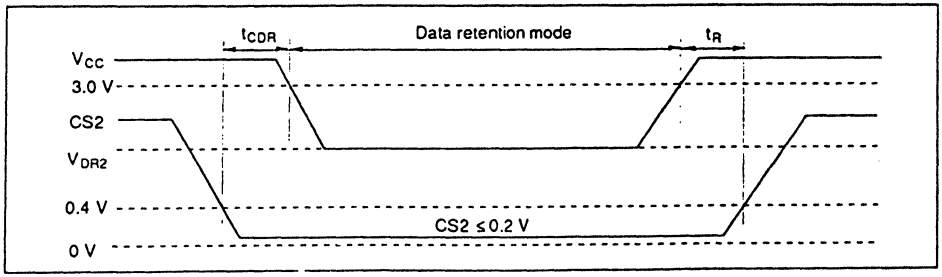
This characteristics is guaranteed only for L-, L-L, and L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	(1) $\overline{CS1} \geq V_{CC} - 0.2$ V, Vin ≥ 0V or (2) 0 V ≤ CS2 ≤ 0.2 V, Vin ≥ 0 V	
Data retention current	I_{CCDR}	—	1	60*1	µA	V_{CC} = 3.0 V, $V_{CC} \geq$ Vin ≥ 0V	Lversion
		—	1	40*2	µA	(1) $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or	L-Lversion
		—	1	20*3	µA	(2) 0 V ≤ CS2 ≤ 0.2 V	L-SLversion
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform	
Operation recovery time	t_R	5	—	—	ms		

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: 1. 25 µA max at Ta = 0 to 40°C (Lversion).
2. 8 µA max at Ta = 0 to 40°C (L-Lversion).
3. 5 µA max at Ta = 0 to 40°C (L-SLversion).
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 > V_{CC} − 0.2 V or 0 V < CS2 < 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

5

131072-Word × 9-Bit High Speed CMOS Static RAM

Description

The Hitachi HM62V9128 is a CMOS static RAM organized 128 kword × 9 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards.

Features

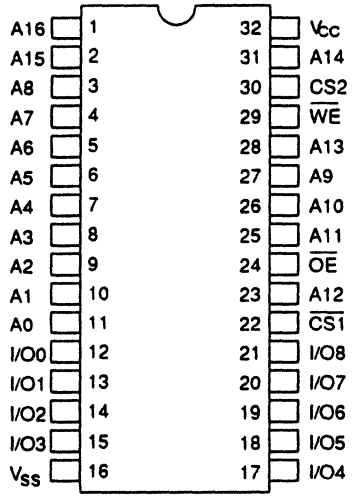
- High Speed
  Fast access time: 150 ns (max)
- Low power
  Active: 30 mW (typ)
  Standby: 3 μW (typ) (L-/L-L/L-SL version)
- Single 3 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- All inputs and outputs CMOS compatible.
- Capability of battery back up operation
  (L-/L-L/L-SL version)
  2 chip selection for battery back up

Ordering Information

Type No.	Access time	Package
HM62V9128LP-15	150 ns	600-mil 32-pin plastic DIP (DP-32)
HM62V9128LP-15L	150 ns	
HM62V9128LP-15SL	150 ns	
HM62V9128LFP-15	150 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V9128LFP-15L	150 ns	
HM62V9128LFP-15SL	150 ns	
HM62V9128LT-15	150 ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
HM62V9128LT-15L	150 ns	
HM62V9128LT-15SL	150 ns	

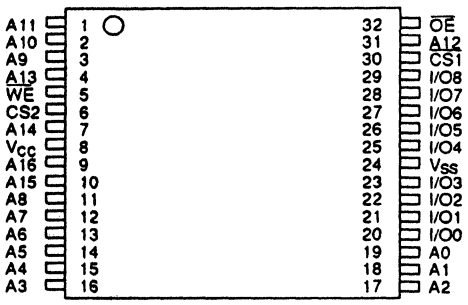
Pin Arrangement

HM62V9128P/FP Series



Top view

HM62V9128T Series



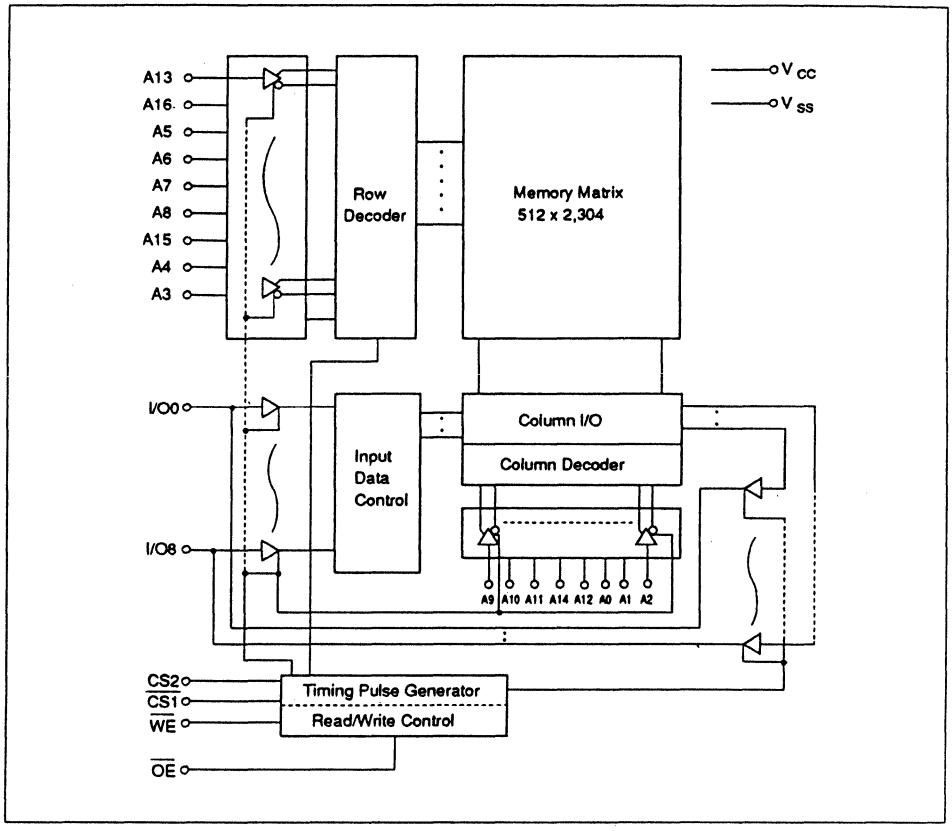
Top view

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O8	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

5

Block Diagram



Function Table

$\overline{CST}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to + 5.5	V
Voltage on any pin relative to V_{SS}	V_T	–0.5[*1] to V_{CC}+0.3	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	–55 to + 125	°C
Storage temperature under bias	Tbias	–10 to 85	°C

Notes: 1. –1.2 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 5.5V.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.3	—	V_{CC}+0.3	V
	V_{IL}	–0.3[*1]	—	0.4	V

Note: 1. –1.2 V for pulse half-width ≤ 30 ns

5

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC} (Read)	—	1	5	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}	
	(Write)	—	5	10	mA	$I_{I/O}$ = 0 mA	
Operating power supply current	I_{CC1}	—	15	30	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
	I_{CC2} (Read)	—	3	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} − 0.2 V, V_{IH} ≥ V_{CC} − 0.2 V, V_{IL} ≤ 0.2 V	
	(Write)	—	10	15	mA		
Standby power supply current: DC	I_{SB}	—	0.5	2	mA	(1) $\overline{CS1}$ = V_{IH}, CS2 = V_{IH} (2) CS2 = V_{IL}	
Standby power supply current (1): DC	I_{SB1}	—	0.01	1	mA	(1) 0 V ≤ Vin ≤ V_{CC}, $\overline{CS1}$ ≥ V_{CC} − 0.2 V,	
		—	1	70	µA	CS2 ≥ V_{CC} − 0.2 V	L-version
		—	1	50	µA	(2) 0 V ≤ Vin ≤ V_{CC} 0 V ≤ CS2 ≤ 0.2 V	L-L version
		—	1	30	µA		L-SLversion
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA	
	V_{OH}	2.6	—	—	V	I_{OH} = −100 µA	

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%, unless otherwise noted.)

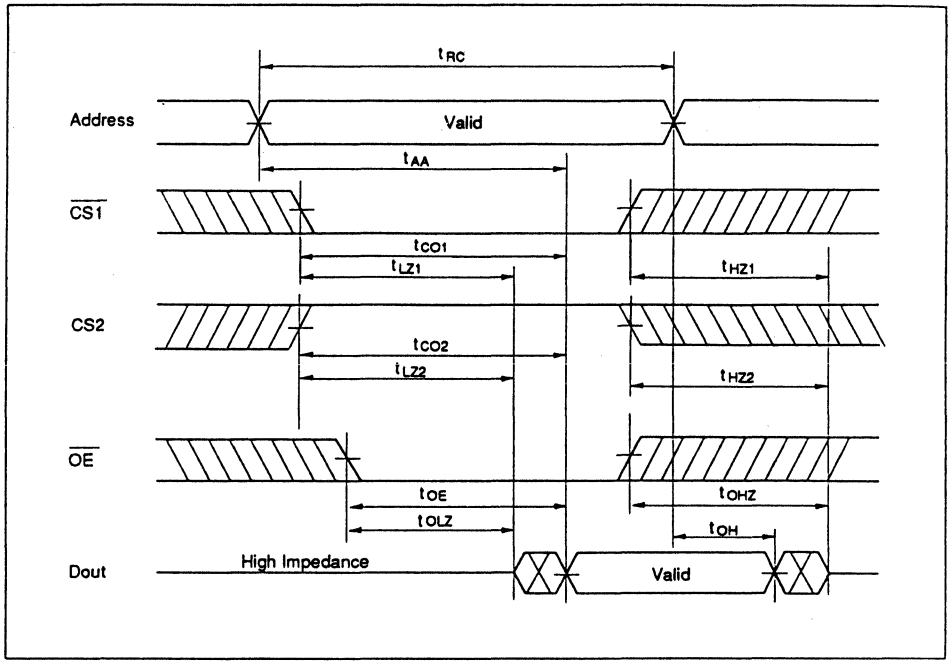
Test Conditions
- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and C_L (100 pF)
  (Including scope & jig)

Read Cycle

		HM62V9128-15			
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t_{RC}	150	—	ns	
Address access time	t_{AA}	—	150	ns	
Chip selection to output valid	t_{CO1}	—	150	ns	
	t_{CO2}	—	150	ns	
Output enable to output valid	t_{OE}	—	100	ns	
Chip selection to output in low-Z	t_{LZ1}	20	—	ns	2
	t_{LZ2}	20	—	ns	2
Output enable to output in low-Z	t_{OLZ}	10	—	ns	2
Chip deselection to output in high-Z	t_{HZ1}	0	60	ns	1, 2
	t_{HZ2}	0	60	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	60	ns	1, 2
Output hold from address change	t_{OH}	20	—	ns	

5

Read Timing Waveform *3



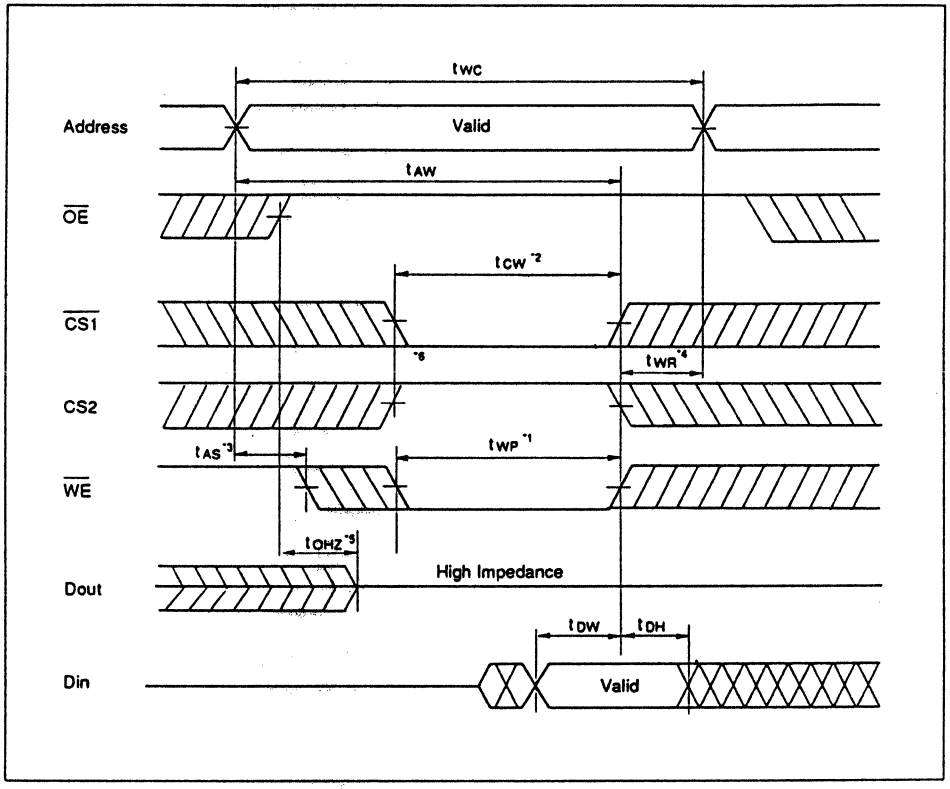
Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.

Write Cycle

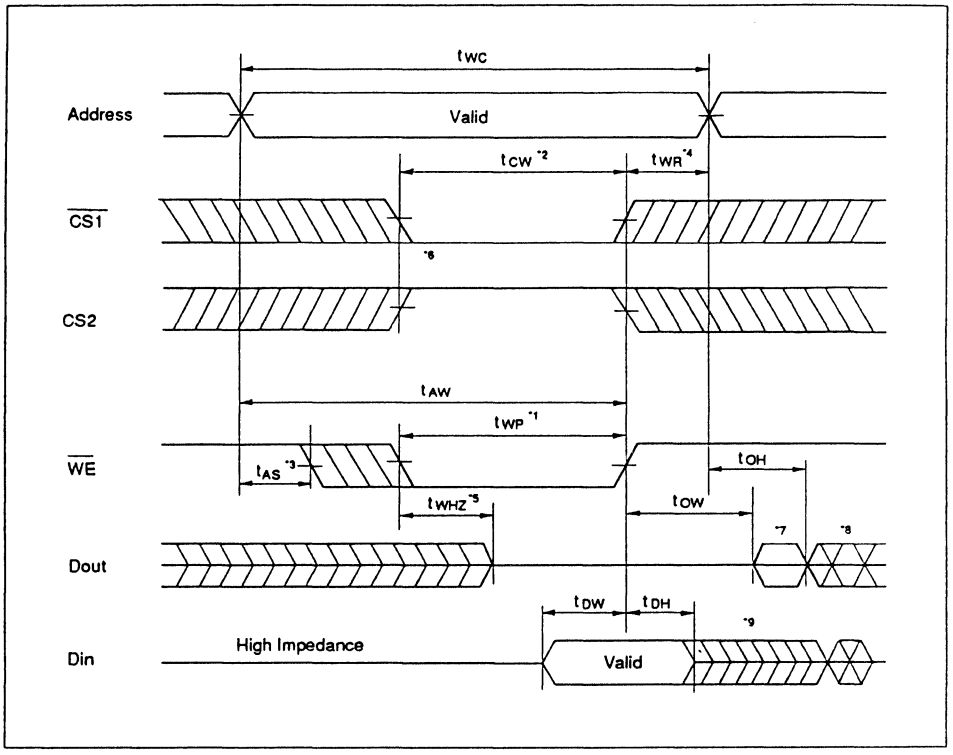
		HM62V9128-15			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	150	—	ns	
Chip selection to end of write	t_{CW}	140	—	ns	
Address setup time	t_{AS}	0	—	ns	
Address valid to end of write	t_{AW}	140	—	ns	
Write pulse width	t_{WP}	130	—	ns	
Write recovery time	t_{WR}	0	—	ns	
		0	—	ns	11
Write to output in high-Z	t_{WHZ}	0	60	ns	10
Data to write time overlap	t_{DW}	80	—	ns	
Write hold from write time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	20	—	ns	10

5

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



Notes:
1. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. This value is measured from CS2 going low to the end of write cycle.

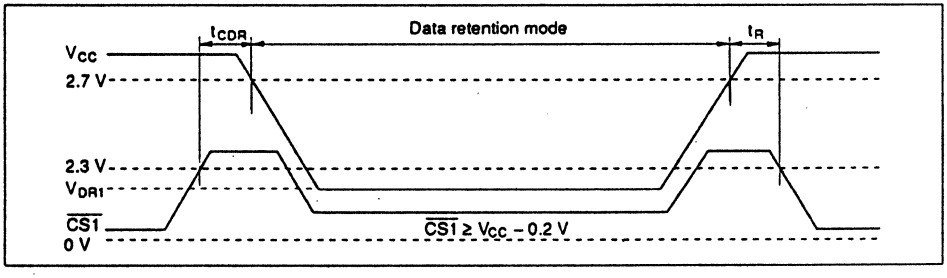
5

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

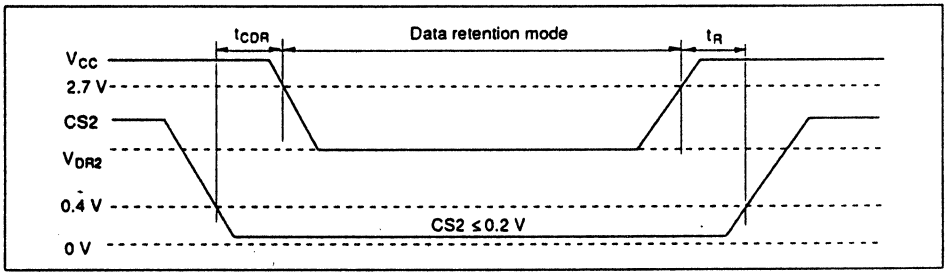
This characteristics is guaranteed only for L-, L-L, and L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
V_{CC} for data retention	V_{DR}	2.0	—	—	V	(1) $\overline{CS1} \geq V_{CC} - 0.2$ V, Vin ≥ 0V or (2) 0 V ≤ CS2 ≤ 0.2 V, Vin ≥ 0 V	
Data retention current	I_{CCDR}	—	1	60*1	µA	V_{CC} = 3.0 V, $V_{CC} \geq$ Vin ≥ 0V	Lversion
		—	1	40*2	µA	(1) $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or	L-Lversion
		—	1	20*3	µA	(2) 0 V ≤ CS2 ≤ 0.2 V	L-SLversion
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform	
Operation recovery time	t_R	5	—	—	ms		

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: 1. 25 µA max at Ta = 0 to 40°C (Lversion).
2. 8 µA max at Ta = 0 to 40°C (L-Lversion).
3. 5 µA max at Ta = 0 to 40°C (L-SLversion).
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 > V_{CC} − 0.2 V or 0 V < CS2 < 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

SECTION 6

PSEUDO STATIC RAMs

- 5.0 V Supply
- 3.0 V & 3.3 V Supply

HM65256B Series

5.0 V Supply

32,768-word × 8-bit High Speed Psuedo Static RAM

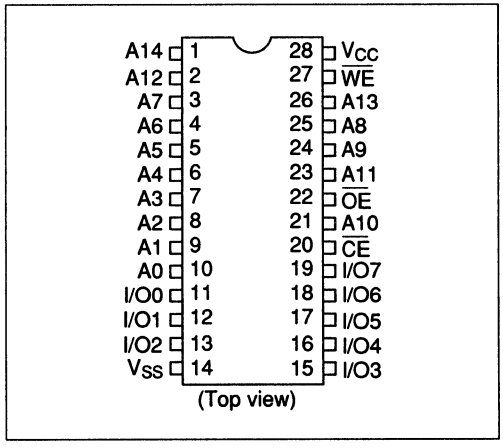
Features

- Single 5 V (±10%)
- Access time
  - — $\overline{CE}$ access time: 100/120/150/200 ns
  - — Address access time: 50/60/75/100 ns (in static column mode)
- Cycle time
  - — Random read/write cycle time: 160/190/235/310 ns
  - — Static column mode cycle time: 55/65/80/105 ns
- Low power: 175 mW typ. active
- All inputs and outputs TTL compatible
- Static column mode capability
- Non-multiplexed address
- 256 refresh cycles (4 ms)
- Refresh functions
  - — Address refresh
  - — Automatic refresh
  - — Self refresh

Ordering Information

Type No.	Access time	Package
HM65256BP-10	100 ns	600-mil 28-pin plastic DIP (DP-28)
HM65256BP-12	120 ns	
HM65256BP-15	150 ns	
HM65256BP-20	200 ns	
HM65256BLP-10	100 ns	
HM65256BLP-12	120 ns	
HM65256BLP-15	150 ns	
HM65256BLP-20	200 ns	
HM65256BSP-10	100 ns	300-mil 28-pin plastic DIP (DP-28N)
HM65256BSP-12	120 ns	
HM65256BSP-15	150 ns	
HM65256BSP-20	200 ns	
HM65256BLSP-10	100 ns	300-mil 28-pin plastic DIP (DP-28N)
HM65256BLSP-12	120 ns	
HM65256BLSP-15	150 ns	
HM65256BLSP-20	200 ns	
HM65256BFP-10T	100 ns	28-pin plastic SOP (FP-28DA)
HM65256BFP-12T	120 ns	
HM65256BFP-15T	150 ns	
HM65256BFP-20T	200 ns	
HM65256BLFP-10T	100 ns	
HM65256BLFP-12T	120 ns	
HM65256BLFP-15T	150 ns	
HM65256BLFP-20T	200 ns	

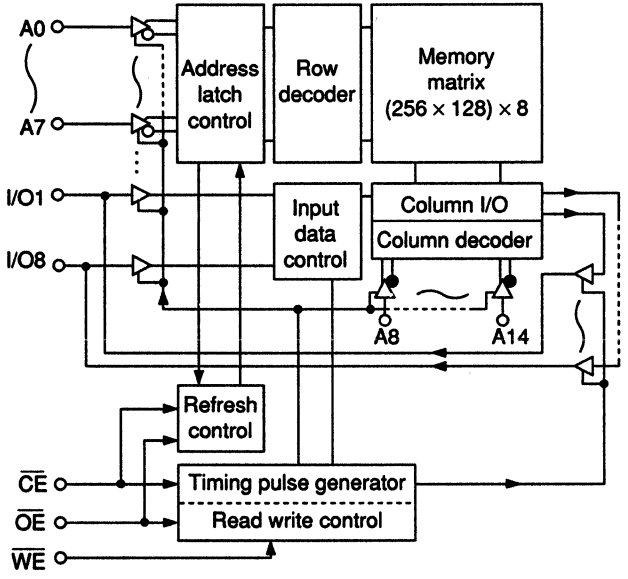
Pin Arrangement



(Top view)

6

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	—
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.5*	—	0.8	V

Note: V_{IL} min = –3.0 V for pulse width ≤ 10 ns.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

		HM65256B			HM65256BL				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Operating power supply current	I_{CC1}	—	35	65	—	35	65	mA	$I_{I/O}$ = 0 mA tcyc = min
Standby power supply current	I_{SB1}	—	1	2	—	1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH} , Vin ≥ 0 v
	I_{SB2}	—	—	—	—	0.05	0.1	mA	$\overline{CE}$ > V_{CC} – 0.2 V, $\overline{OE}$ ≥ V_{CC} – 0.2, Vin ≥ 0
Operating power supply current in self refresh mode	I_{CC2}	—	1	2	—	0.6	1	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	—	—	—	50	100	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, $\overline{OE}$ ≤ 0.2 V, Vin ≥ 0V
Input leakage current	I_{LI}	–10	—	10	–10	—	10	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	–10	—	10	–10	—	10	µA	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –1 mA

Capacitance

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Test conditions**
Input capacitance	Cin	—	5	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	7	pF	$V_{I/O}$ = 0 V

Note: These parameters are sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

AC Test Conditions:

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
- Output load: 1 TTL and 100 pF (including scope and jig)

		HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Random read or write cycle time	t_{RC}	160	—	190	—	235	—	310	—	ns
Static column mode read or write cycle	t_{RSC}	55	—	65	—	80	—	105	—	ns
Chip enable access time	t_{CEA}	—	100	—	120	—	150	—	200	ns
Address access time	t_{AA}	—	50	—	60	—	75	—	100	ns
Output enable access time	t_{OEA}	—	40	—	50	—	60	—	75	ns
Chip disable to output in high Z	t_{CHZ}	—	25	—	25	—	30	—	35	ns
Chip enable to output in low Z	t_{CLZ}	30	—	30	—	35	—	40	—	ns
Output enable to output in low Z	t_{OLZ}	10	—	10	—	10	—	10	—	ns
Output disable to output in high Z	t_{OHZ}	—	25	—	25	—	30	—	35	ns
Chip enable pulse width	t_{CE}	100 ns	4 ms	120 ns	4 ms	150 ns	4 ms	200 ns	4 ms	
Chip enable precharge time	t_P	50	—	60	—	75	—	100	—	ns
Address set-up time	t_{AS}	0	—	0	—	0	—	0	—	ns
Row address hold time	t_{RAH}	20	—	20	—	25	—	30	—	ns
Column address hold time	t_{CAH}	100	—	120	—	150	—	200	—	ns
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns
Output enable hold time	t_{OHC}	0	—	0	—	0	—	0	—	ns
Output enable to chip enable delay time	t_{OCD}	0	—	0	—	0	—	0	—	ns
Output hold time from column address	t_{OH}	5	—	5	—	5	—	10	—	ns
Write command pulse width	t_{WP}	25	—	25	—	30	—	35	—	ns
Chip enable to end of write	t_{CW}	100	—	120	—	150	—	200	—	ns

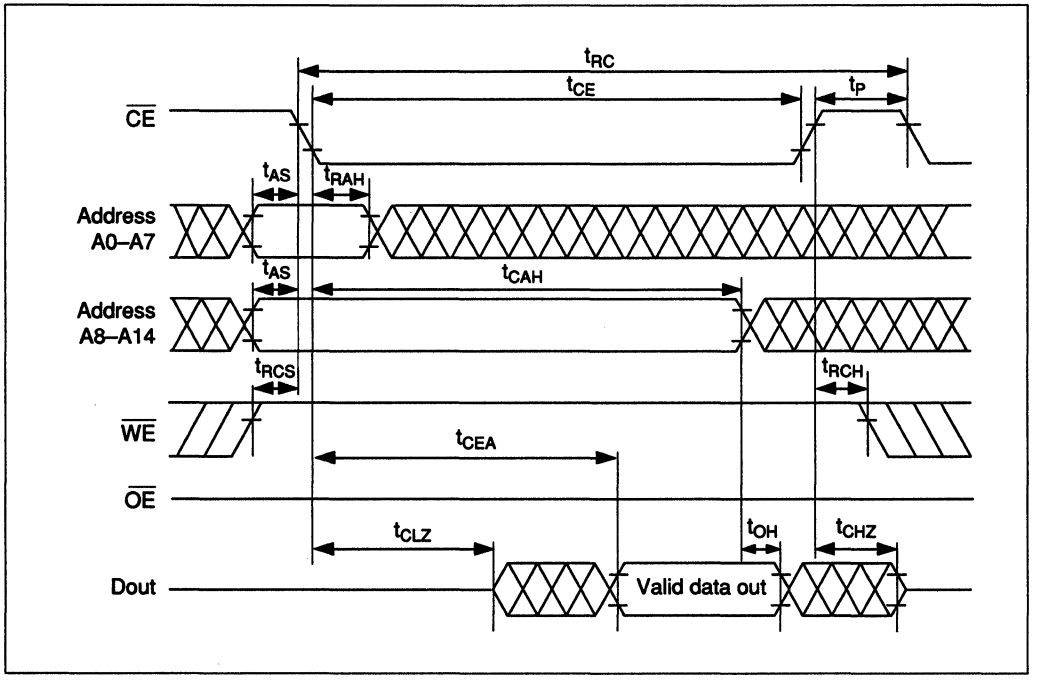
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Parameter	Symbol	HM65256B-10 Min	HM65256B-10 Max	HM65256B-12 Min	HM65256B-12 Max	HM65256B-15 Min	HM65256B-15 Max	HM65256B-20 Min	HM65256B-20 Max	Unit
Column address set-up time	t_{ASW}	0	—	0	—	0	—	0	—	ns
Column address hold time after write	t_{AHW}	0	—	0	—	0	—	0	—	ns
Data valid to end of write	t_{DW}	20	—	20	—	25	—	30	—	ns
Data in hold time for write	t_{DH}	0		0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	5		ns
Write to output in high Z	t_{WHZ}	—	25	—	25	—	30	—	35	ns
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh command delay time	t_{RFD}	50	—	60	—	75	—	100	—	ns
Refresh precharge time	t_{FP}	30	—	30	—	30	—	30	—	ns
Refresh command pulse width for automatic refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic refresh cycle time	t_{FC}	160	—	190	—	235	—	310	—	ns
Refresh command pulse width for self refresh	t_{FAS}	10000	—	10000	—	10000	—	10000	—	ns
Refresh reset time for self refresh	t_{FRS}	160	—	190	—	235	—	310	—	ns
Refresh period	t_{REF}	—	4	—	4	—	4	—	4	ns

Notes:
1. t_{CHZ}, t_{OHZ}, and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T = 5 ns, and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.
4. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
5. If input signals of opposite phase to the outputs are applied in a write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. An initial pause of 100 µs is required after power-up followed by a minimum of 8 initialization cycles.
8. At the end of self refresh, refresh reset time (t_{FRS}) is required to reset the internal self refresh operation of the RAM. During t_{FRS}, $\overline{CE}$ and $\overline{OE}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{OE}$ at the beginning of auto refresh must not occur during t_{FRS} period.

Timing Waveforms

Read Cycle (1) ($\overline{CE}$ controlled)



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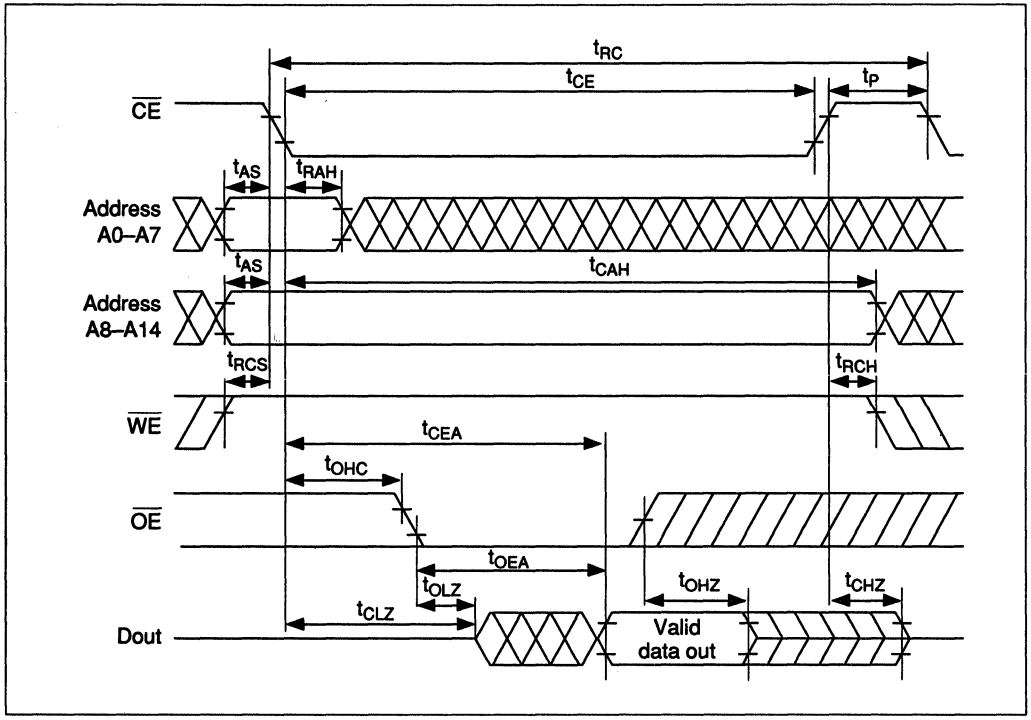
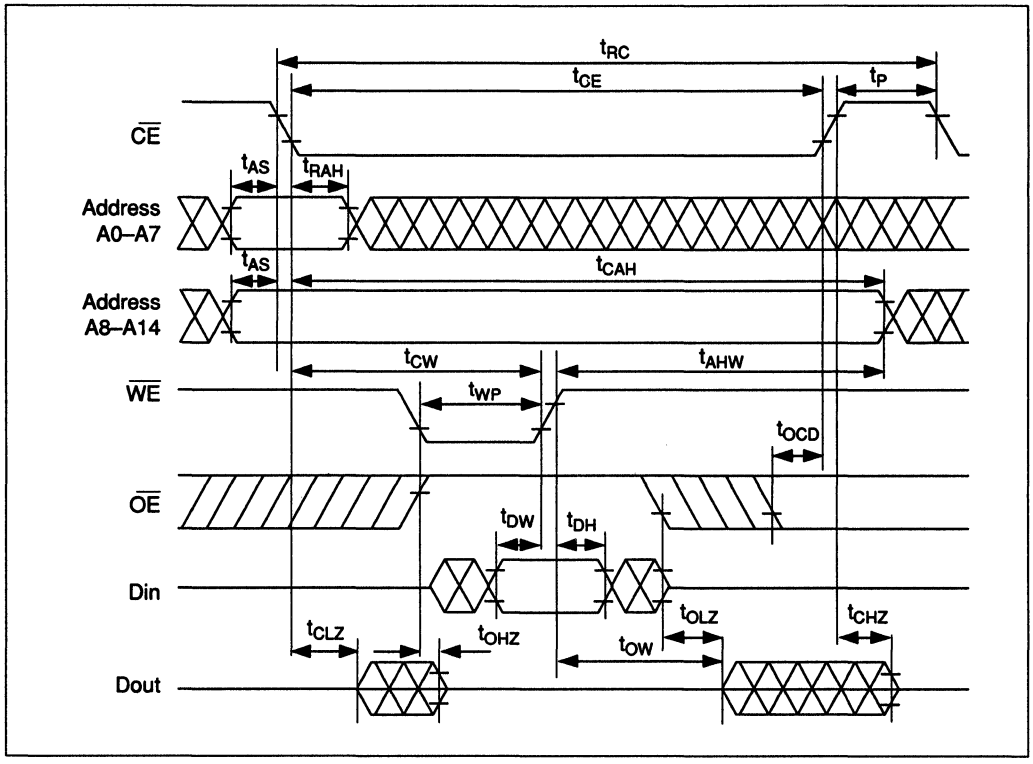
Read Cycle (2) ($\overline{OE}$ controlled)



Write Cycle (1) ($\overline{OE}$ Clock)



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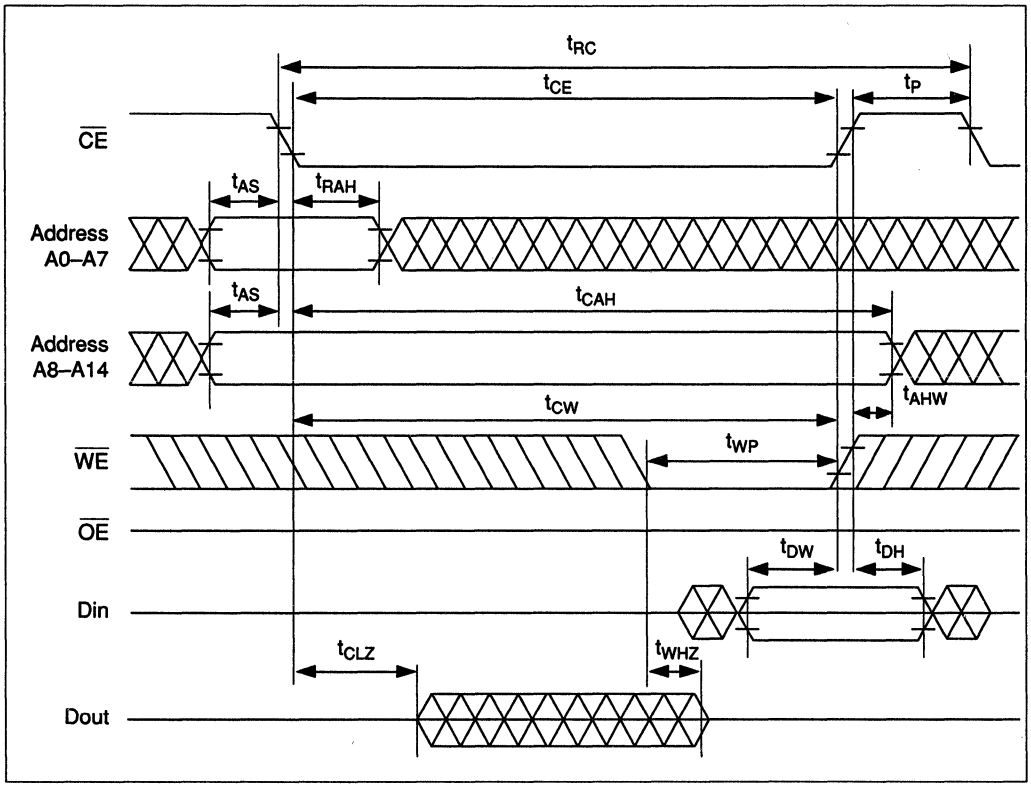
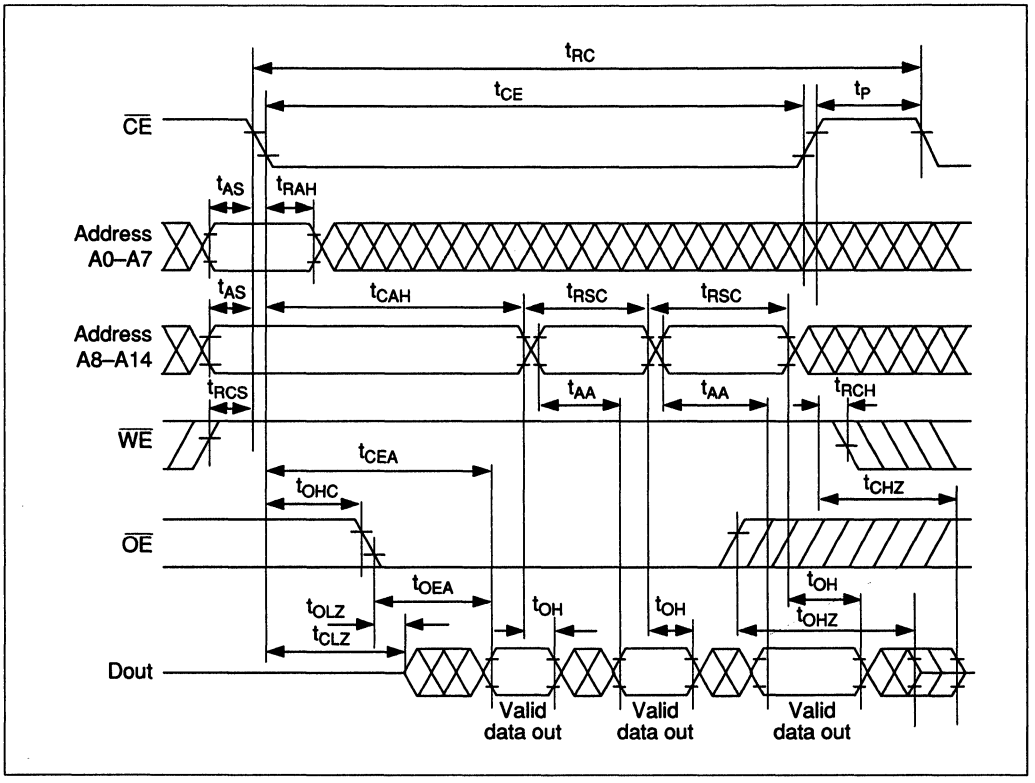
Write Cycle (2) ($\overline{OE}$ fixed low)



Static Column Mode Read Cycle



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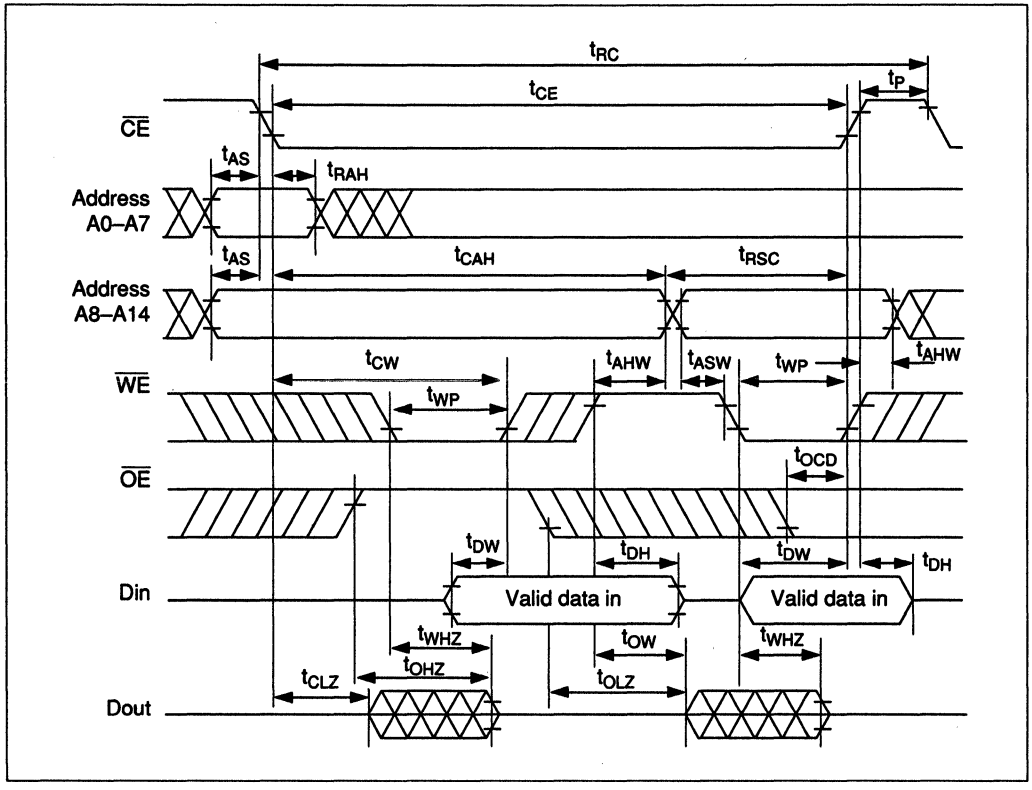
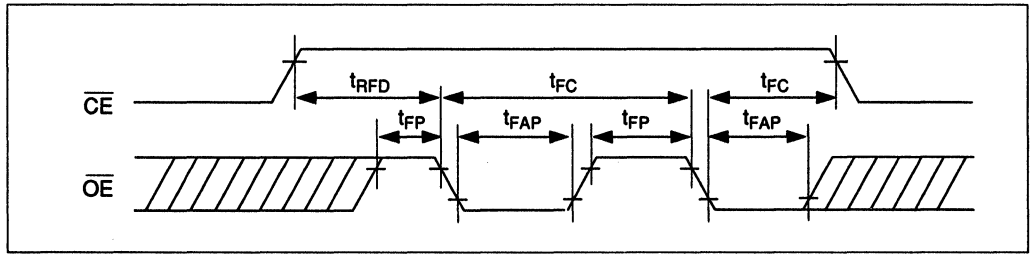
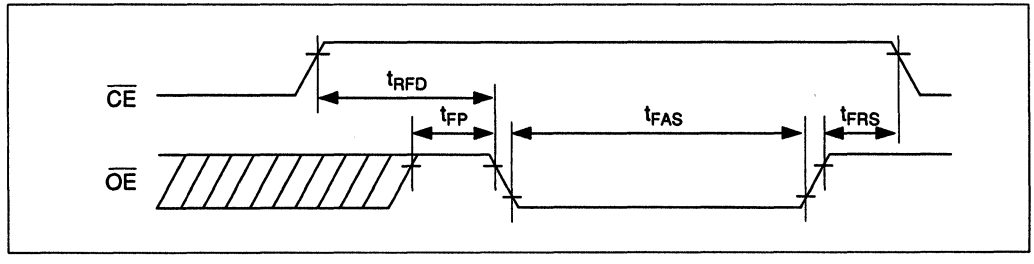
Static Column Mode Write Cycle



Automatic Refresh Cycle



Self Refresh Cycle



HM658128A Series

131072-word × 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128A is a pseudo-static RAM organized as 131,072-word × 8-bit. HM658128A realizes low power consumption and high speed access time by employing 1.3 µm CMOS process technology.

The HM658128A supports 3 refresh functions: address refresh, auto refresh and self refresh. Low power version dissipates only 0.5 mW (typ) in self refresh mode and retains the data with battery. Self refresh mode is guaranteed only for L-version and LL-version.

The HM658128A is pin-compatible with 1-Mbit static RAM.

Features

- Single 5 V (±10%)
- High speed
  - Access time
    $\overline{CE}$ Access time: 80/100/120 ns
  - Cycle time
    Random read/
    Write cycle time : 130/160/190 ns
- Low power: 300 mW typ (active)
  0.5 mW (standby)
- All inputs and outputs TTL compatible
- Non multiplexed address
- 512 refresh cycles (8 ms)
- Refresh functions
  Address refresh
  Automatic refresh
  Self refresh (Only for L-version and LL-version)

Ordering Information

Type No.	Access time	Package
HM658128ADP-8	80 ns	600-mil 32-pin plastic DIP (DP-32)
HM658128ADP-10	100 ns	
HM658128ADP-12	120 ns	
HM658128ALP-8	80 ns	
HM658128ALP-10	100 ns	
HM658128ALP-12	120 ns	
HM658128ALP-8L	80 ns	
HM658128ALP-10L	100 ns	
HM658128ALP-12L	120 ns	
HM658128ADFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658128ADFP-10	100 ns	
HM658128ADFP-12	120 ns	
HM658128ALFP-8	80 ns	
HM658128ALFP-10	100 ns	
HM658128ALFP-12	120 ns	
HM658128ALFP-8L	80 ns	
HM658128ALFP-10L	100 ns	
HM658128ALFP-12L	120 ns	
HM658128ALT-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP (TFP-32D)
HM658128ALT-10	100 ns	
HM658128ALT-12	120 ns	
HM658128ALT-8L	80 ns	
HM658128ALT-10L	100 ns	
HM658128ALT-12L	120 ns	
HM658128ADT-8	80 ns	
HM658128ADT-10	100 ns	
HM658128ADT-12	120 ns	
HM658128ADR-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TFP-32DR)
HM658128ADR-10	100 ns	
HM658128ADR-12	120 ns	
HM658128ALR-8	80 ns	
HM658128ALR-10	100 ns	
HM658128ALR-12	120 ns	
HM658128ALR-8L	80 ns	
HM658128ALR-10L	100 ns	
HM658128ALR-12L	120 ns	

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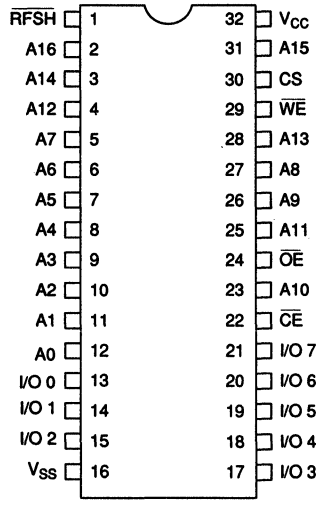
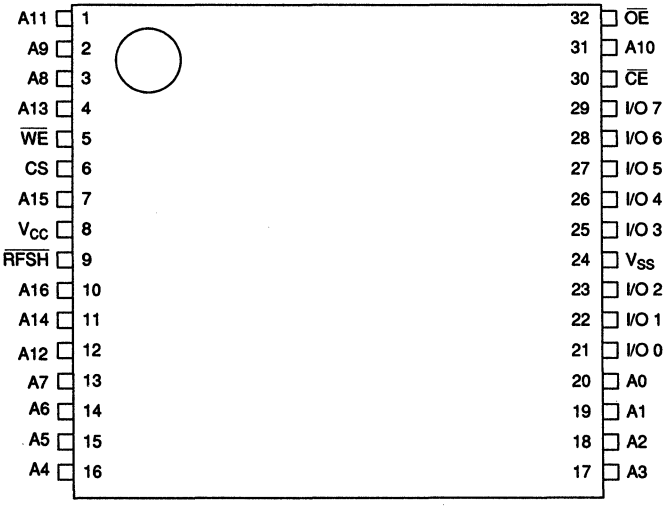
Pin Arrangement

HM658128AP/AFP Series



(Top View)

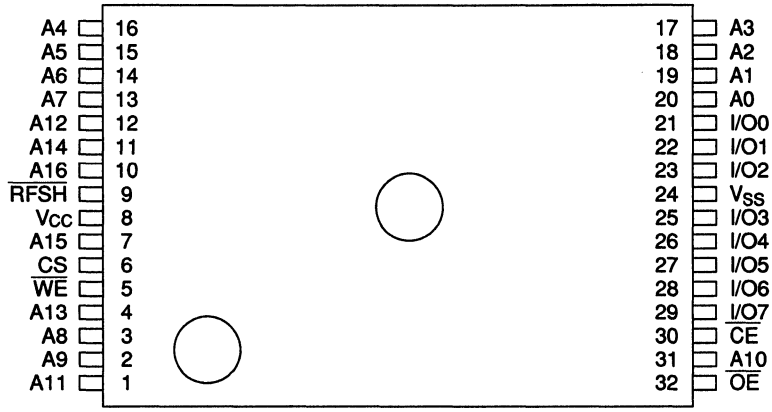
HM658128AT Series



(Top View)

Pin Arrangement (cont)

HM658128AR Series



(Top View)

Pin Description

Symbol	Pin name
A0 – A16	Address inputs
I/O0 – I/O7	Data input/output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
CS	Chip select
V_{CC}	Power supply
V_{SS}	Ground

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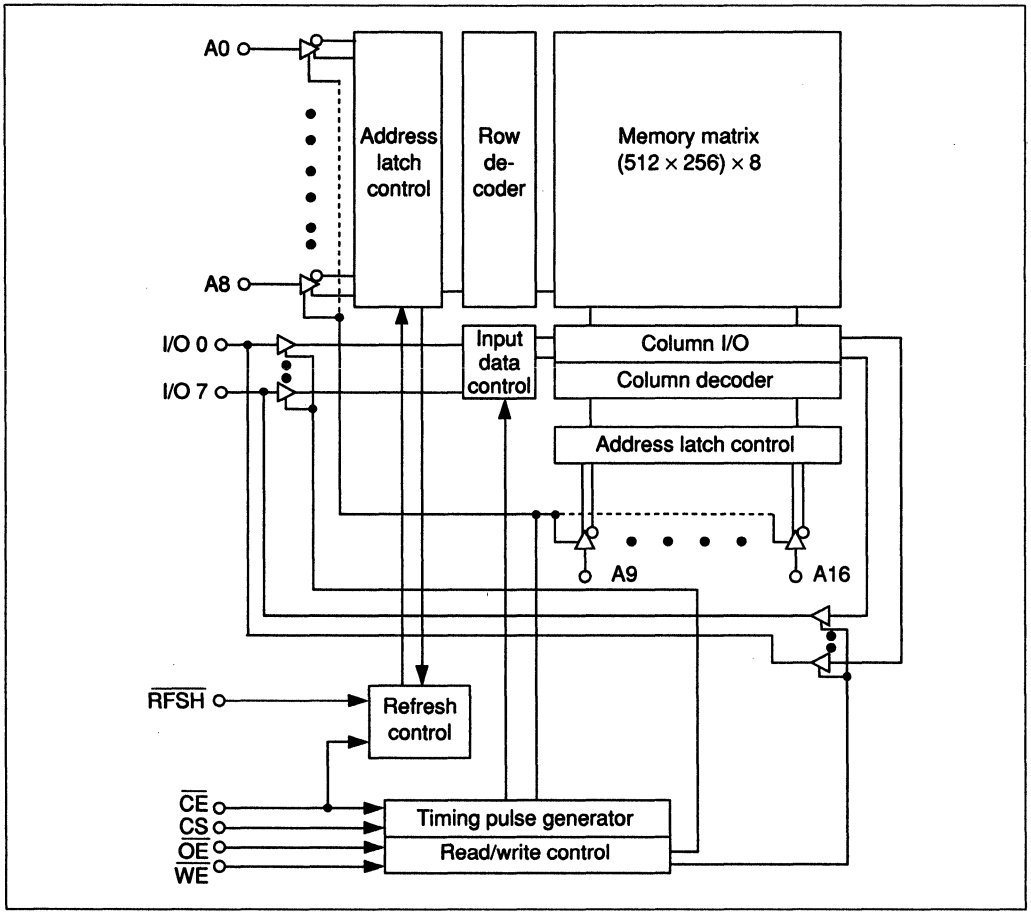
Block Diagram



Truth Table

$\overline{CE}$	CS at $\overline{CE}$ going low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O pin	Mode
L	H	X	L	H	Low-Z	Read
L	H	X	X	L	High-Z	Write
L	H	X	H	H	High-Z	—
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh*1
H	X	H	X	X	High-Z	Standby

Note: 1. Self refresh is guaranteed only for L-version and LL-version.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	– 0.5*1	—	0.8	V

Note: 1. V_{IL} min = –3.0 V for pulse width ≤ 10 ns.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Operating power supply current	I_{CC1}	—	60	85	mA	$I_{I/O}$ = 0 mA tcyc = min.
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}, Vin ≥ 0 V
Standby power supply current	I_{SB2}	—	100*1	200*1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V $\overline{RFSH}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V
		—	70*2	100*2	µA	
Operating power supply current in self refresh mode	I_{CC2}	—	1*1, *2	2*1, *2	mA	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	100*1	200*1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V $\overline{RFSH}$ ≤ 0.2 V, Vin ≥ 0 V
		—	70*2	100*2	µA	
Input leakage current	I_{LI}	–10	—	10	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	–10	—	10	µA	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LL-version.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
- Output load: 1 TTL and 100 pF (including scope and jig)

		HM658128A-8		HM658128A-10		HM658128A-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Random read or write cycle time	t_{RC}	130	—	160	—	190	—	ns
Random read-modify-write cycle time	t_{RWC}	190	—	220	—	260	—	ns
Chip enable access time	t_{CEA}	—	80	—	100	—	120	ns
Output enable access time	t_{OEA}	—	30	—	30	—	40	ns
Chip disable to output in high-Z	t_{CHZ}	0	30	0	30	0	35	ns
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	20	—	ns
Output disable to output in high-Z	t_{OHZ}	—	25	—	25	—	30	ns
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip enable pulse width	t_{CE}	80 ns	10 µs	100 ns	10 µs	120 ns	10 µs	
Chip enable precharge time	t_P	40	—	50	—	60	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address hold time	t_{AH}	30	—	30	—	35	—	ns
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns
$\overline{RFSH}$ hold time	t_{RHC}	15	—	15	—	15	—	ns
Chip select setup time	t_{CSS}	0	—	0	—	0	—	ns
Chip select hold time	t_{CSH}	30	—	30	—	35	—	ns
Write command pulse width	t_{WP}	30	—	30	—	35	—	ns
Chip enable to end of write	t_{CW}	80	—	100	—	120	—	ns
Data in to end of write	t_{DW}	25	—	25	—	30	—	ns
Data in hold time for write	t_{DH}	0	—	0	—	0	—	ns

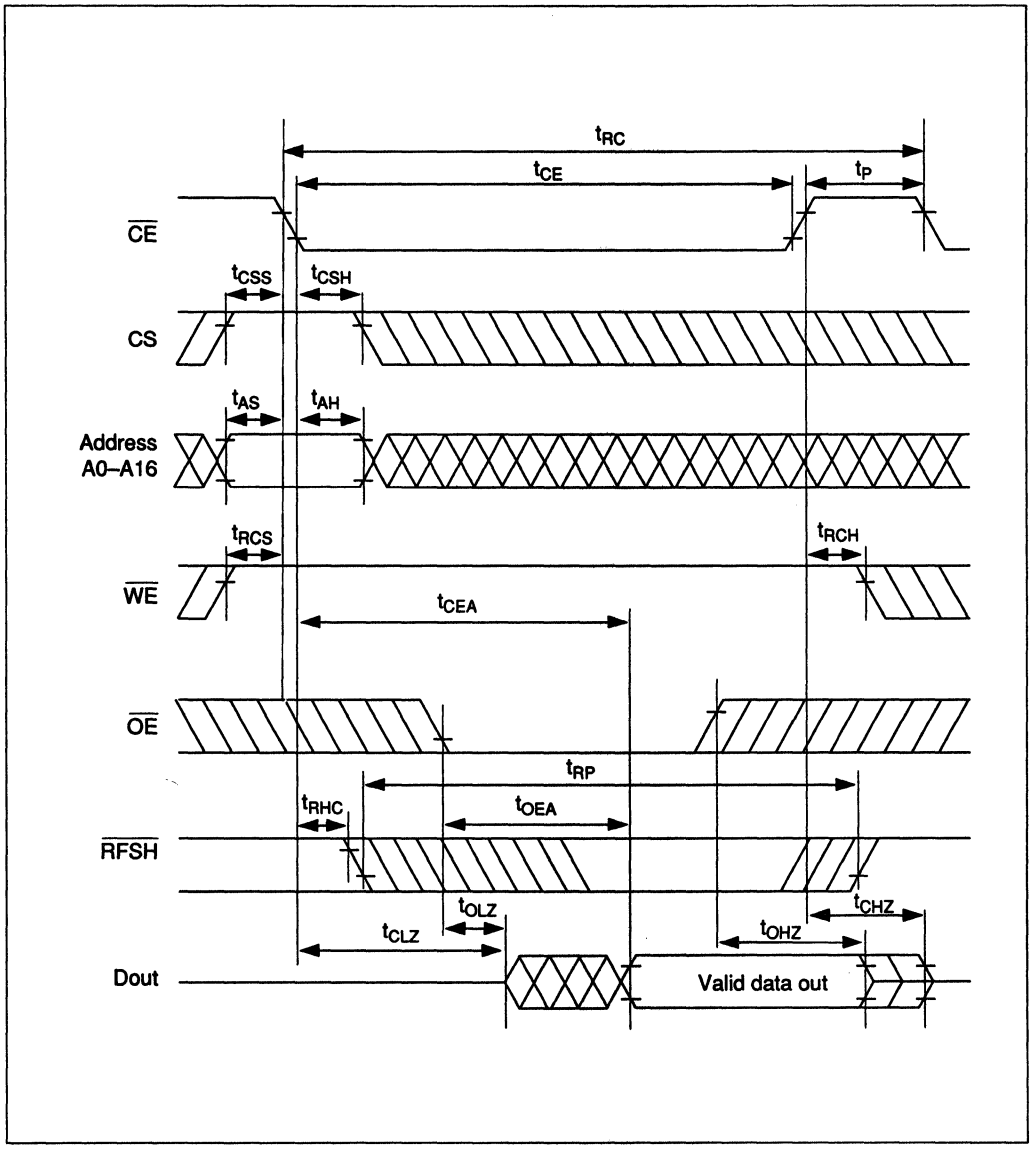
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

		HM658128A-8		HM658128A-10		HM658128A-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns
Write to output in high-Z	t_{WHZ}	—	25	—	25	—	30	ns
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns
Refresh command delay time	t_{RFD}	40	—	50	—	60	—	ns
Refresh precharge time	t_{FP}	40	—	40	—	40	—	ns
Refresh command pulse width	t_{RP}	—	8	—	8	—	8	µs
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs	80 ns	8 µs	
Automatic refresh cycle time	t_{FC}	130	—	160	—	190	—	ns
Refresh command pulse width for self refresh	t_{FAS} *9	8	—	8	—	8	—	µs
Refresh reset time for self refresh	t_{RFS} *9	130	—	160	—	190	—	ns
Refresh period (512 cycles)	t_{REF}	—	8	—	8	—	8	ms

Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause more than 100 µs and execute at least 8 initialization cycles.
8. 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15 µs after self refresh, in order to meet the refresh specification of 8 ms and 512 cycles.
9. This characteristics is guaranteed only for L-version and LL-version.
10. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, $\overline{CE}$ and $\overline{RFSH}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{RFSH}$ at the beginning of auto refresh must not occur during t_{RFS} period.

Timing Waveforms

Read Cycle



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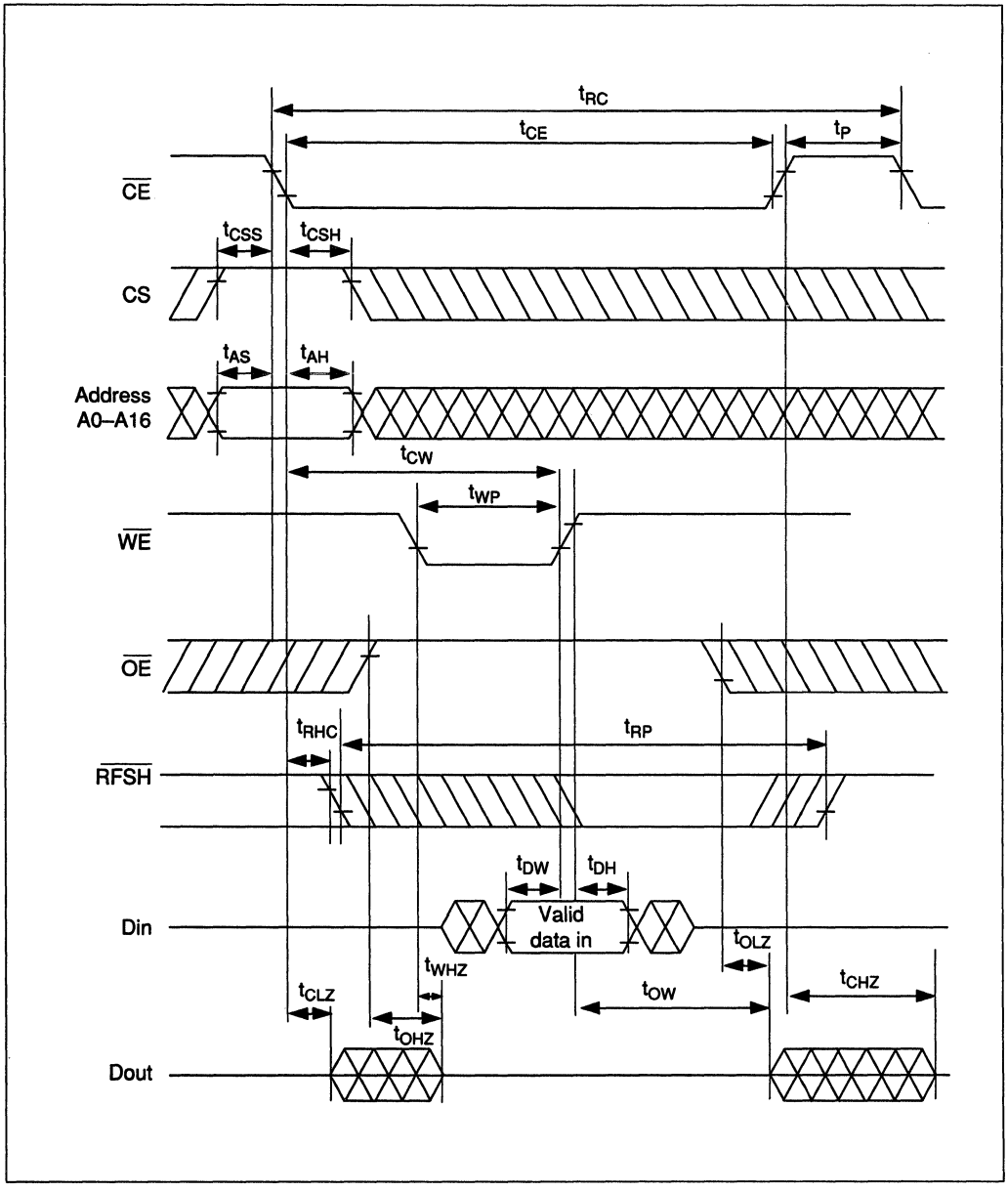
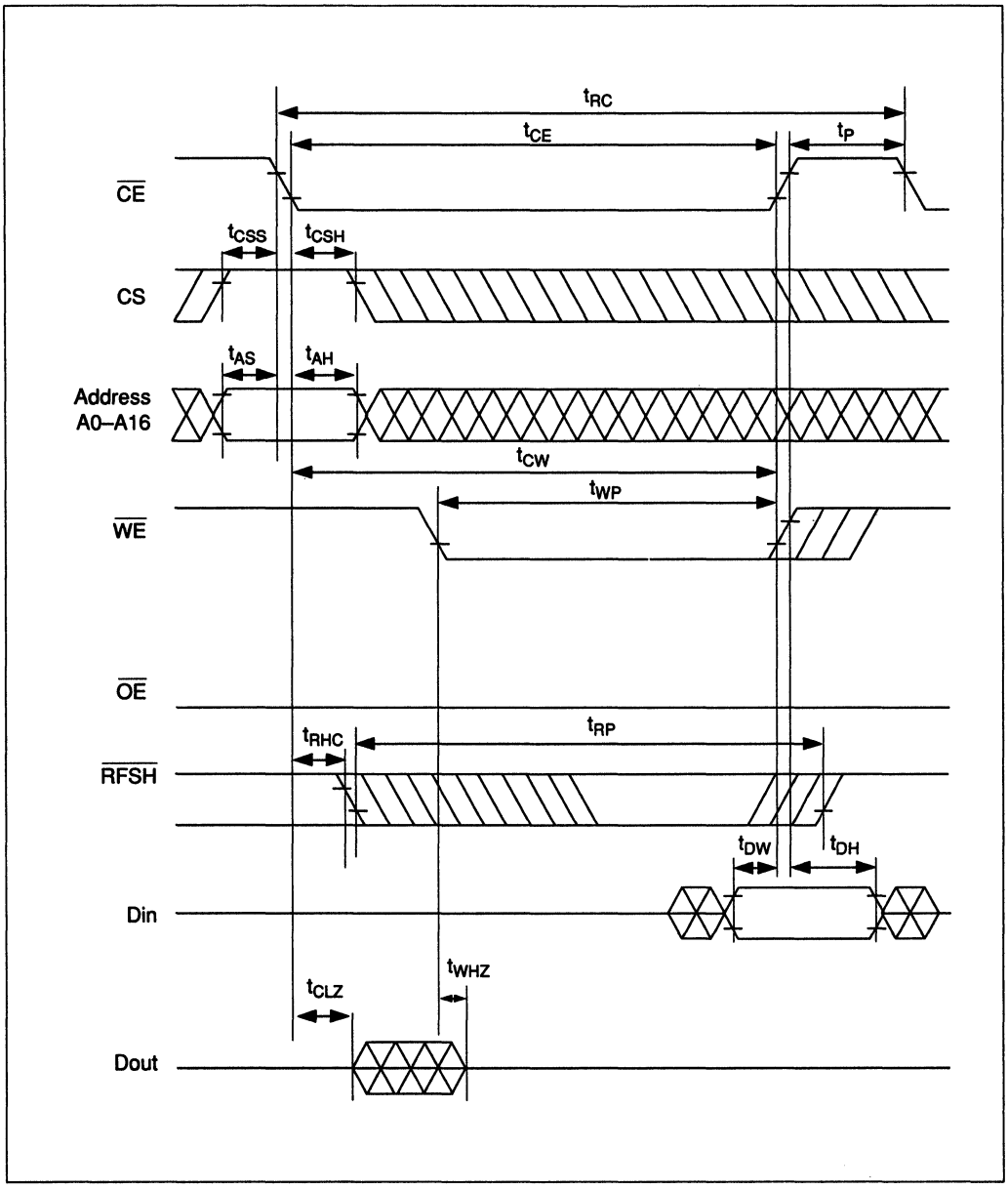
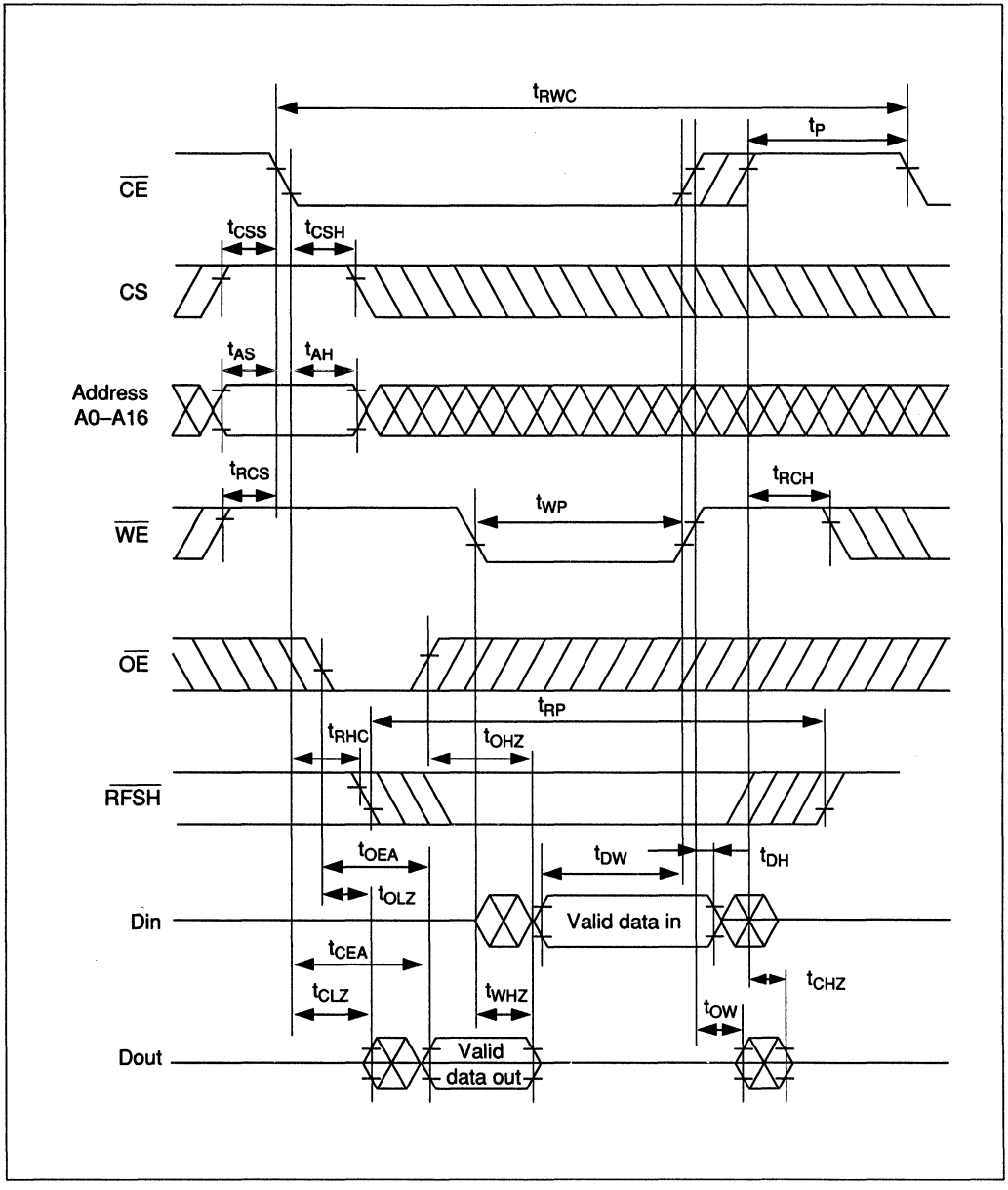
Write Cycle ($\overline{OE}$ clock)



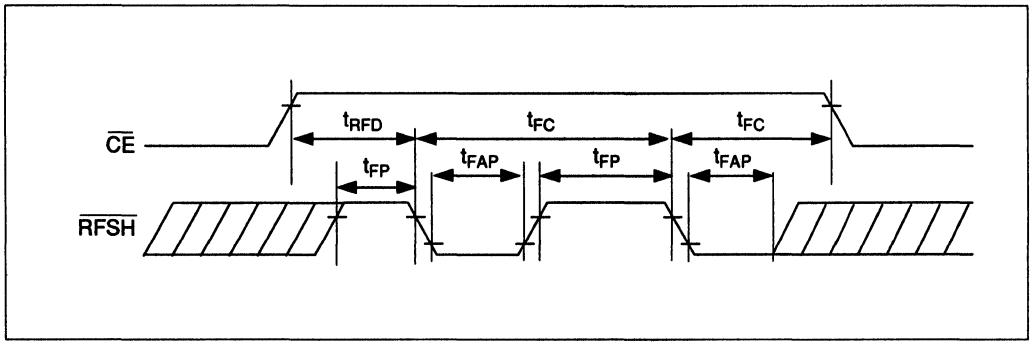
Write Cycle ($\overline{OE}$ Low Fix)



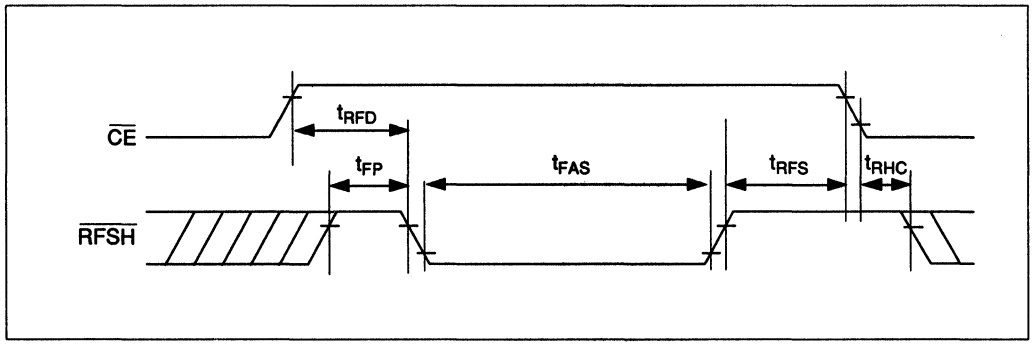
Read-Modify-Write Cycle



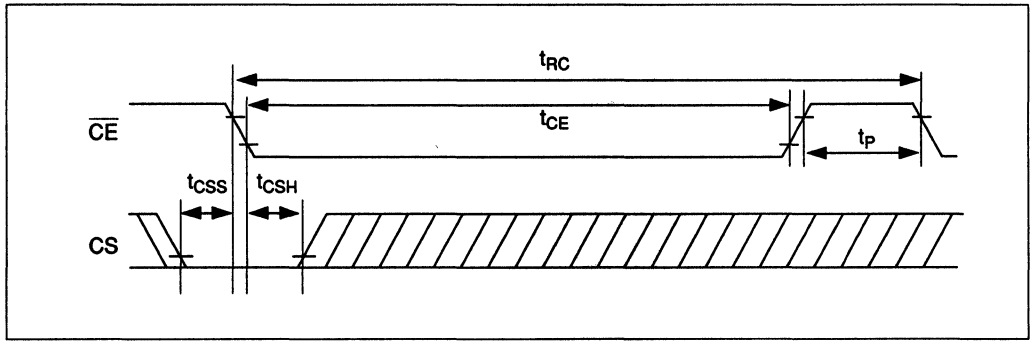
Auto Refresh Cycle



Self Refresh Cycle



CS Standby Mode



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HM658512 Series

524288-Word × 8-Bit High Speed Pseudo Static RAM

Features

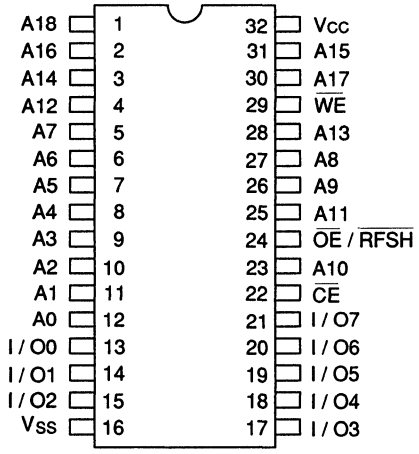
- Single 5 V (±10%)
- High speed
  - Access time
    $\overline{CE}$ access time: 80/85/100/120 ns
  - Cycle time
    Random read/write cycle time:
    130/160/190 ns
- Low power
  - 250 mW typ active
  - 350 µW typ standby (L-version)
  - 200 µW typ standby (LV-version)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
  - 32-pin TSOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - L-version: Address refresh
    LV-version Automatic refresh
    Self refresh
  - D-version: Address refresh
    Automatic refresh

Ordering Information

Type No.	Access	Package
HM658512LP-8	80 ns	600 mil 32-pin plastic DIP (DP-32)
HM658512LP-10	100 ns	
HM658512LP-12	120 ns	
HM658512LP-8V	80 ns	
HM658512LP-10V	100 ns	
HM658512LP-12V	120 ns	
HM658512DP-8	80 ns	
HM658512DP-10	100 ns	
HM658512DP-12	120 ns	
HM658512LFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658512LFP-85	85 ns	
HM658512LFP-10	100 ns	
HM658512LFP-12	120 ns	
HM658512LFP-8V	80 ns	
HM658512LFP-85V	85 ns	
HM658512LFP-10V	100 ns	
HM658512LFP-12V	120 ns	
HM658512DFP-8	80 ns	
HM658512DFP-10	100 ns	
HM658512DFP-12	120 ns	
HM658512DTT-8	80 ns	400 mil 32-pin plastic TSOP (TTP-32D)
HM658512DTT-10	100 ns	
HM658512DTT-12	120 ns	
HM658512LTT-8	80 ns	
HM658512LTT-85	85 ns	
HM658512LTT-10	100 ns	
HM658512LTT-12	120 ns	
HM658512LTT-8V	80 ns	
HM658512LTT-85V	85 ns	
HM658512LTT-10V	100 ns	
HM658512LTT-12V	120 ns	
HM658512DRR-8	80 ns	400 mil 32-pin plastic TSOP reverse type (TTP-32DR)
HM658512DRR-10	100 ns	
HM658512DRR-12	120 ns	
HM658512LRR-8	80 ns	
HM658512LRR-10	100 ns	
HM658512LRR-12	120 ns	
HM658512LRR-8V	80 ns	
HM658512LRR-10V	100 ns	
HM658512LRR-12V	120 ns	

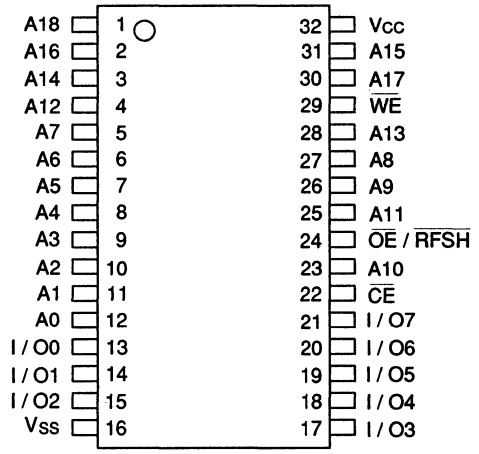
Pin Arrangement

HM658512P/FP Series



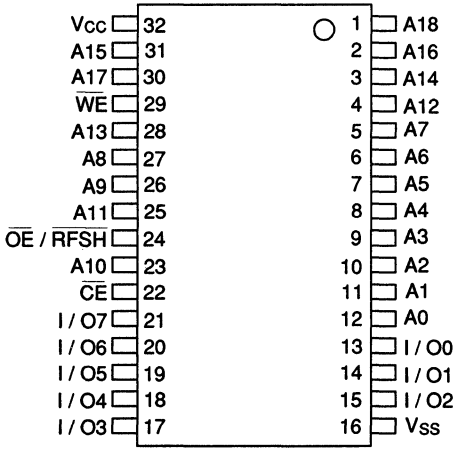
(Top View)

HM658512TT Series



(Top View)

HM658512RR Series



(Top View)

Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/$\overline{RFSH}$	Output enable/refresh
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

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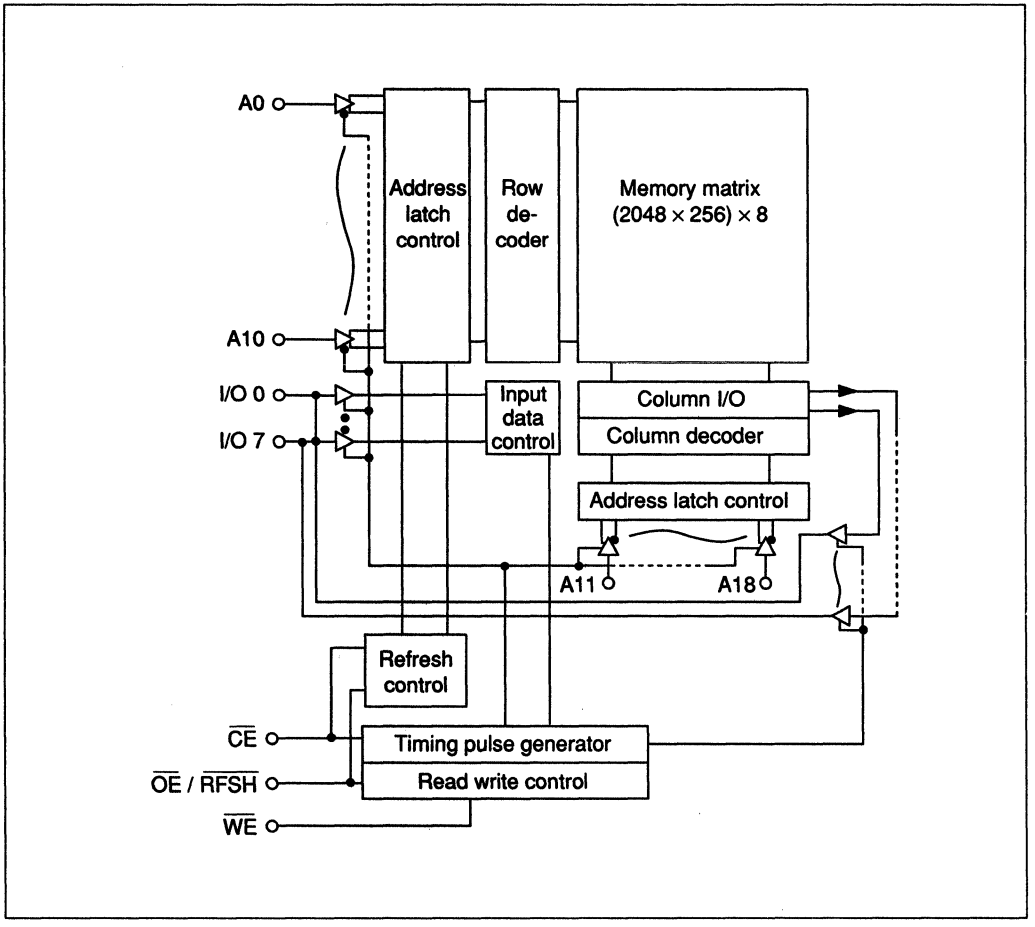
Block Diagram



Function Table

$\overline{CE}$	$\overline{OE}$/$\overline{RFSH}$	$\overline{WE}$	I/O pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh *2
H	H	X	High-Z	Standby

Notes: 1. X means don't care
2. Self refresh is guaranteed only for L-version and LV-version.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	−1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−1.0 *1	—	0.8	V

Note: 1. V_{IL} min = −3.0 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	—	75	mA	$I_{I/O}$ = 0 tcyc = min
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH}, Vin ≥ 0V $\overline{OE}$/$\overline{RFSH}$ = V_{IH}
	I_{SB2}	—	20 *1	200 *1	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V, Vin ≥ 0 V $\overline{OE}$/$\overline{RFSH}$ ≥ V_{CC} − 0.2 V
			20 *2	100 *2	µA	
Operating power supply current in self refresh mode	I_{CC2}	—	1 *1,2	2 *1,2	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/$\overline{RFSH}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	70 *1	200 *1	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V $\overline{OE}$/$\overline{RFSH}$ ≤ 0.2 V Vin ≥ 0 V
			40 *2	100 *2	µA	
Input leakage current	I_{LI}	−10	—	10	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LV-version.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output leakage current	I_{LO}	–10	—	10	µA	$\overline{OE}/\overline{RFSH}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA

Capacitance

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

Input pulse levels: 2.4 V, 0.4 V
Input rise and fall times: 5 ns
Timing measurement level: 2.2 V, 0.8 V
Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
Output load: 1 TTL and 100 pF

		HM658512-8		HM658512-85		HM658512-10		HM658512-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	tRC	130	—	135	—	160	—	190	—	ns	
Chip enable access time	tCEA	—	80	—	85	—	100	—	120	ns	
Read-modify-write cycle time	tRWC	180	—	190	—	220	—	260	—	ns	
Output enable access time	tOEA	—	30	—	30	—	40	—	50	ns	
Chip disable to output in high-Z	tCHZ	0	25	0	25	0	25	0	30	ns	1, 2

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

		HM658512-8		HM658512-85		HM658512-10		HM658512-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	20	—	20	—	ns	2
Output disable to output in high-Z	t_{OHZ}	—	25	—	25	—	25	—	30	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	0	—	ns	2
Chip enable pulse width	t_{CE}	80ns	10μs	85ns	10μs	100ns	10μs	120ns	10μs		
Chip enable precharge time	t_P	40	—	40	—	50	—	60	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address hold time	t_{AH}	20	—	20	—	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Write command pulse width	t_{WP}	25	—	25	—	30	—	35	—	ns	
Chip enable to end of write	t_{CW}	80	—	85	—	100	—	120	—	ns	
Chip enable to output delay time	t_{OCD}	0	—	0	—	0	—	0	—	ns	
Output enable hold time	t_{OHC}	15	—	15	—	15	—	15	—	ns	
Data in to end of write	t_{DW}	20	—	20	—	25	—	30	—	ns	
Data in hold time for write	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	2
Write to output in high-Z	t_{WHZ}	—	20	—	20	—	25	—	30	ns	1
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	

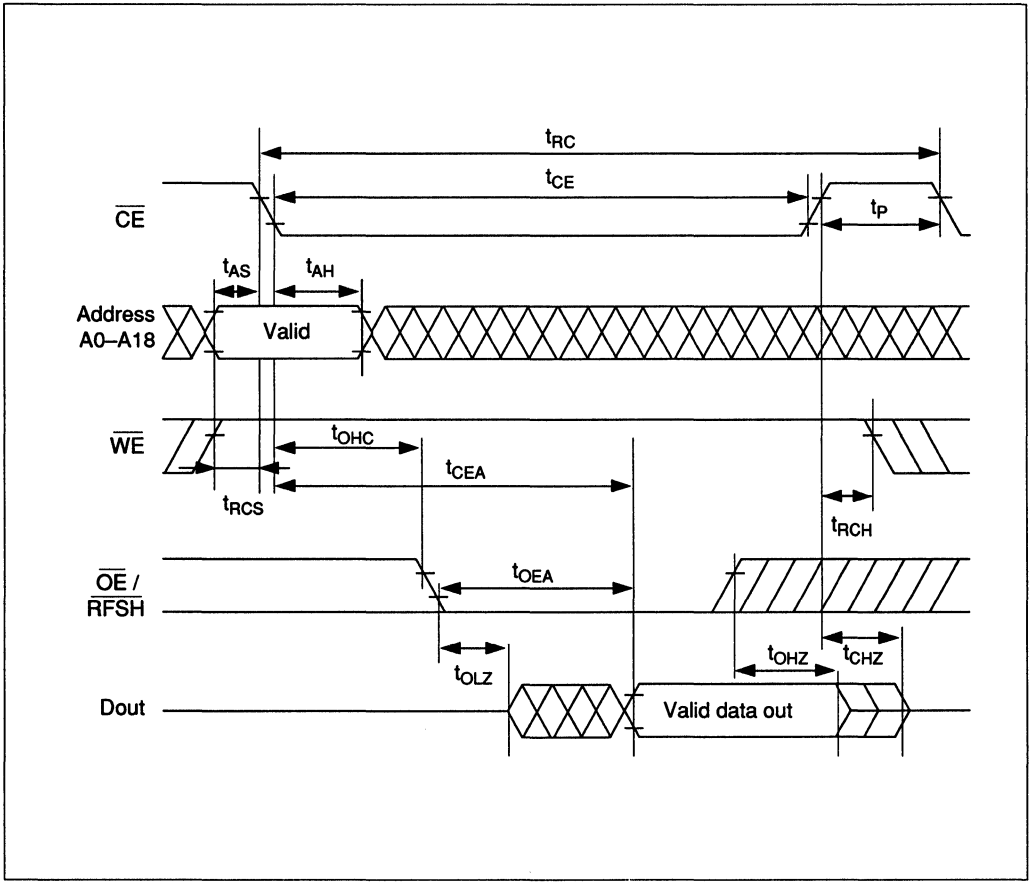
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

		HM658512-8		HM658512-85		HM658512-10		HM658512-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh command delay time	t_{RFD}	40	—	40	—	50	—	60	—	ns	
Refresh precharge time	t_{FP}	40	—	40	—	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	80ns	8µs	80ns	8µs	80ns	8µs	80ns	8µs		
Automatic refresh cycle time	t_{FC}	130	—	135	—	160	—	190	—	ns	
Refresh command pulse width for self refresh	t_{FAS}	8	—	8	—	8	—	8	—	µs	
Refresh reset time from self refresh	t_{RFS}	600	—	600	—	600	—	600	—	ns	
Refresh period	t_{REF}	—	32	—	32	—	32	—	32	ms	2048 cycle

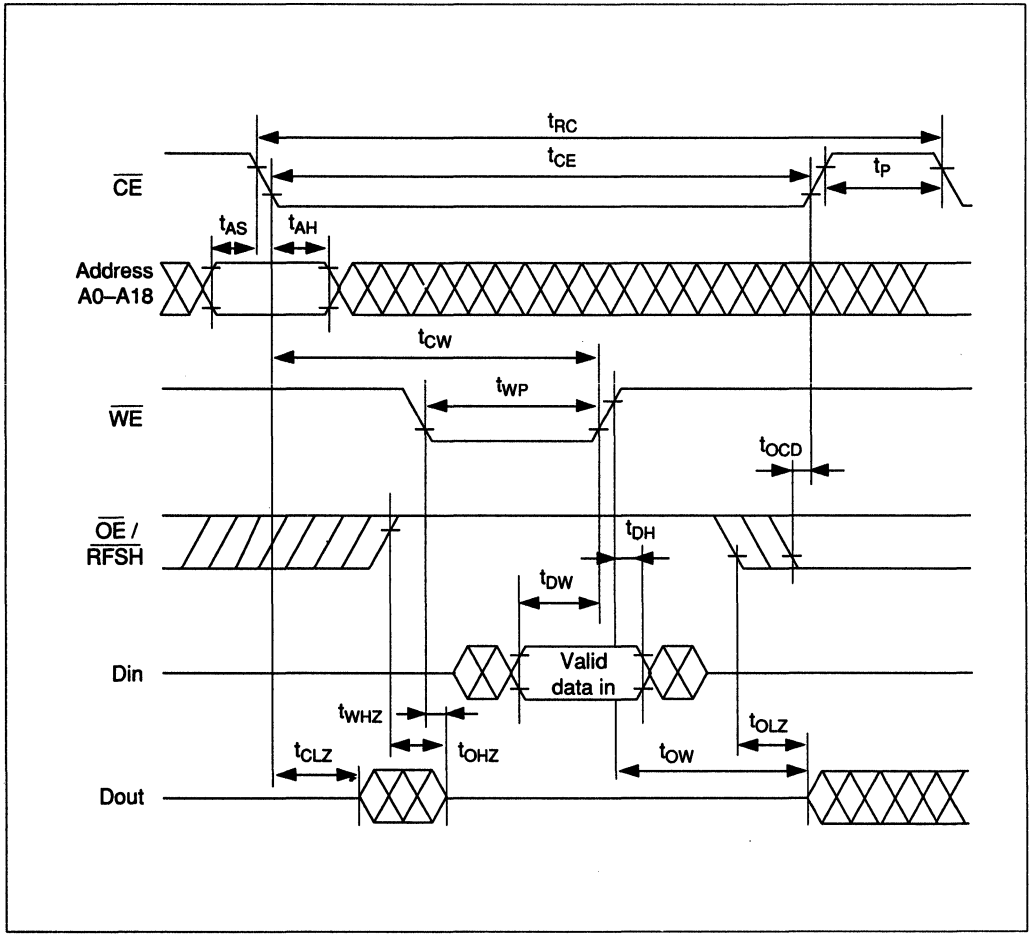
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CHZ}, t_{CLZ} t_{OHZ} t_{OLZ},t_{WHZ} and t_{OW}, are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause for more than 100 µs and execute at least 8 initialization cycles.
8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15µs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
9. This characteristics is guaranteed only for L-version and LL-version.
10. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, $\overline{CE}$ and $\overline{OE}$/$\overline{RFSH}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{OE}$/$\overline{RFSH}$ at the beginning of auto refresh must not occur during t_{RFS} period.

Timing Waveforms

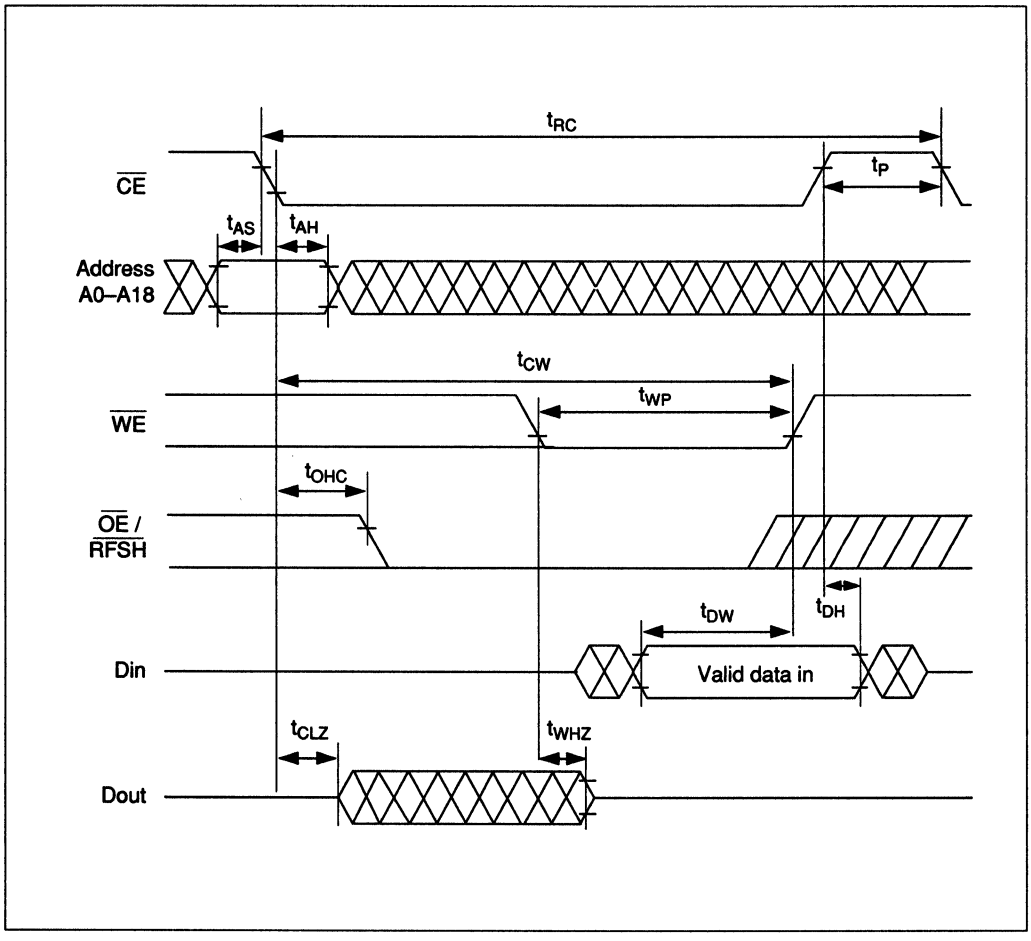
Read Cycle



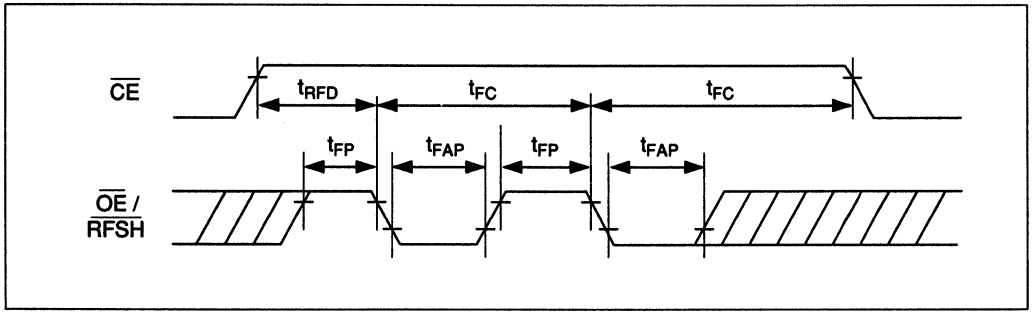
Write Cycle (1) ($\overline{OE}$ High)



Write Cycle (2) ($\overline{OE}$ Low)



Automatic Refresh Cycle



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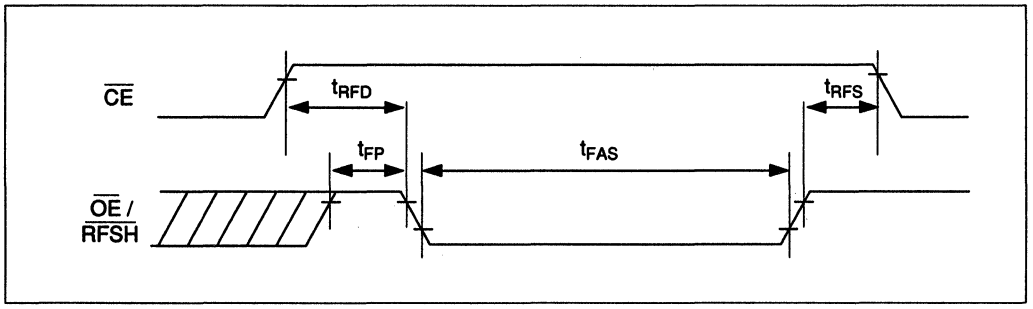
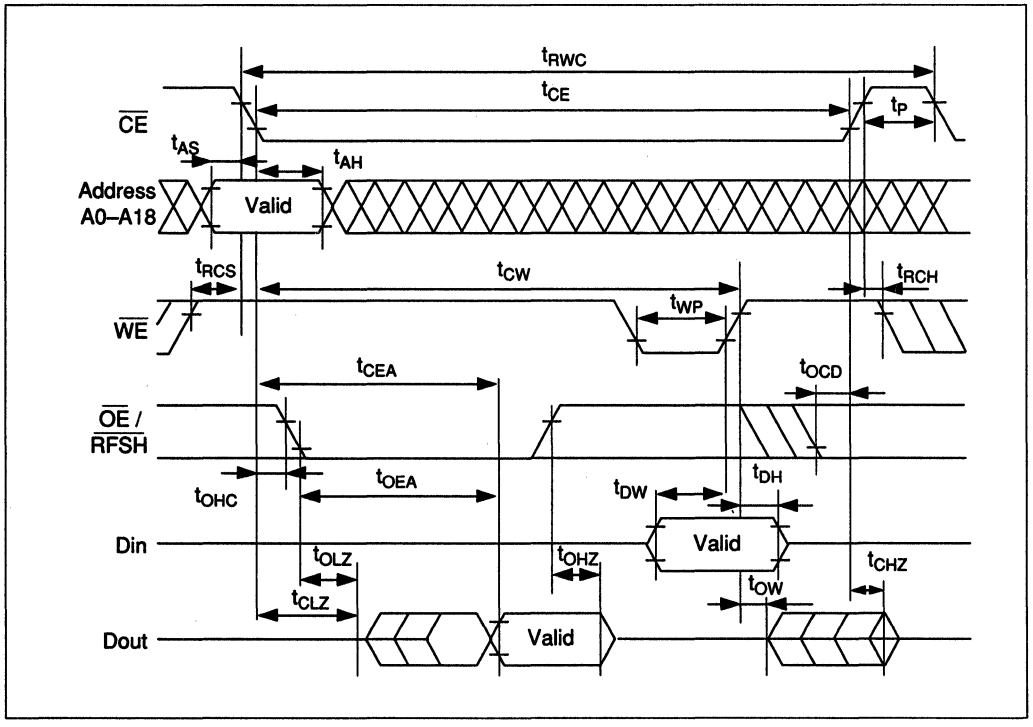
Self Refresh Cycle



Read-Modify-Write Cycle

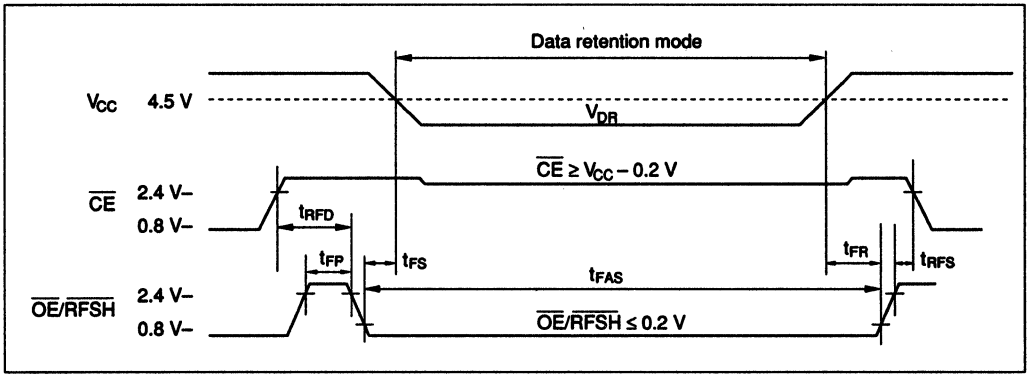


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for LV-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	3.0	—	5.5	V	
Self refresh current	I_{CCDR}	—	—	50	µA	V_{CC} = 3.0 V, $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ Vin ≥ 0 V
		—	—	100	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ Vin ≥ 0 V
Refresh setup time	t_{FS}	0	—	—	ns	
Operation recovery time	t_{FR}	5	—	—	ms	

Low V_{CC} Data Retention Timing Waveform



Notes: 1. Rise time and fall time of power supply voltage must be smaller than 0.05 V/ms.
2. Keep $\overline{CE} \geq V_{CC} - 0.2$ V during data retention mode.
3. Regarding t_{RFD}, t_{FP}, t_{FAS} and t_{RFS}, refer to AC characteristics.
4. Input voltage should be lower than V_{CC} + 1.5 V in data retention mode.

6

HM65V8512 Series

3.0 V & 3.3 V Supply

524288-Word × 8-Bit High Speed Pseudo Static RAM

Description

HM65V8512 is a pseudo-static RAM organized as 524,288-word × 8-bit. HM65V8512 realized low power consumption by employing 0.8 μm CMOS process technology.

Power supply voltage if 3 V ± 10% and all inputs and outputs are CMOS compatible. The low power version dissipates only 60 μW (typ) in self refresh mode, so it retains the data with battery.

The HM65V8512 is pin-compatible with 4-Mbit static RAM and with 4-Mbits 5 V operation Pseudo Static RAM.

Features

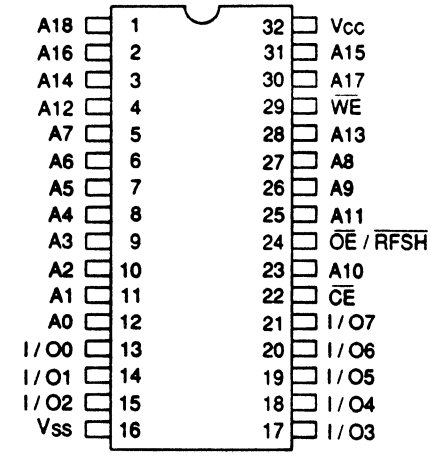
- Single 3 V (±10%)
- High speed
  - —Access time
    CE access time: 120 ns/150 ns (max)
  - —Cycle time
    Random read.write cycle time:
    190 ns/230 ns (min)
- Low power
  - —75 mW typ active
  - —60 μW typ standby
- All inputs and outputs CMOS compatible
- Package
  - —32-pin SOP package
  - —32-pin TSOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions:
  - —L/LV-version: Address refresh
    Automatic refresh
    Self refresh
  - —D-version: Address refresh
    Automatic refresh

Ordering Information

Type No.	Access time	Package
HM65V8512DFP-12	120 ns	32-pin plastic SOP (FP-32D)
HM65V8512DFP-15	150 ns	
HM65V8512LFP-12	120 ns	
HM65V8512LFP-15	150 ns	
HM65V8512LFP-12V	120 ns	
HM65V8512LFP-15V	150 ns	
HM65V8512DTT-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP (TTP-32D)
HM65V8512DTT-15	150 ns	
HM65V8512LTT-12	120 ns	
HM65V8512LTT-15	150 ns	
HM65V8512LTT-12V	120 ns	
HM65V8512LTT-15V	150 ns	
HM65V8512DRR-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TTP-32DR)
HM65V8512DRR-15	150 ns	
HM65V8512LRR-12	120 ns	
HM65V8512LRR-15	150 ns	
HM65V8512LRR-12V	120 ns	
HM65V8512LRR-15V	150 ns	

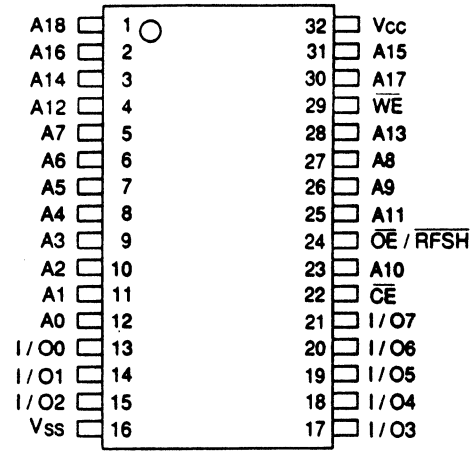
Pin Arrangement

HM65V8512FP Series



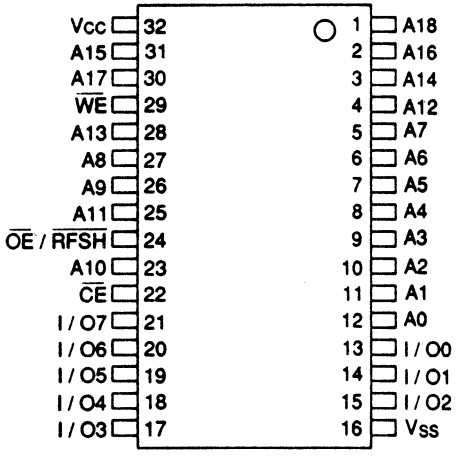
(Top View)

HM65V8512TT Series



(Top View)

HM65V8512RR Series



(Top View)

Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/$\overline{RFSH}$	Output enable/refresh

Pin name	Function
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

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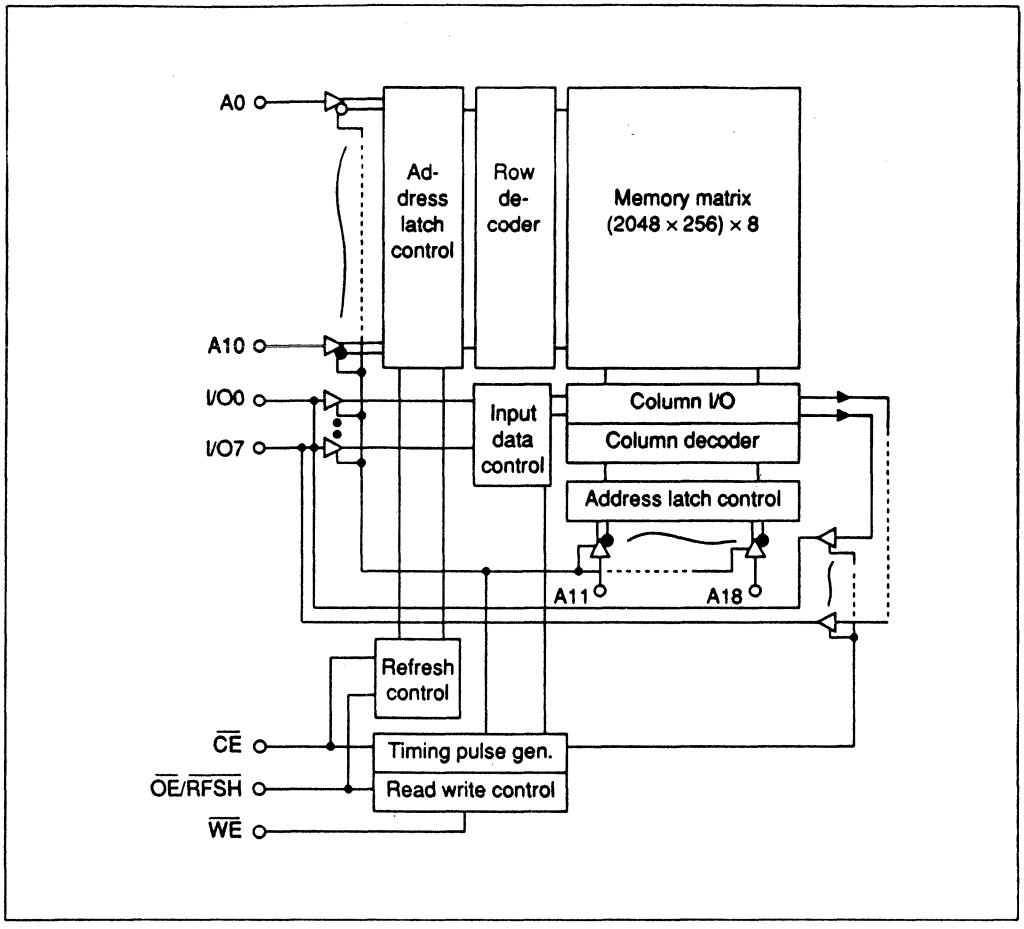
Block Diagram



Function Table

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	$\overline{WE}$	I/O pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh *2
H	H	X	High-Z	Standby

Notes: 1. X means don't care
2. Self refresh is guaranteed only for L-version and LV-version.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–0.5 to +6.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.1	—	6.0	V
	V_{IL}	–0.5 *1	—	0.7	V

Note: 1. V_{IL} min = –1.2 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	25	40	mA	$I_{I/O}$ = 0 tcyc = min
Standby power supply current	I_{SB1}	—	—	0.5	mA	$\overline{CE}$ = V_{IH}, Vin ≥ 0V $\overline{OE}$/$\overline{RFSH}$ = V_{IH}
	I_{SB2}	—	8	20	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V $\overline{OE}$/$\overline{RFSH}$ ≥ V_{CC} – 0.2 V
Operating power supply current in self refresh mode	I_{CC2}	—	—	0.5 *1	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/$\overline{RFSH}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	20 *1	40 *1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V $\overline{OE}$/$\overline{RFSH}$ ≤ 0.2 V Vin ≥ 0 V
Input leakage current	I_{LI}	–5	—	5	µA	V_{CC} = 3.3 V Vin = V_{SS} to V_{CC}

Notes: 1. This characteristics is guaranteed only for L-version and LV-version.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output leakage current	I_{LO}	−5	—	5	µA	$\overline{OE}/\overline{RFSH}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA
	V_{OH}	2.6	—	—	V	I_{OH} = −100 µA

Capacitance

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%)

Test Conditions

Input pulse levels: 2.4 V, 0.6 V
Input rise and fall times: 5 ns
Timing measurement level: 1.5 V
Reference level: V_{OH} = 2.1 V, V_{OL} = 0.9 V
Output load: 50 pF

		HM65V8512-12		HM65V8512-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	190	—	230	—	ns	
Chip enable access time	t_{CEA}	—	120	—	150	ns	
Read-modify-write cycle time	t_{RWC}	250	—	290	—	ns	
Output enable access time	t_{OEA}	—	60	—	80	ns	
Chip disable to output in high-Z	t_{CHZ}	0	30	0	30	ns	1, 2
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	ns	2
Output disable to output in high-Z	t_{OHZ}	—	30	—	30	ns	1, 2
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	ns	2

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%) (cont)

Parameter	Symbol	HM65V8512-12 Min	HM65V8512-12 Max	HM65V8512-15 Min	HM65V8512-15 Max	Unit	Notes
Chip enable pulse width	t_{CE}	120 ns	10 µs	150 ns	10 µs		
Chip enable precharge time	t_P	70	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address hold time	t_{AH}	30	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	
Write command pulse width	t_{WP}	35	—	35	—	ns	
Chip enable to end of write	t_{CW}	120	—	150	—	ns	
Chip enable to output enable delay time	t_{OCD}	0	—	0	—	ns	
Output enable hold time	t_{OHC}	15	—	15	—	ns	
Data in to end of write	t_{DW}	30	—	30	—	ns	
Data in hold time for write	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Write to output in high-Z	t_{WHZ}	—	30	—	30	ns	1, 2
Transition time (rise and fall)	t_T	3	50	3	50	ns	6
Refresh command delay time	t_{RFD}	70	—	80	—	ns	
Refresh precharge time	t_{FP}	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs		
Automatic refresh cycle time	t_{FC}	190	—	230	—	ns	
Refresh command pulse width for self refresh	t_{FAS} *9	8	—	8	—	µs	
Refresh reset time from self refresh	t_{RFS} *9	600	—	600	—	ns	
Refresh period	t_{REF}	—	32	—	32	ms	2048 cycle

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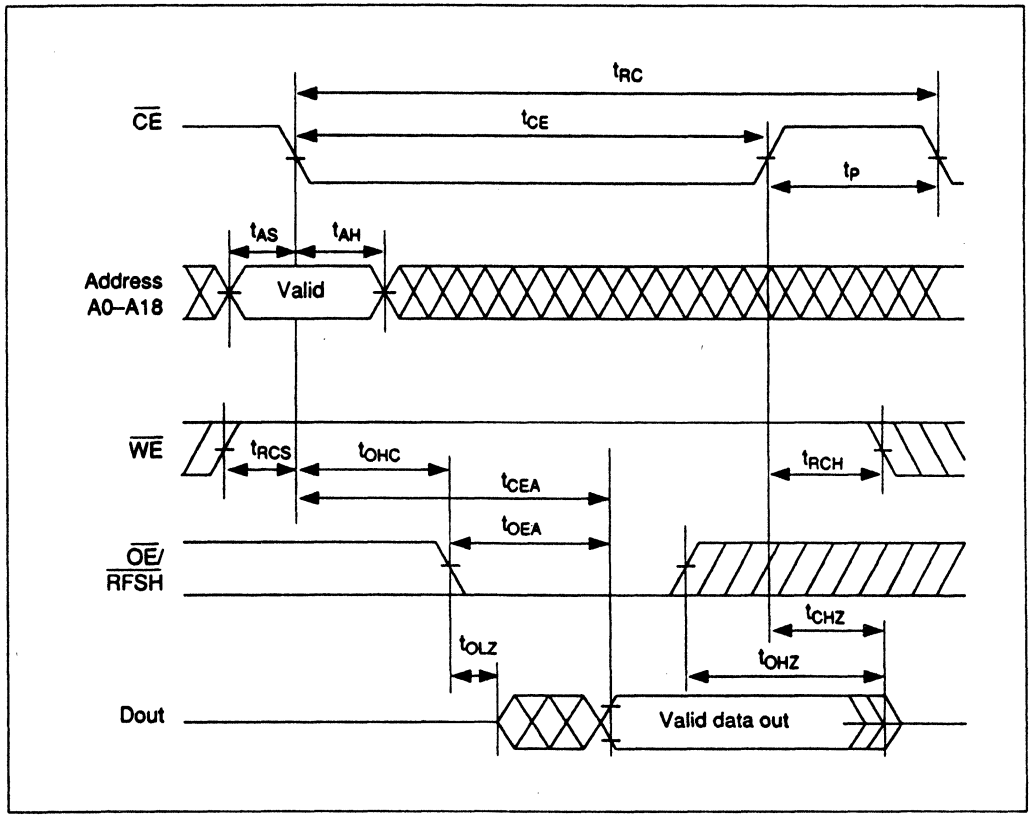
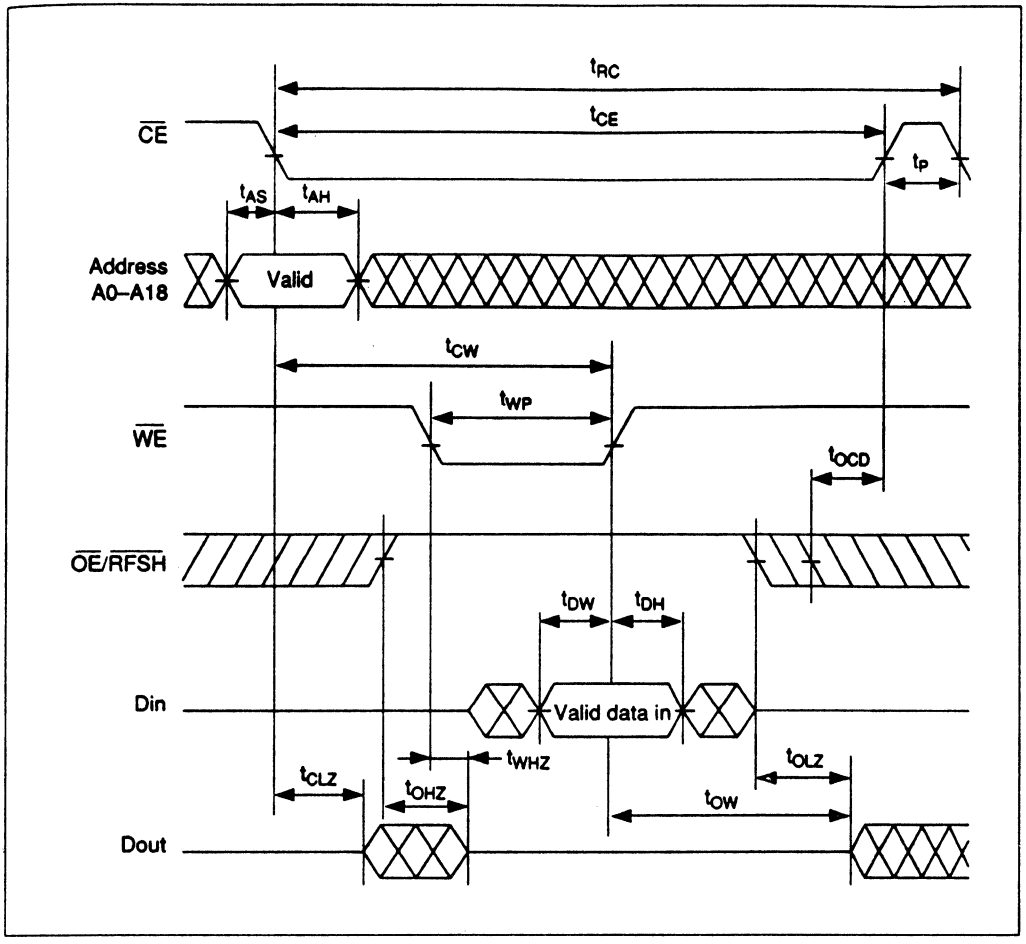
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CHZ}, t_{CLZ} t_{OHZ} t_{OLZ},t_{WHZ} and t_{OW}, are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause for more than 100 µs and execute at least 8 initialization cycles.
8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15µs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
9. This characteristics is guaranteed only for L-version and LV-version.
10. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, $\overline{CE}$ and $\overline{OE}$/$\overline{RFSH}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{OE}$/$\overline{RFSH}$ at the beginning of auto refresh must not occur during t_{RFS} period.

Timing Waveforms

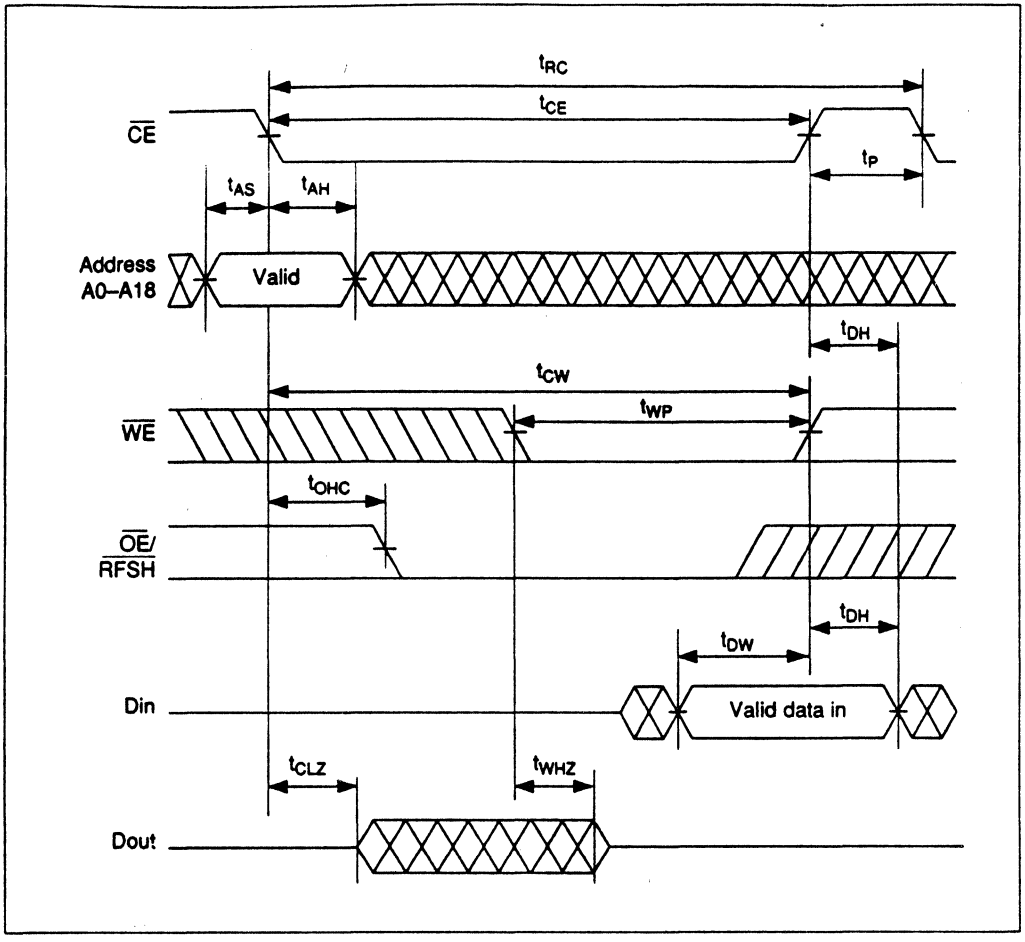
Read Cycle



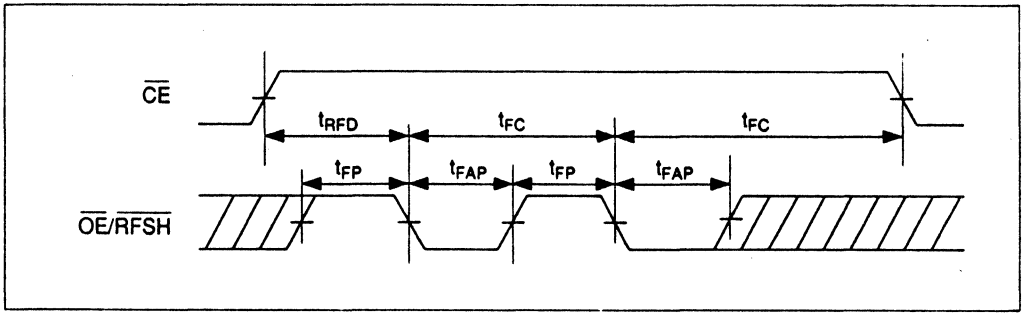
Write Cycle (1) ($\overline{OE}$ High)



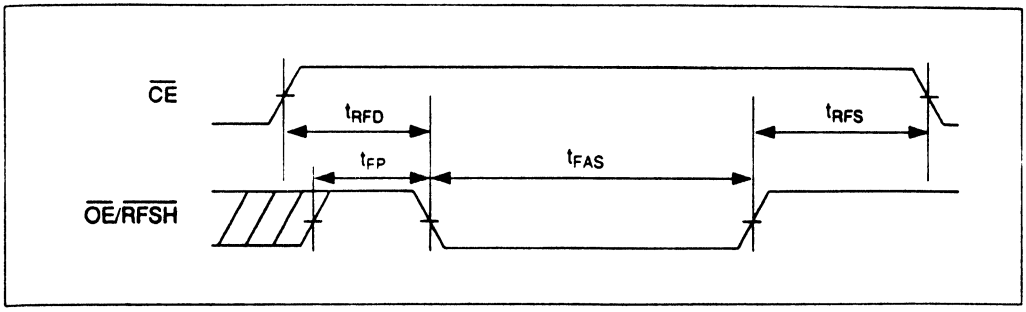
Write Cycle (2) ($\overline{OE}$ Low)



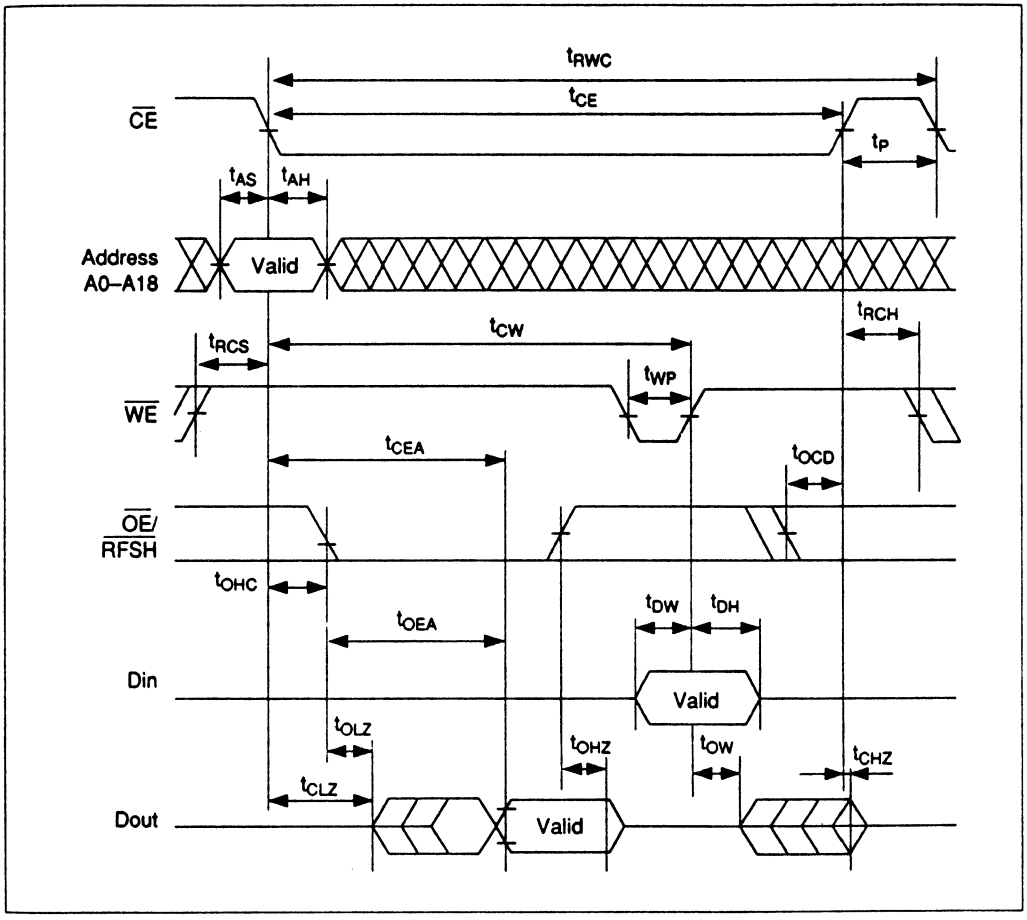
Automatic Refresh Cycle



Self Refresh Cycle



Read-Modify-Write Cycle



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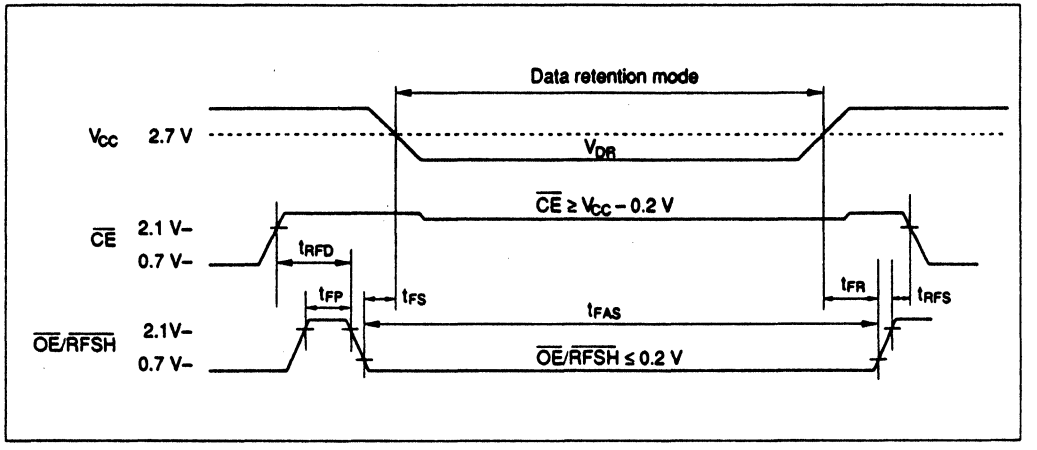
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	3.3	V	
Self refresh current	I_{CCDR}	—	—	25	µA	V_{CC} = 2.0 V others ≥ 0 V $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ V
		—	—	40	µA	V_{CC} = 3.3 V others ≥ 0 V $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ V
Refresh to data retention time	t_{FS}	0	—	—	ns	
Operation recovery time	t_{FR}	5	—	—	ms	

Note: This characteristics is guaranteed only for LV-version.

Low V_{CC} Data Retention Timing Waveform



Notes: 1. t_R, t_F of power supply voltage must be smaller than 0.05 V/ms.
2. Keep $\overline{CE} \geq V_{CC} - 0.2$ V during data retention mode.
3. Regarding t_{RFS}, t_{FP}, t_{FAS} and t_{RFS}, refer to AC characteristics.

524,288-word × 8-bit High Speed Pseudo Static RAM

Description

HM65W8512 is a pseudo-static RAM organized as 524,288-word × 8-bit. Power supply voltage is 3.3 V ± 0.3 V. HM65W8512 utilizes the same die as HM65V8512, V_{CC} of which is 3.0 V ± 10%. Therefore, the electrical characteristics is same as that of HM65V8512 except mentioned below.

Features

- Single 3.3 V ± 0.3 V
- High speed
  - —Access time
    $\overline{CE}$ access time: 120 ns/150 ns (max)
  - —Cycle time
    Random read/Write cycle time:
    190 ns/230 ns (max)
- Low power
  - —100 mW typ (active)
  - —85 μW typ (standby)
- Package
  - —32-pin SOP package
  - —32-pin TSOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - —L/LV version: Address refresh
    Automatic refresh
    Self refresh
  - —D version: Address refresh
    Automatic refresh

The characteristics of HM65W8512 is same as that of HM65V8512 except mentioned below. Regarding pin arrangement, function table, absolute maximum ratings, capacitance and AC characteristics, please refer to the pages of HM65V8512.

Ordering Information

Type No.	Access time	Package
HM65W8512DFP-12	120 ns	32-pin plastic SOP (FP-32D)
HM65W8512DFP-15	150 ns	
HM65W8512LFP-12	120 ns	
HM65W8512LFP-15	150 ns	
HM65W8512LFP-12V	120 ns	
HM65W8512LFP-15V	150 ns	
HM65W8512DTT-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP (TTP-32D)
HM65W8512DTT-15	150 ns	
HM65W8512LTT-12	120 ns	
HM65W8512LTT-15	150 ns	
HM65W8512LTT-12V	120 ns	
HM65W8512LTT-15V	150 ns	
HM65W8512DRR-12	120 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TTP-32DR)
HM65W8512DRR-15	150 ns	
HM65W8512LRR-12	120 ns	
HM65W8512LRR-15	150 ns	
HM65W8512LRR-12V	120 ns	
HM65W8512LRR-15V	150 ns	

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Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −1.2 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	30	50	mA	I_{VO} = 0 tcyc = min
Standby power supply current	I_{SB1}	—	—	1.0	mA	$\overline{CE}$ = V_{IH}, Vin ≥ 0V $\overline{OE}$/RFSH = V_{IH}
	I_{SB2}	—	15	30	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V, Vin ≥ 0V $\overline{OE}$/RFSH ≥ V_{CC} − 0.2 V
Operating power supply current in self refresh mode	I_{CC2}	—	—	1.0*1	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/RFSH = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	25*1	50*1	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V $\overline{OE}$/RFSH ≤ 0.2 V Vin ≥ 0V
Input leakage current	I_{LI}	−5	—	5	µA	V_{CC} = 3.3 V Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	−5	—	5	µA	$\overline{OE}$/RFSH = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
	V_{OH}	2.4	—	—	V	I_{OH} = −2 mA

Note: 1. This characteristics is guaranteed only for L-version and LV-version.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for LV-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	
Self refresh current	I_{CCDR}	—	—	25	µA	V_{CC} = 2.0 V others ≥ 0 V $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ V
		—	—	50	µA	V_{CC} = 3.6 V others ≥ 0 V $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ V
Refresh to data retention time	t_{FS}	0			ns	
Operation recovery time	t_{FR}	5			ms	

Timing Waveform

Regarding low V_{CC} data retention timing waveform, please refer to HM65V8512.

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SECTION 7

STATIC RAM MODULES

- Medium Speed Static RAM Modules

524,288-word × 8-bit High Density CMOS Static RAM Module

The HM66205L is a high density 4-Mbit static RAM module which consists of 4 pieces HM628128LT products (TSOP type 1M static RAM) and a HD74ACT138FP equivalent product (SOP type CMOS decoder logic).
An outline of the HM66205L is the standard 600-mil width 32-pin dual-in-line package. Its pin arrangement is completely compatible with 4-Mbit monolithic static RAM.
The HM66205L offers the features of low power and high speed by using high speed CMOS devices. And, the HM66205L makes high density mounting possible without surface mount technology.
These features make the HM66205L ideally suited for high density compacted memory systems.

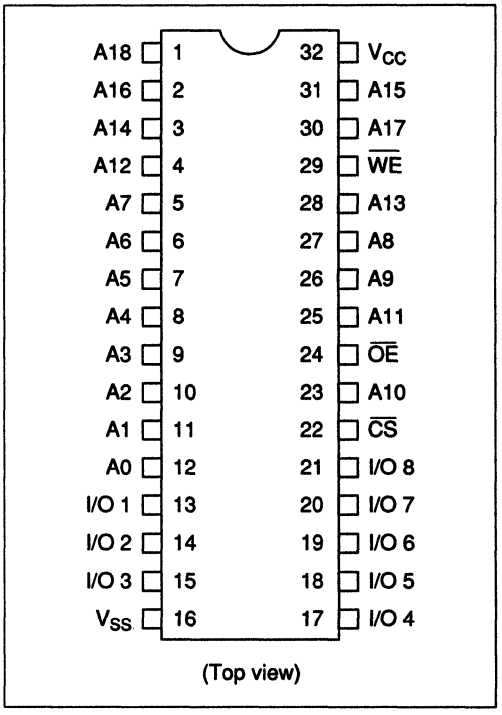
Features

- High density 32-pin DIP
  - Mounting 4 pcs. of 1M static RAM (TSOP; HM628128LT) and CMOS decoder logic (SOP; HD74ACT138FP equivalent)
- Pin compatible with 4M monolithic static RAM
- High speed
  - Fast access time: 85 ns/100 ns/120 ns (max)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby: 40 µW (typ)
  - Operation: 80 mW (typ)
- Comon data input and output, three state outputs
- Capable of battery backup operation
- Directry TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access time	Package
HM66205L-85	85 ns	600-mil 32-pin DIP
HM66205L-10	100 ns	
HM66205L-12	120 ns	

Pin Arrangement



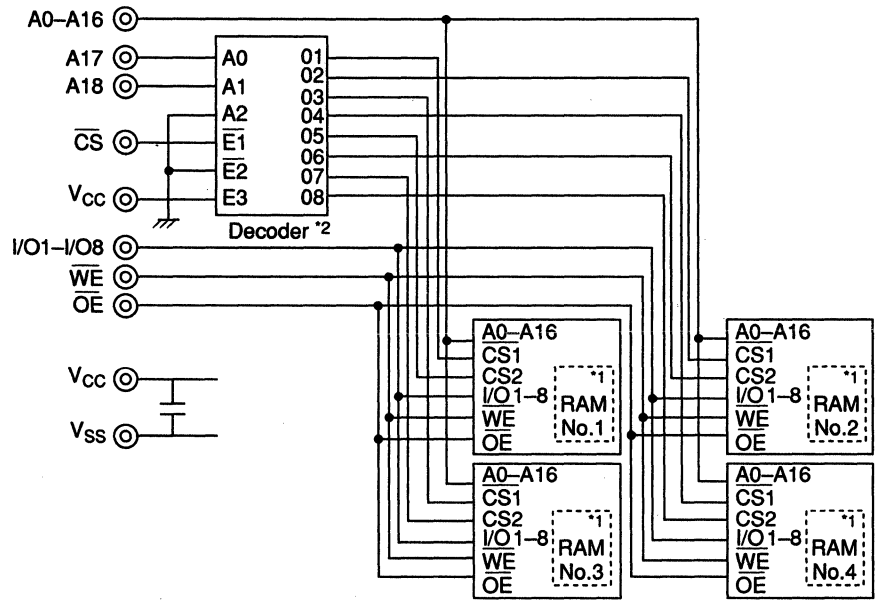
(Top view)

Pin Description

Pin name	Function
A0 – A18	Address
I/O1 – I/O8	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

7

Block Diagram



Notes: 1. RAM No.1–No. 4: HM628128LT
2. CMOS Decoder: HD74ACT138FP

Truth Table

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Ref. cycle
Not selected (Power down)	H	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note: X = Don't care (H or L)

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.3*1	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns.

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DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage currentent	$\|I_{LI}\|$	—	—	8	µA	Vin = V_{SS} to V_{CC}
Output leakage currentent	$\|I_{LO}\|$	—	—	8	µA	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH} or $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC	I_{CC}	—	19	46	mA	$\overline{CS}$ = V_{IL}, others V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
Average operating power supply current (1)	I_{CC1}	—	48	89	mA	Min cycle, duty = 100% $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, others V_{IH}/V_{IL}
Average operating power supply current (2)	I_{CC2}	—	16	36	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V, V_{IH} = V_{CC} − 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC	I_{SB}	—	4	12	mA	$\overline{CS}$ = V_{IH}
Standby power supply current (1)	I_{SB1}	—	8	400	µA	Vin ≥ 0 V $\overline{CS}$ = V_{CC} − 0.2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions	Notes
Input capacitance (1)	Cin1	—	45	pF	Vin = 0 V	A0 – A16, $\overline{WE}$, $\overline{OE}$
Input capacitance (2)	Cin2	—	45	pF	Vin = 0 V	A17 – A18, $\overline{CS}$
Input/output capacitance	$C_{I/O}$	—	50	pF	$V_{I/O}$ = 0 V	I/O1 – I/O8

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

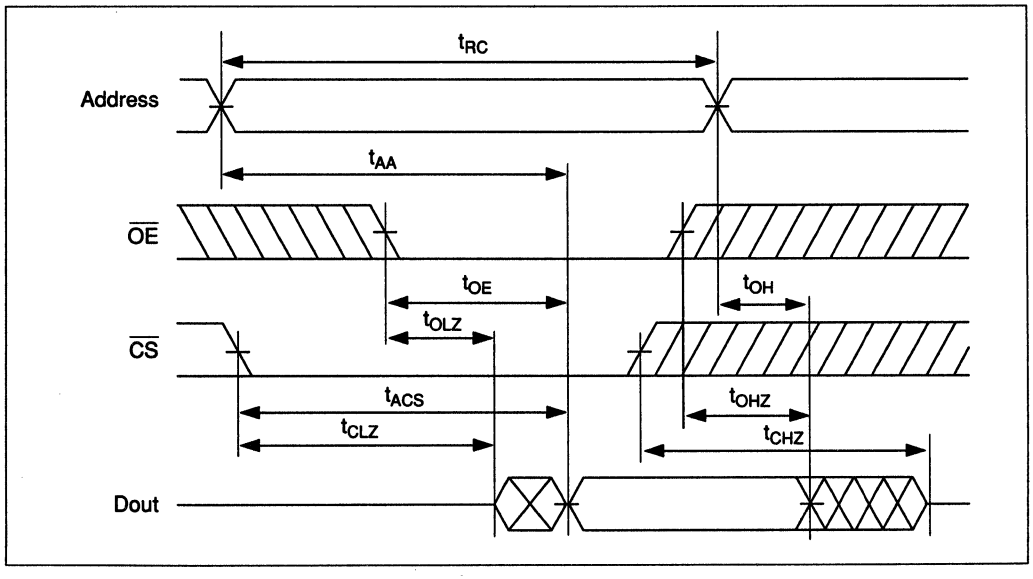
Test Condition

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5 V
- Output load: 1 TTL Gate and CL = 100 pF (Including scope and jig)

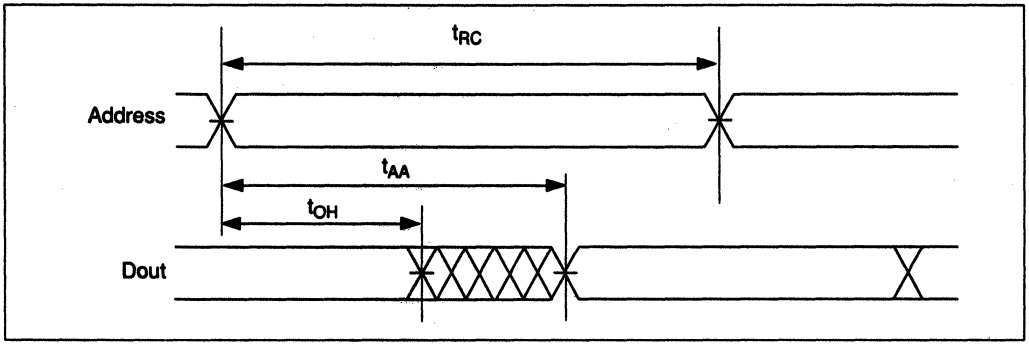
Read Cycle

		HM66205L-85		HM66205L-10		HM66205L-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	85	—	100	—	120	ns
Chip select access time	t_{ACS}	—	85	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	45	—	50	—	60	ns
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	ns
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	0	45	ns
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	45	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns

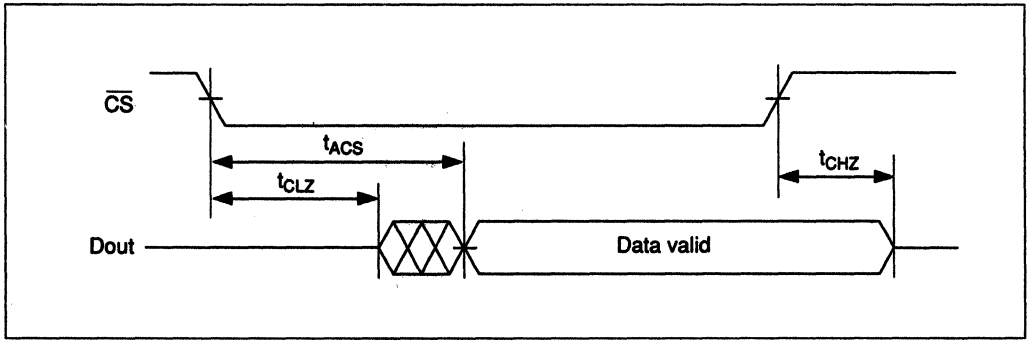
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1, *2, *4



Read Timing Waveform (3) *1, *3, *4

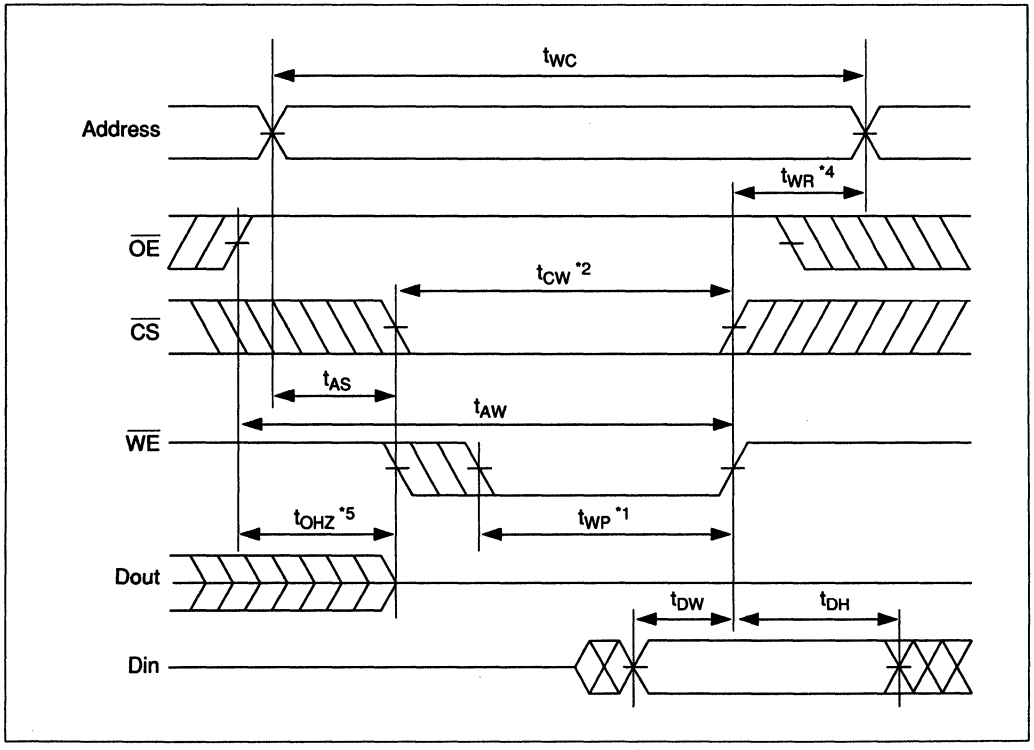


Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address should be valid prior to or coinsident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$

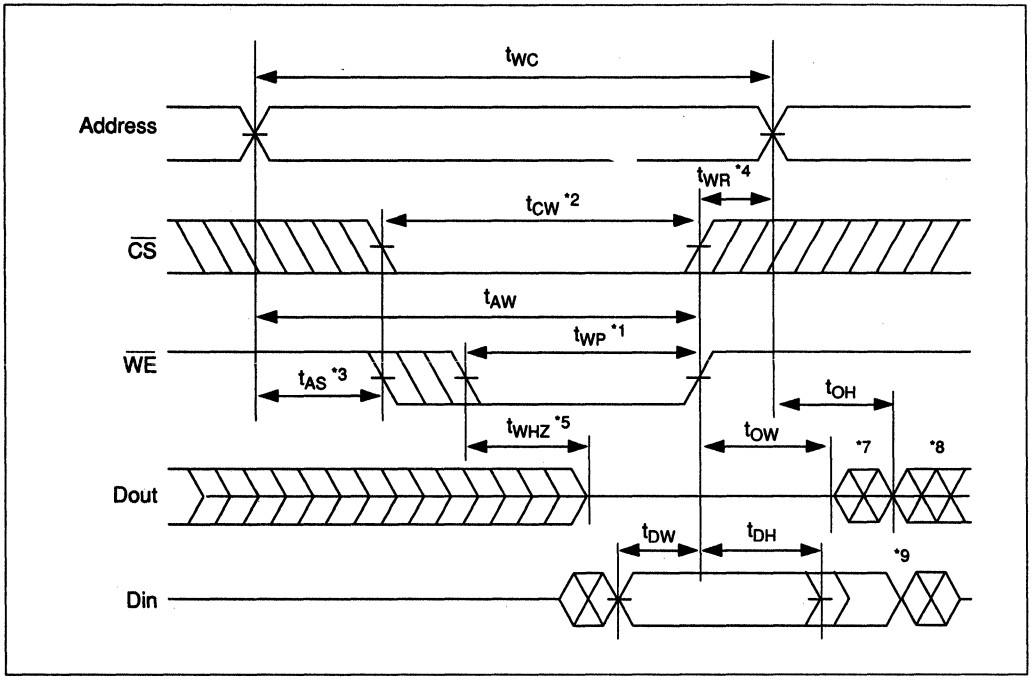
Write Cycle

Parameter	Symbol	HM66205L-85 Min	HM66205L-85 Max	HM66205L-10 Min	HM66205L-10 Max	HM66205L-12 Min	HM66205L-12 Max	Unit
Write cycle time	t_{WC}	85	—	100	—	120	—	ns
Chip selection to end of write	t_{CW}	75	—	90	—	100	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address valid to end of write	t_{AW}	75	—	90	—	100	—	ns
Write pulse width	t_{WP}	65	—	75	—	85	—	ns
Write recovery	t_{WR}	5	—	5	—	10	—	ns
Write to output in high-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to write time overlap	t_{DW}	35	—	40	—	45	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) *5 ($\overline{OE}$ Low Fixed)

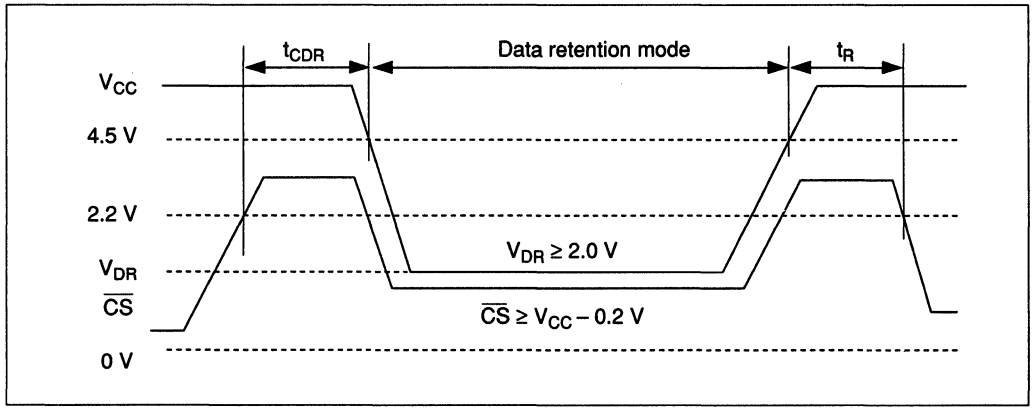


Notes:
1. A write occures during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state.
   The input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occures simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$).
6. Dout should be held in the phase of the written data during this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state.
   The input signals which are opposite to the output level should not be applied to I/O pins.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, A17•A18 $\geq V_{CC} - 0.2$ V, Vin $\geq$ 0 V
Data retention current	I_{CCDR}	—	4	200	µA	V_{CC} = 3.0 V, $\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq$ 0 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Low V_{CC} Data Retention Waveform



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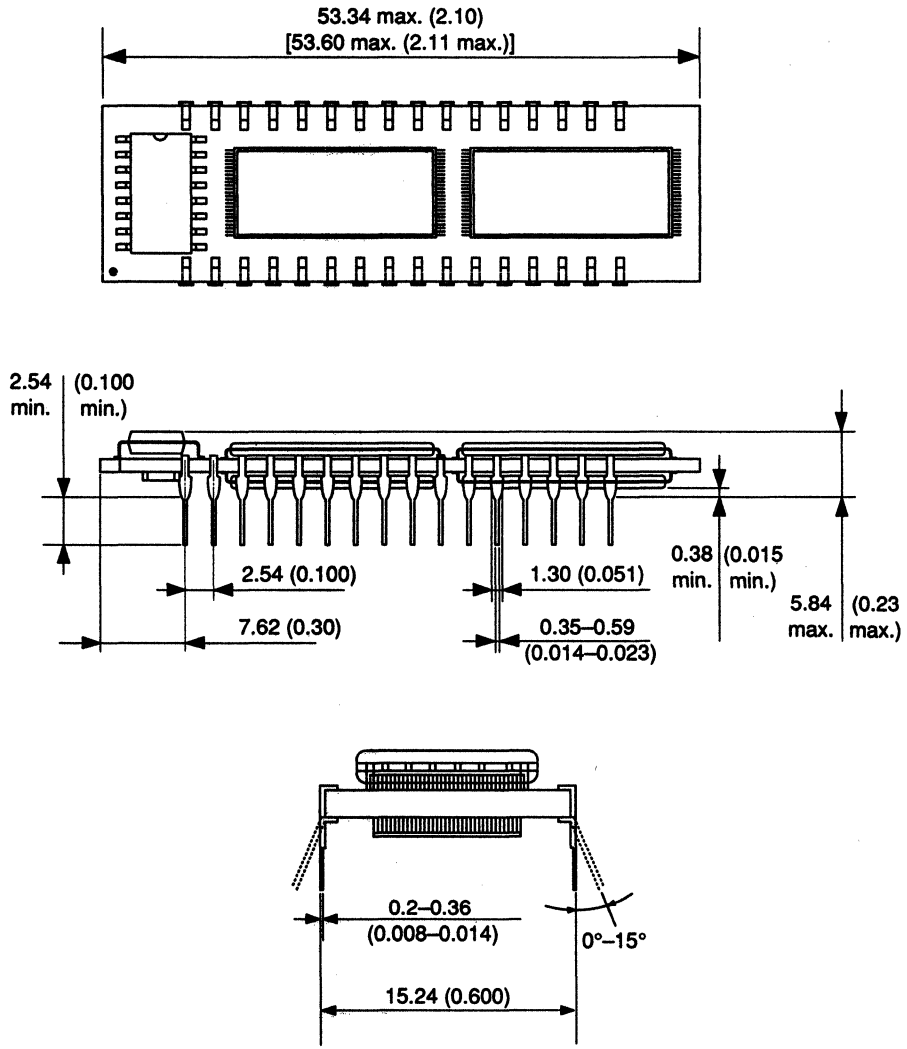
Package Dimension

Unit: mm (inch)



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