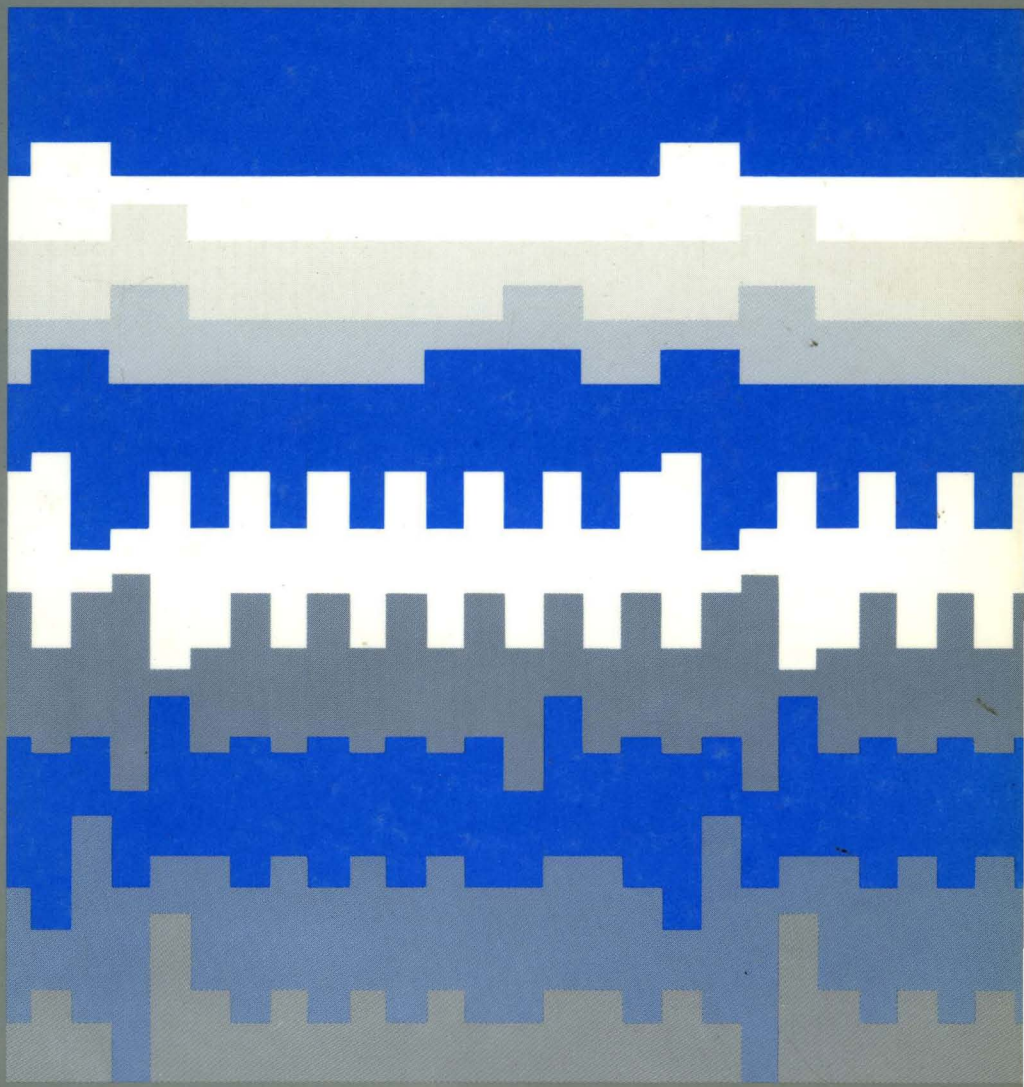
HITACHI®

LCD CONTROLLER/DRIVER LSI DATA BOOK



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M24T013

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Section One

General Information I

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Quick Reference Guide

Type		Column Driver							
Type Number		**HD44100H**	**HD66100F**	**HD61100A**	**HD61200**	**HD61104**	**HD61104A**	**HD66106F**	**HD66107T**
Power supply for internal circuits (V)		5	5	5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		11	6	17	17	26	28	37	37
Power Dissipation (mW)		5	5	5	5	10	10	15	25
Operating Temperature (C)		-20 to +75*1	-20 to +75*1	-20 to +75*1	-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75
Memory	ROM (bit)	–	–	–	–	–	–	–	–
	RAM (bit)	–	–	–	–	–	–	–	–
LCD Driver	Common	20	–	–	–	–	–	80	160
	Column	40 (20)	80	80	80	80	80	80	160
Instruction Set		–	–	–	–	–	–	–	–
Operation Frequency (MHz)		0.4	1	2.5	2.5	3.5	3.5	6	8
Duty		Static-1/32	Static-1/16	Static-1/100	1/32-1/128	1/64-1/200	1/64-1/240	1/100-1/480	1/100-1/480
Package		FP-60	FP-100	FP-100	FP-100	FP-100	FP-100 TFP-100	FP-100	192pin TCP

Type		Column Driver (RAM)				Column Driver (TFT)	
Type Number		**HD44102CH**	**HD61102**	**HD61202**	**HD66108T**	**HD66300T**	**HD66310T**
Power supply for internal circuits (V)		5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		11	15.5	17	15	15	23
Power Dissipation (mW)		5	5	5	5	160	100
Operating Temperature (°C)		-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75*2 (-20 to +65)
Memory	ROM (bit)	–	–	–	–	–	–
	RAM (bit)	200×8	512×8	512×8	165×65	–	–
LCD Driver	Common	–	–	–	0~65	120	160
	Column	50	64	64	100~165	–	–
Instruction Set		6	7	7	7	–	–
Operation Frequency (MHz)		0.28	0.4	0.4	4	4.8	12/15
Duty		1/8,1/12, 1/16,1/24, 1/32	Static-1/64	1/48,1/64, 1/96,1/128	1/32,1/34, 1/36,1/48, 1/50,1/64, 1/66	–	–
Package		FP-80	FP-100	FP-100	208pin TCP	156pin TCP	236pin TCP

*1 -40 to +85°C (Special request). Please contact Hitachi agents.
*2 -20 to +75°C in 12 MHz Version, -20 to +65°C in 15 MHz Version.
*3 Under development

Quick Reference Guide

Type		Segment Display			
Type Number		**HD61602**	**HD61603**	**HD61604**	**HD61605**
Power supply for internal circuits (V)		3 to 5	3 to 5	3 to 5	3 to 5
Power supply for LCD Drive Circuit (V)		5	5	5	5
Power Dissipation (mW)		0.5	0.5	0.5	0.5
Operating Temperature (°C)		−20 to +75*1	−20 to +75*1	−20 to +75*1	−20 to +75*1
Memory	ROM (bit)	–	–	–	–
	RAM (bit)	204	64	204	64
LCD Driver	Common	4	1	4	1
	Column	51	64	51	64
Instruction Set		4	4	4	4
Operation Frequency (MHz)		0.52	0.52	0.52	0.52
Duty		Static, 1/2, 1/3, 1/4	Static	Static, 1/2, 1/3, 1/4	Static
Package		FP-80, FP-80A TFP-80*2	FP-80	FP-80	FP-80

*1 -40 to +85°C (Special request). Please contact Hitachi agents.
*2 Under development

Type		Common Driver					
Type Number		**HD44103CH**	**HD44105H**	**HD61103A**	**HD61203**	**HD61105**	**HD61105A**
Power supply for internal circuits (V)		5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		11	11	17	17	26	28
Power Dissipation (mW)		4.4	4.4	5	5	5	5
Operating Temperature (°C)		−20 to +75	−20 to +75	−20 to +75	−20 to +75	−20 to +75	−20 to +75
Memory	ROM (bit)	–	–	–	–	–	–
	RAM (bit)	–	–	–	–	–	–
LCD Driver	Common	20	32	64	64	80	80
	Column	–	–	–	–	–	–
Instruction Set		–	–	–	–	–	–
Operation Frequency (MHz)		1	1	2.5	2.5	0.1	0.1
Duty		1/8, 1/12, 1/16, 1/24, 1/32	1/8, 1/12, 1/32, 1/48	Static-1/10, 1/64	1/32-1/128	1/64-1/200	1/64-1/240
Package		FP-60	FP-60	FP-100	FP-100	FP-100	FP-100 TFP-100

*1 -40 to +85°C (Special request). Please contact Hitachi agents.
*2 Under development

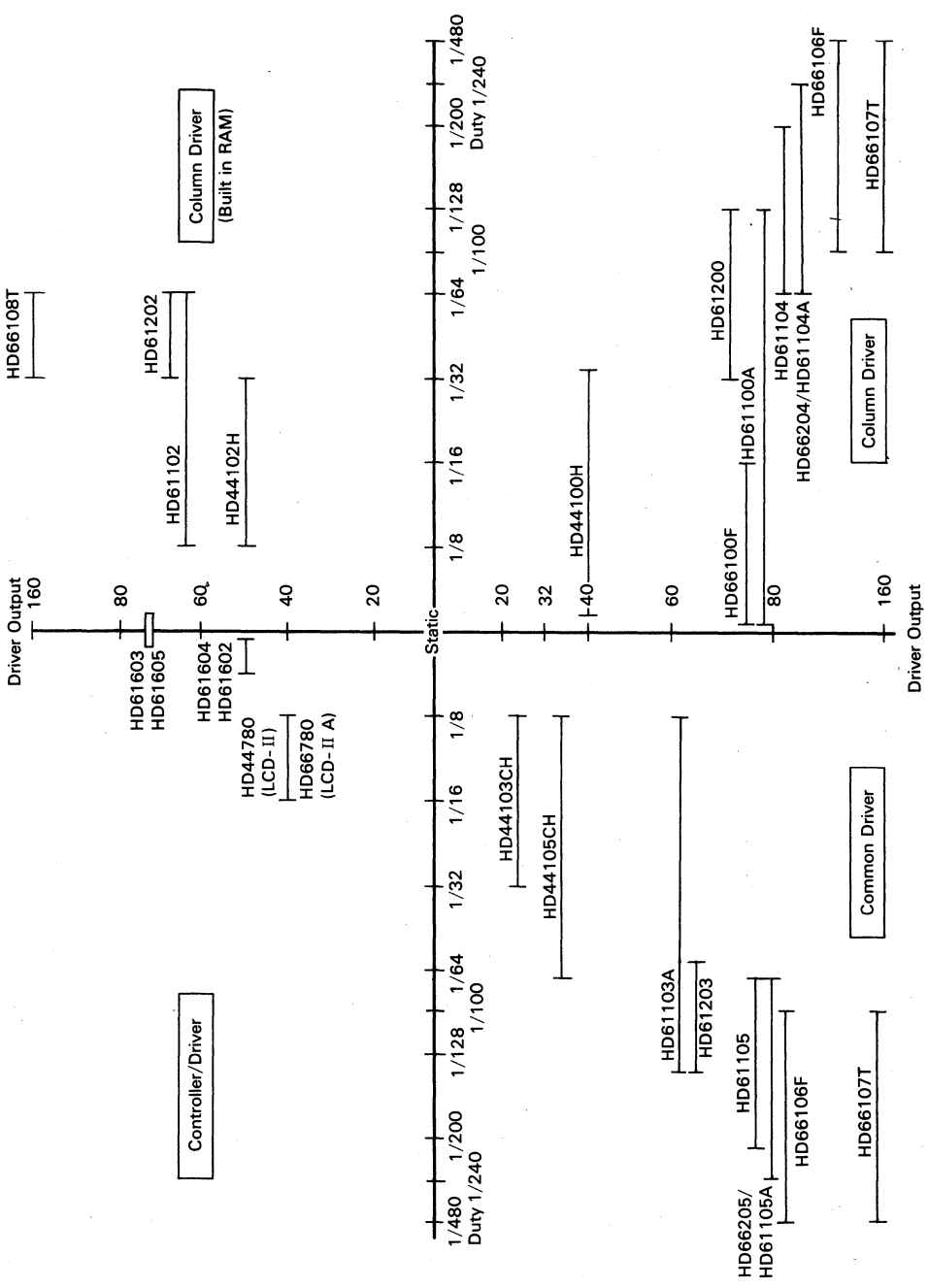
Type		Character Display			Graphic Display				
Type Number		HD43160AH	HD44780 (LCD-II)	HD66780 (LCD-IIA)	HD61830	HD61830B	HD63845F HD64645F HD64646FS LCTC	HD66840F HD66841F LVIC	HD66850 CLINE
Power supply for internal circuits (V)		5	5	5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		–	11	5	–	–	–	–	–
Power Dissipation (mW)		10	2	2	30	50	50	250	500
Operating Temperature (°C)		−20 to +75	−20 to +75*1	−20 to +75	−20 to +75	−20 to +75*1	−20 to +75	−20 to +75	−20 to +75
Memory	ROM (bit)	6420	7200	12000	7360	7360	–	–	–
	RAM (bit)	80×8	80×8, 64×8	80×8, 64×8	–	–	–	–	9762
LCD Driver	Common	–	16	16	–	–	–	–	–
	Column	–	40	40	–	–	–	–	–
Instruction Set		6	11	11	12	12	15	16/24	63
Operation Frequency (MHz)		0.25/0.375	0.25	0.25	1.1	2.4	10	30	32
Duty		1/8,1/12, 1/16	1/8,1/11, 1/16	1/8,1/11, 1/16	Static 1/128	Static 1/128	Static 1/512	Static 1/1024	1/480
Package		FP-54	FP-80, FP-80A TFP-80*2	FP-80A FP-80B	FP-60	FP-60	FP-80, FP-80B	FP-100A	FP-136

*1 -40 to +85°C (Special request). Please contact Hitachi agents.
*2 Under development

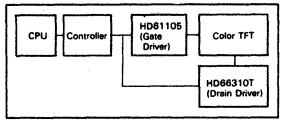
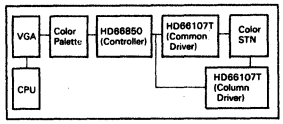
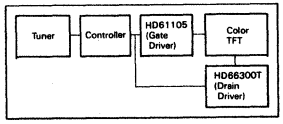
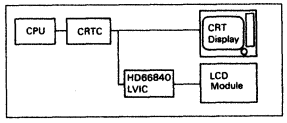
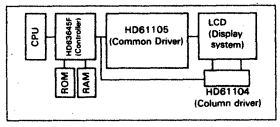
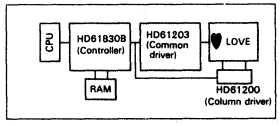
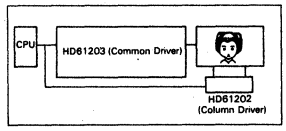
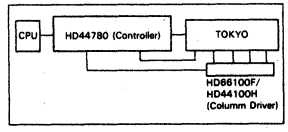
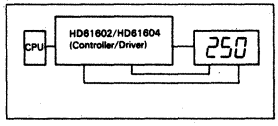
Type Number Order

Type	Function	Reference Page
HD43160AH	LCD Controller	100
HD44100H	LCD Driver with 40 Channel Output	77
HD44102CH	LCD Column Driver with 50 Channel Output	216
HD44103CH	LCD Common Driver with 20 Channel Output	239
HD44105H	LCD Common Driver with 32 Channel Output	247
HD44780 LCD-II	LCD Controller/Driver	114
HD6110A	LCD Column Driver with 80 Channel Output	256
HD61102	LCD Column Driver with 64 Channel Output	268
HD61103A	LCD Common Driver with 64 Channel Output	296
HD61104	LCD Column Driver with 80 Channel Output	320
HD61104A	LCD Column Driver with 80 Channel Output	320
HD61105	LCD Common Driver with 80 Channel Output	332
HD61105A	LCD Common Driver with 80 Channel Output	332
HD61200	LCD Column Driver with 80 Channel Output	350
HD61202	LCD Column Driver with 64 Channel Output	363
HD61203	LCD Common Driver with 64 Channel Output	394
HD61602	Segment Display Type LCD Driver	778
HD61603	Segment Display Type LCD Driver	778
HD61604	Segment Display Type LCD Driver	807
HD61605	Segment Display Type LCD Driver	807
HD61830 LCTC	LCD Timing Controller	413
HD61830B LCTC	LCD Timing Controller	443
HD63645F LCTC	LCD Timing Controller	466
HD64645F LCTC	LCD Timing Controller	466
HD64646FS LCTC	LCD Timing Controller	506
HD66100F	LCD Driver with 80 Channel Output	87
HD66106F	LCD Column/Common Driver with 80 Channel Output	516
HD66107T	LCD Column/Common Driver with 160 Channel Output	531
HD66108T	Graphic LCD Controller/Driver	551
HD66110T	Column Driver	916
HD66204	LCD Column Driver with 80 Channel Output	931
HD66205	LCD Common Driver with 80 Channel Output	945
HD66214T	Micro-TAB 80-Channel Column Driver	959
HD66214TL	Micro-TAB 80-Channel Column Driver	959
HD66300T	TFT Alalog Column Driver	833
HD66310T	TFT Digital Column Driver	894
HD66702 LCD-II	Dot Matrix Liquid Crystal Display Controller and Driver	975
HD66780 LCD-IIA	LCD Controller/Driver	167
HD66840F LVIC	LCD Video Interface Controller	604
HD66841F LVIC-II	LCD Video Interface Controller	652
HD66850F CLINE	Color LCD Interface Engine	708

Selection Guide



Hitachi LCD Driver System

Type	Reference Figure	Screen Size (max)	Lineup	Application
TFT Full Color System		(800×3)×520 dots	HD66310T(Drain) HD61105(Gate) HD66205(Gate)	Personal Computer Terminal Workstation Navigation System
STN Full Color System		(720×3)×480 dots	HD66850F(Controller) HD66107T (Column, Common)	Personal Computer Terminal Work-station
Color LCD-TV System		720×480 dots	HD66300T(Drain) HD61105(Gate) HD66205(Gate)	LCD-TV Portable Video
Video to LCD converter		720×512 dots	HD66840F, HD66841F HD66106F(Driver) HD66107T(Driver), HD61104(Column)/ 61105(Common) HD66204(Column)/ 66205(Common)	Personal Computer, Terminal, OHP
Display System for CRT Compatible		640×400 dots	HD63645F/64645F/ 64646FS(Controller) HD61104(Column)/ 61105(Common) HD66204(Column)/ 66205(Common) HD66106F(Driver)	Personal Computer, Word-processor, Terminal
Graphic Display System		Character 80×16 Graphic 480×128 dots	HD61100A(Column), HD61830B(Controller) HD61200(Column) HD61103A(Common), HD61203(Common)	Laptop Computer, Facsimile, Telex, Copy machine
Graphic Display System (Bitmap)		480×128 dots	HD44102CH(Column)/ 61102(Column) HD44103CH(Common) HD61202(Column) HD44105H(Common)/ 61103A(Common) HD61203(Common) HD66108T (Column/Common)	Laptop Computer, Handy Word-processor, Toy
Character Display System		40 Characters ×2 Columns 80 Characters ×1 Column	HD44780(LCD-II) (Controller/Driver) HD66780(LCD-II A) (Controller/Driver) HD44100H(Column) HD66100F(Column)	Electrical Typewriter, Multifunction Telephone, Handy Terminal
Segment Display System		25 Digits ×1 Column	HD61602 (Controller/Driver) HD61604 (Controller/Driver) HD61603 (Controller/Driver) HD61605 (Controller/Driver)	ECR, Measurement System, Telephone Industrial Measurement System

Application

Character and Graphic Display

1 character=7 × 8 dot (15 × 7 dot + cursor)

<table>
<tr><th>Character
Line</th><th>8</th><th>16</th><th>20</th><th>24</th><th>32</th><th>40</th><th>Over 80</th></tr>
<tr><td>1</td><td rowspan="5"></td><td colspan="5" rowspan="2">HD66100F</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td><td colspan="4" rowspan="2">HD44100H</td></tr>
<tr><td>4</td></tr>
<tr><td>6 to 8</td><td colspan="5"></td></tr>
<tr><td>12 to 15</td><td colspan="7">HD61200 (Column) + HD61203 (Common)</td></tr>
<tr><td>16 to 25</td><td colspan="7" rowspan="2">HD61104 (Column) + HD61105 (Common)
HD66204 (Column) + HD66205 (Common)
HD66106F, HD66107T</td></tr>
<tr><td>26 to 50</td></tr>
</table>

Graphic Display

<table>
<tr><th>Horizontal
Vertical</th><th>48</th><th>96</th><th>120</th><th>180</th><th>240</th><th>480</th><th>Over 640</th></tr>
<tr><td>16</td><td colspan="5" rowspan="4">HD61202 (Column) + HD61203 (Common)</td><td colspan="2" rowspan="4"></td></tr>
<tr><td>32</td></tr>
<tr><td>48</td></tr>
<tr><td>64</td></tr>
<tr><td>128</td><td colspan="5" rowspan="3">HD61104 (Column) + HD61105 (Common)
HD66204 (Column) + HD66205 (Common)
HD66106F, HD66107T</td></tr>
<tr><td>400</td></tr>
<tr><td>Over 400</td></tr>
</table>

Note: Applications on this page are only examples, and this combination of devices is not the best.

Differences Between Products

1. HD66100F and HD44100H

	HD66100F	HD44100H
LCD drive circuits	80	20×2
Power supply for internal logic (V)	3 to 6	4.5 to 11
Display duty	Static to 1/16	Static to 1/32
Package	100 pin plastic QFP	60 pin plastic QFP

2. HD61100A and HD61200

		HD61100A	HD61200
LCD drive circuits	common	–	–
	column	80	80
Display duty		static to 1/128	1/32 to 1/128
Power supply for LCD drive circuits (V)		0 to 17	8 to 17
Power supply limits of LCD driver circuit voltage		V_{CC} to V_{EE} (no limit)	shown in figures below

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y_1 to Y_{80} is specified under the following conditions:
$V_{CC}-V_{EE}=17V$
$V1L=V1R$, $V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$
$V2L=V2R$, $V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$

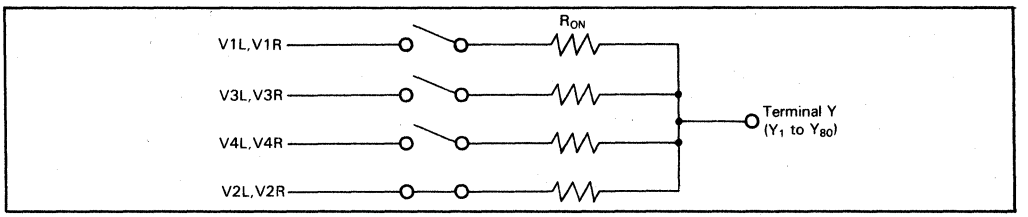


Figure 1 Resistance between Y ard V Terminals

The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice the ΔV depends on power supply voltage $V_{CC}-V_{EE}$.

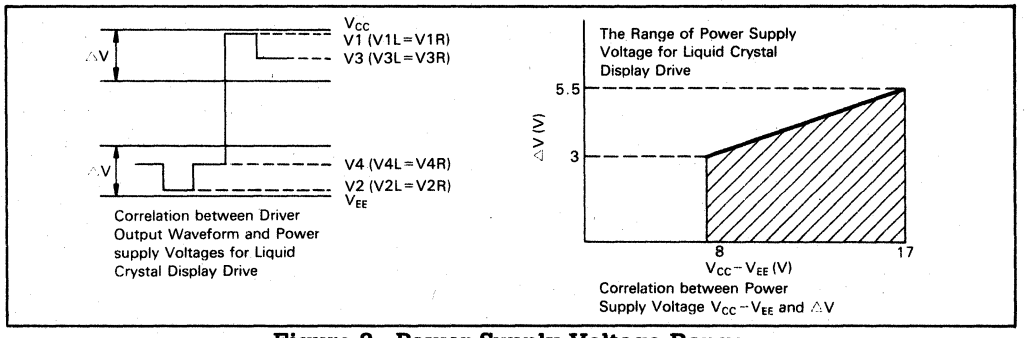


Figure 2 Power Supply Voltage Range

3. HD66100F and HD61100A

		HD66100F	HD61100A
LCD driver circuits	common	–	–
	column	80	80
Power supply for LCD drive circuits (V)		3 to 6	5.5 to 17.0
Display duty		static to 1/16	static to 1/128
Operating frequency (MHz)		1.0 MHz (max)	2.5 MHz (max)
Data fetch method		Shift	Latch
Package		100 pin Plastic QFP (FP-100)	100 pin plastic QFP (FP-100)

4. HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal	External
Operating frequency (MHz)	1.1 MHz	2.4 MHz
Display duty	static to 1/128	static to 1/128
Programmable screen size (Max)	64×240 dots (1/64 duty)	128×480 dots (1/64 duty)
Other	pin 6:C pin 7:R pin 9:CPO	pin 6:$\overline{CE}$ pin 7:$\overline{OE}$ pin 9:NC
Package Marking	Ⓐ	Ⓑ

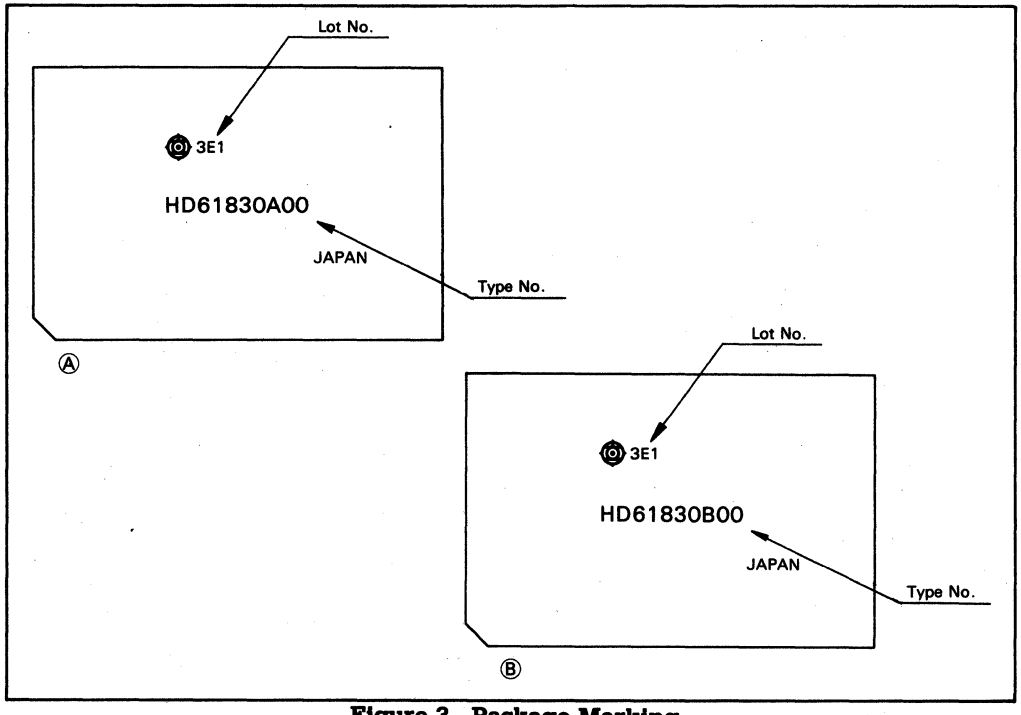


Figure 3 Package Marking

5. HD61102 and HD61202

	HD61102	HD61202
Display duty	static to 1/64	1/32 to 1/64
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 15.5	8 to 17
Power supply limits of LCD driver circuits voltage	V_{CC} to V_{EE} (no limit)	shown in following figures
Pin 88	DY (output)	NC (no connection)
Absolute maximum rating of V_{EE} (V)	$V_{CC}-17.0$ to $V_{CC}+0.3$	$V_{CC}-19.0$ to $V_{CC}+0.3$

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y_1 to Y_{64} is specified under the following conditions:

$V_{CC}-V_{EE}=15V$
$V1L=V1R$, $V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$
$V2L=V2R$, $V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$

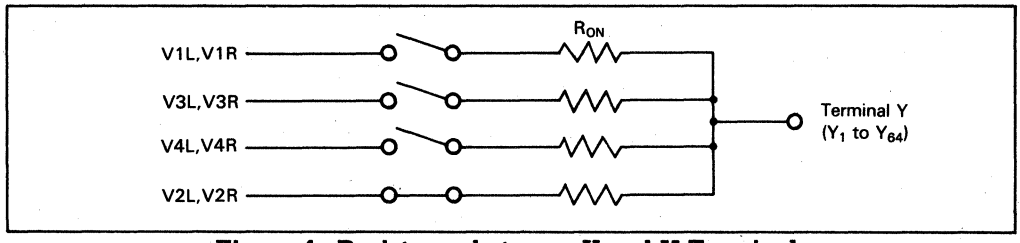


Figure 4 Resistance between Y and V Terminals

The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.

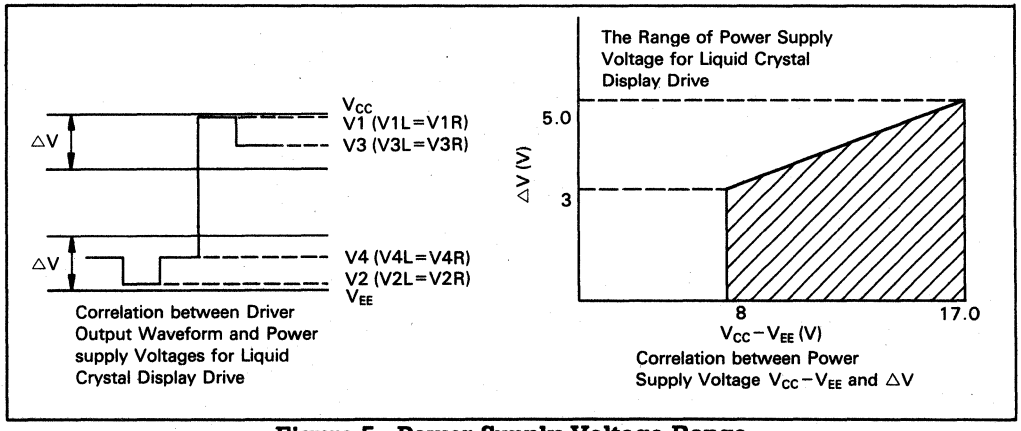


Figure 5 Power Supply Voltage Range

6. HD61103A and HD61203

	HD61103A	HD61203
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 17	8 to 17
Power supply limits of LCD drive circuits voltage	V_{CC} to V_{EE} (no limit)	shown in figures below
Output terminal	shown in following figure 4	shown in following figure 5

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:

$V_{CC}-V_{EE}=17V$
$V1L=V1R$, $V6L=V6R=V_{CC}-1/7\ (V_{CC}-V_{EE})$
$V2L=V2R$, $V5L=V5R=V_{EE}+1/7\ (V_{CC}-V_{EE})$

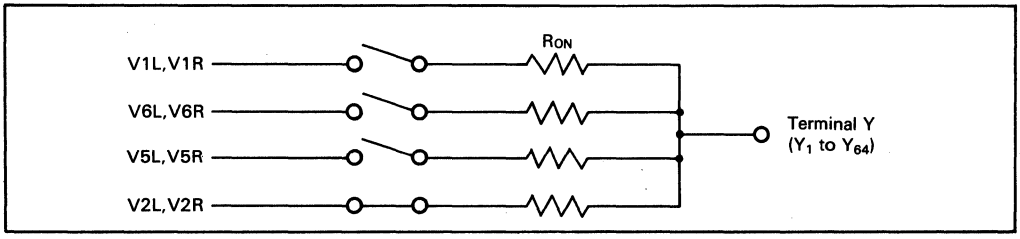


Figure 6 Resistance between Y and V Terminals

Here is a description of the range of power supply voltage for liquid crystal display drive. Apply postive voltage to V1L=V1R and V6L=V6R and negative voltage to V2L=V2R and V5L=V5R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.

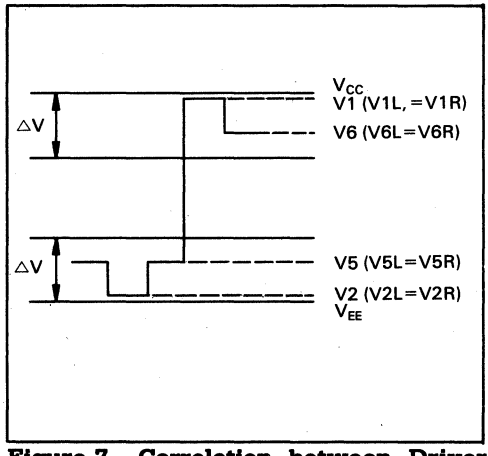


Figure 7 Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

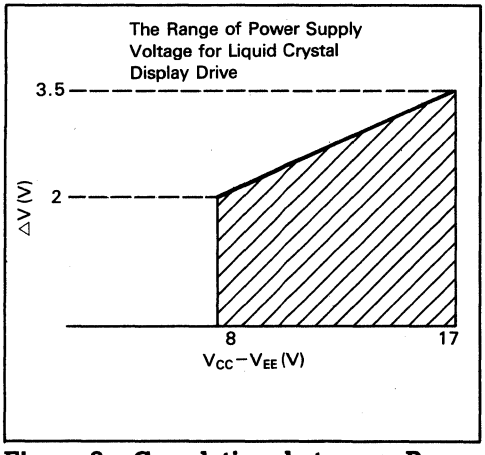


Figure 8 Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

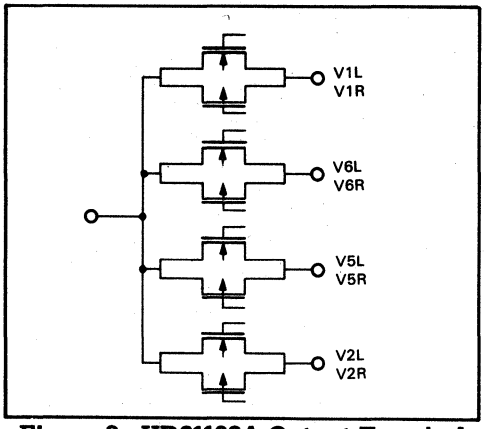


Figure 9 HD61103A Output Terminal

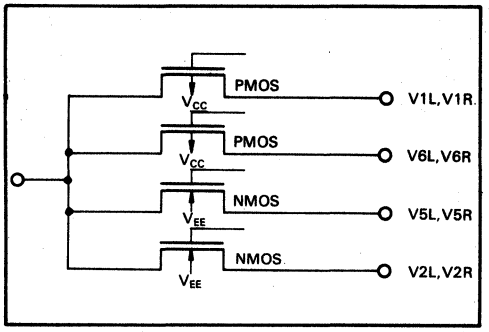


Figure 10 HD61203 Output Terminal

7. HD61602, HD61603, HD61604, and HD61605

		HD61602	HD61603	HD61604	HD61605
Power supply (V_{DD})		2.2~5.5V	2.2~5.5V	4.5~5.5V	4.5~5.5V
Instruction word		8 bits × 2	4 bits × 4	8 bits × 2	4 bits × 4
LCD power supply circuit		Yes	–	–	–
Segment terminals		51	64	51	64
Display size frame frequency (fosc=100 kHz)	Static	6 digits + 3 marks 33Hz	8 digits 33Hz	6 digits + 3 marks 98Hz	8 digits 98Hz
	1/2 duty	12 digits + 6 marks 65Hz	–	12 digits + 6 marks 195Hz	–
	1/3 duty	17 digits 208Hz	–	17 digits 521Hz	–
	1/4 duty	25 digits + 4 marks 223Hz	–	25 digits + 4 marks 781Hz	–

8. HD44780 LCD-II and HD66780 LCD-II A

Item		LCD-II (HD44780)	LCD-II A (HD66780)	Note
Display RAM (Maximum number of display characters)		80 bytes (80 characters)	←	
Character generator ROM (kinds of characters)		7200 bits 192 characters 5×7;160 characters 5×10;32 characters	12000 bits 240 characters 5×10;240 Characters	
Character generator RAM (Number of characters)		64 bytes (8 characters)	←	
LCD driving terminals (Maximum number of display characters/ unit)		16 COMs 40 SEGs (16 characters)	←	
Character font (with a cursor)		5×8 dots 5×11 dots	←	
Multiplexing duty ratio		1/8, 1/11, 1/16	Same as LCD-II	
*1LCD driving voltage	1/4 bias	3.0 to 11 (V)	3.0 to V_{CC} (V)	V_{CC} to V_5
	1/5 bias	4.6 to 11 (V)	3.0 to V_{CC} (V)	
*1LCD driving waveform		waveform A	waveform B	Shown following figures
*Bus timing		1, 1.5MHz	2MHz	
Instruction codes		11 instructions	←	
Power-on reset circuit		Yes	←	
Oscillator (Frequency)		Ceramic filter, Rf, external clock (250 kHz)	←	
Interface		HD44100H	HD44100H or HD66100F	
Package		FP-80, FP-80A, TFP-80*2	FP-80, FP-80A	

Note: *1 Indicates the modified items in LCD-II A.
*2 Under development

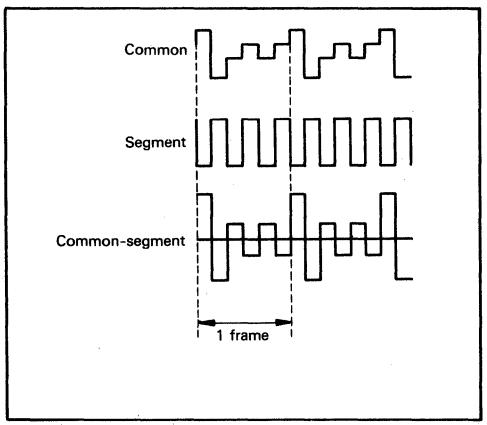


Figure 11 Waveform A (1/3 Duty, 1/3 Bias)

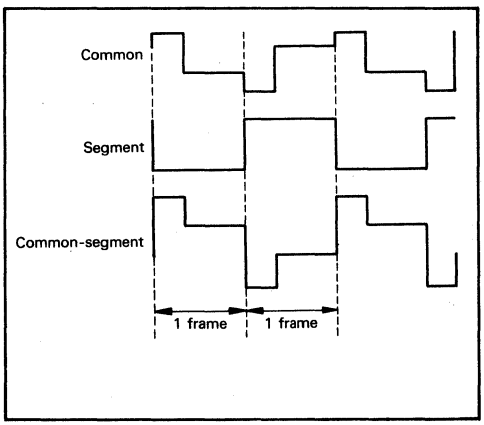


Figure 12 Waveform B (1/3 Duty, 1/3 Bias)

9. HD61104, HD61104A and HD66204

	HD61104	HD61104A	HD66204
LCD drive circuits	80	80	80
Data transfer rate (MHz)	3.5	3.5	8
Power supply for LCD drive circuits (V)	10 to 26	10 to 28	10 to 28
Display off function	No	No	Yes

10. HD61105, HD61105A and HD66205

	HD61105	HD61105A	HD66205
LCD drive circuits	80	80	80
Power supply for LCD drive circuits (V)	10 to 26	10 to 28	10 to 28
Display off function	No	No	Yes

11. HD66106F and HD61104

	HD66106F	HD61104
LCD drive circuits voltage	+14 to +35 (V_{LCD}-GND)	-10 to -26 (V_{CC}-V_{EE})
Display Duty	1/100 to 1/400	1/64 to 1/200
Operating frequency (MHz)	6.0 MHz	3.5 MHz
Function	column and common driver	column driver

12. HD66106F and HD66107T

	HD66106F	HD66107T
LCD drive circuits	80	160
Data transfer	4-bits	4-bits/8-bits
Operating frequency (MHz)	6	8
Power supply for LCD drive circuits	14 to 37	14 to 37
Packge	100-pin plastic QFP (FP-100A)	192-pin TAB

13. HD63645F, HD64645F and HD64646FS

	HD63645F	HD64645F	HD64646FS
CPU interface	68 family	80 family	80 family
Package	80-pin plastic QFP (FP-80)	80-pin plastic QFP (FP-80)	80-pin plastic QFP (FP-80A)
Other	–	–	HD64646 has another LCD drive interface in HD64645

14. HD66840F and HD66841F

	HD66840F	HD66841F
Frame-based thinning control	Each line	Each dot and each line
Display mode 16	Single screen Both sides X/Y driver Horizontal stripe	Dual screen One sides X/Y driver Vertical stripe
Gray-scale palette	No	8 registers

Section Two

General Information II

- TCP (Tape Carrier Package)
- Package Information
- Reliability and Quality Assurance
- Reliability Test Data of LCD Drivers
- Flat Plastic Package (QFP) Mounting Methods
- Liquid Crystal Driving Methods

TCP (Tape Carrier Package)

1 Overview

Hitachi is developing TCP-applied LCD driver LSIs in response to the following situation.

Because LCDs are improving yearly, they have become second only to CRTs in terms of screen size and display quality. At the same time, LCD driver LSIs have also been improving in terms of voltage-resistivity and the number of pins.

At present, LCD screens with a maximum of 640×480 dots has been put into practical use, matching the size of conventional high-definition CRT display screens. Availability of this screen size promotes the development and improvement of new application fields such as laptop personal computers, portable word processors, and the like.

In the light of the above, higher performance has been demanded of LCD driver LSIs, especially in regards to LCD driving voltage, operating speed, and the number of pins. In fact, certain manufacturers of portable devices employing LCDs demand 1-mm-thick packages having a relatively large number of pins.

TCP packages have the advantages of being able to allow extra thin mounting and less restricted design of connecting leads, while in contrast, conventional packages utilizing wire bonding methods such as QFP require a relatively large area for board mounting, thus preventing thin and high-density mounting.

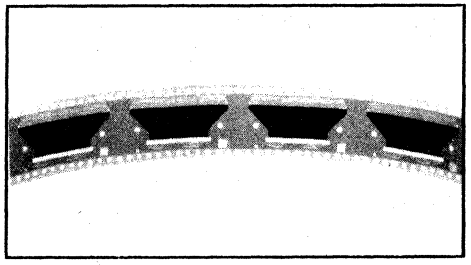
TCP packaging is also called "film carrier" since the wiring pattern for each product is formed continuously on a film-base tape.

TCP features are listed below.

- Great reduction in mounting size
- Increased number of pins for LSI devices
- Power-on burn-in possible

* TCP (Tape Carrier Package)

Photograph 1 shows the TCP tape exterior and figure 1 shows TCP structure.



Photograph 1 TCP Exterior

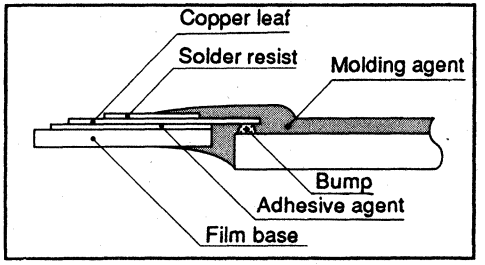


Figure 1 TCP Structure (Cross Section)

1.1 Bump Formation

Although LSI electrodes and package leads are wired with Au-wire bonding for QFP, Au bumps formed on LSI electrodes (Al pads) and inner leads prefabricated on tape are thermo-compressed and bonded together for TCP. This method is called "inner-lead bonding" or ILB for short.

Figure 2 shows the sequence for Au bump formation.

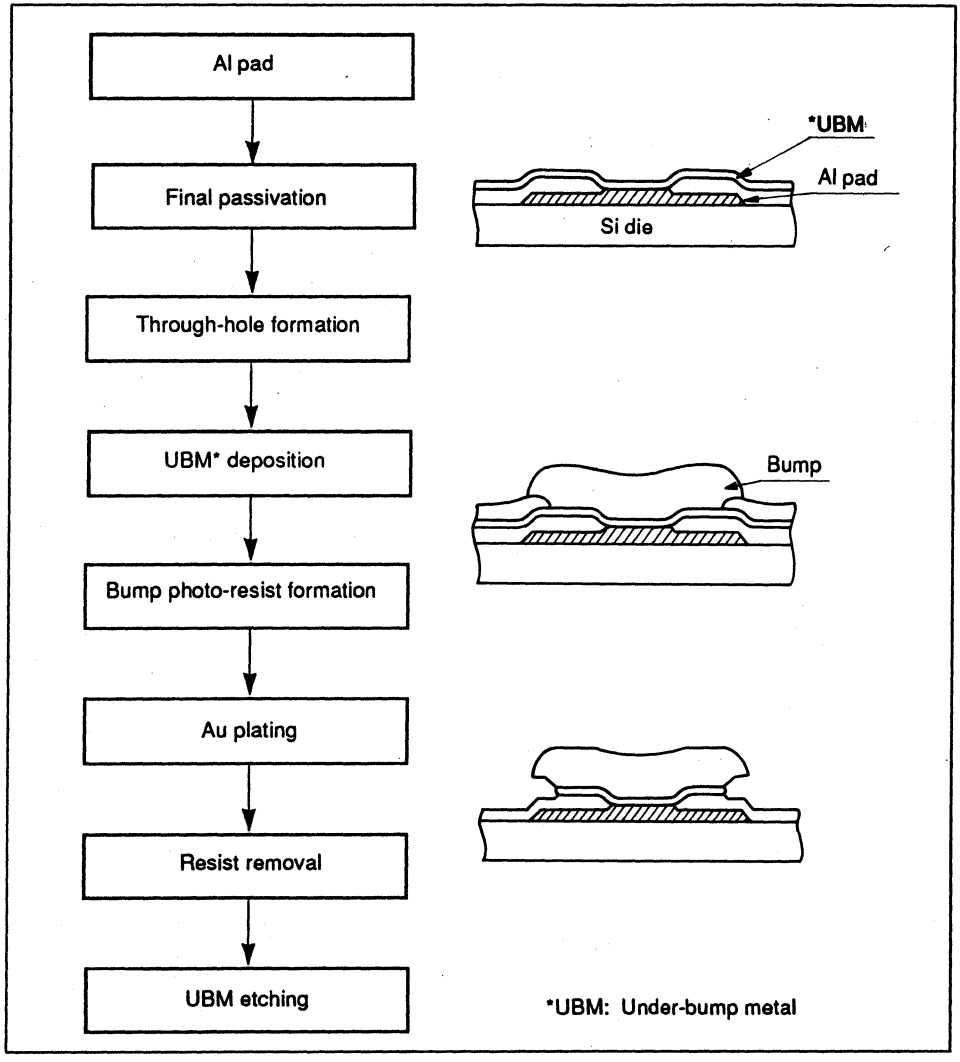


Figure 2 Au Bump Formation

1.2 Reliability Test Data

The result of the reliability test on TCP products are shown in table 1 through 3.

Table 1 HD66107T Reliability Test Result

Test item	Test condition	Result	Remarks
Operation at high temperature	Ta=125°C, V_{CC}=5.5 V t=1000 h	0/32	
Standing at high temperature	Ta=125°C, t=1000 h	0/22	
Standing at low temperature	Ta=–55°C, t=1000 h	0/22	
Standing at high temperature	Ta=65°C, RH=95%, t=1000 h	0/45	
PCT	Ta=121°C, RH=100%, t=60 h	0/22	
Temperature cycle	–40° to 85°C, 200 cycles	0/45	
Thermal shock	0° to 100°C, 15 cycles	0/22	
Solder heat resistance	260°C, 10 s	0/22	Only lead dipped

Table 2 HD61105T Reliability Test Result

Test item	Test condition	Result	Remarks
Operation at high temperature	Ta=125°C, V_{CC}=5.5 V t=1000 h	0/32	
Standing at high temperature	Ta=125°C, t=1000 h	0/22	
Standing at low temperature	Ta=–55°C, t=1000 h	0/22	
Standing at high temperature	Ta=65°C, RH=95%, t=1000 h	0/45	
PCT	Ta=121°C, RH=100%, t=60 h	0/22	
Temperature cycle	–40° to 85°C, 200 cycles	0/45	
Thermal shock	0°C to 100°C, 15 cycles	0/22	
Solder heat resistance	260°C, 10 s	0/22	Only lead dipped

Table 3 Common Reliability Test Results of TCP

Test item	Test condition	Result	Remarks
Solderability	230°C, 5 s, Rosin flux	0/11	
Solvent resistance	Isopropylalcohol, dipping for 10 min.	0/11	
Salt spray	5% NaCl aqueous solution, 35°C, t=24 h	0/22	
Tensile strength of terminal	2.5 kg/mm^2, 10 s, 1 cycle	0/11	Input lead only

2 Standard Product Specifications

2.1 Tape Design and Structure

(1) Tape components

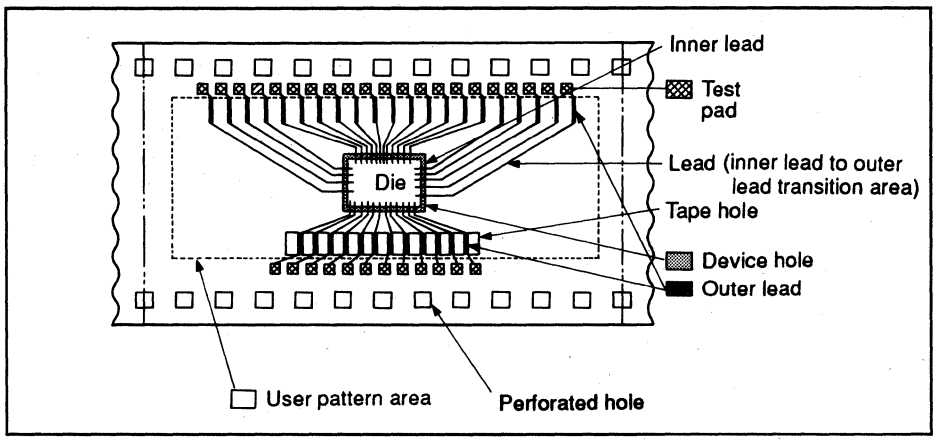


Figure 3 Tape Components

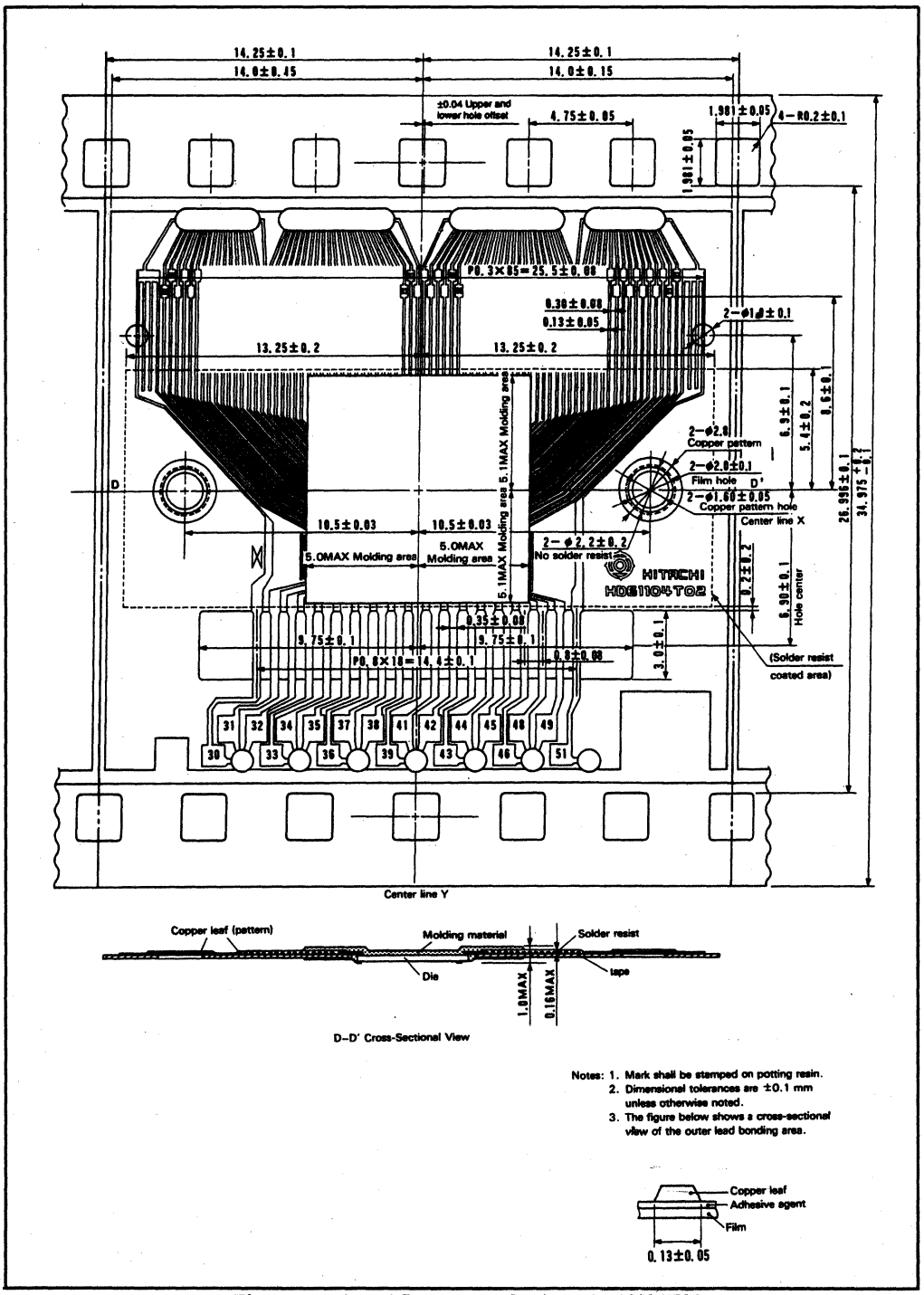
(2) Hitachi standard TCP product structure

Hitachi can provide the standard TCP products listed in table 4 immediately. Figures 4 to 11 show the structure of each TCP product.

Table 4 Hitachi Standard TCP Product Specifications

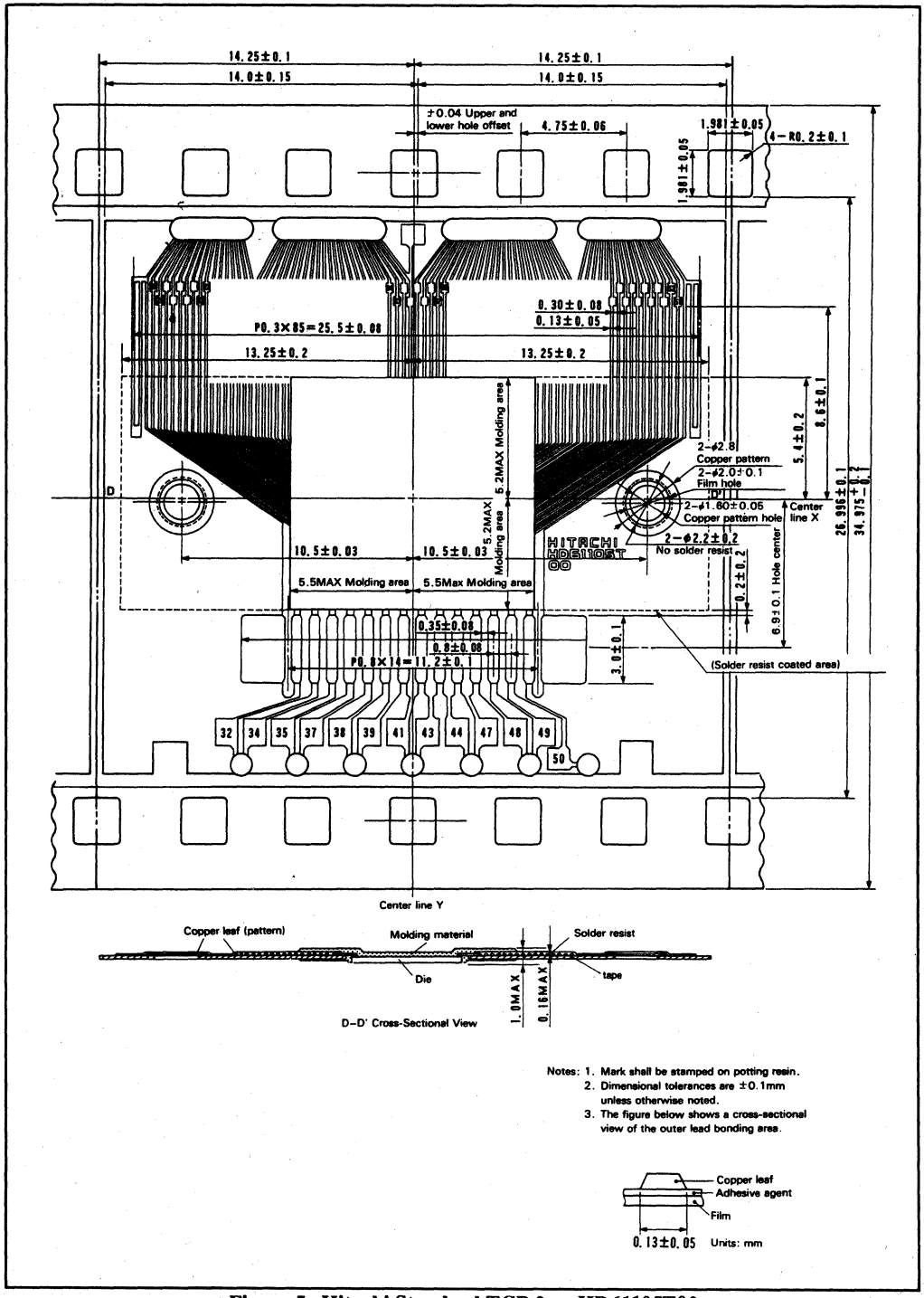
No.	Product	Base Chip	Function	No. of outputs	Outer Lead Pitch (μm)	Product Length*	Tape Thickness
1	HD61104T02	HD61104	Column LCD driver	80	300	6	125
2	HD61105T02	HD61105	Common LCD driver	80	300	6	125
3	HD66107T00	HD66107	LCD driver	160	280	12	75
4	HD66107T01			80	280	12	75
5	HD66107T11**			160	180	8	75
6	HD66107T12**			160	250	10	75
7	HD66108T00	HD66108	Graphic LCD driver	165	400	8	75
8	HD66300T00	HD66300	TFT analog driver	120	300	10	75
9	HD66310T00	HD66310	TFT digital driver	160	180	8	75

*: Number of perforations
**: Under development



Notes: 1. Mark shall be stamped on potting resin.
2. Dimensional tolerances are ±0.1 mm unless otherwise noted.
3. The figure below shows a cross-sectional view of the outer lead bonding area.

Figure 4 Hitachi Standard TCP 1 – HD61104T02 –



Notes: 1. Mark shall be stamped on potting resin.
2. Dimensional tolerances are ±0.1mm unless otherwise noted.
3. The figure below shows a cross-sectional view of the outer lead bonding area.

Figure 5 Hitachi Standard TCP 2 – HD61105T02 –

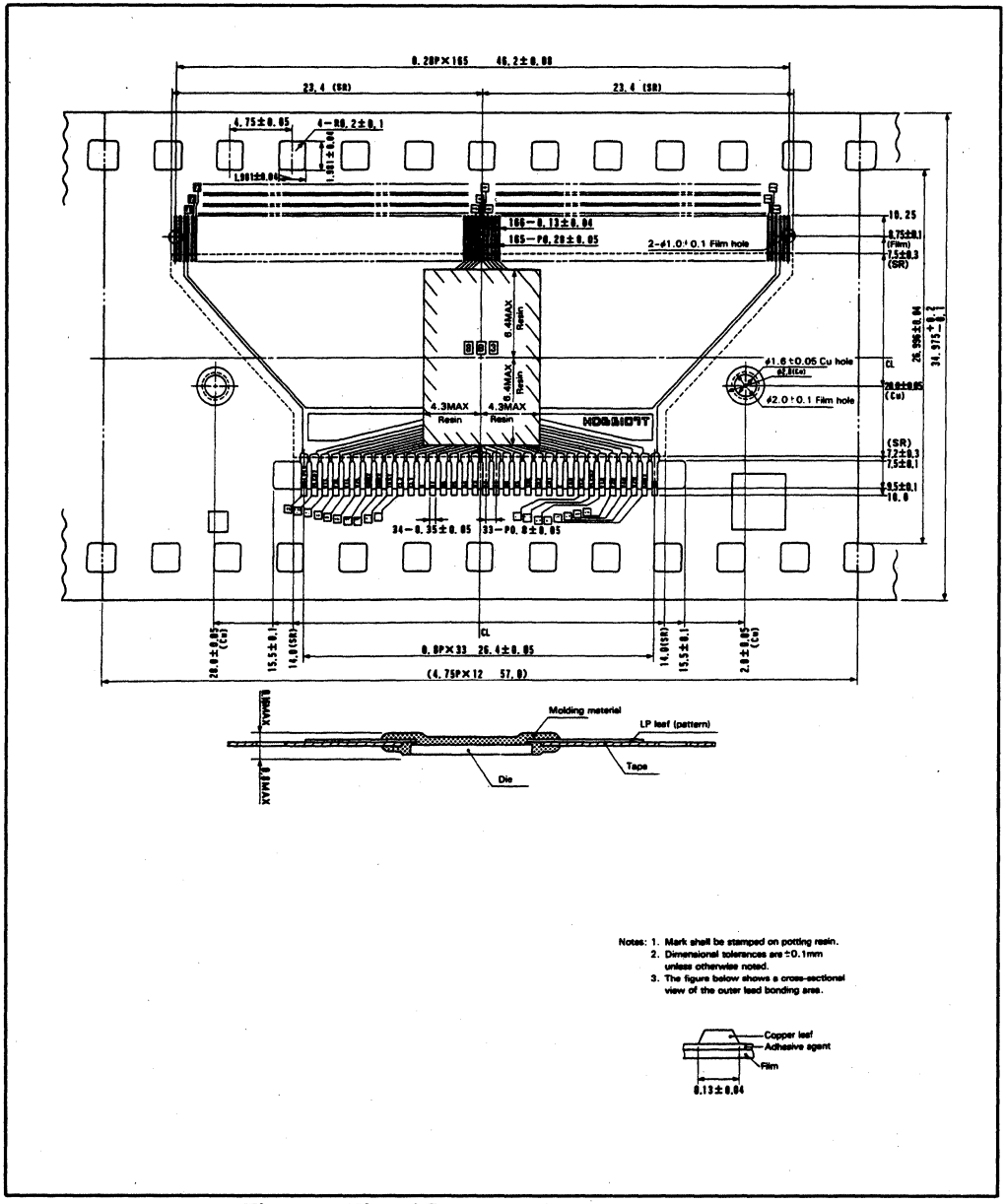


Figure 6 Hitachi Standard TCP 3 – HD66107T00 –

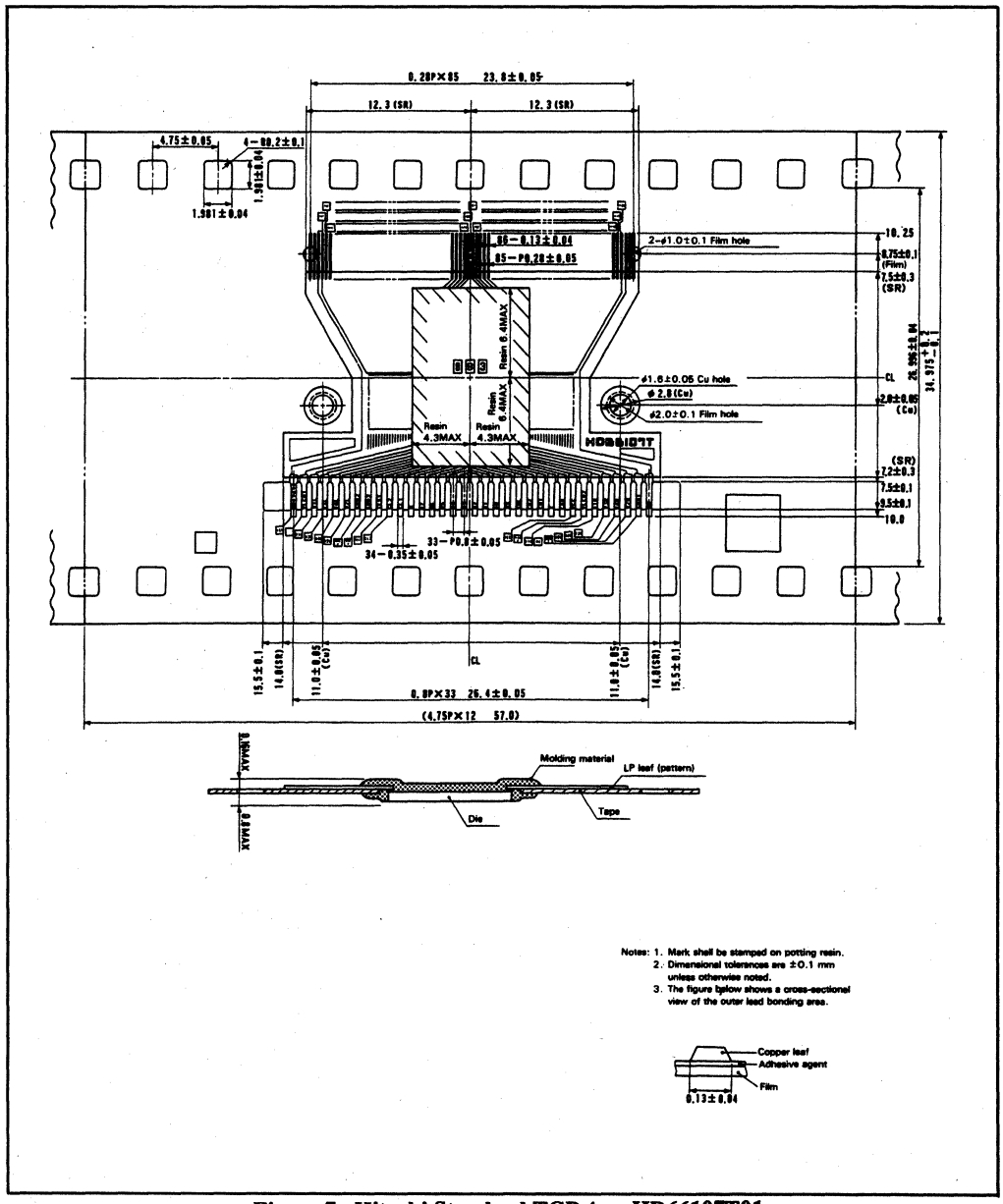


Figure 7 Hitachi Standard TCP 4 – HD66107T01 –

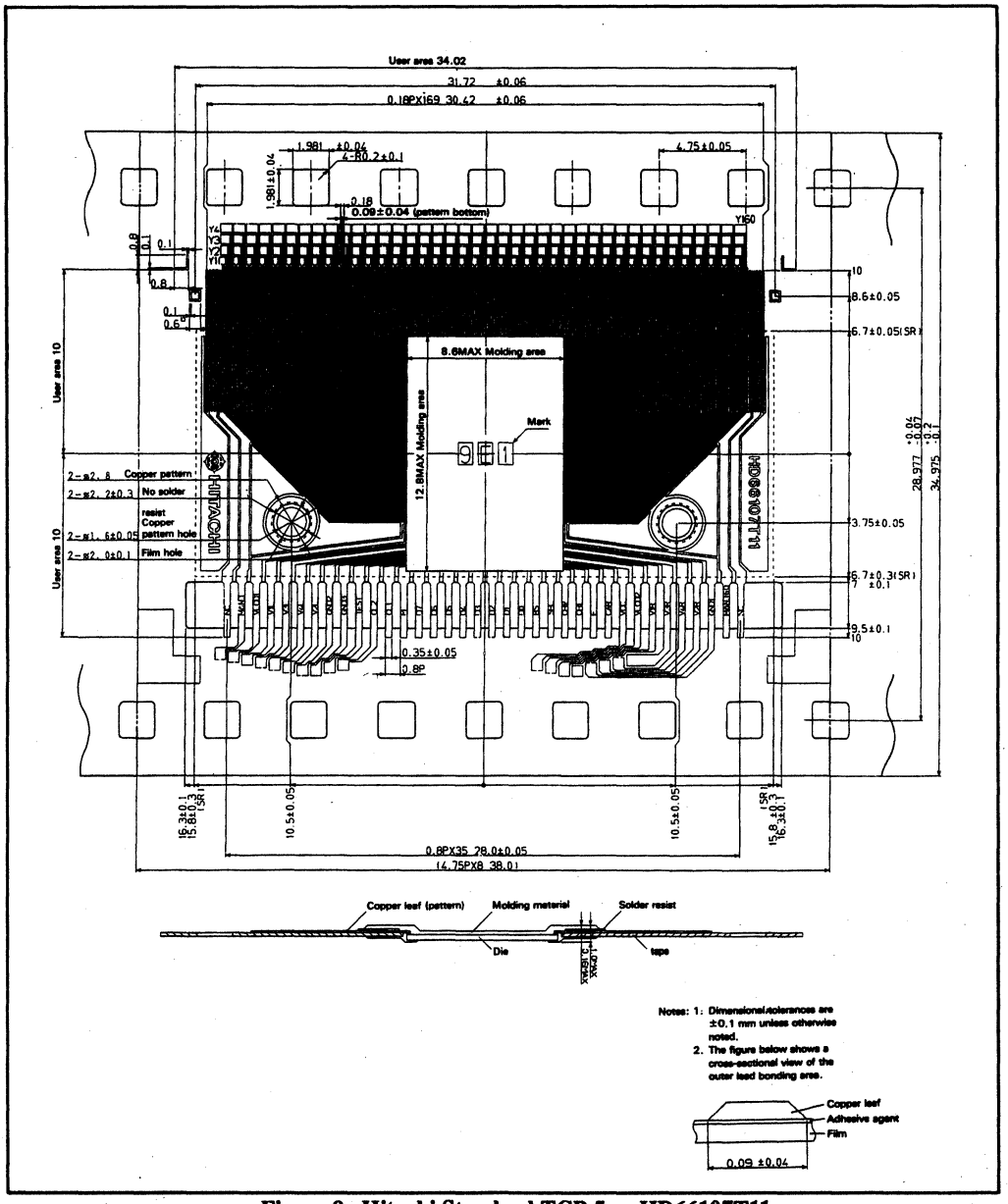


Figure 8 Hitachi Standard TCP 5 – HD66107T11 –

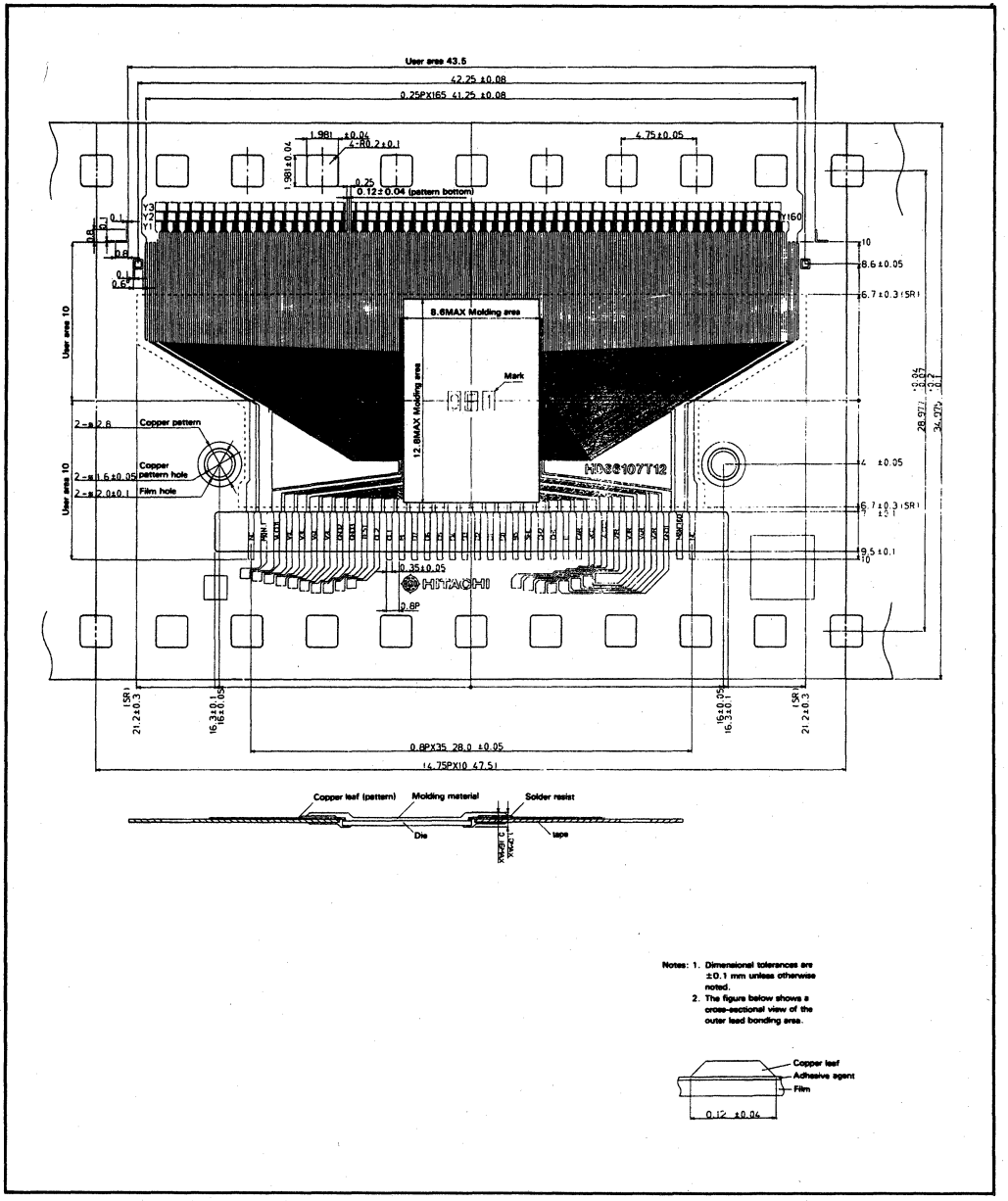


Figure 9 Hitachi Standard TCP 6 – HD66107T12 –

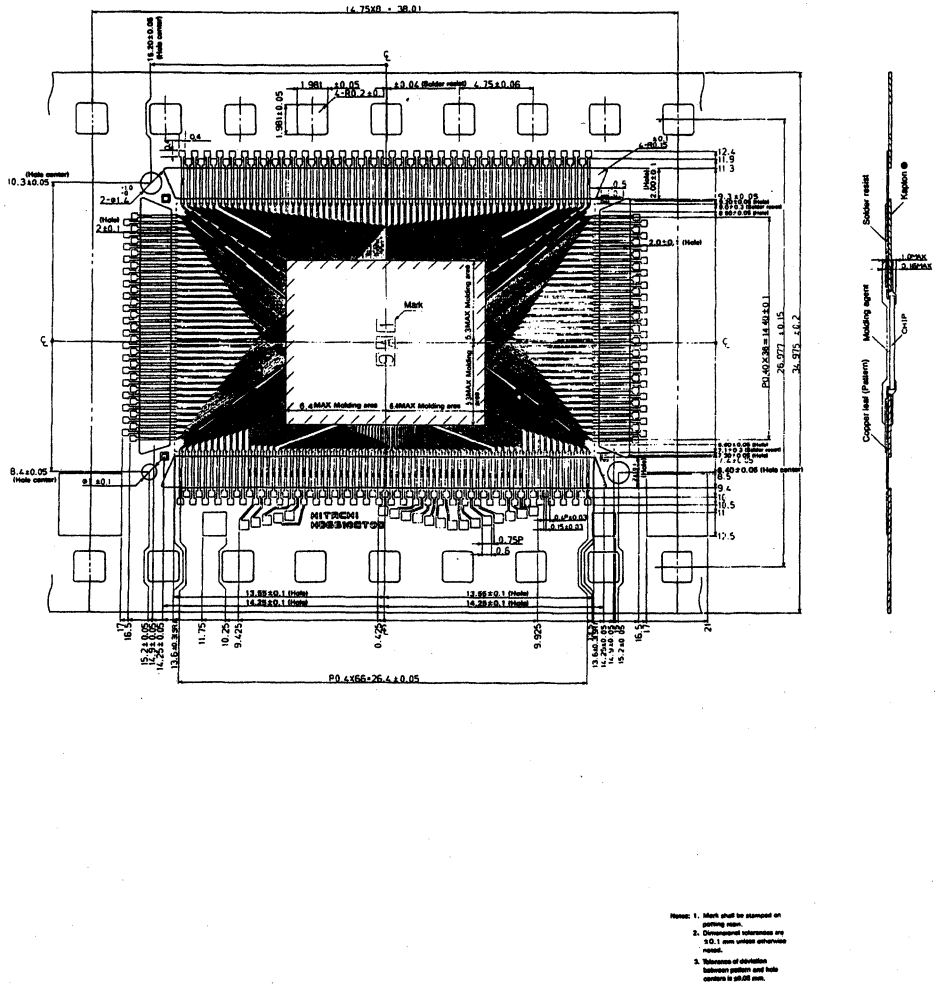


Figure 10 Hitachi Standard TCP 7 – HD66108T00 –

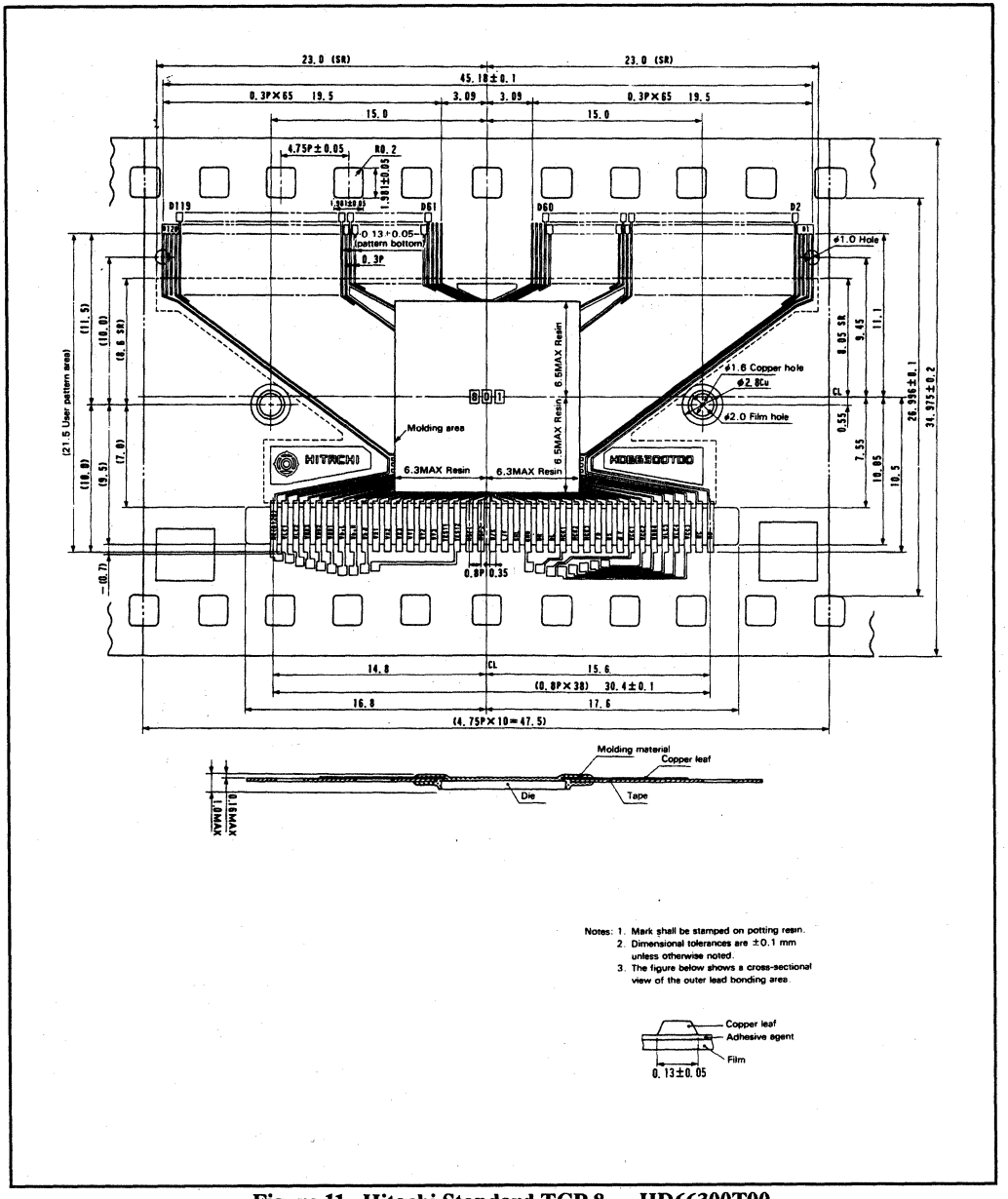


Figure 11 Hitachi Standard TCP 8 – HD66300T00 –

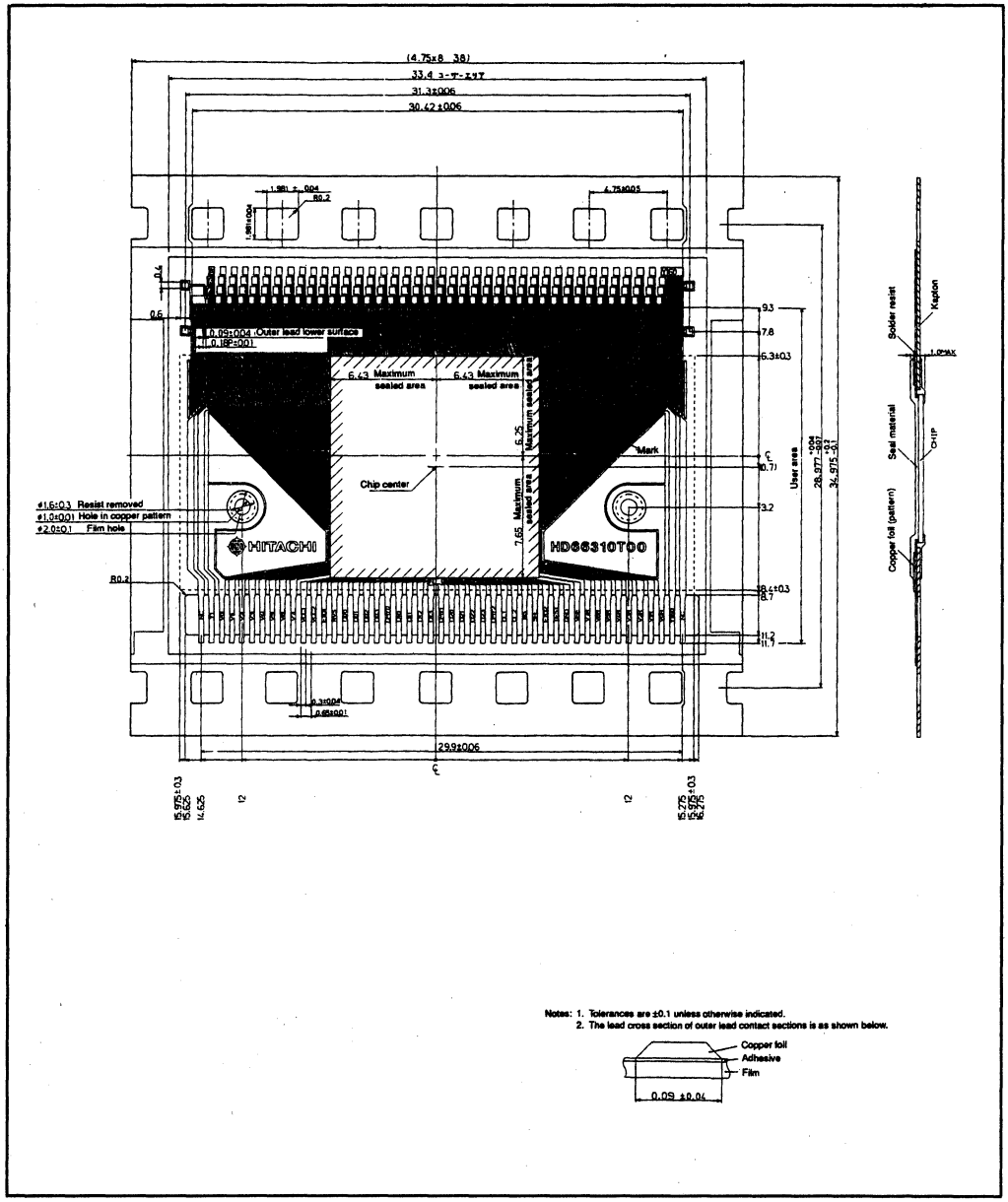


Figure 12 Hitachi Standard TCP 9 – HD66310T00 –

2.2 Product Delivery Specifications

Specifications for product delivery to customers is described below.

2.2.1 Tape Joint (Including Lead Tape Joint)

TCP tape is cut into strips for aging and other purposes, after which they are again joined together. Joint specifications are given below (figure 13).

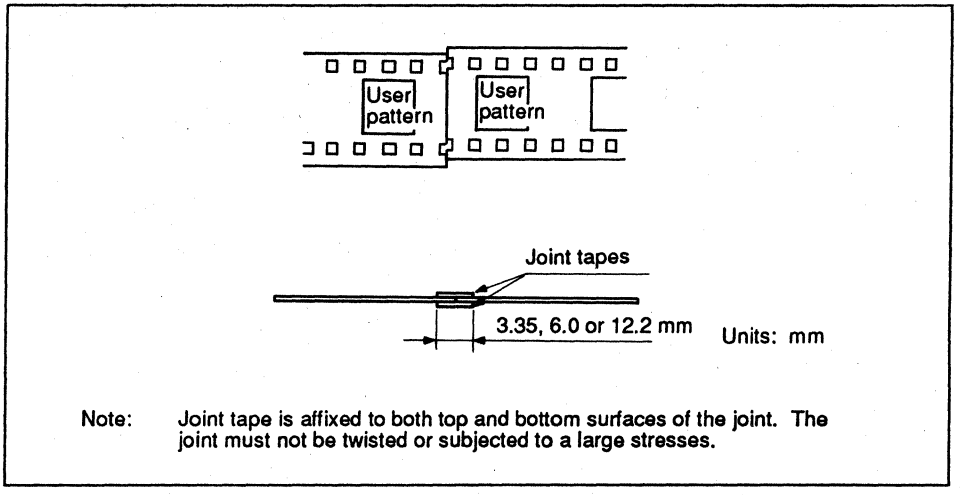


Figure 13 Tape Joint

2.2.2 Mark

Hitachi control code, made up of three or six digits, is marked on potting resin as shown in figure 14. The HD66108T00 is marked on top of the solder resist.

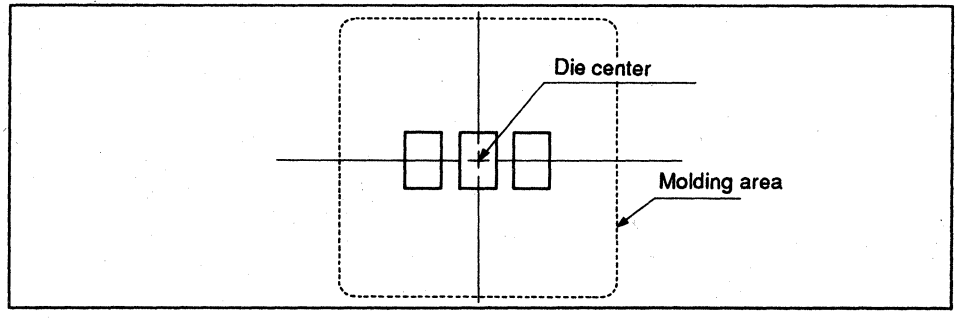


Figure 14 Mark Pattern

2.2.3 Packing

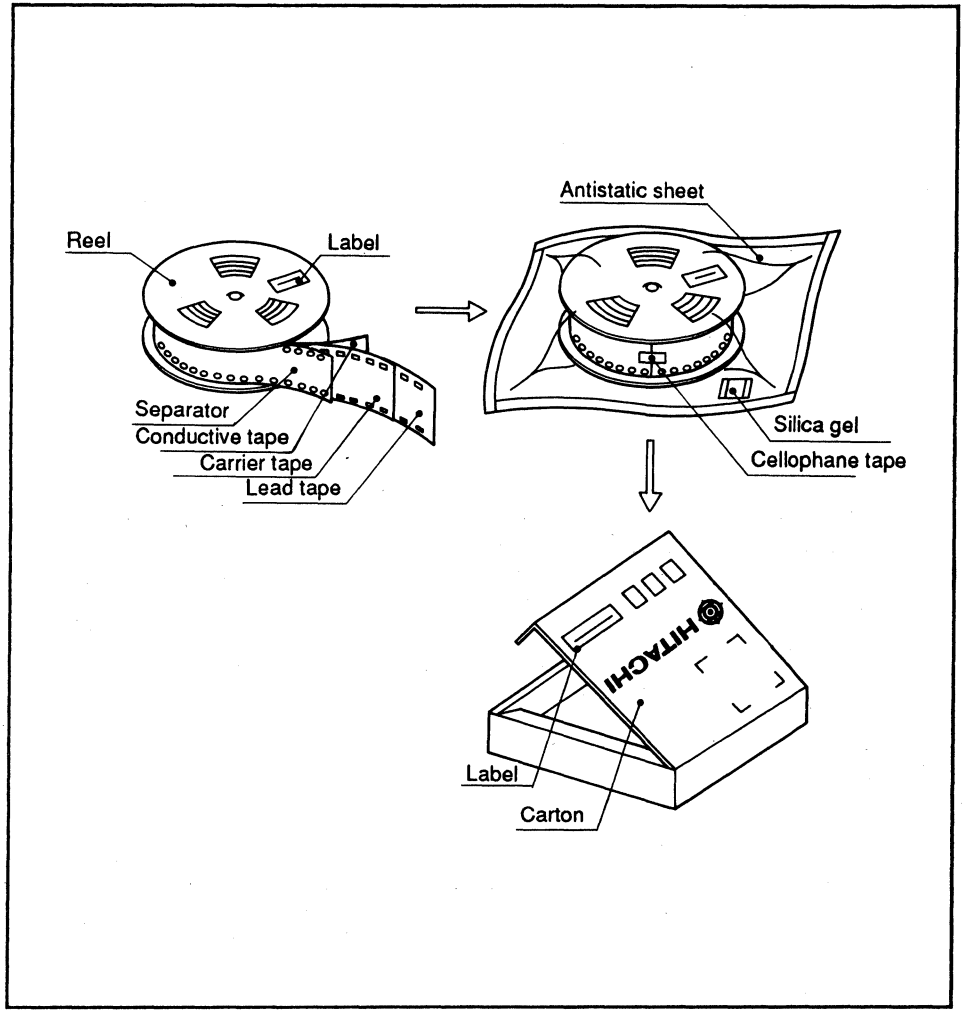


Figure 15 Packing

(1) Delivery

A reel wound with carrier tape is sealed in an opaque antistatic sheet with N2 and packed into a carton before delivery.

(2) Tape

I. Carrier tape: 40 m

II. Lead tape: 2+0/–1 m added to both ends of the carrier tape

III. Conductive tape: 40 m

IV. Separator: 40 m

V. Tape is wound with its pattern surface on the inside.

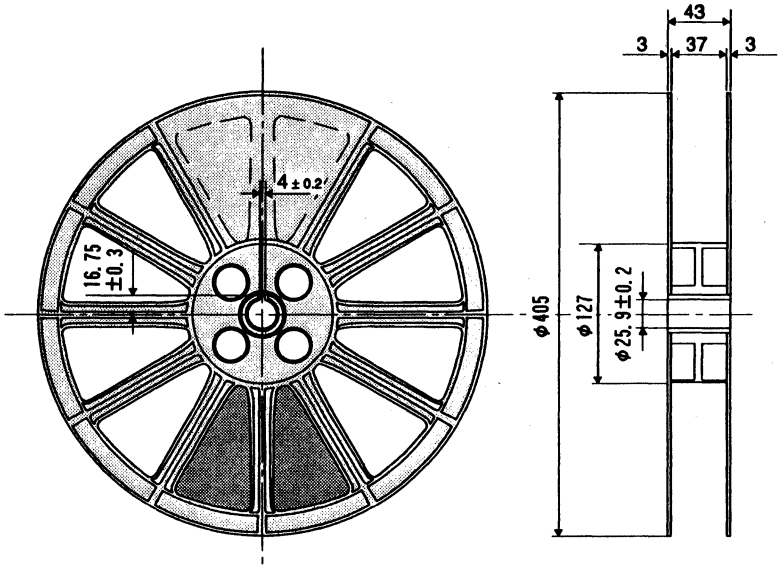
Note: The length of I, III, and IV may vary slightly depending on the number of products contained on the tape.

(3) Request for Recovery of Packing Material

Please return the separator, lead tape, and reel to us after using the TCP product.

Detailed return procedures will be advised by our Sales Department.

(3) Reel



Note: The shaft hole of the reel is slightly greater than the specified shaft size.

Unit: mm
Material: Styrole

Figure 16 Reel Dimensions

Note: LSIs dtermined defective during classification, assembly, or other processes are punched out.

2.2.4 Storage Conditions

(1) When storing in the original packing

Store in normal atmospheric conditions, and use within 6 months of delivery.

(2) Storage after opening

Storage in a nitrogen atmosphere with a dew point of –30°C or below is recommended.

2.2.5 Usage Notes for TCP Products

(1) Prevention of Static Damage

In addition to normal static preventive measures for IC circuits, observe the following precautions for TCP products.

- Since TCP products have a film layer on their base, they acquire a static charge easily. In handling TCP products exert extra caution in the installation of ion blowers and grounding so that the film does not become charged.
- At the same time as handling the circuits in a manner such that static electricity is not applied to the package leads, carry out static electricity damage prevention measures in the equipment, especially in the parts of the tape guide which contact the lead pins.

(2) Lead Outer Coating

The lead spacing of TCP products is significantly narrower than that of other products and shorting problems are more easily caused by conductive foreign elements such as stray solder or machinings. We recommend an outer coating of resin over the leads as a preventive measure.

Also, to enable TCP products to be mounted at a high density, a conductive foil is bonded to the film, and wiring and leads are formed by precision manufacturing techniques. Therefore, it is possible that contamination of the foil with, for example, solder flux, may result in corrosion and broken connections. Thus, special care should be taken to avoid wiring and lead contamination when mounting TCP products by soldering or other methods.

(3) Mechanical and Electrical Handling

To reduce thickness, the back surface of the chip is exposed in TCP products. To prevent chip cracking or static damage, mount TCP products in a manner which results in no mechanical or electrical contact with the back surface of the chip.

Since the wiring and leads on the TCP tape is fabricated from extremely thin copper foil, its mechanical strength is reduced. Mounting techniques and structures which apply strong external forces to the copper foil should be avoided.

Also, to assure electrical characteristics, avoid direct exposure to sunlight.

(4) Unpacking

- The copper foil is plated. To assure good solderability, use the products as soon after unpacking as possible.
- Since TCP products use polyimide as their base film, the film expands when it absorbs moisture. Although the packaging is moisture proof, TCP products should be used as soon after opening as possible.

(5) Other Items

- We recommend the use of the sprocket holes in the stamped product parts in positioning TCP products during individual punching.
- Since lead tape has a poor ability to withstand heat, and shrinks when heated, do not apply high temperatures to the lead tape.
- Bending TCP products can introduce cracks in the solder resist. Care should be taken to avoid bending when handling TCP products.
- When stacking TCP product boxes (the original packaging) for storage, do not stack more than 10 high.
- Do not apply large mechanical shocks to TCP product packaging.

Package Information

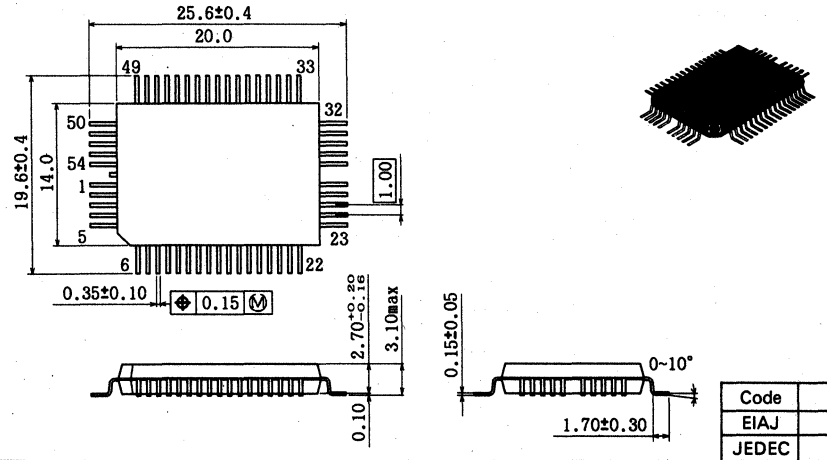
Package Information

The Hitachi LCD driver devices use plastic flat packages to reduce the size of the equipment in which they are incorporated and provide higher density mounting by utilizing the features of thin liquid crystal display elements.

Package Dimensions

Scale: 3/2

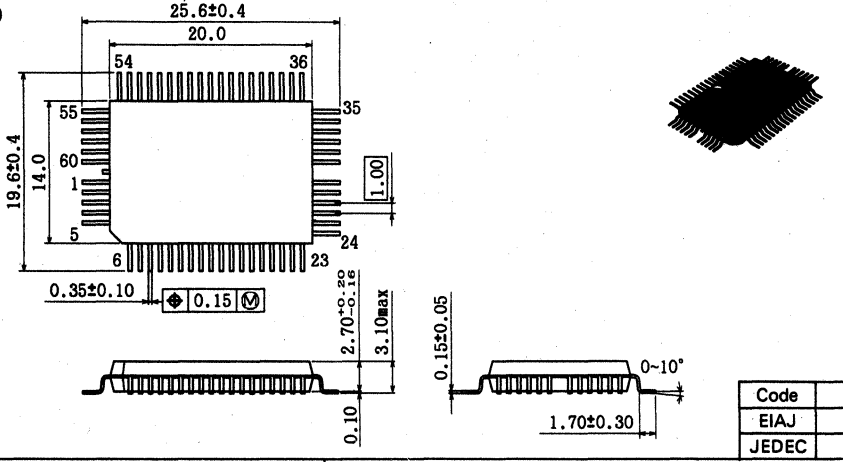
FP-54



Code	FP-54
EIAJ	——
JEDEC	——

Applicable LSI	HD43160AH

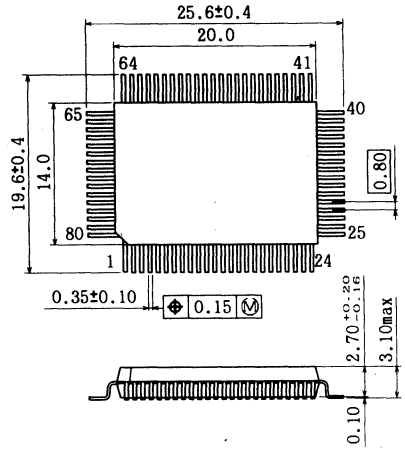
FP-60

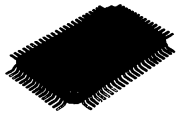


Code	FP-60
EIAJ	——
JEDEC	——

Applicable LSI	HD44100H, HD44103CH, HD44105H HD61830, HD61830B

FP-80

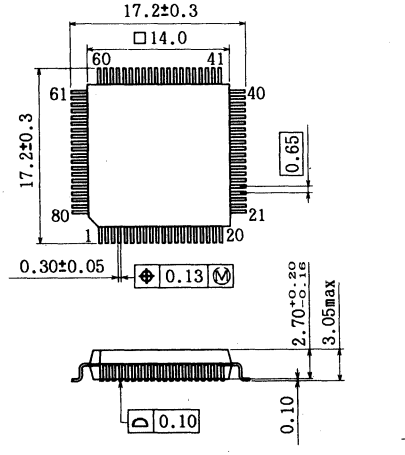




Code	FP-80
EIAJ	——
JEDEC	——

Applicable LSI	HD61602, HD61603, HD61604, HD61605 HD44780, HD66780, HD63645F, HD64645F HD44102CH

FP-80A

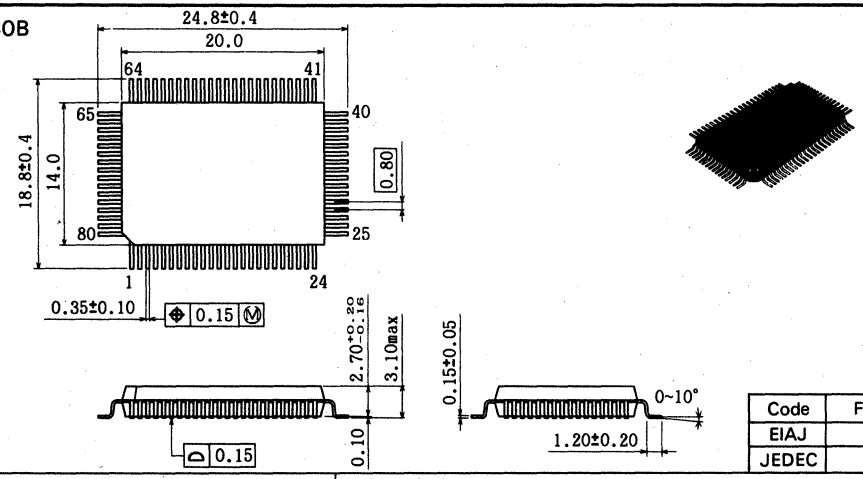


Code	FP-80A
EIAJ	——
JEDEC	——

Applicable LSI	HD66780, HD44780, HD61602

Package Information

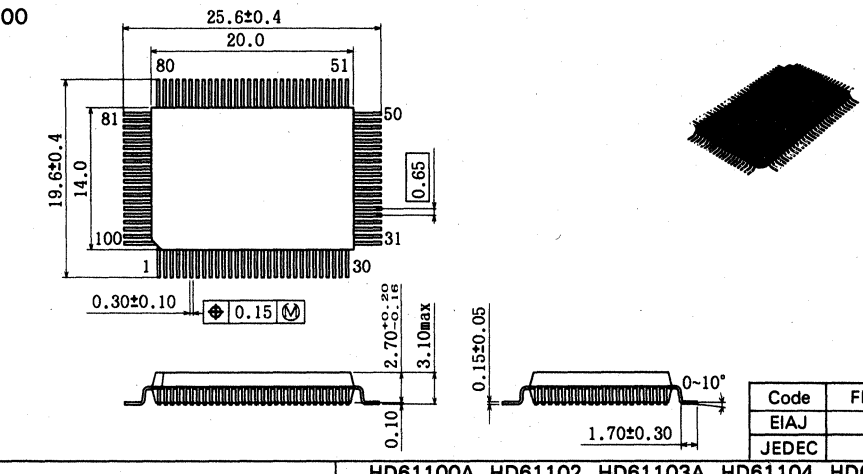
FP-80B



Code	FP-80B
EIAJ	——
JEDEC	——

Applicable LSI	HD64646FS, HD66780

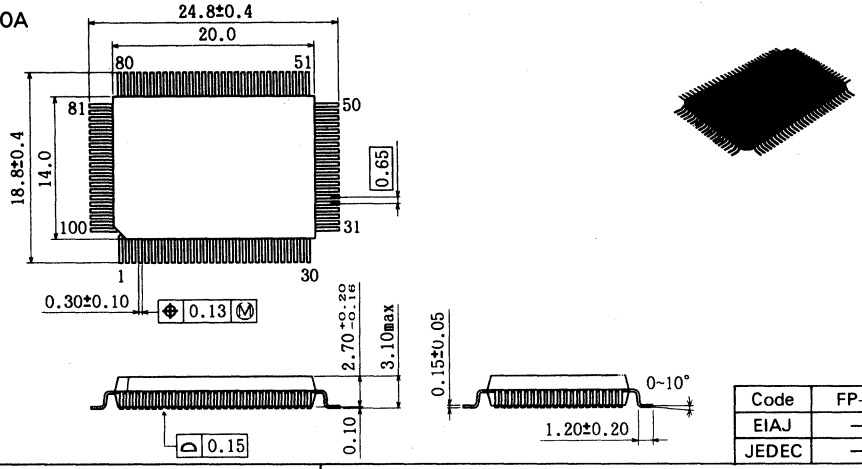
FP-100



Code	FP -100
EIAJ	——
JEDEC	——

Applicable LSI	HD61100A, HD61102, HD61103A, HD61104, HD66204 HD61105, HD66205, HD61200, HD61202, HD61203 HD66100F

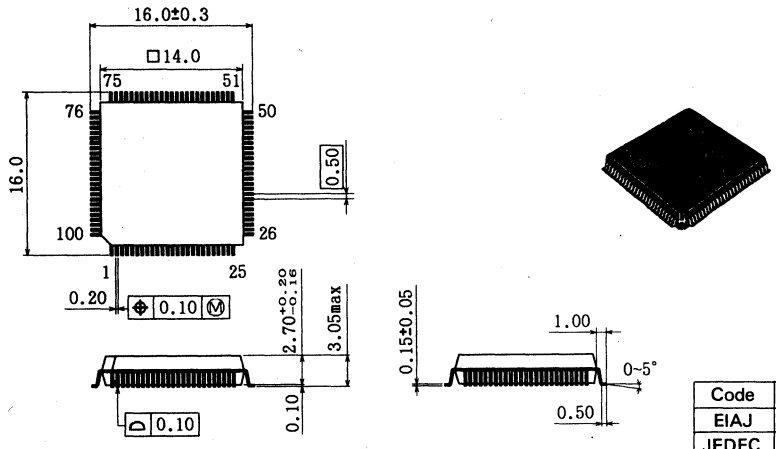
FP-100A



Code	FP-100A
EIAJ	——
JEDEC	——

Applicable LSI	HD66106F, HD66840F, HD66841F

FP-100B

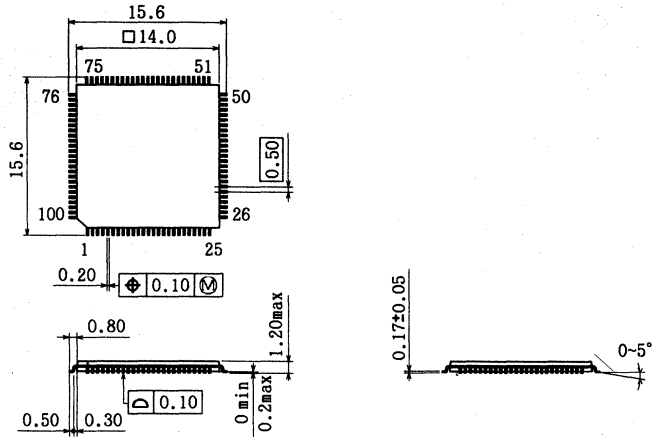


Code	FP-100B
EIAJ	——
JEDEC	——

Applicable LSI	HD66100F

Package Information

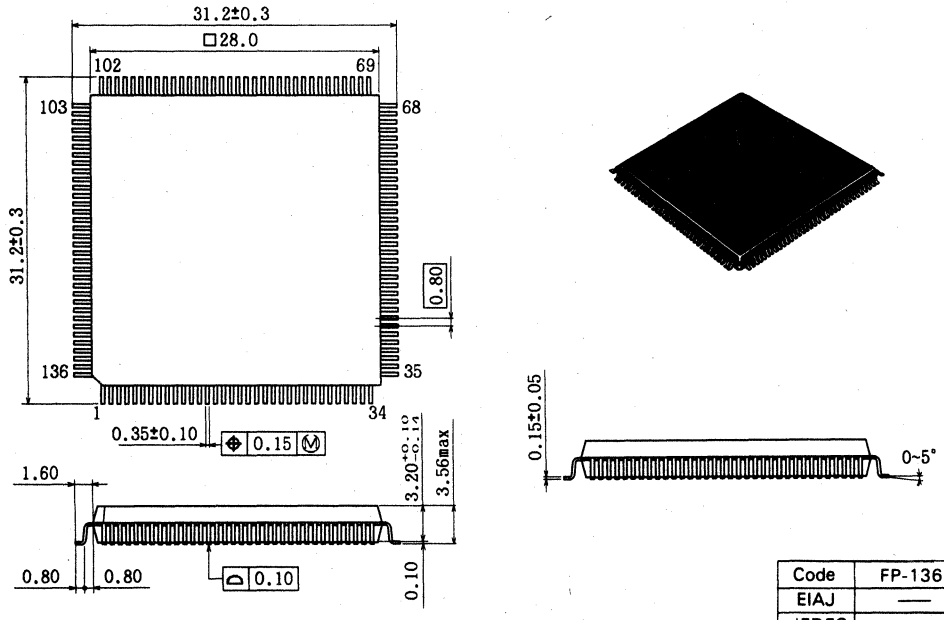
TFP-100



Code	TFP-100
EIAJ	——
JEDEC	——

Applicable LSI	HD61104TF, HD61105TF

FP-136



Code	FP-136
EIAJ	——
JEDEC	——

Applicable LSI	HD66850F

Reliability and Quality Assurance

1. Views on Quality and Reliability

Hitachi's basic quality aims are to meet individual user's purchase purpose and quality required, and to be at a satisfactory quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, Hitachi tries to assure reliability so that semiconductor devices delivered can perform their function in actual operating circumstances. To realize this quality in the manufacturing process, the key points should be to establish a quality control system in the process and to enhance the quality ethic.
In addition, quality required by users of semiconductor devices is going toward higher levels as performance of electronic system in the market is increasing and expanding in size and application fields. To cover the situation, Hitachi is performing the following:

1. Building in reliability in design at the stage of new product development.
2. Buliding in quality at the sources of the manufacturing process.
3. Executing stricter inspection and reliability confirmation of final products.
4. Making quality levels higher with field data feedback.
5. Cooperating with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made to meet users' requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

The reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability targets with failure rates under certain common test conditions. The reliability target is determined corresponding to the character of equipment taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering the operating circumstances of equipment the semiconductor device is used in, reliability target of the system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely study and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

2.2.1 Design Standardization

Establishment of design rules, and standardization of parts, material and process are necessary. To establish design rules, critical quality and reliability items are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in newly developed devices, except in cases where special functions are needed.

2.2.2 Device Design

It is important in device design to consider the total balance of process design, structure design, circuit and layout design. Especially when new processes and new materials are employed, careful technical study is executed prior to device development.

2.2.3 Reliability Evaluation by Test Site

Test site is sometimes called test pattern. It is a useful method for design and process reliability evaluation of ICs and LSIs which have complicated functions.

Purposes of test site are:
- Making fundamental failure mode clear
- Analysis of relation between failure mode and manufacturing process condition
- Search for failure mechanism analysis
- Establishment of QC point in manufacturing

Evaluation by test site is effective because:
- Common fundamental failure mode and failure machanism in devices can be evaluated.
- Factors dominating failure mode can be picked up, and comparison can be made with processes that have been experienced in field.
- Relation between failure causes and manufacturing factors can be analyzed.
- Easy to run tests.
- Etc.

2.3 Design Review

Design review is an organized method to confirm that a design satisfies the required performance (including users') and that design work follows the specified methods, and whether or not improved technical items accumulated in test data of individual major

fields and field data are effectively built in. In addition, from the standpoint of enhancement of the competitive power of products, the major purpose of the design review is to ensure quality and reliability of the products. In Hitachi, design reviews are performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows:

1. Description of the products based on specified design documents.
2. From the standpoint of the specialties of individual participants, design documents are studied, and if unclear matter is found, calculation, experiments, investigation, etc. will be carried out.
3. Determine contents of reliability and methods, etc. based on design documents and drawings.
4. Check process ability of manufacturing line to achieve design goal.
5. Discussion about preparation for production.
6. Planning and execution of subprograms for design changes proposed by individual specialists, and for tests, experiments and calculation to confirm the design changes.
7. Reference of past failure experiences with similar devices, confirmation of methods to prevent them, and planning and execution of test programs for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are:

1. Problems in an individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.
2. Feedback of information should be used to ensure satisfactory level of process capability.
3. To assure required reliability as a result of the items mentioned above is the purpose of quality assurance.

The following discusses device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure required quality and reliability, quality approval is carried out at the trial production stage of device design and the mass production stage based on reliability design as described in section 2.

Hitachi's views on quality approval are:

1. A third party must perform approval objectively from the standpoint of customers.
2. Fully consider past failure experiences and information from the field.
3. Approval is needed for design change or work change.
4. Intensive approval is executed on parts material and process.
5. Study process capability and variation factor, and set up control points at mass production stage.

Considering the views mentioned above, figure 1 shows how quality approval is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control execution is divided organically by function between manufacturing department and quality assurance department, and other related departments. The total function flow is shown in figure 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices improve, the importance of quality control of material and parts (crystal, lead frame, fine wire for wire bonding, package) to build products, and materials needed in manufacturing process (mask pattern and chemicals) increases. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is also key in quality control of parts and materials. The incoming inspection is performed based on an incoming inspection specification, following purchase specification and drawings, and sampling inspection is executed based mainly on MIL-STD-105D.

The other activities of quality assurance are as follows:

1. Outside vendor technical information meeting
2. Approval on outside vendors, and guidance of outside vendors
3. Physical chemical analysis and test

The typical check points of parts and materials are shown in table 1.

3.3.2 Inner Process Quality Control

Inner process quality control performs a very important function in quality assurance of a semiconductor devices. The following is a description of control of semifinal products, final products, manufacturing facilities, measuring equipments, circumstances and submaterials. The quality control in the manufacturing process is shown in figure 3 corresponding to the manufacturing process.

1. Quality Control of Semifinal Products and Final Production Products
   Potential failure factors of semiconductor devices should be removed in manufacturing process. To achieve this, check points are setup in each process, and products that have potential failure factors are not transferred to the next process. For high reliability semiconductor devices, especially manufacturing line is carefully selected, and the quality control in the manufacturing process is tightly executed: Strict check on each process and each lot, 100% inspection to remove failure factor caused by manufacturing variation, and necessary screening, such as high temperature aging and temperature cycling. Contents of inner process quality control are:
   - Condition control on individual equipment and workers, and sampling check of semifinal products.
   - Proposal and carrying-out of work improvement
   - Education of workers
   - Maintenance and improvement of yield
   - Detection of quality problems, and execution of countermeasures
   - Transmission of information about quality

2. Quality Control of Manufacturing Facilities and Measuring Equipment
   Equipment for manufacturing semicon-

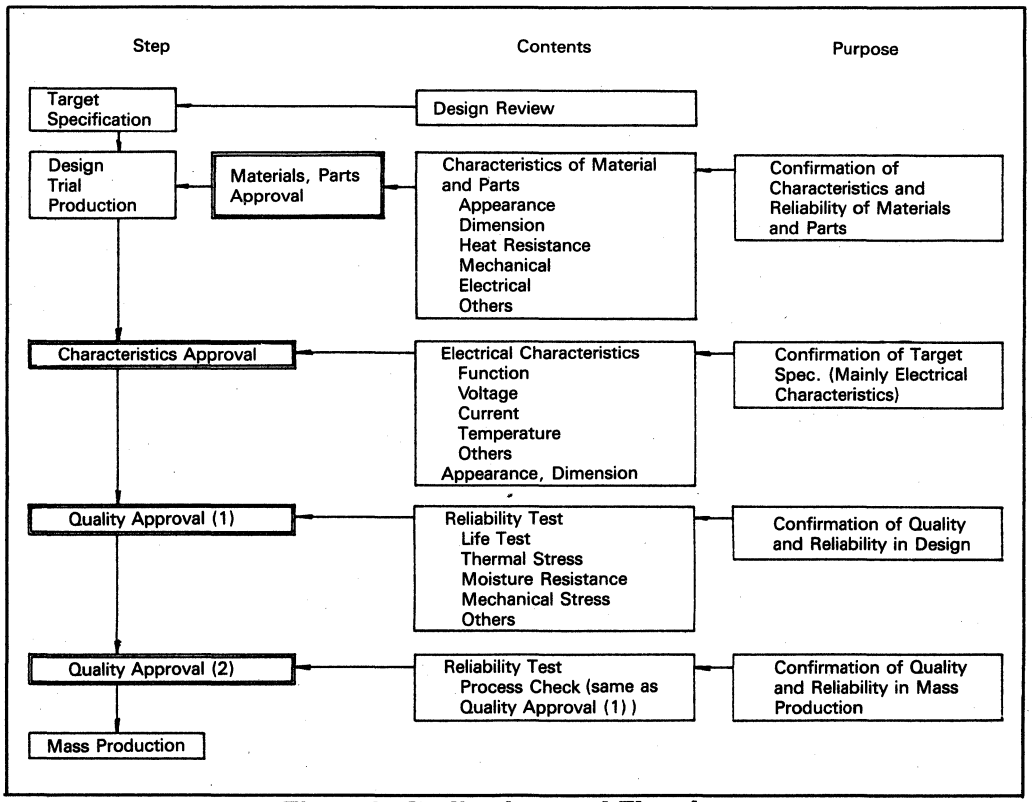


Figure 1 Quality Approval Flowchart

ductor devices have been developing extraordinarily, with required high performance devices and production improvements. They are important factors to determine quality and reliability. In Hitachi, automation of manufacturing equipment is promoted to improve manufacturing variation, and controls maintain proper operation and function of high performance equipment. Maintenance inspection for quality control is performed daily based on related specifications, and also periodical inspections. At the inspection, inspection points listed in the specification are checked one by one to avoid any omissions. During adjustment and maintenance of measuring equipment, maintenance number and specifications are checked one by one to maintain and improve quality.

3. Quality Control of Manufacturing Circumstances and Submaterials
Quality and reliability of semiconductor devices is greatly affected by manufacturing process. Therefore, manufacturing circumstances (temperature, humidity, dust) and the control of submaterials (gas, pure water) used in manufacturing process are intensively controlled. Dust control is described in more detail below.
Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and

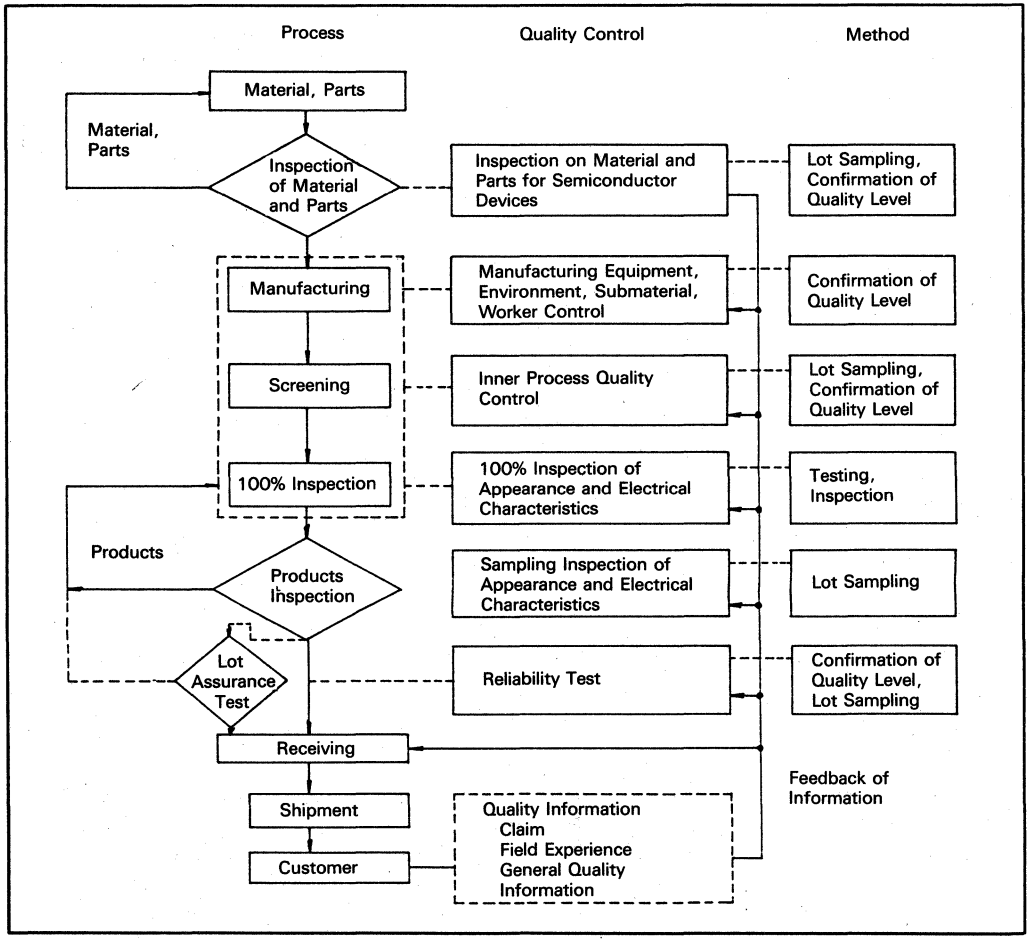


Figure 2 Flowchart of Quality Control in Manufacturing Process

improvement of cleanness and manufacturing site cleanness are executed paying close attention to buildings, facilities, air-conditioning systems, packaging materials, clothes, work, etc., and periodical inspection for floating dust in room, falling dust, and floor dust.

3.3.3 Final Product Inspection and Reliability Assurance

1. Final Product Inspection
   Lot inspection is done by quality assurance department for products that were judged to be 100% good in tests, which is the final process in the manufacturing department. Though 100% good products is expected, sampling inspection is executed to prevent inclusion of failed products by mistake, etc. The inspection is executed not only to confirm that the products meet users' requirements, but to consider potential trouble factors. Lot inspection is executed based on MIL-STD-105D.
1. Reliability Assurance Tests
   To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lots required by user are performed.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Points to Check
Wafer	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratch
	Dimension	Dimension level
	Registration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratch, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratch
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratch
	Dimension	Dimension level
	Leak resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechanical strength
Plastic	Composition	Characteristics of plastic material
	Electrical characteristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

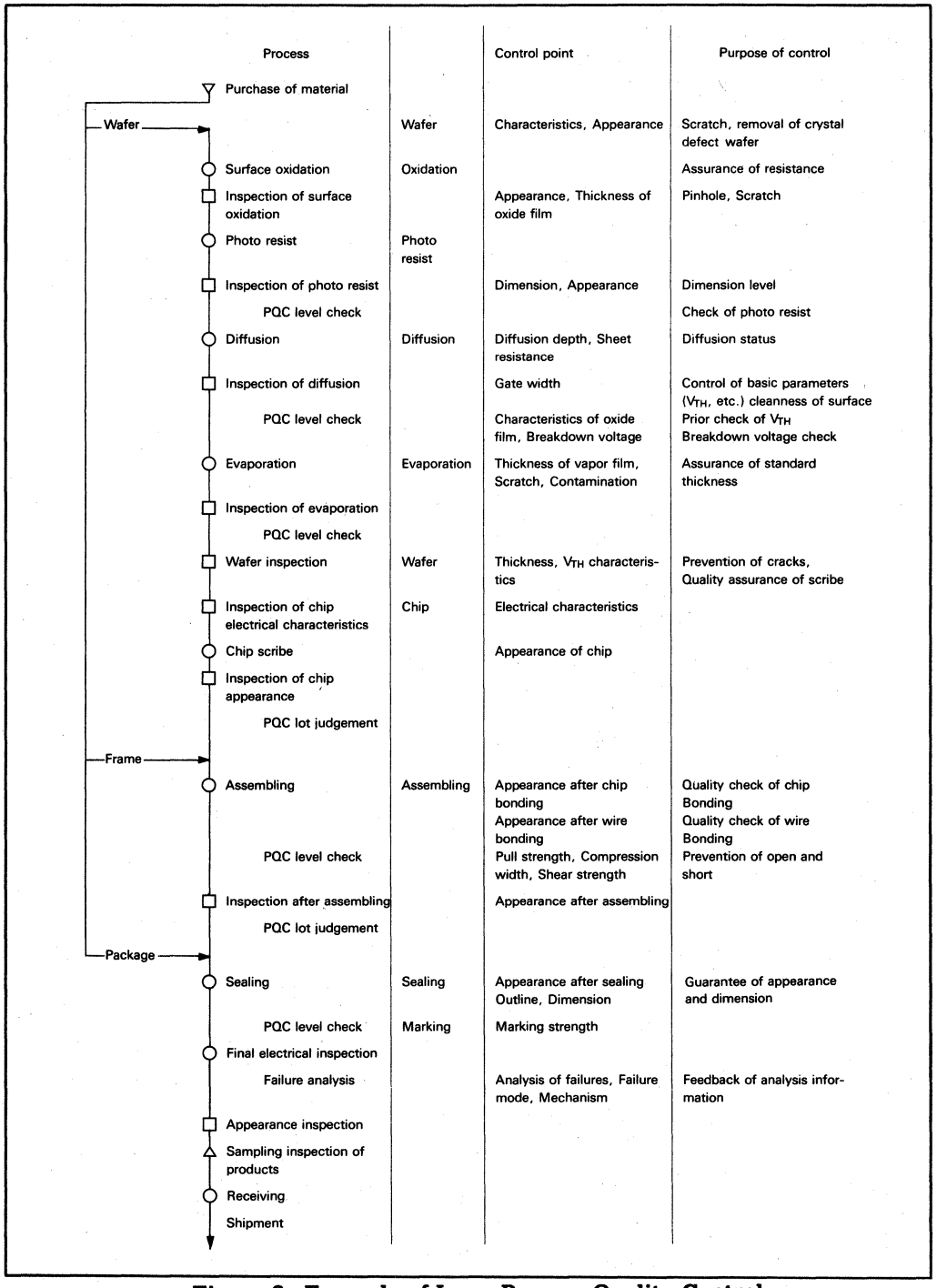


Figure 3 Example of Inner Process Quality Control

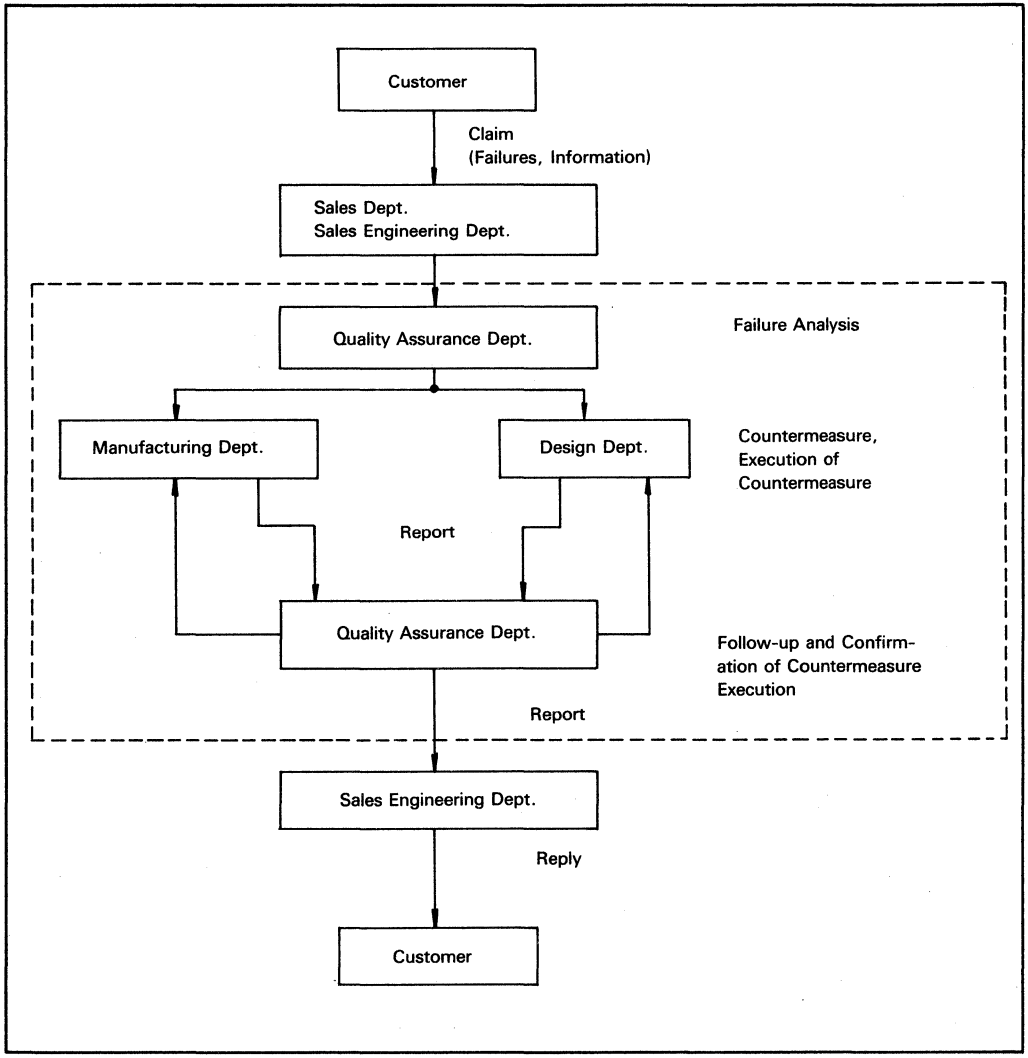


Figure 4 Process Flowchart of Field Failure

Reliability Test Data of LCD Drivers

1. Introduction

The use of liquid crystal displays with microcomputer application systems has been increasing, because of their low power consumption, freedom in display pattern design, and thin shape. Low power consumption and high density packaging have been achieved through the use of the CMOS process and the flat plastic packages, respectively.
This chapter describes reliability and quality assurance data for Hitachi LCD driver LSIs based on test data and failure analysis results.

2. Chip and Package Structure

The Hitachi LCD driver LSI family uses low power CMOS technology and flat plastic package. The Si-gate process is used for high reliability and high density. Chip structure and basic circuit are shown in figure 1, and package structure is shown in figure 2.

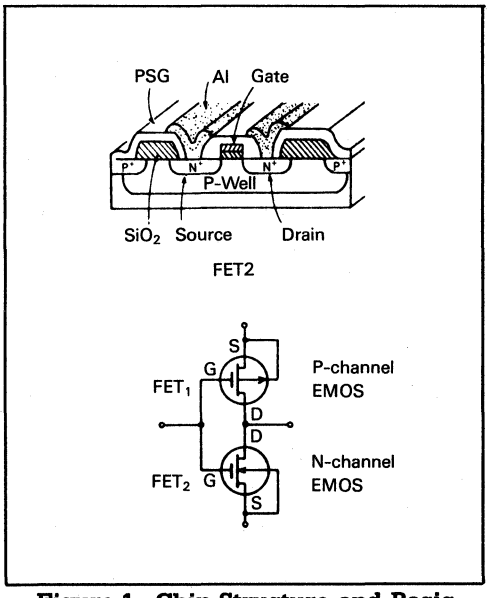


Figure 1 Chip Structure and Basic Circuit

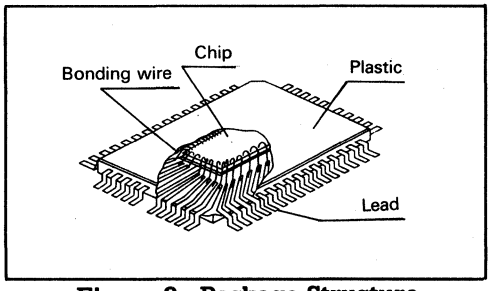


Figure 2 Package Structure

3. Reliability Test Results

The test results of LCD driver LSI family are shown in Tables 1, 2, and 3.

Table 1 Test Result 1, High Temperature Operation ($Ta=125°C$, $V_{CC}=5.5V$)

Device	Sample Size	Component Hour	Failure
HD44100H	40	40,000	0
HD44102H	40	40,000	0
HD44103H	40	40,000	0
HD44780	90	90,000	0
HD66100F	45	45,000	0
HD61100A	80	80,000	0
HD61102	50	50,000	0
HD61103A	50	50,000	0
HD61200	40	40,000	0
HD61202	50	50,000	0
HD61203	40	40,000	0
HD61104	45	45,000	0
HD61105	45	45,000	0
HD61830	40	40,000	0
HD61830B	40	40,000	0
HD63645	32	32,000	0
HD64645	32	32,000	0
HD61602	38	38,000	0
HD61603	32	32,000	0
HD61604	32	32,000	0
HD61605	32	32,000	0
HD66840	45	45,000	0

Table 2 Test Result 2

Test Item	Test Condition	Sample Size	Component Hour	Failure
High temp, storage	Ta=150°C, 1000 h	180	180,000	0
Low temp, storage	Ta=-55°C, 1000 h	140	140,000	0
Steady state humidity	65°C, 95% RH, 1000 h	860	860,000	1*
Steady state humidity, biased	85°C, 90% RH, 1000 h	165	170,000	2*
Pressure cooker	121°C, 2 atm.100 h	200	20,000	0

Note: *Aluminum corrosion

Table 3 Test Results 3

Test Items	Test Condition	Sample Size	Failure
Thermal shock	0 to 100°C 10 cycles	108	0
Temperature cycling	-55°C to 150°C 10 cycles	678	0
Soldering heat	260°C, 10 seconds	283	0
Resistance to VPS	215°C, 30 seconds	88	0
Solderability	230°C, 5 seconds	140	0

4. Quality Data from Field Use

Field failure rate is estimated in advance through production process evaluation and reliability tests. Past field data on similar devices provides the basis for this estimation. Quality information from the users is indispensable to the improvement of product quality. Therefore, field data on products delivered to the users is followed up carefully. On the basis of information furnished by the user, failure analysis is conducted and the results are quickly fed back to the design and production divisions.

Failure analysis results on MOS LSIs returned to Hitachi is shown in figure 3.

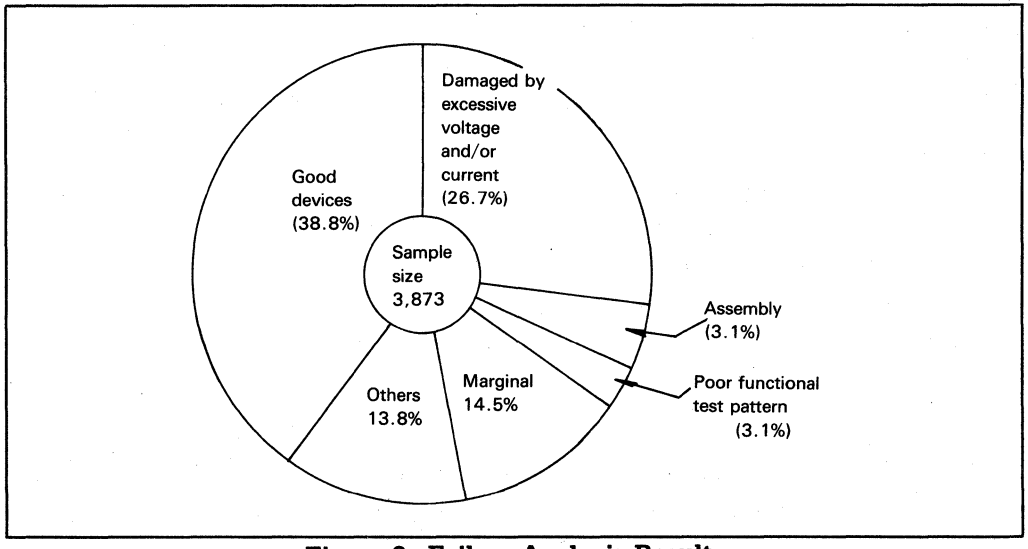


Figure 3 Failure Analysis Result

5. Precautions

5.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent deterioration in their electrical characteristics, solderability, and appearance, or breakage.

1. Store in an ambient temperature of 5 to 30° C, and in a relative humidity of 40 to 60%.
2. Store in a clean air environment, free from dust and reactive gas.
3. Store in a container that does not induce static electricity.
4. Store without any physical load.
5. If semiconductor devices are stored for a long time, store them in unfabricated form. If their lead wires wires are formed beforehand, bent parts may corrode during storage.
6. If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpackaged devices must not be stored for over 3 months.
7. Take care not to allow condensation during storage due to rapid temperature changes.

5.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be taken, too:

1. Use containers or jigs whch will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.
2. Prevent device breakage from clothes-induced static electricity.
3. When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is prevented by shorting terminal circuit. When a conveyor belt is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.
4. When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

5.3 Handling for Measurement

Avoid static electricity, noise, and surge voltage when measuring semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open providing the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, conveyor belt, etc. The device will fail if it touches something that leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units, etc. to leak current through their terminals or housings.

Especially, while testing the devices, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source. During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that there is no soldering bridge or foreign matter before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

Flat Plastic Package (QFP) Mounting Methods

Surface Mounting Package Handling Precautions

1. Package temperature distribution

The most common method used for mounting a surface mounting device is infrared reflow. Since the package is made of a black epoxy resin, the portion of the package directly exposed to the infrared heat source will absorb heat faster and thus rise in temperature more quickly than other parts of the package unless precautions are taken. As shown in the example in figure 1, the surface directly facing the infrared heat source is 20° to 30°C higher than the leads being soldered and 40° to 50°C higher than the bottom of the package. If soldering is performed under these conditions, package cracks may occur.

To avoid this type of problem, it is recommended that an aluminum infrared heat shield be placed over the resin surface of the package. By using a 2-mm thick aluminum heat shield, the top and bottom surfaces of the resin can be held to 175°C when the peak temperature of the leads is 240°C.

2. Package moisture absorption

The epoxy resin used in plastic packages will absorb moisture if stored in a high-humidity environment. If this moisture absorption becomes excessive, there will be sudden vaporization during soldering, causing the interface of the resin and lead frame to spread apart. In extreme cases, package cracks will occur. Therefore, especially for thin packages, it is important that moisture-proof storage be used.
To remove any moisture absorbed during transportation, storage, or handling, it is recommended that the package be baked at 125°C for 16 to 24 hours before soldering.

3. Heating and cooling

One method of soldering electrical parts is the solder dip method, but compared to the reflow method, the rate of heat transmission is an order of magnitude higher. When this method is used with plastic items, there is thermal shock resulting in package cracks and a deterioration of moisture-resistant characteristics. Thus, it is recommended that the solder dip method not be used.
Even with the reflow method, an excessive rate of heating or cooling is undesirable. A rate in temperature change of less than 4°C/sec is recommended.

4. Package contaminants

It is recommended that a resin-based flux be used during soldering. Acid-based fluxes have a tendency of leaving an acid residue which adversely affects product reliability. Thus, acid-based fluxes should not be used.
With resin-based fluxes as well, if a residue is left behind, the leads and other package parts will begin to corrode. Thus, the flux must be thoroughly washed away. If cleansing solvents used to wash away the flux are left on the package for an extended period of time, package markings may fade, so care must be taken.

The precautions mentioned above are general points to be observed for reflow. However, specific reflow conditions will depend on such factors as the package shape, printed circuit board type, reflow method, and device type. For reference purposes, an example of reflow conditions for a QFP infrared reflow furnace is given in figure 2. The values given in the figure refer to the temperature of the package resin, but the leads must also be limited to a maximum of 260°C for 10 seconds or less.

Of the reflow methods, infrared reflow is the most common. In addition, there is also the paper phase reflow method. The recommended conditions for a paper phase reflow furnace are given in figure 3.
For details on surface mounting small thin packages, please consult the separate manual available on mounting. If there are any additional questions, please contact Hitachi, Ltd.

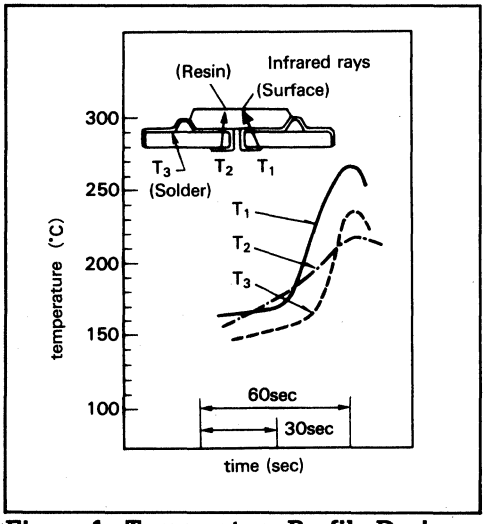


Figure 1 Temperature Profile During Infrared Heat Soldering (Example)

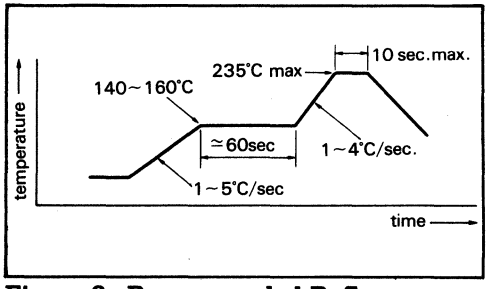


Figure 2 Recommended Reflow Conditions for QFP

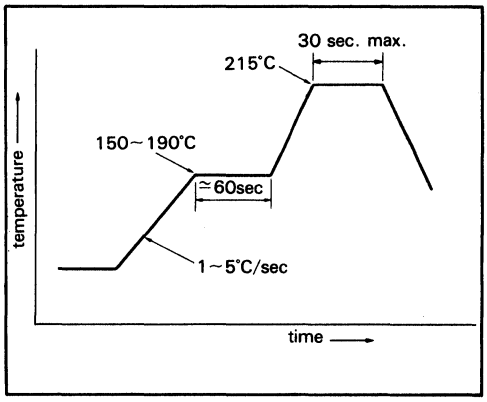


Figure 3 Example Vapor-phase Reflow Conditions

2

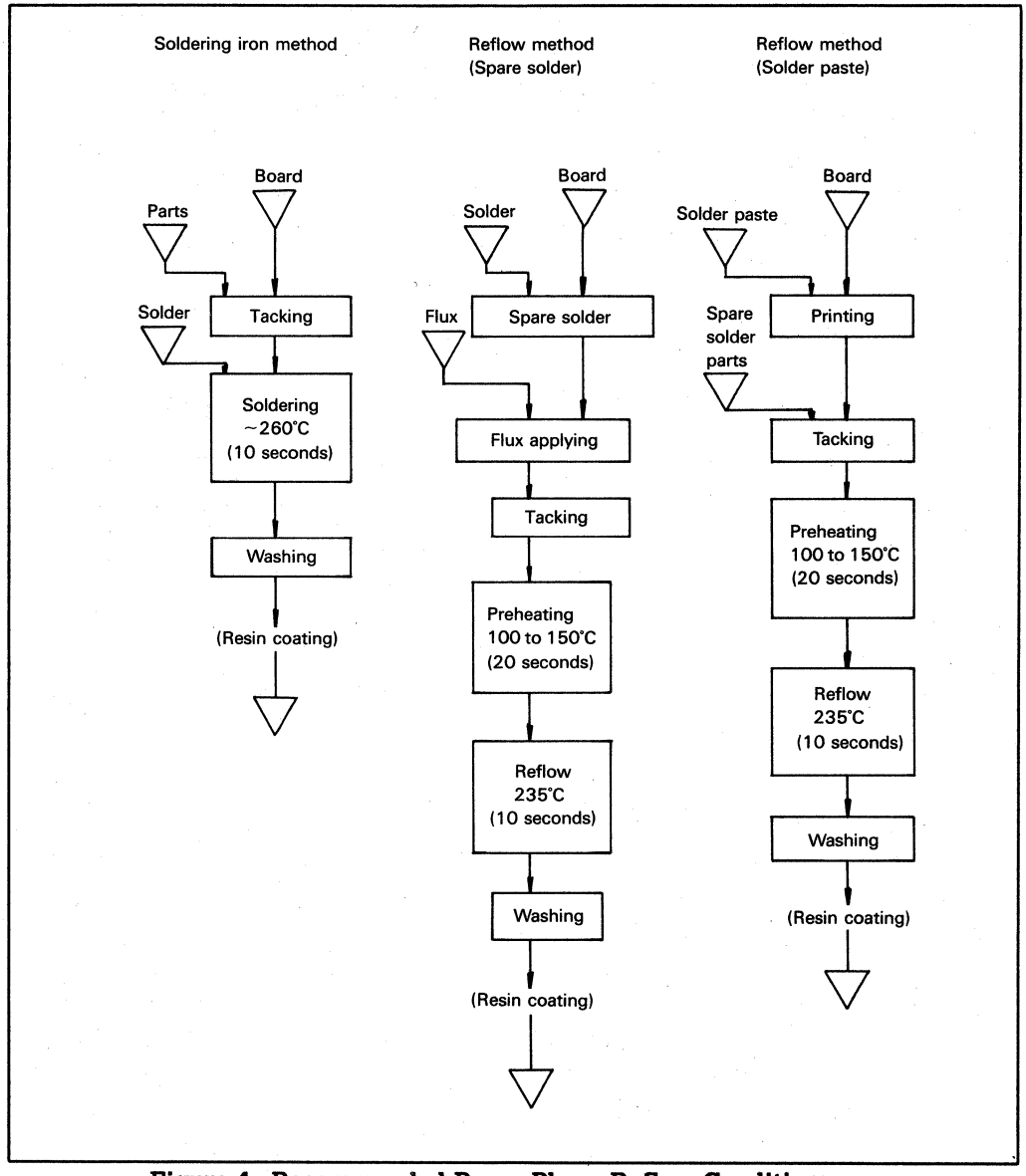


Figure 4 Recommended Paper Phase Reflow Conditions

Liquid Crystal Driving Methods

Driving a liquid crystal at direct current triggers an electrode reaction inside the liquid cell, degrading display quality rapidly. The liquid crystal must be driven by alternating current. The AC driving method includes the static driving method and the multiplex driving method, each of which has features for different applications. Hitachi has developed different LCD driver devices corresponding to the static driving method and the multiplex driving method. The following sections describe the features of each driving method, the driving waveforms, and how to apply bias.

1. Static Driving Method

Figure 1 shows the driving waveforms of the static driving method and an example in which "4" is displayed by the segment method. The static driving method is the most basic method by which good display quality can be obtained. However, it is not suitable for liquid displays with many segments because one liquid crystal driver circuit is required per segment.
The static driving method uses the frame frequency ($1/t_f$) of several tens to several hundreds Hz.

2

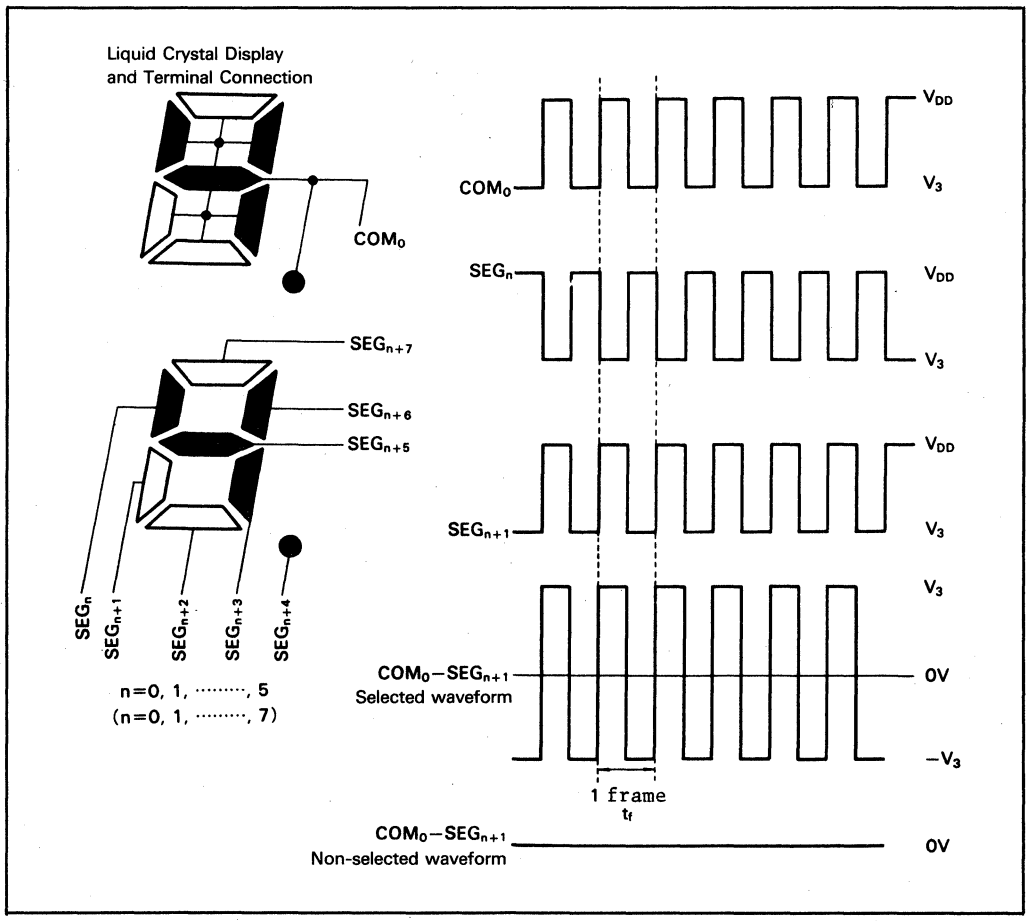


Figure 1 Example of Static Drive Waveforms (Example of HD61602/HD61603)

2. Multiplex Driving Method

The multiplex driving method is effective in reducing the number of driver circuits, the number of connections between the circuit and the display cell, and the cost when driving many display picture elements. Figure 2 shows a comparision of the static drive with the multiplex drive (1/3 duty cycle) in an 8-dight numeric display. The number of liquid crystal driver circuits required is 65 for the former and 27 for the latter. The multiplex drive reduces the number of driver circuits. However, greater multiplexing reduces the driving voltage tolerance. Thus, there are limits to the extent of multiplexing.

There are two types of multiplex drive waveforms: A type and B type. A type, shown in figure 3, is used for alternation in 1 frame. B type is used for alternation in between 2 frames (figure 4). B type has better display quality than A type in high multiplex drive.

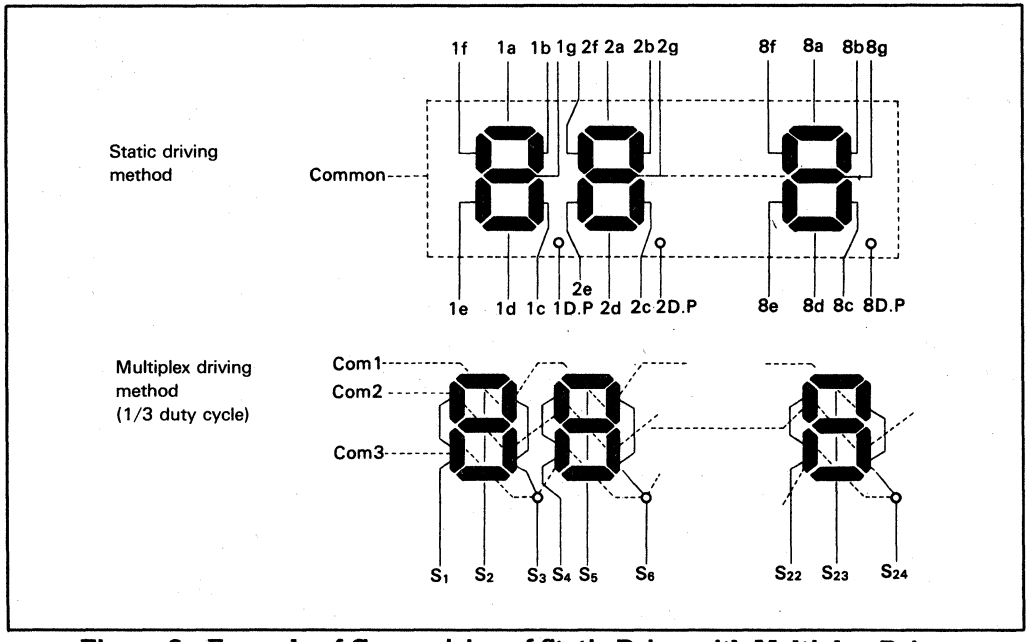


Figure 2 Example of Comparision of Static Drive with Multiplex Drive

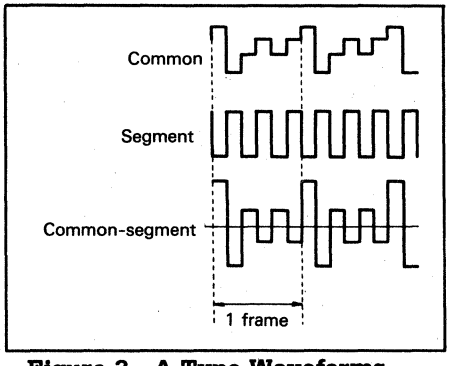


Figure 3 A Type Waveforms (1/3 duty cycle, 1/3 bias)

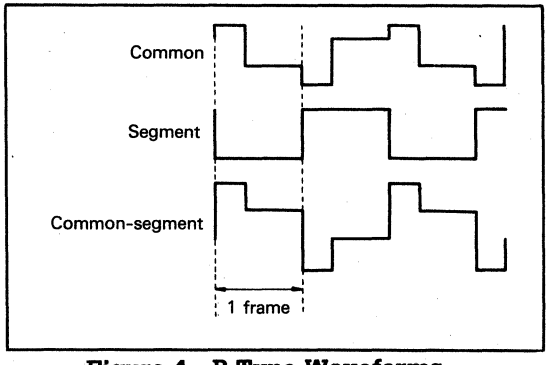


Figure 4 B Type Waveforms (1/3 duty cycle, 1/3 bias)

2.1. 1/2 Bias, 1/2 Duty Drive

In the 1/2 duty drive method, 1 driver circuit drives 2 segments. Figure 5 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

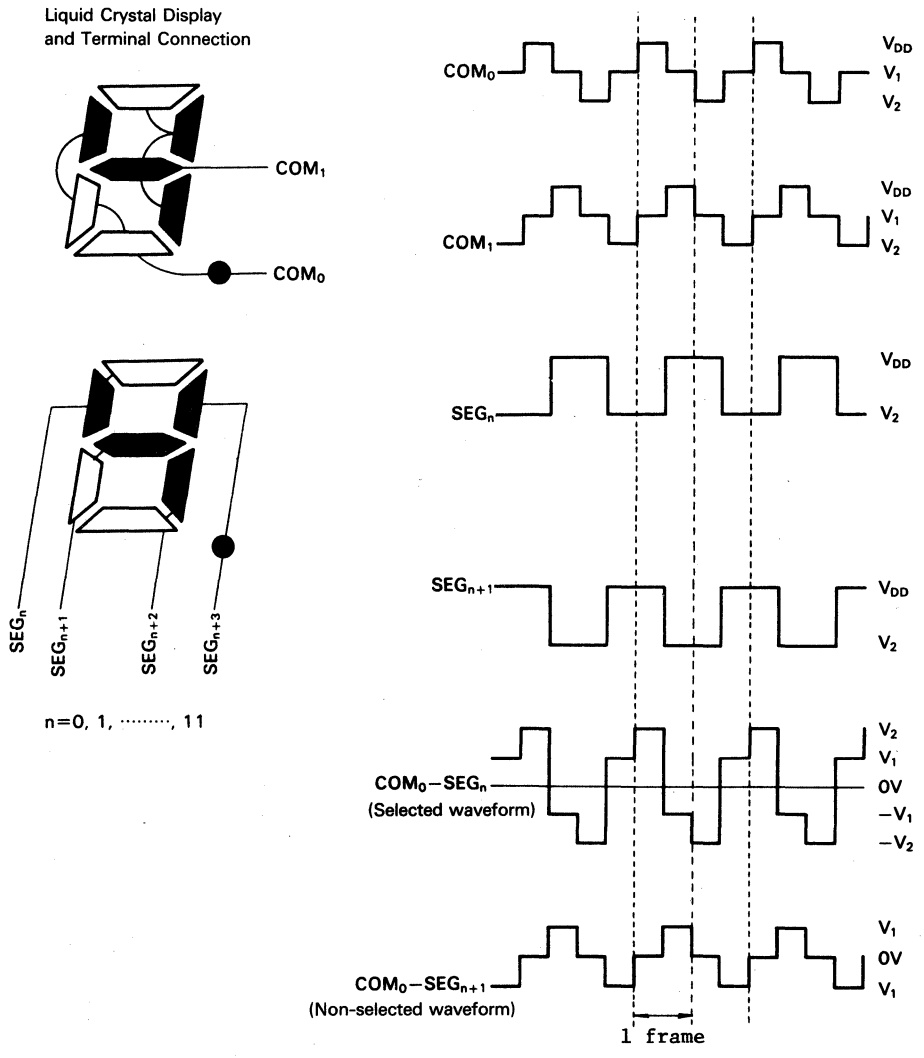


Figure 5 Example of Waveforms in 1/2 Duty Cycle Drive (B type) (Example of HD61602)

2.2 1/3 Bias, 1/3 Duty Cycle Drive

In the 1/3 duty cycle drive, 3 segments are driven by 1 segment output driver. Figure 6 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

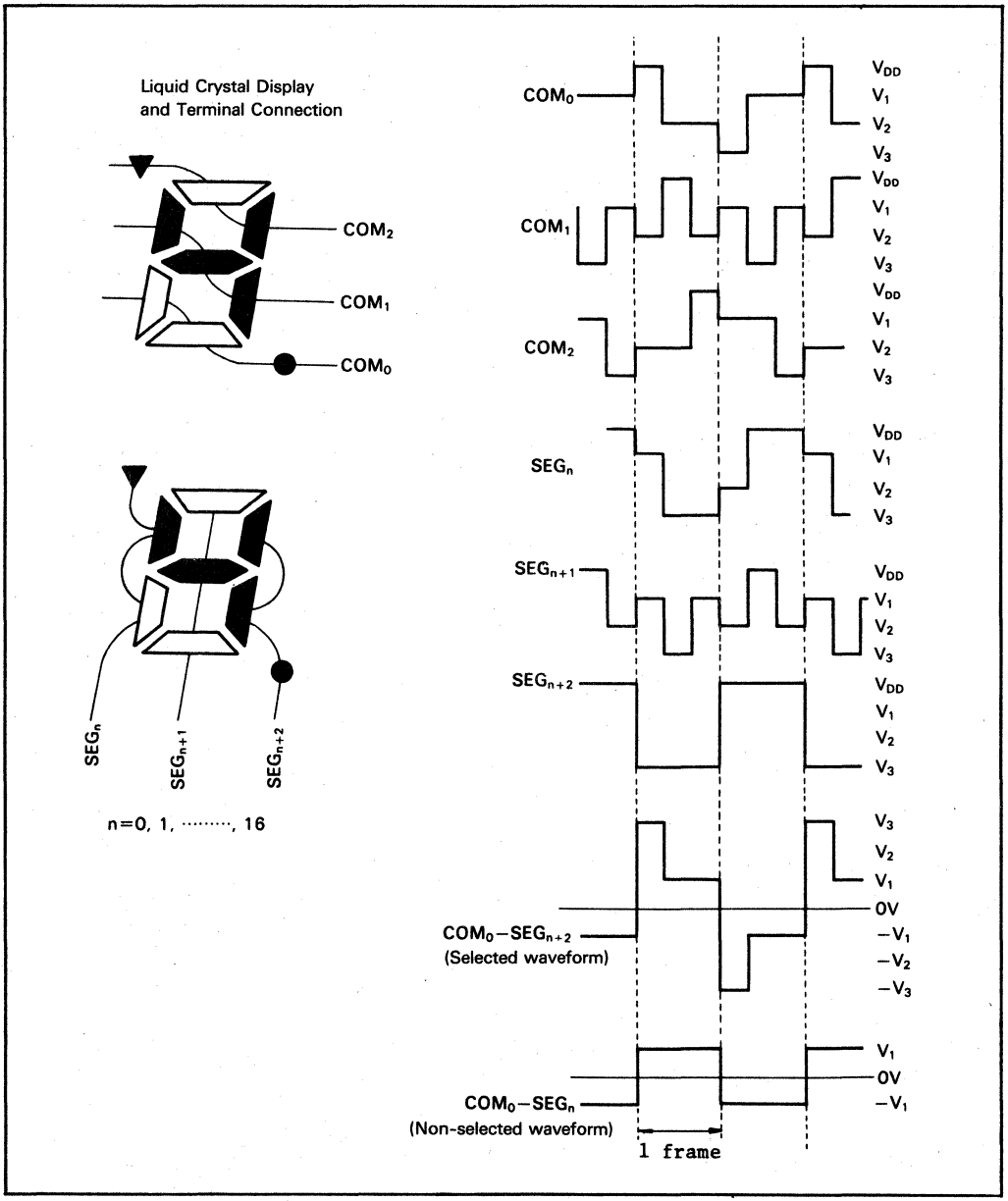


Figure 6 Example of Waveforms in 1/3 Duty Cycle Drive (B type) (Example of HD61602)

2.3 1/3 Bias, 1/4 Duty Cycle Drive

In the 1/4 duty cucle drive, 4 segments are driven by 1 segment output driver. Figure 7 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

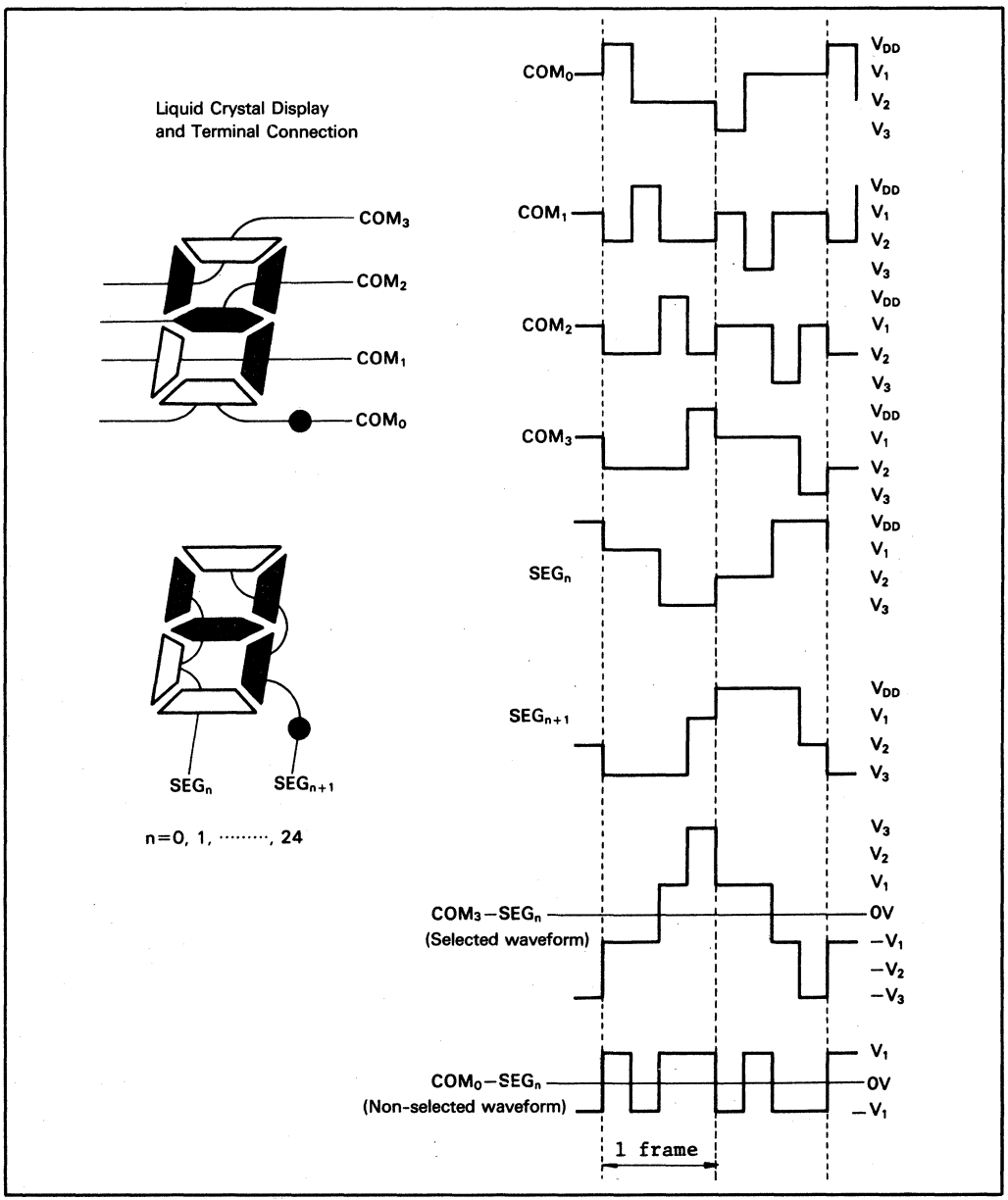


Figure 7 Example of Waveforms in 1/4 Duty Cycle Drive (B type) (Example of HD61602)

2.4 1/4 Bias, 1/8 Duty Cycle Drive

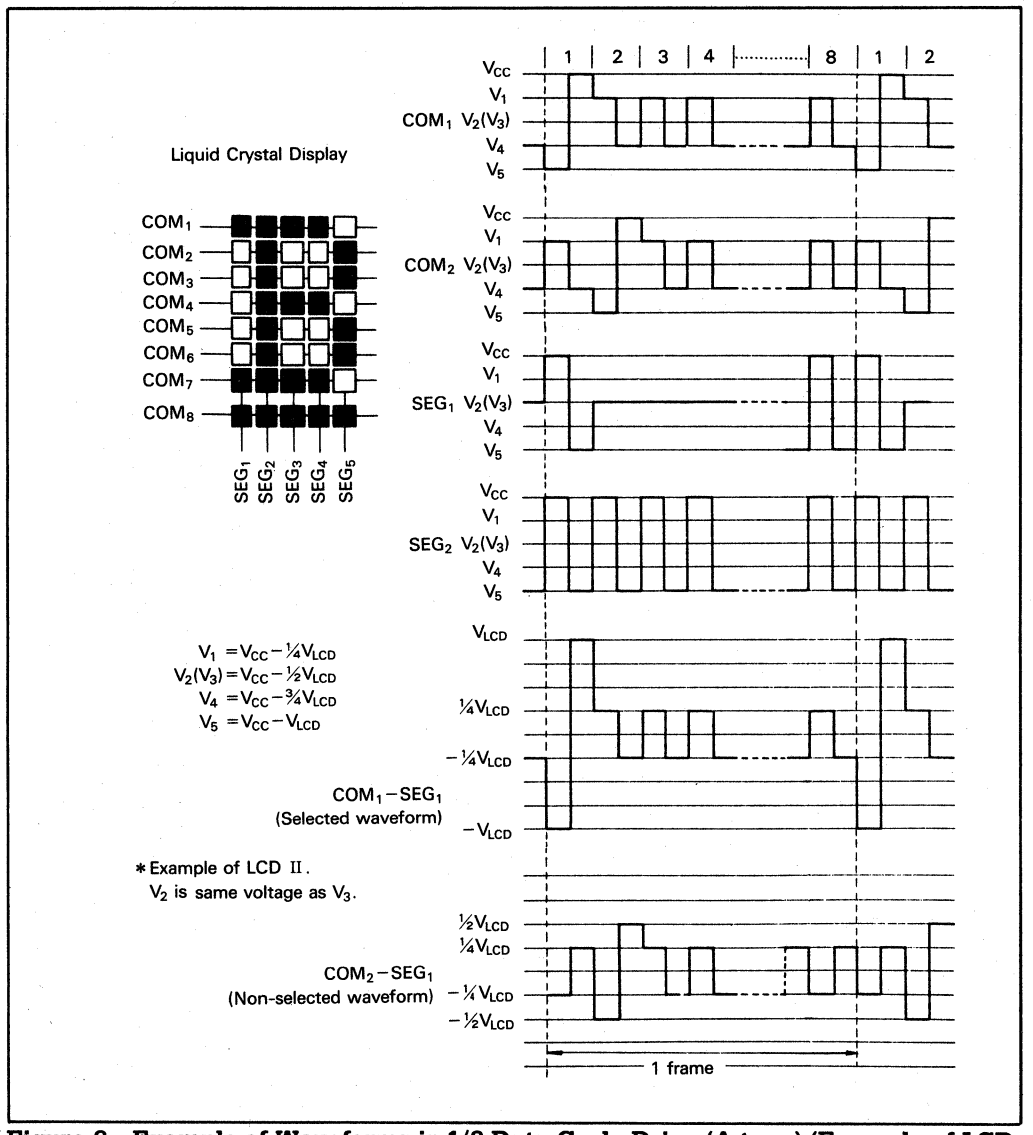


Figure 8 Example of Waveforms in 1/8 Duty Cycle Drive (A type) (Example of LCD-II)

2.5 1/5 Bias, 1/8 Duty Cycle Drive

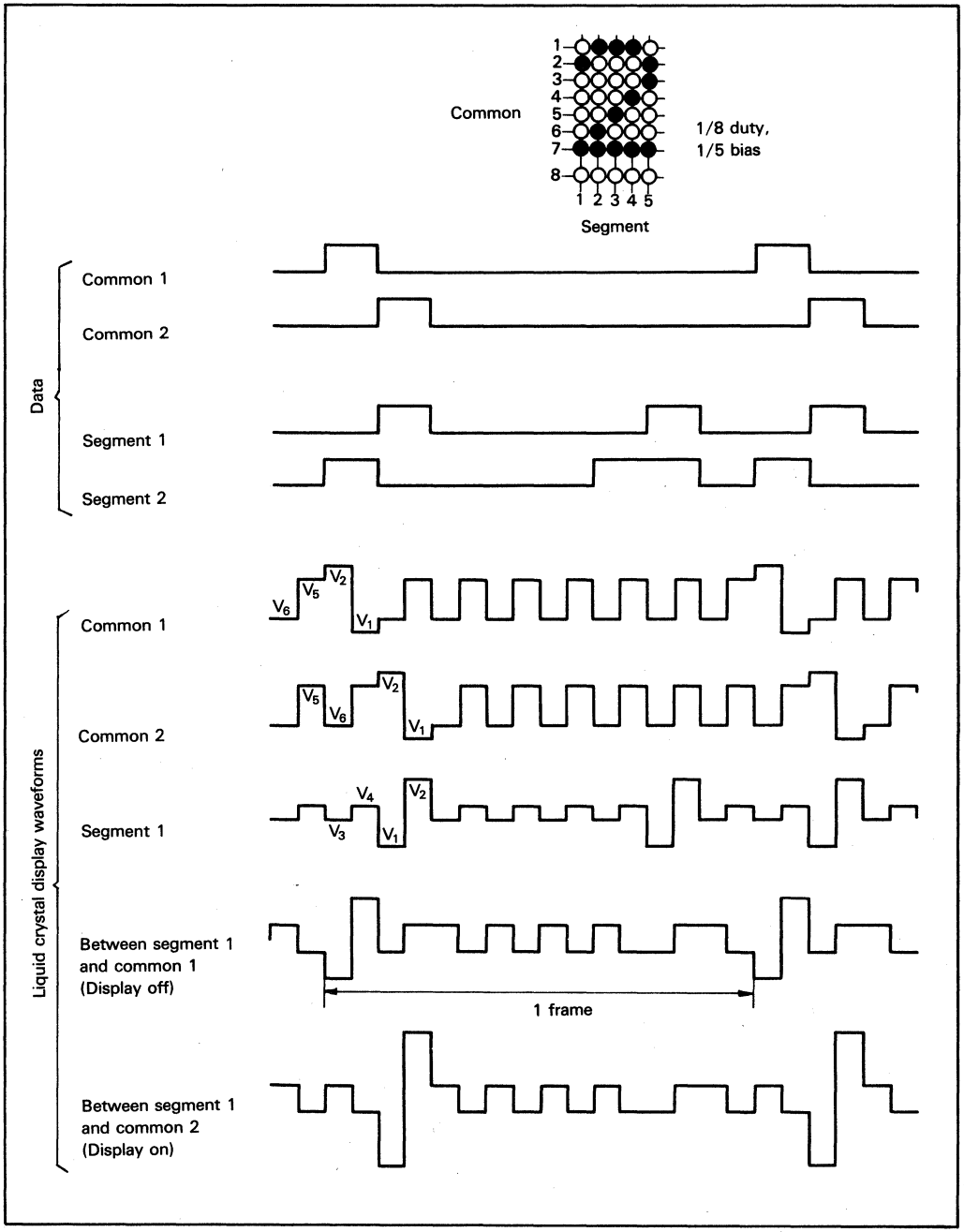


Figure 9 Example of Waveforms in 1/8 Duty Cycle Drive (A type) (Example of HD44100H)

2.6 1/5 Bias, 1/16 Duty Cycle Drive

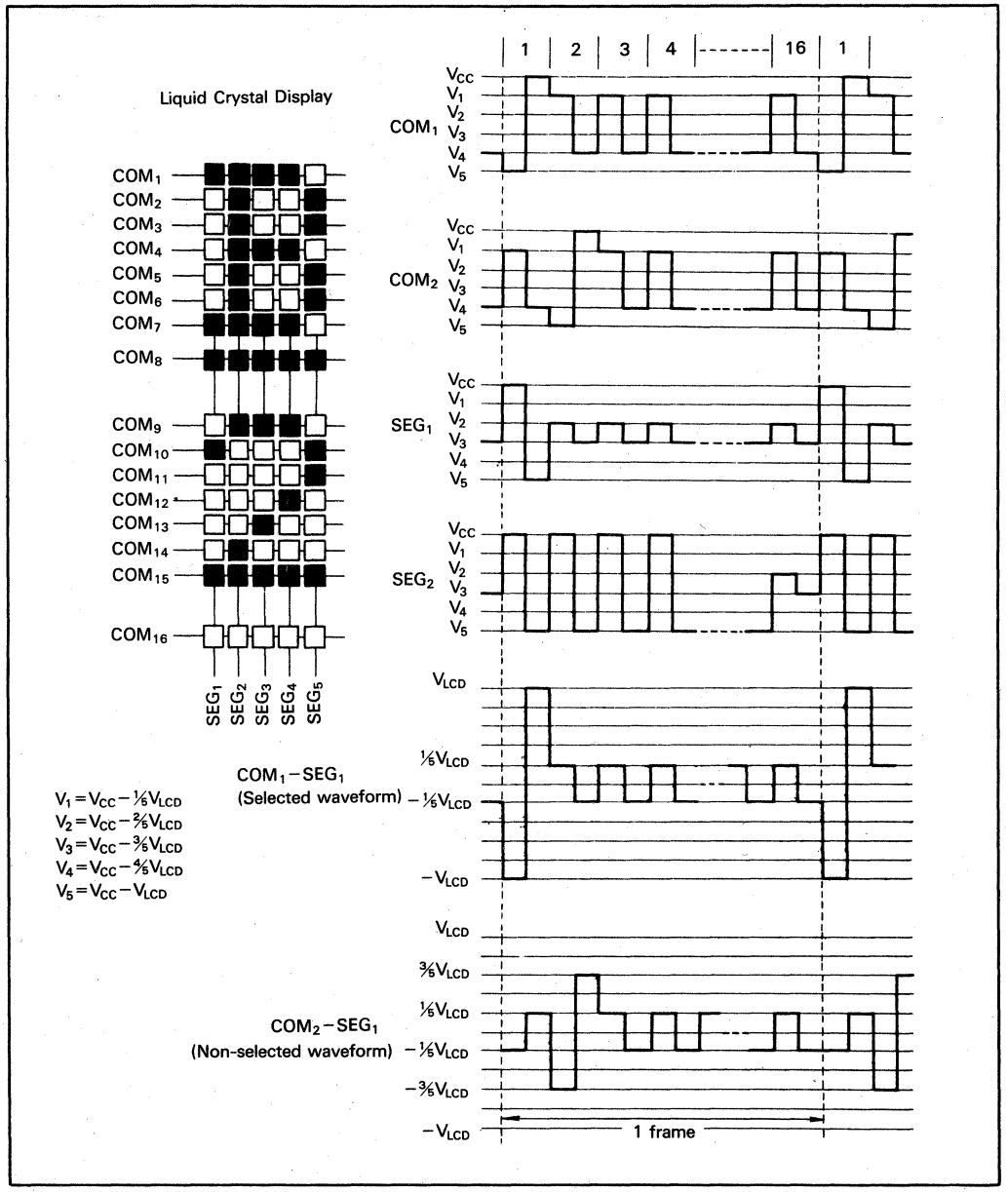


Figure 10 Example of Waveforms in 1/16 Duty Cycle Drive (A type) (Example of LCD-II)

2.7 1/5 Bias, 1/32 Duty Cycle Drive

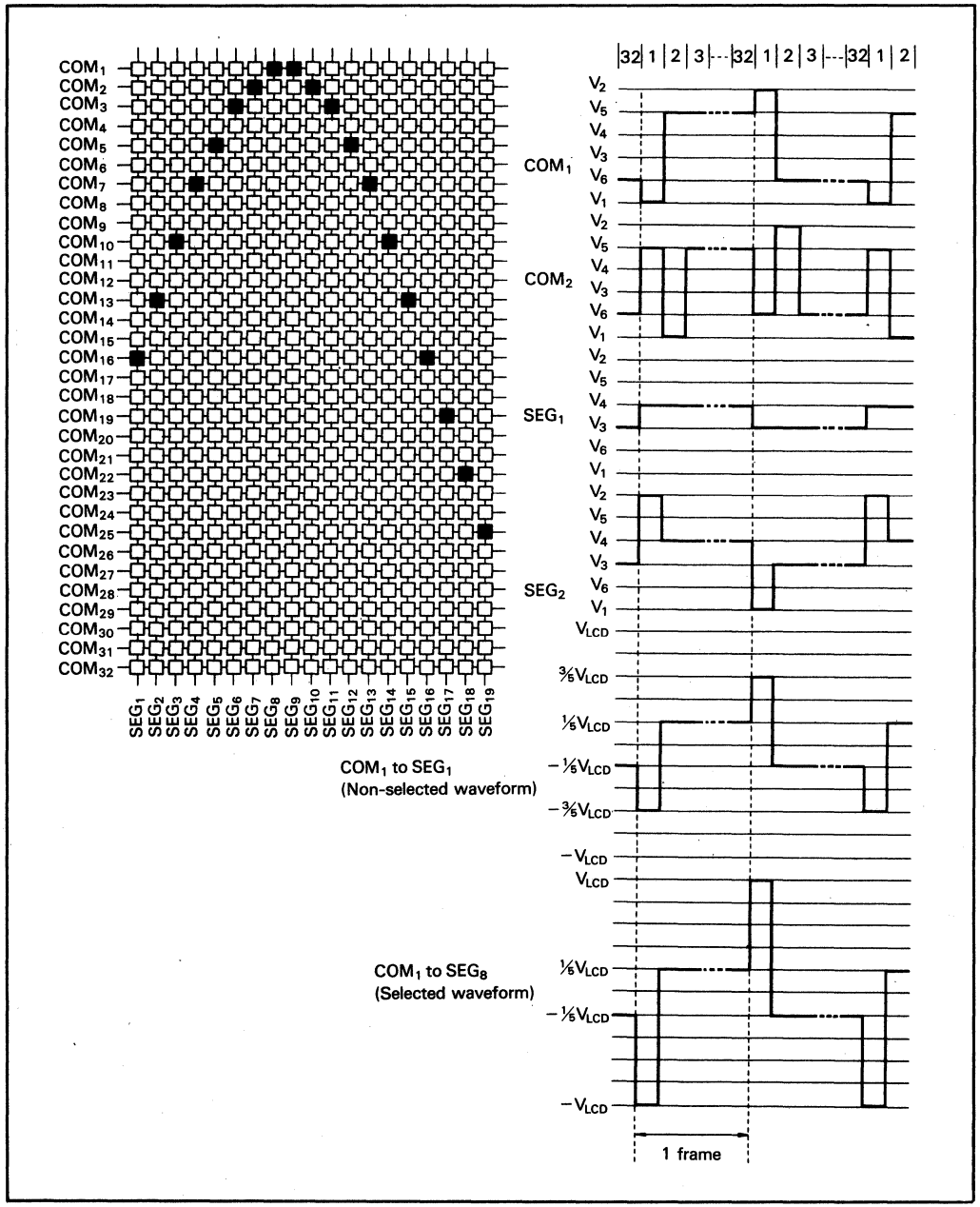


Figure 11 Example of Waveforms in 1/32 Duty Cycle Drive (Example of HD44102CH, HD44103CH)

3. Power Supply Circuit for Liquid Crystal Drive

Table 1 shows the relationship between the number of driving biases and display duty cycle ratios.

3.1 Resistive Dividing

Driving bias is generally generated by a resistive divider (figure 12).

The resistance value settings are determined by considering operating margin and power consumption. Since the liquid crystal display load is capacitive, the drive waveform itself is distorted due to charge/discharge current when the liquid crystal display drive waveform is applied. To reduce distortion, the resistance value should be decreased but this increases the power consumption because of the increase of the current through the dividing resistors. Since larger liquid crystal display panels have larger capacitance,the resistance value must be decreased proportionally.

Table 1 Relationship between the Number of Display Duty Cycle Ratio and the Number of Driving Biases

Display duty ratio	Static	1/2	1/3	1/4	1/7	1/8	1/11	1/12	1/14	1/16	1/24	1/32	1/64
Number of driving biases	2	3 (1/2 bias)	4 (1/3 bias)	4	5 (1/4 bias)	5	5	5	6 (1/5 bias)	6	6	6	6

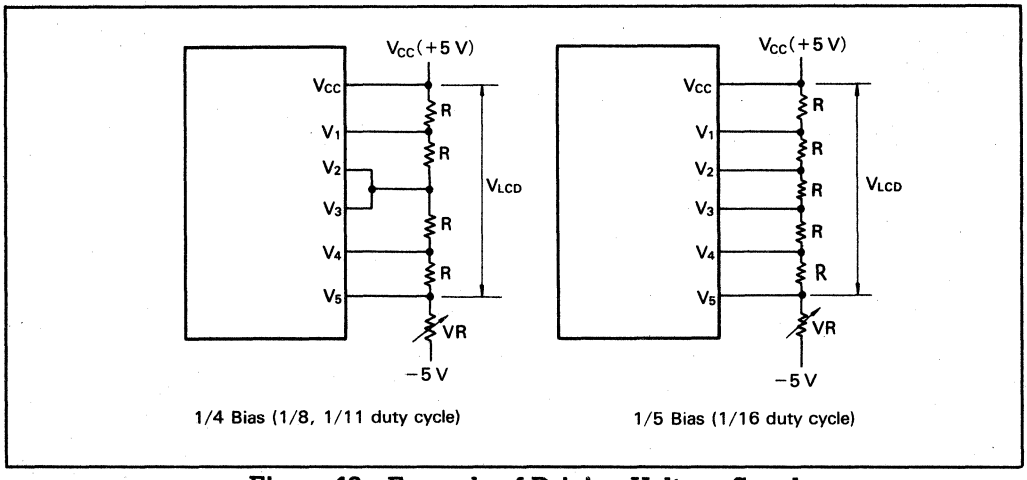


Figure 12 Example of Driving Voltage Supply

It is efficient to connect a capacitor to the resistors in parallel as shown in figure 13 in order to improve charge/discharge distortion. However, the effect is limited. Even if it is attempted to reduce the power consumption with a large resistor and improve waveform distortion with a large capacitor, a level shift occurs and the operating margin is not improved.
Since the liquid crystal display load is in a matrix configuration, the path of the charge/discharge current through the load is complicated. Moreover, it varies depending on display condition. Thus, a value of resistance cannot be simply determined from the load capacitance of liquid crystal display. It must be experimentally determined according to the demand for the power consumption of the equipment in which the liquid crystal display is incorporated.
Generally, R is 1 kΩ to 10 kΩ, and VR is 5kΩ to 50 kΩ. No capacitor is required. A capacitor of 0.1 uF is usually used if necessary.

2

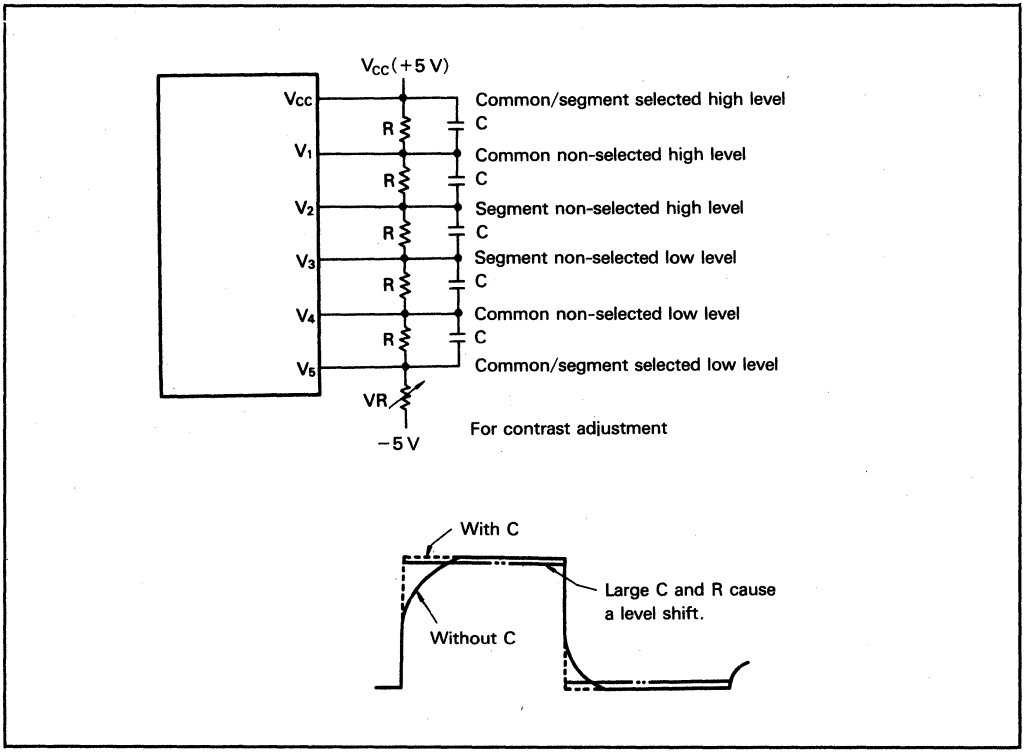


Figure 13 Example of Capacitor Connection for Improvement of Liquid Crystal Display Drive Waveform Distortion (1/5 bias) (Example of LCD-II)

3.2 Drive by Operational Amplifier

In graphic displays, the size of the liquid crystal becomes larger and the display duty ratio becomes smaller, so the stability of liquid crystal drive level is more important than in small display system.
Since the liquid crystal for graphic displays is large and has many picture elements, the load capacitance becomes large. The high impedance of the power supply for liquid crystal drive produces distortion in the drive waveforms, and degcades disiplay quality. For this reason, the liquid crystal drive level impedance should be reduced with operational amplifiers. Figure 14 shows an example of an operational amplifier configuration.

No load current flows through the dividing resistors because of the high input impedance of the operational amplifiers. A high resistance of R = 10 kΩ and VR = 50 kΩ can be used.

3.3 Generation of Liquid Crystal Drive Levels in LSI

The power supply circuit for liquid crystal drive level may be incorporated in the LSI, such as one for a portable calculator with liquid crystal display.
HD61602, HD61603 for small display systems has a built-in power suply circuit for liquid crystal drive levels.

3.4 Precaution on Power Supply Circuits

The LCD driver LSI has two types of power supplies: the one for logical circuits and the other for the liquid crystal display drive circuit. The power supply system is complicated because of several liquid crystal drive levels. For this reason, in the power supply design, take care not to deviate from the voltage range assured in the maximum rating at the rise of power supply and from the potential sequence of each power supply. If the input terminal level is indefinite, through current flows and the power consumption increases because of the use of CMOS process in the LCD driver.
Simultaneously, the potential sequence of each power supply becomes wrong, which may cause latch-up.

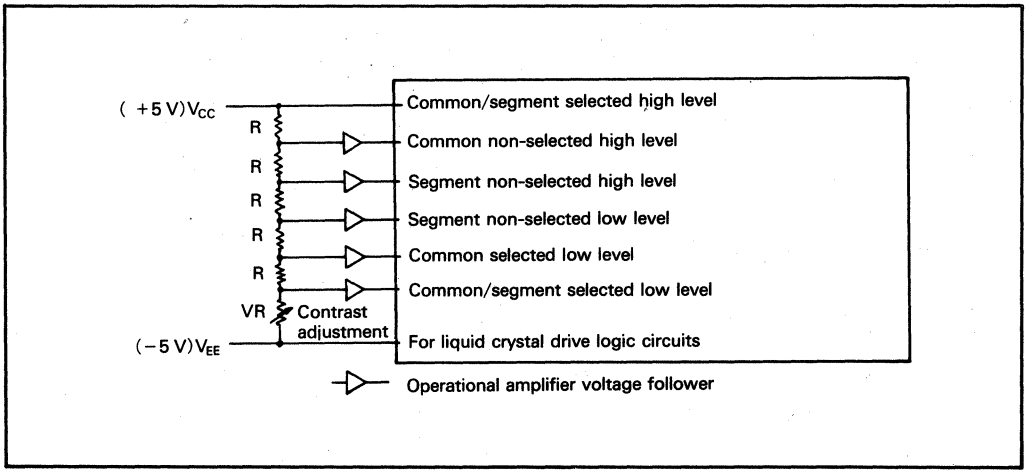


Figure 14 Drive by Operational Amplifier (1/5 bias)

LCD CONTROLLER/DRIVER LSI DATA BOOK

DATA SHEETS

Section Three

3

General Type LCD Driver

HD44100H
(LCD Driver with 40-Channel Outputs)

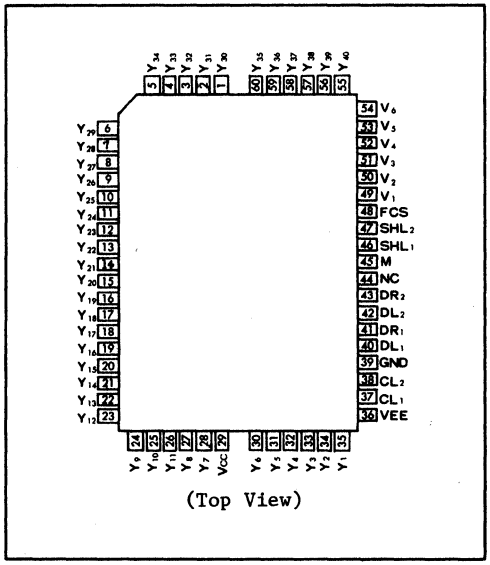
Description

The HD44100H has two sets of 20-bit bidirectional shift registers, 20 data latch flipflops and 20 liquid crystal display driver circuits. It receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.
The HD44100H is a highly general liquid crystal display driver which can drive a static drive liquid crystal and a dynamic drive liquid crystal, and can be applied as a common driver or segment driver.

Features

- Liquid crystal display driver with serial/parallel conversion function
- Serial transfer facilitates board design
- Capable of interfacing to liquid crystal display controllers: HD43160AH, LCTC (HD61830), LCD II(HD44780), LCDIII(HD44790).
- 40 internal liquid crystal display drivers
- Internal serial/parallel conversion circuits:
  —20-bit shift register × 2
  —20-bit shift latch × 2
- Display bias: Static to 1/5
- Power supply:
  —Internal logic: + 5 V
  —Liquid crystal display driver circuit: − 5 V
- Separation of internal logic from liquid crystal display driver circuit increases applicable controllers and liquid crystal types
- CMOS process
- 60-pin flat plastic package

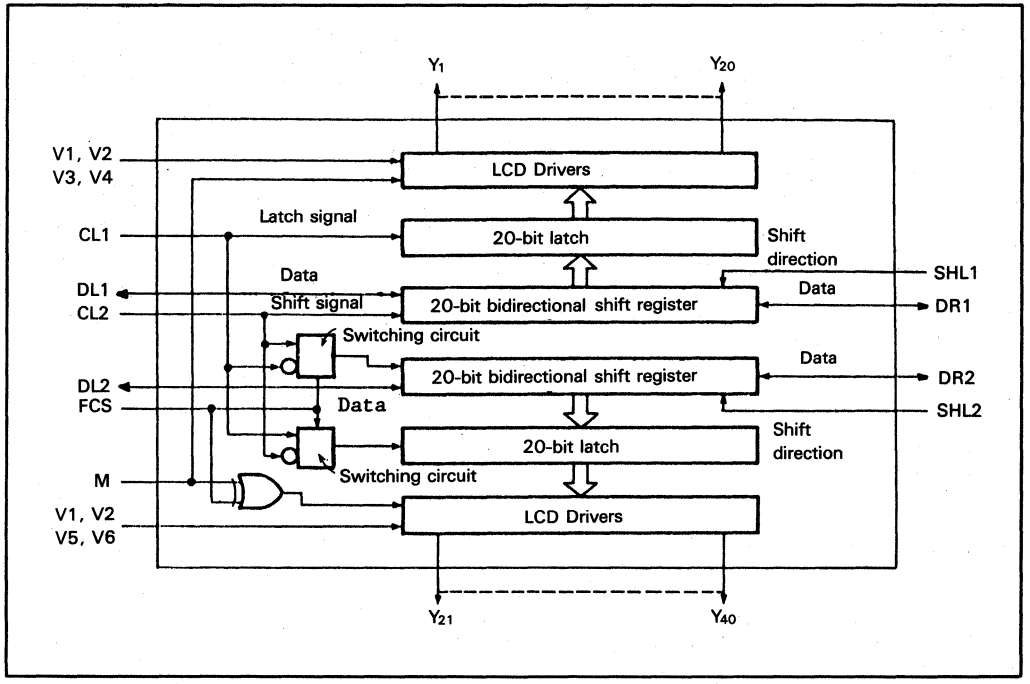
Pin Arrangement



(Top View)

3

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Value	Unit
Supply voltage	Logic	V_{CC} *1	− 0.3 to + 7.0	V
	LCD drivers	V_{EE} *2	V_{CC} − 13.5 to V_{CC} + 0.3	V
Input voltage		V_{T1} *1	− 0.3 to V_{CC} + 0.3	V
Input voltage		V_{T2} *3	V_{CC} + 0.3 to V_{EE} − 0.3	V
Operating temperature		T_{opr}	− 20 to + 75	°C
Storage temperature		T_{stg}	− 55 to + 125	°C

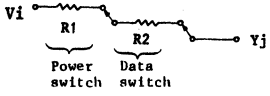
Notes: *1 All voltage values are referred to GND.
*2 Connect a protection resistor of 220 Ω ± 5 % to V_{EE} power supply in series.
*3 Applies to V_1 to V_6.

Electrical Characteristics

(V_{CC} = 5 V ± 10 %, V_{EE} = − 5 V ± 10 %, GND = 0 V, T_a = − 20 to + 75°C)

Item	Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Input voltage	V_{IH}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1,	0.7 V_{CC}	—	V_{CC}	V	
	V_{IL}	SHL2, FCS	0	—	0.3 V_{CC}	V	
Output voltage	V_{OH}	DL1, DL2, DR1, DR2	V_{CC} − 0.4	—	—	V	I_{OH} = − 0.4 mA
	V_{OL}		—	—	0.4	V	I_{OL} = + 0.4 mA
Vi-Yj voltage descending	V_{D1}	*1	—	—	1.1	V	I_{ON} = 0.1 mA for one of Yj
	V_{D2}		—	—	1.5	V	I_{ON} = 0.05 mA for each Yj
Input leakage current	I_{IL}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS, NC	− 5.0	—	5.0	μA	V_{in} = 0 to V_{CC}
Vi leakage current	I_{VL}	*3	− 10.0	—	10.0	μA	V_{in} = V_{CC} to V_{EE}
Power supply current	I_{CC}	*2	—	—	1.0	mA	f_{CL2} = 400 kHz
	I_{EE}		—	—	10	μA	f_{CL1} = 1 kHz

Notes: *1 Vi-Yj (Vi = 1 to 6, j = 1 to 40) equivalent circuit



R1 = 1 kΩ max.
R2 = 10 kΩ max.

*2 Input/output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

*3 Output Y1 to Y40 open.

3

Timing Characteristics

(V_{CC} = 5 V ± 10 %, V_{EE} = − 5 V ± 10 %, GND = 0 V, T_a = − 20 to + 75°C)

Item	Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Data shift frequency	f_{CL}	CL2	—	—	400	kHz	
Clock high level	t_{CWH}	CL1, CL2	800	—	—	ns	
width Low level	t_{CWL}	CL2	800	—	—	ns	
Data set-up time	t_{SU}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	
Clock set-up time	t_{SL}	CL1, CL2	500	—	—	ns	(CL2→CL1)
Clock set-up time	t_{LS}	CL1, CL2	500	—	—	ns	(CL1→CL2)
Data delay time	t_{pd}	DL1, DL2, DR1, DR2	—	—	500	ns	C_L = 15 pF
Clock rise/fall time	t_{ct}	CL1, CL2	—	—	200	ns	
Data hold time	t_{DH}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	

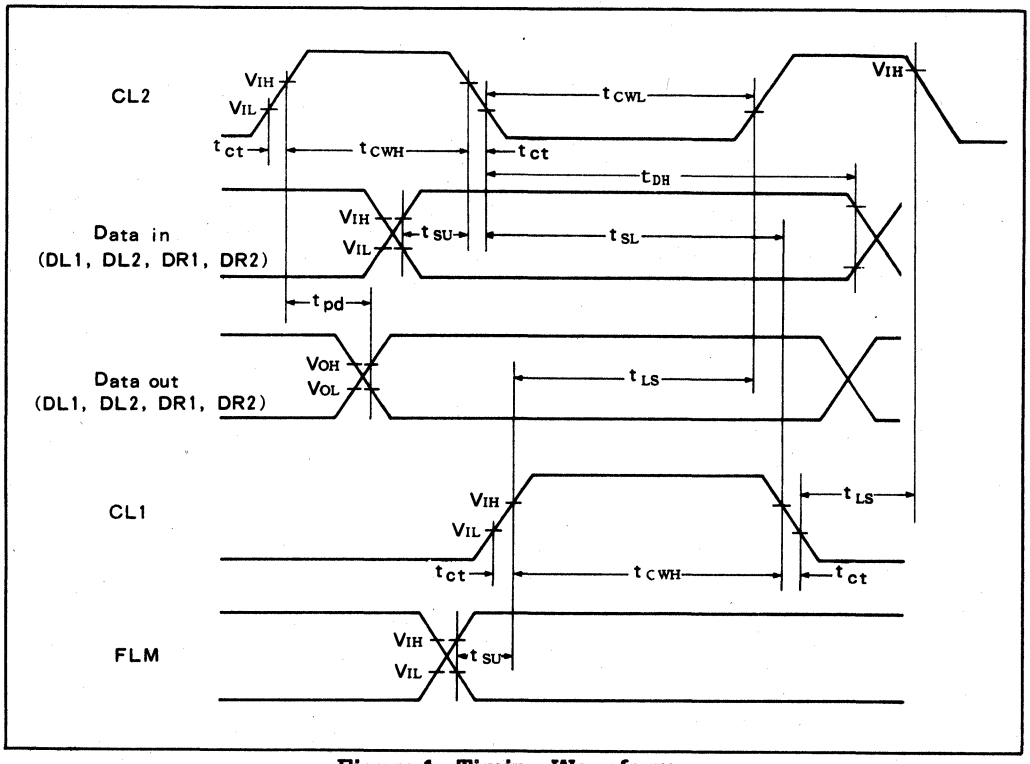


Figure 1 Timing Waveform

Terminal Function

Table 1 Functional Description of Terminals

Signal Name	Number of Lines	Input/ Output	Connected to	Function
V_{CC}	1		power supply	Power supply for logical circuit
GND	1		Power supply	0 V
V_{EE}	1		Power supply	Power supply for liquid crystal display drive
Y_1—Y_{20}	20	Output	Liquid crystal	Liquid crystal driver output (Channel 1)
Y_{21}—Y_{40}	20	Output	Liquid crystal	Liquid crystal driver output (Channel 2)
V_1, V_2	2	Input	Power supply	Power supply for liquid crystal display drive (Select level)
V_3, V_4	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 1)
V_5, V_6	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 2)
SHL1	1	Input	V_{CC} or GND	Selection of the shift direction of channel 1 shift register SHL1 / DL1 / DR1 V_{CC} / Out / In GND / In / Out
SHL2	1	Input	V_{CC} or GND	Selection of the shift direction of channel 2 shift register SHL2 / DL2 / DR2 V_{CC} / Out / In GND / In / Out
DL1, DR1	2	Input/ output	Controller or HD44100H	Data input/output of channel 1 shift register
DL2, DR2	2	Input/ output	Controller or HD44100H	Data input/output of channel 2 shift register
M	1	Input	Controller	Alternated signal for liquid crystal driver output
CL1	1	Input	Controller	Latch signal for channel 1 (⌐‾_) *1 Used for channel 2 when FCS is GND
CL2	1	Input	Controller	Shift signal for channel 1 (⌐‾_) *1 Used for channel 2 when FCS is GND
FCS	1	Input	V_{CC} or GND	Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift signal of channel 2 and inverts M for channel 2. Thus, this signal exchanges the function of channel 2.

	Channel 2			
FCS Level	Latch signal	Shift signal	M Polarity	Function
V_{CC}	CL2 _⌐‾_ *1	CL1 _⌐‾_ *1	$\overline{M}$	For common drive
GND	CL1 ‾_ *1	CL2 ‾_ *1	M	For segment drive

NC	1			Don't connect any wires to this terminal.

Notes: *1 _⌐‾_ and ‾_ indicate the latches at rise and fall times, respectively.
*2 The output level relationship between channel 1 and channel 2 based on the FCS signal level is as follows:

FCS	Data	M	Output Level: Channel 1 (Y_1—Y_{20})	Output Level: Channel 2 (Y_{21}—Y_{40})
	1	1	V_1	V_2
V_{CC}	(Select)	0	V_2	V_1
(1)	0	1	V_3	V_6
	(Non-select)	0	V_4	V_5
	1	1	V_1	V_1
GND	(Select)	0	V_2	V_2
(0)	0	1	V_3	V_5
	(Non-select)	0	V_4	V_6

1 and 0 indicate high and low levels, respectively.

Applications

Segment Driver

When the HD44100H is used as a segment driver, FCS is set to GND to transfer display data with the timing shown in figure 2. In this case, both channel 1 and channel 2 shift data at the fall of CL2 and latch it at the fall of CLI. V_3 and V_5, V_4 and V_6 of the liquid crystal display driver power supply are short-circuited, respectively.

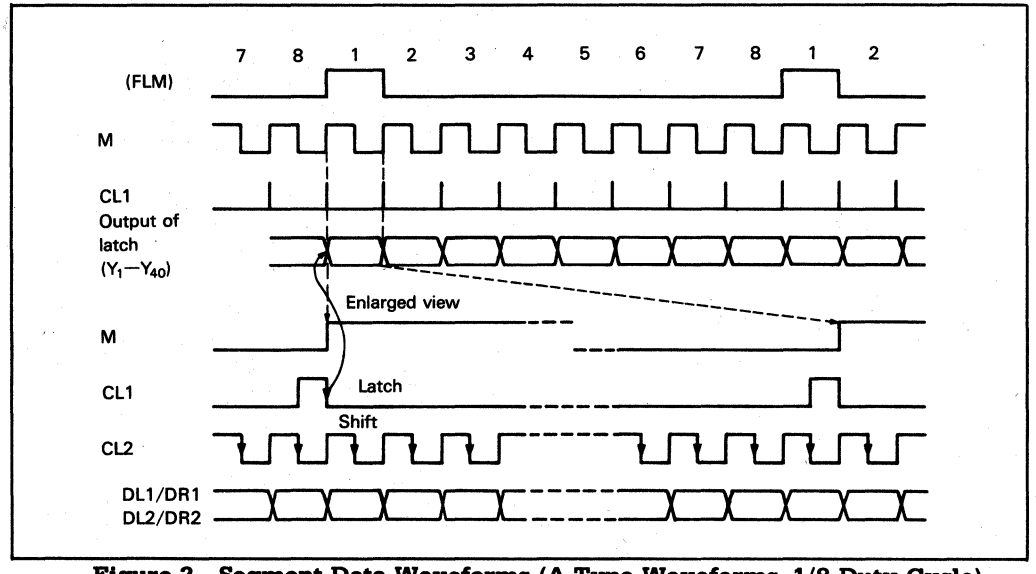


Figure 2 Segment Data Waveforms (A Type Waveforms, 1/8 Duty Cycle)

Common Driver

In this case, channel 1 is used as a segment driver and channel 2 as common driver. When channel 2 of HD44100H is used as common driver, FCS is set to V_{CC} to transfer display data with the timing shown in figure 3.

In this case, channel 2 shifts data at the rise of CL1 and latches it at the rise of CL2. Channel 1 shifts and latches as shown in figure 2.

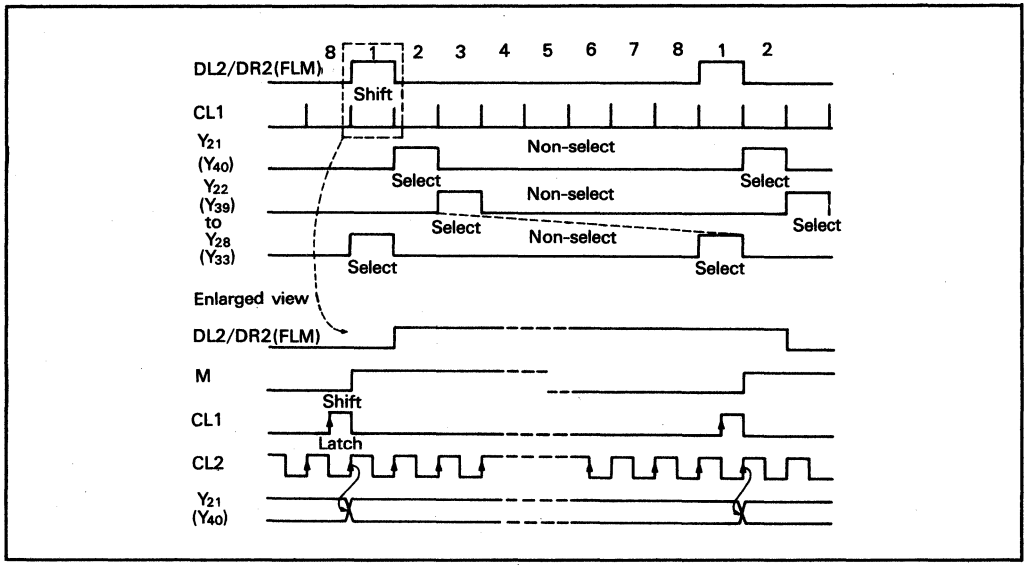


Figure 3 Common Data Waveforms (A Type Waveforms of Channel 2, 1/8 Duty Cycle)

Both Channel 1 and Channel 2 Used as Common Drivers (FCS = GND)

When both of channel 1 and channel 2 of HD44100H are used common drivers, FCS is set to GND and the signals (CL1, CL2, FLM) from the controller are connected as shown in figure 4.
In this case, connection of the liquid crystal display driver power supply is different from that of segment driver, so refer to figure 4.

- V_1, V_2: Select level of segment and common
- V_3, V_4: Non-select level of segment
- V_5, V_6: Non-select level of common

Static Drive

When the HD44100H is used in the static drive method (figure 5), data is transferred at the fall of CL2 and latched at the fall of CL1. The frequency of CL1 becomes the frame frequency of the liquid crystal display driver. The signal applied terminal M must have twice the frequency of CL1 and be synchronized at the fall of CL1. The power supply for liquid crystal display driver is used by short-circuiting V_1, V_4 and V_6, and V_2, V_3, and V_5 respectively.
One of the liquid crystal display driver output terminals can be used for a common output. In this case, FCS is set to GND and data is transferred so that 0 can be always latched in the latch corresponding to the liquid crystal display driver output terminal used as the common output. If the latch signal corresponding to the segment output is 1, the segments of LCD light. They also light for common side = 1, and segment side 0.

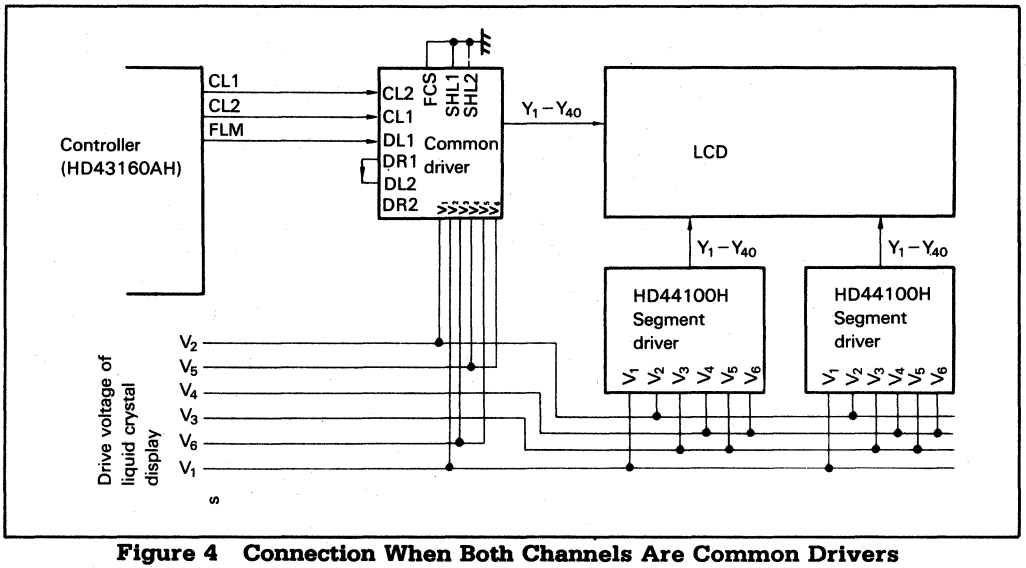


Figure 4 Connection When Both Channels Are Common Drivers

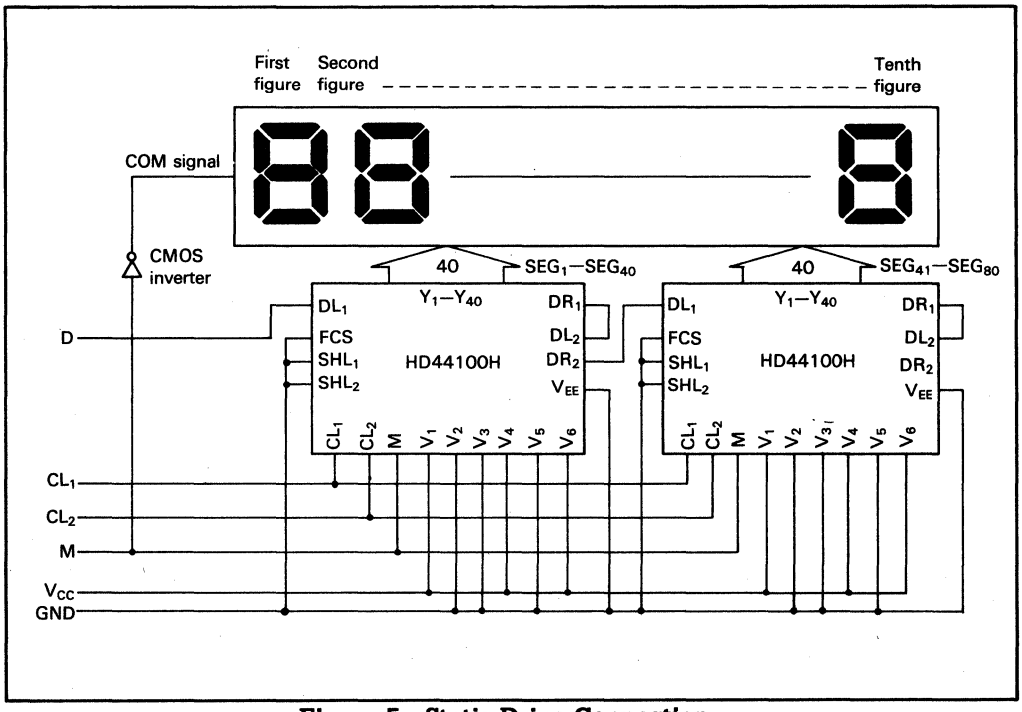
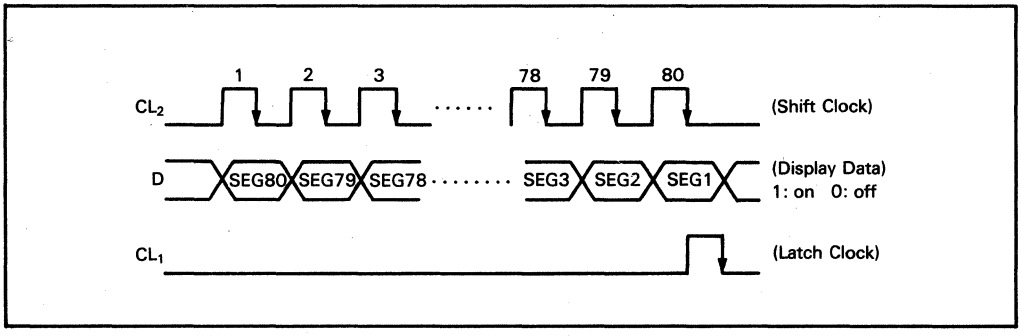


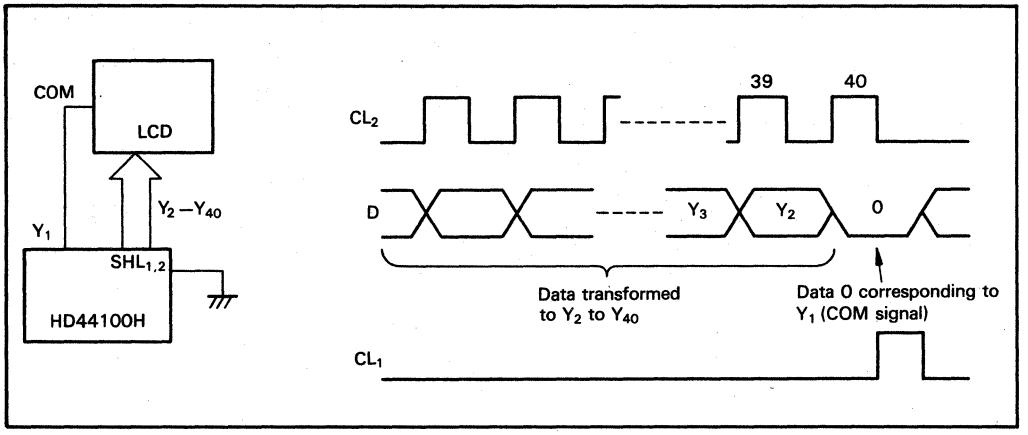
Figure 5 Static Drive Connection

Timing Chart of Input Waveforms



Notes:

1. Input square waves of 50% duty cycle (about 30—500 Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, have CL1 fall synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
   Usually, one of the HD44100H outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.


COM
LCD
$Y_2 - Y_{40}$
Y_1
$SHL_{1,2}$
HD44100H
CL_2
39
40
D
Y_3
Y_2
0
Data transformed to Y_2 to Y_{40}
Data 0 corresponding to Y_1 (COM signal)
CL_1

HD66100F

(LCD Driver with 80-Channel Outputs)

The HD66100 description segment driver with 80 LCD drive circuits is the improved version of the no longer current HD44100H LCD driver with 40 circuits.
It is composed of a shift register, an 80-bit latch circuit, and 80 LCD drive circuits. Its interface is compatible with the HD44100H.
It reduces the number of LSI's and lowers the cost of an LCD module.

Features

- LCD driver with serial/parallel converting function
- Interface compatible with the HD44100H; connectable with HD43160AH, HD61830, HD61830B, LCD-II (HD44780), LCD-III (HD44790)
- Internal output circuits for LCD drive: 80
- Internal serial/parallel converting circuits:
  —80-bit bidirectional shift register
  —80-bit latch circuit
- Power supply
  —Internal logic circuit: +5 V ±10%
  —LCD drive circuit: 3.0 V to 6.0 V
- CMOS process
- 100-pin plastic QFP (FP-100)

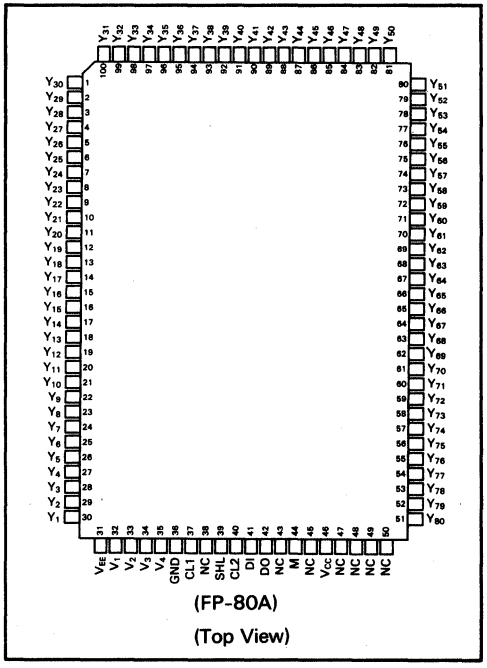
Comparison with HD44100H

Table 1 shows the main differences between HD66100 and HD44100H.

Table 1 Comparison of HD66100 and HD44100H

	HD66100	HD44100H
LCD Drive Outputs	80×1 Channel	20×2 channels
Supply Voltage for LCD Drive Circuits	3 to 6 V	4.5 to 11 V
Multiplexing Duty Ratio	Static to 1/16 duty	static to 1/32 duty
Package	100-pin flat plastic package	60-pin flat plastic package

Pin Arrangement



(FP-80A)

(Top View)

3

Pin Description

V_{CC}, GND, V_{EE}: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground. V_{EE} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1 to V_4 supply power for driving an LCD (figure 2).

CL1: HD66100 latches data at the negative edge of CL1.

CL2: HD66100 receives shift data at the negative edge of CL2.

M: Changes LCD drive outputs to AC.

DI: Inputs data to the shift register.

DO: Output data from the shift register.

SHL: Selects a shift direction of serial data. When the serial data is input in order of D_1, D_2, ..., D_{79}, D_{80}, the relation between the data and the output Y is shown in table 3.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels-V_1, V_2, V_3, or V_4-according to the combination of M and display data (figure 2).

NC: Do not connect any wire to these terminals.

Table 2 Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	46	V_{CC}	–
GND	36	Ground	–
V_{EE}	31	V_{EE}	–
V_1	32	V_1	–
V_2	33	V_2	–
V_3	34	V_3	–
V_4	35	V_4	–
CL1	37	Clock 1	I
CL2	40	Clock 2	I
M	44	M	I
DI	41	Date In	I
DO	42	Date Out	O
SHL	39	Shift Left	I
Y_1-Y_{80}	1-30,51-100	Y_1-Y_{80}	O
NC	38,43,45,47-50	No Connection	–

Table 3 Relation Between SHL and Data Output

SHL	Y_1	Y_2	Y_3.....	Y_{79}	Y_{80}
High	D1	D2	D3.....	D79	D80
Low	D80	D79	D78.....	D2	D1

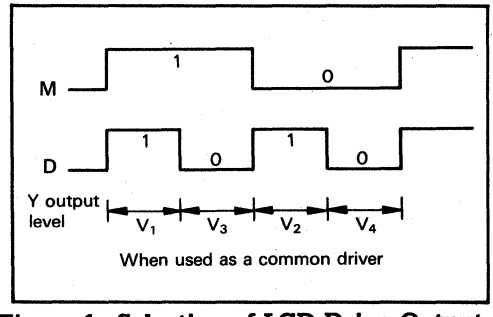


Figure 1 Selection of LCD Drive Output

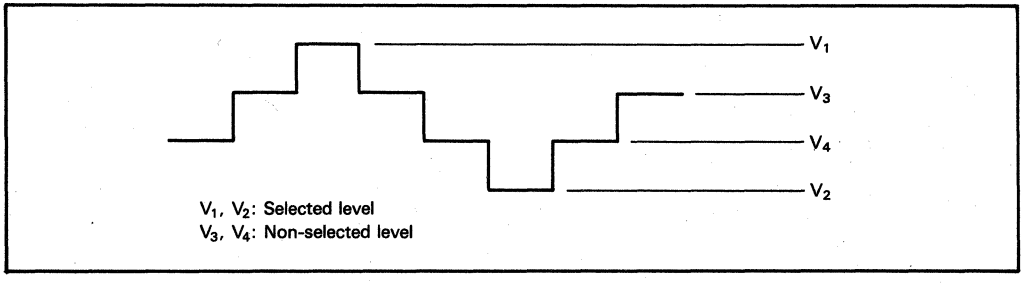


Figure 2 Power Supply for Driving an LCD

Block Functions

LCD Drive Circuits

Select one of four levels of voltage V_1, V_2, V_3, and V_4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

Latch Circuit

Latches the data input from the bidirectional shift register at the fall of CL1 and transfer its outputs to the LCD drive circuits.

Bidirectional Shift Reigster

Shifts the serial data at the fall of CL2 and transfers the output of each bit of the register to the latch circuit. When SHL = GND, the data input from DI shifts from bit 1 to bit 80 in order of entry. On the other hand, when SHL = V_{CC}, the data shifts from bit 80 to bit-1. In both cases, the data of the last bit of the register is latched to be output from DO at the rise of CL2.

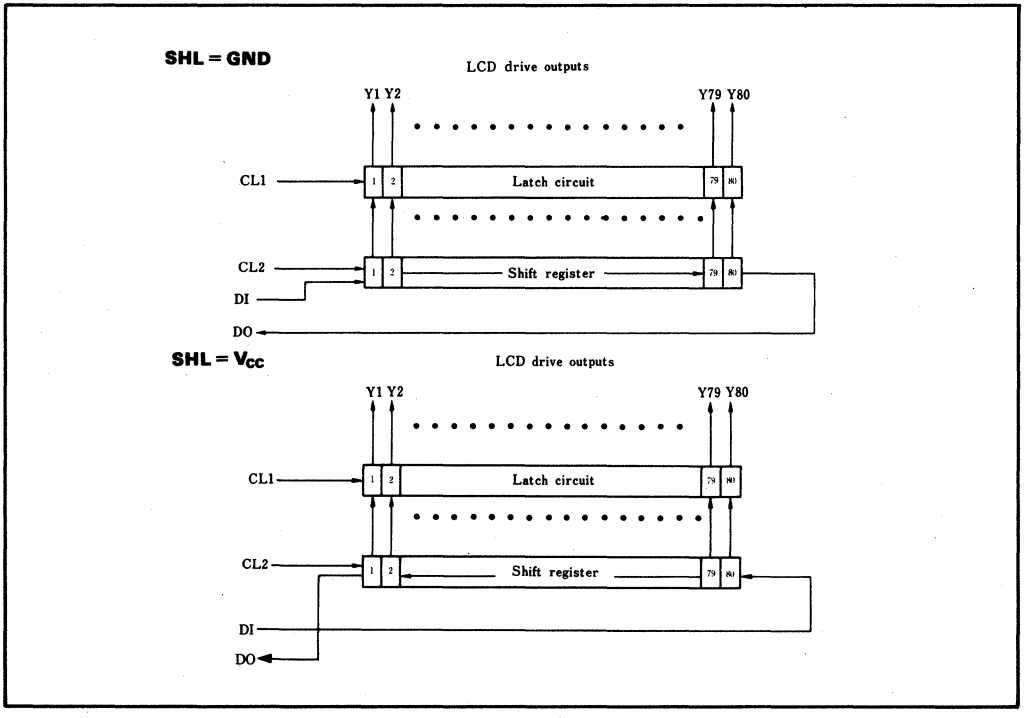


Figure 3 Relation between SHL and the Shift Direction

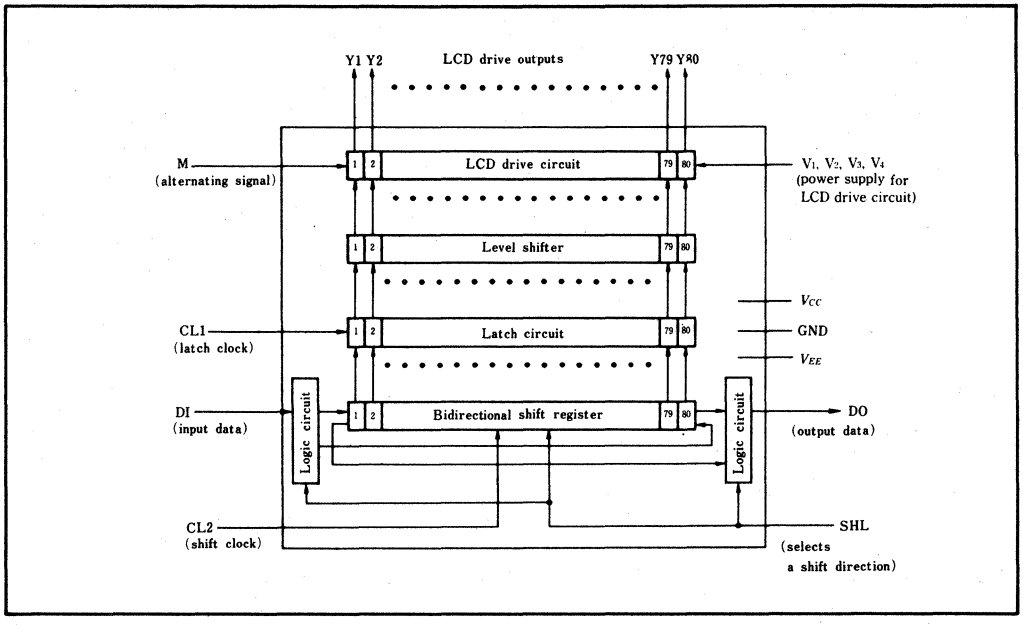


Figure 4 Block Diagram

Primary Operations

Shifting Data

The input data DI shifts at the fall of CL2 and the data delayed 80 bits by the shift register is output from the DO terminal. The output of DO changes synchronously with the rise of CL2. This operation is completely unaffected by the latch clock CL1.

Latching Data

The data of the shift register is latched at the negative edge of the latch clock CL1. Thus, the outputs Y_1-Y_{80} change synchronously with the fall of CL1.

Switching Data Shift Direction

When the shift direction switching signal SHL is connected with GND, the data D80, immediately before the negative edge of CL1, is output from the output terminal Y_1. When SHL is connected with V_{CC}, it is output from Y_{80}.

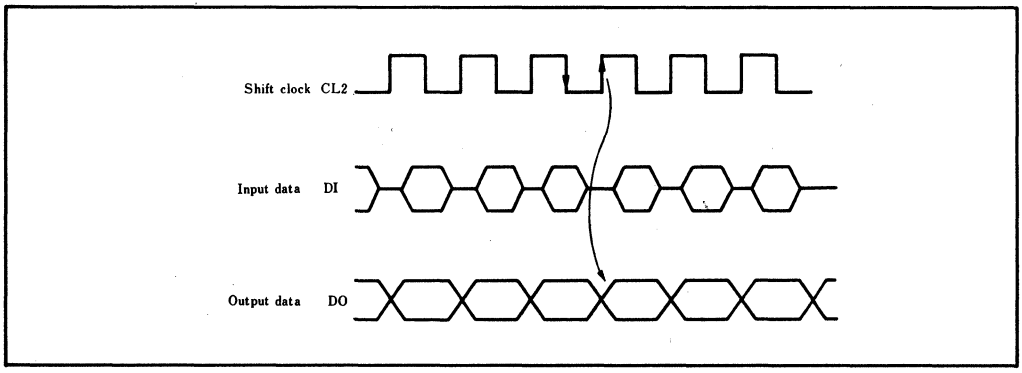


Figure 5 Timing of Receiving and Outputting Data

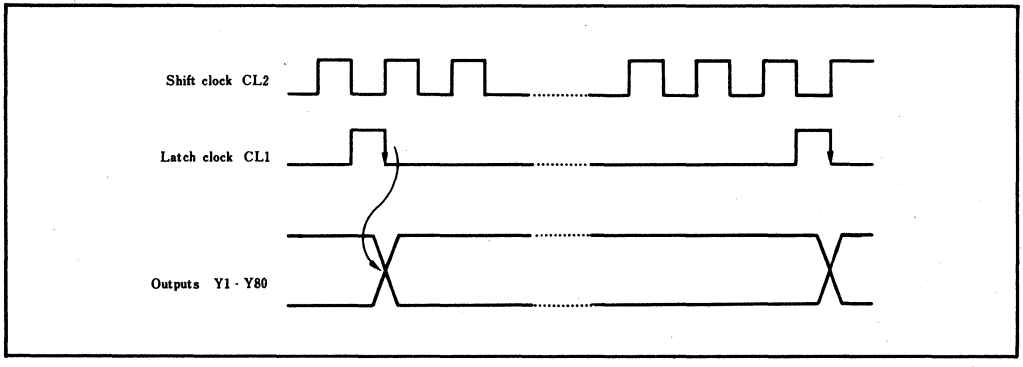


Figure 6 Timing of Latching Data

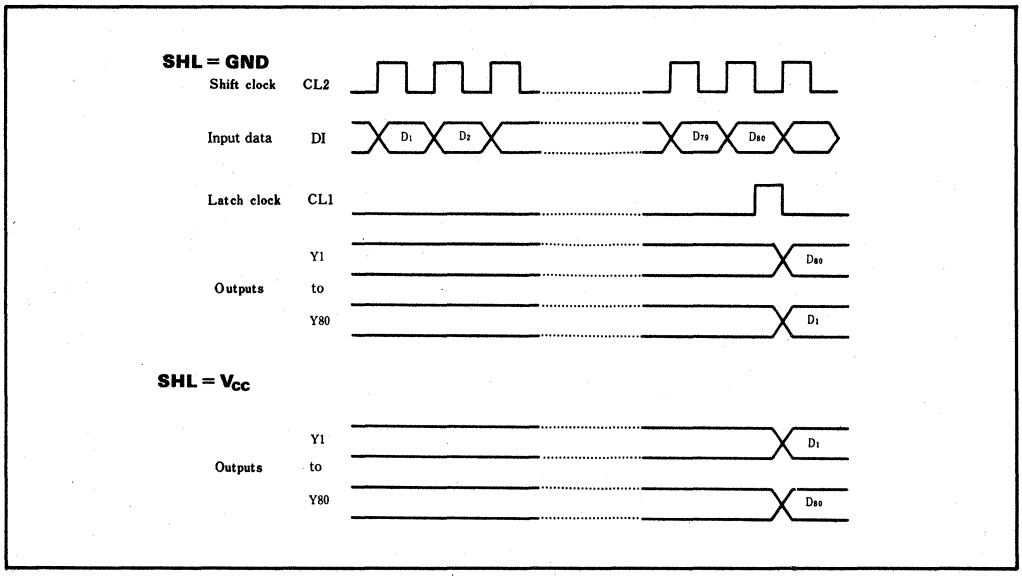


Figure 7 SHL and Waveforms of Data Shift

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Supply Voltage	Logic Circuits	V_{CC}	−0.3 to +7.0	V	*1
	LCD Drive Circuits	V_{CC}—V_{EE}	−0.3 to +7.0	V	
Input Voltage (1)		V_{T1}	−0.3 to V_{CC} + 0.3	V	*1
Input Voltage (2)		V_{T2}	V_{CC} + 0.3 to V_{EE} − 0.3	V	*2
Operation Temperature		T_{opr}	+20 to +75	°C	
Storage Temperature		T_{stg}	−55 to +125	°C	

*1 A reference point is GND (= 0 V)
*2 Applies to $V_1 - V_4$.
Note: If used beyond the absolute maximum ratings, LSIs may be permanently destroyed. It is best to use them at the electrical characteristics for normal operations. If they are not used at these conditions, it may affect the reliability of the device.

3

Electrical Characteristics

DC Characteristics

(V_{CC} = 5 V ± 10%, $V_{CC}-V_{EE}$=3.0 to 6.0 V, GND = 0 V, T_a = −20 to +75°C)

Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Test condition	Note
Input High Voltage	V_{IH}	CL1, CL2	0.8 × V_{CC}	–	V_{CC}	V		
Input Low Voltage	V_{IL}	M, DI, SHL	0	–	0.2 × V_{CC}	V		
Output High Voltage	V_{OH}	DO	V_{CC}−0.4	–	–	V	I_{OH} = −0.4 mA	
Output Low Voltage	V_{OL}		–	–	0.4	V	I_{OL} = +0.4 mA	
On Resistance Vi-Vj	R_{ON1}	Y_1-Y_{80}	–	–	11	kΩ	I_{ON} = 0.1 mA to one Y terminal	
	R_{ON2}	V_1-V_4	–	–	30	kΩ	I_{ON} = 0.05 mA to each Y terminal	
Input Leakage Current	I_{IL}	CL1, CL2, M, DI, SHL	−5.0	–	5.0	μA	V_{in} = 0 V to V_{CC}	
Vi Leakage Current	I_{VL}	V_1-V_4	−5.0	–	5.0	μA	Output Y_1-Y_{80} open V_{in} = V_{CC} to V_{EE}	
Current Dissipation	I_{GND}		–	–	2.0	mA	f_{CL2} = 1.0 MHz	*1
	I_{EE}		–	–	0.1	mA	f_{CL1} = 2.5 kHz	

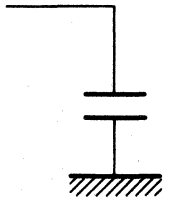
*1 Input/output currents are excluded; when an input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit.
To avoid this, V_{IH} and V_{IL} must be fixed at V_{CC} and GND level respectively.

AC Characteristics

(V_{CC} = 5 V ± 10%, $V_{CC}-V_{EE}$ = 3.0 to 6.0 V, GND = 0 V, T_a = −20 to +75°C)

Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Note
Data Shift Frequency	f_{CL}	CL2	–	–	1	MHz	
Clock High level Width	t_{CWH}	CL1,CL2	450	–	–	ns	
Clock Low level Width	t_{CWL}	CL2	450	–	–	ns	
Data Set-Up Time	f_{SU}	DI	100	–	–	ns	
Clock Set-Up Time (1)	t_{SL}	CL2	200	–	–	ns	*1
Clock Set-Up Time (2)	t_{LS}	CL1	200	–	–	ns	*2
Output Delay Time	t_{pd}	DO	–	–	250	ns	*3
Data Hold Time	t_{DH}	DI	100	–	–	ns	
Clock Rise/Fall Time	f_{CT}	CL1,CL2	–	–	50	ns	

*1 Set-up time from the fall of CL2 to that of CL1.
*2 Set-up time from the fall CL1 to that of CL2.
*3 Test terminal



C_L (Load capacitance on outputs) = 30pF
(Including jig capacitance)

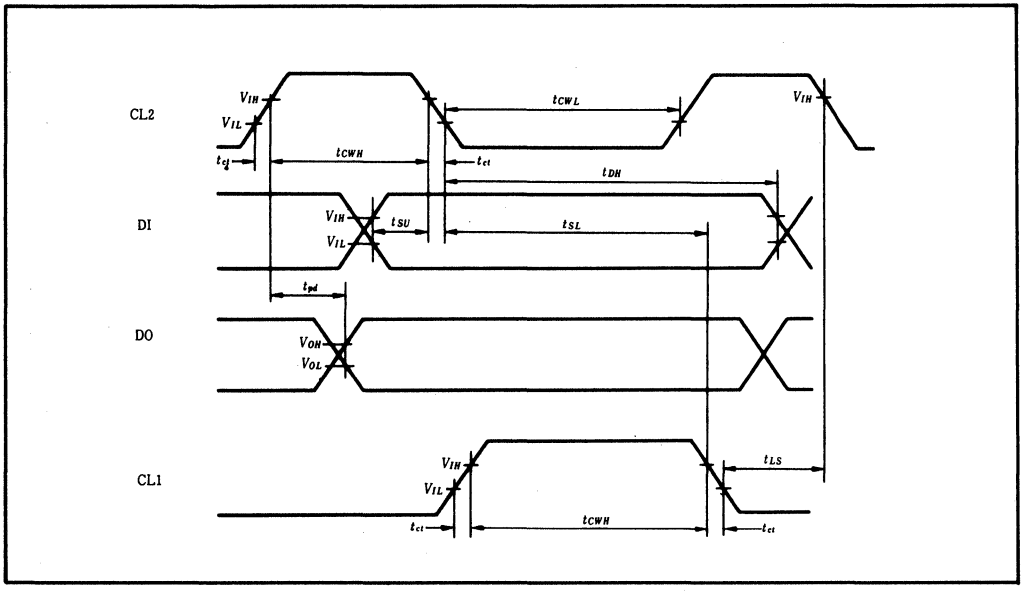


Figure 8 Timing Chart of HD66100F

3

Typical Applications

Connection with the LCD Controller HD44780

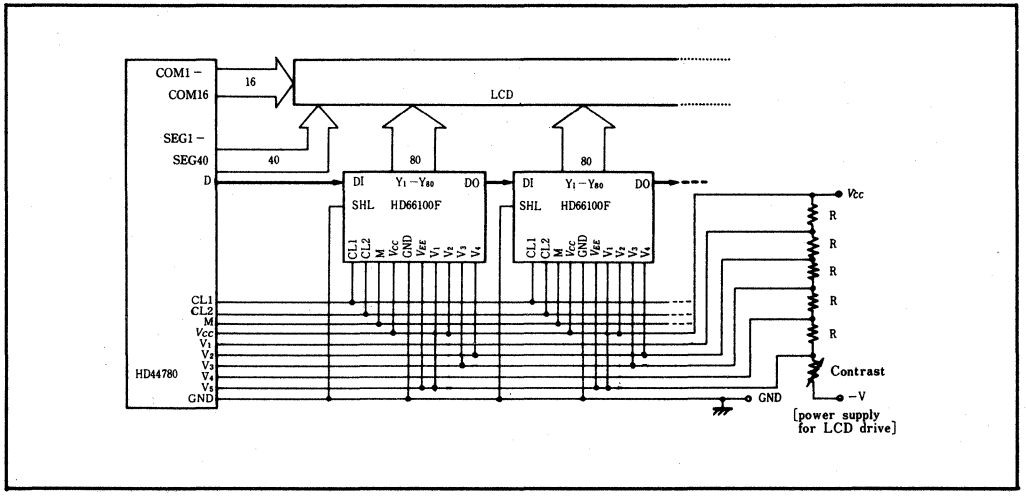


Figure 9 Example of Connection (1/16 duty cycle, 1/5 bias)

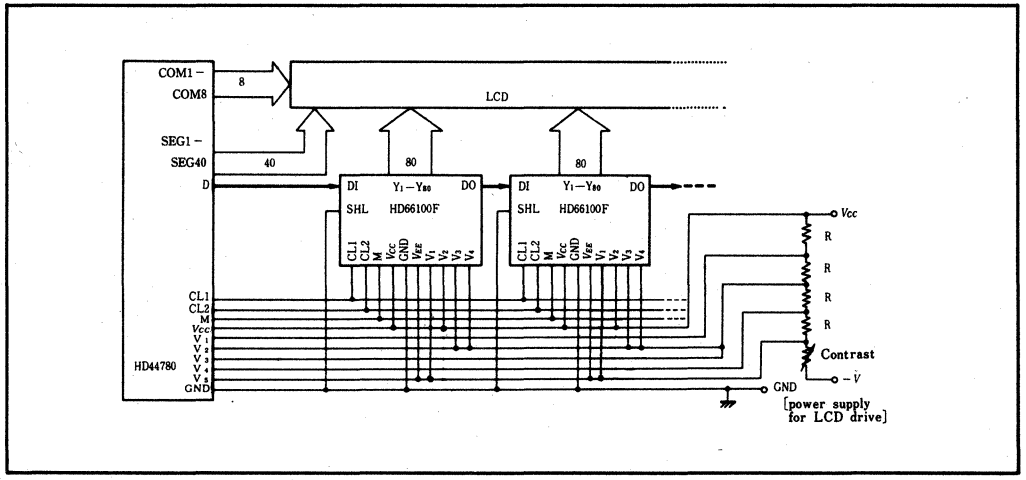


Figure 10 Example of Connection (1/8 duty cycle, 1/4 bias)

Connection with LCD III (HD44790)

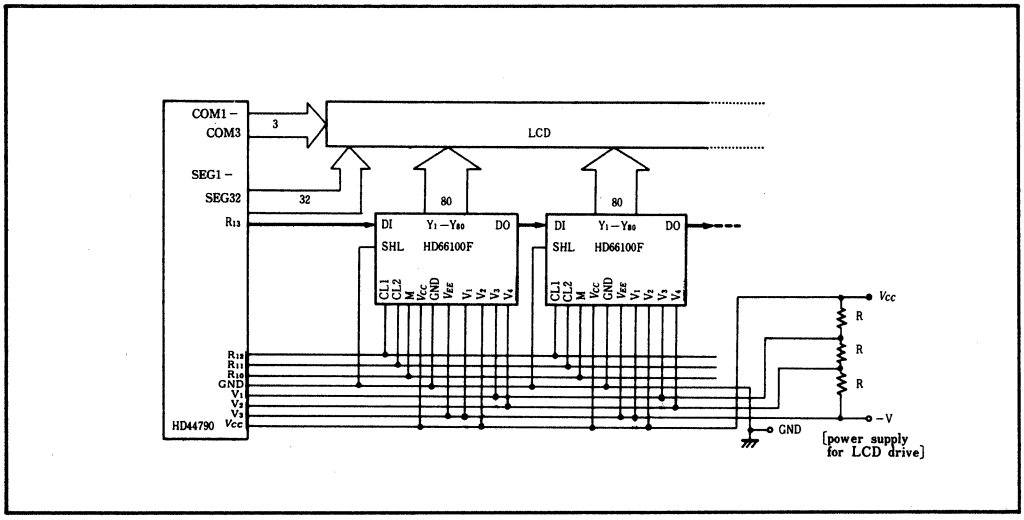


Figure 11 Example of Connection (1/3 duty cycle, 1/3 bias)

3

Static Drive

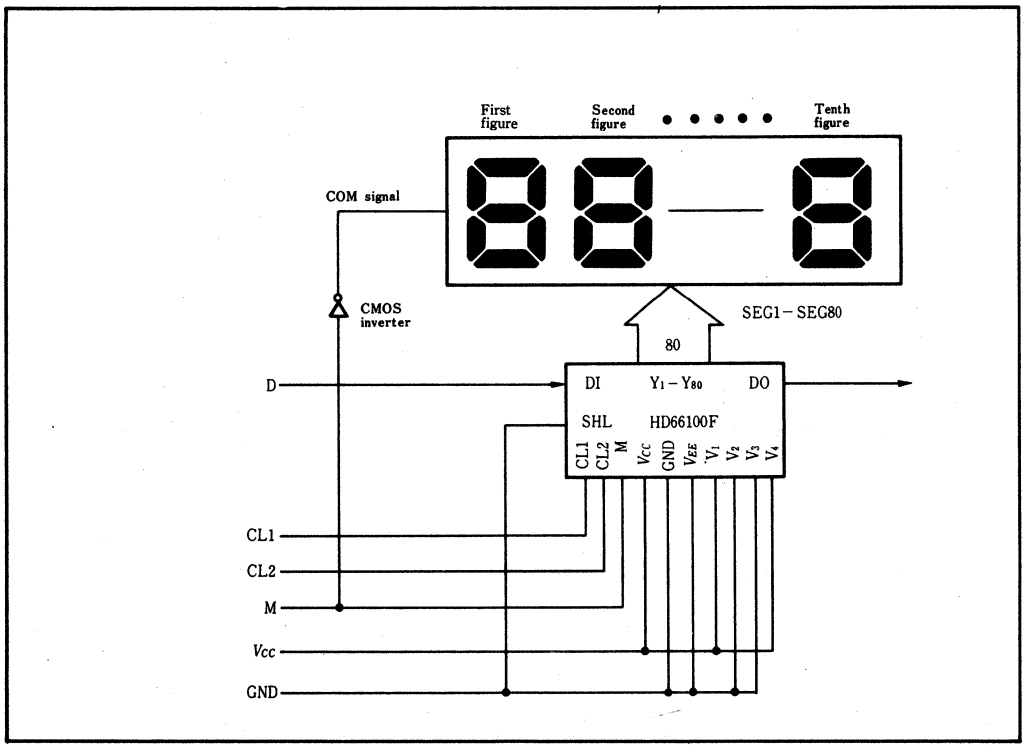


Figure 12 Example of Connection (80-segment display)

- **Timing Chart of Input Waveforms**

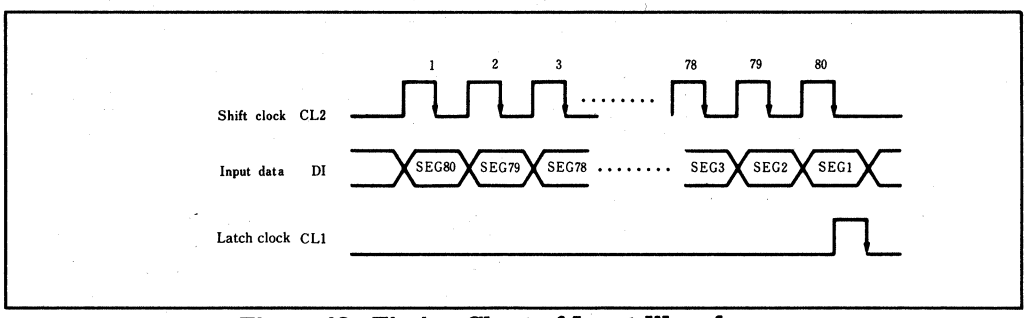


Figure 13 Timing Chart of Input Waveforms

Notes:

1. Input square waves of 50% duty cycle (about 30-500Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, make CL1 fall synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
   Usually, one of the HD66100F outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.

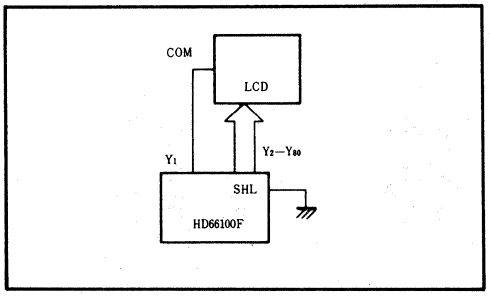


Figure 14 Example of Connection

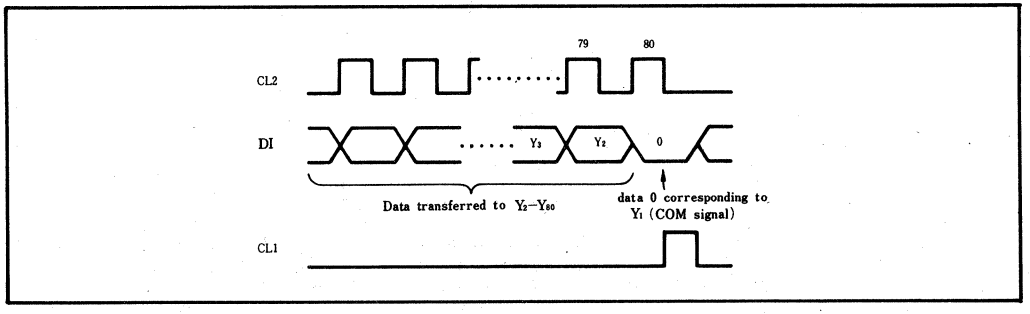


Figure 15 Timing Chart (when Y_1 is used as a COM signal)

Section Four

Character Display LCD Controller/Display

HD43160AH
(Controller with Built in Character Generator)

For Maintenance Only

For new designs please see data sheet for HD44780SA00H

Display Controller and Character Generator for Dot Matrix Liquid Crystal Display System

The HD43160AH receives character data written in ASCII code or JIS code from a microcomputer and stores them in its RAM which has 80 words capacity.

The HD43160AH converts these data into a serial character pattern, then transfers them to LCD drivers.

It also generates other control signals for the LCD. The HD44100H LCD driver can be combined with this controller.

Display Characters Types

- Alphanumeric characters: A-Z, a-z, @, #, %, &, etc.
- Japanese characters (katakana)
- 160 characters in internal character generator (ROM)
  (Max 256 characters in external ROM)

Number Of Characters

- 4, 8, 16, 24, 32, 40, 64, or 80 characters in 1 or 2 lines

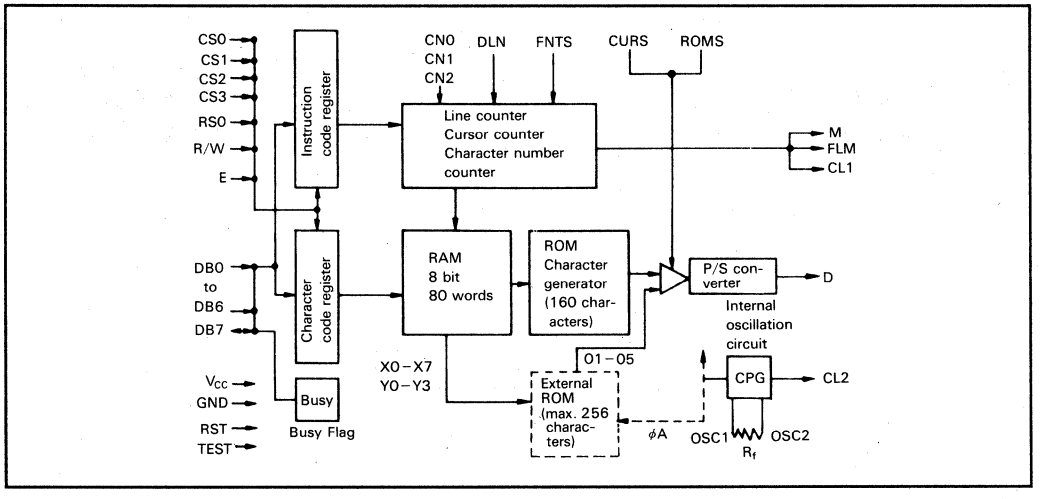
Font

- 5 × 7 + Cursor or 5 × 11 + Cursor

Other Function Controlled By Microcomputer

- Display clear
- Cursor on/off
- Cursor position preset (character position)
- Cursor return

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_T	−0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−55 to +125	°C

Electrical Characteristics (V_{CC} = 5 V ± 5%, GND = 0 V, Ta = −20 to+75°C)

Item	Symbol	Terminal No.	min	typ	max	Unit	Test condition
Input voltage (TTL compatible)	V_{IH}	CS0—CS3, E, R/W, DB0—DB7, RS0	2.0	–	V_{CC}	V	
	V_{IL}		0	–	0.8	V	
Input voltage	V_{IHC}	OSC1, TEST, RST, FNTS, CURS, DLN, ROMS, CN0—CN2, O_1—O_5	0.7 V_{CC}	–	V_{CC}	V	
	V_{ILC}		0	–	0.3 V_{CC}	V	
Output voltage (TTL compatible)	V_{OH}	DB7	2.4	–	–	V	I_{OH} = −0.205 mA
	V_{OL}		–	–	0.4	V	I_{OL} = 1.6 mA
Output voltage	V_{OHC}	FLM, M, D, CL1, CL2, X0—X7, Y0—Y3	V_{CC}−1.0	–	–	V	I_{load} = ±0.4 mA
	V_{OLC}		–	–	1.0	V	
Input leak current	I_{LI}	All inputs	−5	–	5	μA	
Output leak current	I_{LO}	DB7	−10	–	10	μA	
Oscillation frequency	f_{CP1}		130	192	250	kHz	R_f = 200 kΩ ±2%, 5 × 7 + Cursor
	f_{CP2}		200	288	375	kHz	R_f = 130 kΩ ±2%, 5 × 11 + Cursor
Input pull up current	I_{PL}	CS0—CS3, RS0, R/W, DB0—DB7	2	10	20	μA	V_{in} = 0V
Power dissipation	P_T	*	–	–	10	mW	Ta = 25°C, f_{CP} = 400 kHz (external clock)

* Input/output current is excluded. When an input is at the intermediate level in CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low, CS0—CS3, RS0, R/W, DB0—DB7.

4

Pin Arrangement

Pin No.	Power sup. OSC	Input	Output
1	GND (−)		
2			X4
3			X3
4			X2
5			X1
6			X0
7			N.C.
8			N.C.
9			N.C.
10		CURS	
11		FNTS	
12		DLN	
13		CN0	
14		CN1	
15		CN2	
16			CL2
17			CL1
18			M

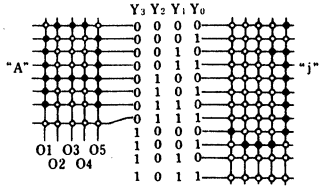
Pin No.	Power sup. OSC	Input	Output
19			D
20			FIM
21			φA
22	OSC1		
23	OSC2		
24		RST	
25		TEST	
26		E	
27	V_{CC}(+)		
28		R/W	
29		RS0	
30		CS0	
31		CS1	
32		CS2	
33		CS3	
34		DB0	
35		DB1	
36		DB2	

Pin No.	Power sup. OSC	Input	Output
37		DB3	
38		DB4	
39		DB5	
40		DB6	
41		DB7	DB7
42		ROMS	
43		O5	
44		O4	
45		O3	
46		O2	
47		O1	
48			Y3
49			Y2
50			Y1
51			Y0
52			X7
53			X6
54			X5

Pin Function

Pin name	Number of terminals	Connected to	I/O	Function
V_{CC} GND	2	Power supply		+5 V ± 10% Power supply 0 V
CN0 CN1 CN2	3	GND or V_{CC}	I	Total displayed character number select
CURS	1	GND or V_{CC}	I	Cursor select V_{CC}: 5 dots ●●●●● GND: 1 dot ●
DLN	1	GND or V_{CC}	I	Display line number select V_{CC}: 2 lines GND: 1 line
FNTS	1	GND or V_{CC}	I	Font select V_{CC}: 5 × 11 + Cursor GND: 5 × 7 + Cursor
RST	1	V_{CC}	I	Only for test. Normally V_{CC}.
TEST	1	GND	I	Only for test. Normally GND.
E	1	MPU	I	Strobe signal Write mode: The HD43160AH latches the data on DB0-DB7 at the falling edge of this signal Read mode: Busy/Ready signal is active on DB7 while this signal is high (Low: Ready, High: Busy)
R/W	1	MPU	I	Read/Write signal L: HD43160AH gets the data from MPU H: MPU gets the Busy/Ready signal from HD43160AH
CS0 CS1 CS2 CS3	4	MPU	I	Chip select When all of CS0—CS3 are 'H', HD43160AH is selected.
RS0	1	MPU	I	Register select HD43160AH has 2 registers. One is for character code and another is for instruction code. Each register latches the data on DB0—DB7 at the falling edge of E, when CS0—CS3 are high and R/W is low. High: Character code register is selected Low: Instruction code register is selected
DB0 to DB7	8	MPU	I I/O (DB7)	Data bus Inputs for character code and instruction code from MPU Output for Busy/Ready flag (DB7)
D	1	HD44100H	O	Serial dot data of characters for LCD drivers
CL2	1	HD44100H	O	Dot data shift signal for LCD drivers
CL1	1	HD44100H	O	Dot data latch signal for LCD drivers

No.	4	8	16	24	32	40	64	80
CN0	GND	V_{CC}	GND	V_{CC}	GND	V_{CC}	GND	V_{CC}
CN1	GND	GND	V_{CC}	V_{CC}	GND	GND	V_{CC}	V_{CC}
CN2	GND	GND	GND	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}

Pin name	Number of terminals	Connected to	I/O	Function
M	1	HD44100H	O	Alternate signal for LCD drivers
FLM	1	HD44100H	O	Signal for common plates scanning
X0 to X7	8	ROM	O	Character code outputs for external character generator (for ext ROM) X7: MSB X0: LSB ex: character 'A' MSB: 0 1 0 0 0 0 0 LSB: 1 '1' = High '0' = Low
Y0 Y1 Y2 Y3	4	ROM	O	Character row code for external character generator 5 × 7 + Cursor 5 × 11 + Cursor 
φA	1	ROM	O	Clock signal for external character generator (dynamic ROM etc.) if necessary
O1 to O5	5	ROM	I	Dot data inputs from external character generator 1 (High): On 0 (Low): Off
ROMS	1	GND or V_{CC}	I	Select internal or external ROM High: External ROM Low: Internal ROM
OSC1 OSC2	2		(I) (O)	Oscillator 5 × 7 + Cursor: R_f = 200 kΩ (typ) 5 × 11 + Cursor: R_f = 130 kΩ (typ)
NC	3			Don't connect any signal to these terminals

4

Character Dot Patterns

5 × 7

The bottom lines of the English small characters "g, i, p, q, y," are on the cursor line (Figure 1).

5 × 11

Only the English small character "g, j, p, q, y," are displayed as below. The others are the same as for 5 × 7 (Figure 2).

Cursor 5 dots: ●●●●●
1 dot : ●

The cursor is displayed on the 8th or 12th line.

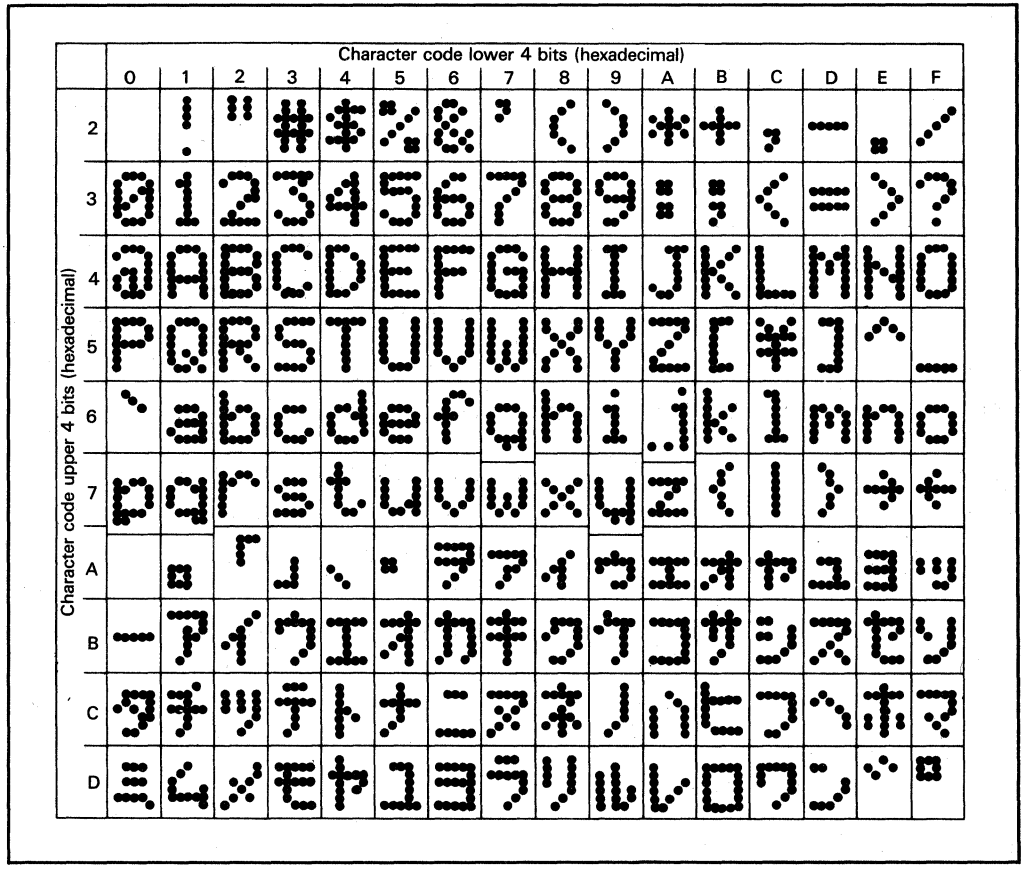


Figure 1 5 × 7 Characters

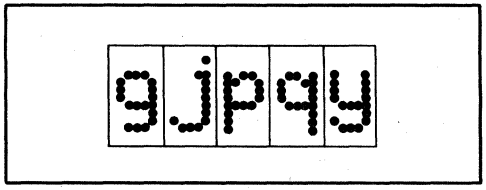


Figure 2 Special 5 × 11 Characters

Application

Setting Up

1. Total character number: CNO—CN2
2. Cursor pattern: CURS
3. Display line number: DLN
4. Font: FNTS

These terminals should be connected to V_{CC} or GND according to the LCD display system. RST and TEST should be connected to V_{CC} and GND respectively.

Interface to the Controller

1. Example 1 Interface to HD6800

In this example (Figure 3), the addresses of HD43160AH in the address area of the HD6800 microcomputer are:

Instruction code register	#'E***'	(R/W=0)
Character code register	#'F***'	(R/W=0)
Busy flag	#'E***' or #'F***'	(R/W=1)

*: don't care
#': hexadecimal

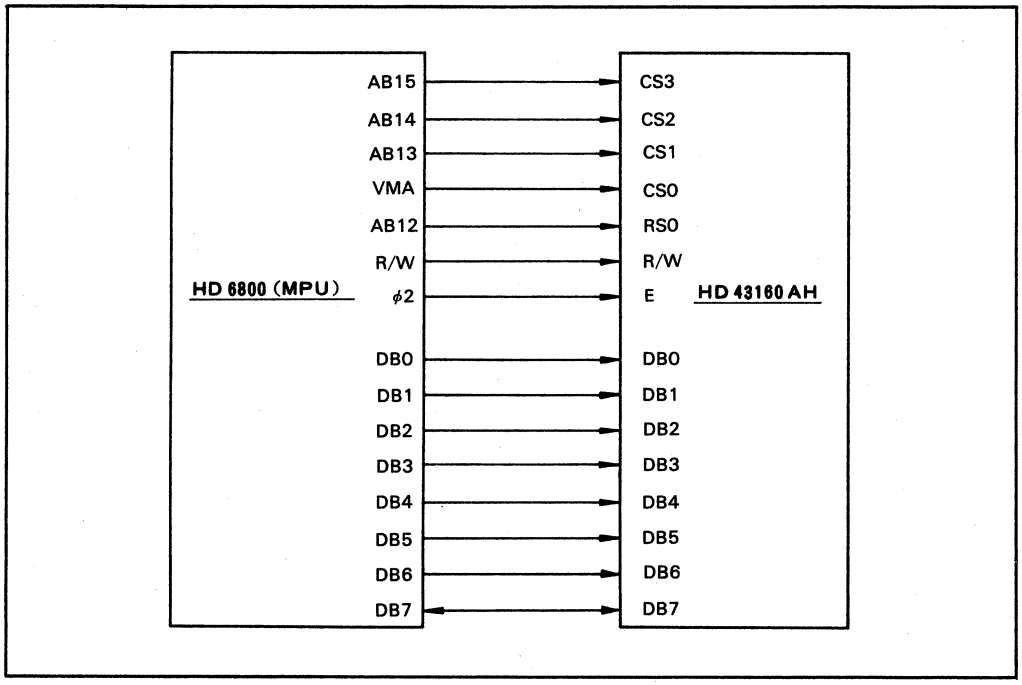


Figure 3 HD6800 Interface

4

2. Example of display program

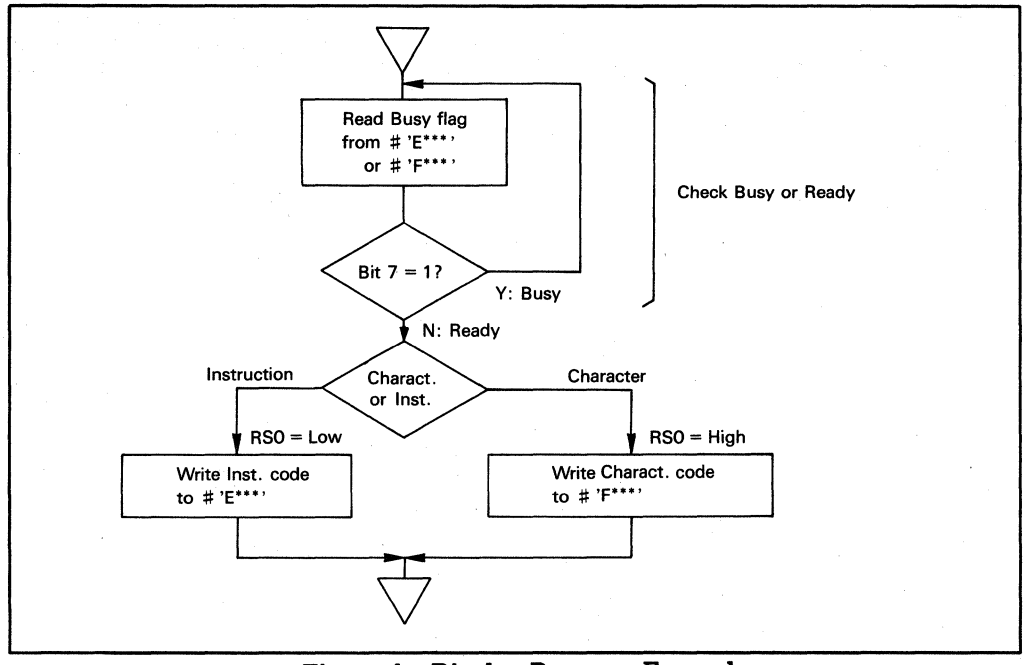
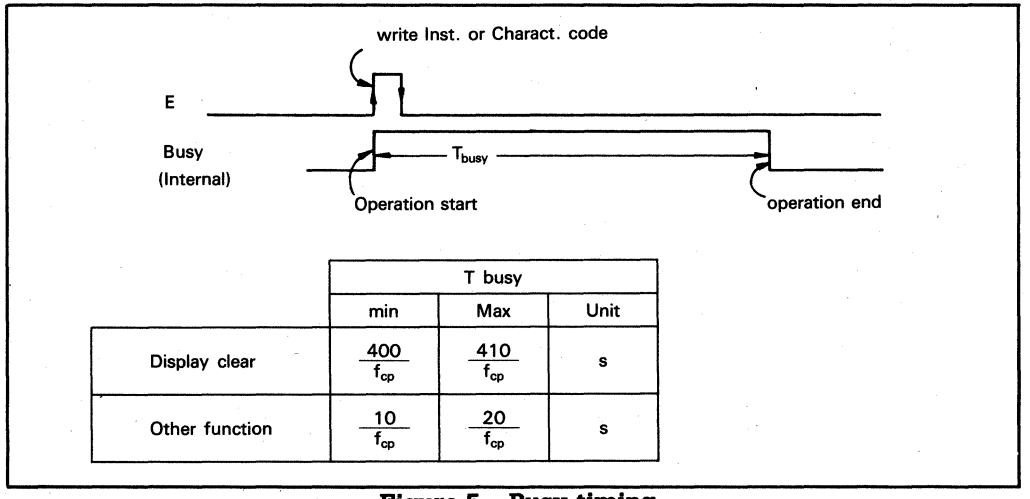


Figure 4 Display Program Example

3. Time length of Busy



	T busy		
	min	Max	Unit
Display clear	$\frac{400}{f_{cp}}$	$\frac{410}{f_{cp}}$	s
Other function	$\frac{10}{f_{cp}}$	$\frac{20}{f_{cp}}$	s

Figure 5 Busy timing

HD43160AH begins the operation from the rising edge of E (Figure 5).
Instruction code register and character code register latch the data on DB0—DB7 at the falling edge of E.

4. Timing chart

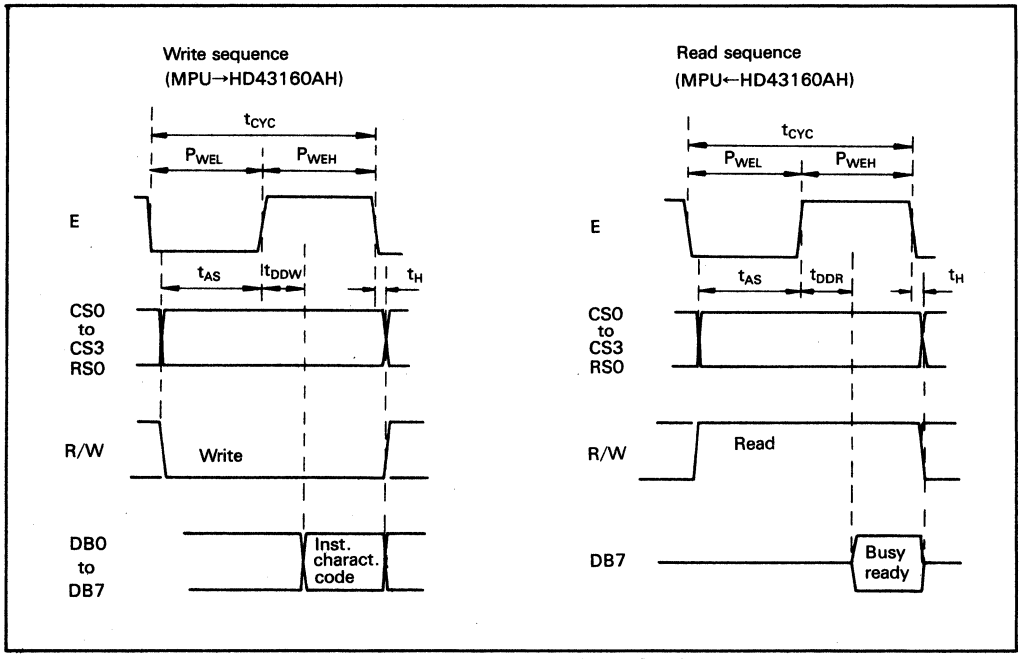


Figure 6 HD6800 Interface Timing

5. Timing characteristics

Item		Symbol	Min	Typ	Max	Unit
Cycle time of E		t_{cyc}	1.0	–	–	μs
Pulse width of E	High level	P_{WEH}	0.45	–	25	μs
	Low level	P_{WEL}	0.45	–	–	μs
Set up time of CS	Write	t_{AS}	140	–	–	ns
Data delay time	Write	t_{DDW}	–	–	225	ns
	Read	t_{DDR}	–	–	300	ns
Hold time		t_H	10	–	–	ns

6. Example 2 Interface to 8085A (Intel)

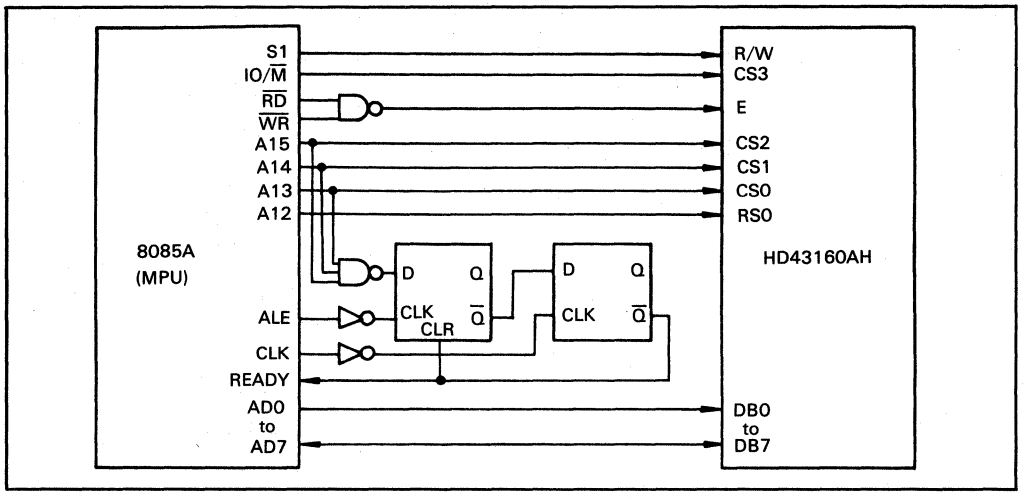


Figure 7 8085A Interface

7. Timing chart

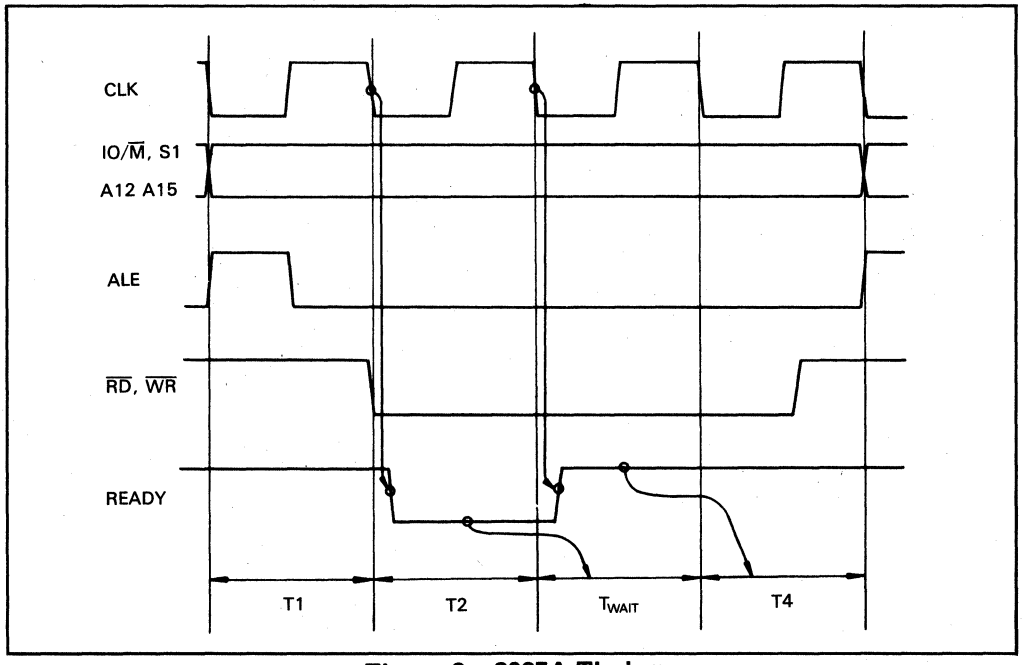


Figure 8 8085A Timing

Pulse widths of $\overline{RD}$ and $\overline{WR}$ signals of the 8085A are 400 ns min, while the pulse width of the E signal of the HD43160AH is 450 ns min (Figure 8).
Therefore, in this example, $\overline{RD}$ and $\overline{WR}$ signal pulse widths are widened by the T_{WAIT} cycle.

Display Commands

Display Control Instructions

These instructions should be written into the instruction register of HD43160AH by the microcomputer. (RS0 = Low, R/W = Low)

1. Display clear

	MSB							LSB
Code:	0	0	0	0	0	0	0	1

Operation: The screen is cleared and the cursor returns to the 1st digit.

2. Cursor return

	MSB							LSB
Code:	0	0	0	0	0	0	1	0

Operation: The cursor returns to the 1st digit and the characters being displayed do not change.

3. Cursor on/off

	MSB							LSB	
Code:	0	0	0	0	0	1	0	0	(On)
	0	0	0	0	0	1	0	1	(Off)

Operation: The cursor appears (on) or disappears (off).

4. Set cursor position

		MSB			LSB
Code:	1 line		1		(N − 1) binary
	2 lines	upper	1	0	(n − 1) binary
		lower	1	1	(m − 1) binary

N, n, m: digit number

Operation: The cursor moves to the Nth (nth, mth) digit.
N ≦ the total character number
n, m ≦ 1/2 total character number

ex 1: 1 line
Set the cursor at digit 55. The code is 10110110.

ex 2: 2 lines
Set the cursor at digit 35 of upper or lower line.
The code is 10100010 (upper).
11100010 (lower).

Display Character Command

When the character code is written into the character register of HD43160AH, the character with thiscode appears where the cursor wasdisplayed and the cursor moves to the next digit. (RS0 = High, R/W = Low)

	MSB	LSB
code:	(Character code)	

ex. 1

before	ABCD_
after	ABCDE_

Read Busy Flag

When CS0—CS3 = High, R/W = High and E = High (RS0 = 'don't care'), the Busy/Ready signal appears on DB7.

DB 7 High: Busy
Low: Ready

Table 1 Time Length of Busy (oscillation frequency = 200 kHz)

	Min	Max	Unit
Display clear	2.0	2.05	ms
Other operations	50	100	μs

(depends on the operating frequency)

Interface to External ROM

1. Example

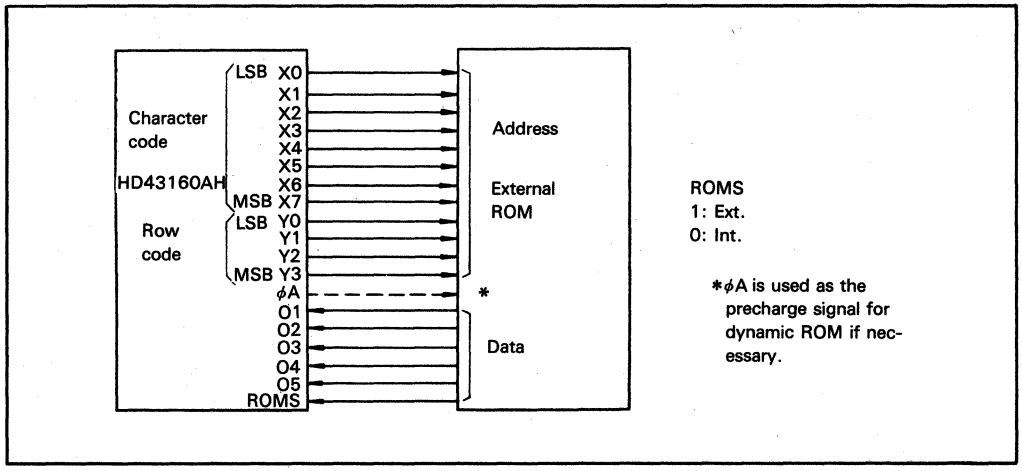


Figure 9 Interface to External ROM

2. Row code

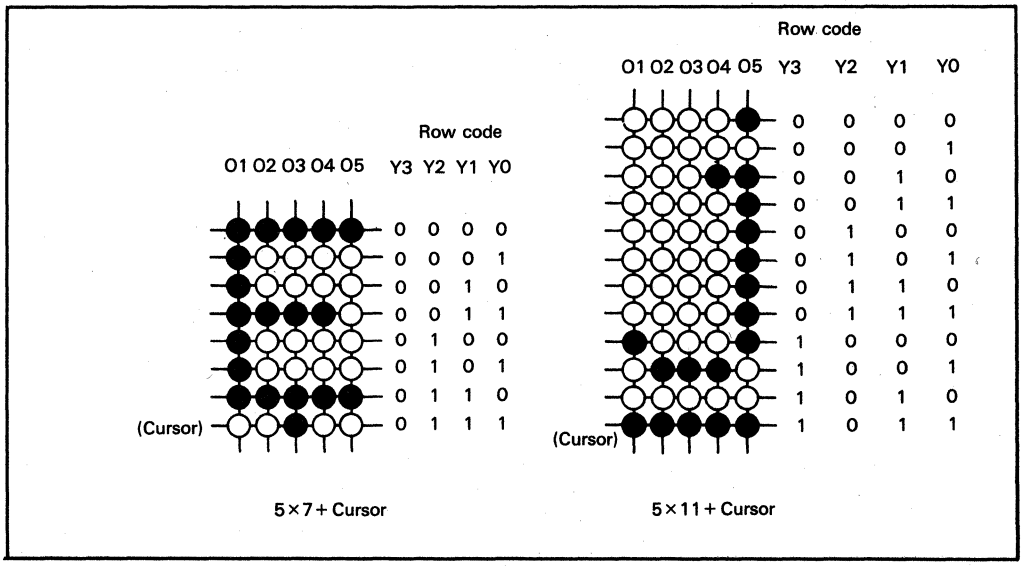


Figure 10 Row Code

3. Timing chart

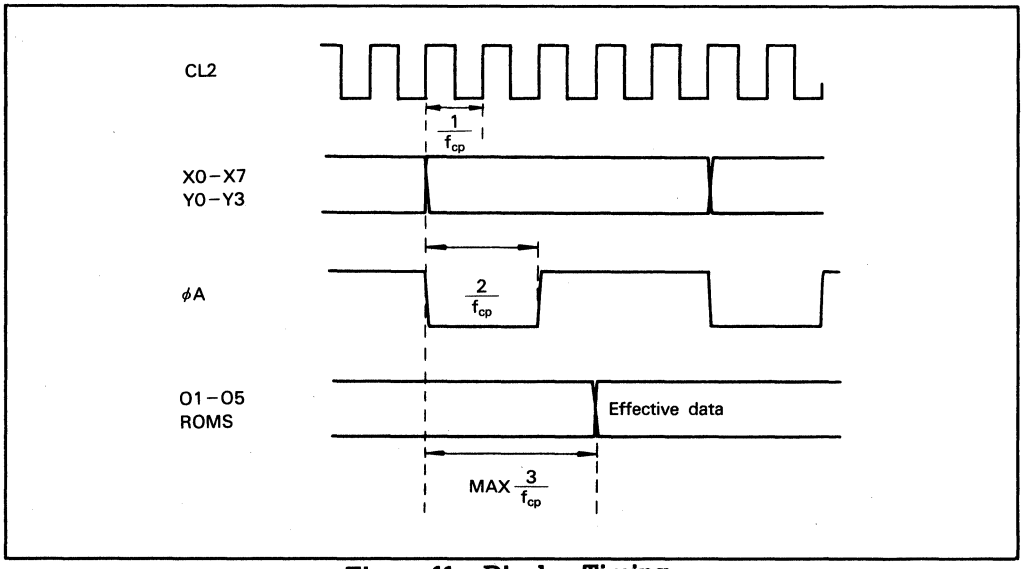


Figure 11 Display Timing

Interface to LCD Drivers

1. Example

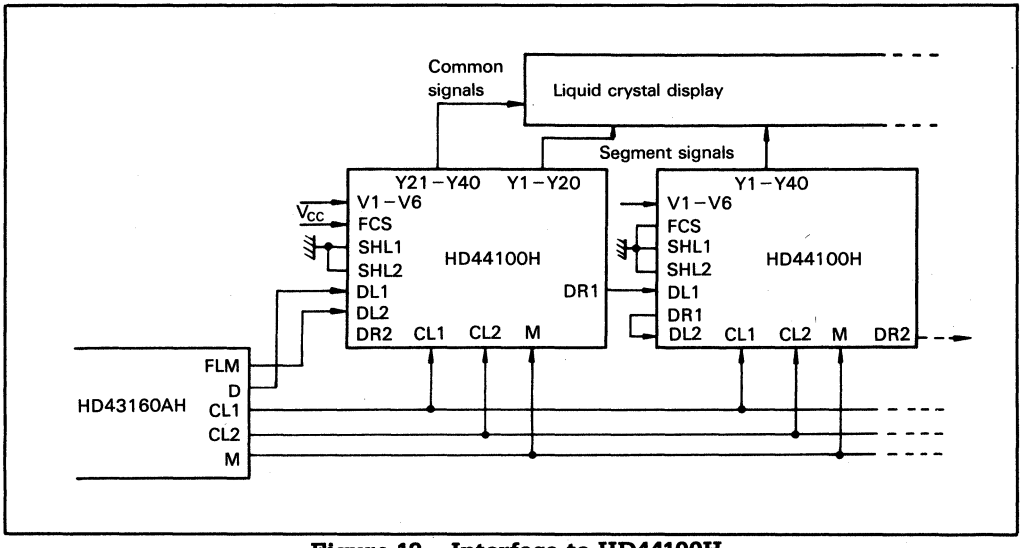


Figure 12 Interface to HD44100H

2. Waveforms (5 × 7 + Cursor 1 line)

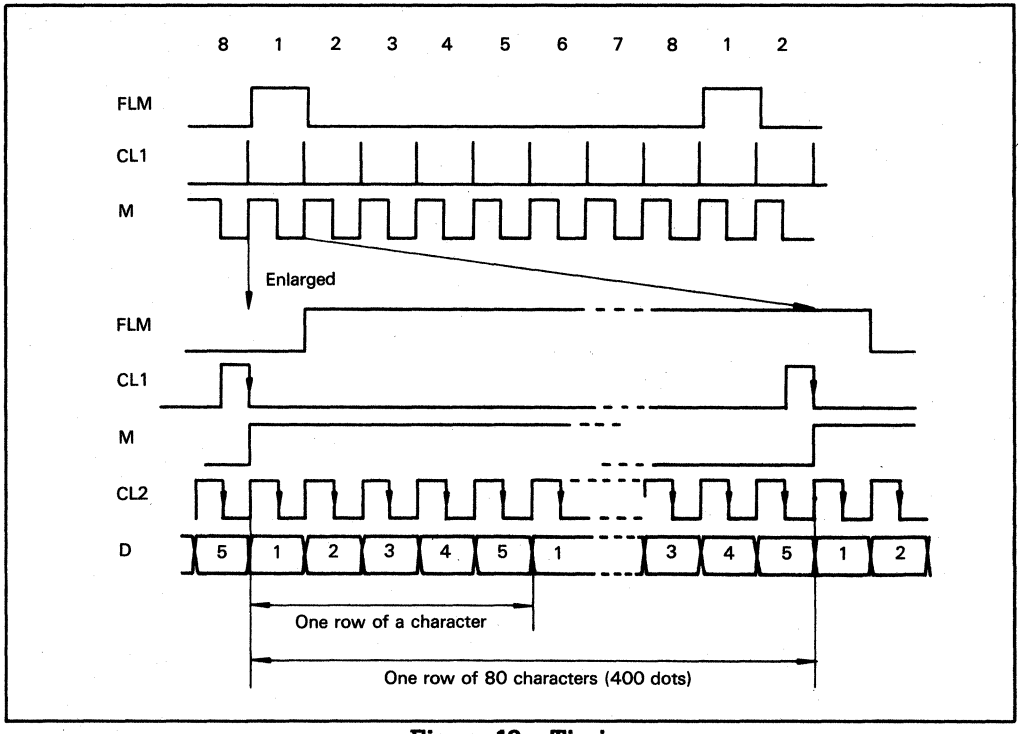


Figure 13 Timing

Dot Matrix Liquid Crystal Display System

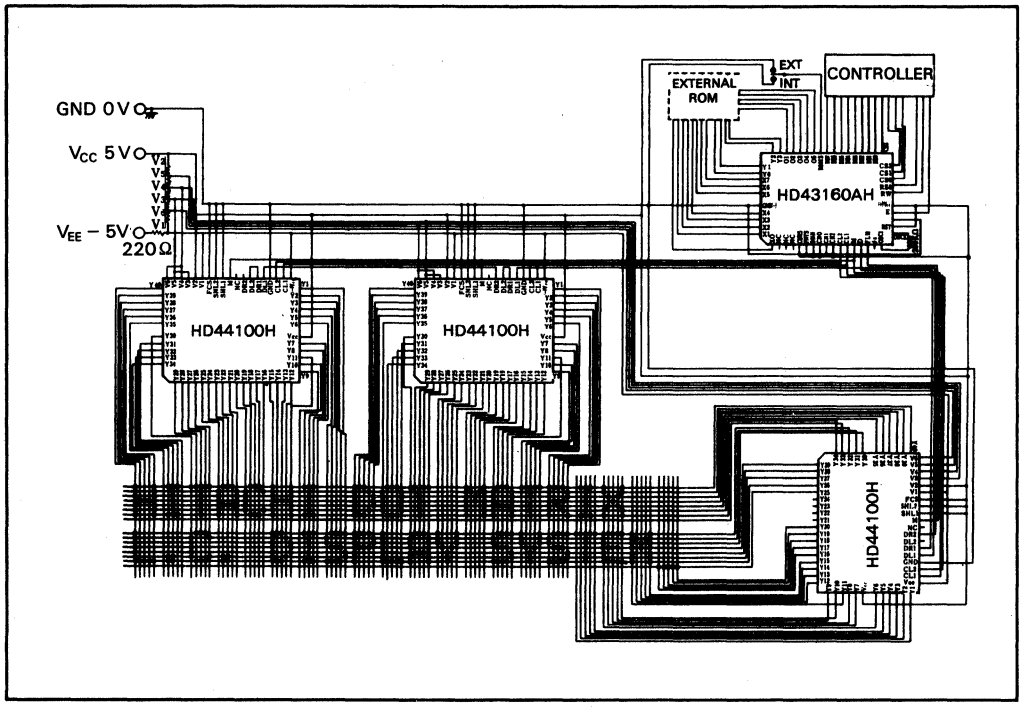


Figure 14. Typical Application 5 × 7 + Cursor, 2 Lines, 40 Characters

4

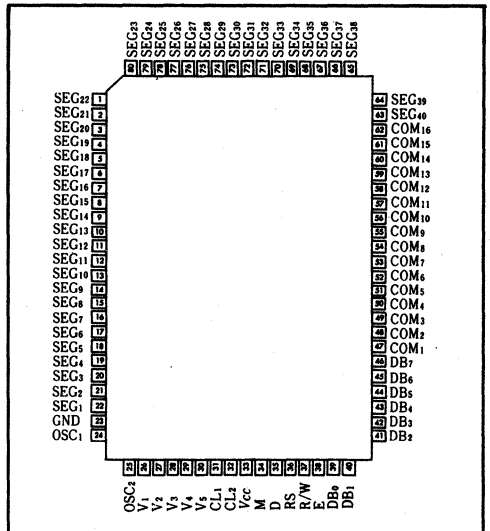
HD44780, HD44780A (LCD-II)

(Dot Matrix Liquid Crystal Display Controller & Driver)

Description

The LCD-II (HD44780, HD44780A) dot matrix liquid crystal display controller & driver LSI displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip. The user can complete dot matrix liquid crystal display systems with low chip count by using the LCD-II (HD44780, HD44780A).
If an HD44100H driver LSI is connected to the HD44780, up to 80 characters can be displayed.
The LCD-II is produced by the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcontroller or microprocessor can complete a portable battery-driver device with low power dissipation.

Pin Arrangement



(FP-80)
(Top View)

(FP-80A)
(Top View)

Feautures

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Capable of interfacing to 4-bit or 8-bit MPU
- Display data RAM: 80 × 8 bits (80 characters, max.)
- Character generator ROM:
  —Character font 5 × 7 dots: 160 characters
  —Character font 5 × 10 dots: 32 characters
- Character generator RAM
  —Character font 5 × 7 dots: 8 characters
  —Character font 5 × 10 dots: 4 characters
- Both display data and character generator RAMs can be read from the MPU
- Internal liquid crystal display driver:
  —16 common signal drivers
  —40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H)
- Duty factor (selected by program):
  —1/8 duty: 1 line of 5 × 7 dots + cursor
  —1/11 duty: 1 line of 5 × 10 dots + cursor

—1/16 duty: 2 line of 5 × 7 dots + cursor

- Wide range of instruction functions:
  Display clear, Cursor home, Display on/off, Cursor on/off,
  Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power on (Internal reset circuit)
- Internal oscillation circuit
  (with external resistor or ceramic filter)
  (External clock operation possible)
- CMOS process
- Logic power supply:
  A single +5 V (excluding power for liquid crystal display drive)
- Operation temperature range:
  −20 to +75℃ (Device for −40 to +85℃ available upon request)
- 80-pin plastic QFP (FP-80, FP-80A)
  80-pin thin plastic QFP (TFP-80: under development)

Maximum Number of Display Characters

No. of Display Lines	Duty Factor	Extension	LCD-II	HD44100H	No. of Display Characters
1-line display	1/8 1/11 duty cycle	Not provided	1	—	8 characters × 1 line
		Porovided	1	9 (8 characters/each)	80 characters × 1 line
2-line display	1/16 duty cycle	Not provided	1	—	8 characters × 2 lines
		Provided	1	4 (8 characters × 2 lines/each)	40 characters × 2 lines

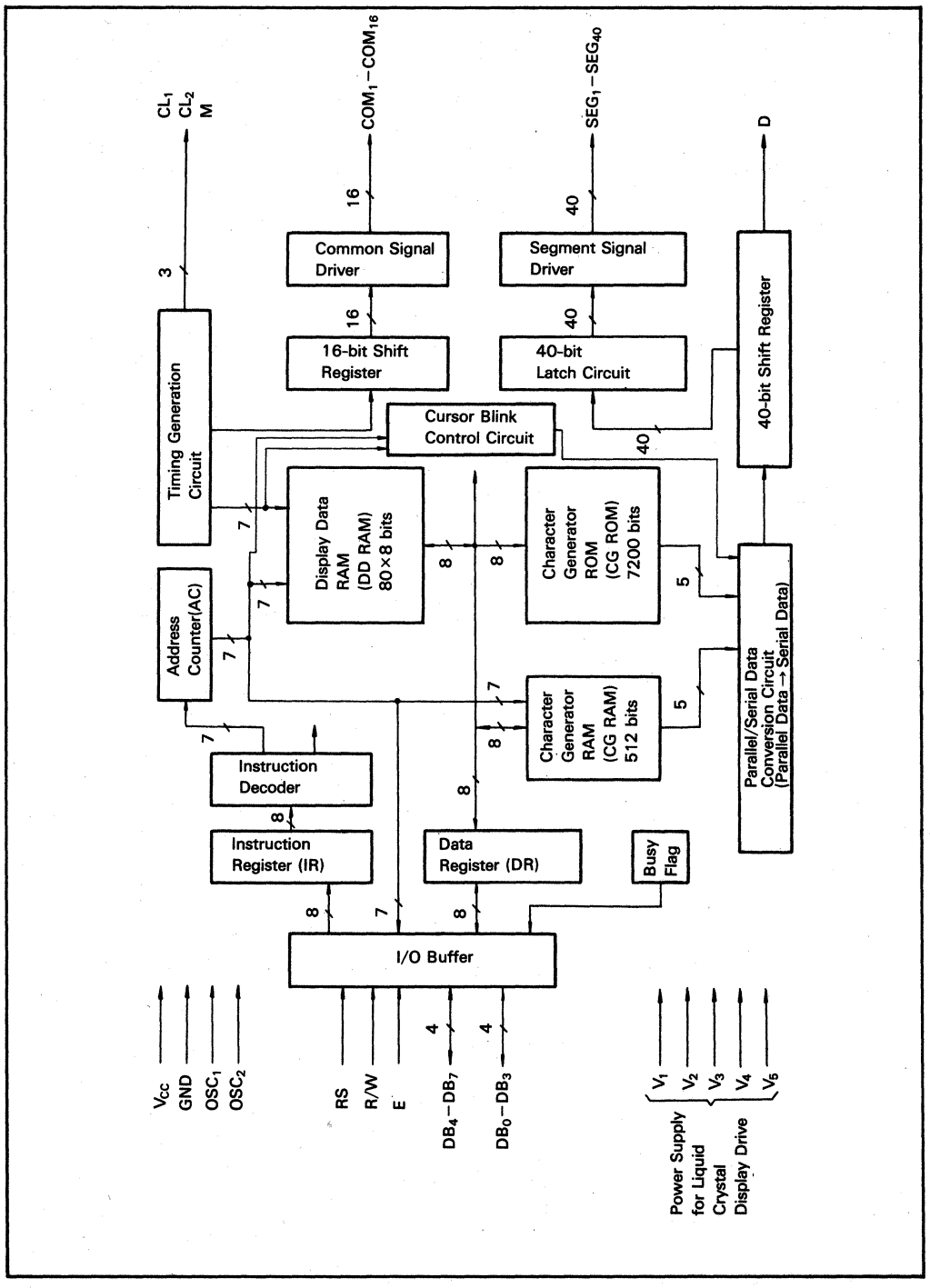
Ordering Information

Type No.	Operation Frequency	Package
HD44780SA**H	1.0 MHz	80-Pin plastic QFP (FP-80)
HD44780SA**FH		80-Pin plastic QFP (FP-80A)
HD44780SA**TF		80-pin thin plastic QFP (TFP-80: under development)
HD44780SA**FA	1.5 MHz	80-Pin plastic QFP (FP-80)

Note: ** = ROM Code No.

4

Block Diagram (LCD-II Interior)



Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	−0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	V_{CC}−13.5 to V_{CC}+0.3	V	3
Input Voltage	V_T	−0.3 to V_{CC}+0.3	V	
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note 1: If LSI's are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

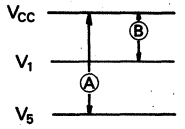
Note 2: All voltage values are referenced to GND = 0 V.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$
(high ← → low)

4

Electrical Characteristics
(V_{CC} = 5 V ± 10%, T_a = −20 to +75°C)

The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".



Ⓐ = $V_{CC} - V_5$
Ⓑ = $V_{CC} - V_1$
Ⓐ ≧ 1.5 V
Ⓑ ≦ 0.25 × Ⓐ

HD44780

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage (1)	V_{IH1}	2.2	—	V_{CC}	V		(2)
Input Low Voltage (1)	V_{IL1}	−0.3	—	0.6	V		(2)
Output High Voltage (1) (TTL)	V_{OH1}	2.4	—	—	V	$-I_{OH}$ = 0.205 mA	(3)
Output Low Voltage (1) (TTL)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.2 mA	(3)
Output High Voltage (2) (CMOS)	V_{OH2}	0.9V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	(4)
Output Low Voltage (2) (CMOS)	V_{OL2}	—	—	0.1V_{CC}	V	L_{OL} = 0.04 mA	(4)
Driver Voltage Descending (COM)	V_{COM}	—	—	2.9	V	Id=0.05 mA	(10)
Driver Voltage Descending (SEG)	V_{SEG}	—	—	3.8	V	Id=0.05 mA	(10)
Input Leakage Current	I_{IL}	−1	—	1	μA	V_{in} = 0 to V_{CC}	(5)
Pull-Up MOS Current	$-I_P$	50	125	250	μA	V_{CC} = 5 V	
Power Supply Current (1)	I_{CC1}	—	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, f_{OSC} = 250 kHz	(6)
Power Supply Current (2)	I_{CC2}	—	0.35	0.6	mA	Rf oscillation External clock operation V_{CC} = 5 V, f_{OSC} = f_{cp} = 270 kHz	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}	125	250	350	kHz		(7)
External Clock Duty Cycle	Duty	45	50	55	%		(7)
External Clock Rise Time	t_{rcp}	—	—	0.2	μs		(7)
External Clock Fall Time	t_{fcp}	—	—	0.2	μs		(7)
Input High Voltage (2)	V_{IH2}	V_{CC} − 1.0	—	V_{CC}	V		(12)
Input Low Voltage (2)	V_{IL2}	—	—	1.0	V		(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{OSC}	190	270	350	kHz	Rf = 91 kΩ ± 2%	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{OSC}	245	250	255	kHz	Ceramic filter	(9)
LCD Voltage	V_{LCD1}	4.6	—	11	V	V_{CC} − V5 1/5 bias	(13)
	V_{LCD2}	3.0	—	11	V	1/4 bias	(13)

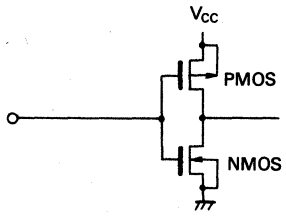
HD44780A

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage (1)	V_{IH1}	2.2	—	V_{CC}	V		(2)
Input Low Voltage (1)	V_{IL1}	−0.3	—	0.6	V		(2)
Output High Voltage (1) (TTL)	V_{OH1}	2.4	—	—	V	$-I_{OH}$ = 0.205 mA	(3)
Output Low Voltage (1) (TTL)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.2 mA	(3)
Output High Voltage (2) (CMOS)	V_{OH2}	0.9V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	(4)
Output Low Voltage (2) (CMOS)	V_{OL2}	—	—	0.1V_{CC}	V	L_{OL} = 0.04 mA	(4)
Driver Voltage Descending (COM)	V_{COM}	—	—	2.9	V	Id = 0.05 mA	(10)
Driver Voltage Descending (SEG)	V_{SEG}	—	—	3.8	V	Id = 0.05 mA	(10)
Input Leakage Current	I_{IL}	−1	—	1	μA	V_{in} = 0 to V_{CC}	(5)
Pull up MOS Current	$-I_P$	50	125	250	μA	V_{CC} = 5 V	
Power Supply Current (1)	I_{CC1}	—	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, fosc = 250 kHz	(6)
Power Supply Current (2)	I_{CC2}	—	0.35	0.6	mA	Rf oscillation External clock operation V_{CC} = 5 V, fosc = f_{cp} = 270 kHz	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}	125	250	350	kHz		(7)
External Clock Duty	Duty	45	50	55	%		(7)
External Clock Rise Time	t_{rcp}	—	—	0.2	μs		(7)
External Clock Fall Time	t_{fcp}	—	—	0.2	μs		(7)
Input High Voltage (2)	V_{IH2}	V_{CC} − 1.0	—	V_{CC}	V		(12)
Input Low Voltage (2)	V_{IL2}	—	—	1.0	V		(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	fosc	190	270	350	kHz	Rf = 91 kΩ±2%	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	fosc	245	250	255	kHz	Ceramic filter	(9)
LCD Voltage	V_{LCD1}	4.6	—	11	V	V_{CC} − V5 1/5 bias	(13)
	V_{LCD2}	3.0	—	11	V	1/4 bias	(13)

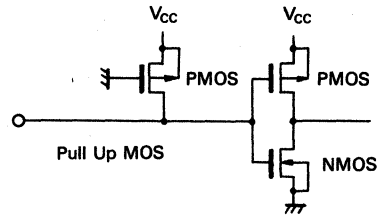
4

Notes: 1. The following are I/O terminal configurations except for liquid crystal display output.

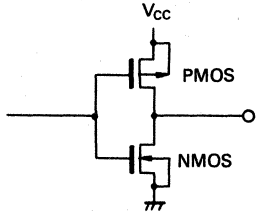
- Input Terminal
  Applicable Terminals: E
  (MOS without pull up)



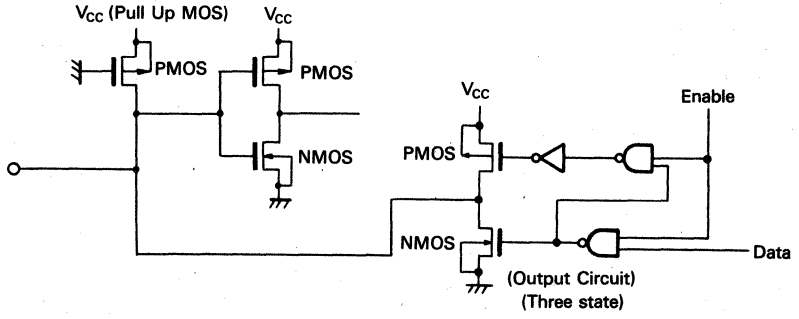
- Applicable Terminals: RS, R/W
  (MOS with pull up)



- Output Terminal
  Applicable Terminals: CL_1, CL_2, M, D

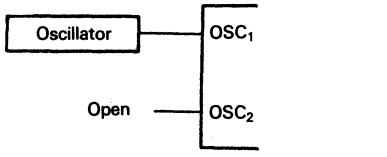


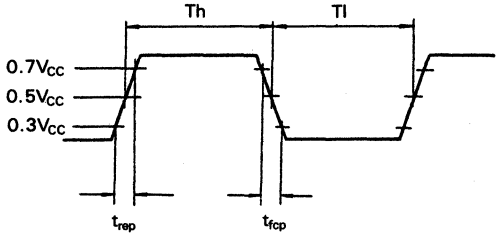
- I/O Terminal
  Applicable Terminals: DB_0 to DB_7



Notes: 2. Input terminals and I/O terminals. Excludes OSC_1 terminals.
Notes: 3. I/O terminals.
Notes: 4. Output terminals.
Notes: 5. Current flowing through pull-up MOSs and output drive MOSs is excluded.
Notes: 6. Input/output current is excluded. When cmos input is at an intermediate level, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

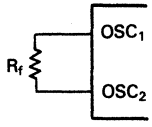
Notes: 7. External clock operation.





$$\text{Duty cycle} = \frac{Th}{Th + Tl} \times 100\%$$

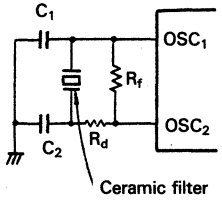
Notes: 8. Internal oscillator operation using oscillation resistor Rf.



R_f: 91 kΩ ± 2%

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacitance, wiring length for these terminals should be minimized.

Notes: 9. Internal oscillator operation using a ceramic filter.

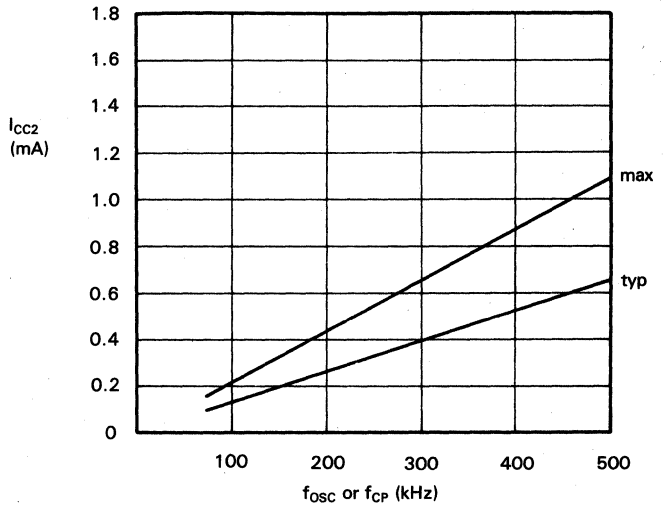


Ceramic filter: CSB250A (Murata)
R_f: 1 MΩ ± 10%
C_1: 680 pF ± 10%
C_2: 680 pF ± 10%
R_d: 3.3 kΩ ± 5%

Notes: 10. Applies to both V_{COM} and V_{SEG} voltage drops.
V_{COM}: From power supply terminal V_{CC}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})
V_{SEG}: From power supply terminal V_{CC}, V_2, V_3, V_5 to each segment signal terminal (SEG_1 to SEG_{40})

4

Notes: 11. Relation between operation frequency and current consumption is shown in this diagram (V_{CC} = 5 V).



Notes: 12. Applied to OSC_1 terminal.
Notes: 13. The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

Timing Characteristics

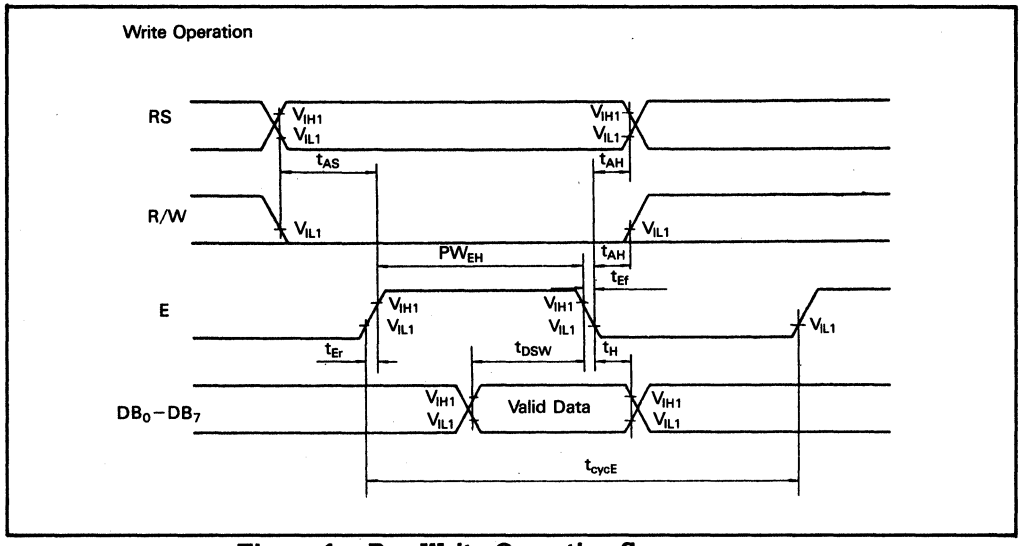


Figure 1 Bus Write Operation Sequence (Writing data from MPU to LCD-II)

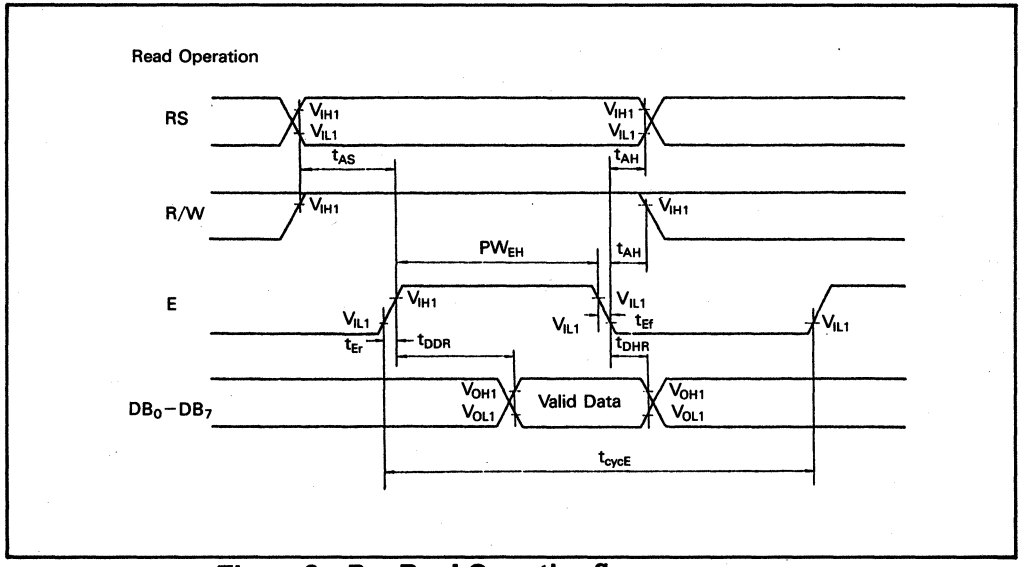


Figure 2 Bus Read Operation Sequence (Reading out data from LCD-II to MPU)

4

Interface Signal with Driver LSI HD44100H

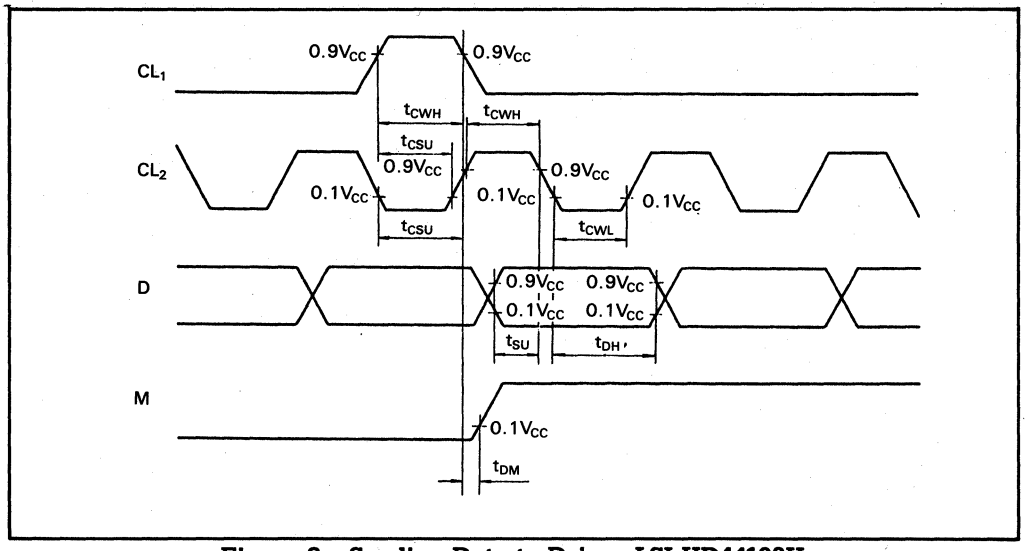


Figure 3 Sending Data to Driver LSI HD44100H

Bus Timing Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = −20 to +75°C)

HD44780

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	1000	—	ns	Fig. 1
Enable Pulse Width	High level	PW_{EH}	450	—	ns	Fig. 1
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 1
Address Set-up Time	RS, R/W E	t_{AS}	140	—	ns	Fig. 1
Address Hold Time		t_{AH}	10	—	ns	Fig. 1
Data Set-up Time		t_{DSW}	195	—	ns	Fig. 1
Data Hold Time		t_H	10	—	ns	Fig. 1

Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	1000	—	ns	Fig. 2
Enable Pulse Width	High level	PW_{EH}	450	—	ns	Fig. 2
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 2
Address Set-up Time	RS, R/W E	t_{AS}	140	—	ns	Fig. 2
Address Hold Time		t_{AH}	10	—	ns	Fig. 2
Data Delay Time		t_{DDR}	—	320	ns	Fig. 2
Data Hold Time		t_{DHR}	20	—	ns	Fig. 2

HD44780A

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	666	—	ns	Fig. 1
Enable Pulse Width	High level	PW_{EH}	300	—	ns	Fig. 1
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 1
Address Set-up Time	RS, R/W E	t_{AS}	60*1	—	ns	Fig. 1
			100*2	—	ns	
Address Hold Time		t_{AH}	10	—	ns	Fig. 1
Data Set-up Time		t_{DSW}	100	—	ns	Fig. 1
Data Hold Time		t_H	10	—	ns	Fig. 1

Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	666	—	ns	Fig. 2
Enable Pulse Width	High level	PW_{EH}	300	—	ns	Fig. 2
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 2
Address Set-up Time	RS, R/W E	t_{AS}	60*1 100*2		ns	Fig. 2
Address Hold Time		t_{AH}	10	—	ns	Fig. 2
Data Delay Time		t_{DDR}	—	190	ns	Fig. 2
Data Hold Time		t_{DHR}	20	—	ns	Fig. 2

Notes: *1. 8-bit interface mode
*2. 4-bit interface mode

Interface Signal with HD44100H Timing Characteristics
(V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = −20 to +75°C)

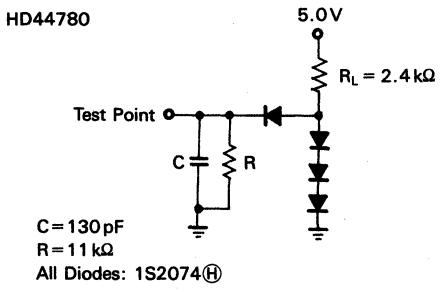
HD44780

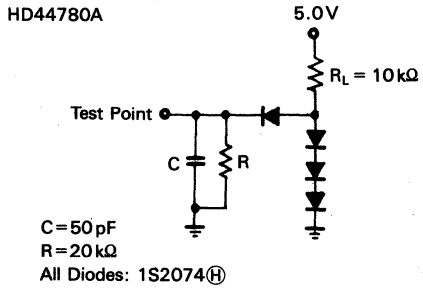
Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Clock Pulse Width	High level	t_{CWH}	800	—	ns	Fig. 3
Clock Pulse Width	Low level	t_{CWL}	800	—	ns	Fig. 3
Clock Set-up Time		t_{CSU}	500	—	ns	Fig. 3
Data Set-up Time		t_{SU}	300	—	ns	Fig. 3
Data Hold Time		t_{DH}	300	—	ns	Fig. 3
M Delay Time		t_{DM}	−1000	1000	ns	Fig. 3

HD44780A

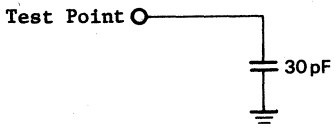
Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Clock Pulse Width	High level	t_{CWH}	800	—	ns	Fig. 3
Clock Pulse Width	Low level	t_{CWL}	800	—	ns	Fig. 3
Clock Set-up Time		t_{CSU}	500	—	ns	Fig. 3
Data Set-up Time		t_{SU}	300	—	ns	Fig. 3
Data Hold Time		t_{DH}	300	—	ns	Fig. 3
M Delay Time		t_{DM}	−1000	1000	ns	Fig. 3

Notes:
Loading Circuit (TTL Load): DB_0 to DB_7





Loading Circuit (CMOS Load): CL_1, CL_2, D, M



4

Power Supply Conditions Using Internal Reset Circuit

LCD-II

Item	Symbol	Limit		Unit	Test Condition
		Min	Max		
Power Supply Rise Time	t_{rcc}	0.1	10	ms	—
Power Supply OFF Time	t_{OFF}	1	—	ms	—

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction. (Refer to "Initializing by Instruction")

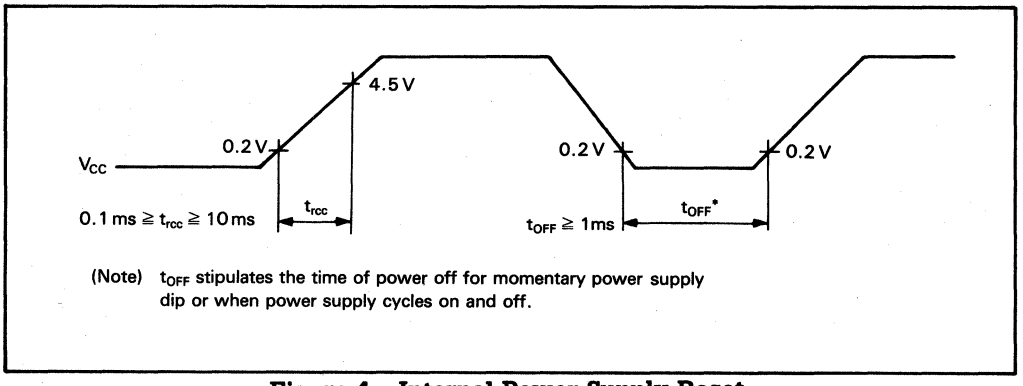


Figure 4 Internal Power Supply Reset

Terminal Function

Table 1 Functional Description of Terminals

Signal Name	No. of Lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W). 0: Write 1: Read
E	1	Input	MPU	Operation start signal for data read/write.
DB_4-DB_7	4	Input/ Output	MPU	Higher order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II. DB_7 can be used as a BUSY flag.
DB_0-DB_3	4	Input/ Output	MPU	Lower order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Sends character pattern data corresponding to each common signal serially. 0: Non selection 1: Selection
COM_1-COM_{16}	16	Output	Liquid crystal display	Common signals that are not used are changed to non-selection waveforms. That is, COM_9-COM_{16} are non-selection waveforms at 1/8 duty factor, and COM_{12}-COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1-SEG_{40}	40	Output	Liquid crystal display	Segment signal.
V_1-V_5	5		Power supply	Power supply for liquid crystal display drive.
V_{CC}, GND	2		Power supply	V_{CC}: +5 V, GND: 0 V.
OSC_1, OSC_2	2			Terminals connected to resistor or ceramic filter for internal clock osillation. For external clock operation, the clock is input to OSC_1.

4

Function Of Each Block

Register

The HD44780 has two 8-bit registers, an instruction register (IR), and a data register (DR).
The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.
The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data is read from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Busy flag (BF)

When the busy flag is 1, the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As table 2 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is 0.

Address counter (AC)

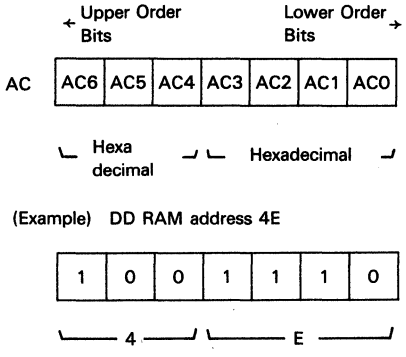
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.
After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output to DB_0 - DB_6 when RS = 0 and R/W = 1, as shown in table 2.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0-DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

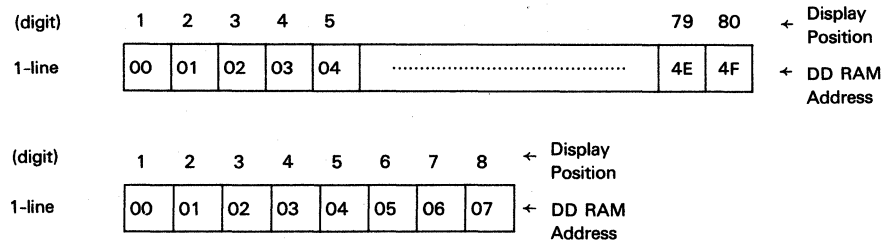
Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.
The DD RAM address (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.

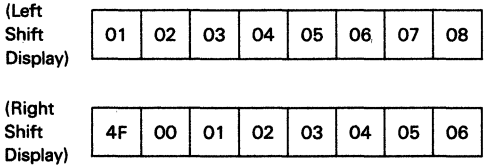


1-Line Display (N = 0)

1. When there are fower than 80 display characters, the display begins at the head position. For example, 8 characters using 1 HD44780 are displayed as:

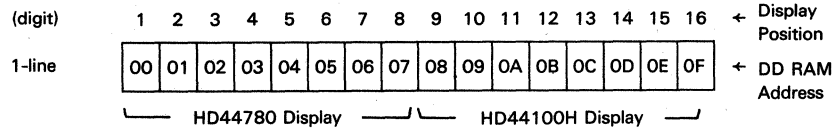


When the display shift operation is performed, the DD RAM address moves as:

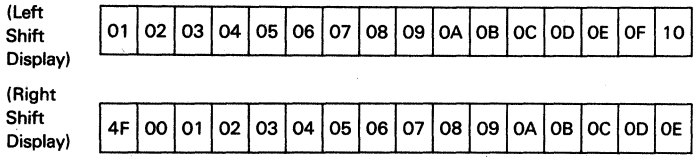


4

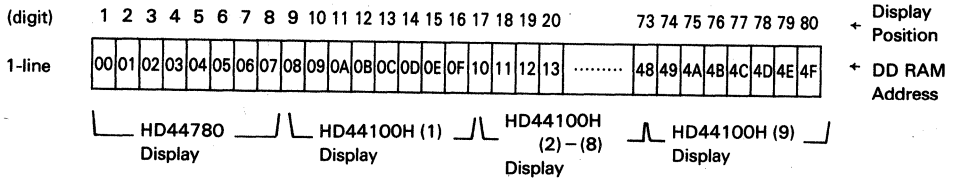
2. 16-character display using an HD44780 and an HD44100H is as shown below:



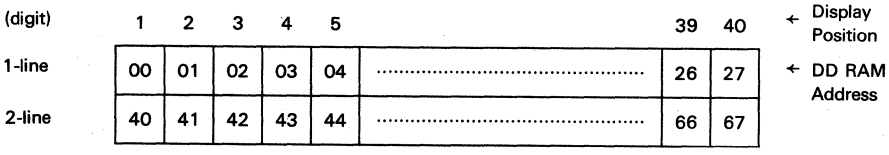
When the display shift operation is performed, the DD RAM address moves as:



3. The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of 2.
Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.



2-Line Display (N = 1)



1. When the number of display characters is less than 40 × 2 lines, the 2 lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters × 2 lines are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

(Right Shift Display)	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

2. 16 characters × 2 lines are displayed when an HD44780 and an HD44100H are used.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

└— HD44780 Display —┘└— HD44100H Display —┘

When display shift is performed, the DD RAM address moves as follows:

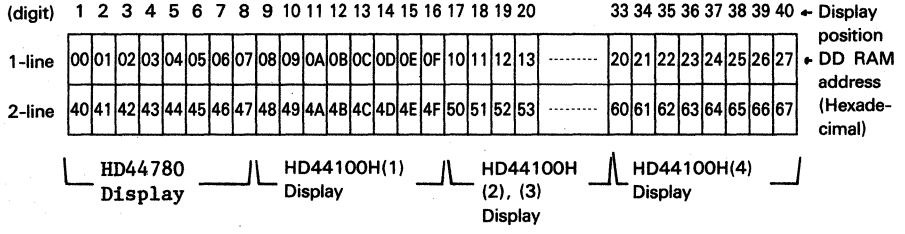
(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

4

3. The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of 2.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting 4 HD44780's externally.



Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns. Table 3 shows the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots, 4 characters can be written.
Write the character codes in the left column of table 3 to display character patterns stored in CG RAM.
Table 4 shows the relation between CG RAM addresses and data and display patterns.
As table 4 shows, an area that is not used for display can be used as a general data RAM.

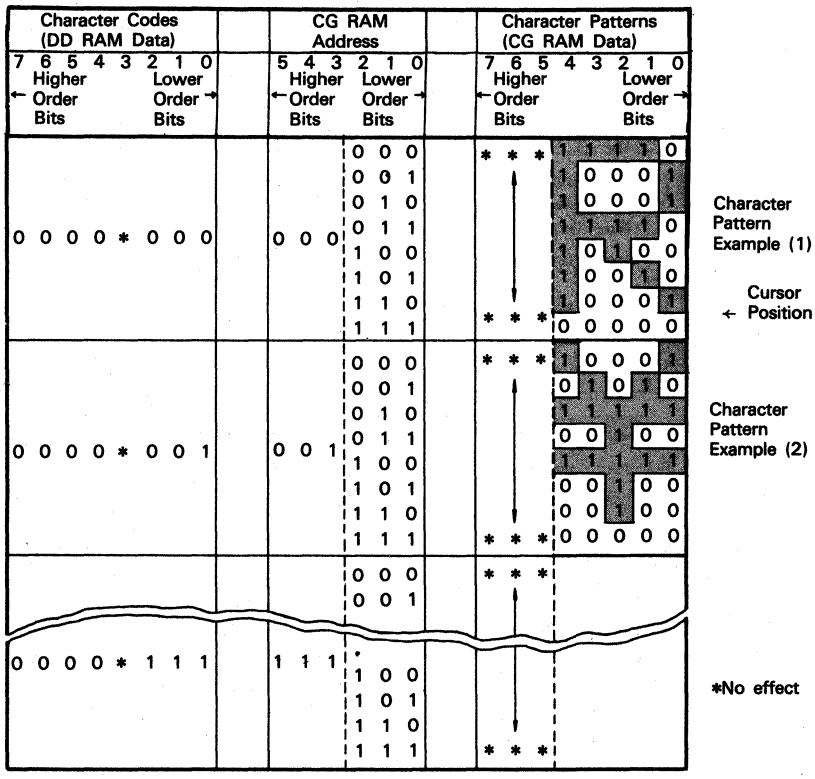
Table 3 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD44780A00)

Note: The user can specify any pattern for character-generator RAM.

4

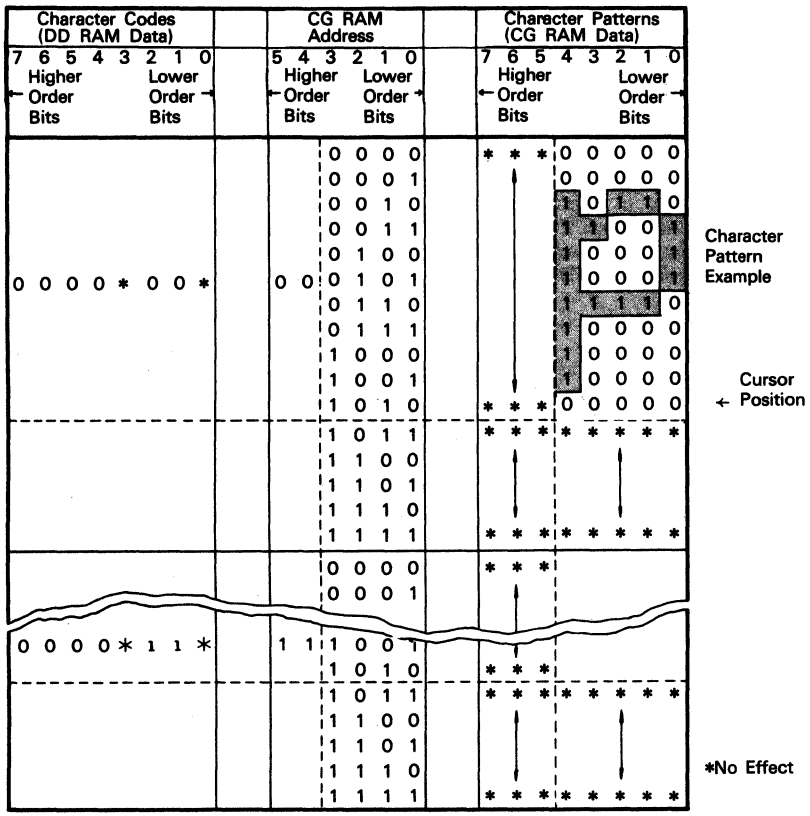
Table 4 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

For 5 × 7 dot character patterns



Notes:
1. Character code bits 0-2 correspond to CG RAM address bits 3-5 (3 bits: 8 types).
2. CG RAM address bits 0-2 designate character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0-4, as shown in the figure (bit 4 being at the left end).
   Since CG RAM data bits 5-7 are not used for display, they can be used for the general data RAM.
4. As shown in table 3, CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 3 has no effect, the "R" display in the character pattern example is selected by character code "00" (hexadecimal) or "08" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

For 5 × 10 dot character patterns



Notes: 1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).
2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.
Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor presence. Since the 12th-16th lines are not used for display, they can be used for general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 have no effect, "P" display in the character pattern example is selected by character codes "00", "01", "08" and "09" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM, and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

Liquid Crystal Display Driver Circuit

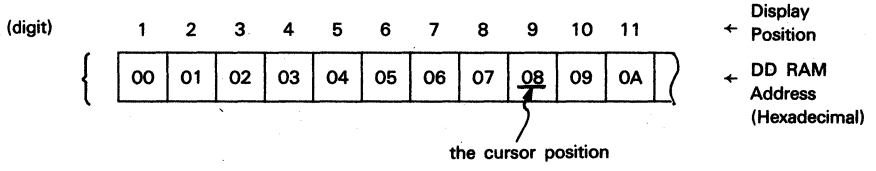
The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.
The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs. The serial data can be sent to HD44100Hs, externally connected in cascade, used for display digit number extension.
Serial data send always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).
Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

Cursor/Blink Control Circuit

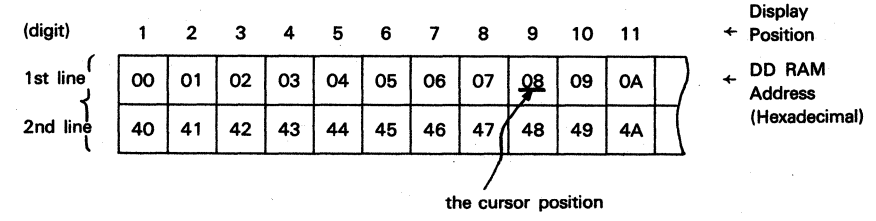
The cursor/blink control circuit generates the cursor or blink. The cursor or the blink appear in the digit at the display data RAM (DD RAM) address set in the address counter (AC).
When the address counter is $(08)_{16}$, the cursor position is:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



In a 2-line display



Note: The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is a CG RAM address.

Interfacing To MPU

In the HD44780, data can be sent in either 2 4-bit operations or 1 8-bit operations so it can interface to both 4- and 8-bit MPUs.

1. When interface data is 4-bits long, data is transferred using only 4 buslines: DB_4-DB_7. DB_0-DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4-DB_7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB_0-DB_3 when interface data is 8 bits long) is transferred.
   Check the busy flag after 4-bit data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data.
2. When interface data is 8 bits long, data is transferred using the 8 data buslines DB_0-DB_7.

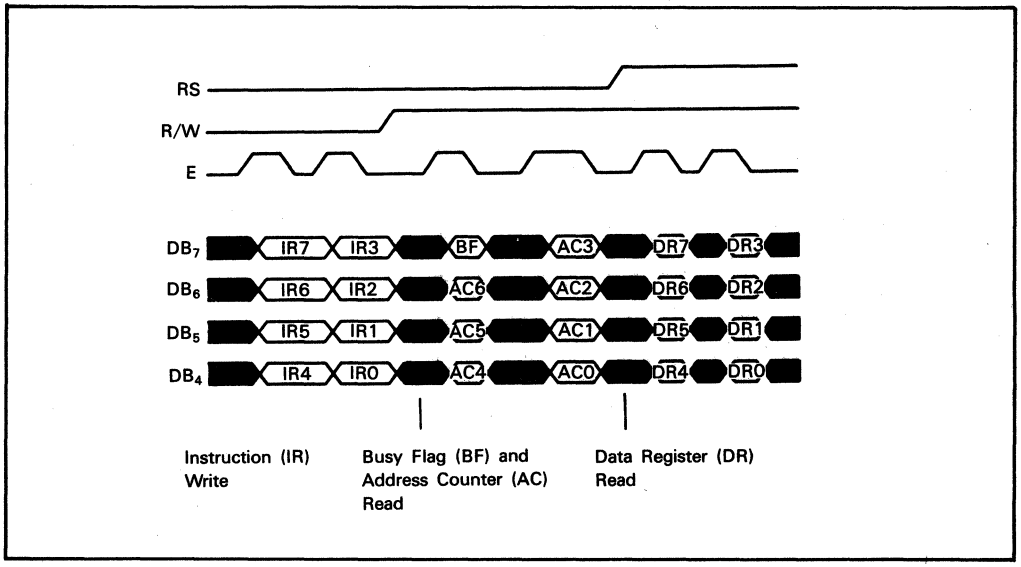


Figure 5 4-Bit Data Transfer Example

4

Reset Function

Initializing by Internal Reset Circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed during initialization. The busy flag (BF) is kept in busy state until initialization ends (BF = 1). The busy state is 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1: 8 bit long interface data
   N = 0: 1-line display
   F = 0: 5 × 7 dot character font
3. Display on/off control:
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blink off
4. Entry mode set:
   I/D = 1: +1 (increment)
   S = 0: No shift

Note: When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required. Use the procedure in figures 6 and 7 for initialization.

1:

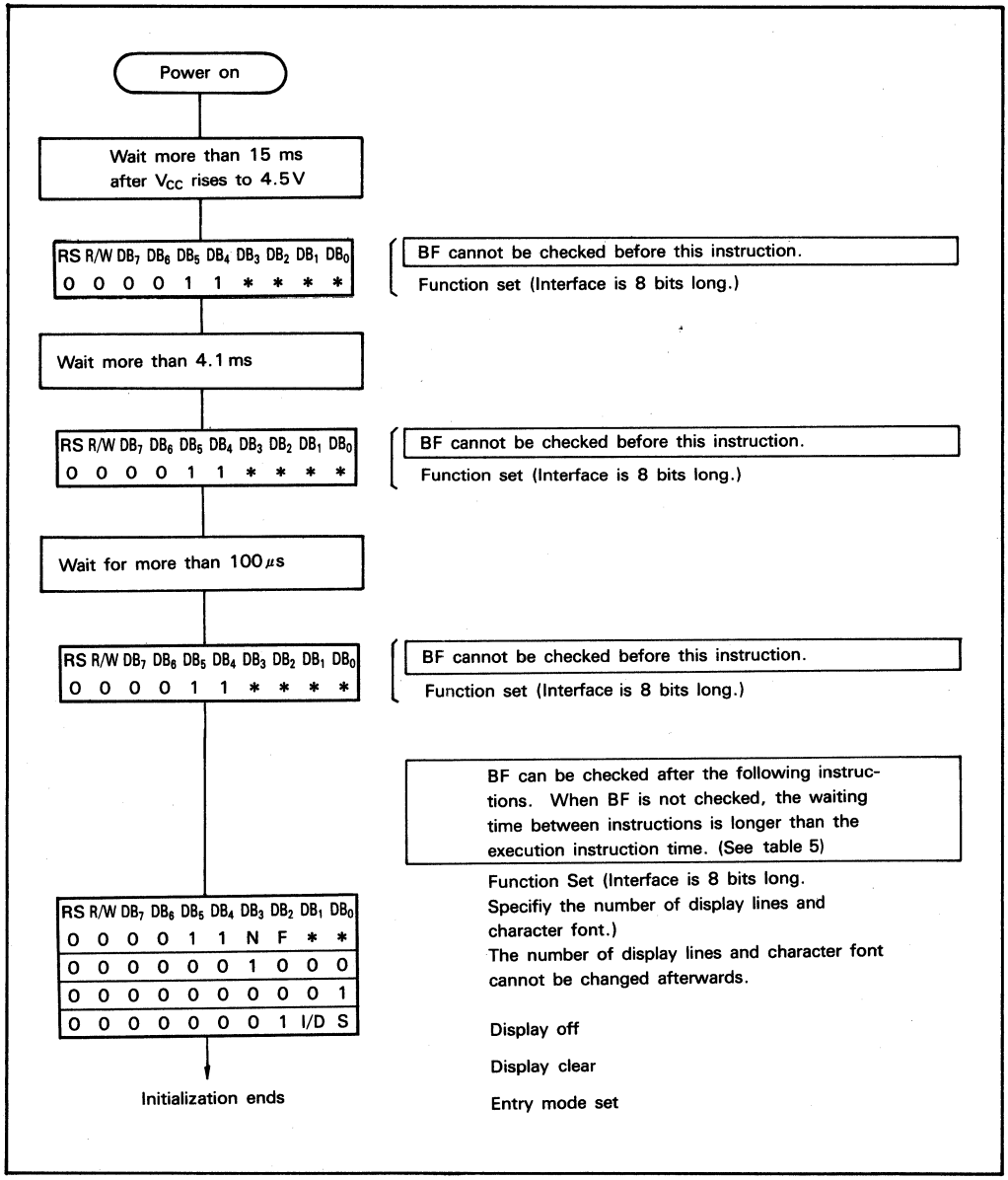


Figure 6 8-Bit Interface

2:

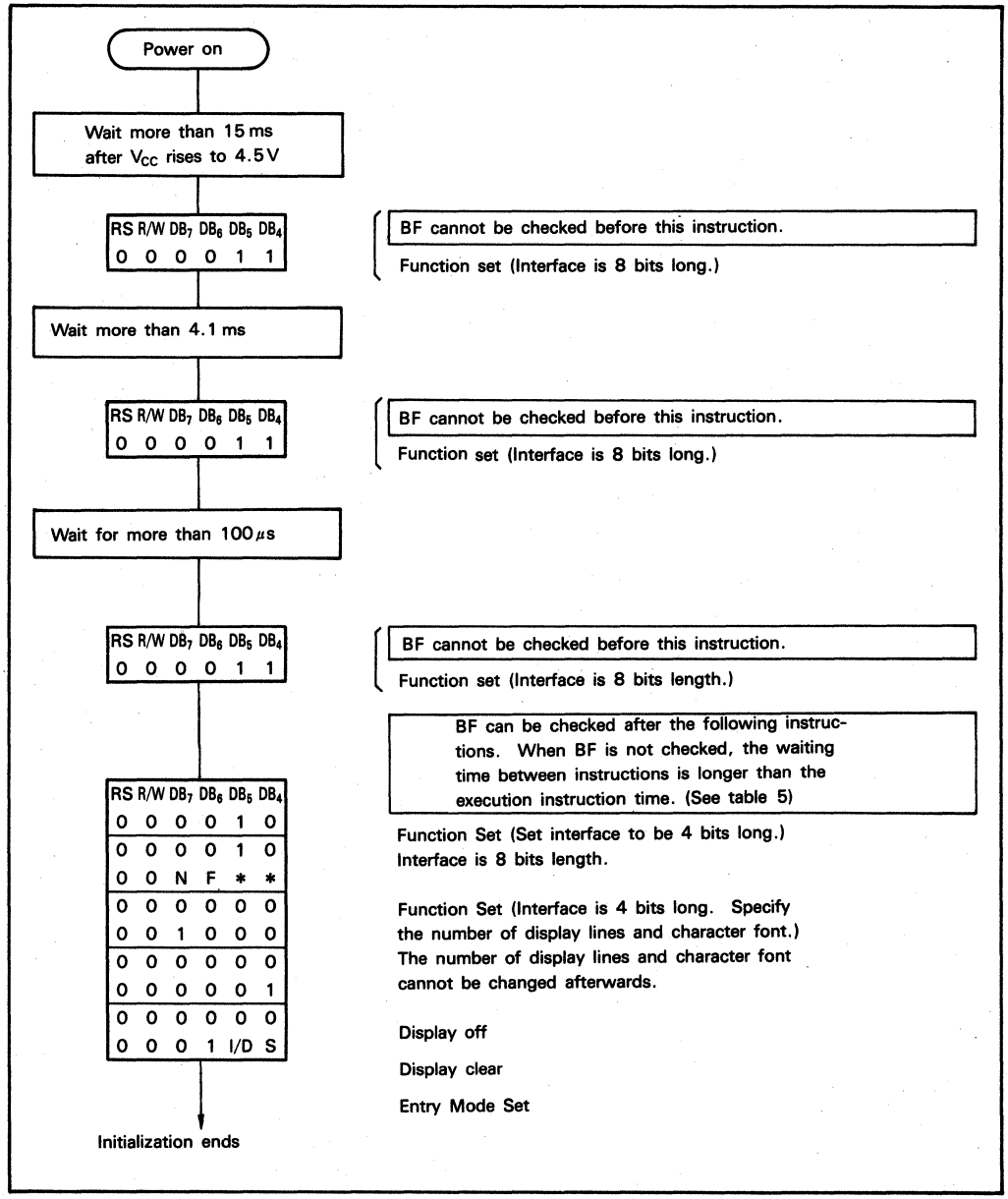


Figure 7 4-Bit Interface

Instructions

Outline

Only two HD44780 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs that operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals (OB_0-DB_7), and are here called instructions. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

1. Designate HD44780 functions such as display format, data length, etc.
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by −1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 7.

When an instruction is executing during internal operation, no insruction other than the busy flag/address read instruction will be executed.

Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is 1 before sending an instruction from the MPU.

Notes: 1. Make sure the HD44780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See table 5 for a list of each instruction execution time.

2. After execution of a CG RAM/DD RAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off. In figure 7 t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

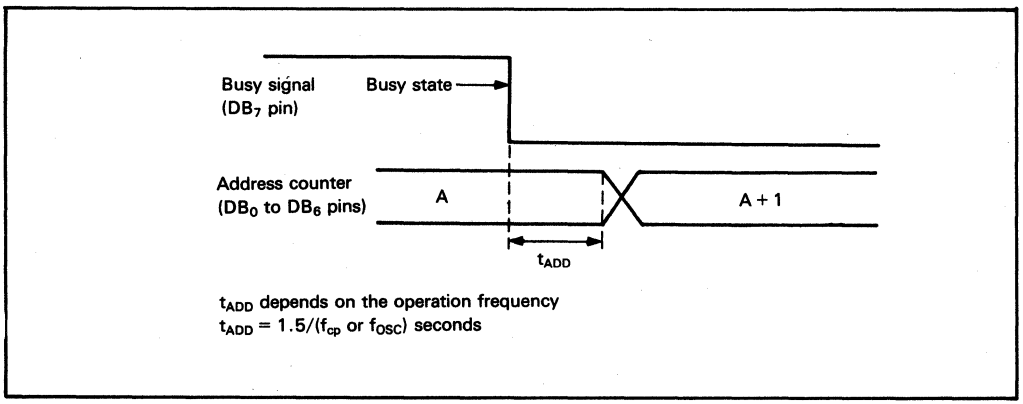


Figure 8 Address Counter Update

Table 5 Instructions

Instruction	Code										Description	Execution Time (max) (when fcp or fosc is 250 kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40μs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40μs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and recevied after this setting.	40μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40μs t_{ADD} = 6 μs (Note 2)
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40μs t_{ADD} = 6 μs (Note 2)
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5×10 dots, F = 0: 5×7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address: Corresponds to cursor address AC: Adress counter used for both DD and CG RAM address.	Execution time changes when frequency changes Example: When fcp or fosc is 270 kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

* No effect

Description of Details

1. Clear Display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Writes space code 20 (hexadecimal) (character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (increment mode) in entry mode. S of entry mode doesn't change.

2. Return Home

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

*Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change.

The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

3. Entry Mode Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

I/O: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.
The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0.
Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM causes a shift when S = 0.

4

4. Display On/Off Control

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: The display is on when D = 1 and off when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed instantly by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5× 10 dot character font is selected (Figure 9).

B: The character indicated by the cursor blinks when B = 1 (Figure 9). The blink is displayed by switching between all blank dots and display characters at 409.6 ms intervals when fcp or fosc = 250 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of fcp or fosc. 406.9 × $\frac{250}{270}$ = 379.2 ms when fcp = 270 kHz.)

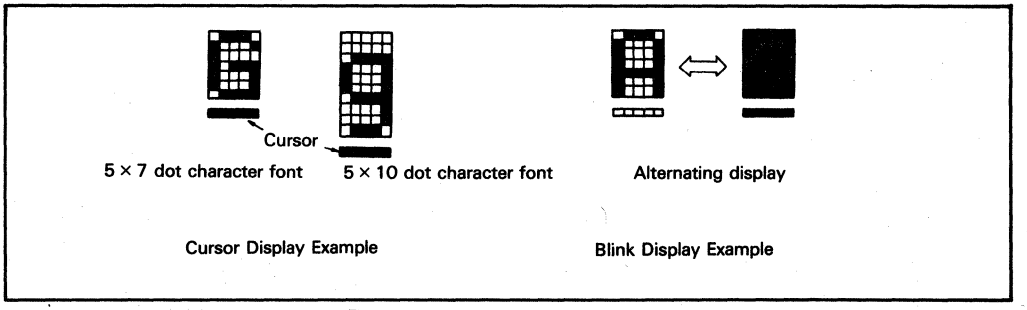
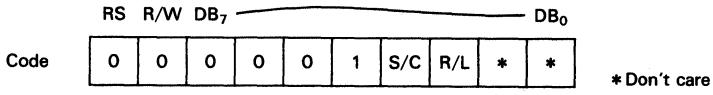


Figure 9 Cursor and Blink

5. Cursor or Display Shift

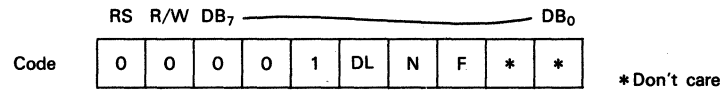


Shifts cursor position or display to the right or left without writing or reading display data (Table 6). This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time.

When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

Address counter (AC) contents do not change if the only action performed is display shift.

6. Function Set



DL: Sets interface data length. Data is sent or received in 8 bit lengths (DB_7-DB_0) when DL = 1 and in 4 bit lengths (DB_7-DB_4) when DL = 0. When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

Note: Perform the function at the head of the program before executing any instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

4

Table 6 Shift Function

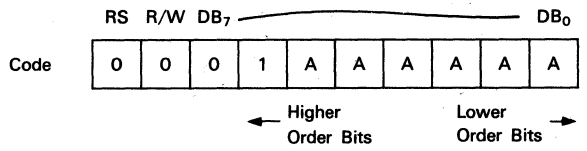
S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 7 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 7 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 7 dots	1/16	Cannot display 2 lines with 5 × 10 dot character font

* Don't care

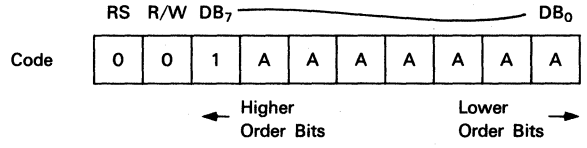
7. Set CG RAM Address



Sets the CG RAM address binary AAAAAA into the address counter.

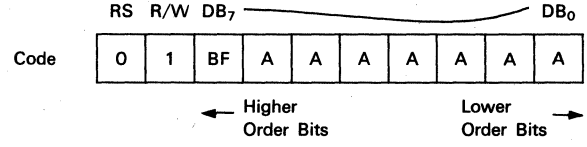
Data is then written or read from the MPU for the CG RAM.

8. Set DD RAM Address



Sets the DD RAM address binary AAAAAAA into the address counter.
Data is then written or read from the MPU for the DD RAM.
However, when N = 0 (1-line display), AAAAAAA can be 00-4F (hexadecimal).
When N = 1 (2-line display), AAAAAAA can be 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

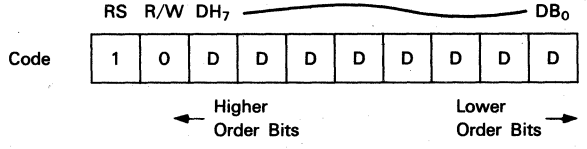
9. Read Busy Flag and Address



Reads the busy flag (BF) that indicates that the system is now internally operating on a previously received instruction.
BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF isset to 0. Check the BF status before the next wire operation.

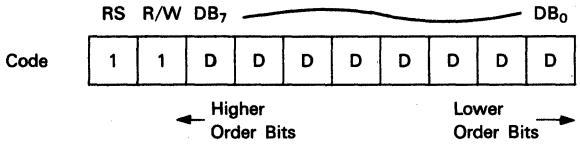
At the same time, the value of the address counter expressed in binary as AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in items 7 and 8.

10. Write Data to CG or DD RAM



Writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.
Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

11. Read Data from CG or DD RAM



Reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data readout are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out execute the "read" instruction from the second time the "read" instruction is sent.

4

How To Use The HD44780

Interface to MPU

1. Interface to 8-Bit MPU

When connecting to 8-bit MPU through PIA
Figure 10 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.
In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively.
Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

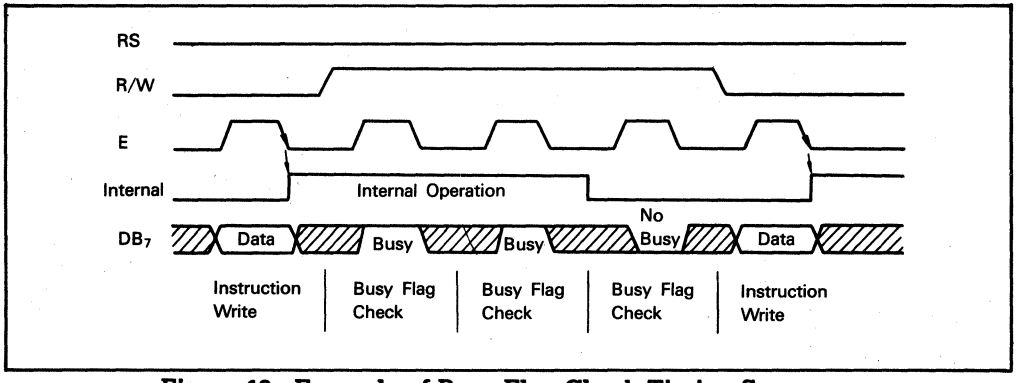


Figure 10 Example of Busy Flag Check Timing Sequence

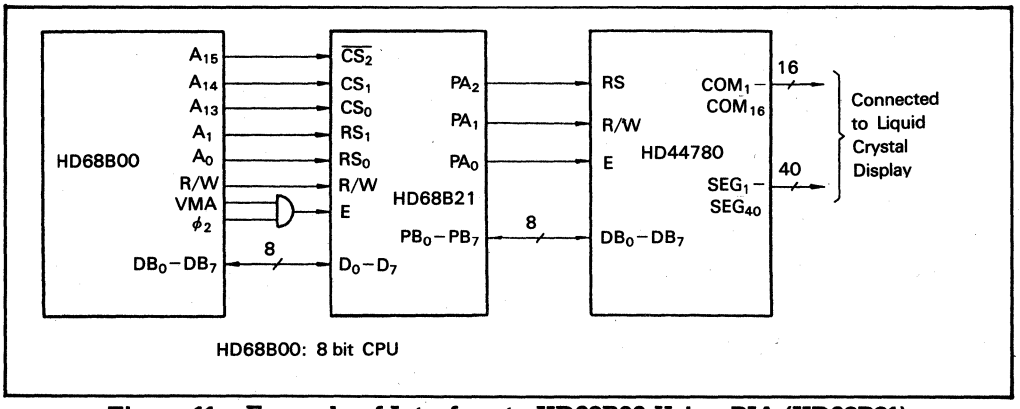


Figure 11 Example of Interface to HD68B00 Using PIA (HD68B21)

Connecting directly to the 8-bit MPU bus line

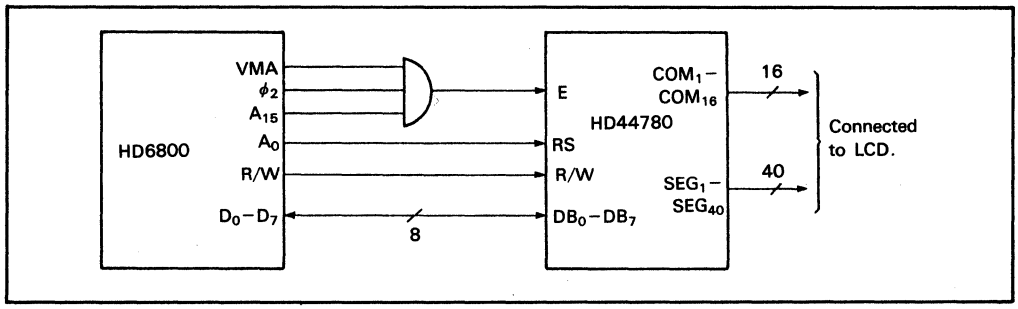


Figure 12 8-Bit MPU Interface

Example of interfacing to the HD6805

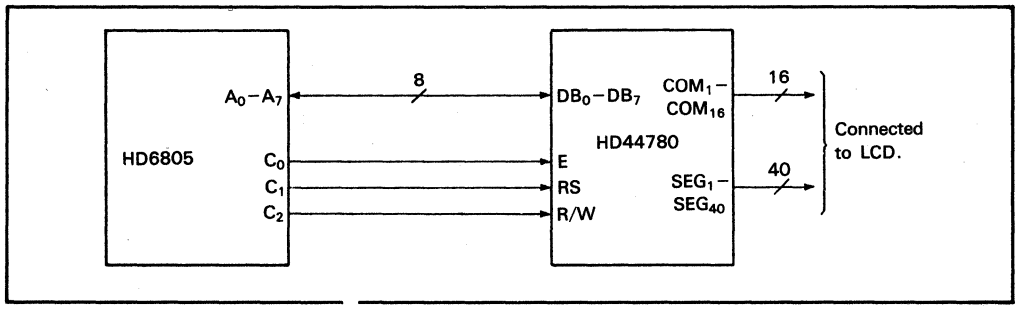


Figure 13 HD6805 Interface

Example of interfacing to the HD6301

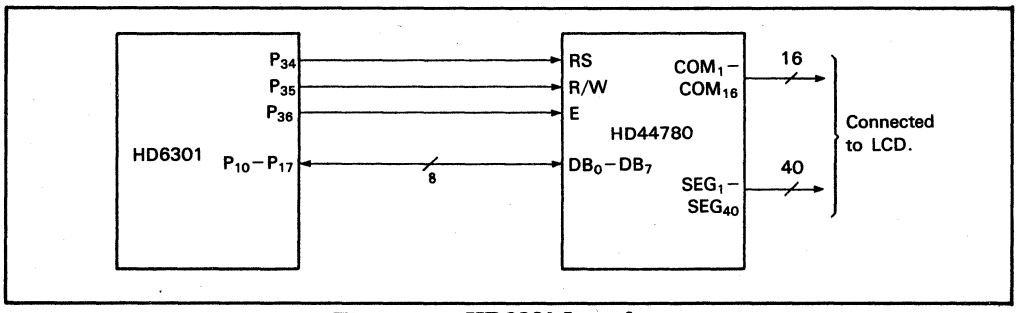
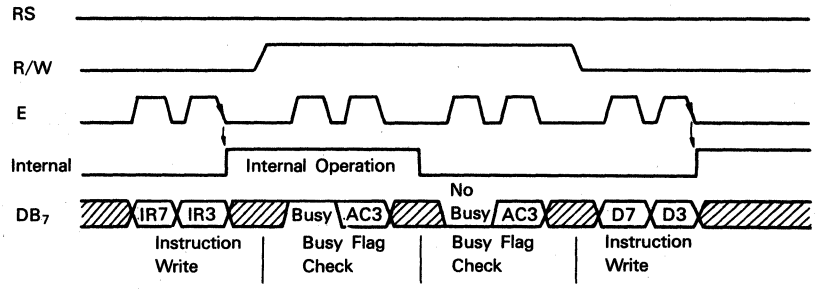


Figure 14 HD6301 Interface

4

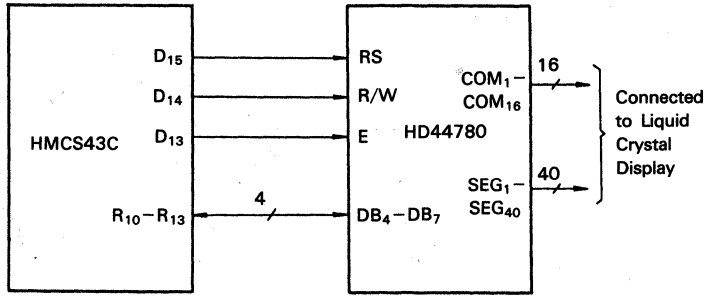
2. Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if there are insufficient bits, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See figure 15)
Figure 15 shows an example of interface to the HMCS43C.
Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.



Note: IR7, IR3: Instruction 7th bit, 3rd bit
AC3: Address Counter 3rd bit

Figure 15 An Example of 4-Bit Data Transfer Timing Sequence



HMCS43C: Hitachi 4-bit single-chip microcontroller

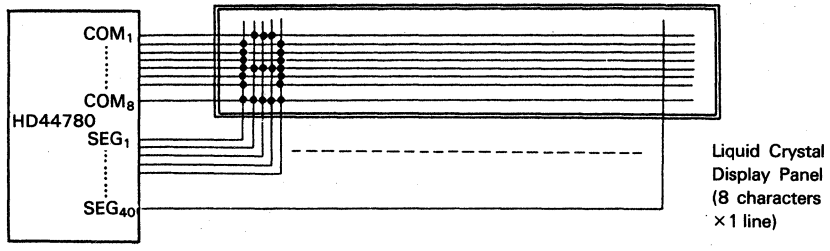
Figure 16 Example of Interface to the HMCS43C

Interface to Liquid Crystal Display

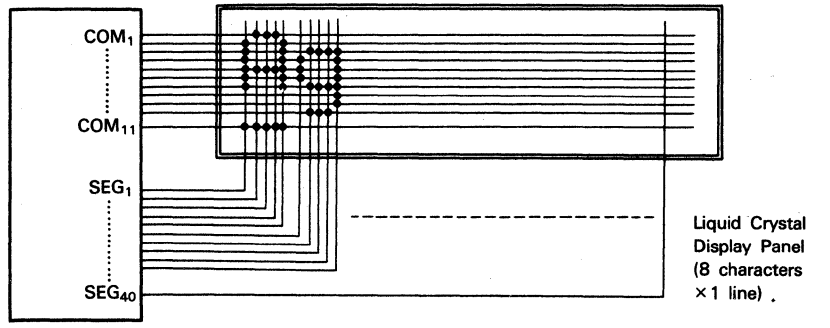
1. Character Font and Number of Lines
   The HD44780 can perform 2 types of display, 5 × 7 dots and 5 × 10 dots character font, with a cursor on each.
   Up to 2 lines are displayed with 5 × 7 dots and 1 line with 5 × 10 dots. Therefore, three types of common signals are available (Table 8).
   Number of lines and font types can be selected by program.
   (See to Table 5, Instructions)
2. Connection to HD44780 and Liquid Crystal Display
   Figure 17 shows connection examples.

Table 8 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + Cursor	8	1/8
1	5 × 10 dots + Cursor	11	1/11
2	5 × 7 dots + Cursor	16	1/16



(a) Example of a 5×7 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

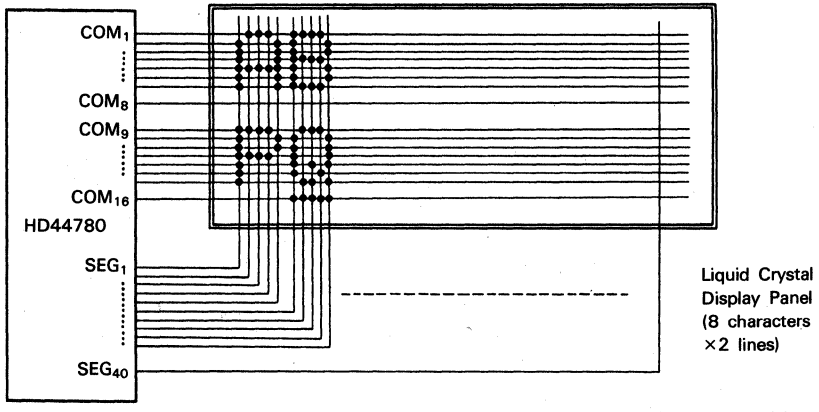


(b) Example of a 5×10 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

Figure 17 Liquid Crystal Display and Connections to HD44780

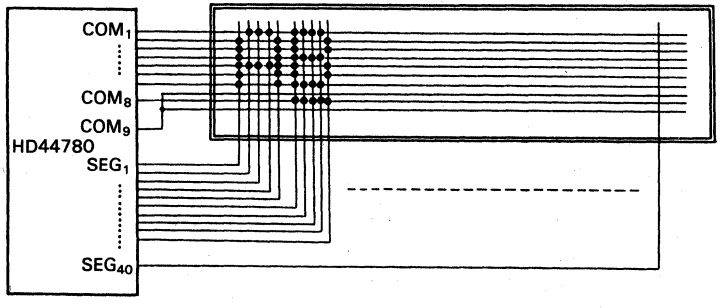
4

Since 5 SEG signal lines can display one digit, one HD44780 can display up to 8 digits for 1-line display and 16 digits for 2-line display.
In Figure 15 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to crosstalk in the floating state by connecting the extra scanning lines to these common signal terminals (Figure 18).



(c) Example of 5×7 dot, 8 character×2 lines Display (1/5 Bias, 1/16 Duty Cycle)

Figure 17 Liquid Crystal Display and Connections to HD44780 (cont)

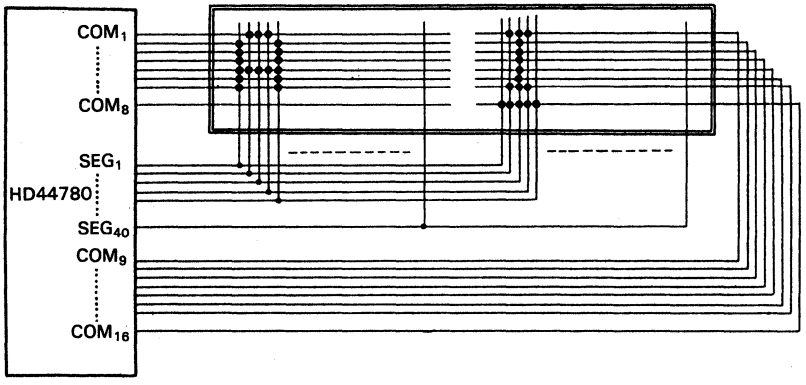


5×7 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

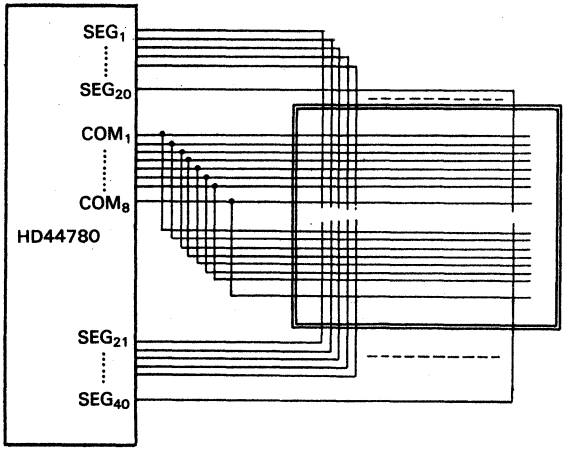
Figure 18 Using COM_9 to Avoid Crosstalk on Unneeded Scanning Line

3. Connection of Changed Matrix Layout

In the preceding examples, the number of lines matched the number of scanning lines. The display types figure 17 are made possible by changing the matrix layout in the liquid crystal display panel. In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in figure 15.



5×7 dot, 16 character×1 line Display
(1/5 Bias, 1/16 Duty Cycle)



5×7 dot, 4 character×2 line Display
(1/4 Bias, 1/8 Duty Cycle)

Figure 19 Changed Matrix Layout Displays

4

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD44780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 9 shows the relation.

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in figure 20.

Table 9. Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor / Power Supply \ Bias	1/8, 1/11 1/4	1/16 1/5
V_1	$V_{CC}-1/4\ V_{LCD}$	$V_{CC}-1/5\ V_{LCD}$
V_2	$V_{CC}-1/2\ V_{LCD}$	$V_{CC}-2/5\ V_{LCD}$
V_3	$V_{CC}-1/2\ V_{LCD}$	$V_{CC}-3/5\ V_{LCD}$
V_4	$V_{CC}-3/4\ V_{LCD}$	$V_{CC}-4/5\ V_{LCD}$
V_5	$V_{CC}-V_{LCD}$	$V_{CC}-V_{LCD}$

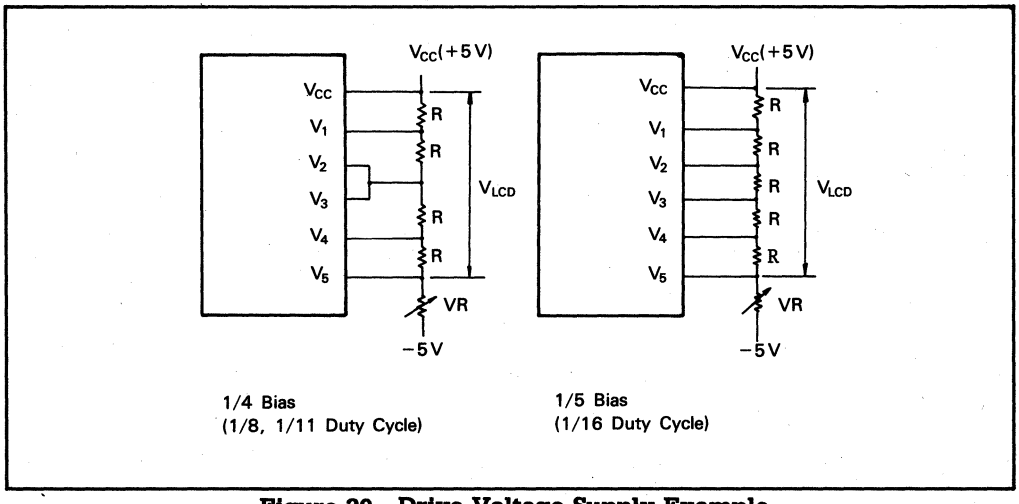
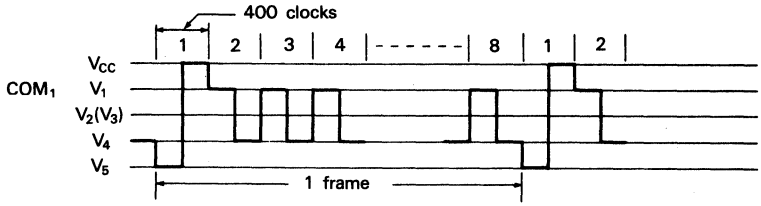


Figure 20 Drive Voltage Supply Example

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The examples in figure 21 of liquid crystal display frame frequency apply only when oscillation frequency is 250 kHz (1 clock = 4 μs).

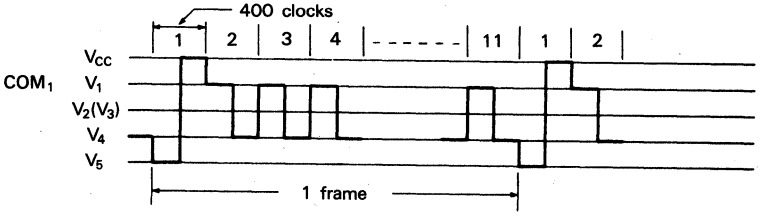
1. 1/8 Duty Cycle



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

Frame frequency = $\frac{1}{12.8\,(\text{ms})}$ = 78.1 (Hz)

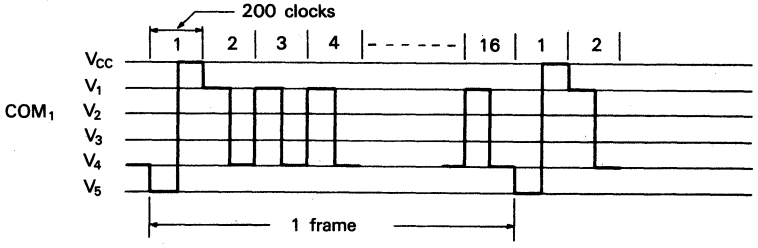
2. 1/11 Duty Cycle



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

Frame frequency = $\frac{1}{17.6\,(\text{ms})}$ = 56.8 (Hz)

3. 1/16 Duty Cycle



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

Frame frequency = $\frac{1}{12.8\,(\text{ms})}$ = 78.1 (Hz)

Figure 21 Frame Frequency

Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting an HD44100H liquid crystal display driver LSI to the HD44780. When connected to the HD44780, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD44780 directly since it supplies CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figure 22 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated.

Up to 9 HD44100H units can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 4 units for the 2-line display (duty factor 1/16). RAM size limits the HD44780 to a maximum of 80 character display digits. The connection method in figure 22 remains unchanged for both 1-line and 2-line display or 5 × 7 and 5 × 10 dot character fonts.

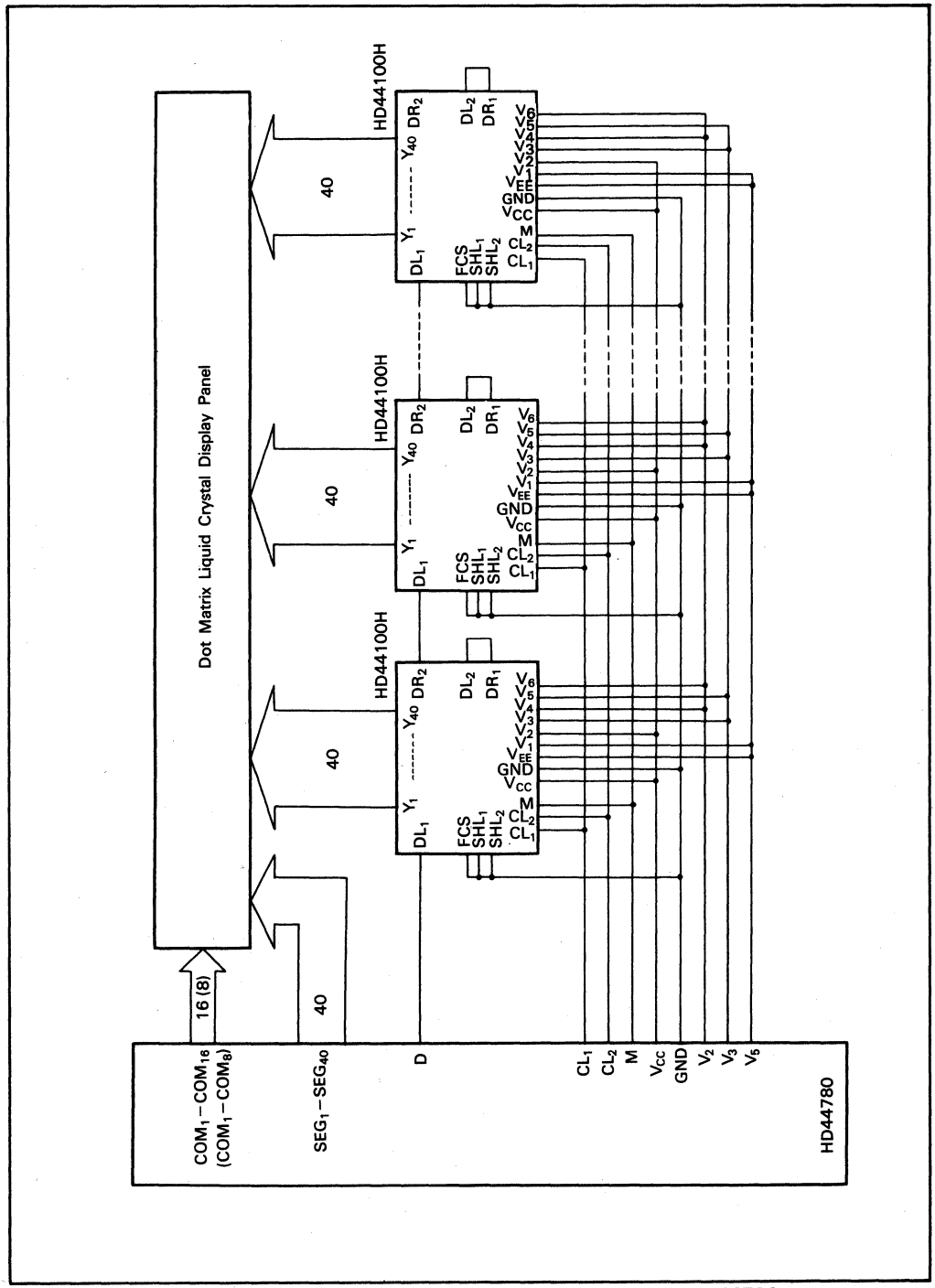


Figure 22 Example of Connecting HD44100H to HD44780

Instruction and Display Correspondence

1. 8-bit operation, 8-digit × 1-line display (using internal reset)

   Table 10 shows an example of 8-bit × 1-line display in 8-bit operation. The HD44780 functions must be set by funtion set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like a lighting board when combined with display shift operation.
   Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

2. 4-bit operation, 8-digit × 1-line display (using internal reset)

   The program must set functions prior to 4-bit operation. Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to DB_0-DB_3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as a function (see table 11). Thus, DB_4-DB_7 of the function set is written twice.

3. 8-bit operation, 8-digit × 2-line display

   For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See table 12). Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD44780 must be initialized by insruction. (See "Initializing by Instruction")

Table 10 8-Bit Operation, 8-Digit 1-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed after this.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI	Writes "I".
7	:	:	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M	Writes "M".
12	:	:	

4

No.	Instruction	Display	Operation
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts the display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	. . . . .	. . . . .	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

Table 11 4-Bit Operation, 8-Digit 1-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ⁓ DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5 × 7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

Table 12 8-Bit Operation, 8-Digit × 2-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD44780 is intialized by the internal reset circuit)		Initalized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	:	:	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	:	:	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift operate at the same time.
14	:	:	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

Modifying Character Patterns

1. Character Pattern Development Procedure

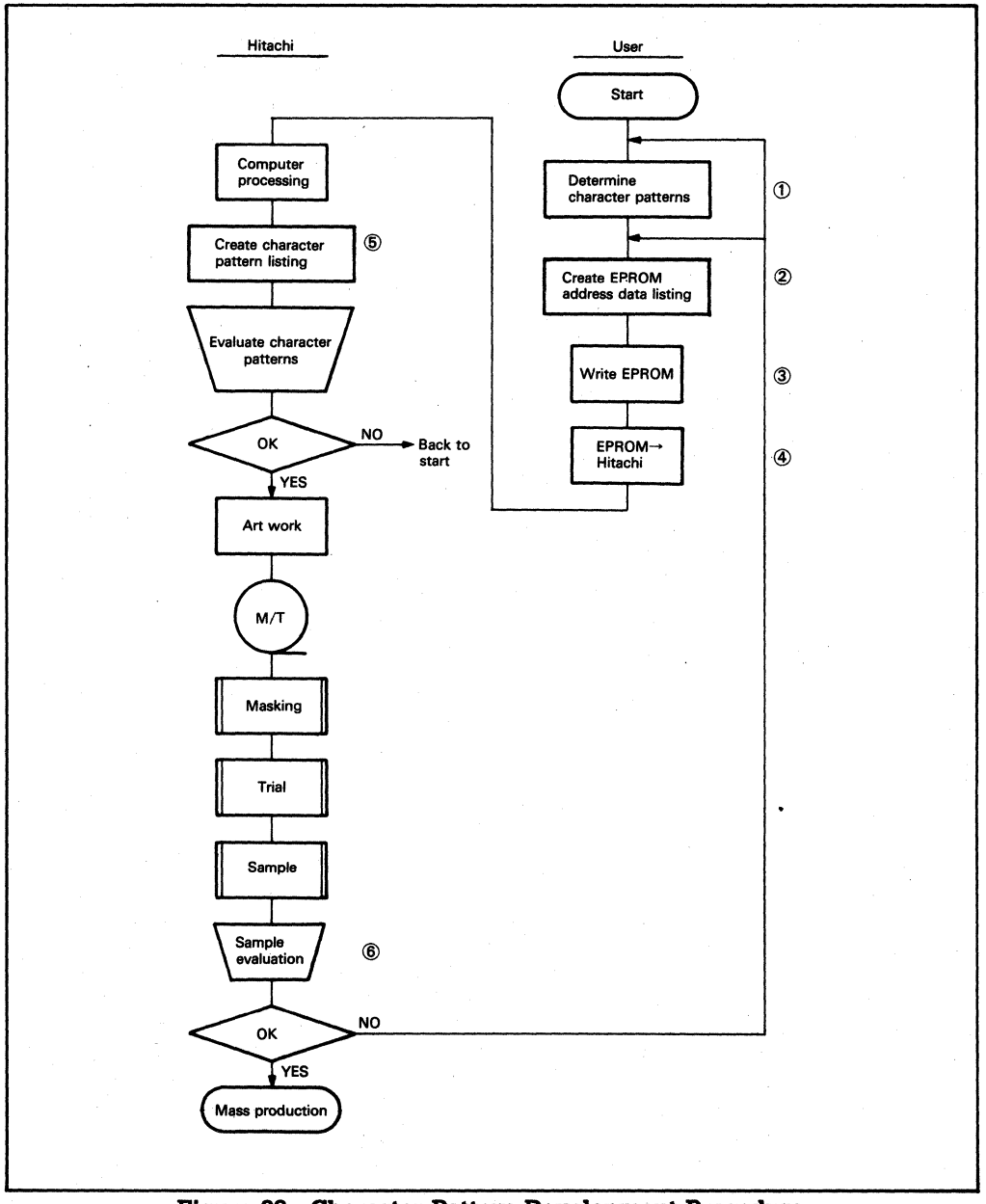


Figure 23 Character Pattern Development Procedure

The numbers in figure 17 correspond to the following operations:

a. Determine the correspondence between character codes and character patterns.

b. Create a listing indicating the correspondence between EPROM addresses and data.

c. Program character patterns in the EPROM.

d. Send the EPROM to Hitachi.

e. Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.

f. If there is no problem in the character pattern listing, Hitachi creates a trial LSI and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, Hitachi starts mass production of the LSI.

2. Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II character generator ROM can generate 160 5 × 7-dot character patterns and 32 5 × 10-dot character patterns for a total of 192 different character patterns.

a. 5 × 7-dot Character Pattern

For a 5×7-dot character pattern, EPROM address data and character pattern correspond with each other as shown below. Table 13 is an example of the correspondence between EPROM address data and character pattern (5 × 7 dots).

Table 13 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 7 dots)

EPROM address											Data				
															(LSB)
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0

Fill line 8 (cursor position) with 0

Character code — Line position

(1) EPROM addresses A_{10} to A_3 correspond to a character code.
(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.
(3) EPROM data O_4 to O_0 correspond to character pattern data.
(4) A lit display position (black) corresponds to 1.
(5) Fill line 8 (cursor position) of character pattern with 0.
(6) EPROM data O_5 to O_7 are not used.

b. 5 × 10-dot Character Pattern

For a 5×10-dot character pattern, EPROM address data and character pattern correspond with each other as shown in table 14.

(1) EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern line 9 and later lines to 0.
(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.
(3) EPROM data O_4 to O_0 correspond to character pattern data.
(4) A lit display position (black) corresponds to 1.
(5) Fill line 11 (cursor position) of character pattern with 0.
(6) EPROM data O_5 to O_7 are not used.

c. Handling Unused Character Patterns

(1) EPROM data outside the character pattern area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(2) EPROM data in CG RAM area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(3) EPROM data used when the user does not use any LCD-II character pattern
Handled in one of the two ways explained below. Select one of the two ways according to the user application.

(a) When unused character patterns are not programed
If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1 when the EPROM is erased.)

(b) Program 0 for unused character patterns
Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (This is equivalent to space).

Table 14 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM address											Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1 (LSB)	O_0
								0	0	0	0	0	0	0	0
								0	0	1	0	0	0	0	0
								0	1	0	0	1	1	0	1
1	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1
								1	0	0	1	0	0	0	1
								1	0	1	1	0	0	0	1
								1	1	0	0	1	1	1	1
								1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0

Fill line 11 (cursor position) with 0.

Character code

Line position

HD66780 (LCD-IIA)
(Dot Matrix Liquid Crystal Display Controller and Driver)

Description

The LCD-IIA (HD66780) a dot matrix liquid crystal display controller and driver LSI displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microcontroller or microprocessor control. All the functions required for driving a dot matrix liquid crystal display are internally provided on one chip.

Designers can complete dot matrix liquid crystal display systems with low chipcount by using the LCD-IIA (HD66780). If a driver LSI (HD44100H or HD66100F) is connected to the HD66780, up to 80 characters can be displayed.

The LCD-IIA is produced by the CMOS process. Therefore, the combination of the LCD-IIA with a CMOS microcontroller or microprocessor can complete a portable battery-driven device with low power dissipation.

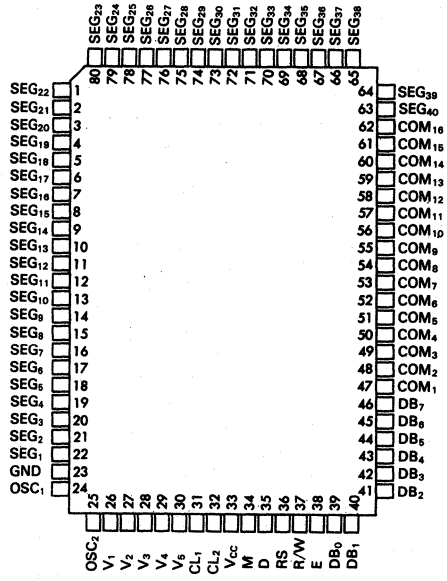
Features

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Can interface to 4-bit or 8-bit MPU
- Display data RAM: 80 × 8 bits (80 characters, max)
- Character generator ROM: 12000 bits; Character font 5×10 dots: 240 characters
- Character generator RAM: 64 × 8 bits; Character font 5×8 dots: 8 characters or character font 5 × 11 dots: 4 characters
- Both display data and character generator RAMs can be read from the MPU
- Internal liquid crystal display driver
  −16 common signal drivers
  −40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H or HD66100F)
- Duty factor selection (selectable by program)
  −1/8 duty: 1 line of 5 × 7 dots + cursor
  −1/11 duty: 1 line of 5 × 10 dots + cursor
  −1/16 duty: 2 lines of 5 × 7 dots + cursor
- Maximum number of display characters as shown in table 1
- Wide range of instruction functions: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Internal automatic reset circuit at power on (internal reset circuit)
- Internal oscillation circuit
  −External resistor or ceramic filter
  −External clock operation possible
- CMOS process
- Single +5 V logic power supply (excluding power for liquid crystal display drive)
- Operation temperature range: -20°C to +75°C (-40°C to +85°C device available upon request)
- 80-pin plastic flat package (FP-80B, FP-80A)
- Low power consumption

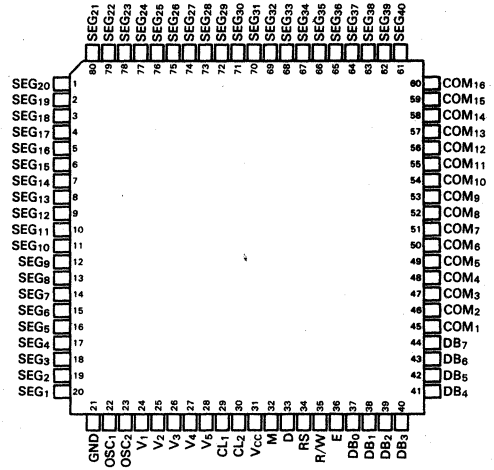
Ordering Information

Type No.	Package
HD66780FS	80-pin plastic QFP (FP-80B)
HD66780FH	80-pin plastic QFP (FP-80A)

Pin Arrangement



(FP-80)



(FP-80A)

(Top-View)

Pin Description

Signal	No. of Lines	I/O	Connected to	Function
RS	1	Input	MPU	Selects register
R/W	1	Input	MPU	Selects read or write
E	1	Input	MPU	Starts data read or write
DB_7-DB_0	8	I/O	MPU	Bidirectional data bus
CL_1	1	Output	Driver LSI	Serial data latch clock
CL_2	1	Output	Driver LSI	Serial data shift clock
M	1	Output	Driver LSI	LCD waveform AC switch signal
D	1	Output	Driver LSI	Character pattern data
COM_1-COM_{16}	16	Output	LCD	Common signals
SEG_1-SEG_{40}	40	Output	LCD	Segment signals
V_1-V_5	5		Power supply	LCD drive voltages
V_{CC}, GND	2		Power supply	+5 V and ground
OSC_1-OSC_2	2			System clock

Pin Function

RS (Register Select)

RS selects the register that the MPU is accessing. RS = 0 selects the instruction register for MPU writes, and the busy flag and address counter for reads. RS = 1 selects the data register for MPU reads and writes.

R/W (Read/Write)

R/W selects whether the MPU will read from (R/W = 1) or write to (R/W = 0) the LCD-IIA.

E (Enable)

The MPU sets the E input high to signal the start of the read/write operation.

DB_7–DB_0 (Data Bus)

The bidirectional, three-state data bus, DB_0–DB_7, transfers data between the MPU and the LCD-IIA. DB_7 can be used as the busy flag. The lower-order four lines, DB_0–DB_4, are not used in four-bit interface operation.

CL_1, CL_2 (Clock 1, Clock 2)

The CL_1 output signals the HD44100H or HD66100F driver LSI to latch the serial data sent on line D. The CL_2 output signals it to shift the data.

M (Master AC Signal)

The HD44100H or HD66100F driver LSIs use the M output to convert the LCD drive waveform to AC.

D (Serial Data)

The LCD-IIA outputs serial character pattern data corresponding to the common signals to the HD44100H or HD66100F driver LSIs on D.

COM_1–COM_{16} (Common)

COM_1–COM_{16} are the LCD common lines. Common signals that are not used are deselected. At 1/8 duty factor COM_9–COM_{16} are not used, so they output non-selected waveforms. At 1/11 duty factor COM_{12}–COM_{16} are not used, so they output non-selected waveforms.

SEG_1–SEG_{40} (Segment)

SEG_1–SEG_{40} are the LCD segment lines.

V_1–V_5 (LCD Voltages)

The LCD-IIA requires the V_1–V_5 voltages to output LCD-driving waveforms.

V_{CC}, GND (Power Supply, Ground)

V_{CC} is the LCD-IIA's logic power supply. GND is the power supply ground.

OSC_1, OSC_2 (Oscillator 1, Oscillator 2)

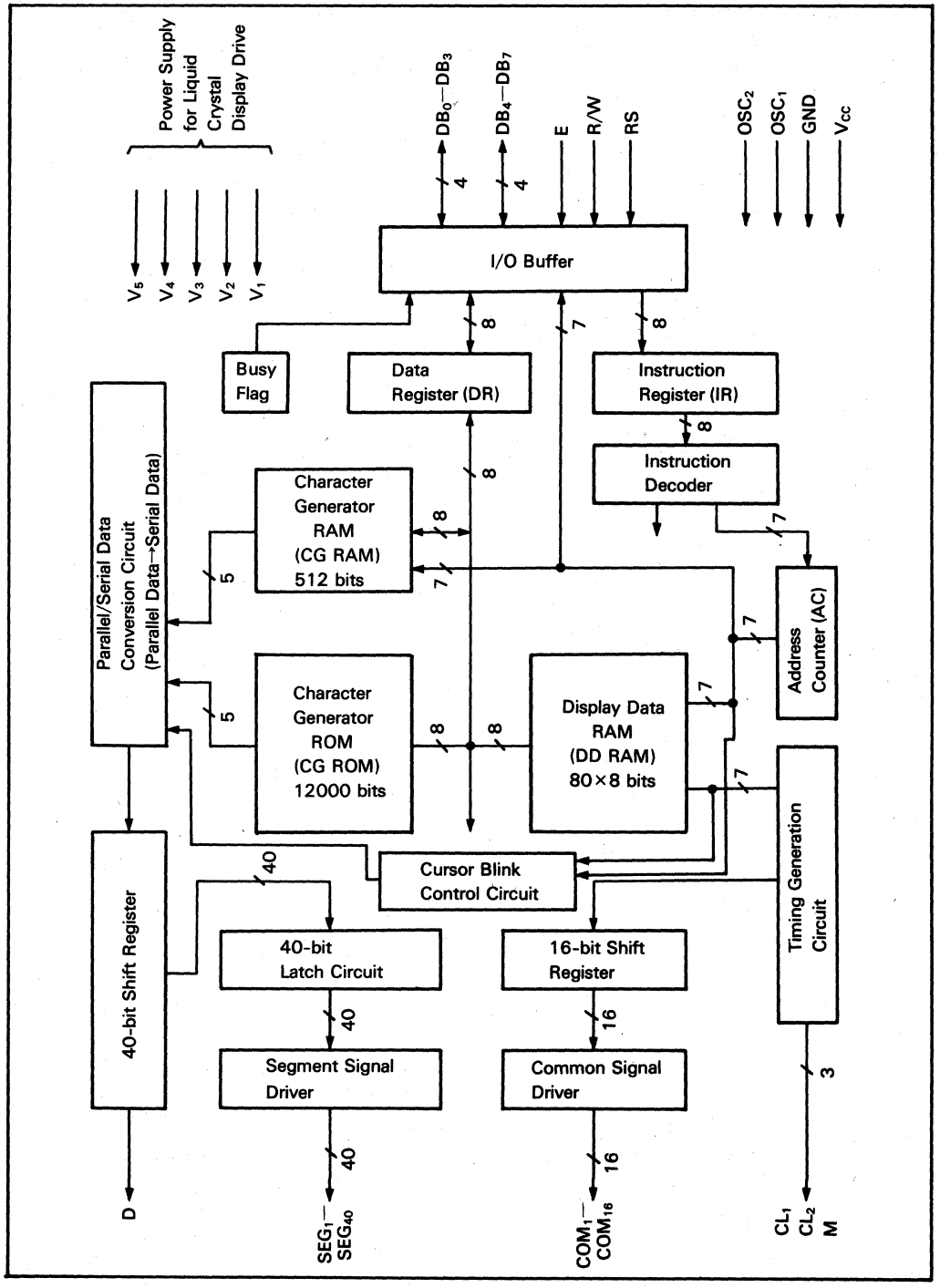
OSC_1 and OSC_2 are the connections for the LCD-IIA system clock. The LCD-IIA can use its internal oscillator if OSC_1 and OSC_2 are connected to a resistor or ceramic filter. An external clock can be input to OSC_1.

4

Table 1 Number of Display Characters

No. of Display Lines	Duty factor	Extension	HD44100H	HD66100F	No. of Display Characters
1-line display	1/8, 1/11 duty	Not provided	–	–	8 characters × 1 line
		Provided	9 pcs. (8 characters/pc.)	5 pcs. (16 characters/pc.)	80 characters × 1 line
2-line display	1/16 duty	Not provided	–	–	8 characters × 2 lines
		Provided	4 pcs.(8 characters × 2 lines/pc.)	2 pcs.(16 characters × 2 lines/pc.)	40 characters × 2 lines

HD66780 Block Diagram



Block Function

Registers

The HD66780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM internally. The MPU also uses the DR for data storage when reading data from the DD RAM or the CG RAM. When the MPU writes address information into the IR, the LCD-IIA sends data to the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, the LCD-IIA sends data in the DD RAM or CG RAM at the next address to the DR for the next read from the MPU. Register selector (RS) signals select these two registers (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66780 is in the internal operation mode, and instructions will not be accepted. As table 2 shows, the busy flag is output to DB $_7$ when RS = 0 and R/W = 1. The next instruction must be written after confirming that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD and CG RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by 1 (or decremented by 1). AC contents are output to DB_0-DB_6 when RS = 0 and R/W = 1, as shown in table 2.

Display Data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown in figure 1.

The DD RAM adress (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.

When there are fewer then 80 display characters, the display begins at the head positon. For example, 8 characters using an HD66780 are displayed as shown in figure 2.

When the display shift operation is performed, the DD RAM address moves as shown in figure 3.

A 16-character display using an HD66780 and an HD44100H is shown in figure 4.

The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD66780 and two or more HD44100Hs can be considered an extension of figure 4.

Since the increase can be 8 digits for each

4

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc)
0	1	Read busy flag (DB_7) and address counter (DB_0-DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

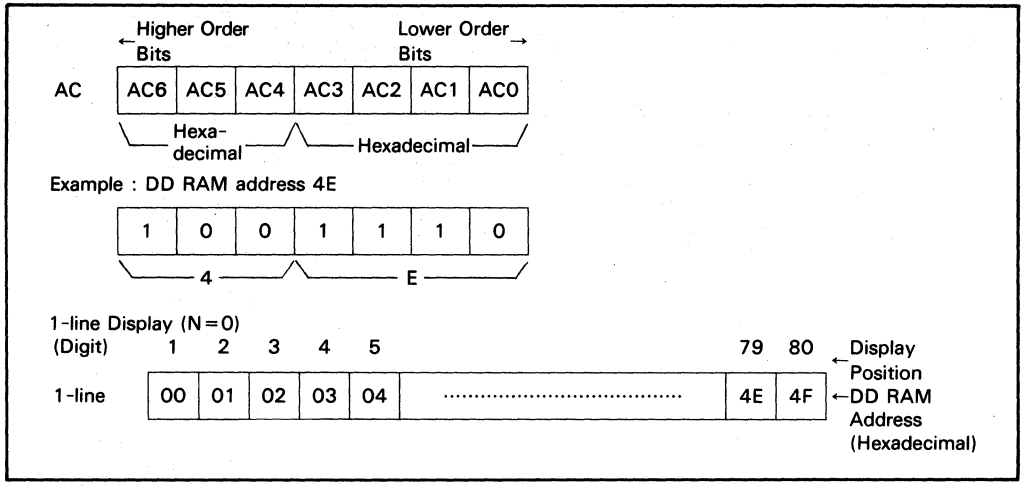


Figure 1 DD RAM Address

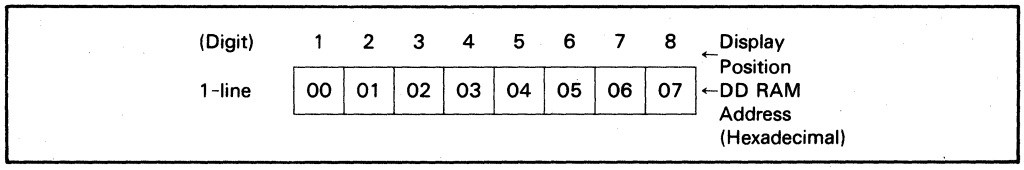


Figure 2 Eight-Character Display Example

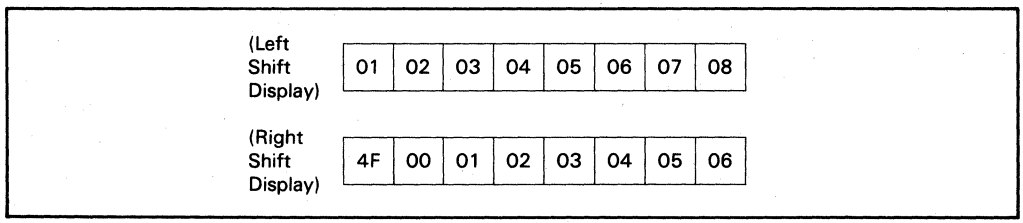


Figure 3 Display shift

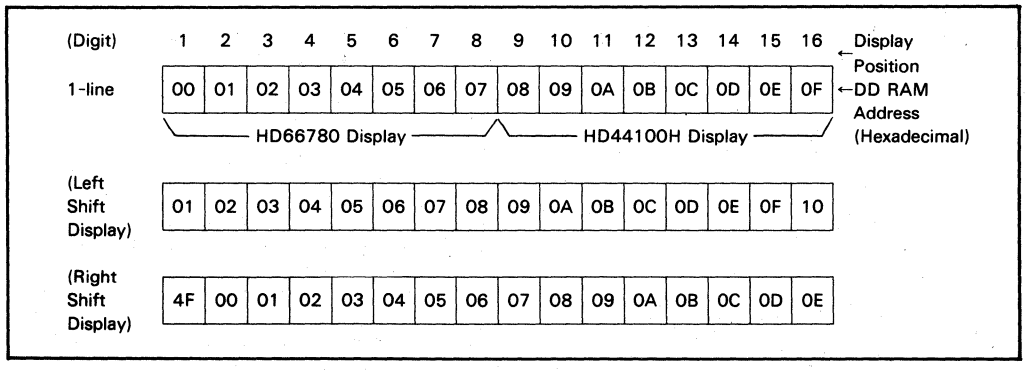


Figure 4 Sixteen-Character Display Example

additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100Hs.

The same holds when HD66100Fs are used as display drivers. Consisting of 80 outputs, one HD66100F can display 16 digits (figure 5).

When the number of display characters is fewer than 40×2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD66780 is used, 8 characters × 2 lines are displayed as shown in figure 6.

When display shift is performed, the DD RAM address moves as shown in figure 7.

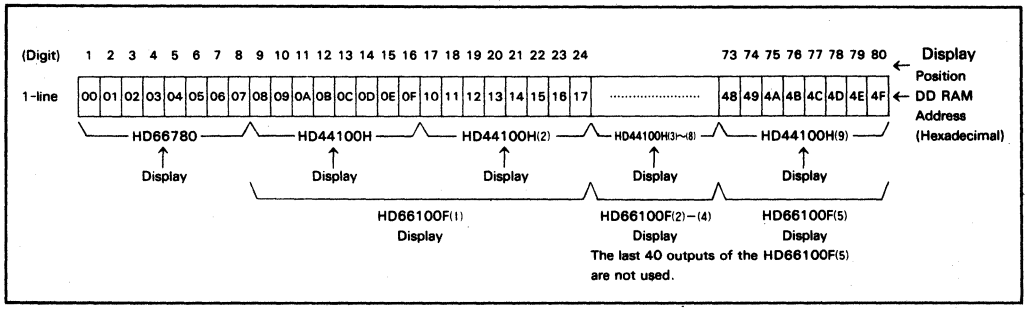


Figure 5 Extended Display

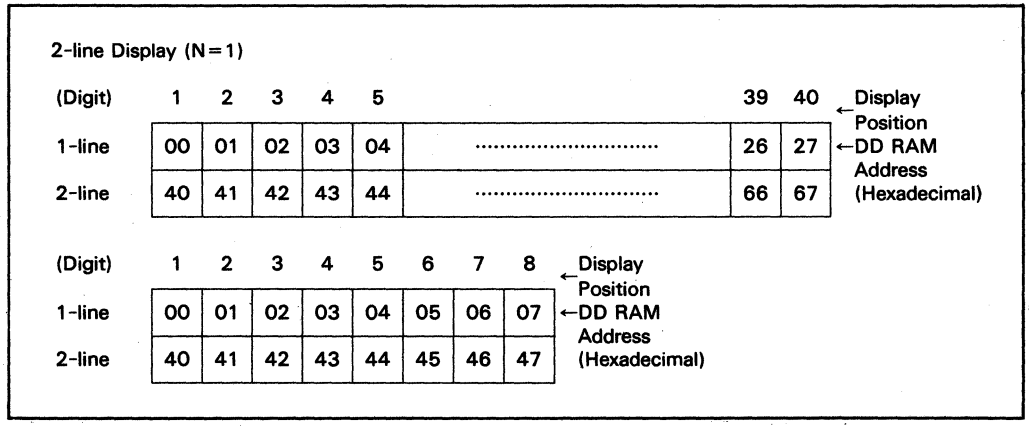


Figure 6 Two-Line by Eight-Character Display Example

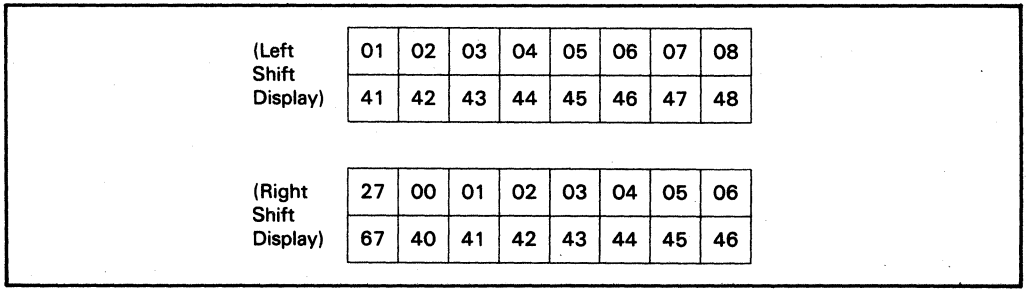


Figure 7 Two-Line Display Shift

16 characters × 2 lines are displayed as in figure 8 when an HD66780 and an HD44100H are used.

The relation between display position and DD RAM address when the number of display digits is increased by using one HD66780 and two or more HD44100Hs, can be considered an extension of figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits × 2 lines can be displayed by connecting 4 HD66780s (or 2 HD66100Fs) externally.

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. A CG ROM has 240 types of 5 × 10 dot character patterns built-in. (Note: In a 5 × 7 dot + cursor display, only the upper part, that is, 5 × 7 dots of 5 × 10 dots, is displayed.)

Table 3 shows the relation between character codes and character patterns in the Hitachi standard HD66780A00. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

With the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots 4 patterns can be written.

Write the character codes in the left columns of table 3 to display character patterns stored in CG RAM.

(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	(Hexadecimal)
	HD66780 Display								HD44100H Display								
(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	
(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

Figure 8 Two-Line by Sixteen-Character Display Example

(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	.....	33	34	35	36	37	38	39	40	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	.....	20	21	22	23	24	25	26	27	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	.....	60	61	62	63	64	65	66	67	(Hexadecimal)
	HD667780 Display								HD44100H(1) Display								HD44100H(2)(3) Display					HD44100H(4) Display								
									HD66100F(1) Display													HD66100F(2) Display								

Figure 9 Two-Line Extended Display Example

Table 3 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD66780A00)

Lower 4 Bits \ Higher 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
××××0000	CG* RAM (1)															
××××0001	(2)															
××××0010	(3)															
××××0011	(4)															
××××0100	(5)															
××××0101	(6)															
××××0110	(7)															
××××0111	(8)															
××××1000	(1)															
××××1001	(2)															
××××1010	(3)															
××××1011	(4)															
××××1100	(5)															
××××1101	(6)															
××××1110	(7)															
××××1111	(8)															

Note: * The user can specify any pattern for character-generator ROM.

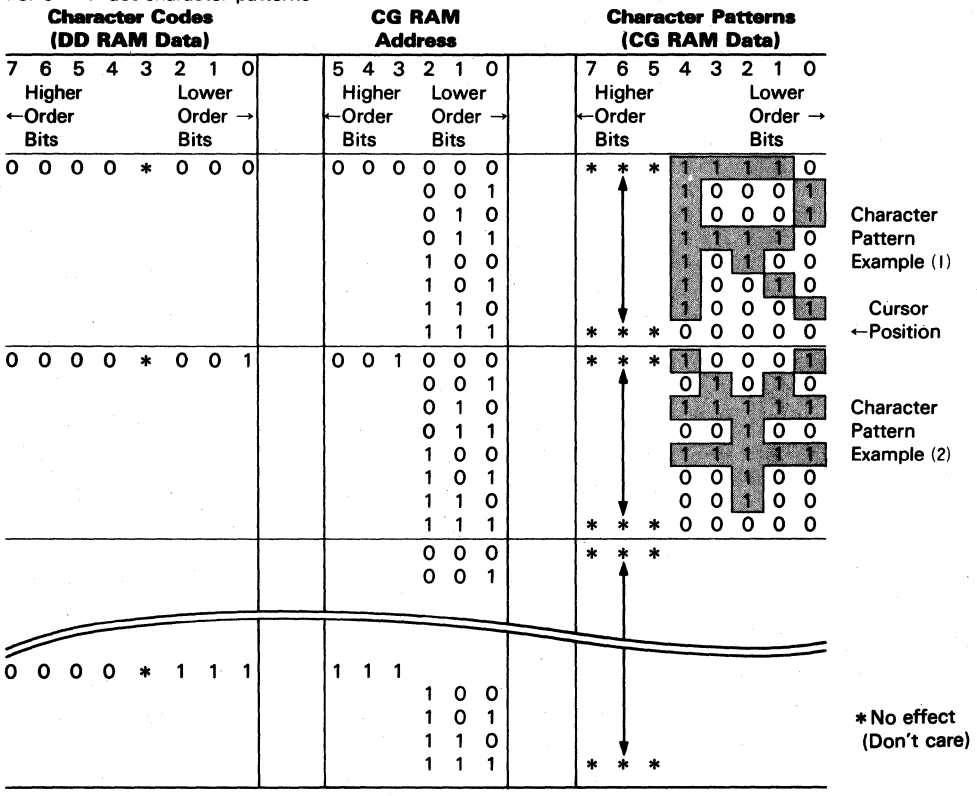
4

Table 4 shows the relation between CG RAM addresses and data and display patterns.

As table 4 shows, an area that is not used for display can be used as general data RAM.

Table 4 Relation between CG RAM Address and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

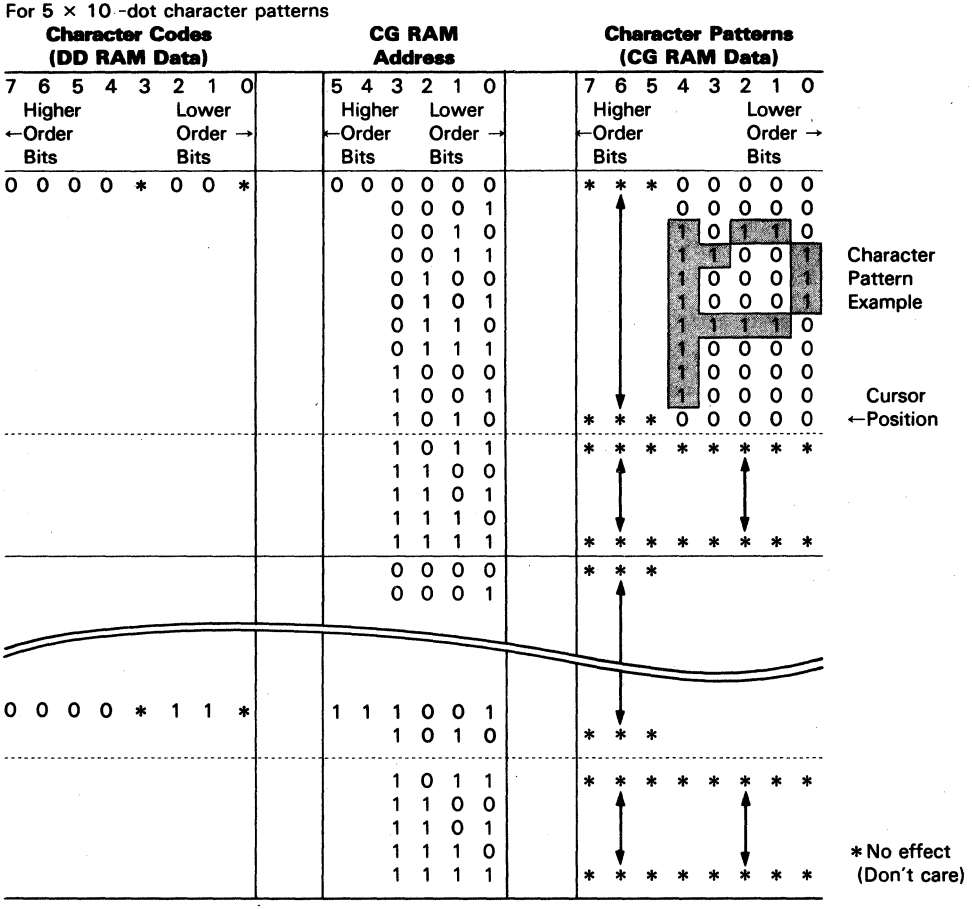
For 5 × 7-dot character patterns



Notes:
1. Character code bits 0-2 correspond to CG RAM address bits 3-5 (3 bits: 8 characters).
2. CG RAM address bits 0-2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0-4, as shown in the figure (bit 4 being at the left end).
   Since CG RAM data bits 5-7 are not used for display, they can be used for the general data RAM.
4. As shown in table 3 and 4, CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 3 is ineffective, the R display in the character pattern example, is selected by character code 00 (hexadecimal) or 08 (hexadecimal).
5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

Table 4 Relation between CG RAM Address and Character Codes (DD RAM) and Character Patterns (CG RAM Data) (Cont)

For 5 × 10-dot character patterns



Notes:
1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 characters).
2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is performed by logical OR with cursor.
   Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor presence. Since the 12nd-16th lines are not used for display, they can be used for the general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 are ineffective, P display in the character pattern example is selected by character code 00, 01, 08 and 09 (hexadecimal).
5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

Timing generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM, and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so that they may not interfere with each other. Therefore, when writing data to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected drivers (HD44100H or HD66100F).

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms. The other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data can be sent to HD44100H or HD66100Fs, externally connected in cascade, to display an extended number of characters.

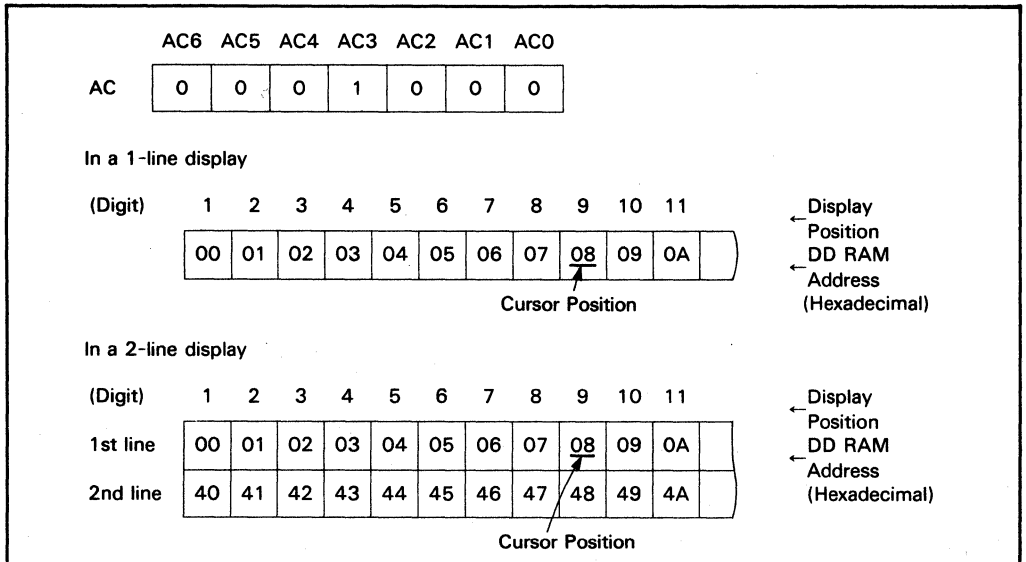
The LCD-IIA always starts sending serial data at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD66780 drives the head of the display. The rest of the display, corresponding to later addresses, are added with each additional HD44100H or HD66100F.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or blinking. The cursor or blinking appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, the cursor position is as shown in figure 10.



Note: The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

Figure 10 Cursor or Blink

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MPU Interface

The HD66780 can send data in either two 4-bit operations or one 8-bit operation so it can interface to both 4-and 8-bit MPU's.

When interface data is 4 bits long, data is transferred using only 4 bus lines: DB_4–DB_7. DB_0–DB_3 are not used. Data transfer between the HD66780 and the MPU completes when 4-bit data is transferred twice.

Data of the higher order 4 bits (contents of DB_4–DB_7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB_0–DB_3 when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bit data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data (figure 11).

When the interface is 8 bits long, data is transferred using the 8 data bus lines DB_0–DB_7.

Reset Function

Initializing by Internal Reset Circuit

The HD66780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed at initialization. The busy flag (BF) is kept in busy state until initialization ends (BF = 1). The busy state lasts 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set
   a. DL = 1: 8-bit long interface data
   b. N = 0: 1-line display
   c. F = 0: 5×7-dot character font
3. Display on/off control
   a. D = 0: Display off
   b. C = 0: Cursor off
   c. B = 0: Blink off
4. Entry mode set
   a. I/D = 1: + 1(increment)
   b. S = 0: No shift

Note: When power supply conditions in the electrical characteristics are not met using internal reset circuit, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to initializing by instruction.

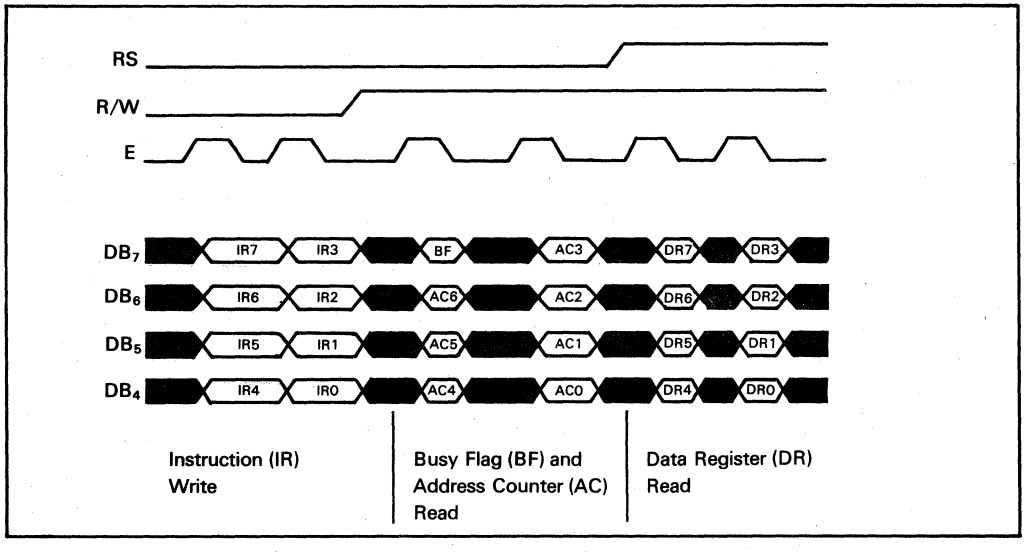

Figure 11 4-Bits Data Transfer Example

Instructions

Only two HD66780 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD66780 internal operation to various types of MPU's which operate at different speeds or to allow interface to peripheral control IC's. HD66780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W), and data bus signals (DB_0–DB_7), and are here called instructions. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate HD66780 functions such as display format, data length, etc
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of HD66780 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 7.

During internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is on 0 before sending an instruction from the MPU.

Note: Make sure the HD66780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD66780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction execution time. See table 5 for a list of each instruction's execution time.

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Table 5 Instructions

Instruction	Code RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (Max) (fcp or fosc 250 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read	40 μs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C), and blink of cursor position character (B)	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N) and character font (F)	40 μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	ADD							Set DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents	0 μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	46 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	46 μs

Notes: 1.

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
S/C = 1: Display shift
S/C = 0: Cursor move
R/L = 1: Shift to the right
R/L = 0: Shift to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
F = 1: 5×10 dots, F = 0: 5×7 dots

BF = 1: Internally operating
BF = 0: Can accept instruction
DD RAM: Display data RAM
CG RAM: Character generator RAM
A_{CG}: CG RAM address
A_{DD} :DD RAM address Corresponds to cursor address
AC : Address counter used for both DD and CG RAM

2. * No effect (Don't care)
3. Execution time changes when freguency changes.
   Example: When fcp or fosc is 270 kHz:

$$40\ \mu s \times \frac{250}{270} = 37\ \mu s$$

Clear Display

Clear display (figure 12) writes space code 20 (hexadecimal)(character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it is shifted. In other words, the display disappears and the cursor or blink goes to the left edge of the display (the first line if 2 lines are displayed). Sets I/D = 1 (increment mode) of entry mode. S of entry mode does not change.

Return Home

Return home (figure 13) sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left of the display (the first line if 2 lines are displayed).

Entry Mode Set

I/D: I/D (figure 14) increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM. Writing into or reading out of the CG RAM does not shift the display. When S = 0, the display does not shift.

Display On/Off Control

D: The display is on when D = 1 and off when D = 0 (figure 15). When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc does not

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	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Figure 12 Clear Display Instruction

	RS	R/W	DB_7					DB_0	
Code	0	0	0	0	0	0	0	1	*

* Don't care

Figure 13 Return Home Instruction

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Figure 14 Entry Mode Set Instruction

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	1	D	C	B

Figure 15 Display On/Off Control Instruction

change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7-dot is selected and 5 dots in the 11th line when the 5× 10-dot character font is selected (figure 16).

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms intervals when fcp or fosc = 250 kHz (figure 15). The cursor and the blink can be set to display simultaneously. (The blink time changes according to the reciprocal of fcp or fosc. For example, 409.6 × $\frac{250}{270}$ = 379.2 ms when fcp = 270 kHz.)

Cursor or Display Shift

Cursor or display shift (figure 17) shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

Table 6 shows how S/C and R/L control shifting.

Address counter (AC) contents do not change if the only action performed is shift display.

Function Set

DL: DL (figure 18) sets interface data length. Data is sent or received in 8-bit length (DB_7-DB_0) when DL = 1 and in 4-bit lengths (DB_7-

Table 6 Cursor or Display Shift Control

S/C	R/L	Function
0	0	Shifts the cursor position to the left (AC is decremented by one)
0	1	Shifts the cursor position to the right (AC is incremented by one)
1	0	Shifts the entire display to the left. The cursor follows the display shift
1	1	Shifts the entire display to the right. The cursor follows the display shift

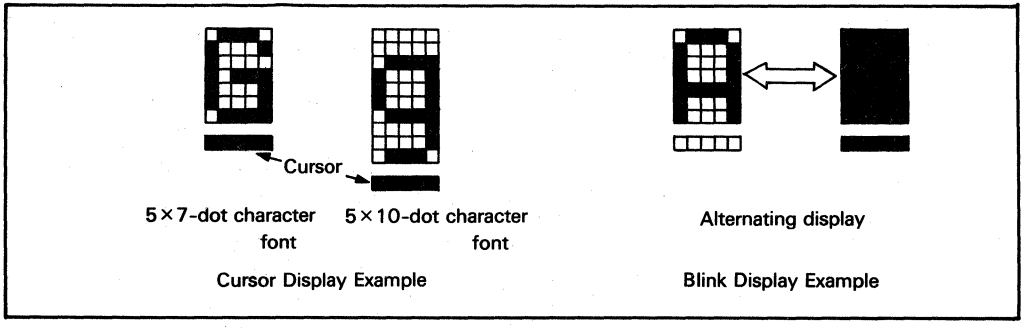

Figure 16 Cursor and Blink Display

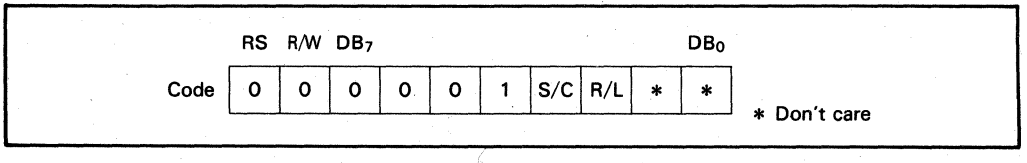

Figure 17 Corsor or Display Shift Instruction

DB_4) when DL = 0.
When the 4-bit length is selected, data must be sent or received twice.

N: N sets number of display lines.

F: F sets character font. See table 7.

Note: Perform the function set at the head of the program before executing any instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address (figure 19) sets the CG RAM address binary AAAAAA into the address counter. Data is then written or read from the MPU for the CG RAM.

Set DD RAM Address

Set DD RAM address (figure 20) sets the DD RAM address binary AAAAAAA into the address counter. Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA is 00-4F (hexadecimal), when N = 1 (2-line display), AAAAAAA is 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

Read Busy Flag and Address

Read busy flag and address (figure 21) reads the busy flag (BF) that indicates the system is now internally operating on a previously

Table 7 Function Set N and F

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5×7 dots	1/8	
0	1	1	5×10 dots	1/11	
1	*	2	5×7 dots	1/16	Cannot display 2 lines with 5×10-dot character font

Note: * Don't care

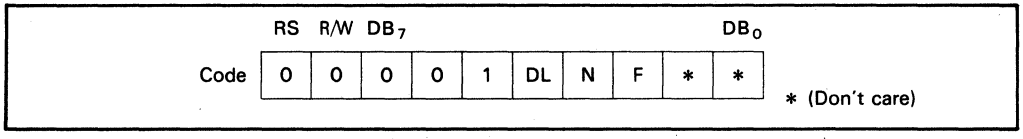

Figure 18 Function Set Instruction

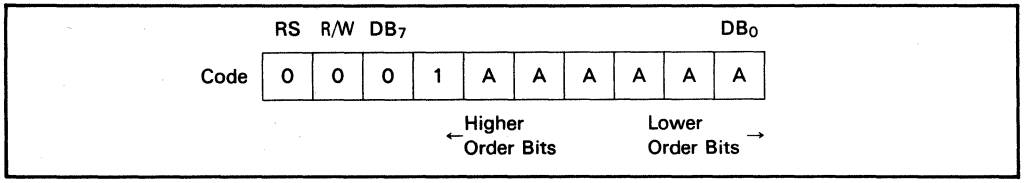

Figure 19 Set CG RAM Address Instruction

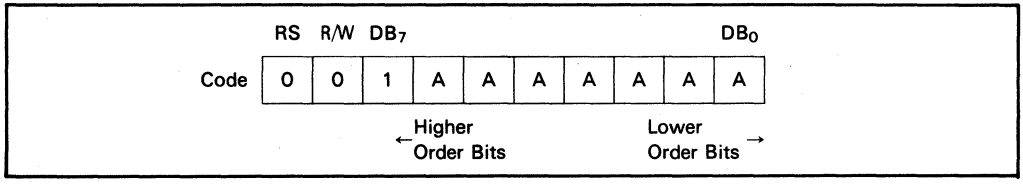

Figure 20 Set DD RAM Address Instruction

received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to 0. Check the BF status before the next write operation (figure 22).

At the same time, the value of the address counter expressed in binary (AAAAAAA) is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in set CG RAM address and set DD RAM address.

Write Data to CG or DD RAM

Write data to CG or DD RAM (figure 23) writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After writing, the LCD-IIA automatically increments or decrements the address by 1, according to entry mode.

Read Data from CG or DD RAM

Read data from CG or DD RAM (figure 24) reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you do not the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift

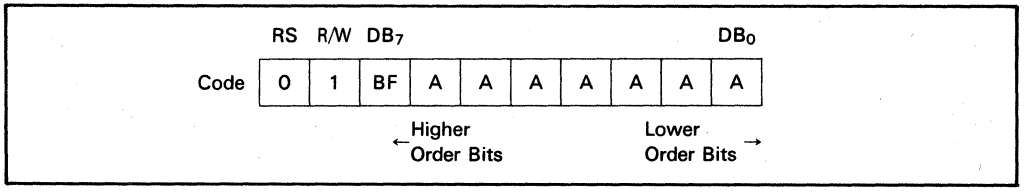

Figure 21 Read Busy Flag and Address Instruction

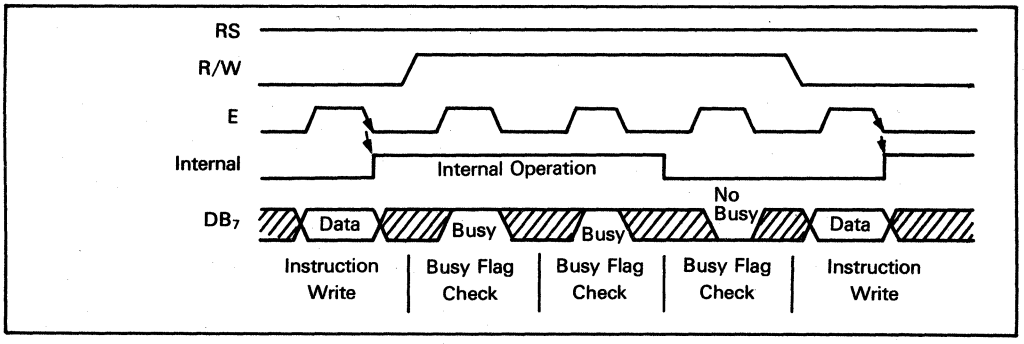

Figure 22 Example of Busy Flag Check Timing Sequence

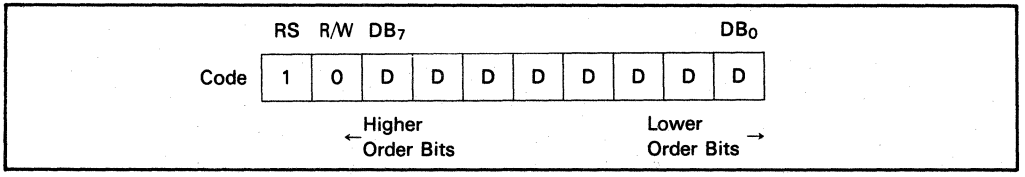

Figure 23 Write Data to CG or DD RAM Instruction

instruction (when reading out of DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display is not shifted no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out, execute the read instruction from the second time the read instruction is sent.

How to Use the HD66780

Interface to 8-Bit MPU

When Connecting to 8-Bit MPU Through PIA: Figure 25 is an example of using a PIA or I/O port (for a microcontroller) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively.

Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

Connecting Directly to the 8-Bit MPU Bus: Figure 26 shows the LCD-IIA connected directly to an HD6800.

Example of Interfacing to the HD6805: Figure 27 shows the LCD-IIA connected directly to an HD6805.

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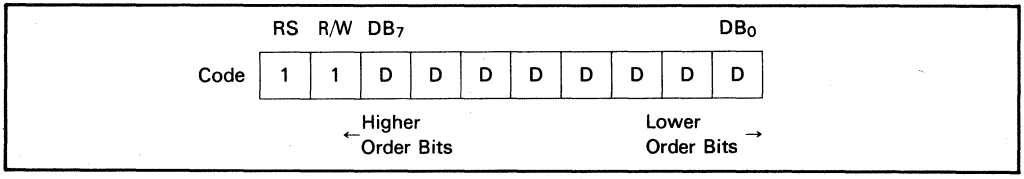


Figure 24 Read Data from CG or DD RAM Instruction

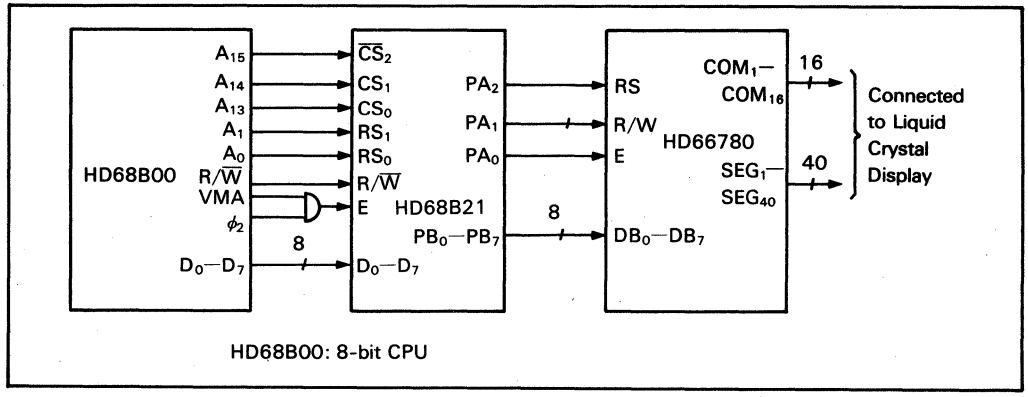


Figure 25 Example of Interface to HD68B00 using PIA (HD68B21)

Example of Interfacing to the HD6301: Figure 28 shows the LCD-IIA connected directly to an HD6301.

Interface to 4-Bit MPU

The HD66780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port, If the I/O port has enough bits, data can be transferred in 8-bit length, but if there aren't enough bits, the transfer is made in two operations of 4 bits each (designating the interface data length as 4 bits). In the latter case, the timing sequence becomes somewhat complex. (see figure 29).

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

Figure 30 shows an example of an interface to the 400 series.

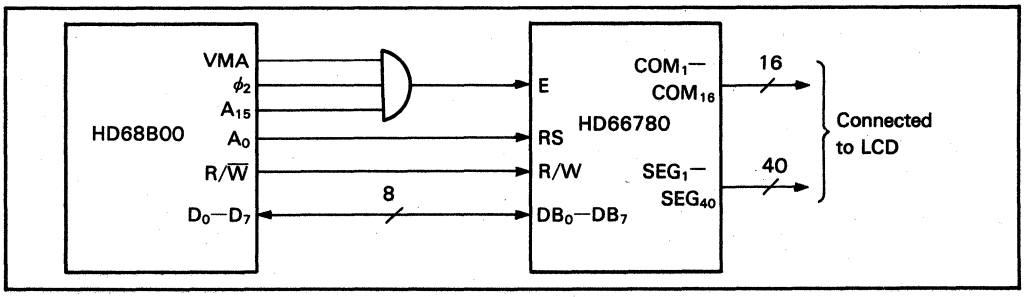


Figure 26 Direct Connection to HD68B00

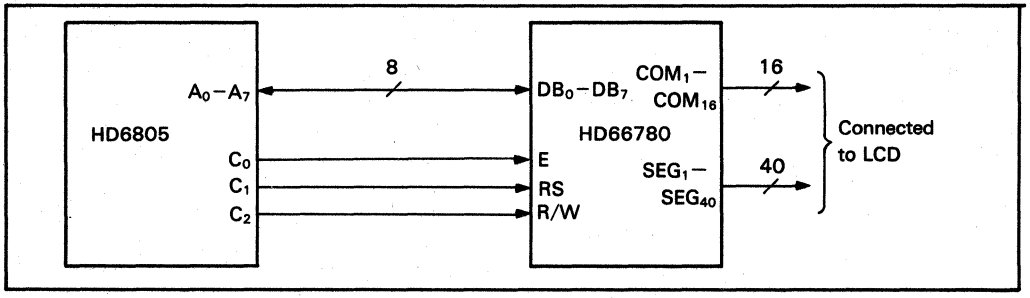


Figure 27 Direct Connection to HD6805

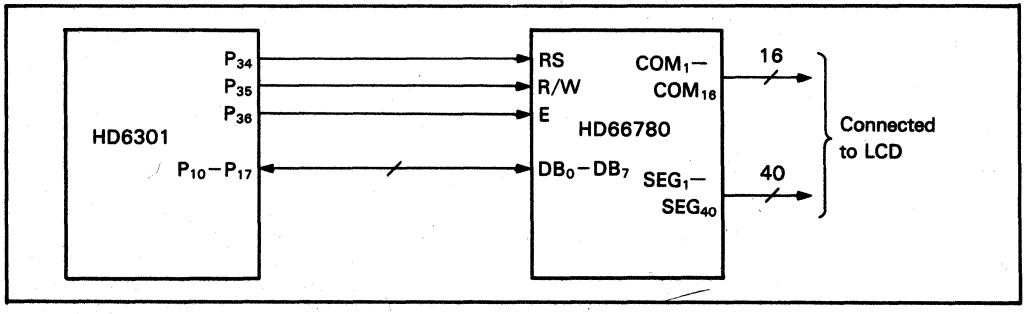


Figure 28 Direct Connection to HD6301

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD66780 can perform 2 types of display, using 5 × 7 dots or 5 × 10 dots for the character font, with a cursor on each.

Up to 2 lines can be displayed with 5 × 7 dots and 1 line with 5 × 10 dots.

Therefore, three types of common signals are available (table 8).

Number of lines and font types can be selected by program (see table 5).

Connection to HD66780 and Liquid Crystal Display: Figure 31 shows connection examples. Since 5 SEG signal lines can display one digit, one HD66780 can display up to 8 digits

Table 8 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 × 7 dots + Cursor	16	1/16

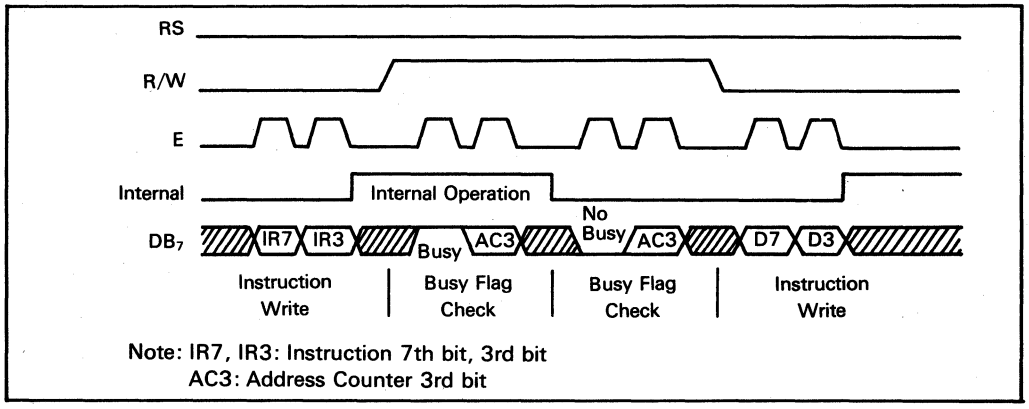


Figure 29 An Example of 4-Bit Data Transfer Timing Sequence

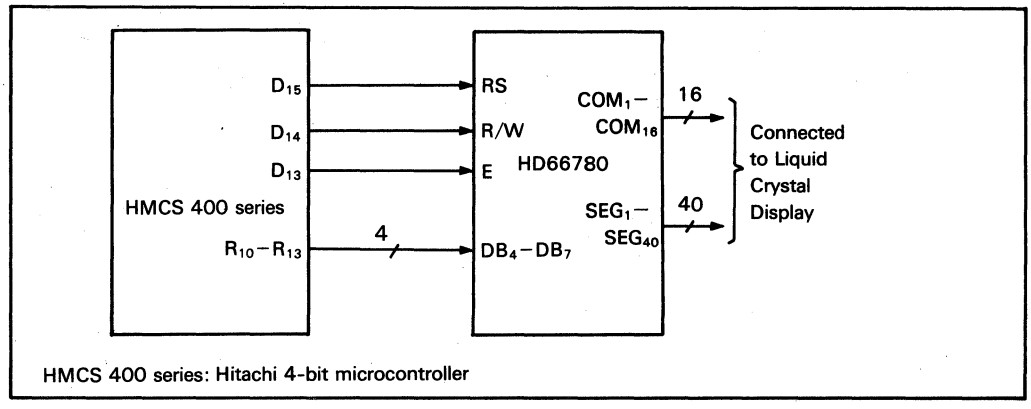


Figure 30 Example of Interface to the 400 Series

for a 1-line display and 16 digits for a 2-line display.

In figure 31 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals (figure 32).

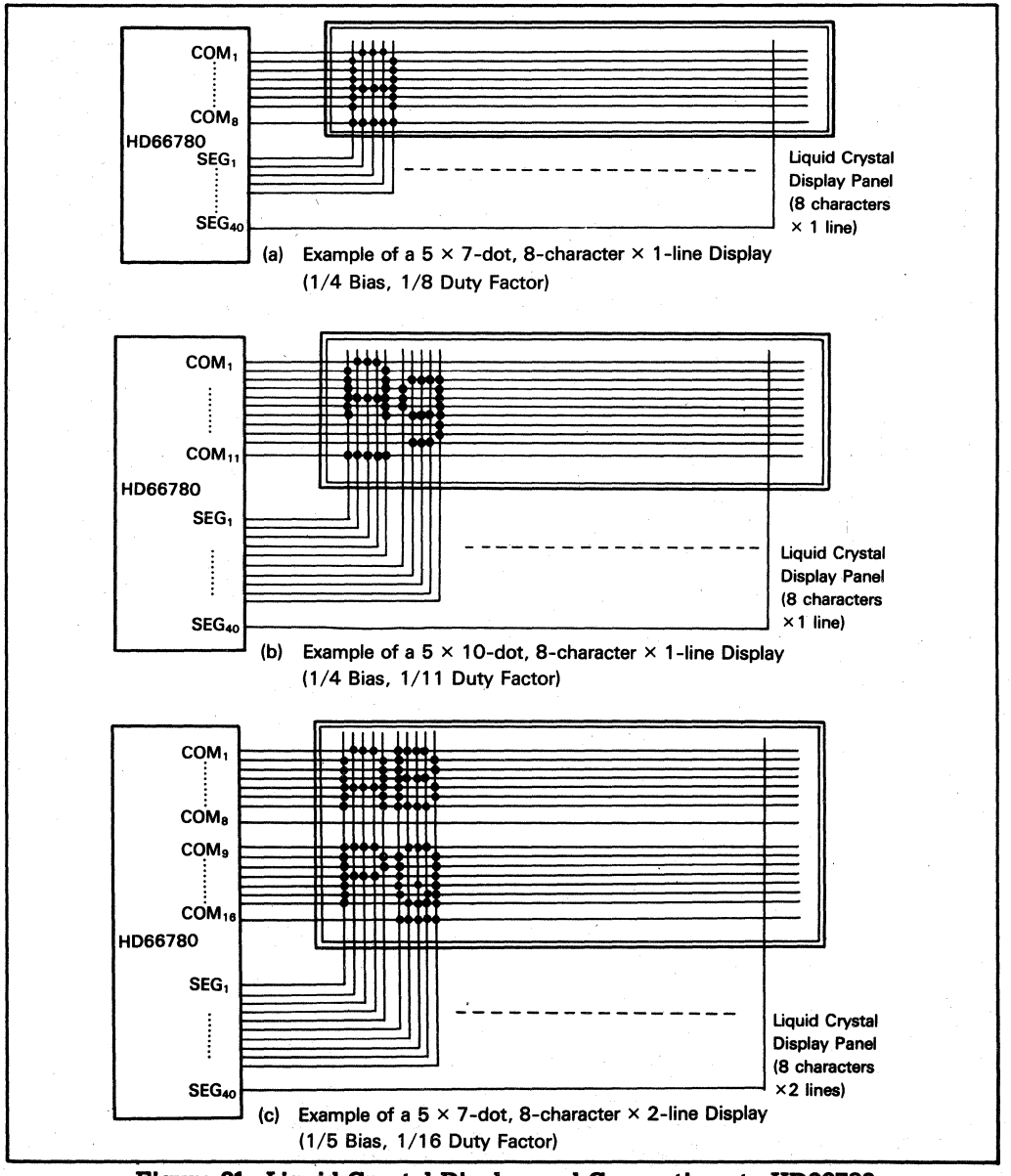


Figure 31 Liquid Crystal Display and Connections to HD66780

Connection for Changed Matrix Layout: In the preceding examples, the number of lines was matched to the number of scanning lines. The display types in figure 33 are possible by changing the matrix layout in the liquid crystal display panel.

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) address for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in figure 31.

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD66780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factors. Table 9 shows the relation.

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in figure 34.

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

Figure 35 shows examples of liquid crystal display frame frequency when the oscillation frequency is 250 kHz (1 clock = 4 μs).

Connection with Driver LSI HD44100H or HD66100F

You can increase the number of display characters by externally connecting liquid crystal display driver LSI's HD44100H or HD66100F to the HD66780.

When connected to the HD66780, the HD44100H or HD66100F is used as a segment signal driver. The HD44100H and the HD66100F can be connected to the HD66780 directly since they supply CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figures 36 and 37 show connection examples.

Note: Connection of voltage supply terminals V_1 through V_6 for the liquid crystal display drive is complicated.

4

Table 9 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor	Bias	Power Supply V_1	V_2	V_3	V_4	V_5
1/8,1/11	1/4	V_{CC} - (1/4)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (3/4)V_{LCD}	V_{CC} - V_{LCD}
1/16	1/5	V_{CC} - (1/5)V_{LCD}	V_{CC} - (2/5)V_{LCD}	V_{CC} - (3/5)V_{LCD}	V_{CC} - (4/5)V_{LCD}	V_{CC} - V_{LCD}

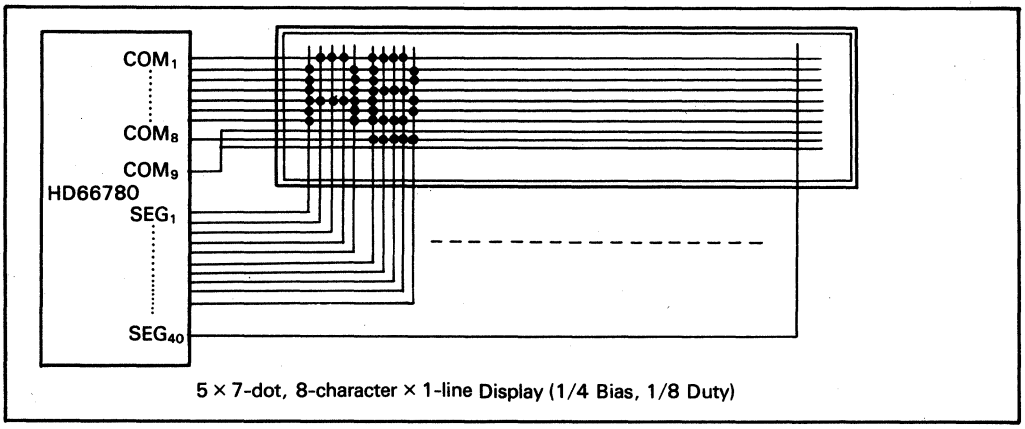


Figure 32 Using COM_9 to Avoid Cross-Talk on Unneeded Scanning Line

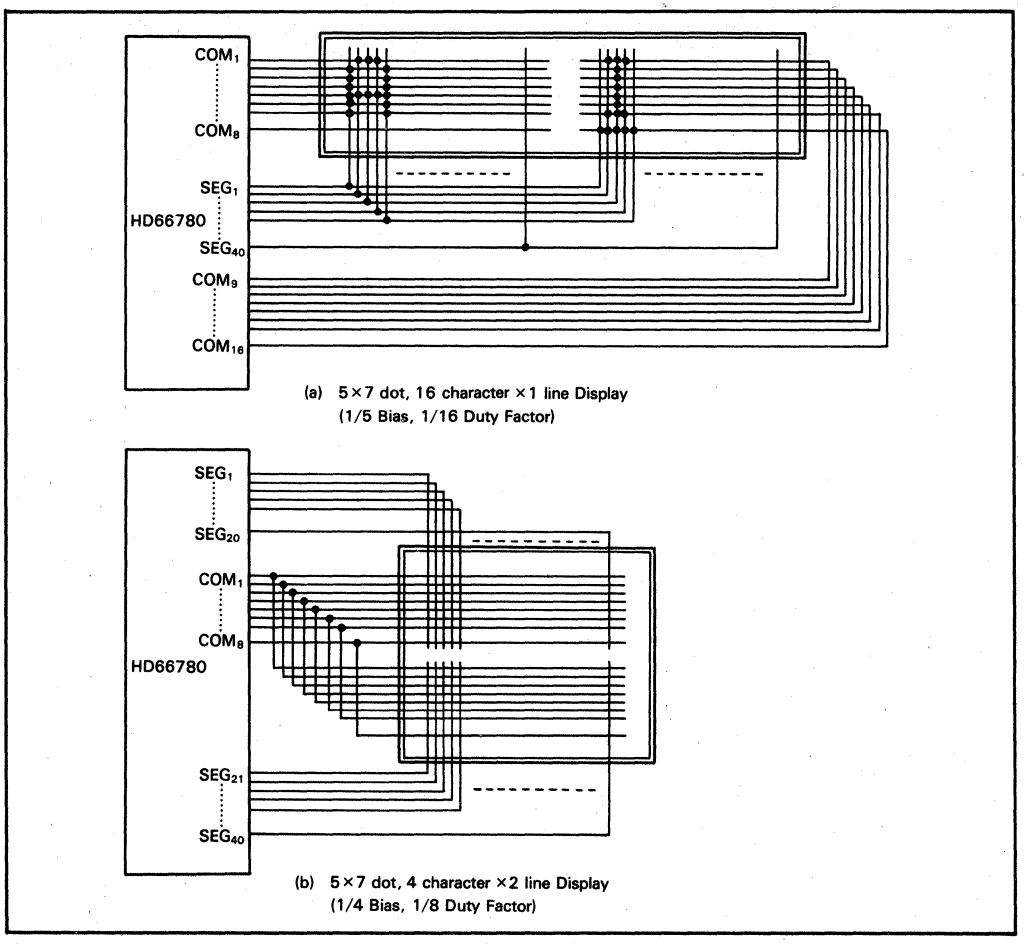


Figure 33 Changed Matrix Layout Displays

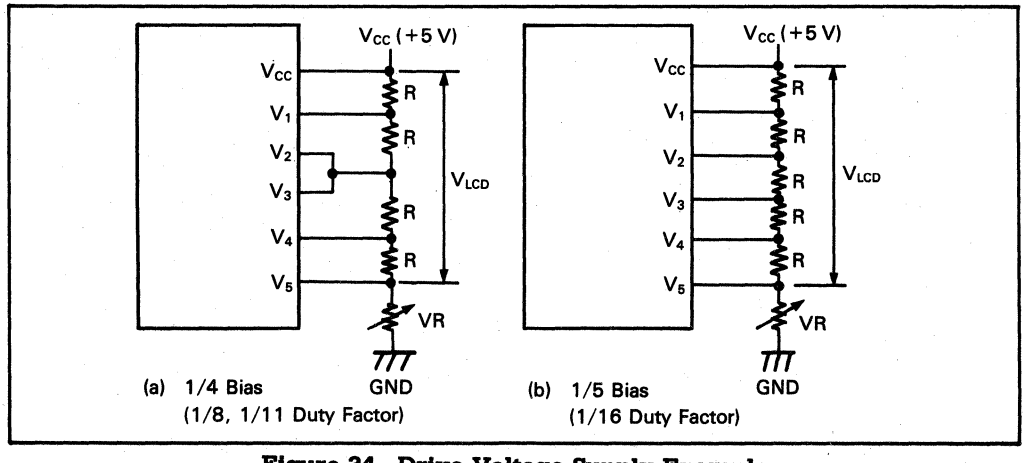
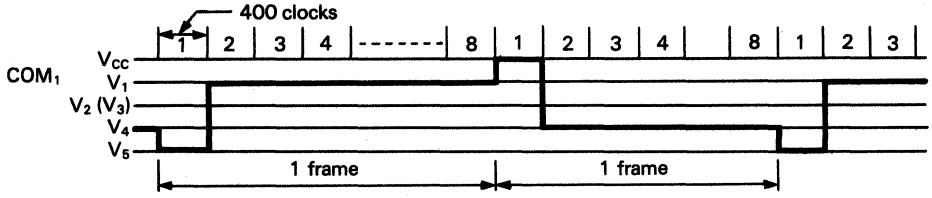


Figure 34 Drive Voltage Supply Example

Up to 9 HD44100Hs can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to 4 for a 2-line display (duty factor 1/16). (For the HD66100F, 5 and 2 units respectively.) RAM size limits the HD66780 to a maximum of 80 character diaplay digits. The connection method in figures 36 and 37 remains unchanged for both 1-line and 2-line display and both 5 × 7-and 5 × 10-dot character fonts.

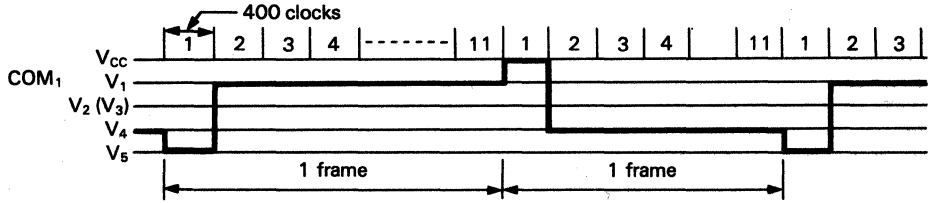
(1) 1/8 Duty Factor



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

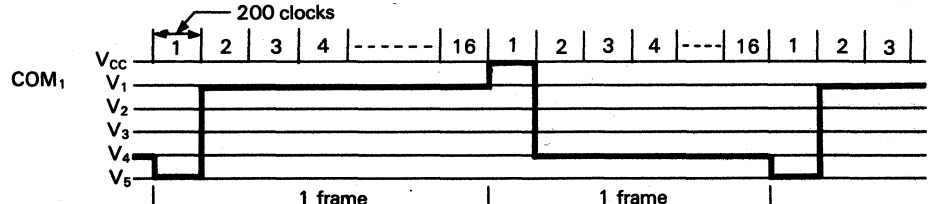
(2) 1/11 Duty Factor



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty Factor



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

Figure 35 Liquid Crystal Display Waveforms (at f_{OSC} = 250kHz)

4

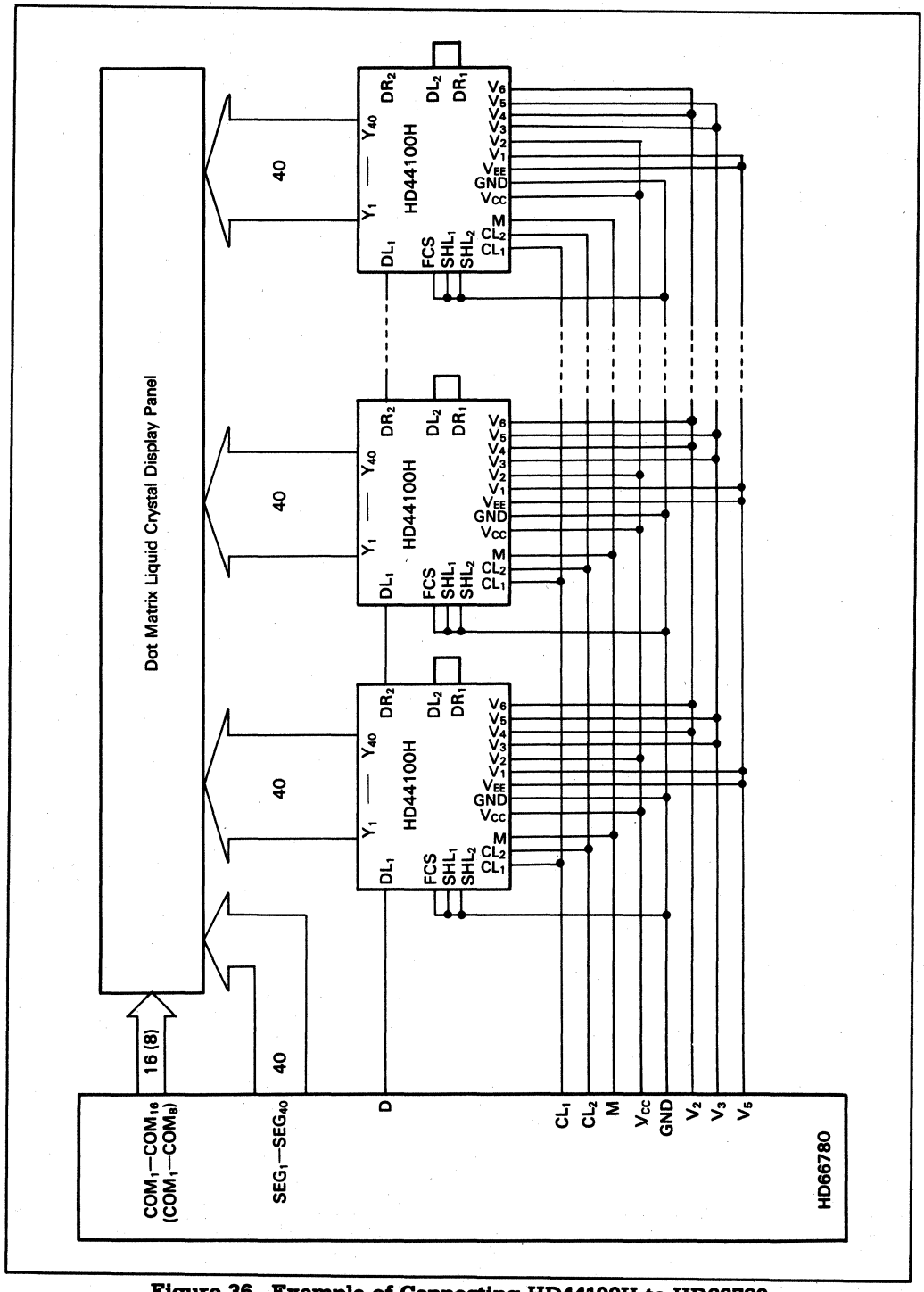


Figure 36 Example of Connecting HD44100H to HD66780

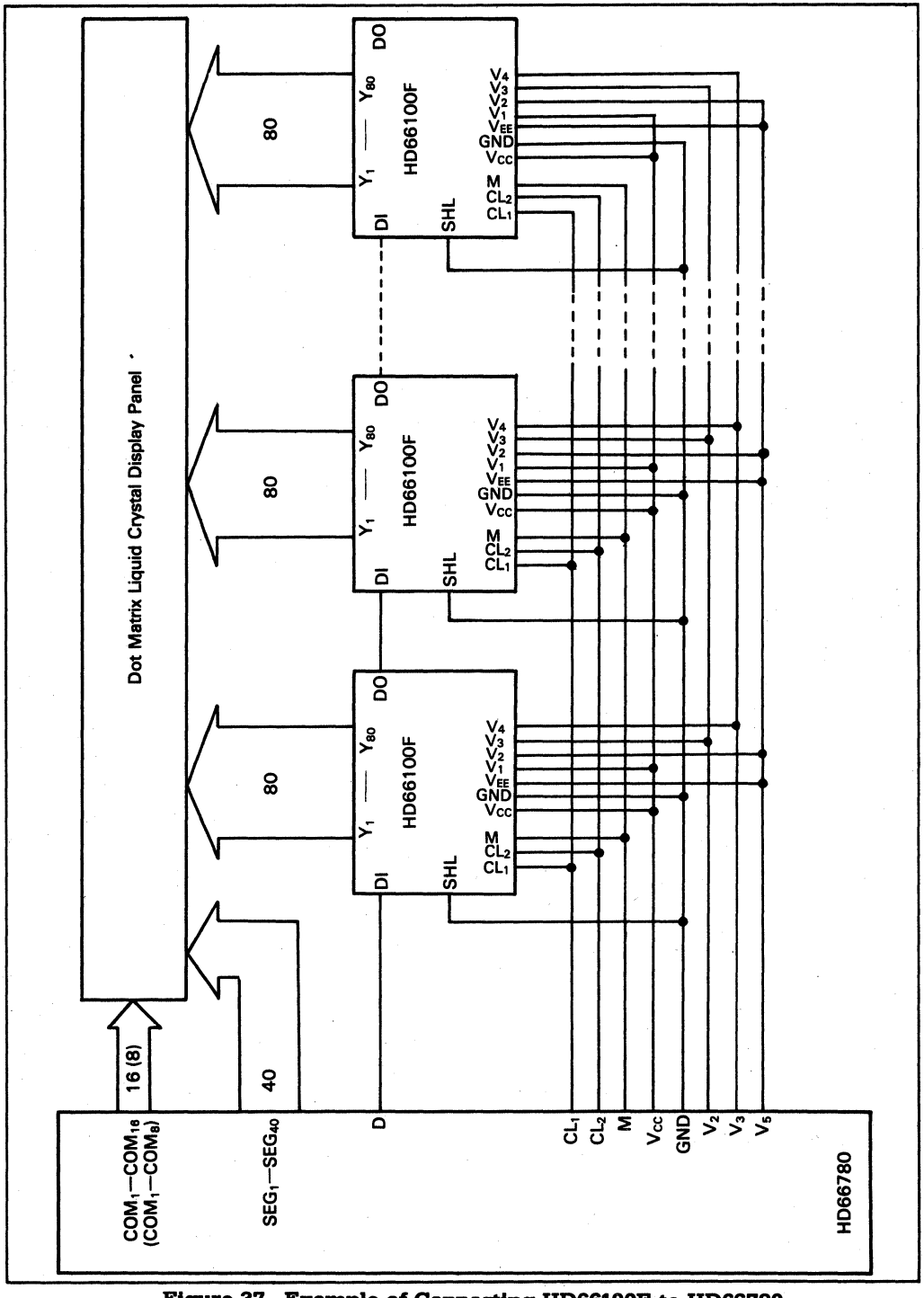


Figure 37 Example of Connecting HD66100F to HD66780

Instruction and Display Correspondence
8-bit Operation, 8-digit × 1-line Display (Using Internal Reset): Table 10 shows an example of an 8-bit × 1-line display in 8-bit operation. The HD66780 functions must be set by the function set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

4-bit Operation, 8-digit × 1-line Display (Using Internal Reset): The program must set functions prior to 4-bit operation. Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the LCD-IIA attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB_0-DB_3, a rewrite is then required. However, since one operation is completed in two 4-bit accesses, a rewrite is needed to set the functions (see table 11 step 3).

Thus, DB_4-DB_7 of the function set is written twice.

8-bit Operation, 8-digit × 2-line Display: For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set after the eighth character is completed (see table 12). Note that the first and second lines of the display are shifted.

In the example, the display is shifted when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD66780 must be initialized by instruction. (See "Initializing by Instruction")

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the LCD-IIA must be initialized by instruction.
When interface is 8 bits long, use the initialization procedure in figure 38.

When interface is 4 bits long, use the initialization procedure in figure 39.

Table 10 8-Bit Operation, 8-Character × 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 • • • DB0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display and one of the three character fonts. (Number of display lines and character font cannot be changed after this.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is on space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI	Writes space.
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO	Shifts only the cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (address 0).

4

Table 11 4-Bit Operation, 8-Character × 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 · · · DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets to 4-bit operation and selects 1-line display and one of the three character fonts. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character font cannot be changed after this.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.

After this, control is the same as 8-bit operation.

Table 12 8-Bit Operation, 8-Character × 2-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB$_7$ · · · DB$_0$ 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and one of the three character fonts.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor may be positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the left. The first and second lines' shift is operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).

4

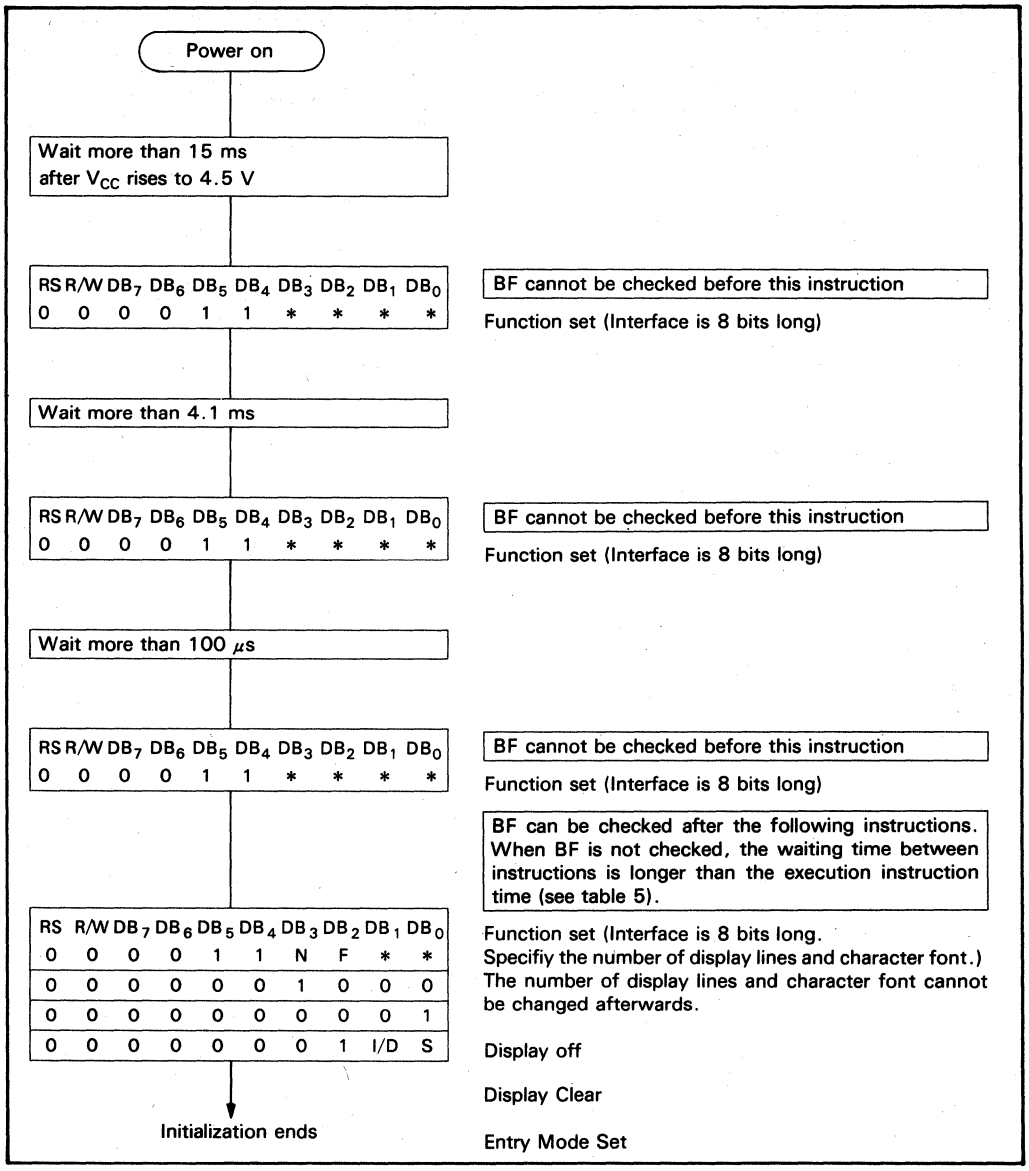


Figure 38 Initialization by Instruction, Eight-Bit Interface

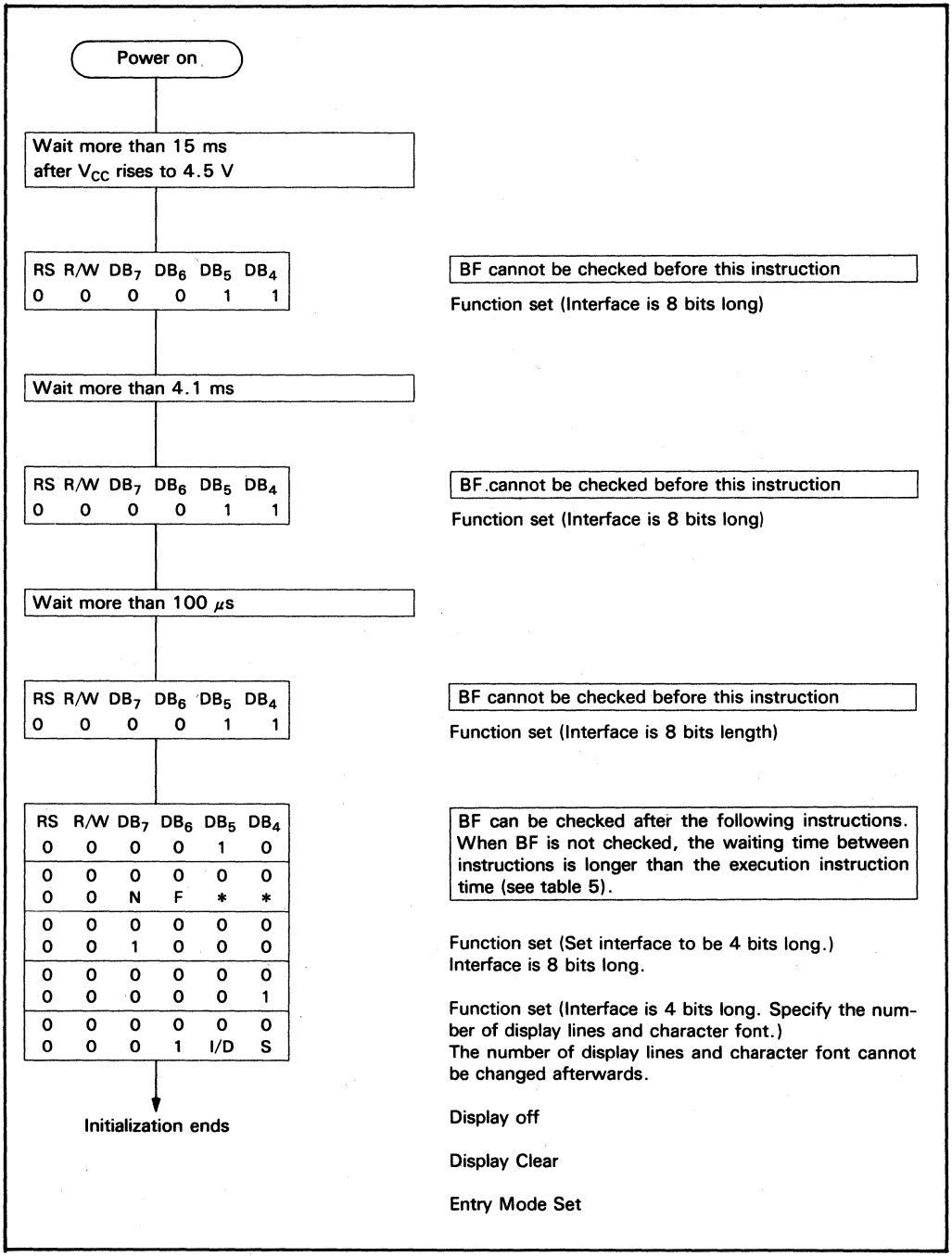


Figure 39 Initialization by Instruction, Four-Bit Interface

4

LCD-II and LCD-IIA

Table 13 shows the differences between the LCD-II and LCA-IIA.

There are two types of multiplex waveforms for LCD driving: A and B. A type, shown in figure 40, is used for alternation in 1 frame, and B type, shown in figure 41, for alternation in 2 frames. B type has better display quality in highly multiplexed drive.

Table 13 Functions Comparison between LCD-II and LCD-IIA

Item		LCD-II (HD44780)	LCD-IIA (HD66780)	Note
Display RAM (Maximum number of display characters)		80 bytes (80 characters)	Same as LCD-II	
* Character generator ROM (Kinds of characters)		7200 bits 192 characters 5×7:160 characters 5×10: 32 characters	12000 bits 240 characters 5×10: 240 characters	
Character generator RAM (Number of characters)		64 bytes (8 characters)	Same as LCD-II	
LCD driving terminals (Maximum number of display characters/ unit)		16 COMs 40 SEGs (16 characters)	Same as LCD-II	
Character font (with a cursor)		5×8 dots 5×11 dots	Same as LCD-II	
Multiplexing duty ratio		1/8, 1/11, 1/16		
* LCD driving voltage	1/4 bias	3.0 to 11 (v)	3.0 to V_{CC} (V)	V_{CC} to V_5 (V)
	1/5 bias	4.6 to 11 (v)	3.0 to V_{CC} (v)	
* LCD driving waveform		A waveform	B waveform	See figures 40,41
* Bus timing		1, 1.5 MHz	2 MHz	
Instruction codes		11 instructions	Same as LCD-II	
Power-on reset circuit		Yes	Same as LCD-II	
Oscillator (Frequency)		Ceramic filter, Rf, external clock (250 kHz)	Same as LCD-II	
Interface		HD44100H	HD44100H or HD66100F	
Package		FP-80, FP-80A	Same as LCD-II	
Pin arrangement		Refer to p.98	Same as LCD-II	

Note: * indicates the modified items on LCD-IIA.

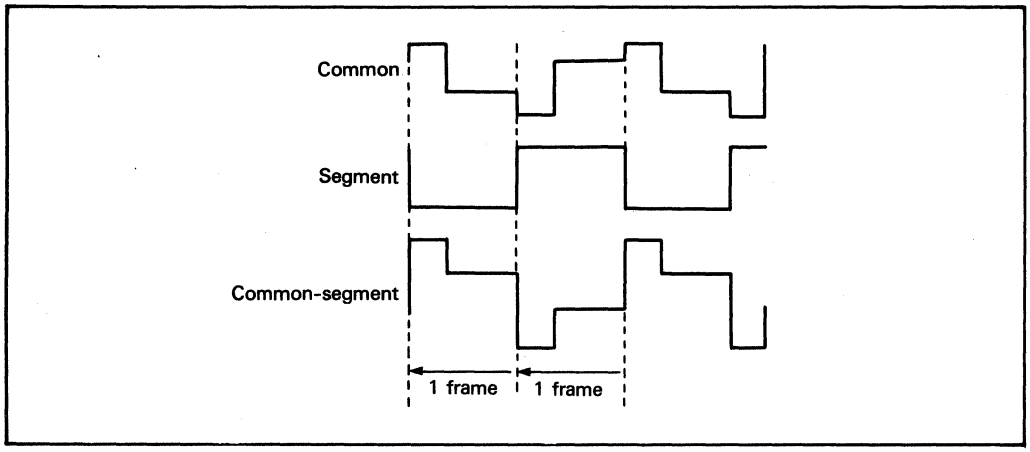


Figure 40 A-Type Waveforms (1/3 Duty Factor, 1/3 Bias)

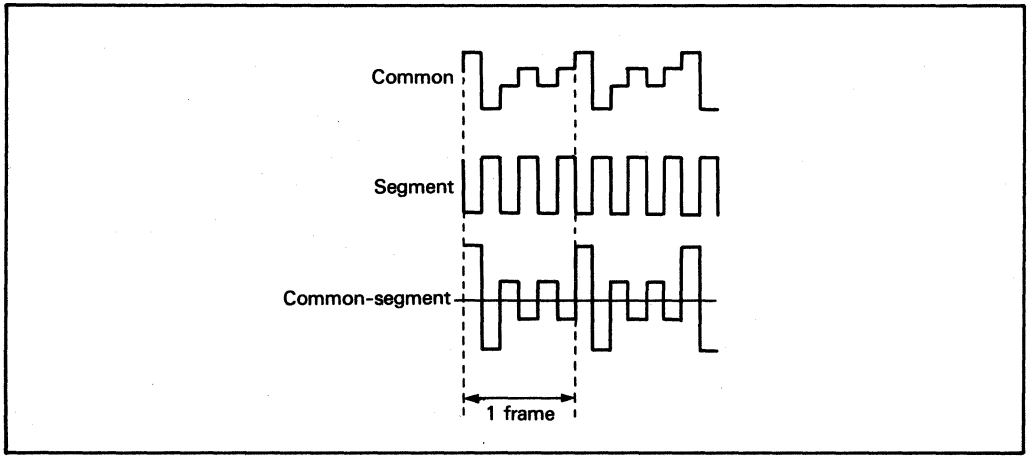


Figure 41 B-Type Waveforms (1/3 Duty Factor, 1/3 Bias)

4

Character Pattern Development Procedure

The numbers in the above figure correspond to the following operations:

1. Determime the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program character patterns in the EPROM.
4. Send the EPROM to Hitachi.
5. Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.
6. If there is no problem in the character pattern listing, Hitachi creates trial LSIs and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, mass production of LSI is started.

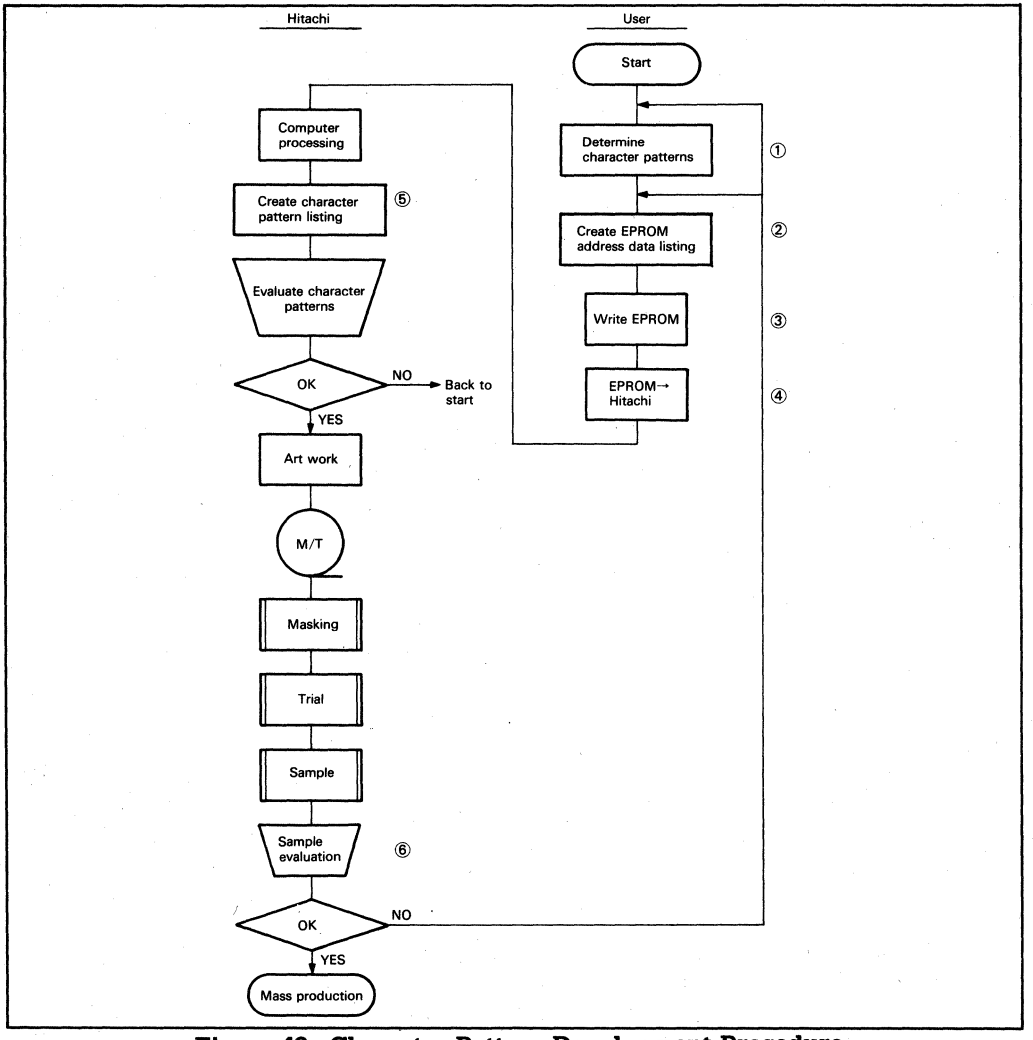


Figure 42 Character Pattern Development Procedure

Character Pattern Program Method

The relationship between the EPROM address and character pattern is shown in table 14.

In order to evaluate ROM patterns, we recommend to use our LCD controller HD61830. We also supply LCD control board (CB1026R).

Table 14 Character Data in EPROM

EPROM Address												Data							
(right sile up)												(LSB)							
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
								0	0	0	0	0	0	0	0	0			
								0	0	0	1	0	0	0	0	0			
								0	0	1	0	0	1	1	0	1			
								0	0	1	1	1	0	0	1	1			
								0	1	0	0	1	0	0	0	1			
1	1	1	1	0	0	0	1	0	1	0	1	1	0	0	0	1			
								0	1	1	0	0	1	1	1	1			
								0	1	1	1	0	0	0	0	1			
								1	0	0	0	0	0	0	0	1			
								1	0	0	1	0	0	0	0	1			
								1	0	1	0	0	0	0	0	0			
								1	0	1	1								
								1	1	0	0								
								1	1	0	1								
								1	1	1	0								
								1	1	1	1								

Character code — Line code

Notes: 1. EPROM Data O_5-O_7 are invalid
2. Data "0" must be programed at 11th line (cursor position).
3. Data at 12-16th line are invalid
4. Data at O_0 locate at the left side of screen. (The relation between the bit number and position is reversed, compared with HD44780.)

4

Handling Unused Character Patterns

1. EPROM data outside the character pattern area

   Ignored by the character generator ROM for display operation so it can be 0 or 1.

2. EPROM data in CG RAM area

   Ignored by the character generator ROM for display operation so it can be 0 or 1.

3. EPROM data used when the user does not use any LCD-II character pattern

   Handled in one of the two ways explained below. Select one of two ways according to the user application.

   a. When unused character patterns are not programed

      If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because the EPROM is filled with 1 when the EPROM is erased.)

   b. Program 0 for unused character patterns

      Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (It is equivalent to space.)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature	Topr	-20 to +75	°C
Storage Temperature	Tstg	-55 to +125	°C

Notes: 1. If LSIs are used above the absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to V1 to V5. The relation: $V_{CC} \geqq V1 \geqq V3 \geqq V4 \geqq V5 \geqq GND$ must be maintained.
(high to low)

Electrical Characteristics

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, Ta = -20 to +75 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage (1)	V_{IH1}	2.3	–	V_{CC}	V		(2)
Input Low Voltage (1)	V_{IL1}	–	–	0.6	V		(2)
Input High Voltage (2)	V_{IH2}	V_{CC} - 1.0	–	V_{CC}	V		(12)
Input Low Voltage (2)	V_{IL2}	–	–	1.0	V		(12)
Output High Voltage (1)(TTL)	V_{OH1}	2.4	–	–	V	$-I_{OH}$ = 0.205 mA	(3)
Output Low Voltage (1)(TTL)	V_{OL1}	–	–	0.4	V	I_{OL} = 1.6 mA	(3)
Output High Voltage (2)(CMOS)	V_{OH2}	0.9V_{CC}	–	–	V	$-I_{OH}$ = 0.04 mA	(4)
Output Low Voltage (2)(CMOS)	V_{OL2}	–	–	0.1V_{CC}	V	I_{OL} = 0.04 mA	(4)
Driver On Resistance (COM)	R_{COM}	–	–	20	kΩ	±Id = 0.05 mA to each COM Pin	(10)
Driver On Resistance (SEG)	R_{SEG}	–	–	30	kΩ	±Id = 0.05 mA to each SEG Pin	(10)
Input Leakage Current	I_{IL}	-1	–	1	μA	V_{in} = 0 to V_{CC}	(5)
Pull up MOS Current	$-I_P$	50	125	250	μA	V_{CC} = 5 V	
Power Supply Current (1)	I_{CC1}	–	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, f_{OSC} = 250 kHz	(6)
Power Supply Current (2)	I_{CC2}	–	0.35	0.6	mA	Rf oscillation, External clock operation V_{CC} = 5 V, f_{OSC} = fcp = 270 kHz	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}	125	250	350	kHz		(7)
External Clock Duty	Duty	45	50	55	%		(7)
External Clock Rise Time	t_{rcp}	–	–	0.2	μs		(7)
External Clock Fall Time	t_{fcp}	–	–	0.2	μs		(7)
Internal Clock Operation (Rf Oscillation)							
Clock Oscillation Frequency	f_{OSC}	190	270	350	kHz	Rf = 82 kΩ±2%	(8)
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{OSC}	245	250	255	kHz	Ceramic filter	(9)
LCD Voltage	V_{LCD1}	3.0	–	V_{CC}	V	V_{CC} - V_5 1/5 bias	(13)
	V_{LCD2}	3.0	–	V_{CC}	V	1/4 bias	(13)

Notes:
1. Figure 43 shows the I/O pin configurations except for liquid crystal display output.
2. Input pins and I/O pins. Excludes OSC_1 pin.
3. I/O pins.
4. Output pins.
5. Current flowing through pull-up MOS's and output drive MOS's is excluded.
6. Input/output current is excluded. When input is at an intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.
7. External clock operation as shown in figure 44.
8. Internal oscillator operation using oscillation resistor Rf (figure 45).
9. Internal oscillator operation using a ceramic filter (figure 46).
10. R_{COM} applies to the resistance between power supply pin (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).
    R_{SEG} applies to the resistance between power supply pin (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{40}).

4

11. Relation between operation frequency and current consumption is shown in figure 47. (V_{CC} = 5 V)
12. Applied to OSC_1 pin.
13. When each COM and SEG output voltage is within ±0.15 V of LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

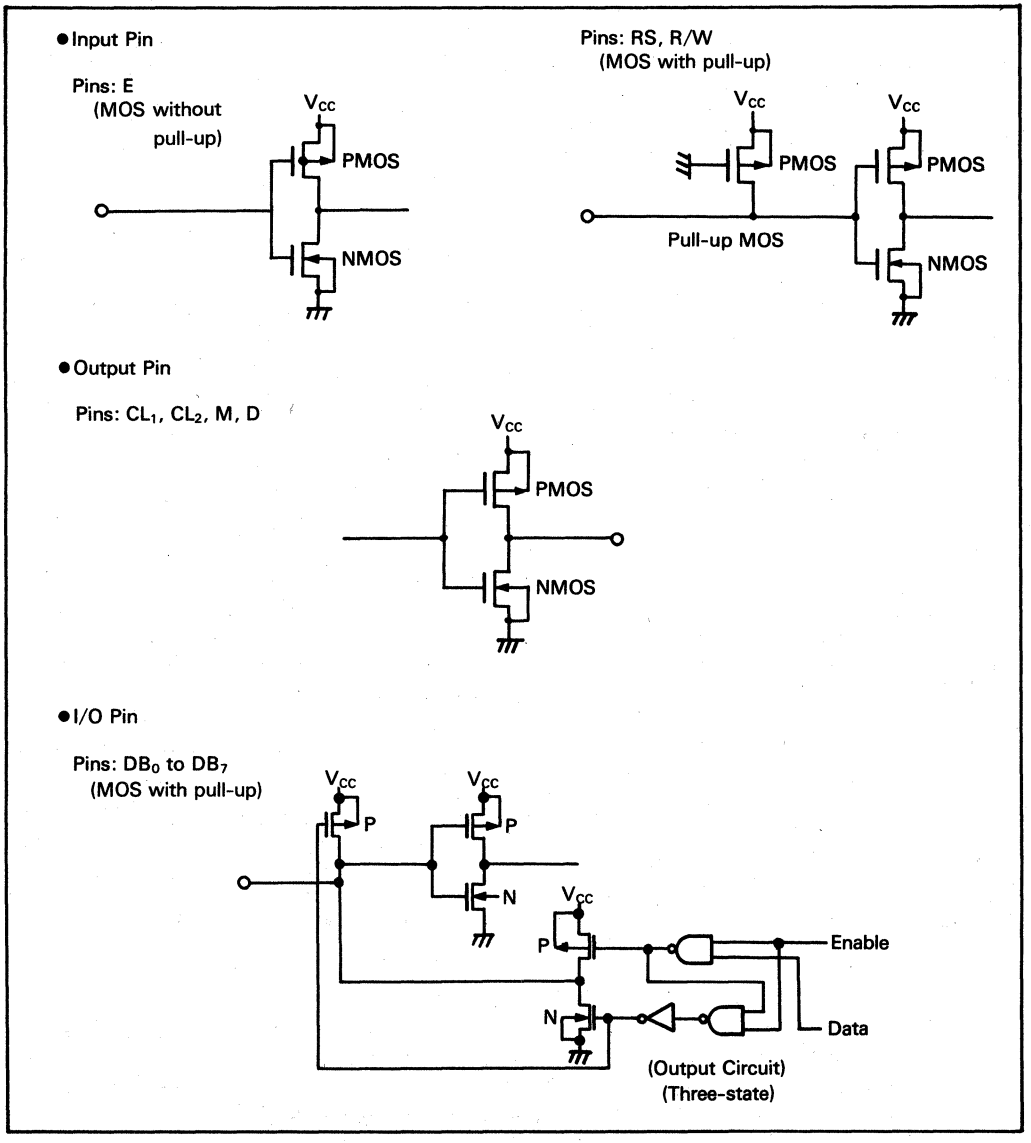


Figure 43 Pin Configuration

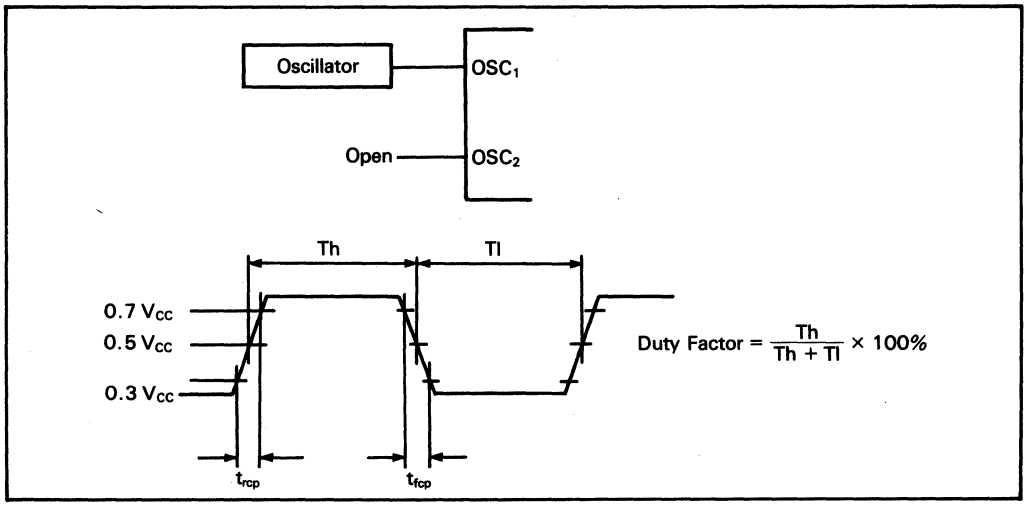


Figure 44 External Clock

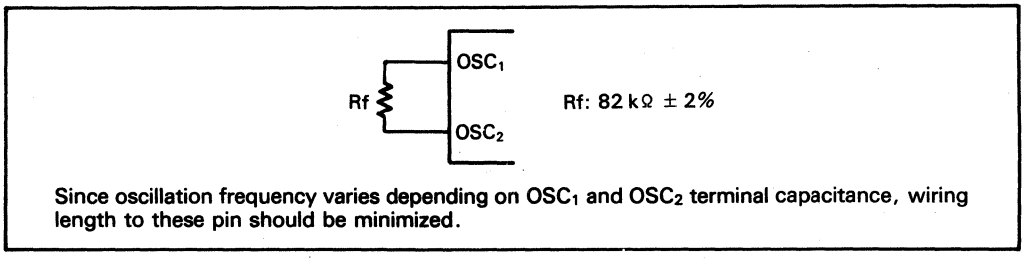


Figure 45 Internal Oscillator, Resistor

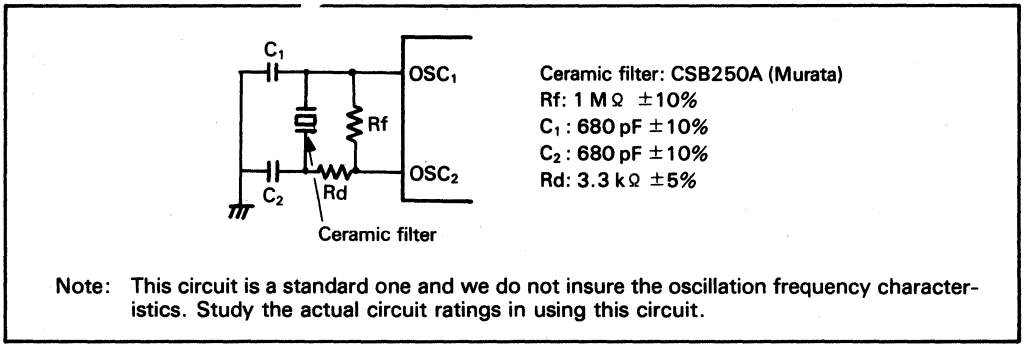


Figure 46 Internal Oscillator, Ceramic Filter

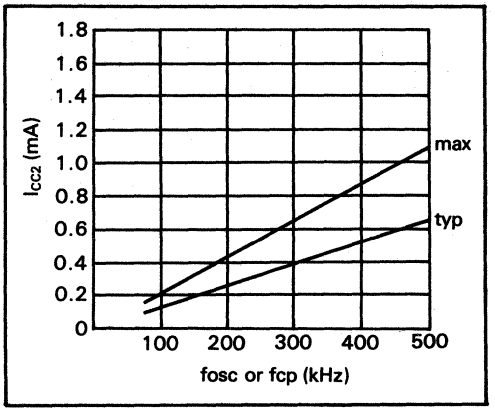
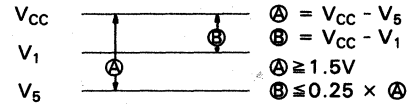


Figure 47 Frequency vs Current



Note: The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level (figure 48). The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

Figure 48 V_1, V_5 Voltages

Bus Timing Characteristics (V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Write Operation (Writing Data from MPU to HD66780)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 52
Enable Pulse Width (High level)	PW_{EH}	220	–	ns	Fig. 52
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 52
Address Set-up Time (RS, R/W–E)	t_{AS}	40	–	ns	Fig. 52
Address Hold Time	t_{AH}	10	–	ns	Fig. 52
Data Set-up Time	t_{DSW}	60	–	ns	Fig. 52
Data Hold Time	t_H	10	–	ns	Fig. 52

Read Operation (Reading Data from HD66780 to MPU)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 53
Enable Pulse Width (High level)	PW_{EH}	250	–	ns	Fig. 53
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 53
Address Set-up Time (RS, R/W–E)	t_{AS}	40	–	ns	Fig. 53
Address Hold Time	t_{AH}	10	–	ns	Fig. 53
Data Delay Time	t_{DDR}	–	250	ns	Fig. 53
Data Hold Time	t_{DHR}	20	–	ns	Fig. 53

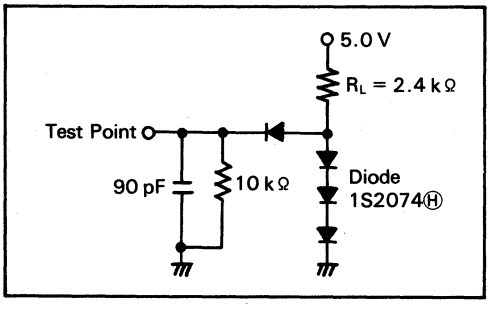


Figure 49 Load Circuit (DB_0–DB_7)

Interface Signal with HD44100H or HD66100F Timing Characteristics
(V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Item		Symbol	Min	Max	Unit	Test Condition
Clock Pulse Width	(High level)	t_{CWH}	800	–	ns	Fig. 54
Clock Pulse Width	(Low level)	t_{CWL}	800	–	ns	Fig. 54
Clock Set-up Time		t_{CSU}	500	–	ns	Fig. 54
Data Set-up Time		t_{SU}	300	–	ns	Fig. 54
Data Hold Time		t_{DH}	300	–	ns	Fig. 54
M Delay Time		t_{DM}	-1000	1000	ns	Fig. 54
Clock Rise/Fall Time		t_{ct}	–	100	ns	Fig. 54

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Max	Unit	Test Condition
Power Supply Rise Time	t_{rCC}	0.1	10	ms	Fig. 51
Power Supply Off Time	t_{OFF}	1	–	ms	Fig. 51

Note: The internal reset circuit will not operate normally unless the preceding conditions are met. In that case, initialize by instruction. (Refer to Initializing by Instruction)

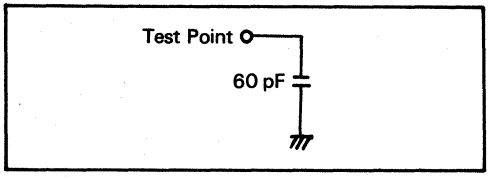


Figure 50 Interface Signal Load Circuit

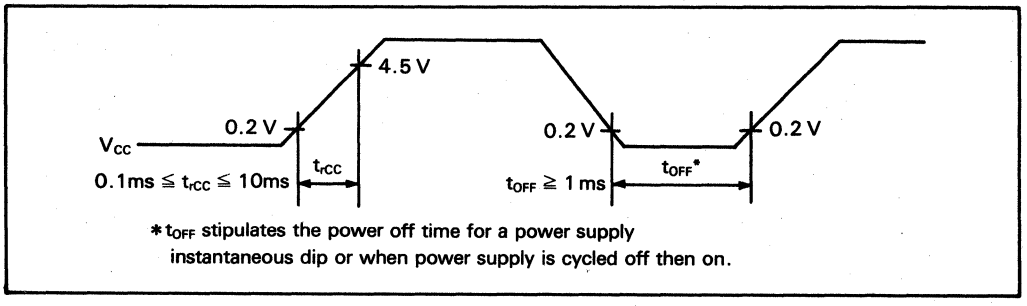


Figure 51 Power Supply Timing

Timing Characteristics

Write Operation

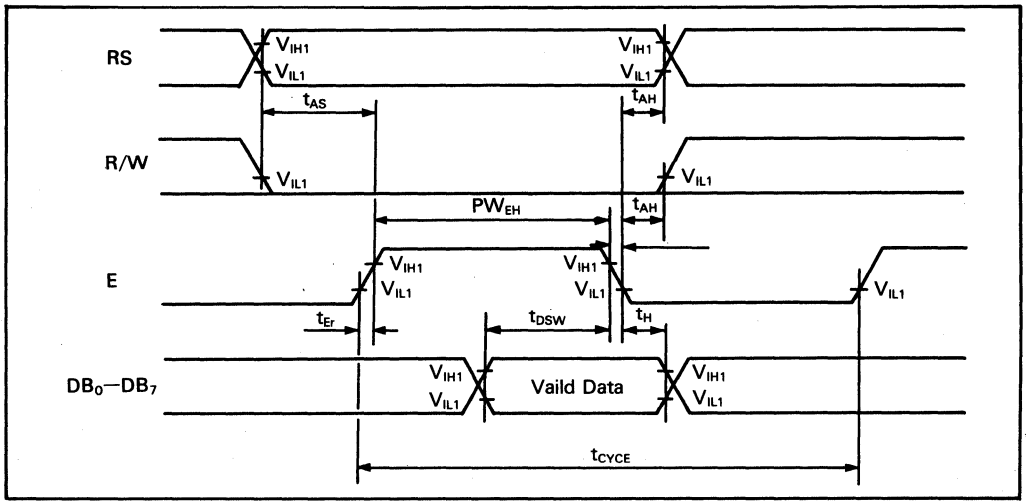


Figure 52 Bus Write Operation Sequence (Writing Data from MPU to HD66780)

Read Operation

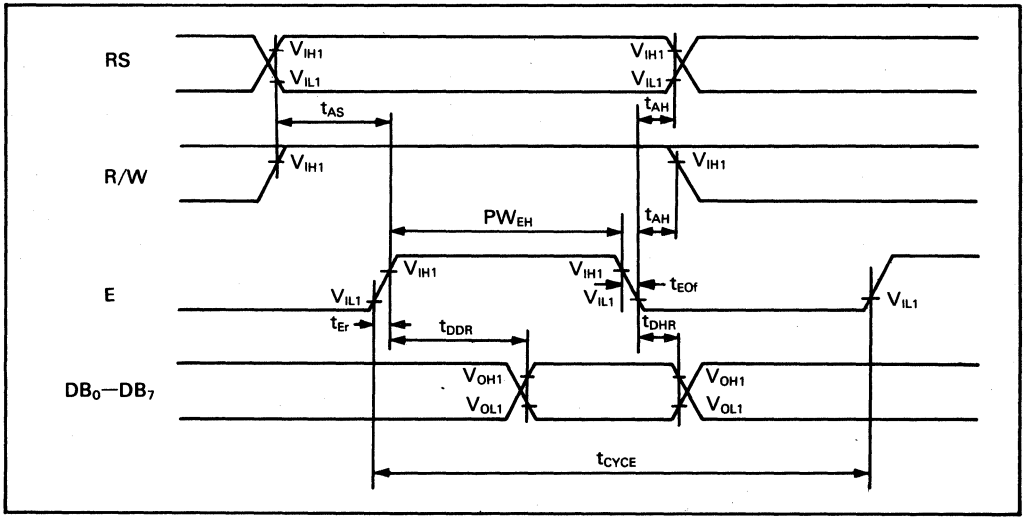


Figure 53 Bus Read Operation Sequence (Reading Data from HD66780 to MPU)

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Interface Signal with Driver LSI HD44100H or HD66100F

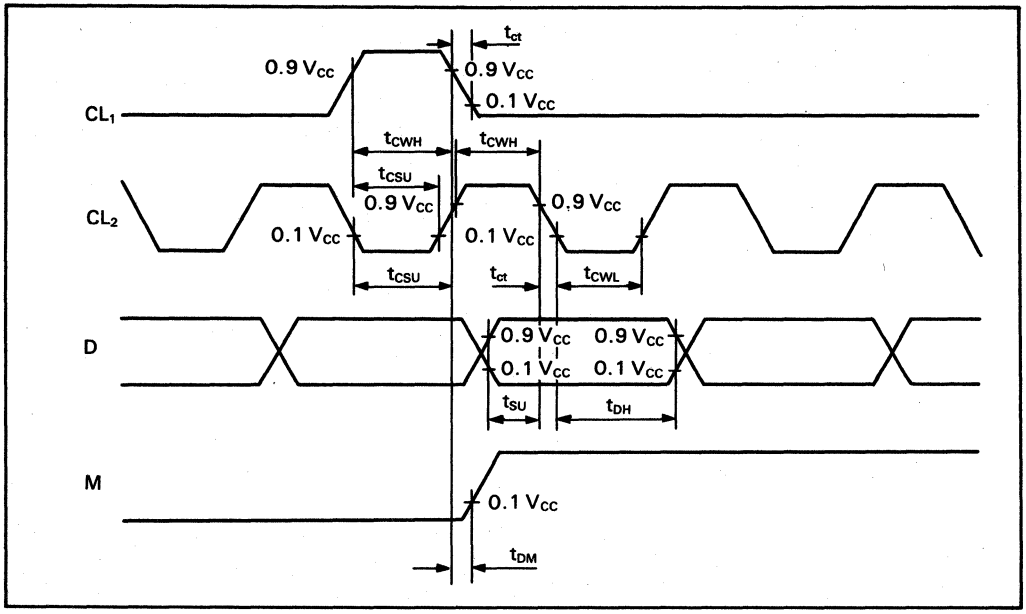


Figure 54 Sending Data to Driver LSI HD44100H or HD66100F

Section Five

Graphic Display LCD Controller/Driver

HD44102CH

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

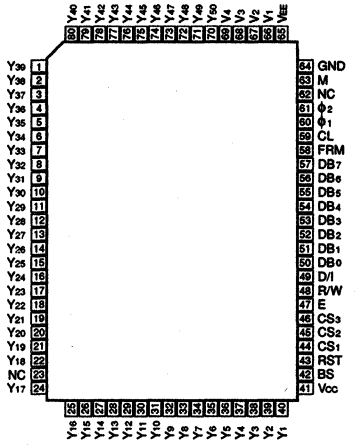
The HD44102CH is a column (segment) driver for dot matrix liquid crystal graphic display systems, storing the display data transferred from a 4-bit or 8-bit microcomputer in the internal display RAM and generating dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of each dot of a liquid crystal display to provide more flexible than character display.

The HD44102CH is produced by the CMOS process. Therefore, the combination of HD44102CH with a CMOS microcontroller can complete portable battery-driven unit ntilizing the liquid crystal display's low power dissipation.

The combination of HD44102CH with the row (common) driver HD44103CH facilitates dot matrix liquid crystal graphic display system configuration.

Pin Arrangement



Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- Interfaces with 4-bit or 8-bit MPU
- RAM data directly displayed by internal display RAM
  RAM bit data 1: On
  RAM bit data 0: Off
- Display RAM capacity: 50 × 8 × 4 (1600 bits)
- Internal liquid crystal display driver circuit (segment output): 50 segment signal drivers
- Duty factor (can be controlled by external input waveform)
  – Selectable duty factors: 1/8, 1/12, 1/16, 1/24, 1/32
- Wide range of instruction functions
  – Display Data Read/Write, Display On/Off, Set Address, Set Display
  – Start Page, Set Up/Down, Read Status
- Low power dissipation
- Power supplies: V_{CC} 5 V ± 10%, V_{EE} 0 to –5 V
- CMOS process
- 80-pin flat plastic package

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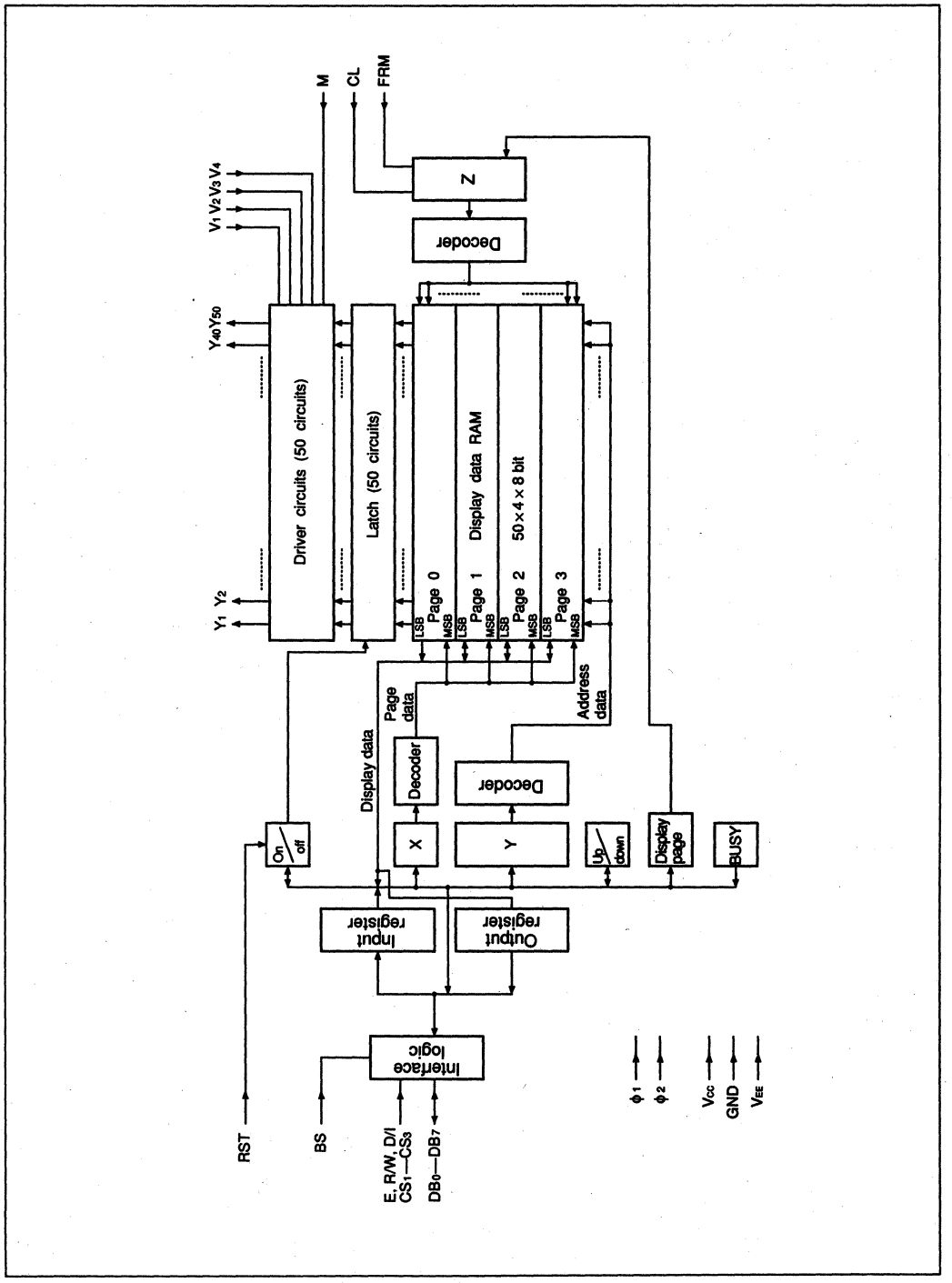
Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} –13.5 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)	V_{T2}	V_{EE} –0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V3, and V4), and I/O common terminals.
3. Applied to terminals V1, V2, V3, and V4.

Electrical Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to –5.5 V, Ta = –20 to 75 °C) (Note 4)

Item	Symbol	Min	Typ	Max	Unit	Test condition	Note
Input high voltage (CMOS)	V_{IHC}	0.7 × V_{CC}	–	V_{CC}	V		5
Input low voltage (CMOS)	V_{ILC}	0	–	0.3 × V_{CC}	V		5
Input high voltage (TTL)	V_{IHT}	2.0	–	V_{CC}	V		6
Input low voltage (TTL)	V_{ILT}	0	–	+0.8	V		6
Output high voltage	V_{OH}	+3.5	–	–	V	I_{OH} = –250 µA	7
Output low voltage	V_{OL}	–	–	+0.4	V	I_{OL} = +1.6 mA	7
Vi-Xj ON resistance	R_{ON}	–	–	7.5	kΩ	V_{EE} = –5 V ± 10%, Load current 100 µA	
Input leakage current (1)	I_{IL1}	–1	–	1	µA	V_{IN} = V_{CC} to GND	8
Input leakage current (2)	I_{IL2}	–2	–	2	µA	V_{IN} = V_{CC} to V_{EE}	9
Operating frequency	f_{CLK}	25	–	280	kHz	φ1, φ2 frequency	10
Dissipation current (1)	I_{CC1}	–	–	100	µA	f_{clk} = 200 kHz frame = 65 Hz during display	11
Dissipation current (2)	I_{CC2}	–	–	500	µA	Access cycle 1 MHz at access	12

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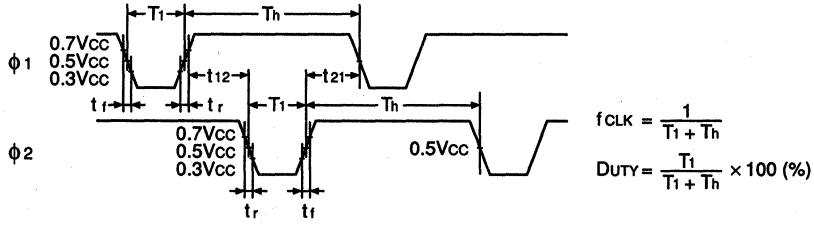
Notes: 4. Specified within this range unless otherwise noted.
5. Applied to M, FRM, CL, BS, RST,ϕ1, ϕ2.
6. Applied to CS1 to CS3, E, D/I, R/W and DBO to DB7.
7. Applied to DB0 to DB7.
8. Applied to input terminals, M, FRM,CL, BS, RST, ϕ1, ϕ2, CS1 to CS3, E, D/I and R/W, and I/O common terminals DB0 to DB7 at high impedance.
9. Applied to V1, V2, V3, and V4.
10. ϕ1 and ϕ2 AC characteristics.

	Symbol	Min	Typ	Max	Unit
Duty factor	Duty	20	25	30	%
Fall time	t_f	–	–	100	ns
Rise time	t_r	–	–	100	ns
Phase difference time	t_{12}	0.8	–	–	µs
Phase difference time	t_{21}	0.8	–	–	µs
$T_1 + T_h$		–	–	40	µs



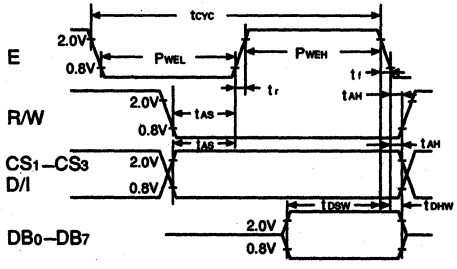
11. Measured by V_{CC} terminal at no output load, at 1/32 dury factor, and frame frequency of 65 Hz, in checker pattern display. Access from the CPU is stopped.
12. Measured by V_{CC} terminal at no output load, 1/32 duty factor and frame frequency of 65 Hz.

Interface AC Characteristics

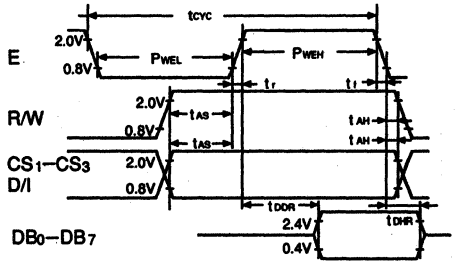
Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	–	–	ns	13, 14
E high level width	P_{WEH}	450	–	–	ns	13, 14
E low level width	P_{WEL}	450	–	–	ns	13, 14
E rise time	t_r	–	–	25	ns	13, 14
E fall time	t_f	–	–	25	ns	13, 14
Address setup time	t_{AS}	140	–	–	ns	13, 14
Address hold time	t_{AH}	10	–	–	ns	13, 14
Data setup time	t_{DSW}	200	–	–	ns	13
Data delay time	t_{DDR}	–	–	320	ns	14, 15
Data hold time at write	t_{DHW}	10	–	–	ns	13
Data hold time at read	t_{DHR}	20	–	–	ns	14

Notes:

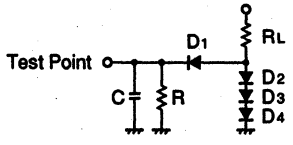
13. At CPU write



14. At CPU read



15. DB0 to DB7 load circuits



R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF (including jig capacitance)
Diodes D_1 to D_4 are all 1S2074 Ⓗ

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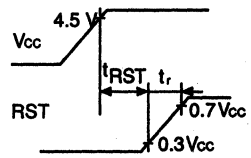
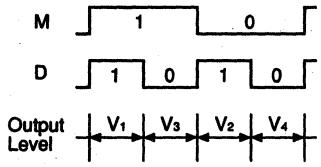
Notes: 16. Display off at initial power up.
The HD44102CH can be placed in the display off state by setting terminal RST to low at initial power up.
No instruction other than the Read Status can be accepted while the RST is at the low level.

	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	–	–	µs
Rise time	t_r	–	–	200	ns



Pin Description

Pin Name	Pin Number	I/O	Function
Y1 – Y50	50	O	Liquid crystal display drive output. Relationship among output level, M and display data (D):



CS1 – CS3 3 I Chip select

CS1	CS2	CS3	State
L	L	L	Non-selected
L	L	H	Non-selected
L	H	L	Non-selected
L	H	H	Selected read/write enable
H	L	L	Selected write enable only
H	L	H	Selected write enable only
H	H	L	Selected write enable only
H	H	H	Selected read/write enable

E 1 I Enable

At write (R/W = Low): Data of DB0 to DB7 is latched at the fall of E.

At read (R/W = High): Data appears at DB0 to DB7 while E is at high level.

Pin Name	Pin Number	I/O	Function
R/W	1	I	Read/Write R/W = High: Data appears at DB0 to DB7 and can be read by the CPU when E = high and CS2, CS3 = high. R/W = Low: DB0 to DB7 can accept input when CS2, CS3 = high or CS1 = high.
D/I	1	I	Data/Instruction D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.
DB0–DB7	8	I/O	Data bus, three-state I/O common terminal

E	R/W	CS1	CS2	CS3	State of DB0 to DB7
H	H	*	H	H	Output state
*	L	H	*	*	Input state,
*	L	*	H	H	High impedance
Others					High impedance

M	1	I	Signal to convert liquid crystal display drive output to AC.
CL	1	I	Display synchronous signal At the rise of CL signal, the liquid crystal display drive signal corresponding to display data appears.
FRM	1	I	Display synchronous signal (frame signal) This signal presets the 5-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
ϕ1, ϕ2	2	I	2-phase clock signal for internal operation The ϕ1 and ϕ 2 clocks are used to perform the operations (input/output of display data and execution of instructions) other than display.
RST	1	I	Reset signal The display disappears and Y address counter is set in the up counter state by setting the RST signal to low level. After releasing reset, the display off state and up mode is held until the state is changed by the instruction.
BS	1	I	Bus select signal BS = Low: DB0 to DB7 operate for 8–bit length. BS = High: DB4 to DB7 are valid for 4–bit length only. 8–bit data is accessed twice in the high and low order.
V1, V2, V3, V4	4		Power supply for liquid crystal display drive V1 and V2: Selection voltage V3 and V4: Non-selection voltage

5

Pin Name	Pin Number	I/O	Function
V_{CC}	3		Power supply
GND			V_{CC}–GND: Power supply for internal logic
V_{EE}			V_{CC}–V_{EE}: Power supply for liquid crystal display drive circuit logic

Function of Each Block

Interface Logic

The HD44102CH can use the data bus in 4-bit or 8-bit word length to enable interface to a 4-bit or 8-bit CPU.

1. 4 bit mode (BS = High)
   8-bit data is transferred twice for every 4 bits through the data bus when the BS signal is high.

The data bus uses the high order 4 bits (DB4 to DB7). First, the high order 4 bits (DB4 to DB7 in 8-bit data length) are transferred and then the low order 4 bits (DB0 to DB3 in 8-bit data length).

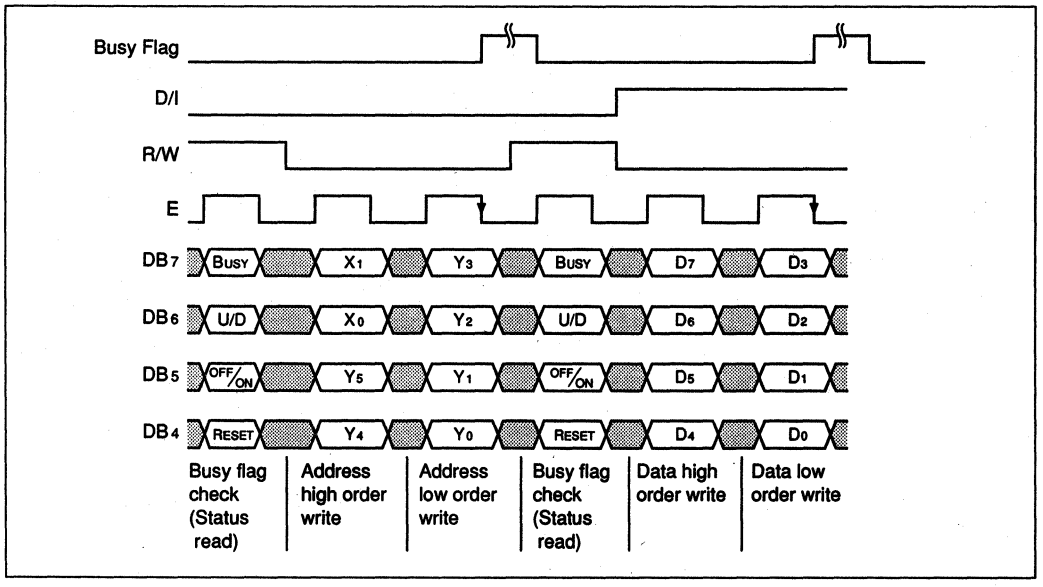


Figure 1 4-Bit Mode Timing

Note: Execute instructions other than status read in 4-bit length each. The busy flag is set at the fall of the second E signal. The status read is executed once. After the execution of the status read, the first 4 bits are considered the high order 4 bits. Therefore, if the busy flag is checked after the transfer of the high order 4 bits, retransfer data from the higher order bits. No busy check is required in the transfer between the high and low order bits.

2. 8-bit mode (BS = Low)

If the BS signal is low, the 8 data bus lines (DB0 to DB7) are used for data transfer.

DB7: MSB (Most significant bit)

DB0: LSB (Least significant bit)

For AC timing, refer to note 12 to note 15 of "Electrical Characteristics".

Input Register

8-bit data is written into this register by the CPU. The instruction and display data are distinguished by the 8-bit data and D/I signal and then a given operation is performed. Data is received at the fall of the E signal when the CS is in the select state and R/W is in write state.

Output Register

The output register holds the data read from the display data RAM. After display data is read, the display data at the address now indicated is set in this output register. After that, the address is increased or decreased by 1. Therefore, when an address is set, the correct data doesn't appear at the read of the first display data. The data at a specified address appears at the second read of data (figure 2).

X, Y Address Counter

The X, Y address counter holds an address for reading/writing display data RAM. An address is set in it by the instruction. The Y address register is composed of a 50-bit up/down counter. The address is increased or decreased by 1 by the read/write operation of display data. The up/down mode can be determined by the instruction or RST signal. The Y address register counts by looping the values of 0 to 49. The X address register has no count function.

Display On/Off Flip/Flop

This flip/flop is set to on/off state by the instruction or RST signal. In the off state, the latch of display data RAM output is held reset and the display data output is set to 0. Therefore, display disappears. In the on state, the display data appears according to the data in the RAM and is displayed. The display data in the RAM is independent of the display on/off.

Up/Down Flip/Flop

This flip/flop determines the count mode of the Y address counter. In the up mode, the Y address register is increased by 1. 0 follows 49. In the down mode, the register is decreased by 1. 0 is followed by 49.

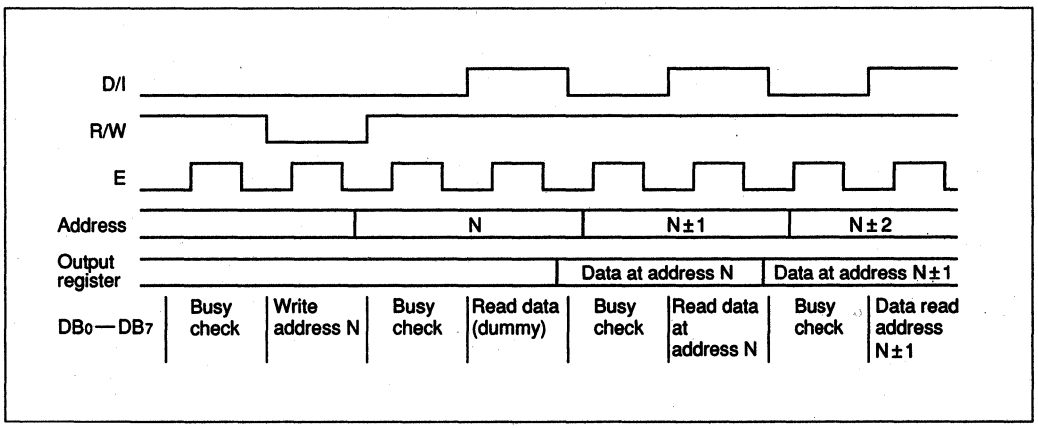


Figure 2 Data Output

5

Display Page Register

The display page register holds the 2-bit data that indicates a display start page. This value is preset to the high order 2 bits of the Z address counter by the FRM signal. This value indicates the value of the display RAM page displayed at the top of the screen.

Busy Flag

After an instruction other than status read is accepted, the busy flag is set during its effective period, and reset when the instruction is not effective (figure 3). The value can be read out on DB7 by the status read instruction.
The HD44102CH cannot accept any other instructions than the status read in the busy state. Make sure the busy flag is reset before issuing an instruction.

Z Address Counter

The Z address counter is a 5-bit counter that counts up at the fall of CL signal and generates an address for outputting the display data synchronized with the common signal. 0 is preset to the low order 3 bits and a display start page to the high order 2 bits by the FRM signal.

Latch

The display data from the display data RAM is latched at the rise of CL signal.

Liquid Crystal Driver Circuit

Each of 50 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of display data from latchs and the M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

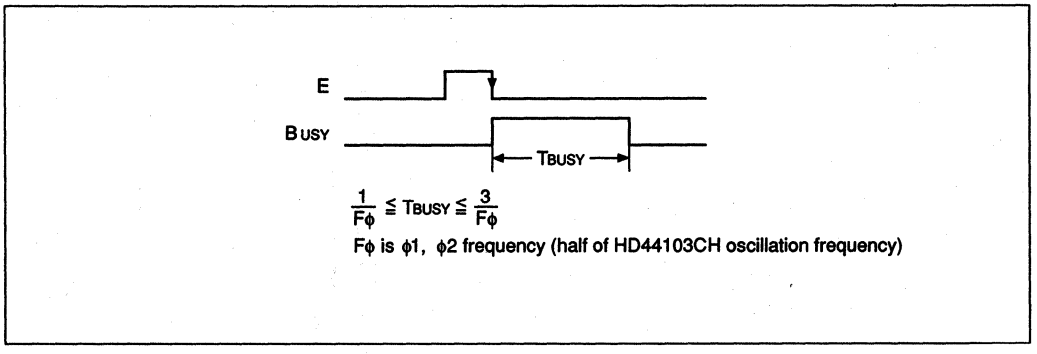


Figure 3 Busy Flag

Display RAM

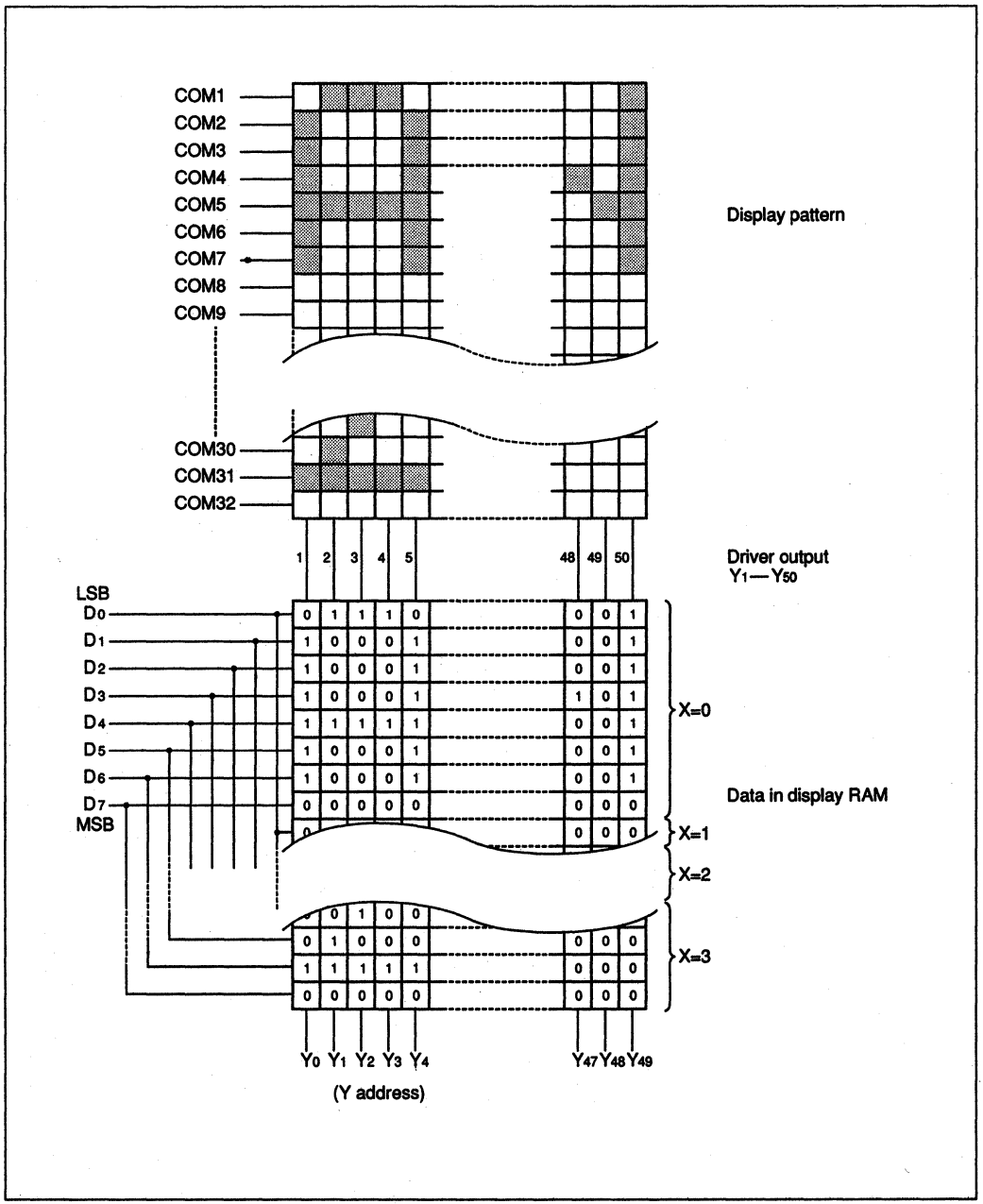


Figure 4 Relationship between Data in RAM and Display (Display start page 0, 1/32 duty)

5

Display Control Instructions

Read/Write Display Data

		MSB DB LSB	
R/W	D/I	7 6 5 4 3 2 1 0	
1	1	(Display data)	
		Read (CPU ← HD44102CH)	
0	1	(Display data)	
		Write (CPU →HD44102CH)	

Sends or receives data to or from the address of the display RAM specified in advance. However, a dummy read may be required for reading display data. Refer to the description of the output register in Function of Each Block.

Display On/Off

		MSB DB LSB	
R/W	D/I	7 6 5 4 3 2 1 0	
0	0	0 0 1 1 1 0 0 1	Display on
0	0	0 0 1 1 1 0 0 0	Display off

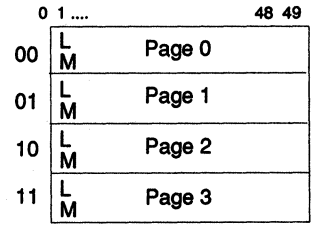
Turns the display on/off. RAM data is not affected.

Set X/Y Address

		MSB DB LSB	
R/W	D/I	7 6 5 4 3 2 1 0	
0	0	0 0	
0	0	0 1	Binary numbers of 0–49
0	0	1 0	
0	0	1 1	

X address (page) — Y address (address)

Y address



Display Data RAM

Display Start Page

		MSB DB LSB	
R/W	D/I	7 6 5 4 3 2 1 0	
0	0	0 0 1 1 1 1 1 0	
		.....	Refer to figure 5 (a)
0	0	0 1 1 1 1 1 1 0	
		.....	Refer to figure 5 (b)
0	0	1 0 1 1 1 1 1 0	
		.....	Refer to figure 5 (c)
0	0	1 1 1 1 1 1 1 0	
		Display start page	
		.....	Refer to figure 5 (d)

Specifies the RAM page displayed at the top of the screen. Display is as shown in figure 4. When the display duty factor is more than 1/32 (For example, 1/24, 1/16), display begins at a page specified by the display start page only by the number of lines.

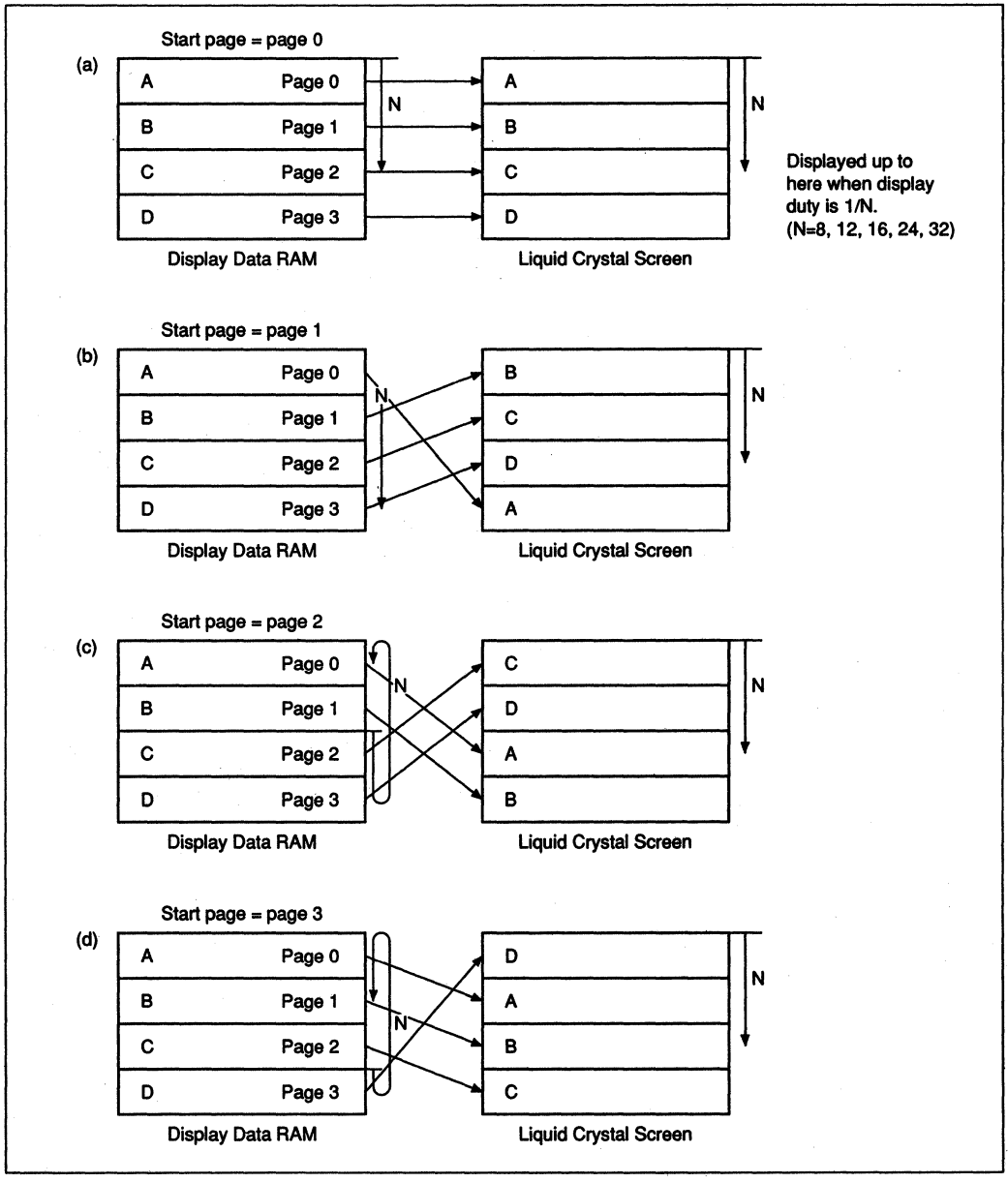


Figure 5 Display Start Page

Up/Down Set

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	1	1	Up mode
0	0	0	0	1	1	1	0	1	0	Down mode

Sets Y address register in the up/down counter mode.

Status Read

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
1	0	BUSY	UP/DOWN	OFF/ON	RESET	0	0	0	0

BUSY → Goes to 1 while all other instructions are being executed.
While 1, none of the other instructions are accepted.

UP/DOWN → Goes to 1 when address counter is in the up mode.
Goes to 0 when address counter is in the down mode.

OFF/ON → Goes to 1 in the display off state.
Goes to 0 on the display on state.

RESET → Goes to 1 when RST is in the reset state
(Busy also goes to 1).
Goes to 0 when RST is in the operating state.

Connection Between LCD Drivers (Example of 1/32 Duty Factor)

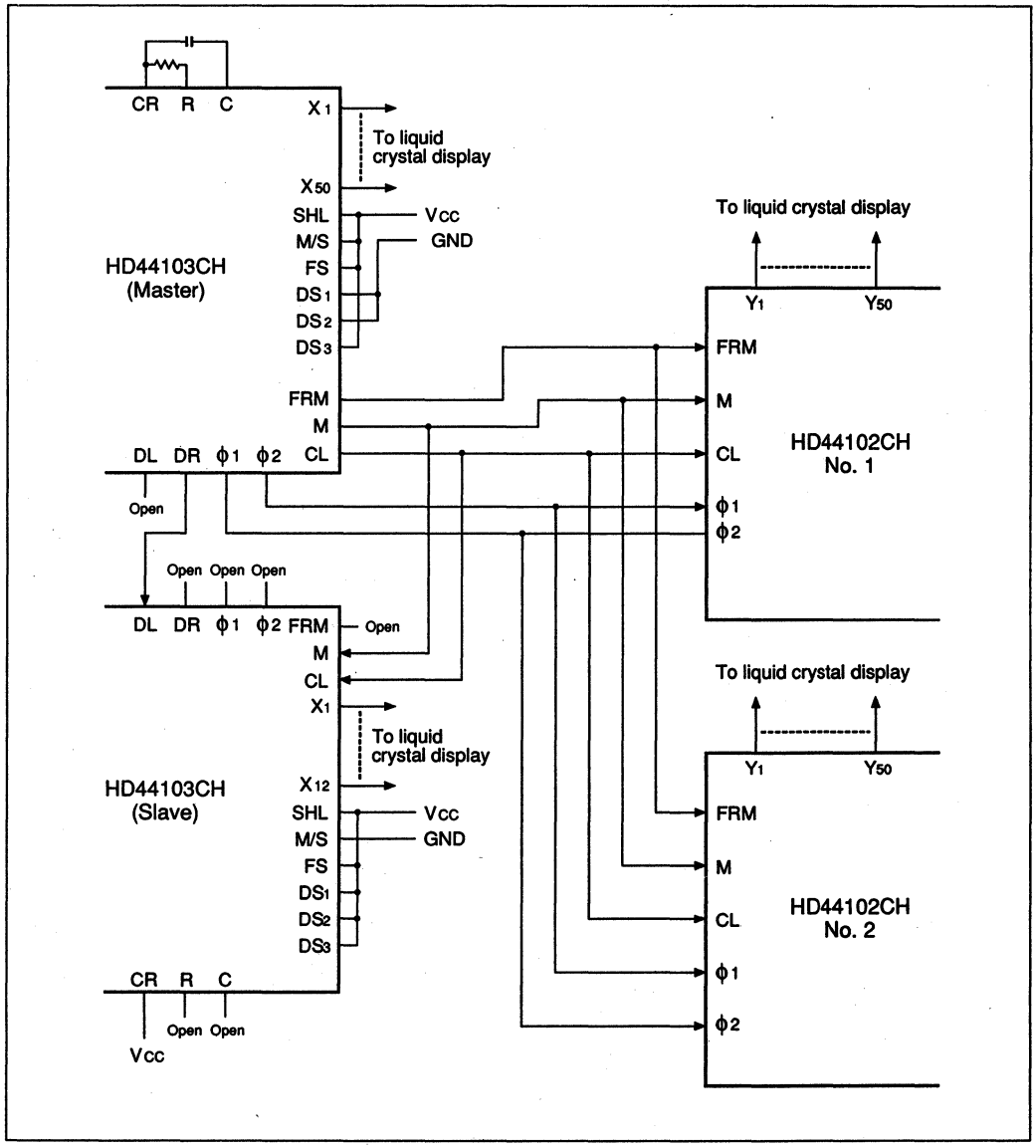


Figure 6 1/32 Duty Factor Connection Example

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Interface to CPU

1. Example of connection to HD6800

In the decoder given in this example, the addresses of HD44102CH in the address space of HD6800 are:
Read/write of display data: $'FFFF'
Write of display instruction: $'FFFE'
Read of status: $'FFFE'

Thus, the HD44102CH can be controlled by reading/writing data at these addresses.

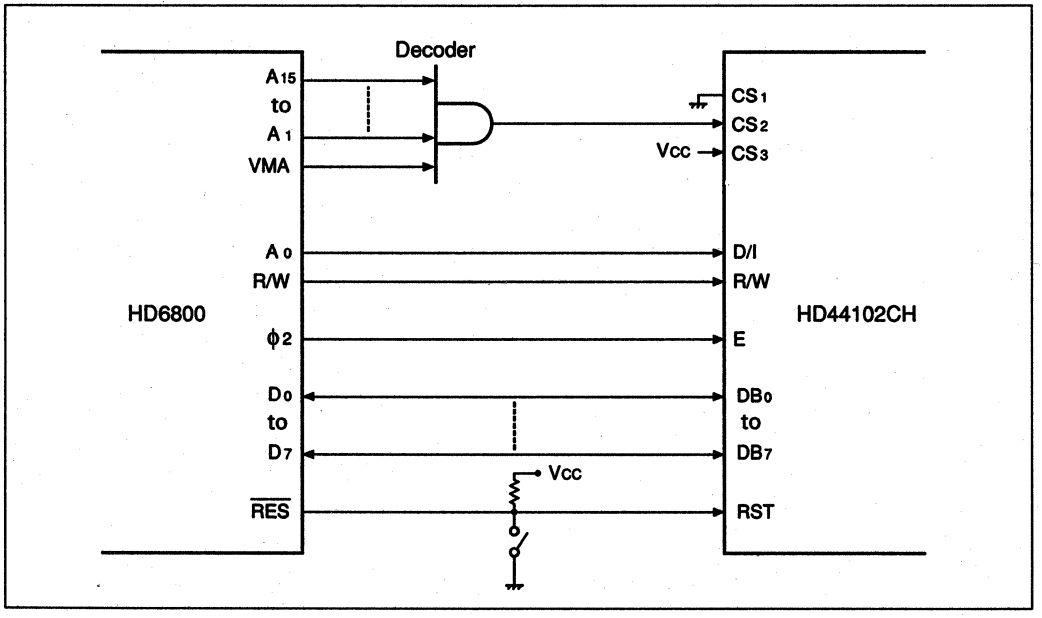

Figure 7 Example of Connection to HD6800 Series

2. Example of connection to HD6801

- The HD6801 is set to mode 5. P10–P14 are used as output ports, and P30–P37 are used as the data bus.
- The 74LS154 is a 4–to–16 decoder that decodes 4 bits of P10–P13 to select the chips.
- Therefore, the HD44102CH can be controlled by selecting the chips through P10–P13 and specifying the D/I signal through P14 in advance, and later conducting memory read or write for external memory space $0100 to $01FF of HD6801. The IOS signal is output to SC1, and the R/W signal is output to SC2.
- For further details on HD6800 and HD6801, refer to their manuals.

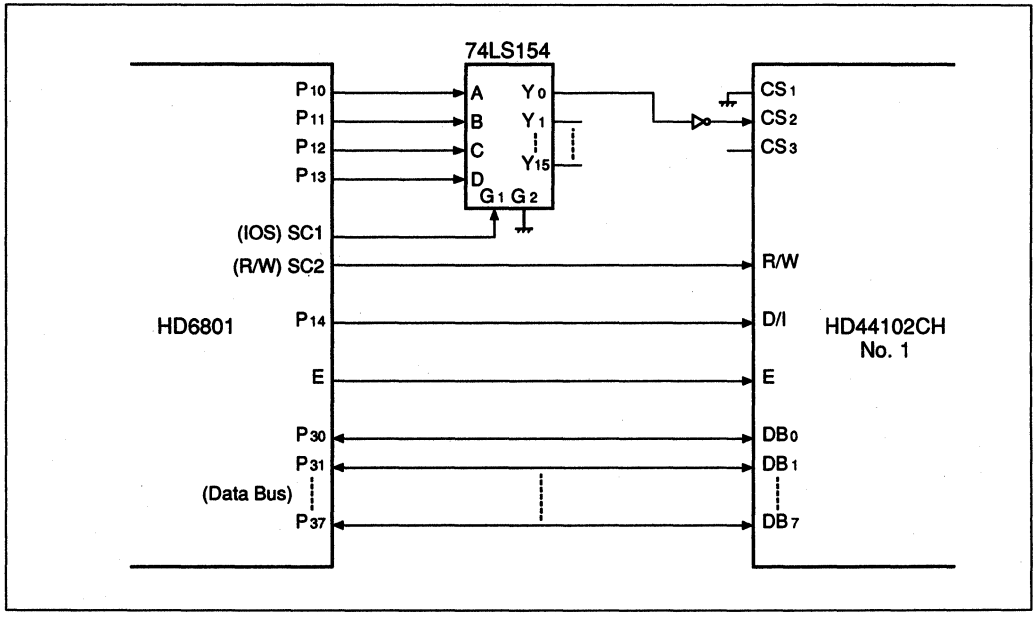

Figure 8 Example of Connection to HD6801

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Connection to Liquid Crystal Display

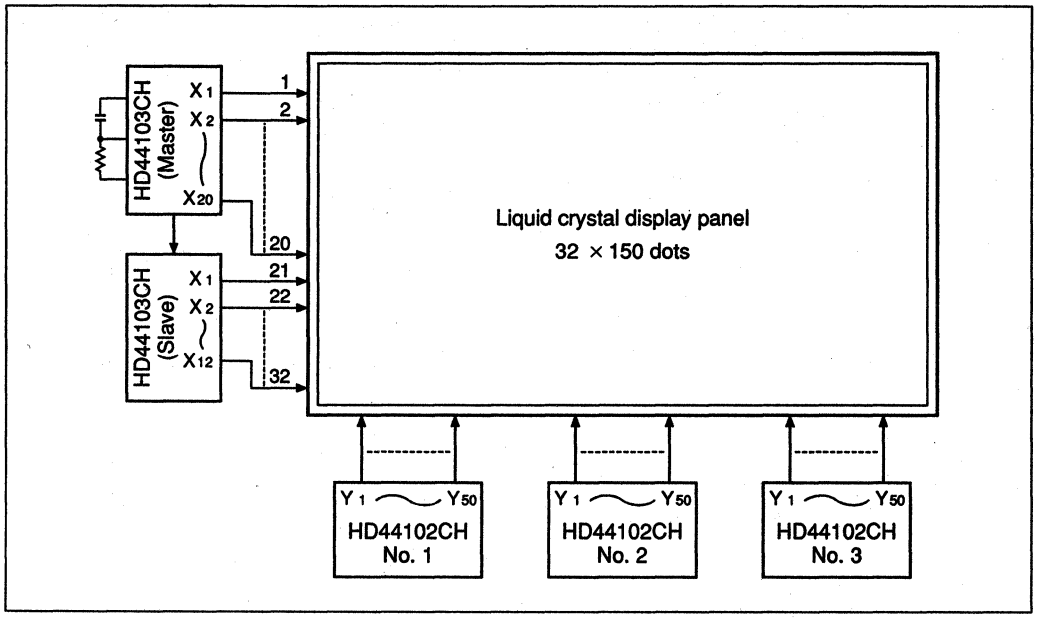

Figure 9 Example of Connection to 1/32 Duty Factor, 1-Screen Display

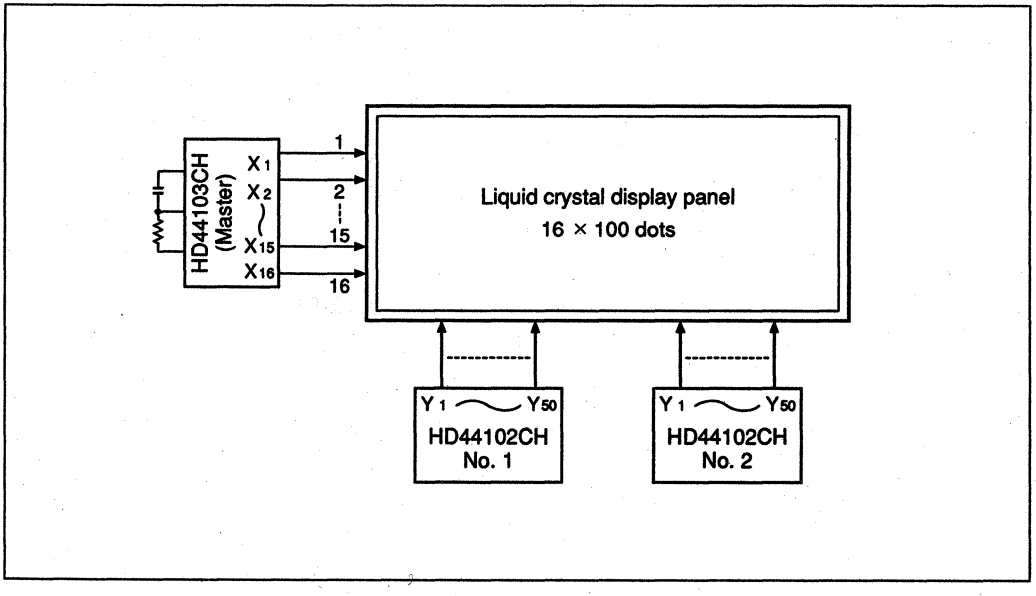

Figure 10 Example of Connection to 1/16 Duty Factor, 1–Screen Display

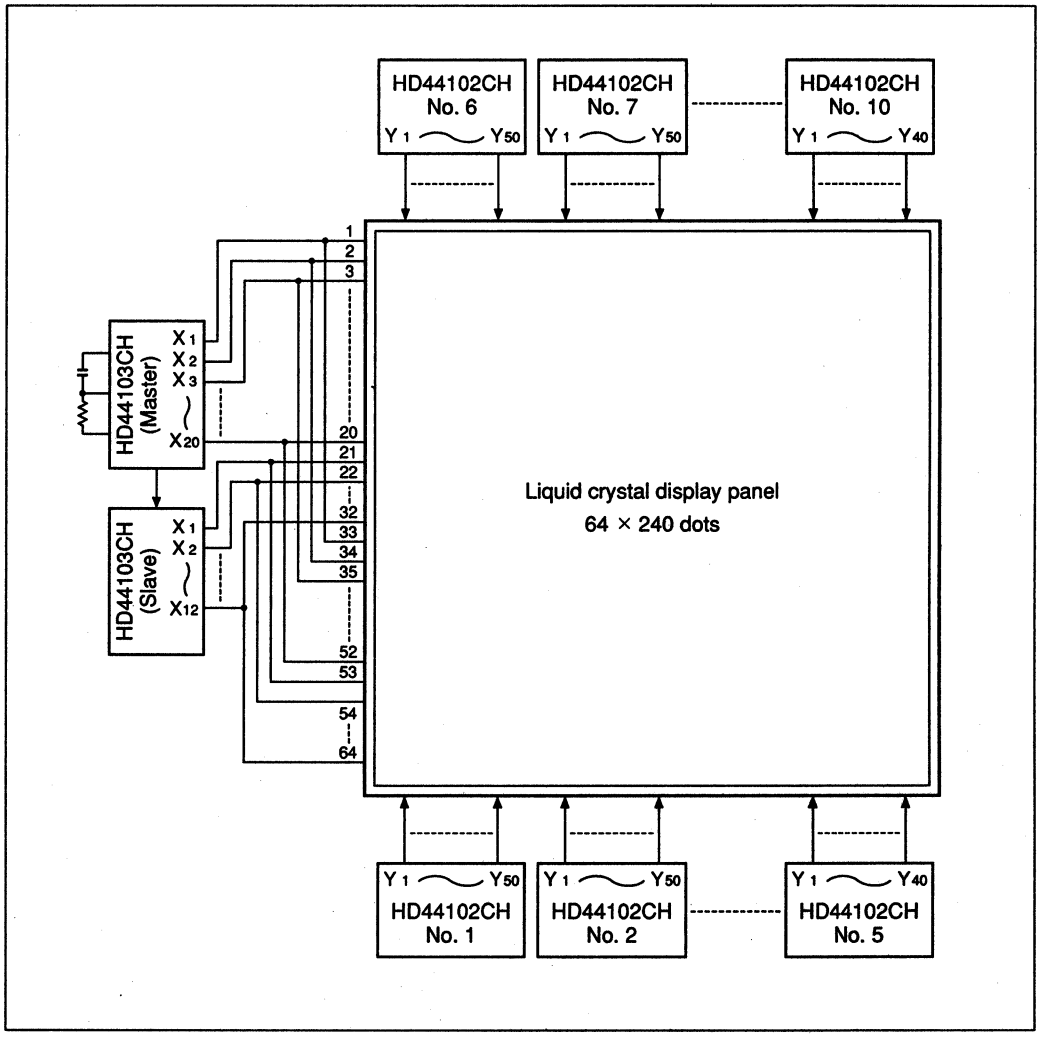

Figure 11 Example of Connection to 1/32 Duty Factor, 2-Screen Display

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Limitations on Using 4-Bit Interface Function

The HD44102 usuallly transfers display control data and display data via 8-bit data bus. It also has the 4-bit interface function in which the HD44102 transfers 8-bit data by dividing it into the high-order 4 bits and the low-order 4-bits in order to reduce the number of wires to be connected. You should take an extra care in using the application with the 4-bit interface function since it has the following limitations.

Limitations

The HD44102 is designed to transfer the high-order 4-bits and the low-order 4-bits of data in that order after busy check. The LSI does not work normally if the signals are in the following state for the time period (indicated with (*) in fifure 11) from when the high-order 4 bits are written (or read) to when the low-order 4 bits are written (or read); R/W = high and D/I = low while the chip is being selected (CS1 = high and CS2 = CS3 = don't care, or CS1 = low and CS2 = CS3 = high).

If the signals are in the limited state mentioned before for the time period indicated with (*) the LSI does not work normally. Please do not make the signals indicated with dotted lines simultaneously. As far as the time period indicated with (**), there is no problem.

The following explains how the malfunction is caused and gives the measures in application.

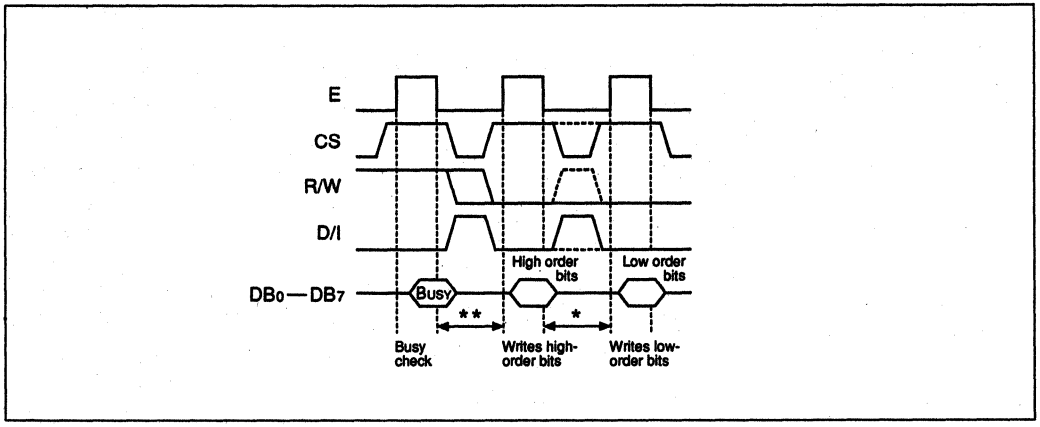

Figure 12 Example of Writing Display Control Instructions

Cause

Busy check checks if the LSI is ready to accept the next instruction or display data by reading the status register to the HD44102. And at the same time, it resets the internal counter counting the order of high-order data and low-order data. This function makes the LSI ready to accept only the high-order data after busy check. Strictly speaking, if R/W = high and D/I = low while the chip is being selected, the internal counter is reset and the LSI gets ready to accept high-order bits. Therefore, the LSI takes low-order data for high-order data if the state mentioned above exist in the interval between transferring high-order data and transferring low-order data.

Measures in Application

1. HD44102 Controlled Via Port

When you control the HD44102 with the port of a single-chip microcomputer, you should take care of the software and observe the limitations strictly.

2. HD44102 Controlled Via Bus

a. Malfunction Caused by Hazard

Hazard of input signals may also cause the phenomenon mentioned before. The phase shift at transition of the input signals may cause the malfunction and so the AC characteristics must be carefully studied.

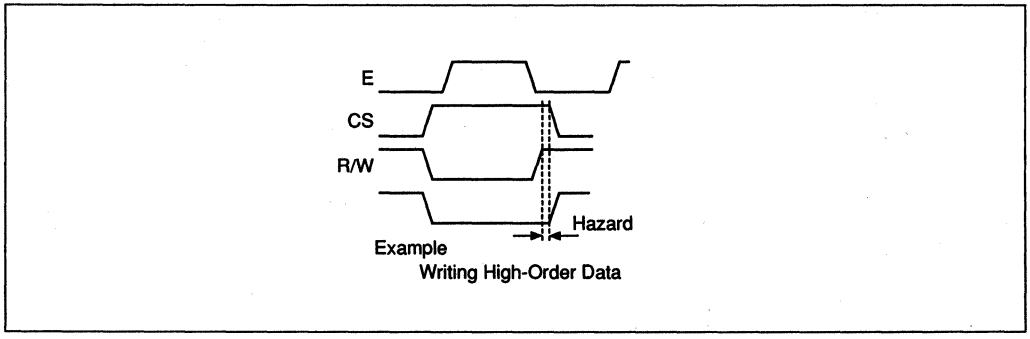

Figure 13 Input Hazard

b. Using 2-Byte Instruction

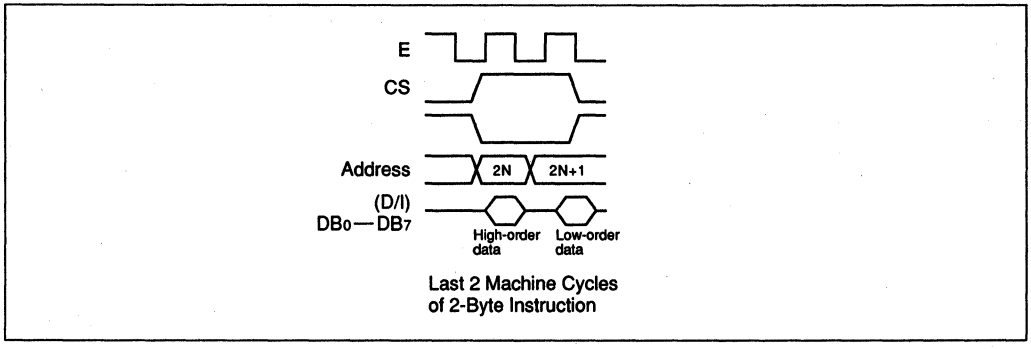

Figure 14 2-Byte Instruction

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In an application with the HD6303, you can prevent malfunction by using 2-byte instructions such as STD and STX. This is because the high-order and low-order data are accessed in that order without a break in the last machine cycle of the instruction and R/W and D/I do not change in the meantime. However, you cannot use the least significant bit of the address signals as the D/I signal since the address for the second byte has an added 1. Design the CS decoder so that the addresses for the HD44102 should be 2N and 2N + 1, and that those addresses should be accessed when using 2-byte instructions. For example, in figure 14 the address signal A_1 is used as D/I signal and A_2 –A_{15} are used for the CS decoder. Addresses 4N and 4N + 1 are for instruction access and addresses 4N + 2 and 4N + 3 are for display data access.

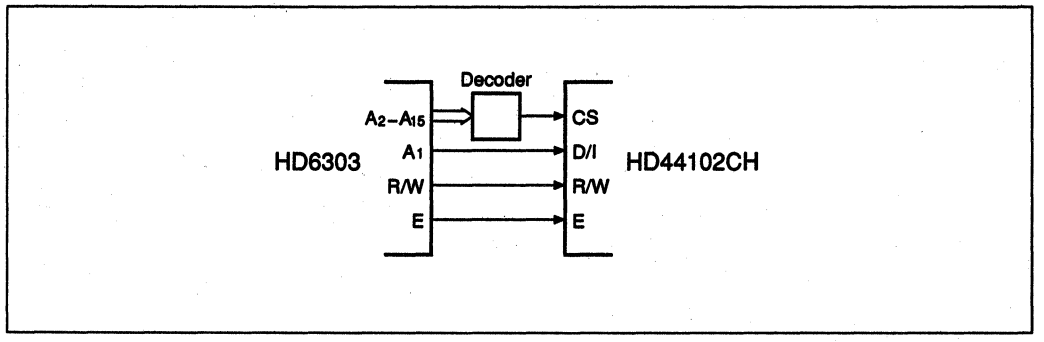


Figure 15 HD6303 Interface

HD44103CH
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

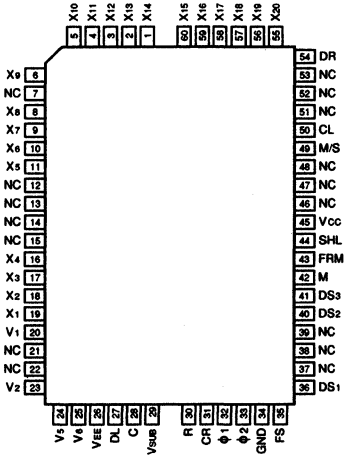
Description

The HD44103CH is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102CH) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty. It can select 5 types of display duty ratio: 1/8, 1/12, 1/16, 1/24, and 1/32. 20 driver output lines are provided, and the impedance is low (500 Ω max.) to enable a large screen to be driven.

Features

- Dot matrix liquid crystal graphic display common driver incorporating the timing generation circuit
- Internal oscillator (Oscillation frequency can be selected by attaching an oscillation resistor and an oscillation capacity)
- Generates display timing signals
- 20-bit bidirectional shift register for generating common signals
- 20 liquid crystal driver circuits with low output impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32
- Low power dissipation
- Power supplies: V_{CC}: 5 V ± 10%, V_{EE}: 0 to –5.5 V
- CMOS process
- 60-pin plastic flat package

Pin Arrangement



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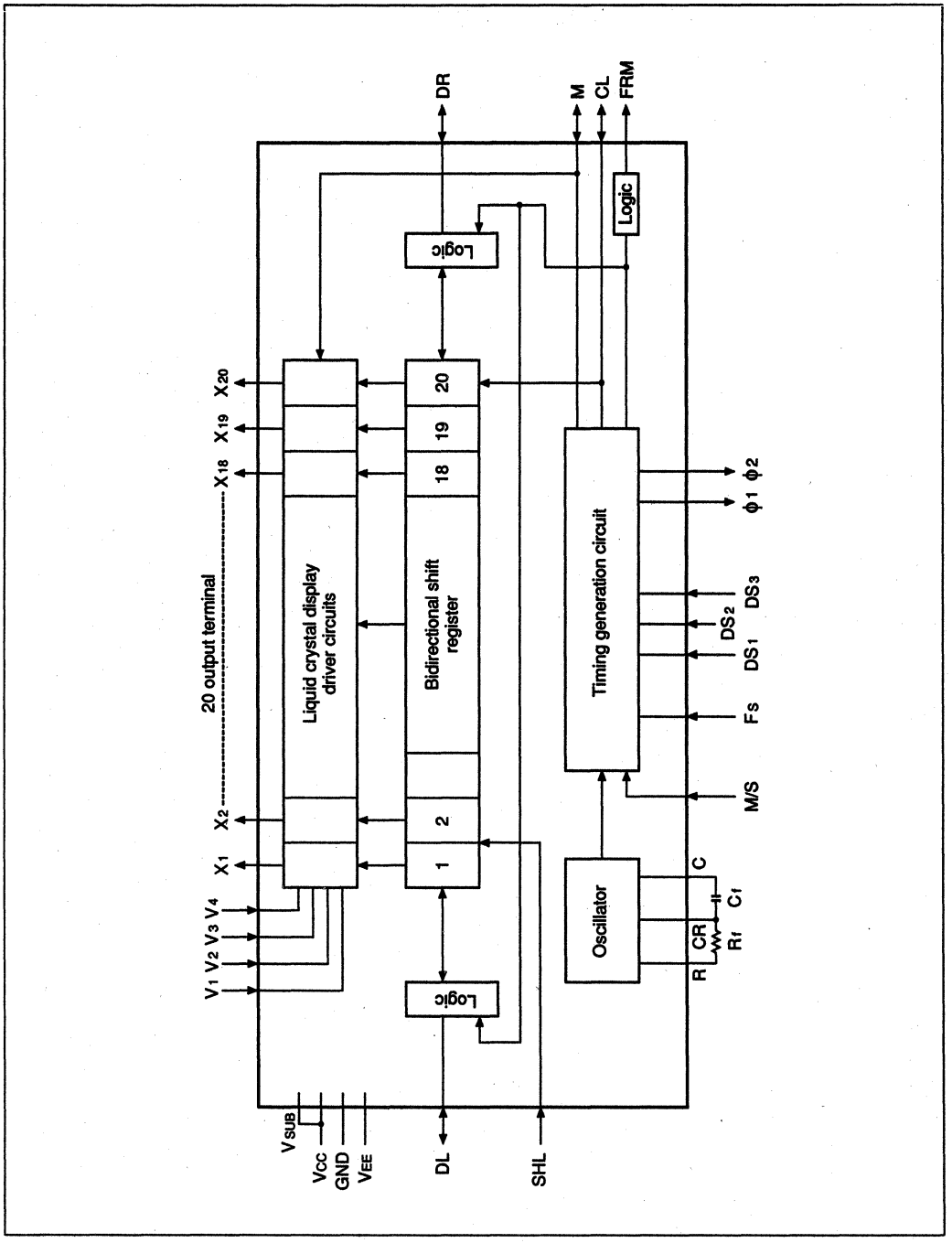
Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} –13.5 to V_{CC} + 0.3	V	4
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} –0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6.
4. Connect a protection resistor of 220 Ω ± 5% to V_{EE} power supply in series.

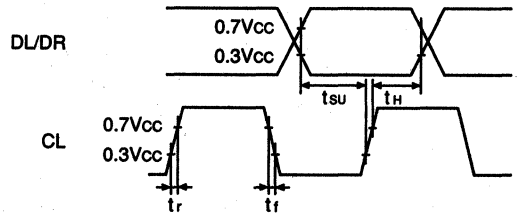
Electrical Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to –5.5 V, Ta = –20 to +75 °C) (Note 5)

Item	Symbol	Min	Typ	Max	Unit	Test condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	–	V_{CC}	V		6
Input low voltage	V_{IL}	0	–	0.3 × V_{CC}	V		6
Output high voltage	V_{OH}	V_{CC} – 0.4	–	–	V	I_{OH} = –400 µA	7
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = +400 µA	7
Vi-Xj on resistance	R_{ON}	–	–	500	Ω	V_{EE} = –5 ± 10%, Load current ±150 µA	
Input leakage current (1)	I_{IL1}	–1	–	1	µA	V_{IN} = V_{CC} to GND	8
Input leakage current (2)	I_{IL2}	–2	–	2	µA	V_{IN} = V_{CC} to V_{EE}	9
Shift frequency	f_{SFT}	–	–	50	kHz	In slave mode	10
Oscillation frequency	f_{OSC}	300	430	560	kHz	R_f = 68 kΩ ± 2%, C_f = 10 pF ± 5%	11
External clock operating frequency	f_{cp}	50	–	560	kHz		
External clock duty	Duty	45	50	55	%		12
External clock rise time	t_{rcp}	–	–	50	ns		12
External clock fall time	t_{fcp}	–	–	50	ns		12
Dissipation power (master)	P_{w1}	–	–	4.4	mW	CR oscillation = 430 kHz	13
Dissipation power (slave)	P_{w2}	–	–	1.1	mW	Frame frequency = 70 Hz	14

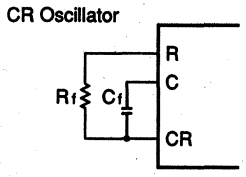
5

Notes: 5. Specified within this range unless otherwise noted.
6. Applied to CR, FS, DS1 to DS3, M, SHL, M/S, CL, DR, and DL.
7. Applied to DL, DR, M, FRM, CL, ϕ1 and ϕ2.
8. Applied to input terminals CR, FS, DS1 to DS3, SHL and M/S, and I/O common terminals DL, DR, M, and CL at high impedance.
9. Applied to V1, V2, V5, and V6.
10. Shift operation timing

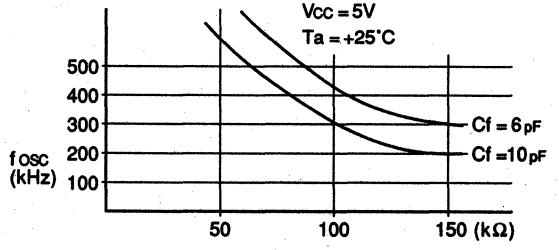


	Min	Typ	Max	Unit
t_{SU}	5	–	–	µs
t_H	5	–	–	µs
t_r	–	–	100	ns
t_f	–	–	100	ns

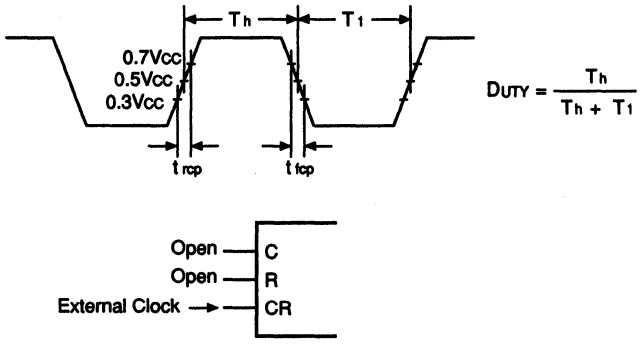
11. Relationship between oscillation frequency and R_f/C_f



The values of R_f and C_f are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to the required value.

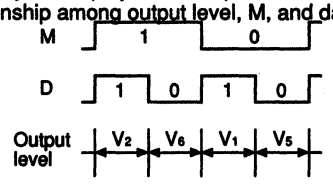
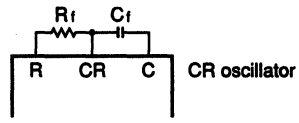


12.



13. Measured by V_{CC} terminal at output non-load of R_f = 68 kΩ ± 2% and C_f = 10pF ± 5%, 1/32 duty factor in the master mode. Input terminals must be fixed at V_{CC} or GND while measuring.
14. Measured by V_{CC} terminal at output non-load, 1/32 duty factor, frame frequency of 70 Hz in the slave mode. Input terminals must be fixed at V_{CC} or GND while measuring.

Pin Description

Pin Name	Pin Number	I/O	Function
X1–X20	20	O	Liquid crystal display driver output. Relationship among output level, M, and data (D) in shift register: 
CR, R, C	3		Oscillator 
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal

5

Pin Name	Pin Number	I/O	Function
CL	1	I/O	Shift register shift clock. Master: Output terminal Slave: Input terminal
FRM	1	O	Frame signal, Display synchronous signal.
DS1–DS3	3	I	Display duty ratio select.

Display Duty Ratio	1/24	1/12	X	1/32	1/16	1/8
DS1	L	H	L	H	L	H	L	H
DS2	L	L	H	H	L	L	H	H
DS3	L	L	L	L	H	H	H	H

Pin Name	Pin Number	I/O	Function
FS	1	I	Frequency select. The relationship between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows: FS = High: $f_{OSC} = 6144 \times f_{FPM}$ (1) FS = Low: $f_{OSC} = 3072 \times f_{FRM}$ (2) Example (1) When FS = high, adjust Rf and Cf so that the oscillation frequency is approx. 430 kHz if the frame frequency is 70 Hz. Example (2) When FS = low, adjust Rf and Cf so that the oscillation is approx. 215 kHz, in order to obtain the same display waveforms as example 1. When compared with example 1, the power dissipation is reduced because of operation at lower frequency. However, the operating clocks $\phi 1$ and $\phi 2$ supplied to the column driver have lower frequencies. Therefore, the access time of the column driver HD44102CH becomes longer.
DL, DR	2	I/O	Data I/O terminals of bidirectional shift register.
SHL	1	I	Shift direction select of bidirectional shift register.

SHL	Shift Direction
H	DL → DR
L	DL ← DR

Pin Name	Pin Number	I/O	Function
M/S	1	I	Master/slave select. M/S = High: Master mode The oscillator and timing generation circuit supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is placed in the output state. M/S = Low: Slave mode The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and Cl are placed in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FD, DS1, DS2, and DS3 to V_{CC}. When display duty ratio is 1/8, 1/12, or 1/16, one HD44103CH is required. Use it in the master mode. When display duty ratio is 1/24 or 1/32, two HD44103CHs are required. Use the one in the master mode to drive common signals 1 to 20, and the other in the slave mode to drive common signals 21 to 24 (32).
ϕ1, ϕ2	2	O	Operating clock output terminals for HD44102CH. The frequencies of ϕ1 and ϕ2 become half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC} GND V_{EE}	3		Power supply. V_{CC}–GND:Power supply for internal logic V_{CC}–V_{EE}: Power supply for driver circuit logic

5

Block Functions

Oscillator

The oscillator is a CR oscillator attached to an oscillation resistor Rf ans osckllation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to Electrical Characteristics (Note 10) to make proper adjustment.

Timing Genaration Circuit

The timing generation circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS, DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

Bidirectional Shift Register

20-bit bidirectional shift register. The shift direction is determined by SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 20 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Applications

Refer to the applications of the HD44102CH.

HD44105H
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD44105H is a common signal driver for LCD dot matrix graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102H) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty cycle. It can select 7 types of display duty cycle 1/8, 1/12, 1/16, 1/24,1/32, 1/48, and 1/64. It provides 32 driver output lines and the impedance is low (1 kΩ max) enough to drive a large screen.

Features

- Dot matrix graphic display common driver including the timing generation circuit
- Internal oscillator (Oscillation frequency is selectable by attaching an oscillation resistor and an oscillation capacitor)
- Generates display timing signals
- 32-bit bidirectional shift register for generating common signals
- 32 liquid crystal driver circuits with low impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64
- Low power dissipation
- Power supplies: V_{CC} = +5 V ± 10%
  V_{EE} = 0 to –5.5 V
- CMOS process
- 60-pin flat plastic package

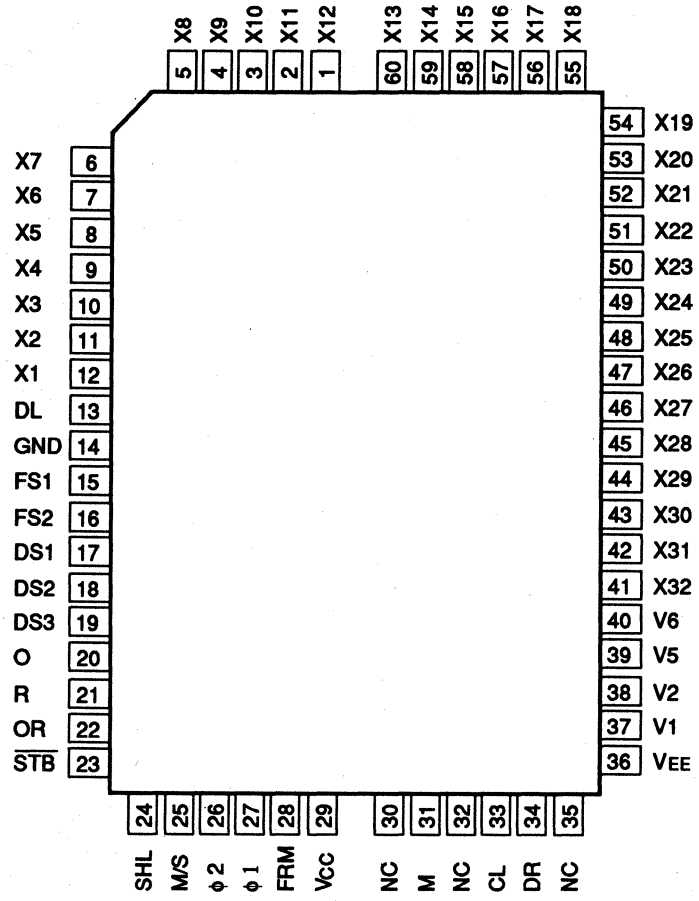
Absolute Maximum Rating (Ta =25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} –13.5 to V_{CC} +0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} +0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} –0.3 to V_{CC} +0.3	V	3
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. Referred to GND = 0 V.
2. Applied to input terminals (except for V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6. Connect a protection resistor of 47 Ω ± 10% to each terminal in series.

5

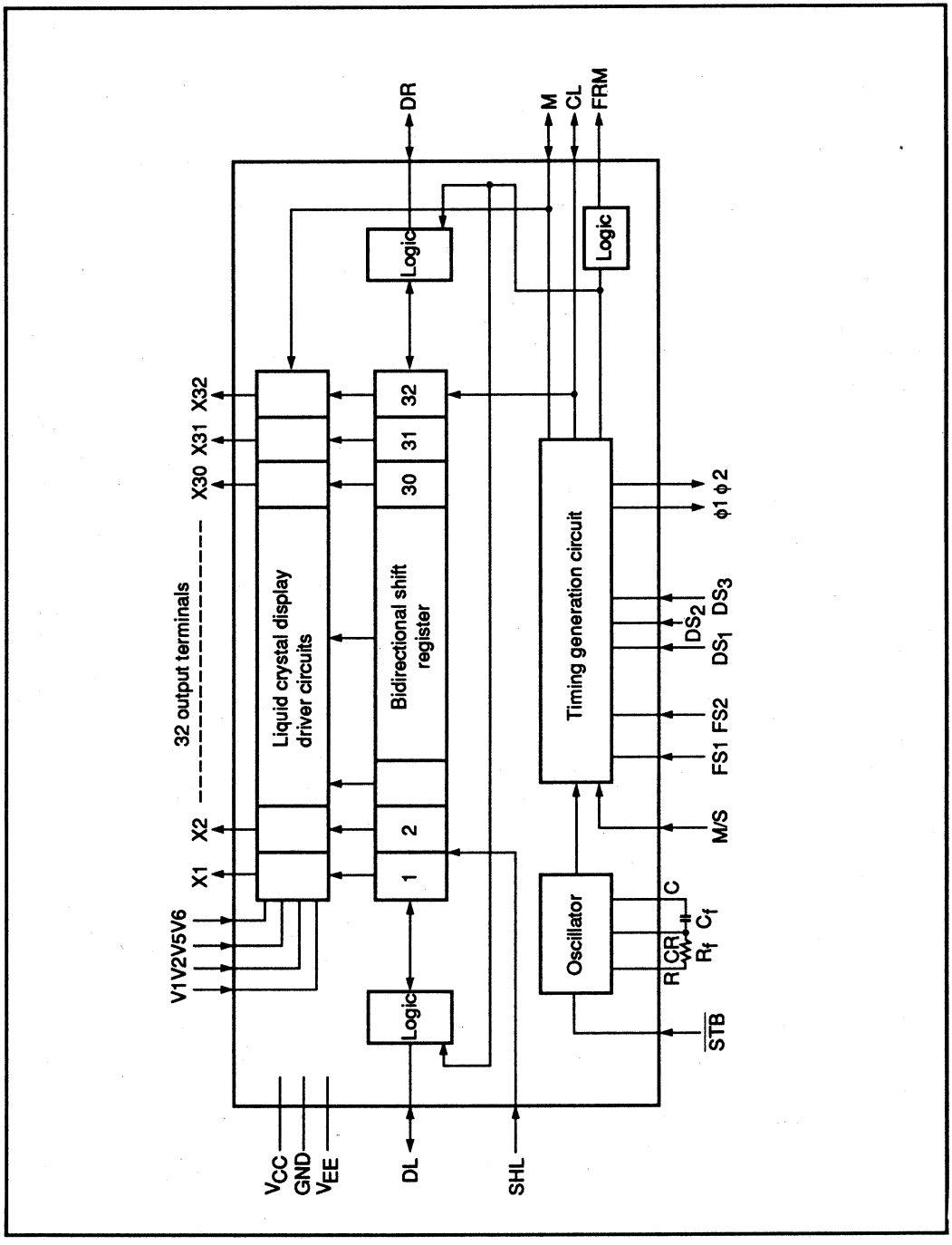
Pin Arrangement



(Top View)

Note: NCs show unused terminals. Don't connect any lines to them in using this LSI.

Block Diagram



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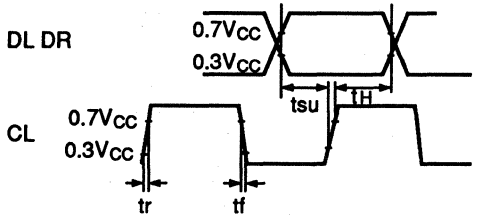
Electrical Characteristics

(Note 4)

(V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to −5.5 V, Ta = −20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		5
Input low voltage	V_{IL}	0	—	0.3 × V_{CC}	V		5
Output high voltage	V_{OH}	V_{CC} −0.4	—	—	V	I_{OH} = −400 µA	6
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	6
Vi-Xj On resistance	R_{ON}	—	—	1000	Ω	V_{EE} = −5 V ± 10%, Load current ±15 µA	
Input leakage current (1)	I_{IL1}	−1	—	1	µA	V_{IN} = V_{CC} to GND	7
Input leakage current (2)	I_{IL2}	−5	—	5	µA	V_{IN} = V_{CC} to V_{EE}	8
Shift frequency	F_{SFT}	—	—	50	kHz	In slave mode	9
Oscillation frequency	f_{OSC}	300	430	560	kHz	Rf = 68 kΩ ± 2%, Cf = 10 pF ± 5%	10
External clock operating frequency	f_{CP}	50	—	560	kHz		11
External clock duty cycle	Duty	45	50	55	%		11
External clock rise time	t_{rCP}	—	—	50	ns		11
External clock fall time	t_{fCP}	—	—	50	ns		11
Dissipation power (Master)	P_{W1}	—	—	4.4	mW	CR oscillation, 430 kHz	12
Dissipation power (Slave)	P_{W2}	—	—	1.1	mW	Frame 70 kHz	13

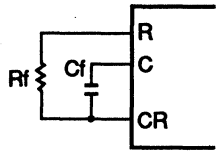
Notes:
4. Specified within this range unless otherwise noted.
5. Applied to CR, FS1, FS2, DS1 to DS3, M, SHL, M/S, CL, DR, DL, and $\overline{STB}$.
6. Applied to DL, DR, M, FRM, CL, φ1, and φ2.
7. Applied to input terminals CR, FS1, FS2, DS1 to DS3, SHL, M/S, and $\overline{STB}$ and I/O common terminals DL, DR, M, and CL at high impedance.
8. Applied to V1, V2, V5, and V6.
9. Shift operation timing.



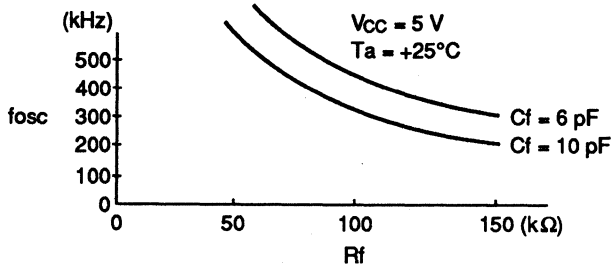
	Min	Typ	Max	Unit
tsu	5	–	–	µs
t_H	5	–	–	µs
tr	–	–	100	ns
tf	–	–	100	ns

Notes: 10. Relation between oscillation frequency and Rf, Cf.

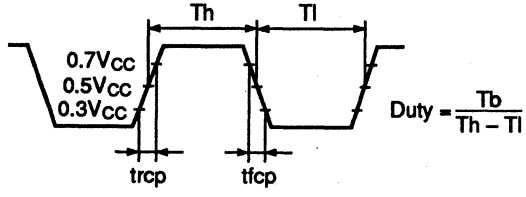
Connection

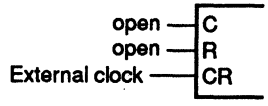


The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



11.





12. Measured by V_{CC} terminal at output non-load of Rf = 68 kΩ ± 2% and Cf = 10 pF ± 5%, and 1/32 duty cycle in the master mode.
Input terminals are connected to V_{CC} or GND.
13. Measured by V_{CC} terminal at output non-load, 1/32 duty cycle, and frame frequency of 70 Hz in the slave mode.
Input terminals are connected to V_{CC} or GND.

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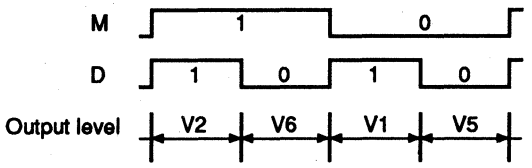
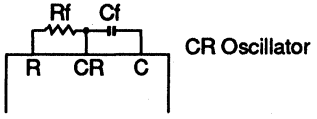
Pin Description

Pin Name	Pin Number	I/O	Function
X1–X32	32	O	Liquid crystal display driver output. Relation among output level, M, and data (D) in shift register. 
CR, R, C	3		Oscillator.  CR Oscillator
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal
CL	1	I/O	Shift register shift clock. Master: Output terminal Slave: Input terminal
FRM	1	O	Frame signal, Display synchronous signal.
DS1–DS3	3	I	Display duty ratio select.

Display Duty Ratio	1/8	1/16	1/32	1/64	–	1/12	1/24	1/48
DS1	L	L	H	H	L	L	H	H
DS2	L	H	L	H	L	H	L	H
DS3	L	L	L	L	H	H	H	H

FS1–FS2 | 2 | I | Selects frequency.

The relation between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows:

FS1	FS2	f_{OSC}(kHz)	f_{FRM}(Hz)	f_M(Hz)	f_{CP}(kHz)
L	L	107.5	70	35	53.8
H	L	107.5	70	35	53.8
L	H	215.0	70	35	107.5
H	H	430.0	70	35	215.0

f_{OSC}: Oscillation frequency
f_{FRM}: Frame frequency
f_M: M signal frequency
f_{CP}: Frequencies of $\phi 1$ and $\phi 2$

Pin Description (cont)

Pin Name	Pin Number	I/O	Function
$\overline{STB}$	1	I	Input terminal for testing. Connect this terminal to V_{CC}.
DL, DR	2	I/O	Data I/O terminals of bidirectional shift register.
SHL	1	I	Selects shift direction of bidirectional shift register. SHL: H — Shift Direction: DL → DR SHL: L — Shift Direction: DL ← DR
M/S	1	I	Selects Master/Slave. M/S = High: Master mode The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is in the output state. M/S = Low: Slave mode The timing generation circuit stop operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FS1, FS2, DS1, DS2, DS3, $\overline{STB}$ to V_{CC}. When display duty ratio is 1/8, 1/12, 1/16, 1/24, 1/32, one HD44105H is required. Use it in the master mode. When display duty ratio is 1/48, 1/64, two HD44105Hs are required. Use one in the master mode to drive common signals 1 to 32, and another in the slave mode to drive common signals 33 to 48(64).
$\phi1$, $\phi2$	2	O	Operating clock output terminals for HD44102CH. The frequencies of $\phi1$ and $\phi2$ are half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC}, GND V_{EE}	3		Power supply. V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for driver circuit logic

5

Block Functions

Oscillator

A CR oscillator attached to an oscillation resistor Rf and an oscillation capacitor Cf. The oscillation frequency v aries with the values of Rf and Cf and the mounting conditions. Refer to electrical characteristics (note 10) to make proper adjustment.

Timing Generation Circuit

This circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS1, FS2 and DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

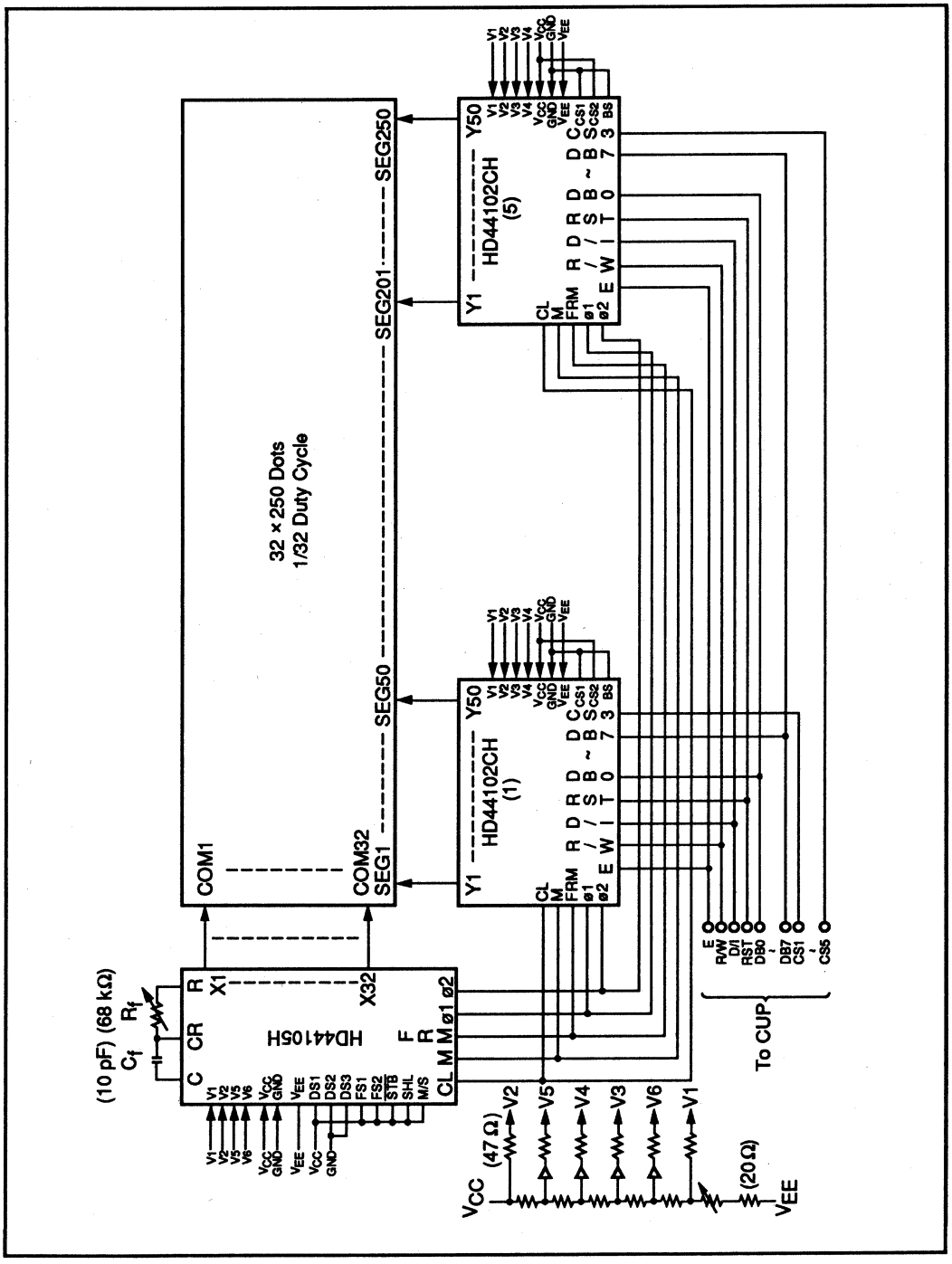
Bidirectional Shift Register

A 32-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 32 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Connection between HD44105H and HD44102CH



HD61100A
(LCD Driver with 80-Channel Output)

Description

The HD61100A is a driver LSI for liquid crystal display systems. It receives serial display data from a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

It has liquid crystal driving outputs which correspond to internal 80-bit flip/flops. Both static drive and dynamic drive are possible according to the combination of transfer clock frequency and latch clock frequency.

Features

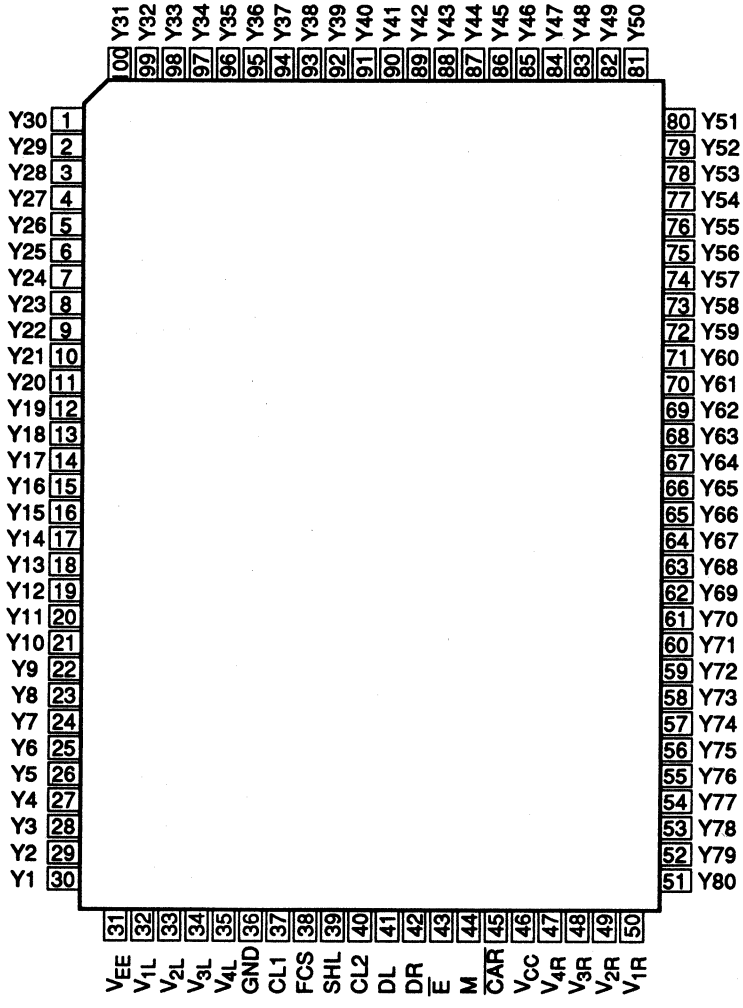
- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Display duty cycle
  Any duty cycle is selectable according to combination of transfer clock and latch clock
- Data transfer rate: 2.5 MHz max.
- Power supply
  V_{CC}: +5 V ± 10% (Internal logic)
  V_{EE}: 0 to –1.5 V (Liquid crystal display driver circuit)
- Liquid crystal driving level: 17.0 V max.
- CMOS process
- 100-pin flat plastic package (FP-100)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	– 0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	– 0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature	Topr	– 20 to +75	°C	
Storage temperature	Tstg	– 55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using it beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, $\overline{E}$, and M.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain:
   $V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}$.
   Connect a protection resistor of 15 Ω ± 10% to each terminals in series.

Pin Arrangement



(Top view)

5

Electrical Characteristics

DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{EE} = 0 to −11.5 V, Ta = −20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		1
Input low voltage	V_{IL}	O	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} −0.4	—	—	V	I_{OH} = − 400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = +400 µA	2
Driver resistance	R_{ON}	—	—	7.5	kΩ	V_{EE} = − 10 V, Load current = 100 µA	3
Input leakage current	I_{IL1}	−1	—	+1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	−2	—	+2	µA	V_{IN} = V_{EE} to V_{CC}	4
Dissipation current (1)	I_{GND}	—	—	1.0	mA		5
Dissipation current (2)	I_{EE}	—	—	0.1	mA		5

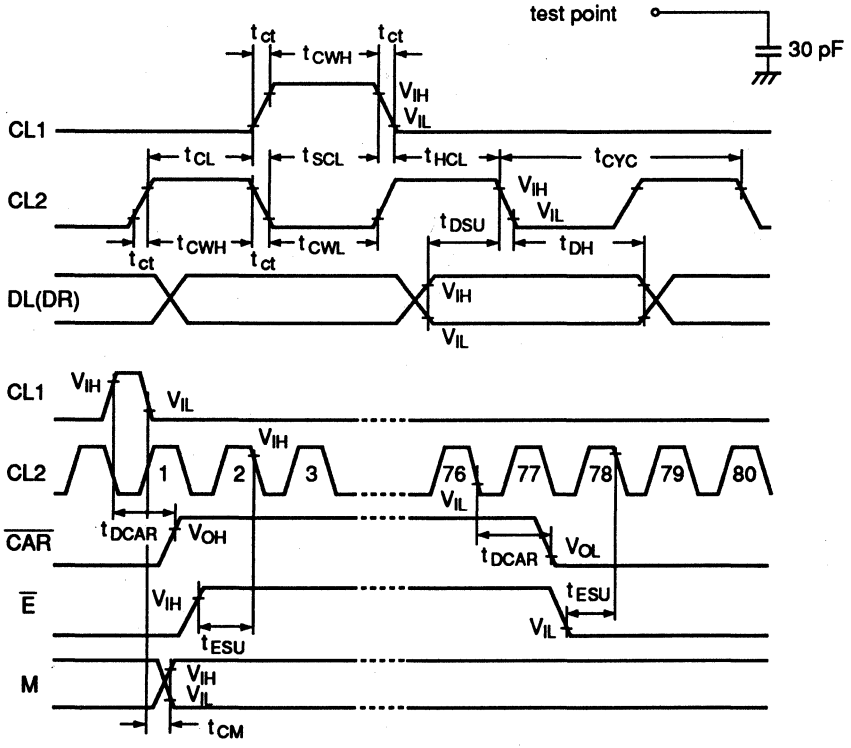
Notes: 1. Applies to CL1, CL2, FCS, SHL, $\overline{E}$, M, DL, and DR.
2. Applies to DL, DR, and $\overline{CAR}$.
3. Applies to Y1—Y80.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.
5. Specified when display data is transferred under following conditions:
   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 30 Hz (frame frequency/2)
   Specified when V_{IH} = V_{CC}, V_{IL} = GND and no load on outputs.
   I_{GND}: currents between V_{CC} and GND.
   I_{EE}: currents between V_{CC} and V_{EE}.

AC Characteristics

(V_{CC} = 5 V ± 10%. GND = 0 V, V_{EE} = 0 to −11.5 V, Ta = −20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{CYC}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{Ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
$\overline{E}$ setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuits are connected for specification:



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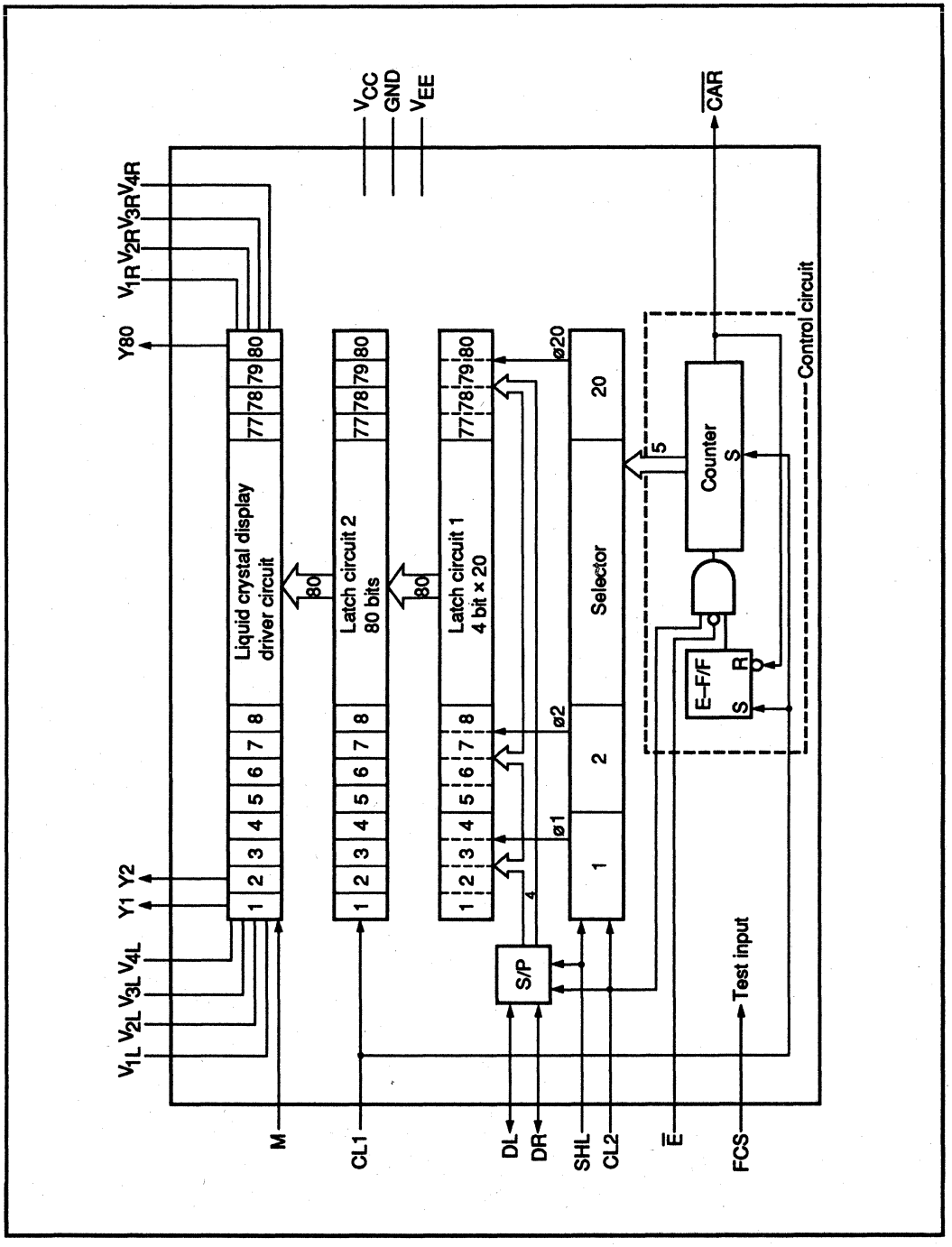
Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/Parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is "L" level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR which is in the output status.
When SHL is "H" level, input data from terminal DR without connecting any lines to terminal DL.

80-bit Latch Circuit 1

The 4-bit data is latched at $\phi 1$ to $\phi 20$ and output to latch circuit 2. When SHL is "L" level, the data from DL are latched one in order of 1→2→3 ... → 80 of each latch. When SHL is "H" level, they are latched in a reverse order (80→79→78 ... →1).

Selector

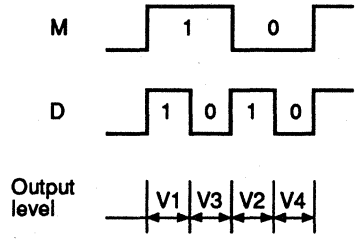
The selector decodes output signals from the counter and generates latch clock $\phi 1$ to $\phi 20$. When the LSI is not active, $\phi 1$ to $\phi 20$ are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E—F/F (enable F/F) indicates "1", S/P conversion is started by inputting "L" level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into "L" level and E—F/F is reset to "0", and consequently the conversion stops. E—F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at "H" level of CL1.
Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into "H" level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61100A.

5

Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}-V_{4L} V_{1R}-V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1—Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2, V3, and V4. Relation among output level, M and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger). Liquid crystal driver signals corresponding to the display data are output synchronized with the fall of CL1.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge trigger.
DL, DR	2	I/O	Controller	Input of serial display data (D). (D): 1 (High) — Liquid Crystal Driver Output: Selection level — Liquid Crystal Display: On (D): 0 (Low) — Liquid Crystal Driver Output: Non-selection level — Liquid Crystal Display: Off I/O status of DL and DR terminals depends on SHL input level. SHL: High — DL: O — DR: I SHL: Low — DL: I — DR: O

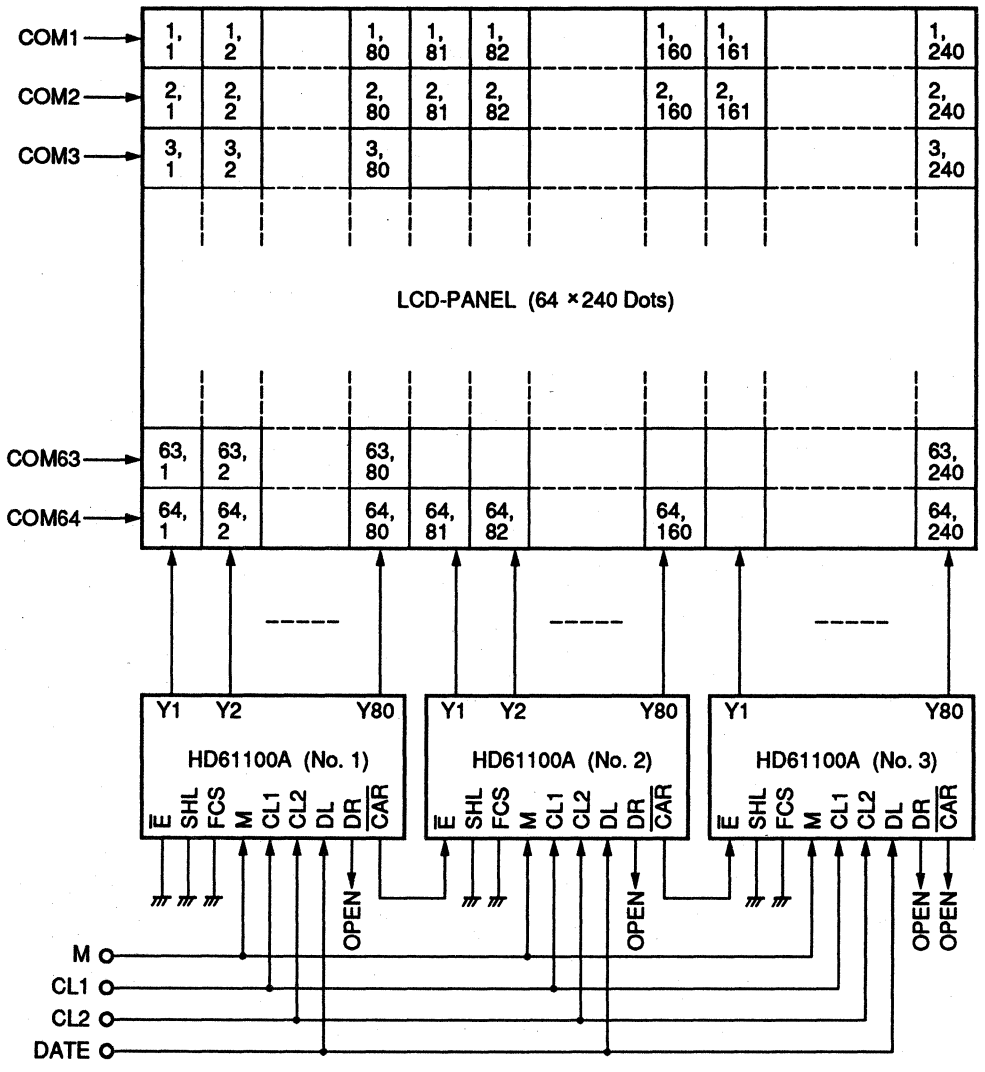
Terminal Functions Description (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
SHL	1	I	V_{CC} or GND	Selects a shift direction of serial data. When the serial data (D) is input in order of D1 → ... → D80, the relations between the data (D) and output Y are as follows. SHL: Low — Y1=D1, Y2=D2, Y3=D3, ..., Y80=D80 SHL: High — Y1=D80, Y2=D79, Y3=D78, ..., Y80=D1 When SHL is low, data is input from the terminal DL. No lines should be connected to the terminal DR, as it is in the output state. When SHL is high, the relation between DL and DR reverses.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61100A	Controls the S/P conversion. The operation stops when $\overline{E}$ is high, and the S/P conversion starts when $\overline{E}$ is low.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61100A	Used for cascade connection with the HD61100A to increase the number of bits which can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

Operation of the HD61100A

The following describes an LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61100A's. Figure 2 is a time chart of HD61100A I/O signals.

5



Cascade three HD61100As. Input data to the terminal DL of No. 1, No 2, and No. 3. Connect $\overline{E}$ of No. 1 to GND. Don't connect any lines to $\overline{CAR}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61103A. (m,n) in LCD panel is the address corresponding to each dot.

Figure 1 LCD driver with 64 × 240 dots

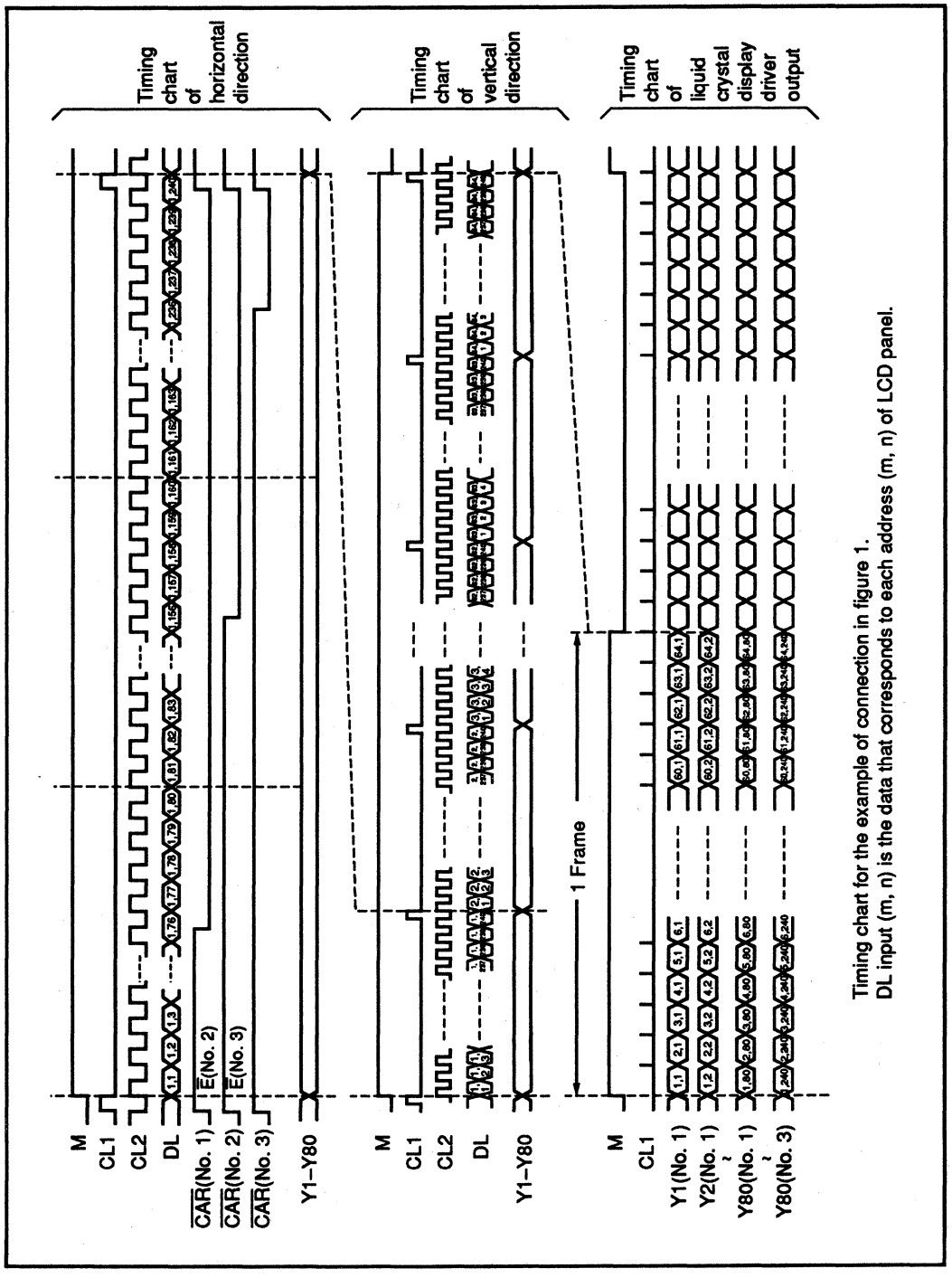


Figure 2 HD61100A Timing Chart

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Application Examples

An Example of 128 × 240 Dot Liquid Crystal Display (1/64 Duty Cycle)

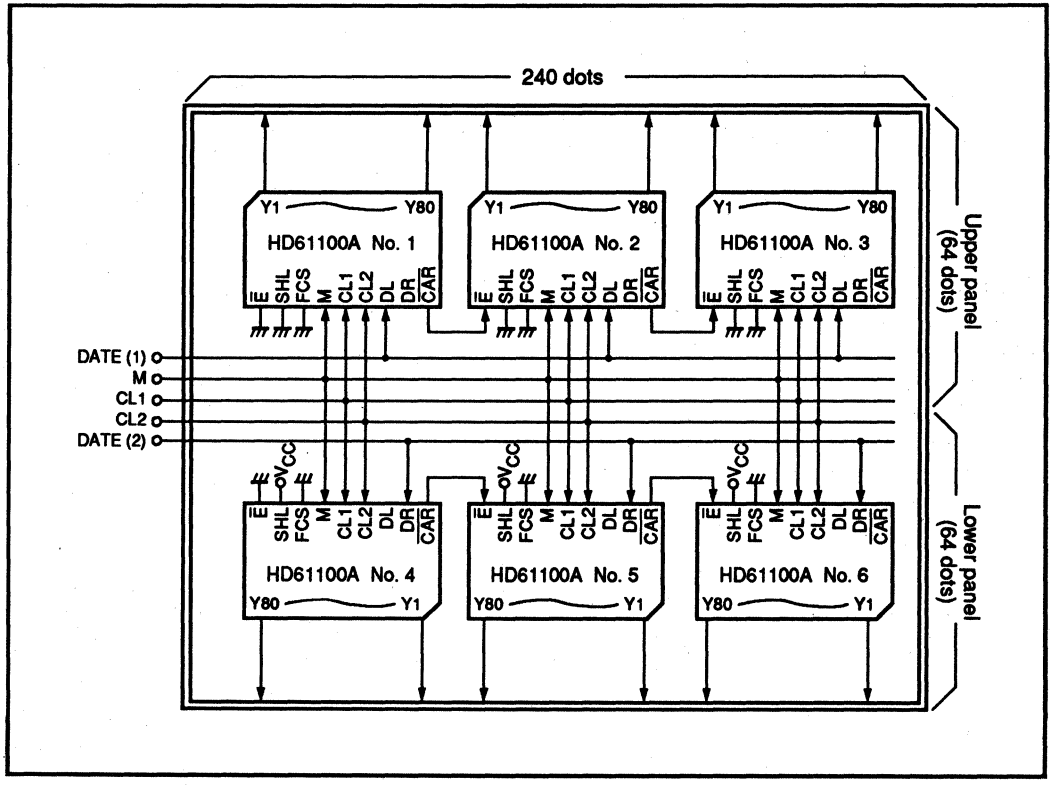


Figure 3 128 × 240 Dot Liquid Crystal Display

The liquid crystal panel (figure 3) is divided into upper and lower parts. These two parts are driven separately. HD61100As No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA(1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow \text{--} Y_{80}$ terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow \text{--} Y_{80}$ of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow \text{--} Y_{80}$ of No. 3 in the order in which they were input (in the case of SHL = low). HD61100As No. 4 to No. 6 drive the lower half. Serial data, which are input from the DATA(2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow \text{--} Y_1$ of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow \text{--} Y_1$ of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow \text{--} Y_1$ of No. 6 in the order in which they were input (in the case of SHL = high). As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

Example of 64 × 150 Dot Liquid Crystal Display (1/64 Duty Cycle, SHL = Low)

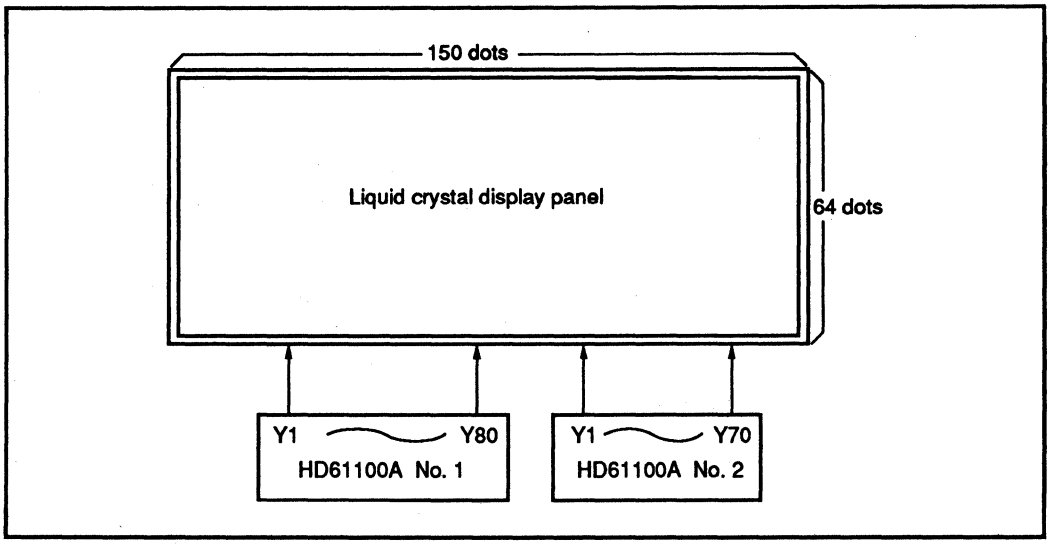


Figure 4 64 × 150 Dot Liquid Crystal Display

4-bit parallel process is used in this LSI to lessen the power dissipation.
Thus, the sum of the dots in horizontal direction should be multiple of 4.
If not, as this example (figure 4), consideration is needed for input signals (figure 5).

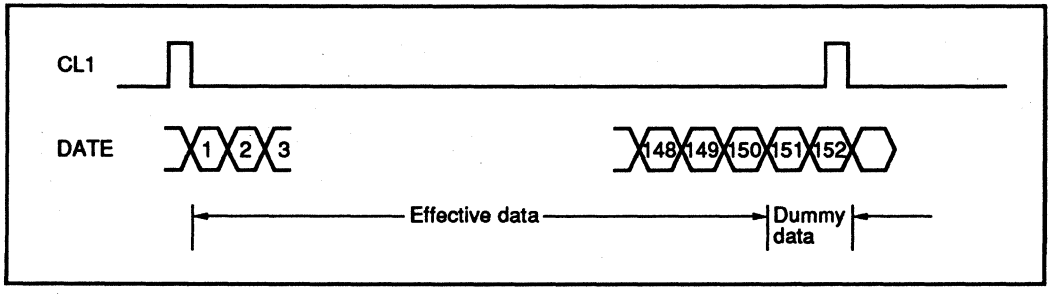


Figure 5 Input Dots, 150 Horizontal Dots

As the sum of dots in lateral direction is 150, 2 more dummy data bits are transferred (152 = 4 × 38).
Dummy data, which is output from Y71 and Y72 of No. 2, can be either 0 or 1 because these terminals do not connect with the liquid crystal display panel.

HD61102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61102 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-controller in internal display RAM and generates dot matrix liquid crystal driving signals.

Each data bit of display RAM corresponds to the on/off state of a dot of the liquid crystal display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic displays with many dots.

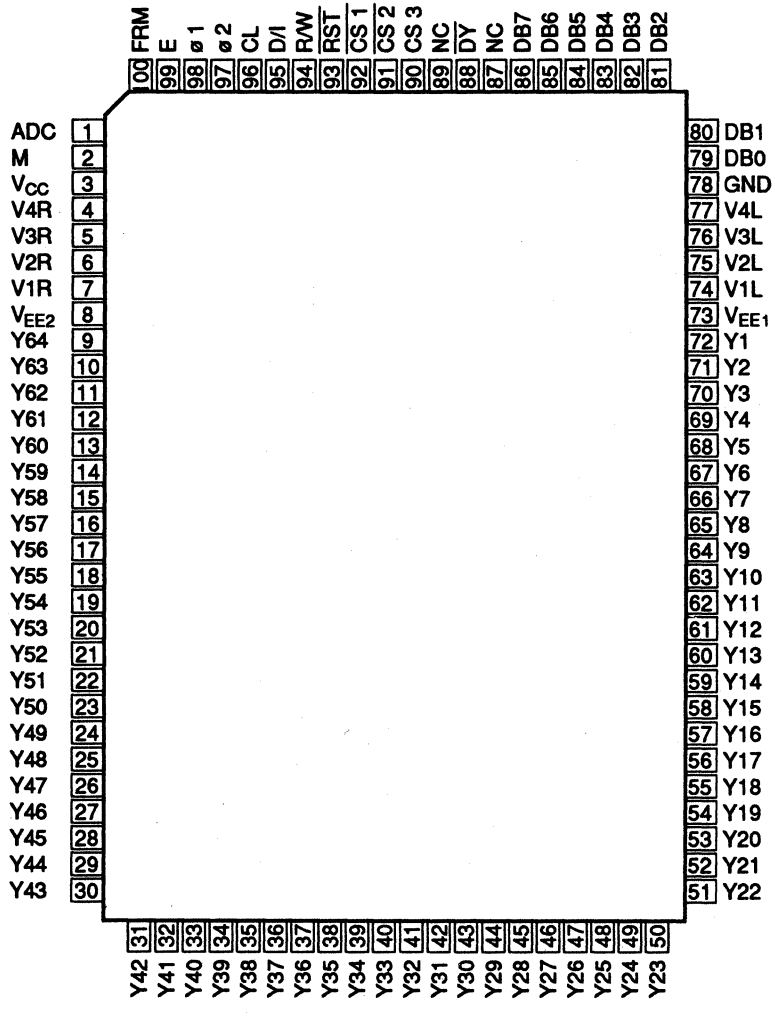
The HD61102, which is produced by the CMOS process, can complete a portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61103A.

Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
  RAM bit data 1: On
  RAM bit data 0: Off
- Internal display RAM address counter:
  Preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty:
  Combination of frame control signal and data latch synchronization signal make it possible to select static or optional duty cycle
- Wide range of instruction function:
  Display Data Read/Write, Display On/Off, Set Address, Set Display Start Line, Read Status
- Lower power dissipation: during display 2mW max
- Power supply: V_{CC}: +5 V ± 10%
  V_{EE}: 0 V to –10 V
- Liquid crystal display driving level: 15.5 V max
- CMOS process
- 100-pin flat plastic package (FP-100)

Pin Arrangement



(Top view)

5

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	– 0.3 to +7.0	V	2
	V_{EE}	V_{CC} – 16.5 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminal voltage (2)	V_{T2}	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the recommended operating conditions. Use beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
   Maintain
   $V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, $\phi1$, $\phi2$, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC, and DB0–DB7.

Electrical Characteristics

(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to −10V, Ta = −20 to +75°C)

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IHC}	0.7 × V_{CC}	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	0.3 × V_{CC}	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	IOH = −205 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	IOL = 1.6 mA	3
Input leakage current	I_{IL}	−1.0	—	+1.0	µA	Vin = GND–V_{CC}	4
High impedance off input current	I_{TSL}	−5.0	—	+5.0	µA	Vin = GND–V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	−2.0	—	+2.0	µA	Vin = V_{EE}–V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	KΩ	V_{CC} − V_{EE} = 15 V ±I_{LOAD} = 0.1 mA	7
Dissipation current	$I_{CC(1)}$	—	—	100	µA	During display	8
	$I_{CC(2)}$	—	—	500	µA	During access: Access cycle = 1 MHz	8

Notes:
1. Applies to M, FRM, CL, $\overline{RST}$, ADC, φ1, and φ2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L—V4L and V1R–V4R.
7. Applies to Y1–Y64.
8. Specified when liquid crystal display is in 1/64 duty.
   Operation frequency: f_{CLK} = 250 kHz (φ1 and φ2 frequency)
   Frame frequency: f_M = 70 Hz (FRM frequency)
   Specified in the state of
   Output terminal: Not loaded
   Input level: $V_{IH} = V_{CC}$ (V)
   V_{IL} = GND (V)
   Measured at V_{CC} terminal

5

Interface AC Characteristics

MPU Interface

(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	—	—	ns	1, 2
E high level width	P_{WEH}	450	—	—	ns	1, 2
E low level width	P_{WEL}	450	—	—	ns	1, 2
E rise time	tr	—	—	25	ns	1, 2
E fall time	tf	—	—	25	ns	1, 2
Address setup time	t_{AS}	140	—	—	ns	1, 2
Address hold time	t_{AH}	10	—	—	ns	1, 2
Data setup time	t_{DSW}	200	—	—	ns	1
Data delay time	t_{DDR}	—	—	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	—	—	ns	1
Data hold time (Read)	t_{DHR}	20	—	—	ns	2

Notes: 1.

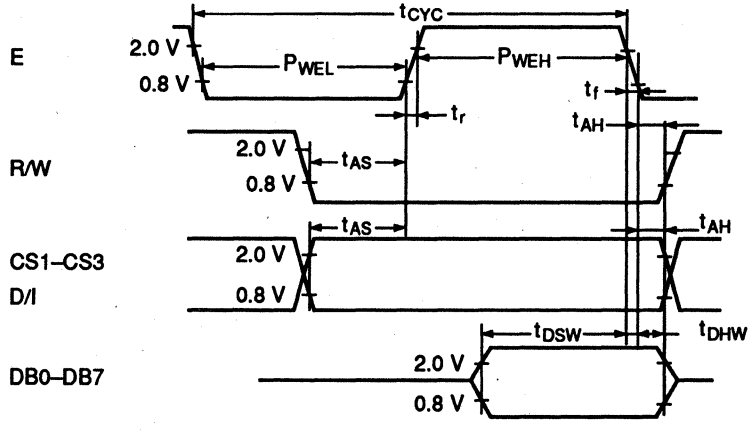


Figure 1 CPU Write Timing

2.

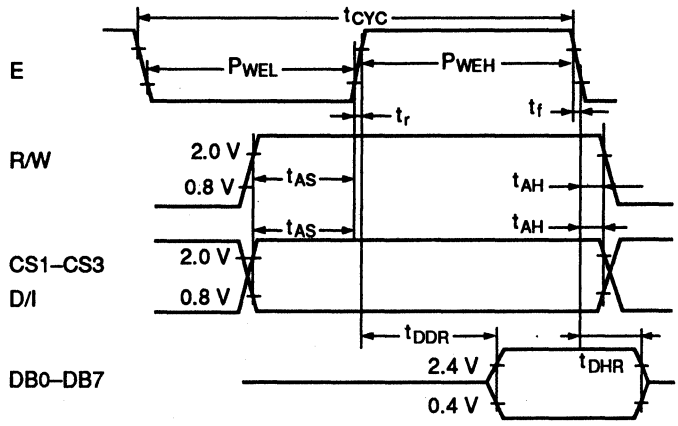
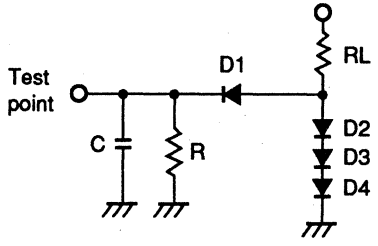


Figure 2 CPU Read Timing

3. DB0–DB7: load circuit



RL = 2.4 kΩ
R = 11 kΩ
C = 130 pF (including jig capacitance)
Diodes D1 to D4 are all IS2074 Ⓗ.

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Clock Timing
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to −10V, Ta = −20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
φ1, φ2 cycle time	tcyc	2.5	—	20	μs	Fig. 3
φ1 low level width	$t_{WL\phi1}$	625	—	—	ns	Fig. 3
φ2 low level width	$t_{WL\phi2}$	625	—	—	ns	Fig. 3
φ1 high level width	$t_{WH\phi1}$	1875	—	—	ns	Fig. 3
φ2 high level width	$t_{WH\phi2}$	1875	—	—	ns	Fig. 3
φ1–φ2 phase difference	t_{D12}	625	—	—	ns	Fig. 3
φ2–φ1 phase difference	t_{D21}	625	—	—	ns	Fig. 3
φ1, φ2 rise time	tr	—	—	150	ns	Fig. 3
φ1, φ2 fall time	tf	—	—	150	ns	Fig. 3

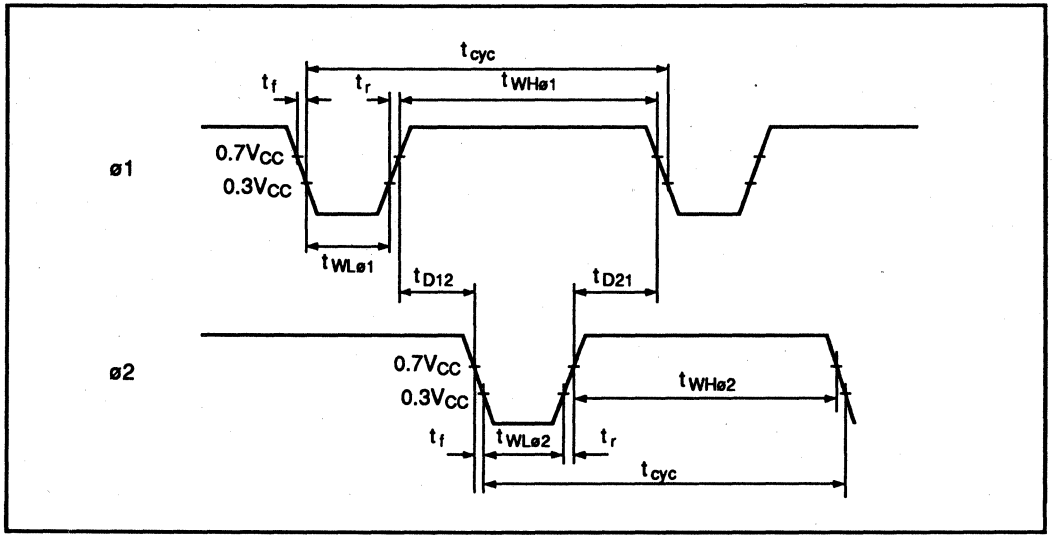

Figure 3 External Clock Waveform

Display Control Timing
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to −10V, Ta = −20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
FRM delay time	t_{DFRM}	−2	—	+2	µs	Fig. 4
M delay time	t_{DM}	−2	—	+2	µs	Fig. 4
CL low level width	t_{WLCL}	35	—	—	µs	Fig. 4
CL high level width	t_{WHCL}	35	—	—	µs	Fig. 4

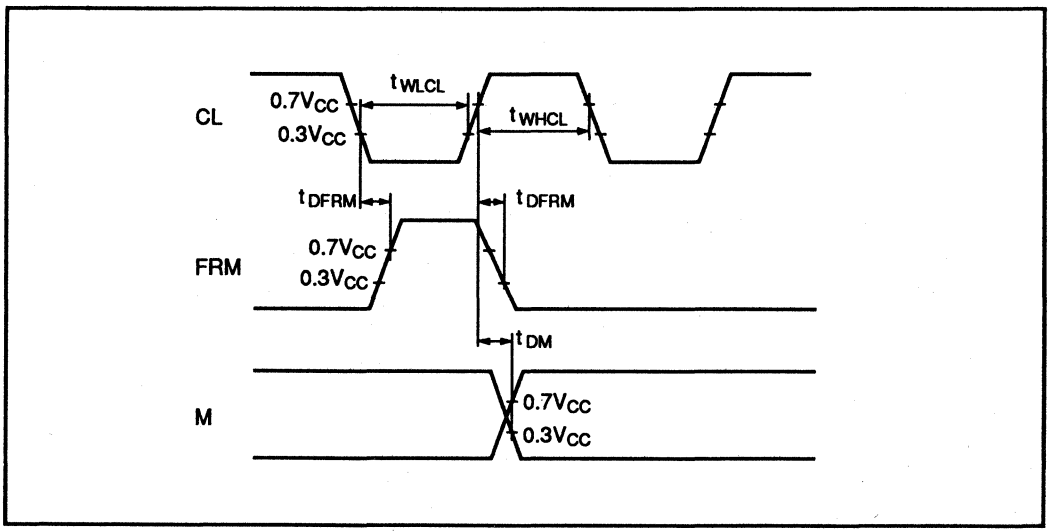

Figure 4 Display Control Signal Waveform

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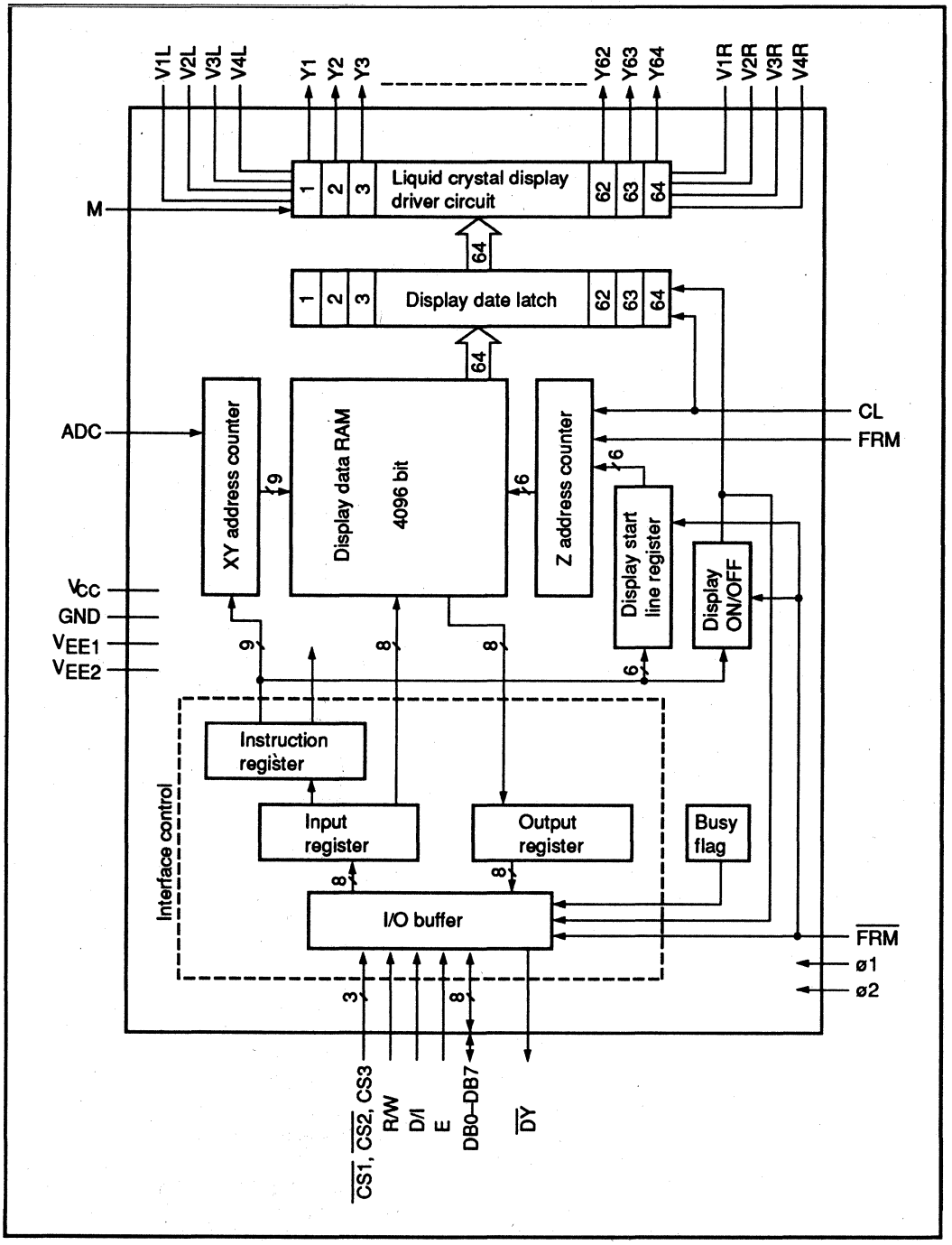
Block Diagram

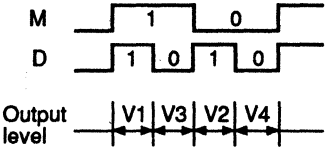


Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is GND = 0 V V_{CC} = +5 V ± 10%
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is V_{CC} −15 to GND. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected to each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified for the liquid crystals within the limit of V_{EE} through V_{CC}. VIL (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal name: $\overline{CS1}$ $\overline{CS2}$ CS3 Condition: L L H
E	1	I	MPU	Enable At write(R/W = low): Data of DB0 to DB7 is latched at the fall of E. At read(R/W = high): Data appears at DB0 to DB7 while E is high.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the CPU when E = high, $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high. R/W = Low: DB0 to DB7 accepted at fall of E when $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high.
D/I	1	I	MPU	Data/Instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.
ADC	1	I	V_{CC}/GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1–$0, Y64–$63 ADC = Low: Y64–$0, Y1–$63

5

Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
DB0–DB7	8	I/O	MPU	Data bus, three-state I/O common terminal.
M	1	I	HD61103A	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61103A	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61103A	Synchronous signal to latch display data. The rising edge of the CL signal increments the display output address counter and latches the display data.
ϕ1, ϕ2	1	I	HD61103A	2-phase clock signal for internal operation. The ϕ1 and ϕ2 clocks are used to perform operations (I/O of display data and execution of instructions) other than display.
Y1-Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins output light on level when 1 is in the display RAM, and light off level when 0 is in it. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level: 1. On/off register set to 0 (display off) 2. Display start line register set to line 0 (displays from line 0) After releasing reset, this condition can be changed only by instruction.
$\overline{DY}$	1	O	Open	Output terminal for test. Normally, don't connect any lines to this terminal.
NC	2		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

1. I/O buffer

Data is transferred through 8 data buses (DB0-DB7).

DB7: MSB (most significant bit)
DB0: LSB (least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

2. Register

Both input register and output register are provided to interface to MPU whose the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

a. Input Register

The input register is used to store data temporarily before writing it into display data RAM. The data from MPU is written into input register, then into display data RAM automatically by internal operation.

When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of E signal.

b. Output Register

The output register is used to store data temporarily that is read from display data RAM. To read out the data from the output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. The read display data instruction outputs data stored in the output register while E is high. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1. The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 5 shows the CPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register).
1	0	Writes data into input register as internal operation (input register → display data RAM).
0	1	Busy check. Read of status data.
0	0	Instruction.

5

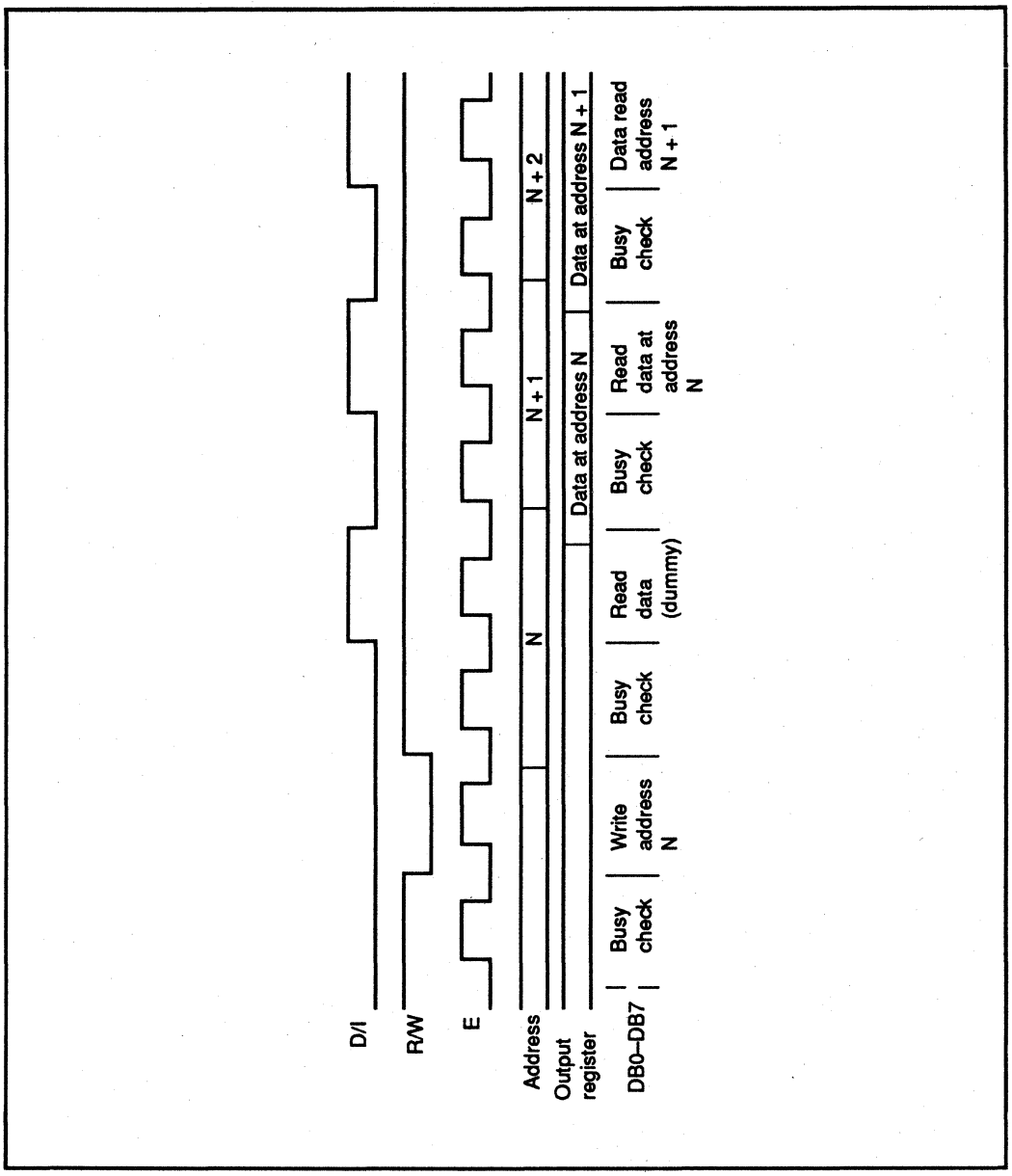


Figure 5 CPU Read Timing

Busy Flag

Busy flag = 1 indicates that HD61102 is operating and no instructions except status read can be accepted (figure 6). The value of the busy flag is read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset (0) before issuing an instruction.

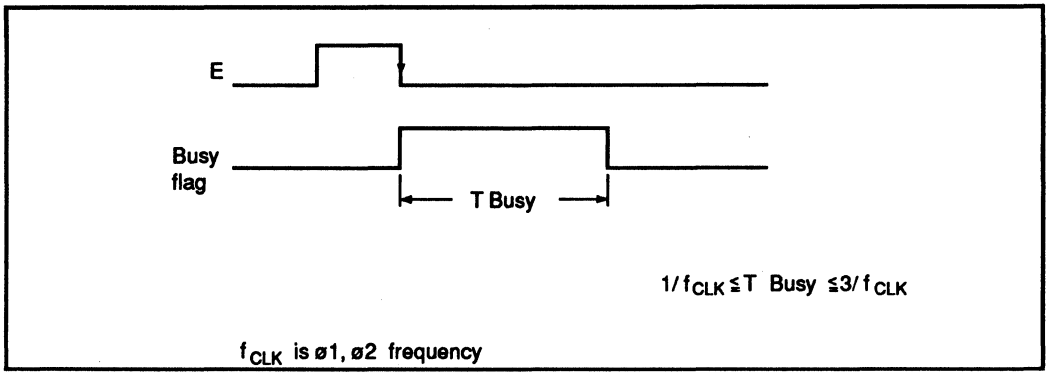


Figure 6 Busy Flag

Display On/Off Flip/Flop

The display On/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by the display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by the status read instruction. The display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, Cl signal (display synchronous signal) should be input correctly.

Display Start Line Register

The register specifies a line in RAM that corresponds to the top line of the LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling the screen.

6-bit display start line information is written into this register by the display start line set instruction, with high level of FRM signal signalling the start of the display, the information in this register is transferred to the Z address counter, which controls the display address, and the Z address counter is preset.

X, Y Address Counter

A 9-bit counter that designates addresses of internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set by the respective instructions.

1. X address counter
Ordinary register with no count functions. An address is set by instruction.

2. Y address counter
An address is set by instruction and it is increased by 1 automatically by display data R/W operations. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.

As the ADC signal controls the Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, always connect ADC pin to V_{CC} or GND when using.

Figure 7 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

5

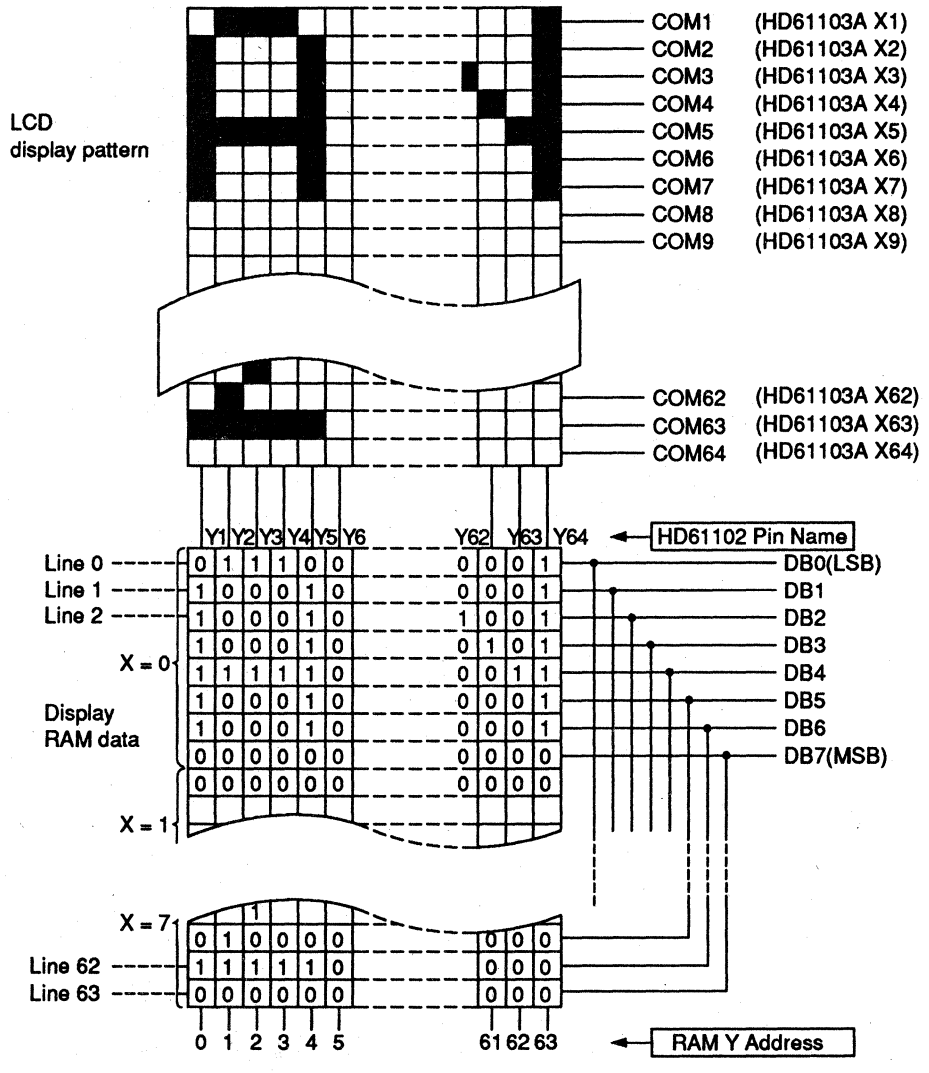


Figure 7 Relation between RAM Data and Display

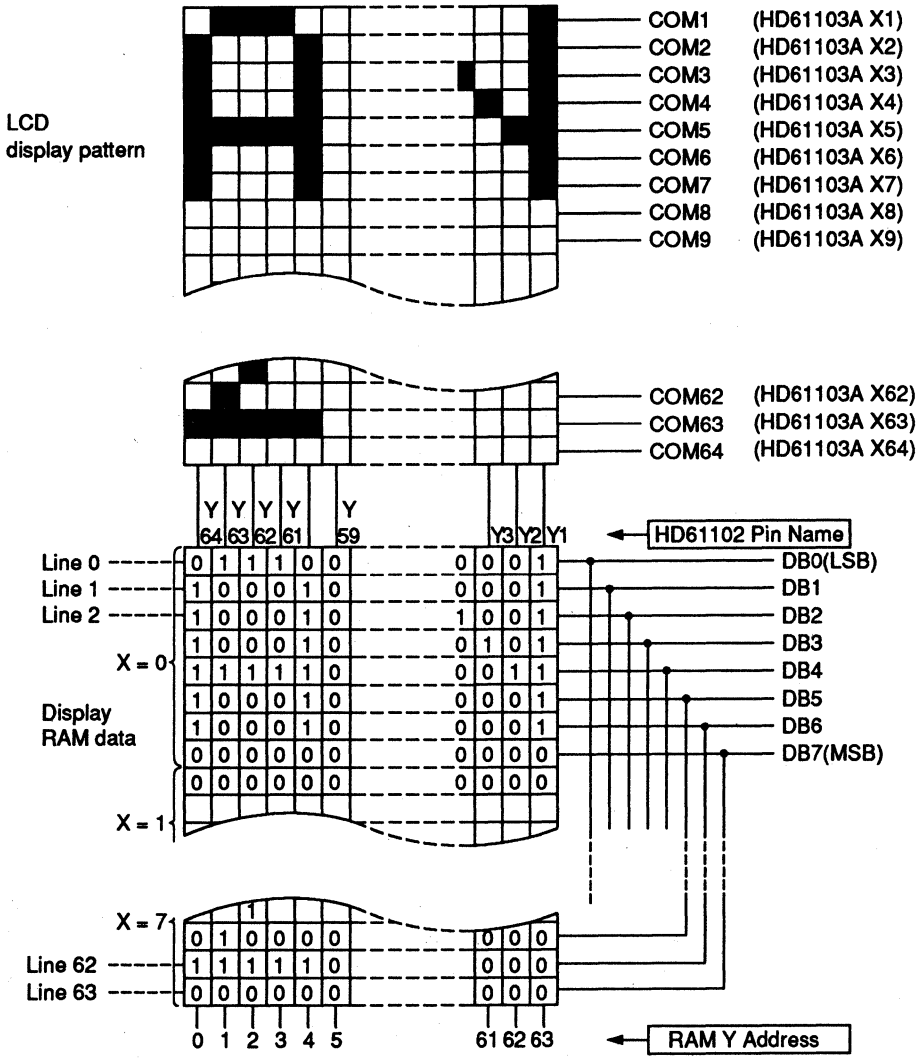


Figure 7 Relation between RAM Data and Display (cont)

5

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At FRM high, the contents of the display start line register are preset in the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit.

Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal to low when turning power on.

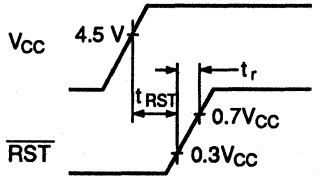
1. **Display off**
2. **Set display start line register line 0**

While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, carry out other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (ready) by status read instruction.
The conditions of the power supply at initial power up are as in table 2.

Table 2 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 3 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.
These explanations are detailed in the following pages. Generally, there are the following three kinds of instructions.

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction are used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than the status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is the proof that an instruction is not being excuted.

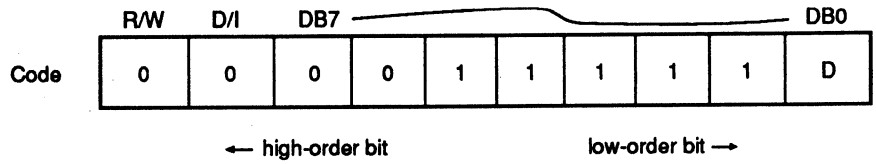
Table 3 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM in the page (X address) register.
Set Y address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.
Status read	1	0	Busy	0	ON/OFF	RESET	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Executing internal operation 0: Ready
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM. Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: 1. Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

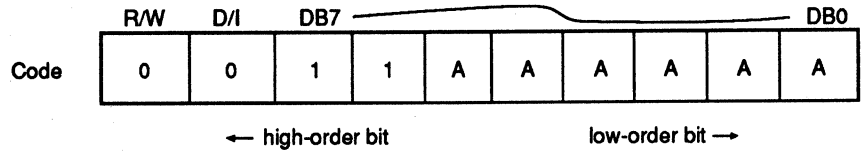
Detailed Explanation

1. Display on/off



The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen when D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

2. Display start line



Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen.
Figure 7 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

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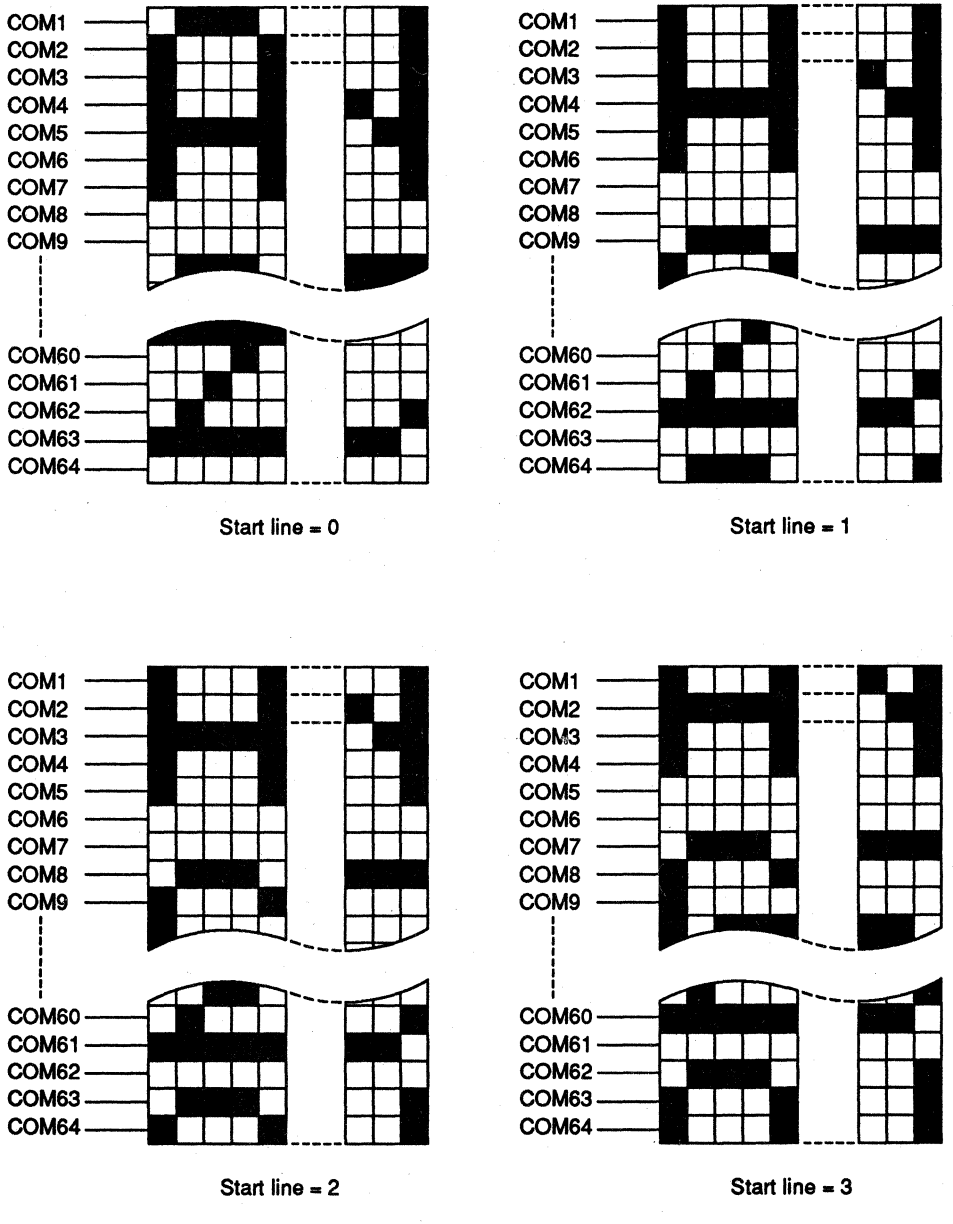

Figure 7 Relation Between Start Line and Display

3. Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order bit low-order bit →

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 8.

4. Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order bit low-order bit →

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

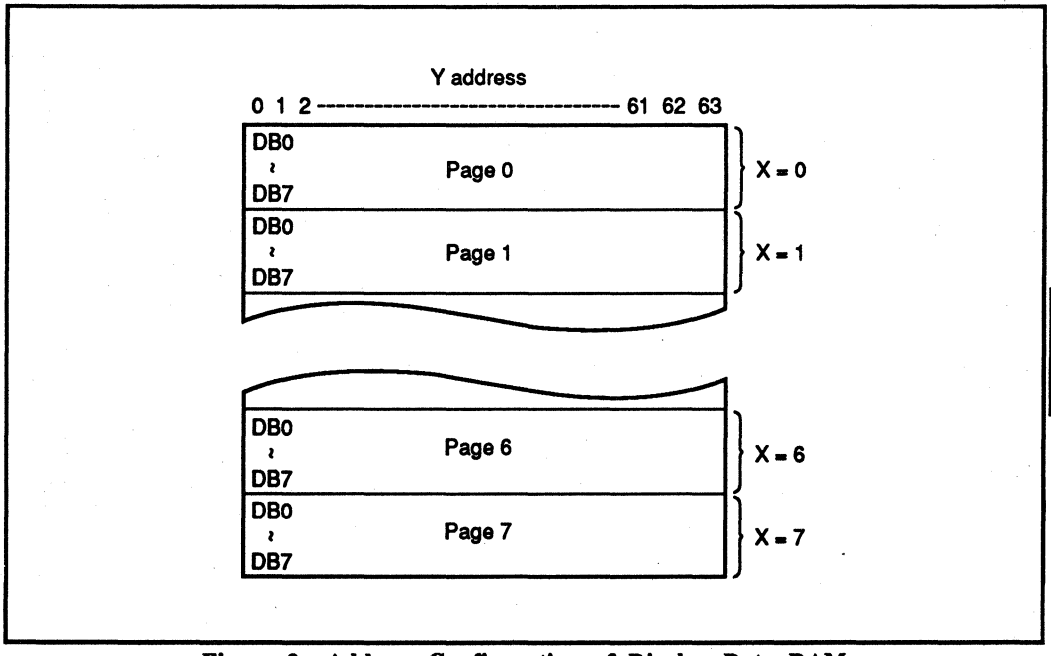

Figure 8 Address Configuration of Display Data RAM

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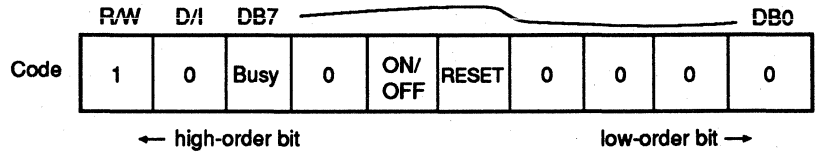
5. Status Read

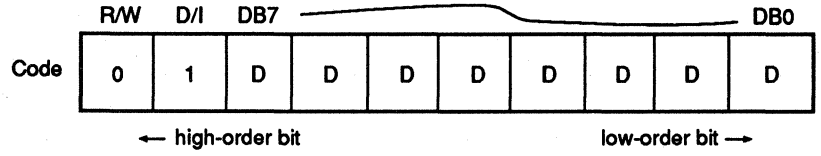


Busy: When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

ON/OFF: Shows the liquid crystal display conditions: on condition or off condition.
When ON/OFF is 1, the display is in off condition.
When ON/OFF is 0, the display is in on condition.

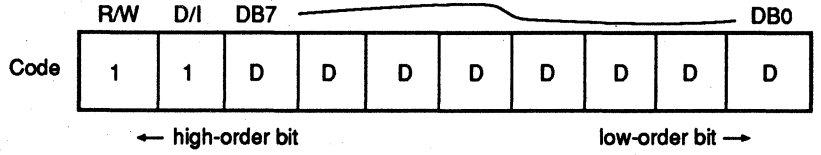
RESET: RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

6. Write Display Data



Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

7. Read Display Data

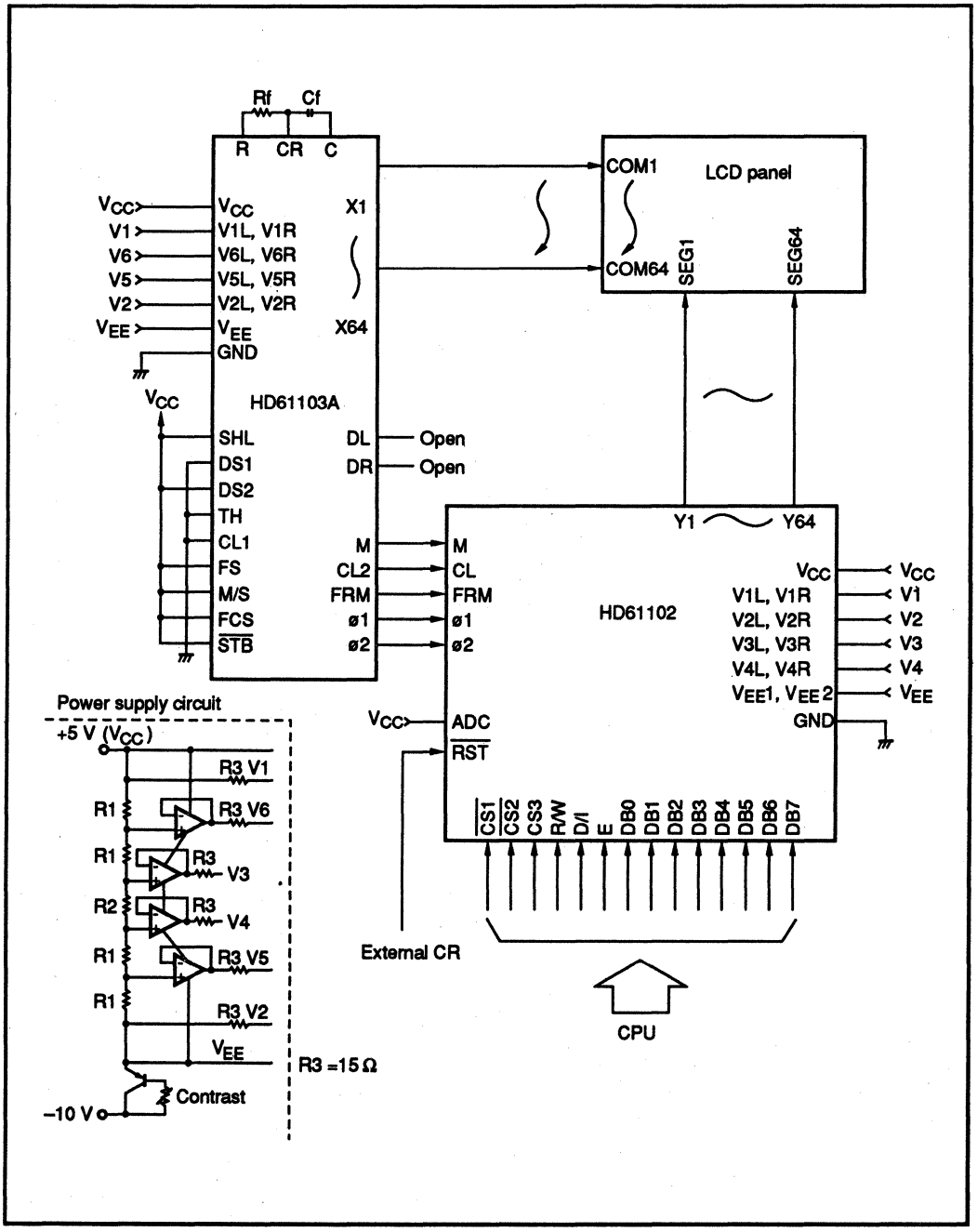


Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

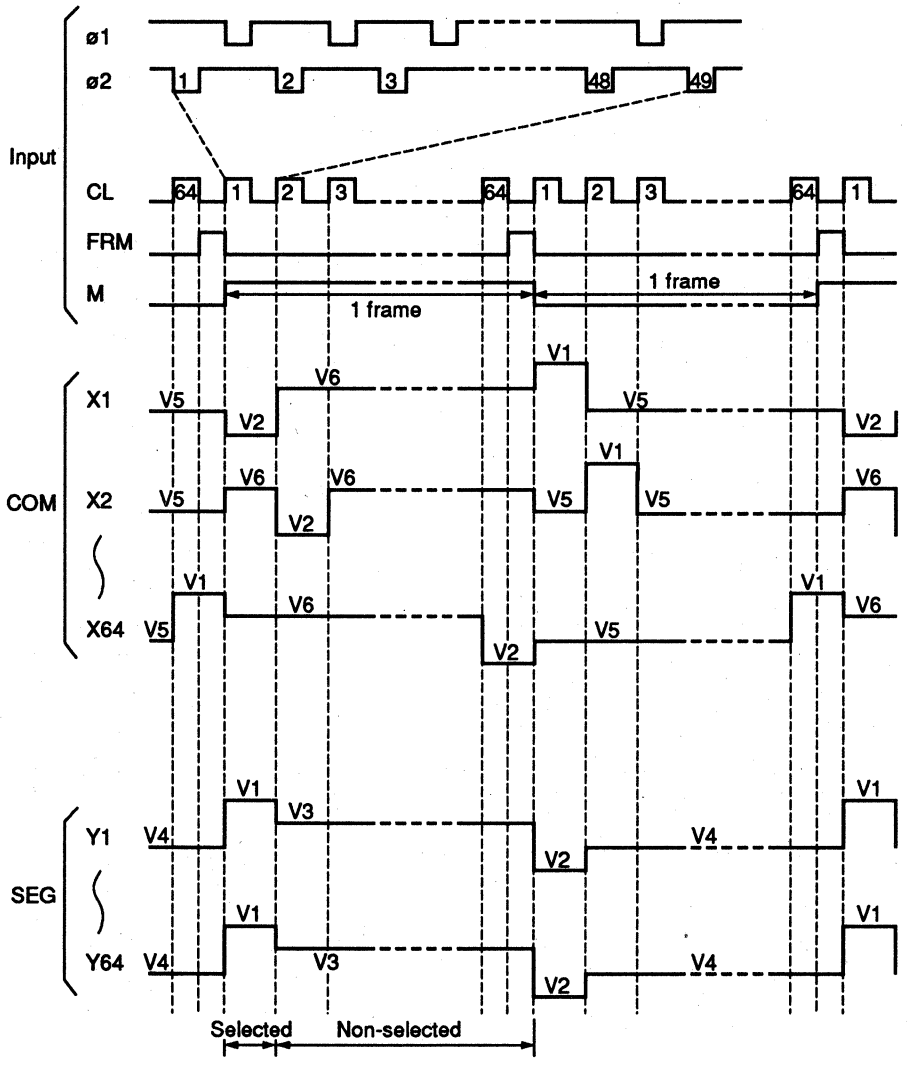
One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

Use of HD61102

Interface with HD61103A (1/64 duty cycle)



5



The waveforms of Y1 to Y64 outputs vary with the display date. In this example, the top line of the panel lights up and other dots do not.

Figure 9 LCD Driver Timing Chart (1/64 duty cycle)

Interface with CPU

1. Example of connection with HD6800

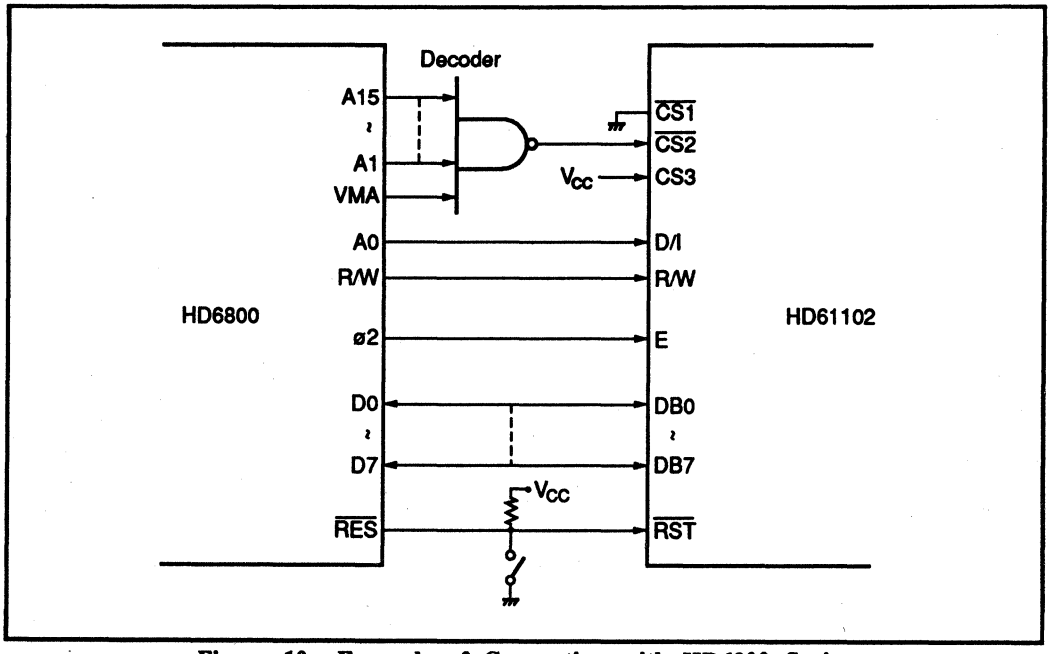


Figure 10 Example of Connection with HD6800 Series

In this decoder (figure 10), addresses of HD61102 in the address area of HD6800 are:

Read/write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control HD61102 by reading/writing the data at these addresses.

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2. Example of connection with HD6801

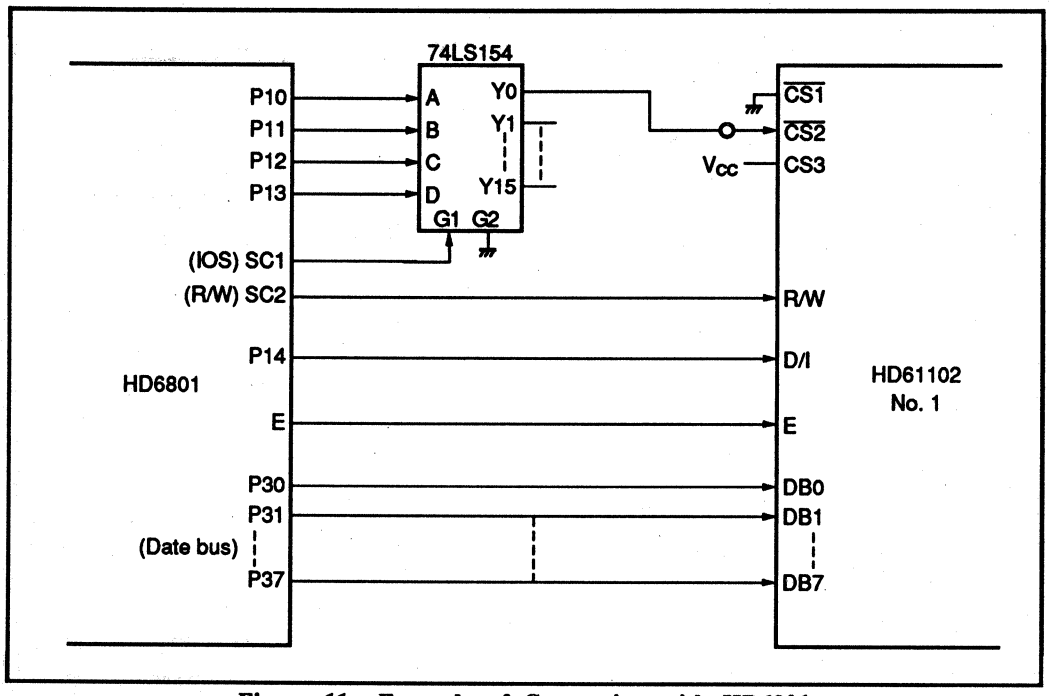


Figure 11 Example of Connection with HD6801

- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus (table 11).
- 74LS154 4–to–16 decoder generates chip select signal to make specified HD61102 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61102. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

Example of Application

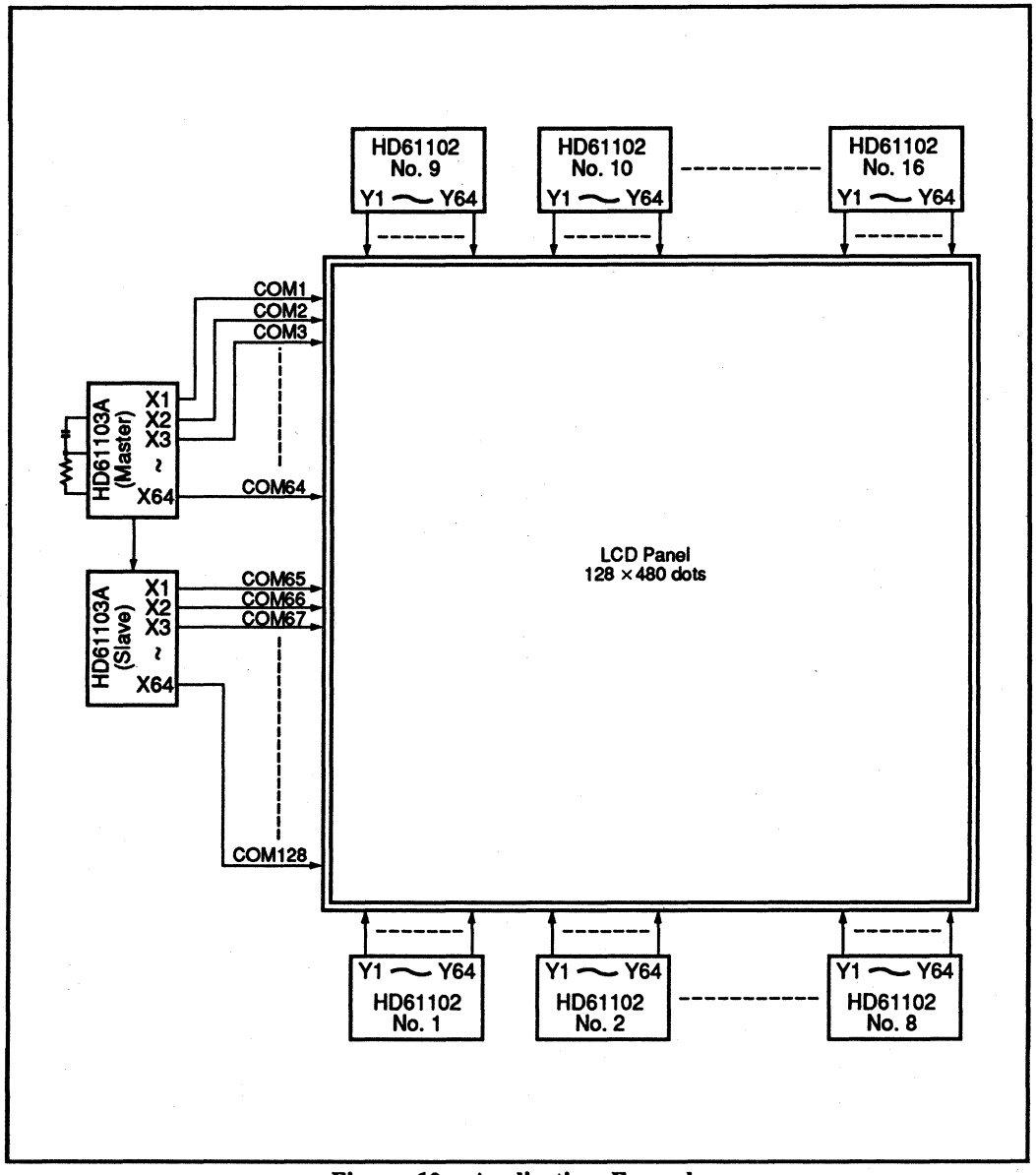


Figure 12 Application Example

Note: In this example (figure 12), two HD61103As output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

5

HD61103A
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD61103A is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61103A is produced by a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61103A and the column (segment) driver HD61102.

Features

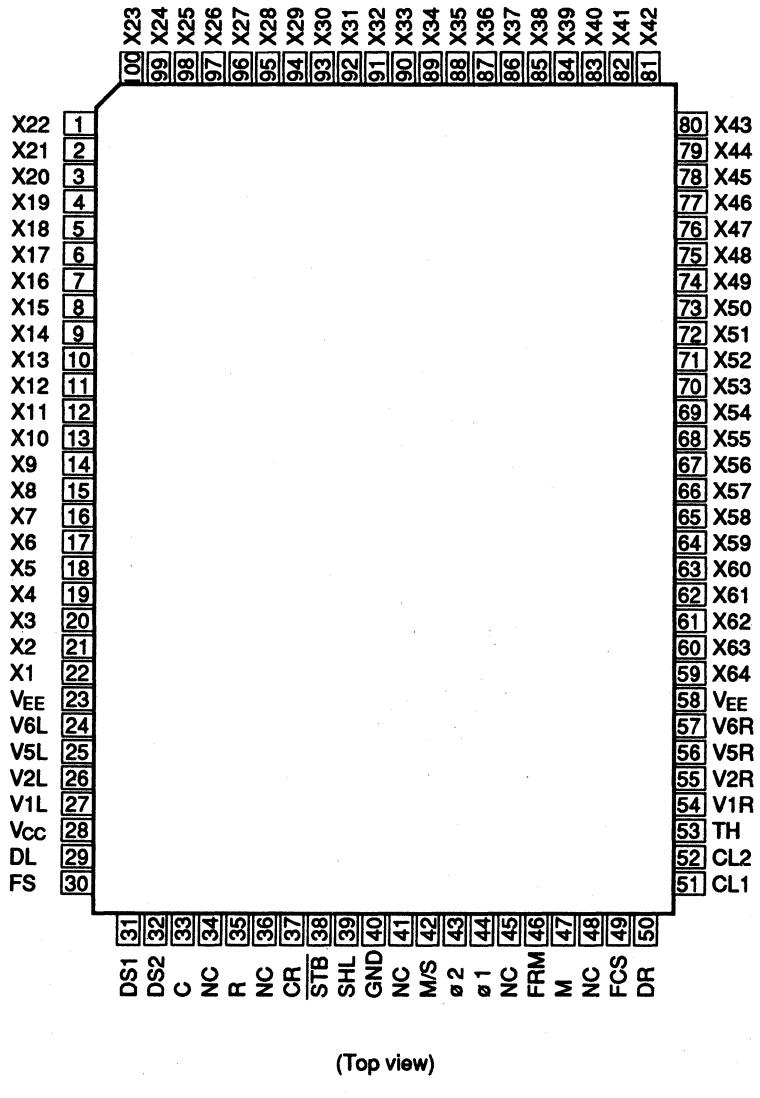
- Dot matrix liquid crystal graphic display common driver with low impedance
- Low impedance: 1.5 kΩ max
- Internal liquid crystal display driver circuit: 64 circuits
- Internal dynamic display timing generator circuit
- Selectable display duty ratio factor 1/48, 1/64, 1/96, 1/128
- Can be used as a column driver transferring data serially
- Low power dissipation: During display: 5 mW
- Power supplies: V_{CC}: +5 V ± 10%
  V_{EE}: 0 to −11.5 V
- LCD driver level: 17.0 V max
- CMOS process
- 100-pin flat plastic package (FP-100)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power supply voltage (1)	V_{CC}	−0.3 to +7.0	V	2
Power supply voltage (2)	V_{EE}	V_{CC} −19.0 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	−0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} − 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to 125	°C	

Notes: 1. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.
2. Based on GND = 0 V.
3. Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) and I/O common terminals at high impedance.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
5. Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.
Maintain $V_{CC} \geq V1L = V1R \geq V6L = V6R \geq V5L = V5R \geq V2L = V2R \geq V_{EE}$

Pin Arrangement



(Top view)

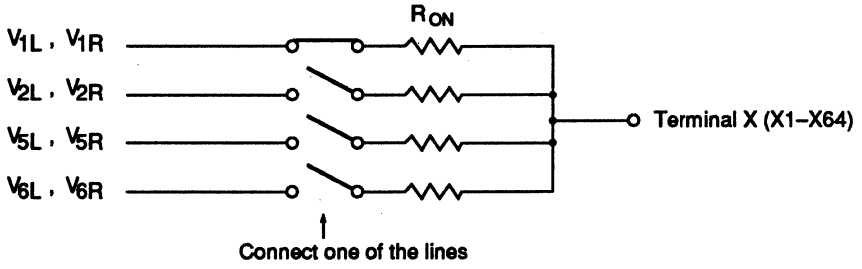
5

Electrical Characteristics

DC Characteristics (V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to −11.5 V, Ta = −20 to +75°C)

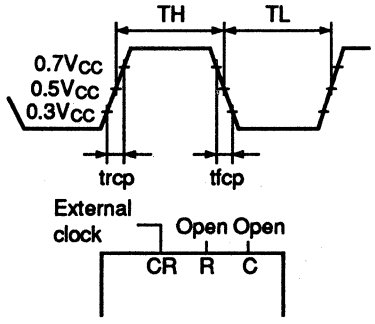
		Specifications					
Test Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Note**
Input high voltage	V_{IH}	0.7 × VCC	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} − 0.4	—	—	V	I_{OH} = −0.4 mA	2
Output low voltage	V_{OL}	—	—	+0.4	V	I_{OI} = +0.4 mA	2
Vi-Xj on resistance	R_{ON}	—	—	1.5	kΩ	V_{CC} − V_{EE} = 10 V Load current ±150 µA	3
Input leakage current	I_{IL1}	−1.0	—	+1.0	µA	Vin = 0 to V_{CC}	4
Input leakage current	I_{IL2}	−2.0	—	+2.0	µA	Vin = V_{EE} to V_{CC}	5
Operating frequency	fopr1	50	—	600	kHz	In master mode External clock operation	6
Operating frequency	fopr2	50	—	1500	kHz	In slave mode Shift register	7
Oscillation frequency	fosc	315	450	585	kHz	Cf = 20 pF ± 5% Rf = 47 kΩ ± 2%	8, 13
Dissipation current (1)	I_{GG1}	—	—	1.0	mA	In master mode 1/128 duty cycle Cf = 20 pF Rf = 47 kΩ	9, 10
Dissipation current (2)	I_{GG2}	—	—	200	µA	In slave mode 1/128 duty cycle	9, 11
Dissipation current	I_{EE}	—	—	100	µA	In master mode 1/128 duty cycle	9, 12

Notes:
1. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH and I/O common terminals DL, M, DR and CL2 in the input state.
2. Applies to output terminals, φ1, φ2, and FRM and I/O common terminals DL, M, DR, and CL2 in the output status.
3. Resistance value between terminal X (one of X1 to X64) and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) when load current is applied to each terminal X. Equivalent circuit between terminal X and terminal V.



4. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH, I/O common terminals DL, M, DR and CL2 in the input status and NC terminals.
5. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
   Don't connect any lines to X1 to X64.
6. External clock is as follows.

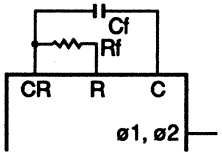
External clock waveform



$$\text{Duty cycle} = \frac{TH}{TH + TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
trcp	–	–	50	ns
tfcp	–	–	50	ns

7. Applies to the shift register in the slave mode. For details, refer to AC Characteristics.
8. Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency ($f\phi$) at $\phi 1$ or $\phi 2$.



Cf = 20 pF
Rf = 47 kΩ fosc = 2 × fø

9. No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH} = V_{CC}$ and $V_{IL} = GND$.
10. This value is specified for current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$, and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in note 8.
11. This value is specified for current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS and CR is connected to V_{CC}, CL1, TH, and M/S to GND and the terminals CL2, M, and DL are respectively connected to terminals CL2, M, and DL of the HD61103A under the conditions described in note 10.

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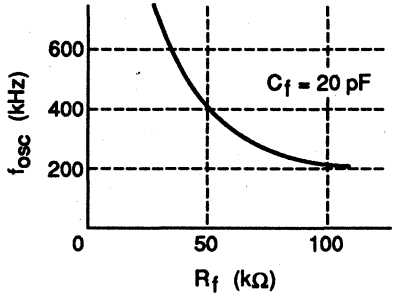
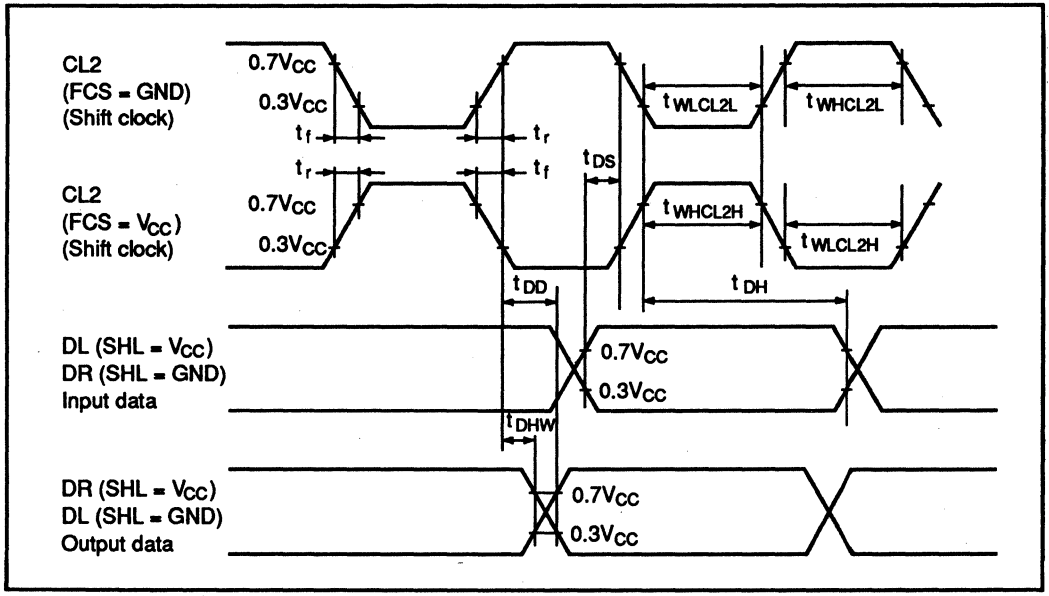
12. This value is specified for current flowing through V_{EE} under the condition described in note 10. Don't connect any lines to terminal V.
13. This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting conditions.



AC Characteristics

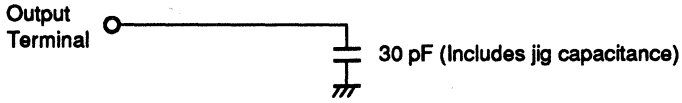
(V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to −11.5 V, Ta = −20 to +75°C)

1. Slave Mode (M/S = GND)



Item	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width (FCS = GND)	t_{WLCL2L}	450	—	—	ns	
CL2 high level width (FCS = GND)	t_{WHCL2L}	150	—	—	ns	
CL2 low level width (FCS = V_{CC})	t_{WLCL2H}	150	—	—	ns	
CL2 high level width (FCS = V_{CC})	t_{WHCL2H}	450	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	100	—	—	ns	
Data delay time	t_{DD}	—	—	200	ns	1
Data hold time	t_{DHW}	10	—	—	ns	
CL2 rise time	tr	—	—	30	ns	
CL2 fall time	tf	—	—	30	ns	

Note: 1. The following load circuit is connected for specification.



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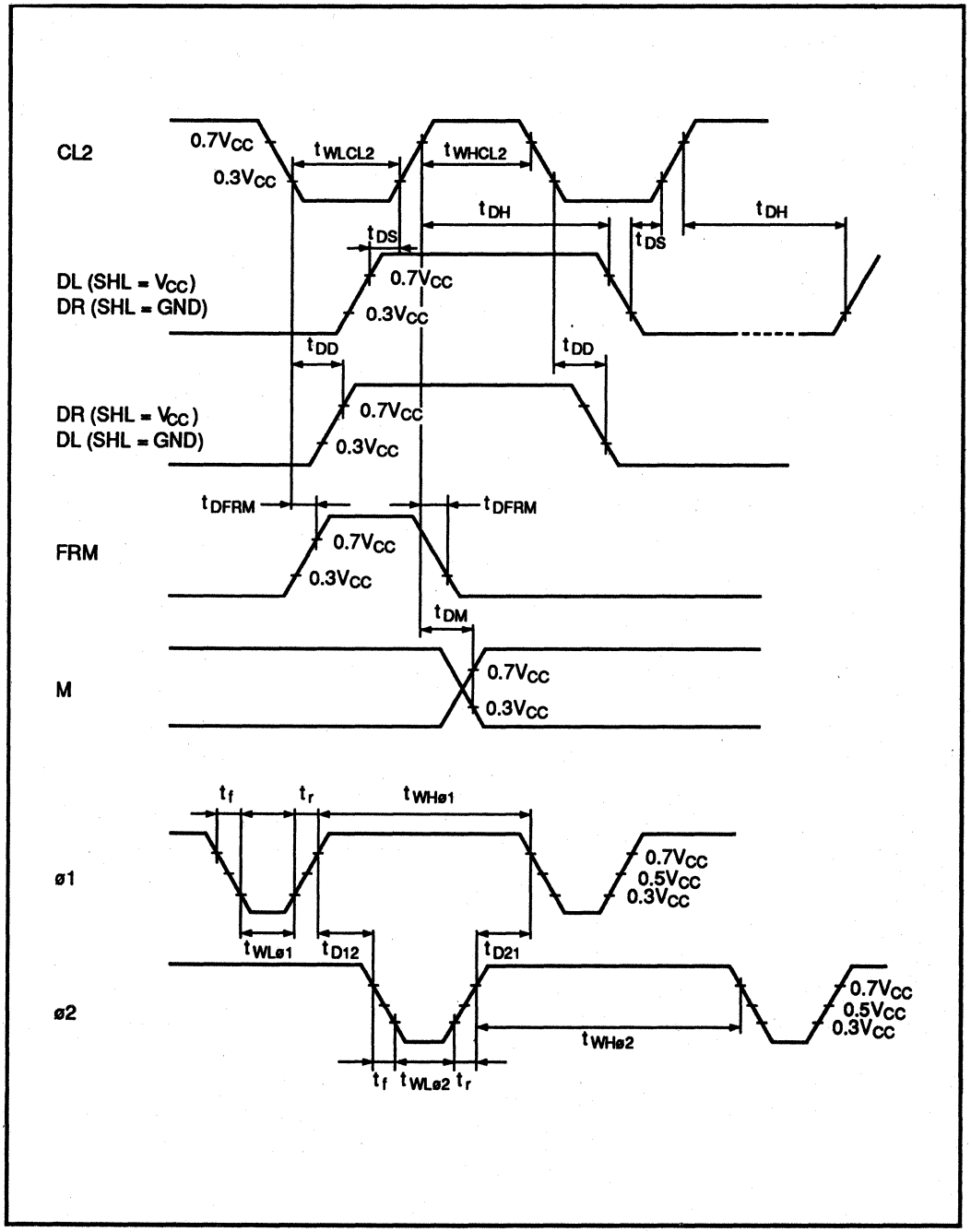
2. Master Mode (M/S = V_{CC}, FCS = V_{CC}, Cf = 20 pF, Rf = 47 kΩ)



Item	Symbol	Min	Typ	Max	Unit	Note
Data setup time	t_{DS}	20	—	—	µs	
Data hold time	t_{DH}	40	—	—	µs	
Data delay time	t_{DD}	5	—	—	µs	
FRM delay time	t_{DFRM}	–2	—	+2	µs	
M delay time	t_{DM}	–2	—	+2	µs	
CL_2 low level width	t_{WLCL2}	35	—	—	µs	
CL_2 high level width	t_{WHCL2}	35	—	—	µs	
ϕ1 low level width	$t_{WL\phi1}$	700	—	—	ns	
ϕ2 low level width	$t_{WL\phi2}$	700	—	—	ns	
ϕ1 high level width	$t_{WH\phi1}$	2100	—	—	ns	
ϕ2 high level width	$t_{WH\phi2}$	2100	—	—	ns	
ϕ1– ϕ2 phase difference	t_{D12}	700	—	—	ns	
ϕ2– ϕ1 phase difference	t_{D21}	700	—	—	ns	
ϕ1, ϕ2 rise time	tr	—	—	150	ns	
ϕ1, ϕ2 fall time	tf	—	—	150	ns	

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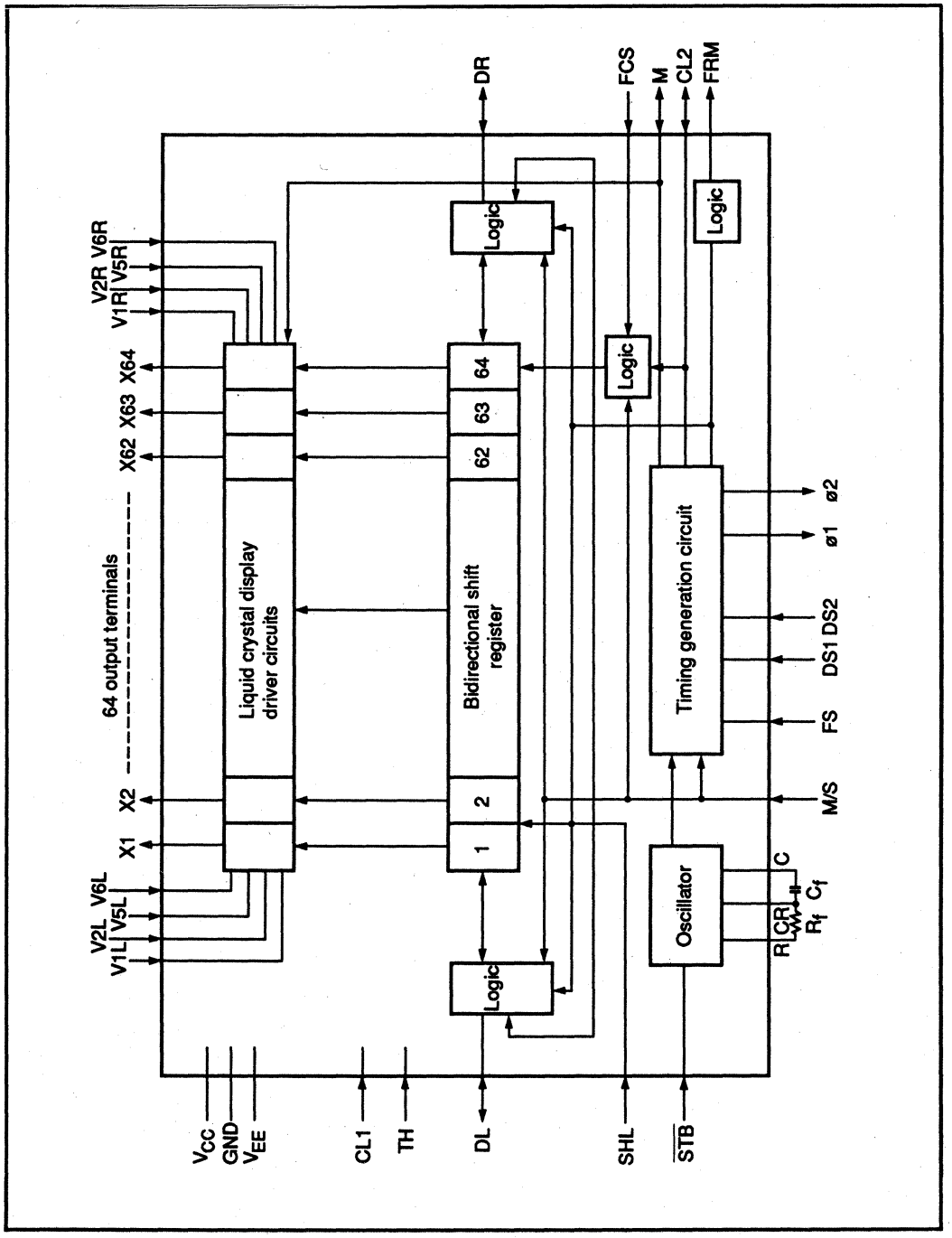
Block Diagram



Block Functions

Oscillator

The CR oscillator generates display timing signals and operating clocks for the HD61102. It is required when the HD61103A is used with the HD61102. An oscillation resistor Rf and an oscillation capacitor Cf are attached as shown in figure 1 and terminal $\overline{STB}$ is connected to the high level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminal R and C.

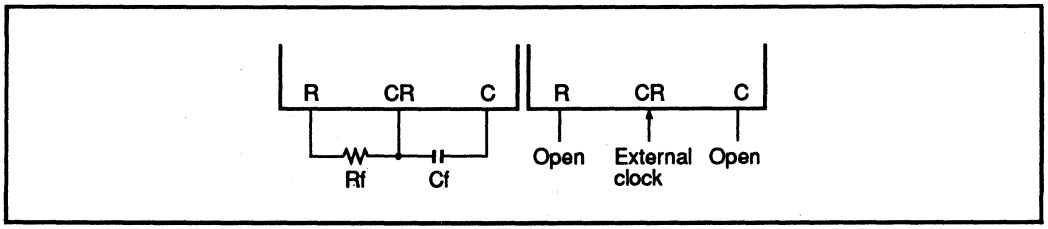


Figure 1 Oscillator Connection with HD61102

The oscillator is not required when the HD61103A is used with the HD61830. Connect terminal CR to the high level and don't connect any lines to terminals R and C (figure 2).

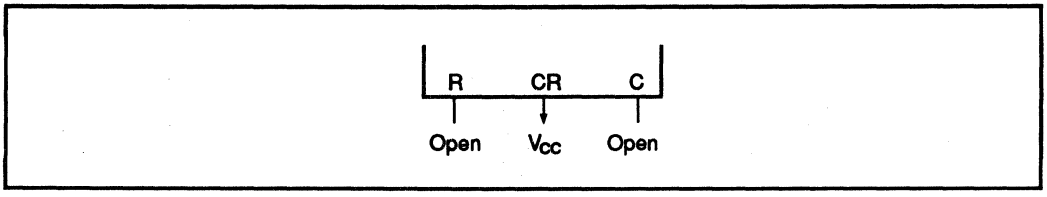


Figure 2 Oscillator Connection with HD61830

Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61102. This circuit is required when the HD61103A is used with the HD61102. Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals FS, DS1, and DS2 to high level and M/S to low level (slave mode).

Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the DL side, corresponds to X1 and the highest order bit on the DR side corresponds to X64.

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals (table 1).

Table 1 Output Levels

Data from the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

HD61103A Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Function
V_{CC} GND V_{EE}	1 1 2		Power supply	V_{CC} – GND: Power supply for internal logic. V_{CC} – V_{EE}: Power supply for driver circuit logic.
V1L, V2L, V5L, V6L, V1R, V2R, V5R, V6R	8		Power supply	Liquid crystal display driver level power supply. V1L (V1R), V2L (V2R): Selected level V5L (V5R), V6L (V6R): Non-selected level Voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects master/slave. M/S = V_{CC}: Master mode When the HD61103A is used with the HD61102, timing generation circuit operates to supply display timing signals and operation clock to the HD61102. Each of I/O common terminals DL, DR, CL2, and M is in the output state. M/S = GND: Slave mode The timing operation circuit stops operating. The HD61103A is used in this mode when combined with the HD61830. Even if combined with the HD61102, this mode is used when display timing signals (M, data, CL2, etc.) are supplied by another HD61103A in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC}: Shift register operates at the rising edge of CL2. Select this condition when HD61103A is used with HD61102 or when MA of the HD61830 connects to CL2 in combination with the HD61830. FCS = GND: Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in combination with the HD61830.

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HD61103A Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Function
FS	1	I	V_{CC} or GND	Selects frequency. When the frame frequency is 70 Hz, the oscillation frequency should be: fosc = 430 kHz at FCS = V_{CC} fosc = 215 kHz at FCS = GND This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.
DS1, DS2	2	I	V_{CC} or GND	Selects display duty factor. Display Duty Factor: 1/48 — 1/64 — 1/96 — 1/128 DS1: GND — GND — V_{CC} — V_{CC} DS2: GND — V_{CC} — GND — V_{CC} These terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.
$\overline{STB}$ TH CL1	1 1 1	I	V_{CC} or GND	Input terminal for testing. Connect $\overline{STB}$ to V_{CC}. Connect TH and CL1 to GND.
CR, R, C	3			Oscillator. In the master mode, use these terminals as shown below. Usage of these terminals in the master mode: Internal oscillation: Rf, Cf; R, CR, C External clock: Open, External Clock, Open; R, CR, C In the slave mode, stop the oscillator as shown below: Open, V_{CC}, Open; R, CR, C
$\phi1$, $\phi2$	2	O	HD61102	Operating clock output terminals for the HD61102. Master mode: Connect these terminals to terminals $\phi1$ and $\phi2$ of the HD61102 respectively. Slave mode: Don't connect any lines to these terminals.

HD61103A Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Function
FRM	1	O	HD61102	Frame signal. Master mode: Connect this terminal to terminal FRM of the HD61102. Slave mode: Don't connect any lines to this terminal.
M	1	I/O	MB of HD61830 or M of HD61102	Signal to convert LCD driver signal into AC. Master mode: Output terminal Connect this terminal to terminal M of the HD61102. Slave mode: Input terminal. Connect this terminal to terminal MB of the HD61830.
CL2	1	I/O	CL1 or MA of HD61830 or CL of HD61102	Shift clock. Master mode: Output terminal Connect this terminal to terminal CL of the HD61102. Slave mode: Input terminal Connect this terminal to terminal CL1 or MA of the HD61830.
DL, DR	2	I/O	Open or FLM of HD61830	Data I/O terminals of bidirectional shift register. DL corresponds to X1's side and DR to X64's side. Master mode: Output common scanning signal. Don't connect any lines to these terminals normally. Slave mode: Connect terminal FLM of the HD61830 to DL (when SHL = V_{CC}) or DR (when SHL = GND)

M/S	V_{CC}		GND	
SHL	V_{CC}	GND	V_{CC}	GND
DL	Output	Output	Input	Output
DR	Output	Output	Output	Input

NC	5		Open	Not used. Don't connect any lines to this terminal.
SHL	1	I	V_{CC} or GND	Selects shift direction of bidirectional shift register.

SHL	Shift Direction	Common Scanning Direction
V_{CC}	DL → DR	X1 → X64
GND	DL ← DR	X1 ← X64

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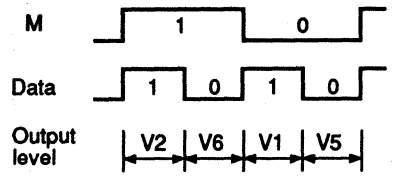
HD61103A Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Function
X1-X64	64	O	Liquid crystal display	Liquid crystal display driver output. Output one of the four liquid crystal display driver levels V1, V2, V5, and V6 with the combination of the dat from the shift register and M signal.  Data 1: Selected level 0: Non–selected level When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

Example of Application

HD61103A Connection List

H: V_{CC} } Fixed
L: GND

"—" means "open". Rf: Oscillation resister
Cf: Oscillation capacitor

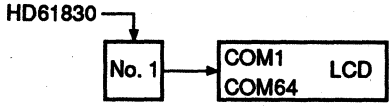
	M/S	TH	CL1	FCS	FS	DS1	DS2	STB	CR	R	C	φ1	φ2	FRM	M	CL2	SHL	DL	DR	X1–X64
A	L	L	L	L	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	—	COM1–COM64
																	L	—	from FLM of HD61830	COM64–COM1
B	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61103A No. 2	COM1–COM64
																	L	to DL/DR of HD61103A No. 2	from FLM of HD61830	COM64–COM1
C	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61103A No. 1	—	COM65–COM128
																	L	—	from DL/DR of HD61103A No. 1	COM128–COM65
D	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	to φ1 of HD61102	to φ2 of HD61102	to FRM of HD61102	to M of HD61102	to CL of HD61102	H	—	—	COM1–COM64
																	L	—	—	COM64–COM1
E	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	to φ1 of HD61102	to φ2 of HD61102	to FRM of HD61102	toM of HD61102 HD61103A	to CL of HD61102 to CL2 of HD61103A	H	—	to DL/DR of HD61103A No. 2	COM1–COM64
																	L	to DL/DR of HD61103A No. 2	—	COM64–COM1
F	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from M of HD61103A No. 1	from CL2 of HD61103A No. 1	H	from DL/DR of HD61103A No. 1	—	COM1–COM64
																	L	—	from DL/DR of HD61103A No. 1	COM64–COM1

5

Outline of HD61103A System Configuration

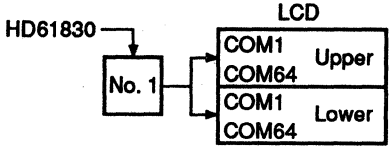
1. Use with HD61830

a. When display duty ratio of LCD is more than 1/64



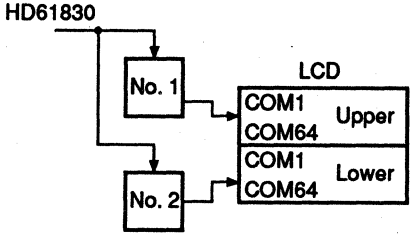
One HD61103A drives common signals.

Refer to Connection list A



One HD61103A drives common signals for upper and lower panels.

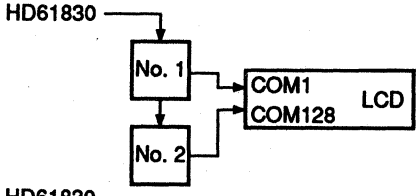
Refer to Connection list A



Two HD61103As drive upper and lower panel separately to ensure the quality of display. No. 1 and No. 2 operate in parallel.

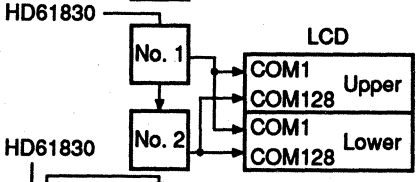
For both of No. 1 and No. 2, refer to Connection list A

b. When display duty ratio of LCD is from 1/65 to 1/128



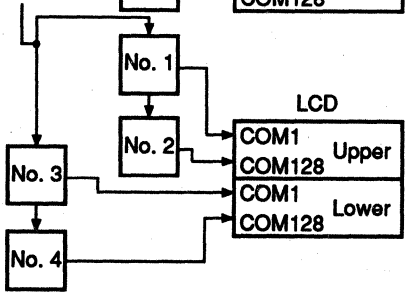
Two HD61103As connected serially drive common signals.

Refer to Connection list B for No. 1. Refer to Connection list C for No. 2.



Two HD61103As connected serially drive upper and lower panels in parallel.

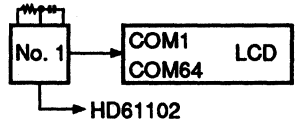
Refer to Connection list B for No. 1. Refer to Connection list C for No. 2.



Two sets of HD61103As connected serially drive upper and lower panels in parallel to ensure the quality of display.

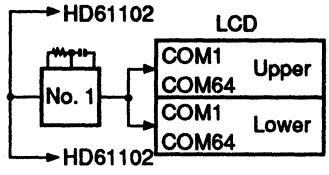
Refer to Connection list B for No. 1 and 3. Refer to Connection list C for No. 2 and 4.

2. Use with HD61102 (1/64 duty ratio)



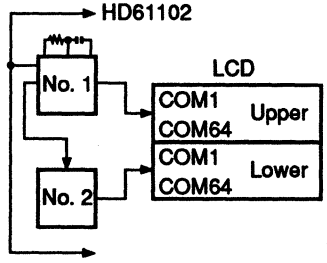
One HD61103A drives common signals and supplies timing signals to the HD61102s.

Refer to Connection list D



One HD61103A drives upper and lower panels and supplies timing signals to the HD61102s.

Refer to Connection list D



Two HD61103As drive upper and lower panels in parallel to ensure the quality of display. No. 1 supplies timing signals to No. 2 and the HD61102s.

Refer to Connection list E for No. 1

Refer to Connection list F for No. 2

5

Connection Example 1

Use with HD61102 (RAM type segment driver).
a. 1/64 duty ratio (See Connection List D)

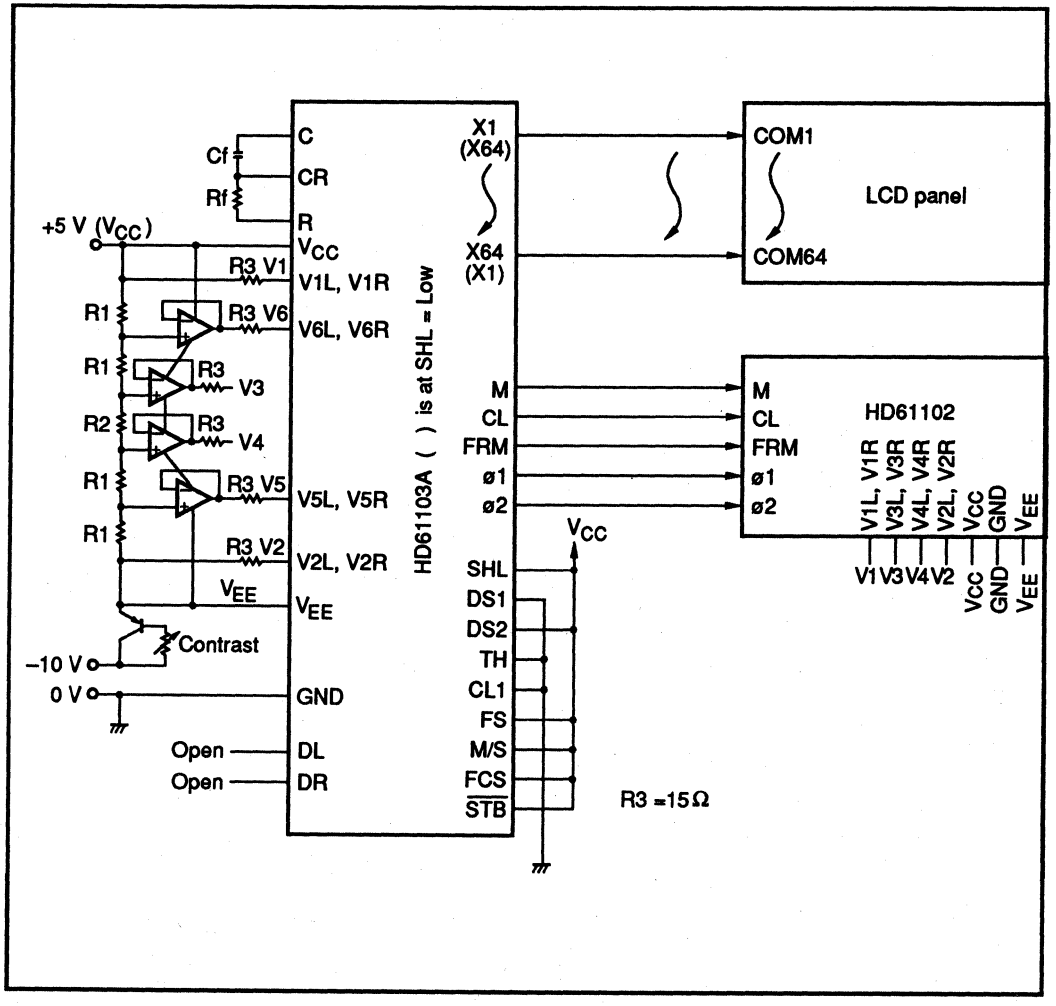


Figure 1 Example 1

Note: 1. The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1 = 3 kΩ, R2 = 15 kΩ

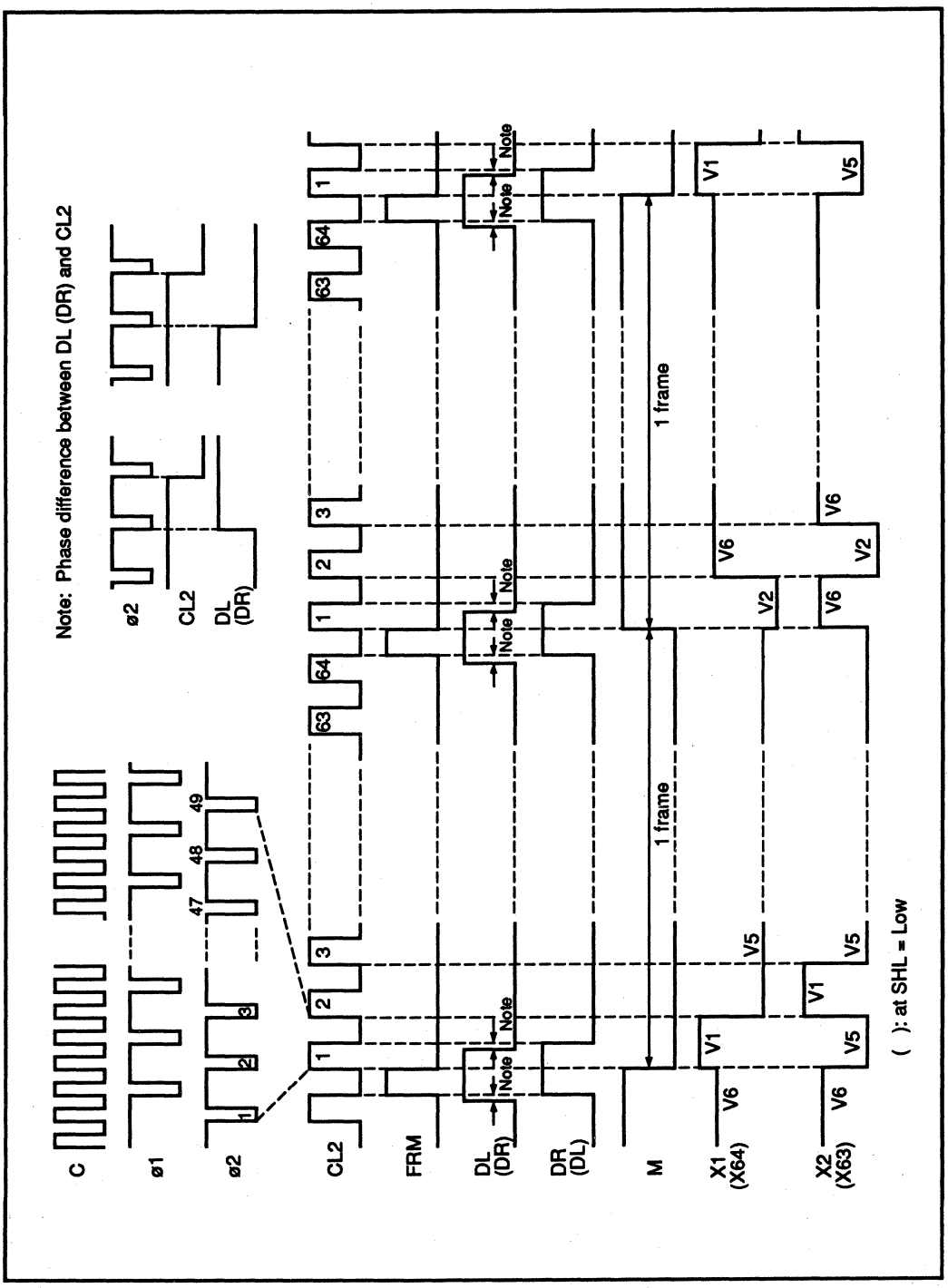


Figure 2 Example 1 Waveform (RAM type, 1/64 duty cycle)

Connection Example 2

Use with HD61830 (Display controller).
a. 1/64 duty ratio (See Connection list A)

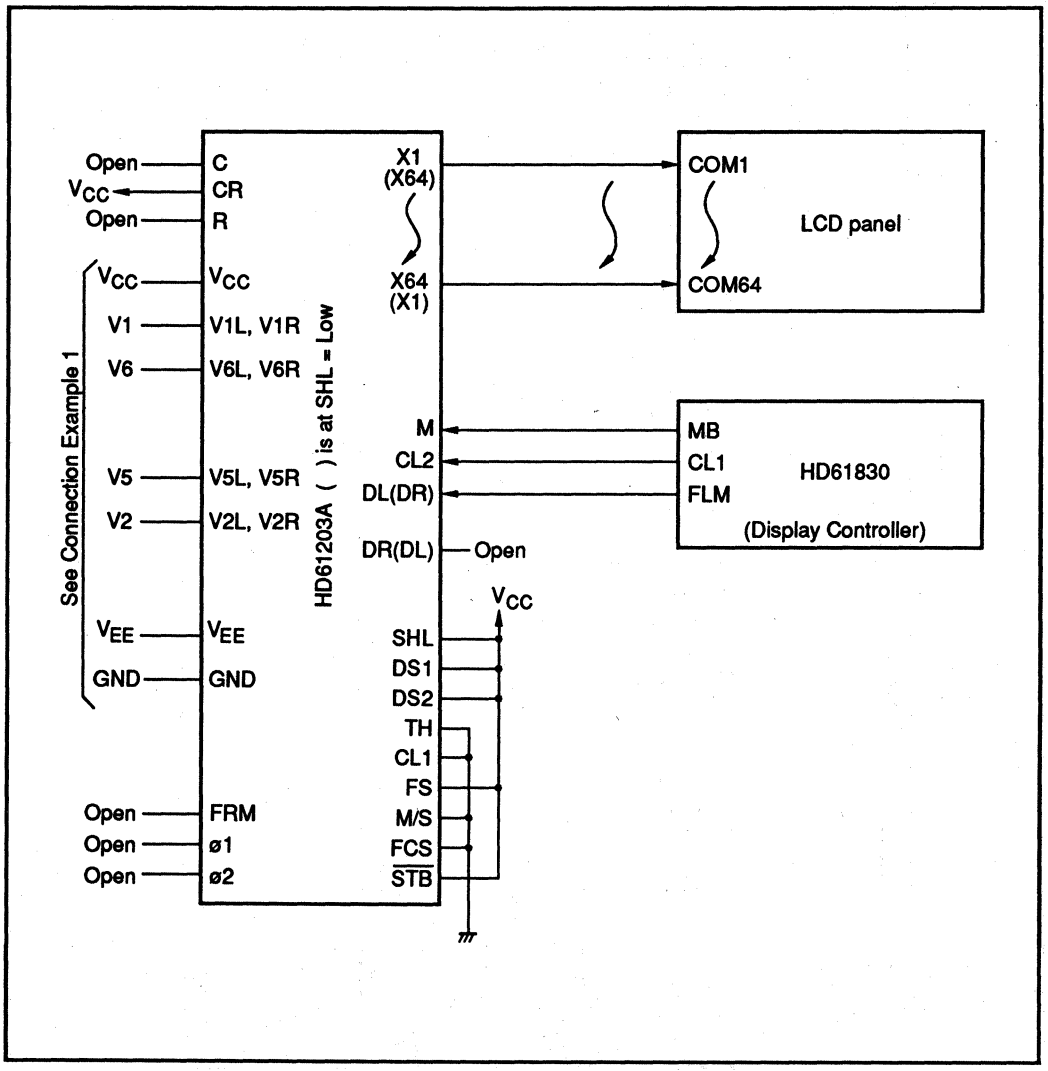


Figure 3 Example 2 (1/64 duty ratio)

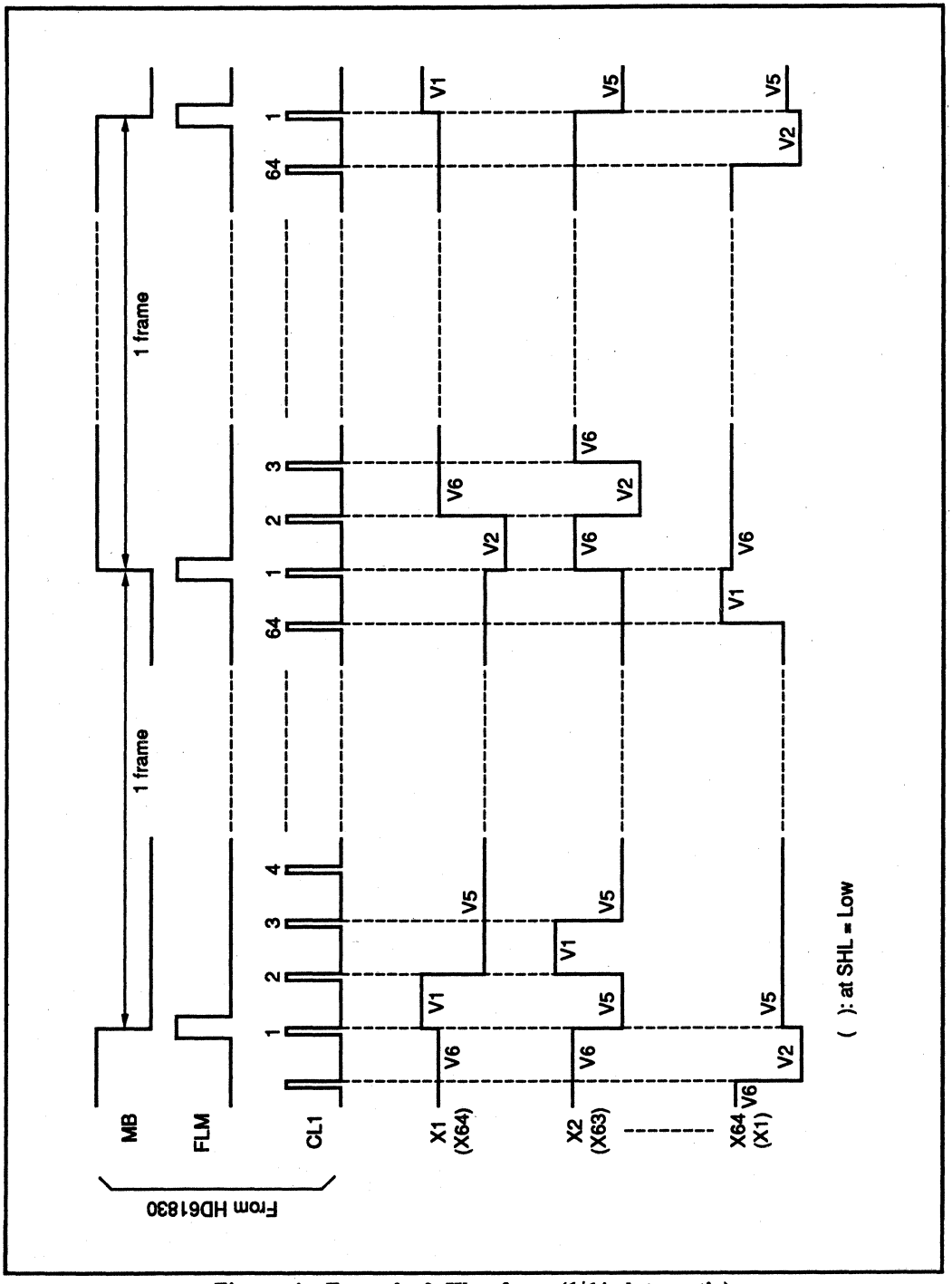


Figure 4 Example 2 Waveform (1/64 duty ratio)

b. 1/100 duty ratio (See Connection list B, C)

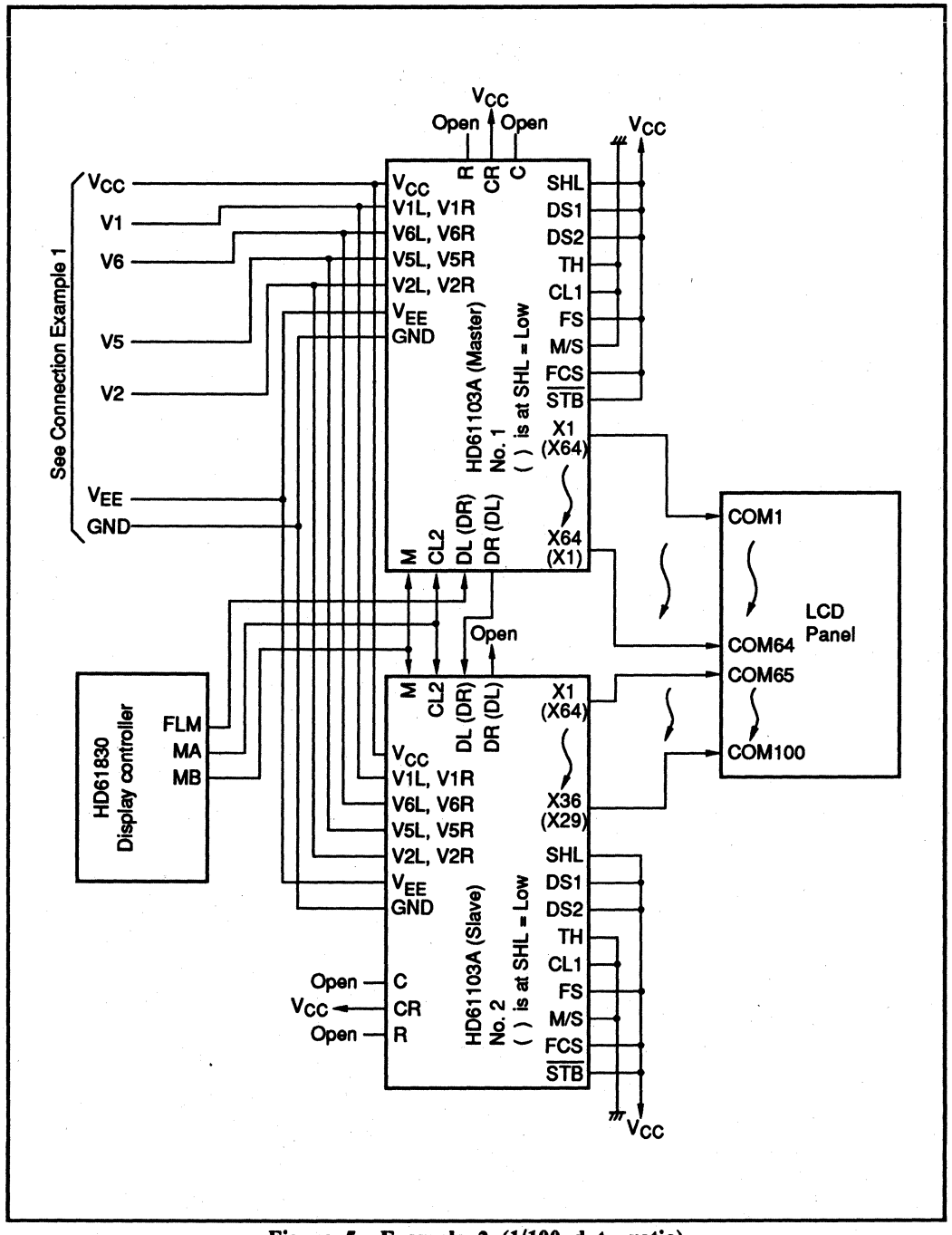


Figure 5 Example 2 (1/100 duty ratio)

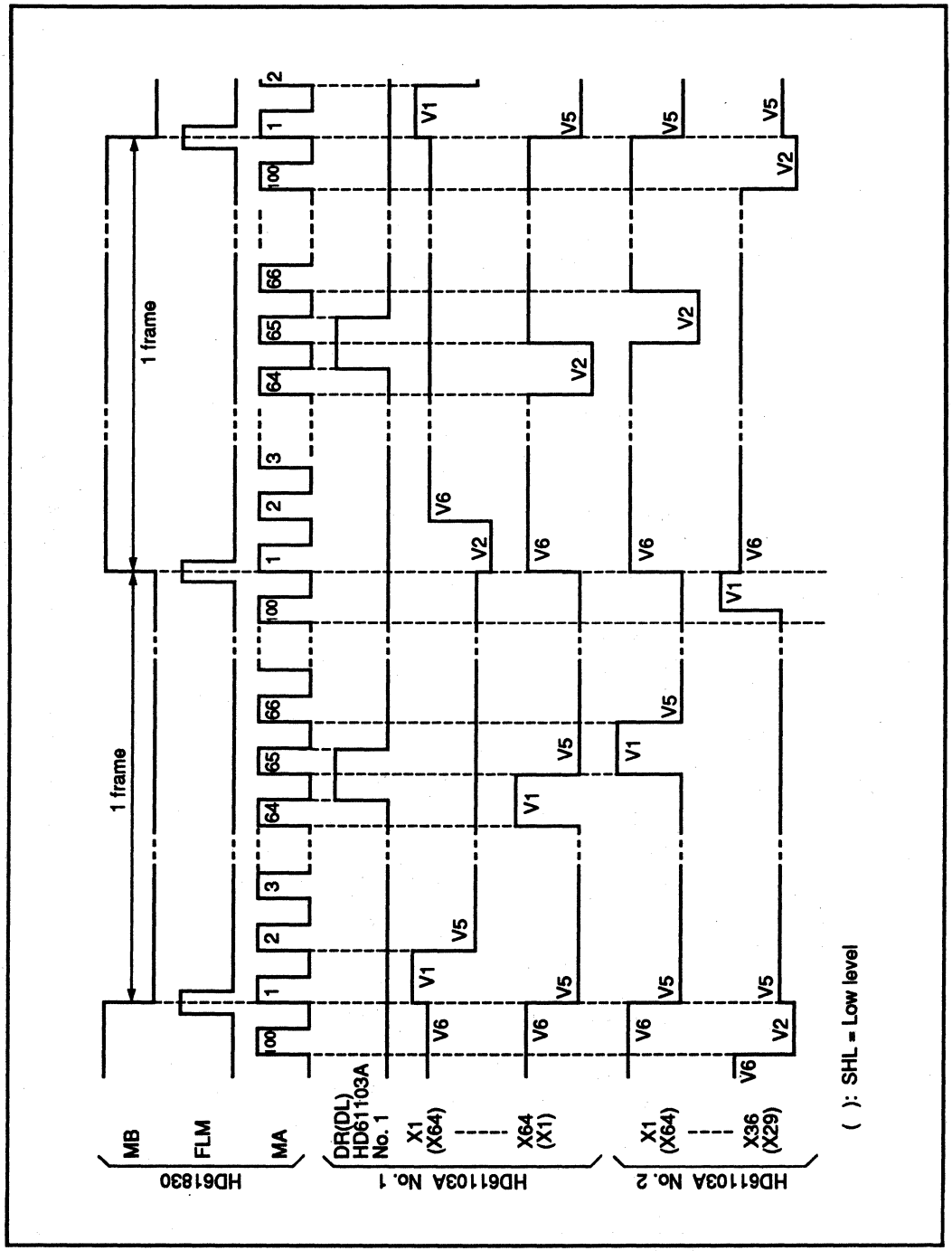


Figure 6 Example 2 (1/100 duty ratio)

5

HD61104, HD61104A
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61104, HD61104A is a column (segment) driver for large-area dot matrix liquid crystal graphic display systems.

Features

- Display duty cycle: 1/64–1/200
- Internal liquid crystal display driver: 80 drivers
- 4-bit bus, bidirectional shift data transfer
- Cascade connection with enable format
- Data transfer rate: 3.5 MHz
- Power supply for logic circuit: 5 V ±10%
- Power supply for LCD drive circuits :
  10 to 26 V (HD61104)
  10 to 28 V (HD61104A)
- Standby function
- CMOS process
- 100-pin flat plastic package

Ordering Information

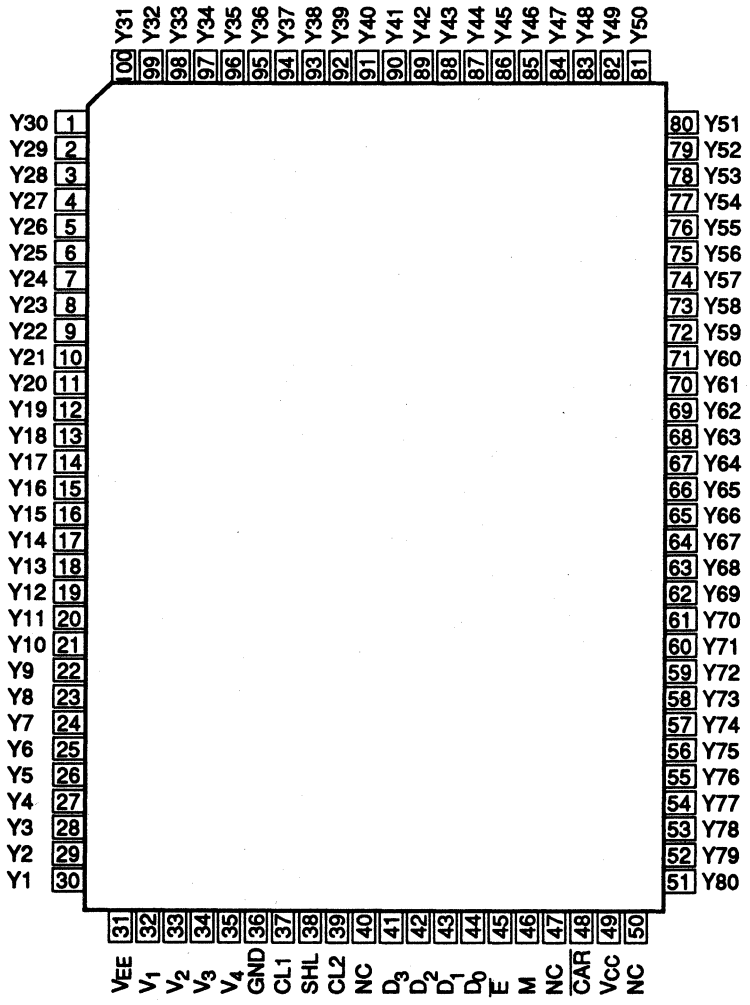
Type No.	LCD Driving Level (V)	Package
HD61104	+10 to +26	100 pin plastic QFP (FP-100)
HD61104A	+10 to +28V	
HD61104TF	+10 to +28V	100 pin plastic T-QFP (TFP-100)

Absolute Maximum Ratings

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	HD61104	V_{EE}	V_{CC} – 28.0 to V_{CC} + 0.3	V	
	HD61104A	V_{EE}	V_{CC} – 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to input terminals, SHL, CL1, CL2, D_0–D_3, $\overline{E}$, and M.
4. Applies to V_1, V_2, V_3, and V_4. Must maintain
   $V_{CC} \geq V_1 \geq V_3 \geq V_4 \geq V_2 \geq V_{EE}$
   Connect a protection resister of 15 Ω ± 10% to each terminal in series.

Pin Arrangement

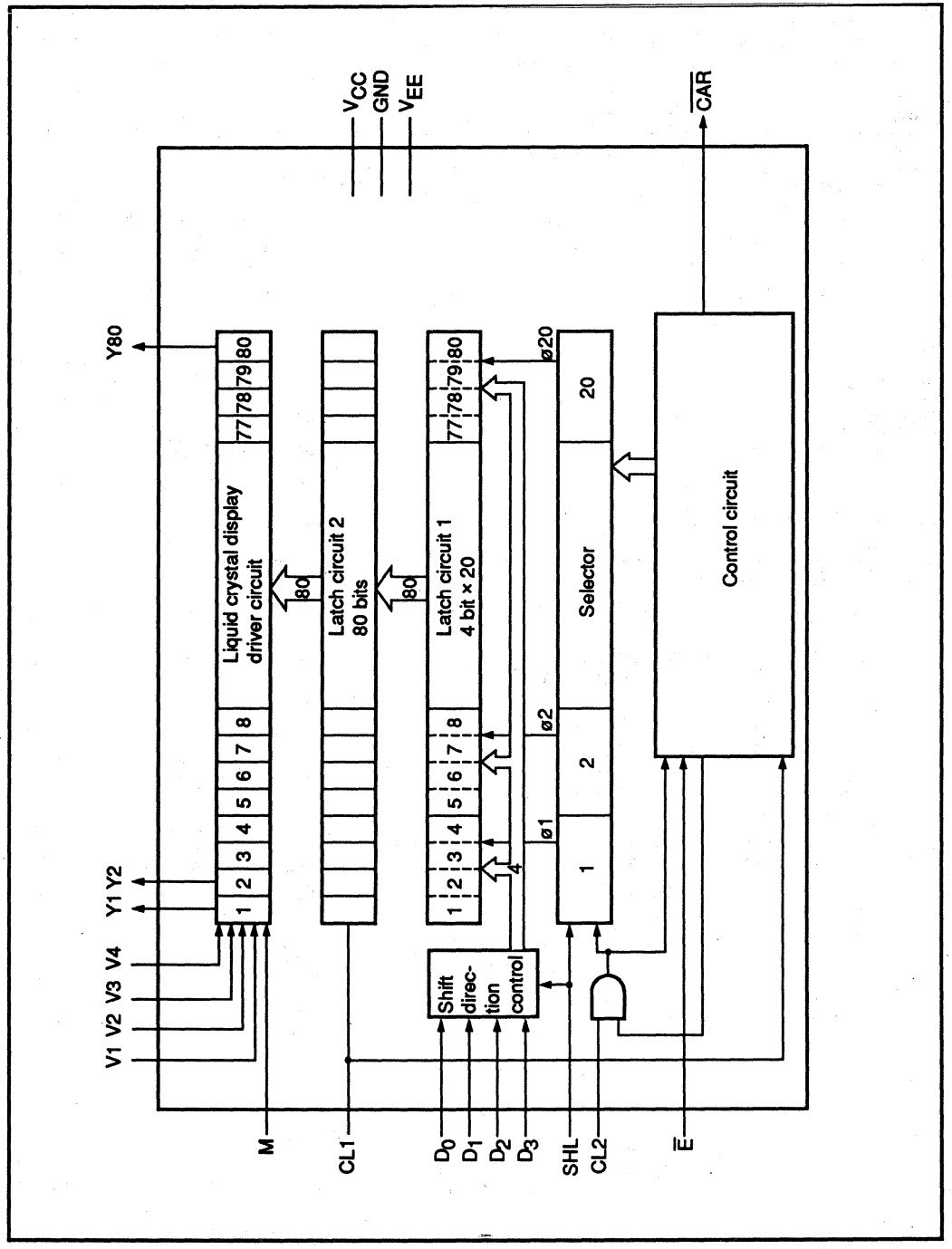


(Top View)

(FP–100/TFP–100)

5

Block Diagram



Electrical Characteristics

DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 26 V (HD61104), V_{CC} – V_{EE} = 10 to 28 V (HD61104A), Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}		V_{CC}	V		1
Input low voltage	V_{IL}	0		0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4			V	I_{OH} = – 400 µA	2
Output low voltage	V_{OL}			0.4	V	I_{OL} = 400 µA	2
Driver on resistance	R_{ON}			7.5	kΩ	V_{EE} = –1 0V,Load current =100 µA	5
Input leakage current	I_{IL1}	–1		1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–25		25	µA	V_{IN} = V_{EE} to V_{CC}	3
Dissipation current (1)	I_{GND}			2.0	mA		4
Dissipation current (2)	I_{EE}			0.2	mA	HD61104	4
				0.4		HD61104A	
Dissipation current (3)	I_{ST}			100	µA		4 5

Notes:
1. Applies to CL1, CL2, SHL, E, M, and D_0-D_3.
2. Applies to $\overline{CAR}$.
3. Applies to V_1, V_2, V_3, and V_4.
4. Specified when display data is transferred under following conditions:
   - CL2 frequency fcp2 = 2.5 MHz (data transfer rate)
   - CL1 frequency fcp1 = 14.0 kHz (data latch frequency)
   - M frequency f_M = 35 Hz (frame frequency/2)
   - Display duty ratio 1/200

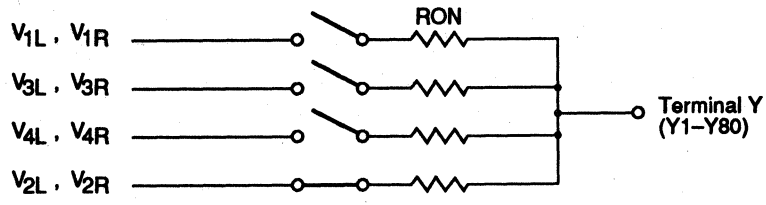
   Specified when V_{IH} = V_{CC}, V_{IL} = GND and no load on outputs.
   - I_{GND}: currents between V_{CC} and GND
   - I_{EE}: currents between V_{CC} and V_{EE}
5. Currents between V_{CC} and GND at standby ($\overline{E}$ input = high).
6. Resistance between terminal Y (one of Y1 to Y80) and terminal V (one of V_1, V_2, V_3, and V_4) when load current flows through one of the terminals Y1 to Y80. This value is specified under the following conditions:

5

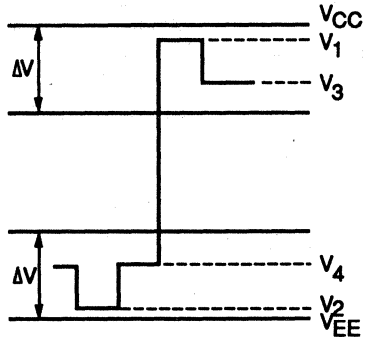
$V_{CC} - V_{EE} = 26$ V

$V_1, V_3 = V_{CC} - 2/10\ (V_{CC} - V_{EE})$

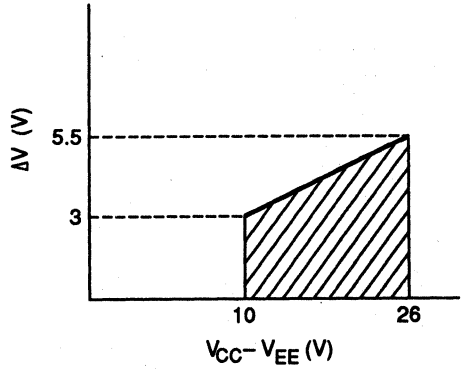
$V_2, V_4 = V_{EE} + 2/10\ (V_{CC} - V_{EE})$



The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V_1 and V_3, and negative voltage to V_2 and V_4, within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

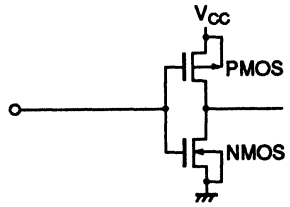


Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

Terminal Configuration

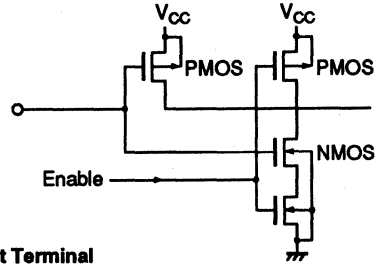
Input Terminal

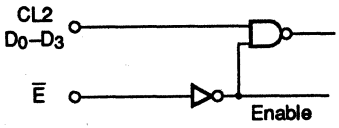
Applicable Terminals : CL1, SHL, $\overline{E}$, M



Input Terminal (controlled by Enable signal)

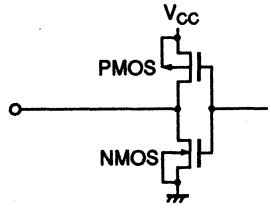
Applicable Terminals : CL2, D_0–D_3





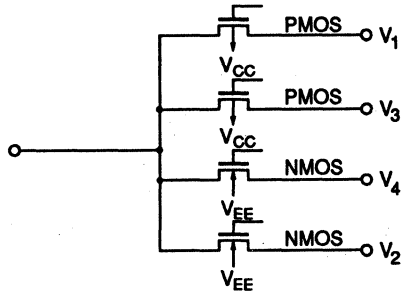
Output Terminal

Applicable Terminal : $\overline{CAR}$



Output Terminal

Applicable Terminals : Y1–Y80



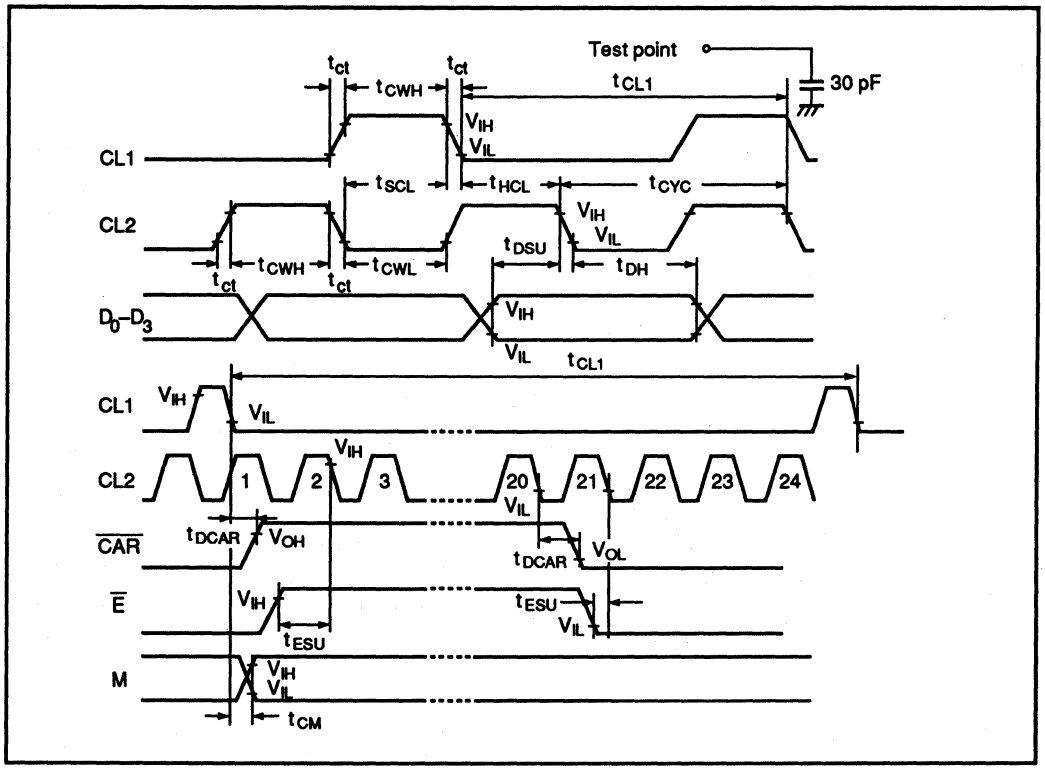
5

AC Characteristics

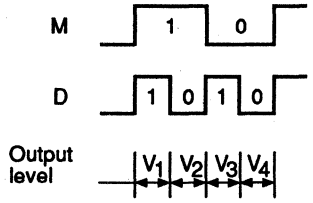
(V_{CC} = 5 V ± 10%, GND = 0 V, Ta = -20 to ±75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Clock cycle time	t_{CYC}	285	—	—	ns	
Clock high level width	t_{CWH}	110	—	—	ns	
Clock low level width	t_{CWL}	110	—	—	ns	
Clock setup time	t_{SCL}	80	—	—	ns	
Clock hold time	t_{HCL}	80	—	—	ns	
Clock rise/fall time	t_{CT}	—	—	30	ns	
Data setup time	t_{DSU}	80	—	—	ns	
Data hold time	t_{DH}	80	—	—	ns	
E setup time	t_{ESU}	75	—	—	ns	
Output delay time	t_{DCAR}	—	—	180	ns	1
M phase difference time	t_{CM}	—	—	300	ns	
CL1 cycle time	t_{CL1}	$t_{CYC} \times 10$	—	—	ns	

Note: 1. The following load circuit is connected for specification:


Test point
30 pF
tct
tCWH
tCL1
VIH
VIL
CL1
tSCL
tHCL
tCYC
CL2
tDSU
tDH
tCWL
D0–D3
CL1
CL2
1
2
3
20
21
22
23
24
CAR
tDCAR
VOH
VOL
E
tESU
M
tCM

5

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_1 V_2 V_3 V_4	4		Power supply	Power supply for liquid crystal drive. V_1, V_2: selection level V_3, V_4: non-selection level
Y1–Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V_1, V_2, V_3, and V_4. Relation among output level, M, and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (falling edge triggered). Synchronized with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge triggered.
D_0–D_3	4	I	Controller	Input of 4-bit display data (D)

D	Liquid Crystal Driver Output	Liquid Crystal Display
1 (High level)	Selection level	On
0 (Low level)	Non-selection level	Off

Truth table (Positive logic)

SHL	Input data and latch circuit 1
0	$D_3 \rightarrow 1 \rightarrow 5 \rightarrow 9 \cdots \rightarrow 73 \rightarrow 77$
	$D_2 \rightarrow 2 \rightarrow 6 \rightarrow 10 \cdots \rightarrow 74 \rightarrow 78$
	$D_1 \rightarrow 3 \rightarrow 7 \rightarrow 11 \cdots \rightarrow 75 \rightarrow 79$
	$D_0 \rightarrow 4 \rightarrow 8 \rightarrow 12 \cdots \rightarrow 76 \rightarrow 80$

Terminal Name	Number of Terminals	I/O	Connected to	Functions
				Truth table (Positive logic) (cont) SHL: 1 — Input data and latch circuit 1 $D_3 \rightarrow 80 \rightarrow 76 \rightarrow 72 \text{ --- } \rightarrow 8 \rightarrow 4$ $D_2 \rightarrow 79 \rightarrow 75 \rightarrow 71 \text{ --- } \rightarrow 7 \rightarrow 3$ $D_1 \rightarrow 78 \rightarrow 74 \rightarrow 70 \text{ --- } \rightarrow 6 \rightarrow 2$ $D_0 \rightarrow 77 \rightarrow 73 \rightarrow 69 \text{ --- } \rightarrow 5 \rightarrow 1$ ex: When SHL = 0, the data that is input to D_3 is latched to each bit of the latch circuit 1 in order of $1 \rightarrow 5 \rightarrow 9 \text{ --- } \rightarrow 77$.
SHL	1	I	V_{CC} or GND	Selects a shift direction of display data.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61104	Enable input. The operation stops at high level, and is enabled at low level.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61104	Enable output. Used for cascade connection.
NC	3			Unused. No wire should be connected.

5

Typical Application

Figure 1 is an LCD panel with 200 × 640 dots on which characters are displayed with 1/200 duty cycle dynamic drive.

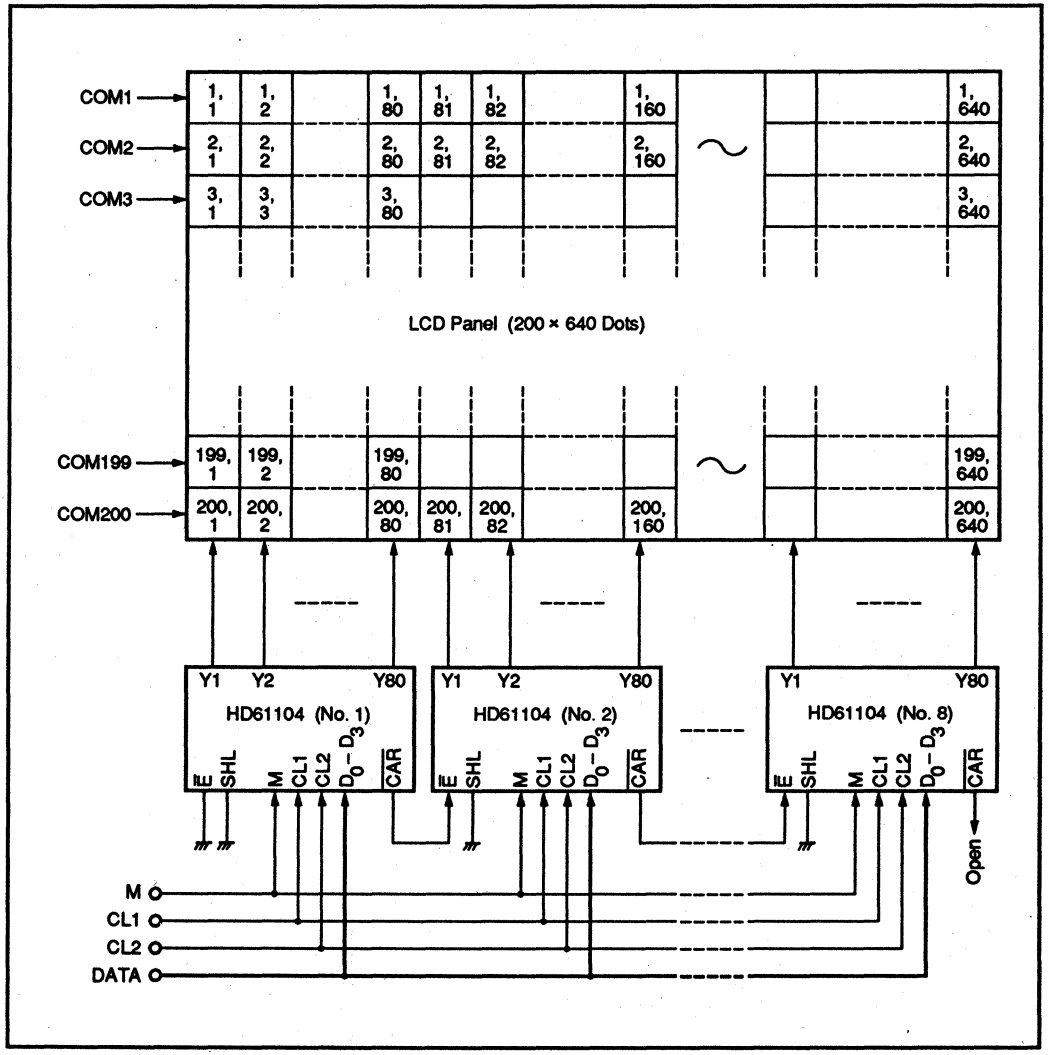


Figure 1 200 × 640 Dot LCD Panel Example

Cascade eight HD61104s. Input data to the D_0—D_3 terminals of Nos. 1–8. Connect $\overline{E}$ of No. 1 to GND. Connect no lines to $\overline{CAR}$ of No. 8 . Connect common signal terminals (COM1–COM200) to the common driver HD61105. (m,n) of LCD panel is the address corresponding to each dot. Figure 2 shows timing.

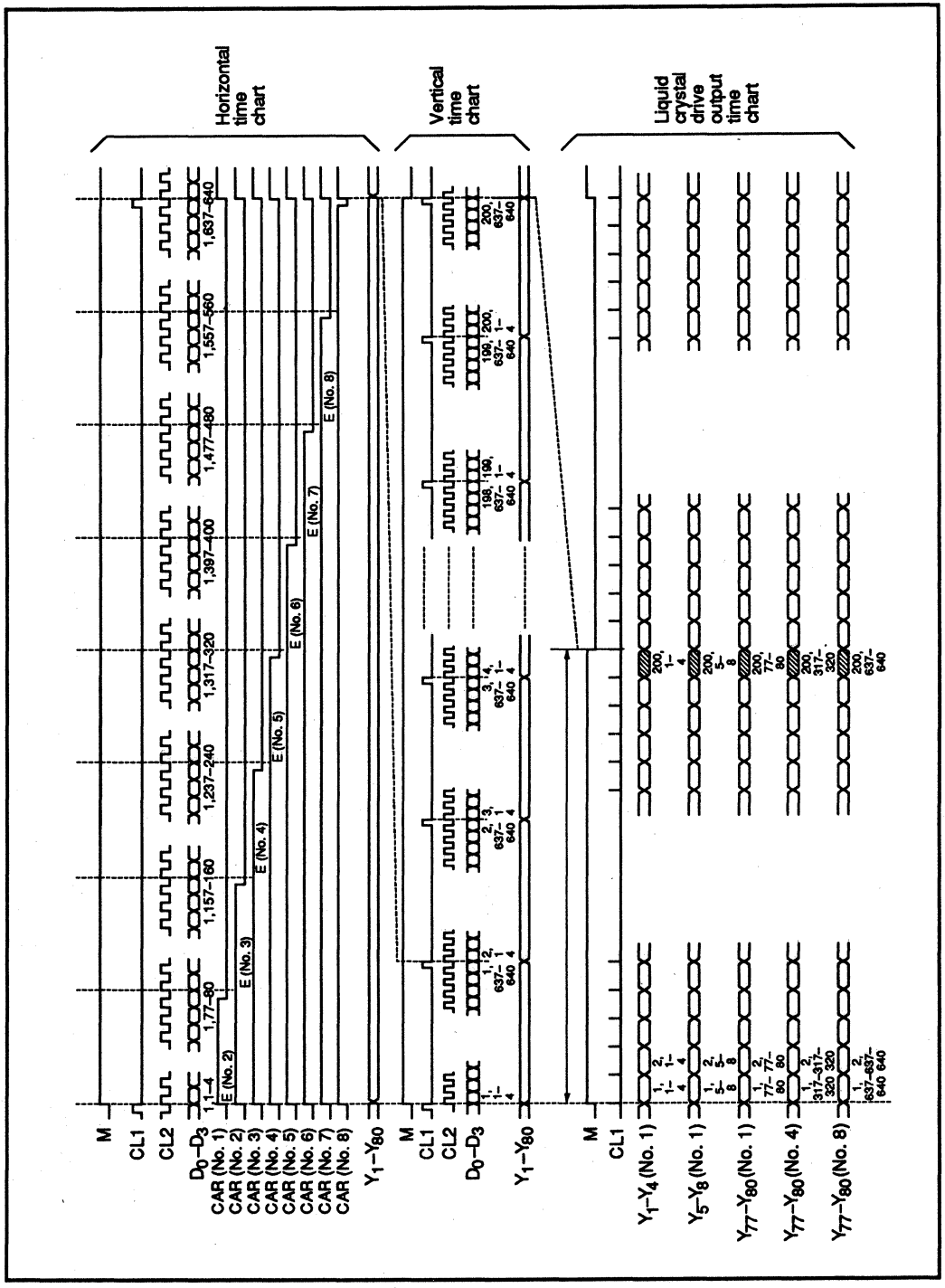


Figure 2 Waveform Example

5

HD61105, HD61105A
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD61105, HD61105A is a common signal driver for dot matrix liquid crystal graphic display systems. It provides 80 driver output lines and the impedance is low enough to drive a large screen.

As the HD61105, HD61105A is produced in a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption.

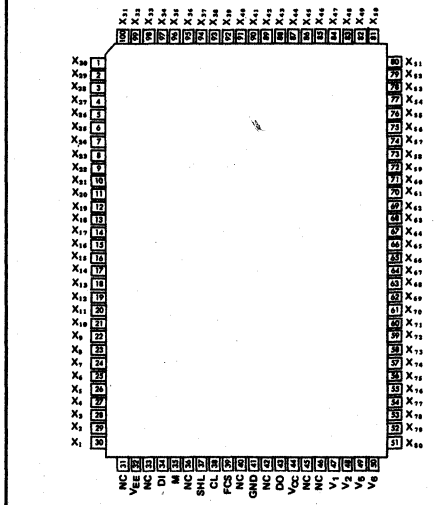
Features

- Dot matrix liquid crystal graphic display common driver with low impedance
- Internal liquid crystal display driver circuit: 80 circuits
- Display duty ratio factor: 1/64—1/200
- Internal 80-bit shift register
- Power supply for logic circuit: 5 ± 10%
- Power supply for LCD drive circuits:
  —10 to 26 V (HD61105)
  —10 to 28 V (HD61105A)
- CMOS process
- 100-pin plastic QFP (FP-100)

Ordering Information

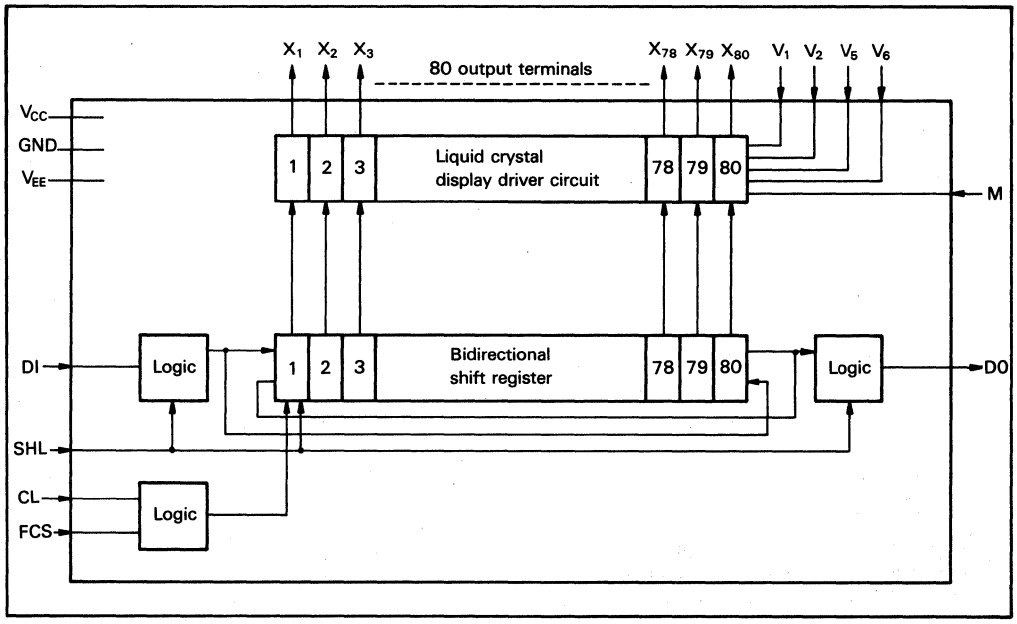
Type No.	LCD Driving Level (V)	Package
HD61105	10 to 26	100 pin plastic QFP (FP-100)
HD61105A	10 to 28	
HD61105TF	10 to 28	100 pin plastic T-QFP (TFP-100)

Pin Arrangement



FP-100/TFP-100
(Top View)

Block Diagram



Absolute maximum ratings

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	− 0.3 to + 7.0	V	2
Supply voltage (2)	HD61105	V_{EE}	V_{CC} − 28.0 to V_{CC} + 0.3	V	5
	HD61105A		V_{CC} − 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	− 0.3 to V_{CC} +0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} − 0.3 to V_{CC} +0.3	V	4, 5
Operating temperature		Topr	− 20 to + 75	°C	
Storage temperature		Tstg	− 55 to + 125	°C	

Notes: 1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to input terminals except V_1, V_2, V_5, and V_6.
4. Applies to V_1, V_2, V_5, and V_6.
5. $V_{CC} \geqq V_1 \geqq V_6 \geqq V_5 \geqq V_2 \geqq V_{EE}$ must be maintained.

5

Electrical Characteristics

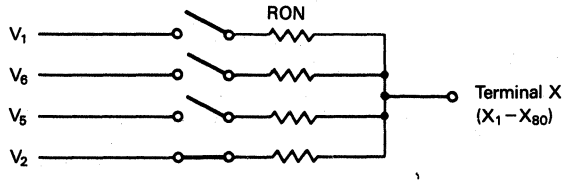
DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} − V_{EE} = 10 to 26 V (HD61105), V_{CC} − V_{EE} = 10 to 28 V (HD61105A), T_a = − 20 to + 75°C)

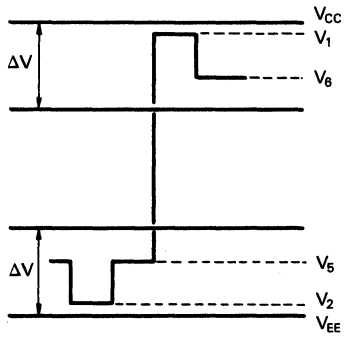
		Specifications					
Test Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**	**Note**
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} − 0.4	—	—	V	I_{OH} = − 0.4mA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.4mA	2
Vi—Xj on resistance	R_{ON}	—	—	2.0	kΩ	V_{CC} − V_{EE} = 10 V Load current ± 150 μA	5
Input leakage current	I_{IL1}	− 1.0	—	1.0	μA	V_{IN} = 0 to V_{CC}	3
Input leakage current	I_{IL2}	− 25	—	25	μA	V_{IN} = V_{EE} to V_{CC}	4
Clock frequency	f_{CL}	—	—	100	kHz	Transfer clock CL	
Dissipation current (1)	I_{GG1}	—	—	200	μA	at 1/200 duty cycle operation	6
Dissipation current (2)	I_{EE}	—	—	100	μA	at 1/200 duty cycle operation	7

Notes:
1. Applies to input terminals FCS, SHL, DI, M, and CL.
2. Applies to output terminal of DO.
3. Applies to the terminals NC, and the input terminals FCS, SHL, DI, M, and CL.
4. Applies to V_1, V_2, V_5, and V_6. No wire should be connected to X_1—X_{80}.
5. Resistance value between terminal X (one of X_1 to X_{80}) and terminal V (one of V_1, V_2, V_5, and V_6) when load current is applied to one of terminals X_1 to X_{80}. This value is specified under the following conditions:

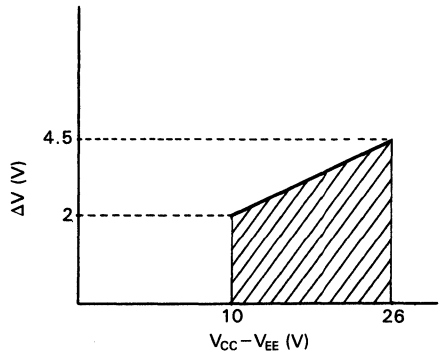
$V_{CC}-V_{EE}=26\,V$
$V_1, V_6=V_{CC}-1/10\,(V_{CC}-V_{EE})$
$V_2, V_5=V_{EE}+1/10\,(V_{CC}-V_{EE})$



The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V_1 and V_6, and negative voltage to V_2 and V_5, within the △V range. This range allows stable impedance on driver output (R_{ON}). Notice that △V depends on power supply voltage V_{CC}—V_{EE}.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

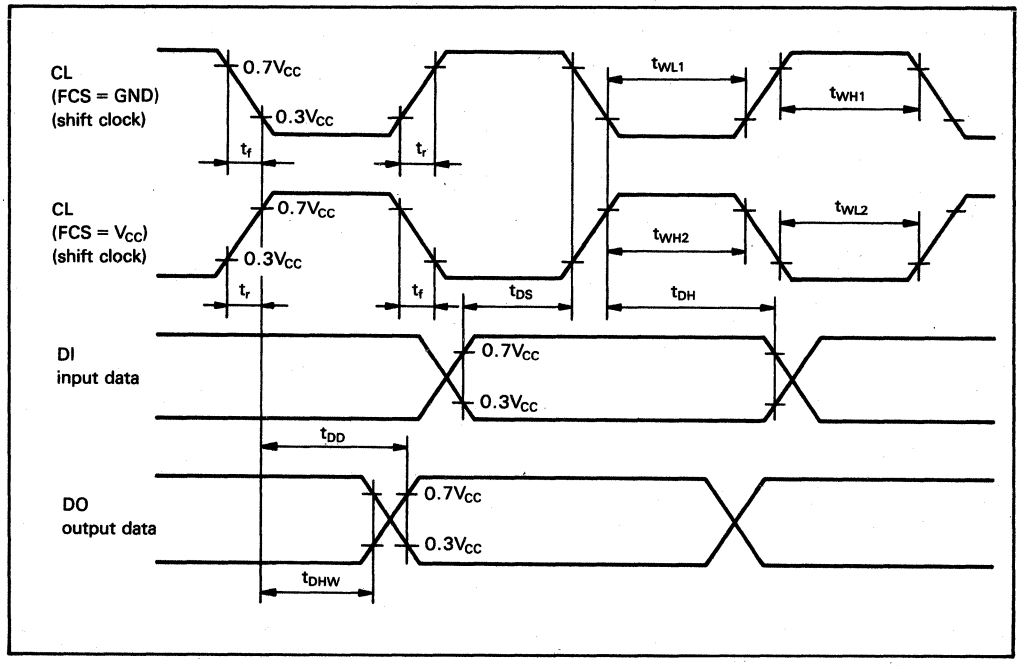


Correlation between Power Supply Voltage V_{CC}—V_{EE} and △V

6. The currents flowing through the GND terminal. Specified when display data is transferred under following conditions:
   CL frequency f_{CL} = 14kHz (data transfer rate)
   M frequency fM = 35 Hz (frame frequency/2) 1/200
   Display duty ratio
   $V_{IH} = V_{CC}$, V_{IL} = GND
   No load on outputs
7. The currents flowing through the V_{EE} terminal in the conditions of note 6. No line should be connected to the V terminal.

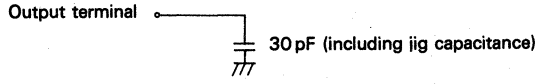
5

AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = − 20 to + 75°C)



Item	Symbol	Min	Typ	Max	Unit	Note
Clock low level width (FCS = GND)	t_{WL1}	5.0			μs	
Clock high level width (FCS = GND)	t_{WH1}	125			ns	
Clock low level width (FCS = V_{CC})	t_{WL2}	125			ns	
Clock high level width (FCS = V_{CC})	t_{WH2}	5.0			μs	
Data setup time	t_{DS}	100			ns	
Data hold time	t_{DH}	100			ns	
Output delay time	t_{DD}			3.0	μs	1
Output hold time	t_{DHW}	100			ns	
Clock rise time	t_r			30	ns	
Clock fall time	t_f			30	ns	

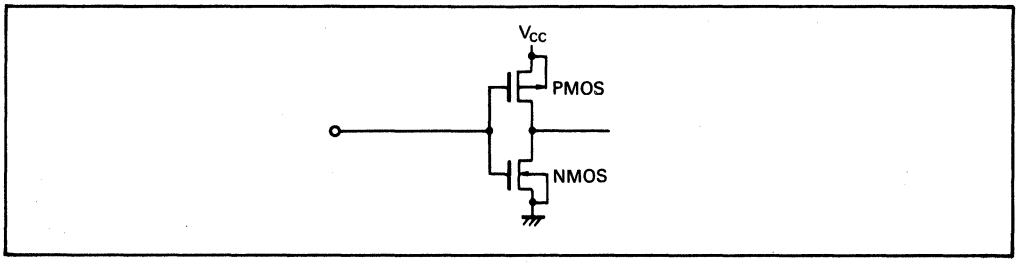
Note: 1. The following load circuits are connected for specification:



Terminal Configuration

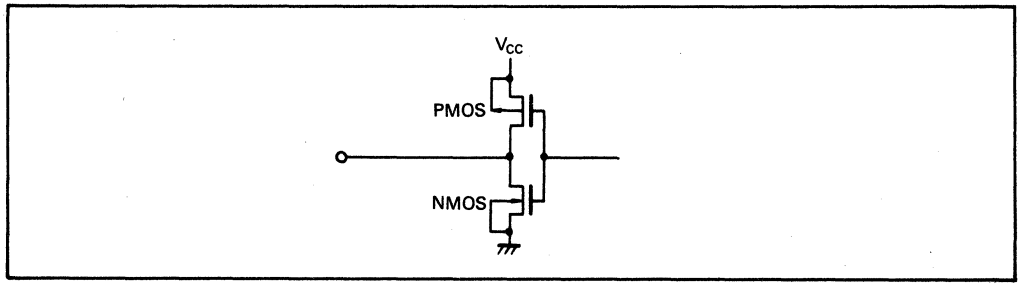
Input Terminal

Applicable Terminals: DI, CL, SHL, FCS, M



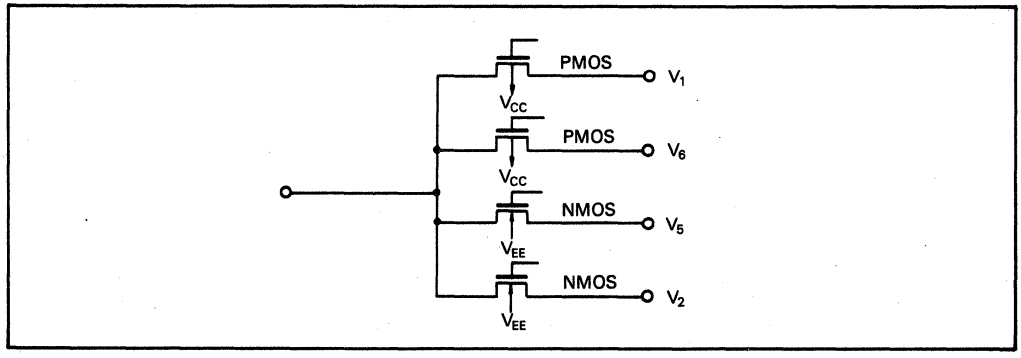
Output Terminal

Applicable Terminal: DO



Output Terminal

Applicable Terminals: X_1—X_{80}



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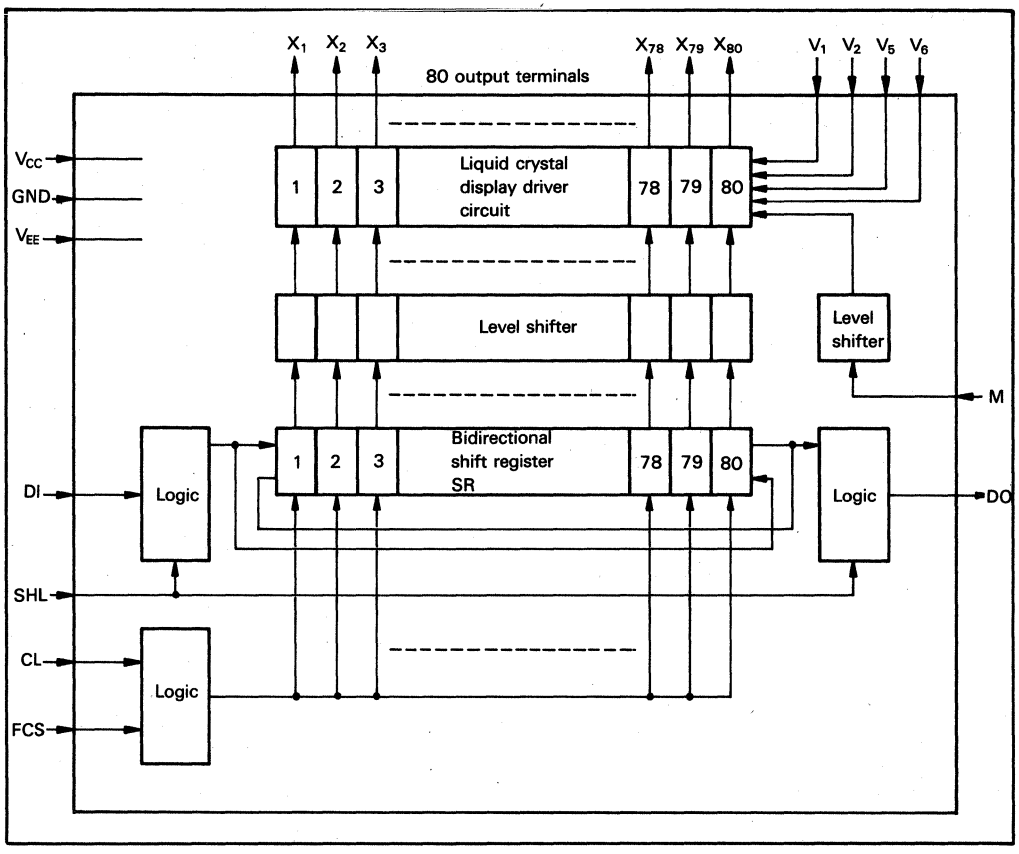
Block Diagram



Block Functions

Bidirectional Shift Register

This is a 80-bit bidirectional register. The data from the DI terminal is shifted by the shift clock CL. The output terminal DO outputs the last shifted data. In case of serial cascade connection, terminal DO functions as the data input to the next LSI. Terminal SHL selects the data shift direction (table 1), and the terminal FCS selects the shift clock phase (table 2).

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals (table 3).

Table 1 SHL Truth Table

(Positive Logic)

SHL	Data Shift Direction
1	DI → SR1 → SR2 → SR3 ····· SR79 → SR80 → DO
0	DI → SR80 → SR79 → SR78 ····· SR2 → SR1 → DO

Table 2 FCS Truth Table

FCS	Shift Clock Phase
0	Shifted at the falling edge of CL
1	Shifted at the rising edge of CL

Table 3 M Truth Table

(Positive Logic)

Data from the Shift Register	M	Output level
0	0	V_5
1	0	V_1
0	1	V_6
1	1	V_2

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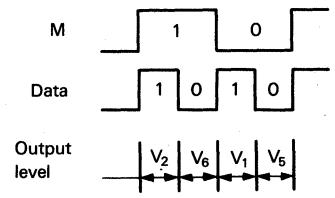
HD61105 Terminal Functions

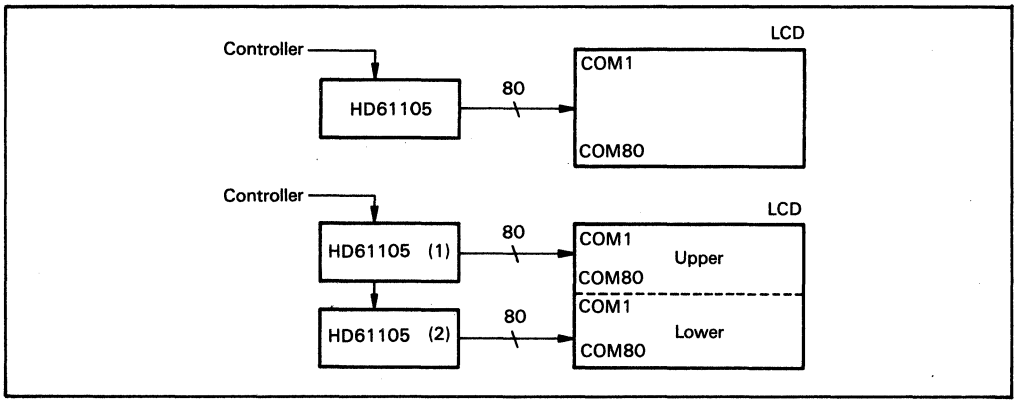
Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} — GND: Power supply for internal logic V_{CC} — V_{EE}: Power supply for LCD drive circuit
V_1 V_2 V_5 V_6	4		Liquid crystal drive level power supply	Power supply for liquid crystal drive V_1, V_2: selection level V_5, V_6: non-selection level
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC} Shift register operates at the rise of CL FCS = GND Shift register operates at the fall of CL
M	1	I	Controller	Signal to convert LCD driver signal into AC
CL	1	I	Controller	Shift clock FCS = V_{CC} Shift register operates at the rise of CL FCS = GND Shift register operates at the fall of CL
DI	1	I	Controller or terminal DO of HD61105	Shift register data input In case of cascade connection, the terminal DI is connected to the terminal DO of the preceding LSI.
DO	1	O	Open or terminal DI of HD61105	Shift register data output In case of cascade connection, the terminal DO is connected to the terminal DI of the next LSI.
SHL	1	I	V_{CC} or GND	Selects shift direction of bidirectional shift register.

SHL	Shift Direction	Common Scanning Direction
V_{CC}	DI → SR1 → SR2 → SR80	$X_1 \rightarrow X_{80}$
GND	DI → SR80 → SR79 → SR1	$X_{80} \rightarrow X_1$

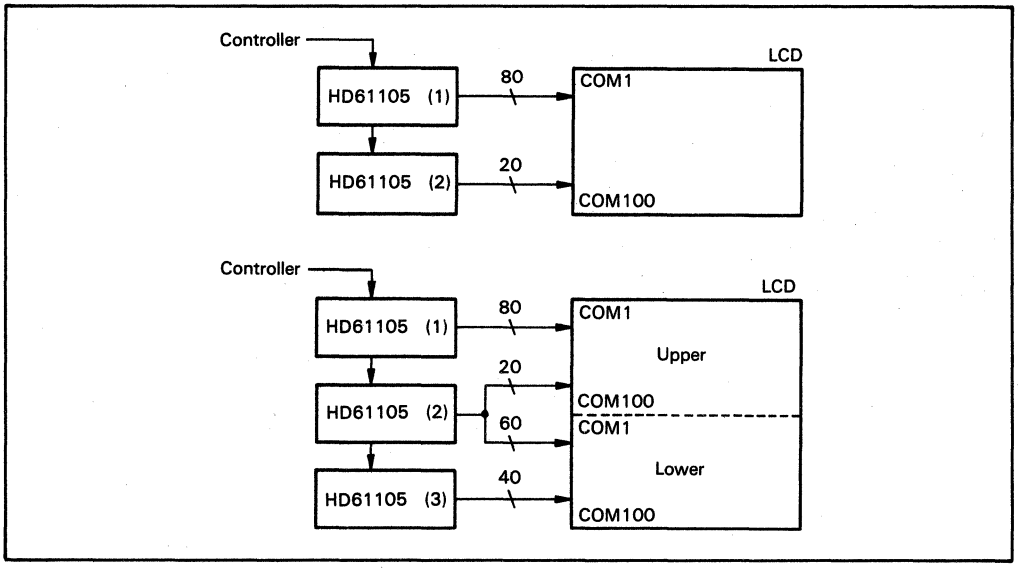
X_1—X_{80}	80	O	Liquid crystal display	Liquid crystal display driver output Outputs one of the four liquid crystal display driver levels V_1, V_2, V_5, and V_6 with the combination of the data from the shift register and M signal.  Data 1: Selection level Data 0: Non-selection level When SHL is V_{CC}, X_1 corresponds to COM1 and X_{80} corresponds to COM80. When SHL is GND, X_{80} corresponds to COM1 and X_1 corresponds to COM80.
NC	7		Open	Unused. No line should be connected.

Outline of HD61105 System Configuration

When display duty ratio of LCD is 1/80



When display duty ratio of LCD is 1/100



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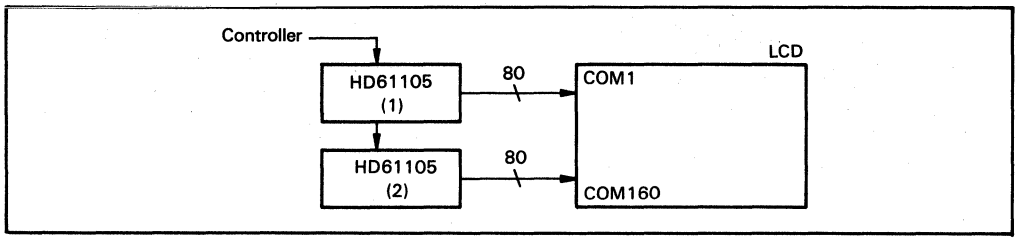
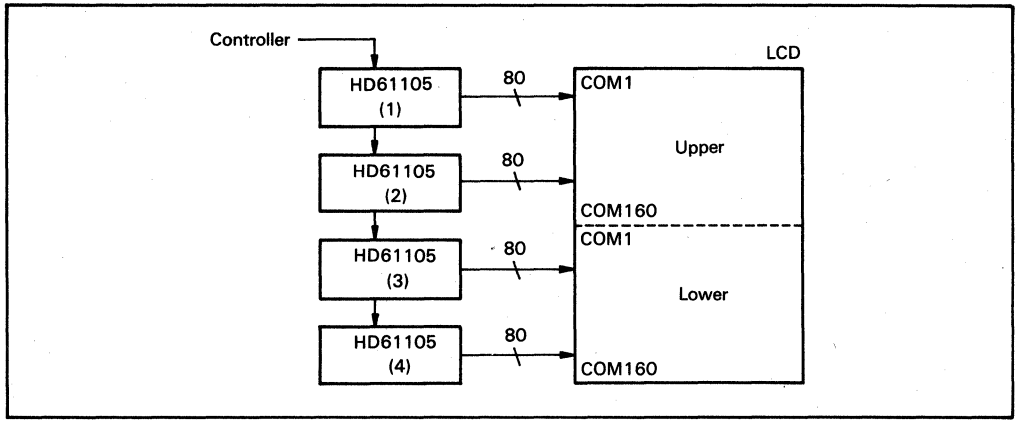
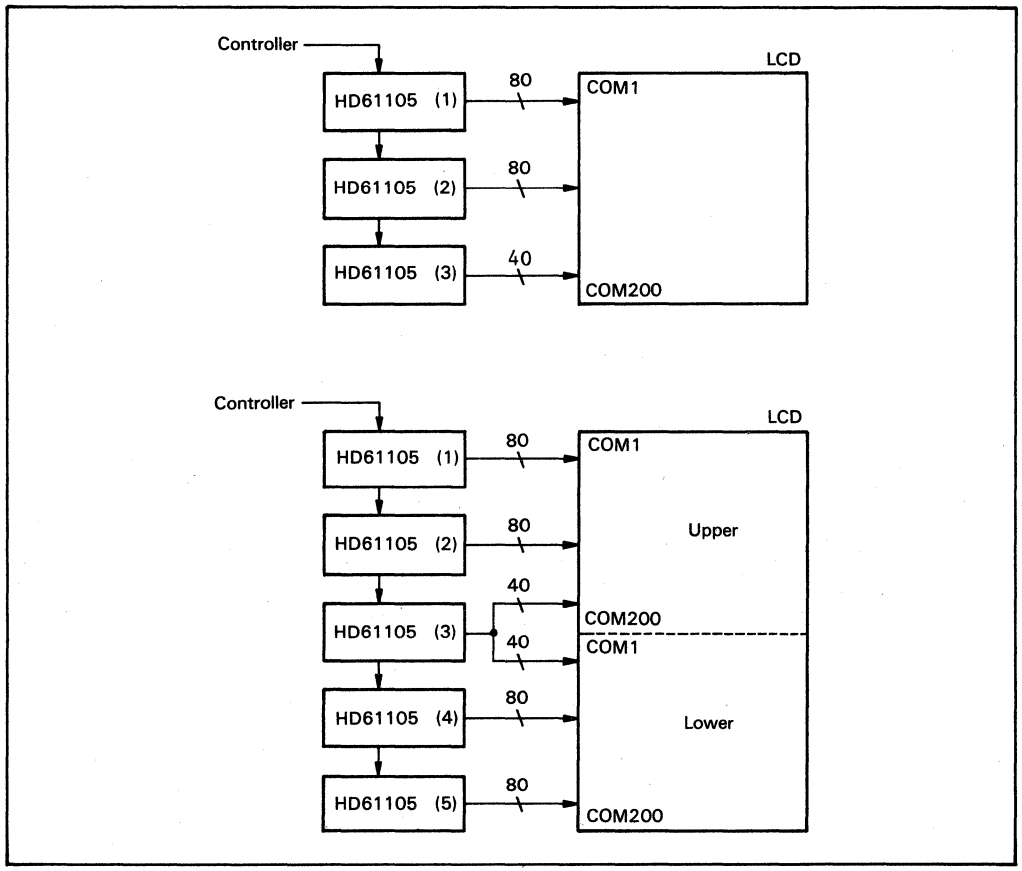
When display duty ratio of LCD is 1/160



When display duty ratio of LCD is 1/160



When display duty ratio of LCD is 1/200



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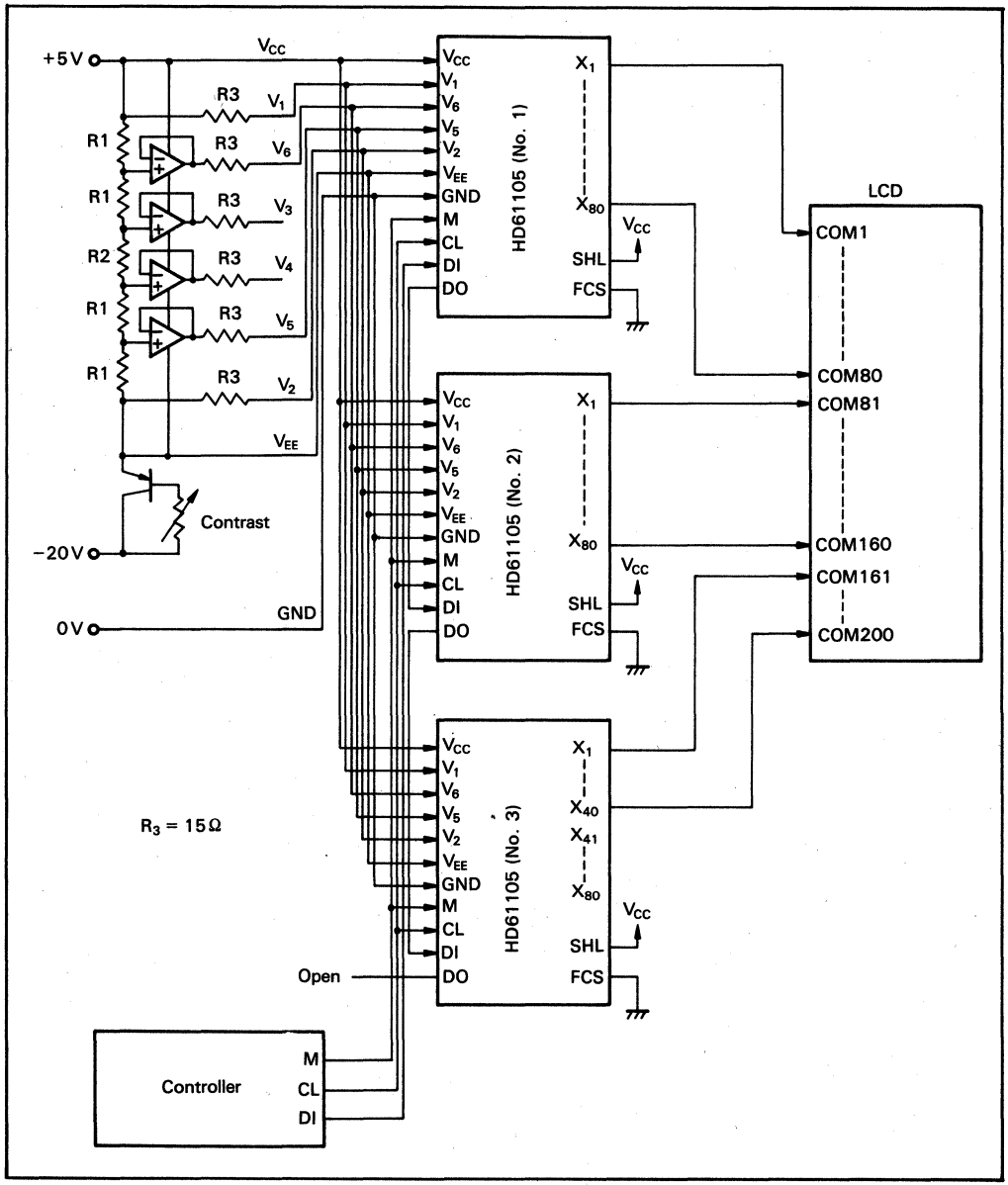
Example of Connection

1/200 duty ratio



Note: 1. The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/15, the values of R1 and R2 should satisfy $\frac{R1}{4R1+R2}=\frac{1}{15}$
For example, R1 = 3 KΩ, R2 = 33 KΩ

Figure 1 Example of Connection (SHL = V_{CC}, FCS = GND)

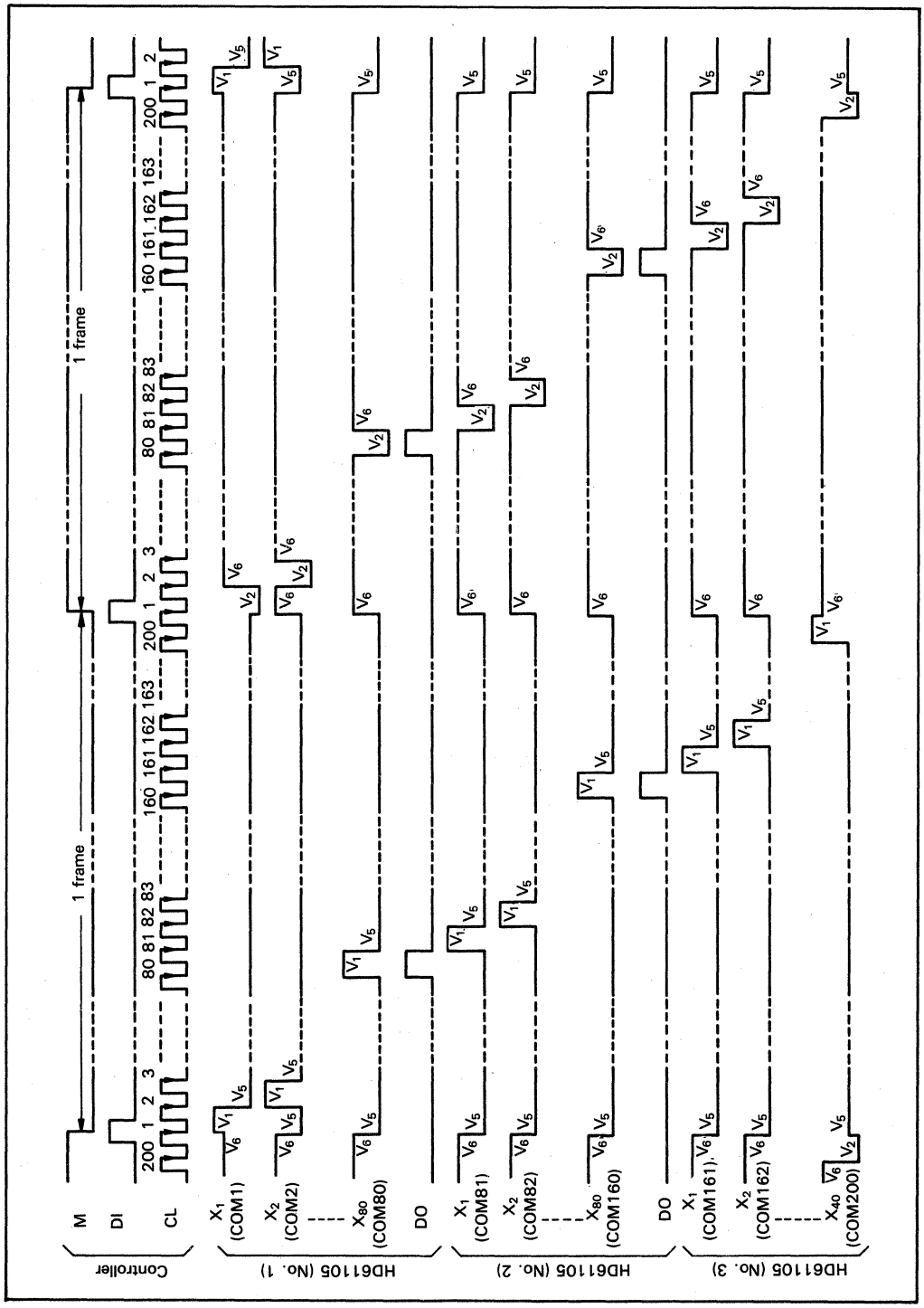


Figure 2 Waveform Example

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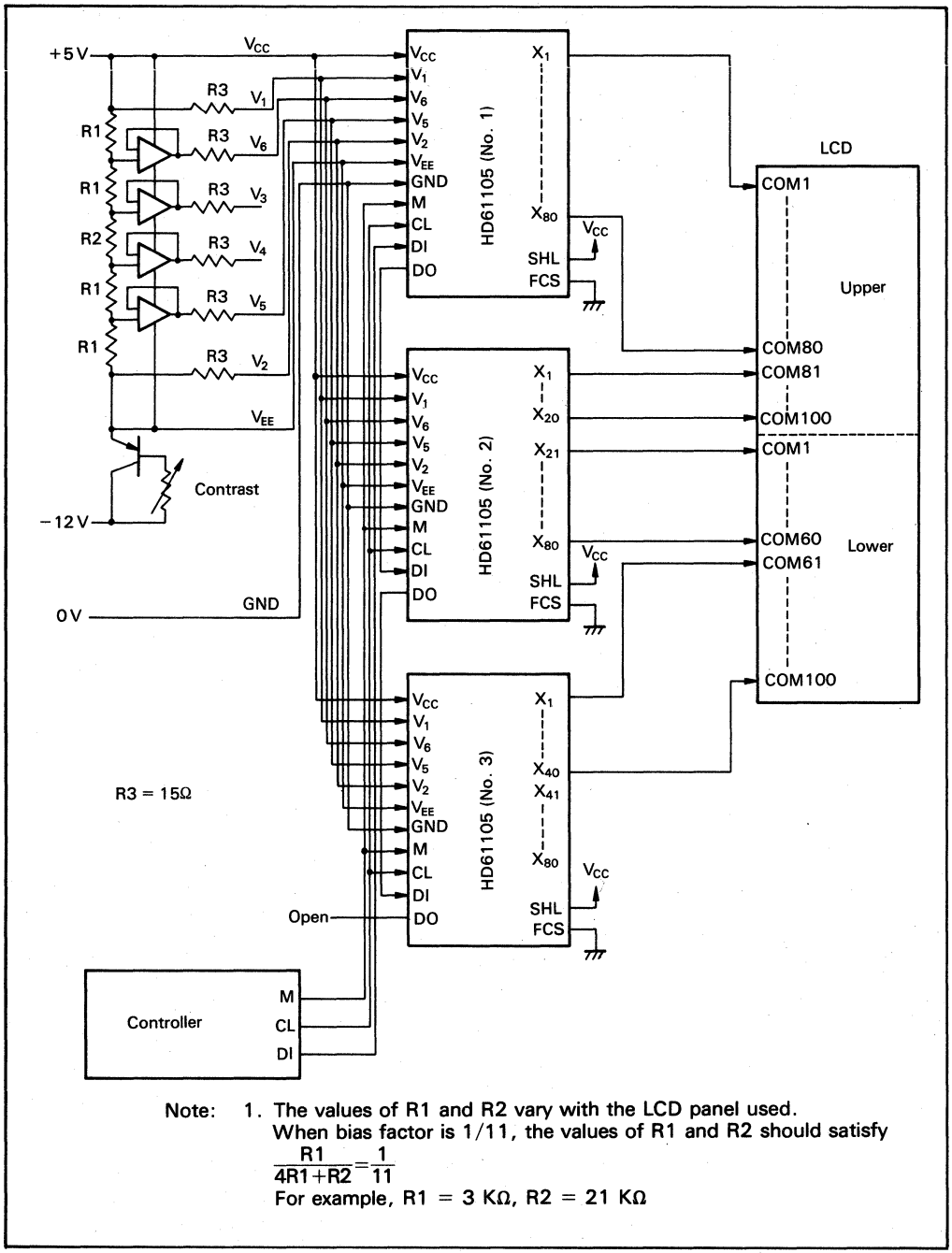


Note: 1. The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/11, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1+R2}=\frac{1}{11}$$

For example, R1 = 3 KΩ, R2 = 21 KΩ

Figure 3 Example of Connection 1 (SHL = V_{CC}, FCS = GND)

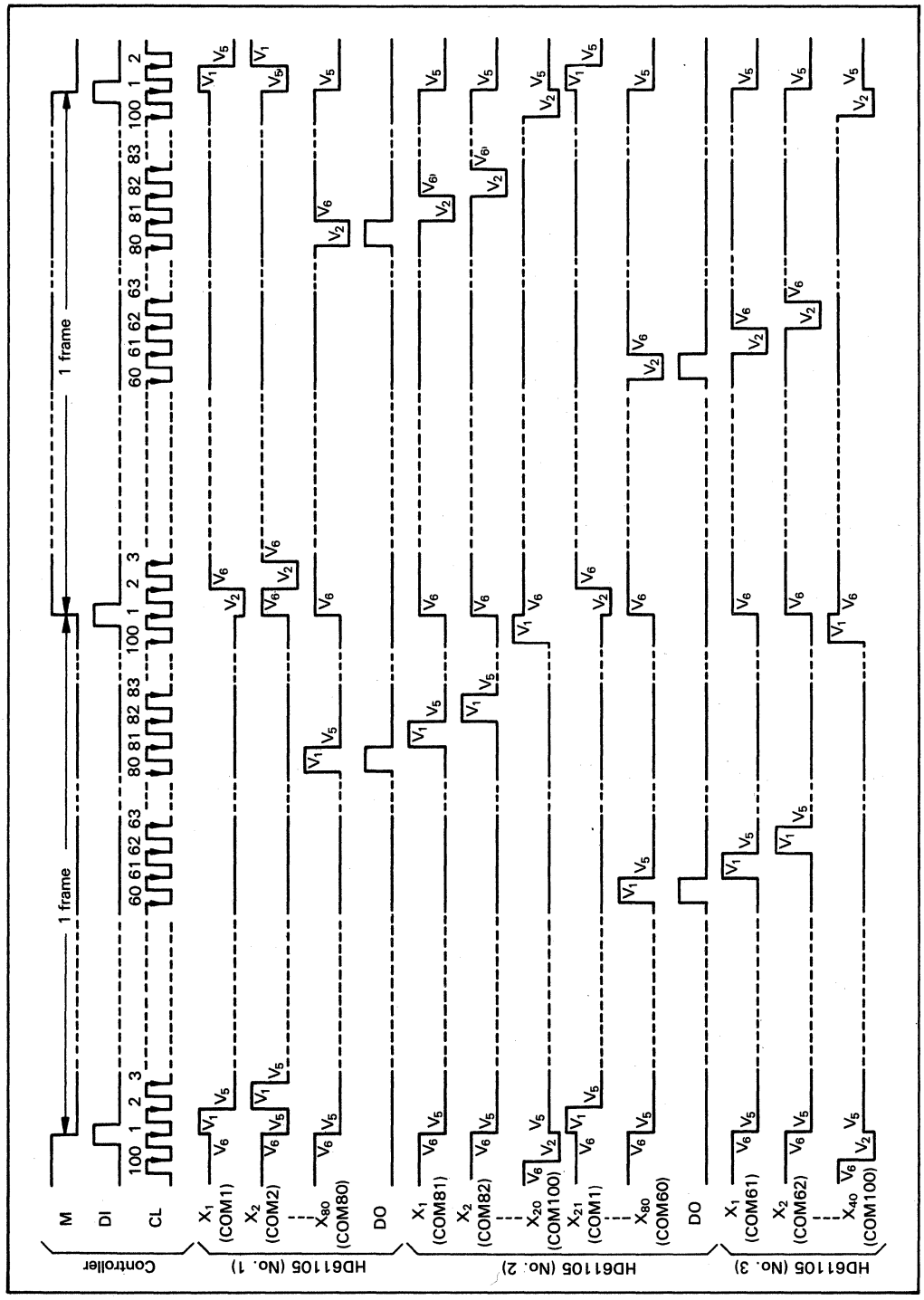
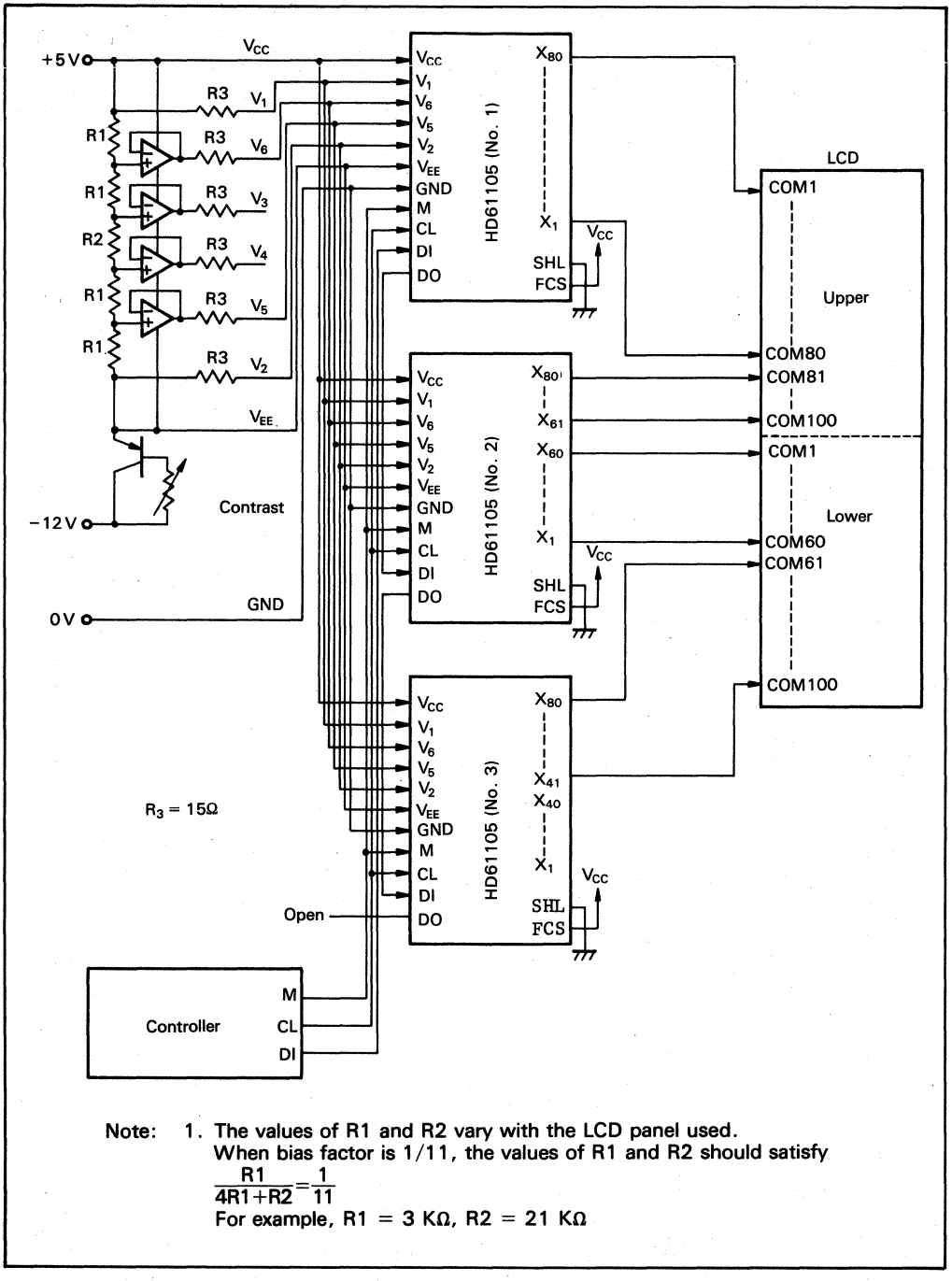


Figure 4 Waveform Example

5



Note: 1. The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/11, the values of R1 and R2 should satisfy
$\frac{R1}{4R1+R2}=\frac{1}{11}$
For example, R1 = 3 KΩ, R2 = 21 KΩ

Figure 5 Example of Connection 2 (SHL = GND, FCS = V_{CC})

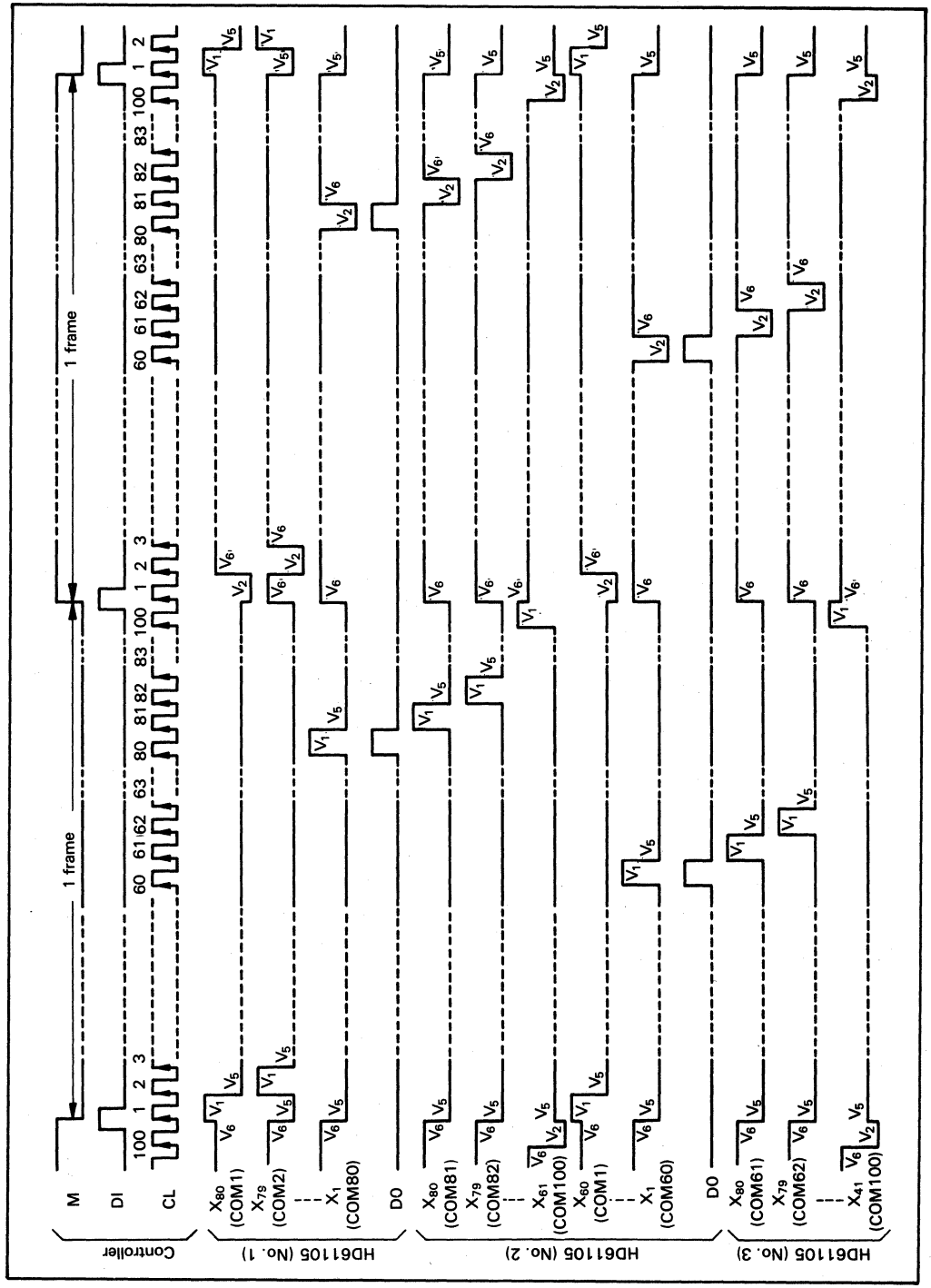


Figure 6 Waveform Example

HD61200
(LCD Driver with 80-Channel Output)

Description

The HD61200 is a column driver LSI for a large-area dot matrix LCD. It employs 1/32 or more duty cycle multiplexing method. It receives serial display data from a micro controller or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

Features

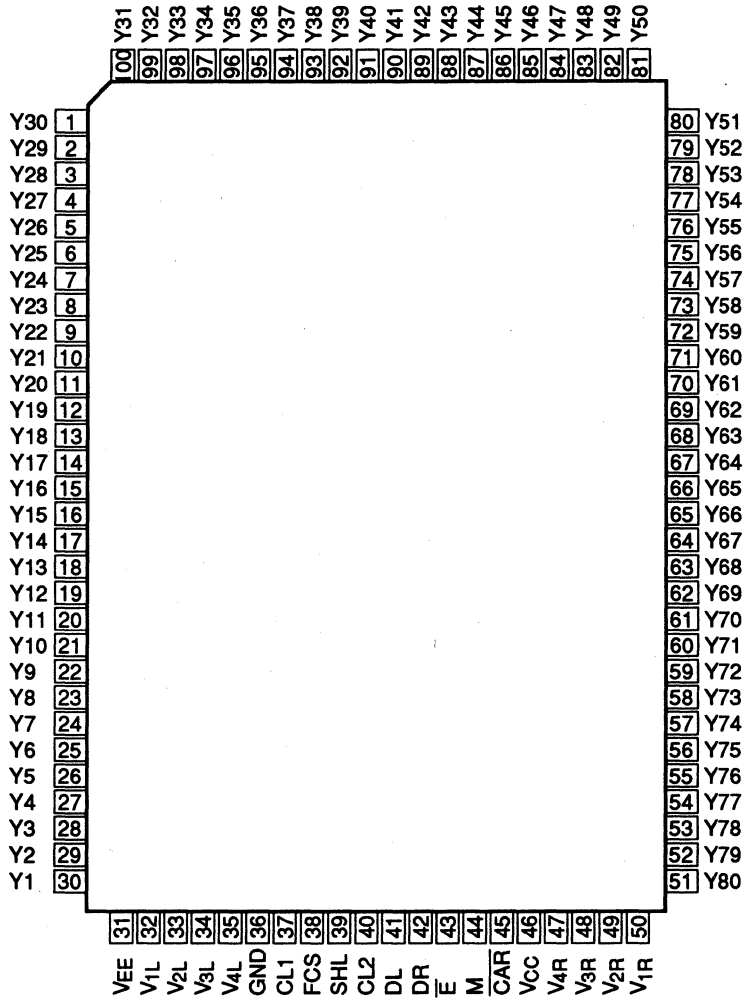
- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Drives liquid crystal panels with 1/32-1/128 duty cycle multiplexing
- Can interface to LCD controllers, HD61830 and HD61830B
- Data transfer rate: 2.5 MHz max
- Power supply: V_{CC}: 5 V ± 10% (Internal logic)
- Power supply voltage for liquid crystal display drive: 8 V to 17 V
- CMOS process
- 100-pin flat plastic package (FP-100)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, $\overline{E}$, and M.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}. Must maintain $V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}$.
Connect a protection resistor of 15 Ω ± 10% to each terminal in series.

Pin Arrangement



(Top view)

5

Electrical Characteristics

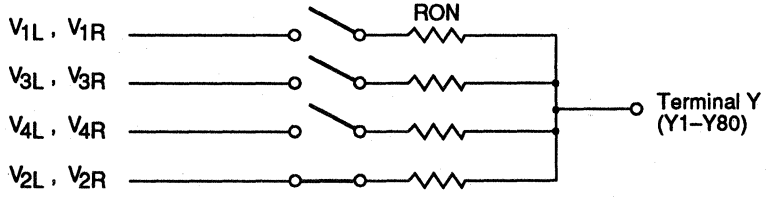
DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – VEE = 8 V to 17 V, Ta = –20 to 75°C)

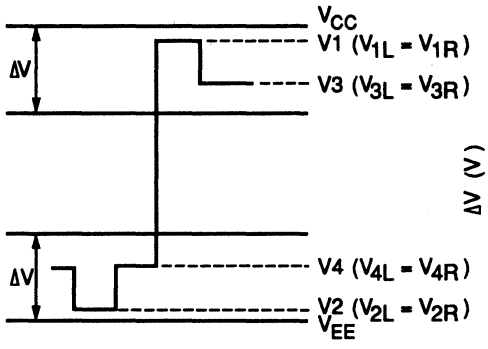
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		1
Input low voltage	V_{IL}	0	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} –0.4	—	—	V	I_{OH} = 400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	2
Driver on resistance	R_{ON}	—	—	7.5	kΩ	Load current = 100 µA	5
Input leakage current	I_{IL1}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–2	—	2	µA	V_{IN} = V_{EE} to V_{CC}	3
Dissipation current (1)	I_{GND}	—	—	1.0	mA		4
Dissipation current (2)	I_{EE}	—	—	0.1	mA		4

Notes:
1. Applies to CL1, CL2, SHL, $\overline{E}$, M, DL, and DR.
2. Applies to $\overline{CAR}$.
3. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.
4. Specified when display data is transferred under following conditions:
   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 35 Hz (frame frequency/2)
   Specified at V_{IH} = V_{CC} (V), V_{IL} = 0 V and load on outputs.
   I_{GND}: currents between V_{CC} and GND.
   I_{EE}: currents between V_{CC} and V_{EE}.
5. Resistance between terminal Y and terminal V (one of V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R} when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition:

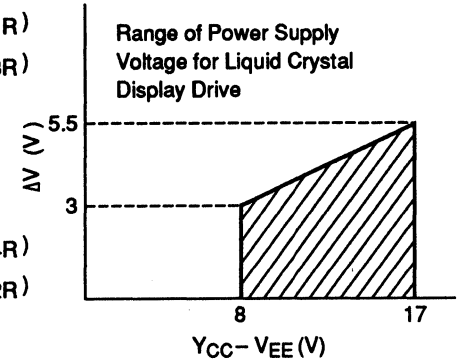
$$V_{CC} - V_{EE} = 17\ V$$
$$V_{1L} = V_{1R},\ V_{3L} = V_{3R} = V_{CC} - 2/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{4L} = V_{4R} = V_{EE} + 2/7\ (V_{CC} - V_{EE})$$



The following here is a description of the range of power supply voltage for liquid crystal display drivers. Apply positive voltage to $V_{1L} = V_{1R}$ and $V_{3L} = V_{3R}$ and negative voltage to $V_{2L} = V_{2R}$ and $V_{4L} = V_{4R}$ within the ΔV range. This range allows stable impedance on driver output (RON). Notice the ΔV depends on power supply voltage V_{CC}–V_{EE}.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

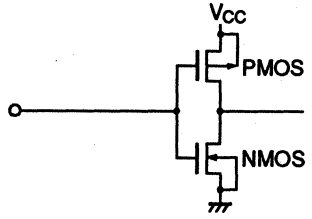


Correlation between Power Supply Voltage V_{CC}– V_{EE} and ΔV

5

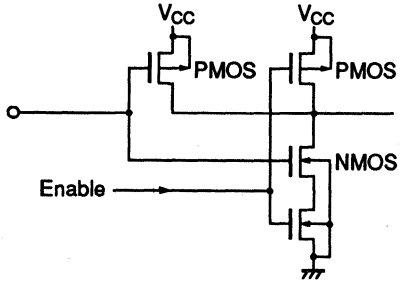
Terminal Configuration

input Terminal

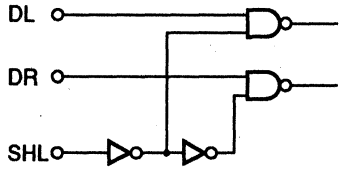


Applicable terminals :
CL1, CL2, SHL, $\overline{E}$, M

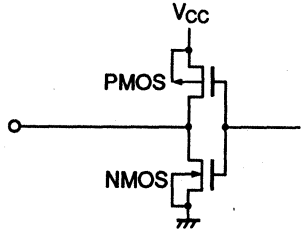
Input Terminal (with Enable)



Applicable terminals: DL, DR

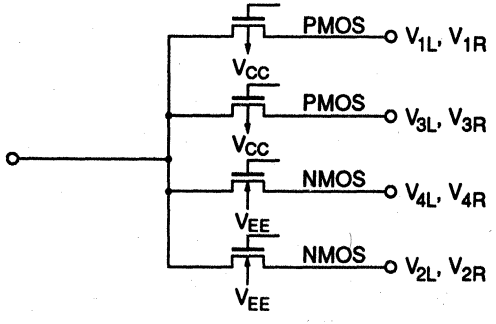


Output Terminal



Applicable terminal: $\overline{CAR}$

Output Terminal



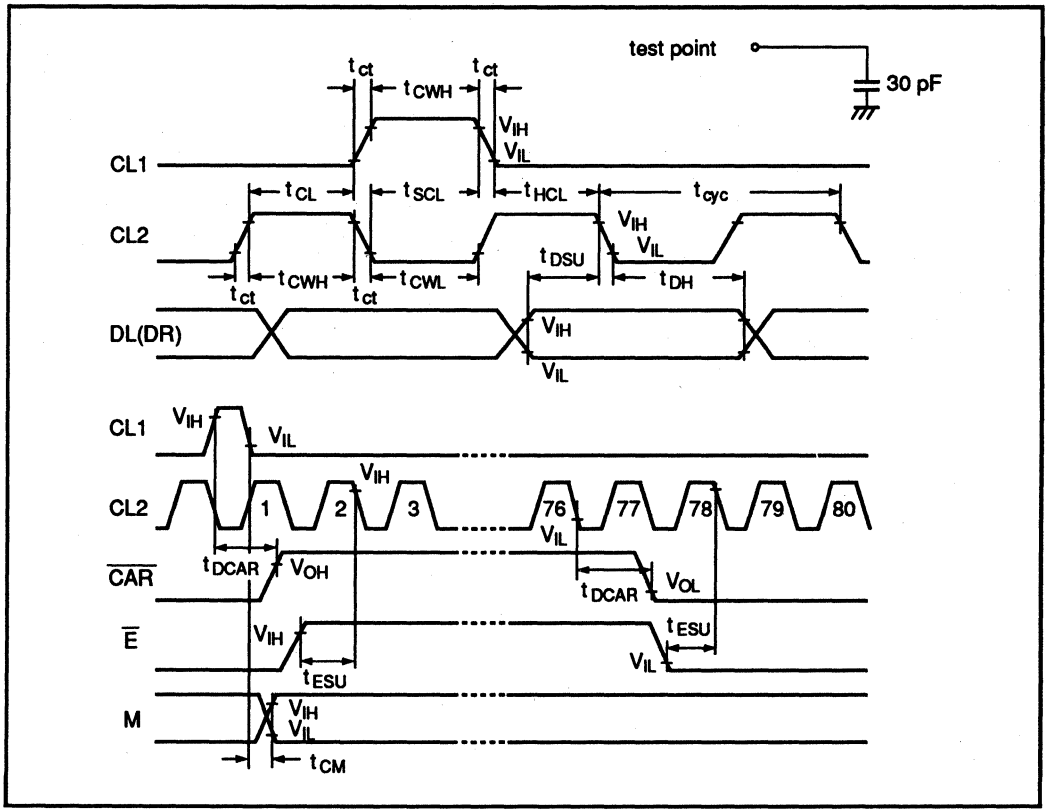
Applicable terminals:
Y1–Y80

AC Characteristics

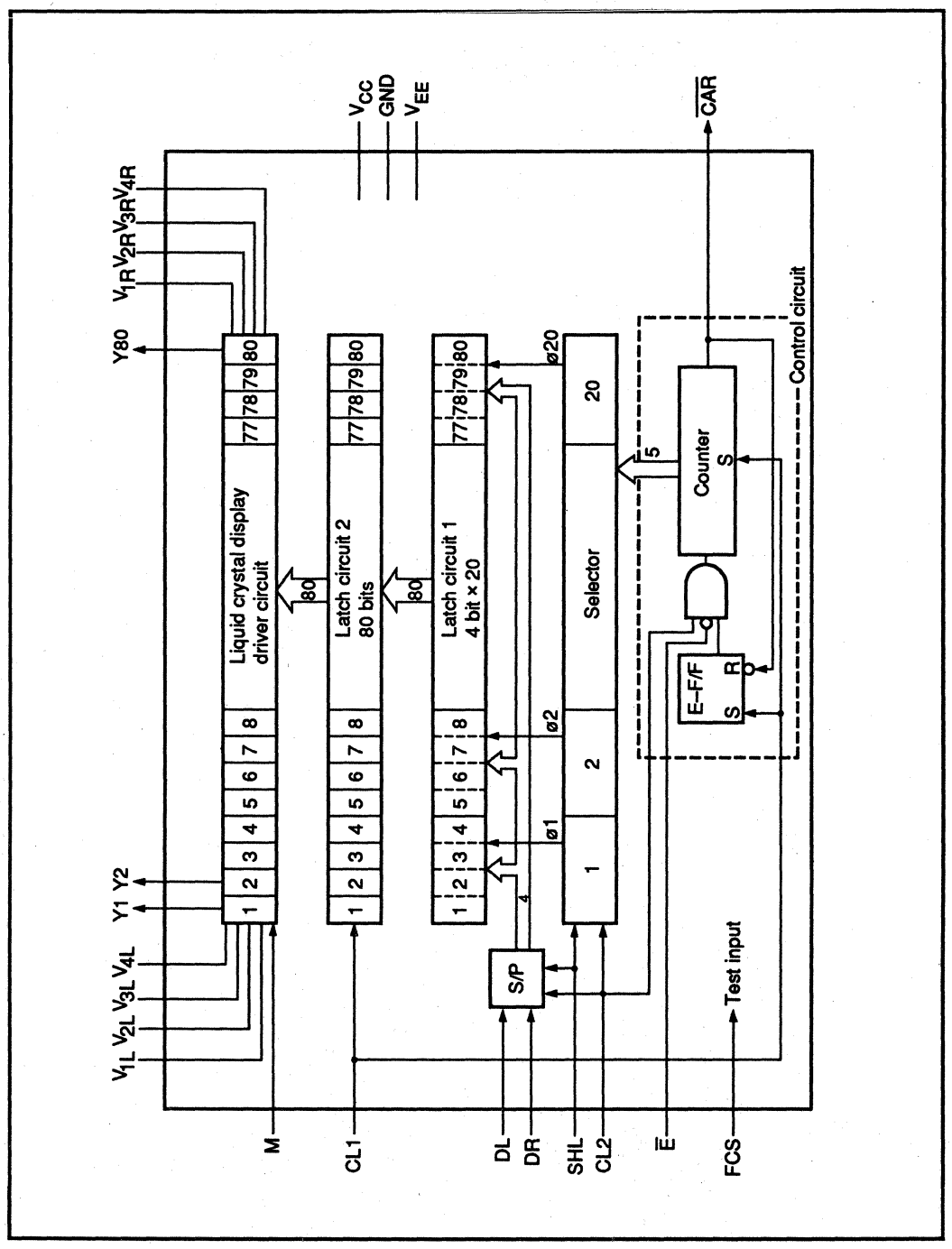
(V_{CC} = 5 V ± 10%, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{CYC}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{Ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
E setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuit is connected for specification:



Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is low level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR.

When SHL is high level, input data from terminal DR without connecting any lines to terminal DL.

80-bit Latch Circuit 1

The 4-bit data is latched at $\phi 1$—$\phi 20$ and output to latch circuit 2. When SHL is low level, the data from DL are latched in order of 1→2→3 ... →80 of each latch. When SHL is high level, they are latched in a reverse order (80→79→78 ... →1).

Selector

The selector decodes output signals from the counter and generates latch clock $\phi 1$ to $\phi 20$. When the LSI is not active, $\phi 1$–$\phi 20$ are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E–F/F (enable F/F) indicates 1, S/P conversion is started by inputting low level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into low level and E–F/F is reset to 0, and consequently the conversion stops. E–F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at high level of CL1.

The counter consists of 7 bits, and the output signals upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into high level at the rise of CL1. The number of bits that can be S/P-converted can be increased by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61200.

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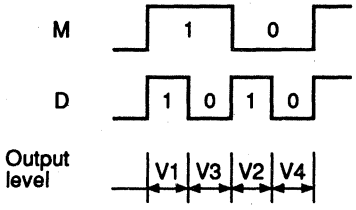
Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}–V_{4L} V_{1R}–V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1-Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2 V3, and V4. Relation among output level, M, and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Synchronous signal (a counter is reset at high level). Latch clock of display data (falling edge triggered). Synchronized with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge triggered.
DL, DR	2	I	Controller	Input of serial display data (D). (D) / Liquid Crystal Driver Output / Liquid Crystal Display 1 (High level) / Selection level / On 0 (Low level) / Non-selection level / Off
SHL	1	I	V_{CC} or GND	Selects the shift direction of serial data. When the serial data (D) is input in order of D1→ ... →D80, the relations between the data (D) and output Y are as follows: SHL: Y1 / Y2 / Y3 / .... / Y80 Low: D1 / D2 / D3 / .... / D80 High: D80 / D79 / D78 / .... / D1

Terminal Functions Description (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
SHL (cont)	1	I	V_{CC} or GND	When SHL is low, data is input from the DL terminal. No lines should be connected to the DR terminal. When SHL is high, the relation between DL and DR reverses.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61200	Controls the S/P conversion. The operation stops on high level, and the S/P conversion starts on low level.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61200	Used for cascade connection with the HD61200 to increase the number of bits that can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

Operation of the HD61200

The following describes an LCD panel with 64 x 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61200s. Figure 2 is a time chart of HD61200 I/O signals.

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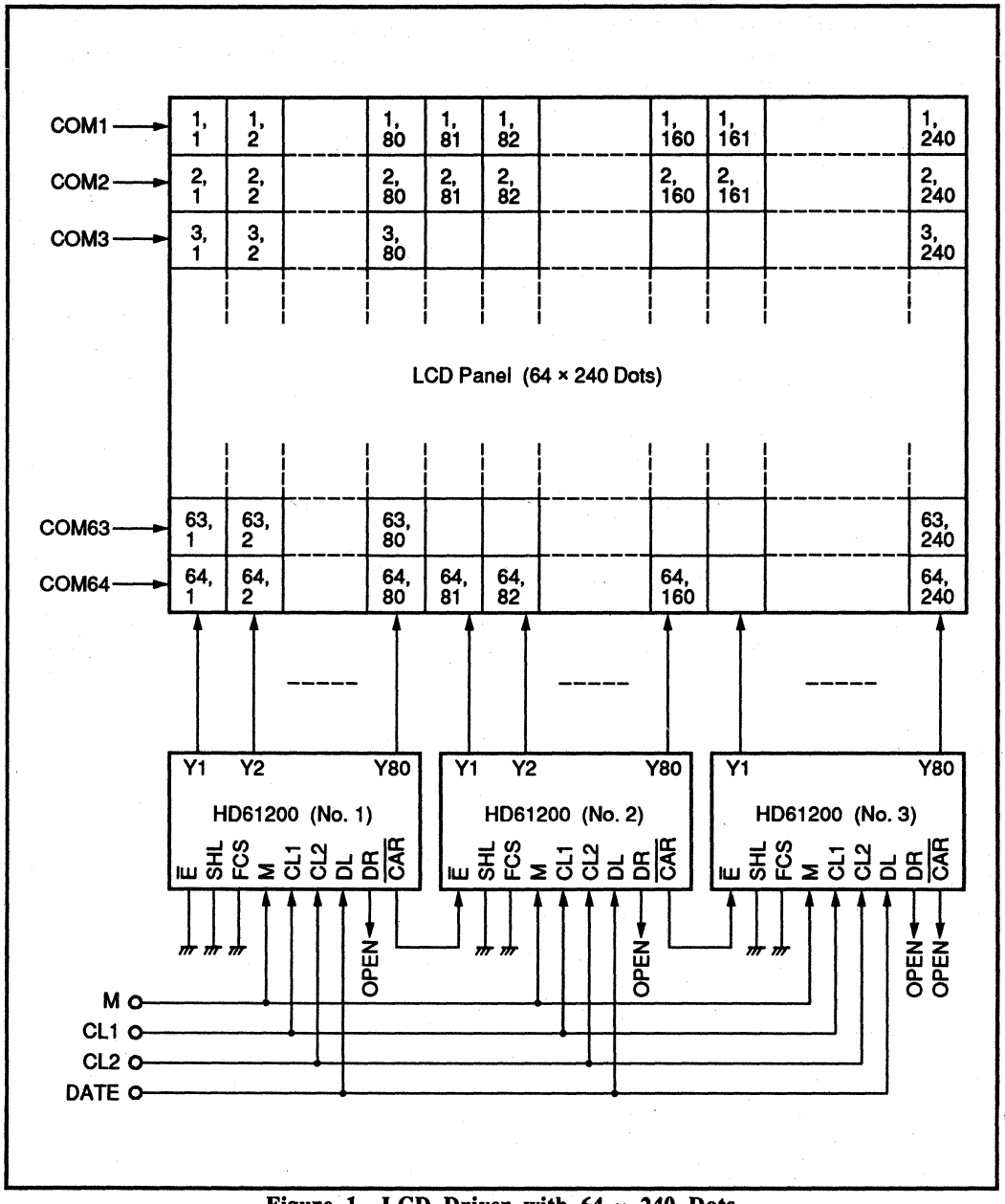

Figure 1 LCD Driver with 64 × 240 Dots

Cascade three HD61200s. Input data to the DL terminal of No. 1, No. 2, and No. 3. Connect $\overline{E}$ of No. 1 to GND. Don't connect any lines to $\overline{CAR}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61203. (m, n) of LCD panel is the address corresponding to each dot.

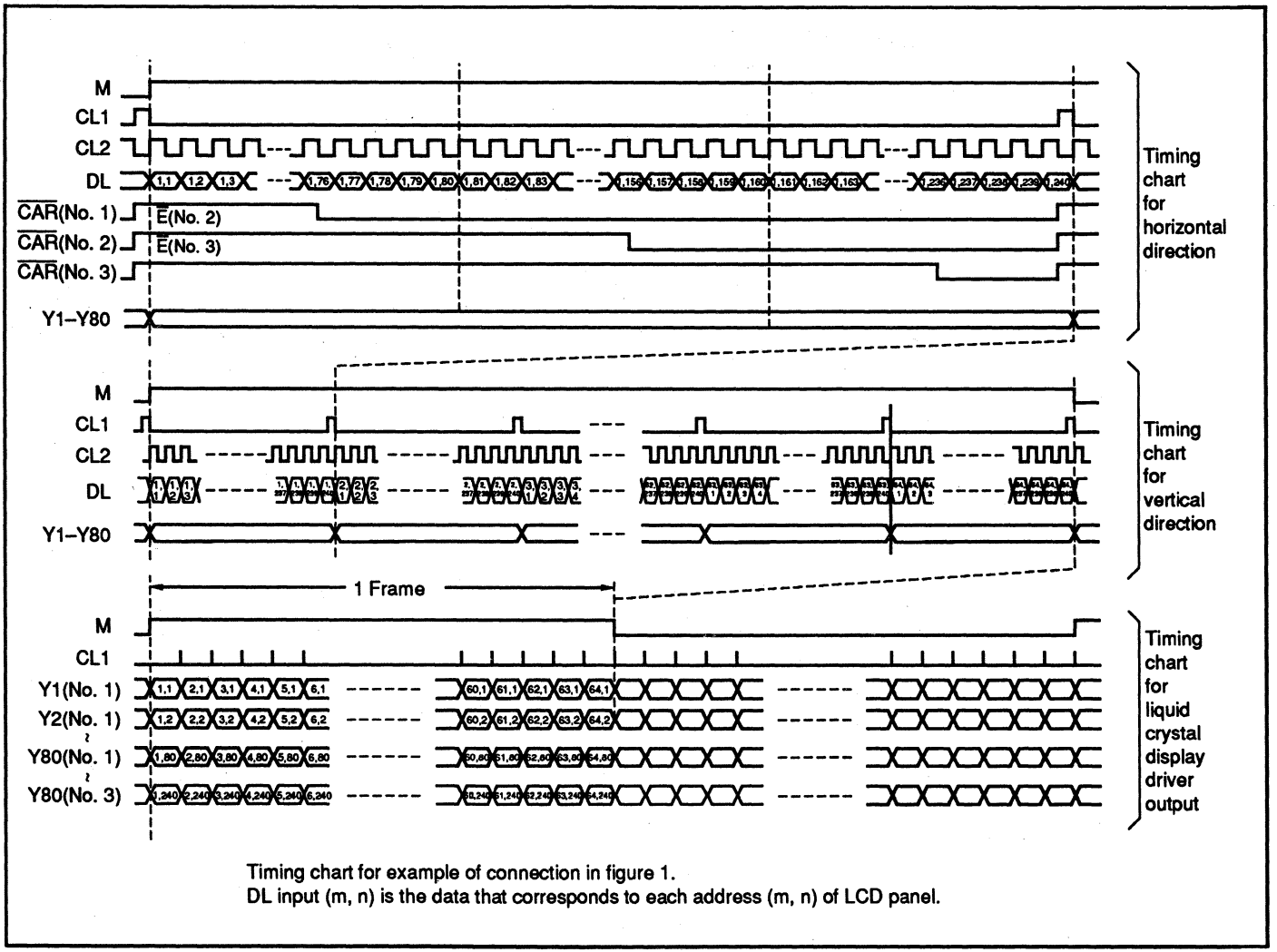

Figure 2 HD61200 Timing Chart

Timing chart for example of connection in figure 1.
DL input (m, n) is the data that corresponds to each address (m, n) of LCD panel.

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Application Example

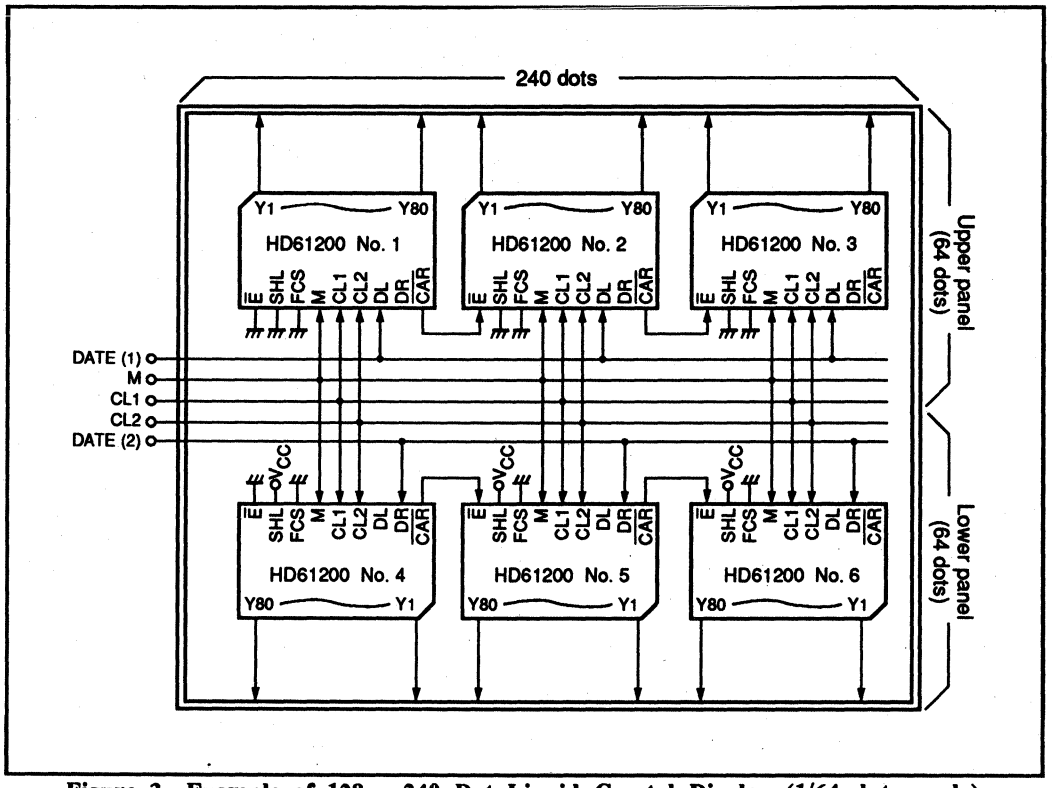


Figure 3 Example of 128 × 240 Dot Liquid Crystal Display (1/64 duty cycle)

The liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61200s No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA (1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow \text{--} \rightarrow Y_{80}$ terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow \text{--} \rightarrow Y_{80}$ of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow \text{--} \rightarrow Y_{80}$ of No. 3 in the order in which they were input (in the case of SHL = low). HD61200s No. 4 to No. 6 drive the lower half. Serial data, which are input from DATA (2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow \text{--} \rightarrow Y_1$ of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow \text{--} \rightarrow Y_1$ of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow \text{--} \rightarrow Y_1$ of No. 6 in the order in which they were input (in the case of SHL = high).

As shown in this example, a PC board for a display divided into upper and lower half can be easily designed by using the SHL terminal effectively.

HD61202
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61202 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro controller in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to the on/off state of a dot of a liquid crystal display to provide more flexible than character display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

The HD61202, which is produced in the CMOS process, can complete portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61203.

Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
  - RAM bit data 1: On
  - RAM bit data 1: Off
- Internal display RAM address counter preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty cycle:
  Drives liquid crystal panels with 1/32–1/64 duty cycle multiplexing
- Wide range of instruction function:
  Display Data Read/Write, Display On/Off, Set Address, Set Display Start Line, Read Status
- Lower power dissipation: during display 2 mW max
- Power supply: V_{CC}: 5 V ± 10%
- Liquid crystal display driving voltage: 8 V to 17.0 V
- CMOS process
- 100-pin flat plastic package (FP-100)

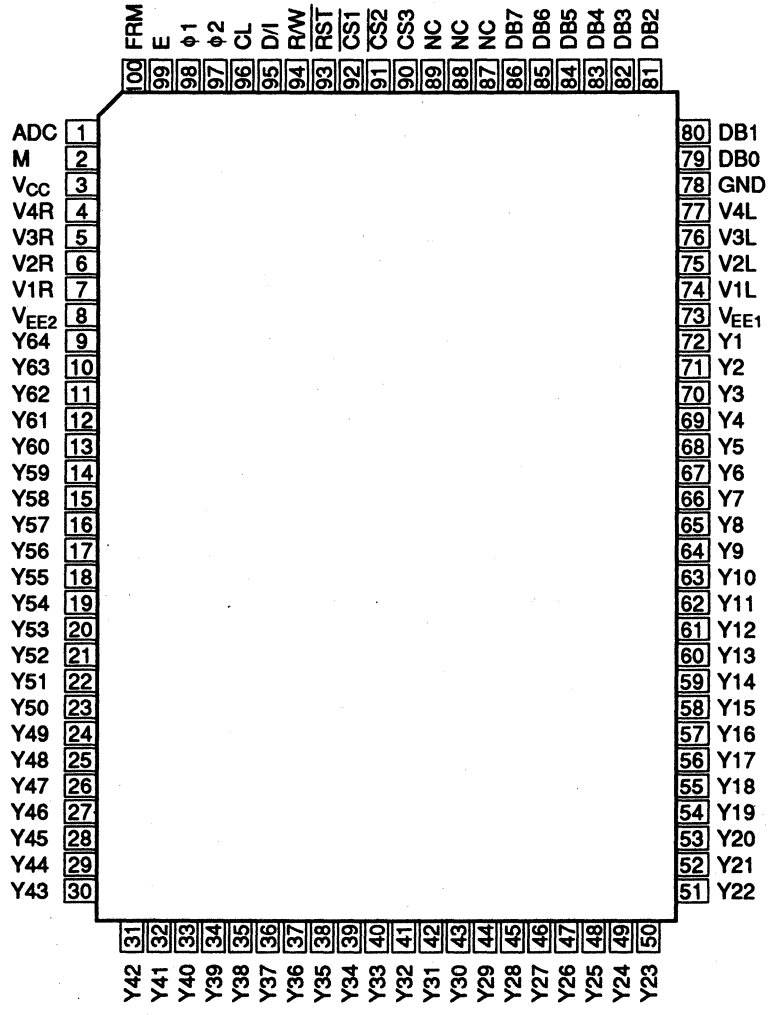
5

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	2
	V_{EE1} V_{EE2}	V_{CC} –19.0 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminla voltage (2)	V_{T2}	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them within the recommended operation conditions.
Using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
Maintain
$V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, $\phi1$, $\phi2$, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.

Pin Arrangement



(Top view)

5

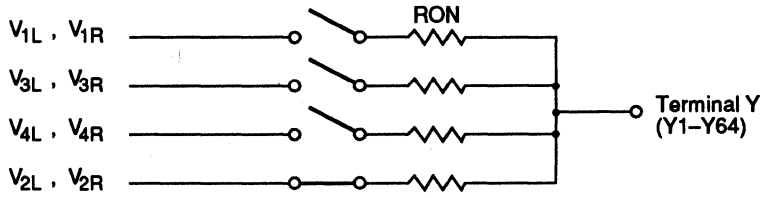
Electrical Characteristics

(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{CC} – V_{EE} = 8 to 17.0 V, Ta = –20 to +75°C)

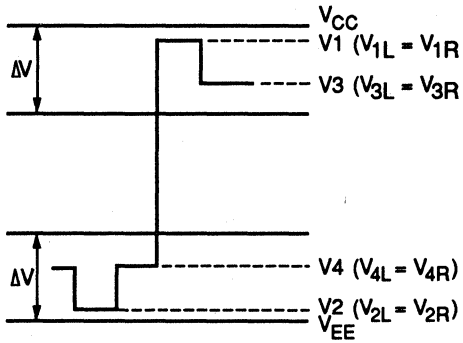
Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IHC}	0.7 × V_{CC}	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	0.3 × V_{CC}	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –205 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA	3
Input leakage current	I_{IL}	–1.0	—	+1.0	µA	Vin = GND–V_{CC}	4
Three-state (off) input current	I_{TSL}	–5.0	—	+5.0	µA	Vin = GND–V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2.0	—	+2.0	µA	Vin = V_{EE} –V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	kΩ	V_{CC} – V_{EE} = 15 V ±I_{LOAD} = 0.1 mA	8
Dissipation current	I_{CC} (1)	—	—	100	µA	During display	7
	I_{CC} (2)	—	—	500	µA	During access access cycle = 1 MHz	7

Notes:
1. Applies to M, FRM, CL, $\overline{RST}$, ϕ1, and ϕ2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Specified when liquid crystal display is in 1/64 duty cycle mode.
   Operation frequency f_{CLK} = 250 kHz (ϕ1 and ϕ2 frequency)
   Frame frequency f_M = 70 Hz (FRM frequency)
   Specified in the state of
   Output terminal: not loaded
   Input level: V_{IH} = V_{CC} (V)
   V_{IL} = GND (V)
   Measured at V_{CC} terminal
8. Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y1 to Y64. This value is specified under the following condition:

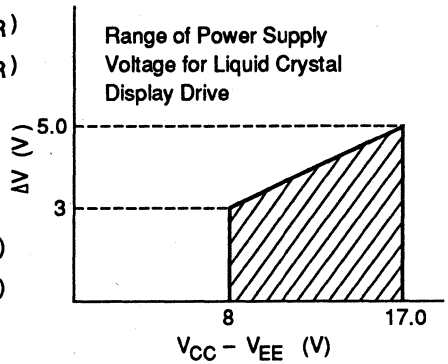
$$V_{CC} - V_{EE} = 15.5\ V$$
$$V_{1L} = V_{1R},\ V_{3L} = V_{3R} = V_{CC} - 2/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{4L} = V_{4R} = V_{CC} + 2/8\ (V_{CC} - V_{EE})$$



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V3L = V3R and negative voltage to V2L = V2R and V4L = V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

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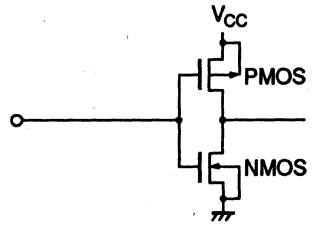
Terminal Configuration

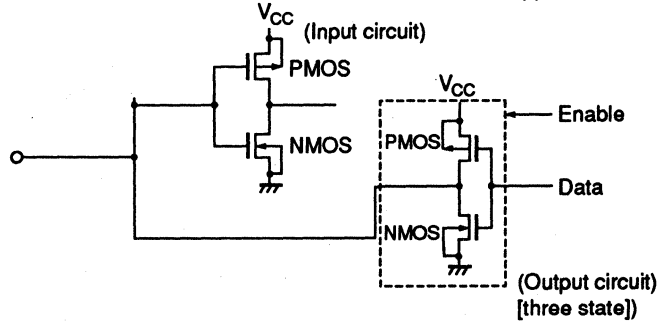
Input Terminal



Applicable terminals :
M, FRM, CL, $\overline{RST}$, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3,
E, R/W, D/I, ADC

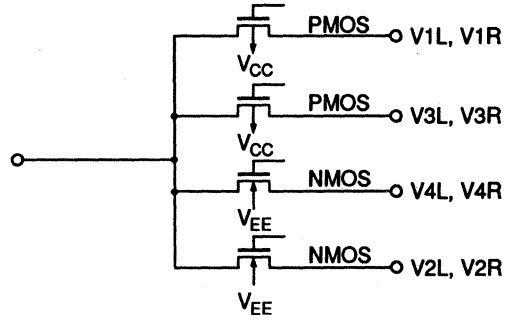
Input/Output Terminal

Applicable terminals: DB0–DB7



Output Terminal

Applicable Terminals:
Y1–Y64



Interface AC Characteristics

MPU Interface
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	—	—	ns	1, 2
E high level width	P_{WEH}	450	—	—	ns	1, 2
E low level width	P_{WEL}	450	—	—	ns	1, 2
E rise time	tr	—	—	25	ns	1, 2
E fall time	tf	—	—	25	ns	1, 2
Address setup time	t_{AS}	140	—	—	ns	1, 2
Address hold time	t_{AH}	10	—	—	ns	1, 2
Data setup time	t_{DSW}	200	—	—	ns	1
Data delay time	t_{DDR}	—	—	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	—	—	ns	1
Data hold time (Read)	t_{DHR}	20	—	—	ns	2

Notes: 1.

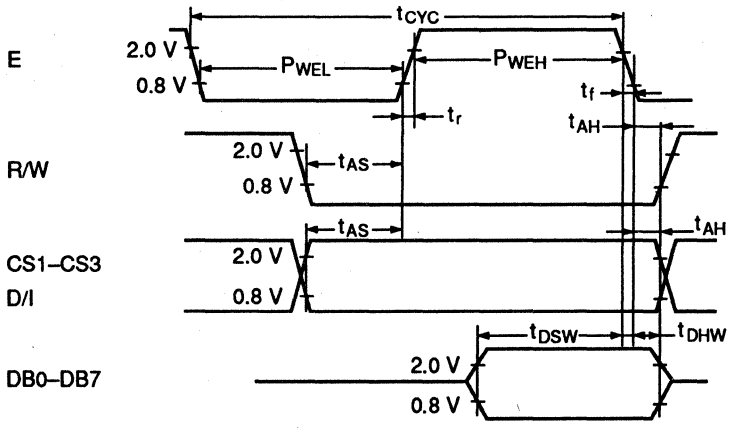


Figure 1 CPU Write Timing

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Notes: 2.

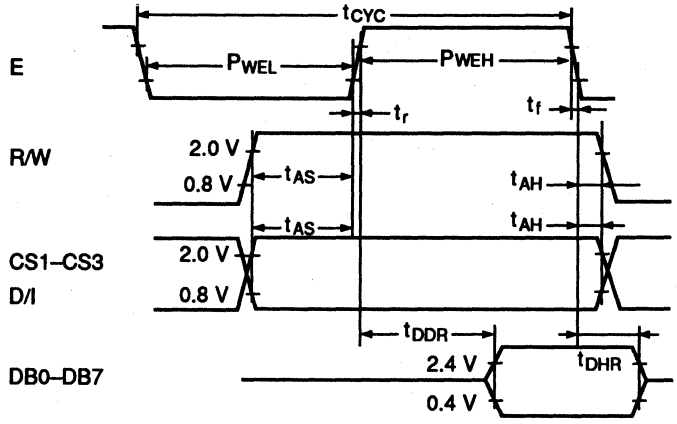
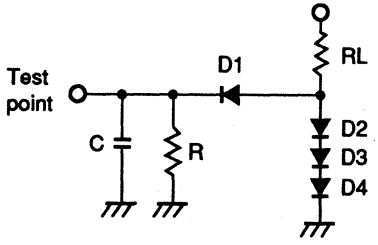


Figure 2 CPU Read Timing

3. DB0–DB7: load circuit



RL = 2.4 k Ω
R = 11 k Ω
C = 130 pF (including jig capacitance)
Diodes D1–D4 are all 1S2074 Ⓗ.

Clock Timing
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
ϕ1, ϕ2 cycle time	tcyc	2.5	—	20	µs	Fig. 3
ϕ1 low level width	$t_{WL\phi1}$	625	—	—	ns	Fig. 3
ϕ2 low level width	$t_{WL\phi2}$	625	—	—	ns	Fig. 3
ϕ1 high level width	$t_{WH\phi1}$	1875	—	—	ns	Fig. 3
ϕ2 high level width	$t_{WH\phi2}$	1875	—	—	ns	Fig. 3
ϕ1—ϕ2 phase difference	t_{D12}	625	—	—	ns	Fig. 3
ϕ2—ϕ1 phase difference	t_{D21}	625	—	—	ns	Fig. 3
ϕ1, ϕ2 rise time	tr	—	—	150	ns	Fig. 3
ϕ1, ϕ2 fall time	tf	—	—	150	ns	Fig. 3

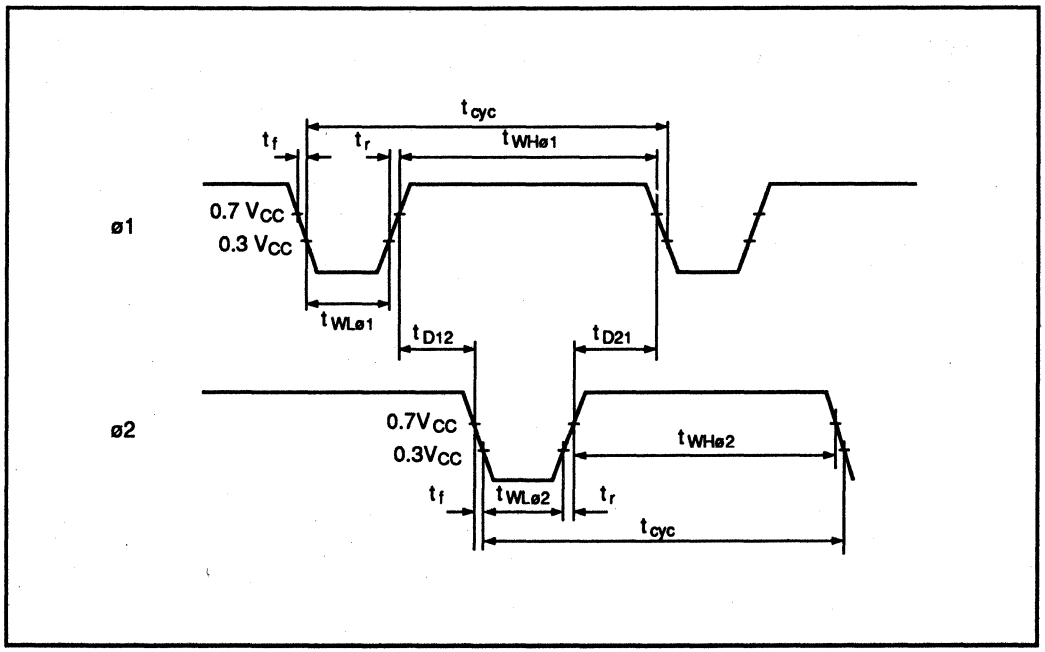


Figure 3 External Clock Waveform

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Display Control Timing
(GND = 0V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75 °C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
FRM delay time	t_{DFRM}	–2	—	+2	µs	Fig. 4
M delay time	t_{DM}	–2	—	+2	µs	Fig. 4
CL low level width	t_{WLCL}	35	—	—	µs	Fig. 4
CL high level width	t_{WHCL}	35	—	—	µs	Fig. 4

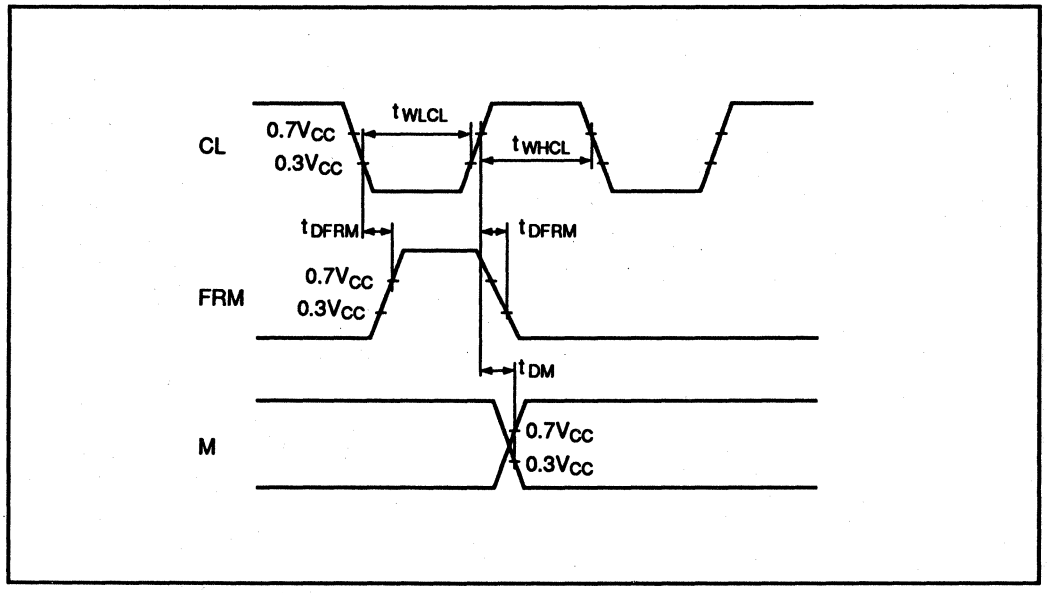
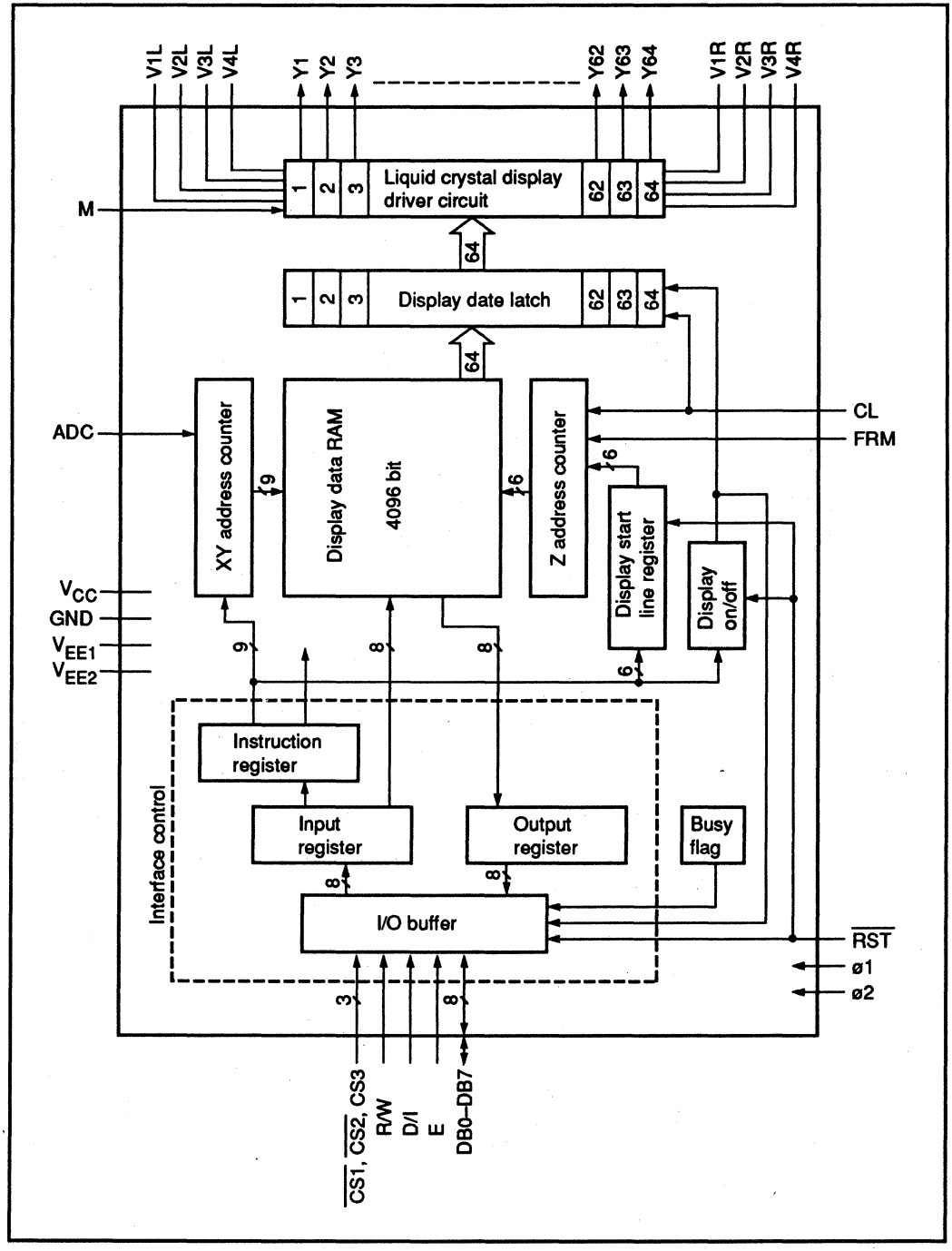


Figure 4 Display Control Signal Waveform

Block Diagram



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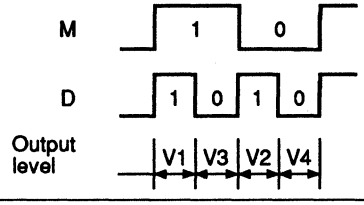
Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is: GND = 0 V V_{CC} = 5 V ±10%
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is $V_{CC} - V_{EE}$ = 8 to 17.0 V. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal Name: $\overline{CS1}$ = L, $\overline{CS2}$ = L, CS3 = H Condition: L, L, H
E	1	I	MPU	Enable. At write(R/W = Low): Data of DB0 to DB7 is latched at the fall of E. At read(R/W = High): Data appears at DB0 to DB7 while E is at high level.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the CPU. When E = high, CS1, CS2 = low and CS3 = high. R/W = Low: DB0 to DB7 can accept at fall of E when CS1, CS2 = low and CS3 = high.
D/I	1	I	MPU	Data/instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.

Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
ADC	1	I	V_{CC}/GND	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1: $0, Y64: $63 ADC = Low: Y64: $0, Y1: $63
DB1-DB7	8	I/O	MPU	Data bus, three-state I/O common terminal.
M	1	I	HD61203	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61203	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes the common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61203	Synchronous signal to latch display data. The rising CL signal increments the display output address counter and latches the display data.
ϕ1, ϕ2	2	I	HD61203	2-phase clock signal for internal operation. The ϕ1 and ϕ2 clocks are used to preform operations (I/O of display data and execution of instructions) other than display.
Y1-Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins outputs light on level when 1 is in the display RAM, and light off level when 0 is it. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level. 1. On/off register 0 set (display off) 2. Display start line register line 0 set (displays from line 0) After releasing reset, this condition can be changed only by instruction.
NC	3		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

5

Function of Each Block

Interface Control

1. I/O buffer

Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (Most significant bit)

DB0: LSB (Least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC; that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively of $\overline{CS1}$ to CS3.

2. Register

Both input register and output register are provided to interface to an MPU whose speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (table 1).

a. Input register

The input register is used to store data temporarily before writing it into display data RAM.

The data from MPU is written into the input register, then into display data RAM automatically by internal operation. When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of the E signal.

b. Output register

The output register is used to store data temporarily that is read from display data RAM. To read out the data from output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With the read display data instruction, data stored in the output register is output while E is high level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.

The contents in the output register are rewritten by the read display data instruction, but are held by address set instruction, etc.

Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 5 shows the CPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

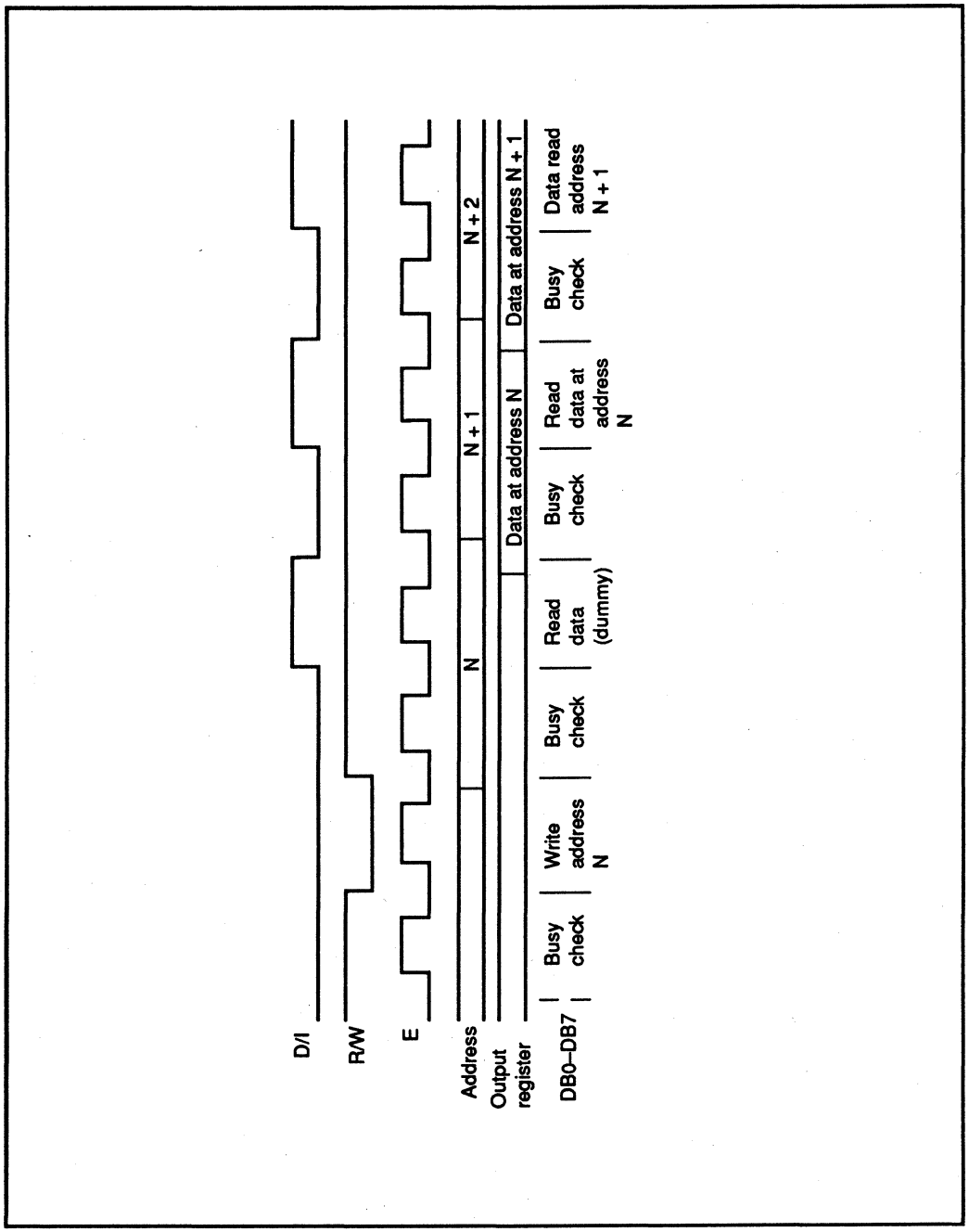


Figure 5 CPU Read Timing

Busy Flag

Busy flag = 1 indicates that HD61202 is operating and no instructions except status read instruction can be accepted. The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing instructions.

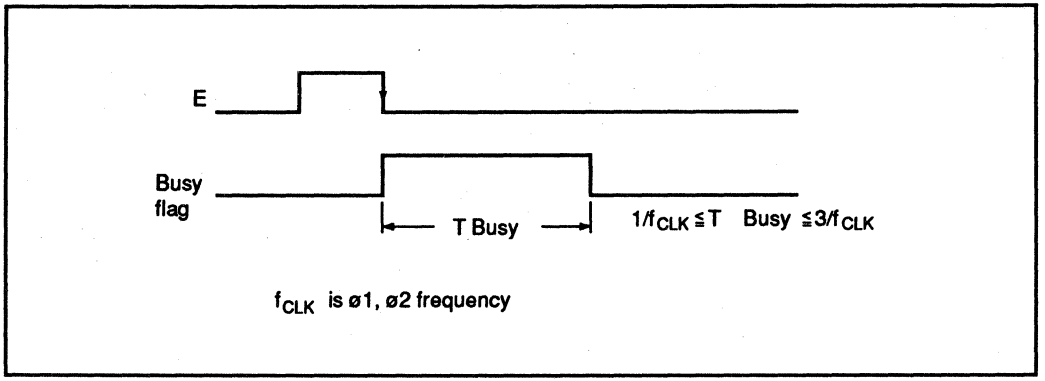


Figure 6 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by status read instruction. Display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, CL signal (display synchronous signal) should be input correctly.

Display Start Line Register

The display start line register specifies the line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by the display start line set instruction. When high level of the FRM signal starts the display, the information in this register is transferred to the Z address counter, which controls the display address, presetting the Z address counter.

X, Y Address Counter

A 9-bit counter which designates addresses of the internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set to each address by the respective instructions.

1. X address counter
Ordinary register with no count functions. An address is set by instruction.

2. Y address counter
An address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment pins can be reversed by ADC signal.

As the ADC signal controls the Y address counter, reversing of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Figure 7 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

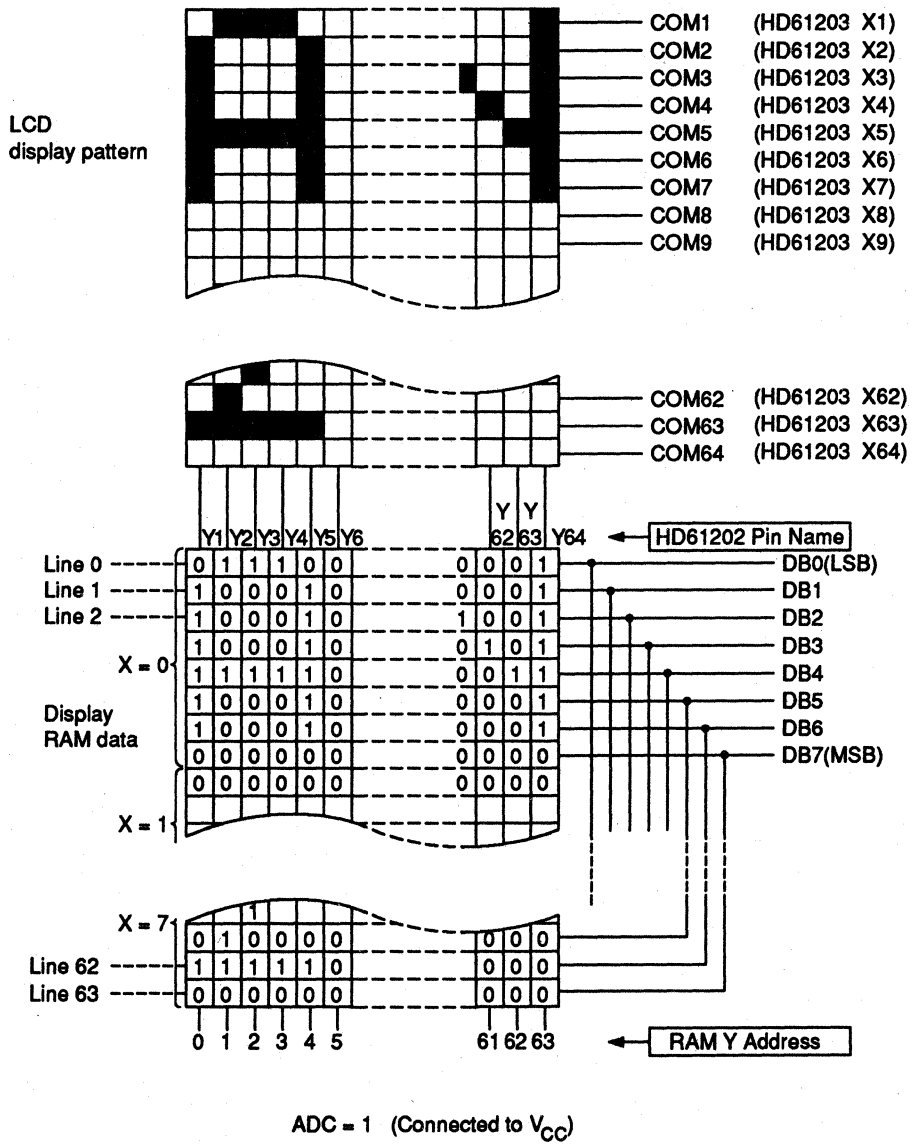


Figure 7 Relation between RAM Data and Display

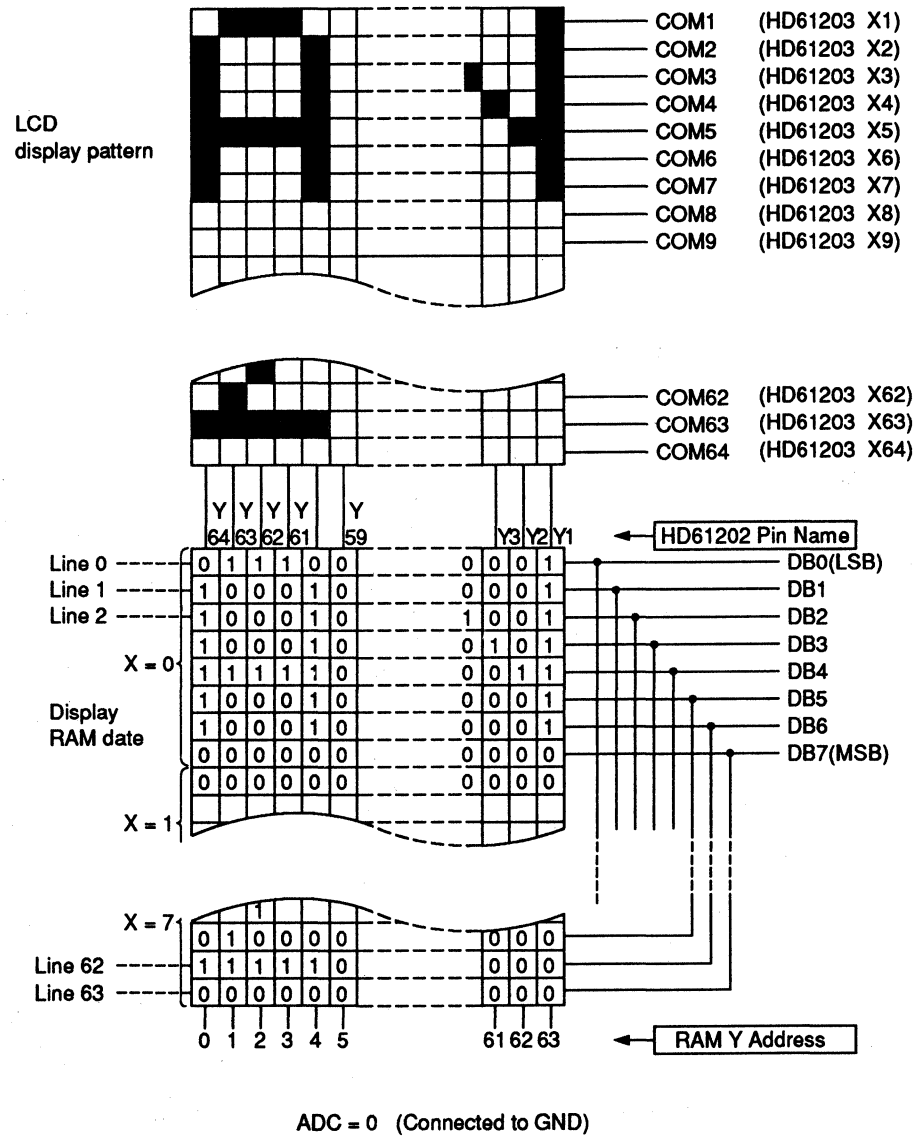


Figure 7 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At the high level of FRM, the contents of the display start line register is preset at the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit. Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal at low level when turning power on.

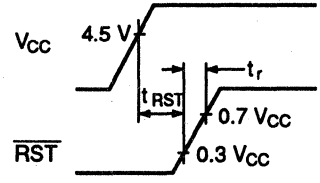
1. Display off
2. Set display start line register line 0.

While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (Ready) by status read instruction. The conditions of power supply at initial power up are shown in table 1.

Table 1 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	μs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 2 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal, and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from the MPU.
These explanations are detailed in the following pages. Generally, there are following three kinds of instructions:

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction is used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is proof that an instruction is not being excuted.

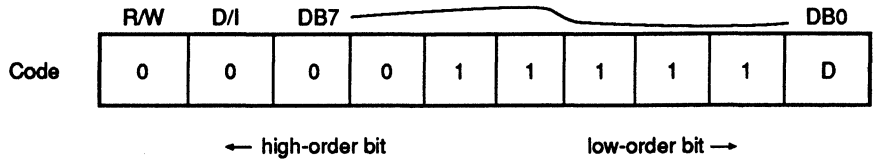
Table 2 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM at the page (X address) register.
Set address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM. Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: 1. Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

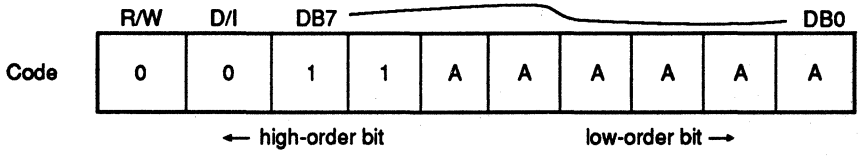
Detailed Explanation

Display on/off



The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display start line



Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 8 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

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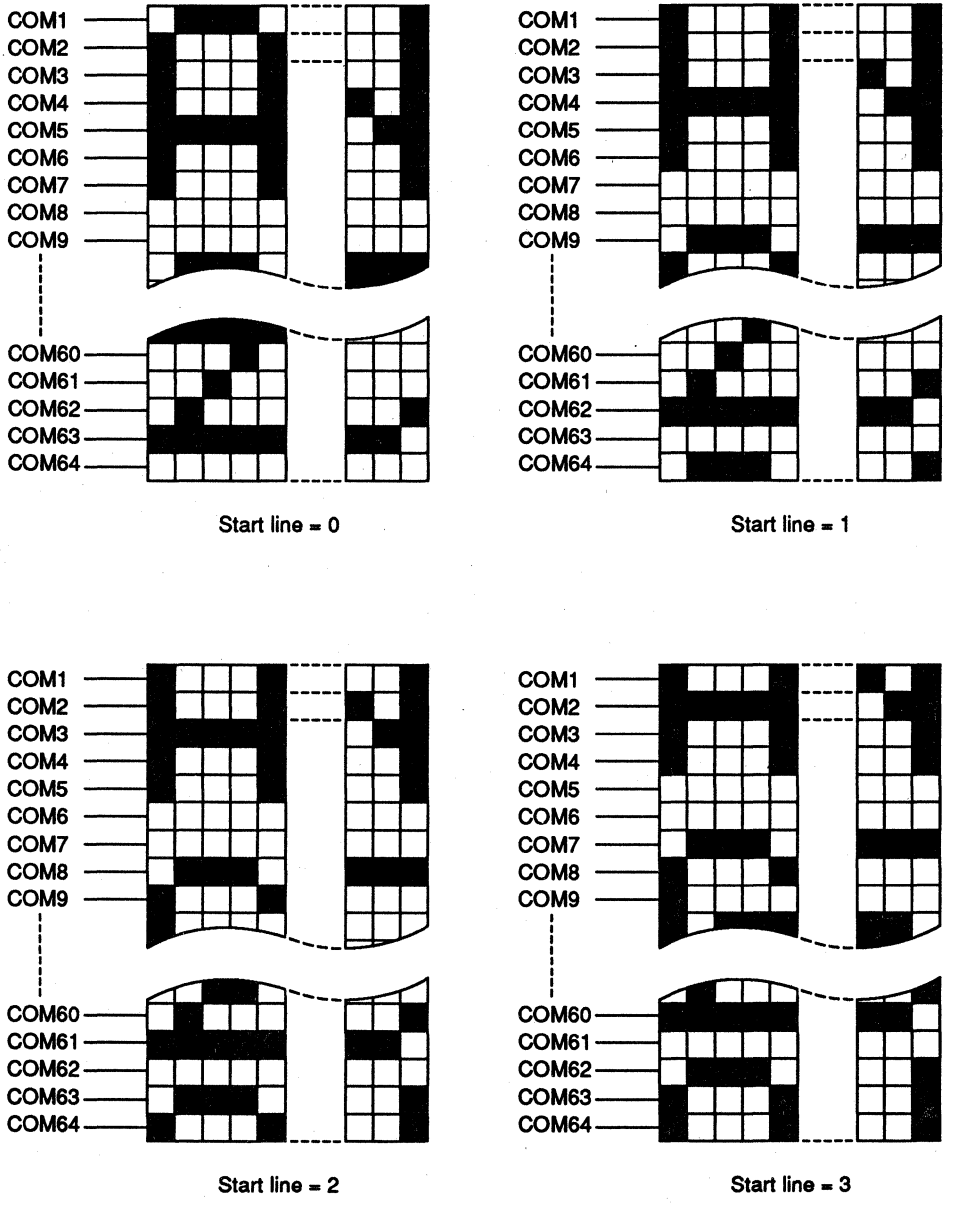

Figure 8 Relation Between Start Line and Display

Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order bit low-order bit →

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 9.

Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order bit low-order bit →

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

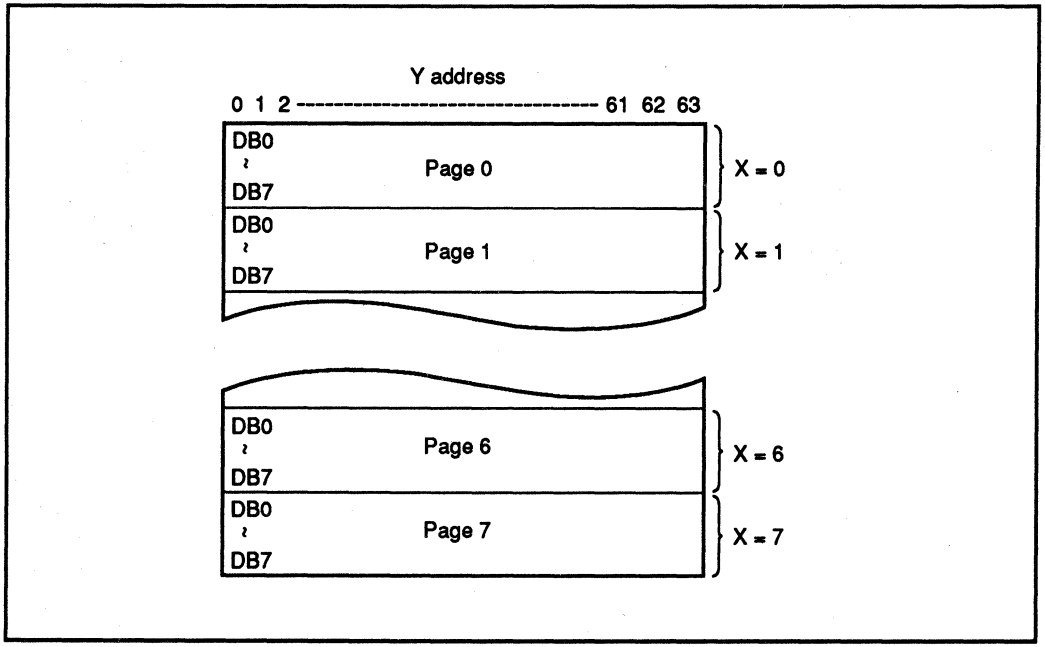

Figure 9 Address Configuration of Display Data RAM

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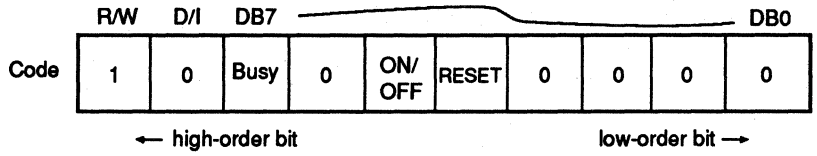
Status Read

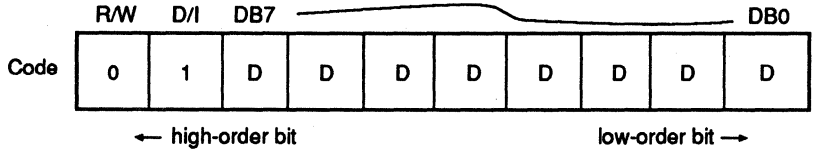


Busy: When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

ON/OFF: Shows the liquid crystal display conditions: on condition or off condition.
When ON/OFF is 1, the display is in off condition.
When ON/OFF is 0, the display is in on condition.

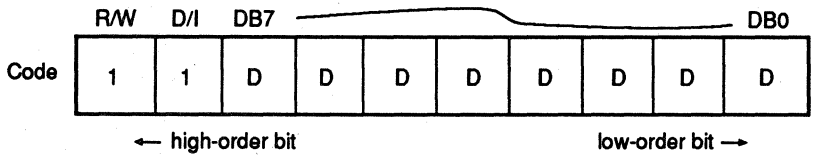
RESET: RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data



Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

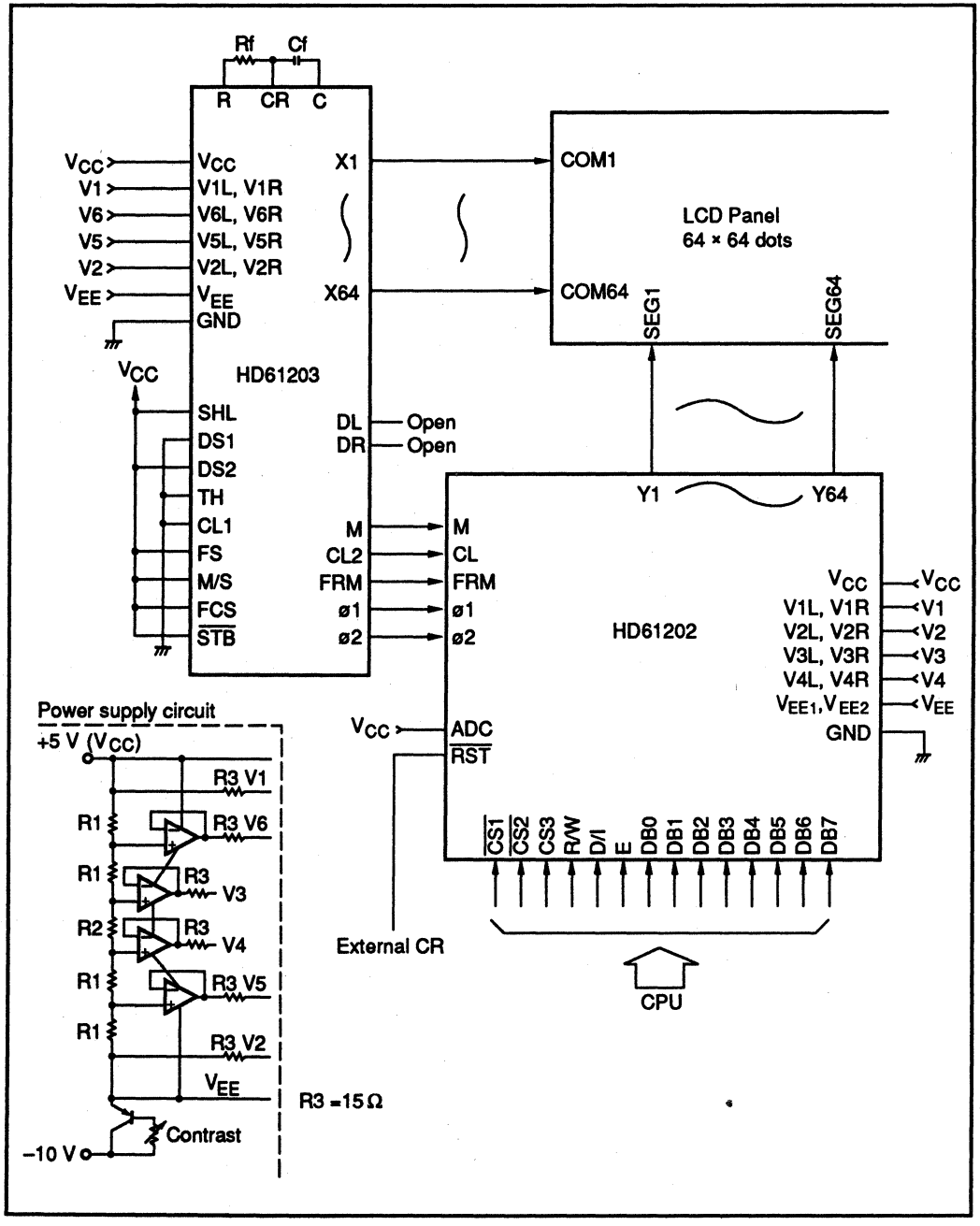
Read Display Data



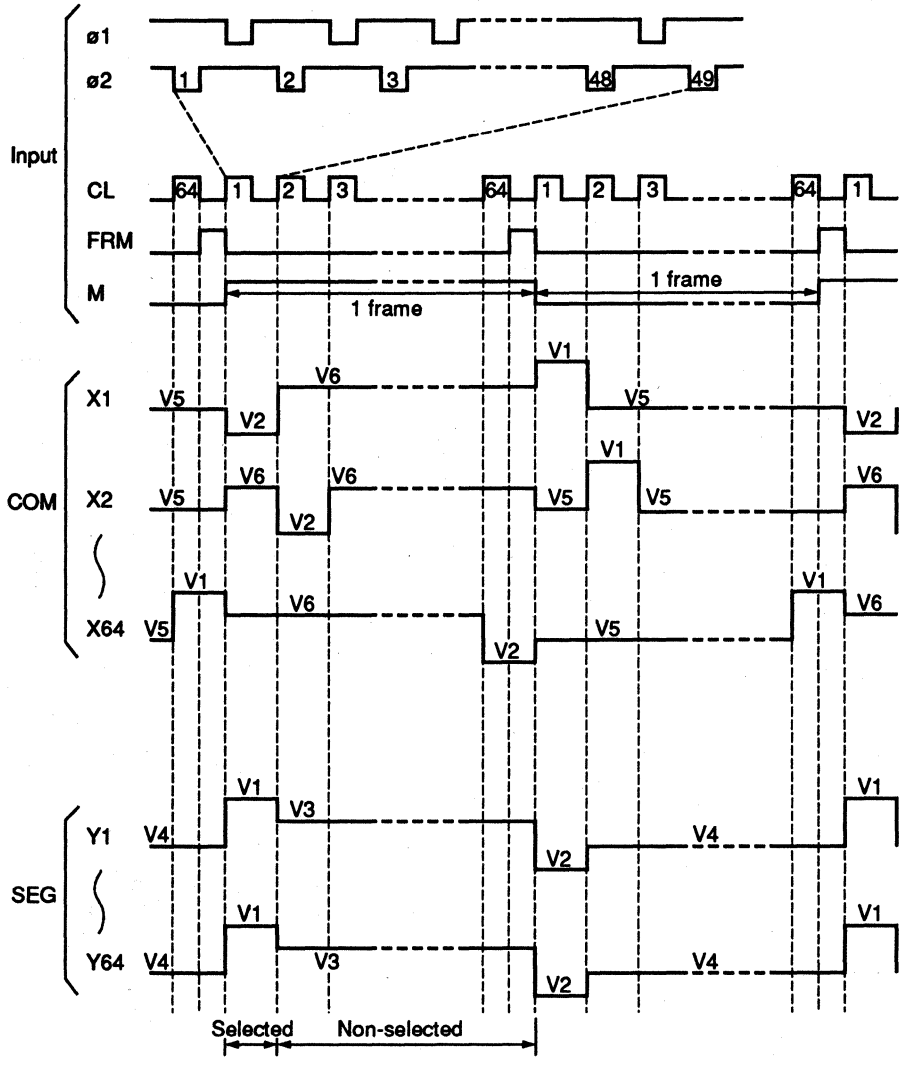
Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.
One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

Use of HD61202

Interface with HD61203 (1/64 duty cycle)



5



The waveforms of Y1 to Y64 outputs vary with the display date. In this example, the top line of the panel lights up and other dots do not.

Figure 10 LCD Driver Timing Chart (1/64 duty cycle)

Interface with CPU

1. Example of connection with HD6800

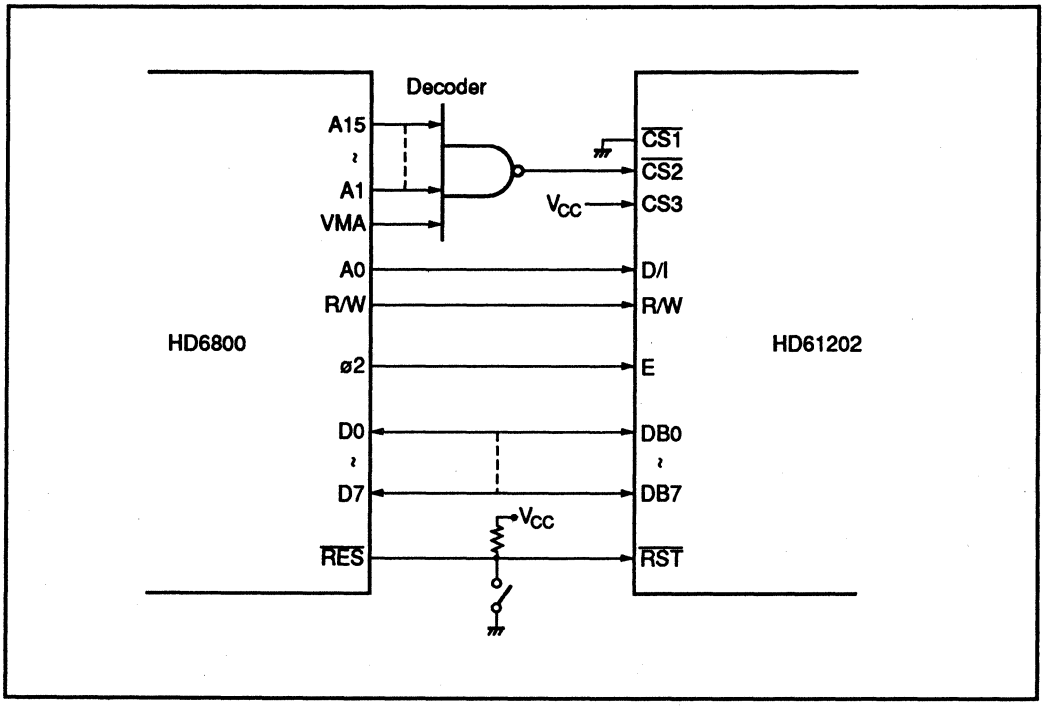


Figure 11 Example of Connection with HD6800 Series

In this decoder, addresses of HD61202 in the address area of HD6800 are:

Read/write of the display data	$FFFF
write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control HD61202 by reading/writing the data at these addresses.

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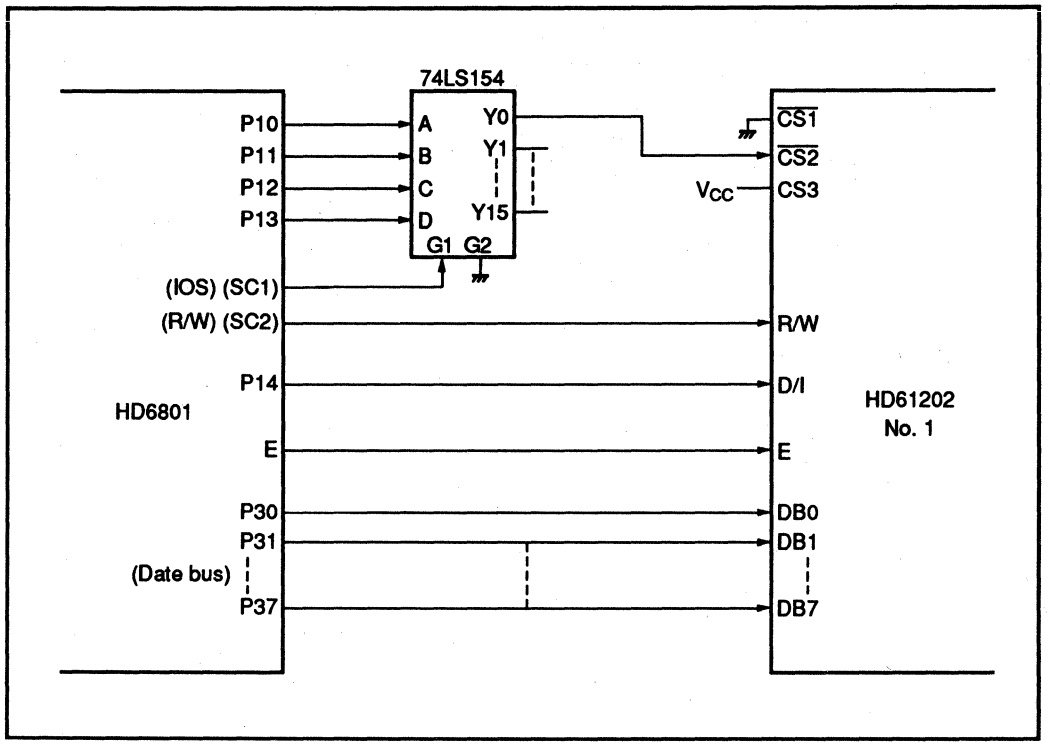
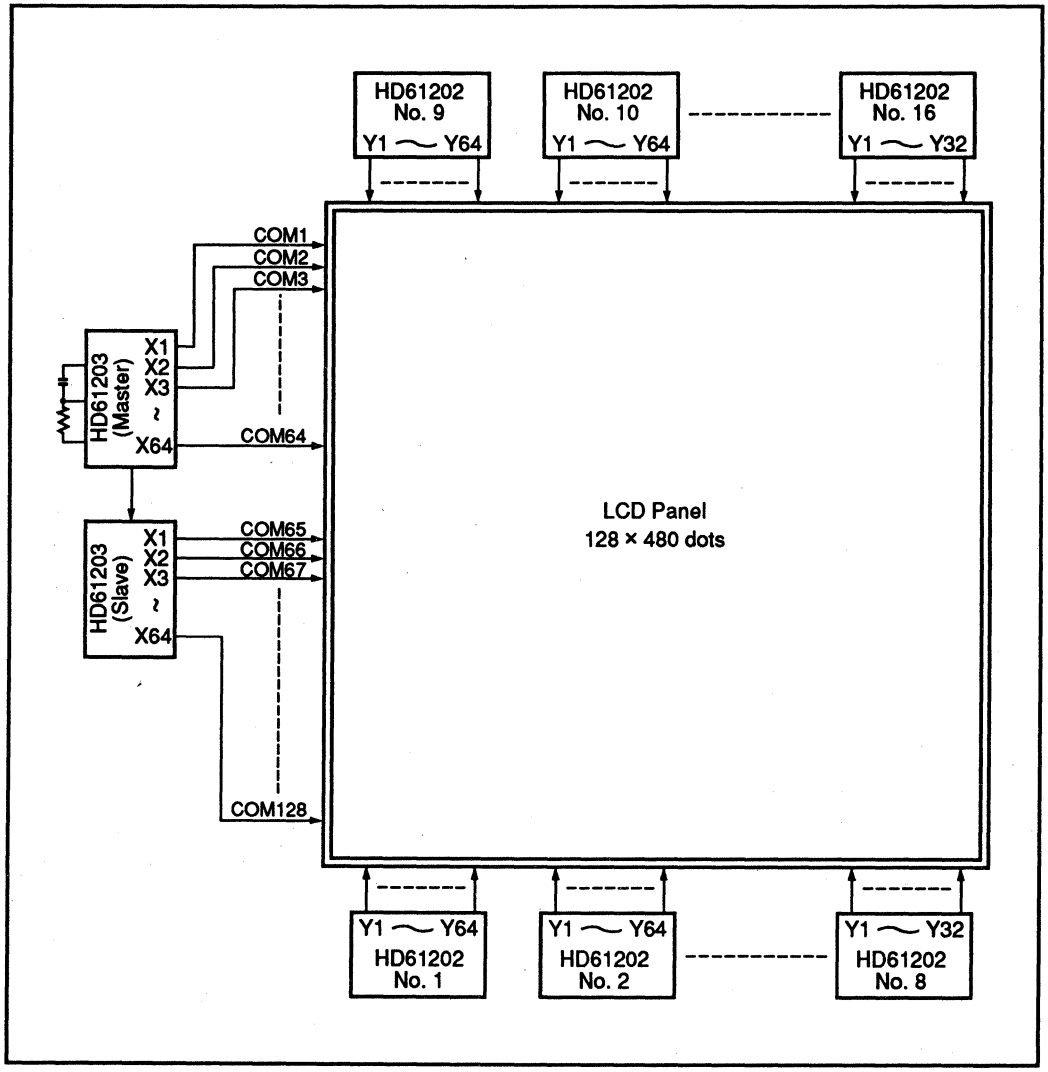
2. Example of connection with HD6801



- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 4-to-16 decoder generates chip select signal to make specified HD61202 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61202. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

Example of Application



Note: In this example, two HD61203s output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

5

HD61203

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD61203 is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61203 is produced by a CMOS process, it is fit for use in portable battery-driven equipment utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61203 and the column (segment) driver HD61202.

Features

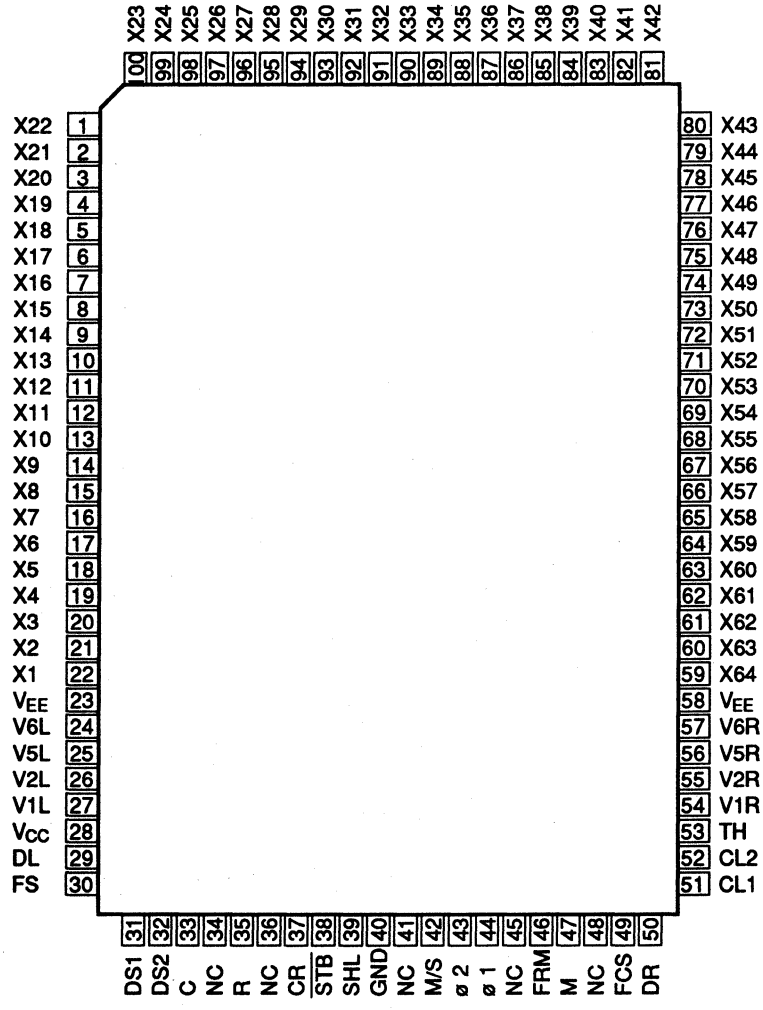
- Dot matrix liquid crystal graphic display common driver with low impedance
- Low impedance: 1.5 kΩ max
- Internal liquid crystal display driver circuit: 64 circuits
- Internal dynamic display timing generator circuit
- Display duty cycle
  When used with the column driver HD61202:
  1/48, 1/64, 1/96, 1/128
  When used with the column driver HD61200:
  Selectable out of 1/32 to 1/128
- Low power dissipation: During display: 5 mW
- Power supplies: V_{CC}: 5 V ± 10%
- Power supply voltage for liquid crystal display drive: 8 V to 17 V
- CMOS process
- 100-pin flat plastic package (FP-100)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Power supply voltage (2)	V_{EE}	V_{CC} –19.0 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	– 0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.
2. Based on GND = 0 V.
3. Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) and I/O terminals at high impedance.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
5. Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.
   Maintain $V_{CC} \geq V1L = V1R \geq V6L = V6R \geq V5L = V5R \geq V2L = V2R \geq V_{EE}$

Pin Arrangement



(Top view)

Electrical Characteristics

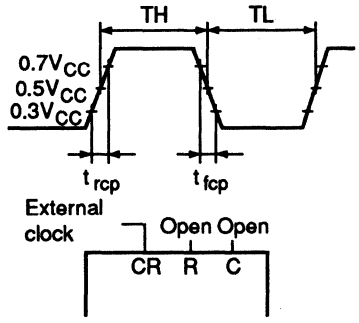
DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 8.0 to 17.0 V, Ta = –20 to +75°C)

Test Item	Symbol	Specifications Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA	2
Vi–Xj on resistance	R_{ON}	—	—	1.5	kΩ	V_{CC} – V_{EE} = 17 V Load current ±150 µA	13
Input leakage current	I_{IL1}	–1.0	—	1.0	µA	Vin = 0 to V_{CC}	3
Input leakage current	I_{IL2}	–2.0	—	2.0	µA	Vin = V_{EE} to V_{CC}	4
Operating frequency	f_{opr1}	50	—	600	kHz	In master mode external clock operation	5
Operating frequency	f_{opr2}	0.5	—	1500	kHz	In slave mode shift register	6
Oscillation frequency	fosc	315	450	585	kHz	Cf = 20 pF ± 5 % Rf = 47 kΩ ± 2%	7, 12
Dissipation current (1)	I_{GG1}	—	—	1.0	mA	In master mode 1/128 duty cycle Cf = 20 pF Rf = 47 kΩ	8, 9
Dissipation current (2)	I_{GG2}	—	—	200	µA	In slave mode 1/128 duty cycle	8, 10
Dissipation current	I_{EE}	—	—	100	µA	In master mode 1/128 duty cycle	8, 11

Notes:
1. Applies to input terminals FS, DS1, DS2, CR, SHL, M/S, and FCS and I/O terminals DL, M, DR, and CL2 in the input state.
2. Applies to output terminals, ø1, ø2, and FRM and I/O common terminals DL, M, DR, and CL2 in the output state.
3. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH, I/O terminals DL, M, DR, and CL2 in the input state and NC terminals.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R. Don't connect any lines to X1 to X64.
5. External clock is as follows.

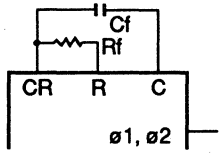
External clock waveform



$$\text{Duty Cycle} = \frac{TH}{TH + TL} \times 100\%$$

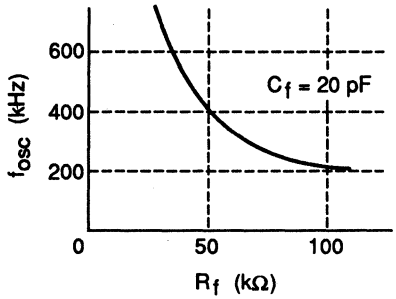
	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
t_{rcp}	–	–	50	ns
t_{fcp}	–	–	50	ns

6. Applies to the shift register in the slave mode. For details, refer to AC Characteristics.
7. Connect oscillation resister (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency (fø) at ø1 or ø2.



Cf = 20 pF
Rf = 47 kΩ $\quad f_{osc} = 2 \times f\text{ø}$

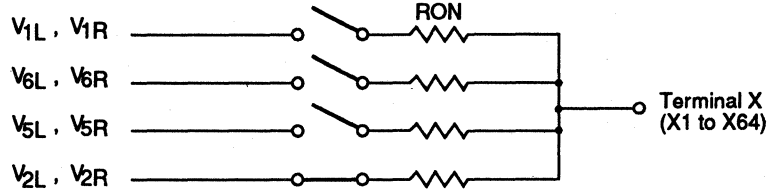
8. No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH} = V_{CC}$ and $V_{IL} = GND$.
9. This value is specified for current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$, and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in note 7.
10. This value is specified for current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS, and CR is connected to V_{CC}, CL1, TH, and M/S to GND and the terminals CL2, M, and DL are respectively connected to terminals CL2, M, and DL of the HD61203 under the condition described in note 9.
11. This value is specified for current flowing through V_{EE} under the condition described in note 9. Don't connect any lines to terminal V.
12. This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting conditions.



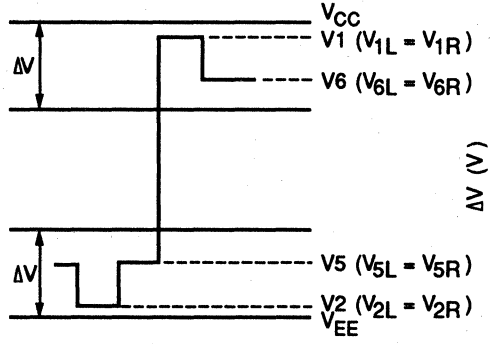
5

13. Resistance between terminal X and terminal V (one of V1L, V1R, V2L, V2P, V5L, V5R, V6L, and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:

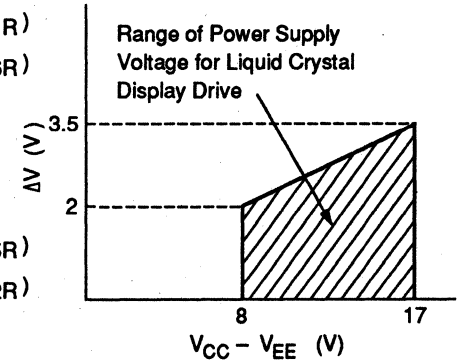
$$V_{CC} - V_{EE} = 17\ V$$
$$V_{1L} = V_{1R},\ V_{6L} = V_{6R} = V_{CC} - 1/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{5L} = V_{5R} = V_{EE} + 1/7\ (V_{CC} - V_{EE})$$



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V6L = V6R and negative voltage to V2L = V2R and V5L = V5R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



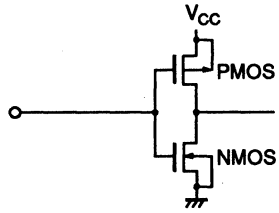
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

Terminal Configuration

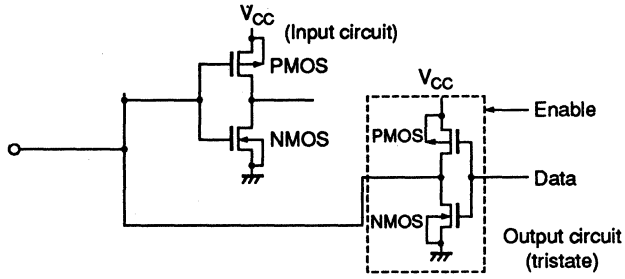
Input Terminal



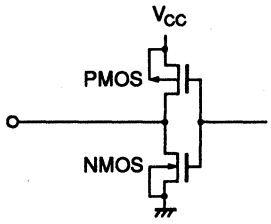
Applicable Terminals :
CR, M/S, SHL, FCS, DS1, DS2, FS

I/O Terminal

Applicable Terminals: DL, DR, CL2, M

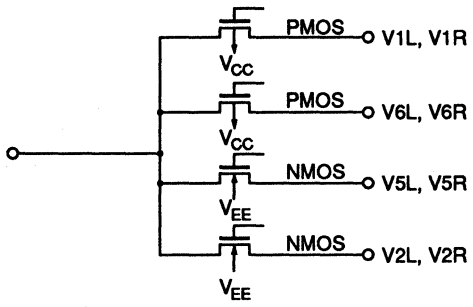


Output Terminal



Applicable Terminals: ø1, ø2, FRM

Output Terminal

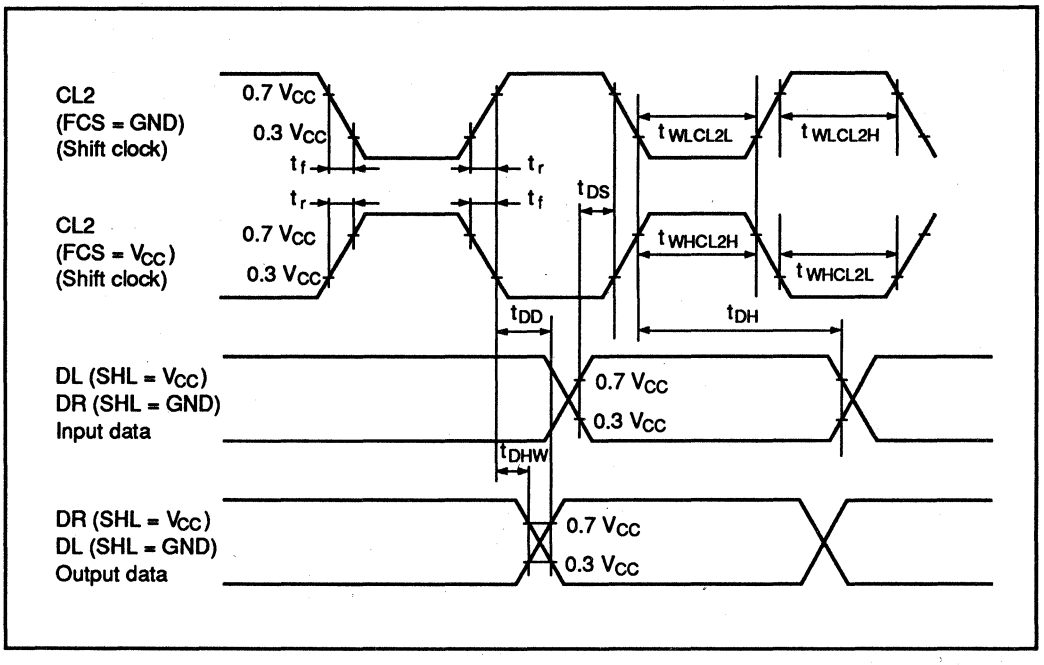


Applicable Terminals:
X1 to X64

5

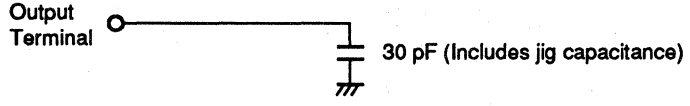
AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, Ta = –20 to +75°C)

In the slave mode (M/S = GND)

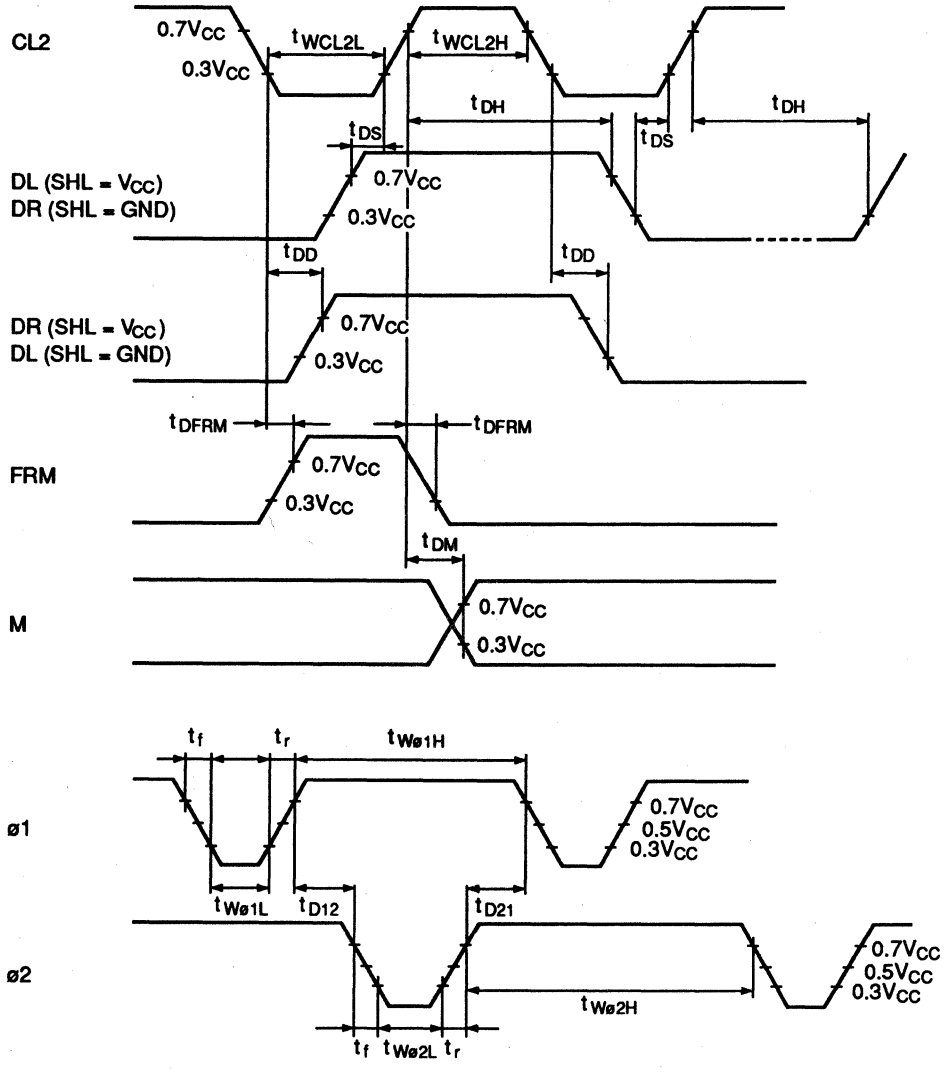


Item	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width (FCS=GND)	t_{WLCL2L}	450	-	-	ns	
CL2 high level width (FCS=GND)	t_{WLCL2H}	150	-	-	ns	
CL2 low level width (FCS=V_{CC})	t_{WHCL2L}	150	-	-	ns	
CL2 high level width (FCS=V_{CC})	t_{WHCL2H}	450	-	-	ns	
Data setup time	t_{DS}	100	-	-	ns	
Data hold time	t_{DH}	100	-	-	ns	
Data delay time	t_{DD}	-	-	200	ns	1
Output data hold time	t_{DHW}	10	-	-	ns	
CL2 rise time	t_r	-	-	30	ns	
CL2 fall time	t_f	-	-	30	ns	

Notes: 1. The following load circuit is connected for specification:



2. In the master mode (M/S = V_{CC}, FCS = V_{CC}, Cf = 20 pF, Rf = 47 kΩ)



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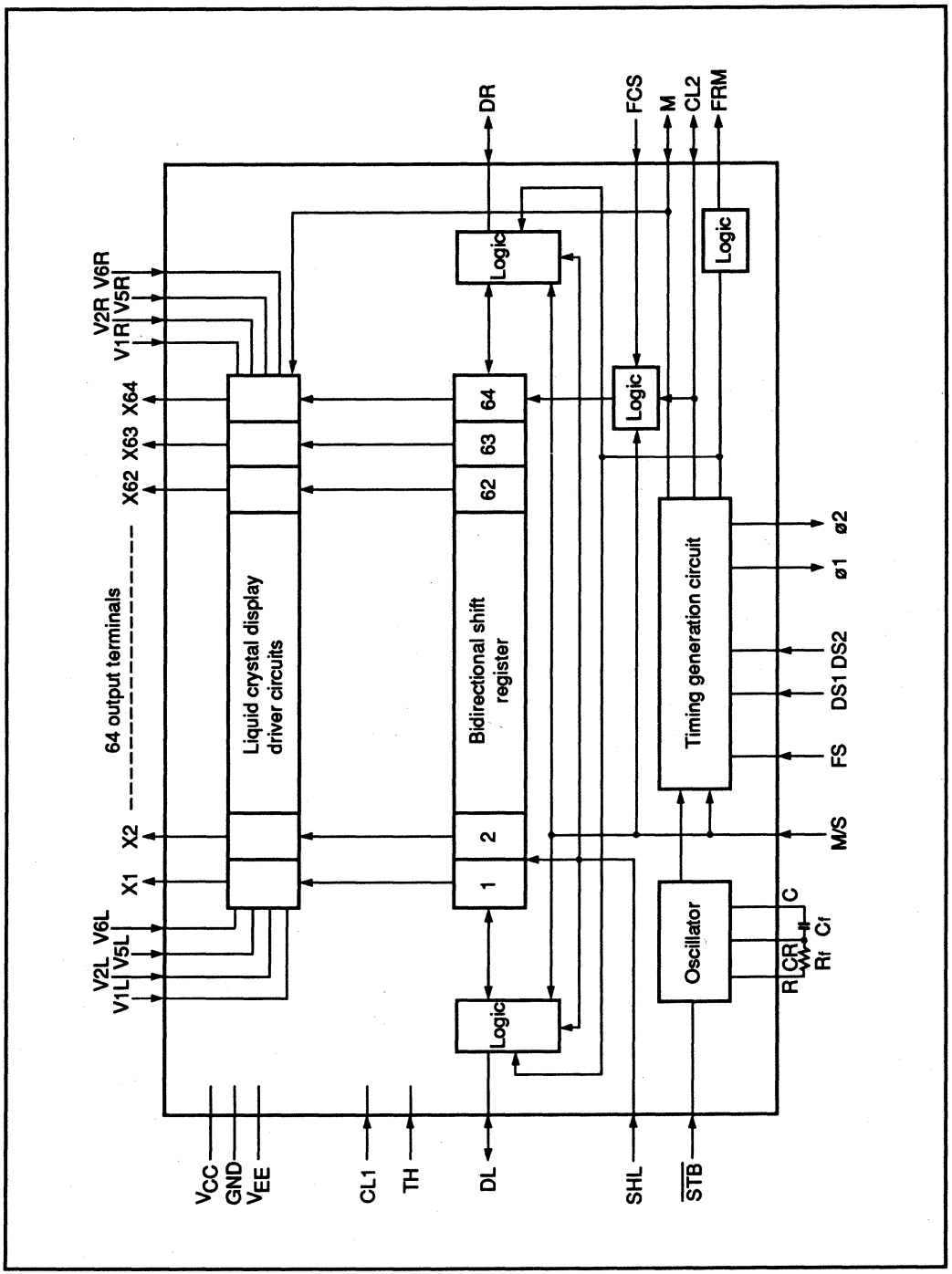
Item	Symbol	Min	Typ	Max	Unit
Data setup time	t_{DS}	20	—	—	µs
Data hold time	t_{DH}	40	—	—	µs
Data delay time	t_{DD}	5	—	—	µs
FRM delay time	t_{DFRM}	–2	—	2	µs
M delay time	t_{DM}	–2	—	2	µs
C_{L2} low level width	t_{WCL2L}	35	—	—	µs
C_{L2} high level width	t_{WCL2H}	35	—	—	µs
ø1 low level width	$t_{Wø1L}$	700	—	—	ns
ø2 low level width	$t_{Wø2L}$	700	—	—	ns
ø1 high level width	$t_{Wø1H}$	2100	—	—	ns
ø2 high level width	$t_{Wø2H}$	2100	—	—	ns
ø1–ø2 phase difference	t_{D12}	700	—	—	ns
ø2–ø1 phase difference	t_{D21}	700	—	—	ns
ø1, ø2 rise time	t_r	—	—	150	ns
ø1, ø2 fall time	t_f	—	—	150	ns

Block Diagram



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Block Functions

Oscillator

The CR oscillator generates display timing signals and operating clocks for the HD61202. It is required when the HD61203 is used with the HD61202. An oscillation resister Rf and an oscillation capacitor Cf are attached as shown in figure 1 and terminal $\overline{STB}$ is connected to the high level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminals R and C.

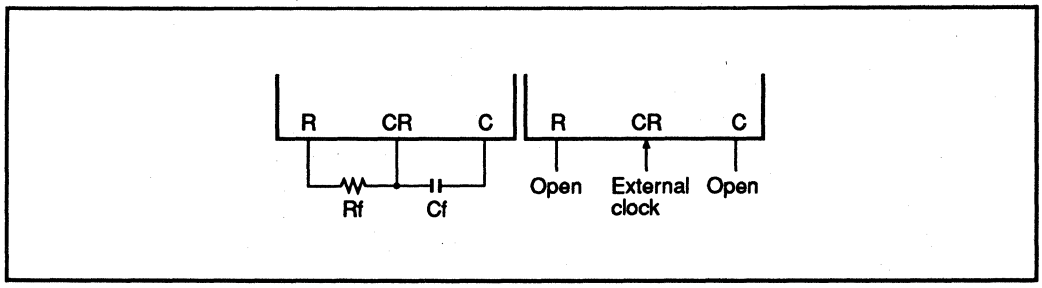


Figure 1 Oscillator Connection with HD61202

The oscillator is not required when the HD61203 is used with the HD61830. Then, connect terminal CR to the high level and don't connect any lines to terminals R and C (figure 2).

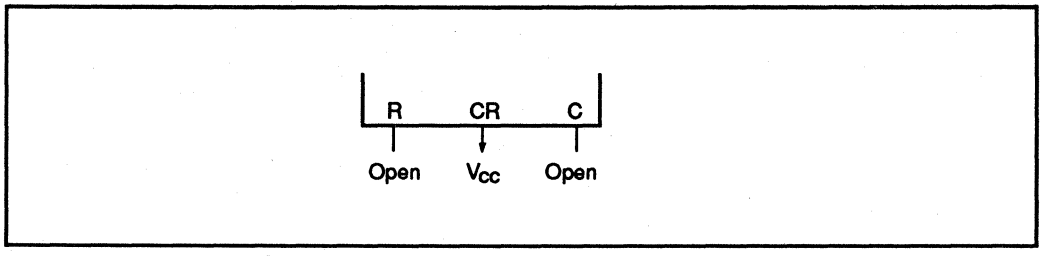


Figure 2 Oscillator Connection with HD61830

Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61202. This circuit is required when the HD61203 is used with the HD61202. Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals Fs, DS1, and DS2 to high level and M/S to low level (slave mode).

Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the DL side, corresponds to X1 and the highest order bit on the DR side corresponds to X64.

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals (table 1).

Table 1 Output Levels

Data from the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

HD61203 Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Function
V_{CC} GND V_{EE}	1 1 2		Power supply	V_{CC}–GND: Power supply for internal logic. V_{CC}–V_{EE}: Power supply for driver circuit logic.
V1L, V2L V5L, V6L V1R, V2R V5R, V6R	8		Power supply	Liquid crystal display driver level power supply. V1L (V1R), V2L (V2R): Selected level V5L (V5R), V6L (V6R): Non-selected level Voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects master/slave. M/S = V_{CC}: Master mode When the HD61203 is used with the HD61202, timing generation circuit operates to supply display timing signals and operation clock to the HD61202. Each of I/O common terminals DL, DR, CL2, and M is in the output state. M/S = GND: Slave mode The timing operation circuit stops operating. The HD61203 is used in this mode when combined with the HD61830. Even if combined with the HD61202, this mode is used when display timing signals (M, data, CL2, etc.) are supplied by another HD61203 in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC}: Shift register operates at the rising edge of CL2. Select this condition when HD61203 is used with HD61202 or when MA of the HD61830 connects to CL2 in combination with the HD61830. FCS = GND: Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in combination with the HD61830.
FS	1	I	V_{CC} or GND	Selects frequency. When the frame frequency is 70 Hz, the oscillation frequency should be: f_{osc} = 430 kHz at FCS = V_{CC} f_{osc} = 215 kHz at FCS = GND This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.

HD61203 Terminal Functions (cont)

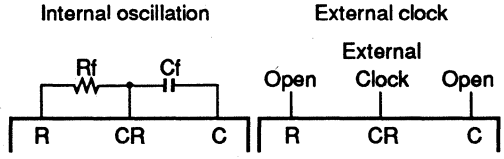
Terminal Name	Number of Terminals	I/O	Connected to	Function
DS1, DS2	2	I	V_{CC} or GND	Selects display duty factor

Display Duty Factor	1/48	1/64	1/96	1/128
DS1	GND	GND	V_{CC}	V_{CC}
DS2	GND	V_{CC}	GND	V_{CC}

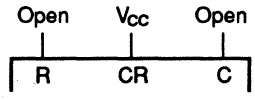
These terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.

$\overline{STB}$	1	I	V_{CC} or GND	Input terminal for testing.
TH	1			Connect to $\overline{STB}$ V_{CC}.
CL1	1			Connect TH and CL1 to GND.
CR, R, C	3			Oscillator.

In the master mode, use these terminals as shown below:



In the slave mode, stop the oscillator as shown below:



ø1, ø2	2	O	HD61202	Operating clock output terminals for the HD61202. Master mode: Connect these terminals to terminals ø1 and ø2 of the HD61202 respectively. Slave mode: Don't connect any lines to these terminals.
FRM	1	O	HD61202	Frame signal. Master mode: Connect this terminal to terminal FRM of the HD61202. Slave mode: Don't connect any lines to this terminal.
M	1	I/O	MB of HD61830 or M of HD61202	Signal to convert LCD driver signal into AC. Master mode: Output terminal. Connect this terminal to terminal M of the HD61202. Slave mode: Input terminal. Connect this terminal to terminal MB of the HD61830.

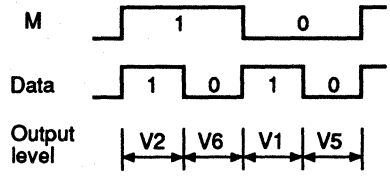
5

HD61203 Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Function
CL2	1	I/O	CL1 or MA of HD61830 or CL of HD61202	Shift clock Master mode: Output terminal Connect this terminal to terminal CL of the HD61202. Slave mode: Input terminal Connect this terminal to terminal CL1 or MA of the HD61830.
DL, DR	2	I/O	Open or FLM of HD61830	Data I/O terminals of bidirectional shift register. DL corresponds to X1's side and DR to X64's side. Master mode: Output common scanning signal. Don't connect any lines to these terminals normally. Slave mode: Connect terminal FLM of the HD61830 to DL (when SHL = V_{CC}) or DR (when SHL = GND)
NC	5		Open	Not used. Don't connect any lines to this terminal.
SHL	1	I	V_{CC} or GND	Selects shift direction of bidirectional shift register.
X1–X64	64	O	Liquid crystal display	Liquid crystal display driver output. Output one of the four liquid crystal display driver levels V1, V2, V5, and V6 with the combination of the data from the shift register and M signal. When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

M/S	V_{CC}		GND	
SHL	V_{CC}	GND	V_{CC}	GND
DL	Output	Output	Input	Output
DR	Output	Output	Output	Input

SHL	Shift Direction	Common Scanning Direction
V_{CC}	DL → DR	X1 → X64
GND	DL ← DR	X1 ← X64



Example of Application

HD61203 Connection List

H: V_{CC} } Fixed
L: GND }

"-" means "open". Rf: Oscillation resister

Cf: Oscillation capacitor

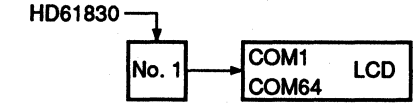
	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	φ1	φ2	FRM	M	CL2	SHL	DL	DR	X1–X64
A	L	L	L	L	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	—	COM1–COM64
																	L	—	from FLM of HD61830	COM64–COM1
B	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61203 No. 2	COM1–COM64
																	L	to DL/DR of HD61203 No. 2	from FLM of HD61830	COM64–COM1
C	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61203 No. 1	—	COM65–COM128
																	L	—	from DL/DR of HD61203 No. 1	COM128–COM65
D	H	L	L	H	H	L or L	L or H	H	Rf Cf	Rf	Cf	to φ1 of HD61202	to φ2 of HD61202	to FRM of HD61202	to M of HD61202	to CL of HD61202	H	—	—	COM1–COM64
																	L	—	—	COM64–COM1
E	H	L	L	H	H	L or L	L or H	H	Rf Cf	Rf	Cf	to φ1 of HD61202	to φ2 of HD61202	to FRM of HD61202	toM of HD61202 HD61203	to CL of HD61202 to CL2 of HD61203	H	—	to DL/DR of HD61203 No. 2	COM1–COM64
																	L	to DL/DR of HD61203 No. 2	—	COM64–COM1
F	L	L	L	H	H	H	H	H	H	—	—	—	—	—	from M of HD61203 No. 1	from CL2 of HD61203 No. 1	H	from DL/DR of HD61203 No. 1	—	COM1–COM64
																	L	—	from DL/DR of HD61203 No. 1	COM64–COM1

5

Outline of HD61203 System Configuration

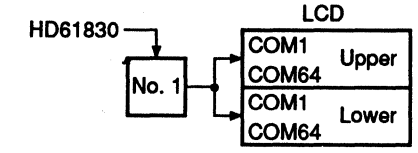
1. Use with HD61830

a. When display duty ratio of LCD is 1/64



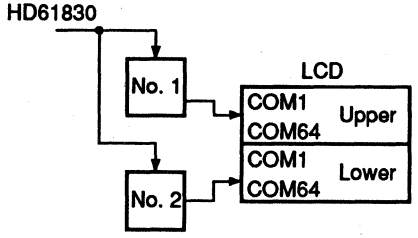
One HD61203 drives common signals.

Refer to Connection list A.



One HD61203 drives common signals for upper and lower panels.

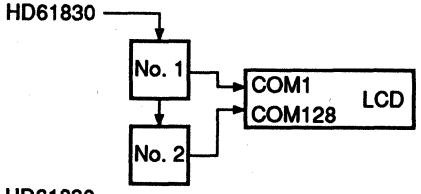
Refer to Connection list A.



Two HD61203s drive upper and lower panels separately to ensure the quality of display. No. 1 and No. 2 operate in parallel.

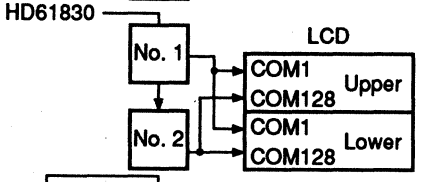
For both of No. 1 and No. 2, refer to Connection list A.

b. When display duty ratio of LCD is from 1/65 to 1/128



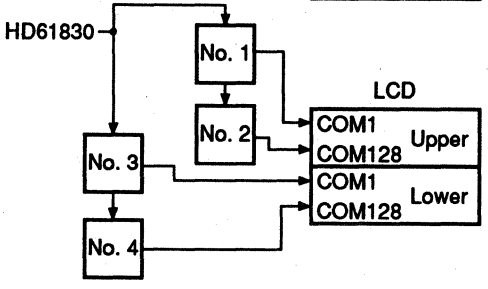
Two HD61203s connected serially drive common signals.

Refer to Connection list B for No. 1. Refer to Connection list C for No. 2.



Two HD61203s connected serially drive upper and lower panels in parallel.

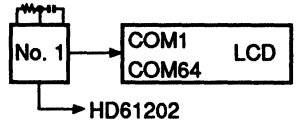
Refer to Connection list B for No. 1. Refer to Connection list C for No. 2.



Two sets of HD61203s connected serially drive upper and lower panels in parallel to ensure the quality of display.

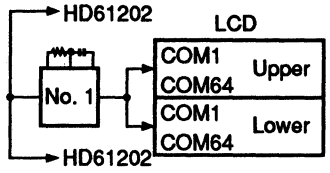
Refer to Connection list B for No. 1 and 3. Refer to Connection list C for No. 2 and 4.

2. Use with HD61202 (1/64 duty ratio)



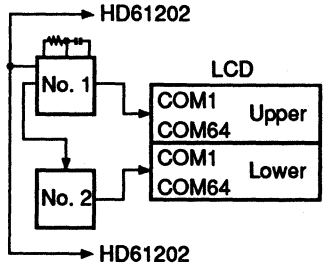
One HD61203 drives common signals and supplies timing signals to the HD61202s.

Refer to Connection list D.



One HD61203 drives upper and lower panels and supplies timing signals to the HD61202s.

Refer to Connection list D.



Two HD61203s drive upper and lower panels in parallel to ensure the quality of display. No. 1 supplies timing signals to No. 2 and the HD61202s.

Refer to Connection list E for No. 1.

Refer to Connection list F for No. 2.

5

Connection Example 1

Use with HD61202 (RAM type segment driver)
a. 1/64 duty ratio (See Connection List D)

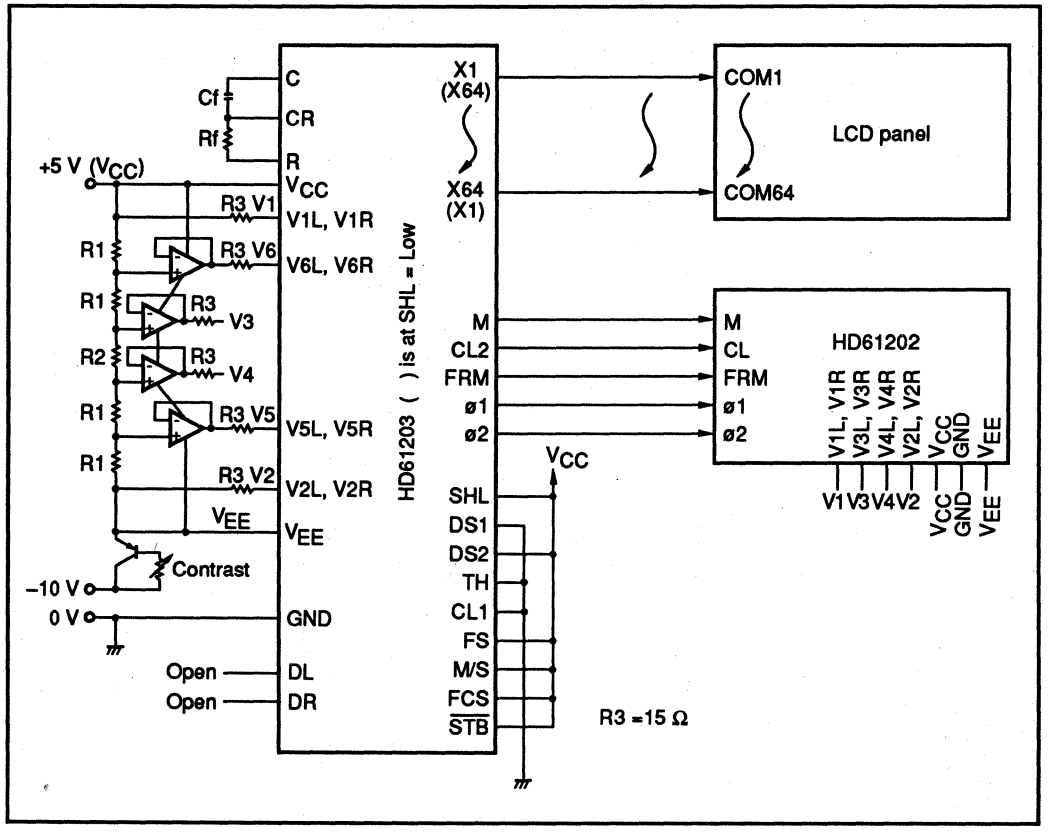


Figure 1 Example 1

Note: The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,
R1 = 3 kΩ, R2 = 15 kΩ

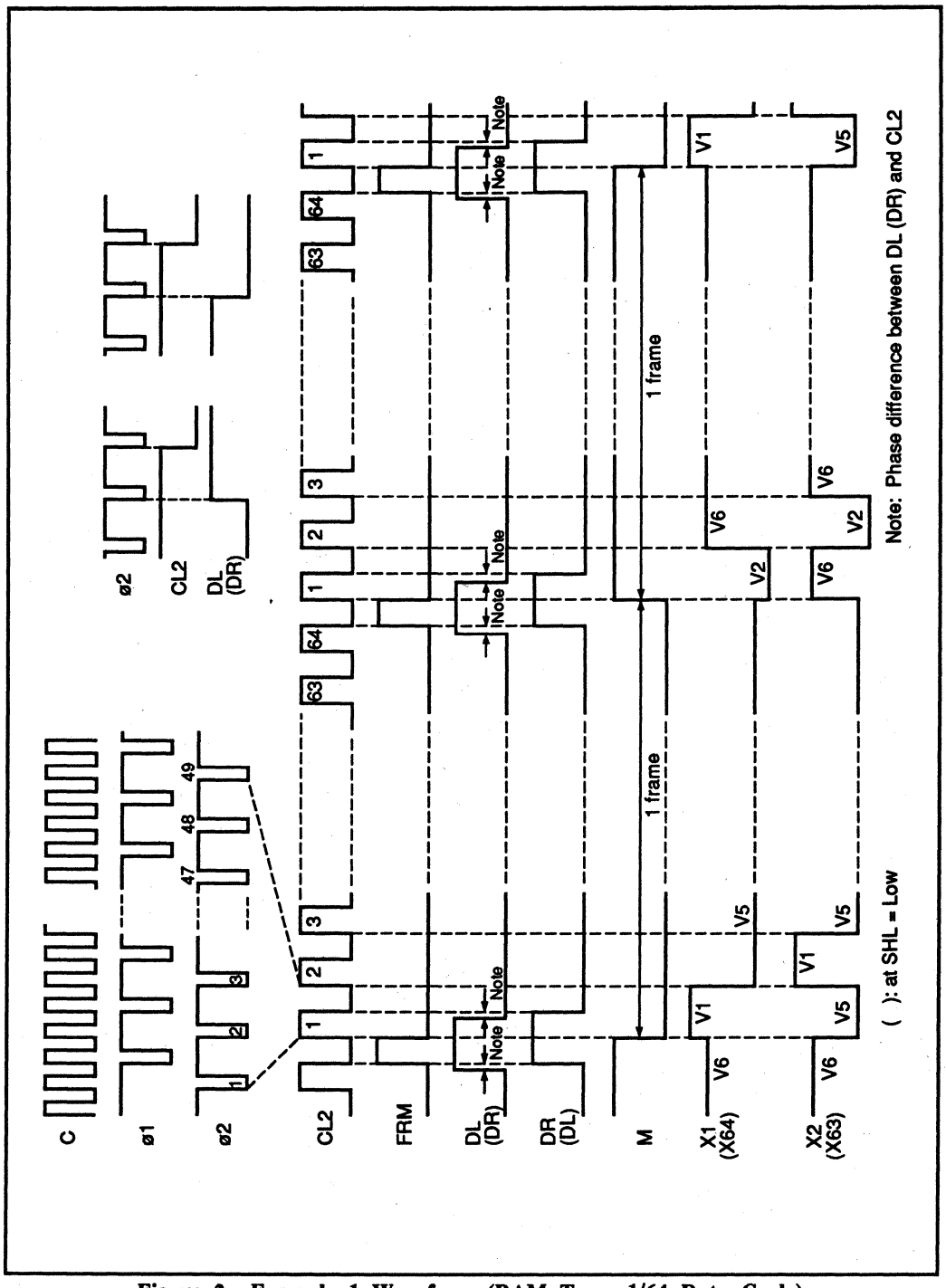


Figure 2 Example 1 Waveform (RAM Type, 1/64 Duty Cycle)

5

Connection Example 2

Use with HD61830 (Dispiay controiler)
a. 1/64 duty ratio (See Connection List A)

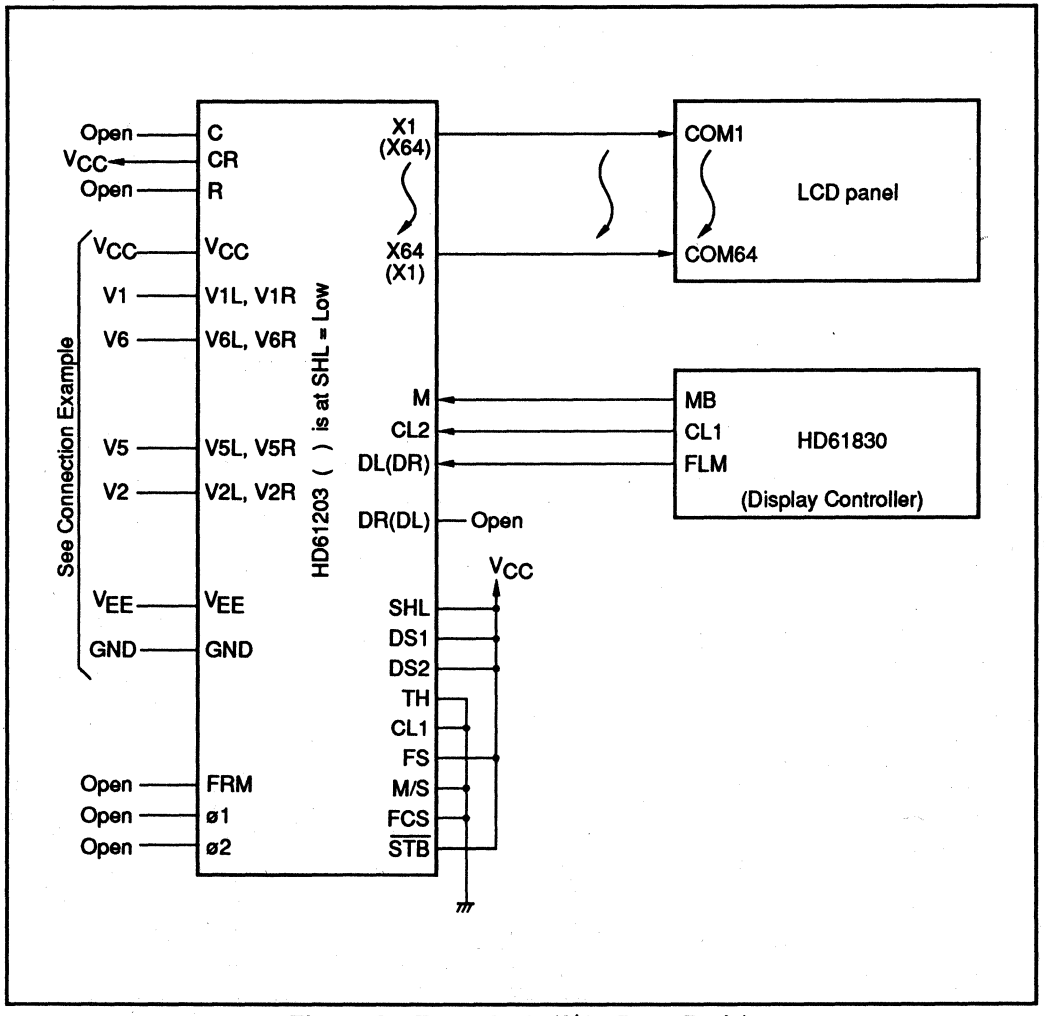


Figure 3 Example 2 (1/64 Duty Ratio)

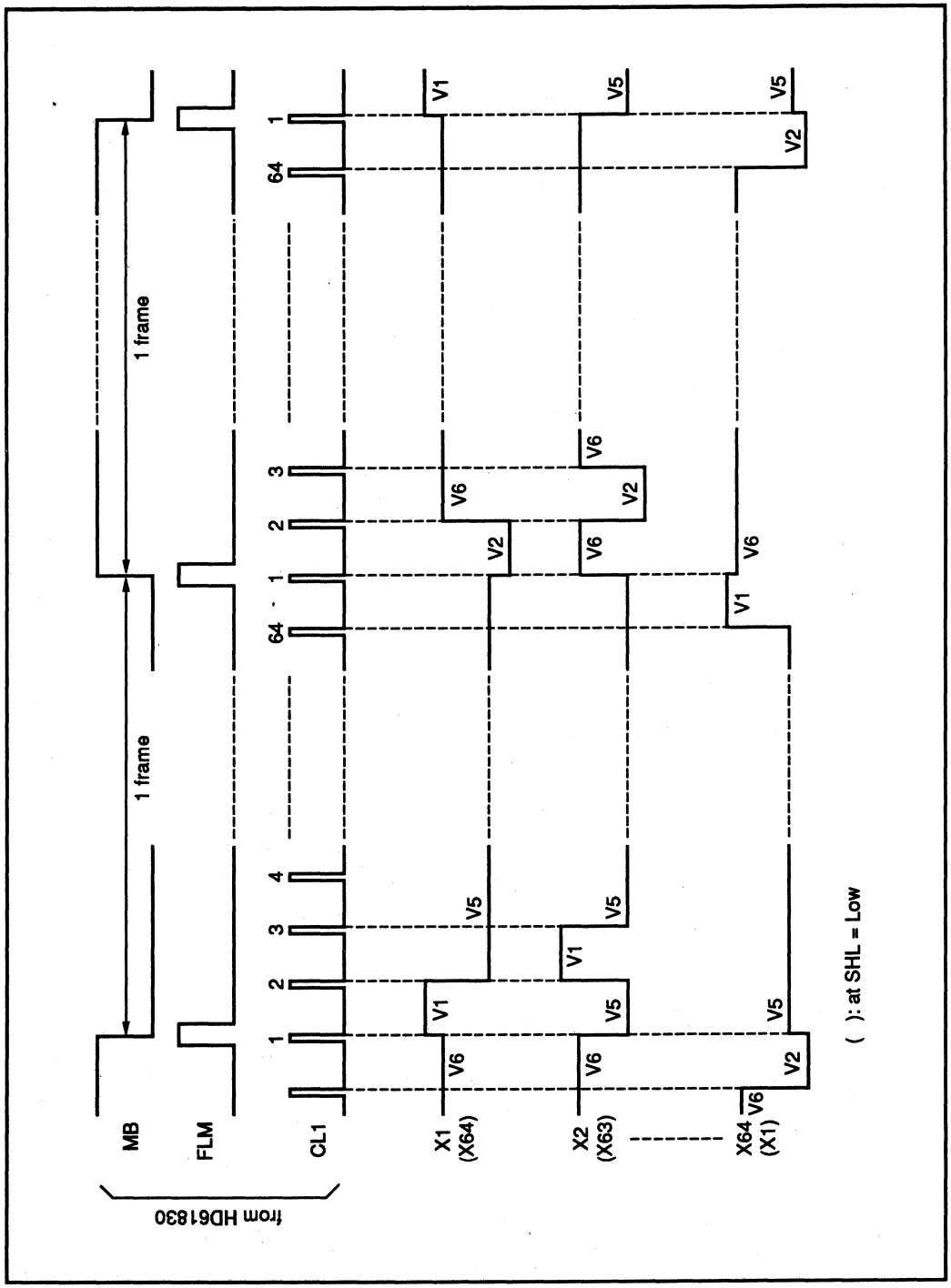


Figure 4 Example 2 Waveform (1/64 Duty Ratio)

b. 1/100 duty ratio (See Connection List B, C)

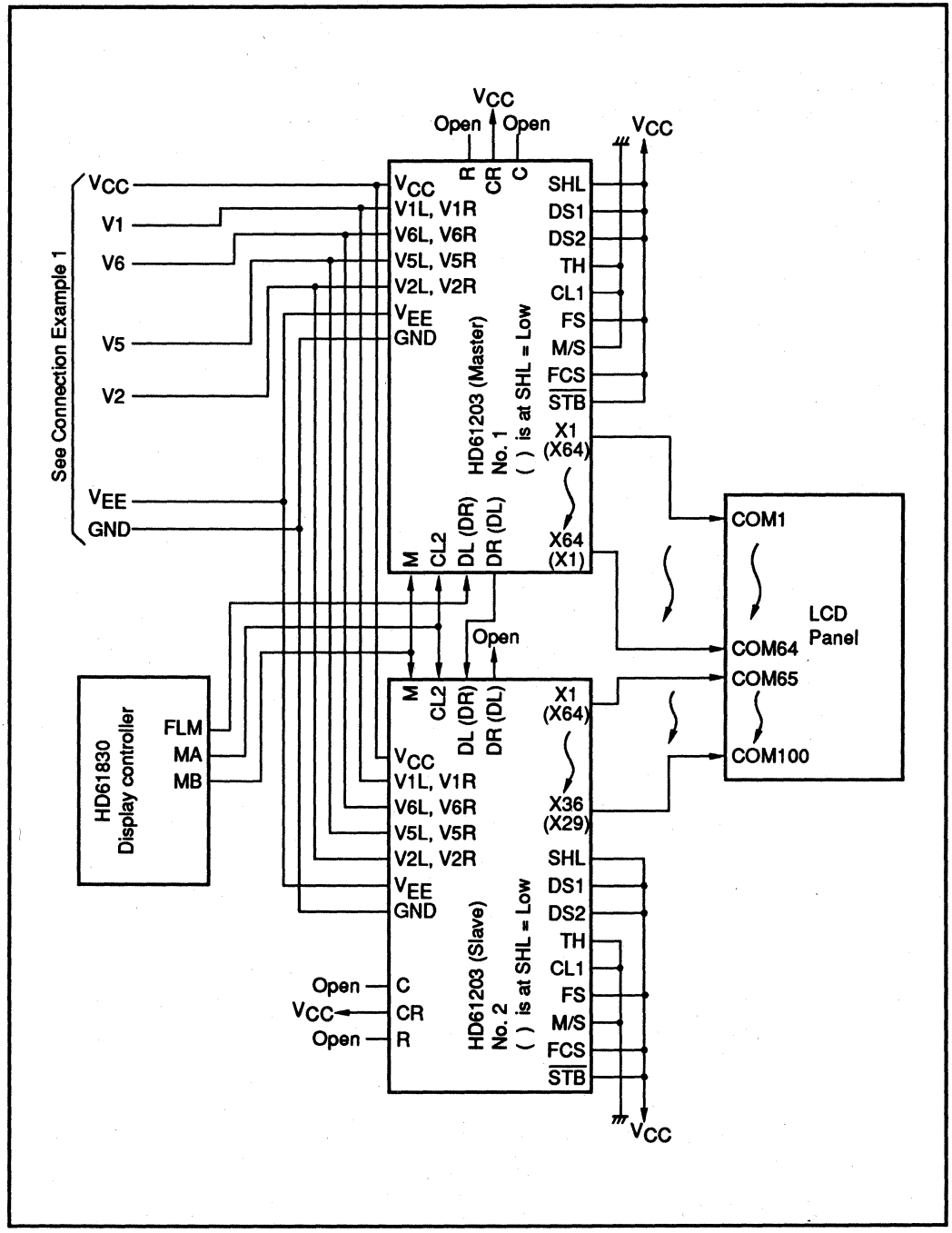


Figure 5 Example 2 (1/100 Duty Ratio)

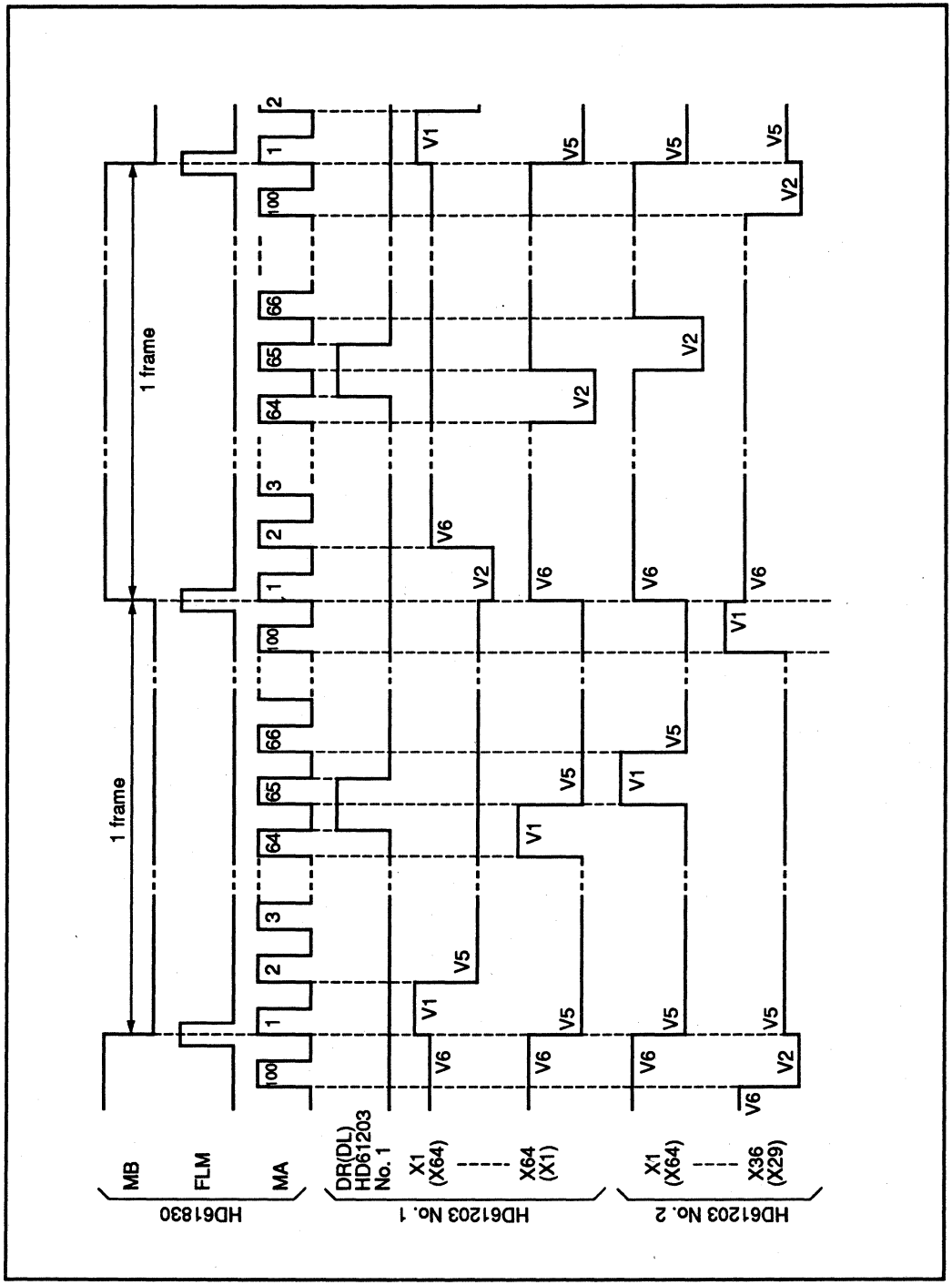


Figure 6 Example 2 Waveform (1/100 Duty Ratio)

HD61830
LCTC (LCD Timing Controller)

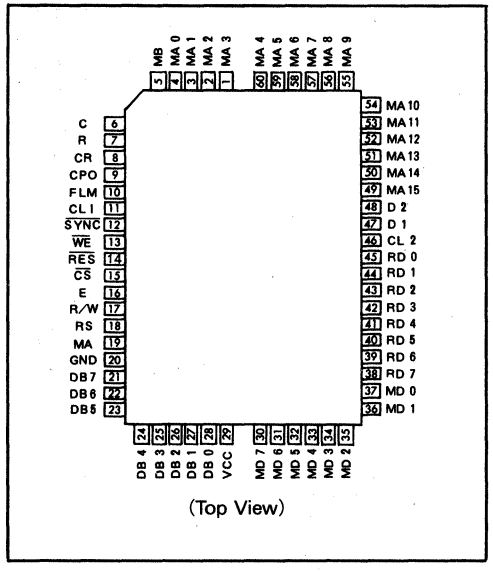
Description

The HD61830 is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcontroller in the external RAM to generate dot matrix liquid crystal driving signals. It has a graphic mode in which 1-bit data in the external RAM corresponds to the on/off state of 1 dot on liquid crystal display and a character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications. The HD61830 is produced by the CMOS process. Thus, combined with a CMOS microcontroller it can complete a liquid crystal display device with low power dissipation.

Features

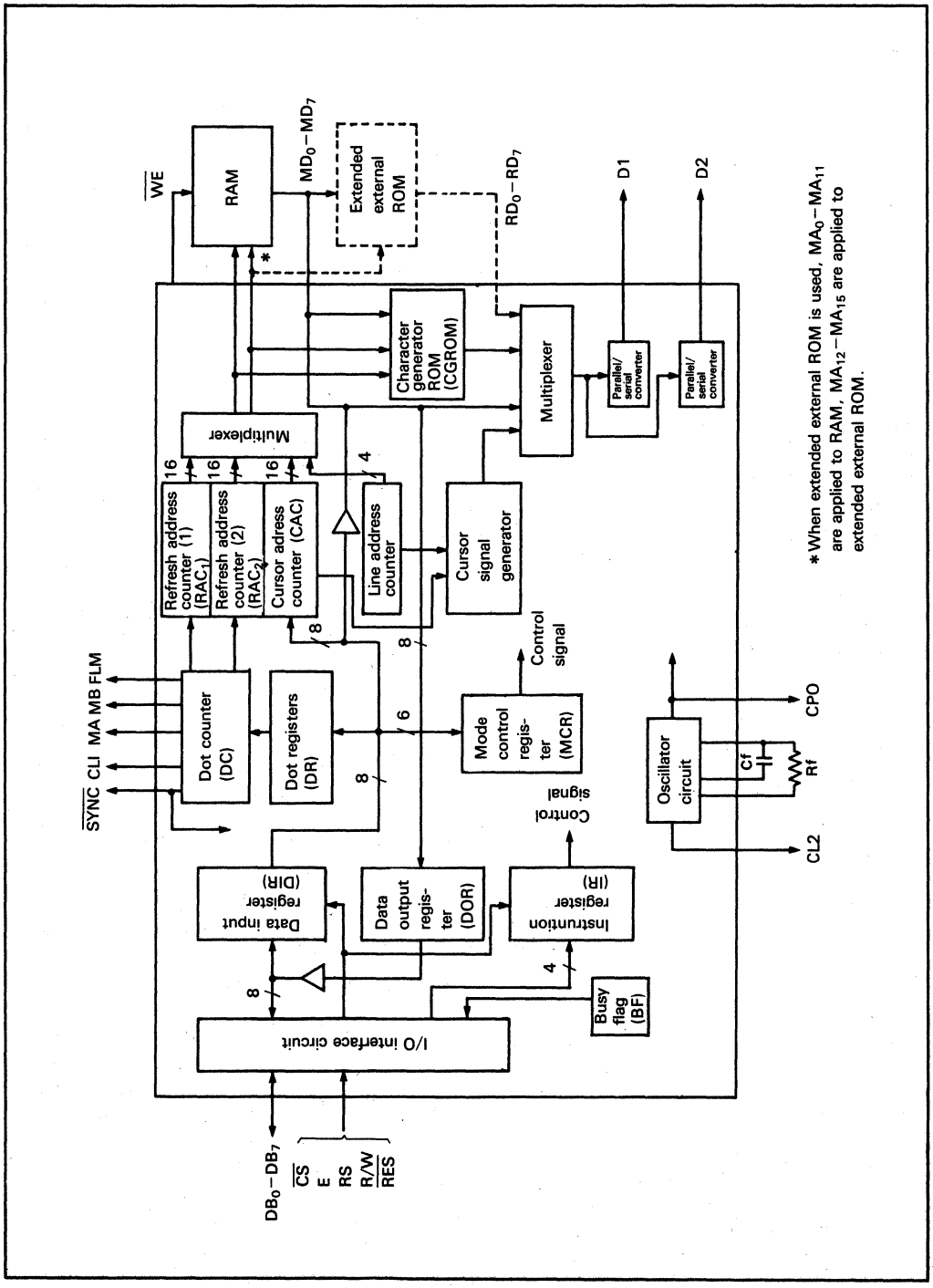
- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - −Graphic mode: 512k dots (2^{16} bytes)
  - −Character mode: 4096 characters (2^{12} characters)
- Internal character generator ROM: 7360 bits
  - −160 types of 5 × 7 dot characters
  - −32 types of 5 × 11 dot characters
    Total 192 characters
  - −Can be extended to 256 characters (4k bytes max.) by external ROM
- Interfaces to 8-bit MPU
- Display duty cycle (Can be selected by a program)
  - −Static to 1/128 duty cycle
- Various instruction functions
  - −Scroll, Cursor on/off/blink, Character blink, Bit manipulation
- Display method: Selectable A or B types
- Internal oscillator (with external resistor and capacitor)
- Operating frequency: 1.1 MHz
- Low power dissipation
- Power supply: Single + 5 V ± 10%
- CMOS process
- Package: 60-pin plastic QFP (FP-60)

Pin Arrangement



(Top View)

Block Diagram



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Block Functions

Registers

The HD61830 has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR), and mode control register (MCR).

The IR is a 4-bit register that stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register, and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR, and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at the high level).

The DR are registers used to store dot information such as character pitches and the number of vertical dots, and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display on/off and cursor on/off/blink. The information sent from the MPU is written in it via the DIR.

Busy flag (BF)

The busy flag = 1 indicates the HD61830 is performing an internal operation. Instructions cannot be accepted. As shown in Control Instruction, read busy flag, the busy flag is output on DB7 under the conditions of RS = 1, R/W = 1, and E = 1. Make sure the busy flag is 0 before writing the next instruction.

Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

Refresh Address Counters (RAC1/RAC2)

The refresh address counters, RAC1 and RAC2, control the addresses of external RAM, character generator ROM (CGROM), and extended external ROM. The RAC1 is used for the upper half of the screen and the RAC2 for the lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12–MA15) are ignored. The 4 bits of line address counter are output instead and used as the address of extended ROM.

Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5 × 7 (160 characters) or 5× 11 (32 characters). The use of extended ROM allows 8 × 16 (256 characters max.) to be used.

Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by instruction. It holds an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of the cursor address counter is automatically increased by 1 after the display data is read or written and after the set/clear bit instruction is executed.

Cursor Signal Generator

The cursor can be displayed by instruction in character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM, or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

Terminal Functions

Name	Function
DB0–DB7	Data bus: Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7
$\overline{CS}$	Chip select: Selected state with $\overline{CS}$ = 0
R/W	Read/Write: R/W = 1: MPU ← HD61830 R/W = 0: MPU → HD61830
RS	Register select: RS = 1: Instruction register RS = 0: Data register
E	Enable: Data is written at the fall of E Data can be read while E is 1
CR, R, C	CR oscillator
$\overline{RES}$	Reset: Reset = 0 results in display off, slave mode and Hp = 6
MA0–MA15	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 (0: Character 1st line, F: Character 16th line)
MD0–MD7	Display data bus: Three-state I/O common terminal
RD0–RD7	ROM data input: Dot data from external character generator is input
$\overline{WE}$	Write enable: Write signal for external RAM
CL2	Display data shift clock for LCD drivers
CL1	Display data latch signal for LCD drivers
FLM	Frame signal for display synchronization
MA	Signal for converting liquid crystal driving signal into AC, A type
MB	Signal for converting liquid crystal driving signal into AC, B type
D1, D2	Display data serial output D1: For upper half of screen D2: For lower half of screen
CPO	Clock signal for HD61830 in slave mode
$\overline{SYNC}$	Synchronous signal for parallel operation Three-state I/O common terminal (with pull-up MOS) Master: Synchronous signal is output Slave: Synchronous signal is input

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	− 0.3 to + 0.7	V	1, 2
Terminal voltage	V_T	− 0.3 to V_{CC} + 0.3	V	1, 2
Operating temperature	T_{opr}	− 20 to + 75	°C	
Storage temperature	T_{stg}	− 55 to + 125	°C	

Notes: 1. All voltages are referenced to GND = 0 V.
2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

Electrical Characteristics

(V_{CC} = 5 V ± 5 %, GND = 0 V, T_a = − 20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage (TTL)	V_{IH}	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	V_{IL}	0	—	0.8	V		2
Input high voltage	V_{IHR}	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	V_{IHC}	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	V_{ILC}	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	V_{OH}	2.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	5
Output low voltage (TTL)	V_{OL}	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	V_{OHC}	V_{CC} − 0.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	6
Output low voltage (CMOS)	V_{OLC}	0	—	0.4	V	I_{OL} = 0.6 mA	6
Input leakage current	I_{IN}	− 5	—	5	μA	V_{IN} = 0−V_{CC}	7
Three-state leakage current	I_{TSL}	− 10	—	10	μA	V_{OUT} = 0−V_{CC}	8
Power dissipation (1)	P_w1	—	10	15	mW	CR oscillation fosc = 500 kHz	9
Power dissipation (2)	P_w2	—	20	30	mW	External clock fcp = 1 MHz	9
Internal clock operation							
Clock oscillation frequency	f_{osc}	400	500	600	kHz	Cf = 15 pF ± 5% Rf = 39 kΩ ± 2%	10
External clock operation							
External clock operating frequency	f_{cp}	100	500	1100	kHz		11
External clock duty	Duty	47.5	50	52.5	%		11
External clock rise time	t_{rcp}	—	—	0.05	μs		11
External clock fall time	t_{fcp}	—	—	0.05	μs		11
Pull-up current	I_{PL}	2	10	20	μA	V_{IN} = GND	12

Note: The I/O terminals have the following configuration:

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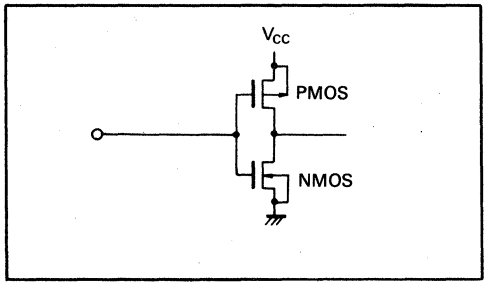
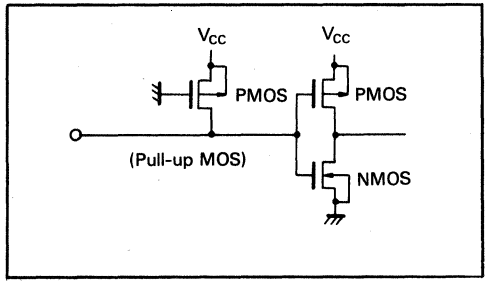
Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/$\overline{W}$, $\overline{RES}$, CR (Without pull-up MOS)

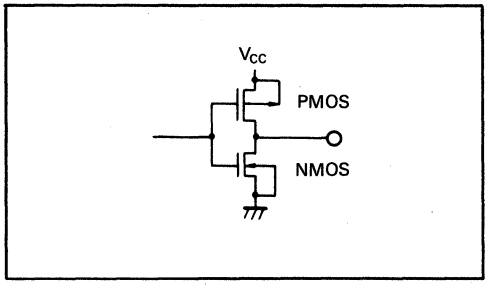


Applicable terminal: RD0–RD7 (With pull-up MOS)



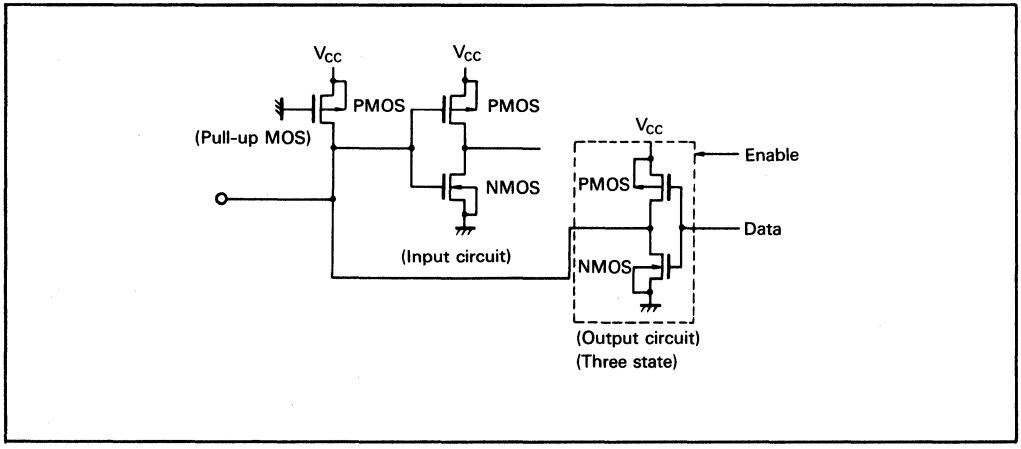
Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, CP0, D1, D2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA0–MA15



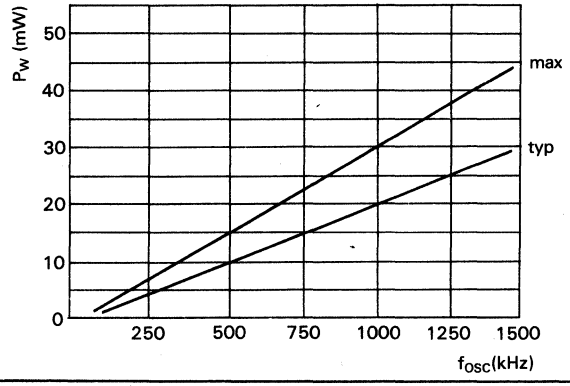
I/O Common Terminal

Applicable terminal: DB0–DB7, $\overline{SYNC}$ (with pull-up MOS), MD0–MD7 (without pull-up MOS)

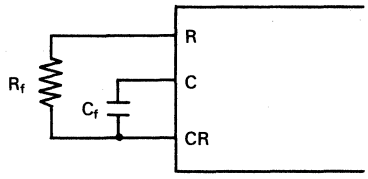


Notes:
1. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR, and $\overline{RES}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.
3. Applied to terminal $\overline{RES}$.
4. Applied to terminals $\overline{SYNC}$ and CR.
5. Applied to terminals DB0–DB7, $\overline{WE}$, MA0–MA15, and MD0–MD7.
6. Applied to terminals $\overline{SYNC}$, CP0, FLM, CL1, CL2, D1, D2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.
9. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

The relationship between the operating frequency and the power dissipation is given below.

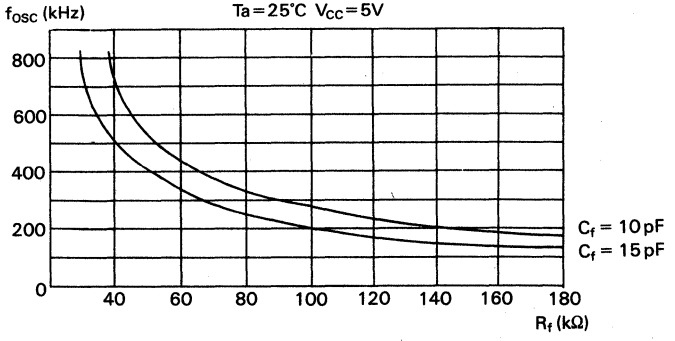


10. Applied to the operation of the internal oscillator when oscillation resistor R_f and oscillation capacity C_f are used.

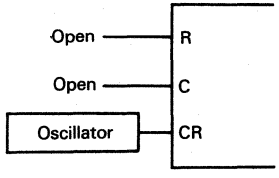


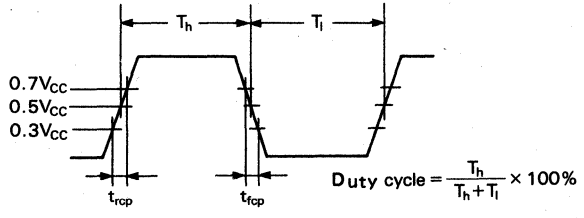
$C_f = 15\,pF \pm 5\%$
$R_f = 39\,k\Omega \pm 2\%$
(when f_{OSC} = 500 kHz typ)

The relationship among oscillation frequency, R_f and C_f is given below.



11. Applied to external clock operation.





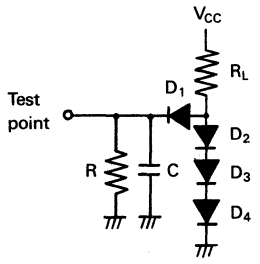
12. Applied to $\overline{SYNC}$, DB0–DB7, and RD0–RD7.

Timing Characteristics

MPU Interface

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	μs
Enable pulse width	High level	t_{WEH}	0.45	—	—	μs
	Low level	t_{WEL}	0.45	—	—	μs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time (Note)		t_{DDR}	—	—	225	ns
Data hold time		t_H	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Data hold time		t_{DH}	20	—	—	ns

Note: The following load circuit is connected for specification:



$R_L = 2.4\,k\Omega$
$R = 11\,k\Omega$
$C = 130\,pF$
Diodes D_1 to D_4 : 1S2074Ⓗ

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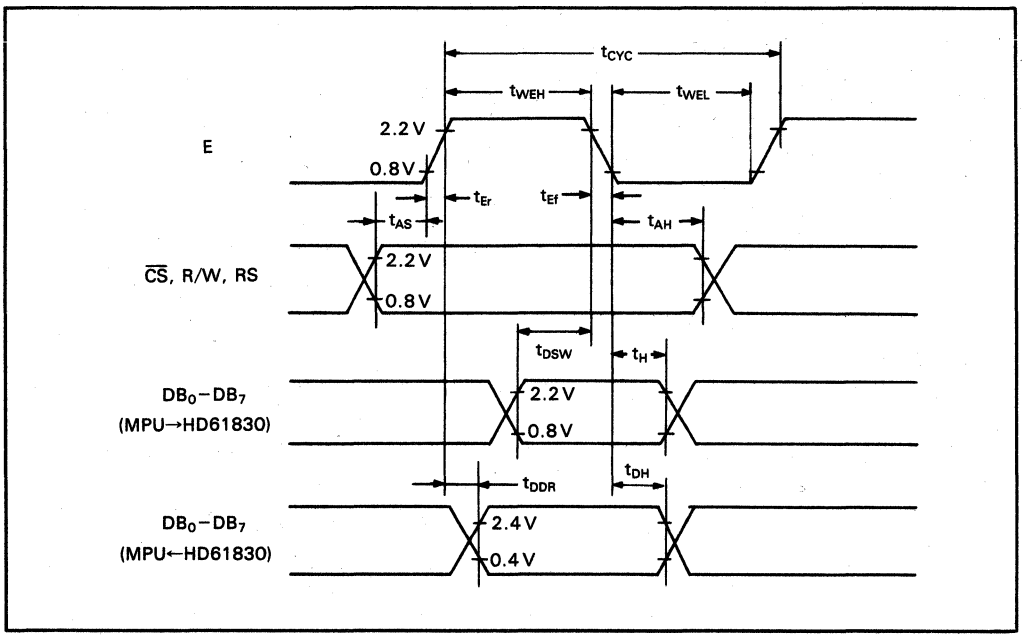
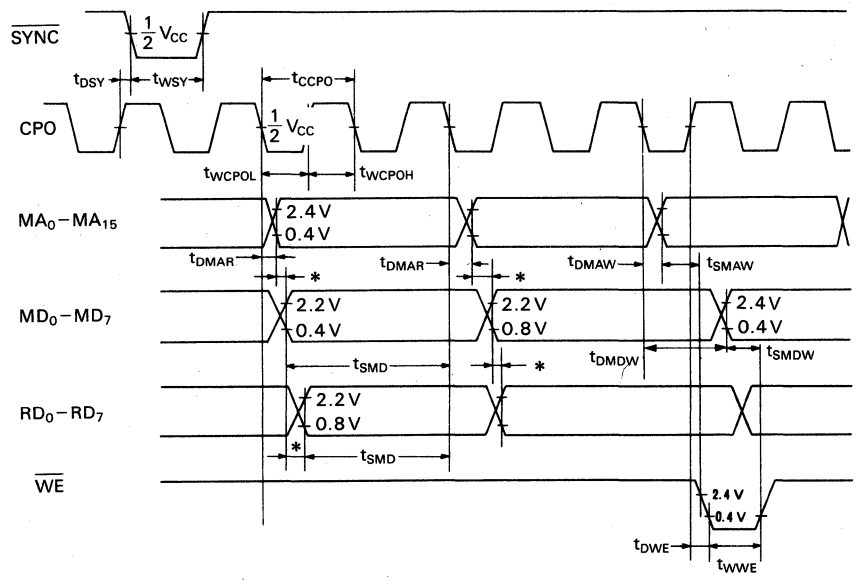

tCYC
tWEH
tWEL
E
2.2 V
0.8 V
tEr
tEf
tAS
tAH
CS, R/W, RS
2.2 V
0.8 V
tDSW
tH
DB0–DB7
(MPU→HD61830)
2.2 V
0.8 V
tDDR
tDH
DB0–DB7
(MPU←HD61830)
2.4 V
0.4 V

External RAM and ROM Interface

Item		Symbol	Min	Typ	Max	Unit
$\overline{SYNC}$ delay time		t_{DSY}	—	—	200	ns
$\overline{SYNC}$ pulse width	High level	t_{WSY}	900	—	—	ns
CP0 cycle time		t_{CCP0}	900	—	—	ns
CP0 pulse width	High level	t_{WCP0H}	450	—	—	ns
	Low level	t_{WCP0L}	450	—	—	ns
MA0 to MA15 refresh delay time		t_{DMAR}	—	—	200	ns
MA0 to MA15 write address delay time		t_{DMAW}	—	—	200	ns
MD0 to MD7 write data delay time		t_{DMDW}	—	—	200	ns
MD0 to MD7, RD0 to RD7 setup time		t_{SMD}	900	—	—	ns
Memory address setup time		t_{SMAW}	250	—	—	ns
Memory data setup time		t_{SMDW}	250	—	—	ns
$\overline{WE}$ delay time		t_{DWE}	—	—	200	ns
$\overline{WE}$ pulse width (low level)		t_{WWE}	450	—	—	ns



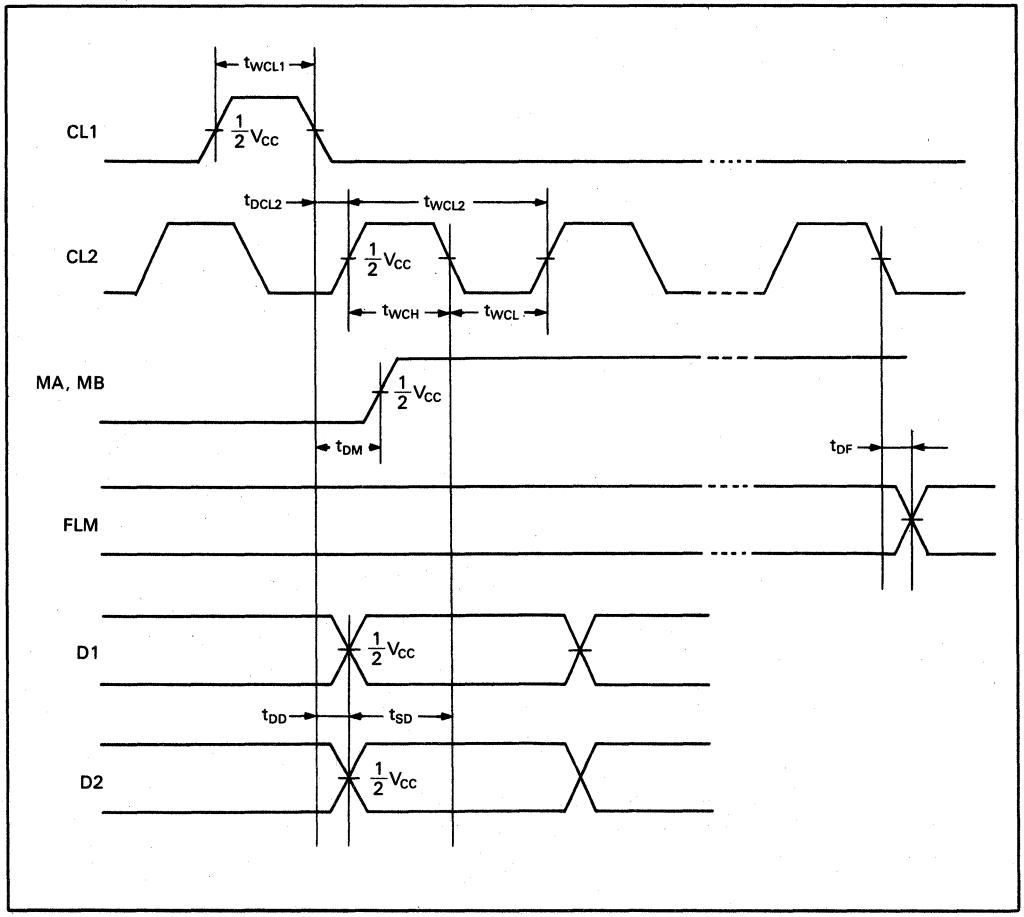
Notes: 1. No load is applied to all the output terminals.
2. "*" indicates the delay time of RAM and ROM.

5

LCD Driver Interface

Item		Symbol	Min	Typ	Max	Unit
Clock pulse width (high level)		t_{WCL1}	450	—	—	ns
Clock delay time		t_{DCL2}	—	—	200	ns
Clock cycle time		t_{WCL2}	900	—	—	ns
Clock pulse width	High level	t_{WCH}	450	—	—	ns
	Low level	t_{WCL}	450	—	—	ns
MA, MB delay time		t_{MD}	—	—	300	ns
FLM delay time		t_{DF}	—	—	300	ns
Data delay time		t_{DD}	—	—	200	ns
Data setup time		t_{SD}	250	—	—	ns

Note: No load is applied to all the output terminals (MA, MB, FLM, D1, and D2).



Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS = 1, and the data register code is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS = 0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

1. Mode control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
I/O	I/O	0	0	0	0	Cursor off	Internal CG	Character display (Character mode)
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor off	External CG	
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display on/off	Master/slave	Blink	Cursor	Graphic/character mode	Ext./Int. CG			

1: Master mode
0: Slave mode

1: Display on
0: Display off

5

2. Set character pitch

Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is included in the determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

Hp indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values (table 1).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p − 1) binary				0	(H_p − 1) binary		

Table 1 H_p Values

Hp	DB2	DB1	DB0	Horizontal character pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8

3. Set number of characters

H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = Hp \times H_N$$

H_N can be set to an even number from 2 to 128 (decimal).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	(H_N − 1) binary						

4. Set number of time divisions (inverse of display duty ratio)

Nx indicates the number of time divisions in multiplex display.
1/Nx is the display duty ratio.
A value of 1 to 128 (decimal) can be set to Nx.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time-divisions reg.	0	0	0	(N_X − 1) binary						

5. Set cursor position

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5 × 7 dot font, the cursor is displayed under a character by specifying Cp = 8 (decimal). The cursor horizontal length is equal to the horizontal character pitch Hp. A value of 1 to 16 (decimal) can be set to Cp. If a smaller value than the vertical character pitch Vp is set (Cp ≦ Vp), and a character overlaps with the cursor, the cursor has higher priority of display (at cursor display on). If Cp is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to Hp.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(C_p − 1) binary			

6. Set display start low order address

Cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address (DB_3–DB_0) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

7. Set cursor address (low order) (RAM write low order address)

Cause cursor addresses to be written in the cursor address counters. The cursor address indicates and address for sending or receiving display data and character codes to or from the RAM.

That is, data at the address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the character specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements setting the cursor address (table 2).

The cursor address counter is a 16-bit up-counter with set and reset functions. When bit N changes from 1 to 0, bit N + 1 is inclemented by 1. When setting the low order address, the LSB (bit 1) of the high order address is inclemented by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in the table 2.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

Table 2 Cursor Address Setting

Condition	Requirement
When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
When you want to rewrite only the low order address.	Don't fail to set the high order address again after setting the low order address.
When you want to rewrite only the high order address.	Set the high order address. You don't have to set the low order address again.

8. Write display data

After the code $"OC" is written into the instruction register with RS = 1, 8-bit data with RS = 0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

9. Read display data

Data can be read from the RAM with RS = 0 after writing code $"OD" into the instruction register. Figure 1 shows the read procedure.

This instruction outputs the contents of data output register on the data bus (DB0 to DB7) and then transfers RAM data specified by the cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second one. Thus, make one dummy read when reading data after setting the cursor address.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MBS (pattern data, character code) LSB							

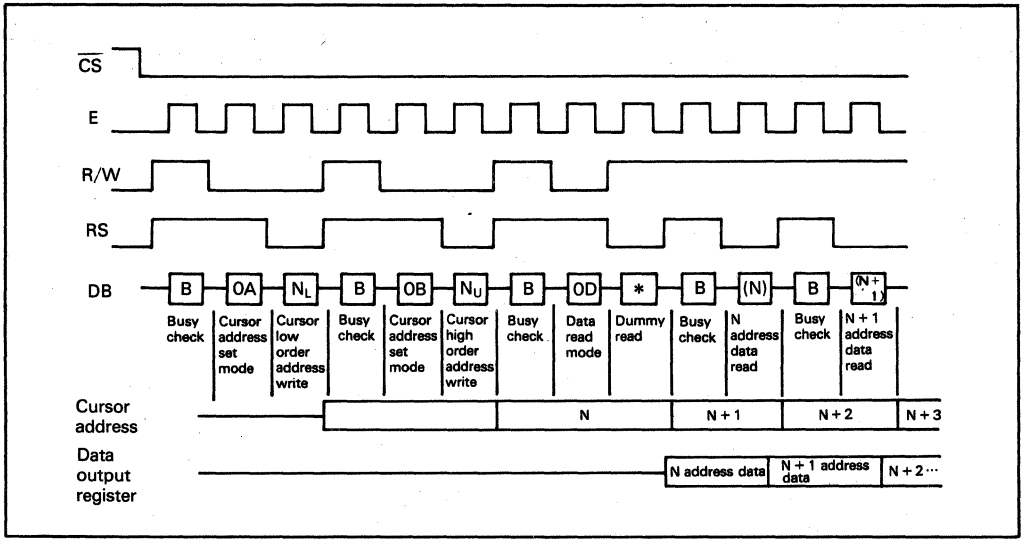


Figure 1 Read Procedure

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10. Clear bit

The clear/set bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value from 1 to 8. N_B = 1 and N_B = 8 indicates LSB and MSB, respectively.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B − 1) binary		

Set bit

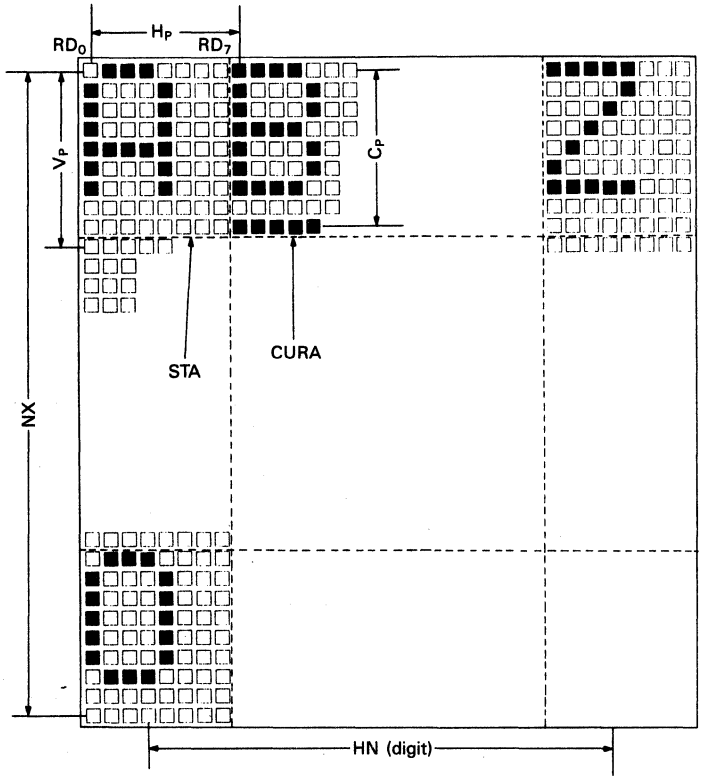
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B − 1) binary		

11. Read busy flag

When the read mode is set with RS = 1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of the other instructions. After the execution, it is set to 0. The next instruction can be accepted. No instruction can be acceped when busy flag = 1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS = 1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS = 1.

The busy flag can be read without specifying any instruction register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	I/O							



Symbol	Name	Meaning	Value
H_P	Horizontal character pitch	Horizontal character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of horizountal characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode.	2 to 128 digits (an even number)
V_p	Vertical character pitch	Vertical character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_X	Number of time divisions	Inverse of display duty ratio	1 to 128 lines

Note: If the number of vertical dots on the screen is m, and the number of horizontal dots is n,

$1/m = 1/N_X$ = display duty ratio
$n = H_p \times H_N$, m/V_p = Number of display lines
$C_p \leq V_p$

Figure 2 Display Variables

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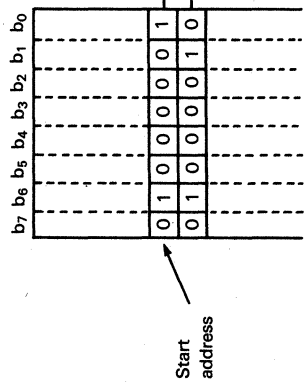
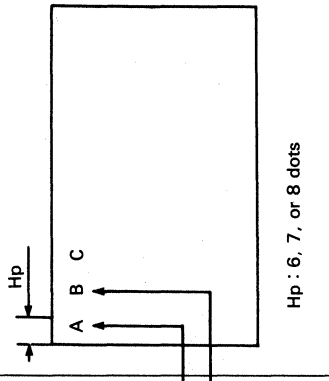
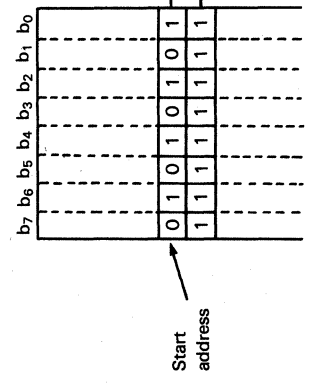
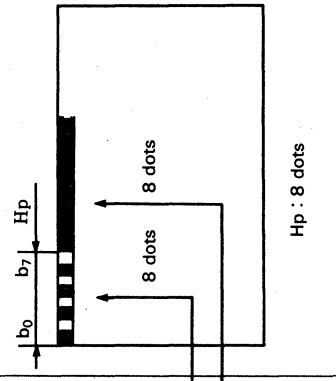
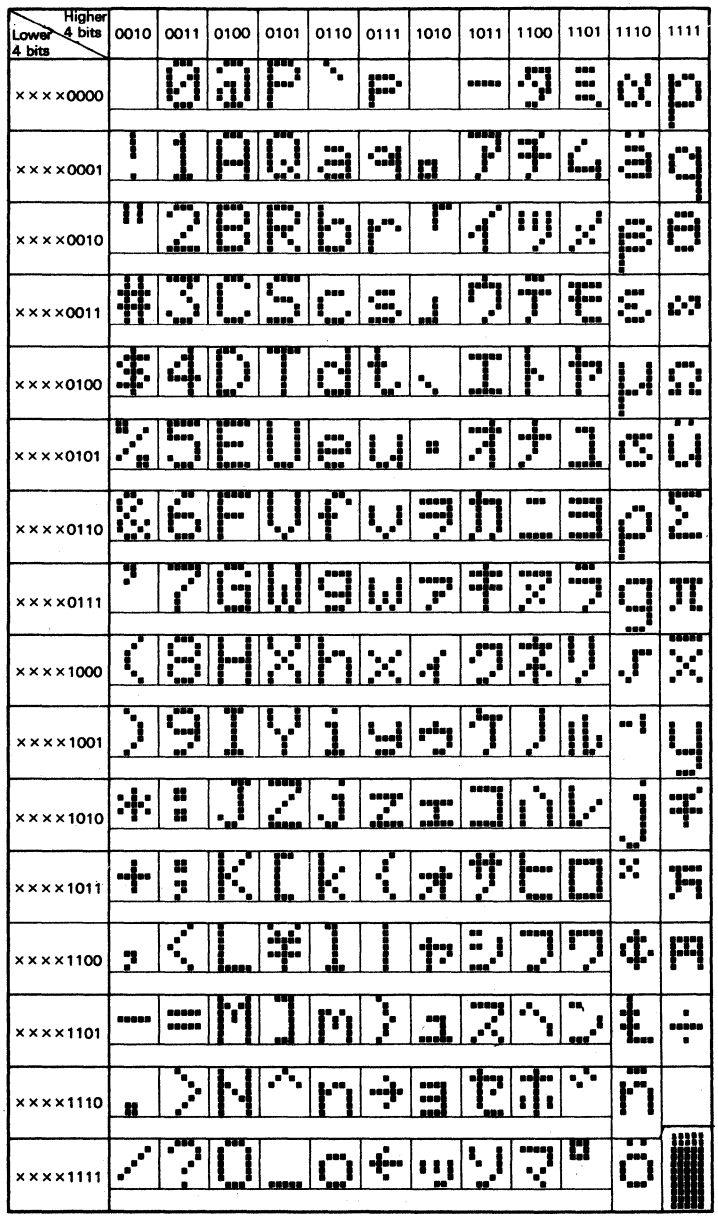
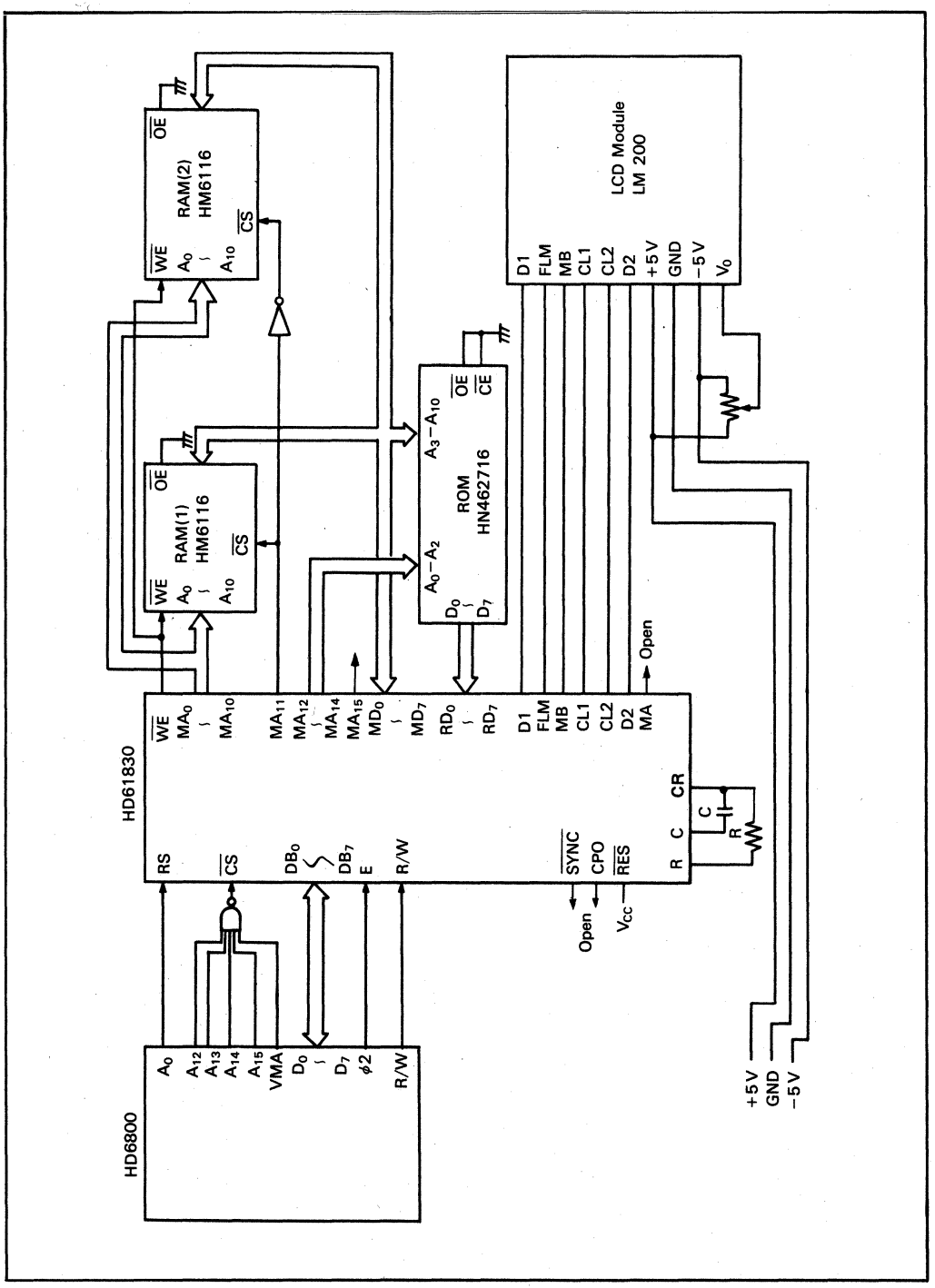
Display Mode

Display Mode	Display Data from MPU	RAM	Liquid Crystal Display Panel
Character display	Character code (8 bits)		
Graphic	Display pattern (8 bits)		

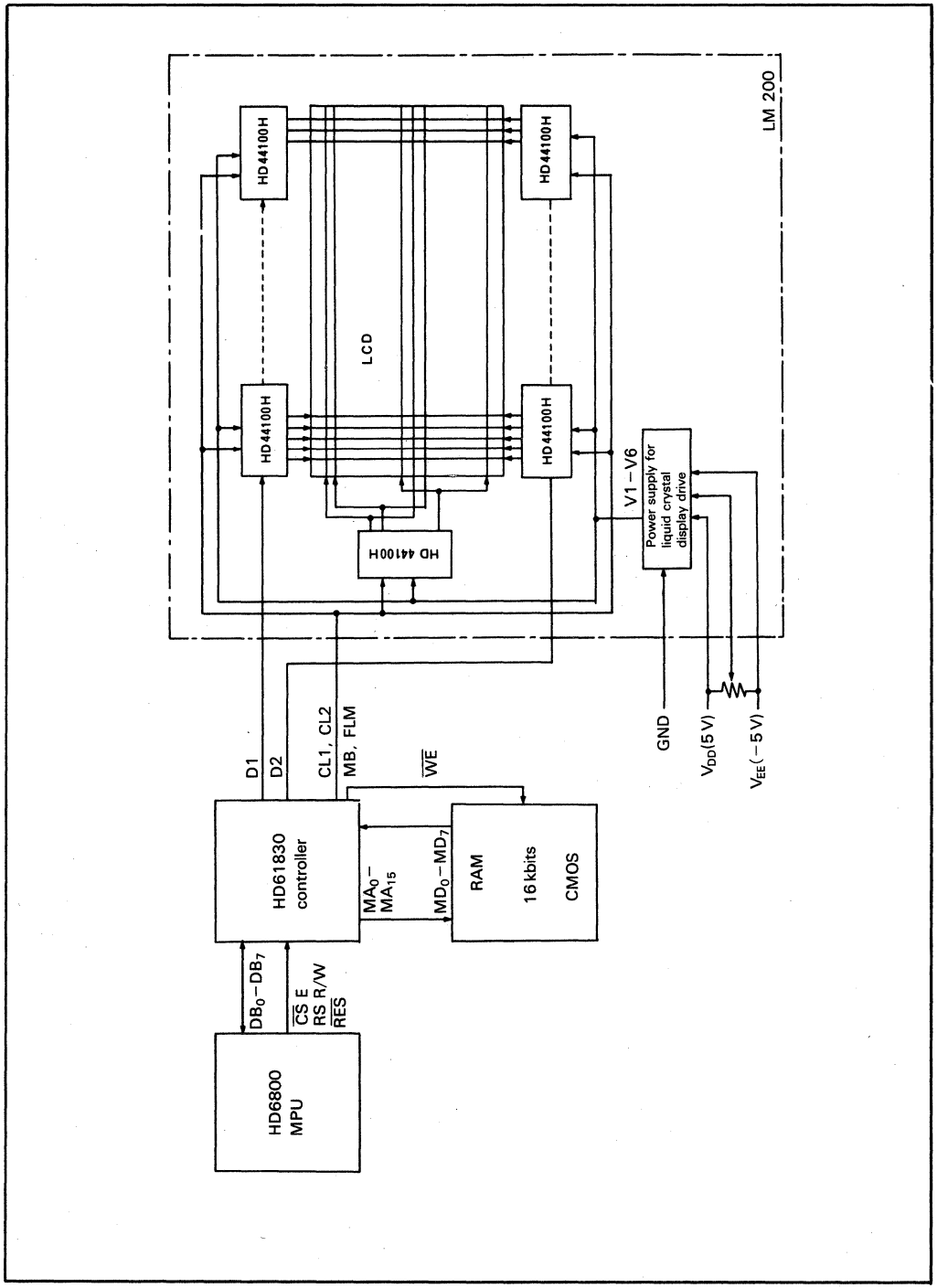
Internal Character Generator Patterns and Character Codes



Application (Character Mode, External CG, Character Font 8 × 8)



Application 2 (Graphic Mode)



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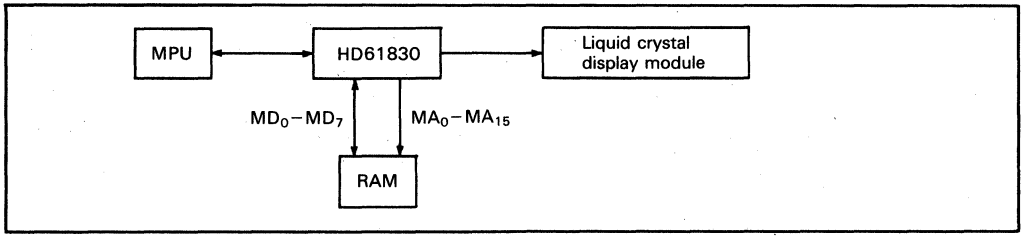
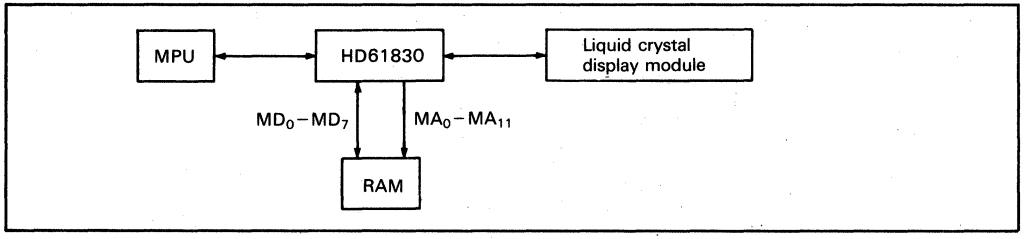
Configuration Examples

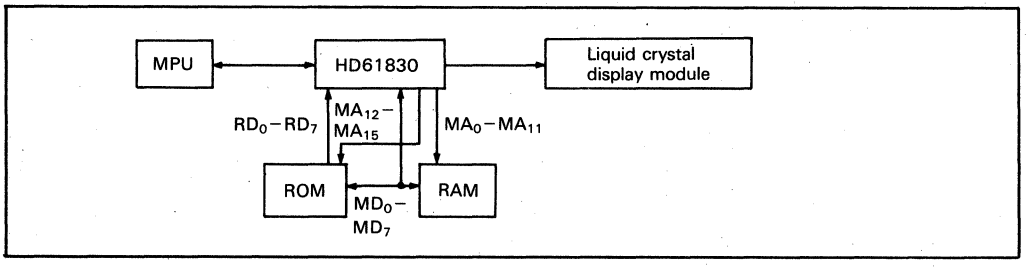
Graphic Mode



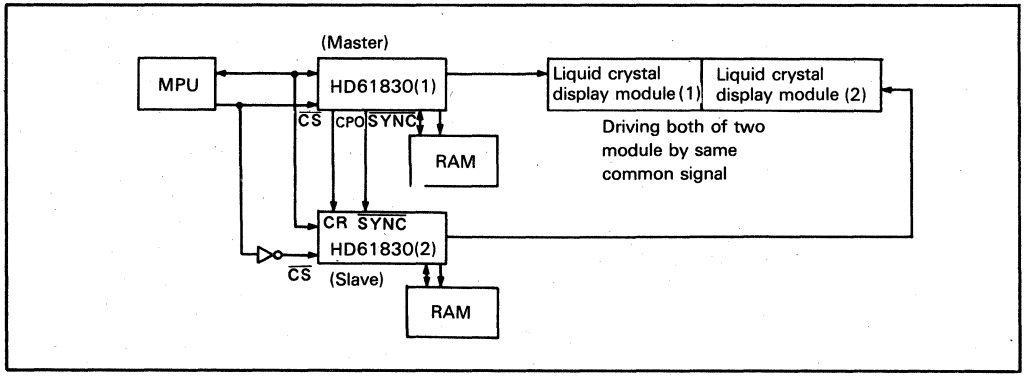
Character Mode (1) (Internal Character Generator)



Character Mode (2) (External Character Generator)



Parallel Operation



HD61830B
LCTC (LCD Timing Controller)

Description

The HD61830B is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcontroller in the external RAM to generate dot matrix liquid crystal driving signals.

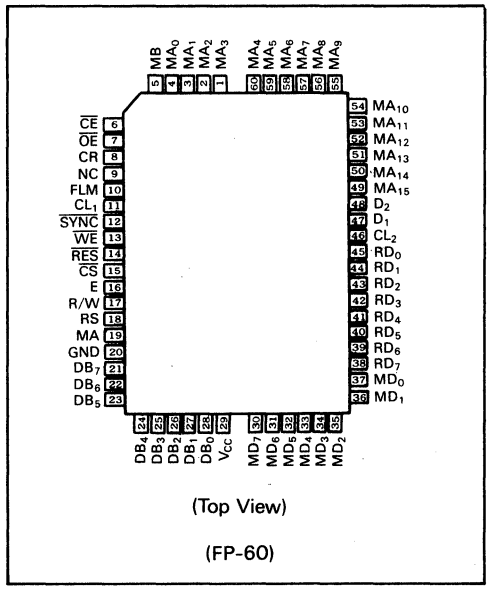
It has a graphic mode in which 1-bit data in the external RAM corresponds to the on/off state of 1 dot on liquid crystal display and a character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830B is produced by the CMOS process. Thus, combined with a CMOS microcontroller it can complete a liquid crystal display device with lower power dissipation.

Features

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - −Graphic mode: 512k dots (2^{16} bytes)
  - −Character mode: 4096 characters (2^{12} characters)
- Internal character generator ROM: 7360 bits
  - −160 types of 5 × 7 dot characters
  - −32 types of 5 × 11 dot characters
    Total 192 characters
  - −Can be extended to 256 characters (4k bytes max.) by external ROM
- Interfaces to 8-bit MPU
- Display duty cycle (Can be selected by a program)
  Static to 1/128 duty cycle
- Various instruction functions
  - −Scroll, Cursor on/off/blink, Character blink, Bit manipulation
- Display method: Selectable A or B types
- Operating frequency: 2.4 MHz
- Low power dissipation
- Power supply: Single +5 V ± 10%
- CMOS process
- Package: 60-pin plastic QFP (FP-60)

Pin Arrangement



(Top View)

(FP-60)

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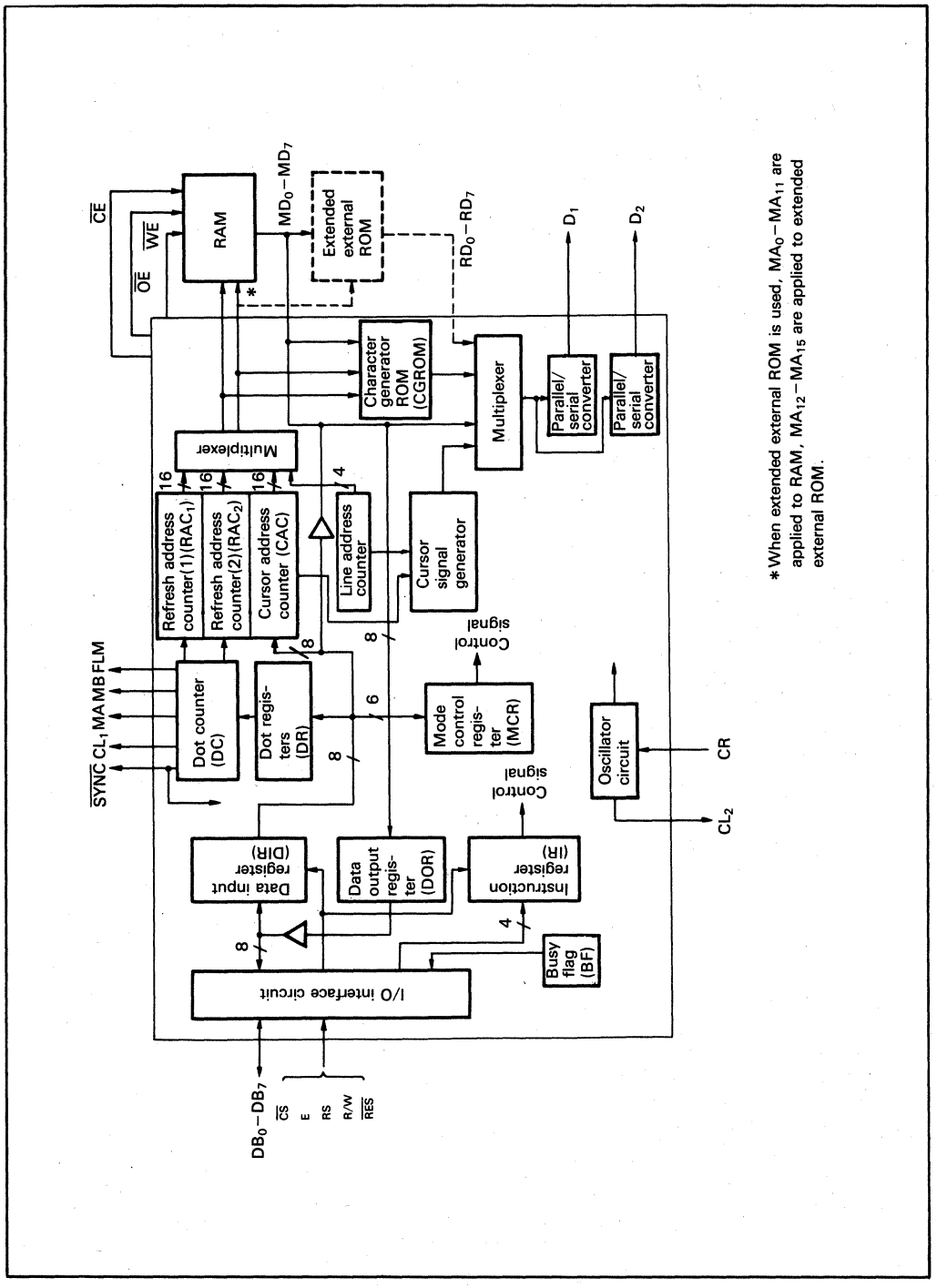
Block Diagram



Block Functions

Registers

The HD61830B has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR), and mode control register (MCR).

The IR is a 4-bit register that stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register, and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR, and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E segnal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at the High level).

The DR are registers used to store dot information such as character pitches and the number of vertical dots and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display on/off and cursor on/off/blink. The information sent from the MPU is written in it via the DIR.

Busy Flag (BF)

The busy flag = 1 indicates the HD61830B is performing an internal operation. Instructions cannot be accepted. As shown in Control Instruction, read busy flag, the busy flag is output on DB7 under the conditions of RS = 1, R/W = 1, and E = 1. Make sure the busy flag is 0 before writing the next instruction.

Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

Refresh Address Counters (RAC1/RAC2)

The refresh address counters RAC1 and RAC2 control the addresses of external RAM, character generator ROM (CGROM), and extended external ROM. The RAC1 is used for upper half of the screen and the RAC2 for the lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12−MA15) are ignored. The 4 bits of line address counter are output instead and used as the address of extended ROM.

Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The charater font is 5 × 7 (160 characters) or 5 × 11 (32 characters). The use of extended ROM allows 8 × 16 (256 characters max.) to be used.

Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by instruction. It holds an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of the cursor address counter is automatically increased by 1 after the display data is read or written and after the set/clear bit instruction is executed.

Cursor Signal Generator

The cursor can be displayed by instruction in character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM, or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

Terminal Functions

Name	Function
DB0–DB7	Data bus: Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7.
$\overline{CS}$	Chip select: Selected state with $\overline{CS}$ = 0
R/W	Read/Write: R/W = 1: MPU ← HD61830B R/W = 0: MPU → HD61830B
RS	Register select: RS = 1: Instruction register RS = 0: Data register
E	Enable: Data is written at the fall of E Data can be read while E is 1
CR	External clock input
$\overline{RES}$	Reset: $\overline{RES}$ = 0 results in display off, slave mode and Hp = 6
MA0–MA15	External RAM address output In character mode, the lane code for external CG is output through MA12 to MA15 (0: Character 1st line, F: Character 16th line)
MD0–MD7	Display data bus: Three-state I/O common terminal
RD0–RD7	ROM data input: Dot data from external character generator is input
$\overline{WE}$	Write enable: Write signal for external RAM
CL2	Display data shift clock for LCD drivers
CL1	Display data latch signal for LCD drivers
FLM	Frame signal for display synchronization
MA	Signal for converting liquid crystal driving signal into AC, A type
MB	Signal for converting liquid crystal driving signal into AC, B type
D1, D2	Display data serial output D1: For upper half of screen D2: For lower half of screen
$\overline{SYNC}$	Synchronous signal for parallel operation Three-state I/O common terminal (with pull-up MOS) Master: Synchronous signal is output Slave: Synchronous signal is input
$\overline{CE}$	Chip enable $\overline{CE}$ = 0: Chip enables make external RAM in active
$\overline{OE}$	Output enable $\overline{OE}$ = 1: Output enable informs external RAM that HD61830B requires data bus
NC	Unused terminal. Don't connect any wires to this terminal

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	− 0.3 to + 0.7	V	1, 2
Terminal voltage	V_T	− 0.3 to V_{CC} + 0.3	V	1, 2
Operating temperature	T_{opr}	− 20 to + 75	°C	
Storage temperature	T_{stg}	− 55 to + 125	°C	

Notes: 1. All voltage is referred to GND = 0 V.
2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage (TTL)	V_{IH}	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	V_{IL}	0	—	0.8	V		2
Input high voltage	V_{IHR}	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	V_{IHC}	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	V_{ILC}	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	V_{OH}	2.4	—	V_{CC}	V	− I_{OH} = 0.6 mA	5
Output low voltage (TTL)	V_{OL}	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	V_{OHC}	V_{CC} − 0.4	—	V_{CC}	V	− I_{OH} = 0.6 mA	6
Output low voltage (CMOS)	V_{OLC}	0	—	0.4	V	I_{OI} = 0.6 mA	6
Input leakage current	I_{IN}	− 5	—	5	μA	V_{IN} = 0−V_{CC}	7
Three-state leakage current	I_{TSL}	− 10	—	10	μA	V_{OUT} = 0−V_{CC}	8
Pull-up current	I_{PL}	2	10	20	μA	V_{in} = GND	9
Power dissipation	P_W	—	—	50	mW	External clock f_{cp} = 2.4 MHz	10

Notes: 1. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR, and $\overline{RES}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.
3. Applied to terminal $\overline{RES}$.
4. Applied to terminals $\overline{SYNC}$ and CR.
5. Applied to terminals DB0−DB7, $\overline{WE}$, MA0−MA15, $\overline{OE}$, $\overline{CE}$, and MD0−MD7.
6. Applied to terminals $\overline{SYNC}$, FLM, CL1, CL2, D1, D2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.
9. Applied to $\overline{SYNC}$, DB0−DB7, and RD0−RD7.
10. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

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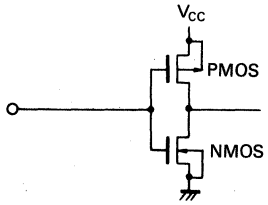
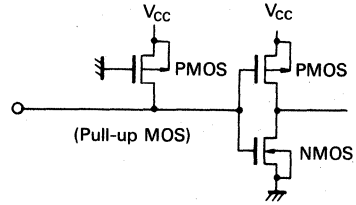
Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (Without pull-up MOS)

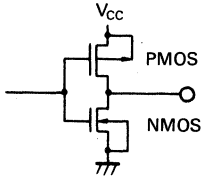


Applicable terminal: RD0–RD7 (With pull-up MOS)



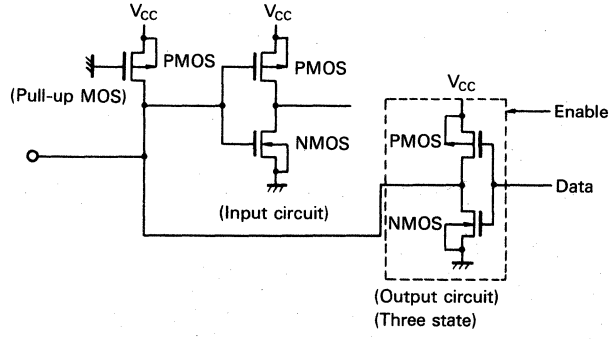
Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, D1, D2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA0–MA15



I/O Common Terminal

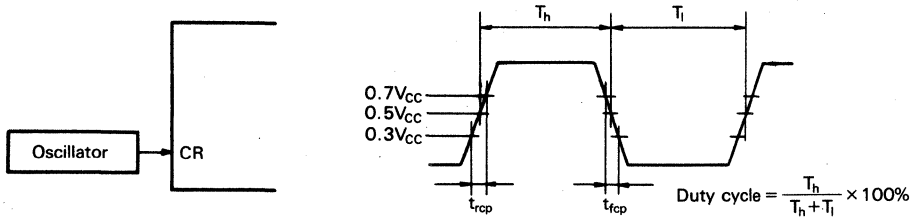
Applicable terminal: DB0–DB7, $\overline{SYNC}$, MD0–MD7 (MD0–MD7 have no pull-up MOS)



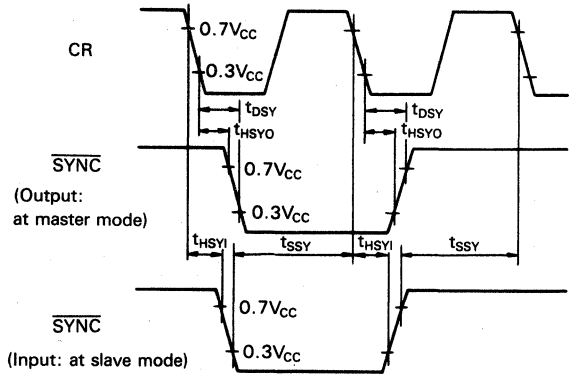
Clock Operation

Item	Symbol	Min	Typ	Max	Unit	Note
External clock operating frequency	f_{cp}	100	—	2400	kHz	1
External clock duty	Duty	47.5	50	52.5	%	1
External clock rise time	t_{rcp}	—	—	25.0	ns	1
External clock fall time	t_{fcp}	—	—	25.0	ns	1
$\overline{SYNC}$ output hold time	t_{HSYO}	30	—	—	ns	2, 3
$\overline{SYNC}$ output delay time	t_{DSY}	—	—	210	ns	2, 3
$\overline{SYNC}$ input hold time	t_{HSYI}	10	—	—	ns	2
$\overline{SYNC}$ input set-up time	t_{SSY}	—	—	180	ns	2

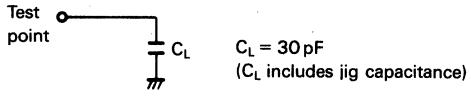
Notes: 1. Applied to external clock input terminal.



2. Applied to $\overline{SYNC}$ terminal.



3. Testing load circuit.



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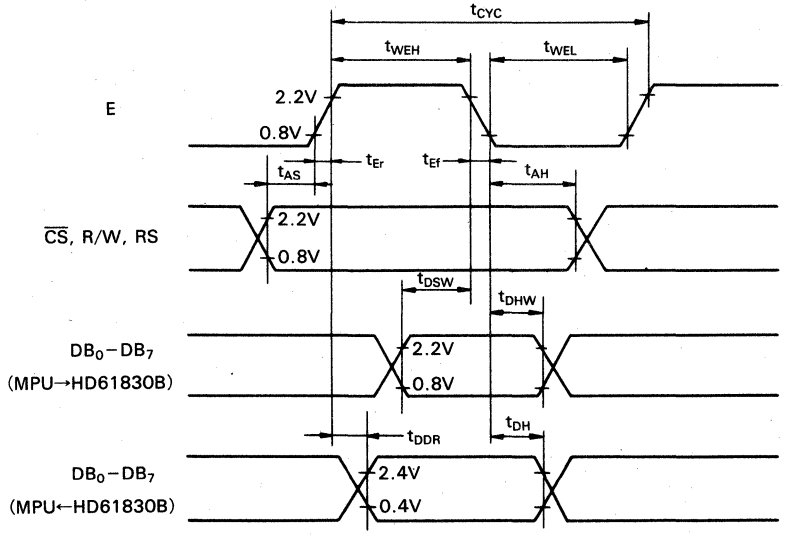
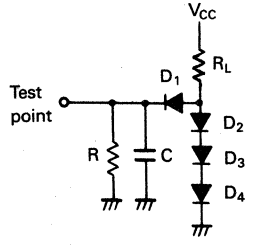
MPU Interface

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	μs
Enable pulse width	High level	t_{WEH}	0.45	—	—	μs
	Low level	t_{WEL}	0.45	—	—	μs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time		t_{DDR}	—	—	225	ns (Note)
Data hold time		t_{DHW}	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Data hold time		t_{DH}	20	—	—	ns

Note: The following load circuit is connected for specification:



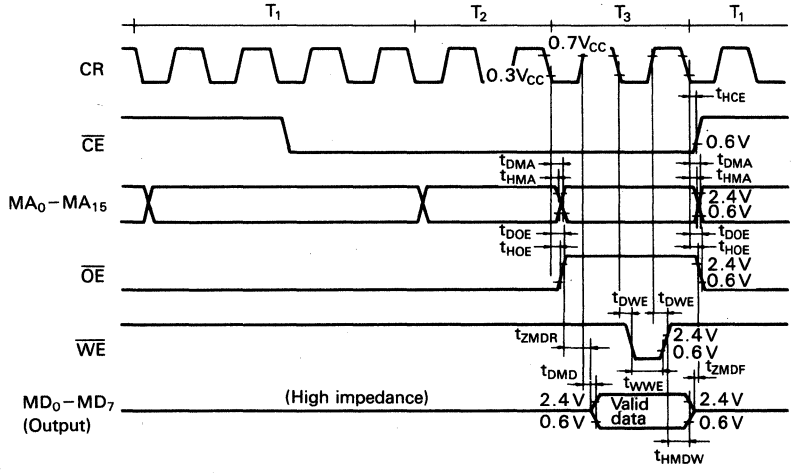


$R_L = 2.4\,k\Omega$
$R = 11\,k\Omega$
$C = 130$ pF (C includes jig capacitance)
Diodes D_1 to D_4: 1S2074Ⓗ

External RAM and ROM Interface

Item	Symbol	Min	Typ	Max	Unit	Note
MA0–MA15 delay time	t_{DMA}	—	—	300	ns	1, 2, 3
MA0–MA15 hold time	t_{HMA}	40	—	—	ns	1, 2, 3
$\overline{CE}$ delay time	t_{DCE}	—	—	300	ns	1, 2, 3
$\overline{CE}$ hold time	t_{HCE}	40	—	—	ns	1, 2, 3
$\overline{OE}$ delay time	t_{DOE}	—	—	300	ns	1, 3
$\overline{OE}$ hold time	t_{HOE}	40	—	—	ns	1, 3
MD output delay time	t_{DMD}	—	—	150	ns	1, 3
MD output hold time	t_{HMDW}	10	—	—	ns	1, 3
$\overline{WE}$ delay time	t_{DWE}	–	—	150	ns	1, 3
$\overline{WE}$ clock pules width	t_{WWE}	150	—	—	ns	1, 3
MD output high impedance time (1)	t_{ZMDF}	10	—	—	ns	1, 3
MD output high impedance time (2)	t_{ZMDR}	50	—	—	ns	1, 3
RD data set-up time	t_{SRD}	50	—	—	ns	2
RD data hold time	t_{HRD}	40	—	—	ns	2
MD data set-up time	t_{SMD}	50	—	—	ns	2
MD data hold time	t_{HMD}	40	—	—	ns	2

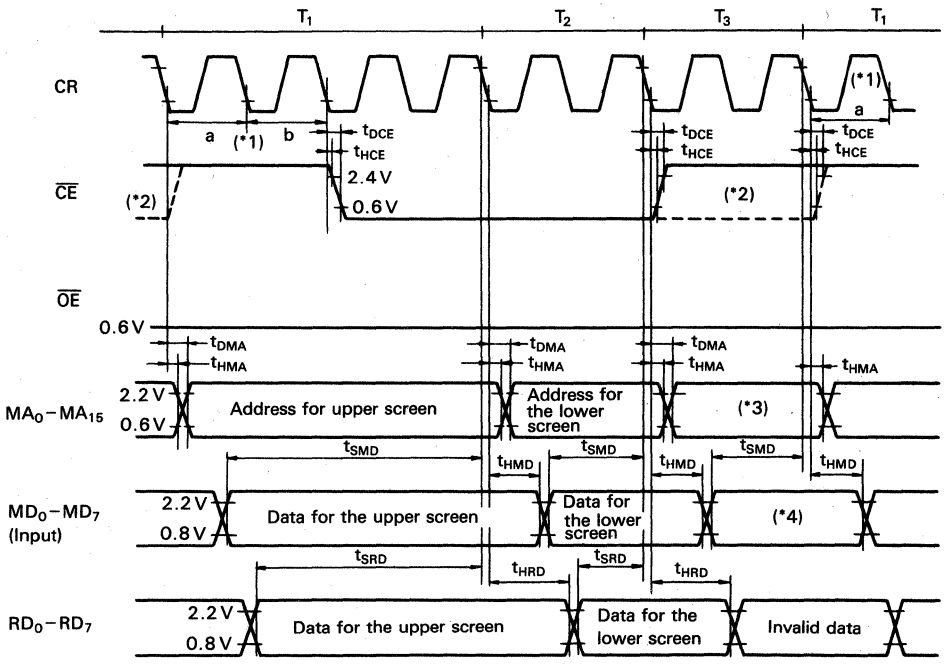
Notes: 1. RAM write timing



T1: Memory data refresh timing for upper screen
T2: Memory data refresh timing for lower screen
T3: Memory read/write timing

5

Notes: 2. ROM/RAM read timing



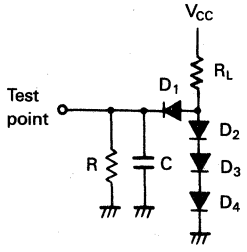
*1 This figure shows the timing for Hp = 8.
For Hp = 7, time shown by "b" becomes zero. For Hp = 6, time shown by "a" and "b" become zero.
Therefore, the number of clock pulses during T1 become 4, 3, or 2 in the case of Hp = 8, Hp = 7, or Hp = 6 respectively.

*2 The waveform for instructions with memory read is shown with a dash line. In other cases, the waveform shown with a solid line is generated.

*3 When an instruction with RAM read/write is excuted, the value of cursor address is output. In other cases, invalid data is output.

*4 When an instruction with RAM read is excuted, HD61830B latches the data at this timing. In other cases, this data is invalid.

3. Test load circuit

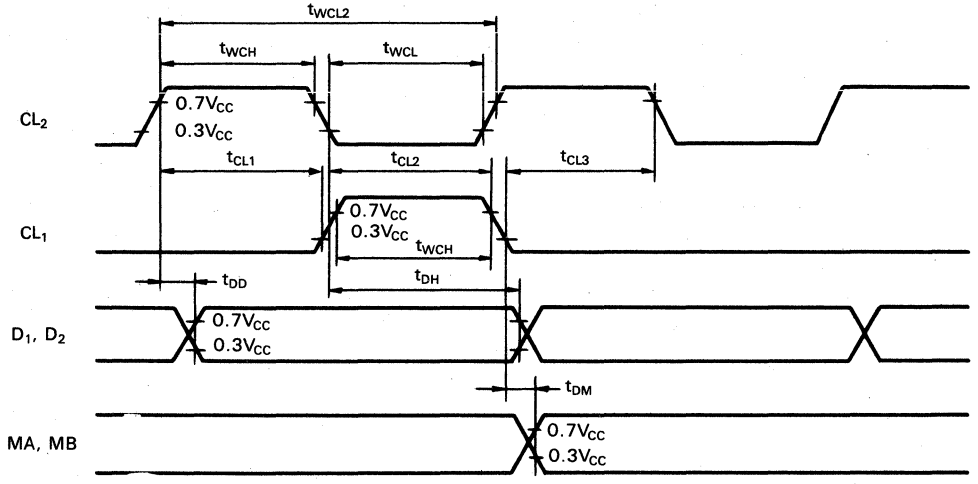


$R_L = 2.4\,k\Omega$
$R = 11\,k\Omega$
$C = 50\,pF$ (C includes jig capacitance)
Diodes D_1 to D_4: 1S2074Ⓗ

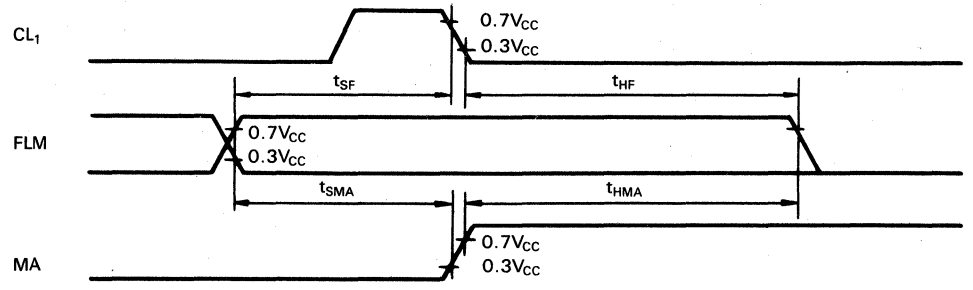
LCD Driver Interface

Item	Symbol	Min	Typ	Max	Unit	Note
Clock cycle time	t_{WCL2}	416	—	—	ns	1, 3
Clock pulse width (High level)	t_{WCH}	150	—	—	ns	1, 3
Clock pulse width (Low level)	t_{WCL}	150	—	—	ns	1, 3
Data delay time	t_{DD}	—	—	50	ns	1, 3
Data hold time	t_{DH}	100	—	—	ns	1, 3
Clock phase difference (1)	t_{CL1}	100	—	—	ns	1, 3
Clock phase difference (2)	t_{CL2}	100	—	—	ns	1, 3
Clock phase difference (3)	t_{CL3}	100	—	—	ns	1, 3
MA, MB delay time	t_{DM}	−200	—	200	ns	1, 3
FLM set-up time	t_{SF}	400	—	—	ns	2, 3
FLM hold time	t_{HF}	1000	—	—	ns	2, 3
MA set-up time	t_{SMA}	400	—	—	ns	2, 3
MA hold time	t_{HMA}	1000	—	—	ns	2, 3

Notes: 1.



2.



3. Test load circuit

Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS = 1, and the data register code is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS = 0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

1. Mode control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
I/O	I/O	0	0	0	0	Cursor off	Internal CG	Character display (Character mode)
		0	1			Cursor on		
		1	0			Cursor off, Character blink		
		1	1			Cursor blink		
		0	0		1	Cursor off	External CG	
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/slave	Blink	Cursor	Graphic/character mode	Ext./Int. CG			

1: Master mode
0: Slave mode

1: Display ON
0: Display OFF

5

2. Set character pitch

Vp indicates the number of vertical dots per character. The spece between the vertically-displayed characters is considered for determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

Hp indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values (Table 1).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p − 1) binary				0	(H_p − 1) binary		

3. Set number of characters

H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = Hp \times H_N$$

H_N can be set to an even number from 2 to 128 (decimal).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	(H_N −1) binary						

Table 1 H_p Values

Hp	DB2	DB1	DB0	Horizontal character pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8

4. Set number of time divisions (inverse of display duty ratio)

Nx indicates the number of time divisions in multiplex display. 1/Nx is the display duty ratio.

A value of 1 to 128 (decimal) can be set to Nx.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time shares reg.	0	0	0	(N_X − 1) binary						

5. Set cursor position

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5 × 7 dot font, the cursor is displayed under a character by specifying Cp = 8 (decimal). The cursor horizontal length is equal to the horizontal character pitch Hp. A value of 1 to 16 (decimal) can be set to Cp. If a smaller value than the vertical character pitch Vp is set (Cp ≦ Vp), and a character overlaps with the cursor, the cursor has higher priority of display (at cursor display on). If Cp is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to Hp.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(C_p − 1) binary			

6. Set display start low order addres

Cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address (DB_3–DB_0) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

7. Set cursor address (low order) (RAM write low order address)

Cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM.

That is, data at the address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the character specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements when setting the cursor address (Table 2).

The cursor address counter is a 16-bit up-counter with set and reset functions. When bit N changes from 1 to 0, bit N + 1 is incremented by 1. When setting the low order address, the LSB (bit 1) of the high order address is added by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in table 2.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

Table 2 Cursor Address Setting

Condition	Requirement
When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
When you want to rewrite only the low order address.	Don't fail to set the high order address again after setting the low order address.
When you want to rewrite only the high order address.	Set the high order address. You don't have to set the low order address again.

8. Write display data

After the code $"0C" is written into the instruction register with RS = 1, 8 bit data with RS = 0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

9. Read display data

Data can be read from the RAM with RS = 0 after writing code $"0C" into the instruction register. Figure 1 shows the read procedure.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MBS (pattern data, character code) LSB							

This instruction outputs the contents of data output register on the data bus (DB0 to DB7) and then transfers RAM data specified by the cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second one. Thus, make one dummy read when reading data after setting the cursor address.

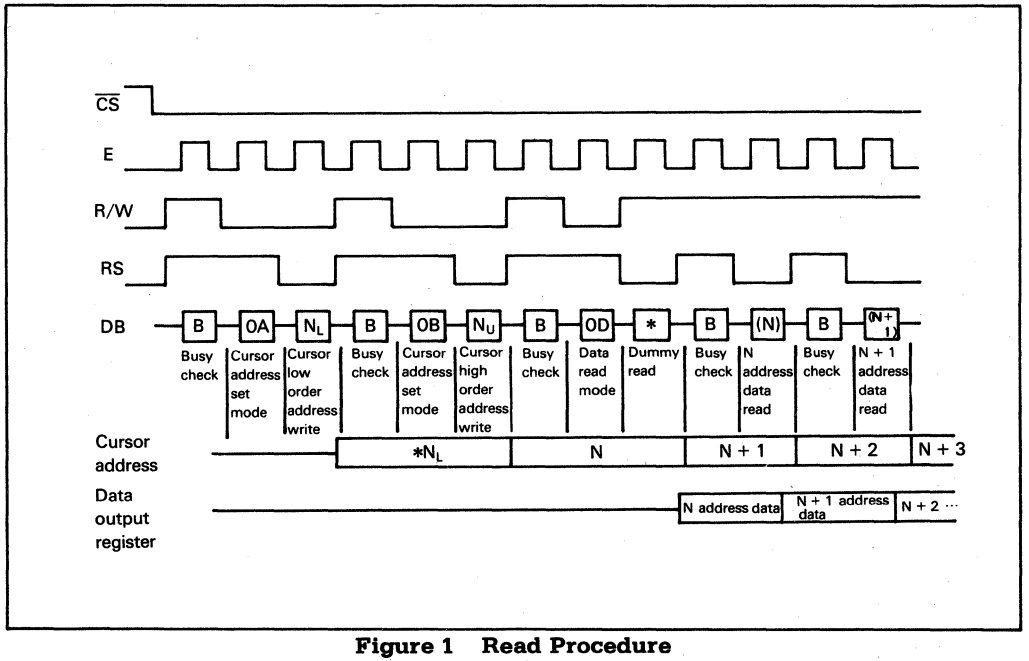


Figure 1 Read Procedure

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10. Clear bit

The clear/set bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value from 1 to 8. N_B = 1 and N_B = 8 indicates LSB and MSB, respectively.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B − 1) binary		

Set bit

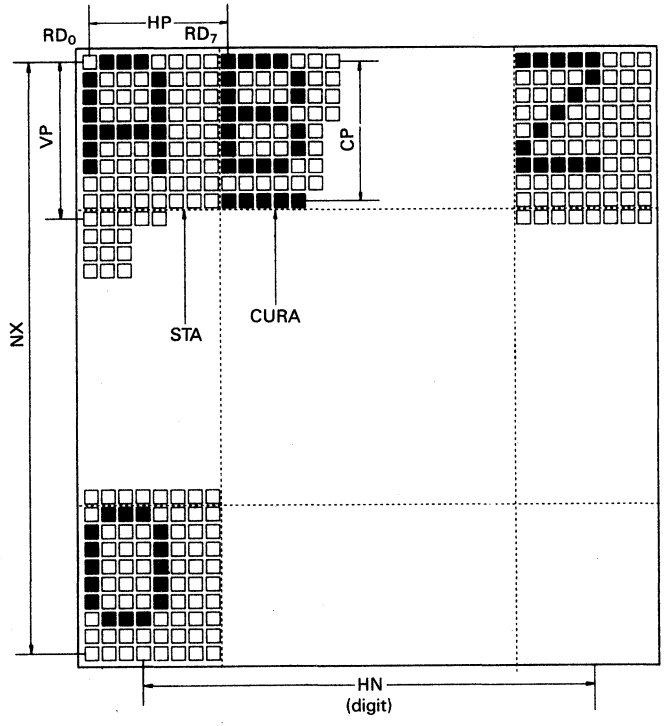
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B − 1) binary		

11. Read busy flag

When the read mode is set with RS = 1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of the other instructions. After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag = 1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS = 1), busy flag doesn't change. Thus, no busy flag check is required just after the write operation into the instruction register with RS = 1.

The busy flag can be read without specifying any instruction register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	I/O	*						



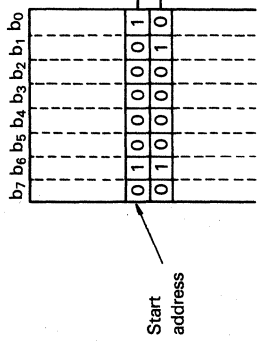
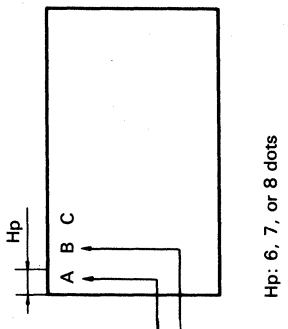
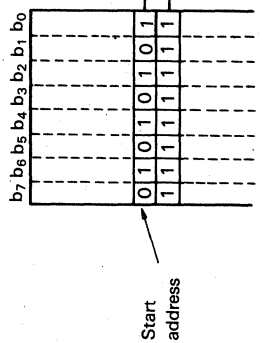
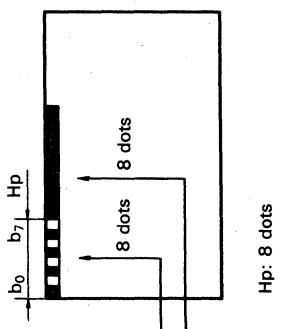
Symbol	Name	Meaning	Value
H_p	Horizontal character fitch	Horizontal character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of horizontal characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode	2 to 128 digits (an even number)
V_p	Vertical character pitch	Vertical character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_X	Number of time divisions	Inverse of dispqay duty ratio	1 to 128 lines

Note: if the number of vertical dots on the screen is m, and the number of horizontal dots is n,

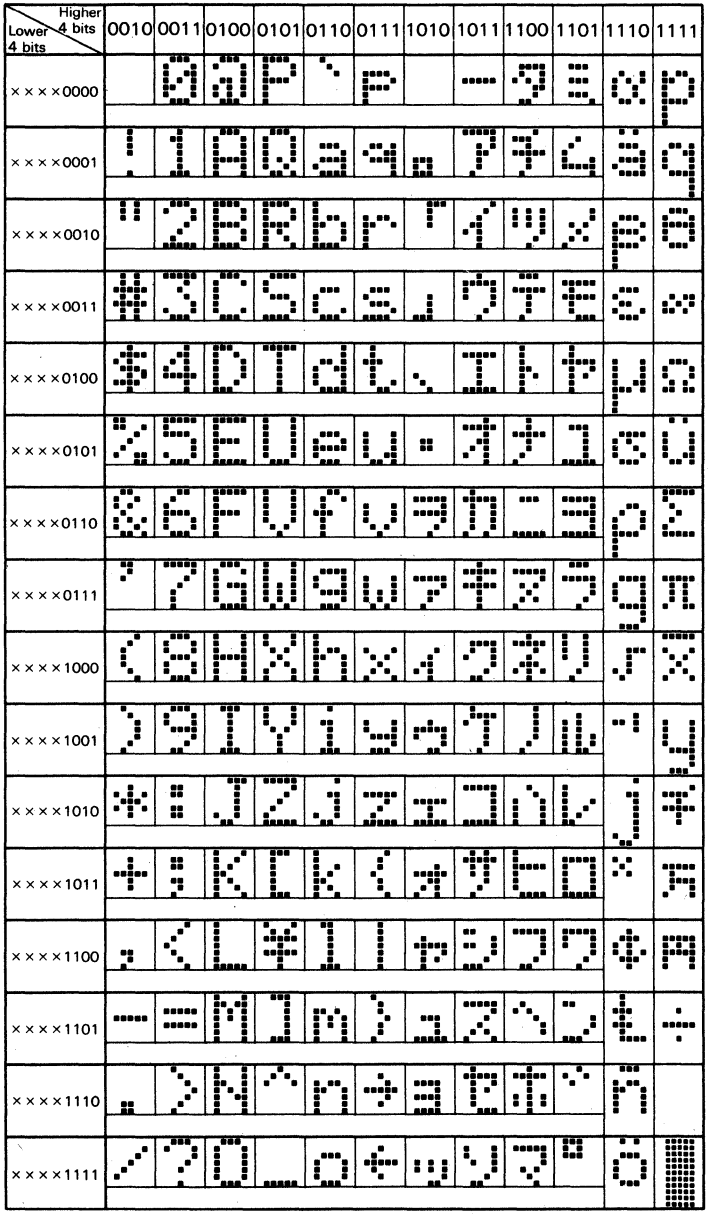
$1/m = 1/N_X$ = display duty ratio
$n = H_p \times H_N$, m/V_p = Number of display lines
$C_p \leqq V_p$

Figure 2 Display Variables

Display Mode

Display Mode	Display Data from MPU	RAM	Liquid Crystal Display Panel
Character display	Character code (8 bits)		
Graphic	Display pattern (8 bits)		

Internal Character Generator Patterns and Character Codes



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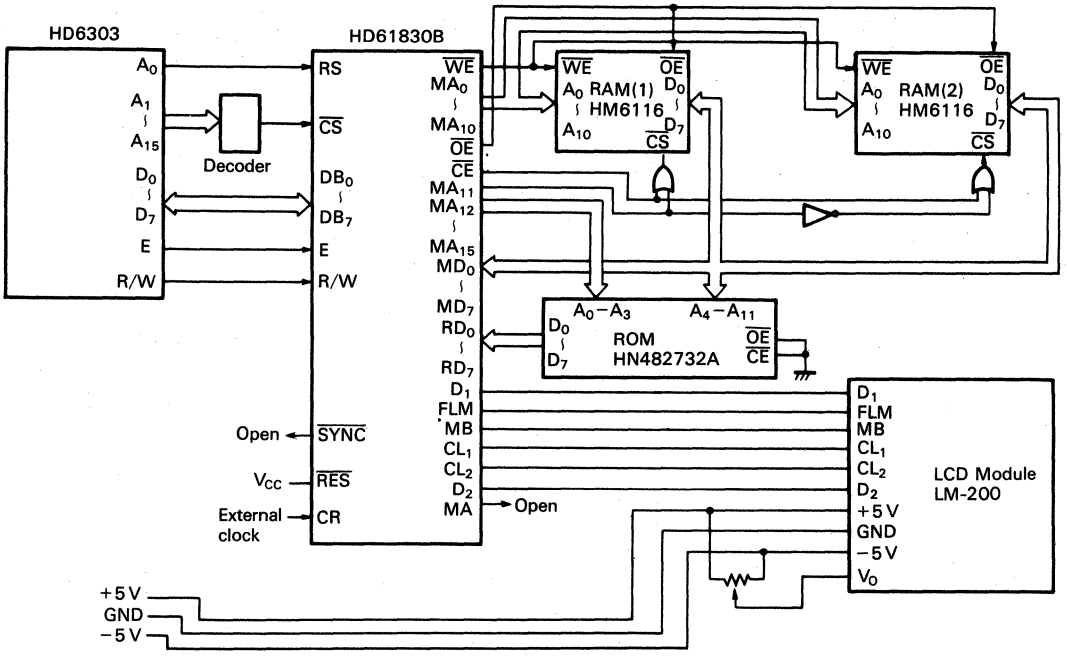
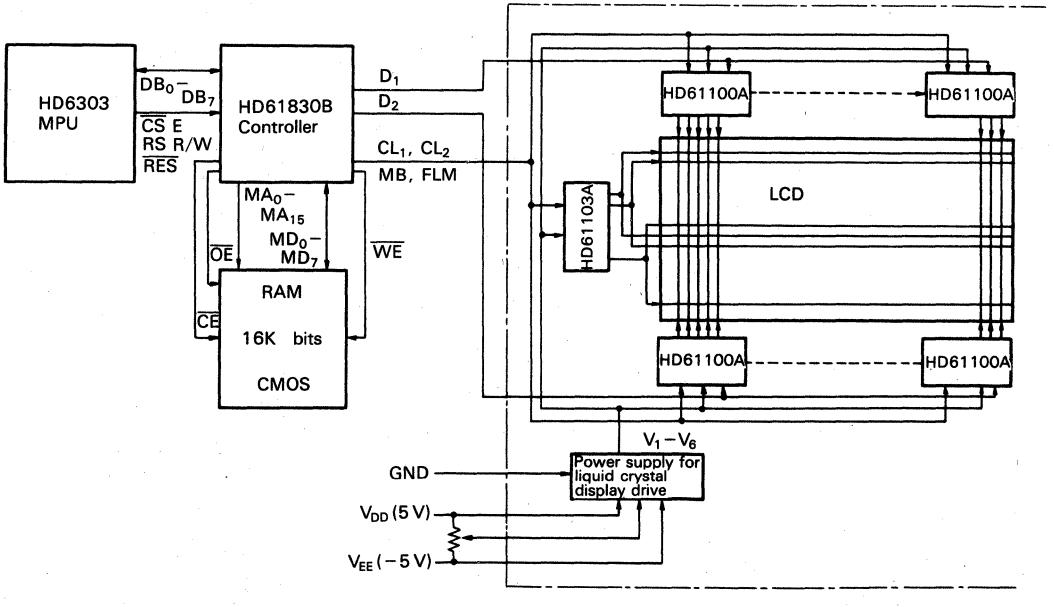
Application (Character Mode, External CG, Character Font 8 × 8)

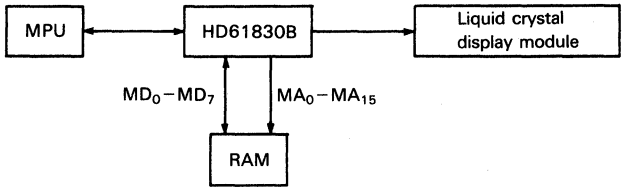


Application (Graphic Mode)

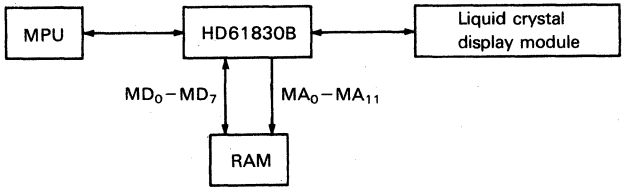


Example of Configuration

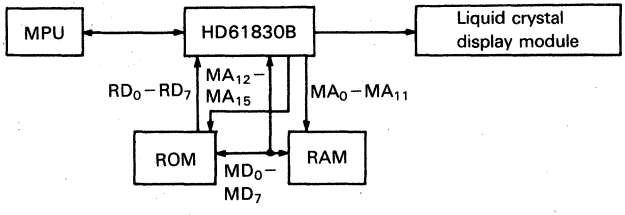
Graphic Mode



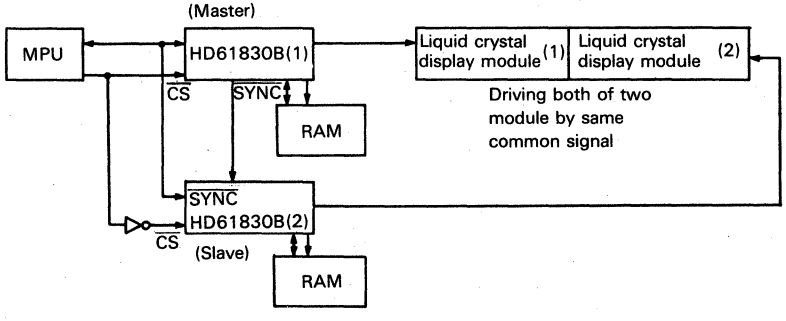
Character Mode (1) (Internal Character Generator)



Character Mode (2) (External Character Generator)



Parallel Operation



5

HD63645F/HD64645F

LCD Timing Controller (LCTC)

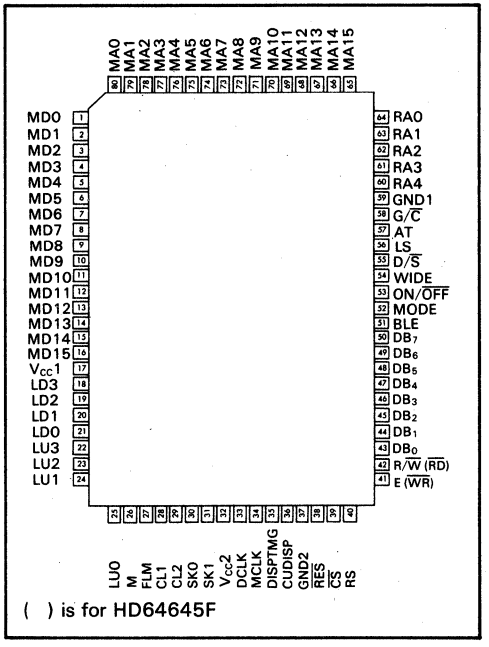
Description

The HD63645F/HD64645F LCTC is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



( ) is for HD64645F

Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/s in character mode
  —Up to 40 Mbits/s in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66204 (column) and HD66205 (common), HD66106, HD66107T (common/column)
- CPU interface: 68 family (HD63645F), 80 family (HD64645F)
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	80-pin Plastic QFP (FP-80)
HD64645	4 MHz	80 System	80-pin Plastic QFP (FP-80)
HD64646	4 MHz	80 System	80-pin Plastic QFP (FP-80B)

Note: See HD64646 data sheet in this data book.

Pin Description

Symbol	Pin Number	Name	I/O
$V_{CC}1$, $V_{CC}2$	17, 32	V_{CC}	—
GND1, GND2	37, 59	Ground	—
LU0-LU3	22-25	LCD Up Panel Data 0-3	O
LD0-LD3	18-21	LCD Down Panel Data 0-3	O
CL1	28	Clock One	O
CL2	29	Clock Two	O
FLM	27	First Line Marker	O
M	26	M	O
MA0-MA15	65-80	Memory Address 0-15	O
RA0-RA4	60-64	Raster Address 0-4	O
MD0-MD7	1-8	Memory Data 0-7	I
MD8-MD15	9-16	Memory Data 8-15	I
DB_0-DB_7	43-50	Data Bus 0-7	I/O
$\overline{CS}$	39	Chip Select	I
E	41	Enable (HD63645 Only)	I
R/$\overline{W}$	42	Read/Write (HD63645 Only)	I
$\overline{WR}$	41	Write (HD64645 Only)	I
$\overline{RD}$	42	Read (HD64645 Only)	I
RS	40	Register Select	I
$\overline{RES}$	38	Reset	I
DCLK	33	D Clock	I
MCLK	34	M Clock	O
DISPTMG	35	Display Timing	O
CUDISP	36	Cursor Display	O
SK0	30	Skew 0	I
SK1	31	Skew 1	I
ON/$\overline{OFF}$	53	On/Off	I
BLE	51	Blink Enable	I
AT	57	Attribute	I
G/$\overline{C}$	58	Graphic/Character	I
WIDE	54	Wide	I
LS	56	Large Screen	I
D/$\overline{S}$	55	Dual/Single	I
MODE	52	Mode	I

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Pin Functions

Power Supply ($V_{cc}1$, $V_{cc}2$, GND)

Power Supply Pin (+5 V): Connect $V_{cc}1$ and $V_{cc}2$ with +5 V power supply circuit.

Ground Pin (0 V): Connect GND1 and GND2 with 0 V.

LCD Interface

LCD Up Panel Data (LU0-LU3), LCD Down Panel Data (LD0-LD3): LU0-LU3 and LD0-LD3 output LCD data as shown in table 1.

Clock One (CL1): CL1 supplies timing clocks for display data latch.

Clock Two (CL2): CL2 supplies timing clock for display data shift.

First Line Marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory Interface

Memory Address (MA0-MA15): MA0-MA15 supply the display memory address.

Raster Address (RA0-RA4): RA0-RA4 supply the raster address.

Memory Data (MD0-MD7): MD0-MD7 receive the character dot data and bit-mapped data.

Memory Data (MD8-MD15): MD8-MD15 receive attribute code data and bit-mapped data.

MPU Interface

Data Bus (DB0-DB7): DB0-DB7 send/receive data as a three-state I/O common bus.

Chip Select ($\overline{CS}$): $\overline{CS}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Enable (E): E receives an enable clock. (HD63645F only).

Read/Write (R/$\overline{W}$): R/$\overline{W}$ enables MPU read of the LCTC internal registers when R/$\overline{W}$ is high, and MPU write when low (HD63634F only).

Write ($\overline{WR}$): $\overline{WR}$ receives MPU write signal (HD64645F only).

Read ($\overline{RD}$): $\overline{RD}$ receives MPU read signal (HD64645F only).

Register Select (RS): RS selects registers. (Refer to table 5.)

Reset ($\overline{RES}$): $\overline{RES}$ performs external reset of the LCTC. Low level of $\overline{RES}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing Signal

D Clock (DCLK): DCLK inputs the system clock.

M Clock (MCLK): MCLK indicates memory cycle; DCLK is divided by four.

Display Timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Cursor Display (CUDISP): CUDISP supplies cursor display timing; connect with MD12 in character mode.

Skew 0 (SK0)/Skew 1 (SK1): SK0 and SK1 control skew timing. Refer to table 2.

Mode Select

The mode select pins ON/$\overline{OFF}$, BLE, AT, G/$\overline{C}$,

Table 1 LCD Up Panel Data and LCD Down Panel Data

	Single Screen		
Pin name	**4-Bit Data**	**8-Bit Data**	**Dual Screen**
LU0-LU3	Data output	Data output	Data output for upper screen
LD0-LD3	Disconnected	Data output	Data output for lower screen

and WIDE are ORed with the mode register (R22) to determine the mode.

On/Off (ON/$\overline{\text{OFF}}$): ON/$\overline{\text{OFF}}$ switches display on and off (High = display on).

Blink Enable (BLE): BLE high level enables attribute code "blinking" (MD13) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/Character (G/$\overline{\text{C}}$): G/$\overline{\text{C}}$ switches between graphic and character display mode (graphic display when high).

Wide (WIDE): WIDE switches between normal and wide display mode (high = wide display, low = normal display).

Large Screen (LS): LS controls a large screen. LS high provides a data transfer rate of 40 Mbits/s for a graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to table 10.

Dual/Single (D/$\overline{\text{S}}$): D/$\overline{\text{S}}$ switches between single and dual screen display (dual screen display when high).

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. (Refer to table 9.)

Table 2 Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character time skew
0	1	2-character time skew
1	1	Prohibited combination

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Function Overview

LCD and CRT Display Systems

Figure 1 shows a system using both LCD and CRT displays.

Main Features of HD63645F/HD64645F

Main features of the LCTC are:

- High-resolution liquid crystal display screen control (up to 720 × 512 dots)
- Software compatible with HD6845 (CRTC)
- Built-in character attribute control circuit

Table 3 shows how the LCTC can be used.

Table 3 Functions, Application, and Configuration

Classification	Item	Description
Functions	Screen Format	● Programmable horizontal scanning cycle by the character clock period ● Programmable multiplexing duty ratio from static up to 1/512 ● Programmable number of vertical displayed characters per character row ● Programmable number of rasters per character row (number of vertical dots within a character row + space between character rows)
	Cursor Control	● Programmable cursor display position, corresponding to RAM address ● Programmable cursor height by setting display start/end rasters ● Programmable blink rate, 1/32 or 1/64 frame rate
	Memory Rewriting	● Time for rewriting memory set either by specifying number of horizontal total characters or by cycle steal utilizing MCLK
	Memory Addressing	● 16-bit memory address output, up to 64 kbytes x 2 memory accessible ● DRAM refresh address output
	Paging and Scrolling	● Paging by updating start address ● Horizontal scrolling by the character, by setting horizontal virtual screen width ● Vertical smooth scrolling by updating display start raster
	Character Attributes	● Reverse video, blinking, nondisplay (white or black), display ON/OFF
Application	CRTC Compatible	● Facilitates system replacement of CRT display with LCD
	OR Function	● Enables superimposing display of character screen and graphic screen
Configuration	LCTC Configuration	● Single 5 V power supply ● I/O TTL compatible except $\overline{RES}$, MODE, SKO, SK1 ● Bus connectable with HMCS 6800 family (HD63645) ● Bus connectable with 80 family (HD64645) ● CMOS process ● Internal logic fully static ● 80-pin flat plastic package

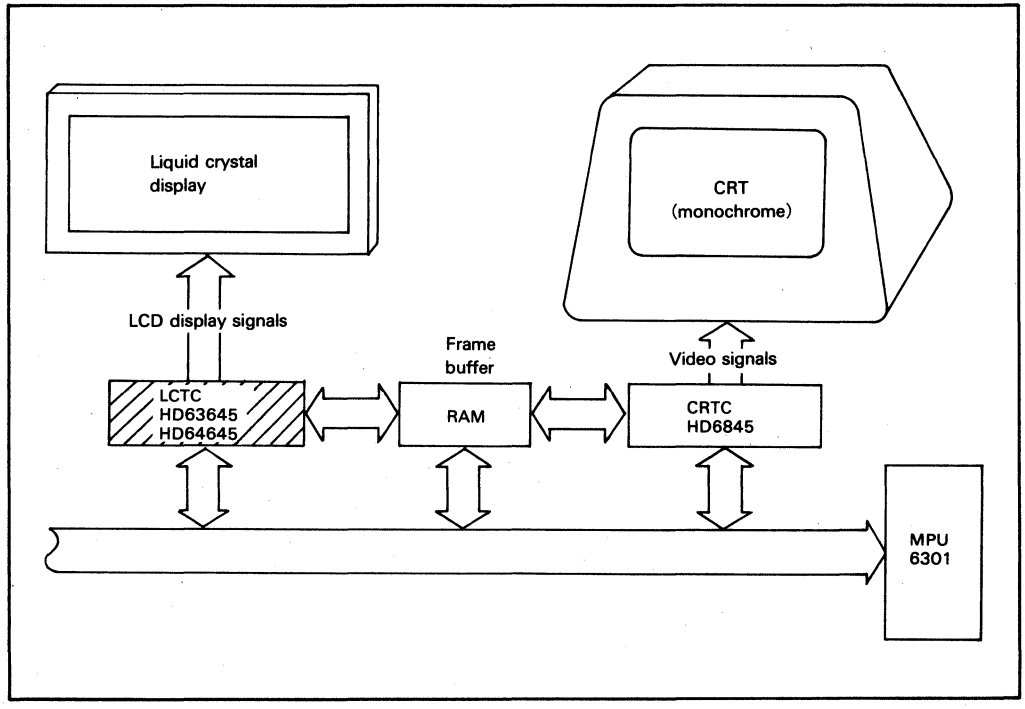


Figure 1 LCD and CRT Displays

5

Internal Block Diagram

Figure 2 is a block diagram of the LCTC.

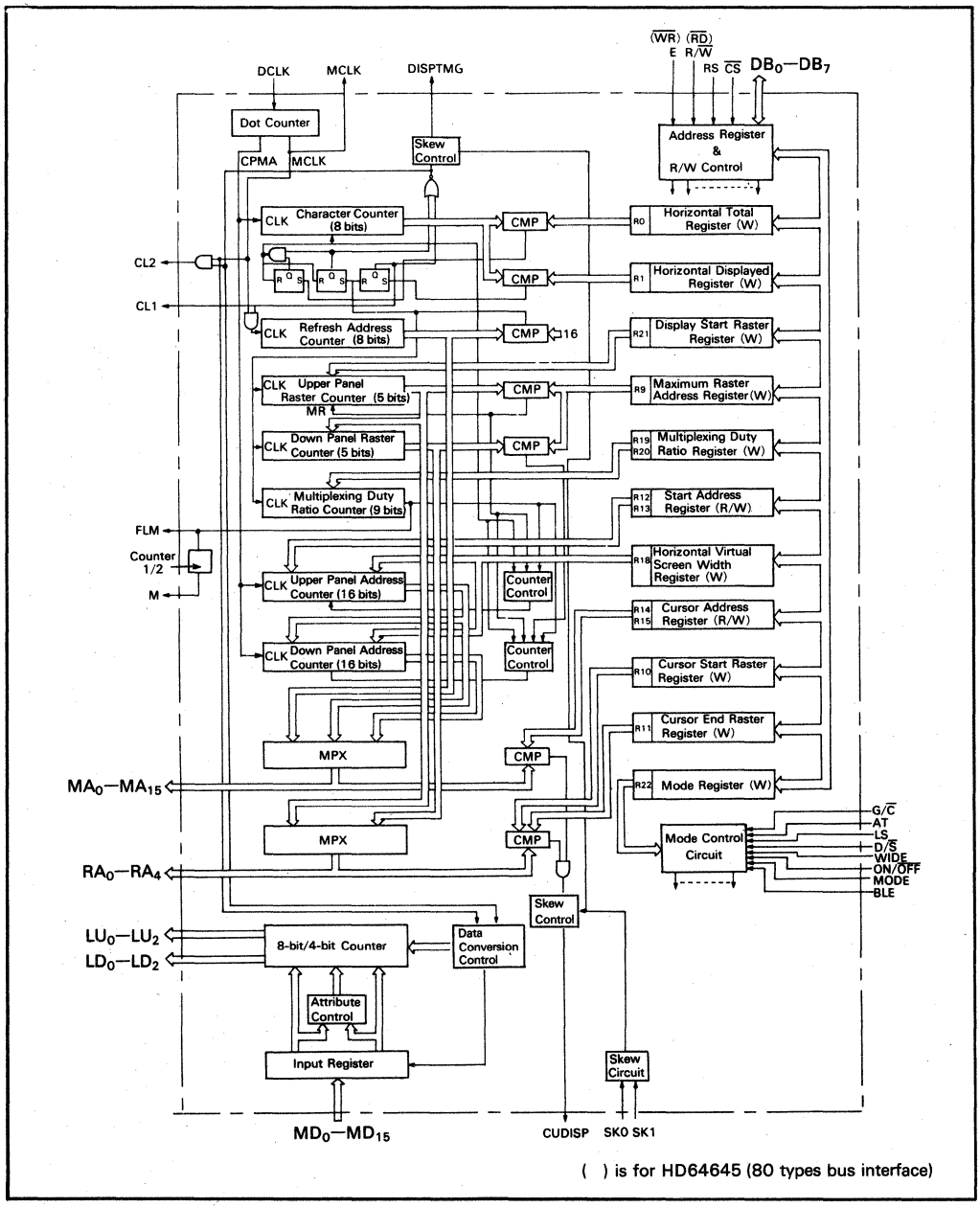


Figure 2 LCTC Block Diagram

System Block Configuration Examples

Figure 3 is a block diagram of a character/ graphic display system. Figure 5 shows two examples using LCD drivers.

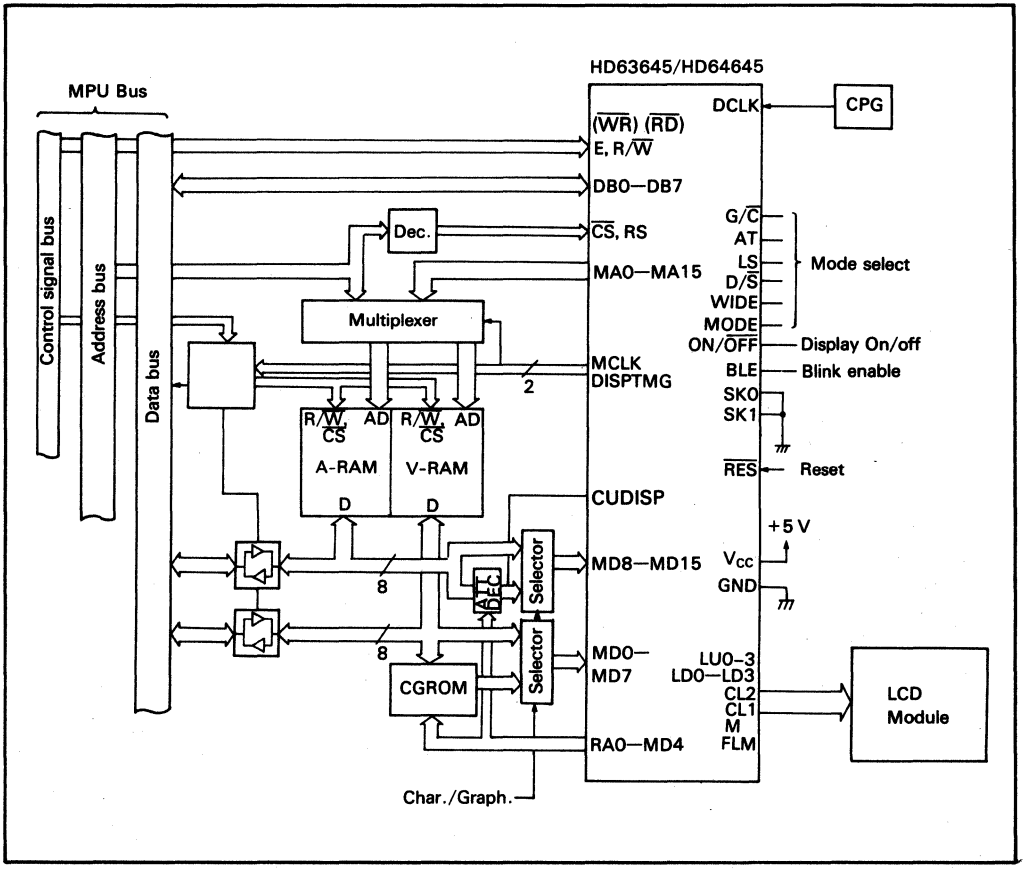
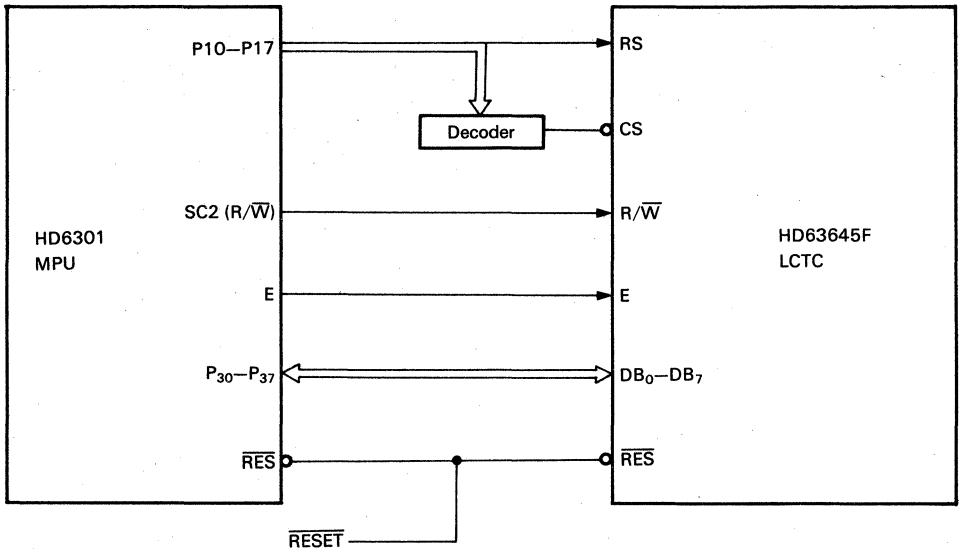


Figure 3 Character/Graphic Display System Example

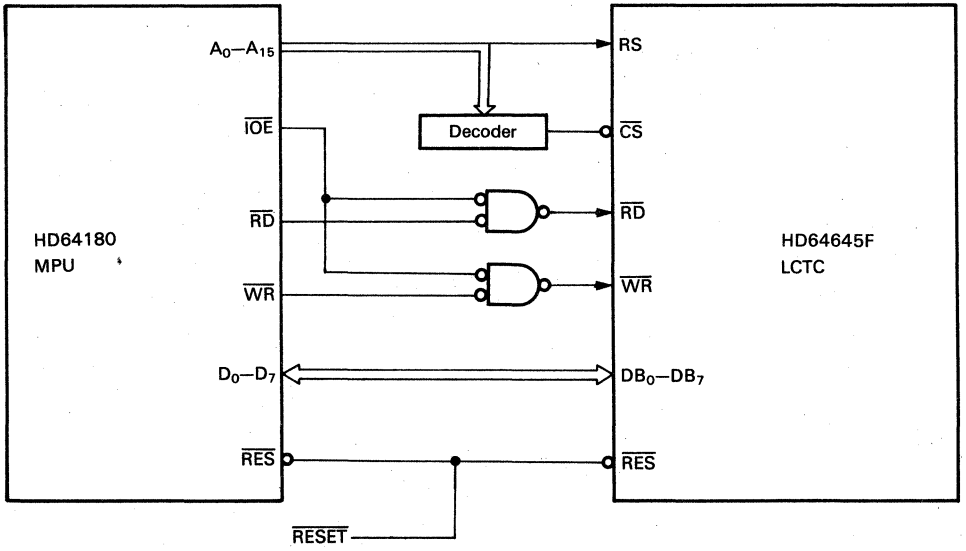
5

Interface to MPU



Note: HD6301 is set in mode 5. P10—P17 are used as output ports, and P30—P37 as data buses. SC2 outputs R/W here.

Interface between HD6301 and HD63645F



Note: In 80 family MPUs, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ORed signals of the interface signals and IOE. So IOE and RD, and IOE and WR should be ORed to satisfy t_{AS}, the timing of CS, RD, and WR.

Interface between HD64180 and HD64645F

Figure 4 Interface to MPU

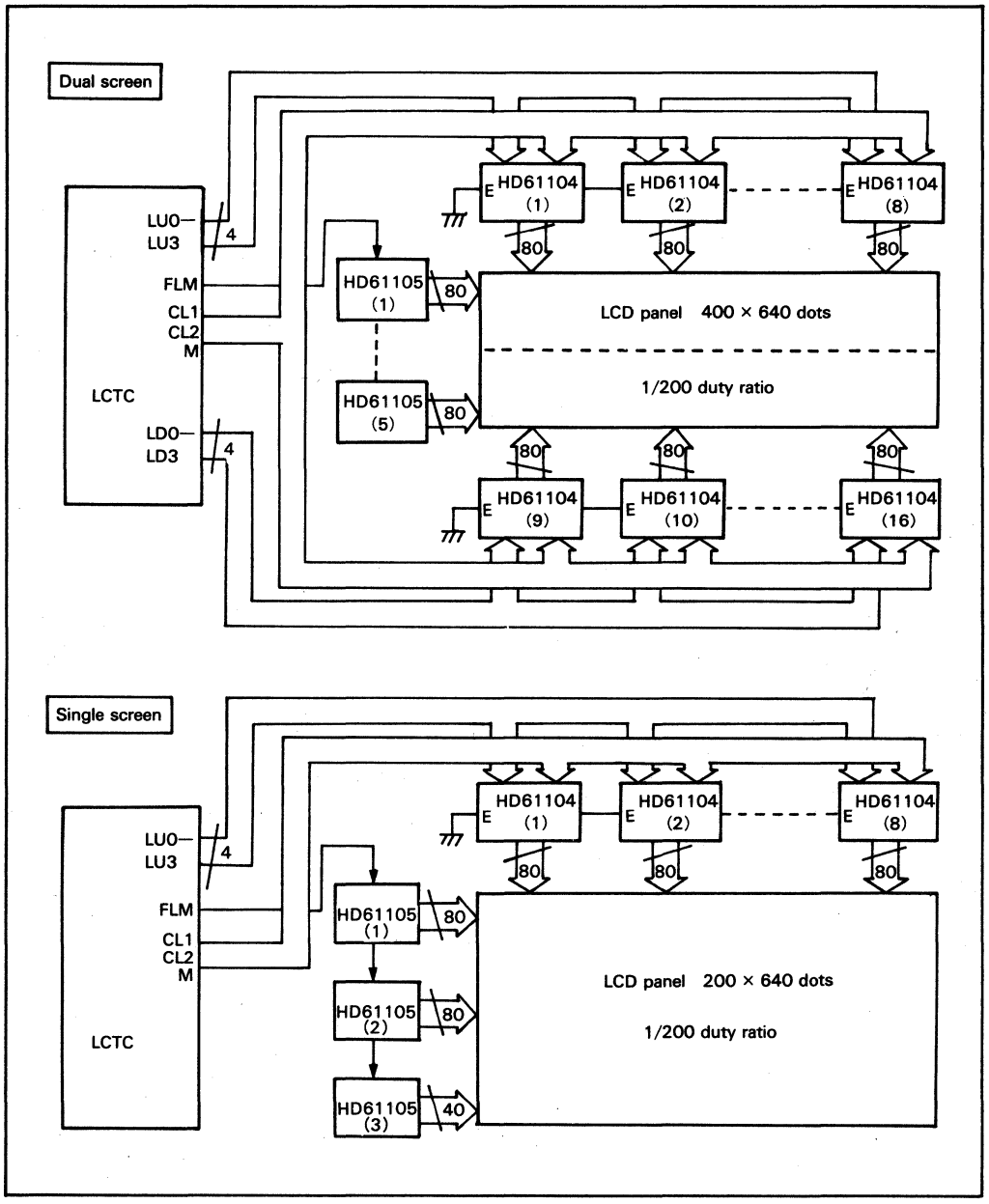


Figure 5 LCD Driver Examples

5

Registers

Table 4 shows the register mapping. Table 5 describes their function. Table 6 shows the differences between CRTC and LCTC registers.

Table 4 Registers Mapping

$\overline{CS}$	RS	Address Register 43210	Reg. no.	Register Name	Program Unit	Symbol	R/W	Data Bit 7	6	5	4	3	2	1	0
1	–	———		Invalid	—	—	—								
0	0	———	AR	Address Register	—	—	W								
0	1	00000	R0	Horizontal Total Characters	Character[3]	Nht	W								
0	1	00001	R1	Horizontal Displayed Char.s	Character	Nhd	W								
0	1	01001	R9	Maximum Raster Address	Raster	Nr	W								
0	1	01010	R10	Cursor Start Raster	Raster[4]	Ncs	W		B	P					
0	1	01011	R11	Cursor End Raster	Raster	Nce	W								
0	1	01100	R12	Start Address (H)	Memory Address	—	R/W								
0	1	01101	R13	Start Address (L)	Memory Address	—	R/W								
0	1	01110	R14	Cursor Address (H)	Memory Address	—	R/W								
0	1	01111	R15	Cursor Address (L)	Memory Address	—	R/W								
0	1	10010	R18	Horizontal Virtual Screen Width	Character	Nir	W								
0	1	10011	R19	Multiplexing Duty Ratio (H)	Raster[3]	Ndh	W								
0	1	10100	R20	Multiplexing Duty Ratio (L)	Raster[3]	Ndl	W								
0	1	10101	R21	Display Start Raster	Raster	Nsr	W								
0	1	10110	R22	Mode Register	—Note[5]	—	W				ON/OFF	G/C	WIDE	BLE	AT

Notes: 1. ▨: Invalid data bits
2. R/W indicates whether write access or read access is enabled to/from each register.
   W: Only write accessible
   R/W: Both read and write accessible
3. The "value to be specified minus 1" should be programmed in these registers: R0, R1 and R20.
4. Data bits 5 and 6 of cursor start register control the cursor status as shown below. (For more details, refer to page 27).

B	P	Cursor Blink Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

5. The OR of mode pin status and mode register data determines the mode.
6. Registers R2-R8, R16, and R17 are not assigned for the LCTC. Programming to these registers will be ignored.

Table 5 Internal Register Description

Reg. No.	Register Name	Size (Bits)	Description
AR	Address Register	5	Specifies the internal control registers (R0, R1, R9-R15, R18-R22) address to be accessed
R0	Horizontal Total Characters	8	Specifies the horizontal scanning period
R1	Horizontal Displayed Characters	8	Specifies the number of displayed characters per character row
R9	Maximum Raster Address	5	Specifies the number of rasters per character row, including the space between character rows
R10	Cursor Start Raster	5 + 2	Specifies the cursor start raster address and its blink mode
R11	Cursor End Raster	5	Specifies the cursor end raster address
R12 R13	Start Address (H) Start Address (L)	16	Specify the display start address
R14 R15	Cursor Address (H) Cursor Address (L)	16	Specify the cursor display address
R18	Horizontal Virtual Screen Width	8	Specifies the length of one row in memory space for horizontal scrolling
R19 R20	Multiplexing Duty Ratio (H) Multiplexing Duty Ratio (L)	9	Specify the number of rasters for one screen
R21	Display Start Raster	5	Specifies the display start raster within a character row for smooth scrolling
R22	Mode Register	5	Controls the display mode

Note: For more details of registers, refer to "Internal Registers".

Table 6 Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC HD63645/HD64645	Comparison	CRTC HD6845
AR	Address Register	Equivalent to CRTC	Address Register
R0	Horizontal Total Characters		Horizontal Total Characters
R1	Horizontal Displayed Characters		Horizontal Displayed Characters
R2	—	Particular to CRTC ;	Horizontal Sync Position
R3		unnecessary for LCTC	Sync Width
R4			Vertical Total Characters
R5			Vertical Total Adjust
R6			Vertical Displayed Characters
R7			Vertical Sync Position
R8			Interlace and Skew
R9	Maximum Raster Address	Equivalent to CRTC	Maximum Raster Address
R10	Cursor Start Raster		Cursor Start Raster
R11	Cursor End Raster		Cursor End Raster
R12	Start Address (H)		Start Address (H)
R13	Start Address (L)		Start Address (L)
R14	Cursor Address (H)		Cursor (H)
R15	Cursor Address (L)		Cursor (L)
R16		Particular to CRTC ;	Light Pen (H)
R17		unnecessary for LCTC	Light Pen (L)
R18	Horizontal Virtual Screen Width	Additional registers for LCTC	
R19	Multiplexing Duty Ratio (H)		
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster		
R22	Mode Register		

Functional Description

Programmable Screen Format

Figure 6 illustrates the relation between LCD display screen and registers. Figure 7 shows a timing chart of signals output from the LCTC in mode 5 as an example.

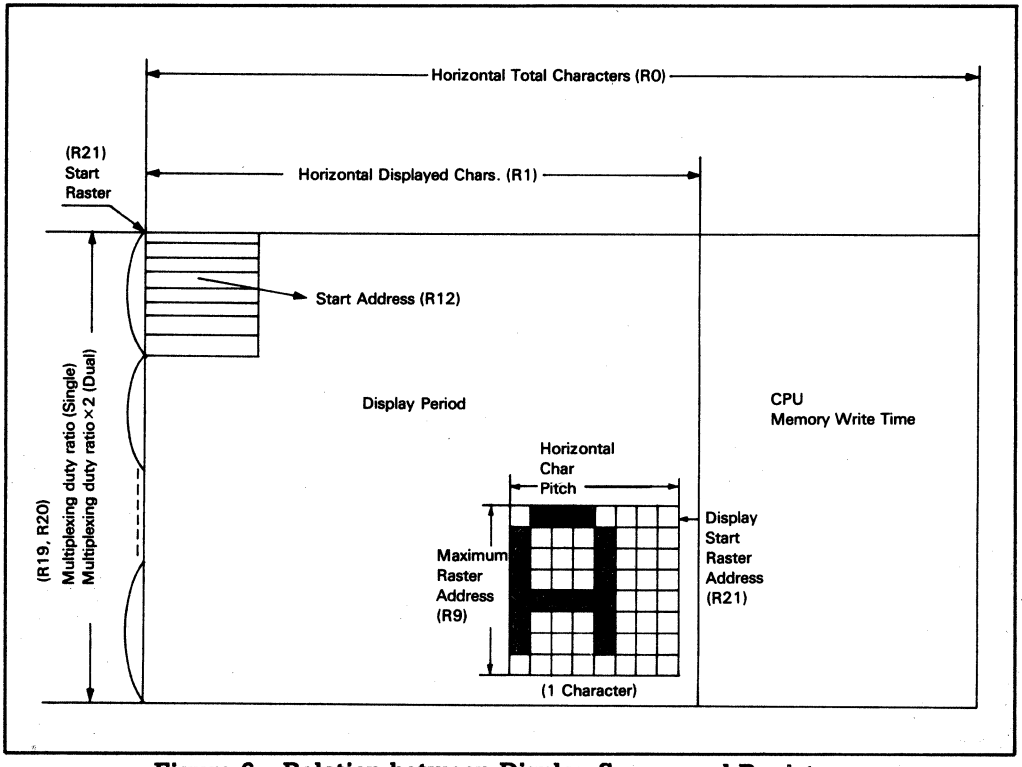


Figure 6 Relation between Display Screen and Registers

5

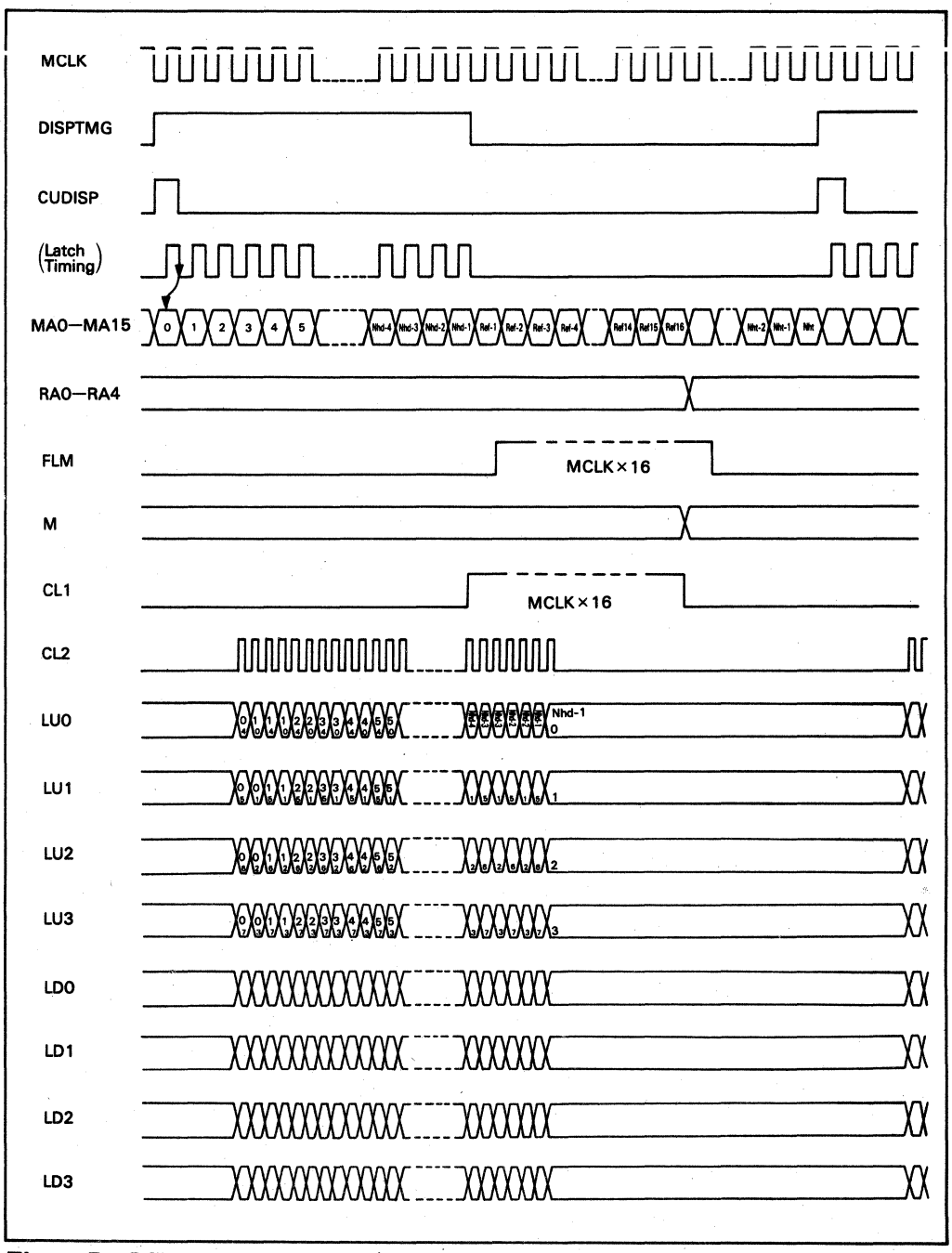


Figure 7 LCTC Timing Chart (In Mode 5: Single Screen, 4-Bit Transfer, Normal Character Display)

Cursor Control

The following cursor functions (figure 8) can be controlled by programming specific registers.

Cursor display position
- Cursor height
- Cursor blink mode

A cursor can be displayed only in character mode. Also, CUDISP pin must be connected to MD12 pin to display a cursor.

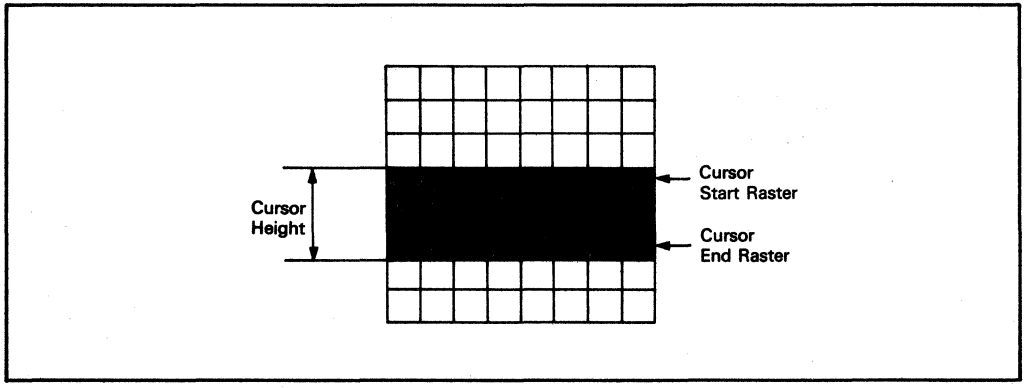


Figure 8 Cursor Display

5

Character Mode and Graphic Mode

The LCTC supports two types of display modes; character mode and graphic mode. Graphic mode 2 is provided to utilize software for a system using the CRTC (HD6845).

The display mode is controlled by an OR between the mode select pins (D/$\overline{S}$, G/$\overline{C}$, LS, WIDE, AT) and mode register (R22).

Character Mode: Character mode displays characters by using CG-ROM. The display data supplied from memory is accessed in 8-bit units. A variety of character attribute functions are provided, such as reverse video, blinking, nondisplay (white or black),by storing the attribute data in attribute RAM (A-RAM).

Figure 9 illustrates the relation between character display screen and memory contents.

Graphic Mode 1: Graphic mode 1 directly displays data stored in a graphic memory buffer. The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. Figure 10 illustrates the relation between graphic display screen and memory contents.

Graphic Mode 2: Graphic mode 2 utilizes software for a system using the CRTC (HD6845). The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. The same memory addresses are output repeatedly the number of times specified by maximum raster register (R9). The raster address is output in the same way as in character mode.

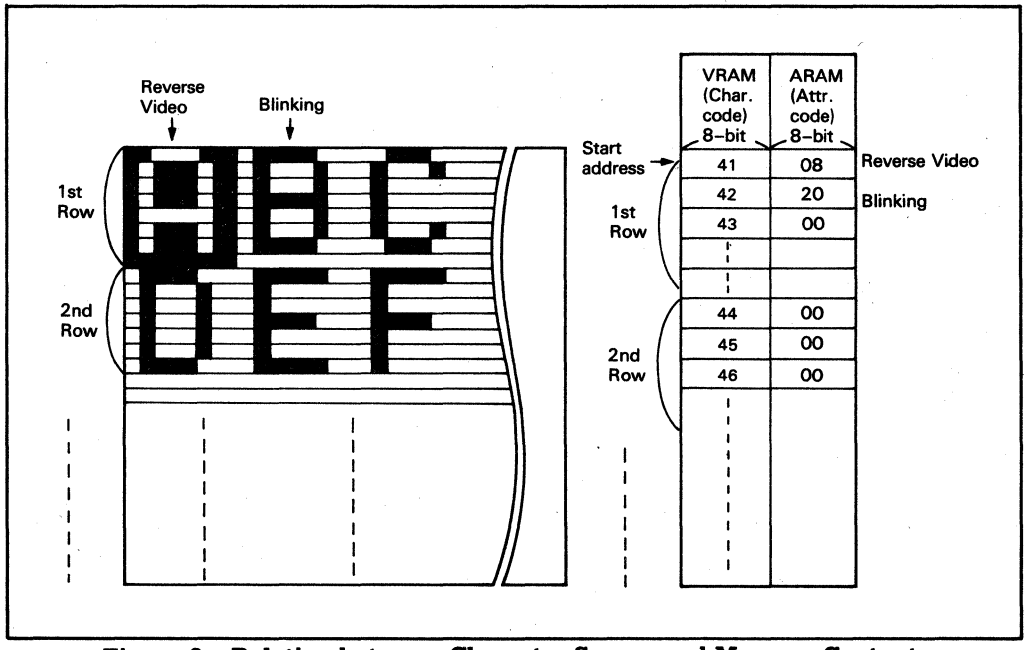


Figure 9 Relation between Character Screen and Memory Contents

Horizontal Virtual Screen Width

Horizontal virtual screen width can be specified by the character in addition to the number of horizontal displayed characters (figure 11).

The display screen can be scrolled in any direction by the character, by setting the horizontal virtual screen width and updating the start address. This function is enabled by programming the horizontal virtual screen width register (R18).

Figure 12 shows an example.

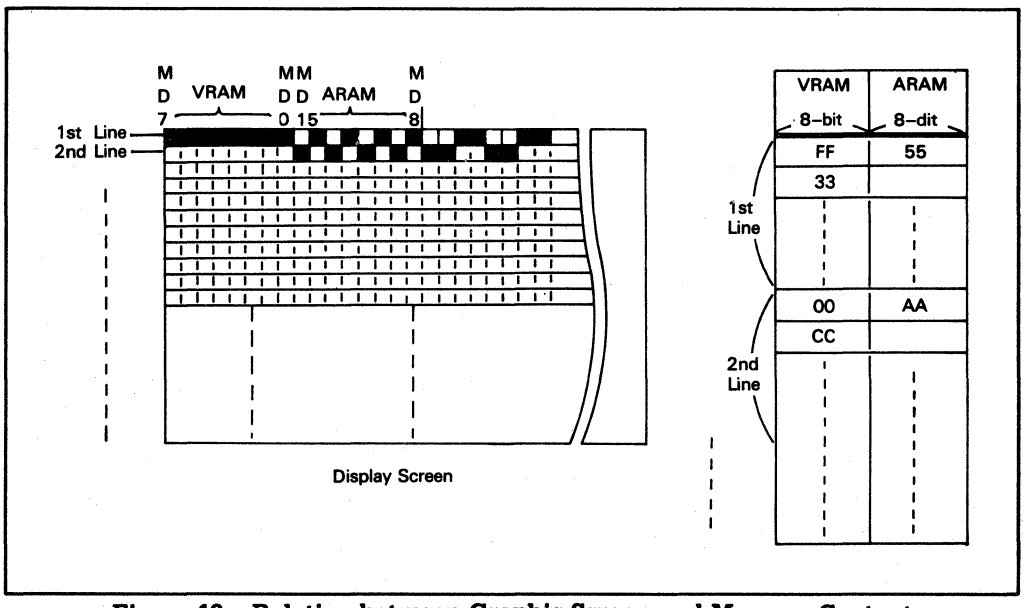


Figure 10 Relation between Graphic Screen and Memory Contents

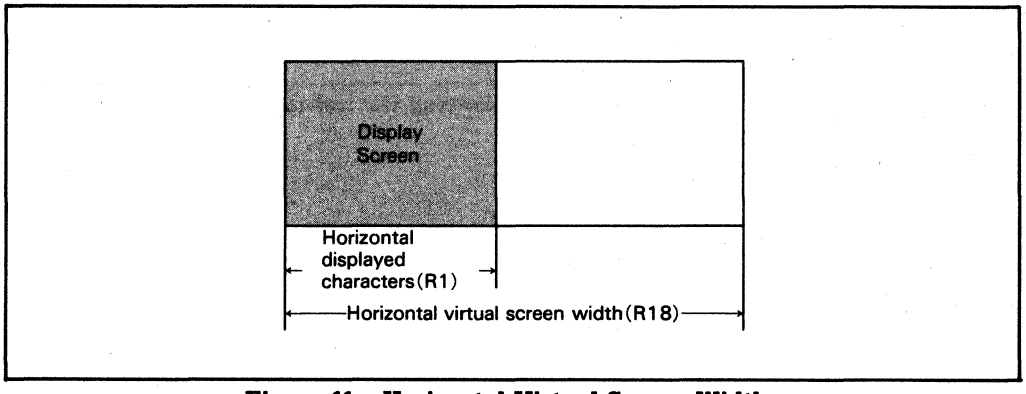


Figure 11 Horizontal Virtual Screen Width

5

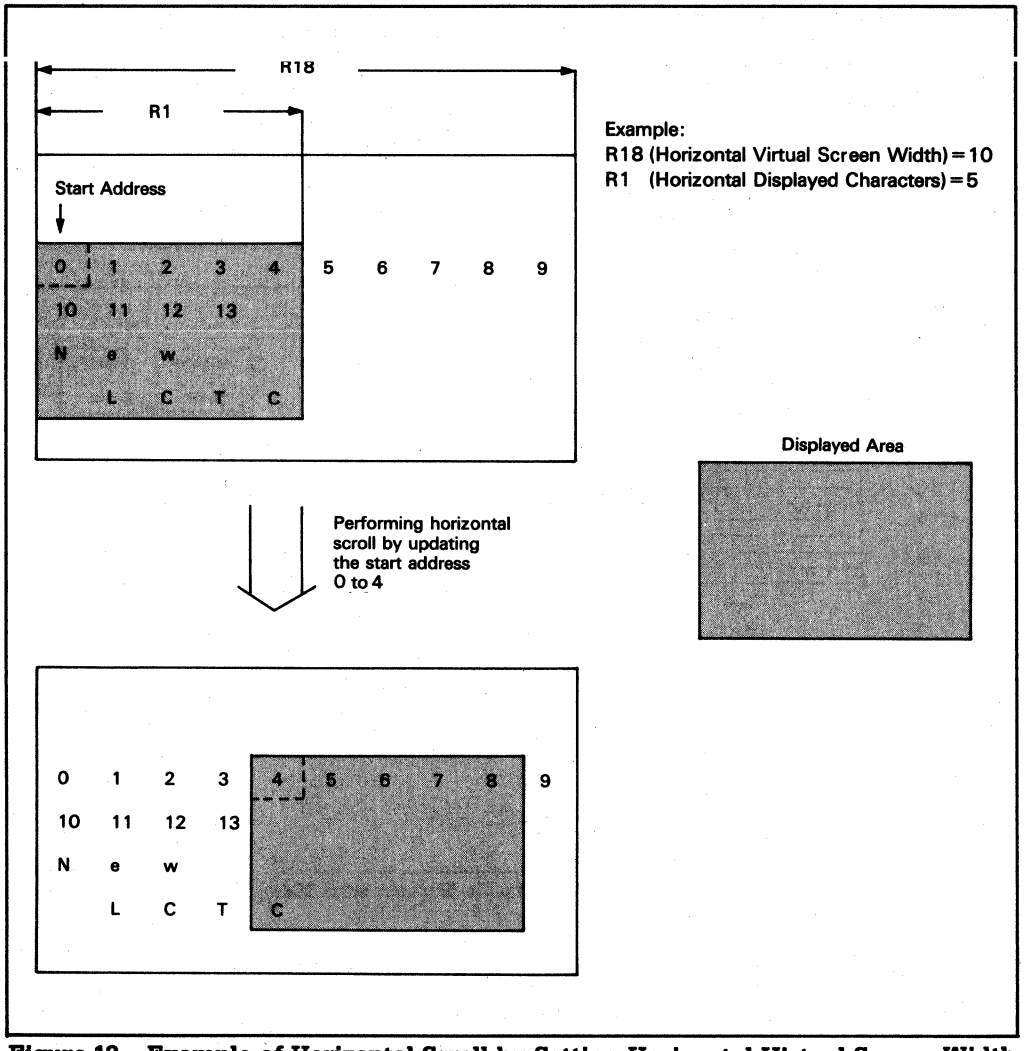


Figure 12 Example of Horizontal Scroll by Setting Horizontal Virtual Screen Width

Smooth Scroll

Vertical smooth scrolling (figure 13) is performed by updating the display start raster, as specified by the start raster register (R21). This function is offered only in character mode.

Wide Display

The character to be displayed can be doubled in width, by supplying the same data twice (figure 14). This function is offered only in character mode, and controlled either by bit 2 of the mode register (R22) or by the WIDE pin.

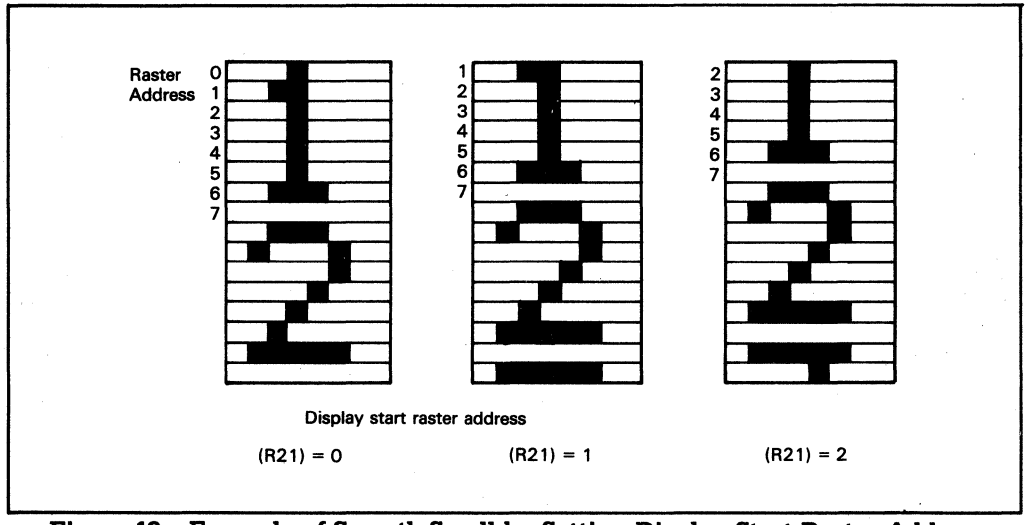


Figure 13 Example of Smooth Scroll by Setting Display Start Raster Address

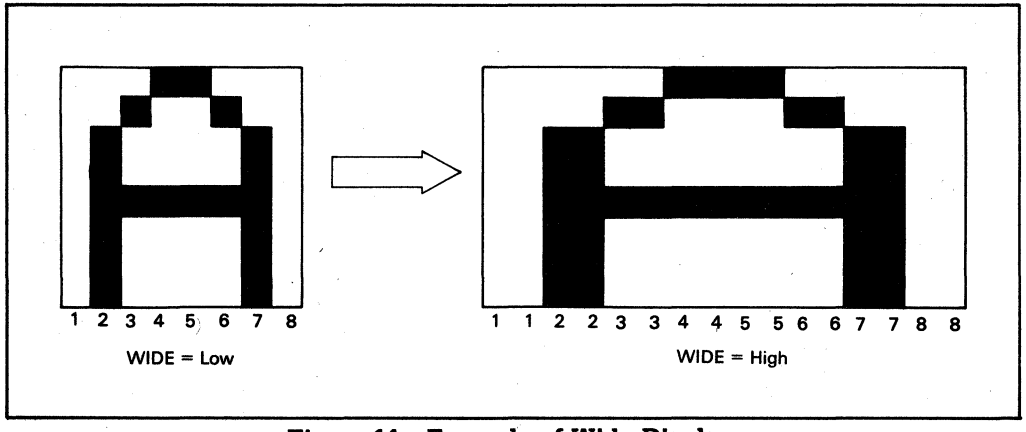


Figure 14 Example of Wide Display

5

Attribute Functions

A variety of character attribute functions such as reverse video, blinking, nondisplay (white) or nondisplay (black) can be implemented by storing the attribute data in A-RAM (attribute RAM). Figure 15 shows a display example using each attribute function.

The attribute functions are offered only in character mode, and controlled either by bit 0 of the mode register (RZZ) or the AT pin. As shown in figure 15, a character attribute can be specified by placing the character code on MD0-MD7, and the attribute code on MD11-MD15. MD8-MD10 are invalid.

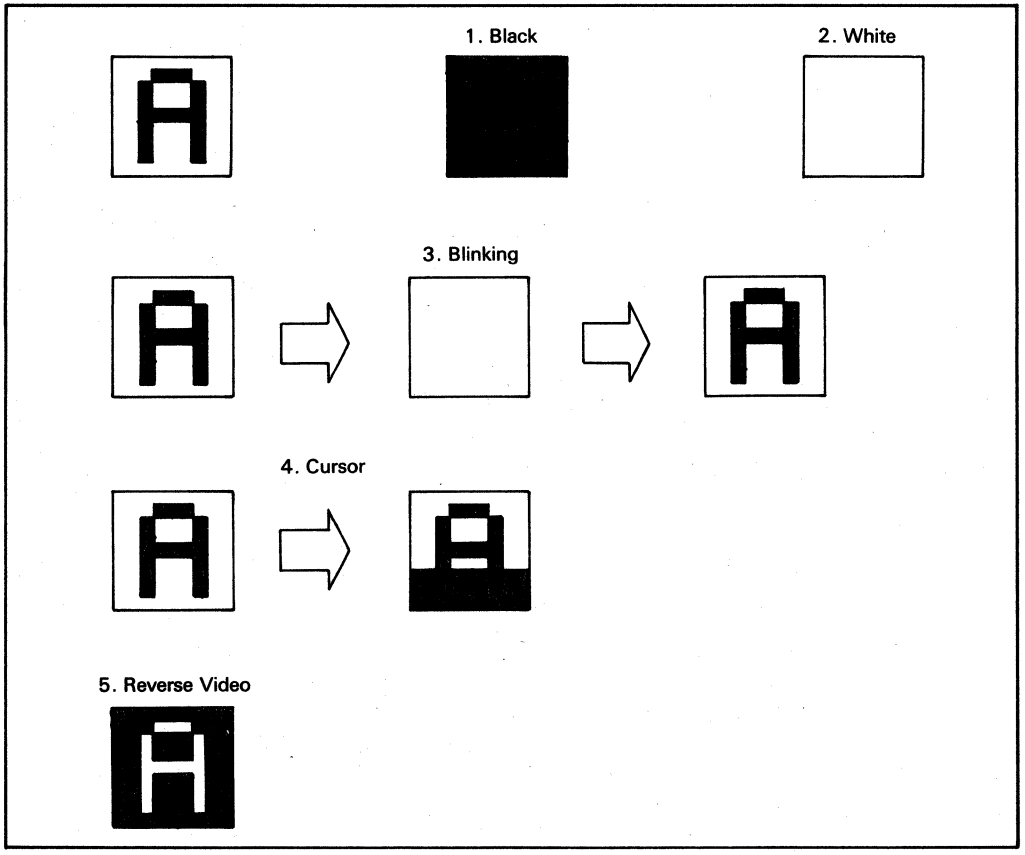


Figure 15 Display Example Using Attribute Functions

MD Input	15	14	13	12	11	10-8	7-0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	* * *	Character Code

*: Invalid

Figure 16 Attribute Code

OR Function —Superimposing Characters and Graphics

The OR function (figure 17) generates the OR of the data entered into MD0-MD7 (e.g. character data) and the data into MD8-MD15 (e.g. graphic data) in the LCTC and transfers this data as 1 byte.

This function is offered only in character mode, and controlled by bit 0 of the mode register (R22) or by the AT pin. Any attribute functions are disabled when using the OR function.

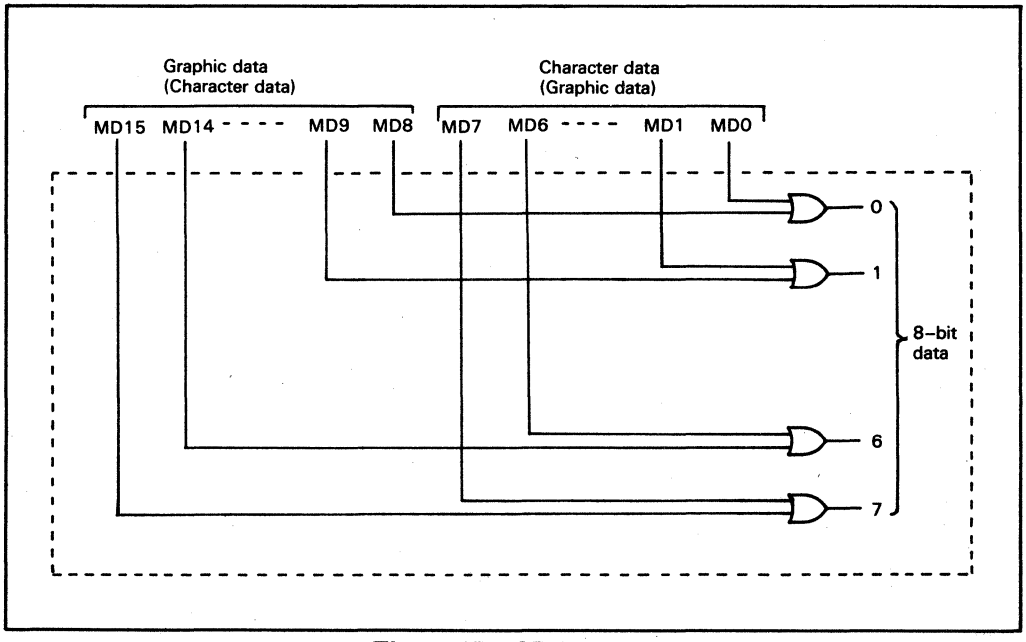


Figure 17 OR Function

5

DRAM Refresh Address Output Function

The LCTC outputs the address for DRAM refresh while CL1 is high, as shown in figure 18. The 16 refresh addresses per scanned line are output 16 times, from $00-$FF.

Skew Function

The LCTC can specify the skew (delay) for CUDISP, DISPTMG, CL2 outputs and MD inputs.

If buffer memory and character generator ROM cannot be accessed within one horizontal character display period, the access is retarded to the next cycle by inserting a latch to memory address output and buffer memory output. The skew function retards the CUDISP, DISPTMG, CL2 outputs, and MD inputs in the LCTC to match phase with the display data signal.

By utilizing this function, a low-speed memory can be used as a buffer RAM or a character generator ROM.

This function is controlled by pins SK0 and SK1 as shown in table 7.

Table 7 Skew Function

SK0	SK1	Skew Function
0	0	No skew
1	0	1 character time skew
0	1	2 character time skew
1	1	Inhibited combination

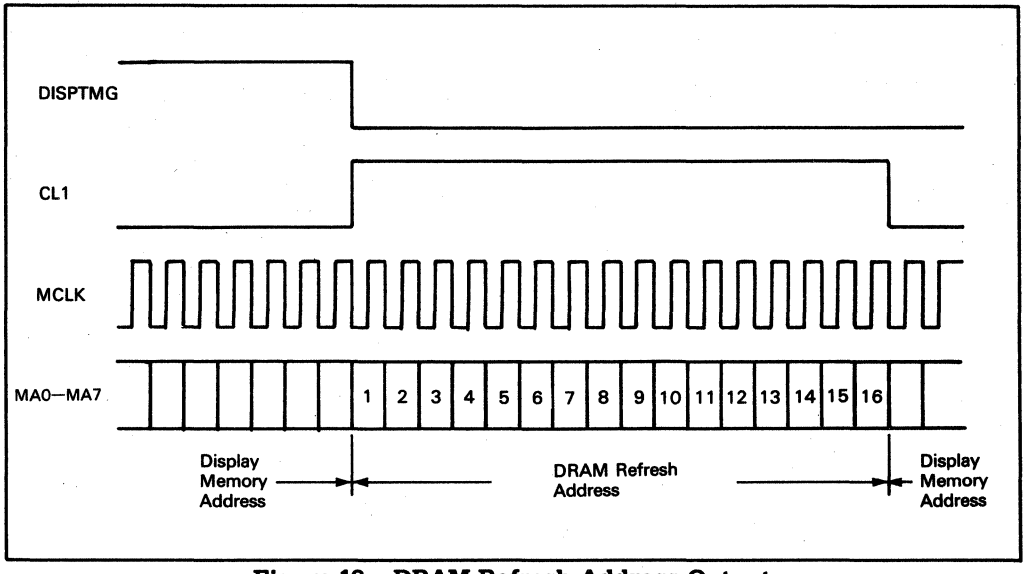


Figure 18 DRAM Refresh Address Output

Easy Mode

This mode utilizes software for systems using the CRTC (HD6845). By setting MODE pin to high, the display mode and screen format are fixed as shown in table 8. With this mode, software for a CRT screen can be utilized in a system using the LCTC, without changing the BIOS.

Automatic Correction of Down Panel Raster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of a display spread over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See figure 19.)

Table 8 Fixed Values in Easy Mode

Reg. No.	Register Name	Fixed Value (decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0

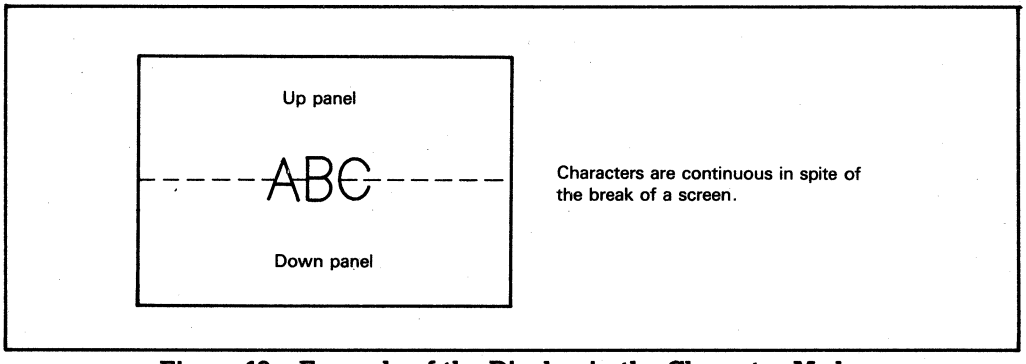


Figure 19 Example of the Display in the Character Mode

5

System Configuration and Mode Setting

LCD System Configuration

The screen configuration, single or dual, must be specified when using the LCD system (figure 20).

Using the single screen configuration, you can construct an LCD system with lower cost than a dual screen system, since the required number of column drivers is smaller and the manufacturing process for mounting them is simpler. However, there are some limitations, such as duty ratio, breakdown voltage of a driver, and display quality of the liquid crystal, in single screen configuration. Thus, a dual screen configuration may be more suitable to an application.

The LCTC also offers an 8-bit LCD data transfer function to support an LCD screen with a smaller interval of signal input terminals. For a general size LCD screen, such as 640 × 200 single, or 640 × 400 dual, the usual 4-bit LCD data transfer is satisfactory.

Hardware Configuration and Mode Setting

The LCTC supports the following hardware configurations:

- Single or dual screen configuration
- 4-or 8-bit LCD data transfer

and the following screen format:

- Character, graphic 1, or graphic 2 display
- Normal or wide display (only in character mode)
- OR or attribute display (only in character mode)

Also, the LCTC supports up to 40 Mbits/s of large screeen mode (mode 13) for large screen display. This mode is provided only in graphic 1 mode.

Table 9 shows the mode selection method according to hardware configuration and screen format. Table 10 shows how they are specified.

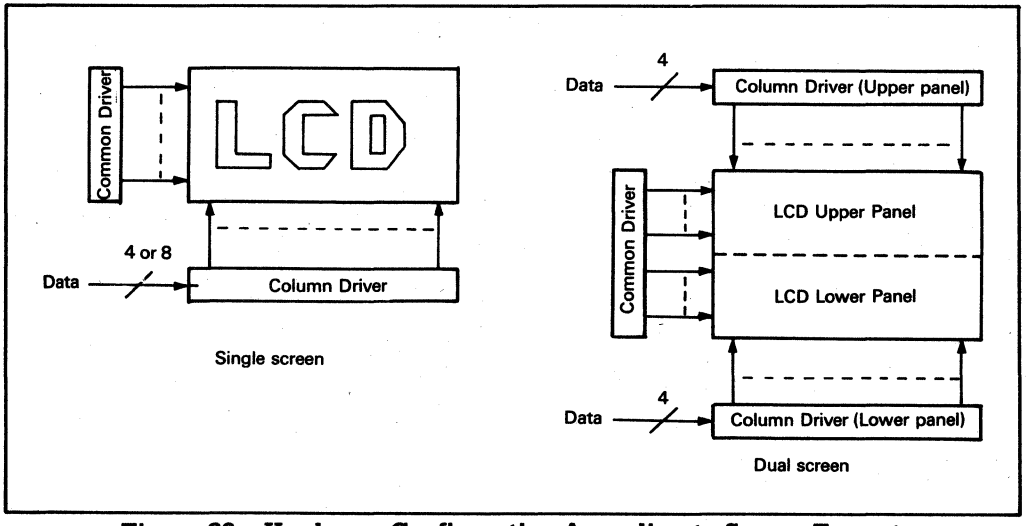


Figure 20 Hardware Configuration According to Screen Format

Table 9 Mode Selection

Hardware Configuration			Screen Format				
LCD Data Transfer	**Screen Configu-ration**	**Screen Size**	**Character/ Graphic**	**Normal/ Wide**	**Attribute/ OR**	**Maximum data transfer speed (Mbps)**	**Mode No.**
4-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	5
				Wide	$\frac{AT}{OR}$	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	$\frac{AT}{OR}$	20	1
				Wide	$\frac{AT}{OR}$	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	9
				Wide	$\frac{AT}{OR}$	10	10
			Graphic 1			20	11
			Graphic 2			20	12

Note: Maximum data transfer speed indicates amount of the data read out of a memory. Thus, the data transfer speed sent to the LCD driver in wide function is 20 Mbps.

5

Mode List

Table 10 Mode List

No.	Mode Name	Pin Name D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Config.	Graphic/ Character	Data Transfer	Wide Display	Attribute
1	Dual-screen character	1	0	0	0	0	Dual screen	Character	4-bit × 2	Normal	OR
		1	0	0	0	1					AT
2	Dual-screen wide character	1	0	0	1	0				Wide	OR
		1	0	0	1	1					AT
3	Dual-screen graphic 1	1	1	0	0	1		Graphic		—	—
4	Dual-screen graphic 2	1	1	0	0	0					
5	Single-screen character	0	0	0	0	0	Single screen	Character	4-bit	Normal	OR
		0	0	0	0	1					AT
6	Single-screen wide character	0	0	0	1	0				Wide	OR
		0	0	0	1	1					AT
7	Single-screen graphic 1	0	1	0	0	1		Graphic		—	—
8	Single-screen graphic 2	0	1	0	0	0					
9	8-bit character	0	0	1	0	0	Single screen	Character	8-bit	Normal	OR
		0	0	1	0	1					AT
10	8-bit wide character	0	0	1	1	0				Wide	OR
		0	0	1	1	1					AT
11	8-bit graphic 1	0	1	1	0	1		Graphic		—	—
12	8-bit graphic 2	0	1	1	0	0					
13	Large screen	1	1	1	0	1	Dual screen		4-bit × 2		

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/C, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22). The display mode can be controlled by either one of the external pins or the data bits of R22.

Note: The above 5 pins have 32 status combinations (high and low). Any combinations other than the above are prohibited, because they may cause malfunctions. If you set an prohibited combination, set the right combination again.

Internal Registers

The HD63645F/HD64645F has one address register and fourteen data registers. In order to select one out of fourteen data registers, the address of the data register to be selected must be written into the address register. The MPU can transfer data to/from the data register corresponding to the written address.

To be software compatible with the CRTC (HD6845), registers R2-R8, R16, and R17, which are not necessary for an LCD are defined as invalid for the LCTC.

Address Register (AR)

AR register (figure 21) specifies one out of 14 data registers. Address data is written into the address register when RS is low. If no register corresponding to a specified address exists, the address data is invalid.

Horizontal Total Characters Register (R0)

R0 register (figure 22) specifies a horizontal scanning period. The total number of horizontal characters less 1 must be programmed into this 8-bit register in character units. Nht indicates the horizontal scanning period including the period when the CPU occupies memory (total number of horizontal characters minus the number of horizontal displayed characters). Its units are, then, converted from time into the number of characters. This value should be specified according to the specification of the LCD system to be used.

Note the following restrictions

$$Nhd + \frac{16}{m} \leq Nht + 1$$

Mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

Horizontal Displayed Characters Register (R1)

R1 register (figure 23) specifies the number of characters displayed per row. The horizontal character pitches are 8 bits for normal character display and 16 dots for wide character display and graphic display.

Nhd must be less than the total number of horizontal characters.

Maximum Raster Address Register (R9)

R9 register (figure 24) specifies the number of rasters per row in characters mode, consisting of 5 bits. The programmable range is 0 (1 raster/row) to 31 (32 rasters/row).

Cursor Start Raster Register (R10)

R10 register (figure 25) specifies the cursor start raster address and its blink mode. Refer to table 11.

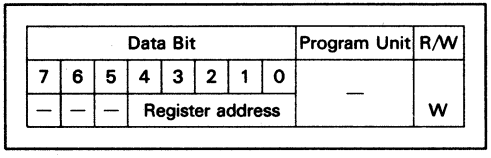


Figure 21 Address Register

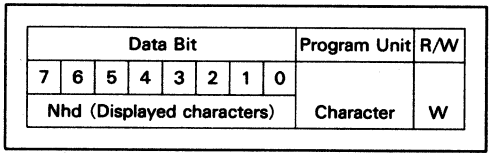


Figure 23 Horizontal Displayed Characters Register

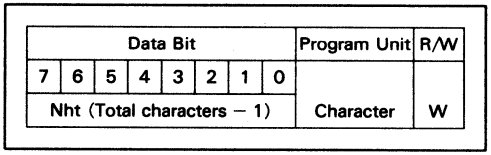


Figure 22 Horizontal Total Characters Register

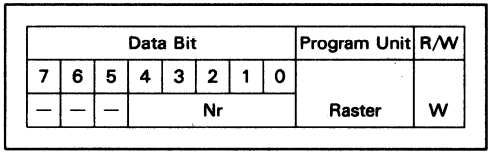
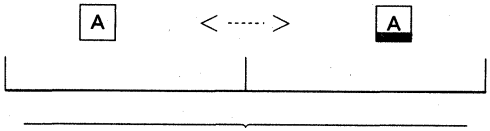


Figure 24 Maximum Raster Address Register



32- or 64-frame

Cursor End Raster Register (R11)

R11 register (figure 26) specifies the cursor end raster address.

Start Address Register (H/L)(R12/R13)

R12/R13 register (figure 27) specifies a buffer memory read start address. Updating this register facilitates paging and scrolling. R14/R15 register can be read and written to/from the MPU.

Cursor Address Register (H/L)(R14/R15)

R14/R15 register (figure 28) specifies a cursor display address. Cusor display requires setting R10 and R11, and CUDISP should be connected with MD12 (in character mode). This register can be read from and written to the MPU.

Horizontal Virtual Screen Width Register (R18)

R18 register (figure 29) specifies the memory width to determine the start address of the next row. By using this register, memory width can be specified larger than the number of horizontal displayed characters. Updating the display start address facilitates scrolling in any direction within a memory space.

The start address of the next row is that of the previous row plus Nir. If a larger memory width than display width is unnecessary, Nir should be set equal to the number of horizontal displayed characters.

Multiplexing Duty Ratio Register (H/L) (R19/R20)

R19/R20 register (figure 30) specifies the number of vertical dots of the display screen. The programmed value differs according to the LCD screen configuration.

In single screen configuration :

(Programmed value) = (Number of vertical dots) − 1.

Table 11 Cursor Blink Mode

B	P	Cursor blink mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	B	P	Ncs (Raster address)					Raster	W

Figure 25 Cursor Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nce (Raster address)					Raster	W

Figure 26 Cursor End Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R12)								Memory address	R/W
Memory address (L) (R13)									

Figure 27 Start Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R14)								Memory address	R/W
Memory address (L) (R15)									

Figure 28 Cursor Address Register

In dual screen configuration :

$$\text{(Programmed value)} = \frac{\text{(Number of vertical dots)}}{2} - 1.$$

Display Start Raster Register (R21)

R21 register (figure 31) specifies the start raster of the character row displayed on the top of the screen. The programmed value should be equal or less than the maximum raster address. Updating this register allows smooth scrolling in character mode.

Mode Register (R22)

The Or of the data bits of R22 (figure 32) register and the external terminals of the same name determines a particular mode. (figure 33)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual width)								Character	W

Figure 29 Horizontal Virtual Screen Width Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Raster address					Raster	W

Figure 31 Display Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	—	—	—	— (R19)	Ndh*	Raster	W
Ndl (Number of rasters – 1) (R20)									

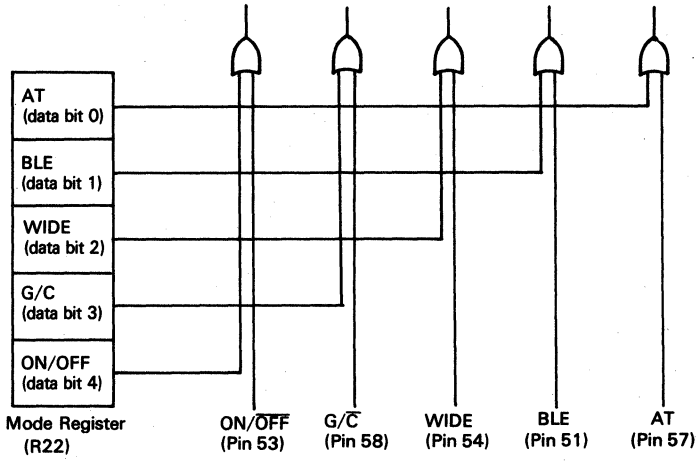
* : Number of rasters

Figure 30 Multiplexing Duty Ratio Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	ON/OFF	G/C	WIDE	BLE	AT	—	W

Figure 32 Mode Register

5



Notes: 1. AT (valid only when G/$\overline{C}$ is low (character mode))
AT = High: Attribute functions enabled, OR function disabled.
AT = Low: OR function enabled, attribute functions disabled.

2. BLE (valid only when G/$\overline{C}$ is low (character mode))
BLE = High: Blinking enable on the character specified by attribute RAM
BLE = Low: No blinking

3. WIDE (valid only when G/$\overline{C}$ is low (character mode))
WIDE = High: Wide display enabled
WIDE = Low: Normal display

4. G/$\overline{C}$
G/C = High: Graphic 1 display (when AT = Low) or Graphic 2 display (when AT = High)
G/C = Low: Character display

5. ON/$\overline{OFF}$
ON/$\overline{OFF}$ = High: Display on state
ON/$\overline{OFF}$ = Low: Display off state

Figure 33 Correspondence between Mode Register and External Pins

Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers are restricted as shown in Table 12.

Table 12 Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Register
Display Format	$1 < Nhd < Nht + 1 \leq 256$	R0, R1
	$Nhd + \frac{16}{m} * 1 \leq Nht + 1$	
	(No. of vertical dots) x (no. of horizontal dots) x (frame frequency; f_{FRM}) ≤ (data transfer speed; V)	R1, R19, R20
	$\left\{\begin{matrix}1\\2\end{matrix}\right\} * 2 \times (Nd + 1) \times Nhd \times \left\{\begin{matrix}8\\16\end{matrix}\right\} * 3 \, f_{FRM} \leq V$	
	$Nhd \leq Nir$	R1, R18
	$0 \leq Nd \leq 511$	R19, R20
Cursor Control	$0 \leq Ncs \leq Nce$	R10, R11
	$Nce \leq Nr$	R10, R9
Smooth Scroll	$Nsr \leq Nr$	R21, R9
Memory Width Set	$0 \leq Nir \leq 255$	R18

Notes' *1 m varies according to the modes. See the following table.

Mode No.	m
5,9	1
1,6,7,8,10,11,12,13	2
2,3,4	4

*2 Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5,6,7,8,9,10,11,12	1
1,2,3,4,13	2

*3 Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1,5,9	8
2,3,4,6,7,8,10,11,12,13	16

5

Reset

$\overline{RES}$ pin determines the internal state of LSI counters and the like. This pin does not affect register contents nor does it basically control output terminals.

Reset is defined as follows (Figure 34):

- At reset: the time when $\overline{RES}$ goes low
- During reset: the period while $\overline{RES}$ remains low
- After reset: the period on and after the $\overline{RES}$ transition from low to high
- Make sure to hold the reset signal low for at least 1 μs

$\overline{RES}$ pin should be pulled high by users during operation.

Reset State of Pins

$\overline{RES}$ pin does not basically control output pins, and operates regardless of other input pins.

1. Preserve states before reset:
   LU0-LU3, LD0-LD3, FLM, CL1, RA0-RA4
2. Fixed at high level:
   MI.CK
3. Preserve states before reset or fixed at low level according to the timing when the reset signal is input:
   DISPTMG, CUDISP, MA0-MA15
4. Fixed at high or low according to mode:
   CL2
5. Unaffected:
   DB_0-DB_7

Reset State of Registers

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be read or written even during a reset state; their contents will be preserved regardless of reset until they are rewritten to.

Notes for HD63645F/HD64645F

1. The HD63645/HD64645 are CMOS LSIs, and it should be noted that input pins must not be left disconnected, etc.
2. At power-on, the state of internal registers becomes undefined. The LSI operation is undefined until all internal registers have been programmed.

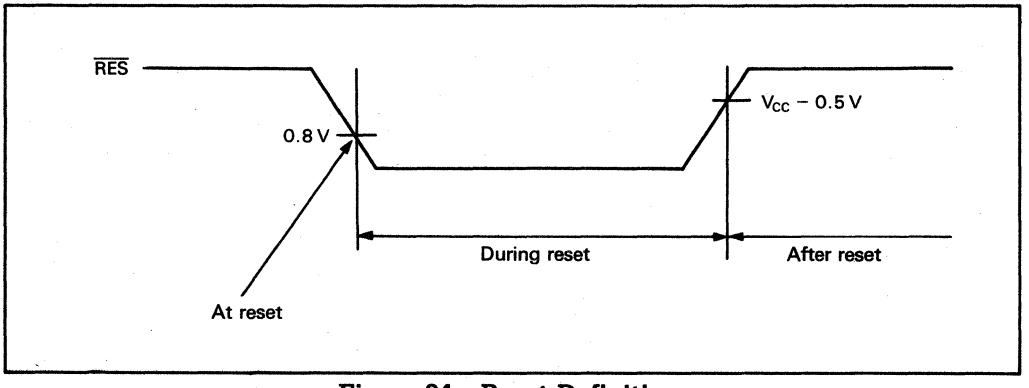


Figure 34 Reset Definition

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.
2. With respect to ground (GND = 0 V)

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL interface[1]	V_{OH}	2.4			V	I_{OH} = −400μA
	CMOS interface[1]		V_{CC}−0.8			V	I_{OH} = −400μA
Output low voltage	TTL interface	V_{OL}			0.4	V	I_{OL} = 1.6mA
	CMOS interface				0.8	V	I_{OL} = 400μA
Input leakage current	All inputs except DB_0−DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0−DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes: 1. TTL Interface; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM
2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.
3. If the capacitive loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

5

AC Characteristics

CPU Interface (HD63645 — 68 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
Enable cycle time	t_{CYCE}	500			ns	35
Enable pulse width (high)	P_{WEH}	220			ns	
Enable pulse width (low)	P_{WEL}	220			ns	
Enable rise time	t_{Er}			25	ns	
Enable fall time	t_{Ef}			25	ns	
$\overline{CS}$, RS, R/$\overline{W}$ setup time	t_{AS}	70			ns	
$\overline{CS}$, RS, R/$\overline{W}$ hold time	t_{AH}	10			ns	
DB_0-DB_7 setup time	t_{DS}	60			ns	
DB_0-DB_7 hold time	t_{DHW}	10			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

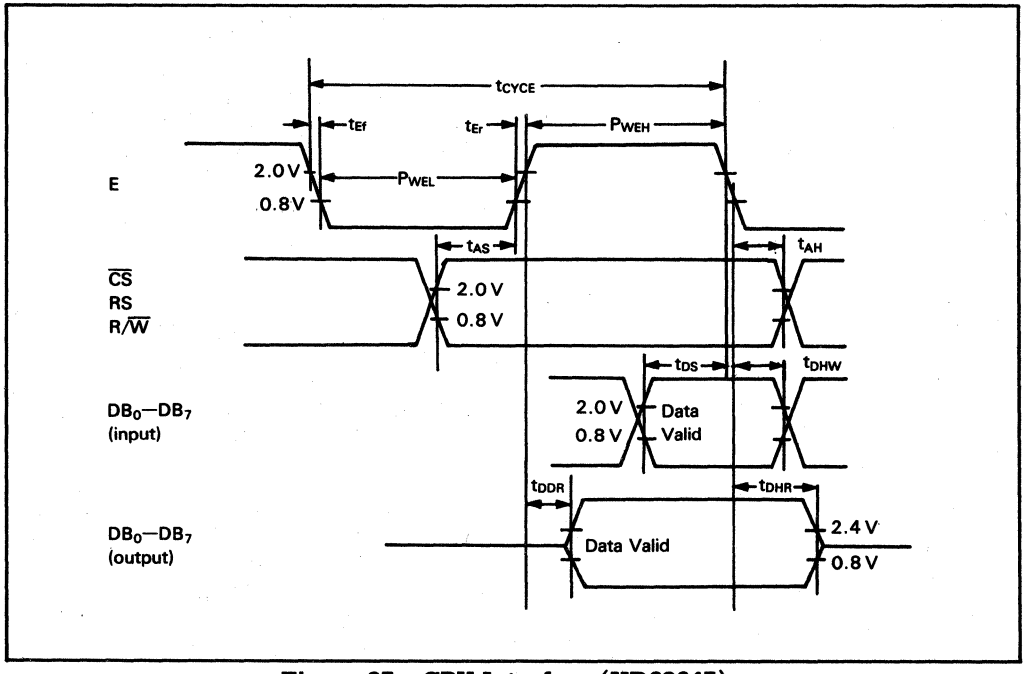


Figure 35 CPU Interface (HD63645)

CPU Interface (HD64645 — 80 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	36
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

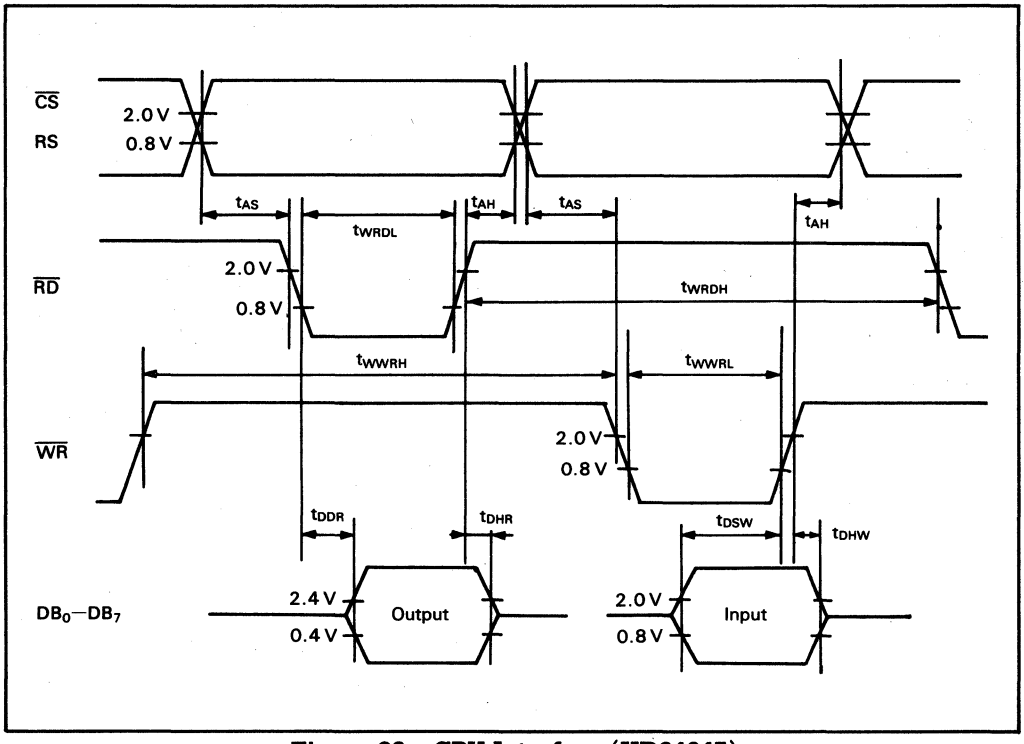


Figure 36 CPU Interface (HD64645)

5

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100	—	—	ns	37
DCLK high level width	t_{WDH}	30	—	—	ns	
DCLK low level width	t_{WDL}	30	—	—	ns	
DCLK rise time	t_{Dr}	—	—	20	ns	
DCLK fall time	t_{Df}	—	—	20	ns	
MCLK delay time	t_{DMD}	—	—	60	ns	
MCLK rise time	t_{Mr}	—	—	30	ns	
MCLK fall time	t_{Mf}	—	—	30	ns	
MA0-MA15 delay time	t_{MAD}	—	—	150	ns	
MA0-MA15 hold time	t_{MAH}	10	—	—	ns	
RA0-RA4 delay time	t_{RAD}	—	—	150	ns	
RA0-RA4 hold time	t_{RAH}	10	—	—	ns	
DISPTMG delay time	t_{DTD}	—	—	150	ns	
DISPTMG hold time	t_{DTH}	10	—	—	ns	
CUDISP delay time	t_{CDD}	—	—	150	ns	
CUDISP hold time	t_{CDH}	10	—	—	ns	
CL1 delay time	t_{CL1D}	—	—	150	ns	
CL1 hold time	t_{CL1H}	10	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
MD0-MD15 setup time	t_{MDS}	30	—	—	ns	
MD0-MD15 hold time	t_{MDH}	15	—	—	ns	

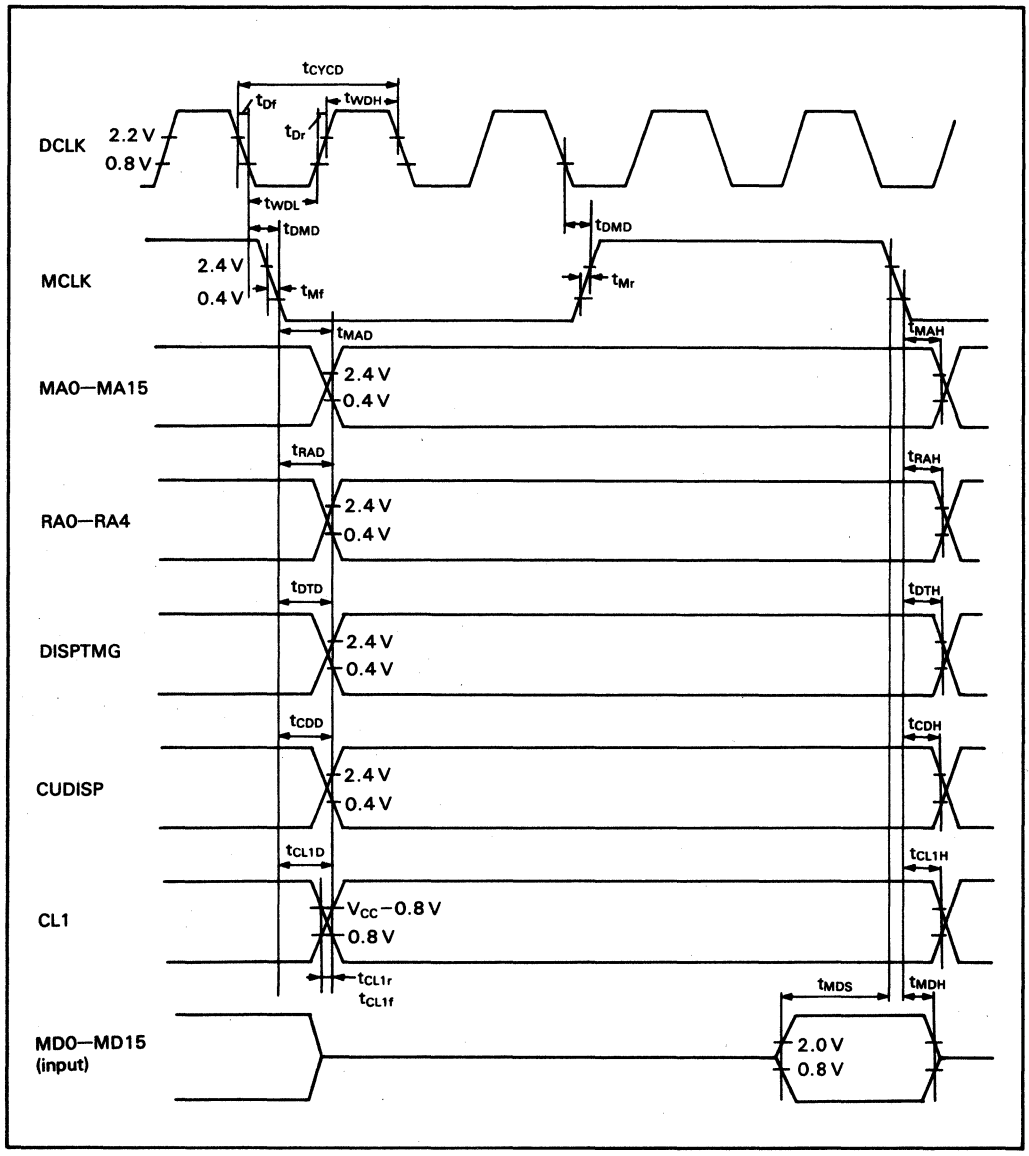


Figure 37 Memory Interface

5

AC Characteristics (Cont)

LCD Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50	—	—	ns	38
Display data hold time	t_{LDH}	100	—	—	ns	
CL2 high level width	t_{WCL2H}	100	—	—	ns	
CL2 low level width	t_{WCL2L}	100	—	—	ns	
FLM setup time	t_{FS}	500	—	—	ns	
FLM hold time	t_{FH}	300	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	

Note : At fCL2 = 3 MHz

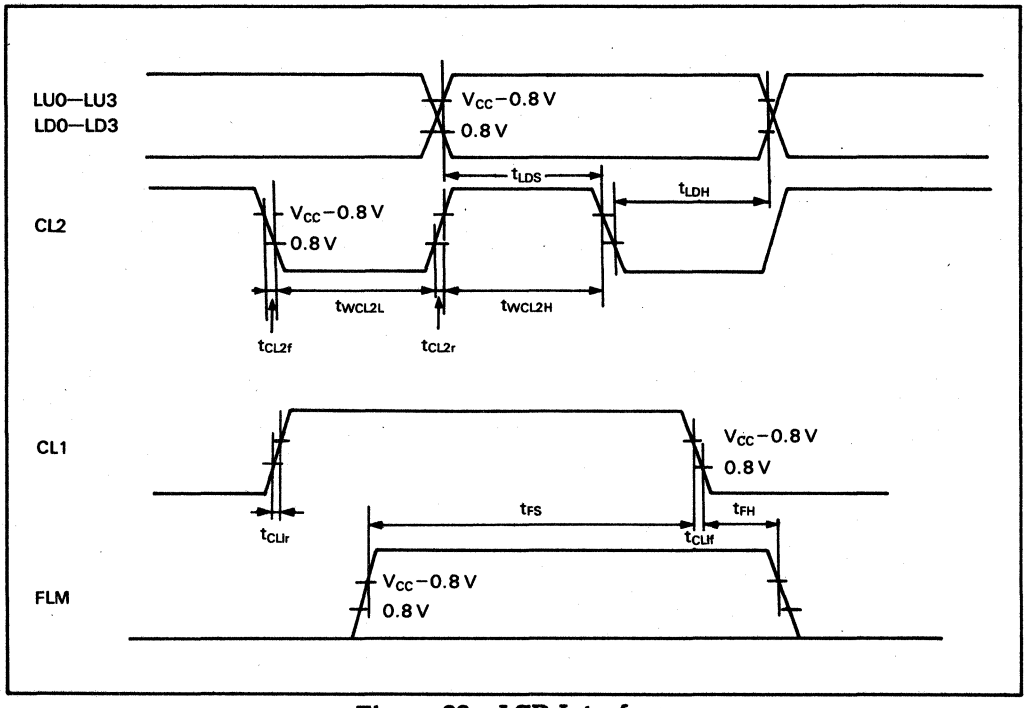
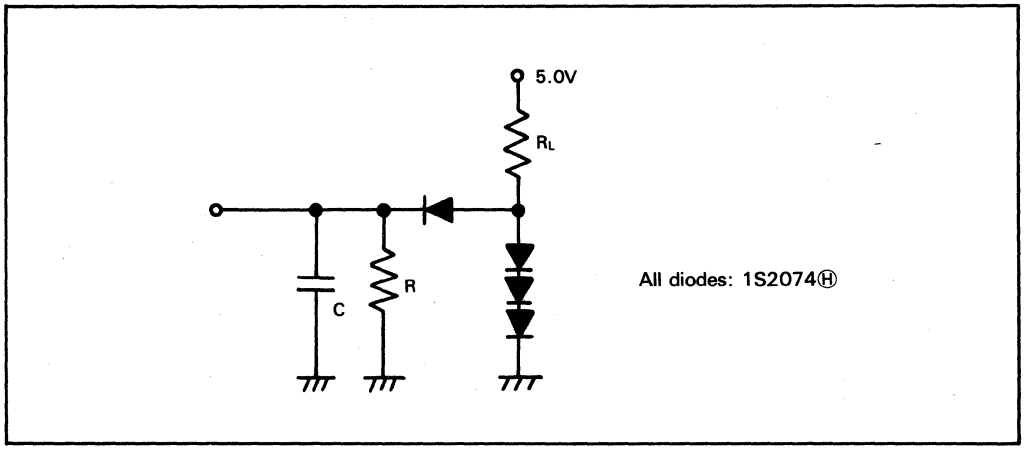


Figure 38 LCD Interface

AC Characteristics

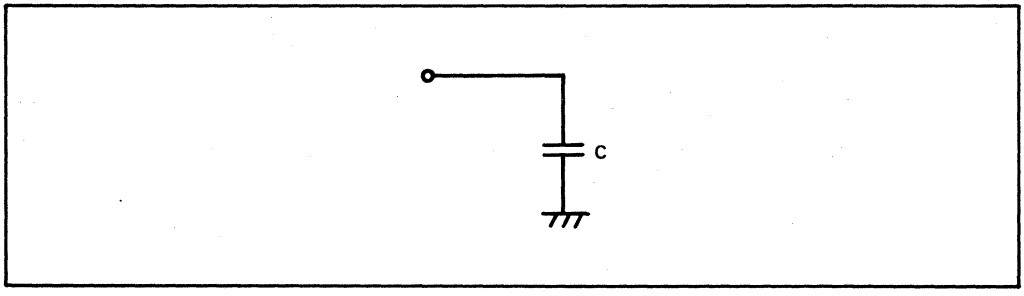
TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf: Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf: Specified



Capacitive Load

Terminal	C	Remarks
CL2	150 pF	tr, tf: Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf: Not specified
FLM	50 pF	



Refer to user's manual (No. 68-1-160) and application note (No. ADE-502-003) for detail of this product.

HD64646FS

LCD Timing Controller (LCTC)

Description

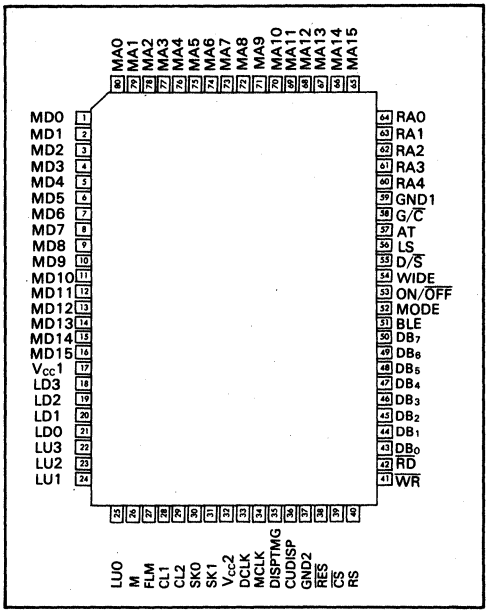
The HD64646F LCTC is a modified version of the HD64645F LCTC with different LCD interface timing.

The HD64646F is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/s in character mode
  —Up to 40 Mbits/s in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66204 (column) and HD66205 (common), HD66106 (column/common)
- CPU interface:
  80 family
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80B)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645F	2 MHz	68 System	FP-80
HD64645F	4 MHz	80 System	FP-80
HD64646FS	4 MHz	80 System	FP-80B

Differences Between HD64645F and HD64646FS

Figure 1 and figure 2 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Figure 1 shows the case without skew function and figure 2 shows the case with skew function.

In figure 1, high period between CL2 and CL1 of HD64645F overlap. HD64646FS has no overlap like HD64645F, and except for this overlap. HD64646FS is the same as HD64645F functionally.

Also for the skew function, phase relation between CL1 and CL2 changes. As figure 2 shows, data transfer period and CL1 high period of HD64646FS never overlap with the skew function.

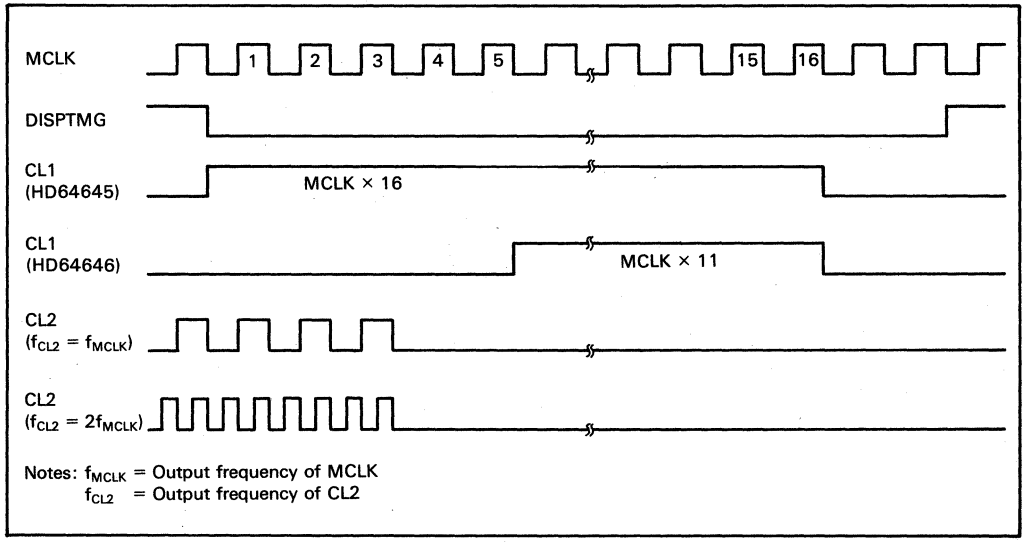


Figure 1 Differences between HD64645F and HD64646FS (no skew)

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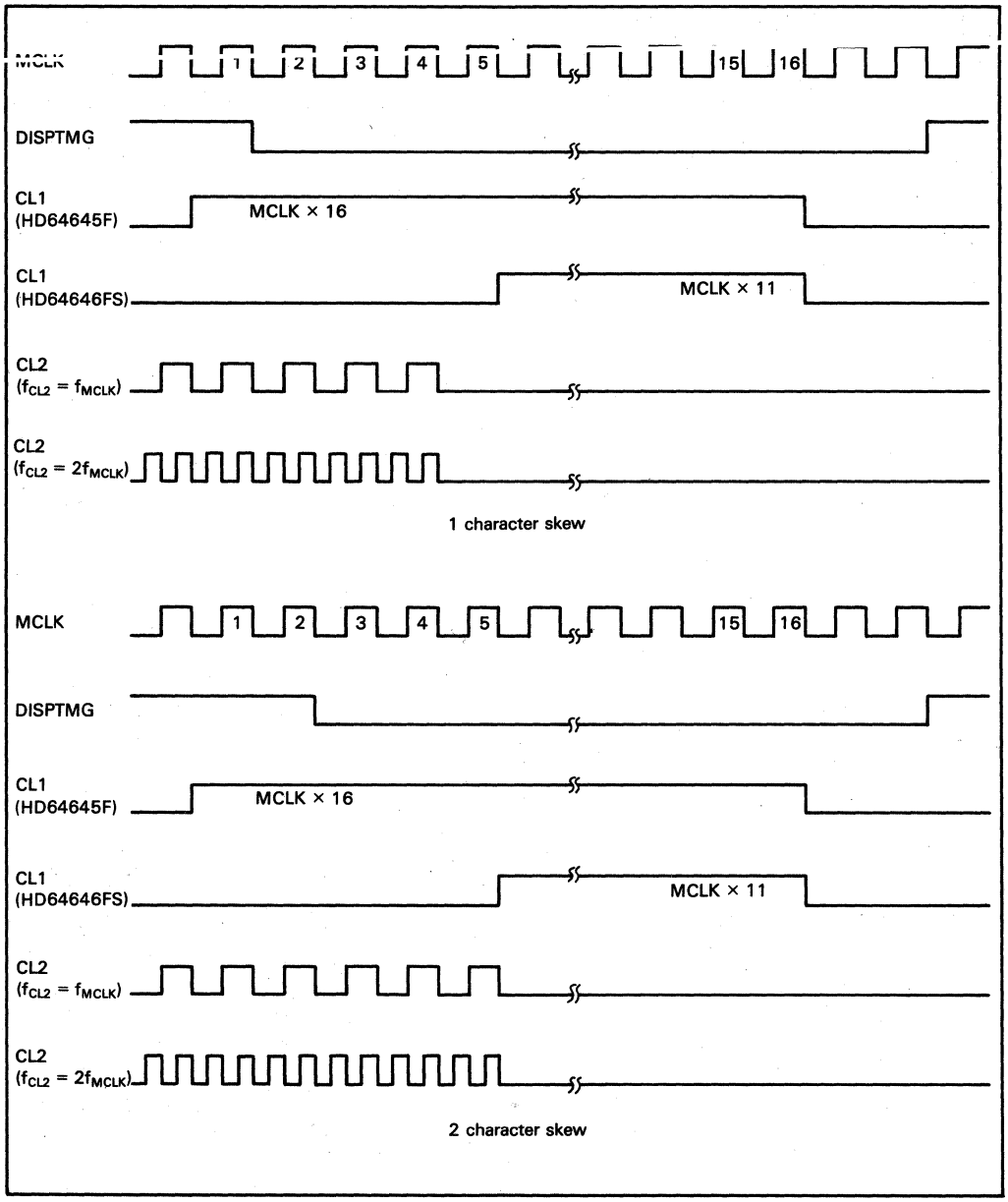

Figure 2 Differences between HD64645F and HD64646FS (skew)

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.
2. With respect to ground (GND = 0 V)

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	I_{OH} = −400 μA
	CMOS Interface[1]		V_{CC}−0.8			V	I_{OH} = −400 μA
Output low voltage	TTL Interface	V_{OL}			0.4	V	I_{OL} = 1.6 mA
	CMOS Interface				0.8	V	I_{OL} = 400 μA
Input leakage current	All inputs except DB_0−DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0−DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes: 1. TTL Interface: MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
CMOS Interface: LU0-LU3, LD0-LD3, CL1, CL2, M, FLM
2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.
3. If the capacitive loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

5

AC Characteristics

CPU Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190	—	—	ns	3
$\overline{RD}$ low level width	t_{WRDL}	190	—	—	ns	
$\overline{WR}$ high level width	t_{WWRH}	190	—	—	ns	
$\overline{WR}$ low level width	t_{WWRL}	190	—	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	—	ns	
DB_0-DB_7 setup time	t_{DSW}	100	—	—	ns	
DB_0-DB_7 hold time	t_{DHW}	0	—	—	ns	
DB_0-DB_7 output delay time	t_{DDR}	—	—	150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20	—	—	ns	

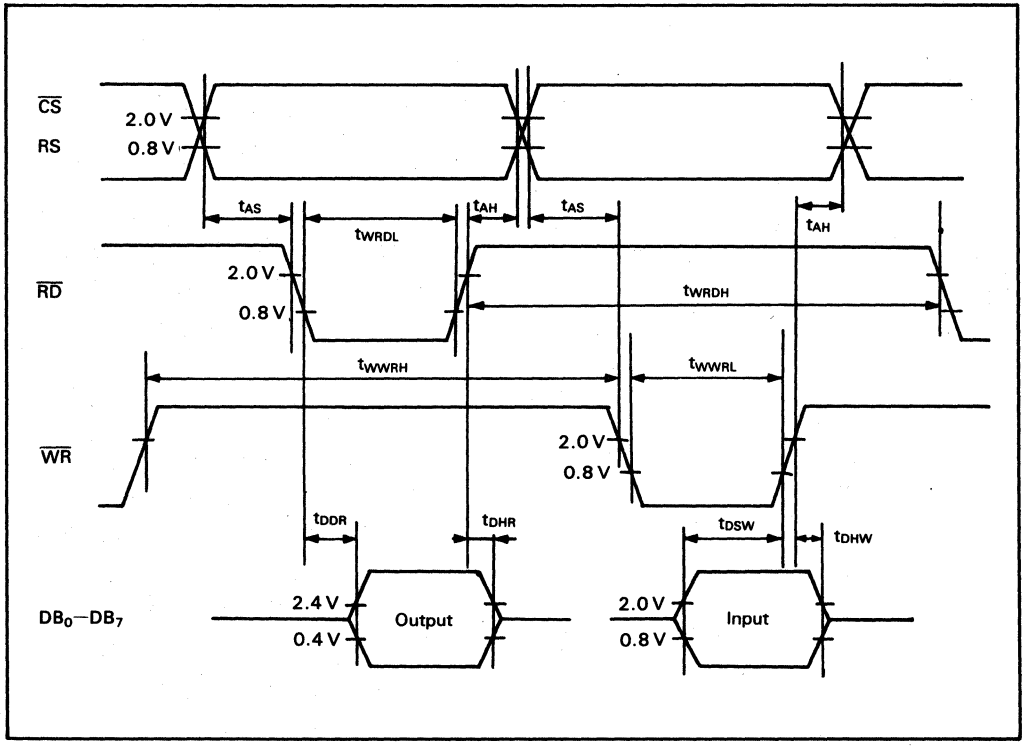

Figure 3 CPU Interface

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100	—	—	ns	4
DCLK high level width	t_{WDH}	30	—	—	ns	
DCLK low level width	t_{WDL}	30	—	—	ns	
DCLK rise time	t_{Dr}	—	—	20	ns	
DCLK fall time	t_{Df}	—	—	20	ns	
MCLK delay time	t_{DMD}	—	—	60	ns	
MCLK rise time	t_{Mr}	—	—	30	ns	
MCLK fall time	t_{Mf}	—	—	30	ns	
MA0-MA15 delay time	t_{MAD}	—	—	150	ns	
MA0-MA15 hold time	t_{MAH}	10	—	—	ns	
RA0-RA4 delay time	t_{RAD}	—	—	150	ns	
RA0-RA4 hold time	t_{RAH}	10	—	—	ns	
DISPTMG delay time	t_{DTD}	—	—	150	ns	
DISPTMG hold time	t_{DTH}	10	—	—	ns	
CUDISP delay time	t_{CDD}	—	—	150	ns	
CUDISP hold time	t_{CDH}	10	—	—	ns	
CL1 delay time	t_{CL1D}	—	—	150	ns	
CL1 hold time	t_{CL1H}	10	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
MD0-MD15 setup time	t_{MDS}	30	—	—	ns	
MD0-MD15 hold time	t_{MDH}	15	—	—	ns	

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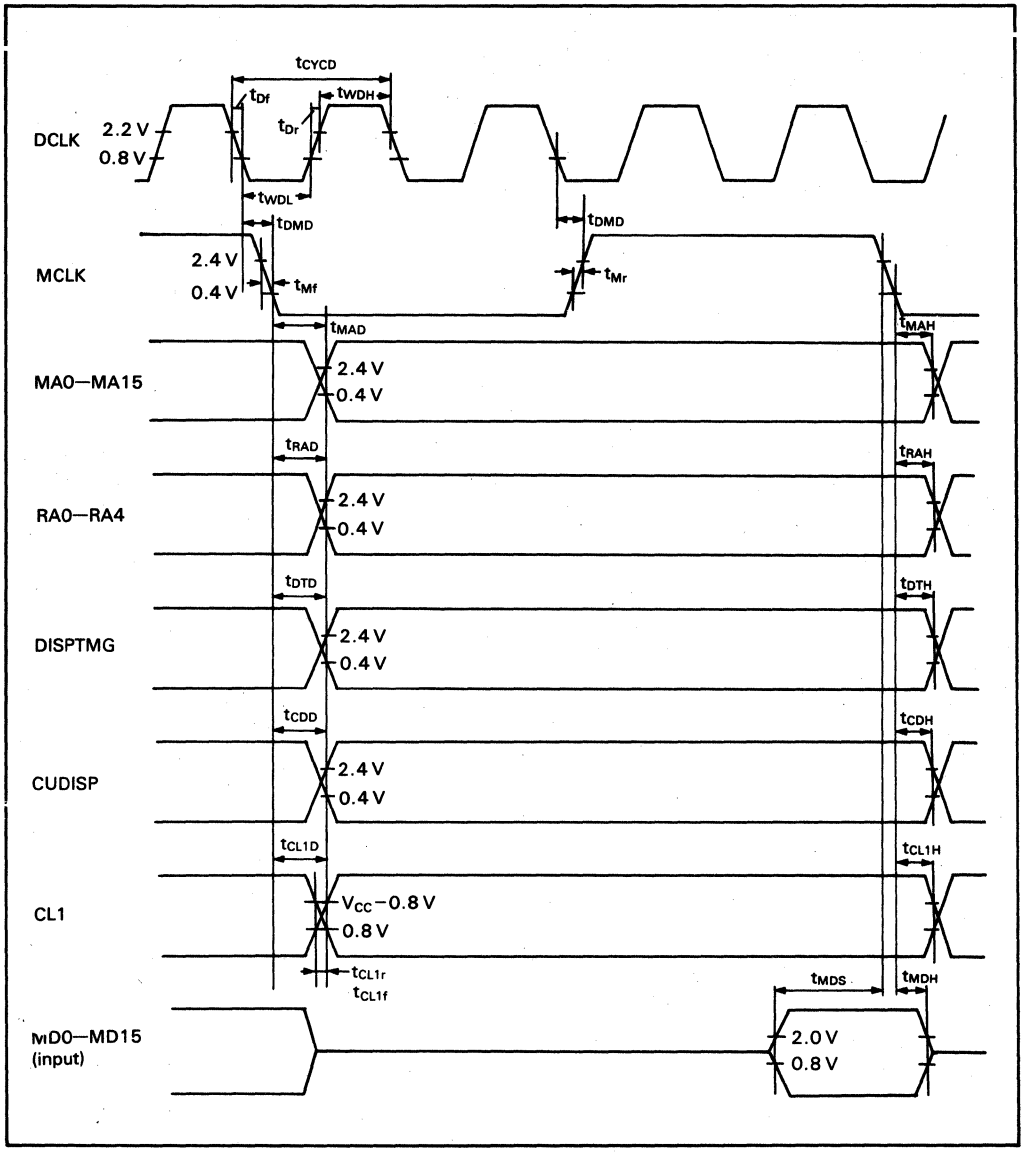


Figure 4 Memory Interface

AC Characteristics (Cont)

LCD Interface 1 (at f_{CL2} = 3 MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM stetup time	t_{Fs}	500	–	–	ns	5
FLM hold time	t_{FH}	300	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	100	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	100	–	–	ns	
CL2 low level width	t_{CL2L}	100	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	80	–	–	ns	
Display data hold time	t_{LDH}	100	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

LCD Interface 2 (at f_{CL2} = 5 MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	–	–	ns	Figure 5
FLM hold time	t_{FH}	500	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	70	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	50	–	–	ns	
CL2 low level width	t_{CL2L}	50	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	30	–	–	ns	
Display data hold time	t_{LDH}	30	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

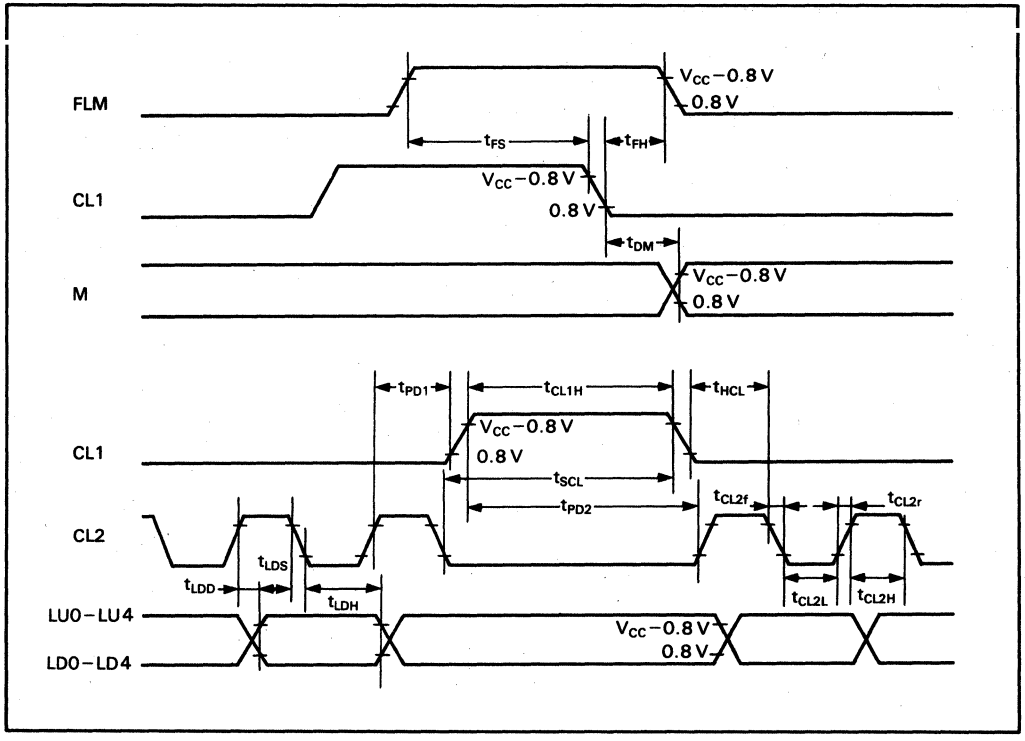
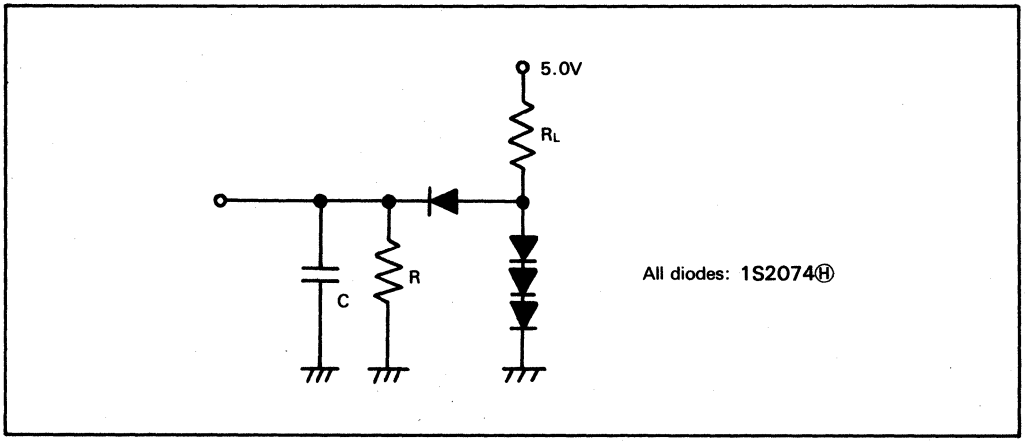


Figure 5 LCD Interface

AC Characteristics

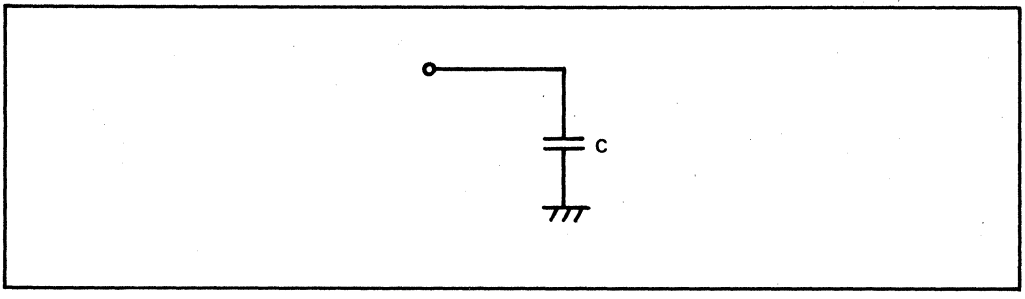
TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf: Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf: Specified



Capacitive Load

Terminal	C	Remarks
CL2	150 pF	tr, tf: Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf: Not specified
FLM	50 pF	



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HD66106F

(LCD Driver for High Voltage)

Description

The HD66106F LCD driver has a high duty ratio and many outputs for driving a large capacity dot matrix LCD panel.

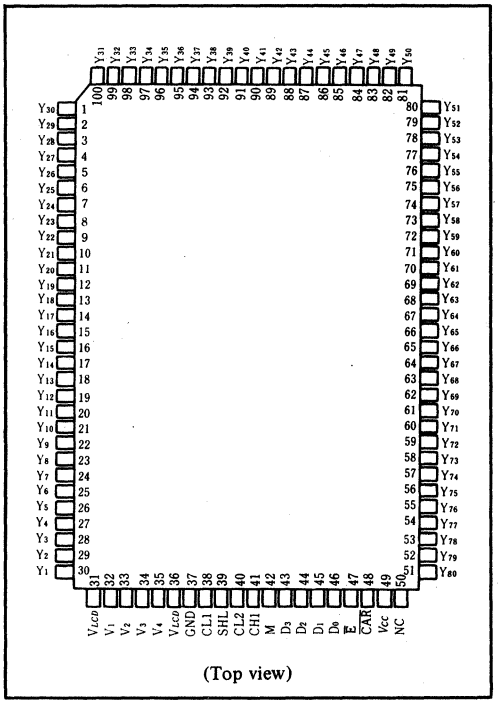
It includes 80 LCD drive circuits and can drive at up to 1/480 duty cycle. For example, only 14 drivers are enough to drive an LCD panel of 640 × 480 dots. It also easily interfaces with various LCD controllers because of its internal automatic chip enable signal generator.

Using this LSI sharply lowers the cost of an LCD system.

Features

- Column and row driver
- 80 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby function
- Recommended LCD controller LSIs: HD63645F and HD64645F (LCTC)
- Power supply: +5 V ± 10% for the internal logic, and 14.0 V to 37.0 V for LCD drive circuits
- Operation frequency: 6.0 MHz (max.)
- CMOS process
- 100-pin flat plastic package (FP-100)

Pin Arrangement



(Top view)

Pin Description

Power supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1-V_4 supply power for driving LCD (figure 1).

Control signals

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_3: D_0-D_3 input display data for the column driver (table 2).

Table 1 Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	49	V_{CC}	I
GND	37	Ground	I
V_{LCD}	31, 36	V_{LCD}	I
V_1	32	LCD voltage 1	I
V_2	33	V_2 LCD voltage 2	I
V_3	34	V_3 LCD voltage 3	I
V_4	35	V_4 LCD voltage 4	I
CL1	38	Clock 1	I
CL2	40	Clock 2	I
M	42	M	I
D_0-D_3	46-43	Data 0 to data 3	I
SHL	39	Shift left	I
$\overline{E}$	47	Enable	I
$\overline{CAR}$	48	Carry	O
CH1	41	Channel 1	I
Y_1-Y_{80}	30-1, 100-51	Drive outputs 1-80	O
NC	50	No connection	–

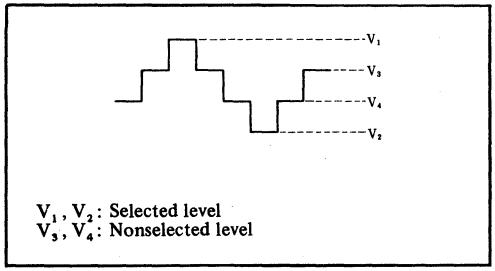


Figure 1 Power Supply for Driving LCD

Table 2 Relation between Display Data and LCD State

Display Data	LCD Outputs	LCD
1 (= high level)	Selected level	On
0 (= low level)	Nonselected level	Off

5

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, E connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). $\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip drives columns when CH1 = V_{CC}, and rows when CH1 = GND.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, or V_4—according to the combination of M and display data (figure 3).

NC: NC is not used. Do not connect any wire.

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI is Used as a Row Driver)

SHL	Shift Direction of Shift Register				Scan Direction of Selected Line				
V_{CC}	$\overline{E}$	→ 1	→ 2	→ 3 ----------→ 80	Y_1	→ Y_2	→ Y_3	----------→	Y_{80}
GND	$\overline{E}$	→ 80	→ 79	→ 78 ----------→ 1	Y_{80}	→ Y_{79}	→ Y_{78}	----------→	Y_1

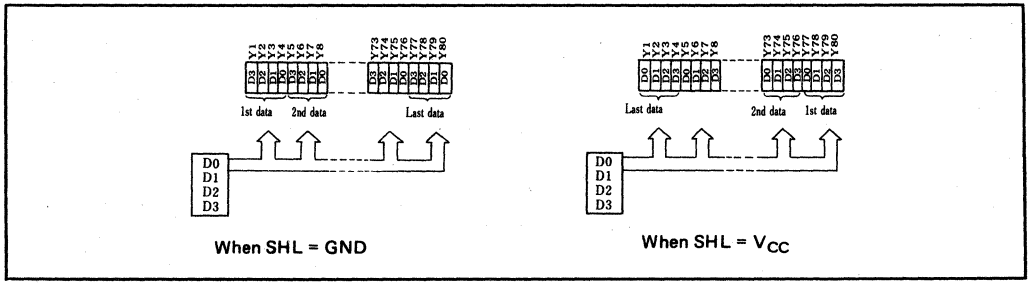


Figure 2 Relation between SHL and Data Output (When LSI is Used as a Column Driver)

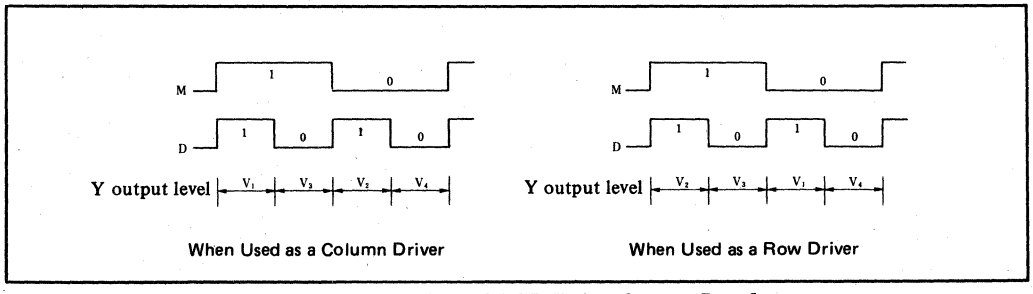


Figure 3 Selection of LCD Drive Output Level

Internal Block Diagram

LCD Drive Circuits

The HD66106F (figure 4) begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Latch Circuit 2

When the LSI is used as a column driver, latch circuit 2 functions as an 80-bit latch circuit. It latches the data sent from latch circuit 1 at the fall of CL1 and transfers its outputs to the LCD drive circuits.

When the LSI is used as a row driver, this circuit functions as an 80-bit bidirectional shift register. The data sent from the $\overline{E}$ pin shifts at the fall of CL2. When SHL = V_{CC}, the data shifts from bit 1 to bit 80 in order of entry. When SHL = GND, the data shifts from bit 80 to bit 1.

Latch Circuit 1

Latch circuit 1 is composed of twenty 4-bit parallel data latches. It latches the display data D_0-D_3 at the fall of CL2 when the LSI is used as a column driver. The signals sent from the selector determine which 4-bit latch should latch the data.

Selector

The selector is composed of a 5-bit up and down counter and a decoder. When the LSI is used as a column driver, it generates the latch signal to be sent to latch circuit 1, incrementing the counter at the negative edge of CL2.

Controller

The controller operates when the LSI is used as a column driver. It stops data latching when twenty pulses of CL2 have been input (= power-down function) and automatically generates the chip enable signal announcing the start of data latching into the next LSI.

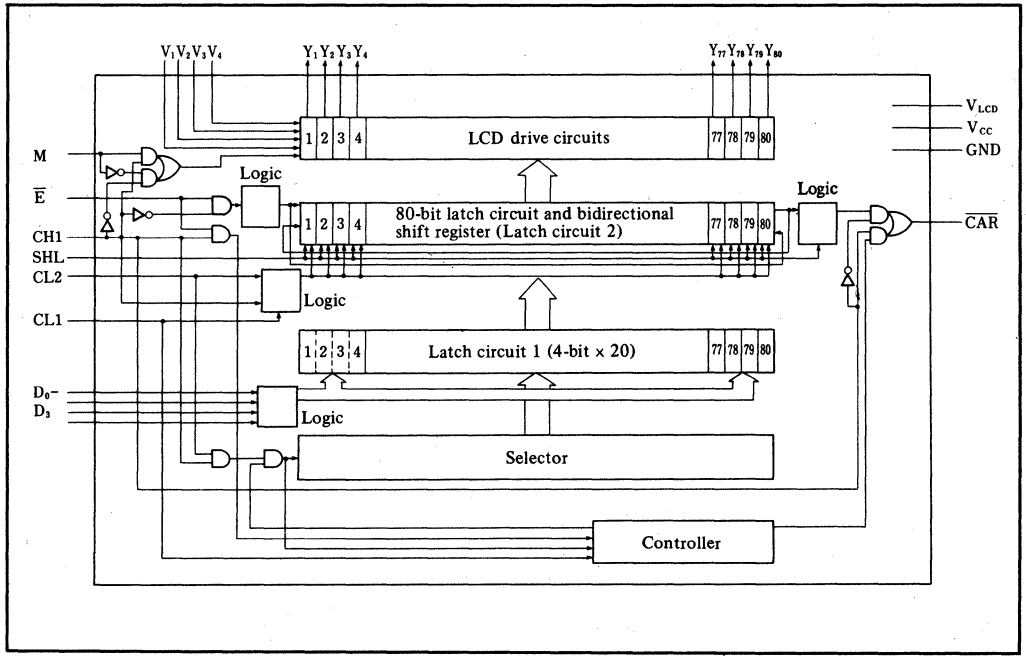


Figure 4 Block Diagram

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Functional Description

When Used as a Column Driver

The HD66106F begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Data outputs change at the fall of CL1. Latched data d_1 is transferred to the output pin Y_1 and d_{80} to Y_{80} when SHL = GND. Conversely, d_{80} is transferred to Y_1 and d_1 to Y_{80} when SHL = V_{CC}. The output level is selected out of V_1-V_4 according to the combination of display data and the alternating signal M (figure 5).

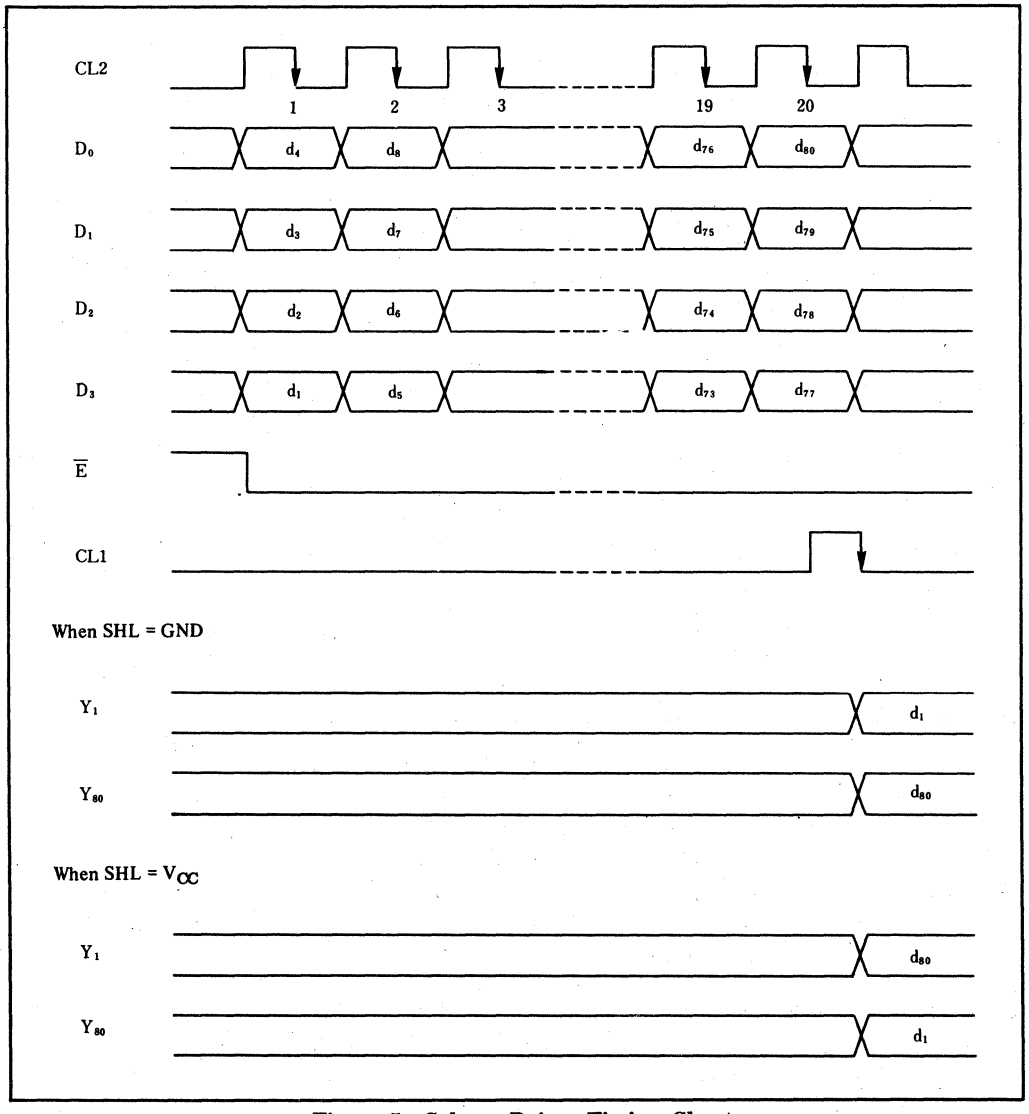

Figure 5 Column Driver Timing Chart

When Used as a Row Driver

The HD66106F shifts the line scan data sent from the pin $\overline{E}$ in order at the fall of CL2. When SHL = V_{CC}, data is shifted from Y_1 to Y_{80} and Y_{80} to Y_1 when SHL = GND.

In both cases, the data delayed for 80 bits by the shift register is output from the $\overline{CAR}$ pin to become the line scan data for the next LSI (figure 6).

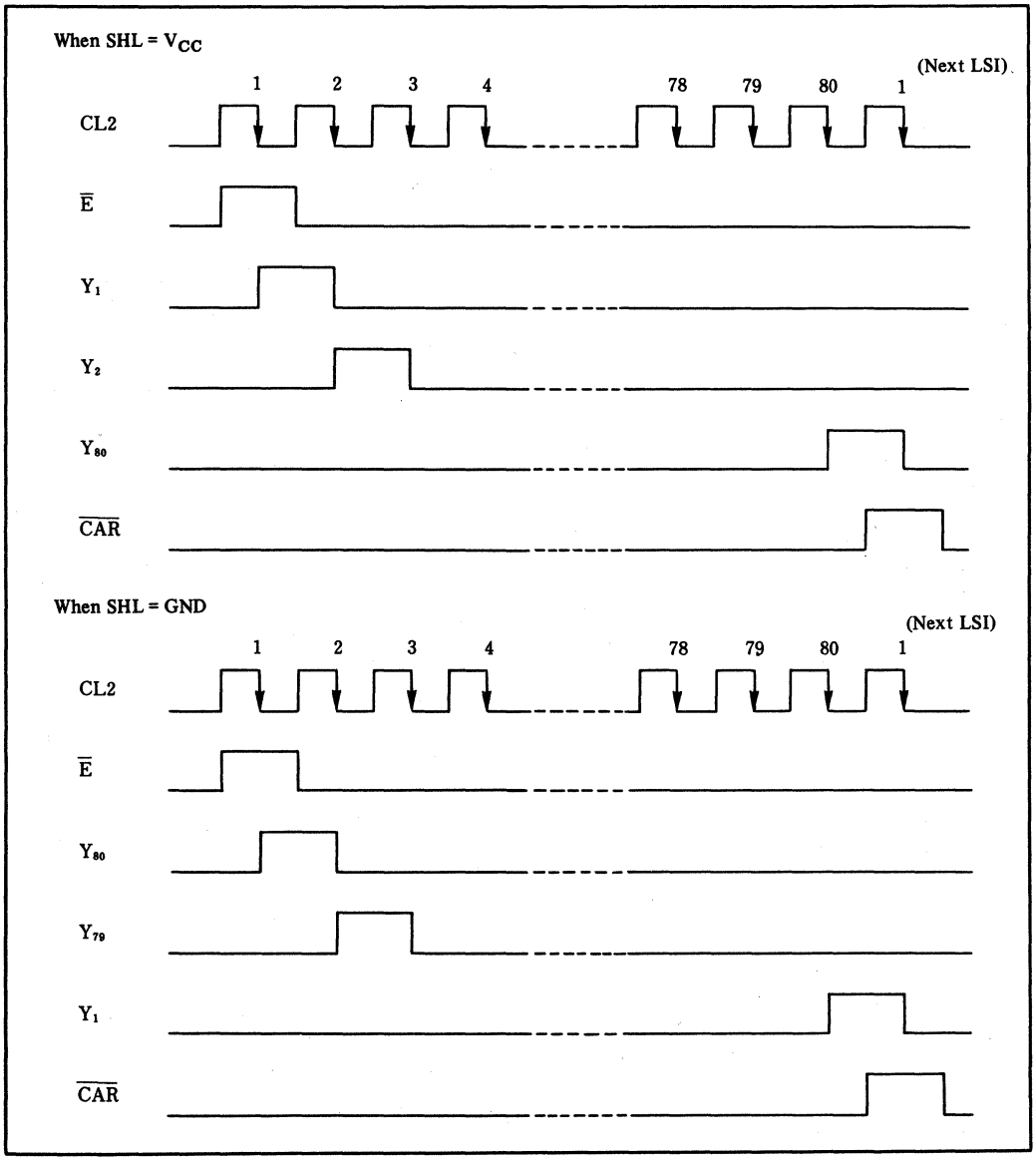

Figure 6 Row Driver Timing Chart

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LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 7). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 8).

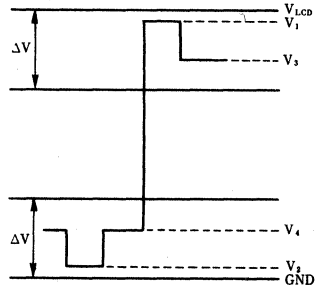


Figure 7 Driver's Output Waveform and Each Level of Voltage

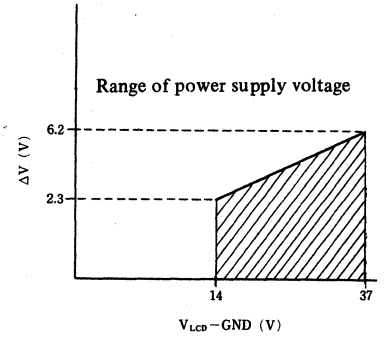
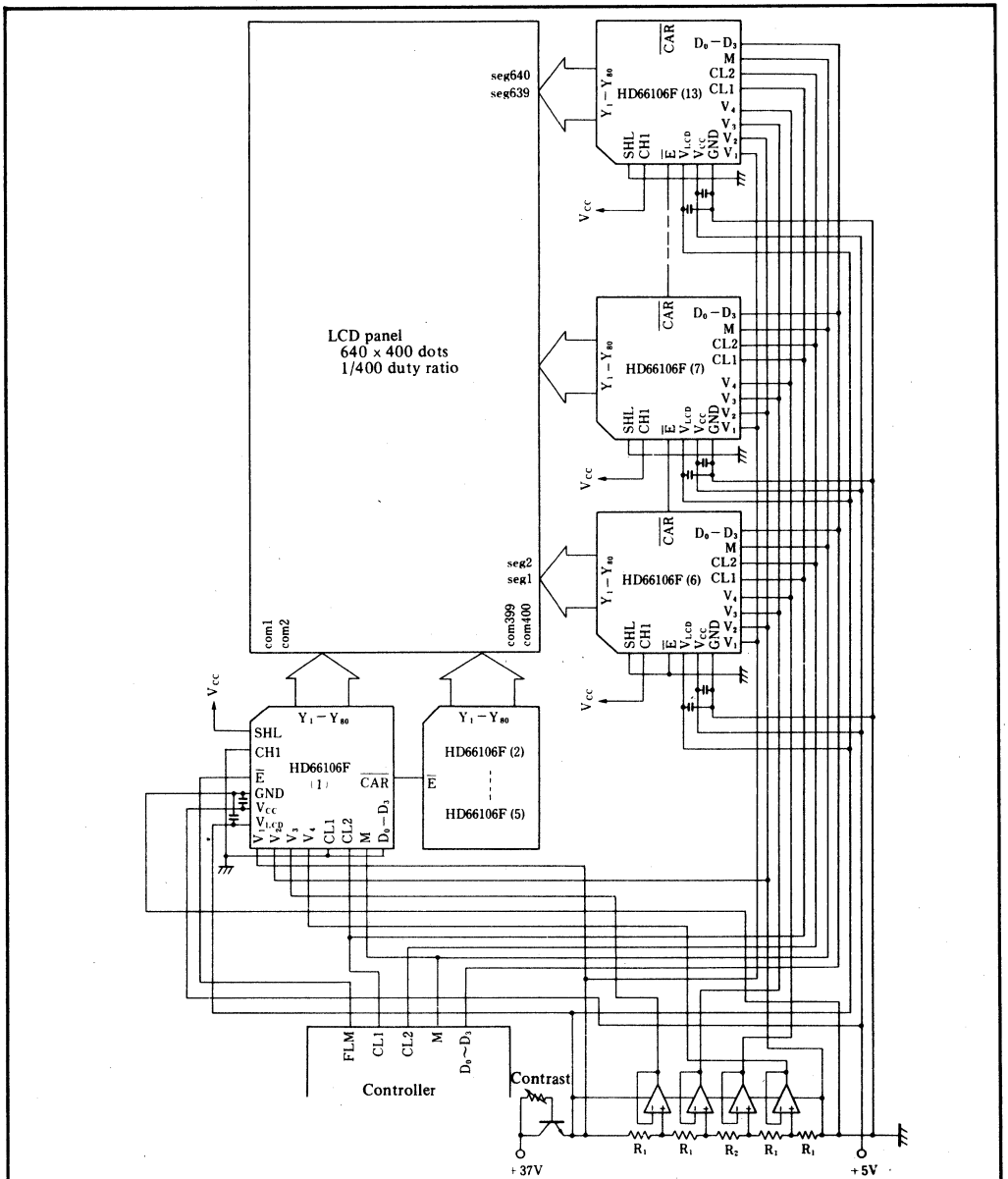


Figure 8 Power Supply Voltage V_{LCD}-GND and ΔV

Application Example

Application Diagram

Figure 9 shows an example of an LCD panel of 640 x 400 dots driven by HD66106Fs.



Notes:
1. R_1 and R_2 depend on the LCD panel in use. When using an LCD panel with 1/20 bias, $R_1/(4R_1 + R_2)$ should be 1/20. For example, R_1 = 3kΩ and R_2 = 48kΩ.
2. Use bypass capacitors to stabilize power supply when designing a board. It is desirable to use two capacitors with some 0.1 μF per LSI, putting one between V_{LCD} and GND, and the other between V_{CC} and GND.

Figure 9 Application Example

Timing waveform example

Figures 10 and 11 show the timing waveforms of the application example shown in figure 9.

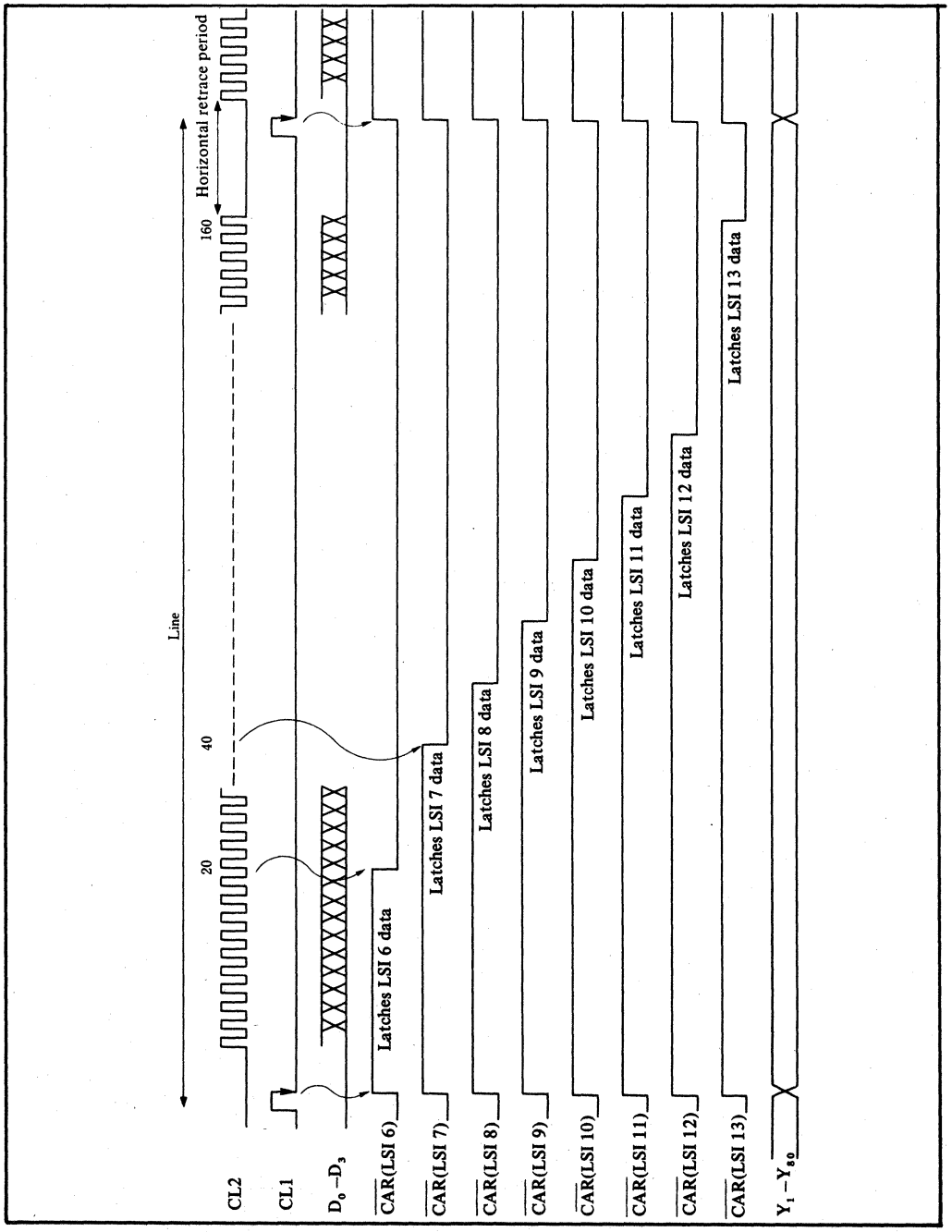


Figure 10 Timing Waveform for Column Drivers (LSI 6-LSI 13)

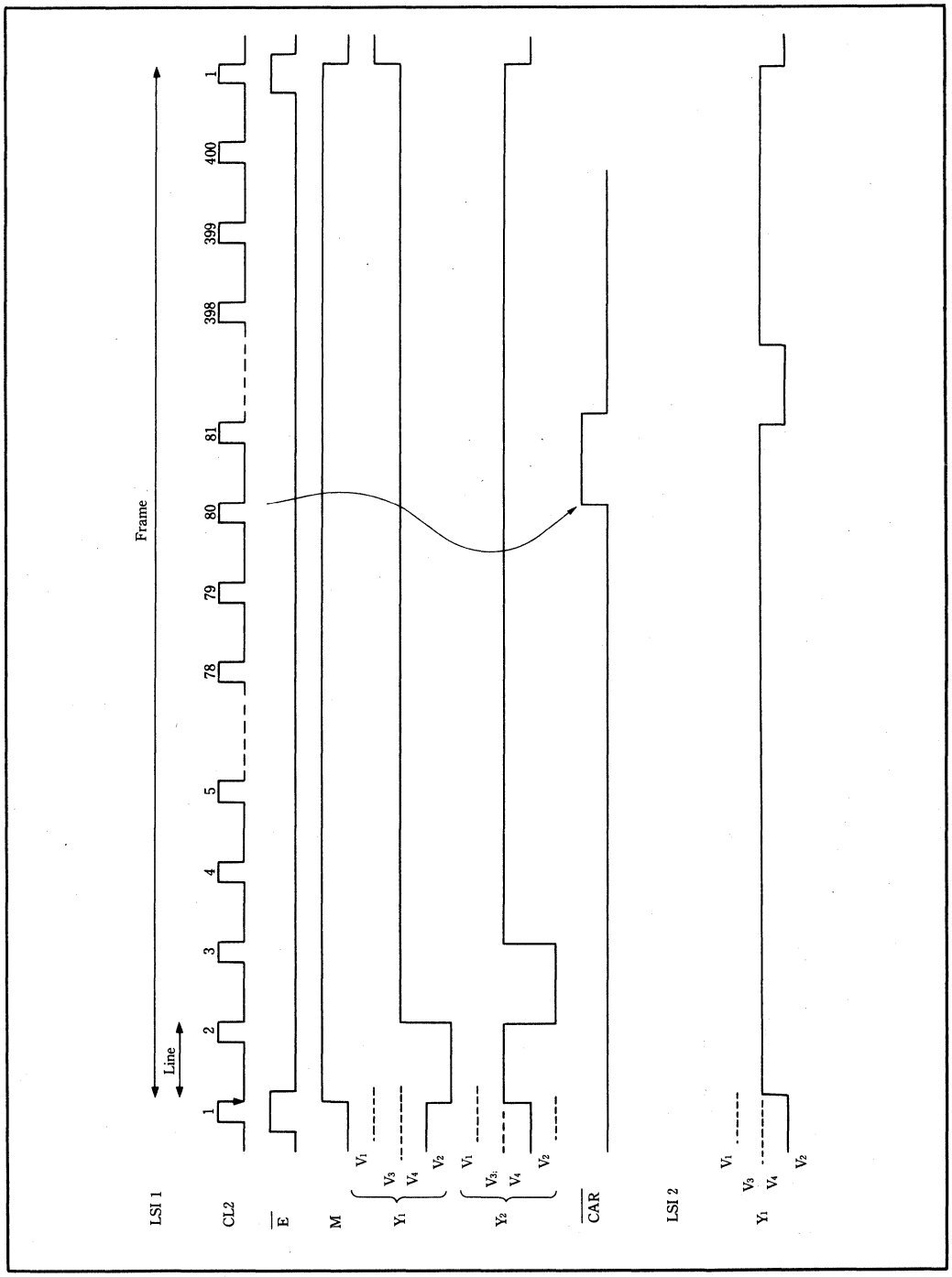


Figure 11 Timing Waveform for Row Drivers (LSI 1-LSI 5)

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Supply Voltage	Logic circuits	V_{CC}	−0.3 to +7.0	V	1
	LCD drive circuits	V_{LCD}	−0.3 to +38	V	1
Input voltage (Logic)		V_{T1}	−0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (LCD drive)		V_{T2}	−0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	−20 to +75	°C	
Storage temperature		T_{stg}	−55 to +125	°C	

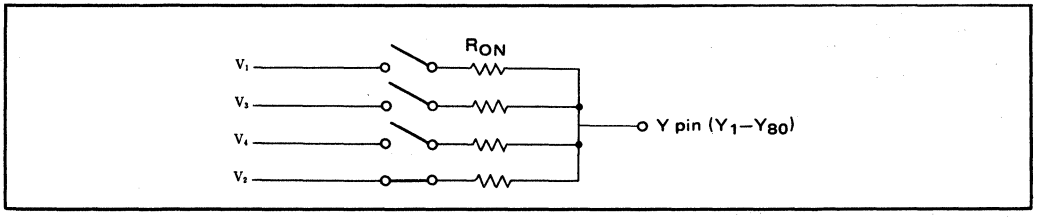
Notes: 1. Reference point is GND (= 0 V).
2. Applies to the input pins for logic circuits.
3. Applies to the input pins for LCD drive circuits.
4. Using an LSI beyond its maximum rating may result in its permanent destruction. LSIs should usually be used under electrical characteristics for normal operations. Exceeding any of these limits may adversely affect reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to 75°C unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	0.8 x Vcc	–	Vcc	V		
Input low voltage	V_{IL}		0	–	0.2 x V_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC} – 0.4	–	–	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}		–	–	0.4	V	I_{OL} = 0.4 mA	
Vi-Yj on resistance	R_{ON}	Y_1–Y_{80}, V_1–V_4	–	–	3.0	kΩ	I_{ON} = 100 μA	4
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	–5.0	–	5.0	μA	V_{IN} = V_{CC} to GND	
Input leakage current (2)	I_{IL2}	V_1–V_4	–50.0	–	50.0	μA	V_{IN} = V_{LCD} to GND	
Current consumption (1)	I_{CC1}		–	–	3.0	mA	f_{CL2} = 6 MHz,	
(2)	I_{LCD1}		–	–	0.5	mA	f_{CL1} = 28 kHz	1
(3)	I_{ST}		–	–	0.2	mA	At the standby state f_{CL2} = 6 MHz, f_{CL1} = 28 kHz	2
(4)	I_{CC2}		–	–	0.2	mA	f_{CL1} = 28 kHz,	1
(5)	I_{LCD2}		–	–	0.1	mA	f_m = 35 Hz	3

Notes: 1. Input and output current is excluded. When the input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit. V_{IH} and V_{IL} must be fixed at V_{CC} and GND respectively to avoid it.
2. Applies when the LSI is used as a column driver.
3. Applies when the LSI is used as a row driver.
4. Indicates the resistance between Y pin and V pin (one of V_1, V_2, V_3, and V_4) when it supplies load current to one of Y_1–Y_{80} pins.
Conditions: V_{LCD} – GND = 37 V
V_1, V_3 = V_{LCD} – 2/20 (V_{LCD} – GND)
V_2, V_4 = GND + 2/20 (V_{LCD} – GND)



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AC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to +75°C unless otherwise noted)

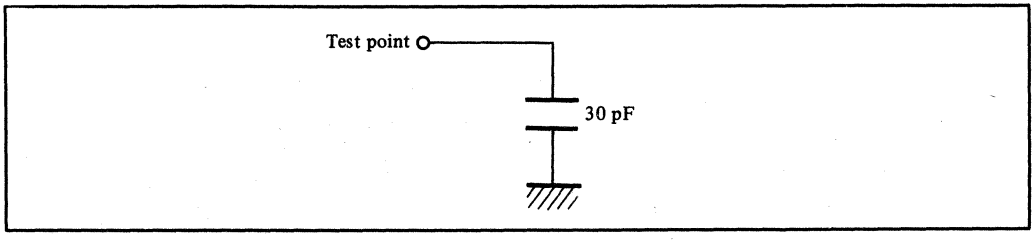
Column Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{cyc}	CL2	166	–	–	ns	
Clock high level width	t_{CWH}	CL2	50	–	–	ns	
Clock low level width	t_{CWL}	CL2	50	–	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	–	ns	
Clock rise/fall time	t_{ct}	CL1, CL2	–	–	30	ns	
Data setup time	t_{DSU}	D_0–D_3	30	–	–	ns	
Data hold time	t_{DH}	D_0–D_3	30	–	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	50	–	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	–	80	ns	1
M phase difference	t_{CM}	M, CL1	–	–	300	ns	

Row Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock low level width	t_{WL1}	CL2	5	–	–	μs	
Clock high level width	t_{WH1}	CL2	125	–	–	ns	
Data setup time	t_{DS}	$\overline{E}$	100	–	–	ns	
Data hold time	t_{DH}	$\overline{E}$	30	–	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	–	3	μs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	–	ns	1
Clock rise/fall time	t_{ct}	CL2	–	–	30	ns	

Note: 1. Values when the following load circuit is connected:



Column Driver

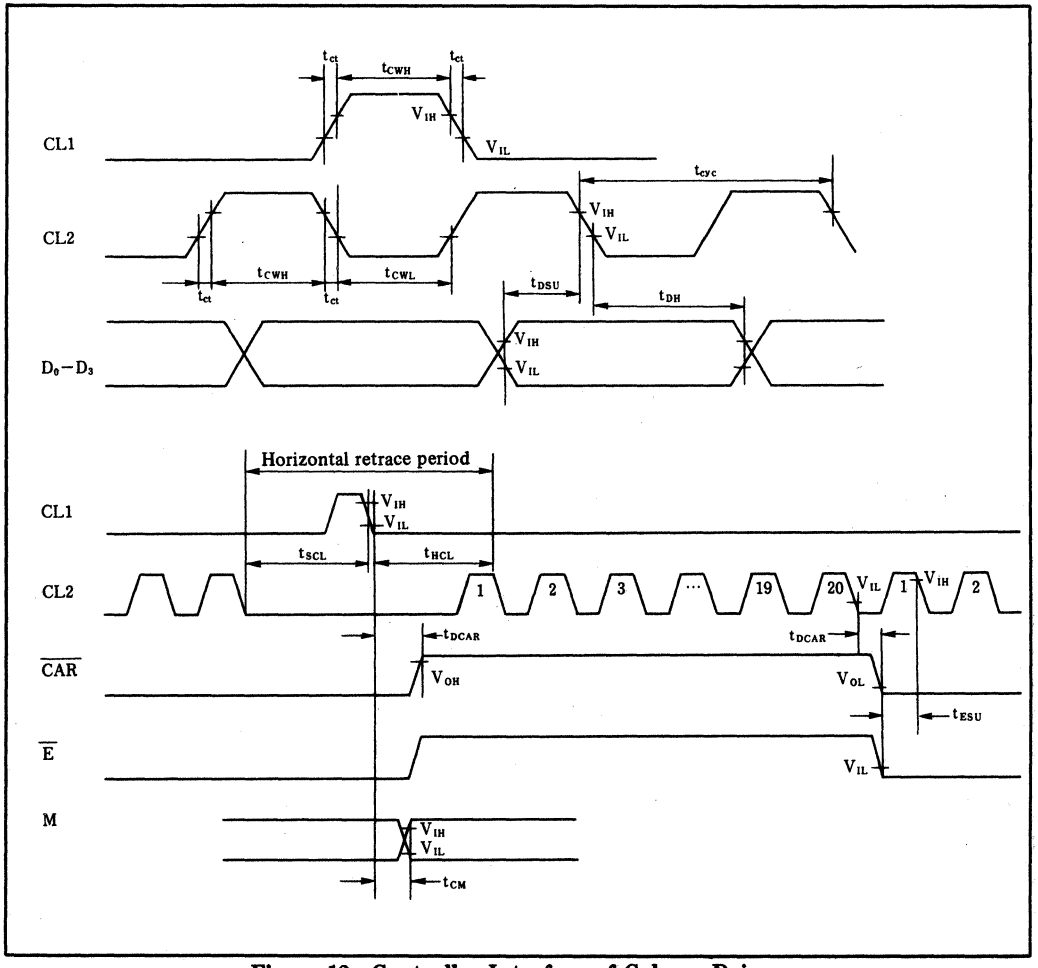


Figure 12 Controller Interface of Column Driver

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Row Driver

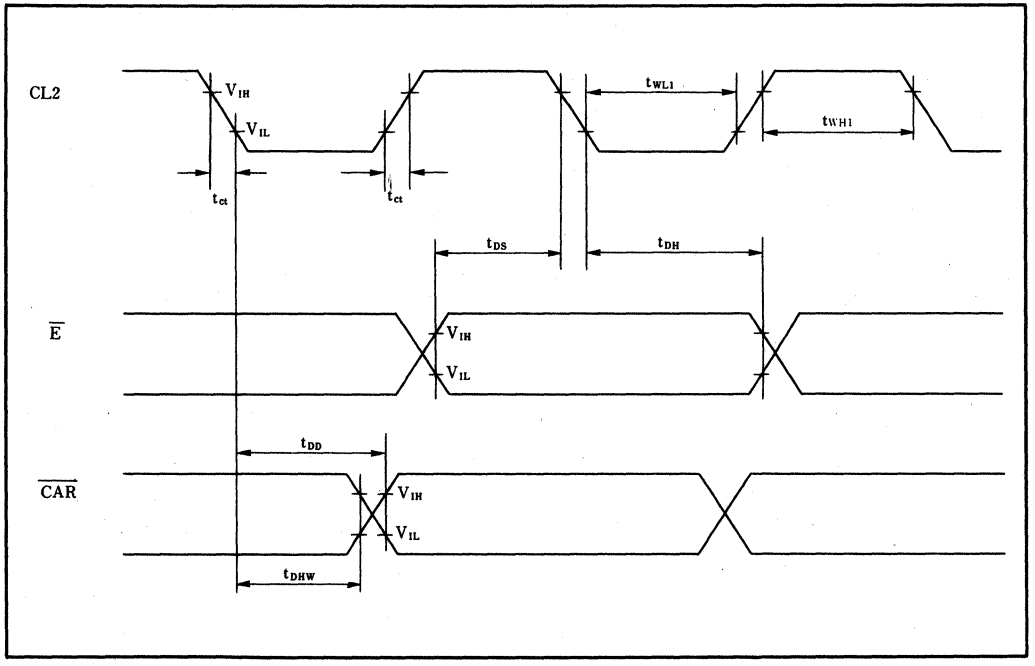


Figure 13 Controller Interface of Row Driver

HD66107T
(LCD Driver for High Voltage)

Description

The HD66107T is a multi-output, high duty ratio LCD driver used for large capacity dot matrix LCD panels. It consists of 160 LCD drive circuits with a display duty ratio up to 1/480: the seven HD66107Ts can drive a 640 × 480 dots LCD panel. Moreover, the LCD driver enables interfaces with various LCD controllers due to a built-in automatic generator of chip enable signals. Use of the HD66107T can help reduce the cost of an LCD-panel configuration, since it reduces the number of LCD drivers, compared with use of the HD61104 and HD61105.

Features

- Column and row driver
- 160 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit and 8-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby mode
- Recommended LCD controller LSIs: HD63645F, HD64645F, and HD64646FS (LCTC), HD66840/HD66841 (LVIC), HD66850 (CLINE)
- Power supply voltage
  —internal logic: +5 V ± 10%
  —LCD drive circuit : 14.0 to 37.0 V
- Operation frequency: 8.0 MHz (max.)
- CMOS Process
- 192-pin TCP (Tape Carrier Package)

Pin Description

Power Supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuits. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

Table 1 Pin Function

Symbol	Pin No.	Pin name	Input/output
V_{CC}	167	V_{CC}	
GND	161, 186, 187	Ground	
V_{LCD}	166, 192	V_{LCD}	
V1L, R V2L, R V3L, R V4L, R	191, 165 188, 162 190, 164 189, 163	V1L, V1R V2L, V2R V3L, V3R V4L, V4R	
CL1	183	Clock 1	Input
CL2	184	Clock 2	Input
M	182	M	Input
D_0-D_7	174-181	DATA0-DATA7	Input
SHL	172	Shift left	Input
CH2	171	Channel 2	Input
BS	173	Bus Select	Input
TEST	185	TEST	Input
Y1-Y160	1-160	Y1-Y160	Output
SHL	172	Shift left	Input
$\overline{E}$	169	Enable	Input
$\overline{CAR}$	168	Carry	Onput
CH1	170	Channel 1	Input

5

V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, V_{4R}: V_1 to V_4 supply power for driving an LCD (figure 1).

Control Signal

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_7: D_0-D_7 input display data for the column driver (table 2).

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{E}$ connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

Table 2 Relation between Display data and LCD state

Display Data	LCD Output	LCD
1 (=high level)	V1L, R/V2L, R	On
0 (=low level)	Nonselected level	Off

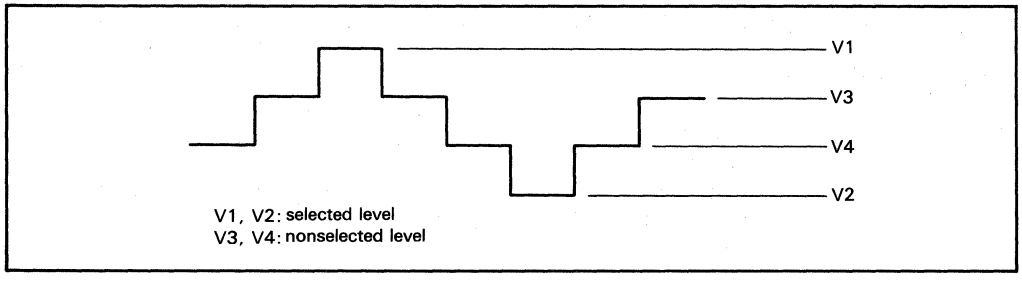


Figure 1 Power Supply for Driving an LCD

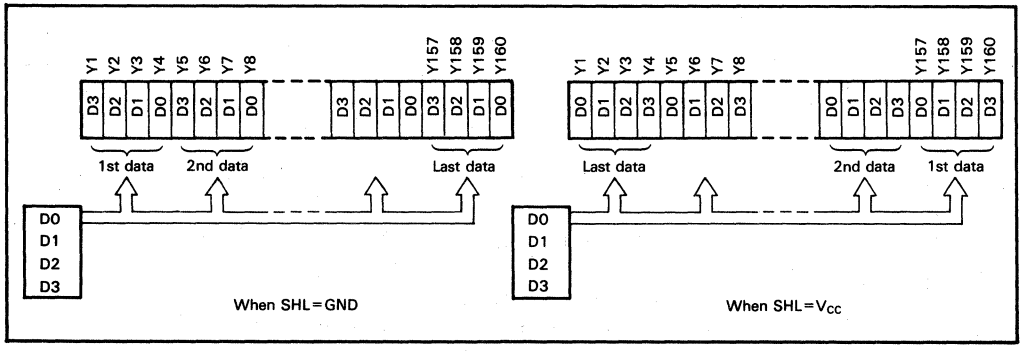


Figure 2 Relation between SHL and Data Output

$\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1=GND). When HD66107Ts are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip devices are columns when CH1 = V_{CC}, and commons when CH1 = GND.

CH2: CH2 selects the number of output data bits. The number of output data bits is 160 when CH2 = GND, and 80 when CH2 = V_{CC}.

BS: BS selects the number of input data bits. When BS = V_{CC}, the chip latches 8-bits data. When BS = GND, the chip latches 4-bits data via D_0 to D_3. Fix D_4 through D_7 to GND.

TEST: Used for testing. Fixed to GND, other wise.

LCD Drive Interface

Y1-Y160: Each Y outputs one of the four voltage levels-V_1, V_2, V_3, V_4-according to the combination of M and display data (figure 3).

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI is Used as Common Driver)

SHL	Shift Direction of Shift Register	Scan Direction of Selected Line
V_{CC}	E→ 1→ 2→ 3→ 4– – – – – – – →160	Y1→ Y2→ Y3→ Y4– – – – – – –→Y160
GND	E→ 160→ 159→ 158→ 157– – – – – – – →1	Y160→ Y159→ Y158→ Y157– – – – – – –→Y1

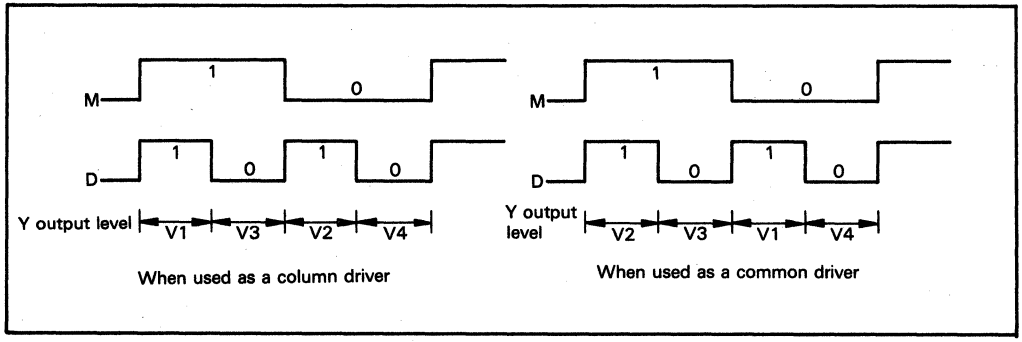
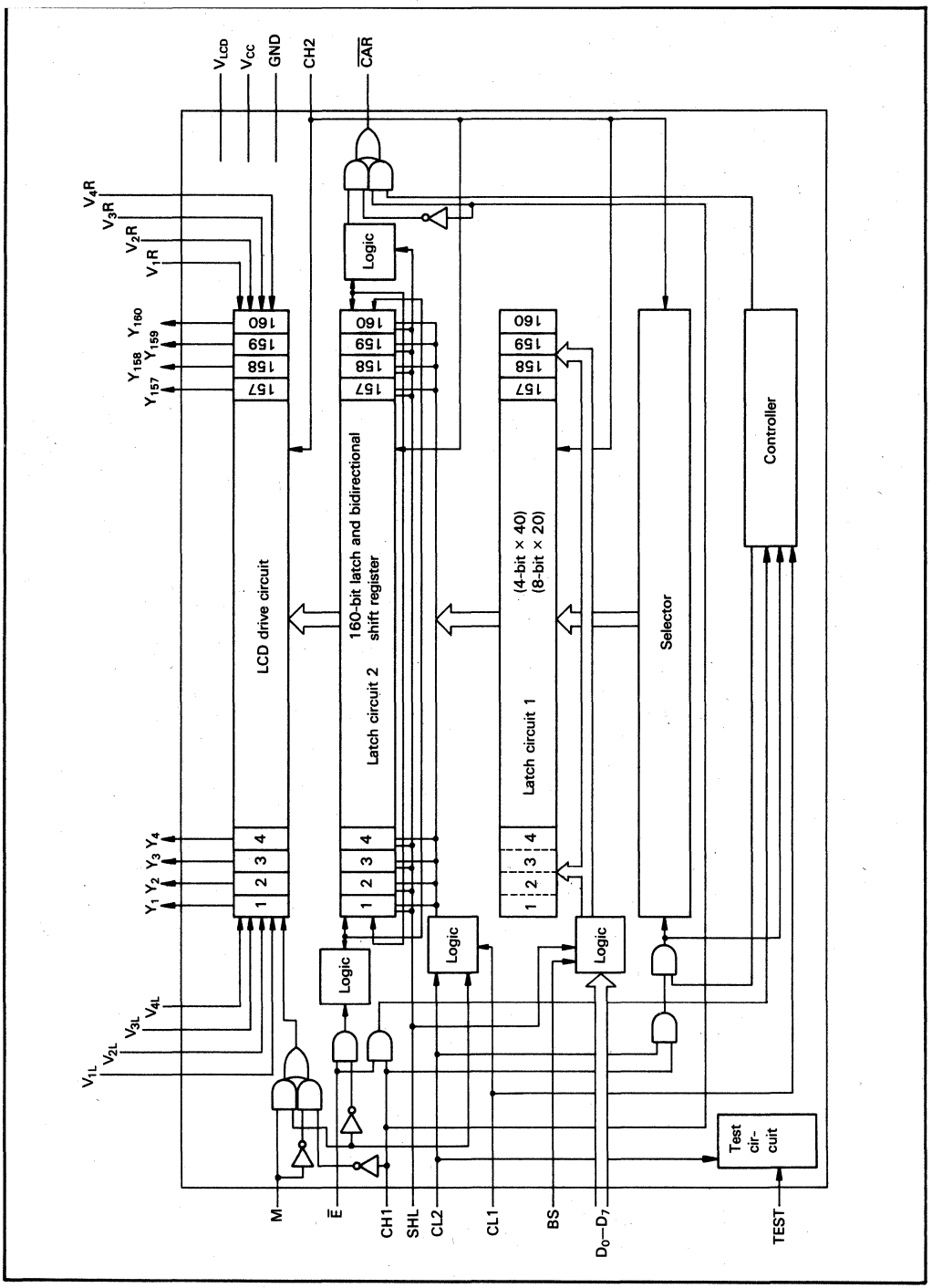


Figure 3 Selection of LCD Driver Output Level

5

Block Diagram



Function

LCD Drive Circuits

The LCD drive circuits generate four levels of voltages-V_1, V_2, V_3, and V_4-for driving an LCD. They select and transfer one of the four levels to the output circuit according to the combination of M and the data in the latch circuit 2.

Latch Circuit 2

Latch circuit 2 is used as a 160-bit latch circuit during column driving. Latch circuit 2 latches data input from latch circuit 1 at the falling edge of CL1 and outputs latched data to the drive circuits.

In the case of row driving, latch circuit 2 is used as a 160-bit bidirectional shift register. Data input from $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted in input order from bit 1 to bit 160 of the shift register. When SHL = GND, data is shifted from bit 160 to bit 1 of the reister. Moreover, this latch circuit can be used as an 80-bit shift register. In this case, Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Latch Circuit 1

Latch circuit 1 consists of twenty 8-bit parallel data latch circuits. It latches data D_0 through D_7 at the falling edge of CL2 during column driving. The selector signals specify which 8-bit circuit latches data. Moreover, this circuit can be used as forty 4-bit parallel data latch circuits by switching BS, in which case the circuit latches data D_0 through D_3. Moreover, this latch circuit can be used as an 80-bit shift register. In this case Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Selector

The selector consists of a 6-bit up and down counter and a decoder. During column driving it generates a latch signal for latch circuit 1, incrementing the counter at the falling edge of CL2.

Controller

This controller is enabled during column driving. It provides a power-down function which detects completion of data latch and stops LSI operations.

Moreover, the controller automatically generates a chip enable signal ($\overline{CAR}$) which starts next-stage data latching.

Test Circuit

The test circuit divides the external clock and generates test signals.

5

Fundamental Operations

Column Driving (1)

- CH2 = GND (160-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

The HD66107T starts data latch when $\overline{E}$ is at low level. In this case, 8-bit parallel data is latched at the falling edge of CL2. When 160-bit data latch is completed, the HD66107T automatically stops and enters standby mode and $\overline{CAR}$ is goes to low level. If $\overline{CAR}$ is connected with $\overline{E}$ of the next-stage LSI, this next-stage LSI is activated when $\overline{CAR}$ of the previous LSI goes low.

Data is output at the falling edge of CL1. When SHL = GND, data d_1 is output to pin Y1 and d_{160} to Y_{160}. On the other hand, when SHL = V_{CC}, data d_{160} is output to pin Y1 and d1 to Y_{160}. The output level is selected from among V_1-V_4 according to the combination of display data and alternating signal M. See figure 4.

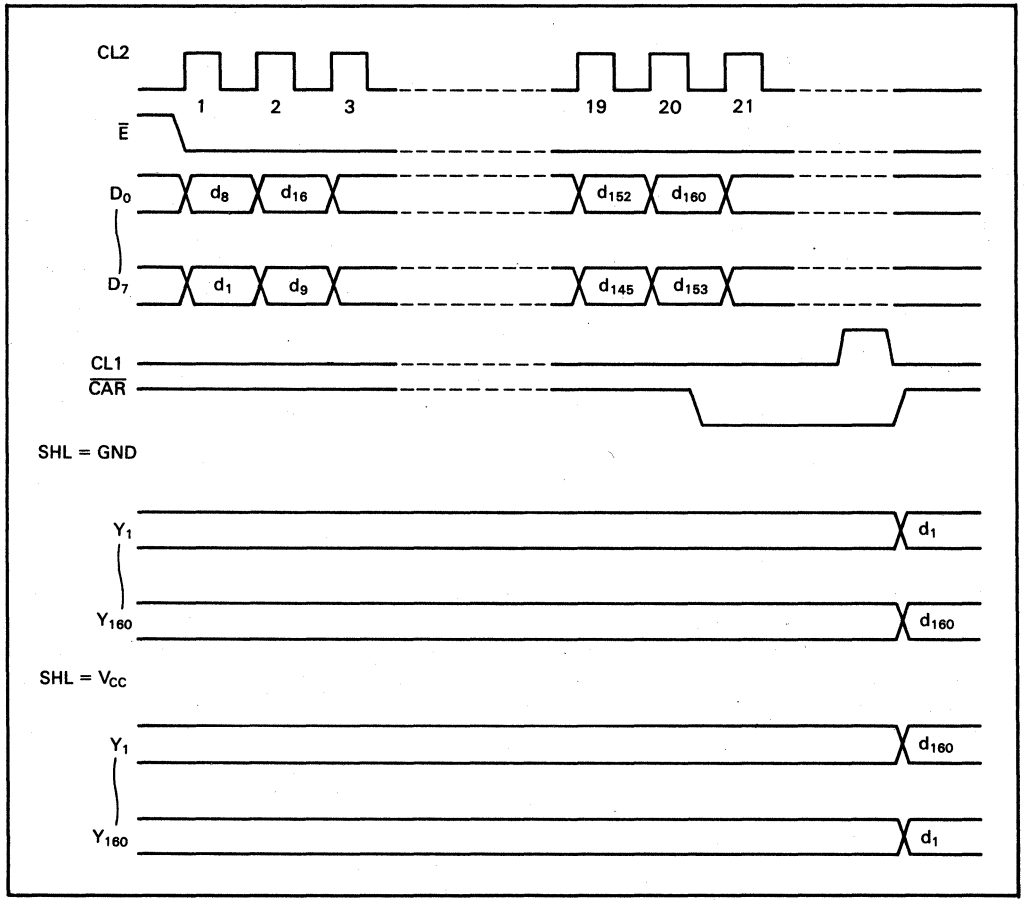


Figure 4 Column Driver Timing Chart (1)

Column Driving (2)

- CH2 = GND (160-bit data output mode)
- BS = GND (4-bit data latch mode)

4-bit display data (D_0-D_3) is latched at the falling edge of CL2. Other operations are performed in the same way as described in "Column Driving (1)". See figure 5.

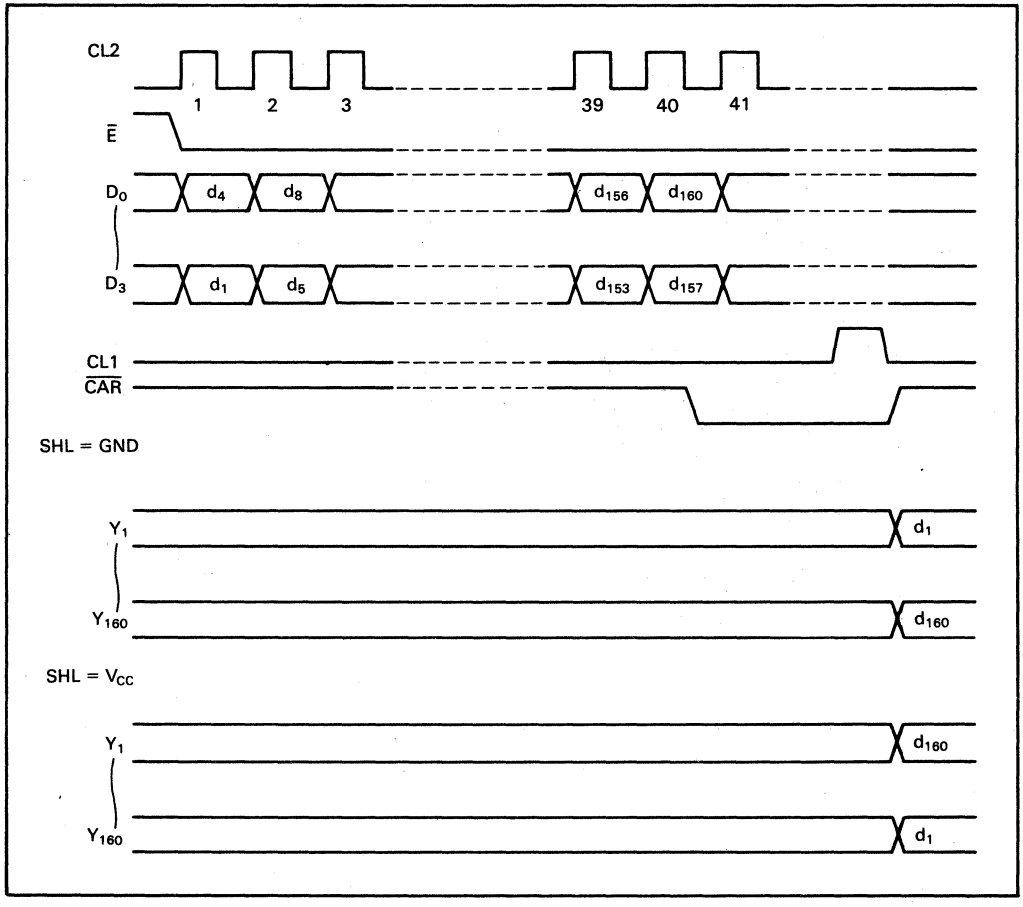


Figure 5 Column Driver Timing Chart (2)

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Column Driving (3)

- CH2 = V_{CC} (80-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

When CH2 is high (V_{CC}), the HD66107T can be used as an 80-bit column driver. In this case, Y_{41} through Y_{120} are enabled, the states of Y_1 through Y_{40} and Y_{121} through Y_{160} remain uncnanged.

When SHL = GND, data d1 is output to pin Y_{41} and d_{80} is output to Y_{120}. Conversely, when SHL = V_{CC}, data d_{80} is output to Y_{41} and d_1 is output to Y_{120}. See figure 6.

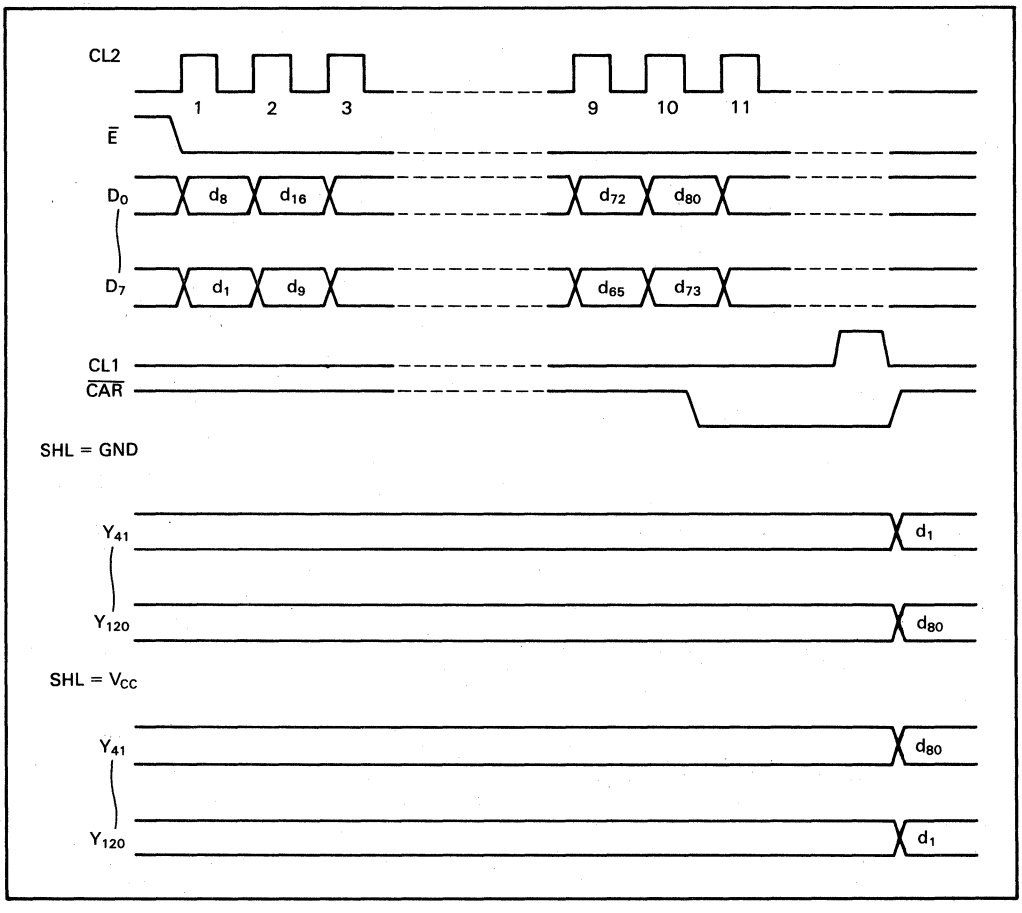

Figure 6 Column Driver Timing Chart (3)

Column Driving (4)

- CH2 = V_{CC} (80-bit data output mode)
- BS = GND (4-bit data latch mode)

When CH2 = V_{CC} and BS = GND, 4-bit parallel data is latched, while 80-bit data is output. The output of latched data is performed in described in "Column Driving (3)". See figure 7.

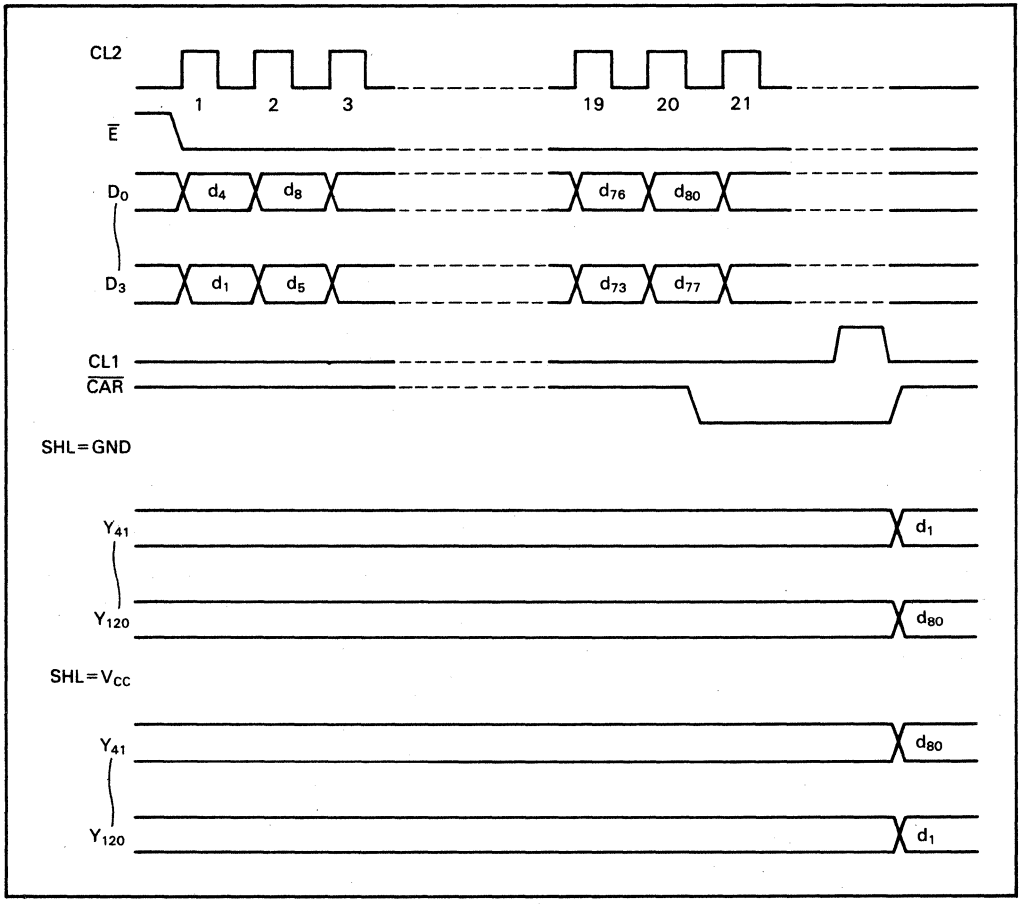

Figure 7 Column Driver Timing Chart (4)

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Common Driving (1)

· CH2 = GND (160-bit data output mode)

The HD66107T shifts line scan data input through $\overline{E}$ at the falling edge of CL2.

When SHL = V_{CC}, 160-bit data is shifted from Y_1 to Y_{160}, whereas when SHL = GND, data is shifted from Y_{160} to Y_1. In both cases the HD66107T outputs the data delayed for 160 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next IC driver. See figure 8.

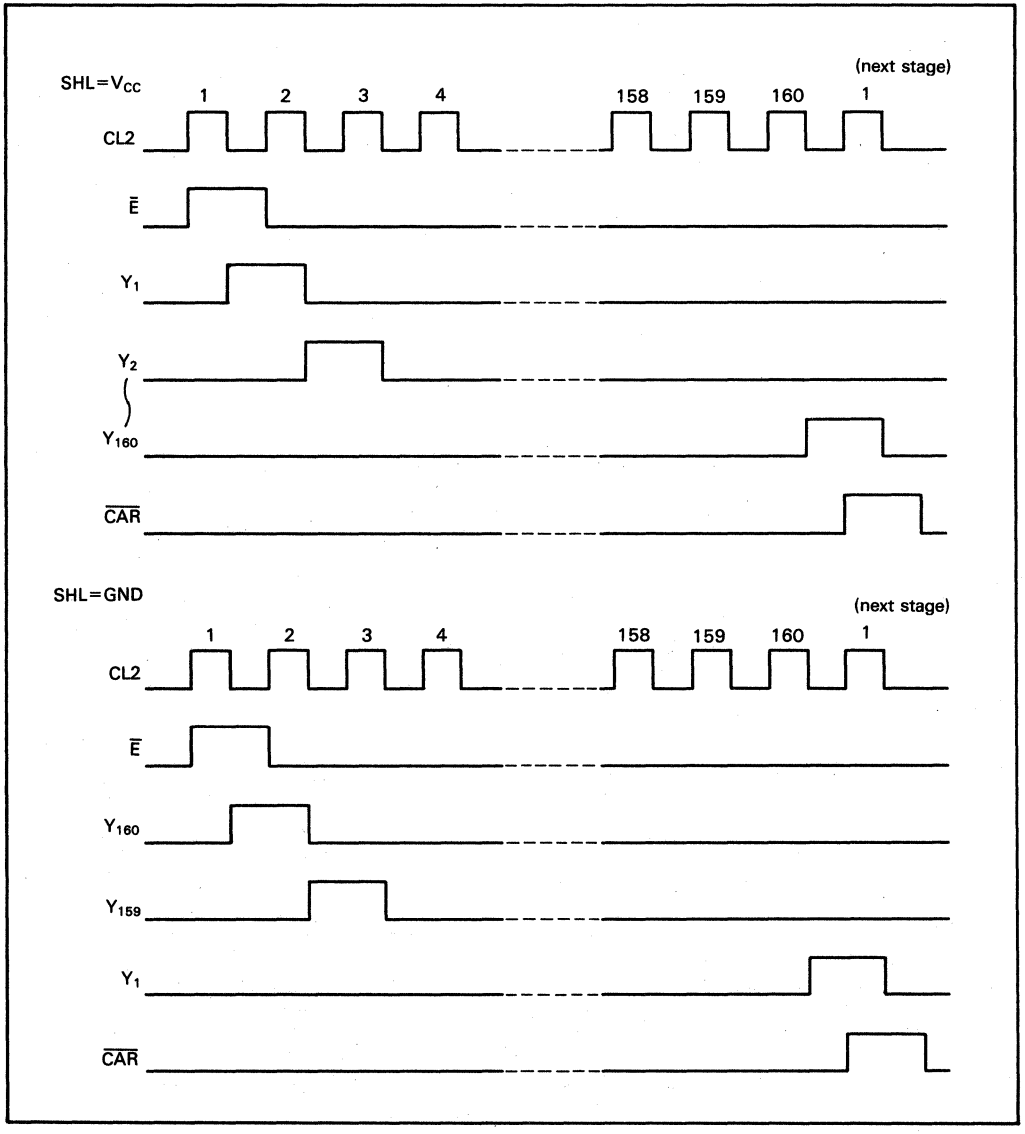


Figure 8 Common Driver Timing Chart (1)

Common Driving (2)

· CH2 = V_{CC} (80-bit data output mode)

When CH2 is high, the HD66107T can be used as an 80-bit row driver. In this case, Y_{41} to Y_{120} are enabled, while the other bits remain unchanged.

Line scan data input through $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted from Y_{41} to Y_{120}. Conversely, when SHL = GND, data is shifted from Y_{120} to Y_{41}. In both cases the HD66107T outputs the data delayed for 80 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next LSI. See figure 9.

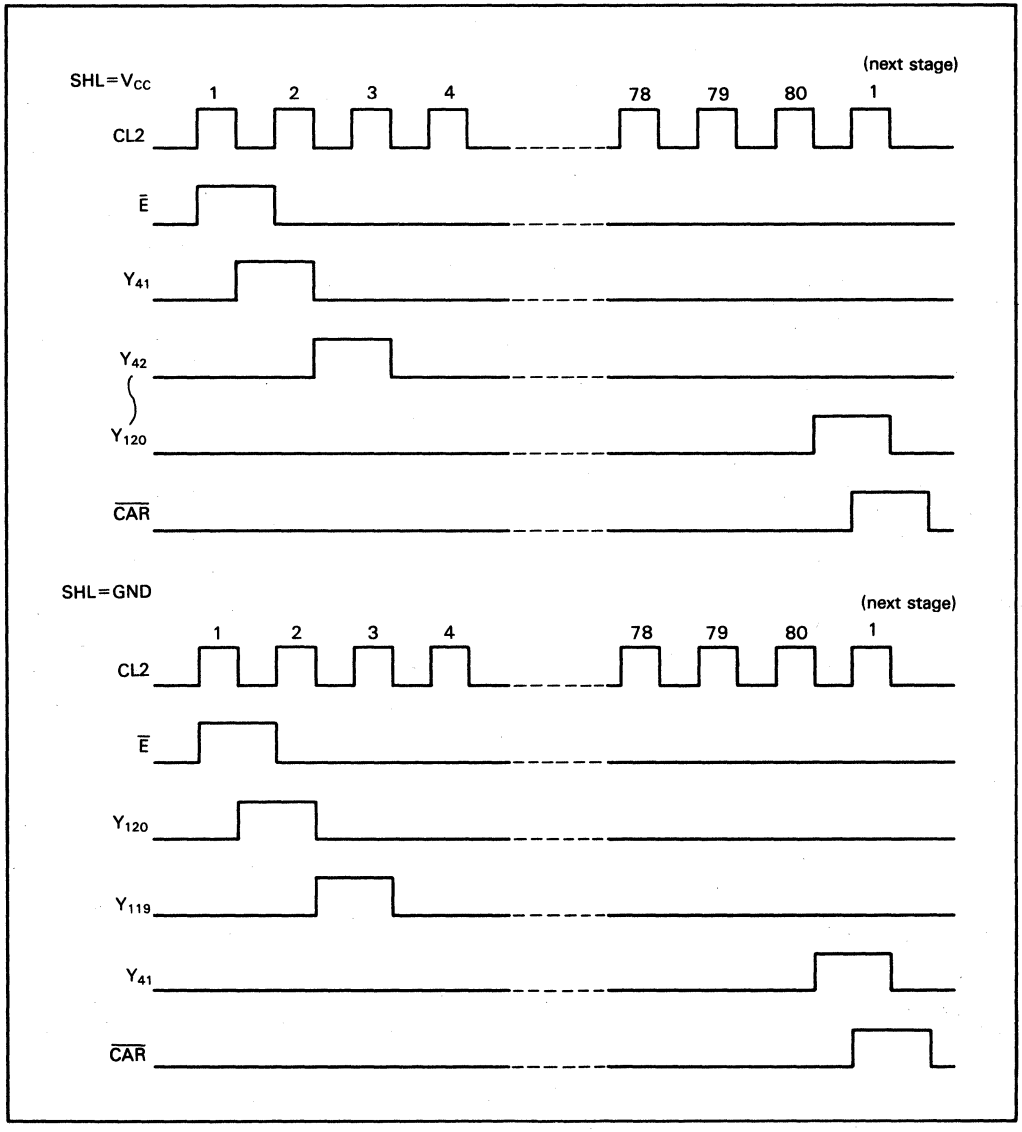


Figure 9 Common Driver Timing Chart (2)

5

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LDC}, and V_2 and V_4 should be near GND (figure 10). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 11).

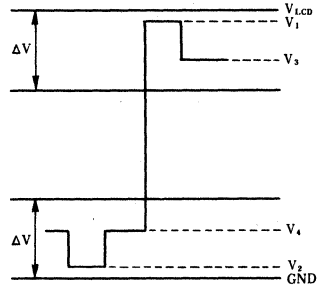


Figure 10 Driver's Output Waveform and Each Level of Voltage

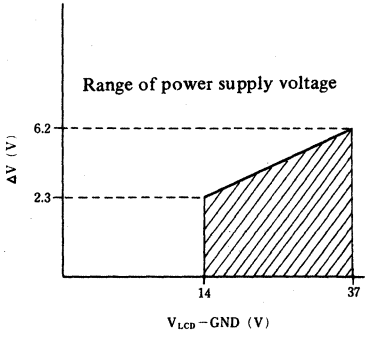
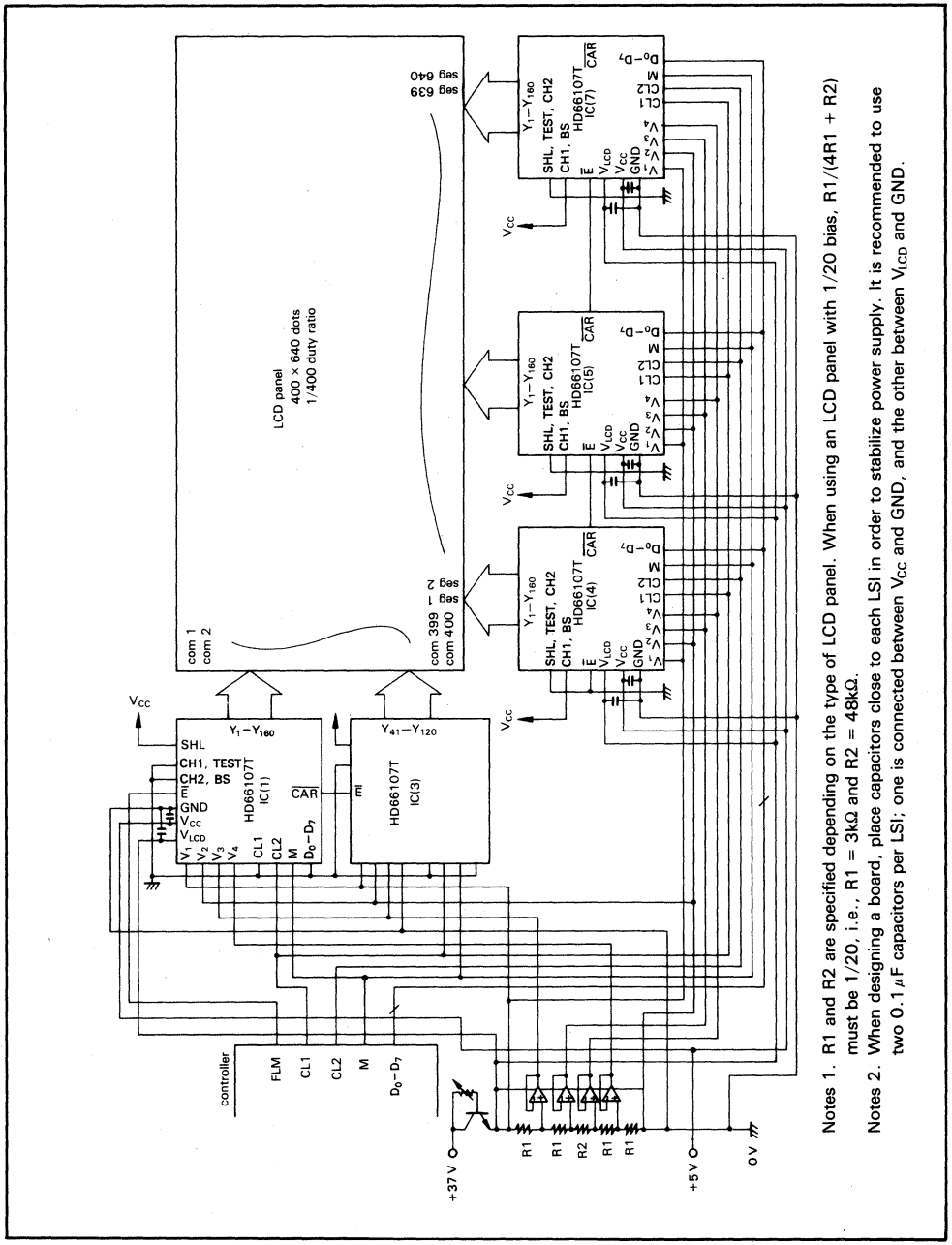


Figure 11 Power Supply Voltage V_{LCD}-GND and ΔV

Application

The following example shows a system configuration for driving a 640×400-dot LCD panel using the HD66107T.



Notes 1. R1 and R2 are specified depending on the type of LCD panel. When using an LCD panel with 1/20 bias, R1/(4R1 + R2) must be 1/20, i.e., R1 = 3kΩ and R2 = 48kΩ.

Notes 2. When designing a board, place capacitors close to each LSI in order to stabilize power supply. It is recommended to use two 0.1 μF capacitors per LSI; one is connected between V_{CC} and GND, and the other between V_{LCD} and GND.

Figure 12 Application Example

5

Waveform Examples

Column Driving

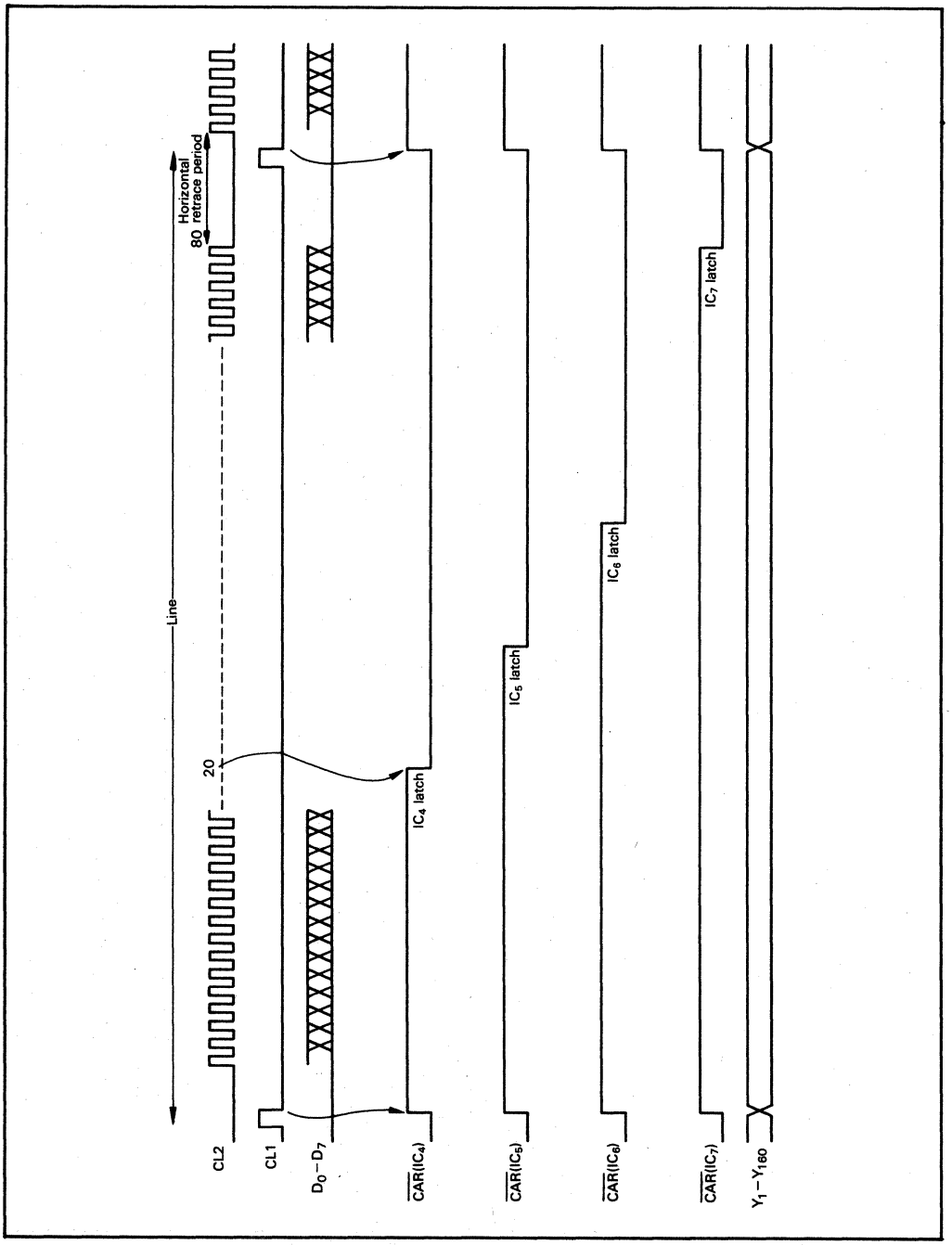


Figure 13 Column Driver Timing Chart (1)

Common Driving

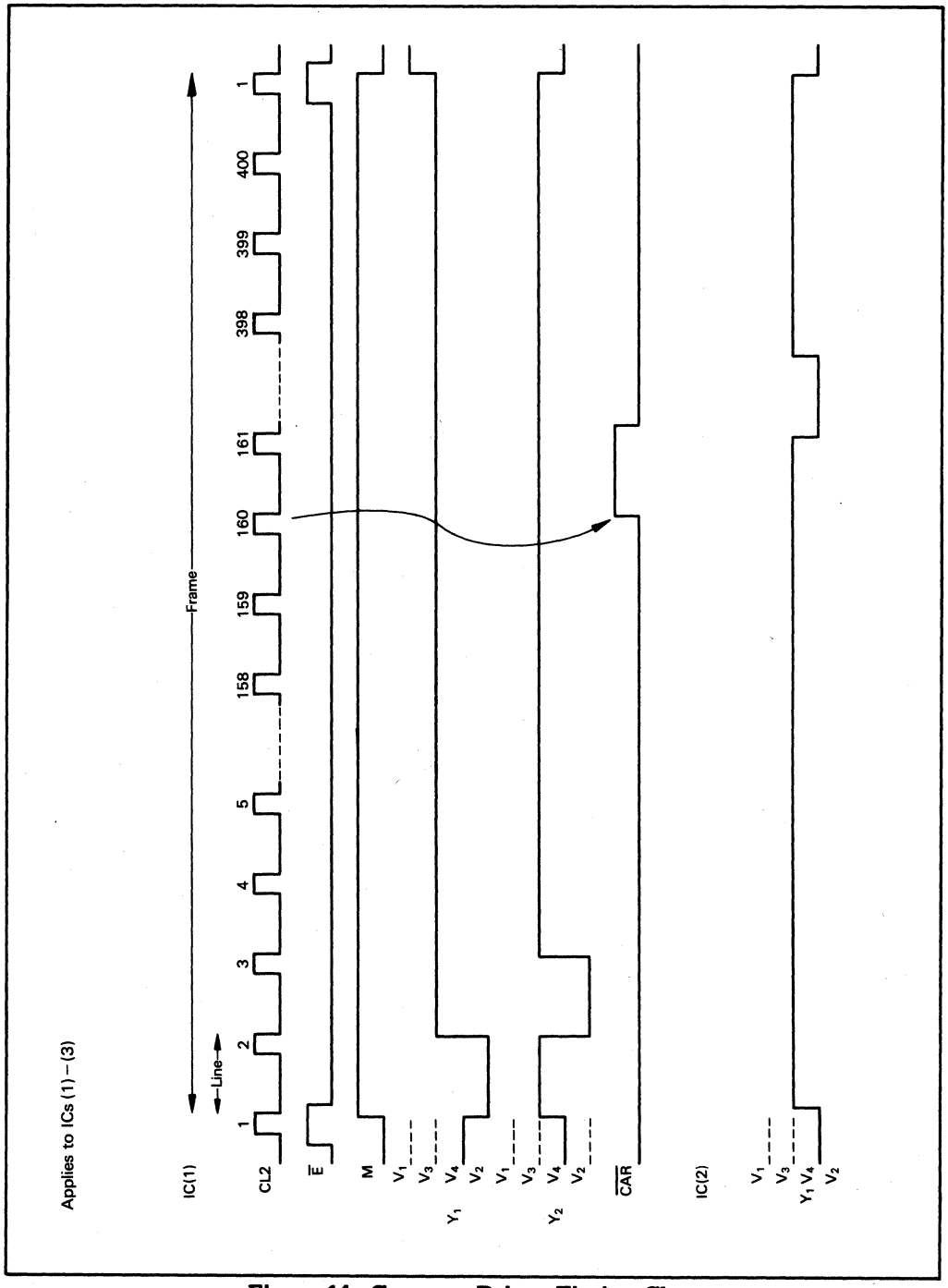


Figure 14 Common Driver Timing Chart

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Absolute Maximum Rating

Item		Symbol	Rating	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	−0.3 − +7.0	V	1
	LCD drive circuit	V_{LCD}	−0.5 − +38	V	1
Input voltage (1)		V_{T1}	−0.3 − V_{CC} + 0.3	V	1, 2
Input voltage (2)		V_{T2}	−0.3 − V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	−20 − +75	°C	
Storage temperature		T_{stg}	−55 − +125	°C	

Notes: 1. Reference point is GND (= 0V).
2. Applies to input pins for logic circuit.
3. Applies to input pins for LCD drive circuits.
4. If the LSI is used beyond absolute maximum ratings, it may be permanently damaged. It should always be used within the above electrical characteristics to prevent malfunction or degradation of the LSI's reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 to 37 V, Ta = −20 to 75°C)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	CL1, CL2, M SHL, BS, CH2,	0.8 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	TEST, D_0-D_7, $\overline{E}$, CH1	0	0.2 × V_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC}−0.4	−	V	I_{OH}=−0.4 mA	
Output low voltage	V_{OL}		−	0.4	V	I_{OL}=0.4 mA	
Vi−Yj on resistance	R_{ON}	Y1−Y160, V1−V4	−	3.0	kΩ	I_{ON}=150 μA	
Input leak current (1)	I_{IL1}	CL1, CL2, M SHL, BS, CH2, TEST, D_0−D_7, $\overline{E}$, CH1	−5.0	5.0	μA	V_{IN}=V_{CC}−GND	
Input leak current (2)	I_{IL2}	V1−V4	−100	100	μA	V_{IN}=V_{LCD}−GND	
Power dissipation (1)	I_{CC1}		−	5.0	mA	f_{CL2}=8 MHz	1
Power dissipation (2)	I_{LCD1}		−	2.0	mA	f_{CL1}=28 kHz	2
Power dissipation (3)	I_{ST}		−	0.5	mA	In standby mode: f_{CL2}=8 MHz, f_{CL1}=28 kHz	1 2
Power dissipation (4)	I_{CC2}		−	1.0	mA	f_{fcL1}=28 kHz	1
Power dissipation (5)	I_{LCD2}		−	0.5	mA	fm=35 Hz	3

Notes: 1. Input and output current is excluded. When an input is at the intermediate level is CMOS, excessive current flows from the power supply though the input circuit. To avoid it, V_{IH} and V_{IL} must be fixed to V_{CC} and GND respectively.
2. Applies to column driving.
3. Applies to row driving.

5

AC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 to 37 V, Ta = −20 to 75°C)

Column Driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock cycle time	t_{cyc}	CL2	125	–	ns	
Clock high-level width	t_{CWH}	CL2	30	–	ns	
Clock low-level width	t_{CWL}	CL2	30	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	ns	
Clock rising/falling time	tct	CL1, CL2	–	30	ns	
Data setup time	t_{DSU}	D_0–D_7	30	–	ns	
Data hold time	t_{DH}	D_0–D_7	30	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	25	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	70	ns	1
M phase difference	t_{CM}	M, CL1	–	300	ns	

Notes: 1. Specified when connecting the load circuit shown in figure 15.

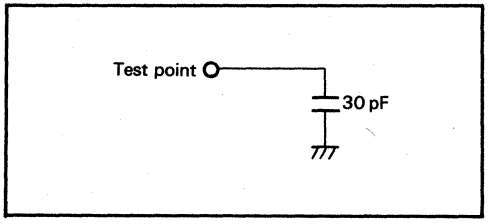

Figure 15 Test Circuit

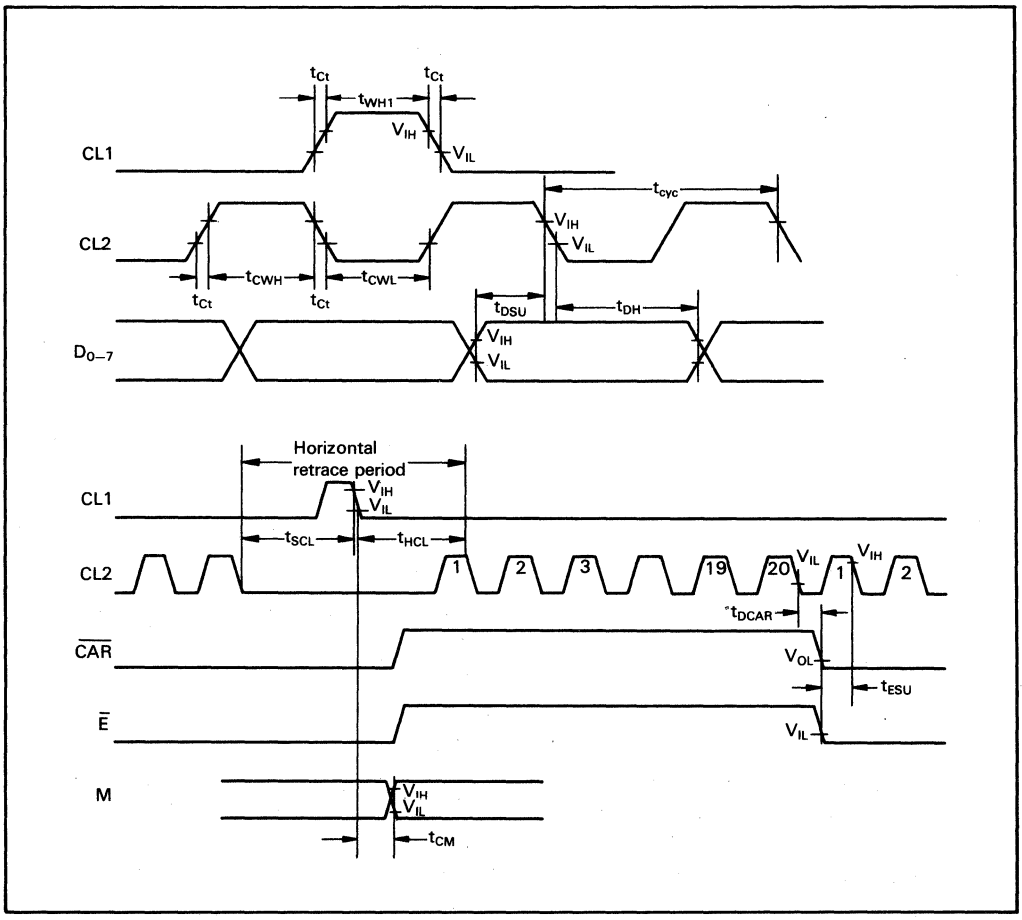

Figure 16 Controller Interface of Column Driver

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Common Driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock low-level width	t_{WL1}	CL2	5	–	μs	
Clock high-level width	t_{WH1}	CL2	60	–	ns	
Data setup time	t_{DS}	$\overline{E}$	100	–	ns	
Data hold time	t_{DH}	$\overline{E}$	30	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	3	μs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	ns	1
Clock rising/falling time	t_{Ct}	CL2	–	30	ns	

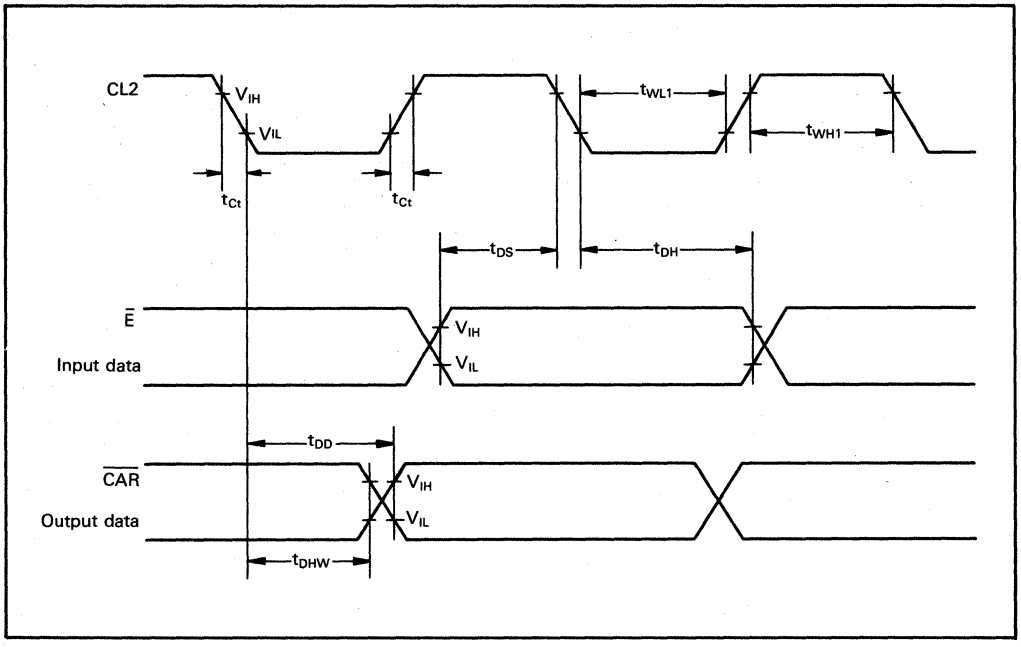


Figure 17 Controller Interface of Common Driver

HD66108T
(RAM-Provided 165-Channel LCD Driver for Liquid-Crystal Dot Matrix Graphics)

Description

The HD66108T under control of an 8-bit MPU can drive a dot matrix graphic LCD (liquid-crystal display) employing bit-mapped display with support of an 8-bit MPU.

Use of the HD66108T enables a simple LCD system to be configured with only a small number of chips, since it has all the functions required for driving the display.

The HD66108T also enables highly-flexible display selection due to the bit-mapped method, in which one bit of data in a display RAM turns one dot of an LCD panel on or off. A single HD66108T can display a maximum of 100 × 65 dots by using its on-chip 165 × 65-bit RAM. Also, by using several HD66108T's, a display can be further expanded.

The HD66108T employs the CMOS process and TAB package. Thus, if used together with an MPU, it can provide the means for a battery-driven pocket-size graphic display device utilizing the low current consumption of LCDs.

Features

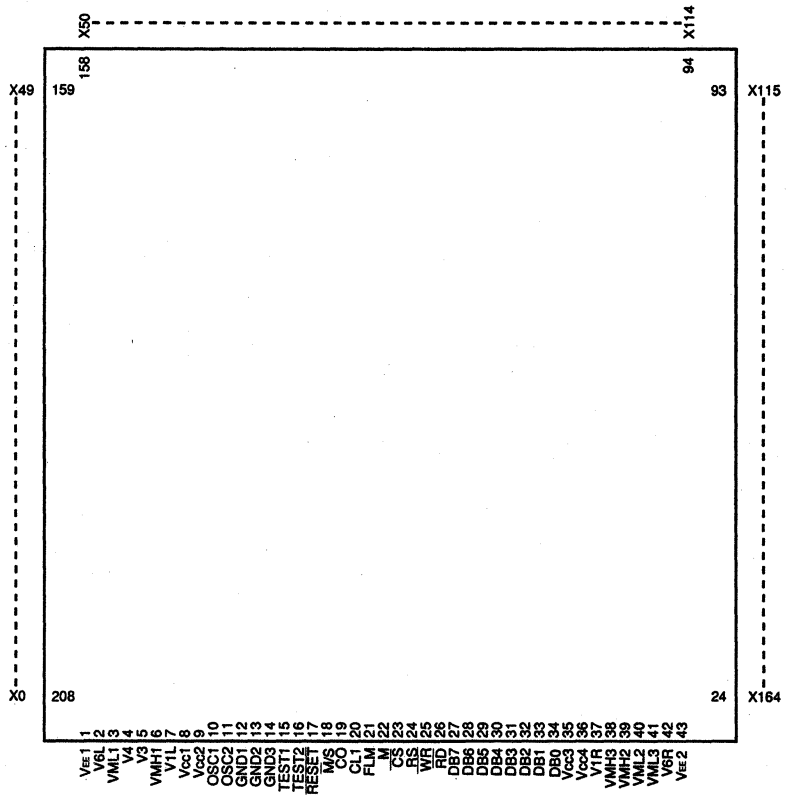
- Four types of LCD driving circuit configurations can be selected:

Configuration Type	No. of Column Outputs	No. of Row Outputs
Column outputs only	165	0
Row outputs from the left and right sides	100	65 (from left: 32, from right: 33)
Row outputs from the right side 1	100	65
Row outputs from the right side 2	132	33

- Seven types of multiplexing duty ratios can be selected: 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, 1/66
  Notes: The maximum number of row outputs is 65.
- Built-in bit-mapped display RAM: 10 kbits (165 × 65 bits)
- The word length of display data can be selected according to the character font: 8-bit or 6-bit
- A standby operation is available
- The display can be extended through a multi-chip operation
- A built-in CR oscillator
- An 80-system CPU interface: Φ = 4 MHz
- Power supply voltage for operation: 2.7 V to 6.0 V
- LCD driving voltage: 6.0 V to 15.0 V
- Low current consumption: 400 µA max (at f_{osc} = 500 kHz, f_{osc} is external clock frequency)
- Package: 208-pin TCP (Tape-Carrier Package)

5

Chip terminals



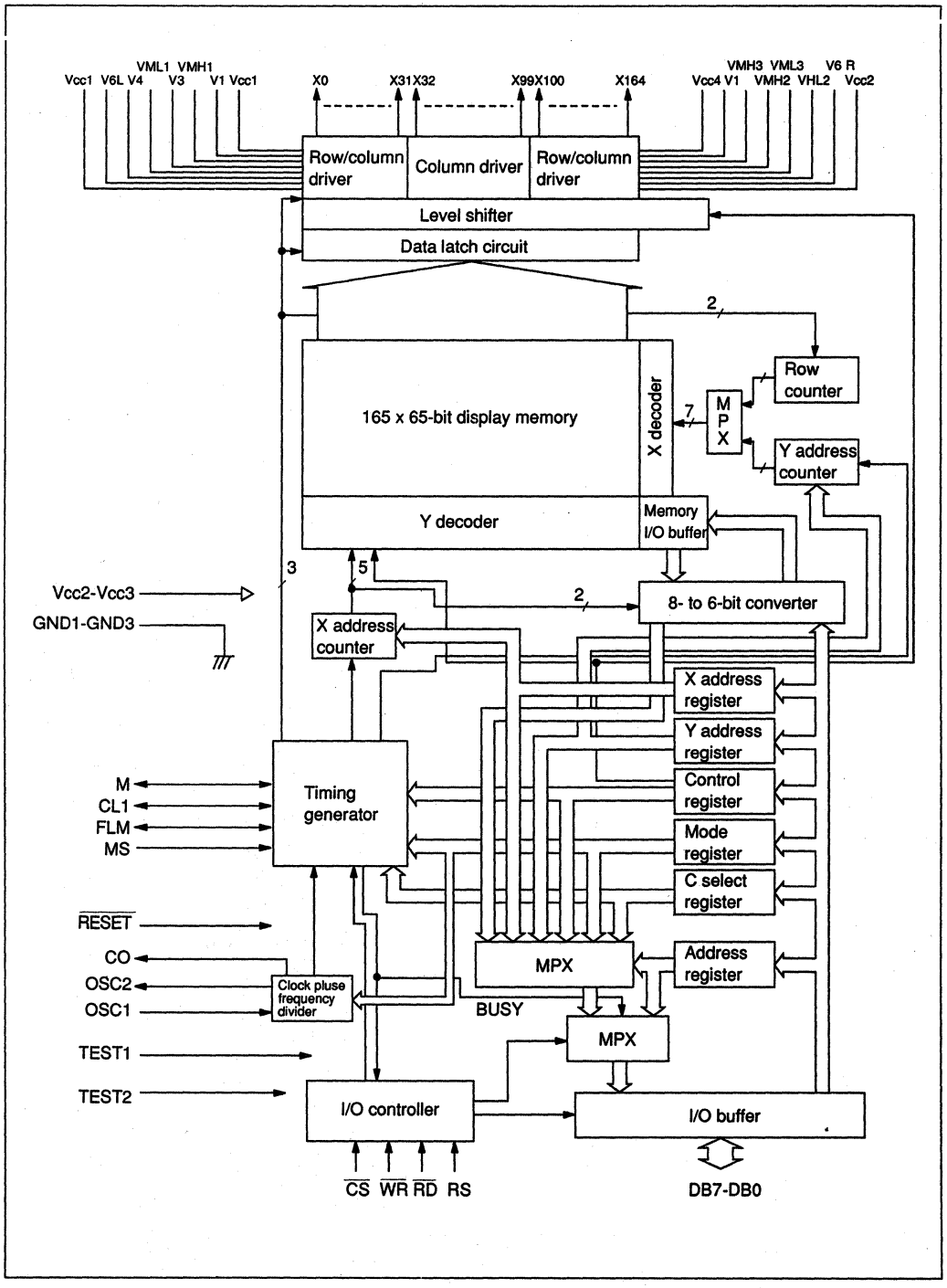
Note: The above view is seen from the grinded surface of the chip, not TCP.

Pin Description

Classification	No. of Pins	Symbol	I/O	No. of Pins	Function
Power Supply	8, 9, 35, 36	$V_{CC}1$–$V_{CC}4$	–	4	Connect these pins to V_{CC}.
	12 ~ 14	GND1–GND3	–	3	Ground these pins.
	1, 43	$V_{EE}1$, $V_{EE}2$	–	2	These pins supply power to the LCD driving circuits and should usually be set to the V6 level.
	2, 7 37, 42 4, 5 6, 39, 38 3, 40, 41	V6L, V1L, V1R, V6R, V4, V3, VMH1–VMH3, VML1–VML3	–	12	Apply an LCD driving voltage V1 to V6 to these pins.
CPU Interface	23	$\overline{CS}$	I	1	Input a chip select signal via this pin. A CPU can access the HD66108T's internal registers only while the $\overline{CS}$ signal is low.
	25	$\overline{WR}$	I	1	Input a write enable signal via this pin.
	26	$\overline{RD}$	I	1	Input a read enable signal via this pin.
	24	RS	I	1	Input a register select signal via this pin.
	27~34	DB0–DB7	I/O	8	Data is transferred between the HD66108T and a CPU via these pins.
LCD Driving Output	44~208	X0–X164	O	165	These pins output LCD driving signals. The X0–X31 and X100–X164 pins are column /row common pins and output row driving signals when so programmed. X32–X99 pins are column pins.
LCD Interface	21	FLM	I/O	1	This pin outputs a first line marker when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.
	20	CL1	I/O	1	This pin outputs latch clock pulses of display data when the chip is a master chip and inputs clock CL1 pulses when the chip is a slave chip.
	22	M	I/O	1	This pin outputs or inputs an M signal, which converts LCD driving outputs to AC; it outputs the signal when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.
Control Signals	10	OSC1	I	1	Input system clock pulses via this pin.
	11	OSC2	O	1	This pin outputs clock pulses generated by the internal CR oscillator.
	19	CO	O	1	This pin outputs the same clock pulses as the system clock pulses, the OSC1 pin of a slave chip. Connect with the OSC1 pin of a slave chip.
	18	$\overline{M}$/S	I	1	This pin specifies master/slave. Set this pin low when the HD66108T is a master chip and set high when the chip is a slave chip; must not be changed after power-on.
	17	$\overline{RESET}$	I	1	Input a reset signal via this pin. Setting this pin low initializes the HD66108T.
	15, 16	TEST1, TEST2	I	2	These pins input a test signal and should usually be set low.

5

Internal Block Diagram



Register List

CS	RS	Reg. No. 2	1	0	Reg. Symbol	Register Name	Read/ Write	Data Bit Assignment 7	6	5	4	3	2	1	0	Busy time
1	–	–	–	–	–	Invalid	–									–
0	0	–	–	–	AR	Address	R	Busy	STBY	DISE			Register No.			None
							W									
0	1	0	0	0	DRAM	Display Memory	R	D7	D6	D5	D4	D3	D2	D1	D0	8 clocks max
							W									
0	1	0	0	1	XAR	X address	R				XAD					None
							W									1.5 clocks max
0	1	0	1	0	YAR	Y address	R		YAD							None
							W									1.5 clocks max
0	1	0	1	1	FCR	Control	R	INC	WLS	PON	ROS		DUTY			None
							W									
0	1	1	0	0	MDR	Mode	R				FFS			DWS		None
							W									
0	1	1	0	1	CSR	C select	R			EOR	CLN					None
							W									
0	1	1	1	0	–	Invalid	–									–
0	1	1	1	1	–	Invalid	–									–

Notes: 1. Shaded bits are invalid. Writing 1 or 0 to invalid bits does not affect LSI operation. Reading these bits returns 0.
2. DRAM is not actually a register but can be handled as one.
3. Setting the WLS bit of control register to 1 invalidates D7 and D6 bits of the display memory register.
4. DRAM must not be written to or read from until a time period of t_{CL1} has elapsed rewriting the DUTY bit of FCR or the FFS bit of MDR. t_{CL1} can be obtained from the following equation; in general, a time period of 1 ms or greater is sufficient if the frame frequency is 60–90 Hz.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}\,(kHz)}\,(ms) \text{ --- Equation 1}$$

D2 (duty correction value 2) : 192 (duty = 1/32, 1/34, or 1/36)
128 (duty = 1/48 or 1/50)
96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits)
: 2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8
Refer to "6. Clock and Frame Frequency."

f_{CLK} : Input clock frequency (kHz)

5

System Description

The HD66108T can assign a maximum of 65 out of 165 channels to row outputs for LCD driving . It also incorporates a timing generator and display memory, which are necessary to drive an LCD.

If connected to an MPU and supplied with LCD driving voltage, one HD66108T chip can be used to configure an LCD system with a 100 x 65 dot panel (figure 1). In this case, clock pulses should be supplied by the internal CR oscillator or the MPU.

Using LCD expansion signals $\overline{CL1}$, $\overline{FLM}$, and M enables the display size to be expanded. In this case, LCD expansion signal pins output corresponding signals when pin $\overline{M}/S$ is set low for master mode and conversely input corresponding signals when pin $\overline{M}/S$ is set high for slave mode; LCD expansion signal pins of both master chip and slave chips must be mutually connected. Figure 2 shows a basic system configuration using two HD66108T chips.

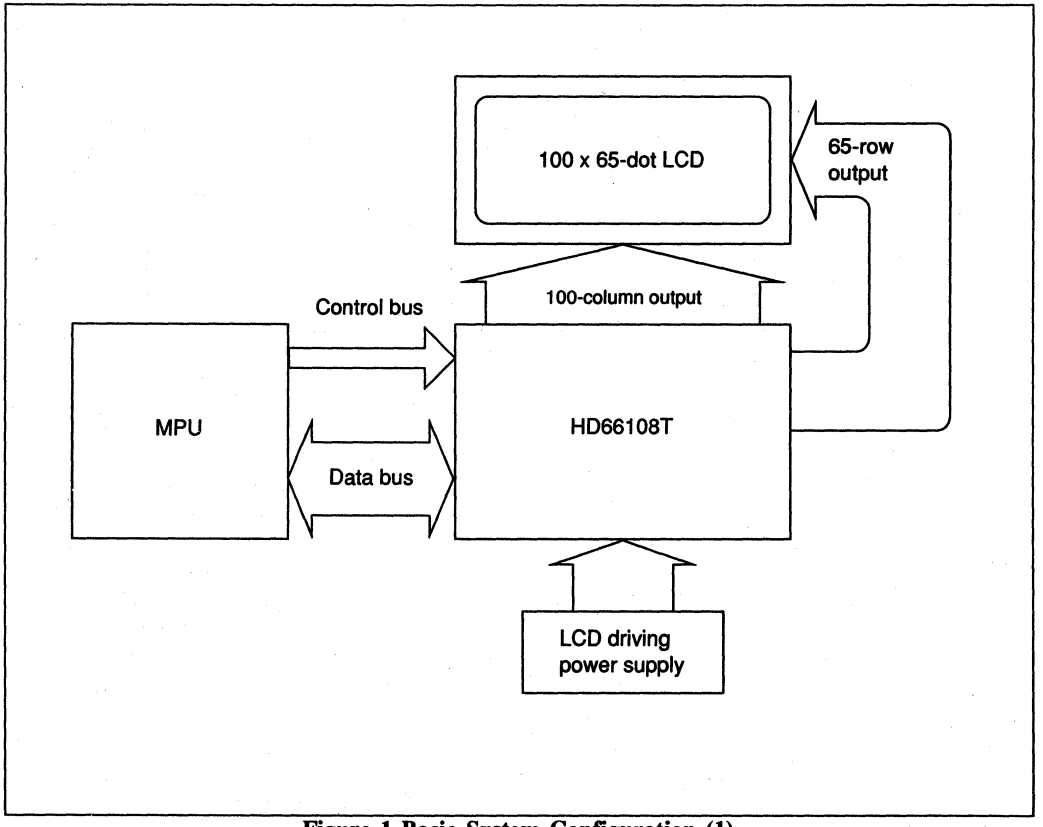


Figure 1 Basic System Configuration (1)

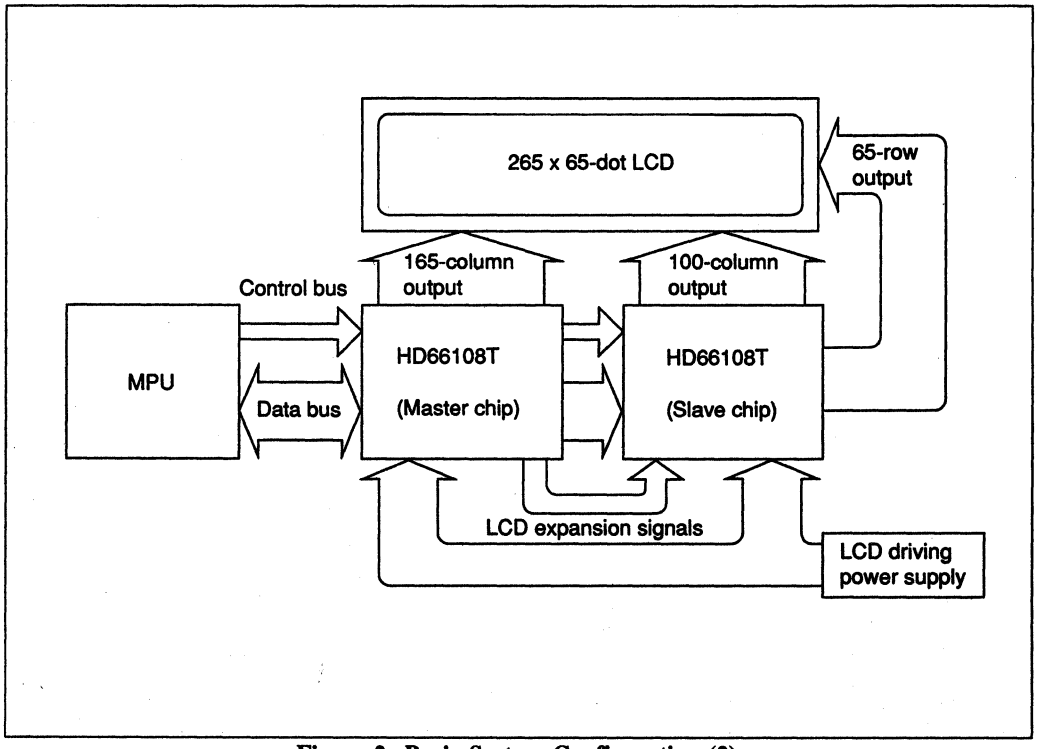


Figure 2 Basic System Configuration (2)

5

Functional Description

1. Display Size Programming

A variety of display sizes can be programmed by changing the system configuration and internal register settings.

(1) System Configuration Using 1 HD66108T Chip

When the 65-row-output mode is selected by internal register settings, a maximum of 100 dots in the X direction can be displayed (figure 3 (a)). Display size in the Y direction can be selected from 32 , 34, 36, 48, 50, 64 , and 65 dots according to display duty setting. Note that Y direction settings does not affect those in the X direction (100 dots).

When the 33-row-output mode is selected by internal register settings, a maximum of 132 dots in the X direction can be displayed (figure 3 (b)).

Table 1 shows the relationship between display sizes and the control register's (FCR) ROS and DUTY bits. ROS and DUTY bit settings determine the function of X pins. For more details, refer to " 4.1 Row Output Pin Selection."

(2) System Configuration Using 1 HD66108T Chip and 1 HD61203 Chip as Row Driver

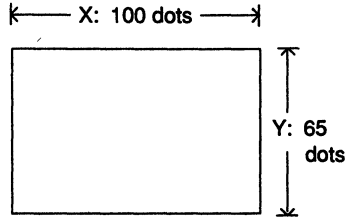
A maximum of 64 dots in the Y direction and 165 dots in the X direction can be displayed. 48 or 64 dots in the Y direction can be selected by HD61203 pin settings (figure 3 (c)).

(3) System Configuration Using 2 or more HD66108T Chips

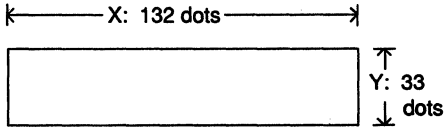
X direction size can be expanded by 165 dots per chip. Figure 3 (d) shows a 265 x 65-dot display. Y direction size can be expanded up to 130 dots with 2 chips; a 100 x 130-dot display provided by 2 chips is shown in figure 3 (e).

Table 1 Relationship between Display Size and Register Settings (No. of Dots)

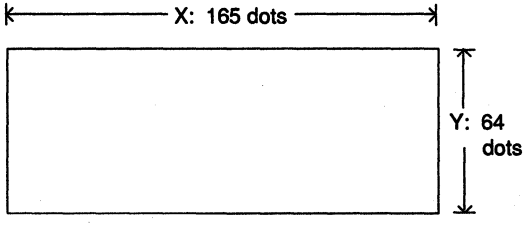
ROS Bit Setting (X0-X164 Pin Function)	Duty Bit Setting (Multiplexing Duty Ratio) 1/32	1/34	1/36	1/48	1/50	1/64	1/66
165-column-output	Specified by a row driver						
65-row-output from the right side	X: 100 Y: 32	X: 100 Y: 34	X: 100 Y: 36	X: 100 Y: 48	X: 100 Y: 50	X: 100 Y: 64	X: 100 Y: 65
65-row-output from the left and right sides	X: 100 Y: 32	X: 100 Y: 34	X: 100 Y: 36	X: 100 Y: 48	X:100 Y: 50	X: 100 Y: 64	X: 100 Y: 65
33-row-output from the right side	X: 132 Y: 32	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33



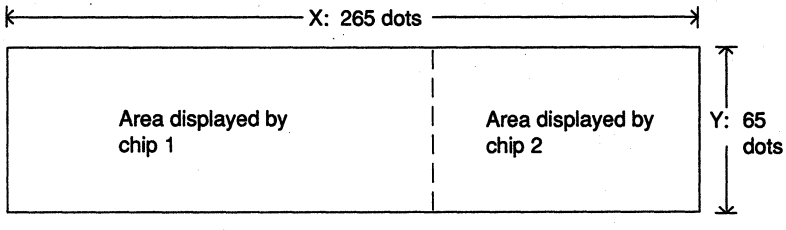
(a) Configuration Using 1 HD66108T Chip (1)
(65-Row Output from the Right Side)



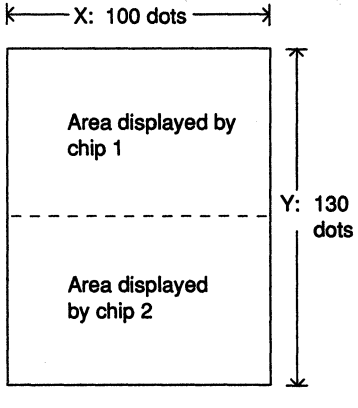
(b) Configuration Using 1 HD66108T Chip (2)
(33-Row Output from the Right Side)



(c) Configuration Using 1 HD66108T Chip and 1 HD61203 as Row Driver
(165-Column Output)



(d) Configuration Using 2 HD66108T Chips (1)



(e) Configuration Using 2 HD66108T Chips (2)

Figure 3 Relationship between System Configurations and Display Sizes

5

2. Display Memory Construction and Word Length Setting

The HD66108T has a bit-mapped display memory of 165 x 65 bits. As shown in figure 4, data from the MPU is stored in the display memory, with the MSB (most significant bit) on the left and the LSB (least significant bit) on the right.

The sections on the LCD panel corresponding to the display memory bits in which 1's are written will be displayed as on (black).

Display area size of the internal RAM is determined by control register (FCR) settings (refer to table 1).

The start address in the Y direction for the display area is always Y0, independent of the register setting. In contrast, the start address in the X direction is X0 in the modes for 165-column-output, 65 -row-output from the right side, and 33-row-output from the right side, and is X32 in the 65-row-output mode from the left and right sides.

Each display area contains the number of dots shown in table 1, beginning from each start address.

For more detail, refer to " 4.2 Row Output Data Setting, " figures 15 to 19.

In the display memory, one X address is assigned to each word of 8 or 6 bits long in X direction. (Either 8 or 6 bits can be selected as word length of display data.) Similarly, one Y address is assigned to each row in Y direction.

Accordingly, X address 20 in the case of 8-bit word and X address 27 in the case of 6-bit word have 5 and 3 bits of display data, respectively. Nevertheless, data is also stored here with the MSB on the left (figure 5).

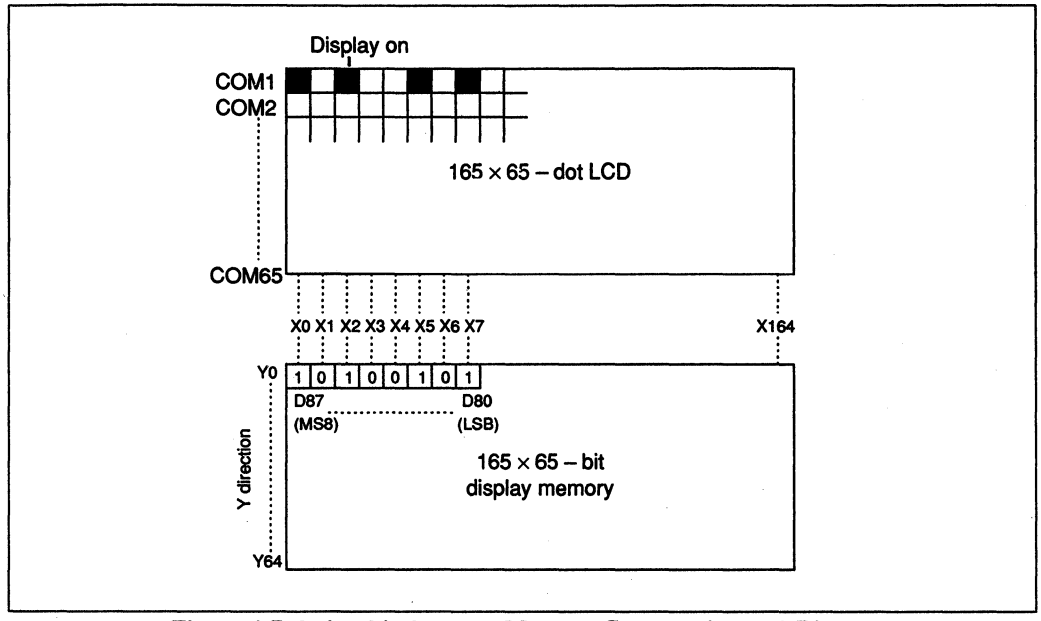


Figure 4 Relationship between Memory Construction and Display

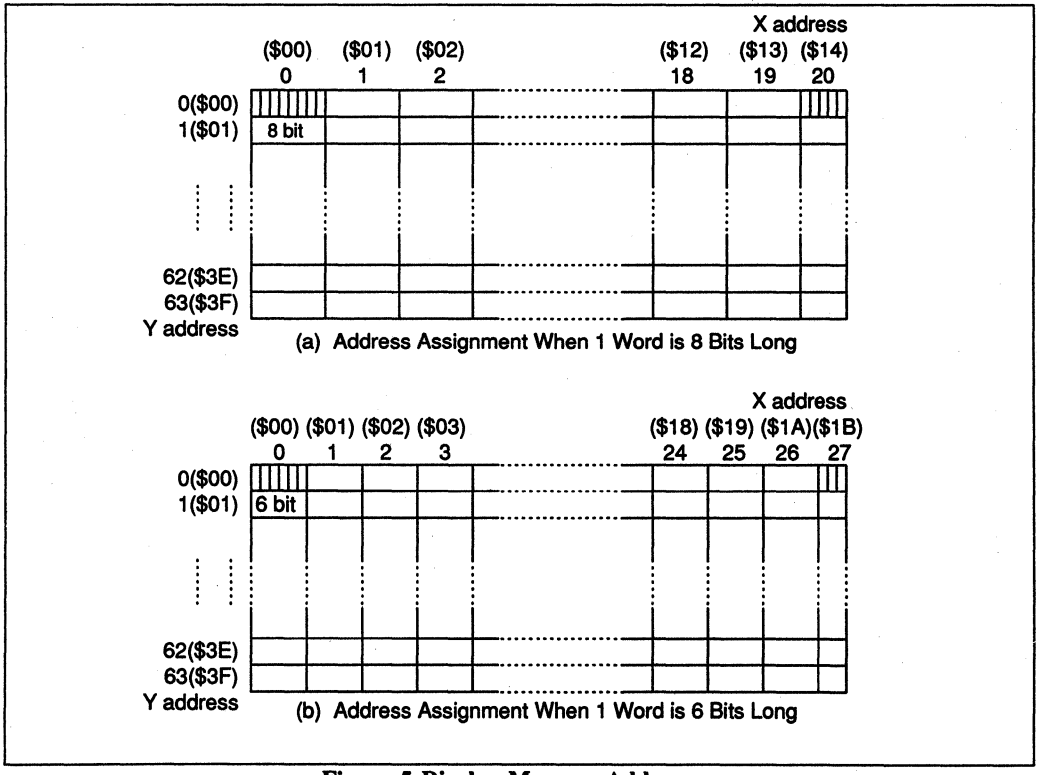


Figure 5 Display Memory Addresses

5

3. Display Data Write

3.1 Display Memory and Data Register Accesses

(1) Access

Figure 6 shows the relationship between the address register (AR) and internal registers and display memory in the HD66108T. Display memory shall be referred to as a data register since it can be handled as other registers.

To access a data register, the register address assigned to the desired register must be written into the address register's Register No.bits. The MPU will access only that register until the register address is updated.

(2) Busy Check

A busy time period appears after display memory read/write or X or Y address register write, since post-access processing is performed synchronously with internal clock pulses. Updating data in registers other than the address register is disabled during this time. Subsequent data must be input after confirming ready mode by reading the address register. The busy time period is a maximum of 8 clock pulses after display memory read/write and a maximum of 1.5 clock pulses after X or Y address register write (figure 7).

(3) Dummy Read

When reading out display data, the data which is read out immediately after setting the X and Y addresses is invalid. Valid data can be read out after one dummy read, which is performed after setting the X and Y addresses desired (figure 8).

(4) Limitations on Access

As shown in figure 9, the display memory must not be rewritten until a time period of t_{CL1} or longer has elapsed after rewriting the control register's DUTY bits or the mode register's FFS bits. However, display memory and registers other than the control register and mode register can be accessed even during this time period. t_{CL1} can be obtained from the following equation. If using an LSI with a frame frequency of 60 Hz or greater, a time period of 1 ms should be sufficient.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}\ (kHz)} \quad (ms) \quad \text{... Equation 1}$$

D2 (duty correction value 2) :

192 (duty = 1/32, 1/34, or 1/36)
128 (duty = 1/48 or 1/50)
96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits)

: 2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8

f_{CLK} : Input clock frequency (kHz)

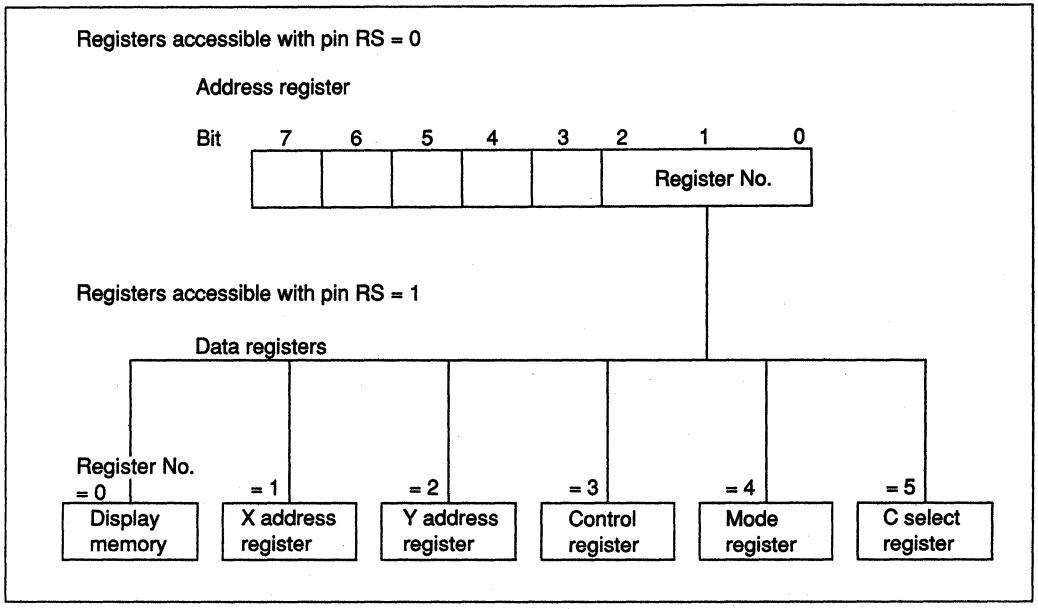


Figure 6 Relationship between Address Register and Register No.

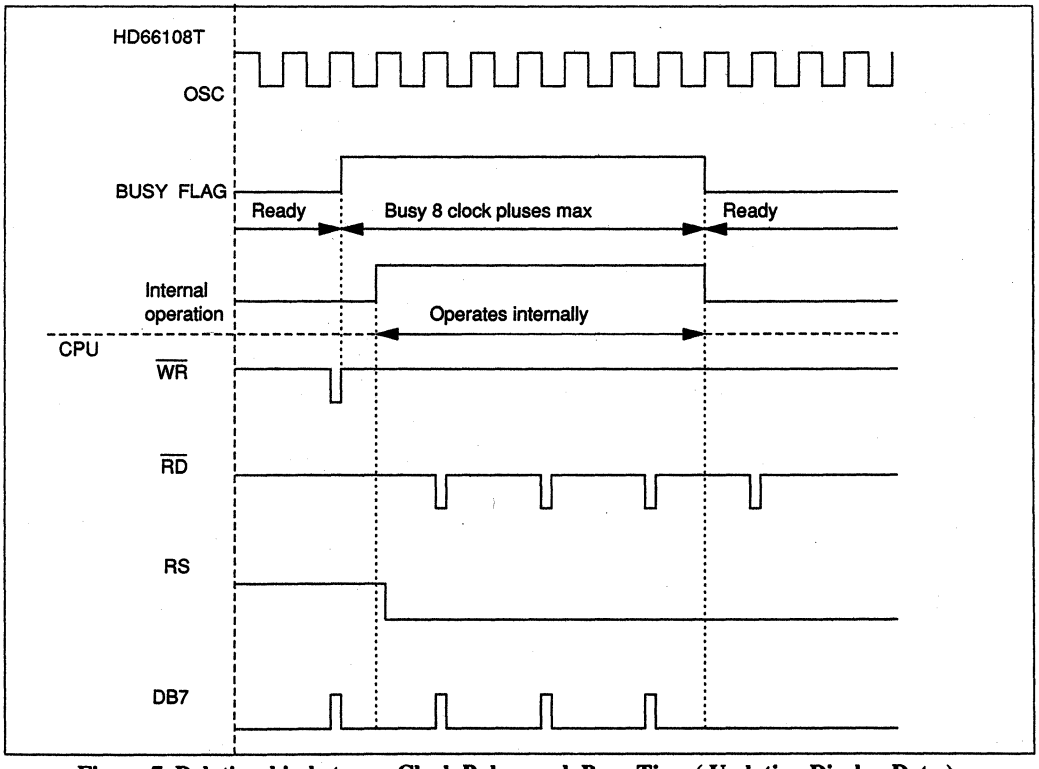


Figure 7 Relationship between Clock Pulses and Busy Time (Updating Display Data)

5

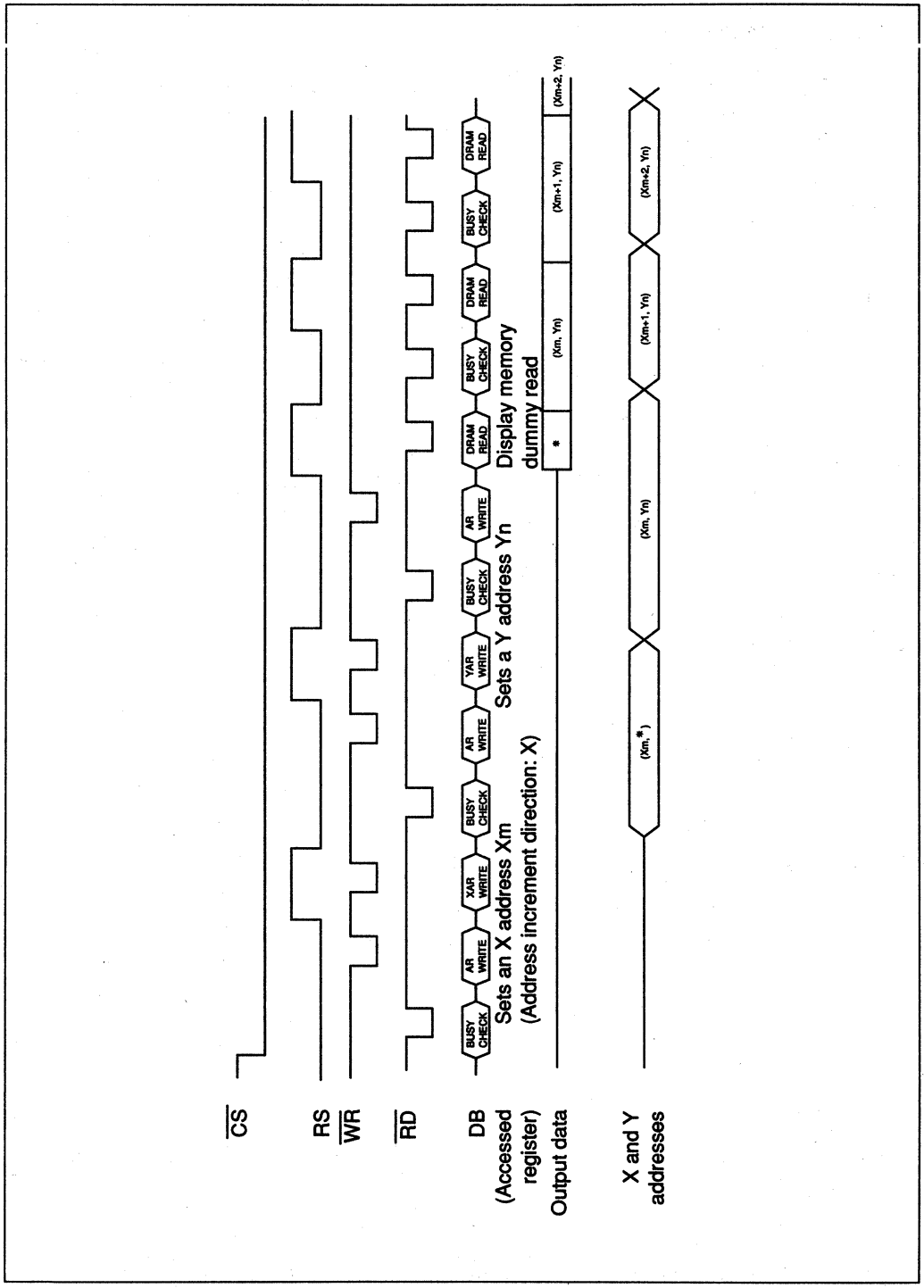


Figure 8 Display Memory Reading

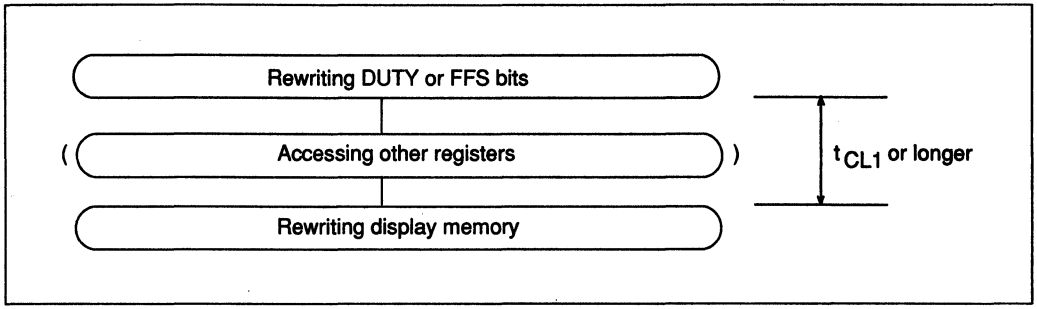


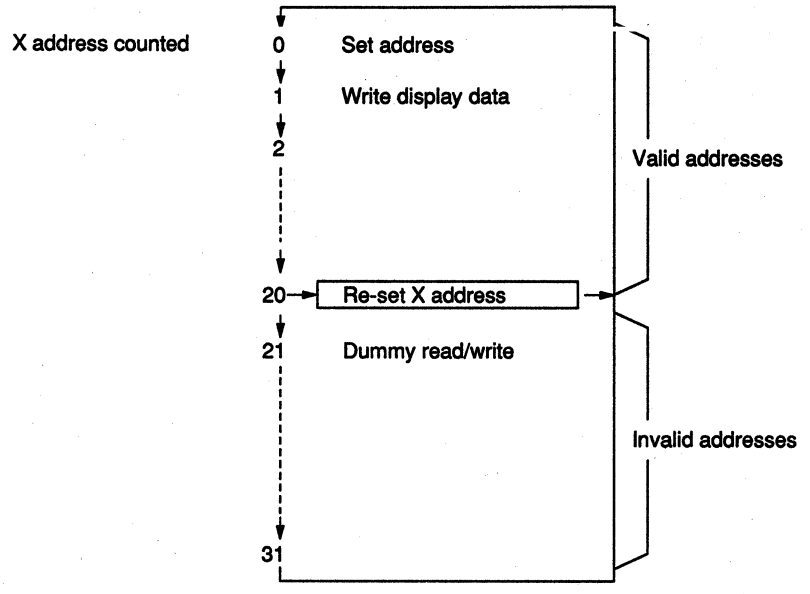
Figure 9 Rewriting Display Memory after Rewriting Registers

3.2 X and Y Address Counter Auto-Incrementing Function

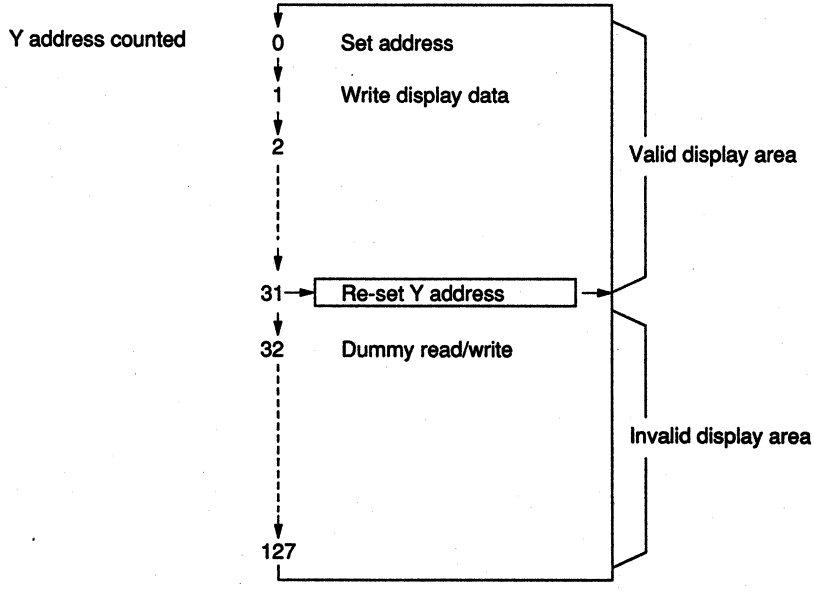
As described in "2. Display Memory Construction and Word Length Setting, " the HD66108T display memory has X and Y addresses. Internal X address counter and Y address counter both employ an auto-incrementing function. After display data is read or written, the X or Y address is incremented according to the address increment direction selected by internal register.

Although X addresses up to 20 are valid when 8 bits make up one word (up to 27 when 6 bits make up one word), the X address counter can count up to 31 since it is a 5-bit free counter. Similarly, although Y addresses up to 64 are valid, the Y address counter can count up to 127. Consequently, X or Y address must be re-set at an appropriate point as shown in figure 10.

5



(1) Example of X Address Counter Increment
(Word Length: 8 bits)



(2) Example of Y Address Counter Increment
(Multiplexing duty ratio: 1/32)

Figure 10 X/Y Address Counter Increment

4. Selection for LCD Driving Circuit Configuration

4.1 Row Output Pin Selection

The HD 66108T can assign a maximum of 65 pins for row outputs among the 165 pins named X0-X164. The X0-X164 pins can be classified into four blocks labeled A, B, C, and D (figure 11 (a)). Blocks A, C, and D consist of row/column common pins and block B consists of column pins only. The output function of the LCD driving pins and the combination of blocks can be selected by internal registers.

Figure 11 shows an example of 165-column-output mode. This configuration is useful when using more than 1 HD66108T chip or using the HD66108T as a slave chip of the HD61203.

Figure 12 shows an example of 65-row-output mode from the right side. Blocks A and B are used for column output and blocks C and D (X100-X164 pins) for row output. This configuration offers an easy way of connecting row output lines in the case of using one or more HD66108T chips.

Figure 13 shows an example of 65-row-output mode from the left and right sides. 32 pins of X0-X31 and 33 pins of X132-X164 are used for row output here. This configuration offers an easy way of connecting row output lines in the case of using only one HD66108T chip.

Figure 14 shows an example of 33-row-output mode from the right side. Block D, i.e., X132-X164 pins, is used for row outputs. This configuration provides a means for assigning many pins to column outputs when 1/32 or 1/34 multiplexing duty ratio is desired.

In all modes, it is row data and multiplexing duty ratio that determine which pins are actually used among the pins assigned to row output. Y values shown in table 1 indicate the numbers of pins that are actually used. Pins not used must be left disconnected.

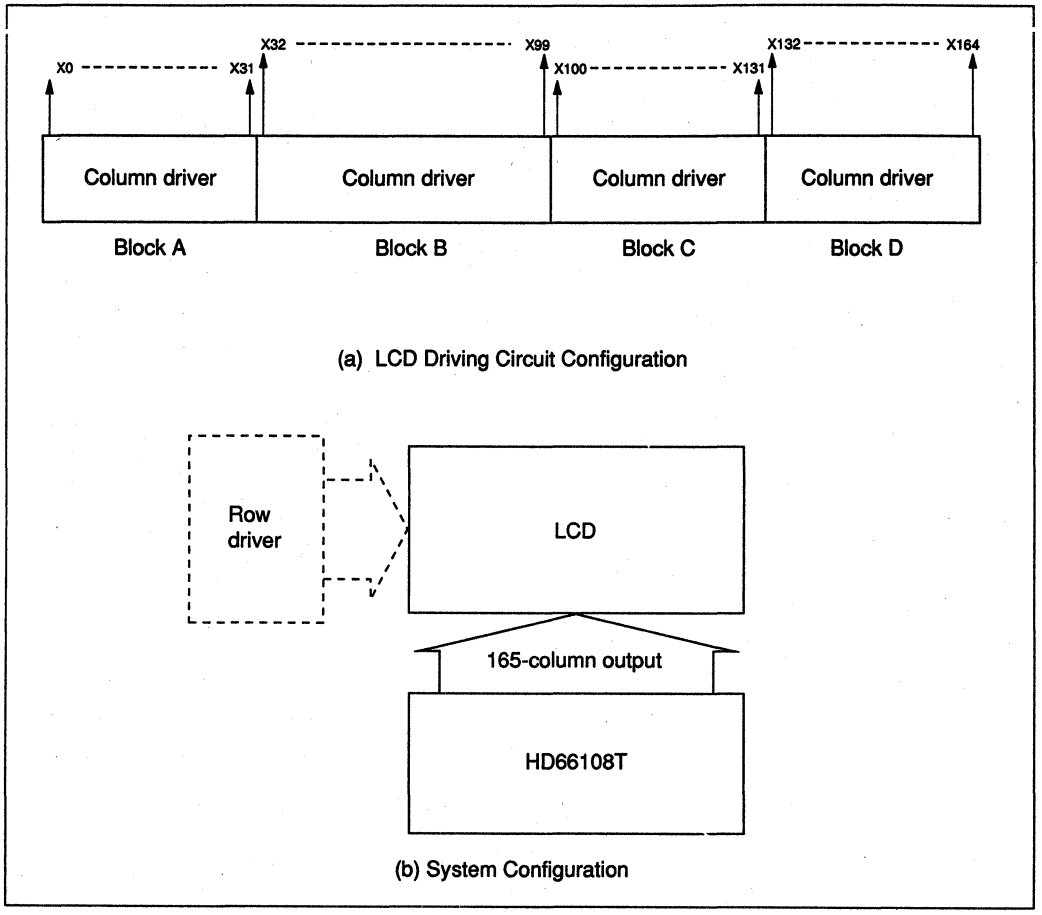
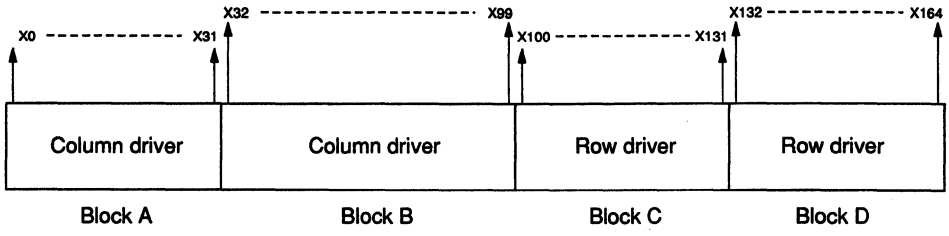
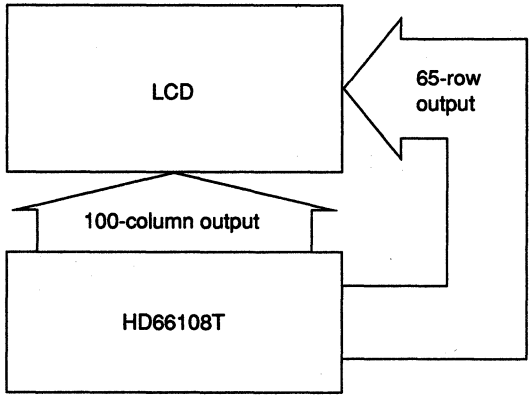


Figure 11 165-Column-Output Mode



(a) LCD Driving Circuit Configuration



(b) System Configuration

Figure 12 65-Row-Output Mode from the Right Side

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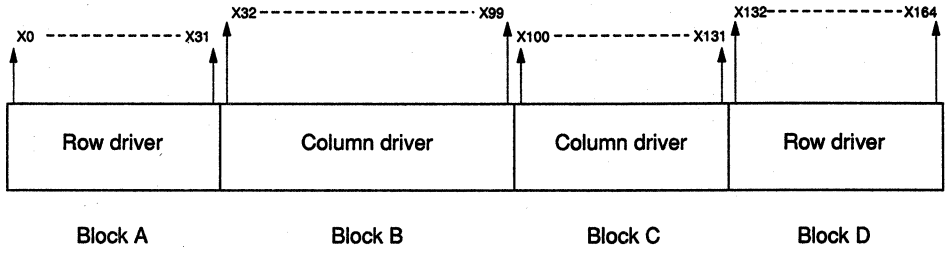
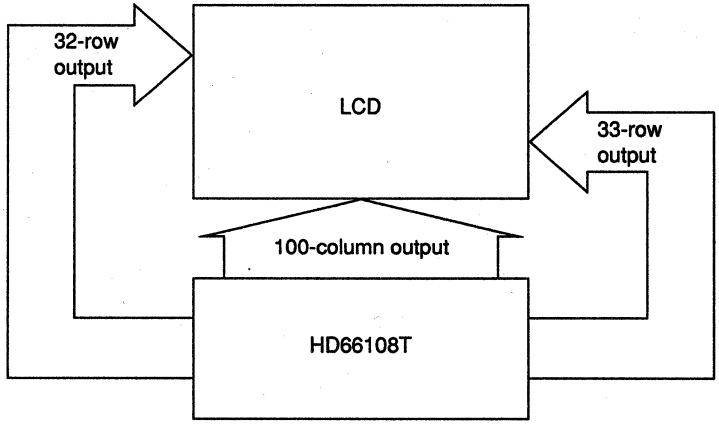
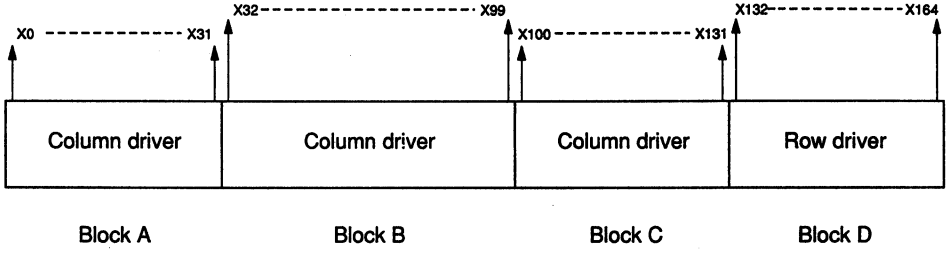


(a) LCD Driving Circuit Configuration

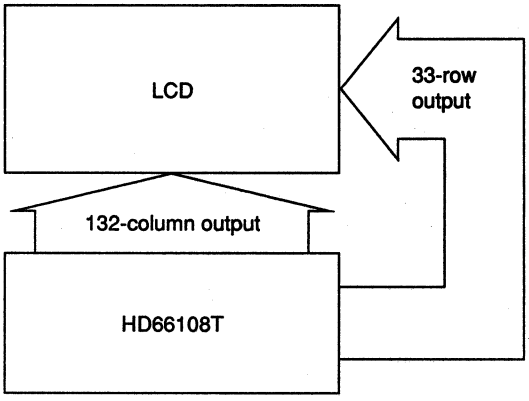


(b) System Configuration

Figure 13 65-Row-Output Mode from the Left and Right Sides



(a) LCD Driving Circuit Configuration



(b) System Configuration

Figure 14 33-Row-Output-Mode from the Right Side

5

4.2 Row Output Data Setting

If certain LCD driving output pins are assigned to row output, data must be written to display memory for row output. The specific area to which this data must be written depends on the row-output mode and the procedure of writing row data to the display memory (0 or 1 to which bits?) depends on which X pin drives which line of the LCD. Row data area is determined by the control register's (FCR) ROS and DUTY bits and is identical to the protected area, which will be described below. (165-column-output mode has no protected area, thus requiring no row data to be written (figure 15).)

Procedure of writing row data to the display memory is as follows. First, 1 must be written to the bit at the intersection between line Yj and line (column) Xi (column). Line Yj is filled with data to be displayed on the first line of the LCD and line Xi is connected to pin Xn, which drives the first line of the LCD. Following this, 0s must be written to the remaining bits on line Yj in the row data area. This rule applies to subsequent lines on the LCD.

Table 2 shows the relationship between FCR settings and protected areas.

Figure 16 shows the relationship between row data and display. Here the mode is 65-row output from the right side. Display data on Y0 is displayed on the first line of the LCD and data on Y64 is displayed on the 65th line of the LCD. If X164 is connected to the first line of the LCD and X100 is connected to the 65th line of the LCD, 1s must be written to the bits on the diagonal line between coordinates (X164, Y0) and (X100, Y64) and 0s to the remaining bits. Row data protect function must be turned off before writing row data and be turned on after writing row data. Turning on the row data protect function disables read/write of display memory area corresponding to the row output pins, i.e., prevents row data from being destroyed. In figure 16, display memory area corresponding to pins X100 to X164 is protected.

Figures 17 to 19 show examples of row data settings. Some multiplexing duty ratios result in invalid display areas. Although an invalid display area can be read from or written to, it will not be displayed.

Table 2 Relationship between FCR Settings and Protected Areas

Control Register (FCR)					
	ROS			LCD Driving Signal Output Pins Connected to	
PON	4	3	Mode	Protected Area of Display Memory	Figures
1	0	0	165-column	No area protected	15
1	0	1	65-row (R)	X100-X164	16, 19
1	1	0	65-row (L/R)	X0-X31 and X132-X164	17
1	1	1	33-row (R)	X132-X164	18

65-row (R) : 65-row-output mode from the right side
65-row (L/R) : 65-row-output mode from the left and right sides
33-row (R) : 33-row-output mode from the right side

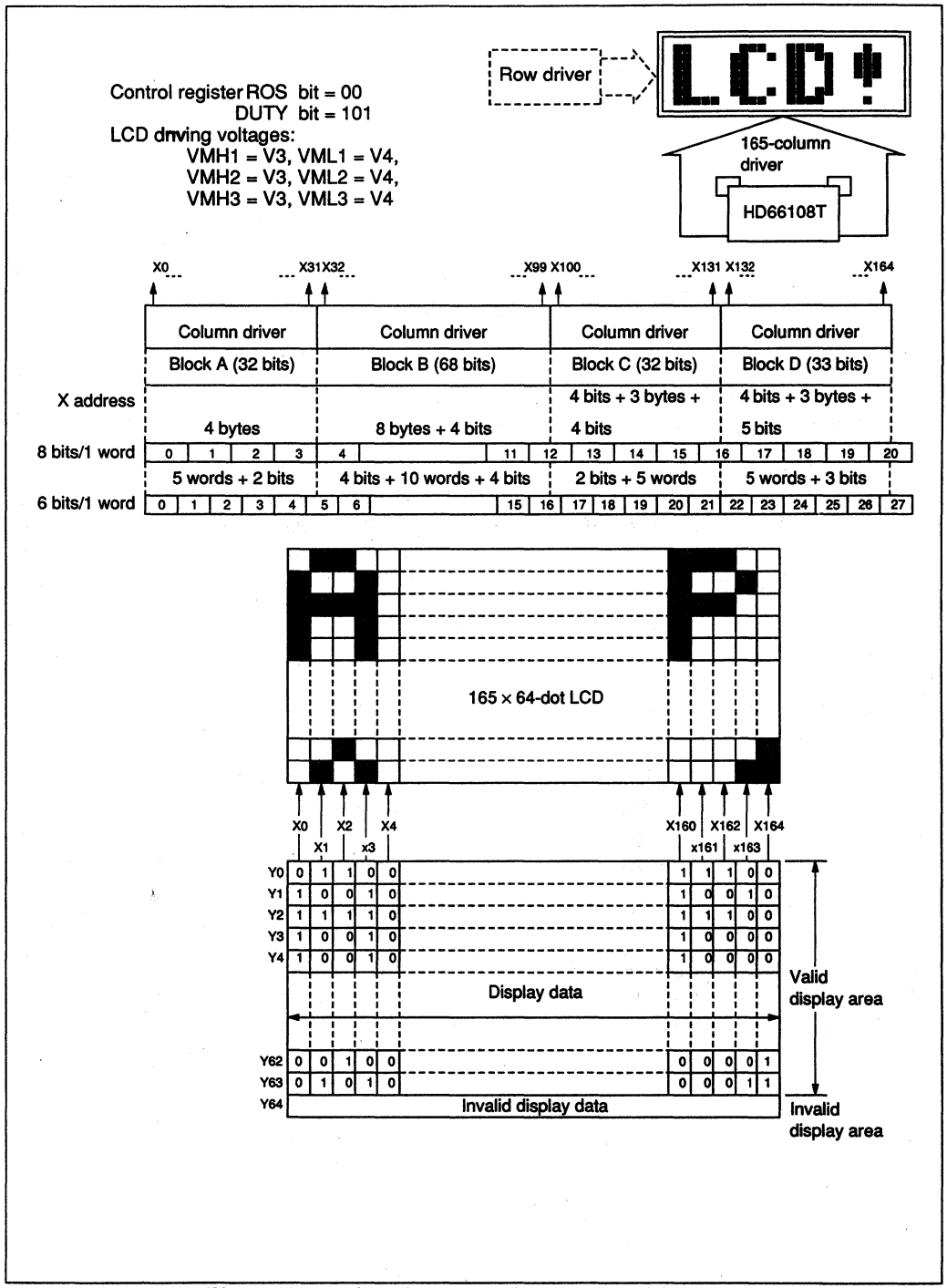


Figure 15 Relationship between Row Data and Display (165-Column Output, 1/64 Multiplexing Duty Ratio)

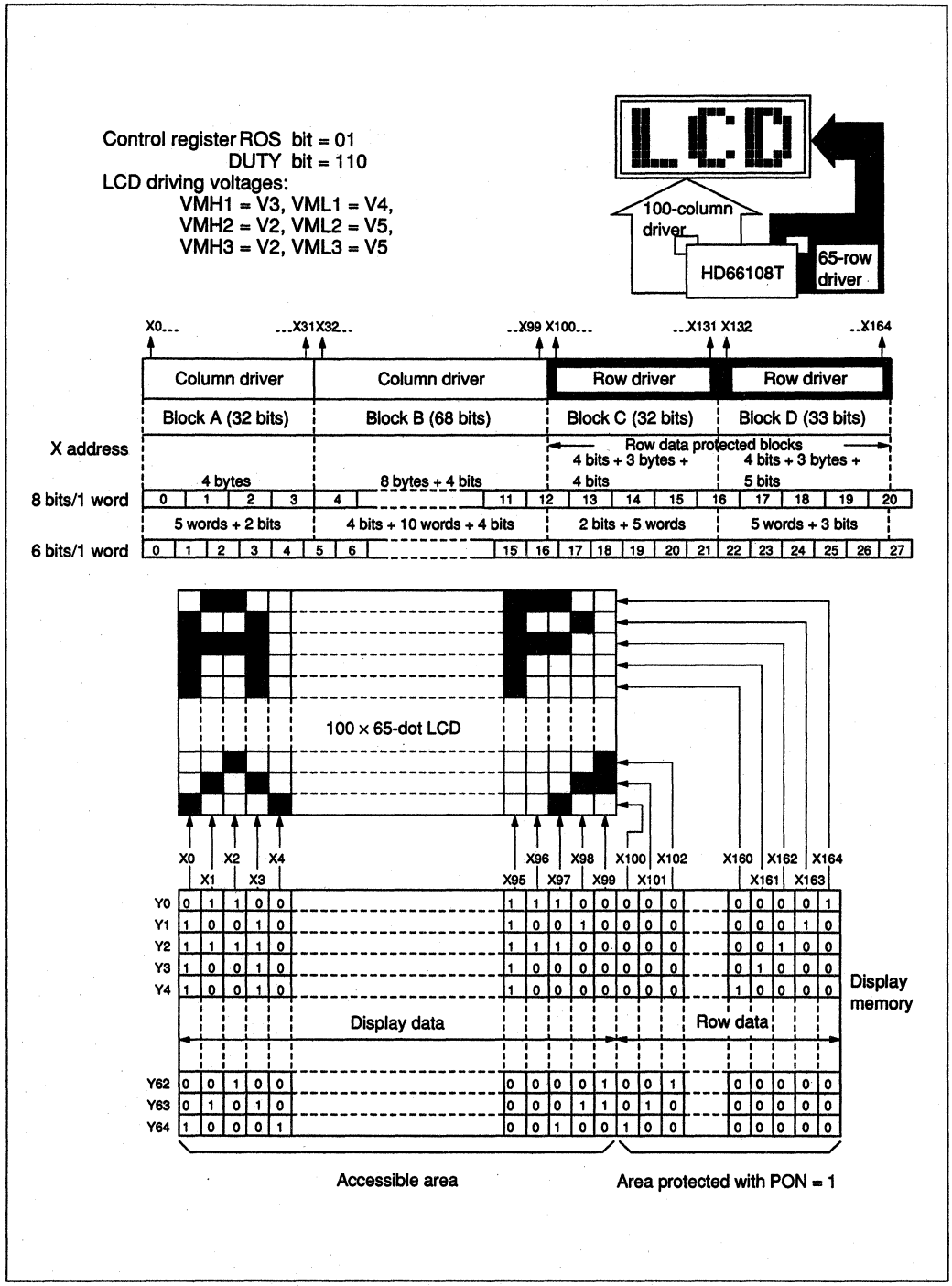


Figure 16 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/66 Multiplexing Duty Ratio)

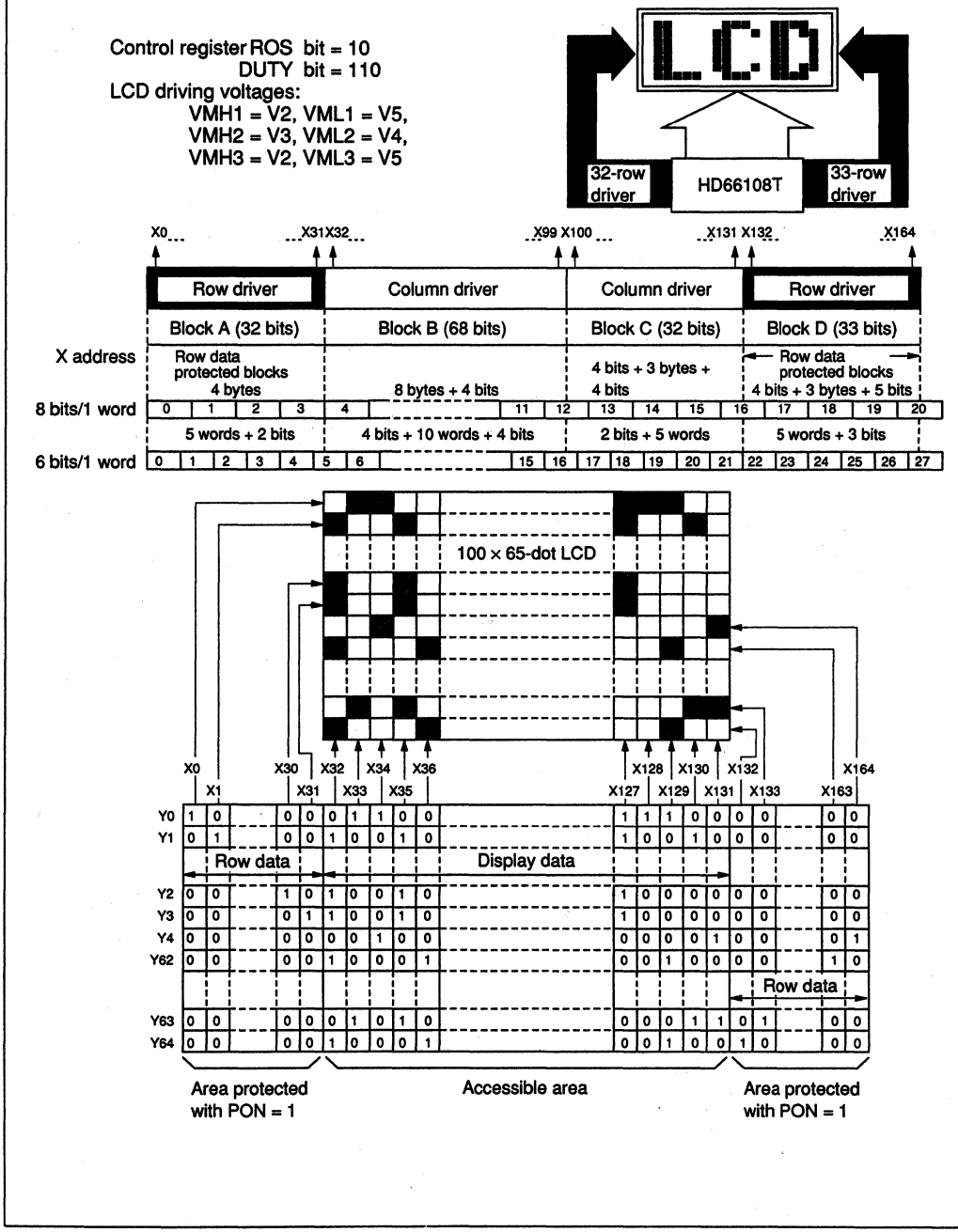


Figure 17 Relationship between Row Data and Display (65-Row Output from the Left and Right Sides, 1/66 Multiplexing Duty Ratio)

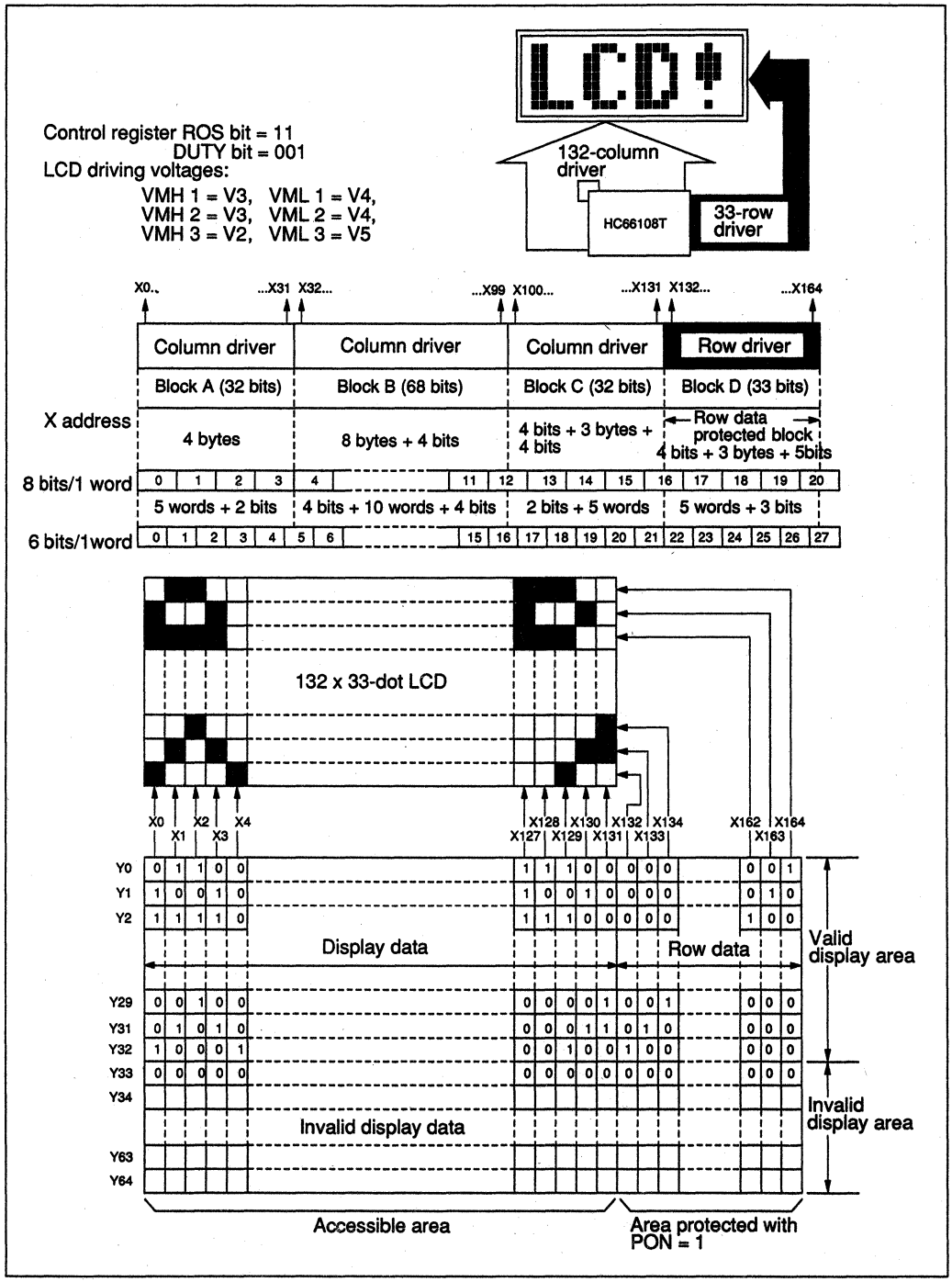
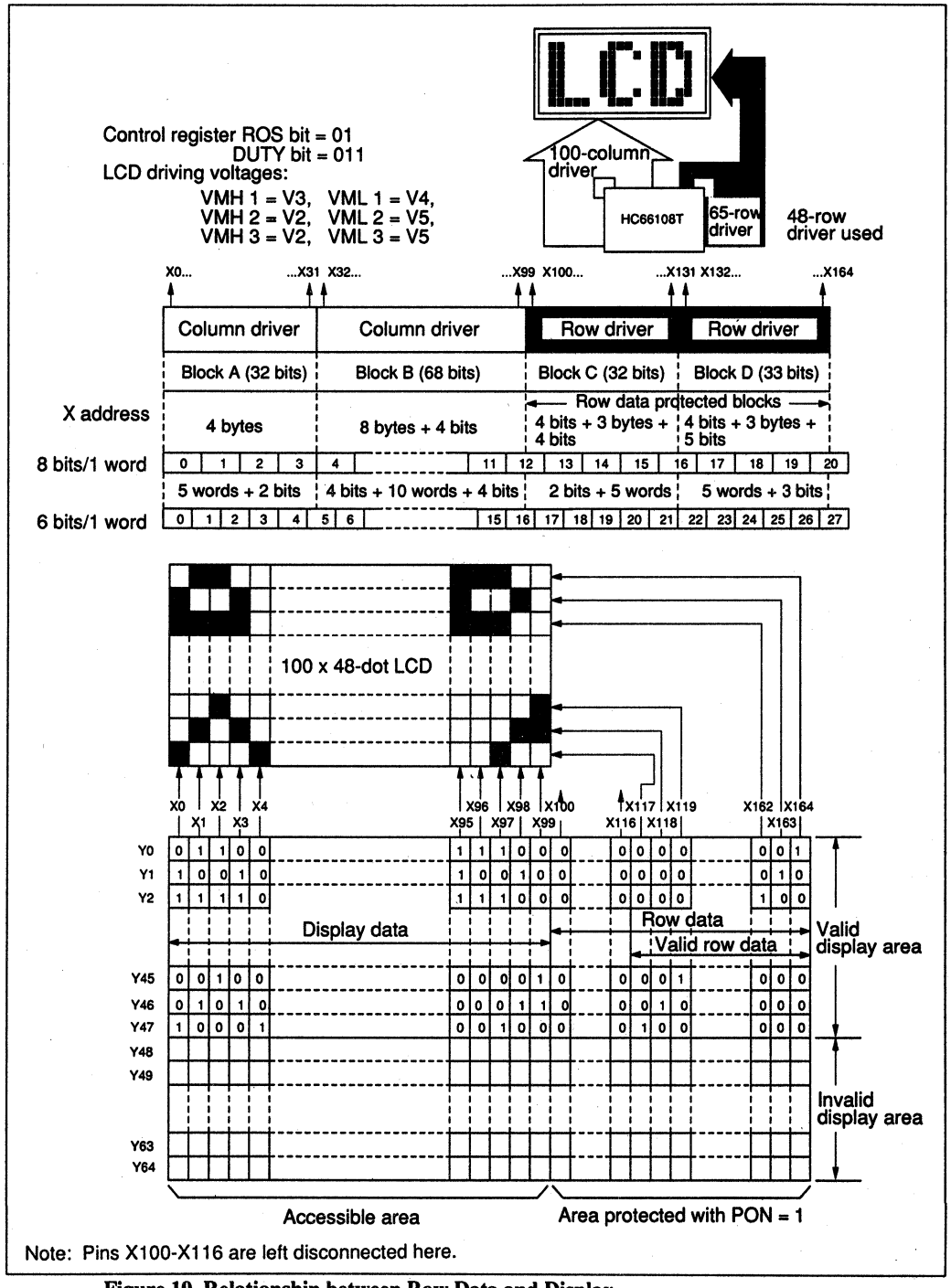


Figure 18 Relationship between Row Data and Display (33-Row Output from the Right Side, 1/34 Multiplexing Duty Ratio)



Note: Pins X100-X116 are left disconnected here.

Figure 19 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/48 Multiplexing Duty Ratio)

5

4.3 LCD Driving Voltage Setting

There are 6 levels of LCD driving voltages ranging from V1 to V6; V1 is the highest and V6 is the lowest. As shown in figure 20, column output waveform is made up of a combination of V1, V3, V4, and V6 while row output waveform is made up of V1, V2, V5, and V6. This means that V1 and V6 are common to both waveforms while mid-voltages are different.

To accommodate this situation, each block of the HD66108T is provided with power supply pins for mid-voltages as shown in figure 21. Each pair of V1R and V1L and V6R and V6L are internally connected and must be applied the same level of voltage. Block B is fixed for column output and must be applied V3 and V4 as mid-voltages. The other blocks must be applied different levels of voltages according to the function of their LCD driving output pins; if the LCD driving output pins are set for row output, VMHn and VMLn must be applied V2 and V5, respectively, while they must be applied V3 and V4, respectively, if the pins are set for column output (n = 1 to 3).

Table 3 Relationship between FCR settings and LCD Driving Voltages

Control Register (FCR)			LCD Driving Voltage Pins									
ROS4	ROS3	Mode	VIR/VIL	V3	V4	VMH1	VML1	VMH2	VML2	VMH3	VML3	V6R/V6L
0	0	165-column	V1	V3	V4	V3	V4	V3	V4	V3	V4	V6
0	1	65-row (R)	V1	V3	V4	V3	V4	V2	V5	V2	V5	V6
1	0	65-row (L/R)	V1	V3	V4	V2	V5	V3	V4	V2	V5	V6
1	1	33-row (R)	V1	V3	V4	V3	V4	V3	V4	V2	V5	V6

65-row (R) : 65-row-output mode from the right side
65-row (L/R) : 65-row-output mode from the left and right sides
33-row (R) : 33-row-output mode from the right side

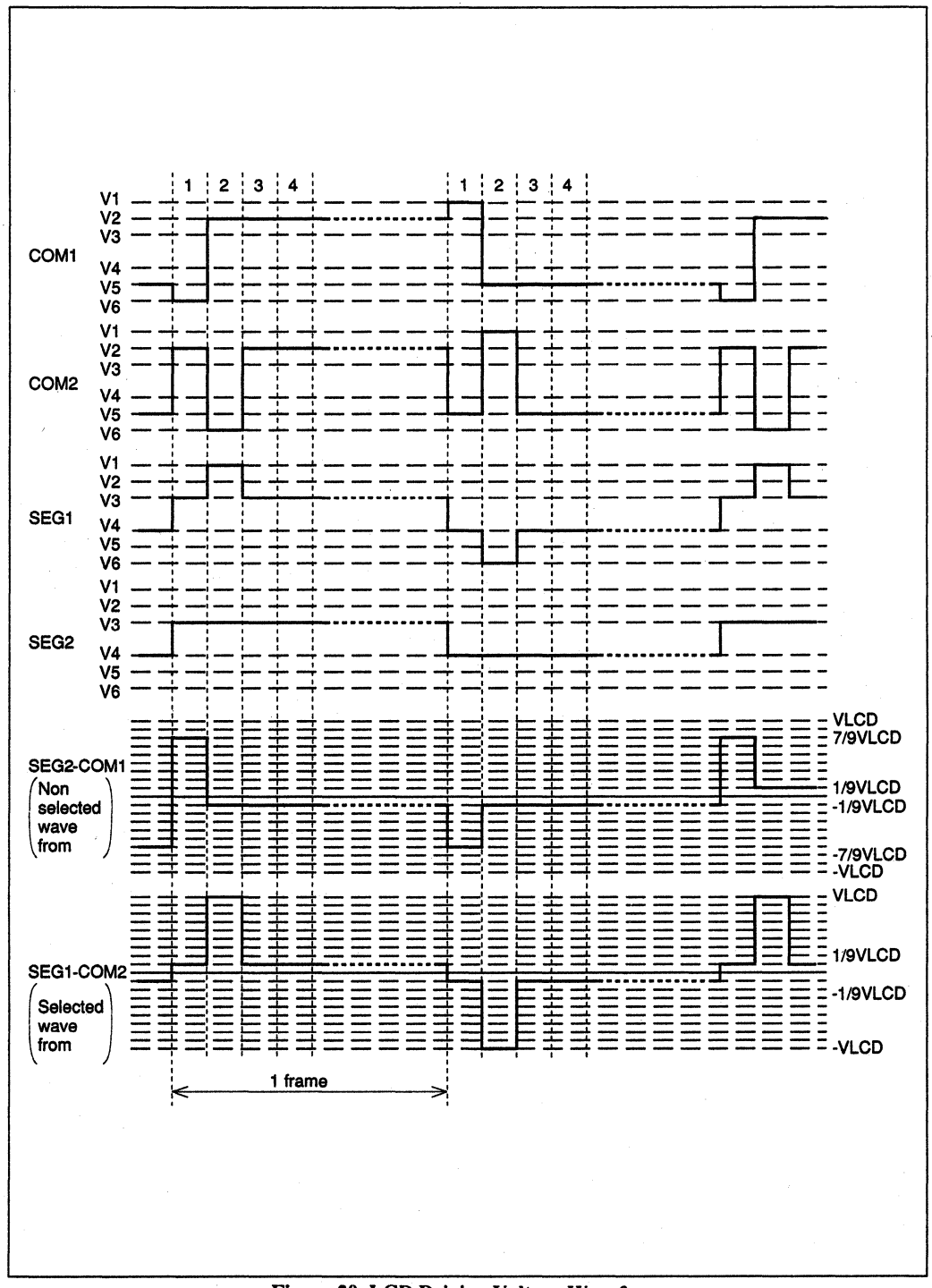


Figure 20 LCD Driving Voltage Waveforms

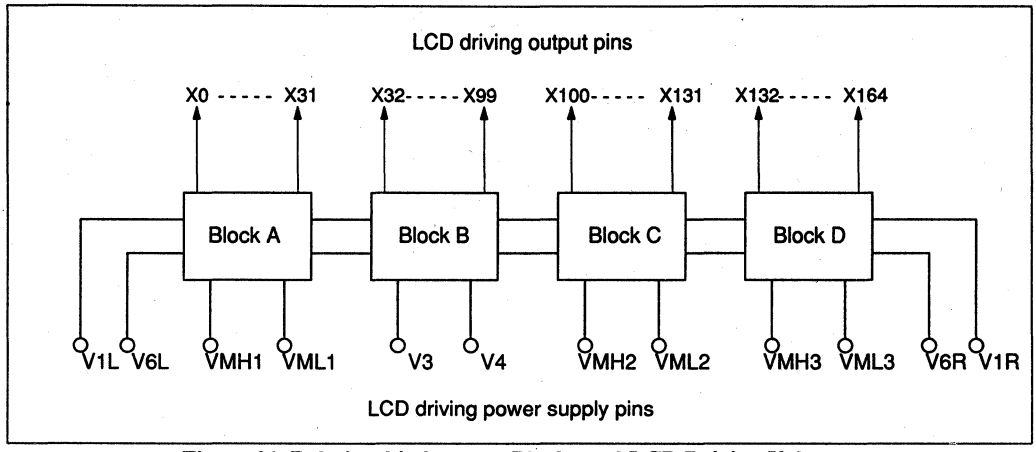


Figure 21 Relationship between Blocks and LCD Driving Voltages

5. Multiplexing Duty Ratio and LCD Driving Waveform Settings

A multiplexing duty ratio and LCD driving waveform can be selected via internal registers.

A multiplexing duty ratio of 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, or 1/66 can be selected according to the LCD panel used. However, since there are only 65 row-output pins, only 65 lines will be displayed even if 1/66 multiplexing duty ratio is selected.

There are three types of LCD driving waveforms, as shown in figure 22: A-type waveform, B-type waveform, and C-type waveform.

The A-type waveform is called per-half-line inversion. Here, the waveforms of M signal and CL1 signal are the same and alternate every LCD line.

The B-type waveform is called per-frame inversion; in this case, the M signal inverts its polarity every frame so as to alternate every two LCD frames. This is the most common type.

The C-type waveform is called per-n-line inversion and inverts its polarity every n lines (n can be set as needed within 1 to 31 via the internal registers). The C-type waveform combines the advantages of the A- and B-types of waveforms. However, some lines will not be alternated depending on the multiplexing duty ratio and n. To avoid this, another C-type waveform is available which is generated from the EOR of the C-type waveform M signal mentioned above and the B-type waveform M signal. Since the relationship between n and display quality usually depends on the LCD panel, n must be determined by observing actual display results.

The B-type waveform should be used if the LCD panel specifies no particular type of waveform. However, in some cases, the C-type waveform may create a better display.

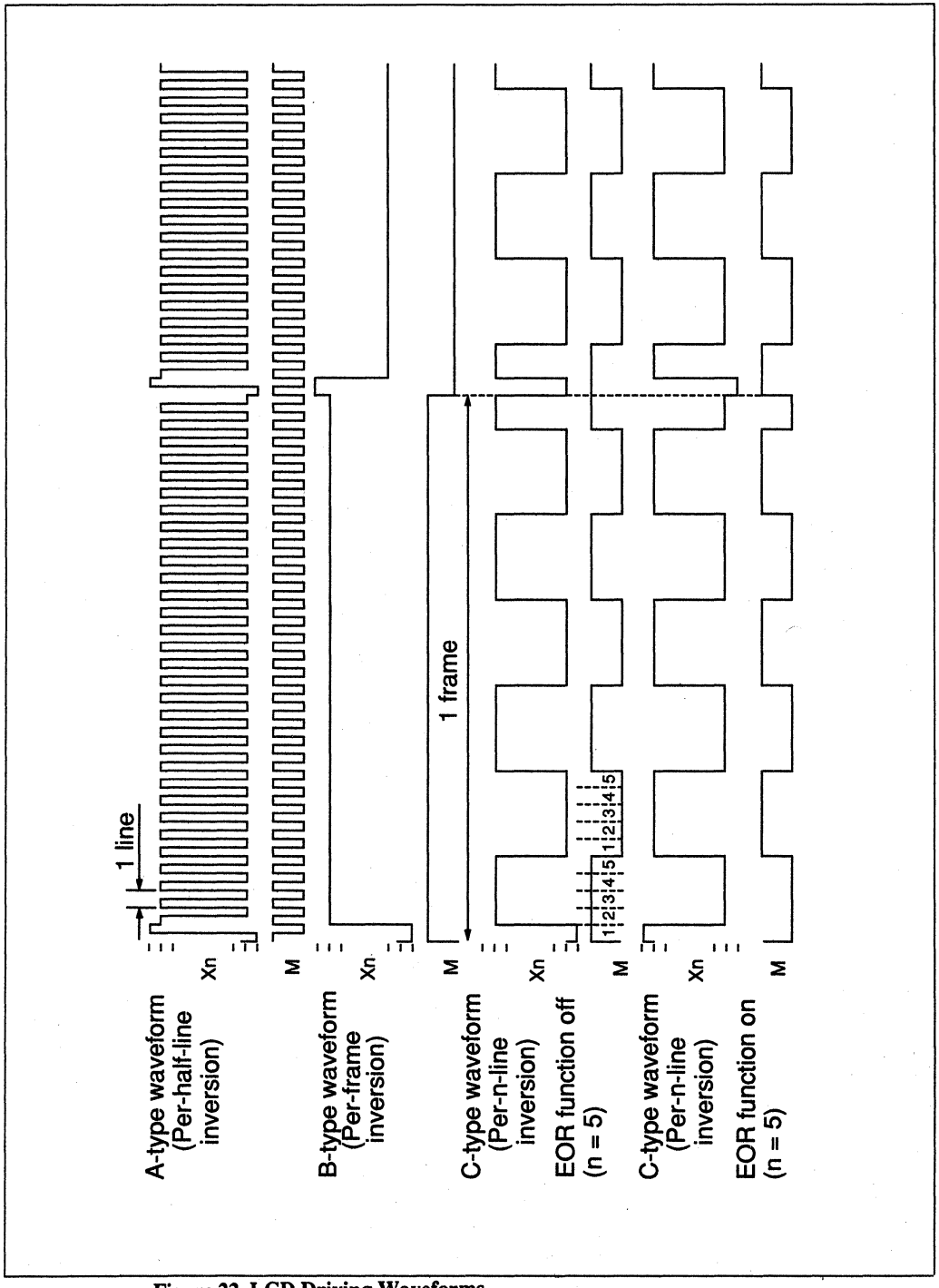


Figure 22 LCD Driving Waveforms (Row Output with a 1/32 Multiplexing Duty Ratio)

6. Clock and Frame Frequency

An input clock with a 200-kHz to 4-MHz frequency can be used for the HD66108T. Note that raising clock frequency increases current consumption although it reduces busy time and enables high-speed operations. An optimum system clock frequency should thus be selected within 200 kHz to 4 MHz.

The clock frequency driving the LCD panel (= frame frequency) is usually 70 Hz to 90 Hz. Accordingly, the HD66108T is so designed that the frequency-division ratio of the input clock can be selected. The HD66108T generates around 80-Hz LCD frame frequency if the frequency-division ratio is 1. The frequency-division ratio can be obtained from the following equation.

$$Ni = \frac{f_F}{f_{CLK}} \times \frac{500}{80} \times D1$$

Ni : Frequency-division ratio
f_F : Frame frequency required for the LCD panel (Hz)
f_{CLK} : Input clock frequency (kHz)
D1 : Duty correction value 1
D1 = 1 when multiplexing duty ratio is 1/32, 1/48 or 1/64
D1 = 32/34 when multiplexing duty ratio is 1/34
D1 = 32/36 when multiplexing duty ratio is 1/36
D1 = 48/50 when multiplexing duty ratio is 1/50
D1 = 64/66 when multiplexing duty ratio is 1/66

The frequency-division ratio nearest the value obtained from the above equation must be selected; selectable frequency-division ratios by internal registers are 2, 1, 1/2, 1/3, 1/4, 1/6, and 1/8.

7. Display Off function

The HD66108T has a display off function which turns off display by rewriting the contents of the internal register. This prevents random display at power-on until display memory is initialized.

8. Standby Function

The HD66108T has a standby function provinding low-power dissipation. Writing a 1 to bit 6 of the address register starts up the standby function.

The LCD driving voltages, ranking from V1 to V6, must be set to V_{CC} to prevent DC voltage from beging applied to an LCD panel during standby state.

The HD66108T operates as follows in standby mode.

(1) Stops oscillation and external clock input
(2) Resets all registers to 0's except the STBY bit

Here, note that the display memory will not preserve data if the standby function is turned on; the display memory as well as registers must be set again after the standby function is terminated.

Table 4 shows the standby status of pins and table 5 shows the status of registers after standby function termination.

Writing a 0 to bit 6 of the address register terminates the standby function. Writing values into the DISP and Register No. bits at this time is ignored; these bits need to be set after the standby function has been completely terminated.

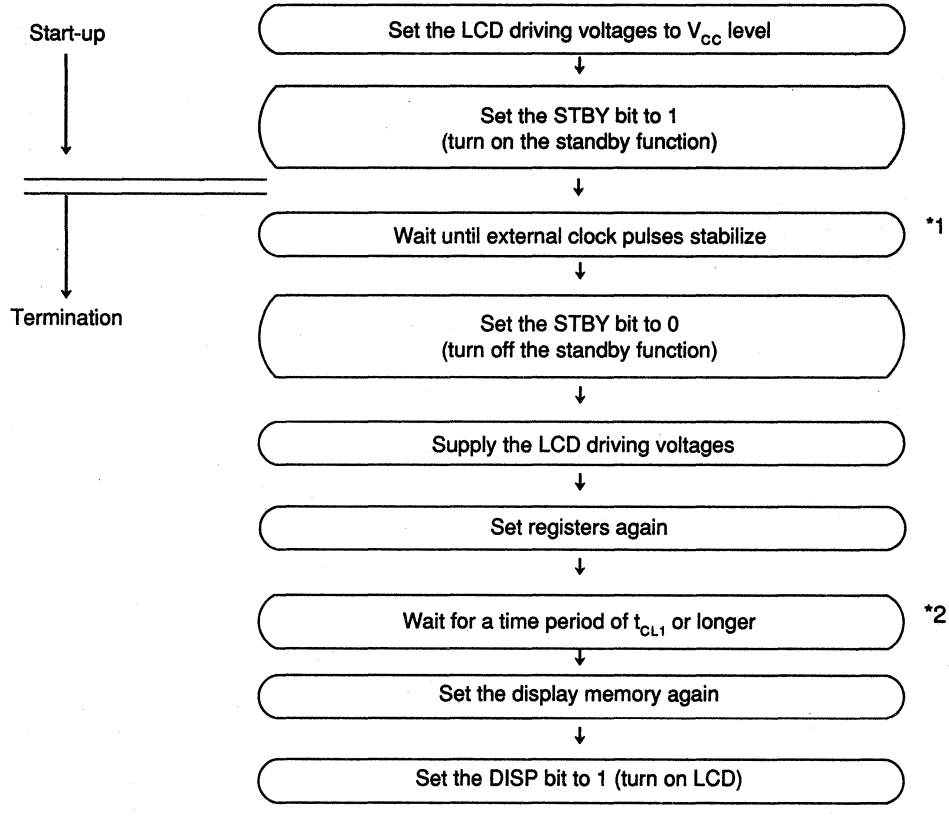
Figure 23 shows the flow for start-up and termination of the standby function and related operations.

Table 4 Standby Status of Pins

Pin	Status
OSC2	High
CO	Low
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn (column output pins)	V4
Xn' (row output pins)	V5

Table 5 Register Status after Standby Function Termination

Register Name	Status after Standby Function Termination
Address register	Reset to 0's except for the STBY bit
X address register	Reset to 0's
Y address register	Reset to 0's
Control register	Reset to 0's
Mode register	Reset to 0's
C select register	Reset to 0's
Display memory	Data not preserved



Notes: 1. Not necessary in the case of using internal oscillation
2. Refer to equation 1 (section 3.1).

Figure 23 Start-Up and Termination of Standby Function and Related Operations

9. Multi-Chip Operation

Using multiple HD66108T chips (= multi-chip operation) provides the means for extending the number of disply dots. Note the following items when using the multi-chip operation.

(1) The master chip and the slave chips must be determined; the $\overline{M}$/S pin of the master chip must be set low and the $\overline{M}$/S pin of the slave chips must be set high.
(2) All the HD66108T chips will be slave chips if HD61203 or its equivalent is used as a row driver.
(3) The master chip supplies the FLM, CL1, and M signals to the slave chips via the corresponding pins, which synchronizes the slave chips with the master chip.
(4) Since a master chip outputs synchronization signals, all data registers must be set.
(5) The following bits for slave chips must always be set:
INC, WLS, PON, and ROS (control register)
FFS (mode register)
It is not necessary to set the control register's DUTY bits, the mode register's DWS bits, or the C select register. For other registers' settings, refer to table 6.
(6) All chips must be set to LCD off in order to turn off the display.
(7) The standby function of slave chips must be started up first while that of the master chip must be terminated first.

Figure 24 to 26 show the connections of the synchronization signals for different system configurations and table 6 lists the differences between master mode and slave mode.

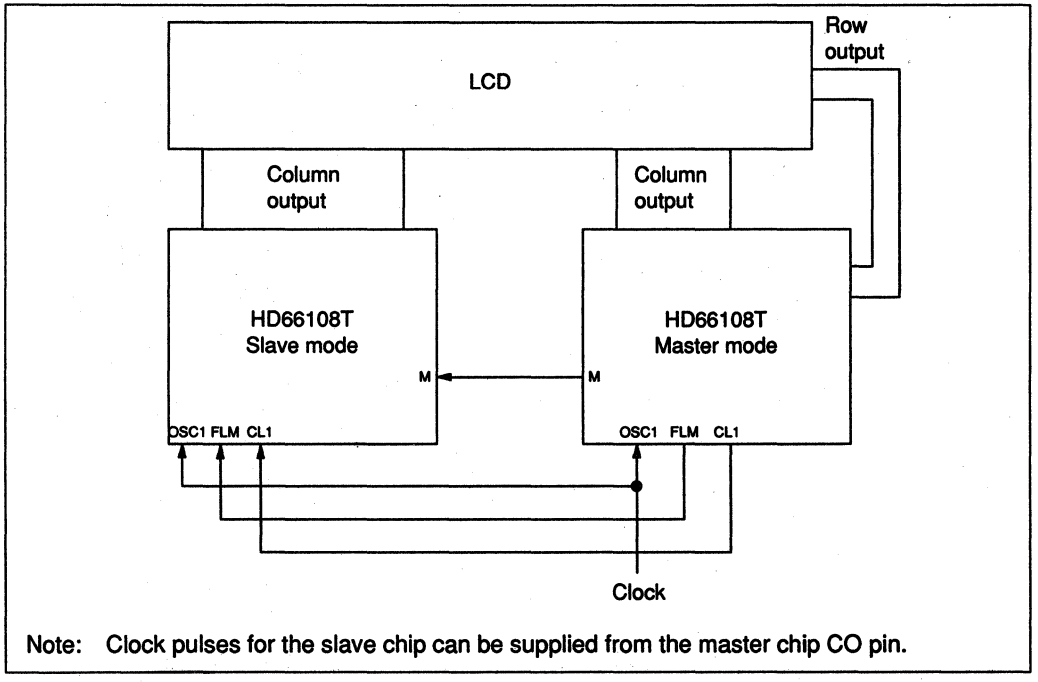
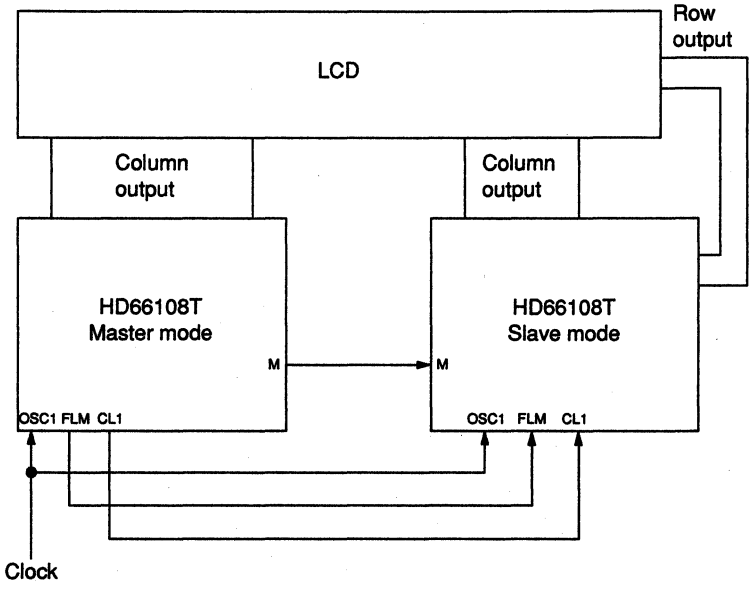


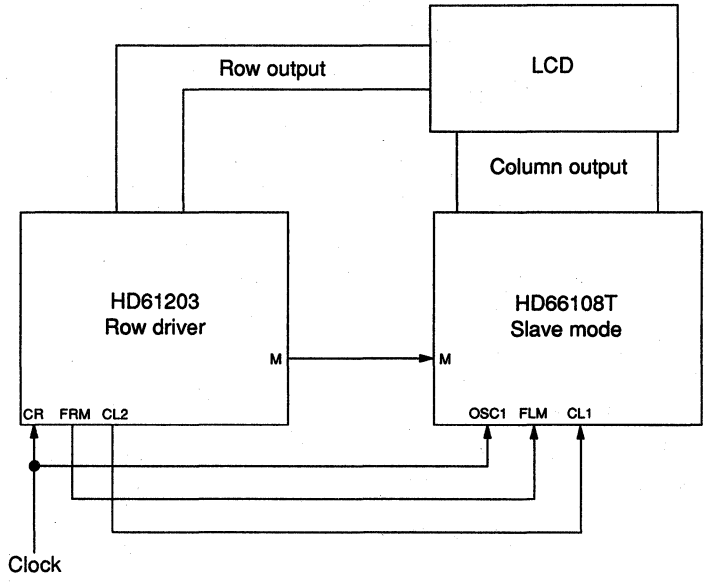
Figure 24 Configuration Using 2 HD66108T Chips (1)



Note: Clock pulses for the slave chip can be supplied from the master chip CO pin.

Figure 25 Configuration Using 2 HD66108T Chips (2)

5



Note: 1. The slave chip can oscillate CR clock pulses. In this case, the clock pulses must be supplied to the HD61203 from the HD66108T's CO pin.
2. The HD61203's control pins must be set in accordance with the type of RAMs.

Figure 26 Configuration Using 1 HD66108T Chip with Another Row Driver (HD61203)

Table 6 Comparison between Master and Slave Mode

Item		Master Mode	Slave Mode
Pin:	$\overline{M}$/S	Must be set low	Must be set high
	OSC1, OSC2	Oscillation is possible	Oscillation is possible
	CO	= OSC1	= OCS1
	FLM, CL1, M	Output signals	Input signals
Register:	AR	Valid	Valid
	XAR	Valid	Valid
	YAR	Valid	Valid
	FCR	Valid	Valid except for the DUTY bits
	MDR	Valid	Valid except for the DWS bits
	CSR	Valid (only if the DWS bits are set for the C-tye waveform)	Invalid

Notes
- Valid : Needs to be set
- Invaid: Need not be set

5

Internal Registers

All HD66108T's registers can be read from and written into. However, the BUSY FLAG and invalid bits cannot be written to and reading invalid bits or registers returns 0's.

1. Address Register (AR) (Accessed with RS = 0)

This register (figure 27) contains Register No. bits, BUSY FLAG bit, STBY bit, and DISP bit. Register No. bits select one of the data registers according to the register number written. The BUSY FLAG bit indicates the internal operation state if read. The STBY bit activates the standby function. The DISP bit turns the display on or off. This register is selected when RS pin is 0.

Bits D4 and D3 are invalid.

D7	D6	D5	D4	D3	D2	D1	D0
BUSY FLAG	STBY	DISP	—		Register No.		

(1) STBY
- 1: Standby function on
- 0: Normal (standby function off)

* When standby function is on, all registers are reset to 0's

(2) DISP
- 1: LCD on
- 0: LCD off

(3) Register No.

	Bit			
No.	2	1	0	Register
0	0	0	0	Display memory
1	0	0	1	X address register
2	0	1	0	Y address register
3	0	1	1	Control register
4	1	0	0	Mode register
5	1	0	1	C select register

(4) BUSY FLAG (Can be read only)
- 1: Busy state
- 0: Ready state

Figure 27 Address Register

2. Display Memory (DRAM) (Accessed with RS = 1, register number = $(000)_2$)

Although display memory (figure 28) is not a register, it can be handled as one. 8- or 6-bit data can be selected by the control register WLS bit according to the character font in use. If 6-bit data is selected, D7 and D6 bits are invalid.

3. X Address Register (XAR) (Accessed with RS = 1, register number = $(001)_2$)

This register (figure 29) contains 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0). It sets X addresses and confirms X addresses after writing or reading to or from the display memory.

4. Y Address Register (YAR) (Accessed with RS = 1, register number = $(010)_2$)

This register (figure 30) contains 1 invalid bit (D7) and 7 valid bits (D6 to D0). It sets Y addresses and confirms Y addresses after writing or reading to or from the display memory.

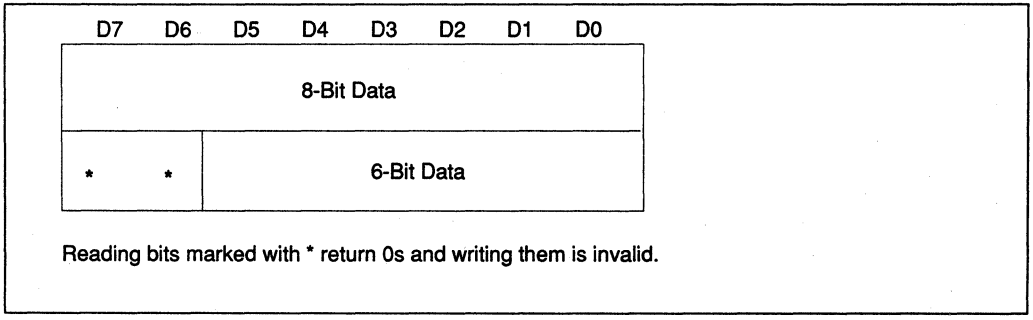


Figure 28 Display Memory

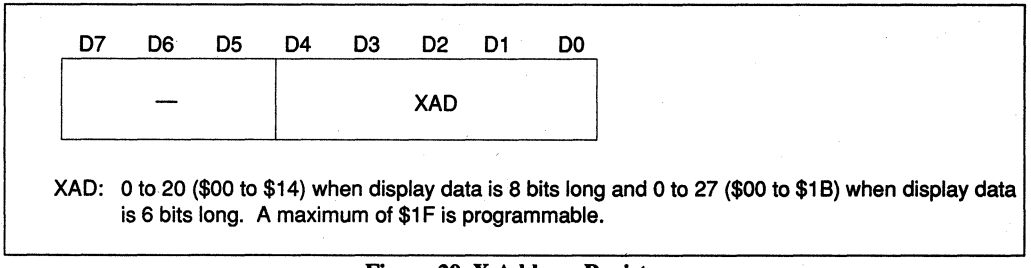


Figure 29 X Address Register

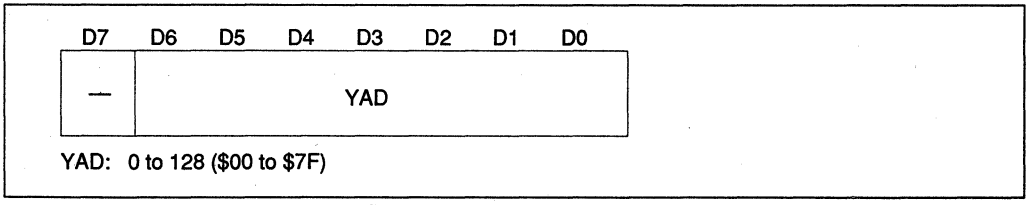


Figure 30 Y Address Register

5

5. Control Register (FCR) (Accessed with RS = 1, register number = $(011)_2$)

This register (figure 31), containing eight bits, has a variety of functions such as specifying the method for accessing RAM, determining RAM valid area, and selecting the function of the LCD driving signal output pins. It must be initialized as soon as possible after power-on since it determines the overall operation of the HD66108T. The PON bit may have to be re-set afterwards. If the DUTY bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 (section 3.1).

D7	D6	D5	D4	D3	D2	D1	D0
INC	WLS	PON	ROS		DUTY		

(1) INC (Address increment direction select)
- 1: X address is incremented
- 0: Y address is incremented

(2) WLS (Word length (of display data) select)
- 1: 6-bit word
- 0: 8-bit word

(3) PON (Row data protect on)
- 1: Protect function on
- 0: Pretect function off

(4) ROS (Row output (function of LCD driving output pins) select)

	Bit	
No.	4	3	Contents
0	0	0	165 column outputs
1	0	1	65 row outputs from the right side
2	1	0	65 row outputs from the left and right sides
3	1	1	33 row outputs from the right side

(5) DUTY (Multiplexing duty ratio)

	Bit			Multiplexing
No.	2	1	0	Duty Ratio
0	0	0	0	1/32
1	0	0	1	1/34
2	0	1	0	1/36
3	0	1	1	1/48
4	1	0	0	1/50
5	1	0	1	1/64
6	1	1	0	1/66
7	1	1	1	Testing mode

Figure 31 Control Register

6. Mode Register (MDR) (Accessed with RS = 1, register number = $(100)_2$)

This register (figure 32), containing 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0), selects a system clock and type of LCD driving waveform. It must also be initialized after power-on since it determines overall HD66108T operation like the FCR register. If the FFS bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 (section 3.1).

D7	D6	D5	D4	D3	D2	D1	D0
—			FFS			DWS	

(1) FFS (Frame frequency select)

	Bit			Frequency-
No.	4	3	2	Division Ratio
0	0	0	0	1
1	0	0	1	1/2
2	0	1	0	1/3
3	0	1	1	1/4
4	1	0	0	1/6
5	1	0	1	1/8
6	1	1	0	2
7	1	1	1	—

(2) DWS (LCD driving waveform select)

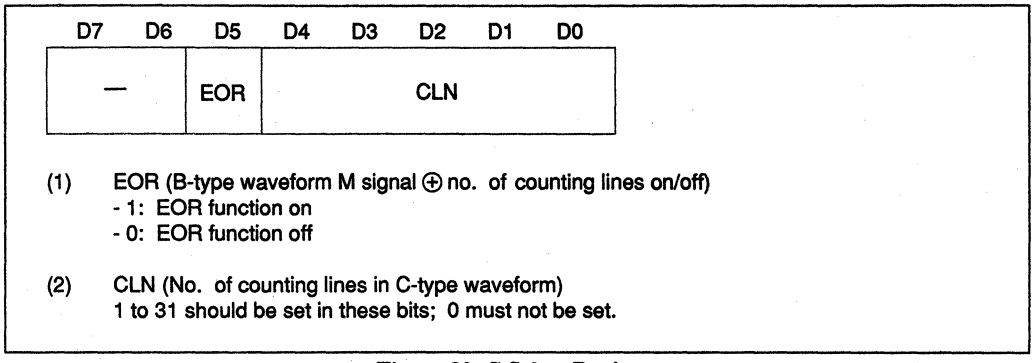
	Bit		
No.	1	0	Driving Waveform
0	0	0	A-type waveform
1	0	1	B-type waveform
2	1	0	C-type waveform
3	1	1	—

Figure 32 Mode Register

5

7. C Select Register (CSR) (Accessed with RS = 1, register number = $(101)_2$)

This register (figure 33) contains 2 invalid bits (D7 and D6) and 5 valid bits (D5 to D0). It controls C-type waveforms and is activated only when MDR register's DWS bits are set for this type of waveform.



(1) EOR (B-type waveform M signal ⊕ no. of counting lines on/off)
- 1: EOR function on
- 0: EOR function off

(2) CLN (No. of counting lines in C-type waveform)
1 to 31 should be set in these bits; 0 must not be set.

Figure 33 C Select Register

Reset Function

The $\overline{\text{RESET}}$ pin starts the HD66108T after power-on. A $\overline{\text{RESET}}$ signal must be input via this pin for at least 20 µs to prevent system failure due to excessive current created after power-on. Figure 34 shows the reset definition.

(1) Reset Status of Pins
Table 7 shows the reset status of output pins. The pins return to normal operation after reset.

(2) Reset Status of Registers
The $\overline{\text{RESET}}$ signal has no effect on registers or register bits except for the address register's STBY bit and the X and Y address registers, which are reset to 0's by the signal. Table 8 shows the reset status of registers.

(3) Status after Reset
The display memory does not preserve data which has been written to it before reset; it must be set again after reset.

A $\overline{\text{RESET}}$ signal terminates the standby mode.

Table 7 Reset Status of Pins

Pin	Status
OSC2	Outputs clock pulses or oscillates
CO	Outputs clock pulses
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn(column output pins)	V4
Xn' (Row output pins)	V5

Table 8 Reset Status of Registers

Register	Status
Address register	Pre-reset status with the STBY bit reset to 0
X address register	Reset to 0's
Y address register	Reset to 0's
Control register	Pre-reset status
Mode register	Pre-reset status
C select register	Pre-reset status
Display memory	Preserves no pre-reset data

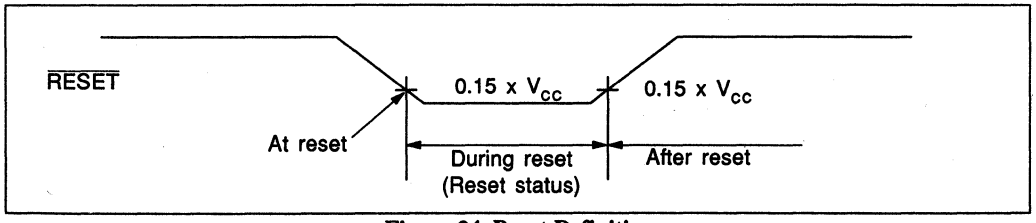


Figure 34 Reset Definition

Precautionary Notes When Using the HD66108T

(1) Install a 0.1-μF bypass capacitor as close to the LSI as possible to reduce power supply impedance (V_{CC}-GND and V_{CC}-V_{EE}).
(2) Do not leave input pins open since the HD66108T is a CMOS LSI; refer to "Pin Functions" on how to deal with each pin.
(3) When using the internal oscillation clock, attach an oscillation resistor as close to the LSI as possible to reduce coupling capacitance.
(4) Make sure to input the reset signal at power-on so that internal units operate as specified.
(5) Maintain the LCD driving power at V_{CC} during standby state so that DC is not applied to an LCD, in which Xn pins are fixed at V4 or V5 level.

Programming Restrictions

(1) After busy time is terminated, an X or Y address is not incremented until 0.5-clock time has passed. If an X or Y address is read during this time period, non-updated data will be read. (The addresses are incremented even in this case.) In addition, the address increment direction should not be changed during this time since it will cause malfunctions.
(2) Although the maximum output rows is 33 when 33-row-output mode from the right side is specified, any multiplexing duty ratio can be specified. Therefore, row output data sufficient to fill the specified duty must be input in the Y direction. Figure 35 shows how to set row data in the case of 1/34 multiplexing duty ratio. In this case, 0s must be set in Y33 since data for the 34th row (Y33) are not output.
(3) Do not set the C select register's CLN bits to 0 for the M signal of C-type waveform.

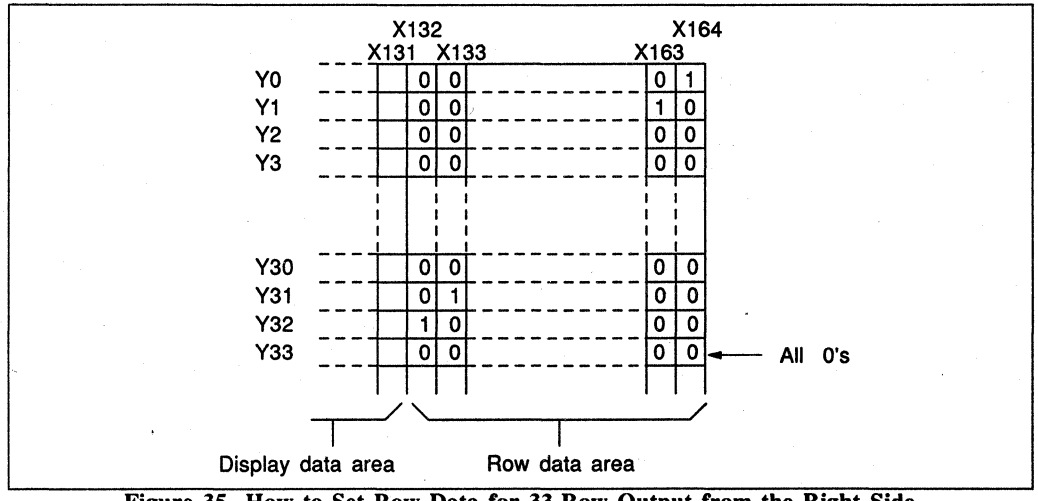


Figure 35 How to Set Row Data for 33-Row Output from the Right Side

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power Supply Voltage (1)	$V_{CC}1$ to $V_{CC}3$	–0.3 to +7.0	V
Power Supply Voltage (2)	$V_{CC} - V_{EE}$	–0.3 to +16.5	V
Input Voltage	V_{in}	–0.3 to VCC + 0.3	V
Operating Temperature	T_{op}	–20 to + 75	°C
Storage Temperature	T_{stg}	–20 to +85	°C

Notes: 1. Permanent LSI damage may occur if the maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 2.7 to 6.0 V, GND = 0 V, Ta = –20 to + 75°C). If these conditions are exceeded, LSI malfunctions could occur.

2. Power supply voltages are referenced to GND = 0 V. Power supply voltage (2) indicates the difference between V_{CC} and V_{EE}.

5

Electrical Characteristics

DC Characteristics (1) (V_{CC} = 5 V ±20%, GND = 0 V, V_{CC} – V_{EE} = 6.0 to 15 V, Ta = –20 to+75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input High Voltage	OSC1	$V_{IH}1$	0.8 × V_{CC}	–	V_{CC} + 0.3	V		
	M/S, CL1, FLM, M, TEST1, TEST2	$V_{IH}2$	0.7 × V_{CC}	–	V_{CC} + 0.3	V		
	$\overline{RESET}$	$V_{IH}3$	0.85 × V_{CC}	–	V_{CC} + 0.3	V		
	The other inputs	$V_{IH}4$	2.0	–	V_{CC} + 0.3	V	V_{CC} = 5 V ±10%	5
Input Low Voltage	OSC1	$V_{IL}1$	–0.3	–	0.2 × V_{CC}	V		
	M/S, CL1, FLM, M, TEST1, TEST2	$V_{IL}2$	–0.3	–	0.3 × V_{CC}	V		
	$\overline{RESET}$	$V_{IL}3$	–0.3	_	0.15 × V_{CC}	V		
	The other inputs	$V_{IL}4$	–0.3	_	0.8	V	V_{CC} = 5V ±10%	6
Output High Voltage	CO, CL1, FLM, M	$V_{OH}1$	0.9 × V_{CC}	–	–	V	$-I_{OH}$ = 0.1 mA	
	DB7–DB0	$V_{OH}2$	2.4	–	–	V	$-I_{OH}$ = 0.2 mA V_{CC} = 5 V ±10%	7
Output Low Voltage	CO, CL1, FLM, M	$V_{OL}1$	–	–	0.1 × V_{CC}	V	I_{OL} = 0.1 mA	
	DB7–DB0	$V_{OL}2$	–	–	0.4	V	I_{OL} = 1.6 mA V_{CC} = 5 V ±10%	8
Input Leakage Current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	–	2.5	µA	V_{in} = 0 to V_{CC}	
Tri-State Leakage Current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	–	10	µA	V_{in} = 0 to V_{CC}	
V Pins Leakage Current	V1, V3, V4, V6, VMHn, VMLn	I_{VL}	–10	–	10	µA	V_{in} = V_{EE} to V_{CC}	
Current Consumption	During display	$I_{CC}1$	–	–	400	µA	External clock f_{OSC} = 500 kHz	1
		$I_{CC}2$	–	–	1.0	mA	Internal oscillation Rf = 91 kΩ	1
	During standby data	I_{SB}	–	–	10	µA		1, 2
ON Resistance between Vi and Xj	X0–X164	R_{ON}	–	–	10	kΩ	±I_{LD} = 50 µA V_{CC} – V_{EE} = 10 V	3
V Pins Voltage Range		ΔV	–	–	35	%		4
Oscillating Frequency		f_{OSC}	315	450	585	kHz	Rf = 91 kΩ	

Notes:
1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity.
2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low. Exposing the LSI to light increases current consumption.
3. I_{LD} indicates the current supplied to one measured pin.
4. $\Delta V = 0.35 \times (V_{CC} - V_{EE})$. For levels V1, V2, and V3, the voltage employed should fall between the V_{CC} and the ΔV and for levels V4, V5, and V6, the voltage employed should fall between the V_{EE} and the ΔV (figure 36).
5. $V_{IH}3$ (min) = 0.7 × V_{CC} when used under conditions other than V_{CC} = 5 v ±10%.
6. $V_{IL}3$ (max) = 0.15 × V_{CC} when used under conditions other than V_{CC} = 5 V ±10%.
7. $V_{OH}2$ (min) = 0.9 × V_{CC} ($-I_{OH}$ = 0.1 mA) when used under conditions other than V_{CC} = 5 V ±10%.
8. $V_{OL}2$ (max) = 0.1 × V_{CC} (I_{OL} = 0.1 mA) when used under conditions other than V_{CC} = 5 V ±10%.

DC Characteristics (2) (V_{CC} = 2.7 to 4.0 V, GND = 0 V, $V_{CC} - V_{EE}$ = 6.0 to 15 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input High Voltage	$\overline{RESET}$	$V_{IH}1$	0.85 × V_{CC}	–	V_{CC} + 0.3	V		
	The other inputs	$V_{IH}2$	0.7 × V_{CC}	–	V_{CC} + 0.3	V		
Input Low Voltage	$\overline{M}$/S, OSC1, CL1, FLM, TEST1, TEST2, M	$V_{IL}1$	–0.3	–	0.3 × V_{CC}	V		
	The other inputs	$V_{IL}2$	–0.3	–	0.15 × V_{CC}	V		
Output High Voltage		$V_{OL}1$	0.9 × V_{CC}	–	–	V	$-I_{OH}$ = 50 µA	
Output Low Voltage		$V_{OL}1$	–	–	0.1 × V_{CC}	V	I_{OL} = 50 µA	
Input Leakage Current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	–	2.5	µA	V_{in} = 0 to V_{CC}	
Tri-State Leakage Current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	–	10	µA	V_{in} = 0 to V_{CC}	
V Pins Leakage Current	V1, V3, V4, V6, VMHn, VMLn	I_{VL}	–10	–	10	µA	V_{in} = V_{EE} to V_{CC}	
Current Consumption	During display	$I_{CC}1$	–	–	260	µA	External clock f_{OSC} = 500 kHz	1
		$I_{CC}2$	–	–	700	µA	Internal oscillation Rf = 75 kΩ	1
	During standby state	I_{SB}	–	–	10	µA		1, 2
ON Resistance between Vi and Xj	X0–X164	R_{ON}	–	–	10	kΩ	±I_{LD} = 50 µA $V_{CC} - V_{EE}$ = 10 V	3
V Pins Voltage Range		ΔV	–	–	35	%		4
Oscillating Frequency		f_{OSC}	315	450	585	kHz	Rf = 75 kΩ	

Notes: 1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity. Exposing the LSI to light increases current consumption.
2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low.
3. I_{LD} indicates the current supplied to one measured pin.
4. $\Delta V = 0.35 \times (V_{CC} - V_{EE})$. For levels V1, V2, and V3, the voltage employed should fall between the V_{CC} and the ΔV and for levels V4, V5, and V6, the voltage employed should fall between the V_{EE} and the ΔV (figure 36)

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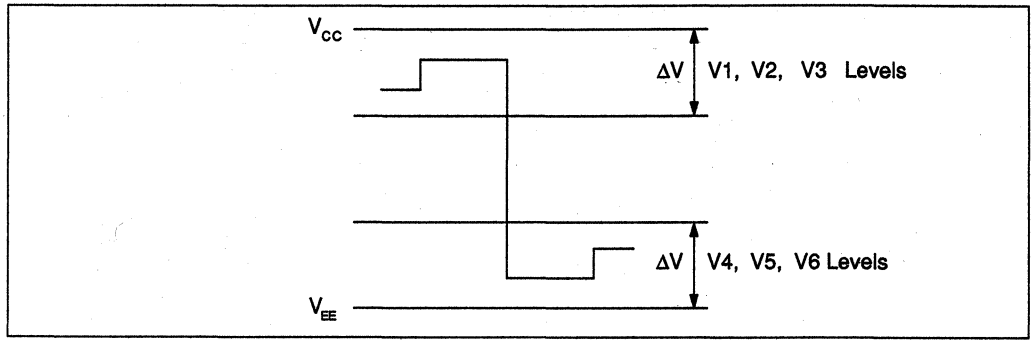

Figure 36 Driver Output Waveform and Voltage Levels

AC Characteristics (1) (V_{CC} = 4.5 to 6.0 V, GND = 0 V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ High-Level Pulse Width	t_{WRH}	190	–	ns	
$\overline{RD}$ Low-Level Pulse Width	t_{WRL}	190	–	ns	
$\overline{WR}$ High-Level Pulse Width	t_{WWH}	190	–	ns	
$\overline{WR}$ Low-Level Pulse Width	t_{WWL}	190	–	ns	
$\overline{WR}$–$\overline{RD}$ High-Level Pulse Width	t_{WWRH}	190	–	ns	
$\overline{CS}$, RS Setup Time	t_{AS}	0	–	ns	
$\overline{CS}$, RS Hold Time	t_{AH}	0	–	ns	
Write Data Setup Time	t_{DSW}	100	–	ns	
Write Data Hold Time	t_{DHW}	0	–	ns	
Read Data Output Delay Time	t_{DDR}	–	150	ns	Note
Read Data Hold Time	t_{DHR}	20	–	ns	Note
External Clock Cycle Time	t_{CYC}	0.25	5.0	µs	
External Clock High-Level Pulse Width	t_{WCH}	0.1	–	µs	
External Clock Low-Level Pulse Width	t_{WCL}	0.1	–	µs	
External Clock Rise and Fall time	tr, tf	–	20	ns	

Note: Measured by test circuit 1 (figure 39).

2. LCD Interface Timing (figure 38)

Item			Symbol	Min	Max	Notes
$\overline{M}$/S = 0	CL1	High-Level Pulse Width	$t_{WCH}1$	35	–	1, 4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}1$	35	–	1, 4, 5
	FLM	Delay Time	$t_{DFL}1$	–2.0	+2.0	4, 5
	FLM	Hold Time	$t_{HFL}1$	–2.0	+2.0	4, 5
	M Output Delay Time		$t_{DMO}1$	–2.0	+2.0	4, 5
$\overline{M}$/S = 1	CL1	High-Level Pulse Width	$t_{WCH}2$	35	–	4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}2$	11 × t_{CYC}	–	2, 4, 5
	FLM	Delay Time	$t_{DFL}2$	–2.0	1.5 × t_{CYC}	3, 4, 5
	FLM	Hold Time	$t_{HFL}2$	–2.0	+2.0	4, 5
	M Delay Time		t_{DMI}	–2.0	+2.0	4, 5

Notes:
1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6 V) or 75 kΩ (V_{CC} = 2.0 to 4.0 V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is 19 × t_{CYC} in other cases.
3. When bitgs FFS are set for 1 or 2. The value is 8.5 × t_{CYC} in other cases.
4. Measured by test circuit 2 (figure 39).
5. Units are µs.

AC Characteristics (2) (V_{CC} = 2.7 to 4.5 V, GND = 0 V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ High-Level Pulse Width	t_{WRH}	1.0	–	µs	
$\overline{RD}$ Low-Level Pulse Width	t_{WRL}	1.0	–	µs	
$\overline{WR}$ High-Level Pulse Width	t_{WWH}	1.0	–	µs	
$\overline{WR}$ Low-Level Pulse Width	t_{WWL}	1.0	–	µs	
$\overline{WR}$–$\overline{RD}$ High-Level Pulse Width	t_{WWRH}	1.0	–	µs	
$\overline{CS}$, RS Setup Time	t_{AS}	0.5	–	µs	
$\overline{CS}$, RS Hold Time	t_{AH}	0.1	–	µs	
Write Data Setup Time	t_{DSW}	1.0	–	µs	
Write Data Hold Time	t_{DHW}	0	–	µs	
Read Data Output Delay Time	t_{DDR}	–	0.5	µs	Note
Read Data Hold Time	t_{DHR}	20	–	ns	Note
External Clock Cycle Time	t_{CYC}	1.6	5.0	µs	
External Clock High-Level Pulse Width	t_{WCH}	0.7	–	µs	
External Clock Low-Level Pulse Width	t_{WCL}	0.7	–	µs	
External Clock Rise and Fall time	tr, tf	–	0.1	µs	

Note: Measured by test circuit 2 (figure 39).

2. LCD Interface Timing (figure 38)

item			Symbol	Min	Max	Notes
$\overline{M}$/S = 0	CL1	High-Level Pulse Width	$t_{WCH}1$	35	–	1, 4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}1$	35	–	1, 4, 5
	FLM	Delay Time	$t_{DFL}1$	–2.0	+2.0	4, 5
	FLM	Hold Time	$t_{HFL}1$	–2.0	+2.0	4, 5
	M Output Delay Time		$t_{DMO}1$	–2.0	+2.0	4, 5
$\overline{M}$/S = 1	CL1	High-Level Pulse Width	$t_{WCH}2$	35	–	4, 5
	CL1	Low-Level Pulse Width	$t_{WCL}2$	11 × t_{CYC}	–	2, 4, 5
	FLM	Delay Time	$t_{DFL}2$	–2.0	1.5 × t_{CYC}	3, 4, 5
	FLM	Hold Time	$t_{HFL}2$	–2.0	+2.0	4, 5
	M Delay Time		t_{DMI}	–2.0	+2.0	4, 5

Notes:
1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6 V) or 75 kΩ (V_{CC} = 2.7 to 4.0 V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is 19 × t_{CYC} in other cases.
3. When bits FFS are set for 1 or 2. The value is 8.5 × t_{CYC} in other cases.
4. Measured by test circuit 2 (figure 39).
5. Units are µs.

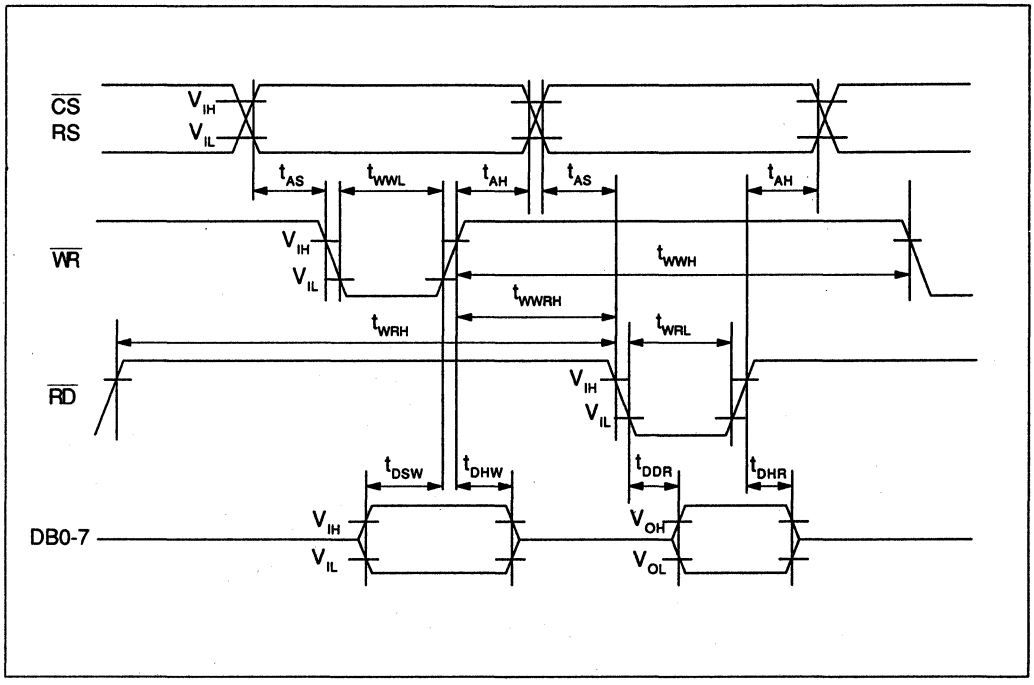

Figure 37 CPU Bus Timing

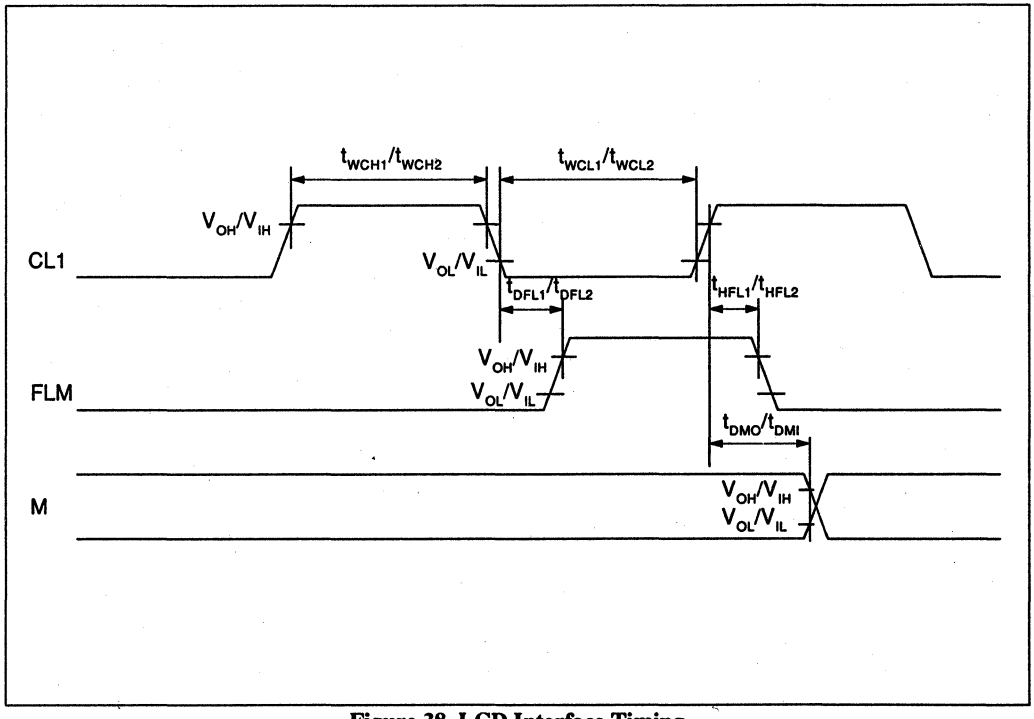

Figure 38 LCD Interface Timing

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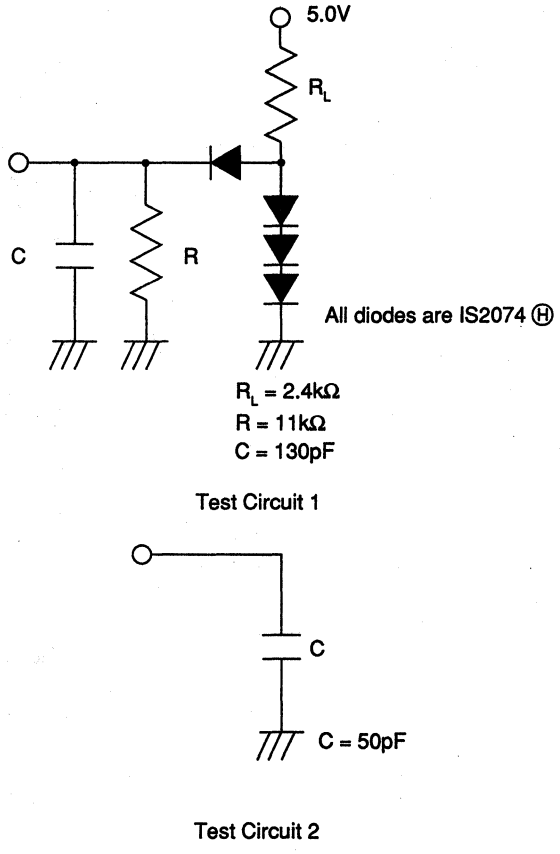
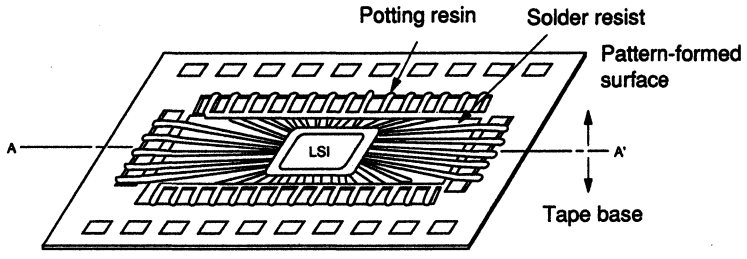


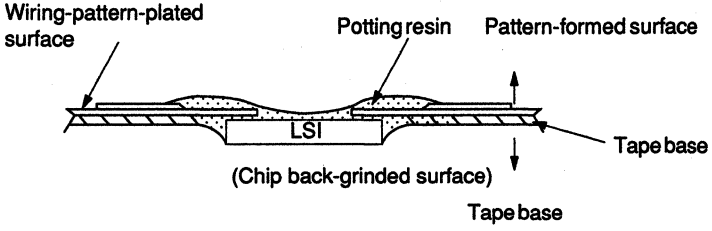
Figure 39 Load Circuits

TCP Sketches and Mounting

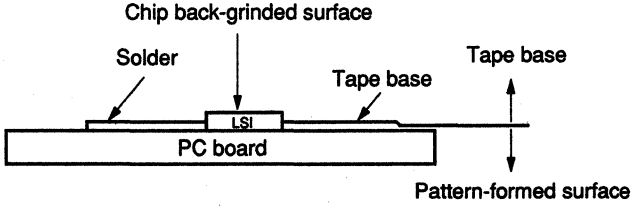
The following shows TCP sketches and TCP mounting on a printed circuit board. These drawings do not restrict TCP shape.



TCP Rough Sketch



A-A' Cross-Sectional View



TCP Mounting on PC Board

5

HD66840F

LCD Video Interface Controller (LVIC)

For Maintenance Only

For new designs please see data sheet for HD66841F

Description

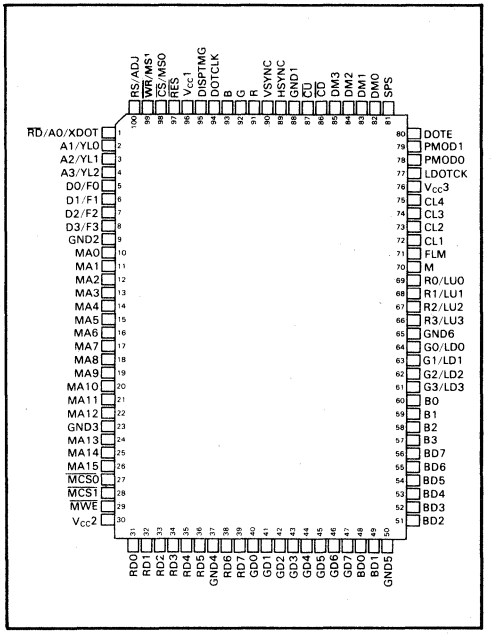
The HD66840F LVIC interface controller converts the standard video signals R, G, B for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes. It also enables the software originally intended for CRT display to control the LCD.

Since the LVIC can control TFT-type LCDs in addition to the current TN-type LCD, it can support color display as well as monochrome display. It can program screen size and can control a large-panel LCD of 720 dots × 512 dots (max).

Features

- Converts video R, G, B signals for CRT display into LCD data:
  - —Monochrome display data
  - —8-level gray scale display data
  - —8-color display data
- Can select LVIC control method:
  - —Pin programming method
  - —Internal register programming method (either with MPU or ROM)
- Can program screen size:
  - —200, 350, 400, 480, 512, or 540 dots (lines) in height and 640, or 720 dots (80, or 90 characters) in width by pin programming method
  - —4-1024 dots (lines) in height and 32-4048 dots (4-506 characters) in width by internal register programming method
- Can regenerate the display timing signal from HSYNC and VSYNC
- Internal PLL circuit can generate the dot clock (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Can control both TN-type LCD and TFT-type LCD
- Maximum operating frequency: 25 MHz (dot clock for CRT display)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, B) parallel data transfer
- Recommended LCD drivers: HD61104 (column) and HD61105 (common), HD66204 (column) and HD66205 (common), HD66106 and HD66107T (column/common)
- CMOS 1.3 μm process
- Single power supply: +5 V ± 10 %
- 100-pin plastic QFP (FP-100A)

Pin Arrangement



Ordering Information

Type No.	Dot clock (MHz)	Package
HD66840F	25 MHz	100-pin Plastic QFP (FP-100A)

Pin Description

Table 1 describes the pins.

Table 1 Pin Description

Symbol	Pin Number	Pin Name	I/O
$V_{CC}1$-$V_{CC}3$	96, 30, 76	$V_{CC}1$, V_{CC} 2, V_{CC} 3	—
GND1-GND6	88, 9, 23, 37, 50, 65	Ground 1-6	—
R, G, B[1]	91, 92, 93	Red, green, blue serial data	I
HSYNC	89	Horizontal synchronization	I
VSYNC	90	Vertical synchronization	I
DISPTMG[2]	95	Display timing	I
DOTCLK	94	Dot clock	I
R0-R3[3] LU0-LU3[4]	69-66 69-66	LCD red data 0-3 LCD up panel data 0-3	O O
G0-G3[3,5] LD0-LD3[4,5]	64-61 64-61	LCD green data 0-3 LCD down panel data 0-3	O O
B0-B3[3,6]	60-57	LCD blue data 0-3	O
CL1	72	LCD data line clock	O
CL2	73	LCD data shift clock	O
CL3[7]	74	Y-driver shift clock 1	O
CL4[7]	75	Y-driver shift clock 2	O
FLM	71	First line marker	O
M	70	LCD driving signal alternation	O
LDOTCK	77	LCD dot clock	I
$\overline{MCS0}$, $\overline{MCS1}$[8]	27, 28	Memory chip select 0, 1	O
$\overline{MWE}$[9]	29	Memory write enable	O
MA0-MA15[9]	10-22, 24-26	Memory address 0-15	O
RD0-RD7[9]	31-36, 38-39	Memory red data 0-7	I/O
GD0-GD7[9,10]	40-47	Memory green data 0-7	I/O
BD0-BD7[9,10]	48, 49 51-56	Memory blue data 0-7	I/O

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Table 1 Pin Description (cont)

Symbol	Pin Number	Pin Name	I/O
PMOD0, PMOD1	78, 79	Program mode 0, 1	I
DOTE	80	Dot clock edge change	I
SPS	81	Synchronization polarity select	I
DM0-DM3	82-85	Display mode 0-3	I
$\overline{CS}$ (MPU programming)[11]	98	Chip select	I
MS0 (pin programming)[11]	98	Memory select 0	I
$\overline{WR}$ (MPU programming)[11,12]	99	Write	I
MS1 (pin programming)[11]	99	Memory select 1	I
$\overline{RD}$ (MPU programming)[12]	1	Read	I
A0 (ROM programming)	1	Address 0	O
XDOT (pin programming)	1	X-dot	I
RS (MPU programming)[11]	100	Register select	I
ADJ (pin programming)[11]	100	Adjust	I
D0-D3 (MPU programming)	5-8	Data 0-3	I/O
D0-D3 (ROM programming)	5-8	Data 0-3	I
F0-F3 (pin programming)	5-8	Fine adjust 0-3	I
A1-A3 (ROM programming)[13]	2-4	Address 1-3	O
YL0-YL2 (pin programming)[13]	2-4	Y-line 0-2	I
$\overline{RES}$[14]	97	Reset	I
$\overline{CD}$	86	Charge down	O
$\overline{CU}$	87	Charge up	O

Notes: 1. When CRT display data is monochrome, G and B pins should be fixed low.
2. Fix high or low when regenerating the display timing signal internally.
3. For 8-color display modes.
4. For monochrome and 8-level gray scale display modes.
5. Leave disconnected in 4-bit/single screen data transfer modes.
6. Leave disconnected in monochrome and 8-level gray scale display modes.
7. Leave disconnected when controlling TN-type LCD.
8. Leave disconnected when using no buffer memories.
9. Leave disconnected when using no buffer memories.
10. In monochrome display modes, the LVIC writes the OR of R, G, B signals into R-plane RAMs. Thus, no RAMs are required for G and B planes in these modes.
Pull up these pins with 20-kΩ resistance. If G and B plane RAMs are connected in monochrome display modes, the LVIC writes G and B signals into each RAM. However, it does not affect the display or the contents of R-plane RAM whether G- and B-plane RAMs are connected or not.
11. Fix high or low when controlling the LVIC by ROM programming method.
12. $\overline{WR}$ and $\overline{RD}$ must not be low at the same time.
13. Fix high or low when controlling the LVIC by MPU programming method.
14. Make sure to input $\overline{RES}$ signal after power-on.

Power Supply

$V_{CC}1$-$V_{CC}3$: Connect $V_{CC}1$-$V_{CC}3$ with +5 V.

GND1-GND6: Ground GND1-GND6.

CRT Display Interface

R, G, B: Input CRT display R, G, B signals on R, G and B respectively.

HSYNC: Input the CRT horizontal synchronization on HSYNC.

VSYNC: Input the CRT vertical synchronization on VSYNC.

DISPTMG: Input the display timing signal, which announces the horizontal or vertical display period, on DISPTMG.

DOTCLK: Input the dot clock for CRT display on DOTCLK.

LCD Interface

R0-R3: R0-R3 output R data for the LCD.

LU0-LU3: LU0-LU3 output LCD up panel data.

G0-G3: G0-G3 output G data for the LCD.

LD0-LD3: LD0-LD3 output LCD down panel data.

B0-B3: B0-B3 output B data for the LCD.

CL1: CL1 outputs the line select clock for LCD data.

CL2: CL2 outputs the shift clock for LCD data.

CL3: CL3 outputs the line select and shift clock when a Y-driver is set on one side of an LCD screen (see "LCD System Configuration").

CL4: CL4 outputs the line select and shift clock when Y-drivers are set on both sides of an LCD screen (see "LCD System Configuration").

FLM: FLM outputs the first line marker for a Y-driver.

M: The M output signal converts the LCD drive signal to AC.

LDOTCK: LDOTCK outputs the LCD dot clock.

Buffer Memory Interface

$\overline{MCS0}$, $\overline{MCS1}$: $\overline{MCS0}$ and $\overline{MCS1}$ output the buffer memory chip select signal.

$\overline{MWE}$: $\overline{MWE}$ outputs the write enable signal of buffer memories.

MA0-MA15: MA0-MA15 output buffer memory addresses.

RD0-RD7: RD0-RD7 transfer data between R data buffer memory and the LVIC.

GD0-GD7: GD0-GD7 transfer data between G data buffer memory and the LVIC.

BD0-BD7: BD0-BD7 transfer data between B data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: The PMOD0-PMOD1 input signals select a programming method (table 6).

DOTE: The DOTE input signal switches the timing of the data latch. The LVIC latches R, G, B signal at the falling edge of DOTCLK when DOTE is high, and at the rising edge when low.

SPS: The SPS input signal selects the polarity of VSYNC. (The polarity of HSYNC is fixed.) VSYNC is high active when SPS is high, and low active when low.

DM0-DM3: The DM0-DM3 input signals select a display mode (table 8).

MS0-MS1: The MS0-MS1 input signals select the kind of buffer memories (table 2).

XDOT: The XDOT input signal specifies the number of horizontal displayed characters. The number is 90 when XDOT is high, and 80 when low.

YL0-YL2: The YL0-YL2 input signals specify the number of vertical displayed lines (table 3).

ADJ: The ADJ input signal determines whether F0-F3 pins adjust the number of vertical displayed lines or the display timing signal. F0-F3 pins adjust the display timing signal when ADJ is high, and adjust the number of vertical displayed lines when low.

F0-F3: F0-F3 input data for adjusting the number of vertical displayed lines (table 4), or the display timing signal (see "Fine

Adjustment of Display Timing Signal").

MPU Interface

$\overline{CS}$: The MPU selects the LVIC when $\overline{CS}$ is low.

$\overline{WR}$: The MPU inputs the $\overline{WR}$ write signal to write data into internal registers of the LVIC. The MPU can write data when $\overline{WR}$ is low and cannot write data when high.

$\overline{RD}$: The MPU inputs the $\overline{RD}$ read signal to read data from internal registers of the LVIC. The MPU can read data when $\overline{RD}$ is low and cannot read data when high.

RS: The MPU inputs the RS signal together with $\overline{CS}$ to select internal registers. The MPU selects data registers (R0-R15) when RS is high and $\overline{CS}$ is low, and selects the address register (AR) when RS is low and $\overline{CS}$ is low.

D0-D3: D0-D3 transfer internal register data between the MPU and LVIC.

$\overline{RES}$: $\overline{RES}$ inputs the external reset signal.

ROM Interface

A0-A3: A0-A3 output address 0 to address 3 to an external ROM.

D0-D3: D0-D3 input data from an external ROM to internal registers.

PLL Circuit Interface

$\overline{CD}$: $\overline{CD}$ outputs the charge down signal to an external charge pump.

$\overline{CU}$: $\overline{CU}$ outputs the charge up signal to an external charge pump.

Table 2 Memory Type and MS1, MS0 Pins

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes memory
1	0	32-kbytes memory
1	1	64-kbytes memory

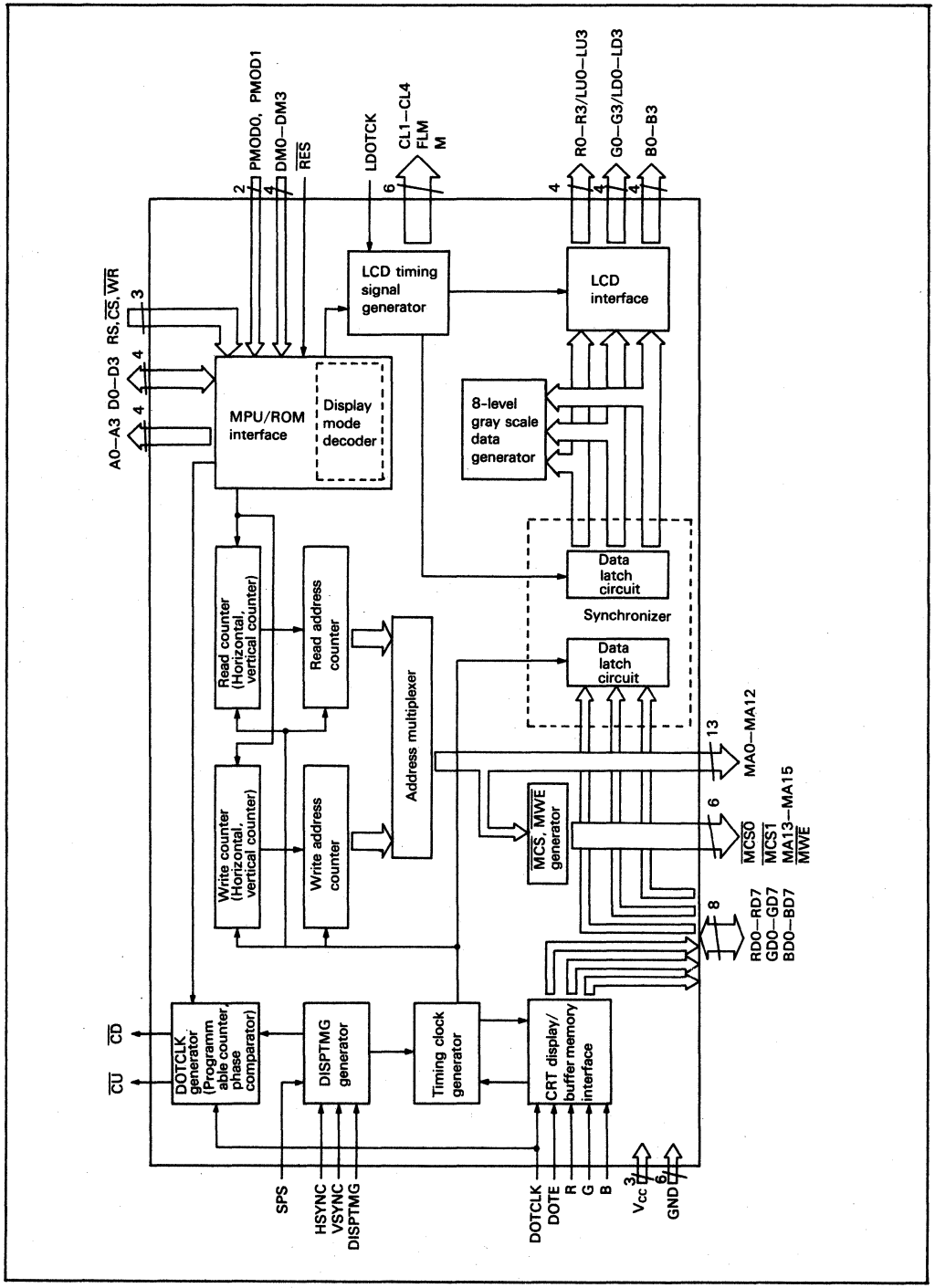
Table 3 Number of Vertical Displayed Lines and YL0-YL2 Pins

YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Prohibited
1	1	1	

Table 4 Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Lines Adjusted
0	0	0	0	± 0
0	0	0	1	+ 1
0	0	1	0	+ 2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+ 14
1	1	1	1	+ 15

Internal Block Diagram



Registers

Table 5 lists the internal registers and figure 1 illustrates the bit assignment to the registers.

Table 5 Register List

		Address Register				Reg.		Program	Read/
$\overline{CS}$	RS	3	2	1	0	No.	Register Name	Unit	Write
1	—	—	—	—	—	—	Invalid	—	—
0	0	—	—	—	—	AR	Address register[1]	—	W
0	1	0	0	0	0	R0	Control register 1	—	R/W
0	1	0	0	0	1	R1	Control register 2	—	R/W
0	1	0	0	1	0	R2	Vertical displayed lines register (middle-order)[2]	Line	R/W
0	1	0	0	1	1	R3	Vertical displayed lines register (low-order)[2]	Line	R/W
0	1	0	1	0	0	R4	Vertical displayed lines register (high-order)[2]	Line	R/W
							CL3 period register (high-order)[3]	Char	R/W
0	1	0	1	0	1	R5	CL3 period register (low-order)[3]	Char	R/W
0	1	0	1	1	0	R6	Horizontal displayed characters register (high-order)[4]	Char	R/W
0	1	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Char	R/W
0	1	1	0	0	0	R8	CL3 pulse width register	Char	R/W
0	1	1	0	0	1	R9	Fine adjust register[5]	Dot	R/W
0	1	1	0	1	0	R10	PLL frequency-dividing ratio register (high-order)[6]	—	R/W
0	1	1	0	1	1	R11	PLL frequency-dividing ratio register (low-order)[6]	—	R/W
0	1	1	1	0	0	R12	Vertical backporch register (high-order)[2,7]	Line	R/W
0	1	1	1	0	1	R13	Vertical backporch register (low-order)[2,7]	Line	R/W
0	1	1	1	1	0	R14	Horizontal backporch register (high-order)[2,7]	Dot	R/W
0	1	1	1	1	1	R15	Horizontal backporch register (low-order)[2,7]	Dot	R/W

Notes: 1. If you attempt to read data from the register with RS = 0, the bus is driven to high-impedance state and the output data is indefinite.
2. (The specified value − 1) should be written into these registers.
3. Valid only in 8-color display modes with horizontal stripes.
4. The most significant bit is invalid in dual screen configuration modes.
5. Valid only when the display timing signal is supplied externally.
6. Valid only when generating the dot clock.
7. Valid only when generating the display timing signal internally.

Register No.	Data Bit				
	3	2	1	0	
—					
AR	Address register				
R0			DSP	DCK	← Control register 1
R1	MC	DON	MS1	MS0	← Control register 2
R2	Vertical displayed				
R3	lines register				
R4					
R5	CL3 period register				
R6	Horizontal displayed				
R7	characters register				
R8	CL3 pulse width register				
R9	Fine adjust register				
R10	PLL frequency-				
R11	dividing ratio register				
R12	Vertical Backporch				
R13	register				
R14	Horizontal Backporch				
R15	register				

Note: ▨ indicates invalid bits. Attempting to read data from these register bits returns indefinite output data.

Figure 1 Register Bit Assignment

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System Configuration

Figure 2 is the block diagram of a system in which the LVIC is used outside of a personal computer.

The LVIC converts the R, G, B serial data sent from the personal computer into parallel data and writes them into the buffer memories once. It reads out the data in turn and outputs them to LCD drivers to drive an LCD. Here the latch clock of the serial data, namely the dot clock (DOTCLK) is generated by a PLL circuit, using HSYNC as a basic clock. The frequency of the dot clock is specified by the PLL frequency-dividing ratio register (R10, R11).

The user may also configure a system without VCO and LPF if supplying the dot clock externally and may configure a system without the MPU if the LVIC is controlled by the pin programming method.

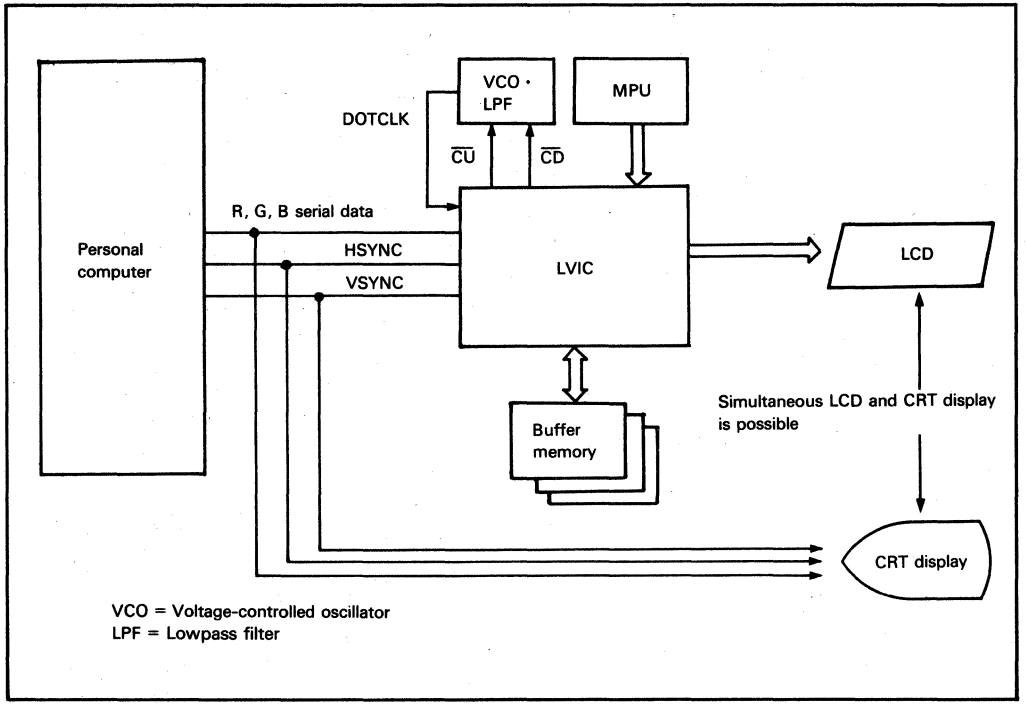

Figure 2 System Block Diagram (MPU Programming Method, Regenerates DOTCLK)

Functional Description

Programming Method

The user may select one of two methods to control the LVIC functions: by pin programming method or by internal registers (internal register programming method). The internal register programming method can be divided into the MPU programming method and the ROM programming method. The MPU writes data into internal registers in the MPU programming method and ROM writes the data in the ROM programming method. Table 6 lists the relation between programming method and pins.

Pin Programming Method: LVIC mode setting pins control functions in the pin programming method.

Internal Register Programming Method: In the internal register programming method, an MPU or ROM writes data into internal registers to control functions. Figure 3 illustrates the connections of MPU or ROM and the LVIC. Figure 3 (1) is an example of using a 4-bit microprocessor, but since the LVIC's MPU bus is compatible with the 4-MHz 80-family controller bus, it can also be connected directly with the bus of host MPU.

Table 6 Programming Method Selection

Pins			
PMOD1	**PMOD0**	**Programming Method**	
0	0	Pin programming	
0	1	Internal register	With MPU
1	0	Programming	With ROM
1	1	Prohibited (Note)	

Note: This combination is for a test mode and disables display.

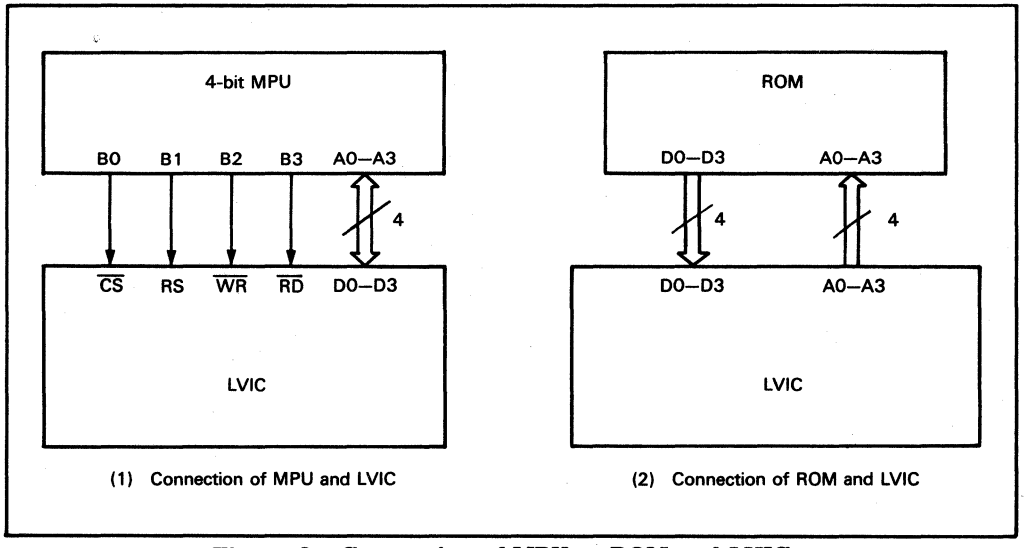

Figure 3 Connection of MPU or ROM and LVIC

5

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, the user may select either 640 dots or 720 dots (80 characters or 90 characters) as the number of horizontal displayed characters with the XDOT pin, and 200, 350, 400, 480, 512, or 540 lines as the number of vertical displayed lines with YL2-YL0 pins. The number of vertical displayed lines can be adjusted with ADJ and F3-F0 pins within +0 to +15 lines.

In the internal register programming method, the user may select any even number from 32 dots to 4048 dots (= 4 characters up to 506 characters) with the horizontal displayed characters register (R6, R7), and any even number from 4 lines up to 1028 lines with the vertical displayed lines register (R2, R3 and the high-order two bits of R4). However, odd number of lines can also be selected when screen configuration is single and a Y-driver (scan driver) is set on one side of an LCD screen.

Figure 4 illustrates the relation between an LCD screen and pins and internal registers controlling screen size.

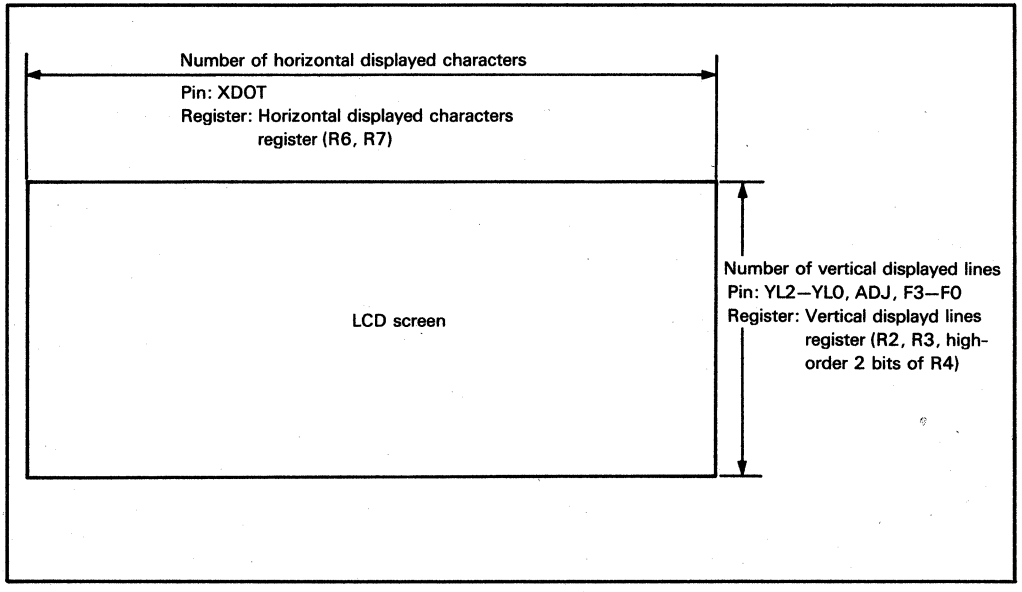

Figure 4 Relation between LCD Screen and Pins and Internal Registers

Memory Selection

The user may select 8-, 32-, or 64-kbyte SRAMs as buffer memory for the LVIC. Since the LVIC has a chip selector for these memories, no external decoder is required. The user selects the memory with pins MS1 and MS0 or with data bits MS1 and MS0 of the control register 2 (R1). Table 7 lists the kinds of memories and pin address assignments.

Memory capacity required depends on screen size and can be obtained with the following expression:

Memory capacity (bytes) = Nhd × Nvd
Nhd: number of horizontal displayed characters
Nvd: number of vertical displayed lines

For example, a screen of 640 × 200 dots requires 16-kbyte memory capacity since 80 characters × 200 lines is 16 kbytes. (8 dots compose a character.) Therefore, each plane needs two HM6264s, which have 8-kbyte memory capacity, in 8-level gray scale display modes. Connect $\overline{MCS0}$ with one of the memories of each plane and $\overline{MCS1}$ with the other (figure 5 (a)).

When the screen size is 640 × 400 dots, 32-kbyte memory capacity is required (figure 5 (b)). Therefore, each plane needs a HM62256, which have 32-kbyte memory capacity.

Connect $\overline{MCS0}$ with $\overline{CS}$ of the memories here.

Table 7 Memories and Pin Address Assignment

Pins or Bits					
MS1	**MS0**	**Memory**	**Address Output Pins**	**Chip Select Pins**	**Address Assignment**
0	0	No memory[1]	—	—	—
0	1	8-kbytes	MA0-MA12	$\overline{MCS0}$	$0000-$1FFF
				$\overline{MCS1}$	$2000-$3FFF
				MA13	$4000-$5FFF
				MA14	$6000-$7FFF
				MA15	$8000-$9FFF
1	0	32-kbytes	MA0-MA14	$\overline{MCS0}$	$00000-$07FFF
				$\overline{MCS1}$	$08000-$0FFFF
				MA15	$10000-$17FFF
1	1	64-kbytes	MA0-MA15	$\overline{MCS0}$	$00000-$0FFFF
				$\overline{MCS1}$	$10000-$1FFFF

Note: 1. There are some limitations when the user uses no memory. Refer to "User Precautions."

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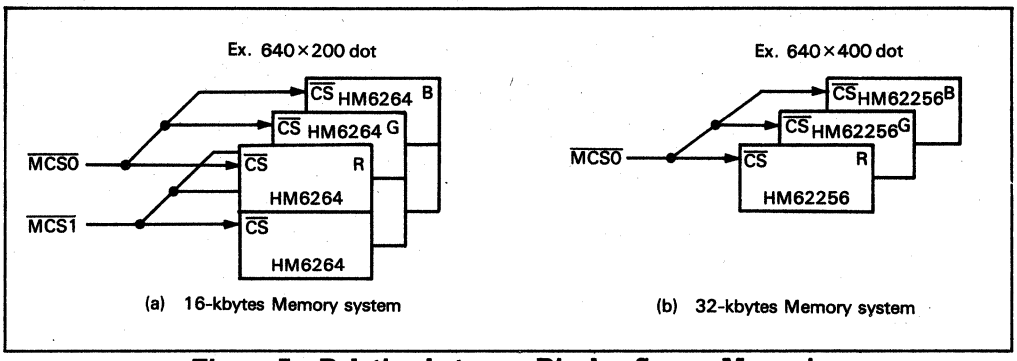

Figure 5 Relation between Display Screen Memories

Display Modes

The LVIC supports 16 display modes, depending on the state of the DM3-DM0 pins. The display mode consists of display color, type of LCD data output, how to set LCD drivers around an LCD screen, how to arrange color data (= type of stripes), and how to output M signal (= type of alternating signal). Table 8 lists display modes.

Table 8 Modes List

Mode	Pins				Display	LCD Data Output		LCD Driver Setting			
						Data	Screen				
No.	DM3	DM2	DM1	DM0	Color	Transfer	Config.	X-Driver[2]	Y-Driver[3]	Stripe[4]	Alternating
1	0	0	0	0	Monochrome	4-bits	Dual	One side	One side	—	Per frame
2	0	0	0	1			Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bits			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level	4-bits	Dual		One side		
7	0	1	1	0	gray scale		Single				
8	0	1	1	1		8-bits					
9[1]	1	0	0	0	8-color	12-bits				Vertical	Per line
10[1]	1	0	0	1		(4 bits			Both sides		
11[1]	1	0	1	0		for R,G,B		Both sides	One side		
12[1]	1	0	1	1		each)			Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16[1]	1	1	1	1					Both sides		

Notes: 1. For TFT-type LCD
2. Data output driver
3. Scan driver
4. Refer to "Display Color, 8-Color Display"

5

Display Color

The LVIC converts R, G, B, the color data for CRT display, into the monochrome, 8-level gray scale, or 8-color display data.

Monochrome Display (Mode 1 to Mode 5): In monochrome modes 1-5, the LVIC displays two colors, namely black (= display on) and white (= display off). As shown in table 9, the OR of CRT display R, G, B data determines the display color.

8-Level Gray Scale Display (Mode 6 to Mode 8): In 8-level gray scale modes 6-8, the LVIC thins out data on certain lines to display an 8-level gray scale according to CRT display color (luminosity). Table 10 shows the relation between CRT display color (luminosity) and LCD color (contrast).

8-Color Display (Mode 9 to Mode 16): In 8-color modes 9-16, the LVIC displays 8 colors with red (R), green (G), and blue (B) filters on liquid crystal cells. The eight colors are the same as those provided by CRT display. As illustrated in figure 5, 8-color display has of two stripe modes: horizontal stripe mode and vertical stripe mode. In the former mode, the LVIC arranges R, G, B data horizontally, with horizontal filters. In the latter mode, the LVIC arranges R, G, B data vertically, with vertical filters. Three cells express a dot in both modes.

Table 9 Monochrome Display

CRT Display Data				LCD	
R	G	B	CRT Display Color	On/Off	Color
1	1	1	White	On	Black
1	1	0	Yellow	On	Black
0	1	1	Cyan	On	Black
0	1	0	Green	On	Black
1	0	1	Magenta	On	Black
1	0	0	Red	On	Black
0	0	1	Blue	On	Black
0	0	0	Black	Off	White

Table 10 8-Level Gray Scale Display

CRT Display Data			CRT		LCD	
R	G	B	Color	Luminosity	Color	Contrast
1	1	1	White	High	Black	Strong
1	1	0	Yellow			
0	1	1	Cyan			
0	1	0	Green			
1	0	1	Magenta			
1	0	0	Red			
0	0	1	Blue			
0	0	0	Black	Low	White	Weak

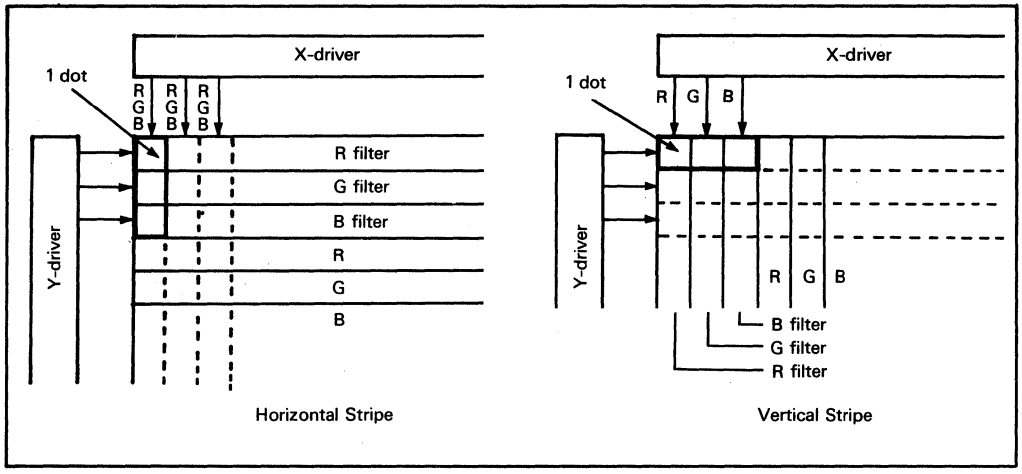

Figure 6 Stripe Modes in 8-Color Display

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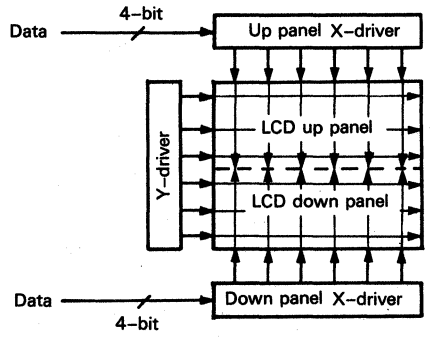
LCD System Configuration

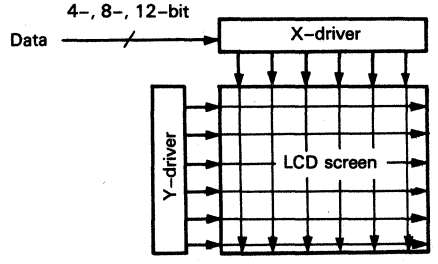
The LVIC supports the following system configurations for LCD:

- Types of LCD data output:
  —Data transfer: 4-bit, 8-bit, or 12-bits (4 bits for R, G, B each)
  —Screen configuration: Single or dual
- How to set LCD drivers around LCD screen:
  —X-driver: On one side or on both sides
  —Y-driver: On one side or on both sides

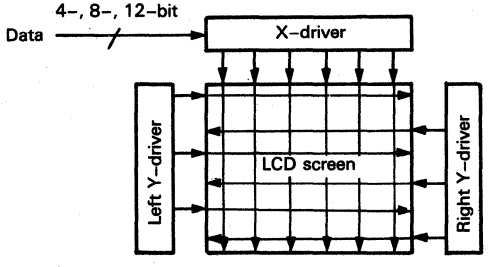
Figure 7 illustrates these system configurations by mode.



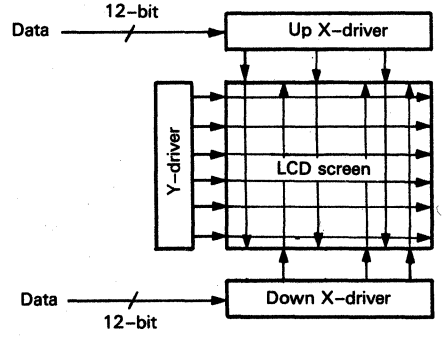
System Configuration for Mode 1 and Mode 6 (4-Bits Data Transfer, Dual Screen, X-Driver and Y-Driver on One Side Each) (Note)



System Configuration for Modes 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-Bits Data Transfer, Single Screen, X-Driver and Y-Driver on One Side Each)



System Configuration for Modes 3, 5, 10, and 14 (4-, 8-, or 12-Bits Data Transfer, Single Screen, X-Driver on One Side and Y-Driver on Both Sides)



System Configuration for Mode 11 and Mode 15 (12-Bits Data Transfer, Single Screen, X-Driver on Both Sides and Y-Driver on One Side)

Note: Although there are two X-drivers, the X-driver is considered to be set on one side, not on both sides, because the LCD up panel and down panel are each regarded as one screen.

Figure 7 System Configurations by Mode

Calculation of LDOTCK

LDOTCK frequency f_L is calculated from the following expression:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd: number of horizontal characters displayed on LCD

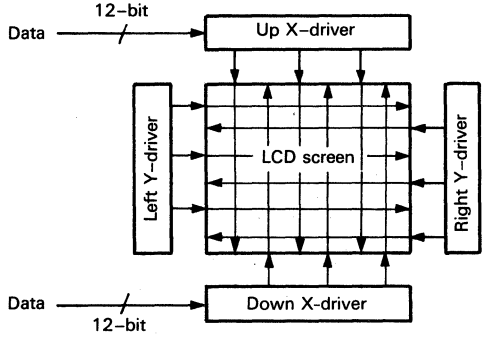
Nvd: number of virtical displayed lines on LCD

f_F: FLM frequency

Here f_L must hold the following relation, where f_D is frequency of dot clock for CRT display (= DOTCLK).

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (The LDOTCK phase must be inverse of the DOTCLK phase in this case)



System Configuration for Mode 12 and Mode 16
(12-Bit Data Transfer, Single Screen, X-Driver and Y-Driver on Both Sides Each)

Notes: 1. X-drivers on both sides: Data output wires run from up and down X-drivers alternately, which widens the interval between wires to twice that for an X-driver an one side (figure 8).

2. Y-drivers on both sides: Line select signal output wires run from right and left Y-drivers alternately, which widens the interval between wires to twice that for Y-driver on one side (figure 9).

Figure 7 System Configurations by Mode (cont)

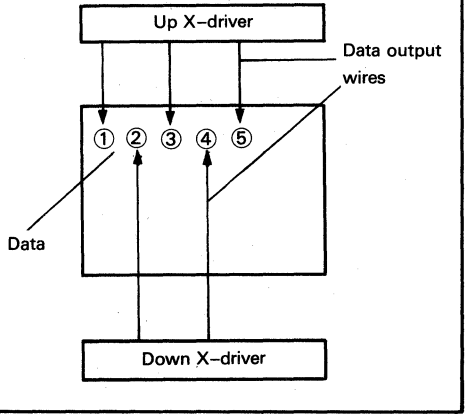


Figure 8 X-Drivers on Both Sides

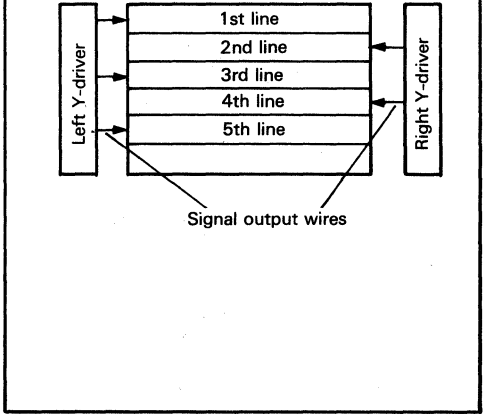


Figure 9 Y-Drivers on Both Sides

Display Timing Signal Generation

CRT display data is classified into display period data and retrace period data. Only display period data is necessary for LCD. Therefore, the LVIC needs a signal announcing whether the CRT display data transferred is for the display period or not. This signal is the display timing signal.

The LVIC can generate the display timing signal from HSYNC and VSYNC. Figure 10 illustrates the relation between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15) respectively.

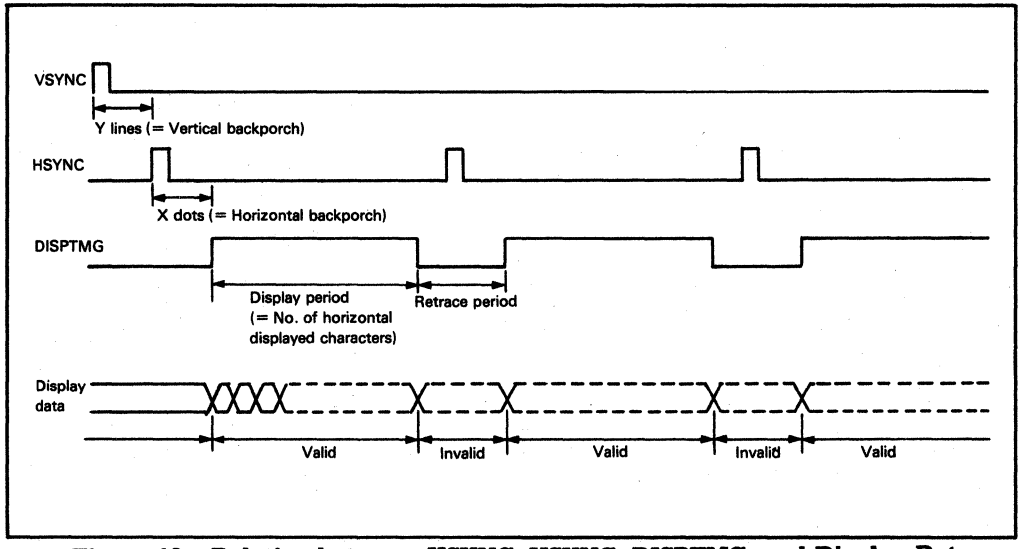


Figure 10 Relation between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal and does not appear from the CRT display plug. Thus it is necessary to generate the dot clock. The LVIC has a programmable counter and a phase comparator which are parts of a PLL circuit, and can generate the dot clock from HSYNC if a charge pump, a lowpass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

Figure 11 is a block diagram of a PLL circuit. A PLL (phase-locked loop) circuit is a feedback controller regenerating a clock whose frequency and phase are the same as those of a basic clock. The basic clock is HSYNC here.

At power-on, VCO outputs to the programmable counter a signal whose frequency depends on the voltage at the time. The counter divides the frequency of the signal according to the value in the PLL frequency-dividing ratio register (R10, R11) and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock and HSYNC and outputs $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs $\overline{CU}$ when the frequency of the clock is lower than that of HSYNC or when the phase of the clock is behind that of HSYNC, while it outputs $\overline{CD}$ in the contrary case. The charge pump and LPF apply voltage to the VCO according to $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and the frequency of the frequency-divided clock coincide with those of HSYNC, making it a stable dot clock.

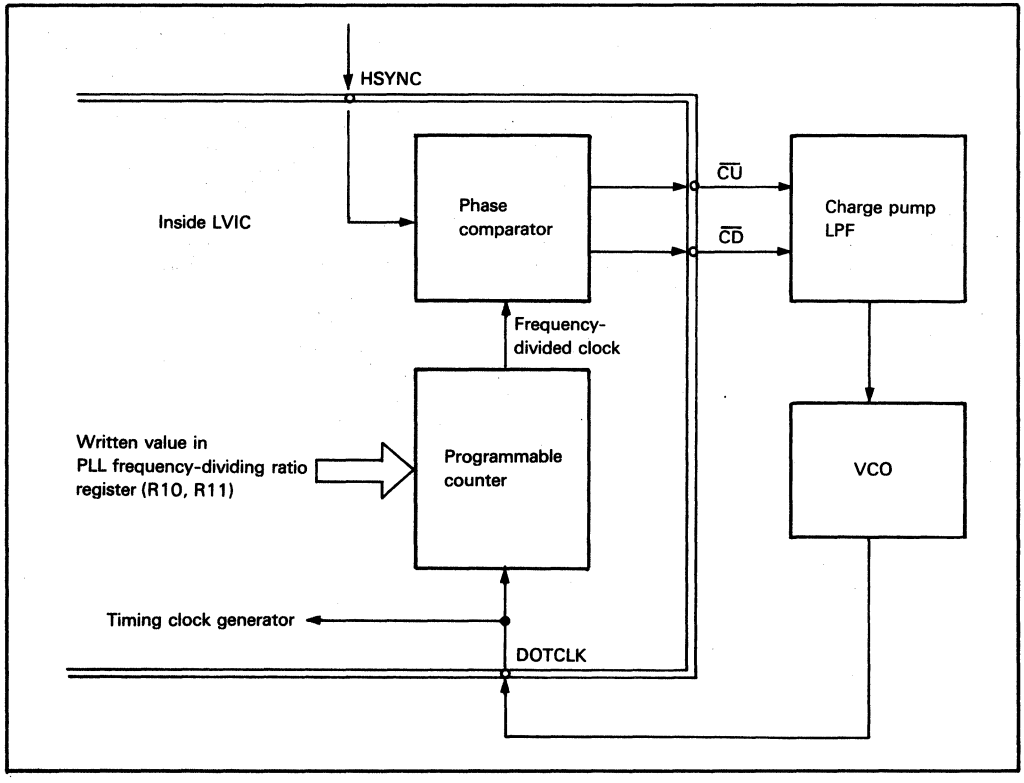


Figure 11 PLL Circuit Block Diagram

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Doubled-in-Height Display

Doubled-in-height display doubles characters and pictures in height as illustrated in figure 12.

In TN-type LCD modes (= modes 1, 2, 4, 6, 7, and 8), CL3 frequency is twice as high as CL1 frequency (figure 13). As a result, using CL3 instead of CL1 as a shift clock (figure 14) enables two lines to be selected while an X-driver (data output driver) is outputting the same data, realizing doubled-in height display. However, the following procedures are necessary in this display since multiplexing duty ratio becomes twice as great as the value specified as the number of vertical displayed lines.

1. Halve the frequency of the LCD dot clock (= LDOTCK)
2. Halve the number of vertical displayed lines

This function is provided only for TN-type LCD.

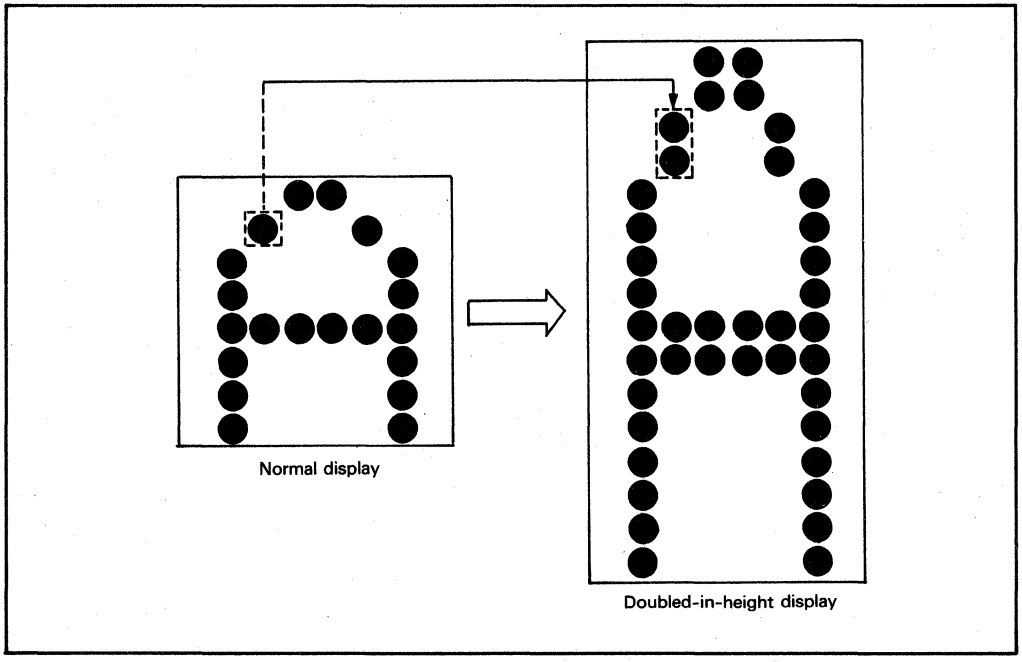

Figure 12 Doubled-in-Height Display Example

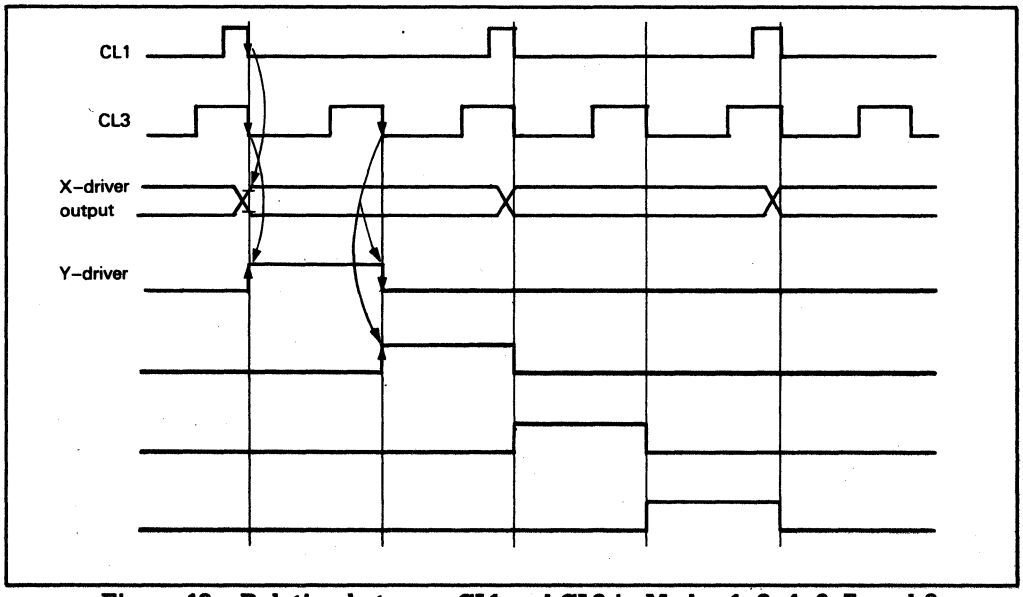

Figure 13 Relation between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

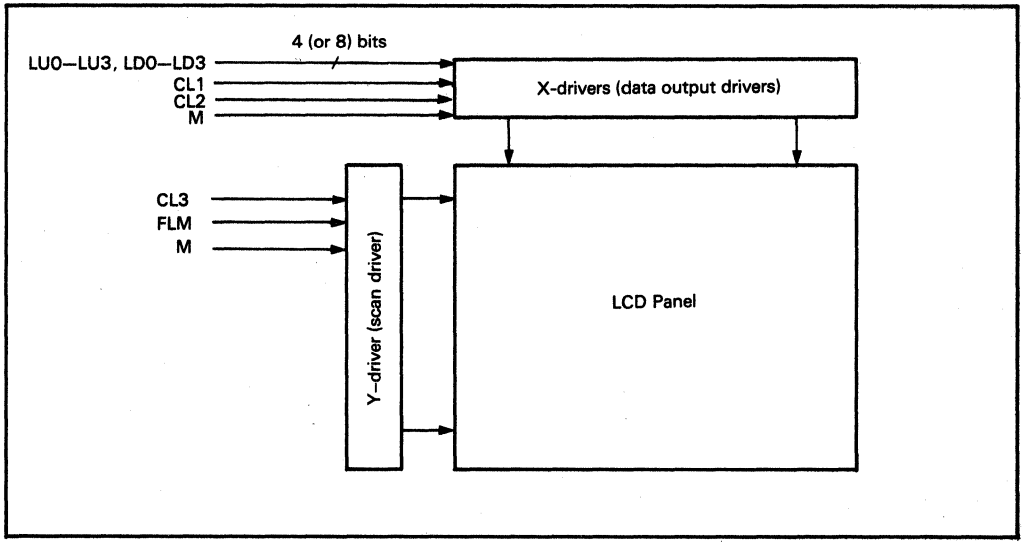

Figure 14 Connection for Doubled-in-Height Display

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Display Timing Signal Fine Adjusment

When the display timing signal is supplied externally, a phase shift might appear between CRT data and the display timing signal. This is because each signal has its own peculiar lag. The LVIC can adjust the display timing signal with the F0-F3 pins or the fine adjust register (R9) to correct this phase shift.

Table 11 shows the relation between F3-F0 pins, data bit 3 to data bit 0 of the fine adjust register, and fine adjustment. Concerning the polarity of the number of dots adjusted, − indicates advancing the phase of the display timing signal and + indicates delaying it. F3 pin or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Figure 15 shows examples of adjusting the display timing signal. Since the signal is two dots ahead of the display start position in case (1), (F3, F2, F1, F0) or (data bits 3, 2, 1, 0 of R9) should be set to (1, 0, 1, 0) to delay the signal for two dots. Since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal for two dots. When there is no need to adjust the signal, settings of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 11 Pins, Data Bits of R9, and Fine Adjustment

Pin:	F3	F2	F1	F0	Number of Dots
R9 Bit:	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	− 1
		⋮	⋮	⋮	⋮
		1	1	0	− 6
		1	1	1	− 7
	1	0	0	0	0
		0	0	1	+ 1
		⋮	⋮	⋮	⋮
		1	1	0	+ 6
		1	1	1	+ 7

Note: When adjusting the display timing signal with pins, set ADJ pin to 1.

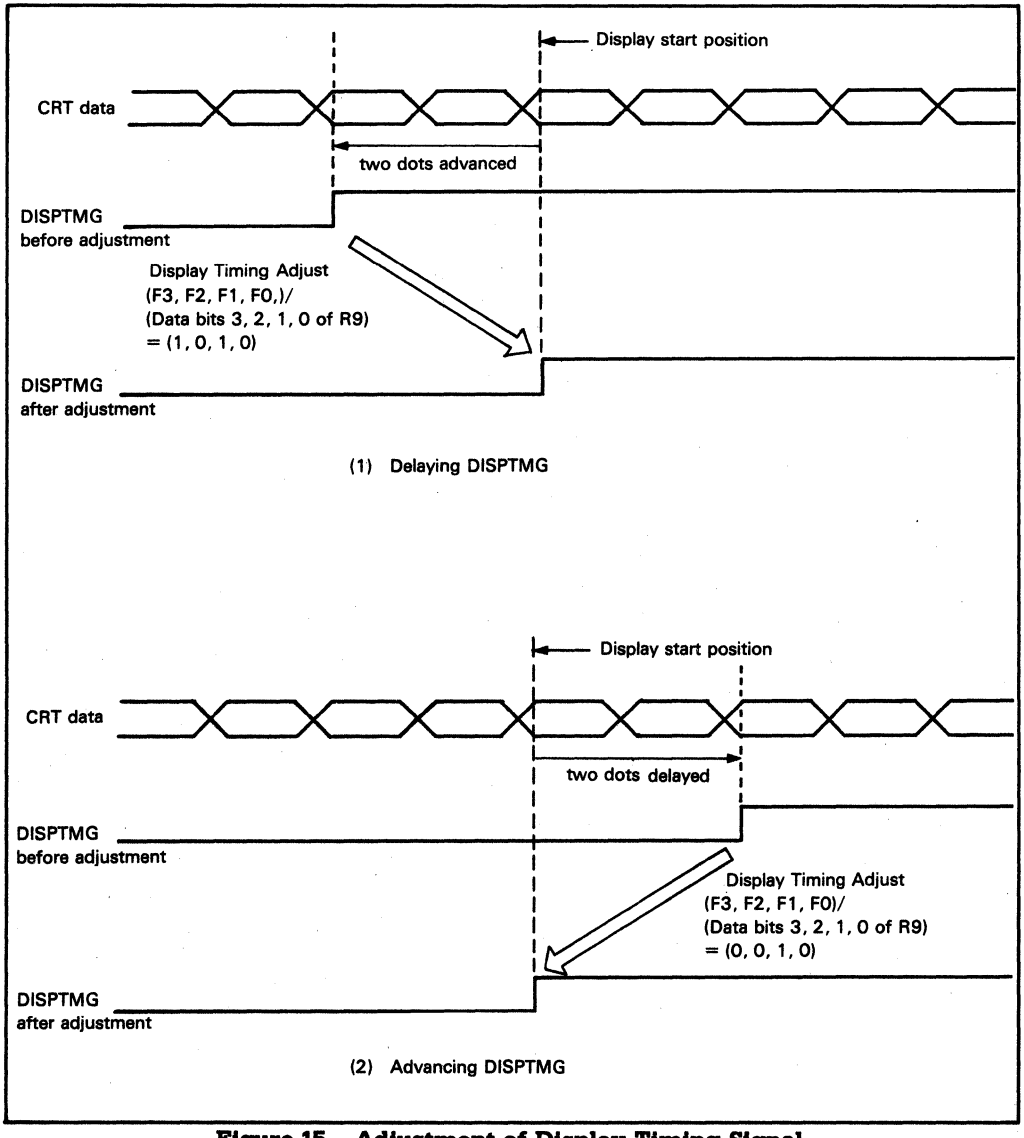

Figure 15 Adjustment of Display Timing Signal

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Internal Registers

The LVIC has an address register (AR) and sixteen data registers (R0-R15). In order to specify one of the sixteen data registers, write its register address into the address register. The MPU transfers data to the data register corresponding to the written address.

All the registers are valid only when the LVIC is controlled by the internal register programming method and are invalid (don't care) when by the pin programming method.

Address Register (AR)

The address register (figure 16) is composed of four bits and specifies one data register out of sixteen. This register is selected by the MPU when RS pin is low and specifies any data register with the register address written by the MPU.

Control Register 1 (R0)

Control register 1 (figure 17) is composed of four bits, including two invalid bits. Each of two valid bits has its own function. Reading from and writing into invalid bits are possible. However, these operations do not affect the LSI function.

- DSP Bit
  —DSP = 1: LVIC generates the display timing signal
  —DSP = 0: LVIC does not generate the display timing signal
  (If DCK = 1, the display timing signal is generated in spite that DSP = 0)

- DCK Bit
  —DCK = 1: LVIC generates the dot clock
  —DCK = 0: LVIC does not generate the dot clock

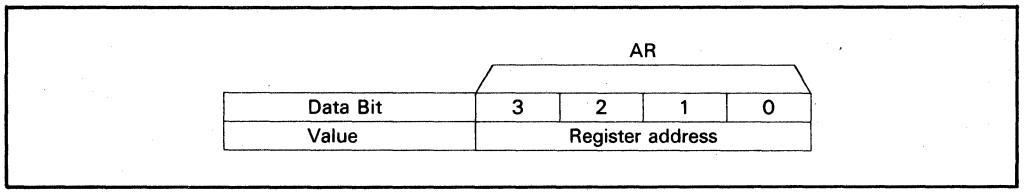


Figure 16 Address Register

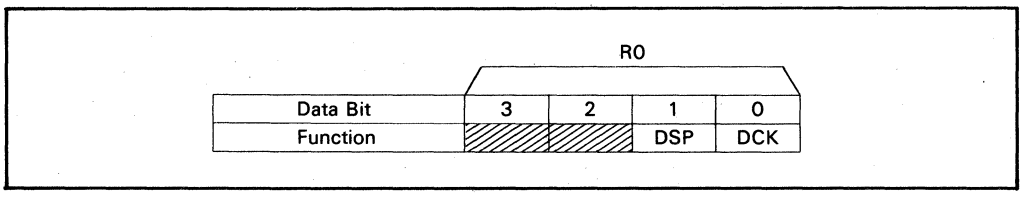


Figure 17 Control Register 1

Control Register 2 (R0)

Control register 2 (figure 18) is composed of four bits and has three functions.

- MC Bit
  —MC = 1: M signal alternates per line
  —MC = 0: M signal alternates per frame
- DON Bit
  —DON = 1: Display on
  —DON = 0: Display off
- MS1 and MS0 Bits
  —Select the memory type (table 12)

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4), CL3 Period Register (Low-order 2 Bits of R4, R5)

The vertical displayed lines register (figure 19) is composed of ten bits (R2 + R3 + high-order two bits of R4) and specifies the number of vertical displayed lines. This register can specify both even and odd numbers in modes for a Y-driver on one side and single screen configuration, but even numbers only in the other modes. The value to be written into this register is (Nvd − 1), where Nvd = number of vertical displayed lines.

The CL3 period register is composed of six bits (low-order two bits of R4 + R5) and specifies the period of CL3 in 8-color display modes with horizontal stripes. Thus this register is invalid in the other modes. CL3 is a clock for the LVIC to output R, G, B data separately to LCD drivers. The value to be written into this register is (Nhd + 6) × 1/3 − 1, where Nhd = number of horizontal displayed characters. When (Nhd + 6) is not divisible by 3, the quotient should be rounded up or rounded down.

Table 12 Memory Type and MS1, MS0

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes
1	0	32-kbytes
1	1	64-kbytes

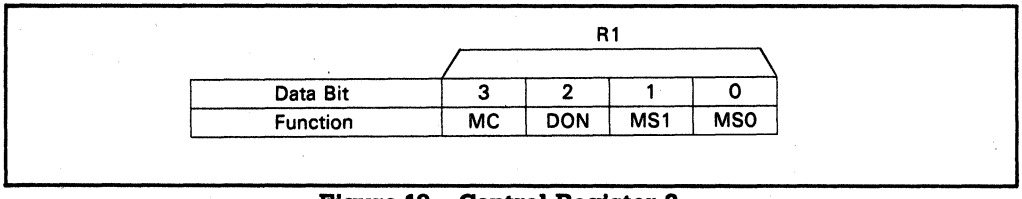


Figure 18 Control Register 2

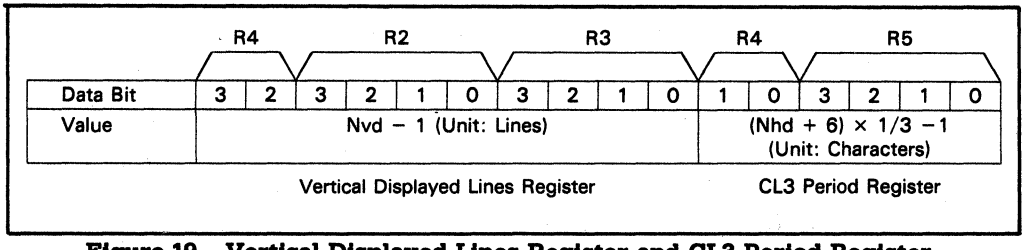


Figure 19 Vertical Displayed Lines Register and CL3 Period Register

Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 20) is composed of eight bits (R6 + R7) and specifies the number of horizontal displayed characters. This register can specify even numbers only. The most significant bit of R6 is invalid in the modes for dual screen configuration. When writing into this register, shift (Nhd − 1) in the low-order direction for one bit to cut off the least significant bit. Figure 20 shows how to write a value into the register when Nhd = 90.

CL3 Pulse Width Register (R8)

The CL3 period register (figure 22) is composed of four bits and specifies the high-level pulse width of CL3. When controlling TFT-type LCDs, each gate of the LCD has to hold data from the time a Y-driver outputs the line select and shift signal to the time an X-driver the outputs next display data. Data must be held while CL3 is high. However, even when the LVIC is not controlling TFT-type LCDs, CL3 appears with the high-level pulse width specified by this register.

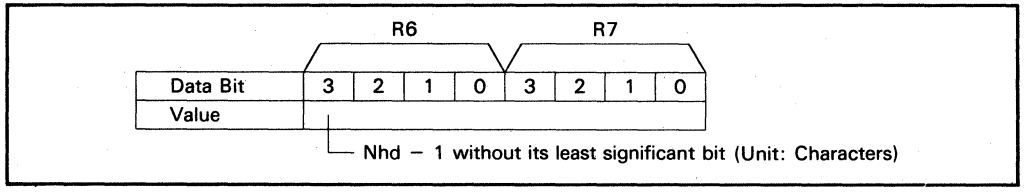


Figure 20 Horizontal Displayed Characters Register

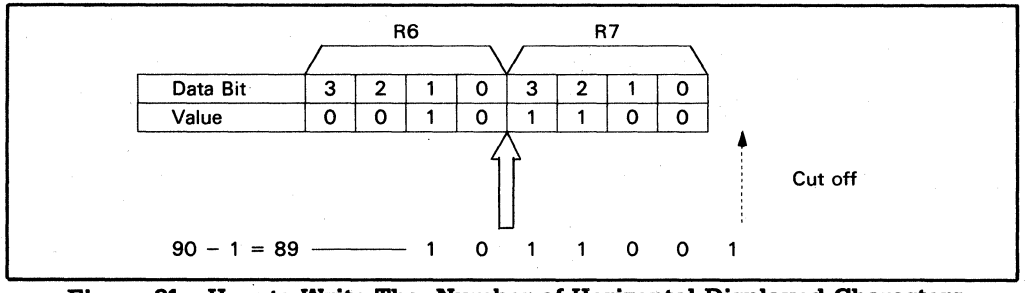


Figure 21 How to Write The Number of Horizontal Displayed Characters

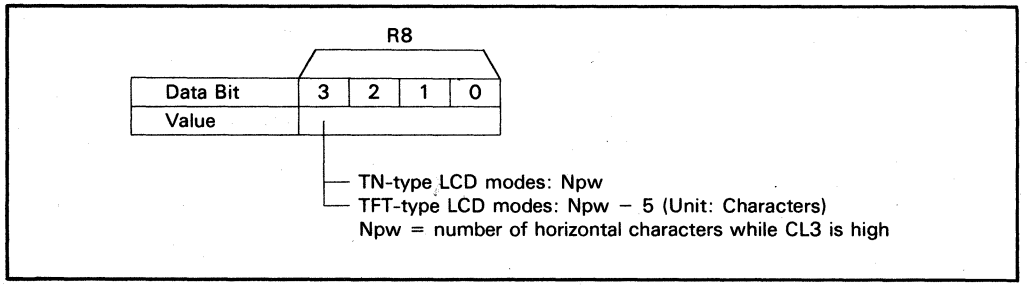


Figure 22 CL3 Pulse Width Register

Fine Adjust Register (R9)

The fine adjust register (figure 23) is composed of four bits and adjusts the externally supplied display timing signal to synchronize its phase with that of LCD data. The value to be written into this register is determined by the interval between the positive edge of the display timing signal and the display start position. For more details, refer to "Display Timing Signal Fine Adjustment." This register is invalid when the display timing signal is generated internally.

PLL Frequency-Dividing Ratio Register (R10, R11)

The PLL frequency-dividing ratio register (figure 24) is composed of eight bits (R10 + R11) and specifies the PLL frequency-dividing ratio for generating a dot clock by a PLL circuit. The value to be written into this register is determined by the ratio of the frequency of HSYNC to that of the dot clock which the user wants. This register is invalid when the dot clock is supplied externally and is valid only when the LVIC is controlled by the internal register programming method and the DCK bit of control register 1 (R0) is 1. The written value in this register (N_{PLL}) is obtained with the following expression:

N_{PLL} = Ncht × 8 − 731
Ncht: total number of characters for CRT
Ncht can be obtained as follows from the specifications of a CRT monitor:
Ncht = 1/8 × (DOTCLK frequency)/(HSYNC frequency)

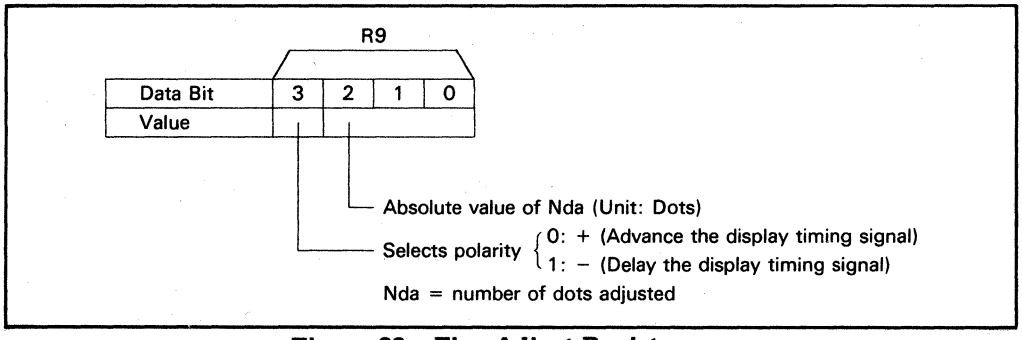
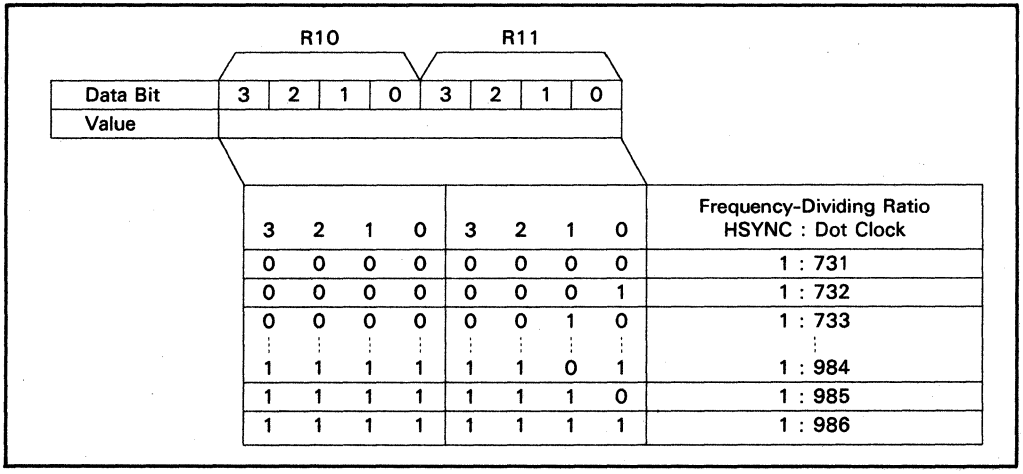


Figure 23 Fine Adjust Register



R10 3	R10 2	R10 1	R10 0	R11 3	R11 2	R11 1	R11 0	Frequency-Dividing Ratio HSYNC : Dot Clock
0	0	0	0	0	0	0	0	1 : 731
0	0	0	0	0	0	0	1	1 : 732
0	0	0	0	0	0	1	0	1 : 733
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	1 : 984
1	1	1	1	1	1	1	0	1 : 985
1	1	1	1	1	1	1	1	1 : 986

Figure 24 PLL Frequency-Dividing Ratio Register

Vertical Backporch Register (R12, R13)

The vertical backporch register (figure 25) is composed of eight bits (R12 + R13) and specifies the vertical backporch. The vertical backporch is the number of lines between the positive edge of VSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation." This register is invalid when the display timing signal is supplied externally and is valid only in a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be regenerated and the register is enabled even when DSP = 0.)

Horizontal Backporch Register (R14, R15)

The horizontal backporch register (figure 26) is composed of eight bits (R14 + R15) and specifies the horizontal backporch. The horizontal backporch is the number of characters between the positive edge of HSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation". This register is invalid when the display timing signal is supplied externally and is valid only in a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be generated and this register is enabled even when DSP = 0.)

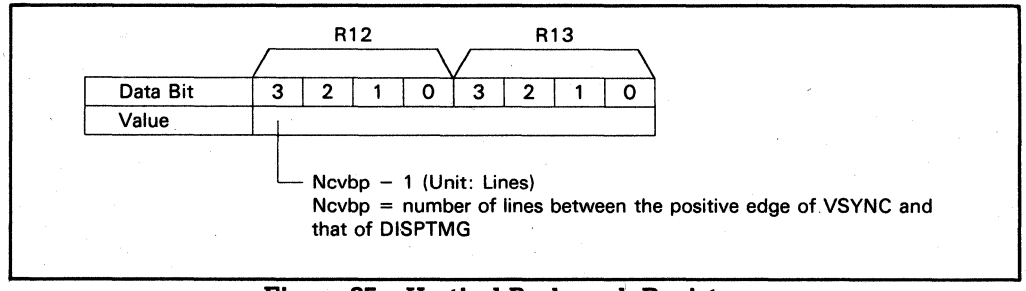


Figure 25 Vertical Backporch Register

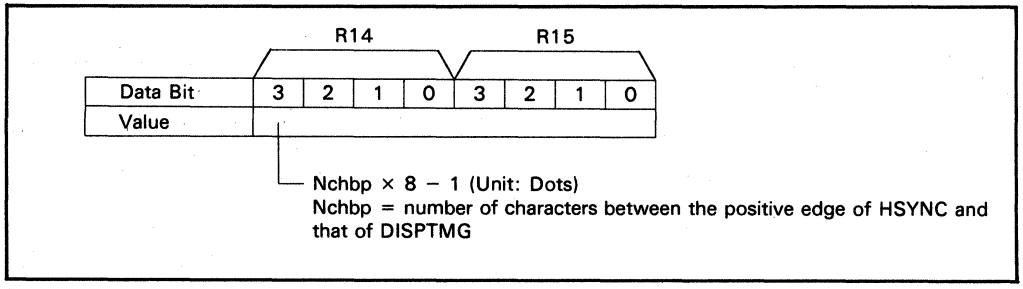


Figure 26 Horizontal Backporch Register

Reset

$\overline{RES}$ pin resets and starts the LVIC. Make sure to hold the reset signal low for at least 1 μs after power-on.

Reset is defined as shown in figure 27.

State of Pins During Reset

$\overline{RES}$ basically does not control output pins and operates regardless of the other input pins. Output pins can be classified into the following five groups depending on their reset state.

1. Keeps state before reset: CL2
2. Driven to high-impedance state (fixed low when using no memory): RD0-RD7, GD0-GD7, BD0-BD7
3. Fixed high: $\overline{MWE}$, CL4, M, $\overline{CD}$, $\overline{MCS1}$
4. Fixed low: MA0-MA12, R0-R3, G0-G3, B0-B3, $\overline{CS}$, CL1, CL3, FLM, A0-A3, $\overline{CU}$
5. Fixed high or low depending on the memory in use (table 13): MA13-MA15, $\overline{MCS0}$

State of Registers During Reset

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be both read and written by the MPU even during reset. Registers keep the contents they had before reset until they are rewritten.

Memory Clear Function

After reset, the LVIC writes 0 in the memory area specified by MSEL0 and MSEL1 (table 7) regardless of R, G, B data.

Table 13 Memory Type and State of Pins During Reset

Kind of Memories	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbyte memory	High	High	High	Low
32-kbyte memory	Low	Low	High	Low
64-kbyte memory	Low	Low	Low	Low

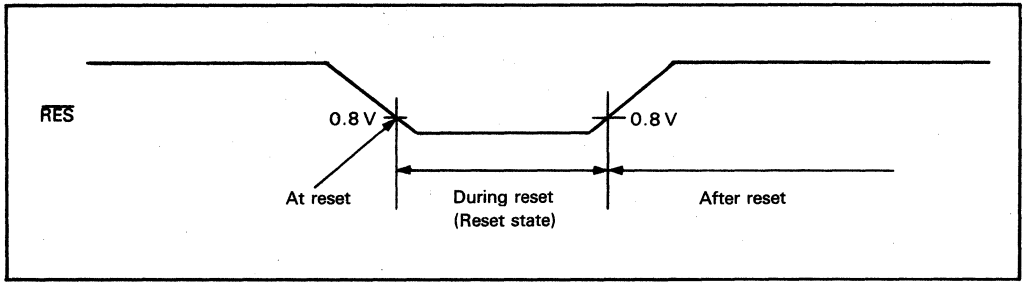


Figure 27 Reset Definition

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User Precautions

1. There are the following limitations when the user uses no memory (MSEL0 = 0, MSEL1 = 1).

   - The display modes for dual screen configuration (= mode 1 and mode 6) are disabled.
   - The LVIC cannot support the LCD systems with Y-drivers on both sides. Even if the user selects the mode for a system with Y-drivers on both sides (= mode 3, 5, 10, 12, 14, or 16), the operation of the LVIC is exactly the same as that in the mode for the system with a Y-driver on one side (= mode 2, 4, 9, 11, 13, or 15).

   Leave CL4 terminal disconnected in this case.

2. The LVIC might operate irregularly until the internal registers have been written after reset in the system which controls the LVIC by internal register programming method.

3. Memory clear function might not work normally at power-on or after reset if MSEL0 and MSEL1 are not properly set to the value corresponding to the memories in use.

4. Since the LVIC is a CMOS LSI, input pins must not be left disconnected. Refer to table 1 concerning how to deal with each pin.

Programming

The values written in internal registers have the limits listed in table 14. The symbols in the table are defined as shown in table 15 and figure 27.

Table 14 Limit on Values Written in Registers

Function	Limit	Notes	Applicable Registers
Screen Configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$		R2, R3, R4, R6, R7
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$	1, 8	
	$(Nhd + 6) \times n \times Nvd \times f_F \leqq f_D \leqq 30$ MHz	2, 8	R2, R3, R4, R6, R7
CL3 Control	$1 \leqq Npw \leqq (Nhd + 6) \times 1/2 - 1$	3	R4, R5, R6, R7, R8
	$1 \leqq Npw \leqq Nhd$	4	
	$1 \leqq Npw \leqq Npc - 1$	5	
DISPTMG	$1 \leqq Nchbp \leqq 256$	6	R12, R13, R14, R15
Regeneration	$1 \leqq Ncvbp \leqq 256$	6	
Without	$4 \leqq Nhd \leqq Nchsp - 4$	7	R2, R3, R4, R6, R7
Buffer Memory	$4 \leqq Nvd \leqq Ncvsp - 4$	7	

Notes: 1. $Nhd \leqq 256$ in dual screen configuration (= mode 1 and mode 6)
2. f_F: FLM frequency, f_D: frequency of CRT dot clock, f_L: frequency of LCD dot clock for LCD $f_L < f_D \times 15/16$, or $f_L = f_D$
3. In modes 1, 2, 4, 6, 7, and 8
4. In modes 3, 5, 9, 10, 11, and 12 (Npw = (value in R8) + 5)
5. In modes 13, 14, 15, and 16 (Npw = (value in R8) + 5)
6. Value in R14, R15 $\leqq$ (Nchsp $\times$ n + Nchbp) $-$ Nhd $\times$ n $-$ 2
   Value in R12, R13 $\leqq$ (Ncvsp + Ncvbp) $-$ Nvd $-$ 2
7. Nht = Nchsp + Nchbp $\times$ 1/n, Nd = Ncvbp + Ncvsp
   (Nht = Nhd + 6, Nd = Nvd when using buffer memory)
8. n: Horizontal character pitch (the number of horizontal dots in one character).

Table 15 Symbol Definition

Symbol	Definition
Nchd	Number of horizontal displayed characters on CRT display
Nchsp	Number of characters between the positive edge of DISPTMG and that of HSYNC (= Horizontal sync position)
Nchbp	Number of dots between the positive edge of HSYNC and that of DISPTMG (= horizontal backporch)
Ncvbp	Number of lines between the negative edge (positive edge when VSYNC is high in active state) of VSYNC and the first positive edge of DISPTMG (= vertical backporch)
Ncvsp	Number of lines between the first positive edge of DISPTMG and the next negative edge of VSYNC (= vertical sync position)
Ncvd	Number of vertical displayed lines on CRT display
Nhd	Number of horizontal displayed characters (on LCD)
Npc	Number of characters during CL3 period (= CL3 pulse cycle)
Npw	Number of characters while CL3 is high (= CL3 pulse width)
Nht	Total number of horizontal characters
Nvd	Number of vertical displayed lines (on LCD)

5

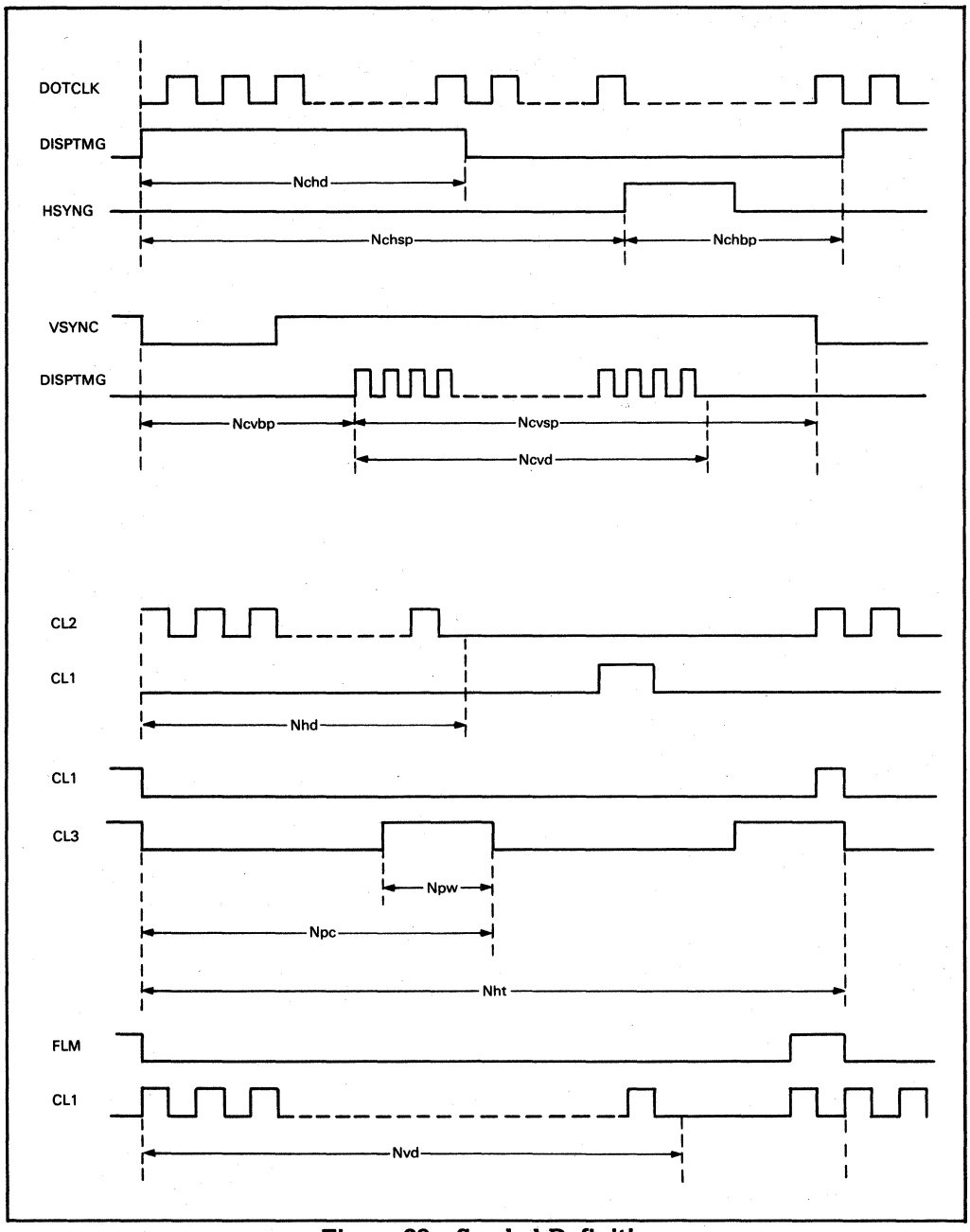

Figure 28 Symbol Definition

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{in}	− 0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	− 20 to + 75	°C
Storage temperature	T_{stg}	− 55 to + 125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of the LSI.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1]		2.0	V_{CC} + 0.3		
	TTL interface[4]		2.2	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1], $\overline{RES}$	V_{IL}	−0.3	0.8	V	
	TTL interface[5]		−0.3	0.6		
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 25 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2
2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4
3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG
4. TTL interface: $\overline{WR}$/MS1, LDOTCK, DOTCLK
5. TTL interface: $\overline{WR}$/MS1

5

DC Characteristics 2 (V_{CC} = 5.0 V ± 5 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1], $\overline{RES}$		2.0	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1]	V_{IL}	−0.3	0.8	V	
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, DOTCLK, LDOTCK, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2

2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

Video Signal Interface

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	40	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	20	—	ns	
DOTCLK low-level pulse width	t_{WDL}	20	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

5

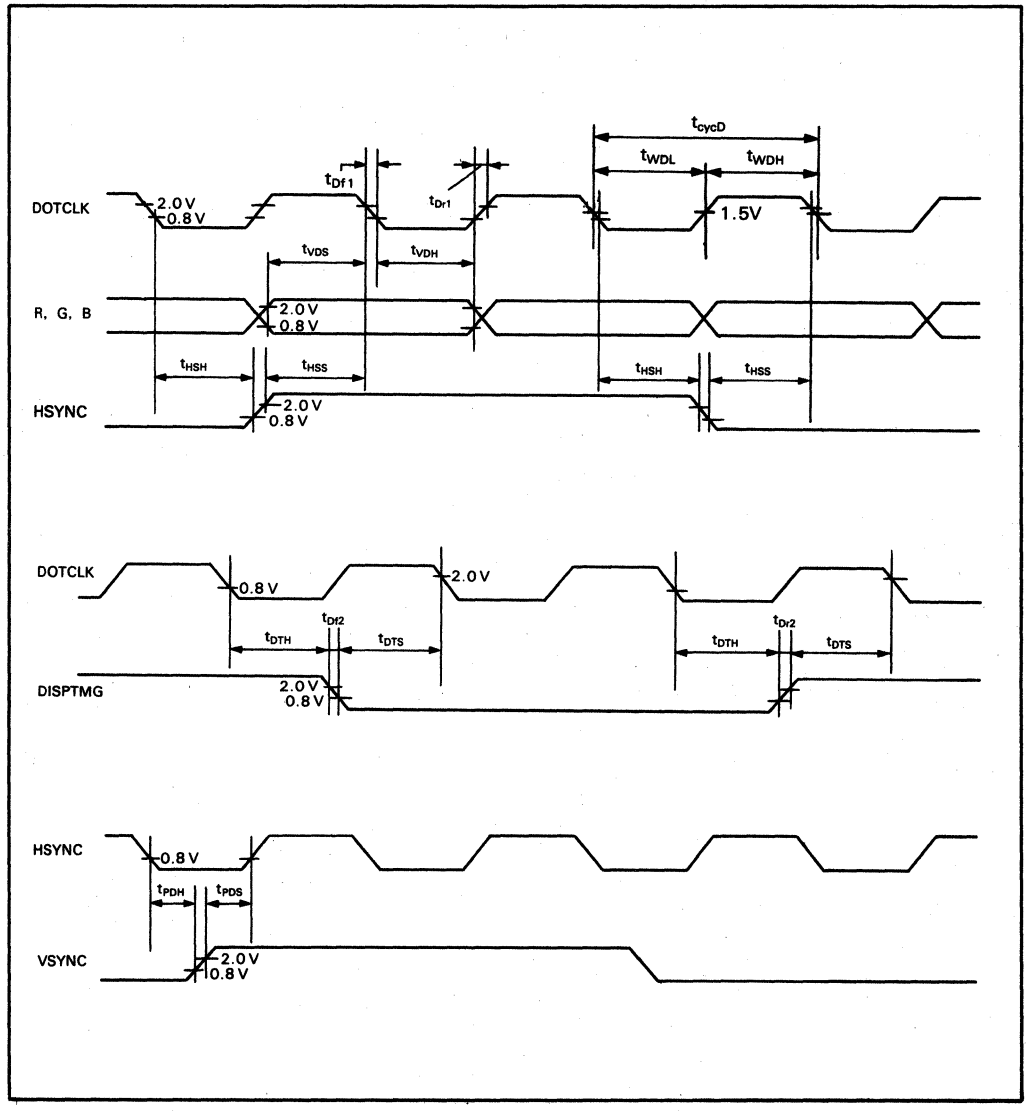

Figure 29 Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	5 t_{CYCD} – 50	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data setup time	t_{SMD}	25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data hold time	t_{HMD}	0	—	ns
Write cycle time	t_{WC}	6 t_{CYCD} – 50	—	ns
Address setup time	t_{AS}	t_{CYCD} – 30	—	ns
Address hold time	t_{WR}	t_{CYCD} – 30	—	ns
Chip select time	t_{CW}	4 t_{CYCD} – 40	—	ns
Write pulse width	t_{WP}	4 t_{CYCD} – 40	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output setup time	T_{SMDW}	2 t_{CYCD} – 25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output hold time	t_{HMDW}	0	—	ns

Note: t_{CYCD} indicates DOTCLK cycle time (min 40 ns, max 1000 ns).

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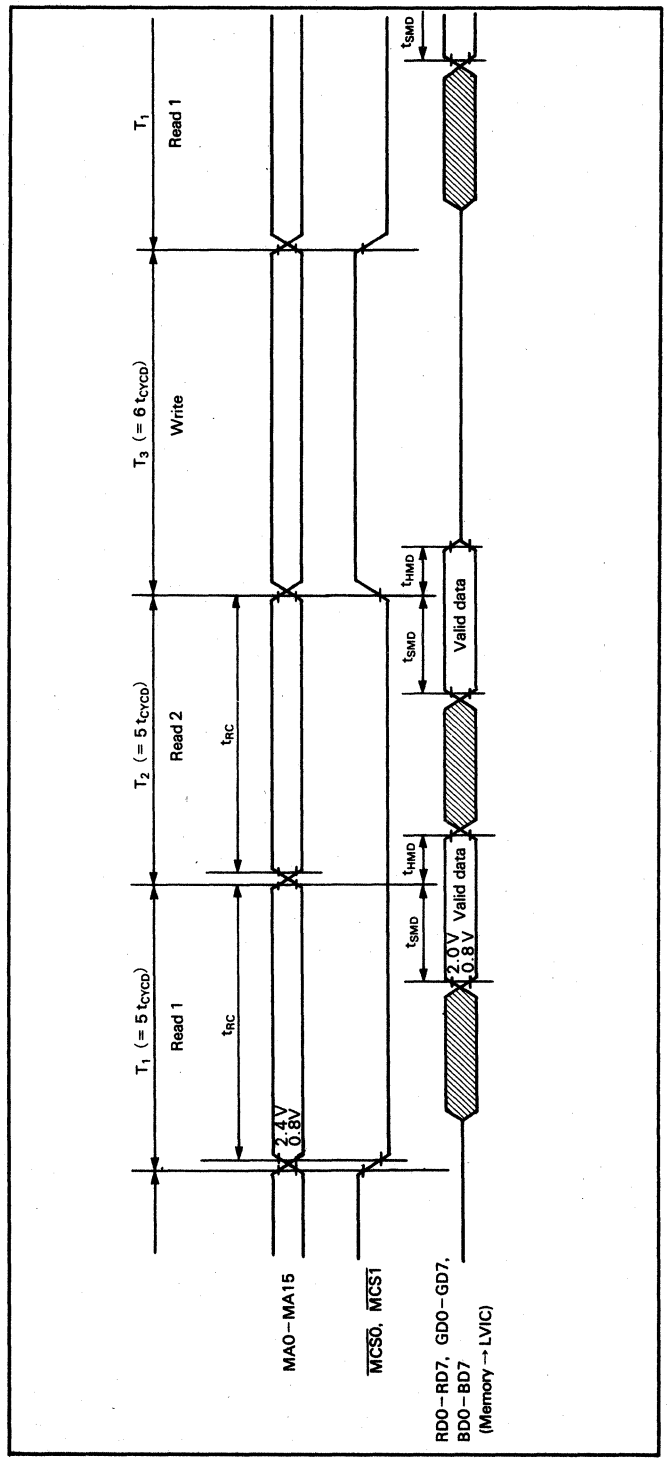

Figure 30 Buffer Memory Interface (RAM Read Timing)

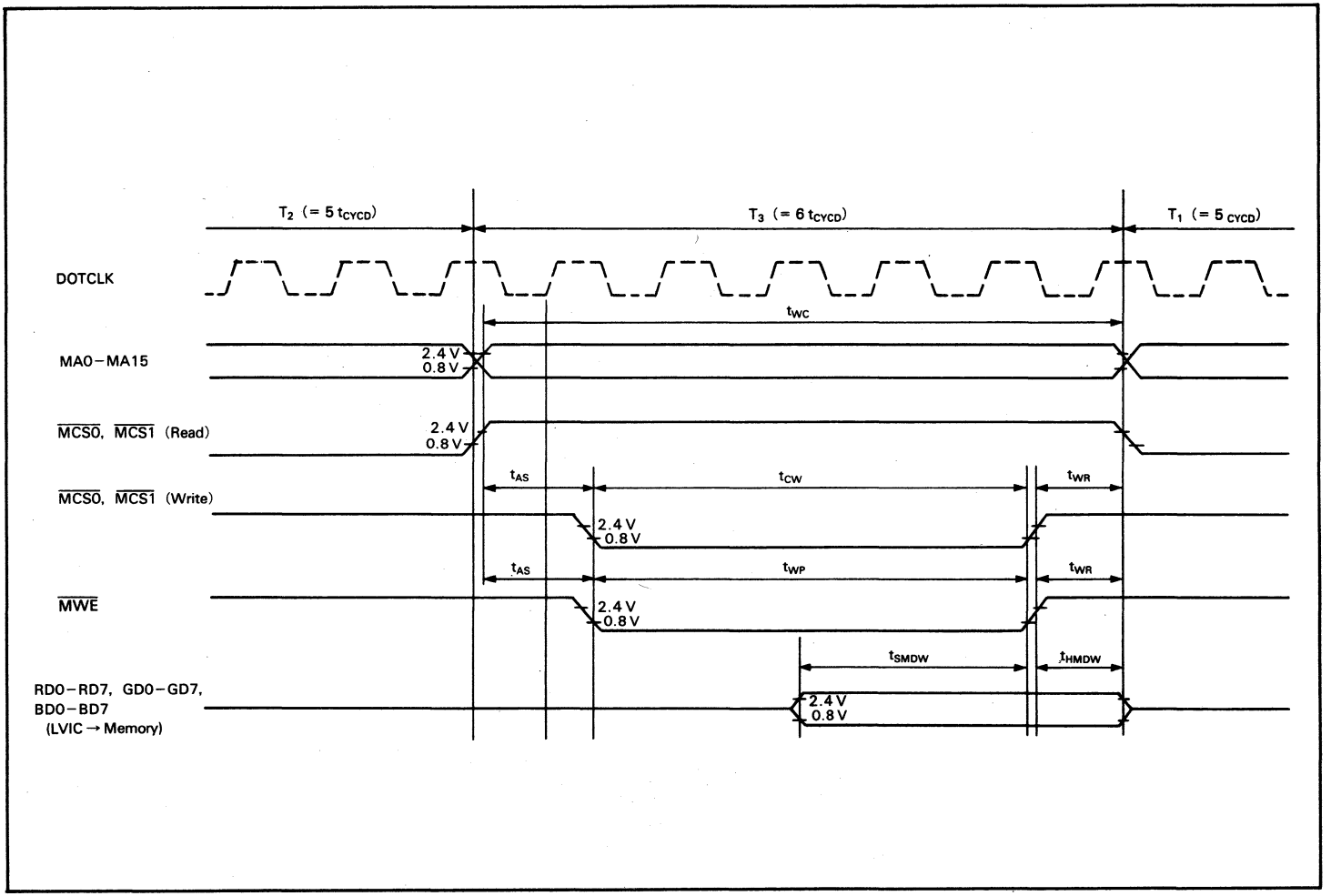

Figure 31 Buffer Memory Interface (RAM Write Timing)

LCD Driver Interface (TN-Type LCD Driver)

Item	Symbol	Min	Max	Unit
CL2 cycle time	t_{WCL2}	166	—	ns
CL2 high-level pulse width	t_{WCL2H}	50	—	ns
CL2 low-level pulse width	t_{WCL2L}	50	—	ns
CL2 rise time	t_{CL2r}	—	30	ns
CL2 fall time	t_{CL2f}	—	30	ns
CL1 high-level pulse width	t_{WCL1H}	200	—	ns
CL1 rise time	t_{CL1r}	—	30	ns
CL1 fall time	t_{CL1f}	—	30	ns
CL1 setup time	t_{SCL1}	500	—	ns
CL1 hold time	t_{HCL1}	200	—	ns
FLM hold time	t_{HF}	200	—	ns
M output delay time	t_{DM}	—	300	ns
Data delay time	t_{DD}	− 20	20	ns
LDOTCK cycle time	t_{WLDOT}	41	—	ns

Note: All the values are measured at f_{CL2} = 6 MHz.

LCD Driver Interface (TFT-Type LCD Driver)

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X drivers on one side)	t_{TCL2S}	160	—	ns	Figure 34, 35
CL2 high-level width (X drivers on one side)	t_{TCL2HS}	30	—	ns	
CL2 low-level width (X drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X drivers on both side)	t_{TCL2D}	320	—	ns	
CL2 high-level width (X drivers on both side)	t_{TCL2HD}	80	—	ns	
CL2 low-level width (X drivers on both side)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	−20	20	ns	
Data set up time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	40	—	ns	

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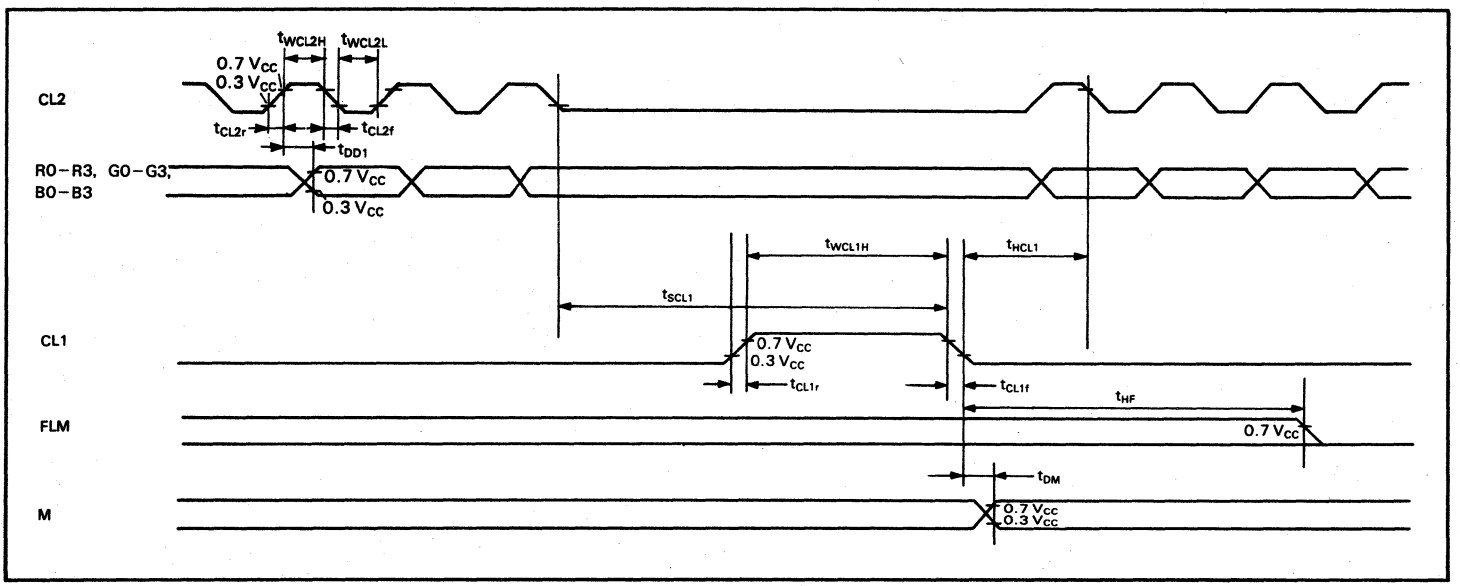

Figure 32 LCD Driver Interface (TN-Type LCD Driver Interface)

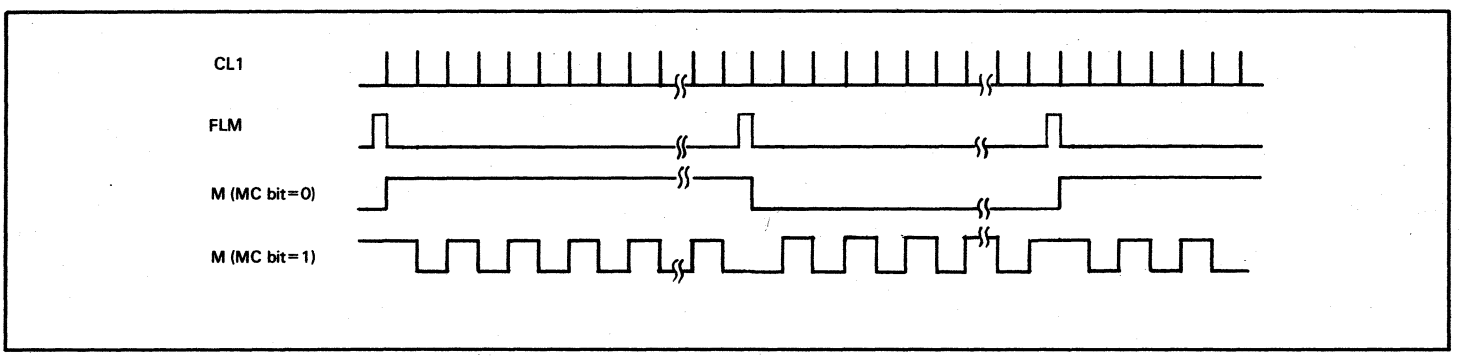

Figure 33 CL1, FLM and M (Reduced View of Figure 32)

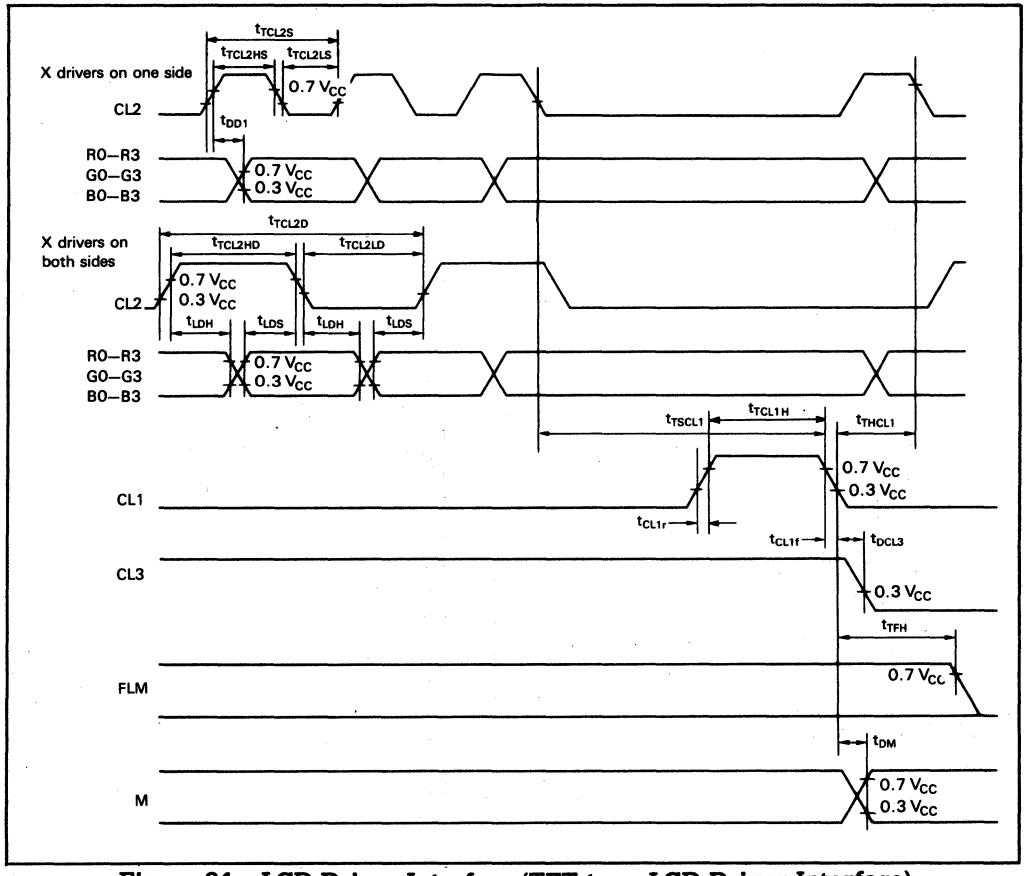

Figure 34 LCD Driver Interface (TFT-type LCD Driver Interface)

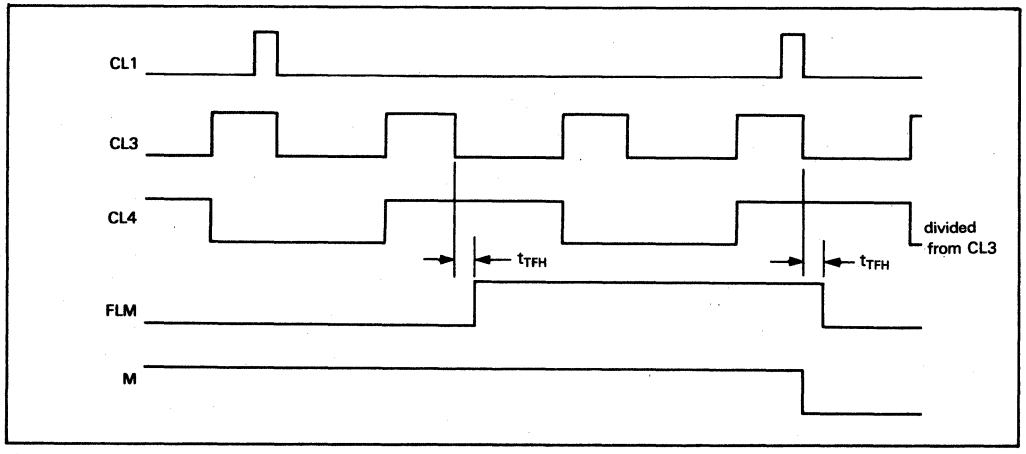

Figure 35 CL1, CL3, CL4, FLM, M (Reduced view of figure 34 in the horizontal stripe mode)

Register Programming, MPU Write

Item	Symbol	Min	Max	Unit
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns
$\overline{WE}$ high-level pulse width	t_{WWEH}	190	—	ns
$\overline{WE}$ low-level pulse width	t_{WWEL}	190	—	ns
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns
D0-D3 setup time	t_{DSW}	100	—	ns
D0-D3 hold time	t_{DHW}	0	—	ns
D0-D3 output delay time	t_{DDR}	—	150	ns
D0-D3 output hold time	t_{DHR}	10	—	ns

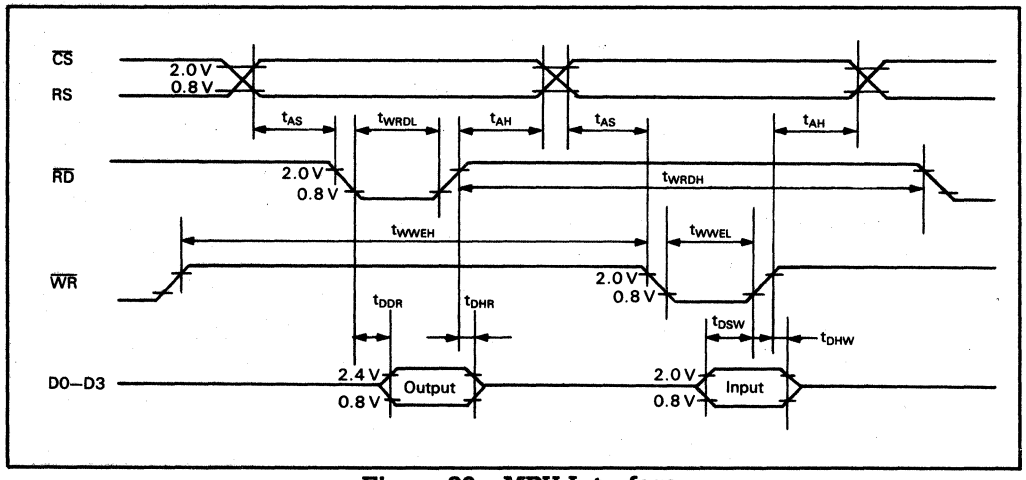

Figure 36 MPU Interface

Register Programming, ROM Write

Item	Symbol	Min	Max	Unit
A cycle time	t_{CYCA}	528	—	ns
A rise time	t_{Ar}	—	100	ns
A fall time	t_{Af}	—	100	ns
D ROM data setup time	t_{DSWD}	120	—	ns
D ROM data hold time	t_{DHWD}	0	—	ns

Note: $t_{CYCA} = 16\ t_{CYCD}$

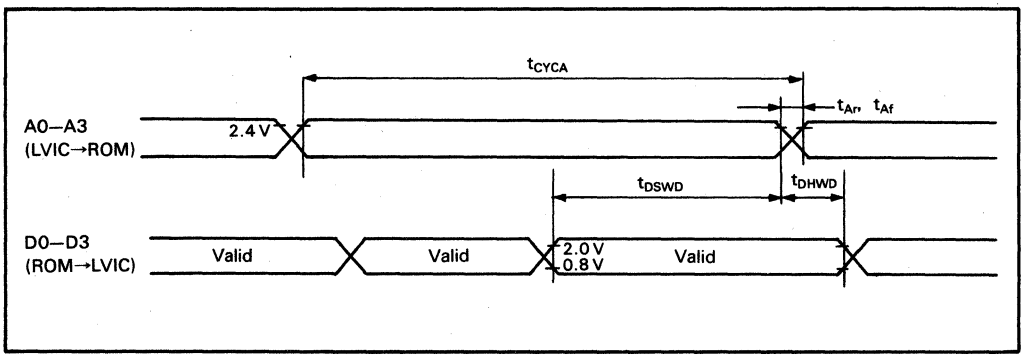

Figure 37 ROM Interface

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PLL Interface

Item	Symbol	Min	Max	Unit
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns

Reset Input

Item	Symbol	Min	Max	Unit
$\overline{RES}$ input pulse width	$t_{\overline{RES}}$	1	—	μs

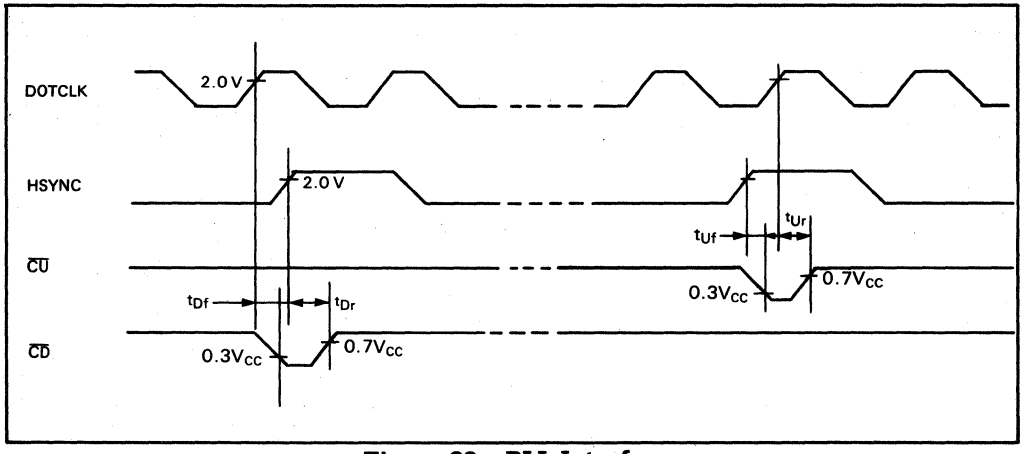


Figure 38 PLL Interface

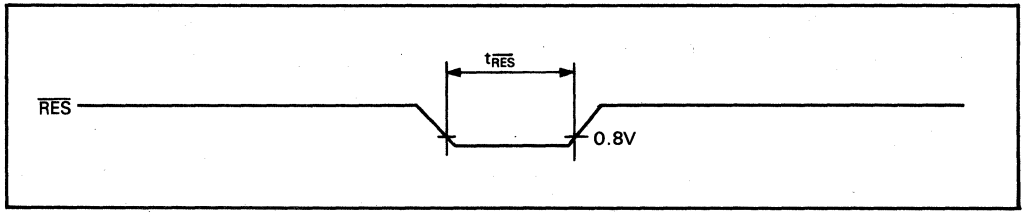


Figure 39 Reset Input

Load Circuits

TTL Load

Pin	R_L	R	C_L	Remarks
MA0-MA15, $\overline{MWE}$, $\overline{MCS0}$, $\overline{MCS1}$, RD0-RD7, GD0-GD7, BD0-BD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/RD/XDOT, A1/YL0-A3/YL2	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pin	C	Remarks
CL1, CL2, CL3, CL4	40 pF	tr, tf: Specified
R0-R3, G0-G3, B0-B3, FLM $\overline{CU}$, $\overline{CD}$, M	40 pF	tr, tf: Not specified

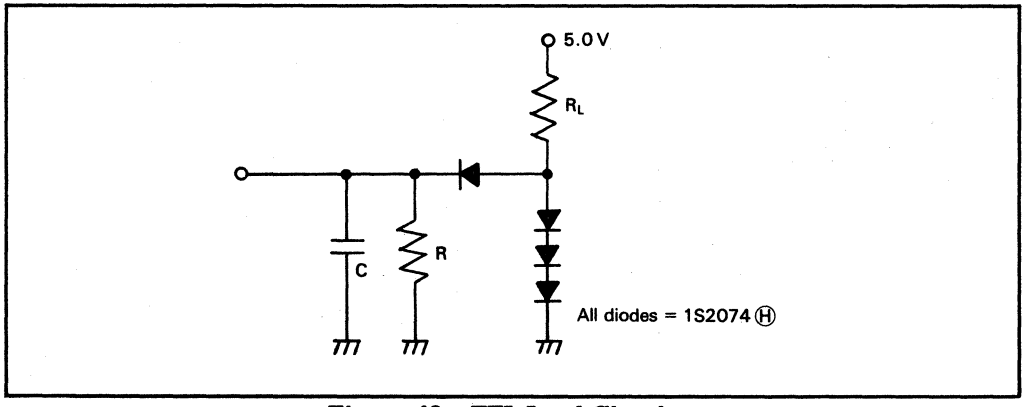


Figure 40 TTL Load Circuit

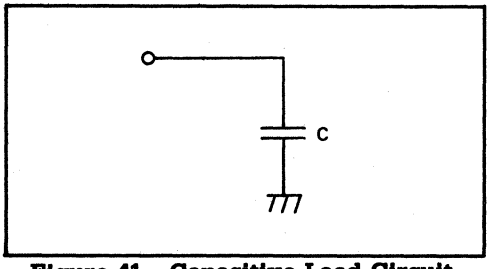


Figure 41 Capacitive Load Circuit

Refer to application note (No. ADE-502-011) for detail of this product.

HD66841F

LCD Video Interface Controller II (LVIC-II)

Description

The HD66841F LCD video interface controller (LVIC-II) converts standard RGB video signals for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes, and it also enables software originally intended for CRT display to control an LCD.

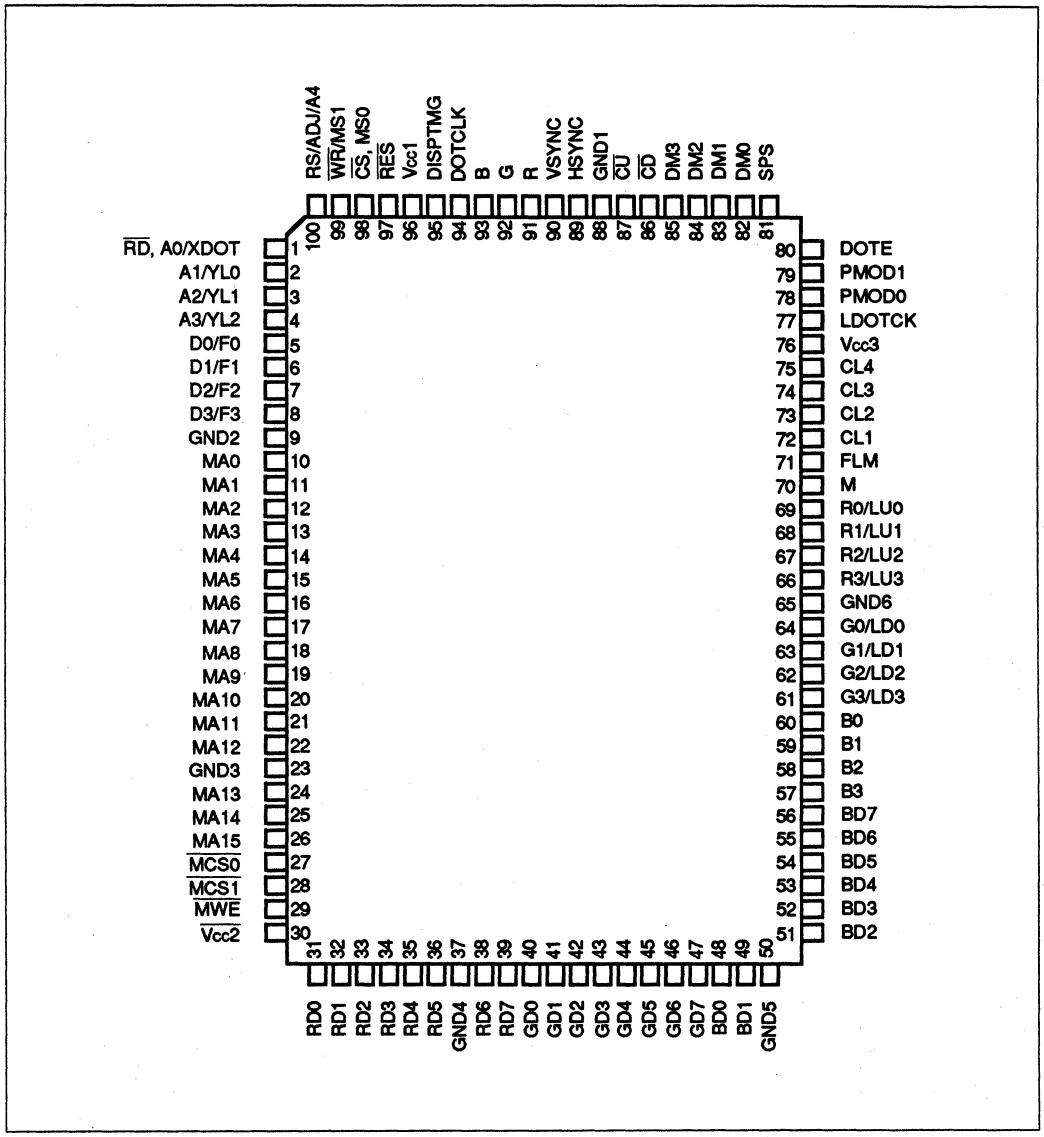
Since the LVIC-II can control TFT-type LCDs in addition to current TN-type LCDs, it can support monochrome, 8-level gray-scale, and 8-color displays. Thanks to a gray-scale palette, any 8 levels can be selected from 13 gray-scale levels, depending on the LCD panel used.

The LVIC-II also features a programmable screen size and can control a large-panel LCD of up to 720 × 512 dots.

Features

- Conversion of RGB video signals used for CRT display into LCD data:
  - Monochrome display data
  - 8-level gray-scale data
  - 8-color display data
- Selectable LVIC-II control method:
  - Pin programming method
  - Internal register programming method (either with MPU or ROM)
- Programmable screen size:
  - 640 or 720 dots (80 or 90 characters) wide by 200, 350, 400, 480, 512, or 540 dots (lines) high, using the pin programming method
  - 32 to 4048 dots (4 to 506 characters) wide by 4 to 1024 dots (lines) high, using the internal register programming method
- Double-height display capability
- Generation of display timing signal (DISPTMG) from horizontal synchronization (HSYNC) and vertical synchronization (VSYNC) signals
- Internal PLL circuit capable of generating a CRT display dot clock (DOTCLK) (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Control of both TN-type LCDs and TFT-type LCDs
- Gray-scale level selection from gray-scale palette
- Maximum operating frequency: 30MHz (DOTCLK)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, and B) parallel data transfer
- Recommended LCD drivers: HD61104 (column), HD61105 (row), HD61106 and HD66107T (column/row)
- Direct interface with buffer memory (no external decoder required)
- 1.3-µm CMOS processing
- Single power supply: +5V ± 10%
- Package: 100-pin plastic QFP (FP-100A)

Pin Arrangement



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Pin Description

The LVIC-II's pins are listed in table 1 and their functions are described below.

Table 1 Pin Description

Classification	Symbol	Pin Number	Pin Name	I/O	Note(s)
Power supply	$V_{CC}1$–$V_{CC}3$	96, 30, 76	$V_{CC}1$ to $V_{CC}3$	—	
	GND1–GND6	88, 9, 23, 37, 50, 65	Ground 1 to Ground 6	—	
Video signal interface	R, G, B	91, 92, 93	Red, green, and blue serial data	I	1
	HSYNC	89	Horizontal synchronization	I	
	VSYNC	90	Vertical synchronization	I	
	DISPTMG	95	Display timing	I	2
	DOTCLK	94	Dot clock	I	
LCD interface	R0–R3	69–66	LCD red data 0–3	O	3
	LU0–LU3	69–66	LCD upper panel data 0–3	O	4
	G0–G3	64–61	LCD green data 0–3	O	3, 5
	LD0–LD3	64–61	LCD lower panel data 0–3	O	4, 5
	B0–B3	60–57	LCD blue data 0–3	O	3, 6
	CL1	72	LCD data line select clock	O	
	CL2	73	LCD data shift clock	O	
	CL3	74	Y-driver shift clock 1	O	7
	CL4	75	Y-driver shift clock 2	O	7
	FLM	71	First line marker	O	
	M	70	LCD driving signal alternation	O	
	LDOTCK	77	LCD dot clock	I	
Buffer memory interface	$\overline{MCS0}$, $\overline{MCS1}$	27, 28	Memory chip select 0, 1	O	8
	$\overline{MWE}$	29	Memory write enable	O	8
	MA0–MA15	10–22, 24–26	Memory address 0–15	O	8
	RD0–RD7	31–36, 38, 39	Memory red data 0–7	I/O	8
	GD0–GD7	40–47	Memory green data 0–7	I/O	8, 9
	BD0–BD7	48, 49, 51–56	Memory blue data 0–7	I/O	8, 9
Mode setting	PMOD0, PMOD1	78, 79	Program mode 0, 1	I	
	DOTE	80	Dot clock edge change	I	
	SPS	81	Synchronization polarity select	I	
	DM0–DM3	82–85	Display mode 0–3	I	
	MS0, MS1	98, 99	Memory select 0, 1	I	10, 11
	XDOT	1	X-dot	I	10
	YL0–YL2	2–4	Y-line 0–2	I	10, 12

Table 1 Pin Description(cont)

Classification	Symbol	Pin Number	Pin Name	I/O	Note(s)
Mode setting	ADJ	100	Adjust	I	10
	F0–F3	5–8	Fine adjust 0–3	I	10
MPU interface	$\overline{CS}$	98	Chip select	I	10, 11
	$\overline{WR}$	99	Write	I	10, 11, 13
	$\overline{RD}$	1	Read	I	10, 13
	RS	100	Register select	I	10
	D0–D3	5–8	Data 0–3	I/O	10
	$\overline{RES}$	97	Reset	I	14
ROM interface	A0–A4	1–4, 100	Address 0–4	O	10
	D0–D3	5–8	Data 0–3	I	10
PLL interface	$\overline{CD}$	86	Charge down	O	
	$\overline{CU}$	87	Charge up	O	

Notes:
1. Fix G and B pins low if CRT display data is monochrome.
2. Fix high or low if the display timing signal is generated internally.
3. For 8-color display modes.
4. For monochrome or 8-level gray-scale display modes.
5. Leave disconnected in 4-bit/single-screen data transfer modes.
6. Leave disconnected in monochrome or 8-level gray-scale display modes.
7. Leave disconnected in TN-type LCD modes.
8. Leave disconnected if no buffer memory is used.
9. Pull up with a resistor of about 20 kΩ in monochrome display modes. The LVIC-II writes the OR of RGB signals into R-plane RAM, so no RAM is required for the G and B planes in these modes. (If G- or B-plane RAM is connected in monochrome display modes, the LVIC-II writes G or B signals into each RAM. However, this does not affect the display or the contents of R-plane RAM.)
10. Multiplexed pins.
11. Fix high or low when using the ROM programming method.
12. Fix high or low when using the MPU programming method.
13. Do not set pins $\overline{WR}$ and $\overline{RD}$ low simultaneously.
14. A reset signal must be input after power-on.

5

Power Supply

$V_{CC}1$–$V_{CC}3$: Must be connected to a +5V power supply.

GND1–GND6: Must be grounded.

CRT Display Interface

R, G, B: Input R, G, and B signals for CRT display.

HSYNC: Inputs the CRT horizontal synchronization signal.

VSYNC: Inputs the CRT vertical synchronization signal.

DISPTMG: Inputs the display timing signal which indicates the horizontal or vertical display period.

DOTCLK: Inputs dot clock pulses used for CRT display.

LCD Interface

R0–R3: Output LCD R data

LU0–LU3: Output LCD upper panel data.

G0–G3: Output LCD G data.

LD0–LD3: Output LCD lower panel data.

B0–B3: Output LCD B data.

CL1: Outputs line select clock pulses for LCD data.

CL2: Outputs shift clock pulses for LCD data.

CL3: Outputs line select and shift clock pulses for LCD data if Y-drivers are positioned on one side of the LCD screen. Refer to the LCD System Configuration section for details.

CL4: Outputs line select and shift clock pulses for LCD data if Y-drivers are positioned on both sides of the LCD screen. Refer to the LCD System Configuration section for details.

FLM: Outputs a first line marker for Y-drivers.

M: Outputs an alternation signal for converting LCD driving signals to AC.

LDOTCK: Inputs LCD dot clock pulses.

Buffer Memory Interface

$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$: Output buffer memory chip select signals.

$\overline{\text{MWE}}$: Outputs the buffer memory write enable signal.

MA0–MA15: Output buffer memory addresses.

RD0–RD7: Transfer data between R-data buffer memory and the LVIC-II.

GD0–GD7: Transfer data between G-data buffer memory and the LVIC-II.

BD0–BD7: Transfer data between B-data buffer memory and the LVIC-II.

Mode Setting

PMOD0, PMOD1: Select the programming method for the LVIC-II (table 2).

DOTE: Switches data latch timing. The LVIC-II latches RGB signals at the falling edge of DOTCLK pulses if the DOTE pin is set high, or at the rising edge if it is set low.

SPS: Selects the polarity of the VSYNC signal. (The HSYNC signal's polarity is fixed.) The VSYNC signal is active-high if SPS is set high, or active-low if it is set low.

DM0–DM3: Select the display mode (table 8).

MS0–MS1: Select the buffer memory type (table 3).

XDOT: Specifies the number of characters displayed on the LCD screen in the horizontal direction (called the horizontal displayed characters). The number is 90 (720 dots) if XDOT is set high, or 80 (640 dots) if it is set low.

YL0–YL2: Specify the number of lines displayed on the LCD screen in the vertical direction (called the vertical displayed lines) (table 4).

ADJ: Determines whether the F0–F3 pins adjust the display timing signal or the number of vertical displayed lines. They pins adjust the display timing signal if ADJ is set high, or the number of vertical displayed lines if it is set low.

F0–F3: Adjust the number of vertical displayed lines (table 5) or the display timing signal. Refer to the Display Timing Signal Fine Adjustment section for details.

MPU Interface

$\overline{CS}$: An MPU inputs the $\overline{CS}$ signal through this pin to select the LVIC. An MPU can access the LVIC-II while this signal is low.

$\overline{WR}$: An MPU inputs the $\overline{WR}$ signal through this pin to write data into the LVIC-II's internal registers. An MPU can write data while this signal is low.

$\overline{RD}$: An MPU inputs the $\overline{RD}$ signal through this pin to read data from the LVIC-II's internal registers. An MPU can read data while this signal is low.

RS: An MPU inputs the RS signal through this pin to select the LVIC's internal registers. An MPU can access data registers (R0–R15) while this signal is high and the $\overline{CS}$ signal is low, and can select the address register (AR) while both this signal and the $\overline{CS}$ signal are low.

D0–D3: Transfer LVIC-II internal register data between an MPU and the LVIC-II.

$\overline{RES}$: Externally resets the LVIC-II.

ROM Interface

A0–A4: Output external ROM addresses.

D0–D3: Input external ROM data to the LVIC-II's internal registers.

PLL Circuit Interface

$\overline{CD}$: Outputs charge-down signals to an external charge pump.

$\overline{CU}$: Outputs charge-up signals to an external charge pump.

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Table 2 Programming Method Selection

PMOD1	PMOD0	Programming Method	
0	0	Pin programming	
0	1	Internal register programming	MPU
1	0		ROM
1	1	Inhibited (Note)	

Note: This combination is for test mode: it disables display.

Table 3 Memory Type Selection

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes memory
1	0	32-kbytes memory
1	1	64-kbytes memory

Table 4 Number of Vertical Displayed Lines

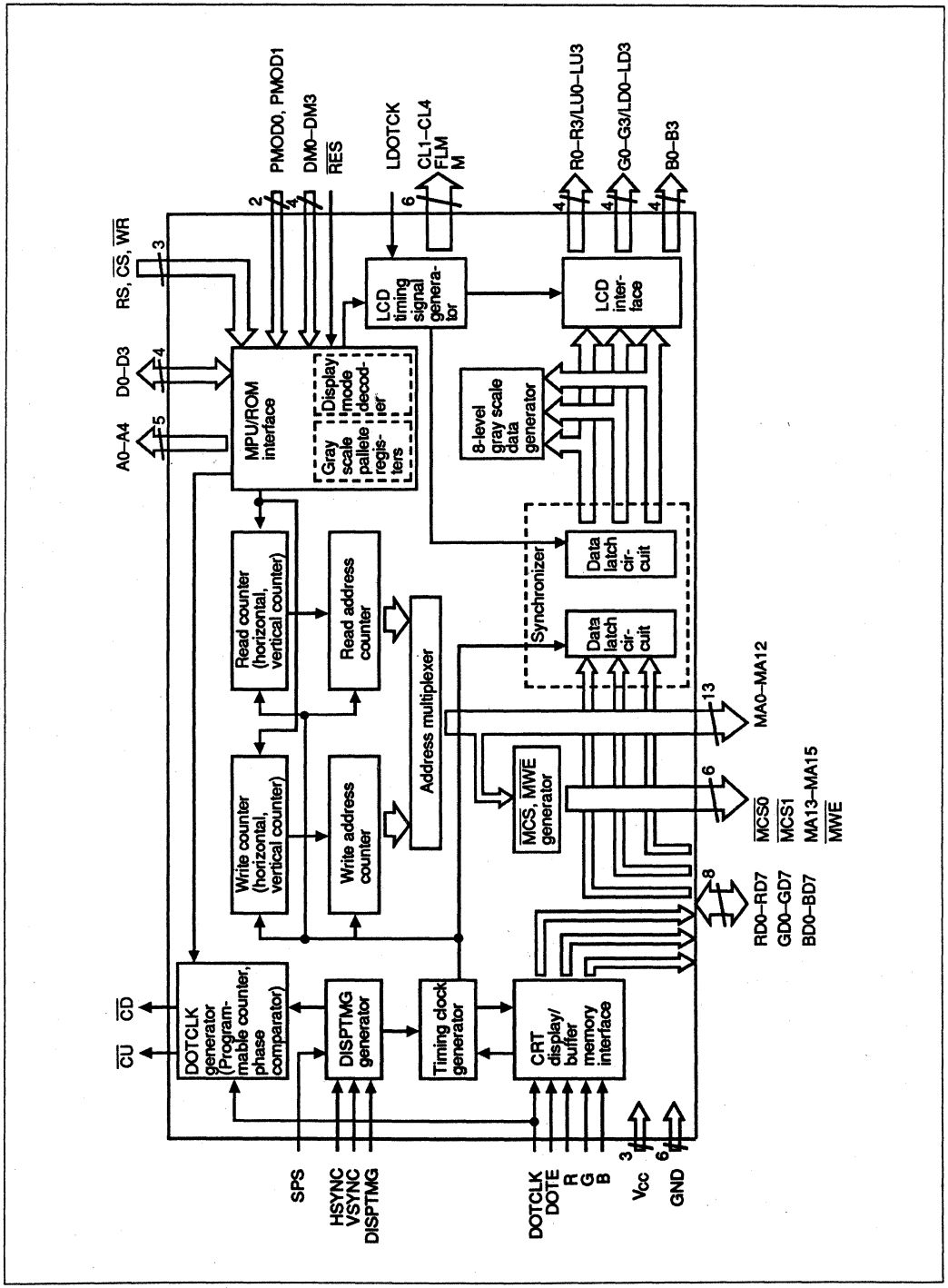
YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Inhibited (Note)
1	1	1	

Note: 480 lines are displayed, but they are practically indistinguishable.

Table 5 Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Adjusted Lines
0	0	0	0	±0
0	0	0	1	+1
0	0	1	0	+2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+14
1	1	1	1	+15

Block Diagram



Registers

The LVIC-II's registers are listed in table 6 and the bit assignments within the registers are shown in figure 1.

Table 6 Register List

$\overline{CS}$	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write[2]	Note(s)
1	—		—	—	—	—	—	—	—	—	—	
0	0		—	—	—	—	AR	Address register	—	—	W	3
0	1	0	0	0	0	0	R0	Control register 1	—	—	R/W	
0	1	0	0	0	0	1	R1	Control register 2	—	—	R/W	
0	1	0	0	0	1	0	R2	Vertical displayed lines register (middle-order)	Lines	Nvd	R/W	4
0	1	0	0	0	1	1	R3	Vertical displayed lines register (low-order)	Lines	Nvd	R/W	4
0	1	0	0	1	0	0	R4	Vertical displayed lines register (high-order)/ CL3 period register (high-order)	Lines/ Chars.	Nvd/ Npc	R/W	4, 5, 6
0	1	0	0	1	0	1	R5	CL3 period register (low-order)	Chars.	Npc	R/W	4, 5, 6
0	1	0	0	1	1	0	R6	Horizontal displayed characters register (high-order)	Chars.	Nhd	R/W	6
0	1	0	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Chars.	Nhd	R/W	6
0	1	0	1	0	0	0	R8	CL3 pulse width register	Chars.	Npw	R/W	6
0	1	0	1	0	0	1	R9	Fine adjust register	Dots	Nda	R/W	7
0	1	0	1	0	1	0	R10	PLL frequency-division ratio register (high-order)	—	N_{PLL}	R/W	8
0	1	0	1	0	1	1	R11	PLL frequency-division ratio register (low-order)	—	N_{PLL}	R/W	8
0	1	0	1	1	0	0	R12	Vertical backporch register (high-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	0	1	R13	Vertical backporch register (low-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	1	0	R14	Horizontal backporch register (high-order)	Dots	Nchbp	R/W	4, 9
0	1	0	1	1	1	1	R15	Horizontal backporch register (low-order)	Dots	Nchbp	R/W	4, 9

Table 6 Register List (cont)

$\overline{CS}$	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write[2]	Note(s)
0	1	1	0	0	0	1	P1	Black palette register	—	—	R/W	
0	1	1	0	0	1	0	P2	Blue palette register	—	—	R/W	
0	1	1	0	0	1	1	P3	Red palette register	—	—	R/W	
0	1	1	0	1	0	0	P4	Magenta palette register	—	—	R/W	
0	1	1	0	1	0	1	P5	Green palette register	—	—	R/W	
0	1	1	0	1	1	0	P6	Cyan palette register	—	—	R/W	
0	1	1	0	1	1	1	P7	Yellow palette register	—	—	R/W	
0	1	1	1	0	0	0	P8	White palette register	—	—	R/W	
0	1	1	1	0	0	1		Reserved				
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮				
0	1	1	1	1	1	1		Reserved				

Notes:
1. Corresponds to bit 2 of control register 1 (R0)
2. W indicates that the register can only be written to; R/W indicates that the register can both be read from and written to.
3. Attempting to read data from this register when RS = 0 drives the bus to high-impedance state; output data becomes undefined.
4. Write (the specified value – 1) into this register.
5. Valid only in 8-color display modes with horizontal stripes.
6. One character consists of eight horizontal dots.
7. Valid only if the display timing signal is supplied externally.
8. Valid only if the dot clock signal is generated internally.
9. Valid only if the display timing signal is generated internally.

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			Reg. Address				Reg.	Data Bits				
$\overline{CS}$	RS	PS[1]	3	2	1	0	No.	3	2	1	0	
1	—	—	—	—	—	—	—	— [2]				
0	0	—	—	—	—	—	AR					← Address register
0	1	—	0	0	0	0	R0	DIZ	PS	DSP	DCK	← Control register 1
0	1	0	0	0	0	1	R1	MC	DON	MS1	MS0	← Control register 2
0	1	0	0	0	1	0	R2					← Vertical displayed lines register
0	1	0	0	0	1	1	R3					
0	1	0	0	1	0	0	R4					
0	1	0	0	1	0	1	R5					← CL3 period register
0	1	0	0	1	1	0	R6[3]					← Horizontal displayed characters register
0	1	0	0	1	1	1	R7					
0	1	0	1	0	0	0	R8					← CL3 pulse width register
0	1	0	1	0	0	1	R9					← Fine adjust register
0	1	0	1	0	1	0	R10					← PLL frequency-division ratio register
0	1	0	1	0	1	1	R11					
0	1	0	1	1	0	0	R12					← Vertical backporch register
0	1	0	1	1	0	1	R13					
0	1	0	1	1	1	0	R14					← Horizontal backporch register
0	1	0	1	1	1	1	R15					
0	1	1	0	0	0	1	P1[4]	0	0	0	0	← Black palette register
0	1	1	0	0	1	0	P2[4]	0	0	1	0	← Blue palette register
0	1	1	0	0	1	1	P3[4]	0	1	0	1	← Red palette register
0	1	1	0	1	0	0	P4[4]	0	1	1	0	← Magenta palette register
0	1	1	0	1	0	1	P5[4]	0	1	1	1	← Green palette register
0	1	1	0	1	1	0	P6[4]	1	0	0	0	← Cyan palette register
0	1	1	0	1	1	1	P7[4]	1	0	1	0	← Yellow palette register
0	1	1	1	0	0	0	P8[4]	1	0	0	0	← White palette register
0	1	1	1	0	0	1	—	— [5]				← Reserved registers
⋮	⋮	⋮		⋮								
0	1	1	1	1	1	1	—					

Notes: 1. Corresponds to bit 2 of control register 1 (R0).
2. Invalid bits. Attempting to read data from these bits returns undefined data.
3. The most significant bit is invalid in dual-screen configuration modes.
4. Bit values shown are default values at reset.
5. Reserved bits. Any attempt to write data into the register is invalid, although it has no affect on LSI operations. Any attempt to read data from the register returns undefined data.

Figure 1 Register Bit Assignment

System Description

Figure 2 is a block diagram of a system in which the LVIC-II is used outside a personal computer.

The LVIC-II converts the RGB serial data sent from the personal computer into parallel data and temporarily writes it to the buffer memory. It then reads out the data in order and outputs it to LCD drivers to drive the LCD. In this case, the CRT display dot clock (DOTCLK), which is a latch clock for serial data, is generated by the PLL cricuit from the horizontal synchronization signal (HSYNC). The DOTCLK signal frequency is specified by the PLL frequency-division ratio register (R10, R11).

The system can be configured without a VCO and LPF if the DOTCLK signal is supplied externally, and it can be configured without an MPU if the LVIC-II is controlled by the pin programming method.

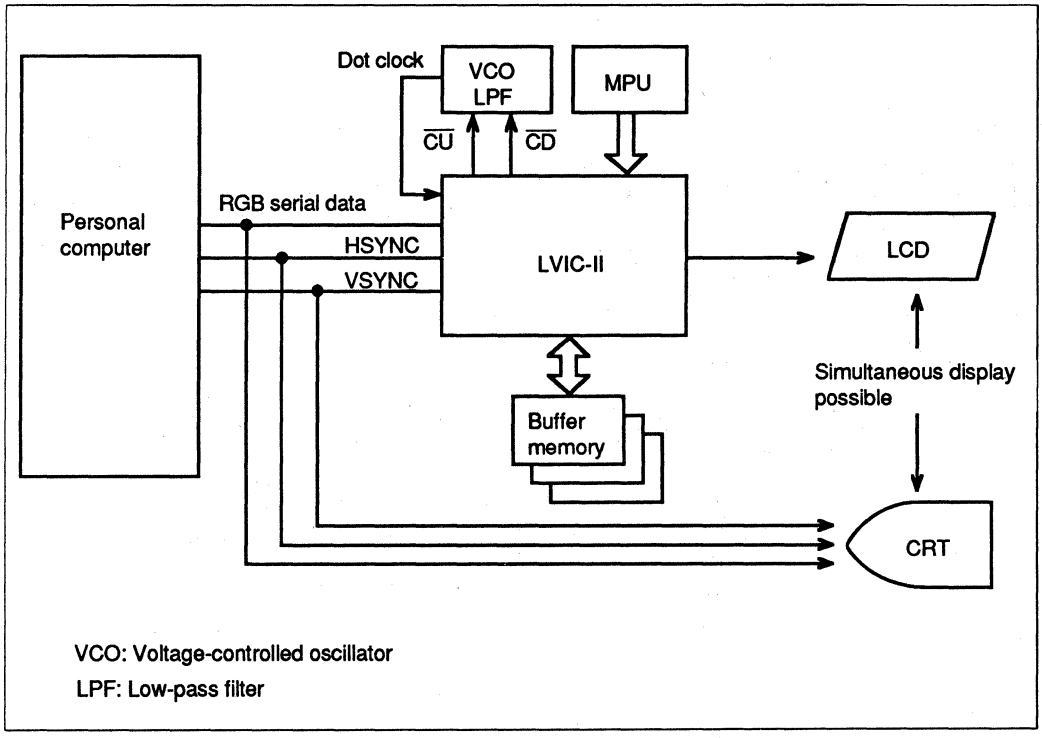

Figure 2 System Block Diagram (with MPU programming method and DOTCLK generated internally)

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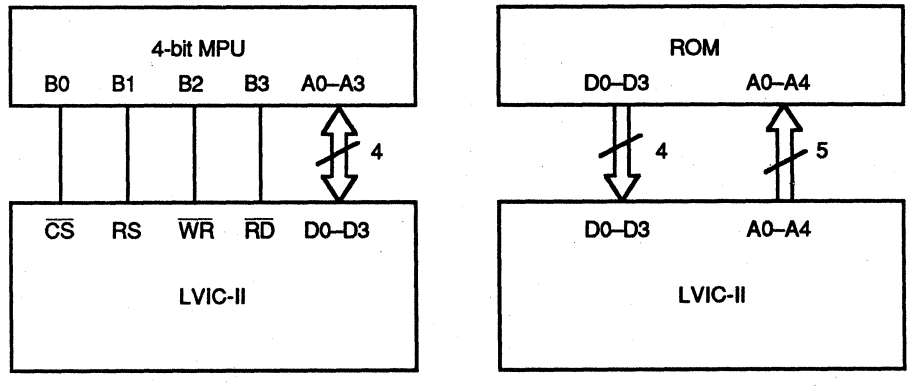
Functional Description

Programming Method

One of two methods of controlling LVIC-II functions can be selected by setting pins PMOD0 and PMOD1. Control by pins is called the pin programming method and control by internal registers is called the internal register programming method. The internal register programming method can be further divided into the MPU programming method and the ROM programming method; an MPU is used to write data into internal registers in the MPU programming method and ROM is used to write data into internal registers in the ROM programming method.

Pin Programming Method: The LVIC-II's mode-setting pins control functions.

Internal Register Programming Method: An MPU or ROM is used to write data into the LVIC-II's internal registers to control functions. Figure 3 shows the connection of either an MPU or ROM to the LVIC-II. Although figure 3 (1) shows an example of the use of a 4-bit microprocessor, the LVIC-II can also be connected directly to the host MPU bus since the LVIC-II MPU bus is compatible with the 4-MHz bus of 80-series microcomputers.



(1) Connection of MPU to LVIC-II

(2) Connection of ROM to LVIC-II

Figure 3 Connection of MPU or ROM to LVIC-II

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, either 640 dots or 720 dots (80 characters or 90 characters) can be selected with the XDOT pin as the number of horizontal displayed characters, and either 200, 350, 400, 480, 512, or 540 lines can be selected with the YL2–YL0 pins as the number of vertical displayed lines. The number of vertical displayed lines can be adjusted by from +0 to +15 lines with the ADJ and F3–F0 pins.

In the internal register programming method, any even number of characters from 4 to 506 (from 32 to 4048 dots) can be selected with the horizontal displayed characters register (R6, R7), and any even number of lines from 4 to 1028 can be selected with the vertical displayed lines register (R2, R3, and the high-order two bits of R4). However, note that an odd number of lines can also be selected if the screen configuration is single-screen and Y-drivers (scan drivers) are positioned on one side of the LCD screen.

The relationship between the LCD screen and the pins and internal registers controlling screen size is shown in figure 4.

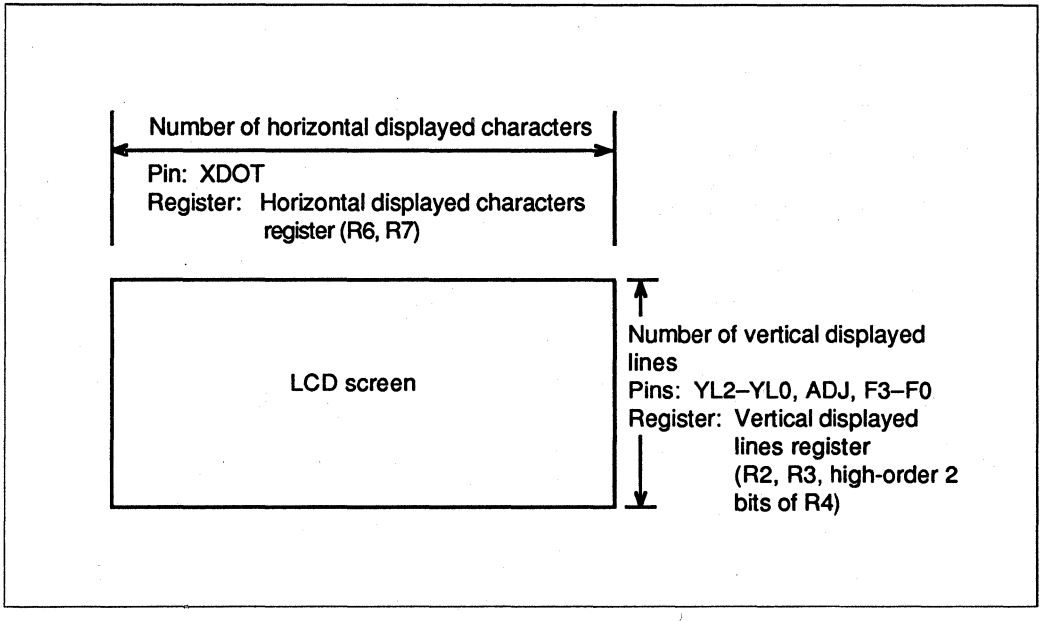


Figure 4 Relationship between LCD Screen and Pins and Internal Registers

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Memory Selection

8-, 32-, or 64-kbytes SRAMs can be selected as buffer memory for the LVIC-II. Since the LVIC-II has a chip select circuit for memory, no external decoder is required. The memory type can be selected with the MS1 and MS0 pins or the MS1 and MS0 bits of control register 2 (R1). Memory types and corresponding pin address assignments are listed in table 7.

The memory capacity required depends on screen size and can be obtained from the following equation:

Memory capacity (bytes) = Nhd × Nvd

Nhd: Number of horizontal displayed characters (where one character consists of 8 horizontal dots)

Nvd: Number of vertical displayed lines

For example, a screen of 640 × 200 dots requires a 16-kbytes memory capacity since 80 characters × 200 lines is 16 kbytes. Consequently, each plane requires two HM6264s (8-kbytes memories) in 8-level gray-scale display modes. The $\overline{MCS0}$ pin must be connected to the $\overline{CS}$ pin of one of the memory chips in each plane, and the $\overline{MCS1}$ pin must be connected to the $\overline{CS}$ pin of the remaining memory chip in each plane (figure 5 (a)).

A screen of 640 × 400 dots requires a 32-kbytes (256-kbit) memory capacity, so each plane requires an HM62256, which is a 32-kbytes memory. In this case, the $\overline{MCS0}$ pin must be connected to the $\overline{CS}$ pin of each memory chip. (figure 5 (b)).

Table 7 Memories and Pin Address Assignments

Pins or Bits					
MS1	MS0	Memory	Address Pins	Chip Select Pins	Address Assignment
0	0	No memory (Note)	—	—	—
0	1	8-kbyte	MA0–MA12	$\overline{MCS0}$	$0000–$1FFF
				$\overline{MCS1}$	$2000–$3FFF
				MA13	$4000–$5FFF
				MA14	$6000–$7FFF
				MA15	$8000–$9FFF
1	0	32-kbyte	MA0–MA14	$\overline{MCS0}$	$00000–$07FFF
				$\overline{MCS1}$	$08000–$0FFFF
				MA15	$10000–$17FFF
1	1	64-kbyte	MA0–MA15	$\overline{MCS0}$	$00000–$0FFFF
				$\overline{MCS1}$	$10000–$1FFFF

Note: There are some limitations if no memory is used. Refer to the User Notes section for details.

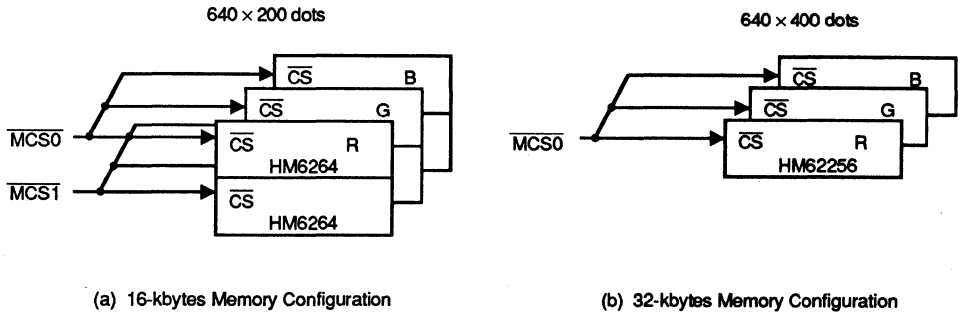

Figure 5 Screen Size and Memory Configuration

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Display Modes

The LVIC-II supports 16 display modes, depending on the states of the DM3–DM0 pins. The display mode controls display color, type of LCD data output, positions of LCD drivers for the LCD screen, arrangement of color data (type of stripes), and method of M signal output (type of alternation signal). Display modes are listed in table 8.

Table 8 Display Mode List

Mode No.	Pins DM3	DM2	DM1	DM0	Display Color	Data Transfer Type	Screen Config.	LCD Driver Positions X-driver[2]	Y-Driver[3]	Stripe[4]	Alternation
1	0	0	0	0	Mono-chrome	4-bit	Dual	One side	One side	—	Every frame
2	0	0	0	1			Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bit			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level gray scale	4-bit	Dual		One side		
7	0	1	1	0			Single				
8	0	1	1	1		8-bit					
9[1]	1	0	0	0	8-color	12-bit (4 bits each for R, G, and B)	Single	One side	Onse side	Vertical	Every line
10[1]	1	0	0	1					Both sides		
11[1]	1	0	1	0				Both sides	One side		
12[1]	1	0	1	1					Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16	1	1	1	1			Dual	One side		Vertical	Every frame

Notes:
1. For TFT-type LCDs.
2. Data output driver.
3. Scan driver.
4. Refer to the 8-color Display section.

Display Color

The LVIC-II converts the RGB color data normally used for CRT display into monochrome, 8-level gray-scale, or 8-color display data.

Monochrome Display (Modes 1 to 5): The LVIC-II displays two colors: black (display on) and white (display off). As shown in table 9, the CRT display RGB data is ORed to determine display on/off.

8-Level Gray Scale Display (Modes 6 to 8): The LVIC-II thins out data on certain lines or dots to provide an 8-level gray-scale display based on CRT display color (luminosity). The relationship between CRT display color (luminosity) and LCD gray scale (contrast) is shown in table 10.

This relationship corresponds to the default values in palette registers; the correspondence between color and gray scale can be changed by writing data into palette registers.

8-Color Display (Modes 9 to 16): The LVIC-II displays 8 colors through red (R), green (G), and blue (B) filters placed on liquid-crystal cells. The eight colors are the same as those provided by a CRT display. As shown in figure 6, 8-color display has two stripe modes: horizontal stripe mode in which the LVIC-II arranges RGB data horizontally for horizontal filters and vertical stripe mode in which it arranges RGB data vertically for vertical filters. Three cells express one dot in both modes.

Table 9 Monochrome Display

CRT Display Data				LCD		
R	G	B	CRT Display Color	On/Off	Color	
1	1	1	White	On	Black	
1	1	0	Yellow	On	Black	
0	1	1	Cyan	On	Black	
0	1	0	Green	On	Black	
1	0	1	Magenta	On	Black	
1	0	0	Red	On	Black	
0	0	1	Blue	On	Black	
0	0	0	Black	Off	White	

Table 10 8-Level Gray-Scale Display

CRT Display Data			CRT		LCD		
R	G	B	Color	Luminosity	Gray Scale	Contrast	
1	1	1	White	High	Black	Strong	
1	1	0	Yellow				
0	1	1	Cyan				
0	1	0	Green				
1	0	1	Magenta				
1	0	0	Red				
0	0	1	Blue				
0	0	0	Black	Low	White	Weak	

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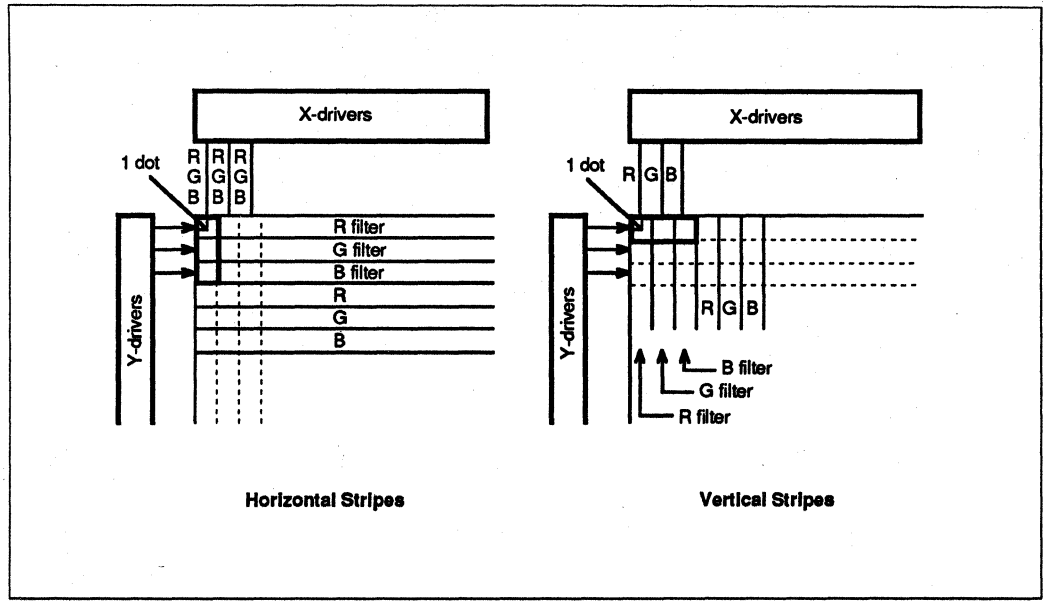


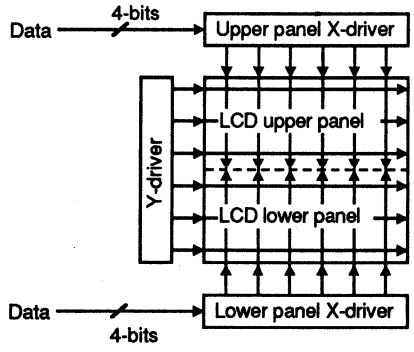
Figure 6 Stripe Modes in 8-Color Display

LCD System Configuration

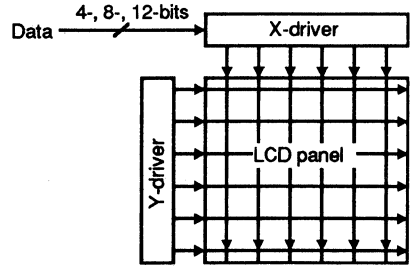
The LVIC-II supports the following LCD system configurations:

- Types of LCD data output:
  - Data transfer: 4-bit, 8-bit, or 12-bit (4 bits each for R, G, and B)
  - Screen configuration: Single or dual
- LCD driver positions around LCD screen:
  - X-drivers: On one side or on both sides
  - Y-drivers: On one side or on both sides

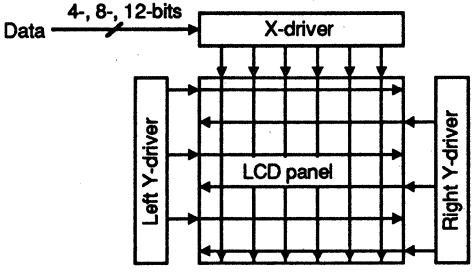
System configurations for different modes are shown in figure 7, and configurations of X- and Y-drivers positioned on both sides of an LCD screen are shown in figure 8.



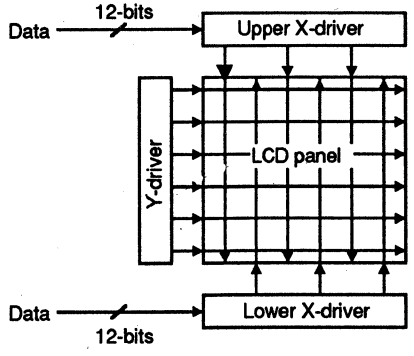
System configuretion for mode 1 and mode 6 (4-bit data transfer, dual screen, X-driver and Y-driver each on one side) Note



System configureation for modes, 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-bit data transfer, single screen, X-driver and Y-driver each on one side)



System configureaton fo rmodes 3, 5, 10, and 14 (4-, 8-, or 12-bit data transfer, single screen, X-driver on one side and Y-driver on both sides)

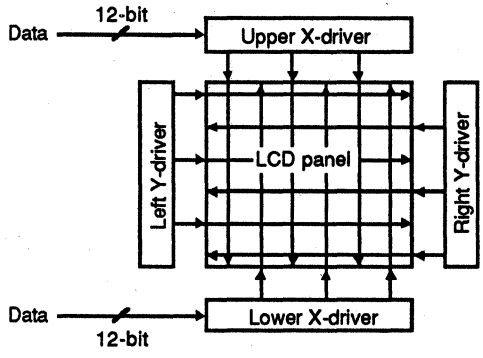


System configureation for mode 11 and mode 15 (12-bit data transfer, single screen, X-edriver on both sides and Y-driver on one side)

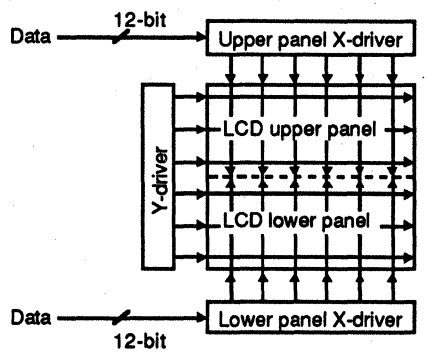
Note: Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 7 System Configurations by Mode

5



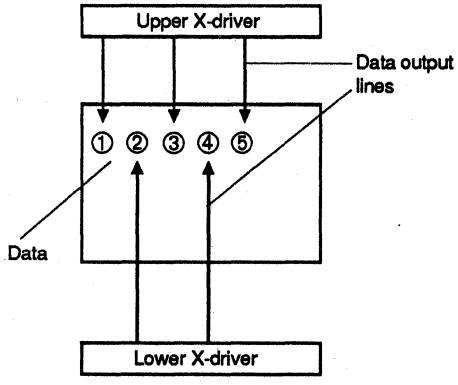
System configuration for mode 12 (12-bit data transfer, single screen, X-driver and Y-driver each on both sides)



System configuration for mode 16 (12-bit data transfer, dual screen, X-driver and Y-driver each on one side)Note

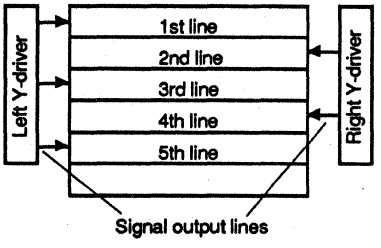
Note: Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 7 System Configurations by Mode (cont)



(1) X-drivers set on both sides

Data output lines run alternately from upper and lower X-drivers, increasing the pitch of the lines to twice that for X-drivers positioned on one side.



(2) Y-drivers set on both sides

Line select signal output lines run alternately from right and left Y-drivers, increasing the pitch of the lines to twice that for Y-drivers positioned on one side.

Figure 8 X- and Y-Drivers Set on Both Sides

LDOTCK Frequency Calculation

The frequency f_L of the LCD dot clock (LDOTCK) can be obtained from the following equation:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd: Number of horizontal displayed characters on LCD = (number of horizontal displayed dots on LCD) × 1/8
Nvd: Number of vertical displayed lines on LCD
f_F: Frame frequency (FLM frequency)

In this case, f_L must satisfy the following relationships, where f_D is the frequency of the dot clock for CRT display (DOTCLK):

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (the phase of LDOTCK must be opposite to that of DOTCLK in this case)

Display Timing Signal Generation

CRT display data is divided into display period data and retrace period data, so the LVIC-II needs a signal indicating whether the CRT display data that has just been transferred is display period data or not. This signal is called the display timing signal.

The LVIC-II can generate the display timing signal from the HSYNC and VSYNC signals. The relationships between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data are shown in figure 9. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15), respectively.

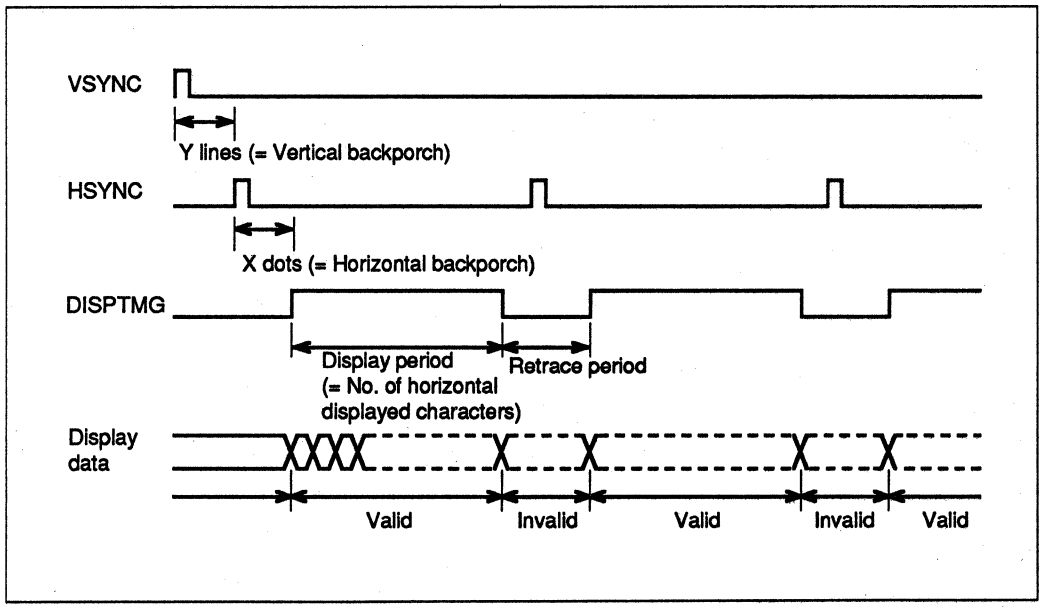


Figure 9 Relationships between HSYNC, VSYNC, DISPTMG, and Display Data

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Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal, so it is not usually output from the CRT display plug. Therefore, the LVIC-II must generate it. The LVIC-II has a programmable counter and a phase comparator which are parts of a phase-locked loop (PLL) circuit, and it can generate the dot clock from the HSYNC signal if a charge pump, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

A block diagram of the PLL circuit is shown in figure 10. A PLL circuit is a feedback controller that generates a clock whose frequency and phase are the same as those of a basic clock. The basic clock is the HSYNC signal in this case.

At power-on, the VCO outputs to the programmable counter a signal whose frequency is determined by the voltage at that time. The counter divides the frequency of the signal according to the value in the PLL frequency-division ratio register (R10, R11), and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock pulses and the HSYNC signal pulses and outputs the $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs the $\overline{CU}$ signal if the frequency of the clock is lower than that of the HSYNC signal or if the phase of the clock is behind that of the HSYNC signal; otherwise it outputs the $\overline{CD}$ signal. The charge pump and LPF apply a voltage to the VCO according to the $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and frequency of the frequency-divided clock match those of the HSYNC signal, making it a stable dot clock.

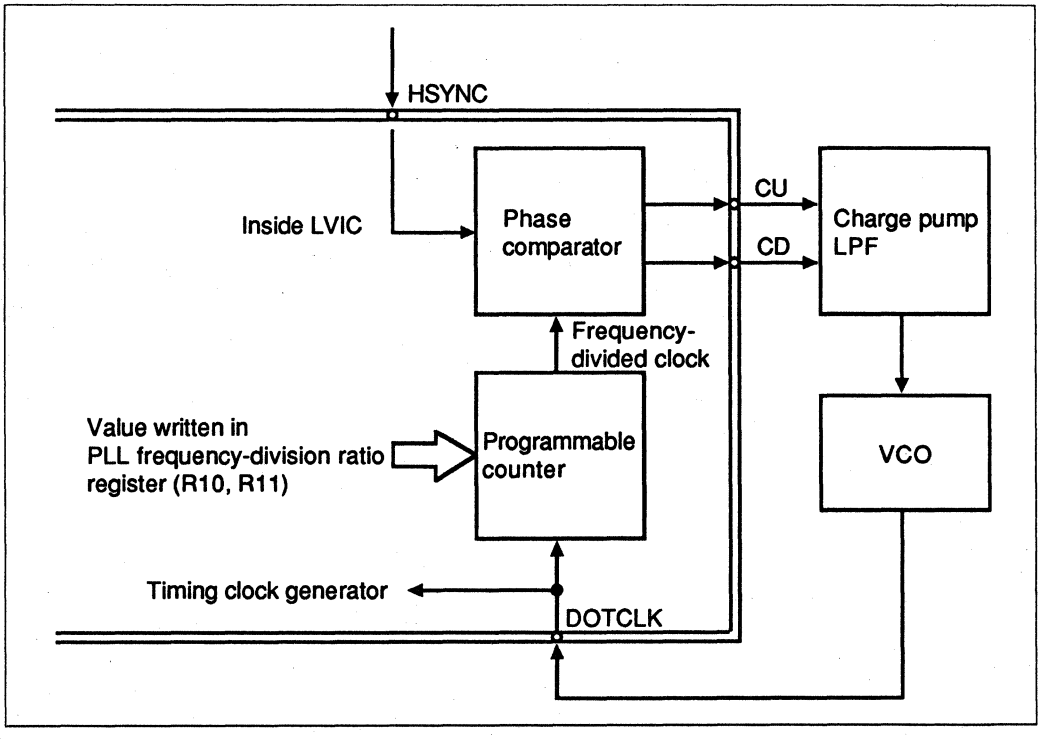

Figure 10 PLL Circuit Block Diagram

Gray-Scale Palette

The HD66841F thins out LCD data on certain dots or lines of an LCD panel every frame, changing integral voltages applied to liquid-crystal cells, to generate intermediate levels of luminosities. Consequently, the difference in depth between adjacent gray-scale shades may not be uniform in some cases since voltage-transmittance characteristics vary with different panels. To allow for this, the HD66841F is designed to generate 13 gray-scale levels and provide palette registers that assign desired levels to certain of the eight CRT display colors.

The relationships between gray scales and corresponding effective applied voltages are shown in figure 11 (a). Each gray scale is displayed according to the characteristics of its effective applied voltage and the optical transmittance of the panel (figure 11 (b)). Using the palette registers to select any 8 out of 13 levels of applied voltages enables an optimal gray-scale display conforming to the characteristics of the LCD panel. The palette registers can also be used to provide 4-level gray-scale display and reverse display.

Table 11 Default Values of Palette Registers

Register No.	CRT Display Data R	G	B	Register Name	Default Value			
P1	0	0	0	Black palette	0	0	0	0
P2	0	0	1	Blue palette	0	0	1	0
P3	1	0	0	Red palette	0	1	0	1
P4	1	0	1	Magenta palette	0	1	1	0
P5	0	1	0	Green palette	0	1	1	1
P6	0	1	1	Cyan palette	1	0	0	0
P7	1	1	0	Yellow palette	1	0	1	0
P8	1	1	1	White palette	1	1	0	0

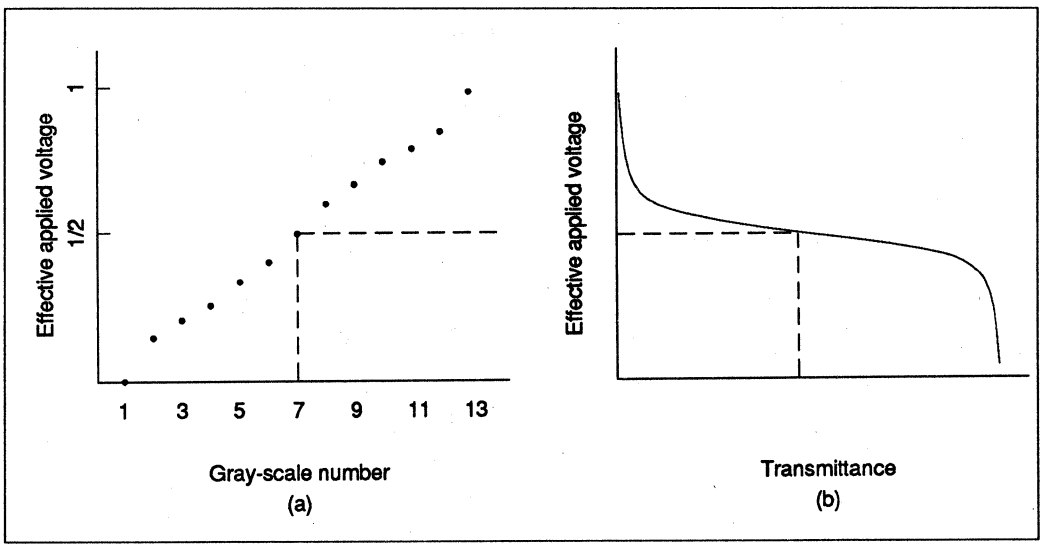

Figure 11 Relationships between Gray Scale, Transmittance, and Effective Applied Voltage

5

Pin Programming Method

The palette registers cannot be used in the pin programming method.

MPU Programming Method

To change the contents of palette registers in the MPU programming method, set bit 2 (the PS bit) of control register 1 (R0), to 1. Since data registers (R1–R15) cannot be accessed while this bit is 1, set in to 0 before accessing the data registers again. However, note that control register 1 (R0) can be accessed regardless of the setting of the PS bit if $0 is set in the address register (AR).

ROM Programming Method

In the ROM programming method, the HD66841F accesses ROM sequentially from address $0000 to $001F. In this case, write 0 to bit 2 of address $0000 (PS bit) before writing data register values to addresses $0001–$000F, and write 1 to bit 2 of address $0010 (PS bit) before writing palette register values to addresses $0011–$0018.

DIZ Function

The HD66841F thins out data on certain lines or dots every frame to enable gray-scale display. If a checker-board pattern consisting of alternately arranged gray scales of different levels (figure 12) is displayed by a simple dot-basis gray-scale display control method, the display might sometimes seem to "flow" horizontally, depending on the gray-scale and LCD panel characteristics.

The HD66841F automatically checks for such a checker-board section and changes the gray-scale display control method of dot-based data thinning to that of frame-based data thinning, to reduce display flow. Setting bit 3 (DIZ) of control register 1 (R0) to 1 enables this function. In frame-based data thinning, however, flickering might appear with some LCD panels; in that case, select the control method that generates the better display.

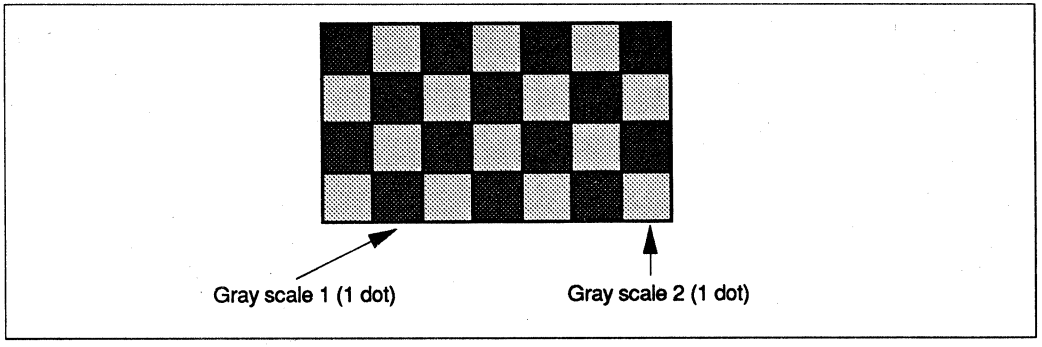

Figure 12 Checker-Board Display

Double-Height Display

The LVIC-II provides double-height display which doubles the vertical size of characters and pictures (figure 13).

In the TN-type LCD modes (display modes 1, 2, 4, and 6-8), the CL3 signal period is half as long as the CL1 signal period, as shown in figure 14. Consequently, using the CL3 signal instead of the CL1 signal (figure 15) as a line shift clock enables two lines to be selected while X-drivers (data output drivers) are outputting identical data, thus realizing double-height display. However, it should be noted that this display requires the following procedure since the LVIC-II displays twice as many lines as specified by pins or internal registers:

1. Halve the LCD dot clock (LDOTCK) frequency calculated from the number of vertical displayed lines of the LCD panel.

2. Specify half the number of vertical displayed lines of the LCD panel as the number of vertical displayed lines. (For instance, if the number of vertical displayed lines of the LCD panel is 400, specify 200 with the YL2–YL0 pins or the vertical displayed lines register.)

This function is available only in the TN-type LCD modes; it is disabled in the TFT-type LCD modes.

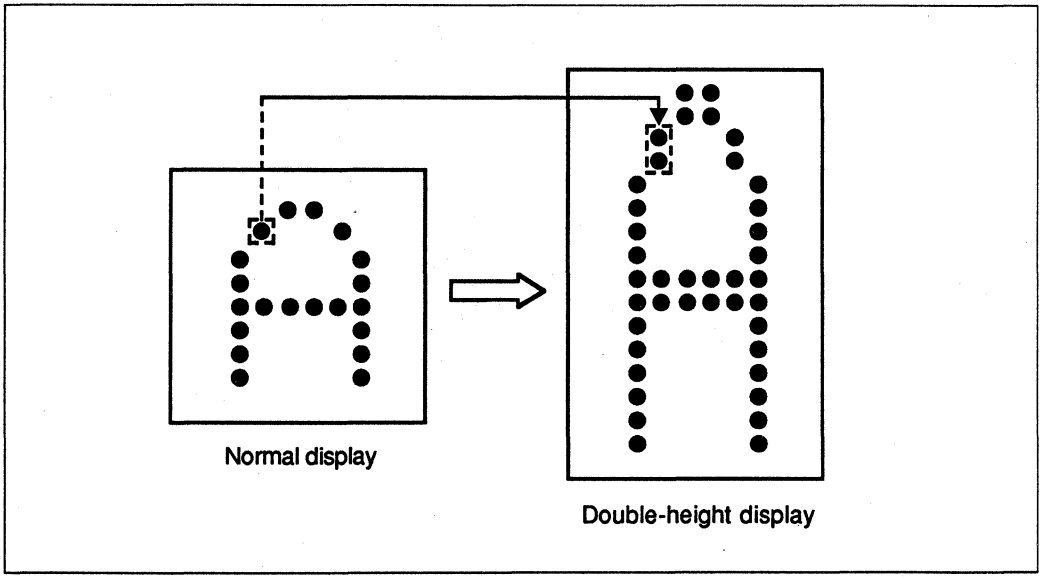

Figure 13 Double-Height Display Example

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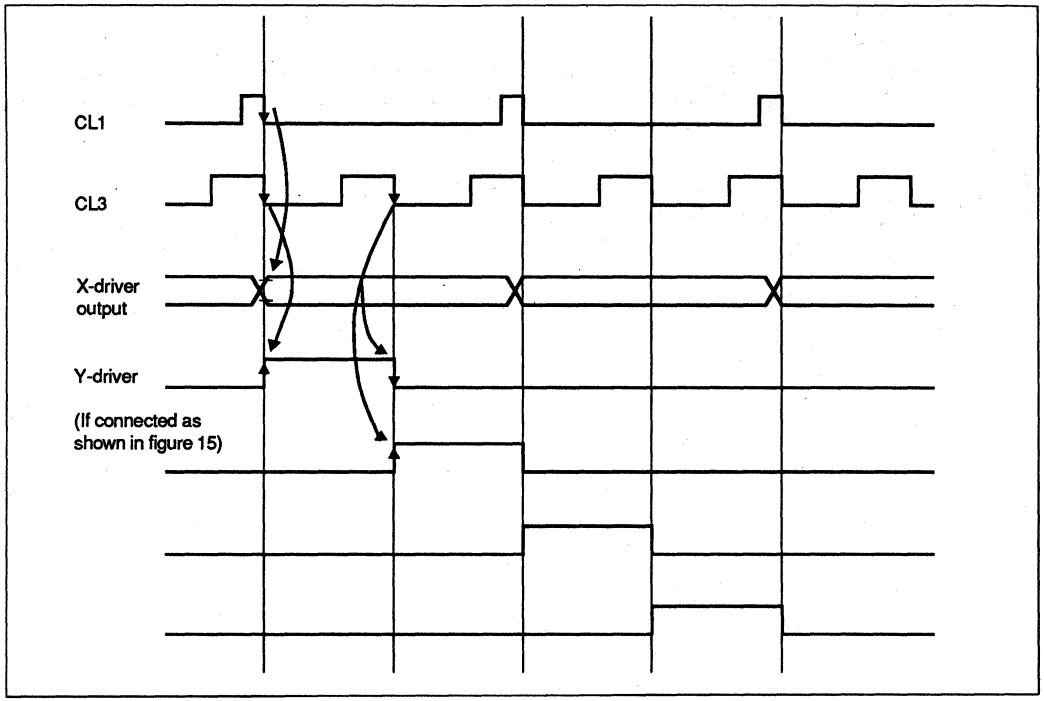

Figure 14 Relationship between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

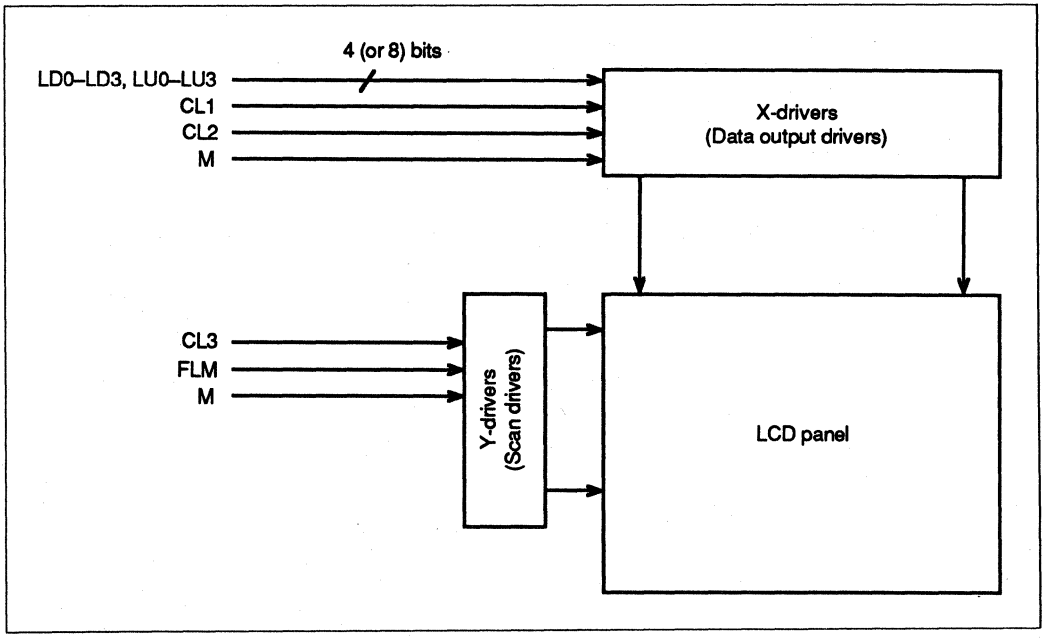

Figure 15 Connection for Double-Height Display

Display Timing Signal Fine Adjustment

If the display timing signal is supplied externally, a phase shift between CRT data and the display timing signal may appear. This is because each signal has its own specific lag. The LVIC-II can adjust the display timing signal according to pins F0–F3 or the fine adjust register (R9) to correct the phase shift.

The relationships between pins F3–F0, data bits 3 to 0 of the fine adjust register, and the resultant fine adjustments are shown in table 12. The polarity of the number of dots adjusted is given by – (minus) indicating advancing the phase of the display timing signal or + (plus) indicating delaying it. Pin F3 or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Examples of adjusting the display timing signal are shown in figure 16. Since the signal is two dots ahead of the display start position in case (1), F3, F2, F1, and F0 or data bits 3, 2, 1, and 0 of R9 should be set to (1, 0, 1, 0) to delay the signal by two dots. Conversely, since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal by two dots. If there is no need to adjust the signal, a setting of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 12 Pins, Data Bits of R9, and Fine Adjustment

Pin	F3	F2	F1	F0	Number of Dots
R9 Bit	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	–1
		⋮	⋮	⋮	⋮
		1	1	0	–6
		1	1	1	–7
	1	0	0	0	0
		0	0	1	+1
		⋮	⋮	⋮	⋮
		1	1	0	+6
		1	1	1	+7

Note: To use pins to adjust the display timing signal, set the ADJ pin to 1.

5

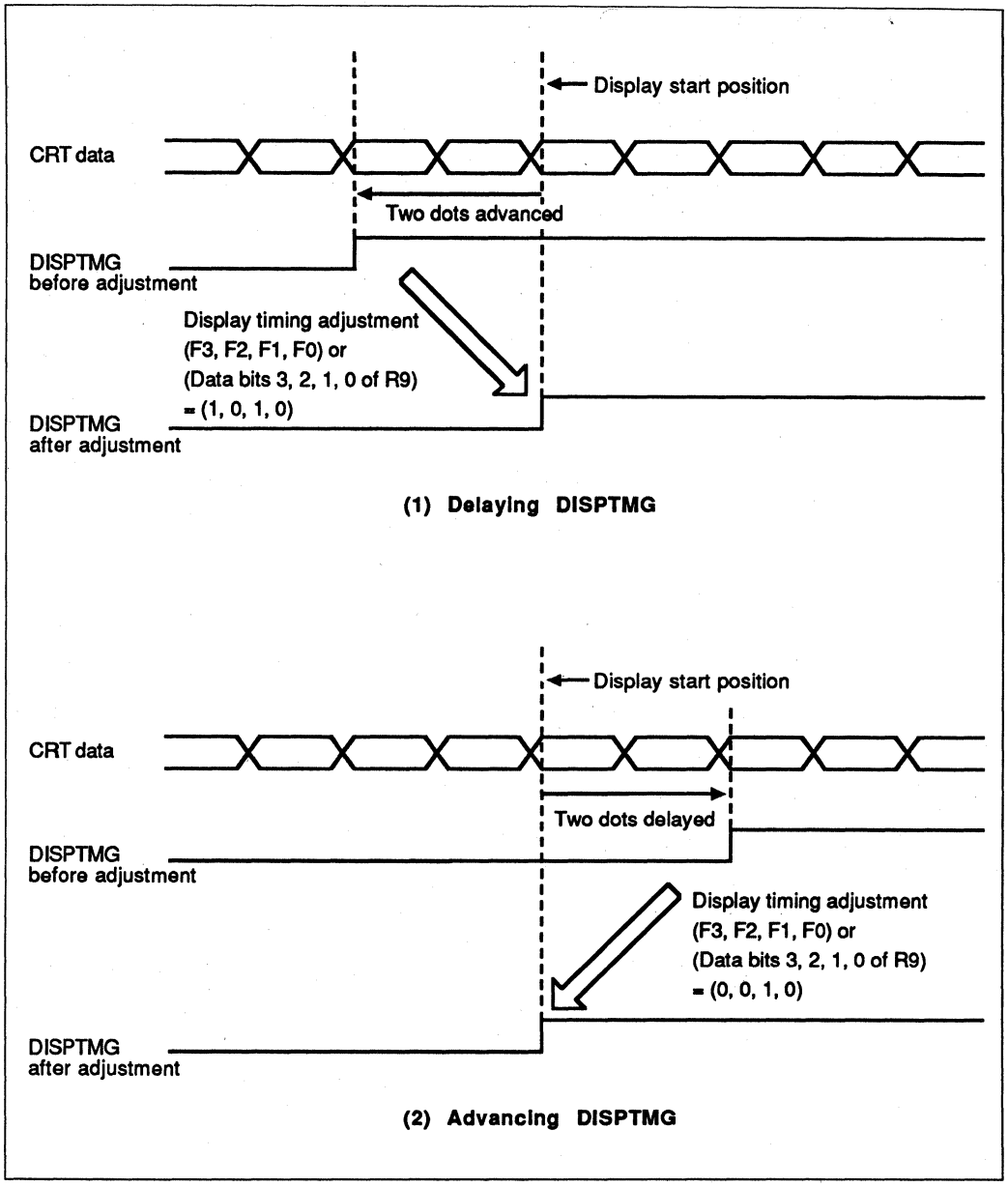

Figure 16 Adjustment of Display Timing Signal

Internal Registers

The HD66841F has an address register (AR), 16 data registers (R0–R15), and 8 palette registers (P1–P8). Write the address of a register to be used into the address register (AR), but only after setting the PS bit of control register 1 (R0) to 0 for a data register or 1 for a palette register. The MPU transfers data to the register corresponding to the written address.

Registers are valid only in the internal register programming method, they are invalid (don't care) in the pin programming method.

The 4-bit address register (figure 17) is used to select one of the 16 data registers or 8 palette registers. It can select any data register or palette register according to the register address written to it by the MPU. The addres register itself is selected if the RS signal is set low.

Control register 1 (figure 18) is composed of four bits whose functions are described below.

- DIZ bit: Changes the method used to control the gray-scale display of a checker-board pattern.
  - DIZ = 0: Data thinned out on a dot basis every frame
  - DIZ = 1: Data thinned out on a frame basis every frame
- PS bit: Specifies access to data registers (R0–R15) or palette registers (P1–P8).

  In MPU programming mode:
  - PS = 0: Specifies access to data registers (R0–R15) only.
  - PS = 1: Specifies access to palette registers (P1–P8) only.

Address Register (AR)

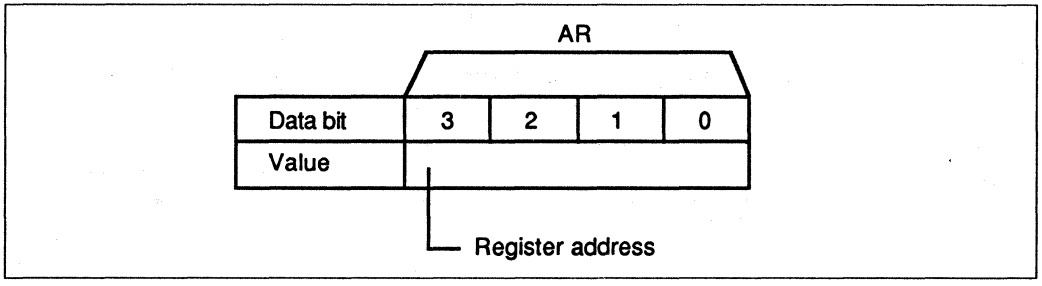

Figure 17 Address Register

Control Register 1 (R0)

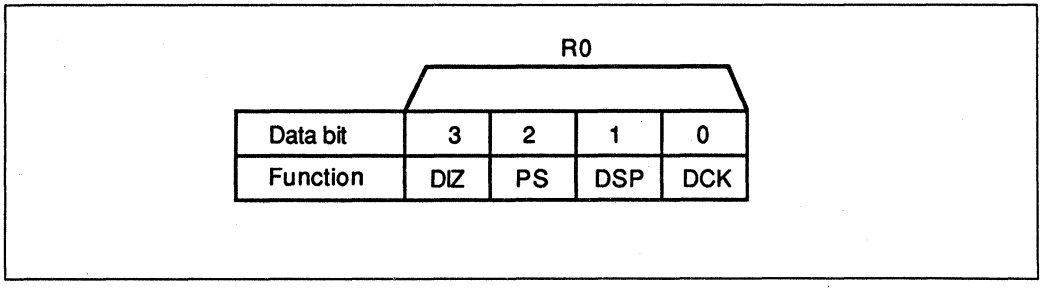

Figure 18 Control Register 1

This register can be always accessed regardless of the PS bit setting, but it cannot be read after the PS bit is set to 1. Read it when PS is 0.

In ROM programming mode: Data for LVIC-II internal data registers can be written into $0001 to $000F when bit 2 (the PS bit) of $0000 is set to 0. Data to be set into palette registers can be written into $0011 to $0018 when the PS bit of $0010 is set to 1 (figure 19 (a)).

- DSP bit
  - DSP = 1: The DISPTMG signal is generated internally.
  - DSP = 0: The DISPTMG signal is supplied externally. (However, note that if DCK is 1, the DISPTMG signal is generated internally even if DSP is 0.)

- DCK bit
  - DCK = 1: The DOTCLK signal is generated internally.
  - DCK = 0: The DOTCLK signal is supplied externally.

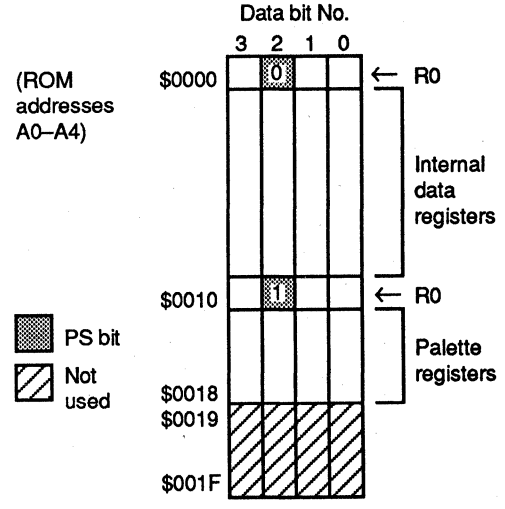

Figure 19 PS Bit Functions in ROM Programming Method

Control Register 2 (R1)

Control register 2 (figure 20) is composed of four bits whose functions are described below.

- MC bit: Specifies M signal alternation.
  - MC = 1: The M signal alternates every line.
  - MC = 0: The M signal alternates every frame.

- DON bit: Specifies whether the LCD is on or off.
  - DON = 1: LCD on
  - DON = 0: LCD off

- MS1, MS0 bits: Specify buffer memory type.
  - (MS1, MS0) = (0, 0): No memory
  - (MS1, MS0) = (0, 1): 8-kbytes memory
  - (MS1, MS0) = (1, 0): 32-kbytes memory
  - (MS1, MS0) = (1, 1): 64-kbytes memory

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4)

The vertical displayed lines register (figure 21) is composed of ten bits (R2, R3, and the high-order two bits of R4). It specifies the number of lines displayed from top to bottom of the screen, called the number of vertical displayed lines. This register can specify both even and odd numbers in single screen modes with Y-drivers positioned on one side, i.e., in display modes 2, 4, and 7–9, but can specify only even numbers in other modes. The value to be written into this register is Nvd – 1, where Nvd is the number of vertical displayed lines.

CL3 Period Register (Low-Order 2 Bits of R4, R5)

The CL3 period register (figure 21), is composed of six bits (R5 and the low-order two bits of R4). It specifies the CL3 signal period in 8-color display modes with horizontal stripes (display modes 13–15), so it is invalid in other modes. CL3 is the clock signal used by the LVIC-II to output RGB data separately to LCD drivers. The value to be written into this register is Npc – 1, i.e., (Nhd + 6) × 1/3 – 1, where Nhd is the number of horizontal displayed dots × 1/8. If (Nhd + 6) is not divisible by 3, round it off.

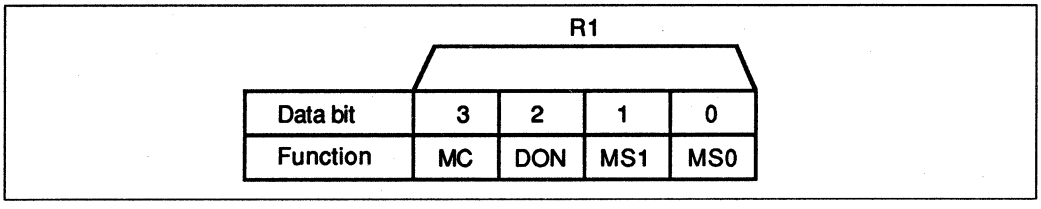

Figure 20 Control Register 2

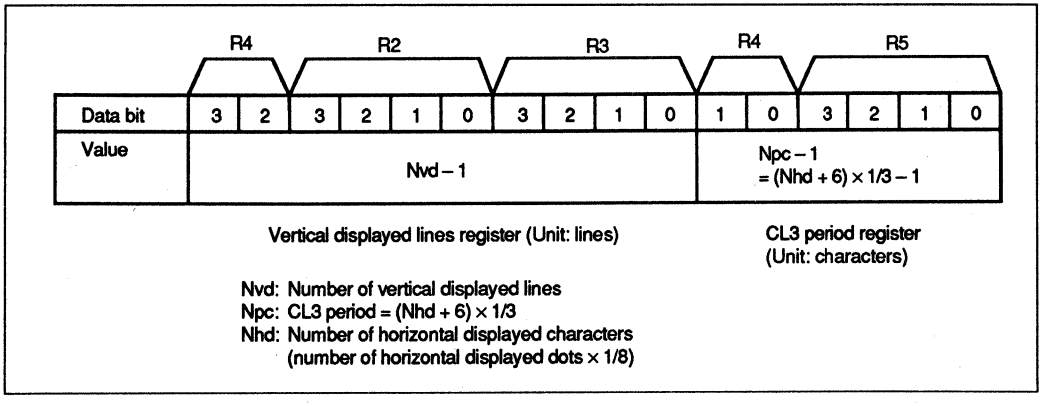

Figure 21 Vertical Displayed Lines Register and CL3 Period Register

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Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 22) is composed of eight bits (R6, R7). It specifies the number of characters displayed on one horizontal line, called the number of horizontal displayed characters.

This register can specify even numbers only. In dual-screen modes (display modes 1, 6, and 16), the most significant bit of this register is invalid. When writing into this register, shift (Nhd – 1) in the low-order direction for one bit to cut off the least significant bit. Figure 23 shows how to write a value into the register when Nhd = 90.

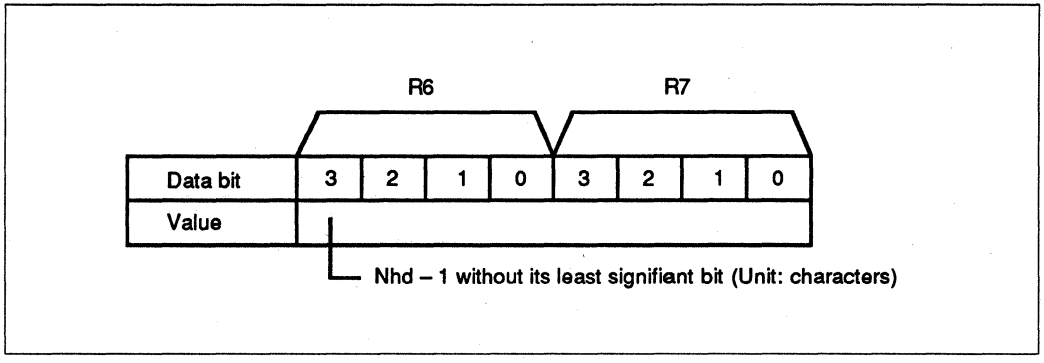

Figure 22 Horizontal Displayed Characters Register

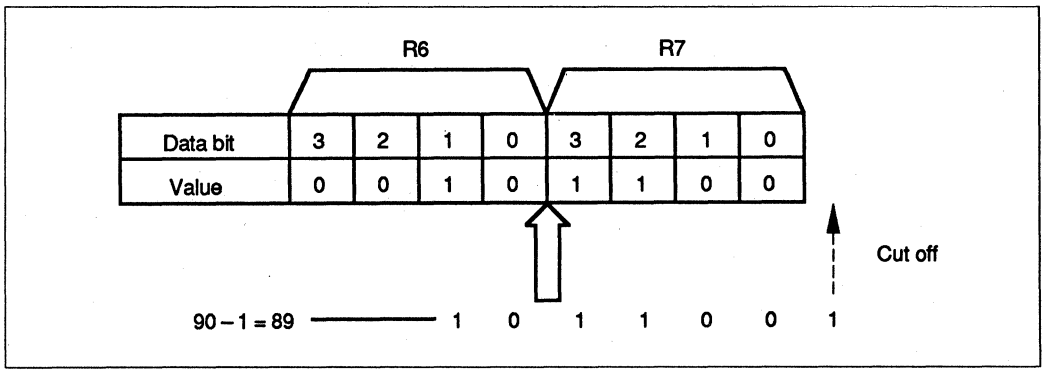

Figure 23 How to Write the Number of Horizontal Displayed Characters

CL3 Pulse Width Register (R8)

The 4-bit CL3 pulse width register (figure 24) specifies the high-level pulse width of the CL3 signal. In TFT-type LCD modes, a data hold time is necessary and it is determined by the high-level pulse width of the CL3 signal. The CL3 signal is output with the high-level pulse width specified by this register even when the LVIC-II is not in a TFT-type LCD mode.

Fine Adjust Register (R9)

The 4-bit fine adjust register (figure 25) adjusts the externally supplied display timing signal (DISPTMG) to synchronize its phase with that of LCD data. The value to be written into this register depends on the interval between the rising edge of the DISPTMG signal and the display start position. For more details, refer to the Display Timing Signal Fine Adjustment section and table 12. This register is invalid if the DISPTMG signal is generated internally, that is, if either the DCK bit or the DSP bit of control register 1 (R0) is 1.

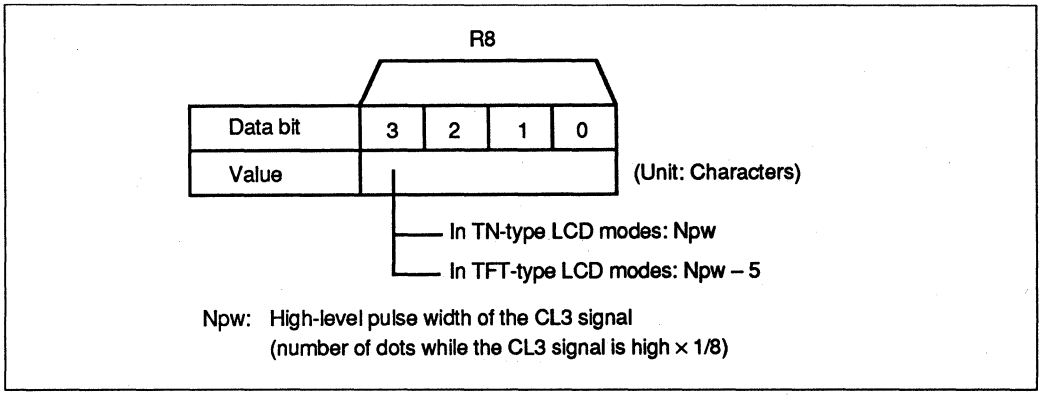

Figure 24 CL3 Pulse Width Resister

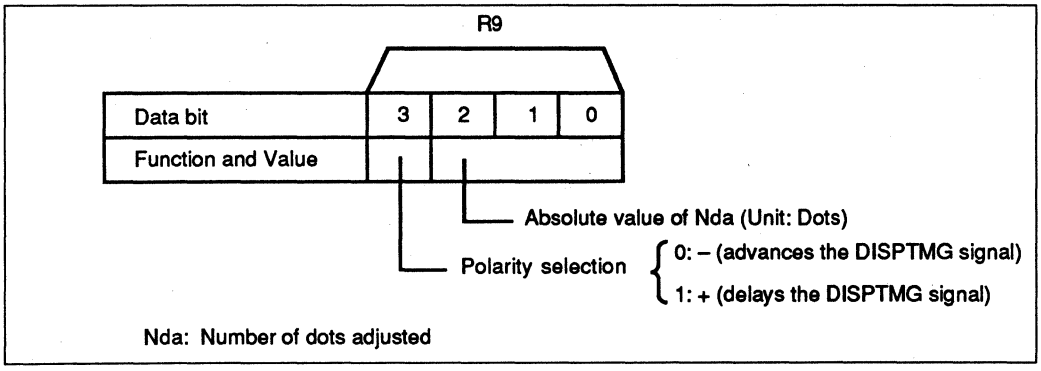

Figure 25 Fine Adjust Register

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PLL Frequency-Division Ratio Register (R10, R11)

The 8-bit PLL frequency-division ratio register (figure 26) specifies the PLL frequency-division ratio used for generating dot clock pulses by a PLL circuit. The PLL frequency-division ratio is the ratio of the DOTCLK signal's frequency to the horizontal synchronization signal's (HSYNC) frequency. The LVIC-II generates the DOTCLK signal according to this ratio. This register is invalid if the DOTCLK signal is supplied externally, i.e., it is valid only in the internal register programming method when the DCK bit of control register 1 (R0) is 0.

The value to be written into this register is N_{PLL} – 731, where N_{PLL} is the PLL frequency-division ratio which can be obtained from the following equation:

$N_{PLL} - 731 = Ncht \times n - 731$

Ncht: Total number of horizontal characters on CRT (Total number of horizontal dots on CRT × 1/n)

n: Horizontal character pitch (number of horizontal dots making up a character)

Ncht can be also obtained from the CRT monitor specifications as follows;

Ncht = 1/n × (DOTCLK frequency/HSYNC frequency)

Vertical Backporch Register (R12, R13)

The 8-bit vertical backporch register (figure 27) specifies the vertical backporch which is the number of lines between the active edge of the vertical synchronization signal (VSYNC) and the rising edge of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the vertical backporch, refer to the Display Timing Signal Generation section and figure 9.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

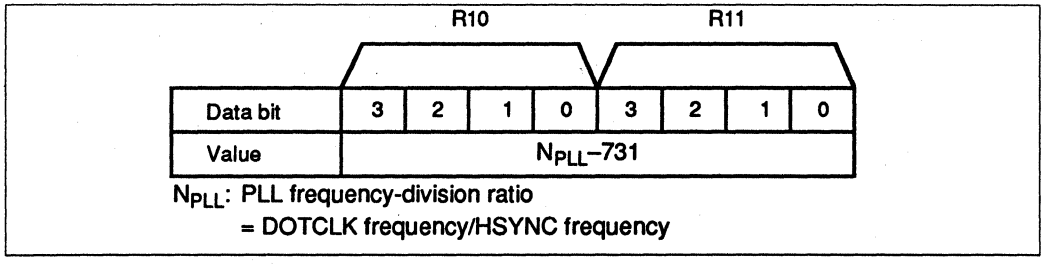

Figure 26 PLL Frequency-Division Ratio Register

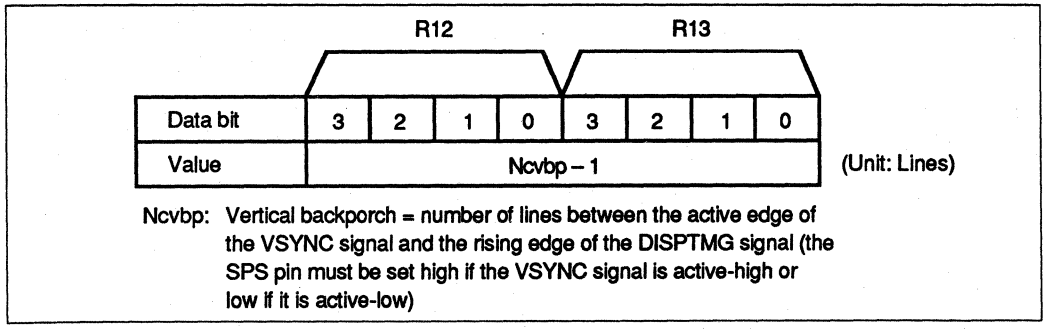

Figure 27 Vertical Backporch Register

Horizontal Backporch Register (R14, R15)

The 8-bit horizontal backporch register (figure 28) specifies the horizontal backporch which is the number of dots between the rising edge of the HSYNC signal and that of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the horizontal backporch, refer to the Display Timing Signal Generation section and figure 9.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

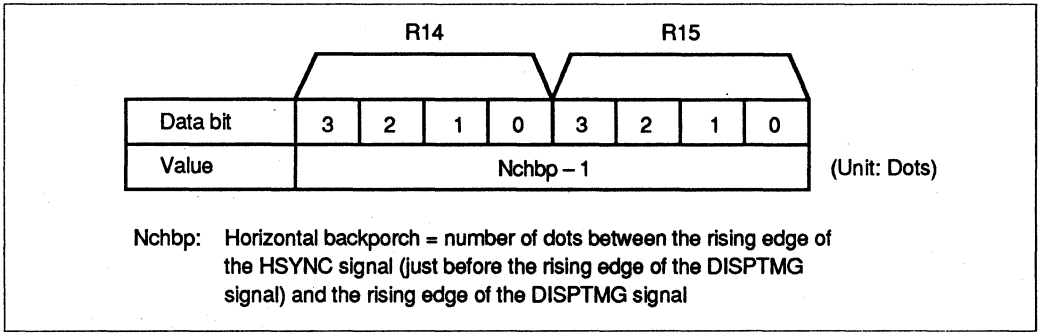

Figure 28 Horizontal Backproch Registers

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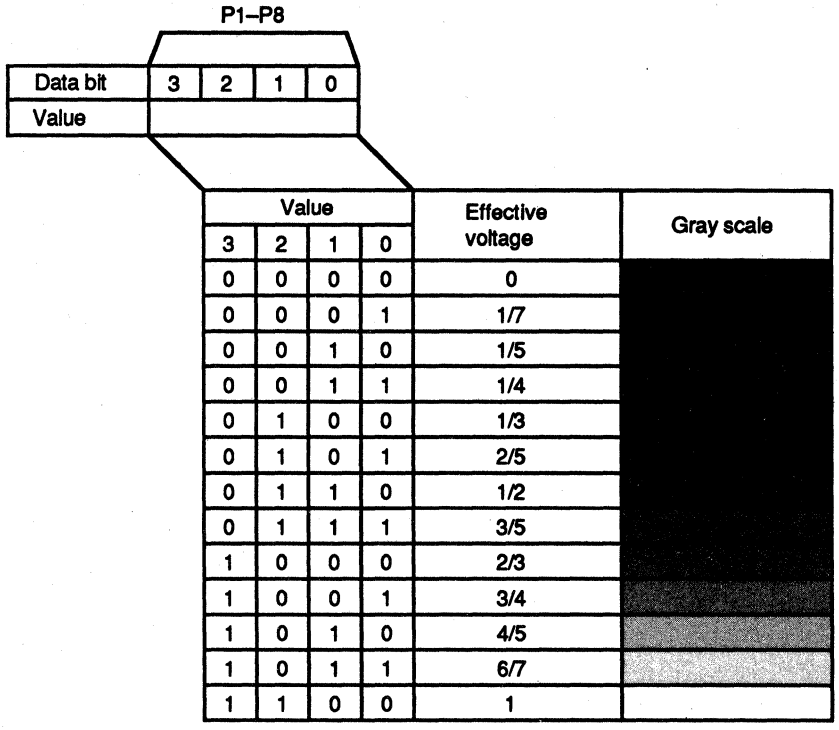
Palette Registers (P1–P8)

The eight 4-bit palette registers (figure 29) each specify one of 13 gray-scale levels for one of the eight colors provided by RGB signals. Use these registers to enable an 8-level gray-scale display appropriate to the characteristics of the LCD panel.



Value				Effective voltage	Gray scale
3	2	1	0		
0	0	0	0	0	
0	0	0	1	1/7	
0	0	1	0	1/5	
0	0	1	1	1/4	
0	1	0	0	1/3	
0	1	0	1	2/5	
0	1	1	0	1/2	
0	1	1	1	3/5	
1	0	0	0	2/3	
1	0	0	1	3/4	
1	0	1	0	4/5	
1	0	1	1	6/7	
1	1	0	0	1	

Figure 29 Palette Registers

Reset

The $\overline{RES}$ signal resets and starts the LVIC-II. The reset signal must be held low for at least 1 µs after power-on.
Reset is defined as shown in figure 30.

State of Pins after Reset

In principle, the $\overline{RES}$ signal does not control output signals and it operates regardless of other input signals. Output signals can be classified into the following five groups, depending on their reset states:

- Retains pre-reset state: CL2, A0–A4
- Driven to high-impedance state (or fixed low if no memory is used): RD0–RD7, GD0–GD7, BD0–BD7
- Fixed high: $\overline{MWE}$, CL4, M, $\overline{CU}$, $\overline{CD}$, $\overline{MCS1}$,
- Fixed low: MA0–MA12, R0–R3, G0–G3, B0–B3, CL3, FLM
- Fixed high or low, depending on memory used (table 13): MA13–MA15, $\overline{MCS0}$

State of Registers after Reset

The $\overline{RES}$ signal does not affect data register contents, so the MPU can both read from and write to data registers, even after reset. Registers will retain their pre-reset contents until they are rewritten.

The palette registers, however, are usually set to their default values by a reset. For the default values, refer to the Gray-Scale Palette section and table 11.

Memory Clear Function

After a reset, the LVIC-II writes 0s in the memory area specified by pins or register bits MS0 and MS1 (table 7).

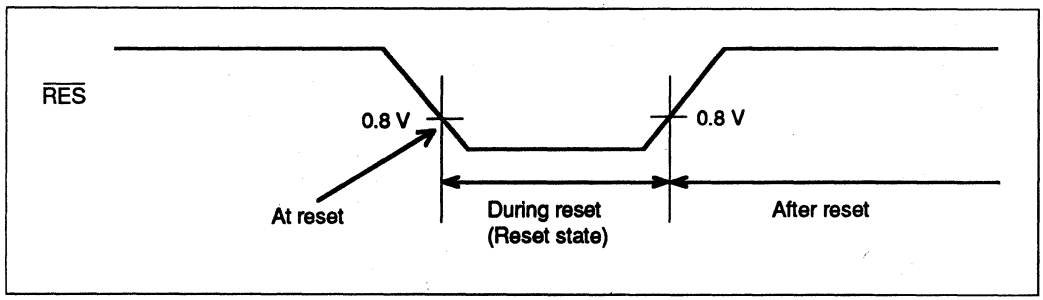


Figure 30 Reset Definition

Table 13 State of Pins after Reset and Memory Type

Memory Type	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbytes memory	High	High	High	Low
32-kbytes memory	Low	Low	High	Low
64-kbytes memory	Low	Low	Low	Low

User Notes

1. The following limitations are imposed if no memory is used (MS0 = 0, MS1 = 0):

   - Dual-screen display modes (modes 1, 6, and 16) are disabled.

   - LCD systems with Y-drivers on both sides are disabled, even if a mode for a system with Y-drivers on both sides (mode 3, 5, 10, 12, or 14) is selected; the LVIC-II operates in exactly the same way as in the corresponding mode for a system with Y-drivers on one side (mode 2, 4, 9, 11, or 13). The CL4 pin must be left disconnected in this case.

2. With the internal register programming method, the operation of the LVIC-II after a reset cannot be guaranteed until its internal registers have been written to.

3. The memory clear function might not work normally at power-on or after a reset if the MS0 and MS1 pins or bits are not set correctly to the value corresponding to the type of memory being used.

4. Since the LVIC-II is a CMOS LSI, input pins must not be left disconnected. Refer to the Pin Description and table 1 for details on pin handling.

Programming Restrictions

The values written into the LVIC-II's internal registers have the limits listed in table 14. The symbols used in table 14 are defined in table 15 and figure 31.

Table 14 Limits on Register Values

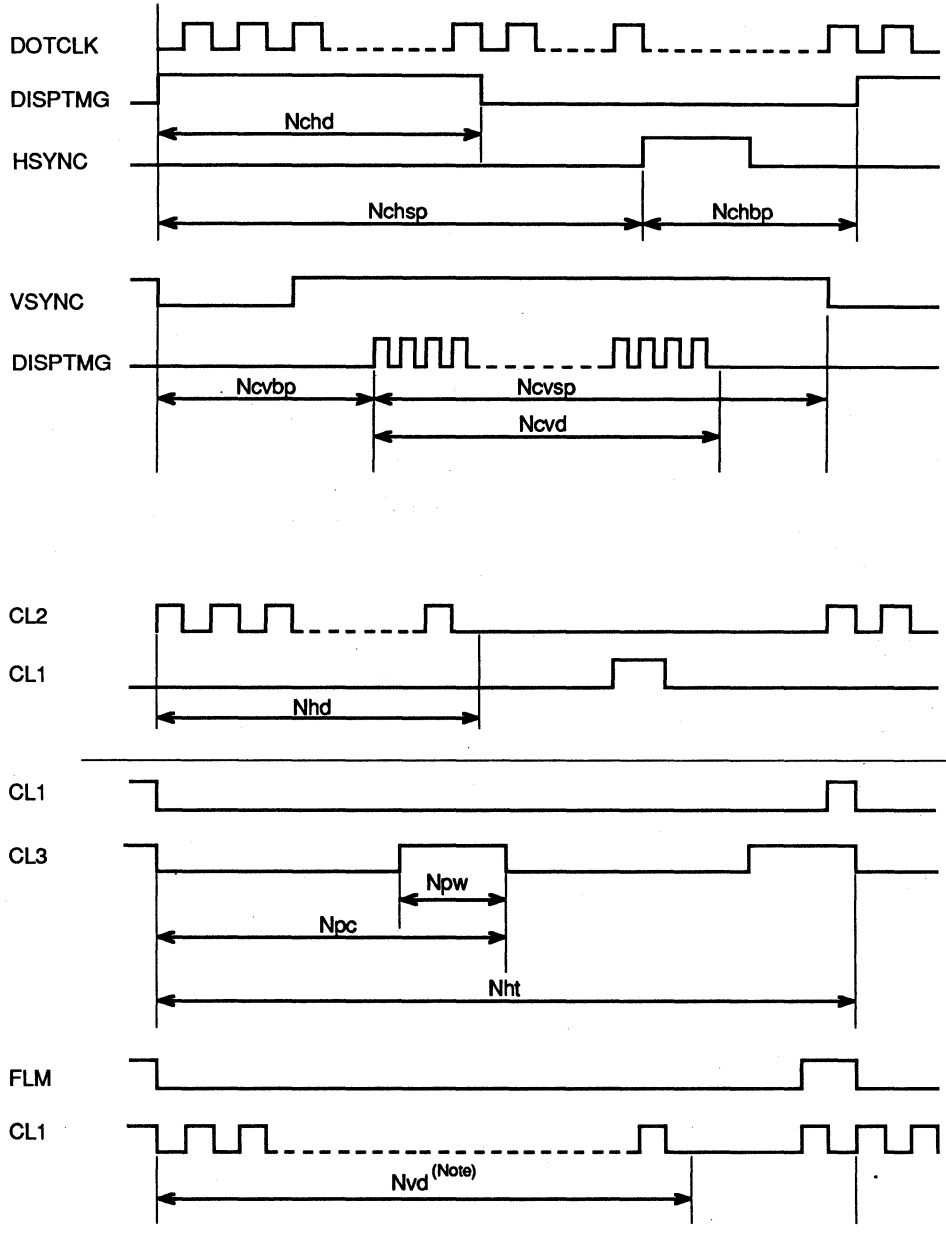
Item	Limits	Notes	Applicable Registers
Screen configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$		R2, R3, R4, R6, R7
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$	1, 2	
	$(Nhd + 6) \times n \times Nvd \times f_{FLM} \leqq f_{DOTCLK} \leqq$ 30MHz	1, 3	R2, R3, R4, R6, R7
CL3 signal control	$1 \leqq Npw \leqq (Nhd + 6)/2 - 1$	4	R4, R5, R6, R7, R8
	$1 \leqq Npw \leqq Nhd$	5	
	$1 \leqq Npw \leqq Npc - 1$	6	
DISPTMG signal generation	$1 \leqq Nchbp \leqq 256$	7	R12, R13
	$1 \leqq Ncvbp \leqq 256$	7	R14, R15
No memory	$4 \leqq Nhd \leqq Nchsp - 4$	8	R2, R3, R4,
	$4 \leqq Nvd \leqq Ncvsp - 1$	8	R6, R7

Notes:
1. Lowercase n indicates the horizontal character pitch which is the number of horizontal dots composing a character.
2. Nhd ≦ 250 in the dual screen modes (display modes 1, 6, and 16).
3. f_{FLM} is the FLM signal frequency and f_{DOTCLK} is the CRT display dot clock (DOTCLK) frequency.
   $f_{LDOTCK} < f_{DOTCLK} \times 15/16$ or $f_{LDOTCK} = f_{DOTCLK}$
   (f_{LDOTCK} is the LCD dot clock (LDOTCK) frequency)
4. In display modes 1, 2, 4, and 6–8
5. In display modes 3, 5, and 9–12 when Npw = (value in R8) + 5
6. In display modes 13–15 when Npw = (value in R8) + 5
7. (Value in R14 and R15) ≦ (Nchsp × n + Nchbp) – Nhd × n – 2
   (n = horizontal character pitch)
   (Value in R12 and R13) ≦ (Ncvsp + Ncvbp) – Nvd – 2
8. Nht = Nchsp + (Nchbp × 1/n), Nvd < Ncvbp + Ncvsp
   (Nht = (Nhd + 6) if buffer memory is used)
   (n = horizontal character pitch)

5

Table 15 Symbol Definitions

Symbol	Definition
Nchd	Number of horizontal displayed characters on the CRT display (number of horizontal displayed dots on the CRT display × 1/8)
Nchsp	Number of characters between the rising edge of the DISPTMG signal and that of the HSYNC signal (number of dots between the rising edge of the DISPTMG signal and that of the HSYNC signal × 1/8) (= horizontal synchronization position)
Nchbp	Number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal (just after the rising edge of the HSYNC signal) (= horizontal backporch)
Ncvbp	Number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal (just after the active edge of the VSYNC signal) (= vertical backporch)
Ncvsp	Number of lines between the rising edge of the DISPTMG signal and the active edge of the VSYNC signal (= vertical synch position)
Ncvd	Number of vertical displayed lines on the CRT display
Nhd	Number of horizontal displayed characters on the LCD (number of horizontal displayed dots on the LCD × 1/8)
Npc	Number of characters during one CL3 signal period (number of dots during one CL3 signal period × 1/8)
Npw	Number of characters while the CL3 signal is high (number of dots while the CL3 signal is high × 1/8)
Nht	Number of characters during a CL1 signal period (number of dots during a CL1 signal period × 1/8)
Nvd	Number of vertical displayed lines on the LCD



Note: For a dual screen, the Nvd period is doubled.

Figure 31 Symbol Definitions

Comparisons with HD66840F

Gray-Scale Generation Method

The HD66840F shifts display data so that data on different lines will be thinned out in different frames, but the HD66841F shifts display data further so that data on different dots will be thinned out in different frames. This reduces deterioration of display contrast.

Display Mode

Mode 16 of the HD66840F (for 8-color display with horizontal stripes and X- and Y-drivers positioned on both sides of the LCD) has been modified into the following new mode in the HD66841F:

Mode number:	16
Pin setting:	(DM3, DM2, DM1, DM0) = (1, 1, 1, 1)
Display colors:	8 colors
LCD data output:	–12-bit-based data transfer –Dual screen configuration
LCD driver settings:	X-drivers and Y-drivers set on one side
Stripes:	Vertical
Alternation mode:	Every frame

In this mode, the HD66841F outputs upper screen data and lower screen data alternately, as shown in figure 32. In this case, the CL2 frequency is one quarter of the LDOTCK frequency.

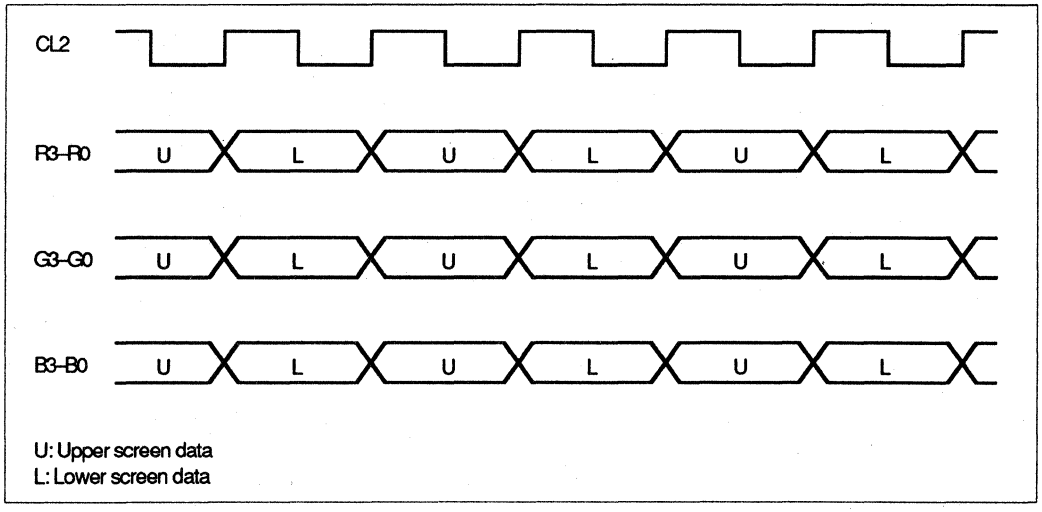


Figure 32 Operation in New HD66841F Mode 16

Table 16 Gray-Scale Palette

	HD66840F	HD66841F
Numbers of registers	16	24 (palette registers have been added to the HD66840's registers)
Selection of correspondence between CRT display colors and gray-scale levels	Impossible	Possible (any of 13 levels assignable to each of 8 colors)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	–0.3 to 7.0	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0V ± 10%, GND = 0 V, Ta = –20°C to +75°C). If these conditions are exceeded, LSI reliability may be affected.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Conditions	Note(s)
Input high voltage						
$\overline{RES}$ pin	V_{IH}	V_{CC} – 0.5	V_{CC} + 0.3	V		
TTL interface pins		2.0	V_{CC} + 0.3			1
TTL interface pins		2.2	V_{CC} + 0.3			4
CMOS interface pins		0.7 V_{CC}	V_{CC} + 0.3			1
Input low voltage						
TTL interface pins, $\overline{RES}$ pin	V_{IL}	–0.3	0.8	V		1
TTL interface pins		–0.3	0.6			5
CMOS interface pins		–0.3	0.3 V_{CC}			1
Output high voltage						
TTL interface pins	V_{OH}	2.4	—	V	I_{OH} = –200 µA	2
CMOS interface pins		V_{CC} – 0.8	—		I_{OH} = –200 µA	
Output low voltage						
TTL interface pins	V_{OL}	—	0.4	V	I_{OL} = 1.6mA	2
CMOS interface pins		—	0.8		I_{OL} = 200µA	
Input leakage current						
All inputs expect	I_{IL}	–2.5	2.5	µA		3
I/O common pins						
Three-state (off-state) leakage current						
I/O common pins	I_{TSL}	–10.0	10.0	µA		3
Power dissipation	I_{CC}	—	250	mW	f_{DOTCLK} = 30 MHz, output pins left disconnected	

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Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0–RD7, GD0–GD7, BD0–BD7, D0–D3, A0/$\overline{RD}$/XDOT, RS/ADJ/A4, $\overline{CS}$/MS0
CMOS interface inputs: DM0–DM3, DOTE, PMOD0, PMOD1, A1/YL0–A3/YL2

2. TTL interface inputs: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, MA0–MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$, RS/ADJ/A4
CMOS interface inputs: $\overline{CU}$, $\overline{CD}$, R0/LU0–R3/LU3, G0/LD0–G3/LD3, B0–B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, RS/ADJ/A4
Inputs other than I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE , DM0–DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

4. TTL interface inputs: $\overline{WR}$/MS1, LDOTCK, DOTCLK

5. TTL interface inputs: $\overline{WR}$/MS1

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C)

Video Signal Interface

Item	Symbol	Min	Max	Unit	Reference
DOTCLK cycle time	t_{CYCD}	33	1000	ns	Figure 33
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
RGB setup time	t_{VDS}	10	—	ns	
RGB hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Figure 33 except for DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	

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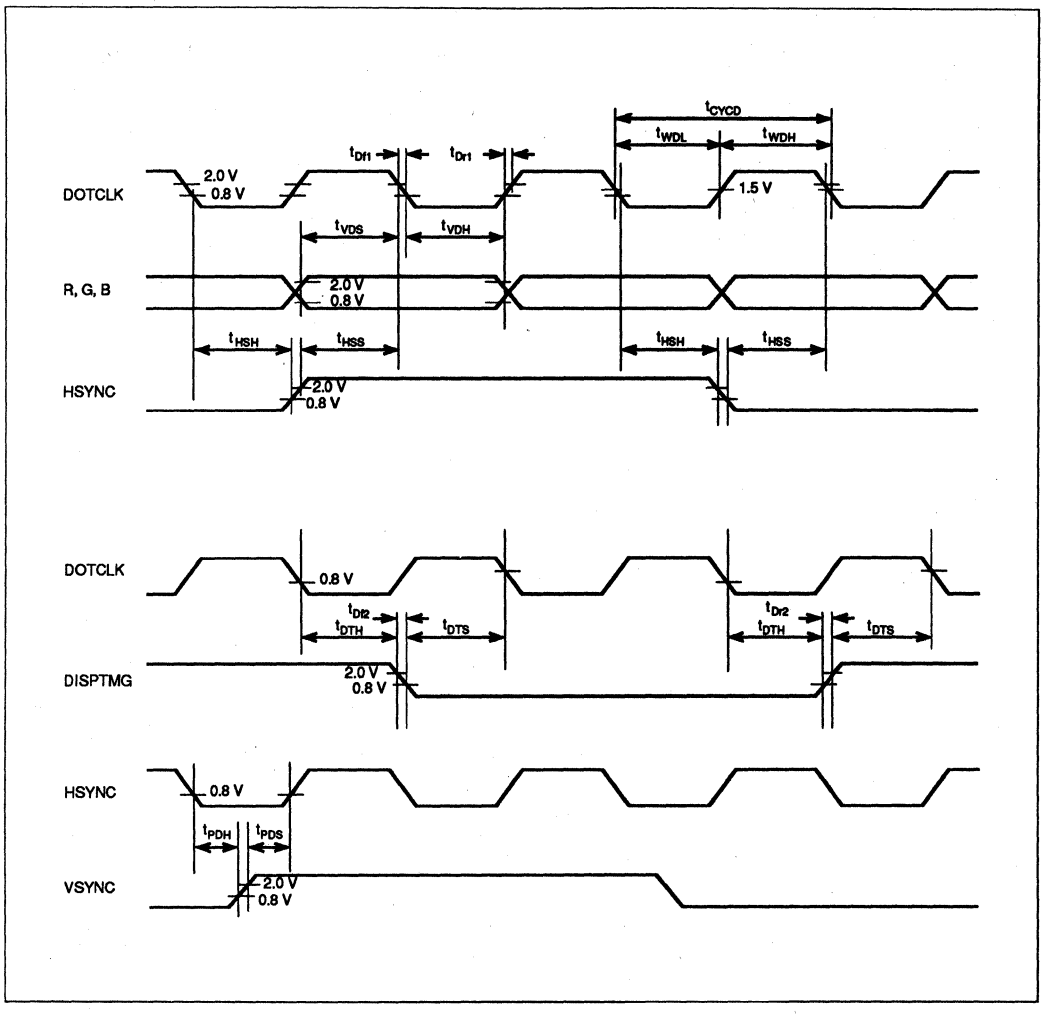

Figure 33 Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Unit	Reference
Read cycle time	t_{RC}	$5\,t_{CYCD} - 50$	ns	Figures 34 and 35
RD0–RD7, GD0–GD7, BD0–BD7 data setup time	t_{SMD}	25	ns	
RD0–RD7, GD0–GD7, BD0–BD7 data hold time	t_{HMD}	0	ns	
Write cycle time	t_{WC}	$6\,t_{CYCD} - 50$	ns	
Address setup time	t_{MAS}	$t_{CYCD} - 30$	ns	
Address hold time	t_{WR}	$t_{CYCD} - 30$	ns	
Chip select time	t_{CW}	$4\,t_{CYCD} - 40$	ns	
Write pulse width	t_{WP}	$4\,t_{CYCD} - 40$	ns	
RD0–RD7, GD0–GD7, BD0–BD7 output setup time	t_{SMDW}	$2\,t_{CYCD} - 25$	ns	
RD0–RD7, GD0–GD7, BD0–BD7 output hold time	t_{HMDW}	0	ns	

Note: t_{CYCD} is the DOTCLK cycle time (min 33 ns, max 1000 ns).

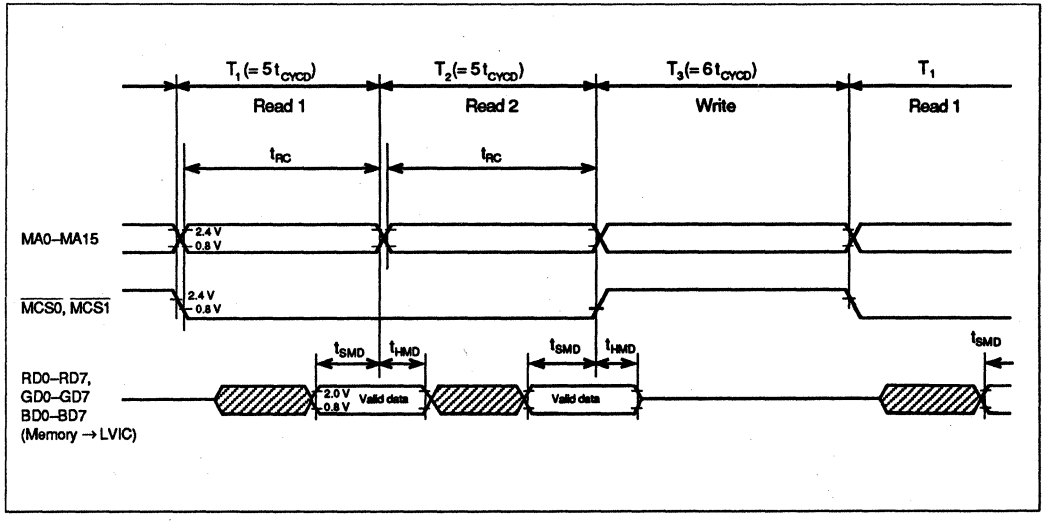

Figure 34 Buffer Memory Interface (RAM read timing)

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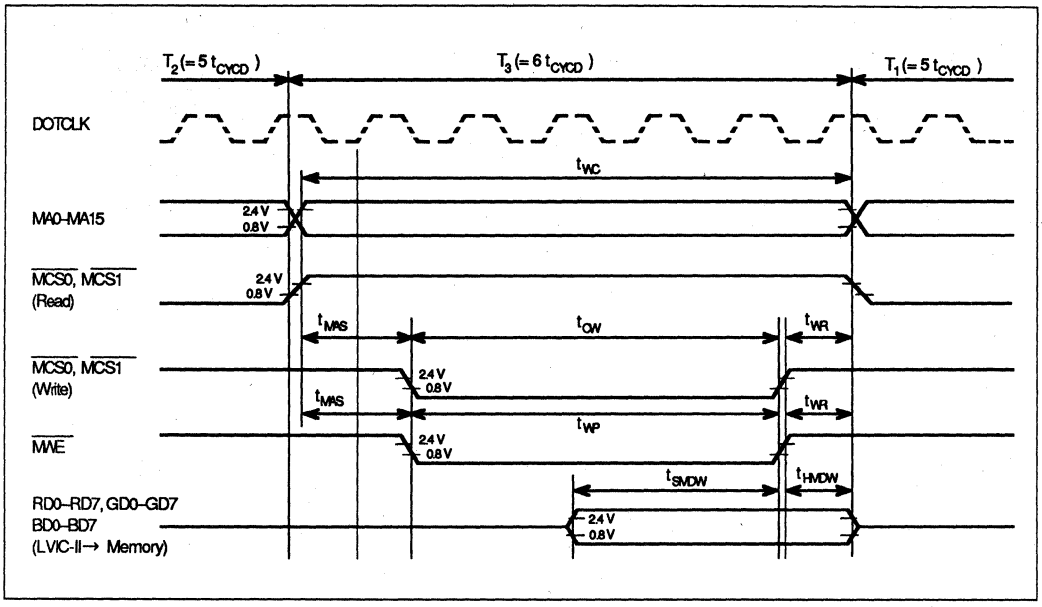


Figure 35 Buffer Memory Interface (RAM write timing)

LCD Driver Interface

TN-Type LCD Driver

Item	Symbol	Min	Max	Unit	Reference
CL2 cycle time	t_{WCL2}	166	—	ns	Figures 36 and 37
CL2 high-level pulse width	t_{WCL2H}	50	—	ns	
CL2 low-level pulse width	t_{WCL2L}	50	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{WCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
CL1 setup time	t_{SCL1}	500	—	ns	
CL1 hold time	t_{HCL1}	200	—	ns	
FLM hold time	t_{HF}	200	—	ns	
M output delay time	t_{DM}	—	300	ns	
Data delay time	t_{DD}	–20	20	ns	
LDOTCK cycle time	t_{WLDOT}	41	—	ns	

Note: All values are measured at f_{CL2} = 6 MHz.

TFT-Type LCD Driver

Item	Symbol	Min	Max	Unit	Reference
CL2 cycle time (X-drivers on one side)	t_{TCL2S}	133	—	ns	Figures 38 and 39
CL2 high-level pulse width (X-drivers on one side))	t_{TCL2HS}	30	—	ns	
CL2 low-level pulse width (X-drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X-drivers on both sides)	t_{TCL2D}	266	—	ns	
CL2 high-level pulse width (X-drivers on both sides)	t_{TCL2HD}	80	—	ns	
CL2 low-level pulse width (X-drivers on both sides)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	–20	20	ns	
Data setup time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	33	—	ns	

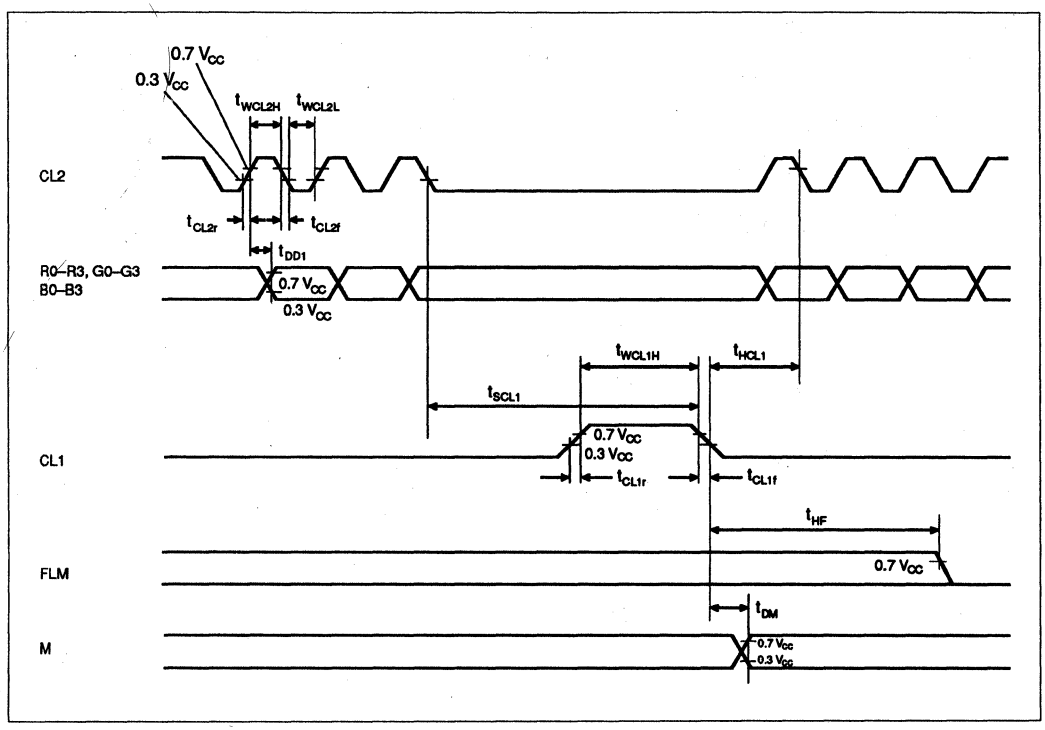


Figure 36 TN-Type LCD Driver Interface

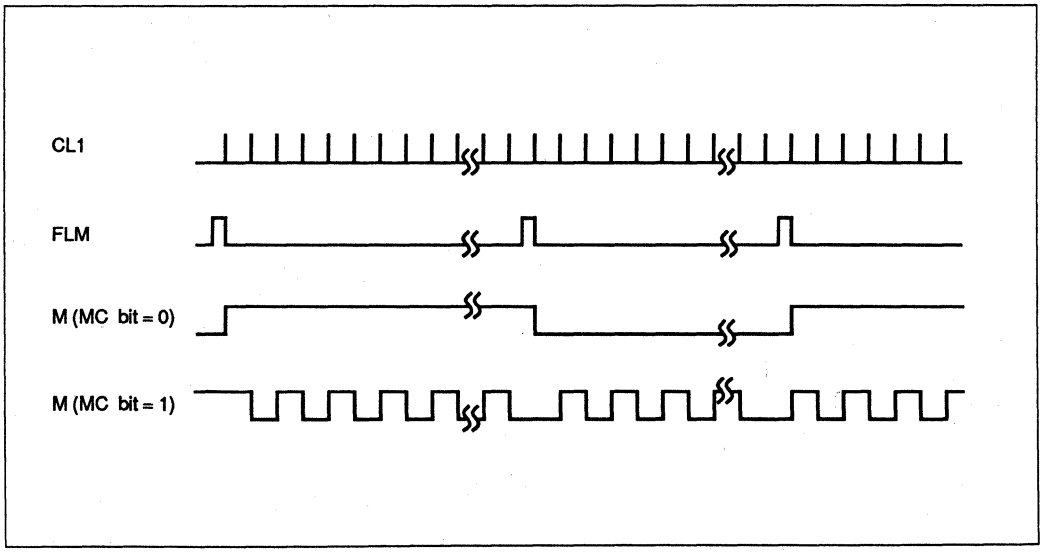


Figure 37 CL1, FLM, and M (expanded detail of figure 36)

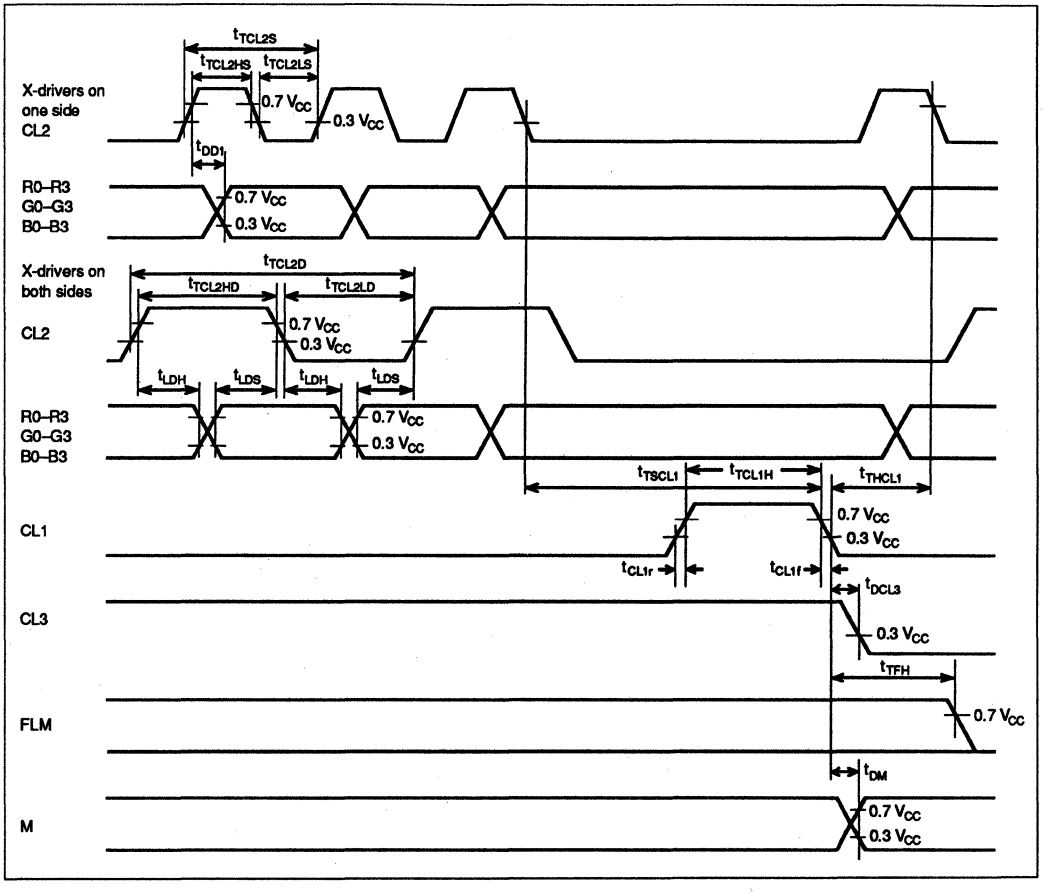


Figure 38 TFT-Type LCD Driver Interface

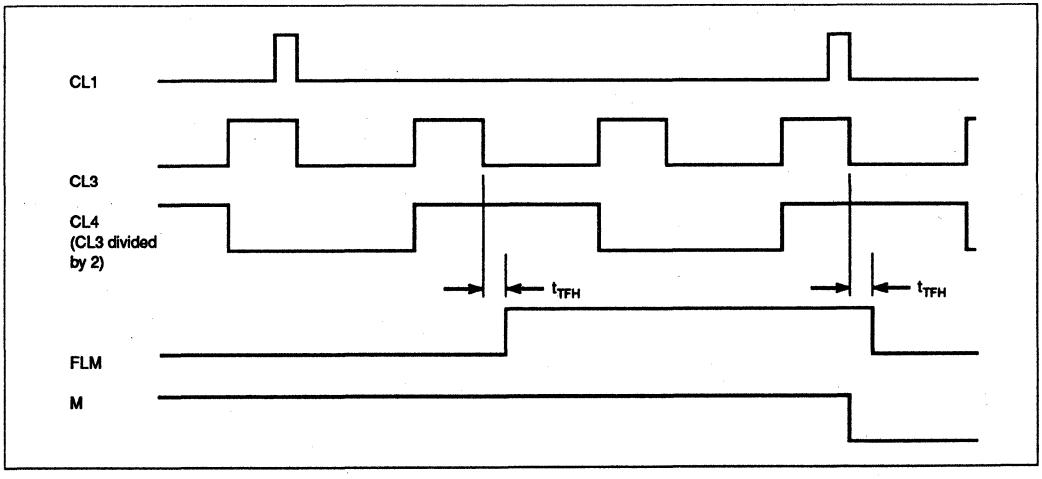


Figure 39 CL1, CL3, CL4, FLM, and M in Horizontal Stripe Modes (expanded detail of figure 38)

Register Programming

MPU Interface

Item	Symbol	Min	Max	Unit	Reference
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns	Figure 40
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns	
$\overline{WR}$ high-level pulse width	t_{WWRH}	190	—	ns	
$\overline{WR}$ low-level pulse width	t_{WWRL}	190	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns	
D0–D3 setup time	t_{DSW}	100	—	ns	
D0–D3 hold time	t_{DHW}	0	—	ns	
D0–D3 output delay time	t_{DDR}	—	150	ns	
D0–D3 output hold time	t_{DHR}	10	—	ns	

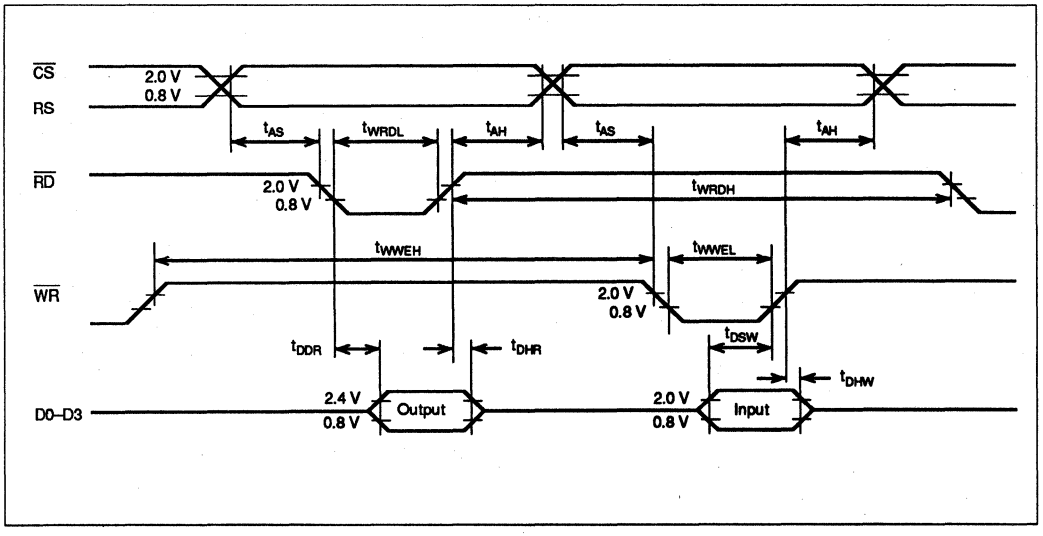


Figure 40 MPU Interface

ROM Interface

Item	Symbol	Min	Max	Unit	Reference
A signal cycle time	t_{CYCA}	528	—	ns	Figure 41
A signal rise time	t_{Ar}	—	100	ns	
A signal fall time	t_{Af}	—	100	ns	
D signal ROM data setup time	t_{DSWD}	120	—	ns	
D signal ROM data hold time	t_{DHWD}	0	—	ns	

Note: $t_{CYCA} = 16\ t_{CYCD}$ (t_{CYCD}: DOTCLK cycle time)

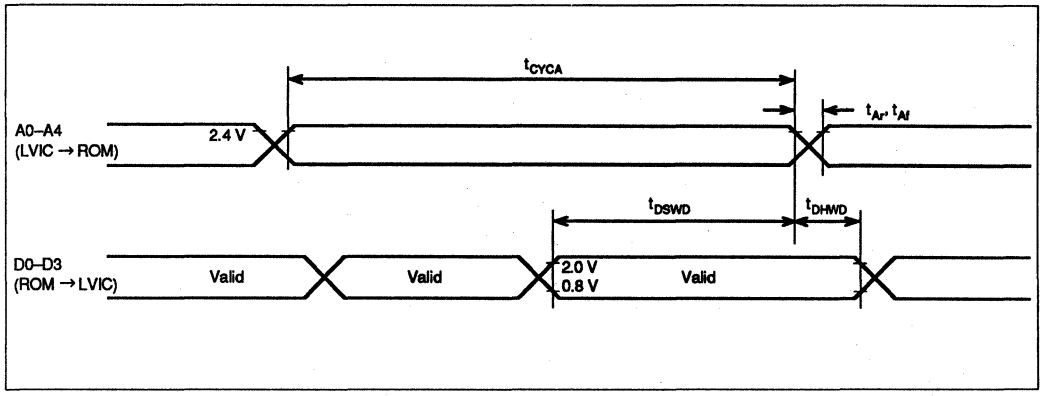


Figure 41 ROM Interface

PLL Interface

Item	Symbol	Min	Max	Unit	Referenc2
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns	Figure 42
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns	
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns	
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns	

Reset Input

Item	Symbol	Min	Max	Unit	Reference
Reset input pulse width	$t_{\overline{RES}}$	1	—	µs	Figure 43

5

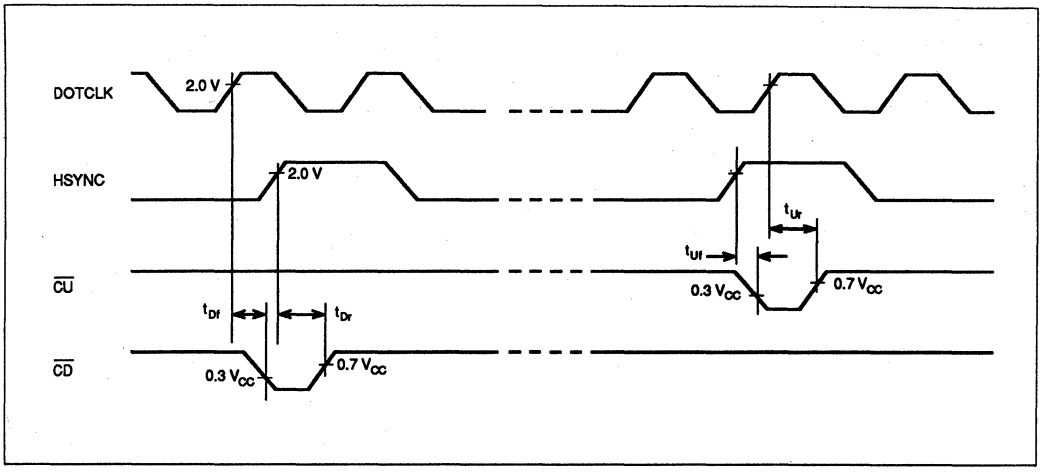


Figure 42 PLL Interface

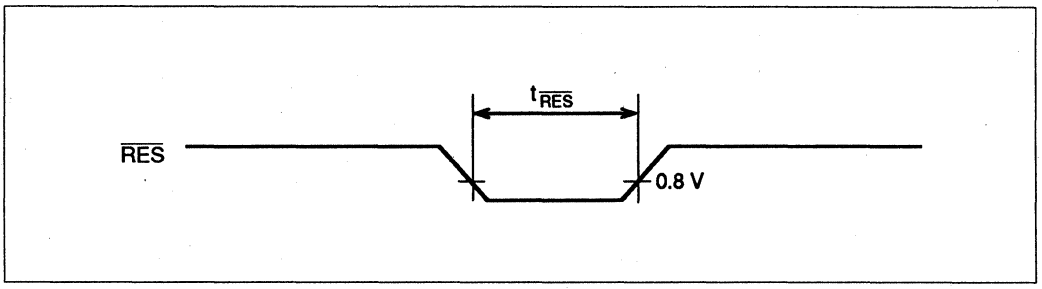


Figure 43 Reset Input

Load Circuits

TTL Load

Pins	R_L	R	C	Remarks
MA0–MA15, $\overline{MWE}$, $\overline{MCS0}$, $\overline{MCS1}$, BD0–BD7, GD0–GD7, RD0–RD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, A4/RS/ADJ	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pins	C	Remarks
CL1, CL2	40 pF	tr, tf: Specified
R0–R3, G0–G3, B0–B3, FLM, M, $\overline{CU}$, $\overline{CD}$, CL3, CL4	40 pF	tr, tf: Not specified

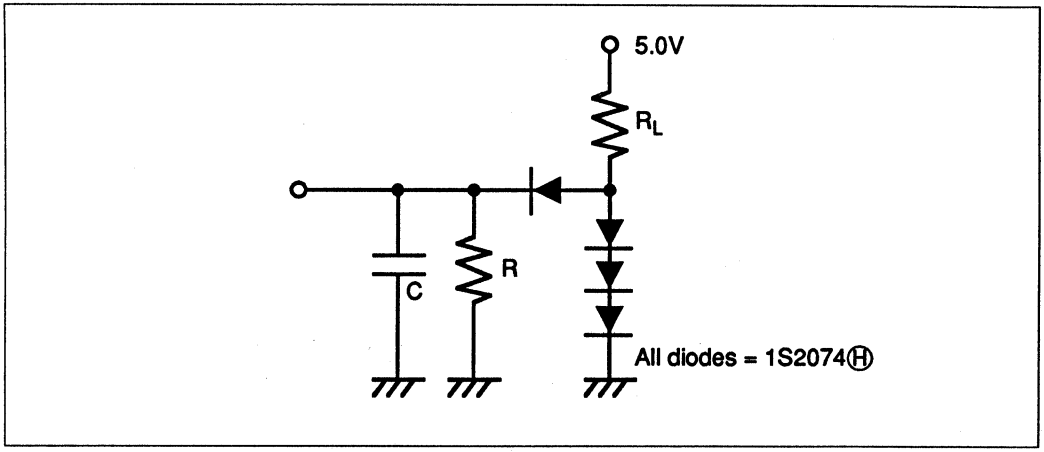


Figure 44 TTL Load Circuit

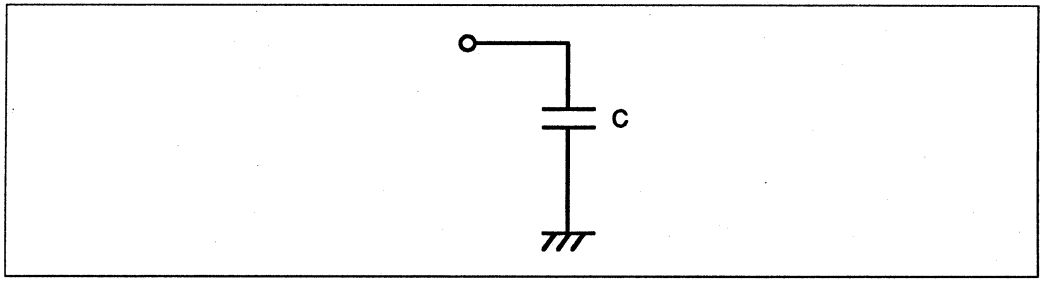


Figure 45 Capacitive Load Circuit

5

HD66850F
Color LCD Interface Engine (CLINE)

Description

The HD66850F CLINE interface controller converts multi-color video signals for CRT display into color or monochrome LCD data.

This device enables an LCD system to replace a CRT display system without any changes to the original display system. It automatically adapts to display modes of the IBM-VGA (Video Graphics Array™) system, facilitating the configuration of an LCD system.

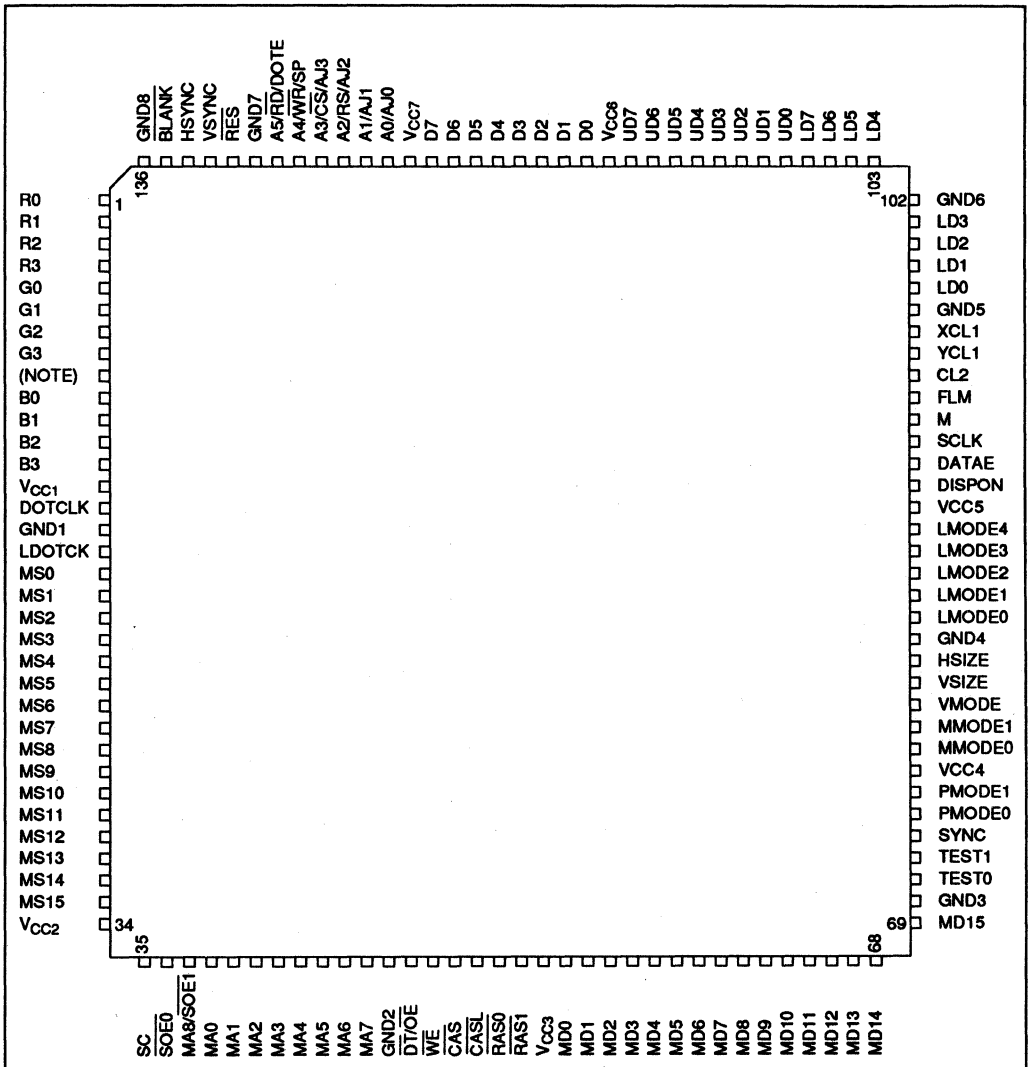
The CLINE can control TN-type (Twisted rematic) color and monochrome LCDs and can display a maximum of 4096 color levels or 16 gray levels.

Note: Video Graphics Array is a trademark of International Business Machines Corporation, U.S.A.

Features

- Various LCD panel sizes supported
  - — 640 or 720 dots wide
  - — 32 to 512 lines high
- Programmable display size
  - — 32 to 720 dots wide
  - — 32 to 512 lines high
- Easy-to-see display
  - — Centering
  - — Stretching (display stretched to fill out the panel)
- Improved gradation display quality using the pulse width modulation method
- Desired gradation levels assignable to each display color through the use of internal gradation level palettes
- Changeable LCD frame frequency
  - — Through the use of a multi-port RAM frame buffer
  - — Within the range of 1/2 to 2 times of CRT display dot clock frequency
- High-speed operating frequency: 32 MHz (CRT display dot clock)
- Recommended LCD drivers: HD66106 and HD66107T (column and common drivers)
- Single power supply: +5 V
- 136-pin flat plastic package (FP-136)

Pin Arrangement



Note: Pin No. 9 is not used; must be fixed low.

5

Pin Description

Type	Symbol	Pin No.	Pin Name	I/O	Function
Power supply	$V_{CC}1$ – $V_{CC}7$	14, 34, 53, 76, 88, 115, 124	$V_{CC}1$ – $V_{CC}7$	—	All of these pins must be connected to a +5V supply
	GND1 – GND8	16, 46, 70, 82, 97, 102, 131, 136	GND1 – GND7	—	All of these pins must be grounded.
MPU/ROM or program interface	D0 – D7*1	(M) 116 – 123	Data 0 – 7	I/O	Transfer data between internal registers and MPU
	D0 – D7*1	(R) 116 – 123	Data 0 – 7	I	Input data to internal registers from external ROM
	DOTE	(P) 130	Dot clock edge change	I	Switches RGB data latch timing High: Data latched at the rising edge of DOTCLK pulses Low: Data latched at the falling edge of DOTCLK pulses
	$\overline{RD}$	(M) 130	Read	I	Inputs a read signal for reading data from internal registers
	A5	(R) 130	Address 5	O	Outputs external ROM address 5
	SP	(P) 129	Spread display select I	I	Selects either of the following display size modes High: Double – width display Low: Normal display
	$\overline{WR}$	(M) 129	Write	I	Inputs a write signal for writing data to internal registers
	A4	(R) 129	Address 4	O	Outputs external ROM address 4
	AJ3	(P) 128	Adjust 3	I	Adjusts the display timing signal (table 1)
	$\overline{CS}$	(M) 128	Chip select	I	Inputs a chip select signal to select the CLINE High: The CLINE not selected Low: The CLINE selected
	A3	(R) 128	Address 3	O	Outputs external ROM address 3
	AJ2	(P) 127	Adjust 2	I	Adjusts the display timing signal (table 1)
	RS	(M) 127	Register select	I	Inputs a register select signal to select either CLINE data registers or index register High: Data registers Low: The index register
	A2	(R) 127	Address 2	O	Outputs external ROM address 2
	AJ0, AJ1*2	(P) 125, 126	Adjust 0, 1	I	Adjust the display timing signal (table 1)
	A0, A1*2	(R) 125, 126	Address 0, 1	O	Output external ROM addresses 0 and 1, respectively

(M): For MPU programming method (R): For ROM programming method (P): For pin programming method
I/O: Input/Output

Pin Description (cont.)

Type	Symbol	Pin No.	Pin Name	I/O	Function
CRT interface	R0 – R3*3	1 – 4	Red serial data 0 – 3	I	Input CRT display R data
	G0 – G3*3	5 – 8	Green serial data 0 – 3	I	Input CRT display G data or monochrome data
	B0 – B3*3	10 – 13	Blue serial data 0 – 3	I	Input CRT display B data: For monochrome display, B1 selects 16-gray-scale display and B0 indicates the type of CRT display data input. B1 = high: Prohibited B1 = low: 16-level gray scale display B0 = high: 64-color data input B0 = low: 16-level gray scale data input
	DOTCLK	15	Dot clock	I	Inputs the dot clock pulses for CRT display
	HSYNC	134	Horizontal synchronization	I	Inputs the CRT horizontal synchronization signal
	VSYNC	133	Vertical synchronization	I	Inputs the CRT vertical synchronization signal
	$\overline{\text{BLANK}}$	135	Blanking	I	Inputs a display timing siganl indicating horizontal or vertical display period, or a blank signal indicating the display period with border area period
LCD interface	UD4 – UD7*4	111 – 114	LCD upper panel data 4 – 7	O	Output LCD upper panel data or R data
	UD0 – UD3*4	107 – 110	LCD upper panel data 0 – 3	O	Output LCD upper panel data or G data
	LD4 – LD7*4	103 – 106	LCD lower panel data 4 – 7	O	Output LCD lower panel data or B data
	LD0 – LD3*4	98 – 101	LCD lower panel data 0 – 3	O	Output LCD lower panel data or I data
	XCL1*4	96	X-driver latch clock	O	Outputs the LCD data latch clock pulses for X-drivers
	YCL1	95	Y-driver shift clock	O	Outputs the LCD data line shift clock pulses for Y-drivers
	CL2	94	Y-driver shift clock	O	Outputs the LCD data line shift clock pulses for Y-drivers
	FLM	93	First line maker	O	Outputs the first line maker for Y-drivers

I/O: Input/Output

Pin Description (cont.)

Type	Symbol	Pin No.	Pin Name	I/O	Function
LCD interface	M	92	M	O	Outputs a signal for converting LCD drive signals to AC
	SCLK	91	Shift lock	O	Outputs clock pulse with a frequency identical to CL2 but without a retrace period
	DATAE*4	90	Data enable	O	Indicates LCD data display period
	DISPON*4	89	Display on	O	Controls LCD on/off
	LDOTCK	17	LCD dot clock	I	Inputs LCD dot clock pulses
Buffer memory interface	MD0 – MD15*5	54 – 69	Memory data 0 – 15	O	Output data to be written to buffer memory
	MS0 – MS15*6	18 – 33	Memory serial data 0 – 15	I	Input data read from buffer memory
	MA0 – MA7*5	38 – 45	Memory address 0 – 7	O	Output buffer memory addresses 0 – 7
	MA8/ $\overline{\text{SOE1}}$*5	37	Memory address 8/ serial output enable 1	O	Outputs buffer memory address 8 when 1-Mbit RAMs are used or outputs a serial data output enable signal when 256-kbit RAMs are used
	$\overline{\text{SOE0}}$*5	36	Serial output enable 0	O	Output a serial data output enable signal for buffer memory
	$\overline{\text{WE}}$*5	48	Write enable	O	Outputs a write enable signal for buffer memory
	$\overline{\text{DT/OE}}$*5	47	Data transfer/output enable	O	Outputs a data transfer signal or an output enable signal for buffer memory
	$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$*5	51, 52	Row address strobe 0, row address strobe 1	O	Outputs a row address strobe signal for buffer memory
	$\overline{\text{CAS}}$, $\overline{\text{CASL}}$*5	49, 50	Column address strobe	O	Outputs a column address strobe signal for buffer memory
	SC*5	35	Serial clock	O	Outputs serial read clock pulses for buffer memory
Mode control	PMODE0, PMODE1	74, 75	Program mode 0, program mode 1	I	Select a CLINE programming method (table 2)
	LMODE0 – LMODE4	83 – 87	LCD mode 0 – 4	I	Select a display mode (table 7)
	MMODE0, MMODE1	77, 78	Memory mode 0, 1	I	Select a memory configuration (table 3)
	SYNC	73	Synchronization	I	Select a basic clock for LCD High: DOTCLK Low: LDOTCK

I/O: Input/Output

Pin Description (cont.)

Type	Symbol	Pin No.	Pin Name	I/O	Function
Mode control (cont)	VMODE	79	VGA mode	I	Specifies a CRT display system High: Non-VGA system Low: VGA system
	VSIZE	80	LCD vertical size	I	Specifies the vertical size of the LCD panel High: 480 lines Low: 400 lines
	HSIZE	81	LCD horizontal size	I	Specifies the horizontal size of the LCD panel High: 720 dots Low: 640 dots
	$\overline{RES}$	132	Reset	I	Inputs an external reset signal
	TEST0, TEST1	71, 72	Test 0, 1	I	Used for tests; Must be grounded

I/O: Input/Output

Notes: 1. Must be fixed low for pin programming method.
2. Must be fixed low for MPU programming method.
3. Must be fixed low when not used.
4. Must be left disconnected when not used.
5. Must be left disconnected when buffer memory is not used.
6. Must be fixed low when buffer memory is not used.

Table 1 Display Timing Signal Fine Adjustment

Pin				Number of Dots Adjusted
AJ3	AJ2	AJ1	AJ0	
0	0	0	0	0
0	0	0	1	–1
0	0	1	0	–2
1	0	0	0	0
1	0	0	1	+1
1	0	1	0	+2
1	0	1	1	+3
1	1	0	0	+4
1	1	0	1	+5
1	1	1	0	+6

Note: – (minus) indicates advancing the phase of the display timing signal,
+ (plus) indicates delaying the phase of the display timing signal.

5

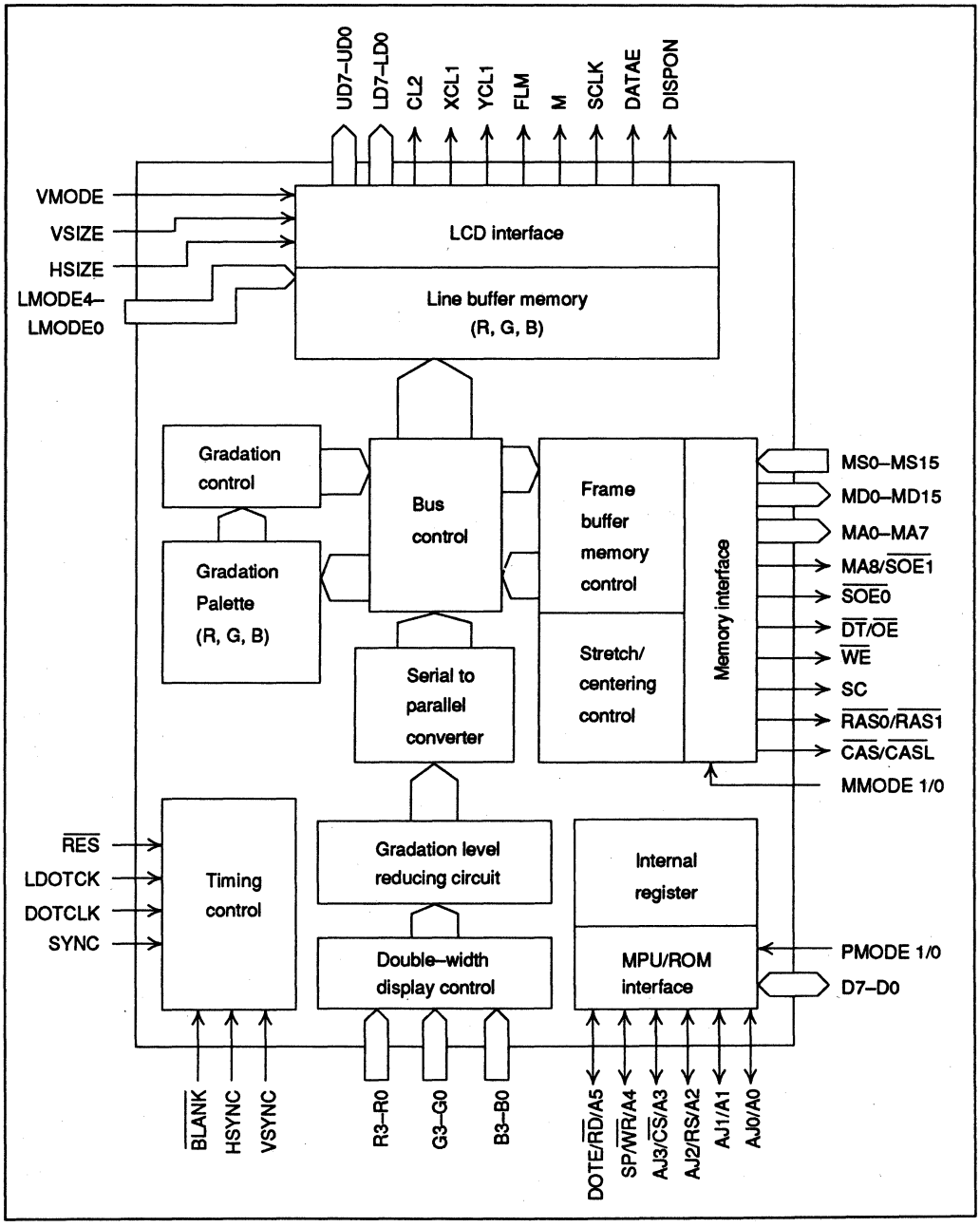
Table 2 Programming Method Selection

Pin		
PMODE1	**PMODE0**	**Programming Method**
0	0	Pin
0	1	Internal registers (MPU)
1	0	Internal registers (ROM)
1	1	Prohibited

Table 3 Memory Configuration Selection

Pin		
MMODE1	**MMODE0**	**Memory Configuration**
0	0	1-Mbit RAM
0	1	256-kbit RAM
1	0	No memory
1	1	No memory (when the CRT controller supports dual screen display)

Block Diagram



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Register List

CLINE registers are summarized in table 4.

Table 4 Register List

CS	RS	Index Reg 3	2	1	0	Reg. No.	Register Name	Program Units	Read/ Write	Data Bits 7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
0	0	0	0	0	0	IR	Index	—	W	—	—	—	—	IA3	IA2	IA1	IA0
0	1	0	0	0	0	R0	Control	—	R/W	—	—	—	STE	CRE	CCE	SP	DISP ON
0	1	0	0	0	1	R1	Input timing control	Dot	R/W	—	—	—	DOTE	AJ3	AJ2	AJ1	AJ0
0	1	0	0	1	0	R2	Horizontal display size	Character	R/W	—	DH6	DH5	DH4	DH3	DH2	DH1	DH0
0	1	0	0	1	1	R3	Vertical display size (high-order)	Line	R/W	—	—	—	—	—	—	—	DV8
0	1	0	1	0	0	R4	Vertical display size (low-order)	Line	R/W	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0
0	1	0	1	0	1	R5	Centering raster	Line (Raster)	R/W	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
0	1	0	1	1	0	R6	Centering character	Character	R/W	—	—	—	CC4	CC3	CC2	CC1	CC0
0	1	0	1	1	1	R7	Border color control	—	R/W	—	—	—	BM	BCI	BCR	BCG	BCB
0	1	1	0	0	0	R8	Stretching control	Line	R/W	—	—	—	—	SF3	SF2	SF1	SF0
0	1	1	0	0	1	R9	Stretching index (high-order)	Line	R/W	SI15	SI14	SI13	SI12	SI11	SI10	SI9	SI8
0	1	1	0	1	0	R10	Stretching index (low-order)	Line	R/W	SI7	SI6	SI5	SI4	SI3	SI2	SI1	SI0
0	1	1	0	1	1	R11	Gradation level palette address	—	W	—	—	PS1	PS0	PA3	PA2	PA1	PA0
0	1	1	1	0	0	R12	Gradation level palette data	—	R/W	—	—	PD5	PD4	PD3	PD2	PD1	PD0
0	1	1	1	0	1	R13	Gradation display clock period (high-order)	Dot	R/W	—	—	—	—	—	—	—	GC8
0	1	1	1	1	0	R14	Gradation display clock period (low-order)	Dot	R/W	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0
0	1	1	1	1	1	R15	Reserved	—	—	—	—	—	—	—	—	—	—

Notes: 1. Bits marked with * cannot either read from or written to.
2. Bits marked with – are invalid and must be initialized to 0s; they cannot be read.

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System Description

Figure 1 shows an example of a VGA-compatible display system implemented with the CLINE. In this system, a color palette HD153119 (Hitachi), which is capable of digital output, is used with a VGA-compatible CRT controller. The CLINE receives digital color data and display sychronization signals from the color pallette and the CRT controller, respectively, and displays 4096-color images on a color LCD, or 16-level grayscale images on a monochrome LCD. With minor modification of the existing CRT display system, simultaneous LCD and CRT display is possible.

Addition of an external frame buffer memory (dual-port RAM) allows the LCD frame frequency to be increased above that of a CRT. This enables easy-to-see gradation display and the control of LCDs having a dual screen configuration.

CLINE operation may be controlled by internal registers through the 80-family MPU bus or an external ROM (as shown in the figure), or simply by pins.

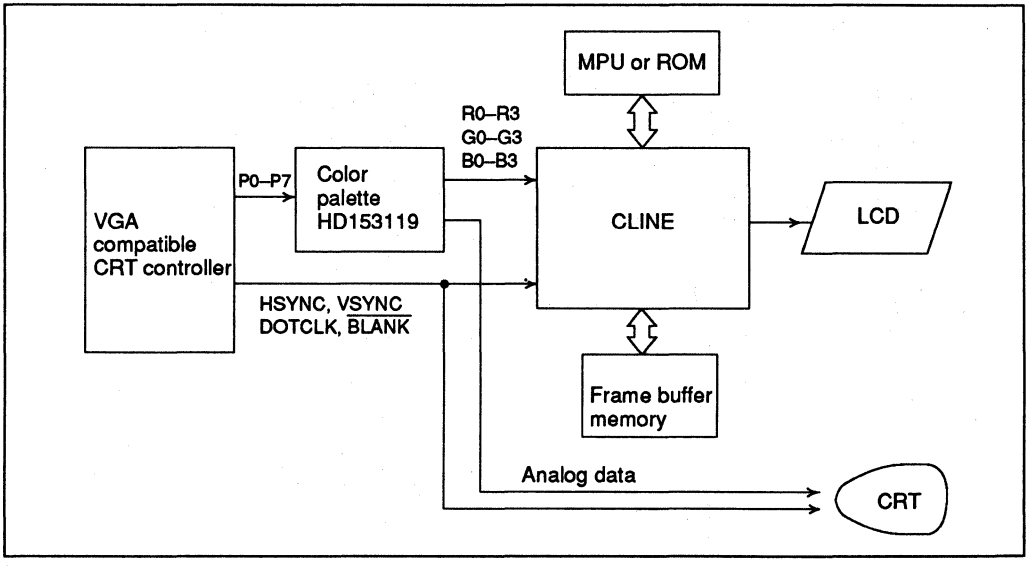

Figure 1 System Block Diagram

5

Functional Description

Programming Methods

To control CLINE functions, set the appropriate pins and/or internal registers according to the functions used. Controlling methods include pin and internal register programming methods. Internal register programming includes the MPU and ROM programming methods. Any of the three methods can be selected by the combined setting of pins PMODE0 and PMODE1 (table 2).

The pin programming method uses pins to control CLINE functions, and the internal register programming method uses data written to the internal registers to control the functions.

Figure 2 (a) shows a connection example of the CLINE and MPU buses for the MPU programming method. The CLINE bus, which is compatible with the 80-family microprocessor bus, can be directly connected to the host MPU bus.

Figure 2 (b) shows a connection example of the CLINE and ROM for the ROM programming method. In this case, data is automatically loaded into internal registers from the external ROM attached for this purpose. Note that with the ROM programming method, the reset signal must be applied before rewriting the internal registers or gradation level palettes.

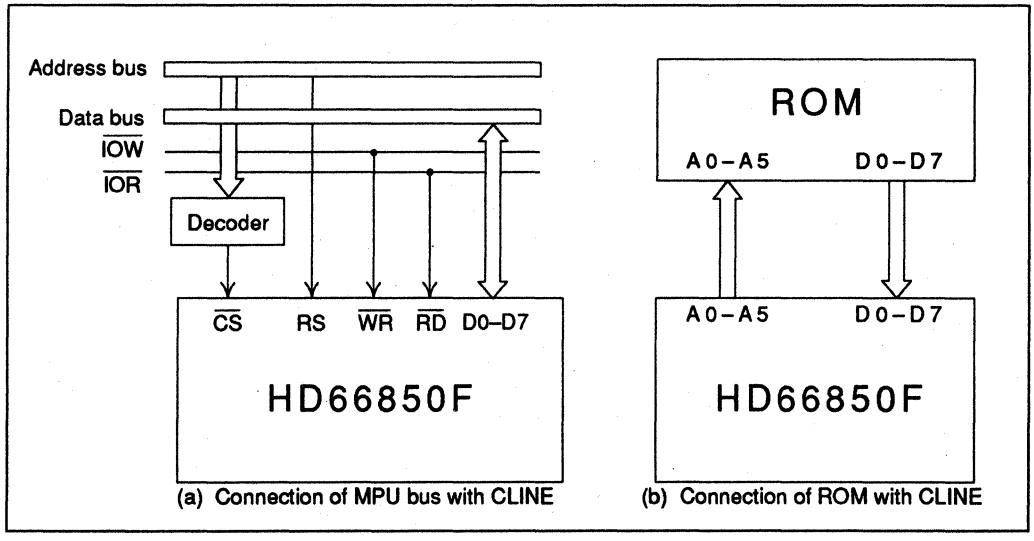

Figure 2 Connection of MPU Bus or ROM with CLINE

Automatic Adaptation to VGA Display Modes

VGA CRT display system display size varies depending on the display mode. (VGA display sizes are: 320, 360, 640, or 720 dots wide and 350, 400, or 480 lines high.) The CLINE identifies the current display mode from VSYNC and HSYNC signal polarities and the display period length, and changes the display size automatically (tables 5 and 6). This function is enabled by setting the VMODE pin low. The CLINE, based on this function, automatically sets the necessary registers (R0, R2, R3, R4, R5, R6, R8, R9, and/or R10) corresponding to the parameters of the display size, double-width display, gradation display clock, and stretching/centering display functions. (In MPU or ROM programming method, selection of vertical centering (bit 3 of R0) or stretching (bit 4 of R0) is not automatic.) Consequently, in VGA display modes, rewriting these registers is disabled.

Note that display stretching and centering are unavailable when buffer memory is not used in the system, even in VGA display modes. In these cases, a display of different vertical size would be placed in the upper section of the LCD panel, resulting in a blank area in the lower section. Centering the display in a system without memory requires external circuits or BIOS tuning.

When displaying an image 720 dots wide (9 dots × 80 characters) on an LCD panel 640 dots wide, the CLINE removes the ninth horizontal dot of each character to prevent losing the far-right portion of the image.

Table 5 Automatic Vertical Display Size Settings for VGA Display Modes

VSYNC	HSYNC	Display Size	Border Rasters	Displayed Rasters
Negative	Positive	350 lines	1-6	7-356
Positive	Negative	400 lines	1-7	8-407
Negative	Negative	480 lines	1-8	9-488

Table 6 Automatic Horizontal Display Size Settings for VGA Display Modes

BLANK Signal High Level

Pulse Width	Display Size	Border Dots	Displayed Dots
256-335 dots	320 dots (256-color)	1-5	6-325
336-359 dots	320 dots (16-color)	1-8	9-328
360-511 dots	360 dots	1-9	10-369
640-703 dots	640 dots	1-8	9-648
704-767 dots	720 dots	1-9	10-729

LCD Panel Size

LCD panel size is specified by either pins or internal registers.

For VGA modes, vertical panel size of 400 or 480 lines can be selected by the VSIZE pin and horizontal panel size of 640 or 720 lines by the HSIZE pin.

For non-VGA modes, the panel size is also specified by the VSIZE and HSIZE pins in pin programming method. In internal register programming method, vertical display size is specified by the vertical display size register (R3 and R4), within the range of 2 to 512 lines. Here, note that the vertical display size specified by R3 and R4 is the CRT display vertical size. When this size differs from the LCD panel vertical size, centering or stretching function must be used. Refer to the following equations for calculating the number of centering rasters and the stretching ratio. For the definition of the centering rasters, see figure 23, Centering Rasters,

- For centering

  LCD panel vertical size (line) =
  CRT display vertical size (line) + centering rasters (lines) × 2

- For stretching

  LCD panel vertical size (line) =
  CRT display vertical size (line) × stretching ratio

Since LCD panel horizontal size is limited to 640 or 720 dots even in internal register programming method, centering function must be used as well so that the total number of horizontal dots including the CRT display area and border areas become 640 or 720. Refer to the following equation to calculate the number of centering characters. For the definition of the border areas and centering characters, see figure 25, Centering Characters.

LCD panel horizontal size (dot) =
{number of horizontal display characters + (number of centering characters × 2)} × 8

Double-Width Display

Some CRT display systems have a low-resolution display mode of 320 horizontal dots in addition to a high-resolution display mode of 640 horizontal dots. In this case, the CRT display system lowers the dot clock frequency to reduce one line of data to 320 dots. If such data is supplied to the LCD system of 640 horizontal dots as-is, the entire display will be placed on the left section of the panel with the right half blank. To accommodate this situation, the CLINE doubles the width of the low-resolution display. This function is enabled by the SP/$\overline{WR}$/A4 pin in pin programming method or the SP bit (bit 1) of the control register (R0) in internal register programming method (table 7). In either method, for VGA display systems, the CLINE detects low-resolution display mode and automatically enables double-width display.

Table 7 Double-Width Display Usage

Programming Method	CRT System Mode	Setting
Pin: SP	VGA	Automatic
	Non-VGA	0: Normal display
		1: Double-width display
Internal register: Control register bit 1 (SP bit)	VGA	Automatic
	Non-VGA	0: Normal display
		1: Double-width display

Stretching and Centering Display

When the display size differs from the LCD panel size, data will be displayed on the upper-left section of the LCD panel with blank space to the right and/or below if no countermeasures are taken. To provide a user-friendly display, the CLINE can stretch a display to fill out the panel or center a display. Both stretching and centering functions are enabled by control register (R0) bits 2, 3, and 4.

Note that stretching and centering functions are available only in a system where buffer memory is used. This is because these functions are realized through adjustment of memory access. Similarly, stretching and centering functions are unavailable in non-VGA modes when the CLINE is controlled by the pin programming method. Simultaneous use of the vertical centering and stretching functions is also impossible.

In the internal register programming method, horizontal centering function is controlled by the centering character register (R6) within the range of 1 to 32 characters (8 to 256 dots), while vertical centering function is controlled by the centering raster register (R5) within the range of 1 to 256 lines.

Stretching function is controlled by the stretching control register (R8) and the stretching index register (R9 and R10) so as to double the vertical display size at most.

Figure 3 shows display examples using stretching/centering functions. In these examples, a display of 640 dots × 350 lines is displayed on an LCD panel of 720 dots × 400 lines, using stretching/centering functions.

For VGA modes, in both internal register programming and pin programming methods, necessary parameters are automatically calculated from the relationship between display size and the LCD panel size and set in the appropriate registers. Consequently, there is no need to account for display size.

However, the vertical centering or stretching function can be selected in the internal register programming method. (In pin programming method, the stretching function is automatically selected.) Table 8 describes the use of the stretching and centering function.

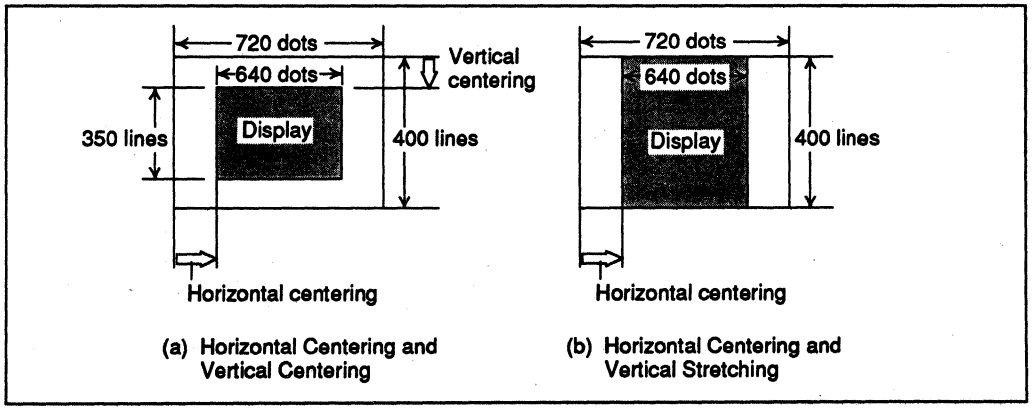

Figure 3 Display Examples Using Stretching/Centering Functions

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Table 8 Stretching and Centering Function Usage

Direction	Programming Method	CRT System Mode	Display Arranging Function	Setting
Vertical	Pin	VGA	Stretching	Automatic
		Non-VGA	None	— *1
	Internal register	VGA	Stretching or centering	Automatic *2
		Non-VGA	Stretching or centering	Necessary
Horizontal	Pin	VGA	Centering	Automatic
		Non-VGA	None	— *1
	Internal register	VGA	Centering	Automatic
		Non-VGA	Centering	Necessary

Notes: 1. Display size must be LCD panel size.
2. Either stretching or centering function must be selected by the internal register.

Display Modes

Display Mode Settings and LCD Module Configurations: The CLINE supports 20 display modes, depending on the settings of the LMODE4 to LMODE0 pins. The display mode includes display color mode (color or monochrome), screen configuration (single or dual), gradation display method, and width of data transfer to LCD drivers. Table 9 lists the display modes and figures 4 (a) to 4 (g) show the corresponding LCD module configurations.

Table 9 Display Modes and LCD Module Configurations

Mode No.	Pin: LMODE 4	3	2	1	0	Display Color Mode (Gradation Display Method)	Screen Config.	Data Width	LCD Module Config.
1	0	0	0	0	0	Monochrome: black and white	Single	4	Fig. 4 (a)
2	0	0	0	0	1		Dual	4	Fig. 4 (b)
3	0	0	0	1	0		Single	8	Fig. 4 (c)
4	0	0	0	1	1		Dual	8	Fig. 4 (d)
5	0	0	1	0	0	Monochrome: 16 gray levels (Frame-based data thinning)	Single	4	Fig. 4 (a)
6	0	0	1	0	1		Dual	4	Fig. 4 (b)
7	0	0	1	1	0		Single	8	Fig. 4 (c)
8	0	0	1	1	1		Dual	8	Fig. 4 (d)
9	0	1	0	0	0	Monochrome: 16 gray levels (1/2 pulse width modulation)	Single	4	Fig. 4 (a)
10	0	1	0	0	1		Dual	4	Fig. 4 (b)
11	0	1	0	1	0		Singale	8	Fig. 4 (c)
12	0	1	0	1	1		Dual	8	Fig. 4 (d)
13	1	0	0	0	0	16 colors	Single	2	Fig. 4 (e)
14	1	0	0	1	0		Single	4	Fig. 4 (f)
15	1	0	0	1	1	8 colors	Single	8	Fig. 4 (g)
16	1	0	1	0	0	4096 color levels (Frame-based data thinning)	Single	2	Fig. 4 (e)
17	1	0	1	1	0		Single	4	Fig. 4 (f)
18	1	0	1	1	1		Single	8	Fig. 4 (g)
19	1	1	0	1	0	4096 color levels (1/2 pulse width modulation)	Sing;le	4	Fig. 4 (f)
20	1	1	0	1	1		Single	8	Fig. 4 (g)

Note: Modes 15, 18, and 20 are interleaving structure modes.

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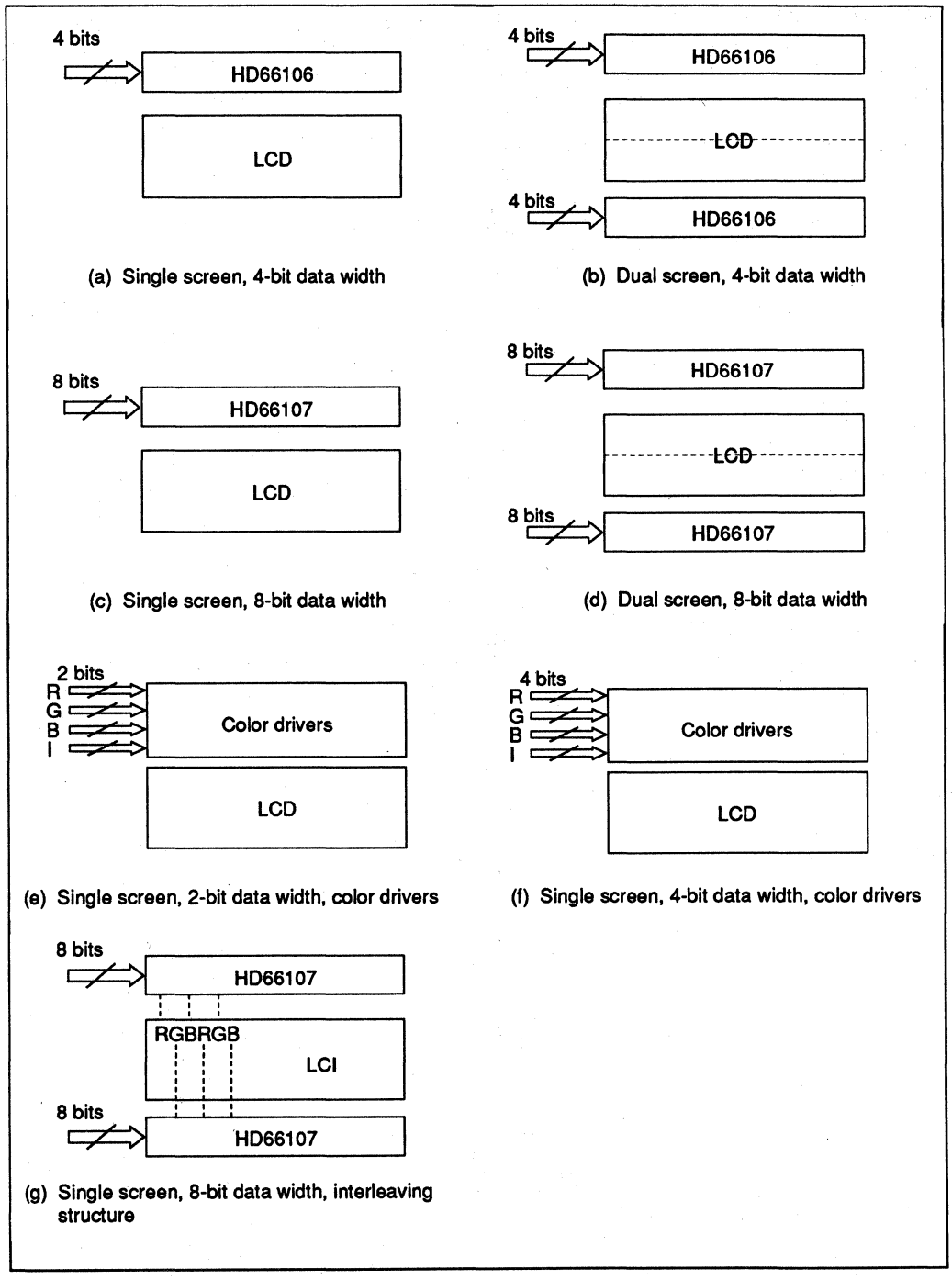

Figure 4 LCD Module Configurations by Display Modes

Gradation Level Reduction: Although a CRT display system can represent information for over 100,000 color levels, an LCD cannot handle so much information.

Consequently, CRT color or gradation level information must be reduced in order for the CLINE to display it. Reduction methods vary depending on the input color or gradation level information, the LCD panel (color or monochrome), and other factors. Table 10 lists gradation level reduction for CLINE modes, where "Input Bits" indicates CRT display color data and "Reduced Data" indicates input to the gradation level palettes.

Input Display Data Connection: Input display data connection and pin settings depend on the CRT input mode (color or gradation level information) and the LCD panel used.

- When monochrome LCD panel is used (LMODE4 = 0)

  — 64-color input and 16-level grayscale output (modes 5-12)

  The B0 pin must be set to 1, and the B1 pin to 0. Unused display data input pins must be fixed to 0. See figure 5 (a).

  — 16-level grayscale input and 16-level grayscale output (modes 5-12)

  Both B0 and B1 pins must be set to 0. Unused display data input pins must be fixed to 0. See figure 5 (b).

- When color LCD panel is used (LMODE4 = 1)

  — 64-color input and 16- or 8-color output (modes13-15)

  Two-bit R, G, and B data must be input to the R2-R3, G2-G3, and B2-B3 pins, respectively. Unused display data input pins must be fixed to 0). See figure 6 (a).

  — 4096-color input and 4096-color output (modes 16-20)

  Four-bit R, G, and B data must be input to the R0-R3, G0-G3, and B0-B3 pins, respectively. If the input has more than 4096 colors, use the high-order four bits of each color. See figure 6 (b).

Table 10 Gradation Level Reduction for CLINE Display Modes

Input Mode	Input Bits R	G	B	CLINE Display Mode	Reduced Data 3	2	1	0	LCD Panel	Gradation Level Reduction (Bits)
4096 colors	4	4	4	4096 color levels	D3	D2	D1	D0	Color	12 → 12
64 colors	2	2	2	16 colors	R	G	B	I	Color	6 → 4
64 colors	2	2	2	16 gray levels	D3	D2	D1	D0	Monochrome	6 → 4
16 gray levels	—	4	—	16 gray levels	D3	D2	D1	D0	Monochrome	4 → 4
16 gray levels	—	4	—	Monochrome (black & white)	All 0s or all 1s				Monochrome	4 → 1

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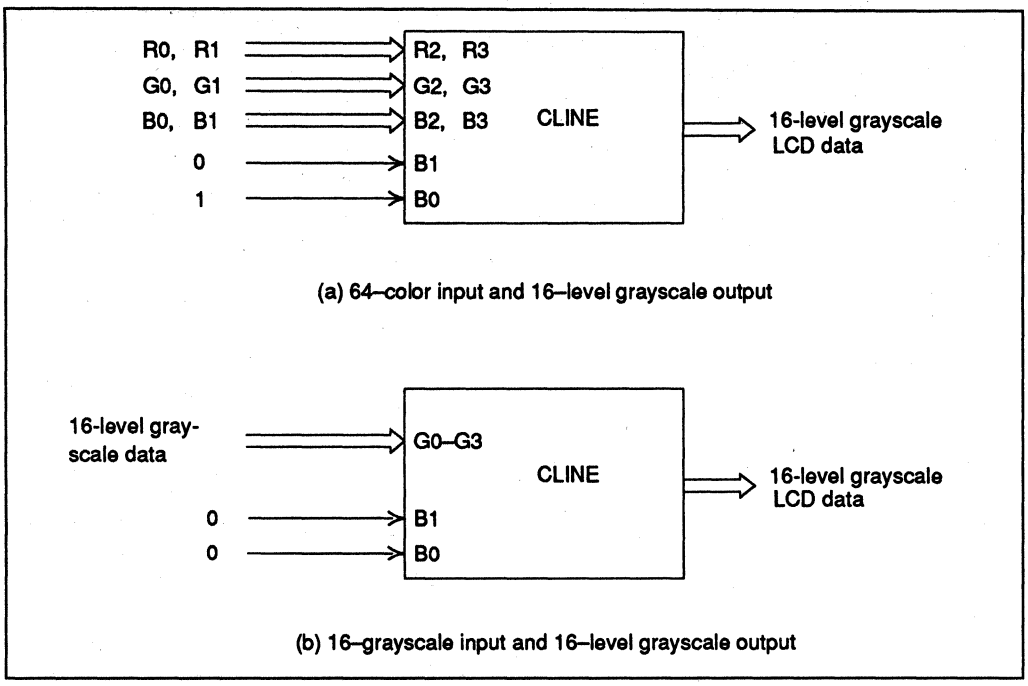

Figure 5 Input Display Data Connection and Pin Settings when a Monochrome LCD Panel is Used

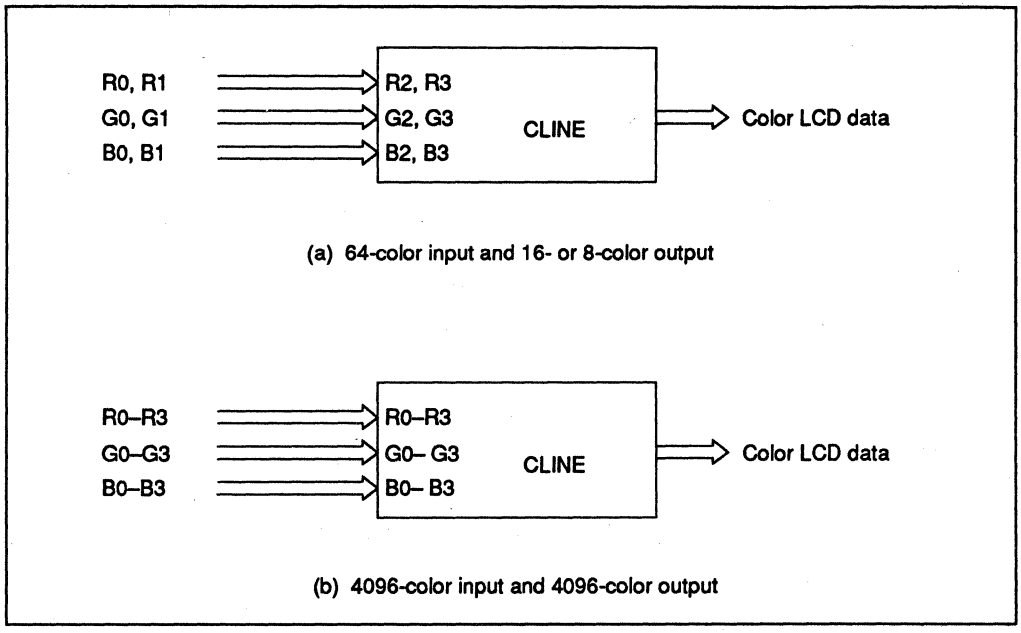

Figure 6 Input Display Data Connection and Pin Settings when a Color LCD Panel is Used

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LCD Data Output: The CLINE uses pins UD7–UD0 and LD7–LD0 for display data output. Output data from these pins depend on the display mode, as shown in table 11. However, data output timings are basically the same in all display modes. Display data output timing for modes 15 and 18 (8-bit color data transfer, bidirectional connection, without pulse width modulation) is shown in figure 7. Display data output timing for the LCD display modes with pulse width modulation is slightly different. This type of example is shown in figure 8. Figure 8 shows the display data output timing in mode 10 (1/2 pulse width modulation, 4-bit monochrome data transfer, and dual screen configuration).

However, LCD lower panel data LD3–LD0 are not shown in the figure.

Table 11 LCD Data Output Pins and Display Data by Display Modes

	Monochrome Modes				Color Modes				
Pin	4-Bit/ Single Screen	4-Bit/ Dual Screen	8-Bit/ Single Screen	8-Bit/ Dual Screen	2-Bit	4-Bit	8-Bit		
UD7	—	—	D7	UD7	—	R3	R15	G10	B5
UD6	—	—	D6	UD6	—	R2	B15	R9	G4
UD5	—	—	D5	UD5	R1	R1	G14	B9	R3
UD4	—	—	D4	UD4	R0	R0	R13	G8	B3
UD3	D3	UD3	D3	UD3	—	G3	B13	R7	G2
UD2	D2	UD2	D2	UD2	—	G2	G12	B7	R1
UD1	D1	UD1	D1	UD1	G1	G1	R11	G6	B1
UD0	D0	UD0	D0	UD0	G0	G0	B11	R5	G0
LD7	—	—	—	LD7	—	B3	G15	B10	R4
LD6	—	—	—	LD6	—	B2	R14	G9	B4
LD5	—	—	—	LD5	B1	B1	B14	R8	G3
LD4	—	—	—	LD4	B0	B0	G13	B8	R2
LD3	—	LD3	—	LD3	—	(I3)	R12	G7	B2
LD2	—	LD2	—	LD2	—	(I2)	B12	R6	G1
LD1	—	LD1	—	LD1	(I1)	(I1)	G11	B6	R0
LD0	—	LD0	—	LD0	(I0)	(I0)	R10	G5	B0

Notes:
1. The left bit corresponds to MSB.
2. U and L indicate upper panel and lower panel data, respectively.
3. Data in parentheses are for 16-color display.
4. — indicates that the corresponding pins are not used; must be left disconnected.

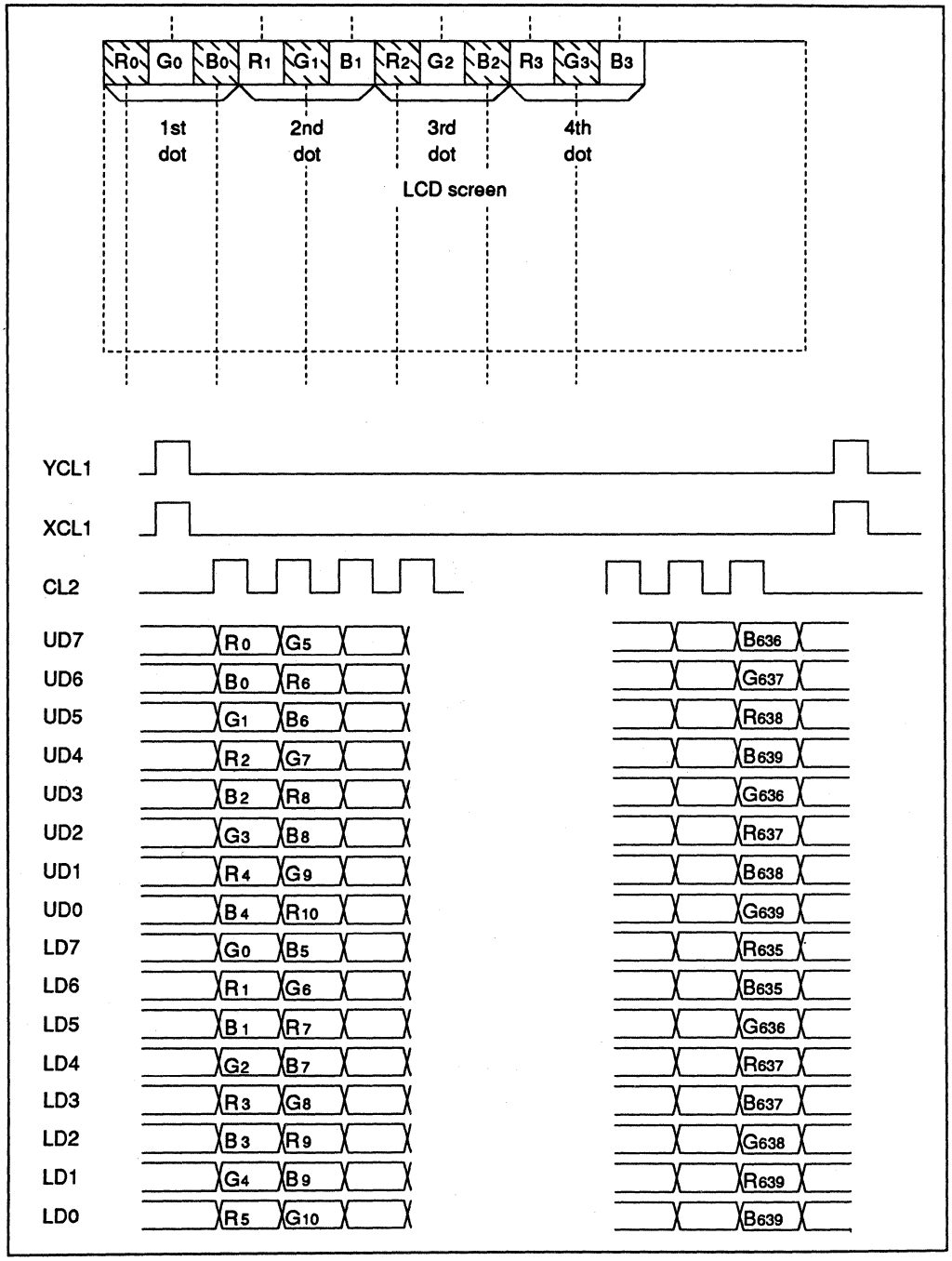

Figure 7 Display Data Output Timing in Display Modes Without Pulse Width Modulation (Modes 15 and 18)

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In figure 8, data P0–0, P4–0, ... P636–0 make up the first set of data for one line to be output to LCD drivers via pin UD3. Likewise, data P0–1, P4–1, ... P636–1 make up the second set of data. The combination of the first and second sets of data determines the display status as follows: (first data, second data) = (0, 0): display off; (1, 0): 1/2 pulse width modulation; and (1, 1): display on. For more details, refer to the Gradation Display Methods section.

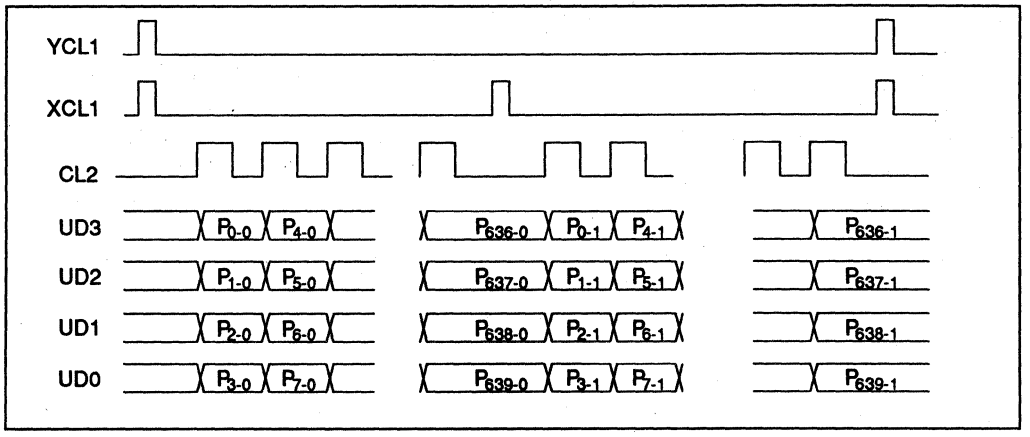

Figure 8 Display Data Output Timing in Display Modes with Pulse Width Modulation (Mode 10)

Gradation Display Methods

The CLINE supports the frame-based data thinning method and pulse width modulation method for gradation display.

Frame-Based Data Thinning Method: In the frame-based data thinning method, the CLINE thins out the display data in line or dot units in the specified frames.

Pulse Width Modulation Method: In the pulse width modulation method, the CLINE combines 1/2 pulse width modulation and frame-based data thinning. In this case, data is output from X-drivers twice in one line-selection period (figure 9). Consequently, the X-driver latch clock must be different from the Y-driver shift clock, and a conventional LCD module configuration cannot be used. Therefore, clock XCL1 must be supplied to X-drivers and clock YCL1 to Y-drivers (figure 10).

The XCL1 period is specified by the gradation display clock period register (R13 and R14) when no buffer memory is used in non-VGA modes and in the internal register programming method. (Pulse width modulation is unavailable when buffer memory is not used in non-VGA modes, pin programming method.) In the other cases, the register is automatically set, since the YCL1 period is fixed (table 12).

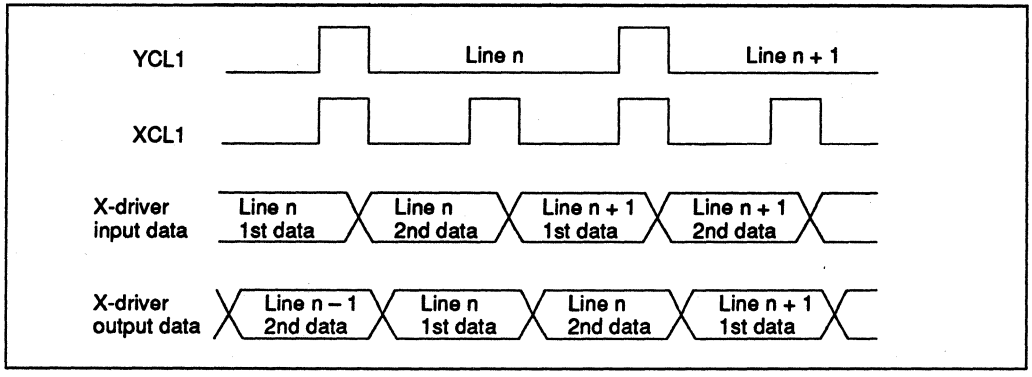

Figure 9 Driver Clock and Display Data Timing for Gradation Display with 1/2 Pulse Width Modulation

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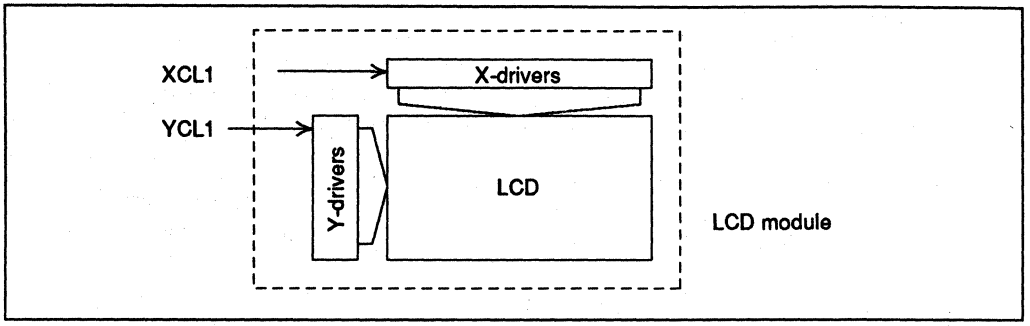

Figure 10 X- and Y-Driver Clock Connection for Pulse Width Modulation Method

Table 12 XCL1 Period Setting

Memory Mode		XCL Period	Setting
With-memory		Half of YCL1 period for 1/2 pulse with modulation method	Automatic
Without-memory	VGA	Half of YCL1 period for 1/2 pulse width modulation method	Automatic (See note below)
	Non-VGA Internal register programming	Conforms to gradation display clock register (R13, R14) settings	Required (R13, R14)
	Pin programming	—	

Note: Total number of horizontal dots must be 400, 450, 800, or 900 for displaying 320, 360, 640, or 720 dots, respectively.

Gradation Level Palettes

Gradation display quality depends greatly on LCD panel characteristics.
Consequently, uniform gradation display may be impossible for some panels. To accommodate this situation, the CLINE incorporates a set of gradation level palettes that can assign any gradation level to any CRT display color as desired.
16 levels are available for gradation display using the frame-based data thinning method and 31 levels using 1/2 pulse width modulation method. Appropriate levels can be selected for the LCD panel used.

The R-, G-, and B-palettes are used for color level display modes, while only the R-palette is used for 16-level grayscale display modes.

In pin programming and MPU programming methods, these palettes are automatically loaded after reset with appropriate data for frame-based data thinning modes and 1/2 pulse width modulation modes. The automatically set data cannot be rewritten in the pin programming method, but can be rewritten, any time after 100 µs have elapsed after reset, in MPU programming method.

By contrast, in the ROM programming method, these palettes are not automatically set. Thus writing the necessary data to the palettes is always required.

Table 13 shows the relationship between the values set in the palettes (through R12) and gradation levels. Values other than those shown here disable correct display.

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Table 13 Relationship between Gradation Levels and Palette (R12) Values

(a) Frame-based data thinning modes

Gradation Level No.	Palette Data (R12 Data Bits) 5	4	3	2	1	0	Gradation Level
0	1	0	0	0	0	0	0.00
1	1	0	0	0	0	1	0.14
2	1	0	0	0	1	0	0.20
3	1	0	0	0	1	1	0.29
4	1	0	0	1	0	0	0.33
5	1	0	0	1	0	1	0.40
6	1	0	0	1	1	0	0.43
7	1	0	0	1	1	1	0.50
8	1	0	1	0	0	0	0.57
9	1	0	1	0	0	1	0.60
10	1	0	1	0	1	0	0.66
11	1	0	1	0	1	1	0.71
12	1	0	1	1	0	0	0.75
13	1	0	1	1	0	1	0.80
14	1	0	1	1	1	0	0.86
15	1	0	1	1	1	1	1.00

(b) 1/2 pulse width modulation modes

Gradation Level No.	Palette Data (R12 Data Bits) 5	4	3	2	1	0	Gradation Level
0	0	1	0	0	0	0	0.00
1	0	1	0	0	0	1	0.07
2	0	1	0	0	1	0	0.10
3	0	1	0	0	1	1	0.14
4	0	1	0	1	0	0	0.17
5	0	1	0	1	0	1	0.20
6	0	1	0	1	1	0	0.21
7	0	1	0	1	1	1	0.25
8	0	1	1	0	0	0	0.29
9	0	1	1	0	0	1	0.30
10	0	1	1	0	1	0	0.33
11	0	1	1	0	1	1	0.36
12	0	1	1	1	0	0	0.38
13	0	1	1	1	0	1	0.40
14	0	1	1	1	1	0	0.43
15	0	1	1	1	1	1	0.50
16	1	1	0	0	0	0	0.50
17	1	1	0	0	0	1	0.57
18	1	1	0	0	1	0	0.60
19	1	1	0	0	1	1	0.64
20	1	1	0	1	0	0	0.67
21	1	1	0	1	0	1	0.70
22	1	1	0	1	1	0	0.71
23	1	1	0	1	1	1	0.75
24	1	1	1	0	0	0	0.79
25	1	1	1	0	0	1	0.80
26	1	1	1	0	1	0	0.83
27	1	1	1	0	1	1	0.86
28	1	1	1	1	0	0	0.88
29	1	1	1	1	0	1	0.90
30	1	1	1	1	1	0	0.93
31	1	1	1	1	1	1	1.00

Display On/Off Control

When the LCD drivers used have an LCD on/off control pin, display can be controlled with the CLINE DISPON signal. When the LCD drivers used do not have an LCD on/off control pin, the CLINE can turn off display by transferring all-0 display data to the drivers.

Display will be turned on with the DISPON pin = 1, turns the display off while DISPON = 0. The DISPON pin is equivalent to the DISPON bit (bit 0) of the control register.

In the pin programming method, display is on except for four frames after reset. The four frame display-off time period prevents random display at power-on. In the MPU programming method, display is turned off at reset, but can be freely turned on or off after four frames after reset by rewriting the corresponding register bit. In the ROM programming method, a 1 must be written to the DISPON bit to turn on display. Like in other programming methods, display is off for four frames after reset.

LDOTCK Frequency and Data Transfer Rate

The LDOTCK frequency (f_{LDOTCK}) for asynchronous mode is calculated from the following equation:

$$f_{LDOTCK} = (Nhd + 48) \times Nvd \times f_F$$

Nhd: Number of dots contained in one horizontal line of the LCD panel
Nvd: Number of horizontal lines from the LCD panel top to bottom
f_F: Frame frequency

In this case, the following relationship must hold true:

$$1/2 \times f_{DOTCLK} < f_{LDOTCK} < 2 \times f_{DOTCLK}$$

f_{DOTCLK}: Dot clock frequency

The data transfer rate to LCD drivers depends on the mode in which the CLINE is used. Specifically, the rate depends on screen configuration (single or dual), data transfer width (bit count), and gradation display methods. For example, the data transfer rate will be doubled for 1/2 pulse width gradation display. This is because data must be transferred two times during one line-selection period. The data transfer rate (f_{CL2}: CL2 frequency) is calculated from the following equation ($f_{LDOTCK} = f_{DOTCLK}$ for synchronous mode):

$$f_{CL2} = \frac{f_{LDOTCK} \times 1}{n \times m}$$

n: Number of panels composing one screen
— 1 for modes 1, 3, 5, 7, 9, 11, 13-20
— 2 for modes 2, 4, 6, 8, 10, 12
m: Number of bits transferred at one time
— 2 for modes 13, 16
— 4 for modes 1, 2, 5, 6, 9, 10, 14, 15, 17-20
— 8 for modes 3, 4, 7, 8, 11, 12
l: Constant for each gradation display
— 1 for modes 1-8, 13-18
— 2 for modes 9-12, 19, 20

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Synchronous/Asynchronous Modes and Memory

The CLINE has two timing modes: asynchronous and synchronous.

In asynchronous mode, dot clock pulses for the CRT system (DOTCLK) are different from those for the LCD system (LDOTCK) in frequency to accommodate frame frequency conversion. This requires buffer memory as shown in figure 11 (a). In this mode, dual screen LCD panels can be used.

In synchronous mode, dot clock pulses for the CRT system are identical to those for the LCD system, thus requiring no buffer memory in principle (synchronous without-memory mode (figure 11 (b)). However, synchronous without-memory mode cannot support dual screen LCD panels.

The CLINE has another mode in which dual screen LCD panels can be used and fewer memory devices are required. This is called "synchronous with-memory mode" (figure 11 (c)). In this mode, the number of memory devices can be reduced to a half or a third that of asynchronous mode. This is because RGB data sent from the CRT system is processed for gradation display before being written into buffer memory. (In asynchronous mode, on the other hand, R, G, and B data sent from the CRT system is separately written into the R-plane, G-plane, and B-plane memories, respectively.)

Table 14 summarizes these modes.

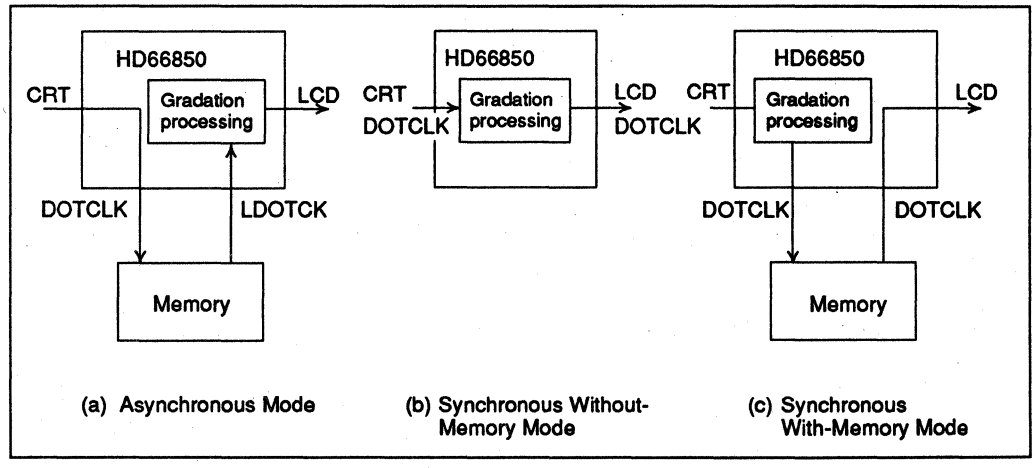

Figure 11 Signal Flow for Synchronous/Asynchronous With-/Without-Memory Modes

The CLINE uses dual port RAMs for buffer memory, enabling high-speed display and independent use of an LCD dot clock and a CRT dot clock.

The CIINE supports three types of memory configurations: 64k × 4 bits (256 k), 256 k × 4 bits (1 M), and 128 k × 8 bits (1 M), any of which can be selected with the MMODE0 and MMODE1 pins (table 3).

The number of memory devices required depends on the LCD panel size and the display mode. However, it depends only on LCD panel vertical size and not on horizontal size since the CLINE uses memory as shown in figure 12. For example, one 256-kbit memory device is required for the panel having 256 or less lines and two for that having 257 to 512 lines. Table 15 lists the number of memory devices required for each mode.

Table 14 Memory Mode Summary

	Asynchronous With-Memory Mode	Synchronous With-Memory Mode	Synchronous Without Memory Mode
Centering/stretching	Possible	Possible	Impossible
Max number of gray levels	16	16	16
Max number of color levels	16	4096 (frame-based data thinning)	4096 (pulse width modulation)
Dual screen	Possible	Possible	Impossible
Max number of display lines	512	512	1024
Frame frequency conversion	Possible	Impossible	Impossible

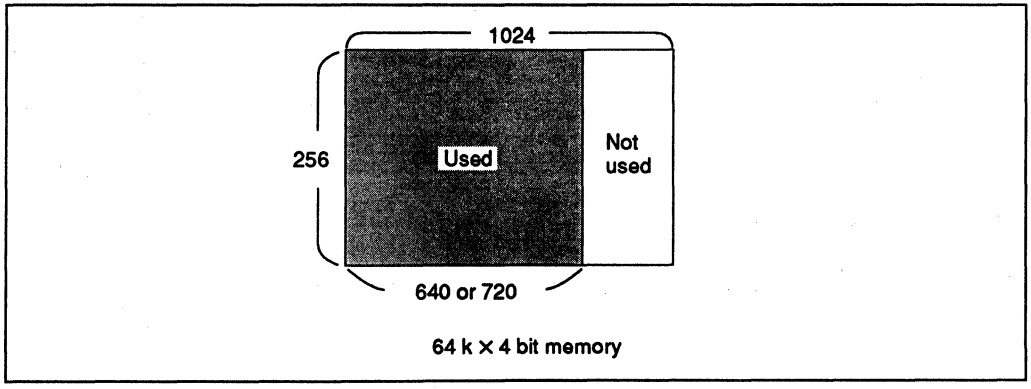

Figure 12 Display Sizes and Memory Area Used

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Table 15 Number of Memory Devices for Different Display modes

	Number of Memory Devices Required					
	Asynchronous			Synchronous		
Display Mode	**64 k × 4**	**256 k × 4**	**128 k × 8**	**64 k × 4**	**256 k × 4**	**128 k × 8**
Monochrome Modes 1–4	2	1	1	2	1	1
16-level grayscale (frame-based) Modes 5–8	8	4	2	2	1	1
16-level grayscale (1/2 pulse width) Modes 9–12	8	4	2	4	2	1
8-color Mode 15	6	3	2	6	3	2
16-color Modes 13, 14	8	4	2	8	4	2
4096-color-scale (frame-based) Modes 16–18	—	—	—	6	3	2

Frame-based: Frame-based data thinning method
1/2 pulse width: 1/2 pulse width modulation method
Note: With-memory mode does not support color level display using the pulse width modulation method.

Display Timing Signal Fine Adjustment

When the display timing signal is supplied externally, a phase shift may appear between CRT data and the display timing signal, since each signal has its own peculiar lag. The CLINE can adjust the display timing signal with pins AJ3–AJ0 (in pin programming method) or with the input timing control register (R1) (in internal register programming method) to compensate the phase shift (table 1).

Figure 13 (a) shows an example of adjusting a display timing signal that is two dots ahead of the display start position. In this case, pins (AJ3, AJ2, AJ1, AJ0) or data bits (3, 2, 1, 0) of R1 must be set to (1, 0, 1, 0) to delay the signal for two dots. Conversely, they must be set to (0, 0, 1, 0) to advance the signal for two dots for the case of figure 13 (b), where the display timing signal is two dots behind.

When there is no need to adjust the signal, a setting of either (0, 0, 0, 0) or (1, 0, 0, 0) will work.

It should be noted that the VGA CRT system applies the BLANK signal, which includes the border area period, as the display timing signal, and that the CLINE removes the border area period. Consequently, the border area period must be considered for adjusting the display timing signal.

5

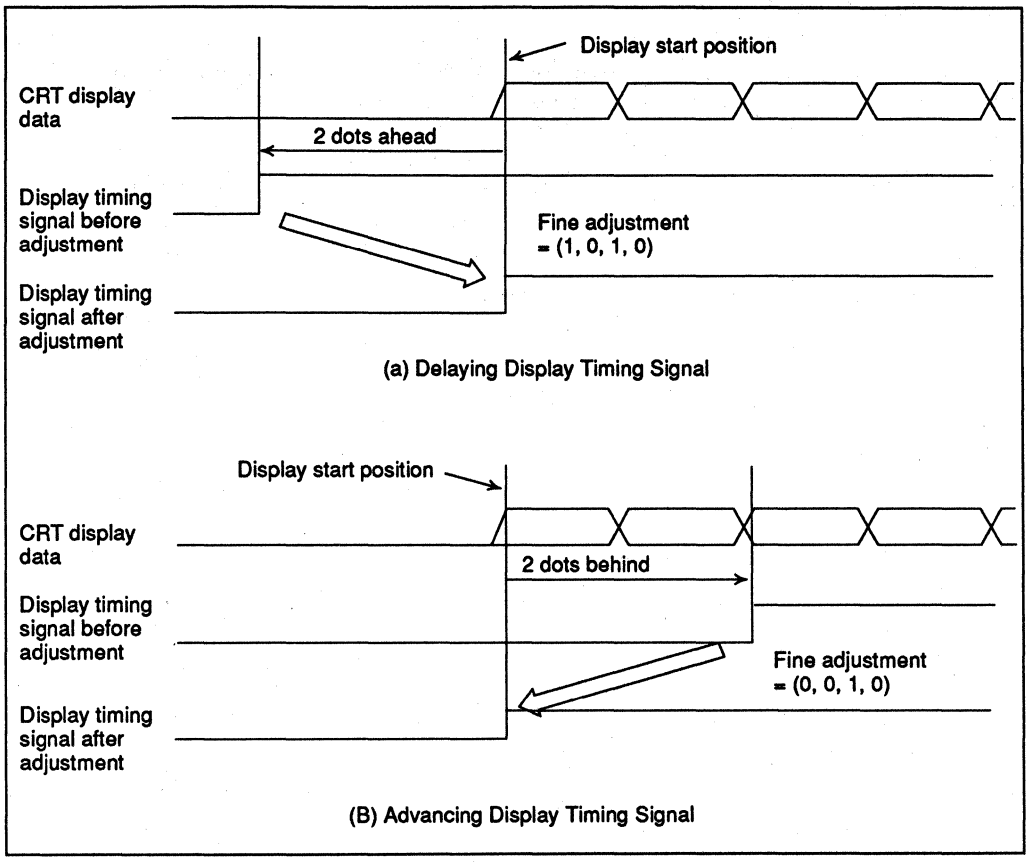

Figure 13 Display Timing Signal Fine Adjustment

Border Color Control

In the internal register programming method, the CLINE can specify the color of a blank area that is left on a centered display (figure 14). Any of 16 colors or the color of the dot immediately before the valid display data can be specified by the border color control register (R7). However, the desired color can be specified only in asynchronous mode.

In the pin programming method, the specified color is always the same color as the dot immediately before the valid display data.

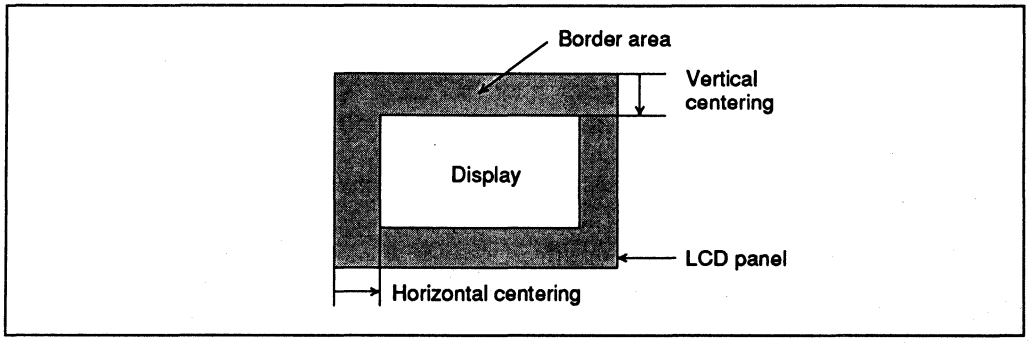

Figure 14 Border Area and an LCD Panel

5

Internal Registers

The CLINE has one index register (IR) and 15 data registers (R0–R14). In the MPU programming method, the desired register address must be written in one cycle into the index register before writing or reading data to/from the register in the following cycle. By contrast, in the ROM programming method, the index register is not used; the CLINE automatically reads data from the ROM, in which data has been written to the ROM addresses corresponding to the desired data registers, and writes it to the data register.

Registers are valid only for the internal register programming method and are invalid (don't care) for the pin programming method. Since all data registers are reset to 0s, they must be rewritten after reset.

Register Access for MPU Programming Method

First write the desired data register address into the index register with $\overline{CS}$ = 0, RS = 0, and $\overline{WR}$ = 0, then write/read data to/from the register with $\overline{CS}$ = 0, RS = 1, and $\overline{WR}$ = 0 or $\overline{RD}$ = 0. Figure 15 shows the timing for writing data into an internal register.

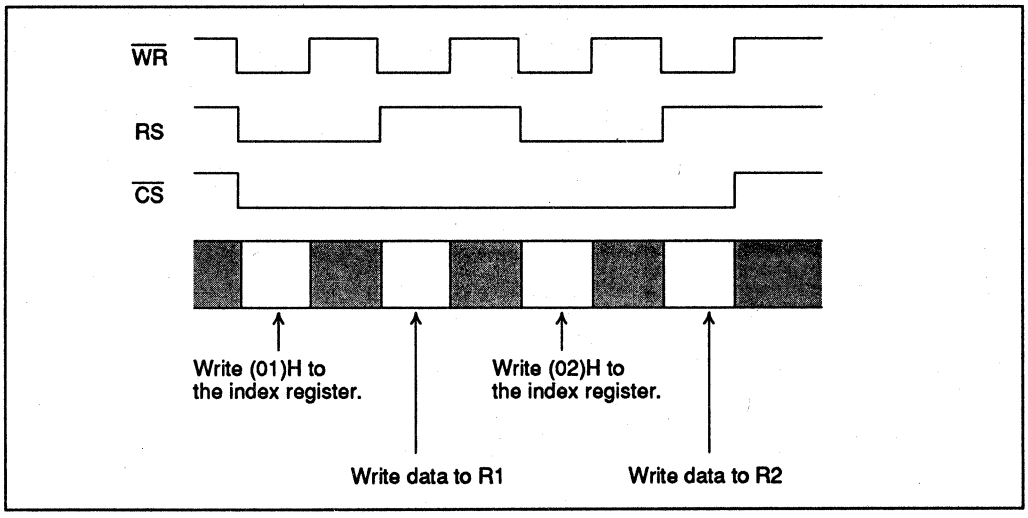

Figure 15 Internal Register Write by MPU

ROM Data Setting for ROM Programming Method

The desired data must have been previously written to the ROM addresses corresponding to the data register addresses; that is, to ROM addresses $0000–$000F. Data for the gradation level palettes must have been written to ROM addresses $0010–$003F. Consequently, data written for internal registers R11 and R12 are invalid. Figure 16 shows the ROM address map.

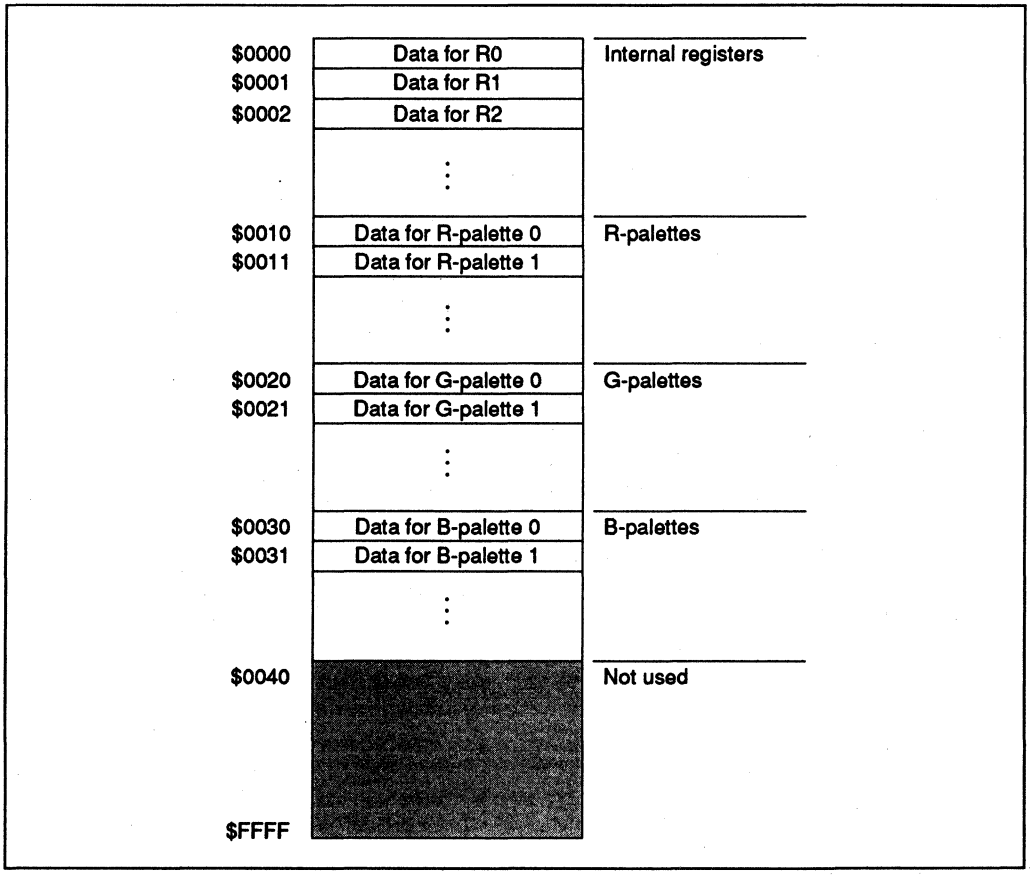

Figure 16 ROM Address Map

5

Register Function

Index Register (IR): The index register (figure 17), composed of four valid bits, selects one of the 15 data registers. The index register itself is selected by the MPU while the RS signal is low and selects a data register with the register address written.

Control Register (R0): The control register (figure 18) is composed of five valid bits, each with a particular function.

- STE bit
  - — STE = 1: Stretching function enabled
  - — STE = 0: Stretching function disabled

- CRE bit
  - — CRE = 1: Vertical centering function enabled
  - — CRE = 0: Vertical centering function disabled

Simultaneous use of stretching and vertical centering functions is impossible; if both the CRE and STE bits are set to 1 at the same time, correct display will be disabled.

- CCE bit
  - — CCE = 1: Horizontal centering function enabled
  - — CCE = 0: Horizontal entering function disabled

- SP bit
  - — SP = 1: Double-width display
  - — SP = 0: Normal display

- DISPON bit
  - — DISPON = 1: Display on
  - — DISPON = 0: Display off

DISPON is always cleared at reset. In the MPU programming method, rewriting this bit can always be rewritten. However, display will be off for four frames after reset, regardless of the status of this bit.

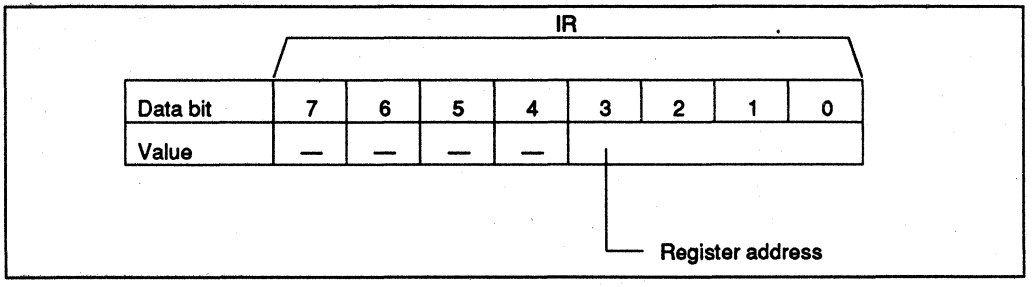

Figure 17 Index Register

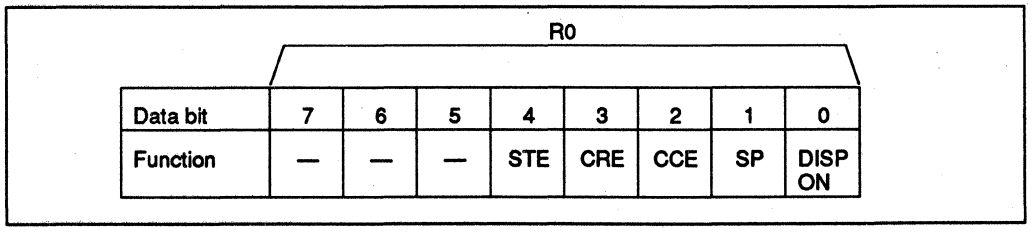

Figure 18 Control Register

Input Timing Control Register: The input timing control register (figure 19) has five valid bits, having two different functions.

- DOTE bit : Switches RGB data latch timing.
  - — DOTE = 1: Latches data at the rising edge of the dot clock pulses
  - — DOTE = 0: Latches data at the falling edge of the dot clock pulses
- AJ3-AJ0 bits: Adjust the externally supplied display timing signal to synchronize its phase with that of LCD data. Write the shift, represented in dots, between the display timing signal and the display start position to these bits. The absolute value of the number of dots to be shifted must be written to the AJ2-AJ0 bits and shift polarity to the AJ3 bit. If there is no need to adjust the display timing signal, these bits may be set to either (1, 0, 0, 0) or (0, 0, 0, 0).

R1

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	DOTE	AJ3	AJ2	AJ1	AJ0

3	2	1	0	Number of Dots Adjusted
0	0	0	0	0
	0	0	1	–1
	0	1	0	–2
1	0	0	0	0
	0	0	1	+1
	0	1	0	+2
	0	1	1	+3
	1	0	0	+4
	1	0	1	+5
	1	1	0	+6

Note: – (minus) and + (plus) in the Number of Dots Adjusted column indicate advancing and delaying the display timing signal, respectively.

Figure 19 Input Timing Control Register

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Horizontal Display Size Register: The horizontal display size register (figure 20), composed of seven valid bits, specifies the horizontal display size in units of characters (eight dots). The value to write to this register is "number of characters displayed on one horizontal line – 1." A maximum of 90 characters (720 dots) can be specified.
This register is set automatically in VGA mode.

Vertical Display Size Register: The vertical display size register (figure 21), composed of nine valid bits, specifies the vertical display size in units of lines. The value to write to this register is "number of lines displayed from display screen top to bottom – 1." A maximum of 512 lines can be specified.
This register is set automatically in VGA mode.

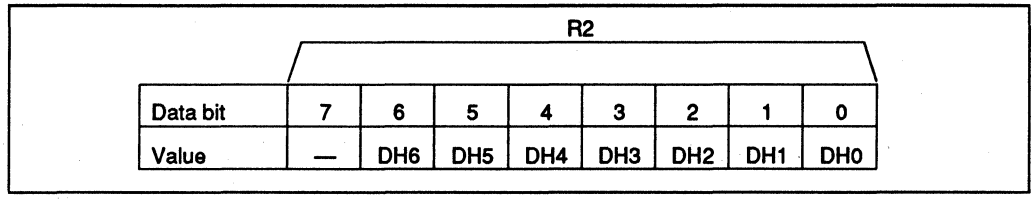

Figure 20 Horizontal Display Size Register

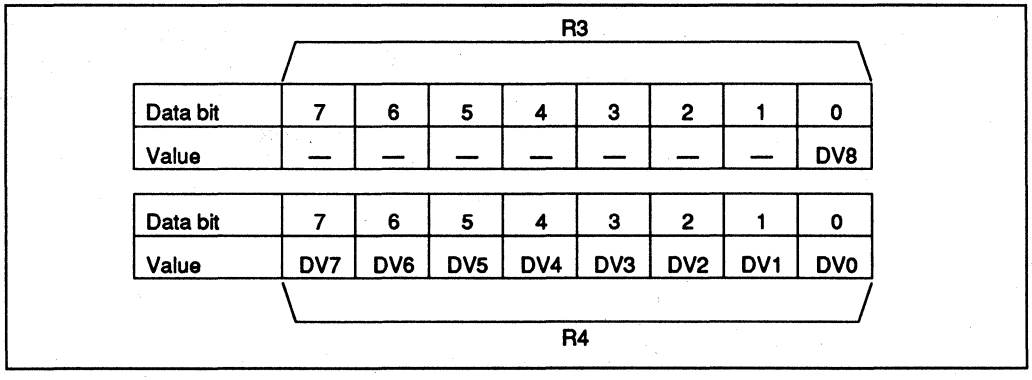

Figure 21 Vertical Display Size Register

Centering Raster Register: The centering raster register (figure 22), composed of eight bits, specifies the number of rasters for vertically centering the display within the range of 1 to 256. The value to write to this register is "number of rasters for centering – 1." As shown in figure 23, the number here indicates the number of rasters in either the upper border area or lower border area, not the total number. Since the LCD panel size is determined by this number and the display size, the number of rasters must be correctly written if the display size differs from the LCD panel size. Incorrect setting disables correct display. This register is enabled the control register's CRE bit is 1. This register is set automatically in VGA mode.

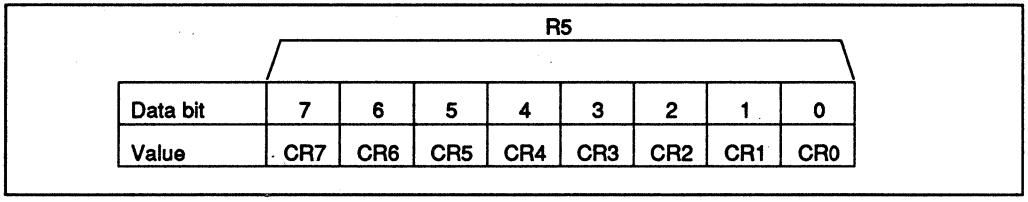

Figure 22 Centering Raster Register

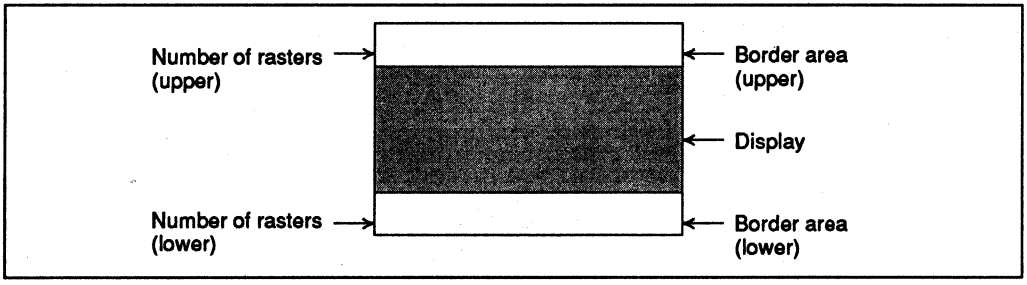

Figure 23 Centering Rasters

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Centering Character Register: The centering character register (figure 24), composed of five valid bits, specifies the number of characters for horizontally centering the display within the range of 1 to 32. The value to write to this register is "number of characters for centering – 1." As shown in figure 25, the number here indicates the number of characters in either the left border area or right border area, not the total number. Since the LCD panel size is determined by this number and the display size, the number of characters must be correctly written when the display size differs from the LCD panel size. Incorrect setting disables correct display. This register is enabled when the control register's CCE bit is 1.
This register is set automatically in VGA mode.

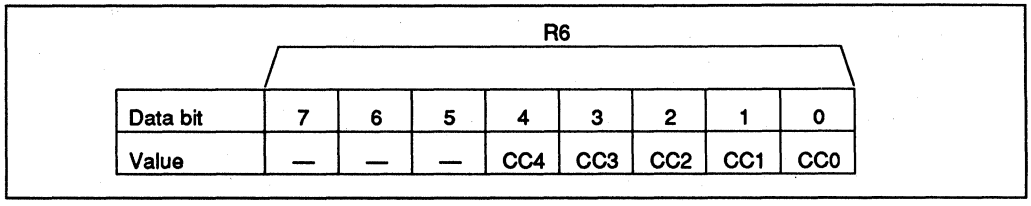

Figure 24 Centering Character Register

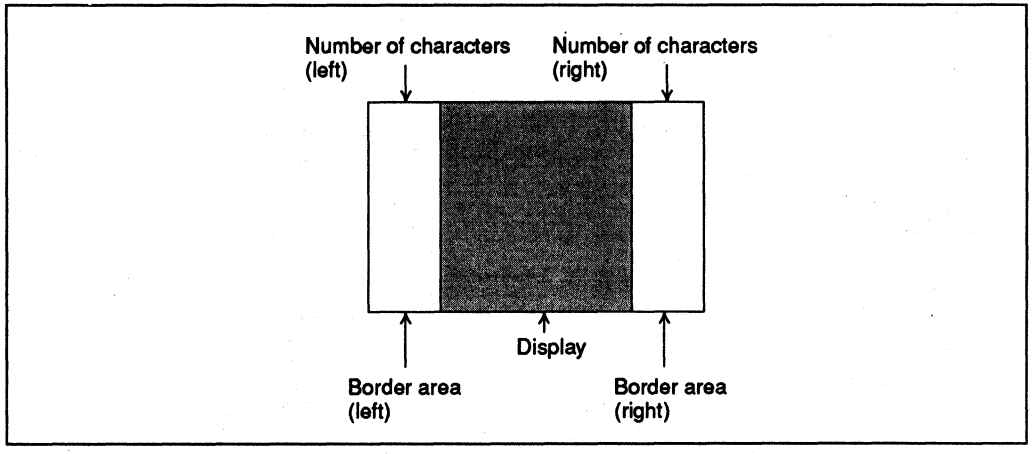

Figure 25 Centering Characters

Border Color Control Register: The border color control register (figure 26), has five valid bite having two different functions. These functions are available only in with-memory mode.

- BM bit: Specifies border control mode; reset to 0. This bit must be 1 in asynchronous mode.
  - — BM = 1: Displays the color specified by the BCI, BCR, BCG, and BCB bits in the border area (disabled in synchronous mode)
  - — BM = 0: Displays the color of the dot immediately before the display period on the border area
- BCI, BCR, BCG, and BCB bits: Specify the color to be displayed on the border area. These bits are enabled when the BM bit is 1; reset to 0s.

Stretching Control Register: The stretching control register (figure 27), composed of four valid bits, is used in combination with the stretching index register (R9 and R10). It specifies the period for stretching in units of lines. The value to write to this register is "number of lines –1." This register is enabled when the control register's STE bit is 1.
This register is set automatically in VGA mode.

R7

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	BM	BCI	BCR	BCG	BCB

Figure 26 Border Color Control Register

R8

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	—	SF3	SF2	SF1	SF0

Figure 27 Stretching Control Register

5

Stretching Index Register: The stretching index register (figure 28), composed of 16 valid bits, is used in combination with the stretching control register (R8). It specifies the lines to be displayed twice among those specified by R8. The lines represented by the SI bits which are set to 1s will be displayed twice. Although this register has 16 bits, only the bits within the period specified by R8 are enabled. For example, when R8 is set to four, only five bits of SI0 to SI4 of this register are enabled (figure 29).
This register is set automatically in VGA mode.

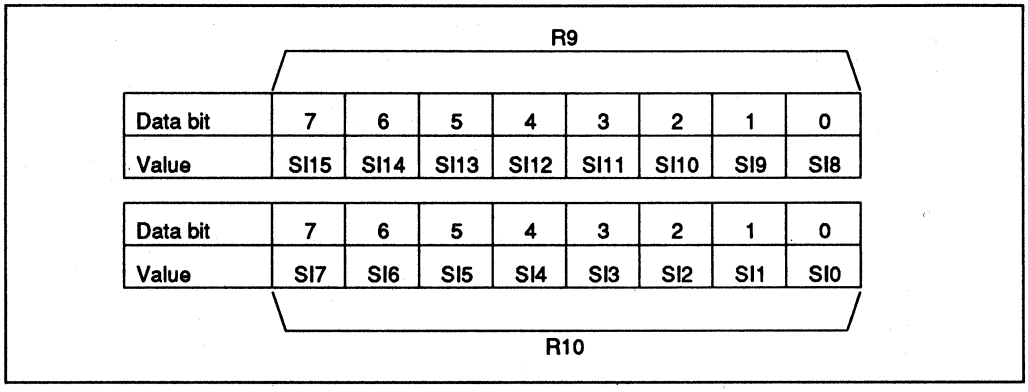

Figure 28 Stretching Index Register

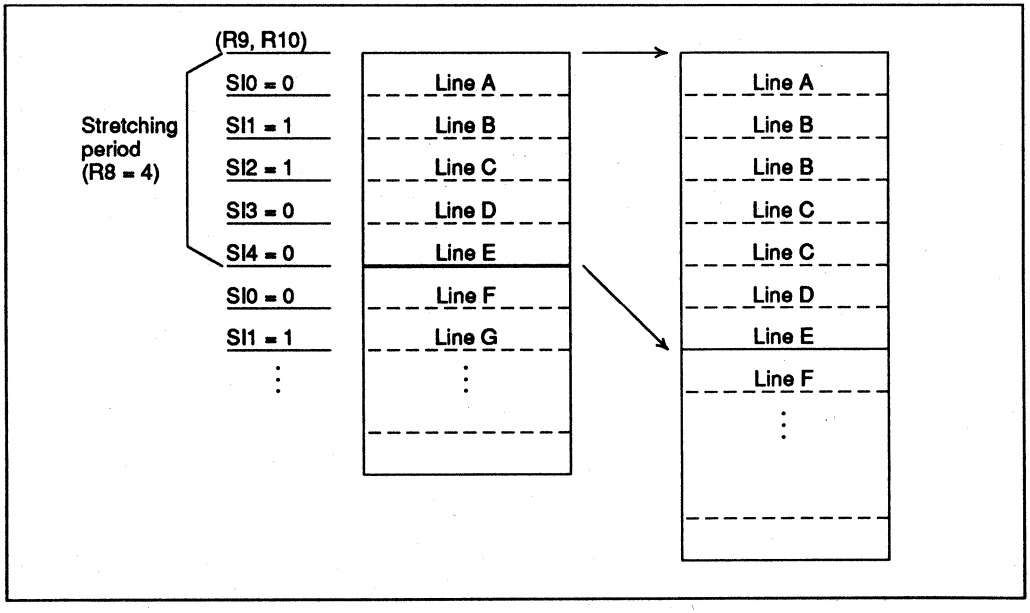

Figure 29 Stretching Display

Gradation Level Palette Address Register: The gradation level palette address register (figure 30) is composed of six valid bits with two different functions.

- PS1 and FS0 bits: Specify a method of selecting the plane of the gradation level palettes (R, G, or B).

  — (PS1, PS0) = (0, 0): Every time the gradation level palette data register (R12) is read from or written to, either R-, G-, or B-palette is automatically selected, in that order

  — (PS1, PS0) = (0, 1): R-palette is selected

  — (PS1, PS0) = (1, 0): G-palette is selected

  — (PS1, PS0) = (1, 1): B-palette is selected

- PA3–PA0 bits: Specify the desired gradation level palette using the address written to these bits. After palette address specification, data is read from or written to the specified palette and the address is automatically incremented by 1. The address increment manner depends on PS1 and PS0 settings.

  — (PS1, PS0) = (0, 0): Gradation level palette address is automatically incremented by 1 after reading/writing data from/to R, G, and B gradation level palettes in that order, through the gradation level palette data register

  —Other settings: Gradation level palette address is automatically incremented by 1 after reading/writing data from/to any one gradation level palette, through the gradation level palette data register

R11

Data bit	7	6	5	4	3	2	1	0
Value	—	—	PS1	PS0	PA3	PA2	PA1	PA0

Figure 30 Gradation Level Palette Address Register

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Gradation Level Palette Data Register: The gradation level palette data register (figure 31), composed of six valid bits, contains data which is read from or written to the gradation level palette specified with the gradation level palette address register (R11).

Gradation level palettes must be set according to the display mode used (16-level grayscale display or 4096-color-scale display); the R-palette must be used for 16-level grayscale display, and R-, G-, and B-palettes for 4096-color-scale display. PD5 bit must be 1 and PD4 bit must be 0 in frame-based data thinning mode. PD4 bit must be 1 in 1/2 pulse width modulation mode. Show table 13.

In the MPU programming method, the gradation level palettes must be read/written after 100 ms have elapsed after reset. Note that display is scattered during palette read/write.

In the MPU programming method, gradation level palettes are not directly read from, but are read from via this register. Consequently, any data that happens to be in this register at that time is read out in the first read cycle, and then data corresponding to the specified address is transferred to this register and read from this register in the following read cycle. The address is incremented (or R-, G-, and B-palettes are switched) at the same time. In other words, after address setting, the first data read is incorrect, and the second data read is correct. Consequently, one dummy read is required after setting a gradation level palette address. Figure 32 shows the timing for reading a gradation level palette.

R12

Data bit	7	6	5	4	3	2	1	0
Value	—	—	PD5	PD4	PD3	PD2	PD1	PD0

Figure 31 Gradation Level Palette Data Register

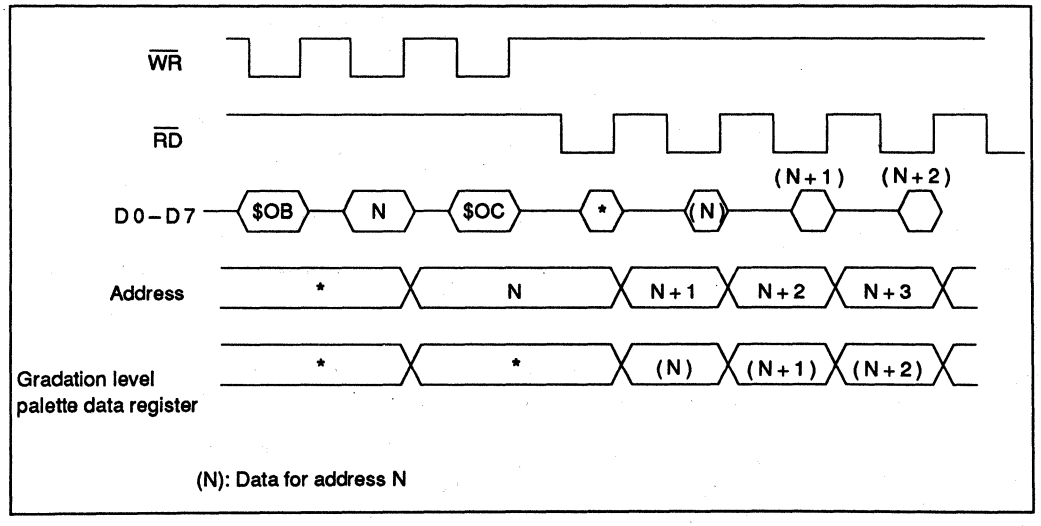

Figure 32 Gradation Level Palette Data Read

Gradation Display Clock Period Register: The gradation display clock period register (figure 33), composed of nine valid bits, specifies the period of XCL1, the LCD data latch clock, when pulse width modulation method is used for gradation display. The value to write to this register is "specified number – 1," in units of dots. Eight through 512 dots can be specified. Note that this register is invalid in with-memory mode.
This register is set automatically in VGA mode.

- GC8–GC0 bits: Specify the number of dots for T1; T1 is the period of XCL1 for 1/2 pulse width gradation display. When the total number of dots for one period of the YCL1 clock pulse cannot be divided by two for 1/2 pulse width gradation display, the remainder is added to T1 as T1', where T1' = T_L – T1 (figure 34).

R13

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	—	—	—	—	GC8

Data bit	7	6	5	4	3	2	1	0
Value	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

R14

Figure 33 Gradation Display Clock Period Register

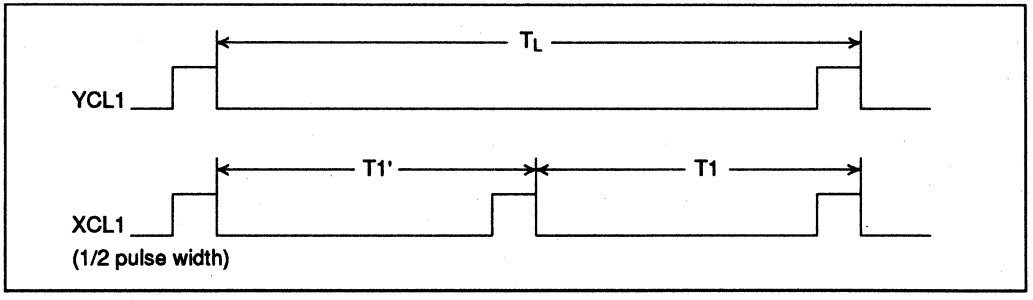

Figure 34 T_L, T1, and T'

Reset Description

The $\overline{RES}$ signal resets and starts the CLINE. The $\overline{RES}$ signal must be supplied at each power-on. Reset is defined as shown in figure 35.

Pin: In principle, the $\overline{RES}$ signal does not control output signals and it operates regardless of other input signals. The reset states of input/output pins are described below.

- D0–D7: Not affected by reset. These pins output data even during the reset state when $\overline{RD}$ = 0, $\overline{CS}$ = 0, RS = 1, and $\overline{WR}$ = 1, in the MPU programming method.
- A0–A5: Always output 0s during the reset state in the ROM programming method. Otherwise, these pins serve as input pins.

Registers: The contents of all internal registers are lost and cleared; the desired data must be rewritten after reset.

Palettes: Palettes are automatically loaded after reset with the appropriate data according to the display mode. When data different from the automatically set data is needed, the data must be overwritten 100 µs or more after reset. (100 µs is required for automatic data setting.)

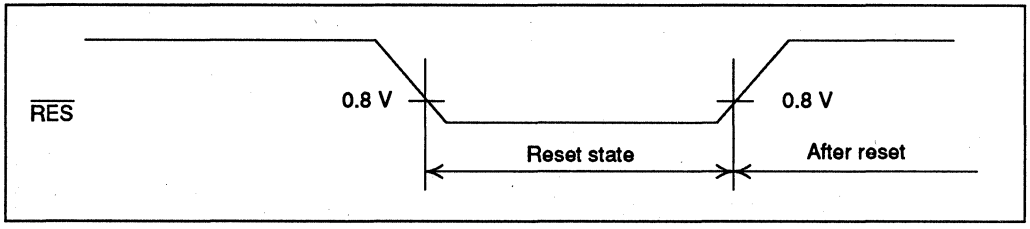

Figure 35 Reset Definition

There are some restrictions and notices in the HD66850F. Please check the following content, and use it.

Input Signal Timing

HSYNC, VSYNC Asserted Width: The HSYNC and VSYNC input signals have the minimum asserted width to operate correctly, please keep the asserted width with the below value or more.

HSYNC to VSYNC, HSYNC to $\overline{\text{BLANK}}$ Phase Shift: There are some restrictions between HSYNC and VSYNC, and HSYNC and $\overline{\text{BLANK}}$. Don't input them within the restricted phase shift.

Table 16 HSYNC, VSYNC Asserted Width

Condition	Item	Symbol	Minimum Dots
All mode	Asserted HSYNC	a	12 dots or more
	Asserted VSYNC	b	2 rasters or mode

Table 17 VSYNC, $\overline{\text{BLANK}}$ Phase Shift

Condition	Item	Symbol	Available Dots
All mode	VSYNC	c	3 dots or less, 16 dots or more
	BLANK	d	1 dot or more

Note: In VGA mode, the polarities of HSYNC and VSYNC depend on the display resolution on CRT, but we will explain them as the active-high input in this document.

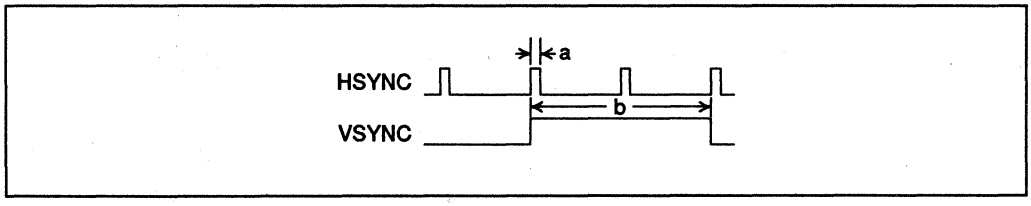

Figure 36 HSYNC, VSYNC Asserted Width

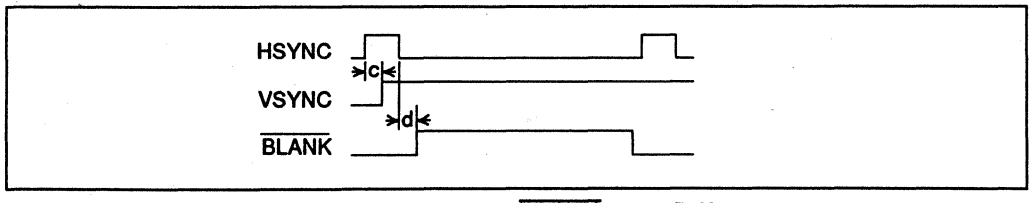

Figure 37 VSYNC, $\overline{\text{BLANK}}$ Phase Shift

5

Total Horizontal Dots: HD66850F needs 48 dots for the horizontal retrace period, and the HSYNC period must be 688 dots or more when 640 dots display, 768 dots or more when 720 dots display.

Horizontal Front Porch: There is a restriction about the horizontal front porch (from negated $\overline{\text{BLANK}}$ to asserted HSYNC) as the below in VGA mode. Please input them with the minimum value or more. Especially in 320 or 360 dots wide, period of the front porch is usually just 3 or 4 dots. Please delay HSYNC asserted timing, and hold the minimum value. Otherwise the first line on a panel will be incorrect.

Table 18 Total Horizontal Dots

Condition	Symbol	Minimum Dots
All mode	e	688 dots. (when 640 dots display)
		768 dots. (when 720 dots display)

Table 19 Horizontal Front Porch

			Dot Adjust								
Condition	Symbol	Item	–2	–1	±0	+1	+2	+3	+4	+5	+6
VGA mode	f	Horizontal 320 or 640 dots display	1 dot or more				3 dots or more				7 dots or more
		Horizontal 360 or 720 dots display	1 dot or more					5 dots or more			

Note: The BLANK 'High' width (g) must be 328 or 336 dots in 320 dots display, 376 dots in 360 dots display, 656 dots in 640 dots display, and 738 dots display in 720 dots display.

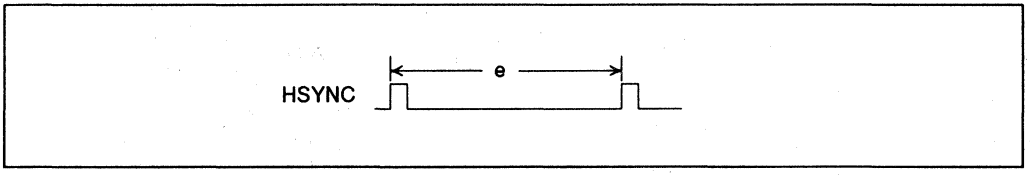

Figure 38 Total Horizontal Dots

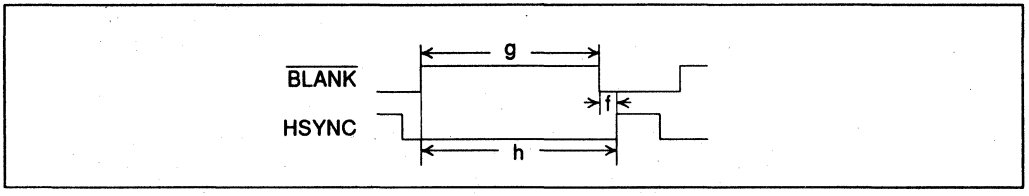

Figure 39 Horizontal Front Porch

When it displays 720 dots wide (text mode) on 640 dots panel in VGA mode, HD66850F removes 1 dot from each 9 dots. It may not display correctly according to the combination of the dot ajust and the period from negated $\overline{\text{BLANK}}$ to asserted HSYNC (h in figure 4). In this case, please change the dot adjust, or delay asserted timing of HSYNC.

This restriction causes trouble when the below equation is satisfied. When the total horizontal dot is 900 dots wide, and the period between negated $\overline{\text{BLANK}}$ to asserted HSYNC is 'h' dots,

$4 \times [(h - 2)/4 \uparrow] = 9 \times M + A$

($\uparrow$: revaluation, M and A: integer)

The 'A' which causes trouble depends on the dot ajust as below.

Table 20 Display Period + Horizontal Front Porch

Condition	Symbol	Item		Dot Adjust -2	-1	±0	+1	+2	+3	+4	+5	+6
VGA mode & with buffer memory mode, 720 dots display on 640 dots panel	h	Monochrome or 8/16 colors mode	743 to 746 dots	NG	ok	ok	ok	ok	NG	ok	ok	ok
			747 to 750 dots	NG	ok	ok	ok	NG	ok	ok	ok	ok
			751 to 754 dots	ok	ok	ok	ok	NG	ok	ok	ok	NG
			755 to 758 dots	ok	ok	ok	NG	ok	ok	ok	ok	NG
			759 to 762 dots	ok	ok	ok	NG	ok	ok	ok	NG	ok
			763 to 766 dots	ok	ok	NG	ok	ok	ok	ok	NG	ok
		64/512/4096 colors mode	743 to 764 dots	ok	NG	ok	ok	ok	ok	NG	ok	ok
			747 to 750 dots	ok	NG	ok	ok	ok	NG	ok	ok	ok
			751 to 754 dots	NG	ok	ok	ok	ok	NG	ok	ok	ok
			755 to 758 dots	NG	ok	ok	ok	NG	ok	ok	ok	ok
			759 to 762 dots	ok	ok	ok	ok	NG	ok	ok	ok	NG
			763 to 766 dots	ok	ok	ok	NG	ok	ok	ok	ok	NG

NGte: The total horizontal dot must be 900 dots wide.

Parameter	Item	Dot Adjust -2	-1	±0	+1	+2	+3	+4	+5	+6
A	Monochrome or 8/16 colors mode	1	2	3	4	5	6	7	8	0
		6	7	8	0	1	2	3	4	5
	64/512/4096 colors mode	0	1	2	3	4	5	6	7	8
		5	6	7	8	0	1	2	3	4

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Automatic Judgement of VGA Display Resolution: In VGA mode, HD66850 judges the current display resolution from the polarities of VSYNC, and HSYNC, and the width of $\overline{\text{BLANK}}$ 'H' automatically. Please input these signals as below to judge the correct resolution.

Table 21 $\overline{\text{BLANK}}$ 'High' Level Width

Condition	Symbol	VGA Mode No.	Horizontal Resolution	$\overline{\text{BLANK}}$ H Width
VGA mode	j	0/1	360 wide	378 dots
		2/3, 7	720 wide	738 dots
		4/5	320 wide	336 dots
		6, F, 10, 11, 12	640 wide	656 dots
		13 (256 col)	320 wide	328 dots

Table 22 Polarities of HSYNC and VSYNC

Condition	VGA Mode No.	Vertical Resolution	HSYNC	VSYNC
VGA mode	F, 10	350 raster high	Positive	Negative
	0/1, 2/3, 4/5, 6, 7, 13	400 raster high	Negative	Positive
	11, 12	480 raster high	Negative	Negative

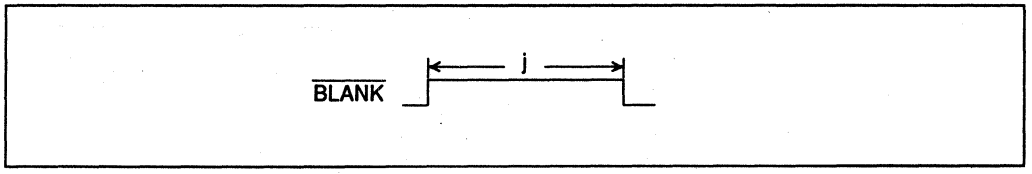

Figure 40 $\overline{\text{BLANK}}$ High Level Width

Border Area: In VGA mode, there is border area around display area. When the border and display area is scanned, $\overline{BLANK}$ is 'high' level. HD66850 internally generates the display timing which indicates just the display area from $\overline{BLANK}$ input. So, please input the $\overline{BLANK}$ with the horizontal border dot wide and vertical border high raster as below.

Table 23 Number of Horizontal Border Dot

Condition	Symbol	VGA Mode No.	Resolution	Border
VGA mode	k	0/1	360	9 dots
		2/3, 7	720	9 dots
		4/5	320	8 dots
		6, F, 10, 11, 12	640	8 dots
		13 (256 col)	320	4 dots

Table 24 Number of Vertical Border Raster

Condition	Symbol	VGA Mode No.	Resolution	Border
VGA mode	m	F, 10	350	6 rasters
		0/1, 2/3, 4/5, 6, 7, 13	400	7 rasters
		11, 12	480	8 rasters

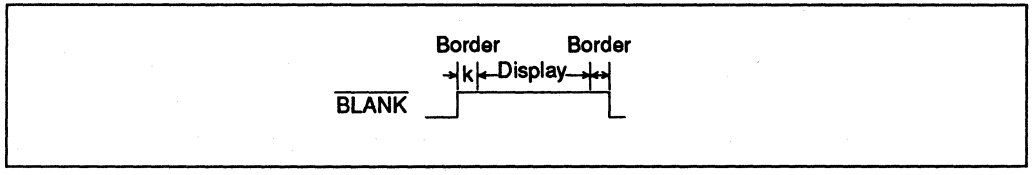

Figure 41 Number of Horizontal Border Dot

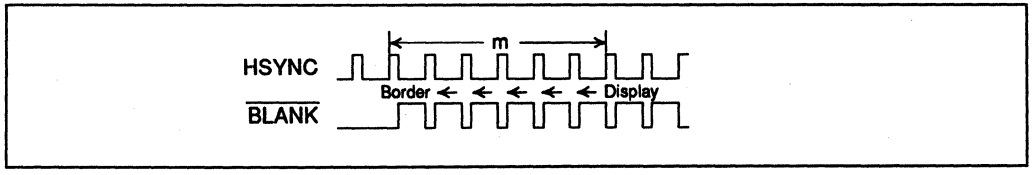

Figure 42 Number of Vertical Border Raster

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When 64 k × 4 bit (256 k) or 128 k × 8 (1M) bit memory is attached for buffer memory, please satisfy the below relationship about vertical display and border raster.

$$[\text{Vertical display raster}]+[\text{Vertical border raster after display}]\leq 512 \text{ raster}$$

Usually, the vertical 480 rasters mode (VGA mode 11, 12) has 6 or 7 border rasters, so this limitation will be no problem.

Table 25 Vertical Display Raster + Vertical Border Raster After Display

Condition	Symbol	Vertical Display Raster + Vertical Border Raster after Display
VGA and with memory mode	n	512 rasters or less

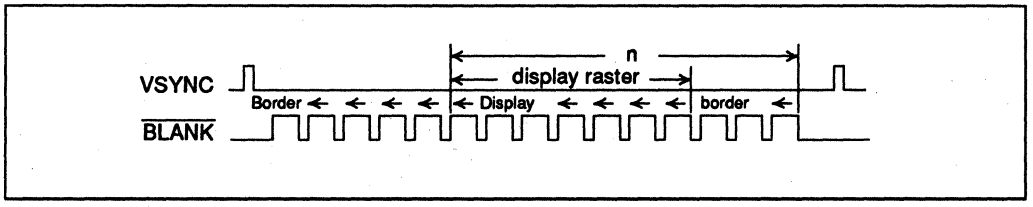

Figure 43 Vertical Display Raster

Asynchronous Mode

In asynchronous mode, the set data in the gradation palette is broken owing to the dot adjust during display. To avoid this problem, in MPU and ROM programming method, please write '1' to bit 4 (BM mode) of the border control register (R7), and all '0' to bit 3-0 (border color) of R7. The register R7 must be '10H'. In pin programming method, please adjust display timing with AJ3-AJ0 pins, and start to display just from left edge on an LCD panel without border dot, rise the $\overline{\text{BLANK}}$ input at same DOTCLK edge as change of the video data (R/G/B).

In 8/16 colors mode, this restriction is no problem in any mode because HD66850F does not access the gradation palette. In 64 / 512 / 4096 colors mode, it does not support asynchronous mode.

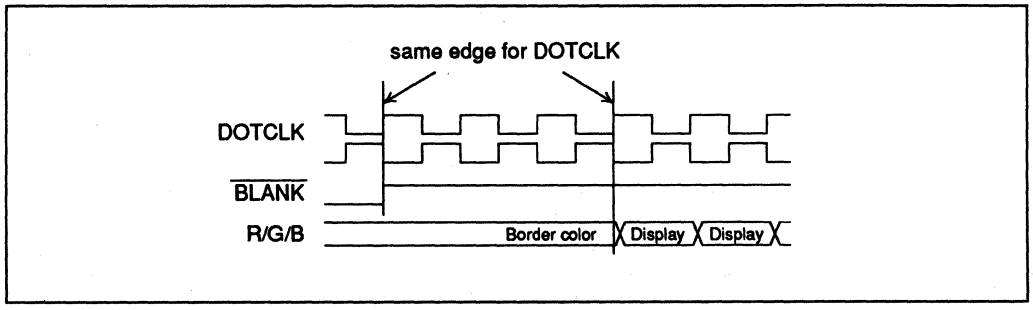

Figure 44 Countermeasure in the Pin Programming Method

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Frame Period

In synchronous with-memory mode, DOTCLK and frame period for CRT are same as one for LCD. When it displays on a full screen with stretching or centering function, HD66850F needs to extend the frame period for displaying on LCD. If this frame period for LCD were longer than one for CRT, HD66850F can not work correctly.
HD66850F needs 48 dots period for the horizontal retrace, and number of the total horizontal dot for LCD is number of the horizontal display dot + 48 dots. This minimum frame period which is necessary to display on LCD is shown as below.

$$\text{Minimum frame period for LCD} = \left(\text{Number of horizontal display dot} + 48\right) \times \text{Vertical panel size [dots]}$$

The frame period for CRT must be longer than the above minimum one for LCD.
For example, when HD66850F stretchs CRT resolution with 640 × 350 dots to the LCD panel with 640 × 480 dots, the minimum frame period for LCD is (640 + 48) × 480 = 330, 240 dots.

On the other hand, when number of the total horizontal dot for CRT is 800 dots wide, 330, 240/800 = 412.8 rasters, so HD66850F needs 413 or more rasters high as the total vertical raster for CRT.

In asynchronous mode, HD66850F separates LCD clock (LDOTCK) from CRT clock (DOTCK), and the both frame period are different. So, this limitation is no problem.

LCD Alternating Signal M

When LCD alternating signal M is changed at same line in each frame, brightness of the line differs from one of another line. To avoid this problem, the signal M is ususally controlled to change at different line in each frame. But period of the signal M may synchronize with the frame period according to the total vertical raster. In this case, adjust period of the M, and don't synchronize them.

Especially, it is easy to synchronize them in VGA 720 × 400 dots mode. For example, when it displays 720 × 400 dots in synchronous with-memory mode, usaually number of the total horizontal dot for CRT is 900 dots wide, and number of the total vertical raster is 448 rasters high, so the frame period for CRT is 900 × 448 = 403,200 [dots]. On the other hand, number of the total horizontal dot for LCD is 720 + 48 = 768 dots wide, and the frame period (403,200 dots) divided by a total horizontal dot for LCD (766 dots) is 512 which is interger. So, when line number of period of the M equals to the following divisor of 512:

[1, 3, 5, 7, 15, 21, 25, 35, 75, 105, 175] (lines),

period of the M synchronizes with the frame period, and a horizontal bright line is appeared when the M is changed.

Vertical Centering

Number of vertical centering line depends on 'the value in register (R5) + 1' in non-VGA mode, or on the VSIZE pin and display resolution in VGA mode. But when '0' is written in the register (R5) and the vertical centering is enabled, HD66850F can not works correctly. Don't set '0' in the register (R5). And when number of vertical display raster is same as the vertical panel size (VSIZE), the vertical centering enable bit (bit 3 in R0) must be cleared. Especially in VGA mode, please update the enable bit according to selected VGA display mode.
When stretching function is selected, there is no restriction about setting '0' in the stretching registers (R8, R9, R10).

Table 26 Notes on VGA Mode Usage by LCD Panel Size

Horizontal Size (dots)	Vertical Size (lines)	Notes
640	—	• In VGA text modes (0/1, 2/3, 7), there is no space between characters.
720	—	• In VGA graphic modes (4/5, 6, F, 10, 11, 12, 13), horizontal centering is necessary. (Display is automatically centered horizontally in with-memory mode. See note below.)
—	400	• Data on line 401 through line 480 in VGA 640-by-480 graphic modes (11, 12) are not displayed. • Vertical centering or stretching is necessary for VGA 640-by-350 graphic modes (F, 10). (Display is automatically stretched in with-memory mode. See note below.)
—	480	• Vertical centering or stretching is necessary for VGA text modes (0/1, 2/3, 7). (Display is automatically stretched in with-memory mode. See note below.) • Vertical centering or stretching is necessary for VGA 640-by-200 or 320-by-200 graphic modes (4/5, 6, 13). (Display is automatically stretched in with-memory mode. See note below.) • Vertical centering or stretching is necessary for VGA 640-by-350 graphic modes (F, 10). (Display is automatically stretched in with-memory mode. See note below.)

Note: For without-memory mode, external circuits or BIOS tuning are required.

Table 27 Notes on Internal Register Settings

Register No.	Bits	Register or Bit Function	Notes VGA	Notes Non-VGA
R0	STE	Stretching enable	1	1
R0	CRE	Vertical centering enable	2	2
R0	CCE	Horizontal centering enable	3	4
R0	SP	Double-width display set	5	4
R0	DISPON	Display on	6	6
R1	DOTE	Dot clock phase select	4	4
R1	AJ3–AJ0	Display timing adjust	4	4
R2	DH6–DH0	Display horizontal size set	7	4
R3–R4	DV8–DV0	Display vertical size set	8	4
R5	CR7–CR0	Centering raster set	8	4
R6	CC4–CC0	Centering character set	3	4
R7	BM	Border control mode select	9	9
R7	BCI, BCR, BCG, BCB	Border color select	10	10
R8	SF3–SF0	Stretching period	8	4
R9–R10	SI15–SI0	Stretching index set	—	—
R11	PS1–PS0	Gradation display palette select	11	11
R11	PA3–PA0	Gradation display palette address set		
R12	PD5–PD0	Gradation level palette data set		
R13–R14	GC8–GC0	Gradation display clock period set	7	12

Notes:
1. Simultaneous use with vertical centering function is impossible.
2. Simultaneous use with stretching function is impossible.
3. Automatically set for a 640- or 320-dot-wide display on a 720-dot-wide LCD panel; cannot be rewritten.
4. Must be set after reset.
5. Automatically set for a middle-resolution display; cannot be rewritten.
6. Display will turn on four frames after reset. Display will not turn on during four frames after reset.
7. Automatically set according to the horizontal panel size and number of displayed horizontal dots; cannot be rewritten.
8. Automatically set according to the vertical panel size and polarity of HSYNC and VSYNC signals; cannot be rewritten.
9. Available only in with-memory mode.
10. Available only in asynchronous with-memory mode.
11. In the MPU programming method, automatically set for 16-level display after reset; can be rewritten 100 µs after reset. In ROM programming method, appropriate data must be written.
12. In with-memory mode, automatically set according to the horizontal panel size and number of displayed horizontal dots; cannot be rewritten. For without-memory mode, appropriate data must be written after reset.

Table 28 Limits on Register Values

Register Function	Applied to	Limits
Horizontal display size control	R2	$4 \le Nchd \le (R2 + 1) \le 90$ (HSIZE = 1) $4 \le Nchd \le (R2 + 1) \le 80$ (HSIZE = 0)
Vertical display size control	R3, R4	$4 \le Ncvd \le (R3, R4 + 1) \le 512$
Vertical centering	R3, R4, R5	$2 \le (R5 + 1) \le 256$ $(R5 + 1) \times 2 + Ncvd = (R3, R4 + 1)$
Horizontal centering	R2, R6	$2 \le (R6 + 1) \le 32$ $(R6 + 1) \times 2 + Nchd = (R2 + 1)$
Gradation display clock period control	R13, R14	$(R13, R14 + 1) = (Ncht \times 8)/n$ (MMODE1 = 1) n: 2 for 1/2 pulse width gradation display $(R2 + 1) + 8 \le Ncht$ (NMODE1 = 0)
Miscellaneous	R2, R3, R4	$1/2f_{DOTCLK} \le \{(R + 1) + 6\} \times 8 \times (R3, R4 + 1) \times f_{FLM} \le 2f_{DOTCLK}$ (SYNC = 0)

Ncht: Total number of characters on a CRT horizontal line (total number of dots on a CRT horizontal line × 1/8)
Nchd: Number of characters displayed on a CRT horizontal line (number of dots displayed on a CRT horizontal line × 1/8)
Ncvd: Number of lines displayed from screen top to bottom on the CRT display
f_{LDOTCK}: LCD dot clock frequency
f_{DOTCLK}: CRT dot clock frequency
f_{FLM}: Frame frequency

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	–0.3 to 7.0	V
Input voltage	Vin	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 ± 10%, GND = 0V, Ta = –20°C to +75°C. (If these conditions are exceeded, LSI reliability may be affected.
2. All voltages are referenced to GND = 0 V.

5

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20 to +75°C, unless otherwise specified)

Item		Symbol	Min	Max	Unit	Test Condition
Input high-level voltage	$\overline{RES}$ pin	V_{IH}	V_{CC} – 0.5	—	V	
	DOTE/$\overline{RD}$/A5, SP/$\overline{WR}$/A4		2.2	—	V	
	Other input pins*1		2.0	—	V	
Input low-level voltage		V_{IL}	—	0.8	V	
Output high-level voltage	TTL interface pins*2	V_{OH}	2.4	—	V	I_{OH} = –200 µA
	CMOS interface pins*3		V_{CC} –0.8	—	V	I_{OH} = –200 µA
Output low-level voltage	TTL interface pins*2	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface pins*3		—	0.8	V	I_{OL} = 200 µA
Input leakage current		I_{TL}	–2.5	+2.5	µA	
Three-state leakage current		I_{TSL}	–10.0	10.0	µA	
Current consumption		I_{CC}	—	100	mA	Output pins open

Notes: 1. Other input pins: DOTCLK, HSYNC, VSYNC, $\overline{BLANK}$, MS0–MS15, LDOTCK, D0–D7, AJ3/$\overline{CS}$/A3, AJ2/RS/A2, AJ1/A1, AJ0/A0, R0–R3, G0–G3, B0–B3, PMODE1, PMODE0, LMODE0–LMODE4, MMODE1, MMODE0, SYNC, VMODE, VSIZE, HSIZE, TEST1, TEST0

2. TTL interface output pins: D0–D7, DOTE/$\overline{RD}$/A5, SP/$\overline{WR}$/A4, AJ3/$\overline{CS}$/A3, AJ2/RS/A2, AJ1/A1, AJ0/A0, MD0–MD15, MA0–MA7, MA8/$\overline{SOE1}$, $\overline{SOE0}$, $\overline{WE}$, DT/$\overline{OE}$, $\overline{RAS1}$, $\overline{RAS0}$, $\overline{CAS}$, $\overline{CASL}$, SC

3. CMOS interface output pins: UD0–UD7, LD0–LD7, XCL1, YCL1, CL2, FLM, M, SCLK, DISPON, DATAE

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20 to +75°C, unless otherwise specified)

Video interface

No.	Item	Symbol	Min	Max	Unit	Reference
1	DOTCLK cycle time	T_{CYCD}	31.2	62.5	ns	Figure 45
2	DOTCLK low-level pulse width	t_{WDL}	15	—	ns	
3	DOTCLK high-level pulse width	t_{WDH}	15	—	ns	
4	DOTCLK rise time	t_{Dr}	—	5	ns	
5	DOTCLK fall time	t_{Df}	—	5	ns	
6	Video data setup time	t_{VDS}	10	—	ns	
7	Video data hold time	t_{VDH}	10	—	ns	
8	$\overline{\text{BLANK}}$ setup time	t_{BLS}	10	—	ns	
9	$\overline{\text{BLANK}}$ hold time	t_{BLH}	10	—	ns	
10	$\overline{\text{BLANK}}$ low-level pulse width	t_{BLW}	12	—	µs	
11	$\overline{\text{BLANK}}$ phase shift	t_{BLPD}	2Tc	—	ns	
12	Phase shift setup time	t_{PDS}	2Tc	—	ns	
13	Phase shift hold time	t_{PDH}	2Tc	—	ns	

Tc: DOTCLK cycle time

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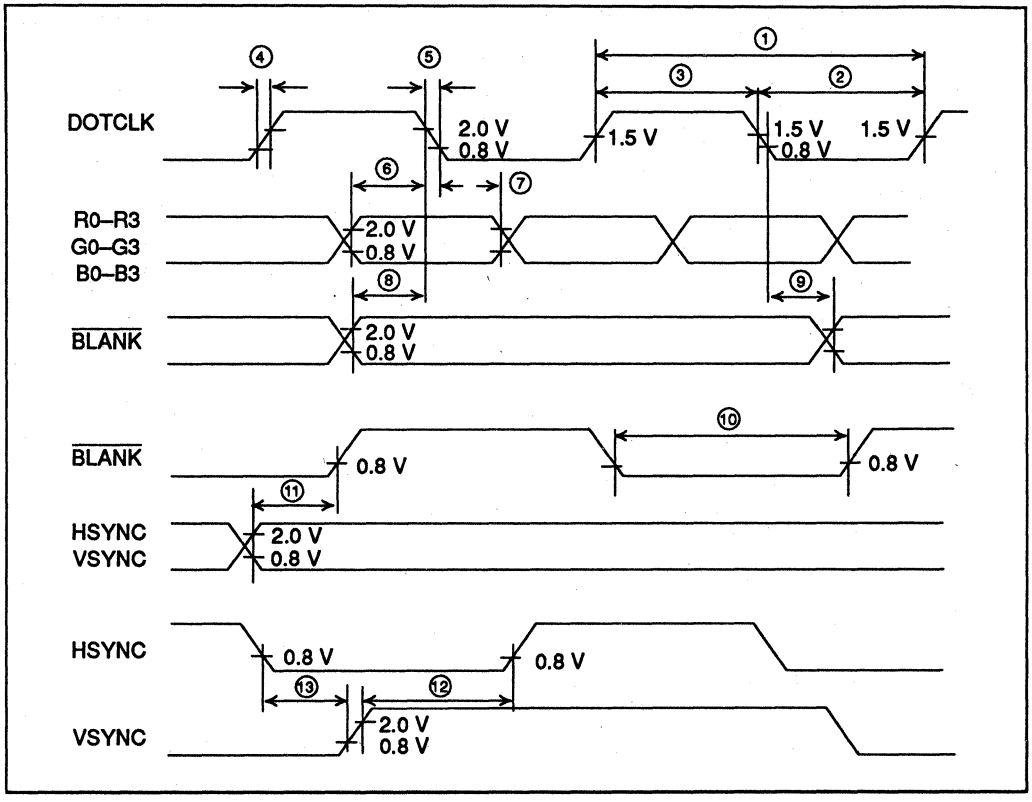

Figure 45 Video Interface

Memory interface

No.	Item	Symbol	Min	Max	Unit	Reference
14	$\overline{RAS}$ cycle time	t_{RC}	12Tc – 10	—	ns	Figure 46
15	$\overline{RAS}$ low-level pulse width	t_{RAS}	5Tc	128Tc – 20	ns	
16	$\overline{RAS}$ high-level pulse width	t_{RP}	4Tc – 40	—	ns	
17	$\overline{CAS}$ hold time	t_{CSH}	6Tc – 50	—	ns	
18	$\overline{RAS}$, $\overline{CAS}$ delay time	t_{RCD}	3Tc – 40	—	ns	
19	$\overline{CAS}$ low-level pulse width	t_{CAS1}	3Tc – 35	—	ns	
20	$\overline{CASL}$ low-level pulse width	t_{CAS2}	2Tc – 30	—	ns	
21	$\overline{CAS}$ high-level pulse width	t_{CP1}	1Tc – 20	—	ns	
22	$\overline{CASL}$ high-level pulse width	t_{CP2}	2Tc – 20	—	ns	
23	$\overline{CAS}$ cycle time	t_{PC}	4Tc – 20	—	ns	
24	$\overline{RAS}$ hold time	t_{RSH}	4Tc – 40	—	ns	
25	Row address setup time	t_{ASR}	2Tc – 50	—	ns	
26	Row address hold time	t_{RAH}	2Tc – 30	—	ns	
27	Column address setup time	t_{ASC}	1Tc – 30	—	ns	
28	Column address hold time	t_{CAH}	2Tc – 40	—	ns	
29	$\overline{WE}$ setup time	t_{WS}	2Tc – 50	—	ns	
30	$\overline{WE}$ hold time	t_{WH}	2Tc – 40	—	ns	
31	Memory data setup time	t_{MDS}	1Tc – 30	—	ns	
32	Memory data hold time	t_{MDH}	2Tc – 35	—	ns	
33	Data transfer $\overline{DT}/\overline{OE}$ setup time	t_{DTS}	2Tc – 50	—	ns	Figure 47
34	Data transfer $\overline{DT}/\overline{OE}$ hold time	t_{DTH}	6Tc – 50	—	ns	
35	Phase shift between $\overline{CAS}$ and $\overline{DT}/\overline{OE}$	t_{CDH}	2Tc – 40	—	ns	
36	Phase shift between $\overline{CAS}$ and $\overline{DT}/\overline{OE}$	t_{DTR}	2Tc – 50	—	ns	
37	$\overline{CAS}$ setup time	t_{CSR}	2Tc – 50	—	ns	Figure 48
38	$\overline{CAS}$ hold time	t_{CHR}	6Tc – 50	—	ns	
39	Phase shift between $\overline{RAS}$ and $\overline{CAS}$	t_{RPC}	2Tc – 50	—	ns	
40	SC cycle time	t_{SCC}	$4T_L$ – 10	—	ns	Figure 49
41	SC high-level pulse width	t_{SC}	$2T_L$ – 50	—	ns	
42	SC low-level pulse width	t_{SCP}	$2T_L$ – 50	—	ns	
43	Memory data read setup time	t_{RDS}	40	—	ns	
44	Memory data read hold time	t_{RDH}	5	—	ns	
45	Phase shift between $\overline{SOE}$ and SC	t_{DSE}	20	—	ns	

T_C: DOTCLK cycle time

T_L: LDOTCK cycle time (= T_C for synchronous mode)

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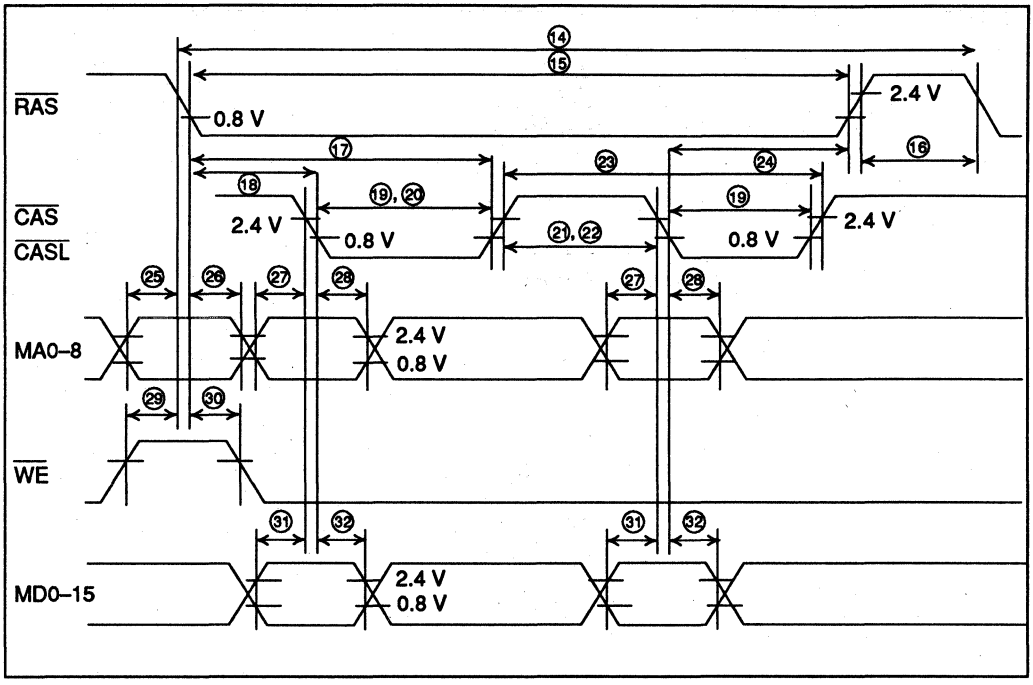

Figure 46 Memory Interface (write)

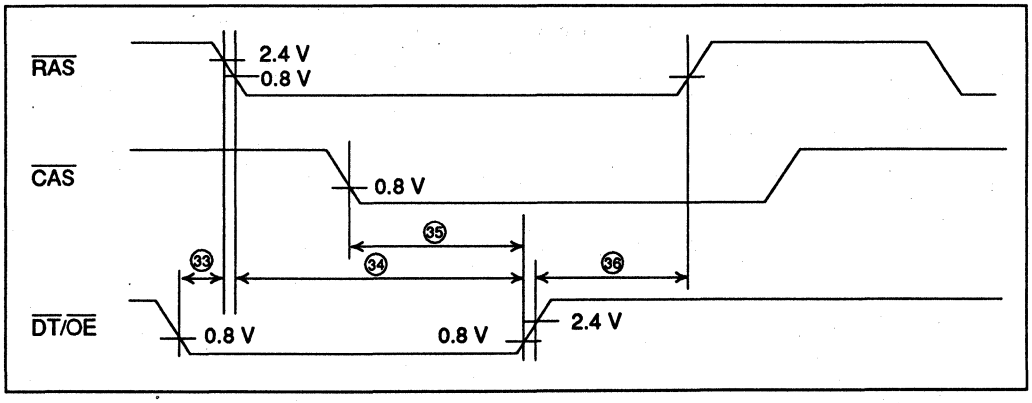

Figure 47 Memory Interface (data transfer)

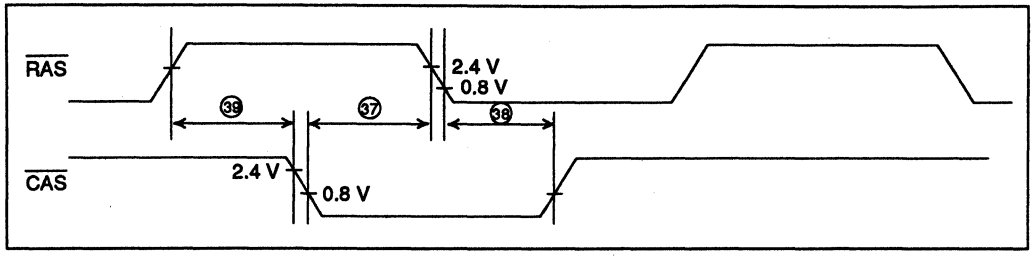

Figure 48 Memory Interface (refresh)

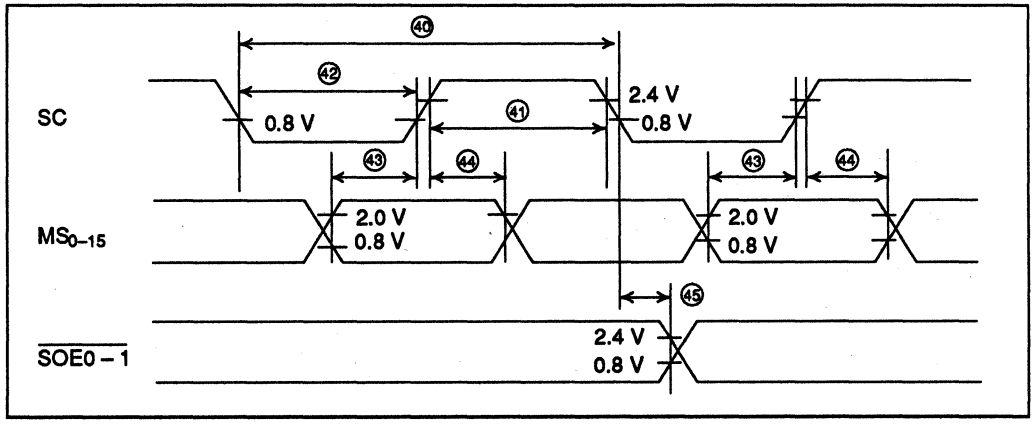

Figure 49 Memory Interface (serial read)

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LCD driver interface

No.	Item	Symbol	Min	Max	Unit	Reference
46	CL2 cycle time	t_{WCL2}	$2T_L - 10$*1	—	ns	Figure 50
			$4T_L - 10$*2			
			$8T_L - 10$*3			
			$16T_L - 10$*4			
47	CL2 high-level pulse width	t_{WCL2H}	$1T_L - 40$*1	—	ns	
			$2T_L - 40$*2			
			$4T_L - 40$*3			
			$8T_L - 40$*4			
48	CL2 low-level pulse width	t_{WCL2L}	$1T_L - 40$*1	—	ns	
			$2T_L - 40$*1			
			$4T_L - 40$*2			
			$8T_L - 40$*4			
49	CL1 high-level pulse width	t_{WCL1h}	150	—	ns	
50	LCD data delay time	t_{DD}	—	30	ns	
51	CL1 setup time	t_{SCL1}	200	—	ns	
52	CL1 hold time	t_{HCL1}	200	—	ns	
53	M output delay time	t_{DM}	—	100	ns	
54	FLM setup time	t_{HF}	100	—	ns	
55	LDOTCK cycle time	t_{CYCL}	31.2	100	ns	
56	LDOTCK high-level pulse width	t_{WLL}	15	—	ns	
57	LDOTCK low-level pulse width	t_{WLH}	15	—	ns	
58	LDOTCK rise time	t_{Lr}	—	5	ns	
59	LDOTCK fall time	t_{Lf}	—	5	ns	

T_L: LDOTCK cycle time (= T_C for synchronous mode)

Notes: 1. For display modes 9, 13, 16, 19, and 20
2. For display modes 1, 5, 10, 11, 14, 15, 17, and 18
3. For display modes 2, 3, 6, 7, and 12
4. For display modes 4, and 8

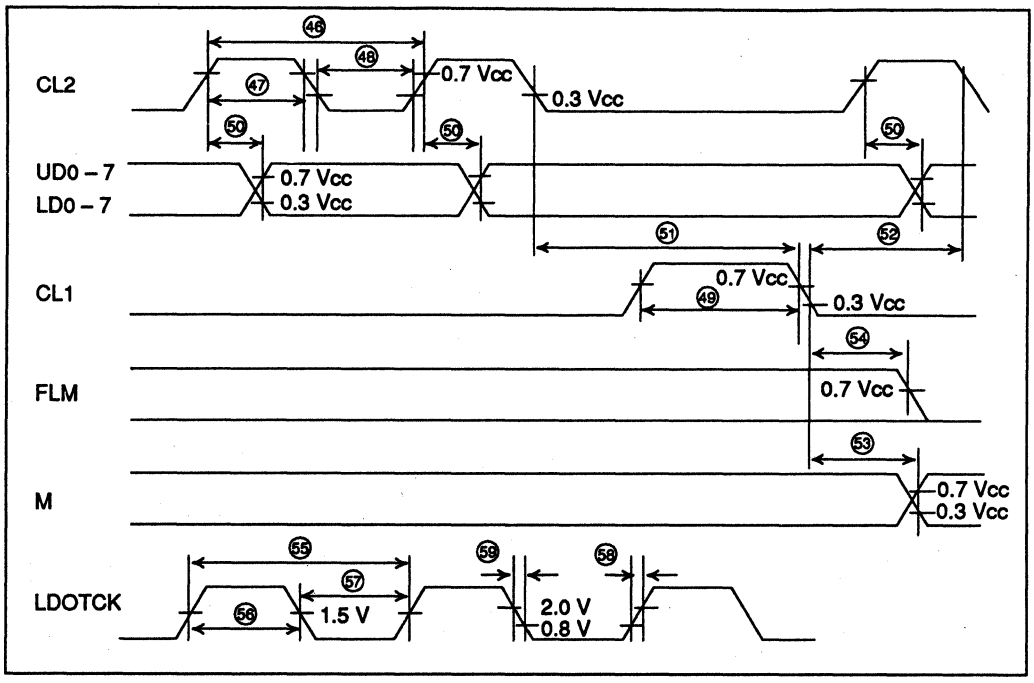


Figure 50 LCD Driver Interface

MPU interface

No.	Item	Symbol	Min	Max	Unit	Reference
60	$\overline{RD}$ low-level pulse width	t_{WRDL}	$4T_C$	—	ns	Figure 51
61	$\overline{RD}$ high-level pulse width	t_{WRDH}	$4T_C$	—	ns	
62	$\overline{WR}$ low-level pulse width	t_{WWRL}	$4T_C$	—	ns	
63	$\overline{WR}$ high-level pulse width	t_{WWRH}	$4T_C$	—	ns	
64	$\overline{RD}$ input inhibited time	t_{RIH}	$4T_C$	—	ns	
65	$\overline{WR}$ input inhibited time	t_{WIH}	$4T_C$	—	ns	
66	Address setup time	t_{AS}	0	—	ns	
67	Address hold time	t_{AH}	0	—	ns	
68	Data delay time	t_{DDR}	—	100	ns	
69	Data output hold time	t_{DHR}	10	—	ns	
70	Data setup time	t_{DSW}	0	—	ns	
71	Data hold time	t_{DHW}	0	—	ns	

T_C: DOTCLK cycle time

5

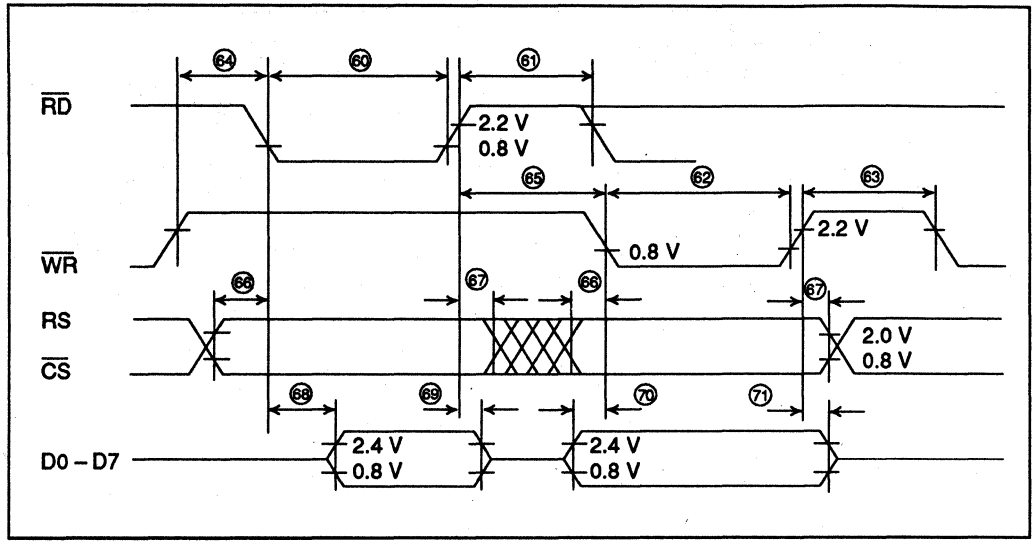


Figure 51 MPU Interface

ROM interface

No.	Item	Symbol	Min	Max	Unit	Reference
72	ROM address cycle time	t_{CYCA}	$16T_C - 20$	—	ns	Figure 52
73	ROM data setup time	t_{DSWD}	150	—	ns	
74	ROM data hold time	t_{DHWD}	10	—	ns	

T_C: DOTCLK cycle time

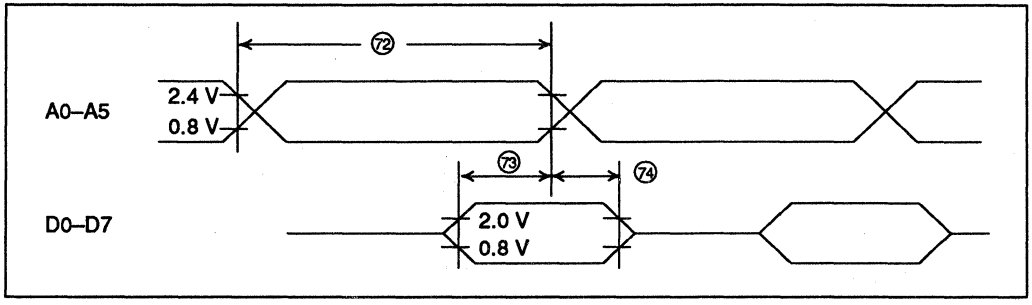


Figure 52 ROM Interface

RES timing

No.	Item	Symbol	Min	Max	Unit	Reference
75	$\overline{RES}$ low-level pulse width	t_{RES}	1	—	µs	Figure 53

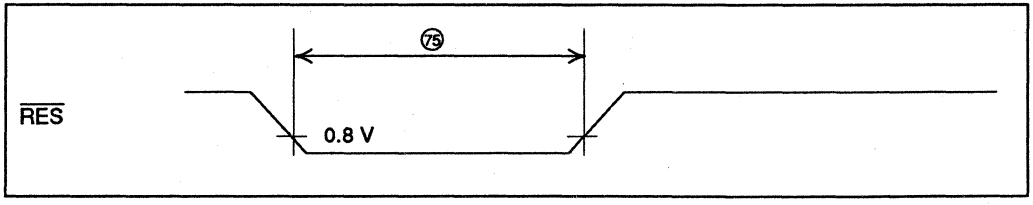


Figure 53 Reset Timing

Load circuit

Pins	R_L	R	C	Reference
MA0 – MA7, MA8/$\overline{SOE1}$, $\overline{DT}$/$\overline{OE}$, $\overline{WE}$, $\overline{CAS}$, $\overline{CASL}$, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{SOE0}$, MD0 – MD15, D0 – D7, A0/AJ0, A1/AJ1, A2/RS/AJ2, A3/$\overline{CS}$/AJ3, A4/$\overline{WR}$/SP, A5/$\overline{RD}$/DOTE	2.4 kΩ	11 kΩ	40 pF	Figure 54
DISPON, DATAE, SCLK, M, FLM, CL2, YCL1, XCL1, LD0 – LD7, UD0 – UD7	—	—	40 pF	Figure 55

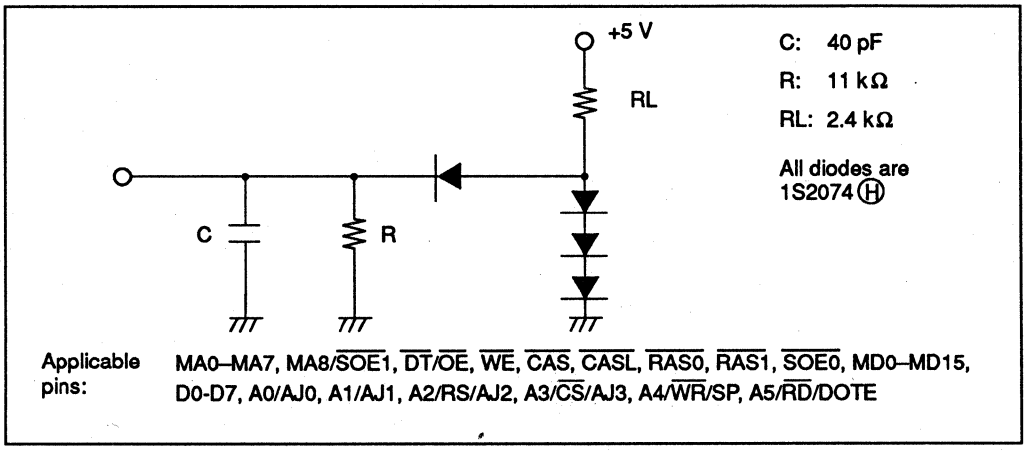


Figure 54 TTL Load Circuit

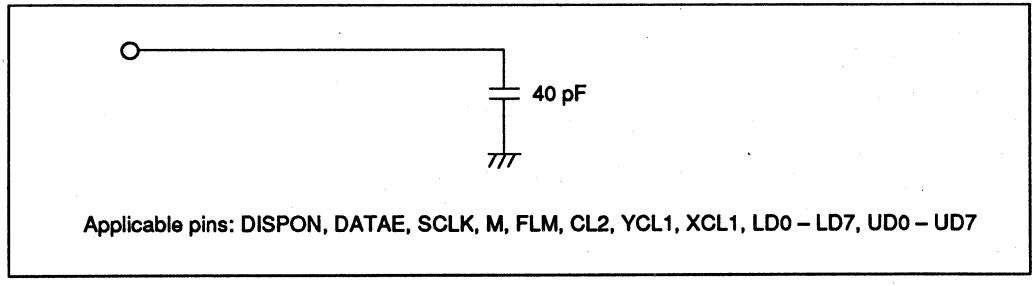


Figure 55 Capacitive Load Circuit

Section Six

Segment Type LCD Controller/Driver

HD61602/HD61603
(Segment Type LCD Driver)

Description

The HD61602 and the HD61603 are liquid crystal display driver LSIs with a TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors such as the HMCS6800 series.

The HD61602 incorporates the power supply circuit for the liquid crystal display driver. Using the software-controlled liquid crystal driving method, several types of liquid crystals can be connected according to the applications.

The HD61603 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Wide-range operating voltage
  - —Operates in a wide range of supply voltage: 2.2 V to 5.5 V
  - —Compatible with TTL interface at 4.5 V to 5.5 V
- Low current consumption
  - —Can run from a battery power supply (100 μA max. at 5 V)
  - —Standby input enables standby operation at lower current consumption (5 μA max. on 5 V)
- Internal power supply circuit for liquid crystal display driver (HD61602)
  - —Internal power supply circuit for liquid crystal display driver facilitates the connection to a microprocessor system

Versatile segment driving capacity

Type No.	Driving Method		Display Segments	Example of Use	Frame Freq. (Hz) at f_{osc} = 100 kHz	Package
HD61602	Static		51	8 segments × 6 digits + 3 marks	33	80-pin Plastic QFP (FP-80 (FP-80A) TFP-80)
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks	65	
	1/3 bias	1/3 duty	153	9 segments × 17 digits	208	
		1/4 duty	204	8 segments × 25 digits + 4 marks	223	
HD61603	Static		64	8 segments × 8 digits	33	80-pin Plastic QFP (FP-80)

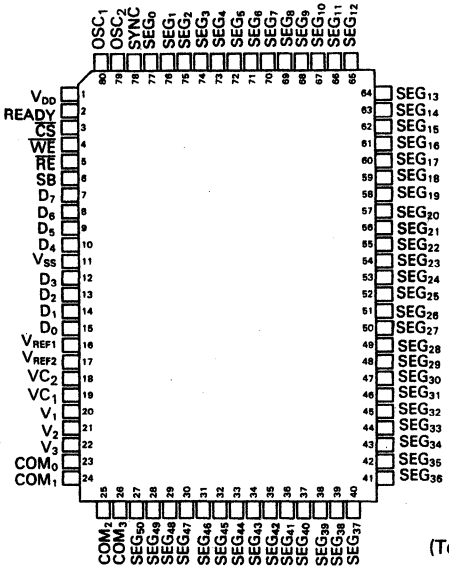
Ordering Information

Type No.	Package
HD61602R	80-pin plastic QFP (FP-80)
HD61602RH	80-pin plastic QFP (FP-80A)
HD61602TF	80-pin thin plastic QFP (TFP-80)*
HD61603R	80-pin plastic QFP (FP-80)

* Under development

Pin Arrangement (Top View)

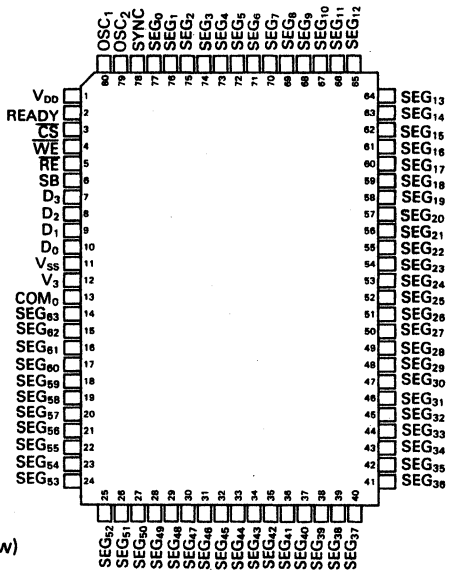
HD61602



(FP-80)

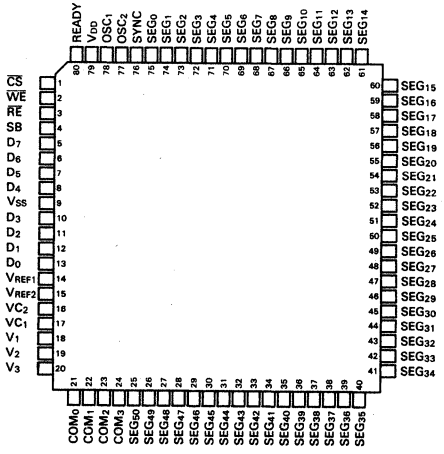
(Top View)

HD61603



(FP-80)

HD61602



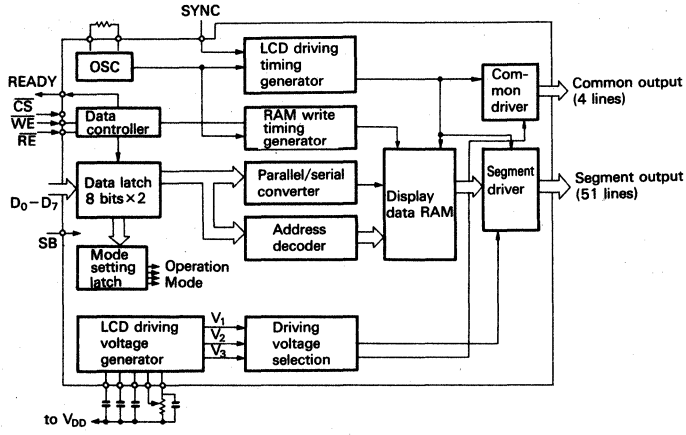
(FP-80A)

(Top View)

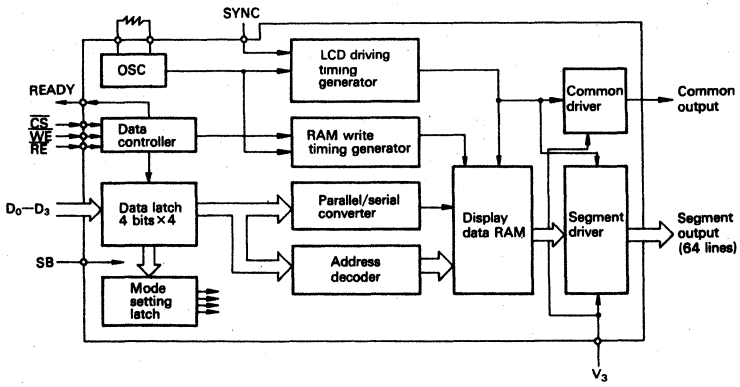
6

Block Diagram

HD61602



HD61603



Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage *	V_{DD}, V_1, V_2, V_3	0.3 to + 7.0	V
Terminal voltage *	V_T	0.3 to V_{DD} − 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	−55 to +125	°C

* Value referenced to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

Item	Symbol	Limit			Unit
		Min	Typ	Max	
Power supply voltage	V_{DD}	2.2	–	5.5	V
	V_1, V_2, V_3	0	–	V_{DD}	V
Terminal voltage *	V_T	0	–	V_{DD}	V
Operating temperature	Topr	−20	–	75	°C

* Value referenced to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics (1)

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = −20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Input high voltage	OSC_1	V_{IH1}	0.8V_{DD}	–	V_{DD}	V	
	Others	V_{IH2}	2.0	–	V_{DD}	V	
Input low voltage	OSC_1	V_{IL1}	0	–	0.2V_{DD}	V	
	Others	V_{IL2}	0	–	0.8	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	V_O = V_{DD}
Output low voltage	READY	V_{OL}	–	–	0.4	V	I_{OL} = 0.4 mA
Input leakage current *1	Input terminal	I_{IL1}	−1.0	–	1.0	μA	V_{IN} = 0−V_{DD}
	V_1	I_{IL2}	−20	–	20	μA	V_{IN} = 0−V_3
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0−COM_3	V_{d1}	–	–	0.3	V	±Id = 3 μA for each COM, V_3 = V_{DD}−3 V
	SEG_0−SEG_{50}	V_{d2}	–	–	0.6	V	±Id = 3 μA for each SEG, V_3 = V_{DD}−3 V
Power supply current		I_{DD}	–	–	100	μA	During display* R_{OSC} = 360 kΩ
		I_{DD}	–	–	5	μA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	–	–	0.4	V	V_{REF2} = V_{DD}−1 V, C_1−C_4 = 0.3 μF, RL = 3 MΩ

* Except the transfer operation of display data and bit data.
*1 V_1, V_2: apply only to HD61602.

6

DC Characteristics (2)

(V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = −20 to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Input high voltage		V_{IH}	0.8V_{DD}	–	V_{DD}	V	
Input low voltage		V_{IL}	0	–	0.1V_{DD}	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	V_{IN} = V_{DD}
Output low voltage	READY	V_{OL}	–	–	0.1V_{DD}	V	I_{OL} = 0.04 mA
Input leakage current *1	Input terminal	I_{IL1}	−1.0	0	1.0	μA	V_{IN} = 0−V_{DD}
	V_1	I_{IL2}	−20	–	20	μA	V_{IN} = 0−V_3
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0−COM_3	V_{d1}	–	–	0.3	V	±Id = 3 μA for each COM, V_3 = V_{DD}−3 V
	SEG_0−SEG_{50}	V_{d2}	–	–	0.6	V	±Id = 3 μA for each SEG, V_3 = V_{DD}−3 V
Power supply current		I_{SS}	–	–	50	μA	During display* R_{OSC} = 330 kΩ
		I_{SS}	–	–	5	μA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	–	–	0.4	V	V_{REF2} = V_{DD}−1 V, C_1−C_4 = 0.3 μF RL = 3 MΩ, V_{DD} = 3−3.8 V

* Except the transfer operation of display data and bit data.
*1 V_1, V_2: apply only to HD61602.

AC Characteristics (1)

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = −20 to+75°C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc}=360 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing		t_S	400	–	–	ns	
		t_H	10	–	–	ns	
		t_{WH}	300	–	–	ns	
		t_{WL}	400	–	–	ns	
		t_{WR}	400	–	–	ns	
		t_{DL}	–	–	1.0	μs	Figure 5
		t_{EN}	400	–	–	ns	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

AC Characteristics (2)

(V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = −20 to+75°C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc}=330 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing		t_S	1.5	–	–	μs	
(V_{DD} = 3.0−3.8 V)		t_H	1.0	–	–	μs	
		t_{WH}	1.5	–	–	μs	
		t_{WL}	1.5	–	–	μs	
		t_{DL}	–	–	2.0	μs	Figure 6
		t_{WR}	1.5	–	–	μs	
		t_{EN}	2.0	–	–	μs	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

6

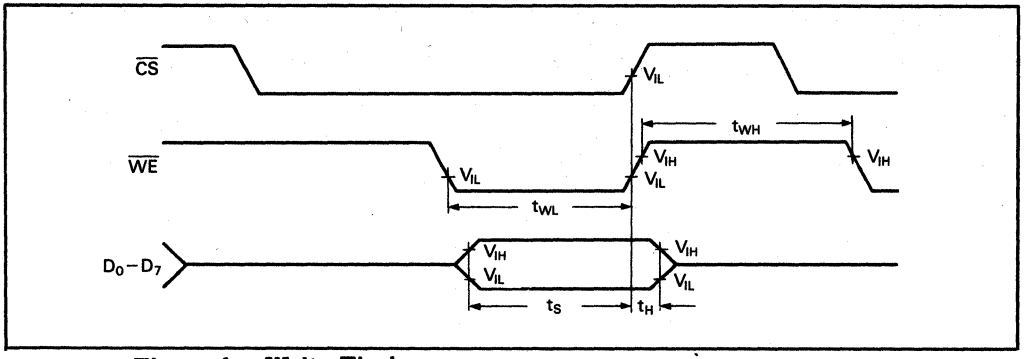


Figure 1 Write Timing
($\overline{RE}$ is fixed at high level, and SYNC at low level)

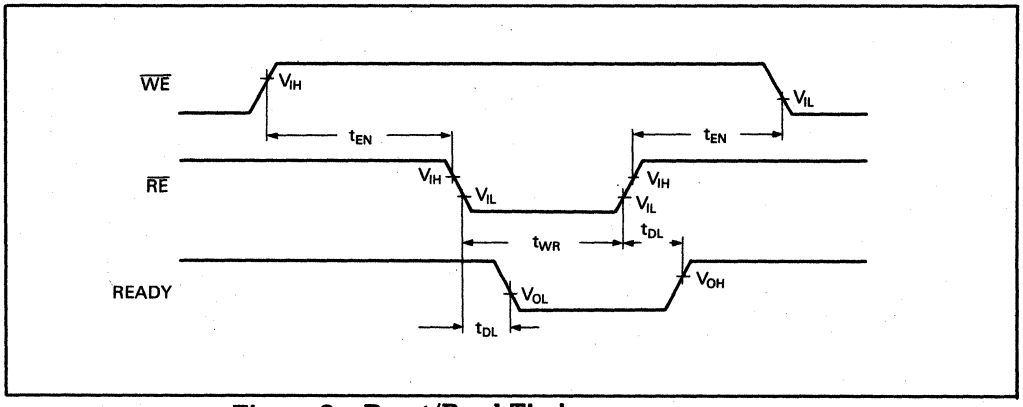


Figure 2 Reset/Read Timing
($\overline{CS}$ and SYNC are fixed at low level)

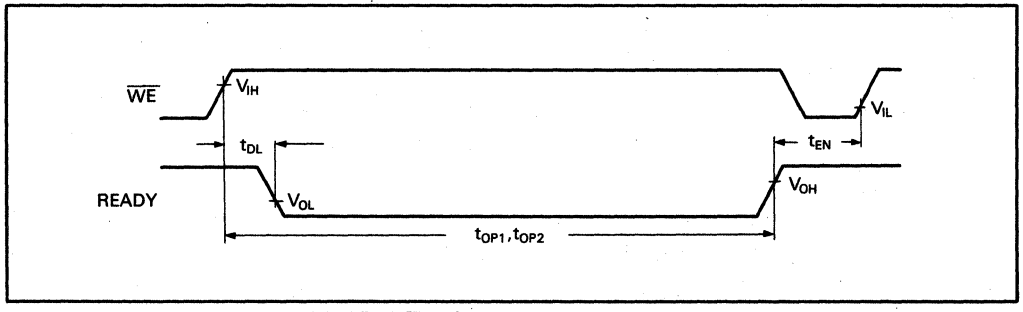


Figure 3 READY Timing
(When the READY output is always available)

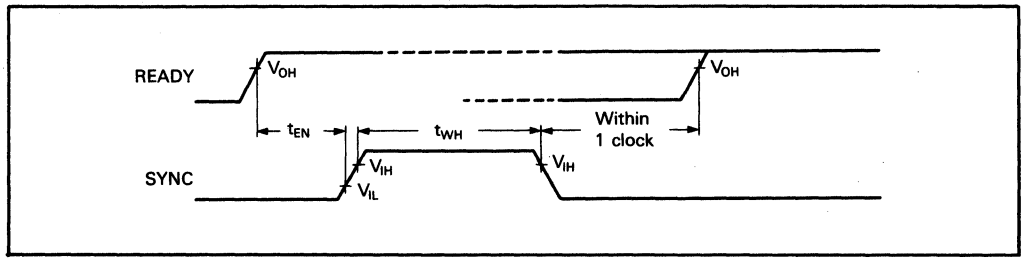


Figure 4 SYNC Timing

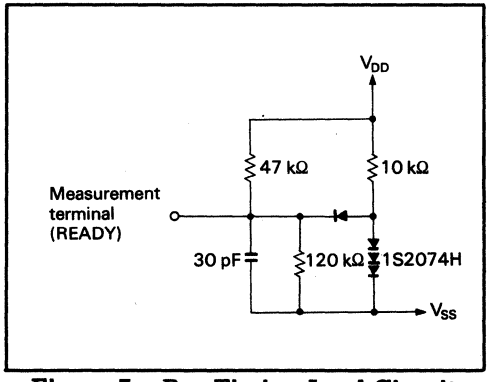


Figure 5 Bus Timing Load Circuit (LS-TTL Load)

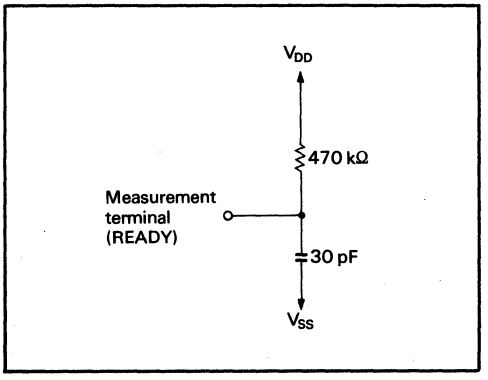


Figure 6 Bus Timing Load Circuit (CMOS Load)

6

Terminal Functions

HD61602 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D7 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0-D_7	8	Input	MCU	Data input terminal for 8-bit × 2-byte data.
V_{SS}	1	Power supply		Negative power supply.
V_{REF1}	1	Output	External R	Reference voltage output. Generates LCD driving voltage.
V_{REF2}	1	Input	External R	Divides the reference voltage of V_{REF1} with external R to determine LCD driving voltage. $V_{REF2} \fallingdotseq V_1$.
V_{C1}, V_{C2}	2	Output	External C	Connection terminals for boosting C of LCD driving voltage generator. An external C is connected between V_{C1} and V_{C2}.
V_1, V_2, V_3	3	Output (Input)	External C	LCD driving voltage outputs. An external C is connected to each terminal.
COM_0-COM_3	4	Output	LCD	LCD common (backplate) driving output.
SEG_0-SEG_{50}	51	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC1.

Note: Logic polarity is positive. 1 = high = active.

HD61603 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D_0 to D_3 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Reset the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops the LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0-D_3	4	Input	MCU	Data input terminal from where 4-bit × 4 data are input.
V_{SS}	1	Power supply		Negative power supply.
V_3	1	Input	Power supply	Power supply input for LCD drive. Voltage between V_{DD} and V_3 is used as driving voltage.
COM_0	1	Output	LCD	LCD common (backplate) driving output.
SEG_0-SEG_{63}	64	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC_1.

Note: Logic polarity is positive. 1 = high = active.

6

Display RAM

HD61602 Display RAM

The HD61602 has an internal display RAM shown in figure 7. Display data is stored in the RAM, or is read according to the LCD driving timing to display on the LCD. One bit of the RAM corresponds to 1 segment of the LCD. Note that some bits of the RAM cannot be displayed depending on LCD driving mode.

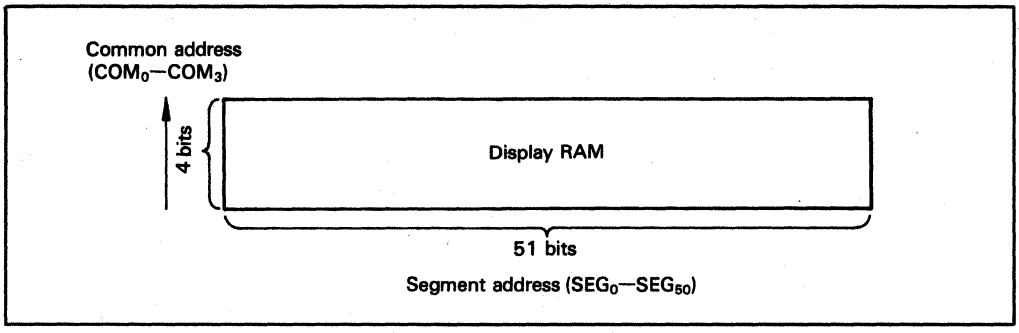
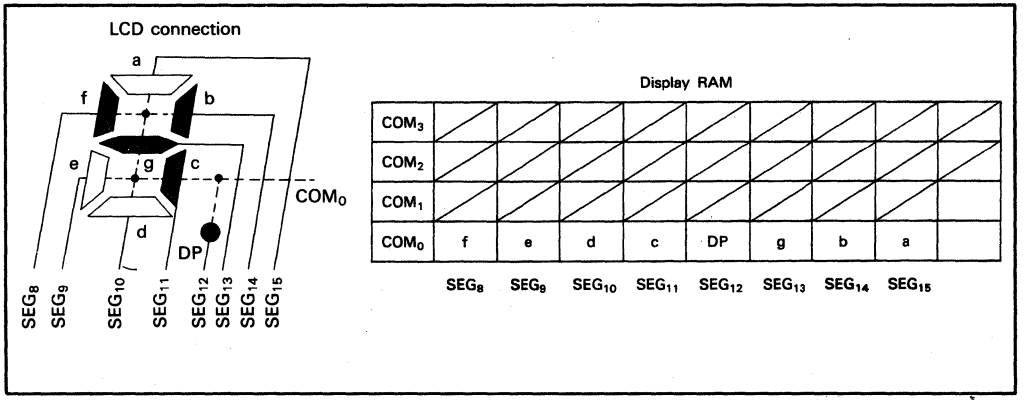


Figure 7 Display RAM

Reading Data from Display RAM: A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn terminal.

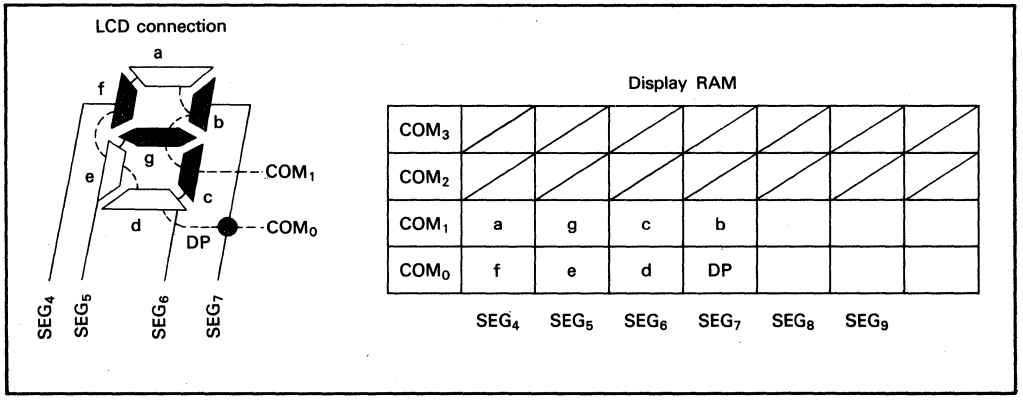
A common address corresponds to the output timing of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.
When a 7-segment type LCD driver is connected, for example, the correspondence between the display RAM and the display pattern in each mode is as follows:

1. Static drive
   In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed.



2. 1/2 duty cycle drive

   In the 1/2 duty cycle drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed.



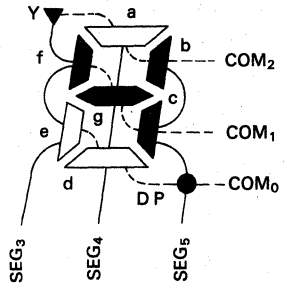
3. 1/3 duty cycle drive

   In the 1/3 duty cycle drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed.

"Y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation to turn on/off the display of "Y".

6

LCD connection



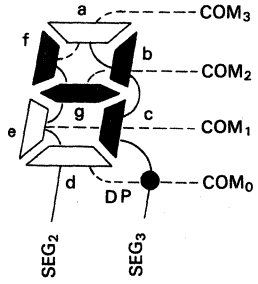
Display RAM

COM_3					
COM_2	Y	a	b		
COM_1	f	g	c		
COM_0	e	d	DP		
	SEG_3	SEG_4	SEG_5	SEG_6	

4. 1/4 duty cycle drive

In the 1/4 duty cycle drive, all the columns of COM_0 to COM_3 are displayed.

LCD connection



Display RAM

COM_3	f	a		
COM_2	g	b		
COM_1	e	c		
COM_0	d	DP		
	SEG_2	SEG_3	SEG_4	

Writing Data into Display RAM: Data is written into the display RAM in the following five methods:

1. Bit manipulation
   Data is written into any bit of RAM on a bit basis.
2. Static display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.
3. 1/2 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.
4. 1/3 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.
5. 1/4 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the alocation of the segment data for 1-digit display depend on the driving methods as described in "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty cycle driving methods. The digits are allocated as shown figure 8 (allocation of digits). As the data can be transferred on a digit basis from a microprocessor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.
Figure 8 shows the digit address (displayed

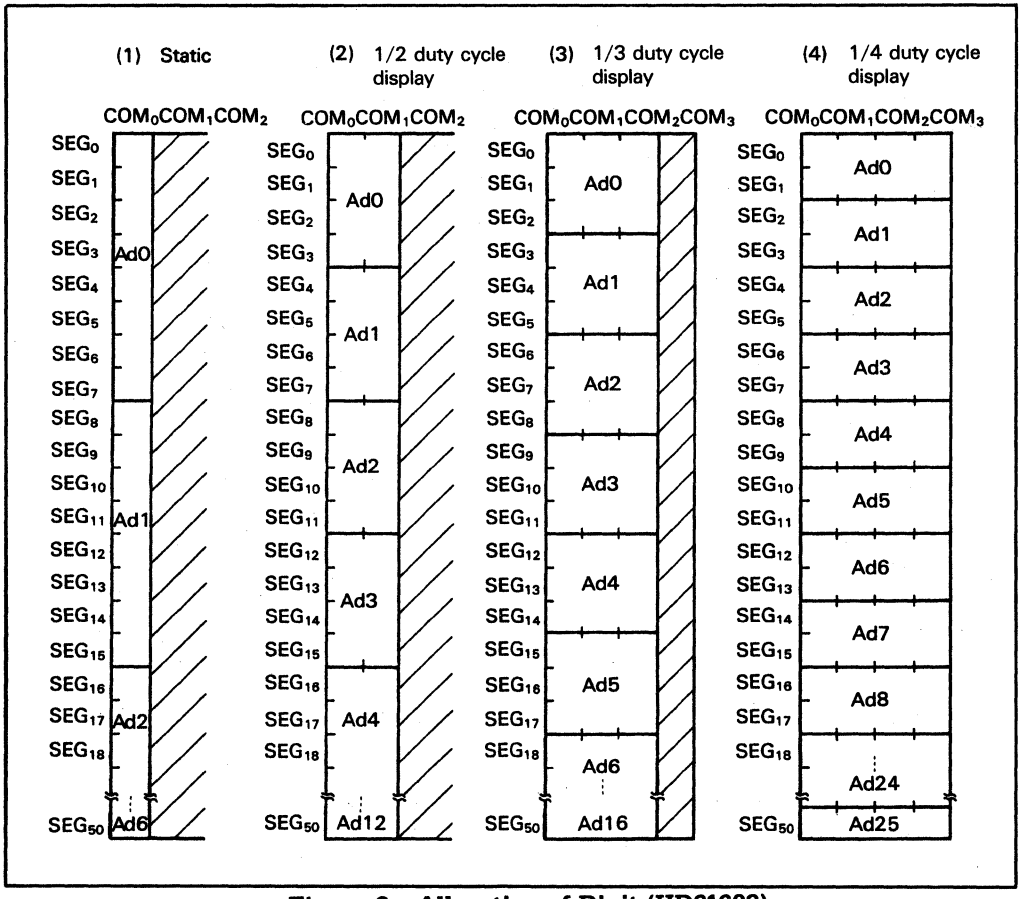


Figure 8 Allocation of Digit (HD61602)

as Adn) to specify the store address of the transferred 8-bit data on a digit basis.
Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.
When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 for static, Ad12 for 1/2 duty cycle, or Ad25 for 1/4 duty cycle, display RAM does not have enough bits for the data.

Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

HD61603 Display RAM

The HD61603 has an internal display RAM an shown in figure 10. Display data is stored in the RAM and output to the segment output terminal.

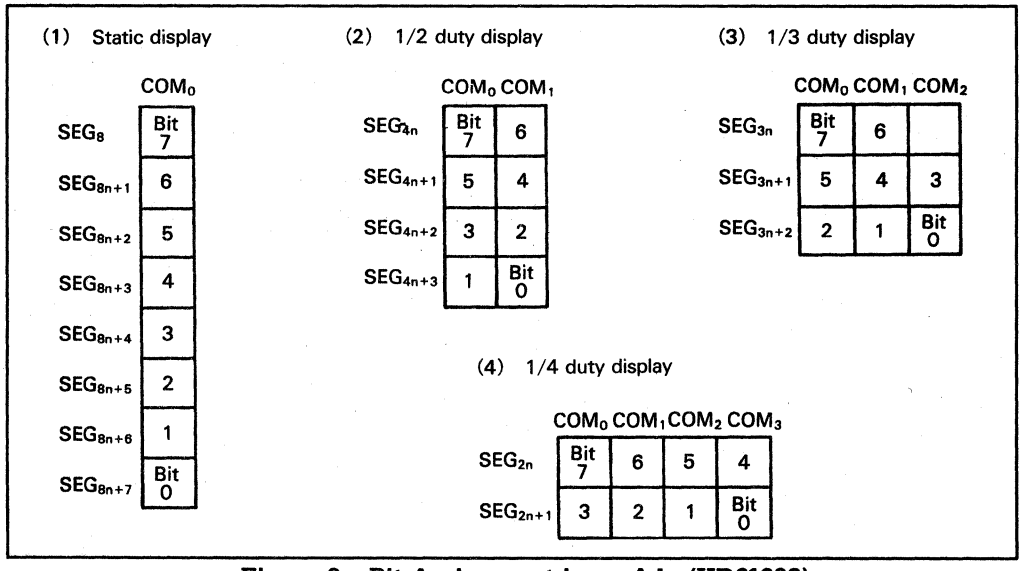


Figure 9 Bit Assignment in an Adn (HD61602)

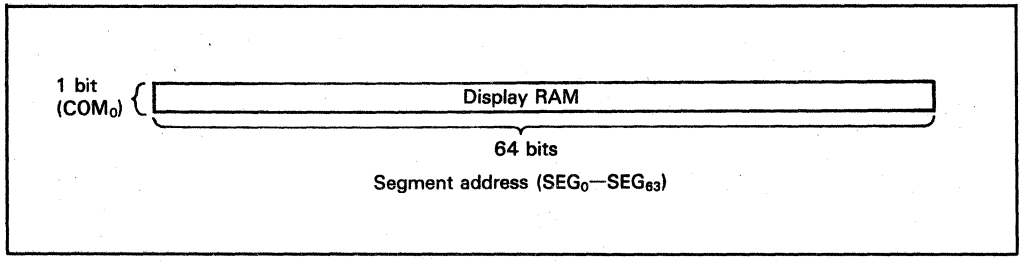


Figure 10 Display RAM (HD61603)

Reading Data from Display RAM: Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn terminal. Figure 11 shows an example of the correspondence between the display RAM bit and the display pattern when a 7-segment type LCD is connected.

Writing Data into Display RAM: Data is written into the display RAM in the following two methods:

1. Bit manipulation
   Data is written into any bit of RAM on a bit basis.
2. Static display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

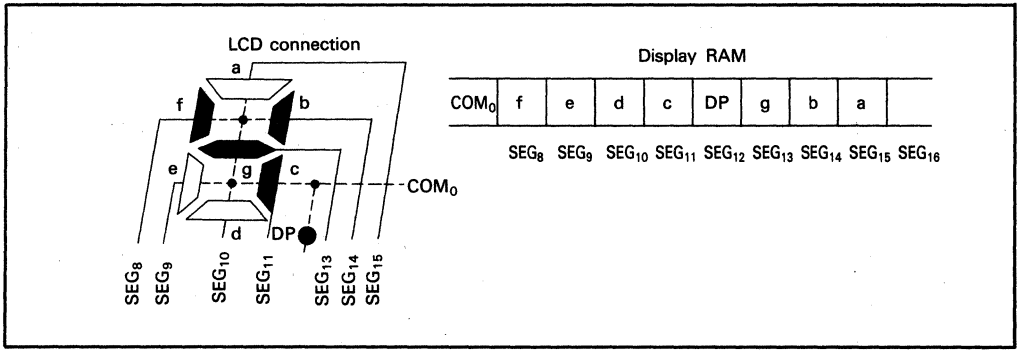


Figure 11 Example of Correspondence between Display RAM Bit and Display Pattern (HD61603)

6

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

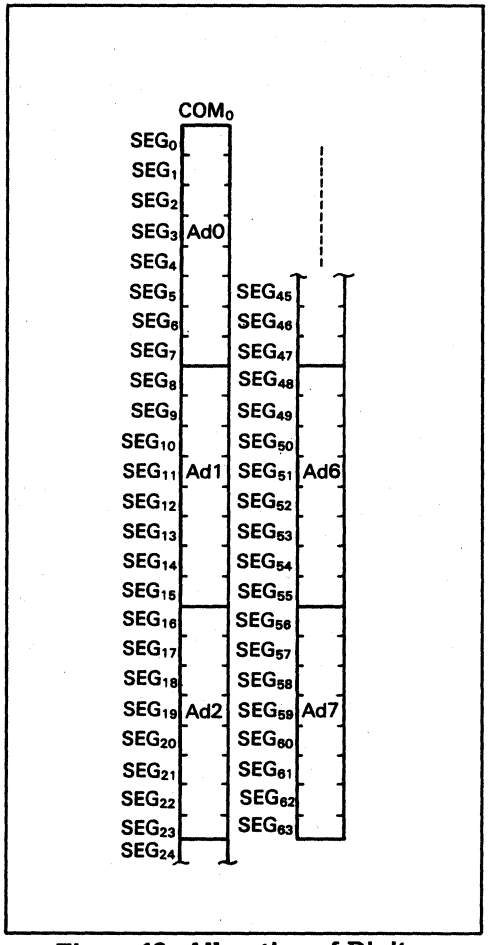


Figure 12 Allocation of Digits (HD61603)

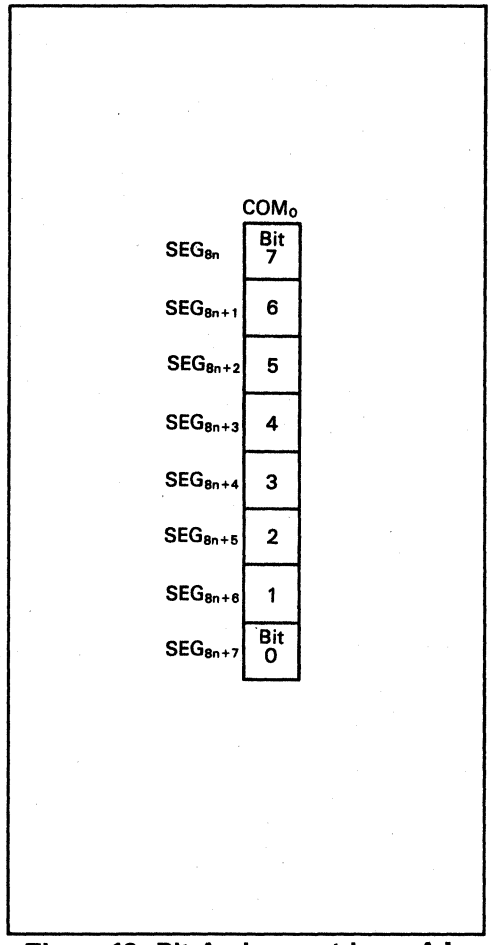


Figure 13 Bit Assignment in an Adn (HD61603)

OPERATING MODES

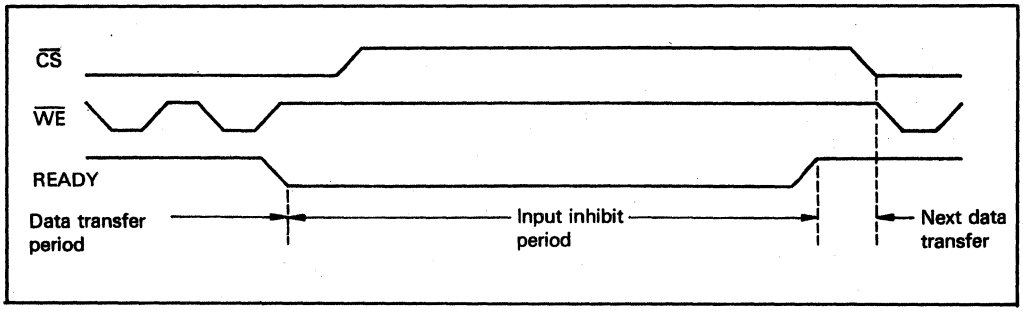
HD61602 Operating Modes
The HD61602 has the following operating modes:

1. LCD drive mode
   Determines the LCD driving method.
   a. Static drive mode
      LCD is driven statically.
   b. 1/2 duty cycle drive mode
      LCD is driven at 1/2 duty cycle and 1/2 bias.
   c. 1/3 duty cycle drive mode
      LCD is driven at 1/3 duty cycle and 1/3 bias.
   d. 1/4 duty cycle drive mode
      LCD is driven at 1/4 duty cycle and 1/3 bias.

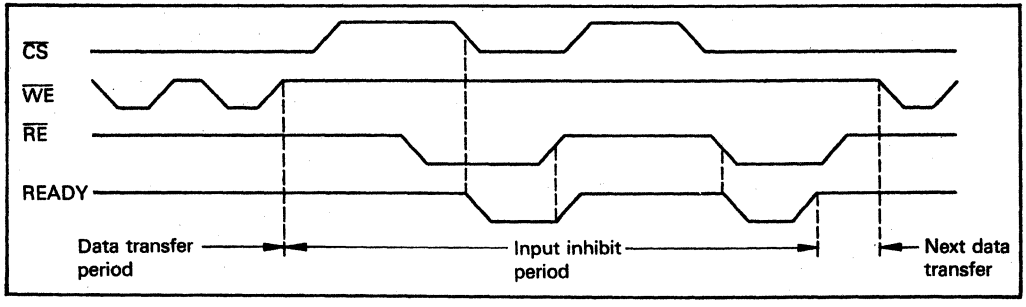
2. Data display mode
   Determines how to write display data into the data RAM.
   a. Static display mode
      8-bit data is written into the display RAM according to the digit in static drive.
   b. 1/2 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.
   c. 1/3 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.
   d. 1/4 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/4 duty cycle drive.

3. READY output mode
   Determines the READY output timing. After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when the READY is output can be selected from the following two modes:

a. READY is mode always available.



b. READY is mode available by $\overline{CS}$ and $\overline{RE}$.



4. LCD OFF mode
   In this mode, the HD61602 stops driving LCD and turns it off.

5. External driving voltage mode
   A mode for using external driving voltage (V_1, V_2, and V_3).

6

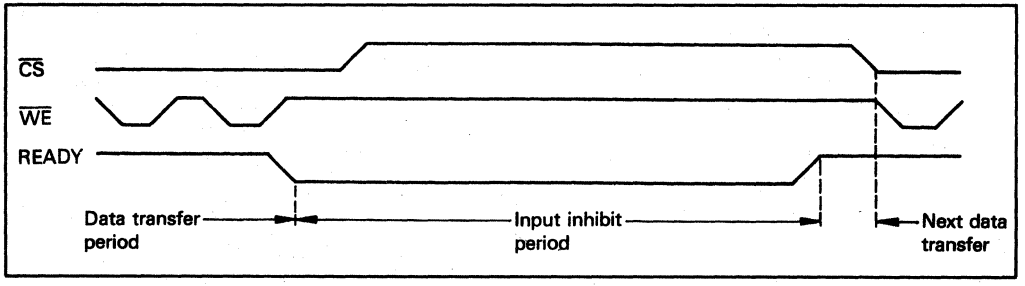
The above 5 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. Bit manipulation is independent of data display mode and can be used regardless of it.

HD61603 Operating Modes

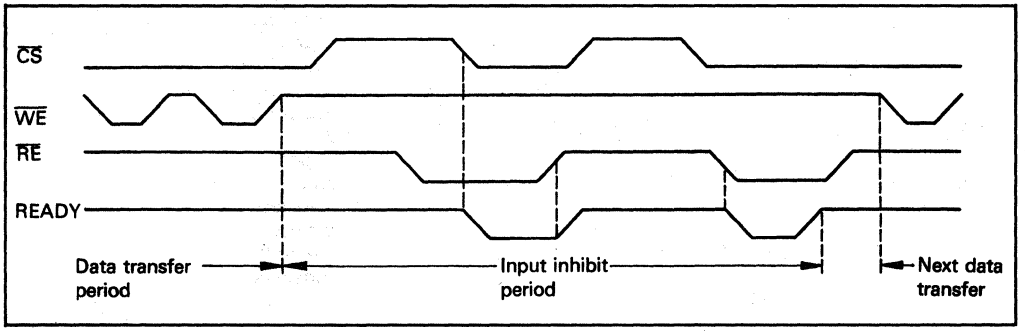
The HD61603 has the following modes:

1. READY output mode
   Determines the READY output timing. After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

   a. READY is always available.



   b. READY is mode available by CS and RE.



2. LCD OFF mode
   In this mode, the HD61603 stops driving the LCD and turns it off.

INPUT DATA FORMATS

HD61602 Input Data Formats
Input data is composed of 8 bits × 2. Input them as 2-byte data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

1. Display data (Updates display on an 8-segment basis)

1st byte

7	6	5	4	3	2	1	0
0	0	×	Display address (Digit address Adn)				

2nd byte

7	6	5	4	3	2	1	0
Display data							

a. Display address: Digit address Adn in accordance with display mode
b. Display data: Pattern data that is written into the display RAM according to display mode and the address

2. Bit manipulation data (Updates display on a segment basis)

1st byte

7	6	5	4	3	2	1	0
0	1	Display data	×	×	×	COM address	

2nd byte

7	6	5	4	3	2	1	0
×	×	SEG address					

a. Display data: Data that is written into 1 bit of the specified display RAM
b. COM address: Common address of display RAM
c. SEG address: Segment address of display RAM

3. Mode setting data

1st byte

7	6	5	4	3	2	1	0
1	0	×	0	External power supply	READY bit	Drive mode bits	

2nd byte

7	6	5	4	3	2	1	0
×	×	×	×	×	OFF/ON bit	Display mode bits	

a. Display mode bits:
00: Static display mode
01: 1/2 duty cycle display mode
10: 1/3 duty cycle display mode
11: 1/4 duty cycle display mode
b. OFF/ON bit:
1: LCD off (set to 1 when SYNC is entered.)
0: LCD on
c. Drive mode bits:
00: Static drive
01: 1/2 duty cycle drive
10: 1/3 duty cycle drive
11: 1/4 duty cycle drive
d. READY bit:
0: READY bus mode; READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered.)
1: READY port mode; READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.
e. External power supply bit:
0: Driving voltage is generated internally.
1: Driving voltage is supplied externally. (set to 1 when SYNC is entered.)

4. 1-byte instruction

1st byte

7	6	5	4	3	2	1	0
1	1	×	×	×	×	×	×

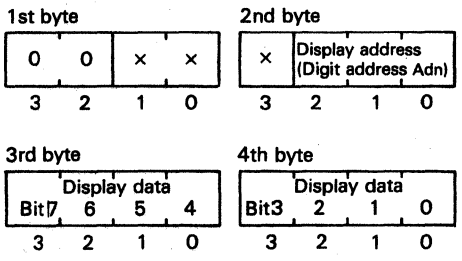
The first data (first byte) is ignored when bit 6 and bit 7 in the byte are 1.

6

HD61603 Input Data Formats

Input data is composed of 4 bits × 4. Input them as four 4-bit data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

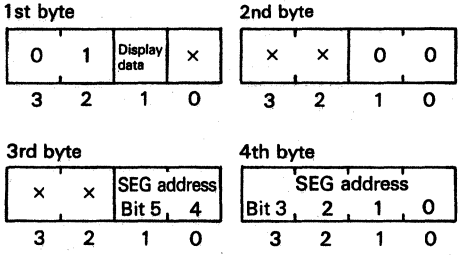
1. Display data (Updates display on an 8-segment basis.)



a. Display address: Digit address Adn shown in figure 12.

b. Display data: Pattern data that is written into the display RAM as shown in figure 13.

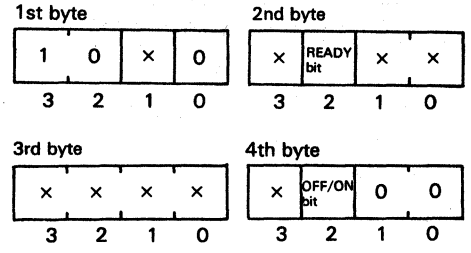
2. Bit manipulation data (Updates display on a segment basis.)



a. Display data: Data that is written into 1 bit of the specified display RAM.

b. SEG address: Segment address of display RAM (segment output).

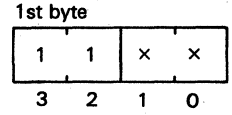
3. Mode setting data



a. OFF/ON bit:
1: LCD off (set to 1 when SYNC is entered.)
0: LCD on

b. READY bits:
0: READY bus mode; $\overline{READY}$ outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered.)
1: READY port mode; $\overline{READY}$ outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.

4. 1-byte instruction



The first data (4 bits) is ignored when bit 3 and 2 in the data are 1.

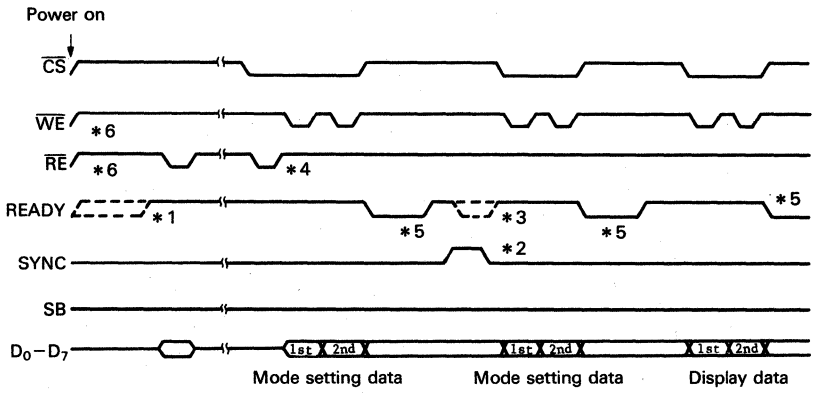
How To Input Data

How to Input HD61602 Data
Input data is composed of 8 bits × 2. Take care that the data transfer is not interrupted, because the first 8-bit data is distinguished from the second one by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ inputs low (no display data changes).
2. Input 2 or more "1-byte instruction" data in which bit 7 and 6 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 14.



*1: READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
*2: High pulse should be applied to SYNC terminal when using two or more chips synchronously.
*3: In the mode in which READY is always available, READY output is in definite while SYNC is high.
*4: Reset the byte counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
*7: It is not always necessary to follow this example.

Figure 14 Example of Data Transfer Sequence

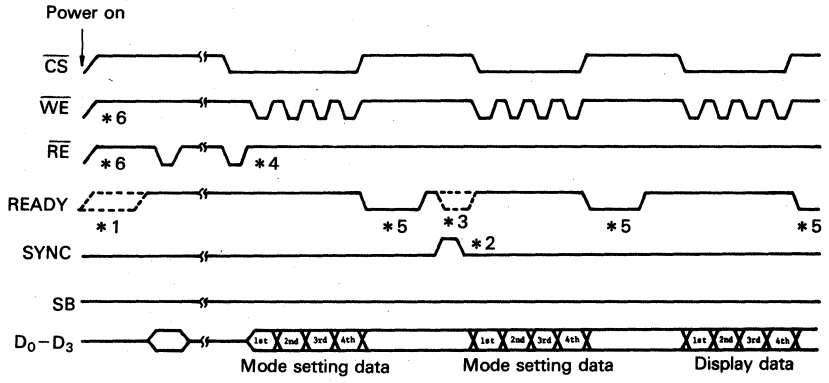
6

How to Input HD61603 Data
Input data is composed of 4 bits × 4. Take care that data transfer is not interrupted, because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ low.
2. Input 4 or more "1-byte instruction" data (4-bit data) in which bit 3 and 2 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, DO to D3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 15.



*1: READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
*2: High pulse should be applied to SYNC terminal when using two or more chips synchronously.
*3: In the mode in which READY is always available, READY output is indefinite while SYNC is high.
*4: Reset the 4-bit data counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
*7: It is not always necessary to follow this example.

Figure 15 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled until the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes:

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in figure 16 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61602 and HD61603.

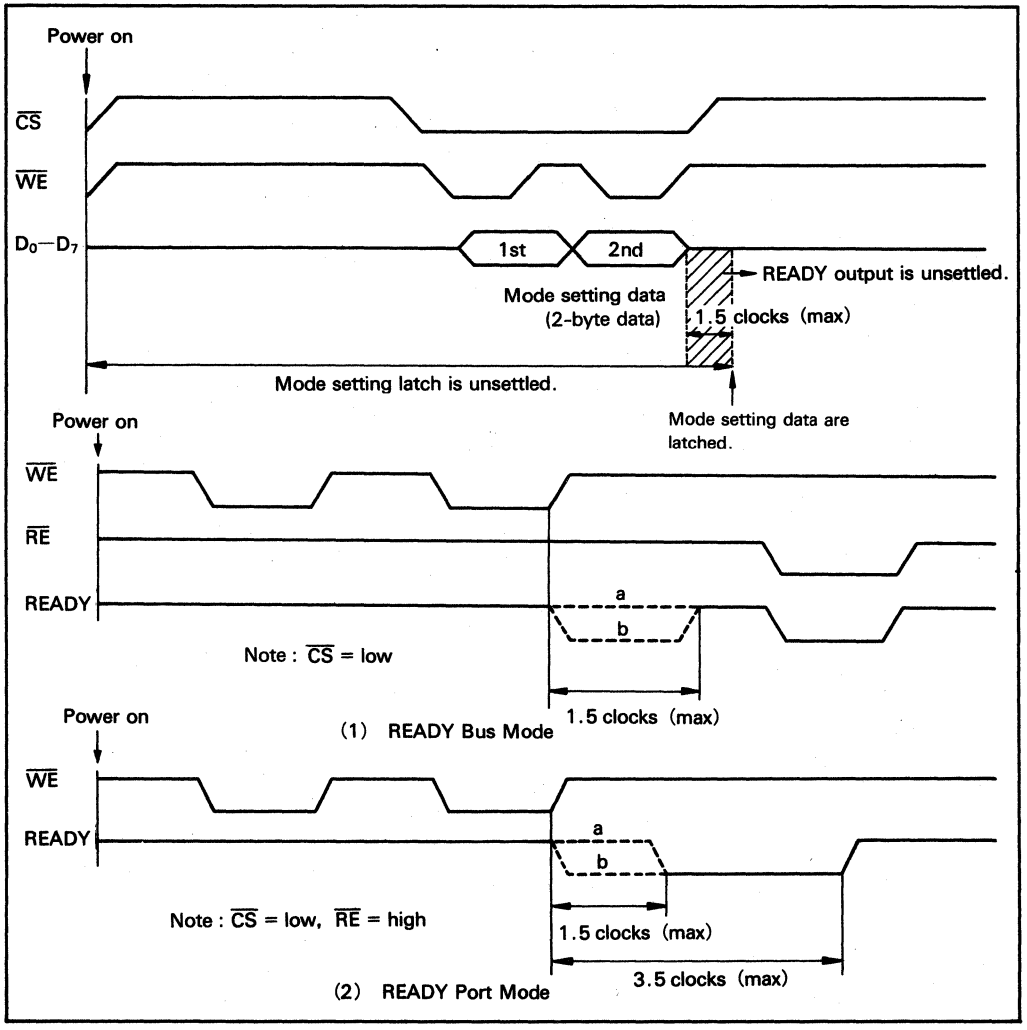


Figure 16 READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multichip Operation

When an LCD is driven with two or more chips, the driving timing of the LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See 3. Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

When SB input is used, after standby mode is released, a high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geqq$ 1 μF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61602)

What is LCD Voltage?

HD61602 drives liquid crystal display using four levels of voltages (figure 17); V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to the liquid crystal display. V_3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61602.

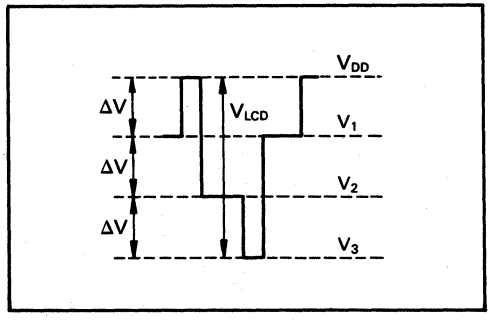


Figure 17 LCD Output Waveform and Output Levels

When Internal Drive Power Supply is Used

When the internal drive power supply is used, attach C_1-C_4 for charge pump circuits and variable resistance R_1 for deciding display drive voltage to HD61602 as shown in figure 18.

Internal voltage is available by setting external voltage switching bits of mode setting data 0.

Figure 19 shows voltage characteristics between V_{DD} and V_{REF1}. Voltage is divided at R_1, and then input into V_{REF2}. Voltage between V_{DD} and V_{REF2} is equivalent to ΔV in figure 19, and so V_{LCD} can be changed by regulating the voltage.

V_{REF2} is usually regulated by variable resistance, but when replacing R_1 with two nonvariable resistances take V_{REF1} between max and min into consideration as shown in figure 19.

Internal drive power supply is generated by using capacitance, and so large current cannot flow. When large liquid crystal display panel is used, examine the external drive power supply.

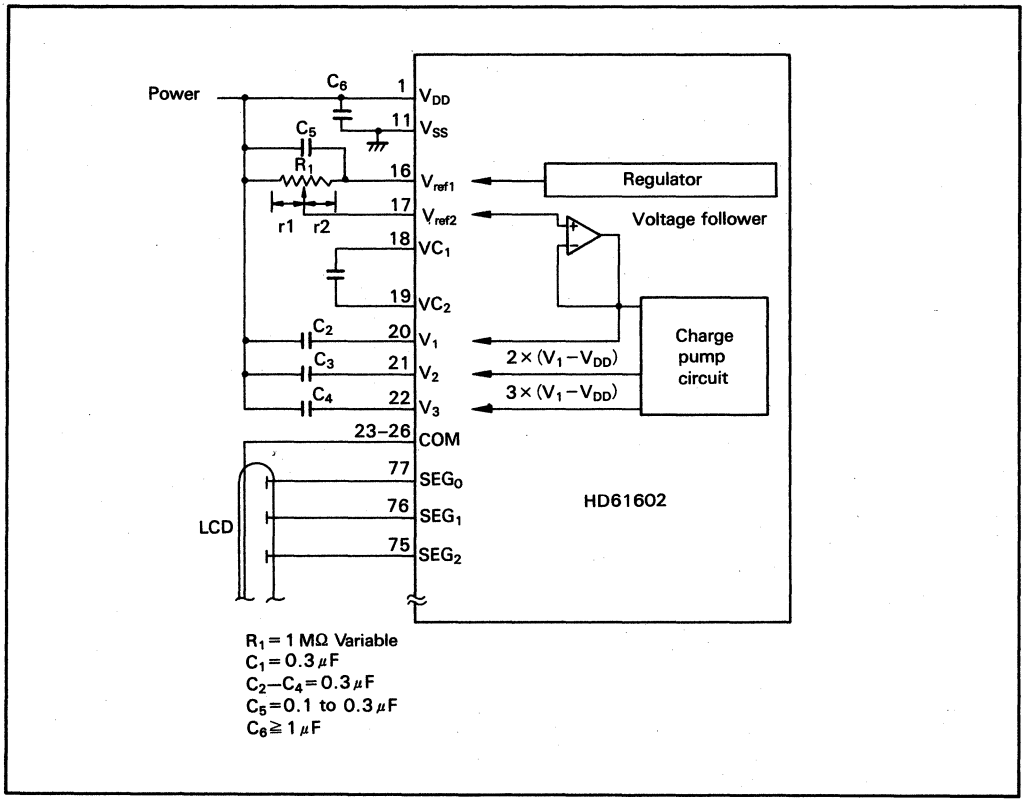


Figure 18 Example

6

When External Drive Power Supply is Used

An external power supply can be used by setting external voltage switching bits of mode setting data to 1. When a large liquid crystal display panel is used, in multichip designs, which need accurate liquid crystal drive voltage, use the external power supply. See figure 20.

R_2-R_5 is connected in series between V_{DD} and V_{SS}, and by these resistance ratio each voltage of ΔV and V_{LCD} is generated and then supplied to V_1, V_2, and V_3. C_2-C_4 are smoothing capacitors.

When regulating brightness, change the resistance value by setting R_5 variable resistance.

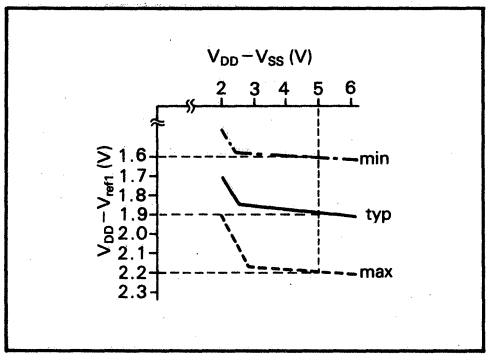
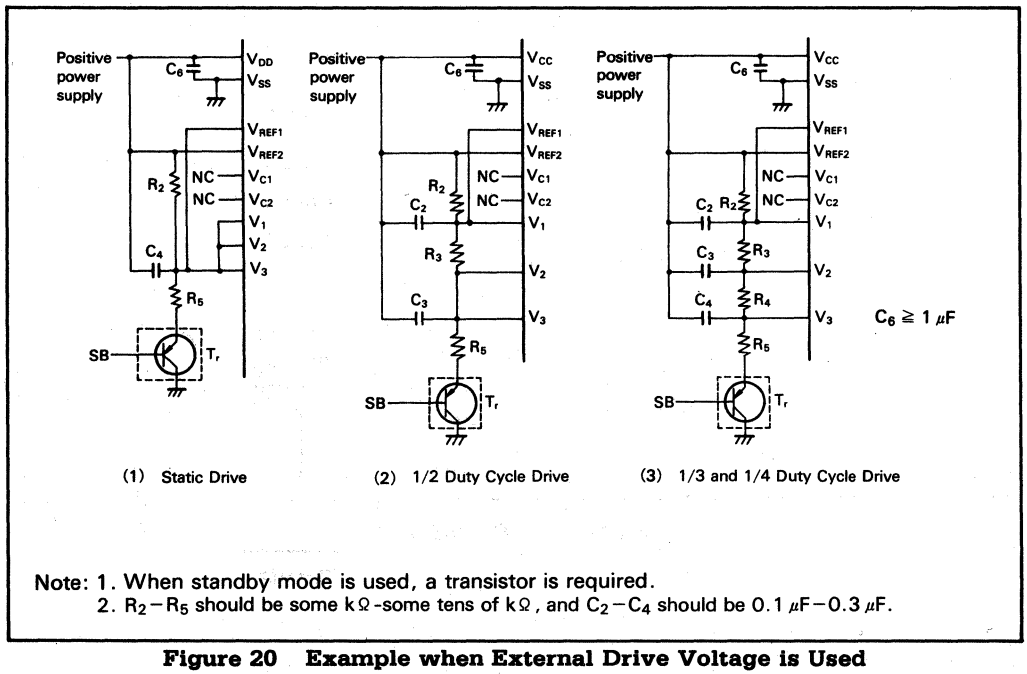


Figure 19 Voltage Characteristics between V_{DD} and V_{ref1}



Note: 1. When standby mode is used, a transistor is required.
2. R_2-R_5 should be some kΩ-some tens of kΩ, and C_2-C_4 should be 0.1 μF−0.3 μF.

Figure 20 Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61603)

As shown in figure 21, apply LCD drive voltage from the external power supply.

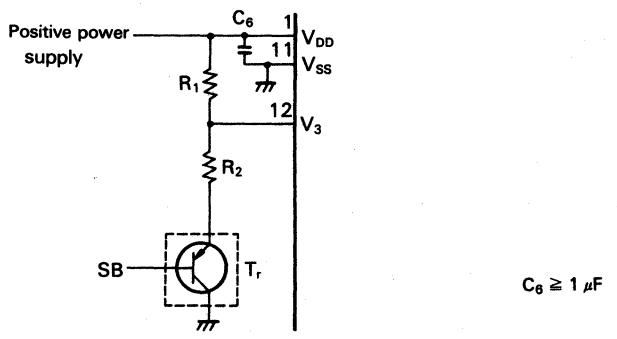
Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation circuit is used, attach an external resister R_{OSC} as shown in figure 22. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC_1 can be used for the input pin. In this case, open pin OSC_2.



Note: When standby mode is used, a transistor is required.

Figure 21 Example of Drive Voltage Generator

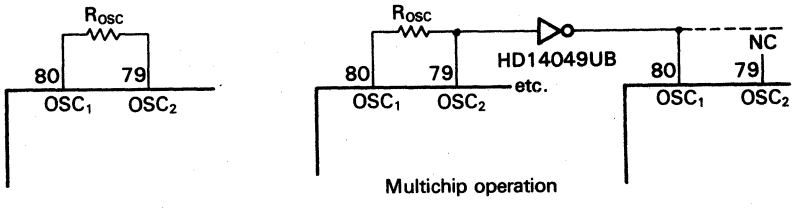


Figure 22 Example of Oscillation Circuit

6

Applications

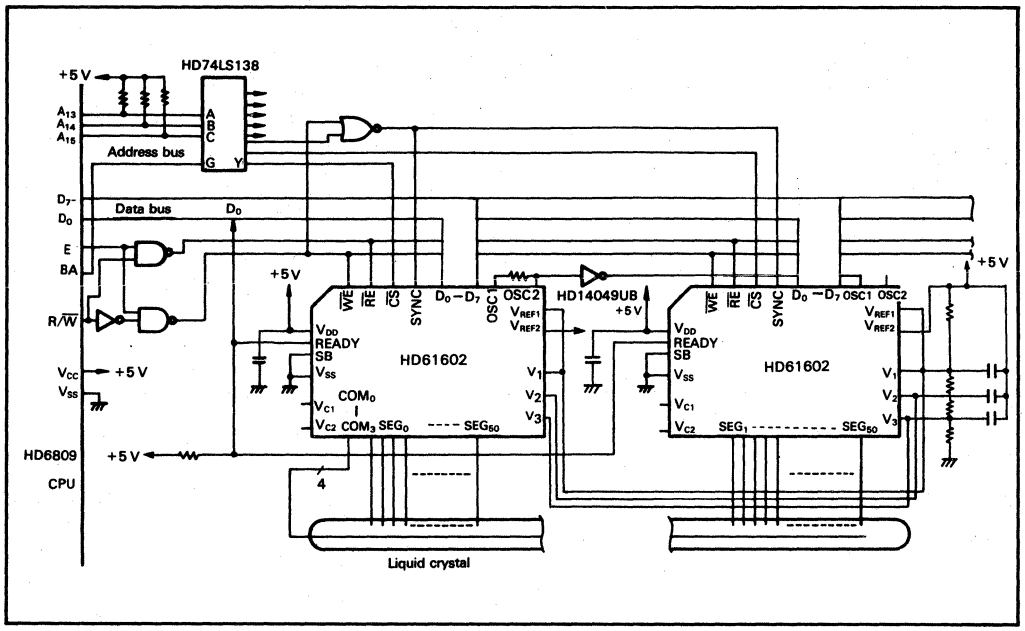


Figure 23 Example (1)

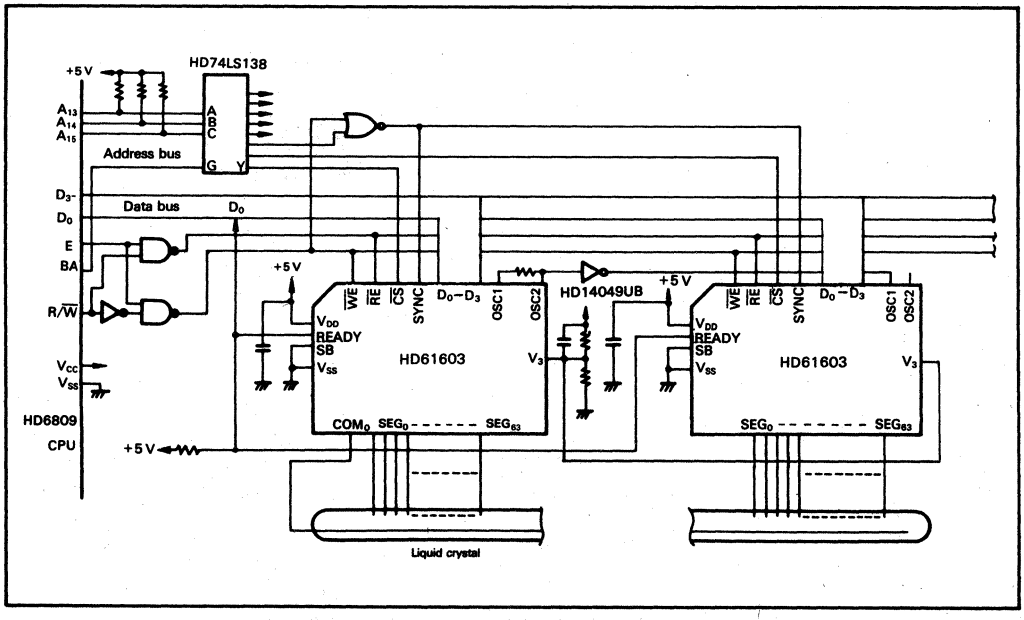


Figure 24 Example (2)

HD61604/HD61605
(Segment Type LCD Driver)

Description

The HD61604 and the HD61605 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors such as the HMCS6800 series.

Several types of liquid crystal displays can be connected to the HD61604 according to the applications because of the software-controlled liquid crystal dispay drive method.

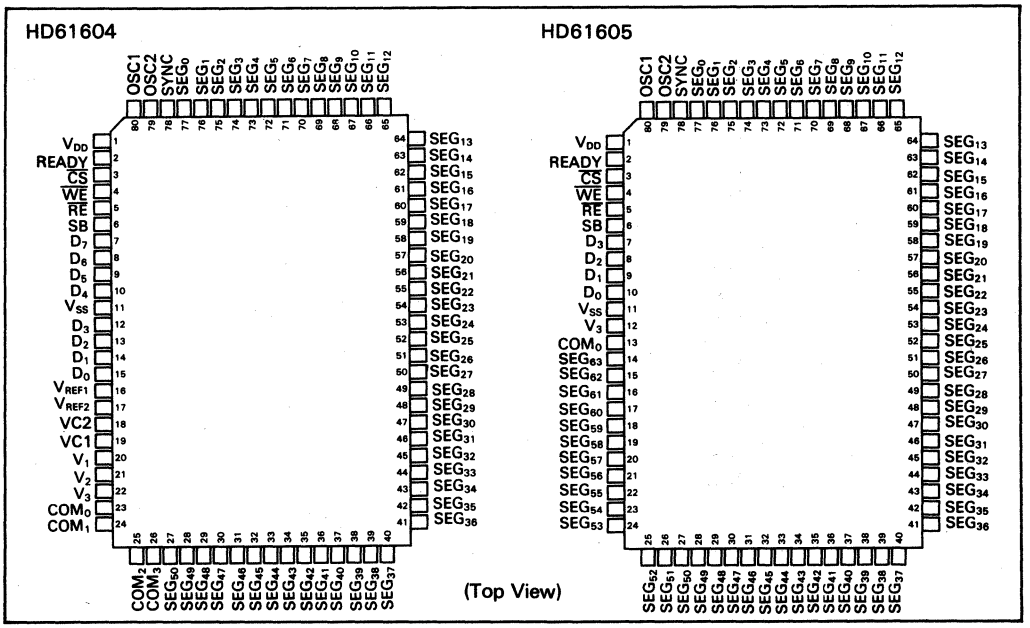
The HD61605 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Low current consumption
  —Can drive from a battery power supply (100 μA max on 5 V).
  —Standby input enables a standby operation at lower current consumption (5 μA max on 5 V).
- Versatile segment drive capacity

Type No.	Drive Method	Display Segments	Example of Use	Frame Freq (Hz) at fosc=100 kHz
HD61604	Static	51	8 segments × 6 digits + 3 marks	98
	1/2 bias 1/2 duty cycle	102	8 segments × 12 digits + 6 marks	195
	1/3 bias 1/3 duty cycle	153	9 segments × 17 digits	521
	1/4 duty cycle	204	8 segments × 25 digits + 4 marks	781
HD61605	Static	64	8 segments × 8 digits	98

Pin Arrangement



Block Diagram

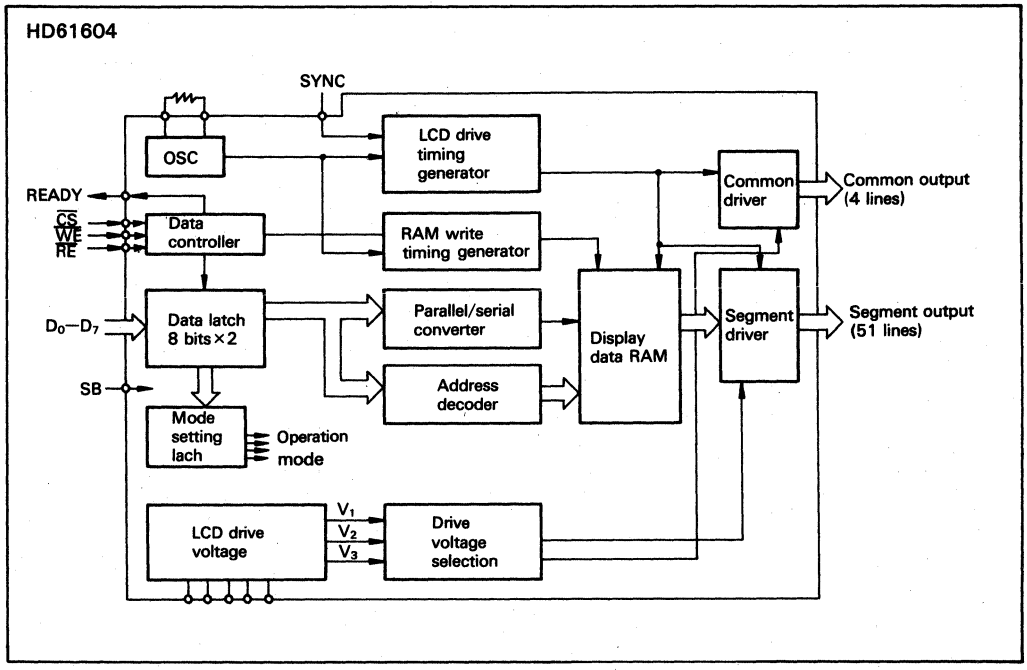


Figure 1 HD61604 Block Diagram

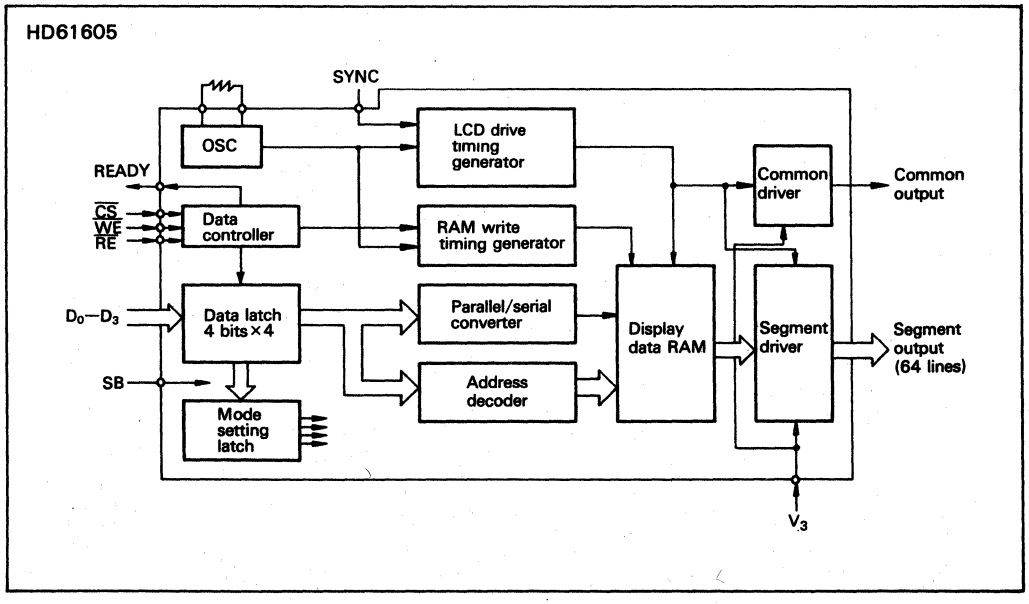


Figure 2 HD61605 Block Diagram

Pin Functions

Table 1 shows the HD61604 pin description. Table 2 shows the HD61605 pin description.

HD61604 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_7 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.

SB (Standby): High level input stops the LSI operations.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D_0-D_7 (Data Bus): Data input pin from which 8-bit × 2-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chip applications. LCD drive timing generator is reset by high input. LCD is off.

COM_0-COM_3 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{50} (Segment): LCD segment drive output.

V_1, V_2, V_3 (LCD Voltage): Power supply for LCD drive.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_{C1}, V_{C2}: Do not connect any wire.

V_{REF1}: Connect this pin to V1 pin.

V_{REF2}: Hold at V_{DD} level.

V_{DD}: Positive power supply.

V_{SS}: Negative power supply.

HD61605 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_3 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the first byte data.

SB (Standby): High level input stops the LSI operations.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D_0-D_3: Data input pin from which 4-bit × 4-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{63} (Segment): LCD segment drive output.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_3 (LCD Voltage): Power supply input for LCD drive.

Voltage between V_{DD} and V_3 is used as drive voltage.

V_{SS}: Negative power supply.

6

V_{DD}: Positive power supply.

Table 1 HD61604 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0-D_7	8	Input	MCU
SYNC	1	Input	MCU
COM_0-COM_3	4	Output	LCD
SEG_0-SEG_{50}	51	Output	LCD
V_1, V_2, V_3	3	Power supply	External R
OSC1, OSC2	2	Input, output	External R
V_{C1}, V_{C2}	2	Output	
V_{REF1}	1	Input	V_1
V_{REF2}	1	Input	V_{DD}
V_{DD}	1	Power supply	
V_{SS}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Table 2 HD61605 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0-D_3	4	Input	MCU
SYNC	1	Input	MCU
COM_0	1	Output	LCD
SEG_0-SEG_{63}	64	Output	LCD
OSC1, OSC2	2	Input, output	External R
V_3	1	Input	Power supply
V_{SS}	1	Power supply	
V_{DD}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Display RAM

HD61604 Display RAM

The HD61604 has an internal display RAM shown in figure 3. Display data is stored in the RAM, or is read according to the LCD drive timing to display on the LCD. One bit of the RAM corresponds to 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD drive modes.

Reading Data from HD61604 Display RAM

A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn pin.

A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

The following shows the correspondence between the 7-segment type LCD connection and the display RAM in each mode.

1. **Static Drive:** In static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 4).

2. **1/2 Duty Cycle Drive:** In the 1/2 duty cycle drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 5).

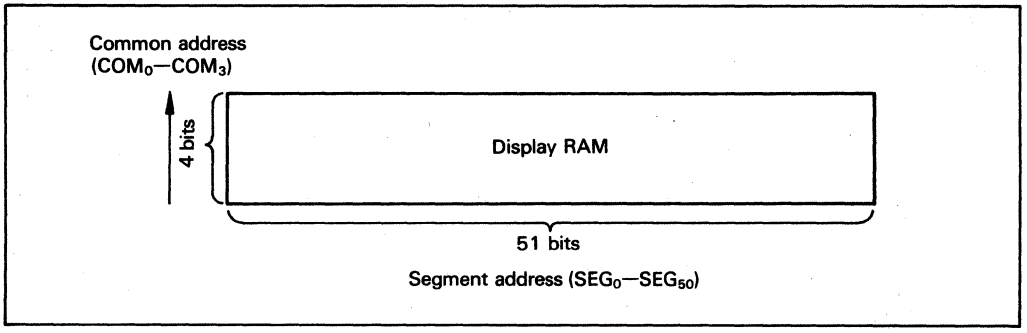


Figure 3 Display RAM (HD61604)

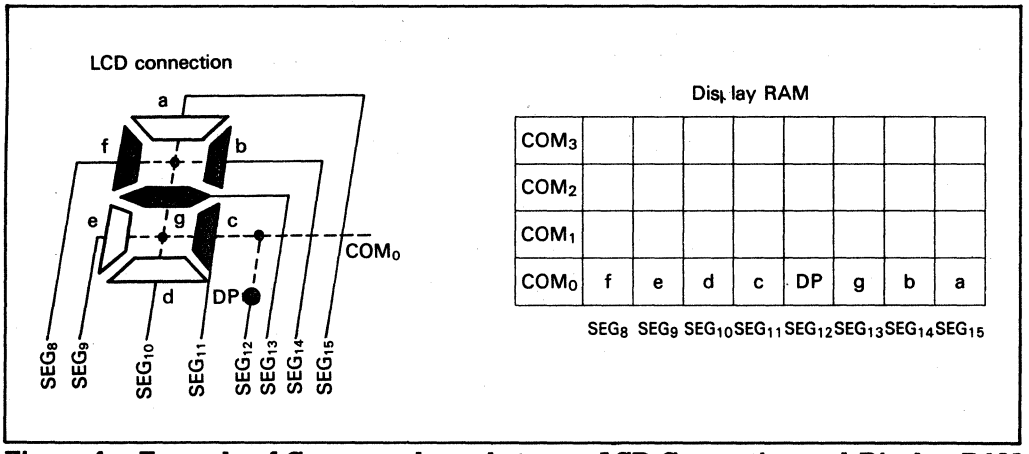


Figure 4 Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61604)

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3. **1/3 Duty Cycle Drive:** In the 1/3 duty cycle drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed. "y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "y" cycle (figure 6).

4. **1/4 Duty Cycle Drive:** In the 1/4 duty cycle drive, all the columns of COM_0 to COM_3 are displayed (figure 7).

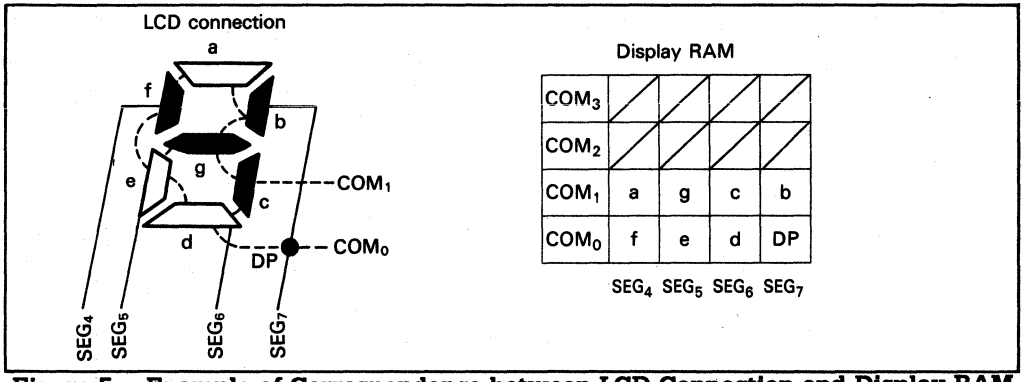

Figure 5 Example of Correspondence between LCD Connection and Display RAM (1/2 Duty Cycle, HD61604)

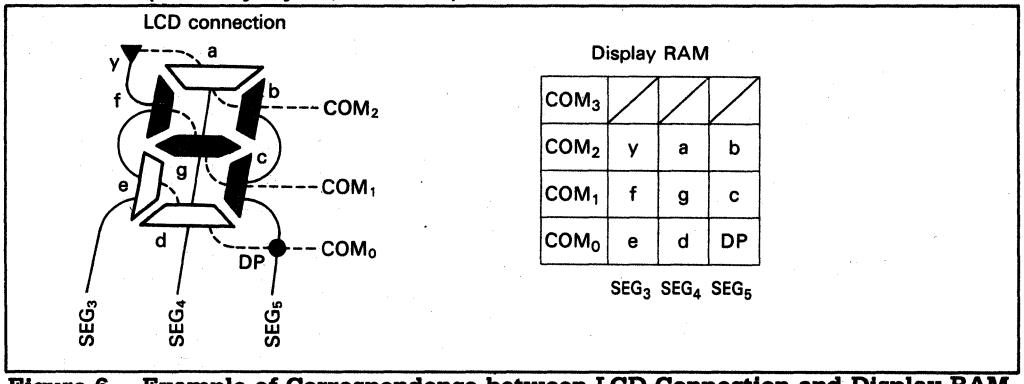

Figure 6 Example of Correspondence between LCD Connection and Display RAM (1/3 Duty Cycle, HD61604)

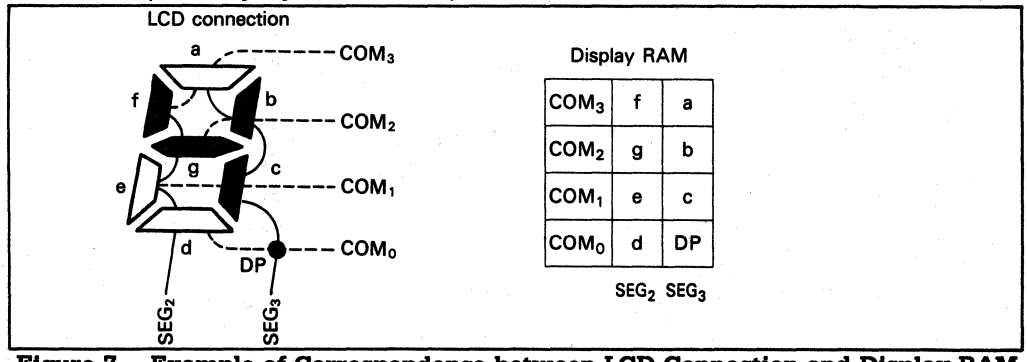

Figure 7 Example of Correspondence between LCD Connection and Display RAM (1/4 Duty Cycle, HD61604)

Writing Data into HD61604 Display RAM

Data is written into the display RAM in the following five methods:

1. **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.
2. **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.
3. **1/2 Duty Cycle Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.
4. **1/3 Duty Cycle Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.
5. **1/4 Duty Cycle Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the drive methods as described in the section of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty drive methods. The digits are allocated as shown in figure 8.

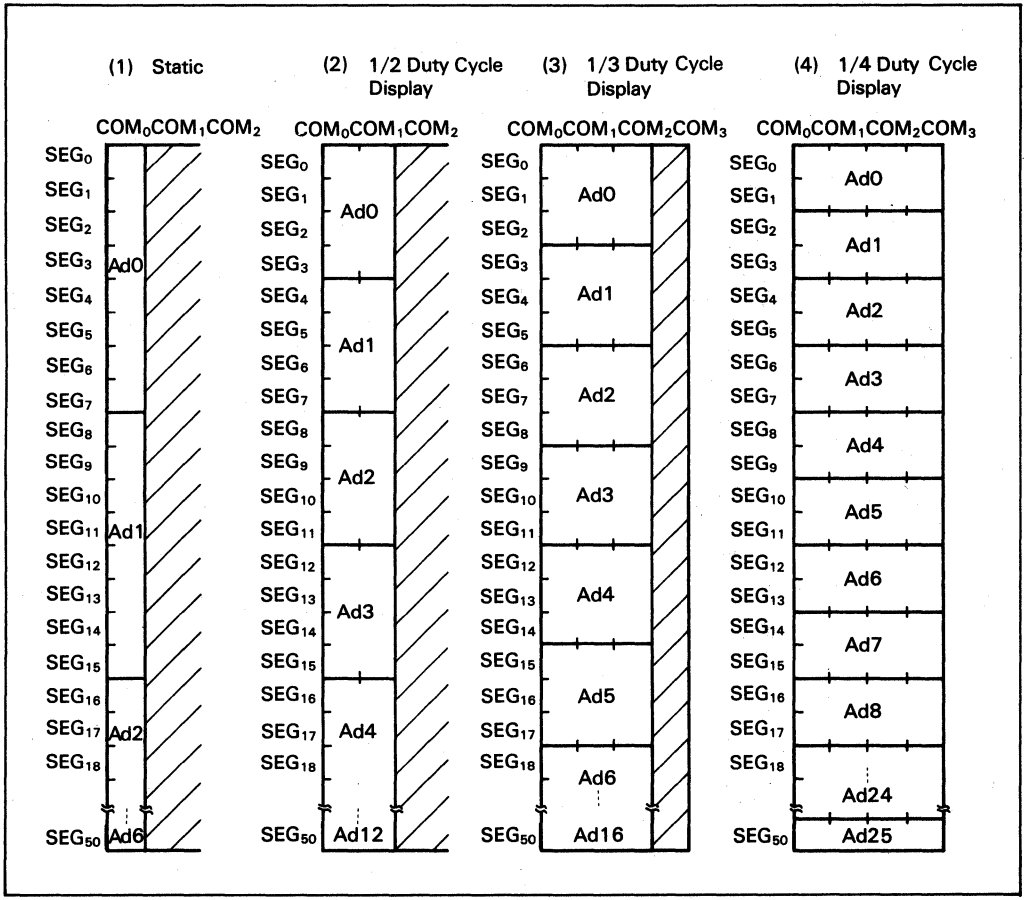

Figure 8 Allocation of Digits (HD61604)

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As the data can be transferred on a digit basis from a microprocessor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty cycle, or Ad25 of 1/4 duty cycle, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits)s and a common address (2 bits) should be specified.

HD61605 Display RAM

The HD61605 has an internal display RAM as shown in figure 10. Display data is stored in the RAM and output to the segment output pin.

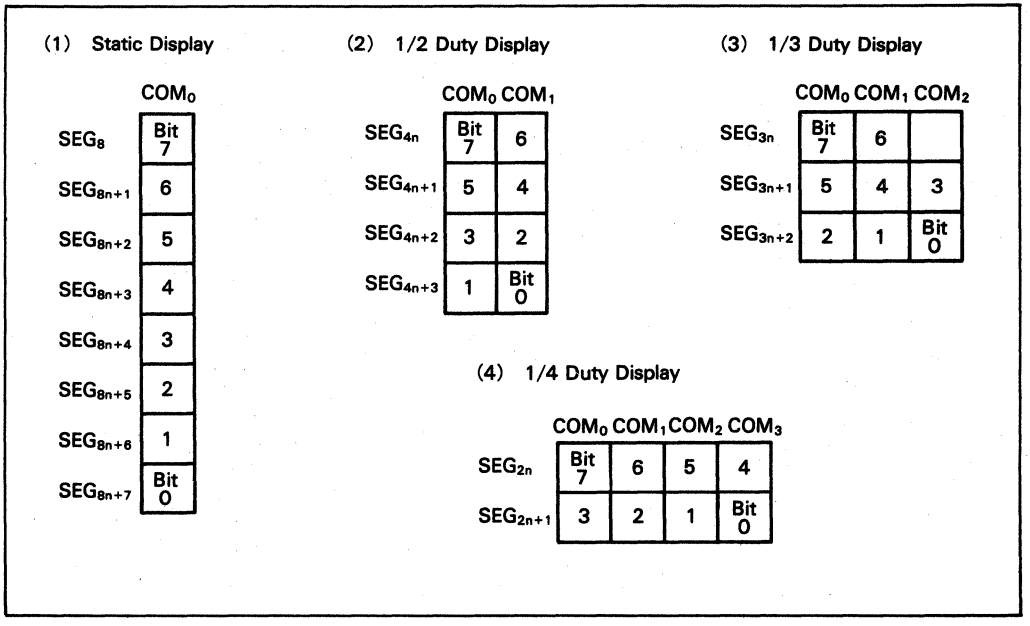

Figure 9 Bit Assignment in an Adn (HD61604)

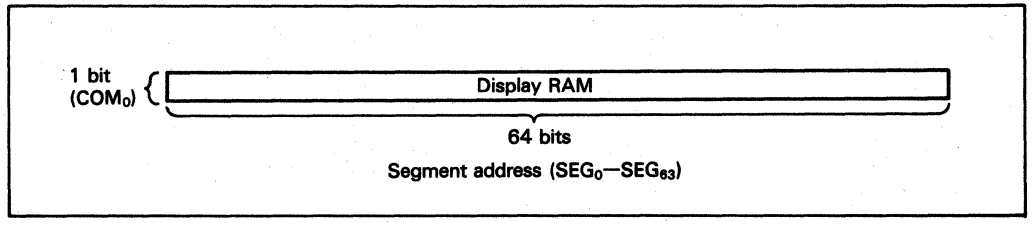

Figure 10 Display RAM (HD61605)

Reading Data from HD61605 Display RAM

Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn pin. Figure 11 shows the correspondence between the 7-segment type LCD connection and the display RAM .

Writing Data into HD61605 Display RAM

Data is written into the display RAM in the following two methods:

1. **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.
2. **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

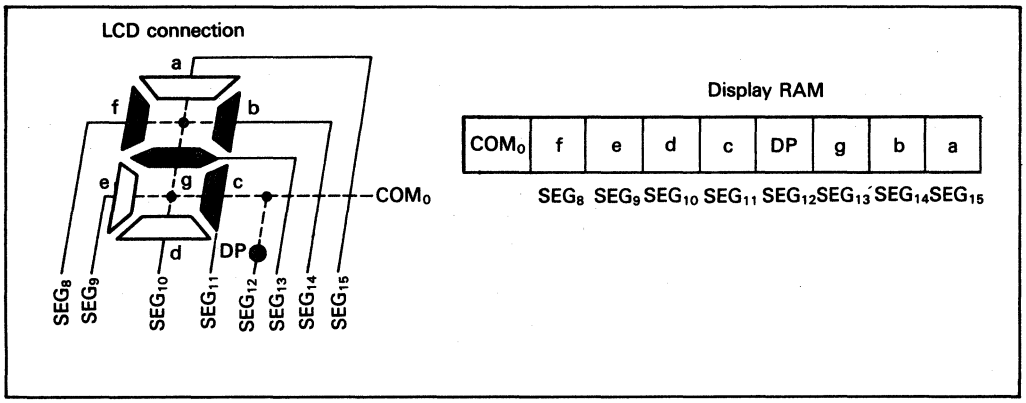

Figure 11 Example of Correspondence between LCD Connection and Display RAM (HD61605)

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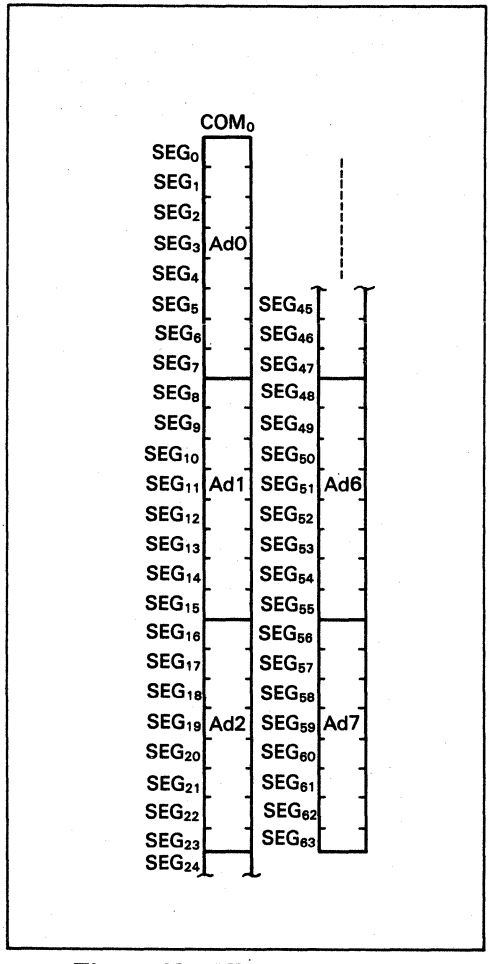

Figure 12 Allocation of Digits (HD61605)

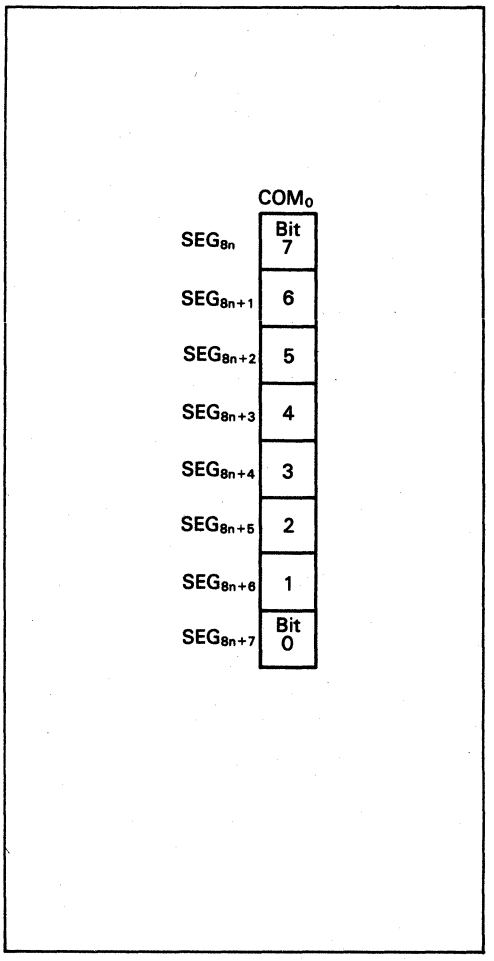

Figure 13 Bit Assignment in an Adn (HD 61605)

Operating Modes

HD61604 Operating Modes

The HD61604 has the following operating modes:

1. **LCD Drive Mode:** Determines the LCD drive method.
   - Static drive mode: LCD is driven statically.
   - 1/2 duty cycle drive mode: LCD is driven with 1/2 duty cycle and 1/2 bias.
   - 1/3 duty cycle drive mode: LCD is driven with 1/3 duty cycle and 1/3 bias.
   - 1/4 duty cycle drive mode: LCD is driven with 1/4 duty cycle and 1/3 bias.
2. **Data Display Mode:** Determines how to write display data into the data RAM.
   - Static display mode: 8-bit data is written into the display RAM according to the digit in static drive.
   - 1/2 duty cycle display mode: 8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.
   - 1/3 duty cycle display mode: 8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.
   - 1/4 duty cycle display mode: 8-bit data is written into the display RAM according to the digit in 1/4 duty cycle display drive.
3. **READY Output Mode:** Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:
   - READY is always available (figure 14).
   - READY is made available by $\overline{CS}$ and $\overline{RE}$ (figure 15).

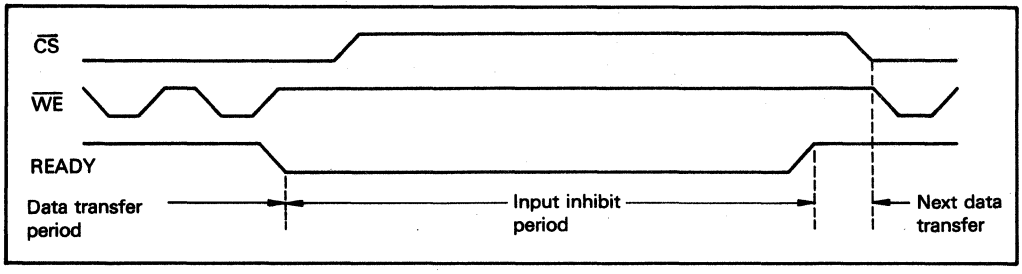

Figure 14 READY Output Timing (When It is Always Available)

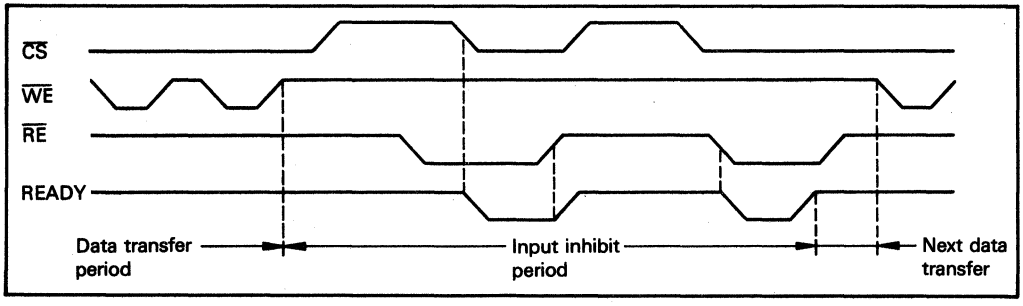

Figure 15 READY Output Timing (When It is Made Available by $\overline{CS}$ and $\overline{RE}$)

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4. **LCD Off Mode:** In this mode, the HD61604 stops driving the LCD and turns it off.

The above 4 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

HD61605 Operating Modes

The HD61605 has the following operating modes:

1. **READY Output Mode:** Determines the READY output timing.

After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 16).
- READY is made available by $\overline{CS}$ and $\overline{RE}$ (figure 17).

2. **LCD Off Mode:** In this mode, the HD61605 stops driving the LCD and turns it off.

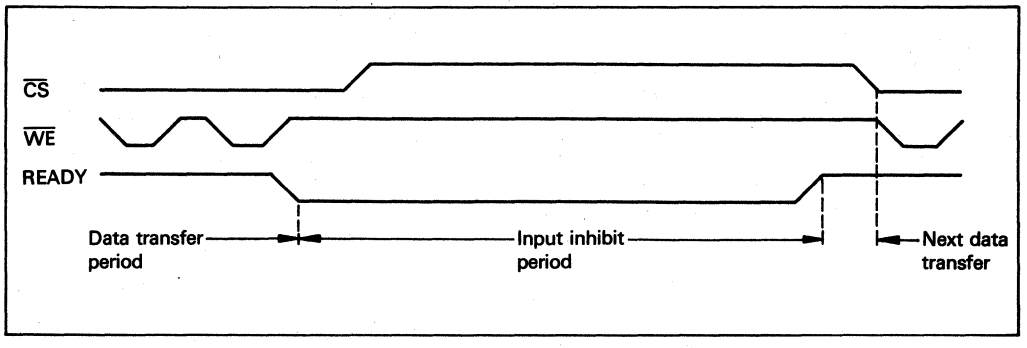


Figure 16 READY Output Timing (When It is Always Available)

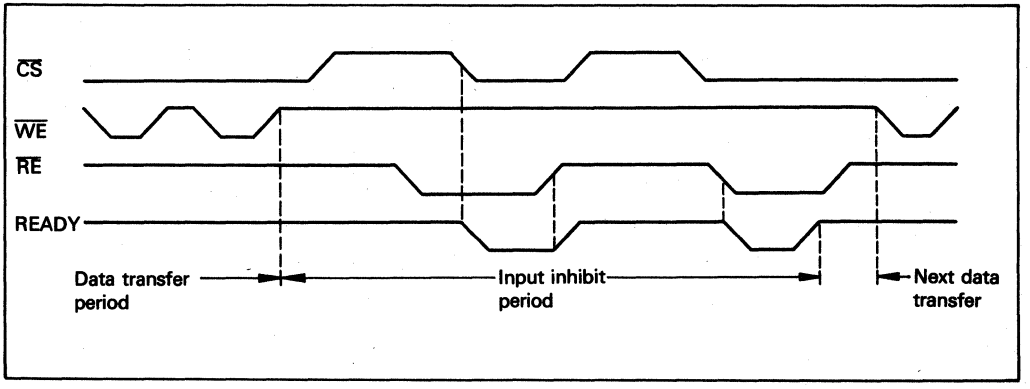


Figure 17 READY Output Timing (When It is Made Available by $\overline{CS}$ and $\overline{RE}$.)

Input Data Formats

HD61604 Input Data Formats

Input data is composed of 8 bits × 2 bytes. Input them as 2-byte data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

1. **Display Data:** Updates display on an 8-segment basis.

1st byte

7	6	5	4	3	2	1	0
0	0	×	Display address (Digit address Adn)				

2nd byte

7	6	5	4	3	2	1	0
Display data							

- Display address: Digit address Adn in accordance with display mode
- Display data: Pattern data written into the display RAM according to display mode and the address

2. **Bit Manipulation Data:** Updates display on a segment basis.

1st byte

7	6	5	4	3	2	1	0
0	1	Display data	×	×	×	COM address	

2nd byte

7	6	5	4	3	2	1	0
×	×	SEG address					

- Display data: Data written into 1 bit of the specified display RAM
- COM address: Common address of display RAM
- SEG address: Segment address of display RAM

3. **Mode Setting Data:**

1st byte

7	6	5	4	3	2	1	0
1	0	×	0	1	READY bit	Drive mode bits	

2nd byte

7	6	5	4	3	2	1	0
×	×	×	×	×	OFF/ON bit	Display mode bits	

- Display mode bits:
  00: Static display mode
  01: 1/2 duty cycle display mode
  10: 1/3 duty cycle display mode
  11: 1/4 duty cycle display mode
- OFF/ON bit:
  1: LCD off (set to 1 when SYNC is entered)
  0: LCD on
- Drive mode bits:
  00: Static drive
  01: 1/2 duty cycle drive
  10: 1/3 duty cycle drive
  11: 1/4 duty cycle drive
- READY bit:
  0: READY bus mode: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)
  1: READY port mode: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

Note: Input the same data to display mode bits and drive mode bits.

4. **1-Byte Instruction:** The first data (first byte) is ignored when the bit 6 and bit 7 in the data are 1.

1st byte

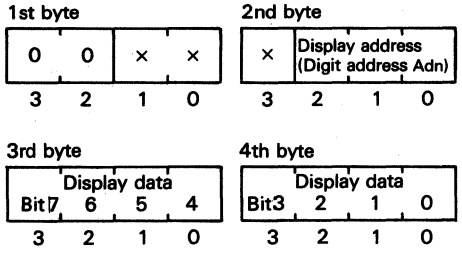
7	6	5	4	3	2	1	0
1	1	×	×	×	×	×	×

6

HD61605 Input Data Formats

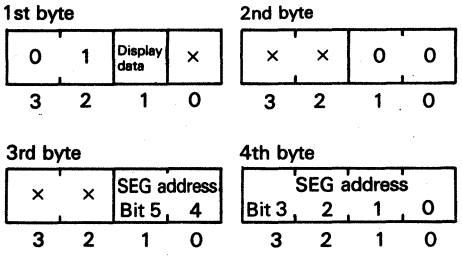
Input data is composed of 4 bits × 4 bytes. Input them as four 4-bit data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

1. **Display Data:** Updates display on an 8-segment basis.



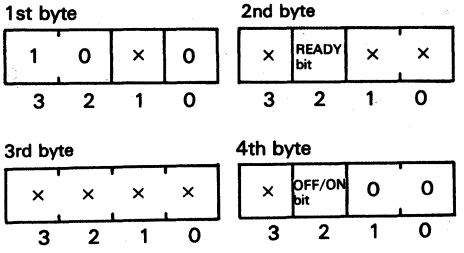
- Display address: Digit address Adn shown in figure 12.
- Display data: Pattern data written into the display RAM as shown in figure 13.

2. **Bit Manipulation Data:** Updates display on a segment basis.



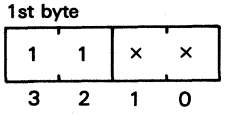
- Display data: Data written into the 1 bit of the specified display RAM.
- SEG address: Segment address of display RAM (segment output).

3. **Mode Setting Data:**



- OFF/ON bit:
  1: LCD off (It is set to 1 when SYNC is entered)
  0: LCD on
- READY bit:
  0: READY bus mode: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)
  1: READY port mode: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

4. **1-Byte Instruction:** The first data (4 bits) is ignored when the bit 3 and bit 2 in the data are 1.



How to Input Data

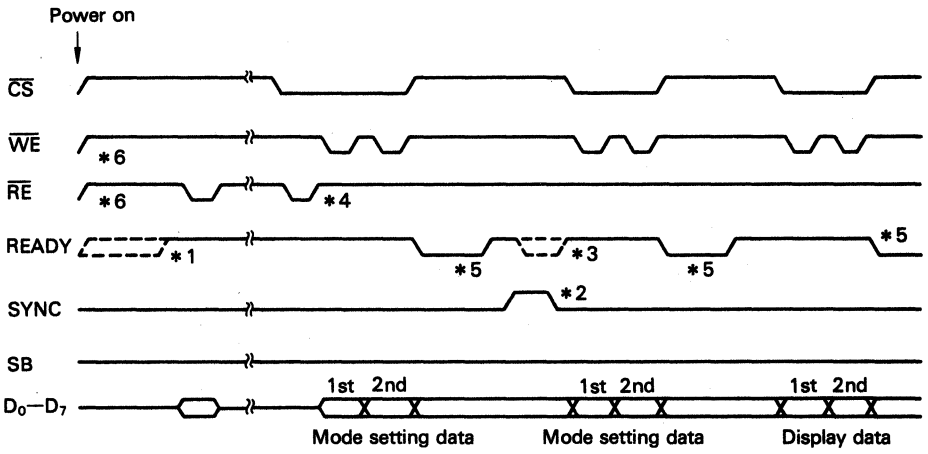
How to Input Data into HD61604

Input data is composed of 8 bits × 2 bytes. Take care that the data transfer is not interrupted because the first 8-bit data is distinguished from the second one by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
2. Input 2 or more 1-byte instruction data whose bit 7 and 6 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and figure 18.



*1: READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
*4: Reset the byte counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 18 Example of Data Transfer Sequence

6

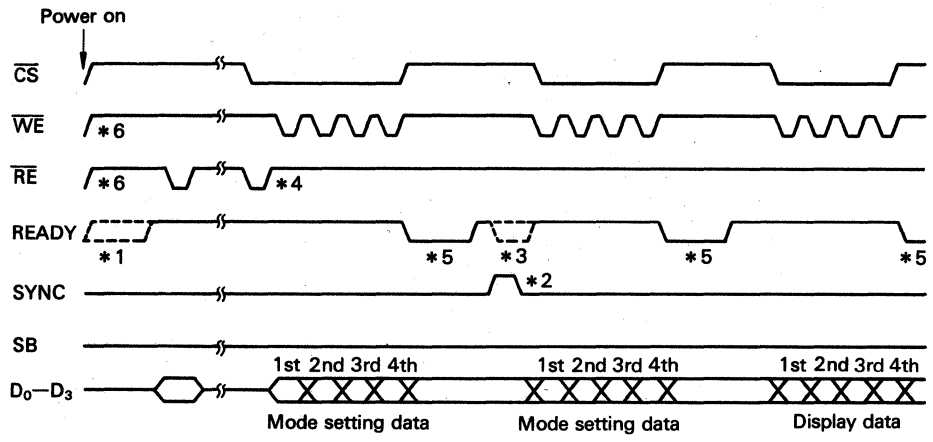
How to Input Data into HD61605

Input data is composed of 4 bits × 4 bytes. Take care that the data transfer is not interrupted because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes.)
2. Input 4 or more 1-byte instruction data (4-bit data) whose bit 3 and 2 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$ D_0 to D_3) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and figure 19.



*1: READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
*4: Reset the 4-bit data counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 19 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled untill the completion of mode setting.

There are two kinds of the READY output waveforms depending on the modes.

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in figure 20 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61604 and HD61605.

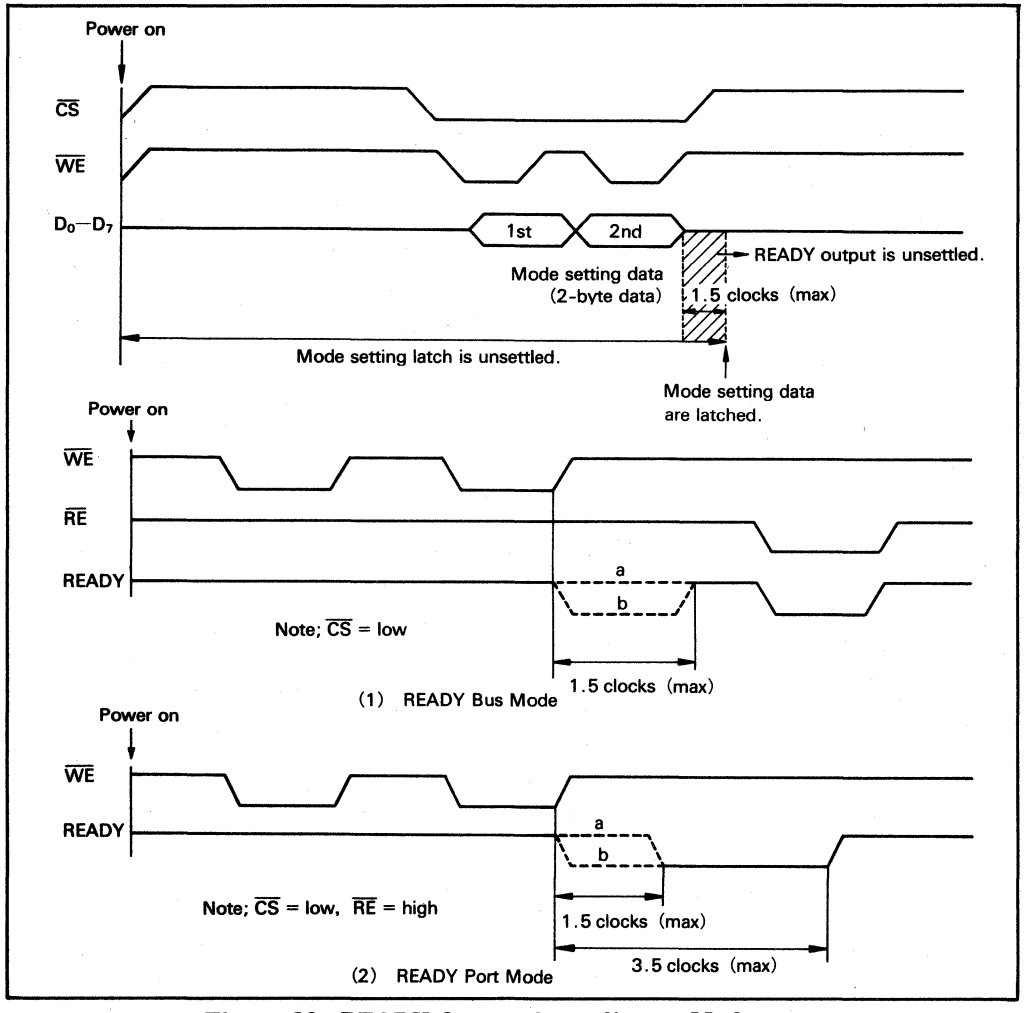


Figure 20 READY Output According to Modes

6

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multi Chip Operation

When an LCD is driven with the two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

When SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geqq$ 1 μF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61604)

What is LCD Voltage?

HD61604 drives liquid crystal display using four levels of voltages (figure 21); V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to the liquid crystal display. V_3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61604.

Connecting R2−R5 in series between V_{DD} and V_{SS} (figure 22) generates ΔV or V_{LCD} by using the resistance ratio to supply these voltage to pins V_1, V_2, V_3. C2−C4 are the smoothing capacitors. Connect a trimmer potentiometer for R5 and change its resistance value to control the contrast.

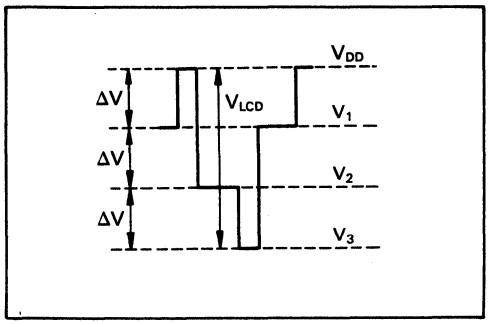
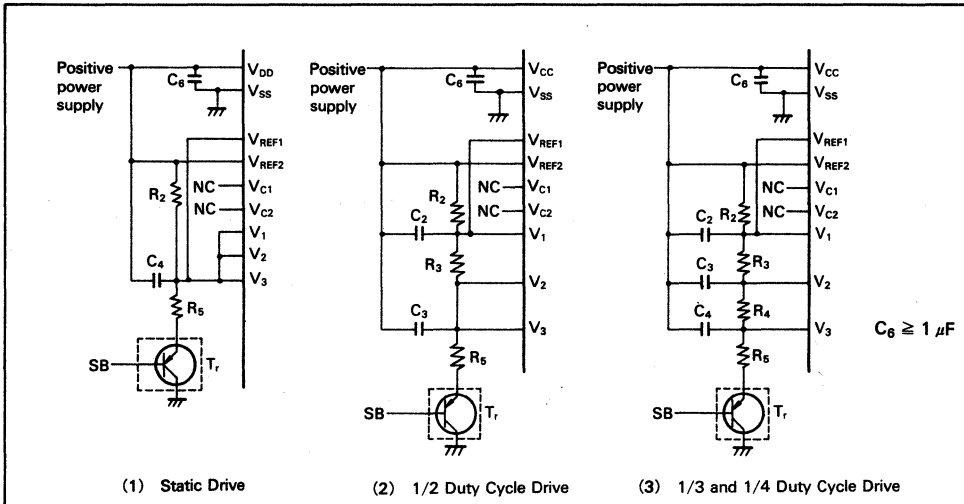


Figure 21 LCD Output Waveform and Output Levels (1/3 Duty Cycle, 1/3 Bias)



Note: 1 When standby mode is used, a transistor is required.
2 R2−R5 should be some kΩ−some tens of kΩ, and C2−C4 should be 0.1 μF−0.3 μF.

Figure 22 Example when External Drive Voltage is Used

6

Liquid Crystal Display Drive Voltage (HD61605)

As shown in figure 23, apply LCD drive voltage from the external power supply.

Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation circuit is used, attach an external resistor R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.

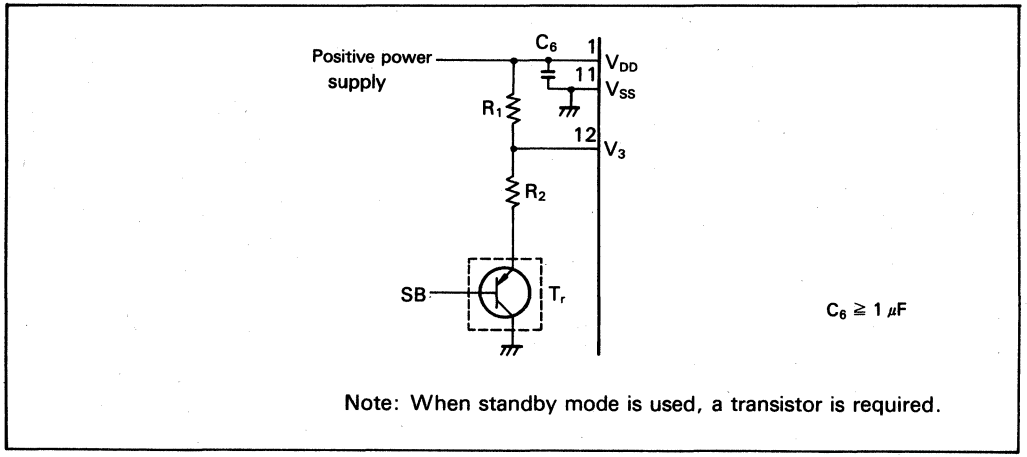


Figure 23 Example of Drive Voltage Generator

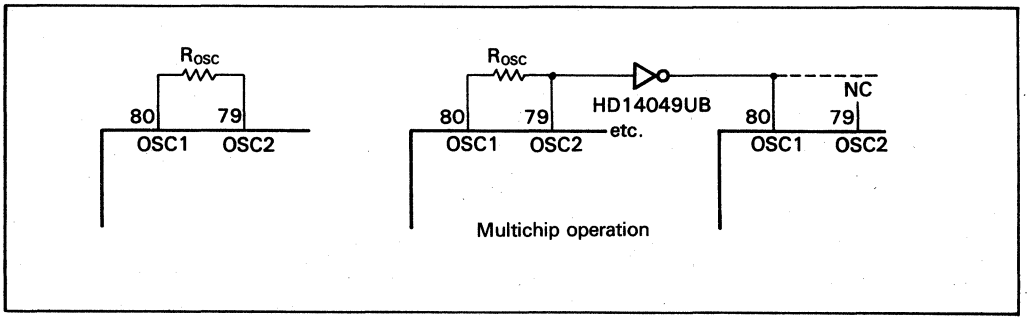


Figure 24 Example of Oscillation Circuit

Applications

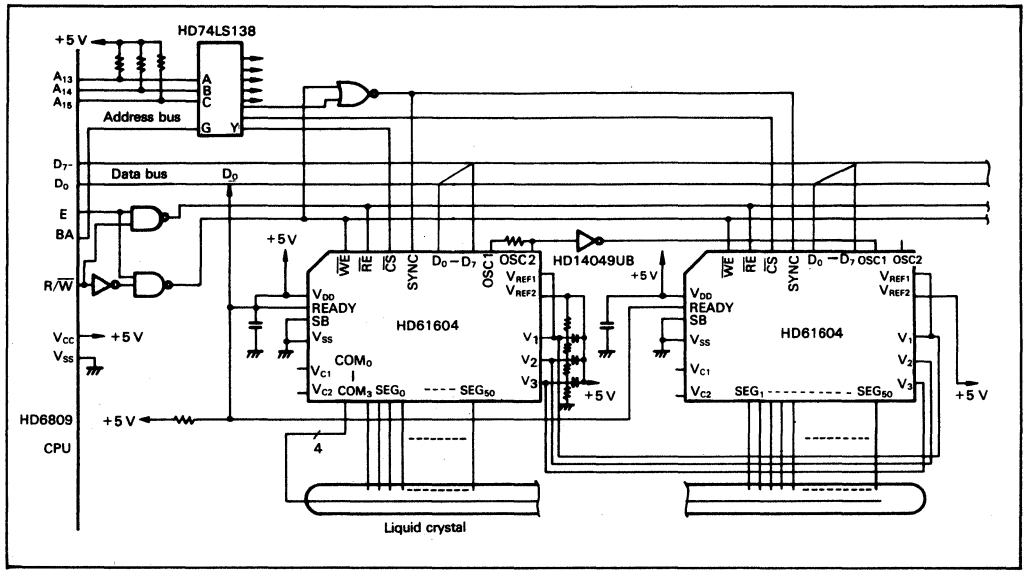


Figure 25 Example (1)

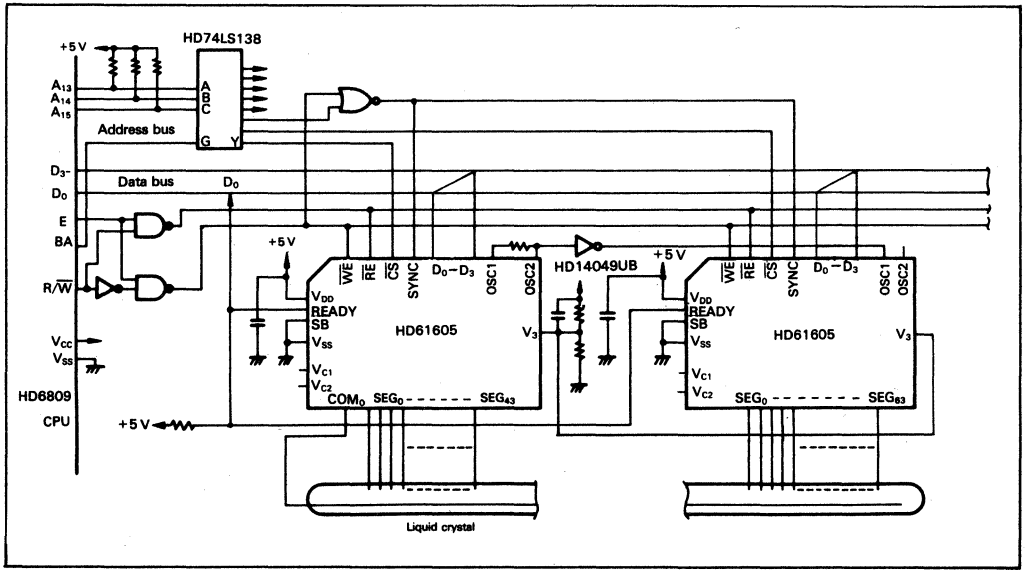


Figure 26 Example (2)

6

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V_1, V_2, V_3	–0.3 to + 7.0	V
Pin voltage*	V_T	–0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}	–20 to + 75	°C
Storage temperature	T_{stg}	–55 to + 125	°C

*Value referenced to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

Item	Symbol	Limit			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	4.5	—	5.5	V
	V_1, V_2, V_3	0	—	V_{DD}	V
Pin voltage*	V_T	0	—	V_{DD}	V
Operating temperature	T_{opr}	–20	—	+75	°C

*Value referenced to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Input high voltage	OSC1	V_{IH1}	0.8V_{DD}	–	V_{DD}	V	
	Others	V_{IH2}	2.0	–	V_{DD}	V	
Input low voltage	OSC1	V_{IL1}	0	–	0.2V_{DD}	V	
	Others	V_{IL2}	0	–	0.8	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	Pull up the pin to V_{DD}
Output low voltage	READY	V_{OL}	–	–	0.4	V	I_{OL}=0.4 mA
Input leakage current *1	Input pin	I_{IL1}	–1.0		1.0	μA	V_{IN}=0 to V_{DD}
	V_1	I_{IL2}	–20	–	20	μA	V_{IN}=V_{DD} to V_3
	V_2, V_3	I_{IL3}	–5.0	–	5.0	μA	
LCD driver voltage drop	COM_0–COM_3	V_{d1}	–	–	0.3	V	±Id=3 μA for each COM, V_3=V_{DD} to 3 V
	SEG_0–SEG_{50}	V_{d2}	–	–	0.6	V	±Id=3 μA for each SEG, V_3=V_{DD} to 3 V
Current consumption *2		I_{DD}	–	–	100	μA	During display * R_{OSC}=360 kΩ
		I_{DD}	–	–	5	μA	At standby

* Except the transfer operation of display data and bit data.

*1 V_1, V_2: applied only to HD61604.

*2 Do not connect any wire to the output pins and connect the input pins to V_{DD} or V_{SS}.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = −20°C to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Oscillation frequency	OSC2	f_{OSC}	70	100	130	kHz	R_{OSC} = 360 kΩ
External clock frequency	OSC1	f_{OSC}	70	100	130	kHz	
External clock duty	OSC1	Duty	40	50	60	%	
I/O signal timing		t_S	400	—	—	ns	
		t_H	10	—	—	ns	
		t_{WH}	300	—	—	ns	
		t_{WL}	400	—	—	ns	
		t_{WR}	400	—	—	ns	
		t_{DL}	—	—	1.0	µs	Figure 31
		t_{EN}	400	—	—	ns	
		t_{OP1}	9.5	—	10.5	Clock	For display data transfer
		t_{OP2}	2.5	—	3.5	Clock	For bit and mode data transfer
Input signal rise and fall time		t_r, t_f	—	—	25	ns	

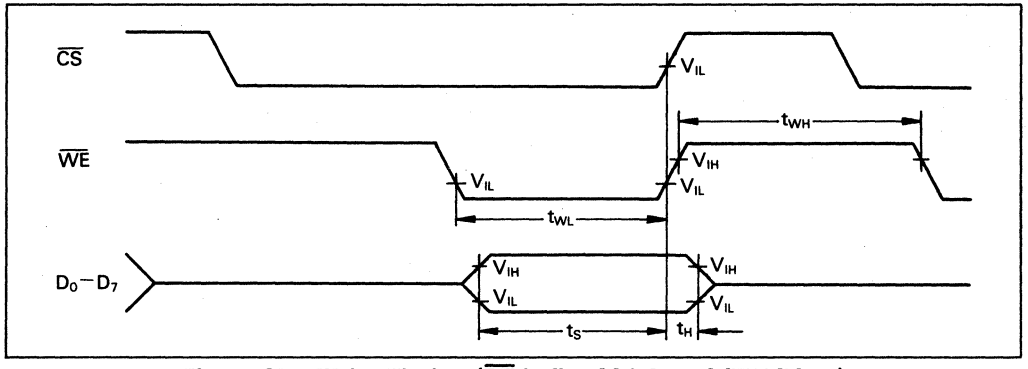


Figure 27 Write Timing ($\overline{RE}$ is fixed high and SYNC low)

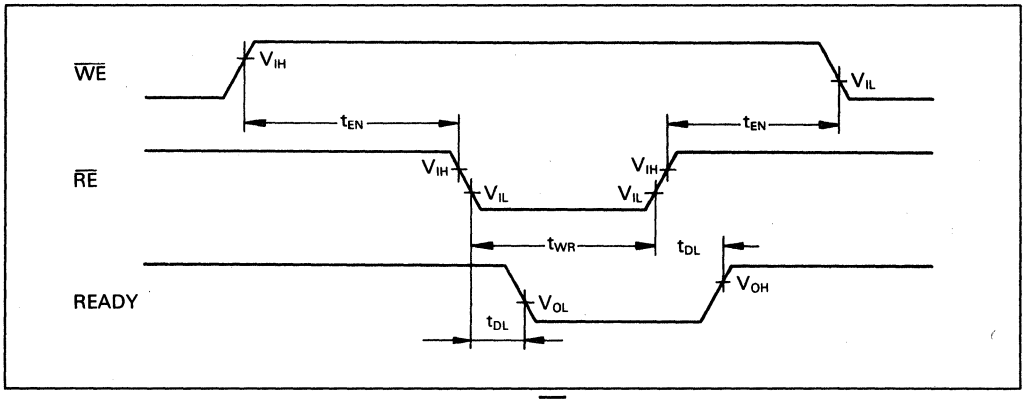


Figure 28 Reset/Read Timing ($\overline{CS}$ and SYNC are fixed low)

6

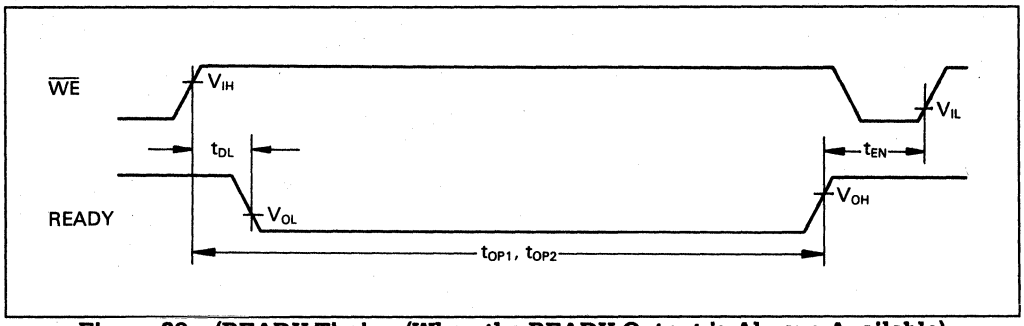


Figure 29 (READY Timing (When the READY Output is Always Available)

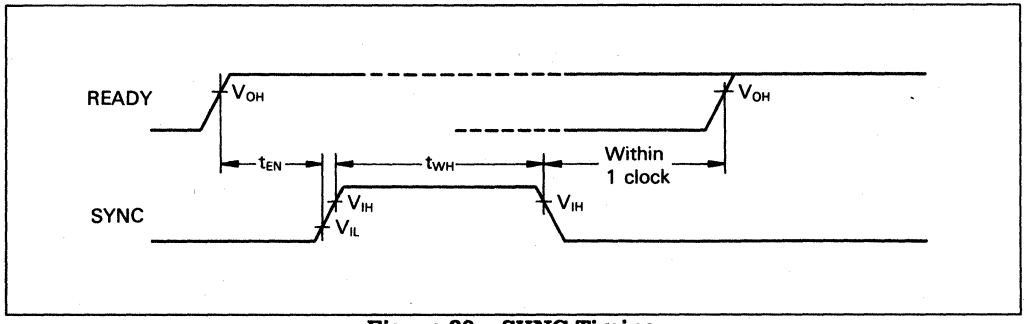


Figure 30 SYNC Timing

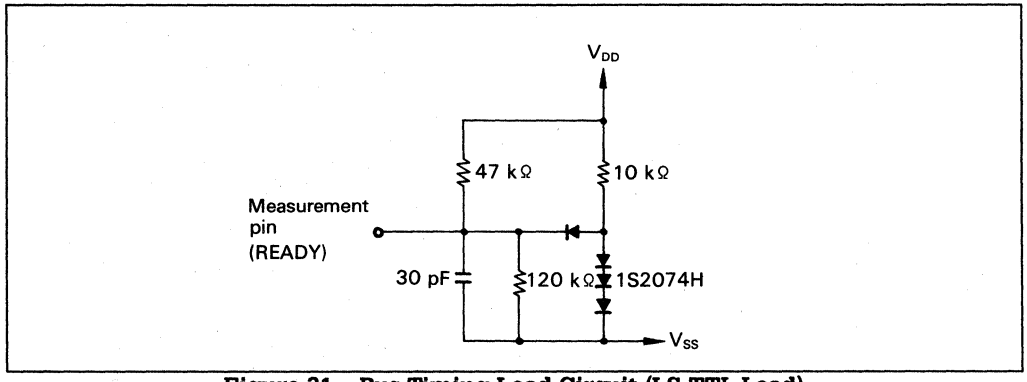


Figure 31 Bus Timing Load Circuit (LS-TTL Load)

LCD CONTROLLER/DRIVER LSI DATA BOOK

Section Seven

Special Application Drivers

7

HITACHI

HD66300T
(Horizontal Driver for TFT-Type LCD Color TV)

The HD66300T is a horizontal driver used for TFT-type (Thin Film Transistor) LCD color TVs. Specifically, it drives the drain bus signals of a TFT-type LCD panel.

The HD66300T receives as input three video signals R, G, B, and their inverted signals $\overline{R}$, $\overline{G}$ and $\overline{B}$. Internal sample and hold circuitry then samples and holds these signals before outputting them via voltage followers to drive a TFT-type LCD panel.

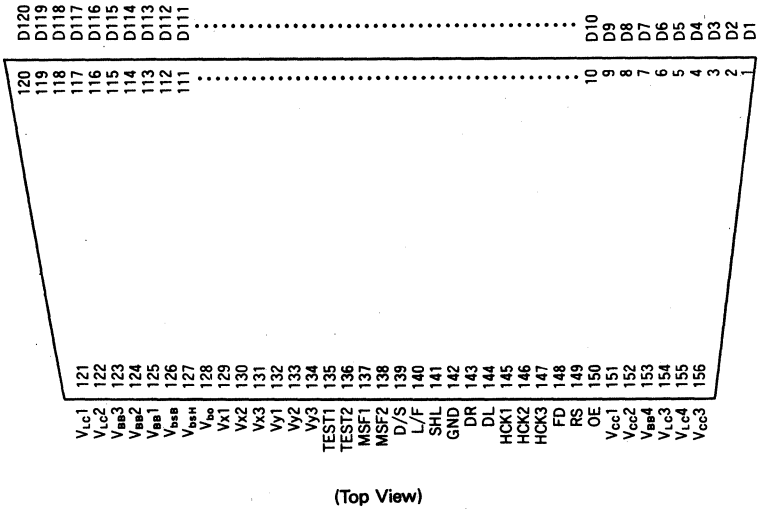
The HD66300T can drive LCD panels from 480 x 240 pixels middle-resolution up to 720 x 480 pixels high-resolution. It has 120 LCD drive outputs and enables design of a compact LCD TV due to TCP (Tape Carrier Package) technology.

Available in TCP packaging only.
Recommended for high volume applications only.

Features

- LCD drive outputs: 120
- Internal sample and hold circuits: 480 (4 circuits per output)
- Support of single-rate sequential drive mode and double-rate sequential drive mode
- Support of various types of color filter arrangements through an internal color sequence controller
- Vertical pixels: 240 (middle-resolution) or 480 (high-resolution)
- Horizontal pixels: 480 to 720
- Support of monodirectional connection mode and interleaved connection mode through a bidirectional shift register
- Dynamic range: 15 V_{PP}
- Package: 156-pin TCP
- Power supply: +5 V and –15 V
- CMOS process

Pin Arrangement



(Top View)

Note: This does not apply to TCP dimensions.

7

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Connected to	Functions (Refer to)
D1 - D120	120	O	LCD panel	1.
HCK1, HCK2, HCK3	3	I	Controller	2.
DL, DR	2	I/O	Controller or next HD66300T	3.
FD	1	I	Controller	4.
RS	1	I	GND	5.
OE	1	I	Controller	6.
SHL	1	I	V_{CC} or GND	7.
D/S	1	I	V_{CC} or GND	8.
L/F	1	I	V_{CC} or GND	9.
MSF1, MSF2	2	I	V_{CC} or GND	10.
TEST1, TEST2	2	I	GND	11.
Vx1, Vx2, Vx3, Vy1, Vy2, Vy3	6	I	Inverter	12.
V_{bo}	1	I	Power source	13.
V_{bsB}, V_{bsH}	2	I	Power source	14.
$V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$	4	—	Power source	15.
$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	3	—	Power source	16.
GND	1	—	Power source	17.
$V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$	4	—	Power source	18.

Pin Functions

1. D1 - D120: These pins output LCD drive signals.

2. HCK1, HCK2, HCK3: These pins input three-phase clock pulses, which determine the signal sampling timing for sample and hold circuits.

3. DL, DR: These pins input or output data into or from the internal bidirectional shift register. The state of pin SHL determines whether these pins input or output data.

SHL	DL	DR
V_{CC}	Output	Input
GND	Input	Output

4. FD: This pin inputs the field determination signal, which allows the sample and hold circuitry and the shift matrix circuit to operate synchronously with TV signals, at its rising and falling edge.

FD = high: First field

FD = low: Second field

When a non-interlace signal is applied, it must be inverted every field.

When an interlace signal is applied in double-rate sequential drive mode with per-line inversion (mode 1, 2, 3), the signal must be set high in both fields. The signal must be set low, however, in each field's horizontal retrace period.

5. RS: This pin inputs a test signal and should be connected to pin GND.

6. OE: This pin inputs the signal which controls the controller of the shift matrix circuit; it changes the selection of a sample and hold circuit and the shift matrix (combination of color data), at its rising edge. It also switches the bias current of the output buffer, as shown in the following table.

OE	Bias Current of Output Buffer
High	Large current (determined by VbsB)
Low	Small current (determined by VbsH)

7. SHL: This pin selects the shift direction of the shift register.

SHL	Shift Direction
High	DL ← DR
Low	DL → DR

8. D/S: This pin selects the LCD drive mode.

D/S	Mode
High	Double-rate sequential drive mode
Low	Single-rate sequential drive mode

9. L/F: This pin selects the inversion mode of LCD drive signals.

L/F	Mode
High	Per-line inversion mode
Low	Per-field inversion mode

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10. MSF1, MSF2: These pins select the function of the shift matrix circuit; they should be set according to both the type of color filter arrangement on a TFT-type LCD panel and the drive mode.

Filter Arrangement	Drive Mode	MSF1	MSF2
Diagonal mosaic	Single-rate	GND	V_{CC}/GND
pattern	Double-rate	GND	V_{CC}/GND
Vertical stripe	Single-rate	V_{CC}	V_{CC}
pattern	Double-rate	V_{CC}	V_{CC}
Unicolor triangular	Single-rate	V_{CC}	V_{CC}
pattern	Double-rate	V_{CC}	GND
Bicolor triangular	Single-rate	V_{CC}	GND
pattern	Double-rate	V_{CC}	GND

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

11. TEST1, TEST2: These pins input test signals and should be connected to pin GND.

12. Vx1, Vx2, Vx3, Vy1, Vy2, Vy3: Video signals are applied to these pins; in general, positive video signals are connected to pins Vxi and negative video signals to pins Vyi.

13. V_{bo}: Bias voltage is applied to this pin for the differential amplifier in the sample and hold circuitry.

14. V_{bsB}, V_{bsH}: Bias voltage is applied to this pin for the two power sources of the output buffer.
VbsB: The voltage for driving a capacitive load
VbsH: The voltage for holding the output voltage

15. $V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$: +5 V LCD drive voltage is applied to these pins.

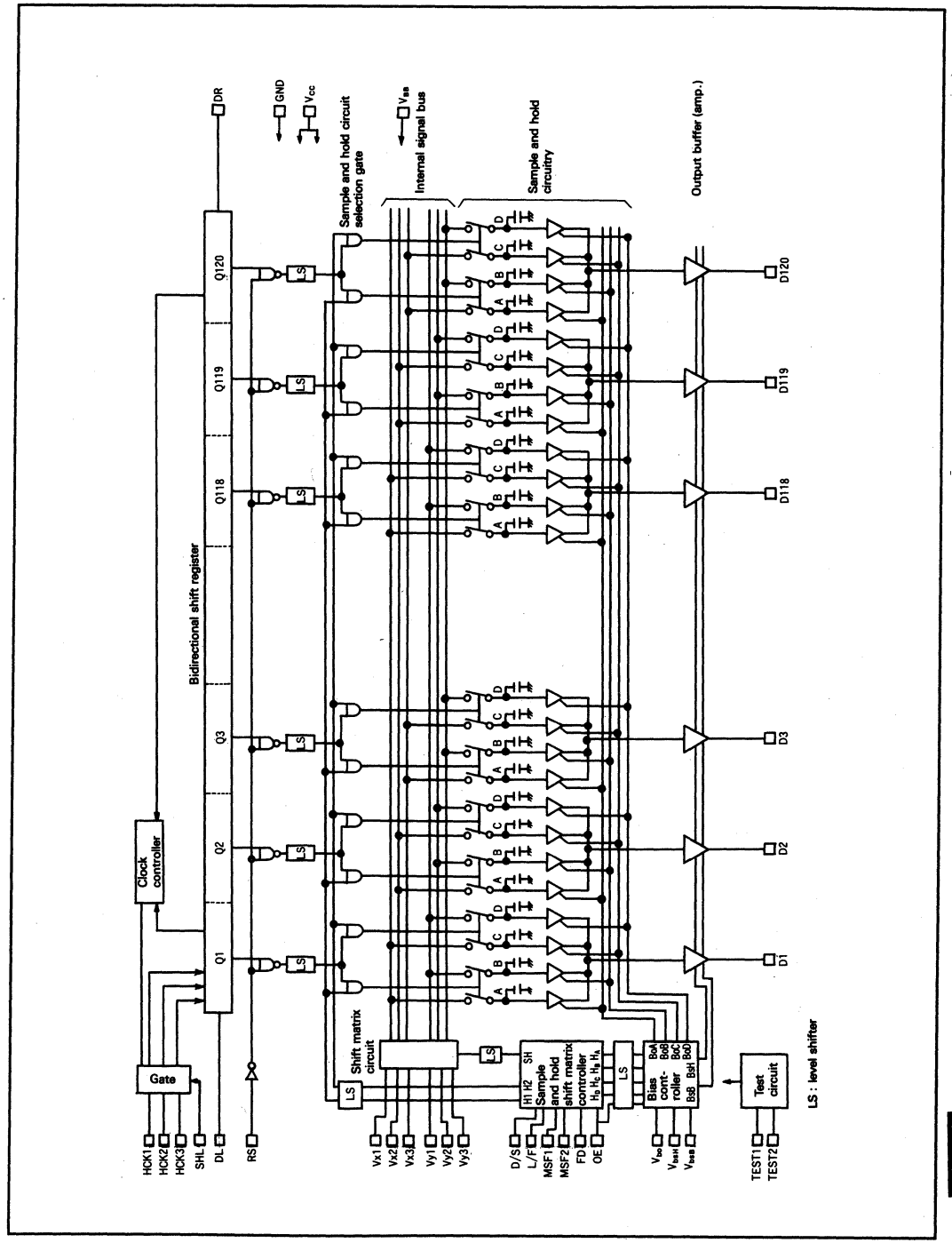
16. $V_{CC}1$, $V_{CC}2$, $V_{CC}3$, $V_{CC}4$: +5 V is applied to these pins for the logic and the analog units.

17. GND: 0 V is applied to this pin for the logic unit.

18. $V_{BB}1$, $V_{BB}2$: –15 V is applied to these pins for the LCD drive unit.

19. $V_{BB}3$, $V_{BB}4$: –15 V is applied to these pins for the LCD drive unit.

Internal Block Diagram



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Block Functions

Shift Register: The shift register generates the sampling timing for video signals. It is driven by three-phase clocks HCK1, HCK2, and HCK3, whose phases are different from each other by 120°; each clock determines the sampling timing for one color signal so that three clocks support the three color signals R, G, and B. The shift direction of this register can be changed.

Level Shifter: The level shifter changes 5-V signals into 20-V signals.

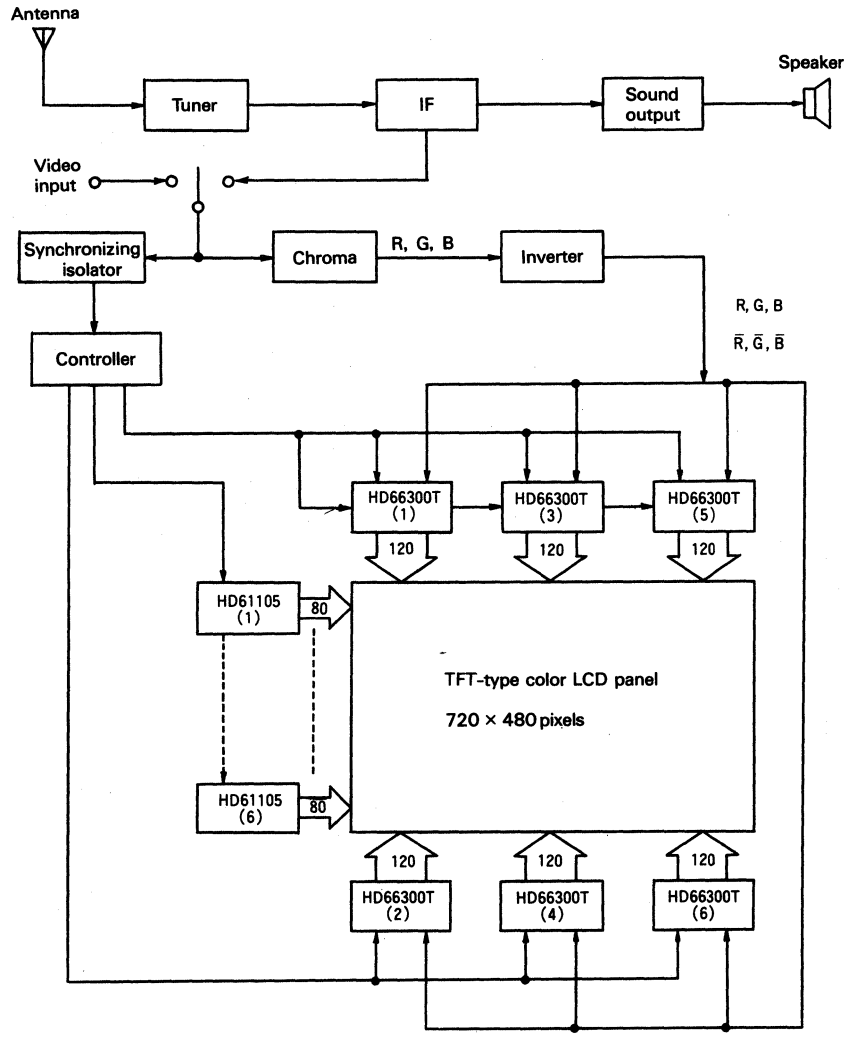
Sample and Hold Circuitry: In double-rate sequential drive mode, two sample and hold circuits are selected to sample video signals during one horizontal scanning period out of the four circuits attached to one LCD drive signal. One of the two selected circuits is read out in the first half of the following horizontal scanning period, and the other selected circuit is read out in the second half. While the two circuits are being read out, the other two circuits sample signals and are alternately read out in the same procedure mentioned above.

In single-rate sequential drive mode, one sample and hold circuit samples a signal during one horizontal scanning period, and is read out in the following horizontal scanning period. While it is being read out, one circuit out of the other three samples a signal.

Shift Matrix Circuit: The shift matrix circuit, a color sequence controller, changes over the sampled video signal every horizontal scanning period.

Output Buffer: The output buffer consists of a source follower circuit and can change the through-rate of an output signal by changing the external bias voltage.

System Block Configuration Example



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Example of HD66300T Connection to LCD Panel

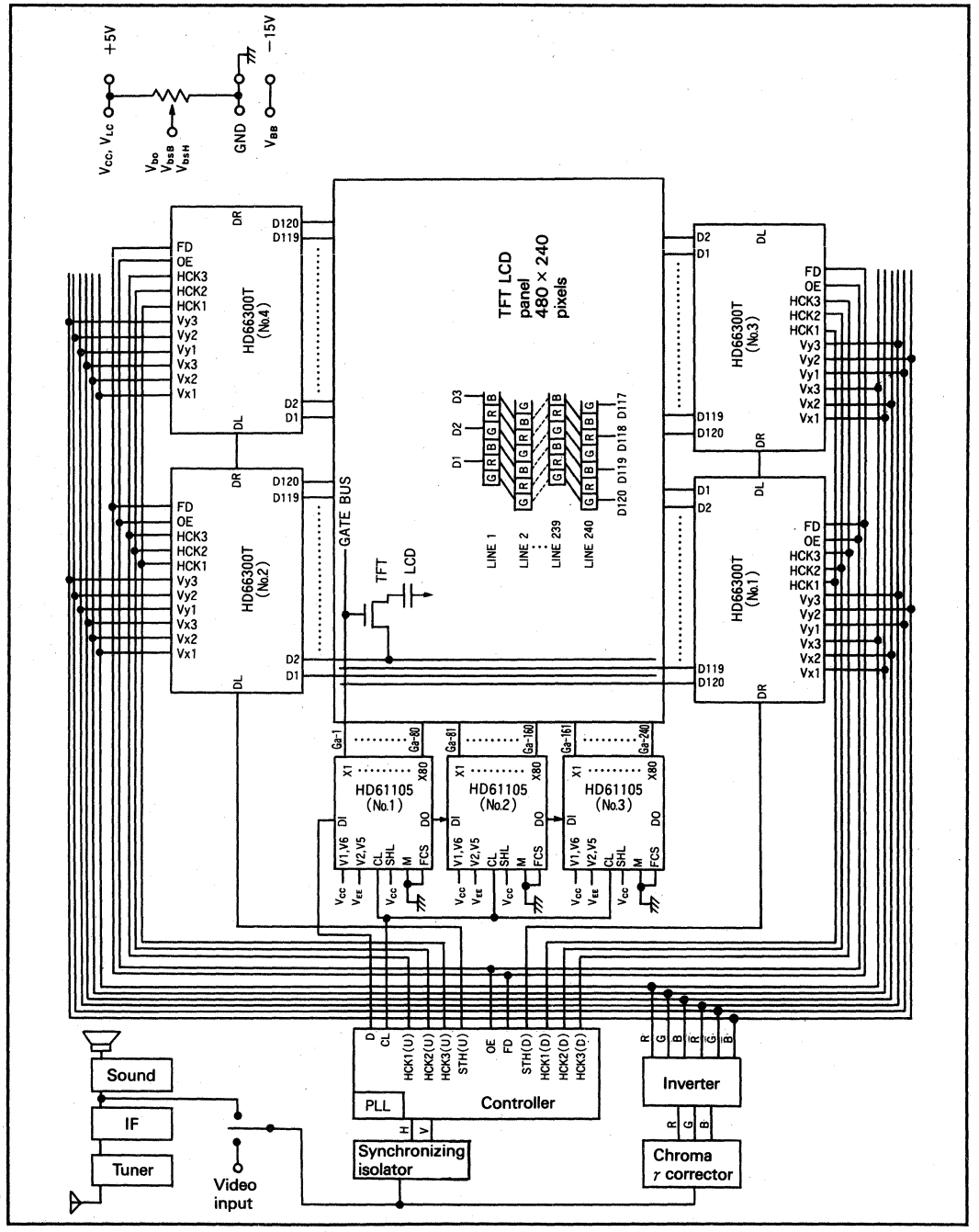
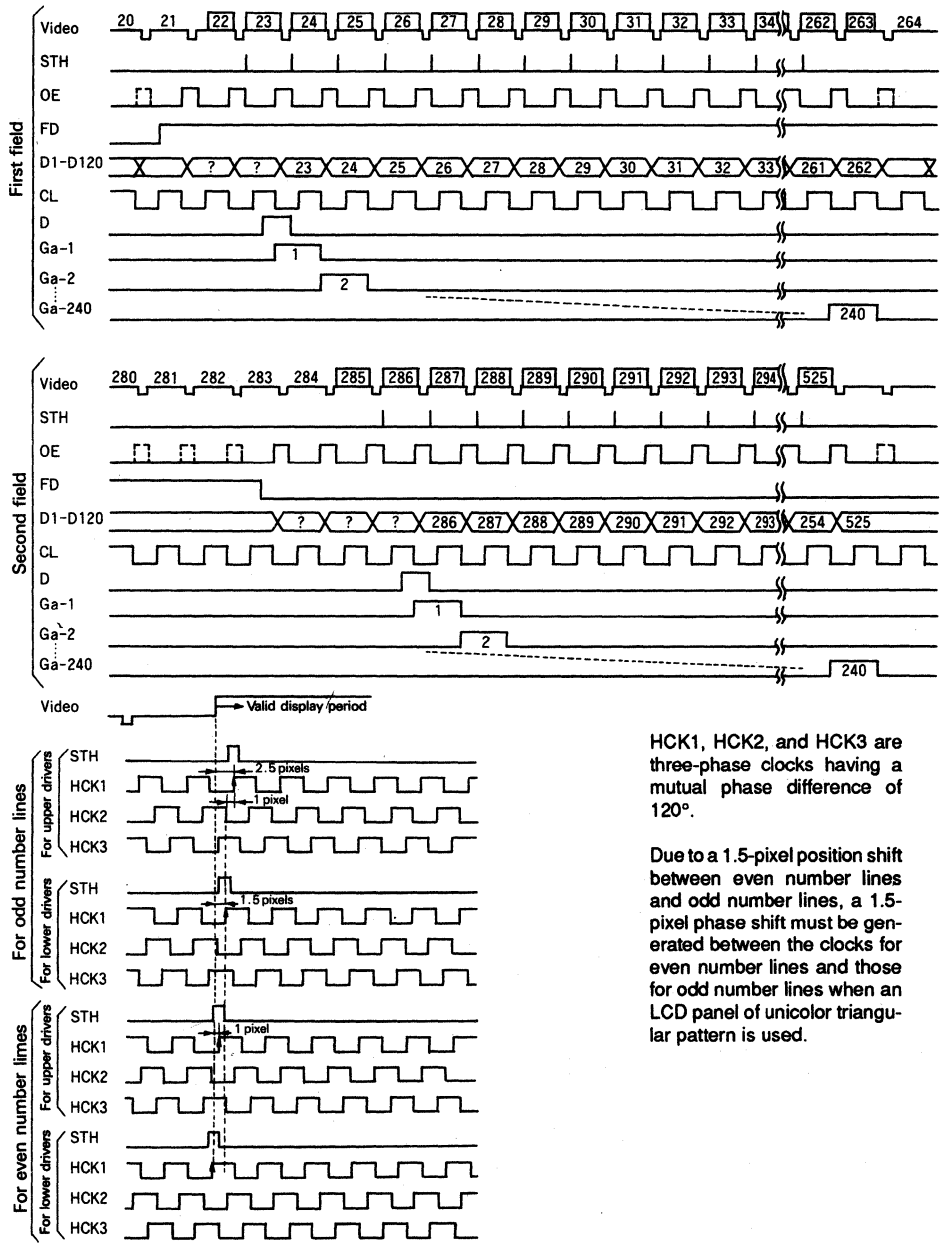


Figure 1 Example of HD66300T Connection to LCD Panel



HCK1, HCK2, and HCK3 are three-phase clocks having a mutual phase difference of 120°.

Due to a 1.5-pixel position shift between even number lines and odd number lines, a 1.5-pixel phase shift must be generated between the clocks for even number lines and those for odd number lines when an LCD panel of unicolor triangular pattern is used.

Figure 2 Timing chart

Functional Description

Screen Size

Number of horizontal pixels:
- 120, 240, 360, 600, and 720 in monodirectional connection mode
- 240, 480, and 720 in bidirectional connection mode

Number of vertical pixels:
- 240 in single-rate sequential drive mode
- 480 in double-rate sequential drive mode

Single-Rate Sequential Drive Mode and Double-Rate Sequential Drive Mode

Single-Rate Sequential Drive Mode: A typical TV signal (Note) has 525 scanning lines, 480 of which are part of the valid display period. In interlace scanning mode, 480 scanning lines are equally divided into a first field and a second field.

In single-rate sequential drive mode, a 240-pixel-high LCD panel is used. 240 scanning lines of the first and second fields of the TV signal are respectively assigned to the 240 lines of the LCD panel.

One line of an LCD panel is driven every horizontal scanning period in this mode.

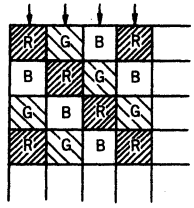
Double-Rate Sequential Drive Mode: To obtain a high-resolution display, a 480-pixel-high LCD panel is used. If 480 scanning lines are respectively assigned to the 480 lines of the LCD panel, the LCD alternating frequency becomes 15 Hz, which causes flickering and degrades display quality. To avoid this problem, the following method is employed. In the first field, the first scanning line is assigned to the first and second lines of the LCD panel, the second scanning line is assigned to the third and fourth lines, and so on. In the second field, the first scanning line is assigned to the second and third lines, the second scanning line is assigned to the fourth and fifth lines, and so on.

Two lines of an LCD panel are driven every horizontal scanning period in this mode.

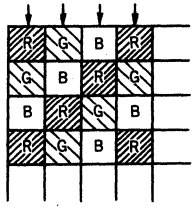
Note:
Refer to the index for the further information of NTSC TV system signals and LCD.

Supportable Types of Color Filter Arrangements

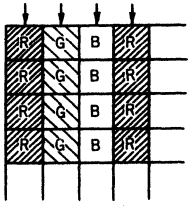
The order and timing for the HD66300T to output color signals depend on the color filter arrangement on a TFT-type LCD panel. The HD66300T can support TFT-type LCD panels having the following color filter arrangements by specifying the operation of the internal color sequence controller and by changing the external signals to be supplied.



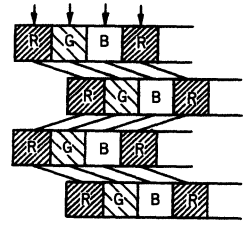
(a) Diagonal from top-left to bottom-right mosaic pattern



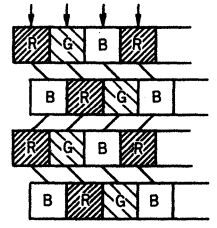
(b) Diagonal from top-right to bottom-left mosaic pattern



(c) Vertical stripe pattern



(d) Unicolor triangular pattern



(e) Bicolor triangular pattern

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Figure 3 Supportable Types of Color Filter Arrangements

Mode Setting Pins

Mode setting pins MSF1, MSF2, and D/S must be set according to both the type of color filter arrangement on the TFT-type LCD panel and the drive mode (single-rate sequential drive mode or double-rate sequential drive mode). These pins activate the internal color sequence controller, which changes the sequence of color video signals corresponding to each sample and hold circuit and allows the LSI to output color data in the right order for the LCD panel being used.

Per-Field Inversion and Per-Line Inversion

The inversion mode of LCD drive signals can be selected by pin L/F.

Per-Field Inversion (available with L/F = low)

In a certain field, all LCD drive signals have one polarity and in the following field, they all have the inverted polarity.

Per-Line Inversion (available with L/F = high)

In a certain field, all LCD drive signals have positive polarity in odd number lines and negative polarity in even number lines, while in the following field, the situation is reversed, that is, negative polarity in odd number lines and positive polarity in even number lines.

Table 1 Mode Setting Pins

Filter Arrangement	Drive Mode	D/S	MSF1	MSF2	Referential Timing Charts
Diagonal mosaic	Single-rate	GND	GND	V_{CC}, GND	MODES 15, 16, 18, and 19
pattern	Double-rate	V_{CC}	GND	V_{CC}, GND	MODES 1, 2, 5, 6, 8, 9, 12, and 13
Vertical stripe	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
pattern	Double-rate	V_{CC}	V_{CC}	V_{CC}	MODES 3, 7, 10, and 14
Unicolor triangular	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
pattern	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11
Bicolor triangular	Single-rate	GND	V_{CC}	GND	MODE 17
pattern	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

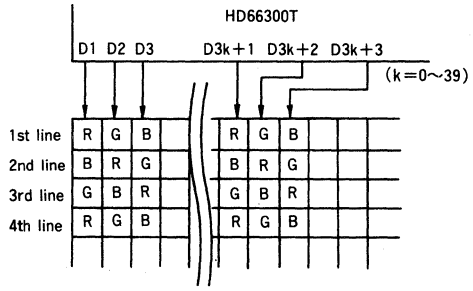
Interface

Video Signals Connection

Video signals must be connected to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3; in principle, positive video signals R, G, and B signals must be input to pins Vx1, Vx2, and Vx3, and negative video signals $\overline{R}$, $\overline{G}$, and $\overline{B}$ to pins Vy1, Vy2, and Vy3. For actual connection between an LCD panel and the LCD drive signal output pins, refer to the following example.

In the case of Diagonal from top-left to bottom-right mosaic pattern.

This example describes the case in which an LCD panel having a diagonal from top-left to bottom-right mosaic pattern is driven in double-rate sequential drive mode and monodirectional connection mode.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → B → G → R →
D2 (=D3k + 2)	G → R → B → G →
D3 (=D3k + 3)	B → G → R → B →

The Signal Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	Vx1 → Vx3 → Vx2 → Vx1 →
D2 (=D3k + 2)	Vx2 → Vx1 → Vx3 → Vx2 →
D3 (=D3k + 3)	Vx3 → Vx2 → Vx1 → Vx3 →

(Refer to MODE 5)

The Connection of Signals

Signal	Color
Vx1	R
Vx2	G
Vx3	B
Vy1	$\overline{R}$
Vy2	$\overline{G}$
Vy3	$\overline{B}$

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In the case of Diagonal from top-right to bottom-left mosaic pattern, Vertical stripe pattern

The same procedure for video signal connection applies to the case in which a TFT-type LCD panel having a diagonal from top-right to bottom-left mosaic pattern or a vertical stripe pattern is used, as well as to the cases where a panel of any pattern is used through the bidirectional connection mode.

Triangular Pattern, Single-Rate Sequential Drive Mode

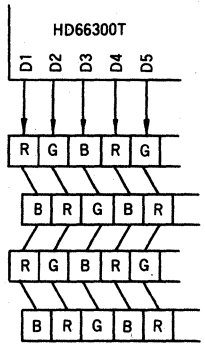
The following procedures are required when a panel of unicolor or bicolor triangular pattern is used:

1. Unicolor Triangular Pattern, Single-Rate Sequential Drive Mode

The clock phase must be changed every line because of the 1.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)
The connection of signals here is the same as that described above.

2. Bicolor Triangular Pattern, Single-Rate Sequential Drive Mode

The clock phase must be changed every line because of the 0.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)
The connection of video signals in the second field must be changed from that in the first field. See the following tables.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → B → R → B →
D2 (=D3k + 2)	G → R → G → R →
D3 (=D3k + 3)	B → G → B → G →

The Signal Sequence for Each Output Pin

	Output Pin	Signal Sequence
1st field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to Mode 17)

The Connection of Signal in Each Field

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	R	$\overline{B}$	R	B
Vx2	G	$\overline{R}$	G	R
Vx3	B	$\overline{G}$	B	G
Vy1	B	$\overline{R}$	$\overline{B}$	$\overline{R}$
Vy2	R	$\overline{G}$	$\overline{R}$	$\overline{G}$
Vy3	G	$\overline{B}$	$\overline{G}$	$\overline{B}$

Triangular Pattern, Double-Rate Sequential Drive Mode

Changing the phase of the sampling clocks is sufficient when the panel is driven in single-rate sequential drive mode. However, when the panel is driven in double-rate sequential drive mode, the above countermeasure does not work, since the display data for two lines is sampled at one time here. Consequently, delaying the input video signal for a time period corresponding to the shift between pixels is required.

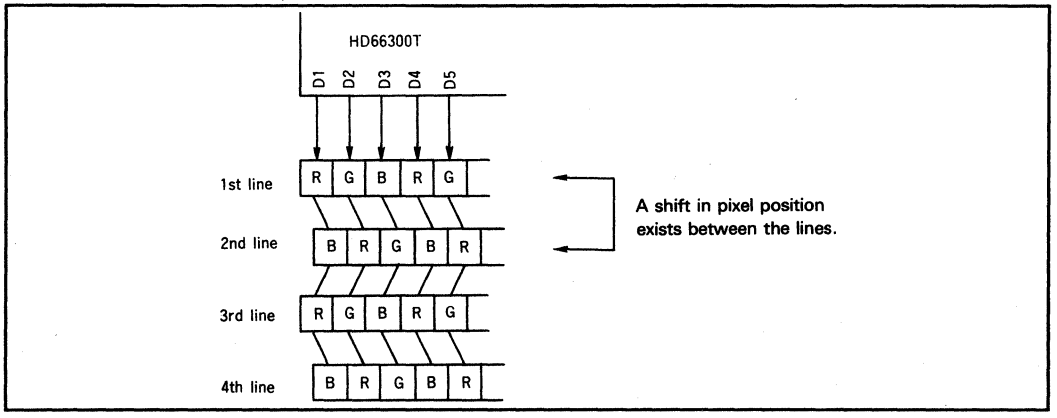


Figure 4

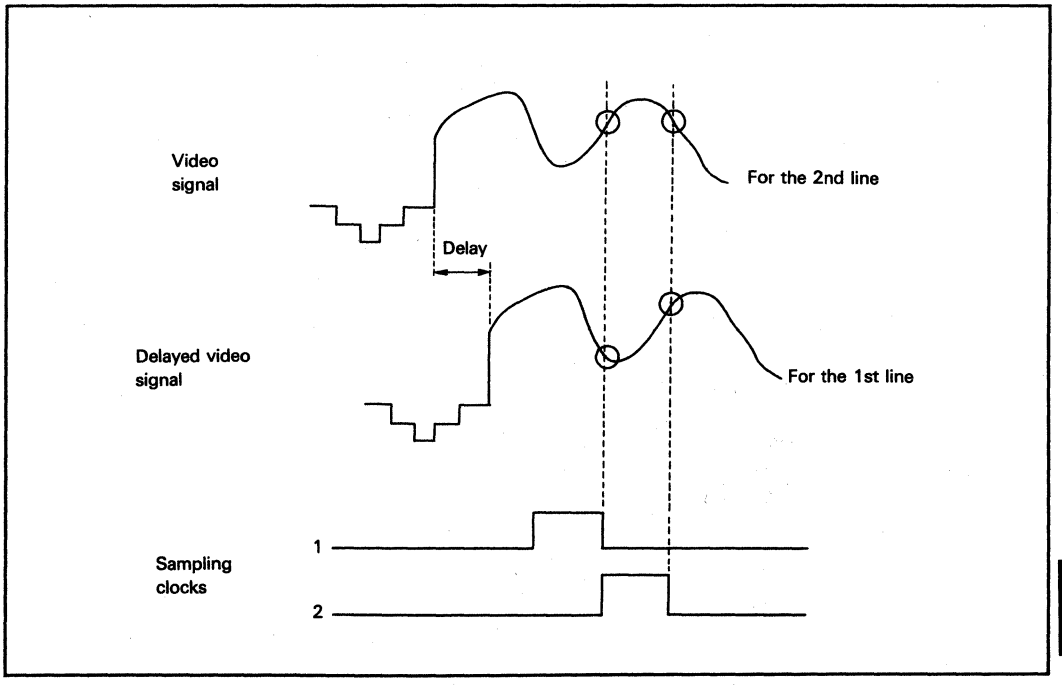
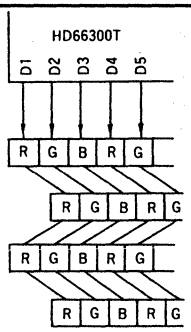


Figure 5

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → R → R → R →
D2 (=D3k + 2)	G → G → G → G →
D3 (=D3k + 3)	B → B → B → B →

The Signal Sequence for Each Output Pin (In Interlace mode)

	Output Pin	Signal Sequence
1st field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In non-interlace mode)

	Output Pin	Signal Sequence
1st field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode (Cont.)

The Connection of Signals in Each Field in Interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	$\overline{R}$	Delayed R	R
Vx2	Delayed G	$\overline{G}$	Delayed G	G
Vx3	Delayed B	$\overline{B}$	Delayed B	B
Vy1	R	Delayed $\overline{R}$	$\overline{R}$	Delayed $\overline{R}$
Vy2	G	Delayed $\overline{G}$	$\overline{G}$	Delayed $\overline{G}$
Vy3	B	Delayed $\overline{B}$	$\overline{B}$	Delayed $\overline{B}$

The Connection of Signals in Each Field in Non-Interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	R	$\overline{R}$	$\overline{R}$	R
Vy2	G	$\overline{G}$	$\overline{G}$	G
Vy3	B	$\overline{B}$	$\overline{B}$	B

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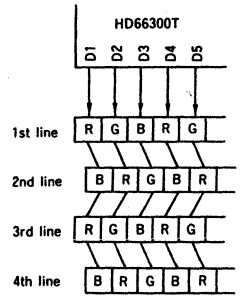
2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → R → R → R →
D2 (=D3k + 2)	G→ R → G → R →
D3 (=D3k + 3)	B → G → B → G →

The Signal Sequence for Each Output Pin (In Interlace mode)

	Output Pin	Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
field	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In non-interlace mode)

	Output Pin	Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode (Cont.)

The Connection of Signals in Each Field in Interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	$\overline{B}$	Delayed R	B
Vx2	Delayed G	$\overline{R}$	Delayed G	R
Vx3	Delayed B	$\overline{G}$	Delayed B	G
Vy1	B	Delayed $\overline{R}$	$\overline{B}$	Delayed $\overline{R}$
Vy2	R	Delayed $\overline{G}$	$\overline{R}$	Delayed $\overline{G}$
Vy3	G	Delayed $\overline{B}$	$\overline{G}$	Delayed $\overline{B}$

The Connection of Signals in Each Field in Non-Interlace Mode

	Per-Field Inversion Mode (L/F = low)		Per-Line Inversion Mode (L/F =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	B	$\overline{B}$	$\overline{B}$	B
Vy2	R	$\overline{R}$	$\overline{R}$	R
Vy3	G	$\overline{G}$	$\overline{G}$	G

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Connection to LCD Panels

There are two modes of connecting HD66300T chips to an LCD panel:

1) monodirectional connection mode
2) interleaved connection mode

In the former mode, the HD66300Ts are set on either the upper side or lower side of the panel, while in the latter mode, the HD66300Ts are set on both sides and the upper drivers and the lower drivers are alternately connected to each pixel-column.

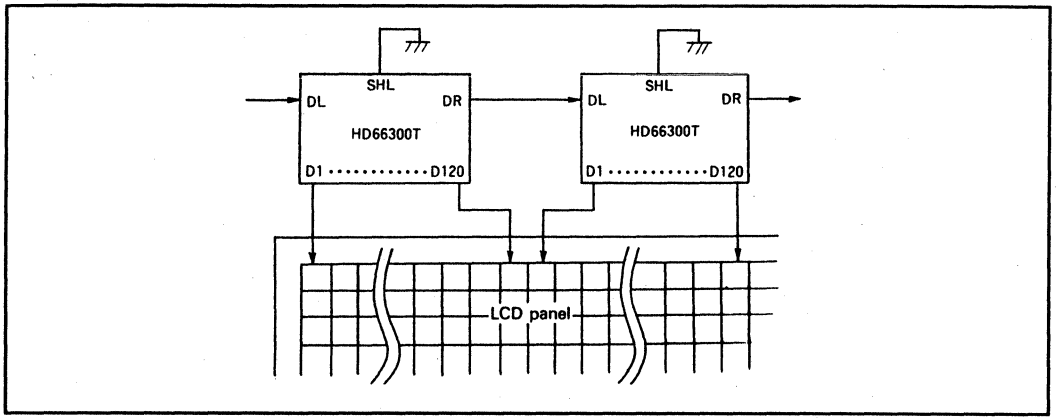

Figure 6 Monodirectional Connection Mode

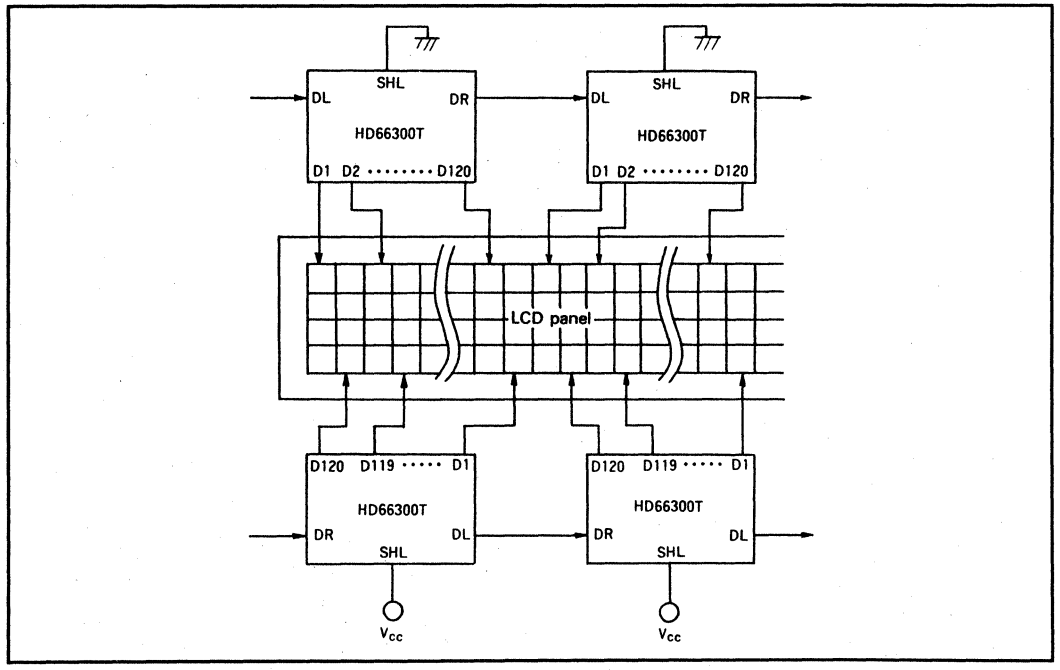

Figure 7 Interleaved Connection Mode

Internal Operation

The HD66300T has four sample and hold circuits for each outputs as shown in the block diagram, and its internal bidirectional shift register controls which circuits to sample data.

It has three-phase shift clocks with mutual phase difference of 120° to drive the shift register, which enables driving an LCD panel with mosaic pattern and triangular pattern.

The operation of sample and hold circuits and sampling operation are described below followed by the description of the relationship between three-phase shift clock phases and frequencies.

After the above description, determination of bias voltage is described; bias voltage controls driving characteristics of a differential amplifier and output buffer of the sample and hold circuits.

Finally, the OE and FD signals are described; they determine the operation of the sample and hold shift matrix circuit. Timing charts for each mode follow the description.

Sample and Hold Circuitry

Operation of Sample and Hold Circuitry

The HD66300T has four sample and hold circuits A, B, C, and D per LCD drive signal output. Sample and hold circuit pair A and B is supplied with the same sampling clock pulses as circuit pair C and D. One of the signals output by these circuits is connected to an output driver.

These sample and hold circuits repeat sampling and outputting of signals alternately to drive an TFT-type LCD panel.

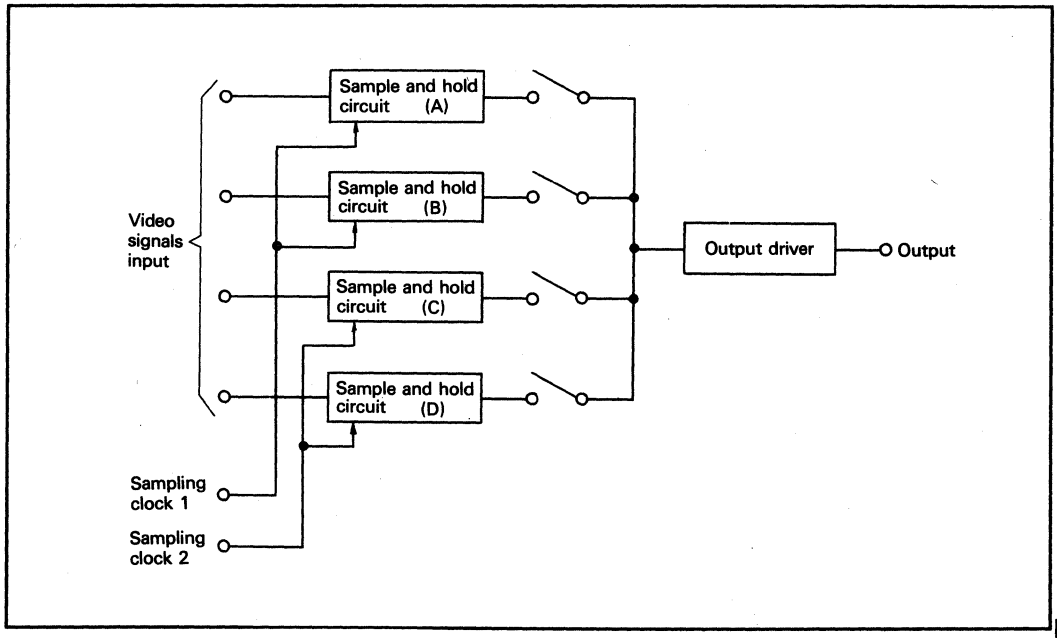

Figure 8 Sample and Hold Circuitry

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In single-rate sequential drive mode, sample and hold circuits A and D are alternately used; circuits B and C perform sampling operation, but are not used since they are not connected to the output driver.

In single-rate sequential drive mode, one sample and hold circuit samples the signal during one horizontal scanning period, and outputs it as an LCD drive signal in the following horizontal scanning period.

In double-rate sequential drive mode, all sample and hold circuits A, B, C, and D are alternately used.

In double-rate sequential drive mode, two sample and hold circuits sample two signals during one horizontal scanning period, and output one of them as an LCD drive signal in the first half of the following horizontal scanning period, and output the other signal in the second half.

The following shows the timing charts of sampling and outputting operation.

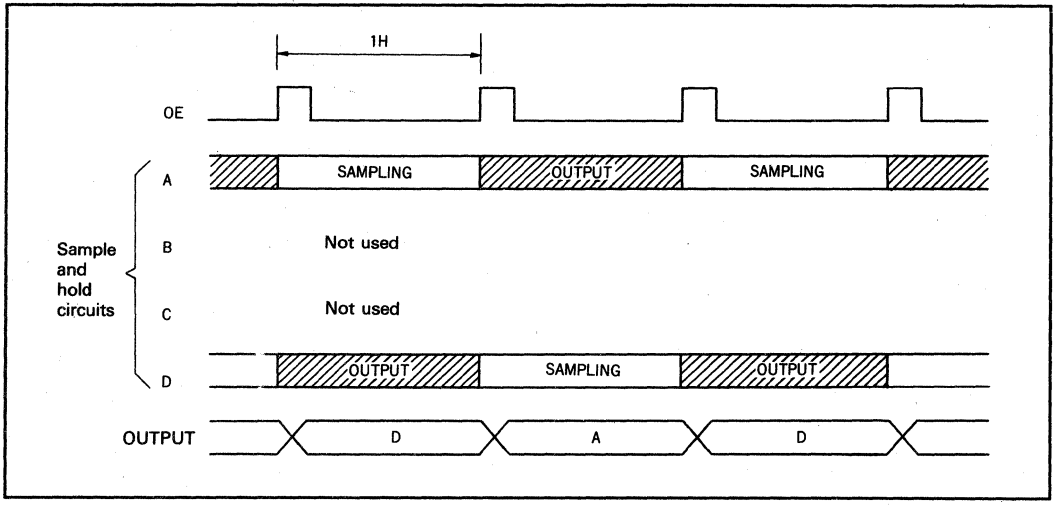

Figure 9 Sampling Timing charts of Single-Rate Sequential Drive Mode

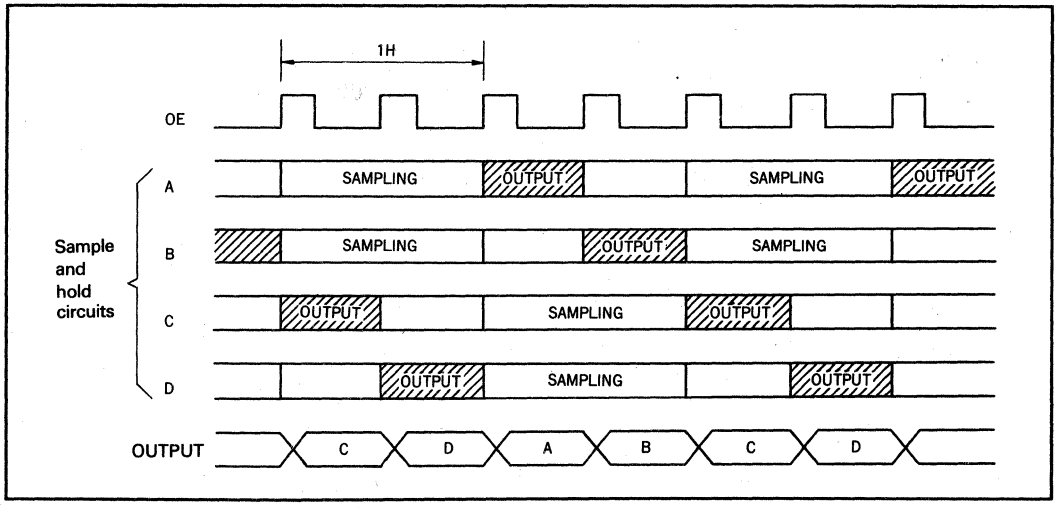

Figure 10 Sampling Timing charts of Double-Rate Sequential Drive Mode

Sampling Operation

The HD66300T has a bidirectional shift register composed of 120 bits and each bit of the shift register generates the sampling pulses to control the sampling operation of the four sample and hold circuits connected to each LCD drive signal output pin. When a bit of the shift register is 1, the corresponding sample and hold circuits are in the sampling state; when it is 0, the corresponding sample and hold circuits are in the hold state. Consequently, shifting a 1 into the shift register activates in turn the sample and hold circuits corresponding to each LCD drive signal output pin.

Figure 11 is a shift register sketch illustrating the relationship between the shift register and the shift clocks HCK1, HCK2, and HCK3. Note that the order of sampling pulse generation depends on the state of pin SHL. D1 corresponds to DL and D120 to DR.

Figure 12 is a timing chart of sampling pulses generated by the shift register.

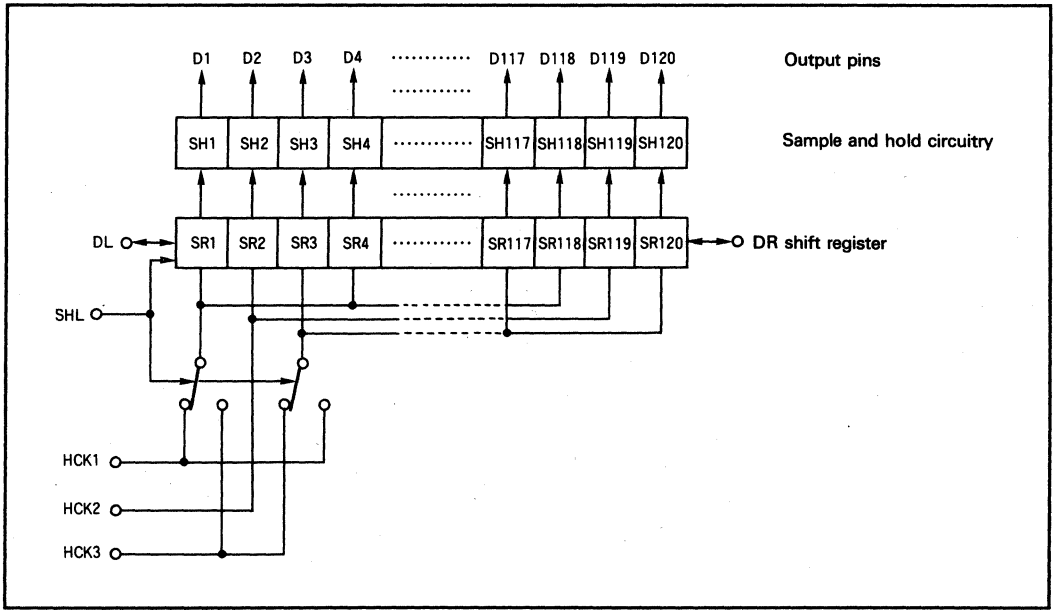

Figure 11 Shift Register Sketch

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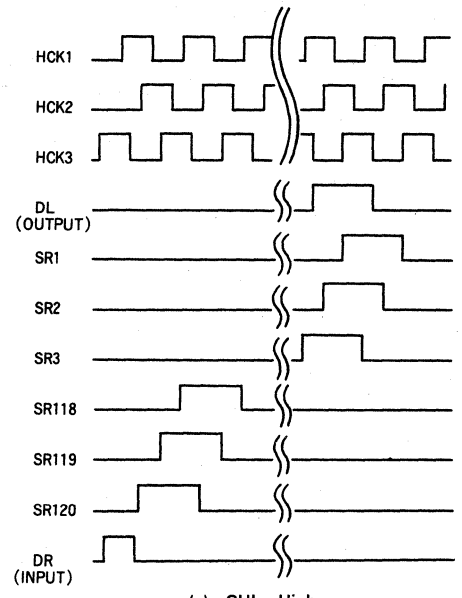
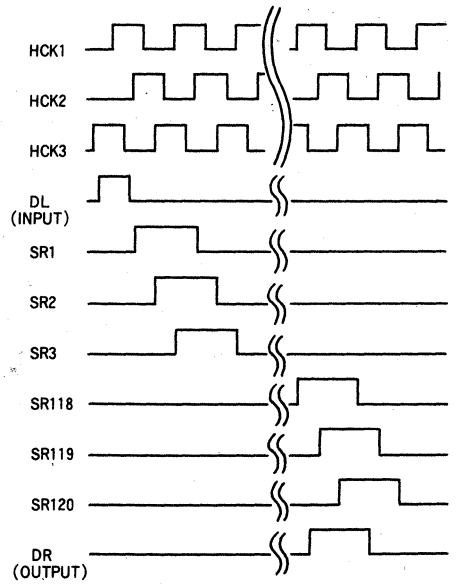


(a) SHL=High



(b) SHL=Low

Figure 12 Sampling Pulse Timing Chart

Three-Phase Shift Clocks

Three-Phase Shift Clocks and Sample Start Signal

Shift clocks HCK1, HCK2, and HCK3, which are operation clocks for the shift register, must be three-phase clocks with 50-percent duty. The HCK2 clock must be generated 120° after the HCK1 clock, and the HCK3 clock 240° after the HCK1 clock. Sampling operation starts when 1 is input from pin DL or DR at a rising edge of the HCK1 clock pulse.

In monodirectional connection mode, all the HD66300T chips must be supplied with the same three-phase shift clock pulses. In interleaved connection mode, the frequency of the three-phase shift clocks must be half of that in monodirectional connection mode, and the phase shift between the upper drivers clocks and the lower drivers clocks must be one pixel.

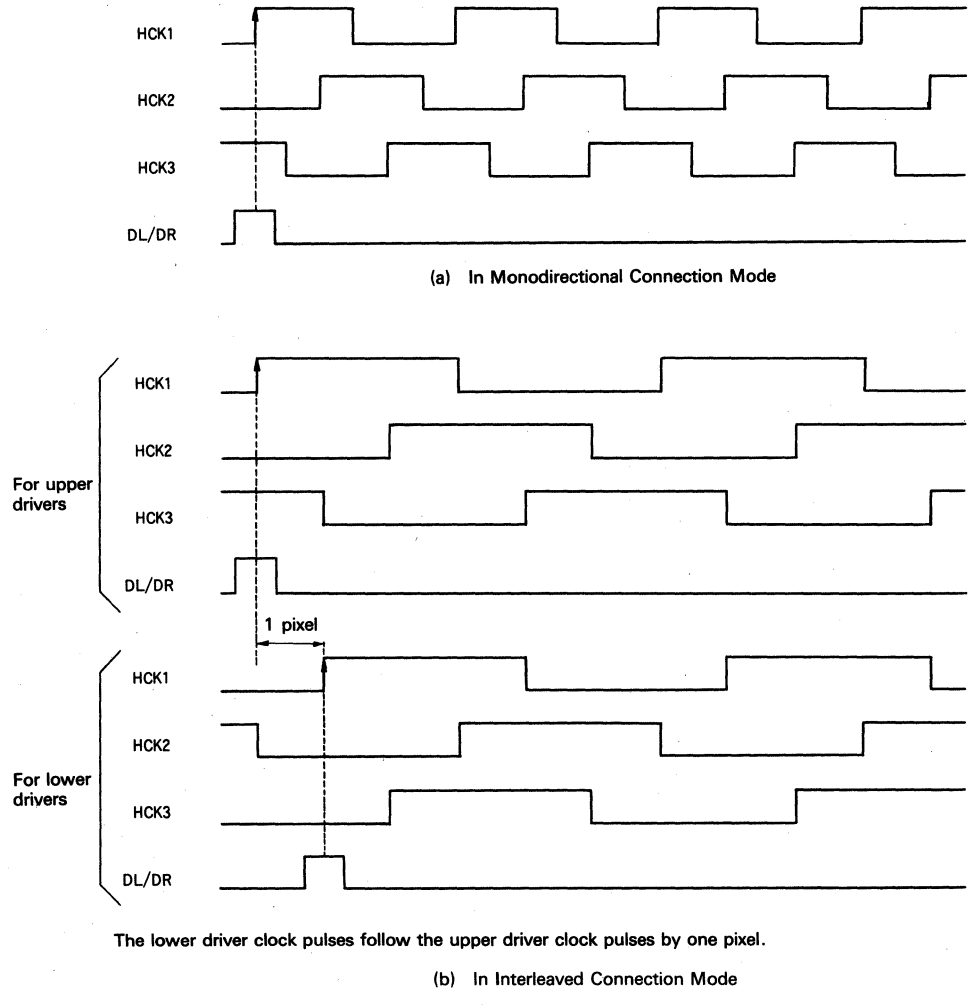
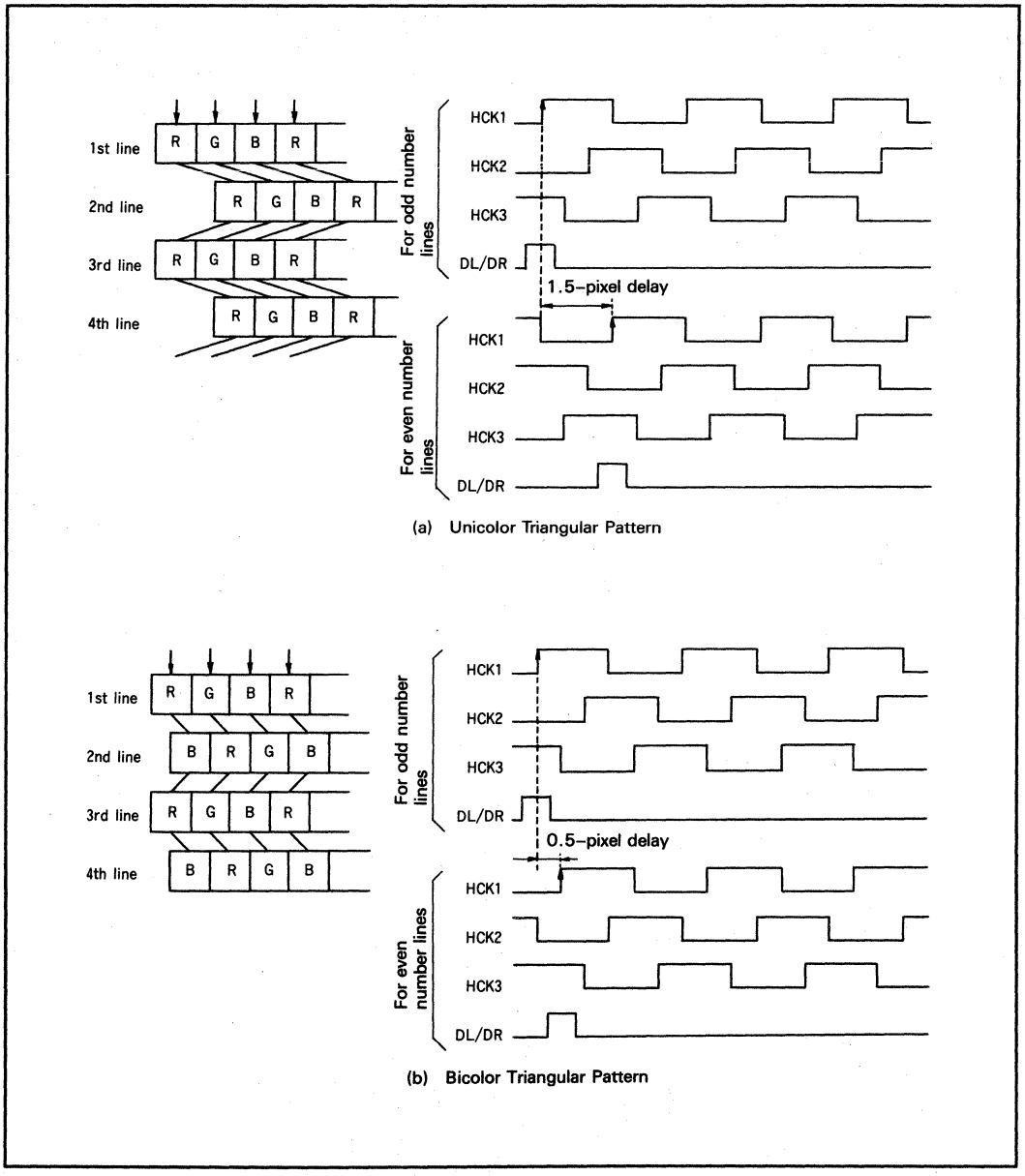


Figure 13 Three-Phase Shift Clocks and Sample Start Signal

Some position shift exists between the pixels of even number lines and those of odd number lines for LCD panels having triangular patterns. This requires generating a phase shift between the three-phase clocks for even number lines and those for odd number lines. The required phase shift is 1.5 pixels for LCD panels having a unicolor triangular pattern, while it is 0.5 pixels for those having a bicolor triangular pattern.



(a) Unicolor Triangular Pattern

(b) Bicolor Triangular Pattern

Figure 14

How to Generate Three-Phase Shift Clocks

Three-phase shift clocks can be generated by dividing the base clock, which is generated from a horizontal synchronizing clock, through the use of a frequency multiplier such as a PLL circuit.

The number of horizontal pixels of the LCD panel and the valid display ratio determines the base clock frequency f.

If the number of horizontal pixels is 480 and the valid display ratio is 95% in the NTSC system, the base clock frequency f is about 9.59 MHz according to the following equation.

f = (1/valid display period) x (no. of horizontal pixels/valid display ratio)
= 480/(52.7 µsec x 0.95)
= 9.59 (MHz)

The three-phase clocks can be generated by dividing f by 3 (in the monodirectional connection mode) or 6 (in the interleaved connection mode).

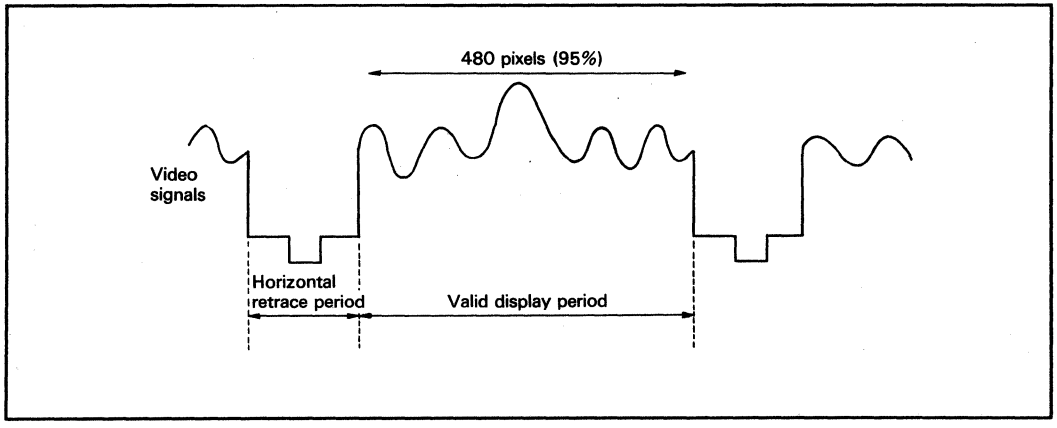


Figure 15 Base Clock

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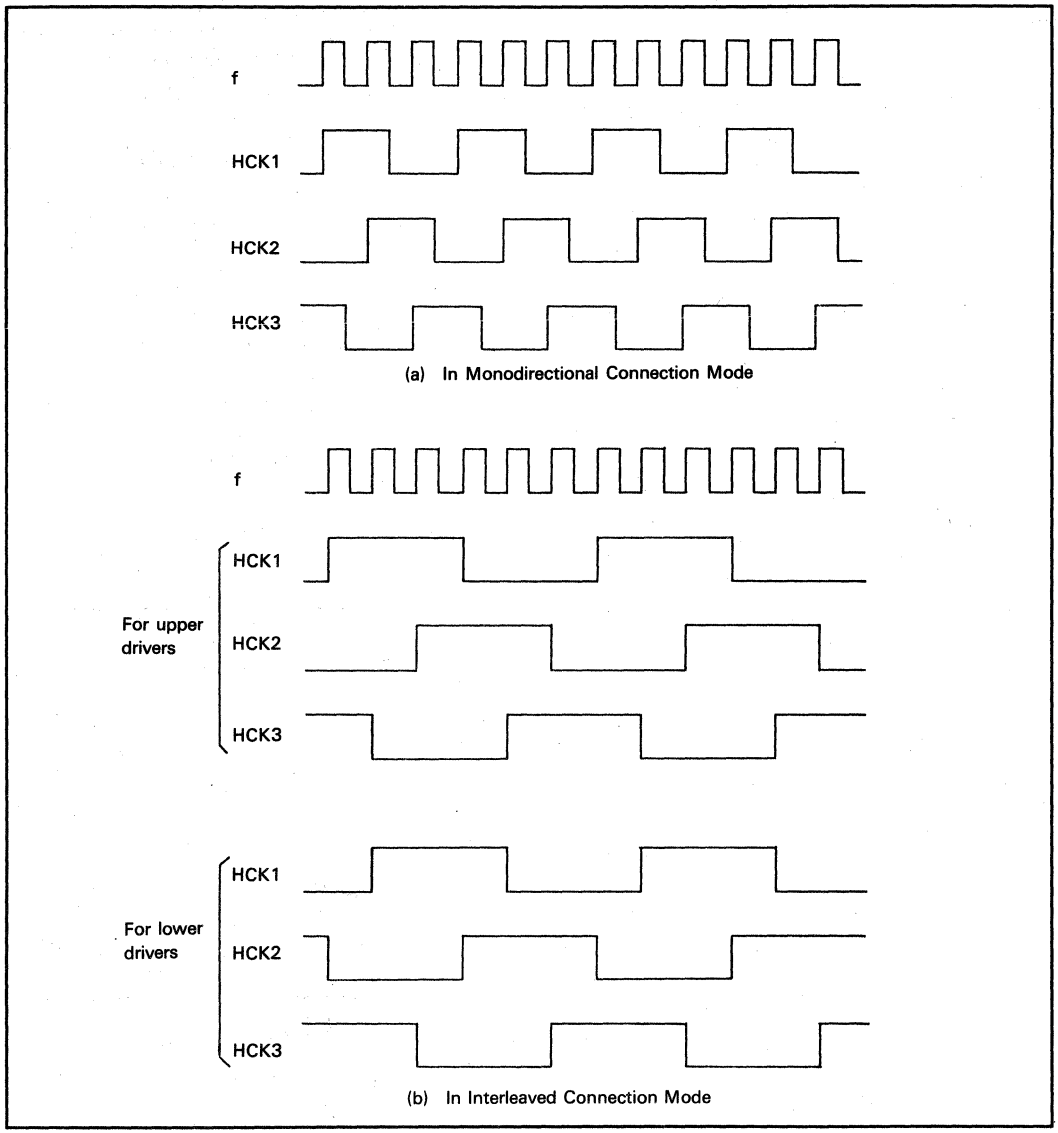

Figure 16 Three-Phase Shift Clocks

Bias Voltage

Voltages V_{bsB}, V_{bsH}, and V_{bo} control the drive capability of the output buffer and differential amplifier. Here the LSI must be used in the range of

$$V_{CC} - 4.0\ V \leqq V_{bsB}, V_{bsH}, V_{bo} \leqq V_{CC} - 2.0\ V$$

V_{bsB} controls the drive current capability of the output buffer when OE is high (IV_{sB}) and V_{bsH} controls the leakage correction current of when OE is low (IV_{sH}). Figure 17 and figure 18 show the relationship between IV_{sB} and V_{bsB} and the relationship between IV_{sH} and V_{bsH}, respectively.

V_{bsB} and V_{bsH} should be to an appropriate level for the electrical characteristics of the LCD panel used.

The rise time (t_{DDR}) and the fall time (t_{DDF}) of the output buffer depend on the input level of V_{bsB}. Figure 19 shows the relationship between t_{DDR}, t_{DDF} and V_{bsB}.

V_{bo} controls the bias current of the differential amplifier (IV_{bo}).

Figure 20 shows the relationship between the rise and fall times (t_{DDR}, t_{DDF}) of the output buffer and V_{bo}. V_{bo} should be adjusted to an appropriate level for the electrical characteristics of the LCD panel used.

The increase of total current consumption is 120 times larger than that of IV_{bsB}, IV_{bsH} and IV_{bo}, because figure 17, 18 and 21 each shows the case of one output and HD66300T has 120 outputs.

Figure 17, 18, 19, 20 and 21 are just for reference and do not guarantee the characteristics.

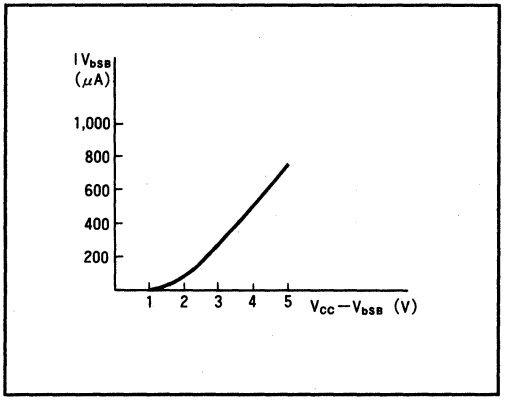

Figure 17 IV_{bsB} vs V_{CC}–V_{bsB}

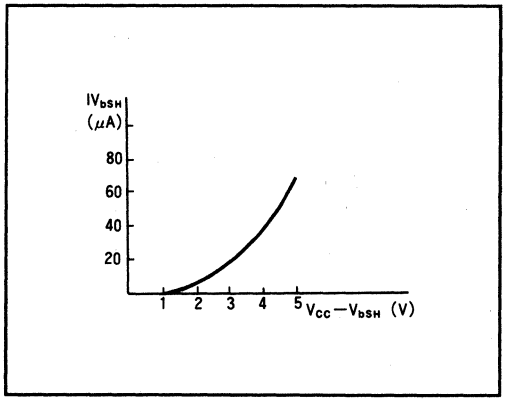

Figure 18 IV_{bsH} vs V_{CC}–V_{bsH}

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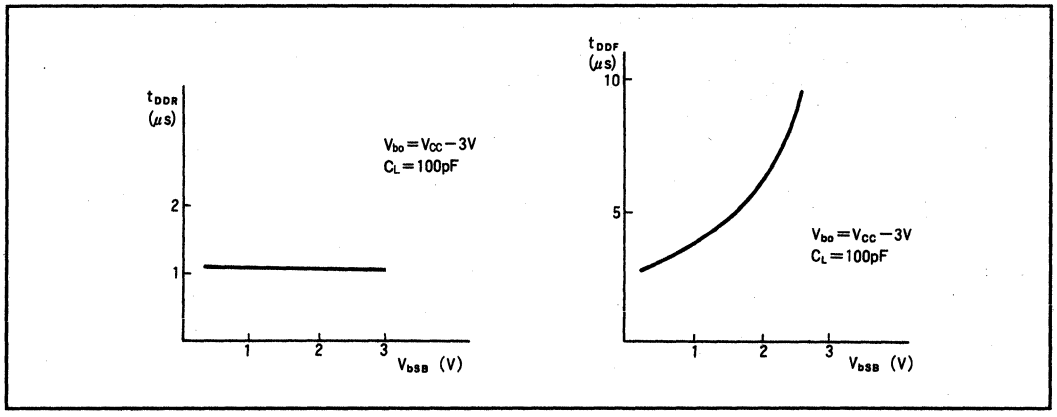

Figure 19 t_{DDR}, t_{DDF} vs V_{bsB}

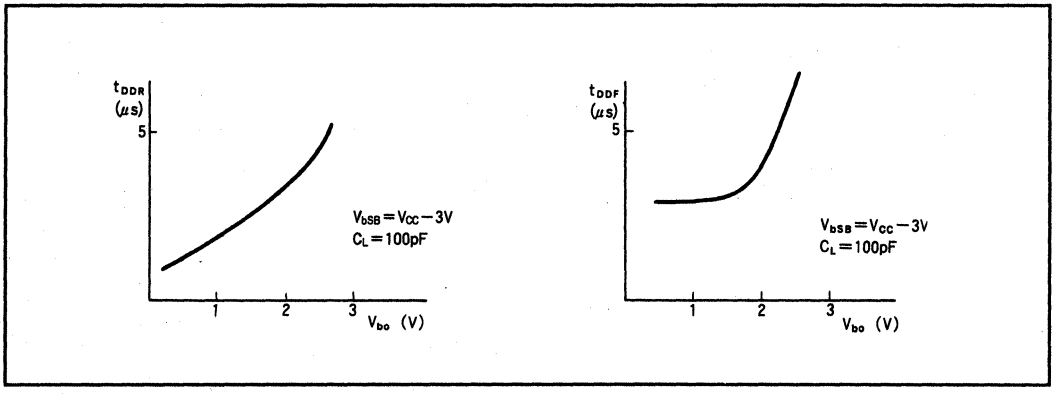

Figure 20 t_{DDR}, t_{DDF} vs V_{bo}

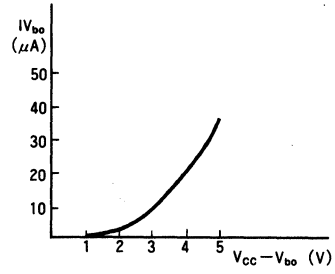

Figure 21 IV_{bo} vs V_{CC}–V_{bo}

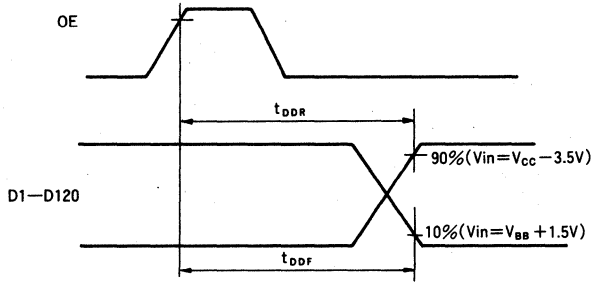

Figure 22 Definition of t_{DDR} and t_{DDF}

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OE Signal

The OE signal has the following functions:

Clock for internal circuits: Controls the sample and hold circuitry and the controller of the shift matrix circuit, and switches the output signal at the OE signal rising edge.

Switching of drive capability of the output buffer: Determines the current drive capability of the output buffer;

OE = high: Drives with large current (300 μA, typ)
OE = low: Drives with small current (20 μA, typ)

This function allows the output buffer to operate with large current during the transition of an output signal, thus shortening its falling time. At the same time it allows the output buffer to operate with small current while an output signal is stable, lowering current consumption.

The drive current is controlled by bias voltages V_{bsB} (large current) and V_{bsH} (small current).

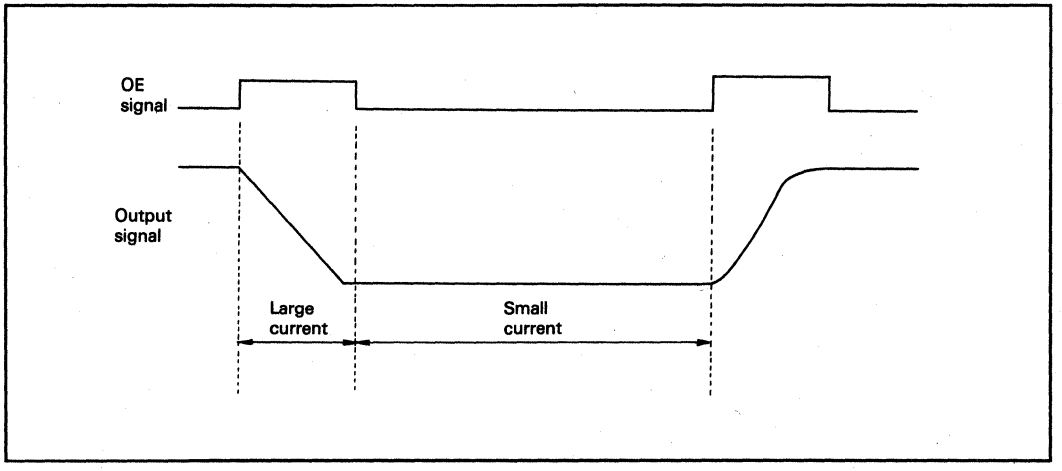

Figure 23 Switching of Drive Capability of the Output Buffer

FD Signal

The FD signal is the field determination signal; a field is determined by the state of this signal at the rising edge of the OE signal. This signal synchronizes the internal controllers with TV signals.

The order of outputting signals is determined at the fourth rising edge of the OE signal after the rising or falling edge of the FD signal in double-rate sequential drive mode, while it is determined at the third rising edge in single-rate sequential drive mode; hereinafter, as long as the FD signal is not changed, signals will be output in the determined order at most every 12 pulses of the OE signal in double-rate sequential drive mode, while at most every 6 pulses in single-rate sequential drive mode.

The FD signal should usually be high in the first field and low in the second field. In some modes, however, it should be high in both fields, but low for at least one-pulse time period of the OE signal during the horizontal scanning period.

The order of outputting signals and the timing of inputting the FD signal vary depending on the mode. For more details, refer to the appropriate timing charts.

Timing Charts for Each Mode

Table 2 Reference timing charts for each mode

			Single (D/S = Low)		Double (D/S = High)			
					Interlace		Non-Interlace	
Filter Arrangement			Per-Line	Per-Field	Per-Line	Per-Field	Per-Line	Per-Field
Mosaic	Top-left to bottom-right	Inter-leaved	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
		Monodi-rectional	MODE 16	MODE 19	MODE 1	MODE 5	MODE 8	MODE 12
	Top-right to bottom-left	Inter-leaved	MODE 16	MODE 19	MODE 1	MODE 5	MODE8	MODE 12
		Monodi-rectional	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
Vertical stripe			MODE 17	MODE 20	MODE 3	MODE 7	MODE 10	MODE 14
Unicolor triangular			MODE 17	MODE 20	MODE 4	MODE 4	MODE 11	MODE 11
Bicolor triangular			MODE 17	MODE 17	MODE 4	MODE 4	MODE 11	MODE 11

Single: Single-rate sequential drive mode
Double: Double-rate sequential drive mode
Per-Line: Per-line inversion mode
Per-Field: Per-field inversion mode
Interleaved: Interleaved connection mode
Monodirectional: Monodirectional connection mode

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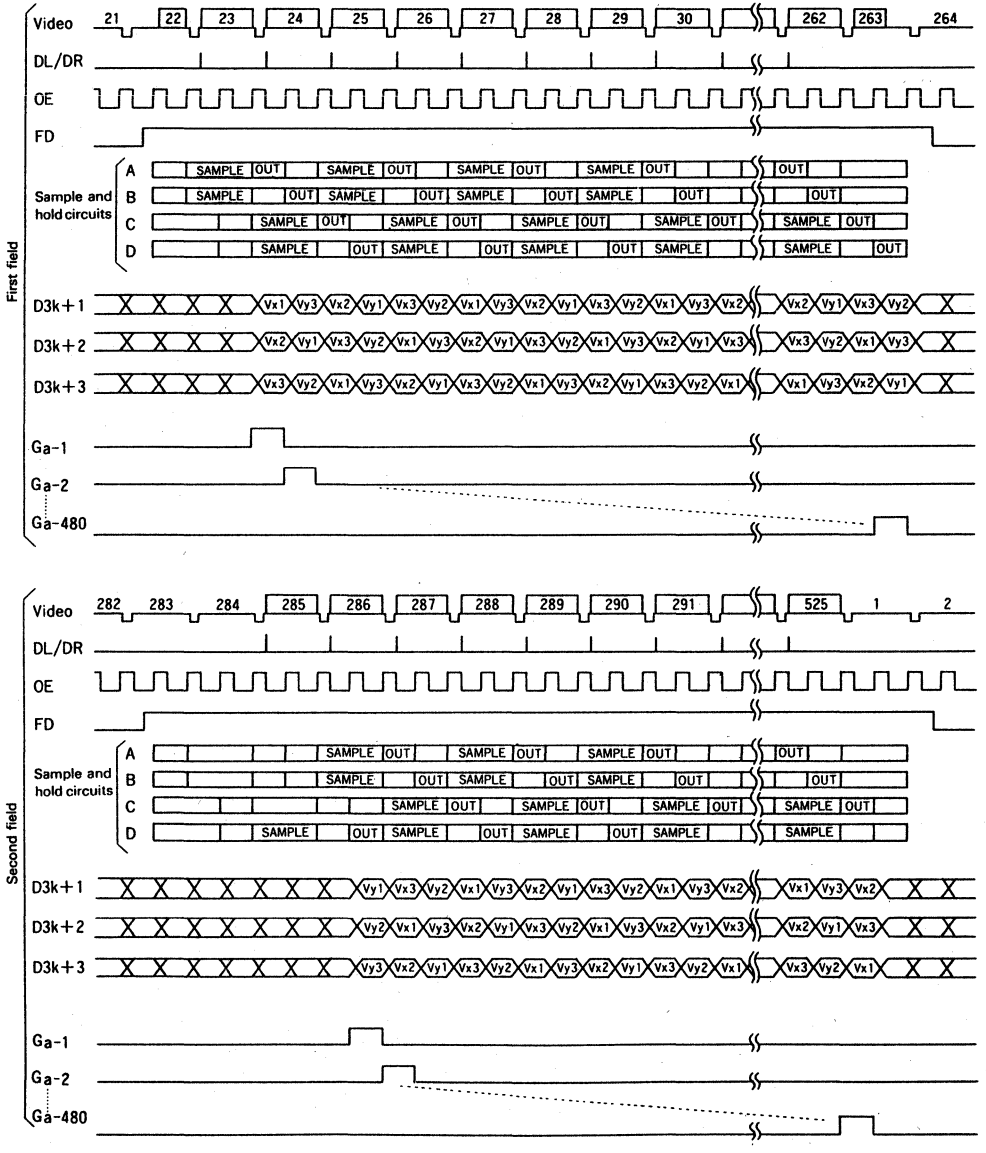
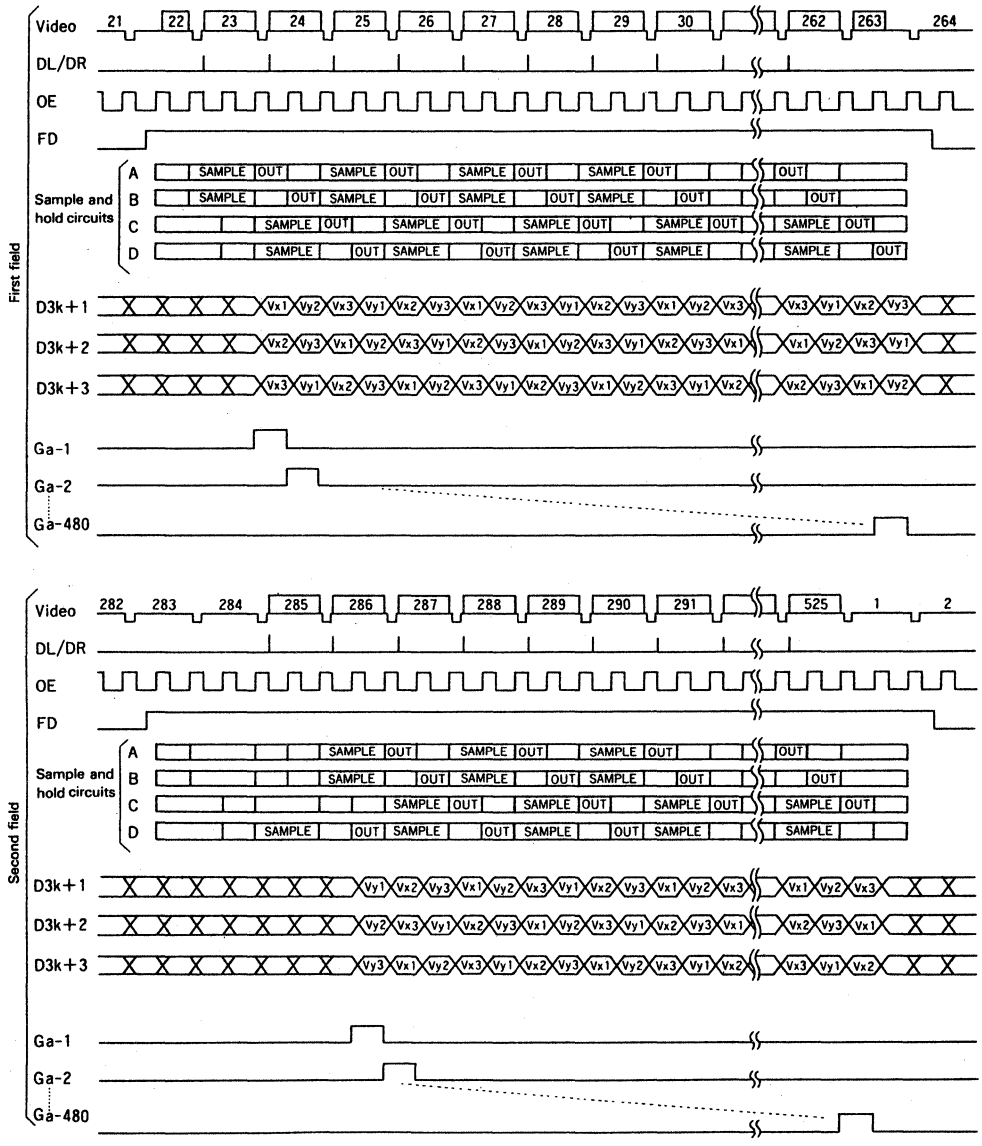
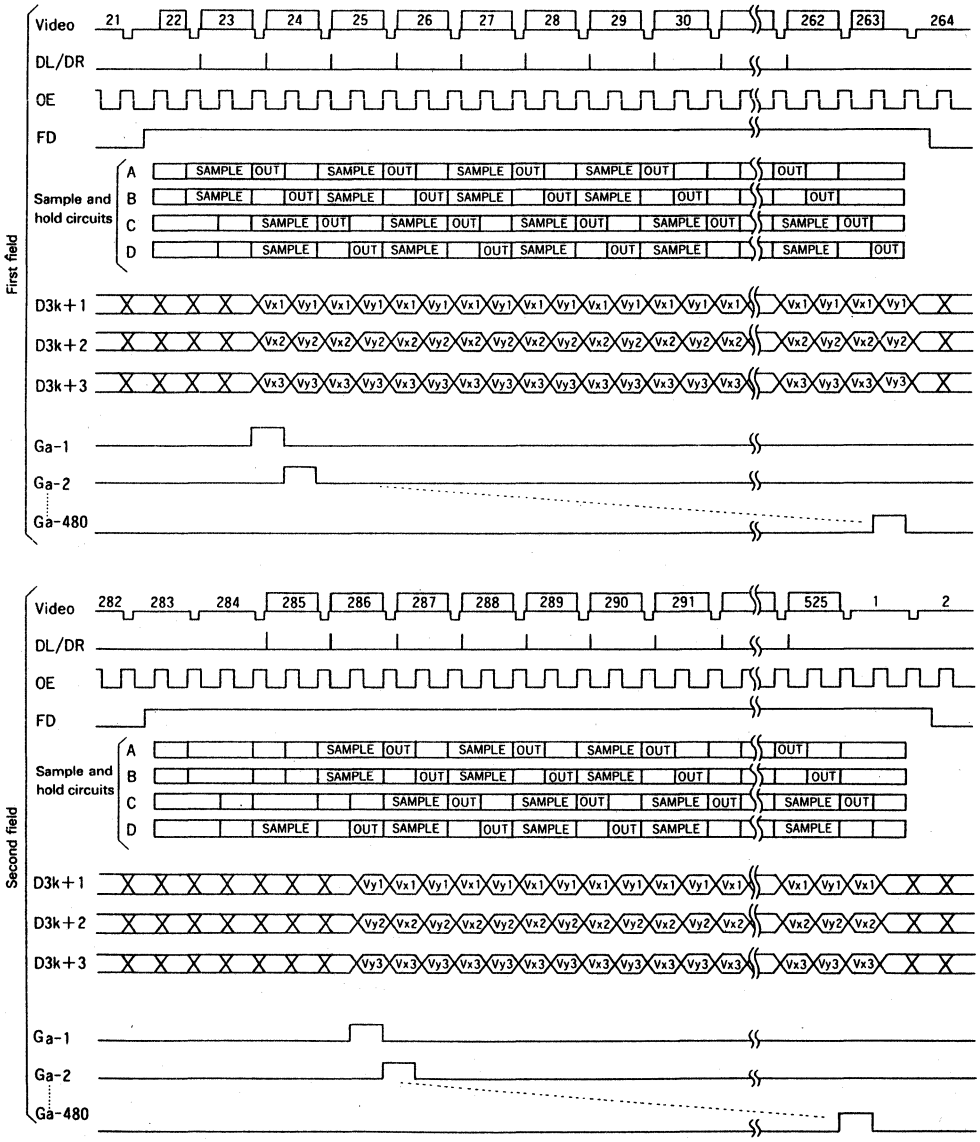
MODE 1	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	V_{cc}



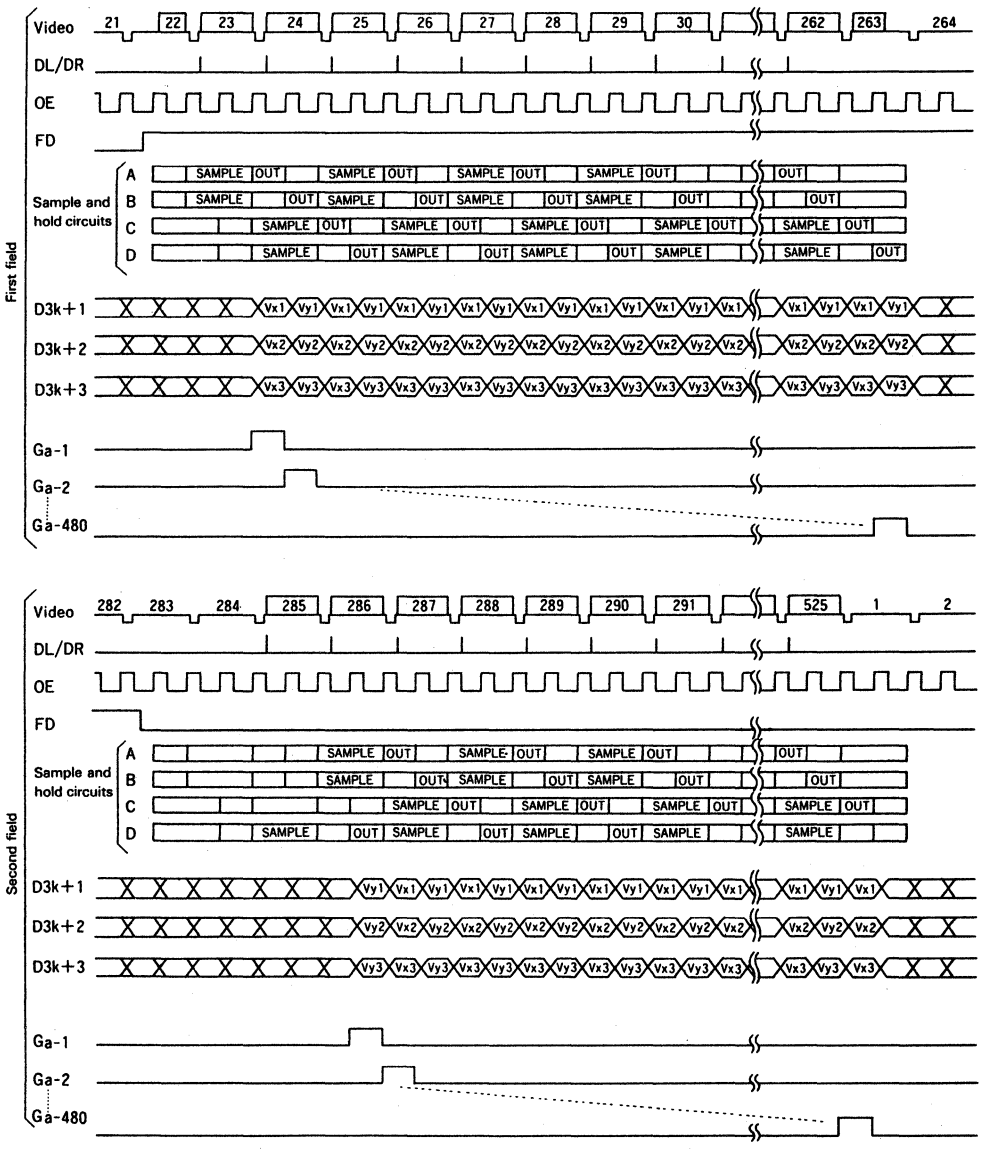
MODE 2	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	GND



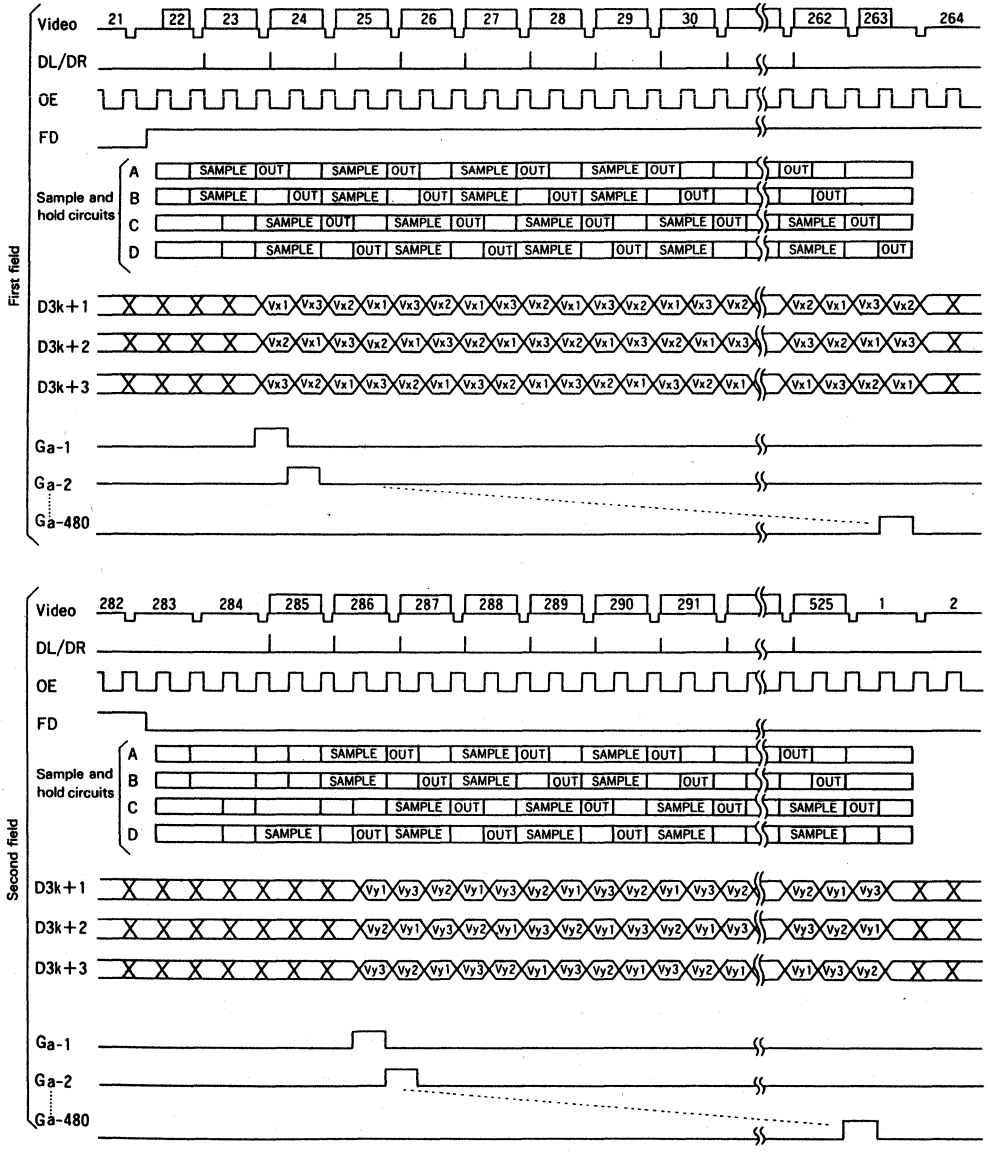
MODE 3	
D/S	V_{cc}
L/F	V_{cc}
MSF1	V_{cc}
MSF2	V_{cc}



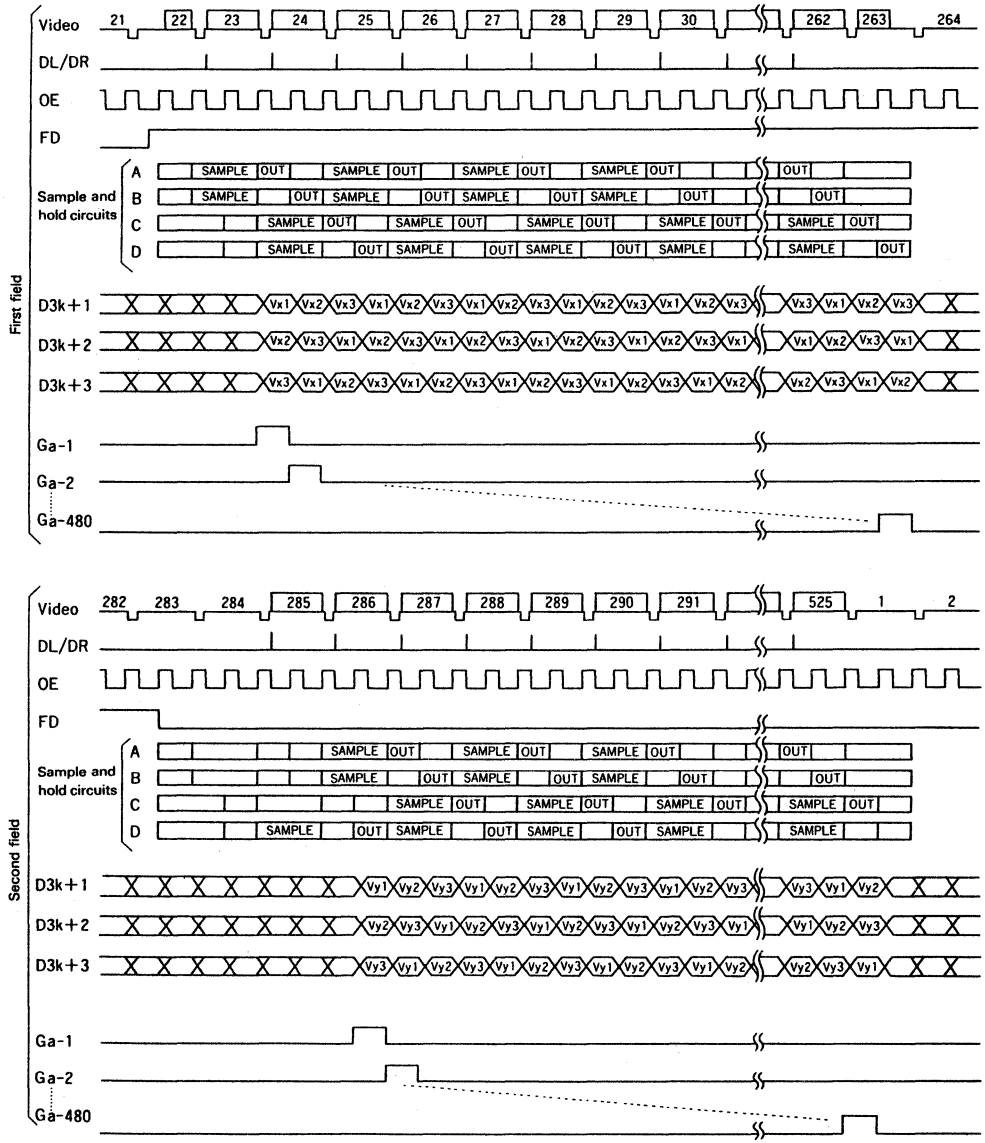
MODE 4	
D/S	V_{CC}
L/F	V_{CC}/GND
MSF1	V_{CC}
MSF2	GND



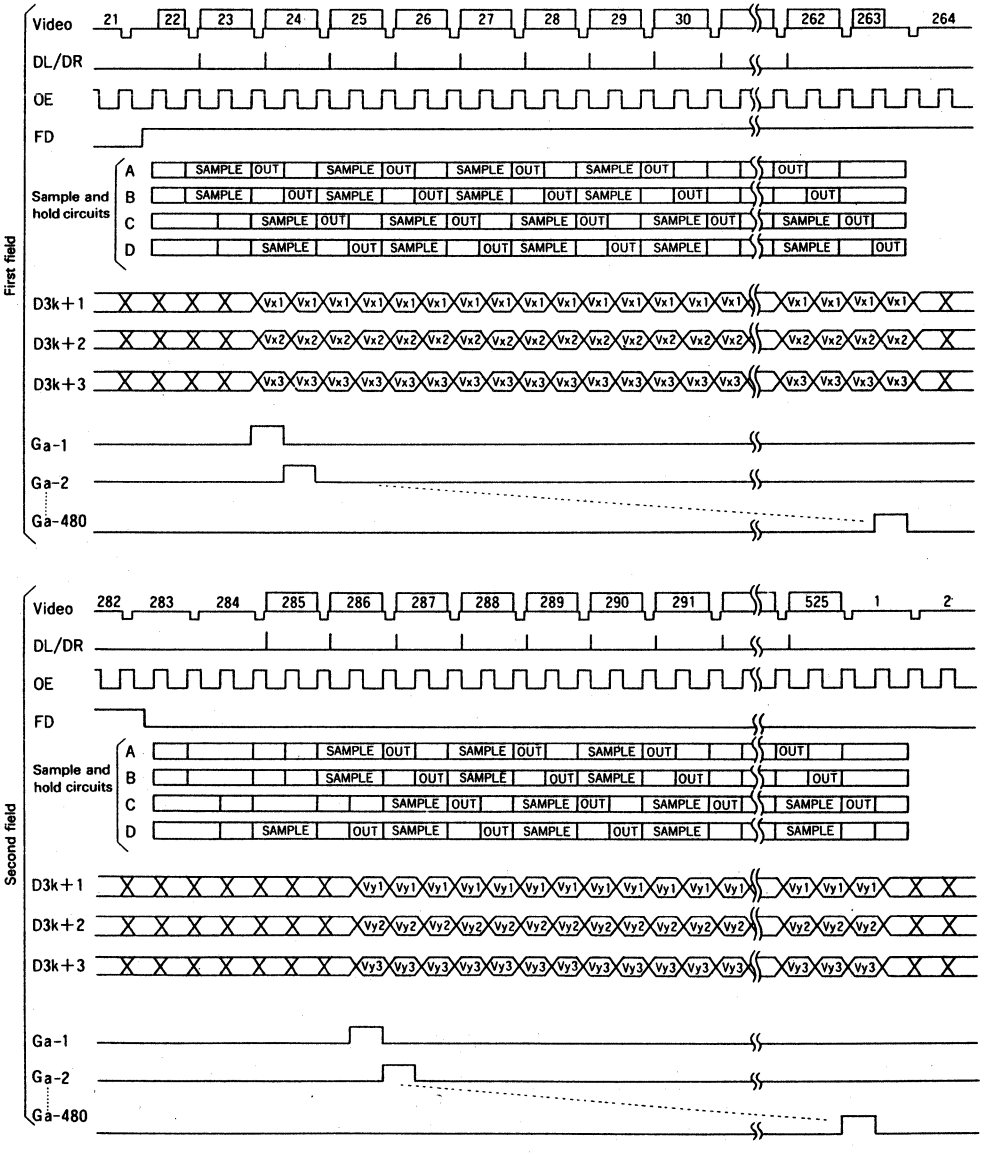
MODE 5	
D/S	V_{cc}
L/F	GND
MSF1	GND
MSF2	V_{cc}



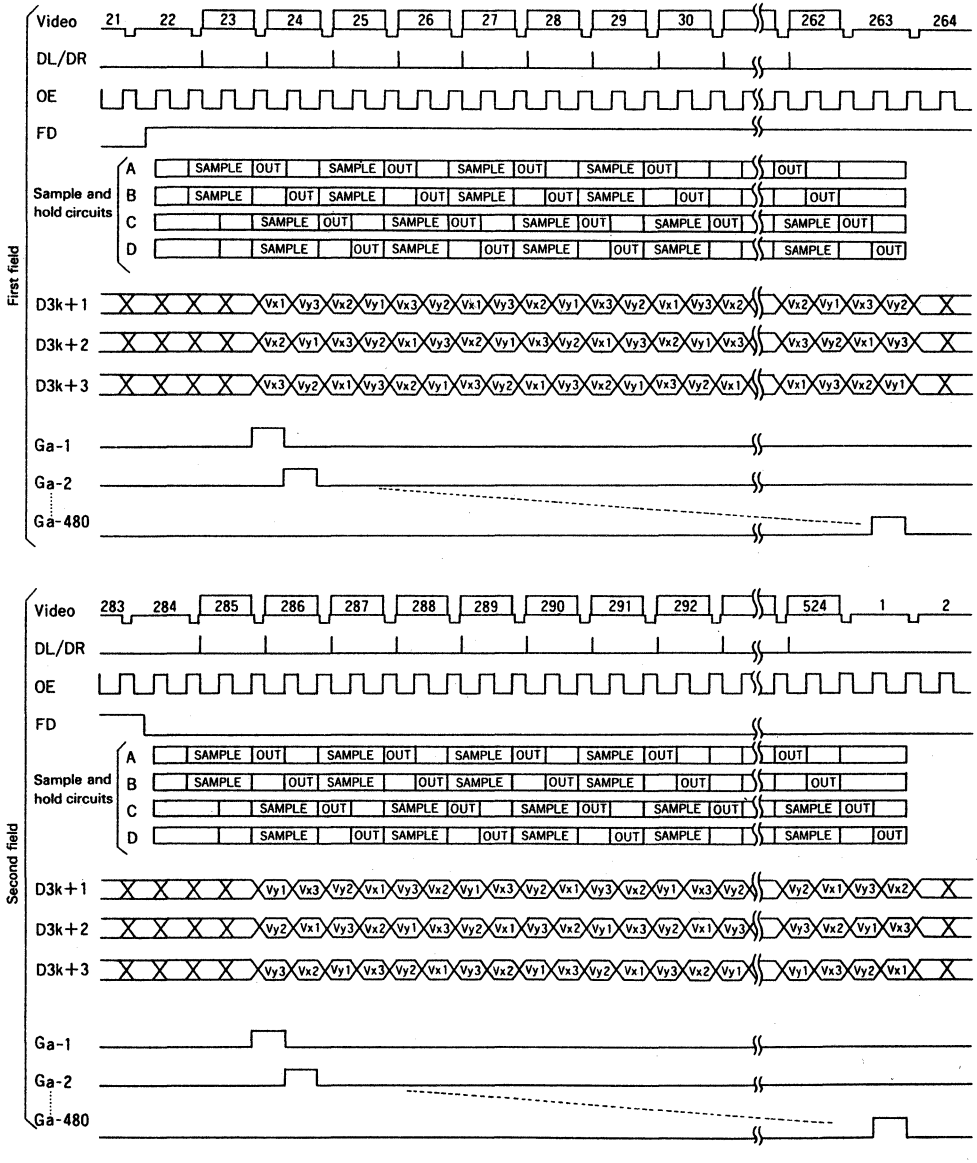
MODE 6	
D/S	V_{cc}
L/F	GND
MSF1	GND
MSF2	GND



MODE 7	
D/S	V_{cc}
L/F	GND
MSF1	V_{cc}
MSF2	V_{cc}



MODE 8	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	V_{cc}



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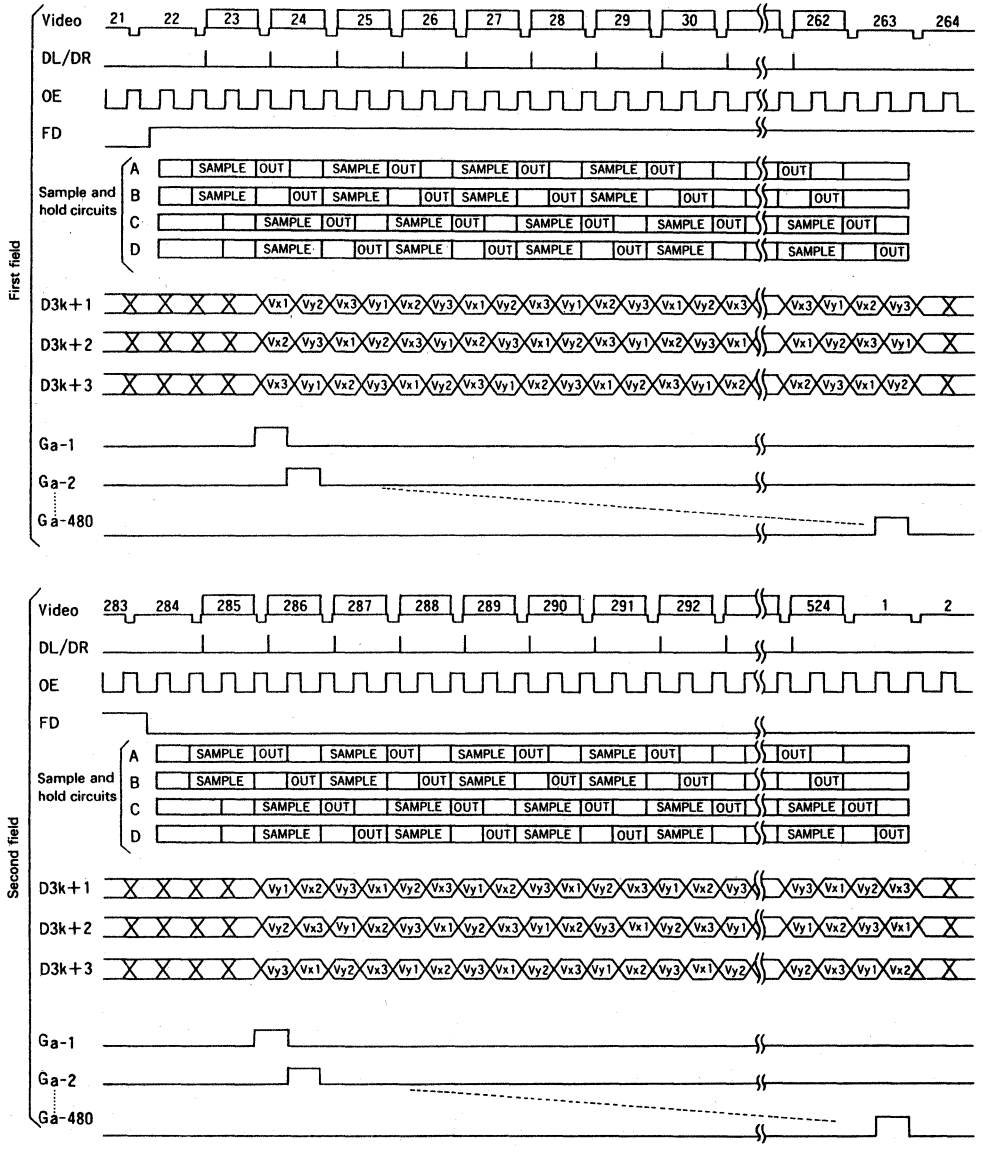
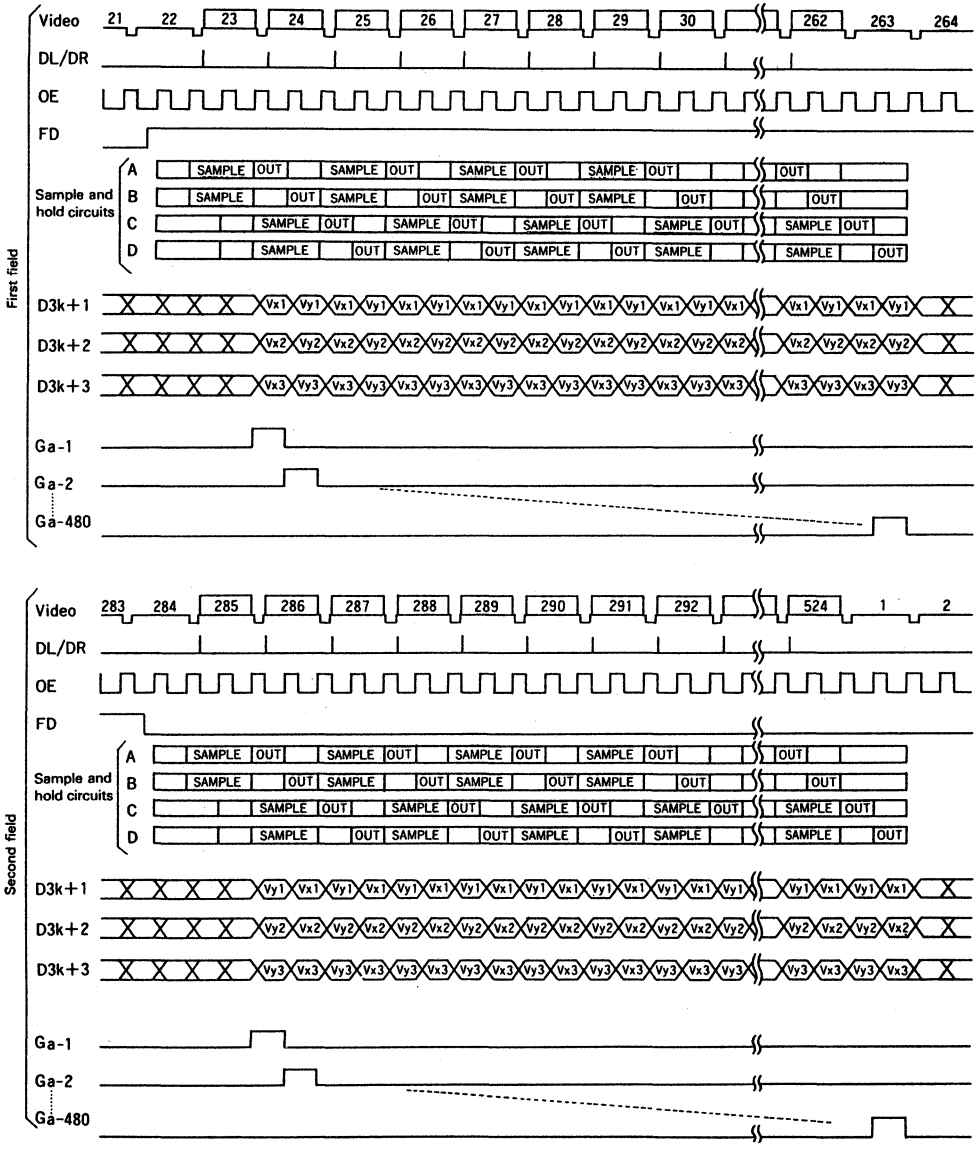
MODE 9	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	GND



MODE10	
D/S	V_{cc}
L/F	V_{cc}
MSF1	V_{cc}
MSF2	V_{cc}



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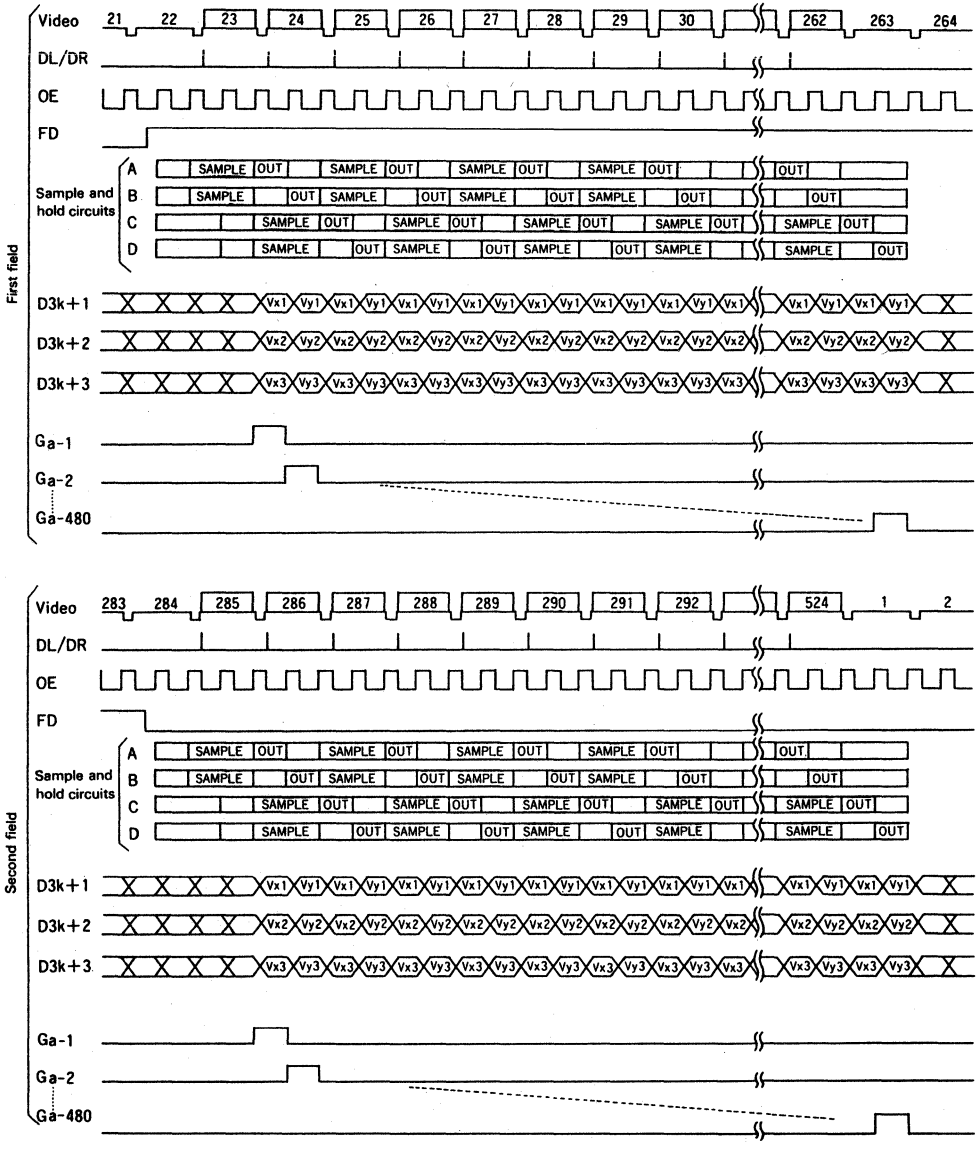
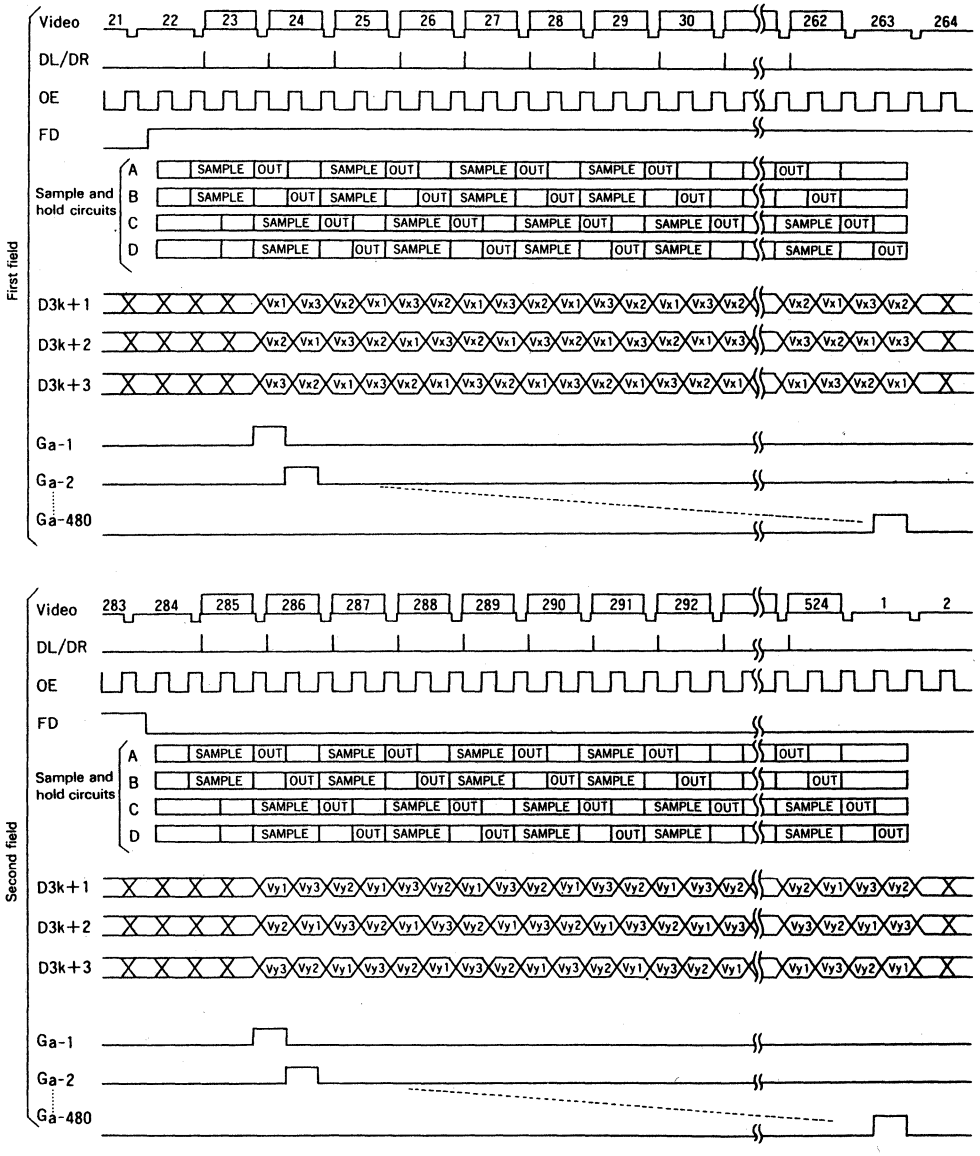
MODE11	
D/S	V_{cc}
L/F	V_{cc}/GND
MSF1	V_{cc}
MSF2	GND



MODE12	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	V_{CC}



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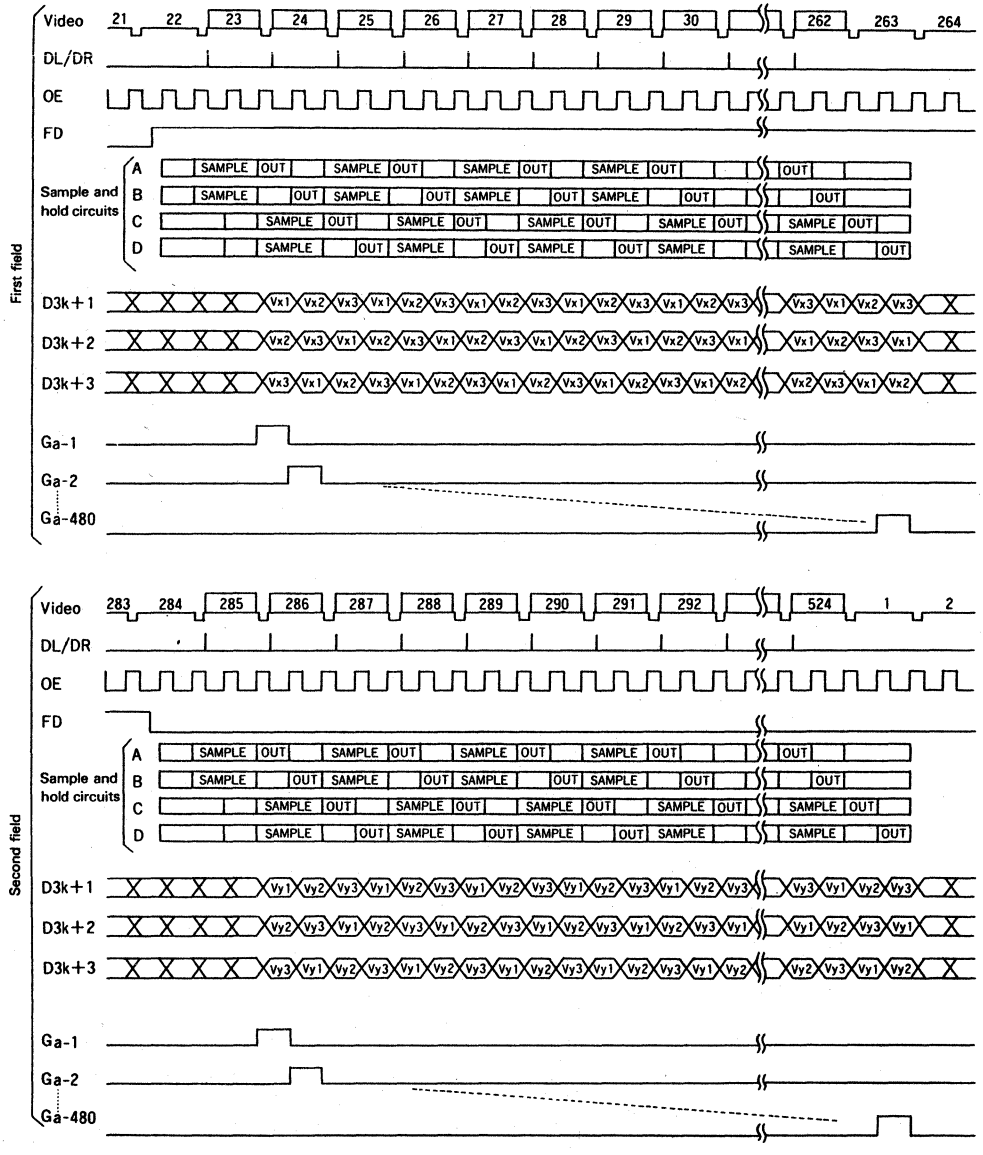
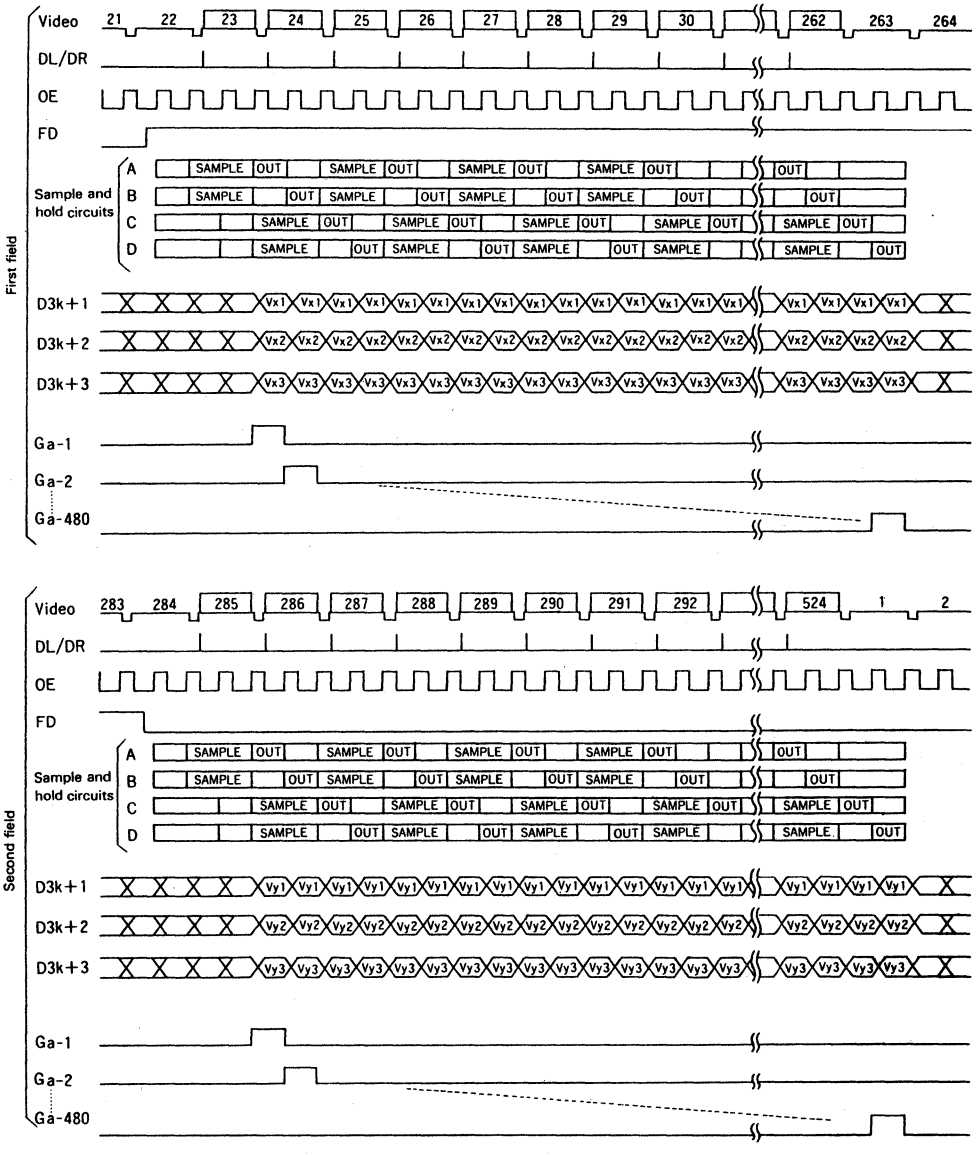
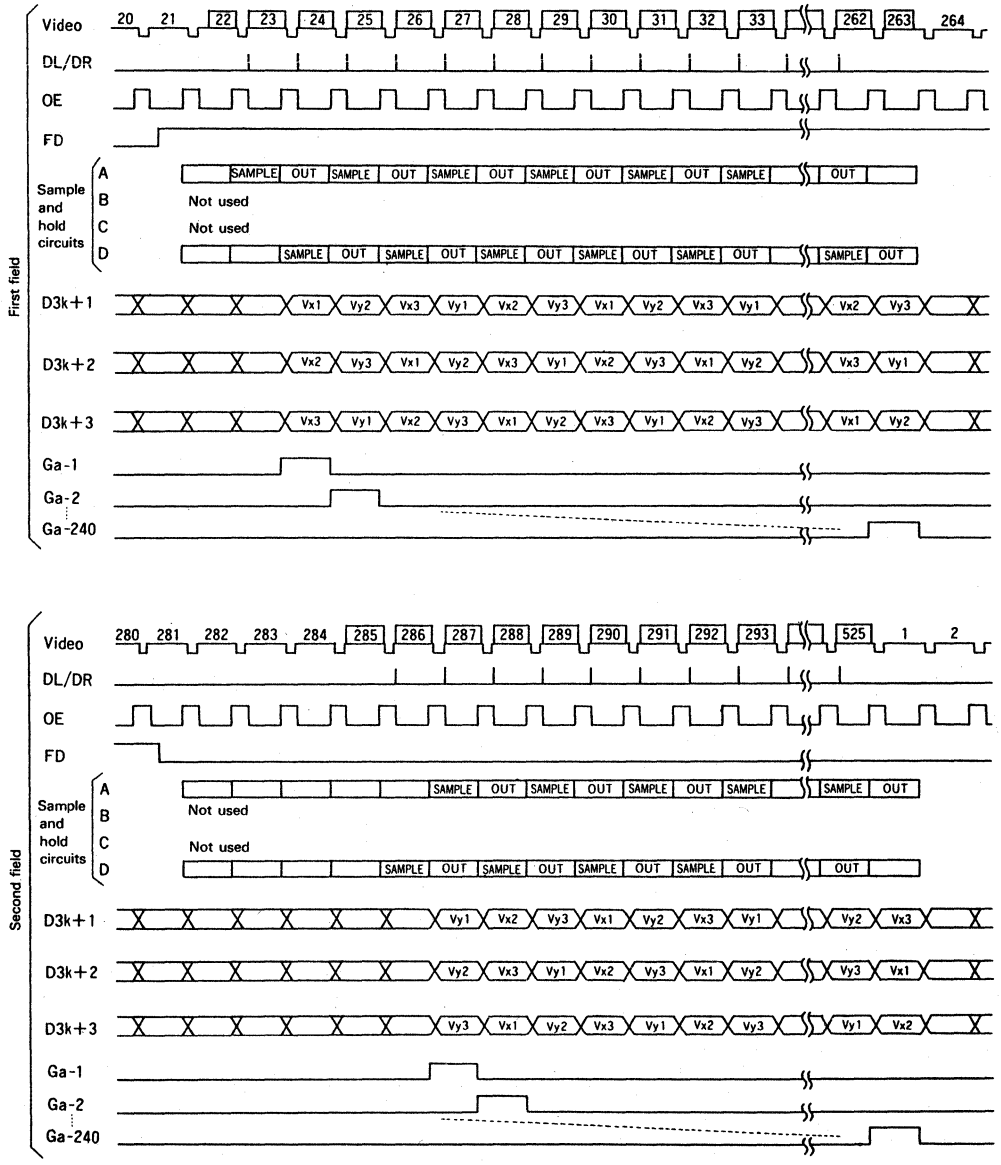
MODE13	
D/S	V_{cc}
L/F	GND
MSF1	GND
MSF2	GND



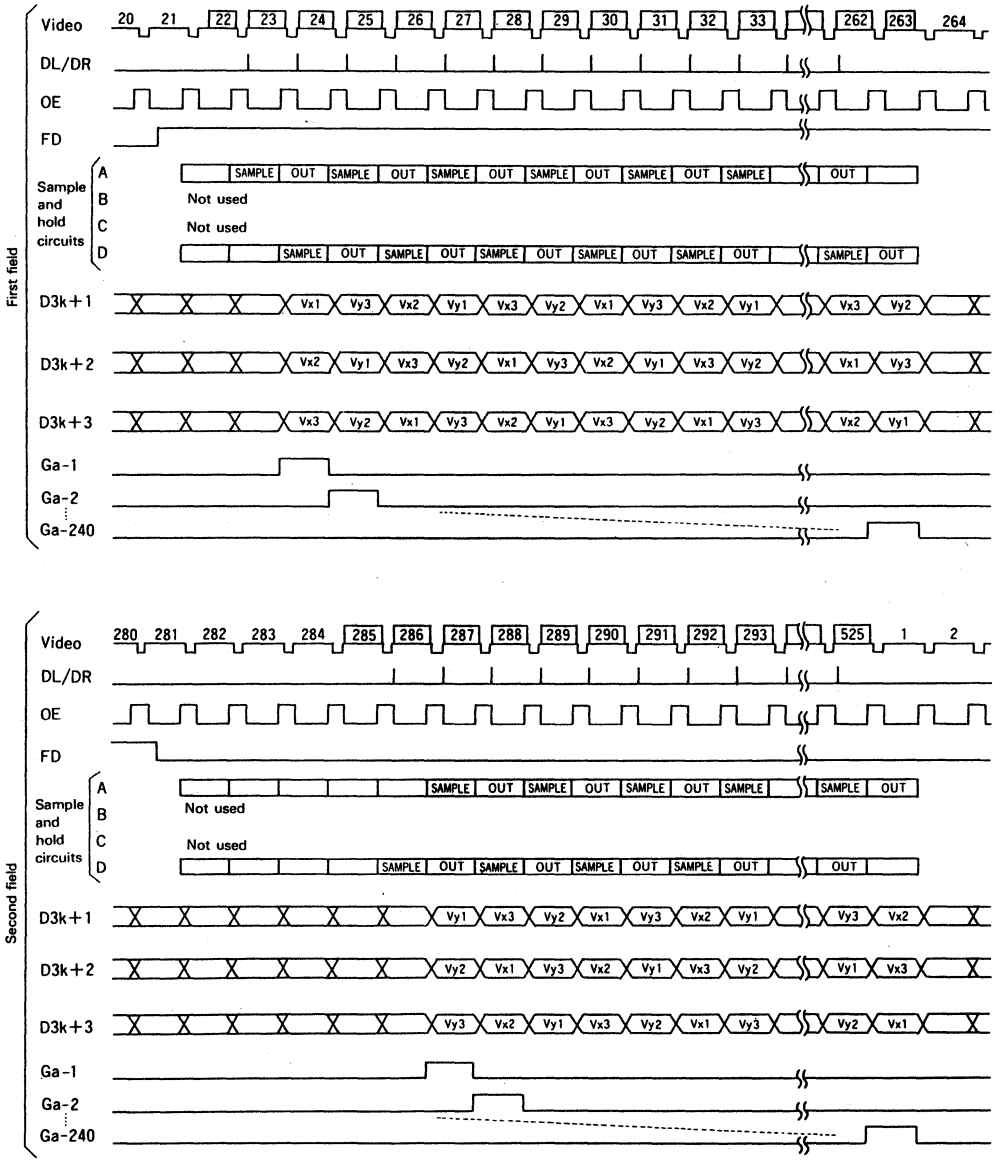
MODE14	
D/S	V_{cc}
L/F	GND
MSF1	V_{cc}
MSF2	V_{cc}



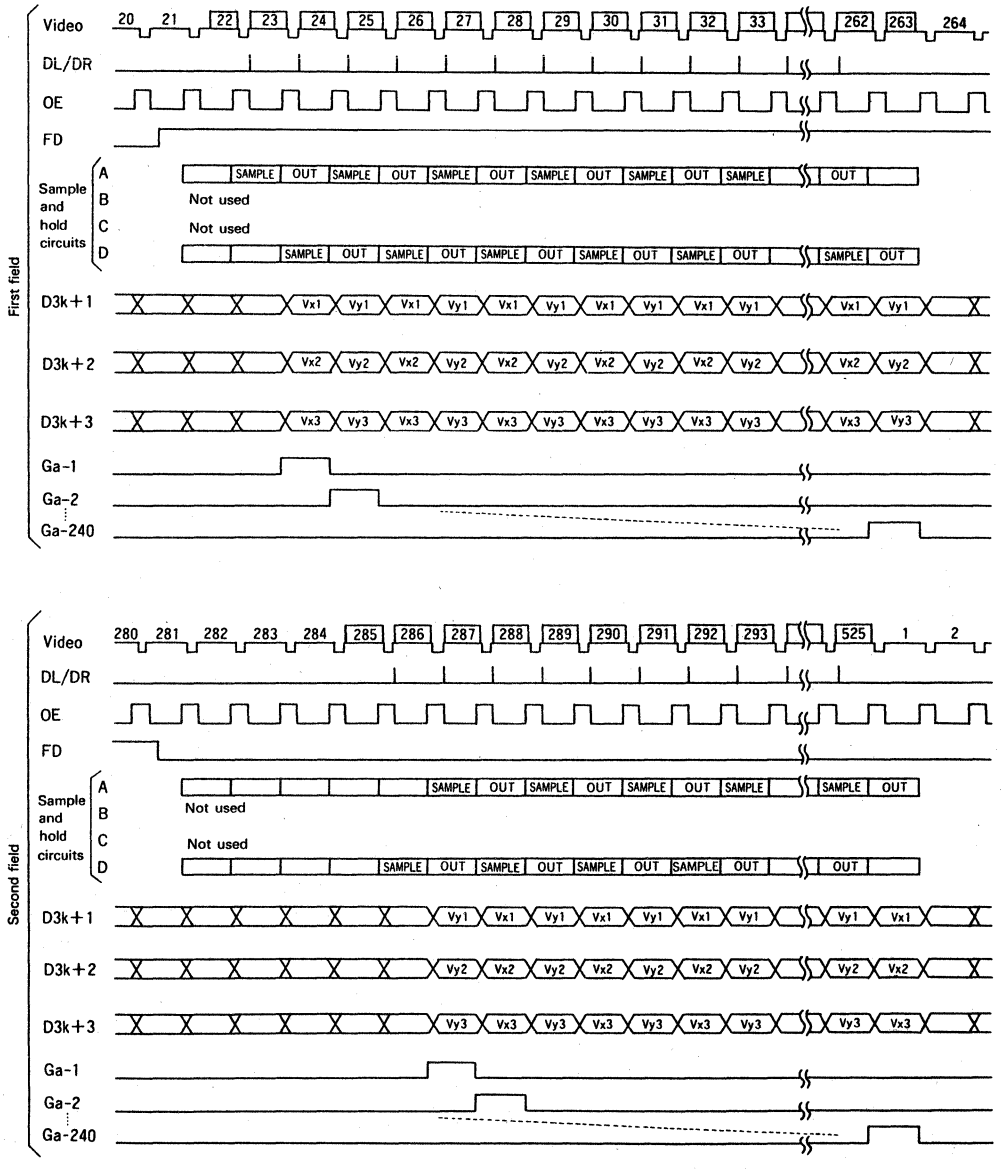
MODE15	
D/S	GND
L/F	V_{cc}
MSF1	GND
MSF2	V_{cc}



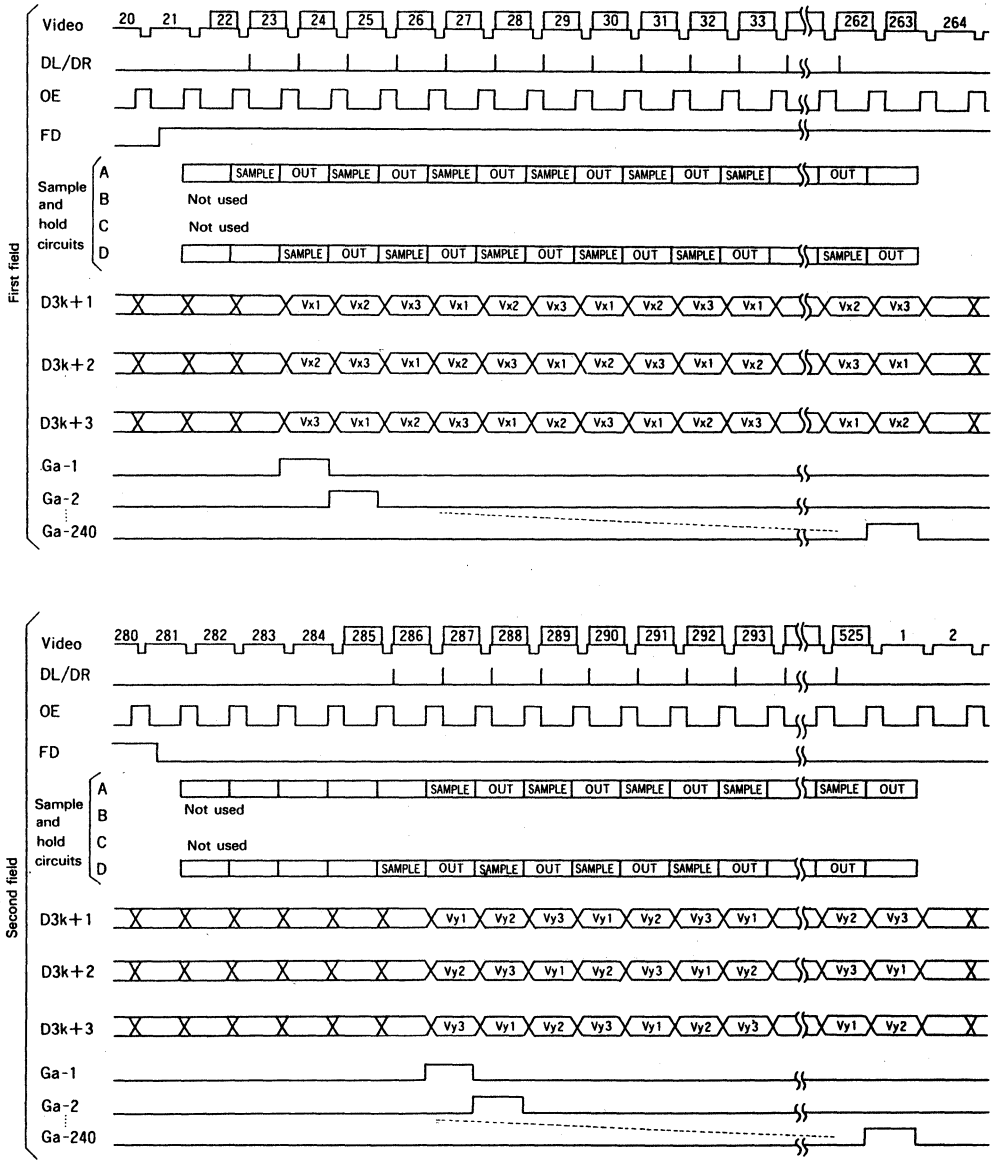
MODE16	
D/S	GND
L/F	V_{cc}
MSF1	GND
MSF2	GND



MODE17	
D/S	GND
L/F	V_{cc}
MSF1	V_{cc}
MSF2	V_{cc}



MODE18	
D/S	GND
L/F	GND
MSF1	GND
MSF2	V_{cc}



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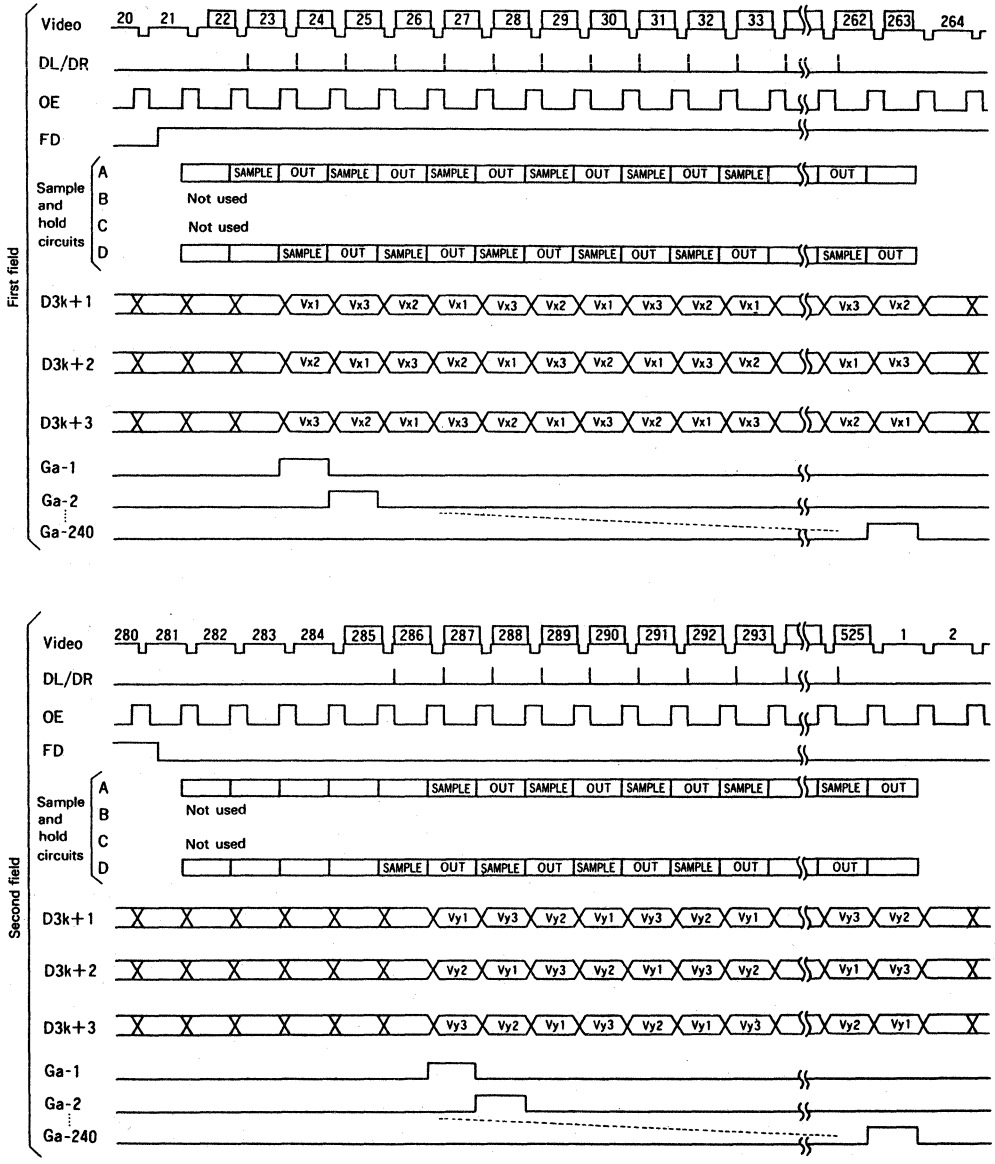
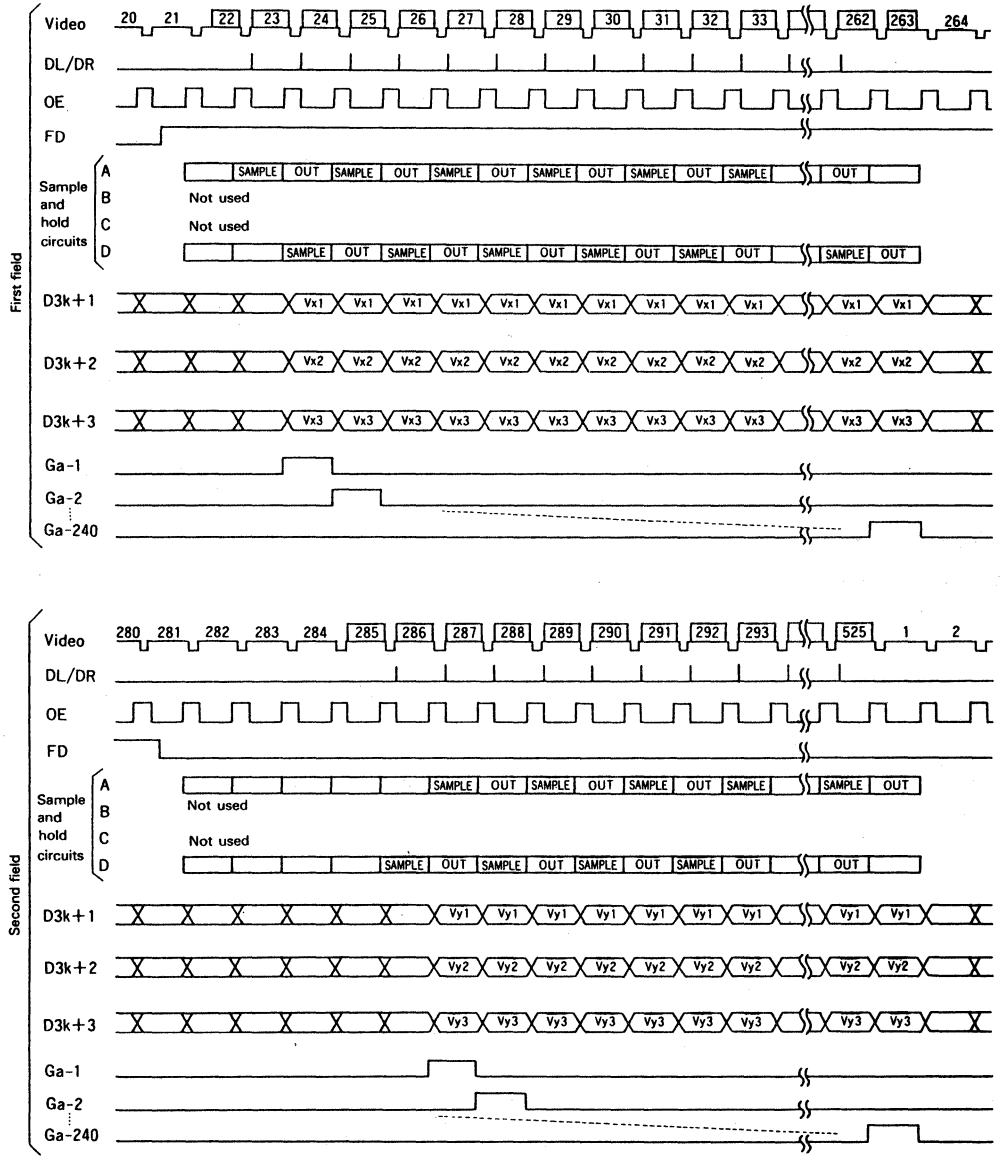
MODE19	
D/S	GND
L/F	GND
MSF1	GND
MSF2	GND



MODE20	
D/S	GND
L/F	GND
MSF1	V_{cc}
MSF2	V_{cc}



NTSC System TV Signals and LCD

A TV screen display, which is updated 30 times per second, is called a "frame" and is composed of 525 scanning lines. One frame contains two fields; scanning lines 1 to 262.5 scan the display in the first field, and scanning lines 262.5 to 525 scan the display in the second field to fill the gaps which are left unscanned in the first field. This scanning mode is called an "interlace scan."

The time period in which one scanning line scans the display is called a "horizontal scanning period" and is about 63.5 µs. Within the horizontal scanning period, the time period that display operation is actually performed is called the "valid display period". The other period is called the "horizontal retrace period".

There are two modes for displaying a TV screen image on an LCD panel. In the first mode, each scanning line in the two fields is assigned to one line of the LCD panel; thus, each of the 240 lines of the panel are driven by the positive signal in the first field and by the negative signal in the second field. Here, 30-Hz alternating frequency is available, but the number of vertical pixels is limited to 240.

(Single-rate sequential drive mode)

In the second mode, every other line of the LCD panel can be driven by the first field and the remaining lines can be driven likewise by the second field. In this case, if one pixel of the LCD panel is considered, it is recognized that the pixel is driven by signals with opposite polarity every frame. This lowers the alternating frequency to 15 MHz, which is only half of the frame frequency. Driving LCD elements with signals of such low alternating frequency causes flickering and degrades display quality. To raise the alternating frequency to 30 MHz, a method can be employed in which LCD elements are driven once every field instead of once every frame.

Specifically, in the first field, the first and second lines of the LCD panel are driven respectively during the first half and second half of the complete horizontal scanning period. The same rule is repeated for the following lines. In the second field, on the other hand, the combination of two lines is different. The first line is driven during the second half of the horizontal scanning period, and then the second and third lines are driven respectively during the first and second half of the following horizontal scanning period. The same rule is repeated for the following lines.

Employing this method enables the implementation of 480 vertical pixels.

(Double-rate sequential drive mode)

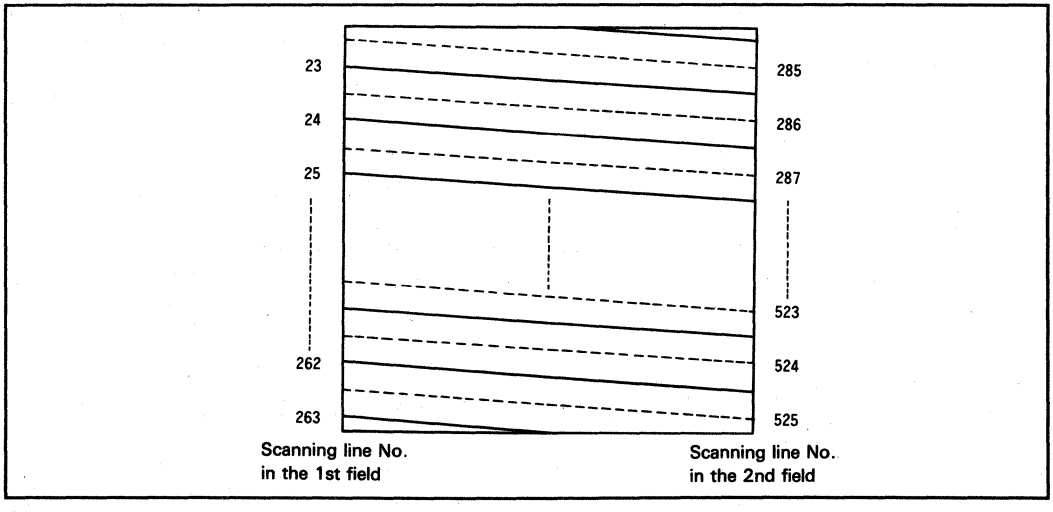


Figure 24 Example of NTSC System TV Signals Scanning

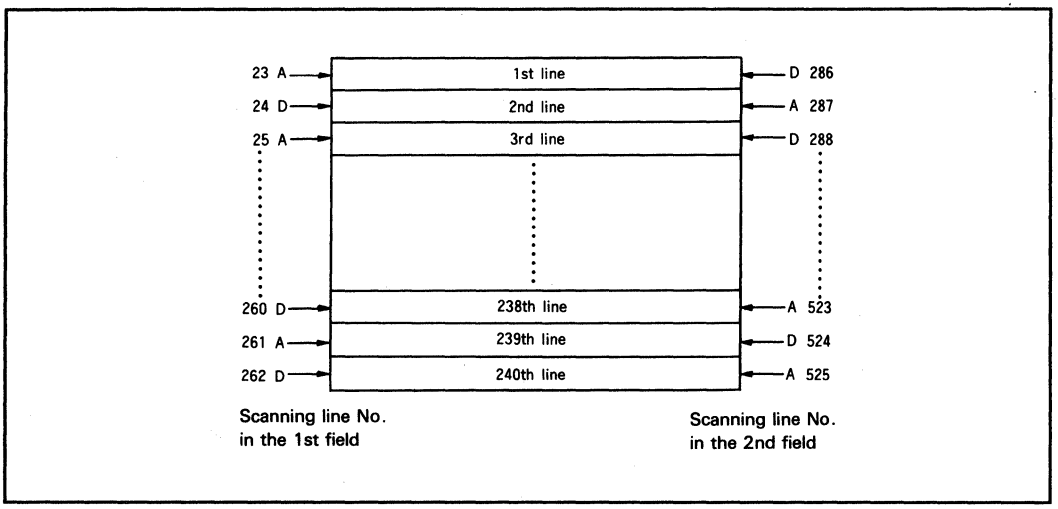


Figure 25 Middle-Resolution Display by Single-Rate Sequential Drive Mode

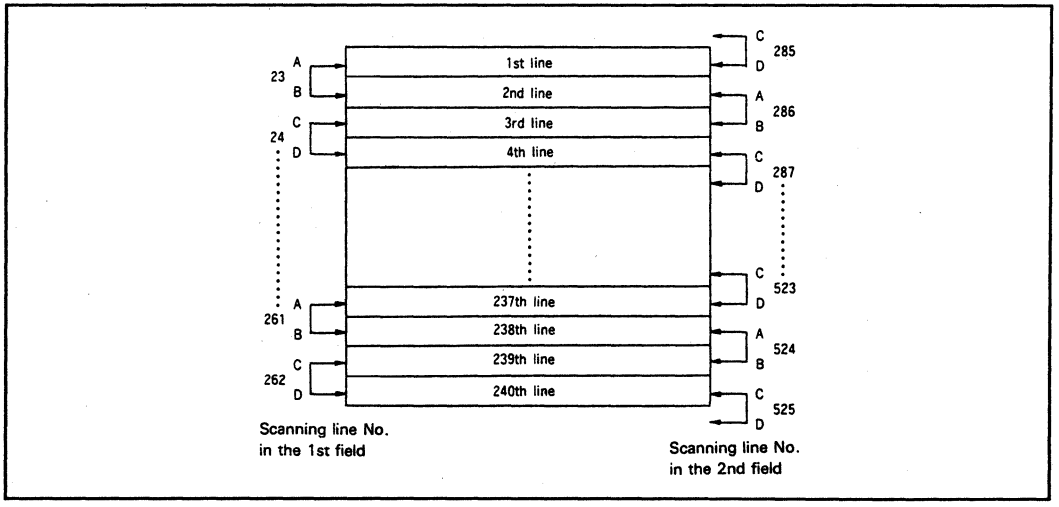


Figure 26 High-Resolution Display by Double-Rate Sequential Drive Mode

7

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit Remarks	Note
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V	
Power supply for analog unit	V_{BB}	V_{CC}– 23 to V_{CC}+ 0.3	V	
Input voltage for logic unit	V_{TC}	–0.3 to V_{CC}+ 0.3	V	3
Input voltage for analog unit	V_{TB}	V_{BB}– 0.3 to V_{CC}+ 0.3	V	4
Operating temperature	T_{opr}	–20 to +75	° C	
Storage temperature	T_{stg}	–20 to +85	° C	
LCD level voltage	V_{LCD}	$V_{BB}$to V_{CC}+ 0.3	V	

Notes:
1. Value referred to GND = 0 V.
2. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, Vbo, VbsH, and VbsB.
4. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.

Electrical Characteristics

DC Characteristics ($V_{LCD} = V_{CC} = 5\ V \pm 10\%$, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, Ta = –20 to +75 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions			Notes
Input high-level voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V				3
Input low-level voltage	V_{IL}	GND	—	0.3V_{CC}	V				
Output high-level voltage	V_{OH}	V_{CC} – 0.4	—	—	V	$-I_{OH} = 0.3$ mA			4
Output low-level voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 0.3$ mA			
Input leakage current (1)	I_{LI1}	–10	—	+10	µA	$V_I = 0$ V, V_{CC}			1
Input leakage current (2)	I_{LI2}	–10	—	+10	µA	$V_I = V_{BB}$, V_{CC}			2
Output current (1)	I_{OUT}	—	—	–150	µA	$V_{CC} - V_{BB} = 20$ V	Dk = V_{in} – 0.5 V	OE = V_{CC}	5
		—	—	–10	µA	Apply V_{in} to Vx and Vy.			
						$V_{in} = (V_{CC} - V_{BB})/2$		OE =GND	
Output current (2)	I_{IN}	+150	—	—	µA	$V_{bo} = V_{CC} - 3$ V	DK = V_{in} + 0.5 V	OE = V_{CC}	
		+10	—	—	µA	$V_{bsH} = V_{CC} - 3$ V			
						$V_{bsB} = V_{CC} - 3$ V		OE =GND	
Current consumption	I_{GND}	—	—	3.0	mA	$f_{ck} = 2.5$ MHz, $V_{bo} = V_{CC} - 3$ V			6
	I_{BB}	—	15	30	mA	$V_{bsH} = V_{CC} - 3$ V, $V_{bsB} = V_{CC} - 3$ V			
						OE = 33 kHz,			
						FD = 30 Hz			
						OE duty = 7/32			
Bias voltage	V_b	$V_{CC} - 4.0$	$V_{CC} - 3.0$	—	V	$V_{bo} = V_{bsH} = V_{bsB}$,			
						$C_L = 100$ pF, $t_{DDR} \leqq 6.3$ µs			
Dynamic range	V_{DY}	$V_{BB} + 1.5$	—	$V_{CC} - 3.5$	V	$V_{CC} - V_{BB} = 20$ V,			5, 7, 9
						$T_a = -10$ to +60°C			
						$-0.5\ V < V_{off} < +0.5$ V			
						$V_{bo} = V_{bsH} = V_{bsB} = V_{CC} - 3$ V			

DC Characteristics ($V_{LCD} = V_{CC} = 5\ V \pm 10\%$, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, Ta = –20 to +75 °C) (Cont.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions		Notes
Offset voltage	$V_{off\ (L)}$	–5 – 180	—	–5 + 180	mV	$V_{CC} - V_{BB} = 20$ V $T_a = -10$ to + 60°C $f_{ck} = 2.5$ MHz $V_{bo} = V_{bsH} = V_{bsB}$ $= V_{CC} - 3$ V	$V_{in} = -11$ V	5, 8, 9
	$V_{off\ (H)}$	+55 – 180	—	+55 + 180	mV		$V_{in} = -1$ V	

Notes:
1. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, V_{bo}, V_{bsH}, and V_{bsB}.
2. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, and TEST2.
4. Applies to pins DL and DR.
5. Applies to pins D1 - D120.
6. The shift register is constantly shifting one 1.
   Mode setting: L/F = V_{CC}, D/S = V_{CC}, MSF1 = GND, MSF2 = V_{CC}
   (The other input pins must be V_{CC} or GND level.)
7. The operations are the same as those when offset voltage is measured.
8. Definition of "offset voltage" is shown figure 27.
9. These characteristics are defined within the temperature which is shown in the test condition.

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AC Characteristics ($V_{LCD} = V_{CC} = 5\ V \pm 10\%$, GND = 0 V, $V_{CC} - V_{BB}$ = 16 to 20 V, T_a = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Test Condition	Notes
Three-phase clock period	t_{CKCK}	210	1000	ns		
Three-phase clock pulse width	t_{CWH} t_{CWL}	100	—	ns		
Interval between three-phase clock falling edge and rising edge	t_{fr1} t_{fr2} t_{fr3}	30	—	ns		1
Interval between three-phase clock rising edge and falling edge	t_{rf}	20	—	ns		2
Clock rise and fall times	t_{ct}	—	30	ns		
DL, DR input setup time	t_{su}	50	—	ns		
DL, DR input hold time	t_{HLI}	20	—	ns		
DL, DR output delay time	t_{pd}	—	90	ns	C_L = 15 pF	
DL, DR output hold time	t_{HLO}	5	—	ns		
OE input period	t_{CYCO}	30	80	µs		
OE input high-level pulse width	t_{OWH}	3	15	µs		
OE rise and fall times	t_{or} t_{of}	—	30	ns		
FD input setup time	t_{FS}	100	—	ns		
FD input hold time	t_{FH}	100	—	ns		

Note: 1. Necessary for preventing the three-phase shift register from racing.
2. t_{rf} must satisfy the DR and DL input hold time (t_{HLI}) of the next horizontal driver.
($t_{rf} + t_{HLO} > t_{HLI}$)

7

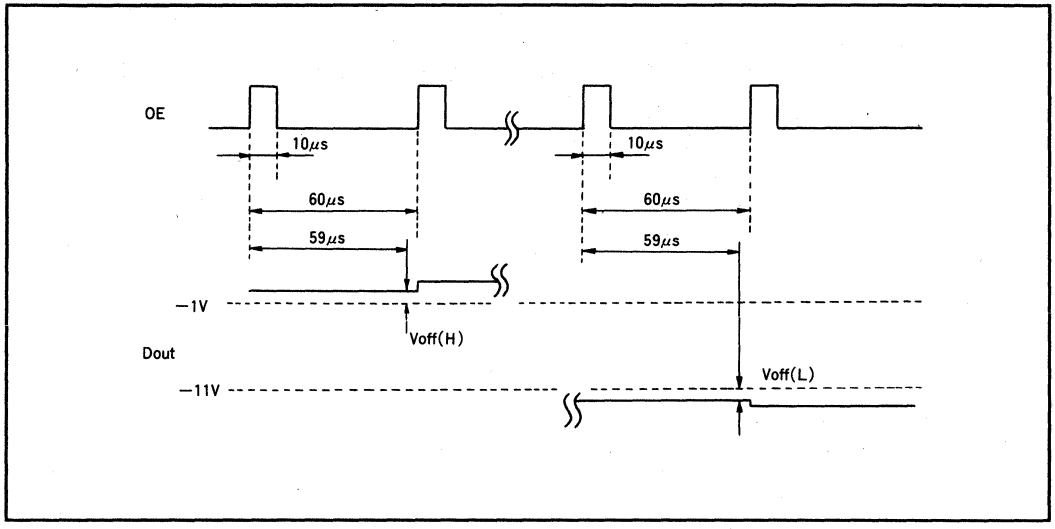

Figure 27 Offset Voltage

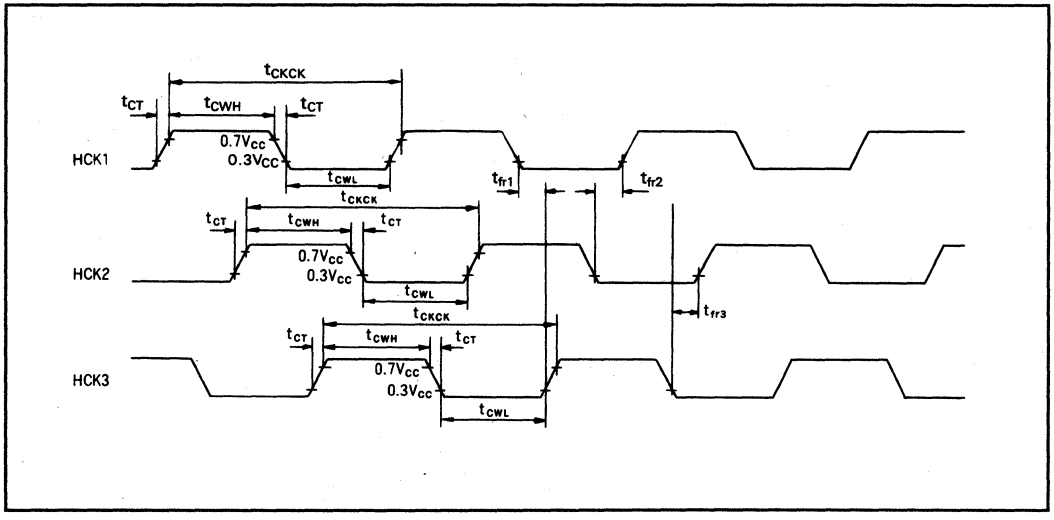

Figure 28 Three-Phase Clock Timing

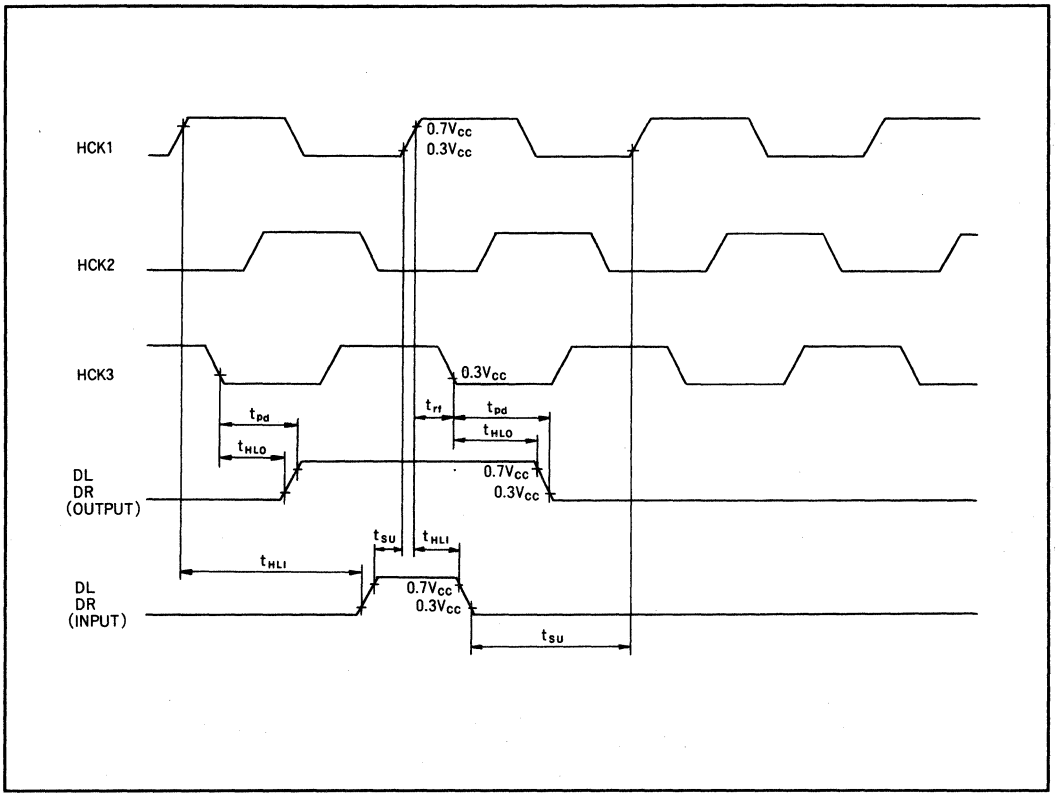

Figure 29 Input and Output Timing

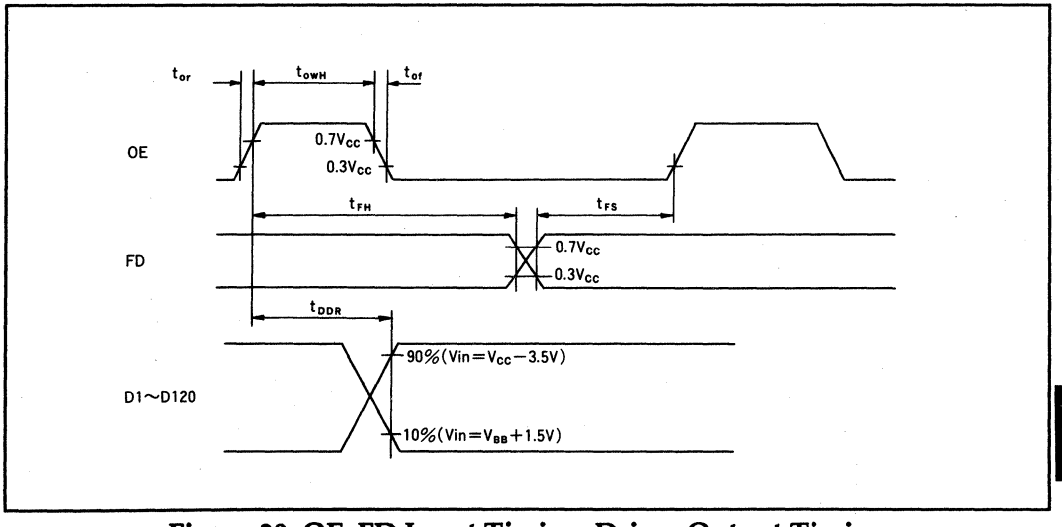

Figure 30 OE, FD Input Timing, Driver Output Timing

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HD66310T
(TFT-Type LCD Driver for VDT)

Description

The HD66310T is a drain bus driver for TFT-type (thin film transistor) LCDs. It receives 3-bit digital data for one dot, selects a level from eight voltage levels, and outputs the level to an LCD.

The HD66310T can drive an LCD panel with an RGBW filter to display a maximum of 4096 colors.

Features

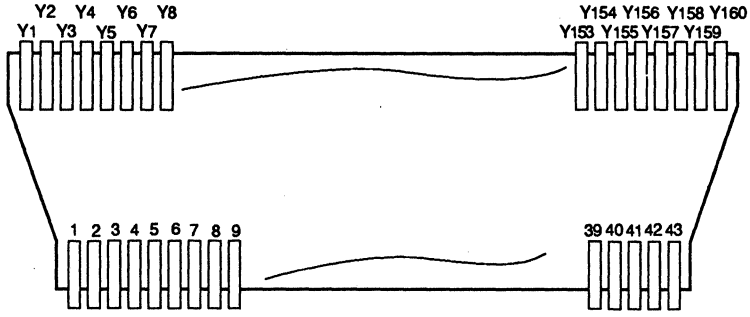
- Full color display: a maximum of 4096 colors
  RGB color-filter: 512 colors, 8 gray scales
  RGBW color filter: 4096 colors, 8 gray scales
- High-speed operation
  Number of input data bits: 3 bits × 4
  Maximum operation clock frequency:
  — 12 MHz (HD66310T**12)
  — 15 MHz (HD66310T**15)
  Maximum pixels: 480 × 640 dots
- 160 internal driver circuits
- Bidirectional shift
- Internal chip enable signal generator
- Stand-by function
- LCD driving voltage: 15 V to 23 V
- CMOS process
- Package: 203-pin TCP

Available in TCP packaging only.
Recommended for high volume applications only.

Difference between HD66310T**12 and HD66310T**15

Item	HD66310T**12	HD66310T**15
Maximum operating clock frequency	12 MHz	15 MHz
Power supply for logic unit	5 V ±10%	5 V ±5%
Operating temperature	–20 to +75°C	–20 to +65°C

Pin Arrangement



(Top view)

1	V0L	22	DMY1
2	V1L	23	D20
3	V2L	24	D21
4	V3L	25	D22
5	V4L	26	D23
6	V5L	27	DMY2
7	V6L	28	CL1
8	V7L	29	CL2
9	V_{CC1}	30	BS
10	V_{CC2}	31	SHL
11	EIO1	32	EIO2
12	$\overline{RVS}$	33	TEST
13	D00	34	GND
14	D01	35	V_{EE}
15	D02	36	V7R
16	D03	37	V6R
17	DMY0	38	V5R
18	D10	39	V4R
19	D11	40	V3R
20	D12	41	V2R
21	D13	42	V1R
		43	V0R

Note: This does not apply to TCP dimensions.

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Functions (Refer to)
$V_{CC}1$, $V_{CC}2$	2	Power supply	1.
GND	1	Power supply	
V_{EE}	1	Power supply	
V0L–V7L, V0R–V7R	16	Power supply	2.
CL1	1	Input	3.
CL2	1	Input	4.
D00, D10, D20, to D03, D13, D23	12	Input	5.
$\overline{RVS}$	1	Input	6.
SHL	1	Input	7.
EIO1, EIO2	2	Input/output	8.
TEST, BS	2	Input	9.
Y1–Y160	160	Output	10.
DMY0–DMY2	3	—	11.

7

Pin Functions

1. $V_{CC}1$, $V_{CC}2$, GND, V_{EE}: These pins are used for the power supply.

V_{CC}–GND: Power supply of low voltage
V_{CC}–V_{EE}: Power supply of high voltage

2. V0L–V7L, V0R–V7R: 8-level LCD driving voltage is applied to these pins. One of the eight levels is selected according to the value of the 3-bit input display data. The L and R pins of the same voltage level are connected in the driver.

3. CL1: Inputs clock pulses, which determine the output timing of the LCD driving voltage. The output changes at the CL1 rising edge.

4. CL2: Inputs clock pulses, which determine the input timing of display data. The driver samples data at the CL2 falling edge.

Table 1 Voltage Level Selection According to Display Data Value

Display Data			Voltage Level	
D2]	D1]	D0]	$\overline{RVS}$ = 1	$\overline{RVS}$ = 0
0	0	0	V0	V7
0	0	1	V1	V6
0	1	0	V2	V5
0	1	1	V3	V4
1	0	0	V4	V3
1	0	1	V5	V2
1	1	0	V6	V1
1	1	1	V7	V0

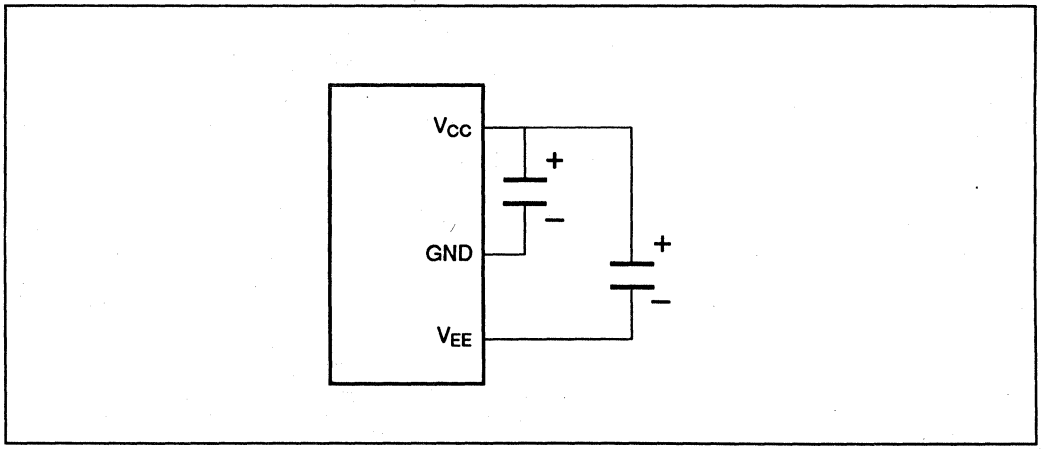


Figure 1 Power Supply for the Device

5. D00–D03, D10–D13, D20–D23: Input display data. See table 1 for the voltage level selection by the display data.

6. $\overline{RVS}$: Determines if logical I/O display data is reversed. Display data is reversed when $\overline{RVS}$ is low.

7. SHL: Selects the shift direction of display data.

8. EIO1, EIO2: Inputs/outputs chip enable signals. The SHL signal selects which pin is for input or output. When the chip enable input signal is low, data input starts. When display data corresponding to 160 outputs are input, the chip enable output signal changes from high to low.

9. TEST, BS: Used for test purposes only. Connect to a low level for normal operation.

10. Y1–Y160: Output LCD driving signals.

11. DMY0–DMY2: Reserved pins that should be left open.

Table 2 Input/Output Selection for EIO1 and EIO2

SHL	EIO1	EIO2
GND	Input	Output
V_{CC}	Output	Input

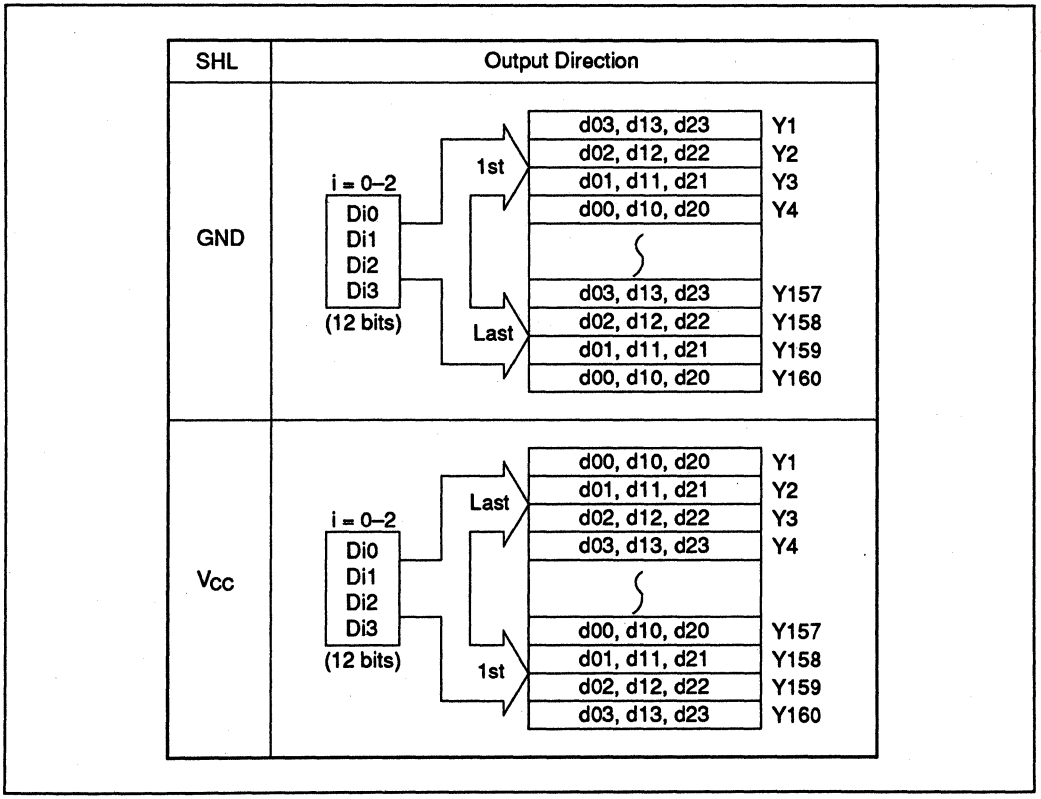
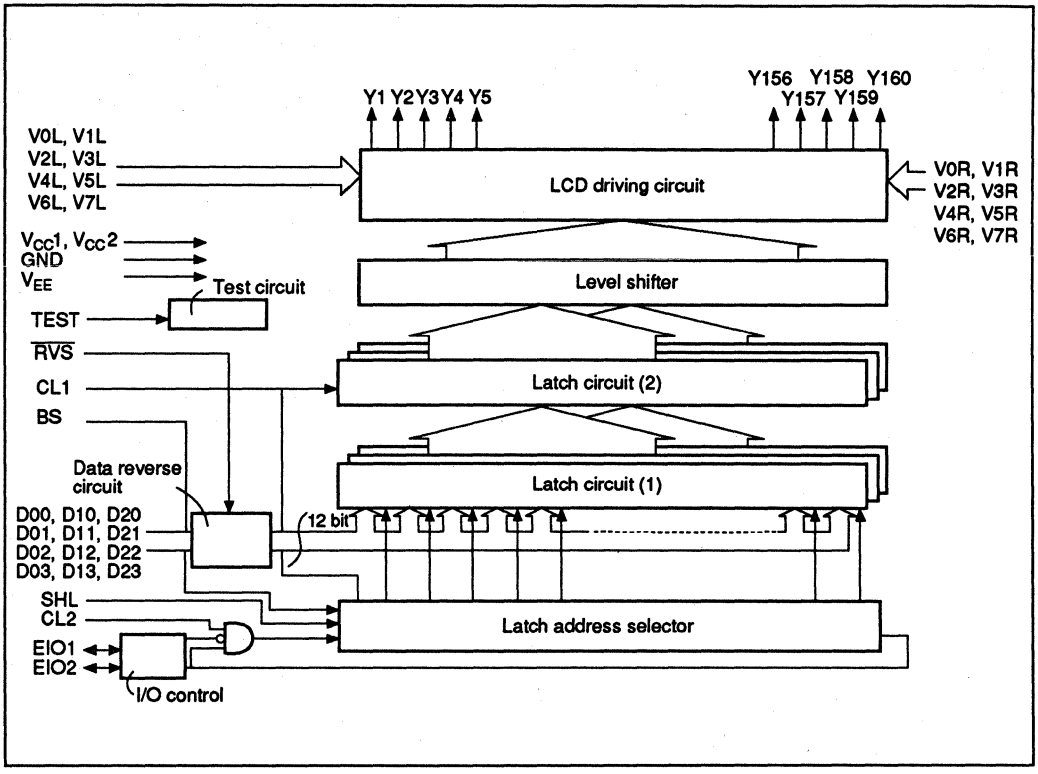


Figure 2 Display Data and Output Direction

Internal Block Diagram



Block Functions

Latch Address Selector: Contains a 6-bit up/down counter and a decoder, and sends the latch signals to latch circuit (1) at the CL2 falling edge.

Data Reverse Circuit: Reverses the input display data when $\overline{RVS}$ = 0, and does not reverse data when $\overline{RVS}$ = 1.

Latch Circuit (1): Consists of three planes of 160-bit latch circuit. Each bit of 3-bit data is separately latched in its corresponding plane depending on its significance. Each plane is divided into forty 4-bit blocks, and all four bits are latched into the block at once, as specified by the latch signal from the address selector. In total, the 3-plane circuit latches 12 bits of data at one time.

Latch Circuit (2): Consists of three planes of 160-bit latch circuit, which latches the data from latch circuit (1) at the timing determined by CL1, and holds the data for one line scanning period.

Level Shifter: Raises the driving voltage of 5 V to the appropriate LCD driving voltage.

LCD Driving Circuit: Outputs an 8-level LCD driving voltage. This circuit receives 3-bit data for one dot from latch circuit (2) and selects one level from eight voltage levels.

Test Circuit: Generates test signals.

System Configuration

A block configuration of the TFT-type color display system using the HD66310 is shown in figure 3.

The HD66310 receives 3-bit data for one pixel and selects one of the eight LCD driving voltage levels to send to the LCD. The LCD driving output circuit, which is produced by the CMOS structure, can use any LCD driving voltage level from V_{CC} to V_{EE}. When the LCD panel uses an RGB color filter (the Triad arrangement), 512 (8^3) colors can be displayed. When using an RGBW color filter (the Quad arrangement), 4096 (8^4) colors can be displayed.

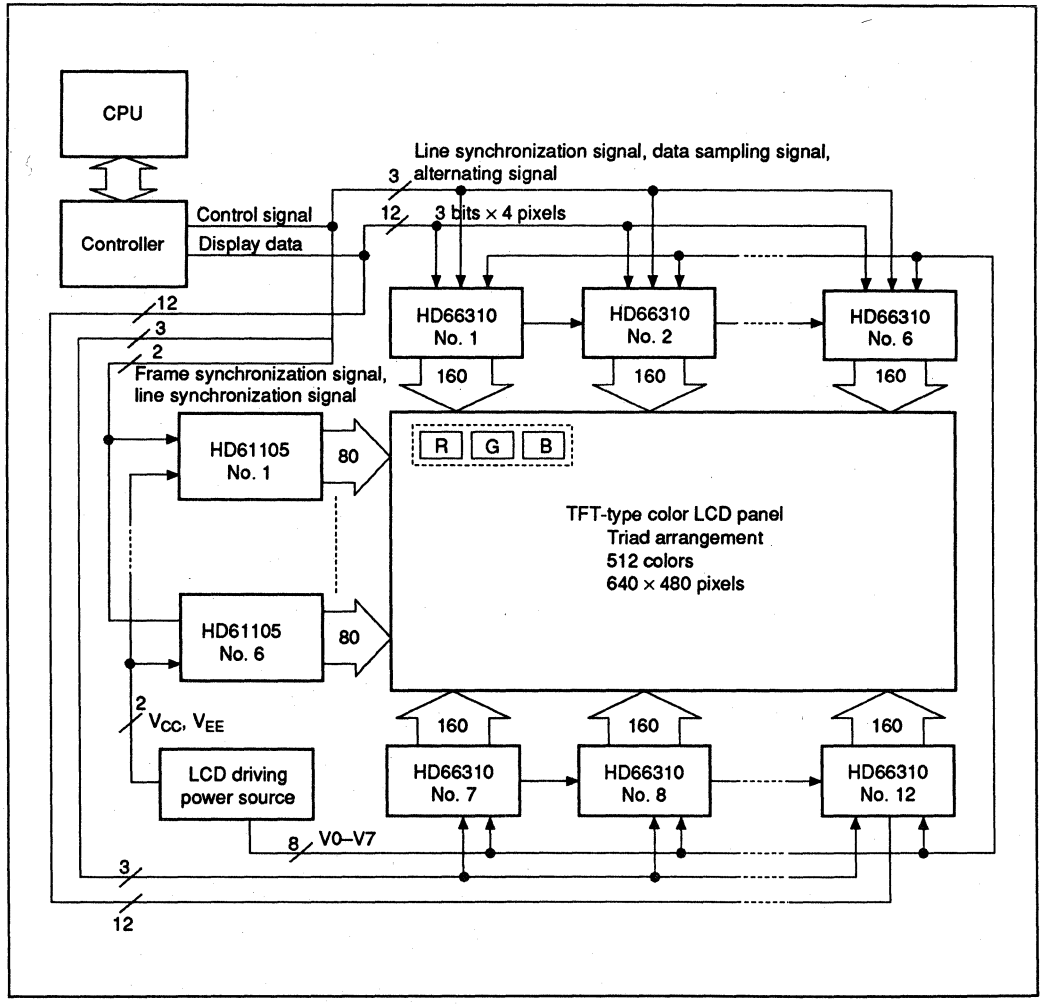


Figure 3 TFT-Type Multiple Color Display System

Internal Operation

8-Level Output

The HD66310 internal circuit unit for one data output is shown in figure 4. The circuit receives 3-bit data (D0j, D1j, D2j) and selects one of eight voltage levels (V0–V7) to output to the LCD.

The transfer gates of the output circuit are produced by the CMOS structure. Therefore, any voltage level between V_{CC} to V_{EE} can be applied to lines V0 to V7.

The HD66310 has 160 of the above circuits.

Operation Timing

The HD66310 operation timing is shown in figure 5.

When the SHL signal is at the GND level, data input is started by a low EIO1 (data input enable) signal. At the CL2 falling edge, 12 bits of data, which are for four outputs (3 bits for gray scales × 4 outputs), are input together. When the data input corresponding to 160 outputs are completed, the HD66310 automatically enters the stand-by mode, and the EIO2 signal changes to low.

The LCD driving output changes at the CL1 rising edge. The voltage level selected by data d1 is output from pin Y1, and the level selected by d160 is output from Y160. See table 1 for the voltage level selection by the input data.

When the SHL signal is at the V_{CC} level, data input is started by a low EIO2 signal. When the data input for 160 outputs are completed, the EIO1 signal changes to low. The voltage level selected by data d1 is output from pin Y160, and the level selected by d160 is output from Y1.

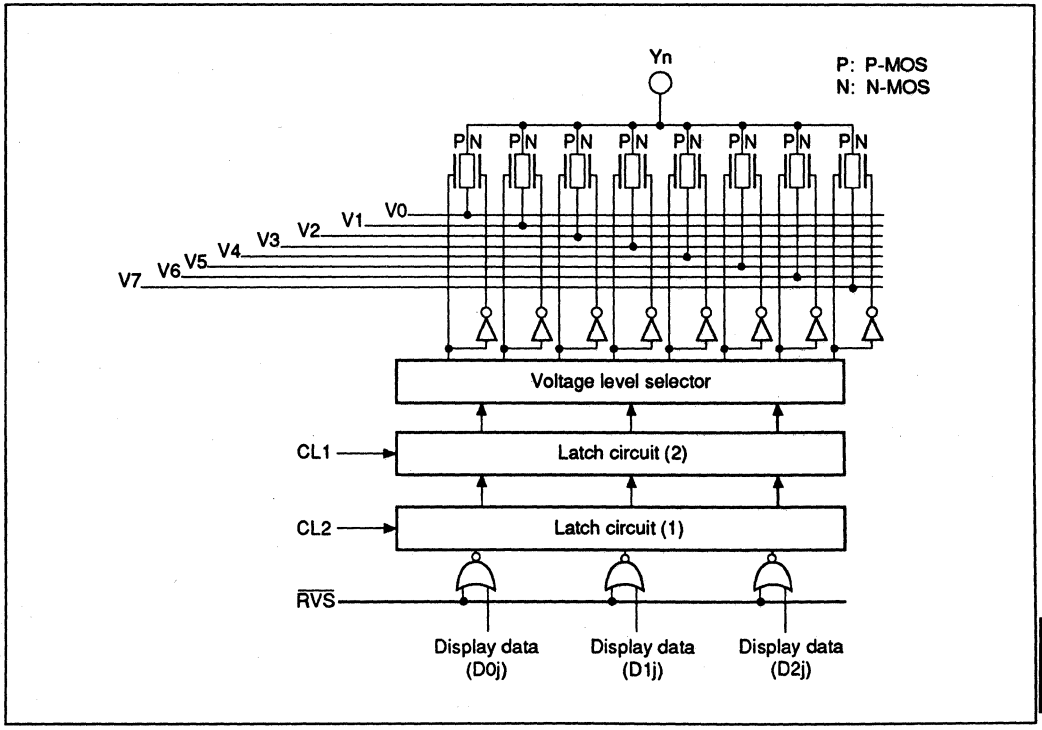


Figure 4 LCD Driving Circuit

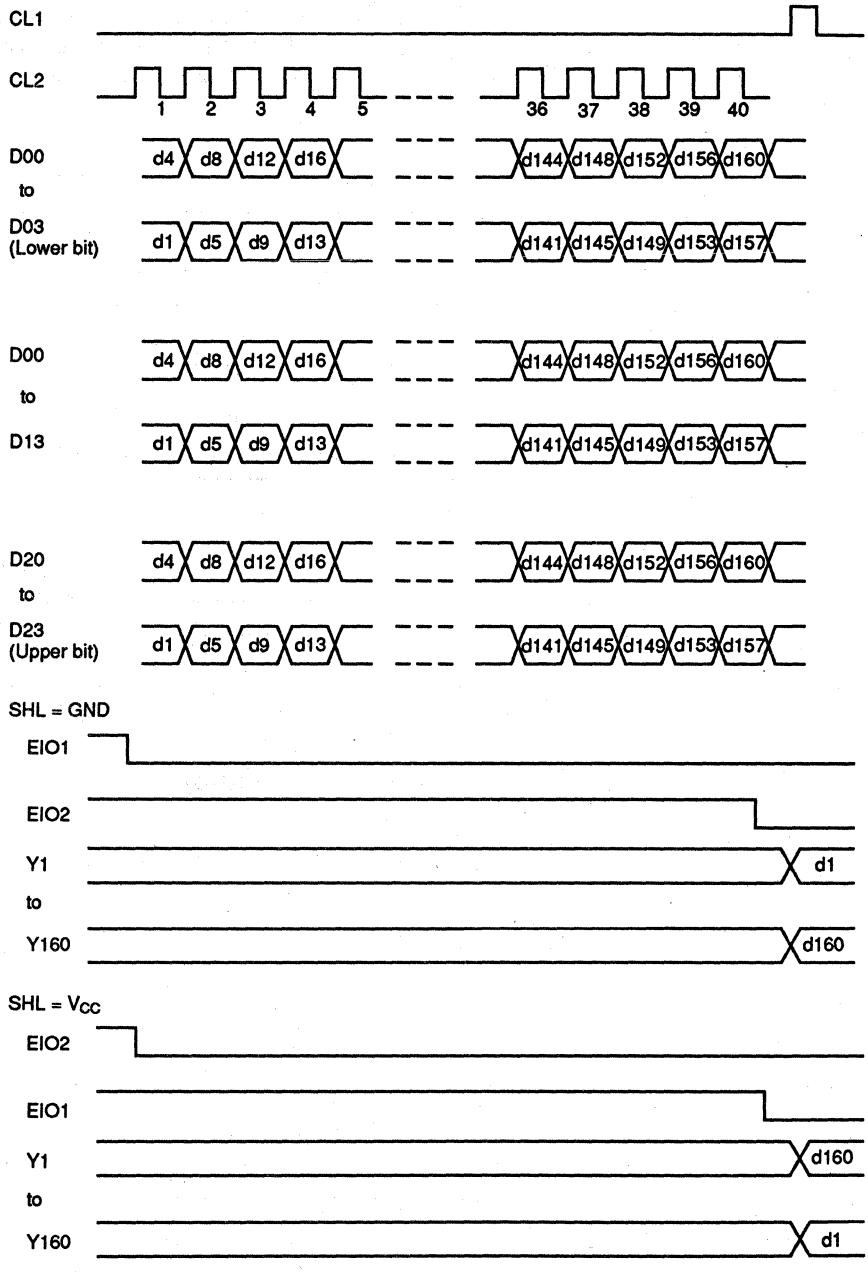


Figure 5 Basic Operation Timing Chart

Cascade Connection

When the SHL signal is at the GND level, the HD66310 begins to input data when the EIO1 signal goes low. When the data input is completed, the EIO2 signal changes to low. By connecting the EIO2 pin of the first HD66310 to the EIO1 pin of the next HD66310, the low EIO2 signal activates the next HD66310. Figure 6 shows a connection example.

When the SHL signal is at the V_{CC} level, the EIO2 pin of the first HD66310 is connected to GND, and the EIO1 pin is connected to the next HD66310 EIO2 pin.

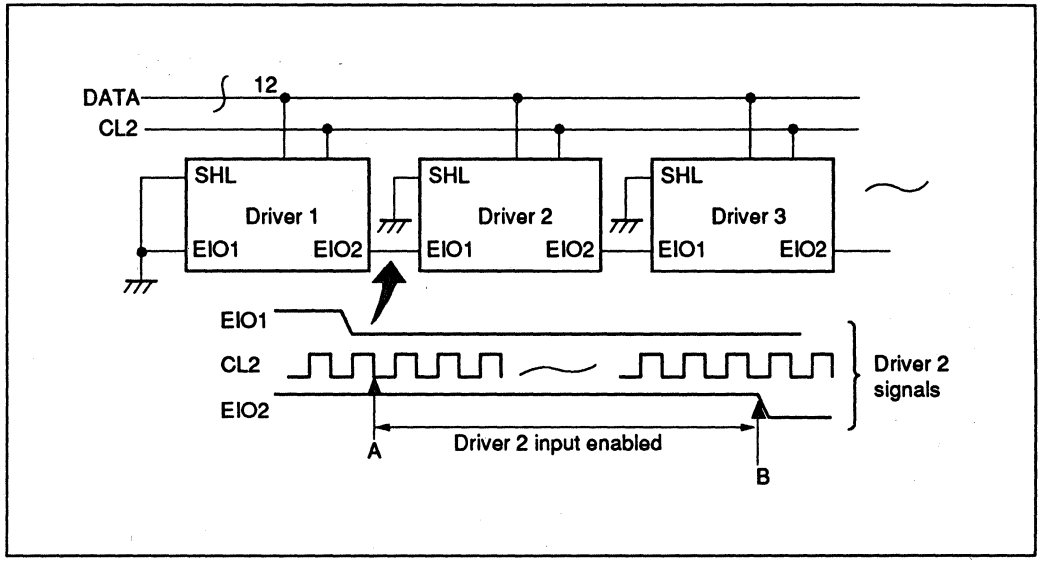


Figure 6 Chip Enable Operation (SHL = GND)

7

LCD Driving Power Supply Circuitry

Multiple-Level Driving Voltage Method

AC voltage must be applied to the LCD, since DC voltage deteriorates the LCD. To display eight gray scales, 16 voltage levels, shown in figure 7, must be applied.

Although the HD66310 has eight LCD driving voltage input levels, it can output 16 driving voltage levels using the level selector shown in figure 8, since the transfer gates of the output circuit are produced by the CMOS structure.

External Power Supply Circuitry

Figures 8 and 9 show the external power supply circuit when displaying 512 colors in the Triad arrangement, and figure 10 shows the circuit for displaying 64 colors in the Triad arrangement. Table 3 shows the specifications of the LCD panel and the HD66310 pins for each power supply circuit.

The circuit shown in figure 8 is the basic one used when displaying 512 colors in the Triad arrangement. However, the HD66310 can dispense with the level selector, as shown in figure 9, using the internal $\overline{RVS}$ (output reverse) pin. See table 1 for detailed $\overline{RVS}$ functions.

When displaying 64 colors in the Triad arrangement, the $\overline{RVS}$ pin functions as the alternating signal input pin, as shown in figure 10.

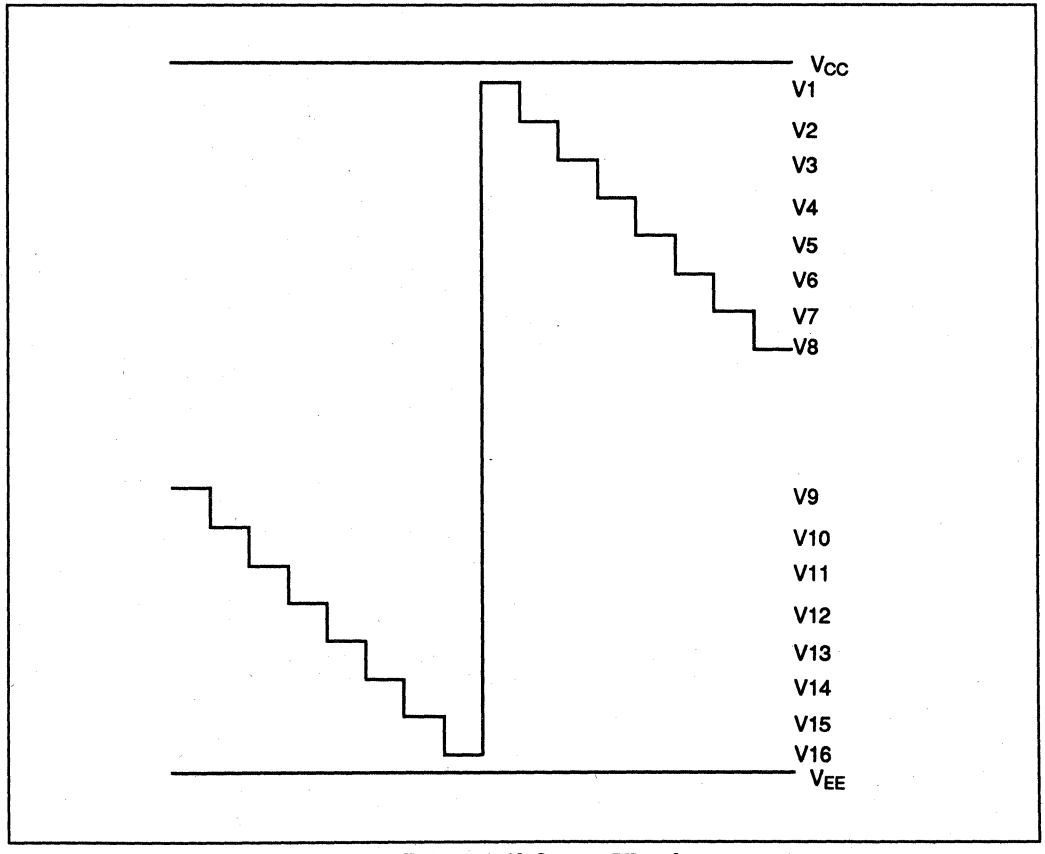


Figure 7 HD66310 Output Waveform

Table 3 Color Display and Pin Specifications

Output Level	Panel Spec.	Display Data DI2	DI1	DI0	$\overline{RVS}$ pin	Power Supply (Refer to)
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	1	Fig. 8
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	Alternating signal	Fig. 9
4 × 2 (AC)	Quad: 256 colors Triad: 64 colors	1	1/0 (upper bit)	1/0 (lower bit)	Alternating signal	Fig. 10

1: V_{CC} level voltage
0: GND level voltage

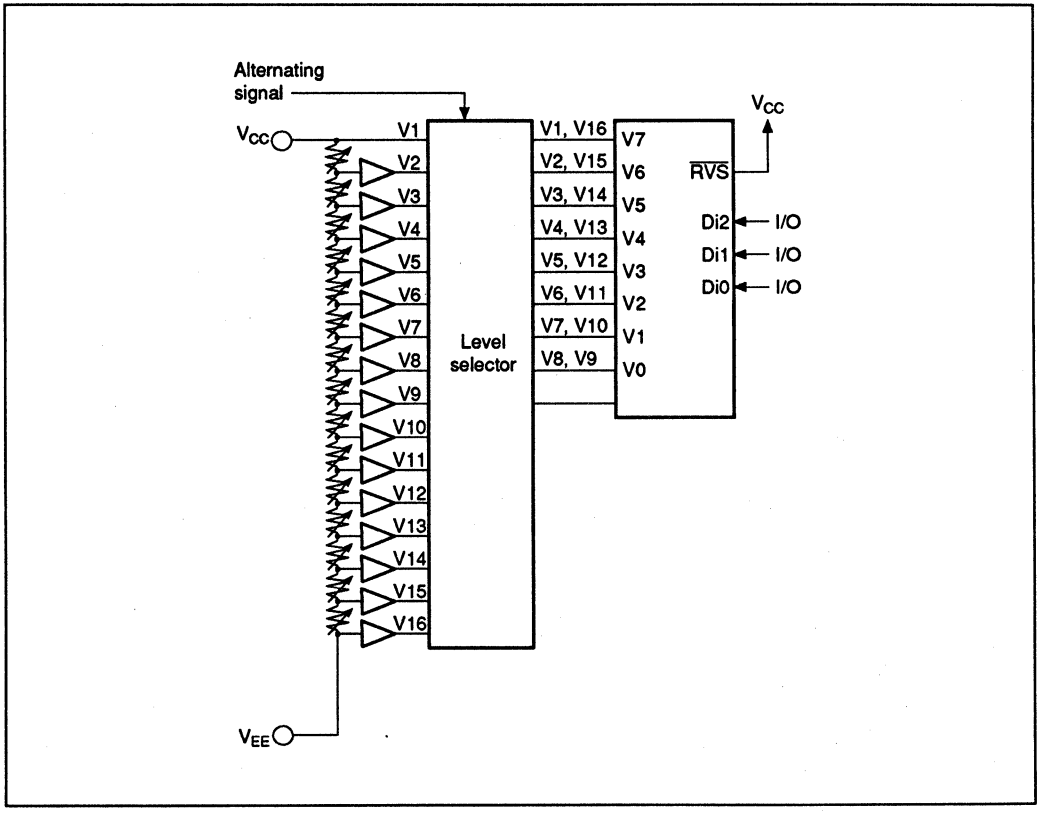


Figure 8 External Power Supply Example 1

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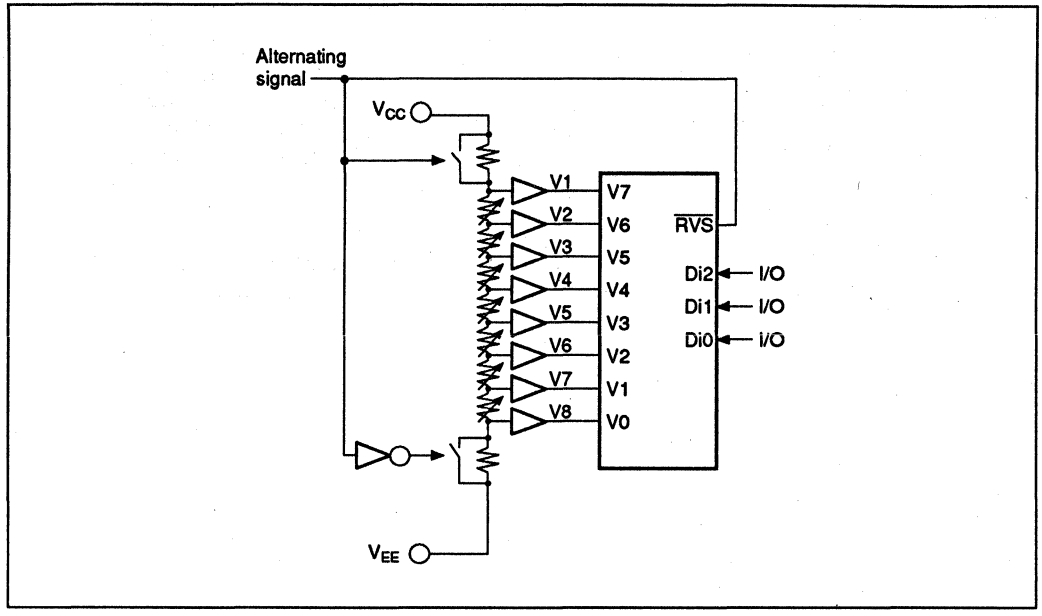


Figure 9 External Power Supply Example 2

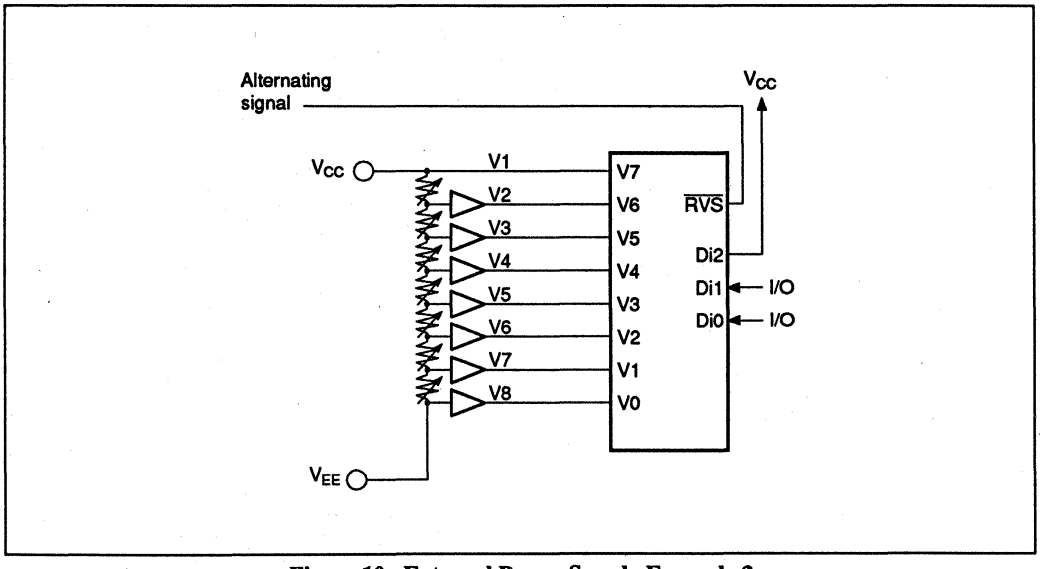


Figure 10 External Power Supply Example 3

Design for Timing

When using the $\overline{RVS}$ pins to simplify the power source, as shown in figures 9 and 10, it is recommended to add a vertical retrace period, (a scanning period in which no scan electrode is selected) at the end of a frame scanning period, as shown in figure 12, for the following two reasons.

- As shown in figure 4, the data reverse circuit is before the latch circuit (1). The LCD driving output is reversed one CL1 period after a transition of the $\overline{RVS}$ signal, as shown in figure 11. However, the power supply lines immediately reverses polarity after a transition of the $\overline{RVS}$ signal, as shown in figures 9 and 10. Therefore, the HD66310 outputs invalid data during the last CL1 of a frame period.
- In the power supply circuits shown in figures 9 and 10, voltage temporarily becomes unstable just after the $\overline{RVS}$ transition, causing the LCD display to become jumbled.

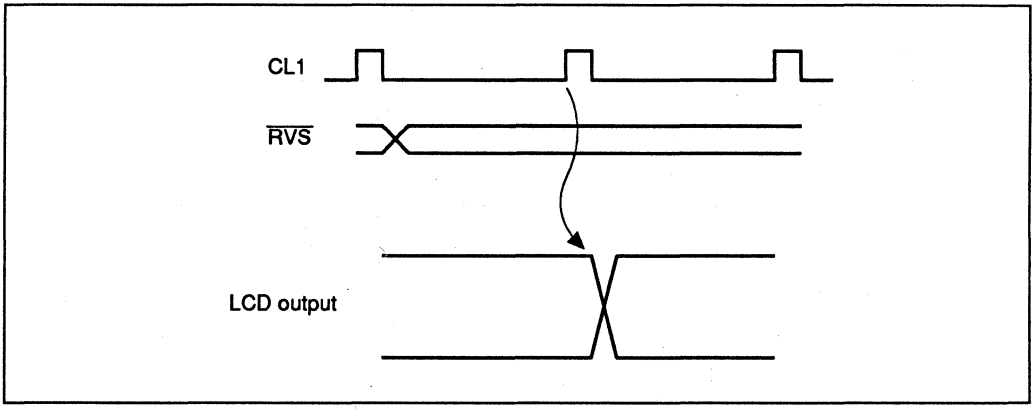


Figure 11 $\overline{RVS}$ and LCD Driving Signals Timing

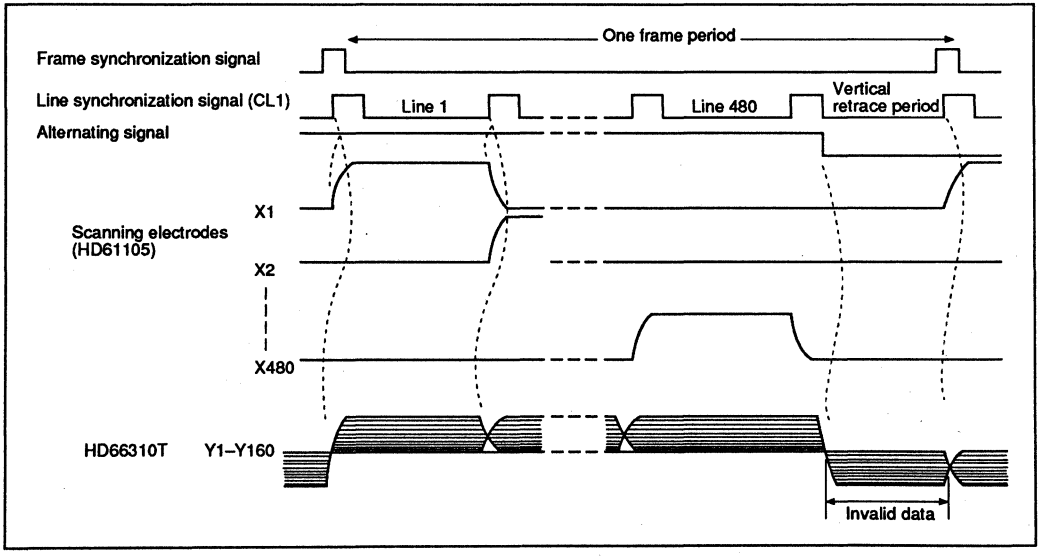


Figure 12 Vertical Retrace Period

Application

Figure 13 shows an HD66310T application for a 480 × 640-dot, 512-color LCD panel. Figure 14 shows the operation timing chart for the system.

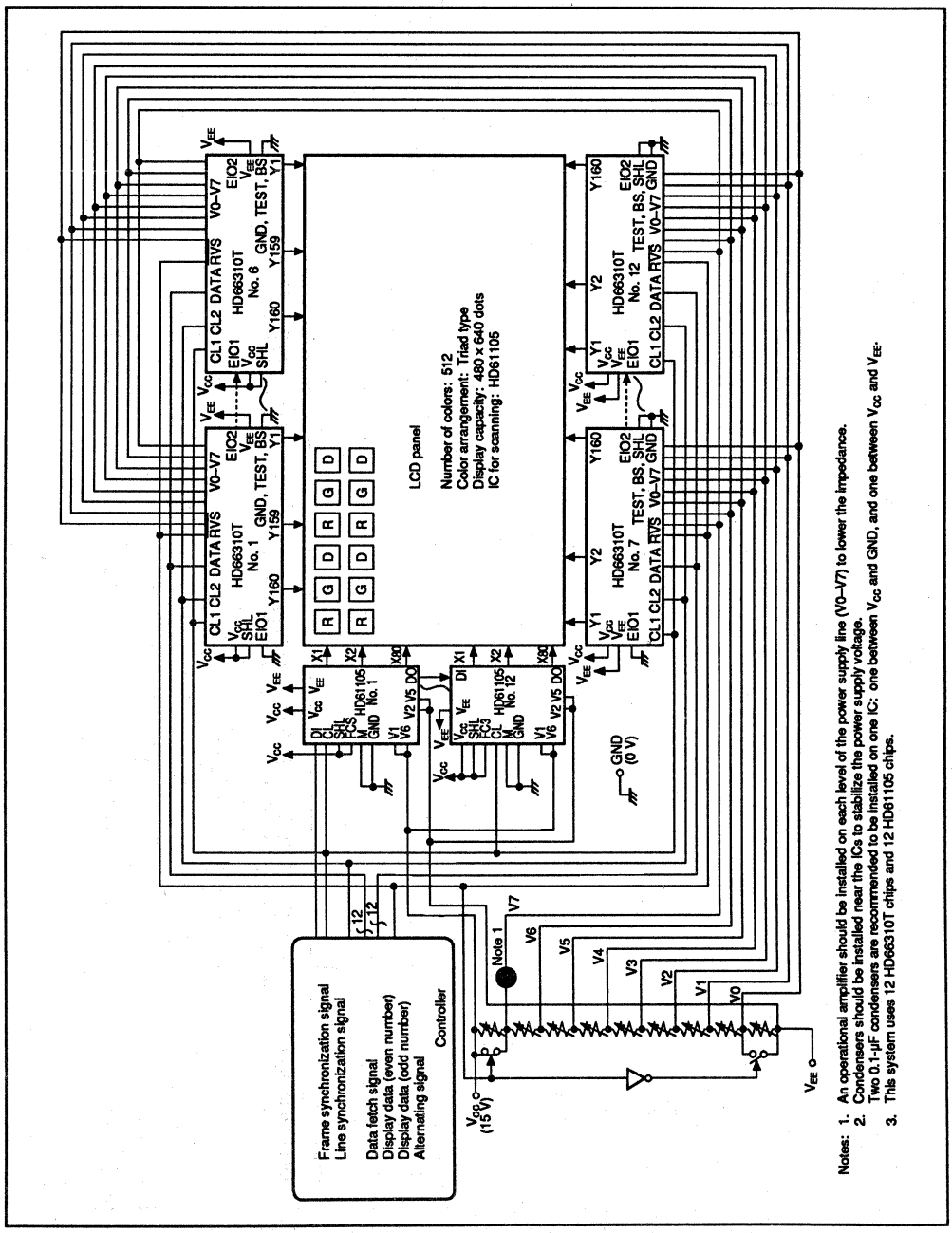


Figure 13 Application System Connection Example

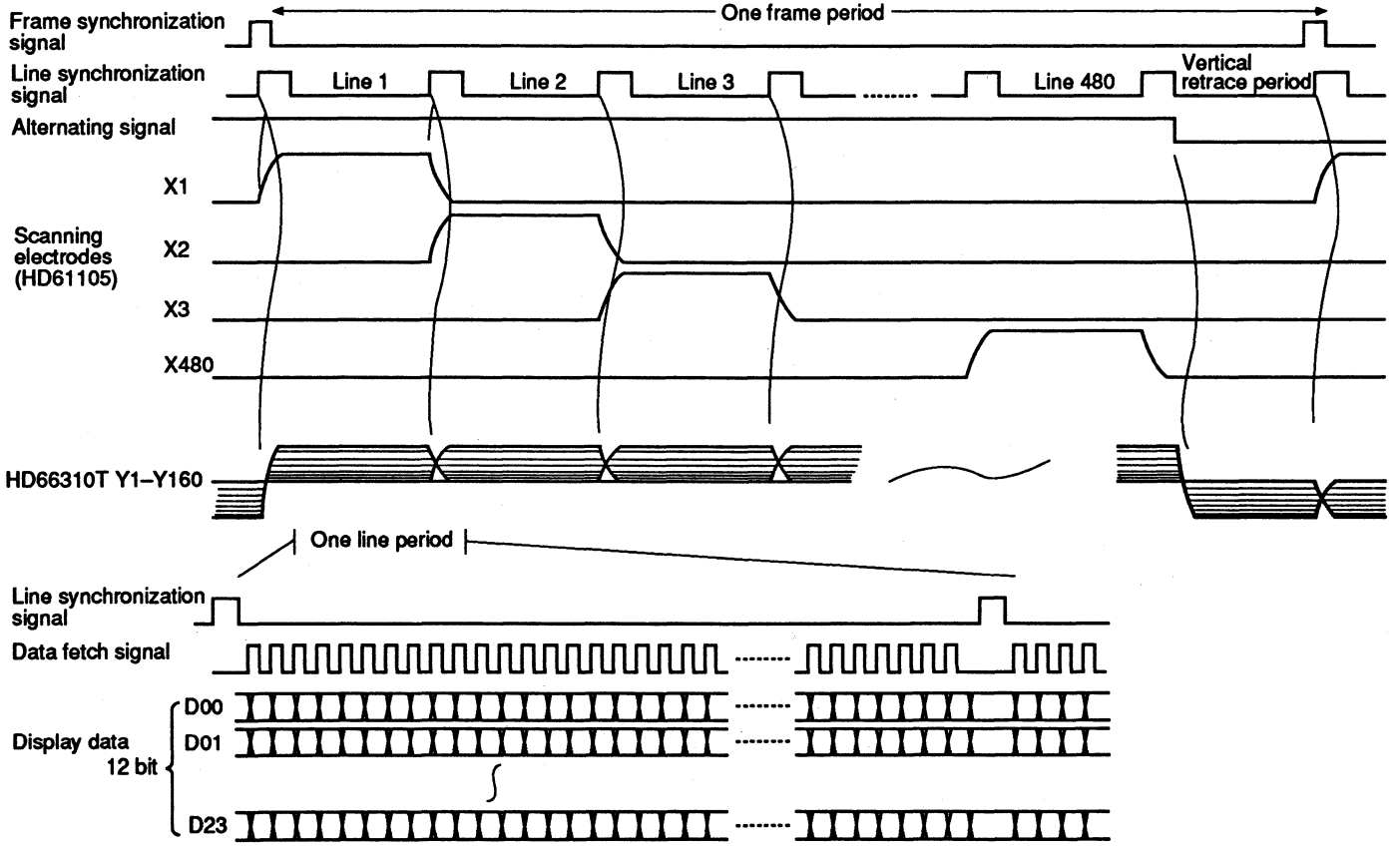


Figure 14 Timing Chart

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Notes
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V	2
Power supply for LCD driving unit	V_{EE}	V_{CC} – 25 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Input voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	
Operating temperature	T_{opr}	–20 to +75 (HD66310T**12) –20 to +65 (HD66310T**15)	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. Exceeding the absolute maximum ratings could result in permanent damage to the LSI. The recommended operating conditions are within the electrical characteristic limits listed on the following pages. Exceeding these limits may cause malfunctions and affect reliability.
2. Values are in reference to GND = 0 V.
3. Applies to input pins SHL, CL1, CL2, BS, $\overline{RVS}$, TEST, and D00–D23. Also applies to input/output pins EIO1 and EIO2 when these pins function as input pins.

Electrical Characteristics

DC Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
LCD driving power supply voltage	$V_{CC} - V_{EE}$			23	V		1
Input high-level voltage	V_{IH}	$0.8 \times V_{CC}$		V_{CC}	V		2
Input low-level voltage	V_{IL}	0		$0.2 \times V_{CC}$	V		2
Output high-level voltage	V_{OH}	$V_{CC} - 0.4$			V	I_{OH} = –0.4 mA	3
Output low-level voltage	V_{OL}			0.4	V	I_{OL} = 0.4 mA	3
Input leakage current (1)	I_{L1}	–5.0		+5.0	µA	$V_{IN} = V_{CC}$ to GND	4
Input leakage current (2)	I_{L2}	–10		+10	µA	$V_{IN} = V_{CC}$ to GND	5
Input leakage current (3)	I_{L3}	–100		+100	µA	$V_{IN} = V_{CC}$ to V_{EE}	6
LCD driver on resistance	RON			2.5	kΩ	$V_{CC} - V_{EE}$ = 20 V	7
Current consumption (1)	$-I_{P1}$			25 30	mA mA	Data fetch 12 MHz Data fetch 15 MHz	8, 10
Current consumption (2)	$-I_{P2}$			2 2.5	mA mA	Stand-by 12 MHz Stand-by 15 MHz	8, 10
Current consumption (3)	$-I_{P3}$			3 3.7	mA mA	12 MHz 15 MHz	9, 10

Notes:
1. Voltage between V_{CC} and V_{EE}.
2. Applies to CL1, CL2, SHL, Dij, $\overline{RVS}$, EIO1 (input), EIO2 (input), TEST, and BS.
3. Applies to EIO1 (output) and EIO2 (output).
4. Applies to CL1, CL2, SHL, $\overline{RVS}$, Dij, TEST, and BS.
5. Applies to EIO1 (input) and EIO2 (input).
6. Applies to V0L to V7L and V0R to V7R.
7. Applies to Y1 to Y160.
8. Current between V_{CC} and GND under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.
9. Current between V_{CC} and V_{EE} under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.
10. f_{CL2} and f_{CL1} are 15 MHz, 37.5 kHz respectively in 15 MHz version.

7

AC Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Clock period	t_{CYC}	83 (66)			ns		1
Clock high-level pulse width	t_{CWH}	30 (23)			ns		1
Clock low-level pulse width	t_{CWL}	30 (23)			ns		1
Clock rise time	t_R			10 (10)	ns		2
Clock fall time	t_F			10 (10)	ns		2
Clock setup time	t_{SU}	100 (100)			ns		2
Clock hold time	t_H	100 (100)			ns		2
Data setup time	t_{DSU}	20 (10)			ns		3
Data hold time	t_{DH}	30 (25)			ns		3
Enable input setup time	t_{ESU}	20 (10)			ns		4
Enable output delay time	t_{ED}			53 (46)	ns	See figure 16 for test load	4
CL1 high-level pulse width	t_{WH}	100 (100)			ns		5
$\overline{RVS}$ setup time	t_{RSU}	50 (50)			ns		6
$\overline{RVS}$ hold time	t_{RH}	50 (50)			ns		6

Data in ( ) is the characteristics in 15 MHz version.

Notes: 1. Applies to CL2.
2. Applies to CL1 and CL2.
3. Applies to Dij and CL2.
4. Applies to EIO1, EIO2, and CL2.
5. Applies to CL1.
6. Applies to $\overline{RVS}$ and CL2.

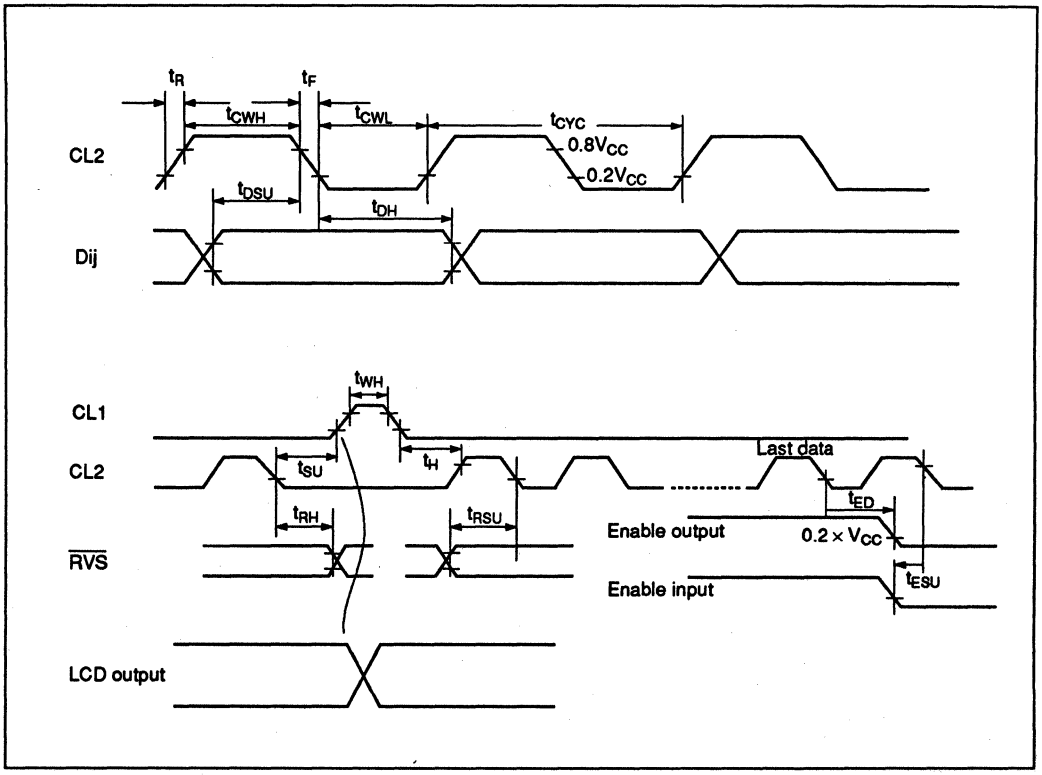


Figure 15 Timing Chart

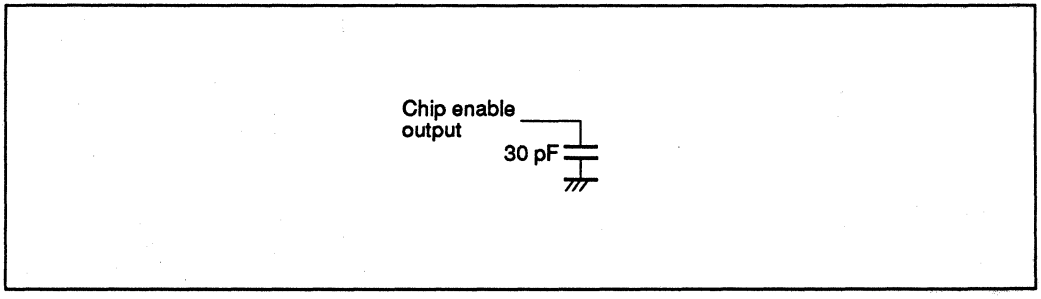


Figure 16 Test Load

7

Section Eight

New Product Information

HD66110T
Column Driver

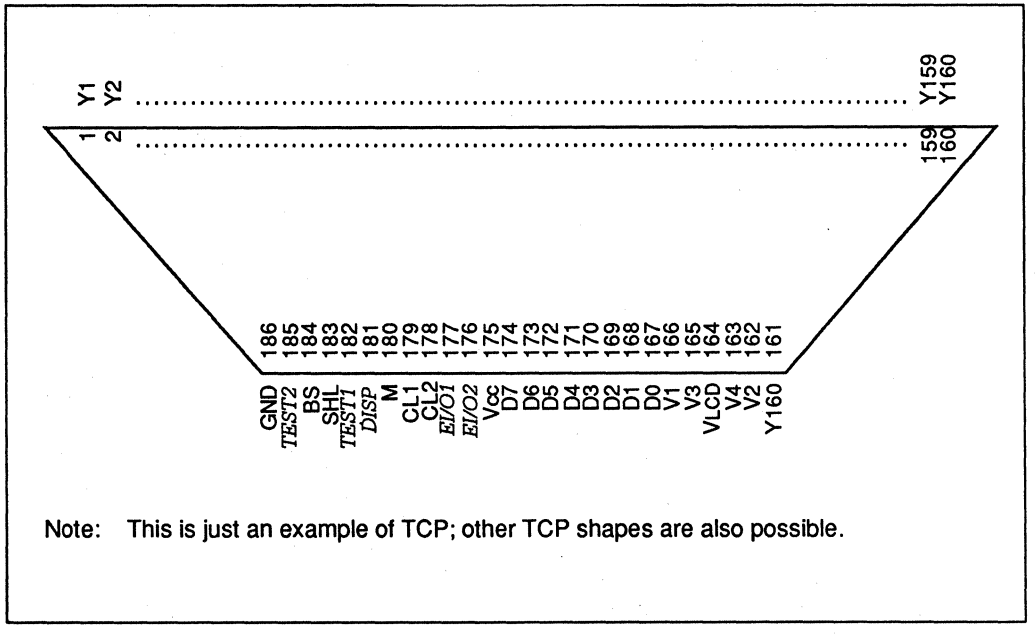
Description

The HD66110T, the column driver for a large liquid crystal display (LCD) panel, features as many as 160 LCD outputs powered by 160 internal LCD drive circuits, and a high duty cycle. This device can interface to various LCD controllers by using an internal automatic chip enable signal generator. Its strip shape enables a slim tape carrier package (TCP).

Features

- 186-pin TCP
- CMOS fabrication process
- High voltage
  - — LCD drive: 28 – 40 V
- High speed
  - — Maximum clock speed: 12 MHz
- 4- and 8-bit data bus interface
- Display off function
- Standby function
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850

Pin Arrangement



Note: This is just an example of TCP; other TCP shapes are also possible.

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	175	V_{CC}	—	Power supply
GND	186	GND	—	Power supply
V_{LCD}	164	V_{LCD}	—	Power supply
V1	166	V1	Input	Power supply
V2	162	V2	Input	Power supply
V3	165	V3	Input	Power supply
V4	163	V4	Input	Power supply
CL1	179	Clock 1	Input	Control signal
CL2	178	Clock 2	Input	Control signal
M	180	M	Input	Control signal
D_0–D_7	167–174	Data 0–data 7	Input	Control signal
SHL	183	Shift left	Input	Control signal
$\overline{EI/O1}$, $\overline{EI/O2}$	177, 176	Enable IO 1, enable IO 2	Input/output	Control signal
$\overline{DISP}$	181	Display off	Input	Control signal
BS	184	Bus select	Input	Control signal
$\overline{TEST1}$, $\overline{TEST2}$	182, 185	Test 1, test 2	Input	Control signal
Y_1–Y_{160}	1–160	Y_1–Y_{160}	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, V_{LCD}, GND: V_{CC} – GND supplies power to the internal logic circuits. V_{LCD} – GND supplies power to the LCD drive circuits. See figure 1.

V1, V2, V3, V4: Supply different levels of power to drive the LCD. V1 and V2 are selected levels, and V3 and V4 are non-selected levels.

Control Signals

CL1: Inputs display data latch pulses for latch circuit 2. Latch circuit 2 latches display data input from latch circuit 1, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for latch circuit 1. Latch circuit 1 latches display data input via D_0–D_7 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_7: Input display data. High-voltage level (V_{CC} level) of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level (GND level) data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output, and determines which chip enable pin ($\overline{EI/O1}$ or $\overline{EI/O2}$) is an input and which is an output. See figure 2.

$\overline{EI/O1}$, $\overline{EI/O2}$: If SHL is GND level, $\overline{EI/O1}$ inputs the chip enable signal, and $\overline{EI/O2}$ outputs the signal. If SHL is Vcc level, $\overline{EI/O1}$ outputs the chip enable signal, and $\overline{EI/O2}$ inputs the signal. The chip enable input pin of the first HD66110T must be grounded, and those of the other HD66110Ts must be connected to the chip enable output pin of the previous HD66110T. The chip enable output pin of the last HD66110T must be open.

$\overline{DISP}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{160} to V2 level.

BS: Selects either the 4-bit or 8-bit display data bus interface. If BS is V_{CC} level, the 8-bit bus is selected, and if BS is GND level, the 4-bit bus is selected. In 4-bit bus mode, data is latched via D_0–D_3; D_4–D_7 must be grounded.

$\overline{TEST1}$, $\overline{TEST2}$: Used to test the LSI, and must be connected to V_{CC} level.

LCD Drive Output

Y_1–Y_{160}: Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on a combination of the M signal and display data levels. See figure 3.

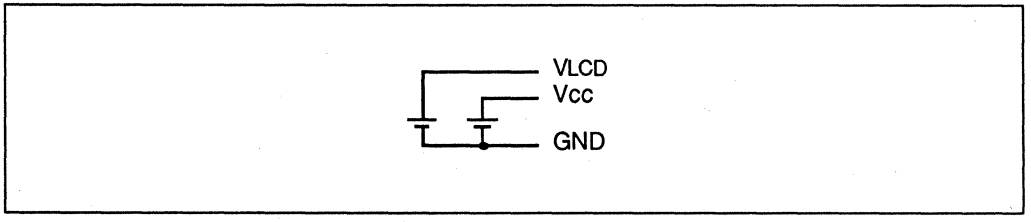


Figure 1 Power Supply for Logic and LCD Drive Circuits

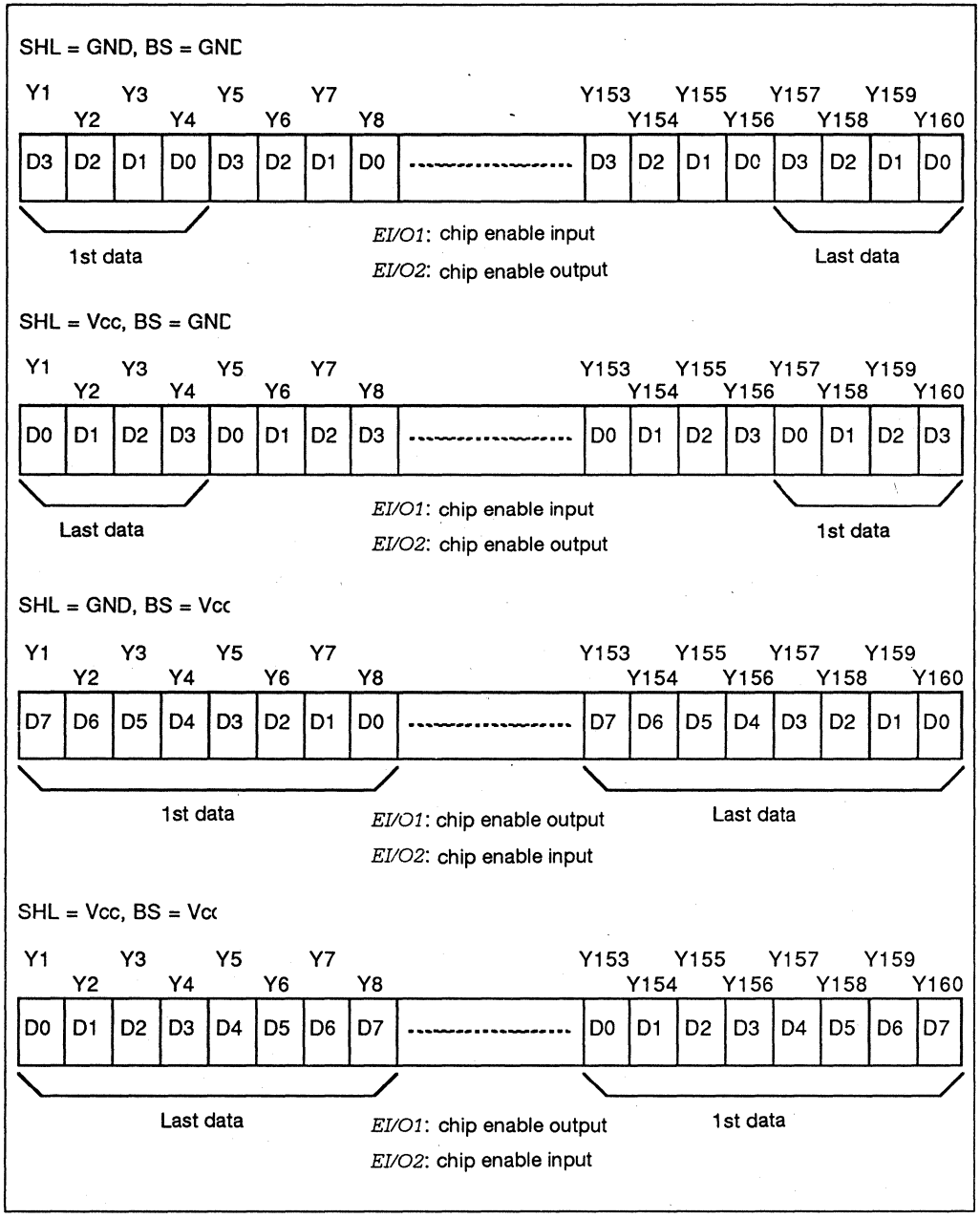


Figure 2 Selection of Destinations of Display Data Output

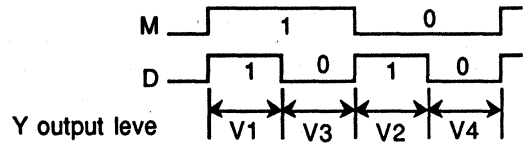


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

The 160-bit LCD drive circuit generates four voltage levels V1, V2, V3, and V4, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the latch circuit 2.

Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Latch Circuit 2

160-bit latch circuit 2 latches data input from latch circuit 1, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

Latch Circuit 1

160-bit latch circuit 1 latches 4-bit or 8-bit parallel data input via the D_0 to D_7 pins at the timing generated by the shift register.

Shift Register

The 40-bit shift register generates and outputs data latch signals for latch circuit 1 at the falling edge of each clock 2 (CL2) pulse.

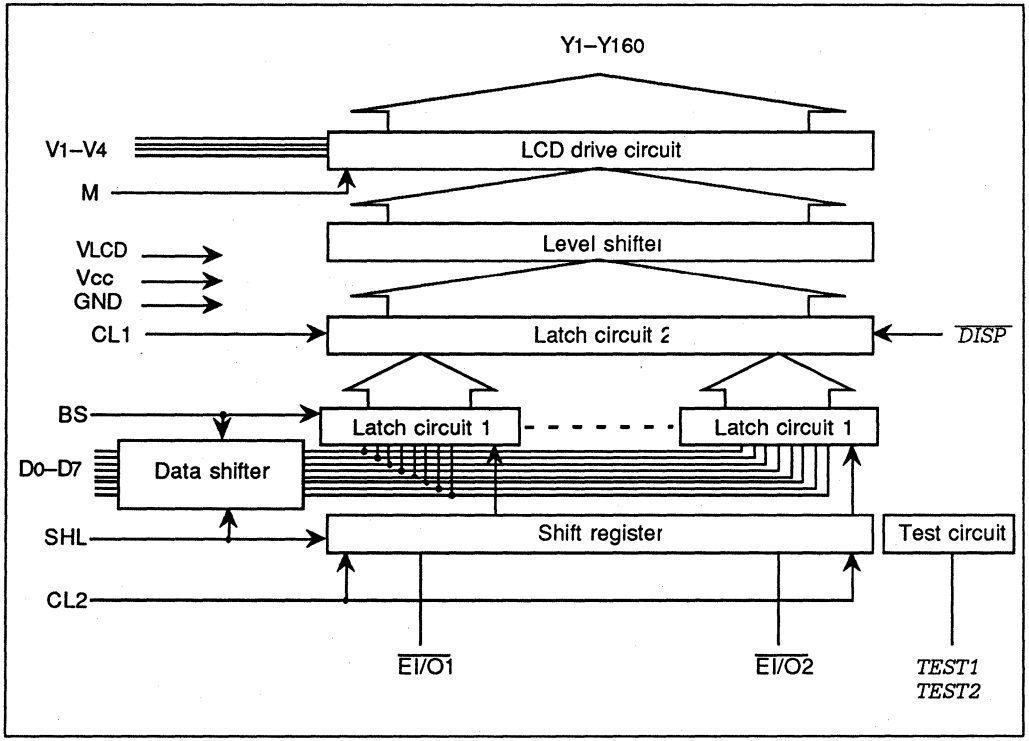
Data Shifter

The data shifter shifts the destinations of display data output, when necessary.

Test Circuit

The test circuit divides the external clock pulses and generates test signals ($\overline{TEST1}$ and $\overline{TEST2}$).

Block Diagram



Comparison of the HD66110T with the HD66107T

Item	HD66110T	HD66107T
Common LCD drive circuits	Not provided	160
Column LCD drive circuits	160	160 or 80
LCD drive voltage range	28 to 40 V	14 to 37 V
Speed	12 MHz	8 MHz
Clock hold time (t_{HCL}) definition	From the falling edge of CL1 to the rising edge of CL2 (figure 1)	From the falling edge of CL1 to the falling edge of CL2 (figure 1)
Test pin level at normal operation	V_{CC}	GND
Display off function	Provided	Not provided
TCP shape	Can be thin	Cannot be thin

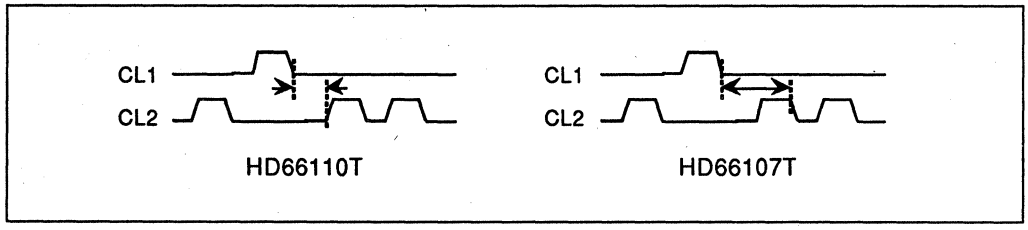


Figure 4 t_{HCL} Definitions of the HD66110T and HD66107T

Operation Timing

4-Bit Bus Mode (BS = GND)

Figure 5 shows 4-bit data latch timing when SHL = GND, that is, the $\overline{EI/O1}$ pin is a chip enable input and $\overline{EI/O2}$ pin is a chip enable output. When SHL = V_{CC}, the $\overline{EI/O1}$ pin is a chip enable output and $\overline{EI/O2}$ pin is a chip enable input.

When a low chip enable signal is input via the $\overline{EI/O1}$ pin, the HD66110T is first released from data standby state, and, at the falling edge of the following CL2 pulse, it is released entirely from standby state and starts latching data.

It simultaneously latches 4 bits of data at the falling edge of each CL2 pulse. When it has latched 156 bits of data, it sets the $\overline{EI/O2}$ signal low. When it has latched 160 bits of data, it automatically stops and enters standby state, initiating the next HD66110T, as long as its $\overline{EI/O2}$ pin is connected to the $\overline{EI/O1}$ pin of the next HD66110T.

The HD66110Ts output one line of data from the Y_1–Y_{160} pins at the falling edge of each CL1 pulse. Data d_1 is output from Y_1, and d_{160} from Y_{160} when SHL = GND, and d_1 is output from Y_{160}, and d_{160} from Y_1 when SHL = V_{CC}.

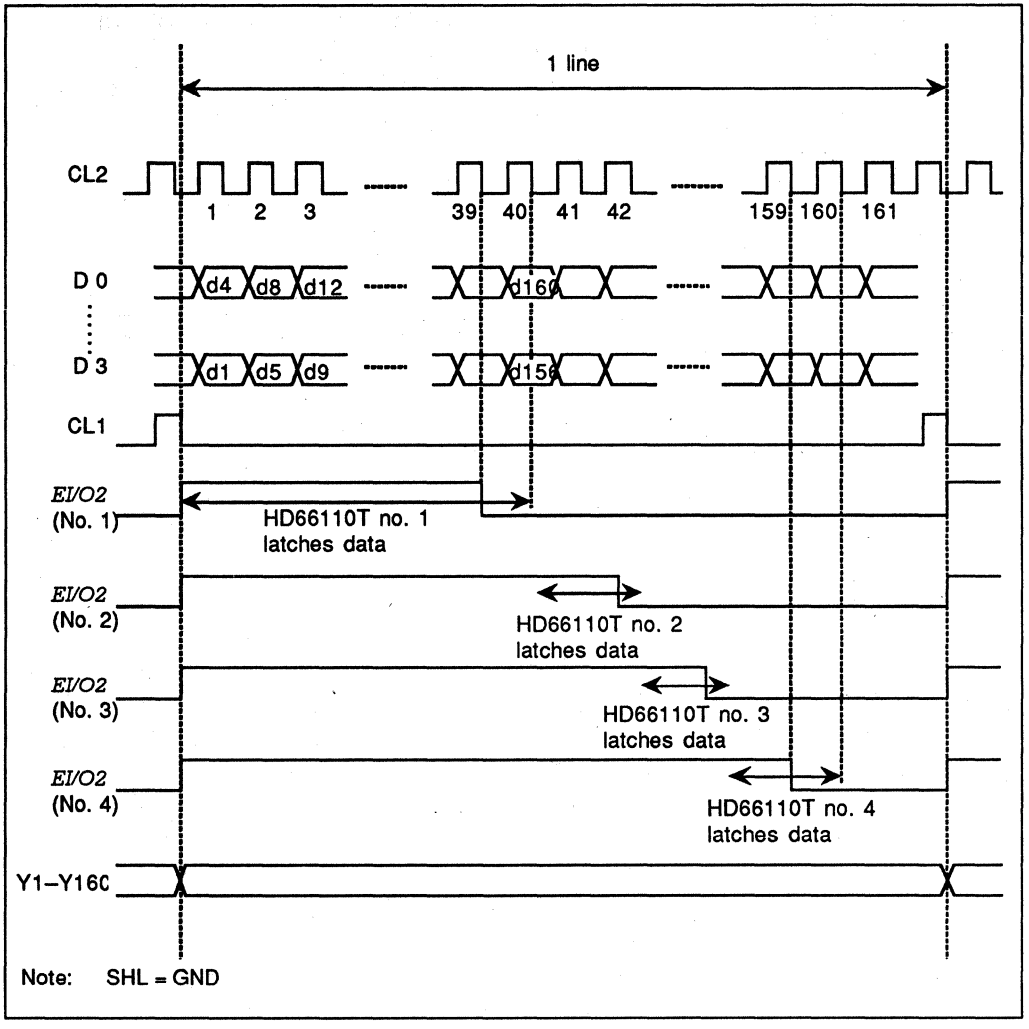


Figure 5 4-Bit Data Latch Timing (SHL = GND)

8-Bit Bus Mode (BS = V_{CC})

Figure 6 shows 8-bit data latch timing when SHL = GND, that is, the $\overline{EI/O1}$ pin is a chip enable input and $\overline{EI/O2}$ pin is a chip enable output.

When SHL = V_{CC}, the EI/O1 pin is a chip enable output and $\overline{EI/O2}$ pin is a chip enable input.

The operation is the same as that in 4-bit bus mode except that 8 bits of data are latched simultaneously.

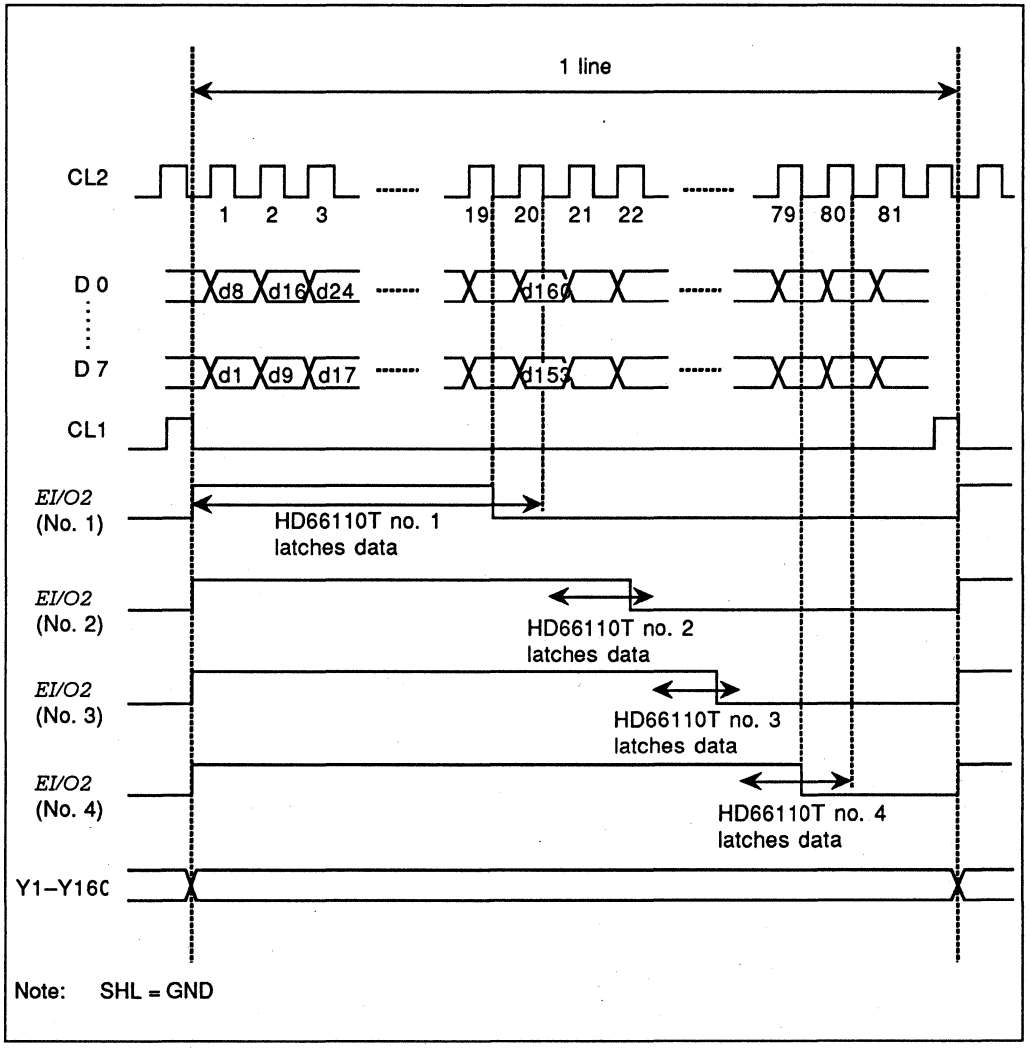
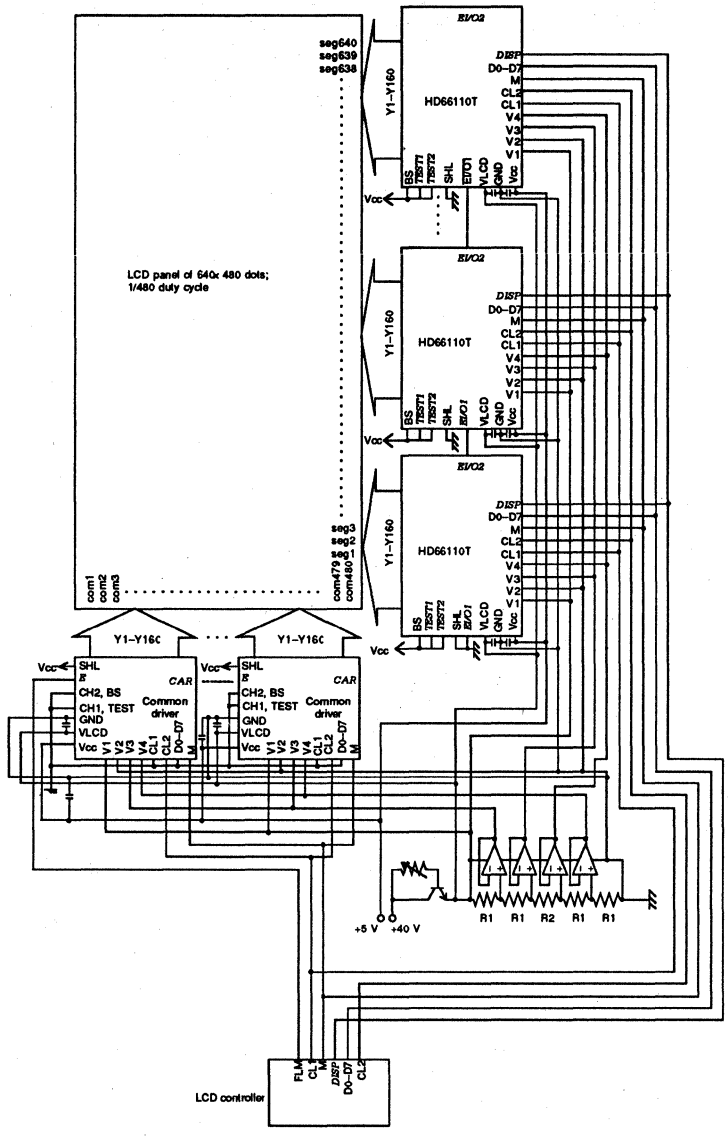


Figure 6 8-Bit Data Latch Timing (SHL = GND)

Application Example



Notes:

1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/20 bias, R1 and R2 must be 3 kΩ and 48 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/20.
2. To stabilize the power supply, place two 0.1-μF capacitors near each LCD driver: one between the Vcc and GND pins, and the other between the V_{LCD} and GND pins.
3. The load must be less than 30 pF between the $\overline{EI/O2}$ and $\overline{EI/O1}$ connections of HD66110Ts.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 2, 5
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 3
Input voltage 2	V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes:
1. The reference point is GND (0 V).
2. Indicates the voltage between GND and V_{LCD}.
3. Applies to input pins for logic circuits, that is, control signal pins.
4. Applies to input pins for LCD drive level voltages, that is, V1–V4 pins.
5. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} – GND = 28 to 40 V, and T_a = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	1	0.8 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	1	0	0.2 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	V_{IN} = V_{LCD} to GND	
Current consumption 1	I_{CC}	—	—	5.0	mA	f_{CL2} = 12 MHz f_{CL1} = 28 kHz	2
Current consumption 2	I_{LCD}	—	—	3.0	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	0.7	mA	Same as above	2, 3

Pins and notes on next page.

Pins:
1. CL1, CL2, M, SHL, BS, EI/O1, EI/O2, $\overline{DISP}$, $\overline{TEST1}$, $\overline{TEST2}$, D_0–D_7
2. $\overline{EI/O1}$, $\overline{EI/O2}$
3. Y_1–Y_{160}, V1–V4
4. V1–V4

Notes:
1. Indicates the resistance between one pin from Y_1–Y_{160} and another pin from V1–V4 when load current is applied to the Y pin; defined under the following conditions.

   V_{LCD} – GND = 40 V

   V1, V3 = V_{LCD} – {1/20(V_{LCD} – GND)}

   V2, V4 = V_{LCD} + {1/20(V_{LCD} – GND)}

   V1 and V3 should be near V_{LCD} level, and V2 and V4 should be near GND level (figure 7). All voltage must be within ΔV. ΔV is the range within which RON, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{LCD} – GND (figure 8).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

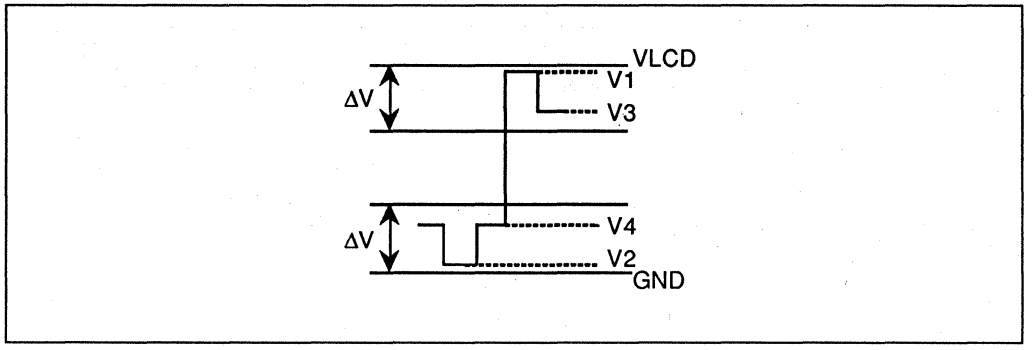


Figure 7 Relation between Driver Output Waveform and Level Voltages

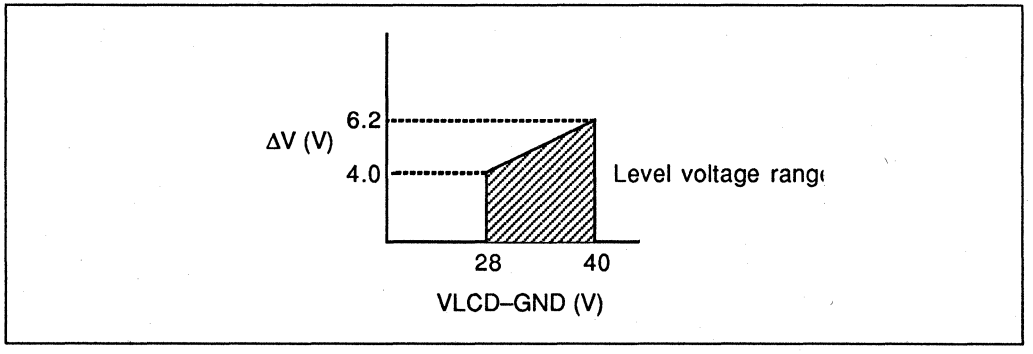


Figure 8 Relation between V_{LCD} – GND and ΔV

AC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} – GND = 28 to 40 V, and T_a = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit
Clock cycle time	t_{CYC}	CL2	83	—	ns
Clock high-level width 1	t_{CWH2}	CL2	20	—	ns
Clock low-level width	t_{CWL2}	CL2	20	—	ns
Clock high-level width 2	t_{CWH1}	CL1	50	—	ns
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns
Clock hold time	tHCL	CL1, CL2	100	—	ns
Clock rise time	t_r	CL1, CL2	—	20	ns
Clock fall time	t_f	CL1, CL2	—	20	ns
Data setup time	t_{DS}	D_0–D_7, CL2	20	—	ns
Data hold time	t_{DH}	D_0–D_7, CL2	20	—	ns
M phase difference time	t_{CM}	M, CL1	—	300	ns

Note: The load must be less than 30 pF between the $\overline{EI/O2}$ and $\overline{EI/O1}$ connections of HD66110Ts.

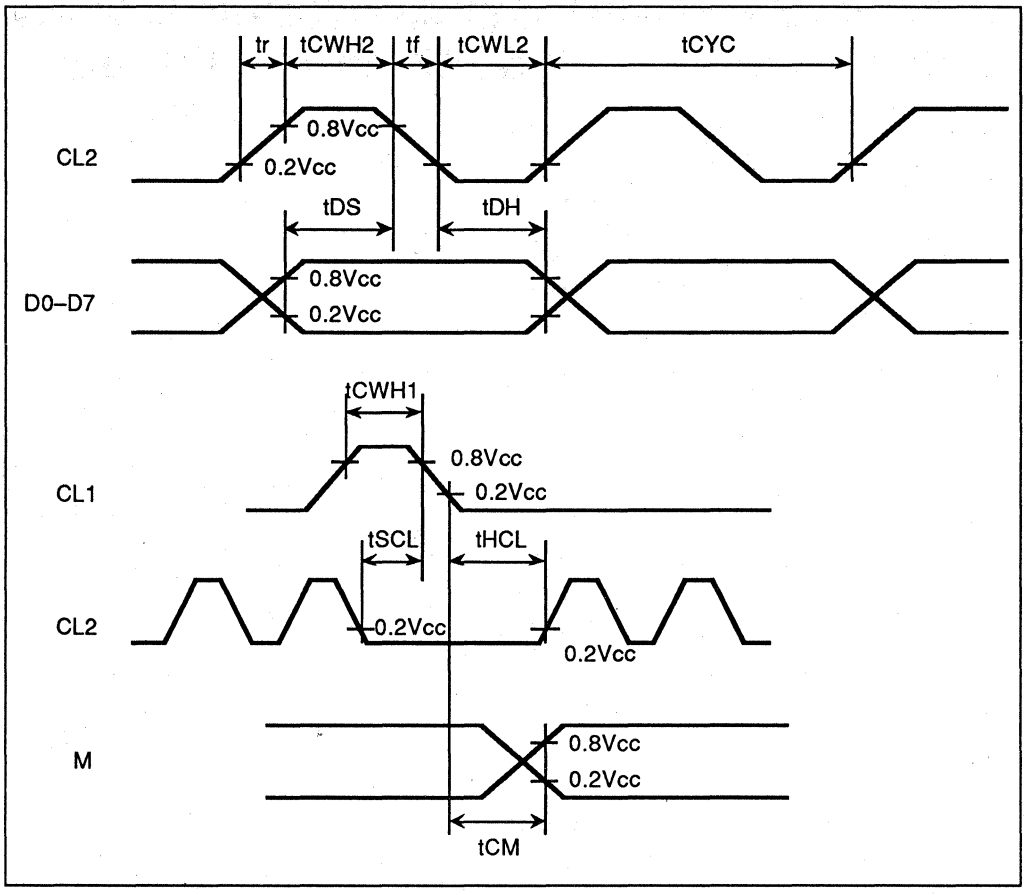


Figure 9 LCD Controller Interface Timing

HD66204

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

Description

The HD66204F/HD66204FL/HD66204TF/HD66204TFL, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66204 has a complete line-up: the HD66204F, a standard device powered by 5 V ± 10%; the HD66204FL, a 2.7–5.5 V, low power dissipation device suitable for battery-driven portable equipment such as "notebook" personal computers and palm-top personal computers; and the HD66204TF and HD66204TFL, thin package devices powered by 5 V ± 10% and 2.7–5.5 V, respectively.

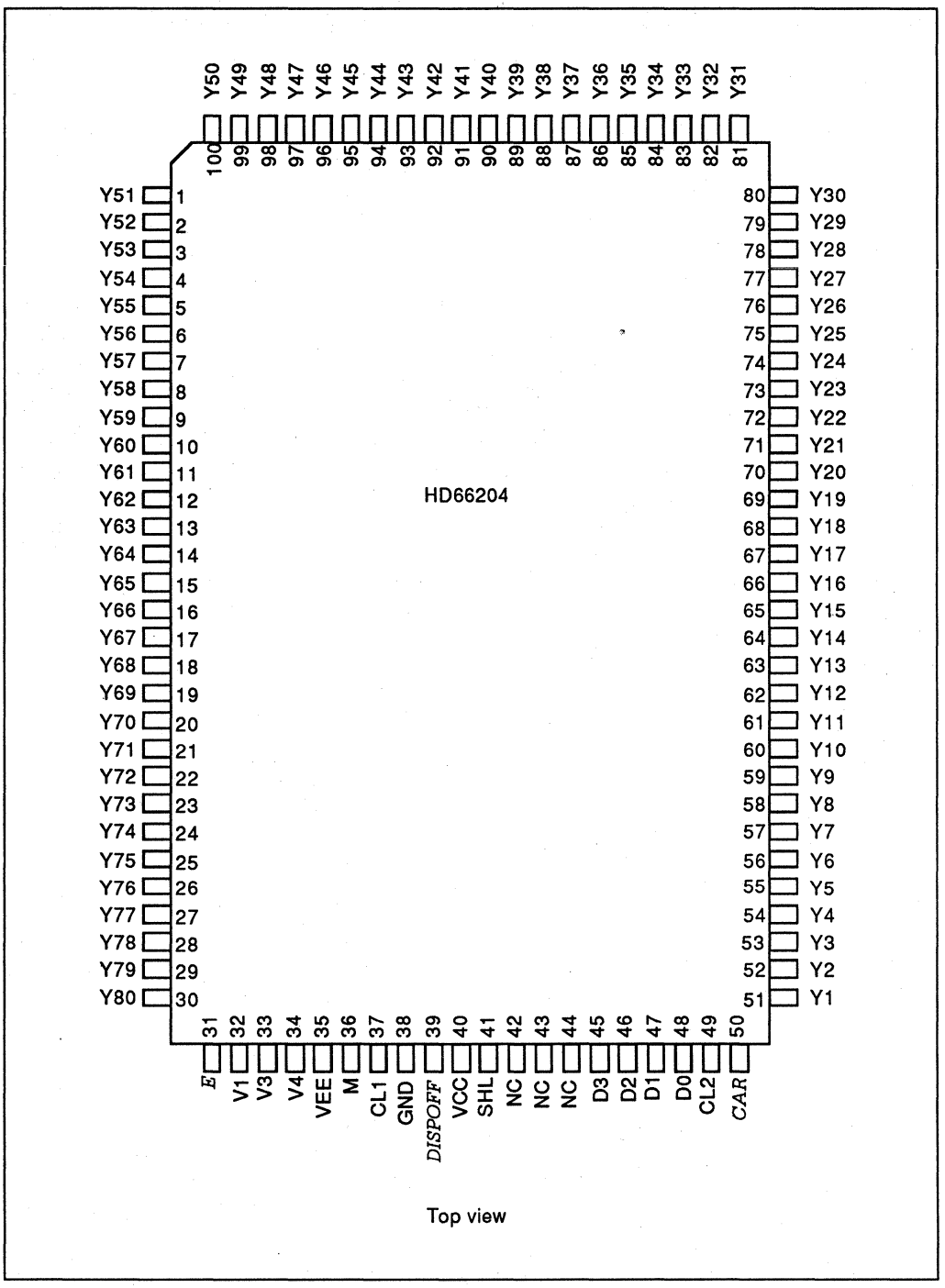
Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10–28 V
- High clock speed
  - — 8 MHz max under 5-V operation (HD66204F/HD66204TF)
  - — 4 MHz max under 3-V operation (HD66204FL/HD66204TFL)
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850

Ordering Information

Type No.	Voltage Range	Package
HD66204F	5 V ± 10%	FP-100 (flat package)
HD66204TF	5 V ± 10%	TFP-100 (thin flat package)
HD66204FL	2.7–5.5 V	FP-100 (flat package)
HD66204TFL	2.7–5.5 V	TFP-100 (thin flat package)

Pin Arrangement



Top view

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	40	V_{CC}	—	Power supply
GND	38	GND	—	Power supply
V_{EE}	35	V_{EE}	—	Power supply
V1	32	V1	Input	Power supply
V3	33	V3	Input	Power supply
V4	34	V4	Input	Power supply
CL1	37	Clock 1	Input	Control signal
CL2	49	Clock 2	Input	Control signal
M	36	M	Input	Control signal
D_0–D_3	48–45	Data 0–data 3	Input	Control signal
SHL	41	Shift left	Input	Control signal
$\overline{E}$	31	Enable	Input	Control signal
$\overline{CAR}$	50	Carry	Output	Control signal
$\overline{DISPOFF}$	39	Display off	Input	Control signal
Y_1–Y_{80}	51–100, 1–30	Y1–Y80	Output	LCD drive output
NC	42, 43, 44	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D_0–D_3 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_3: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66204 if HD66204s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{80} to V1 level.

LCD Drive Output

Y_1–Y_{80}: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

NC: Must be open.

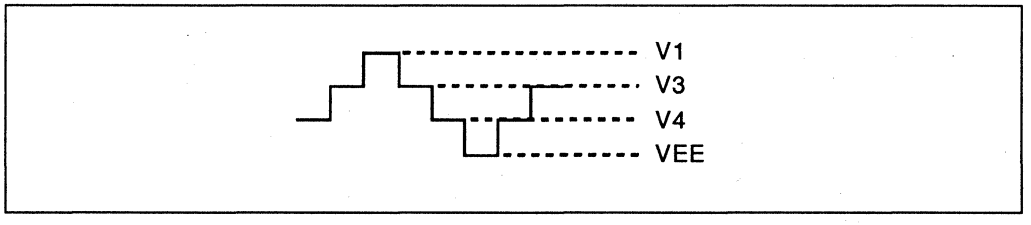


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

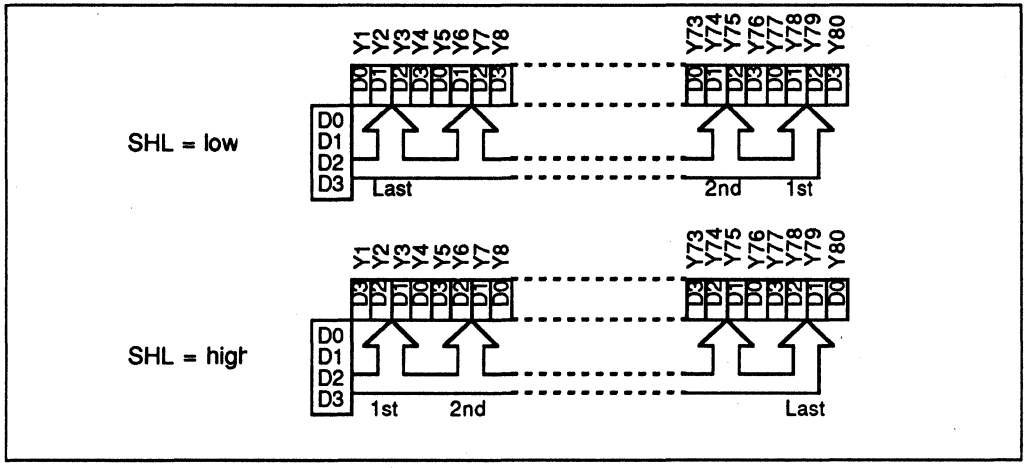


Figure 2 Selection of Destinations of Display Data Output

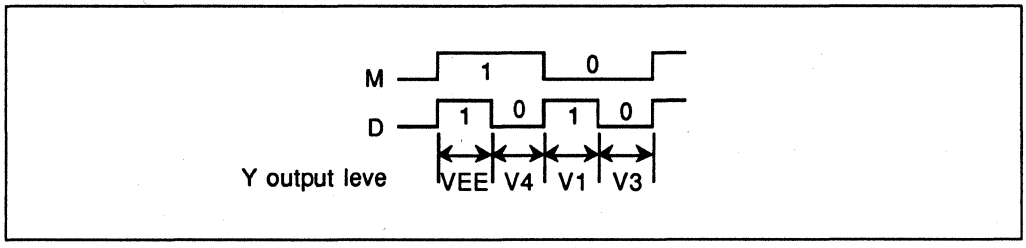


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D_0 to D_3 pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

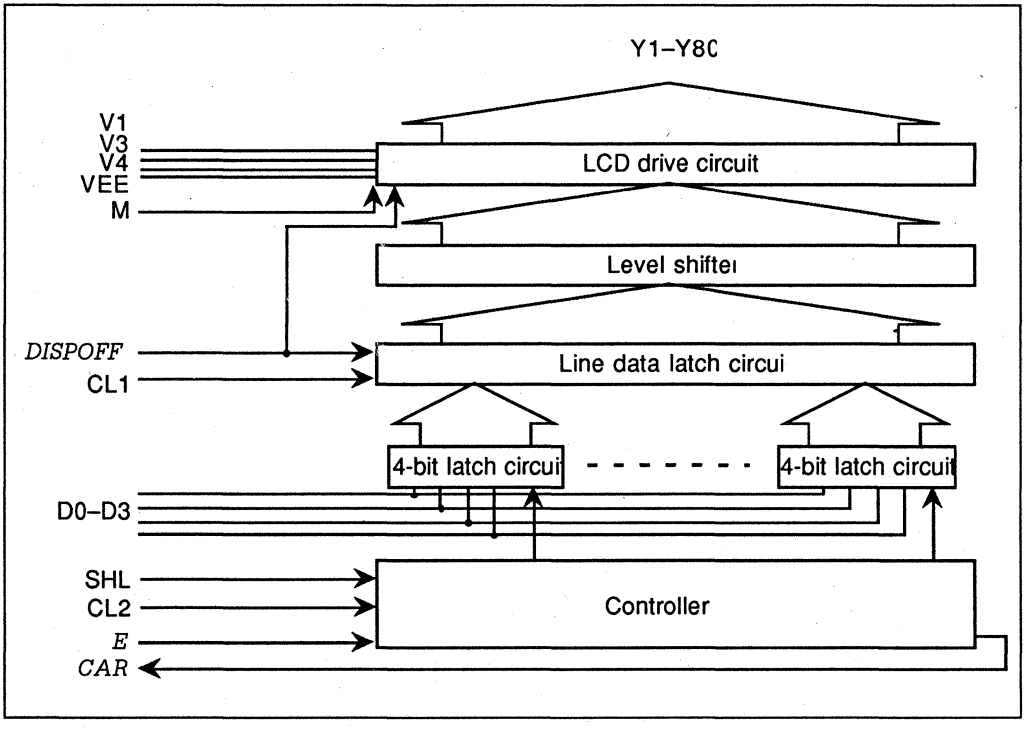
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and VEE, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



Comparison of the HD66204 with the HD61104

Item	HD66204	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as VEE level)	V1, V2, V3, V4

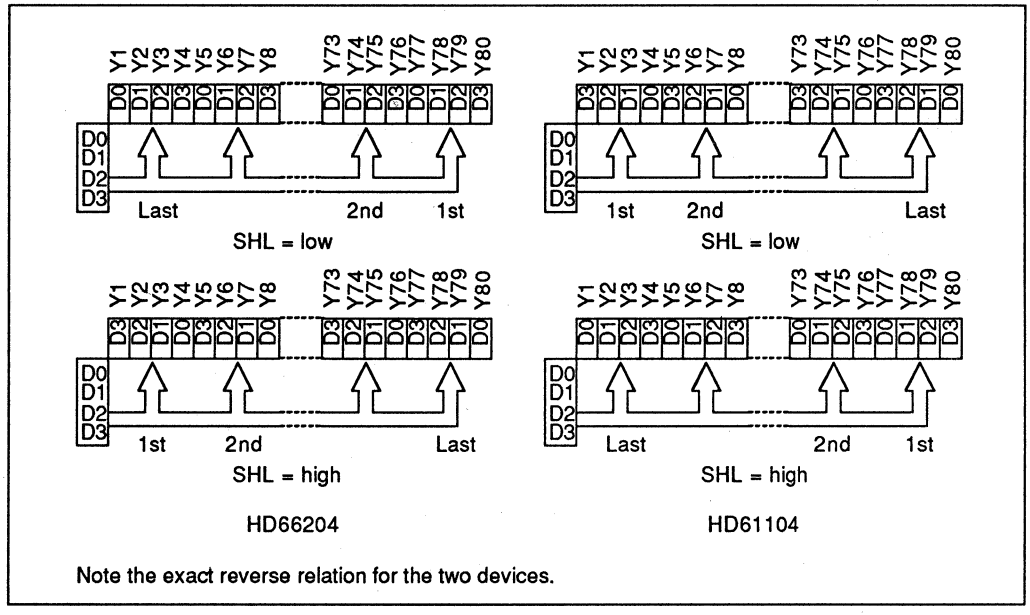


Figure 4 Relation between SHL and LCD Output Destinations for the HD66204 and HD61104

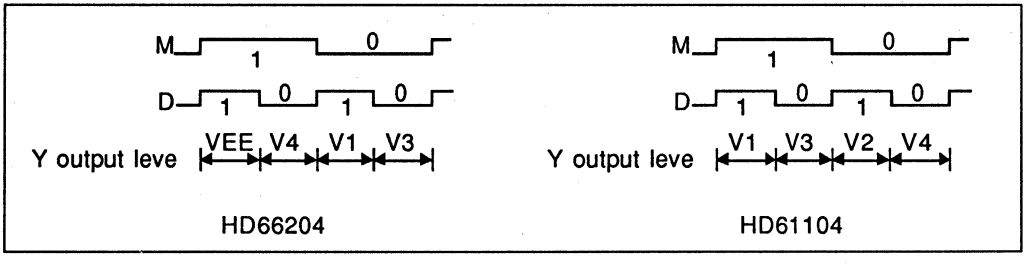
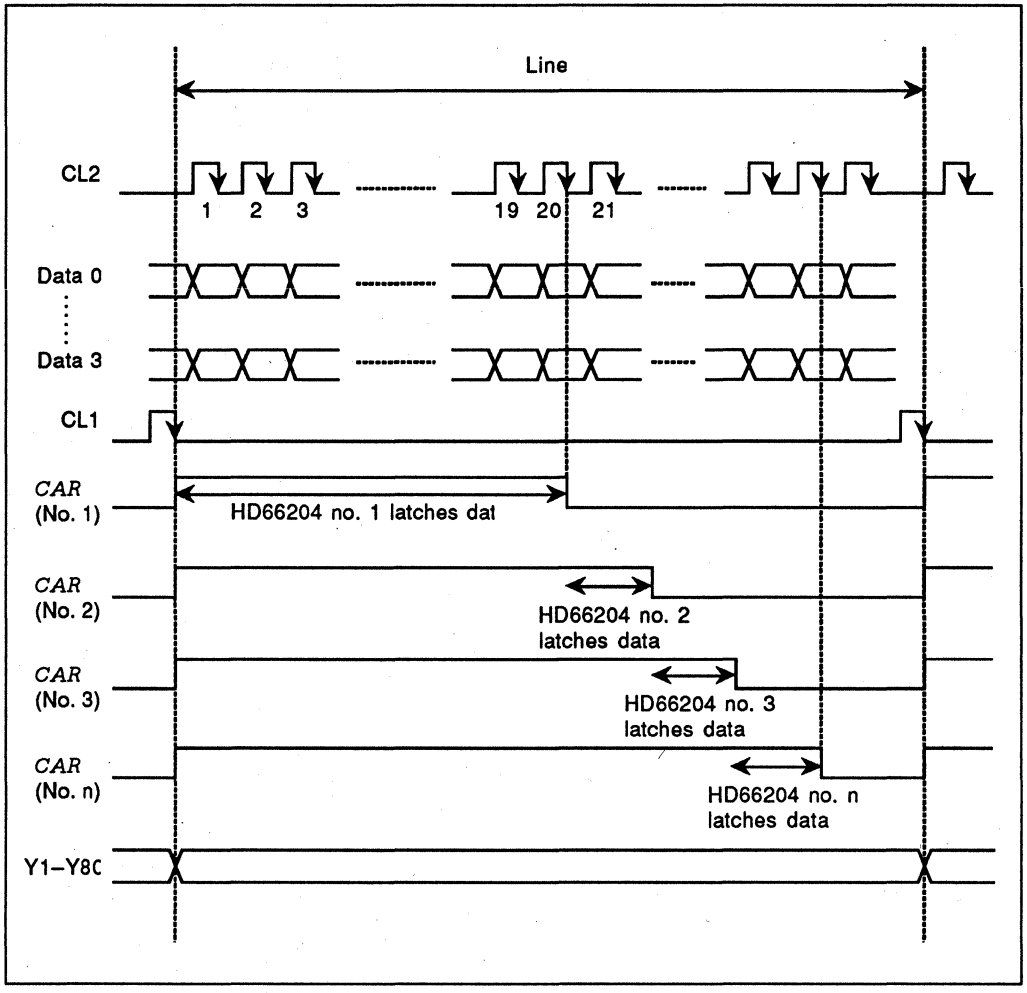
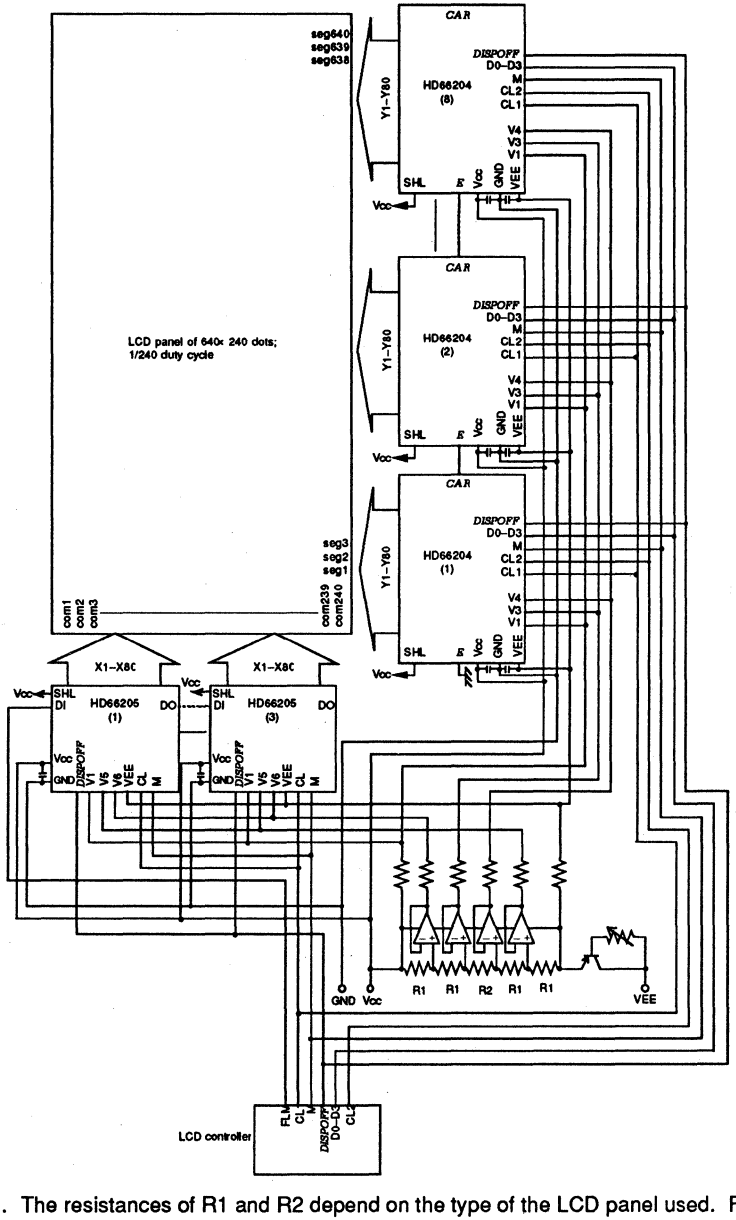


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66204 and HD61104

Operation Timing



Application Example



Notes:
1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/15.
2. To stabilize the power supply, place two 0.1-μF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

8

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. The reference point is GND (0 V).

2. Applies to pins CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$.

3. Applies to pins V1, V3, and V4.

4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	µA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	1	0.7 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	1	0	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	f_{CL2} = 4.0 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	50	µA	Same as above	2, 3

Pins:
1. CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$
2. $\overline{CAR}$
3. Y_1–Y_{80}, V1, V3, V4
4. V1, V3, V4

Notes:
1. Indicates the resistance between one pin from Y_1–Y_{80} and another pin from V1, V3, V4, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions.

   V_{CC} – GND = 28 V

   V1, V3 = $V_{CC} - \{2/10(V_{CC} - V_{EE})\}$

   V4 = $V_{EE} + \{2/10(V_{CC} - V_{EE})\}$

   V1 and V3 should be near V_{CC} level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 7).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

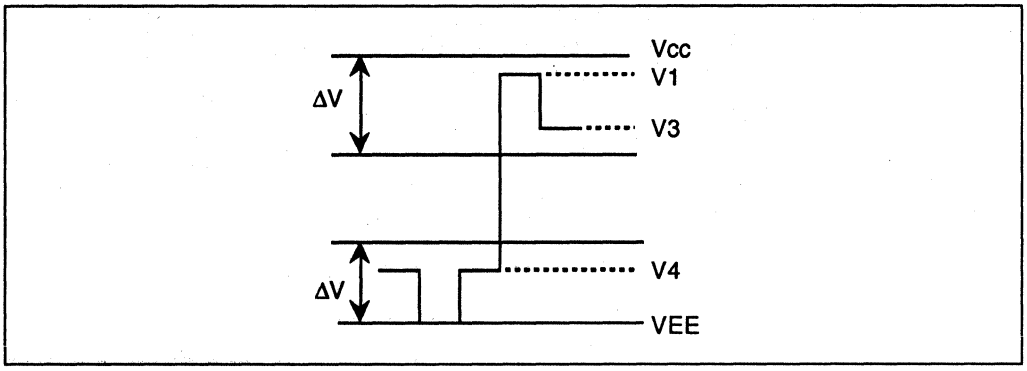


Figure 6 Relation between Driver Output Waveform and Level Voltages

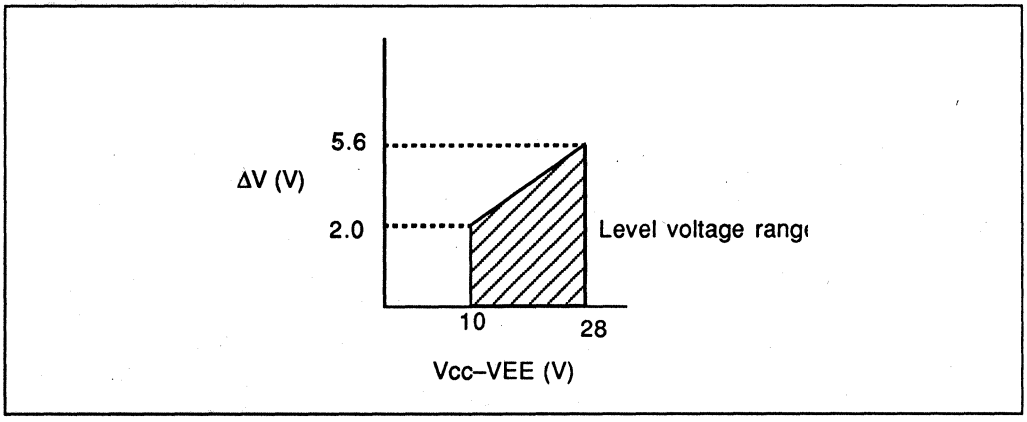


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	20	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	20	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	30	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	1	
Clock fall time	t_f	CL1, CL2	—	Note 1	1	
Data setup time	t_{DS}	D_0–D_3, CL2	50	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	50	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	65	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

Notes: 1. t_r, $t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \leq 50$ ns

2. The load circuit shown in figure 8 is connected.

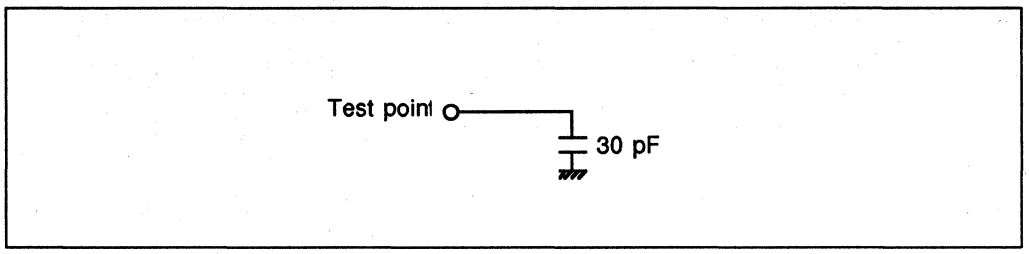


Figure 8 Load Circuit

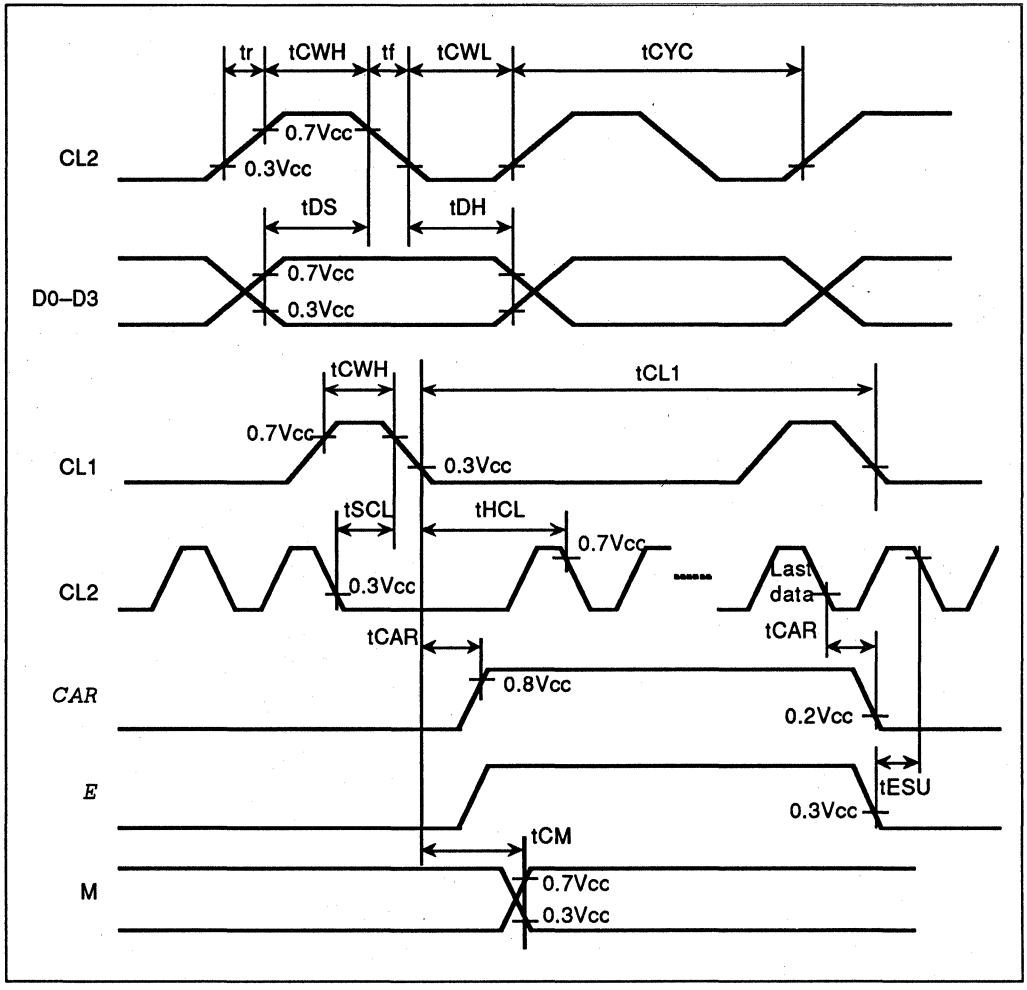


Figure 9 LCD Controller Interface Timing

HD66205

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

Description

The HD66205F/HD66205FL/HD66205TF/HD66205TFL/HD66205T/HD66205TL, the row LCD driver, features low output impedance and as many as 80 LCD outputs powered by 80 internal LCD drive circuits, and can drive a large liquid crystal graphic display. Because this device is fabricated by the CMOS process, it is suitable for battery-driven portable equipment, which fully utilizes the low power dissipation of liquid crystal elements. The HD66205 has a complete line-up: the HD66205F, a standard device powered by 5 V ± 10%; the HD66205FL, a 2.7–5.5 V, low power dissipation device; the HD66205TF and HD66205TFL, thin film package devices each powered by 5 V ± 10% and 2.7–5.5 V; and the HD66205T and HD66205TL, tape carrier package (TCP) devices powered by 5 V ± 10% and 2.7–5.5 V, respectively.

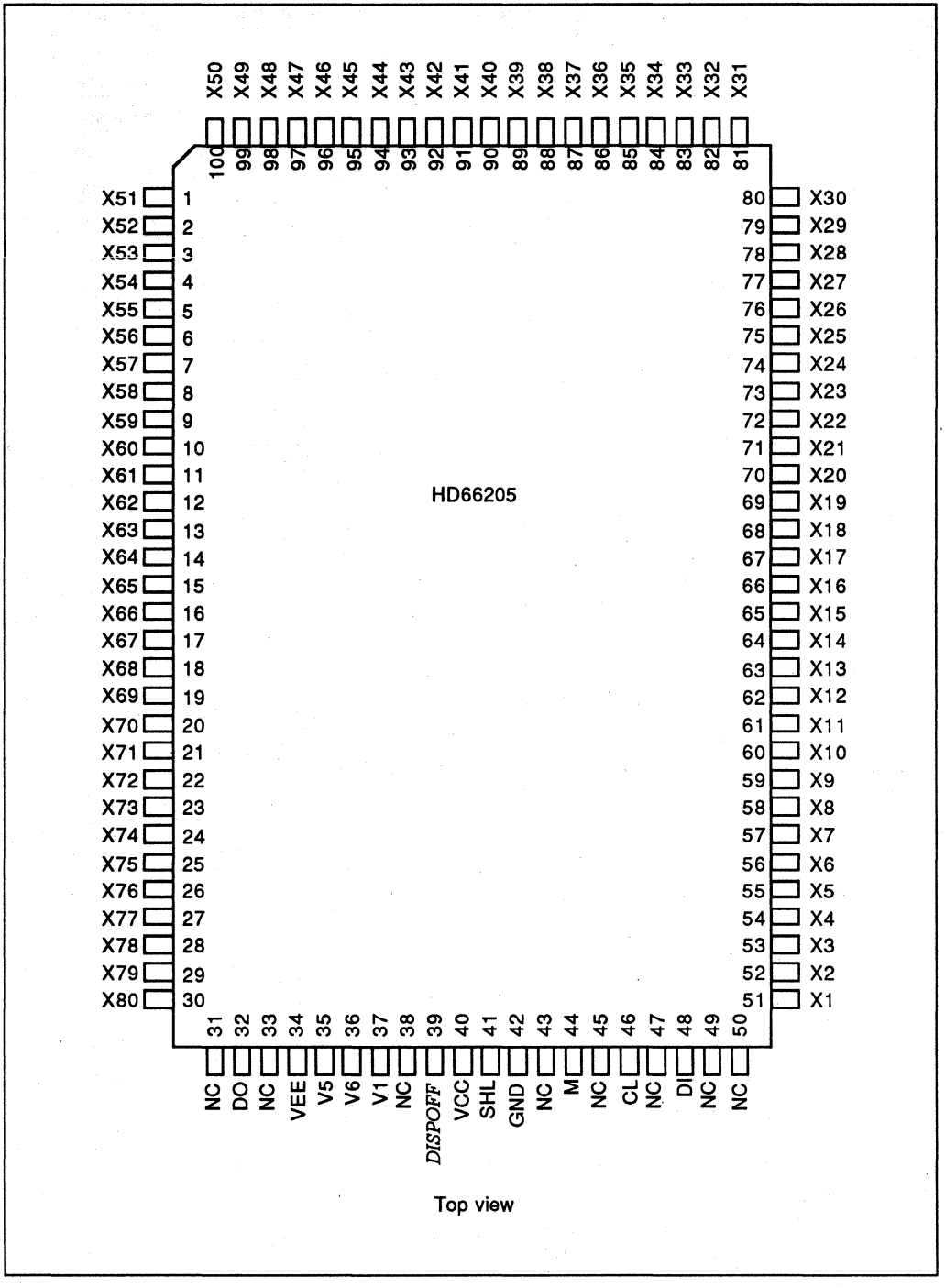
Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10–28 V
- Display off function
- Internal 80-bit shift register
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850

Ordering Information

Type No.	Voltage Range	Package
HD66205F	5 V ± 10%	FP-100 (flat package)
HD66205FL	2.7–5.5 V	FP-100 (flat package)
HD66205TF	5 V ± 10%	TFP-100 (thin flat package)
HD66205TFL	2.7–5.5 V	TFP-100 (thin flat package)
HD66205T	5 V ± 10%	TCP-92 (tape carrier package)
HD66205TL	2.7–5.5 V	TCP-92 (tape carrier package)

Pin Arrangement



Top view

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	40	V_{CC}	—	Power supply
GND	42	GND	—	Power supply
V_{EE}	34	V_{EE}	—	Power supply
V1	37	V1	Input	Power supply
V5	35	V5	Input	Power supply
V6	36	V6	Input	Power supply
CL	46	Clock	Input	Control signal
M	44	M	Input	Control signal
DI	48	Data in	Input	Control signal
DO	32	Data out	Output	Control signal
SHL	41	Shift left	Input	Control signal
$\overline{\text{DISPOFF}}$	39	Display off	Input	Control signal
X_1–X_{80}	51–100, 1–30	X1–X80	Output	LCD drive output
NC	31, 33, 38, 43, 45, 47, 49, 50	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V5, V6: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V5 and V6 are non-selected levels. See figure 1.

Control Signal

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts display data input via the DI pin.

M: Changes LCD drive outputs to AC.

DI: Inputs display data. DI of the first HD66205 must be connected to an LCD controller, and those of the other HD66205s must be connected to DI of the previous HD66205.

DO: Outputs display data. DO of the last HD66205 must be open, and those of the other HD66205s must be connected to DI of the next HD66205.

SHL: Selects the data shiftt direction for the shift register. See figure 2.

$\overline{\text{DISPOFF}}$: A low $\overline{\text{DISP}}$ sets LCD drive outputs X_1–X_{80} to V1 level.

LCD Drive Output

X_1–X_{80}: Each X outputs one of the four voltage levels V1, V5, V6, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

Other

NC: Must be open.

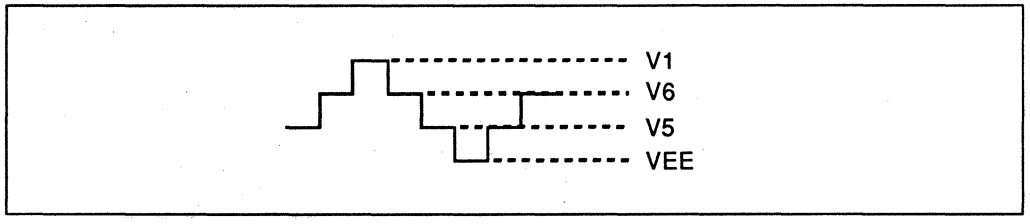


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

SHL level	Data shift directior	Common signa scan direction
Low	DI → SR1 → SR2 → SR80	X1 → X80
High	DI → SR80 → SR79 → SR1	X80 → X1

Figure 2 Selection of Display Data Shift Direction

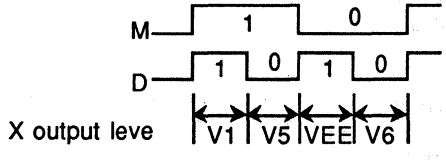


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V5, V6, and V_{EE}, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the shift register

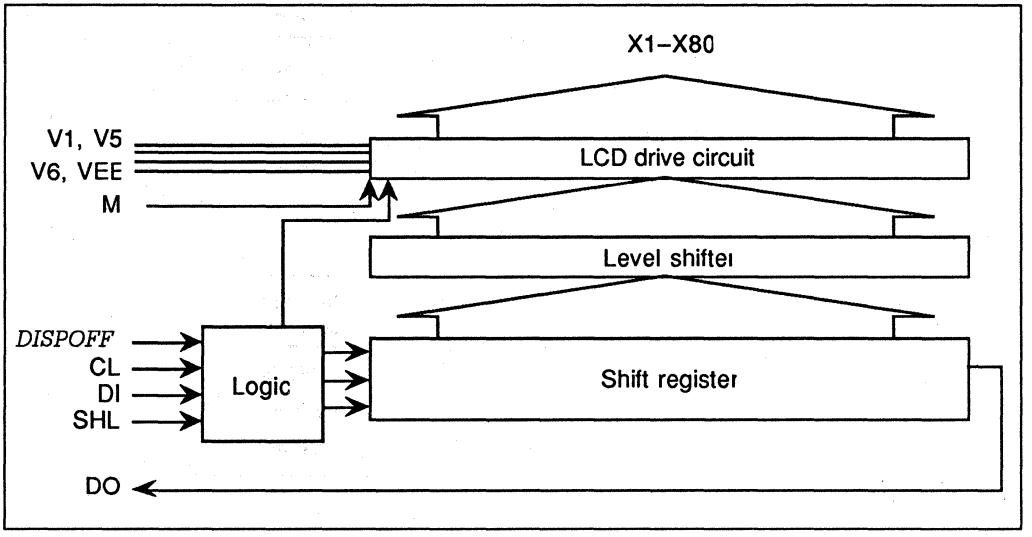
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Shift Register

The 80-bit shift register shifts data input via the DI pin by one bit, and the one bit of shifted-out data is output from the DO pin. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse

Block Diagram



Comparison of the HD66205 with the HD61105

Item	HD66205	HD61105
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Shift clock phase selection function	Not provided	Provided (FCS pin)
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V5, V6 (V2 level is the same as V_{EE} level)	V1, V2, V5, V6

SHL level	Data shift directior	Common signa scan direction
Low	DI → SR1 → SR2 → SR80	X1 → X80
High	DI → SR80 → SR79 → SR1	X80 → X1

HD66205

SHL level	Data shift directior	Common signa scan direction
Low	DI → SR80 → SR79 → SR1	X80 → X1
High	DI → SR1 → SR2 → SR80	X1 → X80

HD61105

Note the exact reverse relation for the two devices.

Figure 4 Relation between SHL and LCD Output Destinations for the HD66205 and HD61105

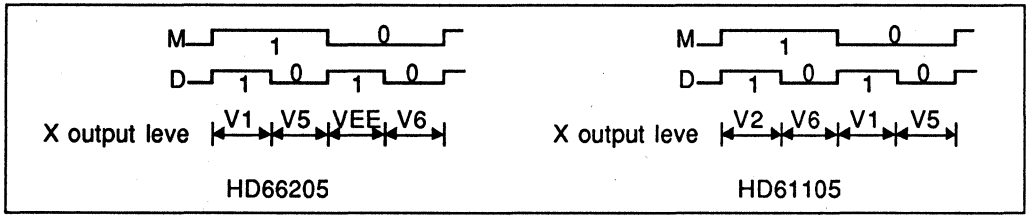


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66205 and HD61105

Operation Timing

Figure 6 shows the operation timing for the Application Example.

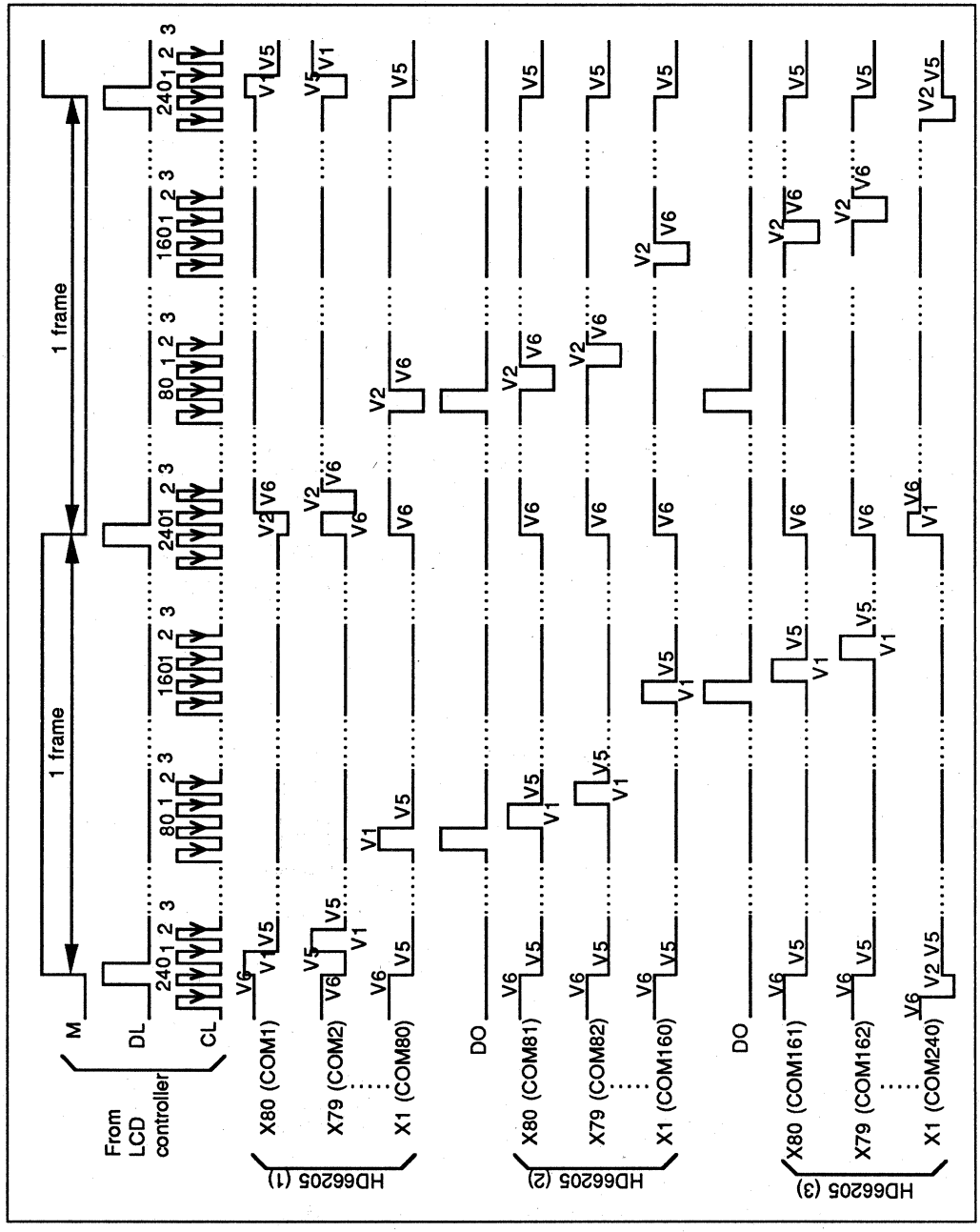
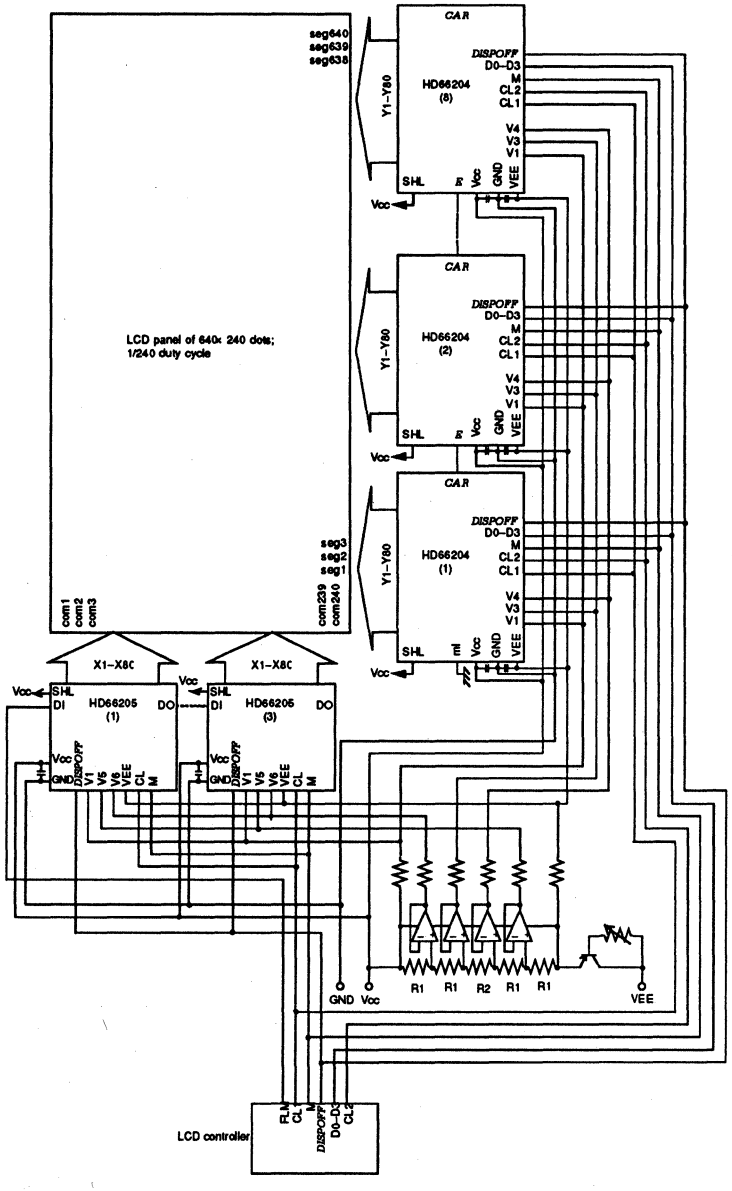


Figure 6 Relation between SHL and LCD Output Destinations

Application Example



Notes:
1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/15.
2. To stabilize the power supply, place two 0.1-μF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

8

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	4

Notes: 1. The reference point is GND (0 V).

2. Applies to pins CL, M, SHL, DI, $\overline{\text{DISPOFF}}$.
3. Applies to pins V1, V5, and V6.
4. –40 to +125°C for TCP devices.
5. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66205F/HD66205TF/HD66205T (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	2.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	100	µA	f_{CL} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2

Pins and notes on next page.

DC Characteristics for the HD66204FL/HD66204TFL/HD66204TL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	2.0	kΩ	I_{ON} = 100 mA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	$V_{IN} = V_{CC0}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	100	µA	f_{CL} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V	2
Current consumption 2	I_{EE}	—	—	250	µA	Same as above	2

Pins: 1. CL, M, SHL, DI, $\overline{\text{DISPOFF}}$

2. DO
3. X_1–X_{80}, V1, V5, V6
4. V1, V5, V6

Notes: 1. Indicates the resistance between one pin from X_1–X_{80} and another pin from V1, V5, V6, and V_{EE}, when load current is applied to the X pin; defined under the following conditions.

$V_{CC} - V_{EE}$= 28 V

V1, V6 = $V_{CC} - \{1/10(V_{CC} - V_{EE})\}$

V5 = $V_{EE} + \{1/10(V_{CC} - V_{EE})\}$

V1 and V6 should be near V_{CC} level, and V5 should be near V_{EE} level (figure 7). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 8).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

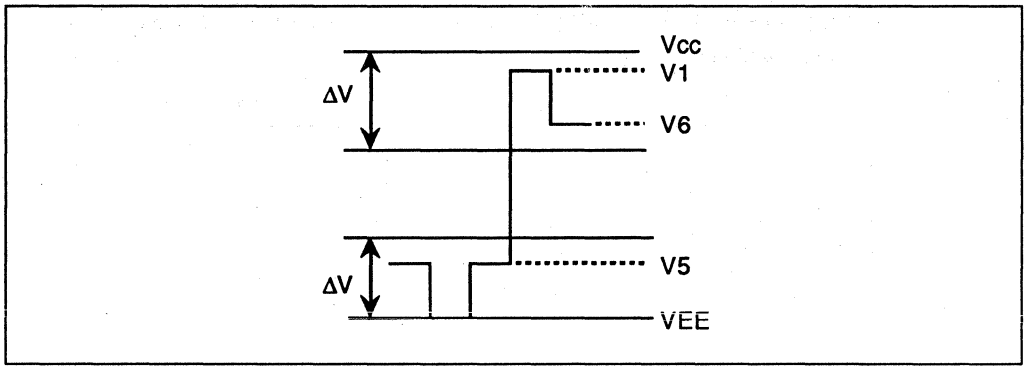


Figure 7 Relation between Driver Output Waveform and Level Voltages

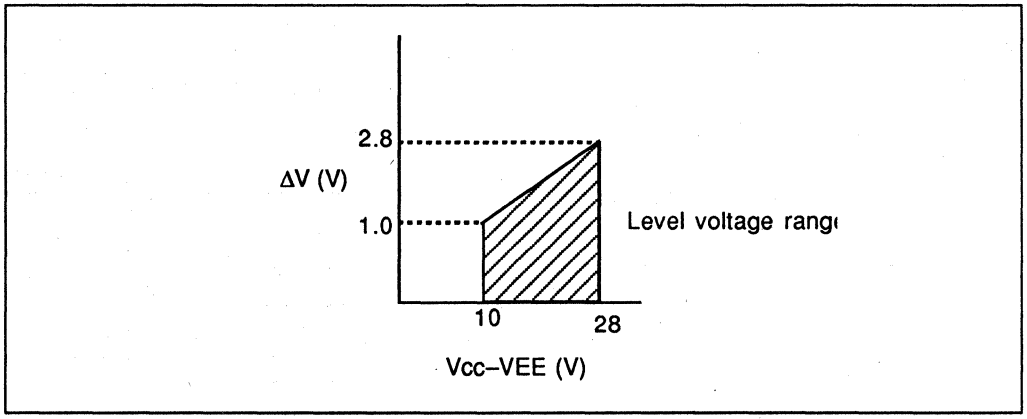


Figure 8 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66205F/HD66205TF/HD66205T (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL	10	—	µs	
Clock high-level width 1	t_{CWH}	CL	50	—	ns	
Clock low-level width	t_{CWL}	CL	1.0	—	µs	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, CL	100	—	ns	
Data hold time	t_{DH}	DI, CL	100	—	ns	
Data output delay time	t_{DD}	DO, CL	—	3.0	µs	1
Data output hold time	t_{DHW}	DO, CL	100	—	ns	

AC Characteristics for the HD66205FL/HD66205TFL/HD66205TL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL	10	—	µs	
Clock high-level width 1	t_{CWH}	CL	80	—	ns	
Clock low-level width	t_{CWL}	CL	1.0	—	µs	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, CL	100	—	ns	
Data hold time	t_{DH}	DI, CL	100	—	ns	
Data output delay time	t_{DD}	DO, CL	—	7.0	µs	1
Data output hold time	t_{DHW}	DO, CL	100	—	ns	

Notes: 1. The load circuit shown in figure 9 is connected.

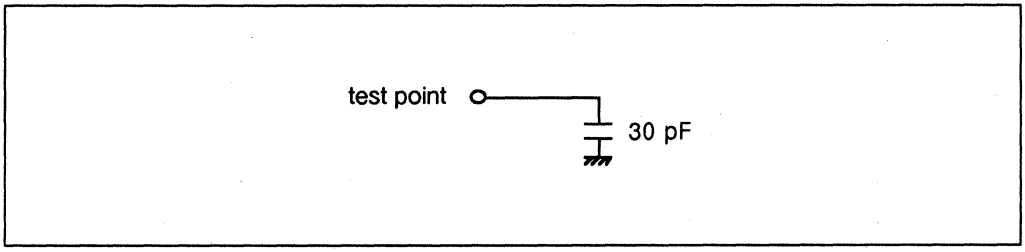


Figure 9 Load Circuit

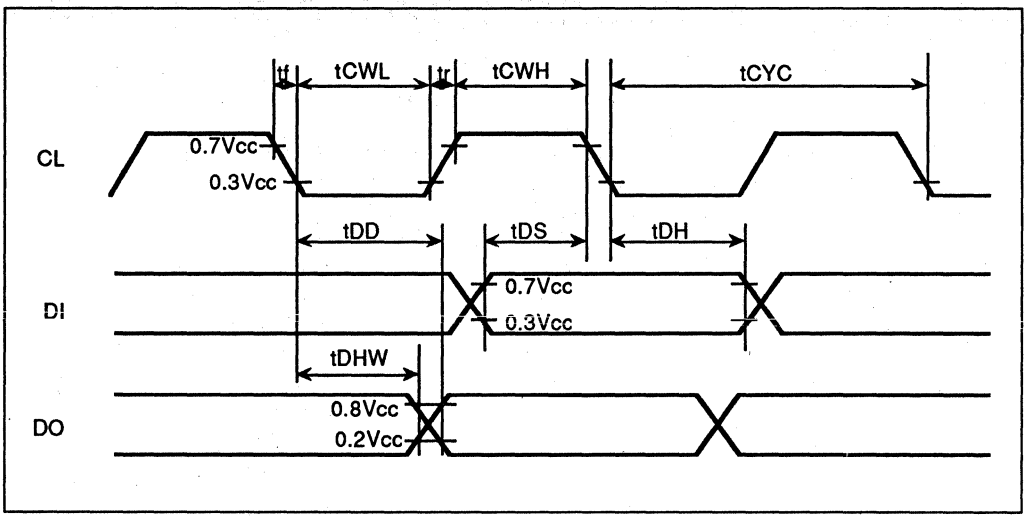


Figure 10 LCD Controller Interface Timing

HD66214T/HD66214TL (Micro-TAB)— (80-Channel Column Driver in Micro-TCP)

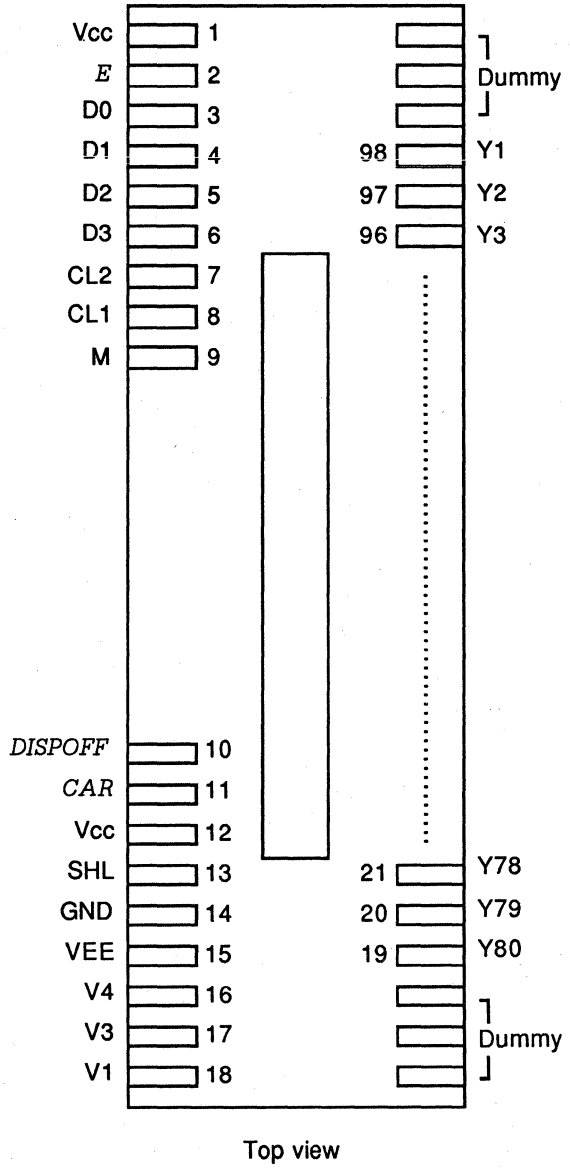
Description

The HD66214T/HD66214TL, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66214, packaged in an 8-mm-wide micro-tape carrier package (micro-TCP), enables a compact LCD system with a narrower frame (peripheral areas for LCD drivers) —about half as large as that os an existing system. The HD66214 provides HD66214T, a standard device powered by 5 V ± 10%, and HD66214TL, a low power dissipation device powered by 2.7–5.5 V suitable for battery-driven portable equipment such as notebook personal computers and palm-top personal computers.

Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10–28 V
- High clock speed
  - — 8 MHz max under 5-V operation (HD66214T)
  - — 4 MHz max under 3-V operation (HD66244TL)
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850
- 98-pin TCP

Pin Arrangement



Top view

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	1, 12	V_{CC}	—	Power supply
GND	14	GND	—	Power supply
V_{EE}	15	V_{EE}	—	Power supply
V1	18	V1	Input	Power supply
V3	17	V3	Input	Power supply
V4	16	V4	Input	Power supply
CL1	8	Clock 1	Input	Control signal
CL2	7	Clock 2	Input	Control signal
M	9	M	Input	Control signal
D_0–D_3	3–6	Data 0–data 3	Input	Control signal
SHL	13	Shift left	Input	Control signal
$\overline{E}$	2	Enable	Input	Control signal
$\overline{CAR}$	11	Carry	Output	Control signal
$\overline{DISPOFF}$	10	Display off	Input	Control signal
Y_1–Y_{80}	19–98	Y1–Y80	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. Vcc–VEE supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D_0–D_3 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_3: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66214 if HD66214s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{80} to V1 level.

LCD Drive Output

Y_1–Y_{80}: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

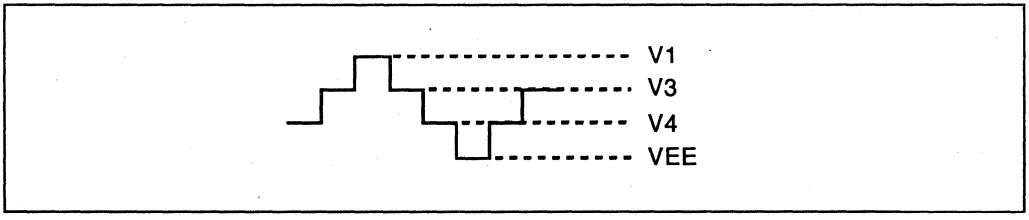


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

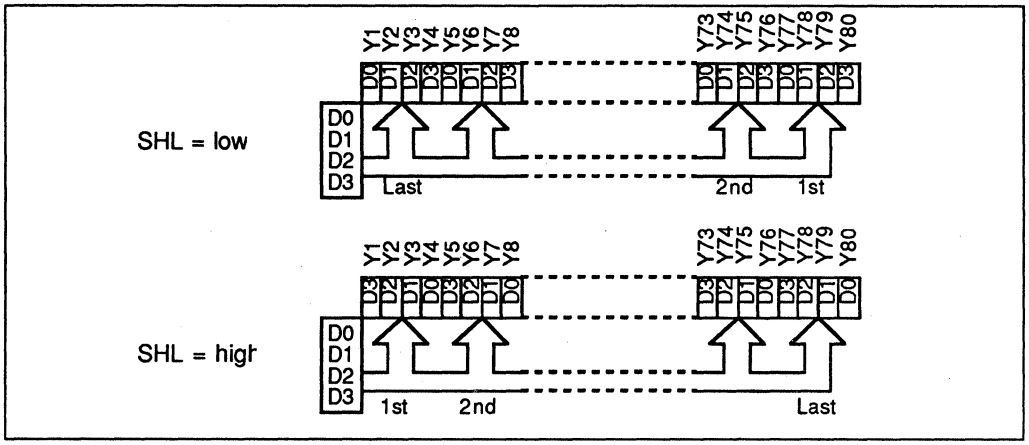


Figure 2 Selection of Destinations of Display Data Output

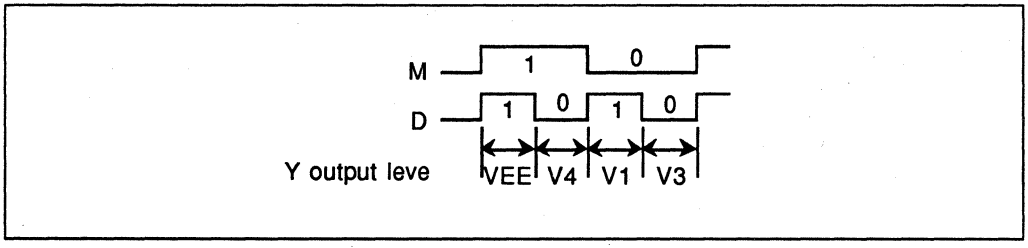


Figure 3 Selection of LCD Drive Output Level

Block Functions

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D0 to D3 pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

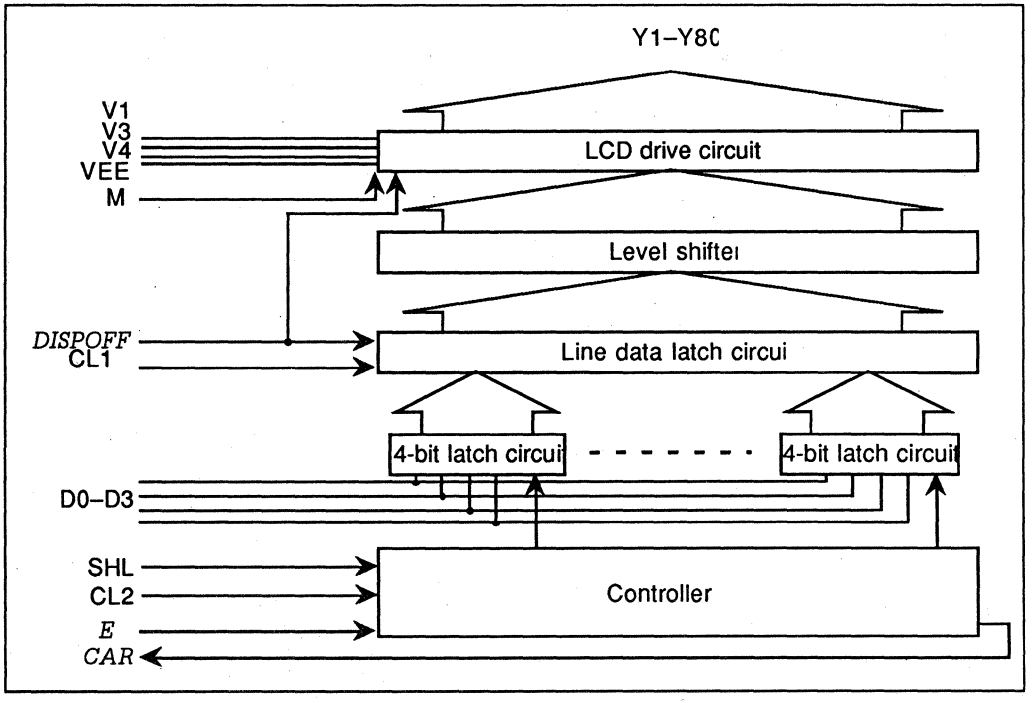
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and VEE, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



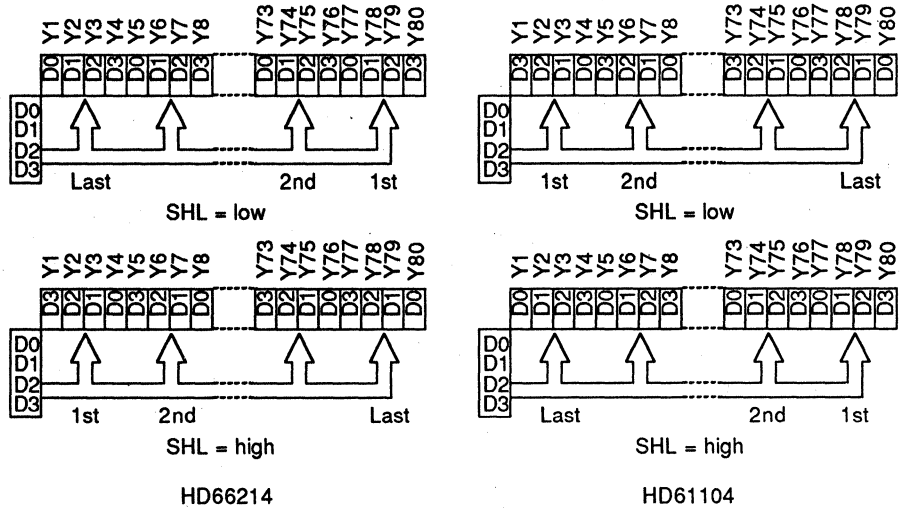
Ordering Information

Type No.	Voltage Range	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66214TA1	5 V ± 10%	0.15 mm	0.80 mm	3 sprocket holes
HD66214TA1L	2.7–5.5 V	0.15 mm	0.80 mm	3 sprocket holes
HD66214TA2	5 V ± 10%	0.18 mm	0.80 mm	3 sprocket holes
HD66214TA2L	2.7–5.5 V	0.18 mm	0.80 mm	3 sprocket holes
HD66214TA3	5 V ± 10%	0.20 mm	0.80 mm	3 sprocket holes
HD66214TA3L	2.7–5.5 V	0.20 mm	0.80 mm	3 sprocket holes
HD66214TA4	5 V ± 10%	0.22 mm	0.80 mm	3 sprocket holes
HD66214TA4L	2.7–5.5 V	0.22 mm	0.80 mm	3 sprocket holes
HD66214TA5	5 V ± 10%	0.25 mm	0.80 mm	3 sprocket holes
HD66214TA5L	2.7–5.5 V	0.25 mm	0.80 mm	3 sprocket holes
HD66214TA6	5 V ± 10%	0.20 mm	0.45 mm	3 sprocket holes
HD66214TA6L	2.7–5.5 V	0.20 mm	0.45 mm	3 sprocket holes
HD66214TA7	5 V ± 10%	0.22 mm	0.45 mm	3 sprocket holes
HD66214TA7L	2.7–5.5 V	0.22 mm	0.45 mm	3 sprocket holes
HD66214TA8	5 V ± 10%	0.25 mm	0.55 mm	3 sprocket holes
HD66214TA8L	2.7–5.5 V	0.25 mm	0.55 mm	3 sprocket holes

Notes:
1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75 mm.
4. Tape film is Upirex (a trademark of Ube Industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.

Comparison of the HD66214 with the HD61104

Item	HD66214	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as VEE level)	V1, V2, V3, V4
Storage temperature	–40 to 125°C	–55 to 125°C
Package	TCP (tape carrier package)	QFP (quad flat package)



Note the exact reverse relation for the two devices.

Figure 4 Relation between SHL and LCD Output Destinations for the HD66214 and HD61104

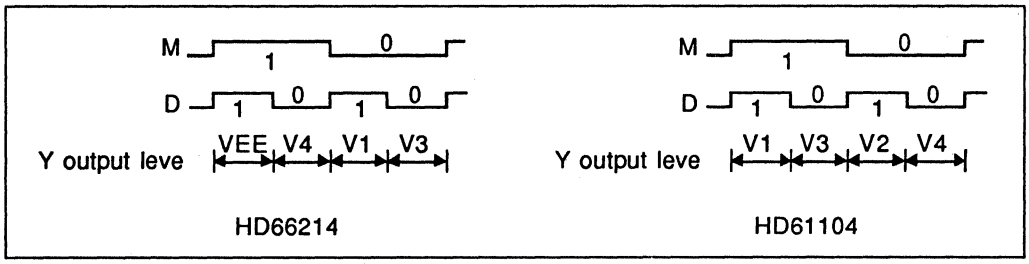
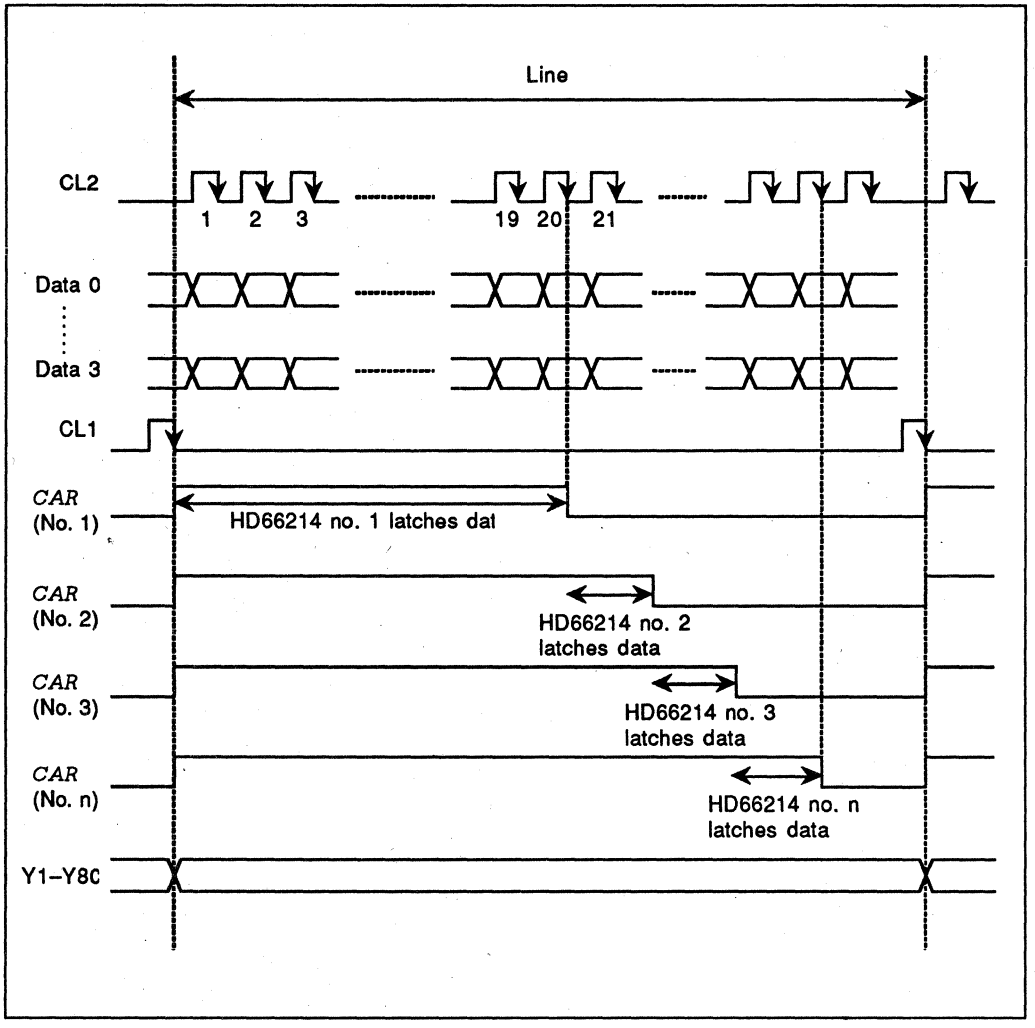
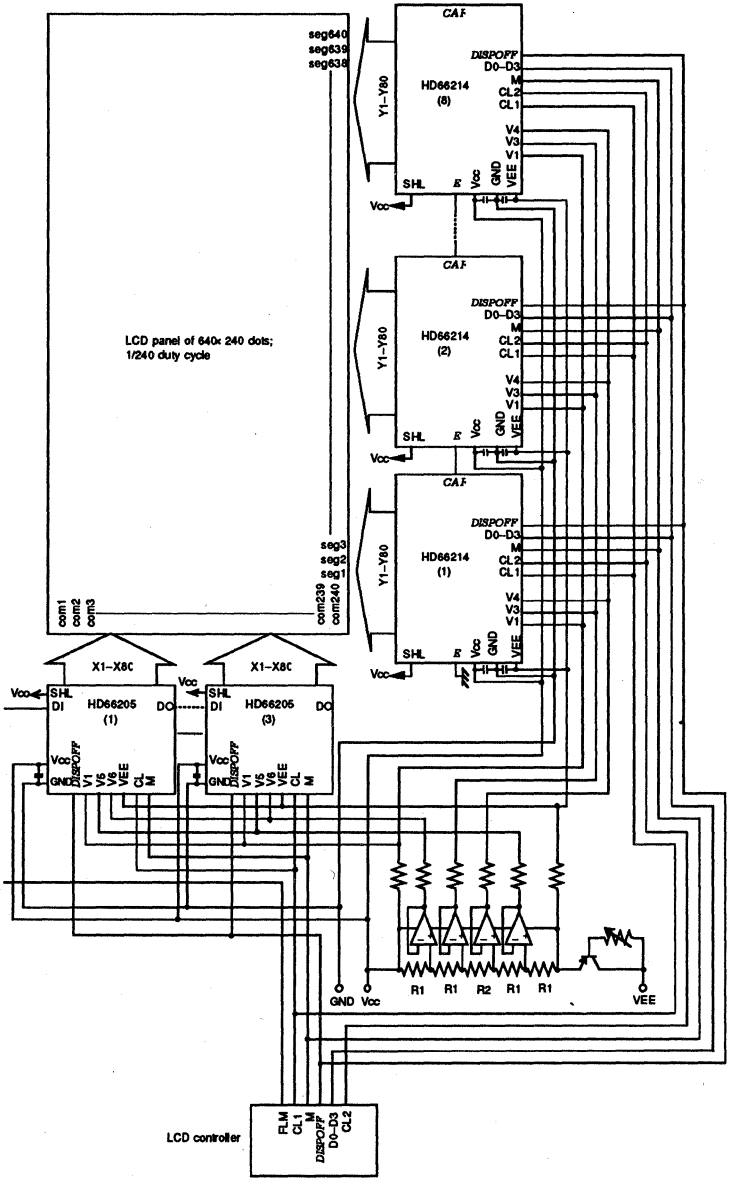


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66214 and HD61104

Operation Timing



Application Example



Notes:
1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/15.
2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0 V).

2. Applies to pins CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$.

3. Applies to pins V1, V3, and V4.

4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66214T (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	µA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics for the HD66214TL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	1	0.7 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	1	0	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	f_{CL2} = 4.0 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	50	µA	Same as above	2, 3

Pins: 1. CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$

2. $\overline{CAR}$

3. Y_1–Y_{80}, V1, V3, V4

4. V1, V3, V4

Notes: 1. Indicates the resistance between one pin from Y_1–Y_{80} and another pin from V1, V3, V4, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions.

V_{CC} – GND = 28 V

V1, V3 = $V_{CC} - \{2/10(V_{CC} - V_{EE})\}$

V4 = $V_{EE} + \{2/10(V_{CC} - V_{EE})\}$

V1 and V3 should be near Vcc level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 7).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

3. Applies to standby mode.

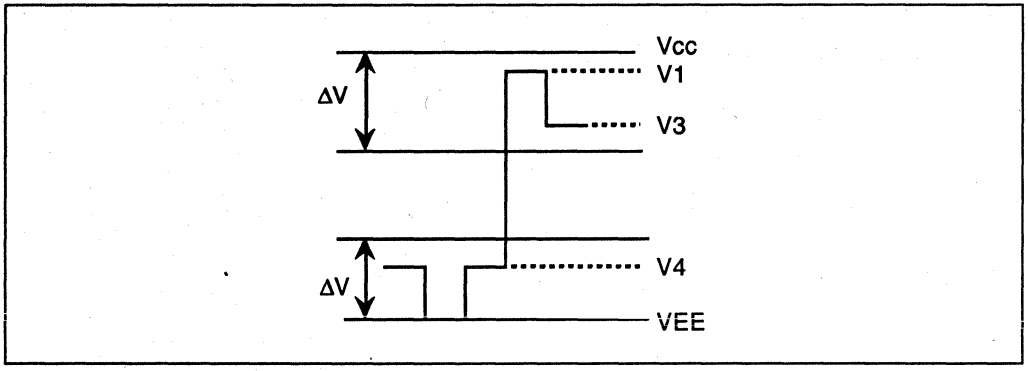


Figure 6 Relation between Driver Output Waveform and Level Voltages

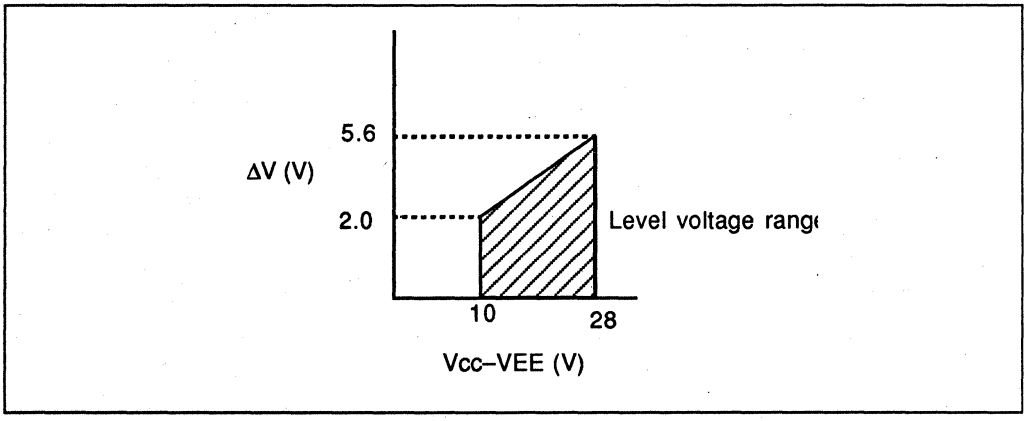


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66214T (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	20	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	20	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	30	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics for the HD66214TL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	120	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	50	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	50	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	65	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

Notes: 1. t_r, $t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \leq 50$ ns

2. The load circuit shown in figure 8 is connected.

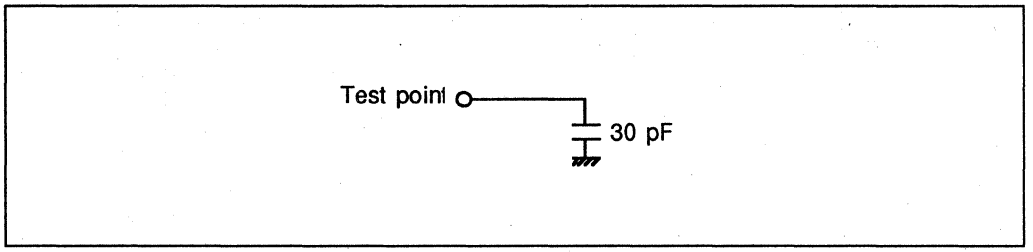


Figure 8 Load Circuit

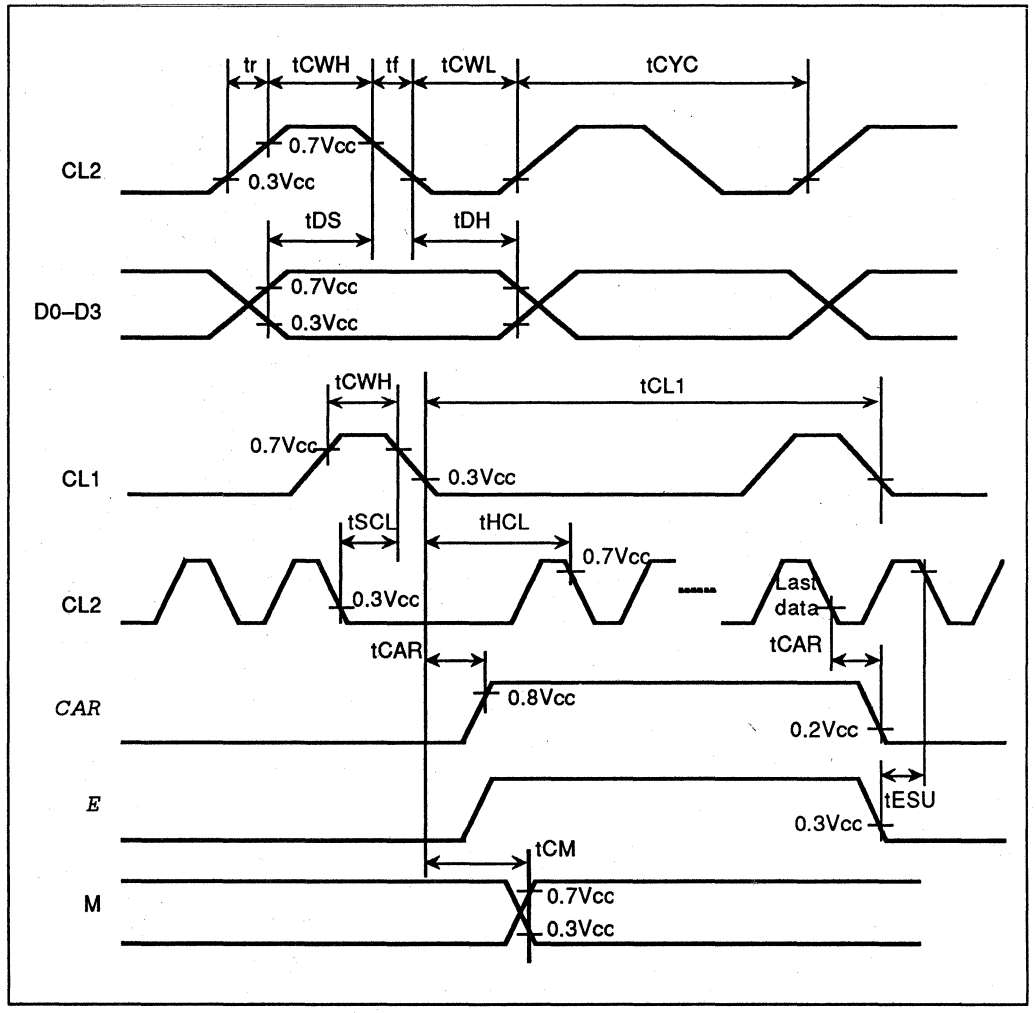


Figure 9 LCD Controller Interface Timing

HD66702 LCD-II/E20
(Dot Matrix Liquid Crystal Display Controller and Driver)

—Preliminary—

Description

The LCD-II/E20 (HD66702) dot matrix liquid crystal display controller and driver LSI displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microprocessor control. Since all the functions required for dot matrix liquid crystal display drive are internally provided on one chip, a small system can be configured with this LSI.

A single LCD-II/E20 can display up to two lines, each of 20 characters. The addition of driver LSI HD44100s enables a maximum display of two lines, each of 40 characters.

The LCD-II/E20 of 3-V power supply (whose development is under consideration) is suitable for any portable battery-driven apparatus requiring low power dissipation.

Ordering Information

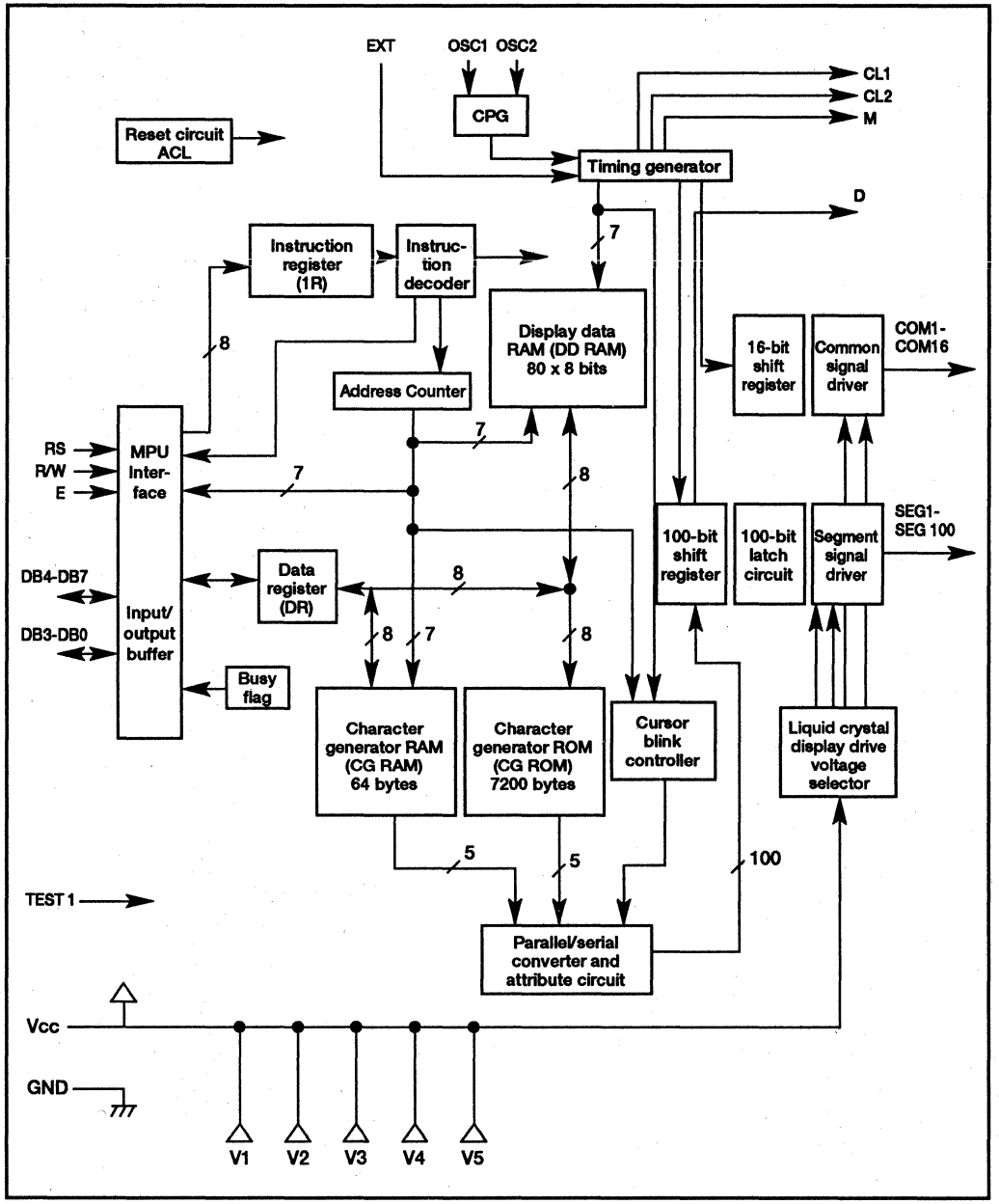
Type No.	Package	Operating Voltage
HCD66702	144-pin bare chip	4.5 to 5.5 V
HCD66702L	144-pin bare chip	2.7 to 3.3 V

Features

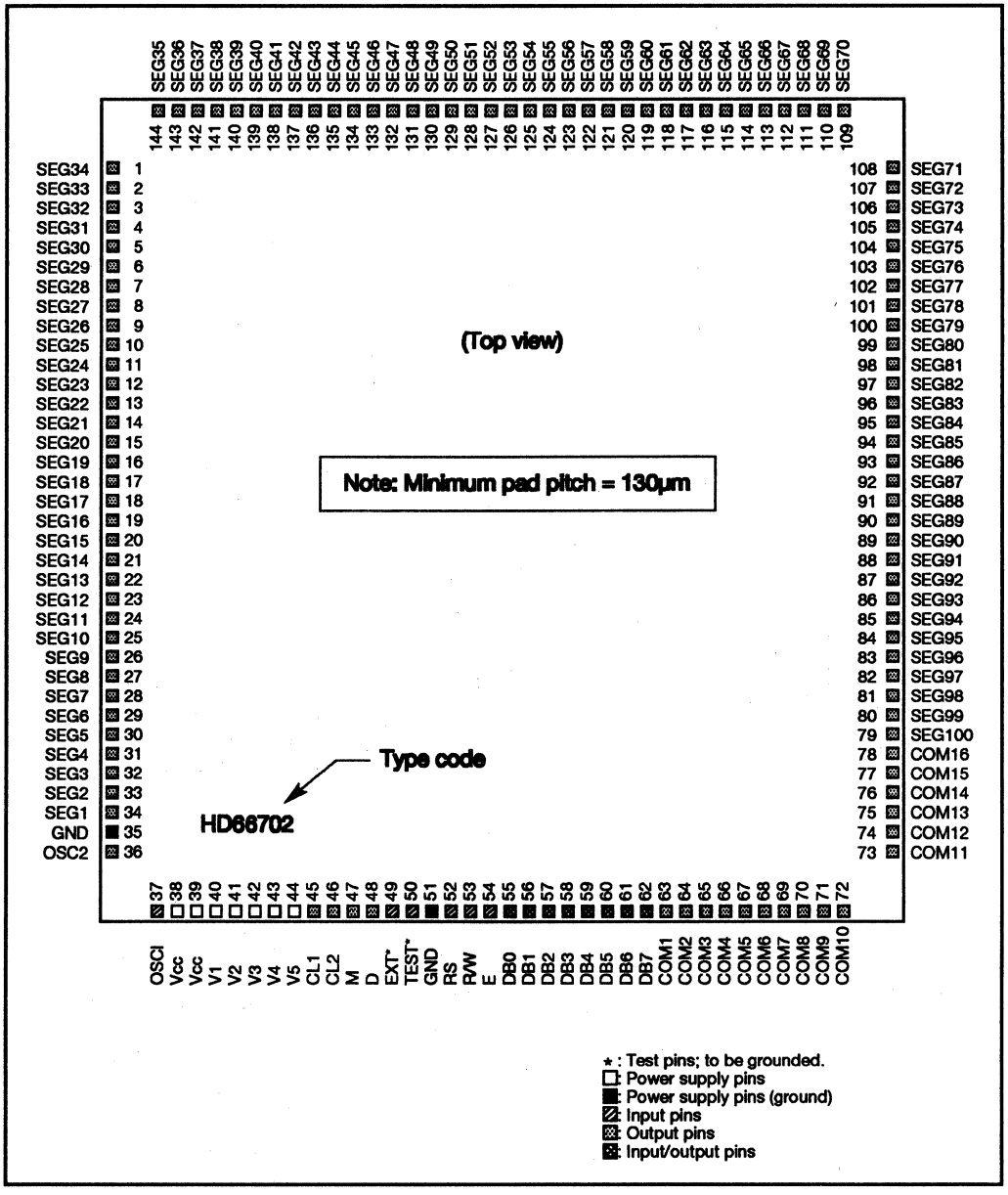
- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller and driver
- Internal display RAM of 80 × 8 bits (80 characters max.)
- Internal character generator ROM of 7200 bits:
  160 character fonts of 5 × 7 dots
  32 character fonts of 5 × 10 dots
- Internal character generator RAM of 64 × 8 bits:
  8 character fonts of 5 × 7 dots
  4 character fonts of 5 × 10 dots
- Internal liquid crystal display driver with 16 common signal drivers and 100 segment signal drivers
- Programmable duty cycles
  — 1/8 for 1 line of 5 × 7 dots + cursor
  — 1/11 for 1 line of 5 × 10 dots + cursor
  — 1/16 for 2 lines of 5 × 7 dots + cursor
- **Maximum display characters**
- Wide range of instruction functions:
  — Display clear, Cursor home, Display On/Off, Cursor On/Off, Display character blink, Cursor shift, Display shift
- Wide range of power supply (V_{cc}): 4.5 to 5.5 V (standard version), 2.7 to 3.3 V (low V_{cc} version)
- Internal automatic reset circuit after power on (provided by standard version only)
- Independent LCD drive voltage on the logic power supply (V_{cc}): 3.0 to 6.0 V

Display Type	Duty Cycle	When not Extended	When Extended with an HD44100H	Maximum Extension
1-line display	1/8	20 characters × 1 line	28 characters × 1 line	80 characters × 1 line
	1/11	20 characters × 1 line	28 characters × 1 line	80 characters × 1 line
2-line display	1/16	20 characters × 2 lines	28 characters × 2 lines	40 characters × 2 lines

Block Diagram (LCD-II/E20 Interior)



LCD-II/E20 Pad Arrangement



LCD-II Family Comparison

Item		LCD-II (HD44780)	LCD-II/A (HD66780)	LCD-II/E20 (HD66702)
Power supply voltage		5 V ± 10%	5 V ± 10%	5 V ± 10% for standard version; 3 V ± 10% for low V_{CC} version
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11 V	3.0 V to V_{CC}	3.0 to 6.0 V
	1/5 bias	4.6 to 11 V	3.0 V to V_{CC}	3.0 to 6.0 V
Max display digits per chip		16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)	40 digits (20 digits × 2 lines)
Display duty cycle		1/8, 1/11 and 1/16	1/8, 1/11 and 1/16	1/8, 1/11 and 1/16
CG ROM		7,200 bits (160 character fonts of 5 × 7 dots and 32 character fonts of 5 × 10 dots)	12,000 bits (240 character fonts of 5 × 10 dots)	7,200 bits (160 character fonts of 5 × 7 dots and 32 character fonts of 5 × 10 dots)
CG RAM		64 bytes	64 bytes	64 bytes
DD RAM		80 bytes	80 bytes	80 bytes
Segment signals		40	40	100
Common signals		16	16	16
Liquid crystal drive waveform		A	B	B
Ladder resistor for liquid crystal drive power supply		External	External	External
Clock source		External resistor, external ceramic filter, or external clock	External resistor, external ceramic filter, or external clock	External resistor, or external clock
Rf oscillation frequency (frame frequency)		270 kHz ± 30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ± 30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ± 30% (69 to 128 Hz for 1/8 and 1/16 duty cycles; 50 to 93 Hz for 1/11 duty cycle)
Rf resistance		91 kΩ ± 2%	83 kΩ ± 2%	68 kΩ (T.B.D.) for standard version; 56 kΩ (T.B.D.) for low V_{CC} version
Instructions		Fully compatible within the LCD-II family		
CPU bus timing		1 MHz	2 MHz	1 MHz
Package		QFP1420-80, QFP1414-80, and 80-pin bare chip	QFP1420-80 and QFP1414-80	144-pin bare chip (no package)

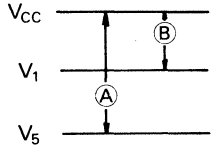
Note: Development of QFP2020-144 (144-pin quad flat package) is under consideration.

Electrical Characteristics

Absolute Maximum Ratings for Low V_{CC} Version

Item	Symbol	Unit	Rating	Note
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	
Power supply voltage (2)	V_1 to V_5	V	–0.3 to +7.0	3
Input voltage	V_t	V	–0.3 to V_{CC} + 0.3	
Operating temperature	T_{opr}	°C	–20 to + 75	4
Storage temperature	T_{stg}	°C	–55 to + 125	

Notes: 1. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to V_1 to V_5; must maintain $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$; see below.



Ⓐ = $V_{CC} - V_5$
Ⓑ = $V_{CC} - V_1$
Ⓐ ≧ 1.5 V
Ⓑ ≦ 0.25 × Ⓐ

The conditions of V_1 and V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage VLCD."

4. This temperature is for packaged devices; +75°C is the guaranteed operating temperature for bare chip devices.

DC Characteristics for Low V_{CC} Version (V_{CC} = 3 V ± 10%, T_a = –20°C to +75°C*1)

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
Input high voltage (1)	V_{IH1}	V		T.B.D.	—	V_{CC}	2
Input low voltage (1)	V_{IL1}	V		–0.3	—	T.B.D.	2
Input high voltage (2) (OSC1)	V_{IH2}	V		T.B.D.	—	V_{CC}	11
Input low voltage (2) (OSC1)	V_{IL2}	V		—	—	T.B.D.	11
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	V	$-I_{OH}$ = 0.1 mA	T.B.D.	—	—	3
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	V	I_{OL} = 0.1 mA	—	—	T.B.D.	3
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	V	$-I_{OH}$ = 0.04 mA	T.B.D.	—	—	4
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	V	I_{OL} = 0.04 mA	—	—	T.B.D.	4
Driver ON resistance (COM pin)	R_{COM}	kΩ	± I_d = 0.05 mA (all COM pins)	—	—	20	9
Driver ON resistance (SEG pin)	R_{SEG}	kΩ	± I_d = 0.05 mA (all SEG pins)	—	—	30	9
Input/Output leakage current	I_{LI}	µA	V_{in} = 0 to V_{CC}	–1	—	1	5
Pull-up MOS current (RS, R/W)	$-I_p$	µA	V_{CC} = 3 V	T.B.D.	T.B.D.	T.B.D.	
Power supply current	I_{CC}	mA	Rf oscillation, external clock operation, V_{CC} = 3 V f_{OSC} = 320 kHz		T.B.D.		6, 10
LCD voltage	V_{LCD1}	V	$V_{CC} - V_5$ 1/5 bias	3.0	—	6.0	12
	V_{LCD2}	V	$V_{CC} - V_5$ 1/4 bias	3.0	—	6.0	12

Notes for DC Characteristics on pages 983 and 984.

AC Characteristics for Low V_{cc} Version (V_{cc} = 3 V ± 10%, T_a = –20°C to +75°C*1)

Clock Characteristics

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
External clock operating frequency	f_{cp}	kHz		125	—	410	7
External clock duty cycle	Duty	%		45	50	55	7
External clock rise time	t_{rcp}	µs		—	—	0.2	7
External clock fall time	t_{rcp}	µs		—	—	0.2	7
Rf oscillation internal clock operating frequency	f_{OSC}	kHz	Rf = T.B.D.	230	320	410	8

Notes on pages 983 and 984

Bus Timing Characteristics

Write Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 1	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 1	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 1	40	—	—
Address hold time	t_{AH}	ns	Figure 1	10	—	—
Data setup time	t_{DSW}	ns	Figure 1	195	—	—
Data hold time	t_H	ns	Figure 1	10	—	—

Read Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 2	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 2	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 2	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 2	40	—	—
Address hold time	t_{AH}	ns	Figure 2	10	—	—
Data delay time	t_{DDR}	ns	Figure 2	—	—	320
Data hold time	t_{DHR}	ns	Figure 2	20	—	—

Segment extension signal timing

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Clock pulse high level width	t_{CWH}	ns	Figure 3	800	—	—
Clock pulse low level width	t_{CWL}	ns	Figure 3	800	—	—
Clock setup time	t_{CSU}	ns	Figure 3	500	—	—
Data setup time	t_{SU}	ns	Figure 3	300	—	—
Data hold time	t_{DH}	ns	Figure 3	300	—	—
M delay time	t_{DM}	ns	Figure 3	–1000	—	1000
Clock rise/fall time	t_{ct}	ns	Figure 3		—	100

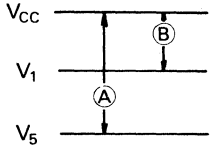
Power supply conditions for using internal reset circuit
Since the internal reset circuit will not operate normally in the 3-V V_{cc} LCD-II/E20, initialize the LSI by instruction.

Bus Timing Characteristics

Absolute Maximum Ratings for Standard V_{cc} Version

Item	Symbol	Unit	Rating	Note
Power supply voltage (1)	V_{cc}	V	–0.3 to +7.0	
Power supply voltage (2)	V_1 to V_5	V	–0.3 to +7.0	3
Input voltage	V_t	V	–0.3 to V_{cc} + 0.3	
Operating temperature	T_{opr}	°C	–20 to + 75	4
Storage temperature	T_{stg}	°C	–55 to + 125	

Notes: 1. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to V_1 to V_5; must maintain $V_{cc} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$; see below.



Ⓐ = $V_{cc} - V_5$
Ⓑ = $V_{cc} - V_1$
Ⓐ ≧ 1.5 V
Ⓑ ≦ 0.25 × Ⓐ

The conditions of V_1 and V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage VLCD."

4. This temperature is for packaged devices; +75°C is the guaranteed operating temperature for bare chip devices.

DC Characteristics for Standard Version (V_{cc} = 5 V ± 10%, T_a = –20°C to +75°C*1)

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
Input high voltage (1)	V_{IH1}	V		2.2	—	V_{cc}	2
Input low voltage (1)	V_{IL1}	V		–0.3	—	0.6	2
Input high voltage (2) (OSC1)	V_{IH2}	V		V_{cc} – 1	—	V_{cc}	11
Input low voltage (2) (OSC1)	V_{IL2}	V		—	—	1.0	11
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	V	$-I_{OH}$ = 0.205 mA	2.4	—	—	3
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	V	I_{OL} = 1.6 mA	—	—	0.4	3
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	V	$-I_{OH}$ = 0.04 mA	0.9 V_{cc}	—	—	4
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	V	I_{OL} = 0.04 mA	—	—	0.1 V_{cc}	4
Driver ON resistance (COM pin)	R_{COM}	kΩ	± I_d = 0.05 mA (all COM pins)	—	—	20	9
Driver ON resistance (SEG pin)	R_{SEG}	kΩ	± I_d = 0.05 mA (all SEG pins)	—	—	30	9
Input/Output leakage current	I_{LI}	µA	V_{in} = 0 to V_{cc}	–1	—	1	5
Pull-up MOS current (RS, R/W)	$-I_p$	µA	V_{cc} = 5 V	T.B.D.	125	T.B.D.	
Power supply current for RS, R/W	I_{cc}	mA	Rf oscillation, external clock operation, V_{cc} = 5 V f_{OSC} = 320 kHz		T.B.D.		6, 10
LCD voltage	V_{LCD1}	V	$V_{cc} - V_5$ 1/5 bias	3.0	—	6.0	12
	V_{LCD2}	V	$V_{cc} - V_5$ 1/4 bias	3.0	—	6.0	12

Notes for DC Characteristics on pages 983 and 984.

AC Characteristics for Standard Version (V_{cc} = 5 V ± 10%, T_a = –20°C to +75°C*1)

Clock Characteristics

Item	Symbol	Unit	Test Conditions	min.	typ.	max.	Note
External clock operating frequency	f_{cp}	kHz		125	—	410	7
External clock duty cycle	Duty	%		45	50	55	7
External clock rise time	t_{rcp}	µs		—	—	0.2	7
External clock fall time	t_{rcp}	µs		—	—	0.2	7
Rf oscillation internal clock operating frequency	f_{OSC}	kHz	Rf = T.B.D.	230	320	410	8

Notes on pages 983 and 984

Bus Timing Characteristics (see note on page 14 for load circuits)

Write Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 1	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 1	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 1	40	—	—
Address hold time	t_{AH}	ns	Figure 1	10	—	—
Data setup time	t_{DSW}	ns	Figure 1	195	—	—
Data hold time	t_H	ns	Figure 1	10	—	—

Read Operation

Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Enable cycle time	t_{CYCE}	ns	Figure 2	1000	—	—
Enable pulse high level width	PW_{EH}	ns	Figure 2	450	—	—
Enable rise/fall time	t_{Er}, t_{Ef}	ns	Figure 2	—	—	25
Setup time for RS, R/W, E	t_{AS}	ns	Figure 2	40	—	—
Address hold time	t_{AH}	ns	Figure 2	10	—	—
Data delay time	t_{DDR}	ns	Figure 2	—	—	320
Data hold time	t_{DHR}	ns	Figure 2	20	—	—

Segment extension signal timing

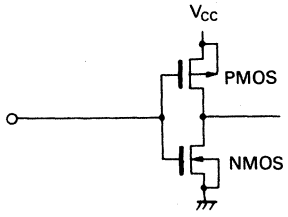
Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Clock pulse high level width	t_{CWH}	ns	Figure 3	800	—	—
Clock pulse low level width	t_{CWL}	ns	Figure 3	800	—	—
Clock setup time	t_{CSU}	ns	Figure 3	500	—	—
Data setup time	t_{SU}	ns	Figure 3	300	—	—
Data hold time	t_{DH}	ns	Figure 3	300	—	—
M delay time	t_{DM}	ns	Figure 3	–1000	—	1000
Clock rise/fall time	t_{ct}	ns	Figure 3	—	—	100

Power supply conditions for using internal reset circuit

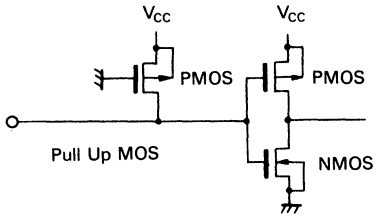
Item	Symbol	Unit	Test Conditions	min.	typ.	max.
Power supply rise time	t_{rCC}	ms	Figure 4	0.1	—	10
Power supply off time	t_{OFF}	ms	Figure 4	1	—	—

Note: 1. The following are I/O terminal configurations except for liquid crystal display output.

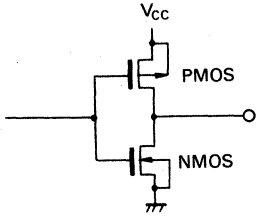
- Input Terminal Applicable Terminals: E
  (MOS without pull up)



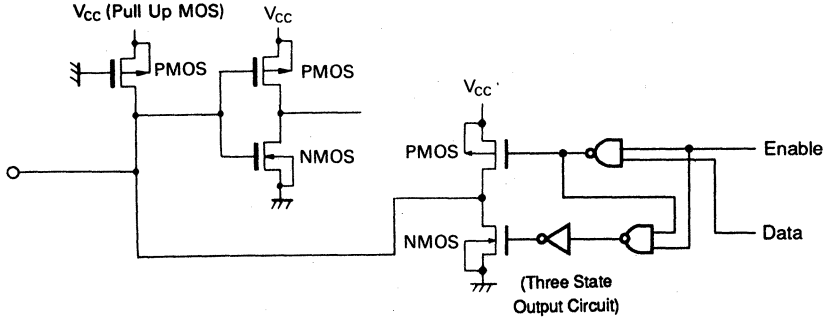
- Applicable Terminals: RS, R/W
  (MOS with pull up)



- Output Terminal
  Applicable Terminals: CL_1, CL_2, M, D



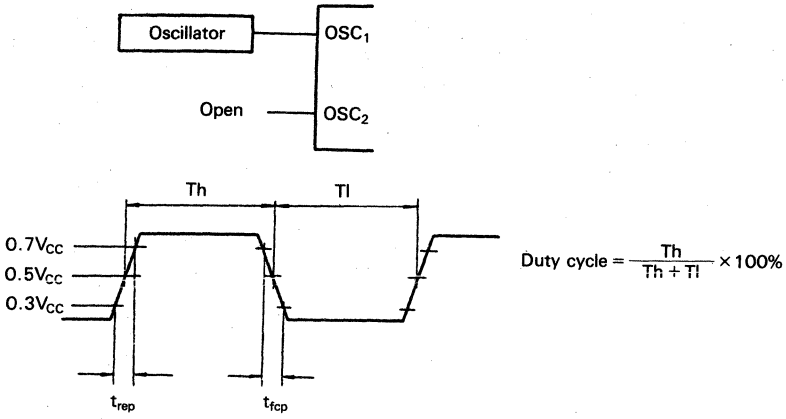
- I/O Terminal
  Applicable Terminals: DB_0 to DB_7



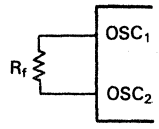
Note: 2. Input terminals and I/O terminals. Excludes OSC_1 terminals.
Note: 3. I/O terminals.
Note: 4. Output terminals.
Note: 5. Current flowing through pull-up MOSs and output drive MOSs is excluded.
Note: 6. Input/output current is excluded. When CMOS input is at an intermediate level, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

8

Note: 7. External clock operation.



Note: 8. Internal oscillator operation using oscillation resistor Rf.

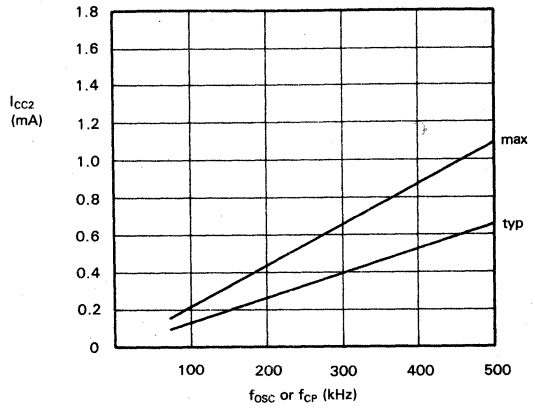


Rf: 56 kΩ ± 2% (V_{CC} = 3 V)
Rf: 68 kΩ ± 2% (V_{CC} = 5 V)
Reference values (T.B.D.)

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacitance, wiring length for these terminals should be minimized.

Note: 9. Applies to both V_{COM} and V_{SEG} voltage drops.
V_{COM}: From power suply terminal V_{CC}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})
V_{SEG}: From power suply terminal V_{CC}, V_2, V_3, V_6 to each segment signal terminal (SEG_1 to SEG_{40})

Note: 10. Relation between operation frequency and current consumption is shown in this diagram (V_{CC} = 5 V).



Note: 11. Applied to OSC_1 terminal.
Note: 12. The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

Timing Characteristics

Write operation

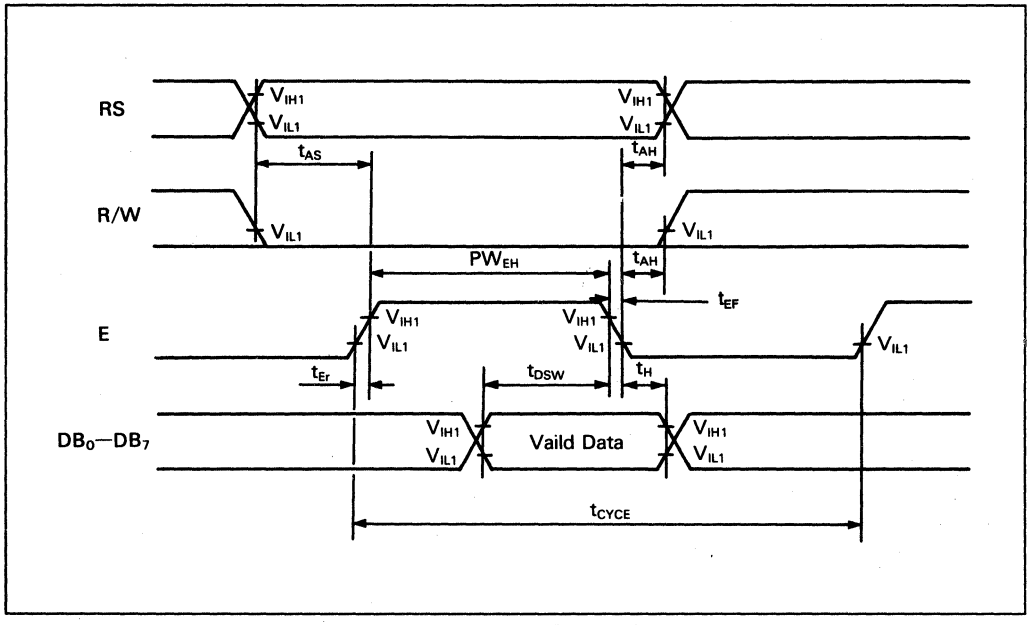


Figure 1 Write Operation

Read operation

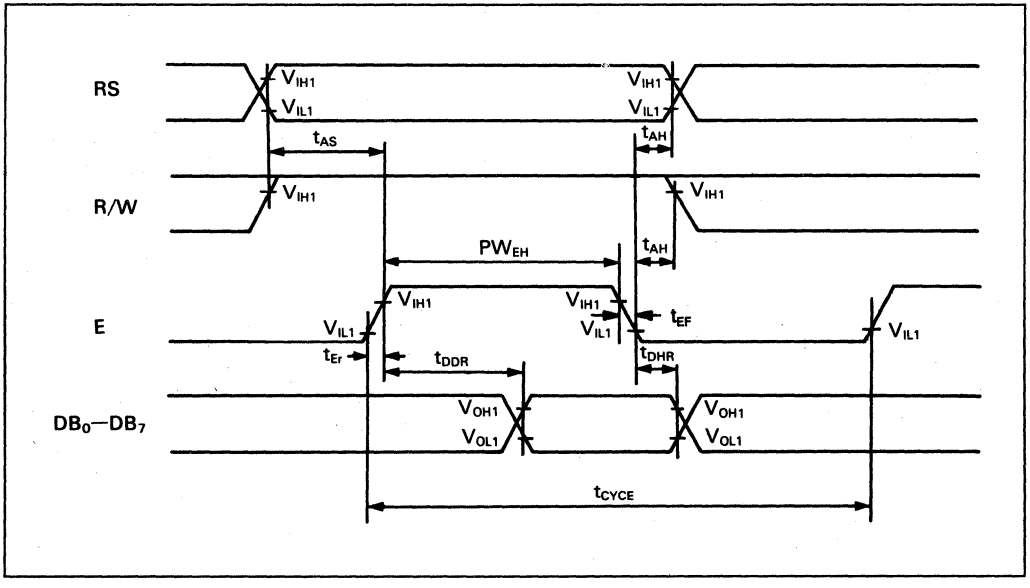


Figure 2 Read Operation

Interface signals with driver LSI HD44100H

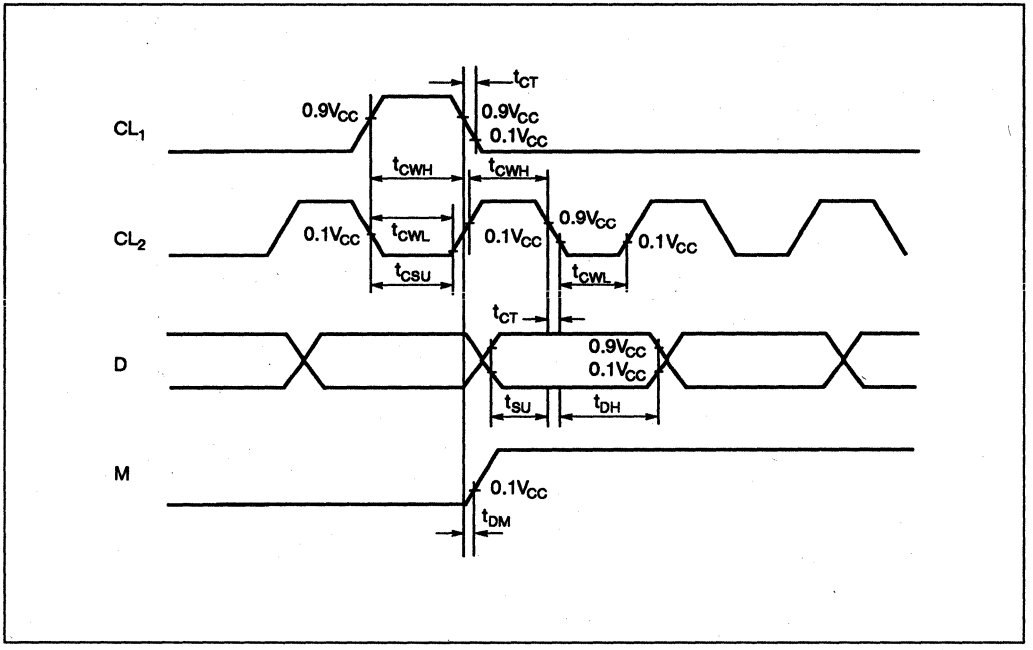


Figure 3 Extension Driver Interface Timing

Power on sequence

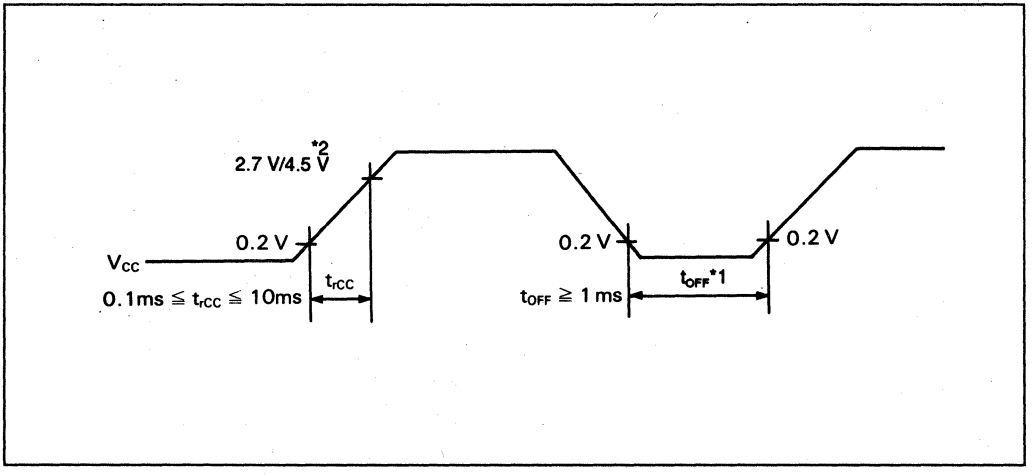
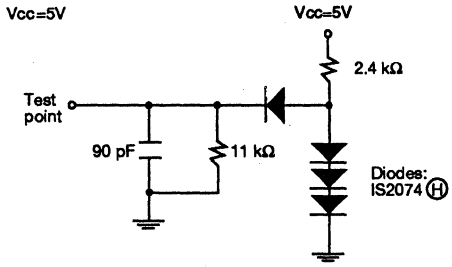


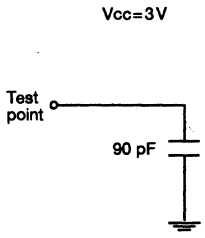
Figure 4 Power on Sequence

Notes: 1. t_{off} defines the time of power off for momentary power supply dip or when power supply is repeatedly turned on and off.
2. 2.7 when V_{CC} = 5 V, and 4.5 V when V_{CC} = 3 V.
3. Since the internal reset circuit will not operate normally if the above conditions are not satisfied, initialize the LSI by instruction. Refer to "Initializing by Instruction."

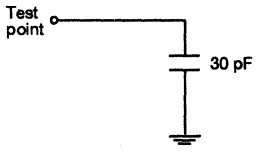
Note: Load Circuits

Data bus DB_0–DB_7





Segment extention signals



Terminal Function

Table 1 Functional Description of Terminals

Signal Name	No. of Lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W). 0: Write 1: Read
E	1	Input	MPU	Operation start signal for data read/write.
DB_4–DB_7	4	Input/Output	MPU	Higher order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II/E20. DB_7 can be used as a BUSY flag.
DB_0–DB_3	4	Input/Output	MPU	Lower order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II/E20. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Sends character pattern data corresponding to each common signal serially.
COM_1–COM_{16}	16	Output	Liquid crystal display	Common signals that are not used are changed to non-selection waveforms. That is, COM_9–COM_{10} are non-selection waveforms at 1/8 duty factor, and COM_{12}–COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1–SEG_{100}	100	Output	Liquid crystal display	Segment signal.
V_1–V_5	5		Power supply	Power supply for liquid crystal display drive.
V_{CC}, GND	2		Power supply	V_{CC}: +5 V, GND: 0 V.
TEST	1	Input	—	Test pin; to be grounded.
EXT	1	Input	—	Test pin; to be grounded.

Function Of Each Block

Register

The HD66702 had two 8-bit registers, an instruction register (IR), and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data is read from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Busy flag (BF)

When the busy flag is 1, the HD66702 is in the internal operation mode, and the next instruction will not be accepted. As table 2 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is 0.

Address counter (AC)

The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output to DB_0–DB_6 when RS = 0 and R/W = 1, as shown in table 2.

Table 2 Register Selection

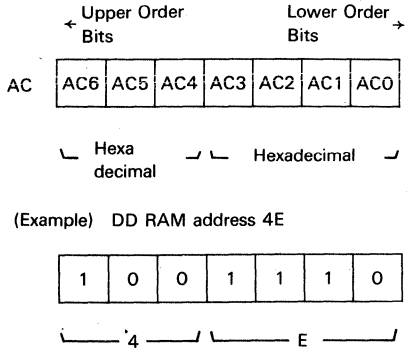
RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0–DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

Display data RAM (DD RAM)

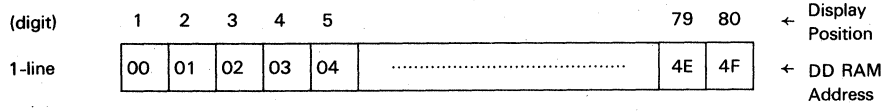
The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM.

Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

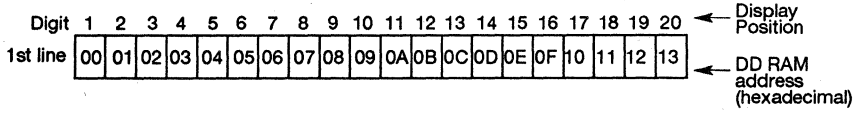
The DD RAM address (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.



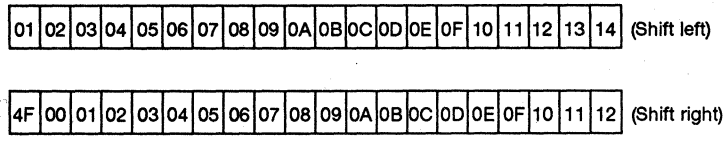
1-Line Display (N = 0)



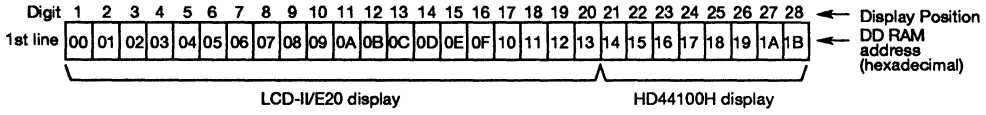
1. When there are fewer than 80 display characters, the display begins at the head position. For example, 20 characters using an HD66702 are displayed as:



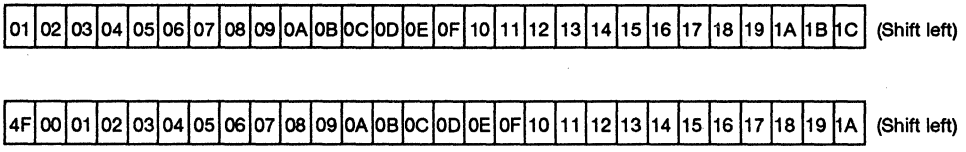
When the display shift operation is performed, the DD RAM address moves as:



2. 28-character display using an HD66702 and an HD44100H is as shown below:

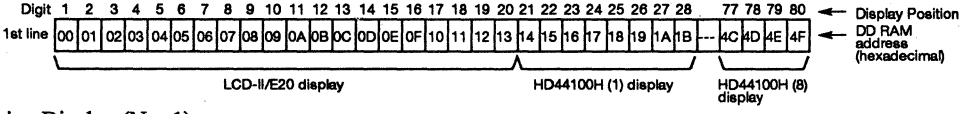


When the display shift operation is performed, the DD RAM address moves as:

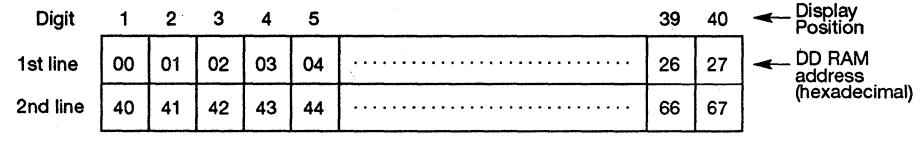


3. The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD66702 and two or more HD44100H's can be considered an extension of 2.

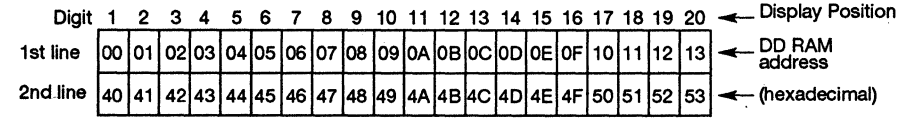
Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 8 HD44100H's.



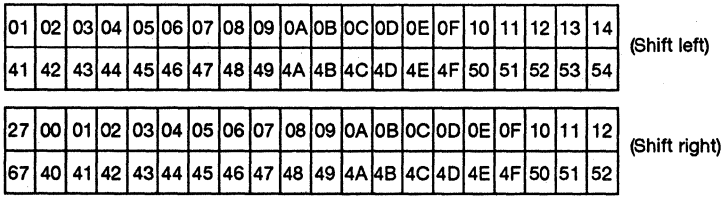
2-Line Display (N = 1)



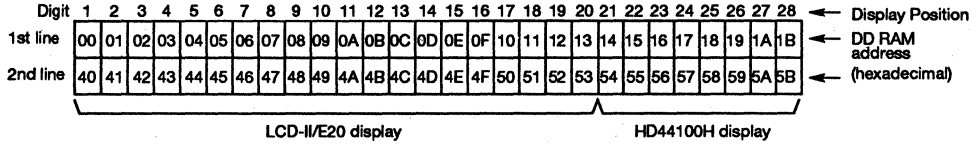
1. When the number of display characters is less than 40 × 2 lines, the 2 lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when an HD66702 is used, 20 characters × 2 lines are displayed as:



When display shift is performed, the DD RAM address moves as:



2. 28 characters × 2 lines are displayed when an HD66702 and an HD44100H are used.



When display shift is performed, the DD RAM address moves as follows:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C

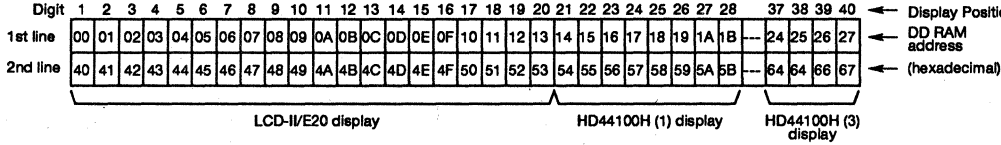
(Shift left)

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A

(Shift right)

3. The relation between display position and DD RAM address when the number of display digits is increased by using one HD66702 and two or more HD44100H's, can be considered an extension of 2.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting three HD44100H's externally.



Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns. Table 5 shows the relation between character codes and character patterns in the Hitachi standard HD66702. User defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots, 4 characters can be written.

Write the character codes in the left column of table 5 to display character patterns stored in CG RAM.

Table 6 shows the relation between CG RAM addresses and data and display patterns.

As table 6 shows, an area that is not used for display can be used as a general data RAM.

Modifying Character Patterns

1. Character Pattern Development Procedure

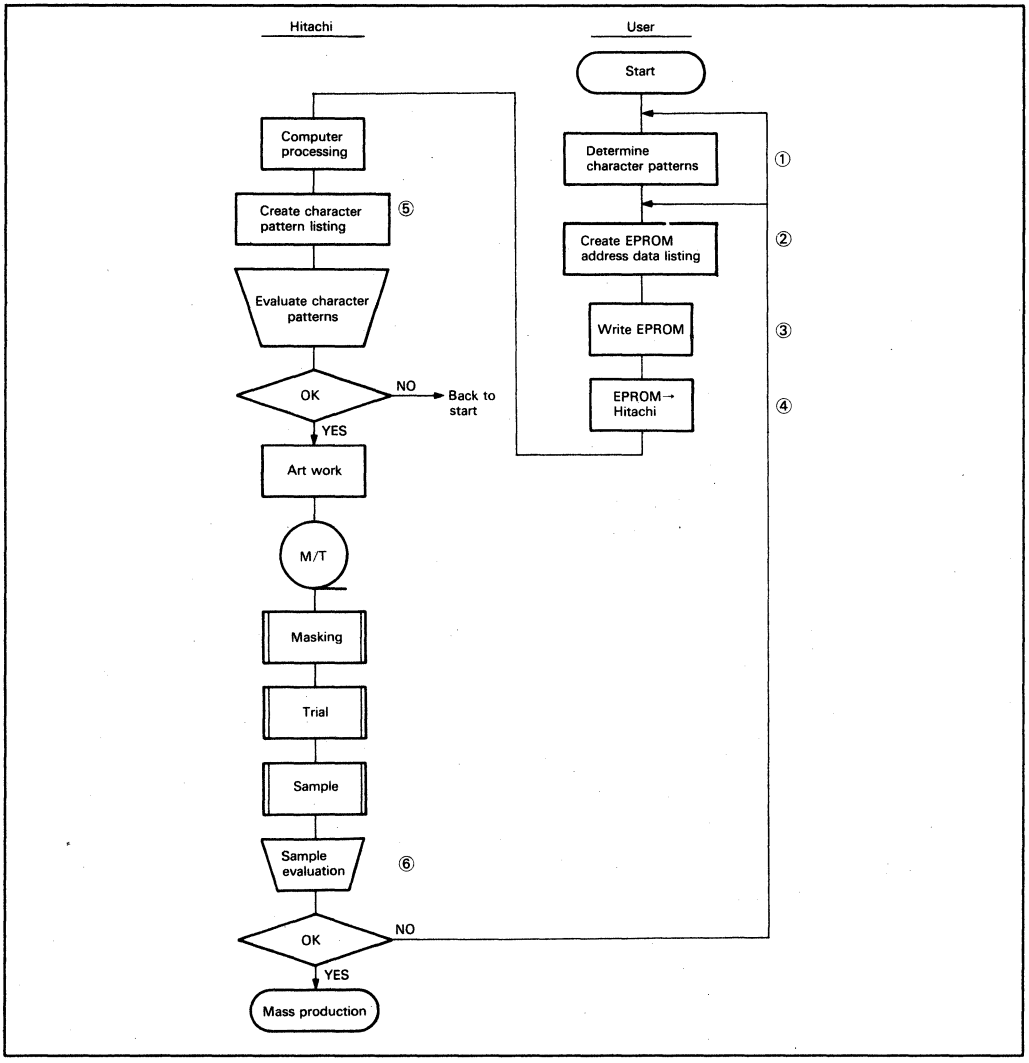


Figure 5 Character Pattern Development Procedure

The numbers in figure 5 correspond to the following operations:

① Determine the correspondence between character codes and character patterns.

② Create a listing indicating the correspondence between EPROM addresses and data.

③ Program character patterns in the EPROM.

④ Send the EPROM to Hitachi.

⑤ Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.

⑥ If there is no problem in the character pattern listing, Hitachi creates a trial LSI and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, Hitachi starts mass production of the LSI.

2. Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II/E20 character generator ROM can generate 160 5 × 70-dot character patterns and 32 5 × 10-dot character patterns for a total of 192 different character patterns.

a. 5 × 7-dot Character Pattern

For a 5 × 7-dot character pattern, EPROM address data and character pattern correspond with each other as shown below. Table 3 is an example of the correspondence between EPROM address data and character pattern (5 × 7 dots).

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 7 dots)

EPROM address											Data				
														(LSB)	
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0

Character code — Line position

Fill line 8 (cursor position) with 0

(1) EPROM address A_{10} to A_3 correspond to a character code.

(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.

(3) EPROM data O_4 to O_0 correspond to character pattern data.

(4) A lit display position (black) corresponds to 1.

(5) Fill line 8 (cursor position) of character pattern with 0.

(6) EPROM data O_5 to O_7 are not used.

b. 5 × 10-dot Character Pattern

For a 5 × 10-dot character pattern, EPROM address data and character pattern correspond with each other as shown in table 4.

(1) EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern line 9 and later lines to 0.
(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.
(3) EPROM data O_4 to O_0 correspond to character pattern data.
(4) A lit display position (black) corresponds to 1.
(5) Fill line 11 (cursor position) of character pattern with 0.
(6) EPROM data O_5 to O_7 are not used.

c. Handling Unused Character Patterns

(1) EPROM data outside the character pattern area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(2) EPROM data in CG RAM area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(3) EPROM data used when the user does not use any HD66702 character pattern
Handled in one of the two ways explained below. Select one of the two ways according to the user application.

(a) When unused character patterns are not programed
If an unused character code is written in the LCD-II/E20 DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1s when the EPROM is erased.)

(b) Program 0 for unused character patterns
Nothing is displayed even if unused character codes are written in LCD-II/E20 DD RAM. (This is equivalent to space.)

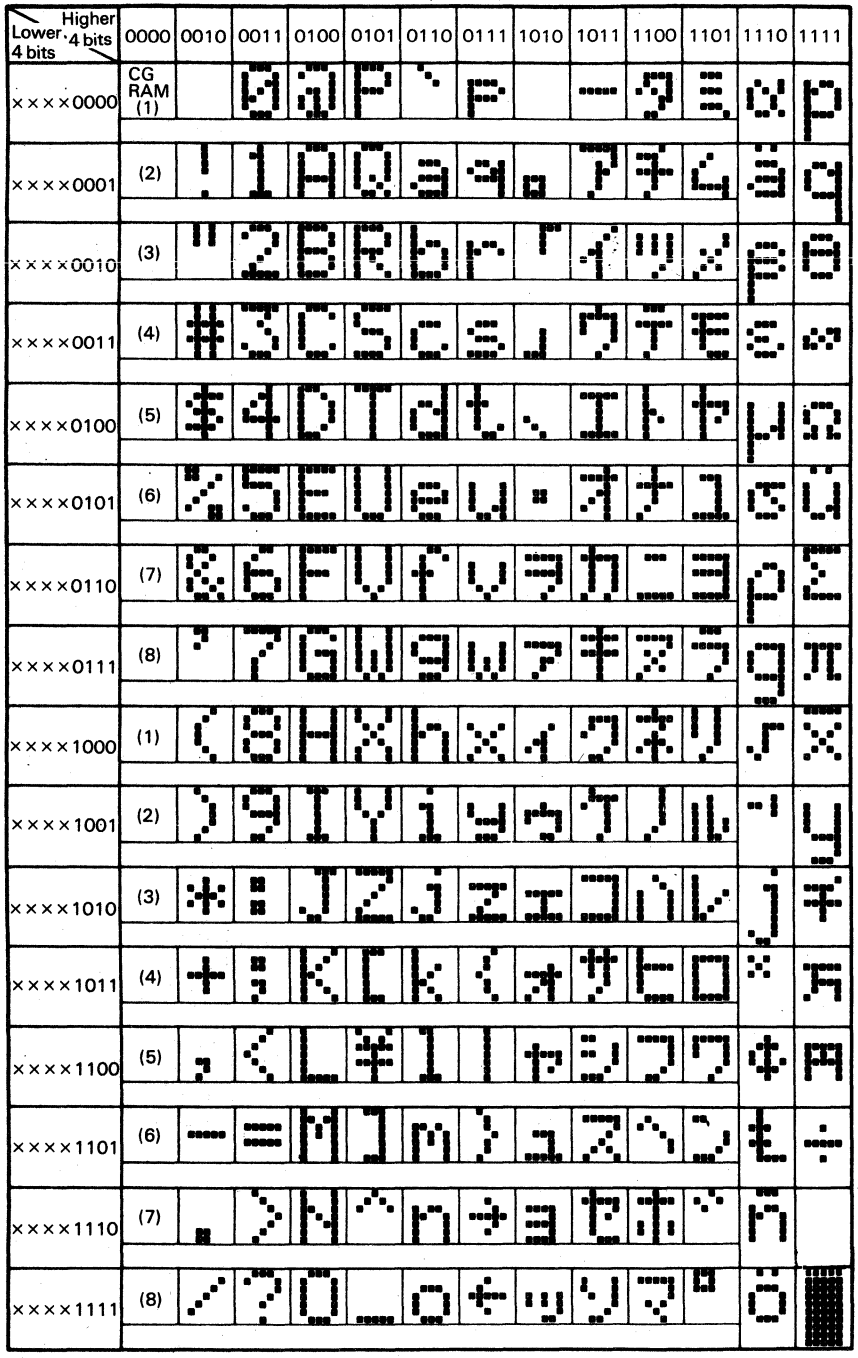
Table 4 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM address											Data				
															(LSB)
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
								0	0	0	0	0	0	0	0
								0	0	1	0	0	0	0	0
								0	1	0	0	1	1	0	1
1	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1
								1	0	0	1	0	0	0	1
								1	0	1	1	0	0	0	1
								1	1	0	0	1	1	1	1
								1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0

Character code — Line position

Fill line 11 (cursor position) with 0

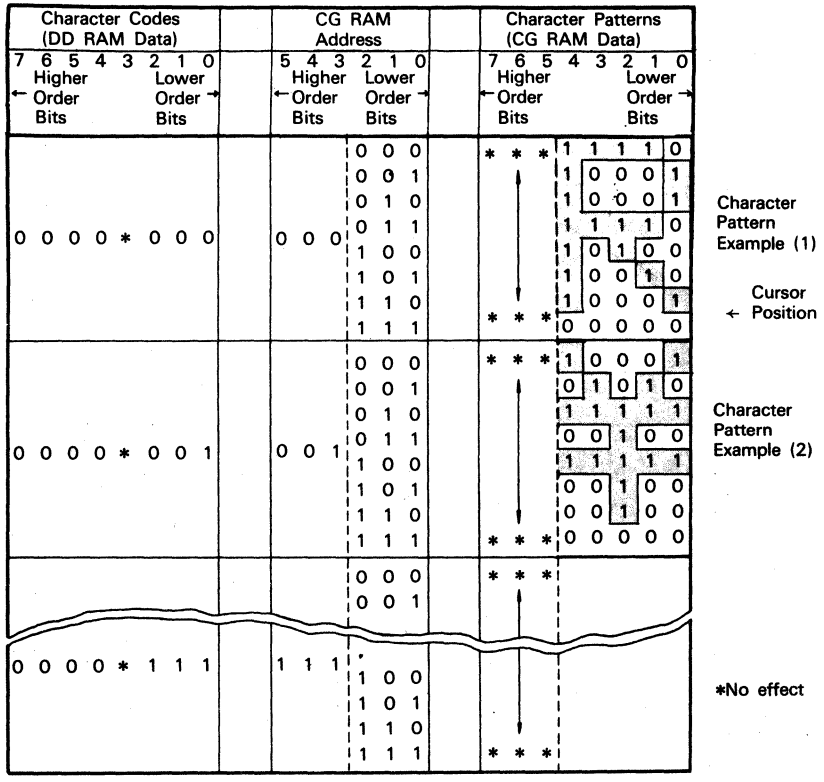
Table 5 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD66702)



Note: The user can specify any pattern for character-generator RAM.

Table 6 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

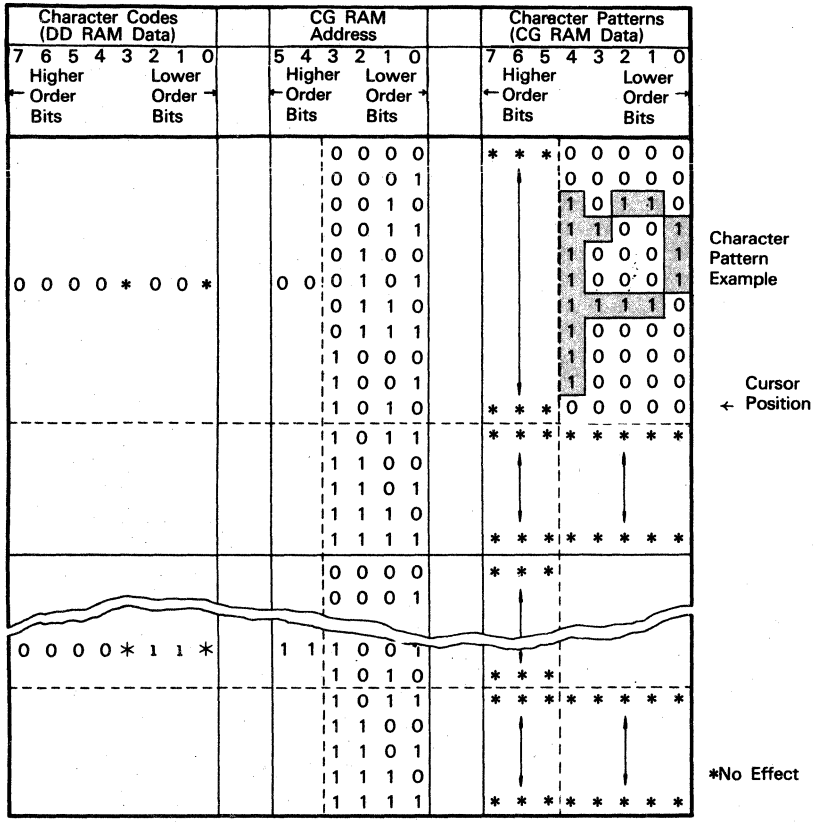
For 5 x 7 dot character patterns



Notes:
1. Character code bits 0–2 correspond to CG RAM address bits 3–5 (3 bits: 8 types).
2. CG RAM address bits 0–2 designate character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0–4, as shown in the figure (bit 4 being at the left end).
   Since CG RAM data bits 5–7 are not used for display, they can be used for the general data RAM.
4. As shown in tables 3 and 4, CG RAM character patterns are selected when character code bits 4–7 are all 0. However, since character code bit 3 has no effect, the "R" display in the character pattern example is selected by character code "00" (hexadecimal) or "08" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

Table 6 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data) (Continued)

For 5 × 10 dot character patterns



Notes: 1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).
2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.
Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor presence. Since the 12th-16th lines are not used for display, they can be used for general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 have no effect, "P" display in the character pattern example is selected by character codes "00", "01", "08" and "09" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM, and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 100 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 100-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs. The serial data can be sent to HD44100H's, externally connected in cascade, used for display digit number extension.

Serial data send always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66702 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

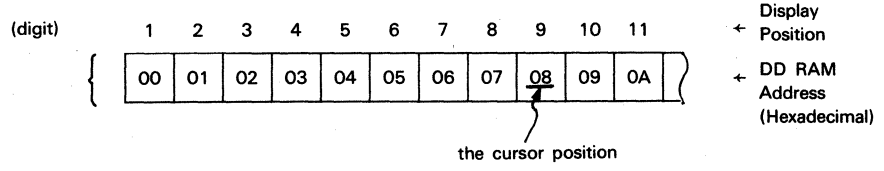
Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or blink. The cursor or the blink appear in the digit at the display data RAM (DD RAM) address set in the address counter (AC).

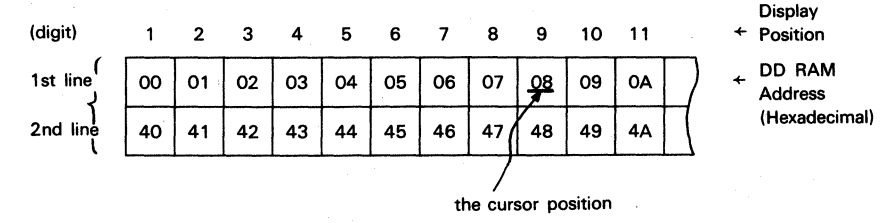
When the address counter is $(08)_{16}$, the cursor position is:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



In a 2-line display



Note: The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is a CG RAM address.

Interfacing To MPU

In the HD66702, data can be sent in either two 4-bit operations or one 8-bit operations so it can interface to both 4- and 8-bit MPUs.

1. When interface data is 4-bits long, data is transferred using only 4 buslines: DB_4–DB_7. DB_0–DB_3 are not used. Data transfer between the HD66702 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4–DB_7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB_0–DB_3 when interface data is 8 bits long) is transferred.

   Check the busy flag after 4-bit data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data.

2. When interface data is 8 bits long, data is transferred using the 8 data buslines DB_0–DB_7.

Reset Function

Initializing by Internal Reset Circuit

The HD66702 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed during initialization. The busy flag (BF) is kept in busy state until initialization ends (BF = 1). The busy state is 10 ms after V_{cc} rises to 4.5 V.

1. Display clear

2. Function set:
   DL = 1: 8-bit-long interface data
   N = 0: 1-line display
   F = 0: 5 × 7 dot character font

3. Display on/off control:
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blink off

4. Entry mode set:
   I/D = 1: +1 (increment)
   S = 0: No shift

Note: When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

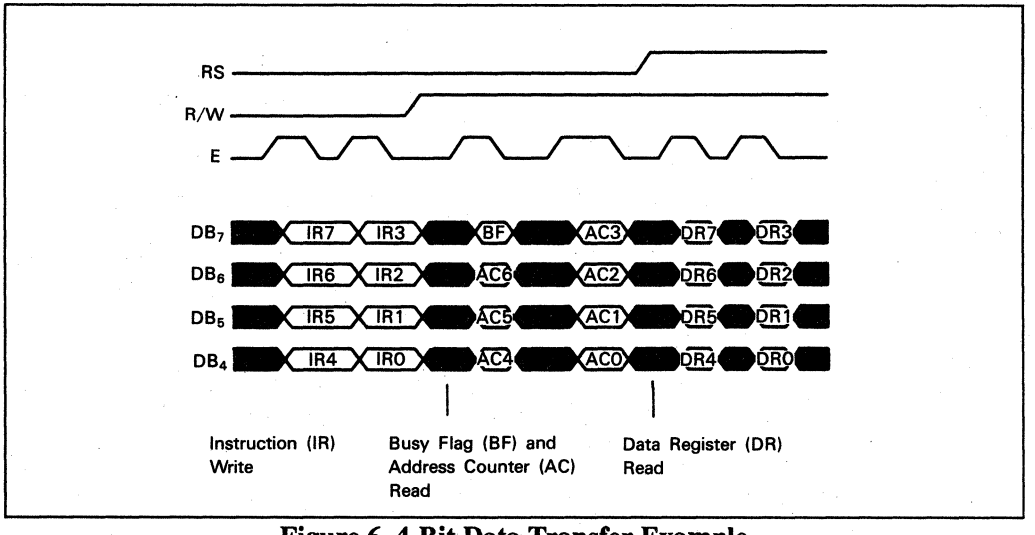


Figure 6 4-Bit Data Transfer Example

Instructions

Outline

Only two HD66702 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD66702 internal operation to various types of MPUs that operate in different speeds or to allow interface to peripheral control ICs. HD66702 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals (OB_0–DB_7), and are here called instructions. Table 7 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

1. Designate HD66702 functions such as display format, data length, etc.
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by–1) of HD66702 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 12.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed.

Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is 1 before sending an instruction from the MPU.

Note: Make sure the HD66702 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD66702. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See table 7 for a list of each instruction execution time.

Table 7 Instructions

Instruction	Code RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{osc} is 320 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.28 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.28 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	31 µs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets On/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	31 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	31 µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	31 µs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	31 µs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	31 µs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	31 µs t_{ADD}=4.7 µs (Note)
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	31 µs t_{ADD}=4.7 µs (Note)
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 x 10 dots, F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address: Corresponds to cursor address AC: Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes Example: When f_{CD} or F_{OSC} is 270 kHz: $31\ \mu s \times \frac{320}{270} = 37\ \mu s$

*No effect

Note: After execution of a CG RAM/DD RAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off. In figure 7, tADD is the time elapsed after the busy flag turns off until the address counter is updated.

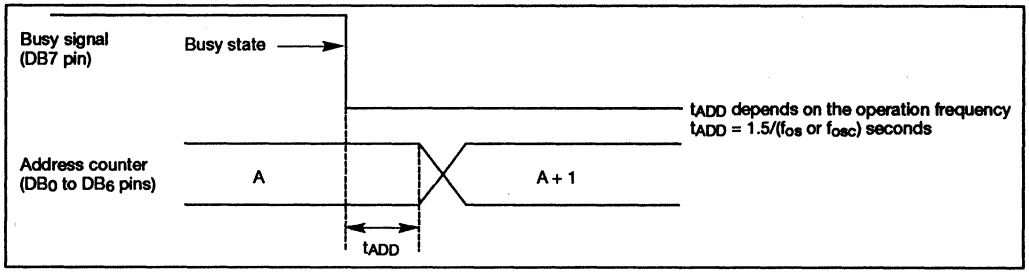


Figure 7 Address Counter Update

Description of Details

1. Clear Display

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	0	0	1

Writes space code 20 (hexadecimal) (character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (increment mode) in entry mode. S of entry mode doesn't change.

2. Return Home

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	0	1	*

* Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change.

The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

3. Entry Mode Set

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.

The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0.

Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM causes a shift when S = 0.

4. Display On/Off Control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: The display is on when D = 1 and off when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed instantly by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5 × 10 dot character font is selected (Figure 8).

B: The character indicated by the cursor blinks when B = 1 (Figure 8). The blink is displayed by switching between all blank dots and display characters at 320 ms intervals when f_{cp} or f_{osc} = 320 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of f_{cp} or f_{osc}.

$320 \times \frac{320}{270} = 379.2$ ms when $f_{cp} = 270$ kHz.)

5. Cursor or Display Shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Don't care

Shifts cursor position or display to the right or left without writing or reading display data (Table 8). This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time.

When the displayed data is shifted repeatedly each line only moves hirizontally. The 2nd line display does not shift into the 1st line position.

Address counter (AC) contents do not change if the only action performed is display shift.

6. Function Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* Don't care

DL: Sets interface data length. Data is sent or received in 8 bit lengths (DB_7–DB_0) when DL = 1 and in 4 bit lengths (DB_7–DB_4) when DL = 0.

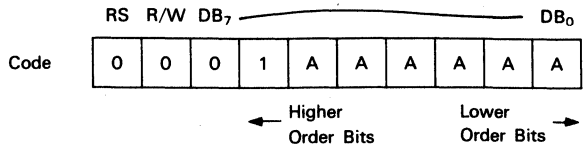
When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

Note: Perform the function at the head of the program before executing any instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

7. Set CG RAM Address



Sets the CG RAM address binary AAAAAA into the address counter.

Data is then written or read from the MPU for the CG RAM.

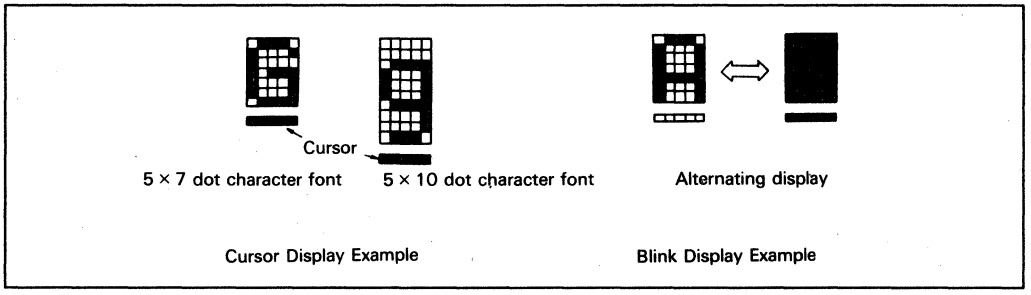
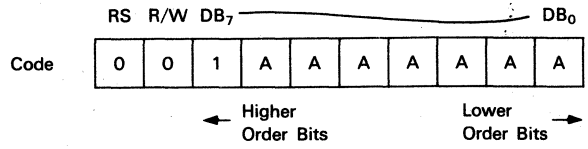


Figure 8 Cursor and Blink

8. Set DD RAM Address

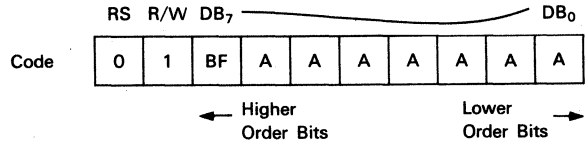


Sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA can be 00-4F (hexadecimal). When N = 1 (2-line display), AAAAAAA can be 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

9. Read Busy Flag and Address



Reads the busy flag (BF) that indicates that the system is now internally operating on a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not accepted until BF is set to 0. Check the BF status before the next wire operation. At the same, the value of the address counter expressed in binary as AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in items 7 and 8.

Table 8 Shift Function

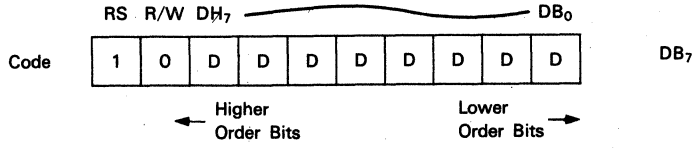
S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 9 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 x 7 dots	1/8	
0	1	1	5 x 10 dots	1/11	
1	*	2	5 x 7 dots	1/16	Cannot display 2 lines with 5 x 10 dot character font

*Don't care

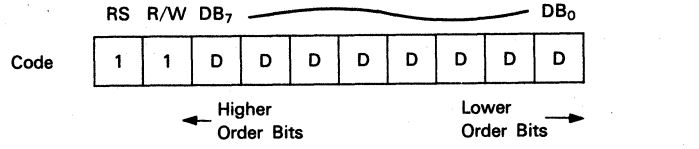
10. Write Data to CG or DD RAM



Writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

11. Read Data from CG or DD RAM



Reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering either the CG RAM or DD RAM address set instruction, If you don't, the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data readout are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out execute the "read" instruction from the second time the "read" instruction is sent.

Connecting directly to the 8-bit MPU bus line

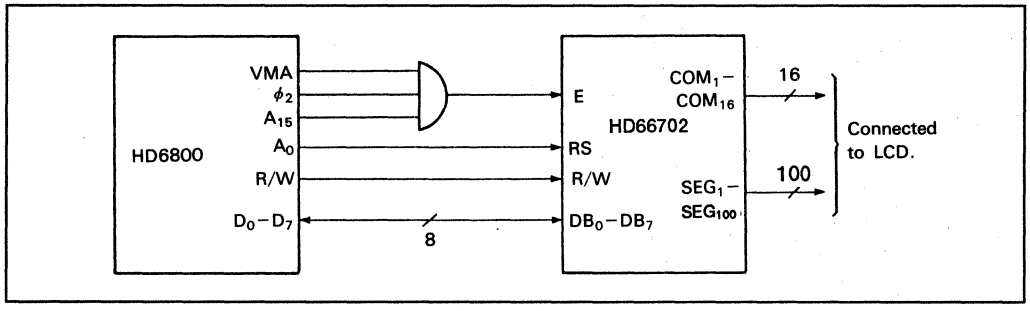


Figure 11 8-Bit MPU Interface

Example of interfacing to the HD6805

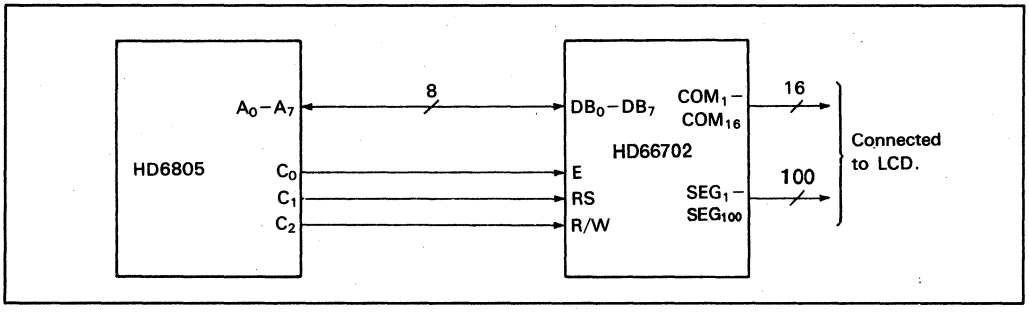


Figure 12 HD6805 Interface

8

Example of interfacing to the HD6301

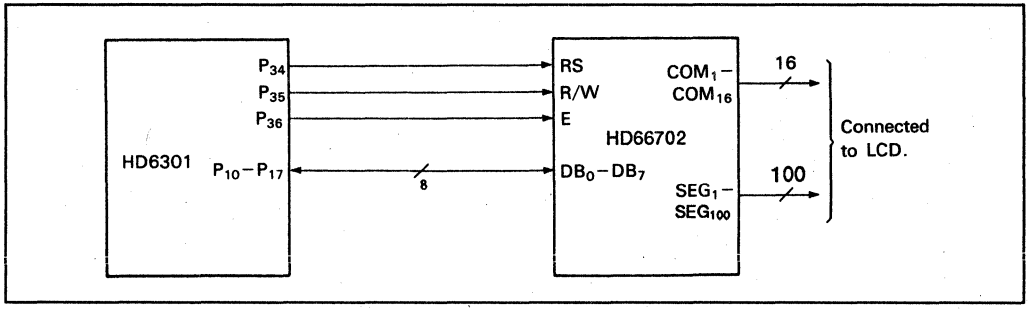


Figure 13 HD6301 Interface

How To Use The HD66702

Interface to MPU

1. Interface to 8-Bit MPU

When connecting to 8-bit MPU through PIA

Figure 15 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively.

Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

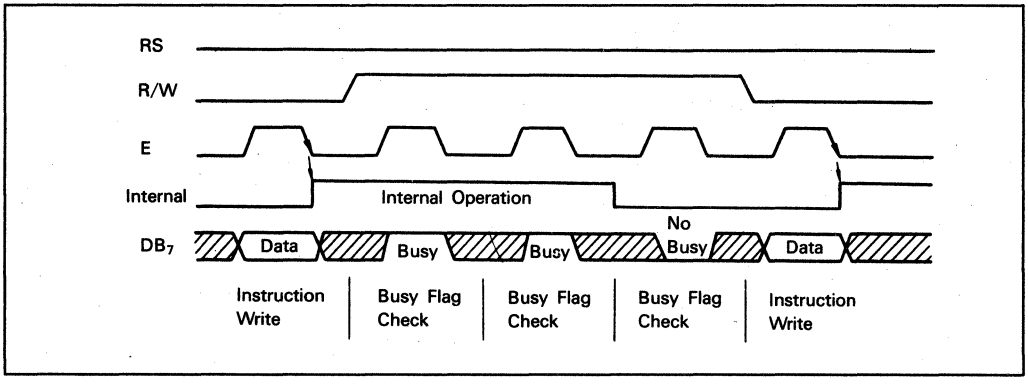


Figure 14 Example of Busy Flag Check Timing Sequence

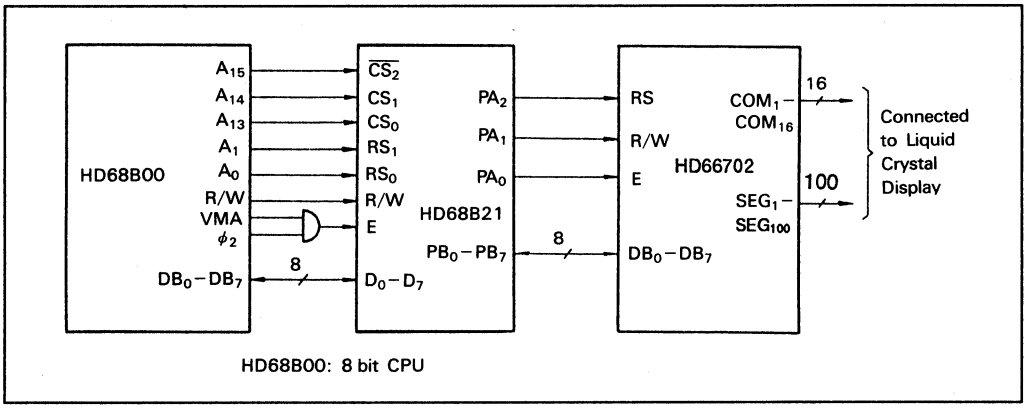


Figure 15 Example of Interface to HD68B00 Using PIA (HD68B21)

2. Interface to 4-bit MPU

The HD66702 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if there are insufficient bits, the transfer is made in two operations of 4 bit each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex (See figure 16).

Figure 17 shows an example of interface to the HMCS43C.

Note: that 2 cycles are needed for the busy flag check as well as the data trnsfer. 4-bit operation is selected by program.

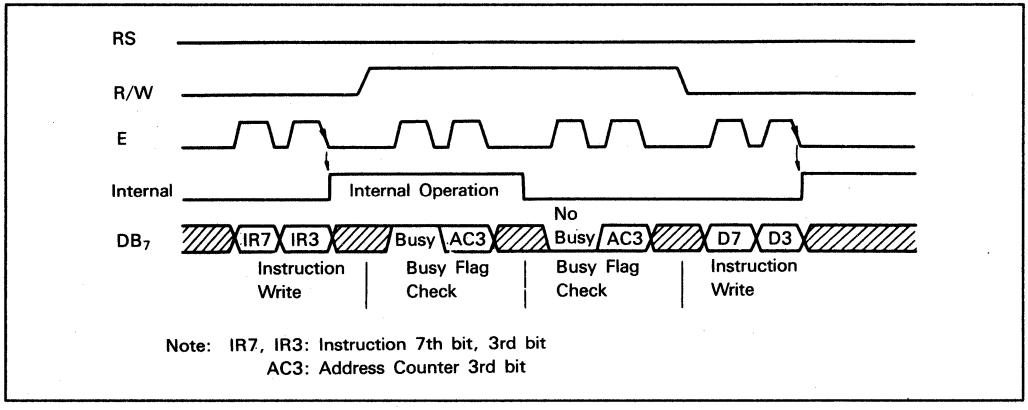


Figure 16 An Example of 4-Bit Data Transfer Timing Sequence

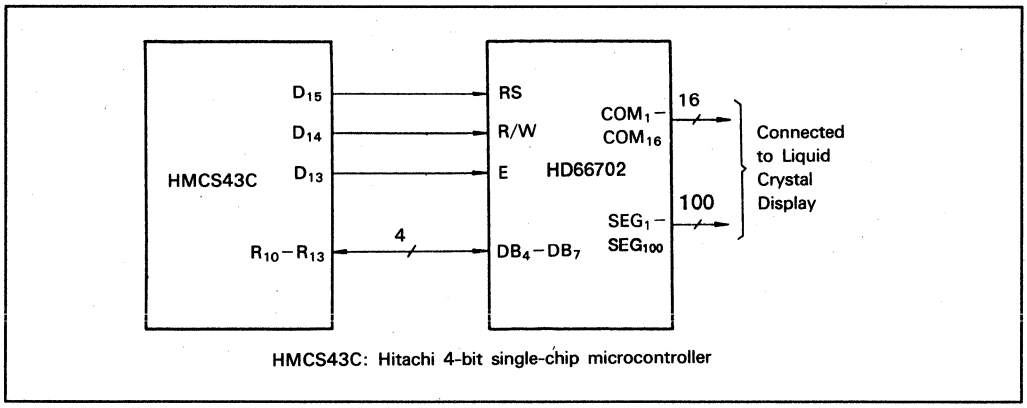


Figure 17 Example of Interface to the HMCS43C

Interface to Liquid Crystal Display

1. Character Font and Number of Lines

   The HD66702 can perform 2 types of display, 5 × 7 dots and 5 × 10 dots character font, with a cursor on each.

   Up to 2 lines are displayed with 5 × 7 dots and 1 line with 5 × 10 dots. Therefore, three types of common signals are available (Table 10).

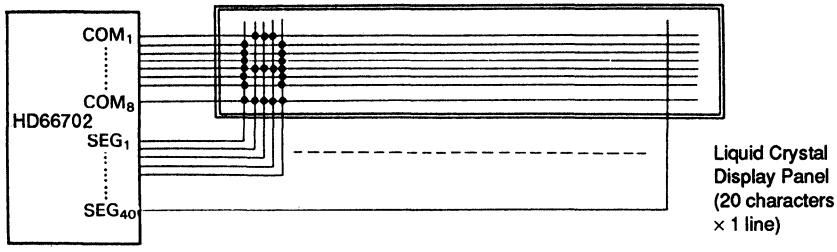
   Number of line and font types can be selected by program. (See Table 7, Instructions).

2. Connection to HD67702 and Liquid Crystal Display

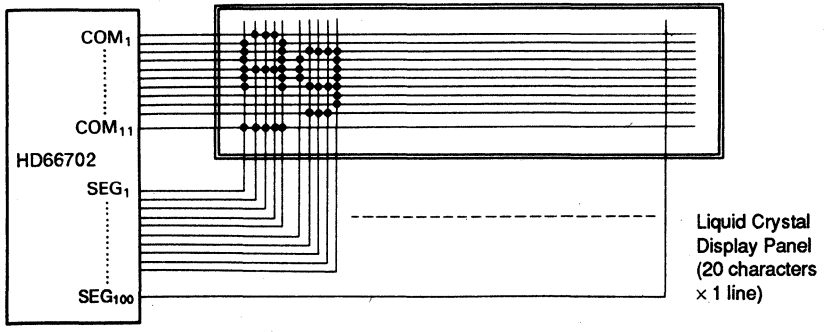
   Figure 18 shows connection examples.

Table 10 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 x 7 dots + Cursor	8	1/8
1	5 x 10 dots + Cursor	11	1/11
2	5 x 7 dots + Cursor	16	1/16



(a) Example of a 5×7 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

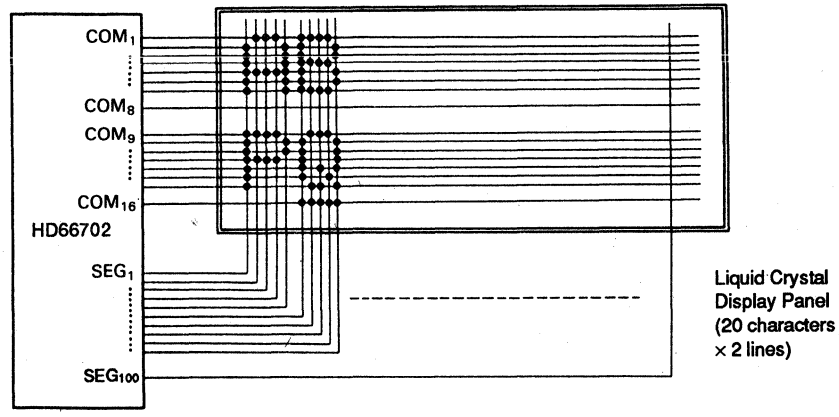


(b) Example of 5 × 10 dot, 20 character × 1 line Display (1/4 Bias, 1/8 Duty Cycle)

Figure 18 Liquid Crystal Display and Connections to HD66702

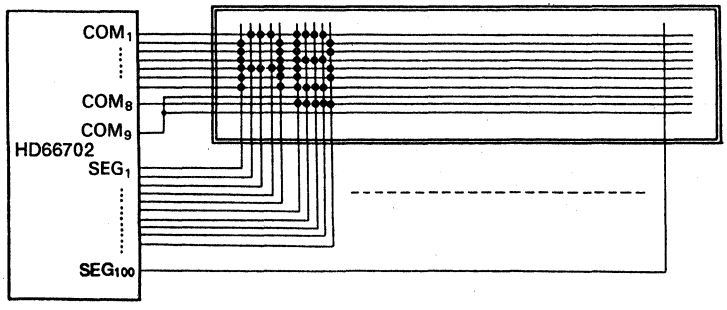
Since 5 SEG signal lines can display one digit, one HD66702 can display up to 20 digits for 1-line display and 40 digits for 2-line display.

In Figure 19 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to crosstalk in the floating state by connecting the extra scanning lines to these common signal terminals (Figure 20).



(c) Example of 5 × 7 dot, 20 character × 2 lines Display (1/5 Bias, 1/16 Duty Cycle)

Figure 19 Liquid Crystal Display and Connections to HD66702 (Cont'd.)

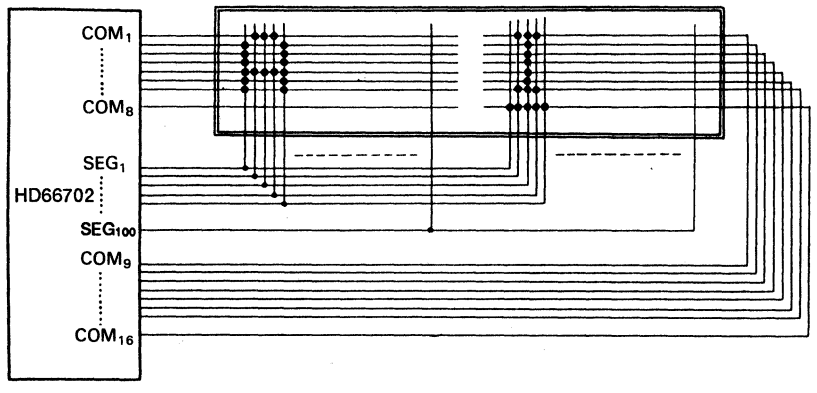


5 × 7 dot, 20 character × 1 line Display (1/4 Bias, 1/8 Duty Cycle)

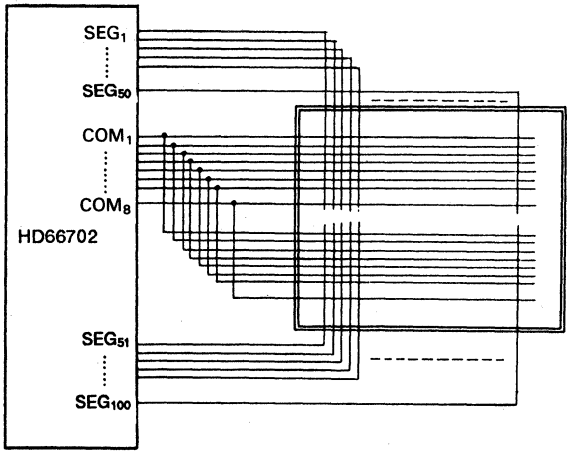
Figure 20 Using COM9 to Avoid Crosstalk on Unneeded Scanning Line

3. Connection of Changed Matrix Layout

In the preceding examples, the number of lines matched the number of scanning lines. The display types Figure 21 are made possible by changing the matrix layout in the liquid crystal display panel. In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 10 characters × 2 lines and 40 characters × 1 line are the same as shown in Figure 19.



5 × 7 dot, 40 character × 1 line Display
(1/5 Bias, 1/16 Duty Cycle)



5×7 dot, 4 character×2 line Display
(1/4 Bias, 1/8 Duty Cycle)

Figure 21 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD66702 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 11 shows the relation.

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in Figure 22.

Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor		1/8, 1/11	1/16
Power Supply	**Bias**	**1/4**	**1/5**
V_1		$V_{cc} - 1/4\ V_{LCD}$	$V_{cc} - 1/5\ V_{LCD}$
V_2		$V_{cc} - 1/2\ V_{LCD}$	$V_{cc} - 2/5\ V_{LCD}$
V_3		$V_{cc} - 1/2\ V_{LCD}$	$V_{cc} - 3/5\ V_{LCD}$
V_4		$V_{cc} - 3/4\ V_{LCD}$	$V_{cc} - 4/5\ V_{LCD}$
V_5		$V_{cc} - V_{LCD}$	$V_{cc} - V_{LCD}$

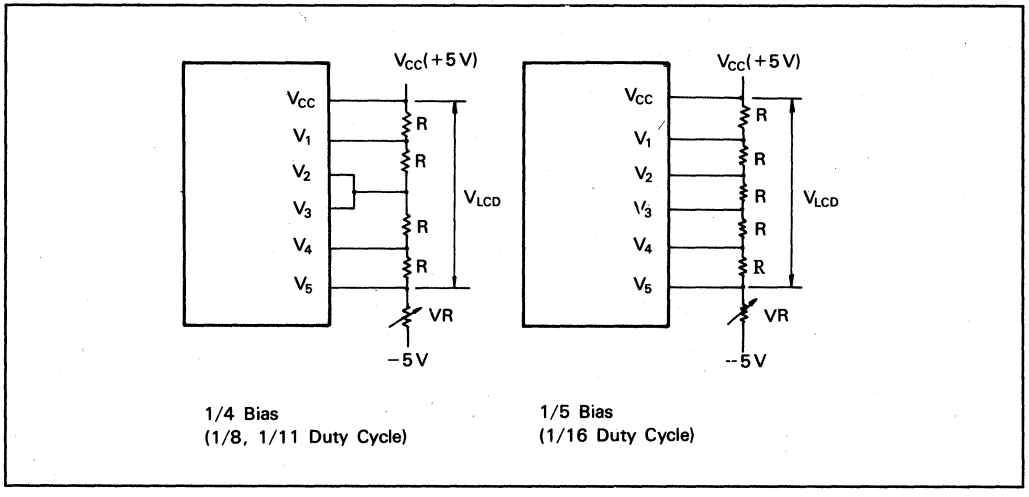
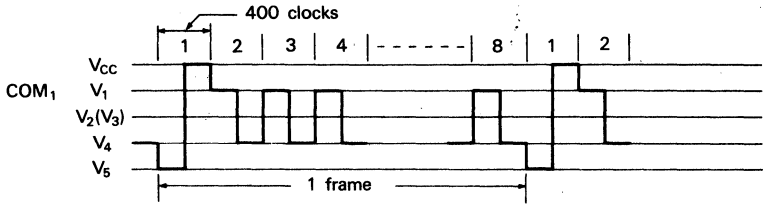


Figure 22 Drive Voltage Supply Example

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The examples in Figure 23 of liquid crystal display frame frequency apply only when oscillation frequency is 320 kHz (1 clock pulse = 3.125 μs).

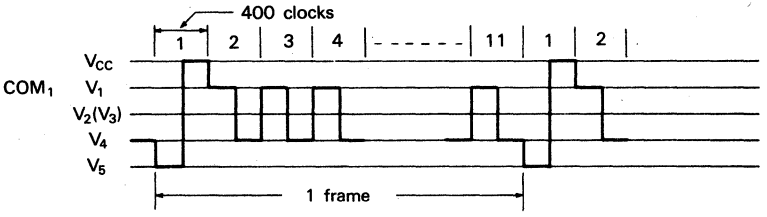
1. 1/8 Duty Cycle



1 frame = 3.125 (μs) × 400 × 8 = 10000 (μs) = 10 (ms)

$$\text{Frame frequency} = \frac{1}{10\ (\text{ms})} = 100\ (\text{Hz})$$

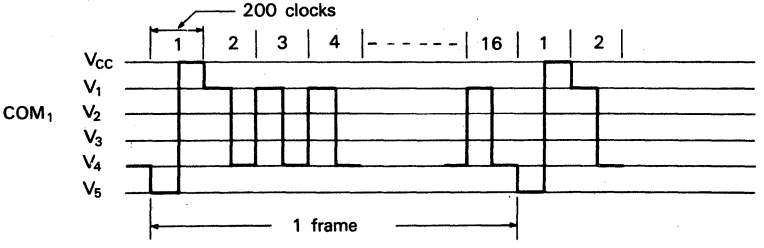
2. 1/11 Duty Cycle



1 frame = 3.125 (μs) × 400 × 11 = 13750 (μs) = 13.75 (ms)

$$\text{Frame frequency} = \frac{1}{13.75\ (\text{ms})} = 72.7\ (\text{Hz})$$

3. 1/16 Duty Cycle



1 frame = 3.125 (μs) × 200 × 16 = 10000 (μs) = 10 (ms)

$$\text{Frame frequency} = \frac{1}{10\ (\text{ms})} = 100\ (\text{Hz})$$

Figure 23 Frame Frequency

Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting an HD44100H liquid crystal display driver LSI to the HD66702. When connected to the HD66702, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD66702 directly since it supplies CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figure 24 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated. The EXT pin must be fixed low if the HD44100H is connected to the HD66702.

Up to 8 HD44100H units can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 3 units for the 2-line display (duty factor 1/16). RAM size limits the HD66702 to a maximum of 80 character display digits. The connection method in figure 22 remains unchanged for both 1-line and 2-line display or 5 × 7 and 5 × 10 dot character fonts.

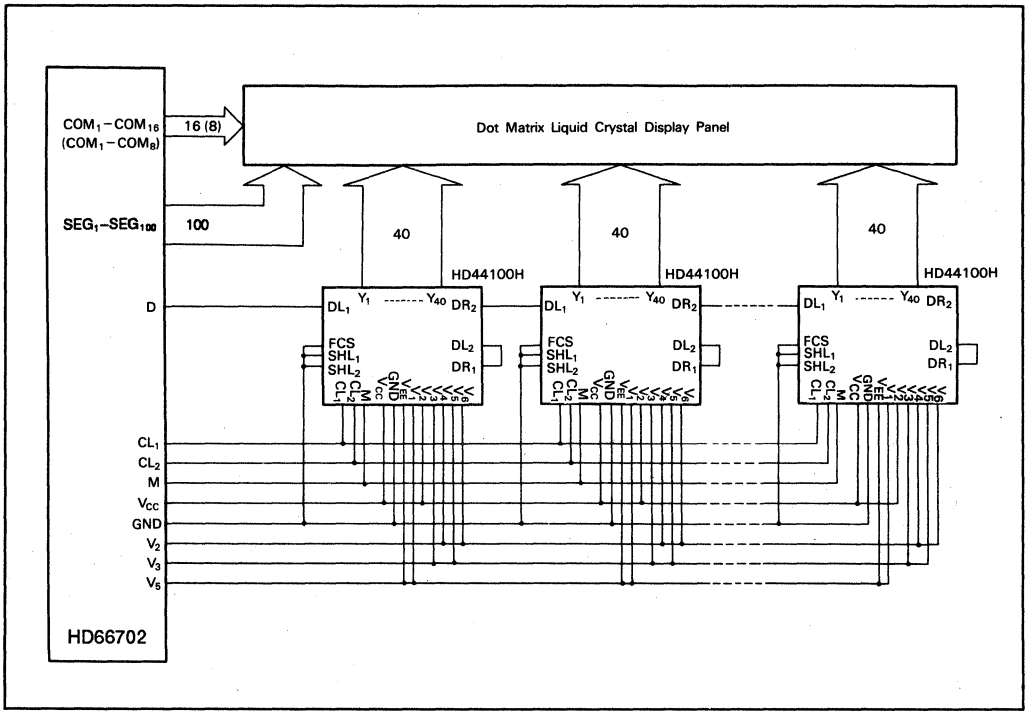


Figure 24 Example of Connecting HD44100H to HD66702

Instruction and Display Correspondence

1. 8-bit operation, 20-digit × 1-line display (using internal reset)

   Table 12 shows an example of 8-bit × 1-line display in 8-bit operation. The HD66702 functions must be set by function set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like a lighting board when combined with display shift operation.

   Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

2. 4-bit operation, 20-digit × 1-line display (using internal reset)

   The program must set functions prior to 4-bit operation. Table 13 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to DB_0–DB_3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as function (see table 13). Thus, DB_4–DB_7 of the function set is written twice.

3. 8-bit operation, 20-digit × 2-line display

   For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 20 characters in the first line, the DD RAM address must again be set after the 20th character is completed. (See table 14). Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and the second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the LCD-II/E20 must be initialized by instruction. (As the internal reset does not function correctly in the 3-V LCD-II/E20, it must always be initialized by instruction.) See "Initializing by Instruction."

Table 12 8-Bit Operation, 20-Digit 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/WDB 7 • • • DB0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display and one of the three character fonts. (Number of display lines and character font cannot be changed after this.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is on space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI	Writes space.
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO	Shifts only the cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (address 0).

Table 13 4-Bit Operation, 20-Digit 1-Line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 · · · DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets to 4-bit operation and selects 1-line display and one of the three character fonts. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character font cannot be changed after this.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.

After this, control is the same as 8-bit operation.

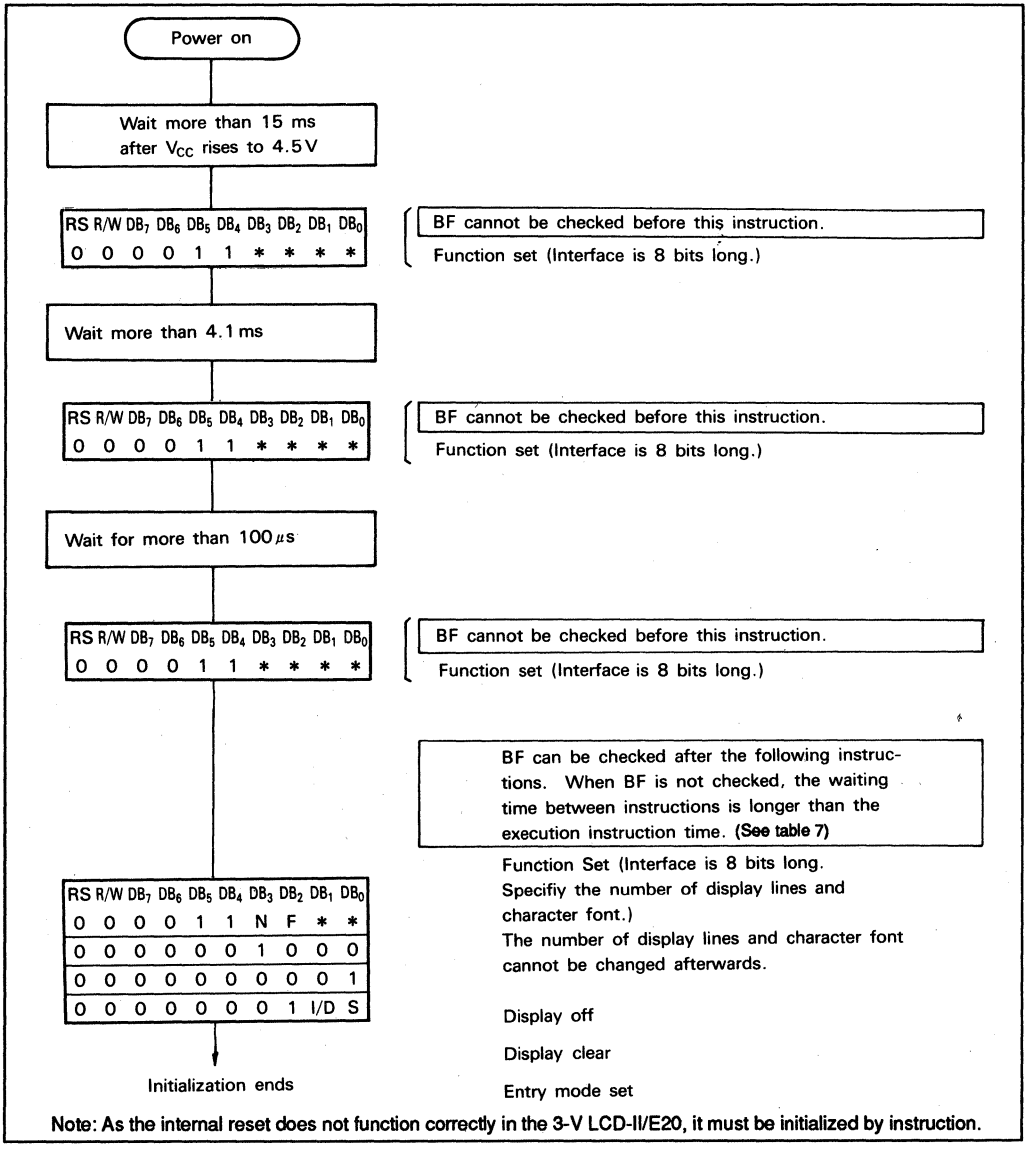
Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD66702 is intialized by the internal reset circuit)		Initalized. No display appears.
2	Function Set RS R/WDB$_7$ ~~~ DB$_0$ 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift operate at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required. Use the procedure in Figures 25 and 26 for initialization.

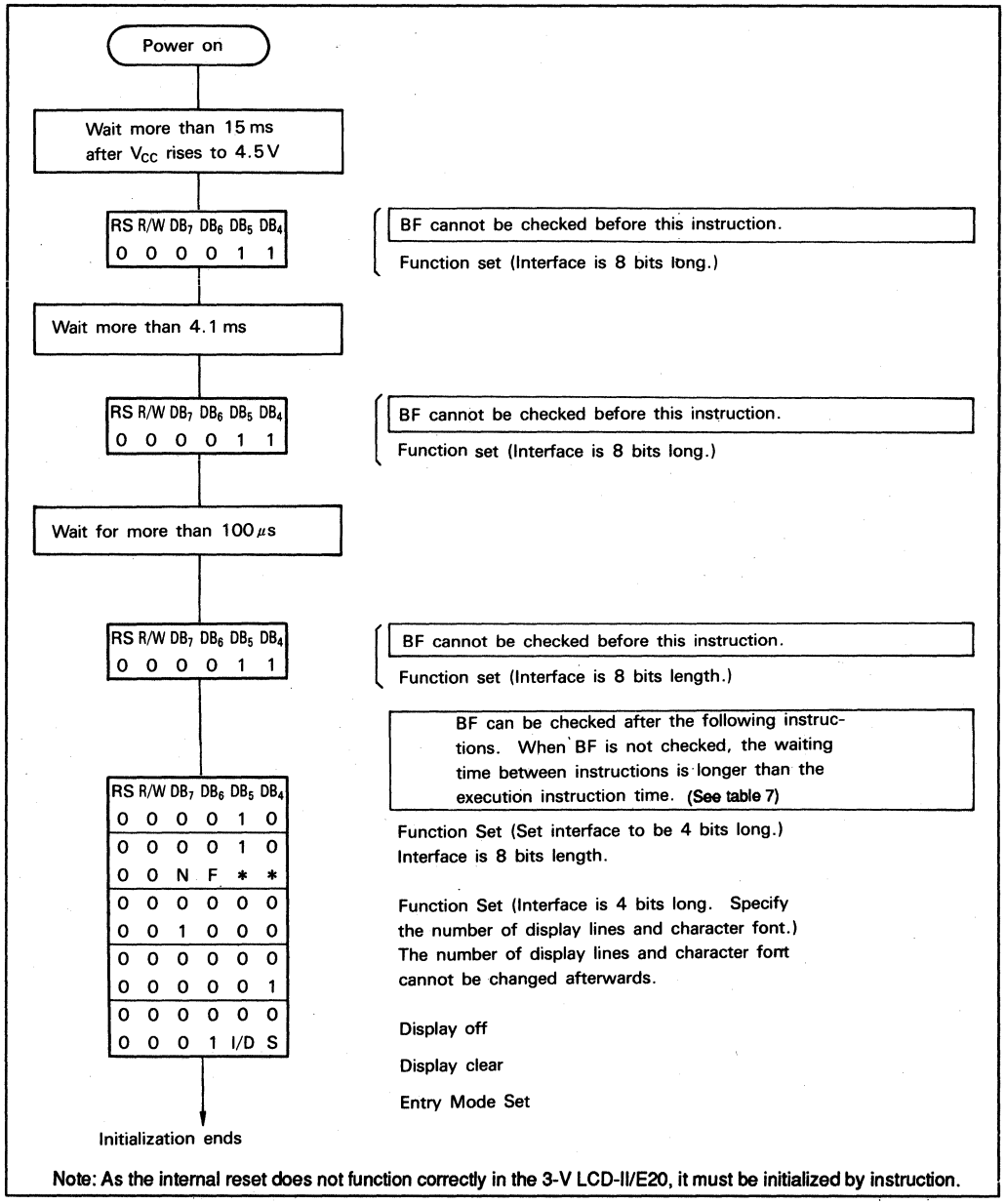
1:



Note: As the internal reset does not function correctly in the 3-V LCD-II/E20, it must be initialized by instruction.

Figure 25 8-Bit Interface

2:



Note: As the internal reset does not function correctly in the 3-V LCD-II/E20, it must be initialized by instruction.

Figure 26 4-Bit Interface

NOTES

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