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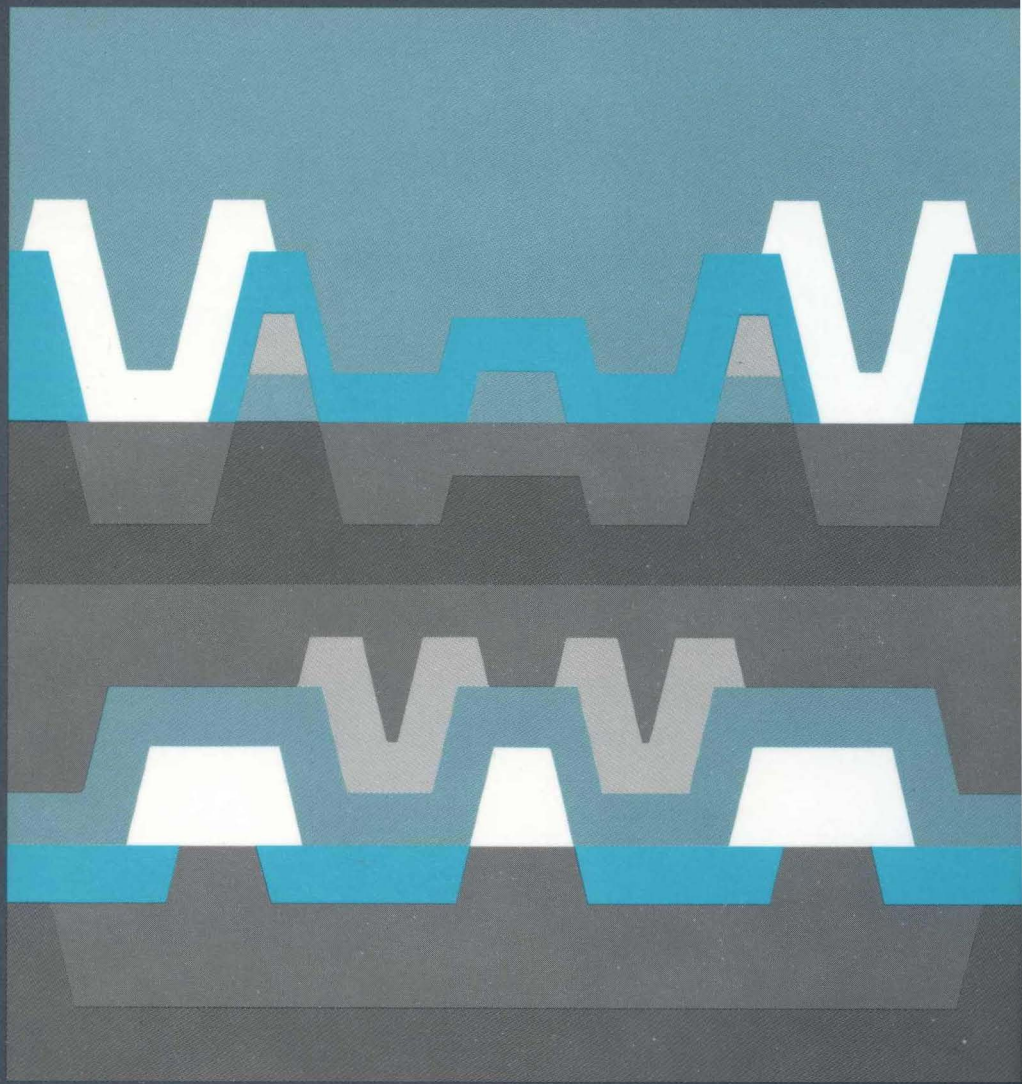
SRAM DATA BOOK



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March 1991

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- Quick Reference to Hitachi I.C. Memories
- Package Information
- Reliability of Hitachi I.C. Memories
- Quality Assurance of I.C. Memory
- Outline of Testing Method
- Application

QUICK REFERENCE GUIDE TO HITACHI MEMORIES

• MOS RAM

Mode	Total	Type No.	Process	Organization (word x bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package						Maintenance Only	Page
									Pin No.	DG	DP	FP	CP	TFP		
Static	16Kb	HM6268-25	CMOS	4K x 4	25	25	+5	0.1m/0.25	20		●					36
		HM6268-35			35	35					●					36
		HM6268-45			45	45					●					36
		HM6268L-25			25	25		5μ/0.25			●					36
		HM6268L-35			35	35					●					36
		HM6268L-45			45	45					●					36
		HM6267-35		16K x 1	35	35		0.1m/0.2			●					43
		HM6267-45			45	45					●					43
		HM6267-55			55	55					●					43
		HM6267L-35			35	35		5μ/0.2			●					43
		HM6267L-45			45	45					●					43
		HM6267L-55			55	55					●					43
	64Kb	HM6264A-10	CMOS	8K x 8	100	100		0.1m/15m	28		●	●				50
		HM6264A-12			120	120					●	●				50
		HM6264A-15			150	150					●	●				50
		HM6264AL-10			100	100		10μ/15m			●	●				50
		HM6264AL-12			120	120					●	●				50
		HM6264AL-15			150	150					●	●				50
		HM6264AL-10L			100	100		10μ/15m			●	●				50
		HM6264AL-12L			120	120					●	●				50
		HM6264AL-15L			150	150					●	●				50
		HM6288-25		16K x 4	25	25		0.1m/0.3	22 24 (SOJ)		●		●			59
		HM6288-35			35	35					●		●			59
		HM6288L-25			25	25					●		●			59
		HM6288L-35			35	35					●		●			59
		HM6788-25	Bi-CMOS		25	25		10m/0.23	22		●				●	67
		HM6788-30			30	30					●				●	67
		HM6788H-15			15	15		0.28			●				●	71
		HM6788H-20			20	20					●				●	71
		HM6788HA-12			12	12		0.3			●					75
		HM6788HA-15			15	15					●					75
		HM6788HA-20			20	20					●					75
	64Kb	HM6289-25	CMOS	16K x 4 (with OE\)	25	25		0.1m/0.3	24				●			80
		HM6289-35			35	35							●			80
		HM6289L-25			25	25							●			80
		HM6289L-35			35	35							●			80
		HM6789-25	Bi-CMOS		25	25		0.23			●		●		●	91
		HM6789-30			30	30					●		●		●	91
		HM6789H-15			15	15		0.28			●		●		●	98
		HM6789H-20			20	20					●		●		●	98
		HM6789HA-12			12	12		0.3			●		●			105
		HM6789HA-15			15	15					●		●			105
		HM6789HA-20			20	20					●		●			105
		HM6287-45	CMOS	64K x 1	45	45		0.1m/0.3	22		●				●	113
		HM6287-55			55	55					●				●	113
		HM6287-70			70	70					●				●	113
		HM6287L-45			45	45		10μ/0.3			●				●	113
		HM6287L-55			55	55					●				●	113
		HM6287L-70			70	70					●				●	113
		HM6287H-25			25	25		0.1m/0.3	22 24 (SOJ)		●		●			120
		HM6287H-35			35	35					●		●			120
		HM6287HL-25			25	25		10μ/0.3			●		●			120
		HM6287HL-35			35	35					●		●			120
		HM6787-25	Bi-CMOS		25	25		0.18	22		●				●	129
		HM6787-30			30	30					●				●	129
		HM6787H-15			15	15		0.21	22		●		●		●	134
		HM6787H-20			20	20					●		●		●	134
		HM6787HA-12			12	12		0.3	24 (SOJ)		●		●			139
		HM6787HA-15			15	15					●		●			139
		HM6787HA-20			20	20					●		●			139

1

• MOS RAM

Mode	Total	Type No.	Process	Organization (word x bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package						Maintenance Only	Page
									Pin No	DG	DP	FP	CP	TFP		
Static	256Kb	HM62256-8	CMOS	32K x 8	85	85	+5	0.2m/40m	28		●	●				144
		HM62256-10			100	100					●	●				144
		HM62256-12			120	120					●	●				144
		HM62256-15			150	150					●	●				144
		HM62226L-8			85	85		10μ/40m			●	●				144
		HM62256L-10			100	100					●	●				144
		HM62256L-12			120	120					●	●				144
		HM62256L-15			150	150					●	●				144
		HM62256L-10SL			100	100		10μ/40m			●	●				144
		HM62256L-12SL			120	120					●	●				144
		HM62256L-15SL			150	150					●	●				144
		HM62256A-8			85	85		0.2m/40m			●	●				152
		HM62256A-10			100	100					●	●				152
		HM62256A-12			120	120					●	●				152
		HM62256A-15			150	150					●	●				152
		HM62226AL-8			85	85		10μ/40m			●	●		●		152
		HM62256AL-10			100	100					●	●		●		152
		HM62256AL-12			120	120					●	●		●		152
		HM62256AL-15			150	150					●	●		●		152
		HM62256AL-8SL			85	85		30μ/0.3			●	●		●		152
		HM62256AL-10SL			100	100					●	●		●		152
		HM62256AL-12SL			120	120					●	●		●		152
		HM62256AL-15SL			150	150					●	●		●		152
		HM62832H-25			25	25		0.1m/0.3			●		●			160
		HM62832H-35			35	35					●		●			160
		HM62832UH-15			15	15		15μ/0.55			●		●			166
		HM62832UH-20			20	20					●		●			166
		HM62832UHL-15			15	15		15μ/0.4			●		●			166
		HM62832UHL-20			20	20					●		●			166
		HM67832SH-10	Bi-CMOS		10	10		0.4					●			173
		HM67832SH-12			12	12							●			173
		HM6208H-25	CMOS	64K x 4	25	25		0.1m/0.3			●		●			181
		HM6208H-35			35	35					●		●			181
		HM6208HL-25			25	25		30μ/0.3			●		●			181
		HM6208HL-35			35	35					●		●			181
		HM6708A-15	Bi-CMOS		15	15		0.45	28		●		●			188
		HM6708A-20			20	20					●		●			188
		HM6708A-25			25	25					●		●			188
		HM6708SH-10			10	10		0.4					●			193
		HM6708SH-12			12	12							●			193
		HM6709A-15			15	15		0.45			●		●			202
		HM6709A-20			20	20					●		●			202
		HM6709A-25			25	25					●		●			202
		HM6709SH-10			10	10		0.4					●			209
		HM6709SH-12			12	12							●			209
		HM6207H-25	CMOS	256K x 1	25	25		0.1m/0.3	24		●		●			217
		HM6207H-35			35	35					●		●			217
		HM6207HL-25			25	25		20μ/0.3			●		●			217
		HM6207HL-35			35	35					●		●			217
		HM6707A-15	Bi-CMOS		15	15		0.45			●		●			224
		HM6707A-20			20	20					●		●			224
		HM6707A-25			25	25					●		●			224
	288Kb	HM62932-15	CMOS	32K x 9	15	15		15μ/0.35	32				●			229
		HM62932-20			20	20							●			229
		HM62932L-15			15	15							●			229
		HM62932L-20			20	20							●			229
		HM62D932-15			15	15							●			237
		HM62D932-20			20	20							●			237
		HM62D932L-15			15	15							●			237
		HM62D932L-20			20	20							●			237

• **MOS RAM**

Mode	Total	Type No.	Process	Organization (word x bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package: Pin No.	DG	DP	FP	CP	TFP	Maintenance Only	Page
Static	1Mb	HM628128-7	CMOS	128K x 8	70	70	+5	0.1m/75m	32		●	●		●		245
		HM628128-8			85	85					●	●		●		245
		HM628128-10			100	100					●	●		●		245
		HM628128-12			120	120					●	●		●		245
		HM628128L-7			70	70		10μ/75m			●	●		●		245
		HM628128L-8			85	85					●	●		●		245
		HM628128L-10			100	100					●	●		●		245
		HM628128L-12			120	120					●	●		●		245
		HM624256A-20		256K x 4	20	20		0.1m/0.35	28		●		●			257
		HM624256A-25			25	25					●		●			257
		HM624256A-35			35	35					●		●			257
		HM624256AL-20			20	20					●		●			257
		HM624256AL-25			25	25					●		●			257
		HM624256AL-35			35	35					●		●			257
		HM624257-35			35	35			32				●			267
		HM624257-45			45	45							●			267
		HM624257L-35			35	35							●			267
		HM624257L-45			45	45							●			267
		HM621100A-20		1M x 1	20	20			28		●		●			275
		HM621100A-25			25	25					●		●			275
		HM621100A-35			35	35					●		●			275
		HM621100AL-20			20	20					●		●			275
		HM621100AL-25			25	25					●		●			275
		HM621100AL-35			35	35					●		●			275
	4Mb	HM628512-5		512K x 8	55	55		10μ/75m	32		●	●				281
		HM628512-7			70	70					●	●				281
		HM628512-8			85	85					●	●				281
		HM628512-10			100	100					●	●				281
		HM628512L-5			55	55					●	●				281
		HM628512L-7			70	70					●	●				281
		HM628512L-8			85	85					●	●				281
		HM628512L-10			100	100					●	●				281
		HM628512L-5L			55	55					●	●				281
		HM628512L-7L			70	70					●	●				281
		HM628512L-8L			85	85					●	●				281
		HM628512L-10L			100	100					●	●				281
		HM624100-25		1M x 4	25	25		0.05/0.75					●	●		295
		HM624100-30			30	30							●	●		295
		HM624100-35			35	35							●	●		295
		HM624100-45			45	45							●	●		295
		HM624100L-30			30	30		0.5m/0.7					●	●		295
		HM624100L-35			35	35							●	●		295
		HM624100L-45			45	45							●	●		295
		HM621400-25		4M x 1	25	25		0.05/0.75					●	●		302
		HM621400-30			30	30							●	●		302
		HM621400-35			35	35							●	●		302
		HM621400-45			45	45							●	●		302
		HM621400L-30			30	30		0.5m/0.7					●	●		302
		HM621400L-35			35	35							●	●		302
		HM621400L-45			45	45							●	●		302
Static RAM Module	4Mb	HM66205L-85		512K x 8	85	85		40μ/80m	32		●					288
		HM66205L-10			100	100					●					288
		HM66205L-12			120	120					●					288

• Cache Static RAM and Fast SRAM Modules

Mode	Total	Type No.	Process	Organization (word x bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package						Maintenance Only	Page
									Pin No	DG	DP	FP	CP	TFP		
Cache Static RAMs	120Kb	HM62A168-25	CMOS	8K x 16 (2 way)	25	25	+5	1.1 (max)	52				●			311
		HM62A168-30			30	30							●			311
		HM62A168-35			35	35							●			311
		HM62A168B-25			25	25							●			311
		HM62A168B-35			35	35							●			311
	128Kb	HM62A188-25		8K x 18 (2 way)	25	25							●			311
		HM62A188-30			30	30							●			311
		HM62A188-35			35	35							●			311
		HM62A188B-25			25	25							●			311
		HM62A188B-35			35	35							●			311
	288Kb	HM62A932-14		32K x 9	14	20		TBD	44				●			323
		HM62A932-19			19	25							●			323
		HM62A932-24			24	30							●			323
		HM62A932-34			34	40							●			323
	328Kb	HM62A2016-17		8K x 20 (2 way)	17	17							●			333
		HM62A2016-20			20	20							●			333
		HM62A2016-25			25	25		1.1 (max)	52				●			333
		HM62A2016-30			30	30							●			333
	1Mb	HM62A8128-20		128K x 8	30	20							●			346
	1.2Mb	HM62A9128-20		128K x 9	30	20		25m/0.75	32				●			346
Fast SRAM Module	256Kb	HB66B1616A-25		16K x 16 (module)	25	25										355
		HB66B1616A-35			35	35		0.4m/1.2	36							355
	2Mb	HB66A2568A-25		256K x 8 (module)	25	25										365
		HB66A2568A-35			35	35		0.8m/2.4	60							365

• MOS Pseudo Static RAM

Mode	Total	Type No.	Process	Organization (word x bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package						Maintenance Only	Page
									Pin No	DG	DP	FP	CP	TFP		
Pseudo Static	256Kb	HM65256B-10	CMOS	32K x 8	100	160	+5	2m/0.175	28		●	●				375
		HM65256B-12			120	190					●	●				375
		HM65256B-15			150	235					●	●				375
		HM65256B-20			200	310					●	●				375
		HM65256BL-10			100	160					●	●				375
		HM65256BL-12			120	190					●	●				375
		HM65256BL-15			150	235					●	●				375
		HM65256BL-20			200	310					●	●				375
	1Mb	HM658128A-8		128K x 8	80	130		0.35m/0.25	32		●	●		●		383
		HM658128A-10			100	160					●	●		●		383
		HM658128A-12			120	190					●	●		●		383
		HM658128AL-8			80	130					●	●		●		383
		HM658128AL-10			100	160					●	●		●		383
		HM658128AL-12			120	190					●	●		●		383
		HM658128AL-8L			80	130					●	●		●		383
		HM658128AL-10L			100	160					●	●		●		383
		HM658128AL-12L			120	190					●	●		●		383
	4Mb	HM658512-8		512K x 8	80	130		0.2m/0.25			●	●				395
		HM658512-10			100	160					●	●				395
		HM658512-12			120	190					●	●				395
		HM658512L-8			80	130					●	●				395
		HM658512L-10			100	160					●	●				395
		HM658512L-12			120	190					●	●				395
		HM658512L-8L			80	130					●	●				395
		HM658512L-10L			100	160					●	●				395
		HM658512L-12L			120	190					●	●				395

• ECL RAM

Mode	Total	Type No.	Process	Organization (word x bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package						Maintenance Only	Page
									Pin No	DG	FG	CG				
ECL 10K	64Kb	HM10494-10	Bi-CMOS	16K x 4	10	10	-5.2	0.8	28	●	●					404
		HM10494-12			12	12				●	●					404
		HM10490-10		64K x 1	10	10		0.57	22	●						408
		HM10490-12			12	12				●						408
	256Kb	HM10500-15		256K x 1	15	15		0.52	24	●						412
ECL 100K	64Kb	HM100494-10		16K x 4	10	10	-4.5	0.65	28	●	●					417
		HM100494-12			12	12				●	●					417
	256Kb	HM100504-10		64K x 4	10	10		0.5			●					421
		HM100504-12			12	12					●					421
		HM100500-18		256K x 1	18	18		0.5	24	●		●				425
	1Mb	HM100514-15		256K x 4	15	15		0.8	32		●					430
		HM100510-15		1M x 1	15	15		0.7	28		●					434
ECL 101K	64Kb	HM101494-10		16K x 4	10	10	-5.2	0.75	28	●	●					438
		HM101494-12			12	12				●	●					438
		HM101490-10		64K x 1	10	10		0.57	22	●						442
		HM101490-12			12	12				●						442
	256Kb	HM101504-10		64K x 4	10	10		0.5	28		●					446
		HM101504-12			12	12					●					446
		HM101500-15		256K x 1	15	15		0.5	24		●	●				450
	1Mb	HM101514-15		256K x 4	15	15		0.8	32		●					454
		HM101510-15		1M x 1	15	15		0.7	28		●					458

• FIFO Memory

Mode	Total	Type No.	Process	Organization (word x bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package						Maintenance Only	Page
									Pin No	DG	DP	FP	CP	TFP		
FIFO	18Kb	HM63921-20	CMOS	2K x 9	20	20	+5	0.6 (max)	28		●					465
		HM63921-25			25	25					●					465
		HM63921-35			35	35					●					465
	36Kb	HM63941-20		4K x 9	20	20					●					477
		HM63941-25			25	25					●					477
		HM63941-35			35	35					●					477

The package codes apply to the material as follows:

DP Dual In-line Package—Plastic
DG Dual In-line Package—Ceramic
FP Flat Package/SOP (Dual = 2-sided; Quad. = 4-sided)—Plastic
FG Flat Package—Ceramic
TFP Thin SOP—Plastic
CG Chip Carrier (4-sided)—Ceramic
CP J-lead Package (SOJ = 2-sided; PLCC = 4-sided)—Plastic

Package Information

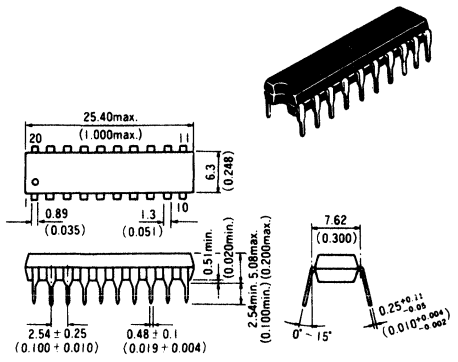
HITACHI®

■ PACKAGE INFORMATION

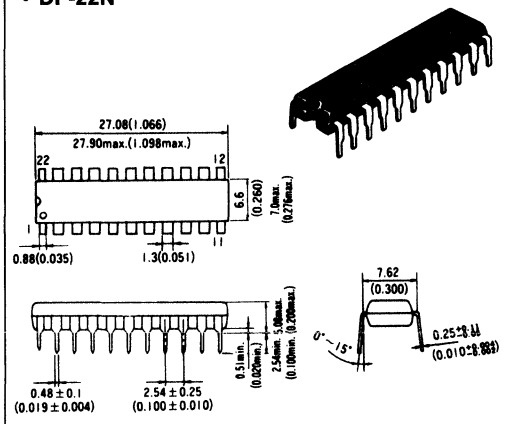
• **Dual-in-line Plastic**

Unit: mm (inch) Scale 1/1

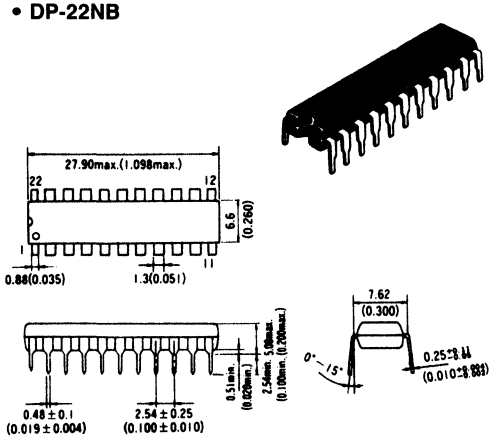
• **DP-20N**



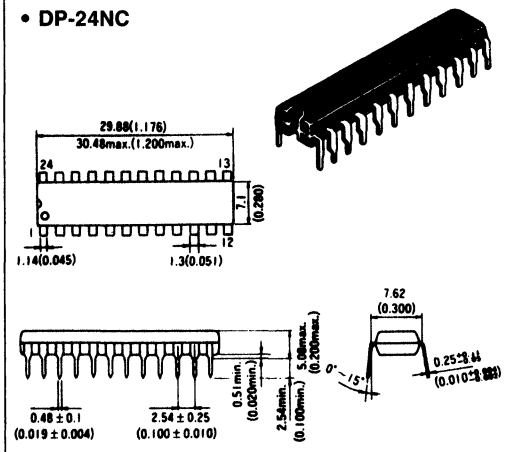
• **DP-22N**



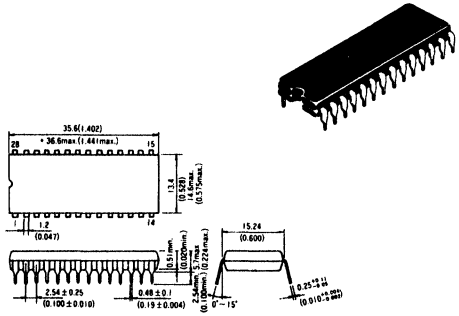
• **DP-22NB**



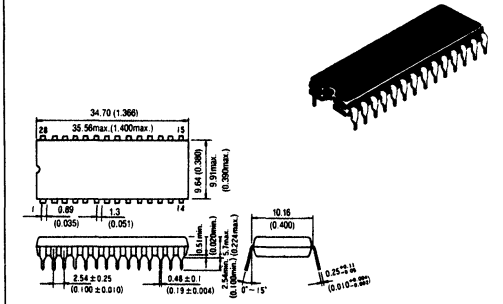
• **DP-24NC**



• **DP-28**



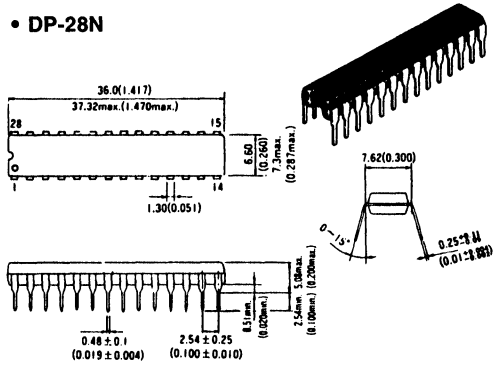
• **DP-28C**



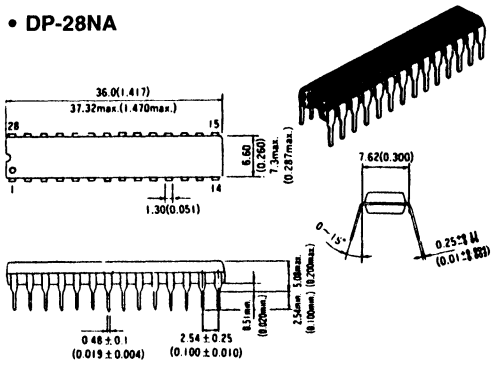
• Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

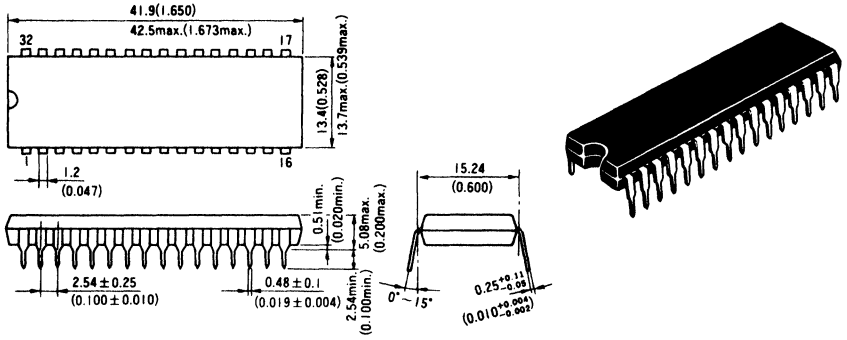
• DP-28N



• DP-28NA



• DP-32



Applicable ICs

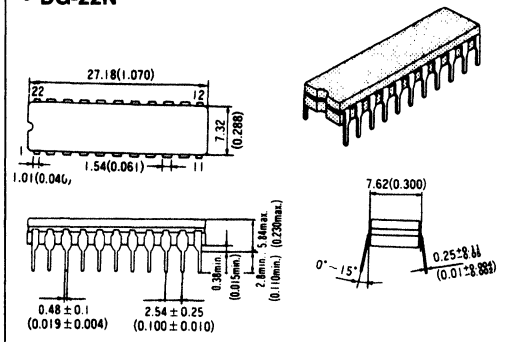
DP-20N	HM6268P Series, HM6268LP Series, HM6267P Series, HM6267LP Series
DP-22N	HM6287P Series, HM6287LP Series
DP-22NB	HM6288P Series, HM6288LP Series, HM6788P Series, HM6788HP Series, HM6788HAP Series, HM6287HP Series, HM6287HLP Series, HM6787P Series, HM6787HP Series, HM6787HAP Series, HM6787HAJP Series
DP-24NC	HM6789P Series, HM6789HP Series, HM6789HAP Series, HM6208HP Series, HM6208HLP Series, HM6708AP Series, HM6207HP Series, HM6207HLP Series, HM6707AP Series
DP-28	HM6264AP Series, HM6264ALP Series, HM6264ALP-L Series, HM62256P Series, HM62256LP Series, HM62256LP-L Series, HM65256BP Series, HM65256BLP Series, HM62256AP Series, HM62256ALP Series, HM62256ALP-SL Series
DP-28C	HM624256P Series, HM624256LP Series, HM624256AP Series, HM624256ALP Series, HM621100AP Series, HM621100ALP Series
DP-28N	HM6264ASP Series, HM6264ALSP Series, HM6264ALSP-L Series, HM6709AP Series
DP-28NA	HM62832HP Series, HM62832UHP Series, HM67832SHP Series, HM63921P Series, HM63941P Series, HM62256ASP Series, HM62256ALSP Series, HM62256ALSP-SL Series
DP-32	HM658128ALP Series, HM658128ALP-L Series, HM658128ADP Series, HM658128DP Series, HM658128LP Series, HM658512LP Series, HM658512P Series, HM628128P Series, HM628128LP Series, HM628128LP-SL Series, HM628512P Series, HM628512LP Series, HM628512LP-L Series

PACKAGE INFORMATION

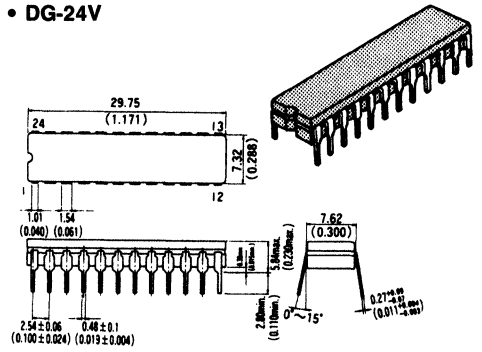
• **CERDIP**

Unit: mm (inch) Scale 1/1

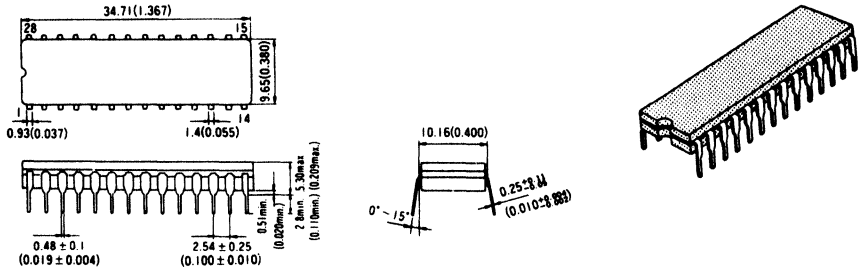
• **DG-22N**



• **DG-24V**



• **DG-28N**



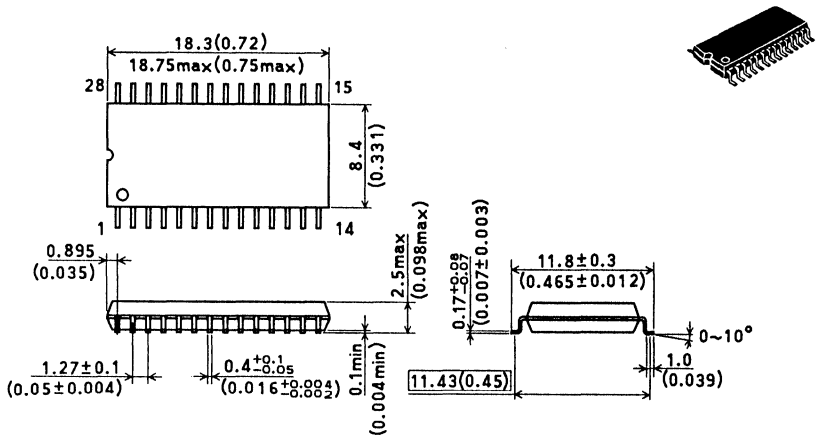
Applicable ICs

DG-22N	HM10490 Series, HM101490 Series
DG-24V	HM10500 Series, HM100500 Series
DG-28N	HM10494 Series, HM100494 Series, HM101494 Series

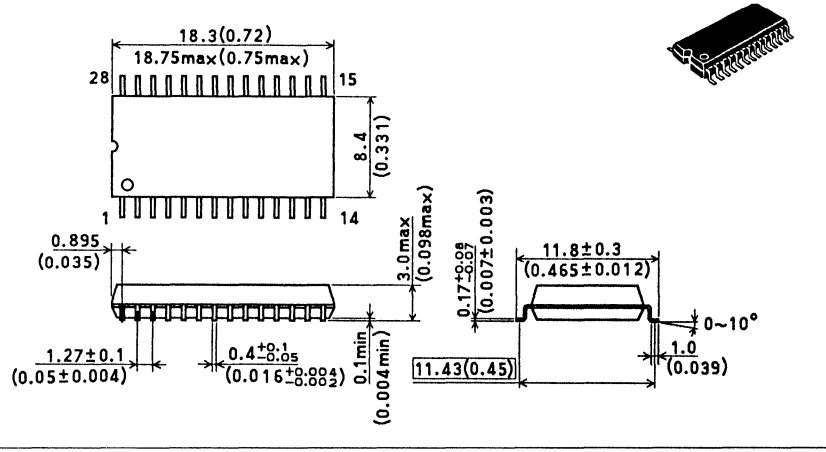
- **Flat Package**

Unit: mm (inch) Scale 1½

- **FP-28D**



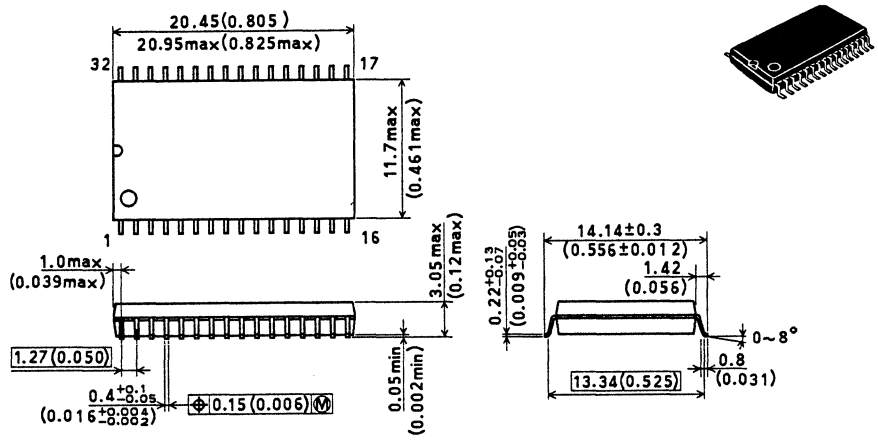
- **FP-28DA**



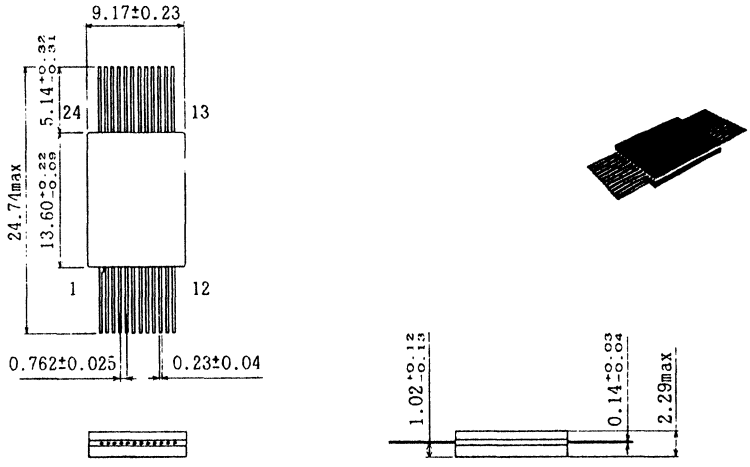
- **Flat Package**

Unit: mm (inch) Scale 1½

- **FP-32D**



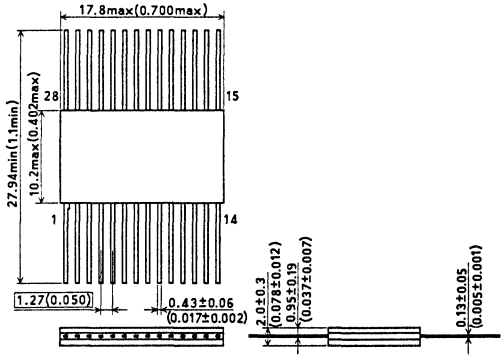
- **FG-24A**



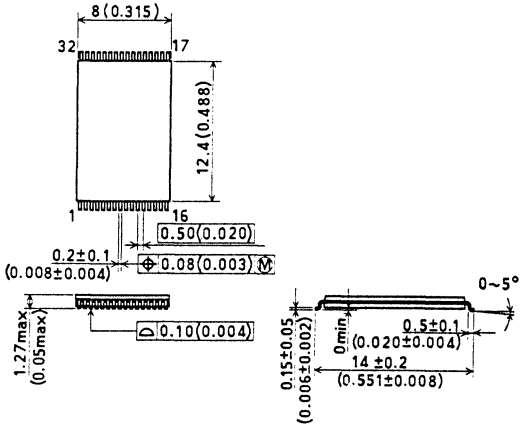
- **Flat Package**

Unit: mm (inch) Scale 1½

- **FG-28D**



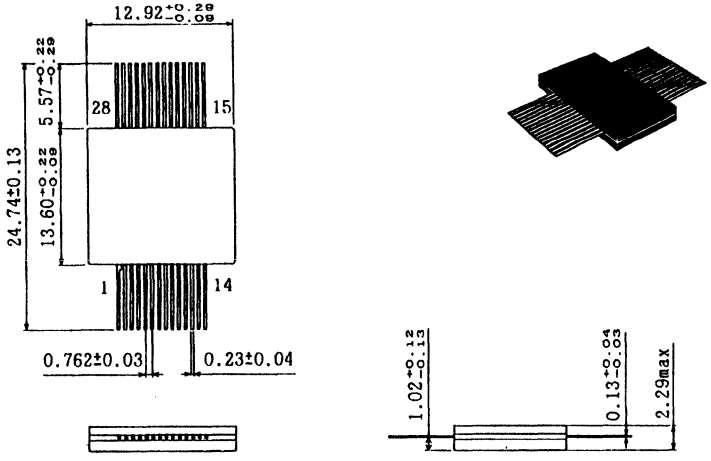
- **TFP-32DA**



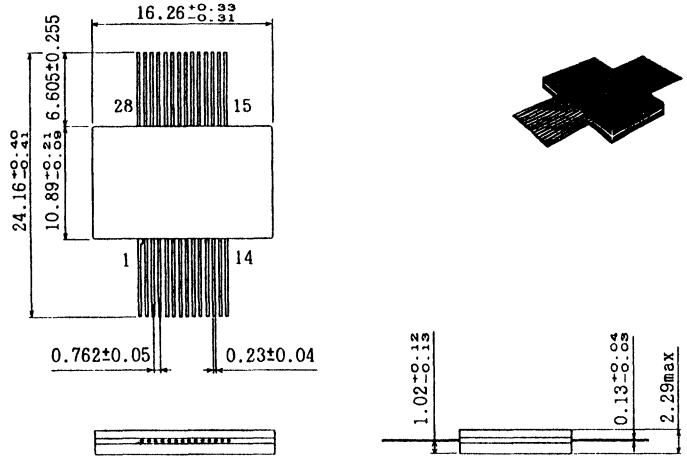
- **Flat Package**

Unit: mm (inch) Scale 1½

- **FG-28DA**



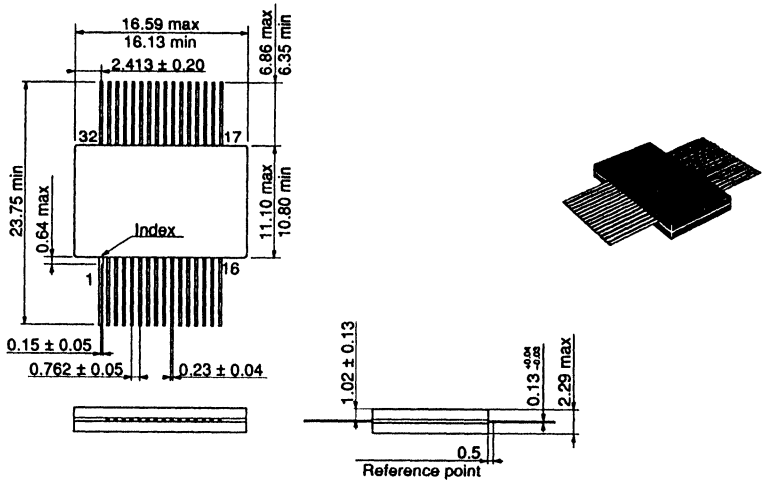
- **FG-28DB**



• Flat Package

Unit: mm (inch) Scale 1½

• FG-32D



Applicable ICs

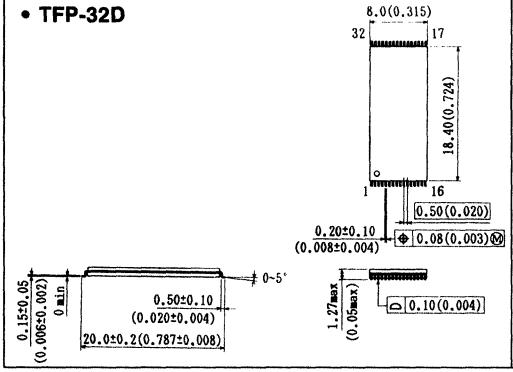
FP-28D	HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series
FP-28DA	HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series, HM62256FP-T Series, HM62256LFP-T Series, HM62256LFP-SLT Series, HM65256BFP-T Series, HM65256BLFP-T Series, HM62256AFP-T Series, HM62256ALFP-T Series, HM62256ALFP-SLT Series
FP-32D	HM628128FP Series, HM628128LFP Series, HM658128DFP Series, HM658128LFP Series, HM658512LFP Series, HM658512DFP Series, HM65256BFP-T Series, HM65256BLFP-T Series, HM62256AFP-T Series, HM62256ALFP-T Series, HM62256ALFP-SLT Series, HM628128LFP-SL Series, HM628512FP Series, HM628512LFP Series, HM628512LFP-SL Series, HM658128ALFP Series, HM658128ALFP-L Series, HM658128ADFP Series
FG-24A	HM100500F Series, HM101500F Series
FG-28D	HM10494F Series, HM100494F Series, HM101494F Series
TFP-32DA	HM628128T Series, HM628128LT Series, HM62256A Series, HM62256AL Series
FG-28DA	HM101510F Series, HM100510F Series
FPG-28DB	HM100504F Series
FG-32D	HM100514F Series, HM101514F Series

PACKAGE INFORMATION

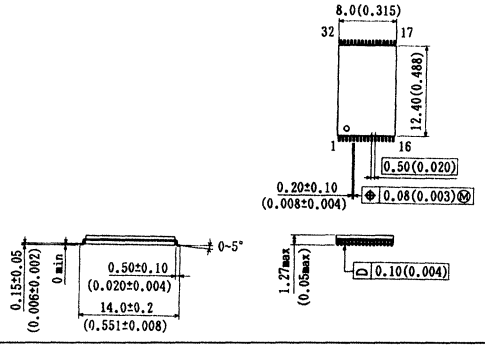
• TSOP Packages

Unit: mm (inch) Scale 1½

• TFP-32D



• TFP-32DA



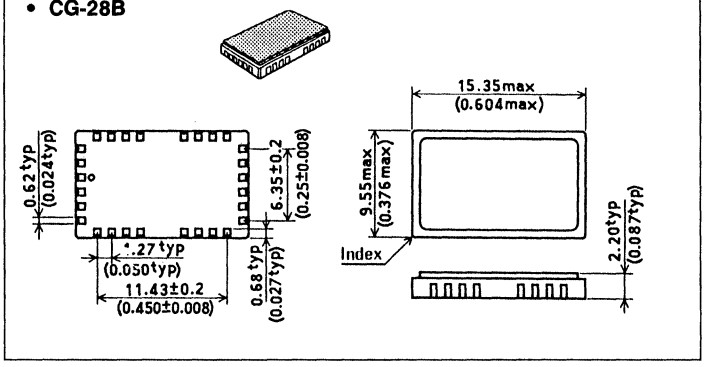
Applicable ICs

TFP-32D	HM628128LT Series, HM628128LR Series
TFP-32DA	HM62256ALT Series, HM62256ALT-SL Series, HM658128ALT-L Series, HM658128ALT Series, HM658128ADT Series

• Leadless Chip Carrier

Unit: mm (inch) Scale 1½

• CG-28B



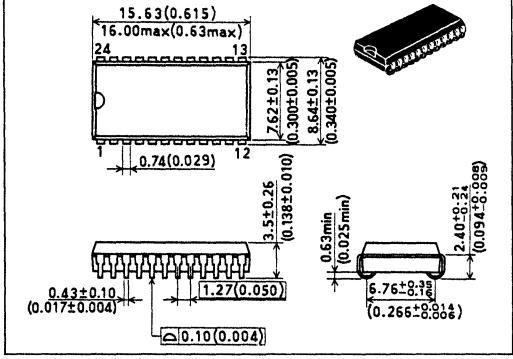
Applicable ICs

CG-28B	HM100500CG Series, HM101500CG Series

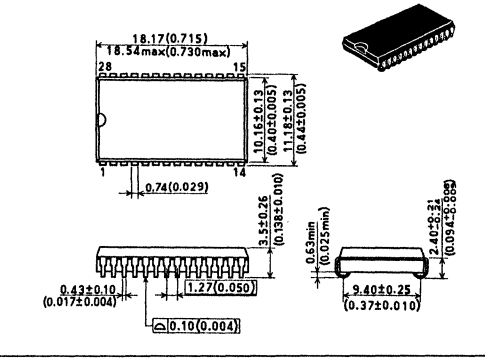
• Flat Package (J-bend Leads)

Unit: mm (inch) Scale 1½

• CP-24D



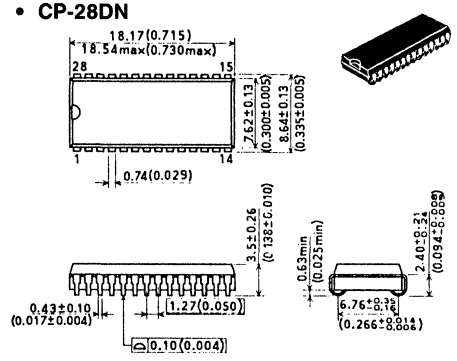
• CP-28D



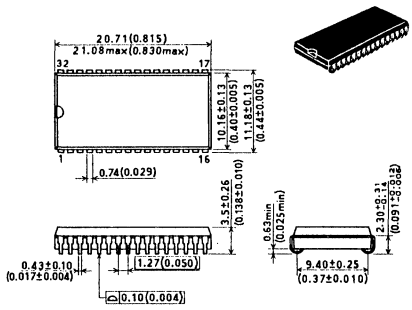
• Flat Package (J-bend Leads)

Unit: mm (inch) Scale 1½

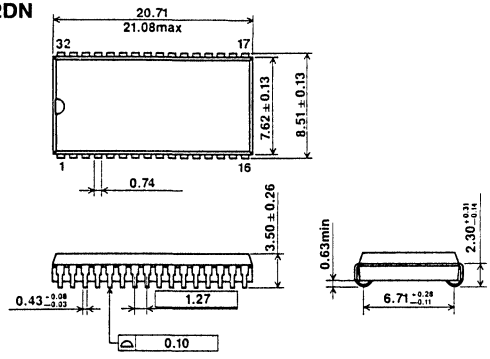
• CP-28DN

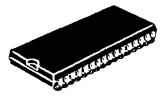


• CP-32D

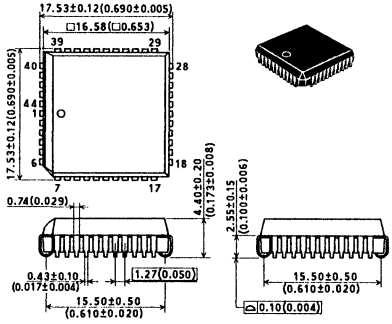


• CP-32DN

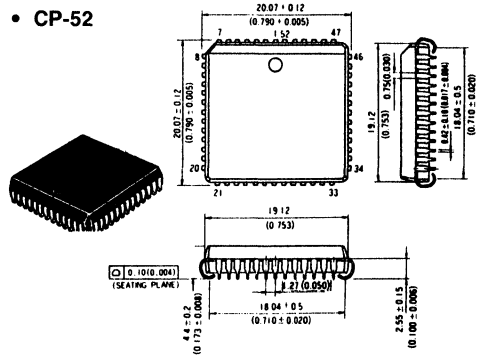




• CP-44



• CP-52



Applicable ICs

CP-24D	HM6288JP Series, HM6288LJP Sseries, HM6289JP Series, HM6289LJP Series, HM6789JP Series, HM6789HJP Series, HM6789HAJP Series, HM6287HJP Series, HM6287HLJP Series, HM6787HJP Series, HM6287HAJP Series, HM6208HJP Series, HM6208HLJP Series, HM6708AJP Series, HM6207HJP Series, HM6207HLJP Series, HM6207AJP Series
CP-28D	HM624256JP Series, HM624256LJP Series, HM624256AJP Series, HM624256ALJP Series, HM621100AJP Series, HM621100ALJP Series
CP-28DN	HM62832HJP Series, HM62832UHJP Series, HM62832SHJP Series, HM6709AJP Series
CP-32D	HM624257JP Series, HM624257LJP Series, HM101504JP Series, HM62A8128JP Series, HM62A9128JP Series HM624100JP Series, HM624100JLP Series, HM621400JP Series, HM621400JLP Series
CP-32DN	HM62932JP Series, HM62932LJP Series, HM62D932JP Series, HM62D932LJP Series
CP-44	HM62A932CP Series
CP-52	HM62A168CP Series, HM62A188CP Series, HM62A2016CP Series

RELIABILITY CHARACTERISTICS FOR SEMICONDUCTOR DEVICES

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along with proper environmental conditions. It is important to examine semiconductor device characteristics in light of their reliability.

- Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.
- Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.
- Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.
- Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data cannot be used in some cases.
- Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.
- Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should also be reviewed when electrode and package materials are not suited for particular environmental conditions.
- Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

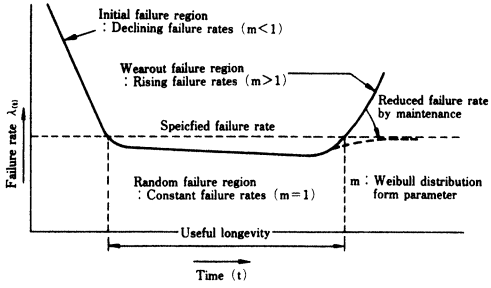


Figure 1 Typical failure rate curve

Device reliability is generally represented by the failure rate. 'Failure' means that a device loses its function, including intermittent degradation as well as complete destruction.

Generally, the failure rate of electric components and equipment is represented by the bathtub curve shown in Figure 1. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

SEMICONDUCTOR FAILURE TYPES AND THEIR MECHANISM

Semiconductor device failures are categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These are summarized in Table 1. Typical failure mechanisms are:

Surface Deterioration

The pn junction has a charge density of 10^{14}–$10^{20}/cm^3$. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to a depletion layer, electric characteristics of the junction tend to be easily varied. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model.

Table 1 Failure Modes, Mechanisms and Related Causes

Failure modes	Failure mechanisms	Failure related causes	
Withstanding voltage reduced, Short, Leak current increased, h_{FE} degraded, Threshold voltage variation, Noise	Pin hole, Crack, Uneven thickness, Contamination, Surface inversion, Hot carrier injected	Passivation	Surface oxide film, Insulating film between wires
Open, Short, Resistance increased	Flaw, Void, Mechanical damage, Break due to uneven surface, Non-ohmic contact, Insufficient adhesion strength, Improver thickness, Electromigration, Corrosion	Metallization	Interconnection, Contact, Through hole
Open, Short Resistance increased	Bonding runout, Compounds between metals, Bonding position mismatch, Bonding damaged	Connection	Wire bonding, Ball bonding
Open, Short	Disconnection, Sagging, Short	Wire lead	Internal connection
Withstanding voltage reduced, Short	Crystal defect, Crystallized impurity, Photo resist mismatching	Diffusion, Junction	Junction diffusion, Isolation
Open, Short, Unstable operation, Thermal resistance increased	Peeling, chip, Crack	Die bonding	Connection between die and package
Short, Leak current Increased, Open, Corrosion disconnection, Soldering failure	Integrity, moisture ingress, Impurity gas, High temperature, Surface contamination, Lead rust, Lead bend, break	Package sealing	Packaging, Hermetic Seal, Lead plating, Hermetic package & plastic package, Filler gas
Short, Leak current increased	Dirt, Conducting foreign matter, Organic carbide	Foreign matter	Foreign matter in package
Short, Open, Fusing	Electron destroyed	Input/output pin	Electrostatistics, Excessive Voltage, Surge
Soft error	Electron hole generated	Disturbance	α particle
Leak current increased	Surface inversion		High electric field

One example is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage (BV_{DS}) by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 2 μm to 0.8 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices employ improved design and process techniques to prevent these problems. However, as processes becomes finer, surface deterioration may possibly become a serious problem.

Electrode-Related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticeable failures include electromigration and Al wiring corrosion in plastic sealed packages.

ELECTROMIGRATION

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with the current of scattering electrons, an 'electron wind' is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

MULTI-METAL LINE RELATED FAILURES

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

AL LINE CORROSION AND DISCONNECTION

When plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Figure 2). Under high-temperature and high-humidity, corrosion is randomly generated over the element surface. However, after an extended period of time, the corrosion has not significantly increased. Accordingly, this failure is possibly due

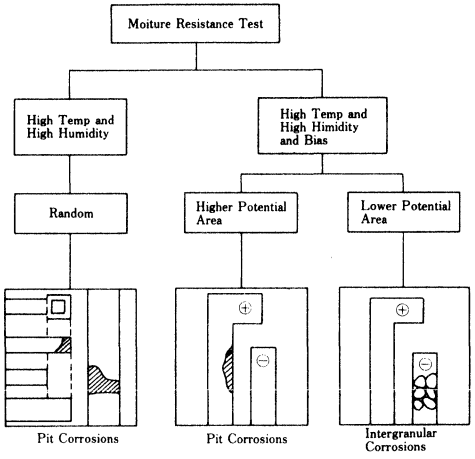


Figure 2 Categorized Al corrosion mode

to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high-temperature, high-humidity condition, corrosion is generated in higher potential areas while in lower potential areas, grain corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Figure 3.

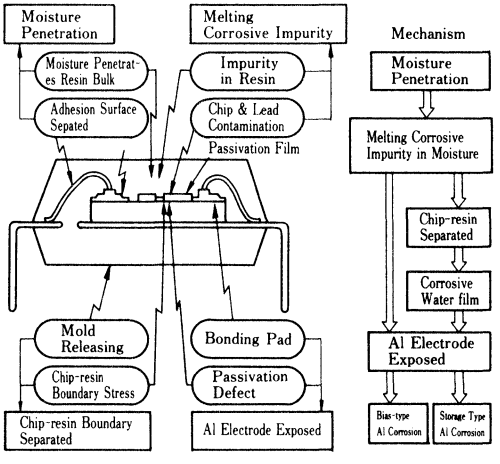


Figure 3 Plastic package cross section and Al corrosion mechanism

Bonding Related Failures

DEGRADATION CAUSED BY INTERMETALLIC FORMATION

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film. This is the most serious problem in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

WIRE CREEP

Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

CHIP CRACK

With the increase in chip size associated with the increased number of incorporated functions, more problems can occur during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

REDUCED MAXIMUM POWER DISSIPATIONS

Heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance, resulting in decreased maximum power dissipations.

Sealing Related Failures

Hermetically sealed packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between the different ionized materials.
2. Intermittent moving foreign metals short.
3. Al line corrosion due to extraneous H_2O caused by hermetic failure.

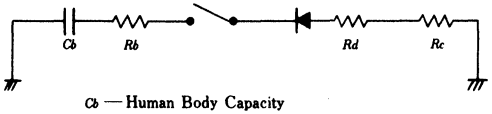
Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parastic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone and then amplifying it.

Disturbance

ELECTROSTATIC DISCHARGE DESTRUCTION

Destruction caused by electrostastic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure; the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Fig. 4. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged with 2000V, the dissipated energy is obtained as follows: With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.



Cb — Human Body Capacity
Rb — Human Body Resistance
Rd — Device Resistance
Rc — Resistance Between Device and Ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} J$$

Figure 4 Equivalent circuit of human body model

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Fig. 5. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

In the field induced model, a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction: 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high-frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

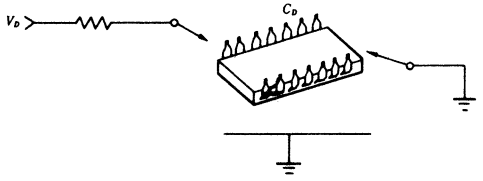


Figure 5 Equivalent circuit of charging model

LATCH-UP

Latch-up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch-up can occur when: 1) an accidental surge voltage exceeds the maximum rating, 2) there is a power supply ripple, 3) an unregulated power supply and noise is applied or 4) a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parasitic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is turned off or the flowing current reduced to a certain level. Once latch-up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch-up. Latch-up triggering input or output currents start to flow under the following conditions:

$V < {}_{in}V_{CC}$ or $V_{in} <$ GND for input level
$V > {}_{out}V_{CC}$ or $V_{out} <$ GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

Soft errors

When α particles are generated from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating modes, causing temporary soft errors. This phenomenon is shown in Fig. 6. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, organic material, PIQ, is applied to the surface of the device.

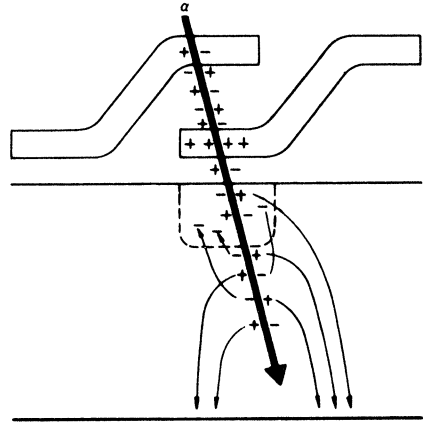


Figure 6 Soft error caused by α particles in dynamic memory

FINE GEOMETRY RELATED PROBLEMS

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 3 μm → 2 μm → 1.3 μm → 0.8 μm.

The problems associated with finer geometry are shown in Table 2.

Table 2 Finer geometry related problems

Item	Problems	Countermeasure
5V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering • Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical & horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

RELIABILITY TEST DATA ON Hi-BiCMOS MEMORY

Hi-BiCMOS memory is newly designed based on the latest fine machining technologies which features the low electric consumption/high integrity of CMOS and the high speed/high drivability of bipolar. These devices can attain the high speed of ECL and the low electric consumption of CMOS. Input and output level supports both ECL and TTL. Reliability test data with the HM100490-15 (64k-words × 1-bit) and the HM6788P-25 (16k-words × 4-bits) are listed in Tables 3 and 4.

Table 3 Results of Hi-BiCMOS Memory Reliability Tests

Test item	HM100490-15 (Cerdip)					Test item	HM6788P-25 (Plastic)					Remarks
	Test conditon	Samples	Total test time	Failures	Failure rate		Test condition	Samples	Test test time	Failures	Failure rate	
High-temperature pulse operation	T_a=125°C V_{EE}=−4.5V	380	C.H. 3.8×10^5	0	1.g 2.4×10^{-6}	High temperature pulse operation	T_a=125°C V_{CC}=5.0V	420	C.H. 4.2×10^5	1*1	1/h 4.8×10^{-6}	*1 foreign matter
						Moisture endurance	85°C 85%RH 5V	210	2.1×10^5	0	4.8×10^{-6}	
High-temp. storage	T_a=200°C	330	3.3×10^5	0	3.0×10^{-6}	Pressure cooker	121°C100%RH	80	0.16×10^5	0	6.3×10^{-5}	

Table 4 Results of Hi-BiCMOS Memory Environmental Tests

Test item	Test condition	HM100490-15 (Cerdip)		HM6788P-25 (Plastic)	
		Samples	Failure	Samples	Failure
Temperature cycling	−55°C ~ −150°C 100 cyles	180	0	180	0
Soldering heat	250°C 10 seconds	22	0	22	0
Thermal shock	0°C ~ 100°C 10 cycles	50	0	50	0
Mechanical shock	1500G, 0.5ms Three times each for X, Y and Z	22	0	—	—
Variable frequency	100 ~ 200Hz, 20G Three times each for X, Y and Z	22	0	—	—
Constant acceleration	20000G, 1 minute, each for X, Y and Z	22	0	—	—

RELIABILITY TEST DATA ON MOS MEMORIES

The reliability test data on the HM62256 (32k-word × 8-bit) and the HM628128 (128K-word × 8-bit) are listed in Tables 5 and 6.

Table 5 Results of MOS Memory Reliability Tests

Test item	Test condition	HM62256FP (SOP)				HM628128FP (SOP)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr.)	Samples	Total total time	Failures	Failure rate* (1/hr.)	
High-temperature pulse operation	125°C/5.5V	3088	3.11×10^6	0	$8.88 \times 10^{*7}$	1038	1.04×10^6	0	$8.86 \times 10^{*7}$	*1 Foreign×2 *2 Leak×1
	125°C/7V	455	4.55×10^5	0	$2.02 \times 10^{*6}$	951	5.33×10^5	1*1	$3.79 \times 10^{*6}$	
	150°C/7V	103	1.00×10^5	1*1	$2.02 \times 10^{*5}$	80	1.60×10^5	0	$5.75 \times 10^{*6}$	
Moisture endurance	85°C/85% RH 7V	680	6.80×10^5	0	$1.35 \times 10^{*6}$	127	2.54×10^5	0	$3.62 \times 10^{*6}$	
Pressure cooker	121°C/100% RH	320	6.40×10^4	1*2	$3.16 \times 10^{*5}$	90	2.70×10^4	0	$3.41 \times 10^{*5}$	

*Confidence level 60%

Table 6 Results of MOS Memory Environmental Tests

Test item	Test condition	HM62256FP (SOP)		HM628128FP (SOP)	
		Samples	Failure	Samples	Failure
Temperature cycling	-55°C to 150°C 500 cycles	482	0	105	0
Soldering heat	260°C 10 seconds	22	0	22	0
Thermal shock	-65°C to 150°C 15 cycles	76	0	77	0
Mechanical shock	1500G. 0.5ms	—	—	—	—
Variable frequency	100 to 2000 Hz, 20G	—	—	—	—
Constant acceleration	6000G	—	—	—	—

Figure 7 Time change in access time for Hi-BiCMOS memory

Example	
Device name	HM100490
Test condition	Ta = 125°C, V_{EE} = -4.5V all bit scanning
Failure criteria	t_{AA} = 15ns
Failure mechanism	Surface degradation
Results: Access time is stabilized.	

Example of time change in access time for Hi-BI CMOS memory

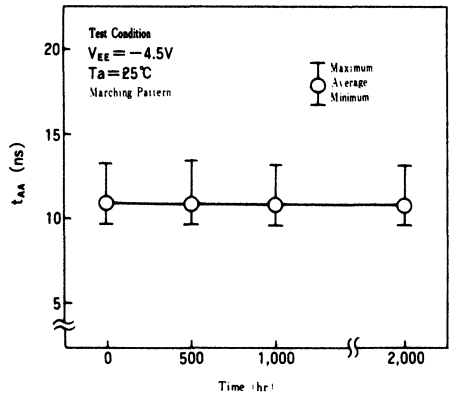


Figure 8 Time change in V_{CC} min and t_{AA} for Hi-BiCMOS memory

Example	
Device name	HM6788P-25
Test condition	Ta = 125°C, V_{CC} = –5.0V all bit scanning
Failure criteria	V_{CC} = 4.5V, t_{AA} = 25ns
Failure mechanism	Surface degradation
Results: Both of V_{CC} (min) and t_{AA} are stabilized.	

Example of time change in V_{CC} min and t_{AA} for Hi-Bi CMOS memory

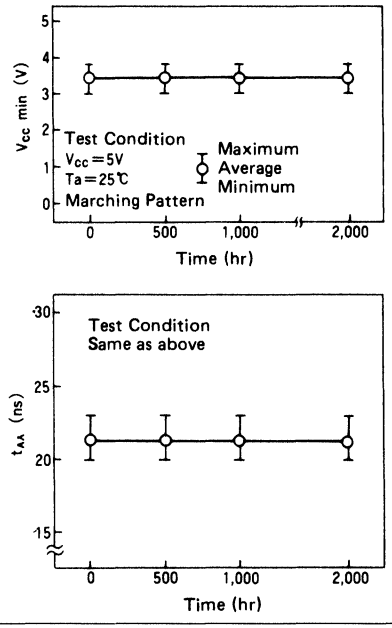
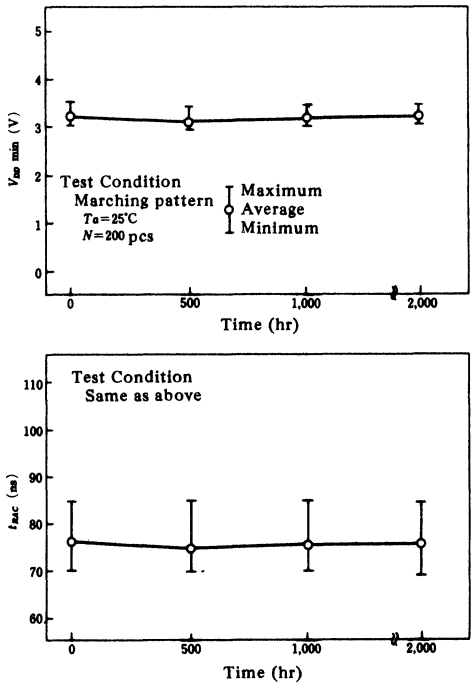


Figure 9 Time change in V_{DD} min and t_{RAC} for MOS memory

Example	
Device name	HM511000P
Test condition	Ta = 125°C, V_{CC} = –7V all bit scanning
Failure criteria	V_{DD} = 4.5V, $\triangle V_{DD}$ = 1.0V
Failure mechanism	Surface degradation
Results: Access time (t_{AA}) is stabilized and is within the failure criteria.	
Note: Test accuracy is 0.2V, 2 ns.	

Example of time change in V_{DD} min and t_{RAC} for MOS



1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are to meet individual users' purpose and their required quality level and also to maintain the satisfied level for general application. Hitachi has made efforts to assure the standardized reliability of our IC memories in actual usage. To meet users' requests and to cover expanding application, Hitachi performs the followings;

(1) Establish the reliability in design at the stage of new product development.
(2) Establish the quality at all steps in manufacturing process.
(3) Intensify the inspection and the assurance of reliability of products.
(4) Improve the product quality based on marketing data.

Furthermore, to get higher quality and reliability, we cooperate with our research laboratories.
With the views and methods mentioned above, Hitachi makes the best efforts to meet the users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Target

Establishment of reliability target is important in manufacturing and marketing as well as function and price. It is not practical to determine the reliability target based on the failure rate under single common test condition. So, the reliability target is determined based on many factors such as each characteristics of equipment, reliability target of system, derating applied in design, operating condition and maintenance.

2.2 Reliability Design

Timely study and execution are essential to achieve the reliability based on reliability targets. The main items are the design standardization, device design including process and structural design, design review and reliability test.

(1) Design Standardization
Design standardization needs establishing design rules and standardizing parts, material, and process. When design rules are established on circuit, cell, and layout design, critical items about quality and reliability should be examined. Therefore, in using standardized process or material, even newly developed products would have high reliability, with the exception of special requirement on function.

(2) Device Design
It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in case of applying new process or new material, we study the technology prior to development of the device in detail.

(3) Reliability Test by Test Site
Test site is sometimes called Test Pattern. It is useful method for evaluating reliability of designing and processing ICs with complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode;
   - Analysis of relation between failure mode and manufacturing process condition.
   - Analysis of failure mechanism.
   - Establishment of QC point in manufacturing.
2. Effects of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and compared with the process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

2.3 Design Review

Design review is a method to confirm systematically whether or not design satisfies the performance required including by users, follows the specified ways, and whether or not the technical items accumulated in test data and application data are effectively applied.
In addition, from the standpoint of competition with other products, the major purpose of design review is to insure quality and reliability of the product. In Hitachi, design review is performed in designing new products and also in changing products.
The followings are the items to consider at design review.

(1) Describe the products based on specified design documents.
(2) Considering the documents from the standpoint of each participant, plan and execute the subprogram such as calculation, experiments and

investigation if unclear matter is found.

(3) Determine the contents and methods of reliability test based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Arrange the preparation for production.

(6) Plan and execute the sub-programs of design changes proposed by individual specialists, for tests, experiments and calculation to confirm the design change.

(7) Refer to the past failure experiences with similar devices, confirm the prevention against them, and plan and execute the test program for confirmation of them.

In Hitachi, these study and decision at design review are made using the individual check lists according to its objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

The following items are the general views of overall quality assurance in Hitachi;

(1) Problems is solved in each process so that even the potential failure factors will be removed at final stage of production.

(2) Feedback of information is made to insure satisfied level of process ability.

As the result, we assure the reliability.

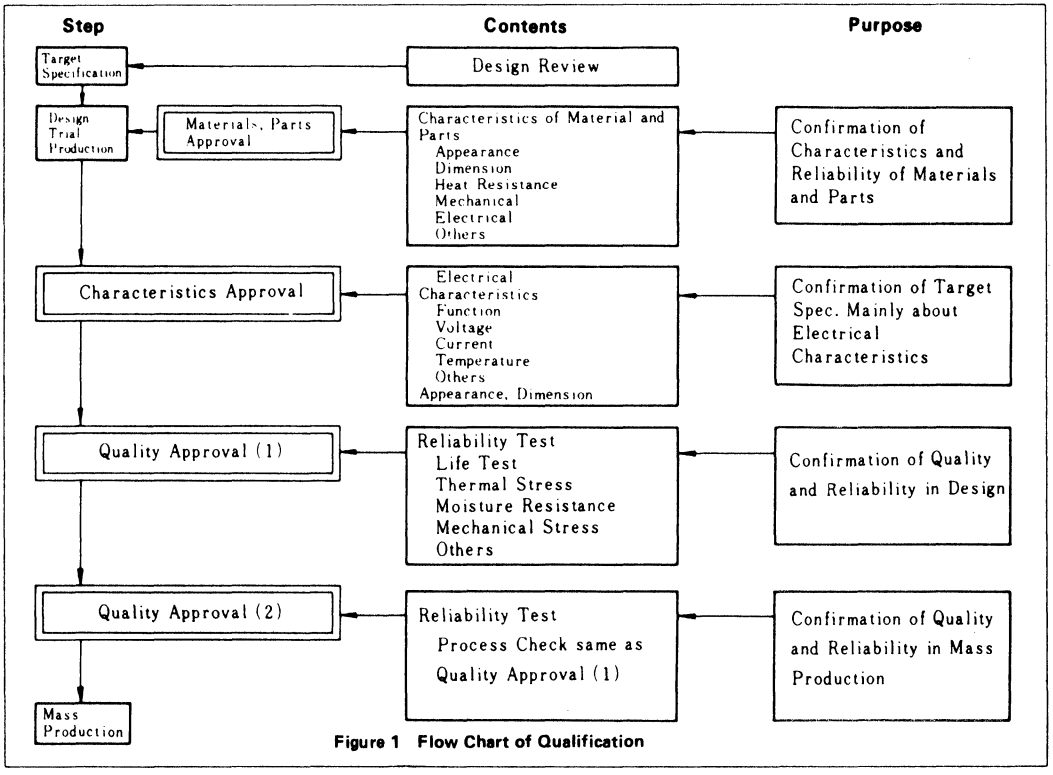


Figure 1 Flow Chart of Qualification

3.2 Qualification

To assure the quality and reliability, the qualification tests are done at each stage of trial production and mass production based on the reliability design described in section 2.

The followings are the views on qualification in Hitachi:

(1) From the standpoint of customers, qualify the products objectively by a third party.
(2) Consider the failure experiences and data from customers.
(3) Qualify every change in design and work.
(4) Qualify intensively on parts and materials and process.
(5) Considering the process ability and factor of manufacturing fluctuation, establish the control points in mass production.

Considering the views mentioned above, qualification shown in Fig. 1 is done.

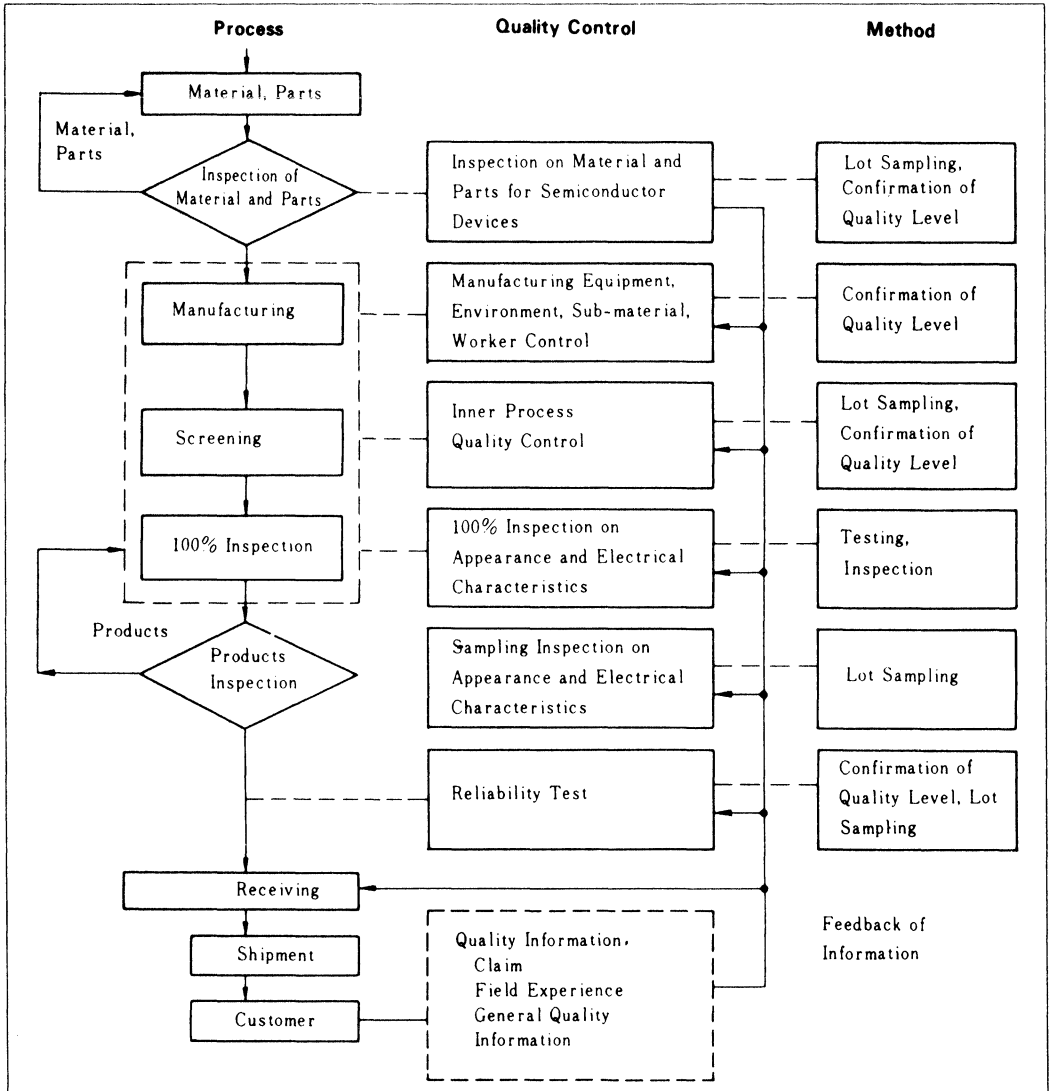


Figure 2 Flow Chart of Quality Control in Manufacturing Process

3.3 Quality and Reliability Control in Mass Production

To assure quality in mass production, quality is controlled functionally by each department, mainly by manufacturing department and quality assurance department. The total function flow is shown in Fig. 2.

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, quality control of parts and materials becomes more important. The items such as crystal, lead frame, fine wire for wire bonding, package and materials required in manufacturing process like mask pattern and chemicals, are all subject to inspection and control.

Besides qualification of parts and materials stated in 3.2, quality control of parts and materials is defined in incoming inspection. Incoming inspection is performed based on its purchase specification, drawing and mainly sampling test based on MIL-STD-105D. The other activities for quality assurance are as follows.

- **Table 1. Quality Control Check Points of Parts and Material (example)**

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

(1) Technology Meeting with Vendors
(2) Approval and Guidance of Vendors
(3) Analysis and tests of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

To control inner process quality is very significant for quality assurance of devices. The quality control of products in every stage of production is explained below. Fig. 3 shows inner process quality control.

(1) Quality Control of Products in Every Stage of Production

Potential failure factors of devices should be removed in manufacturing process. Therefore, check points are set up in each process so as not to move the products with failure factors to the next process. Especially, for high reliability devices, manufacturing lines are rigidly selected in order to control the quality in process. Additionally we perform rigid check per process or per lot, 100% inspection in proper processes so as to remove failure factors caused by manufacturing fluctuation, and screenings depending on high temperature aging or temperature cycling. Contents of controlling quality under processing are as follows:

- Control of conditions of equipment and workers and sampling test of uncompleted produsts.
- Proposal and execution of working improvement.
- Education of workers
- Maintenance and improvement of yield
- Picking up of quality problems and execution of countermeasures toward them.
- Communication of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing facilities have been developed with the need of higher devices in performance and the automated production. It is also important to determine quality and reliability.

In Hitachi, automated manufacturing is promoted to avoid manufacturing fluctuation, and the operation of high performance equipment is controlled to function properly.

As for maintenance inspection for quality control, daily and periodically inspections are performed based on specification on every check point.

As for adjustment and maintenance of measuring equipment, the past data and specifications are clearly checked to keep and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-material.

Quality and reliability of devices are affected especially by manufacturing process. Therefore, we thoroughly control the manufacturing circumstances such as temperature, humidity, dust, and the sub-materials like gas or pure water used in manufacturing process.

Dust control is essential to realize higher integration and higher reliability of devices. To maintain and improve the clearness of manufacturing site, we take care buildings, facilities, air-conditioning system, materials, clothes and works. Moreover, we periodically check on floating dust in the air, fallen dust or dirtiness on floor.

Process		Control Point		Purpose of Control
	▽ Purchase of Material			
Wafer		Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
	○ Surface Oxidation	Oxidation		Assurance of Resistance
	○ Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
	○ Photo Resist	Photo Resist		
	○ Inspection on Photo Resist		Dimension, Appearance	Dimension Level
	◇ PQC Level Check			Check of Photo Resist
	○ Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
	○ Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
	◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	
	○ Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
	○ Inspection on Evaporation			
	◇ PQC Level Check			
	○ Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
	○ Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
	○ Chip Scribe		Appearance of Chip	
	○ Inspection on Chip Appearance			
	◇ PQC Lot Judgement			
Frame				
	○ Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
			Appearance after Wire Bonding	Quality Check of Wire Bonding
	◇ PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
	○ Inspection after Assembling		Appearance after Assembling	
	◇ PQC Lot Judgement			
Package				
	○ Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
	◇ PQC Level Check	Marking	Marking Strength	
	○ Final Electrical Inspection			
	◇ Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
	○ Appearance Inspection			
	△ Sampling Inspection on Products			
	○ Receiving			
	Shipment			

Figure 3 Example of Inner Process Quality Control

3.3.3 Final Tests and Reliability Assurance

(1) Final Tests

Lot inspection is done by quality assurance department for the product passed in 100% test in final manufacturing process. Though 100% of passed products is expected, sampling inspection is subjected to prevent mixture of failed products by mistake. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Our lot inspection is based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability, the reliability tests are performed periodically, and performed on each manufacturing lot if user requires.

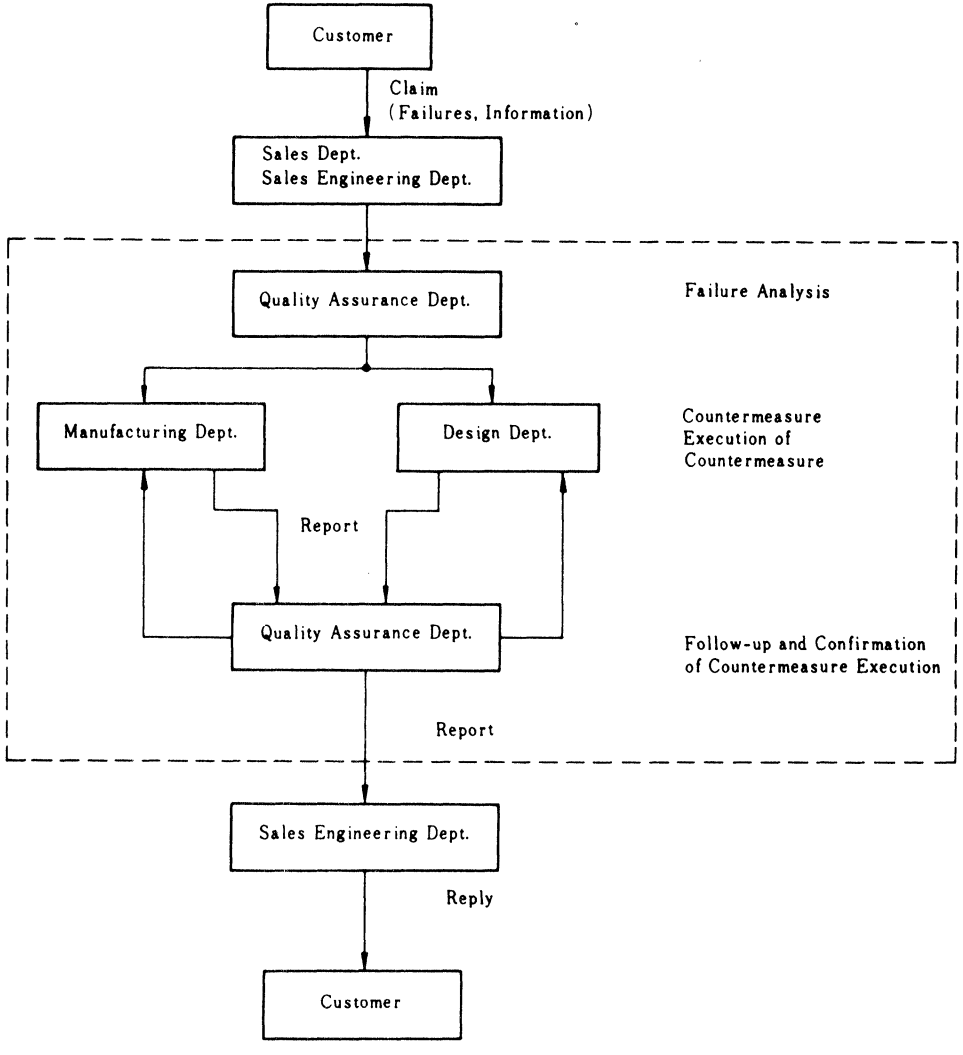


Figure 4 Process Flow Chart of Coping with Failure to a Customer

■ OUTLINE OF TESTING METHOD

1. INSPECTION METHOD

Compared to conventional core memories, IC memories contain all peripheral circuits, such as the decoder circuit, write circuit and read circuit. As a result, assembly and electrical inspection of ICs are all performed by IC manufacturers. Consequently, as the electrical inspection of IC memories are becoming more systematic, conventional IC inspection facilities are becoming useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a simple DC parameter facility. However, when the address input becomes multiplexed as in 16K, 64K and 256K memory, even the generation of the function test pattern becomes a serious problem.

In the memory IC inspection, its quality cannot be judged by DC test on external pins only, because the number of the element such as transistor which can be judged in the DC test is only 1/1000 of all elements. The followings are the address patterns proposed to inspect whether the internal circuits are functioning correctly.

(1) All "Low", All "High"
(2) Checker Flag
(3) Stripe Pattern
(4) Marching Pattern
(5) Galloping
(6) Waling
(7) Ping-Pong

Those are not all, but only representative ones. There are the pattern to check the mutual interference of bits and the pattern for the maximum power dissipation. Among the above mentioned patterns, those of (1) to (4) are called N pattern, which can check one sequence of N bit IC memory with the several times of N patterns at most. Those of (5) to (7) are called N^2 pattern, which need several times of N^2 patterns to check one sequence of N bit IC memory. Serious problem arises in using N^2 pattern in a large-capacity memory. For example, inspection of 16K memory with galloping pattern takes a lot of time – about 30 minutes. (1), (2) and (3) are rather simple and good methods, however, they are not perfect to find any failure in decoder circuits. Marching is the most simple and necessary pattern to check the function of IC memories.

2. MARCHING PATTERN

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits of "0"s. For example, a simple addressing of 16 bit memory is described below.

(1) Clear all bits . . . . . See Fig. 1 (a)
(2) Read "0" from 0th address and check that the read data is "0". Hereafter, "Read" means "checking and judging data"
(3) Write "1" on 0th address. . . . . See Fig. 1(b)
(4) Read "0" from 1st address.
(5) Write "1" on 1st address.
(6) Read "0" from nth address.
(7) Write "1" on nth address . . . . . See Fig. 1(c)
(8) Repeat (6) to (7) to the last address. Finally, all data will be "1".
(9) After all data become "1", repeat from (2) to (8) replacing "0" and "1".

In this method, 5N address patterns are necessary for the N-bit memory.

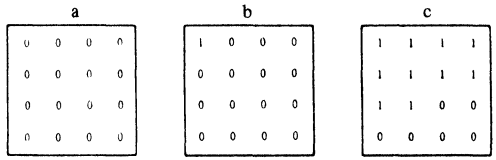


Figure 1 Addressing method of for 16 bit memory in the Marching pattern

1. Static RAM

1.1. Static RAM Memory Cell

The static RAM memory cell consists of flip-flops organized as 4 NMOS transistors and 2 load resistors as shown in figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

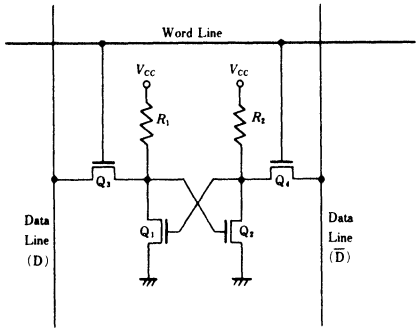


Figure 1-1. Static RAM Memory Cell

1.2. Data Retention Mode and Battery Back-up System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. So, it enables a battery back-up system to retain data during power failure.

Data Retention Mode: The important point in designing a battery back-up system is the timing relation between the memory power supply during the change (ordinal source → battery) and the chip select signal. If the timing for the change is missed, the data in memory might be destroyed.

Figure 1-2. shows the timing for switching the power supply. The following explains the technical terms related to the data retention mode.

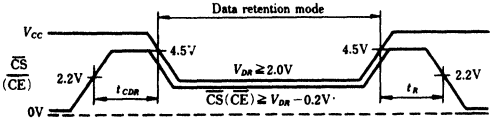


Figure 1-2. Timing for Battery Back-up Application

Data retention mode: The period that the power supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS}$ = V_{DR} - 0.2V).

t_{CDR} (time for chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (Operation recovery time): The minimum time needed to change from data retention mode to operating mode. Normally, it is the same as the cycle time of the memory.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally, the minimum supply voltage needed to retain memory data is 2 V.

I_{CCDR} (data retention current): The current consumption in data retention mode. It depends on memory power supply voltage and ambient temperature. It is specified at supply voltage (V_{DR}) = 3.0 V.

Battery Back-up System: battery back-up sequence is described in the following:

1. External circuit detects failure of system power supply.
2. External circuit changes RAM to standby mode.
3. External circuit separates RAM from system power supply.
4. External circuit switches to Back-up power supply.

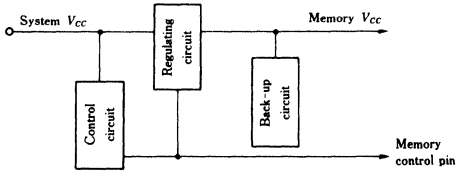


Figure 1-3. Example of Battery Back-up System

The control circuit detects the power failure and cuts off the power after switching memories to standby mode. On recovery, it confirms power supply and after some delay, returns memories to operating mode. The memory control signals depend on the types of memories used in the system.

* Using memory with only one $\overline{CS}$. NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. As the level of $\overline{CS}$ in data retention mode must be higher than V_{DR} – 0.2V, the power supply for this NAND gate must either be shared with the memory power supply, or be pulled up to the memory power supply.
* Using memory with two $\overline{CS}$. Basically, the signals are the same as mentioned above. In general use, two pins should be used for the control signal and the chip select signal respec-

tively. $\overline{CS}$, which can intercept current path of other pins in the input buffers, is for control signal input of data retention mode.

* Using memory with $\overline{CS}$ and CS. As CS selects the chips at high level, it is better to use CS than $\overline{CS}$ as control signal input for data retention mode. As soon as power down is detected, signals should be brought to low level. So a pull-up to the memory power supply level is not needed and circuit organization is simplified.

Figure 1-4 shows an example of a battery back-up system circuit. Hitachi recommends using CMOS logic for gate G_1 in control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch regulating circuit from system power supply to back-up power supply.

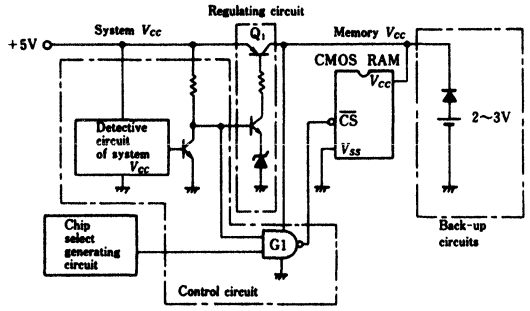


Figure 1-4. Example of Battery Back-up System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

A new type of memory, pseudo-static RAM has been developed to provide the advantages of dynamic RAM (low cost, high density) and static RAM (easy usage). IC memory consists of memory cells for data storage, and input/output circuits for interfacing to the external circuits. PSRAM provides the memory cell and peripheral circuits of DRAM and the external control circuits, which includes a part of the refresh control circuits not provided by dynamic RAM, and interface circuits similar to that of static RAM, on a chip, as shown in table 2-1. Address input is not multiplexed and data input/output is byte-wide like standard static RAM. With PSRAM × 8 organization, medium density memory system can be designed easily. PSRAM provides address refresh, automatic refresh and self refresh.

Figure 2-1 shows examples of system design using PSRAM and DRAM. Using PSRAM, the circuits interfacing CPU to DRAM can be drastically reduced.

Figure 2-2 shows block diagram of pseudo static RAM.

Table 2-1. PSRAM Features

	SRAM	PSRAM	DRAM
Memory Cell	4 Tr + 2 R	1 Tr + 1 C	
Organization	x1, x4, x8	x8	x1, x4
Address	Single Address		Multiplexed Address
Refresh	Nor Necessary	Necessary	
External Circuits	Simple ⟺ Complex		

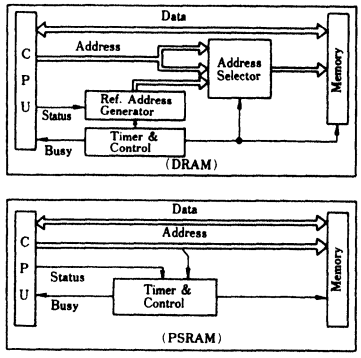


Figure 2-1. System Organization

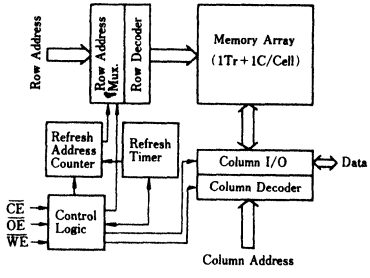


Figure 2-2. Block Diagram (PSRAM)

2.2. 1 Mbit Pseudo-Static RAM Function

Read/Write Cycle: Figure 2-3 and figure 2-4 show the timing chart for the read/write cycle of 1 Mbit pseudo-static RAM HM658128. The HM658128 can perform 2 types of access in a read cycle, $\overline{CE}$ access (Figure 2-3 (a)) and $\overline{OE}$ access figure 2-3 (b)). It writes the data at the rising edge of $\overline{WE}$ (figure 2-4 (a)) or at the rising edge of $\overline{CE}$ (figure 2-4 (b)). The $\overline{CS}$ pin should be brought high when the address is latched at the falling edge of $\overline{CE}$ in the read/write cycle. The HM658128 has no $\overline{OE}$ specification at the falling edge of $\overline{CE}$ as it provides both $\overline{OE}$ pin and $\overline{RFSH}$ pin.

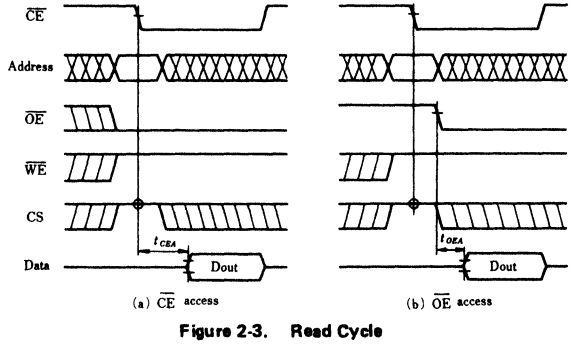


Figure 2-3. Read Cycle

CS Standby Mode: The HM658128 enters CS standby mode for one cycle if CS turns to low at the falling edge of $\overline{CE}$ (figure 2-5).

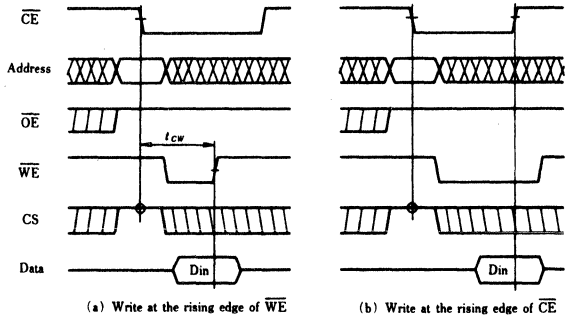


Figure 2-4. Write Cycle

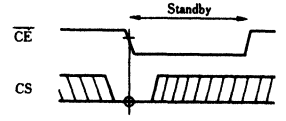


Figure 2-5. CS Standby Mode

Address Refresh: Address refresh mode performs refresh by access to row address (A0 – A8) 0 – 511 sequentially within 8 ms, as shown in figure 2-6 (in distributed mode). In this mode, CS should be high at falling edge of $\overline{CE}$.

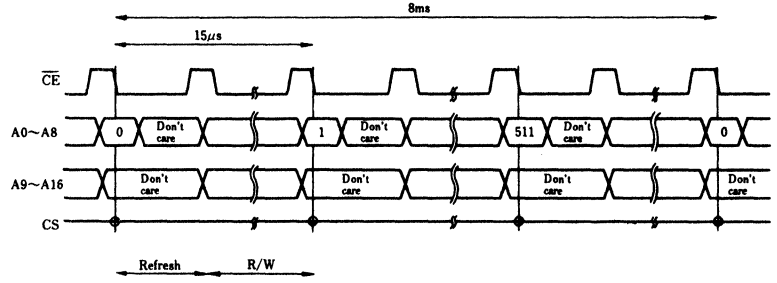


Figure 2-6. Address Refresh

Automatic Refresh: The HM658128 goes to automatic refresh mode if $\overline{RFSH}$ falls while $\overline{CE}$ is high and it is kept low for more than 180 ns.
It is not required to input the refresh address from address pins A0 – A8, as it is generated internally. Figure 2-7 shows the timing chart for distributed refresh. In automatic refresh mode, the timing for only $\overline{CE}$ and $\overline{RFSH}$ are specified.

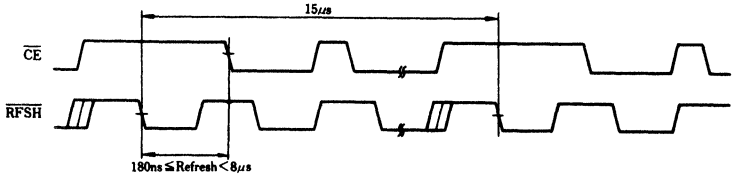


Figure 2-7. Automatic Refresh

Self Refresh: Self refresh mode performs refresh at the internally determined interval. The HM658128 enters the mode when the internal refresh timer is enabled by keeping $\overline{CE}$ high and $\overline{RFSH}$ low for more than 8 μs (figure 2-8).

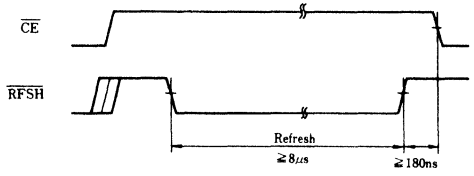


Figure 2-8. Self Refresh

Considerations on Using HM658128: The following should be considered when using the HM658128.

- Data retention. The HM658128 can retain the data with a battery (but not for long time). The HM658128L, low power version, offers typical self-refresh or standby current of 100μA.
  A 1-Mbyte system (using eight HM658128Ls) can retain the data for about 1.5 months with battery of 100 mAh current. V_{CC} = 5 V ± 10% must be maintained for data retention.
- Power on. Start HM658128 operation by executing more than eight initial cycles (dummy cycles) more than 100 μs after power voltage reaches 4.5 V – 5.5 V after power on.
- Bypass capacitor. Hitachi recommends inserting 1 bypass capacitor per RAM.

2.3 Pseudo-Static RAM Data Retention

PSRAM with self refresh retains data $\overline{CE}$ and $\overline{OE}$ are fixed for more than defined period. The following explains considerations for PSRAM data retention.

First, PSRAM cannot retain the data at low supply voltage.

They employ 1 MOS type memory cell as shown in figure 2-9. The charge is stored on the capacitor C as memory data. The data 1, written at low supply

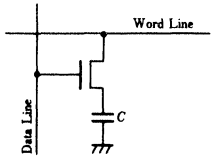


Figure 2-9. Memory Cell of PSRAM

voltage, cannot be read as 1 at high supply voltage.

Figure 2-10 indicates the operation voltage for self refresh and subsequent read of PSRAM. If the data is read out at more than 5 V of V_{CC}, for example, after self refresh is performed at V_{CC} = 3.7 V, it is destroyed.

PSRAM must be used at supply voltage from 4.5V to 5.5V.

Second self refresh current increases at low supply voltage.

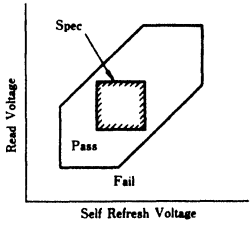


Figure 2-10. PSRAM Operating Voltage

PSRAM provides the voltage level detector circuit to reduce self refresh current. However, it should be noted that the circuit increases the current with low supply voltage in self refresh (figure 2-11). Self refresh current also increases at low temperature (figure 2-12).

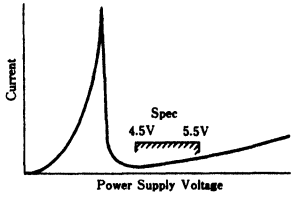


Figure 2-11. Self Refresh Current vs. Voltage

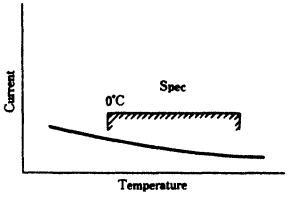


Figure 2-12. Self-Refresh Current vs Temperature

Please use PSRAM within the recommended operation range (V_{CC} more than 4.5 V, temperature more than 0°C) for data retention, especially using a battery.

3. INSTRUCTIONS FOR USING MEMORY DEVICES

3.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled according to the following instructions:

1. In transporting and storing memory devices, put them in conductive magazine or put all pins of each device into a conductive mat so that they are kept at the same potential. Manufacturers should give enough consideration to packing when shipping their products.
2. When devices touch a human body in mounting or inspection, the handler must be grounded. Do not forget to insert a resistor (1MΩ approx. is desirable) in series to protect the handles from electrical shock.
3. Keep the relative ambient humidity at about 50% in process.
4. For working clothes, cotton is preferrable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.
6. In transporting the board with memory devices mounted on it, cover it with conductive sheets.
7. Use conductive sheets of high resistance (about 10^9 ohm/□) to protect devices from electrostatic discharge. For, if dropped onto conductive materials like a metal sheet, devices may deteriorate or even breakdown owing to sudden discharg of the charge stored on the surface.
8. Never set the system to which memory devi/ are applied near anything that generates hig,, voltage (e.g. CRT Anode electrode, etc.).

3.2 Using CMOS Memories

As shown in figure 3-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistor. Figure 3-2 shows the relationship between the input voltage and current in this inverter. The top and bottom transistors turn ON and make current flown when the input voltage becomes intermediate level. Therefore, it is necessary to keep the input voltage below 0.2 V or above V_{CC} – 0.2 V in order to minimize power consumption. The data sheet specifies the stand-by current for both the cases of input level with minimum V_{IH} and maximum V_{IL} and that with 0.2V or V_{CC} – 0.2 V, and the difference in value is remarkably great. Some memory devices are designed to cut off such current flow in standby mode by the control of input signals, but it depends on device type. This should be confirmed in data sheet for each device type.

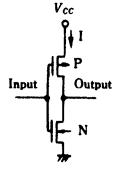


Figure 3-1. CMOS Inverter

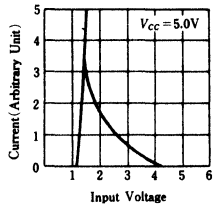


Figure 3-2. Relationship between Input Voltage & Current In CMOS Inverter

Another problem particular to CMOS devices is latch-up. Figure 3-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in figure 3-4. When positive DC current or pulse noise is applied (figure 3-4 (a)), TR3 is turned on owing to the bias voltage generated between base and emitter. And trigger current flows into GND through R_P, the base resistance of TR2. As a result, TR2 becomes conductive and current flows from power supply (V_{CC}) through the base resistance of TR1 (R_N), which puts TR1 into conduction, too. Then, as the base of TR2 is re-biased by collector current from TR1, the closed loop consisting of TR1 and TR2 reacts. Thus current flows constantly between power supply (V_{CC}) and GND even without trigger current caused by outside noise.

Latch-up can be caused by a negative pulse, too (figure 3-4 (bb)). Most of semiconductor memory manufacturers are trying to improve latch-up immunity of their products. Hitachi provides enough guard band by applying diffusion layer around inputs and outputs, taking care not to connect input to p + diffusion layer. Input voltage for 64 kbit static RAM HM6264A, for example, is specified as follows:

V_{IH} max 6.0 V (not depending on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
−0.3 V (DC level)

Thus almost no consideration for latch-up is required in system design.

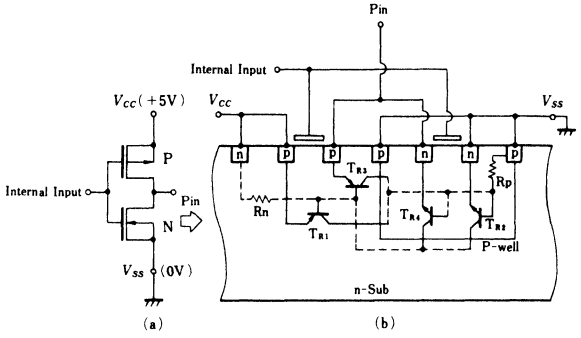


Figure 3-3. Cross Section Structure of CMOS Inverter

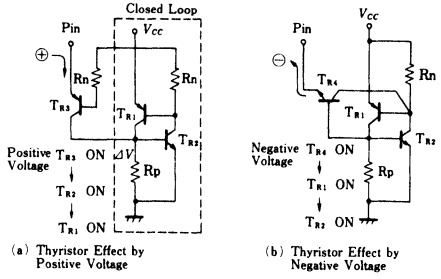


Figure 3-4. Equivalent Circuit of Parasitic Thyristor

3.3 Noise Prevention

Noise in semiconductor memories is roughly classified into input signal noise and power supply noise.

3.3.1 Input Signal Noise

Input signal noise is caused by overshoot and undershoot. If either of them is out of recommended DC operating conditions, normal operation is hindered, and voltage over absolute maximum rating will break the device. In operating high speed system, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohm into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because it is often caused by unstable reference voltage (GND level).

3.3.2 Power Supply Notice

The power source noise can be classed as low-frequency noise and high-frequency noise as shown in figure 3-5. To assure stable memory operation, the peak-to-peak power supply voltage in the presence of low-or high-frequency noise should be held below 10 percent of its standard level.

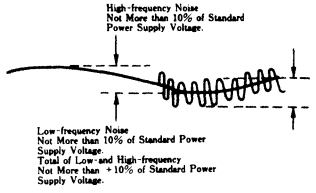


Figure 3-5. Power Source Noise

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1 – 0.01 μF should be inserted near the device. The following points must be considered in designing pattern of the board:

★For bypass capacitors, use titanium ceramic, or tantalum capacitors which have better high-frequency characteristics.

★Bypass capacitors must be applied as near to the power supply pin of memory devices as possible, and inductance in the path from V_{CC} pin to V_{SS} pin through the bypass capacitor must be as little as possible.

★The line connected to the power supply on the board should be as wide as possible.

★It is preferrable for the power supply line to be at right angles to devices selected at the same time, less too much peak current should flow through one power supply line at a time

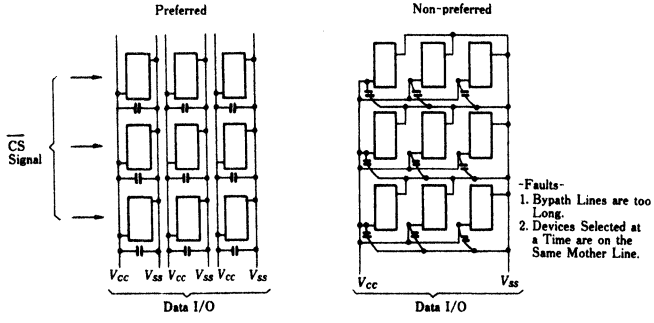


Figure 3-6. Examples of Power Supply Board Pattern

3.4 Address Input Waveform of Hi-BiCMOS Memory

Data stored in memory might be destructed in case that Address Input of the HM6716, HM6719, HM6787, HM6788 and HM6789 series becomes floating and sticks at and around threshold voltage. (e.g. CPU does Address Bus to off state in Figure 1.) Consequently, the following three methods are recommended so as to preserve malfunction of memory device.

A: Insert latch as shown in Figure 3-7 lest Address Input should become floating.

B: Put $\overline{CS}$ into High while Address Input becomes floating.
(Dotted line in Figure 3.8)

C: Insert Pull-up Resistor (R) to hold time constant of Rising Edge wave form of Address Input pin (tr = R × C) below 150 ns.

Stable operation can be assured if you have already adopted the above three method (A, B, C), while if you have any problem, please contact our sales offices.

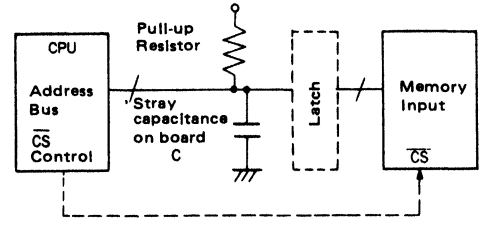


Figure 3-7

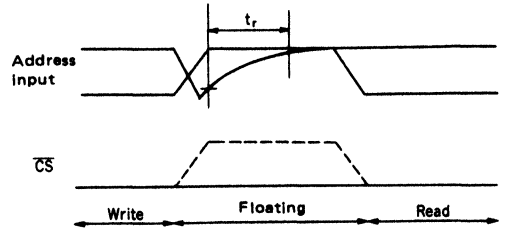


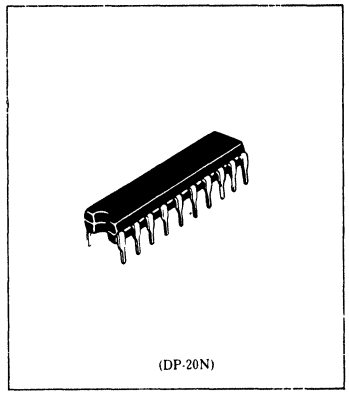
Figure 3-8

2

Section 2
MOS Static RAM

HITACHI®

4096-word x 4-bit High Speed CMOS Static RAM



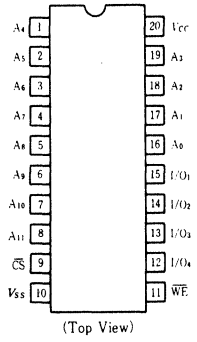
■FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35/45ns (max.)
- Low Power Standby: 100μW typ, 5μW typ (L-version)
  Active: 250mW typ.
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

■ORDERING INFORMATION

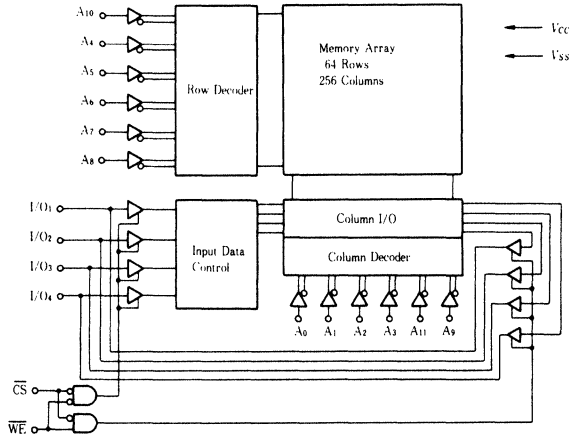
Type No.	Access Time	Package
HM6268P-25 HM6268P-35 HM6268P-45	25ns 35ns 45ns	300mil 20pin Plastic DIP
HM6268LP-25 HM6268LP-35 HM6268LP-45	25ns 35ns 45ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width≦10ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED OPERATING CONDITIONS (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width≦10ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C

Parameter	Symbol	Test Condition	Min.	Typ.*1	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, min. cycle	–	50*3	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ ≥ V_{CC} −0.2V,	–	0.02	2.0	mA
		0V ≤ V_{IN} ≤ 0.2V or V_{CC} − 0.2V ≤ V_{IN}	–	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −0.4mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. 40mA typ. for 45ns version.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

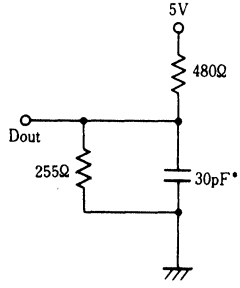
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	9	pF

Note: This parameter is sampled and not 100% tested.

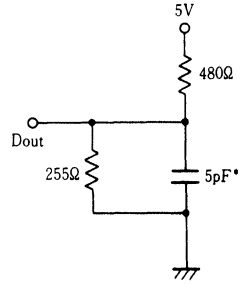
■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C, unless otherwise noted.)

- **AC Test Conditions**
  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



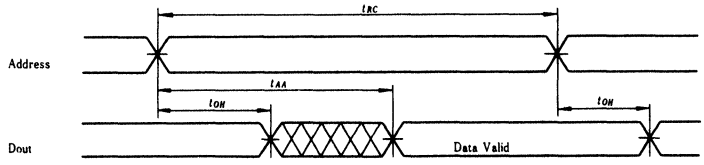
*Including scope and jig.

● READ CYCLE

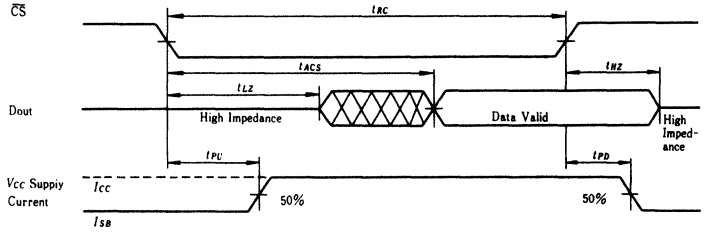
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*1	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	25	—	30	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1(1),(2)



● Timing Waveform of Read Cycle No. 2(1),(3)



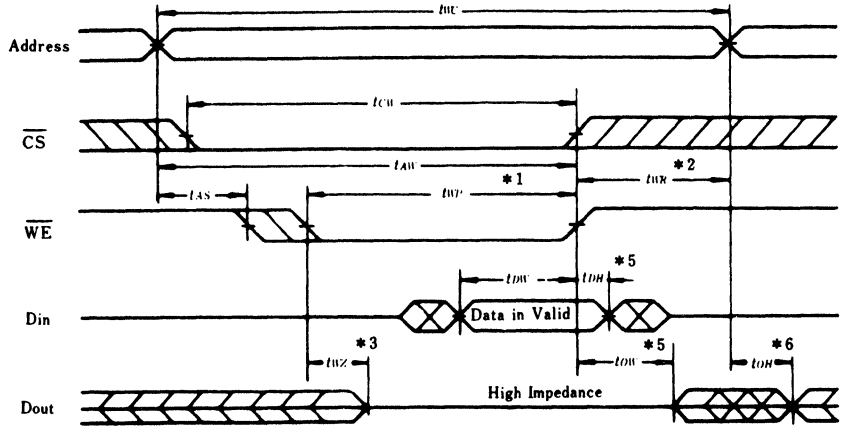
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

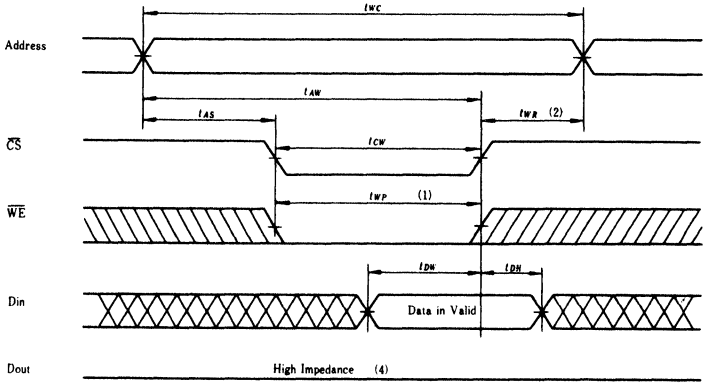
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	35	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}*1	0	8	0	10	0	15	ns
Output Active from End of Write	t_{OW}*1	0	—	0	—	0	—	ns

Note)*1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

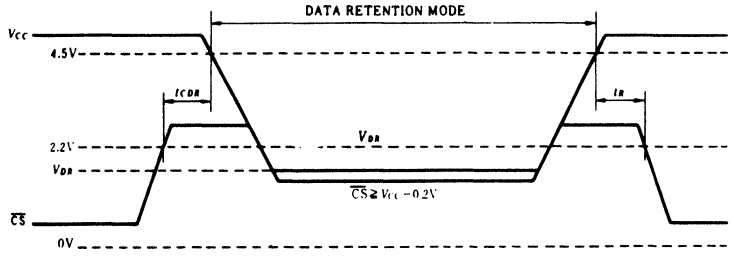
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leq Ta \leq 70°C$)

This characteristics guaranteed only for L-version.

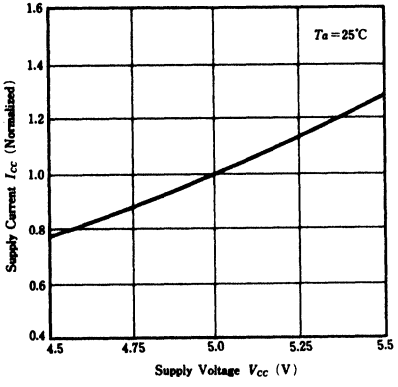
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{in} \geq V_{CC} - 0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. V_{CC} = 3.0V *3. V_{CC} = 2.0V

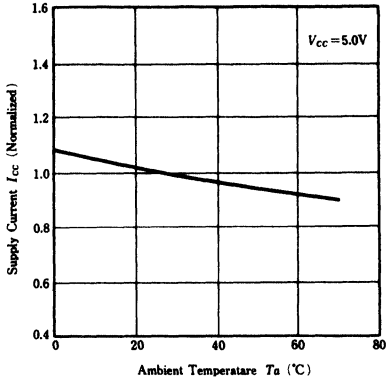
●LOW V_{CC} DATA RETENTION WAVEFORM



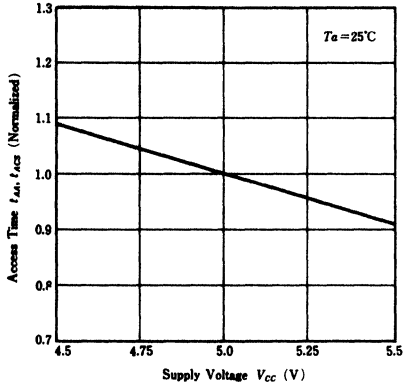
SUPPLY CURRENT VS. SUPPLY VOLTAGE



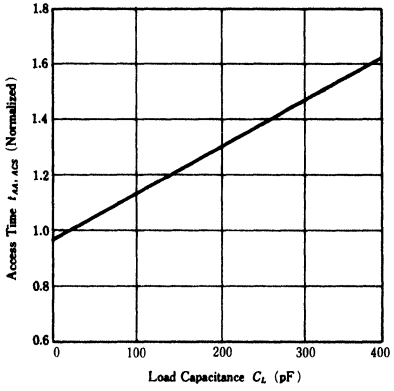
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



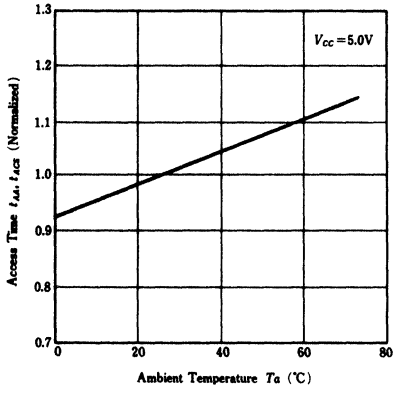
ACCESS TIME VS. SUPPLY VOLTAGE



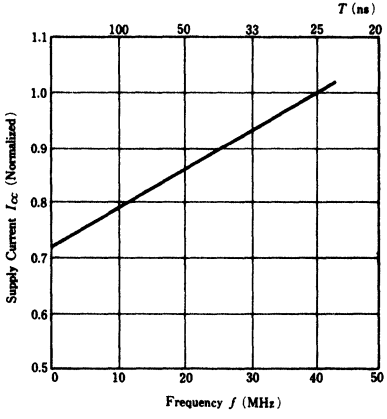
ACCESS TIME VS. LOAD CAPACITANCE



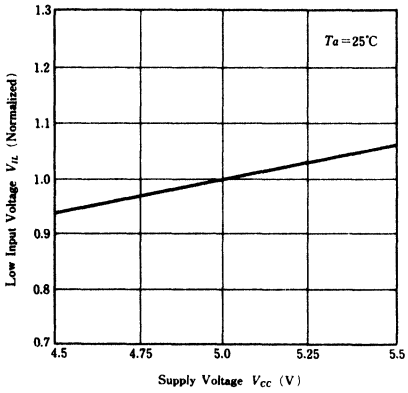
ACCESS TIME VS. AMBIENT TEMPERATURE



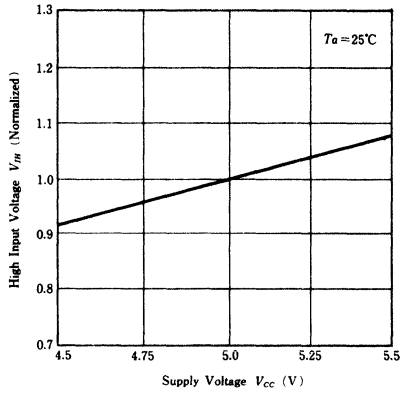
SUPPLY CURRENT VS. FREQUENCY



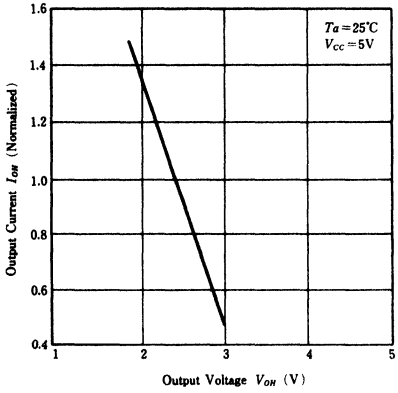
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



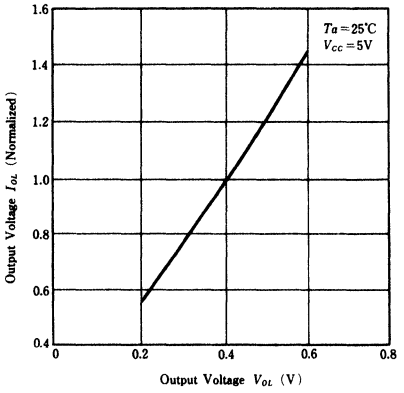
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



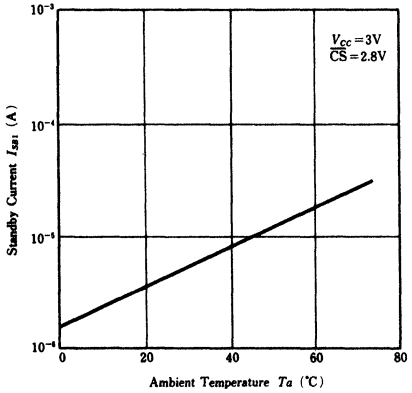
OUTPUT CURRENT VS. OUTPUT VOLTAGE



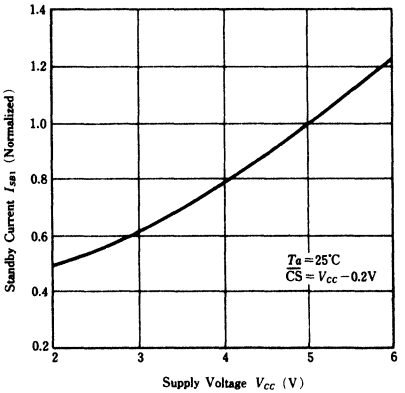
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



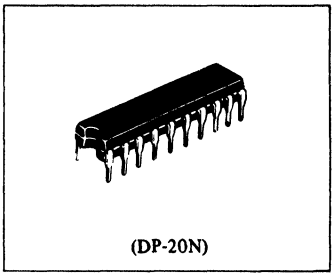
STANDBY CURRENT VS. SUPPLY VOLTAGE



16384-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 35/45/55ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.)/5μW (typ.) (L-version),
  Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

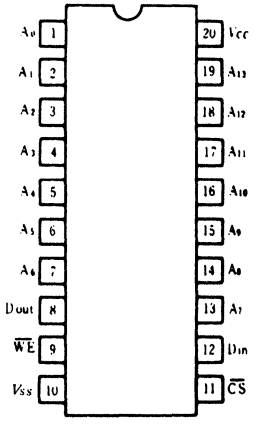


(DP-20N)

■ ORDERING INFORMATION

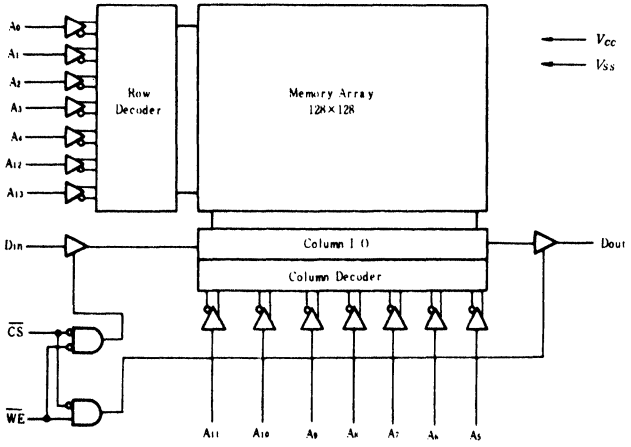
Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plactic DIP
HM6267P-45	45ns	
HM6267P-55	55ns	
HM6267LP-35	35ns	
HM6267LP-45	45ns	
HM6267LP-55	55ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*1	V_T	-0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

Notes) *1. With respect ot V_{SS}.
*2. -3.5V for pulse width ≦ 20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.5*1	–	0.8	V

Note) *1. -3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6267-35			HM6267-45/55			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT}=0mA, min. cycle	–	40	100	–	40	80	mA
Stand by Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, min cycle	–	10	20	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} – 0.2V, 0V ≦ V_{IN} ≦ 0.2V or V_{CC} – 0.2V ≦ V_{IN}	–	0.02	2	–	0.02	2	mA
			–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = -4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limts are at V_{CC} = 5V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	—	7	pF	V_{OUT}=0V

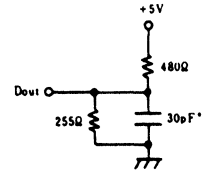
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

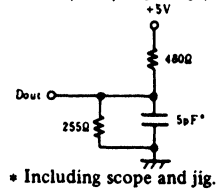
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

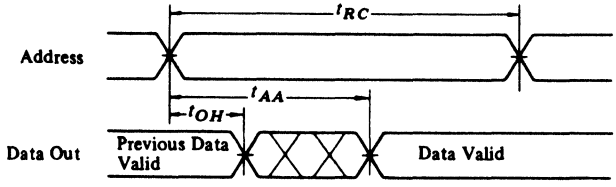


* Including scope and jig.

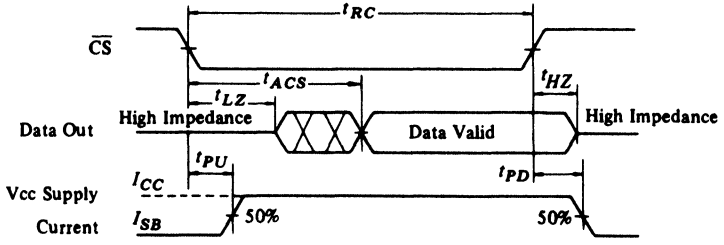
• Read Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	-	45	–	55	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	-	55	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2,3,7
Chip Deselectio to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2,3,7
Chip Selectio to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	–	30	ns	

• TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



• TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

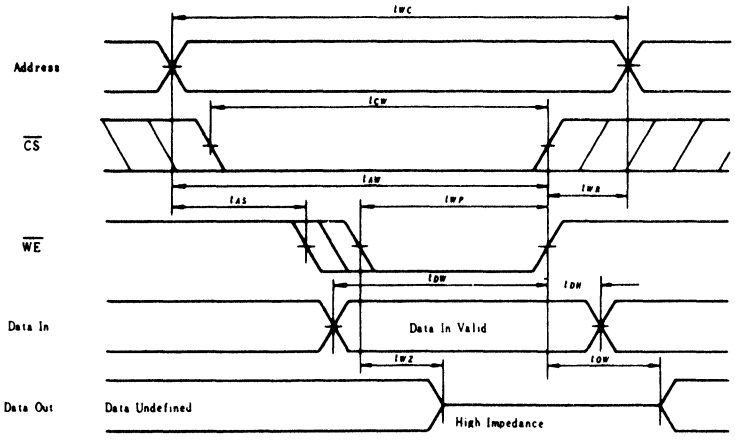


Notes) 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

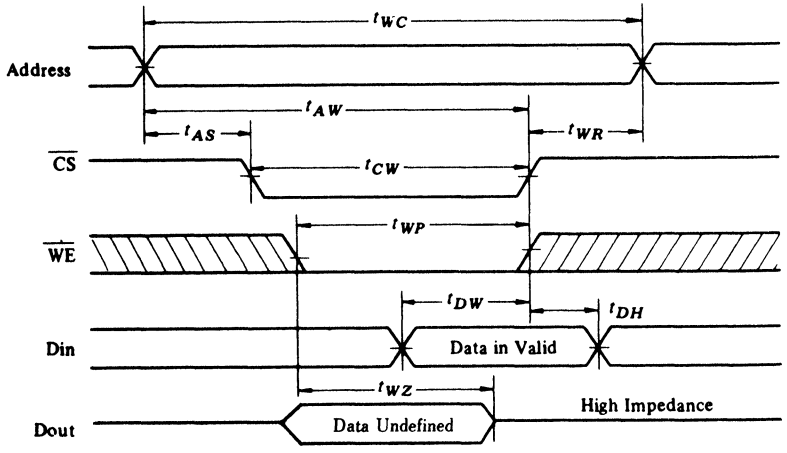
• Write Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	55	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	25	ns	3,4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3,4

- **TIMING WAVEFORM OF WRITE CYCLE NO. 1** ($\overline{WE}$ Controlled)



- **TIMING WAVEFORM OF WRITE CYCLE NO. 2** ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

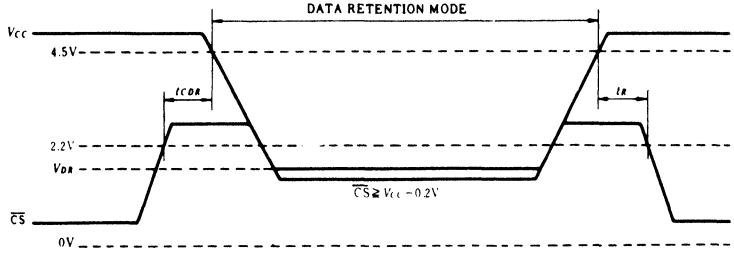
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics is guaranteed only for L-version.

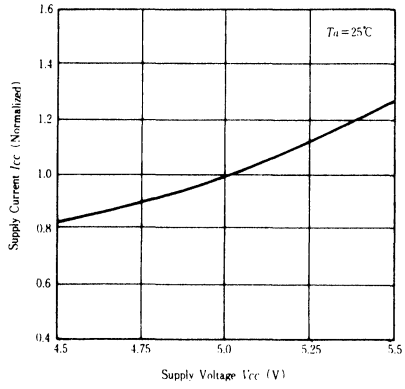
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	—	—	30*2 20*3	μA
Chip Deselect to Data Retention Time	t_{CDR}	see retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time.
*2. $V_{CC} = 3.0V$
*3. $V_{CC} = 2.0V$

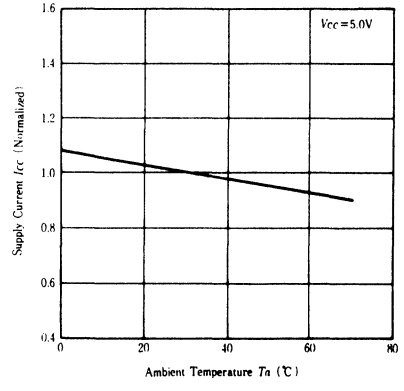
●LOW V_{CC} DATA RETENTION WAVEFORM



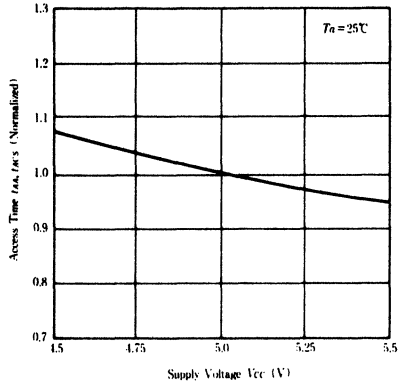
SUPPLY CURRENT VS. SUPPLY VOLTAGE



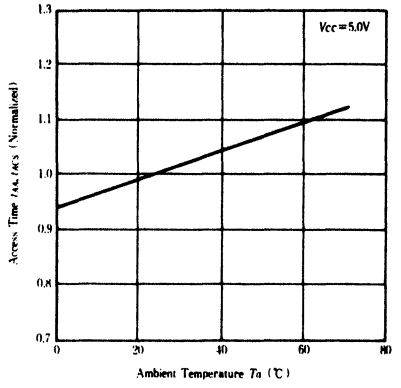
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



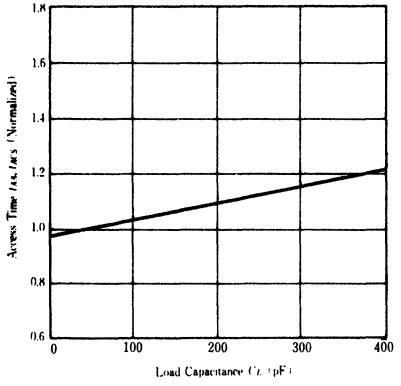
ACCESS TIME VS. SUPPLY VOLTAGE



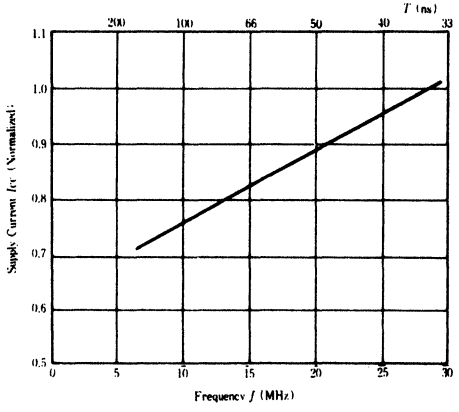
ACCESS TIME VS. AMBIENT TEMPERATURE



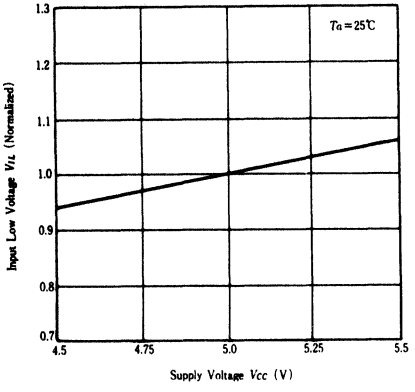
ACCESS TIME VS. LOAD CAPACITANCE



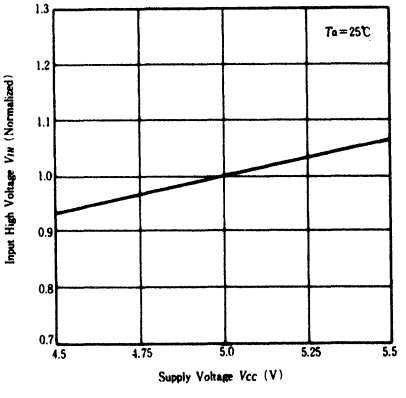
SUPPLY CURRENT VS. FREQUENCY



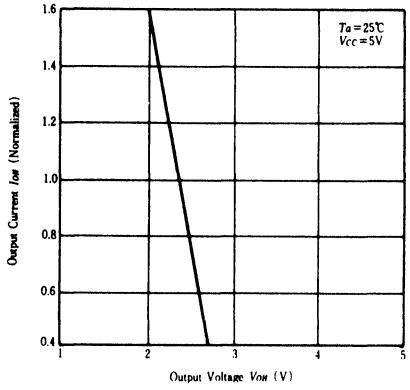
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



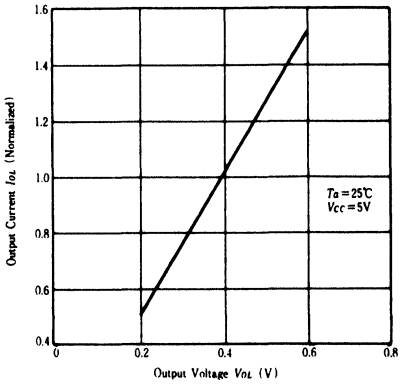
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



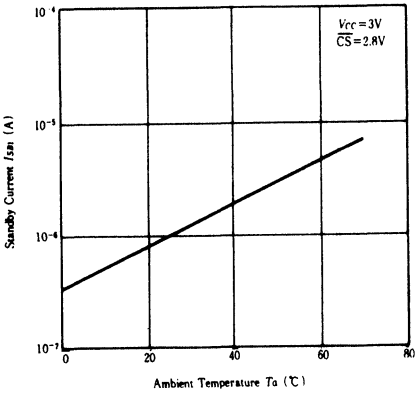
OUTPUT CURRENT VS. OUTPUT VOLTAGE



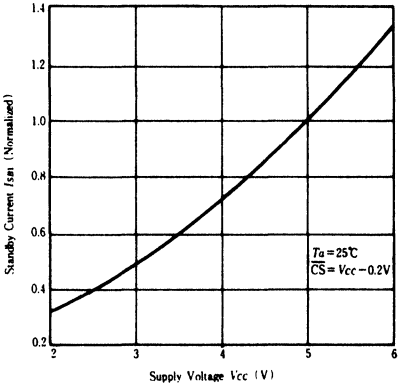
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



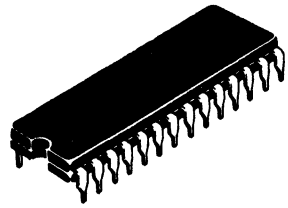
HM6264A Series

8192-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

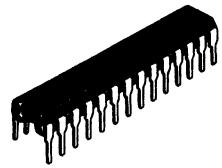
- Low Power Standby — Standby: 0.1mW (typ.) 10μW (typ.) L-/LL-version
- Low Power Operation — Operating: 15mW/MHz (typ.)
- Fast access Time — 100ns/120ns/150ns (max.)
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- . Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/LL-version)

HM6264AP Series



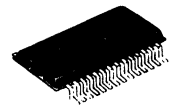
(DP-28)

HM6264ASP Series



(DP-28N)

HM6264AFP Series



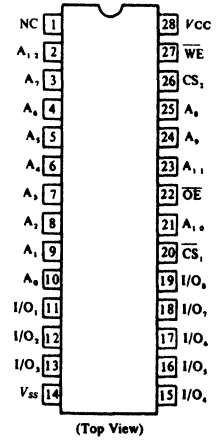
(FP-28D/DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6264AP-10	100ns	600 mil 28 pin Plastic DIP
HM6264AP-12	120ns	
HM6264AP-15	150ns	
HM6264ALP-10	100ns	
HM6264ALP-12	120ns	
HM6264ALP-15	150ns	
HM6264ALP-10L	100ns	
HM6264ALP-12L	120ns	
HM6264ALP-15L	150ns	
HM6264ASP-10	100ns	300 mil 28 pin Plastic DIP
HM6264ASP-12	120ns	
HM6264ASP-15	150ns	
HM6264ALSP-10	100ns	
HM6264ALSP-12	120ns	
HM6264ALSP-15	150ns	
HM6264ALSP-10L	100ns	
HM6264ALSP-12L	120ns	
HM6264ALSP-15L	150ns	
HM6264AFP-10	100ns	28 pin Plastic SOP (Note)
HM6264AFP-12	120ns	
HM6264AFP-15	150ns	
HM6264ALFP-10	100ns	
HM6264ALFP-12	120ns	
HM6264ALFP-15	150ns	
HM6264ALFP-10L	100ns	
HM6264ALFP-12L	120ns	
HM6264ALFP-15L	150ns	

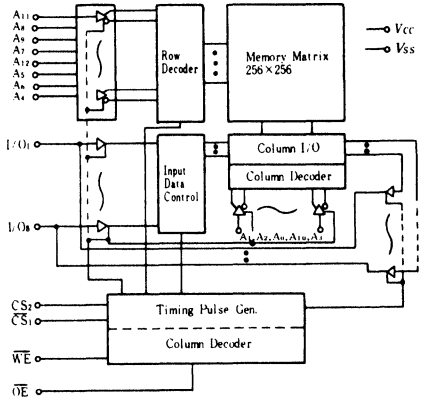
Note) T is added to the end of the type no. for a SOP of 3.00 mm (max.) thickness.

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage*1	V_T	−0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

Notes) *1. With respect to V_{SS}.
*2. −3.0V for pulse width ≦ 50ns

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB},I_{SB1}	
X	X	L	X		High Z	I_{SB},I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read Cycle
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	--	6.0	V
	V_{IL}	−0.3*1	--	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{in}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, $I_{I/O}$=0mA	–	7	15	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1}=V_{IL}$, CS2=V_{IH} $I_{I/O}$=0mA	–	30	45*5	mA
				30	55*6	
	I_{CC2}	Cycle time = 1μs, duty = 100%, $I_{I/O}$ = 0mA, $\overline{CS1} \leqq 0.2V$, CS2 $\geqq V_{CC}-0.2V$ $V_{IH} \geqq V_{CC}-0.2V$, $V_{IL} \leqq 0.2V$	–	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}	–	1	3	mA
	I_{SB1}*2	$\overline{CS1} \geqq V_{CC}-0.2V$, CS2 $\geqq V_{CC}-0.2V$ or 0V $\leqq$ OS2 $\leqq$ 0.2V, 0V $\leqq V_{in}$	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. V_{IL} min=–0.3V
*3. This characteristics is guaranteed only for L-version.
*4. This characteristics is guaranteed only for LL-version.
*5. For 120ns/150ns version.
*6. For 100ns version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• **AC TEST CONDITIONS**

Input Pulse Levels: 0.8V/2.4V
Input Rise and Fall Time: 10ns
Input Timing Reference Level: 1.5V
Output Timing Reference Level: 0.8V/2.0V
Output Timing Reference Level: HM6264A-10 1.5V
HM6264A-12/15 0.8V/2.0V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

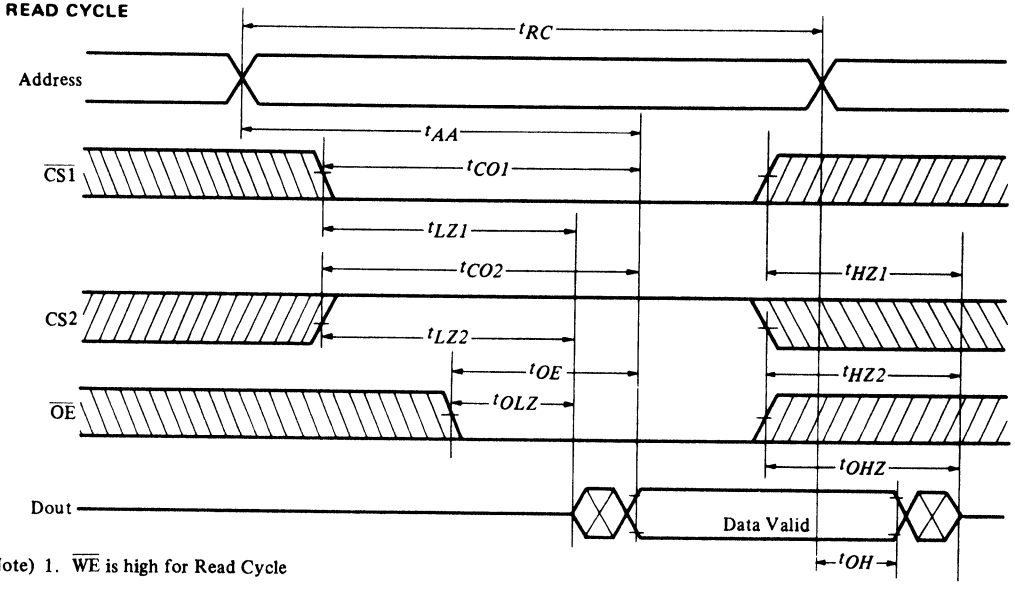
• READ CYCLE

Item		Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	10	–	ns

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from d device to device.

2

• READ CYCLE

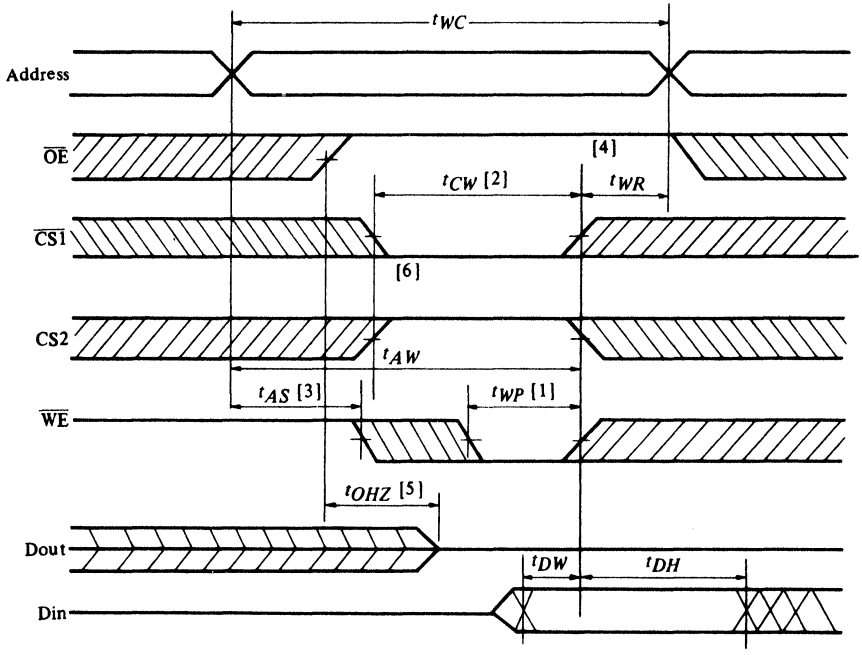


Note) 1. $\overline{WE}$ is high for Read Cycle

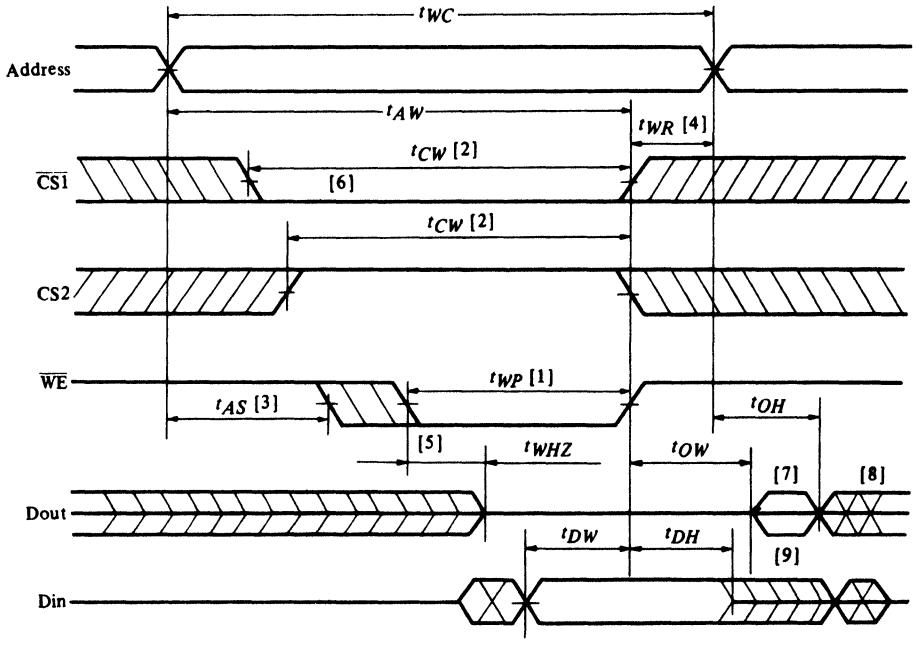
• WRITE CYCLE

Item	Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	80	–	85	–	100	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width	t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Enable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

• WRITE CYCLE (1) ($\overline{OE}$ clock)



• WRITE CYCLE (2) ($\overline{OE}$ Low Fix)



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

3) t_{AS} is measured from the address valid to the beginning of write.

4) t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

7) Dout is the same phase of the latest written data in this write cycle.

8) Dout is the read data of next address.

9) If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

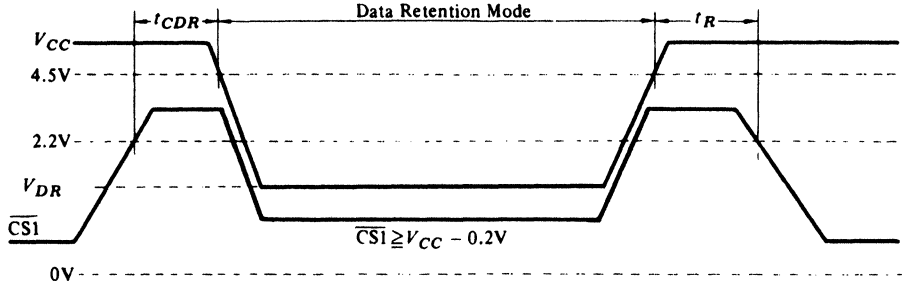
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L/LL-version.

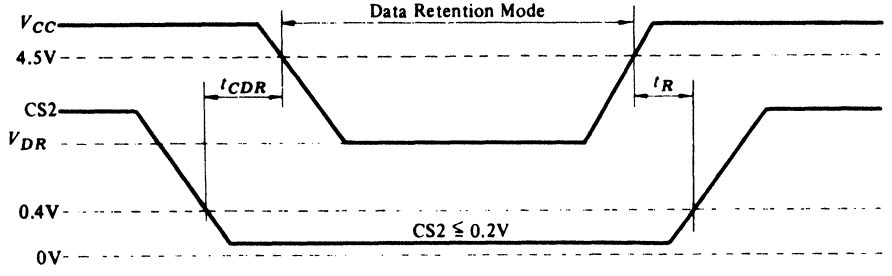
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$	2.0	–	–	V
Data RetentionCurrent	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $0V \leq CS2 \leq 0.2V, 0V \leq V_{in}$	–	1*1	50*1	μA
			–	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*3	–	–	ns

Notes) *1. V_{IL} min = −0.3V, 20μA max at T_a=0 to 40°C, This characteristics is guaranteed only for L-version.
*2. V_{IL} min = −0.3V, 10μA max at T_a = 0 to 40°C, This characteristics is guarnteed only for LL-version.
*3. t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

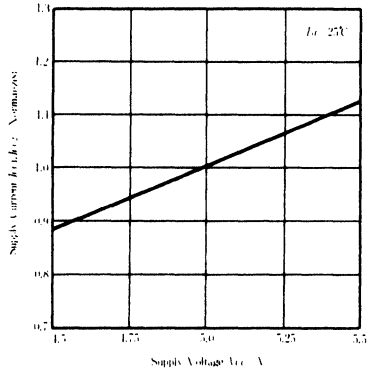


• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)

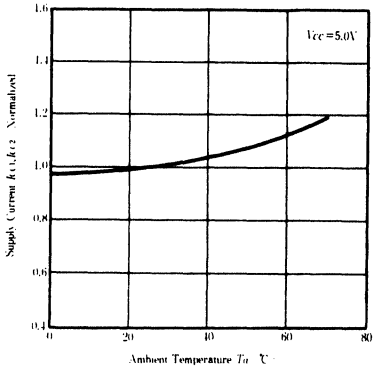


Note) In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

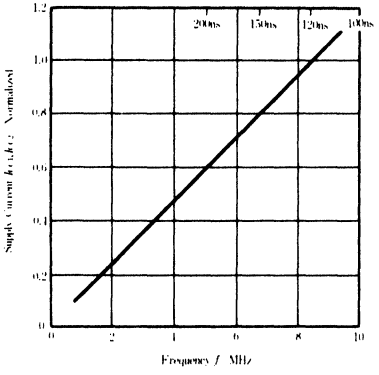
SUPPLY CURRENT VS. SUPPLY VOLTAGE



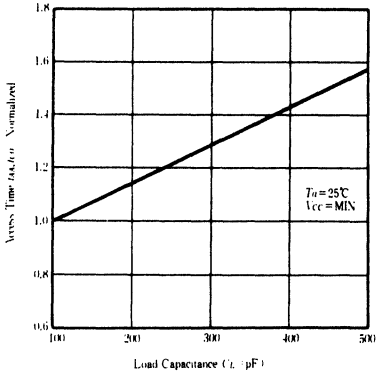
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



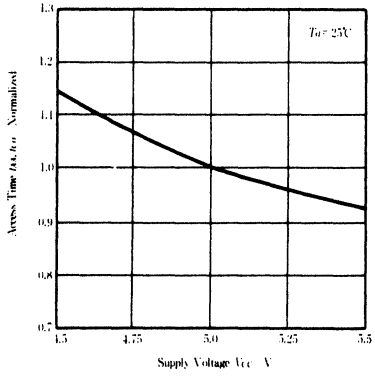
SUPPLY CURRENT VS. FREQUENCY



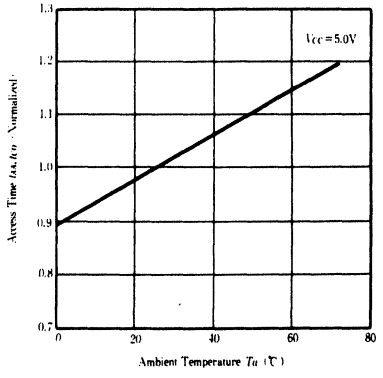
ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. SUPPLY VOLTAGE

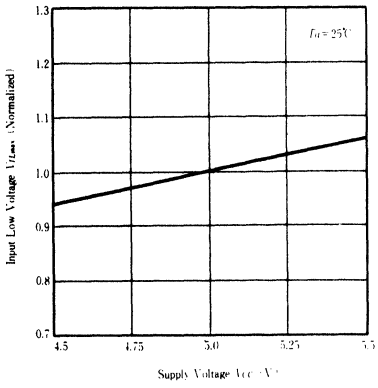


ACCESS TIME VS. AMBIENT TEMPERATURE

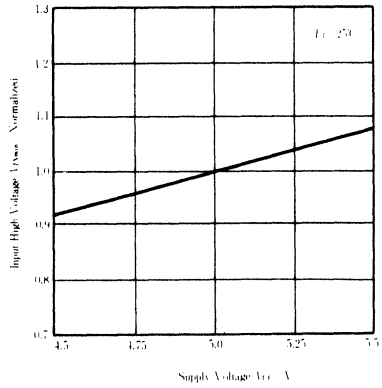


2

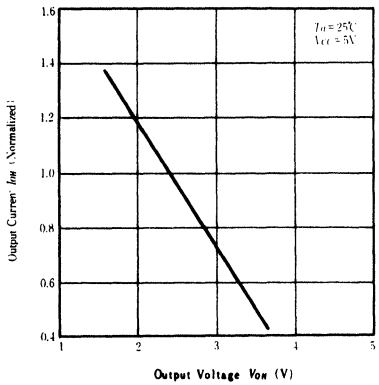
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



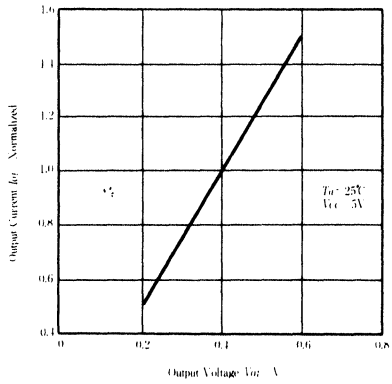
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



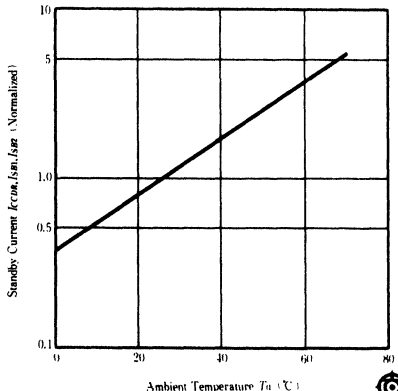
OUTPUT CURRENT VS. OUTPUT VOLTAGE



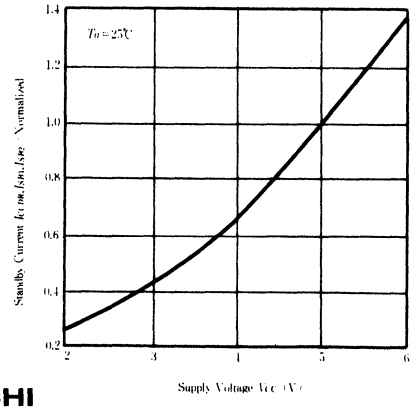
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



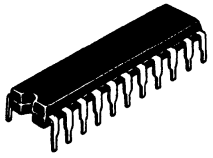
HM6288 Series

16384-word×4-bit High Speed CMOS Static RAM

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6288, packaged in a 300 mil plastic DIP and SOJ, is available for high density mounting. Low power version retains the data with battery back up.



(DP-22NB)

(CP-24D)

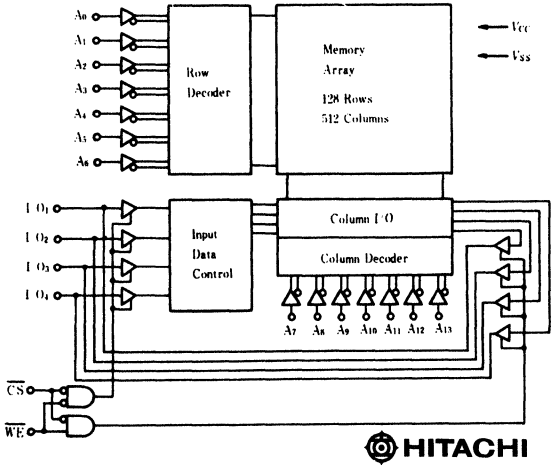
■FEATURES

- Single 5V Supply and High Density Plastic Package.
- High Speed: Fast Access Time 25/35/45 ns (max.)
- Low Power dissipation
  - Active mode 300mW (typ.)
  - Standby mode 100μW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

■ ORDERING INFORMATION

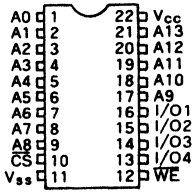
Type No.	Access Time	Package
HM6288P-25 HM6288P-35	25ns 35ns	300 mil 22-pin Plastic DIP (DP-22NB)
HM6288LP-25 HM6288LP-35	25ns 35ns	
HM6288JP-25 HM6288JP-35	25ns 35ns	300 mil 24-pin SOJ (CP-24D)
HM6288LJP-25 HM6288LJP-35	25ns 35ns	

■BLOCK DIAGRAM



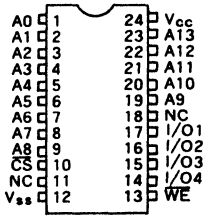
■PIN ARRANGEMENT

- HM6288P Series



(Top View)

- HM6288JP Series



(Top View)

■Pin Description

Pin Name	Function
A0 - A13	Address
I/O1–I/O4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

HITACHI

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5^{*1} to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note: *1. V_T min. = −2.0V for pulse width ≦ 10ns

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read'Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5^{*1}	–	0.8	V

Note: *1. V_{IL} min. = −2.0V for pulse width ≦ 10ns

■DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=MAX. V_{IN}=V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, min. cycle	–	60	120	mA
Standby V_{CC} Current	I_{SB}	$\overline{CS}$=V_{IH}, min. cycle	–	15	30	mA
Standby V_{CC} Current 1	I_{SB1}*2	$\overline{CS}$ ≧ V_{CC}−0.2V	–	0.02	2.0	mA
	I_{SB1}*3	0V ≦ V_{IN} ≦ 0.2V or V_{CC}−0.2V ≦ V_{IN}	–	0.02	0.1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Notes: *1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
*2. P version
*3. LP version

■CAPACITANCE (Ta=25°C, f=1.0MHz)

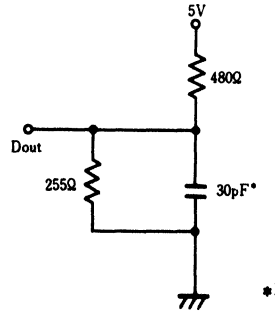
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note: This parameter is sampled and not 100% tested

■AC CHARACTERISTICS

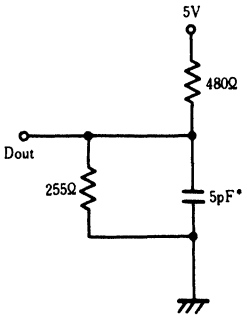
- AC Test Conditions

Input pulse levels: 0V to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure



Output Load (A)

*Including scope & jig.



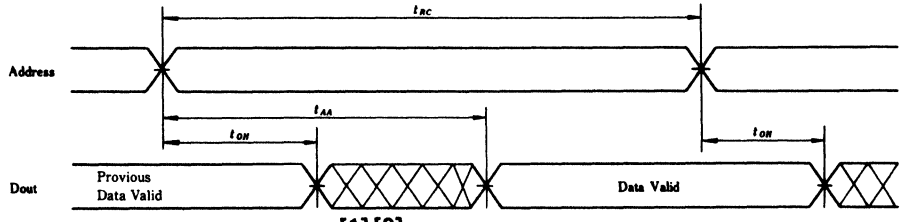
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

■ READ CYCLE

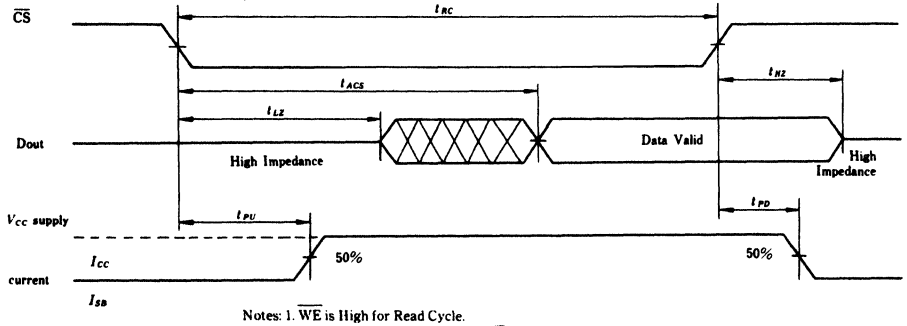
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	ns
Address Access Time	t_{AA}	–	25	–	35	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	ns
Output Hold from Address Change	t_{OH}	3	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Seselection to Power Down Time	t_{PD}	–	25	–	30	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No.1 [1] [2]



● Timing Waveform of Read Cycle No.2 [1] [3]



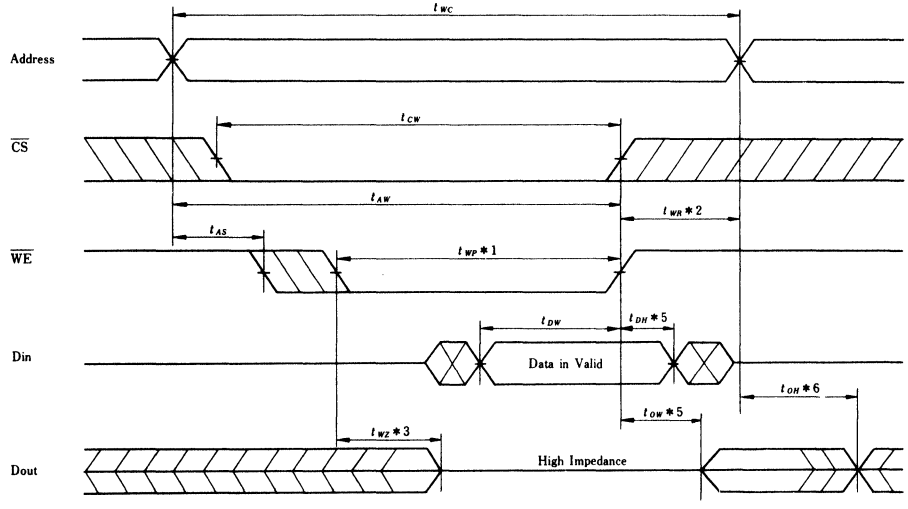
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

■ WRITE CYCLE

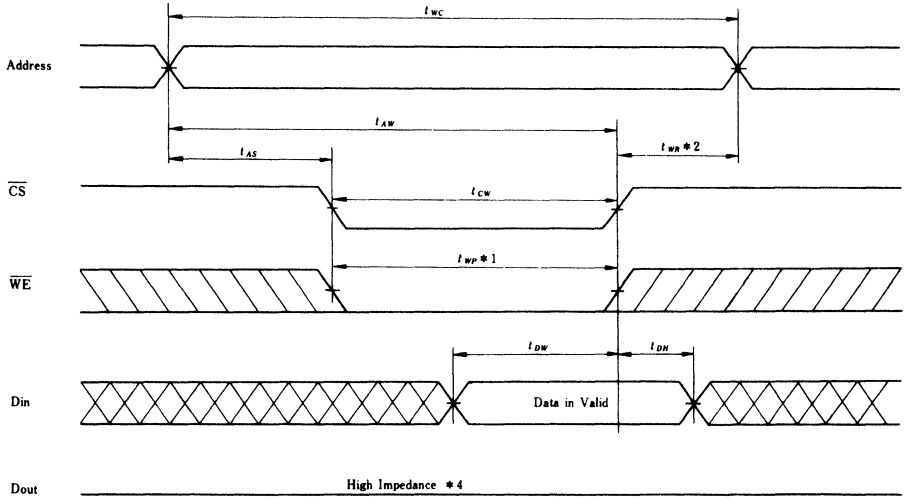
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Date Valid to End of Write	t_{DW}	12	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WZ}*	0	8	0	10	ns
Output Active from End of Write	t_{OW}*	5	–	5	–	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 ($\overline{WE}$ Controlled)



● Timing Waveform of Write Cycle No.2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

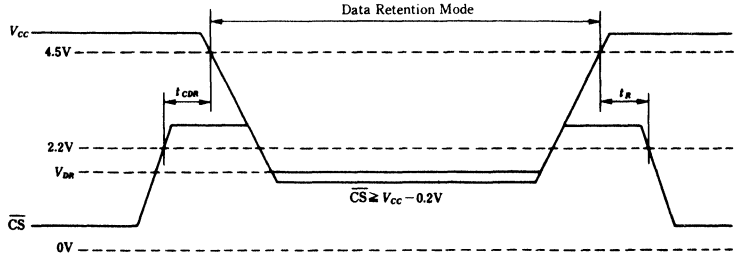
● Low *Vcc* Data Retention Characteristics (Ta = 0 to +70°C)

(This Characteristics is guaranteed only for L-version.)

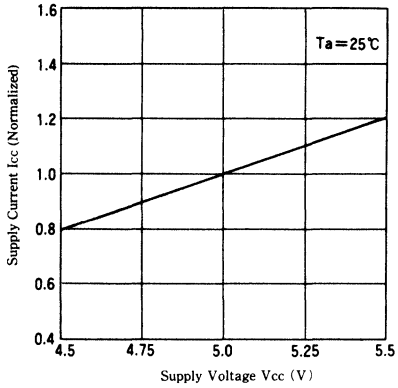
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Data retention current	I_{CCDR}	–	–	50[2] 35[3]	μA	
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[1]	–	–	ns	

NOTE : 1. t_{RC} = Read cycle time
2. V_{CC} = 3.0V
3. V_{CC} = 2.0V

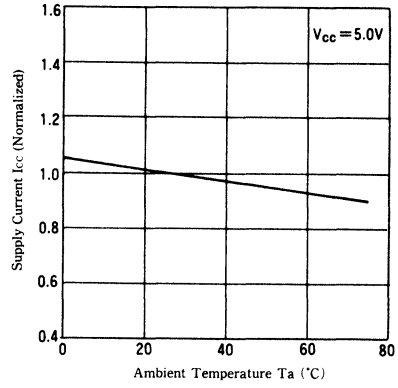
Low *Vcc* Data Retention Waveform



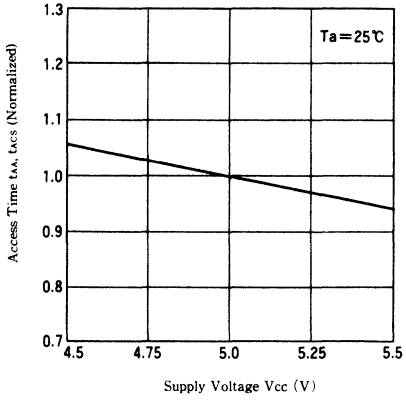
SUPPLY CURRENT VS. SUPPLY VOLTAGE



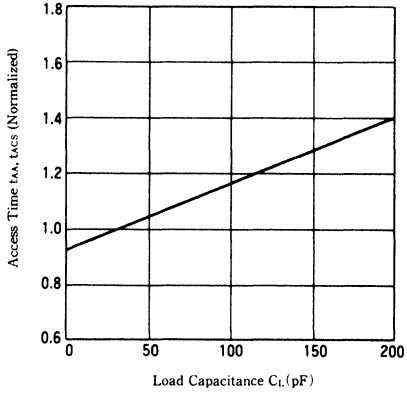
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



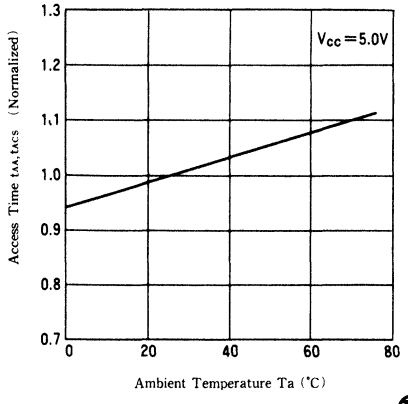
ACCESS TIME VS. SUPPLY VOLTAGE



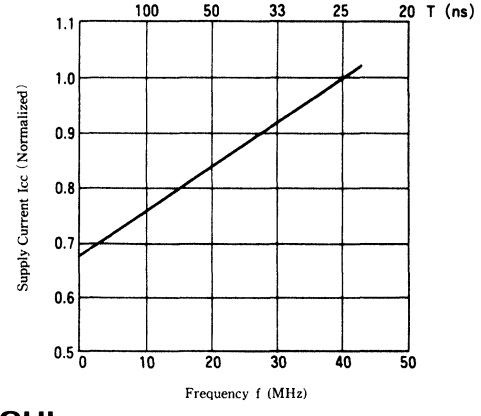
ACCESS TIME VS. LOAD CAPACITANCE



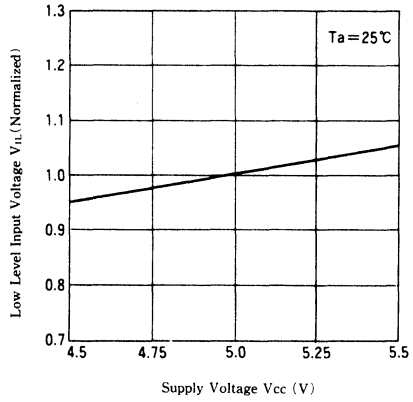
ACCESS TIME VS. AMBIENT TEMPERATURE



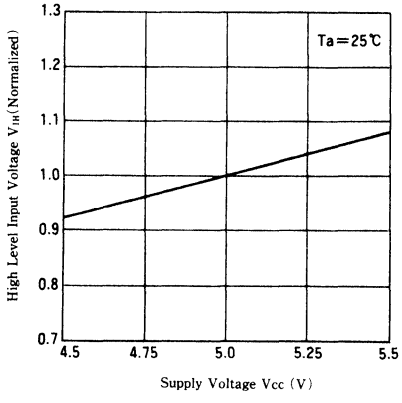
SUPPLY CURRENT VS. FREQUENCY



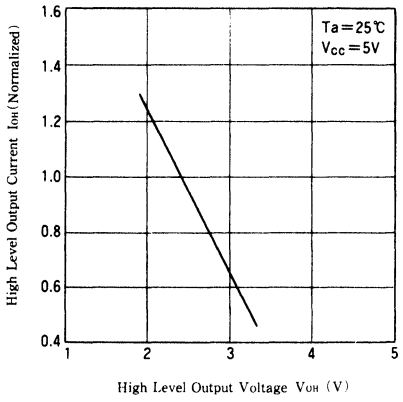
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



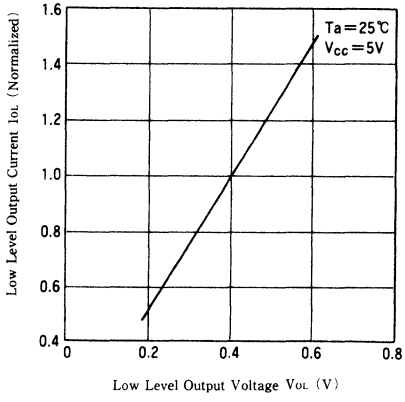
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



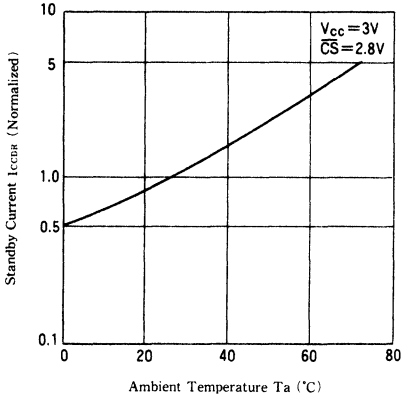
OUTPUT CURRENT VS. OUTPUT VOLTAGE(1)



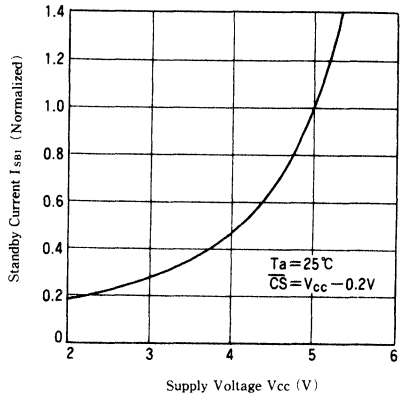
OUTPUT CURRENT VS. OUTPUT VOLTAGE(2)



STANDBY CURRENT VS. AMBIENT TEMPERATURE

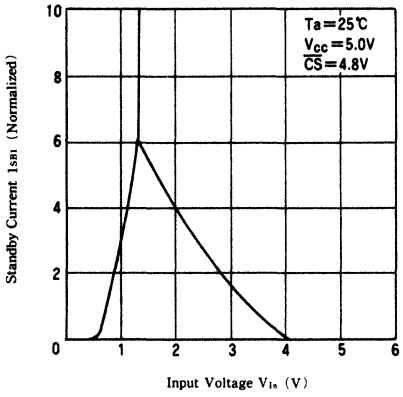


STANDBY CURRENT VS. SUPPLY VOLTAGE



2

STANDBY CURRENT VS. INPUT VOLTAGE



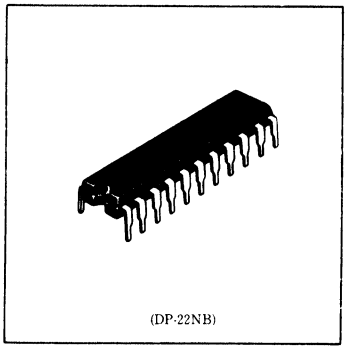
HM6788 Series — Maintenance Only

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

Refer to HM6788HA Series

■FEATURES

- Super Fast Access Time : 25/30ns (max.)
- Low power Operation
  Operating: 230mW (typ), Standby: 10mW (typ)
- +5V Single Supply
- Completely Static Memory —
  No Clock or Timing Strobe required
- Balanced Read and Write Cycle Time
- Fully TTL compatible Input and Output

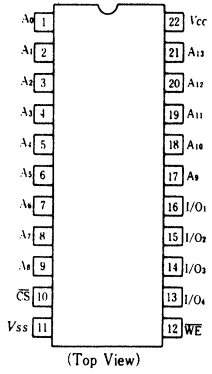


(DP-22NB)

■ ORDERING INFORMATION

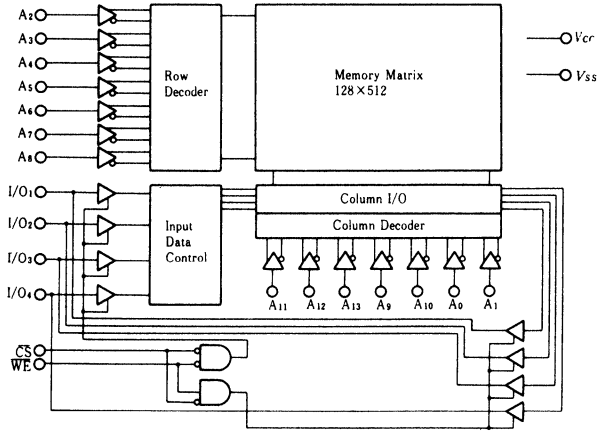
Type No.	Access Time	Package
HM6788P-25	25ns	300 mil 22 pin Plastic DIP
HM6788P-30	30ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2)

×: H or L

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 20ns pulse width.

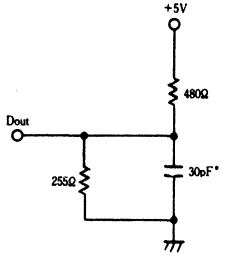
■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	80	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	–	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.5	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

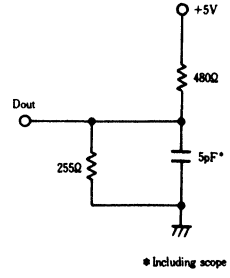
■AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall time: 4ns
  Input and Output reference levels: 1.5V
  Output Load: See Figure



Output Load A



* Including scope and jig.

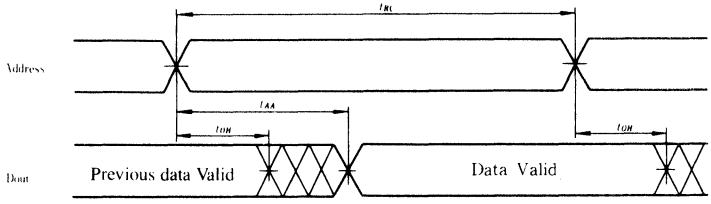
Output Load B
(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW})

● READ CYCLE

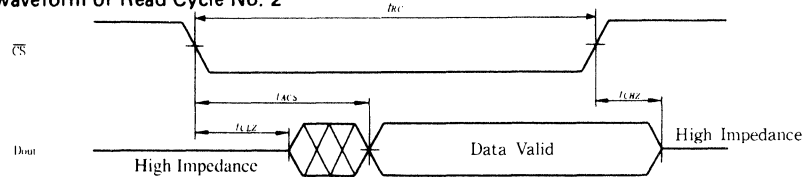
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Address Access Time	t_{AA}	—	25	—	30	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	ns
Chip Selection to Output in Low Z	t_{CLZ} *2	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ} *2	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time*1	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time*1	t_{PD}	—	20	—	30	ns
Input Voltage Rise/Fall Time*3	t_r	—	150	—	150	ns

Notes) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV form steady state voltage with Load (B). This parameter is sampled and not 100% tested
*3. If t_r becomes more than 150ns, there is possibility of function fail.
please contact your nearest Hitachi Sales Dept. regarding specification.

● Timing waveform of Read Cycle No. 1 *1,*2



● Timing waveform of Read Cycle No. 2 *1,*3



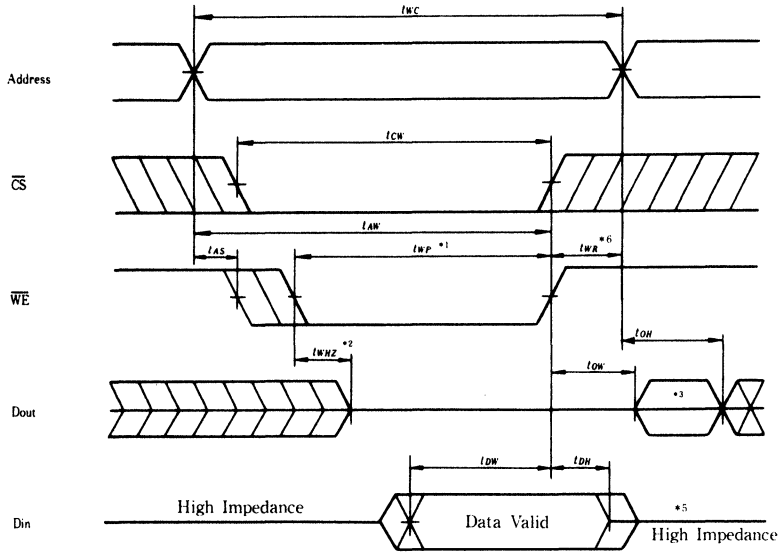
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

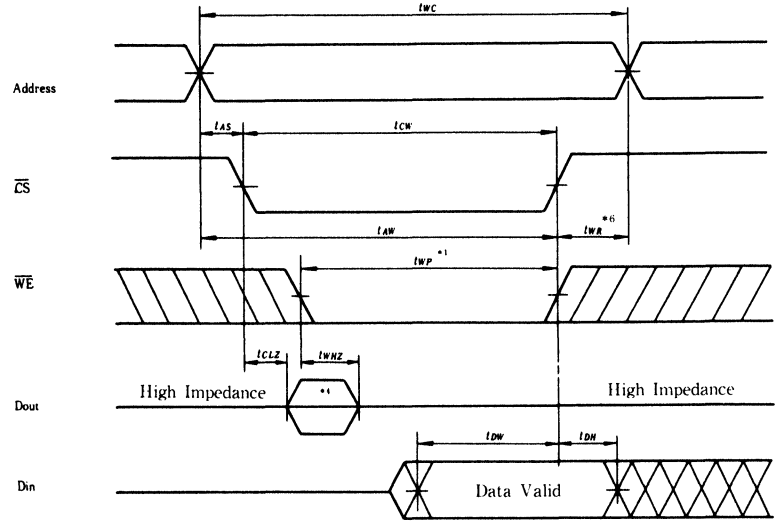
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	20	—	25	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	20	—	25	—	ns
Write Pulse Width	t_{WP}	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High Z	t_{WHZ} *1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	—	15	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Output Active from End of Write	t_{OW} *1	0	—	0	—	ns

*1. Transition is measured ±200mV from steady state voltage with Lood(B).
This parameter is sampled and not 100% tested.

- Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Dout is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
*6. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	8.0	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

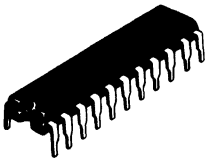
HM6788H Series — Maintenance Only

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

Refer to HM6788HA Series

Features

- Super Fast Access Time : 15/20ns (max.)
- Low power Operation
  Operating: 280mW (typ)
- +5V Single Supply
- Completely Static Memory –
  No Clock or Timing Strobe required
- Equal Access and Cycle Times
- Fully TTL compatible Input and Output

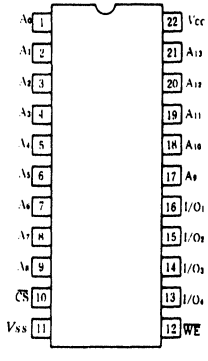


(DP-22NB)

Ordering Information

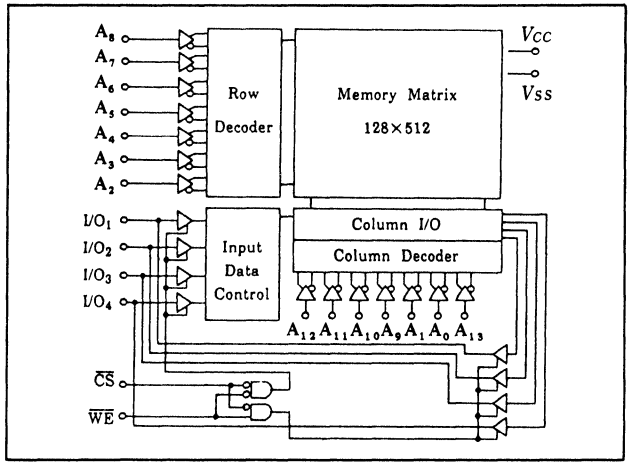
Type No.	Access Time	Package
HM6788HP-15	15ns	300 mil 22 pin Plastic DIP
HM6788HP-20	20ns	

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1), (2)

×: H or L

Recommended DC Operating Conditions ($0°C \leq Ta \leq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 10ns pulse width.

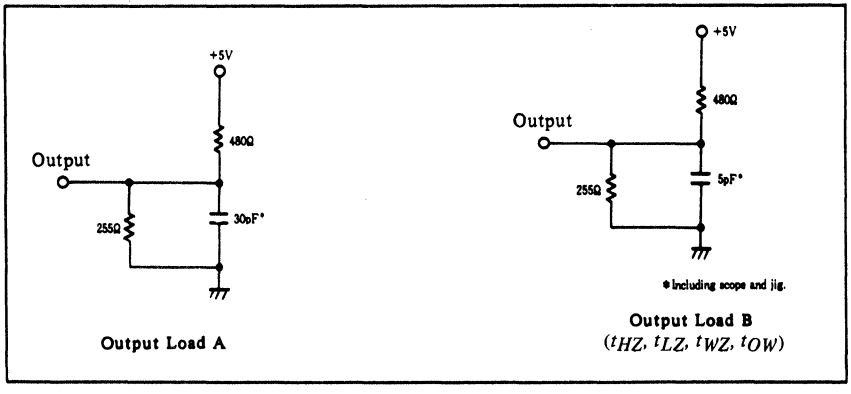
DC and Operating Characteristics ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	10	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}=0mA$	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	–	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

AC Characteristics (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall time: 4ns
  Input and Output reference levels: 1.5V
  Output Load: See Figure

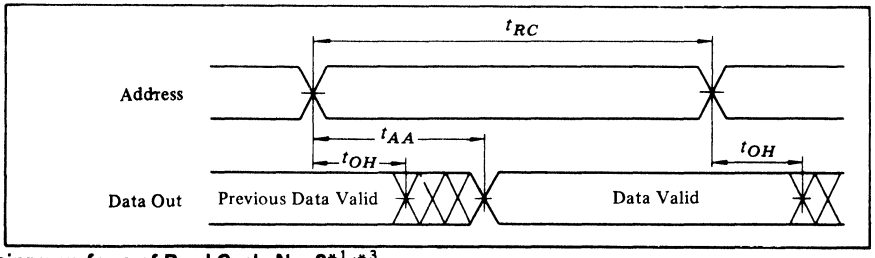


Read Cycle

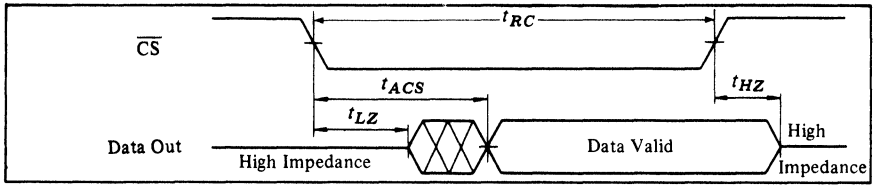
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	

Note) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

- **Timing waveform of Read Cycle No. 1*1,*2**



- **Timing waveform of Read Cycle No. 2*1,*3**



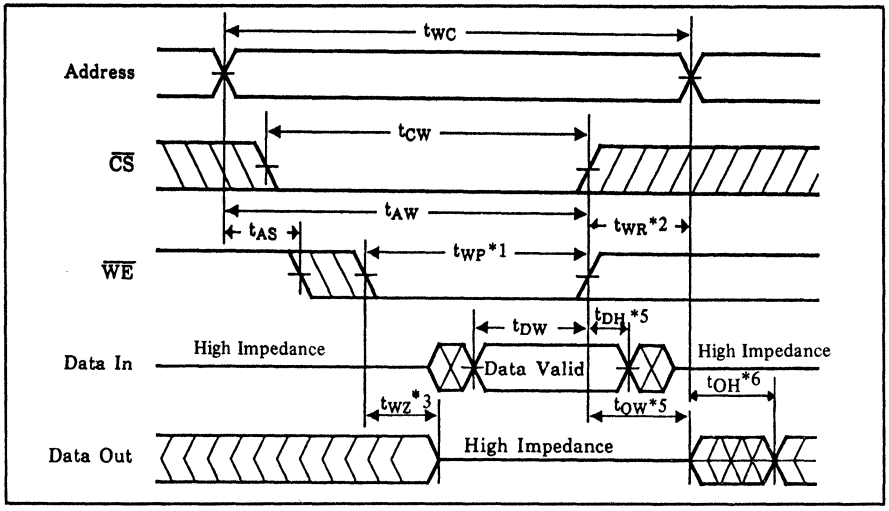
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

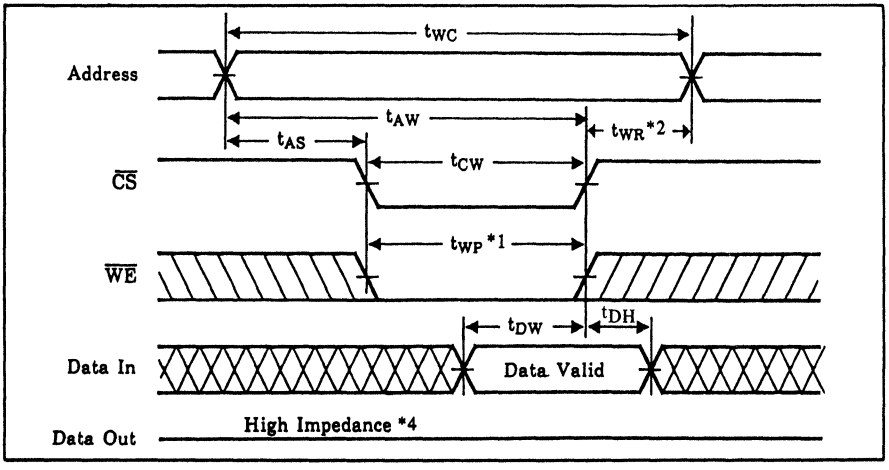
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	1	–	1	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Data Valid to End of Write	t_{DW}	9	–	10	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

- **Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)**



- **Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)**



Note)*1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

*6. Data Out is the same phase of write data of this write cycle.

Capacitance (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	$V_{I/O}$=0V

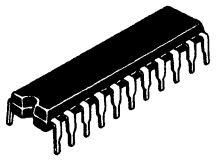
Note) This parameter is sampled and not 100% tested.

HM6788HA Series — Preliminary

16384-Word × 4-Bit High Speed Static RAM

■ FEATURES

- Super Fast
  Access Time. . . . . .12/15/20ns (max.)
- +5V Single Supply
- Low Power Dissipation
  (DC) Operating . . . . . .300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible—All Inputs and Outputs

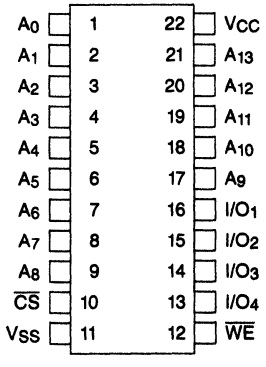


(DP-22NB)

■ ORDERING INFORMATION

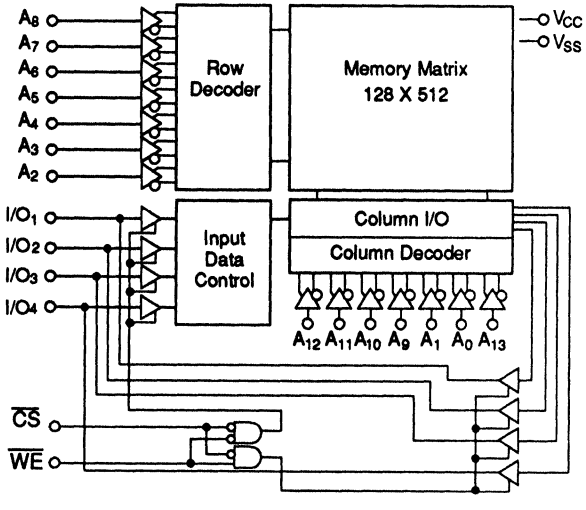
Type No.	Access Time	Package
HM6788HAP-12	12ns	300 mil 22 pin
HM6788HAP-15	15ns	Plastic DIP
HM6788HAP-20	20ns	(DP-22NB)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

*Pulse width ≤ 10ns, DC: -0.5V

■ TRUTH TABLE

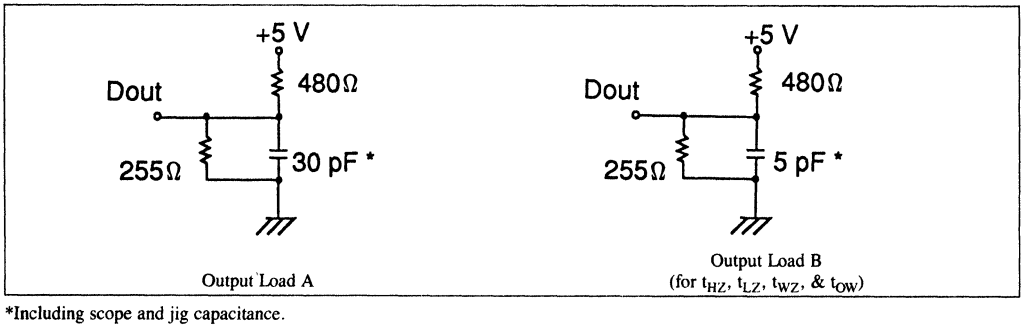
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1), (2)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$, $V_{SS} = 0V$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O}$, = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle Duty: 100% $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	—	30	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Load: See Figure
- Input Rise and Fall Times: 4ns
- Output Reference Levels: 1.5V



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ}, & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6788HA-12		HM6788HA-15		HM6788HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	5	—	5	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	6	0	8	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6788HA-12		HM6788HA-15		HM6788HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	2
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	6	—	7	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	3, 4

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

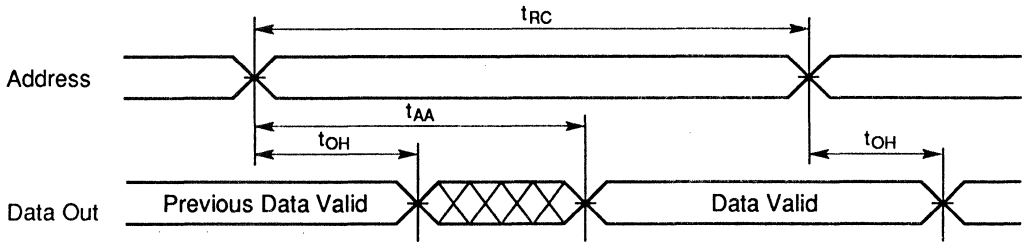
2. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

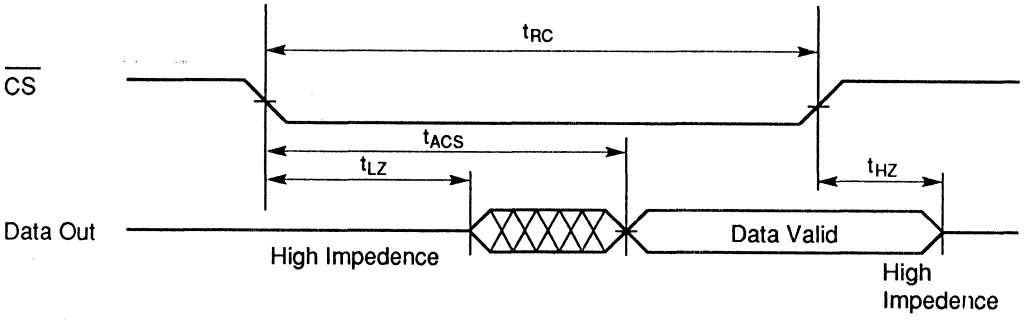
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1) (1) (2)

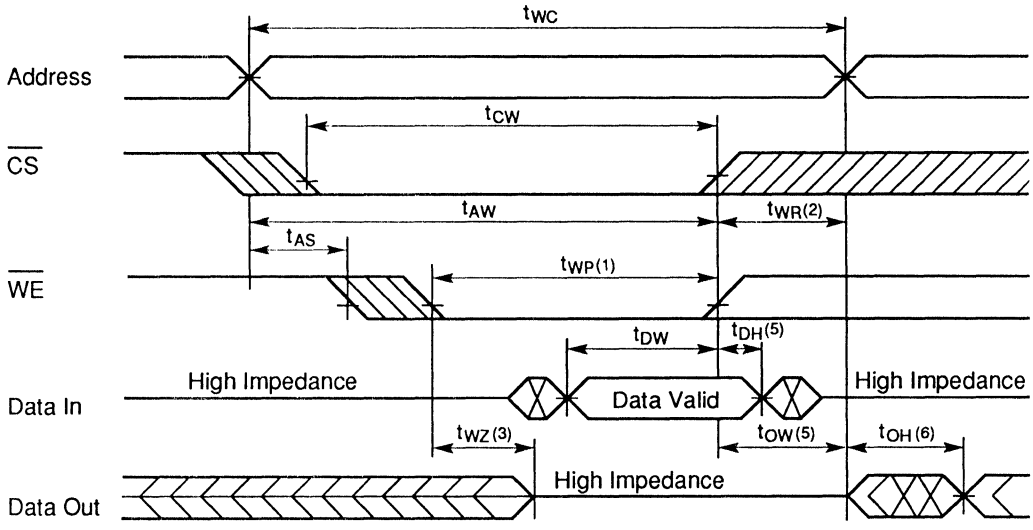


• Read Cycle (2) (1) (3)

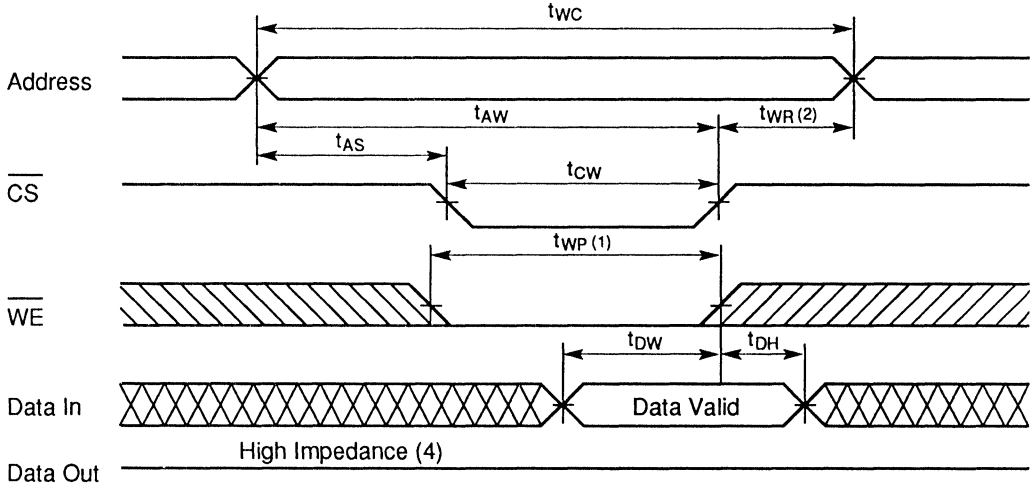


NOTES: 1. $\overline{WE}$ is High for READ cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle.

HM6289 Series

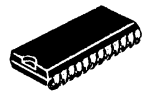
16384-Word × 4-Bit High Speed CMOS Static RAM (with $\overline{OE}$)

The Hitachi HM6289 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. Low power version retains the data with battery back up.

HM6289 Series

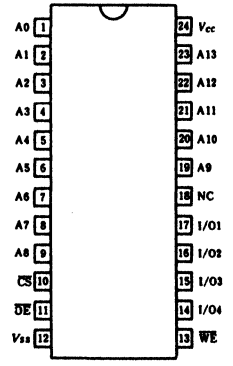


(CP-24D)

Features

- High speed
  - Access time: 25/35 ns (max)
- High density 24-pin SOJ package
- Low power
  - Active mode: 300 mW (typ)
  - Standby mode: 100 µW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

Pin Arrangement



(Top View)

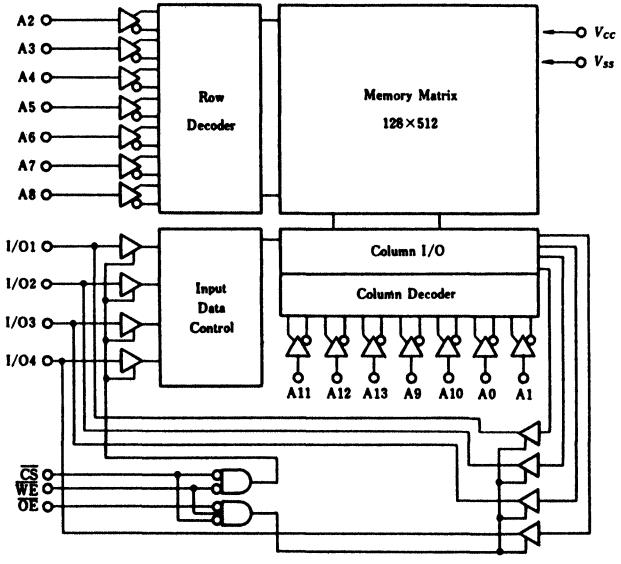
Ordering Information

Type No.	Access Time	Package
HM6289JP-25	25 ns	300-mil
HM6289JP-35	35 ns	24-pin
HM6289LJP-25	25 ns	SOJ
HM6289LJP-35	35 ns	(CP-24D)

Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



HITACHI

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O pin	Ref. Cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	Icc	Dout	Read cycle (1)–(3)
L	H	L	Write	Icc	Din	Write cycle (1)–(2)
L	L	L	Write	Icc	Din	Write cycle (3)–(6)

Note: ×; H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{in}	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +85	°C

Note: *1. Vin min = −2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: *1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	Vcc = Max Vin = 0V to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0 V to Vcc
Operating Vcc current	Icc	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. cycle
Standby Vcc current (1)	I_{SB1}*2	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc − 0.2 V
	I_{SB1}*3	—	0.02	0.1	mA	0V ≤ Vin ≤ 0.2 V or Vcc − 0.2 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. P-version
*3. LP-version

Capacitance (Ta = 25°C, f = 1MHz)

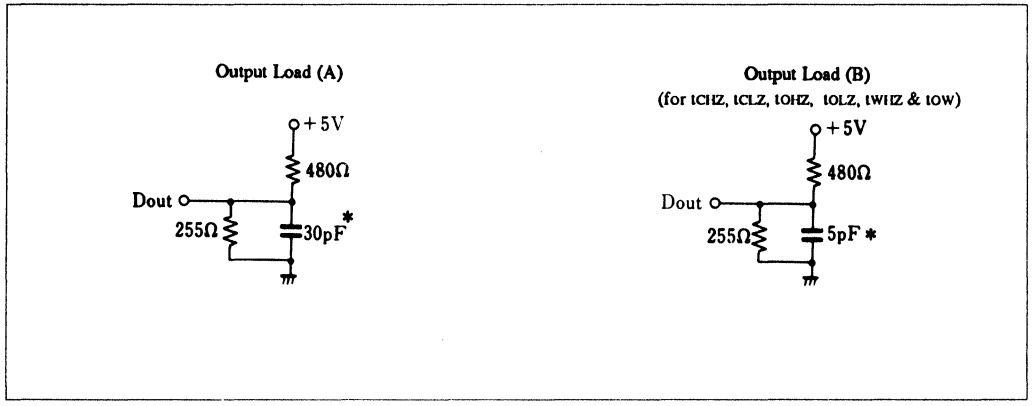
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	V I/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures



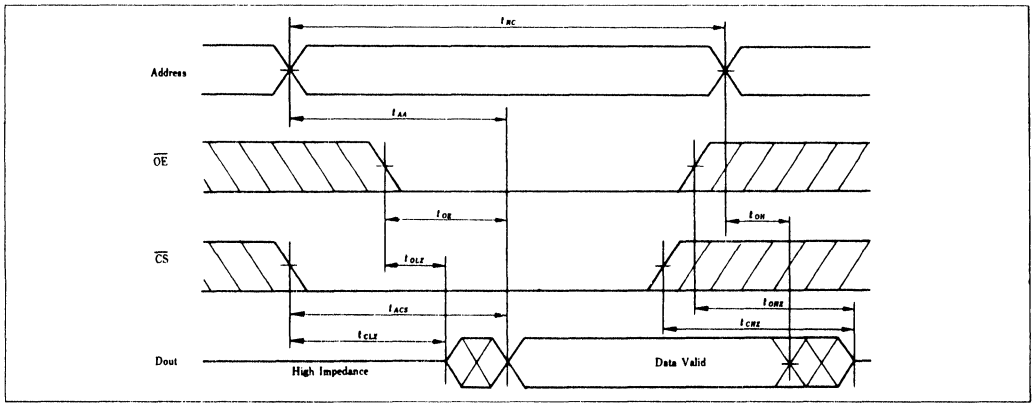
Note: * Including scope & jig.

Read Cycle

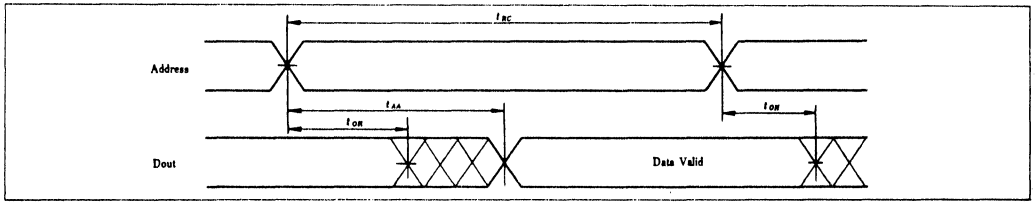
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	12	0	20	ns
Chis disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Note: *1. Output transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

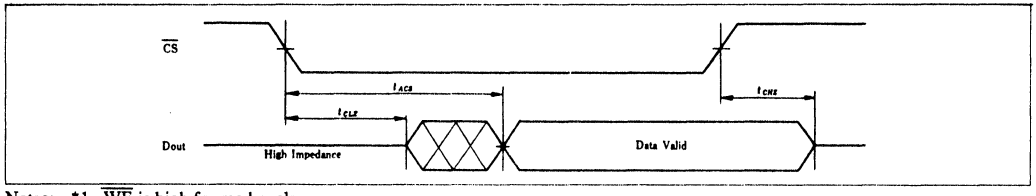
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1,*2,*4



Read Timing Waveform (3) *1,*3,*4



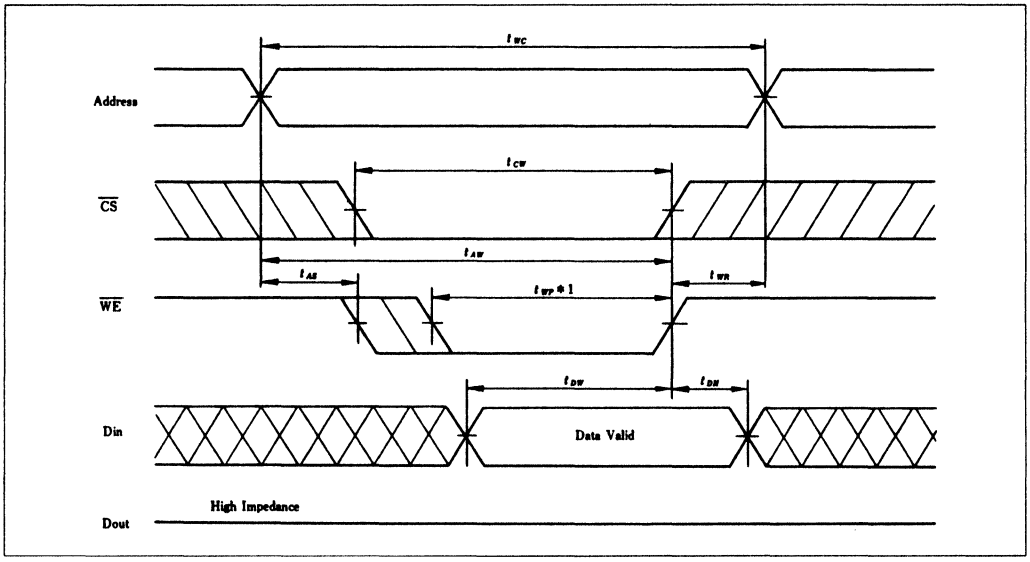
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

Write Cycle

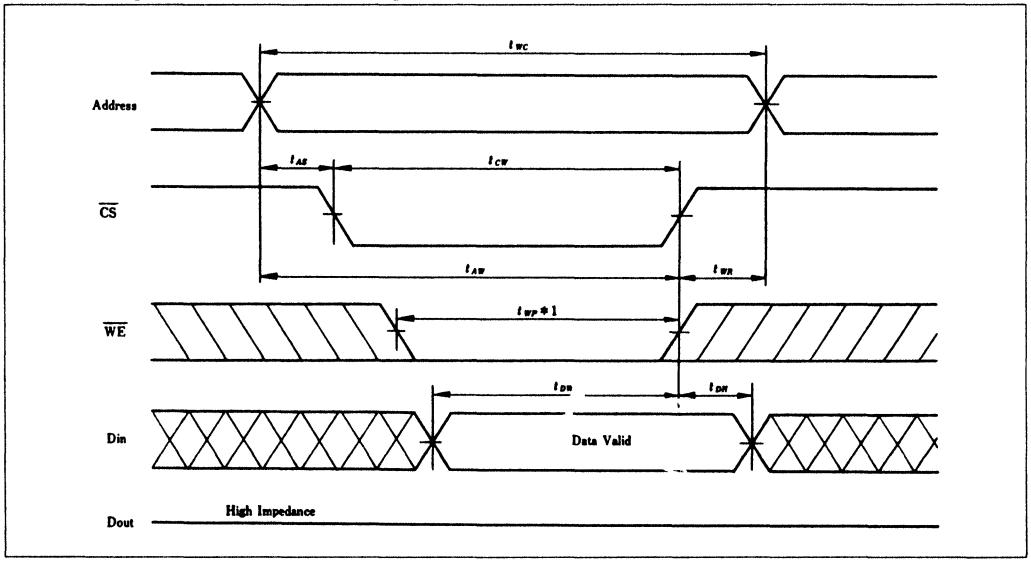
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Write cycle time	tWC	25	—	35	—	ns
Chip selection to end of write	tCW	20	—	30	—	ns
Address valid to end of write	tAW	20	—	30	—	ns
Address setup time	tAS	0	—	0	—	ns
Write pulse width	tWP	20	—	30	—	ns
Write recovery time	tWR	0	—	0	—	ns
Output disable to output in high-Z*1	tOHZ	0	10	0	10	ns
Write to output in high-Z*1	tWHZ	0	8	0	10	ns
Data to write time overlap	tDW	12	—	20	—	ns
Data hold from write time	tDH	0	—	0	—	ns
Output active from end of write*1	tOW	5	—	5	—	ns

Note: *1. Output transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

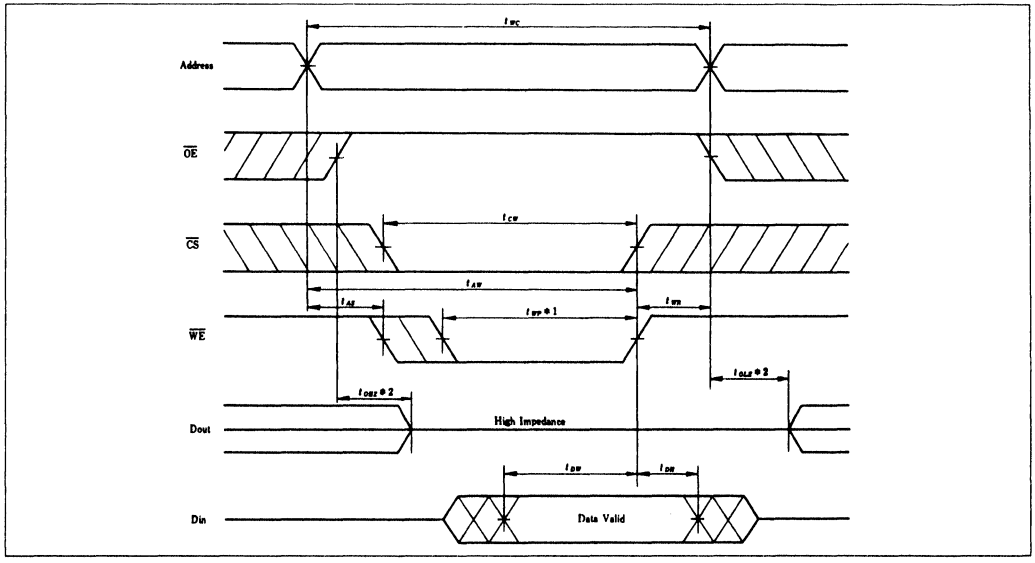
Write Timing Waveform (1) ($\overline{OE}$ = High, $\overline{WE}$ = Controlled)



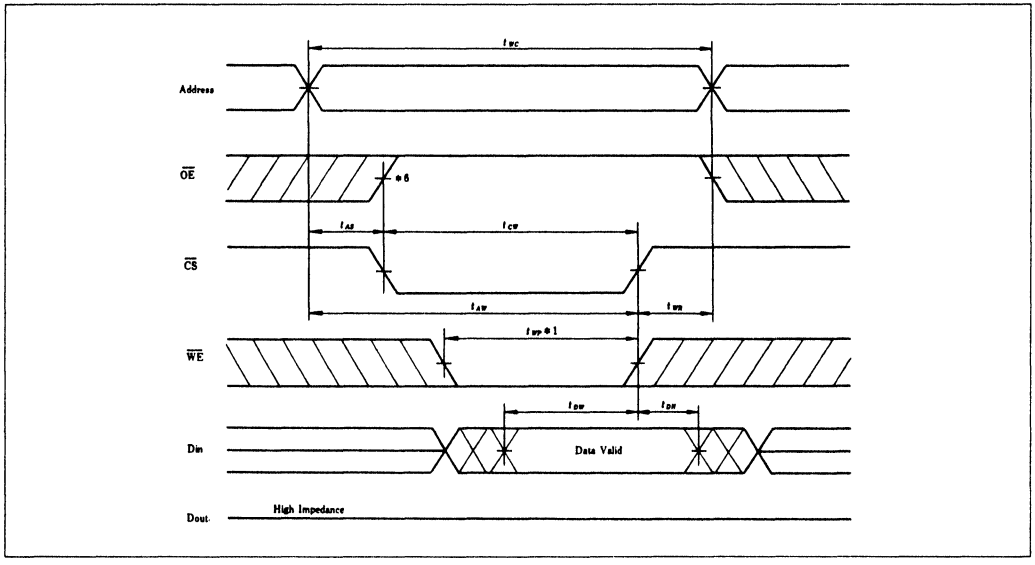
Write Timing Waveform (2) ($\overline{OE}$ = High, $\overline{CS}$ = Controlled)



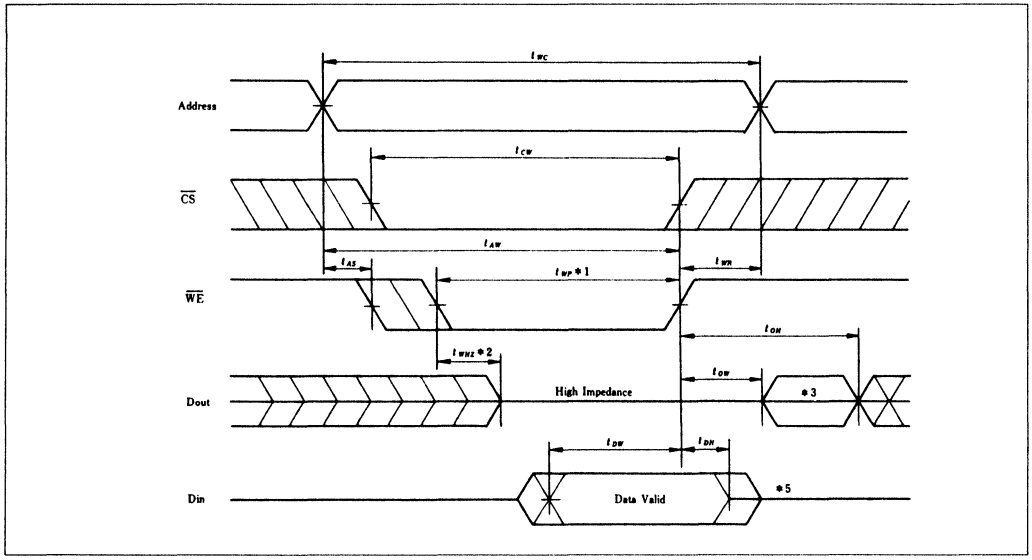
Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ = Controlled)



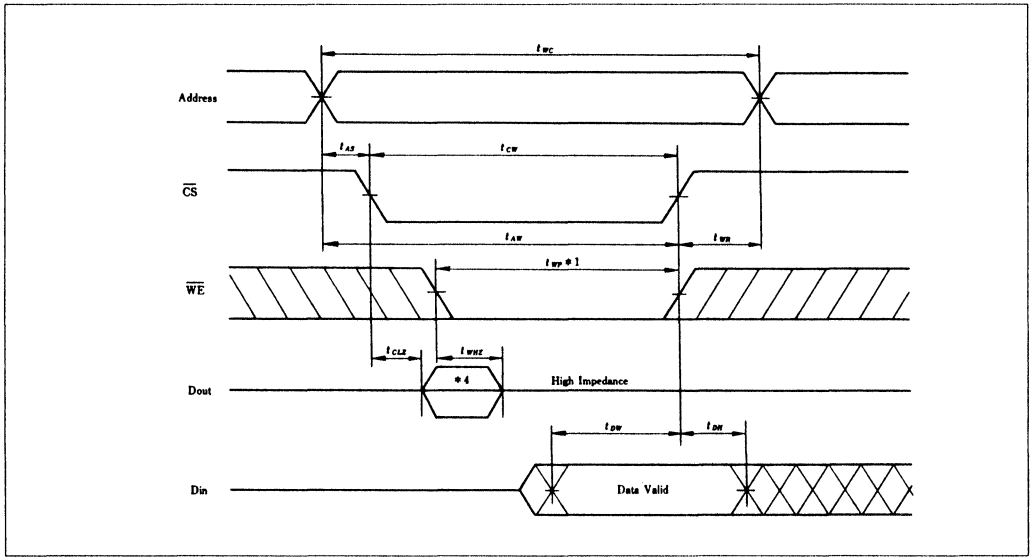
Write Timing Waveform (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ = Controlled)



Write Timing Waveform (5) ($\overline{OE}$ = Low, $\overline{WE}$ = Controlled)



Write Timing Waveform (6) ($\overline{OE}$ = Low, $\overline{CS}$ = Controlled)



Notes: *1 A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (tWP)

*2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tOW. Then the data input signals of opposite phase to the outputs must not be applied to them.

*6. Dout is the same phase of write data of this write cycle, if tWR is long enough.

*7. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

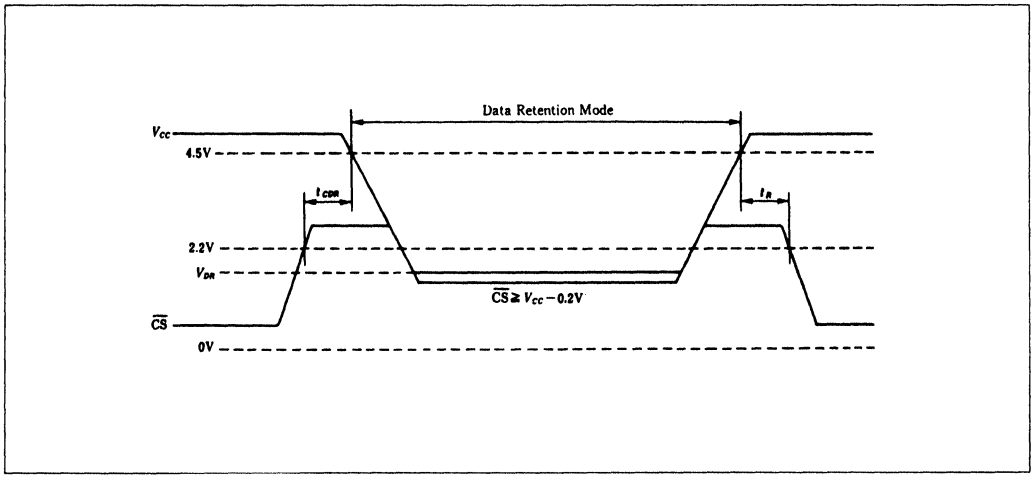
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

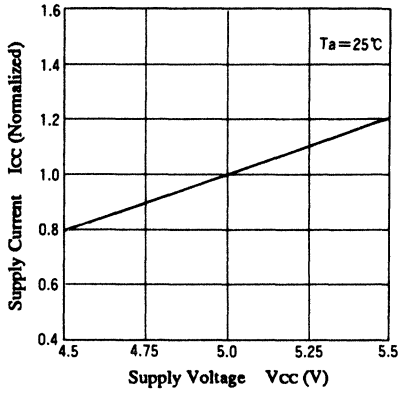
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V,
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Note: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

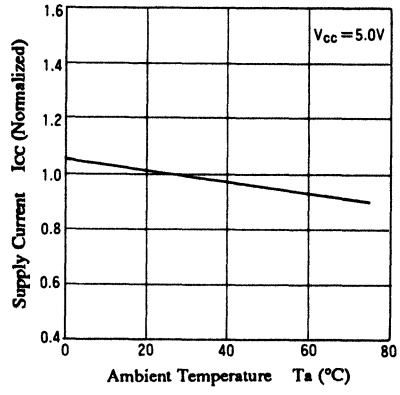
Low Vcc Data Retention Waveform



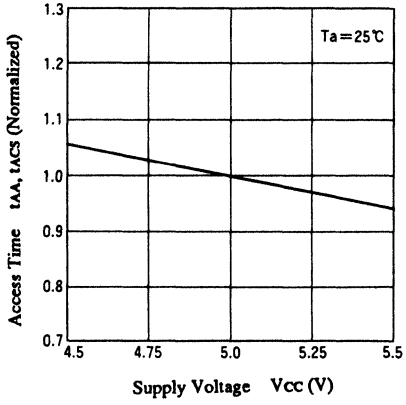
Supply Current vs. Supply Voltage



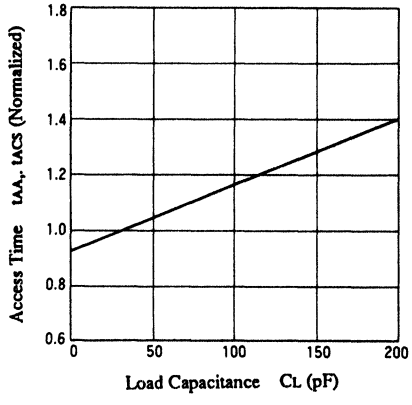
Supply Current vs. Ambient Temperature



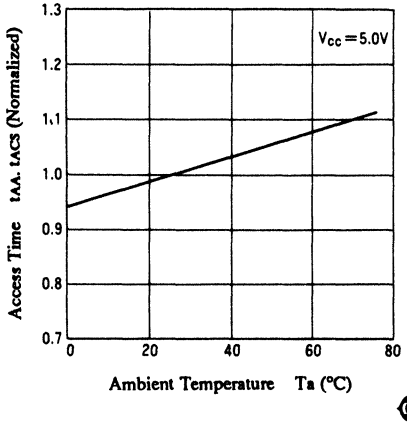
Access Time vs. Supply Voltage



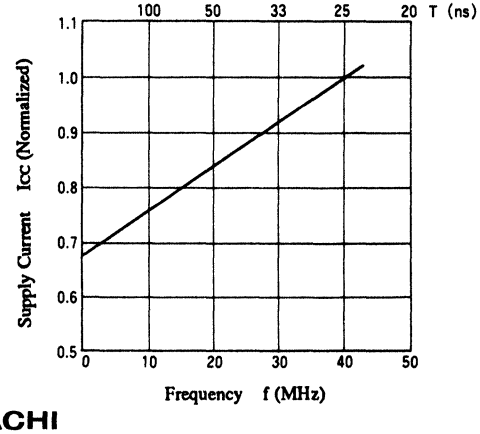
Access Time vs. Load Capacitance



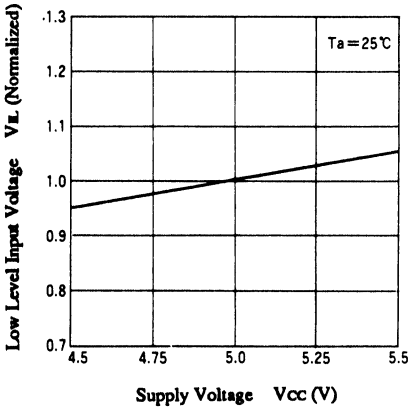
Access Time vs. Ambient Temperature



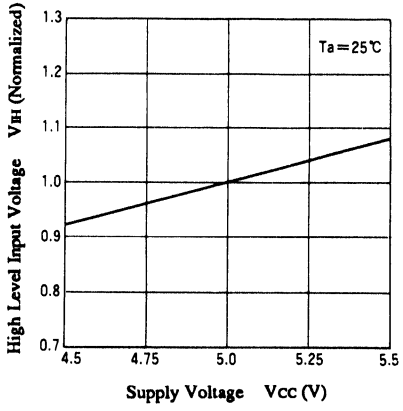
Supply Current vs. Frequency



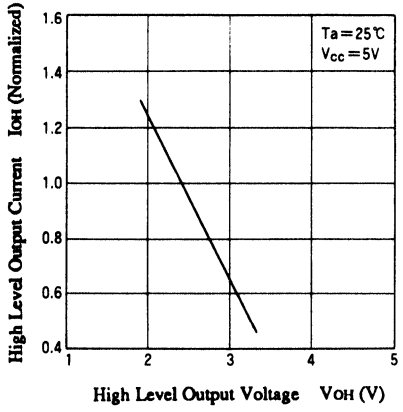
Low Level Input Voltage vs. Supply Voltage



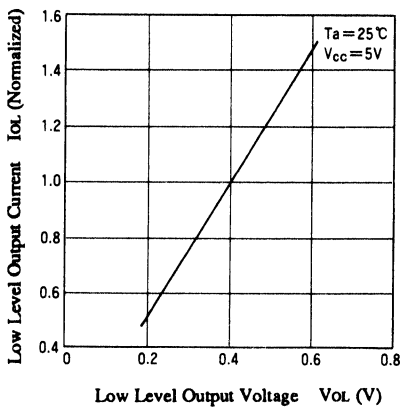
High Level Input Voltage vs. Supply Voltage



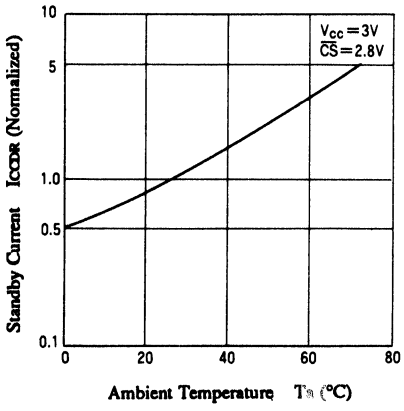
Output Current vs. Output Voltage (1)



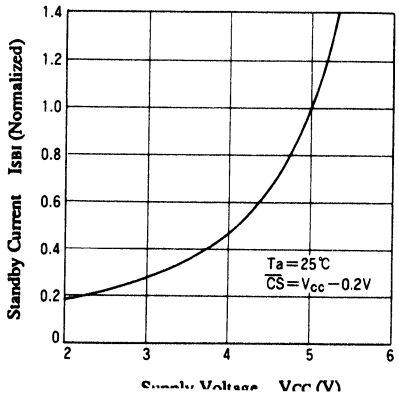
Output Current vs. Output Voltage (2)



Standby Current vs. Ambient Temperature

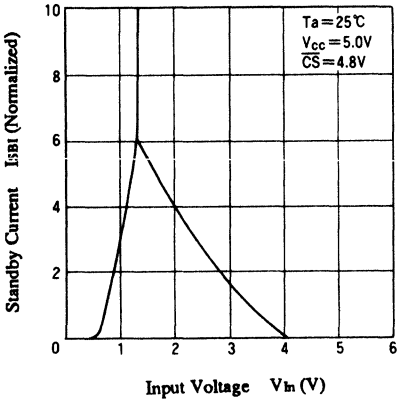


Standby Current vs. Supply Voltage



2

Standby Current vs. Input Voltage



HM6789 Series — Maintenance Only

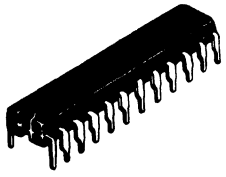
Refer to HM6789HA Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

- Super Fast Access Time: . . . . . 25/30 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 230 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789P Series



(DP-24NC)

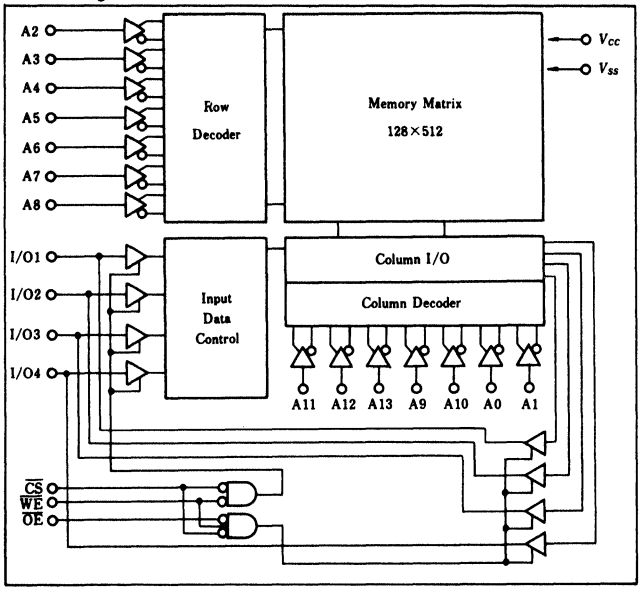
HM6789JP Series

(CP-24D)

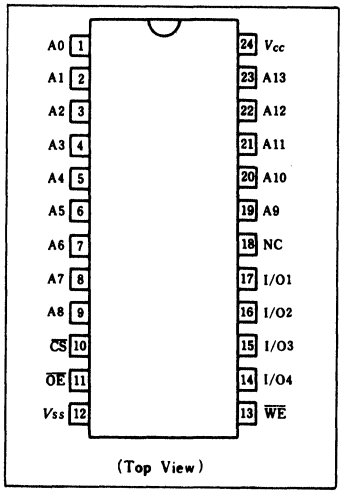
Ordering Information

Type No.	Access Time	Package
HM6789P-25	25ns	300 mil 24 pin
HM6789P-30	30ns	plastic DIP
HM6789JP-25	25ns	300 mil 24 pin
HM6789JP-30	30ns	Plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range under bias	T_{stg}(bias)	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 20ns.

Function Table

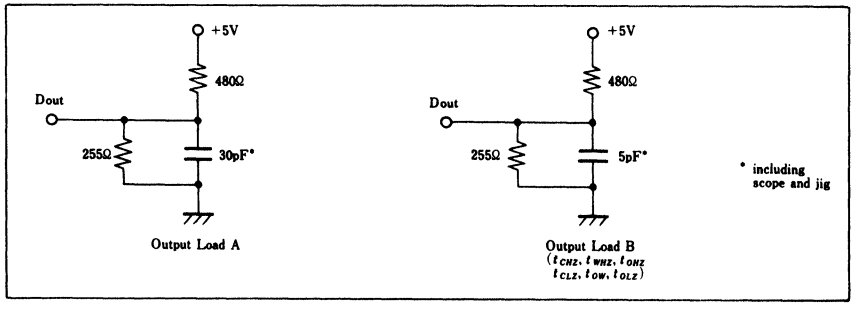
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Din	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} – 0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} – 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	8	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	0	–	0	–	ns
Output Enable to Output Valid	t_{OE}	0	15	0	15	ns
Output Enable to Output in Low Z	t_{OLZ}*1	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Input Voltage Rise/Fall Time	t_T*2	–	150	–	150	ns

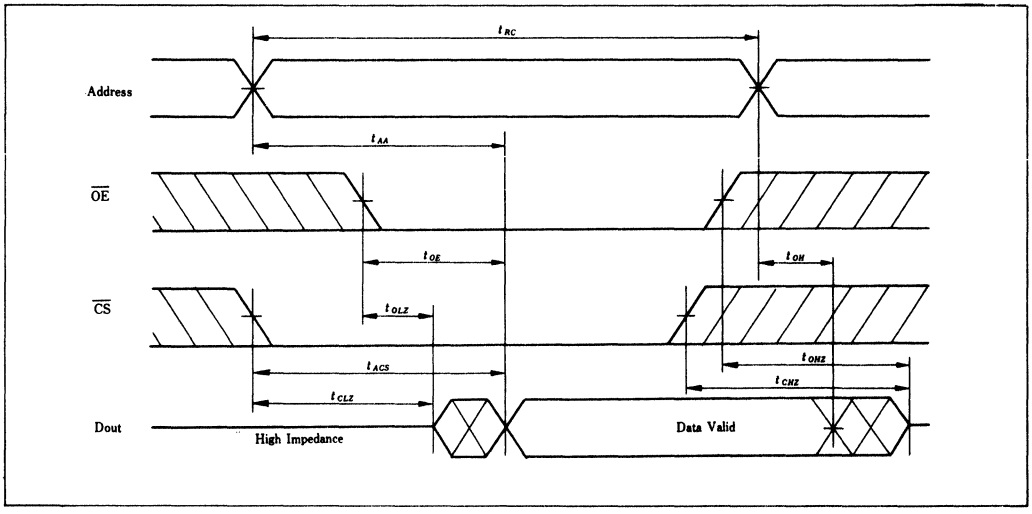
Write Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	30	–	ns
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	20	–	25	–	ns
Write Pulse Width	t_{WP}	20	–	25	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}*1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	–	20	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Output Disable to Output in Hihg Z	t_{OHZ}*1	0	10	0	10	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

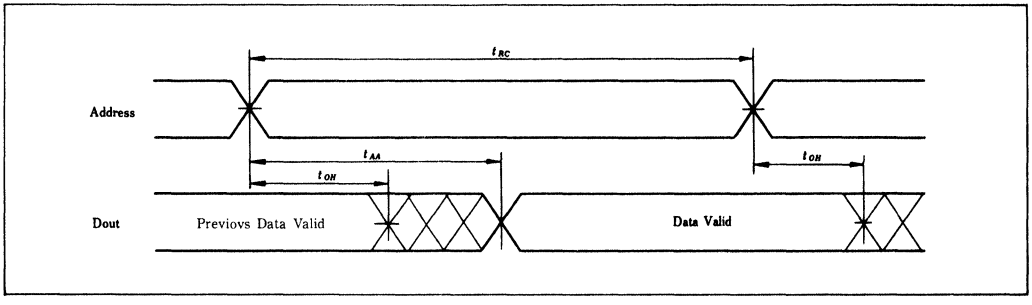
Notes) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.
*2. If t_T becomes more than 150ns, there is possibility of function fail.
Please contact your nearest Hitachi Sales Dept. regarding specification.

Timing Waveform

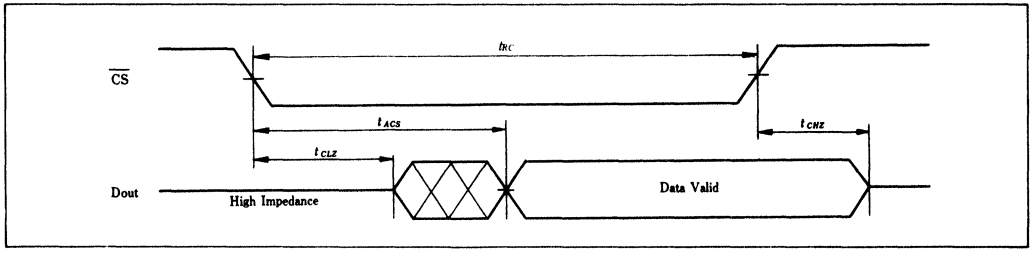
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

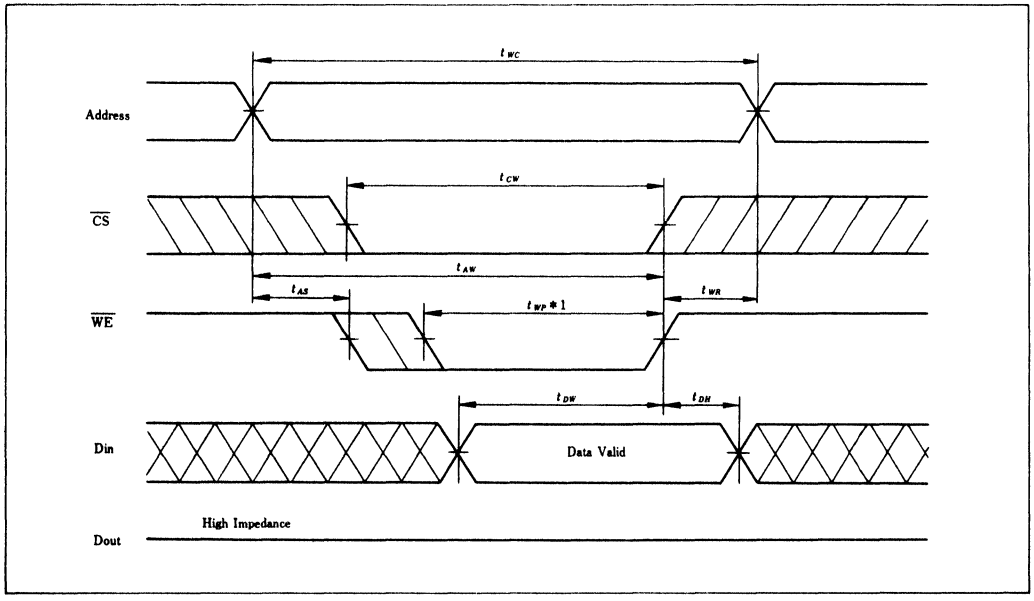


Read Cycle (3) *1, *3, *4

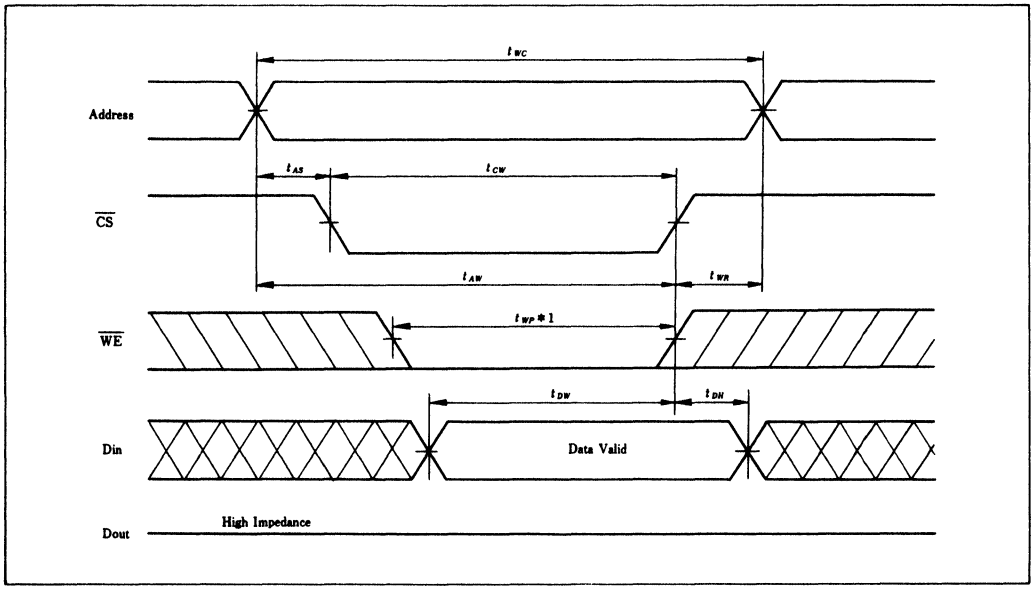


Notes) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. $\overline{OE} = V_{IL}$
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

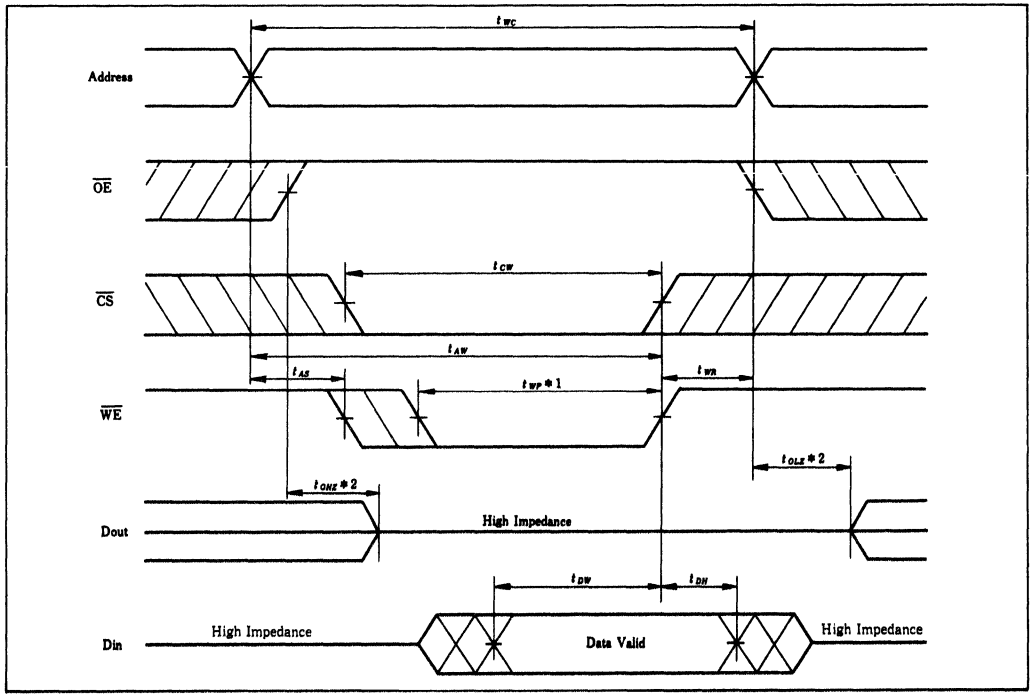
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



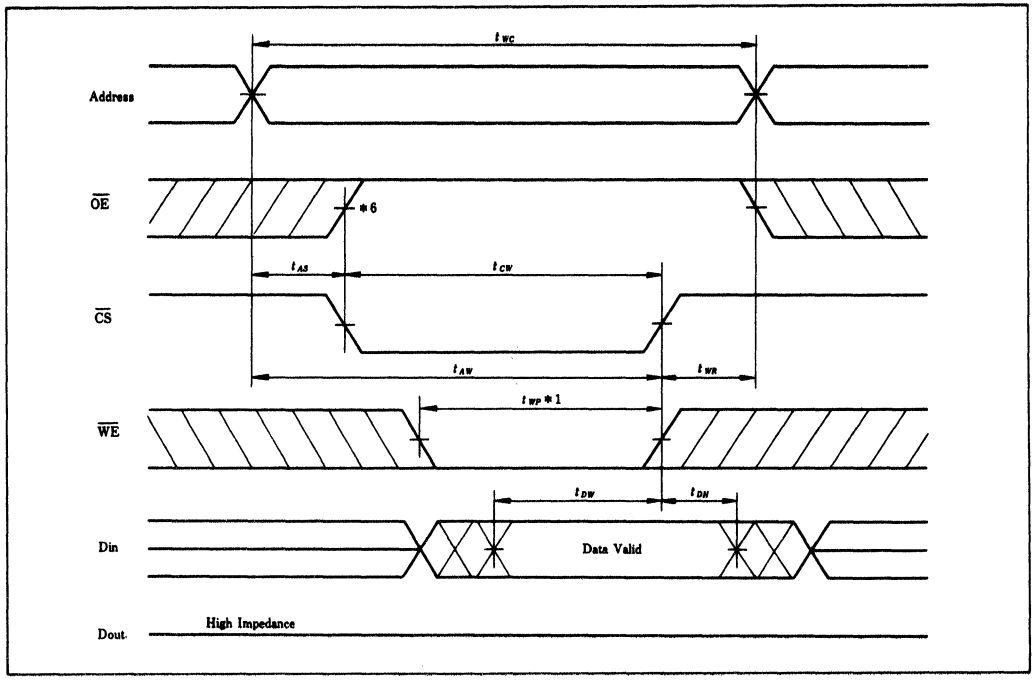
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



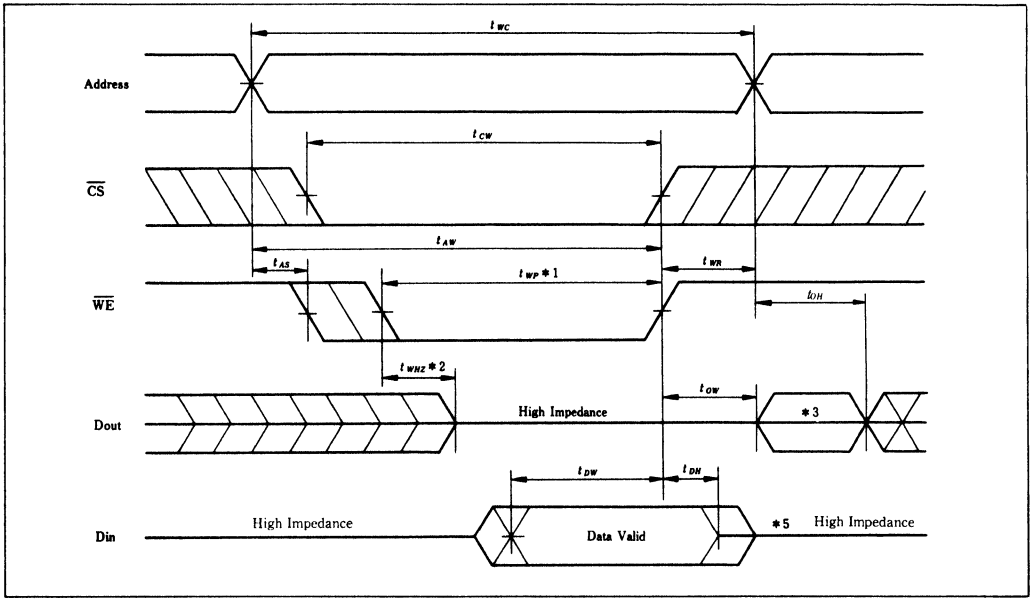
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



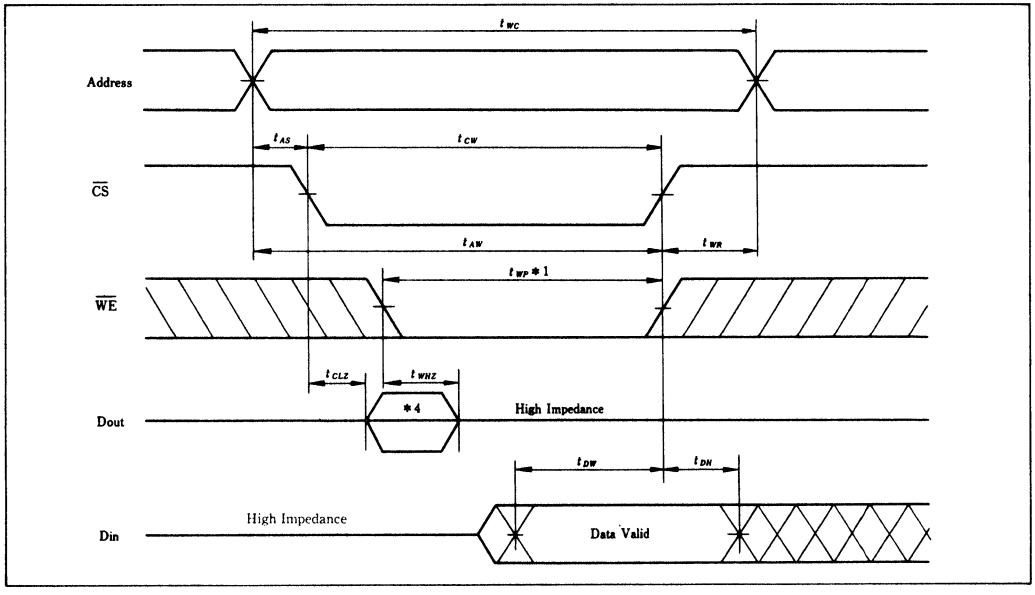
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3. Dout is the same phase of write data of this write cycle.

*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6789H Series — Maintenance Only

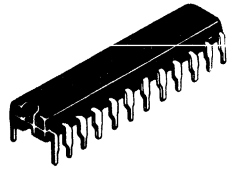
Refer to HM6789HA Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

- Super Fast Access Time: . . . . . 15/20 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 280 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789HP Series



(DP-24NC)

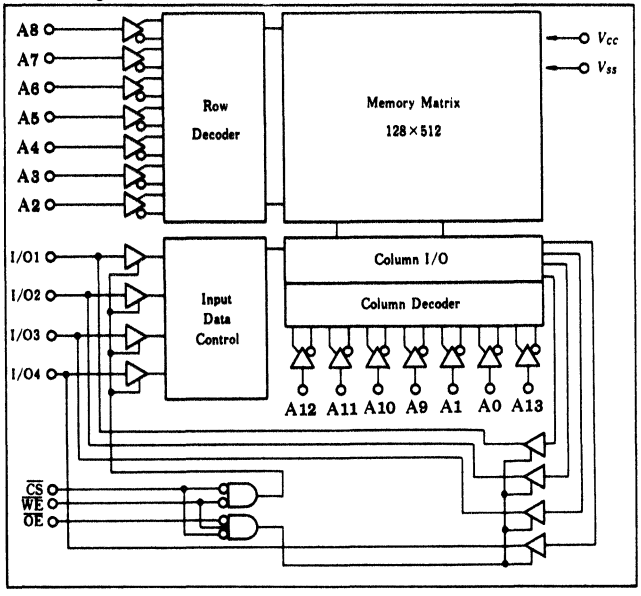
HM6789HJP Series

(CP-24D)

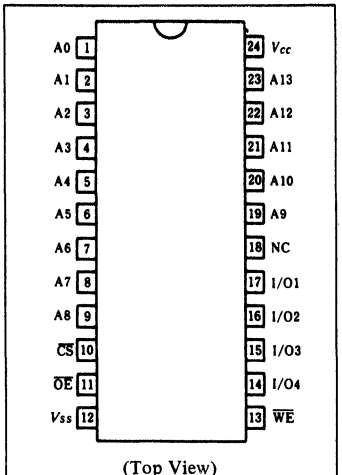
Ordering Information

Type No.	Access Time	Package
HM6789HP-15	15ns	300 mil 24 pin
HM6789HP-20	20ns	plastic DIP
HM6789HJP-15	15ns	300 mil
HM6789HJP-20	20ns	24 pin plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range under bias	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Note) The specifications of this device are subject to change without notice. Please contact Hitachi's Sales Dept. regarding specifications.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 10ns.

Function Table

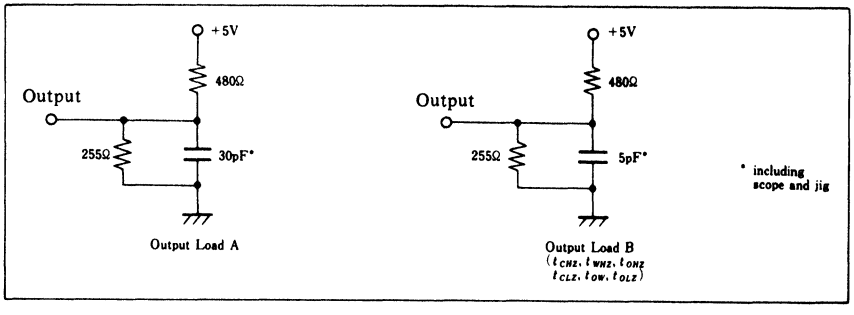
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data Out	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} − 0.2V, V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} − 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4mA

AC Test Conditions

- Input pulse levels . . . . . V_{SS} to 3.0V
- Input and Output reference levels . . . . . 1.5 V
- Input rise and fall time . . . . . 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	15	–	20	–	ns
Address Access Time	t_{AA}	–	15	–	20	ns
Chip Select Access Time	t_{ACS}	–	15	–	20	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	3	–	3	–	ns
Output Enable to Output Valid	t_{OE}	0	12	0	12	ns
Output Enable to Output in Low Z	t_{OLZ}*1	3	–	3	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	6	0	8	ns
Output Hold from Address Change	t_{OH}	3	–	3	–	ns

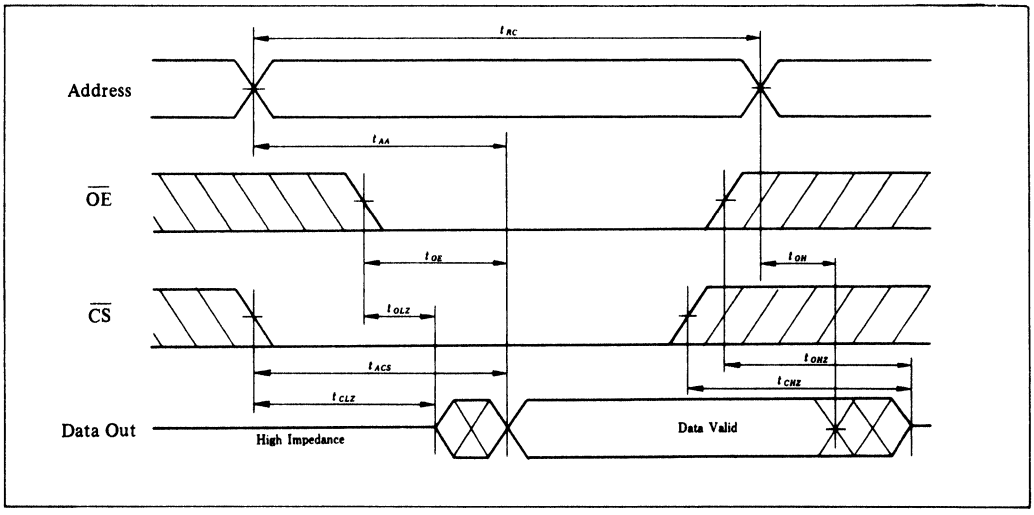
Write Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	15	–	20	–	ns
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	10	–	15	–	ns
Write Pulse Width	t_{WP}	10	–	15	–	ns
Write Recovery Time	t_{WR}	1	–	1	–	ns
Write to Output in High Z	t_{WHZ}*1	0	6	0	8	ns
Data Valid to End of Write	t_{DW}	9	–	10	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}*1	0	6	0	8	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

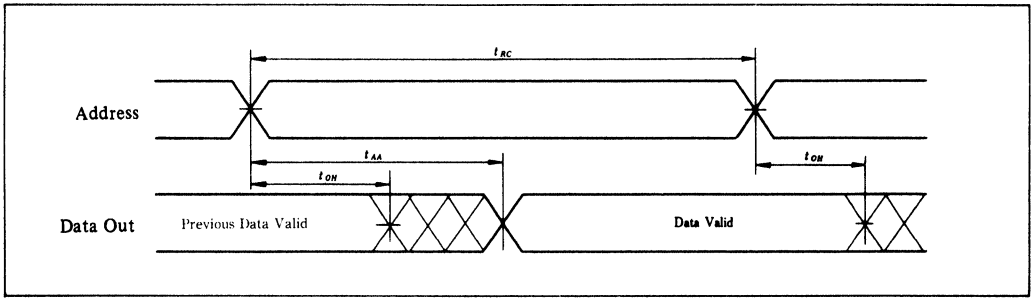
Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Timing Waveform

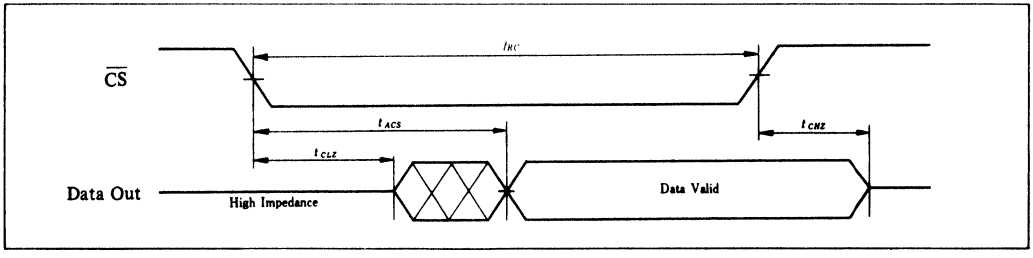
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

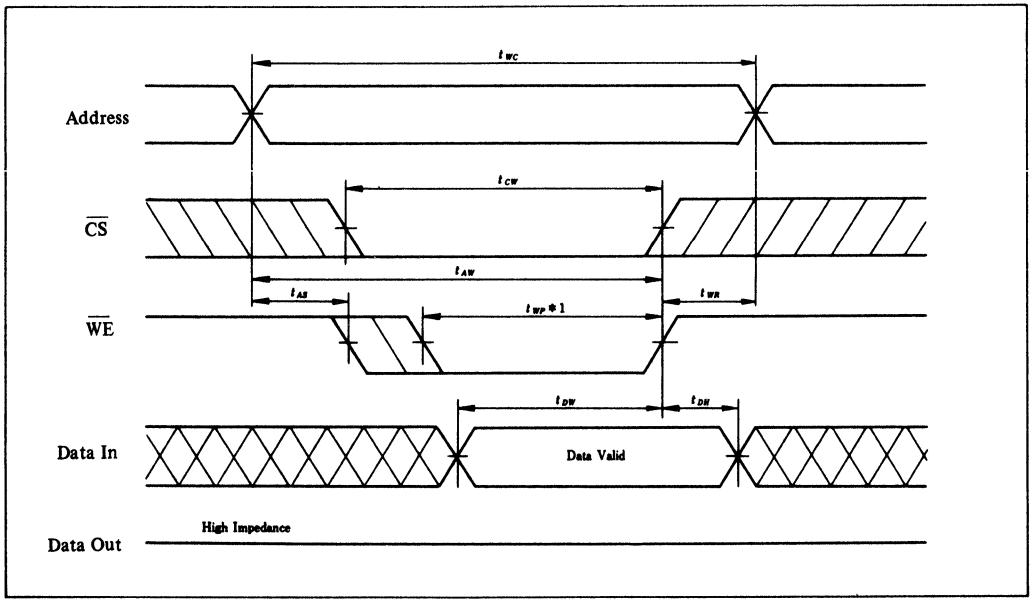


Read Cycle (3) *1, *3, *4

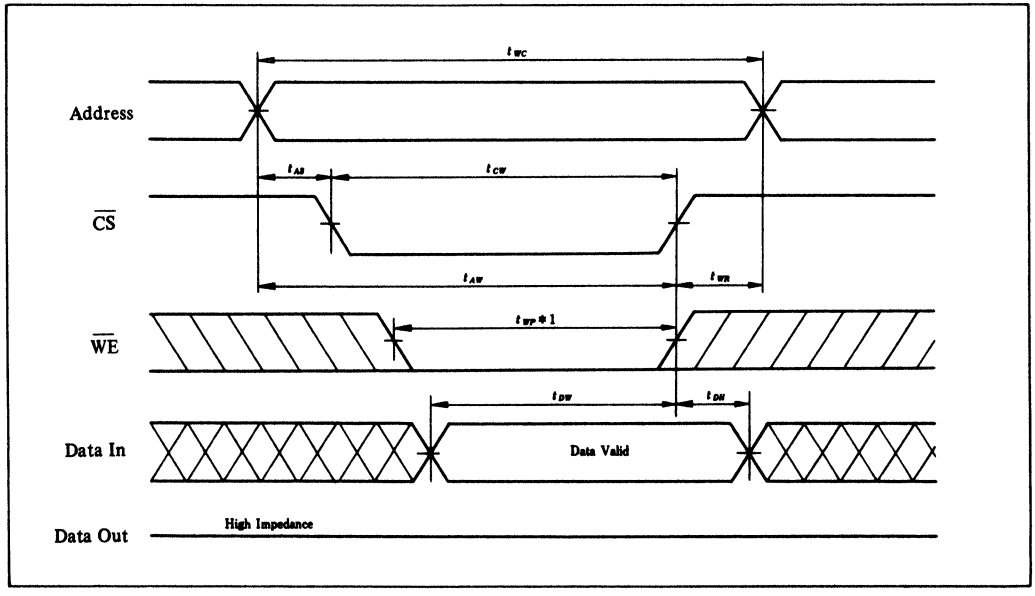


Notes) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. $\overline{OE} = V_{IL}$
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

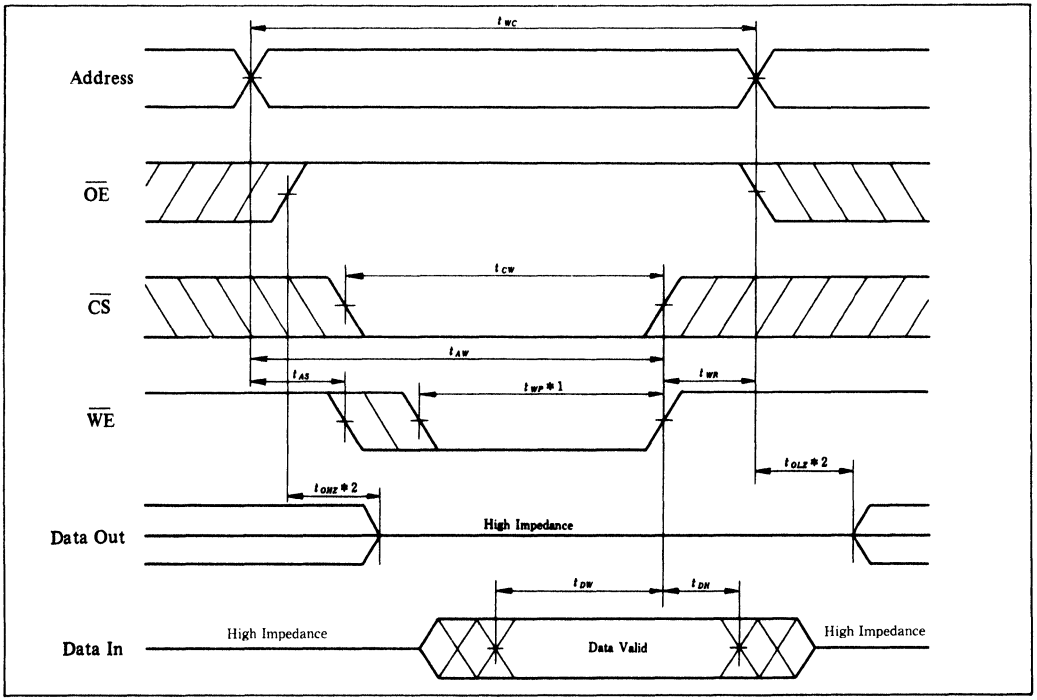
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



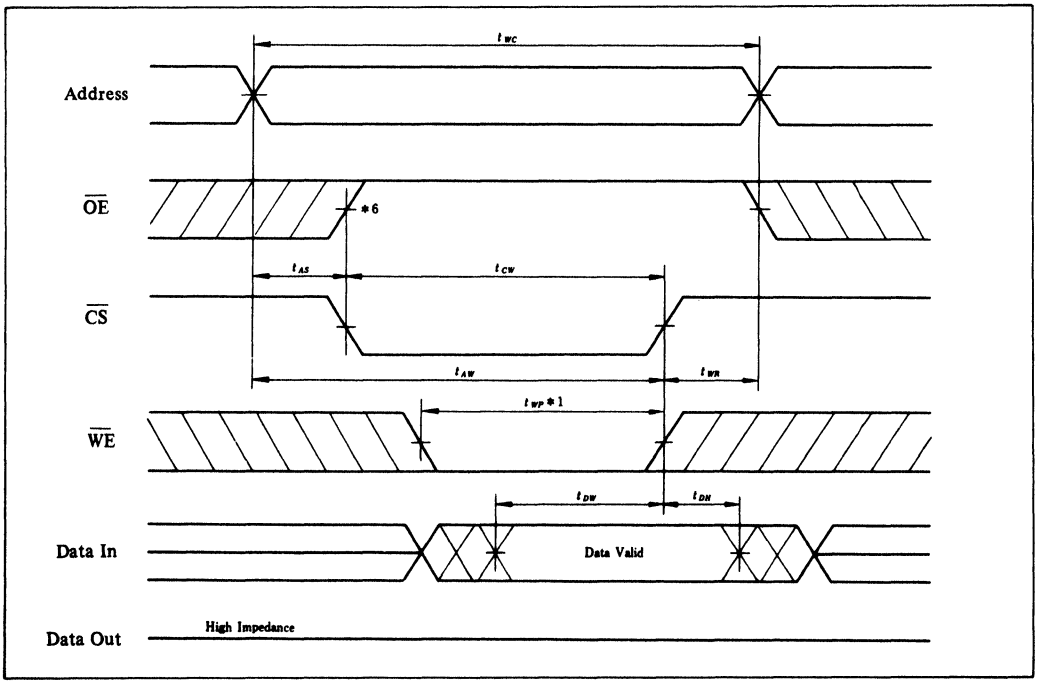
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



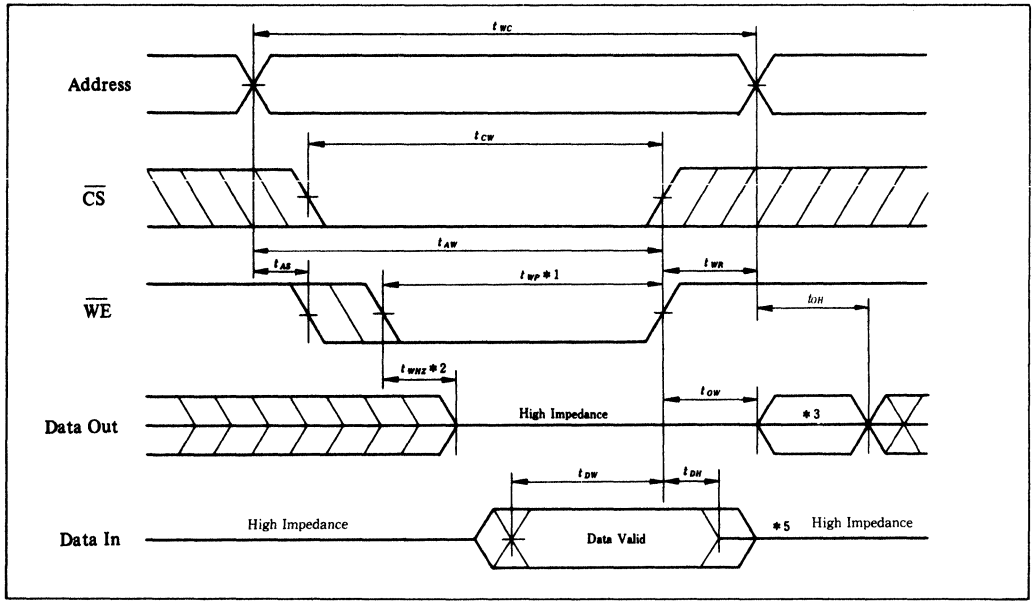
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



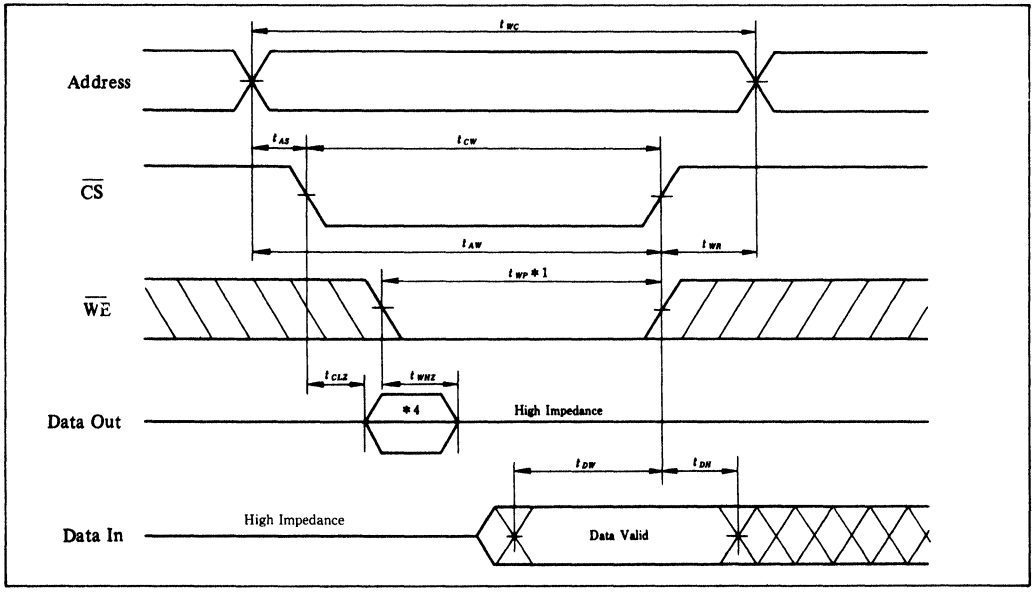
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3. Data Out is the same phase of write data of this write cycle.

*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6789HA Series

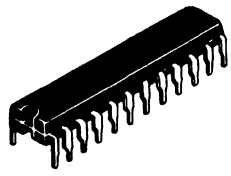
16384-Word × 4-Bit High Speed Static RAM (with $\overline{OE}$)

■ FEATURES

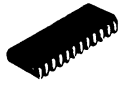
- Super Fast
  Access Time .....Add. 12/15/20ns (max.)
  $\overline{OE}$ 6/7/8ns (max.)
- Low Power Dissipation
  (DC) Operating .....300mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6789HAP-12	12ns	300 mil 24 pin
HM6789HAP-15	15ns	Plastic DIP
HM6789HAP-20	20ns	(DP-24NC)
HM6789HAJP-12	12ns	300 mil 24 pin
HM6789HAJP-15	15ns	Plastic SOJ
HM6789HAJP-20	20ns	(CP-24D)

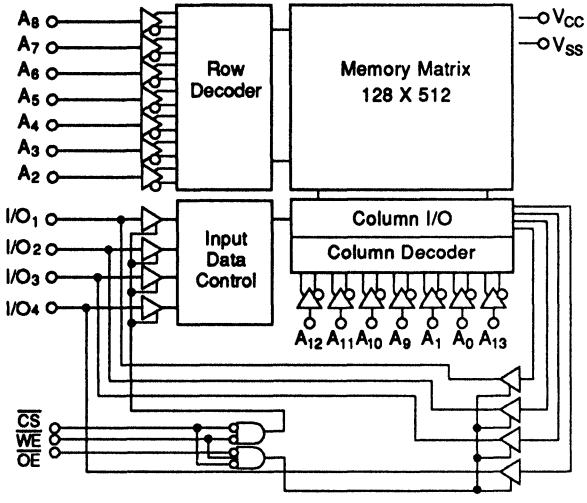


(DP-24NC)

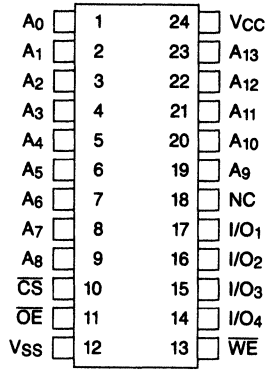


(CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

2

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	-3.0	—	0.8	V

*Pulse width ≤ 10ns, DC: -0.5V

■ TRUTH TABLE

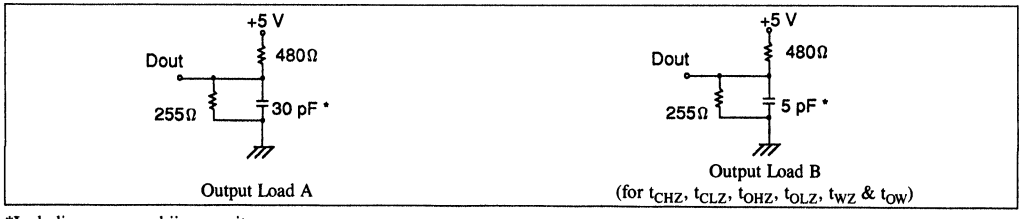
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$, $V_{SS} = 0V$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O}$, = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V

■ AC TEST CONDITIONS

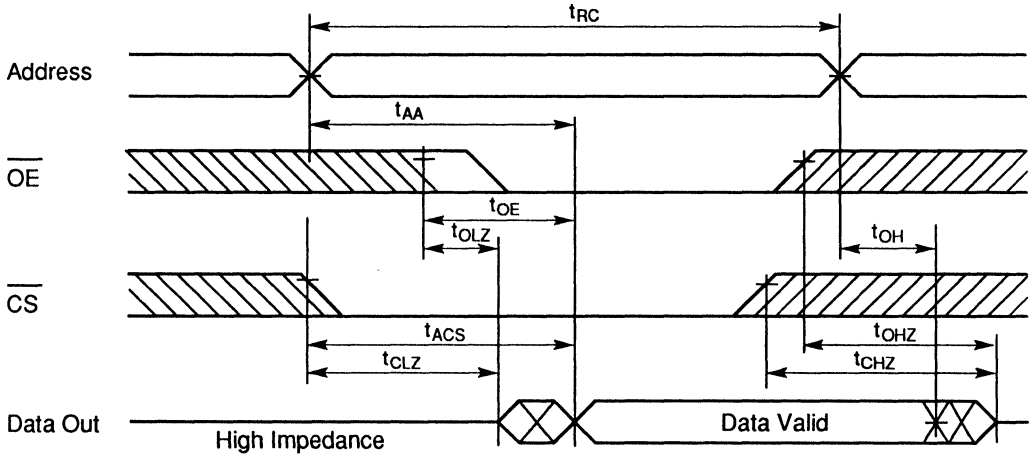
- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Reference Levels: 1.5V ± 200mV from steady level (Output Load B)
- Input Rise and Fall Time: 4ns
- Output Load: See Figure



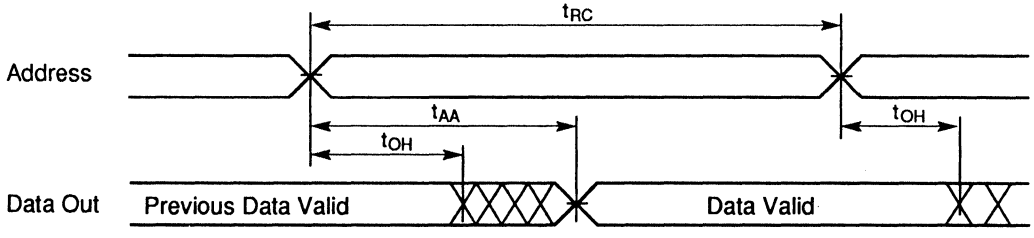
*Including scope and jig capacitance.

■ TIMING WAVEFORM

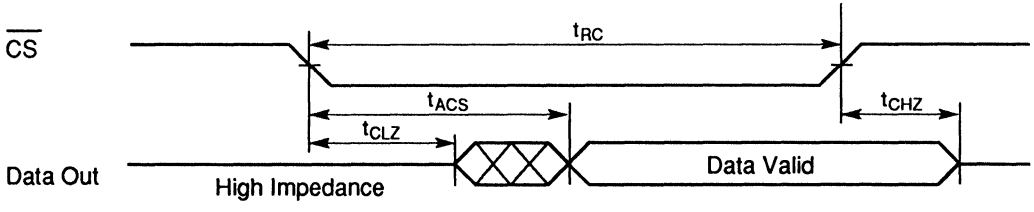
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)



• **Read Cycle (3)** (1) (3) (4)



NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

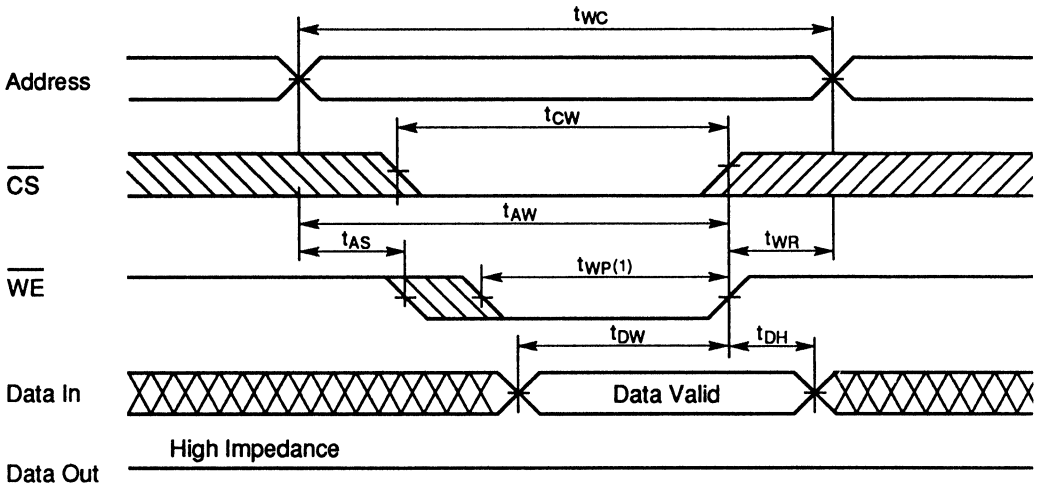
Item	Symbol	HM6789HA-12		HM6789HA-15		HM6789HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Chip Selection to Output in Low Z	t_{CLZ}	3	—	5	—	5	—	ns	1, 2
Output Enable to Output Valid	t_{OE}	0	6	0	7	0	8	ns	1
Output Enable to Output in Low Z	t_{OLZ}	2	—	2	—	2	—	ns	1, 2
Chip Deselection to Output in High Z	t_{CHZ}	0	6	0	6	0	8	ns	1, 2
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—

• Write Cycle

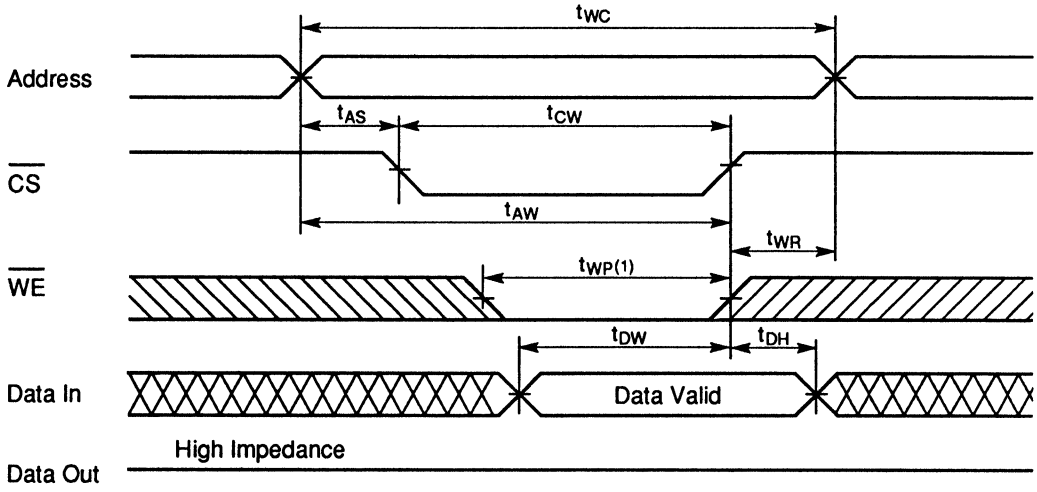
Item	Symbol	HM6789HA-12		HM6789HA-15		HM6789HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	—
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Write to Output in High Z	t_{WHZ}	0	6	0	6	0	8	ns	1, 2
Data Valid to End of Write	t_{DW}	6	—	7	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	1	6	1	6	1	8	ns	1, 2
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	1, 2

NOTES: 1. Transition is measured ±200mV from steady state voltage with Load B.
2. This parameter is sampled and not 100% tested.

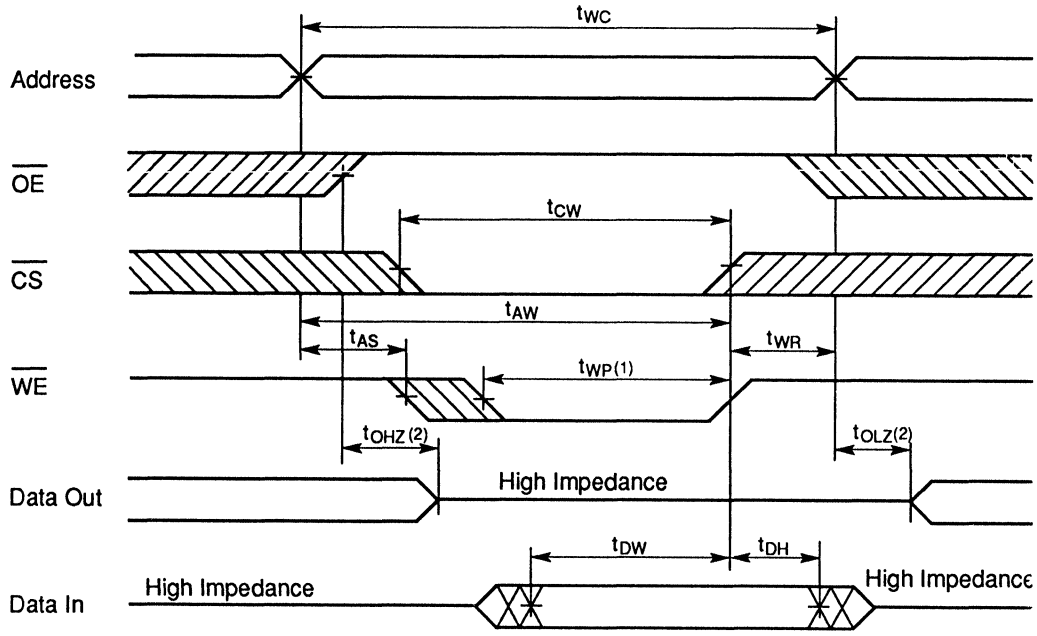
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



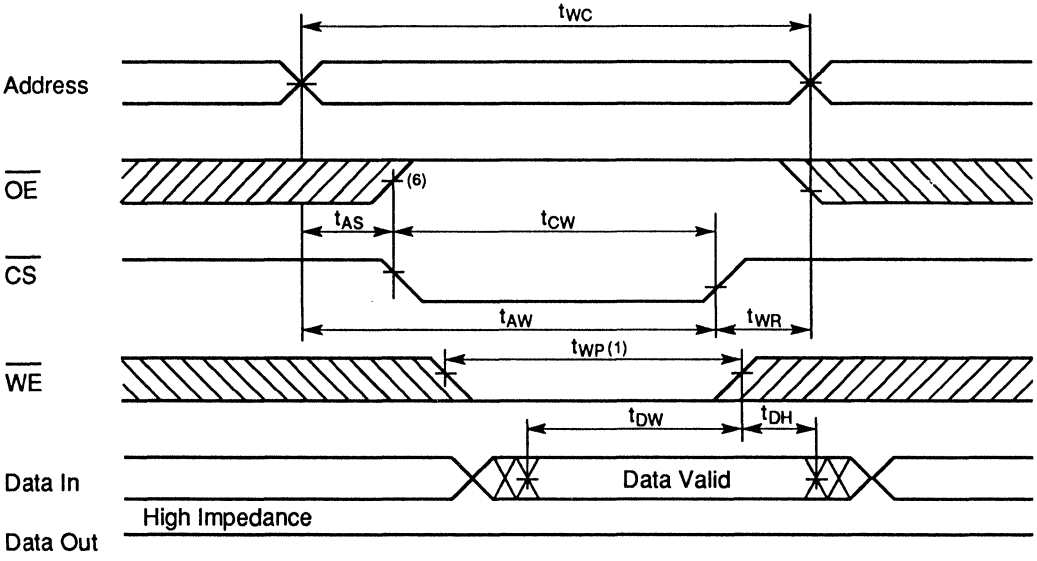
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



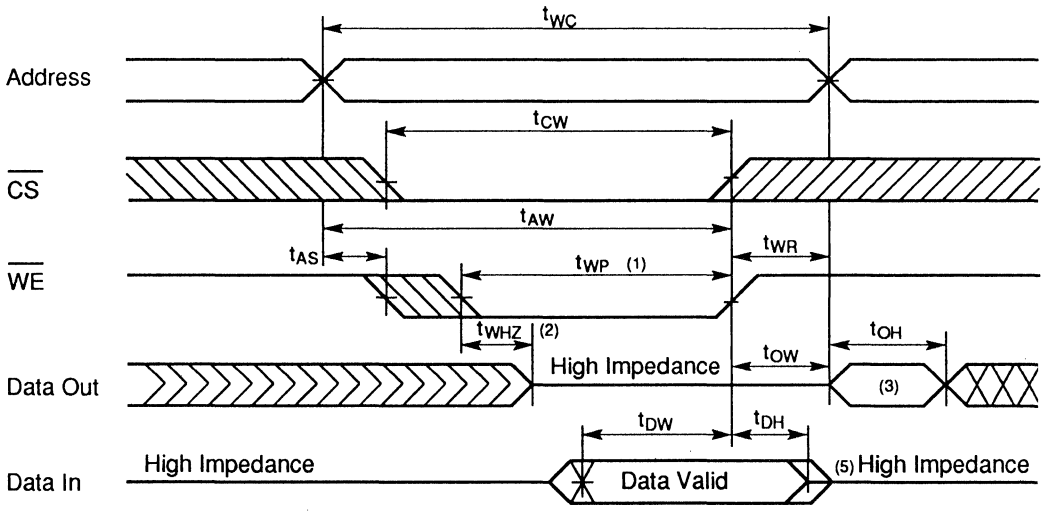
• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)

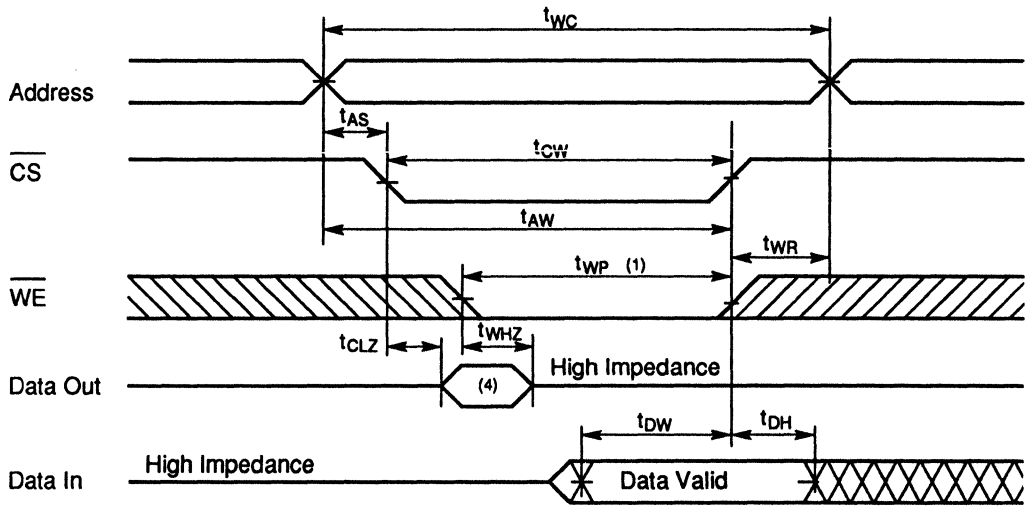


• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



2

• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. D_{out} is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

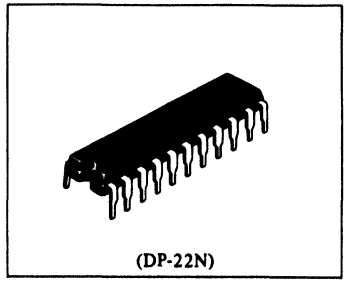
HM6287 Series — Maintenance Only

65536-word x 1-bit High Speed CMOS Static RAM

Refer to HM6287H Series

■ FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
  Standby: 100μW (typ.)/10μW (typ.) (L-version)
  Operation: 300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output
- Capability of Battery Back Up Operation (L-version)

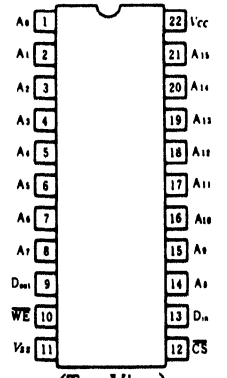


(DP-22N)

■ ORDERING INFORMATION

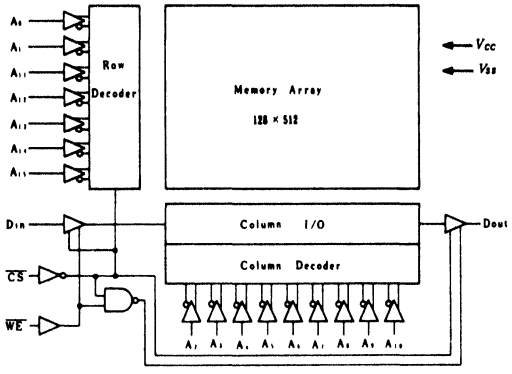
Type No.	Access Time	Package
HM6287P-45	45ns	300 mil 22 pin Plastic DIP
HM6287P-55	55ns	
HM6287P-70	70ns	
HM6287LP-45	45ns	
HM6287LP-55	55ns	
HM6287LP-70	70ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width ≦ 20ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{out} = 0mA, min. cycle	–	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	10	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V,	–	0.02	2.0	mA
		0V ≦ V_{in} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{in}	–	2*2	100*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = −4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	5	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	7.5	pF

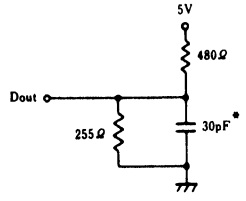
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

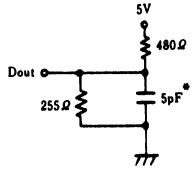
Input Pulse Levels: V_{SS} to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

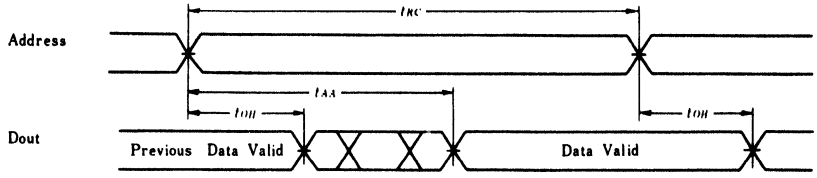


*Including scope & jig capacitance

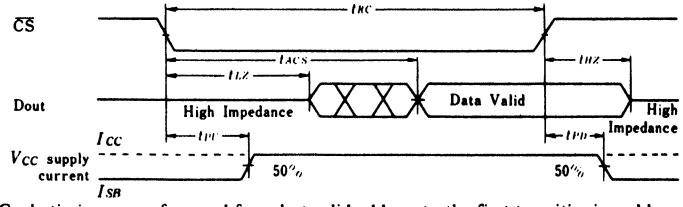
• READ CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns	1
Address Access Time	t_{AA}	–	45	–	55	–	70	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	7
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	–	40	ns	7

• Timing Waveform of Read Cycle No. 1 (4)(5)



• Timing Waveform of Read Cycle No. 2 (4)(6)

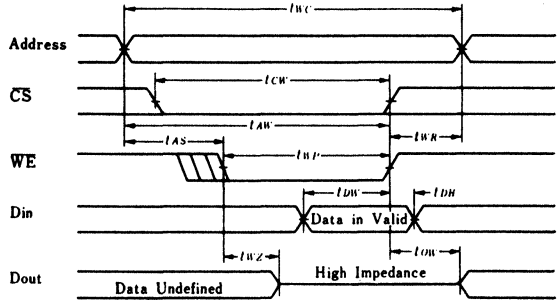


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

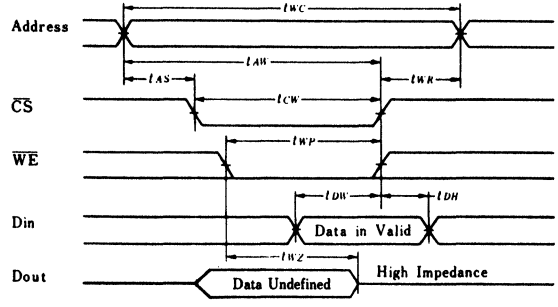
• WRITE CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns	2
Chip Selection to End of Write	t_{CW}	40	–	50	–	55	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	55	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	40	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	30	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3, 4

• Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



• Timing Waveform of Write Cycle No. 1 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high Simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

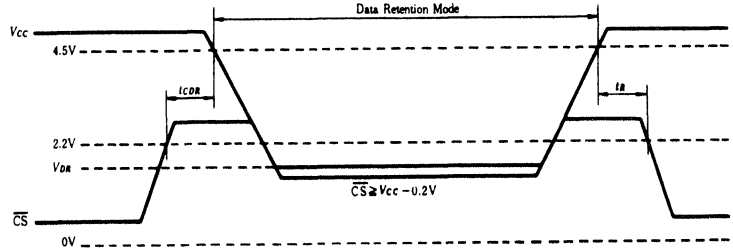
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L-version.

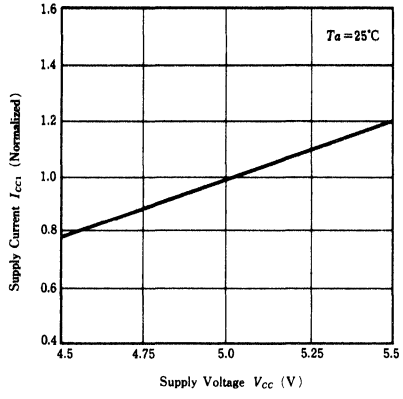
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}		–	1	50*2	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

Note) *1. t_{RC} = Read Cycle Time
*2. V_{CC} = 3.0V

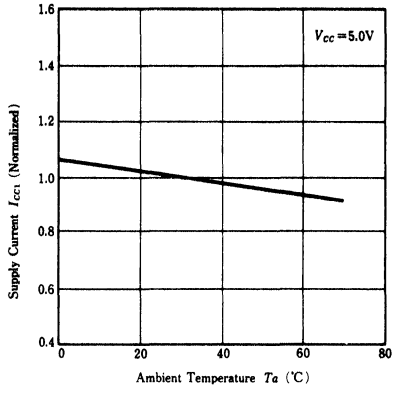
● LOW V_{CC} DATA RETENTION WAVEFORM



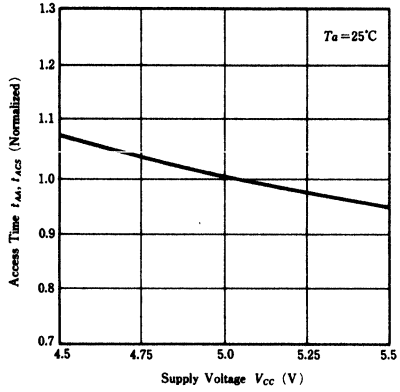
SUPPLY CURRENT vs. SUPPLY VOLTAGE



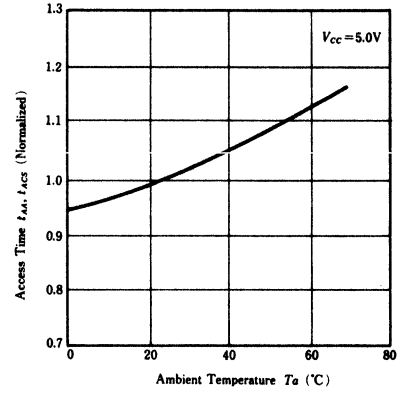
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



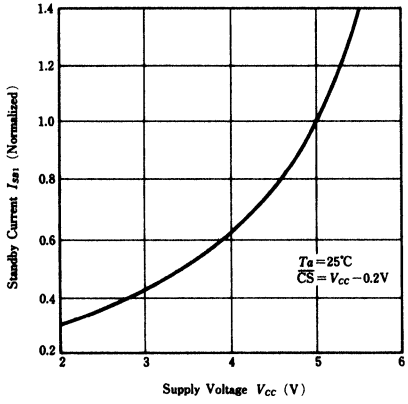
ACCESS TIME vs. SUPPLY VOLTAGE



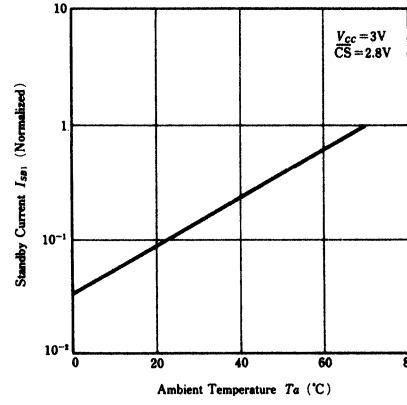
ACCESS TIME vs. AMBIENT TEMPERATURE



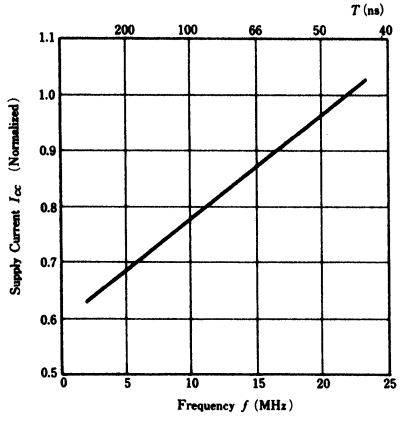
STANDBY CURRENT vs. SUPPLY VOLTAGE



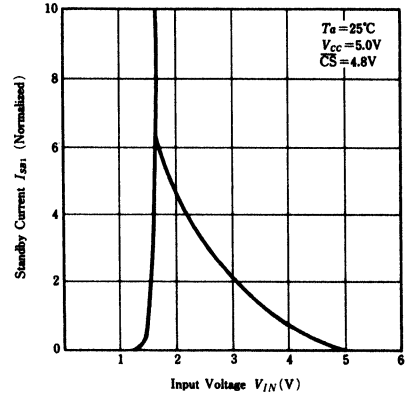
STANDBY CURRENT vs. AMBIENT TEMPERATURE



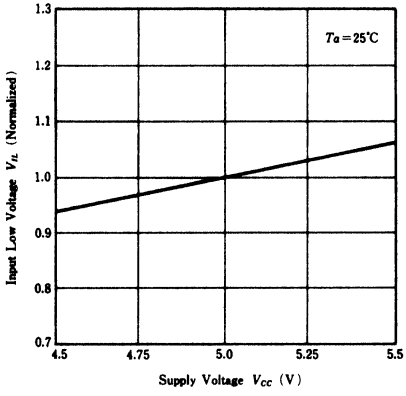
SUPPLY CURRENT vs. FREQUENCY



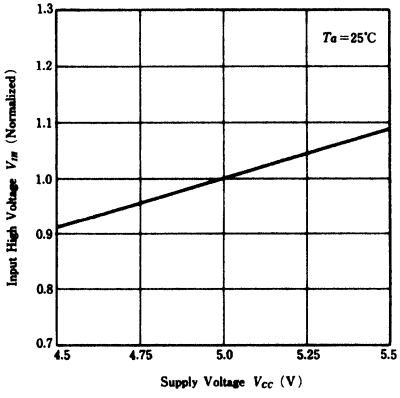
STANDBY CURRENT vs. INPUT VOLTAGE



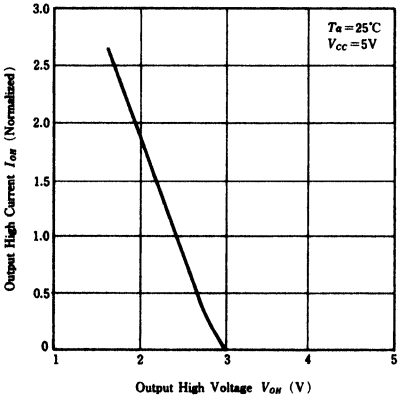
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



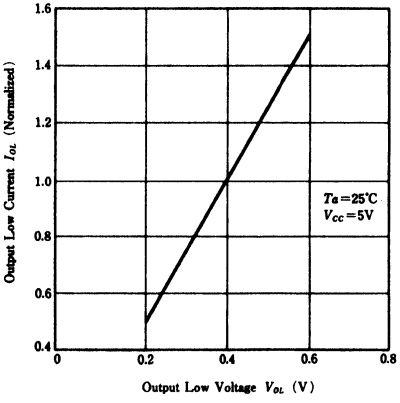
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



2

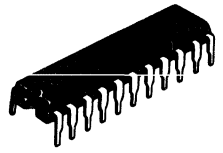
HM6287H Series

65536-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6287H is a high speed 64K static RAM organized as 64-kword × 1-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6287H packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting.

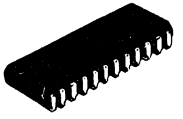
Low power version retains the data with battery back up.

HM6287HP Series



(DP-22NB)

HM6287HJP Series



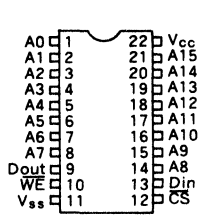
(CP-24D)

Features

- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

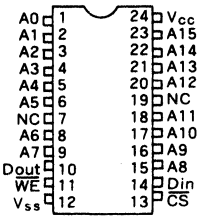
Pin Arrangement

HM6287HP Series



(Top View)

HM6287HJP Series



(Top View)

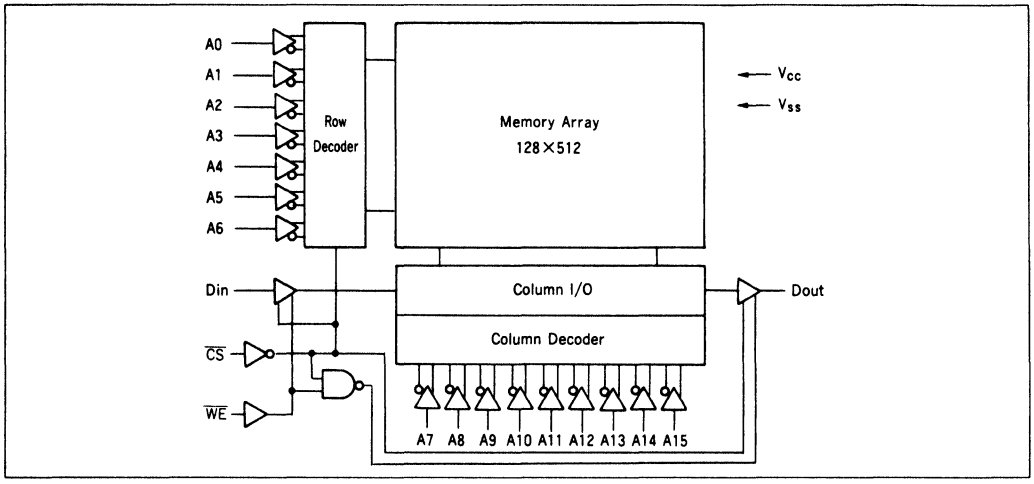
Pin Description

Pin Name	Function
A0 – A15	Address
Din	Input
Dout	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM6287HP-25	25 ns	300-mil 22-pin plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

Block diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	D_{out} Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	D_{out}	Read cycle 1, 2
L	L	Write	Icc	High-Z	Write cycle 1, 2

Note: ×: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: *1. V_T min = −2.0 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: *1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	Vcc = Max Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = Vss to Vcc
Operating Vcc current	Icc	—	60	120	mA	$\overline{CS}$ = V_{IL} Iout = 0 mA, min cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby Vcc current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V 0 V ≤ Vin ≤ 0.2V or Vcc – 0.2 V ≤ Vin
		—	0.02*2	0.1*2	mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	8	pF	Vout = 0 V

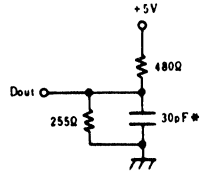
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

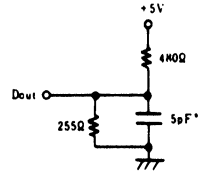
Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B) (for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

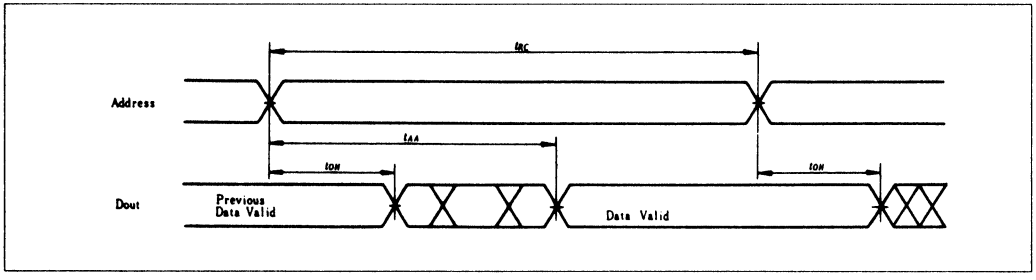


Note: Including scope & jig

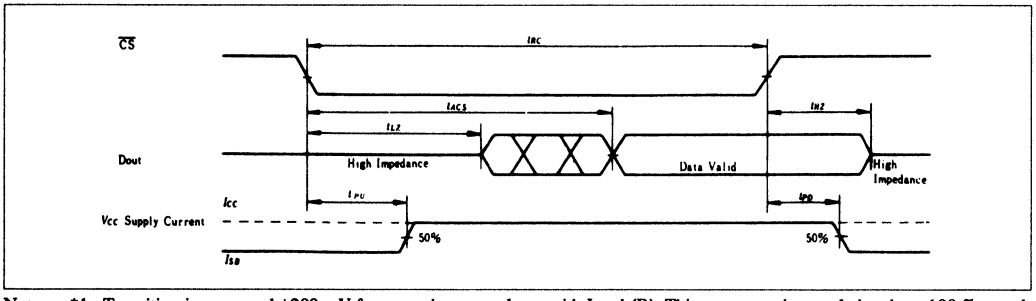
Read Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	12	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Read Timing Waveform (1) *2, *3, *5



Read Timing Waveform (2) *2, *4

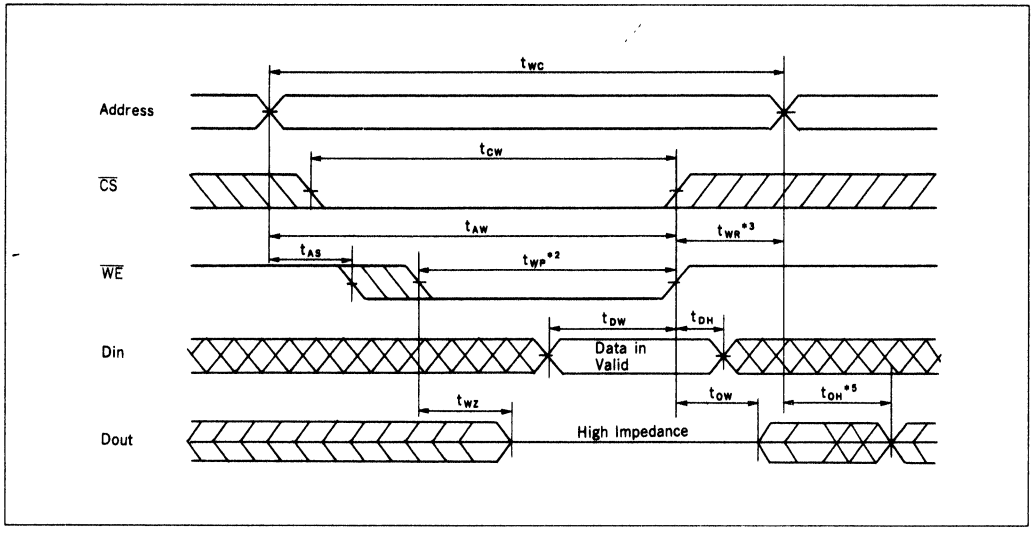


Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100 % tested.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. All read cycle timing are referenced from last valid address to the first transitioning address.

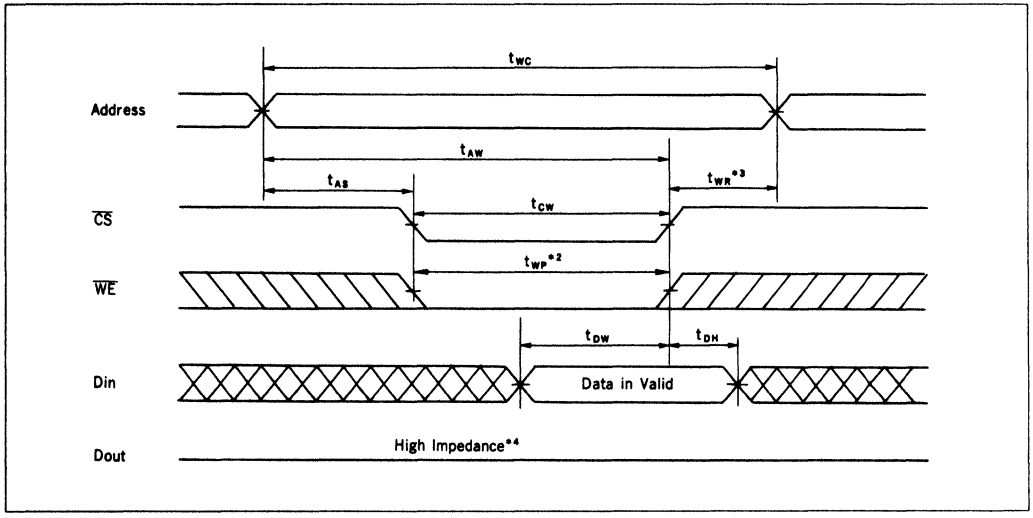
Write Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}*1	0	8	0	10	ns
Output active from end of write	t_{OW}*1	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{WE}$ controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

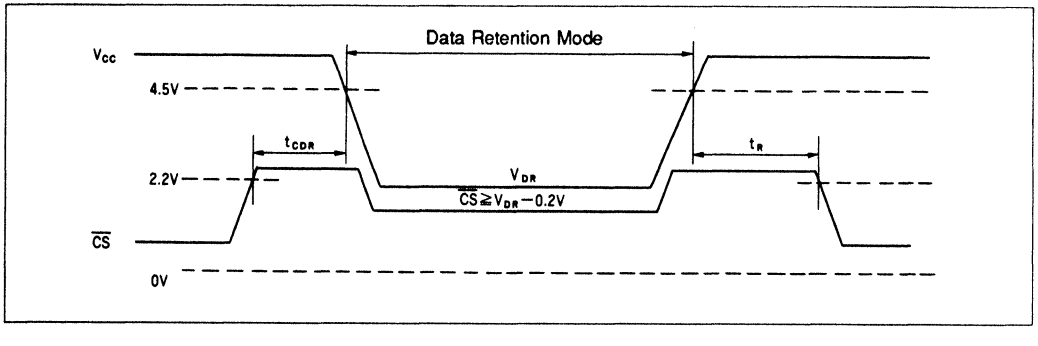
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

(This specification is guaranteed only for L-version.)

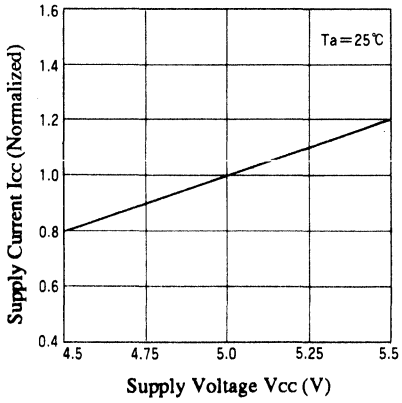
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Notes: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

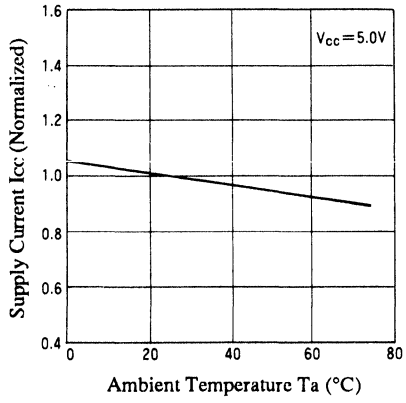
Low Vcc Data Retention Timing Waveform



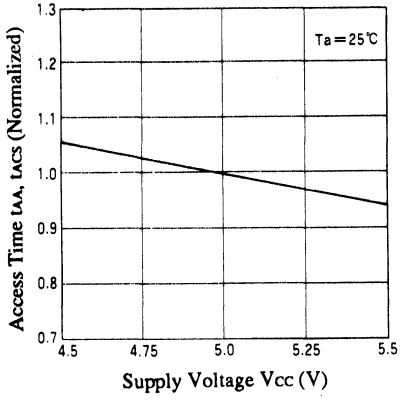
Supply Current vs. Supply Voltage



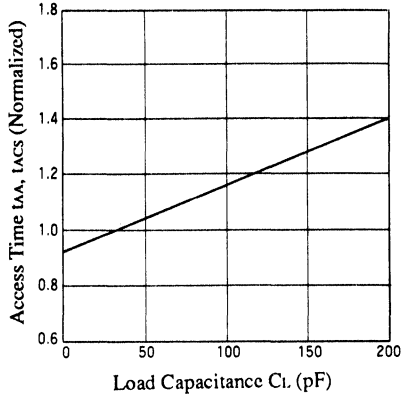
Supply Current vs. Ambient Temperature



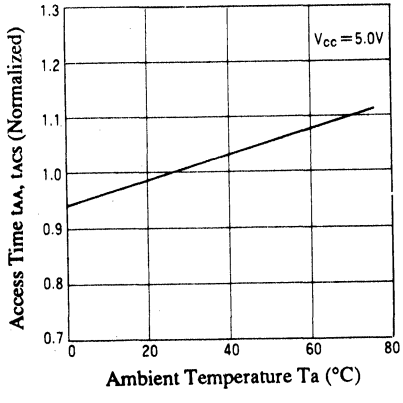
Access Time vs. Supply Voltage



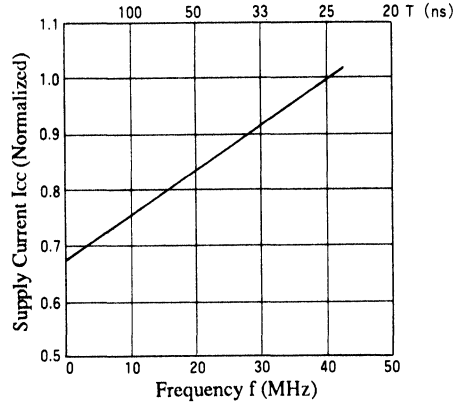
Access Time vs. Load Capacitance



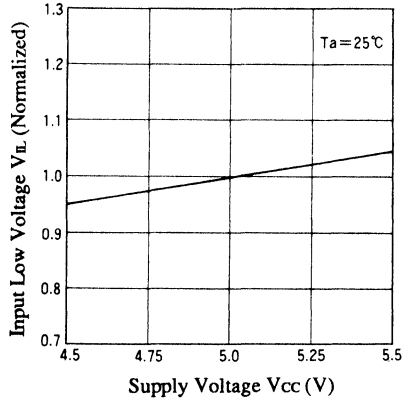
Access Time vs. Ambient Temperature



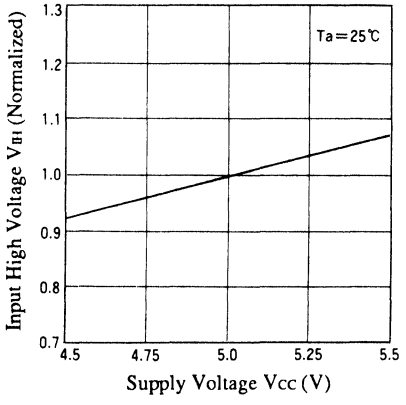
Supply Current vs. Frequency



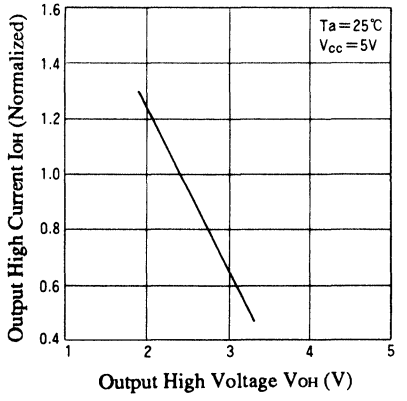
Input Low Voltage vs. Supply Voltage



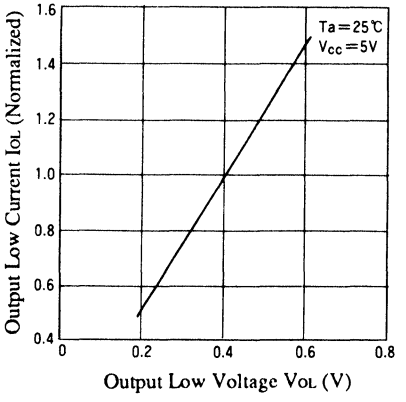
Input High Voltage vs. Supply Voltage



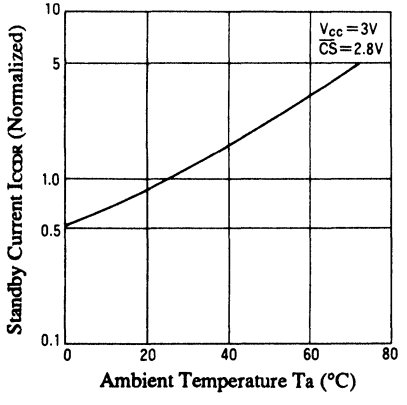
Output Current vs. Output Voltage (1)



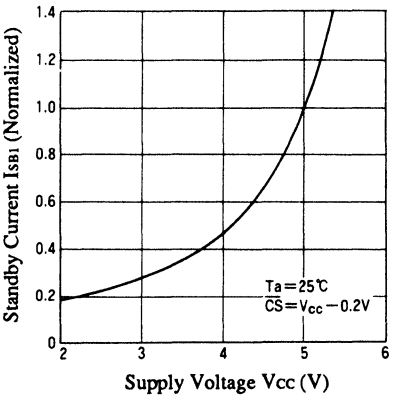
Output Current vs. Output Voltage (2)



Standby Current vs. Ambient Temperature



Standby Current vs. Supply Voltage



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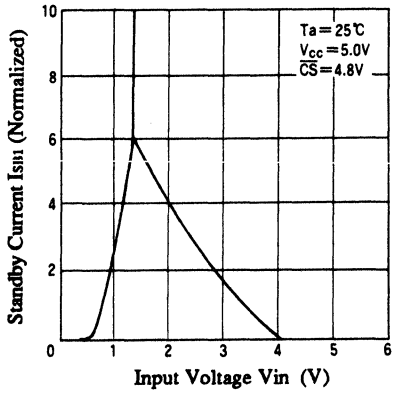
Standby Current vs. Input Voltage



HM6787 Series

Maintenance Only

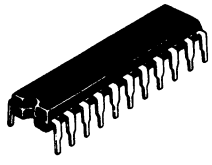
Refer to HM6787HA Series

65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

■ FEATURES

- Super Fast Access Time: 25ns/30ns (max.)
- Low Power Dissipation (DC):
  Operating 180mW (typ)
- High Driving Capability: I_{OL} 16mA
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- Skinny 22-pin Plastic Dip (300 mil) and 22-pin Chip Carrier

HM6787P Series



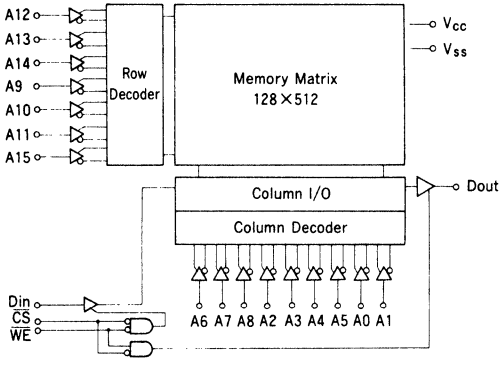
(DP-22NB)

2

■ ORDERING INFORMATION

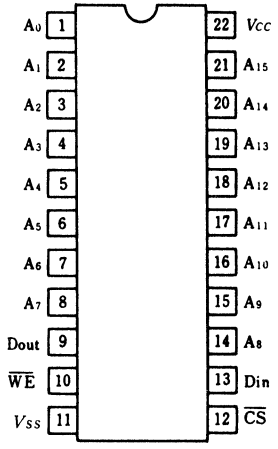
Type No.	Access Time	Package
HM6787P-25	25ns	300 mil 22 pin
HM6787P-30	30ns	Plastic DIP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

- HM6787P Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}	Dout
L	L	Write	I_{CC}	High Z

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	-0.5*1	–	0.8	V

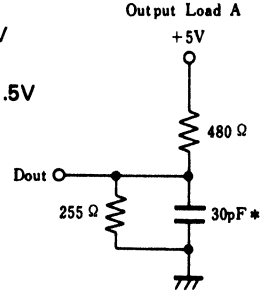
Note) *1. -3.0V for pulse width $\leqq$ 20ns.

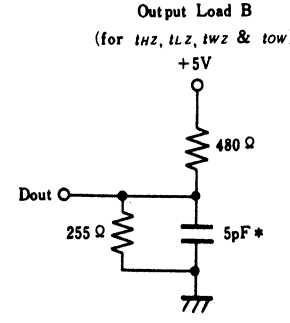
■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to +70°C)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	–	40	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}$ -0.2V $V_{IN} \leqq$ 0.2V or $V_{IN} \geqq V_{CC}$ -0.2V	–	–	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 16mA	–	–	0.5	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	–	–	V

■ AC TEST CONDITIONS

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure





* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	7.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

• READ CYCLE

Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	
Address Access Time	t_{AA}	–	25	–	30	ns	
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	2
Chip Deselection to Power Down Time	t_{PD}	–	25	–	30	ns	2
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	3

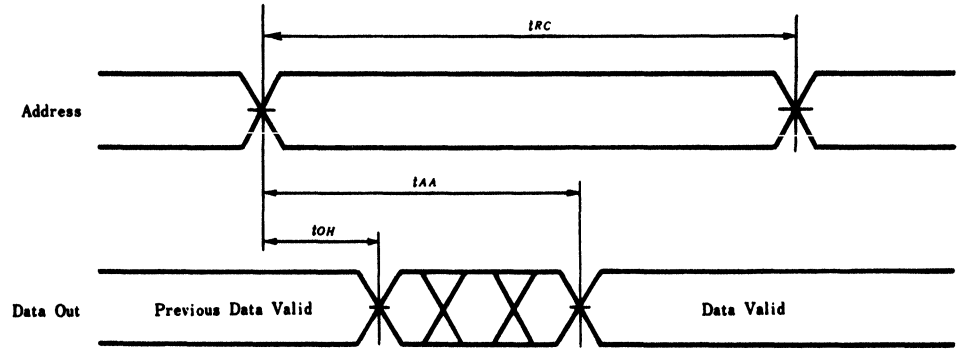
Notes) 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
2. This parameter is sampled and not 100% tested.
3. If t_T becomes more than 150ns, there is possibility of function fail.
Please contact your nearest Hitachi's Sale Dept. regarding specification.

• WRITE CYCLE

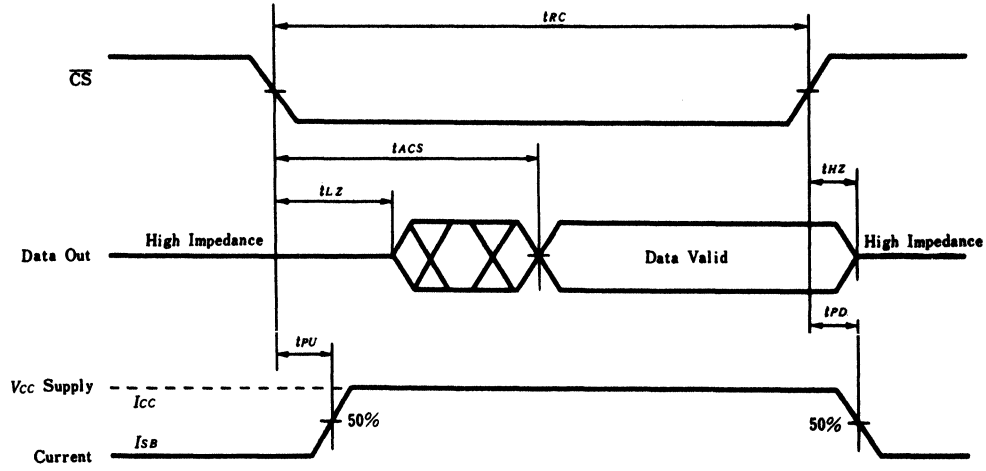
Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	25	–	30	–	ns	2
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	5	–	5	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1[1), 2)]

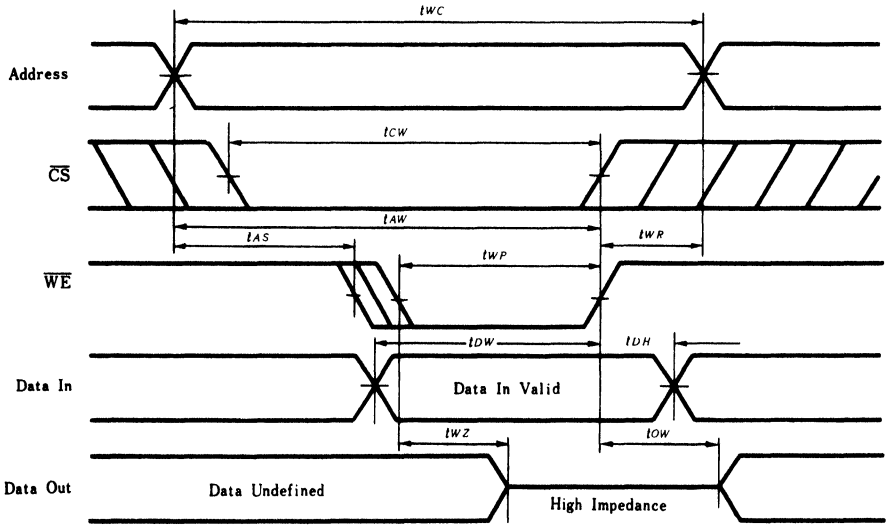


• TIMING WAVEFORM OF READ CYCLE NO. 2[1), 3)]



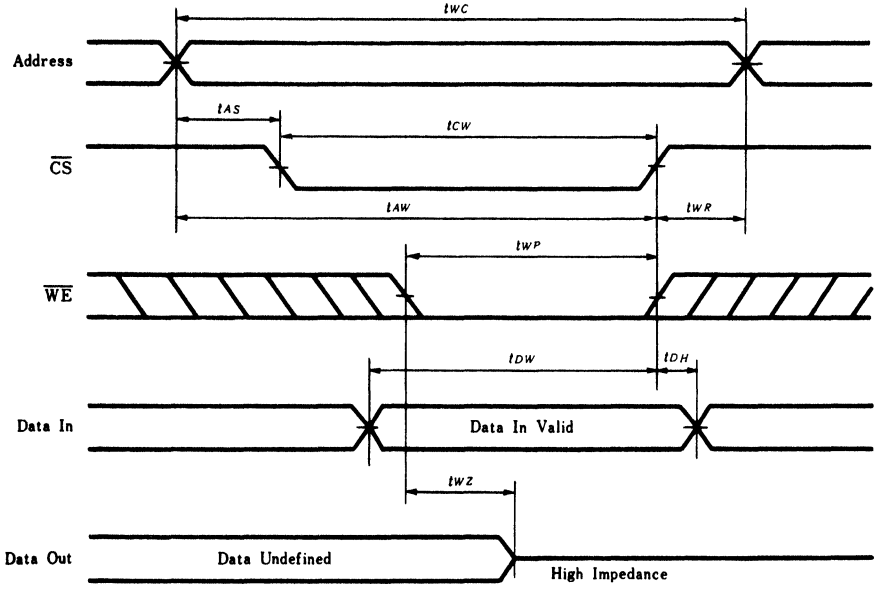
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

HM6787H Series — Maintenance Only

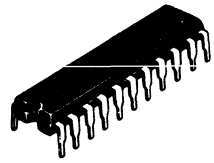
Refer to HM6787HA Series

65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

Features

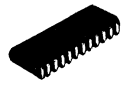
- Super Fast Access Time: 15ns/20ns (max.)
- Low Power Dissipation (DC):
  Operating 210mW (typ)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6787HP Series



(DP-22NB)

HM6787HJP Series

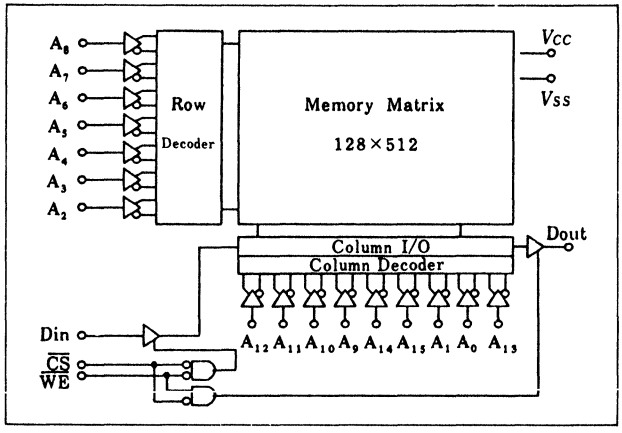


(CP-24D)

Ordering Information

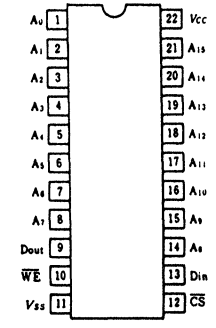
Type No.	Access Time	Package
HM6787HP-15	15ns	300 mil 22 pin
HM6787HP-20	20ns	Plastic DIP
HM6787HJP-15	15ns	300 mil 24 pin
HM6787HJP-20	20ns	Plastic SOJ

Block Diagram



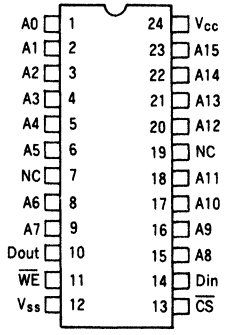
Pin Arrangement

HM6787HP Series



(Top View)

HM6787HJP Series



Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Dout
L	L	Write	I_{CC}, I_{CC1}	High Z

Recommended DC Operating Conditions ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

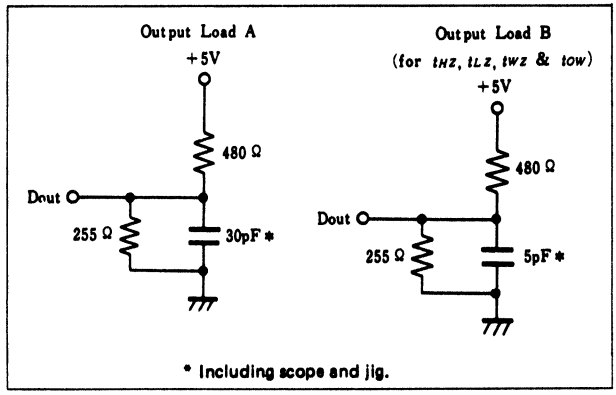
Note) *1. −3.0V for pulse width ≦ 10ns.

DC and Operating Characteristics (V_{CC} = 5V±10%, T_a = 0°C to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, I_{OUT}=0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100% I_{OUT}=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4mA

AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2

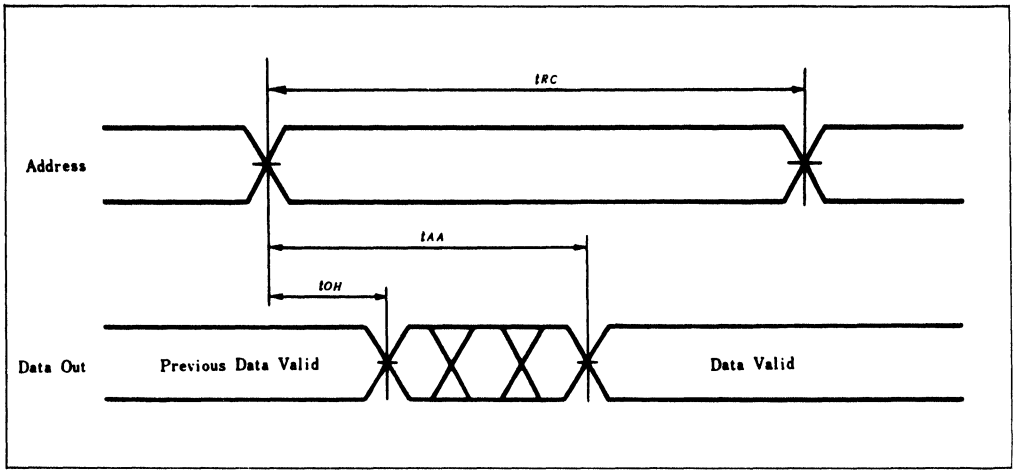
Note: 1. This parameter is sampled and 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Write Cycle

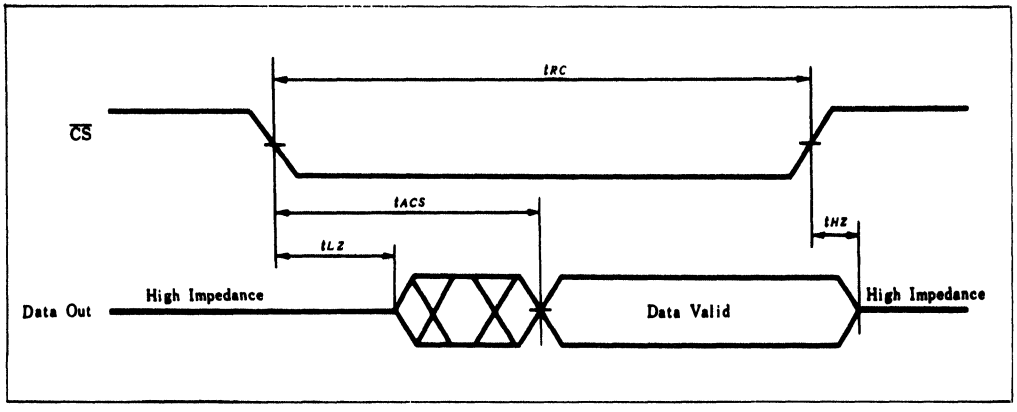
Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	3	–	3	–	ns	
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Timing Waveform of Read Cycle No. 1[1), 2)]

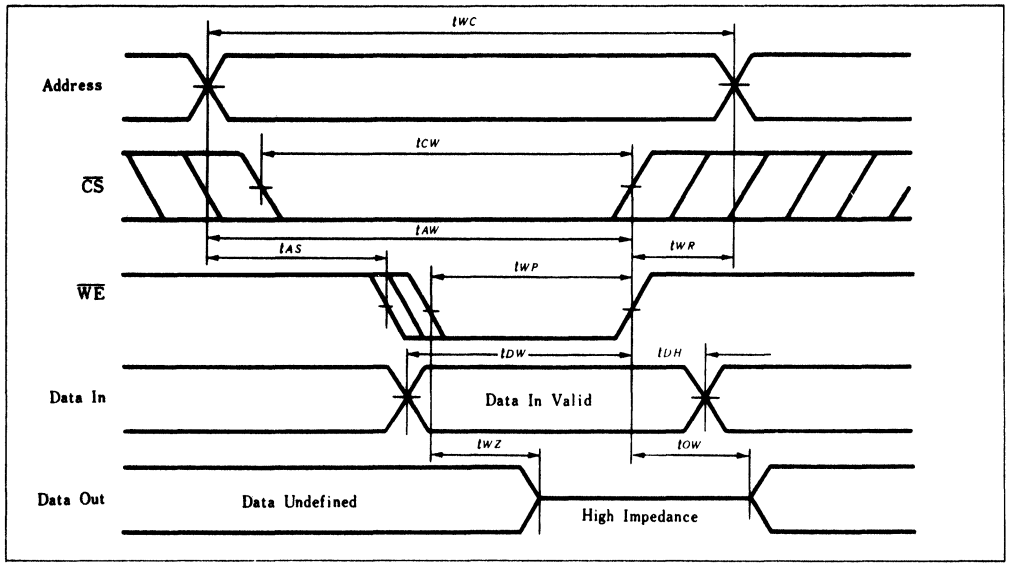


Timing Waveform of Read Cycle No. 2[1), 3)]



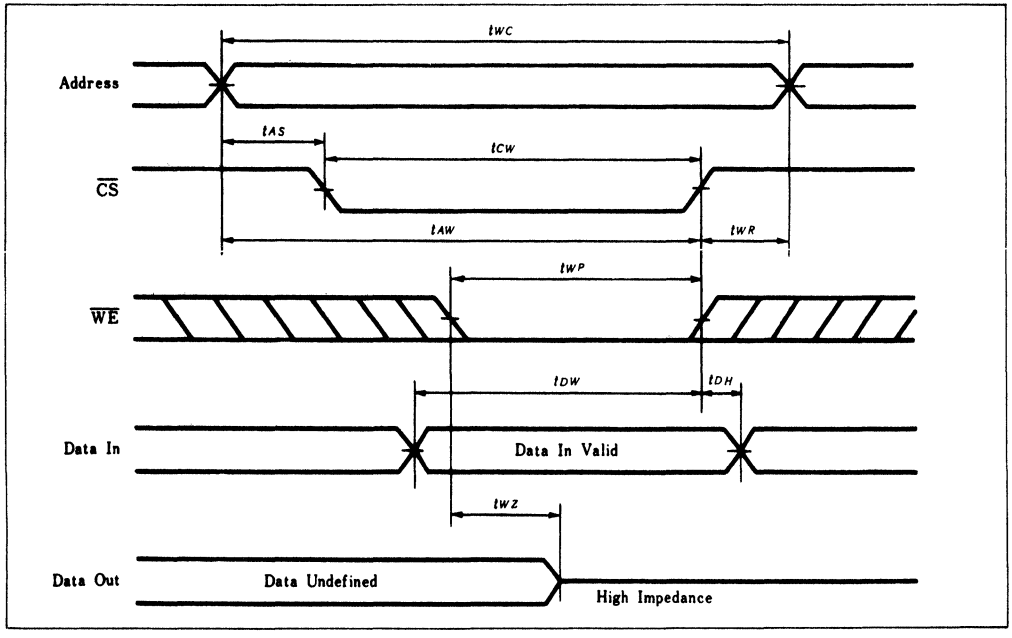
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

HM6787HA Series

65,536-Word x 1-Bit High Speed Static Random Access Memory

■ FEATURES

- 65,536-Words x 1 bit organization
- 1.3 μm Hi-BiCMOS process
- Super fast
  Access time 12/15/20 ns (max.)
- Low power dissipation
  (DC) operating: 300mW (typ)
- +5V single supply
- Completely static memory
  No clock or timing strobe required
- Fully TTL compatible input and output

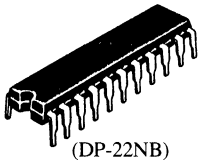
■ ORDERING INFORMATION

Type No.	Cycle Time	Package
HM6787HAP-12 HM6787HAP-15 HM6787HAP-20	12 ns 15 ns 20 ns	300-mil, 22 pin Plastic DIP (DP-22NB)
HM6787HAJP-12 HM6787HAJP-15 HM6787HAJP-20	12 ns 15 ns 20 ns	300-mil, 24 pin Plastic SOJ (CP-24D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{15}	Address Input
D_{in}	Data Input
D_{out}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{SS}	Ground
V_{CC}	Supply Voltage

■ PACKAGE OUTLINE

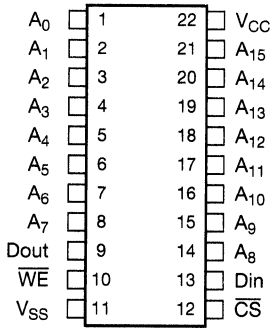


(DP-22NB)

(CP-24D)

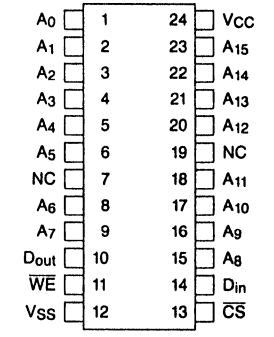
■ PIN ARRANGEMENT

HM6787HAP Series



(Top View)

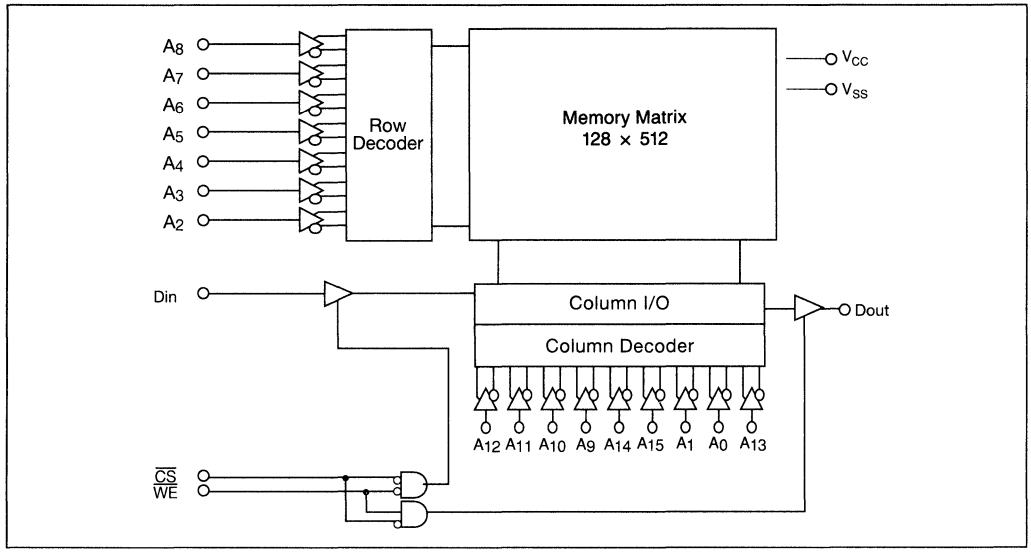
HM6787HAJP Series



(Top View)

2

■ BLOCK DIAGRAM



■ TRUTH TABLE

Input		Output	Mode	V_{CC} Current
$\overline{CS}$	$\overline{WE}$			
H	X	High Z	Not Selected	I_{SB}, I_{SB1}
L	H	D_{out}	Read	I_{CC}, I_{CC1}
L	L	High Z	Write	I_{CC}, I_{CC1}

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	–0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg} (bias)	–10 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	–3.0[1]	—	0.8	V

Notes 1. Pulse width 10 ns, DC: –0.5V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	2	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT}= 0V to V_{CC}	—	—	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT}= 0 mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle Duty: 100%, I_{OUT} = 0 mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN}= V_{IH} or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} –0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} –0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

• Read Cycle

Item	Symbol	HM6787HA-12		HM6787HA-15		HM6787HA-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns
Address Access Time	t_{AA}	—	12	—	15	—	20	ns
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns
Chip Selection to Output in Low Z	t_{LZ}[1, 2]	3	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}[1, 2]	0	6	0	6	0	8	ns

Notes 1.This parameter is sampled and not 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

• Write Cycle

Item	Symbol	HM6787HA-12		HM6787HA-15		HM6787HA-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}[1]	12	—	15	—	20	—	ns
Chip Selection to End of Write	t_{CW}	8	—	10	—	13	—	ns
Address Valid to End of Write	t_{AW}	8	—	10	—	13	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	8	—	10	—	13	—	ns
Write Recovery Time ($\overline{WE}$)	t_{WR}	0.5	—	0.5	—	0.5	—	ns
Write Recovery Time ($\overline{CS}$)	t_{WR1}	1	—	1	—	1	—	ns
Data Valid to End of Write	t_{DW}	7	—	8	—	10	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[2, 3]	0	6	0	6	0	8	ns
Output Active from End of Write	t_{OW}[2, 3]	3	—	3	—	3	—	ns

Notes 1. All Write Cycle timings are referenced from the last valid address to the first transitioning address
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

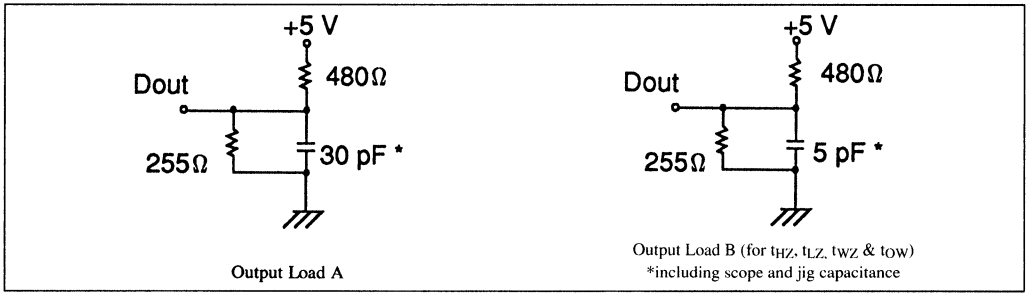
• Capacitance (T_a = 25°C, f = 1 MHz)

Item	Symbol	Max	Unit	Test Condition
Input Capacitance	C_{in}[1]	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}[1]	10	pF	V_{OUT} = 0V

Notes 1. This parameter is sampled and not 100% tested.

■ AC TEST CONDITIONS

- Input pulse levels: V_{SS} to 3.0V
- Input timing reference levels: 1.5V
- Output load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5V

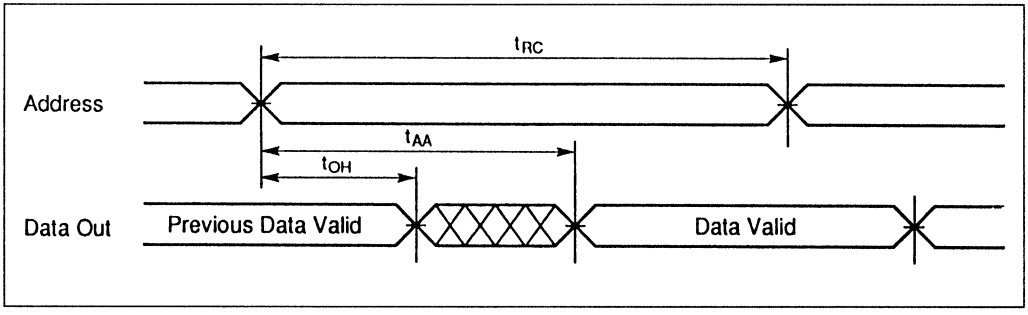


Output Load A

Output Load B (for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})
*including scope and jig capacitance

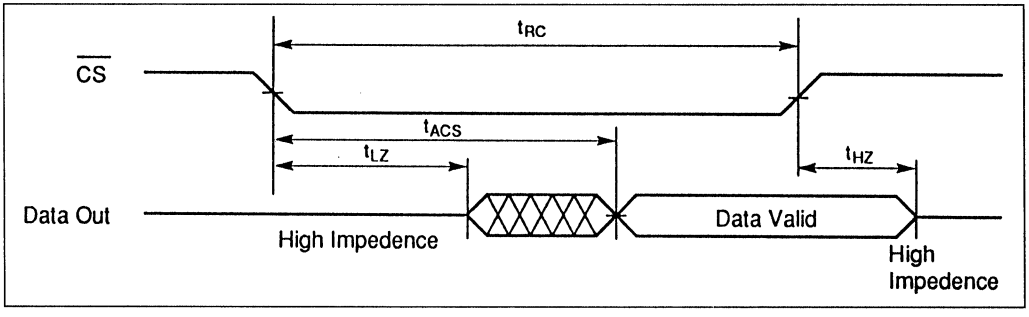
■ TIMING WAVEFORMS

- **Read Cycle –1[1, 2]**



Notes 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

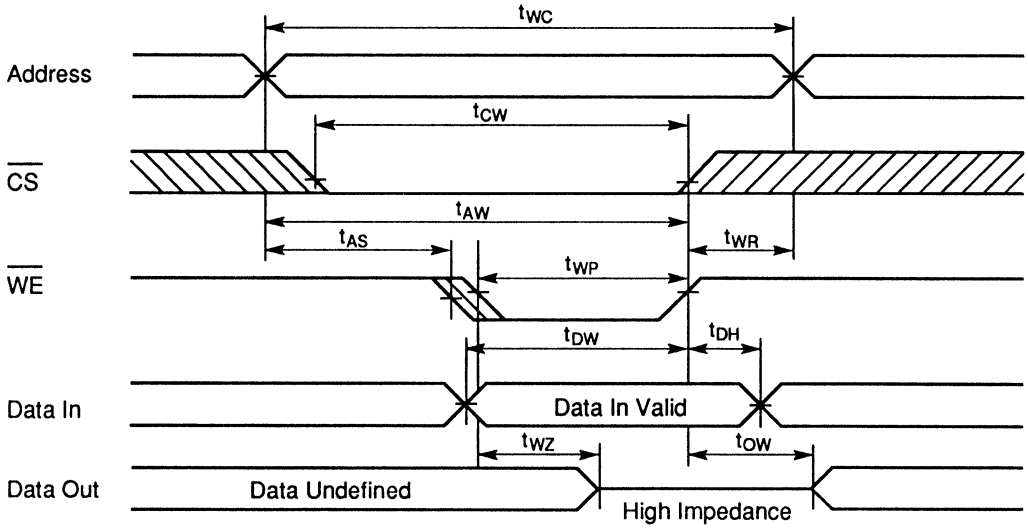
- **Read Cycle –2[1, 2, 3]**



Notes 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

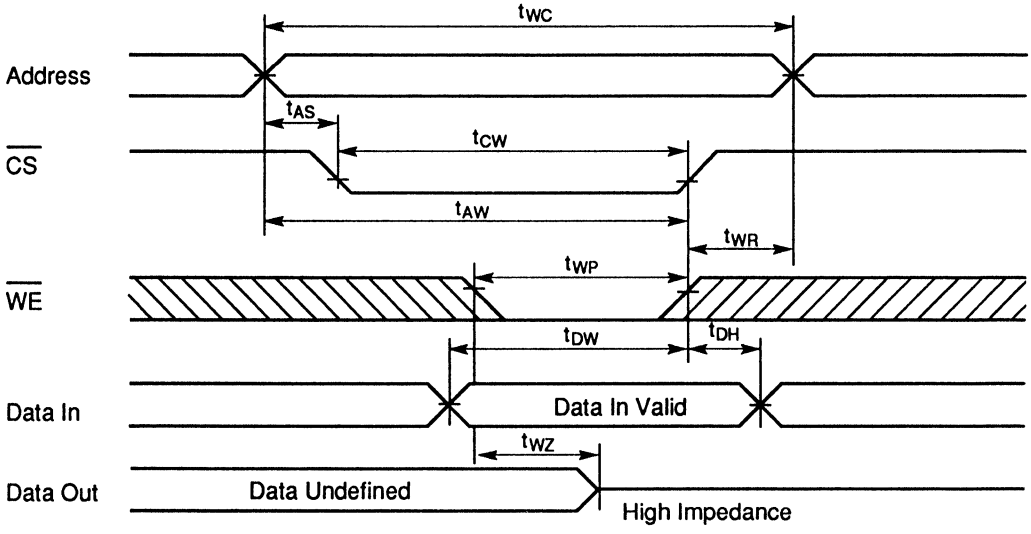
■ TIMING WAVEFORMS

• **Write Cycle –1**[1] ($\overline{WE}$ Controlled)



NOTE: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle –2**[1] ($\overline{CS}$ Controlled)



NOTE: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

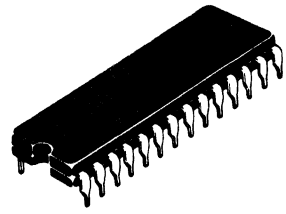
HM62256 Series

32768-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

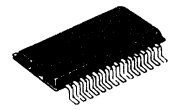
- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 200μW (typ)/10μW (typ) (L-version),
  Operation: 40mW (typ.) (f = 1MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/L-SL version)

HM62256P Series



(DP-28)

HM62256FP Series

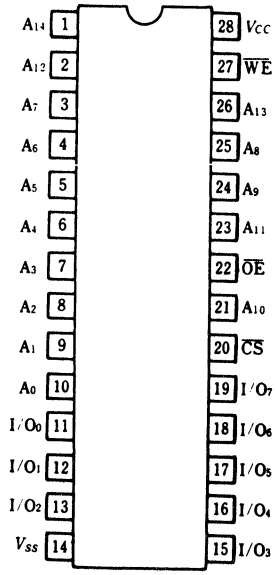


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62256P-8	85ns	600 mil 28 pin Plastic DIP
HM62256P-10	100ns	
HM62256P-12	120ns	
HM62256P-15	150ns	
HM62256LP-8	85ns	
HM62256LP-10	100ns	
HM62256LP-12	120ns	
HM62256LP-15	150ns	
HM62256LP-10SL	100ns	
HM62256LP-12SL	120ns	
HM62256LP-15SL	150ns	
HM62256FP-8T	85ns	28 pin Plastic SOP
HM62256FP-10T	100ns	
HM62256FP-12T	120ns	
HM62256FP-15T	150ns	
HM62256LFP-8T	85ns	
HM62256LFP-10T	100ns	
HM62256LFP-12T	120ns	
HM62256LFP-15T	150ns	
HM62256LFP-10SLT	100ns	
HM62256LFP-12SLT	120ns	
HM62256LFP-15SLT	150ns	

■ PIN ARRANGEMENT



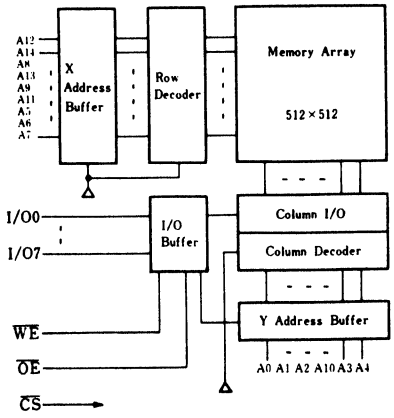
(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.0V for pulse width ≦ 50ns

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item		Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current		$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current		$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	8	15	mA
Average Operating Power Supply Current	HM62256-8	I_{CC1}	Min. Cycle, duty=100%, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	50	70	mA
	HM62256-10			–	40	70	
	HM62256-12			–	35	70	
	HM62256-15			–	33	70	
		I_{CC2}	$\overline{CS}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0V, $I_{I/O}$ = 0mA, f = 1MHZ	–	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS}$ = V_{IH}	–	0.5	3	mA
		I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V, 0V ≦ V_{IN}	–	0.04	2	mA
				–	2*2	100*2	μA
				–	2*3	50*3	
Output Voltage		V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
		V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V

Notes) *1. Typical values are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

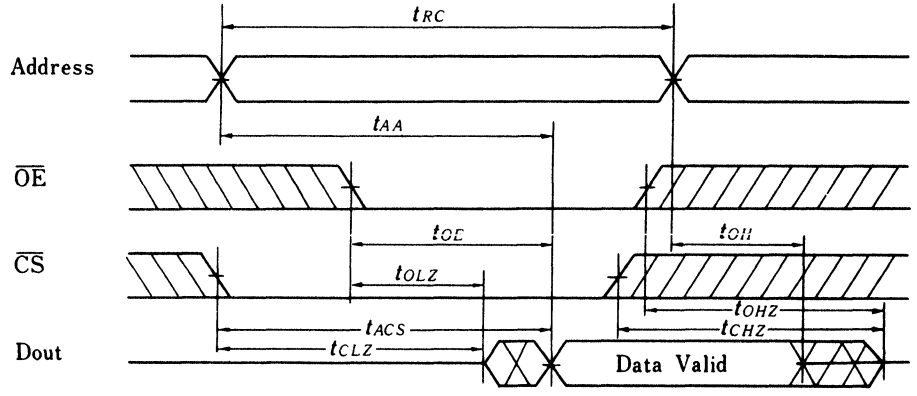
■ AC CHARACTERISTICS (V_{CC}=5V± 10%, T_a=0 to +70°C unless otherwise noted)

- **AC Test Conditions**
  - ○ Input pulse levels: 0.8V to 2.4V
  - ○ Input rise and fall times: 5ns
  - ○ Input and Output timing reference levels: 1.5V
  - ○ Output load: 1TTL Gate and C_L (100pF) (Including scope and jig)

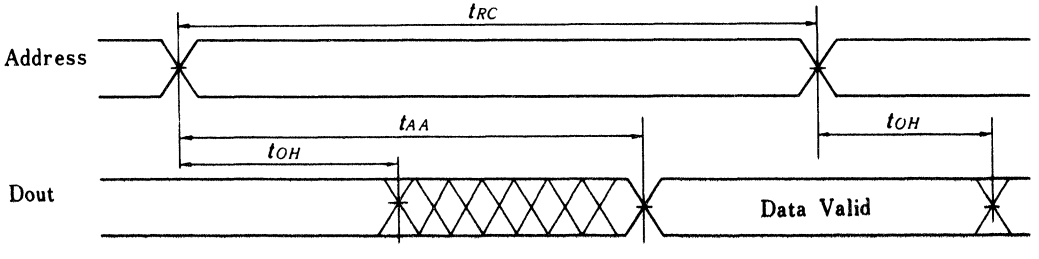
- **Read Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	–	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	85	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	45	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

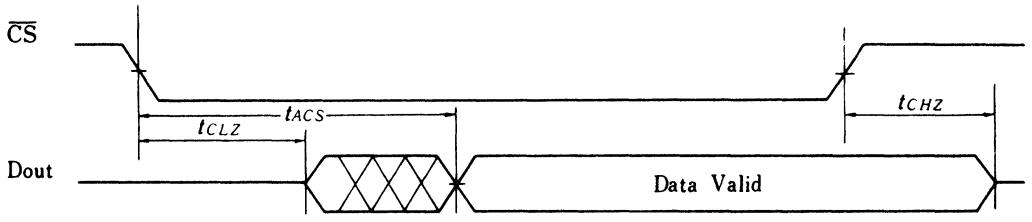
- **Timing Waveform of Read Cycle No. 1[1]**



- **Timing Waveform of Read Cycle No. 2[1][2][4]**



- **Timing Waveform of Read Cycle No. 3[1][3][4]**

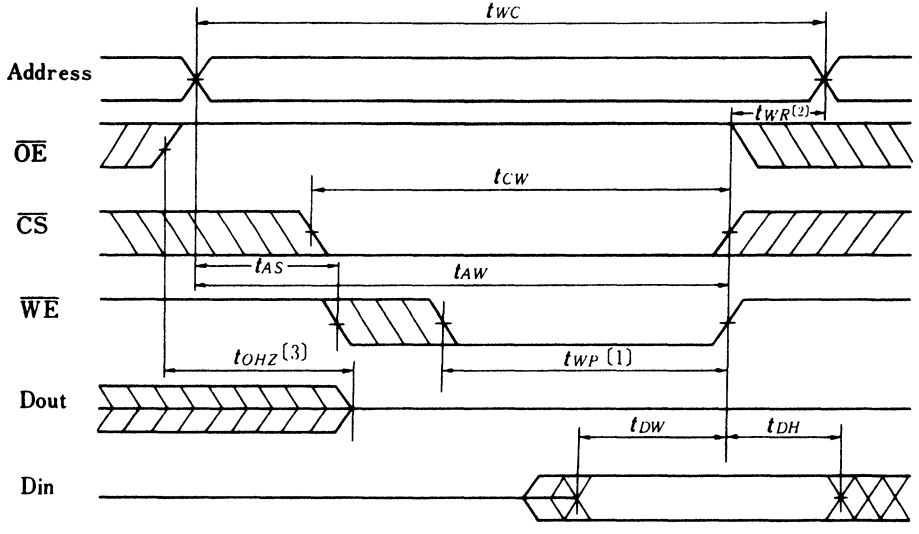


Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

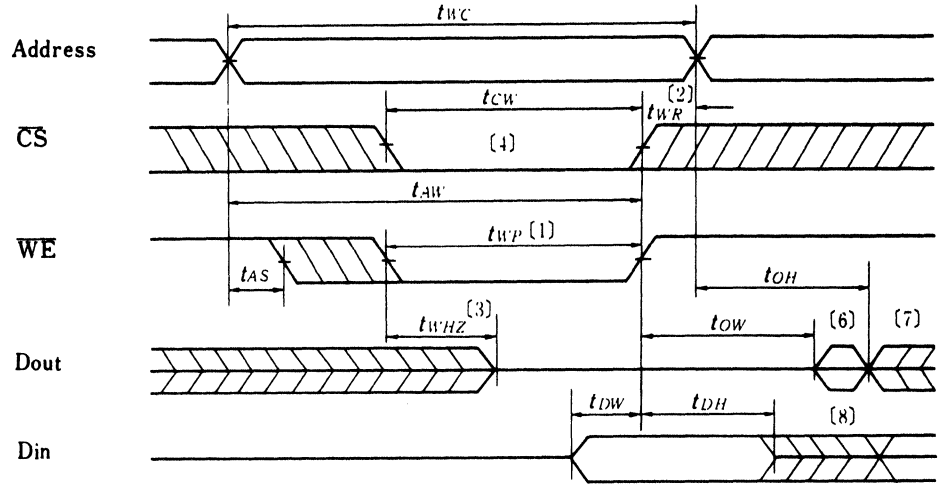
- **Write Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	–	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	75	–	80	–	85	–	100	–	ns
Address Valid to End of Write	t_{AW}	75	–	80	–	85	–	100	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	60	–	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns

- **Timing Waveform of Write Cycle No. 1 ($\overline{OE}$ Clock)**



- **Timing Waveform of Write Cycle No. 2[5] ($\overline{OE}$ Low Fixed)**



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

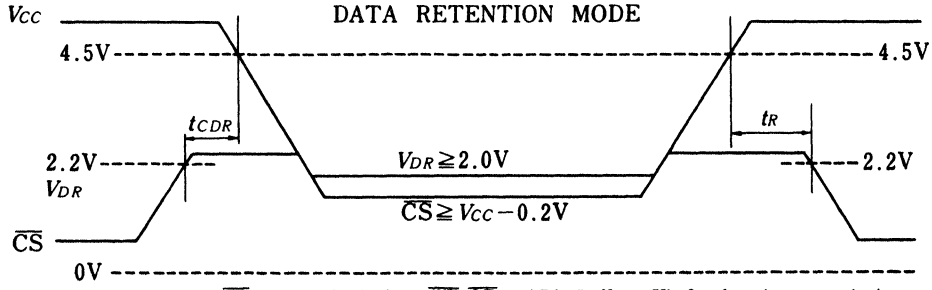
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

(This characteristics is guaranteed only for L-and L-SL version)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Date Retention	V_{DR}	$\overline{CS} \geqq V_{CC}$ –0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geqq$ 2.8V 0V ≦ V_{in}	–	–	50*2	μA
			–	–	10*3	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

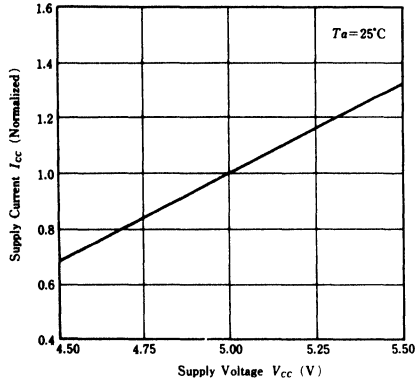
Note) *1. t_{RC} = Read Cycle Time
*2. This characteristic is guaranteed only for L-version, 20μA max. at T_a = 0 to 40°C.
*3. This characteristic is guaranteed only for L-SL version, 3μA max. at T_a = 0 to 40°C.

- **Low V_{CC} Data Retention Waveform**

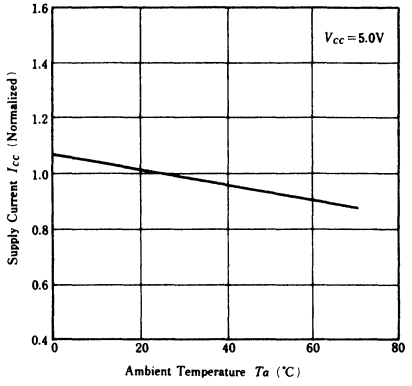


Note) In Data Retention Mode, $\overline{CS}$ controls the Address, $\overline{WE}$, $\overline{OE}$, and Din Buffers. *Vin* for these inputs can be in high impedance state in data retention mode.

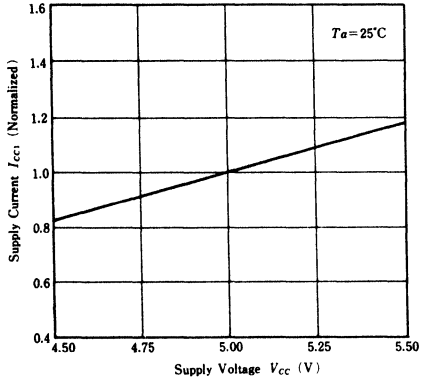
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1)



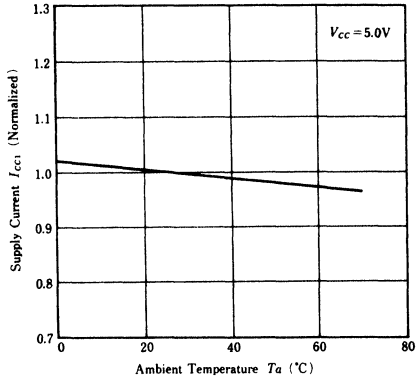
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (1)



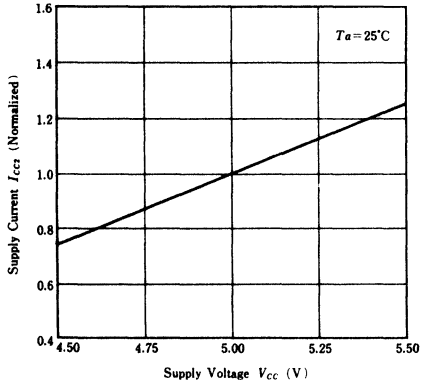
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2)



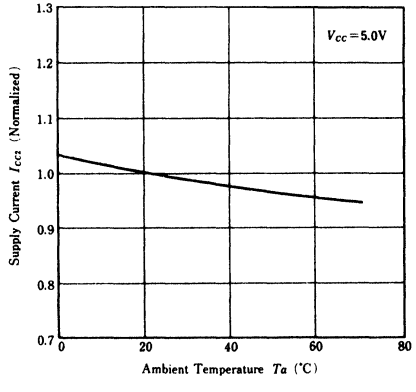
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (2)



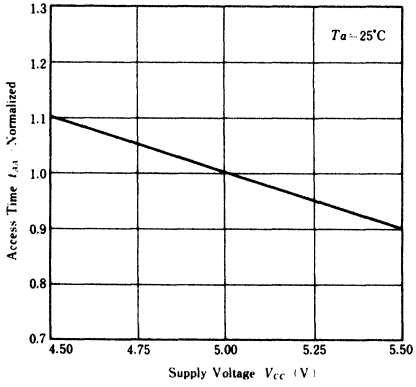
SUPPLY CURRENT vs. SUPPLY VOLTAGE (3)



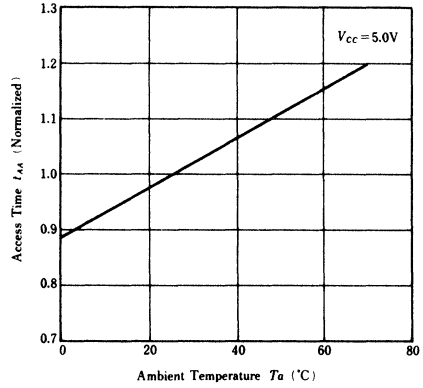
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (3)



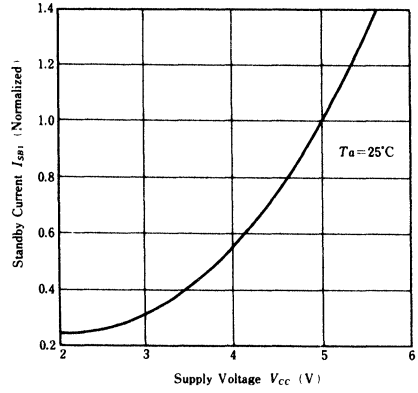
ACCESS TIME vs. SUPPLY VOLTAGE



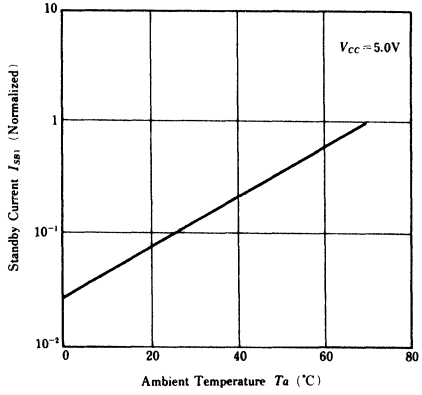
ACCESS TIME vs. AMBIENT TEMPERATURE



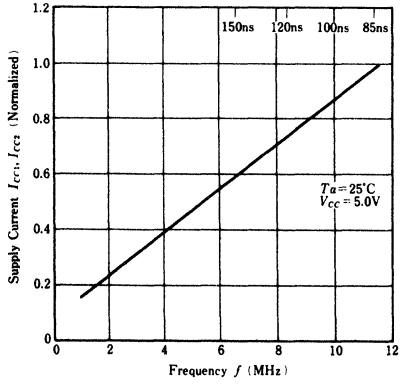
STANDBY CURRENT vs. SUPPLY VOLTAGE



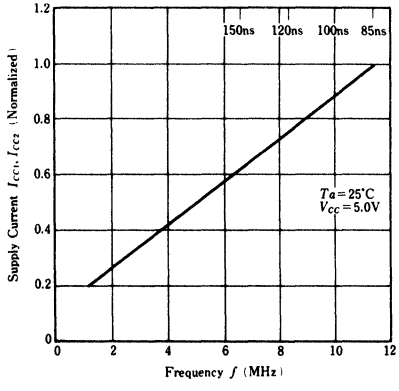
STANDBY CURRENT vs. AMBIENT TEMPERATURE



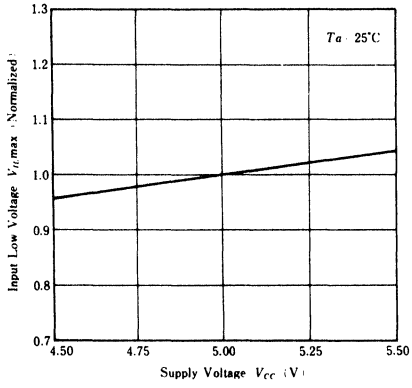
SUPPLY CURRENT vs. FREQUENCY (READ)



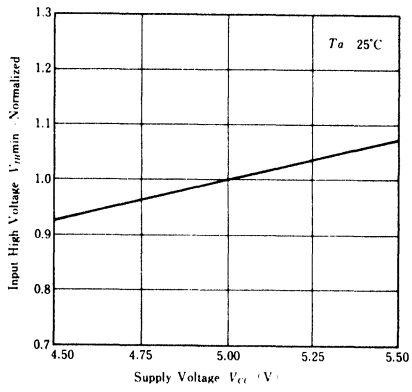
SUPPLY CURRENT vs. FREQUENCY (WRITE)



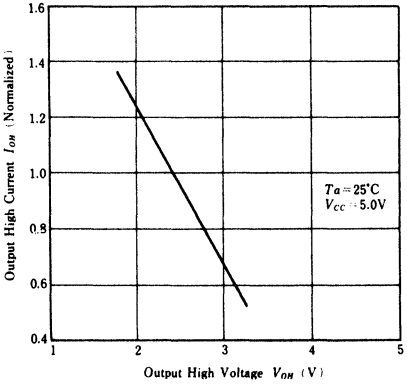
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



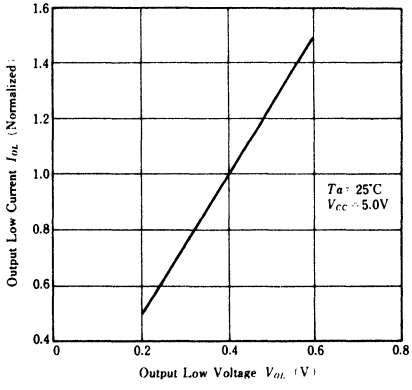
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



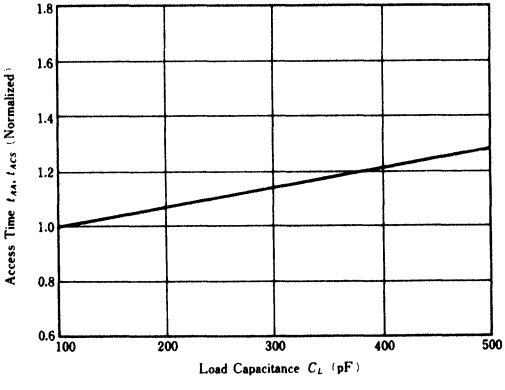
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME vs. LOAD CAPACITANCE



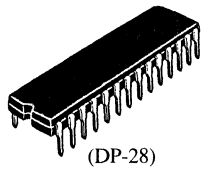
HM62256A Series

Preliminary

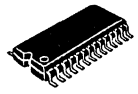
32,768-Word x 8-Bit High Speed CMOS Static RAM

■ DESCRIPTION

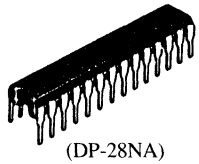
The Hitachi HM62256A is a CMOS static RAM organized 32k-word x 8-bit. It realizes higher performance and low power consumption by employing 0.8 μm HI-CMOS process technology. The device, packaged in a 8 x 14 mm TSOP with thickness of 1.2 mm, 450-mil SOP (foot print pitch width), 600-mil plastic DIP, or 300-mil plastic DIP, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided. It offers power standby power dissipation; therefore, it is suitable for battery back up system.



(DP-28)



(FP-28DA)



(DP-28NA)

(TFP-32DA)

■ FEATURES

- High speed:
  Fast access time 85/100/120/150 ns (max.)
- Low power
  Standby: 10 μW (typ.) (L/L-SL version)
  Operation: 40 mW (typ.) (f = 1 MHz)
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation

■ ORDERING INFORMATION

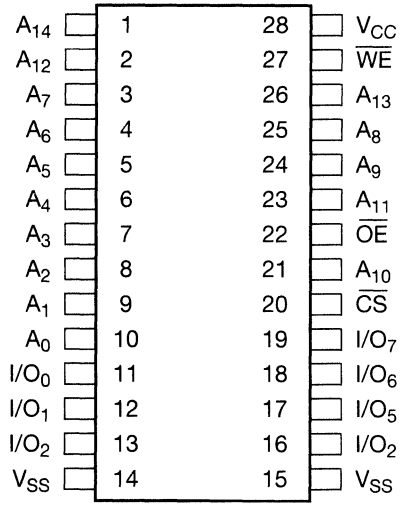
Type No.	Access Time	Package
HM62256AP-8	85 ns	
HM62256AP-10	100 ns	
HM62256AP-12	120 ns	
HM62256AP-15	150 ns	
HM62256ALP-8	85 ns	600-mil 28-Pin Plastic DIP (DP-26)
HM62256ALP-10	100 ns	
HM62256ALP-12	120 ns	
HM62256ALP-15	150 ns	
HM62256ALP-8SL	85 ns	
HM62256ALP-10SL	100 ns	
HM62256ALP-12SL	120 ns	
HM62256ALP-15SL	150 ns	
HM62256ASP-8	85 ns	
HM62256ASP-10	100 ns	
HM62256ASP-12	120 ns	
HM62256ASP-15	150 ns	
HM62256ALSP-8	85 ns	300-mil 28-Pin Plastic DIP (DP-28NA)
HM62256ALSP-10	100 ns	
HM62256ALSP-12	120 ns	
HM62256ALSP-15	150 ns	
HM62256ALSP-8SL	85 ns	
HM62256ALSP-10SL	100 ns	
HM62256ALSP-12SL	120 ns	
HM62256ALSP-15SL	150 ns	
HM62256AFP-8T	85 ns	
HM62256AFP-10T	100 ns	
HM62256AFP-12T	120 ns	
HM62256AFP-15T	150 ns	
HM62256ALFP-8T	85 ns	450-mil 28-Pin Plastic SOP (FP-28DA)
HM62256ALFP-10T	100 ns	
HM62256ALFP-12T	120 ns	
HM62256ALFP-15T	150 ns	
HM62256ALFP-8SLT	85 ns	
HM62256ALFP-10SLT	100 ns	
HM62256ALFP-12SLT	120 ns	
HM62256ALFP-15SLT	150 ns	

■ TSOP SERIES

Type No.	Access Time	Package
HM62256ALT-8	85 ns	
HM62256ALT-10	100 ns	
HM62256ALT-12	120 ns	8 mm x 14 mm 32-Pin TSOP (Normal Type) (TFP-32DA)
HM62256ALT-15	150 ns	
HM62256ALT-8SL	85 ns	
HM62256ALT-10SL	100 ns	
HM62256ALT-12SL	120 ns	
HM62256ALT-15SL	150 ns	
HM62256ALR-8	85 ns	
HM62256ALR-10	100 ns	
HM62256ALR-12	120 ns	8 mm x 14 mm 32-Pin TSOP (Reverse Type) (TFP-32DAR)
HM62256ALR-15	150 ns	
HM62256ALR-8SL	85 ns	
HM62256ALR-10SL	100 ns	
HM62256ALR-12SL	120 ns	
HM62256ALR-15SL	150 ns	

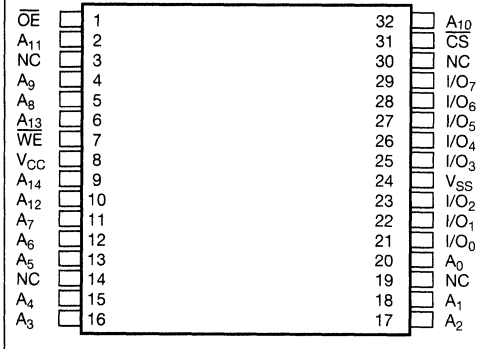
■ PIN ARRANGEMENT

HM62256AP/AFP/ASP Series



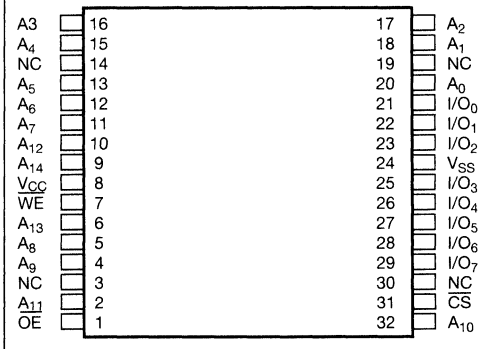
(Top View)

HM62256AT Series



(Top View)

HM62256AR Series



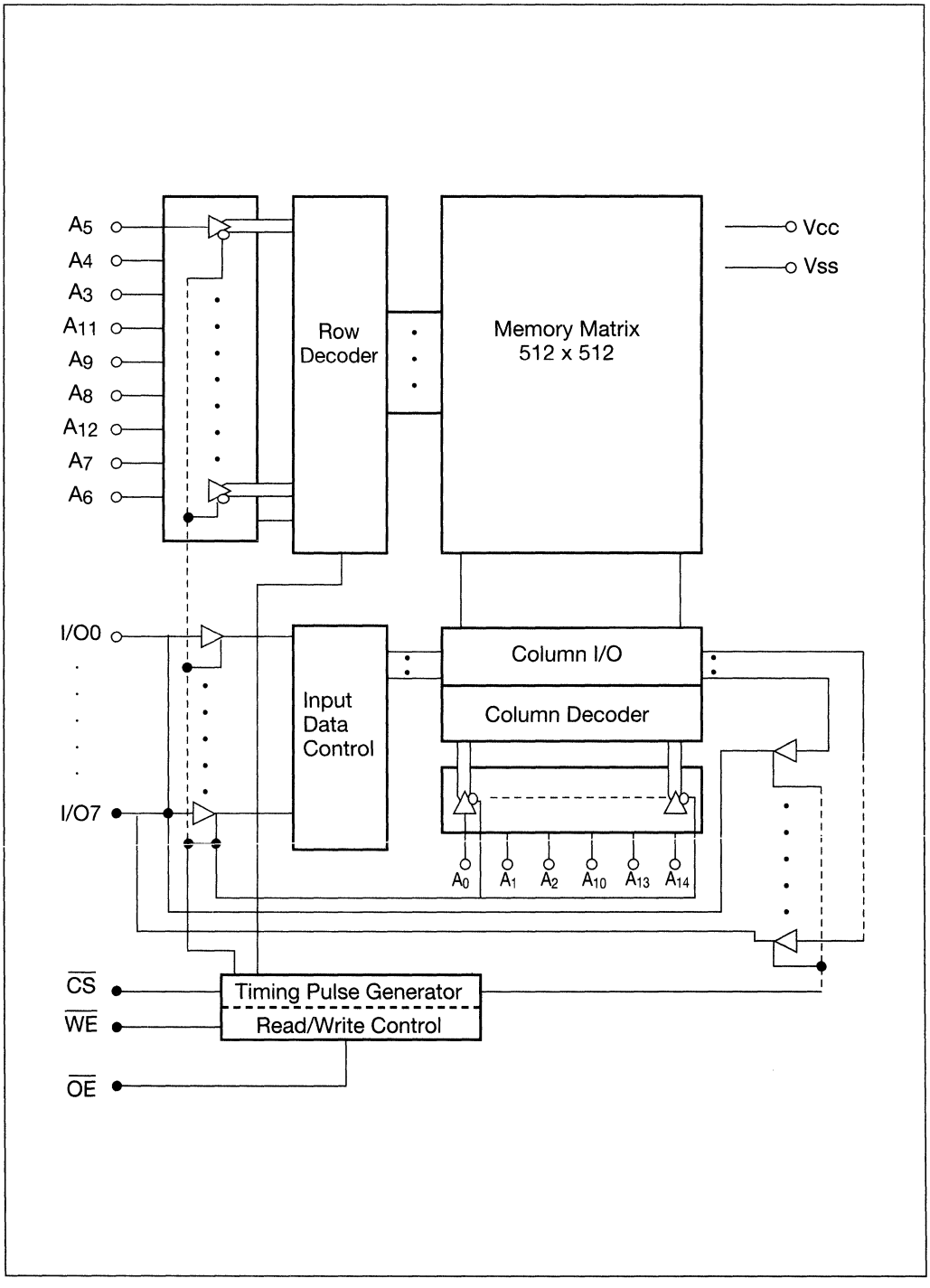
(Top View)

■ PIN DESCRIPTION

Symbol	Function
A_0–A_{14}	Address
I/O_0-I/O_7	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
NC	No Connection
V_{CC}	Power Supply
V_{SS}	Ground

2

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
X	H	X	Not Selected	I_{SS}, I_{SS1}	High-Z	—
H	L	H	Output Disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	D_{out}	Read Cycle
L	L	H	Write	I_{CC}	D_{in}	Write Cycle (1)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (2)

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5^{*1} to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_T min = −3.0 V for pulse half-width ≤ 50 ns

■ RECOMMENDED DC OPERATION CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	5.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5^{*1}	—	0.8	V

Note: 1. V_{IL} min = −3.0 V for pulse half-width ≤ 50 ns

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	Min.	Typ[1]	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	1	µA	V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{SS} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC}	—	8	15	mA	$\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL}, I_{out} = 0 mA
	I_{CC1}	—	40	70	mA	Min Cycle, Duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	8	15	mA	Cycle Time = 1µs, $I_{I/O}$ = 0 mA, $\overline{CS}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0
Standby V_{CC} Current	I_{SS}	—	0.5	3	mA	$\overline{CS}$ = V_{IH}
	I_{SS1}	—	0.02	2	mA	V_{in} ≥ 0V, $\overline{CS}$ ≥ V_{CC} −0.2V
		—	1*2	100*2	µA	
		—	1*3	50*3	µA	
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Notes: 1. Typical values are at V_{CC} = 3.0V, T_a = +25°C and specified loading.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a = 25°C, f= 1 MHz.)*1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

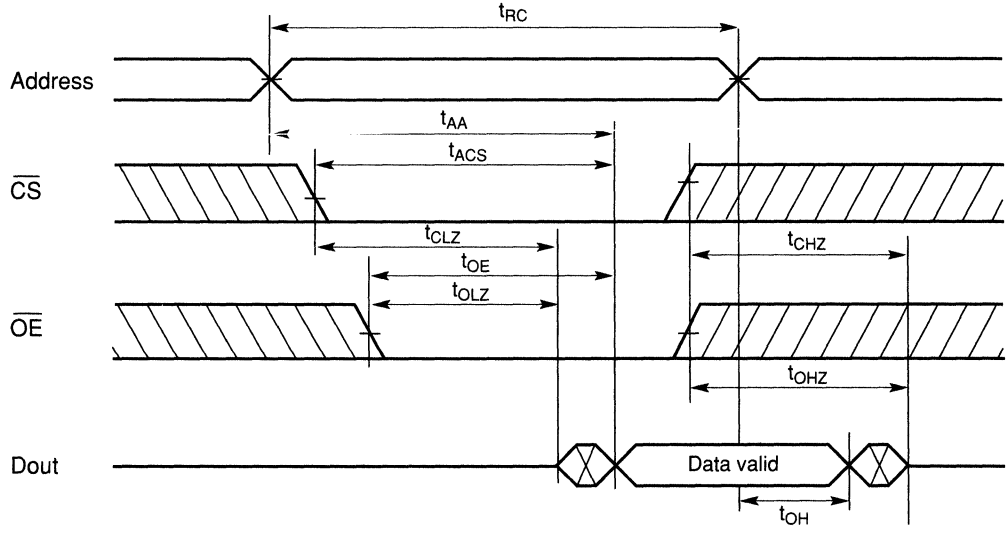
Test Conditions

- Input pulse levels: 0.8V to 2.4V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5V
- Output load: 1 TTL Gate + C_L (100 pF) (including scope & jig)

■ READ CYCLE

Item	Symbol	HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	85	—	100	—	120	—	150	—	ns	
Address access time	t_{AA}	—	85	—	100	—	120	—	150	ns	
Chip select access time	t_{ACS}	—	85	—	100	—	120	—	150	ns	
Output enable to output valid	t_{OE}	—	45	—	50	—	60	—	70	ns	
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns	1,2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns	1,2
Output hold from address change	t_{CH}	5	—	10	—	10	—	10	—	ns	

■ READ TIMING WAVEFORM*3

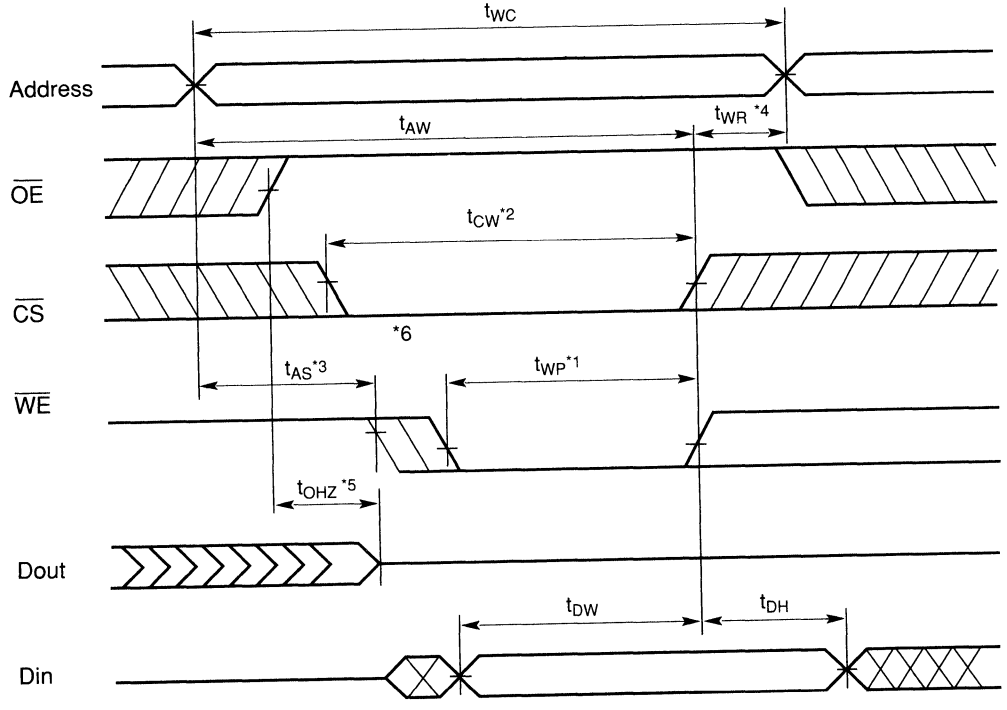


Notes: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. $\overline{WE}$ is high for read cycle.

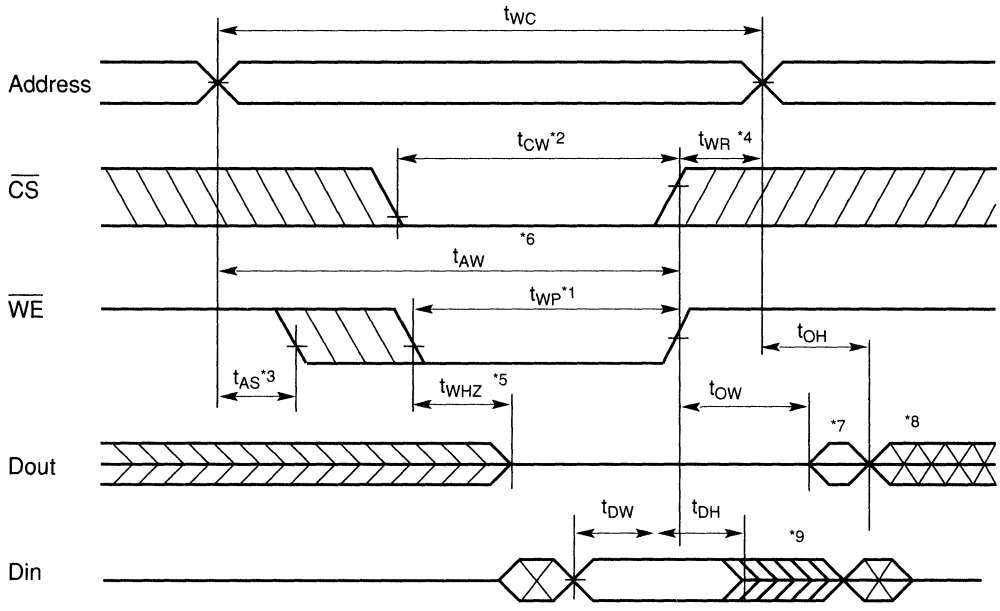
■ WRITE CYCLE

Parameter	Symbol	HM62256A-8		HM62256A-10		HM62256A-12		HM62256A-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	85	—	100	—	120	—	150	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	85	—	100	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	t_{AW}	75	—	80	—	85	—	100	—	ns	
Write pulse width	t_{WP}	55	—	60	—	70	—	90	—	ns	
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns	
WE to output in high–Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns	10
Data to write time overlap	t_{DW}	40	—	40	—	50	—	60	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	10

■ WRITE TIMING WAVEFORM (1) ($\overline{OE}$ Clock)



■ WRITE TIMING WAVEFORM (2) ($\overline{OE}$ Low Fixed)



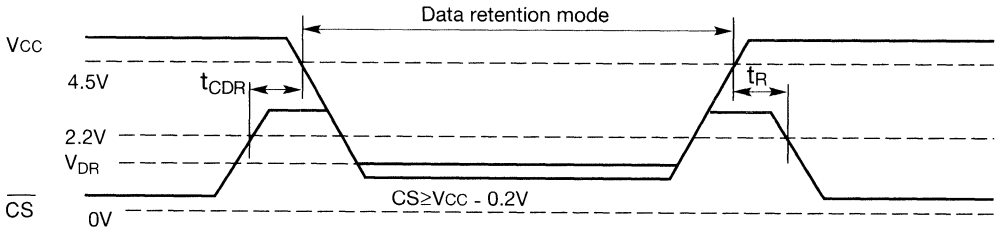
Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
7. D_{out} is the same phase of the write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

This characteristics is guaranteed only for L/L-SL version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2V, $V_{in} \geq 0V$
Data Retention Current	I_{CCDR}	—	0.5	10*2	µA	V_{CC} = 3.0V, $V_{in} \geq 0V$, $\overline{CS} \geq V_{CC}$ –0.2V
		—	0.5	10*2	µA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation Recovery Time	t_R	5	—	—	ms	

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



Notes:
1. 20 µA max at T_a = 0 to +40°C. (only for L-version)
2. 3 µA max at T_a = 0 to +40°C. (only for L-SL version).
3. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and D_{in} buffer. If $\overline{CS}$ controls data retention mode, V_{in} levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

32768-WORD × 8-BIT HIGH SPEED CMOS STATIC RAM

■ FEATURES

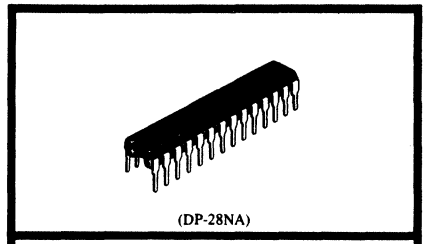
- High speed: Fast Access time 25/35 ns (max.)

HM62832H—Low power
Standby: 300 mW (typical)
Active: 30 μW (typical) (L-version)

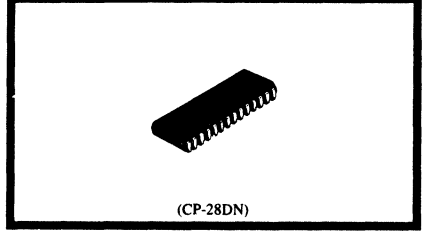
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output—Three stage output
- Directly TTL compatible—All inputs and outputs

■ ORDERING INFORMATION

Part No.	Access	Package
HM62832HP-25 HM62832HP-35	25 ns 35 ns	300 mil 28-pin Plastic DIP (DP-28NA)
HM62832HJP-25 HM62832HJP-35	25 ns 35 ns	300 mil 28-pin Plastic SOJ (CP-28DN)



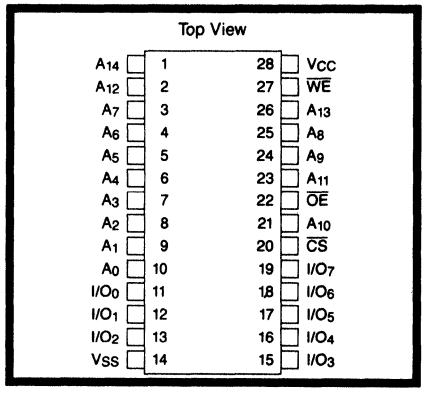
(DP-28NA)



(CP-28DN)

PIN ARRANGEMENT

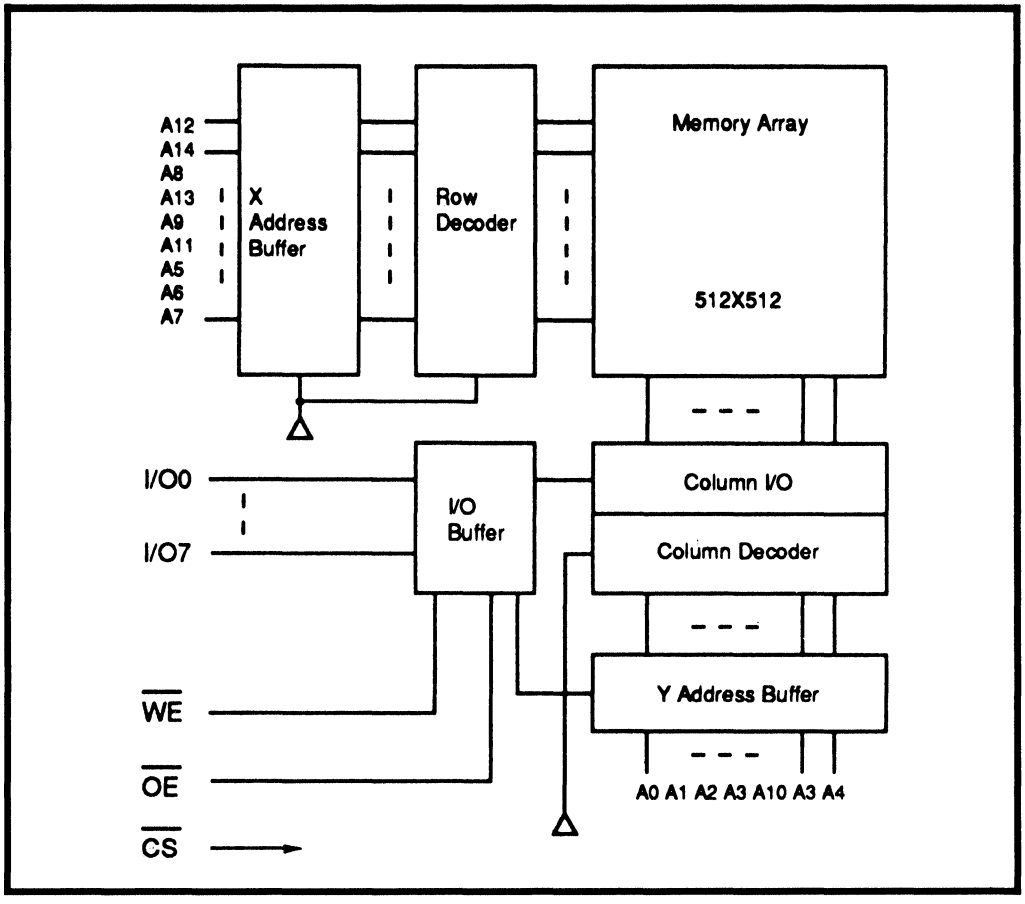
Top View



■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{14}	Address
I/O_0–I/O_7	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



2

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	-0.5*[1] to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. -2.5 V for pulse width ≤ 10 ns

■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	• Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	D_{out}	Read Cycle(1) to (3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	L		I_{CC}	D_{in}	Write Cycle(2)

NOTE: 1. X : H or L

■ DC CHARACTERISTICS for HM62832H (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	2	μA	V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating Power Supply Current	I_{CC}	—	60	120	mA	Min. cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
Standby Power Supply Current	I_{SB1}	—	0.02	2	mA	$\overline{CS}$ ≥ V_{CC} - 0.2V, 0 V ≤ V_{in} ≤ 0.2 V, or V_{in} ≥ V_{cc} - 0.2 V	
		—	0.006	0.1	mA		L-version
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = -4 mA	

NOTE: 1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

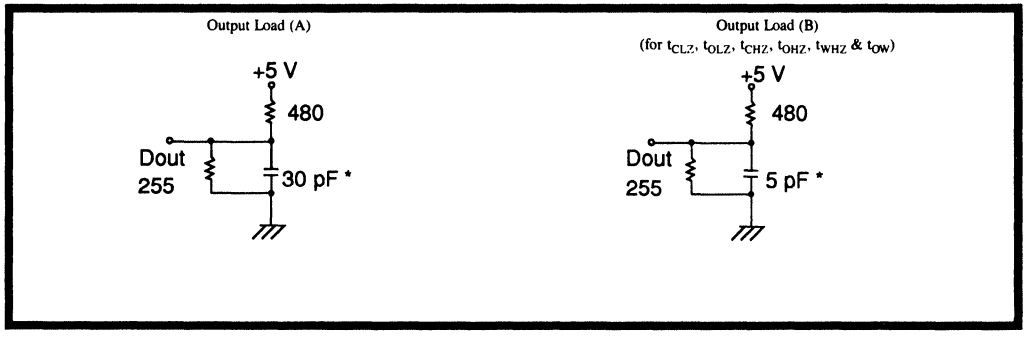
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures

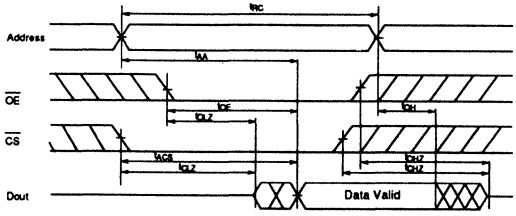


NOTE: *Including scope & jig.

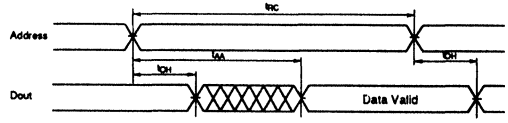
■ Read Cycle

Parameter	Symbol	HM62832H-25		HM62832H-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{CLZ}	5	—	5	—	ns
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}	0	12	0	15	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	ns

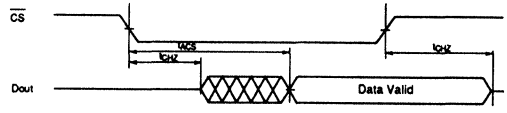
Read Cycle Timing (1) *1



Read Cycle Timing (2) *1, *2, *4



Read Cycle Timing (3) *1, *3, *4

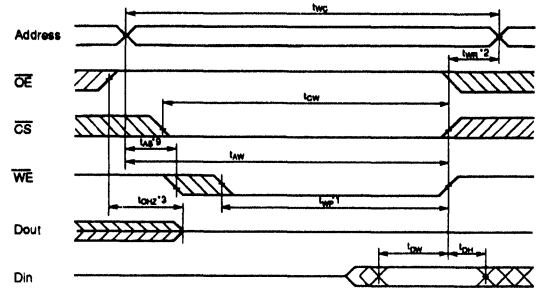


NOTES: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

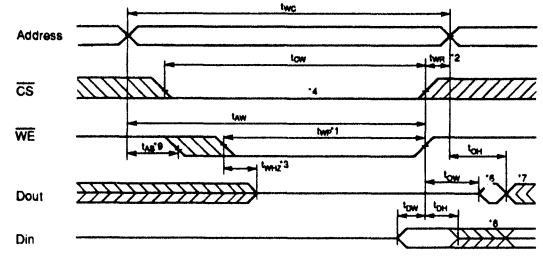
■ Write Cycle

Parameter	Symbol	HM62832H-25		HM62832H-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	15	—	20	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High-Z	t_{WHZ}	0	15	0	15	ns
Data to Write Time Overlap	t_{DW}	12	—	15	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	ns
Output Active From End of Write	t_{OW}	5	—	5	—	ns

Write Cycle Timing (1) ($\overline{OE}$ Clock)



Write Cycle Timing (2) ($\overline{OE}$ Low Fixed)



NOTES: *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

*5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL}).

*6. D_{out} is in the same phase of written data of this write cycle.

*7. D_{out} is the read data of next address.

*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.

*9. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

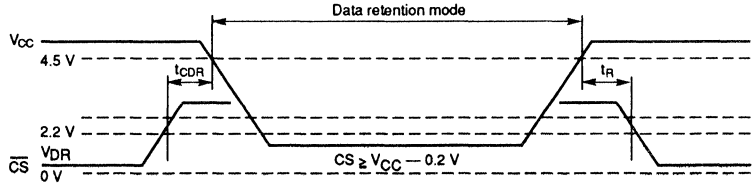
■ Low V_{CC} Data Retention Characteristics (T_A = 0 to +70°C)

This characteristics is guaranteed only for L-version

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or 0 V ≤ V_{in} ≤ 0.2 V
Data Retention Current	I_{CCDR}	—	1	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	t_{RC}*1	—	—	ns	

NOTES: *1. t_{RC} = read cycle time.
*2. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform

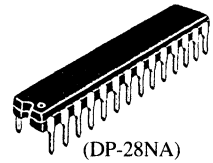


HM62832UH Series

32,768-Word x 8-Bit High Speed CMOS Static RAM

■ FEATURES

- High speed
  Access time 15/20 ns (max.)
- Low power
  Standby: 15 μW (typ.) (L-version)
  Operation: 550/400 mW (typ.)
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output—Three state output
- Directly TTL compatible—All inputs and outputs



(DP-28NA)

(CP-28DN)

■ ORDERING INFORMATION

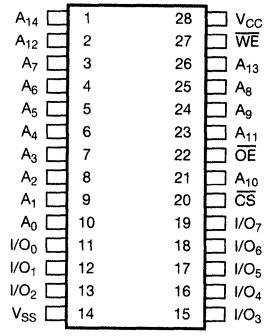
Type No.	Access Time	Package
HM62832UHP-15 HM62832UHP-20	15 ns 20 ns	300-mil, 28 pin Plastic DIP (DP-28NA)
HM62832UHLP-15 HM62832UHLP-20	15 ns 20 ns	
HM62832UHJP-15 HM62832UHJP-20	15 ns 20 ns	300-mil, 28 pin Plastic SOJ (CP-28DN)
HM62832UHLJP-15 HM62832UHLJP-20	15 ns 20 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{14}	Address
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

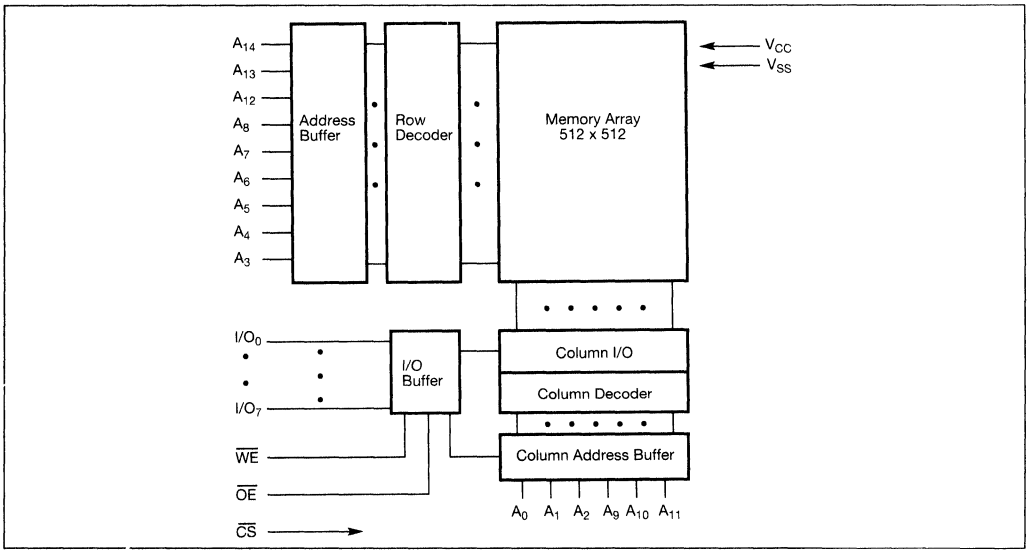
■ PIN ARRANGEMENT

HM62832UH Series



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle 1, 2, 3
L	H	L	Write	I_{CC}	D_{in}	Write Cycle 1
L	L	L	Write	I_{CC}	D_{in}	Write Cycle 2

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	−0.5*2 to +7.0	V
Voltage on any Pin Relative to V_{SS}*1	V_T	−0.5*2 to V_{CC} +0.5	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

Notes 1. With respect to V_{SS}
2. V_{CC} and V_T min = −2.5V for pulse width ≤ 10 ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

Note *1. V_{IL} min = −2.0V for pulse width ≤ 10 ns

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	Test Conditions	Min	Typ*1	Max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2.0	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	—	—	2.0	µA
Operating V_{CC} Current	I_{CC1} (–15)*3	Min. Cycle	—	135	170	mA
	I_{CC2} (–15)	2 x Min. Cycle*2	—	100	120	mA
	I_{CC1} (–20)	Min. Cycle	—	120	150	mA
	I_{CC2} (–20)	2 x Min. Cycle	—	90	110	mA
Standby V_{CC} Current	I_{SB} (-15)	$\overline{CS}$ = V_{IH}, Min. Cycle	—	40	60	mA
	I_{SB} (-20)	$\overline{CS}$ = V_{IH}, Min. Cycle	—	30	50	mA
Standby V_{CC} Current (1)	I_{SB1} (L-version)	$\overline{CS}$ ≥ V_{CC} –0.2V, 0V ≤ V_{in} ≤ 0.2V or V_{CC} –0.2V ≤ V_{in}	—	0.02	2.0	mA
			—	0.003	0.1	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –4.0 mA	2.4	—	—	V

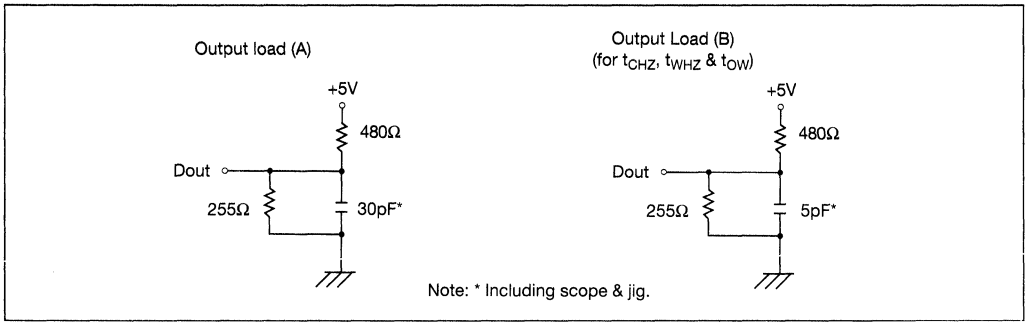
■ CAPACITANCE (T_a = 25°C, f = 1.0 MHz)*1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	—	—	10	pF	$V_{I/O}$ = 0V

Note *1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} 5V ± 10%, unless otherwise noted.)

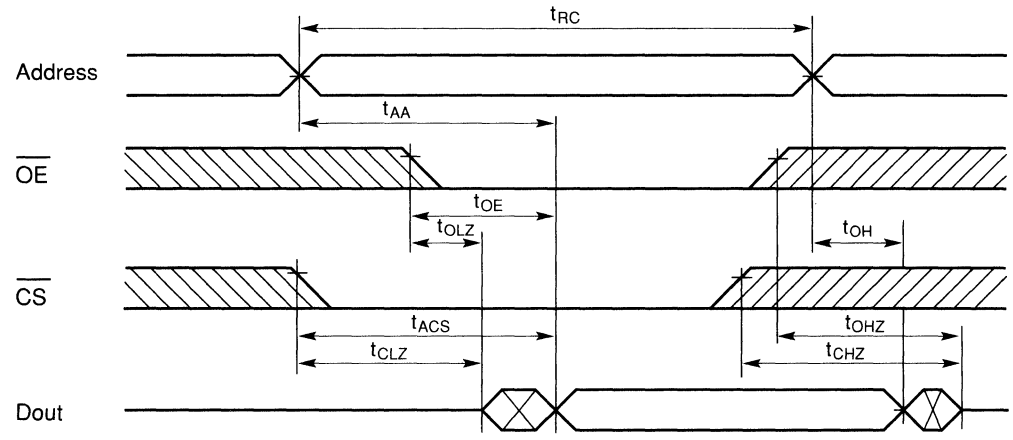
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 4ns
- Input and Output timing reference levels: 1.5V
- Output load: See figures

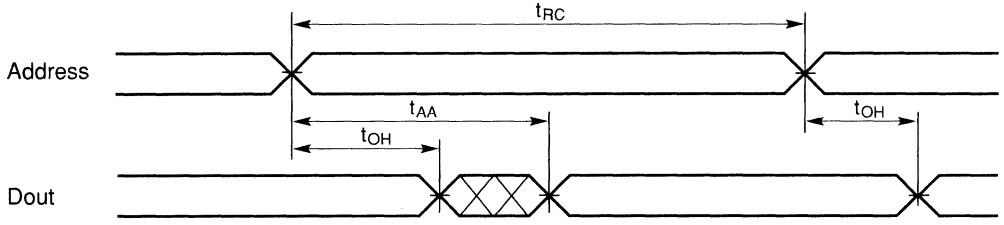


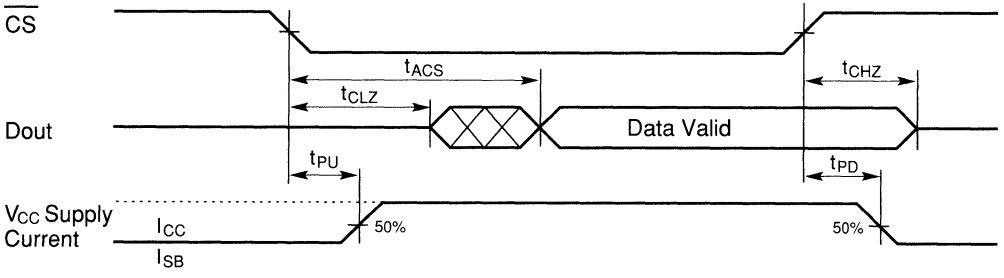
■ READ CYCLE

Item	Symbol	HM62832UH-15		HM62832UH-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	—	20	—	ns
Address Access Time	t_{AA}	—	15	—	20	ns
Chip Select Access Time	t_{ACS}	—	15	—	20	ns
Chip Selection to Output in Low–Z	t_{CLZ}*1	3	—	3	—	ns
Output Enable to Output Valid	t_{OE}	—	8	—	10	ns
Output Enable to Output in Low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip Deselection to Output in High–Z	t_{CHZ}*1	0	7	0	10	ns
Chip Disable to Output in High–Z	t_{OHZ}*1	0	7	0	10	ns
Output Hold from Address Change	t_{OH}	3	—	3	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	20	ns

■ READ TIMING WAVEFORM (1) *1, *2





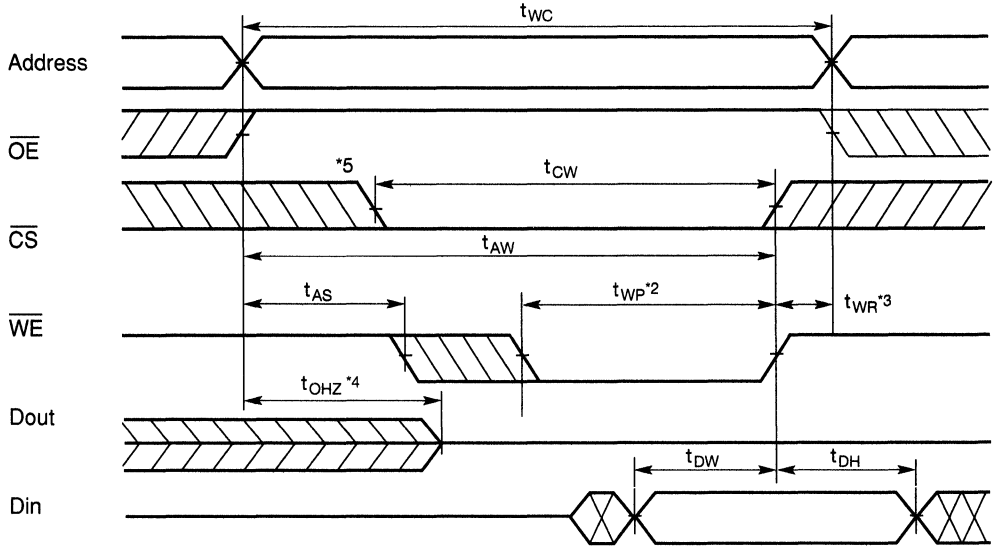


Notes:
1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low
5. $\overline{OE} = V_{IL}$.

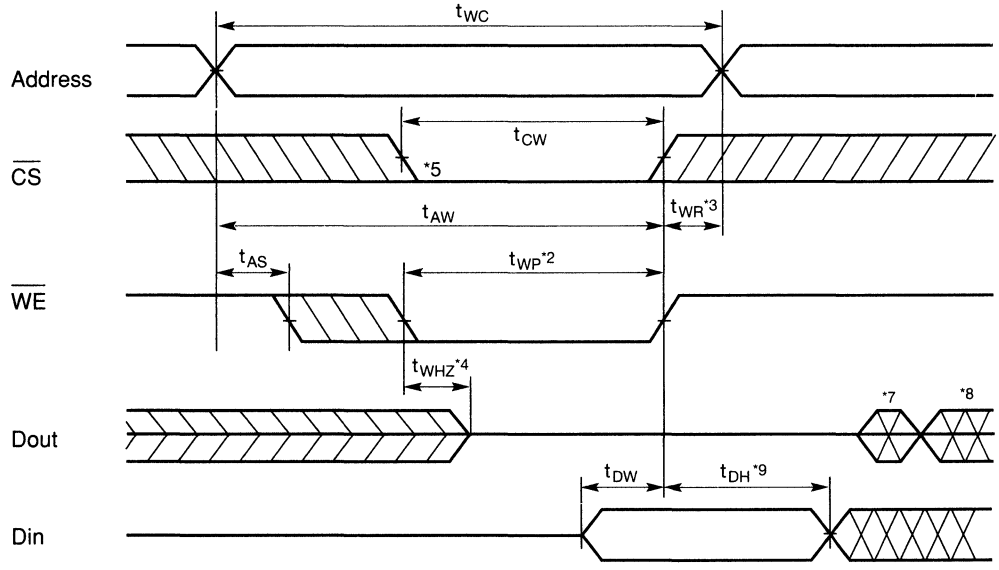
■ WRITE CYCLE

Item	Symbol	HM62832UH-15		HM62832UH-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15	—	20	—	ns
Chip Selection to End of Write	t_{CW}	10	—	12	—	ns
Address Valid to End of Write	t_{AW}	13	—	15	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	10	—	12	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Output Disable to Output in High-Z*1	t_{OHZ}	0	7	0	10	ns
Write to Output in High-Z*1	t_{WHZ}	0	7	0	10	ns
Data to Write Time Overlap	t_{DW}	8	—	10	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write*1	t_{OW}	3	—	3	—	ns

■ WRITE TIMING WAVEFORM (1)



■ WRITE TIMING WAVEFORM (2) *6



Notes:
1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This paramter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$).
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. $\overline{WE}$ must be high during all address transition except when device is disable with $\overline{CS}$.

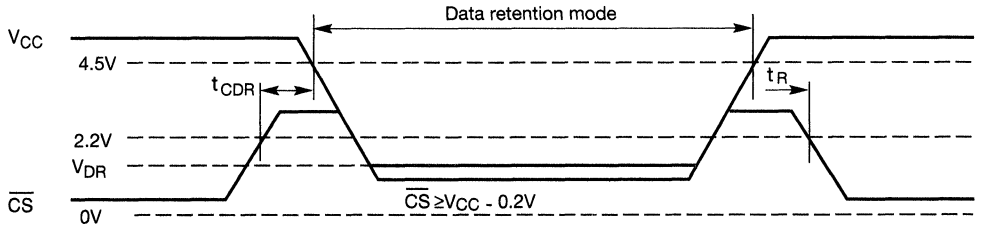
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C,)

This characteristics is guaranteed only for L-version

Item	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{in} \geq V_{CC} - 0.2V$ or $0V \leq V_{in} \leq 0.2V$
Data Retention Current	I_{CCDR}	—	2	50*1	µA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note *1. V_{CC} = 3.0V.

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



HM67832SH Series — Preliminary

32,768-Words x 8-Bit High Speed Static Random Access Memory

■ FEATURES

- 32,768-words x 8 bit organization
- Directly TTL compatible input and output
- 0.8μm Hi-BiCMOS process
- +5V Single supply
- Completely static memory
- No clock or timing strobe required
- Low power dissipation (DC) operating: 400mW (typ)
- Super fast access time: 10/12 ns (max)

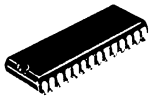
■ ORDERING INFORMATION

Type No.	Organization	Access Time	Package
HM67832SHJP-10	32K x 8	10 ns	300 mil 28 pin Plastic SOJ (CP-28DN)
HM67832SHJP-12		12 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{14}	Address Input
I/O_1–I/O_8	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
V_{SS}	Ground
V_{CC}	Power Supply

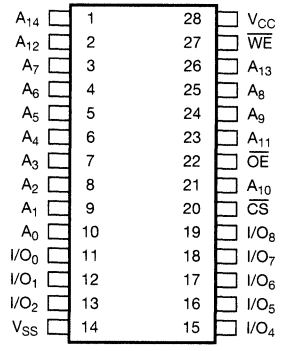
■ PACKAGE OUTLINE



(CP-28DN)

■ PIN ARRANGEMENT

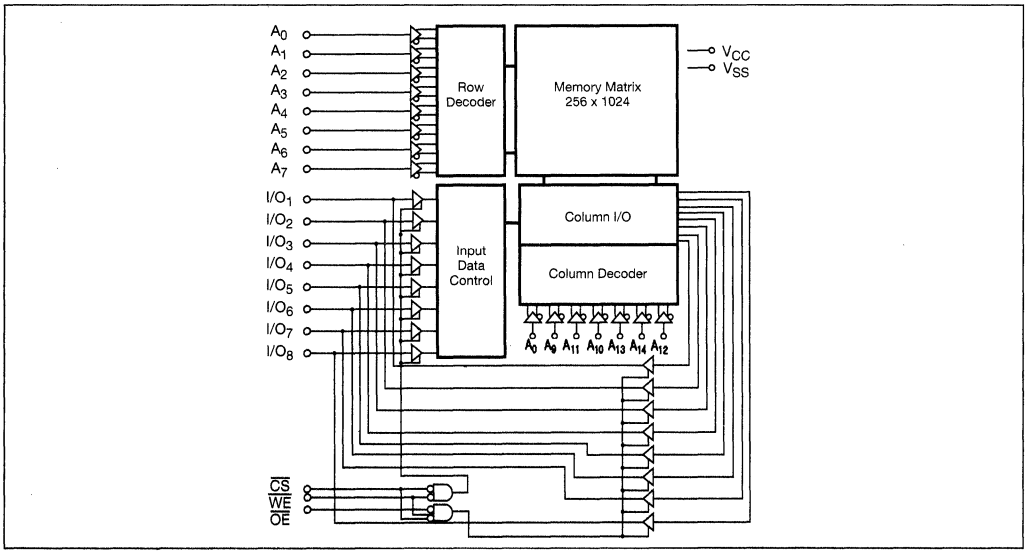
HM67832SH Series



(Top View)

2

■ BLOCK DIAGRAM



■ TRUTH TABLE

Input			Output	Mode	V_{CC} Current	Ref. Cycle
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$				
H	X	X	High Z	Not Selected	I_{SB}, I_{SB1}	—
L	H	H	High Z	Output Disable	I_{CC}, I_{CC1}	—
L	H	L	Data Out	Read	I_{CC}, I_{CC1}	Read Cycle (1,2,3)
L	L	H	Data In	Write	I_{CC}, I_{CC1}	Write Cycle (1,2,3,4)
L	L	L	Data In	Write	I_{CC}, I_{CC1}	Write Cycle (5,6)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*1	V_{CC}	–0.5 to +7.0	V
Voltage on any Pin Relative to V_{SS}*1	V_T	–0.5 to V_{CC} +0.5	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	–10 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Notes 1. With respect to V_{SS}

Under the DC and AC specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input Low Voltage	V_{IL}	–3.0[1]	—	0.8	V

Note 1. Pulse width 10 ns, DC: –0.5V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM67832-10		HM67832-12		Unit
			Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	2	—	2	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = , V_{IH}, $\overline{WE}$ = V_{IL} $V_{I/O}$ 0V to V_{CC}	—	10	—	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	—	200	—	195	mA
Average Operating Current	I_{CC1}	15 ns Cycle, $I_{I/O}$ = 0 mA	—	150	—	140	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	—	40	—	40	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} –0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} –0.2V	—	30	—	30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	—	2.4	—	V

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C unless otherwise noted.)

• Read Cycle

Item	Symbol	HM67832UH-10		HM67832UH-12		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10	—	12	—	ns
Address Access Time	t_{AA}	—	10	—	12	ns
Chip Select Access Time	t_{ACS}	—	10	—	12	ns
Chip Selection to Output in Low Z	t_{LZ}[1, 2]	3	—	4	—	ns
Output Enable to Output Valid	t_{OE}	—	5	—	6	ns
Output Enable to Output in Low Z	t_{OLZ}[1, 2]	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{HZ}[1, 2]	0	5	0	5	ns
Output Hold from Address Change	t_{OH}	3	—	4	—	ns

Notes 1. This parameter is sampled and not 100% tested.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

• Write Cycle

Item	Symbol	HM67832UH-10		HM67832UH-12		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}[1]	11	—	12	—	ns
Chip Selection to End of Write	t_{CW}	8	—	9	—	ns
Address Valid to End of Write	t_{AW}	10	—	11	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	8	—	9	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	6	—	6	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[2, 3]	0	5	0	6	ns
Output Disable to Output in High Z	t_{OHZ}[2, 3]	0	6	0	6	ns
Output Active from End of Write	t_{OW}[2, 3]	4	—	4	—	ns

Notes 1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3 Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

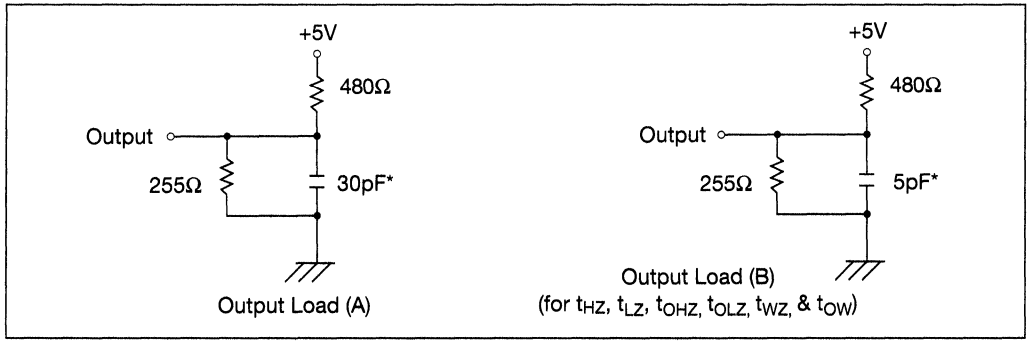
■ CAPACITANCE (T_a = 25°C, f= 1 MHz.)

Item	Symbol	Max	Unit	Test Condition
Input Capacitance	C_{in}[1]	6	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$[1]	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

■ AC TEST CONDITIONS

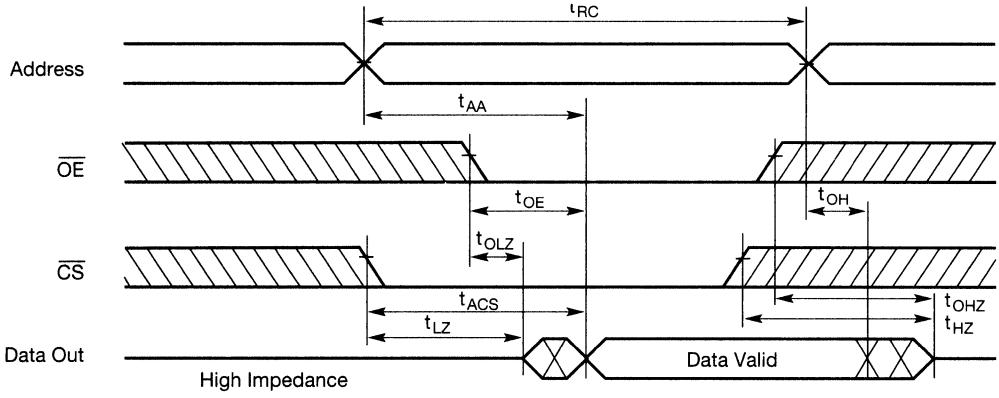
- Input pulse levels: V_{SS} to 3.0V
- Input timing reference levels: 1.5V
- Output load: See figure
- Input rise and fall times: 4ns
- Output Ireference levels: 1.5V



*includes scope and jig capacitance

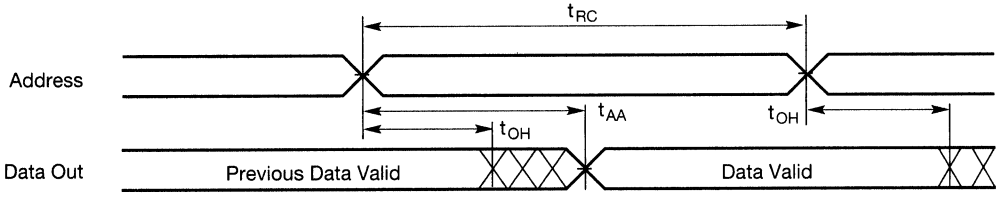
■ TIMING WAVEFORMS

• Read Cycle –1[1]



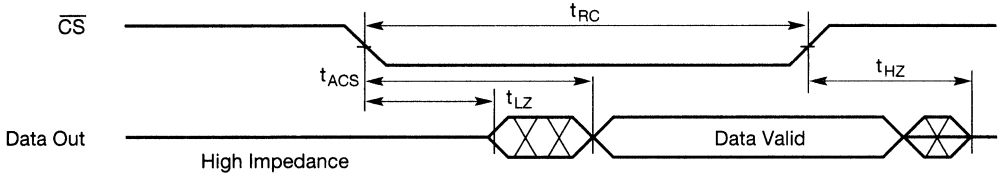
Notes 1. $\overline{WE}$ = V_{IH}.

• Read Cycle –2[1, 2, 3]



Notes 1. $\overline{WE}$ = V_{IH}.
2. $\overline{CS}$ = V_{IL}.
3. $\overline{OE}$ = V_{IL}

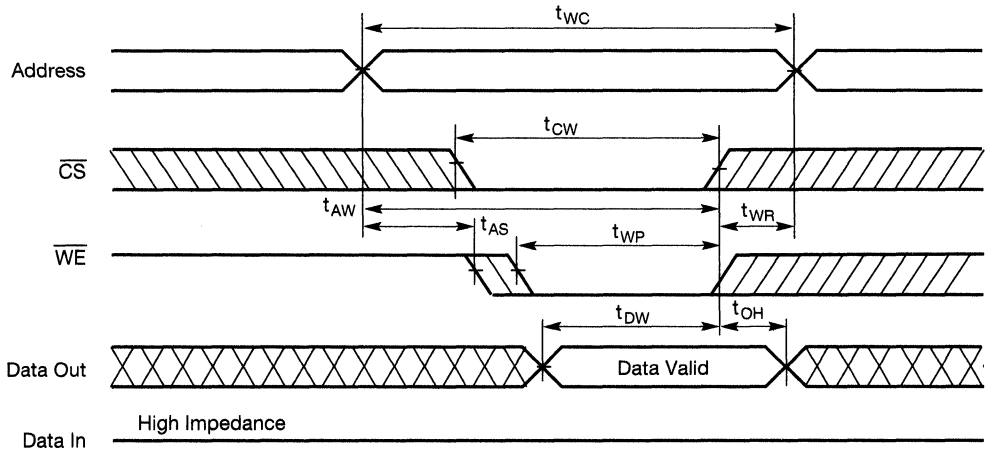
• Read Cycle –3[1, 2, 3]



Notes 1. $\overline{WE}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

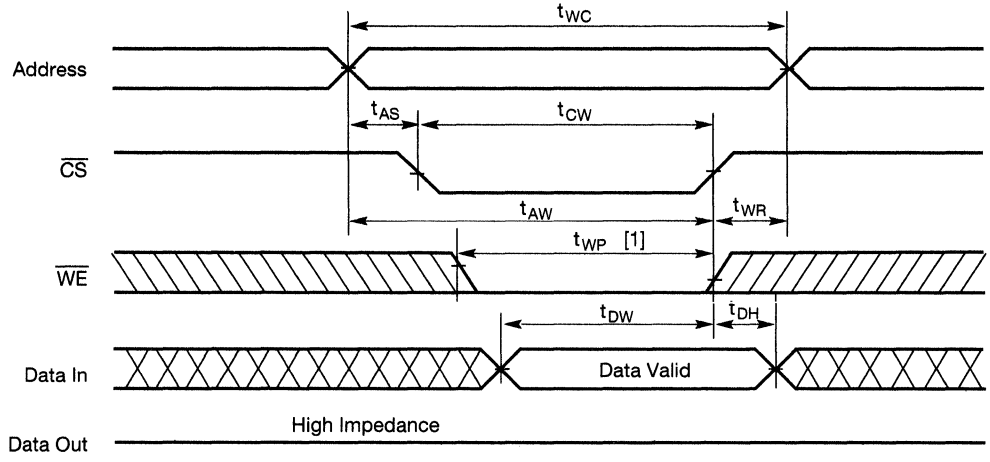
■ TIMING WAVEFORMS

• Write Cycle -1[1] ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



Note 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ t(WP).

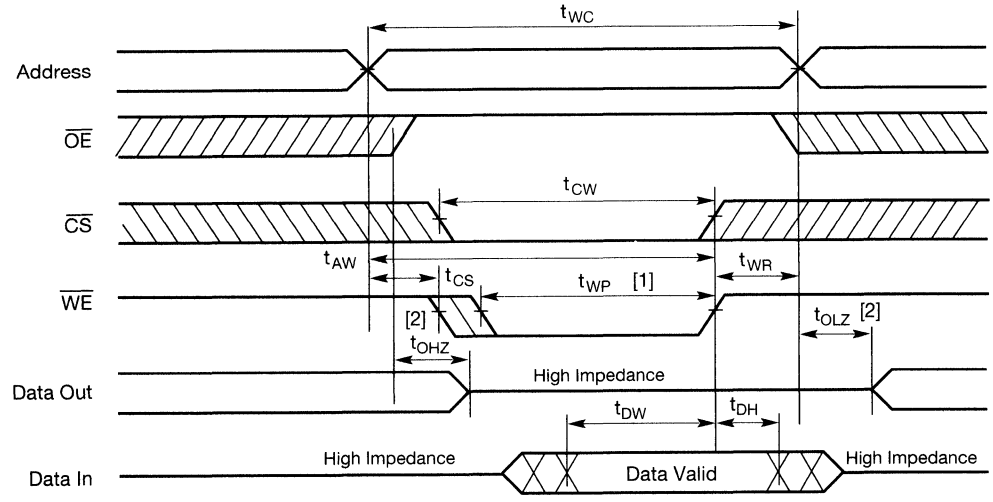
• Write Cycle -2[1] ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



Note 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (tWP).

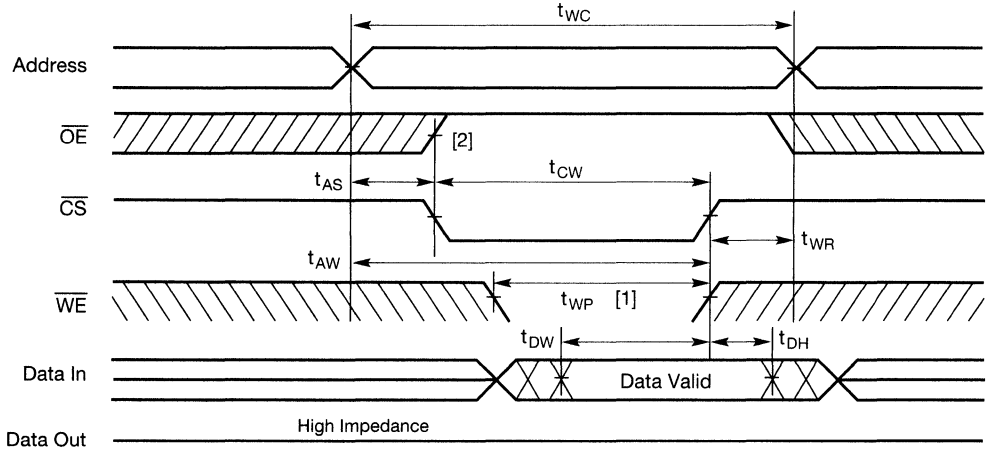
■ TIMING WAVEFORMS

• Write Cycle –3[1, 2] ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



Notes 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ t(WP).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

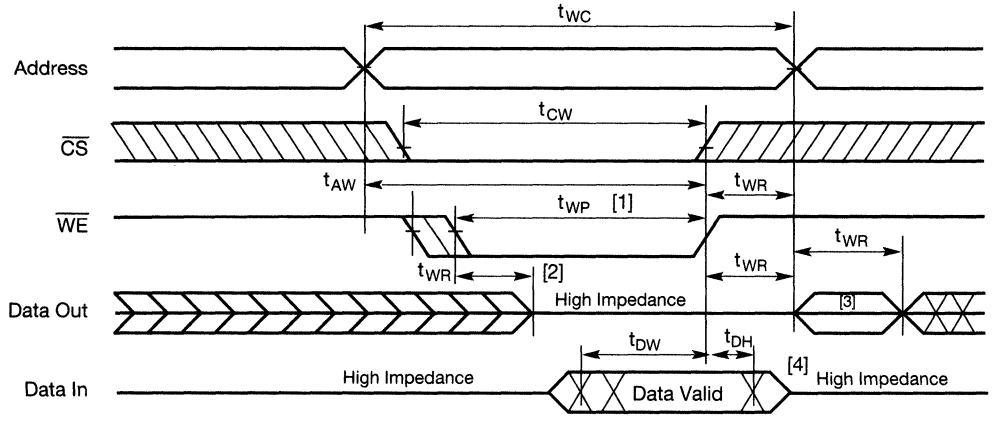
• Write Cycle –4[1, 2] ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Notes 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (tWP).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

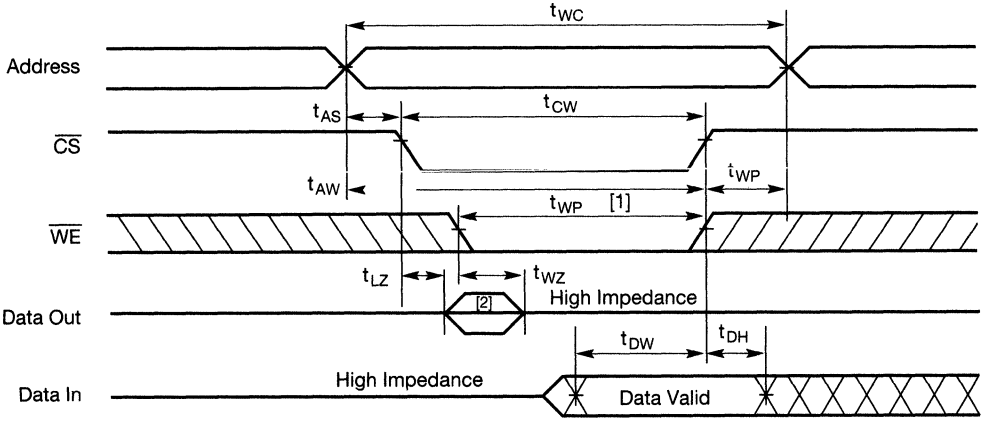
■ TIMING WAVEFORMS

• Write Cycle –5[1, 2, 3, 4] ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Notes 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ t(WP).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

• Write Cycle –6[1, 2] ($\overline{OE}$ = L, $\overline{CS}$ Controlled)

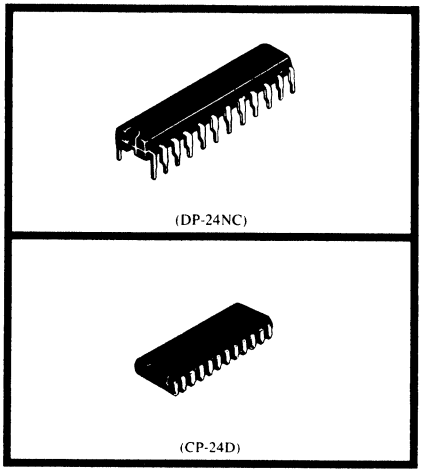


Notes 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (tWP).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

65536-Word × 4-Bit High Speed CMOS Static RAM

The Hitachi HM6208H is a high speed 256k static RAM organized as 64k-word × 4 bit. It realizes high speed access time (25/35) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous wherever high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6208H is packaged in the industry standard 300-mil, 24 pin, plastic DIP. The HM6208H is also available in a 300-mil, 24 pin, plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.



(DP-24NC)

(CP-24D)

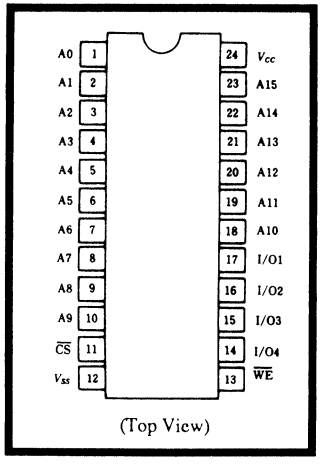
Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35 ns (max.)
- Low power
  - Active: 300 mW (typ.)
  - Standby: 100 μW (typ.)
    30 μW (typ.) (L-version)
- Completely static operation requires
  No clock or timing strobe
- Access and cycle times are equivalent
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6208HP-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6208HP-35	35 ns	
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HJLP-25	25 ns	
HM6208HJLP-35	35 ns	

Pin Arrangement

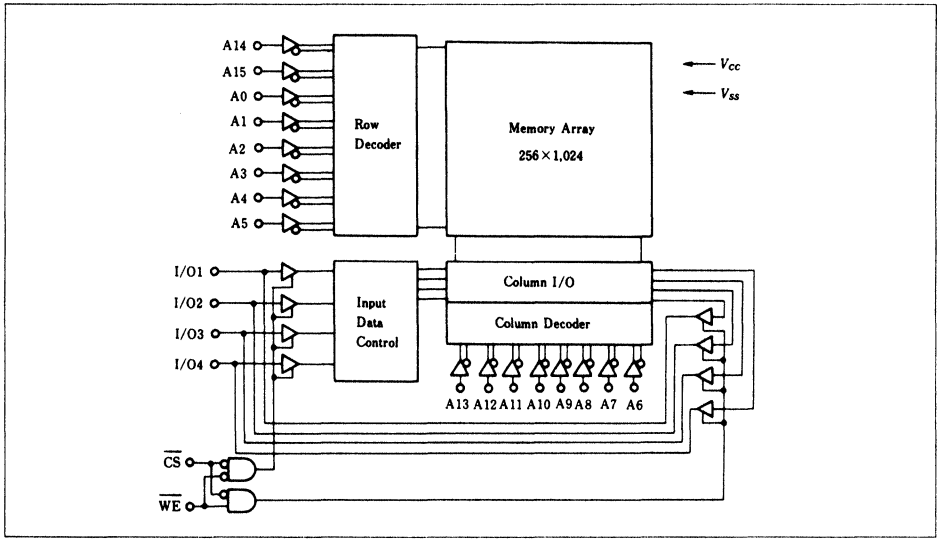


(Top View)

Pin Description

Pin Name	Function
A0 – A15	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	Din	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	—	2.0	μA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle, Duty = 100%
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. Cycle
Standby Power Supply Current "H" Version	I_{SB}	—	20	40	mA	
Standby Power Supply Current	I_{SB1}	—	20	2000	μA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Standby Power Supply Current L-Version	I_{SB1}	—	6	100	μA	
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	Cvo	—	10	pF	Vvo = 0 V

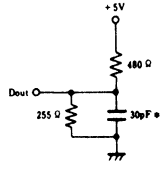
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

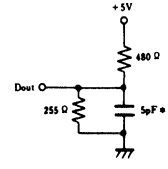
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWZ & tOW)



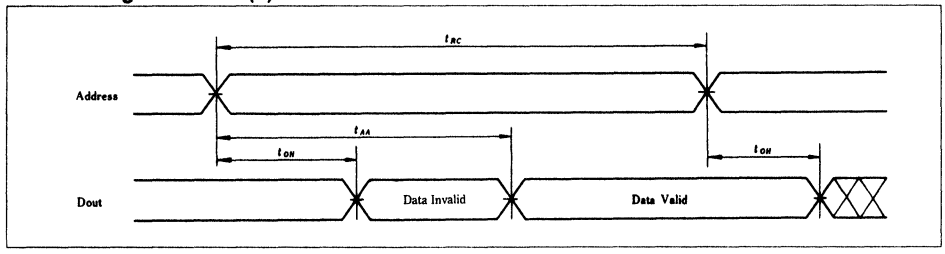
Note: * Including scope & jig.

■ Read Cycle

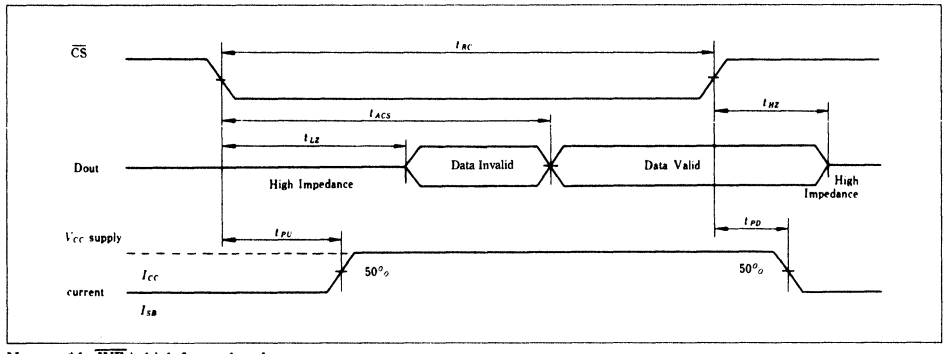
Item	Symbol	HM6208H-25		HM6208H-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Selection to Power Down Time	t_{PD}	—	15	—	25	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

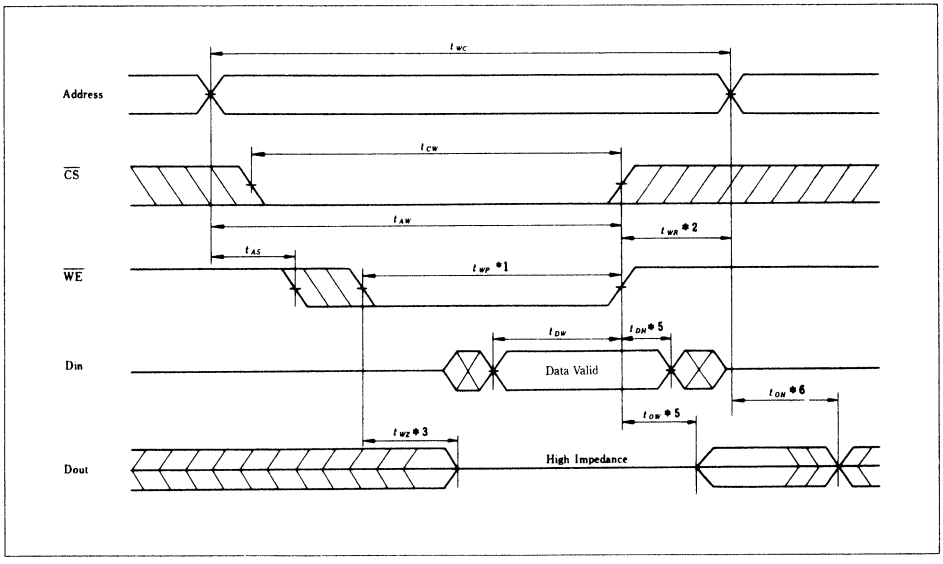
■ Write Cycle

Item		Symbol	HM6208H-25		HM6208H-35		Unit
			Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	25	—	35	—	ns
Chip Selection to End of Write		t_{CW}	20	—	30	—	ns
Address Valid to End of Write		t_{AW}	20	—	30	—	ns
Address Setup Time		t_{AS}	0	—	0	—	ns
Write Pulse Width		t_{WP}	20	—	30	—	ns
	"H" Version				25		
Write Recovery Time		t_{WR}	3	—	3	—	ns
Data Valid to End of Write		t_{DW}	15	—	20	—	ns
Data Hold Time		t_{DH}	0	—	0	—	ns
Write Enabled to Output in High-Z		t_{WZ}*1	0	8	0	10	ns
Output Active From End of Write		t_{OW}*1	0	—	0	—	ns

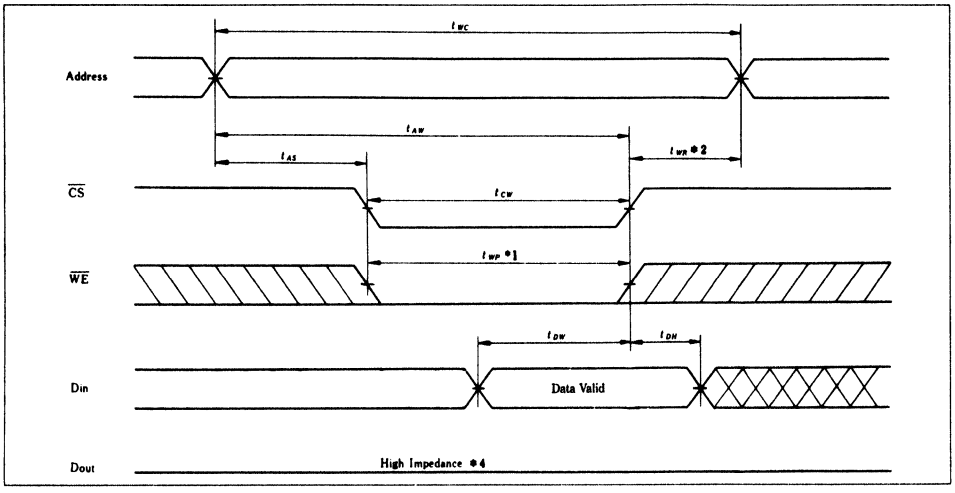
Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is ampled and not 100% tested.

2

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



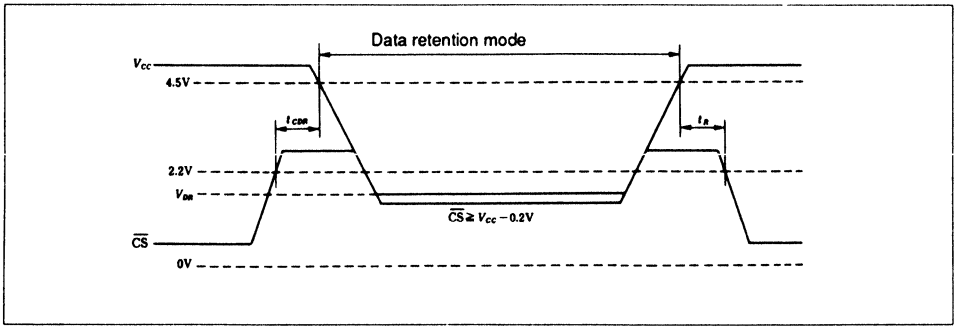
Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

These characteristics are guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50 *2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	t_{RC} *1	—	—	ns	

Notes: *1. t_{RC} = read cycle time.
*2. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform



HM6708 Series

65536-word × 4-bit High Speed Hi-BiCMOS Static RAM

The HM6708 Series has been converted to the HM6708A Series. The new A Series is completely compatible with the non-A Series.

Please refer to the specification comparison below to assist in your conversion.

		HM6708				HM6708A						
		20		25		15		20		25		
		min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	Unit
DC	IL_I		2		2		2		2		2	μA
	IL_O		10		10		10		10		10	μA
	I_{cc}		100		100		100		100		100	mA
	$I_{cc}1$		120		120		120		120		120	mA
	I_{sb}		30		30		30		30		30	mA
	$I_{sb}1$		10		10		10		10		10	mA
	V_{ol}		0.4		0.4		0.4		0.4		0.4	V
	V_{oh}	2.4		2.4		2.4		2.4		2.4		V
Read	t_{RC}	2.0		25		15		20		25		ns
	t_{AA}		20		25		15		20		25	ns
	t_{ACS}		20		25		15		20		25	ns
	t_{OH}	5		5		4		5		5		ns
	t_{LZ}	5/0		5/0		4		★5		★5		ns
	t_{HZ}	0	8	0	15/10	0	6	0	8	0	★10	ns
Write	t_{WC}	20		25		15		20		25		ns
	t_{CW}	15		20		10		15		20		ns
	t_{AW}	15		20		10		15		20		ns
	t_{AS}	0		0		0		0		0		ns
	t_{WP}	15		20		10		15		20		ns
	t_{WR}	1.5		3		0		★0		★0		ns
	t_{DW}	15/20		20/15		8		★10		★12		ns
	t_{DH}	0		0		0		0		0		ns
	t_{WZ}	0	15/8	0	15/10	0	6	0	8	0	10	ns
	t_{OW}	0		0		0		0		0		ns

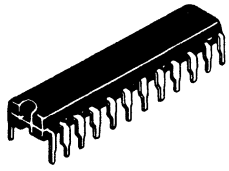
★ Modified specifications

HM6708A Series — Preliminary

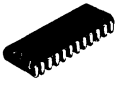
65536-Word × 4-Bit High Speed Static RAM

■ FEATURES

- 65536-words × 4 bit organization
- Fully TTL compatible input and output
- 1.0μ Hi-BiCMOS process
- +5V single supply
- Completely static memory
  No clock or timing strobe required
- Low power dissipation
  Operating: 450mW (typ.)
- Super fast
  Access time: 15/20/25 ns (max.)



(DP-24NC)

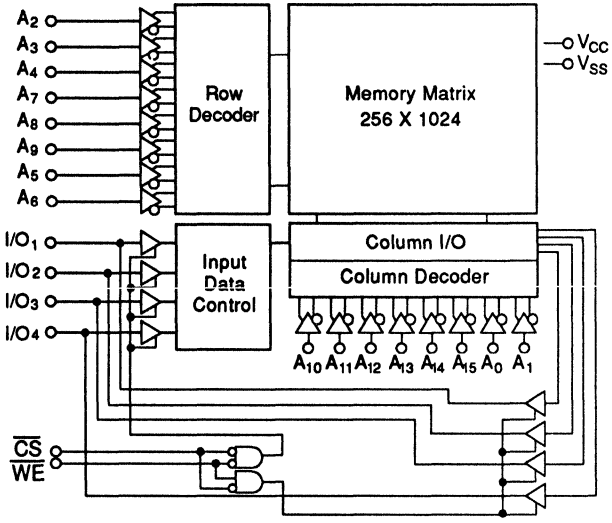


(CP-24D)

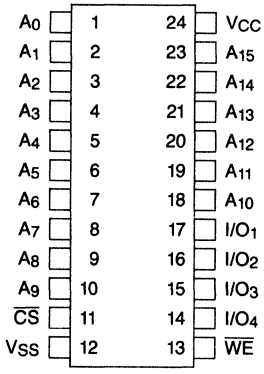
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6708AP-15	15ns	300 mil 24 pin
HM6708AP-20	20ns	Plastic DIP
HM6708AP-25	25ns	(DP-24NC)
HM6708AJP-15	15ns	300 mil 24 pin
HM6708AJP-20	20ns	Plastic SOJ
HM6708AJP-25	25ns	(CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{15}	Address Input
I/O_1-I/O_4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{SS}	Ground
V_{CC}	Power Supply

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low (Logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

*Pulse width 20ns, DC: −0.5V

■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5.0\ V \pm 10\%$, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6708A-15			HM6708A-20/25			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5\ V$, $V_{IN}=0\ V$ to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{I/O}=0\ V$ to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0\ mA$	—	—	100	—	—	100	mA
Average Operating Current	I_{CC1}	min. cycle, Duty: 100% $I_{I/O}=0\ mA$	—	—	140	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$, $V_{IN}=V_{IH}$ or V_{IL}	—	—	30	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2\ V$ $V_{IN} \leq 0.2\ V$ or $V_{IN} \geq V_{CC}-0.2V$	—	—	10	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8\ mA$	—	—	0.4	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4\ mA$	2.4	—	—	2.4	—	—	V

■ AC CHARACTERISTICS ($V_{CC}=5\ V \pm 10\%$, Ta=0 to +70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6708A-15		HM6708A-20		HM6708A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns
Address Access Time	t_{AA}	—	15	—	20	—	25	ns
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns
Output Hold from Address Change	t_{OH}	4	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}[1), 2)]	4	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}[1), 2)]	0	6	0	8	5	10	ns

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

• **Write Cycle**

Item	Symbol	HM6708A-15		HM6708A-20		HM6708A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}[1]	15	—	20	—	25	—	ns
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	8	—	10	—	12	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[2), 3)]	0	6	0	8	0	10	ns
Output Active from End of Write	t_{OW}[2), 3)]	0	—	0	—	0	—	ns

NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

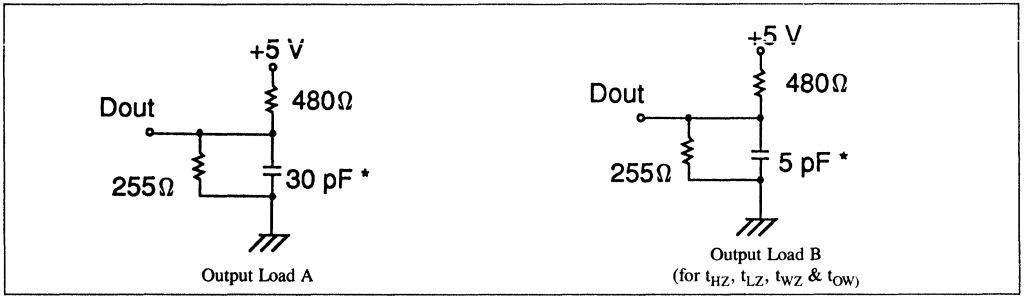
■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Max.	Unit	Test Condition
Input Capacitance	C_{IN}[1)]	6	pF	V_{IN}=0 V
Output Capacitance	$C_{I/O}$[1)]	10	pF	$V_{I/O}$=0 V

NOTES: 1. This parameter is sampled and not 100% tested.

■ AC TEST CONDITIONS

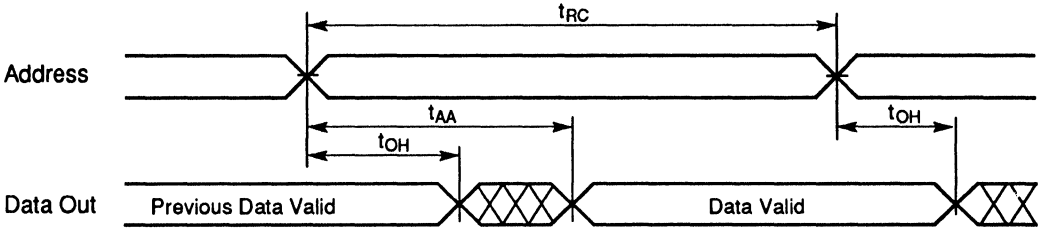
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5 V



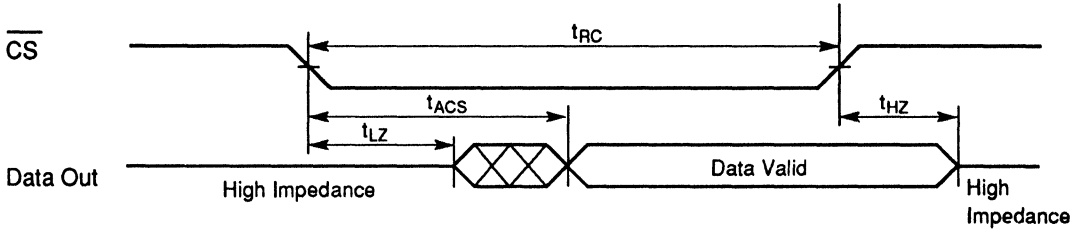
*Including scope and jig capacitance.

■ TIMING WAVEFORM

• **Read Cycle (1)** (1) (2)

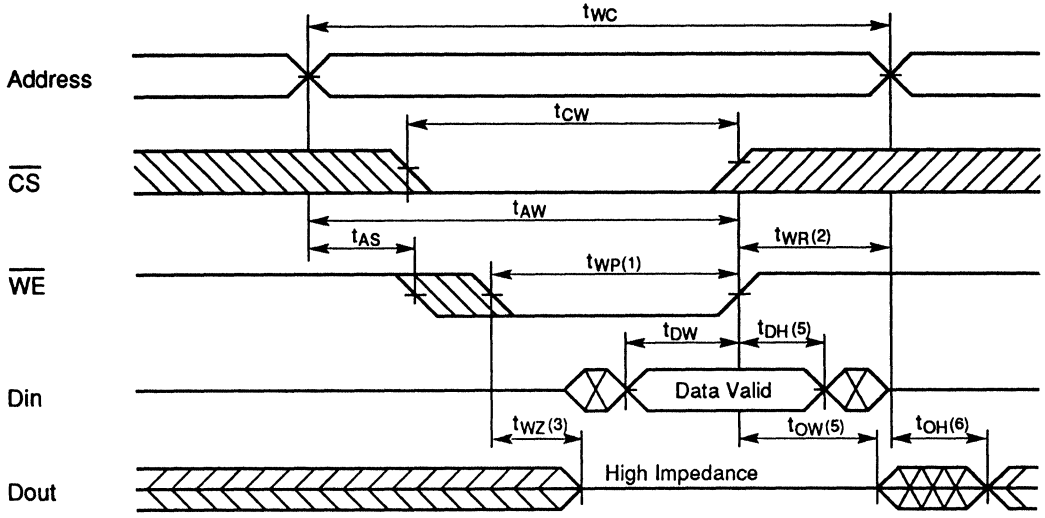


• **Read Cycle (2)** (1) (3)

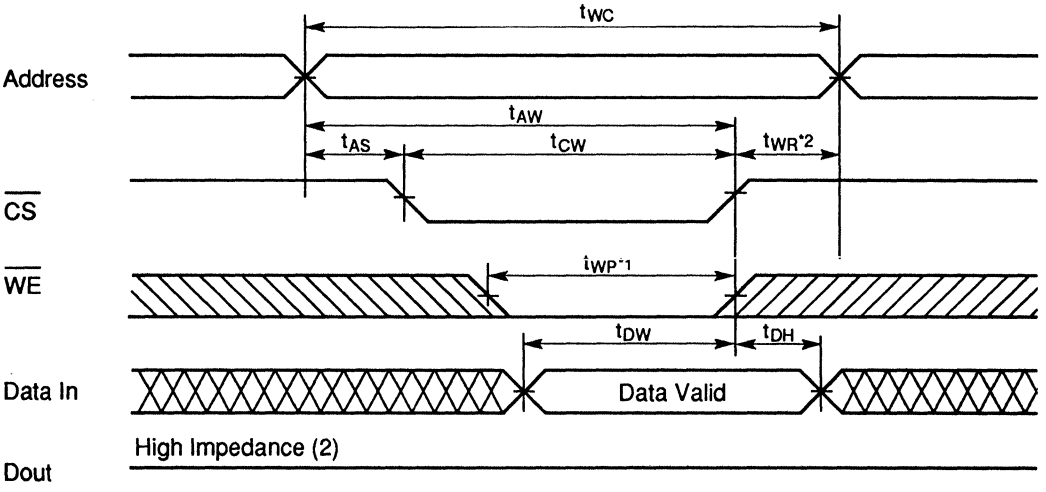


NOTES: 1. $\overline{WE}$ is High for READ cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES:

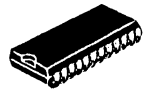
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Output data is the same phase of write data of this write cycle.

HM6708SH Series — Preliminary

65,536-words x 4-Bit High Speed Static Random Access Memory

■ FEATURES

- 65,536-words x 4 bit organization
- Directly TTL compatible input and output
- 0.8 μm Hi-BiCMOS process
- +5V single supply
- Completely static memory
- No clock or timing strobe required
- Low power dissipation (DC) operating: 400mW typ
- Super fast access time: 10/12ns (max)



(CP-24D)

■ ORDERING INFORMATION

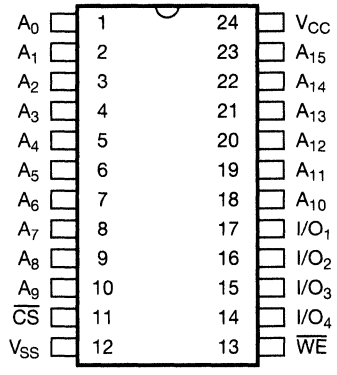
Type No.	Organ-ization	Access Time	Package
HM6708SHJP-10 HM6708SHJP-12	64k x 4	10 ns 12 ns	300 mil 24 pin Plastic SOJ (CP-24D)

■ PIN DESCRIPTION

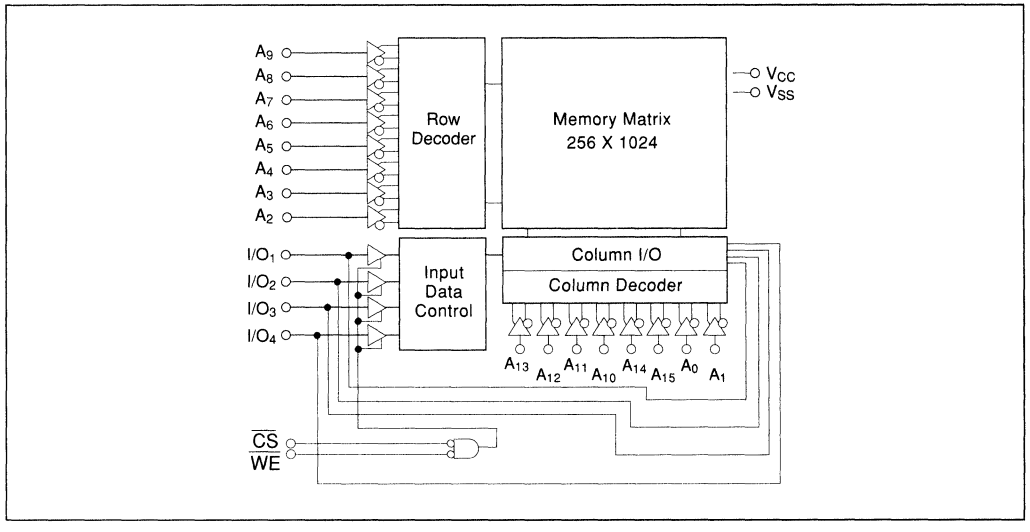
Pin Name	Function
A0–A15	Address Input
I/O1–I/O4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{SS}	Ground
V_{CC}	Power Supply
NC	Not Connect

■ PIN ARRANGEMENT

HM6708SH Series



(Top View)



■ TRUTH TABLE

Input		Output	Mode	V_{CC} Current	Ref. Cycle
$\overline{CS}$	$\overline{WE}$				
H	X	High Z	Not Selected	I_{SB}, I_{SB1}	—
L	H	Dout	Write "0"	I_{CC}, I_{CC1}	Read Cycle (2), (3)
L	L	High Z	Write "1"	I_{CC}, I_{CC1}	Write Cycle (1), (2)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage[1]	V_{CC}	-0.5 to +7.0	V
Voltage on any Pin Relative to V_{SS}	V_t	-0.5 to V_{CC} +0.5	V
Power Dissipation	P_t	1.0	W
Operating Temperature Range	T_{ppr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg} (bias)	–10 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Note: 1. With respect to V_{SS}.

Under the dc and ac specifications shown ing the Tables, this device is tested under the minimum trasverse air flow exceeding 500 linear feet per minute.

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-3.0[1]	—	0.8	V

Note: 1. Pulse width 10 ns, DC: -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $+70°C$)

Item	Symbol	Test Conditions	10			12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{IN}=0V to V_{CC}	–	–	2	–	–	2	µA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} V_{IO} = 0V to V_{CC}	–	–	10	–	–	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	60	100	–	60	100	mA
Average Operating Current	I_{CC1}	15ns cycle, $I_{I/O}$ = 0mA	–	130	180	–	120	175	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} =V_{IH} or V_{IL}	–	–	40	–	–	40	mA
	I_{SB1}	$\overline{CS} \ge V_{CC} = 0.2V$ $V_{IN} \le 0.2V$or $V_{IN} \ge V_{CC}$ - 0.2V	–	–	30	–	–	30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = .4mA	2.4	–	–	2.4	–	–	V

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	10	–	12		ns
Address Access Time	t_{AA}	–	10	–	12	ns
Chip Select Access Time	t_{ACS}	–	10	–	12	ns
Chip Selction to Output in Low Z	t_{LZ}[1, 2]	3	–	4	–	ns
Chip Deselection to Output in High Z	t_{HZ}[1,2]	0	5	0	5	ns
Output Hold from Address Change	t_{OH}	3	–	4	–	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

• Write Cycle

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}[1]	11	–	12	–	ns
Chip Selection to End of Write	t_{CW}	8	–	9	–	ns
Address Valid to End of Write	t_{AW}	10	–	11	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	8	–	9	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	6	–	6	–	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[2,3]	0	5	0	6	ns
Output Active from End of Write	t_{OH}[2,3]	4	–	4	–	ns

Notes: 1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured in ± 200 mV from steady state voltage with specified loading in Load (B).

• **Capacitance** (T_a = 25°C, f = 1MHz)

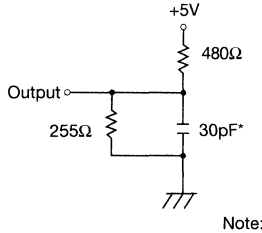
Parameter	Symbol	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}[1]	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$[1]	10	pF	$V_{I/O}$ = 0V

Notes 1. This parameter is sampled and not 100% tested.

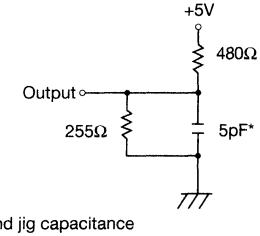
■ AC TEST CONDITIONS

- Input pulse levels: V_{SS} to 3.0V
- Input timing reference levels: 1.5V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5V

Output load (A)



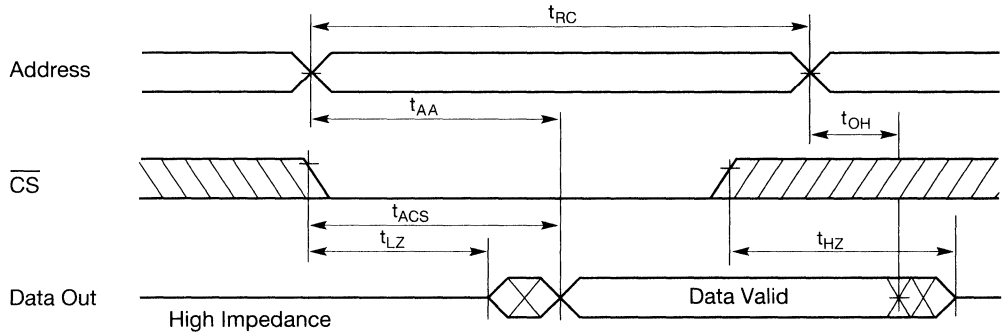
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ}, & t_{OW})



Note: * Including scope and jig capacitance

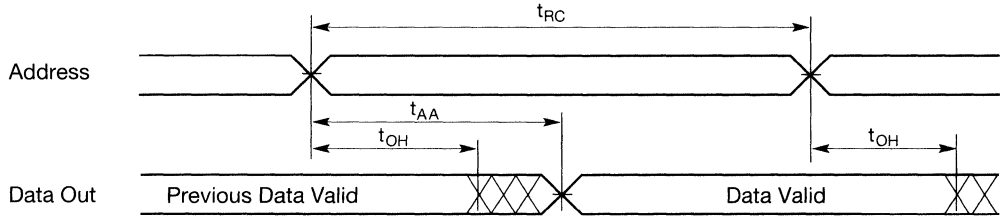
■ TIMING WAVEFORMS

Read Cycle No. – 1[1]



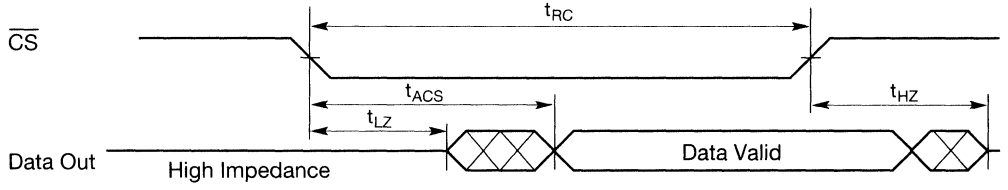
Notes: 1. $\overline{WE}$ = V_{IH}

Read Cycle – 2 [1, 2, 3]



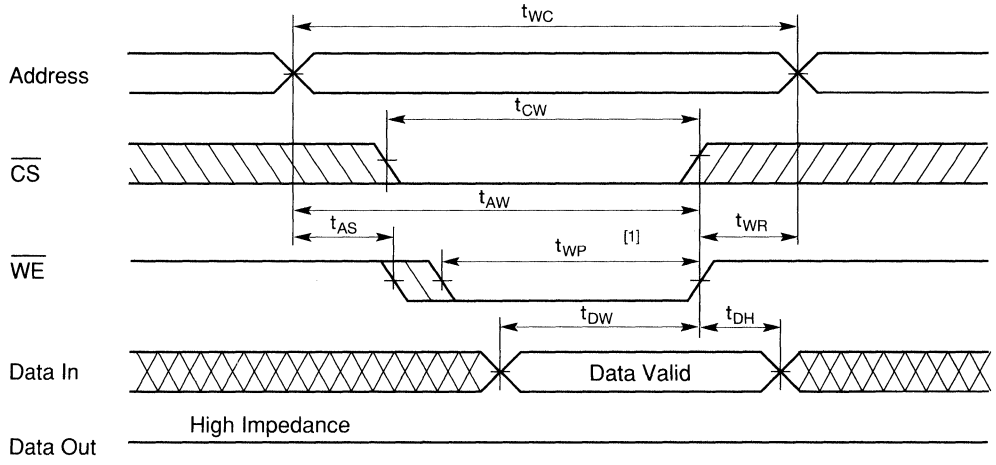
Notes: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}

Read Cycle –3 [1, 2, 3]



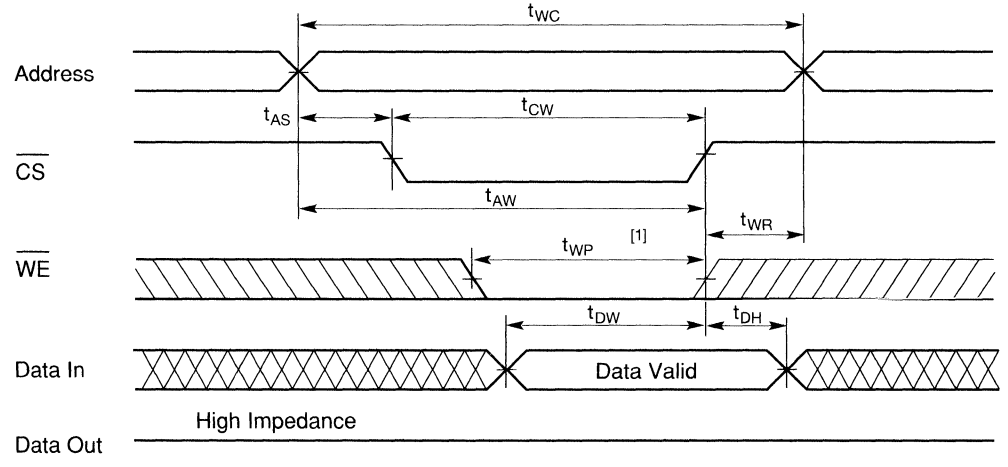
Notes: 1. $\overline{WE}$ = V_{IH}
2. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle –1[1]



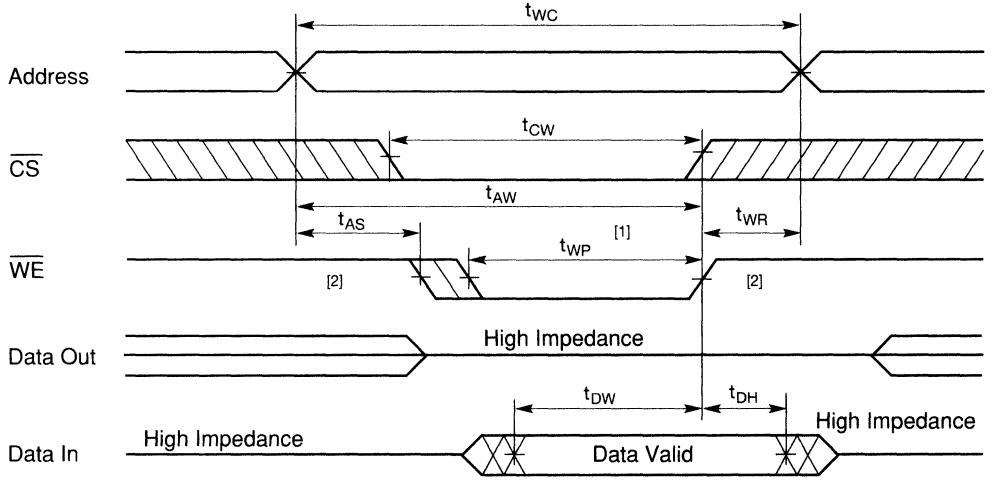
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle –2 [1]



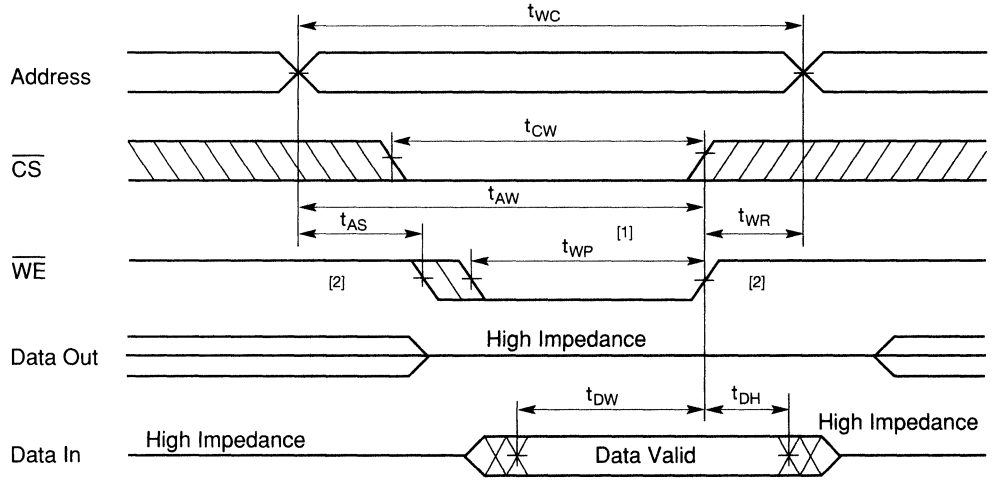
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle – 3 [1, 2]



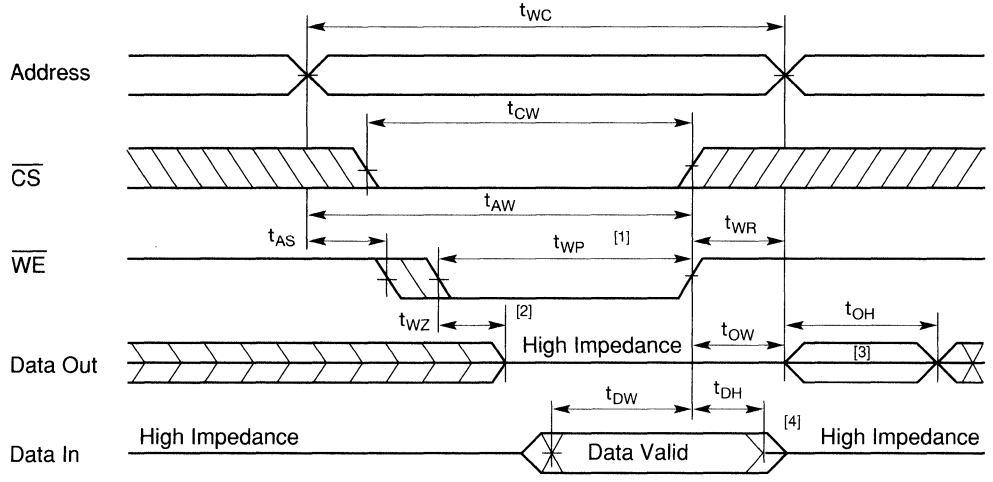
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input state of opposite phase to the outputs must not be applied.

Write Cycle – 4 [1, 2] ($\overline{OE}$ = Clocked $\overline{CS}$ Controlled)



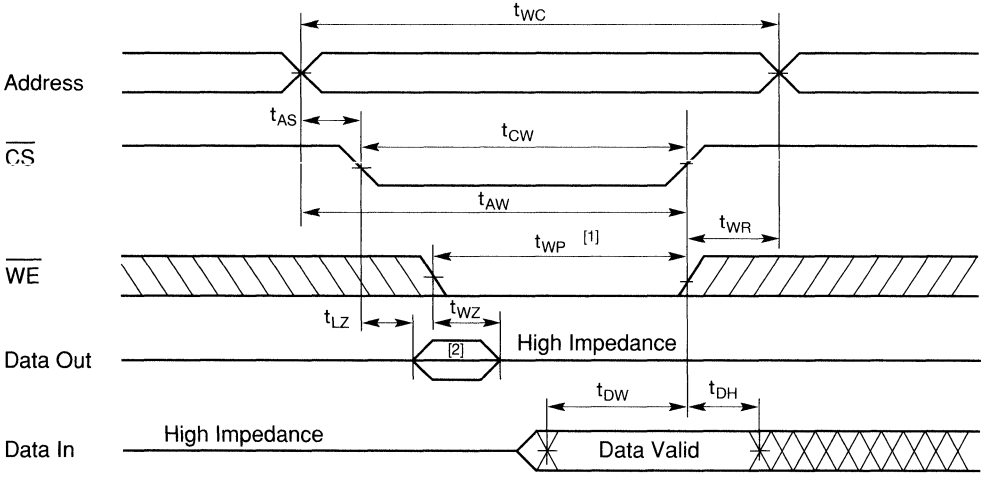
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle – 5 [1, 2, 3, 4]



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle – 6 [1, 2, 6]



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM6709 Series

65536-word × 4-bit High Speed Hi-BiCMOS Static RAM

The HM6709 Series has been converted to the HM6709A Series. The new A Series is completely compatible with the non-A Series.

Please refer to the specification comparison below to assist in your conversion.

		HM6709				HM6709A						
		20		25		15		20		25		
		min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	Unit
DC	IL_I		2		2		2		2		2	μA
	IL_O		10		10		10		10		10	μA
	I_{cc}		100		100		100		100		100	mA
	$I_{cc}1$		120		120		140		120		120	mA
	I_{sb}		30		30		30		30		30	mA
	$I_{sb}1$		10		10		10		10		10	mA
	V_{ol}		0.4		0.4		0.4		0.4		0.4	V
	V_{oh}	2.4		2.4		2.4		2.4		2.4		V
Read	t_{RC}	20		25		15		20		25		ns
	t_{AA}		20		25		15		20		25	ns
	t_{ACS}		20		25		15		20		25	ns
	t_{OH}	5		5		4		5		5		ns
	t_{LZ}	0		0		4		★4		★4		ns
	t_{HZ}	0	8	0	10	0	6	0	8	0	10	ns
	t_{OE}	0	10	0	10	0	7	0	10	0	10	ns
	t_{OLZ}	0		0		0		0		0		ns
Write	t_{WC}	20		25		15		20		25		ns
	t_{CW}	15		20		10		15		20		ns
	t_{AW}	15		20		10		15		20		ns
	t_{AS}	0		0		0		0		0		ns
	t_{WP}	15		20		10		15		20		ns
	t_{WR}	1.5		1.5		0		★0		★0		ns
	t_{DW}	12		15		8		★10		★12		ns
	t_{DH}	0		0		0		0		0		ns
	t_{WZ}	0	8	0	10	0	6	0	8	0	10	ns
	t_{OHZ}	0	8	0	10	0	6	0	8	0	10	ns
	t_{OW}	0		0		0		0		0		ns

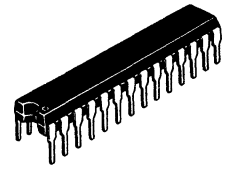
★ Modified specifications

HM6709A Series — Preliminary

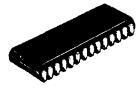
65536-Word × 4-Bit High Speed Static RAM

■ FEATURES

- 65536-words × 4 bit organization
- Fully TTL compatible input and output
- 1.0μm Hi-BiCMOS process
- +5V single supply
- Completely static memory
  No clock or timing strobe required
- Low power dissipation
  Operating: 450mW (typ.)
- Super fast
  Access time: 15/20/25 ns (max.)
  $\overline{OE}$ access time: 7/10/10ns (max.)



(DP-28N)

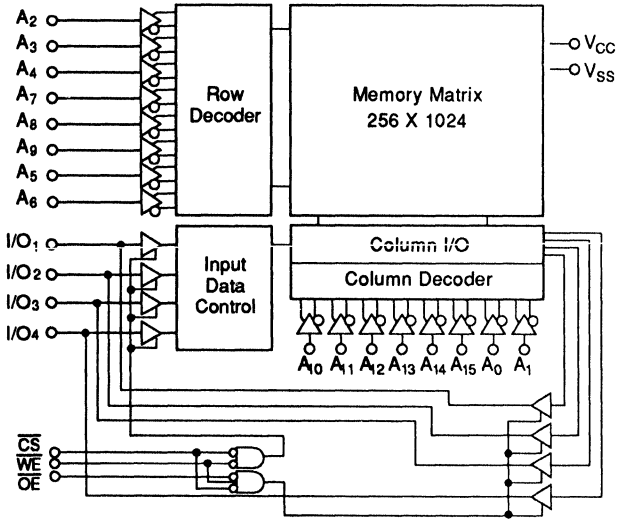


(CP-28DN)

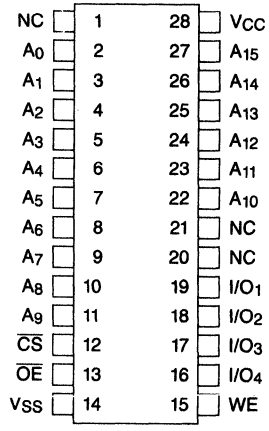
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6709AP-15	15ns	300 mil 28 pin
HM6709AP-20	20ns	Plastic DIP
HM6709AP-25	25ns	(DP-28N)
HM6709AJP-15	15ns	300 mil 28 pin
HM6709AJP-20	20ns	Plastic SOJ
HM6709AJP-25	25ns	(CP-28DN)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{15}	Address Input
I/O_1-I/O_4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
V_{SS}	Ground
V_{CC}	Power Supply

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	-3.0	—	0.8	V

*Pulse width: 15ns, DC: -0.5V

■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5.0\ V \pm 10\%$, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6709A-15			HM6709A-20/25			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5\ V$, $V_{IN}=0\ V$ to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $\overline{WE}=V_{IL}$ $V_{I/O}=0\ V$ to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0\ mA$	—	—	100	—	—	100	mA
Average Operating Current	I_{CC1}	min. cycle, Duty: 100% $I_{I/O}=0\ mA$	—	—	140	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$, $V_{IN}=V_{IH}$ or V_{IL}	—	—	30	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2\ V$ $V_{IN} \leq 0.2\ V$ or $V_{IN} \geq V_{CC}-0.2V$	—	—	10	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8\ mA$	—	—	0.4	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-.4\ mA$	2.4	—	—	2.4	—	—	V

■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Max.	Unit	Test Condition
Input Capacitance	C_{IN}[1)]	6	pF	$V_{IN}=0\ V$
Output Capacitance	$C_{I/O}$[1)]	10	pF	$V_{I/O}=0\ V$

NOTES: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC}=5 V ± 10%, Ta=0 to +70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns
Address Access Time	t_{AA}	—	15	—	20	—	25	ns
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns
Chip Selection to Output in Low Z	t_{LZ}[1), 2)]	4	—	4	—	4	—	ns
Output Enable to Output Valid	t_{OE}	0	7	0	10	0	10	ns
Output Enable to Output in Low Z	t_{OLZ}[1), 2)]	0	—	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{HZ}[1), 2)]	0	6	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	4	—	5	—	5	—	ns

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

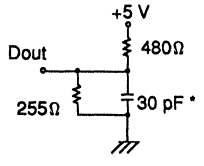
• Write Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}[1)]	15	—	20	—	25	—	ns
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	8	—	10	—	12	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[2), 3)]	0	6	0	8	0	10	ns
Output Disable to Output in High Z	t_{OHZ}[2), 3)]	0	6	0	8	0	10	ns
Output Active from End of Write	t_{OW}[2), 3)]	0	—	0	—	0	—	ns

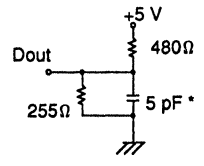
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

■ AC TEST CONDITIONS

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 2.5 V



Output Load A

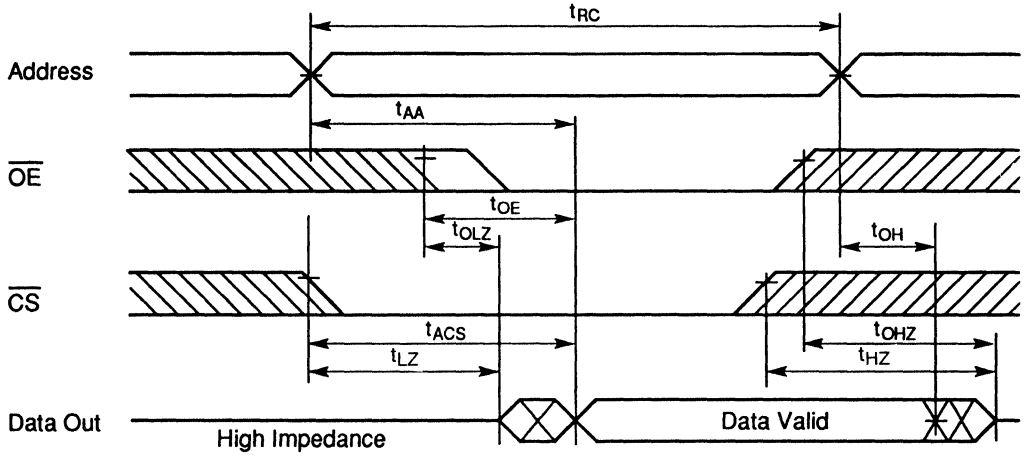


Output Load B
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ} & t_{OW})

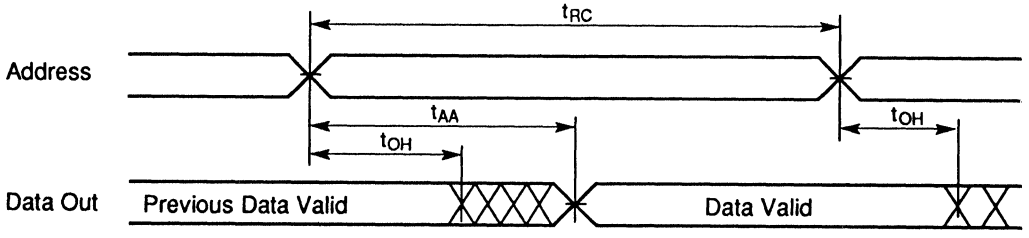
*Including scope and jig capacitance.

■ TIMING WAVEFORM

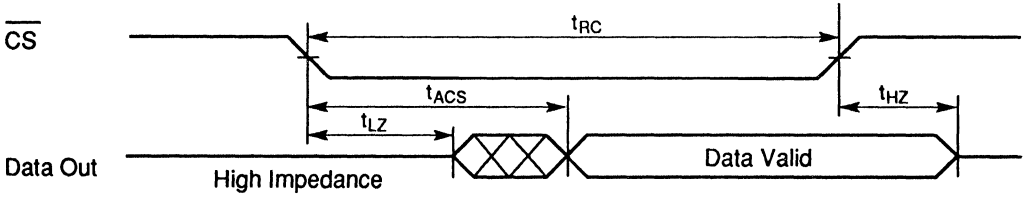
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)

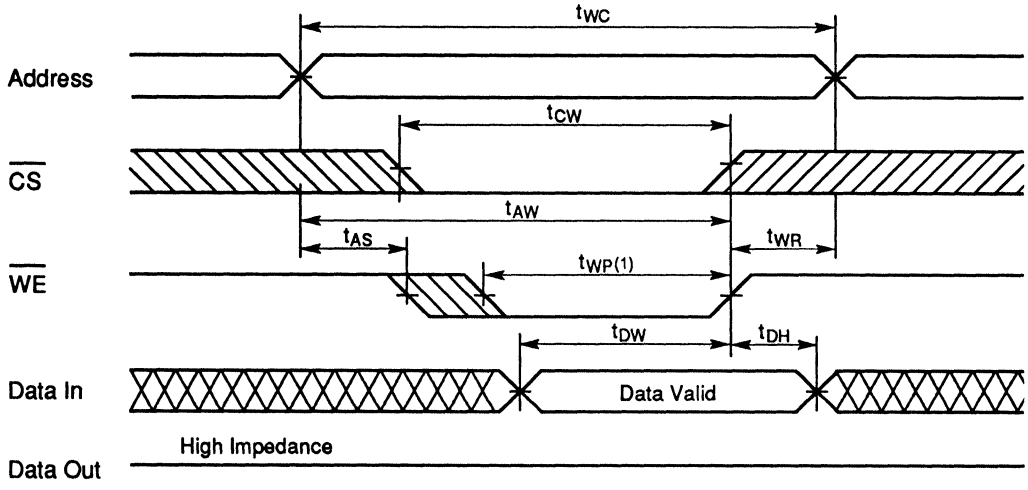


• **Read Cycle (3)** (1) (3) (4)

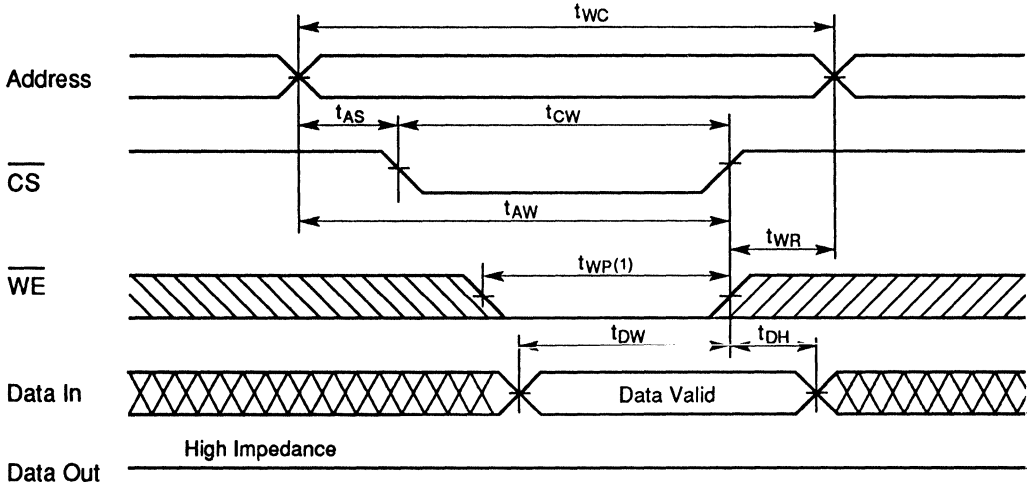


NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}.
3. $\overline{OE}$ = V_{IL}.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

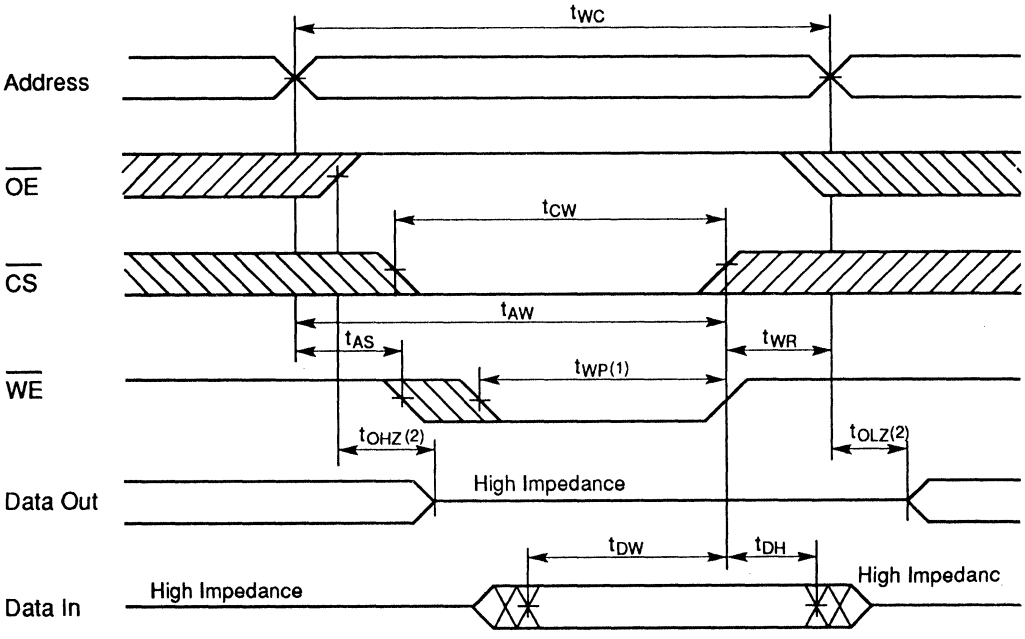
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



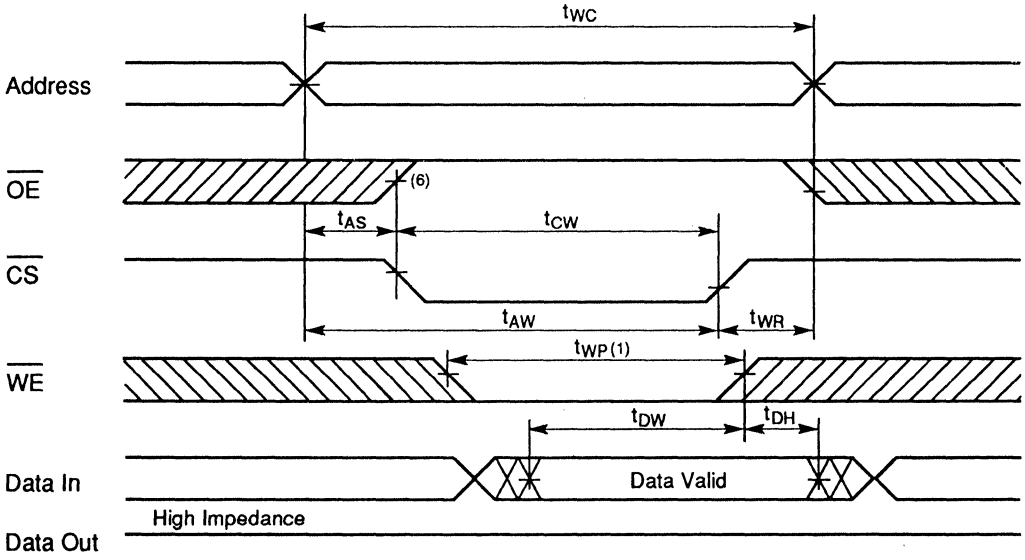
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



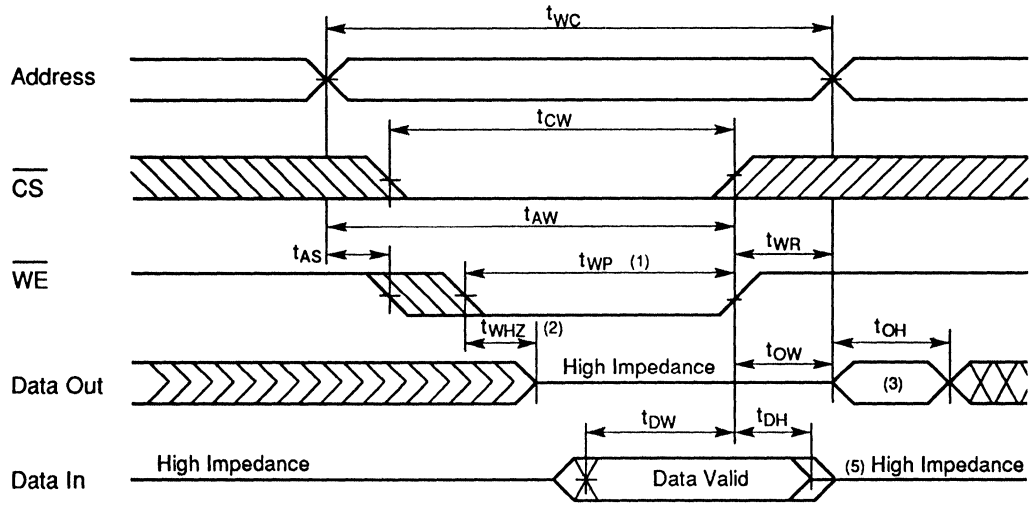
• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



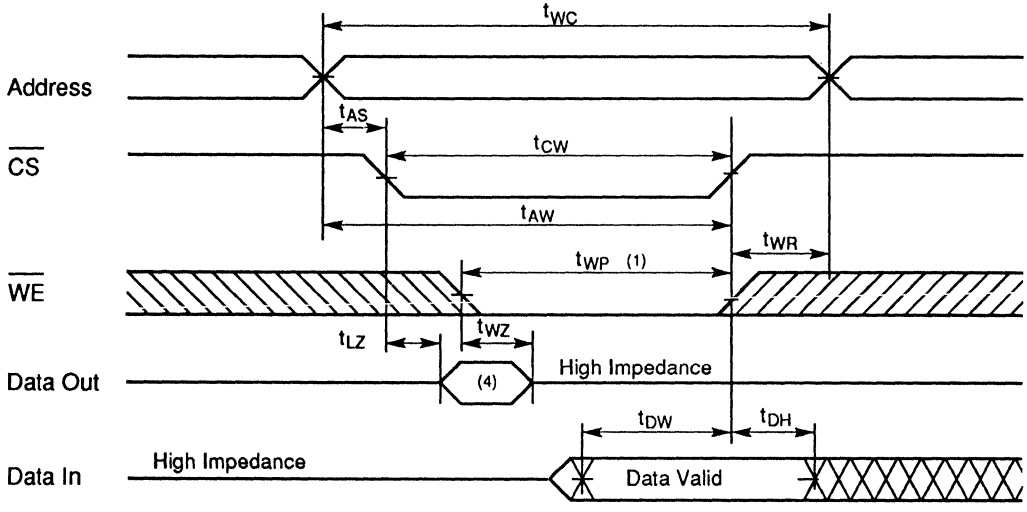
• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

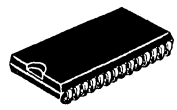
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6709SH Series — Preliminary

65,536-words x 4-Bit High Speed Static Random Access Memory

■ FEATURES

- 65,536-words x 4 bit organization
- Directly TTL compatible input and output
- 0.8 μm Hi-BiCMOS process
- +5V single supply
- Completely static memory
- No clock or timing strobe
- Low power dissipation (DC) operating: 400mW typ
- Super fast access time: 10/12ns (max)



(CP-28DN)

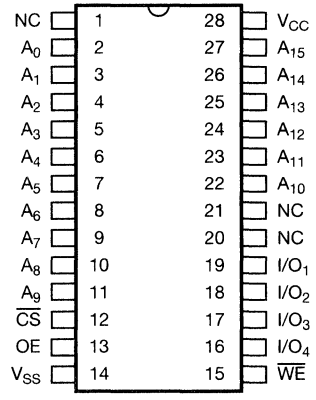
■ ORDERING INFORMATION

Type No.	Organ-ization	Access Time	Package
HM6709SH-10 HM6709SH-12	64kx4 with $\overline{OE}$	10 ns 12 ns	300 mil 28 pin Plastic SOJ (CP-28DN)

■ PIN DESCRIPTION

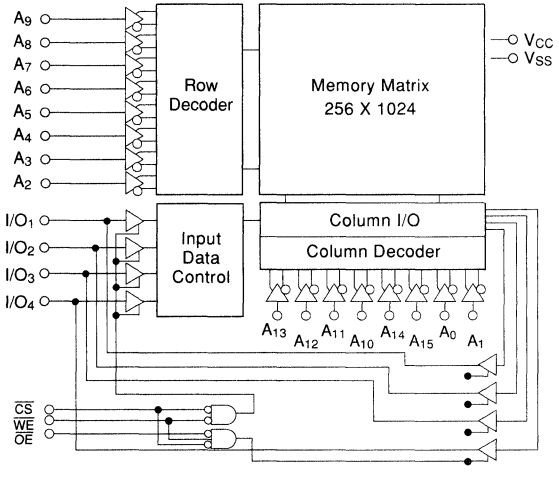
Pin Name	Function
A_0–A_{15}	Address Input
I/O_1–I/O_4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
V_{SS}	Ground
NC	Not Connect

HM6709SH Series



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

Input			Output	Mode	V_{CC} Current	Ref. Cycle
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$				
H	X	X	High Z	Not Selected	I_{SB}, I_{SB1}	–
L	H	H	High Z	Output Disable	I_{CC}, I_{CC1}	–
L	H	L	Data In	Read	I_{CC}, I_{CC1}	Read Cycle (1), (2), (3)
L	L	H	Data In	Write	I_{CC}, I_{CC1}	Write Cycle (1), (2), (3), (4)
L	L	L	Data In	Write	I_{CC}, I_{CC1}	Write Cycle (5), (6)

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
Supply Voltage[1]	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_t	-0.5 to V_{CC} +0.5	V
Power Dissipation	P_t	1.0	W
Operating Temperature Range	T_{ppr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg} (bias)	–10 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Note: 1. With respect to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	-3.0[1]	—	0.8	V

Note: 1. Pulse width 10 ns, DC: -0.5V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_a = 0°C to +70°C)

Item	Symbol	Test Conditions	-10			-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage	$I_{IL1}I$	V_{CC} = 5.5V, V_{IN}=0V to V_{CC}	–	–	2	–	–	2	µA
Output Leakage Current	I_{IL01}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} V_{IO} = 0V to V_{CC}	–	–	10	–	–	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	60	100	–	60	100	mA
Average Operating Current	I_{CC1}	15ns cycle, $I_{I/O}$ = 0mA	–	130	180	–	120	175	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} =V_{IH} or V_{IL}	–	–	40	–	–	40	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} = 0.2V V_{IN} ≤ 0.2Vor V_{IN} ≥ V_{CC} = 0.2V	–	–	30	–	–	30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = .4mA	2.4	–	–	2.4	–	–	V

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	10	–	12	–	ns
Address Access Time	t_{AA}	–	10	–	12	ns
Chip Select Access Time	t_{ACS}	–	10	–	12	ns
Chip Selection to Output in Low Z	t_{LZ}[1, 2]	3	–	4	–	ns
Output Enable to Output Valid	t_{OE}	–	5	–	6	ns
Output Enable to Output in Low Z	t_{OLZ}[1,2]	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{HZ}[1,2]	0	5	0	5	ns
Output Hold from Address Change	t_{OH}	3	–	4	–	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

• Write Cycle

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}[1]	11	–	12	–	ns
Chip Selection to End of Write	t_{CW}	8	–	9	–	ns
Address Valid to End of Write	t_{AW}	10	–	11	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	8	–	9	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	6	–	6	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enable to Output in High Z	t_{WZ}[2,3]	0	5	0	6	ns
Output Disable to Output in High Z	t_{OHZ}[2,3]	0	6	0	6	ns
Output Active from End of Write	t_{OW}[2,3]	4	–	4	–	ns

Notes: 1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured in ± 200 mV from steady state voltage with specified loading in load (B).

• **Capacitance**

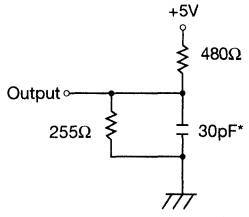
Item	Symbol	Max.	Unit	Test Condition
Input Capacitance	C_{in}[1]	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$[1]	10	pF	$V_{I/O}$ = 0V

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = to 70°C)

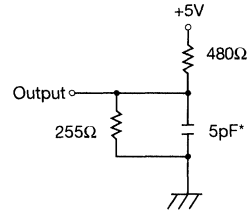
Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input timing reference levels: 1.5V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5V

Output load (A)

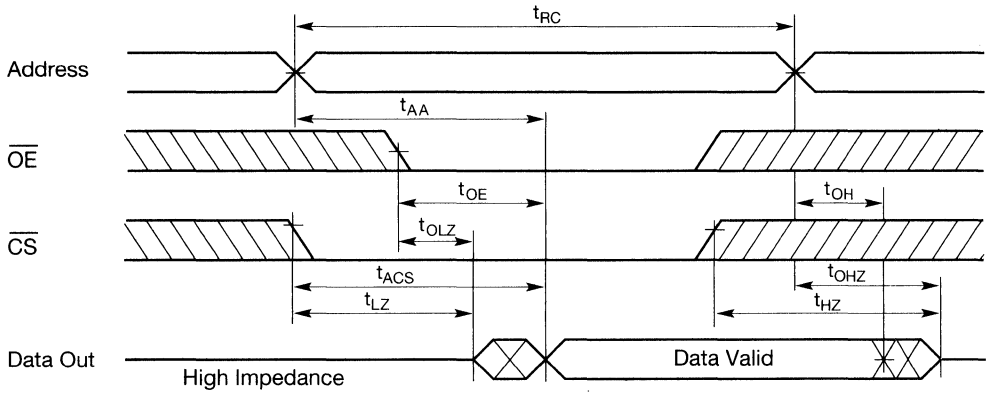


Output Load (B)
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ}, & t_{OW})



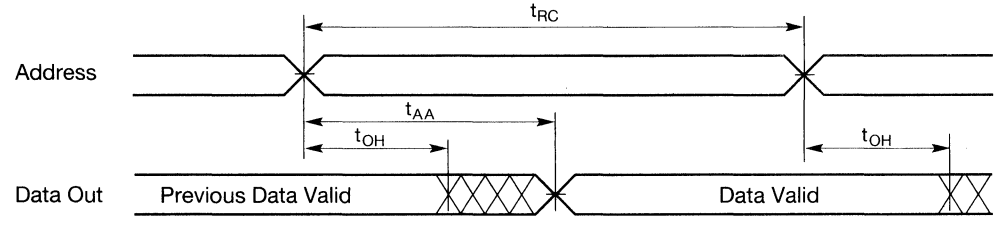
Note: * Including scope and jig capacitance

■ READ CYCLE (1)[1]



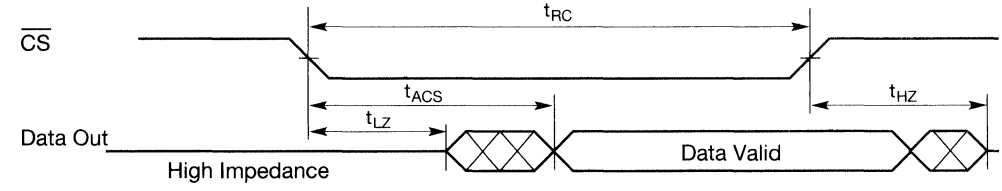
Notes: 1. $\overline{WE} = V_{IH}$

■ READ CYCLE (2)[1,2,3]



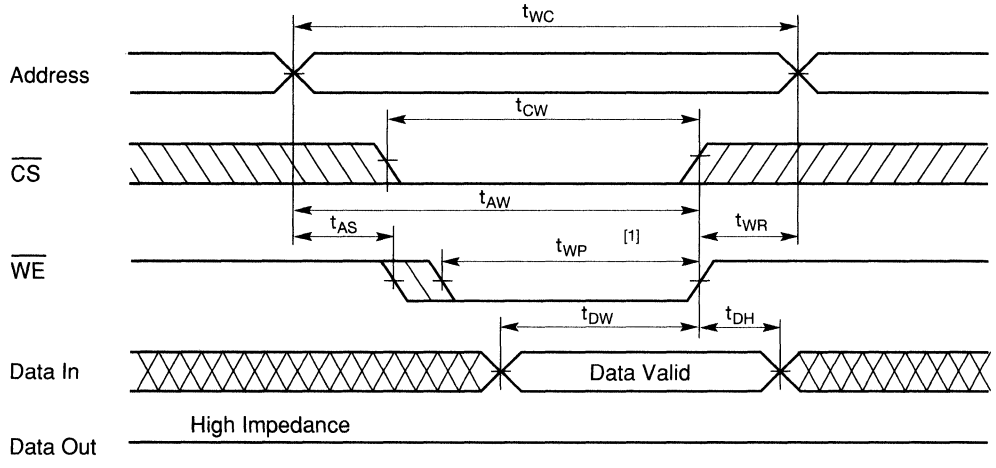
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

■ READ CYCLE (3)[1,2,3]



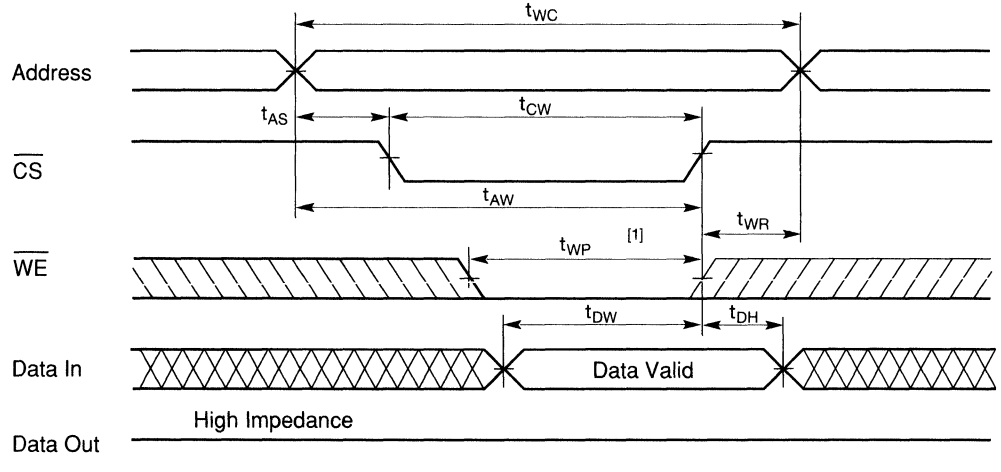
Notes: 1. $\overline{WE} = V_{IH}$
2. $OE = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ WRITE CYCLE (1)[1] ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



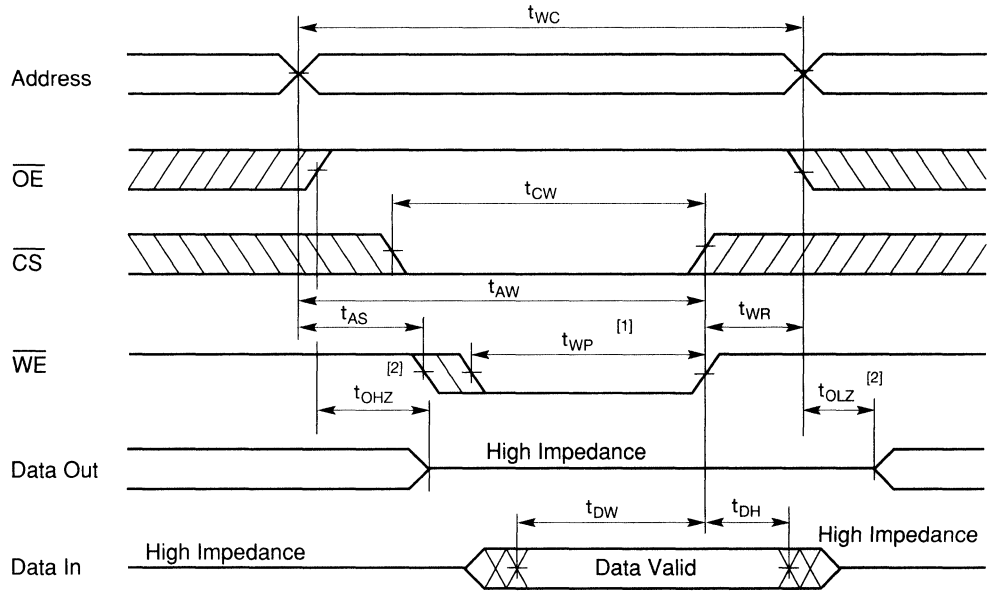
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).

■ WRITE CYCLE (2)[1] ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



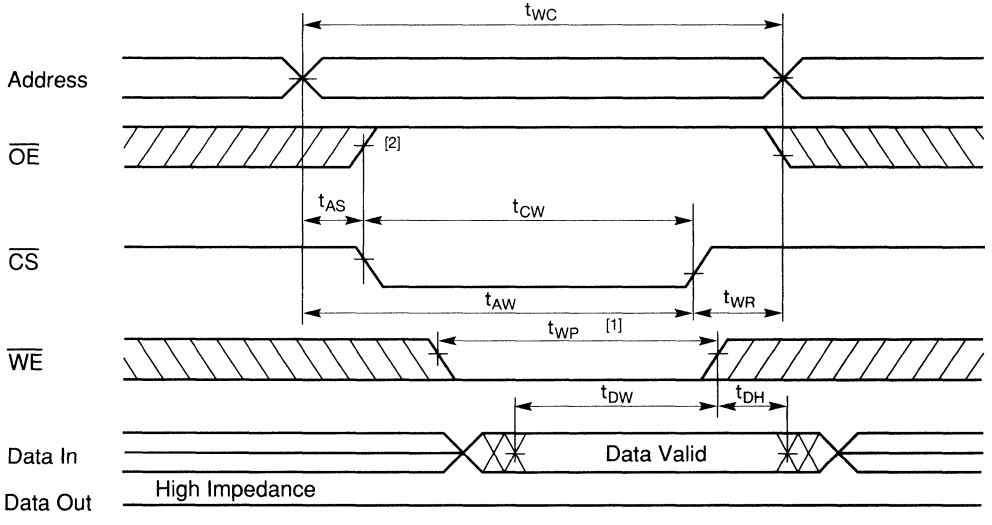
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).

■ WRITE CYCLE (3)[1,2] ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



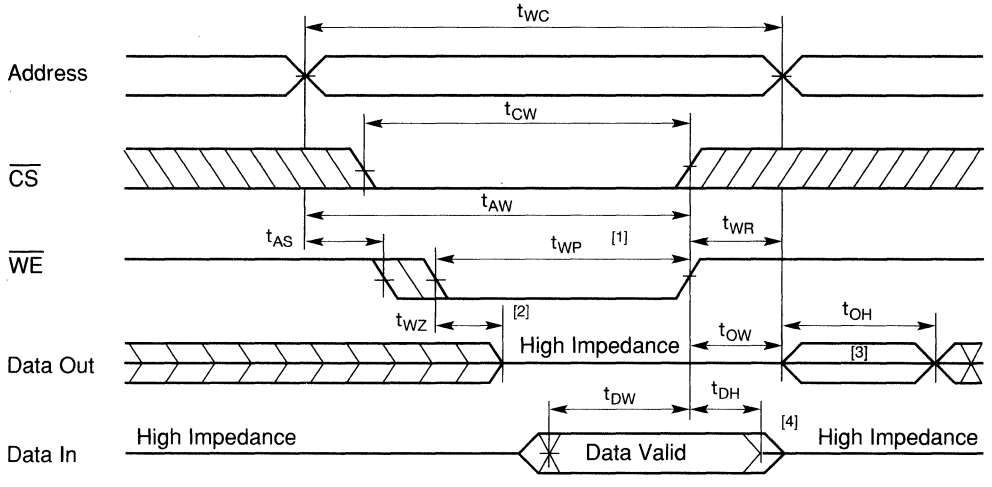
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).
2. During this period, I/O pins are in the output state so that the input state of opposite phase to the outputs must not be applied.

■ WRITE TIMING WAVEFORM (4)[1,2] ($\overline{OE}$ = Clocked $\overline{CS}$ Controlled)



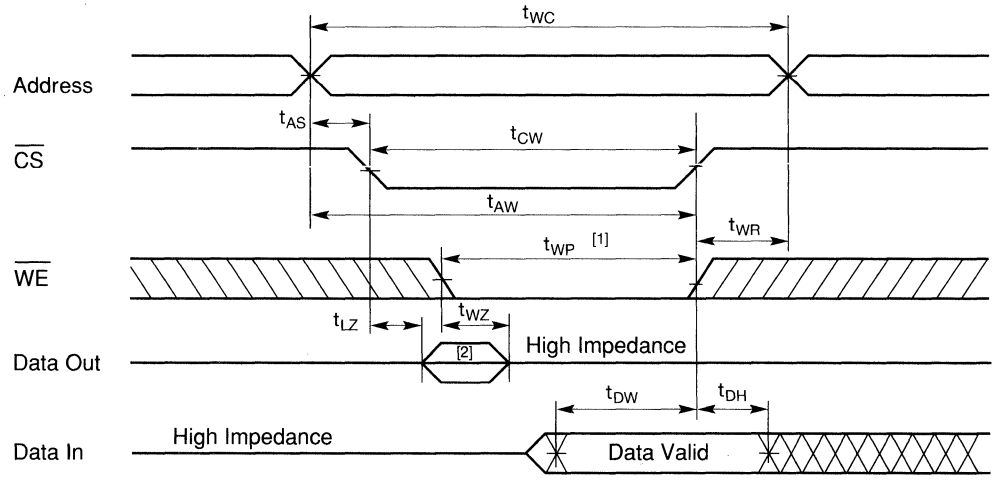
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).

■ WRITE CYCLE (5)[1,2,3,4] ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

■ WRITE CYCLE (6)[1,2,3,4] ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



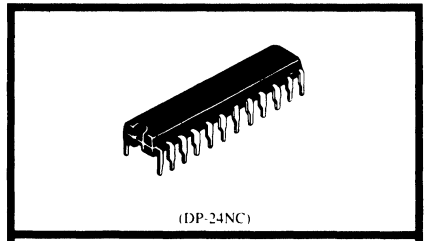
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

HM6207H Series

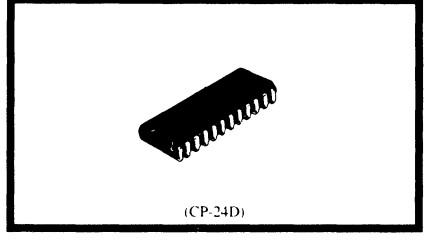
262144-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6207H is a high speed 256k static RAM organized as 256k-word × 1 bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous wherever high speed and high density memory is required.

The HM6207H is packaged in the industry standard 300-mil, 24-pin, plastic DIP. The HM6207H is also available in a 300-mil, 24-pin plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.



(DP-24NC)



(CP-24D)

Features

- Single 5 V supply and high density 24-pin package
- High speed
  Access time: 25/35 ns (max.)
- Low power
  Active: 300 mW (typ.)
  Standby: 100 μW (typ.)
  30 μW (typ.) (L-version)
- Completely static memory requires
  No clock or timing strobe requires
- Equal access and cycle time
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

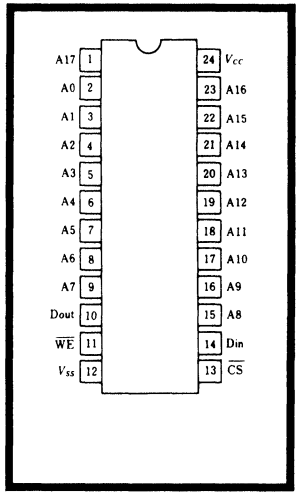
Ordering Information

Type No.	Access Time	Package
HM6207HP-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6207HP-35	35 ns	
HM6207HLP-25	25 ns	
HM6207HLP-35	35 ns	
HM6207HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6207HJP-35	35 ns	
HM6207HJLP-25	25 ns	
HM6207HJLP-35	35 ns	

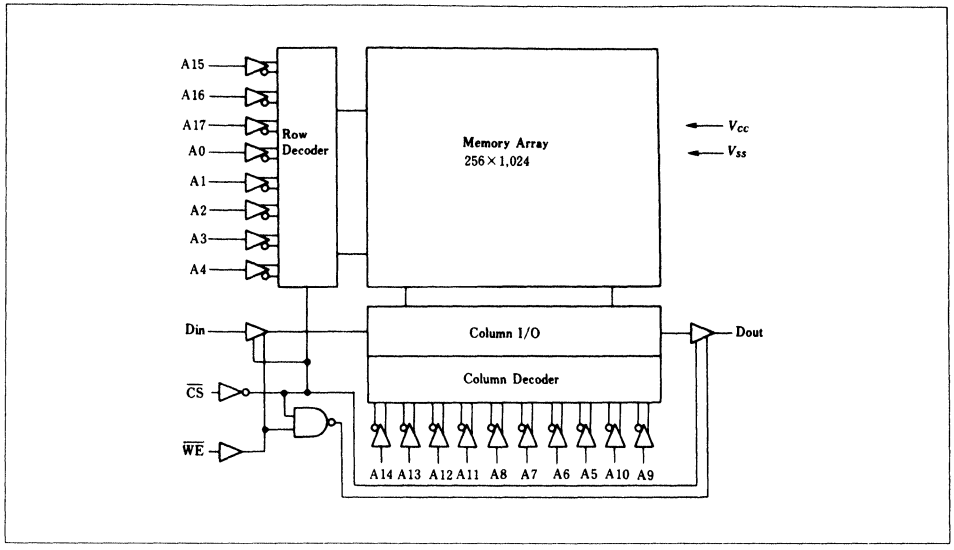
Pin Description

Pin Name	Function
A0 – A17	Address
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Pin Arrangement



Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	High-Z	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item		Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current		$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current		$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current		I_{CC}	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle, Duty = 100%
Standby Power Supply Current		I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. Cycle
Standby Power Supply Current	"H" Version	I_{SB}	—	20	40	mA	
Standby Power Supply Current (1)		I_{SB1}	—	20	2000	μA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Standby Power Supply Current (1)	L-Version	I_{SB1}	—	6	100	μA	
Output Low Voltage		V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage		V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	V_{out} = 0 V

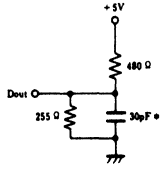
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

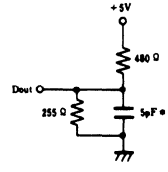
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for tHZ, tLZ, twz & tow)



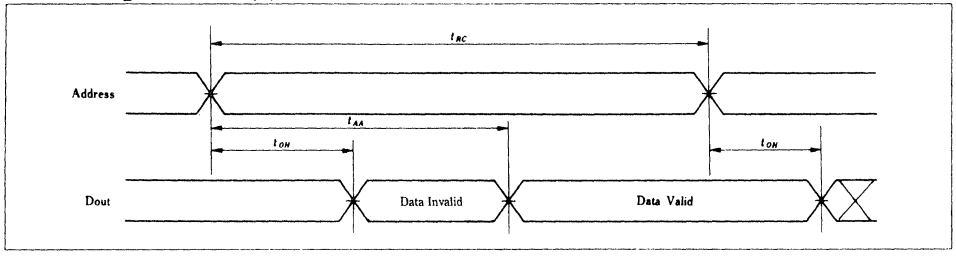
Note: * Including scope & jig.

Read Cycle

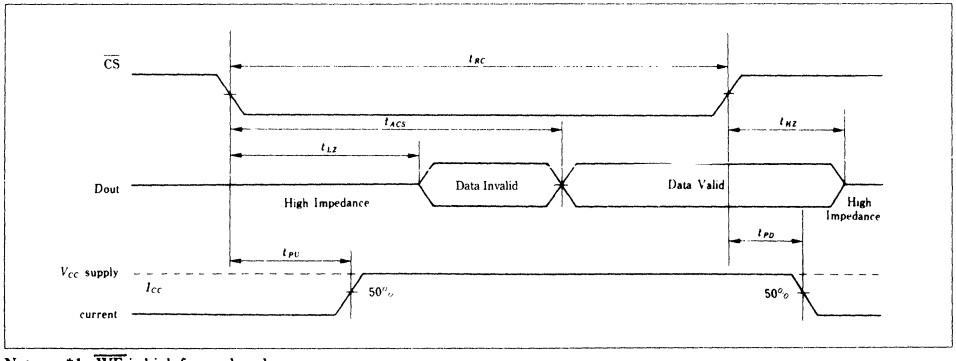
Item	Symbol	HM6207H-25		HM6207H-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Selection to Power Down Time	t_{PD}	—	15	—	25	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

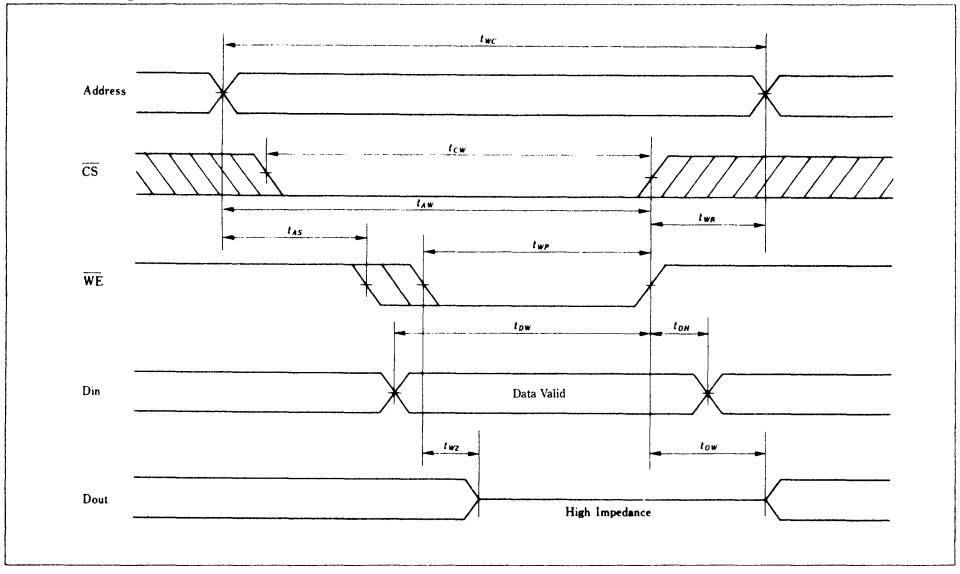
■ Write Cycle

Item		Symbol	HM6207H-25		HM6207H-35		Unit
			Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	25	—	35	—	ns
Chip Selection to End of Write		t_{CW}	20	—	30	—	ns
Address Valid to End of Write		t_{AW}	20	—	30	—	ns
Address Setup Time		t_{AS}	0	—	0	—	ns
Write Pulse Width		t_{WP}	20	—	30	—	ns
	"H" Version				25		
Write Recovery Time		t_{WR}	3	—	3	—	ns
Data Valid to End of Write		t_{DW}	15	—	20	—	ns
Data Hold Time		t_{DH}	0	—	0	—	ns
Write Enabled to Output in High-Z		t_{WZ}*1	0	8	0	10	ns
Output Active From End of Write		t_{OW}*1	0	—	0	—	ns

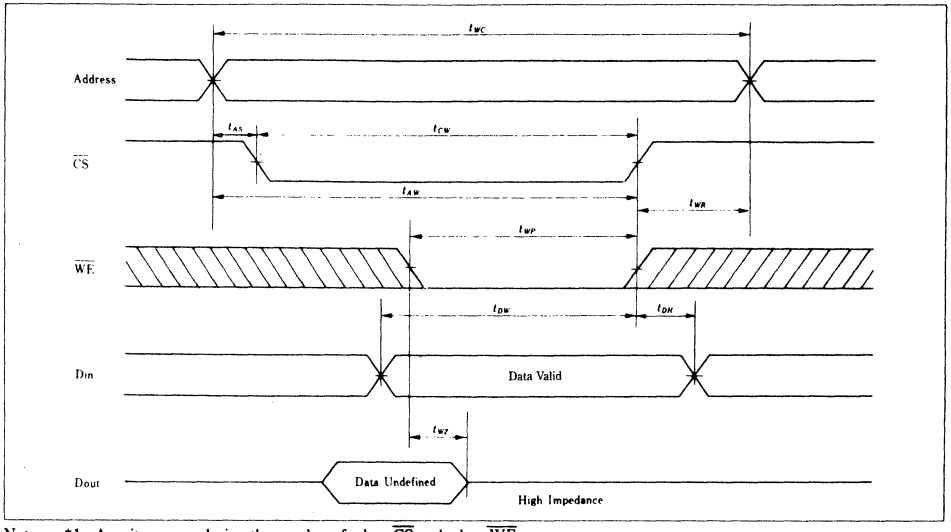
Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is ampled and not 100% tested.

2

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

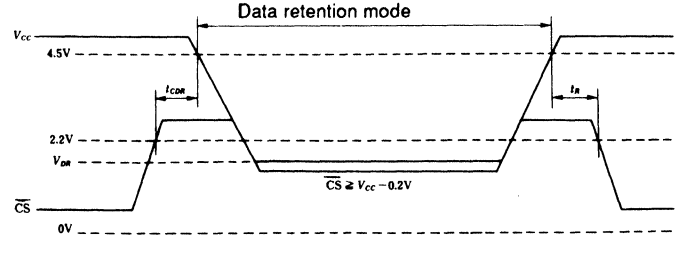
Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

These characteristics are guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50*2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Notes: *1. t_{RC} = read cycle time.
*2. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform



HM6707 Series

262144-word × 1-bit High Speed Hi-BiCMOS Static RAM

The HM6707 Series has been converted to the HM6707A Series. The new A Series is completely compatible with the non-A Series.

Please refer to the specification comparison below to assist in your conversion.

		HM6707				HM6707A						
		20		25		15		20		25		
		min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	Unit
DC	IL_I		2		2		2		2		2	μA
	IL_O		10		10		10		10		10	μA
	I_{cc}		100		100		100		100		100	mA
	$I_{cc}1$		120		120		140		120		120	mA
	I_{sb}		30		30		30		30		30	mA
	$I_{sb}1$		10		10		10		10		10	mA
	V_{ol}		0.4		0.4		0.4		0.4		0.4	V
	V_{oh}	2.4		2.4		2.4		2.4		2.4		V
Read	t_{RC}	20		25		15		20		25		ns
	t_{AA}		20		25		15		20		25	ns
	t_{ACS}		20		25		15		20		25	ns
	t_{OH}	5		5		4		5		5		ns
	t_{LZ}	5/0		5/0		4		★5		★5		ns
	t_{HZ}	0	8	0	15/10	0	6	0	8	0	★10	ns
Write	t_{WC}	20		25		15		20		25		ns
	t_{CW}	15		20		10		15		20		ns
	t_{AW}	15		20		10		15		20		ns
	t_{AS}	0		0		0		0		0		ns
	t_{WP}	15		20		10		15		20		ns
	t_{WR}	1.5		3		0		★0		★0		ns
	t_{DW}	15/12		20/15		8		★10		★12		ns
	t_{DH}	0		0		0		0		0		ns
	t_{WZ}	0	15/8	0	15/10	0	6	0	8	0	10	ns
	t_{OHZ}	0		0		0		0		0		ns

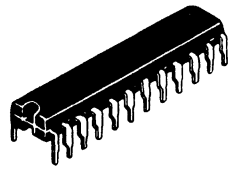
★ Modified specifications

HM6707A Series

262144-Word × 1-Bit High Speed Static RAM

■ FEATURES

- 262144-words × 1 bit organization
- Fully TTL compatible input and output
- 1.0μ Hi-BiCMOS process
- +5V single supply
- Completely static memory
  No clock or timing strobe required
- Low power dissipation
  Operating: 450mW typ.
- Super fast
  Access time: 15/20/25ns (max.)



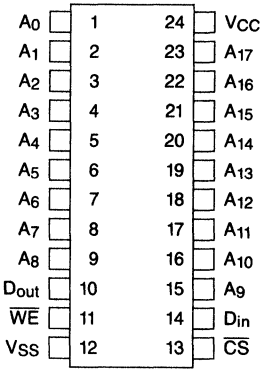
(DP-24NC)

(CP-24D)

■ ORDERING INFORMATION

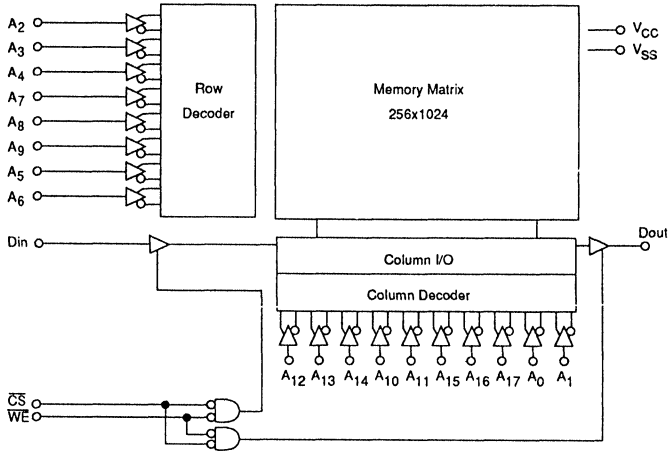
HM6707AP-15	15ns	300 mil 24 pin
HM6707AP-20	20ns	Plastic DIP
HM6707AP-25	25ns	(DP-24NC)
HM6707AJP-15	15ns	300 mil 24 pin
HM6707AJP-20	20ns	Plastic SOJ
HM6707AJP-25	25ns	(CP-24D)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{17}	Address Input
D_{in}	Data Input
D_{out}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{SS}	Ground
V_{CC}	Power Supply

■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	V_{CC} Current
H	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	Read	D_{out}	I_{CC}, I_{CC1}
L	L	Write	High Z	I_{CC}, I_{CC1}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-3.0*	—	0.8	V

NOTE: Pulse width 20ns, DC: -0.5 V

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5.0 V ± 10%, Ta=0 to 70°C)

Item	Symbol	Test Conditions	HM6707A-15			HM6707A-20/25			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5 V, V_{IN}=0 V to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=0 V to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT}=0 mA	—	—	100	—	—	100	mA
Average Operating Current	I_{CC1}	min. cycle, Duty: 100%, I_{OUT}=0 mA	—	—	140	—	—	120	mA
Standby Power Supply Current	I_{SB}	CS=V_{IH}, V_{IN}=V_{IH} or V_{IL}	—	—	30	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC}-0.2 V	—	—	10	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8 mA	—	—	0.4	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4 mA	2.4	—	—	2.4	—	—	V

■ AC CHARACTERISTICS (V_{CC}=5 V ± 10%, Ta=0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6707A-15		HM6707A-20		HM6707A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns
Address Access Time	t_{AA}	—	15	—	20	—	25	ns
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns
Output Hold from Address Change	t_{OH}	4	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}[1), 2)]	4	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}[1), 2)]	0	6	0	8	0	10	ns

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

• **Write Cycle**

Item	Symbol	HM6707A-15		HM6707A-20		HM6707A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}[1]	15	—	20	—	25	—	ns
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	12	—	15	—	20	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	10	—	10	—	12	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[2), 3)]	0	6	0	8	0	10	ns
Output Active from End of Write	t_{OW}[2), 3)]	0	—	0	—	0	—	ns

NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

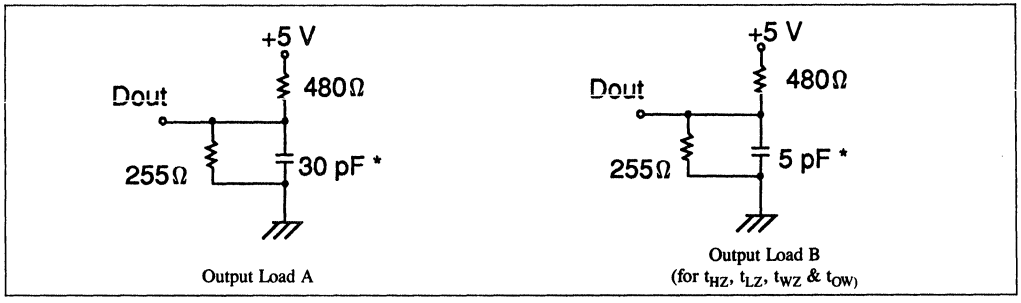
■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Max.	Unit	Test Condition
Input Capacitance	C_{IN}[1]	6	pF	V_{IN}=0 V
Output Capacitance	C_{OUT}[1]	10	pF	V_{OUT}=0 V

NOTES: 1. This parameter is sampled and not 100% tested.

■ AC TEST CONDITIONS

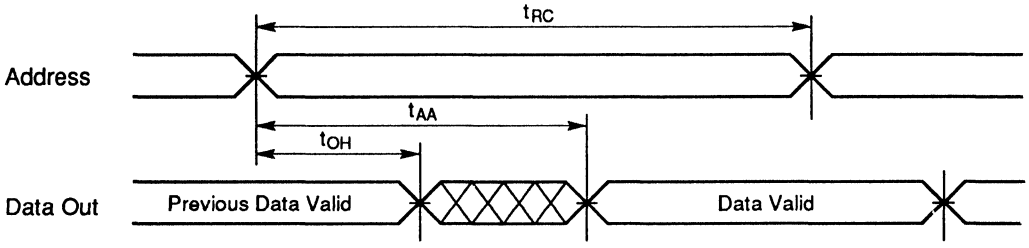
- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5 V



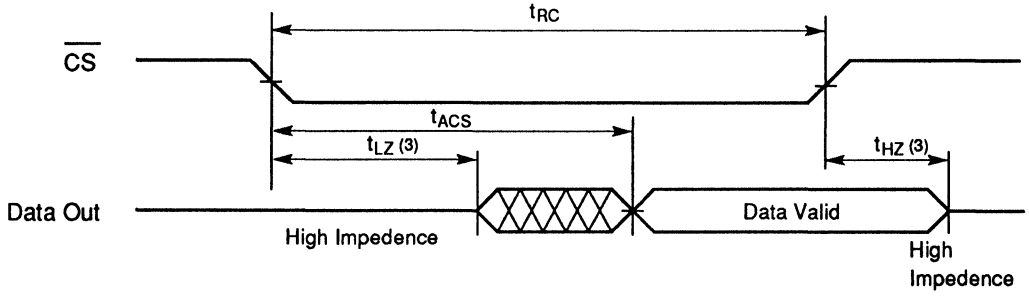
*Including scope and jig capacitance.

■ TIMING WAVEFORM

• **Read Cycle (1)** (1)

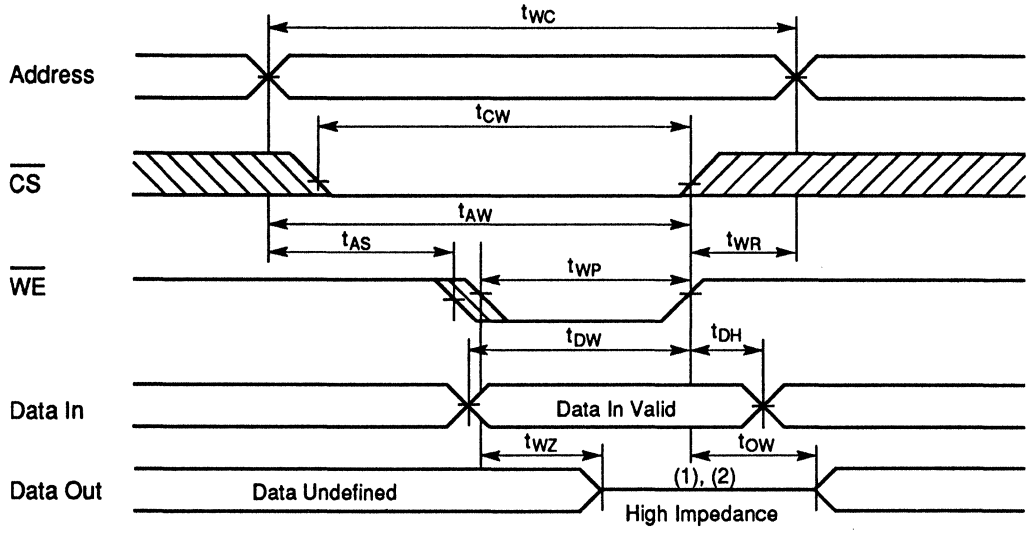


• **Read Cycle (2)** (2)



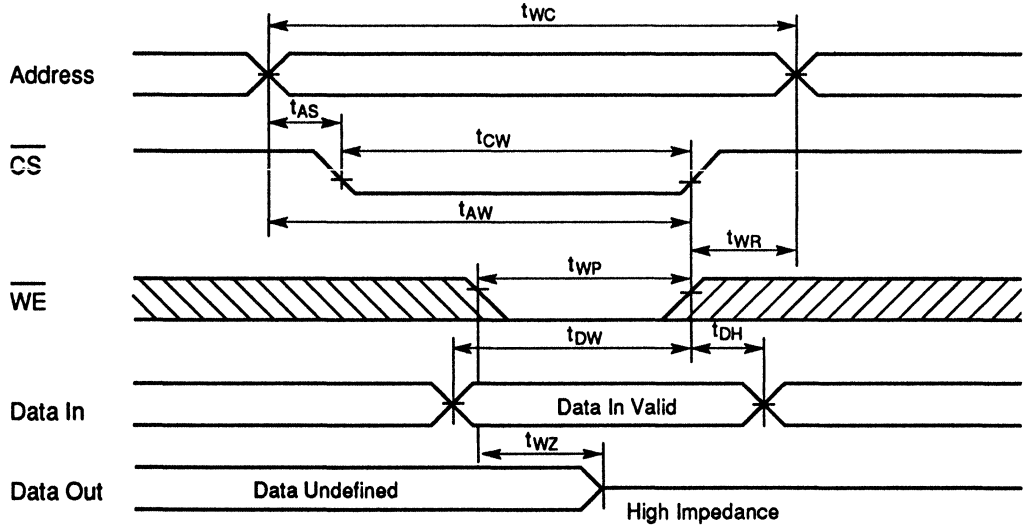
NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



NOTES: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

• **Write Cycle (2)** ($\overline{CS}$ Controlled)



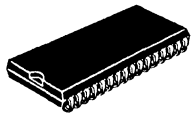
NOTES: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

HM62932 Series — Preliminary

32,768-Word x 9-Bit High Speed CMOS Static Ram

■ FEATURES

- High speed: fast access time 15/20 ns (max)
- Low Power
  Standby: 15μW (typ.) (L-version)
  Operation: 350mW (typ.)
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output—Three state output
- Directly TTL compatible—All inputs and outputs



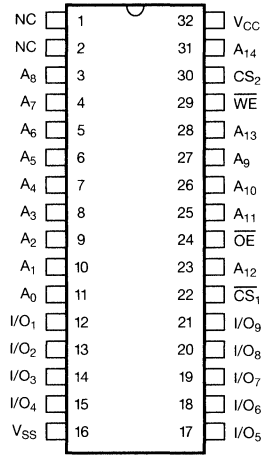
(CP-32DN)

■ ORDERING INFORMATION

Type No.	Access	Package
HM62932JP-15	15 ns	300 mil 32 pin Plastic SOJ (CP-32DN)
HM62932JP-20	20 ns	
HM62932LJP-15	15 ns	
HM62932LJP-20	20 ns	

■ PIN ARRANGEMENT

HM62932 Series

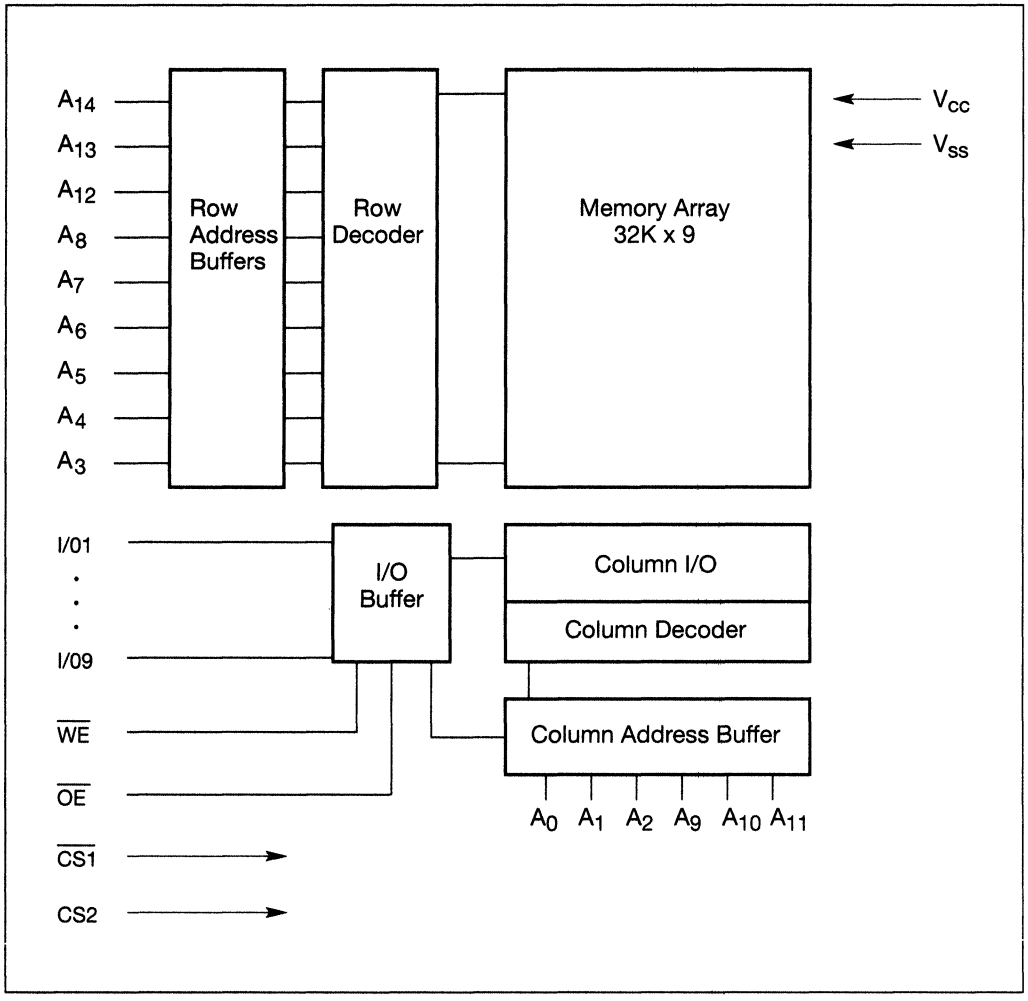


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A14	Address
I/O1–I/O9	Data Input/Output
$\overline{CS}_1$	Chip Select 1
$\overline{CS}_2$	Chip Select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
VSS	Ground

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	L	X	X	Standby	I_{CC}	High-Z	—
L	H	H	H	Output Disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read Cycle 1,2,3
L	H	H	L	Write	I_{CC}	Din	Write Cycle 1
L	H	L	L	Write	I_{CC}	Din	Write Cycle 2

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage 1	V_{CC}	-0.5[2] + 7.0	V
Voltage on any pin relative to V_{SS}[1]	V_T	–0.5 [2] to V_{CC} + 0.5	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature Under Bias	T_{bias}	–10 to +85	°C

Note: 1. With respect to V_{SS}
2. V_{CC} and V_T min = –2.5V for pulse width 10ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low (Logic 0) Voltage	V_{IL}	–0.5[1]	—	0.8	V

Note: 1.V_{IL} min = –2.0V for pulse width 10ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{CC} = 0V)

Item	Symbol	Min.	Typ[1]	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} =5.5V., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	µA	Output Disable $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC}	—	70	TBD	mA	$\overline{CS}_1$ = V_{IL} I_{out} = 0 mA, min. cycle
Standby V_{CC} Current	I_{SB}	—	30	TBD	mA	$\overline{CS}_1$ = V_{IH}, min cycle
Standby V_{CC} Current (1)	I_{SB1} (L-version)	—	0.02	2.0	mA	*2
		—	0.003	0.1		
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Note: 1. Typical limits are at V_{CC} = 5.0 V, T_a = 25°C and specified loading.
2. $\overline{CS}_1$ V_{CC} –0.2V, 0V V_{in} 0.2V or V_{CC} –0.2V V_{in}

■ CAPACITANCE (T_a = 25°C, f = 1.0 MHz)[1]

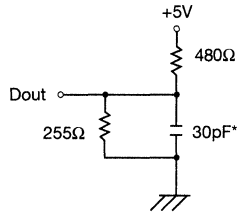
Item	Symbol	Min	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0V
Output Capacitance	C_{out}	—	—	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.5

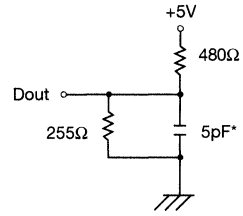
■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} 5V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 4ns
- Input and Output timing reference levels: 1.5V
- Output load: See figures



Output Load (A)



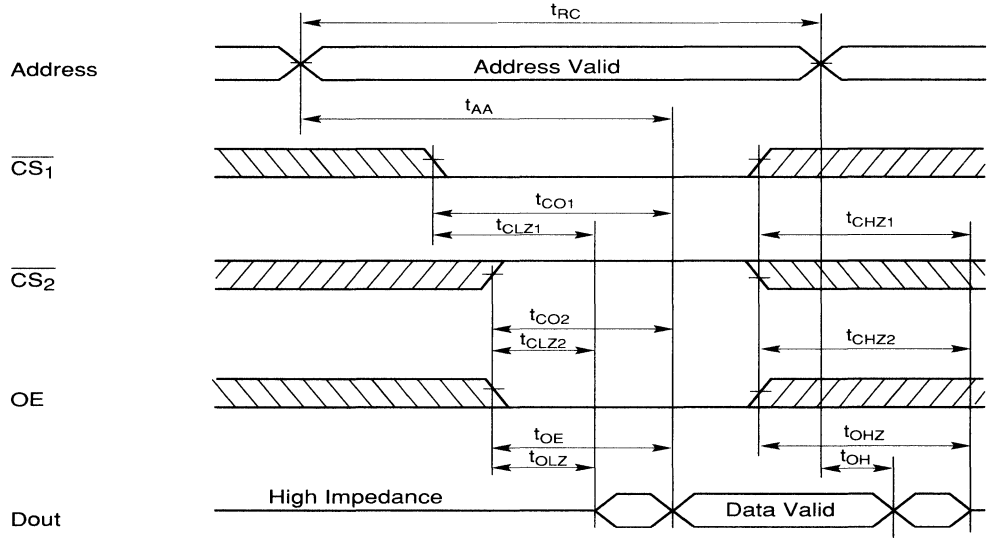
Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})

* Including scope & jig.

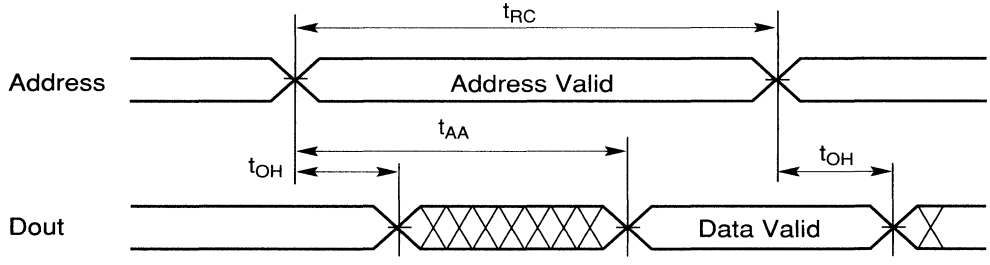
■ READ CYCLE

Item	Symbol	HM62932–15		HM62932–20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	—	20	—	ns
Address Access Time	t_{AA}	—	15	—	20	ns
Chip Select Access Time	t_{CO1}	—	15	—	20	ns
	t_{CO2}	—	7	—	10	ns
Chip Selection to Output in Low-Z	t_{CLZ1}[1]	3	—	3	—	ns
	t_{CLZ2}[1]	0	—	0	—	ns
Output Enable to Output Valid	t_{OE}	—	7	—	10	ns
Output Enable to Output in Low-Z	t_{OLZ}[1]	0	—	0	—	ns
Chip deselection to Output in High-Z	t_{CHZ1}, t_{CHZ2}*[1]	0	7	0	10	ns
Chip Disable to Output in High-Z	t_{OHZ}[1]	0	7	0	10	ns
Output Hold from Address Change	t_{OH}	3	—	3	—	ns

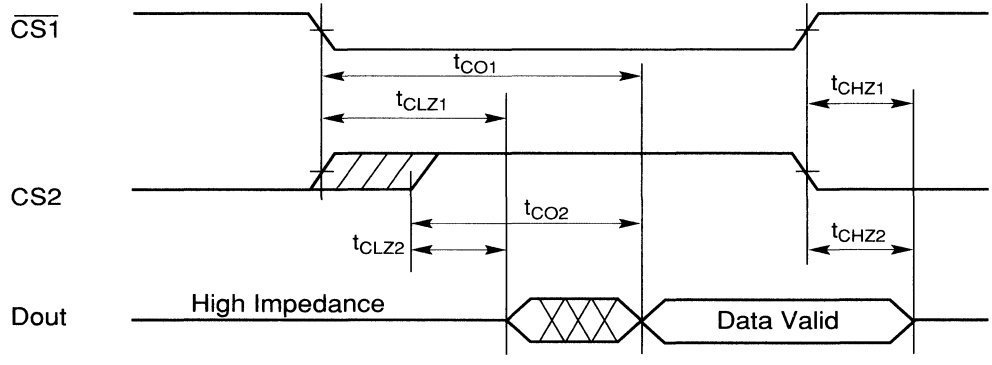
■ READ TIMING WAVEFORM (1)[1, 2]



■ READ TIMING WAVEFORM (2)[*2,*3,*5]



■ READ TIMING WAVEFORM (3)[*1, *2, *4, *5]

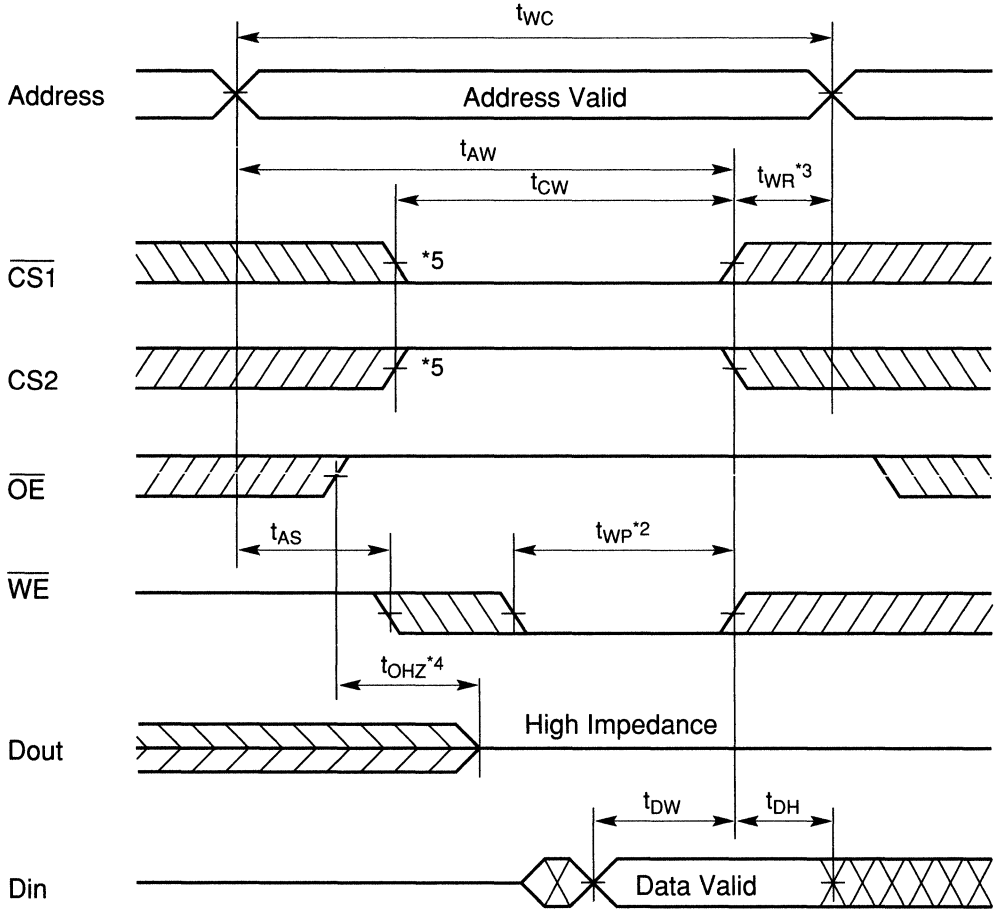


Notes: 1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS_1} = V_{IL}$ and $CS_2 = V_{IH}$.
4. Address valid prior to or coincident with $\overline{CS_1}$ transition low and CS_2 transition high.
5. $\overline{OE} = V_{IL}$.

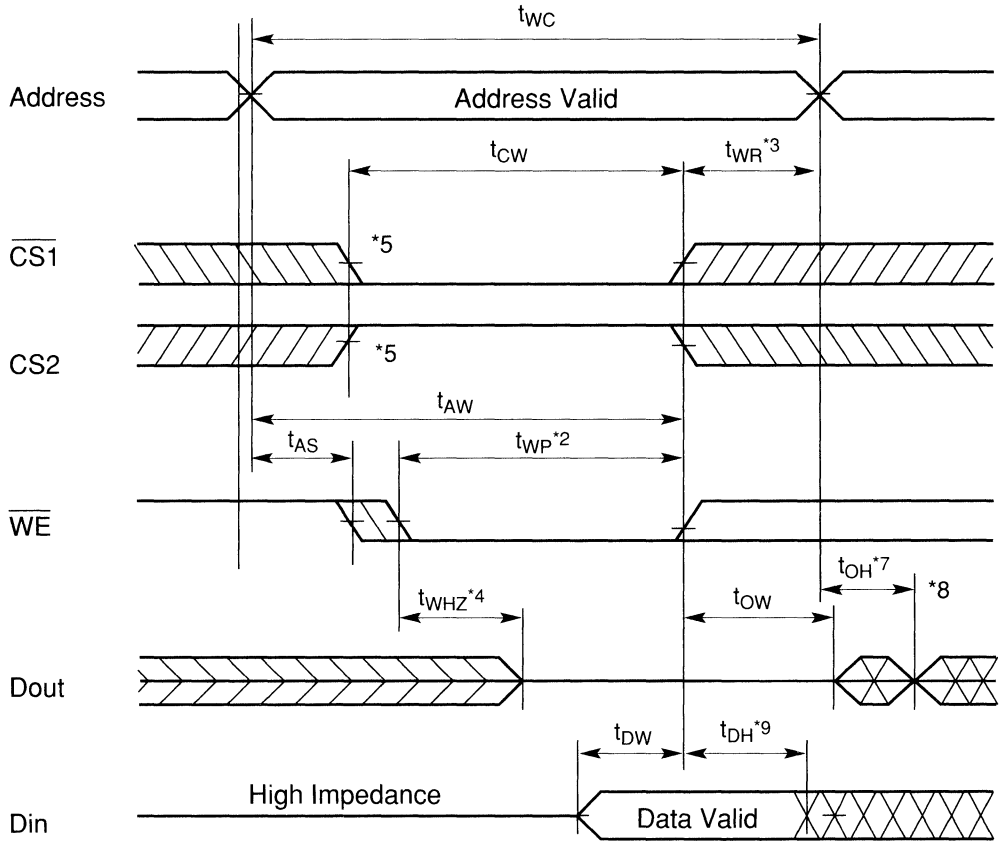
■ WRITE CYCLE

Parameter	Symbol	HM62932-15		HM62932-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15	—	20	—	ns
Chip Selection to End of Write	tCW	10	—	12	—	ns
Address Valid to End of Write	tAW	13	—	15	—	ns
Address Setup Time	tAS	0	—	0	—	ns
Write Pulse Width	tWP	10	—	12	—	ns
Write Recovery Time	tWR	0	—	0	—	ns
Output Disable to Output in High-Z	tOHZ[1]	0	7	0	10	ns
Write to Output in High-Z	tWHZ[1]	0	7	0	10	ns
Data to Write Time Overlap	tDW	8	—	10	—	ns
Data Hold From Write Time	tDH[1]	0	—	0	—	ns
Output Active from End of Write	tOW[1]	3	—	3	—	ns

■ WRITE TIMING WAVEFORM (1)



■ WRITE TIMING WAVEFORM (2)*6



Notes: 1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}_1$, a high CS_2, and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to outputs must not be applied.
5. If the $\overline{CS}_1$ low or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low, ($\overline{OE} = V_{IL}$)
7. Dout is the same phase of write data of this write cycle.
8. Dout is read data of next address.
9. If $\overline{CS}_1$ is low and CS_2 high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. $\overline{WE}$ or $\overline{CS}_1$ must be high during all address transitions except when device is disable with $\overline{CS}_1$ or CS_2.

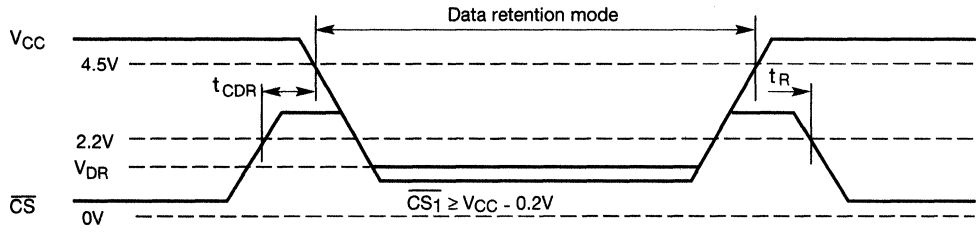
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristic is guaranteed only for L version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	—	—	—	V	$\overline{CS}_1$ V_{CC} –0.2V, V_{in} V_{CC} –0.2V or 0V V_{in} 0.2V
Data Retention Current	I_{CCDR}	—	2	50[1]	µA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0V

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



HM62D932 Series — Preliminary

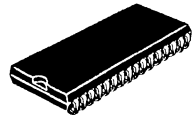
32,768-Word x 9-Bit High Speed CMOS Static Ram with Address Latch

■ FEATURES

- High speed: fast access time 15/20 ns (max.)
- Low Power
  Standby: 15μW (typ.) (L-version)
  Operation: 350mW (typ.)
- Single 5V supply
- Address Latch
- Common data input and output—Three state output
- Directly TTL compatible—All inputs and outputs

■ ORDERING INFORMATION

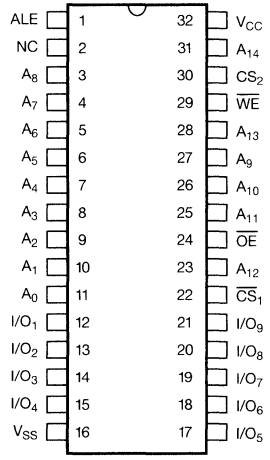
Type No.	Access	Package
HM62D932JP-15	15 ns	300 mil 32 pin Plastic SOJ (CP-32DN)
HM62D932JP-20	20 ns	
HM62D932LJP-15	15 ns	
HM62D932LJP-20	20 ns	



(CP-32DN)

■ PIN ARRANGEMENT

HM62D932 Series

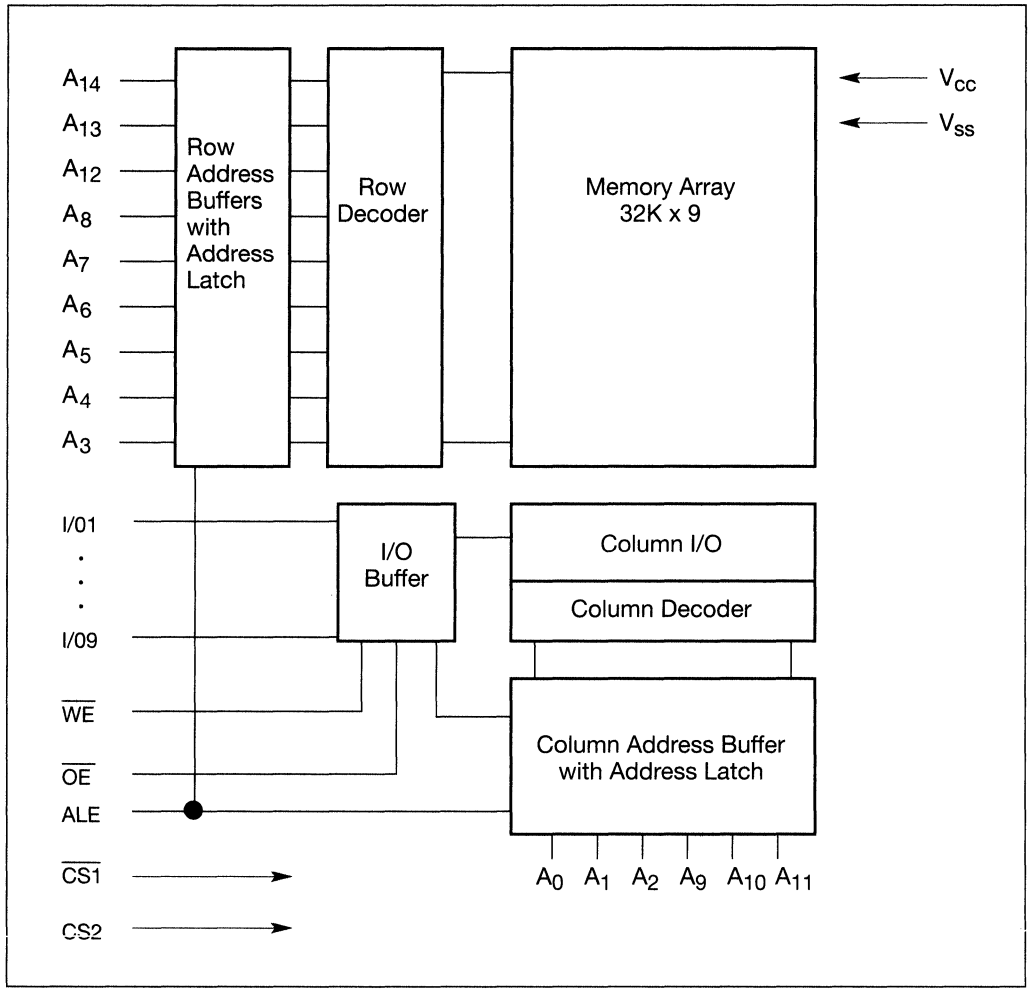


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{14}	Address
ALE	Address Latch Enable
I/O_1–I/O_9	Data Input/Output
$\overline{CS}_1$	Chip Select 1
$\overline{CS}_2$	Chip Select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	L	X	X	Standby	I_{CC}	High-Z	—
L	H	H	H	Output Disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read Cycle 1,2,3
L	H	H	L	Write	I_{CC}	Din	Write Cycle 1
L	H	L	L	Write	I_{CC}	Din	Write Cycle 2

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage 1	V_{CC}	-0.5^{2} + 7.0	V
Voltage on Any Pin Relative to V_{SS}[1]	V_T	-0.5^{2} to V_{CC} + 0.5	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature Under Bias	T_{bias}	–10 to +85	°C

Notes: 1. With respect to V_{SS}
2. V_{CC} and V_T min = –2.5V for pulse width 10ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low (Logic 0) Voltage	V_{IL}	–0.5[1]	—	0.8	V

Note: *1.V_{IL} min = –2.0V for pulse width 10ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS}= 0V)

Item	Symbol	Min.	Typ[1]	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	µA	Output Disable $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC}	—	70	TBD	mA	$\overline{CS}_1$ = V_{IL} I_{out} = 0mA, min. cycle
Standby V_{CC} Current	I_{SB}	—	30	TBD	mA	$\overline{CS}_1$ = V_{IH}, min. cycle
Standby V_{CC} Current (1)	I_{SB1} (L-version)	—	0.02	2.0	mA	2
		—	0.003	0.1		
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

Not 1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
2. $\overline{CS}_1$ V_{CC} –0.2V, 0V V_{in} 0.2V or V_{CC} –0.2V V_{in}.

■ CAPACITANCE (T_a = 25°C, f = 1.0 MHz)[1]

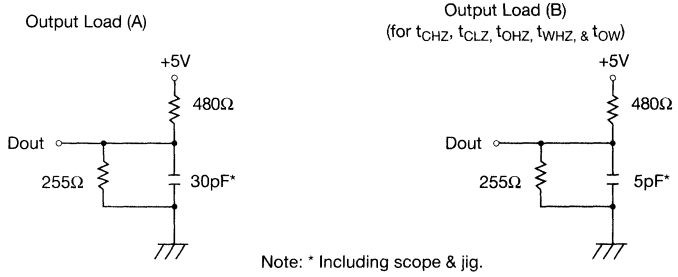
Item	Symbol	Min	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0V
Output Capacitance	C_{out}	—	—	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} 5V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 4ns
- Input and Output timing reference levels: 1.5V
- Output load: See figures

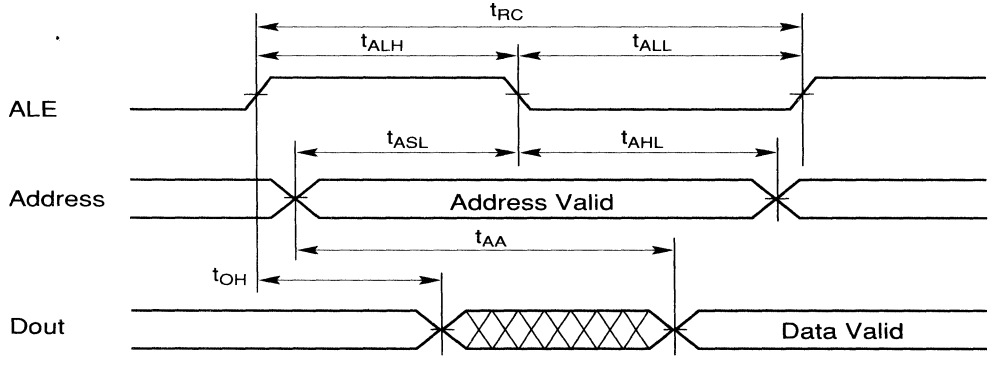


Note: * Including scope & jig.

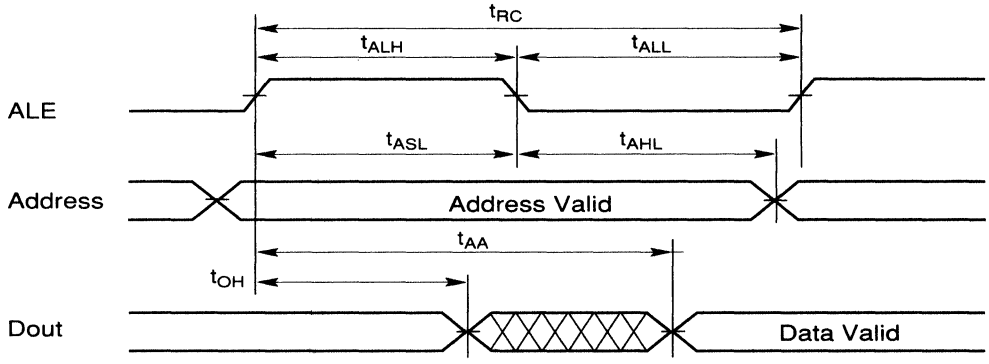
■ READ CYCLE

Item	Symbol	HM62D932-15		HM62D932-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	—	20	—	ns
Address Access Time	t_{AA}	—	15	—	20	ns
Chip Select Access Time	t_{CO4}	—	15	—	20	ns
	t_{CO2}	—	7	—	10	ns
Chip Selection to Output in Low-Z	t_{CLZ1}[4]	3	—	3	—	ns
	t_{CLZ2}[4]	0	—	0	—	ns
Output Enable to Output Valid	t_{OE}	—	7	—	10	ns
Output Enable to Output in Low-Z	t_{OLZ}[4]	0	—	0	—	ns
Chip deselection to Output in High-Z	t_{CHZ1}, t_{CHZ2}[4]	0	7	0	10	ns
Chip Disable to Output in High-Z	t_{OHZ}[4]	0	7	0	10	ns
Output Hold from Address Change	t_{OH}	3	—	3	—	ns
Address Latch Enable High Time	t_{ALH}	5	—	6	—	ns
Address Latch Enable Low time	t_{ALL}	5		6	—	ns
Address Setup to Latch Low	t_{ASL}	3	—	4	—	ns
Address Hold to Latch Low	t_{AHL}	3	—	4	—	ns

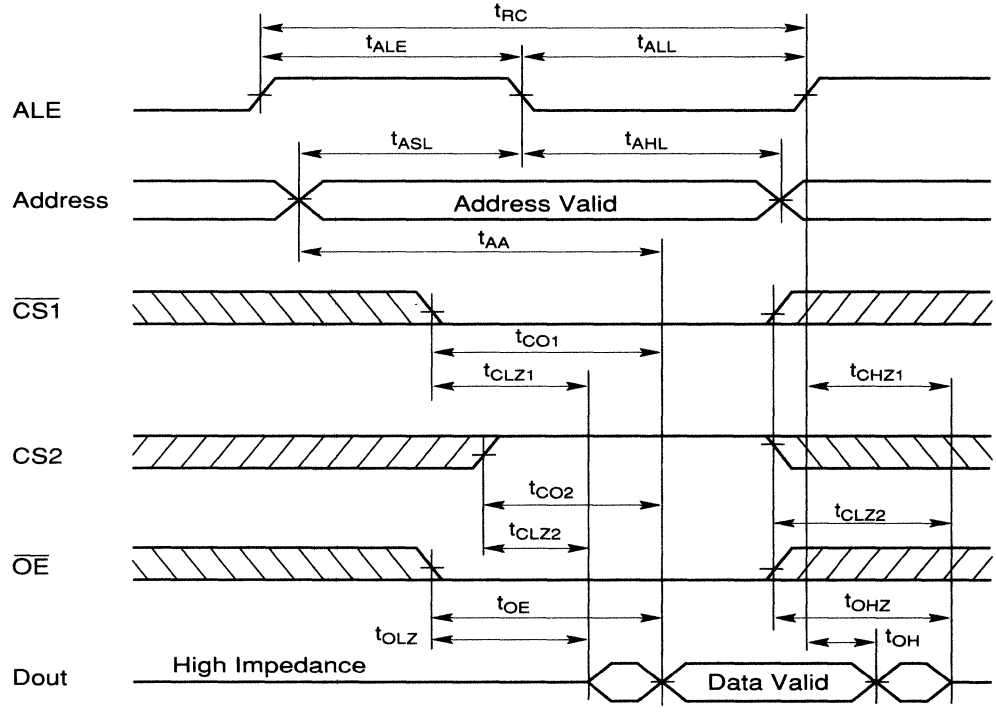
■ READ TIMING WAVEFORM (1)[1, 2, 3]



■ READ TIMING WAVEFORM (2)[1, 2, 3]



■ READ TIMING WAVEFORM (3)[1, 2, 4,]

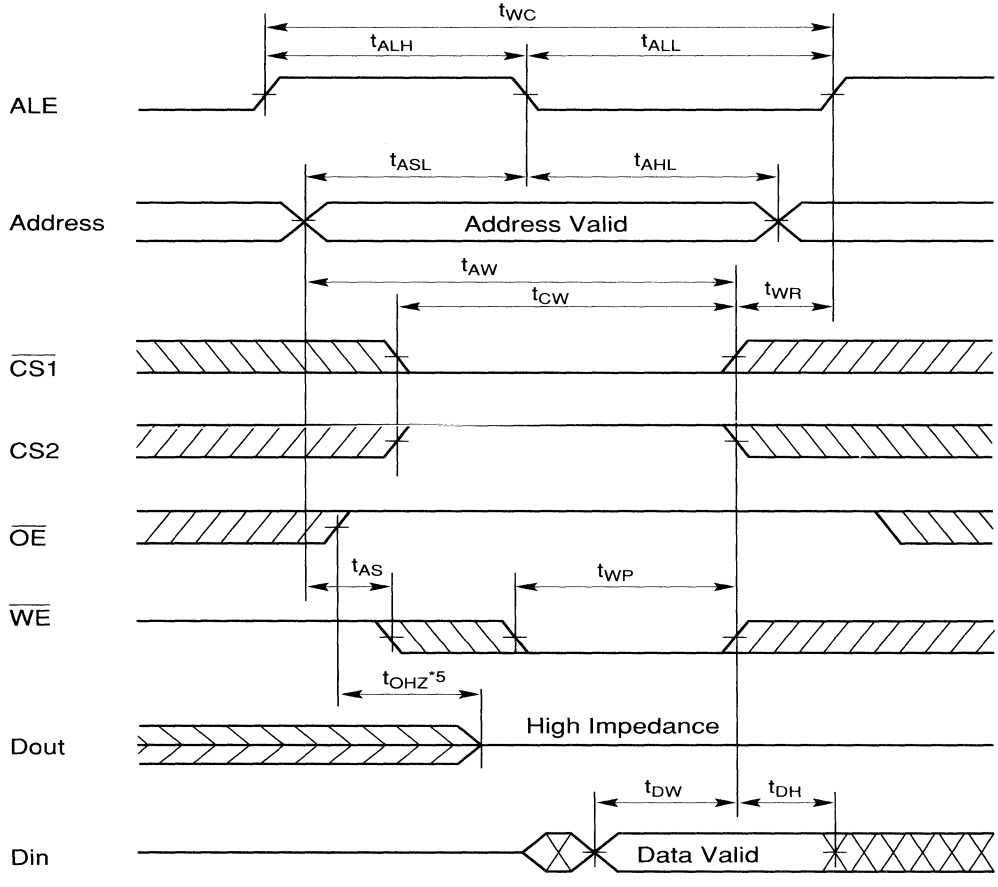


Notes: 1. Address inputs are latched on the falling edge of ALE. When ALE is high, the latch is transparent.
2. $\overline{WE}$ is high for read cycle.
3. $\overline{CS_1}$ = V_{IL}, CS2 = V_{IH}, and $\overline{OE}$ = V_{IL}.
4. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

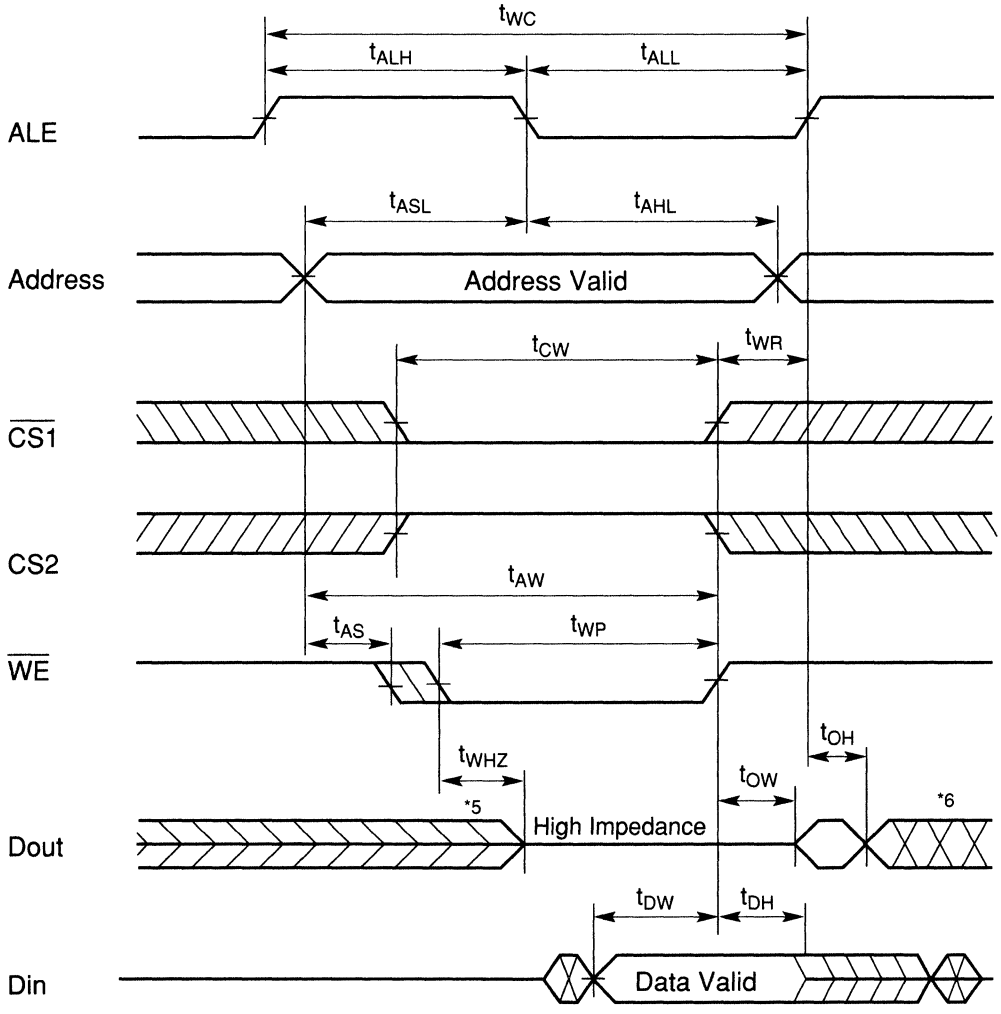
■ WRITE CYCLE

Parameter	Symbol	HM62D932-15		HM62D932-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15	—	20	—	ns
Chip Selection to End of Write	t_{CW}	10	—	12	—	ns
Address Valid to End of Write	t_{AW}	13	—	15	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	10	—	12	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}[4]	0	7	0	10	ns
Write to Output in High-Z	t_{WHZ}[4]	0	7	0	10	ns
Data to Write Time Overlap	t_{DW}	8	—	10	—	ns
Data Hold From Write Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write	t_{OW}[4]	3	—	3	—	ns
Address Latch Enable High Time	t_{ALH}	5	—	6	—	ns
Address Latch Enable Low Time	t_{ALL}	5	—	6	—	ns
Address Setup to Latch low	t_{ASL}	3	—	4	—	ns
Address Hold to Latch Low	t_{AHL}	3	—	4	—	ns

■ WRITE TIMING WAVEFORM (1)[1, 2, 3, 4]



■ WRITE TIMING WAVEFORM (2)[1, 2, 3, 4]



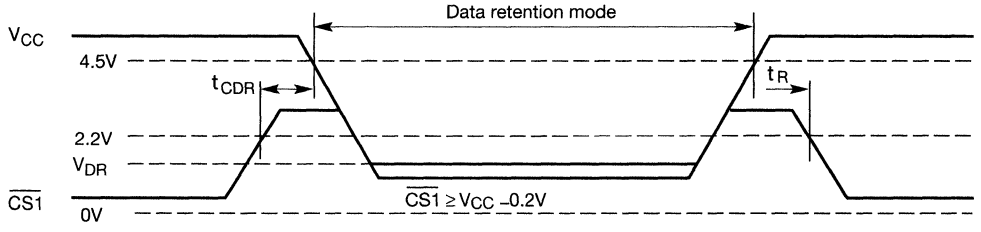
Notes:
1. Address inputs are latched on the falling edge of ALE. When ALE is high, the latch is transparent.
2. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled not 100% tested.
3. a write occurs during the overlap (tWP) of a low $\overline{CS_1}$, a high CS_2, and a low $\overline{WE}$.
4. If the $\overline{CS_1}$ low and CS_2 high transition occurs simultaneously with $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristic is guaranteed only for L–version.

Item	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	20	—	—	V	$\overline{CS_1}$ V_{CC} –0.2V, V_{in} V_{CC} –0.2V or 0V V_{in} 0.2V
Data Retention Current	I_{CCDR}	—	2	50*1	µA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0V.



HM628128/HM628128I Series

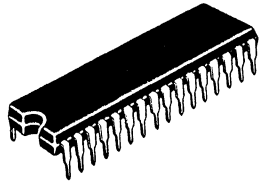
131,072-Word × 8-Bit High Speed Hi-CMOS Static RAM

■ DESCRIPTION

The Hitachi HM628128 is a CMOS static RAM organized 128k-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology. The HM628128I is available in industrial temperature range (–40 to +85°C).

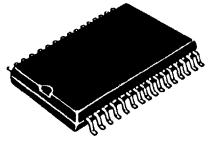
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 8 × 20 mm TSOP with a thickness of 1.2 mm, 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, is available for high density mounting.

HM628128P Series



(DP-32)

HM628128FP Series



(FP-32D)

(TFP-32DA)

■ FEATURES

- High Speed: Fast access time .....70/85/100/120ns (max.)
- Low Power
  - Standby: .....10 μW (typ.) (L-version)
  - Operation: .....75 mW (typ.)
- Single 5V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L & SL)
  - 2 chip selection for battery back up.

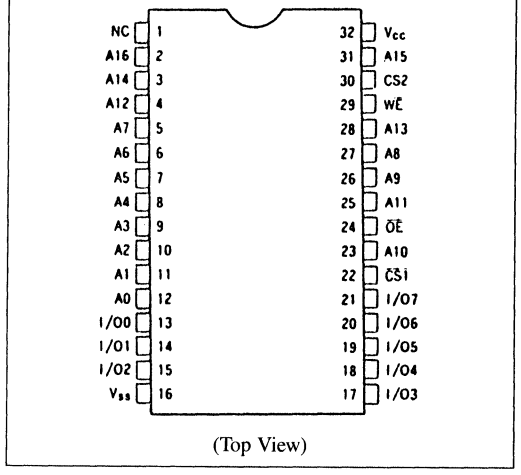
Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
Vcc	Power supply
Vss	Ground

2

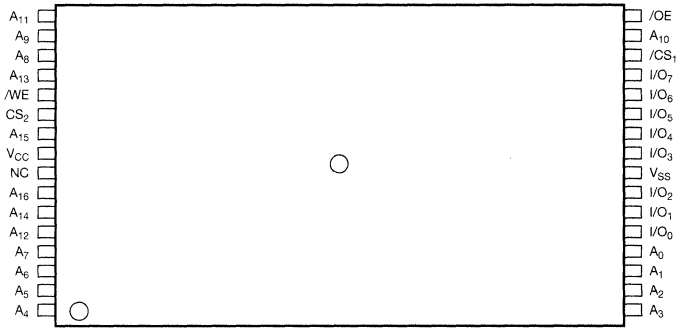
■ PIN ARRANGEMENT

(DP-32 & FP-32D)



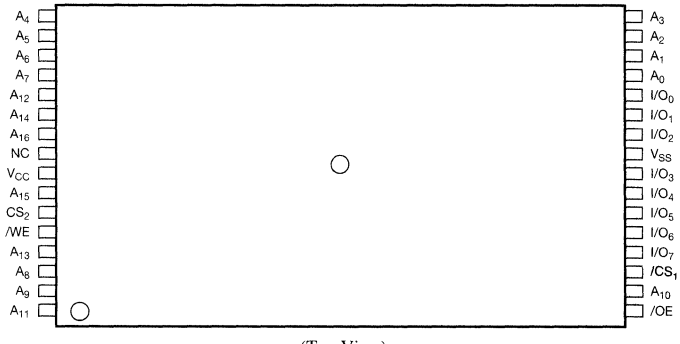
(Top View)

(TFP-32DA)



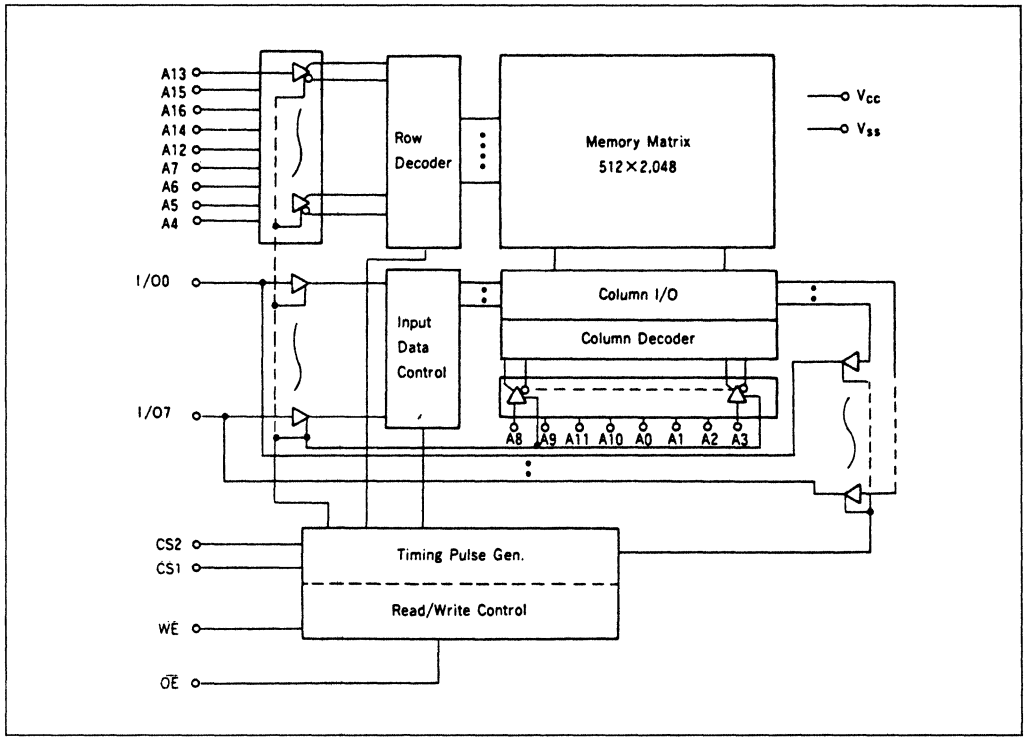
(Top View)

(TFP-32DAR)



(Top View)

Block Diagram



■ ORDERING INFORMATION

Part No.	Access	Package	Part No.	Access	Package
HM628128P-7	70ns	600 mil 32 pin Plastic DIP (DP-32)	HM628128LP-7SL	70ns	600 mil 32 pin Plastic DIP (DP-32)
HM628128P-8	85ns		HM628128LP-8SL	85ns	
HM628128P-10	100ns		HM628128LP-10SL	100ns	
HM628128P-12	120ns		HM628128LP-12SL	120ns	
HM628128LP-7	70ns				
HM628128LP-8	85ns				
HM628128LP-10	100ns				
HM628128LP-12	120ns				
HM628128FP-7	70ns	525 mil 32 pin Plastic SOP (FP-32D)	HM628128LFP-7SL	70ns	525 mil 32 pin Plastic SOP (FP-32D)
HM628128FP-8	85ns		HM628128LFP-8SL	85ns	
HM628128FP-10	100ns		HM628128LFP-10SL	100ns	
HM628128FP-12	120ns		HM628128LFP-12SL	120ns	
HM628128LFP-7	70ns				
HM628128LFP-8	85ns				
HM628128LFP-10	100ns				
HM628128LFP-12	120ns				

• TSOP SERIES

Type No.	Access Time	Package
HM628128T-7	70 ns	8mm×20mm 32-Pin TSOP (Normal Type) (TFP-32DA)
HM628128T-8	85 ns	
HM628128T-10	100 ns	
HM628128T-12	120 ns	
HM628128LT-7	70 ns	
HM628128LT-8	85 ns	
HM628128LT-10	100 ns	
HM628128LT-12	120 ns	
HM628128LT-7L	70 ns	
HM628128LT-8L	85 ns	
HM628128LT-10L	100 ns	
HM628128LT-12L	120 ns	
HM628128R-7	70 ns	8mm×20mm 32-Pin TSOP (Reverse Type) (TFP-32DAR)
HM628128R-8	85 ns	
HM628128R-10	100 ns	
HM628128R-12	120 ns	
HM628128LR-7	70 ns	
HM628128LR-8	85 ns	
HM628128LR-10	100 ns	
HM628128LR-12	120 ns	
HM628128LR-7L	70 ns	
HM628128LR-8L	85 ns	
HM628128LR-10L	100 ns	
HM628128LR-12L	120 ns	

• INDUSTRIAL TEMPERATURE SERIES

Type No.	Access Time	Package
HM628128PI-8	85 ns	600-mil 32-Pin Plastic DIP (DP-32)
HM628128PI-10	100 ns	
HM628128PI-12	120 ns	
HM628128LPI-8	85 ns	
HM628128LPI-10	100 ns	
HM628128LPI-12	120 ns	
HM628128FPI-8	85 ns	525-mil 32-Pin Plastic SOP (FP-32)
HM628128FPI-10	100 ns	
HM628128FPI-12	120 ns	
HM628128LFPI-8	85 ns	
HM628128LFPI-10	100 ns	
HM628128LFPI-12	120 ns	

Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
×	H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	
×	×	L	×		I_{SB}, I_{SB1}	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature (HM628128 Series)	T_{opr}	0 to +70	°C
Operating temperature (HM628128I Series)	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias (HM628128 Series)	T_{bias}	−10 to +85	°C
Storage temperature under bias (HM628128I Series)	T_{bias}	−40 to +85	°C

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions

(Ta=0 to +70°C, for HM628128 Series, Ta=−40° to +85°C for HM628128I Series)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V	
Input low (logic 0) voltage	V_{IL}	−0.3*1	—	0.8	V	

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

DC Characteristics

(Ta=0 to +70°C, for HM628128 Series, Ta=−40° to +85°C for HM628128I Series, V_{CC}=5 V ± 10%, V_{SS}=0 V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	μA	Vin=V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS1}$=V_{IH} or CS2=V_{IL}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}
Operating power supply current: DC	I_{CC}	—	15	35 (45)	mA	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, others=V_{IH}/V_{IL}, $I_{I/O}$=0 mA (HM628128I Series)
Operating Power supply current	I_{CC1}	—	45	70 (80)	mA	Min. cycle, duty=100%, $\overline{CS1}$=V_{IL}, CS2=V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$=0 mA (HM628128I Series)
	I_{CC2}	—	15	30 (40)	mA	Cycle time = 1μs, duty = 100%, $I_{I/O}$=0 mA, CS1≤0.2V, CS2≥ V_{CC} −0.2V, V_{IH}≥V_{CC}−0.2V, V_{IL}≤0.2V (HM628128I Series)
Standby V_{CC} current: DC	I_{SB}	—	1	3	mA	$\overline{CS1}$=V_{IH}, CS2=V_{IH} or CS2=V_{IL}
Standby V_{CC} current (1): DC	I_{SB1}	—	0.02	2	mA	Vin≥ 0 V, CS1≥ V_{CC} −0.2V, CS2≥ V_{CC} −0.2V or 0 V≤ CS2≤ 0.2 V
		—	2*2	100*2	μA	
		—	2*3	50*3		
Output low voltage	V_{OL}	—	—	0.4	0	I_{OL}=2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH}= −1.0 mA

Note: 1. Typical values are at V_{CC}=5.0V, Ta=+25°C and specified loading.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for SL-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	CI/O	—	—	10	pF	VI/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta=0 to +70°C, for HM628128 Series, Ta=–40 to +85°C for HM628128I Series, V_{CC}=5 V ± 10%, unless otherwise noted)

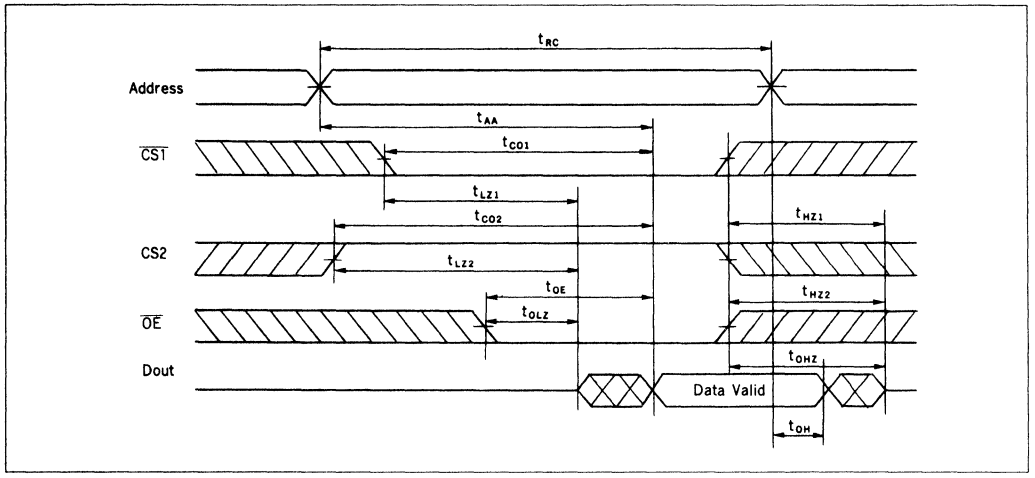
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V for HM628128 Series
  0.5 V to 2.5 V for HM628128I Series
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5V
- Output load: 1 TTL Gate and CL (100pF) (Including scope & jig)

Read Cycle

Item	Symbol	HM628128-7		HM628128I-8 HM628128-8		HM628128I-10 HM628128-10		HM628128I-12 HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	tRC	70	—	85	—	100	—	120	—	ns	
Address access time	tAA	—	70	—	85	—	100	—	120	ns	
Chip selection ($\overline{CS1}$) to output valid	tCO1	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	tCO2	—	70	—	85	—	100	—	120	ns	
Output enable ($\overline{OE}$) to output valid	tOE	—	35	—	45	—	50	—	60	ns	
Chip selection ($\overline{CS1}$) to output in low-Z	tLZ1	10	—	10	—	10	—	10	—	ns	*1, *2,
Chip selection (CS2) to output in low-Z	tLZ2	10	—	10	—	10	—	10	—	ns	*1, *2,
Output enable ($\overline{OE}$) to output in low-Z	tOLZ	5	—	5	—	5	—	5	—	ns	*1, *2,
Chip deselection ($\overline{CS1}$) to output in high-Z	tHZ1	0	25	0	30	0	35	0	45	ns	*1, *2,
Chip deselection (CS2) to output in high-Z	tHZ2	0	25	0	30	0	35	0	45	ns	*1, *2,
Output disable ($\overline{OE}$) to output in high-Z	tOHZ	0	25	0	30	0	35	0	45	ns	*1, *2,
Output hold from address change	tOH	10	—	10	—	10	—	10	—	ns	

Read Cycle Timing

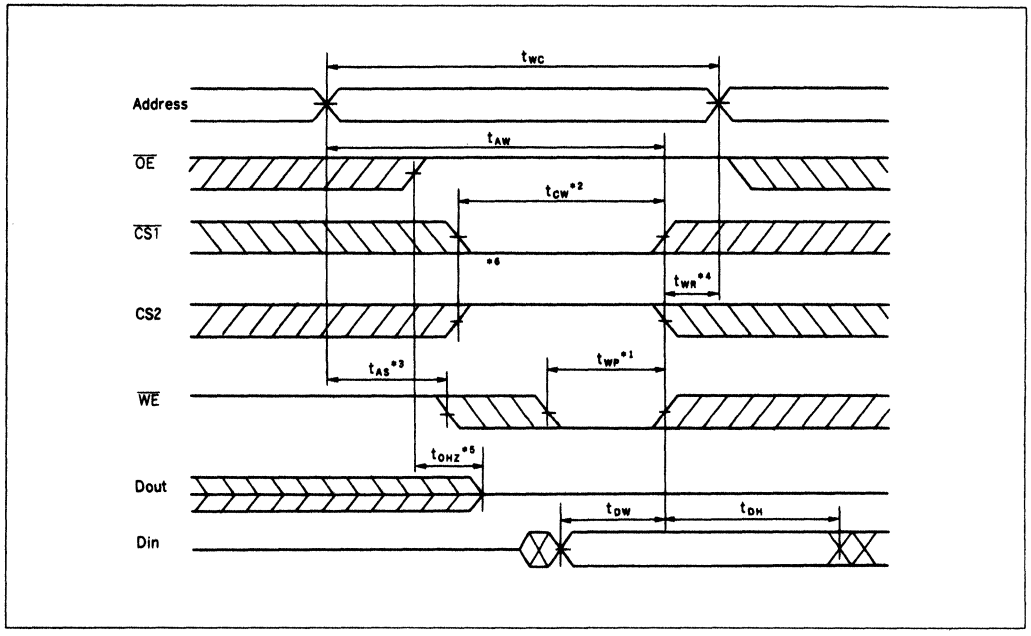


Notes: *1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
*2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
*3. $\overline{WE}$ is high for read cycle.

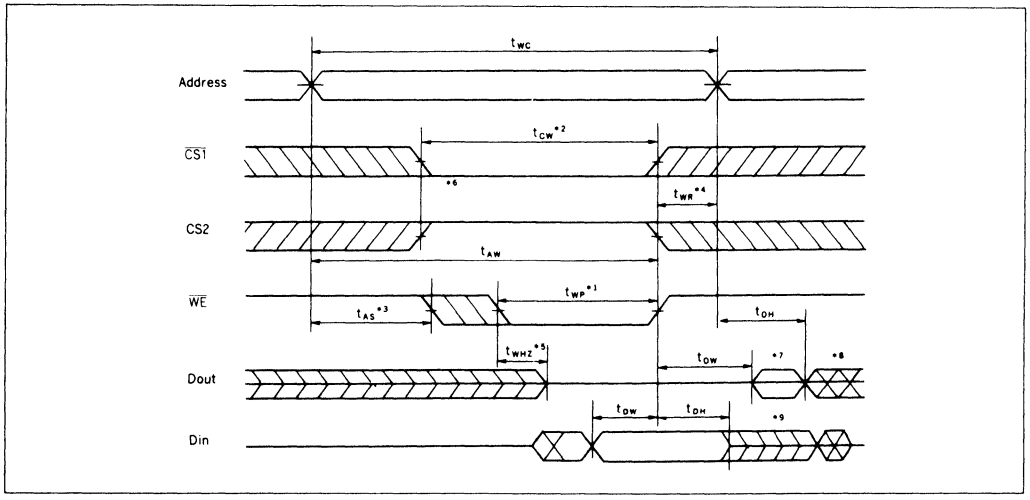
Write Cycle

Parameter	Symbol	HM628128-7		HM628128I-8 HM628128-8		HM628128I-10 HM628128-10		HM628128I-12 HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	80	—	85	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	t_{AW}	60	—	75	—	80	—	85	—	ns	
Write pulse width	t_{WP}	50	—	55	—	60	—	70	—	ns	
Write recovery time	t_{WR}	5	—	5 (10)	—	5 (10)	—	10 (15)	—	ns	*12
		10	—	10 (15)	—	10 (15)	—	15 (15)	—	ns	*11 *12
Write to output in high-Z	t_{WHZ}	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	t_{DW}	30	—	35	—	40	—	45	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	*10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fix)



Notes: *1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

*6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

*7. Dout is the same phase of the latest written data in this write cycle.

*8. Dout is the read data of next address.

*9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

*10. This parameter is sampled and not 100% tested.

*11. This value is measured from CS2 going low to the end of write cycle.

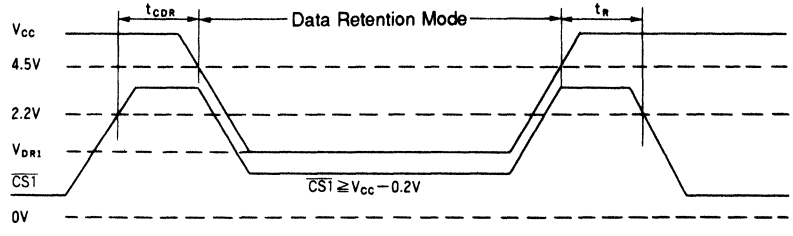
*12. Parenthesis denote specification for HM6281281 Series only.

Low V_{CC} Data Retention Characteristics (Ta=0 to +70°C) for HM628128 Series, Ta=-40 to +85°C for HM628128I Series.

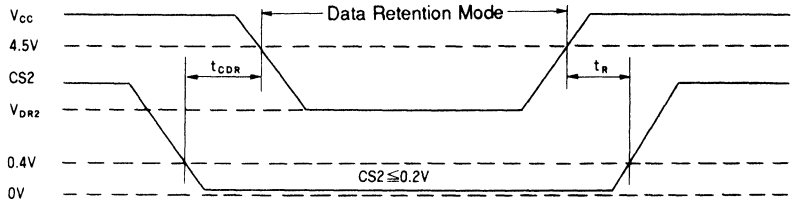
(This characteristics is guaranteed only for L & SL version.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions*2
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC}$ -0.2 V, CS2 ≥ V_{CC} -0.2 V or 0 V ≤ CS2 ≤ 0.2 V Vin ≥ 0 V
Data retention current	I_{CCDR}			50*13	μA	V_{CC}=3.0 V, Vin ≥ OV $\overline{CS1} \geq V_{CC}$ -0.2 V, CS2 ≥ V_{CC} -0.2 V or 0 V ≤ CS2 ≤ 2.0V
				15*14		
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation recovery time	t_R	5*15	—	—	ms	

Low Vcc Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)



Note: 13. *1: for L-version and 20 uA max. at Ta=0 to 40°C
*2: for SL-version and 3uA max. at Ta=0 to 40°C.

14. CS2 controls address buffer, WE buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 $\geq V_{CC}$ -0.2V or 0V $\leq$ CS2 $\leq$ 0.2V. The other input levels (address, $\overline{WE}$ $\overline{OE}$, I/O) can be in the high impedance state.

15. V_{CC} rise time must be more than 50ms when V_{CC} rise time is less than 50ms, t_R must be 50ms or more.

2

HM66204 Series

131072-word × 8-bit High Density CMOS Static RAM Module

The HM66204 module was designed for pinout and signal compatibility with the HM628128 128K × 8 Monolithic Device.

This device is now obsolete and no longer in manufacture.

New designs should be based on the HM628128 Monolithic Device.

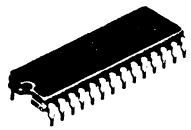
HM624256A Series — Preliminary

262,144-Word x 4-Bit High Speed CMOS Static RAM

■ DESCRIPTION

The Hitachi HM624256A is a high speed 1M Static RAM organized as 256-kword x 4-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624256A, packaged in a 400 mil plastic SOJ is available for high density mounting.



(DP-28C)

(CP-28D)

■ FEATURES

- Single 5V supply and high density 28-pin package (DIP and SOJ)
- High speed
  Access time: 20/25/35 ns (maximum)
- Low power dissipation
  Active mode 350 mW (typical)
  Standby mode 100 µW (typical)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  All inputs and outputs

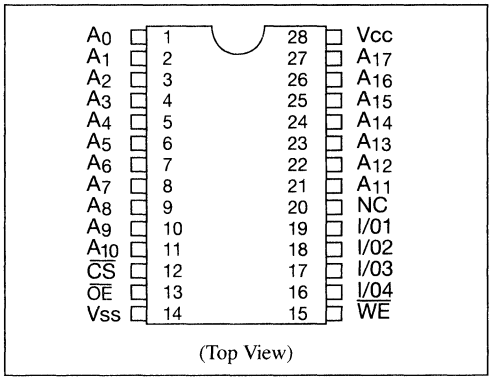
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624256AP-20	20 ns	400-mil 28-Pin Plastic DIP (DP-28C)
HM624256AP-25	25 ns	
HM624256AP-35	35 ns	
HM624256ALP-20	20 ns	
HM624256ALP-25	25 ns	
HM624256ALP-35	35 ns	
HM624256AJP-20	20 ns	400-mil 28-Pin PlasticSOJ (CP-28D)
HM624256AJP-25	25 ns	
HM624256AJP-35	35 ns	
HM624256ALJP-20	20 ns	
HM624256ALJP-25	25 ns	
HM624256ALJP-35	35 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{17}	Address
I/O_0-I/O_4	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

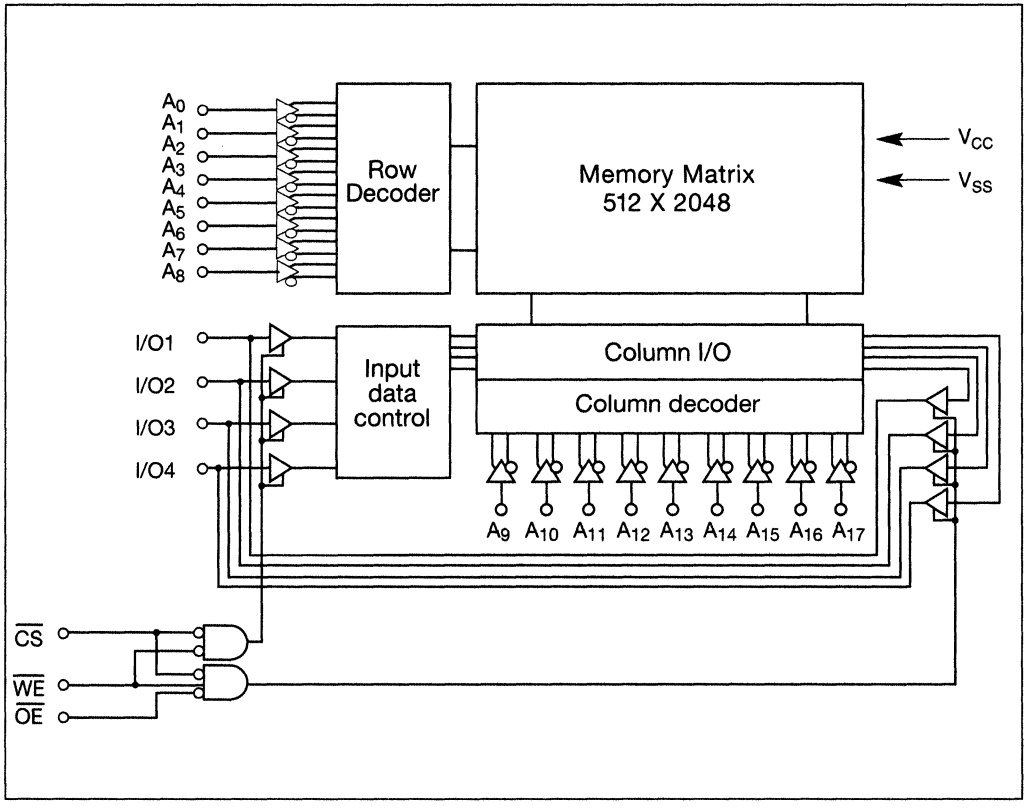
■ PIN ARRANGEMENT (DIP and SOJ)



(Top View)

2

■ BLOCK DIAGRAM



■ FUNCTION TABLE

CS	$\overline{OE}$	WE	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle (1–3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle (1)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (2)

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{in}	−0.5[*1] to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_{in} min = −2.0 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATION CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	–0.5*1	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM624256A-20			HM624256A-25/35			Unit	Test Conditions
		Min.	Typ*1	Max.	Min	Typ*1	Max		
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = Max V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min Cycle
Standby Power Supply Current	I_{SB}	—	—	60	—	—	40	mA	$\overline{CS}$ = V_{IH}, Min Cycle
Standby Power Supply Current (1)	I_{SB1}*2 I_{SB1}*3	— —	0.02 —	2.0 100	— —	0.2 —	2.0 100	mA µA	$\overline{CS}$ ≥ V_{CC} –0.2V, 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} –0.2V
Output Low Voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} =–4 mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.
2. P and JP version.
3. LP and LJP version.

■ CAPACITANCE (T_a = 25°C, f= 1 MHz.)

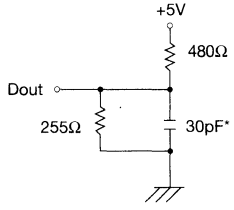
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

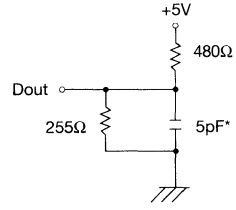
■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0V to 3.0V
- Input rise and fall times: 4 ns
- Input timing reference levels: 1.5V
- Output timing reference levels: 1.5V
- Output load: See figures



Output Load (A)
*Including scope & jig.

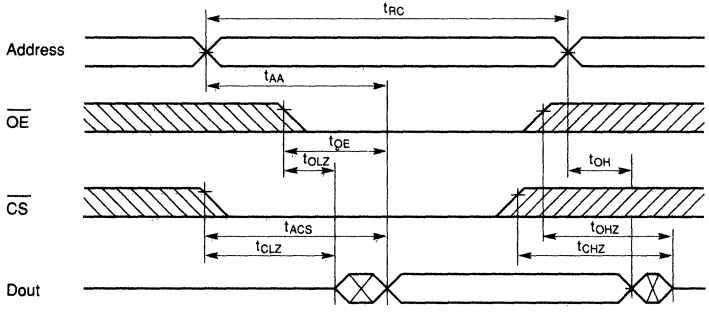


Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})

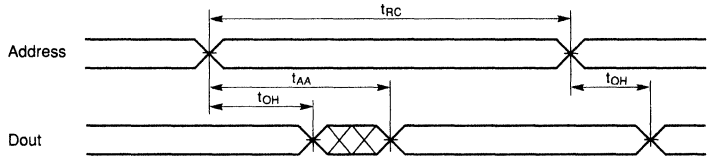
■ READ CYCLE

Parameter	Symbol	HM624256A-20		HM624256A-25		HM624256A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20	—	25	—	35	—	ns
Address Access Time	t_{AA}	—	20	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	20	—	25	—	35	ns
Chip Selection to Output in Low-Z	t_{CLZ}*1	5	—	5	—	5	—	ns
Output Enable to Output Valid	t_{OE}	—	10	—	12	—	15	ns
Output Enable to Output in Low-Z	t_{OLZ}*1	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}*1	0	10	0	12	0	15	ns
Chip Disable to Output in High-Z	t_{OHZ}*1	0	10	0	10	0	10	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Deselection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	12	—	15	—	25	ns

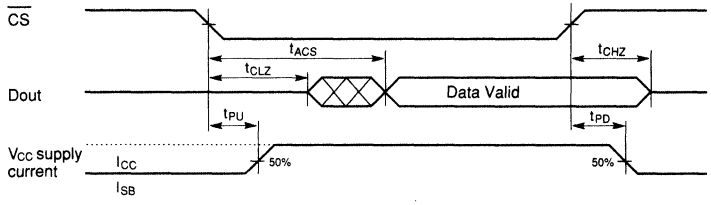
■ READ TIMING WAVEFORM (1) *1, *2



■ READ TIMING WAVEFORM (2) *2, *3, *5



■ READ TIMING WAVEFORM (3) *1, *2, *4, *5

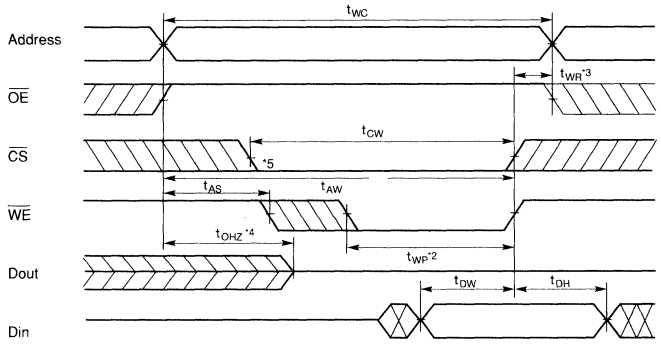


Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE} = V_{IL}$.

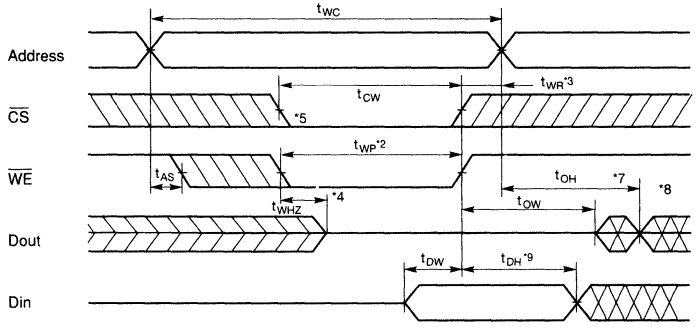
■ WRITE CYCLE

Parameter	Symbol	HM624256A-20		HM624256A-25		HM624256A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20	—	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	14	—	17	—	25	—	ns
Address Valid to End of Write	t_{AW}	16	—	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	14	—	17	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Output Disable to Output in High-Z*1	t_{OHZ}	0	10	0	10	0	10	ns
Write to Output in High-Z*1	t_{WHZ}	0	13	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write*1	t_{OW}	0	—	0	—	0	—	ns

■ WRITE TIMING WAVEFORM (1)



■ WRITE TIMING WAVEFORM (2)*6



Notes:
1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is a continuously low ($\overline{OE} = V_{IL}$).
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS}$ is low during the period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

2

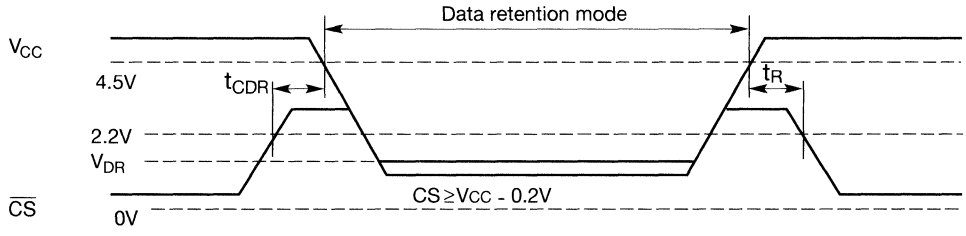
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

This characteristic is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
VCC for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq VCC - 0.2V$, $Vin \geq VCC - 0.2V$ or $0V \leq Vin \leq 0.2V$
Data Retention Current	I_{CCDR}	—	2	100*1	µA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0V

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



262144-WORD × 4-BIT HIGH SPEED CMOS STATIC RAM

The Hitachi HM624257 is a high speed 1M static RAM organized as 256-kword × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624257, packaged in a 400-mil plastic SOJ is available for high density mounting.

(CP-32D)

■ FEATURES

- Single 5 V supply and high density 32-pin package (SOJ)
- High speed: Access time 35/45 ns (max.)
- Low power dissipation
  Active mode: 350 mW (typ.)
  Standby: 100 μW (typ.)
- Completely static memory:
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

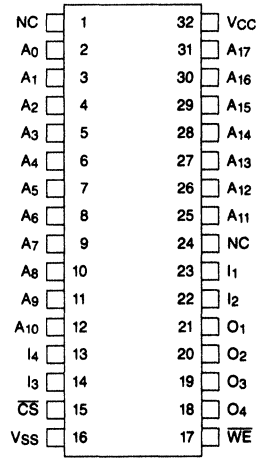
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624257JP-35	35 ns	400 mil 32-pin Plastic SOJ (CP-32D)
HM624257JP-45	45 ns	
HM624257LJP-35	35 ns	
HM624257LJP-45	45 ns	

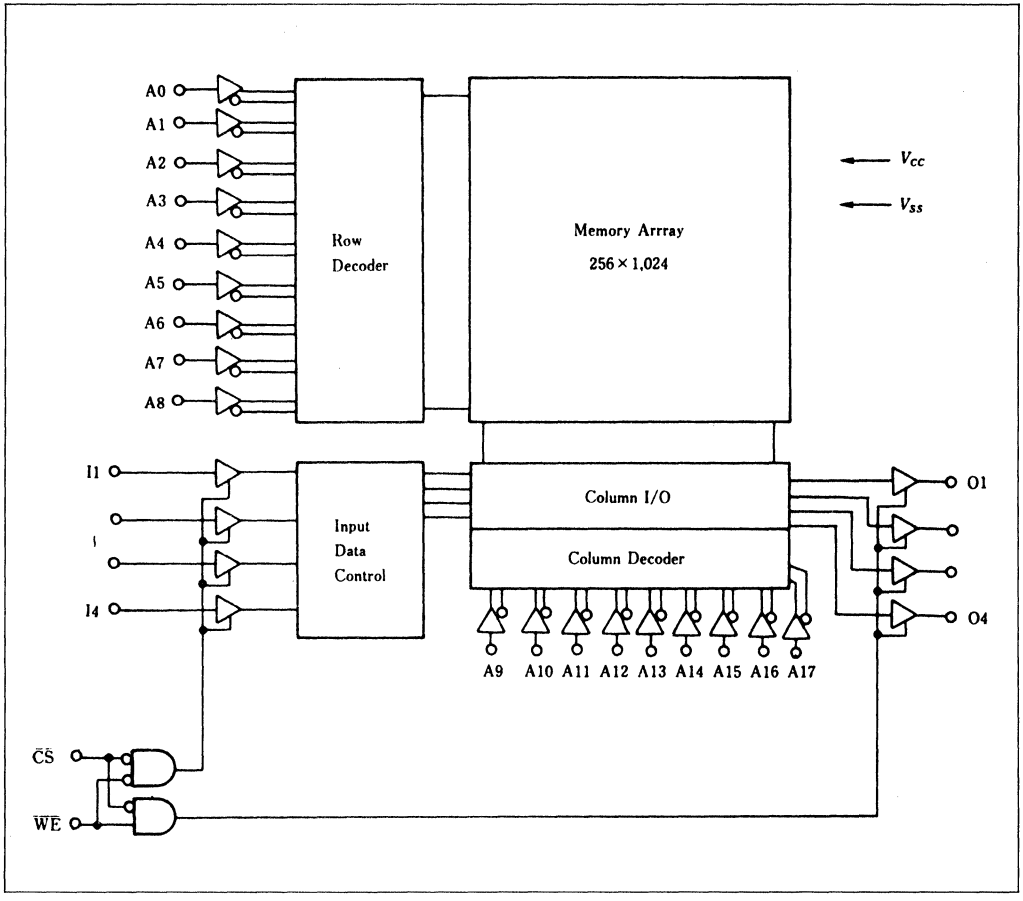
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{17}	Address
I_1–I_4	Data Input
I_1–O_4	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

PIN ARRANGEMENT
Top View



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{in}	-0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: *1. V_{in} min. ≈ -2.0 V for pulse width ≤ 10 ns.

■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle(1)-(2)
L	L	Write	I_{CC}	High-Z	Write Cycle(1)-(2)

NOTE: X : H or L

2

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5*1	—	0.8	V

NOTE: *1. V_{IL} min. = -2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min. cycle
Standby Power Supply Current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

NOTE: 1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

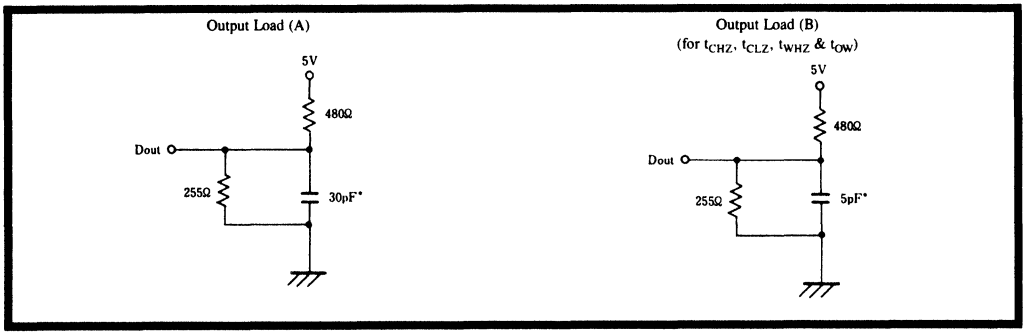
Item	Symbol	Min.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0 V
Output Capacitance	C_{out}	—	11	pF	V_{out} = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures



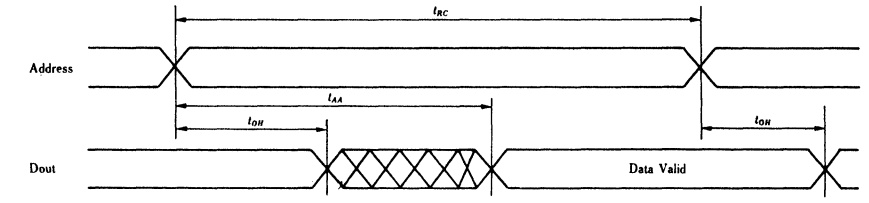
NOTE: *Including scope & jig.

■ Read Cycle

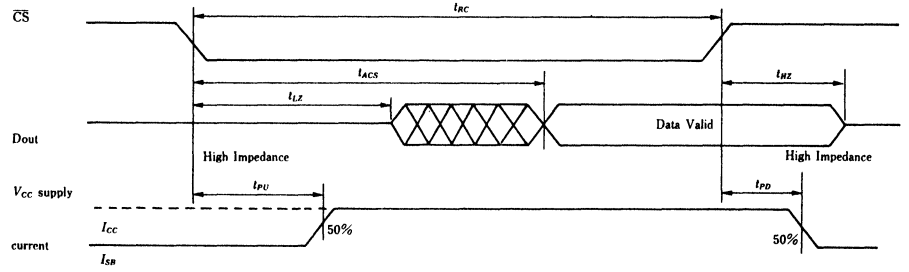
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—		—	30	ns

NOTE: 1. Transition is measured ±200 mV from steady voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



NOTES: *1. $\overline{WE}$ is high for read cycle.

*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

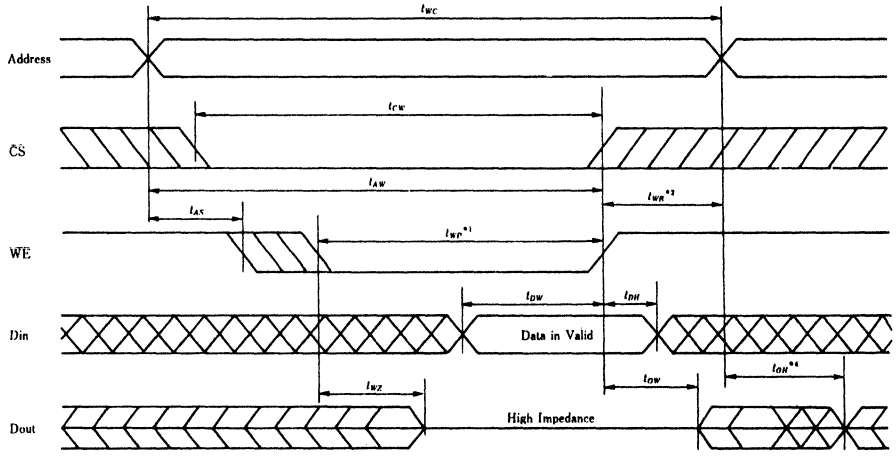
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ Write Cycle

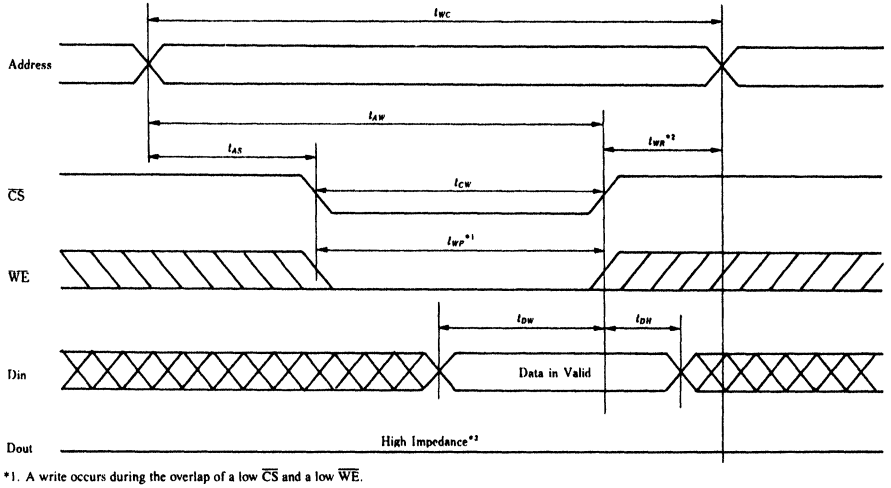
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	20	—		—	ns
Data Hold Time	t_{DH}	3	—	3	—	ns
Write Enabled to Output in High-Z	t_{WZ}*1	0	15	0	20	ns
Output Active From End of Write	t_{OW}*1	5	—	5	—	ns

NOTE: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



NOTES: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output buffers remain in a high impedance state.

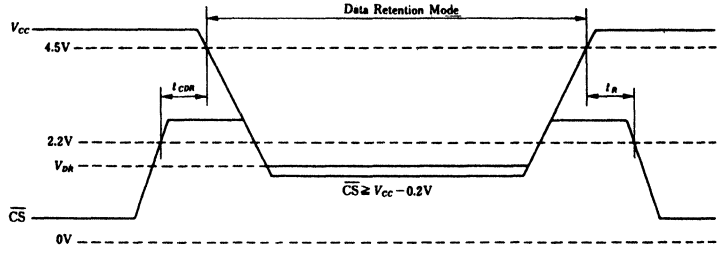
*4. D_{OUT} is the same phase of write data of this write cycle.

■ Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or $0 V \leq V_{in} \leq 0.2$ V
Data Retention Current	I_{CCDR}	—	2	100*1	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

NOTE: *1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform



HM621100A Series

Preliminary

1,048,576-Word x 1-Bit High Speed CMOS Static Ram

■ DESCRIPTION

The HM621100A is a high speed 1M Static RAM organized as 1,048,576-word x 1-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

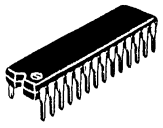
The HM621100A, packaged in a 400 mil plastic SOJ is available for high density mounting.

■ FEATURES

- Single 5V supply and high density 28-pin package (DIP and SOJ)
- High speed
  Access time 20 ns/25 ns/35 ns (maximum)
- Low power dissipation
  Active mode 350 mW (typical)
  Standby mode 100µW (typical)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  All inputs and outputs

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM621100AP-20	20 ns	400-mil 28-pin plastic DIP (DP-28C)
HM621100AP-25	25 ns	
HM621100AP-35	35 ns	
HM621100ALP-20	20 ns	
HM621100ALP-25	25 ns	
HM621100ALP-35	35 ns	
HM621100AJP-20	20 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM621100AJP-25	25 ns	
HM621100AJP-35	35 ns	
HM621100ALJP-20	20 ns	
HM621100ALJP-25	25 ns	
HM621100ALJP-35	35 ns	

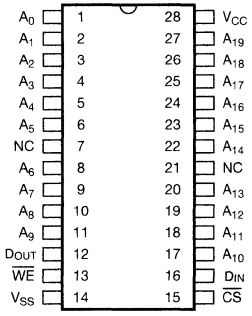


(DP-28C)

(CP-28D)

■ PIN ARRANGEMENT

HM621100A Series (DIP and SOJ)



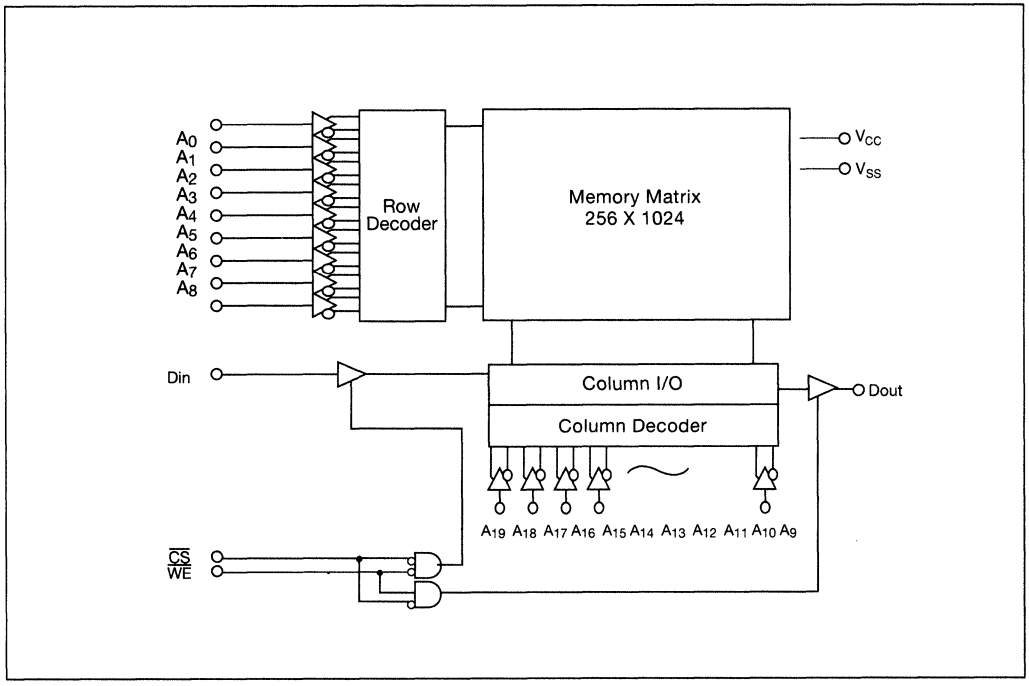
(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0-A19	Address
D_{IN}	Input
D_{OUT}	Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

2

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

Note: 1. X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{in}	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_{in} min = −2.0 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM621100A-20			HM621100A-25/35			Unit	Test Conditions
		Min.	Typ[1]	Max.	Min.	Typ.[1]	Max.		
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	—	150	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle
Standby Power Supply Current (1)	I_{SB1}[2] I_{SB1}[3]	— —	0.02 —	2.0 100	— —	0.02 —	2.0 100	mA µA	CS = V_{CC} -0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} -0.2V
Output Low Voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL}= 8mA
Output High Voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.
2. P and JP version
3. LP and LJP version

2

■ CAPACITANCE (T_a = 25°C, f= 1 MHz)

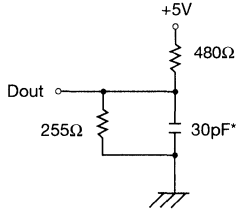
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0V
Output Capacitance	C_{out}	—	10	pF	V_{out} = 0V

Note: 1. This parameter is sampled and not 100% tested.

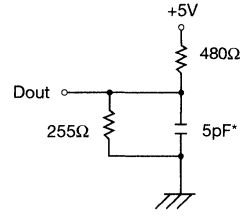
■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.6 V to 2.4 V
- Input rise and fall times: 4 ns
- Input timing reference levels: 2.2 V and 0.8 V
- Output timing reference levels: 2.0 V and 0.8 V
- Output load: See Figures



Output Load (A)



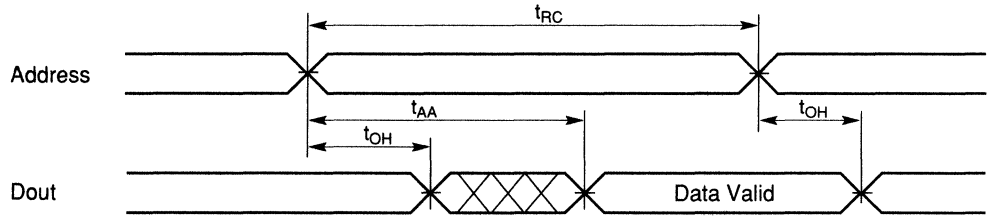
Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})

* Including scope & jig.

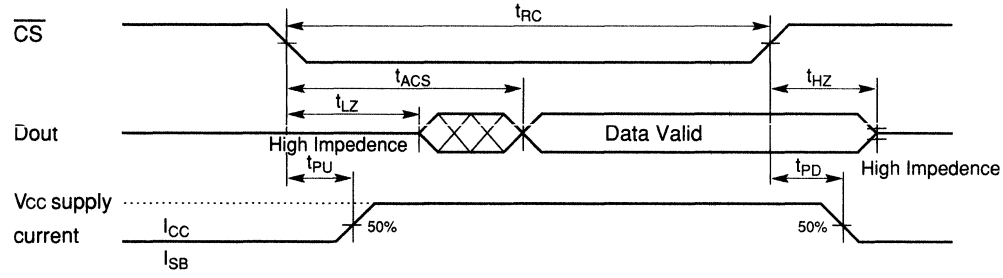
■ READ CYCLE

Parameter	Symbol	HM621100A -20		HM621100A -25		HM621100A -35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20	—	25	—	35	—	ns
Address Access Time	t_{AA}	—	20	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	20	—	25	—	35	ns
Chip Selection to Output in Low-Z	t_{LZ}[1]	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}[1]	0	10	0	12	0	15	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Power-Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	12	—	15	—	25	ns

■ READ TIMING WAVEFORM (1) [2, 3]



■ READ TIMING WAVEFORM (2) [2, 4]

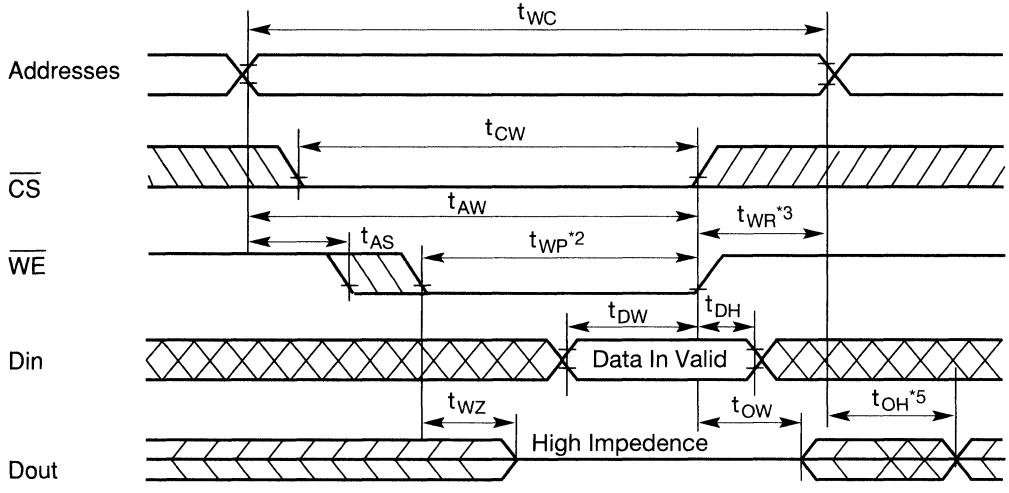


Notes: 1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. Device is continuously selected, $\overline{CS} = V_{IL}$.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

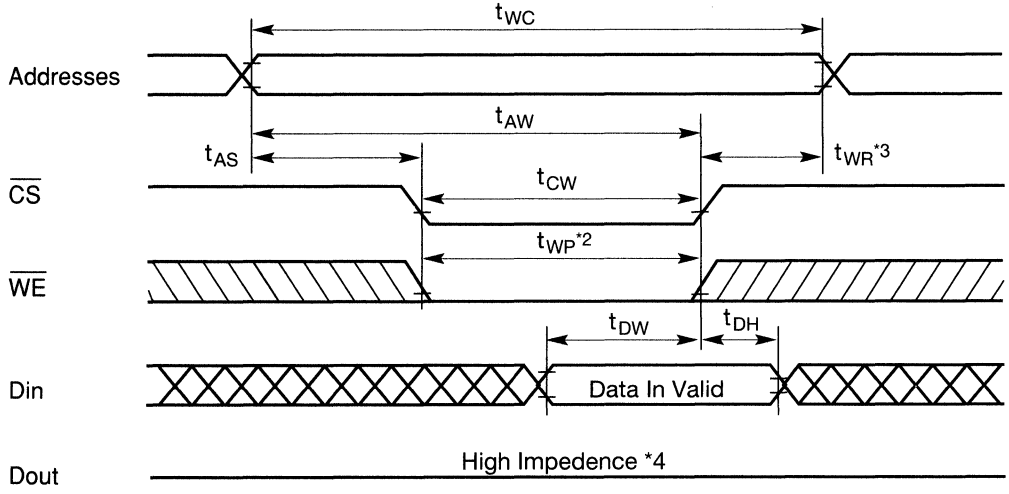
■ WRITE CYCLE

Parameter	Symbol	HM621100A -20		HM621100A -25		HM621100A -35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20	—	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	14	—	17	—	25	—	ns
Address Valid to End of Write	t_{AW}	16	—	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	14	—	17	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Write to Output in High-Z	t_{WZ}[1]	0	12	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}[1]	0	—	0	—	0	—	ns

■ WRITE TIMING WAVEFORM (1) ($\overline{WE}$ Controlled)



■ WRITE TIMING WAVEFORM (2) ($\overline{CS}$ Controlled)



Notes: 1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.

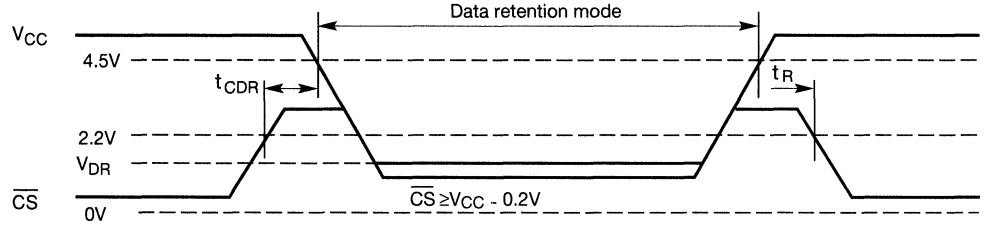
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristic is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$–0.2V $V_{in} \geq V_{CC}$ -0.2V or 0V ≤ V_{in} ≤ 0.2V
Data Retention Current	I_{CCDR}	—	2	100[1]	µA	
Chip Deselect to Data Retention Time	tCDR	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: V_{CC} = 3.0 V.

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



HM628512 Series

Preliminary

524,288-Word x 8-Bit High Speed CMOS Static RAM

■ DESCRIPTION

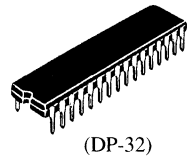
The Hitachi HM628512 is a 4M-bit Static RAM organized 512-kword x 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5 μm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 600-mil plastic DIP, is available for high density mounting. LP-version is suitable for battery back up system.

■ FEATURES

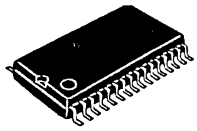
- High speed
  Fast Access time 55/70/85/100 ns (max.)
- Low power
  Standby: 10 μW (typ.) (L/L-SL version)
  Operation: 75 mW/MHz (typ.)
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state input
- Directly TTL compatible: All inputs and outputs
- Capacility of battery back up operation
  (L/L-SL version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM628512P-5	55 ns	600-mil, 32 pin Plastic DIP (DP-32)
HM628512P-7	70 ns	
HM628512P-8	85 ns	
HM628512P-10	100 ns	
HM628512LP-5	55 ns	
HM628512LP-7	70 ns	
HM628512LP-8	85 ns	
HM628512LP-10	100 ns	
HM628512LP-5SL	55 ns	
HM628512LP-7SL	70 ns	
HM628512LP-8SL	85 ns	
HM628512LP-10SL	100 ns	
HM628512FP-5	55 ns	525-mil, 32 pin Plastic SOP (FP-32D)
HM628512FP-7	70 ns	
HM628512FP-8	85 ns	
HM628512FP-10	100 ns	
HM628512LFP-5	55 ns	
HM628512LFP-7	70 ns	
HM628512LFP-8	85 ns	
HM628512LFP-10	100 ns	
HM628512LFP-5SL	55 ns	
HM628512LFP-7SL	70 ns	
HM628512LFP-8SL	85 ns	
HM628512LFP-10SL	100 ns	



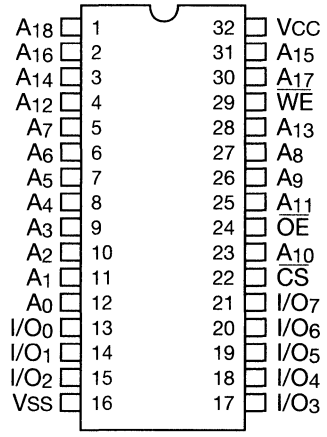
(DP-32)



(FP-32D)

■ PIN ARRANGEMENT

HM628512 Series



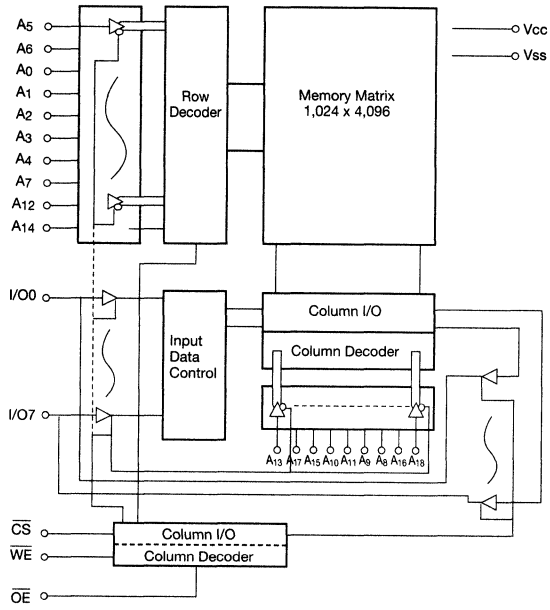
(Top View)

■ PIN DESCRIPTION

Symbol	Function
A_0–A_{18}	Address
I/O_0–I/O_7	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

2

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
X	H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output Disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	D_{out}	Read Cycle
L	L	H	Write	I_{CC}	D_{in}	Write Cycle (1)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (2)

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	–0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature Under Bias	T_{bias}	–10 to +85	°C

Notes 1. –3.0V for pulse half-width ≤ 30 ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	–0.3*1	—	0.8	V

Note *1. -3.0V for pulse half-width ≤ 30ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	Test Conditions	Min	Typ*1	Max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	—	—	2	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$= V_{SS} to V_{CC}	—	—	2	µA
Operating Power Supply Current: DC	I_{CC}	$\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL}, $I_{I/O}$= 0 mA	—	15	35	mA
Operating Power Supply Current	I_{CC1}	Min. Cycle, Duty = 100% $\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA	—	55	90	mA
	I_{CC2}	Cycle Time = 1 µs, Duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2V, V_{IH} ≥ V_{CC} –0.2V, V_{IL} ≤ 0.2V	—	15	30	mA
Standby Power Supply Current: DC	I_{SB}	$\overline{CS}$ = V_{IH}	—	1	3	mA
Standby Power Supply Current (1): DC	I_{SB1}	V_{in} ≥ 0V, $\overline{CS}$ ≥ V_{CC} –0.2V	—	0.02	2	mA
		V_{in} ≥ 0V, $\overline{CS}$ ≥ V_{CC} –0.2V	—	2*2	100*2	µA
		V_{in} ≥ 0V, $\overline{CS}$ ≥ V_{CC} –0.2V	—	2*3	50*3	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –1.0 mA	2.4	—	—	V

Notes: 1. Typical values are at V_{CC} = 5.0V, T_a = +25°C and specified loading.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a = 25°C, f = 1.0 MHz)*1

Item	Symbol	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	8	pF	V_{IN} = 0V
Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

Note *1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} 5V ± 10%, unless otherwise noted.)

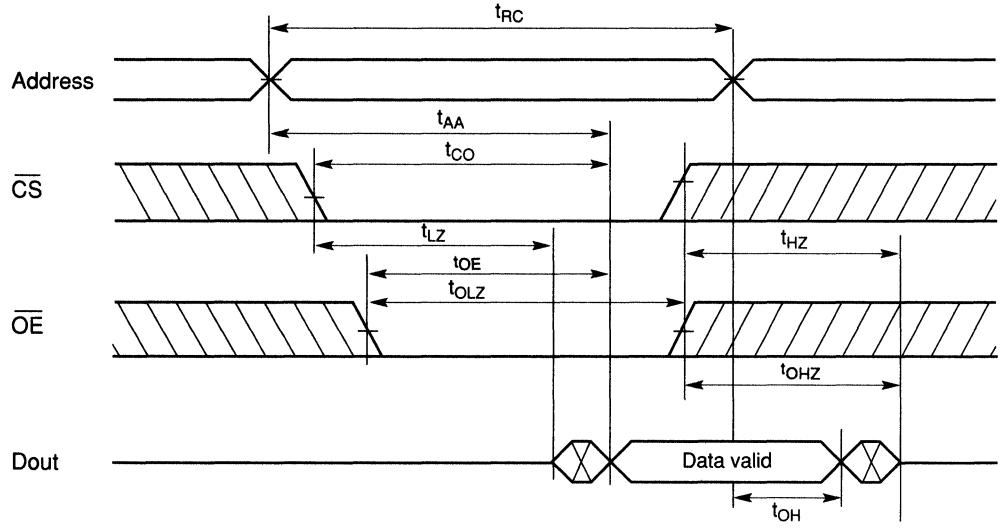
Test Conditions

- Input pulse levels: 0.8V to 2.4V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: 1 TTl gate + C_L (100 pF) (including scope and jig)

■ READ CYCLE

Item	Symbol	HM628512-5		HM628512-7		HM628512-8		HM628512-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	55	—	70	—	85	—	100	—	ns	
Address Access Time	t_{AA}	—	55	—	70	—	85	—	100	ns	
Chip Select Access Time	t_{CO}	—	55	—	70	—	85	—	100	ns	
Output Enable to Output Valid	t_{OE}	—	25	—	35	—	45	—	50	ns	
Chip Selection to Output in Low-Z	t_{LZ}	5	—	10	—	10	—	10	—	ns	1,2,3
Output Enable to Output in Low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	1,2,3
Chip Deselection to Output in High-Z	t_{HZ}	0	20	0	25	0	30	0	35	ns	1,2,3
Output Disable to Output in High-Z	t_{OHZ}	0	20	0	25	0	30	0	35	ns	1,2,3
Output Hold from Address Change	t_{OH}	5	—	10	—	10	—	10	—	ns	

■ READ TIMING WAVEFORM*4

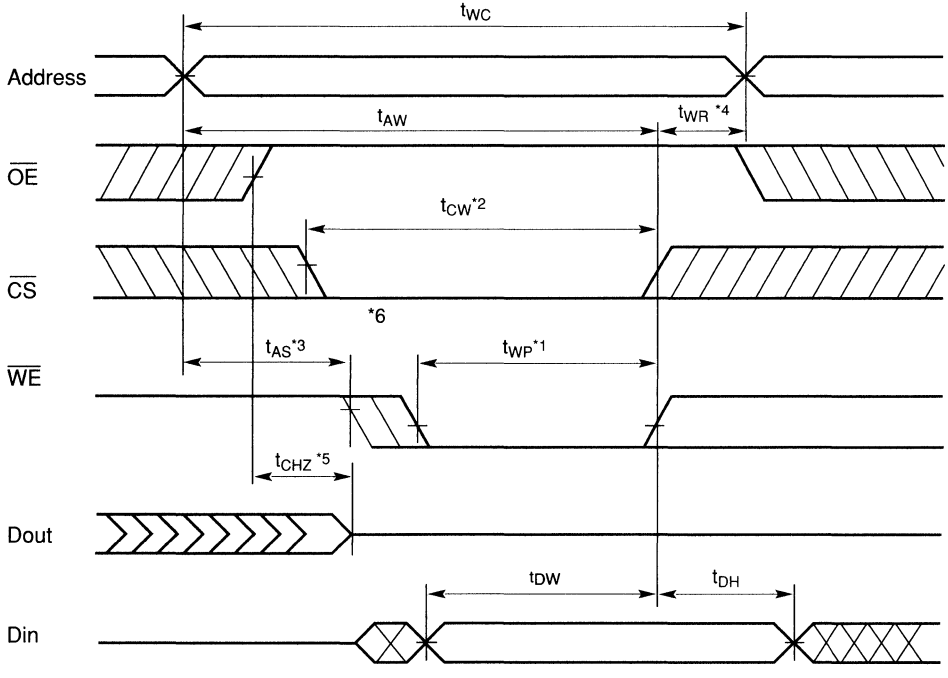


Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve and open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for read cycle.

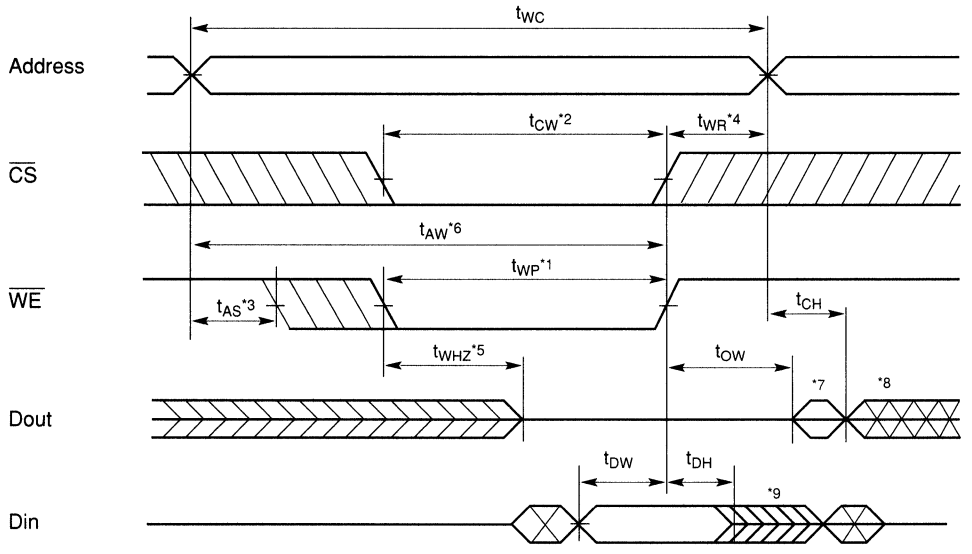
■ WRITE CYCLE

Parameter	Symbol	HM628512-5		HM628512-7		HM628512-8		HM628512-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	tWC	55	—	70	—	85	—	100	—	ns	
Chip Selection to End of Write	tCW	55	—	60	—	75	—	80	—	ns	
Address setup Time	tAS	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	tAW	50	—	60	—	75	—	80	—	ns	
Write Pulse Width	tWP	40	—	50	—	55	—	60	—	ns	
Write Recovery Time	tWR	5	—	5	—	5	—	5	—	ns	
$\overline{WE}$ to Output in High-Z	tWHZ	0	20	0	25	0	30	0	35	ns	10
Data to Write Time Overlap	tDW	25	—	30	—	35	—	40	—	ns	
Data Hold from Write Time	tDH	0	—	0	—	0	—	0	—	ns	
Output Active from End of Write	tOW	5	—	5	—	5	—	5	—	ns	10

■ WRITE TIMING WAVEFORM (1) ($\overline{OE}$ Clock)



■ WRITE TIMING WAVEFORM (2) ($\overline{OE}$ Low Fixed)



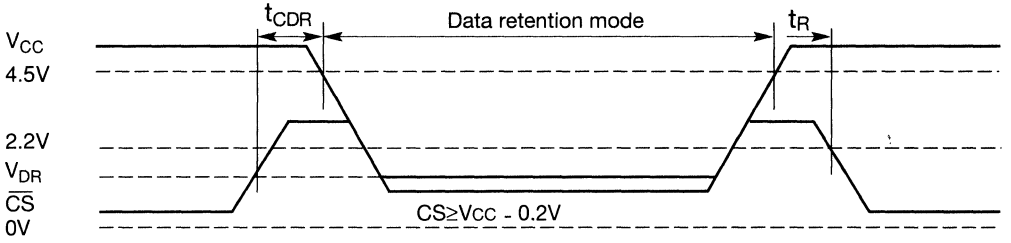
Notes:
1. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from $\overline{CS}$ going low to the end of write.
3. tAS is measured from $\overline{CS}$ going low to the end of write.
4. tWR is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If CS is low during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C,)

This characteristics is guaranteed only for L/L-SL version

Item	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2V, $V_{in} \geq 0V$
Data Retention Current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3.0V, $V_{in} \geq 0V$
		—	1	15*2	µA	$\overline{CS} \geq V_{CC}$ –0.2V
Chip Select to Data Retention Time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation Recovery Time	t_R	5	—	—	ms	

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM ($\overline{CS}$ Controlled)



Notes: 1. For L-version and 20 µA max. at T_a = 0 to 40°C.
2. For SL-version and 3 µA max. at T_a = 0 to 40°C.
3. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and D_{in} buffer. In data retention mode, V_{in} levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM66205 Series

524,288-Word × 8-Bit High Density CMOS Static RAM Module

Description

The HM66205 is a high density 4M-bit static RAM module consisting of 4 pieces HM628128LTS products (TSOP type 1M static RAM) and a HD74ACT138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66205 is the standard 600 mil width 32 pin dual-inline package. Its pin arrangement is completely compatible with the forthcoming 4M-bit monolithic static RAM.

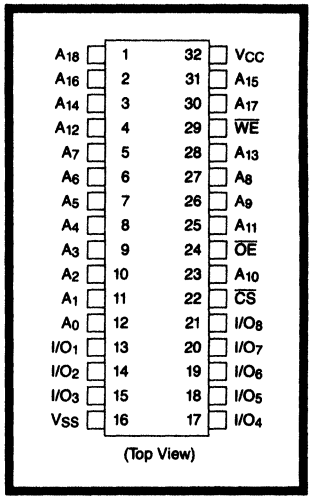
The HM66205 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66205 makes high density mounting possible with no surface mount technology.

These features make the HM66205 ideally suited for high density, compact memory system.

Features

- High density 32 pin DIP
  - Mounting 4 pcs. of 1M static RAM (TSOP; HM628128LTS) and CMOS decoder logic (SOP; HD74ACT138FP equivalent).
- Pin compatible with 4M monolithic static RAM
- High speed
  - Fast access time 85/100/120ns (maximum).
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low Power standby and low power operation
  - Standby: .....40 μW (typical)
  - Operation: .....80 mW (typical)
- Common data input and output, three state outputs
- Capable of battery backup operation
- Directly TTL compatible: All inputs and outputs

■ PIN ARRANGEMENT



■ PIN DESCRIPTION

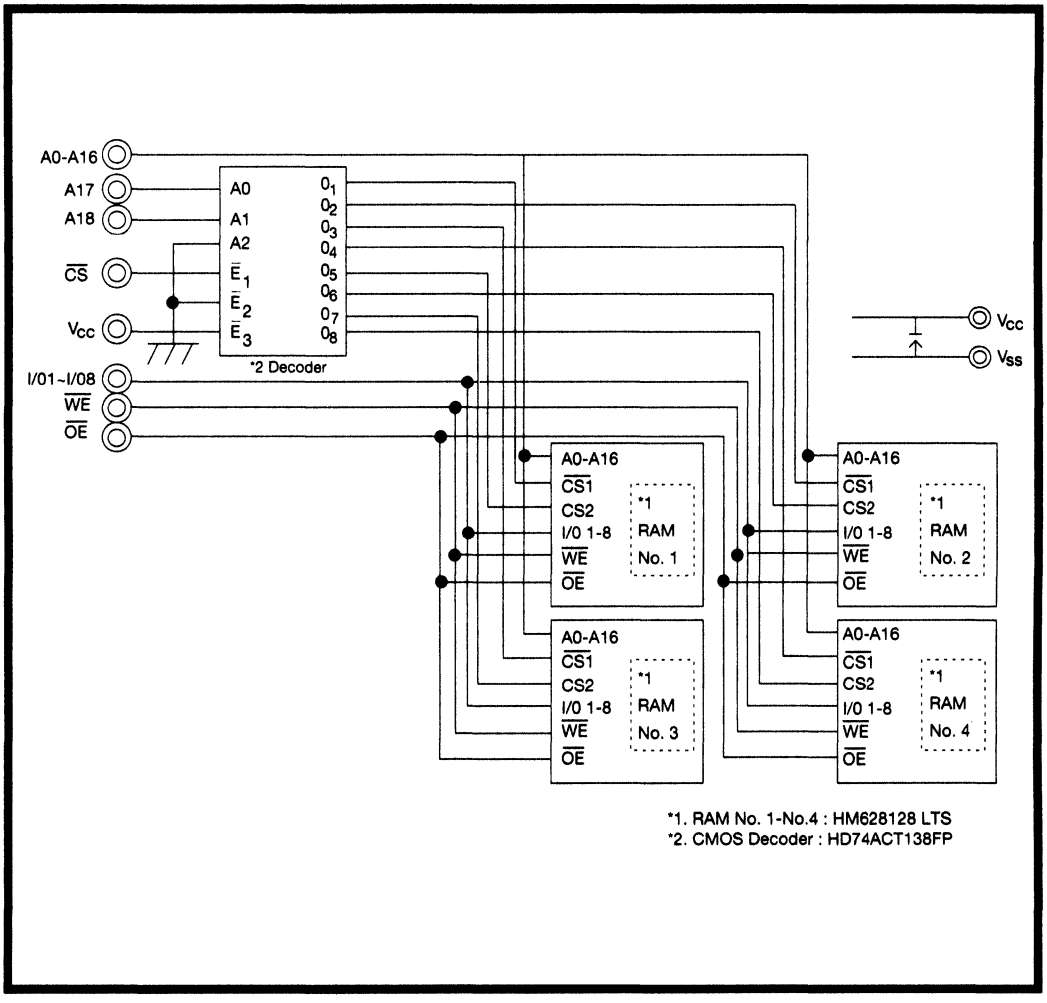
Pin Name	Function
A_0–A_{18}	Address
I/O_1–I/O_8	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ TYPE OF PRODUCTS

Part No.	Access	Package
HM66205L-85	85 ns	600-mil Module DIP
HM66205L-10	100 ns	
HM66205L-12	120 ns	

The 66205 module was designed for pinout and signal compatibility with the forthcoming 512K × 8 monolithic device.

■ BLOCK DIAGRAM



2

■ MODE SELECTION

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not Selected (Power Down)	H	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	D_{out}	I_{CC}	Read Cycle(1)-(3)
Write	L	L	H	D_{in}	I_{CC}	Write Cycle(1)
	L	L	L	D_{in}	I_{CC}	Write Cycle(2)

NOTE: X = Don't care (H or L).

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 ~ +85	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5	—	0.8	V

■ DC CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2	μA	$V_{in} = V_{SS} \sim V_{CC}$
Output Leakage Current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O} = V_{SS} \sim V_{CC}$
Operating Power Supply Current: DC	I_{CC}	—	19	46	mA	$\overline{CS} = V_{IL}$, Others V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average Operating Power Supply Current(1)	I_{CC1}	—	48	89	mA	Min. Cycle, Duty = 100% $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0 mA, Other V_{IH}/V_{IL}
Average Operating Power Supply Current(2)	I_{CC2}	—	16	36	mA	Cycle Time = 1μs, Duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS} \leq 0.2V$, $V_{IH} = V_{CC} - 0.2V$, $V_{IL} \leq 0.2V$
Standby Power Supply Current: DC	I_{SB}	—	4	12	mA	$\overline{CS} = V_{IH}$
Standby Power Supply Current(1)	I_{SB1}	—	8	400	μA	$V_{in} \geq 0V$, $\overline{CS} = V_{CC} - 0.2$
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -1.0 mA

NOTE: 1. Typical values are at V_{CC} = 5.0V, T_A = +25°C and specified loading.

■ CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Input Capacitance (1)	C_{in1}	—	45	pF	V_{in} = 0V	A_0-A_{16}, $\overline{WE}$, $\overline{OE}$
Input Capacitance (2)	C_{in2}	—	45	pF	V_{in} = 0V	A_{17}-A_{18}, $\overline{CS}$
Input/Output Capacitance	$C_{I/O}$	—	50	pF	$V_{I/O}$ = 0V	I/O_1-I/O_8

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

AC Test Conditions

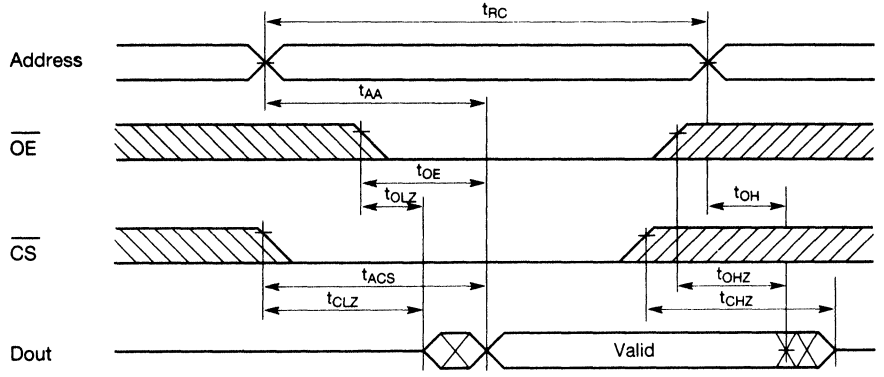
Input pulse levels: 0.8V to 2.4V
Input rise and fall times: 5 ns
Input and output timing reference level: 1.5V
Output load: 1 TTL gate and C_L - 100 pF (including scope and jig)

2

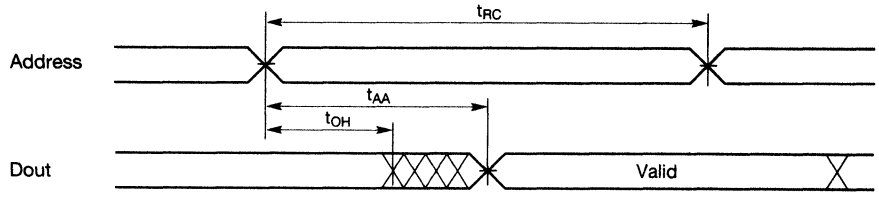
• Read Cycle

Parameter	Symbol	HM66205L-85		HM66205L-10		HM66205L-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85	—	100	—	120	—	ns
Address Access Time	t_{AA}	—	85	—	100	—	120	ns
Chip Select Access Time	t_{ACS}	—	85	—	100	—	120	ns
Output Enable to Output Valid	t_{OE}	—	35	—	45	—	50	ns
Chip Selection to Output in Low-Z	t_{CLZ}	10	—	10	—	10	—	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}	0	25	0	30	0	35	ns
Output Disable to Output in High-Z	t_{OHZ}	0	20	0	30	0	35	ns
Output Hold From Address Change	t_{OH}	10	—	10	—	10	—	ns

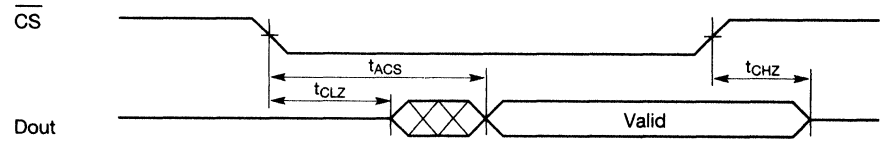
• Read Cycle Timing (1) *1



• **Read Cycle Timing (2)** *1, *2, *4



• **Read Cycle Timing (3)** *1, *3, *4



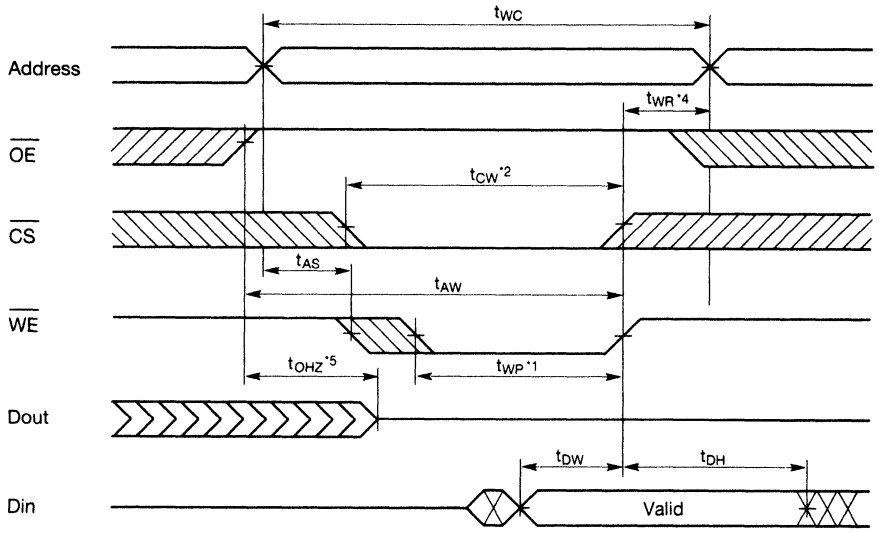
Not Valid

NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.

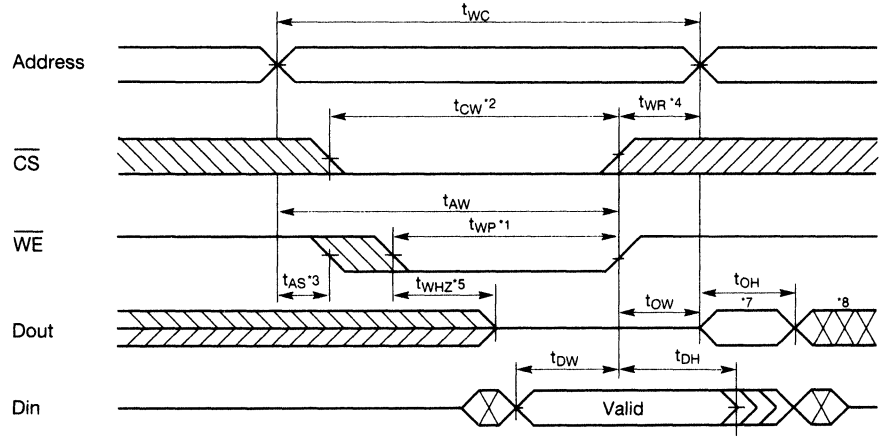
• **Write Cycle**

Parameter	Symbol	HM66205L-85		HM66205L-10		HM66205L-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85	—	100	—	120	—	ns
Chip Selection to End of Write	t_{CW}	75	—	90	—	100	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	75	—	90	—	100	—	ns
Write Pulse Width	t_{WP}	65	—	75	—	85	—	ns
Write Recovery	t_{WR}	5	—	5	—	10	—	ns
Write to Output in High-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	45	—	ns
Data Hold From Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Active From End of Write	t_{OW}	5	—	5	—	5	—	ns

• **Write Cycle Timing (1)** ($\overline{OE}$ Clock)



• **Write Cycle Timing (2)** *5 ($\overline{OE}$ Low Fixed)



NOTES:
1. A write occurs during the overlap (t_{WP} of a low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$).
6. D_{out} should be held in the phase of the written data during this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

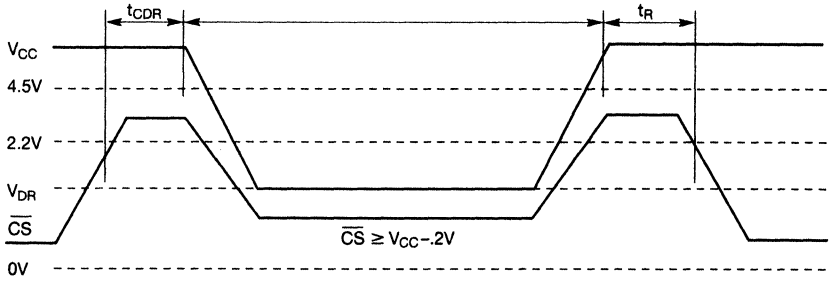
Not Valid

• **Low V_{CC} Data Retention Characteristics** (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{IN}$, A_{17}-$A_{18} \geq V_{IN}$
Data Retention Current	I_{CCDR}	—	4	200	µA	$\overline{CS} \geq V_{IN}$, V_{IN} = 0V
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation Recovery Time	t_R	t_{RC}	—	—	ns	

NOTE: 1. t_{RC} = Read Cycle Time.

■ **Low V_{CC} Data Retention Waveform**

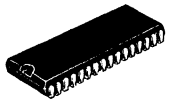


HM624100 Series —Preliminary

1,048,576-Word x 4-Bit High Speed CMOS Static Ram

■ FEATURES

- High Speed:
  Fast access time 25/30/35/45 ns(max.) (P-version)
  30/35/45 ns (max.) (LP-version)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle time
- TTL compatible–All inputs and outputs
- Thin plastic package for high density mounting



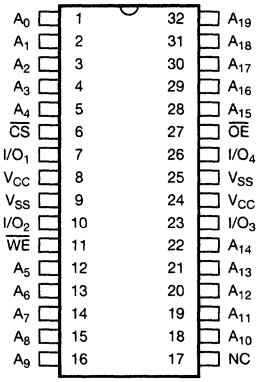
(CP-32D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624100JP-25	25 ns	400 mil 32-pin SOJ (CP-32D)
HM624100JP-30	30 ns	
HM624100JP-35	35 ns	
HM624100JP-40	45 ns	
HM624100JLP-30	30ns	
HM624100JLP-35	35ns	
HM624100JLP-45	45ns	
HM624100P-25	25ns	32-pin TSOP (II)
HM624100P-30	30ns	
HM624100P-35	35ns	
HM624100P-45	45ns	
HM624100LP-30	30ns	
HM624100LP-35	35ns	
HM624100LP-45	45ns	

■ PIN ARRANGEMENT

HM624100 Series

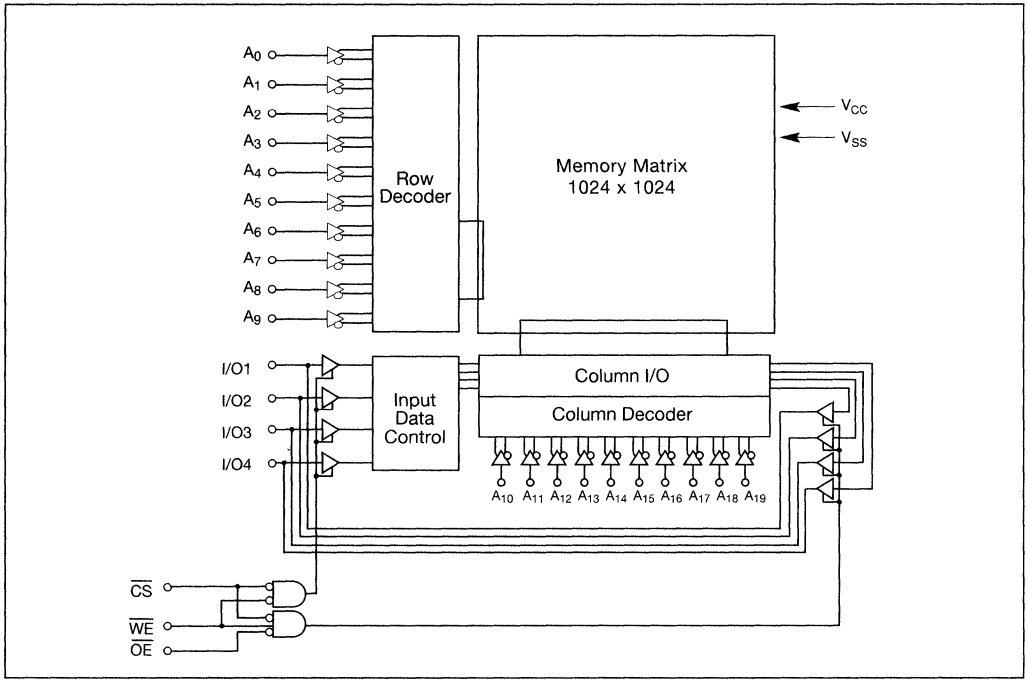


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A19	Address Input
I/O1–I/O4	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
VSS	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Deselect	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read Cycle 1, 2, 3
L	H	L	Write	I_{CC}	Din	Write Cycle 1
L	L	L	Write	I_{CC}	Din	Write Cycle 2

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5^1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature Under Bias	T_{bias}	–10 to +85	°C

Note: 1. V_T min = –2.0 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	–0.5[1]	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	HM624100P			HM624100LP			Unit	Test Conditions
		Min.	Typ	Max.	Min.	Typ	Max.		
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC}	—	—	150	—	—	140	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Cycle=25 ns. (P), 35 ns. (LP)
Standby VCC Current	I_{SB}	—	—	60	—	—	5	mA	$\overline{CS}$ = V_{IH} Cycle=25 ns. (P), 35 ns. (LP)
	I_{SB1}	—	—	10	—	—	0.1	mA	$\overline{CS}$ ≥ V_{CC} –0.2V 0 V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} –0.2V
Output Low Voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL}= 8mA
	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4mA

■ CAPACITANCE (Ta = 25°C, f= 1 MHz)

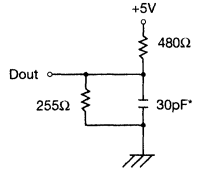
Item	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{in} = 0 V
Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

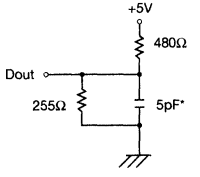
■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 4 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See Figures



Output Load (A)



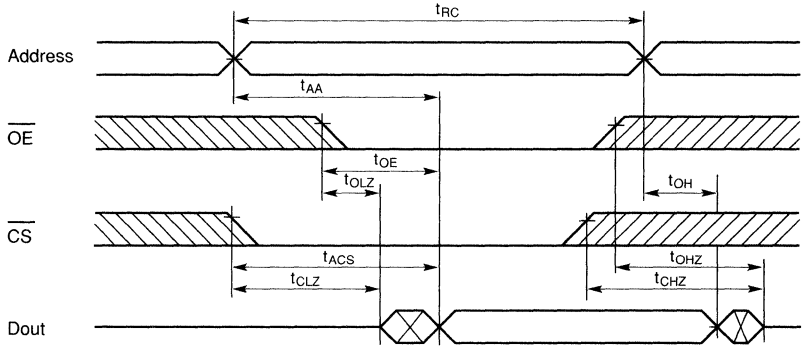
Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})

* Including scope & jig.

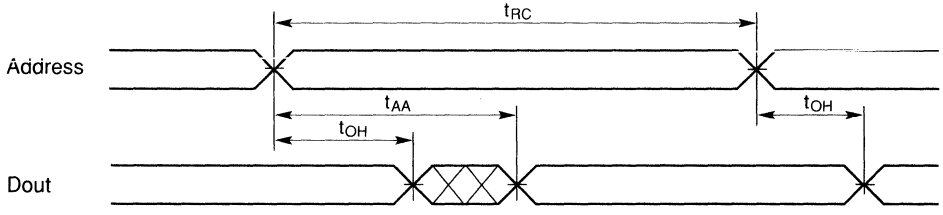
■ READ CYCLE

Item	Symbol	HM624100-25 P		HM624100-30 P/LP		HM624100-35 P/L		HM624100-45 P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ}[1]	5	—	5	—	5	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	15	—	20	ns
Output Enable to Output in Low-Z	t_{OLZ}[1]	0	—	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}[1]	0	10	0	10	0	15	0	15	ns
Chip Disable to Output in High-Z	t_{OHZ}[1]	0	10	0	10	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	30	—	20	ns

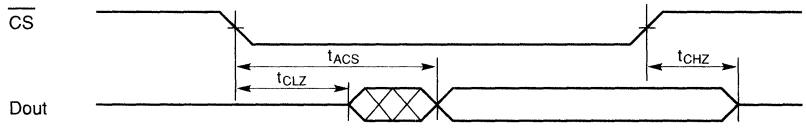
■ READ TIMING WAVEFORM (1) [1, 2]



■ READ TIMING WAVEFORM (2) [2, 3, 5]



■ READ TIMING WAVEFORM (3) [1, 2, 4, 5]

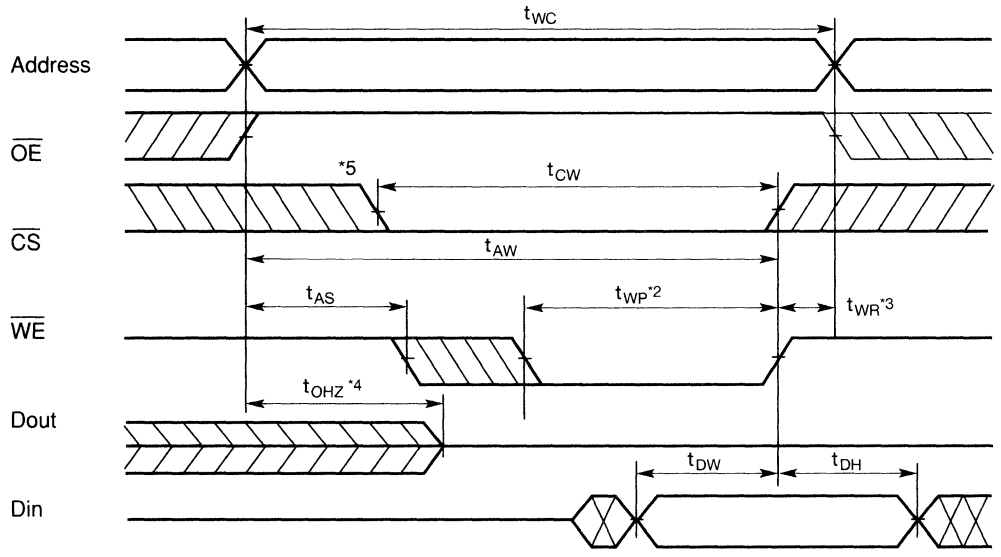


Notes: 1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. $\overline{CS}$ is low.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE}$ = V_{IL}.

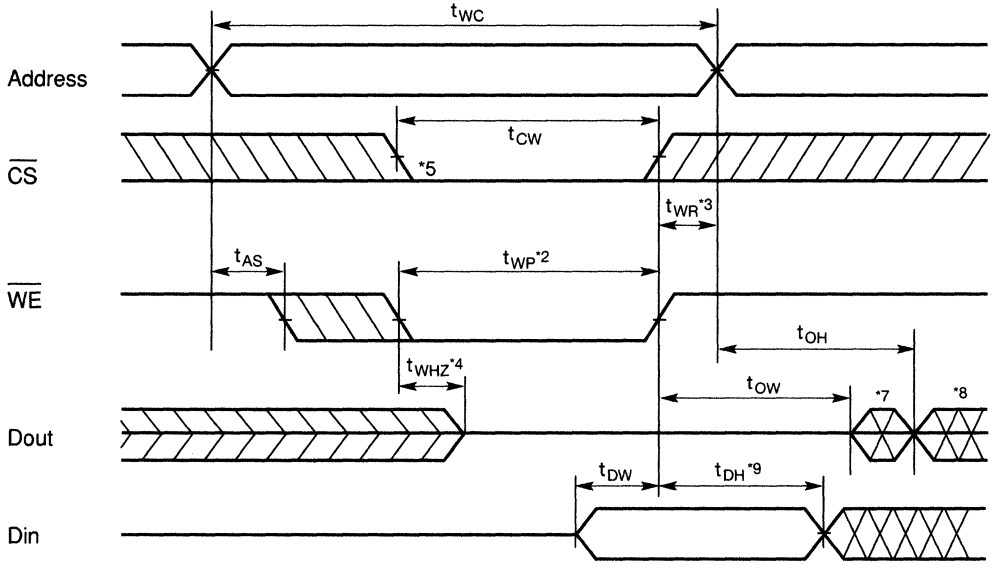
■ WRITE CYCLE

Parameter	Symbol	HM624100-25 P		HM624100-30 P/LP		HM624100-35 P/L		HM624100-45 P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	25	—	30	—	35	—	45	—	ns
Chip Selection to End of Write	tCW	15	—	20	—	25	—	35	—	ns
Address Valid to End of Write	tAW	15	—	20	—	25	—	35	—	ns
Address Setup Time	tAS	0	—	0	—	0	—	0	—	ns
Write Pulse Width	tWP	15	—	20	—	25	—	35	—	ns
Write Recovery Time	tWR	0	—	0	—	0	—	0	—	ns
Output Disable to Output in High-Z	tOHZ	0	10	0	10	0	15	0	15	ns
Write to Output in High-Z[1]	tWHZ	0	10	0	10	0	15	0	15	ns
Data to Write Time Overlap	tDW	12	—	15	—	20	—	30	—	ns
Data Hold from Write Time	tDH	0	—	0	—	0	—	0	—	ns
Output Active from End of Write	tOW	0	—	0	—	0	—	0	—	ns

■ WRITE TIMING WAVEFORM (1)



■ WRITE TIMING WAVEFORM (2) [6]



Notes:
1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or WE going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
5. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the WE transition, output remain a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied.

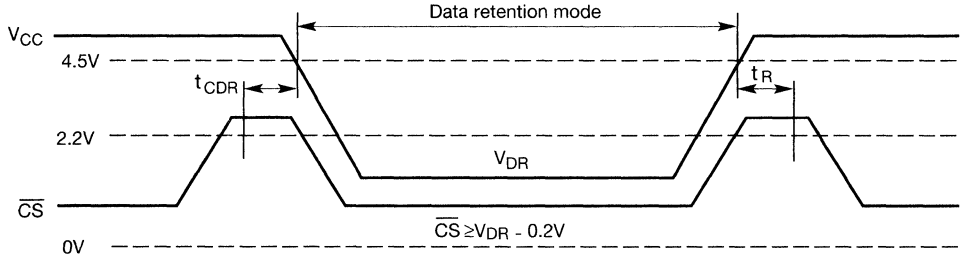
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristic is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$–0.2V, $V_{in} \geq V_{CC}$ -0.2V or 0V ≤ V_{in} ≤ 0.2V
Data Retention Current	I_{CCDR}	—	—	100[1]	µA	
Chip Select to Data Retention Time	tCDR	0	—	—	ns	
Operation Recovery Time	tR	5	—	—	ms	

Note: V_{CC} = 3.0 V.

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



2

HM621400 Series — Preliminary

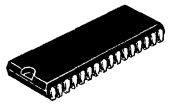
4,194,304-Word x 1-Bit High Speed CMOS Static RAM

■ FEATURES

- High Speed:
  Fast access time 25/30/35/45 ns(max.) (P-version)
  30/35/45 ns(max.) (LP-version)
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- TTL compatible: All inputs and outputs
- Thin plastic package for high density mounting

■ ORDERING INFORMATION

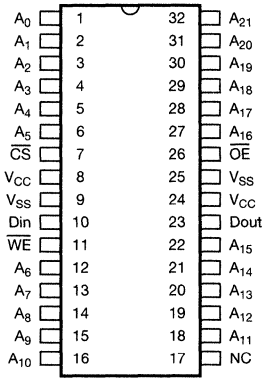
Type No.	Access Time	Package
HM621400JP-25	25 ns	400-mil, 32 pin SOJ (CP-32D)
HM621400JP-30	30 ns	
HM621400JP-35	35 ns	
HM621400JP-45	45 ns	
HM621400JLP-30	30 ns	
HM621400JLP-35	35 ns	
HM621400JLP-45	45 ns	
HM621400P-25	25 ns	32-pin TSOP (II)
HM621400P-30	30 ns	
HM621400P-35	35 ns	
HM621400P-45	45 ns	
HM621400LP-30	30 ns	
HM621400LP-35	35 ns	
HM621400LP-45	45 ns	



(CP-32D)

■ PIN ARRANGEMENT

HM621400 Series

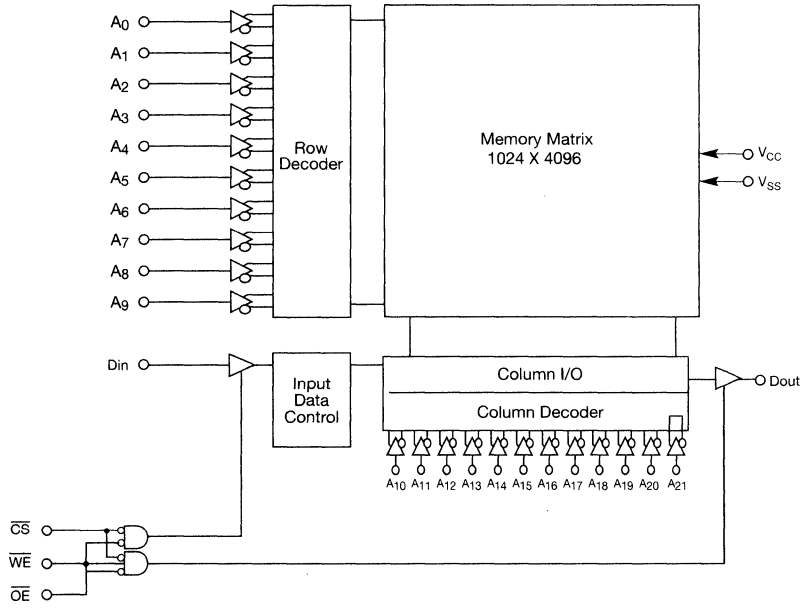


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{21}	Address Input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	X	Deselect	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle 1, 2, 3
L	H	L	Write	I_{CC}	D_{in}	Write Cycle 1
L	L	L	Write	I_{CC}	D_{in}	Write Cycle 2

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	-0.5^{*1} to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

Note 1. V_T min. = −2.0V for pulse width ≤ 10 ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.5^{*1}	—	0.8	V

Note 1. V_{IL} min. = −2.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	HM621400P					HM621400LP				
		Min	Typ	Max	Unit	Test Conditions	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}	—	—	2.0	µA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC}	—	—	150	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA Cycle = 25 ns	—	—	140	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA Cycle = 30 ns
Standby V_{CC} Current	I_{SB}	—	—	60	mA	$\overline{CS}$ = V_{IH}, Cycle = 25 ns	—	—	5	mA	$\overline{CS}$ = V_{IH}, Cycle = 30 ns
	I_{SB1}	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} –0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} –0.2V	—	—	0.1	mA	$\overline{CS}$ ≥ V_{CC} –0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} –0.2V
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	—	—	0.4	V	I_{OL} = 8 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	2.4	—	—	V	I_{OH} = –4 mA

■ CAPACITANCE (T_a = 25°C, f = 1 MHz)

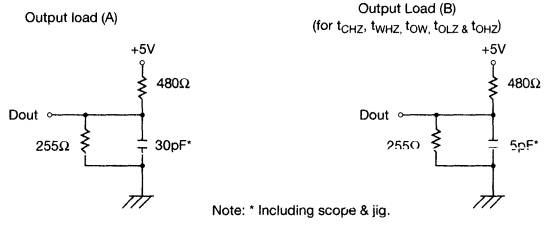
Item	Symbol	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

Note 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} 5V ± 10%, unless otherwise noted.)

Test Conditions

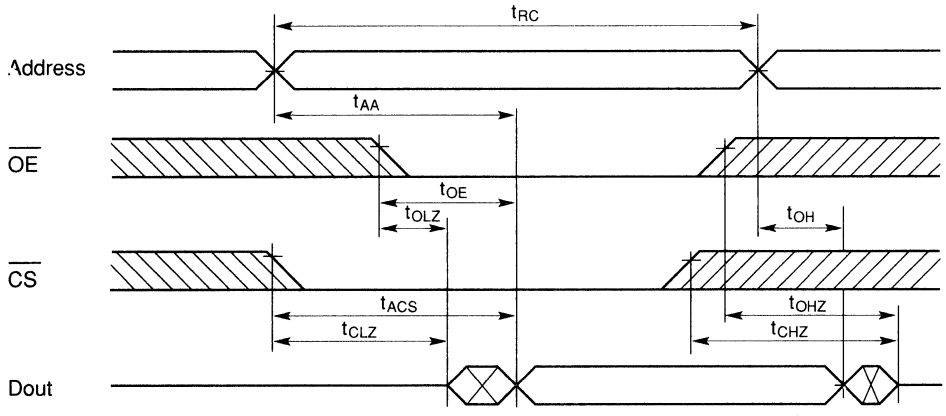
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 4ns
- Input and Output timing reference levels: Input 1.5V
  Output 1.5V
- Output load: See Figures



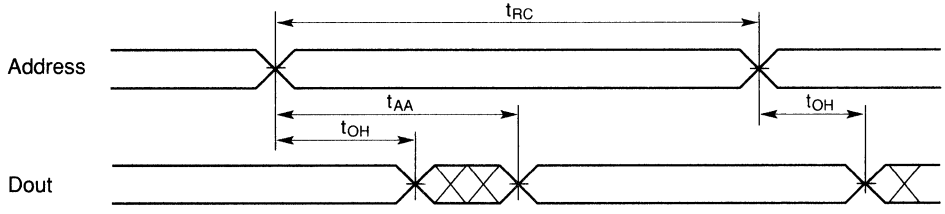
■ READ CYCLE

Item	Symbol	HM621400-25P		HM621400-30P/LP		HM621400-35P/LP		HM621400-45P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ}*1	5	—	5	—	5	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	15	—	20	ns
Output Enable to Output in Low-Z	t_{OLZ}*1	0	—	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}*1	0	10	0	10	0	15	0	15	ns
Chip Disable to Output in High-Z	t_{OHZ}*1	0	10	0	10	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	30	—	30	ns

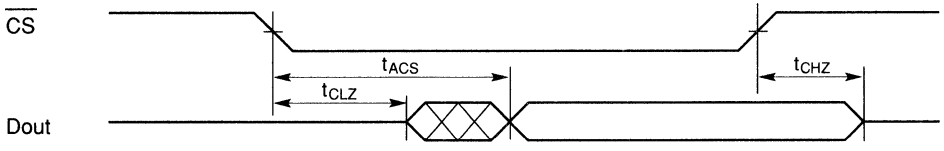
■ READ TIMING WAVEFORM (1)*1, *2



■ READ TIMING WAVEFORM (2)*2, *3, *5



■ READ TIMING WAVEFORM (3)*1, *2, *4, *5

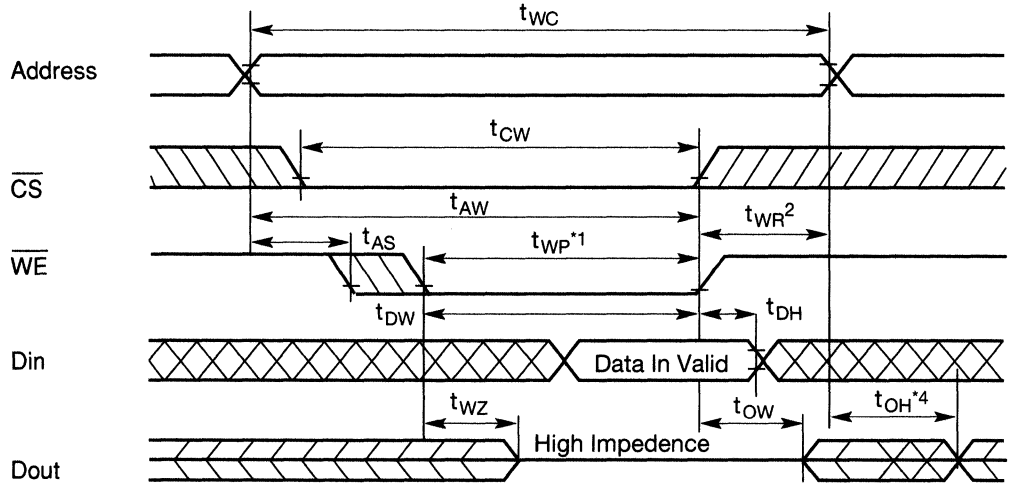


Notes:
1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. $\overline{CS}$ is low.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE}$ = V_{IL}.

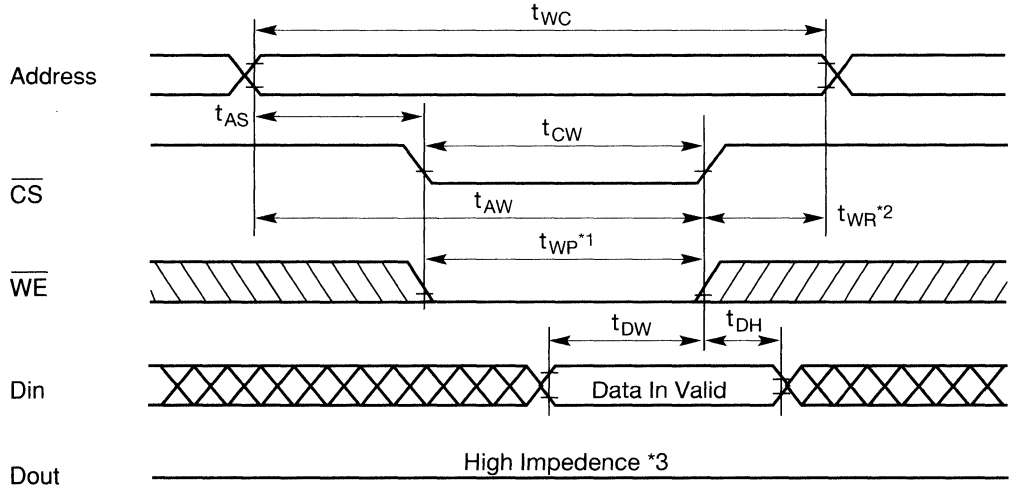
■ WRITE CYCLE

Parameter	Symbol	HM621400-25P		HM621400-30P/LP		HM621400-35P/LP		HM621400-45P/LP		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	25	—	30	—	35	—	45	—	ns	
Chip Selection to End of Write	t_{CW}	15	—	20	—	25	—	35	—	ns	
Address Valid to End of Write	t_{AW}	15	—	20	—	25	—	35	—	ns	
Address setup Time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	15	—	20	—	25	—	35	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	5	—	0	—	ns	
Output Disable to Output in High-Z	t_{OHZ}*5	0	10	0	10	0	15	0	15	ns	
Write to Output in High-Z	t_{WHZ}*5	0	10	0	10	0	15	0	15	ns	
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	30	—	ns	
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Ouput Active from End of Write	t_{OW}	0	—	0	—	0	—	0	—	ns	

■ WRITE TIMING WAVEFORM (1) ($\overline{WE}$ Controlled)



■ WRITE TIMING WAVEFORM (2) ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
4. D_{out} is the same phase of write data of this write cycle.
5. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

2

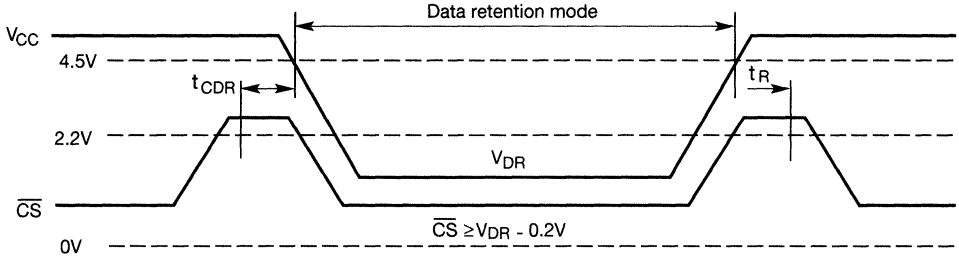
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2V, $V_{in} \geq V_{CC}$ –0.2V or 0V ≤ V_{in} ≤ 0.2V
Data Retention Current	I_{CCDR}	—	—	100*1	µA	
Chip Select to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0V.

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



Section 3
Cache Static RAM and Fast SRAM Modules

3

HITACHI®

HM62A168, HM62A188 Series

Direct Mapped 8,192-Word x 16(18)-Bit/ 2-Way 4,096-Word x 16(18)-Bit Static Cache Memory

■ DESCRIPTION

The Hitachi HM62A168/188 is a high speed 128(144)-k Cache memory organized as 2-way set associative 4k x 16(18) or direct mapped 8k x 16(18).

By using two HM62A168/188 can be achieved high performance 32-bit microprocessor system. The HM62A168/188, packaged in a 52-pin PLCC is available for high density mounting.

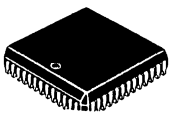
■ FEATURES

- Single 5V supply and high density 52-pin PLCC package
- High speed
  Access time: 25/30/35 ns (maximum)
- Directly TTL compatible
  All inputs and outputs
- Address latch
- Pin programmable for 8k x 16(18) or 2-way 4k x 16(18)

■ ORDERING INFORMATION

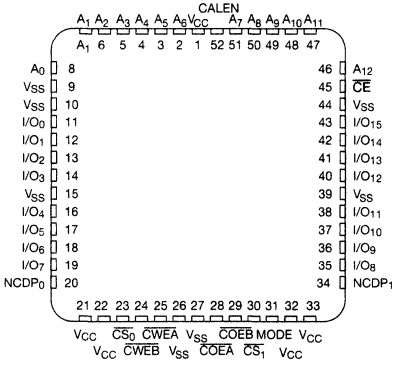
Type No.	Access Time	Package
HM62A168CP-25	25 ns	52-pin PLCC (CP-52)
HM62A168CP-25R	25 ns	
HM62A168CP-30	30 ns	
HM62A168CP-35	35 ns	
HM62A188CP-25	25 ns	
HM62A188CP-25R	25 ns	
HM62A188CP-30	30 ns	
HM62A188CP-35	35 ns	
HM62A168BCP-25*	25 ns	
HM62A168BCP-35*	35 ns	
HM62A188BCP-25*	25 ns	
HM62A188BCP-35*	35 ns	

*Please see note 6



(CP-52)

■ PIN ARRANGEMENT



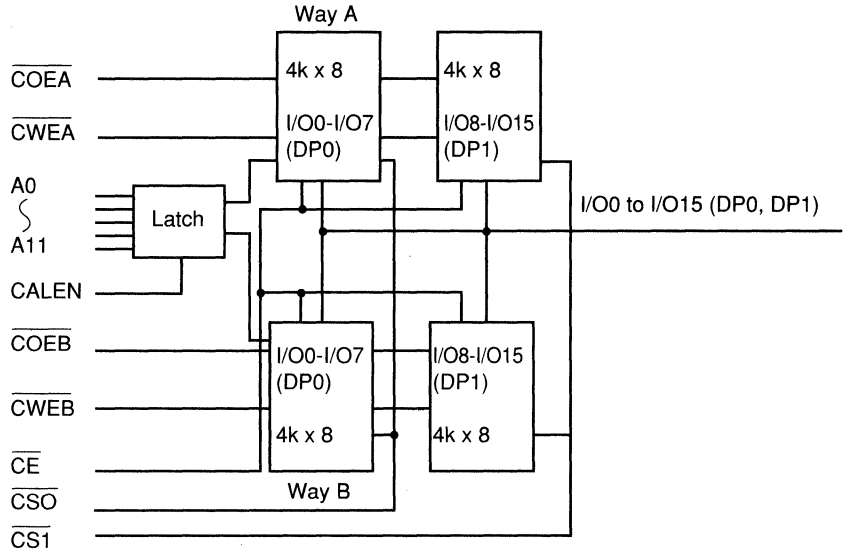
(Top View)

■ PIN DESCRIPTION

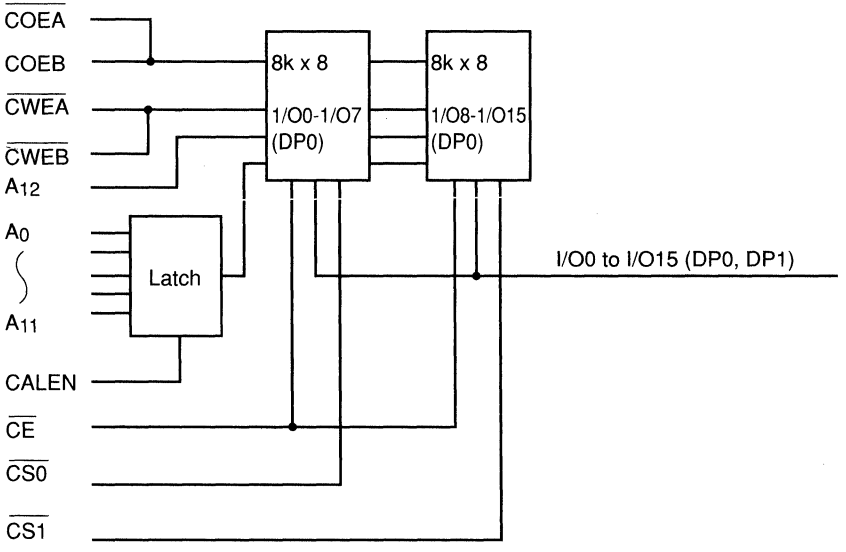
Pin Name	Function
CALEN	Cache Address Latch Enable
MODE	Mode Select
A0-A12	Address
$\overline{CS_0}$, $\overline{CS_1}$	Cache Chip Select
$\overline{COEA}$, $\overline{COEB}$	Cache Output Enable
$\overline{CWEA}$, $\overline{CWEB}$	Cache Write Enable
I/O0-I/O15	Data Input/Output
$\overline{CE}$	Cache Chip Enable
NC	No Connection
DP0, DP1	Parity Input/Output

■ BLOCK DIAGRAM

• **Topology Two-Way Set Associative** (MODE = Logic high)



• **Topology Direct Mapped** (MODE = Logic low)



Signal Description

Signal Name	Pin Number	Signal Description
A0-A6 A7-A11	8-2 51-47	Address inputs to the memory array. A0-A11 are latched on the falling edge of CALEN.
A12	46	A12 address input. In the two-way mode, address input A12 will be a "don't care" and should be externally wired to ground. In the direct-mapped mode. When MODE is connected to V_{SS}, A12 selects which of the two 4K x 16(18) banks is read from or written to. A12 is not latched by CALEN, as are the other address inputs.
CALEN	52	Cache Address Latch Enable input. This signal controls the internal address latches for inputs A0-A11 When CALEN is high, the latch is transparent. The falling edge of CALEN latches the current address input levels. A12 is static and is not controlled by CALEN.
I/O0-I/O15	11-14, 16-19, 35-38, 40-43	Data inputs and outputs. These are the three-state lines that provide data access to the memory array.
MODE	31	MODE input. This signal controls whether the memory device is to be used in a direct-mapped configuration (8K x 16(18)). When the MODE signal is high, the device is placed in the two-way mode. When the mode input is low, the cache is in the direct-mapped mode. This is a hard wired strap option and must not be changed dynamically.
$\overline{CS_0}$, $\overline{CS_1}$	23, 30	Cache Chip Select inputs. These active low signals selectively enable the two bytes of memory. $\overline{CS_0}$ low enables bits I/O0-I/O7 and DP0. $\overline{CS_1}$ low enables bits I/O8-I/O15 and DP1. This applies to both the direct-mapped and two-way modes.
$\overline{CE}$	45	Cache Chip Enable input (active low). This signal functions as a global chip enable. It gates the $\overline{COEA}$, $\overline{COEB}$, $\overline{CWEA}$, and $\overline{CWEB}$ inputs. A chip enable controlled write can be done by taking $\overline{CE}$ inactive high while one of the $\overline{CWEX}$ signals is active (assuming all other timings for a write cycle are met).
$\overline{COEA}$, $\overline{COEB}$	28, 29	Cache Output Enable inputs. These active low input enable cache bank A or bank B to drive the data bus when in the two-way mode. In the two-way mode, bank A is enabled when $\overline{COEA}$ is low and bank B is enabled when $\overline{COEB}$ is low. If both banks are activated at the same time, then both banks become deselected. In the direct-mapped mode, $\overline{COEA}$ and $\overline{COEB}$ must be tied together externally. A low on $\overline{COEA}$ and $\overline{COEB}$ then enables the outputs of the 8K x 16(18) memory. A12 is used to determine which 4K x 16(18) bank is accessed.
$\overline{CWEA}$, $\overline{CWEB}$	25, 24	Cache Write Enable inputs (active low). In the two-way mode when $\overline{CWEA}$ ($\overline{CWEB}$) is active, data is written into memory bank A (B). In the direct-mapped mode, $\overline{CWEA}$ and $\overline{CWEB}$ must be tied together externally. A low on $\overline{CWEA}$ and $\overline{CWEB}$ enables data to be written into the 8K x 16(18) memory. A12 is used to determine which 4K x 16(18) bank is accessed.
DP0 or NC DP1 or NC	20 34	Parity data inputs and outputs (HM62A188). These are three-state lines that provide parity data access to the memory array. For the HM62A168, these two pins are not used (NC) and must not be physically tied to V_{CC}, V_{SS}, or any other device inputs.
V_{CC}	1, 21, 22, 32, 33	System Power +5V. (21, 22, 32, 33 are for outputs)
V_{SS}	9, 10, 15, 26, 27 39, 44	System Ground. (10, 15, 39, 44 are for outputs)

■ FUNCTION TABLE

Two-Way Mode (Mode = High) 2-4K x 16(18)

$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	I/O_0-I/O_7 (DP_0)	I/O_8-I/O_{15} (DP_1)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output High-Z
X	X	X	L	L	X	X	High-Z	High-Z	Output High-Z
L	L	H	L	H	H	H	Output	High-Z	Read Way A
L	L	H	H	L	H	H	Output	High-Z	Read Way B
L	H	L	L	H	H	H	High-Z	Output	Read Way A
L	H	L	H	L	H	H	High-Z	Output	Read Way B
L	L	L	L	H	H	H	Output	Output	Read Way A
L	L	L	H	L	H	H	Output	Output	Read Way B
L	L	H	X	X	L	H	Input	High-Z	Write Way A
L	L	H	X	X	H	L	Input	High-Z	Write Way B
L	H	L	X	X	L	H	High-Z	Input	Write Way A
L	H	L	X	X	H	L	High-Z	Input	Write Way B
L	L	L	X	X	L	H	Input	Input	Write Way A
L	L	L	X	X	H	L	Input	Input	Write Way B
L	L	H	X	X	L	L	Input	High-Z	Write Way A & B
L	H	L	X	X	L	L	High-Z	Input	Write Way A & B
L	L	L	X	X	L	L	Input	Input	Write Way A & B

Direct Mode (Mode = Low) 8K x 16(18)

$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	I/O_0-I/O_7 (DP_0)	I/O_8-I/O_{15} (DP_1)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output High-Z
L	L	H	L	L	H	H	Output	High-Z	Read
L	H	L	L	L	H	H	High-Z	Output	Read
L	L	L	L	L	H	H	Output	Output	Read
L	L	H	X	X	L	L	Input	High-Z	Write
L	H	L	X	X	L	L	High-Z	Input	Write
L	L	L	X	X	L	L	Input	Input	Write

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{in}	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.4	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_{in} min = −2.5 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATION CONDITIONS (T_a = 0 to +70°C, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5*1	5.0	5.5*1	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*2	—	0.8	V

Note: 1. V_{CC} min = 4.75V and V_{CC} max. = 5.25V for HM62A168/188-25/25R/30.
2. V_{IL} min = −2.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%*1, V_{SS} = 0V, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10.0	µA	Output Disable $V_{I/O}$ = V_{SS} to V_{CC}
Active Operating Power Supply Current	I_{CC}	—	—	220	mA	V_{in} - V_{SS}/V_{CC}, $I_{I/O}$ = 0 mA, 2X Min. Cycle, $\overline{CE}$, $\overline{CS}$ = V_{IL} Max., CALEN = V_{IH} Min.
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} =4 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Notes: 1. V_{CC} = 5V ± 5% for HM62A168/188-25/25/25R/30, HM62A168B/188B-25.
2. Typical limits are at V_{CC} = 5.0, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f= 1 MHz.)*1

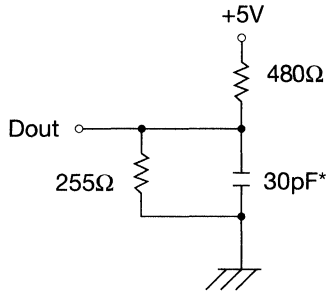
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	12	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

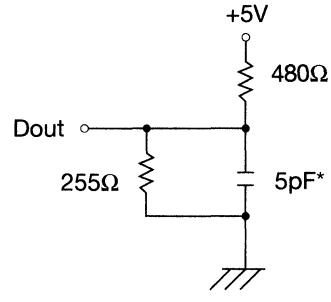
■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} 5V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 3ns
- Input and Output timing reference levels: 1.5V
- Output load: See figures
- Exceeding minimum air flow equipment: See air flow requirements



Output Load (A)
*Including scope & jig.



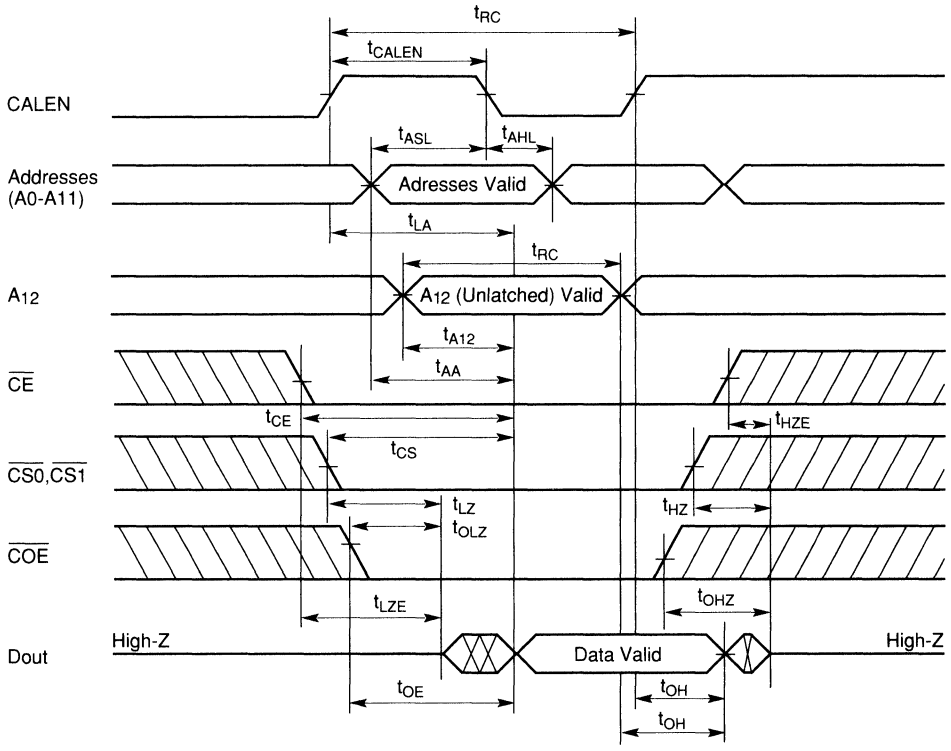
Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})

Note: 1. V_{CC} = 5V ± 5% for HM62A168/188-25/25R/30, HM62A168B/188B-25.

■ READ CYCLE

Parameter	Symbol	HM62A168/B-25 HM62A188/B-25		HM62A168-25R HM62A188-25R		HM62A168-30 HM62A188-30		HM62A168/B-35 HM62A188/B-35		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	25	—	25	—	30	—	35	—	ns	
Address Access Time	t_{AA}	—	25	—	25	—	30	—	35	ns	
A_{12} Address Access Time	t_{A12}	—	17	—	17	—	20	—	25	ns	
Chip Select Access Time	t_{CS}	—	20	—	20	—	20	—	25	ns	
Chip Enable Access Time	t_{CE}	—	20	—	22	—	22	—	25	ns	
CALEN High to Output Valid	t_{LA}	—	25	—	25	—	30	—	35	ns	1
Output Enable to Output Valid	t_{OE}	—	10	—	10	—	12	—	13	ns	
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	3	—	ns	2
Chip Select to Output Low-Z	t_{LZ}	3	—	3	—	3	—	3	—	ns	3
Chip Enable Low to Output Low-Z	t_{LZE}	5	—	5	—	5	—	5	—	ns	3
Output Enable to Output Low-Z	t_{OLZ}	2	—	2	—	2	—	2	—	ns	3
Chip Deselect to Output High-Z	t_{HZ}	—	15	—	15	—	15	—	25	ns	3
Chip Enable High to Output High-Z	t_{HZE}	—	15	—	15	—	15	—	25	ns	3
Output Disable to Output High-Z	t_{OHZ}	—	10	—	10	—	10	—	14	ns	3
Address Latch Enable Pulse Width	t_{CALEN}	8	—	8	—	8	—	10	—	ns	
Address Setup to Latch Low	t_{ASL}	4	—	4	—	4	—	6	—	ns	
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	5	—	ns	

■ READ TIMING WAVEFORM (1) ($\overline{CWE}$ = High)

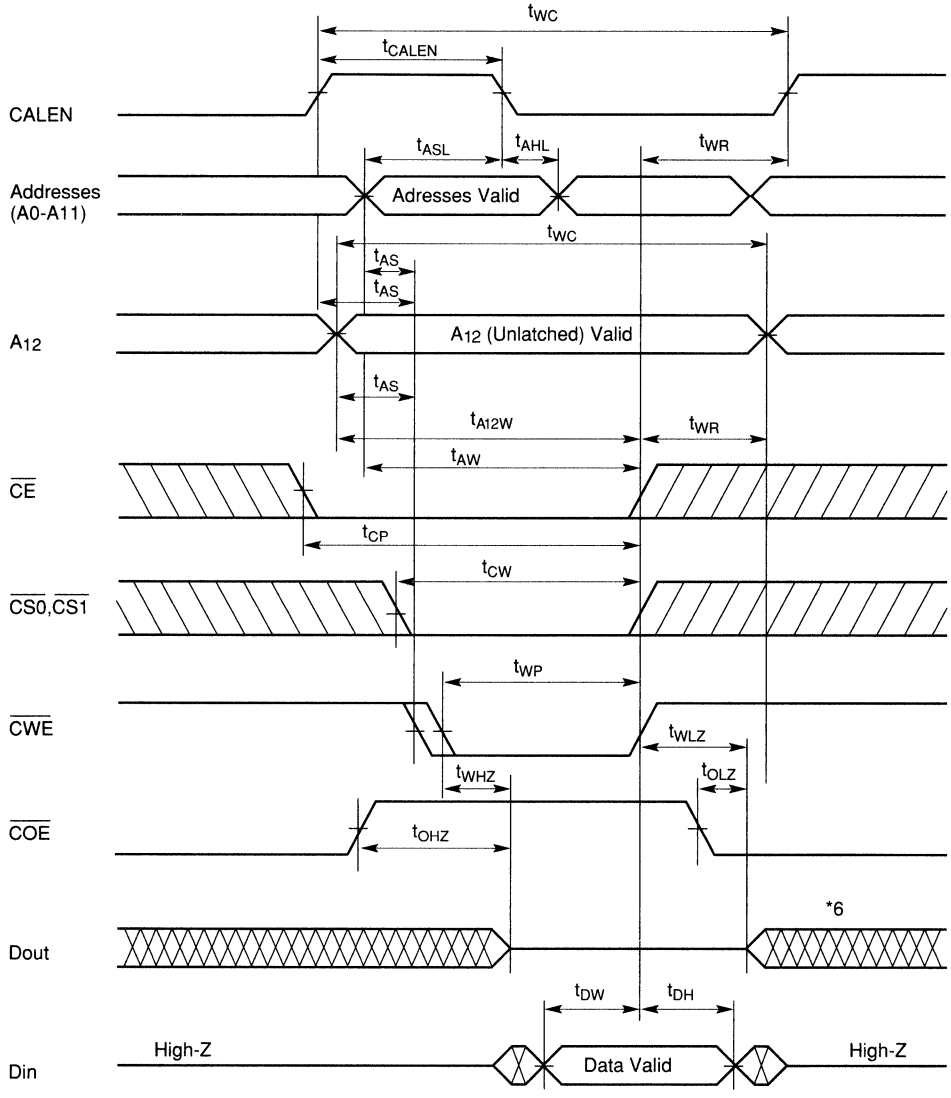


Notes:
1. t_{LA} is applied to the case that address is valid before CALEN goes high.
2. t_{OH} is determined by the earliest of CALEN going high, valid addresses A_0-A_{11} transition with CALEN high, or A_{12} transition.
3. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

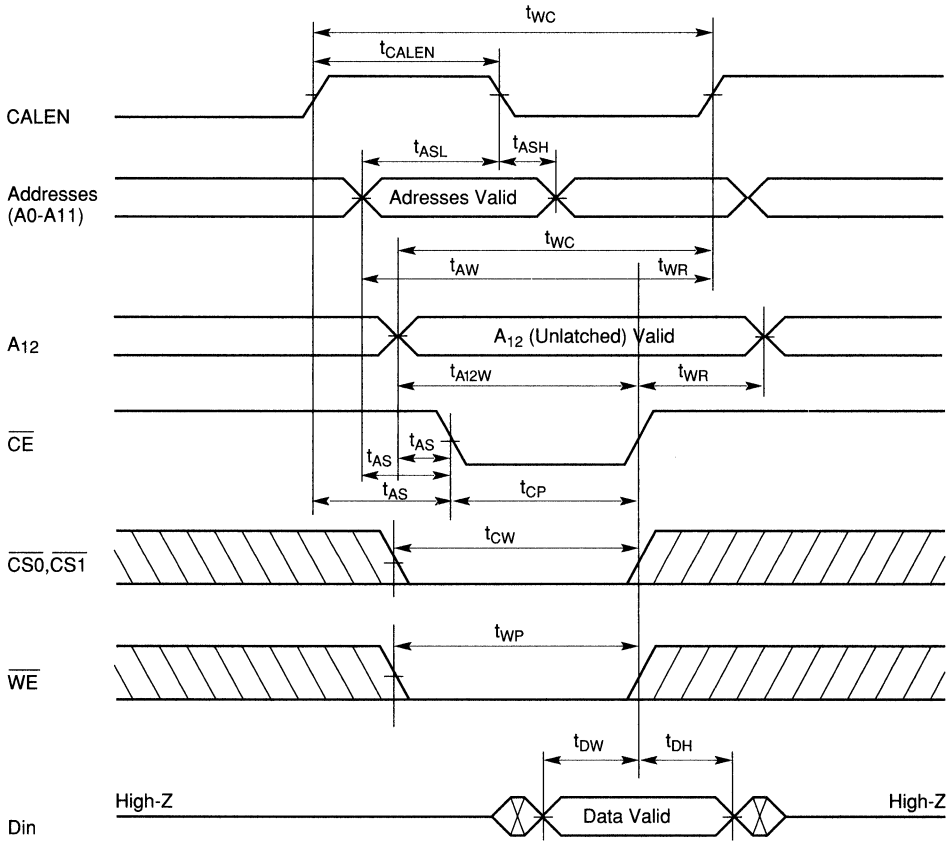
■ WRITE CYCLE

Parameter	Symbol	HM62A168/B-25 HM62A188/B-25		HM62A168-25R HM62A188-25R		HM62A168-30 HM62A188-30		HM62A168/B-35 HM62A188/B-35		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	tWC	25	—	25	—	30	—	35	—	ns	
Address Valid to End of Write	tAW	18	—	18	—	18	—	25	—	ns	1
A_{12} Valid to End of Write	tA12W	18	—	18	—	18	—	25	—	ns	
Chip Select to End of Write	tCW	18	—	18	—	18	—	25	—	ns	
Data Valid to End of Write	tDW	10	—	10	—	10	—	10	—	ns	
Data Hold from End of Write	tDH	0	—	0	—	0	—	0	—	ns	
Write Enable Active to High-Z	tWHZ	—	15	—	15	—	15	—	15	ns	5
Write Enable Inactive to Low-Z	tWLZ	3	—	3	—	3	—	3	—	ns	5
Write Pulse Width	tWP	15	—	15	—	18	—	25	—	ns	
$\overline{CE}$ Pulse Width During Chip Enable Controlled Write	tCP	15	—	15	—	18	—	25	—	ns	
Address Setup Time	tAS	0	—	0	—	0	—	0	—	ns	2
Write Recovery Time	tWR	0	—	0	—	0	—	0	—	ns	3
Address Latch Enable Pulse Width	tCALEN	8	—	8	—	8	—	10	—	ns	
Address Setup to Latch Low	tASL	4	—	4	—	4	—	6	—	ns	
Address Hold to Latch Low	tAHL	5	—	5	—	5	—	5	—	ns	
Chip Enable Low to Output Low-Z	tOLZ	2	—	2	—	2	—	2	—	ns	
Output Disable to Output Hig-Z	tOHZ	—	10	—	10	—	10	—	10	ns	

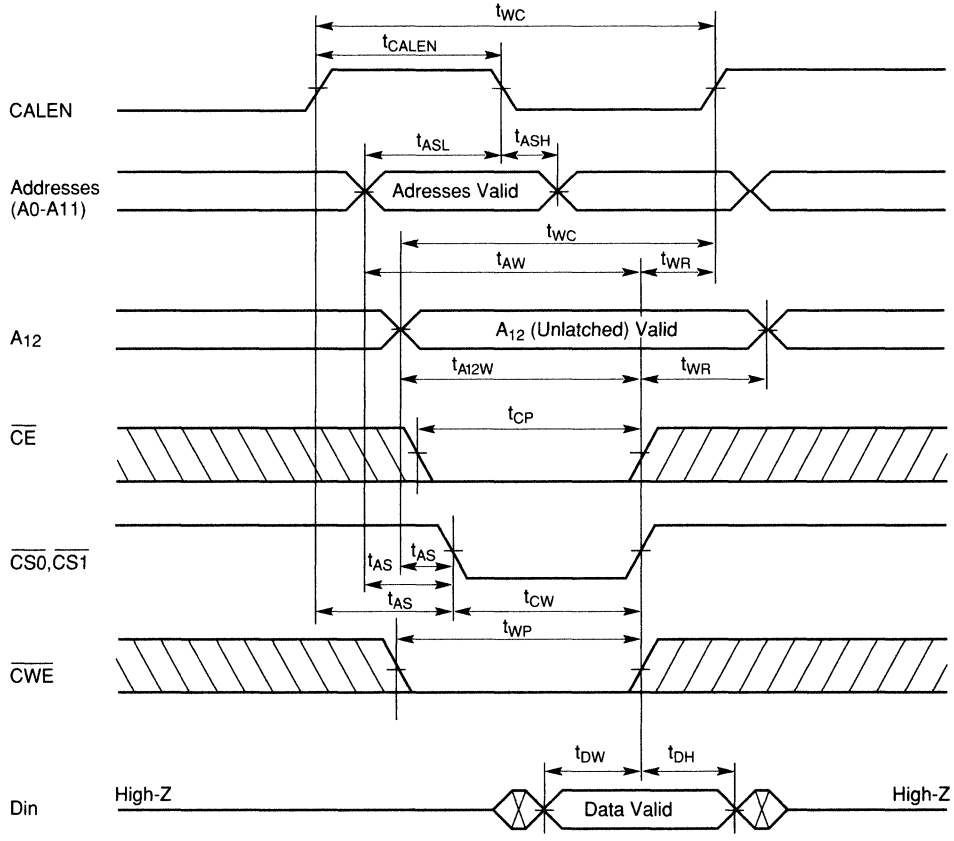
■ WRITE TIMING WAVEFORM (1) ($\overline{WE}$ Controlled)



■ WRITE TIMING WAVEFORM (2) ($\overline{COE}$ = High, $\overline{CE}$ Controlled)

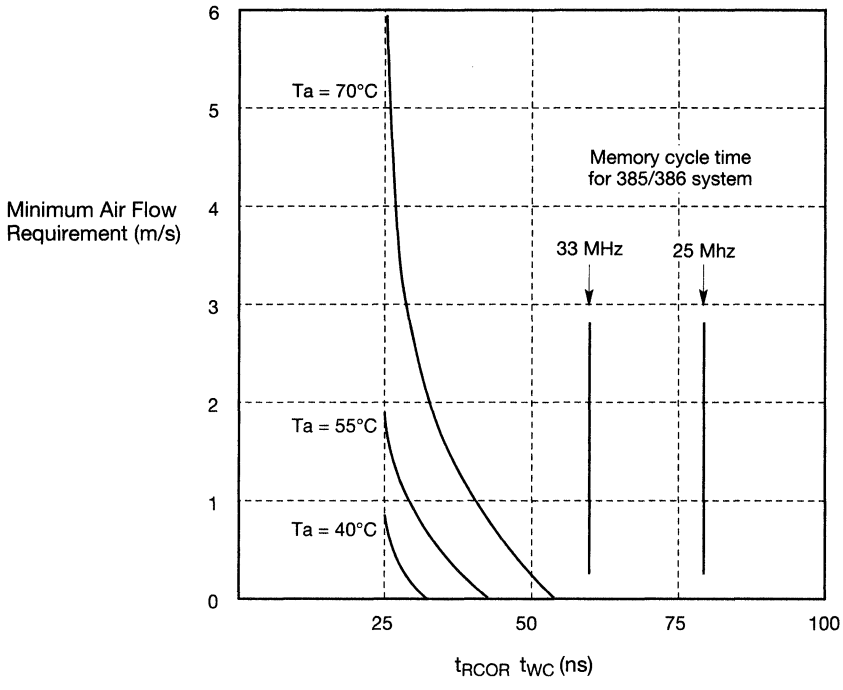


■ WRITE TIMING WAVEFORM (3) ($\overline{COE}$ = High, $\overline{CS}$ Controlled)



Notes:
1. t_{AW} is measured from the later of CALEN going high, or addresses A_0-A_{11} transition with CALEN high to the end of write cycle
2. t_{AS} is measured from the latest of CALEN going high, addresses A_0-A_{11} transition with CALEN high, or address A_{12} transition to the beginning of write cycle.
3. t_{WR} is measured from the earliest of $\overline{CS_0}$, $\overline{CS_1}$, $\overline{CE}$, or $\overline{WE}$ going high to the earlier of CALEN going high, or address A_{12} transition.
4. A write occurs during the overlap of a low $\overline{CS_0}$ or $\overline{CS_1}$, a low $\overline{CE}$, and a low $\overline{WE}$.
5. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. D_{out} is not the same phase of write data of this write cycle. Normal read cycle shall be used for write verify. This does not apply to the HM62A168B and HM62A188B.

■ AIR FLOW REQUIREMENTS



HM62A932 Series — Preliminary

32k x 9 Data Cache RAM

■ DESCRIPTION

The Hitachi HM62A932 is a high speed 288-kbit synchronous static cache RAM optimized for use in secondary caches for 32-bit microprocessor system. This RAM has a 32-kword x 9-bit organization for building a 32k x 32-bit cache data array, with byte parity by using four of these chips. The HM62A932 is available in a 44-pin PLCC for high density mounting.

■ FEATURES

- 32-kword x 9-bit organization
- Synchronous read and write
- Internal burst read/write address counter
- Self-timed write
- Matches timing of 50 MHz 32-bit micro processor
- Additional address strobe input for implementing extended burst

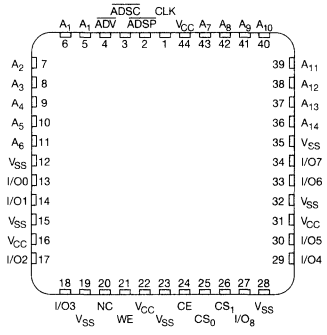
■ ORDERING INFORMATION

Type No.	Access Time	CPU Clock Rate	Package
HM62A932CP-14	14 ns	50 MHz	44-pin PLCC
HM62A932CP-19	19 ns	40 MHz	
HM62A932CP-24	24 ns	33 MHz	
HM62A932CP-34	34 ns	25 MHz	

(CP-44)

■ PIN ARRANGEMENT

HM62A932 Series



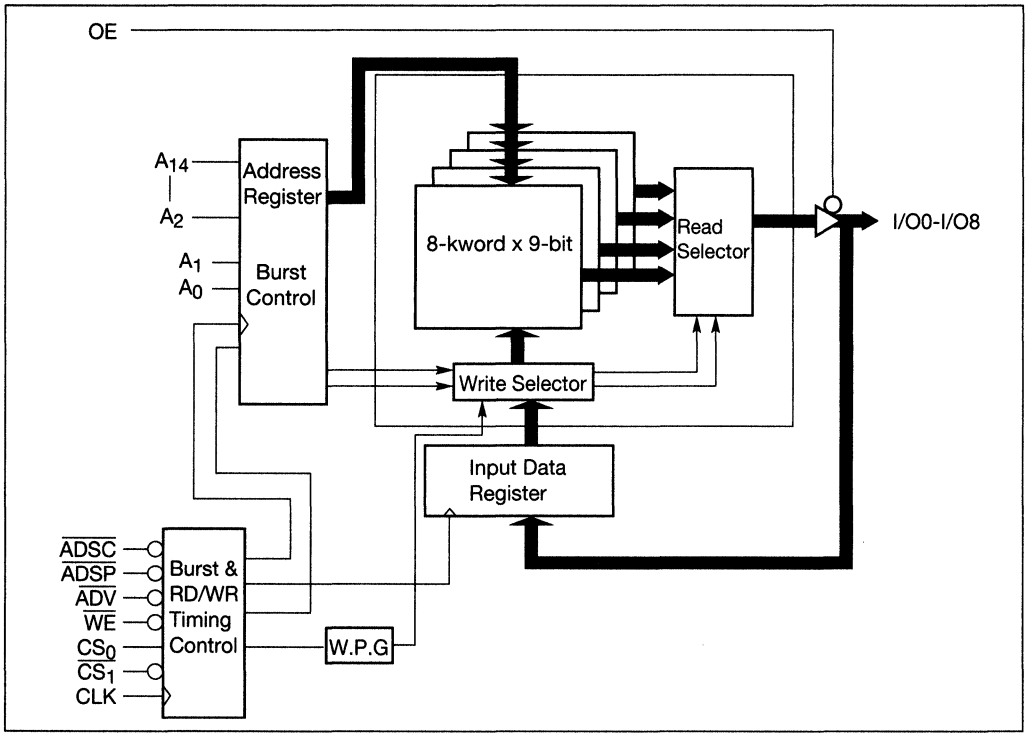
(Top View)

■ PIN DESCRIPTION

Pin Name	Function
CLK	Clock Input
$\overline{ADSP}$	Address Status Input from MPU
$\overline{ADSC}$	Address Status Input from the Cache Controller
CS_0, $\overline{CS_1}$	Complementary Chip Select Input
A_0-A_{14}	Base Address Input
$\overline{ADV}$	Synchronous Address Advance Input
$\overline{WE}$	Synchronous Write Enable Input
$\overline{OE}$	Asynchronous Data Output Enable Input
I/O_0–I/O_7, I/O_8	Input/Output Data Pin
NC	No Connection

3

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Table 1. Synchronous Operation

CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	CLK	I/O Pin	Function
X	H	X	X	X	X	↑	High-Z	Disable
L	X	X	X	X	X	↑	High-Z	Disable
H	L	L	X	X	X	↑	Output	Latch Base Address Read Address
H	L	H	L	X	L	↑	Input	Latch Base Address Sample Write Data Start a Self-Timed Write
H	L	H	L	X	H	↑	Output	Latch Base Address Read Access
H	L	H	H	L	L	↑	Input	Sample Write Data Advance Burst Count Start a Self-Timed Write
H	L	H	H	L	H	↑	Output	Advance Burst Count Read Access
H	L	H	H	H	L	↑	Input	Start a Self-Timed Write
H	L	H	H	H	H	↑	Output	Read Access

X = Don't care, H = High, L = Low, High-Z = High Impedance

Table 2. Asynchronous Output Control (See Notes 2 and 3 Below)

OE	I/O Pin
L	Output
H	High-Z

Notes:
1. Two separate address strobe inputs are provided and both will load a new base address. $\overline{ADSP}$, from the MPU will override all other functions and cause a read access to the base address. $\overline{ADSC}$, from the controller, is affected by $\overline{WE}$ if $\overline{ADSP}$ is inactive, and $\overline{ADSC}$ will start either a read or write cycle to the base address.
2. The CS_0 and $\overline{CS_1}$ inputs are sampled with the addresses when $\overline{ADSP}$ or $\overline{ADSC}$ is sampled active. Only if CS_0 and $\overline{CS_1}$ are sampled active will $\overline{WE}$ or $\overline{OE}$ affect the chip.
3. Any time $\overline{WE}$ is active when $\overline{ADSP}$ is inactive, a self-timed write will start.
4. During data read cycles, data is always presented asynchronously with clock after $\overline{OE}$ becomes low.
5. If the asynchrous $\overline{OE}$ signal is activated during a self-timed write cycle, I/O pins will be in High-Z state.
6. $\overline{OE}$ must not be driven by any controller when setting up for a write cycle, since the data collision would corrupt the write data.

3

Pin Description

CLK	Clock input signal. It samples all of the input signals except $\overline{OE}$.
$\overline{ADSP}$	Address status input signal from MPU. When activated, a new "base" address is latched and an internal read access is performed. All other synchronous inputs are ignored when it is sampled active.
$\overline{ADSC}$	Address status input signal from the cache controller. When activated, a new "base" address is latched. Used during extended burst, and write-back cases when the cache controller must tell the device what addresses to access.
CS_0, $\overline{CS_1}$	Complementary chip select input signals. These are sampled along with the addresses when $\overline{ADSP}$ or $\overline{ADSC}$ is sampled. For any read/write or data bus activity to occur, CS_0 must be sampled high and $\overline{CS_1}$ must be sampled low.
A_0, A_{14}	Base address input signals. They are sampled when $\overline{ADSP}$ or $\overline{ADSC}$ is active. A_0–A_{14} may change after $\overline{ADSP}$ or $\overline{ADSC}$ samples them. A_1 and A_0 are latched and modified by the internal burst counter which XORs the bits in a certain burst order.
$\overline{ADV}$	Address advance input signal. When $\overline{ADV}$ is sampled active, and $\overline{ADSP}$ and $\overline{ADSC}$ are both sampled inactive, $\overline{ADV}$ will increment the burst counter prior to a read or write access. If $\overline{ADV}$ and $\overline{WE}$ are sampled active, the address will be incremented before a self-timed write starts. If $\overline{ADV}$ is sampled active with $\overline{WE}$ inactive, the address will be incremented before a read access starts.
$\overline{WE}$	Write enable input signal. When $\overline{WE}$ is sampled active and $\overline{ADSP}$ is sampled inactive, a self-timed write will start. When $\overline{WE}$ is sampled inactive, a self-timed write will start. When $\overline{WE}$ is sampled inactive, a read access will start. Active $\overline{WE}$ with $\overline{ADSC}$ active will cause a write to occur.
$\overline{OE}$	Asynchronous data output enable signal input. When active, the I/O pins will be driven will be driven with the read data available inside chip. $\overline{OE}$ activated while an internal self-timed write is in progress will cause the I/O pins to be High-Z. $\overline{OE}$ must be activated while an internal self-timed write is in progress will cause the I/O pins to be High-Z. $\overline{OE}$ must be inactive with enough margin before a self-timed write is started to guarantee that no data bus contention occurs.
I/O_0, I/O_8	Input/Output data pins.

■ FUNCTIONAL DESCRIPTION

This cache RAM contains both data and address edge triggered latches to perform high speed synchronous accesses. These latches, combined with internal self-timed write logic, allow the write decision to be postponed until it is known that a write must be done.

An internal burst address counter is provided to support burst read and burst write cycles. The counter sequences through the four internal bytes on the rising edge of the clock when input is sampled active. If the device reaches end of the normal burst sequence, the counter will wrap-around to the initial base address.

The rules for handling the low order address bits during a burst sequence is shown here (the low order address bits):

Initial access:	Use base address provided with $\overline{ADSC}$ or $\overline{ADSP}$
Next burst access:	Invert only base address A_0
Next burst access:	Invert only base address A_1
Next burst access:	Invert only base address A_1–A_0
Next burst access:	Wrap-around, use initial base address

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.2	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_T min = −2.5 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10	µA	Output Disable $V_{I/O}$ = V_{SS} to V_{CC}
Active Operating Power Supply Current	I_{CC}	—	—	TBD	mA	TBD
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} =3.2 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −2.0 mA

Note: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading

■ CAPACITANCE (T_a = 25°C, f = 1 MHz)*1

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

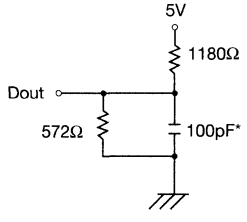
Note: 1. This parameter is sampled and not 100% tested.

3

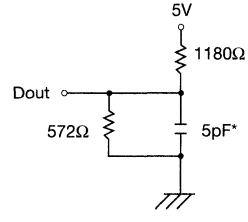
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Test Conditions

- Input and Output timing reference levels: 1.5V
- Input pulse levels: V_{SS} to 3V
- Input rise and fall times: 3ns
- Output load: See figures



Output Load (A)



Output Load (B)
(for t_{OLZ} & t_{OHZ})

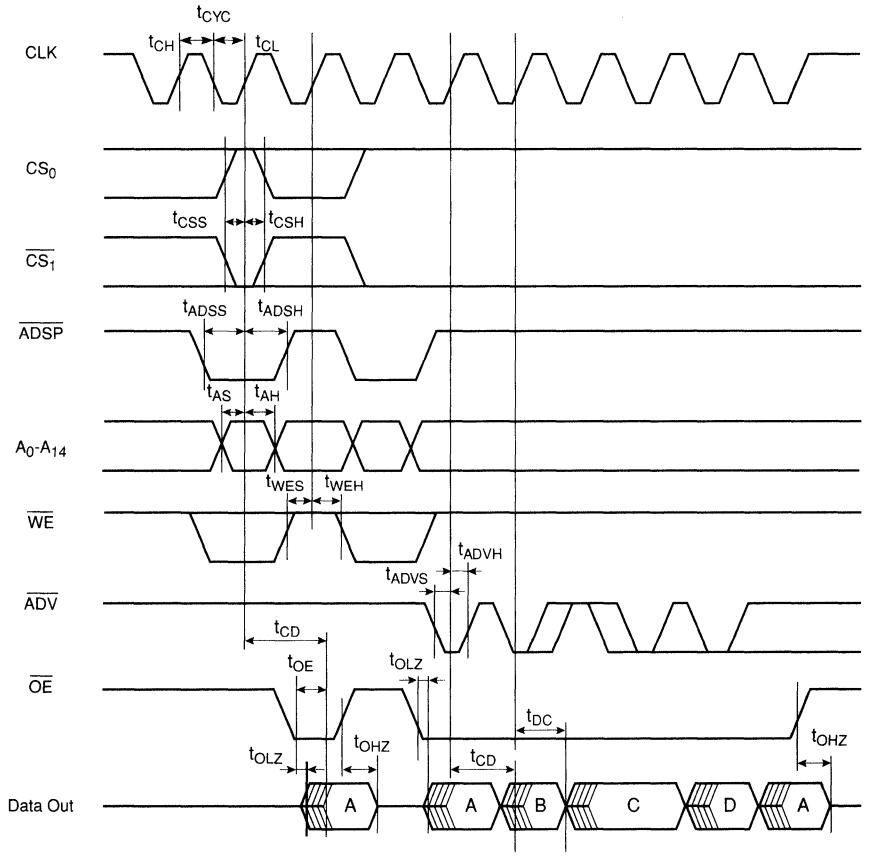
* Including scope & jig.

Parameter	Symbol	HM62A932-14		HM62A932-19		HM62A932-24		HM62A932-34		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{CYC}	20	—	25	—	30	—	40	—	ns
Clock Pulse High	t_{CH}	8	—	9.5	—	11	—	14	—	ns
Clock Pulse Low	t_{CL}	8	—	9.5	—	11	—	14	—	ns
Address Setup Time	t_{AS}	3	—	3	—	5	—	5	—	ns
ADS Setup Time	t_{ADSS}	3	—	3	—	5	—	5	—	ns
Output Select Setup Time	t_{CSS}	3	—	3	—	5	—	5	—	ns
Address Hold Time	t_{AH}	2	—	2	—	3	—	3		ns
ADS Hold Time	t_{ADSH}	2	—	2	—	3	—	3	—	ns
Chip Select Hold Time	t_{CSH}	2	—	2	—	3	—	3		ns
Input Data Setup Time	t_{DS}	3	—	3	—	5	—	5	—	ns
ADV Setup Time	t_{ADVS}	3	—	3	—	5	—	5	—	ns
Write Enable Setup Time	t_{WES}	3	—	3	—	5	—	5	—	ns
Input Data Hold Time	t_{DH}	2	—	2	—	3	—	3	—	ns
ADV Hold Time	t_{ADVH}	2	—	2	—	3	—	3	—	ns
Write Enable Hold Time	t_{WEH}	2	—	2	—	3	—	3	—	ns
Clock to Output Valid	t_{CD}	—	14	—	19	—	24	—	34	ns
Output Enable Low to Output Valid	t_{OE}	—	7	—	8	—	9	—	10	ns
Output Enable Low to Output Low-Z	t_{OLZ}*1,*2	0	—	0	—	0	—	0	—	ns
Read Data Hold After New Clock	t_{DC}	3	—	3	—	3	—	3	—	ns
Output Enable High to Output High-Z	t_{OHZ}*1,*2	—	7	—	8	—	9	—	10	ns
System Clock Skew	t_{SKEW}	—	1	—	1	—	1	—	1	ns
Frequency		50		40		33		25		MHz

Notes: 1. Transition is measured ± 200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORMS

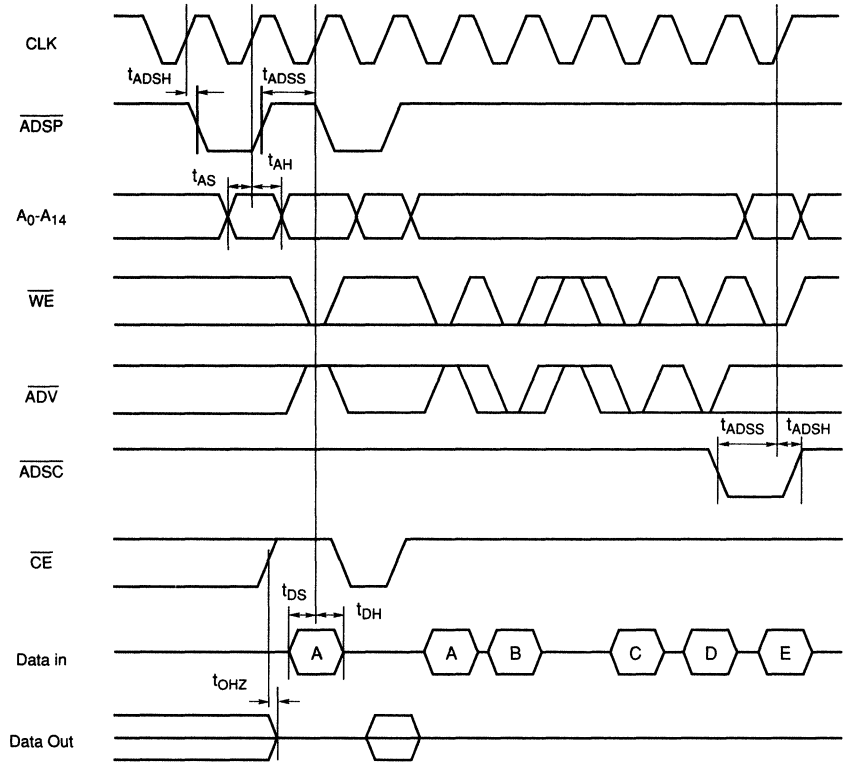
(1) Read Cycle Followed by Burst with Wait State Added to Data C



A–Data from Base ADDR
B–Data from Base ADDR except A_0 is now $\overline{A}_0$
C–Data from Base ADDR except A_1 is now $\overline{A}_1$
D–Data from Base ADDR except A_0 and $\overline{A}_1$ are now $\overline{A}_0$ and $\overline{A}_1$

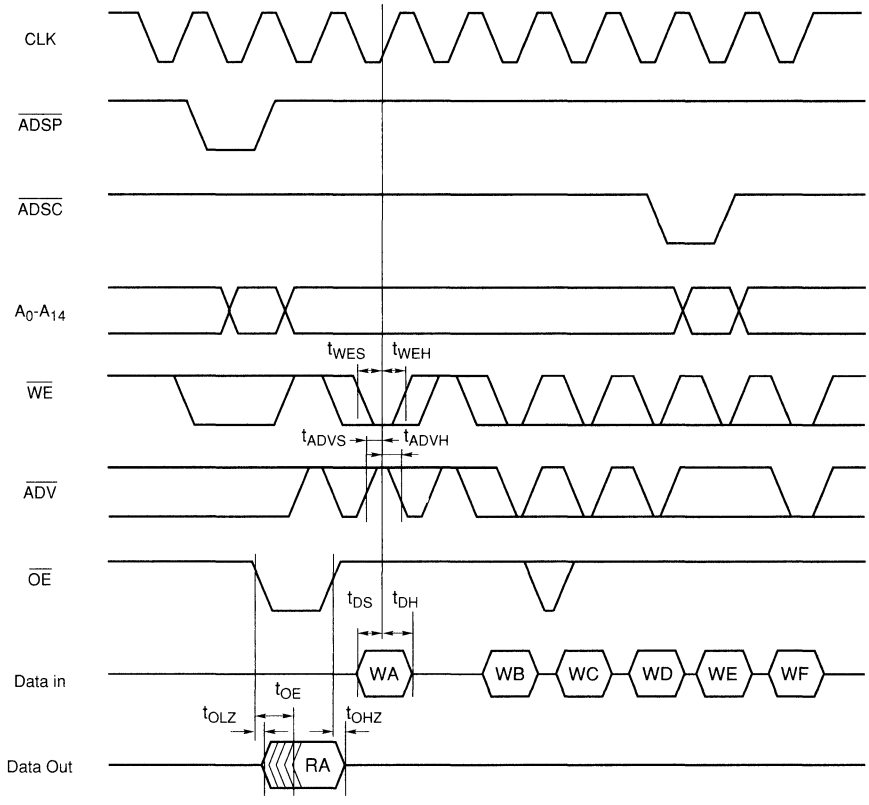
Note: 1. If $\overline{ADSP}$ or $\overline{ADSC}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.

(2) Write Cycle Followed by Burst Write with Wait State Added to Data C



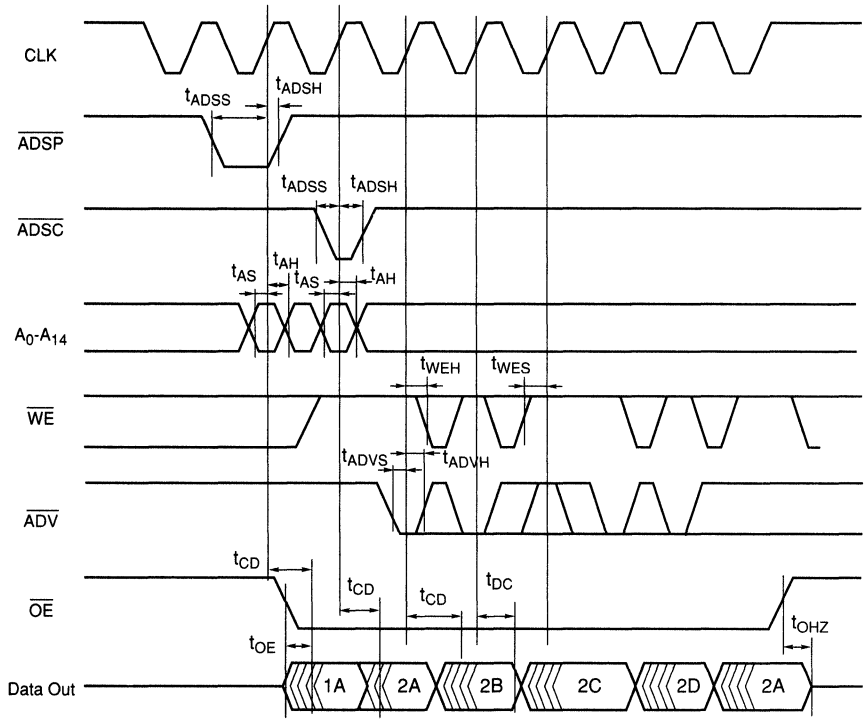
A–Data to be written to Base ADDR
B–Data to be written to Base ADDR except A_0 is now $\overline{A}_0$
C–Data to be written to Base ADDR except A_1 is now $\overline{A}_1$
D–Data to be written to Base ADDR except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$
E–Data to be written to new Base ADDR loaded by $\overline{ADSC}$

(3) Burst Mixed Read/Write Cycles



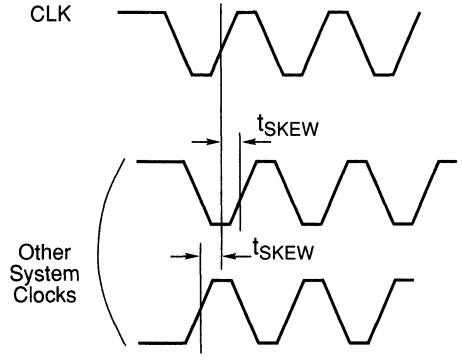
RA–Data from Base ADDR
WA–Data to be written to Base ADDR
WB–Data to be written to Base ADDR except A_0 is now $\overline{A}_0$
WC–Data to be written to Base ADDR except A_1 is now $\overline{A}_1$
WD–Data to be written to Base ADDR except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$
WE–Data to be written to new Base ADDR
WF–Data to be written to new Base ADDR except A_0 is now $\overline{A}_0$

(4) Sequencial $\overline{ADSP}$/$\overline{ADSC}$ Cycles



1A–Data from Base ADDR1
2A–Data from Base ADDR2
2B–Data from Base ADDR2 except A_0 is now $\overline{A}_0$
2C–Data from Base ADDR2 except A_1 is now $\overline{A}_1$
2D–Data from Base ADDR2 except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$

(5) System Clock Skew Requirements



For this synchronous memory to meet its system timing requirements, the system clock skew must not exceed the specified range. Larger clock skews will require smaller clock-to-access times (t_{CD}).

HM62A2016 Series

Dual 8,192-Word x 20-Bit Static Cache Memory

■ DESCRIPTION

The HM62A2016 is a high speed 327,680-bit cache memory organized as two banks of 8,192 words by 20-bits. The device includes dual address latches, dual chip select latches, data multiplexer with multiple chip enables and output enables. It can be used in a cache memory system adopting Harvard architecture which requires separate instruction and data storages.

(CP-52)

■ FEATURES

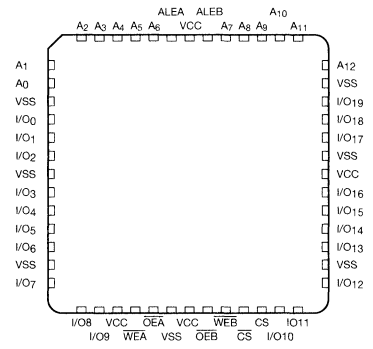
- High speed: up to 33 MHz operation
  - Address access time: 17/20/25/30 ns
  - Output enable access time: 7/7/8/8 ns
- Dual 8k x 20 memory arrays with data multiplexer
- Dual latches for address and chip select inputs
- Expandable both in width and depth
  - Two separate chip selects
- 52-pin PLCC

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62A2016CP-17	17 ns	52-pin PLCC (CP-52)
HM62A2016CP-20	20 ns	
HM62A2016CP-25	25 ns	
HM62A2016CP-30	30 ns	

■ PIN ARRANGEMENT

HM62A2016 Series



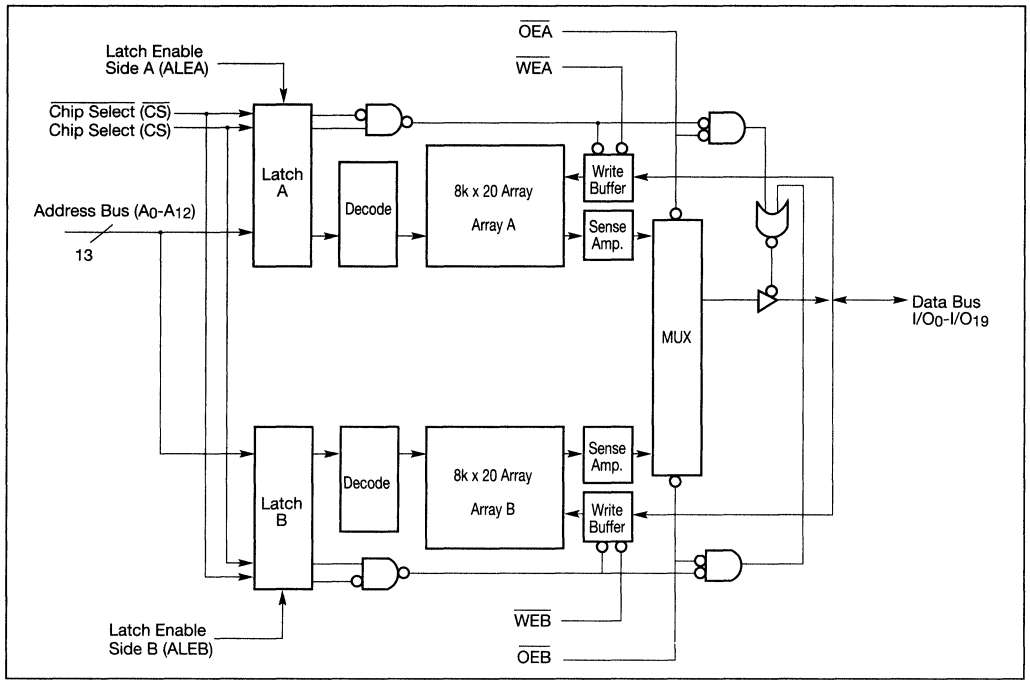
(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0-A12	Address Inputs
ALEA, ALEB	Latch Enables
$\overline{OEA}$, $\overline{OEB}$	Output Enables
$\overline{WEA}$, $\overline{WEB}$	Write Enable
I/O0-I/O19	Data Inputs Outputs
CS, $\overline{CS}$	Chip Selects

3

■ BLOCK DIAGRAM



Signal Description

Signal Name	Pin Number	Signal Description
A0-A12	3–9 46–51	Shared address inputs to both Memory Array A and Memory Array B. Current A_0–A_{12} values are latched into Latch A or Latch B by the falling edge of ALEA or ALEB.
ALEA, ALEB	2, 52	Latch enable inputs. When ALEA or ALEB is high, Latch A or Latch B is transparent to address and chip select input values. The falling edge of ALEA and ALEB latches current inputs at A_0–A_{12} and current states of CS and $\overline{CS}$. These latched values remain applied to the respective memory arrays until ALEA or ALEB transition to a high state.
$\overline{CS}$, CS	30, 31	Active low and active high chip select inputs. The current states of CS and $\overline{CS}$ are latched by the falling edge of ALEA and ALEB. When $\overline{CS}$ is low and CS is high read and write access to both arrays is possible. $\overline{CS}$ should be grounded and CS should be tied to V_{CC} in applications where no device depth expansion takes place. See the Depth Expansion Section for a detailed description of the chip select function.
$\overline{WEA}$, $\overline{WEB}$	24, 29	Active low write enable inputs. $\overline{WEA}$ controls writing into Array A and $\overline{WEB}$ controls writing into Array B. Both $\overline{WEA}$ and $\overline{WEB}$ must not be both low simultaneously.
$\overline{OEA}$, $\overline{OEB}$	25, 28	Active low output enable inputs. $\overline{OEA}$ and $\overline{OEB}$ are used to control driving of stored data from Array A or Array B onto the I/O lines during read operations. $\overline{OEA}$ and $\overline{OEB}$ must not be both low simultaneously.
I/O_0, I/O_{19}	11–13, 15–18 20–22, 32–34, 36–39, 42–44	Data inputs and outputs. These are three-state lines that provide data access to both memory arrays.

3

■ FUNCTION TABLE

CS	$\overline{CS}$	ALEA	ALEB	$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	Operation	I/O Status
L	X	*1	*1	X	X	X	X	Not Selected	Outputs High-Z
X	H	*1	*1	X	X	X	X	Not Selected	Outputs High-Z
H	L	X	X	H	H	H	H	Data I/O's Disabled	Outputs High-Z
H	L	H	X	H	H	L	H	Read from Array A (Current Addresses)	Data Out
H	L	L	X	H	H	L	H	Read from Array A (Latched Addresses)	Data Out
H	L	X	H	H	H	H	L	Read from Array B (Current Addresses)	Data Out
H	L	X	L	H	H	H	L	Read from Array B (Latched Addresses)	Data Out
H	L	X	X	X	X	L*2	L*2	Not Allowed in Same Phase	—
H	L	H	X	L	H	H	H	Write to Array A (Current Addresses)	Data In
H	L	L	X	L	H	H	H	Write to Array A (Latched Addresses)	Data In
H	L	X	X	L*3	H	L*3	H	Not Allowed in Same Phase	—
H	L	X	X	L*4	H	H	L*4	Not Allowed in Same Phase	—
H	L	X	H	H	L	H	H	Write to Array B (Current Addresses)	Data In
H	L	X	L	H	L	H	H	Write to Array B (Latched Addresses)	Data In
H	L	X	X	H	L*4	L*4	H	Not Allowed in Same Phase	—
H	L	X	X	H	L*3	H	L*3	Not Allowed in Same Phase	—
H	L	X	X	L*5	L*5	X	X	Not Allowed in Same Phase	—

X = Don't care, H = High, L = Low, High-Z = High Impedance

Notes: 1. CS and CS values shown in the table must have propagated through transparent latches and meet specified chip select setup times before a deselect operation can occur.
2. If data are read simultaneously from both arrays, an undefined data outputs. Specified AC and DC parameters are not guaranteed in this state.
3. Simultaneous reading and writing of a single array or of both arrays is not permitted.
4. Simultaneous reading from one array while writing to the other array is not possible.
5. Simultaneous writing to both arrays is not permitted during normal R3000 based cache operation.

■ FUNCTIONAL DESCRIPTION

The HM62A2016 is a highly-integrated memory device with several performance-enhancing features which allow direct interfacing to a MIPS R3000 or R3000A RISC processor. Two independent address latches, with fast setup times, are provided on-chip to allow faster addressing of two 8k x 20 memory arrays, Array A and Array B. Address inputs and data I/O lines are shared between the two arrays.

Two sets of $\overline{OE}$ and $\overline{WE}$ inputs, coupled with an on-board multiplexer control read and write access to each of the arrays. Integrating a 2:1 output data multiplexer on-chip reduces the problem of data bus contention that may occur when using discrete SRAMs and multiplexers, and allows easier synchronization of output enable signals.

$\overline{OEA}$ and $\overline{OEB}$ inputs directly control the driving of stored data at the outputs of the HM62A2016 during read operations. Fast (7 ns) output enable and disable times are matched and permit data to be quickly taken off the data bus as well as driven on. This high level of device feature integration demonstrated by the HM62A2016 allows construction of a dual 32-kbyte cache memory subsystem by combining only three devices together to reach the full 60-bit tag plus data width requirements of the MIPS R3000(a) processor.

The HM62A2016 is designed to permit storage and retrieval of tag address and cache data information to and from the two memory arrays in a direct-mapped, split data/instruction cache format. It is functionally compatible to and meets all MIPS R3000(A) cache memory timing requirements. The HM62A2016 fully supports "pipelined" reads and writes, as described below.

Valid addresses that appear at A_0—A_{12} inputs are recognized by on-chip Latches A or B when they are transparent (i.e. when ALEA or ALEB inputs are high). Current address input values are latched by the falling edge of ALEA and ALEB.

For an R3000(A) to HM62A2016 cache interface, addresses are latched during the first phase of a 2-phase read operation cycle, and valid data appears at outputs (I/O_0–I/O_{19}) during the second phase. These addresses will remain latched and applied to Array A or Array B as long as ALEA or ALEB remains low. Similarly, for a write operation, valid addresses are also latched during the first phase, while data is actually written into the addressed location during the second phase.

These sequential reads occur in a pipe-lined manner, where data or instructions are read from one array during the same phase when addresses for a subsequent read from the other array are latched. Similarly, alternating consecutive writes to the two memory arrays are possible as long as the minimum 2-phase write operation cycle is met with correct timings.

A write operation to a memory array can occur in the phase that immediately precedes or follows a read operation from the other array.

It is not possible to write to or read from both arrays at the same time. Nor is it possible to do more than one read or write per phase. It is not possible to read from or write to the same array in consecutive phases because of the minimum 2-phase read/write operation cycle requirements. See the Function Table for a detailed listing of prohibited operations, as well as legitimate read and write modes.

Array A and B are interchangeable and can arbitrarily be designated as for data or instruction storage.

Depth Expansion

Overview

Each HM62A2016 has a latched active high chip select input (CS) as well as an active low input ($\overline{CS}$). Depth expansion is achieved by connecting address line (A_{13}) into CS and $\overline{CS}$ inputs of two HM62A2016's and grounding or tying to V_{CC} the other remaining chip select of each device, as shown in figure 1. Corresponding (A or B) control inputs ($\overline{OE}$, $\overline{WE}$, and ALE) of depth-expanded HM62A2016's should be tied together.

The latched chip select function of the HM62A2016 is designed to permit one array to be latched "on" (active for read or write access) while the other corresponding array of a different davice is turned "off".

Detailed Description

The current states of CS and $\overline{CS}$ are latched on-chip by the falling edge of ALEA or ALEB. An "array select" state (both CS = 1 and $\overline{CS}$ = 0), that passes through a single transparent Latch (A or B) and meets t_{CSL} timing, will permit that particular array (A or B) to be active for read and write access. An array in a selected state will remain active as long as its ALE input remains low. If an array select state is recognized by both transparent latches (A and B), then both arrays for that HM62A2016 device will be active.

A "deselect" state (either $\overline{CS}$ = 0 or CS = 1) that propagates through a single transparent latch (A or B) and meets the minimum specified chip select setup time will disable both read and write access to that respective array (Array A or Array B). If a deselecting input state passes through both transparent latches A and B, then read and write access to both arrays is disabled.

Example

An example of consecutive reads from two depth-expanded HM62A2016's is shown in Read Cycle No. 2. In the first phase, an instruction is read from the I-cache of the "low RAM". At the beginning of this phase, A_{13} transitions from low to high and causes the selection of the D-cache array of the "high RAM" for a read operation in the following phase. This high A_{13} state also deselects the D-cache array of the "low RAM" for the following phase.

Consecutive operations are possible because the latching of A_{13} to select or deselect an array can occur in the same phase as a read or write operation from another array of a different HM62A2016.

As a further example, the timings for a depth-expanded store-load sequence are shown in Write Cycle No. 2.

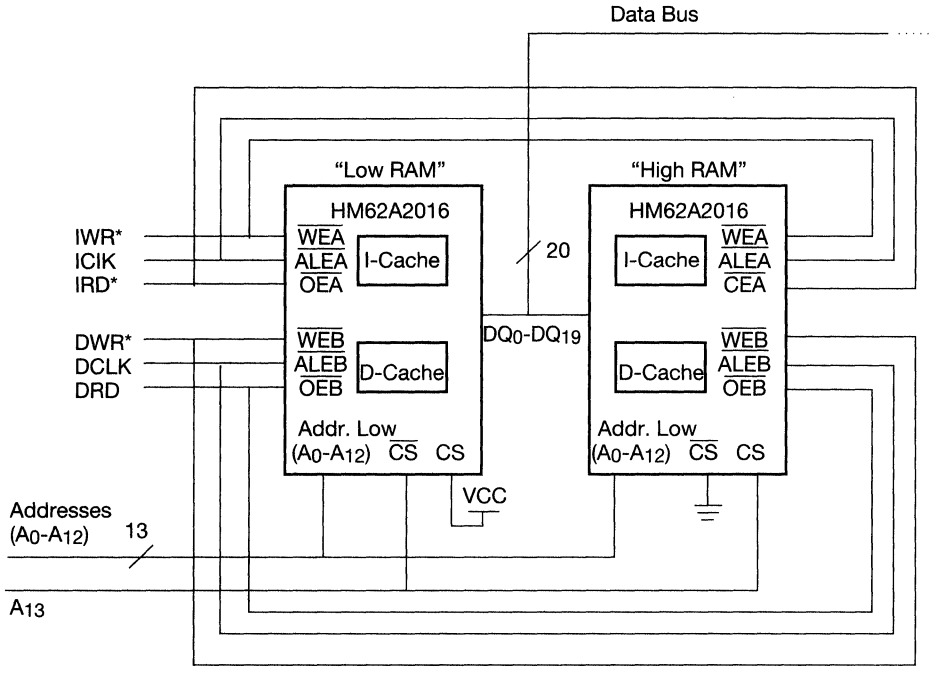


Figure 1. 16k x 20 x 2 Cache SRAM from two 8K x 20 x 2 Cache SRAMs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage relative to V_{SS}	V_{CC}	-0.5^{*1} to +7.0	V
Voltage on any pin relative to V_{SS}	V_{in}	-0.5^{*1} to V_{CC} +0.3	V
Power Dissipation	P_T	2.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_{in} min = −2.5 V for pulse width 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5^{*1}	—	0.8	V

Note: 1. V_{IL} min = −2.0V for pulse width 10 ns.
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	µA	Output Disable $V_{I/O}$ = V_{SS} to V_{CC}
Active Operating Power Supply Current	I_{CC}	—	—	220	mA	V_{in} = V_{SS} to V_{CC}, Outputs Open Load, I_{out} = 0 mA, t_{cycle} = Min. Cycle, $\overline{CS}$ = V_{IL} Max., CS = V_{IH} Min.
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} =8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA

Note: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading

■ CAPACITANCE (T_a = 25°C, f= 1 MHz.)*1

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

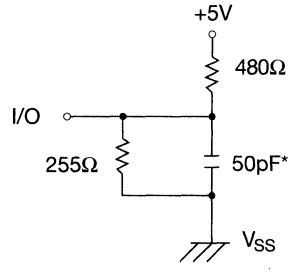
Note: 1. This parameter is sampled and not 100% tested.

3

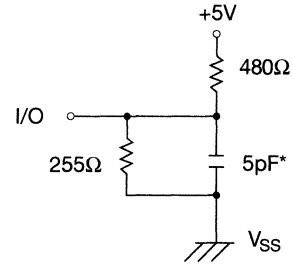
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = to 70°C, exceeding minimum air flow requirement)

Test Conditions

- Input and Output timing reference levels: 1.5V
- Input pulse levels: V_{SS} to 3V
- Output load: See figures



Output Load (A)
*Including scope & jig.



Output Load (B)
(for t_{OLZ} & t_{OHZ})

■ READ CYCLE

Parameter	Frequency / Symbol	33 MHz HM62A2016-17		25 MHz HM62A2016-20		20 MHz HM62A2016-25		16.67 MHz HM62A2016-30		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17	—	20	—	25	—	30	—	ns
Address Valid to Output Valid	t_{AA}	—	17	—	20	—	25	—	30	ns
Chip Select Access Time	t_{ACS}*1	—	17	—	20	—	25	—	30	ns
Output Enable Low to Output Valid	t_{OE}	—	7	—	7	—	8	—	8	ns
Output Enable Low to Output Low-Z	t_{OLZ}	1	—	2	—	2	—	2	—	ns
Output Enable High to Output High-Z	t_{OHZ}	0	7	0	7	0	8	0	8	ns
Output Hold from Latch Enable	t_{LOH}	3	—	3	—	3	—	3	—	ns
Address Setup to Latch Enable Low	t_{ASL}	5	—	5	—	5	—	5	—	ns
Address Hold from Latch Enable Low	t_{AHL}	2	—	2	—	2	—	2	—	ns
Chip Select Setup to Latch Enable Low	t_{CSL}*1	5	—	5	—	5	—	5	—	ns
Chip Select Hold from Latch Enable Low	t_{CSH}*1	2	—	2	—	2	—	2	—	ns
Output Enable Separation Time	t_{OSP}	2	—	2	—	2	—	2	—	ns
Latch High to Address Valid	t_{LAV}	3	—	3	—	3	—	3	—	ns

Note: 1. Indicates depth expansion parameter only. These parameters apply for both CS and $\overline{CS}$.

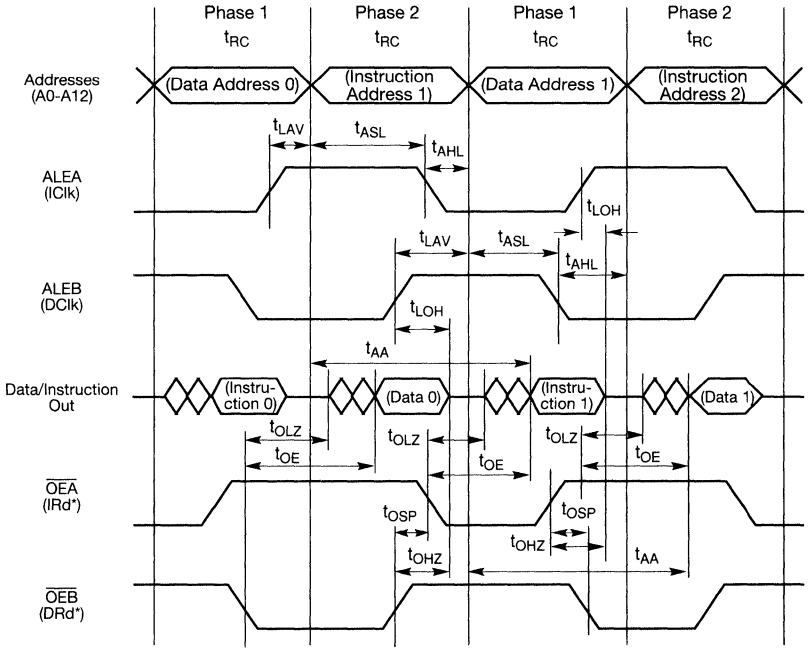
■ WRITE CYCLE

Parameter	Frequency	33 MHz		25 MHz		20 MHz		16.67 MHz		Unit
	Symbol	HM62A2016-17		HM62A2016-20		HM62A2016-25		HM62A2016-30		
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17	—	20	—	25	—	30	—	ns
Address Valid to End of Write	t_{AW}	12	—	15	—	20	—	25	—	ns
Data Valid to End of Write	t_{DS}	6	—	8	—	8	—	10	—	ns
Data Hold from End of Write	t_{DH}	0	—	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	10	—	15	—	17	—	22	—	ns
Chip Enable to End of Write	t_{CW}*1	12	—	15	—	20	—	25	—	ns
Address Setup Time Before Write Start	t_{AS}	0	—	0	—	0	—	0	—	ns
Latch Enable Hold from End of Write	t_{WHL}	0	—	0	—	0	—	0	—	ns
Address Setup to Latch Enable Low	t_{ASL}	5	—	5	—	5	—	5	—	ns
Address Hold from Latch Enable Low	t_{AHL}	2	—	2	—	2	—	2	—	ns
Chip Select Setup to Latch Enable Low	t_{CSL}*1	5	—	5	—	5	—	5	—	ns
Chip Select Hold from Latch Enable Low	t_{CSH}*1	2	—	2	—	2	—	2	—	ns
Read/Write Separation Time	t_{RWS}	2	—	2	—	2	—	2	—	ns
Latch High to Address Valid	t_{LAV}	3	—	3	—	3	—	3	—	ns

Note: 1. Indicates depth expansion parameter only. These parameters apply for both CS and $\overline{CS}$.

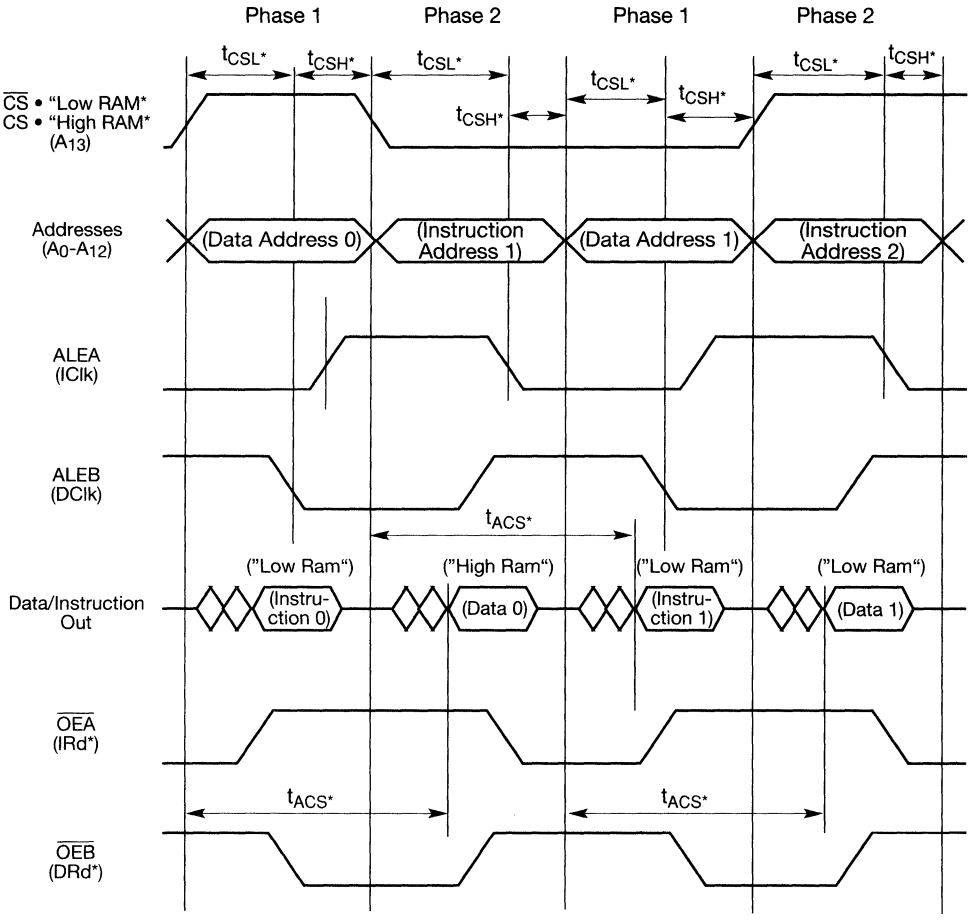
■ TIMING WAVEFORMS

Read Cycle No. 1 ($\overline{CS}$ = Low, CS, $\overline{WEA}$, $\overline{WEB}$ = High)



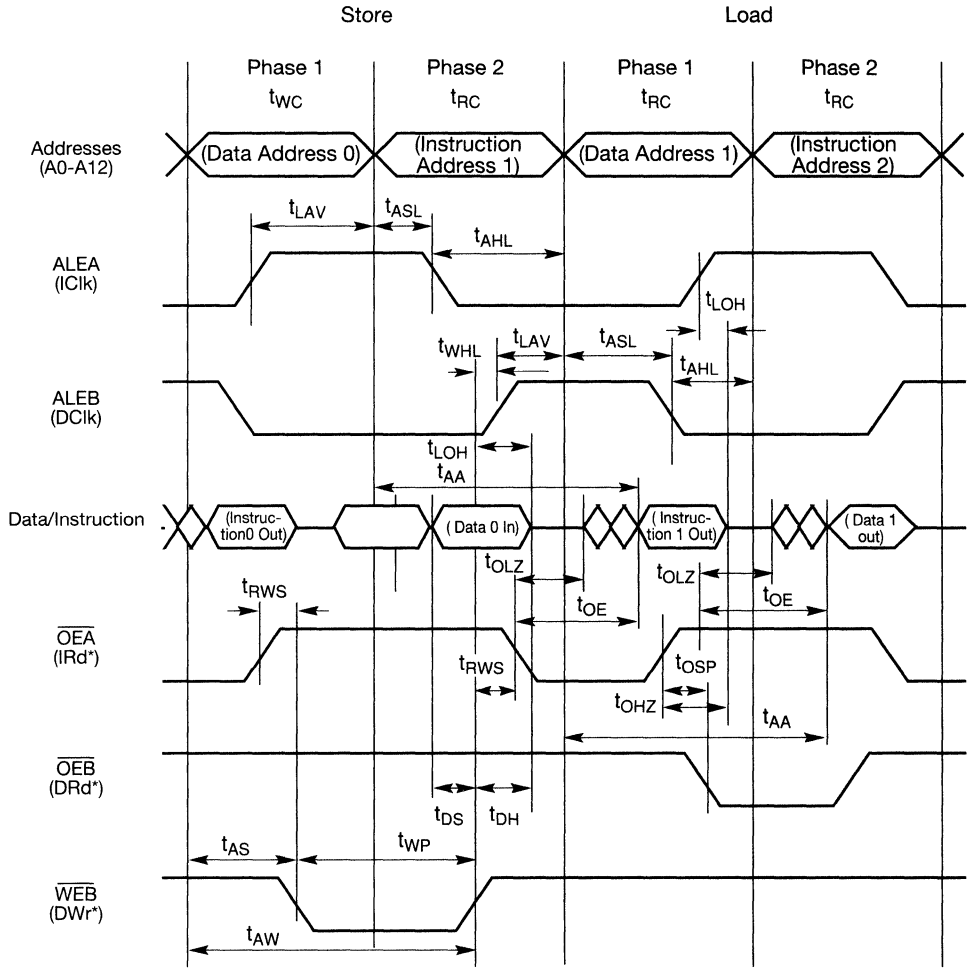
Notes:
1. All timing parameters are measured with output Load A unless otherwise noted.
2. Read cycle time (t_{RC}) refers to read operations with current addresses applied to a transparent (high) latch. Read timing parameters are referenced from the last valid address to the first transition address.
3. Transition is measured ±200 mV from steady state voltage with output Load B for t_{OLZ} and t_{OHZ} These parameters are sampled and not 100% tested.

Read Cycle No. 2 ($\overline{WEA}$, $\overline{WEB}$ = High) (Consecutive Reads from Two Depth-Expanded HM62A2016's)



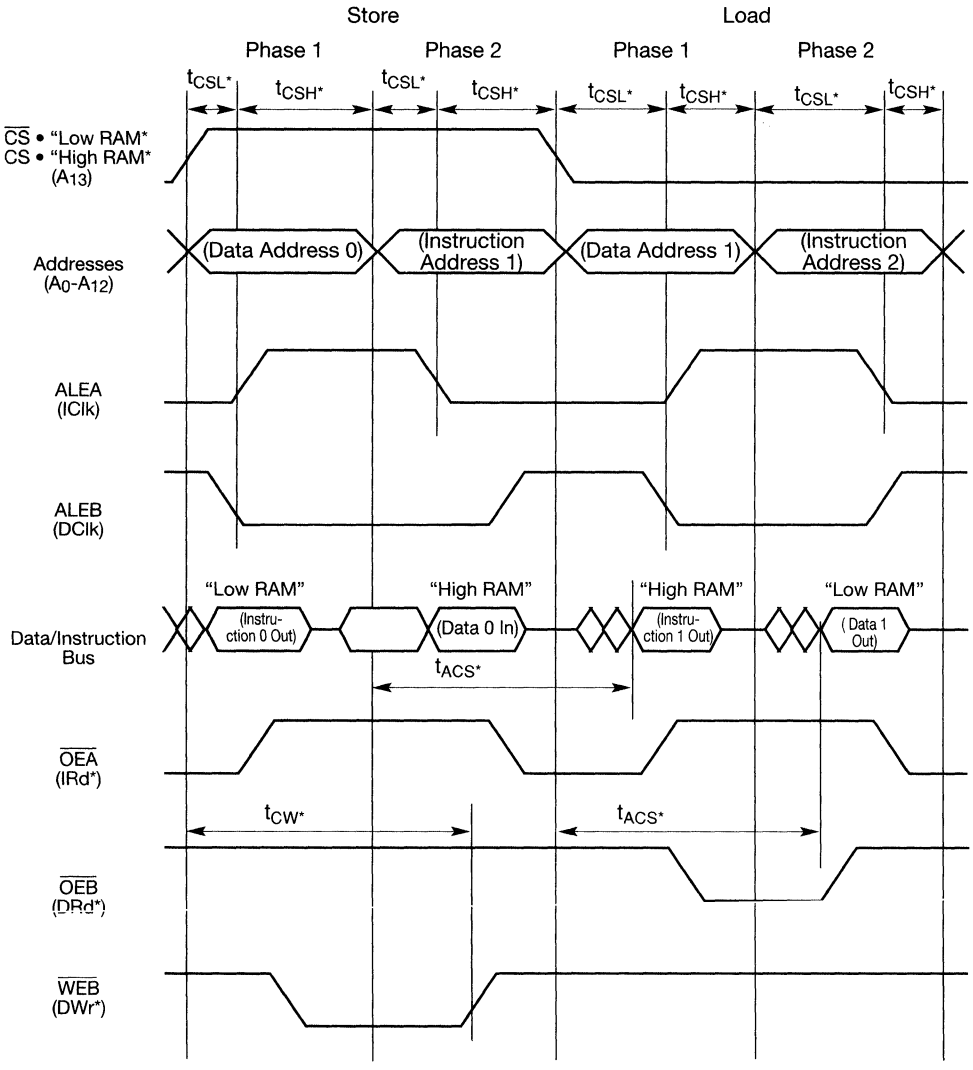
Note: 1. All other non depth-expansion parameters shown in Read Cycle No. 1 still apply, and are not shown for simplicity.

Write Cycle No. 1 ($\overline{CS}$ = Low, CS, $\overline{WEA}$ = High)



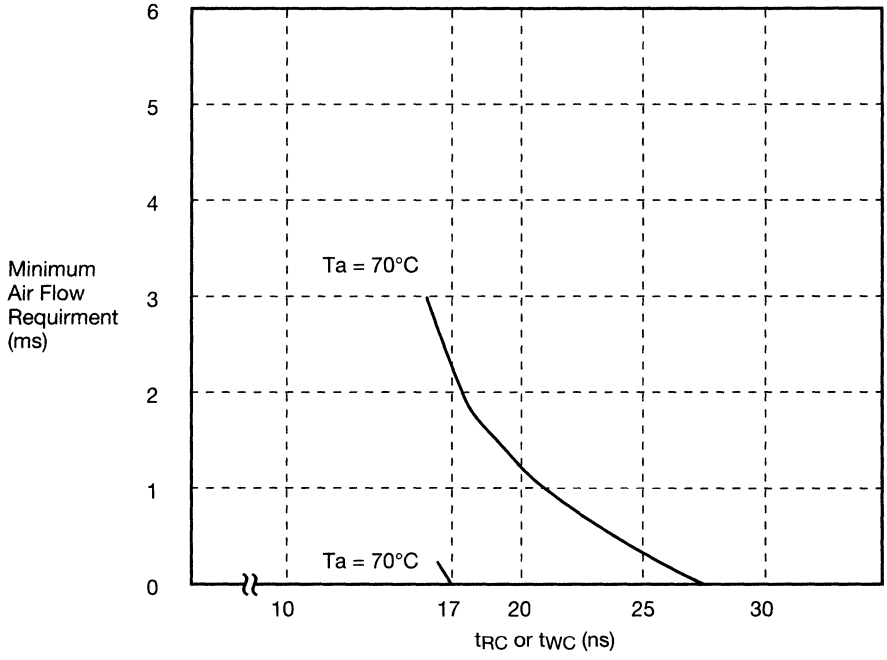
Notes:
1. All timing parameters are measured with output Load A unless otherwise noted.
2. Write cycle time refers to write operations with current addresses applied to a transparent (high) latch.
3. Transition is measured ± 200 mV from steady state voltage with output Load B for t_{OLZ} and t_{OHZ}. These parameters are sampled and not 100% tested.

Write Cycle No. 2 ($\overline{WEA}$ = High) (Store-Load Sequence of Two Depth-Expanded HM62A2016's)



Note: 1. All other non depth-expansion parameters shown in Write Cycle No. 1 still apply, and are not shown for simplicity.

Air Flow Requirements



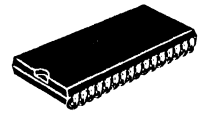
3

HM62A9128/8128 Series — Preliminary

131,072-Word x 9(8)-Bit Synchronous Cache SRAM

■ FEATURES

- For high speed cache memory applications
- Pipeline access capability with on-chip address, strobe and I/O registers
- Organization: 128 kword x 9(8) bit
- SOJ: 32-pin
- TTL I/O



(CP-32D)

■ MAIN CHARACTERISTICS

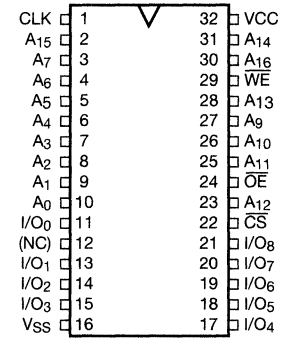
Type No.	Spec.	Remarks
Clock Cycle Time	20 ns (min)	
Clock to Data Valid	10 ns (max)	
Power Dissipation	788 mW (max)	50 MHz

■ ORDERING INFORMATION

Type No.	Clock Cycle Time	Package
HM62A9128JP-20	20 ns	32-pin SOJ 400 mil. (CP-32D)
HM62A8128JP-20	20 ns	

■ PIN ARRANGEMENT

HM62A9128/8128 Series

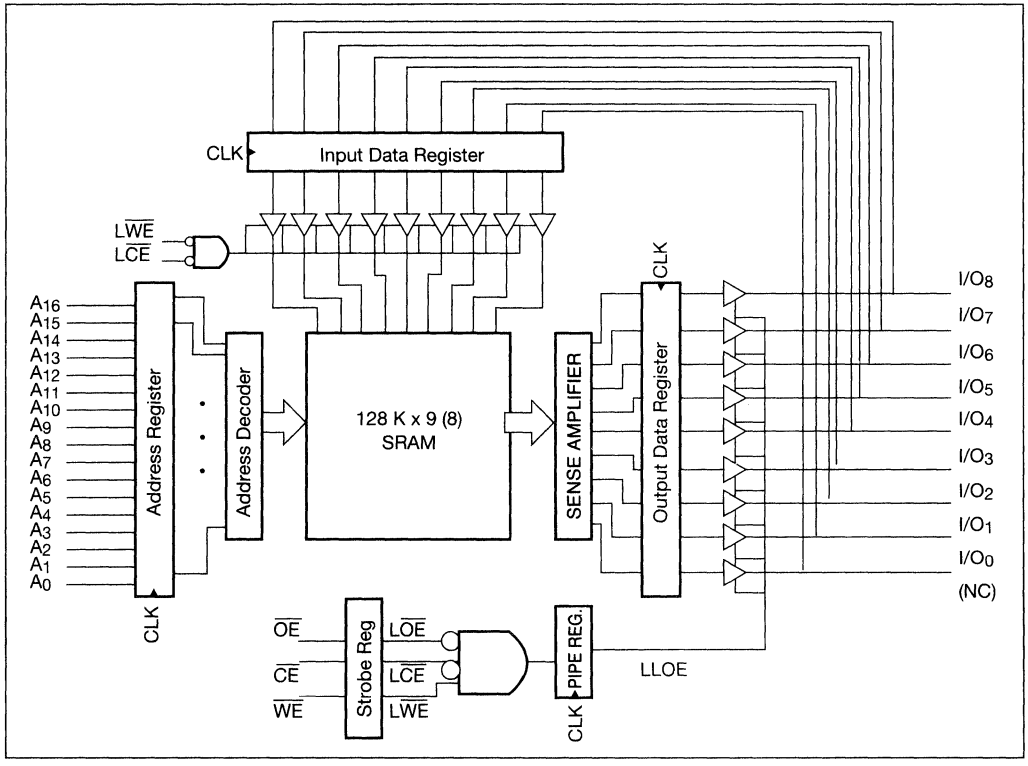


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0-A12	Address
I/O0–I/O8	Input/Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
CLK	Clock Input
VCC	Power Supply
VSS	Ground
NC	No Connection (for x 8)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	D_{in}	CLK	SRAM Mode	Next Cycle D_{out}	Ref. Cycle	Note
H	X	X	X	↗	Not Selected	High-Z	Read Cycle	
L	H	H	X	↗	Not Selected	High-Z		
L	L	H	X	↗	Read	Read Data	Read Cycle	
L	H	L	Data	↗	Write	High-Z	Write Cycle	
L	L	L	Data	↗	Write	High-Z		

Registers

CLK	Mode	Register Output
↗	Load	Register Input
L or H	Hold	Not Changed

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with Bias)	$T_{stg\ (bias)}$	–10 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ	Max.	Unit	Note
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
	V_{SS}	0	0	0	V	
Input Voltage	V_{IH}	2.2	—	6.0	V	
	V_{IL}	–0.5	—	0.8	V	1

Note: 1. V_{IL} min = –2.0V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Item	Symbol	Min.	Typ	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = 5.25V, V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10	µA	D_{out} High-Z State $V_{I/O}$ = V_{SS} to V_{CC}
Average Operating Current	I_{CC1}	—	—	150	mA	Min. Cycle, $\overline{CE}$ = V_{IL} Duty: 100%, $I_{I/O}$ = 0 mA
Standby Power Supply Current	I_{SB}	—	—	50	mA	Power Standby CLK ≤ V_{IL}, Min. Cycle
	I_{SB1}	—	—	5	mA	Power Standby CLK ≤ 0.2VV_{IL}, V_{in}, ≤ 0.2V or V_{in} ≥ V_{CC} –0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} =8.0 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

■ CAPACITANCE (T_a = 25°C, f= 1.0 MHz)

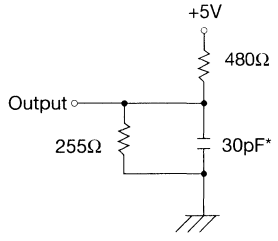
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

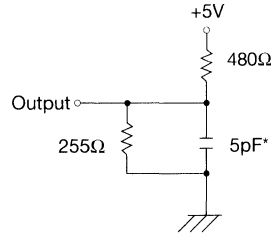
■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%)

Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 2ns
- Input and output timing reference levels: 1.5V
- Output Load: See figure



Output Load (A)
*Including scope & jig Capacitance



Output Load (B)
(for t_{HZ} & t_{LZ})

■ READ AND WRITE CYCLE

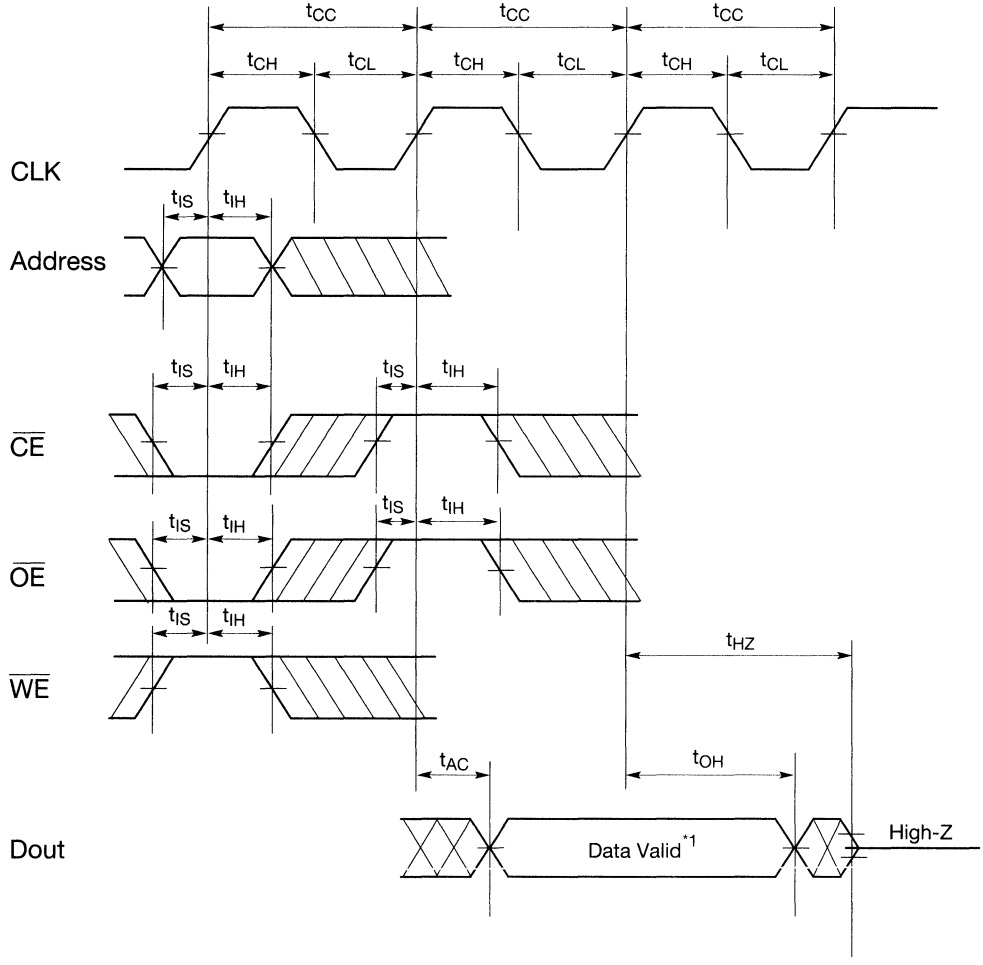
Item	Symbol	Min.	Max.	Unit	Note
Clock Cycle Time	t_{CC}	20	—	ns	
Clock High Pulse Width	t_{CH}	5	—	ns	
Clock Low Pulse Width	t_{CL}	5	—	ns	
Input Setup Time (Address, Data, Strobes)	t_{IS}	3	—	ns	
Input Hold Time (Address, Data, Strobes)	t_{IH}	1	—	ns	
Clock to Output Data Valid	t_{AC}	—	10	ns	
Output Data Hold From Clock	t_{OH}	2	—	ns	
Clock to Output in Low-Z	t_{LZ}	0	—	ns	1, 2
Clock to Output in High-Z	t_{HZ}	—	10	ns	1, 2

Notes: 1. Transition is measured ± 200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.

3

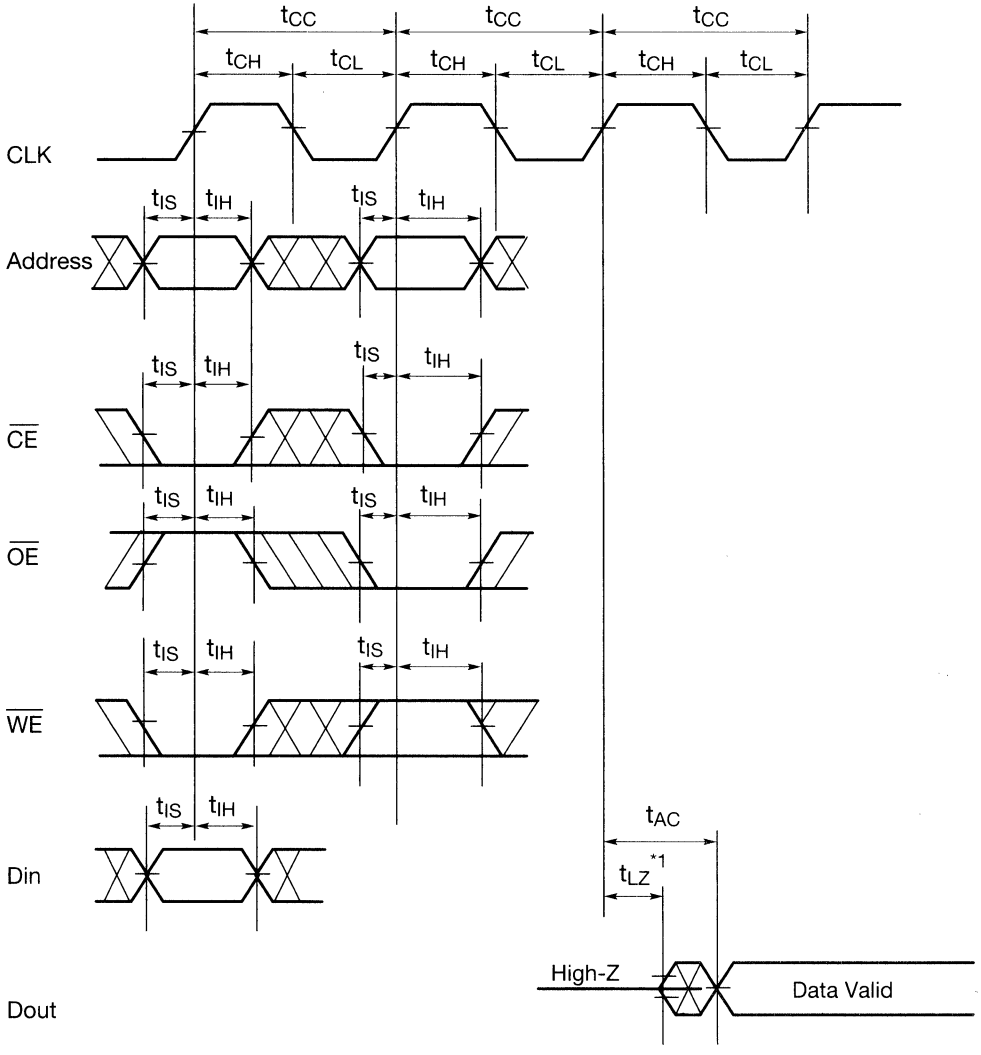
■ TIMING WAVEFORMS

Read Cycle



Notes: 1. Read data is valid on next cycle.
2. High impedance state is obtained on next cycle from $\overline{CE}$ = H, $\overline{OE}$ = H, or $\overline{WE}$ = L.

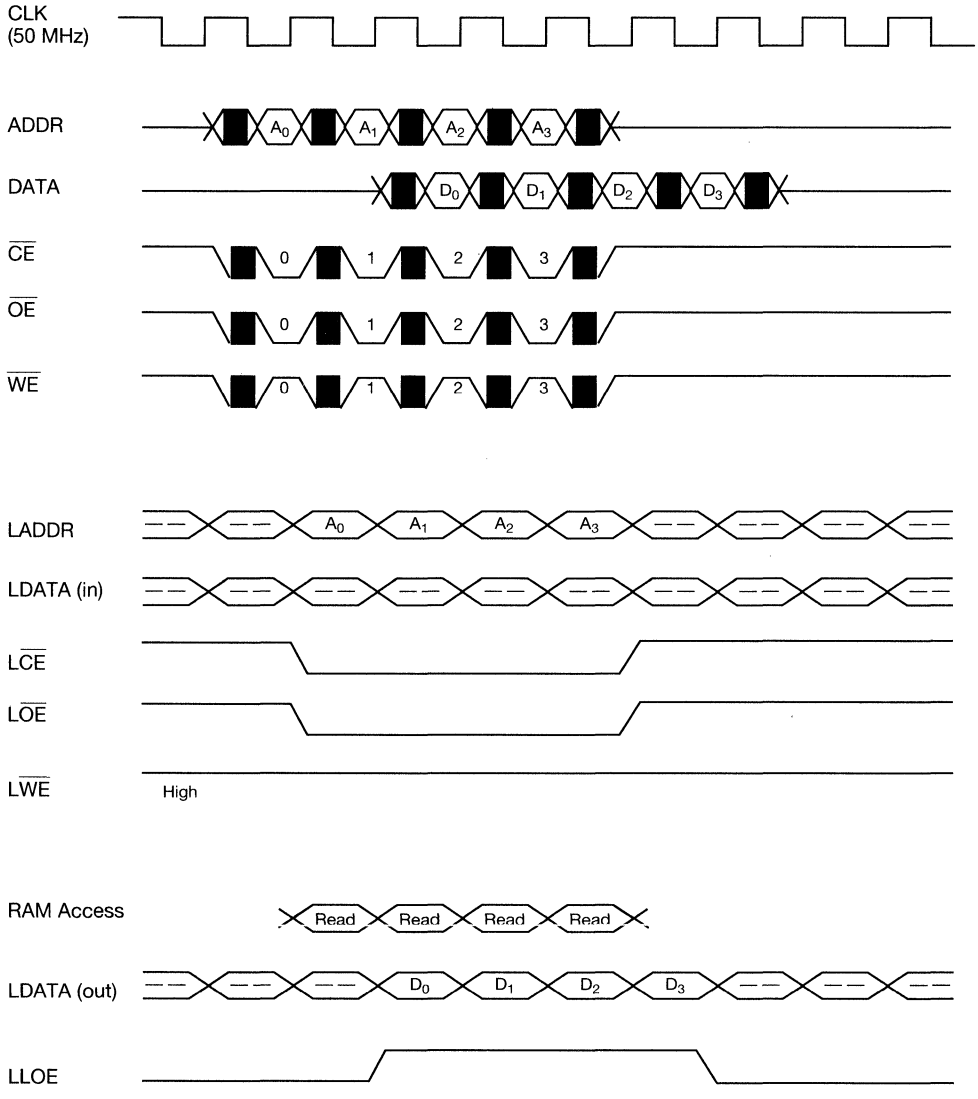
Write/Read Cycle



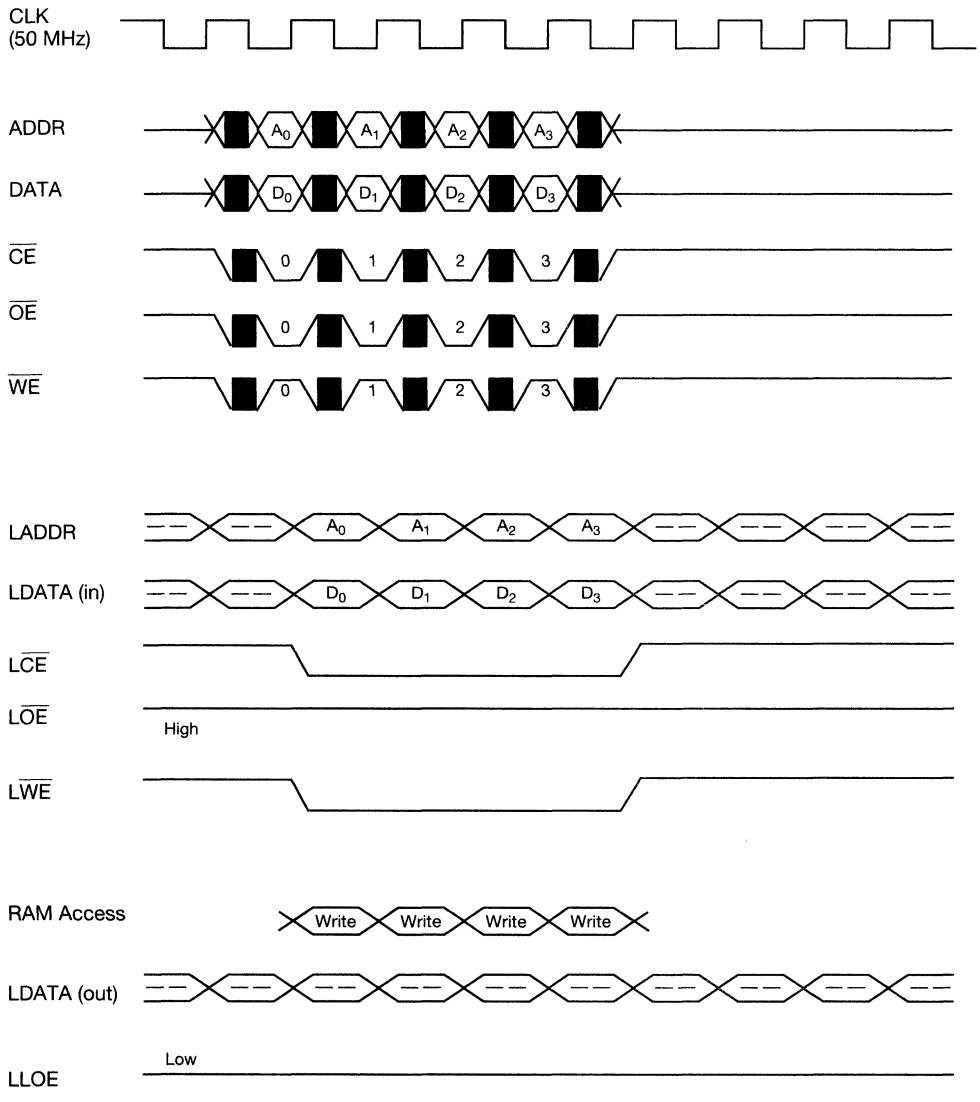
Note: 1. Low impedance state is obtained on next cycle from $\overline{OE}$ = L, $\overline{CE}$ = L, or $\overline{WE}$ = H.

3

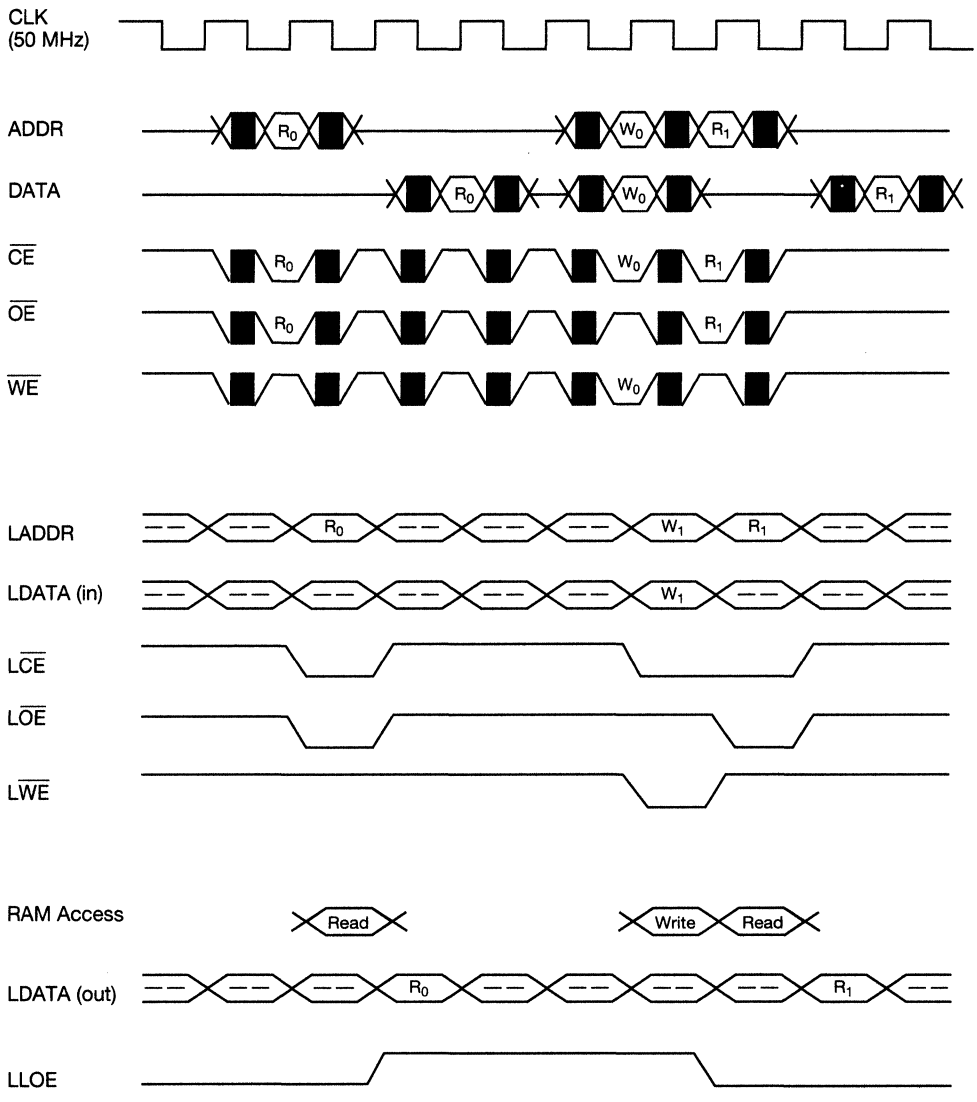
Pipelined Read Cycle (including internal signals)



Pipelined Write Cycle (including internal signals)



Alternate Read/Write/Read Cycle (including internal signals)



HB66B1616A Series

16,384-Word × 16-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66B1616A is a high speed 16K × 16 Static RAM module, mounted 4 pieces of 64K bit SRAM (HM6289JP) sealed in SOJ package. An outline of the HB66B1616A is 36-pin dual in-line package. Therefore, the HB66B1616A makes high density mounting possible without surface mount technology. The HB66B1616A provides common data inputs and outputs. Its module board has decoupling capacitors to reduce noise.

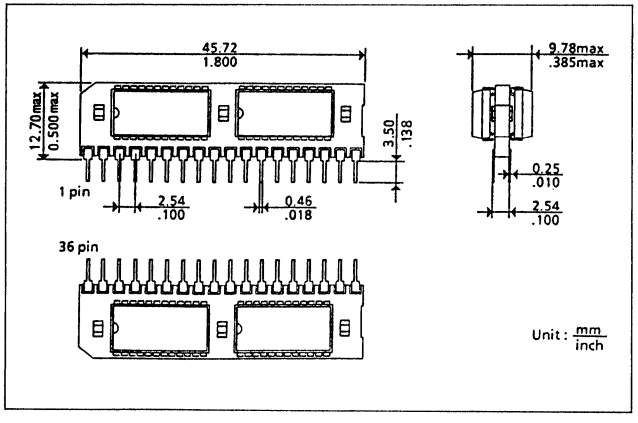
■ FEATURES

- Single 5V (± 5%) Supply
- High Speed
  - Access Time . . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .1200mW typ.
  - Standby Mode . . . . . .300mW typ. (TTL level)
  - 0.4mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

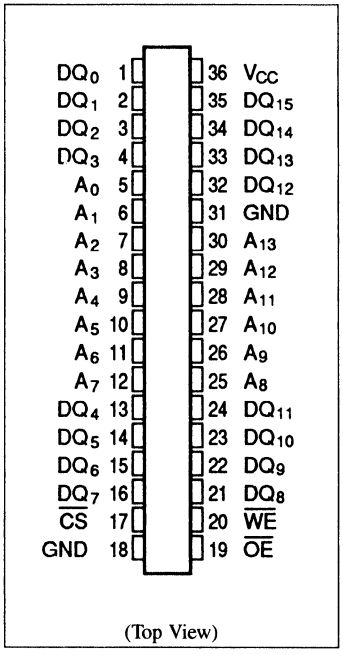
■ ORDERING INFORMATION

Part No.	Access	Package
HB66B1616A-25	25ns	36-pin dual in-line leaded type
HB66B1616A-35	35ns	

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT



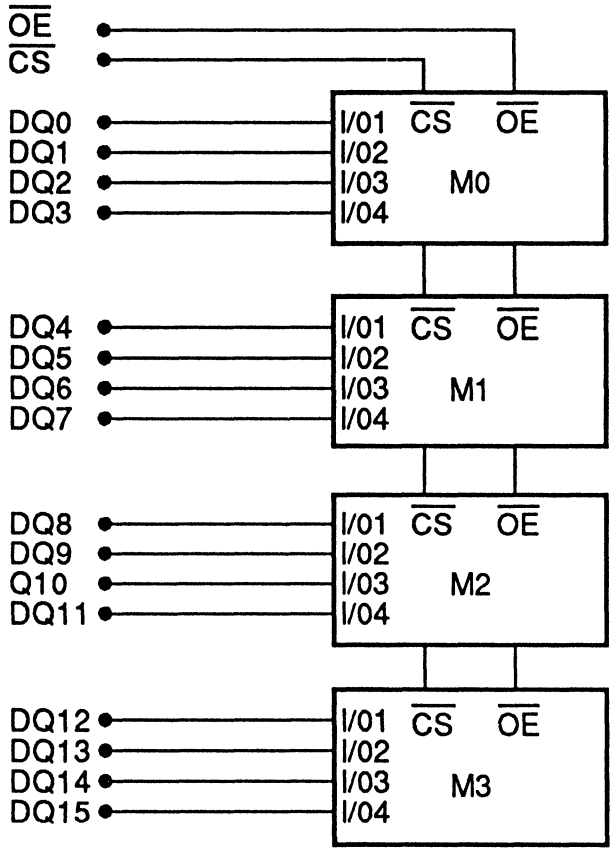
(Top View)

■ PIN DESCRIPTION

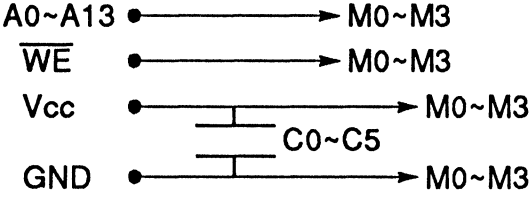
Pin Name	Function
A_0 ~ A_{13}	Address Input
DQ_0 ~ DQ_{15}	Data-in, Data-out
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
GND	Ground

3

■ BLOCK DIAGRAM



* M0~M3 : HM6289JP



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	-0.5[1] to +7.0	V
Power Dissipation	P_T	4.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. V_{in} min. = -2.0V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle (1-3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle (1) (2)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (3-6)

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5[1]	—	0.8	V

NOTE: 1. V_{IL} min. = -2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.[1]	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	-10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	-2	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA Min. Cycle	—	240	480	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} Min. Cycle	—	60	120	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ = ≥ V_{CC} -0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} -0.2V	—	0.08	8	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)[1]

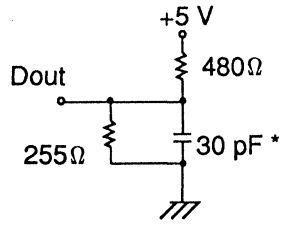
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	C_{in}	V_{in} = 0V	—	35	pF
Input/Output Capacitance (DQ)	$C_{I/O}$	$V_{I/O}$ = 0V	—	15	pF

NOTE: 1. This parameter is sampled and not 100% tested.

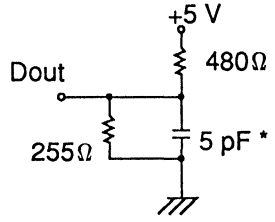
■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Levels: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figures



Output Load A



Output Load B
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} & t_{OW})

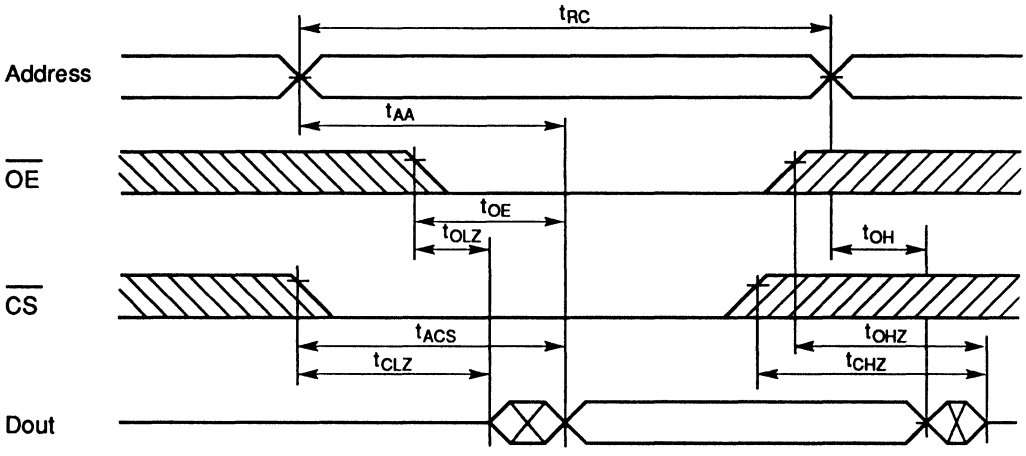
*Including scope and jig capacitance.

• Read Cycle

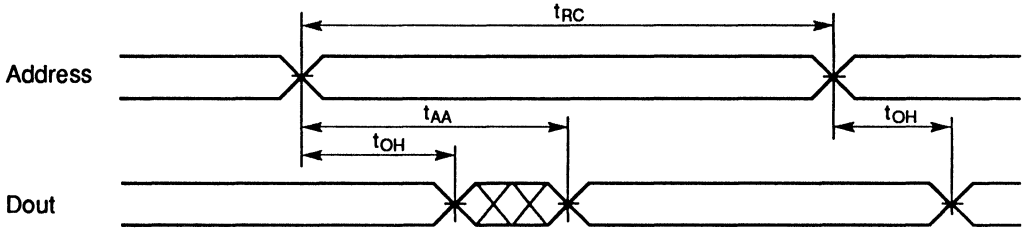
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Chip Selection to Output in Low-Z	t_{CLZ}(1)	5	—	5	—	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	ns
Output Enable to Output in Low-Z	t_{OLZ}(1)	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}(1)	0	12	0	20	ns
Chip Disable to Output in High-Z	t_{OHZ}(1)	0	10	0	10	ns
Output Hold from Address Change	t_{OH}	3	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	30	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

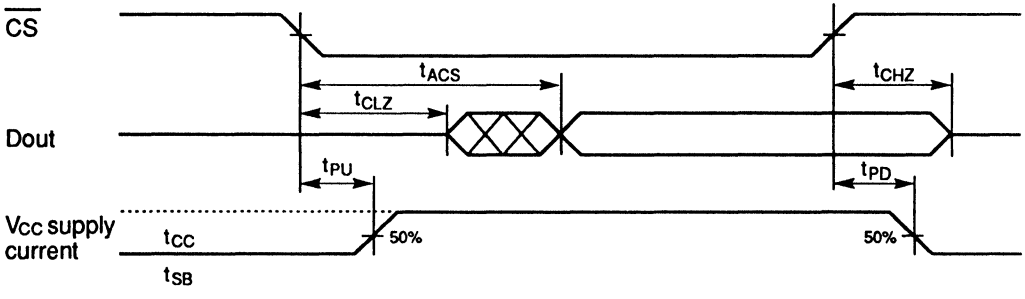
• **Read Timing Waveform (1)** (1)



• **Read Timing Waveform (2)** (1) (2) (4)



• **Read Timing Waveform (3)** (1) (3) (4)



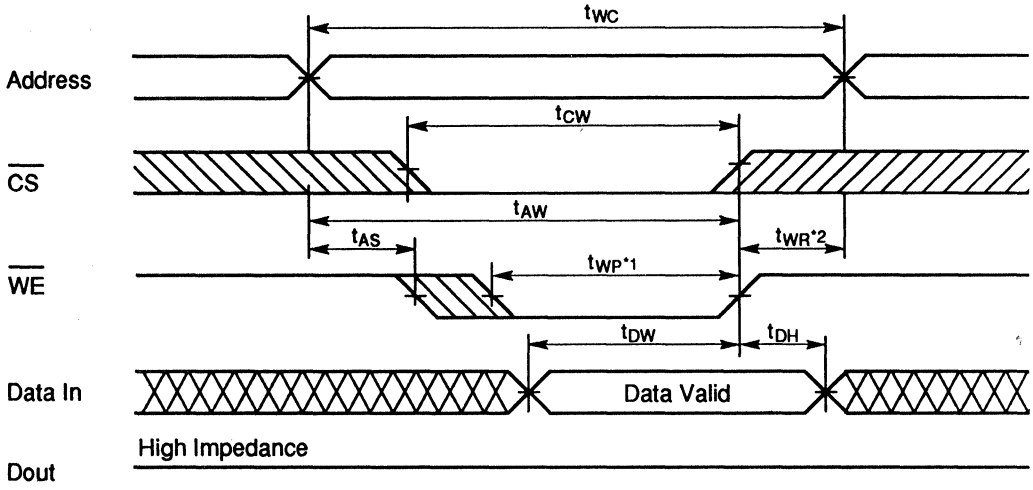
NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.

• **Write Cycle**

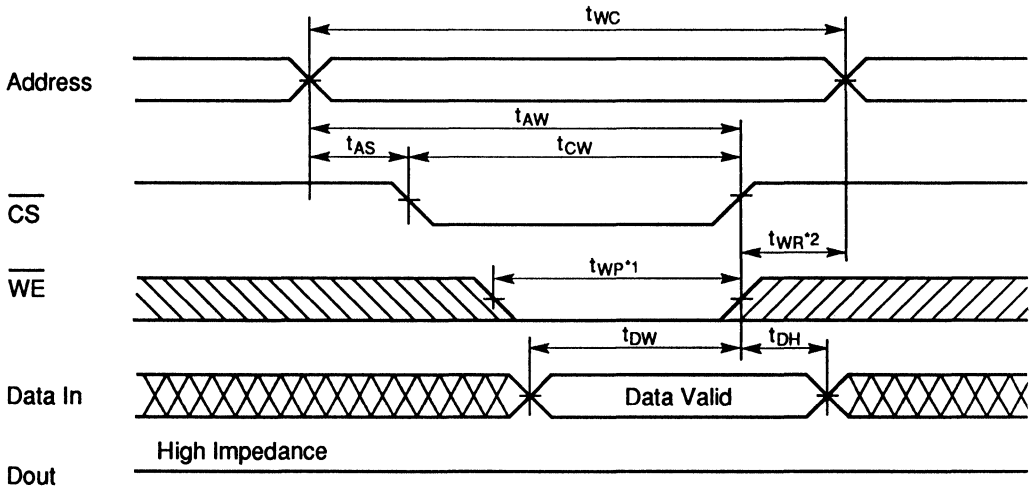
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}(1)	0	10	0	10	ns
Write to Output in High-Z	t_{WHZ}(1)	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	12	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write	t_{OW}(1)	5	—	5	—	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

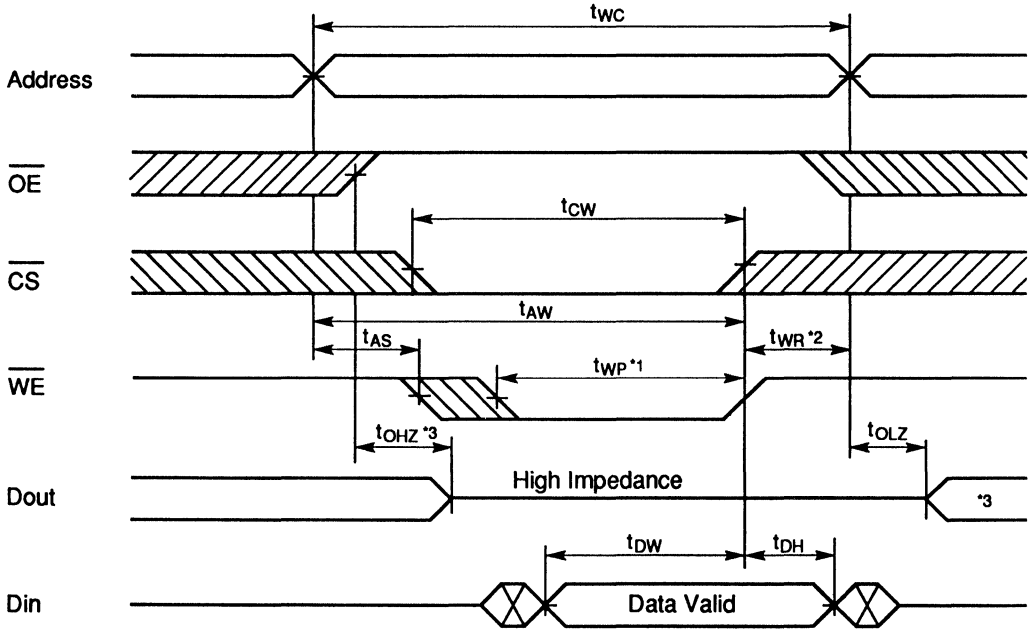
• **Write Timing Waveform (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



• **Write Timing Waveform (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)

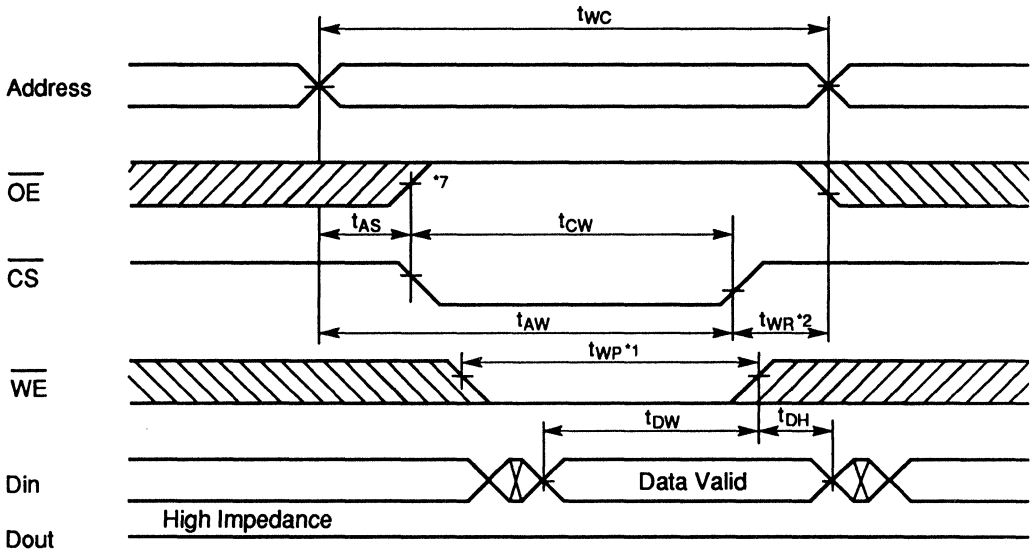


• **Write Timing Waveform (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)

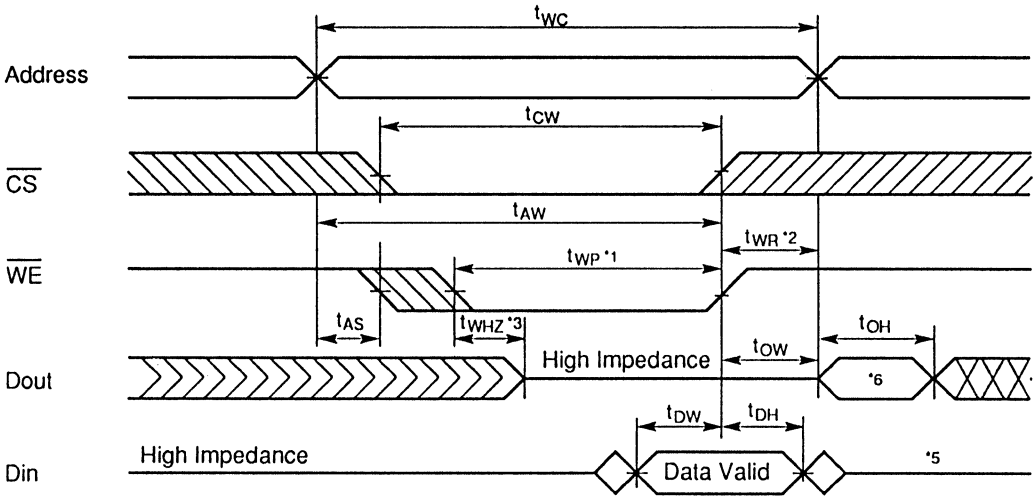


3

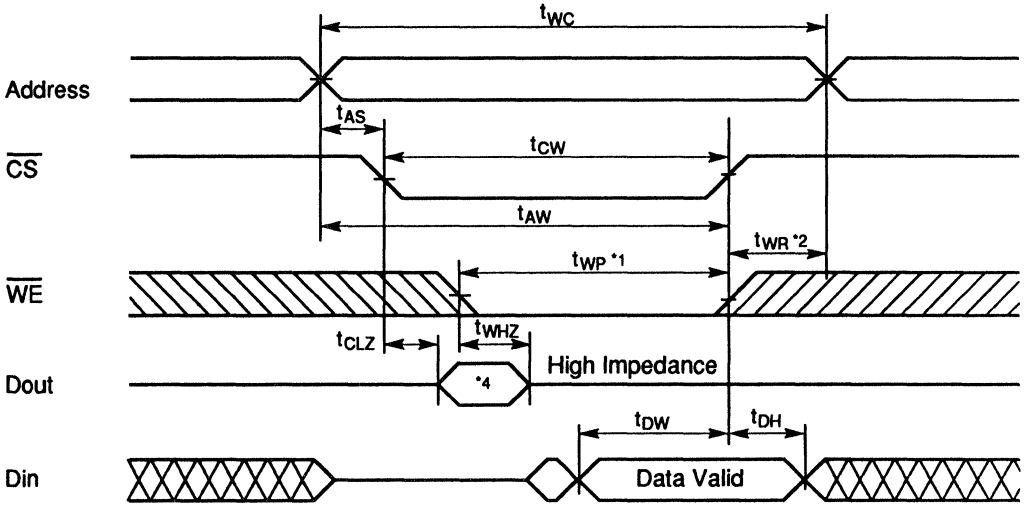
• **Write Timing Waveform (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Timing Waveform (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Timing Waveform (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after t_{OW}. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.
7. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, the output buffers remain in a high impedance state.

HB66A2568A Series

262,144-Word × 8-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66A2568A is a high speed 256K × 8 Static RAM module, mounted 8 pieces of 256K bit SRAM (HM6207HJP) sealed in SOJ package. An outline of the HB66A2568A is 60-pin zigzag in-line package. Therefore, the HB66A2568A makes high density mounting possible without surface mount technology. The HB66A2568A provides separate data inputs and output. Its module board has decoupling capacitors to reduce noise.

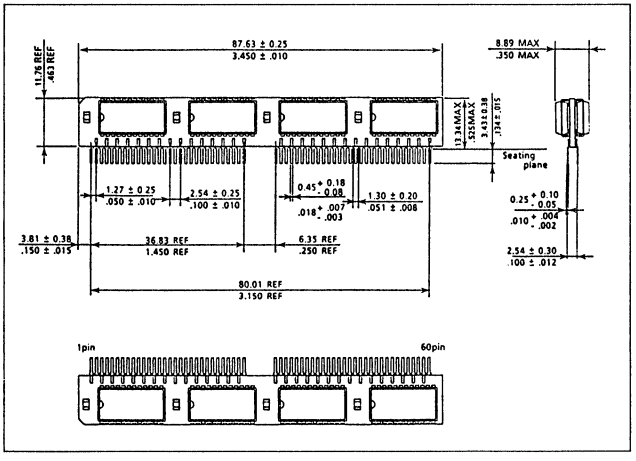
■ FEATURES

- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .2400mW typ.
  - Standby Mode . . . . . .800mW typ. (TTL level)
    0.8mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

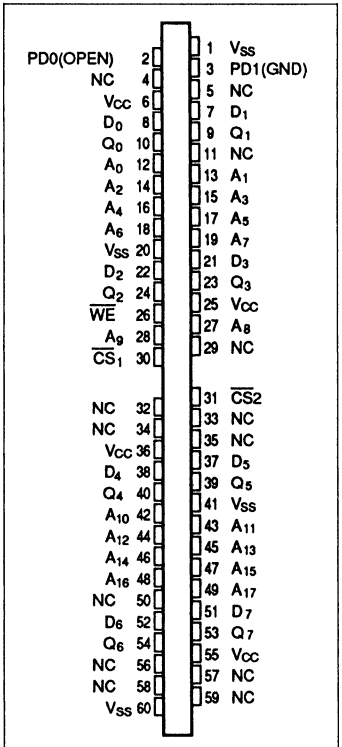
■ ORDERING INFORMATION

Part No.	Access	Package
HB66A2568A-25	25ns	60-pin zigzag in-line leaded type
HB66A2568A-35	35ns	

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT



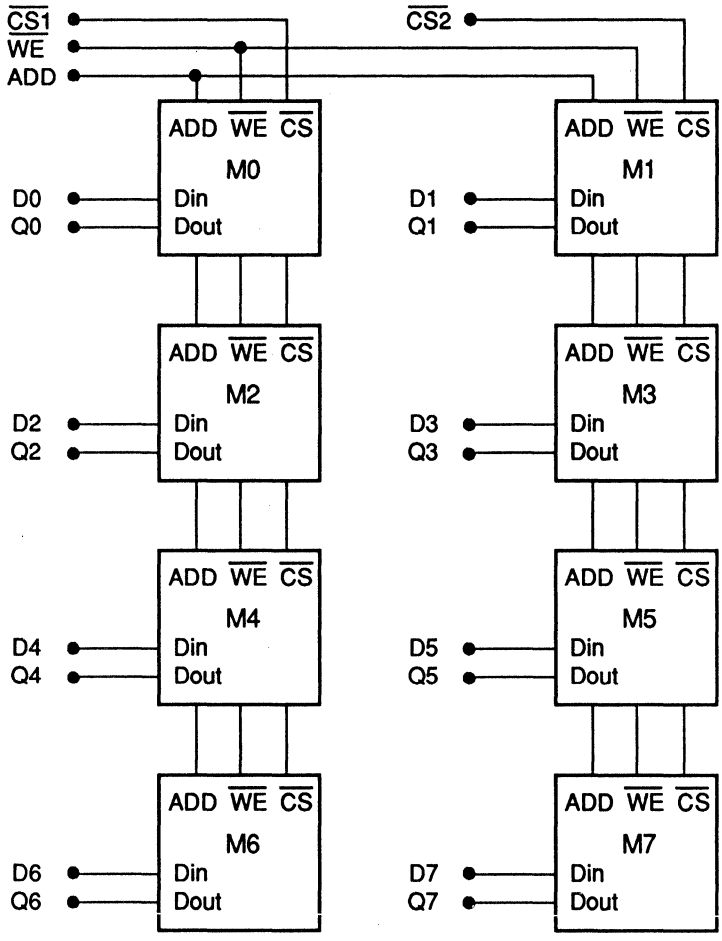
(Top View)

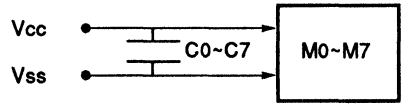
■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_{17}	Address Input
D_0 ~ D_7	Data-in
Q_0 ~ Q_7	Data-out
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-connection

3

■ BLOCK DIAGRAM





C=0.22μF

* M0~M7 : HM6207HJP

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	-0.5[1] to +7.0	V
Power Dissipation	P_T	8.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. V_{in} min. = -2.5V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}_1$, $\overline{CS}_2$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5[1]	—	0.8	V

NOTE: 1. V_{IL} min. = -2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.[1]	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	-10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	-10	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IL}, $I_{I/O}$ = 0mA Min. Cycle, Duty = 100%	—	480	960	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH} Min. Cycle	—	160	320	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}_1$, $\overline{CS}_2$ = ≥ V_{CC} -0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} -0.2V	—	0.16	16	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)[1]

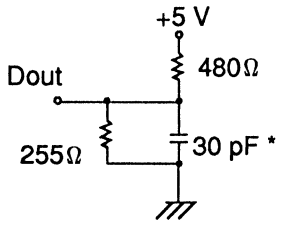
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{WE}$)	C_{I1}	V_{in} = 0V	—	70	pF
Input Capacitance ($\overline{CS}$)	C_{I2}	V_{in} = 0V	—	45	pF
Input Capacitance (Data in)	C_{I3}	V_{in} = 0V	—	12	pF
Output Capacitance (Data out)	C_O	V_{out} = 0V	—	16	pF

NOTE: 1. This parameter is sampled and not 100% tested.

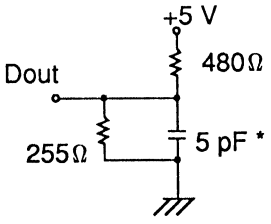
■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Levels: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figures



Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

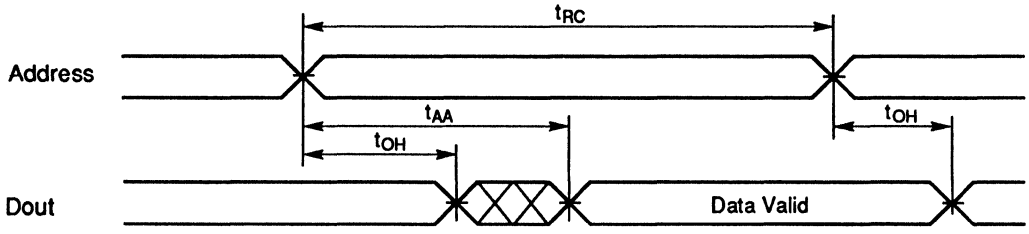
*Including scope and jig capacitance.

• Read Cycle

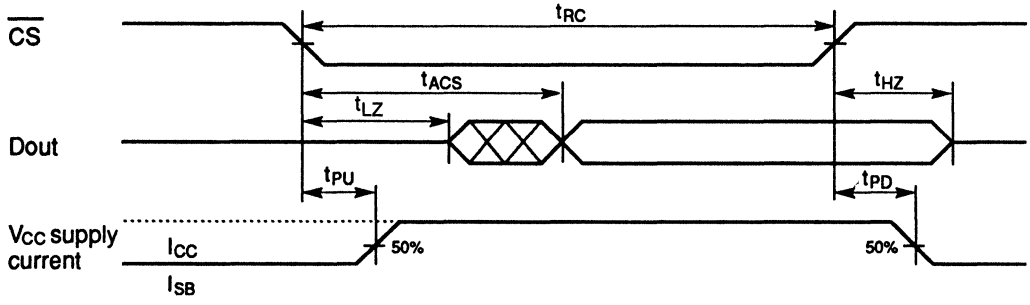
Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}(1)	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}(1)	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	ns

NOTE: 1. Transition is measured ±200mV from steady state voltage with Load (B)
This parameter is sampled and not 100% tested.

• **Timing Waveform of Read Cycle (1)** (1) (2)



• **Timing Waveform of Read Cycle (2)** (1) (3)



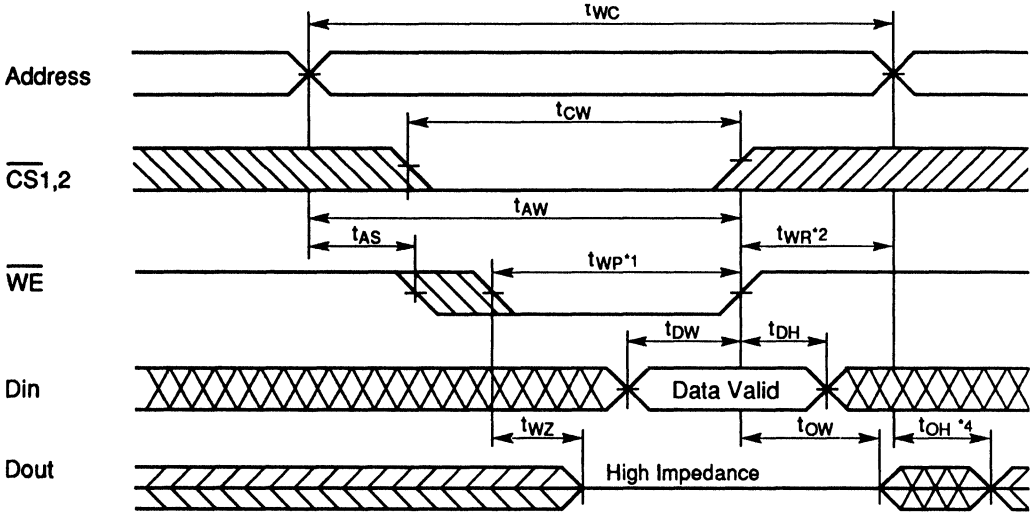
NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle**

Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High-Z	t_{WZ}(1)	0	8	0	10	ns
Output Active from End of Write	t_{OW}(2)	0	—	0	—	ns

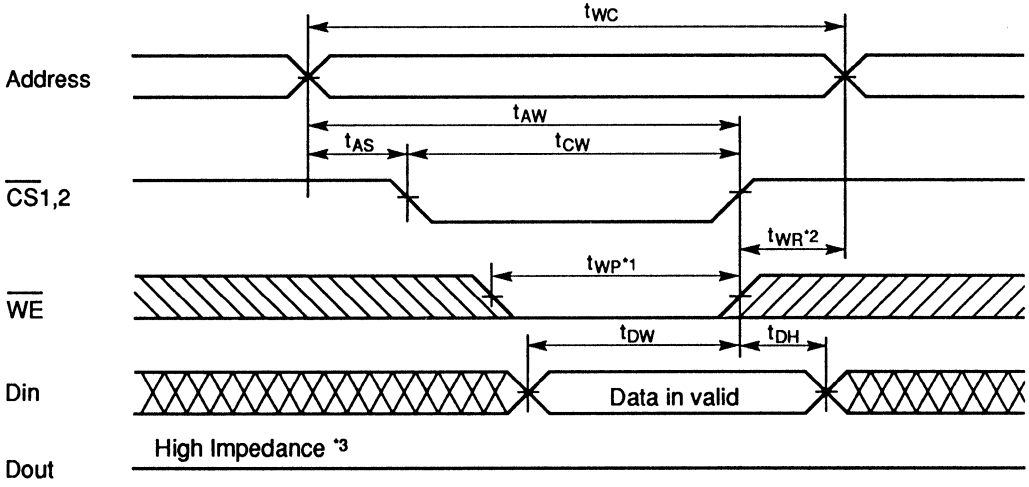
NOTE: 1. Transition is measured ±200mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• **Timing Waveform of Write Cycle (1)** ($\overline{WE}$ Controlled)



3

• **Timing Waveform of Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

4. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.

Section 4
MOS Pseudo Static RAM

4

HITACHI®

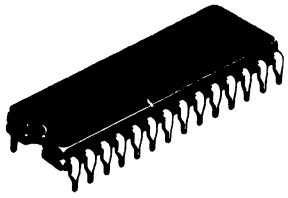
HM65256B Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

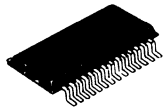
- Single 5V (±10%)
- High Speed
  Access Time
  $\overline{CE}$ Access Time 100/120/150/200ns
  Address Access Time 50/60/75/100ns
  (in Static Column Mode)
  Cycle Time
  Random Read/Write Cycle Time 160/190/235/310ns
  Static Column Mode Cycle Time 55/65/80/105ns
- Low Power
  175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh

HM65256BP Series



(DP-28)

HM65256BFP Series

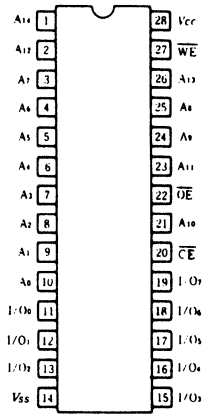


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM65256BP-10	100ns	600 mil 28 pin Plastic DIP
HM65256BP-12	120ns	
HM65256BP-15	150ns	
HM65256BP-20	200ns	
HM65256BLP-10	100ns	
HM65256BLP-12	120ns	
HM65256BLP-15	150ns	
HM65256BLP-20	200ns	
HM65256BFP-10T	100ns	28 pin Plastic SOP
HM65256BFP-12T	120ns	
HM65256BFP-15T	150ns	
HM65256BFP-20T	200ns	
HM65256BLFP-10T	100ns	
HM65256BLFP-12T	120ns	
HM65256BLFP-15T	150ns	
HM65256BLFP-20T	200ns	

■ PIN ARRANGEMENT



(Top View)

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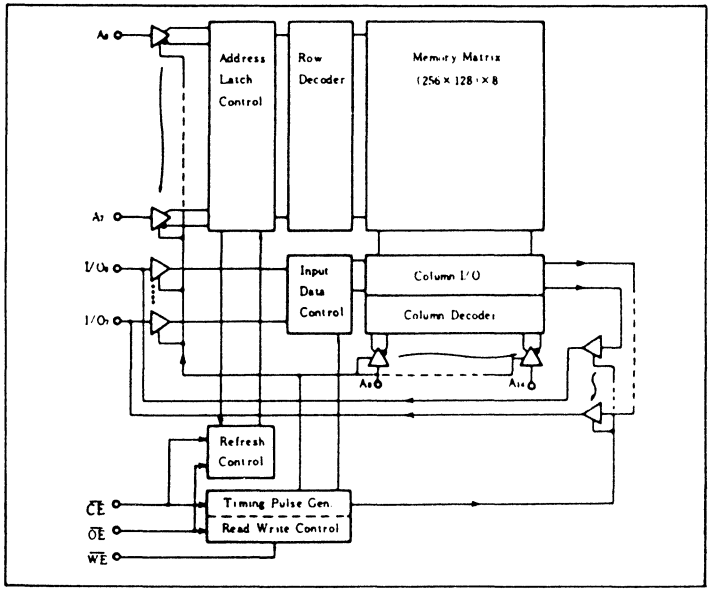
■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	–
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Conditions	HM65256B Series			HM65256BL Series			Unit
			min.	typ.	max.	min.	typ.	max.	
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0mA, t_{cyc} = min.	–	35	65	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	–	1	2	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \geq V_{CC}-0.2V$	–	–	–	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	–	1	2	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \leq 0.2V$	–	–	–	–	50	100	μA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, Vin = V_{SS} to V_{CC}	−10	–	10	−10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	−10	–	10	−10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = −1 mA	2.4	–	–	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	Cin	Vin = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

- AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level . . . . . V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load . . . . . 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	235	–	310	–	ns
Static Column Mode Read or Write Cycle	t_{RSC}	55	–	65	–	80	–	105	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	–	200	ns
Address Access Time	t_{AA}	–	50	–	60	–	75	–	100	ns
Output Enable Access Time	t_{OEA}	–	40	–	50	–	60	–	75	ns
Chip Disable to Output in High Z	t_{CHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	30	–	35	–	40	–	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable Pulse Width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	50	–	60	–	75	–	100	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	20	–	20	–	25	–	30	–	ns
Column Address Hold Time	t_{CAH}	100	–	120	–	150	–	200	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns
Output Enable Hold Time	t_{OHC}	0	–	0	–	0	–	0	–	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	–	0	–	0	–	0	–	ns
Output Hold Time from Column Address	t_{OH}	5	–	5	–	5	–	10	–	ns
Write Command Pulse Width	t_{WP}	25	–	25	–	30	–	35	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	200	–	ns
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	0	–	ns

(to be continued)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Column Address Hold Time after Write	t_{AHW}	0	–	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	20	–	25	–	30	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	50	–	60	–	75	–	100	–	ns
Refresh Precharge Time	t_{FP}	30	–	30	–	30	–	30	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	160	–	190	–	235	–	310	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	–	10000	–	10000	–	10000	–	ns
Refresh Reset Time for Self Refresh	t_{FRS}	160	–	190	–	235	–	310	–	ns
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.

(2) t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T=5ns, and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

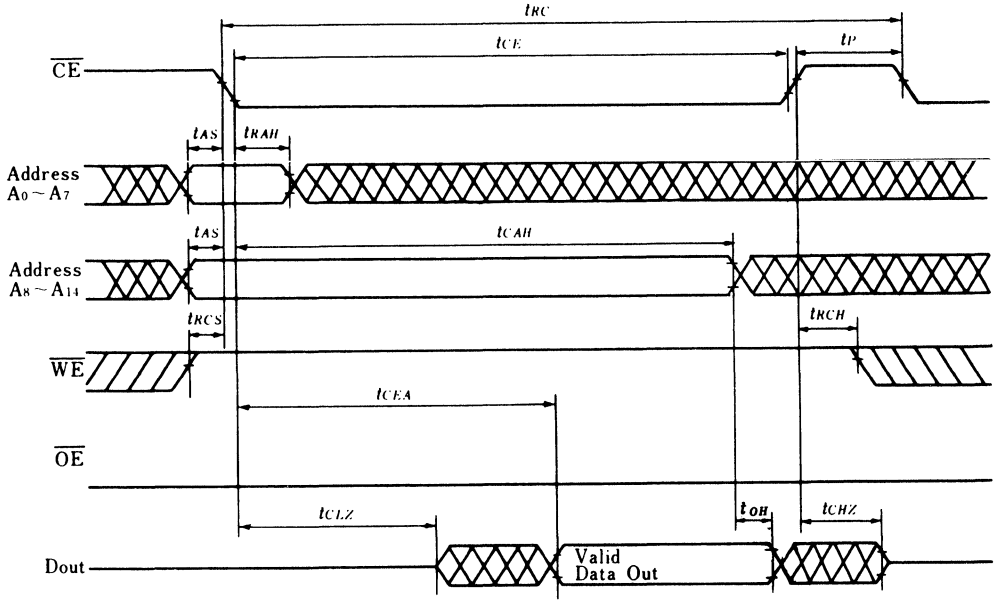
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

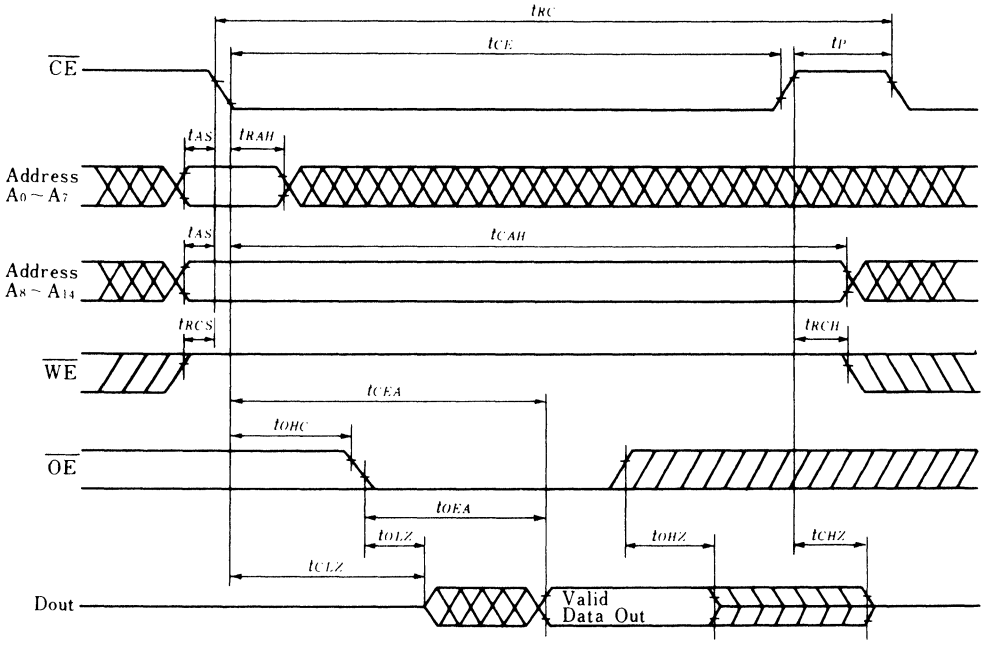
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

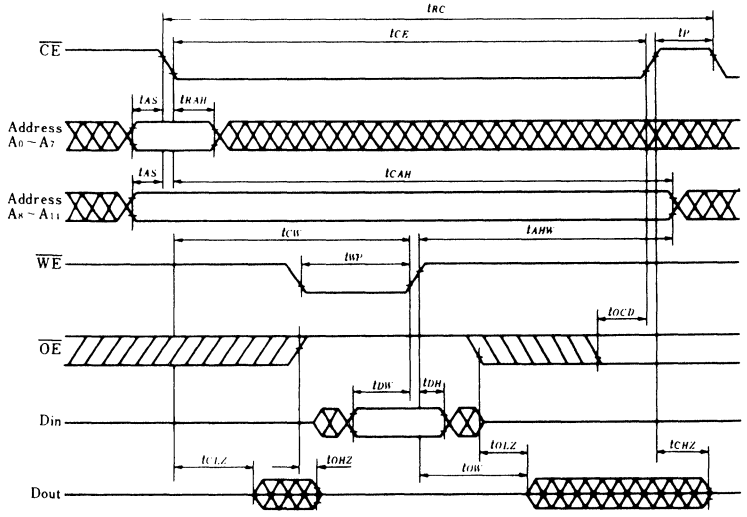
• Read Cycle No. 1 ($\overline{CE}$ controlled)



- **Read Cycle No. 2 ($\overline{OE}$ controlled)**



- **Write Cycle No. 1 ($\overline{OE}$ Clock)**



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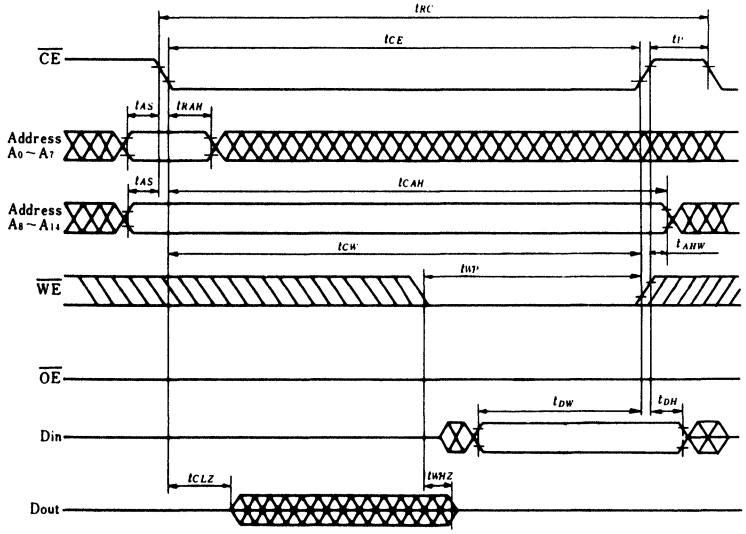
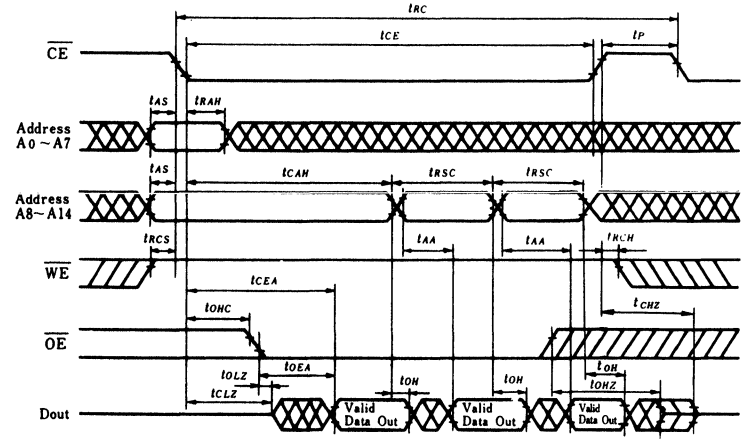
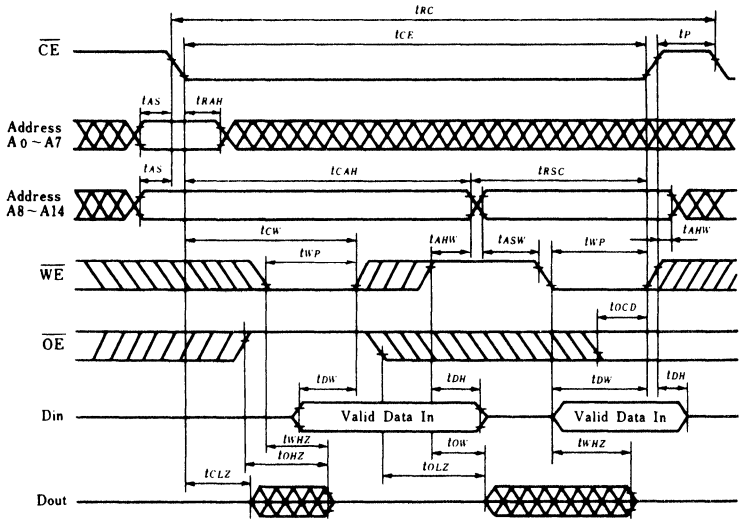
- **Write Cycle No. 2 ($\overline{OE}$ low fix)**



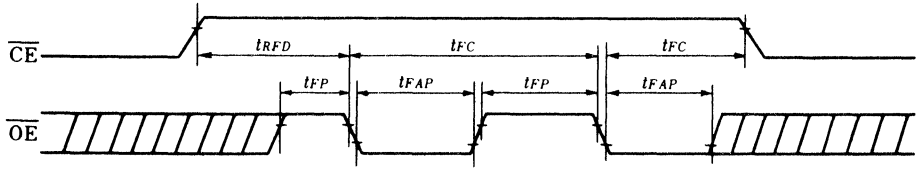
- **Static Column Mode Read Cycle**



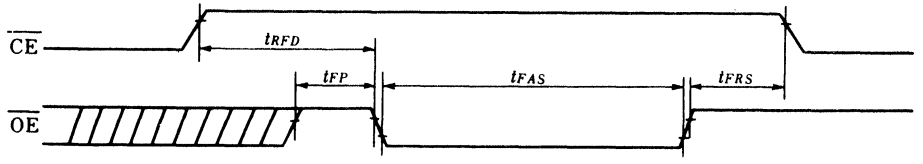
- **Static Column Mode Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



4

HM658128 Series

131,072-Word × 8-Bit High Speed Psuedo Static Ram

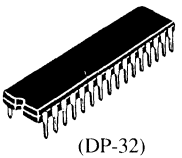
The HM658128 Series has been converted to the HM658128A Series.

HM658128A Series

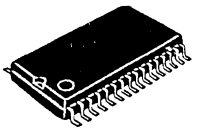
131,072-Word x 8-Bit High Speed Pseudo Static RAM

■ FEATURES

- Single 5V (±10%)
- High speed
  - Access time
    - CE access time: 80/100/120 ns
  - Cycle time
    - Random read/write cycle time: 130/160/190 ns
- Low power
  - 250 mW typ. Active
  - 350 μW typ. Standby (L-version, LL-version)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
  - 32-pin TSOP package
- Non multiplexed address
- 512 refresh cycles (8ms)
- Refresh functions
  - LP/LLP-version: Address refresh, automatic refresh, self refresh
  - DP-version: Address refresh, automatic refresh



(DP-32)



(FP-32D)

(TFP-32D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658128ALP-8L HM658128ALP-10L HM658128ALP-12L	80 ns 100 ns 120 ns	600-mil 32-Pin Plastic DIP Series (DP-32)
HM658128ALP-8 HM658128ALP-10 HM658128ALP-12	80 ns 100 ns 120 ns	
HM658128ADP-8 HM658128ADP-10 HM658128ADP-12	80 ns 100 ns 120 ns	
HM658128ALFP-8L HM658128ALFP-10L HM658128ALFP-12L	80 ns 100 ns 120 ns	525-mil 32-Pin Plastic SOP Series (FP-32D)
HM658128ALFP-8 HM658128ALFP-10 HM658128ALFP-12	80 ns 100 ns 120 ns	
HM658128ADFP-8 HM658128ADFP-10 HM658128ADFP-12	80 ns 100 ns 120 ns	
HM658128ALT-8L HM658128ALT-10L HM658128ALT-12L	80 ns 100 ns 120 ns	8mm x 20mm 32-Pin Plastic TOSP Series (TFP-32D)
HM658128ALT-8 HM658128ALT-10 HM658128ALT-12	80 ns 100 ns 120 ns	
HM658128ADT-8 HM658128ADT-10 HM658128ADT-12	80 ns 100 ns 120 ns	
HM658128ALR-8L HM658128ALR-10L HM658128ALR-12L	80 ns 100 ns 120 ns	8mm x 20mm 32-Pin Plastic TSOP Series (TFP-32DR)
HM658128ALR-8 HM658128ALR-10 HM658128ALR-12	80 ns 100 ns 120 ns	
HM658128ADR-8 HM658128ADR-10 HM658128ADR-12	80 ns 100 ns 120 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{16}	Address
I/O_0–I/O_7	Input/Output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
CS	Chip Select
V_{CC}	Power Supply
V_{SS}	Ground

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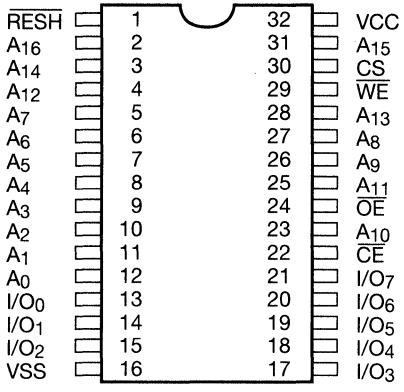
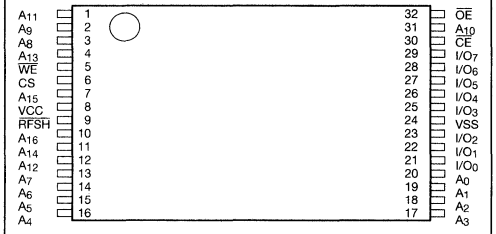
■ PIN ARRANGEMENT

HM658128AP/AFP Series



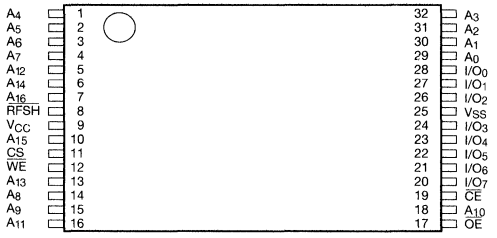
(Top View)

HM658128AT Series



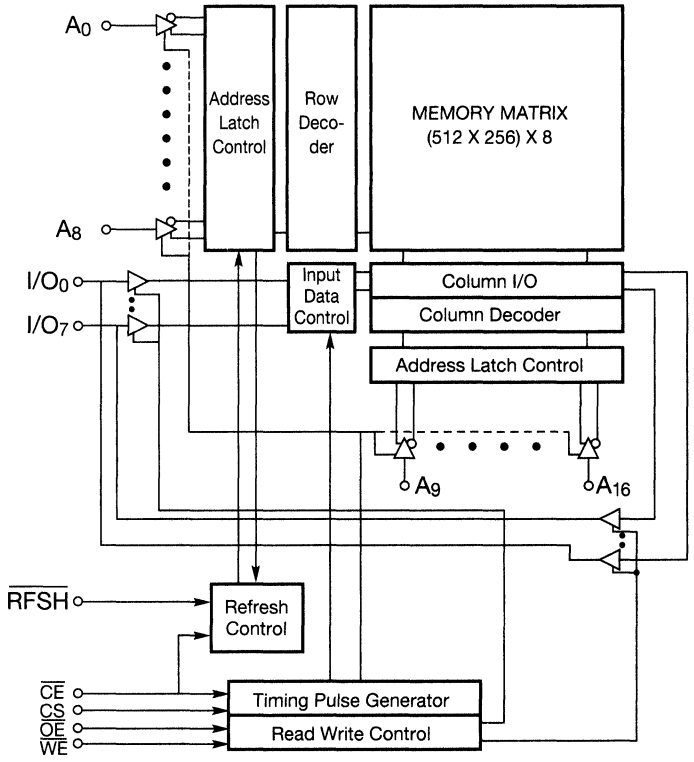
(Top View)

HM658128AR Series



(Top View)

■ BLOCK DIAGRAM



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Pin Functions

$\overline{CE}$: Chip Enable (Input)
$\overline{CE}$ is a basic clock. RAM is active when $\overline{CE}$ is low, and is on standby when $\overline{CE}$ is high.

A_0–A_{16}: Address Inputs (Input)
A_0–A_8 is a row address and A_9–A_{16} is a column address. The entire address A_0–A_{16} is fetched into RAM by the falling edge of $\overline{CE}$.

$\overline{WE}$: Write Enable (Input)
RAM is in write mode when $\overline{WE}$ is low, and is in read mode when $\overline{WE}$ is high. I/O data is fetched into RAM by the rising edge of $\overline{WE}$ or $\overline{CE}$ (earlier timing) and the data is written into memory cells.

$\overline{OE}$: Output Enable (Input)
$\overline{OE}$ controls the output condition of the I/O pins. The I/O pins are active when $\overline{OE}$ is low, and are at high impedance when $\overline{OE}$ is high.

$\overline{RFSH}$: Refresh (Input)
RAM goes into refresh mode when $\overline{RFSH}$ goes low in standby mode. (i.e., when $\overline{CE}$ is high). There are two refresh modes controlled by $\overline{RFSH}$: automatic refresh and self refresh.

CS: Chip Select (Input)
RAM is active when CS is high. The CS signal is fetched into RAM by the falling edge of $\overline{CE}$, and is held for one read/write cycle.

I/O_0–I/O_7: Input/Output (Input and Output)
These pins are data I/O pins.

Refresh

There are three refresh modes: address refresh, automatic refresh, and self refresh.

(1) Address refresh

Data is refreshed by accessing all 512 row addresses every 8 ms. A read is one method of accessing those addresses. Each row address (each of the 512 addresses A_0–A_8) must be read at least once every 8 ms. In address refresh mode, $\overline{OE}$ can remain high. In this case, the I/O pins remain at high impedance, but the refresh is done within RAM.

(2) Automatic refresh

Instead of address refresh, automatic refresh can be used. RAM goes to automatic refresh mode if $\overline{RFSH}$ fall while $\overline{CE}$ is high and it remains low for at least t_{FAP}. One automatic refresh cycle is executed by one low pulse of $\overline{RFSH}$. It is not necessary to input the refresh address from outside since it is generated internally by an on-chip address counter. 512 automatic refresh cycles must be done every 8 ms.

(3) Self refresh

Self refresh mode is suitable for data retention by battery. In standby mode, a self refresh starts automatically when $\overline{RFSH}$ stays low for more than 8 µs. Refresh addresses are automatically specified by the on-chip address counter, and the refresh period is determined by the on-chip timer.

Automatic refresh and self refresh are distinguished from each other by the width of the $\overline{RFSH}$ low pulse in standby mode. If the $\overline{RFSH}$ low pulse is wider than 8 µs, RAM enters self refresh mode; if the $\overline{RFSH}$ low pulse is less than 8 µs, it is recognized as an automatic refresh instruction.

Notes on Using the HM658128A

Since pseudo static RAM consists of dynamic circuits like DRAM, it is more noise-sensitive than conventional SRAM.

(1) If a short $\overline{CE}$ pulse of a width less than t_{CE} min is applied to RAM, an incomplete read occurs and stored data may be destroyed. Make sure that $\overline{CE}$ low pulses of less than t_{CE} min are inhibited. Note that a 10 ns $\overline{CE}$ low pulse may sometimes occur owing to the gate delay on the board if the $\overline{CE}$ signal is generated by the decoding of higher address signals on the board. Avoid these short pulses.

(2) A short $\overline{RFSH}$ low pulse may cause an incomplete refresh that will destroy data. Make sure that $\overline{RFSH}$ low pulses of less than t_{FAP} min are also inhibited.

(3) Start the HM658128A operating by executing at least eight initial cycles (dummy cycles) at least 100 µs after the power voltage reaches 4.5V–5.5V after power-on.

■ FUNCTION TABLE

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low-Z	Read
L	H	X	X	L	High-Z	Write
L	H	X	H	H	High-Z	—
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh
H	X	H	X	X	High-Z	Standby

Note: 1. X means don't care.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	–1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature Under Bias	T_{bias}	–10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	–0.5	—	0.8	V

Note: 1. V_{IL} min = –3.0 V for pulse width 10 ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ	Max.	Unit	Test Conditions	Note
Operating Power Supply Current	I_{CC1}	—	50	85	mA	$I_{I/O}$ = 0, t_{cyc} = 130 ns	
Standby Power Supply Current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}	
	I_{SB2}	— —	100 70	200 100	µA	$\overline{CE}$ ≥ V_{CC} –0.2V, $\overline{RFSH}$ ≥ V_{CC} –0.2V	L-version LL-version
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	—	1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}	L-version LL-version
	I_{CC3}	— —	100 70	200 100	µA	$\overline{CE}$ ≥ V_{CC} –0.2V, $\overline{RFSH}$ ≤ –0.2V	L-version LL-version
Input Leakage Current	I_{LI}	–10	—	10	µA	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	I_{LO}	–10	—	10	µA	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA	

4

■ CAPACITANCE

Item	Symbol	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	8	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

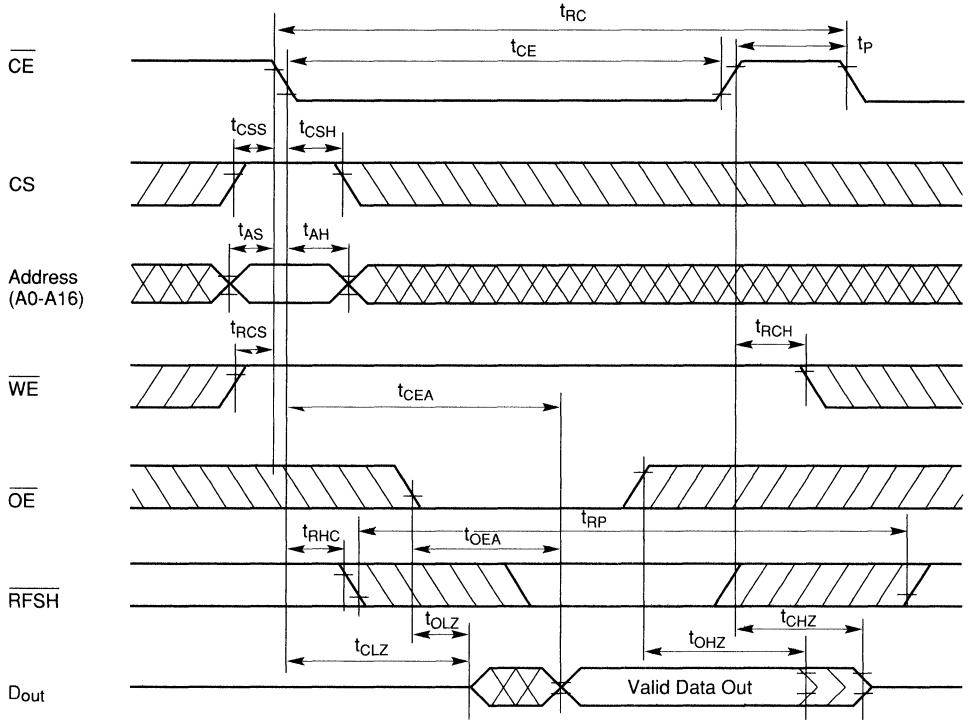
AC Test Conditions

- Input pulse levels: 2.4V, 0.4V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2V, 0.8V
- Reference level: V_{OH} = 2.0V, V_{OL} = 0.8V
- Output load: 1 TTL and 100 pF

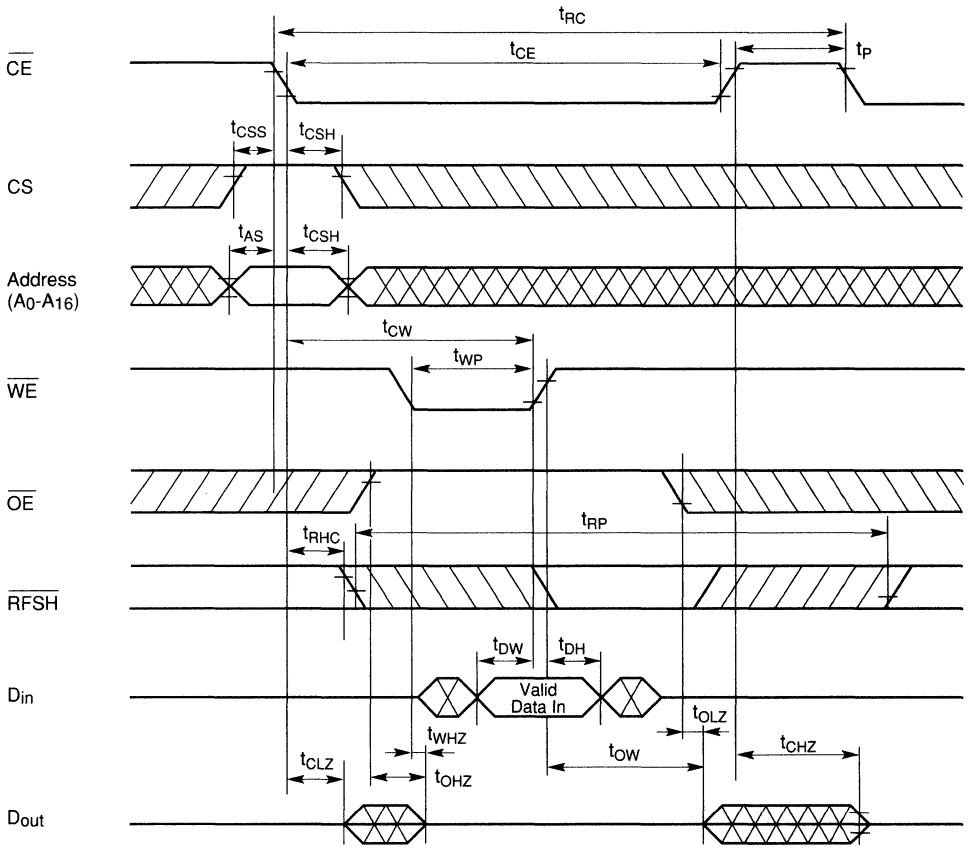
Item	Symbol	HM658128A-8		HM658128A-10		HM658128A-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	190	—	ns	
Random Read Modify Write Cycle Time	t_{RWC}	190	—	220	—	260	—	ns	
Chip Enable Access Time	t_{CEA}	—	80	—	100	—	120	ns	
Output Enable Access Time	t_{OEA}	—	30	—	30	—	40	ns	
Chip Disable to Output in High-Z	t_{CHZ}	0	30	0	30	0	35	ns	1, 2
Chip Enable to Output in Low-Z	t_{CLZ}	20	—	20	—	20	—	ns	2
Output Disable to Output in High-Z	t_{OHZ}	—	25	—	25	—	30	ns	1, 2
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns	2
Chip Enable Pulse Width	t_{CE}	80 ns	10 µs	100 ns	10 µs	120 ns	10 µs		
Chip Enable Precharge Time	t_P	40	—	50	—	60	—	ns	
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	30	—	30	—	35	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
RFSH Hold Time	t_{RHC}	15	—	15	—	15	—	ns	
Chip Select Set-up Time	t_{CSS}	0	—	0	—	0	—	ns	
Chip Select Hold Time	t_{CSH}	30	—	30	—	35	—	ns	
Write Command Pulse Width	t_{WP}	30	—	30	—	35	—	ns	
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns	
Data In to End of Write	t_{DW}	25	—	25	—	30	—	ns	
Data In Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns	
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	ns	2
Write to Output in High-Z	t_{WHZ}	—	25	—	25	—	30	ns	1, 2
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
Refresh Command Delay Time	t_{RFD}	40	—	50	—	60	—	ns	
Refresh Precharge Time	t_{FP}	40	—	40	—	40	—	ns	
Refresh Command Pulse Width	t_{RP}	—	8 µs	—	8 µs	—	8 µs		
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs	80 ns	8 µs		
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	190	—	ns	
Refresh Command Pulse Width for Self Refresh	t_{FAS}	8	—	8	—	8	—	µs	
Refresh Reset Time from Self Refresh	t_{RFS}	130	—	160	—	190	—	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	512 cycle

Notes:
1. t_{CHZ}, t_{OHZ}, and t_{WHZ} define the time at which the output achieves the open circuit conditions under the condition of t_T = 5 ns and not 100% tested.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of a low CE and low WE. Write end is defined at the earlier of WE going high or CE going high.
4. If CE goes low simultaneously with WE going low or after WE going low, the outputs remain in high impedance state.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. An initial pause of 100 µs is required after power-up followed by a minimum of 8 initialization cycles.
8. 512 cycles of burst refresh or distributed automatic refresh must be executed within 15 µs after self refresh, in order to meet the refresh specification of 8 ms and 512 cycle.

■ READ CYCLE


tRC
tCE
tP
CE
tCSS
tCSH
CS
tAS
tAH
Address
(A0-A16)
tRCS
tRCH
WE
tCEA
OE
tRP
tRHC
tOEA
RFSH
tOLZ
tCLZ
tCHZ
tOHZ
Dout
Valid Data Out

■ WRITE CYCLE ($\overline{OE}$ Clock)



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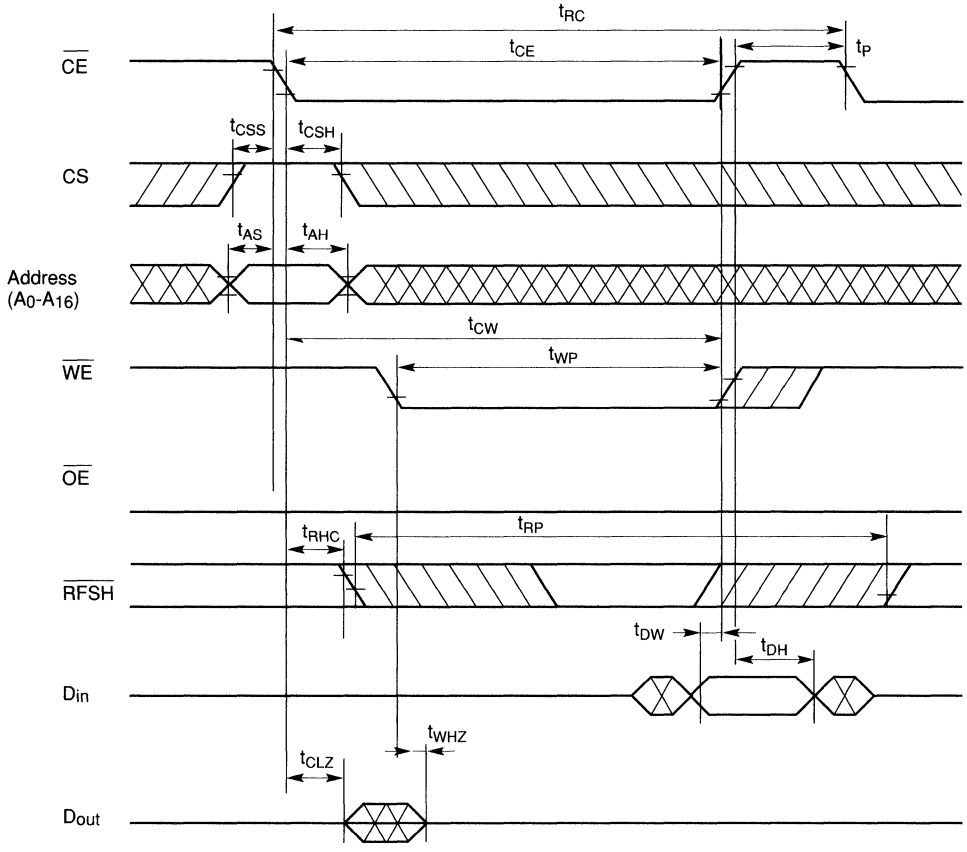
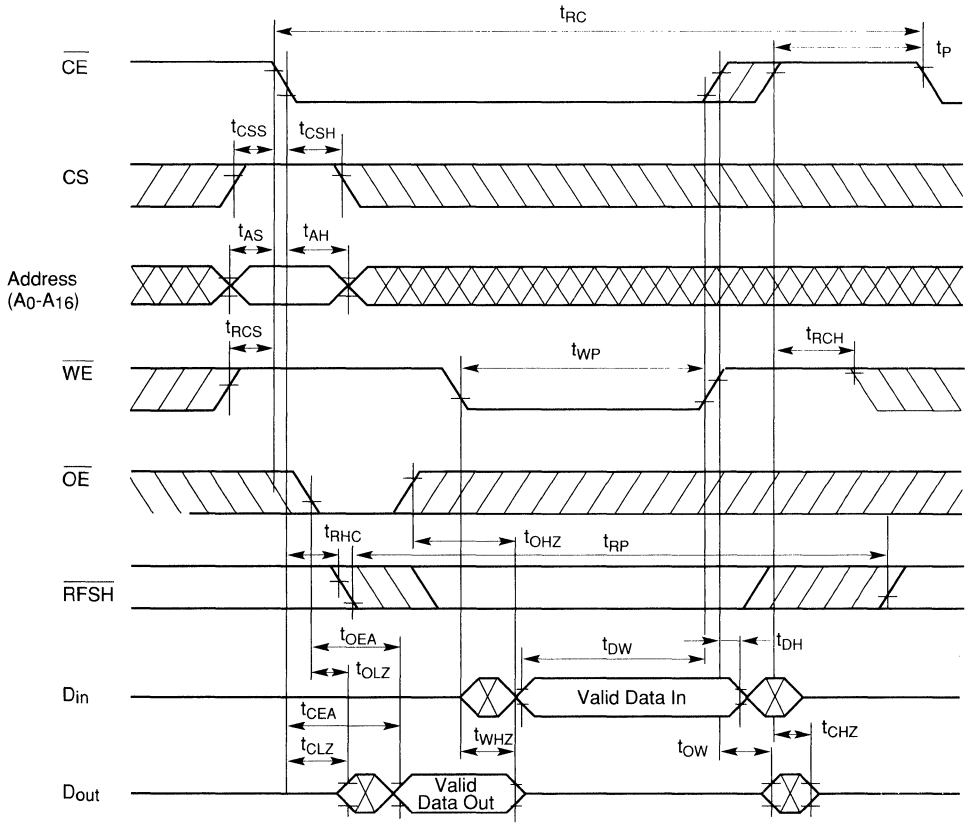
■ WRITE CYCLE ($\overline{OE}$ Low Fix)



■ READ-MODIFY-WRITE CYCLE



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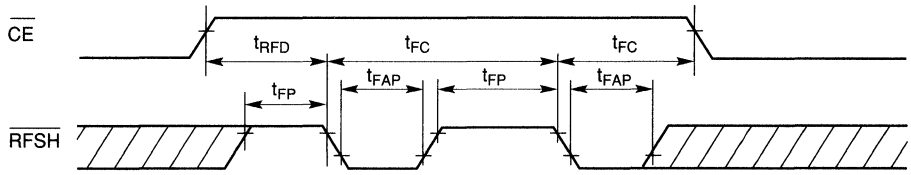
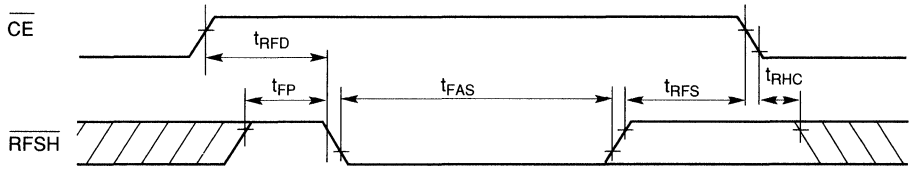
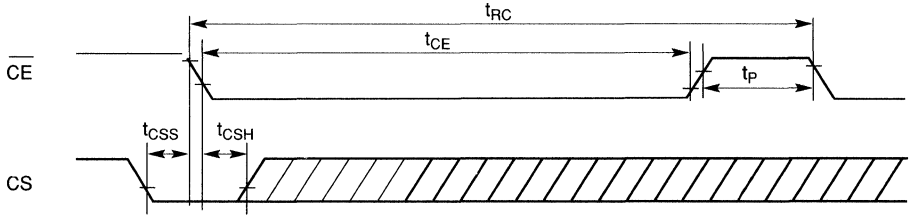
■ AUTO REFRESH CYCLE



■ SELF REFRESH CYCLE



■ CS STANDBY MODE

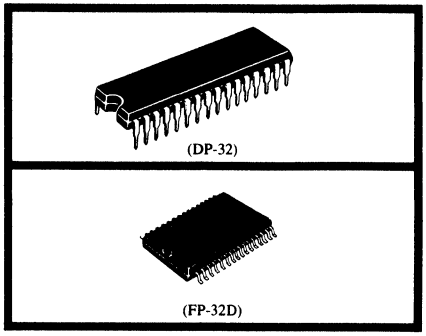


HM658512 Series

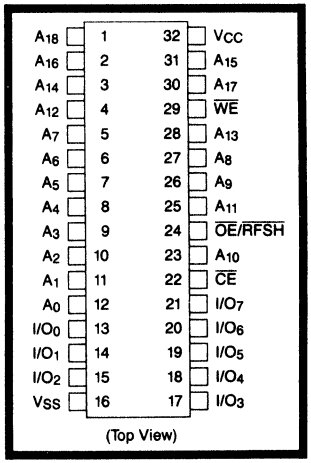
524,288-Word × 8-Bit High Speed Pseudo Static RAM

Features

- Single 5 V (± 10%)
- High speed
  - Access time
    - $\overline{CE}$ access time ..... 80/100/120 ns
  - Cycle time
    - Random read/write cycle time ..... 130/160/190 ns
- Low power
  - Active: 250 mW (typ.)
  - Standby: 200 μW (typ.)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - L/LL/LV-version ..... Address refresh
    Automatic refresh
    Self refresh
  - D-version ..... Address refresh
    Automatic refresh



■ PIN ARRANGEMENT



■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658512LP-8	80 ns	600 mil 32 pin Plastic DIP (DP-32)
HM658512LP-10	100 ns	
HM658512LP-12	120 ns	
HM658512DP-8	80 ns	
HM658512DP-10	100 ns	
HM658512DP-12	120 ns	
HM658512LP-8L	80 ns	
HM658512LP-10L	100 ns	
HM658512LP-12L	120 ns	
HM658512LP-8LV	80 ns	
HM658512LP-10LV	100 ns	
HM658512LP-12LV	120 ns	
HM658512LFP-8	80 ns	32 pin Plastic SOP (FP-32D)
HM658512LFP-10	100 ns	
HM658512LFP-12	120 ns	
HM658512DFP-8	80 ns	
HM658512DFP-10	100 ns	
HM658512DFP-12	120 ns	
HM658512LFP-8L	80 ns	
HM658512LFP-10L	100 ns	
HM658512LFP-12L	120 ns	
HM658512LFP-8LV	80 ns	
HM658512LFP-10LV	100 ns	
HM658512LFP-12LV	120 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{18}	Address
I/O_0–I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

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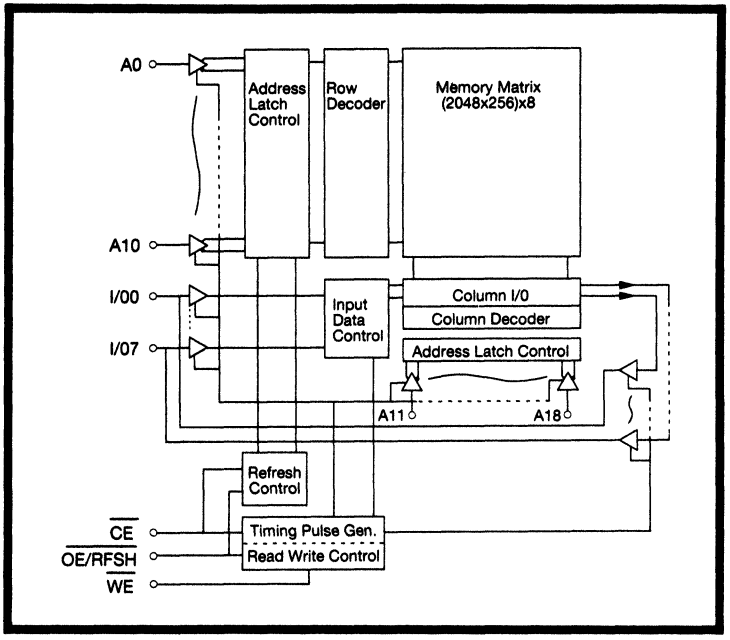
■ BLOCK DIAGRAM



Pin Functions

$\overline{CE}$: Chip Enable (Input)

$\overline{CE}$ is a basic clock. RAM is active when $\overline{CE}$ is low, and is on standby when $\overline{CE}$ is high.

A_0–A_{18}: Address Inputs (Input)

A_0–A_{10} is a row address and A_{11}–A_{18} is a column address. The entire address A_0–A_{18} is fetched into RAM by the falling edge of $\overline{CE}$.

$\overline{WE}$: Write Enable (Input)

RAM is in write mode when $\overline{WE}$ is low, and is in read mode when $\overline{WE}$ is high. I/O data is fetched into RAM by the rising edge of $\overline{WE}$ or $\overline{CE}$ (earlier timing) and the data is written into memory cells.

$\overline{OE}$/$\overline{RFSH}$: Output Enable/Refresh (Input)

This pin has two functions. Basically it works as $\overline{OE}$ when $\overline{CE}$ is low, and as $\overline{RFSH}$ when $\overline{CE}$ is high (in standby mode). After a read or write cycle finishes, refresh does not start if $\overline{CE}$ goes high while $\overline{OE}$/$\overline{RFSH}$ is held low. In order to start a refresh in standby mode, $\overline{OE}$/$\overline{RFSH}$ must go high to reset the refresh circuits of the RAM. After the refresh circuits are reset, the refresh starts when $\overline{OE}$/$\overline{RFSH}$ goes low.

I/O_0–I/O_7: Input/Output (Inputs and Outputs)

These pins are data I/O pins.

Refresh

There are three refresh modes: address refresh, automatic refresh, and self refresh.

(1) Address refresh

Data is refreshed by accessing all 2048 row addresses every 32 ms. A read is one method of accessing those addresses. Each row address (2048 addresses of A_0-A_{10}) must be read at least once every 32 ms. In address refresh mode, $\overline{OE}$/$\overline{RFSH}$ can remain high. In this case, the I/O pins remain at high impedance, but the refresh is done within RAM.

(2) Automatic refresh

Instead of address refresh, automatic refresh can be used. RAM goes to automatic refresh mode if $\overline{OE}$/$\overline{RFSH}$ falls while $\overline{CE}$ is high and it remains low for at least t_{FAP}. One automatic refresh cycle is executed by one low pulse of $\overline{OE}$/$\overline{RFSH}$. It is not necessary to input the refresh address from outside since it is generated internally by an on-chip address counter. 2048 automatic refresh cycles must be done every 32 ms.

(3) Self refresh

Self refresh mode is suitable for data retention by battery. In standby mode, a self refresh starts automatically when $\overline{OE}$/$\overline{RFSH}$ stays low for more than 8 μs. Refresh addresses are automatically specified by the on-chip address counter, and the refresh period is determined by the on-chip timer.

Automatic refresh and self refresh are distinguished from each other by the width of the $\overline{OE}/\overline{RFSH}$ low pulse in standby mode. If the $\overline{OE}/\overline{RFSH}$ low pulse is wider than 8 μs, RAM changes into self refresh mode; if the $\overline{OE}/\overline{RFSH}$ low pulse is less than 8 μs, it is recognized as an automatic refresh instruction.

Notes on Using the HM658512

Since pseudo static RAM consists of dynamic circuits like DRAM, it is more noise-sensitive than conventional SRAM.

(1) If a short $\overline{CE}$ pulse of a width less than t_{CE} min. is applied to RAM, an incomplete read occurs and stored data may be destroyed. Make sure that $\overline{CE}$ low pulses of less than t_{CE} min. are inhibited. Note that a 10 ns $\overline{CE}$ low pulse may sometimes occur owing to the gate delay on the board if the CE signal is generated by the decoding of higher address signals on the board. Avoid these short pulses.

(2) $\overline{OE}/\overline{RFSH}$ works as refresh control in standby mode. A short $\overline{OE}/\overline{RFSH}$ low pulse may cause an incomplete refresh that will destroy data. Make sure that $\overline{OE}/\overline{RFSH}$ low pulses of less than t_{FAP} min. are also inhibited.

(3) t_{OHC} and t_{OCD} are the timing specs which distinguish the $\overline{OE}$ function of $\overline{OE}/\overline{RFSH}$ from the $\overline{RFSH}$ function. The t_{OHC} and t_{OCD} specs must be strictly maintained.

(4) Start the HM658512 operating by executing at least eight initial cycles (dummy cycles) at least 100 μs after the power voltage reaches 4.5V–5.5V after power-on.

■ FUNCTION TABLE

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh
H	H	X	High-Z	Standby

NOTE: 1. X means don't care.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_A = 0°C to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−1.0*1	—	0.8	V

NOTES: 1. V_{IL} min. = −3.0V for pulse width 30 ns.

■ DC CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating Power Supply Current	I_{CC1}	—	—	75	mA	$I_{I/O}$ = 0, t_{cyc} = min.
Standby Power Supply Current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IH}, V_{IN} ≥ 0V
	I_{SB2}	—	20	200 100*2	μA	$\overline{CE}$ ≥ V_{CC} -0.2V $\overline{OE}/\overline{RFSH}$ ≥ V_{CC} -0.2V V_{IN} ≥ 0V
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	—	1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IL}, V_{IN} ≥ 0V
	I_{CC3}	—	70*1 40*2	200*1 100*2	μA	$\overline{CE}$ ≥ V_{CC} -0.2V $\overline{OE}/\overline{RFSH}$ ≤ 0.2V V_{IH}, V_{IN} ≥ 0V
Input Leakage Current	I_{LI}	-10	—	10	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	-10	—	10	μA	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = -1 mA

NOTES: 1. Only for L-Version.
2. Only for LL/LV-Version.

■ CAPACITANCE

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	8	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Test Conditions

Input pulse levels: 2.4V, 0.4V
Input rise and fall times: 5 ns
Timing measurement level: 2.2V, 0.8V
Reference level: V_{OH} = 2.0V, V_{OL} = 0.8V
Output load: 1 TTL and 100 pF

■ AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

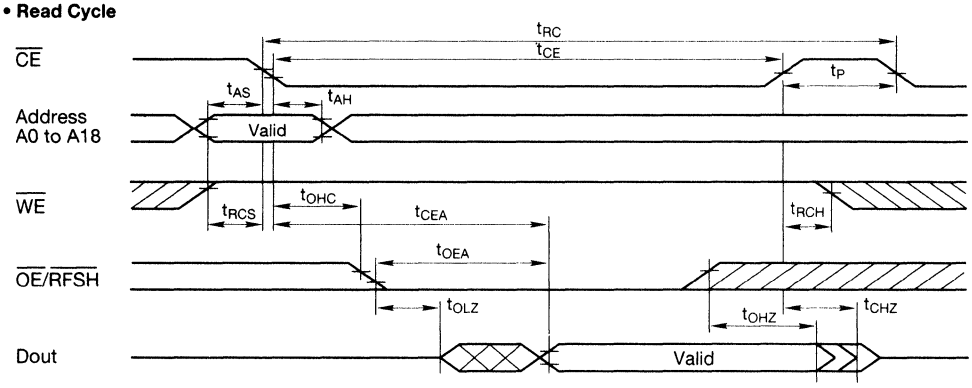
Item	Symbol	HM658512-8		HM658512-10		HM658512-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	190	—	ns	
Chip Enable Access Time	t_{CEA}	—	80	—	100	—	120	ns	
Read-Modify-Write Cycle Time	t_{RWC}	180	—	220	—	260	—	ns	
Output Enable Access Time	t_{OEA}	—	30	—	40	—	50	ns	
Chip Disable to Output in High-Z	t_{CHZ}	0	25	0	25	0	30	ns	1
Chip Enable to Output in Low-Z	t_{CLZ}	20	—	20	—	20	—	ns	2
Output Disable to Output in High-Z	t_{OHZ}	—	25	—	25	—	30	ns	1
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns	2
Chip Enable Pulse Width	t_{CE}	80 ns	10 μs	100 ns	10 μs	120 ns	10 μs		
Chip Enable Pre-Charge Time	t_P	40	—	50	—	60	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	20	—	25	—	30	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Write Command Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns	
Chip Enable to Output Enable Delay Time	t_{OCD}	0	—	0	—	0	—	ns	
Output Enaole Hold Time	t_{OHC}	15	—	15	—	15	—	ns	
Data in to End of Write	t_{DW}	20	—	25	—	30	—	ns	
Data in Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns	
Output Active From End of Write	t_{OW}	5	—	5	—	5	—	ns	2
Write to Output in High-Z	t_{WHZ}	—	20	—	25	—	30	ns	1
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
Refresh Command Delay Time	t_{RFD}	40	—	50	—	60	—	ns	
Refresh Precharge Time	t_{FP}	40	—	40	—	40	—	ns	
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80 ns	8 μs	80 ns	8 μs	80 ns	8 μs		
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	190	—	ns	
Refresh Command Pulse Width for Self Refresh	t_{FAS}	8	—	8	—	8	—	μs	
Refresh Reset Time From Self Refresh	t_{RFS}	600	—	600	—	600	—	ns	
Refresh Period	t_{REF}	—	32	—	32	—	32	ms	2048 cycle

NOTES:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} (min.) and V_{IL} (max.).
7. After power-up, pause for more than 100 μs and execute at least 8 initialization cycles, preferably as 8 refresh cycles.
8. 2048 cycles of burst refresh or distributed automatic refresh must be executed within 15 μs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycle.

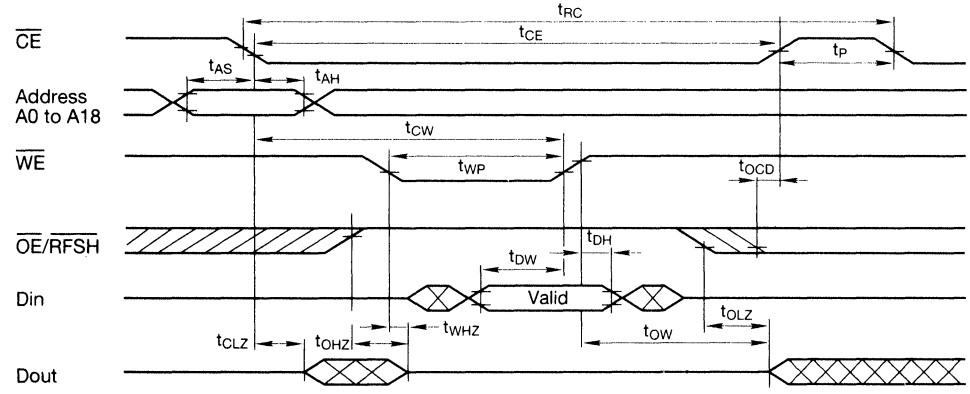
4

■ TIMING WAVEFORMS

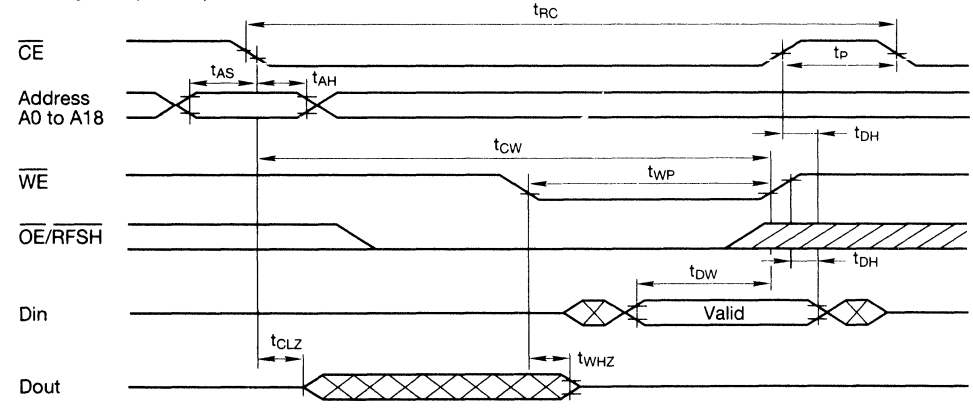
• Read Cycle



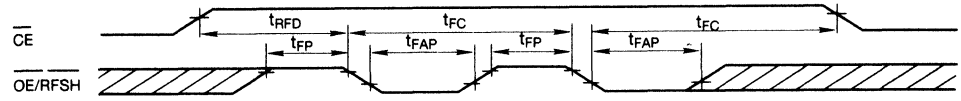
• Write Cycle (1) ($\overline{OE}$ High)



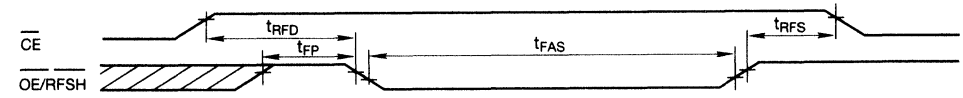
• Write Cycle (2) ($\overline{OE}$ Low)



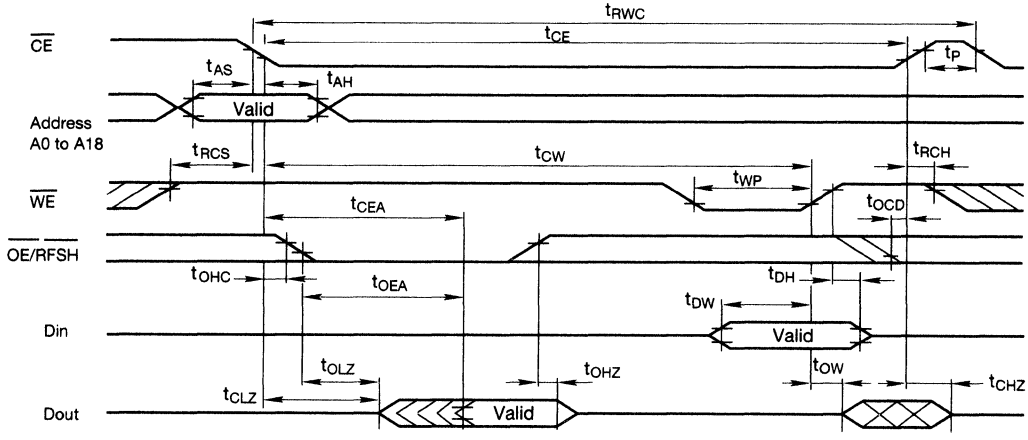
• **Automatic Refresh Cycle**



• **Self Refresh Cycle**



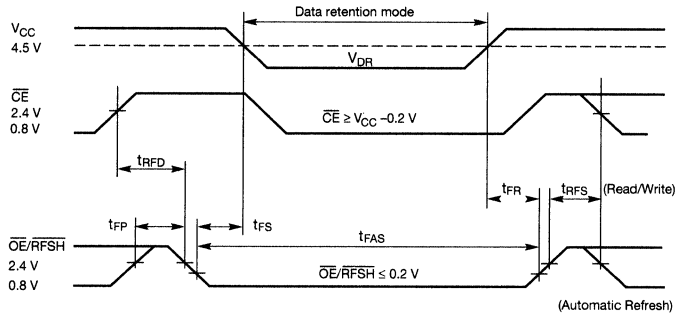
• **Read-Modify-Write Cycle**



• **Low V_{CC} Data Retention Characteristics** Ta=0 to 70°C. This characteristic is guaranteed only for LV-version.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	4.0	—	5.5	V	
Self refresh current	I_{CCDR}			50	μA	V_{CC}=4.0 V $\overline{CE} \geq V_{CC}$ -0.2 V $\overline{OE}/\overline{RFSH} \leq 0.2$ V $V_{in} \geq 0$ V
				100	μA	V_{CC} = 5.5 V $\overline{CE} \geq V_{CC}$ -0.2 V $\overline{OE}/\overline{RFSH} \leq 0.2$ V $V_{in} \geq 0$ V
Refresh setup time	t_{FS}	0			ns	
Operation recovery time	t_{FR}	5			ms	

• Low V_{CC} Data Retention Timing Waveform



Notes: 1. t_R (rise time), t_F (fall time) of power supply voltage must be smaller than 0.05 V/ms.
2. Keep $\overline{CE} \geq V_{CC}$ -0.2 V during data retention mode.
3. Regarding t_{RFD}, t_{FP}, t_{FAS} and t_{RFS}, refer to AC characteristics.

Section 5
ECL RAM

5

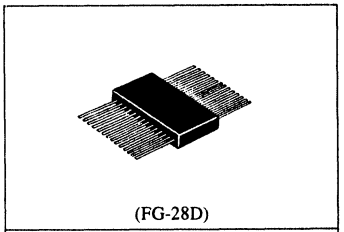
HITACHI®

HM10494 Series

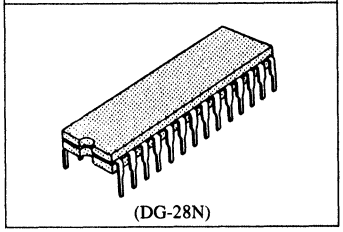
16384-word × 4-bit Fully Decoded Random Access Memory

Description

The HM10494 is ECL 10K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.



(FG-28D)



(DG-28N)

Features

- 16384-word × 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6 ns (min)
- Low power dissipation: 800 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

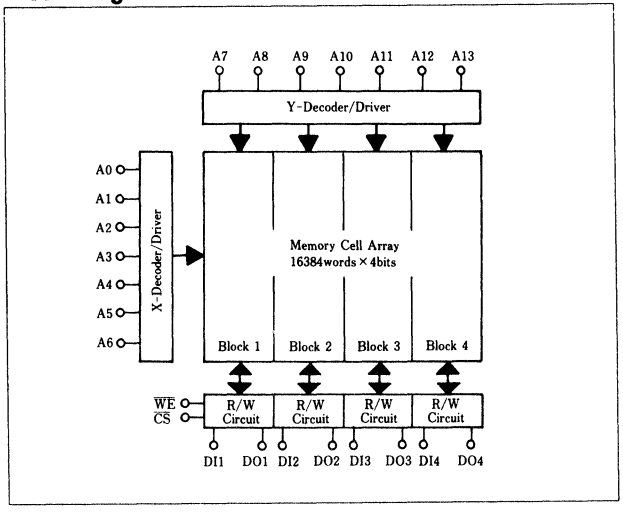
Type No.	Access Time	Package
HM10494-10	10 ns	400 mil 28 pin Cerdip
HM10494-12	12 ns	(DG-28N)
HM10494F-10	10 ns	28 pin Ceramic Flat
HM10494F-12	12 ns	(FG-28D)

Function Table

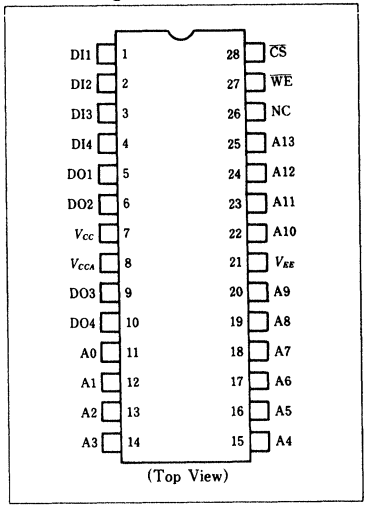
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



(Top View)

HITACHI

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature	Tstg (Bias)*1	−55 to +125	°C

Note: *1; Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = −5.2V, R_L = 50Ω to −2.0 V, Ta = 0 to +75°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions	
Output Voltage	V_{OH}	−1000	—	−840	mV	Vin = V_{IHA} or V_{ILB}	0°C
		−960	—	−810			+25°C
		−900	—	−720			+75°C
	V_{OL}	−1870	—	−1665			0°C
		−1850	—	−1650			+25°C
		−1830	—	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	—	—	mV	Vin = V_{IHB} or V_{ILA}	0°C
		−980	—	—			+25°C
		−920	—	—			+75°C
	V_{OLC}	—	—	−1645			0°C
		—	—	−1630			+25°C
		—	—	−1605			+75°C
Input Voltage	V_{IH}	−1145	—	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1105	—	−810			+25°C
		−1045	—	−720			+75°C
	V_{IL}	−1870	—	−1490		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	—	−1475			+25°C
		−1830	—	−1450			+75°C
Input Current	I_{IH}	—	—	220	μA	Vin = V_{IHA}	0 to +75°C
	I_{IL}	0.5	—	170		Vin = V_{ILB} $\overline{CS}$	0 to +75°C
		−50	—	—		Vin = V_{ILB} Others	0 to +75°C
Supply Current	I_{EE}	−180	—	—	mA	All Inputs and Outputs Open	Ta = 0°C
		−180	—	—			Ta = 75°C

AC Characteristics (V_{EE} = −5.2 V ± 5%, Ta = 0 to +75°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

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Write Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	t_W	6	—	—	8	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	tw = tw min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

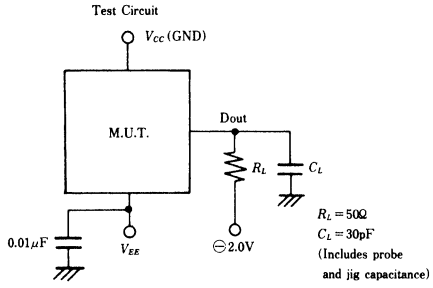
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

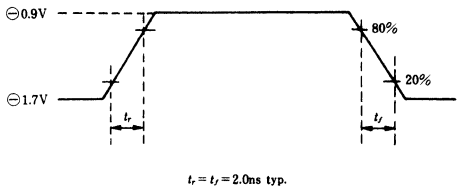
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

Loading Condition

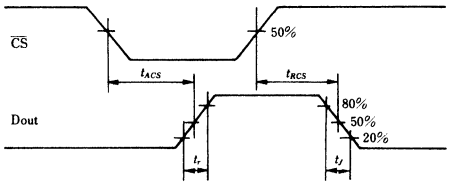


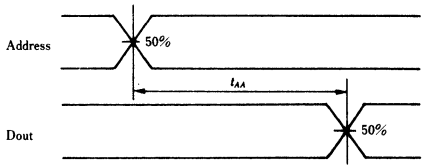
Input Pulse



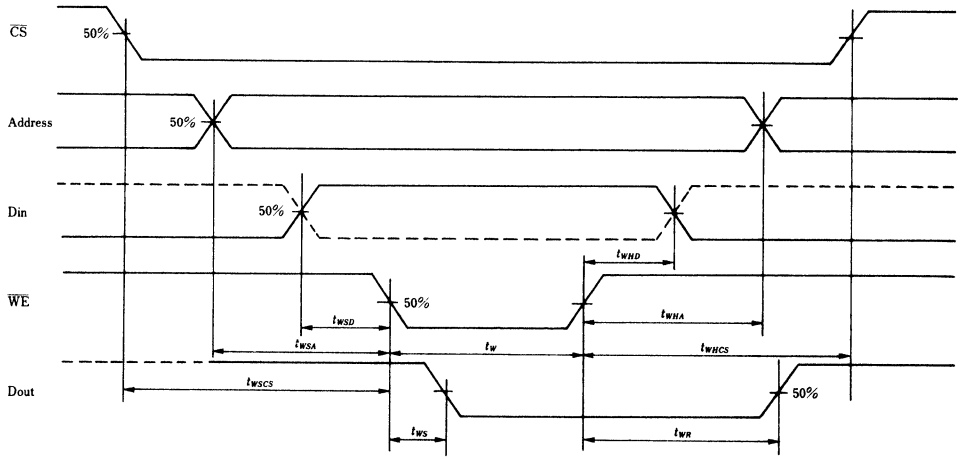
$t_r = t_f = 2.0$ns typ.

Read Mode





Write Mode



5

HM10490 Series

65536-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

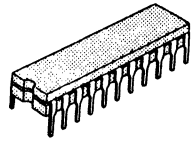
The HM10490 is ECL 10K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

■ FEATURES

- 65536 × 1 Bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .6/8ns (min.)
- Low Power Dissipation . . . . . .570mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

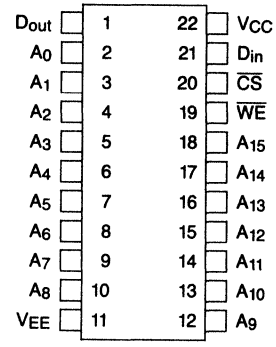
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM10490-10 HM10490-12	10ns 12ns	300 mil 22 pin Cerdip (DG-22N)



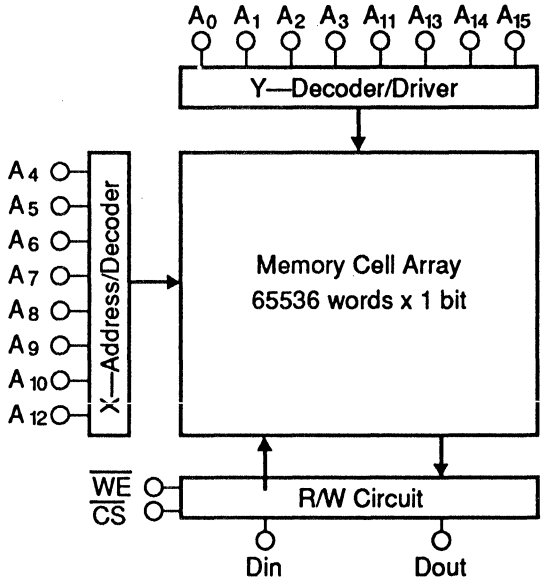
(DG-22N)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$*	Θ55 to +125	°C

NOTE: * = Under bias.

■ DC CHARACTERISTICS (V_{EE} = Θ5.2V, R_L = 50Ω to Θ2.0V, T_a = 0 to +75°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}	0°C	Θ1000	—	Θ840	mV
			+25°C	Θ960	—	Θ810	
			+75°C	Θ900	—	Θ720	
	V_{OL}		0°C	Θ1870	—	Θ1665	
			+25°C	Θ1850	—	Θ1650	
			+75°C	Θ1830	—	Θ1625	
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}	0°C	Θ1020	—	—	mV
			+25°C	Θ980	—	—	
			+75°C	Θ920	—	—	
	V_{OLC}		0°C	—	—	Θ1645	
			+25°C	—	—	Θ1630	
			+75°C	—	—	Θ1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	Θ1145	—	Θ840	mV
			+25°C	Θ1105	—	Θ810	
			+75°C	Θ1045	—	Θ720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	Θ1870	—	Θ1490	
			+25°C	Θ1850	—	Θ1475	
			+75°C	Θ1830	—	Θ1450	
Input Current	I_{IH}	V_{in} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0 to +75°C	0.5	—	170
			Others		Θ50	—	—
Supply Current	I_{EE}	All Inputs and Outputs Open	0°C, 75°C	Θ140	—	—	mA

■ AC CHARACTERISTICS (V_{EE} = Θ5.2V ± 5%, T_a = 0 to +75°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM10490-10			HM10490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Write Pulse Width	t_W	$t_{WSA} = t_{WSA}$ min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_W$ min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

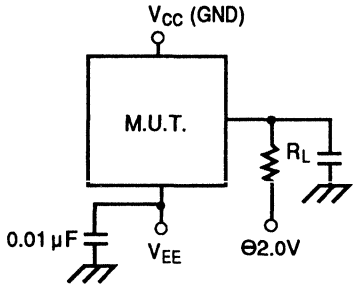
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

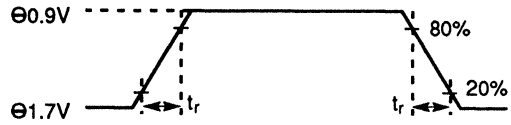
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

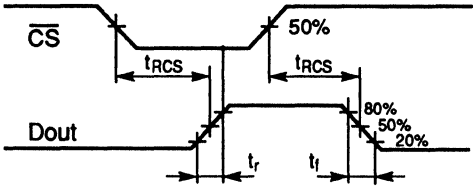
1. Loading Condition

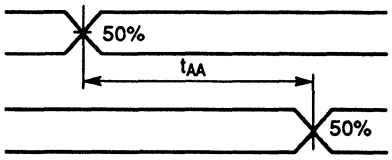


2. Input Pulse

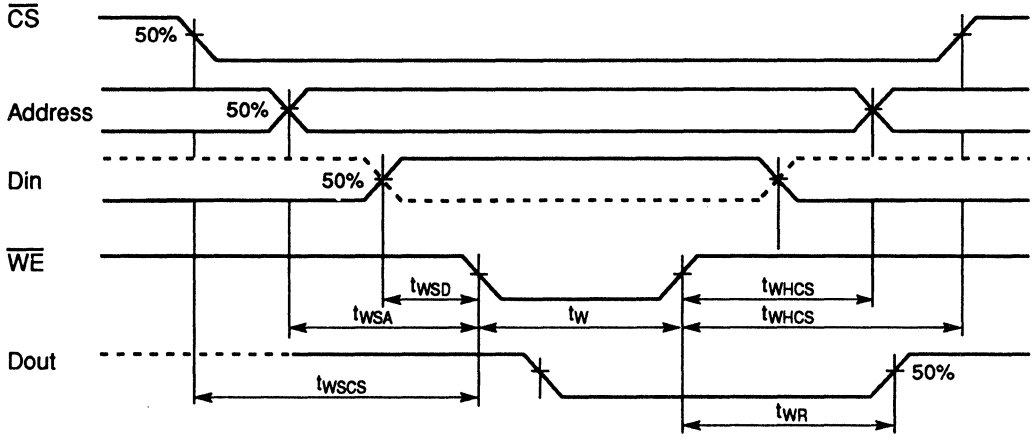


3. Read Mode





4. Write Mode



HM10500 Series

Preliminary

262,144 Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

HM10500-15 is ECL 10K compatible, 262,144-words × 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

■ FEATURES

- 262,144-words × 1-bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time. . . . . .15ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .520mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

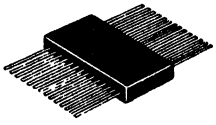
Type No.	Access Time	Package
HM10500-15	15ns	300 mil 24 pin Cerdip (DG-24V)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out} *1	Read

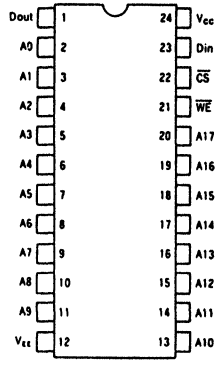
NOTES: X = Irreievant

*1 = Read Out Noninvert



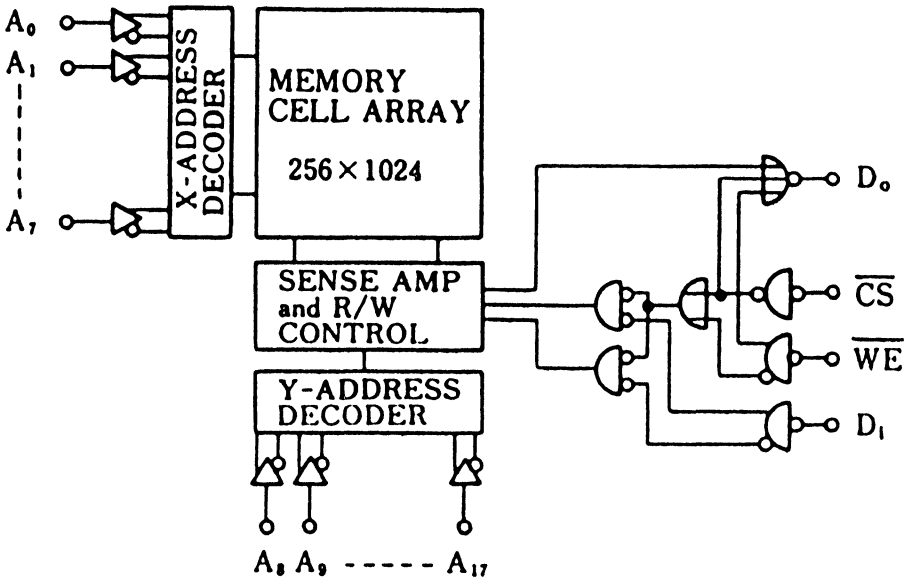
(DG-24V)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



5

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{In}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

Electrical Characteristics

DC Characteristics (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min (B)	typ	max (A)	Unit	Test Condition	
Output Voltage	V_{OH}	−1000	–	−840	mV	V_{in}=V_{IHA} or V_{ILB}	0°C
		−960	–	−810			+25°C
		−900	–	−720			+75°C
	V_{OL}	−1870	–	−1665			0°C
		−1850	–	−1650			+25°C
		−1830	–	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	–	–	mV	V_{in}=V_{IHB} or V_{ILA}	0°C
		−980	–	–			+25°C
		−920	–	–			+75°C
	V_{OLC}	–	–	−1645			0°C
		–	–	−1630			+25°C
		–	–	−1605			+75°C
Input Voltage	V_{IH}	−1145	–	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1105	–	−810			+25°C
		−1045	–	−720			+75°C
	V_{IL}	−1870	–	−1490		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	–	−1475			+25°C
		−1830	–	−1450			+75°C
Input Current	I_{IH}	–	–	220	μA	V_{in}=V_{IHA}	0 to +75°C
	I_{IL}	0.5	–	170		$\overline{CS}$ — V_{in}=V_{ILB}	0 to +75°C
		−50	–	–		Others	
Supply Current	I_{EE}	−180	–	–	mA	All Inputs and Outputs Open, Test Pin 12	Ta=0°C
		−180	–	–			Ta=75°C

AC Characteristics (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	–	–	15	ns	
Chip Select Recovery Time	t_{RCS}	–	–	10	ns	
Address Access Time	t_{AA}	–	–	15	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	10	–	–	ns	t_{WSA}=2ns
Data Setup Time	t_{WSD}	2	–	–	ns	
Data Hold Time	t_{WHD}	3	–	–	ns	
Address Setup Time	t_{WSA}	2	–	–	ns	t_W=10ns
Address Hold Time	t_{WHA}	3	–	–	ns	
Chip Select Setup Time	t_{WSCS}	2	–	–	ns	
Chip Select Hold Time	t_{WHCS}	3	–	–	ns	
Write Disable Time	t_{WS}	–	–	10	ns	
Write Recovery Time	t_{WR}	–	–	18	ns	

Rise/Fall Time

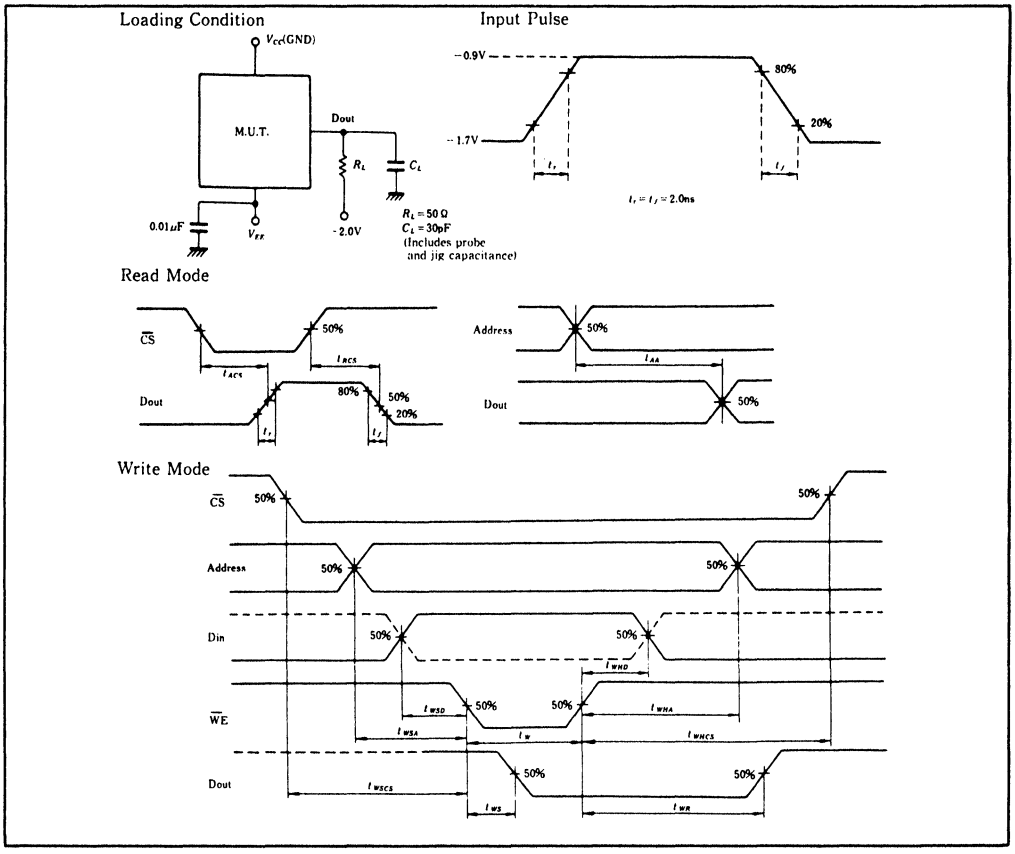
Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	–	2	–	ns	
Output Fall Time	t_f	–	2	–	ns	

Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	C_{in}	–	3	–	pF	
Output Capacitance	C_{out}	–	5	–	pF	

5

Test Circuit and Waveforms

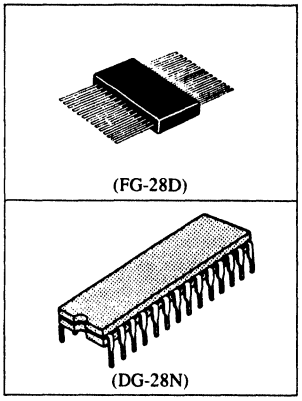


HM100494 Series

16384-word × 4-bit Fully Decoded Random Access Memory

Description

The HM100494 is ECL 100K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.



Features

- 16384-word × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6 ns (min)
- Low power dissipation: 650 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

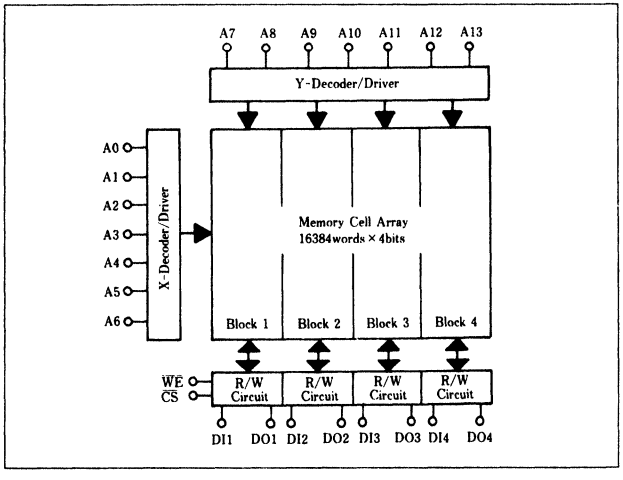
Type No.	Access Time	Package
HM100494-10	10 ns	400 mil 28-pin Cerdip
HM100494-12	12 ns	(DG-28N)
HM100494F-10	10 ns	28-pin Ceramic Flat
HM100494F-12	12 ns	(FG-28D)

Function Table

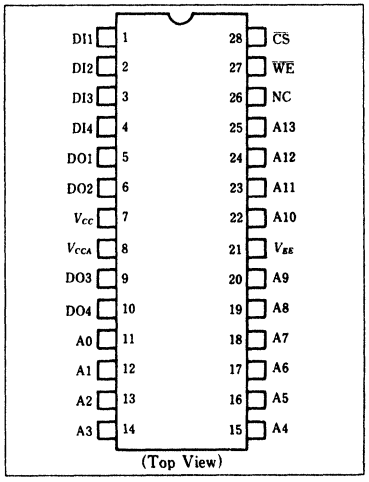
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



5

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature	Tstg (Bias)[1]*	−55 to +125	°C

Note: *1: Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = −4.5 V, R_L = 50Ω to −2.0 V, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Input Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		−50	—	—		Others
Supply Current	I_{EE}	−180	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = −4.5 V ± 5%, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM100494-10			HM100494-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM100494-10			HM100494-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	tw	6	—	—	8	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	tw = tw min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

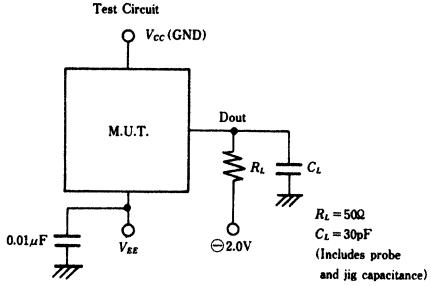
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

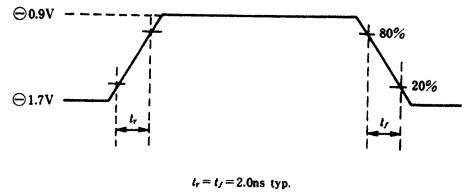
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

Loading Condition

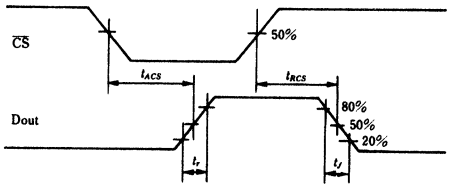


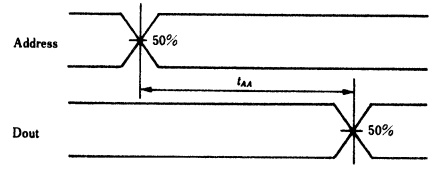
Input Pulse



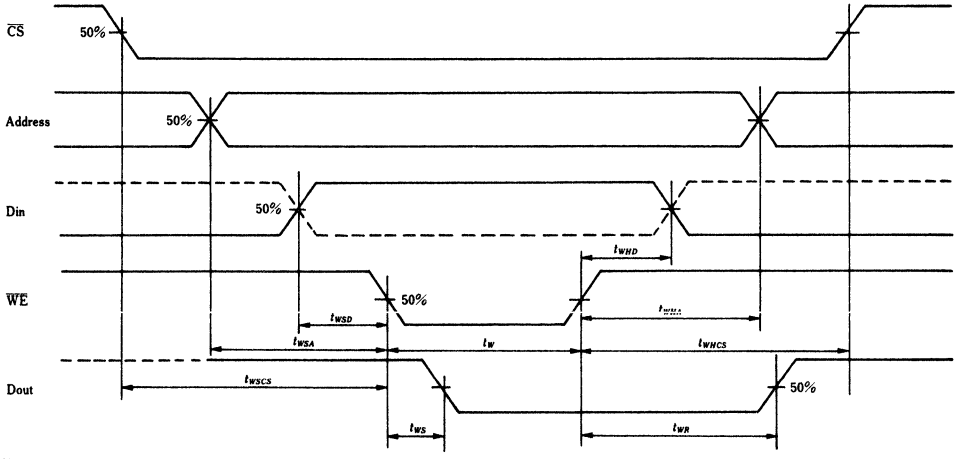
$t_r = t_f = 2.0$ns typ.

Read Mode





Write Mode



HM100504 Series — Preliminary

65,536-Words x 4-Bit Random Access Memory

■ DESCRIPTION

The Hitachi HM100504 is ECL 100k compatible, 65,536 words by 4 bits read/write random access memory developed for high speed systems such as cache and control/buffer storage.

■ FEATURES

- 65,536-words x 4 bit organization
- Fully compatible with 100k ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 10/12 ns (max.)
- Write pulse width: 7/9 ns (min.)
- Low power dissipation: 500 mW (typ.)
- Output obtainable by wired-OR (open emitter)

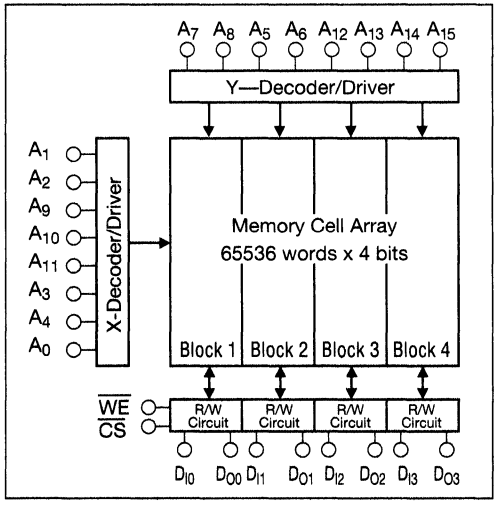
■ ORDERING INFORMATION

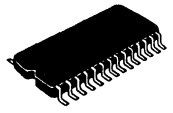
Type No.	Access Time	Package
HM100504F-10 HM100504F-12	10 ns 12 ns	28 pin Ceramic Flat (30 mil Lead Pitch) FG-28DA

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{15}	Address Input
D_{I0}–D_{I3}	Data Input
D_{O0}–D_{O3}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

■ BLOCK DIAGRAM

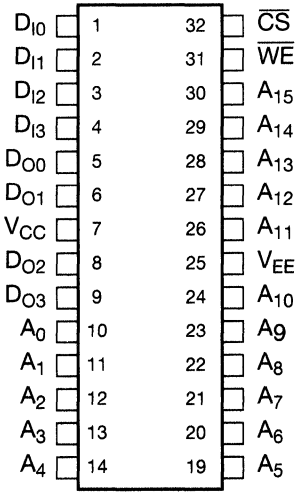




FG-28DA

■ PIN ARRANGEMENT

HM100504 Series



(Top View)

5

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X[1]	X[1]	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X[1]	D_{out}[2]	Read

Notes: 1. Irrelevant
2. Read Out Noninvert

■ ABSOLUTE MAXIMUM RATING (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	–30	mA
Storage Temperature	T_{stg}	–65 to +150	°C
Storage Temperature	T_{stg} (bias)[1]	–55 to +125	°C

Note: 1. Under bias (V_{EE} = 6.0V min.)

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = –4.5V, R_L = 50Ω to –2.0V, T_C = 0 to +85°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	V_{in} = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	V_{in} = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	–1810	—	–1475	mV	
Input Current	I_{IH}	—	—	220	µA	V_{in} = V_{IHA}
	I_{IL}	0.5	—	170	µA	V_{in} = V_{ILB} ($\overline{CS}$)
		–50	—	—	µA	V_{in} = V_{ILB} (Others)
Supply Current	I_{EE}	–180	—	—	mA	All Inputs and Outputs Open

■ AC CHARACTERISTICS (V_{EE} = –4.5V ± 5%, T_c = 0 to +85°C)

• Read Mode

Item	Symbol	HM100504-10			HM100504-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	7	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	7	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

• **Write Mode**

Item	Symbol	HM100504-10			HM100504-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	tW	7	—	—	9	—	—	ns	tWSA = tWSA min
Data Setup Time	tWSD	1	—	—	1	—	—	ns	
Data Hold Time	tWHD	1	—	—	1	—	—	ns	
Address Setup Time	tWSA	1	—	—	1	—	—	ns	tW = tW min
Address Hold Time	tWHA	2	—	—	2	—	—	ns	
Chip Select Setup Time	tWSCS	1	—	—	1	—	—	ns	
Chip Select Hold Time	tWHCS	1	—	—	1	—	—	ns	
Write Disable Time	tWS	—	—	6	—	—	6	ns	
Write Recovery Time	tWR	—	—	12	—	—	14	ns	

• **Rise/Fall Time**

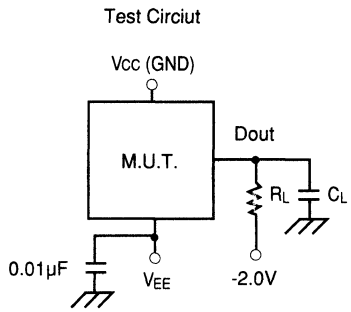
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

• **Capacitance**

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	C_{in}	3	pF			
Output Capacitance	C_{OUT}	5	pF			

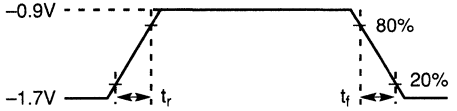
■ TEST CIRCUIT AND WAVEFORMS

1. Loading Condition



R_L = 50Ω
C_L = 30pF
(Includes probe and jig capacitance)

2. Input Pulse

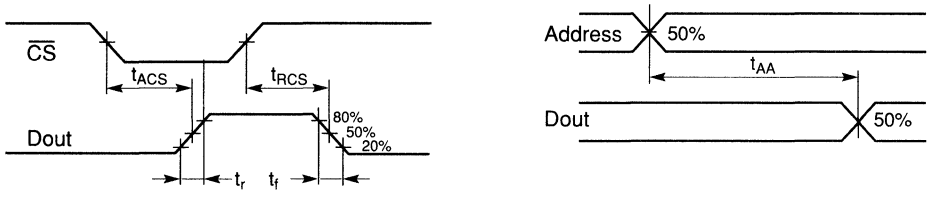


t_r = t_f = 2.0ns typ

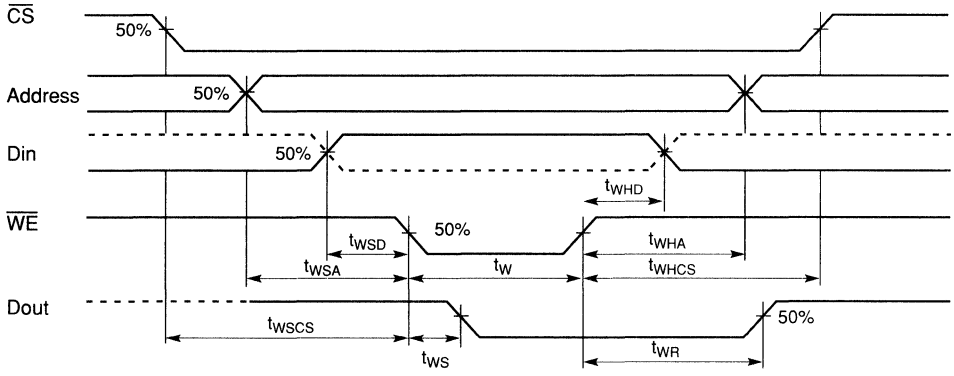
5

■ TIMING WAVEFORM

3. Read Mode



4. Write Mode



HM100500 Series — Preliminary

262,144-Word × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM100500CG-18 is ECL 100K compatible, 262,144-word × 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

■ FEATURES

- 262,144-Word × 1-Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time. . . . . .18ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM100500-18	18ns	24 pin CERDIP (DG-24V)
HM100500CG-18	18ns	28 pin LCC (CG-28B)
HM100500F-18	18ns	24 pin Ceramic Flat (FG-24A)

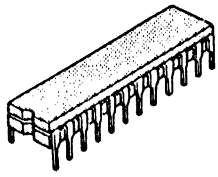
■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*1	Read

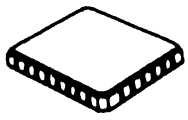
NOTES: X = Irrelevant

*1 = Read Out Noninvert

(FG-24A)



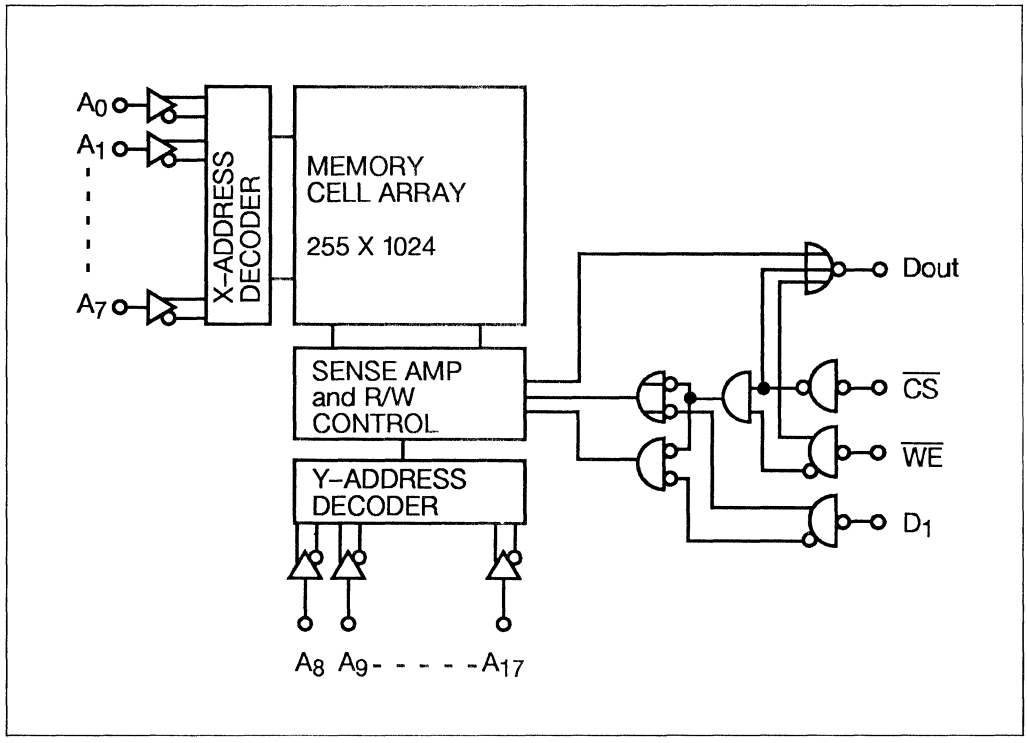
(DG-24V)



(CG-28B)

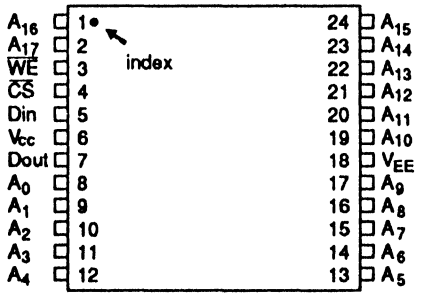
5

BLOCK DIAGRAM



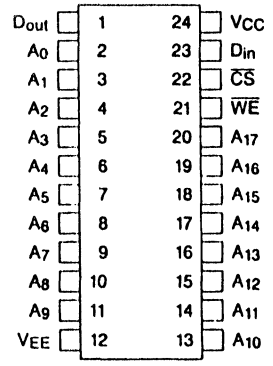
Pin Arrangement

(FG-24A)



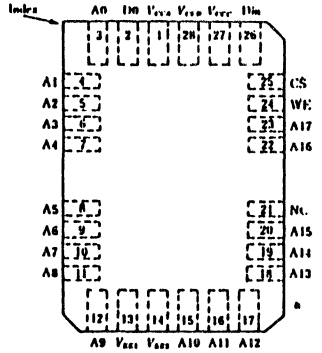
(Top View)

(DG-24V)



(Top View)

(CG-28B)



(Top View)

5

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature	Tstg (Bias)*1	−55 to +125	°C

Note: *1; UnderBias

Electrical Characteristics

DC Characteristics (V_{EE} = −4.5 V, R_L = 50Ω to −2.0 V, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions
Output Voltage	V_{OH}	−1025	−955	−880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Input Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		−50	—	—		Vin = V_{ILB} Others
Supply Current	I_{EE}	−160	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = −4.5 V ± 5%, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	Min	Typ	CG-18 Max	F-18 Max	Unit	Test Conditions
Chip Select Access Time	t_{ACS}	—	—	18	15	ns	
Chip Select Recovery Time	t_{RCS}	—	—	18	10	ns	
Address Access Time	t_{AA}	—	—	18	18	ns	

Write Mode

Item	Symbol	Min	Typ	CG-18 Max	F-18 Max	Unit	Test Conditions
Write Pulse Width	tw	10	—	—		ns	t_{WSA} = 2 ns
Data Setup Time	t_{WSD}	2	—	—			
Data Hold Time	t_{WHD}	3	—	—		ns	
Address Setup Time	t_{WSA}	2	—	—		ns	t_W = 10 ns
Address Hold Time	t_{WHA}	3	—	—		ns	
Chip Select Setup Time	t_{WSCS}	2	—	—		ns	
Chip Select Hold Time	t_{WHCS}	3	—	—		ns	
Write Disable Time	t_{WS}	—	—	15	10	ns	
Write Recovery Time	t_{WR}	—	—	21	21	ns	

Rise/Fall Time

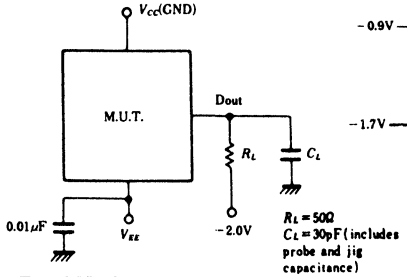
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

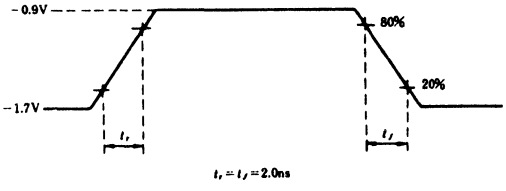
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

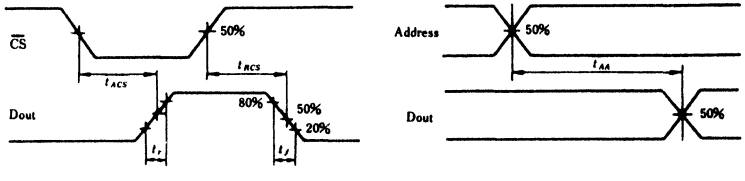
Loading Condition



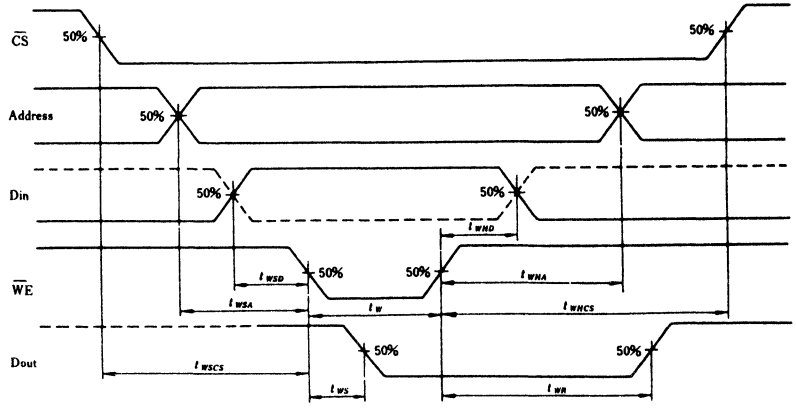
Input Pulse



Read Mode



Write Mode



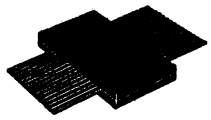
5

HM100514 Series — Preliminary

262,144-words x 4-bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM100514 is ECL 100k compatible, 262,144-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

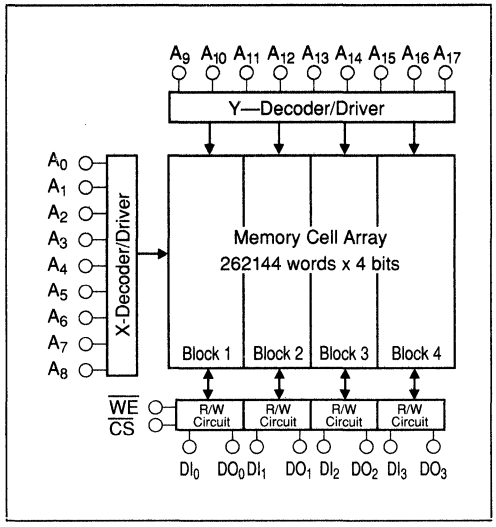


(FG-32D)

■ FEATURES

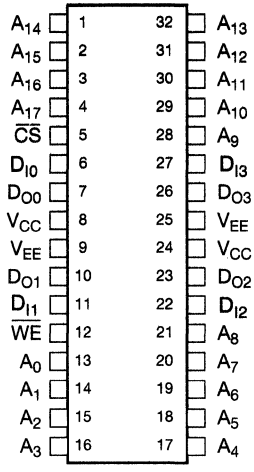
- 262,144 x 4-bit organization
- Fully compatible with 100k ECL level
- Address access time: 15 ns (max.)
- Write pulse width: 9 ns (min.)
- Low power dissipation: 800 mW (typ.)
- Output obtainable by wired-OR (open emitter)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

HM100514 Series



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A17	Address Input
DI0–DI3	Data Input
DO0–DO3	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
VCC	Ground
VEE	Supply Voltage

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

Notes: X: Irrelevant
*: Read Out Noninvert

■ ABSOLUTE MAXIMUM RATING (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	–30	mA
Storage Temperature	T_{stg}	–65 to +150	°C
Storage Temperature	T_{stg} (bias)*	–55 to +125	°C

Note: 1. Under bias (V_{EE} = 6.0V min.)

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = –4.5V, R_L = 50Ω to –2.0V, T_C = 0 to +85°C)[2]

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	V_{in} = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	V_{in} = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	–1810	—	–1475	mV	
Input Current	I_{IH}	—	—	220	µA	V_{in} = V_{IHA}
	I_{IL}	0.5	—	170	µA	V_{in} = V_{ILB} ($\overline{CS}$)
		–50	—	—	µA	V_{in} = V_{ILB} (Others)
Supply Current	I_{EE}	–180	—	—	mA	All Outputs Open

■ AC CHARACTERISTICS (V_{EE} = –4.5V ± 5%, T_c = 0 to +85°C)[2]

• Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	10	ns	
Chip Select Recovery Time	t_{RCS}	—	—	10	ns	
Address Access Time	t_{AA}	—	—	15	ns	

5

• Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Write Pulse Width	t_W	9	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	ns	t_W = t_W min
Address Hold Time	t_{WHA}	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	15	ns	
Write Recovery Time	t_{WR}	—	—	17	ns	

• Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	t_r	—	1	—	ns	
Output Fall Time	t_f	—	1	—	ns	

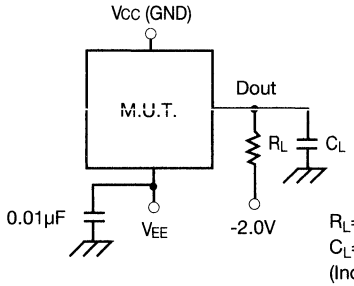
• Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{OUT}	—	5	—	pF	

■ TEST CIRCUIT AND WAVEFORMS

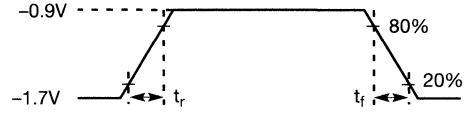
• Loading Condition

Test Circuit



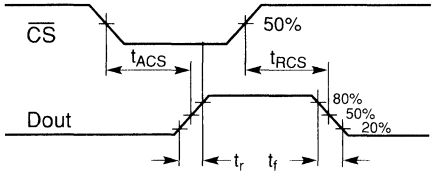
R_L=50Ω
C_L=30pF
(Includes probe
and jig capacitance)

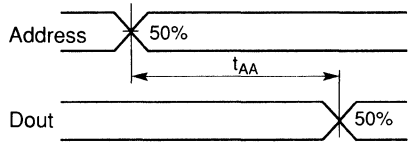
• Input Pulse



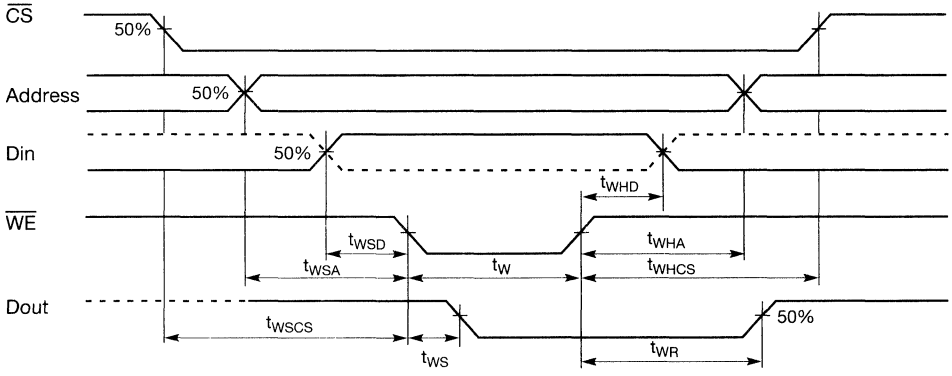
t_r=t_f=2.0ns typ

- **Read Mode**





- **Write Mode**



5

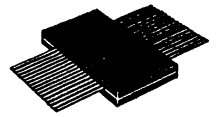
HM100510 Series

Preliminary

1,048,576-words x 1-Bit Random Access Memory

■ DESCRIPTION

The Hitachi HM100510 is ECL 100k compatible, 1,048,576 words by 1 bit read/write random access memory developed for high speed systems.



(FG-28DB)

■ FEATURES

- 1,048,576-words x 1 bit organization
- Fully compatible with 100k ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 15 ns (max.)
- Write pulse width: 9 ns (min.)
- Low power dissipation: 700 mW (typ.)
- Output obtainable by wired-OR (open emitter)

■ ORDERING INFORMATION

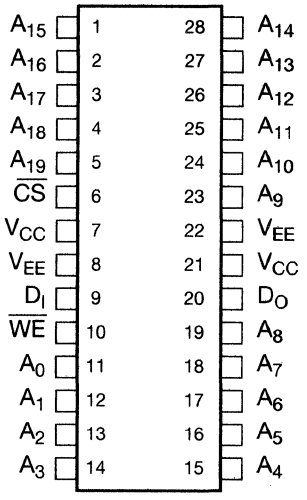
Type No.	Access Time	Package
HM100510F-15	15 ns	28 pin Ceramic Flat (30 mil Lead Pitch) (FG-28DB)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{19}	Address Input
D_I	Data Input
D_O	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

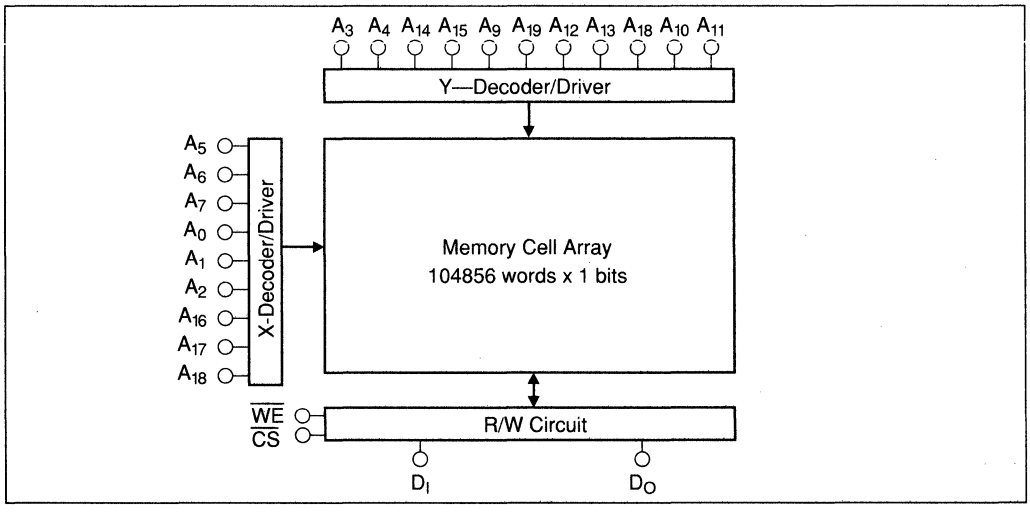
■ PIN ARRANGEMENT

HM100510 Series



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X[1]	X[1]	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X[1]	D_{out}[2]	Read

Notes: 1. Irrelevant
2. Read Out Noninvert

■ ABSOLUTE MAXIMUM RATING (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	–30	mA
Storage Temperature	T_{stg}	–65 to +150	°C
Storage Temperature	T_{stg} (bias)[1]	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0V min.)

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = –4.5V, R_L = 50Ω to –2.0V, T_C = 0 to +85°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	V_{in} = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	V_{in} = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	–1810	—	–1475	mV	
Input Current	I_{IH}	—	—	220	µA	V_{in} = V_{IHA}
	I_{IL}	0.5	—	170	µA	V_{in} = V_{ILB} ($\overline{CS}$)
		–50	—	—	µA	V_{in} = V_{ILB} (Others)
Supply Current	I_{EE}	–180	—	—	mA	All Outputs Open

■ AC CHARACTERISTICS (V_{EE} = –4.5V ± 5%, T_c = 0 to +85°C)

• Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	10	ns	
Chip Select Recovery Time	t_{RCS}	—	—	10	ns	
Address Access Time	t_{AA}	—	—	15	ns	

5

• Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Write Pulse Width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data Setup Time	t_{WSD}	3	—	—	ns	
Data Hold	t_{WHD}	3	—	—	ns	
Address Setup Time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address Hold Time	t_{WHA}	3	—	—	ns	
Chip Select Setup Time	t_{WSCS}	3	—	—	ns	
Chip Select Hold Time	t_{WHCS}	3	—	—	ns	
Write Disable Time	t_{WS}	—	—	15	ns	
Write Recovery Time	t_{WR}	—	—	18	ns	

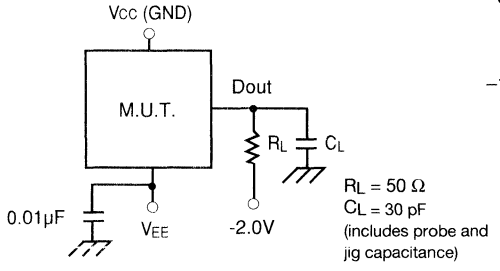
• Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	t_r	—	1.5	—	ns	
Output Fall Time	t_f	—	1.5	—	ns	

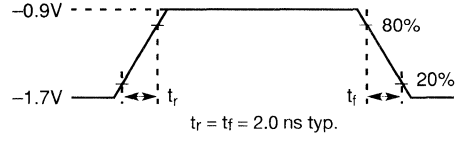
• Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{OUT}	—	5	—	pF	

■ AC TEST CONDITION

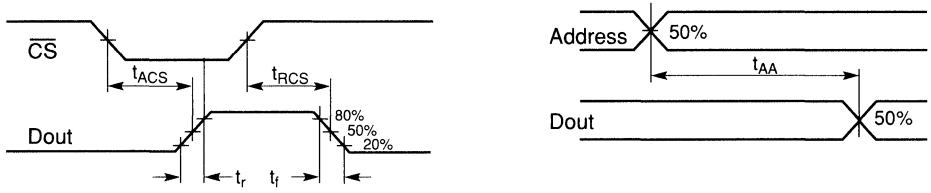


■ INPUT PULSE

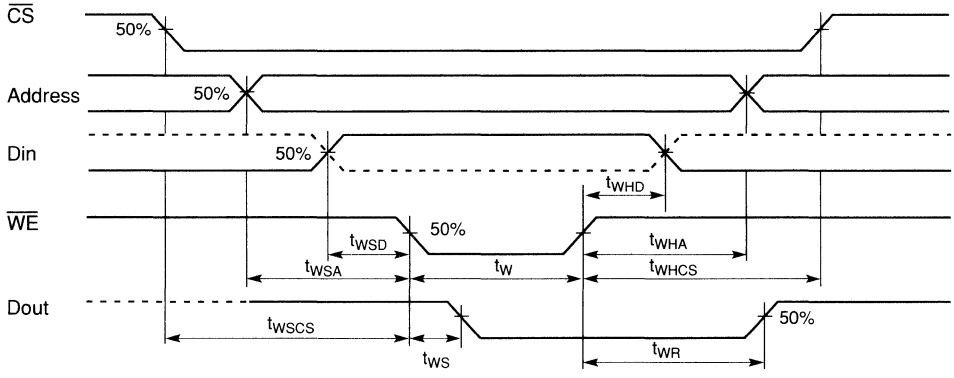


■ TIMING WAVEFORM

- **Read**



- **Write**



HM101494 Series

16384-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

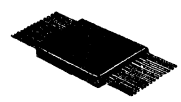
The HM101494 is ECL 100K compatible, 16384-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

■ FEATURES

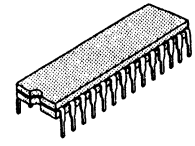
- 16384 × 4 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time .....10/12ns (max.)
- Write Pulse Width .....6/8ns (min.)
- Low Power Dissipation .....750mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101494-10 HM101494-12	10ns 12ns	400 mil 28 pin Cerdip (DG-28N)
HM101494F-10 HM101494F-12	10ns 12ns	28 pin Ceramic Flat (FG-28D)

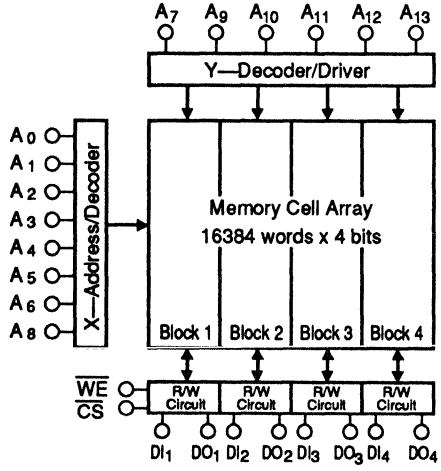


(FG-28D)

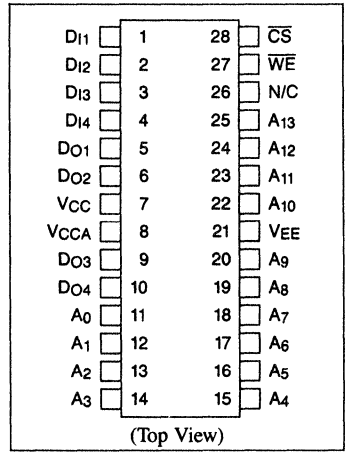


(DG-28N)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$(1)	Θ55 to +125	°C

NOTES: 1. Under bias.
2. Ceramic flat ... T_C, Cerdip ... T_a.

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = -5.2V, R_L = 50Ω to -2.0V(2), T_a = 0 to +85°C, air flow exceeding 2m/sec.(2), T_C = 0 to +85°C)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ180	—	—	mA

• **AC Characteristics** (V_{EE} = -5.2V ± 5%(2), T_a = 0 to +85°C, air flow exceeding 2m/sec.(2), T_C = 0 to +85°C)

1. Read Mode

Item	Symbol	Test Condition	HM101494-10			HM101494-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM101494-10			HM101494-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

5

3. Rise/Fall Time

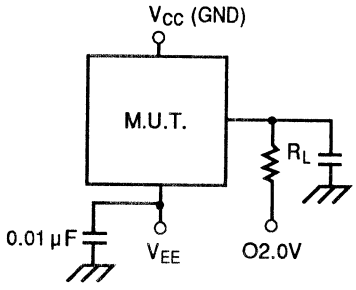
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

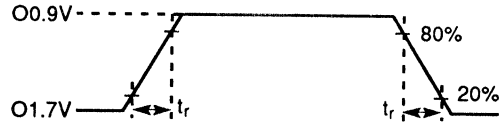
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	$\overline{WE}$, $\overline{CS}$, D_{I1}, D_{I2}	—	5	—	pF
		Others	—	3	—	pF
Output Capacitance	C_{out}		—	3	—	pF

■ TEST CIRCUIT AND WAVEFORMS

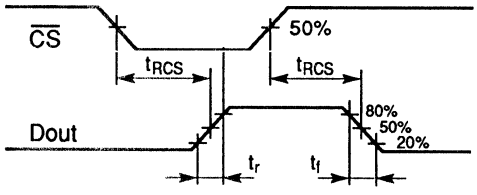
1. Loading Condition

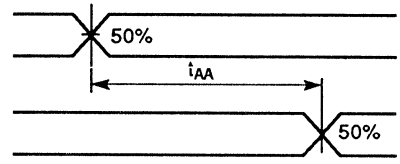


2. Input Pulse

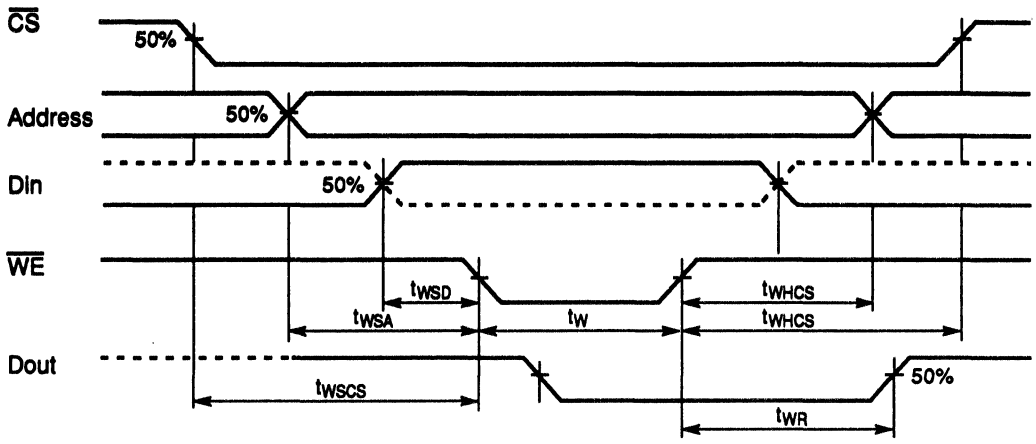


3. Read Mode





4. Write Mode



5

HM101490 Series

65536-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM101490 is ECL 100K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

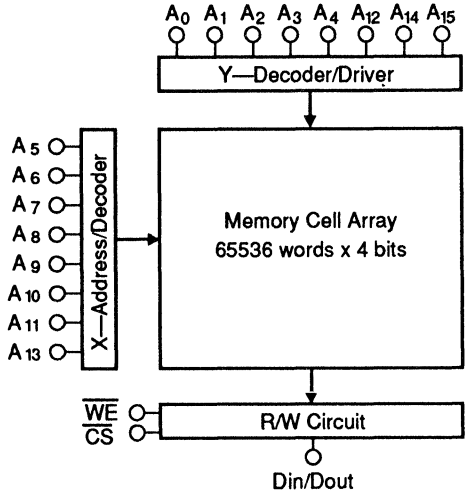
■ FEATURES

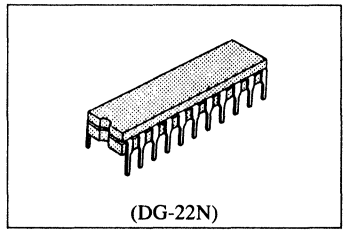
- 65536 × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time .....10/12ns (max.)
- Write Pulse Width .....6/8ns (min.)
- Low Power Dissipation .....570mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101490-10	10ns	300 mil 22 pin Cerdip (DG-22N)
HM101490-12	12ns	

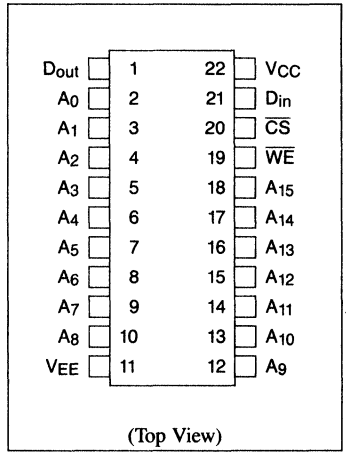
■ BLOCK DIAGRAM





(DG-22N)

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to Θ3.0	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(under\ bias)}$	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ140	—	—	mA

• **AC Characteristics** (V_{EE} = -5.2V ± 5%, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM101490-10			HM101490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM101490-10			HM101490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

5

3. Rise/Fall Time

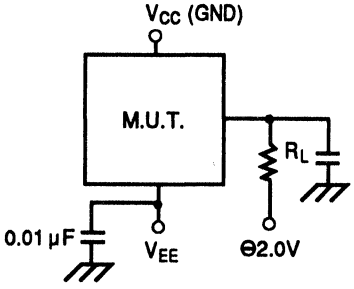
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

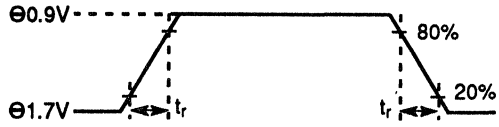
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

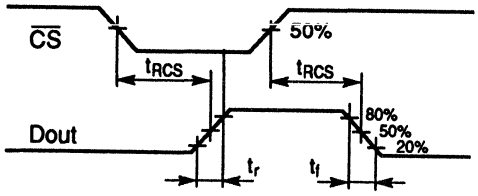
1. Loading Condition

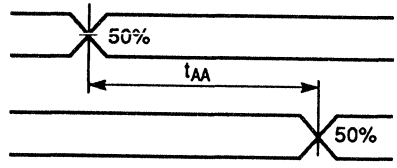


2. Input Pulse

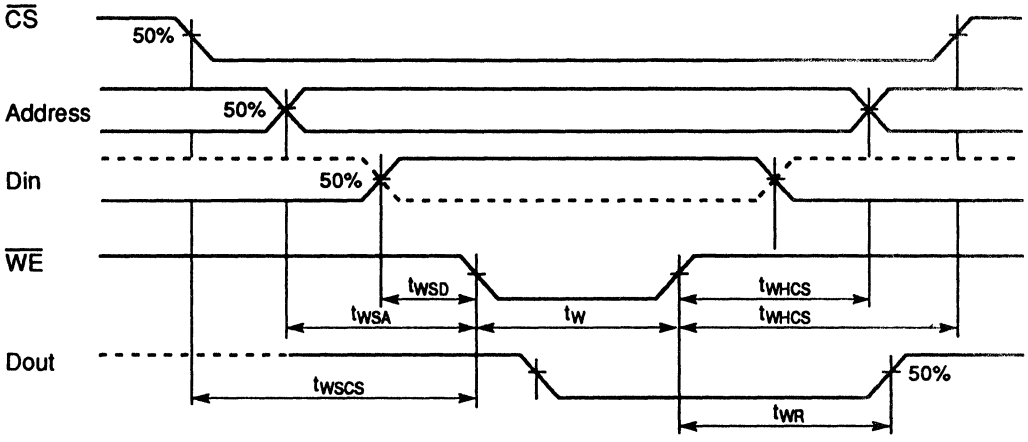


3. Read Mode





4. Write Mode

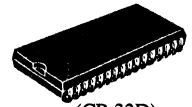

CS
Address
Din
WE
Dout
50%
50%
50%
50%
tWSD
tWSA
tW
tWHCS
tWHCS
tWSCS
tWR

HM101504 Series — Preliminary

65,536-Words x 4-Bit Random Access Memory

■ DESCRIPTION

The Hitachi HM101504 is ECL 100k compatible, 65,536 words by 4 bits read/write random access memory developed for high speed systems such as cache and control/buffer storage.



(CP-32D)

■ FEATURES

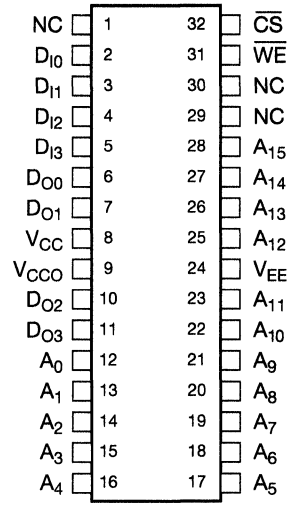
- 65,536-words x 4 bit organization
- Fully compatible with 100k ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 10/12 ns (max.)
- Write pulse width: 7/9 ns (min.)
- Low power dissipation: 500 mW (typ.)
- Output obtainable by wired-OR (open emitter)

■ ORDERING INFORMATION

Type No.	Cycle Time	Package
HM101504F-10 HM101504F-12	10 ns 12 ns	400 mil 32 pin Plastic SOJ (CP-32D)

■ PIN ARRANGEMENT

HM101504 Series

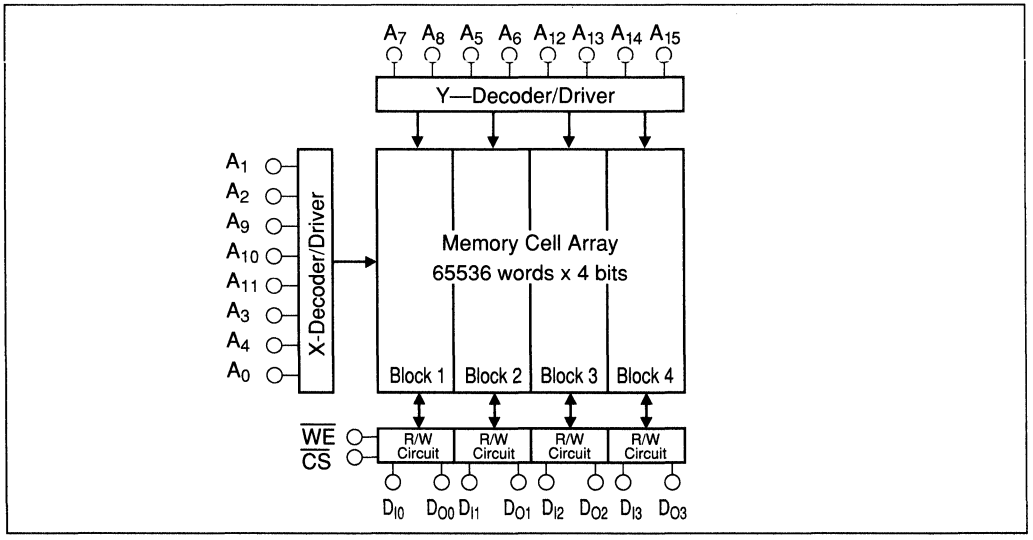


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{15}	Address Input
D_{I0}–D_{I3}	Data Input
D_{O0}–D_{O3}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input		D_{in}	Output	Mode
$\overline{CS}$	$\overline{WE}$			
H	X[1]	X[1]	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X[1]	D_{out}[2]	Read

Notes: 1. Irrelevant
2. Read Out Noninvert

■ ABSOLUTE MAXIMUM RATING (T_j = 125°C max)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	–30	mA
Power Dissipation	P_T	1.2	W
Operating Temperature	T_{opr}[2]	0 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature	T_{stg} (bias)[1, 2]	–10 to +85	°C

Note: 1. Under bias (V_{EE} = –6.0V min.)
2. Case temperature

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = –5.2V, R_L = 50Ω to –2.0V, T_C = 0 to +85°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	V_{in} = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	V_{in} = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	–1810	—	–1475	mV	
Input Current	I_{IH}	—	—	220	µA	V_{in} = V_{IHA}
	I_{IL}	0.5	—	170	µA	V_{in} = V_{ILB} ($\overline{CS}$)
		–50	—	—	µA	V_{in} = V_{ILB} (Others)
Supply Current	I_{EE}	–180	—	—	mA	All Inputs and Outputs Open

■ AC CHARACTERISTICS (V_{EE} = –5.2V ± 5%, T_C = 0 to +85°C)

• Read Mode

Item	Symbol	HM101504-10			HM101504-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	tACS	—	—	6	—	—	7	ns	
Chip Select Recovery Time	tRCS	—	—	6	—	—	7	ns	
Address Access Time	tAA	—	—	10	—	—	12	ns	

5

• **Write Mode**

Item	Symbol	HM101504-10			HM101504-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	tW	7	—	—	9	—	—	ns	tWSA = tWSA min
Data Setup Time	tWSD	1	—	—	1	—	—	ns	
Data Hold Time	tWHD	1	—	—	1	—	—	ns	
Address Setup Time	tWSA	1	—	—	1	—	—	ns	tW = tW min
Address Hold Time	tWHA	2	—	—	2	—	—	ns	
Chip Select Setup Time	tWSCS	1	—	—	1	—	—	ns	
Chip Select Hold Time	tWHCS	1	—	—	1	—	—	ns	
Write Disable Time	tWS	—	—	6	—	—	6	ns	
Write Recovery Time	tWR	—	—	12	—	—	14	ns	

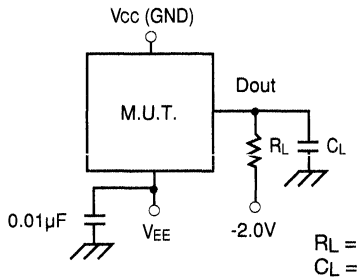
• **Rise/Fall Time**

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

• **Capacitance**

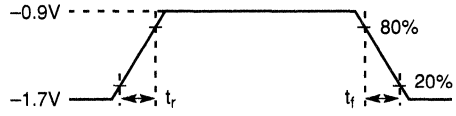
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{OUT}	—	5	—	pF	

■ AC TEST CONDITION



R_L = 50 W
C_L = 30 pF
(includes probe and jig capacitance)

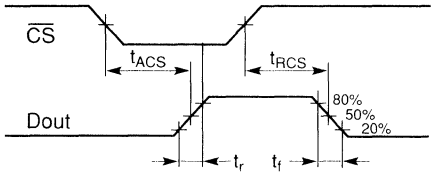
■ INPUT PULSE

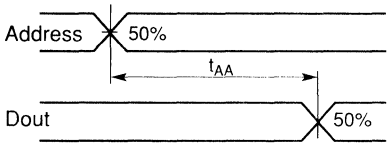


$t_r = t_f$ = 2.0 ns typ.

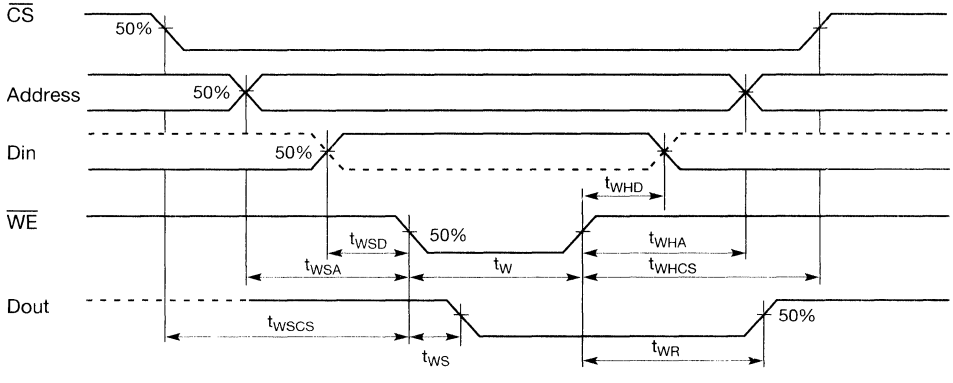
■ TIMING WAVEFORM

- **Read**





- **Write**



HM101500 Series

Preliminary

262144-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

HM101500F-15 is ECL 100K compatible, 262144-words by 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

■ FEATURES

- 262,144-Words × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time. . . . . .15ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ TRUTH TABLE

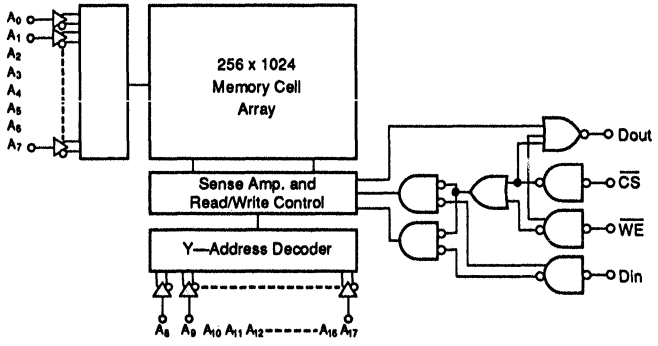
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

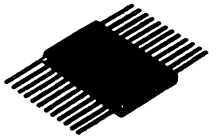
NOTES: X = Irrelevant;
* = Read out noninvert

■ ORDERING INFORMATION

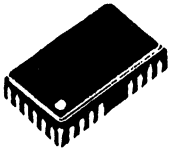
Type No.	Access Time	Package
HM101500F-15	15 ns	24 pin Ceramic Flat
HM101500CG-15	15 ns	28 pin Ceramic LCC

■ BLOCK DIAGRAM



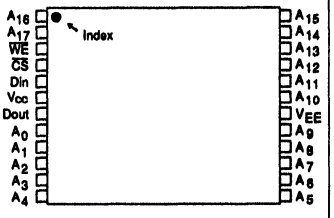


(FG-24A)

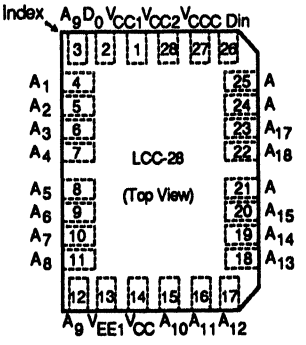


(CG-28B)

■ PIN ARRANGEMENT



(Top View)



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$*	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_C = 0 to +85°C)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ200	—	—	mA

• AC Characteristics (V_{EE} = -5.2V ± 5%, T_C = 0 to +85°C)

1. Read Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Chip Select Access Time	t_{ACS}		—	—	15	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	15	ns

2. Write Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	10	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		3	—	—	ns
Address Setup Time	t_{WSA}	t_W = 10ns	2	—	—	ns
Address Hold Time	t_{WHA}		3	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		3	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	18	

5

3. Rise/Fall Time

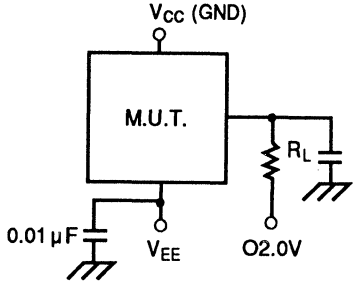
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

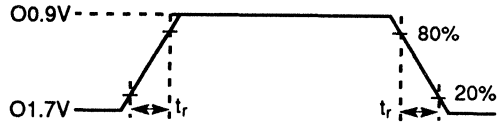
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

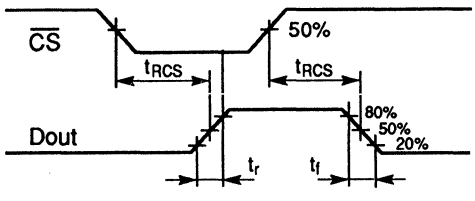
1. Loading Condition

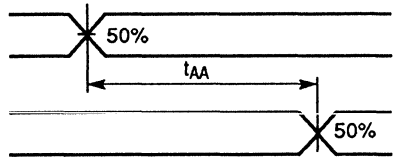


2. Input Pulse

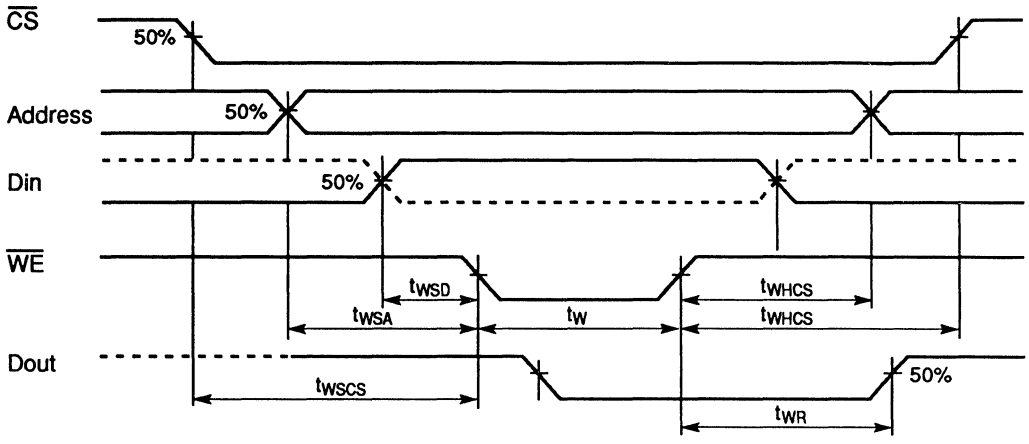


3. Read Mode





4. Write Mode



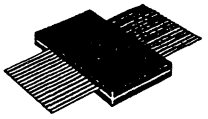
5

HM101514 Series — Preliminary

262,144-words x 4-Bit Random Access Memory

■ DESCRIPTION

The Hitachi HM101514 is ECL 100k compatible, 262,144 words by 4 bits read/write random access memory developed for high speed systems.



(FG-32D)

■ FEATURES

- 262,144-words x 4 bit organization
- Fully compatible with 100k ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 15 ns (max.)
- Write pulse width: 9 ns (min.)
- Low power dissipation: 800 mW (typ.)
- Output obtainable by wired-OR (open emitter)

■ ORDERING INFORMATION

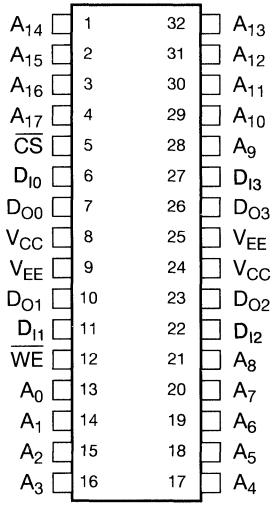
Type No.	Cycle Time	Package
HM101514F-15	15 ns	32 pin Ceramic Flat (30 mil Lead Pitch) (FG-32D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{17}	Address Input
D_{I0}–D_{I3}	Data Input
D_{O0}–D_{O3}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

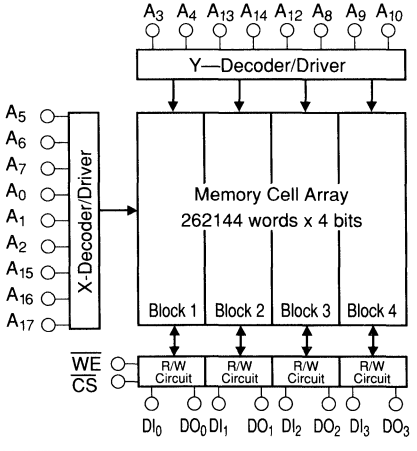
■ PIN ARRANGEMENT

HM101514 Series



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input		Din	Output	Mode
$\overline{CS}$	$\overline{WE}$			
H	X[1]	X[1]	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X[1]	Dout[2]	Read

Notes: 1. Irrelevant
2. Read Out Noninvert

■ ABSOLUTE MAXIMUM RATING (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (bias)[1]	−55 to +125	°C

Note: 1. Under bias (V_{EE} = −6.0V min.)

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, T_C = 0 to +85°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	V_{in} = V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	V_{in} = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	−1810	—	−1475	mV	
Input Current	I_{IH}	—	—	220	µA	V_{in} = V_{IHA}
	I_{IL}	0.5	—	170	µA	V_{in} = V_{ILB} ($\overline{CS}$)
		−50	—	—	µA	V_{in} = V_{ILB} (Others)
Supply Current	I_{EE}	−200	—	—	mA	All Outputs Open

■ AC CHARACTERISTICS (V_{EE} = −5.2V ± 5%, T_C = 0 to +85°C)

• Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	10	ns	
Chip Select Recovery Time	t_{RCS}	—	—	10	ns	
Address Access Time	t_{AA}	—	—	15	ns	

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• Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Write Pulse Width	t_W	9	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	3	—	—	ns	
Data Hold	t_{WHD}	3	—	—	ns	
Address Setup Time	t_{WSA}	3	—	—	ns	t_W = t_W min
Address Hold Time	t_{WHA}	3	—	—	ns	
Chip Select Setup Time	t_{WSCS}	3	—	—	ns	
Chip Select Hold Time	t_{WHCS}	3	—	—	ns	
Write Disable Time	t_{WS}	—	—	15	ns	
Write Recovery Time	t_{WR}	—	—	18	ns	

• Rise/Fall Time

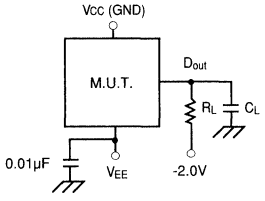
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	t_r	—	1.5	—	ns	
Output Fall Time	t_f	—	1.5	—	ns	

• Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{OUT}	—	5	—	pF	

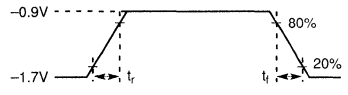
■ AC TEST CONDITION

Test Circuit



R_L = 50Ω
C_L = 30pF
(Includes probe and jig capacitance

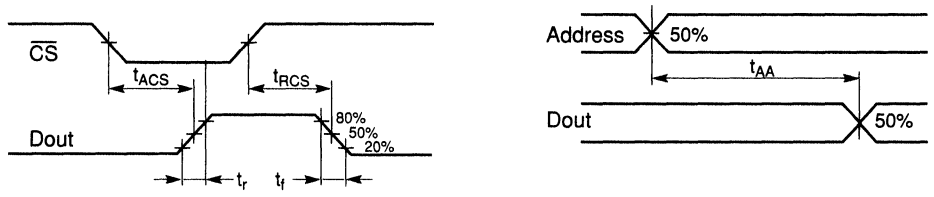
■ INPUT PULSE



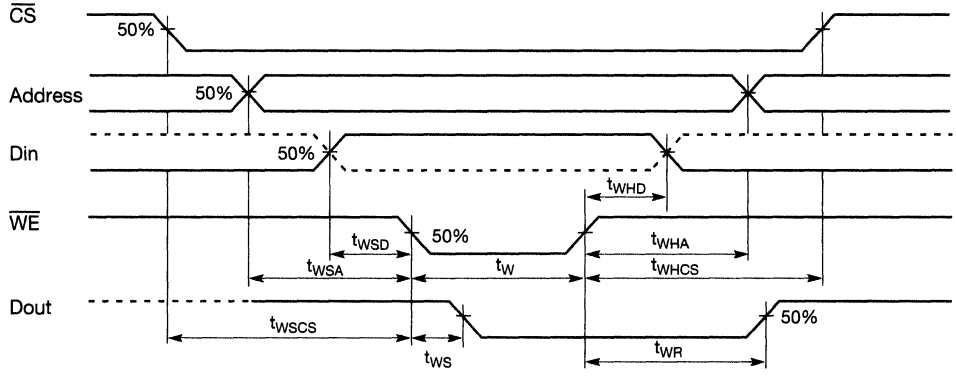
$t_r = t_f$ = 2.0ns typ

■ TIMING WAVEFORM

- **Read**



- **Write**



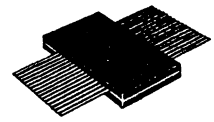
5

HM101510 Series — Preliminary

1,048,576-words x 1-Bit Random Access Memory

■ DESCRIPTION

The Hitachi HM101510 is ECL 100k compatible, 1,048,576 words by 1 bit read/write random access memory developed for high speed systems.



(FG-28DB)

■ FEATURES

- 1,048,576-words x 1 bit organization
- Fully compatible with 100k ECL level
- 0.8 μm Hi-BiCMOS process
- Address access time: 15 ns (max.)
- Write pulse width: 9 ns (min.)
- Low power dissipation: 700 mW (typ.)
- Output obtainable by wired-OR (open emitter)

■ ORDERING INFORMATION

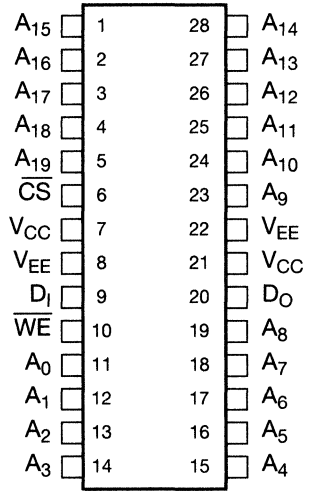
Type No.	Access Time	Package
HM101510F-15	15 ns	32 pin Ceramic Flat (30 mil Lead Pitch) (FG-28DB)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{19}	Address Input
D_I	Data Input
D_O	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

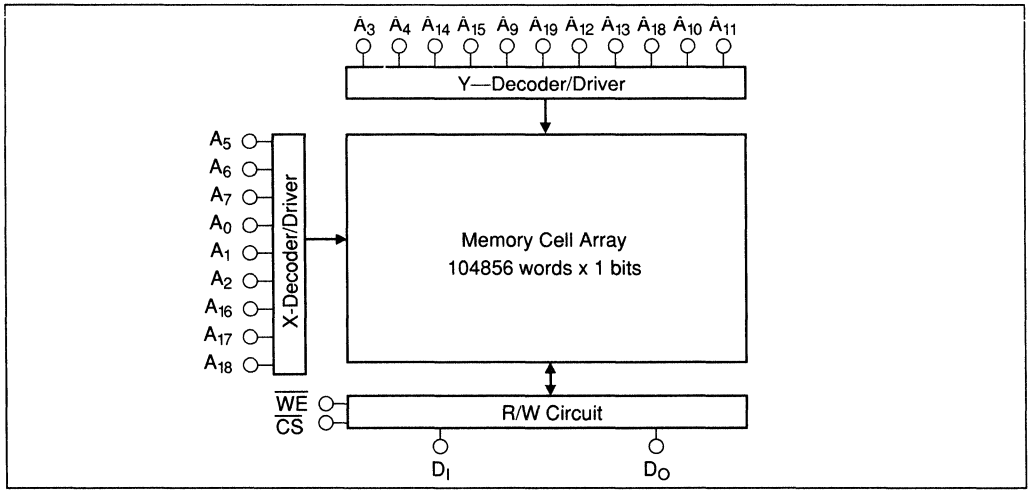
■ PIN ARRANGEMENT

HM101510 Series



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X[1]	X[1]	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X[1]	D_{out}[2]	Read

Notes: 1. Irrelevant
2. Read Out Noninvert

■ ABSOLUTE MAXIMUM RATING (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	–30	mA
Storage Temperature	T_{stg}	–65 to +150	°C
Storage Temperature	T_{stg} (bias)[1]	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0V min.)

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = –5.2V, R_L = 50Ω to –2.0V, T_C = 0 to +85°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	V_{in} = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	V_{in} = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage High/Low for All Inputs
	V_{IL}	–1810	—	–1475	mV	
Input Current	I_{IH}	—	—	220	µA	V_{in} = V_{IHA}
	I_{IL}	0.5	—	170	µA	V_{in} = V_{ILB} ($\overline{CS}$)
		–50	—	—	µA	V_{in} = V_{ILB} (Others)
Supply Current	I_{EE}	–180	—	—	mA	All Outputs Open

■ AC CHARACTERISTICS (V_{EE} = –5.2V ± 5%, T_c = 0 to +85°C)

• Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	10	ns	
Chip Select Recovery Time	t_{RCS}	—	—	10	ns	
Address Access Time	t_{AA}	—	—	15	ns	

5

• Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Write Pulse Width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data Setup Time	t_{WSD}	3	—	—	ns	
Data Hold	t_{WHD}	3	—	—	ns	
Address Setup Time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address Hold Time	t_{WHA}	3	—	—	ns	
Chip Select Setup Time	t_{WSCS}	3	—	—	ns	
Chip Select Hold Time	t_{WHCS}	3	—	—	ns	
Write Disable Time	t_{WS}	—	—	15	ns	
Write Recovery Time	t_{WR}	—	—	18	ns	

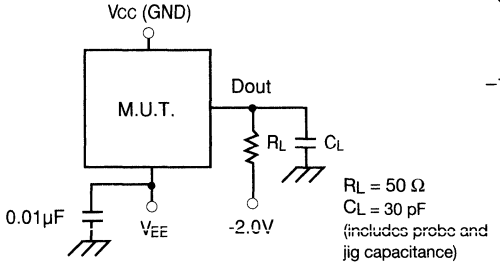
• Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	t_r	—	1.5	—	ns	
Output Fall Time	t_f	—	1.5	—	ns	

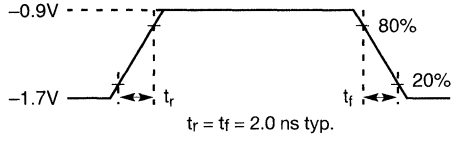
• Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{OUT}	—	5	—	pF	

■ AC TEST CONDITION

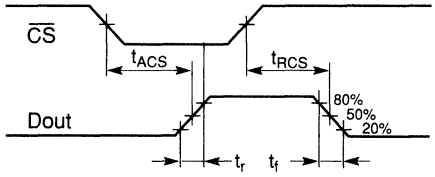


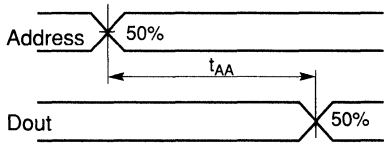
■ INPUT PULSE



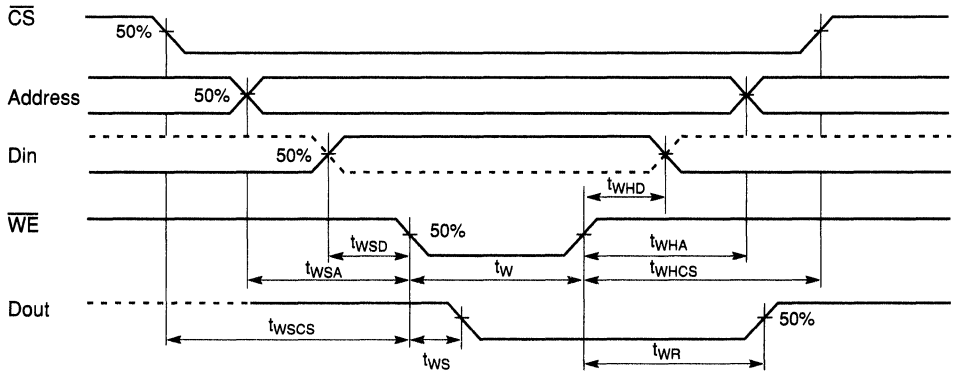
■ TIMING WAVEFORM

- **Read**





- **Write**



5

Section 6
FIFO Memory

HITACHI®

6

HM63921 Series

2K × 9-Bit CMOS Parallel In-Out FIFO Memory

■ DESCRIPTION

The HM63921 is a First-In, First-Out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and half-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

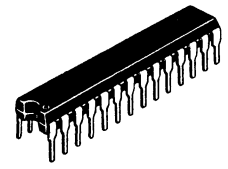
Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 30/35/45ns. Organization of HM63921 provides a 9-bit data bus. the ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3micron technology. The device is available in DIP.

■ FEATURES

- First-In, First-Out Dual Port Memory
- 2k × 9 Organization
- Low-Power CMOS 1.3micron Technology
- Asynchronous and Simultaneous Read and Write
- Fully Expandable in Depth and/or Width
- Single 5V (±10%) Power Supply
- Empty and Full Warning Flags
- Half-Full Flag
- Access Time 20/25/35ns
- Package . . . . . .300-mil 28-pin Plastic DIP Package

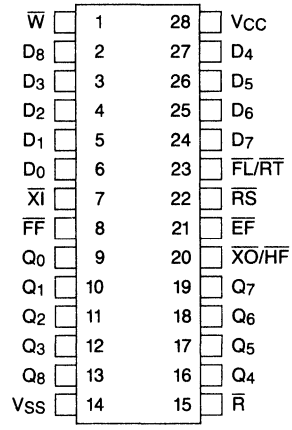
■ ORDERING INFORMATION

Type Name	Access Time	Package
HM63921P-20	20ns	300-mil 28-pin
HM63921P-25	25ns	Plastic DIP
HM63921P-35	35ns	(DP-28NA)



(DP-28NA)

■ PIN ARRANGEMENT

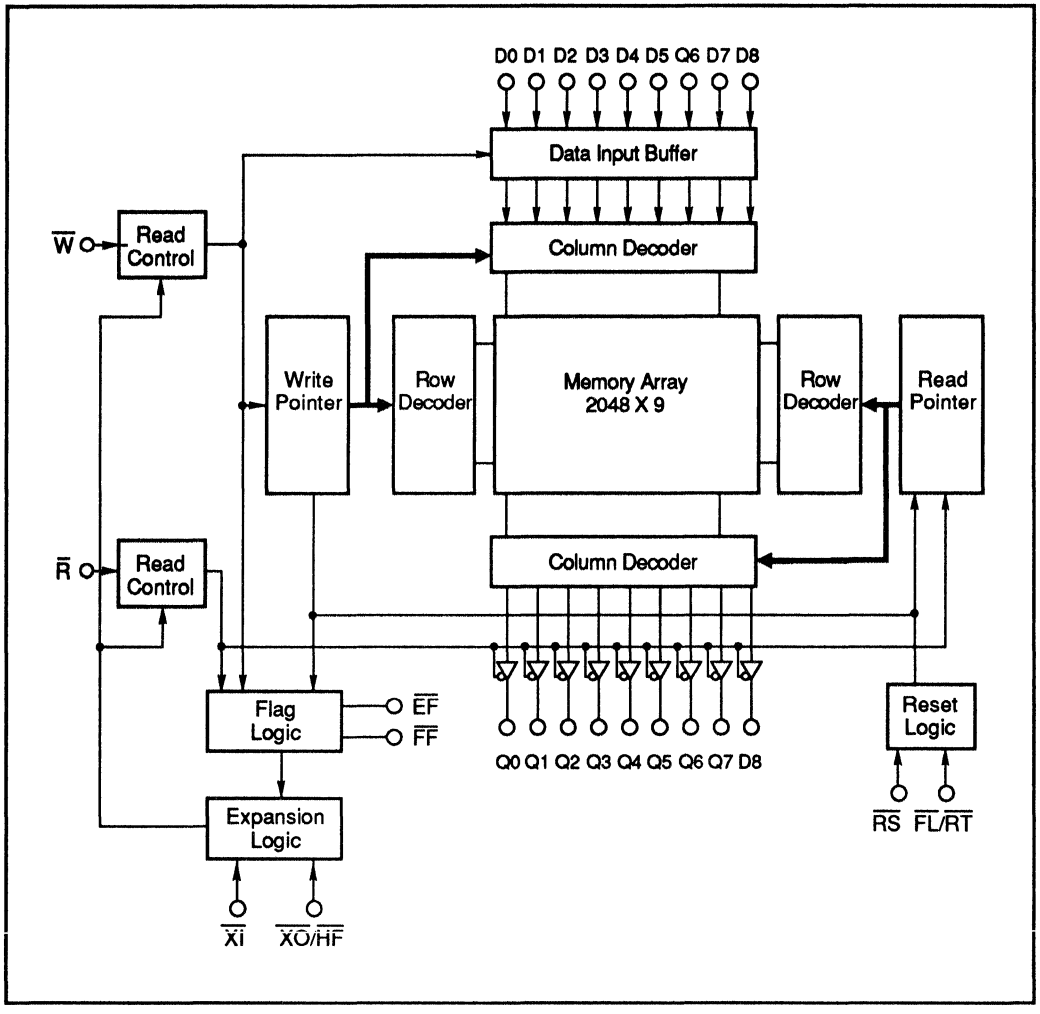


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_0-D_8	Data Inputs
$\overline{RS}$	Reset
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{FL}$	First Load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-In
$\overline{XO}$	Expansion-Out
$\overline{HF}$	Half-Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
Q_0-Q_8	Data Outputs

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	-0.5(2) to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTES: 1. Relative to V_{SS}.
2. -3.5V for pulse width ≤ 10ns.

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5(1)	—	0.8	V

NOTE: 1. -3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = 0V - V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{R}$ = V_{IH}, V_{out} = 0V - V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC1}	Average Operating Current	-20	—	120	mA
			-25	—	110	mA
			-35	—	100	mA
Standby Power Supply Current	I_{SB1}	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	—	—	10	mA
	I_{SB2}	All inputs ≥ V_{CC} - 0.2V or ≤ V_{CC}	—	—	1	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

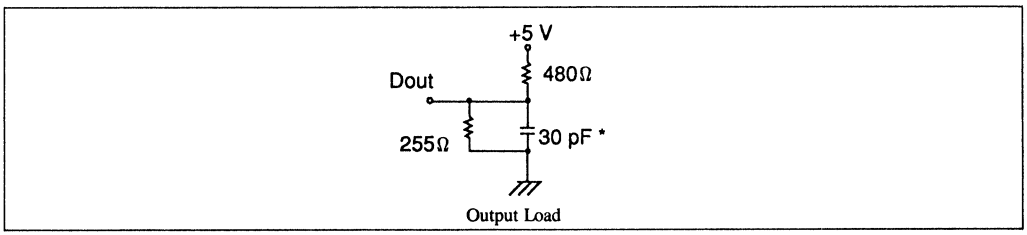
Parameter	Symbol	Test Conditions	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	10	pF

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5 ± 10%)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figure



*Including scope and jig.

• Read Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	30	—	35	—	45	—	ns
Access Time	t_A	—	20	—	25	—	35	ns
Read Recovery Time	t_{RR}	10	—	10	—	10	—	ns
Read Pulse Width	t_{RPW}	20	—	25	—	35	—	ns
Read Low to DB Low Z	t_{RLZ}(1)	5	—	5	—	5	—	ns
Read High to DB High Z	t_{RHZ}(1)	—	15	—	15	—	20	ns
Data Valid from Read High	t_{OH}	3	—	3	—	3	—	ns
Read Pulse Width After Empty Flag High	t_{RPE}	20	—	25	—	35	—	ns
Write High to DB Low Z (Read Data Flow Through Mode)	t_{WLZ}(1)	3	—	3	—	3	—	ns

NOTE: 1. t_{RLZ}, t_{RHZ} and t_{WLZ} are sampled and not 100% tested.

• Write Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	30	—	35	—	45	—	ns
Write Recovery Time	t_{WR}	10	—	10	—	10	—	ns
Write Pulse Width	t_{WPW}	20	—	25	—	35	—	ns
Data Setup Time	t_{DS}	10	—	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	5	—	ns
Effective Write Pulse Width After Full Flag High	t_{WPF}	20	—	25	—	35	—	ns

• Reset Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle Time	t_{RSC}	30	—	35	—	45	—	ns
Reset Pulse Width	t_{RS}	25	—	25	—	35	—	ns
Reset Setup Time	t_{RSS}	0	—	0	—	0	—	ns
Reset Recovery Time	t_{RSR}	10	—	10	—	10	—	ns

• Retransmit Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Retransmit Cycle Time	t_{RTC}	30	—	35	—	45	—	ns
Retransmit Pulse Width	t_{RT}	20	—	20	—	35	—	ns
Retransmit Setup Time	t_{RTS}	0	—	0	—	0	—	ns
Retransmit Recovery Time	t_{RTR}	10	—	10	—	10	—	ns

• Flag Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset to Empty Flag Low	t_{EFL}	—	20	—	25	—	35	ns
Reset to Full Flag High	t_{FFH}	—	20	—	25	—	35	ns
Reset to Half-Full Flag High	t_{HFH}	—	30	—	35	—	45	ns
Read Low to Empty Flag Low	t_{REF}	—	20	—	25	—	35	ns
Read High to Full Flag High	t_{RFF}	—	20	—	25	—	35	ns
Write High to Empty Flag High	t_{WEF}	—	20	—	25	—	35	ns
Write Low to Full Flag Low	t_{WFF}	—	20	—	25	—	35	ns
Write Low to Half-Full Flag Low	t_{WHF}	—	30	—	35	—	45	ns
Read High to Half-Full Flag High	t_{RHF}	—	30	—	35	—	45	ns

• Expansion Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Expansion in Setup to Write or Read	t_{EFL}	—	15	—	20	—	30	ns
Expansion in Recovery Time	t_{RFF}	—	15	—	20	—	30	ns
Expansion in Pulse Width	t_{WHF}	10	—	10	—	10	—	ns
Expansion Out High Delay From Clock	t_{REF}	10	—	10	—	10	—	ns
Expansion Out Low Delay From Clock	t_{RFF}	10	—	10	—	15	—	ns

SIGNAL DESCRIPTIONS

Inputs

- Reset ($\overline{RS}$)
  The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and half-full ($\overline{HF}$) will go high during reset cycle.
- Write enable ($\overline{W}$)
  Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of ($\overline{W}$) are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.
- Read enable ($\overline{R}$)
  Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data has been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.
- First load/retransmit ($\overline{FL}/\overline{RT}$)
  For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.
- Expansion-in ($\overline{XI}$)
  For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.
- Data In (D_0 to D_8)
  Data inputs for 9-bit wide data.

Outputs

- Full Flag ($\overline{FF}$)
  The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.
- Empty flag ($\overline{EF}$)
  The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.
- Expansion-out ($\overline{XO}$)/Half-full flag ($\overline{HF}$)
  This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is almost full.
- Data outputs (Q_0 to Q_8)
  Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

VARIOUS OPERATIONS MODE

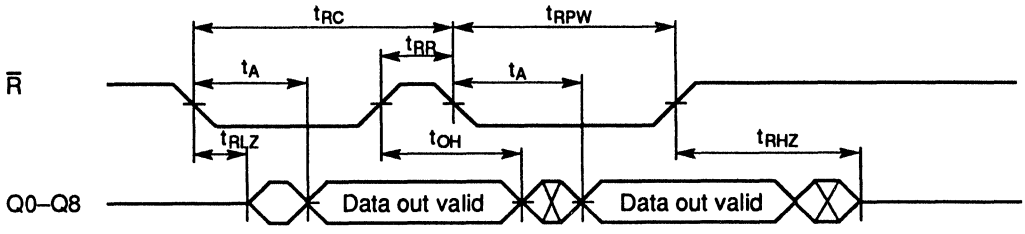
- Single device mode
  If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.
- Width expansion mode
  Width expansion by 9-bit increments may be achieved when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short periods of time, the flag outputs should not be wired together.
- Depth expansion mode
  Multiple of FIFOs could provide multiple of 2k × 9 as (N) × (2k) by 9-bits wide, where N is the number of FIFOs connected in depth expansion mode.

  The following arrangement must be provided.

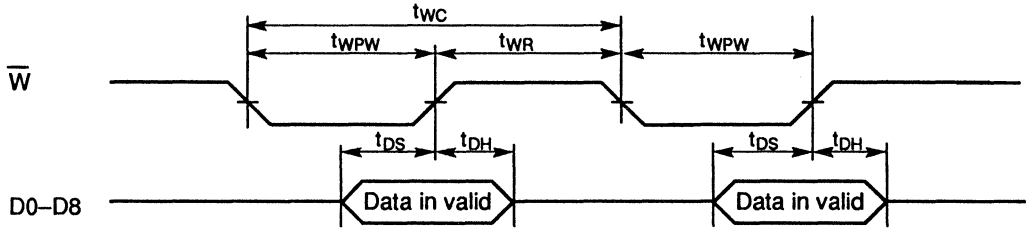
  1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
  2. All other ($\overline{FL}$) should be connected to V_{CC}.
  3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
  4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
  5. ($\overline{RT}$) and ($\overline{AF}$) will not be available in this mode.
- Compound expansion mode
  Combination of width and depth expansion modes will provide larger FIFO arrays.

■ TIMING WAVEFORM

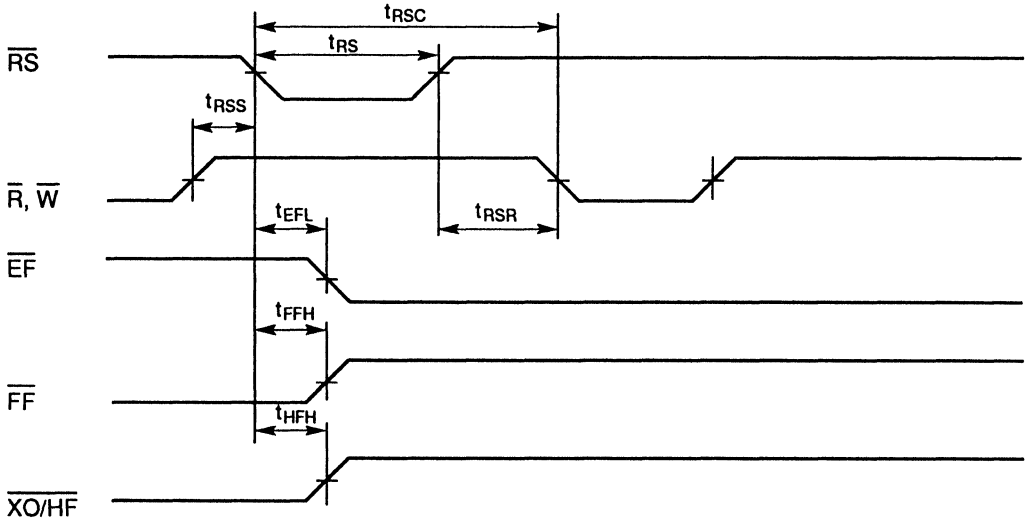
• Read Cycle



• Write Cycle



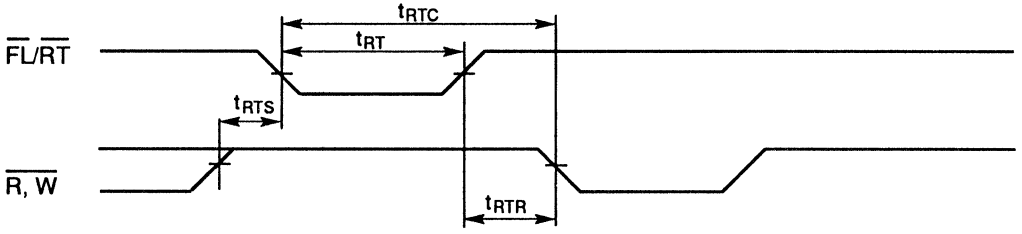
• Reset Cycle



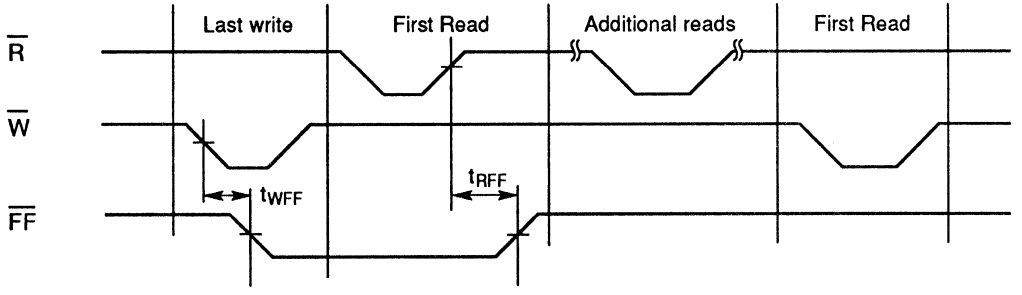
NOTES: 1. $\overline{W} = \overline{R} = V_{IH}$ during reset.

2. $t_{RSC} = t_{RST}, t_{RSR}$.

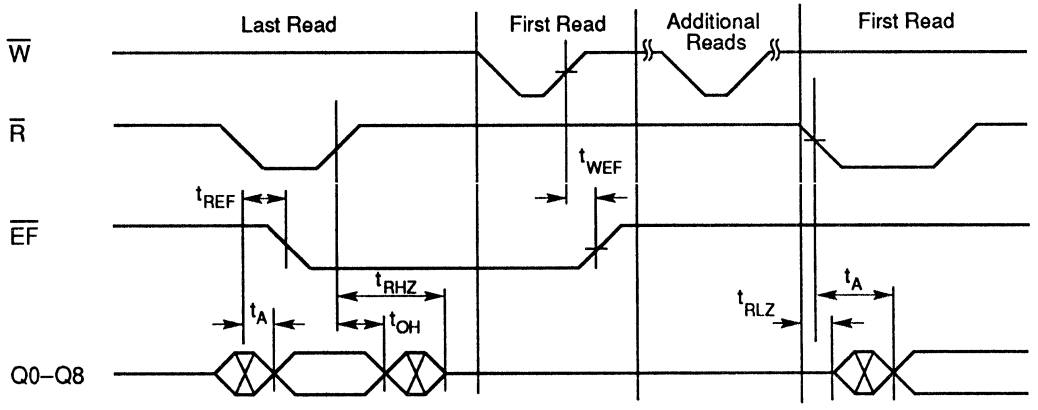
• **Retransmit Cycle**



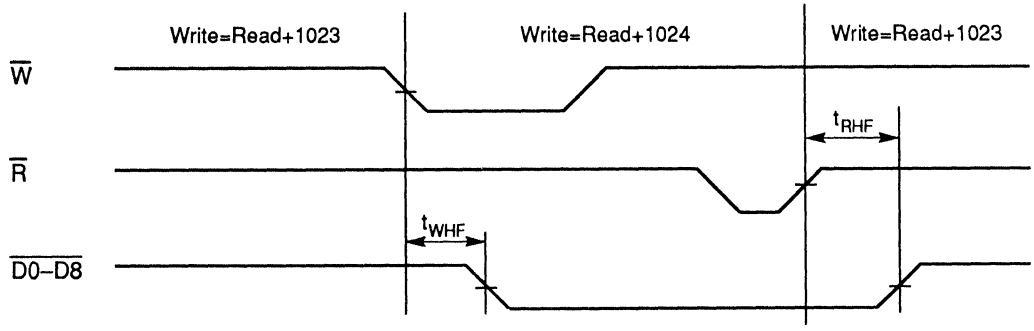
• **Full-Flag Cycle** (From Last Write to First Read)



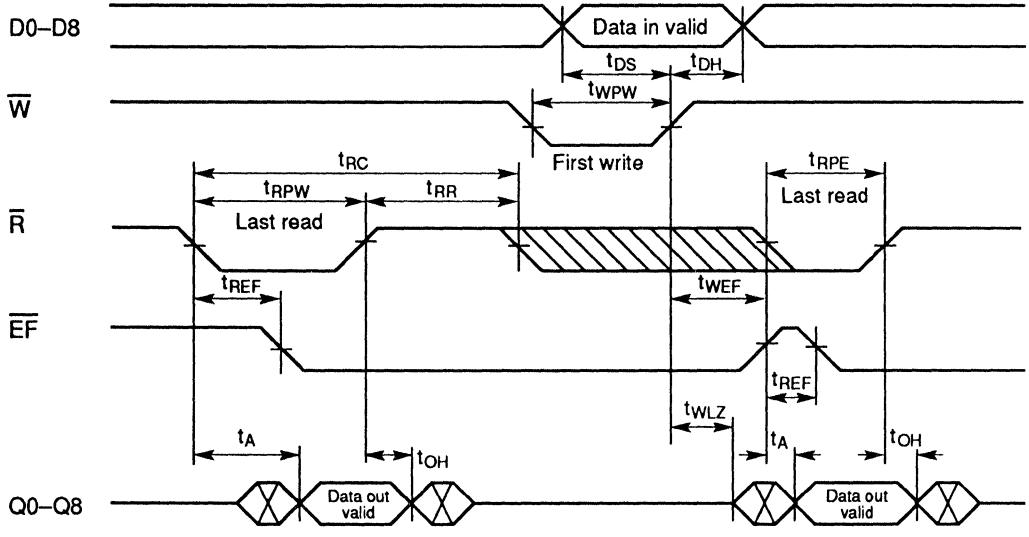
• **Empty-Flag Cycle** (From Last Read to First Write)



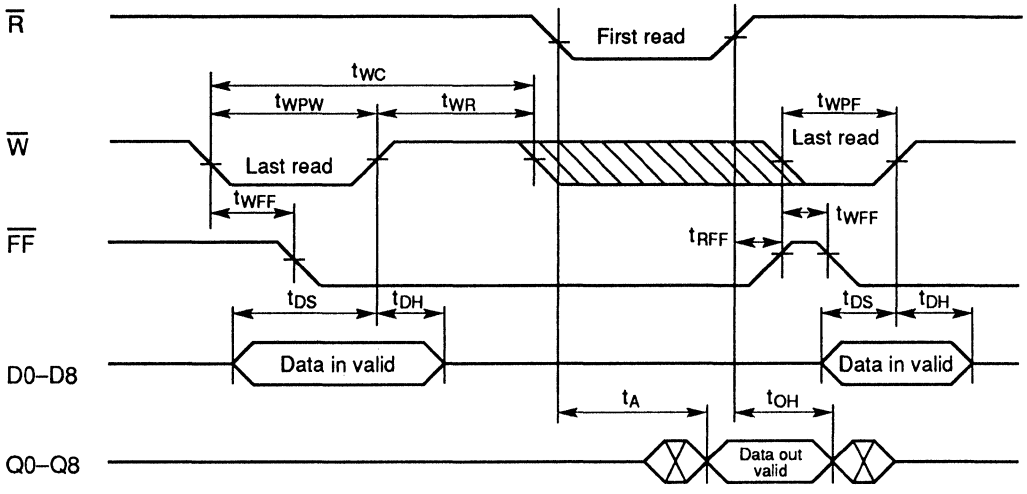
• **Half-Full Flag Cycle**



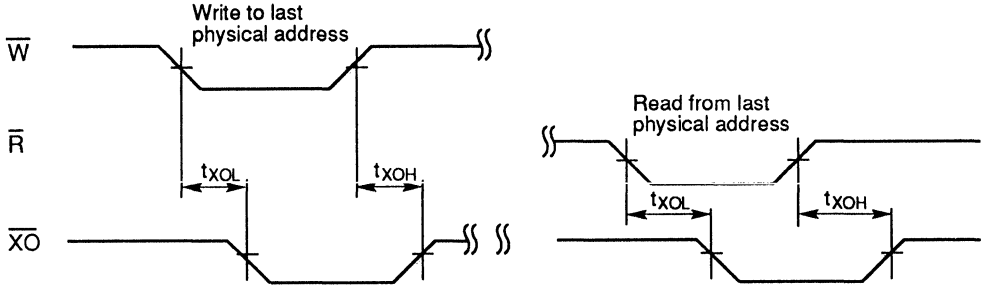
• **Read Data Flow Through Mode**



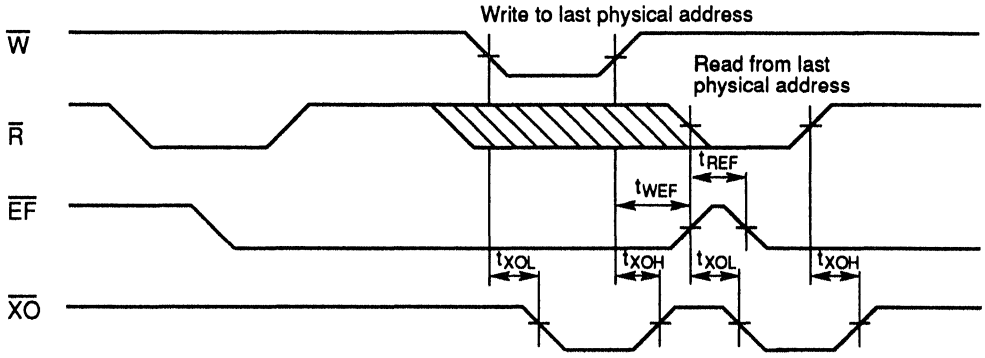
• **Write Data Flow Through Mode**



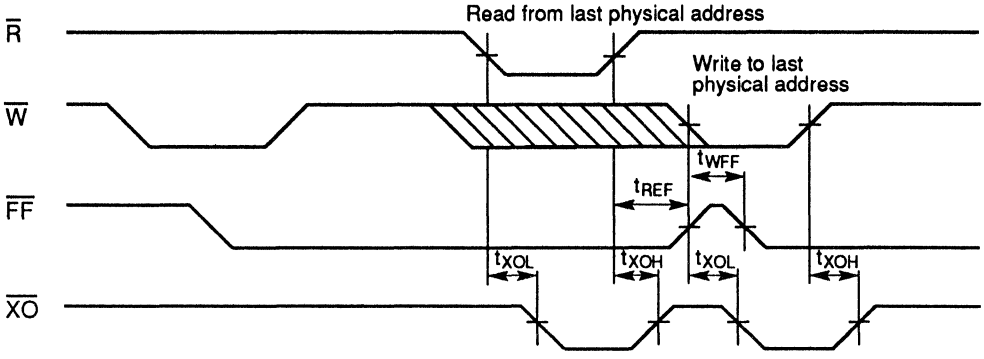
• **Expansion Out Cycle 1**



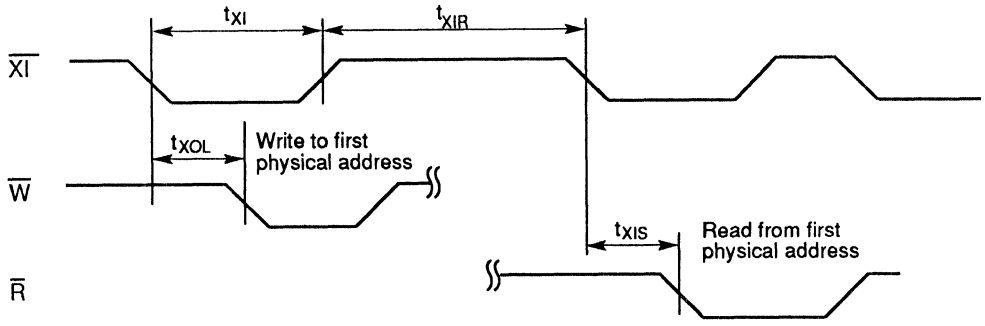
• **Expansion Out Cycle 2** (Read Data Flow Through Mode)



• **Expansion Out Cycle 3** (Write Data Flow Through Mode)



• **Expansion In Cycle**



HM63941 Series — Preliminary

4K × 9-Bit CMOS Parallel In-Out FIFO Memory

■ DESCRIPTION

The HM63941 is a First-In, First-Out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and almost-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

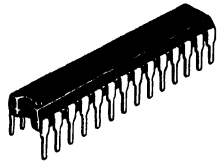
Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 35/45/60ns. Organization of HM63941 provides a 9-bit data bus. the ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3micron technology. The device is available in DIP.

■ FEATURES

- First-In, First-Out Dual Port Memory
- 4k × 9 Organization
- Low-Power CMOS 1.3micron Technology
- Asynchronous and Simultaneous Read and Write
- Fully Expandable in Depth and/or Width
- Single 5V (± 10%) Power Supply
- Empty and Full Warning Flags
- Almost-Full Flag
- Access Time 25/35/45ns
- Package. . . . . .28-pin DIP Package

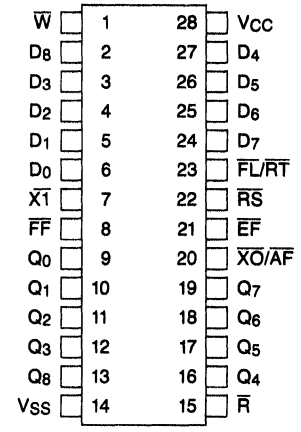
■ ORDERING INFORMATION

Type Name	Access Time	Package
HM63941P-25	25ns	28-pin Plastic DIP
HM63941P-35	35ns	
HM63941P-45	45ns	



(DP-28NA)

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_0–D_8	Data inputs
$\overline{RS}$	Reset
$\overline{W}$	Write enable
$\overline{R}$	Read enable
$\overline{FL}$	First load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-in
$\overline{XO}$	Expansion-out
$\overline{AF}$	Almost-full flag
$\overline{FF}$	Full flag
$\overline{EF}$	Empty flag
Q_0–Q_8	Data outputs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	-0.5(2) to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTES: 1. Relative to V_{SS}.
2. -3.5V for pulse width ≤ 10ns.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	—	6.0	V
	V_{IL}	-0.5(1)	—	0.8	V

NOTE: 1. -3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = 0V - V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{R}$ = V_{IH}, V_{out} = 0V - V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC1}	Average Operating Current	—	—	80	mA
	I_{CC2}	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	—	—	10	mA
Standby Power Supply Current	I_{SB}	All Inputs ≥ V_{CC} - 0.2V or ≤ V_{CC}	—	—	1	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

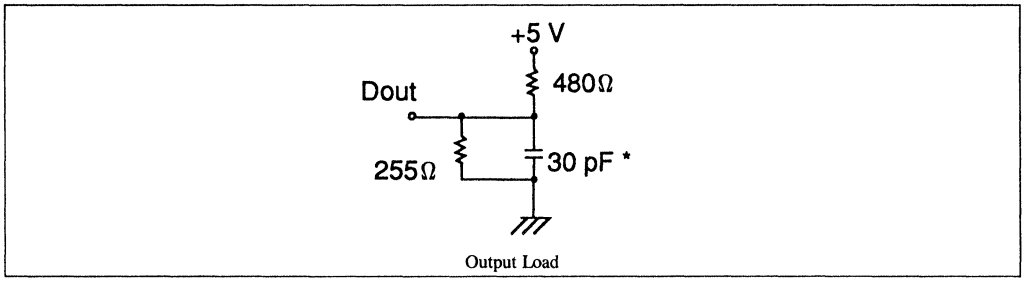
■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	TBD	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	TBD	pF

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5 ± 10%)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figure



Output Load

*Including scope and jig.

• Read Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	60	—	ns
Access Time	t_A	—	25	—	35	—	45	ns
Read Recovery Time	t_{RR}	10	—	10	—	15	—	ns
Read Pulse Width	t_{RPW}	25	—	35	—	45	—	ns
Read Low to DB Low Z	t_{RLZ}	5	—	5	—	10	—	ns
Read High to DB High Z	t_{RHZ}	—	15	—	20	—	25	ns
Data Valid from Read High	t_{OH}	5	—	5	—	5	—	ns

• Write Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	60	—	ns
Write Recovery Time	t_{WR}	10	—	10	—	15	—	ns
Write Pulse Width	t_{WPW}	20	—	35	—	45	—	ns
Data Setup Time	t_{DS}	15	—	20	—	25	—	ns
Data Hold Time	t_{DH}	0	—	0	—	5	—	ns

• Reset Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle Time	t_{RSC}	35	—	45	—	60	—	ns
Reset Pulse Width	t_{RS}	25	—	35	—	45	—	ns
Reset Recovery Time	t_{RSR}	10	—	10	—	15	—	ns

• Retransmit Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Retransmit Cycle Time	t_{RTC}	35	—	45	—	60	—	ns
Retransmit Pulse Width	t_{RT}	20	—	35	—	45	—	ns
Retransmit Recovery Time	t_{RTR}	10	—	10	—	15	—	ns

• Flag Timing

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset to Empty Flag Low	t_{EFL}	—	30	—	45	—	60	ns
Read Low to Empty Flag Low	t_{REF}	—	25	—	35	—	45	ns
Read High to Full Flag High	t_{RFF}	—	25	—	35	—	45	ns
Write High to Empty Flag High	t_{WEF}	—	25	—	35	—	45	ns
Write Low to Full Flag Low	t_{WFF}	—	25	—	35	—	45	ns
Write Low to Almost-Full Low	t_{WAF}	—	30	—	40	—	55	ns
Read High to Almost-Full High	t_{RAF}	—	30	—	40	—	55	ns

SIGNAL DESCRIPTIONS

Inputs

- Reset ($\overline{RS}$)
  The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and almost-full ($\overline{AF}$) will go high during reset cycle.
- Write enable ($\overline{W}$)
  Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of ($\overline{W}$) are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.
- Read enable ($\overline{R}$)
  Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data has been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.
- First load/retransmit ($\overline{FL}/\overline{RT}$)
  For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.
- Expansion-in ($\overline{XI}$)
  For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.
- Data In (D_0 to D_8)
  Data inputs for 9-bit wide data.

Outputs

- Full Flag ($\overline{FF}$)
  The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.
- Empty flag ($\overline{EF}$)
  The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.
- Expansion-out ($\overline{XO}$)/Almost-full flag ($\overline{AF}$)
  This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is almost full.
- Data outputs (Q_0 to Q_8)
  Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

VARIOUS OPERATIONS MODE

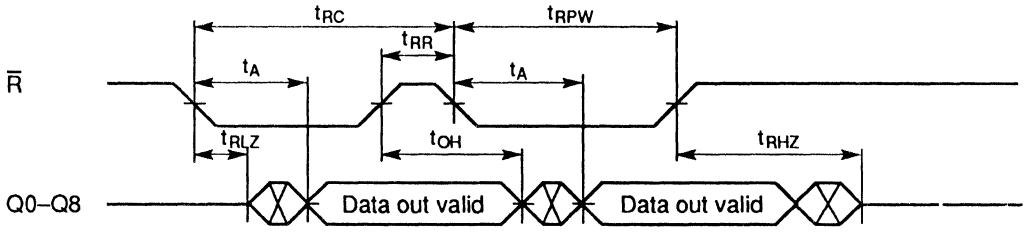
- Single device mode
  If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.
- Width expansion mode
  Width expansion by 9-bit increments may be achieved when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short periods of time, the flag outputs should not be wired together.
- Depth expansion mode
  Multiple of FIFOs could provide multiple of 4k × 9 as (N) × (4k) by 9-bits wide, where N is the number of FIFOs connected in depth expansion mode.

  The following arrangement must be provided.

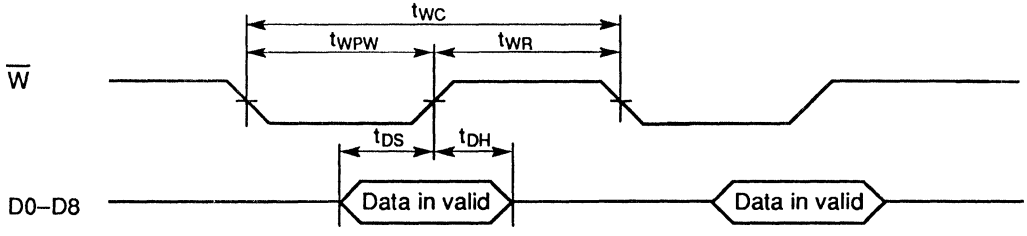
  1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
  2. All other ($\overline{FL}$) should be connected to V_{CC}.
  3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
  4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
  5. ($\overline{RT}$) and ($\overline{AF}$) will not be available in this mode.
- Compound expansion mode
  Combination of width and depth expansion modes will provide larger FIFO arrays.

■ TIMING WAVEFORM

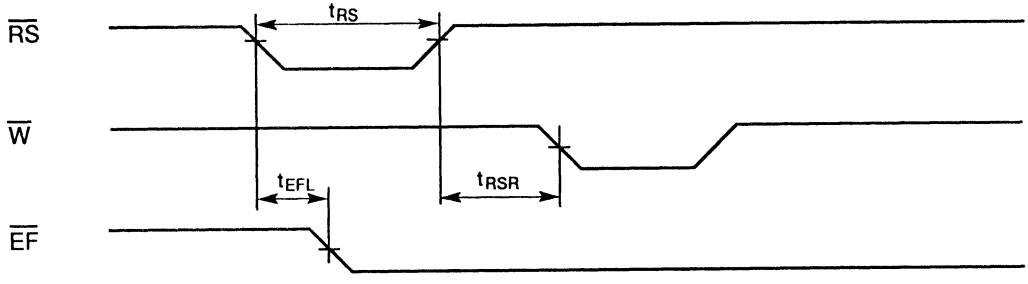
• Read Cycle



• Write Cycle

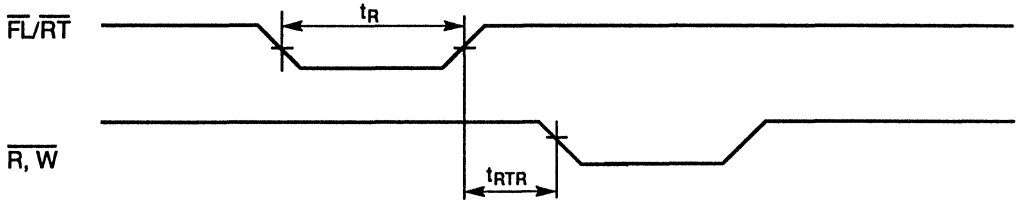


• Reset Cycle

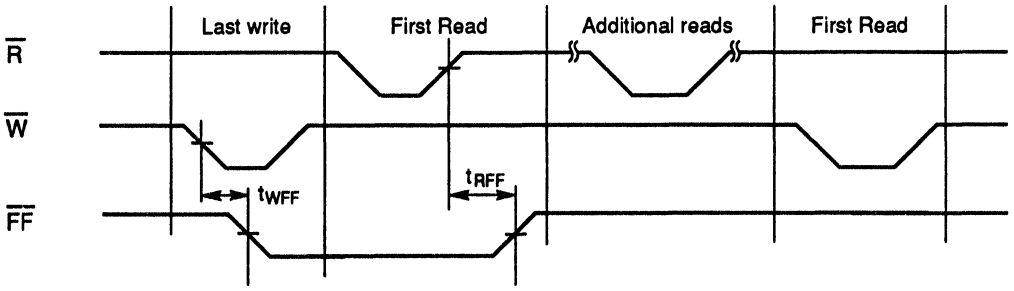


NOTES: 1. $\overline{W} = \overline{R} = V_{IH}$ during reset.
2. $t_{RSC} = t_{RST}, t_{RSR}$.

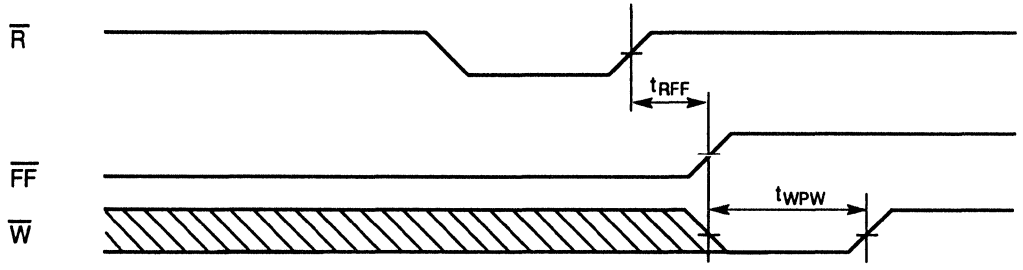
• **Retransmit Cycle**



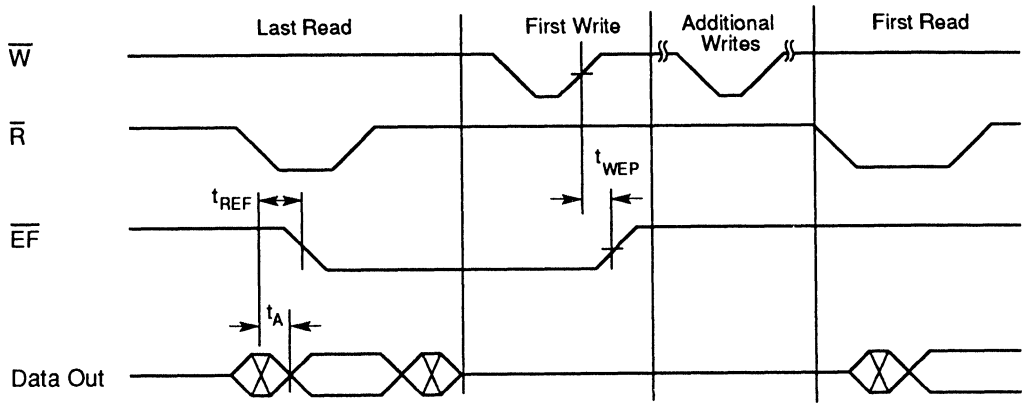
• **Full-Flag Cycle** (From Last Write to First Read)



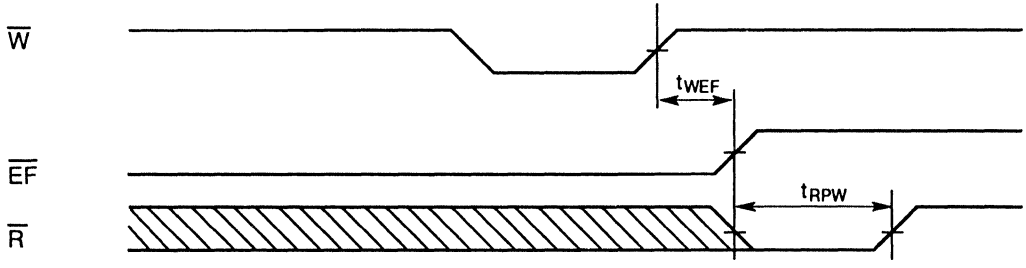
• **Full-Flag Cycle** (Effective Write Pulse Width After $\overline{FF}$ High)



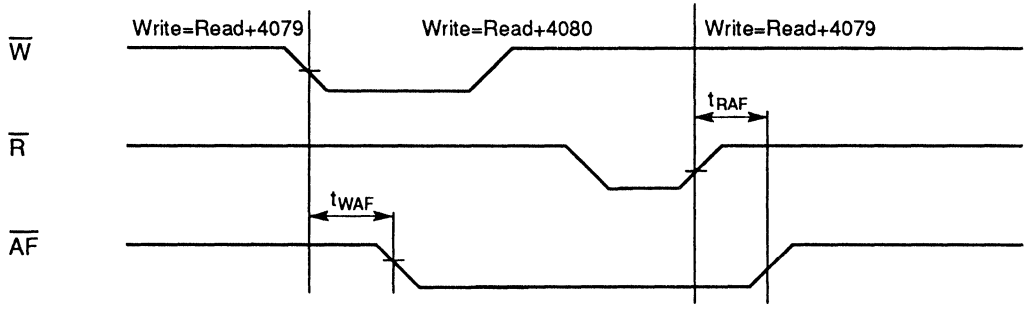
• **Empty-Flag Cycle** (From Last Write to First Read)



• **Empty-Flag Cycle** (Effective Read Pulse Width After $\overline{EF}$ High)



• **Almost-Full Flag Cycle**



NOTES

NOTES

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SRAM Data Book Errata

The following are corrections to the SRAM Data Book (Order Number M12T014). Note the changes and update accordingly.

■ HM658512 Series—Page 395

- 120 ns Access Time and 190 ns Cycle Time not available
- LL and D versions no longer available
- Ordering Information revised.

■ HM658512 Series—Page 399

- AC Characteristics Table—HM658512-12 Min.–Max. vertical column removed.

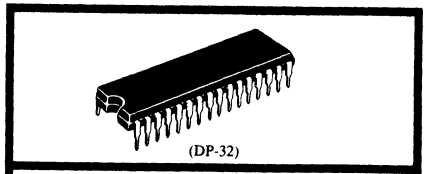
Note: The following two pages illustrate the technical data as it should appear.

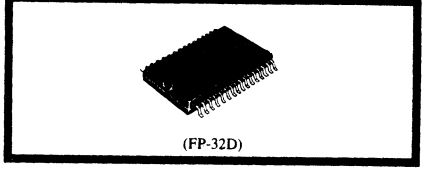
HM658512 Series

524,288-Word × 8-Bit High Speed Pseudo Static RAM

Features

- Single 5 V (± 10%)
- High speed
  - Access time
    - $\overline{CE}$ access time ..... 80/100 ns
  - Cycle time
    - Random read/write cycle time ..... 130/160 ns
- Low power
  - Active: 250 mW (typ.)
  - Standby: 200 μW (typ.)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - L/LV-version ..... Address refresh
    - Automatic refresh
    - Self refresh

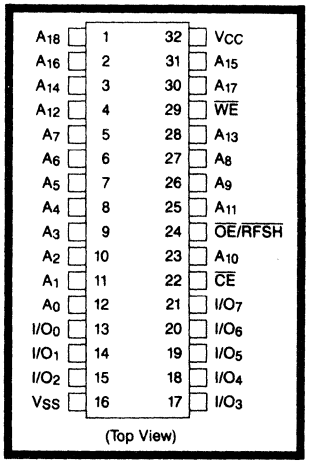

(DP-32)


(FP-32D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6585121.P 8 HM6585121.P-10	80 ns 100 ns	600 mil 32 pin Plastic DIP (DP-32)
HM6585121.P-8LV HM6585121.P-10LV	80 ns 100 ns	
HM6585121.FP-8 HM6585121.FP-10	80 ns 100 ns	32 pin Plastic SOP (FP-32D)
HM6585121.FP-8LV HM6585121.FP-10LV	80 ns 100 ns	

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{18}	Address
I/O_0–I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Item	Symbol	HM658512-8		HM658512-10		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	ns	
Chip Enable Access Time	t_{CEA}	—	80	—	100	ns	
Read-Modify-Write Cycle Time	t_{RWC}	180	—	220	—	ns	
Output Enable Access Time	t_{OEA}	—	30	—	40	ns	
Chip Disable to Output in High-Z	t_{CHZ}	0	25	0	25	ns	1
Chip Enable to Output in Low-Z	t_{CLZ}	20	—	20	—	ns	2
Output Disable to Output in High-Z	t_{OHZ}	—	25	—	25	ns	1
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	ns	2
Chip Enable Pulse Width	t_{CE}	80 ns	10 μs	100 ns	10 μs		
Chip Enable Pre-Charge Time	t_P	40	—	50	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Address Hold Time	t_{AH}	20	—	25	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	
Write Command Pulse Width	t_{WP}	25	—	30	—	ns	
Chip Enable to End of Write	t_{CW}	80	—	100	—	ns	
Chip Enable to Output Enable Delay Time	t_{OCD}	0	—	0	—	ns	
Output Enaole Hold Time	t_{OHC}	15	—	15	—	ns	
Data in to End of Write	t_{DW}	20	—	25	—	ns	
Data in Hold Time for Write	t_{DH}	0	—	0	—	ns	
Output Active From End of Write	t_{OW}	5	—	5	—	ns	2
Write to Output in High-Z	t_{WHZ}	—	20	—	25	ns	1
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	
Refresh Command Delay Time	t_{RFD}	40	—	50	—	ns	
Refresh Precharge Time	t_{FP}	40	—	40	—	ns	
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80 ns	8 μs	80 ns	8 μs		
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	ns	
Refresh Command Pulse Width for Self Refresh	t_{FAS}	8	—	8	—	μs	
Refresh Reset Time From Self Refresh	t_{RFS}	600	—	600	—	ns	
Refresh Period	t_{REF}	—	32	—	32	ms	2048 cycle

NOTES:

1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} (min.) and V_{IL} (max.).
7. After power-up, pause for more than 100 μs and execute at least 8 initialization cycles, preferably as 8 refresh cycles.
8. 2048 cycles of burst refresh or distributed automatic refresh must be executed within 15 μs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycle.

Our Standards Set Standards

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1091/20M/GI/RD
Order Number: M12T014

Our Standards Set Standards

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391/25M/GI/LP/RD
Order Number: M12T014