

10-1 A
May 1990

0,8 μm - Technology.

Hitachi Memory
Quick Reference
Guide

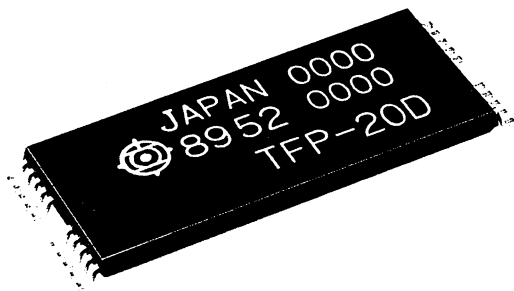
- 4M DRAMs ●
- 1M SRAMs ●
- 4M EPROMs ●
- 1M Flash EEPROMs ●
- 4M Pseudo Static RAMs ●
- 8/16 Mbit MASK ROMs ●



 **HITACHI**

0,8 μm - Technology.

- 4M DRAMs ●
- 1M SRAMs ●
- 4M EPROMs ●
- 1M Flash EEPROMs ●
- 4M Pseudo Static RAMs ●
- 8/16 Mbit MASK ROMs ●



 **HITACHI**

MOS MEMORIES

Dynamic RAM

Capacity	Config. (word x bit)	Process	Product Number (Package Code)	Suffix	Characteristics		
					Access (ns) max	max Icc (mA) Act./Std-by	
4M	4Mx1	C 0.8 μm	HM514100JP/LJP (CP-20DA) ZP/LZP (ZP-20)	-12	120	70/2 (0.3)	
				-10	100	80/2 (0.3)	
			-8	80	90/2 (0.3)		
			-8H	80	90/2 (0.3)		
			-10	100	80/2 (0.3)		
			-8	80	90/2 (0.3)		
			-7	70	100/2 (0.3)		
			-65	65	110/2 (0.3)		
			-6R	60	110/2 (0.3)		
			-10	100	80/2 (0.3)		
	4M		1Mx4	HM514400JP/LJP (CP-20DA) ZP/LZP (ZP-20)	-12	120	70/2 (0.3)
					-10	100	80/2 (0.3)
				-8	80	90/2 (0.3)	
				-8H	80	90/2 (0.3)	
				-10	100	80/2 (0.3)	
				-8	80	90/2 (0.3)	
				-7	70	100/2 (0.3)	
				-65	65	110/2 (0.3)	
				-6R	60	110/2 (0.3)	
				-10	100	80/2 (0.3)	
4M	512Kx8	HM514400AS/ALS (CP-20D) AZ/ALZ (ZP-20) AJ/ALJ (CP-20DA)	-8	80	90/2 (0.3)		
			-7	70	100/2 (0.3)		
		-65	65	110/2 (0.3)			
		-6R	60	110/2 (0.3)			
		-12	120	70/2			
		-10	100	80/2			
		-8	80	90/2			
		-8H	80	90/2			
		-12	120	70/2			
		-10	100	80/2			
4M	512Kx8	HM514410JP (CP-20DA) ZP (ZP-20)	-12	120	70/2		
			-10	100	80/2		
		-8	80	90/2			
		-8H	80	90/2			
		-12	120	70/2			
		-10	100	80/2			
		-8	80	90/2			
		-8H	80	90/2			
		-12	120	70/2			
		-10	100	80/2			
4M	512Kx8	HM514412JP* (CP-20DA) ZP* (ZP-20)	-12	120	70/2		
			-10	100	80/2		
		-8	80	90/2			
		-8H	80	90/2			
		-12	120	70/2			
		-10	100	80/2			
		-8	80	90/2			
		-8H	80	90/2			
		-12	120	70/2			
		-10	100	80/2			
32M	4Mx8	C 0.8 μm	HB56A48A (SIP-30) AT (SIP-30) B (SIM-30)	-12	120	560/16	
				-10	100	640/16	
			-8	80	720/16		
			-8F	80	720/16		
			-12	120	560/16		
			-10	100	640/16		
			-8	80	720/16		
			-8H	80	720/16		
			-12	120	560/16		
			-10	100	640/16		
36M	4Mx9	C 0.8 μm	HB56A49A (SIP-30) AT (SIP-30) B (SIM-30)	-12	120	630/18	
				-10	100	720/18	
			-8	80	810/18		
			-8F	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
			-8	80	810/18		
			-8H	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
32M	1Mx32	C 0.8 μm	HB56A49B (SIP-30) HB56A49BR (SIM-30)	-12	120	630/18	
				-10	100	720/18	
			-8	80	810/18		
			-8F	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
			-8	80	810/18		
			-8H	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
64M	2Mx32	C 0.8 μm	HB56B49A (SIP-30) AT (SIP-30) B (SIM-30)	-12	120	630/18	
				-10	100	720/18	
			-8	80	810/18		
			-8F	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
			-8	80	810/18		
			-8H	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
36M	1Mx36	C 0.8 μm	HB56C49A (SIP-30) AT (SIP-30) B (SIM-30)	-12	120	630/18	
				-10	100	720/18	
			-8	80	810/18		
			-8F	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
			-8	80	810/18		
			-8H	80	810/18		
			-12	120	630/18		
			-10	100	720/18		
36M	1Mx36	C 0.8 μm	HB56D132BR (SIM-72)	-12	120	560/16	
				-10	100	640/16	
			-8	80	720/16		
			-8F	80	720/16		
			-12	120	560/16		
			-10	100	640/16		
			-8	80	720/16		
			-8H	80	720/16		
			-12	120	560/16		
			-10	100	640/16		
64M	2Mx32	C 0.8 μm	HB56D232B (SIM-72)	-12	120	600/32	
				-10	100	680/32	
			-8	80	760/32		
			-8F	80	760/32		
			-12	120	600/32		
			-10	100	680/32		
			-8	80	760/32		
			-8H	80	760/32		
			-12	120	600/32		
			-10	100	680/32		
36M	1Mx36	C 0.8 μm	HB56D136B/BR (SIM-72)	-12	120	760/24	
				-10	100	880/24	
			-8	80	1000/24		
			-8F	80	1000/24		
			-12	120	760/24		
			-10	100	880/24		
			-8	80	1000/24		
			-8H	80	1000/24		
			-12	120	760/24		
			-10	100	880/24		

DRAM Module

MOS MEMORIES

DRAM Module

Static RAM

Pseudo SRAM

SRAM Module

EPROM

FLASH-EEPROM

MASK ROM

Multiport Video RAM

Capacity	Config. (word x bit)	Process	Product Number (Package Code)	Suffix	Characteristics	
					Access (ns) max	max Icc (mA) Act./Std-by
72M	2Mx36	C 0.8 μm	HB56D236B (SIM-72)	-12 -10 -8 -8F	120 100 80 80	820/48 940/48 1060/48 1060/48
1M	256Kx4	C 0.8 μm	HM624256P (DP-28)	-45	45	120/2
			JP (CP-28D)	-35	35	
	HM624257JP (CP-32D)		-45	45	120/2	
			-35	35		
	128Kx8		HM628128P/LP (DP-32)	-12	120	70/2 (0.05)
			FP/LFP (FP-32D)	-10 -8	100 85	
	HM628128LFP-xxSL (FP-32D)	-7 -12	70 120	70/2 (0.05)		
		-10 -8	100 85			
	HM628128LT/LR (TFP-32D)	-12	120	70/2 (0.05)		
		-10 -8	100 85			
4M	512Kx8	C 0.8 μm	HM658512DP/LP (DP-32) DFP/LFP (FP-32D)	-12 -10 -8	120 100 80	75/2 (0.2)
4M	512Kx8	C 0.8 μm	HM66205L (DM-32A)	-12 -10 -8	120 100 85	80/(0.4)
4M	256Kx16	C 0.8 μm	HN27C4096G (DG-40A)	-15 -12 -10	150 120 100	100 (10MHz) /0.02
			HN27C4096CC (CC-44)	-15 -12	150 120	100 (10MHz) /0.02
				-10	100	
			HN27C4096CP* (CP-44)	-15 -12	150 120	TBD
1M	128Kx8	C 0.8 μm	HN29C101P (DP-32)	-15 -12	150 120	TBD
			HN29C101T* (TFP-32DA)	-15 -12	150 120	TBD
4M	512Kx8 256Kx16	C 0.8 μm	HN62414P (DP-40)		200	50/0.03
			HN62414FP (FP-44A)	Z	170	
			F (FP-48)			
			HN62444BP* (DP-40)		100	50/0.03
	BCP* (CP-44)					
	HN62314BP (DP-32)			200	50/0.03	
	BF (FP-32DA)		Z	170		
	HN62444P (DP-40)			100	50/0.03	
	FP (FP-44A)					
	F (FP-48)					
	TFP (TFP-44)					
	HN62344BP (FP-44A)			100	50/0.03	
8M	1Mx8	HM62408P (DP-42)		200	50/0.03	
	512Kx16	FP (FP-44A)				
		F (FP-48)				
1Mx8	HN62308BP (DP-32)		200	50/0.03		
16M	2Mx8 1Mx16	BF (FP-32D)				
		HN624016P (DP-42)		200	50/0.03	
		F (FP-48)				
1M	RAM 256Kx4 SAM 512x4 RAM 128Kx8 SAM 256x8	C 0.8 μm	HM534251A/3AJP* (CP-28D)	-10 -8	100/25 80/25	100/7 115/7
			AZP* (ZP-28)			
			HM538121A/3AJP* (CP-40D)	-10 -8	100/25 80/25	TBD

* under development

SUBMICRON MOS MEMORY SHORTFORM

FOREWORD

May, 1990

This is the first edition of the Hitachi Submicron MOS Memory Shortform. It contains information about the currently available Hitachi Submicron Memory Products.

All products are designed and manufactured with leading edge 0.8 micron design rules. This technology provides many advantages to engineers and system designers, including higher density, faster speeds, lower power, and increased package variety - particularly in modules.

This book contains an overview of all DRAM with x 1, x 8, x 9, x 16, and x 18 configurations; through-hole ZIP and surface mount SOJ packages; standard and low power options; and with four operating modes including fast page, write per bit, nibble and static columns. Hitachi also offers 4 Megabit DRAMS in 300 mil wide SOJ packages and TSOP packages. Modules are described with data widths of x 8, x 9, x 32 and x 36.

Other devices are in design and in the initial stages of production. In addition to the information included here, Hitachi can supply devices and data sheets with 60 and 65ns access times. Ask for:

HM514100AJ/AZ-65

HM514100AJ/AZ-6R

HM514400AJ/AZ-65

HM514400AJ/AZ-6R

In addition to the 4 Megabit DRAM devices and modules, all other submicron products like 1 Megabit EPROM, 4 Megabit PSRAM, 4 Megabit EPROM, 1 Megabit Flash EEPROM and 4, 8, 16 Megabit MaskROMS are also included in this shortform.

New designs will continue to evolve from this advanced technology. Faster speeds, slimmer packages, devices with wider data busses and an increasing variety of modules, including custom designs, will meet the requirements of specific customers and applications.

For additional information, contact the nearest Hitachi Europe Ltd. sales office, Representative or Distributor. For your convenience, Hitachi sales locations are listed at the end of this book.

This document contains information on new products.
Specifications and information contained herein are
Subject to change without notice.

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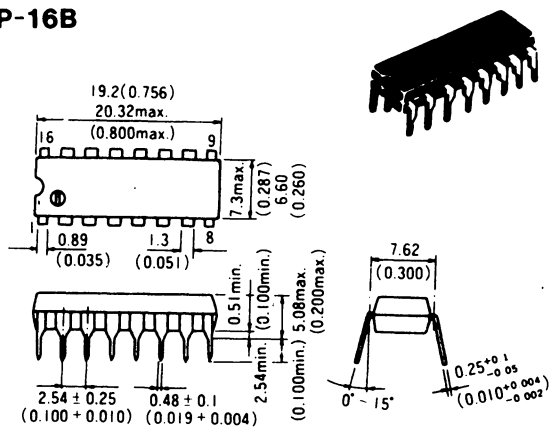
Package Information

PACKAGE INFORMATION

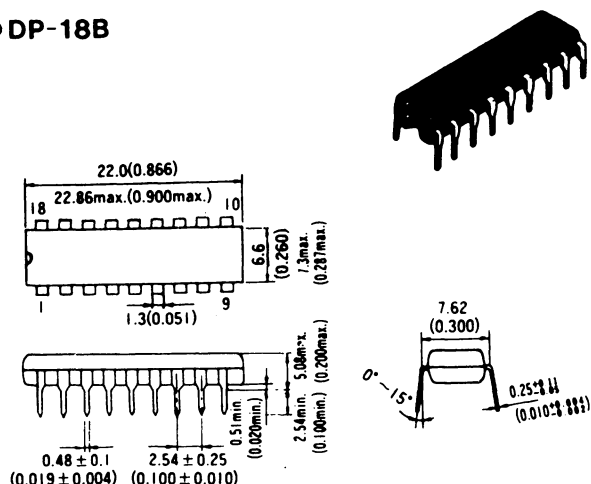
● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

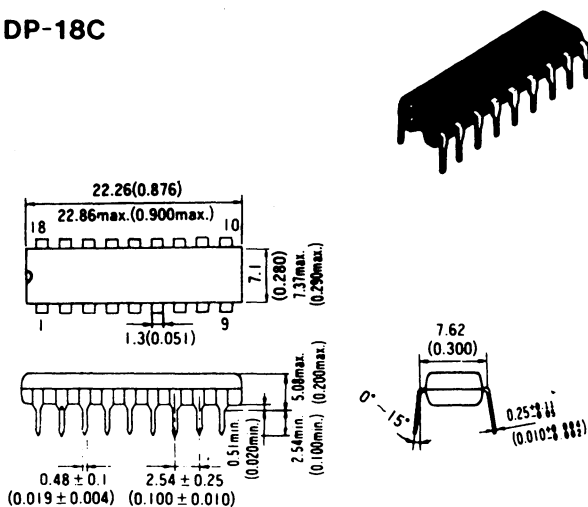
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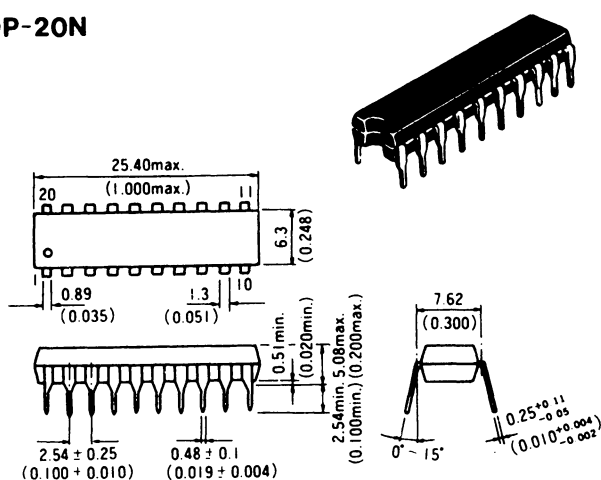
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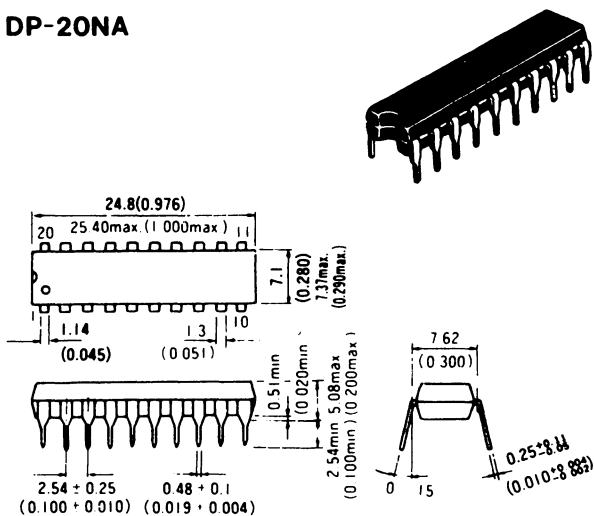
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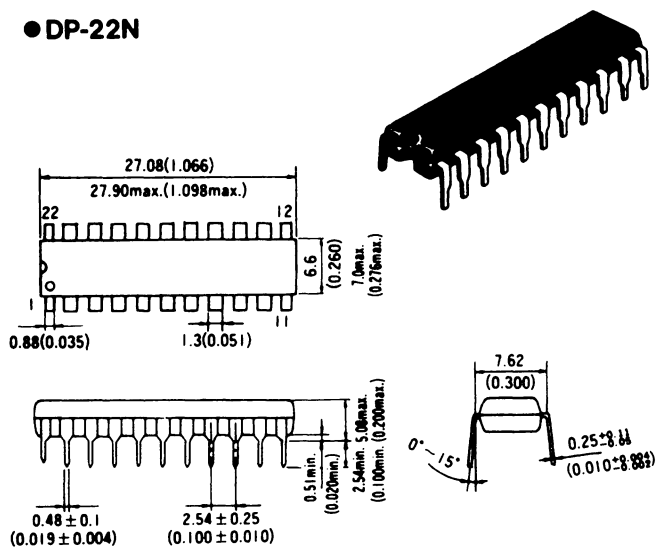
● DP-20N



● DP-20NA



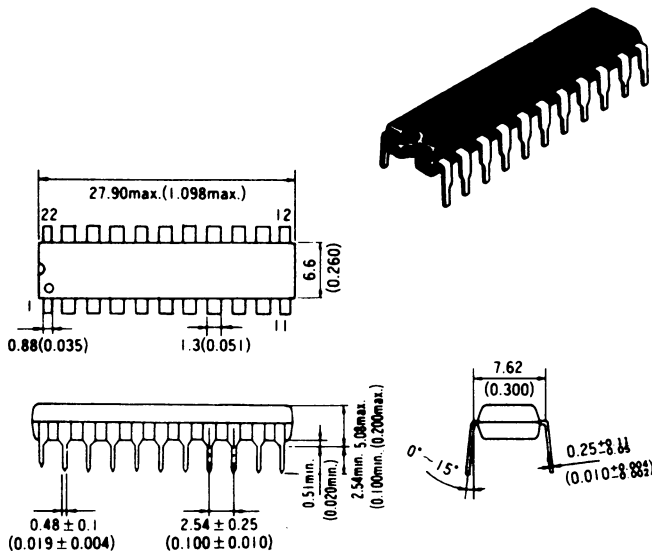
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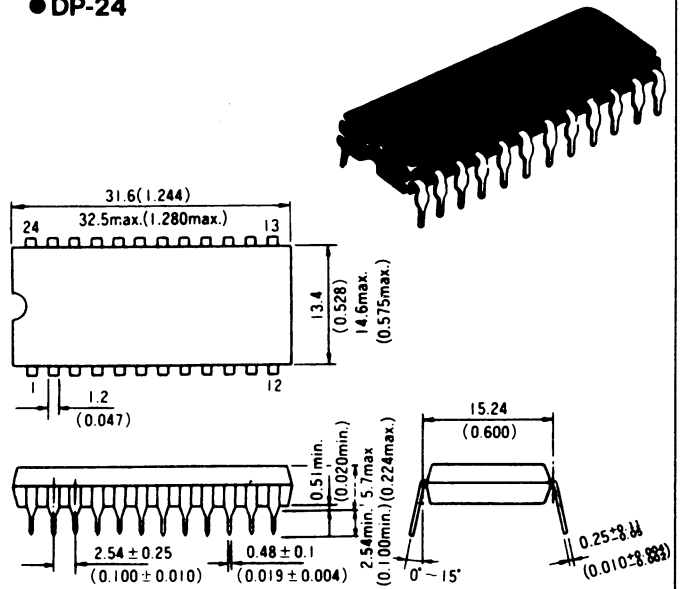
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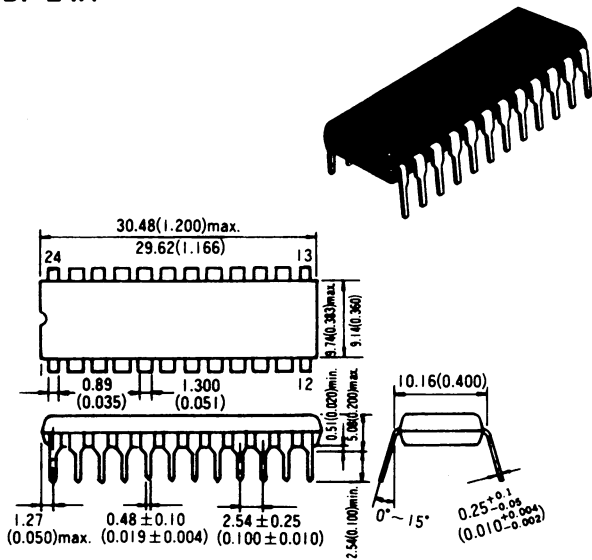
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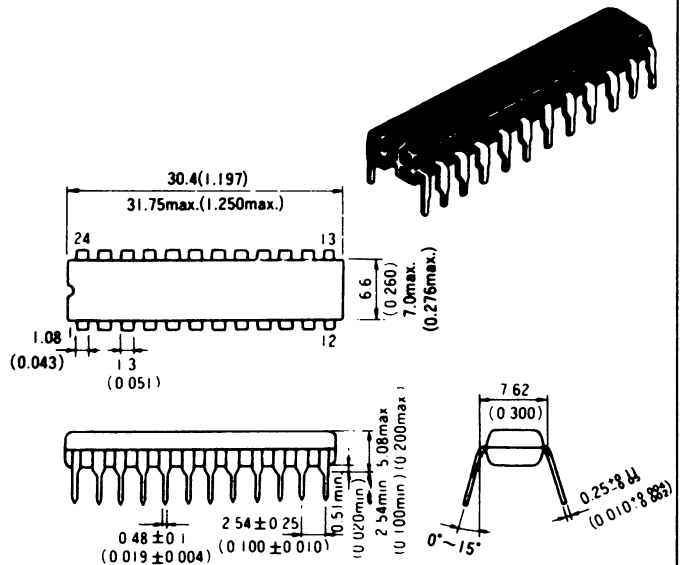
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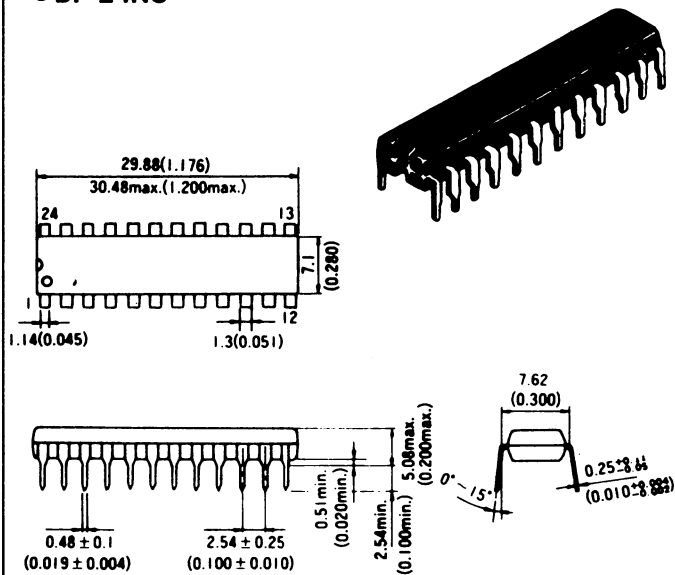
● DP-24A



● DP-24N

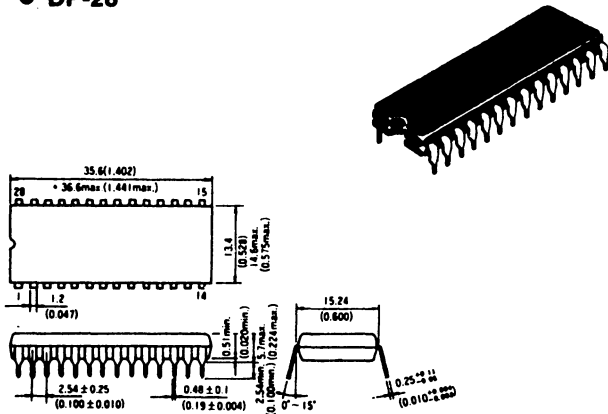


● DP-24NC

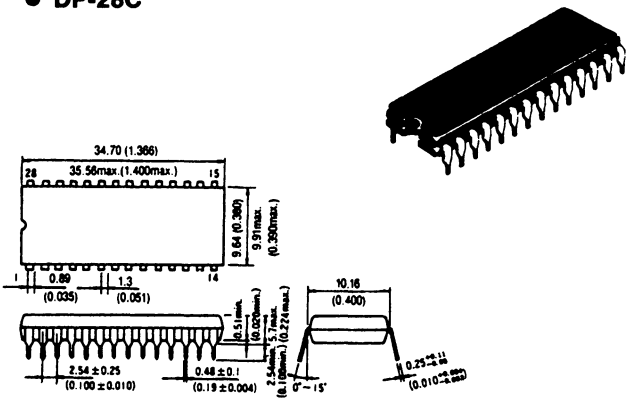


● Dual-in-line Plastic

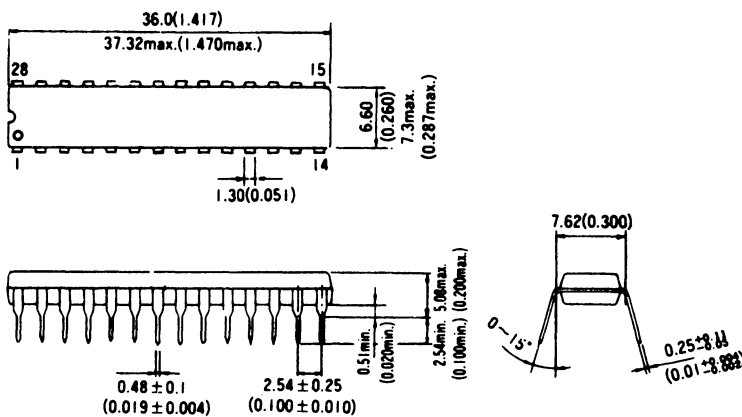
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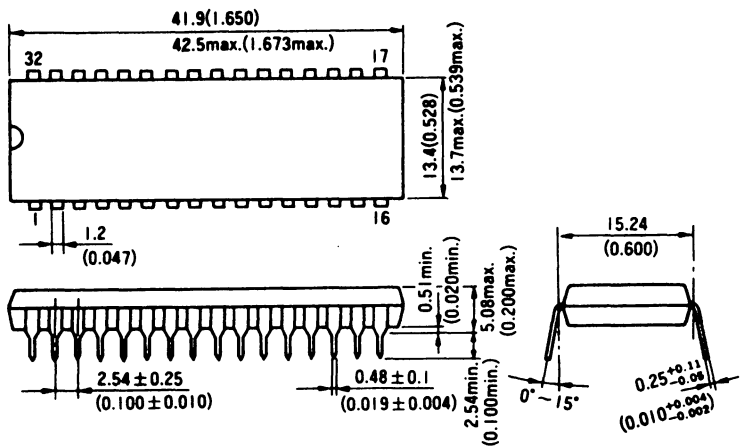
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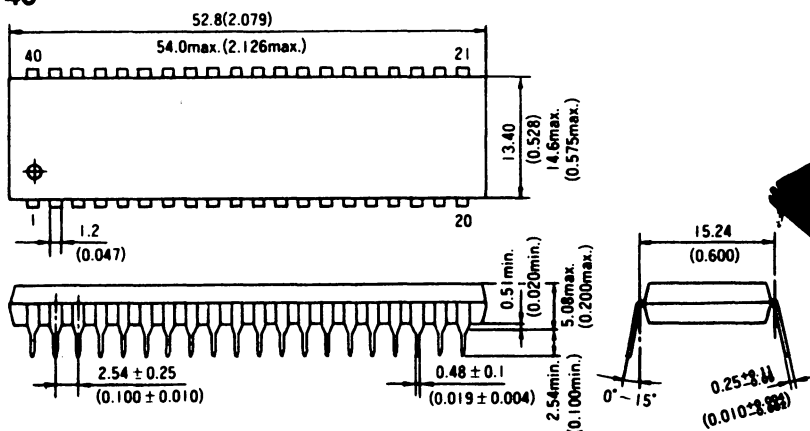
● DP-28N



● DP-32



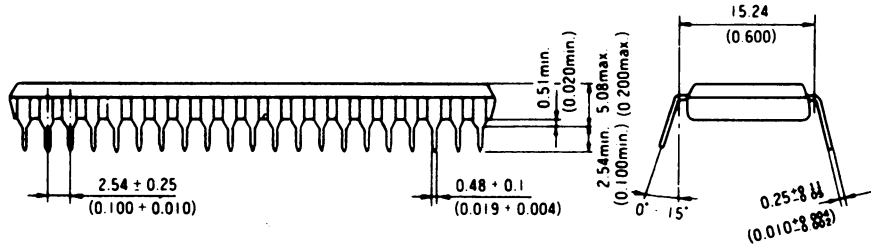
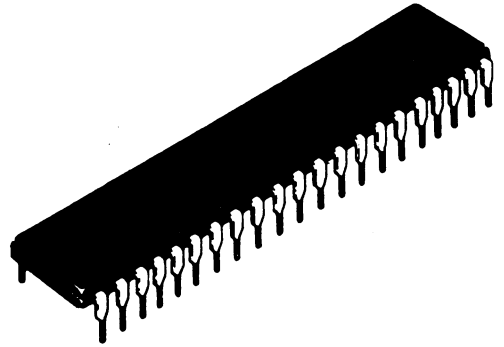
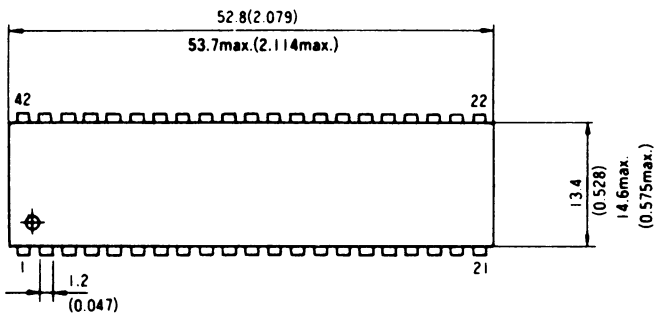
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● Dual-in-line Plastic

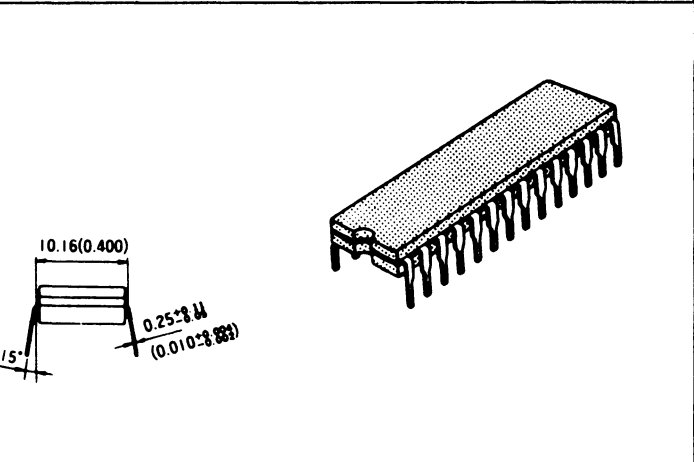
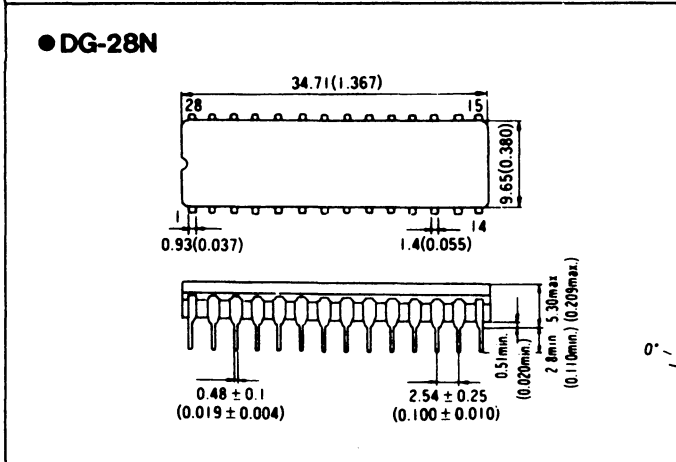
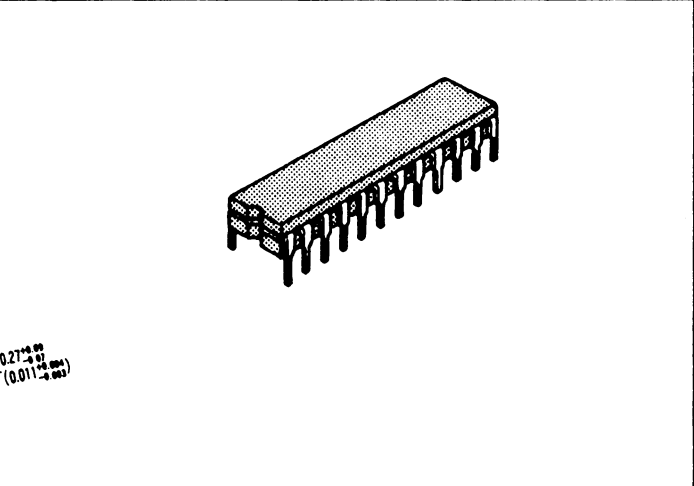
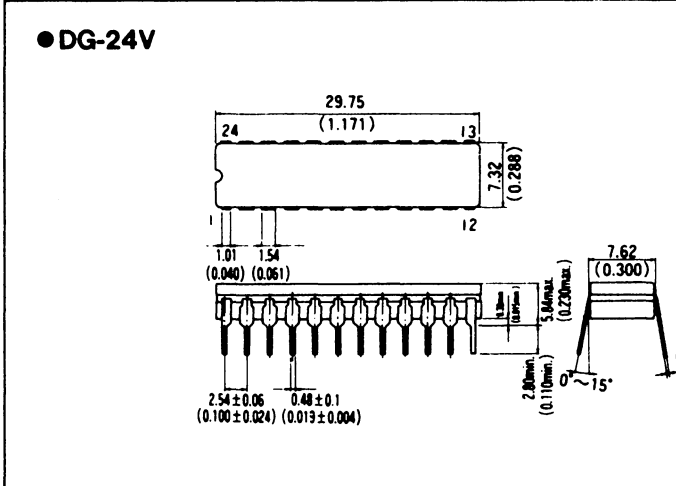
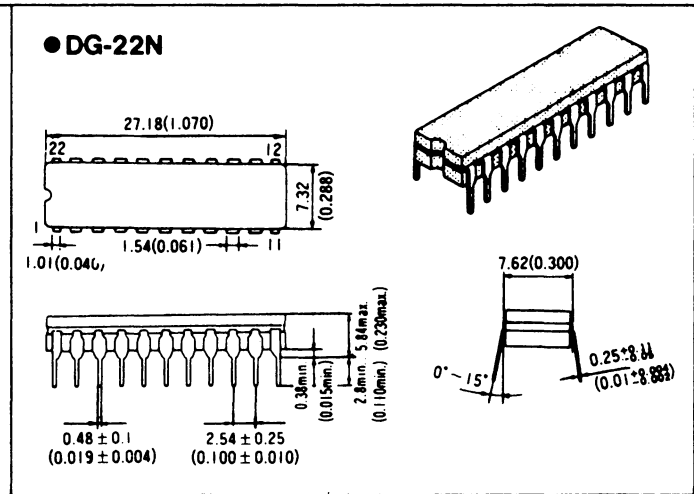
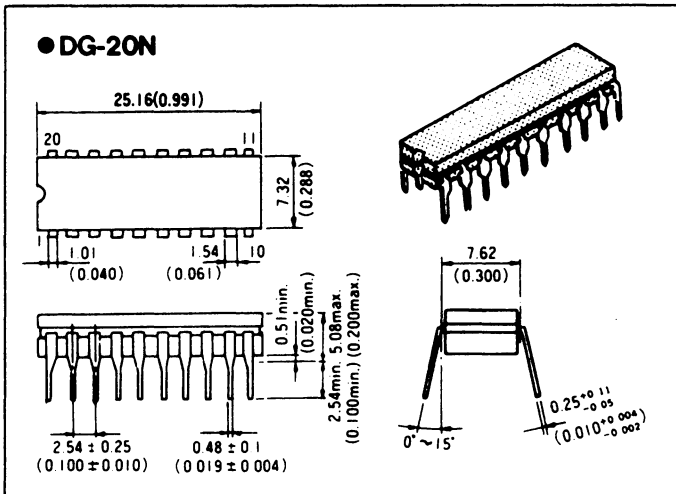
Unit: mm (inch) Scale 1/1

● DP-42



● CERDIP

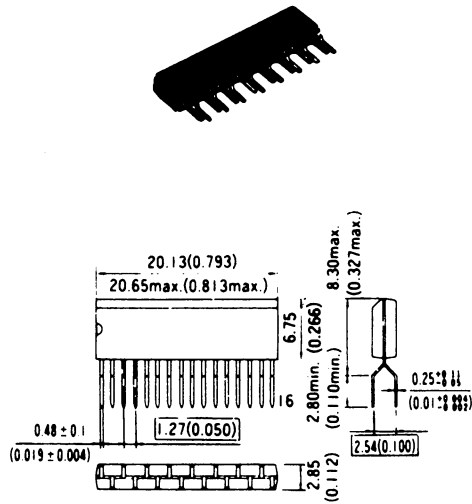
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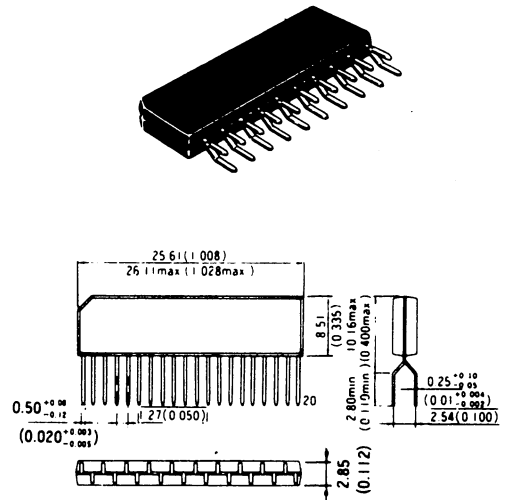
● Zigzag-in-line Plastic

Unit: mm (inch) Scale 1/1

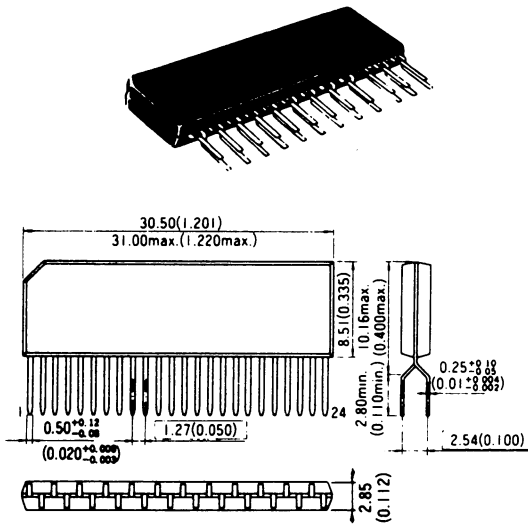
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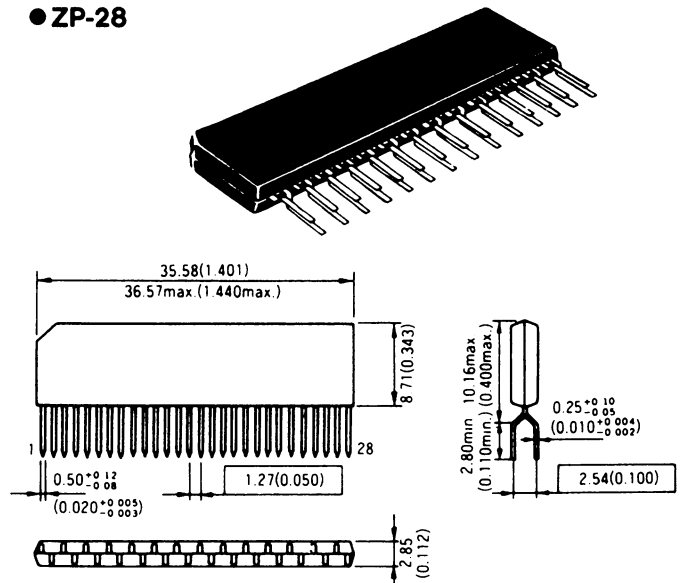
● ZP-20



● ZP-24

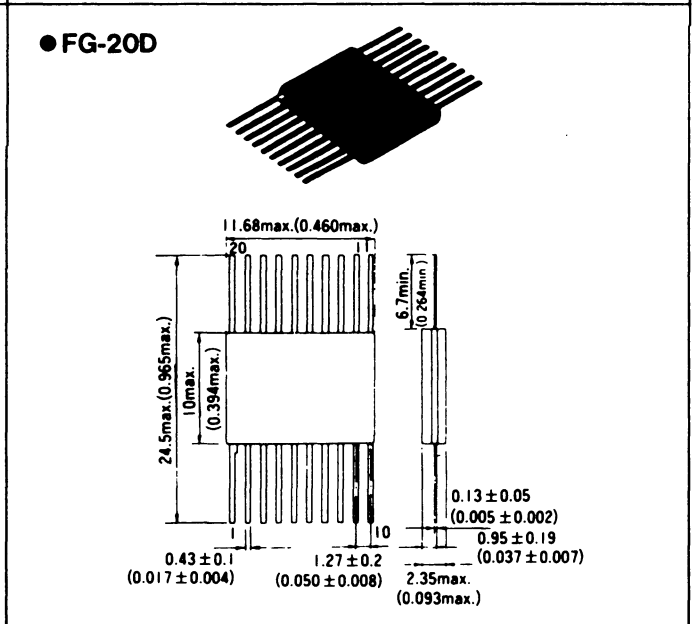
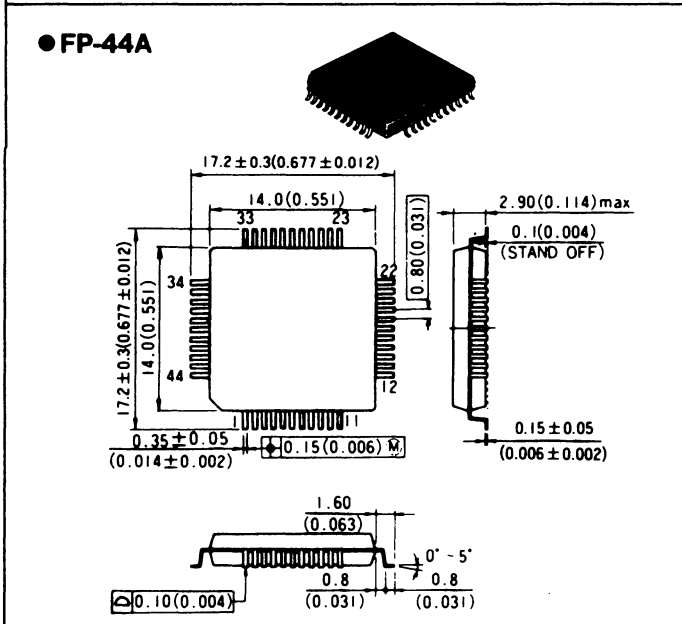
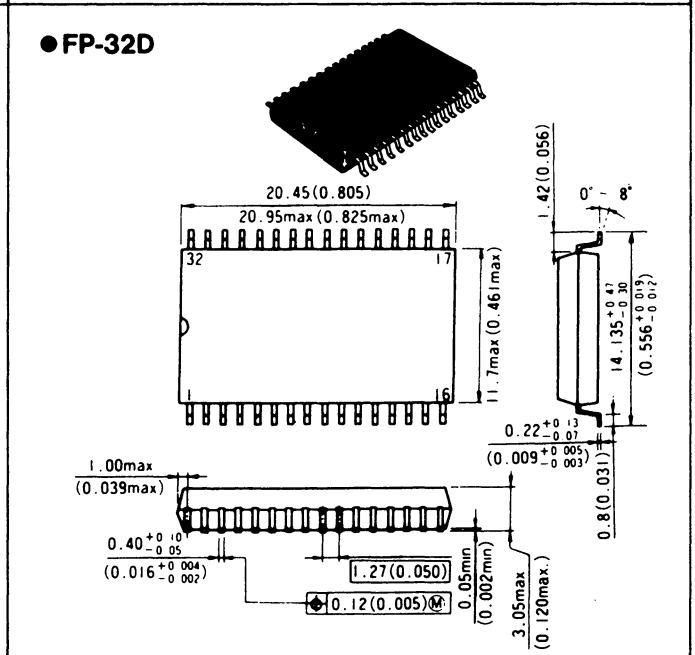
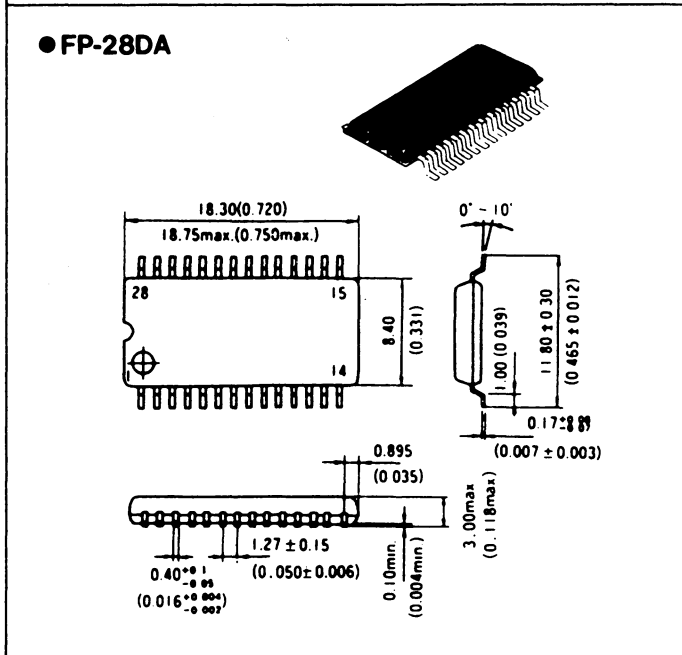
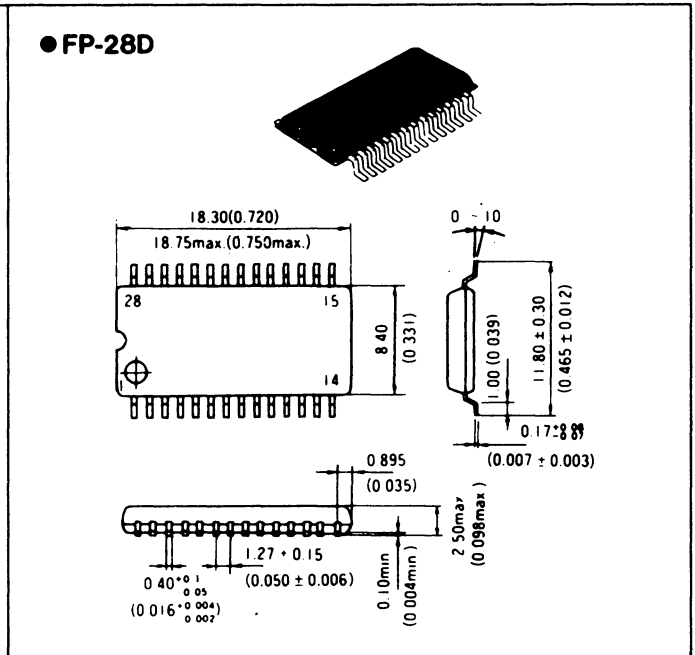
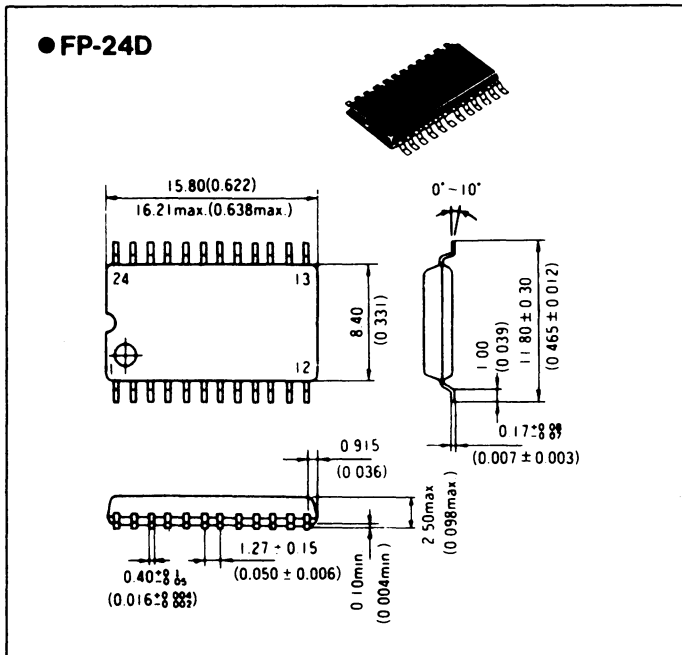


● ZP-28



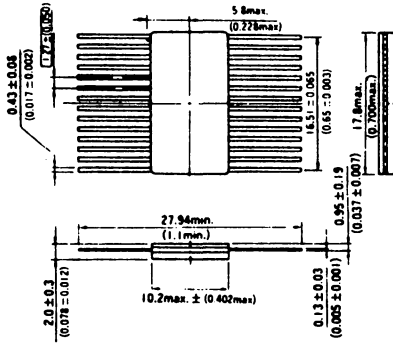
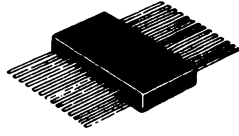
● Flat Package

Unit mm (inch) Scale 1/2

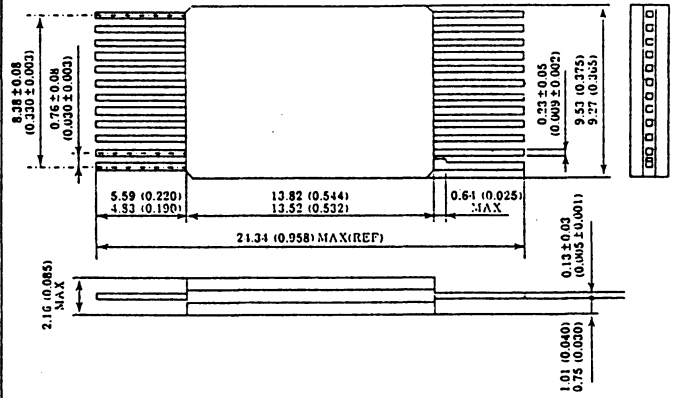


● Flat Packages (continued)

● FG-28D

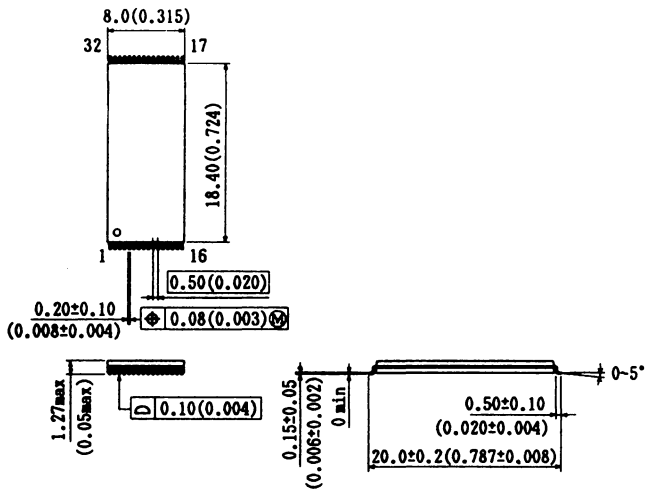


● FG-24A

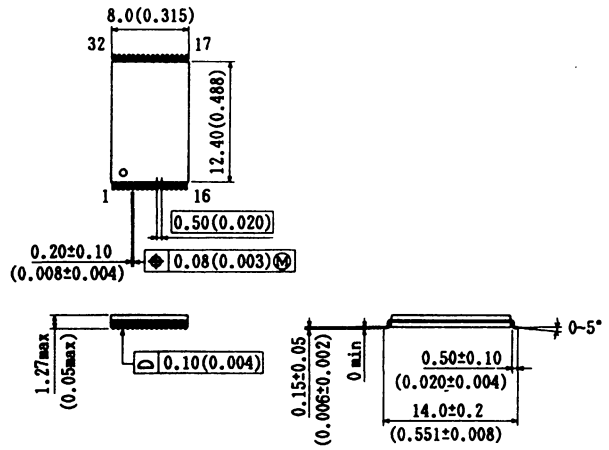


● TSOP Packages

● TFP-32D

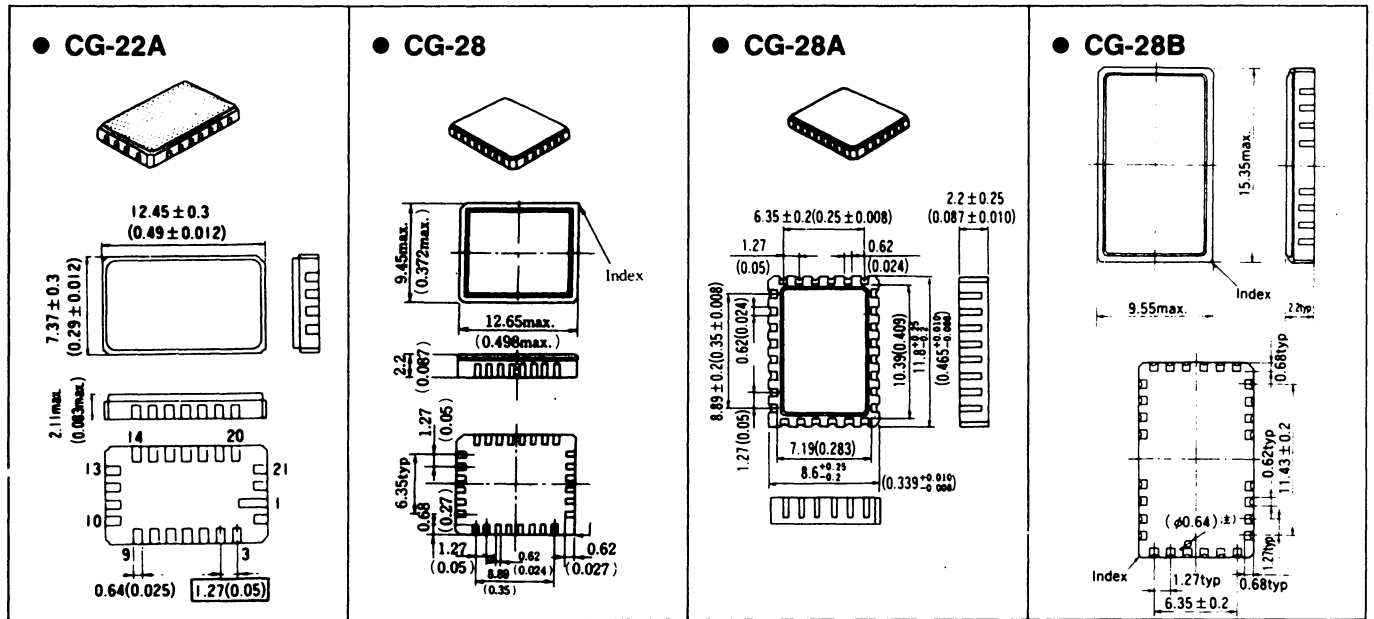


● TFP-32DA

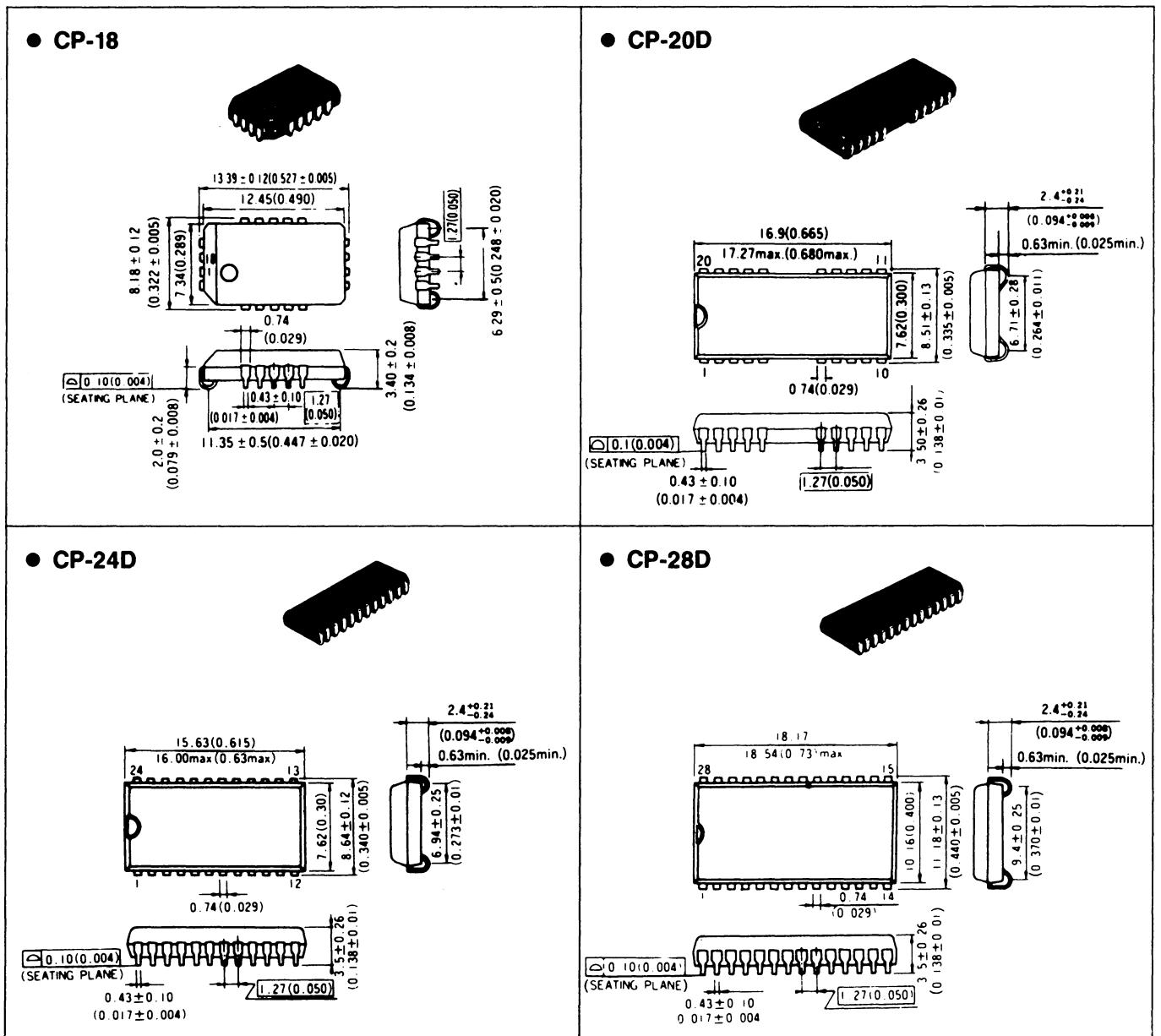


PACKAGE INFORMATION

● **Leadless Chip Carrier**



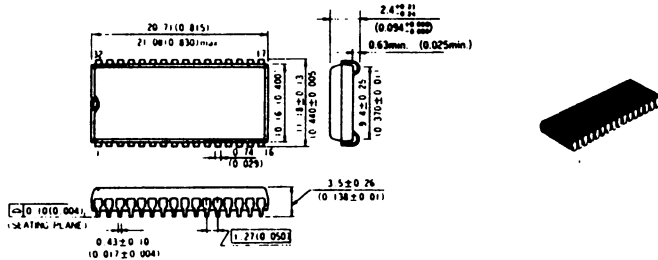
● **Flat Package (J-bend Leads)**



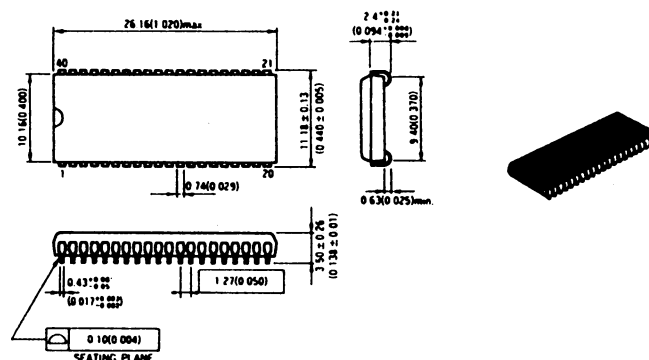
● Flat Packages (J-Bend Leads) (continued)

Unit: mm (inch) Scale 1½

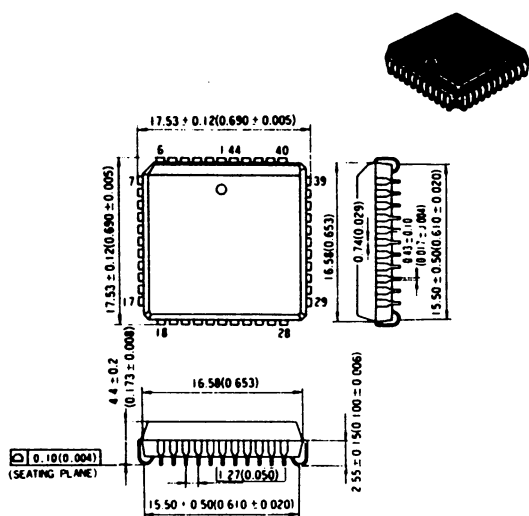
● CP-32D



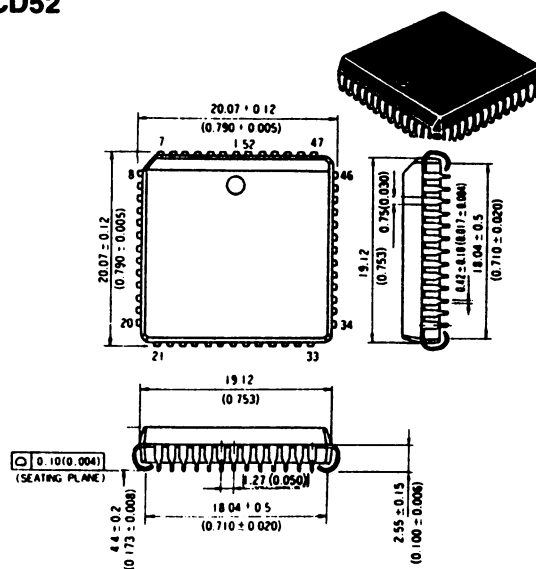
● CP-40D



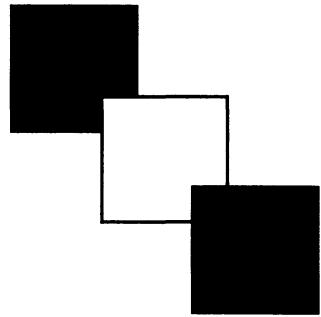
● CP-44



● CD52



Rev. 5
Dec. 29, 1989



HM514100JP/ZP-8/10/12

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

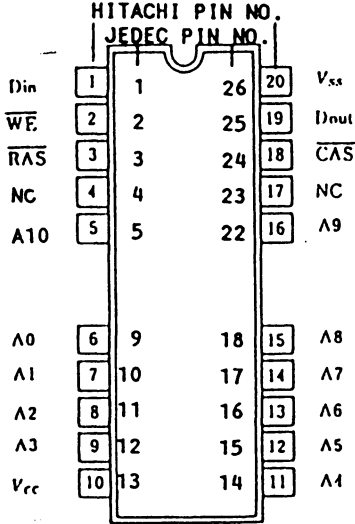
- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- * Test function

Ordering Informations

Part No.	Access	Package
HM514100JP-8	80 ns	350 mil 20-pin plastic SOJ
HM514100JP-10	100 ns	
HM514100JP-12	120 ns	
HM514100ZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514100ZP-10	100 ns	
HM514100ZP-12	120 ns	

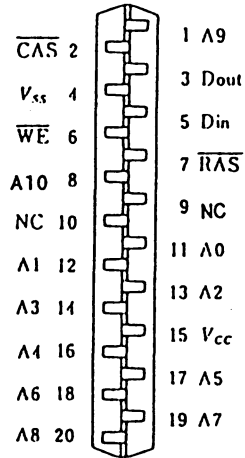
Pin Out

• HM514100JP Series



(Top View)

• HM514100ZP Series

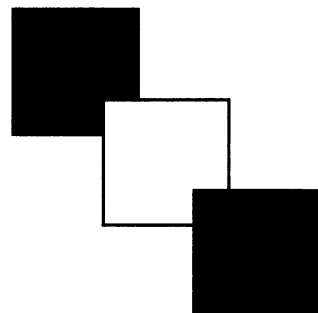


(Bottom View)

Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
DIN	Data-in
DOUT	Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
VCC	Power (+5V)
VSS	Ground

Rev. 3
Feb. 23, 1990



HM514100LJP/LZP-8/10/12

(Low Power Version)

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (128 ms)
- * 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- * Test function
- * Battery back up operation

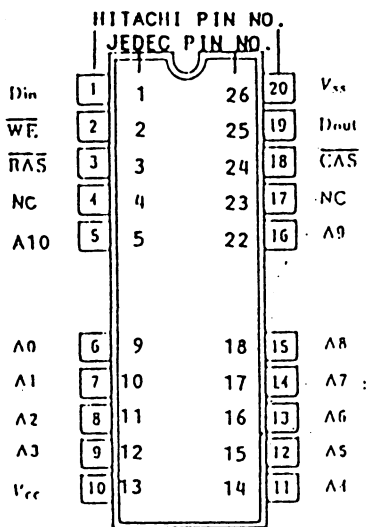
Ordering Informations

Part No.	Access	Package
HM514100LJP-8	80 ns	350 mil 20-pin plastic SOJ
HM514100LJP-10	100 ns	
HM514100LJP-12	120 ns	
HM514100LZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514100LZP-10	100 ns	
HM514100LZP-12	120 ns	

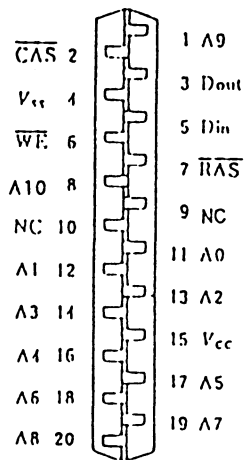
Pin Out

• HM514100LJP Series

• HM514100LZP Series



(Top View)



(Bottom View)

Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
DIN	Data-in
DOUT	Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
VCC	Power (+5V)
VSS	Ground

* DC Electrical Characteristics (Ta = 0 to +70 °C , VCC = 5 V ± 10 % , VSS = 0 V)

Parameter	Symbol	HM514100L		HM514100L		HM514100L		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating current	ICC1	-	90	-	80	-	70	mA	RAS, CAS cycling tRC = min	1,2
Standby current	ICC2	-	2	-	2	-	2	mA	TTL interface RAS, CAS = VIH Dout = High-Z	
		-	200	-	200	-	200	µA	CMOS interface RAS, CAS and WE ≥ VCC - 0.2V or ≤ 6.5 V Address and Din: stable Dout = High-Z	
RAS-only refresh current	ICC3	-	90	-	80	-	70	mA	tRC = min	2
Standby current	ICC5	-	5	-	5	-	5	mA	RAS = VIH CAS = VIL Dout = enable	1,4
CAS-before-RAS refresh current	ICC6	-	90	-	80	-	70	mA	tRC = min	
Fast page mode current	ICC7	-	90	-	80	-	70	mA	tPC = min	1,3
Battery back up operating current (standby with CBR refresh)	ICC10	-	300	-	300	-	300	µA	tRC = 125 µs tRAS ≤ 1 µs VCC - 0.2V ≤ VIH ≤ 6.5V 0V ≤ VIL ≤ 0.2V WE = VIH Address and Din: stable Dout = High-Z	
Input leakage current	ILI	-10	10	-10	10	-10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	ILO	-10	10	-10	10	-10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	VOH	2.4	VCC	2.4	VCC	2.4	VCC	V	High Iout = -5 mA	
Output low voltage	VOL	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Note:
1. ICC depends on output load condition when the device is selected, ICC max is specified at the output open condition.
 2. Address can be changed once or less while RAS = VIL.
 3. Address can be changed once or less while CAS = VIH.
 4. Clock voltages (RAS and CAS) must be applied simultaneously with or prior to applying supply voltage.

HM514100JP/ZP-8H

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 μ m CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V ($\pm 10\%$)
- * High speed
 - Access time
80 ns (max)
- * Low power dissipation
 - Active mode
495 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function

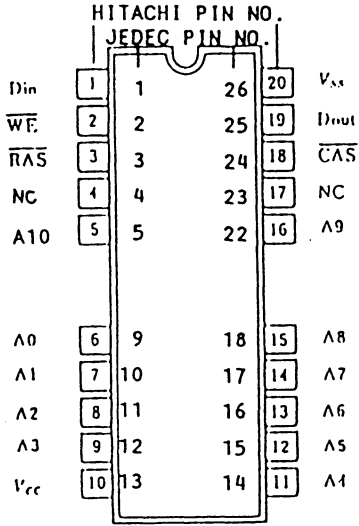
Ordering Informations

Part No.	Access	Package
HM514100JP-8H	80 ns	350 mil 20-pin plastic SOJ
HM514100ZP-8H	80 ns	400 mil 20-pin plastic ZIP

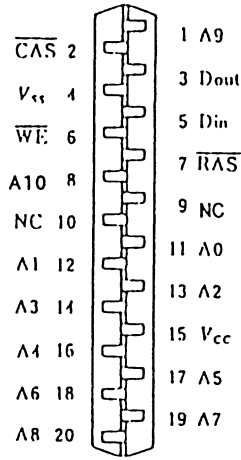
Pin Out

• HM514100JP Series

• HM514100ZP Series



(Top View)



(Bottom View)

Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
DIN	Data-in
DOUT	Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
VCC	Power (+5V)
VSS	Ground

Rev. 5
Dec. 29, 1989

HM514101JP/ZP-8/10/12

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514101 is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514101 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514101 offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM514101 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

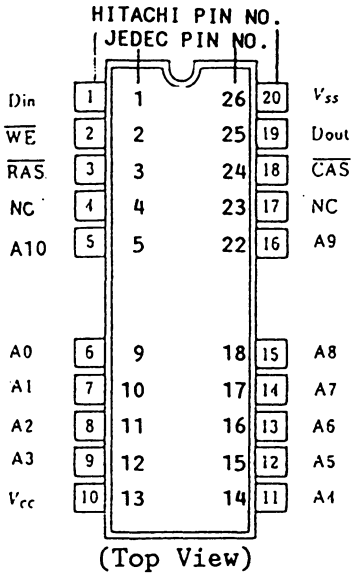
- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Nibble mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function

Ordering Informations

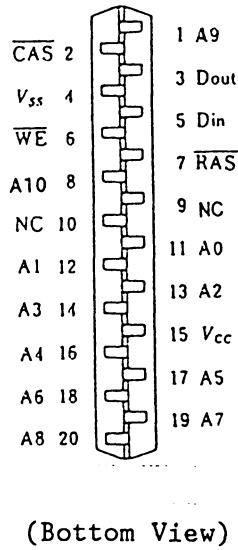
Part No.	Access	Package
HM514101JP-8	80 ns	350 mil 20-pin plastic SOJ
HM514101JP-10	100 ns	
HM514101JP-12	120 ns	
HM514101ZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514101ZP-10	100 ns	
HM514101ZP-12	120 ns	

Pin Out

• HM514101JP Series



• HM514101ZP Series



Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
DIN	Data-in
DOUT	Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read./Write Enable
VCC	Power (+5V)
VSS	Ground

HM514102JP/ZP-8/10/12

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514102 is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514102 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514102 offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM514102 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

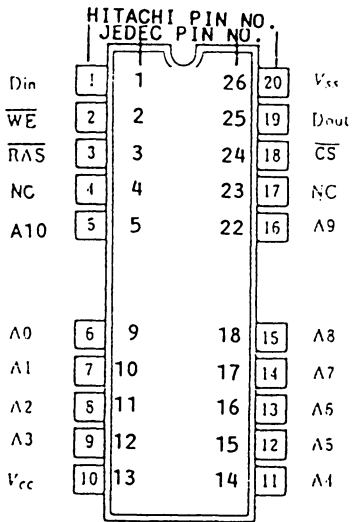
- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Static column mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CS-before-RAS refresh
 - Hidden refresh
- * Test function

Ordering Informations

Part No.	Access	Package
HM514102JP-8	80 ns	350 mil 20-pin plastic SOJ
HM514102JP-10	100 ns	
HM514102JP-12	120 ns	
HM514102ZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514102ZP-10	100 ns	
HM514102ZP-12	120 ns	

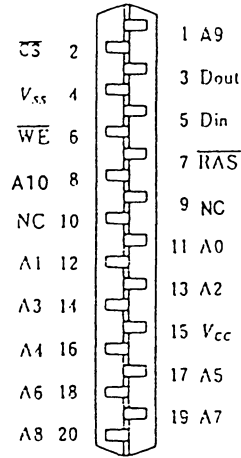
Pin Out

• HM514102JP Series



(Top View)

• HM514102ZP Series



(Bottom View)

Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
DIN	Data-in
DOUT	Data-out
RAS	Row Address Strobe
CS	Chip Select
WE	Read / Write Enable
VCC	Power (+5V)
VSS	Ground

NEW PRODUCT

Rev. 2
Jan. 12, 1990

HM514100AJ/AS/AZ-7/8/10

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514100A is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514100A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100A to be packaged in standard 350-mil 20-pin plastic SOJ, standard 300-mil 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

Ordering Informations

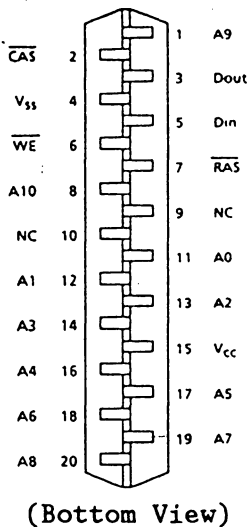
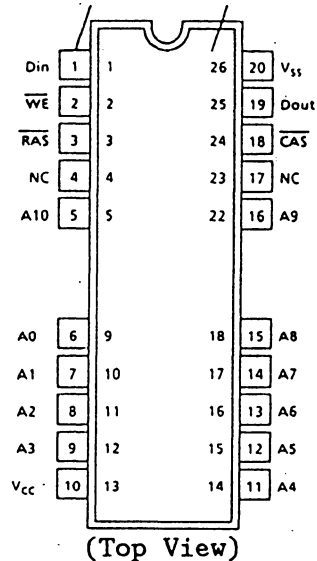
	Type No.	Access Time	Package
* Single 5 V (±10%)	HM514100AJ-7	70 ns	350-mil 20-pin
* High speed	HM514100AJ-8	80 ns	plastic SOJ
- Access time	HM514100AJ-10	100 ns	(CP-20DA)
70 ns/80 ns/100 ns (max)	HM514100AS-7	70 ns	300-mil 20-pin
* Low power dissipation	HM514100AS-8	80 ns	plastic SOJ
- Active mode	HM514100AS-10	100 ns	(CP-20D)
550 mW/495 mW/440 mW (max)	HM514100AZ-7	70 ns	400-mil 20-pin
- Standby mode 11 mW (max)	HM514100AZ-8	80 ns	plastic ZIP
* Fast page mode capability	HM514100AZ-10	100 ns	(ZP-20)
* 1,024 refresh cycles ---- (16 ms)			
* 3 variations of refresh			
- <u>RAS</u> -only refresh			
- <u>CAS</u> -before- <u>RAS</u> refresh			
- Hidden refresh			
* Test function			

Pin Out

- HM514100AJ Series
HM514100AS Series

- HM514100AZ Series

Hitachi Pin No. JEDEC Pin No.



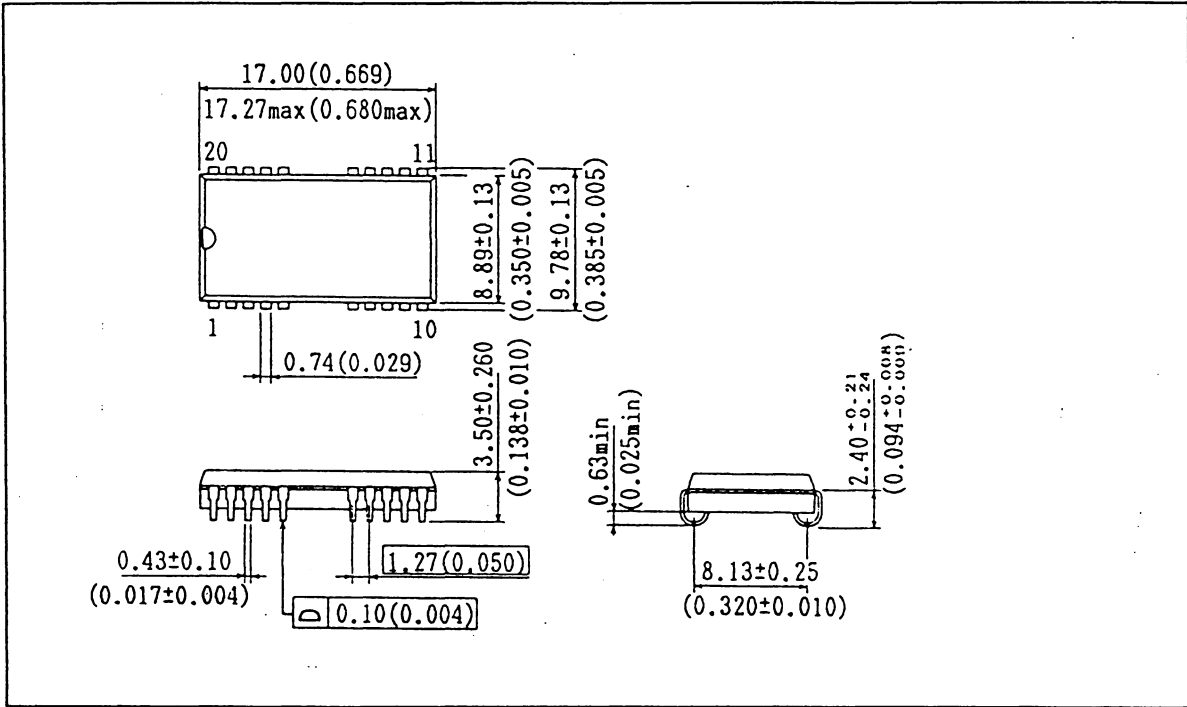
Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
Din	Data-in
Dout	Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
VCC	Power (+5V)
VSS	Ground
NC	No Connection

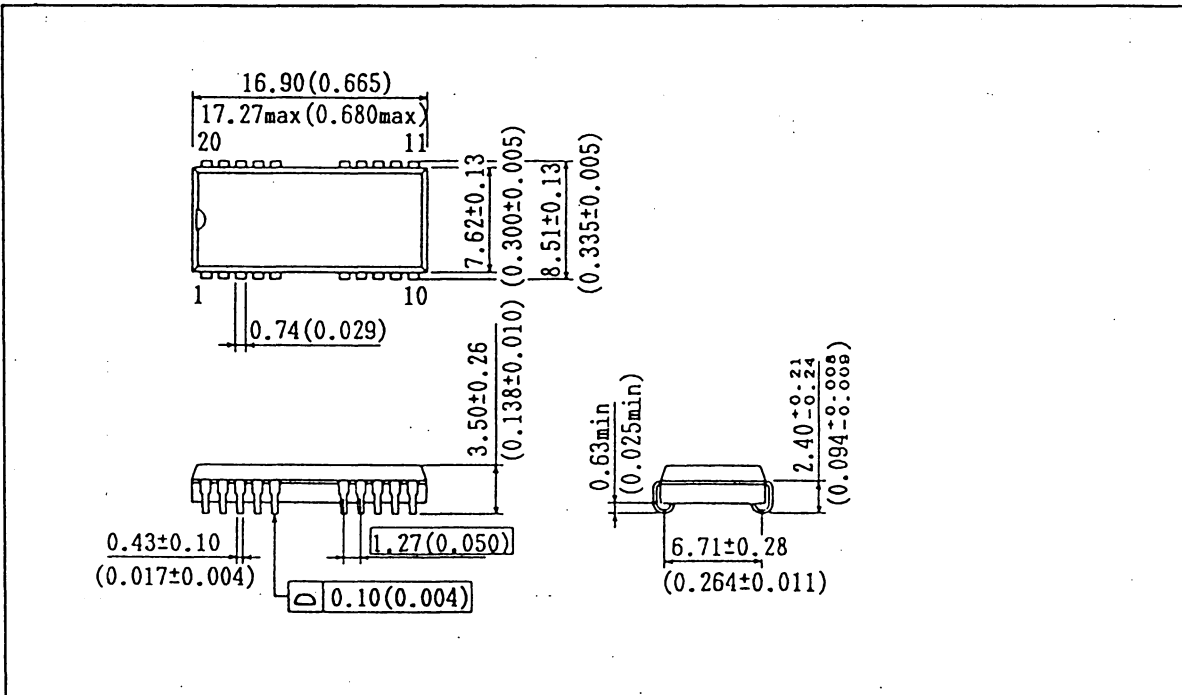
Outline Dimensions

Unit: mm(inch)

- HM514100AJ Series (CP-20DA)



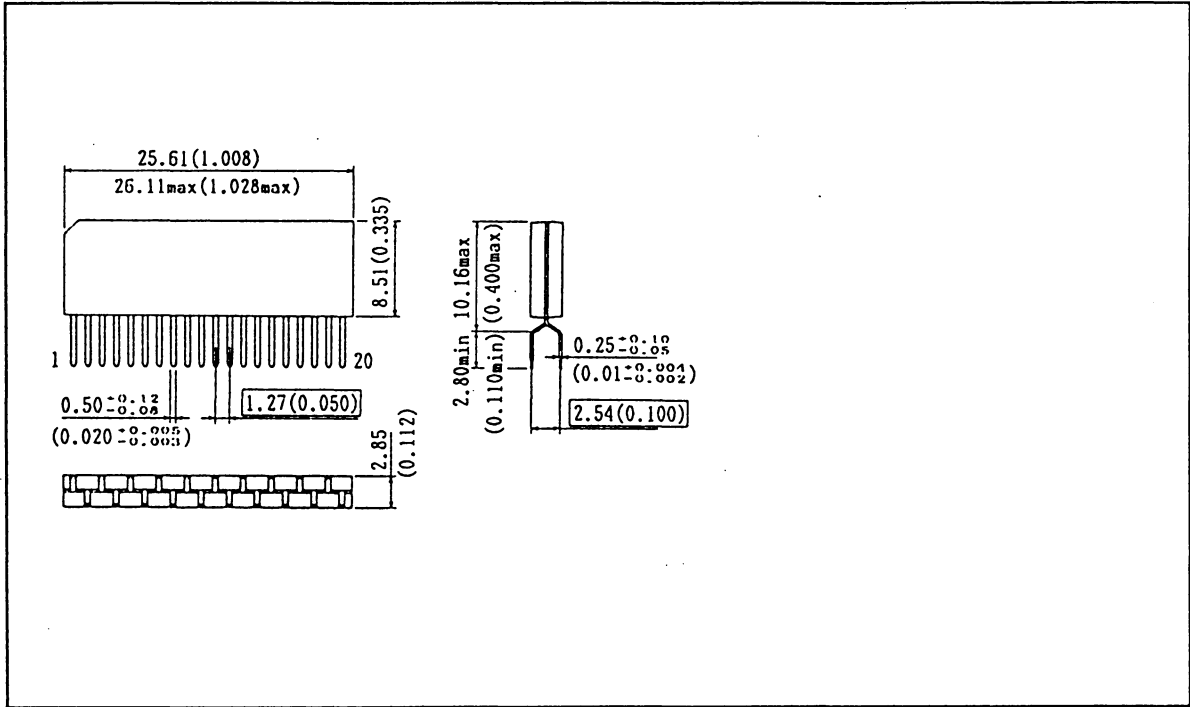
- HM514100AS Series (CP-20D)



Outline Dimensions (Continued)

Unit: mm(inch)

- HM514100AZ Series (ZP-20)



NEW PRODUCT

Rev. 0
Jan. 12, 1990

HM514101AJ/AS/AZ-7/8/10

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514101A is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514101A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514101A offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM514101A to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
70 ns / 80 ns / 100 ns (max)
- * Low power dissipation
 - Active mode
550 mW / 495 mW / 440 mW (max)
 - Standby mode 11 mW (max)
- * Nibble mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function

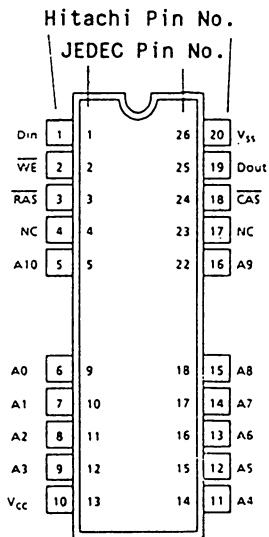
Ordering Informations

Part No.	Access	Package
HM514101AJ-7	70 ns	350 mil 20-pin
HM514101AJ-8	80 ns	plastic SOJ
HM514101AJ-10	100 ns	(CP-20DA)
HM514101AS-7	70 ns	300-mil 20-pin
HM514101AS-8	80 ns	plastic SPJ
HM514101AS-10	100 ns	(CP-20D)
HM514101AZ-7	70 ns	400 mil 20-pin
HM514101AZ-8	80 ns	plastic ZIP
HM514101AZ-10	100 ns	(ZP-20)

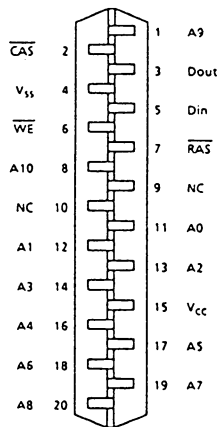
Pin Arrangement

- HM514101AJ Series
HM514101AS Series

- HM514101AZ Series



(Top View)



(Bottom View)

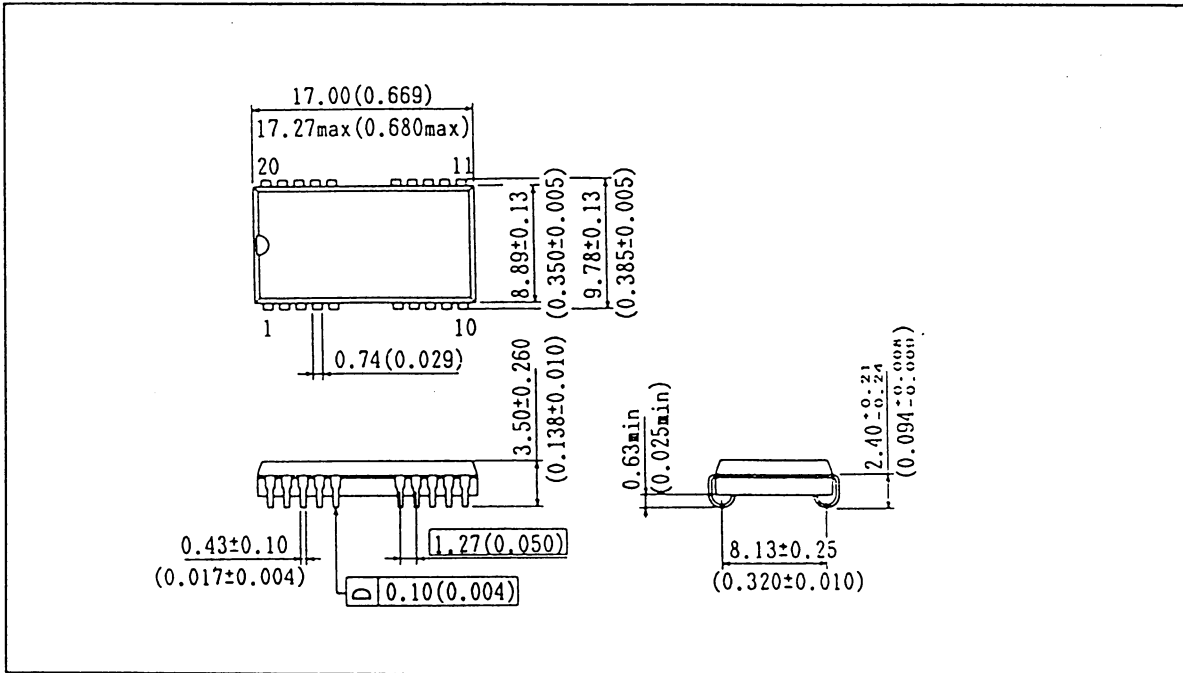
Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
Din	Data-in
Dout	Data-out
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Read / Write Enable
VCC	Power (+5V)
VSS	Ground

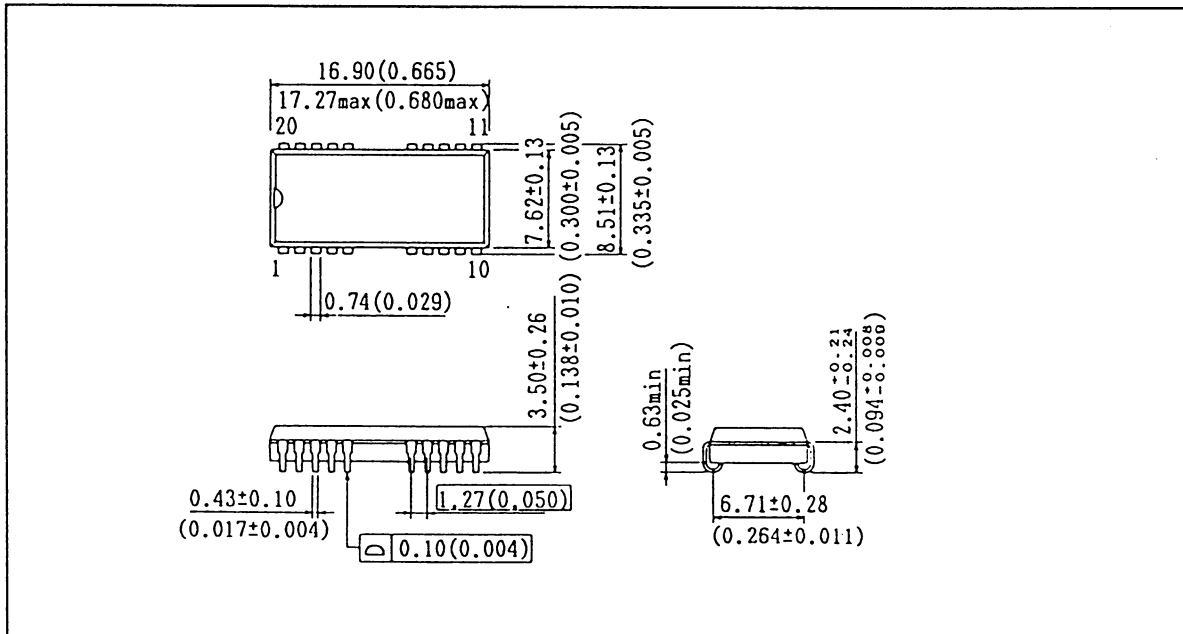
Outline Dimensions

Unit: mm (inch)

- HM514101AJ Series (CP-20DA)



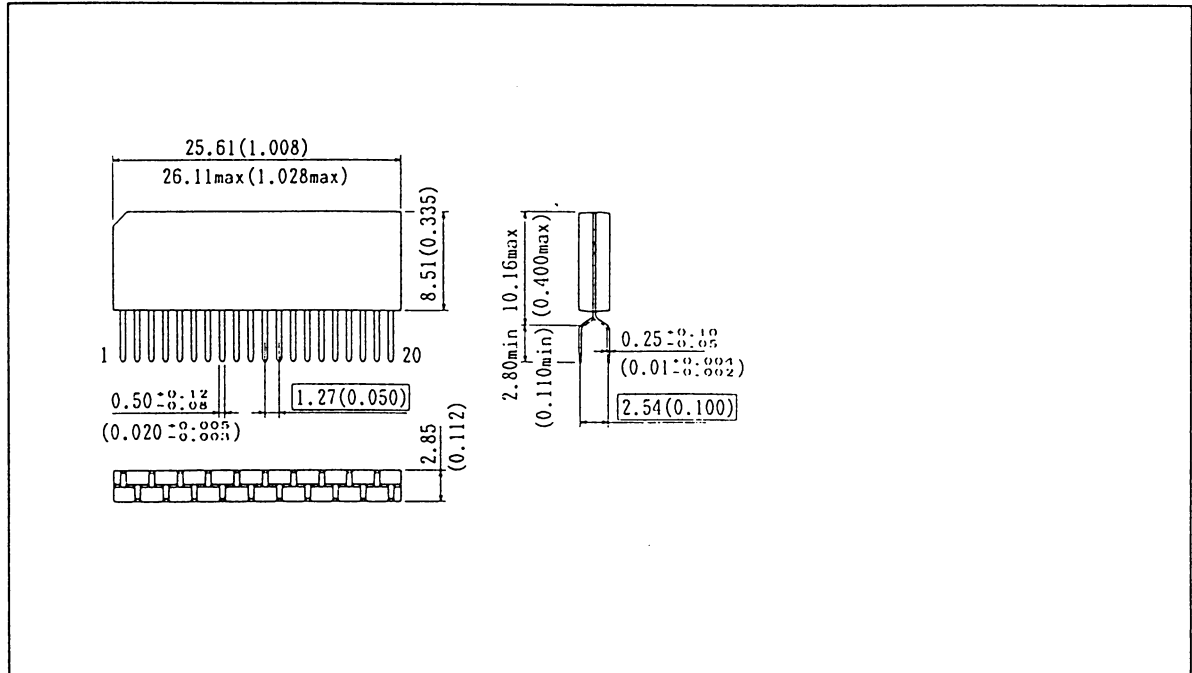
- HM514101AS Series (CP-20D)



Outline Dimensions (Continued)

Unit: mm (inch)

- HM514101AZ Series (ZP-20)



HM514100ASLJ/ASLS/ASLZ-7/8/10

(Super Low Power Version)

4,194,304-Word × 1-Bit Dynamic Random Access Memory

Description

The Hitachi HM514100A is a CMOS dynamic RAM organized 4,194,304 word x 1 bit. HM514100A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100A to be packaged in standard 350-mil 20-pin plastic SOJ, standard 300-mil 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
70 ns/80 ns/100 ns (max)
- * Low power dissipation
 - Active mode
550 mW/495 mW/440 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function
- * Data Retention Operation

Ordering Informations

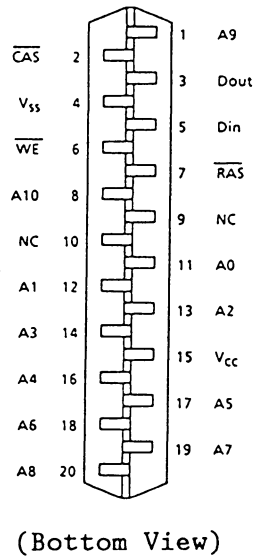
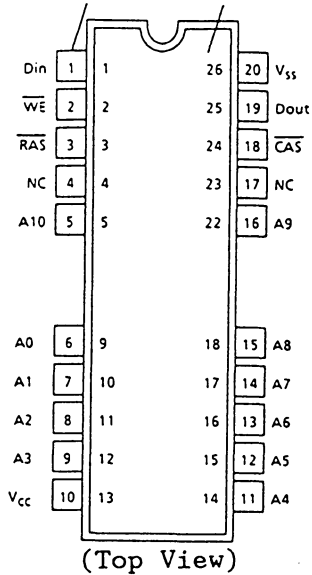
Type No.	Access Time	Package
HM514100ASLJ-7	70 ns	350-mil 20-pin
HM514100ASLJ-8	80 ns	plastic SOJ
HM514100ASLJ-10	100 ns	(CP-20DA)
HM514100ASLS-7	70 ns	300-mil 20-pin
HM514100ASLS-8	80 ns	plastic SOJ
HM514100ASLS-10	100 ns	(CP-20D)
HM514100ASLZ-7	70 ns	400-mil 20-pin
HM514100ASLZ-8	80 ns	plastic ZIP
HM514100ASLZ-10	100 ns	(ZP-20)

Pin Out

- HM514100ASLJ Series
- HM514100ASLS Series

- HM514100ASLZ Series

Hitachi Pin No. JEDEC Pin No.



Pin Description

Pin Name	Function
A0 - A10	Address Input
A0 - A9	Refresh Address Input
Din	Data-in
Dout	Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
VCC	Power (+5V)
VSS	Ground
NC	No Connection

* DC Electrical Characteristics (Ta = 0 to +60 °C , VCC = 5 V ± 10 % , VSS = 0 V)

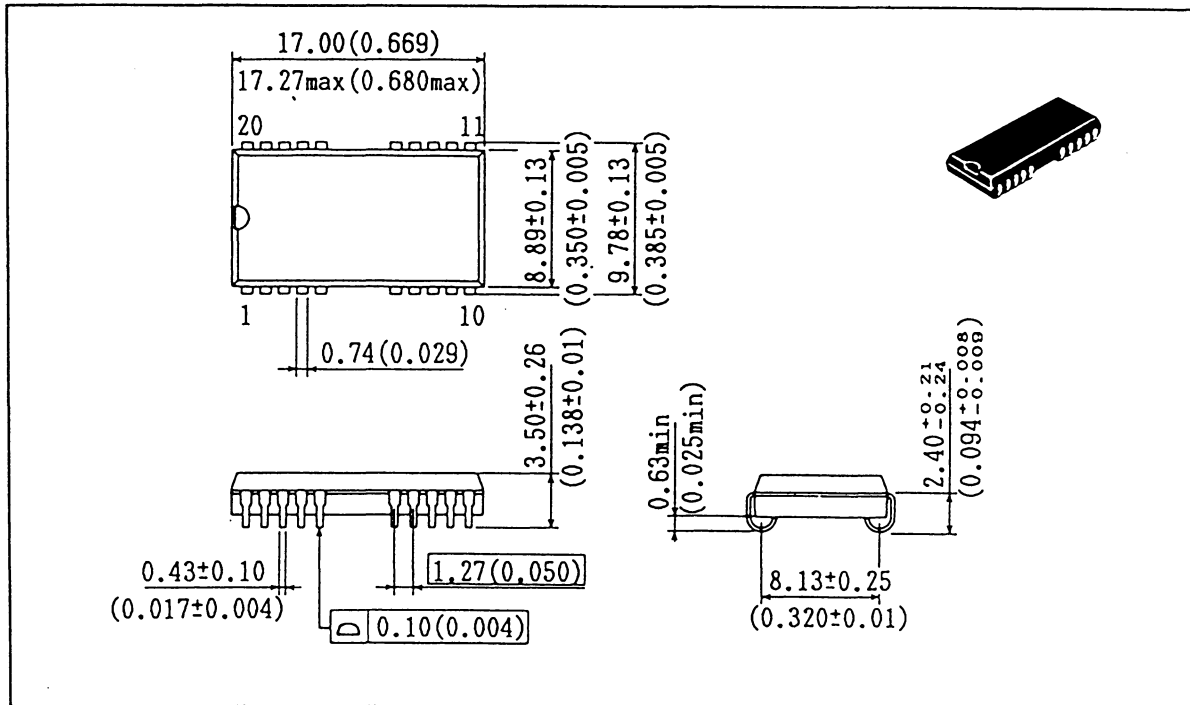
Parameter	Symbol	HM514100A -7		HM514100A -8		HM514100A -10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating current	ICC1	-	100	-	90	-	80	mA	RAS, CAS cycling tRC = min	1,2
Standby current	ICC2	-	2	-	2	-	2	mA	TTL interface RAS, CAS = VIH Dout = High-Z	
		-	100	-	100	-	100	µA	CMOS interface RAS, CAS = VIH WE, Address and Din = VIH or VIL Dout = High-Z	4
RAS-only refresh current	ICC3	-	100	-	90	-	80	mA	tRC = min	2
Standby current	ICC5	-	5	-	5	-	5	mA	RAS = VIH CAS = VIL Dout = enable	1
CAS-before-RAS refresh current	ICC6	-	100	-	90	-	80	mA	tRC = min	
Fast page mode current	ICC7	-	100	-	90	-	80	mA	tpc = min	1,3
Data Retention current (Equivalent Refresh Time is 256 ms)	ICC10	-	150	-	150	-	150	µA	tRC = 250 µs tRAS < 200 ns WE = VIH, CAS = VIL Address and Din = VIH or VIL Dout = High-Z 4.0 V ≤ VCC ≤ 5.5 V	4
Input leakage current	ILI	-10	10	-10	10	-10	10	µA	0 V ≤ VIN ≤ 7 V	
Output leakage current	ILO	-10	10	-10	10	-10	10	µA	0 V ≤ VOUT ≤ 7 V DOUT = disable	
Output high voltage	VOH	2.4	VCC	2.4	VCC	2.4	VCC	V	High IOUT = -5 mA	
Output low voltage	VOL	0	0.4	0	0.4	0	0.4	V	Low IOUT = 4.2 mA	

- Note:
1. ICC depends on output load condition when the device is selected, ICC max is specified at the output open condition.
 2. Address can be changed once or less while RAS = VIL.
 3. Address can be changed once or less while CAS = VIH.
 4. VCC - 0.2 V ≤ VIH ≤ 6.5 V and 0 V ≤ VIL ≤ 0.2 V

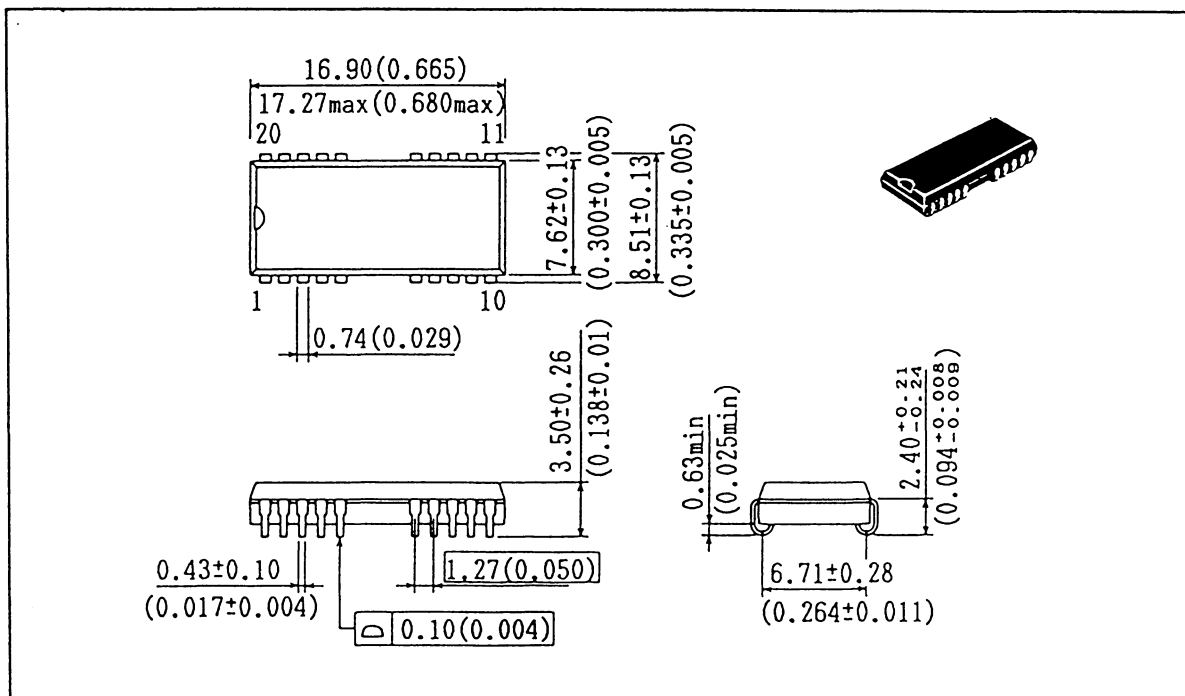
Outline Dimensions

Unit: mm(inch)

- HM514100ASLJ Series (CP-20DA)



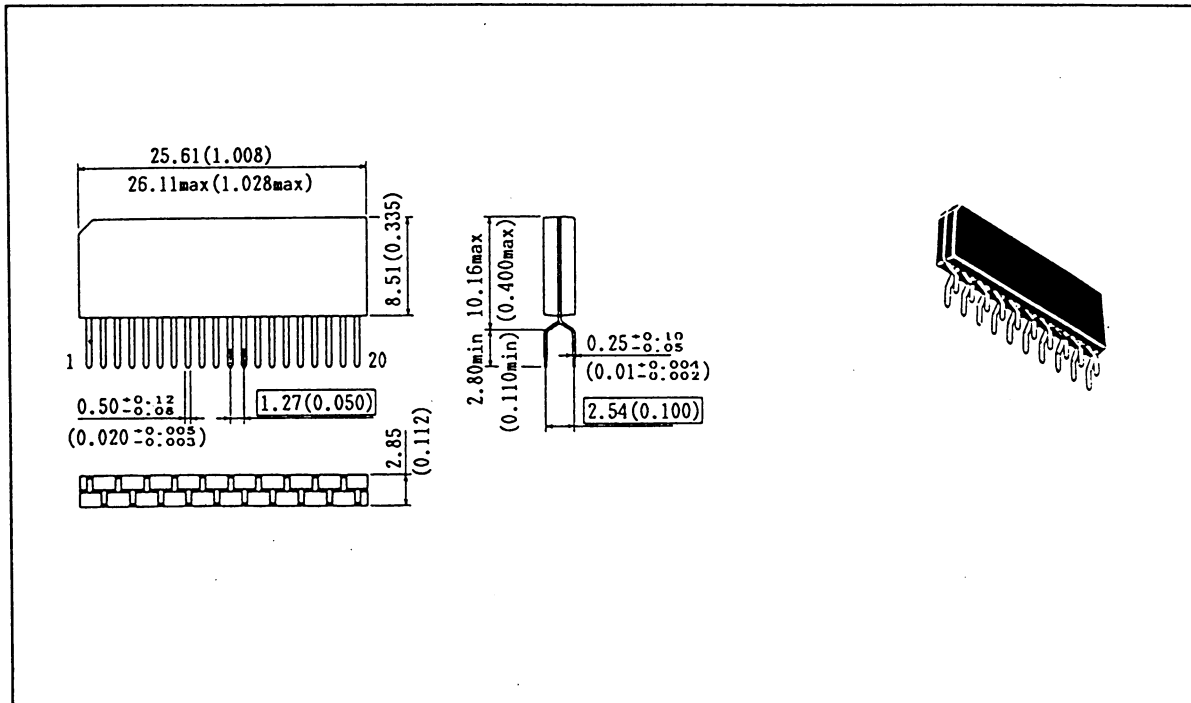
- HM514100ASLS Series (CP-20D)



Outline Dimensions (Continued)

Unit: mm(inch)

- HM514100ASLZ Series (ZP-20)



HM514400ASLJ/ASLS/ASLZ-7/8/10

(Super Low Power Version)

1,048,576-Word × 4-Bit Dynamic Random Access Memory

Description

The Hitachi HM514400A is a CMOS dynamic RAM organized 1,048,576 word x 4 bit. HM514400A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400A to be packaged in standard 350-mil 20-pin plastic SOJ, standard 300-mil 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
 - 70 ns/80 ns/100 ns (max)
- * Low power dissipation
 - Active mode
 - 550 mW/495 mW/440 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function
- * Data Retention Operation

Ordering Informations

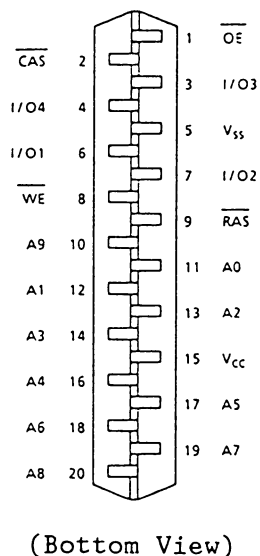
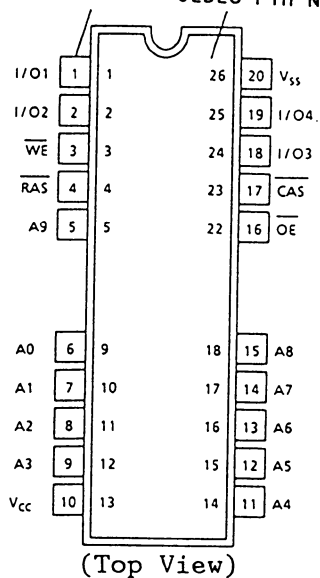
Type No.	Access Time	Package
HM514400ASLJ-7	70 ns	350-mil 20-pin
HM514400ASLJ-8	80 ns	plastic SOJ
HM514400ASLJ-10	100 ns	(CP-20DA)
HM514400ASLS-7	70 ns	300-mil 20-pin
HM514400ASLS-8	80 ns	plastic SOJ
HM514400ASLS-10	100 ns	(CP-20D)
HM514400ASLZ-7	70 ns	400-mil 20-pin
HM514400ASLZ-8	80 ns	plastic ZIP
HM514400ASLZ-10	100 ns	(ZP-20)

Pin Out

- HM514400ASLJ Series
HM514400ASLS Series

- HM514400ASLZ Series

Hitachi Pin No. JEDEC Pin No.



Pin Description

Pin Name	Function
A0 - A9	Address Input
A0 - A9	Refresh Address Input
I/O1 - I/O4	Data-in / Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
OE	Output Enable
VCC	Power (+5V)
VSS	Ground

* DC Electrical Characteristics (Ta = 0 to +60 °C , VCC = 5 V ± 10 % , VSS = 0 V)

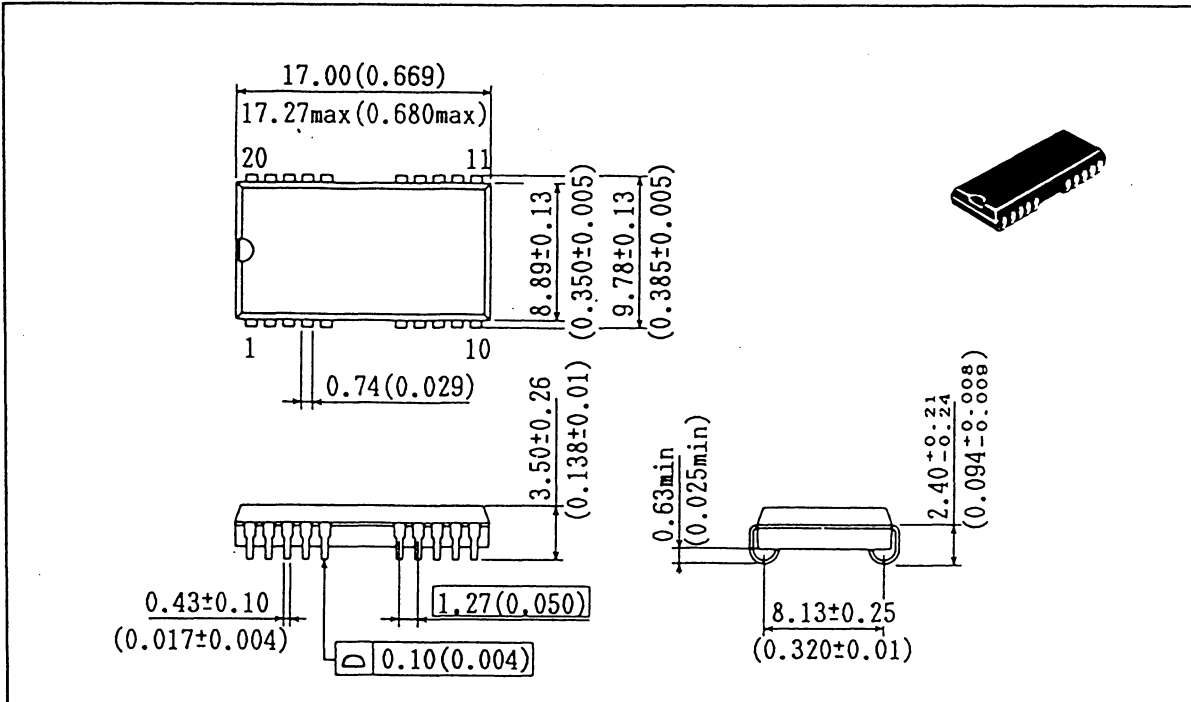
Parameter	Symbol	HM514400A -7		HM514400A -8		HM514400A -10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating current	ICC1	-	100	-	90	-	80	mA	RAS, CAS cycling tRC = min	1,2
Standby current	ICC2	-	2	-	2	-	2	mA	TTL interface RAS, CAS = VIH Dout = High-Z	
		-	100	-	100	-	100	µA	CMOS interface RAS, CAS = VIH WE, OE, Address and Din = VIH or VIL Dout = High-Z	4
RAS-only refresh current	ICC3	-	100	-	90	-	80	mA	tRC = min	2
Standby current	ICC5	-	5	-	5	-	5	mA	RAS = VIH CAS = VIL Dout = enable	1
CAS-before-RAS refresh current	ICC6	-	100	-	90	-	80	mA	tRC = min	
Fast page mode current	ICC7	-	100	-	90	-	80	mA	tPC = min	1,3
Data Retention current (Equivalent Refresh Time is 256 ms)	ICC10	-	150	-	150	-	150	µA	tRC = 250 µs tRAS ≤ 200 ns WE = VIH, CAS = VIL OE, Address and Din = VIH or VIL Dout = High-Z 4.0 V ≤ VCC ≤ 5.5 V	4
Input leakage current	ILI	-10	10	-10	10	-10	10	µA	0 V ≤ VIN ≤ 7 V	
Output leakage current	ILO	-10	10	-10	10	-10	10	µA	0 V ≤ VOUT ≤ 7 V DOUT = disable	
Output high voltage	VOH	2.4	VCC	2.4	VCC	2.4	VCC	V	High IOUT = -5 mA	
Output low voltage	VOL	0	0.4	0	0.4	0	0.4	V	Low IOUT = 4.2 mA	

- Note: 1. ICC depends on output load condition when the device is selected, ICC max is specified at the output open condition.
 2. Address can be changed once or less while RAS = VIL.
 3. Address can be changed once or less while CAS = VIH.
 4. VCC-0.2 V ≤ VIH ≤ 6.5 V and 0 V ≤ VIL ≤ 0.2 V

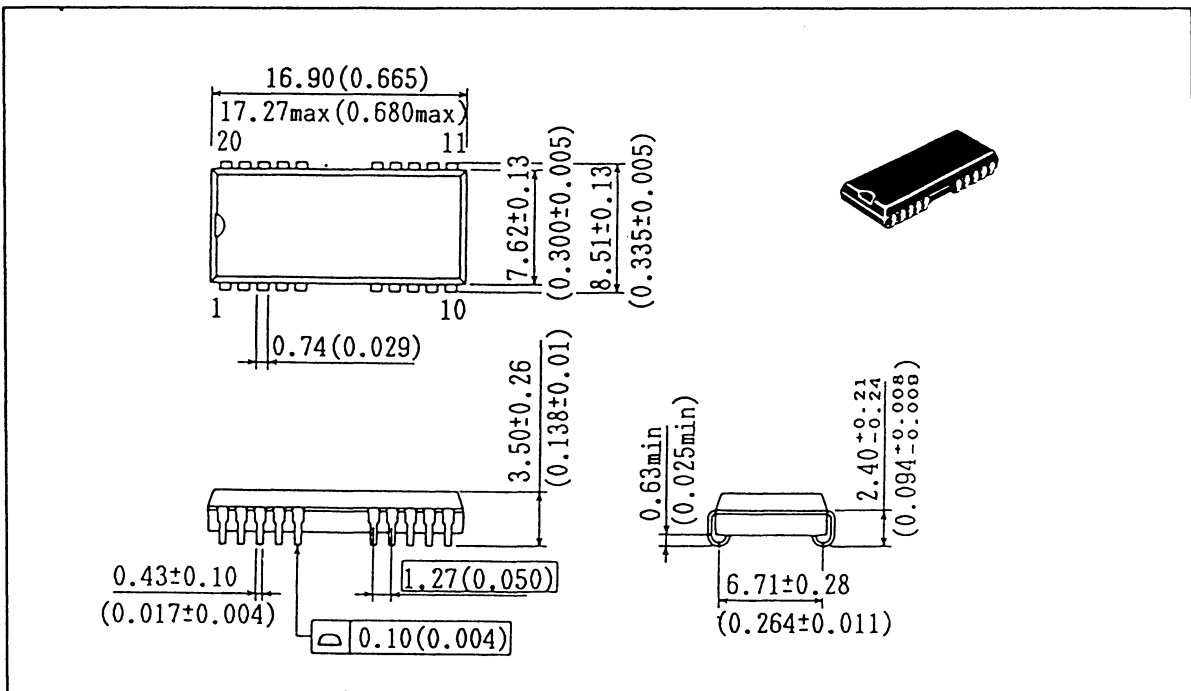
Outline Dimensions

Unit: mm(inch)

- HM514400ASLJ Series (CP-20DA)



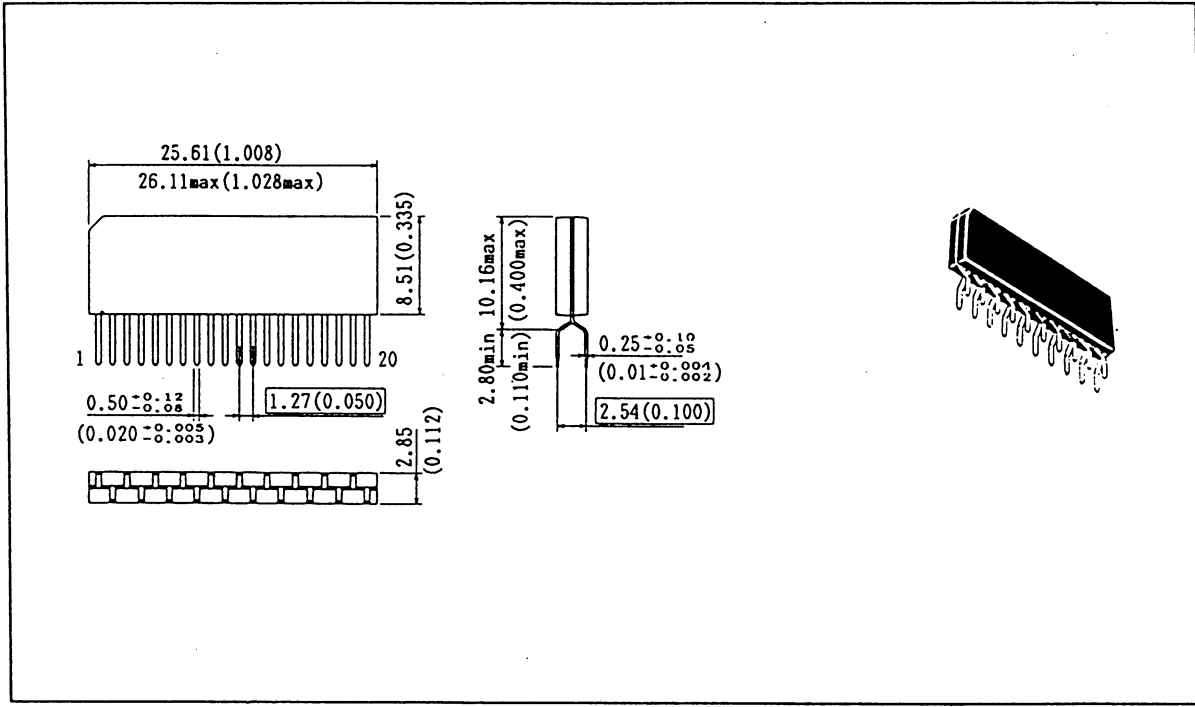
- HM514400ASLS Series (CP-20D)



Outline Dimensions (Continued)

Unit: mm(inch)

- HM514400ASLZ Series (ZP-20)



NEW PRODUCT

Rev. 5
Dec. 29, 1989

HM514400JP/ZP-8/10/12

1,048,576-Word × 4-Bit Dynamic Random Access Memory

Description

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576 word x 4 bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

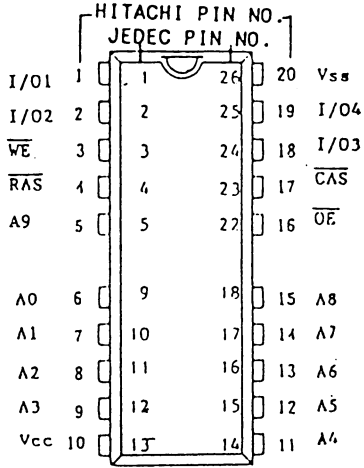
- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- * Test function

Ordering Informations

Part No.	Access	Package
HM514400JP-8	80 ns	350 mil 20-pin plastic SOJ
HM514400JP-10	100 ns	
HM514400JP-12	120 ns	
HM514400ZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514400ZP-10	100 ns	
HM514400ZP-12	120 ns	

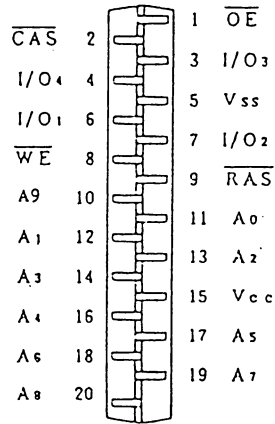
Pin Out

• HM514400JP Series



(Top View)

• HM514400ZP Series



(Bottom View)

Pin Description

Pin Name	Function
A0 - A9	Address Input
A0 - A9	Refresh Address Input
I/O1 - I/O4	Data-in / Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
OE	Output Enable
VCC	Power (+5V)
VSS	Ground

Rev. 1
Dec. 29, 1989

HM514400JP/ZP-8H

1,048,576-Word × 4-Bit Dynamic Random Access Memory

Description

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576 word x 4 bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

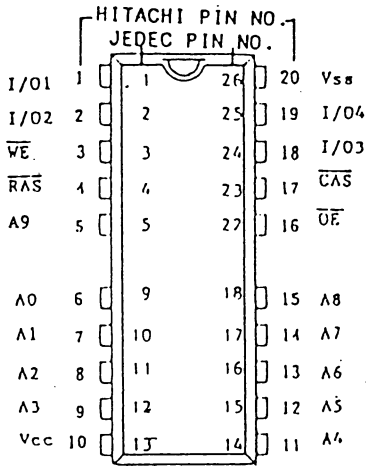
- * Single 5 V ($\pm 10\%$)
- * High speed
 - Access time
 - 80 ns (max)
- * Low power dissipation
 - Active mode
 - 495 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- * Test function

Ordering Informations

Part No.	Access	Package
HM514400JP-8H	80 ns	350 mil 20-pin plastic SOJ
HM514400ZP-8H	80 ns	400 mil 20-pin plastic ZIP

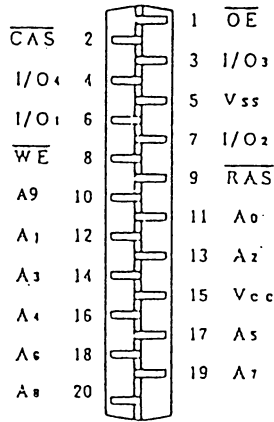
Pin Out

• HM514400JP Series



(Top View)

• HM514400ZP Series



(Bottom View)

Pin Description

Pin Name	Function
A0 - A9	Address Input
A0 - A9	Refresh Address Input
I/O1 - I/O4	Data-in / Data-out
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Read / Write Enable
\overline{OE}	Output Enable
VCC	Power (+5V)
VSS	Ground

NEW PRODUCT

Rev. 3
Feb. 23, 1990

HM514400LJP/LZP-8/10/12

(Low Power Version)

1,048,576-Word × 4-Bit Dynamic Random Access Memory

Description

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576 word x 4 bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (128 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function
- * Battery back up operation

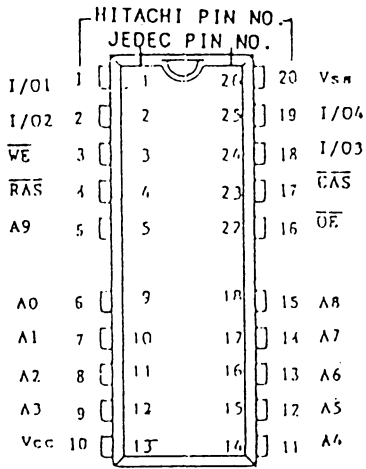
Ordering Informations

Part No.	Access	Package
HM514400LJP-8	80 ns	350 mil 20-pin plastic SOJ
HM514400LJP-10	100 ns	
HM514400LJP-12	120 ns	
HM514400LZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514400LZP-10	100 ns	
HM514400LZP-12	120 ns	

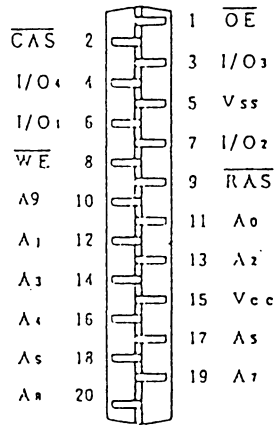
Pin Out

• HM514400LJP Series

• HM514400LZP Series



(Top View)



(Bottom View)

Pin Description

Pin Name	Function
A0 - A9	Address Input
A0 - A9	Refresh Address Input
I/O1 - I/O4	Data-in / Data-out
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Read / Write Enable
\overline{OE}	Output Enable
VCC	Power (+5V)
VSS	Ground

* DC Electrical Characteristics (Ta = 0 to +70 °C, VCC = 5 V ± 10 %, VSS = 0 V)

Parameter	Symbol	HM514400L		HM514400L		HM514400L		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating current	ICC1	-	90	-	80	-	70	mA	RAS, CAS cycling tRC = min	1,2
Standby current	ICC2	-	2	-	2	-	2	mA	TTL interface RAS, CAS = VIH Dout = High-Z	
		-	200	-	200	-	200	µA	CMOS interface RAS, CAS and WE > VCC-0.2V or < 6.5V Address and Din: stable Dout = High-Z	
RAS-only refresh current	ICC3	-	90	-	80	-	70	mA	tRC = min	2
Standby current	ICC5	-	5	-	5	-	5	mA	RAS = VIH CAS = VIL Dout = enable	1,4
CAS-before-RAS refresh current	ICC6	-	90	-	80	-	70	mA	tRC = min	
Fast page mode current	ICC7	-	90	-	80	-	70	mA	tpc = min	1,3
Battery back up operating current (standby with CBR refresh)	ICC10	-	300	-	300	-	300	µA	tRC = 125 µs tRAS ≤ 1 µs VCC-0.2V ≤ VIH ≤ 6.5V 0V ≤ VIL ≤ 0.2V WE and OE = VIH Address and Din: stable Dout = High-Z	
Input leakage current	ILI	-10	10	-10	10	-10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	ILO	-10	10	-10	10	-10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	VOH	2.4	VCC	2.4	VCC	2.4	VCC	V	High Iout = -5 mA	
Output low voltage	VOL	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Note: 1. ICC depends on output load condition when the device is selected, ICC max is specified at the output open condition.
 2. Address can be changed once or less while RAS = VIL.
 3. Address can be changed once or less while CAS = VIH.
 4. Clock voltages (RAS and CAS) must be applied simultaneously with or prior to applying supply voltage.

—

NEW PRODUCT

Rev. 5
Dec. 29, 1989

HM514402JP/ZP-8/10/12

1,048,576-Word × 4-Bit Dynamic Random Access Memory

Description

The Hitachi HM514402 is a CMOS dynamic RAM organized 1,048,576 word x 4 bit. HM514402 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514402 offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM514402 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

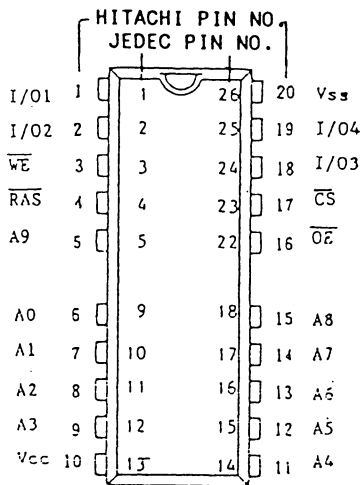
- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Static column mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function

Ordering Informations

Part No.	Access	Package
HM514402JP-8	80 ns	350 mil 20-pin plastic SOJ
HM514402JP-10	100 ns	
HM514402JP-12	120 ns	
HM514402ZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514402ZP-10	100 ns	
HM514402ZP-12	120 ns	

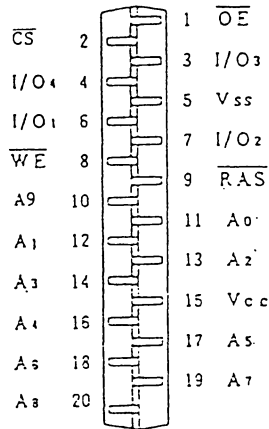
Pin Out

• HM514402JP Series



(Top View)

• HM514402ZP Series



(Bottom View)

Pin Description

Pin Name	Function
A0 - A9	Address Input
A0 - A9	Refresh Address Input
I/O1 - I/O4	Data-in / Data-out
RAS	Row Address Strobe
CS	Chip Select
WE	Read / Write Enable
OE	Output Enable
VCC	Power (+5V)
VSS	Ground

NEW PRODUCT

Rev. 1
Dec. 29, 1989

HM514410JP/ZP-8/10/12

1,048,576-Word × 4-Bit Dynamic Random Access Memory

Description

The Hitachi HM514410 is a CMOS dynamic RAM organized 1,048,576 word x 4 bit. HM514410 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514410 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514410 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
80 ns / 100 ns / 120 ns (max)
- * Low power dissipation
 - Active mode
495 mW / 440 mW / 385 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- * Test function
- * Write per bit capability

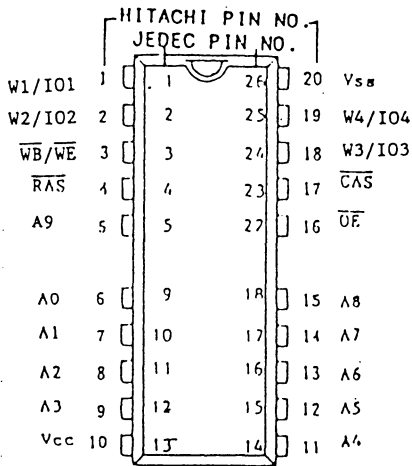
Ordering Informations

Part No.	Access	Package
HM514410JP-8	80 ns	350 mil 20-pin plastic SOJ
HM514410JP-10	100 ns	
HM514410JP-12	120 ns	
HM514410ZP-8	80 ns	400 mil 20-pin plastic ZIP
HM514410ZP-10	100 ns	
HM514410ZP-12	120 ns	

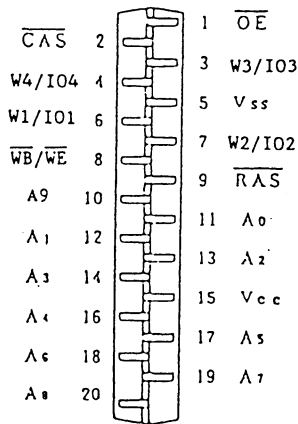
Pin Out

• HM514410JP Series

• HM514410ZP Series



(Top View)



(Bottom View)

Pin Description

Pin Name	Function
A0 - A9	Address Input
A0 - A9	Refresh Address Input
W1/I01 - W4/I04	Write Select / Data-in / Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WB/WE	Write Per Bit / Write Enable
OE	Output Enable
VCC	Power (+5V)
VSS	Ground

Rev. 1
Jan. 12, 1990

HM514400AJ/AS/AZ-7/8/10

1,048,576-Word × 4-Bit Dynamic Random Access Memory

Description

The Hitachi HM514400A is a CMOS dynamic RAM organized 1,048,576 word x 4 bit. HM514400A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400A to be packaged in standard 350-mil 20-pin plastic SOJ, standard 300-mil 20-pin plastic SOJ and 20-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
70 ns/80 ns/100 ns (max)
- * Low power dissipation
 - Active mode
550 mW/495 mW/440 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- * Test function

Ordering Informations

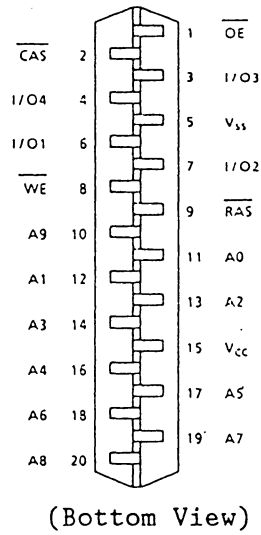
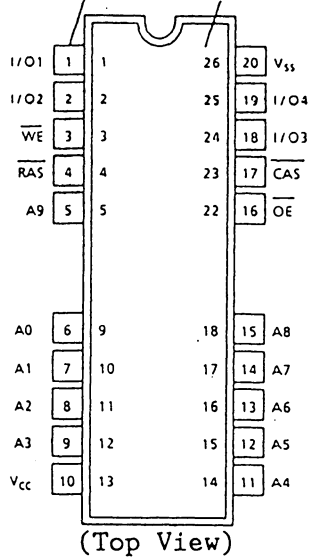
Type No.	Access Time	Package
HM514400AJ-7	70 ns	350-mil 20-pin
HM514400AJ-8	80 ns	plastic SOJ
HM514400AJ-10	100 ns	(CP-20DA)
HM514400AS-7	70 ns	300-mil 20-pin
HM514400AS-8	80 ns	plastic SOJ
HM514400AS-10	100 ns	(CP-20D)
HM514400AZ-7	70 ns	400-mil 20-pin
HM514400AZ-8	80 ns	plastic ZIP
HM514400AZ-10	100 ns	(ZP-20)

Pin Out

- HM514400AJ Series
HM514400AS Series

- HM514400AZ Series

Hitachi Pin No. JEDEC Pin No.



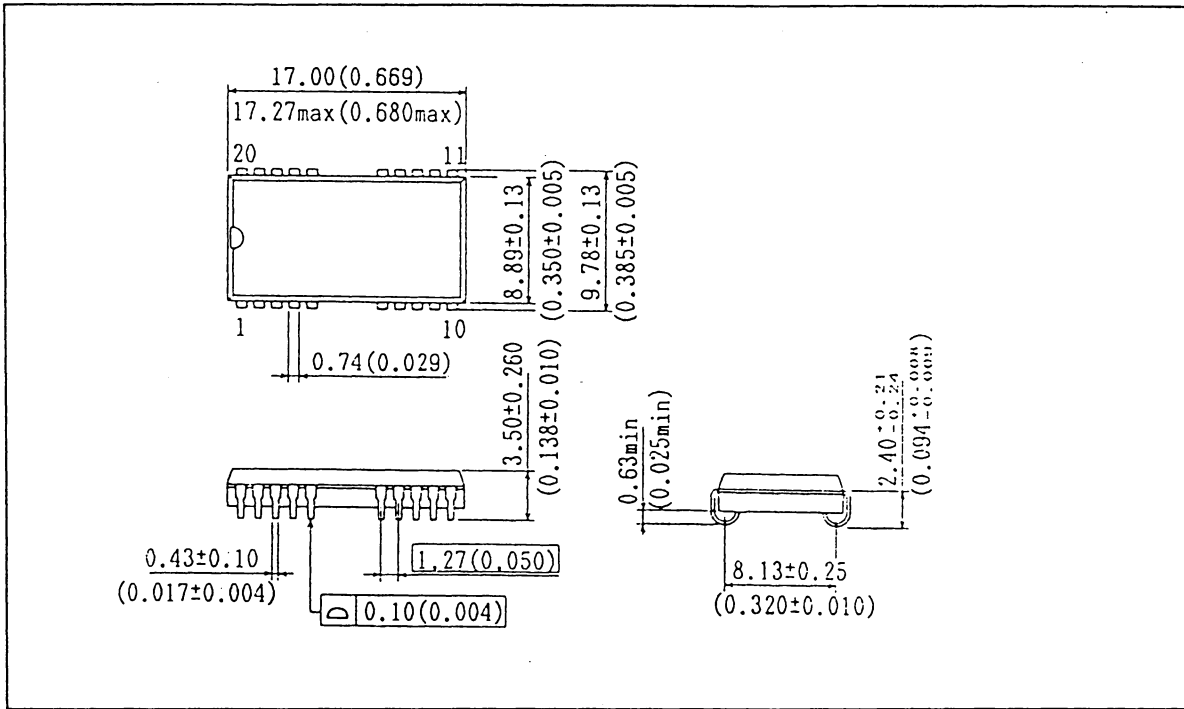
Pin Description

Pin Name	Function
A0 - A9	Address Input
A0 - A9	Refresh Address Input
I/O1 - I/O4	Data-in / Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
OE	Output Enable
VCC	Power (+5V)
VSS	Ground

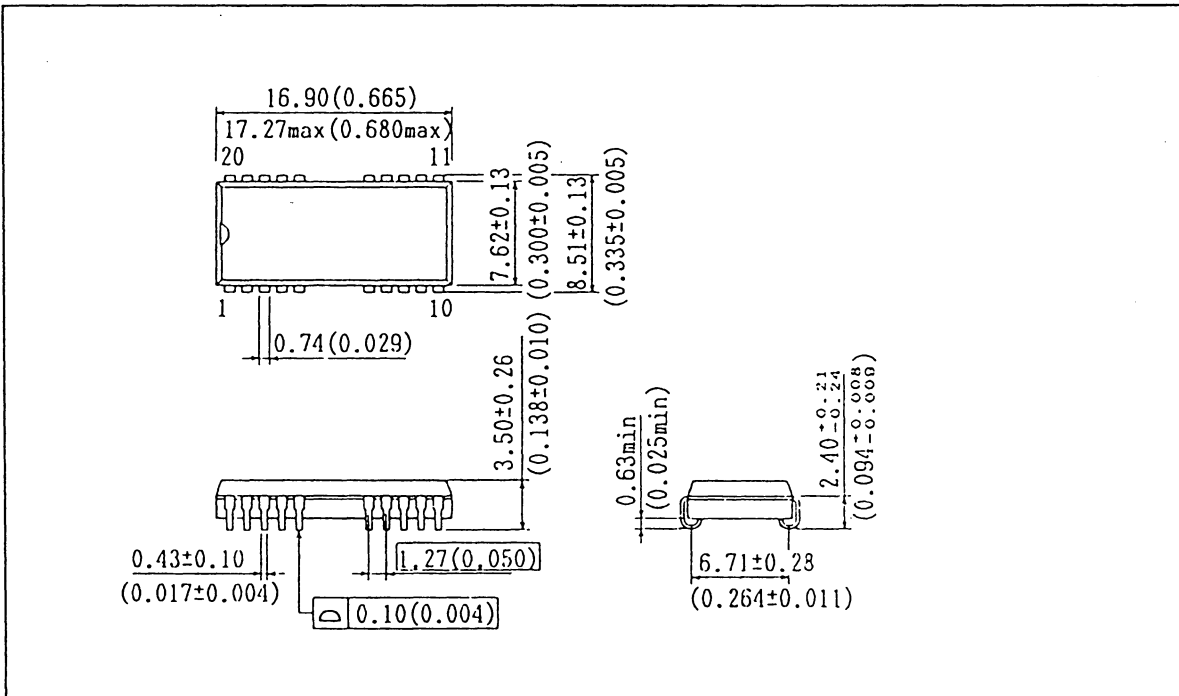
Outline Dimensions

Unit: mm(inch)

- HM514400AJ Series (CP-20DA)



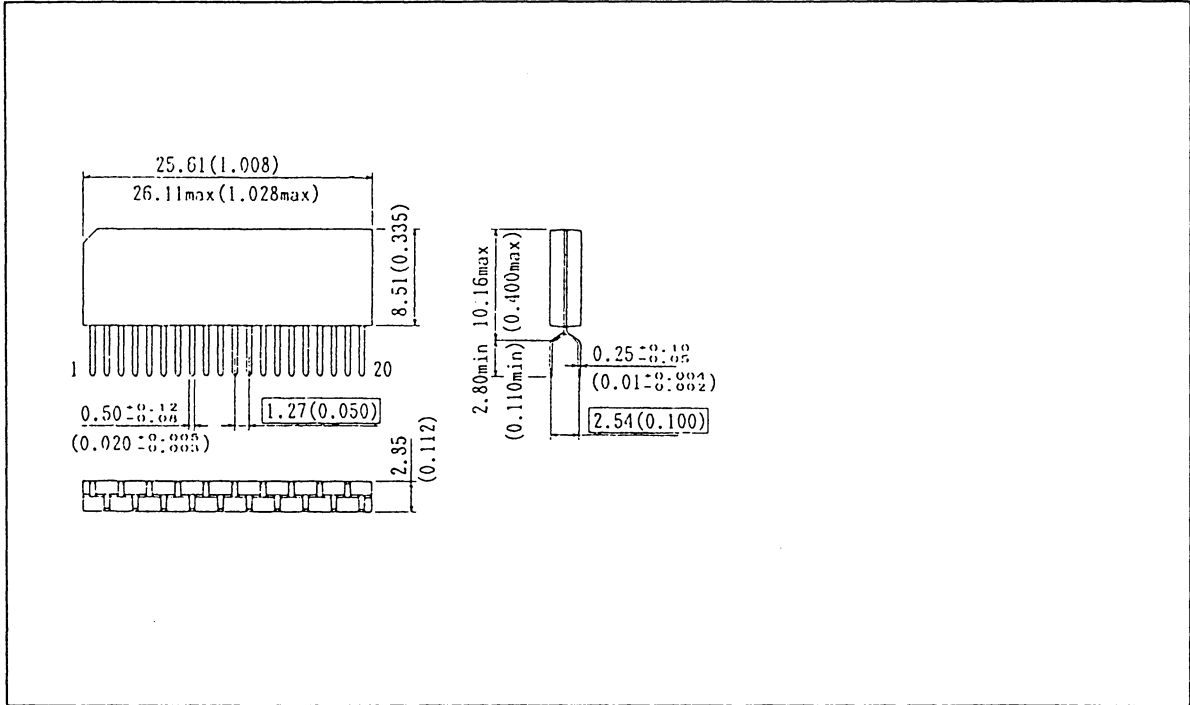
- HM514400AS Series (CP-20D)



Outline Dimensions (Continued)

Unit: mm(inch)

- HM514400AZ Series (ZP-20)



NEW PRODUCT

Rev. 4
Mar. 16, 1990

HM514800JP/ZP-7/8/10

524,288-Word × 8-Bit Dynamic Random Access Memory

The Hitachi HM514800 are CMOS dynamic RAM organized as 524,288-word x 8-bit. HM514800 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514800 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514800 to be packaged in standard 400-mil 28-pin plastic SOJ, standard 400-mil 28-pin plastic ZIP.

Features

- * Single 5 V (±10%)
- * High speed
 - Access time
70 ns/80 ns/100 ns (max)
- * Low power dissipation
 - Active mode
605 mW/550 mW/495 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh

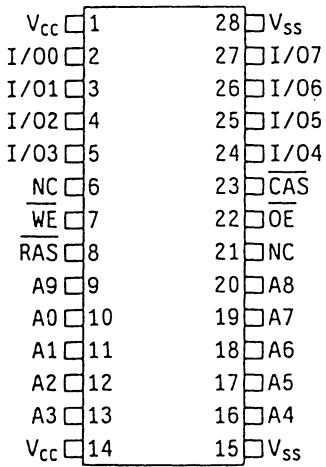
Ordering Informations

Type No.	Access Time	Package
HM514800JP-7	70 ns	400-mil 28-pin
HM514800JP-8	80 ns	plastic SOJ
HM514800JP-10	100 ns	(CP-28D)
HM514800ZP-7	70 ns	400-mil 28-pin
HM514800ZP-8	80 ns	plastic ZIP
HM514800ZP-10	100 ns	(ZP-28)

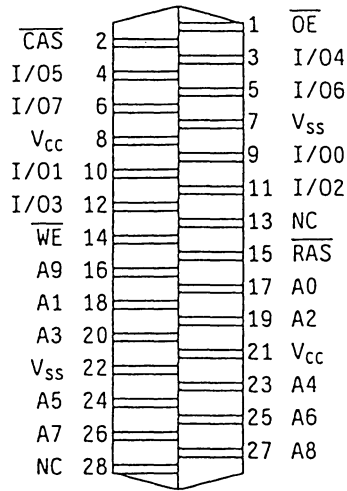
Pin Arrangement

• HM514800JP Series

• HM514800ZP Series



(Top View)



(Bottom View)

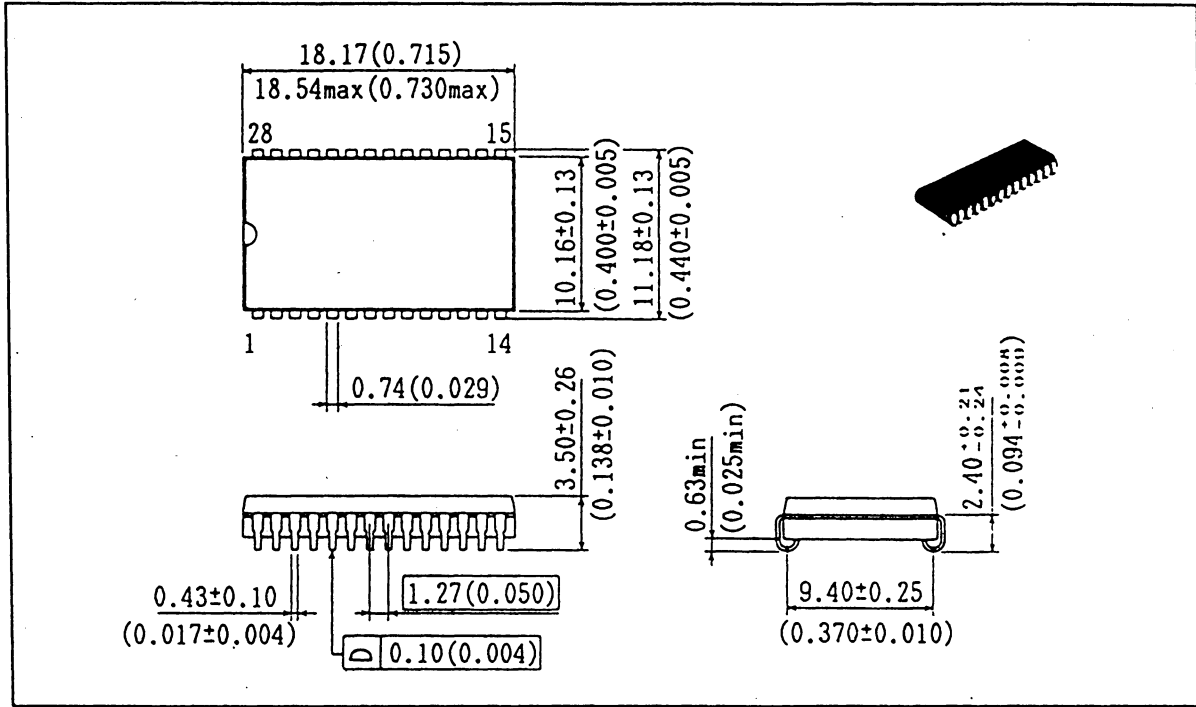
Pin Description

Pin Name	Function
A0-A9	Address input
	Refresh address input
I/O0-I/O7	Data-in/data-out
RAS	Row address strobe
CAS	Column address strobe
WE	Read/write enable
OE	Output enable
VCC	Power (+5V)
VSS	Ground

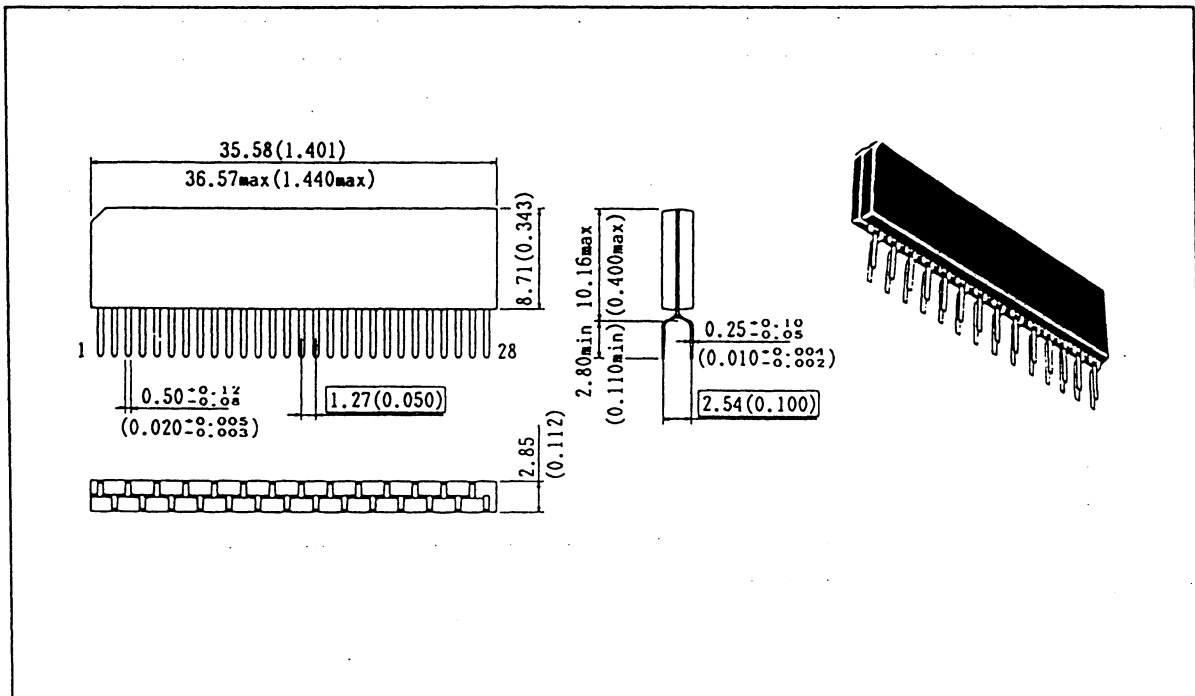
Outline Dimensions

Unit: mm(inch)

• HM514800JP Series (CP-28D)



• HM514800ZP Series (ZP-28)



NEW PRODUCT

Rev. 4
Mar. 16, 1990

HM514900JP/ZP-7/8/10

524,288-Word × 9-Bit Dynamic Random Access Memory

The Hitachi HM514900 are CMOS dynamic RAM organized as 524,288-word x 9-bit. HM514900 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514900 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514900 to be packaged in standard 400-mil 28-pin plastic SOJ, standard 400-mil 28-pin plastic ZIP.

Features

- * Single 5 V (±10%)
- * High speed
 - Access time
70 ns/80 ns/100 ns (max)
- * Low power dissipation
 - Active mode
605 mW/550 mW/495 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh

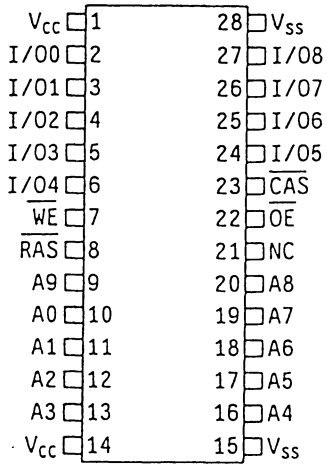
Ordering Informations

Type No.	Access Time	Package
HM514900JP-7	70 ns	400-mil 28-pin
HM514900JP-8	80 ns	plastic SOJ
HM514900JP-10	100 ns	(CP-28D)
HM514900ZP-7	70 ns	400-mil 28-pin
HM514900ZP-8	80 ns	plastic ZIP
HM514900ZP-10	100 ns	(ZP-28)

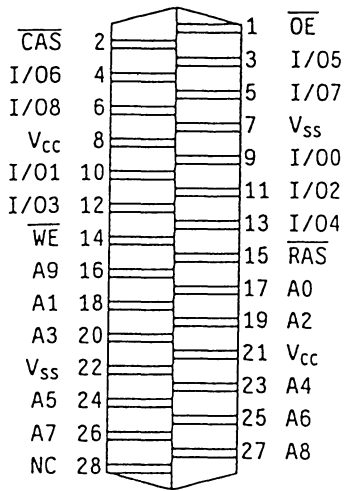
Pin Arrangement

• HM514900JP Series

• HM514900ZP Series



(Top View)



(Bottom View)

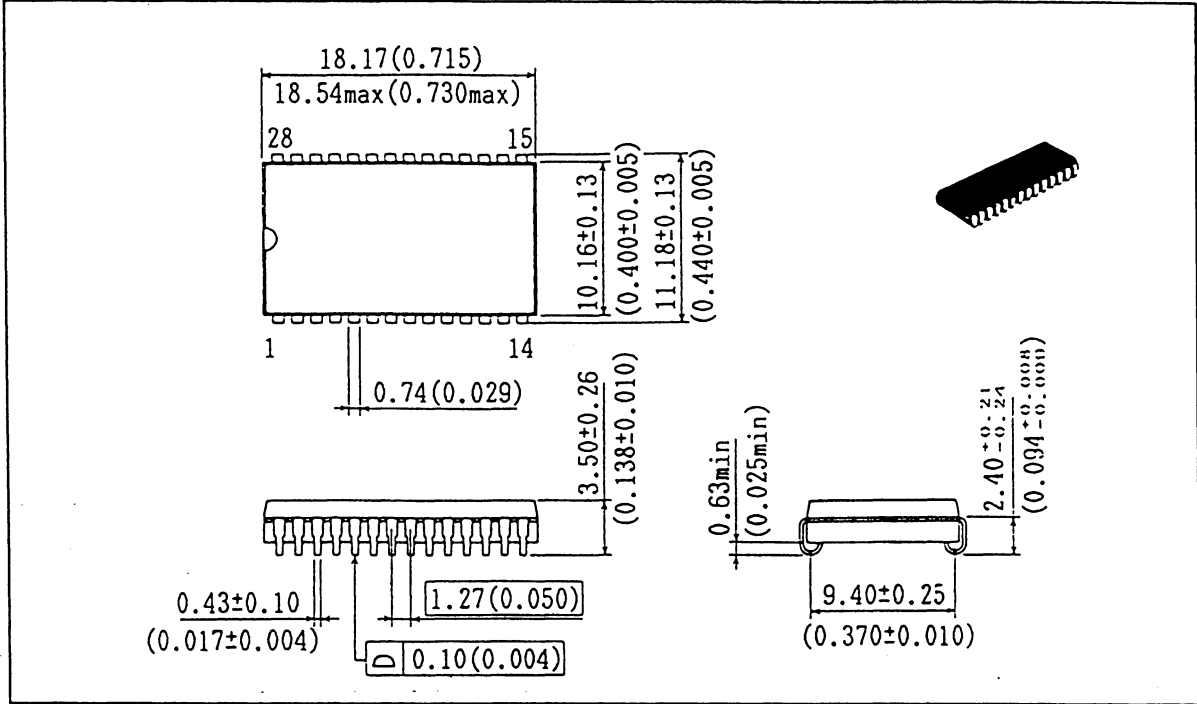
Pin Description

Pin Name	Function
A0-A9	Address input
	Refresh address input
I/00-I/08	Data-in/data-out
RAS	Row address strobe
CAS	Column address strobe
WE	Read/write enable
OE	Output enable
VCC	Power (+5V)
VSS	Ground

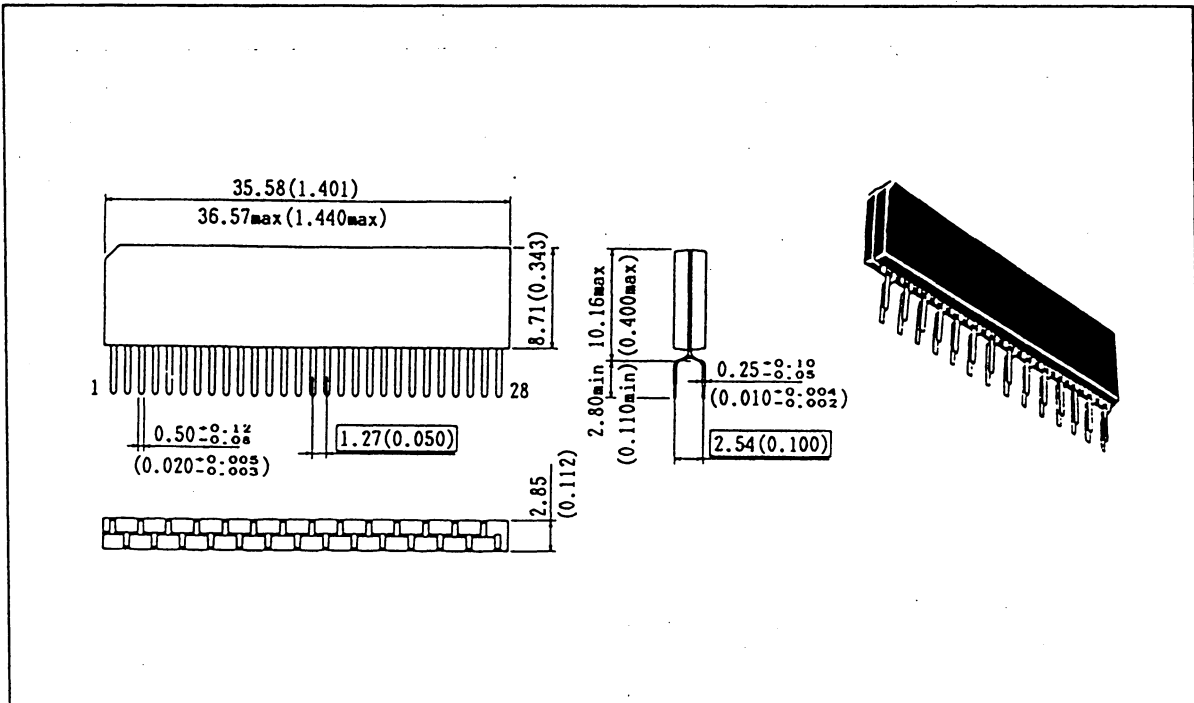
Outline Dimensions

Unit: mm(inch)

- HM514900JP Series (CP-28D)



- HM514900ZP Series (ZP-28)



NEW PRODUCT

Rev. 3
Mar. 16, 1990

HM514160JP/ZP-7/8/10

262,144-Word × 16-Bit Dynamic Random Access Memory

The Hitachi HM514160 are CMOS dynamic RAM organized as 262,144-word x 16-bit. HM514160 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514160 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514160 to be packaged in standard 400-mil 40-pin plastic SOJ, standard 400-mil 40-pin plastic ZIP.

Feature

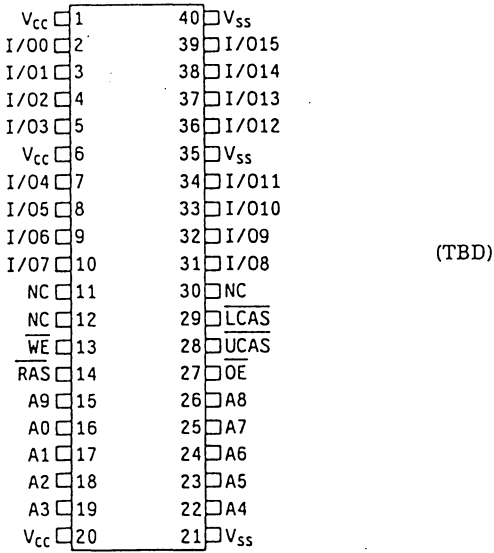
- * Single 5 V (±10%)
- * High speed
 - Access time
70 ns/80 ns/100 ns (max)
- * Low power dissipation
 - Active mode
715 mW/660 mW/605 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh

Ordering Informations

Type No.	Access Time	Package
HM514160JP-7	70 ns	400-mil 40-pin
HM514160JP-8	80 ns	plastic SOJ
HM514160JP-10	100 ns	(CP-40D)
HM514160ZP-7	70 ns	400-mil 40-pin
HM514160ZP-8	80 ns	plastic ZIP
HM514160ZP-10	100 ns	(ZP-40)

Pin Arrangement

- HM514160JP Series
- HM514160ZP Series



(Top View)

(Bottom View)

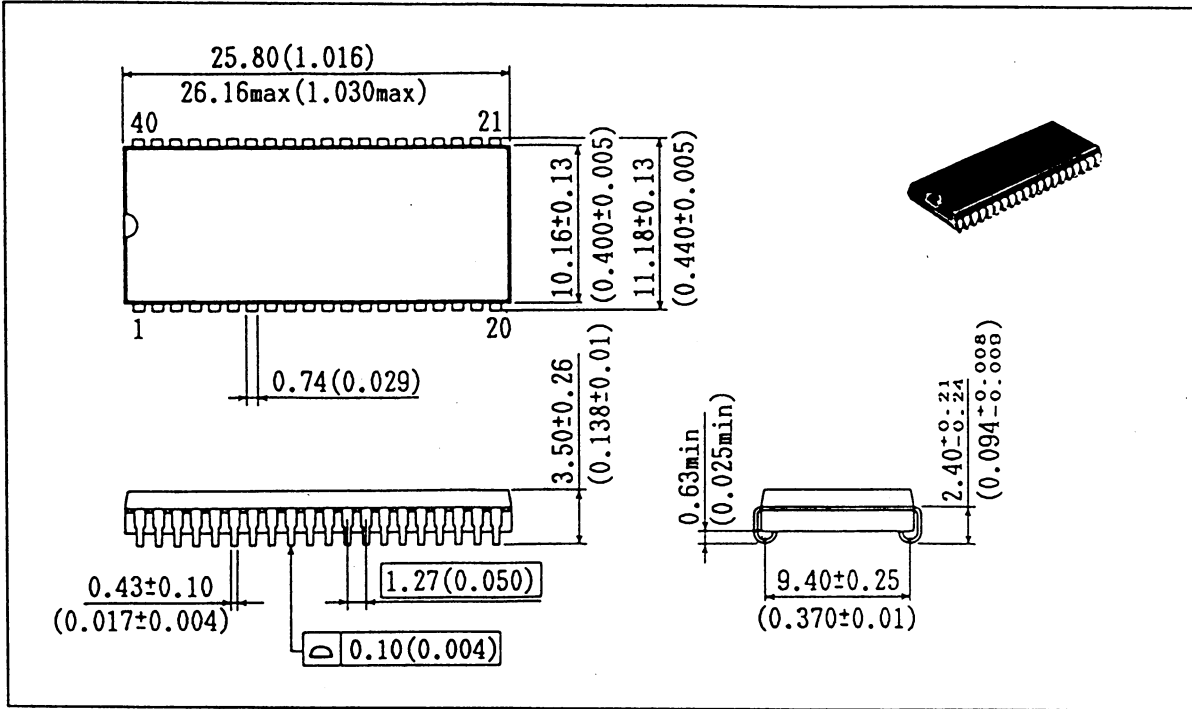
Pin Description

Pin Name	Function
A0-A9	Address input
	Refresh address input
I/O0-I/O15	Data-in/data-out
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Read/write enable
OE	Output enable
VCC	Power (+5V)
VSS	Ground

Outline Dimensions

Unit: mm(inch)

- HM514160JP Series (CP-40D)



Rev. 3
Mar. 16, 1990

HM514180JP/ZP-7/8/10

262,144-Word × 18-Bit Dynamic Random Access Memory

The Hitachi HM514180 are CMOS dynamic RAM organized as 262,144-word x 18-bit. HM514180 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514180 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514180 to be packaged in standard 400-mil 40-pin plastic SOJ, standard 400-mil 40-pin plastic ZIP.

Feature

- * Single 5 V (±10%)
- * High speed
 - Access time
70 ns/80 ns/100 ns (max)
- * Low power dissipation
 - Active mode
715 mW/660 mW/605 mW (max)
 - Standby mode 11 mW (max)
- * Fast page mode capability
- * 1,024 refresh cycles ---- (16 ms)
- * 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh

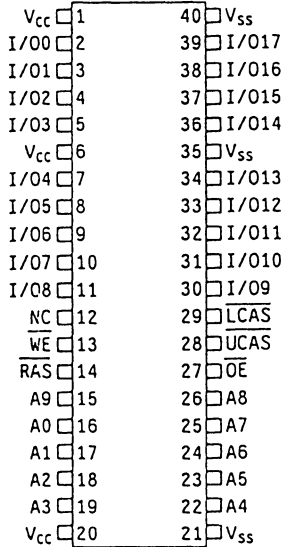
Ordering Informations

Type No.	Access Time	Package
HM514180JP-7	70 ns	400-mil 40-pin
HM514180JP-8	80 ns	plastic SOJ
HM514180JP-10	100 ns	(CP-40D)
HM514180ZP-7	70 ns	400-mil 40-pin
HM514180ZP-8	80 ns	plastic ZIP
HM514180ZP-10	100 ns	(ZP-40)

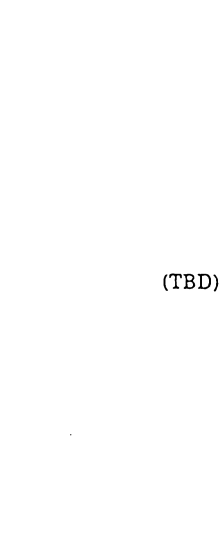
Pin Arrangement

• HM514180JP Series

• HM514180ZP Series



(Top View)



(TBD)

(Bottom View)

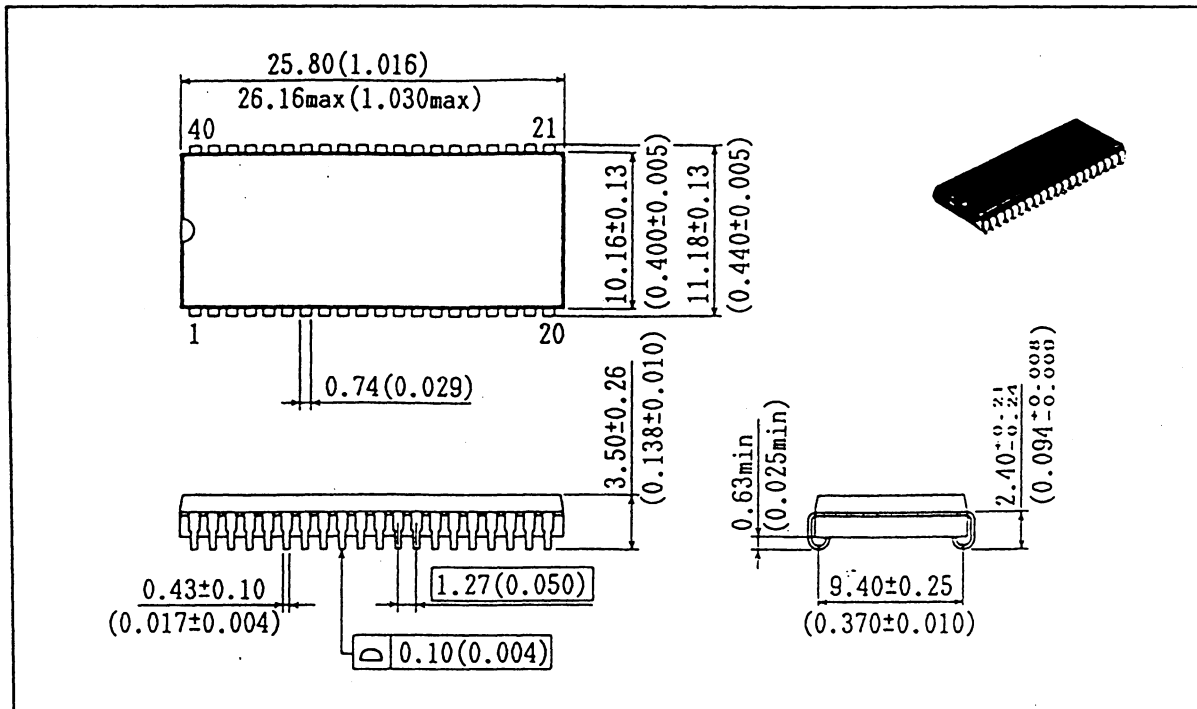
Pin Description

Pin Name	Function
A0-A9	Address input Refresh address input
I/00-I/017	Data-in/data-out
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Read/write enable
OE	Output enable
VCC	Power (+5V)
VSS	Ground

Outline Dimensions

Unit: mm(inch)

- HM514180JP Series (CP-40D)



Rev.1
Jul. 11, 1989

HB56A48A/AT/B-8/10/12

4,194,304-Word × 8-Bit High Density Dynamic RAM Module

Description

The HB56A48 is a 4M × 8 dynamic RAM module, mounted eight 4Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A48 is 30-pin single in-line package having Lead types (HB56A48A, HB56A48AT), Socket type (HB56A48B). Therefore, the HB56A48 makes high density mounting possible without surface mount technology. The HB56A48 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

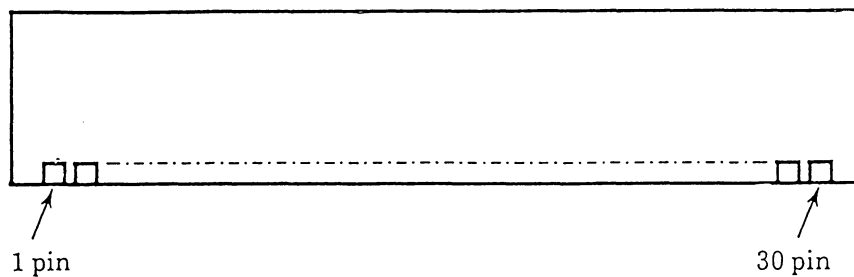
Feature

- 30-pin single in-line package
 - Lead pitch 2.54mm
- Single 5V (±10%) supply
- High speed
 - Access time 80ns/100ns/120ns (max.)
- Low power dissipation
 - Active mode 3.96W/3.52W/3.08W (max.)
 - Standby mode 88mW (max.)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

Ordering Information

Access time	Package		
	30-pin SIP Lead type	30-pin SIP Low Profile Lead type	30-pin SIP Socket type
80ns	HB56A48A-8	HB56A48AT-8	HB56A48B-8
100ns	HB56A48A-10	HB56A48AT-10	HB56A48B-10
120ns	HB56A48A-12	HB56A48AT-12	HB56A48B-12

■ Pin Out

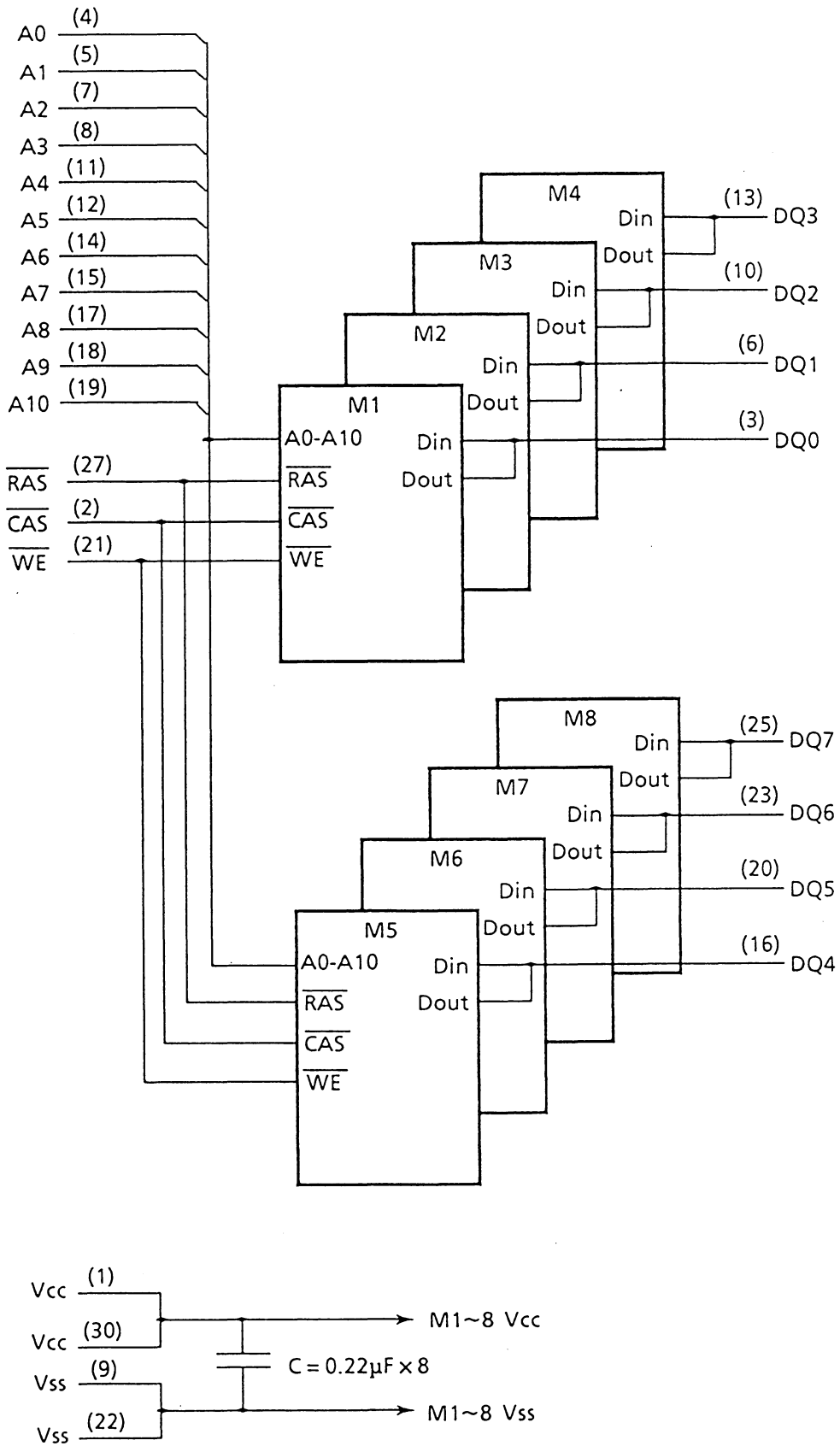


Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ4
2	$\overline{\text{CAS}}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{\text{WE}}$
7	A2	22	V _{SS}
8	A3	23	DQ6
9	V _{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	NC
12	A5	27	$\overline{\text{RAS}}$
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	V _{CC}

■ Pin Description

Pin Name	Function
A0~A10	Address Input
A0~A9	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
DQ0~DQ7	Data-in / Data-out
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
NC	Non-connection

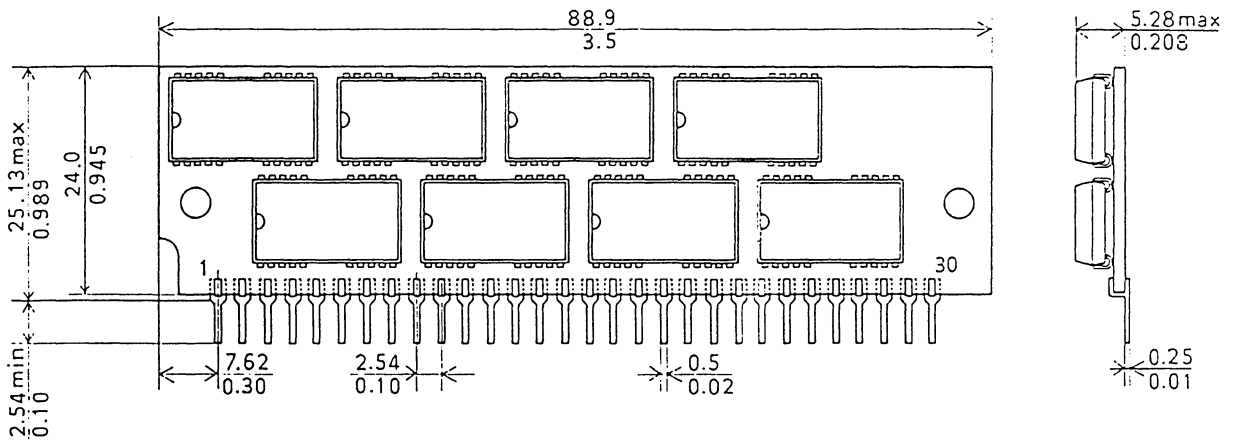
■ Block Diagram



■ Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$

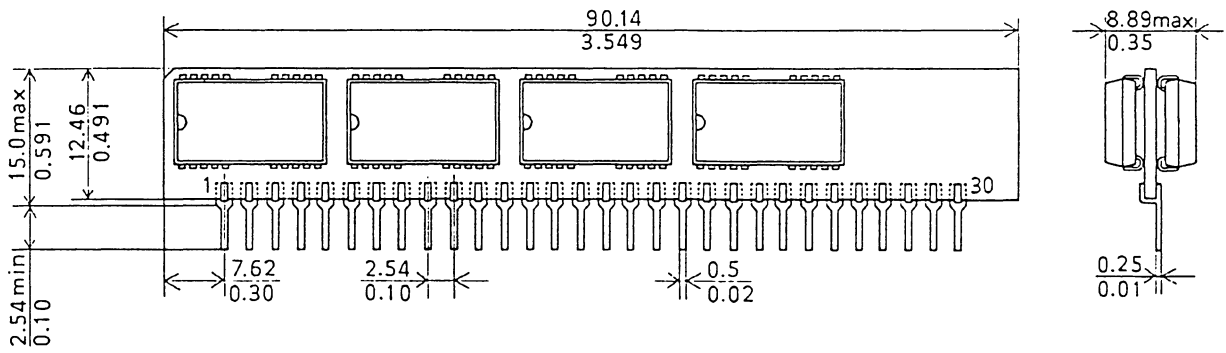
● HB56A48A serie



Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$

● HB56A48AT serie



HB56A48A/AT/B-8F

4,194,304-Word × 8-Bit High Density Dynamic RAM Module

Description

The HB56A48 is a 4M × 8 dynamic RAM module, mounted eight 4Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A48 is 30-pin single in-line package having lead types (HB56A48A, HB56A48AT), socket type (HB56A48B). Therefore, the HB56A48 makes high density mounting possible without surface mount technology. The HB56A48 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

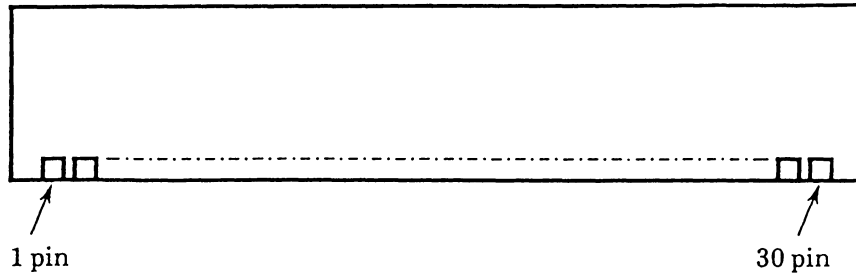
■ Feature

- 30-pin single in-line package
 - Lead pitch 2.54mm
- Single 5V (±10%) supply
- High speed
 - Access time 80ns (max.)
- Low power dissipation
 - Active mode 3.96W (max.)
 - Standby mode 88mW (max.)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

■ Ordering Information

	Package		
	30-pin SIP lead type	30-pin SIP Low Profile lead type	30-pin SIP socket type
Access time 80ns	HB56A48A-8F	HB56A48AT-8F	HB56A48B-8F

■ Pinout

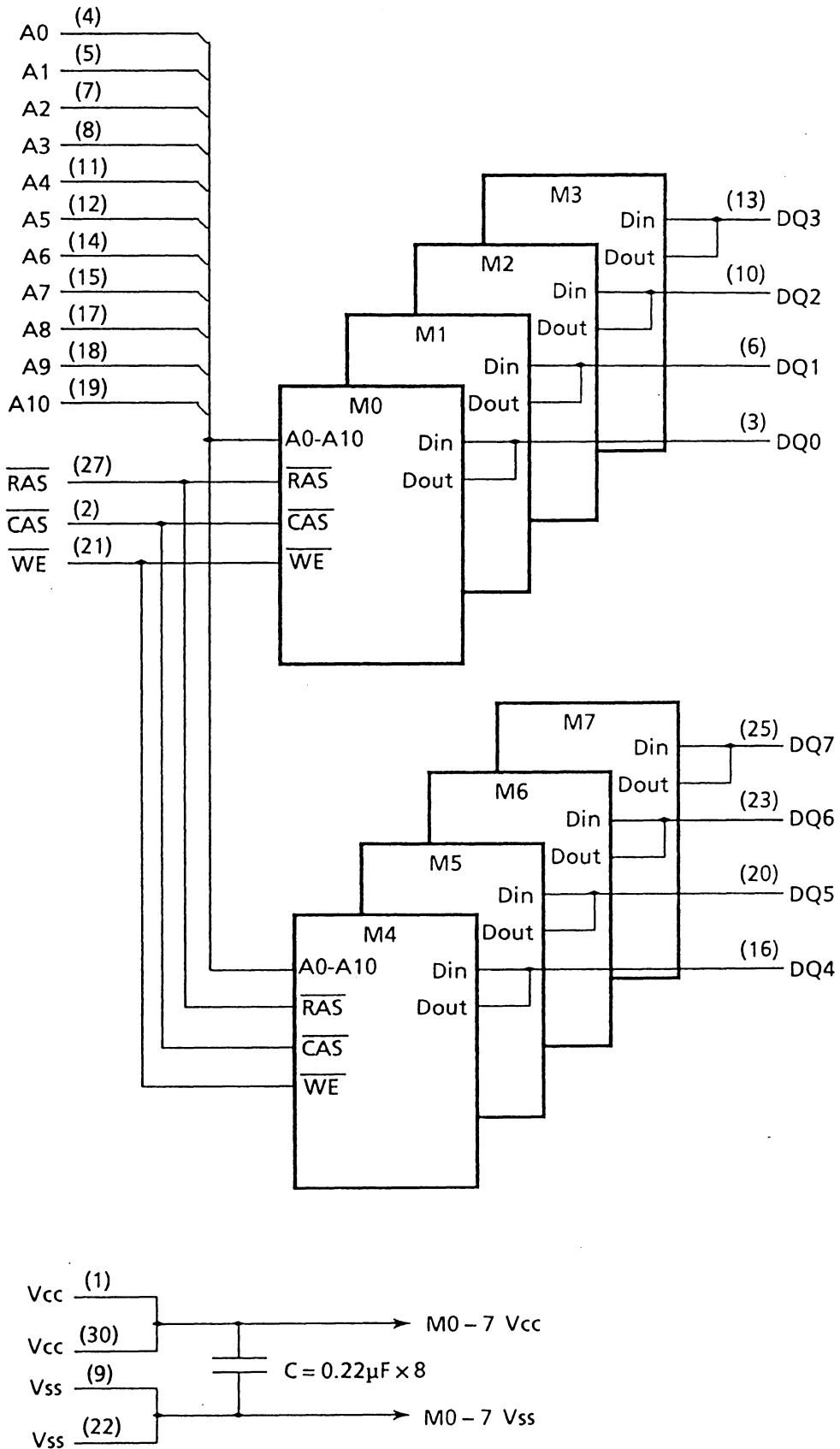


Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ4
2	CAS	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	WE
7	A2	22	V _{SS}
8	A3	23	DQ6
9	V _{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	NC
12	A5	27	RAS
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	V _{CC}

■ Pin Description

Pin Name	Function
A0 – A10	Address Input
A0 – A9	Refresh Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read / Write Enable
DQ0 – DQ7	Data-in / Data-out
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
NC	No connection

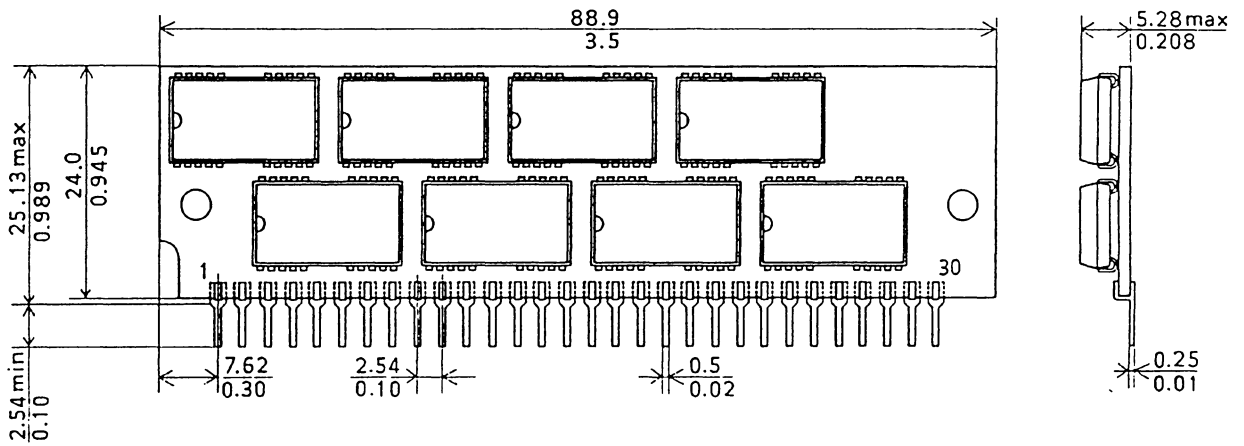
■ Block Diagram



Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$

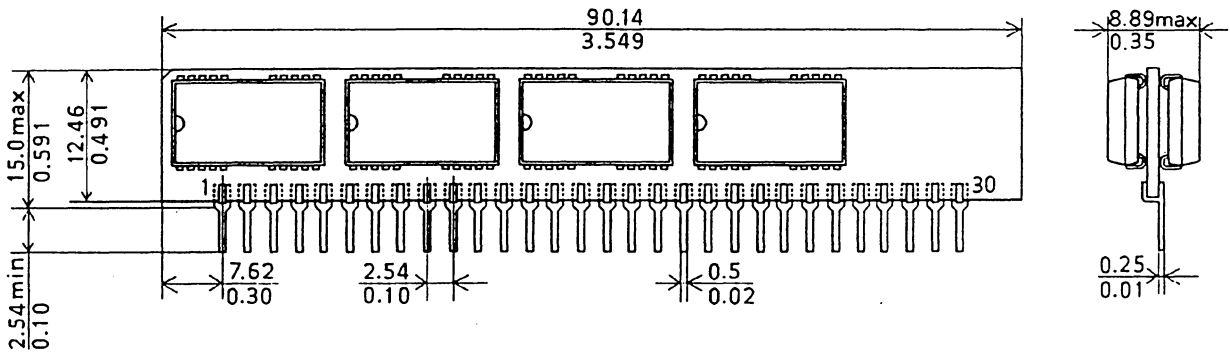
● HB56A48A serie



■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

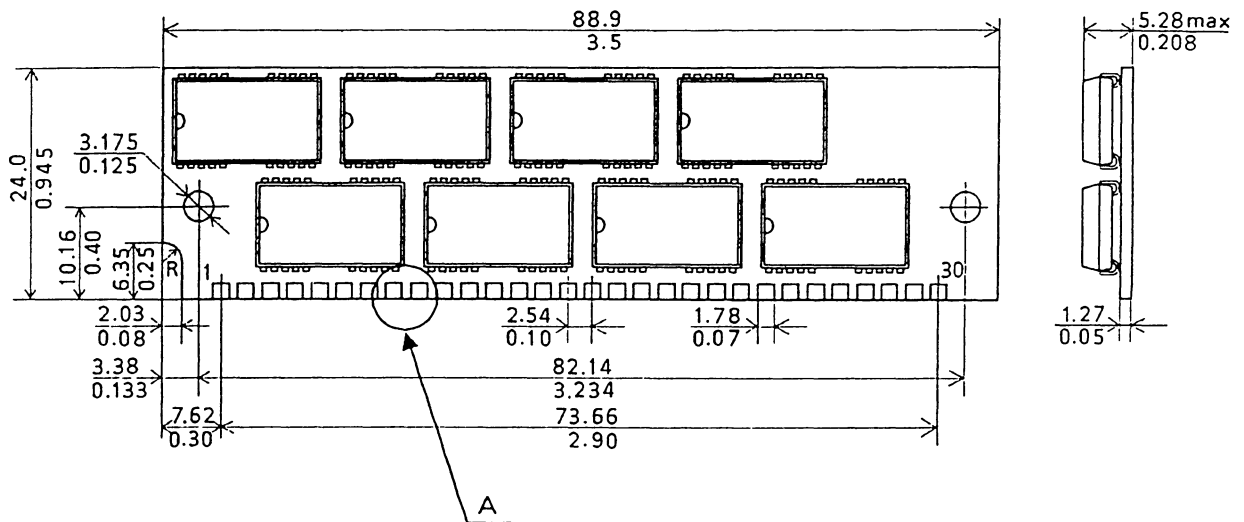
● HB56A48AT serise



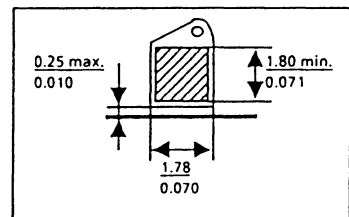
■ Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$

● HB56A48B serie



Note : The plating of the contact finger is solder coat.



Detail A

Rev.1
Jul. 11, 1989

HB56A49A/AT/B-8/10/12

4,194,304-Word × 9-Bit High Density Dynamic RAM Module

Description

The HB56A49 is a 4M×9 dynamic RAM module, mounted nine 4Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A49 is 30-pin single in-line package having Lead types (HB56A49A, HB56A49AT), Socket type (HB56A49B). Therefore, the HB56A49 makes high density mounting possible without surface mount technology. The HB56A49 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

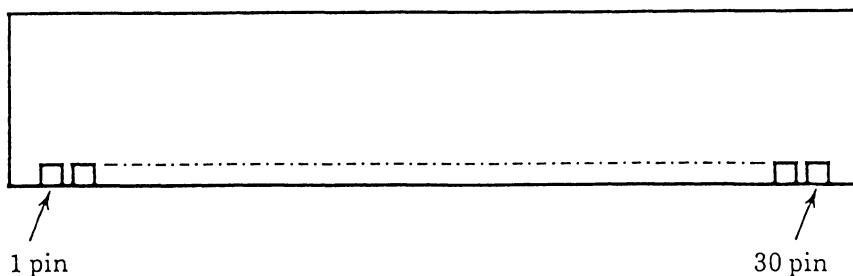
■ Feature

- 30-pin single in-line package
 - Lead pitch 2.54mm
- Single 5V (±10%) supply
- High speed
 - Access time 80ns/100ns/120ns (max.)
- Low power dissipation
 - Active mode 4455mW/3960mW/3465mW (max.)
 - Standby mode 99mW (max.)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - CAS before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

■ Ordering Information

Access time	Package		
	30-pin SIP Lead type	30-pin SIP Low Profile Lead type	30-pin SIP Socket type
80ns	HB56A49A-8	HB56A49AT-8	HB56A49B-8
100ns	HB56A49A-10	HB56A49AT-10	HB56A49B-10
120ns	HB56A49A-12	HB56A49AT-12	HB56A49B-12

■ Pin Out

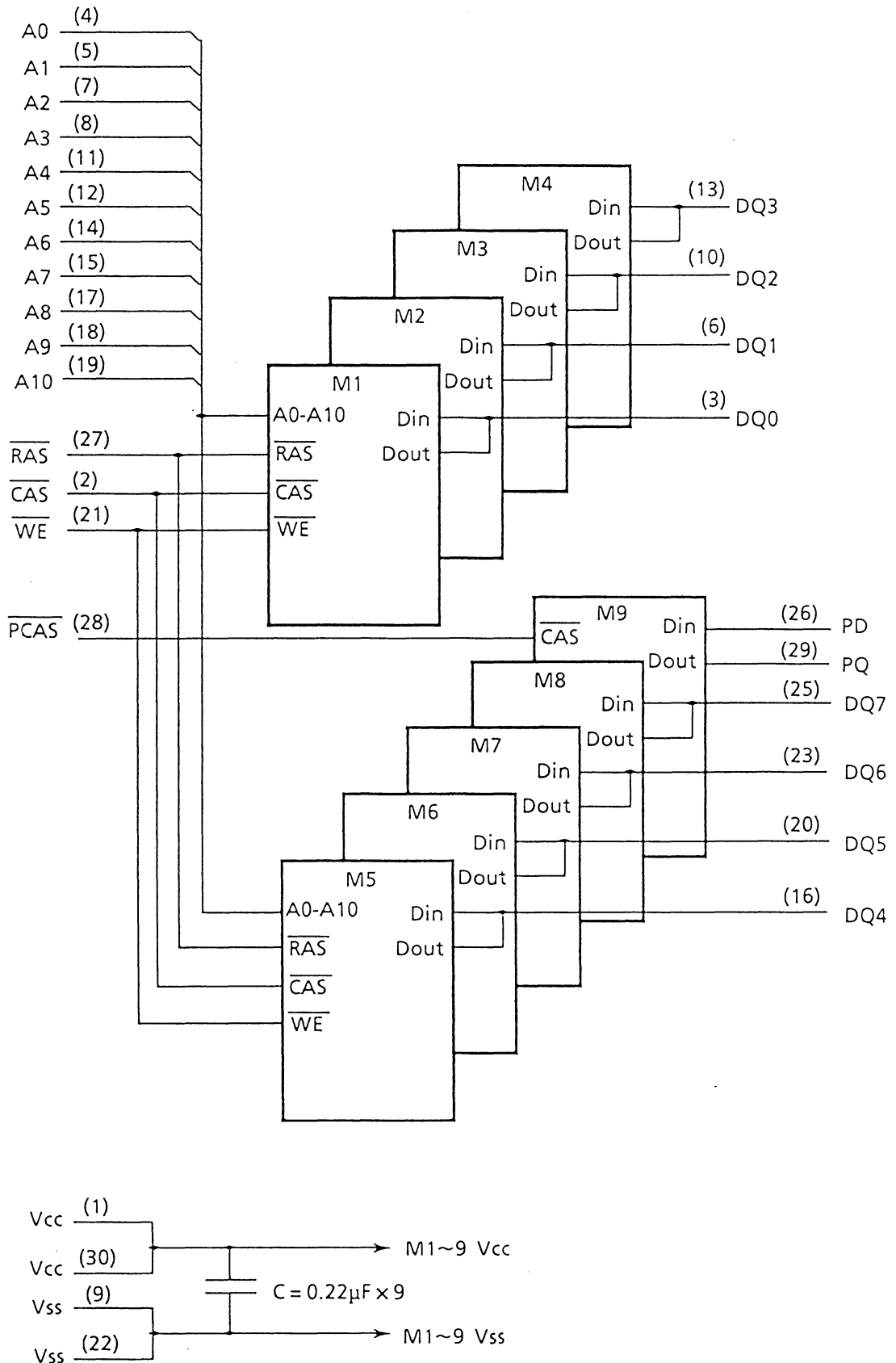


Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ4
2	$\overline{\text{CAS}}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{\text{WE}}$
7	A2	22	V _{SS}
8	A3	23	DQ6
9	V _{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{\text{RAS}}$
13	DQ3	28	$\overline{\text{PCAS}}$
14	A6	29	PD
15	A7	30	V _{CC}

■ Pin Description

Pin Name	Function
A0~A10	Address Input
A0~A9	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$, $\overline{\text{PCAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
DQ0~DQ7	Data-in / Data-out
PD	Parity Data-in
PQ	Parity Data-out
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
NC	Non-connection

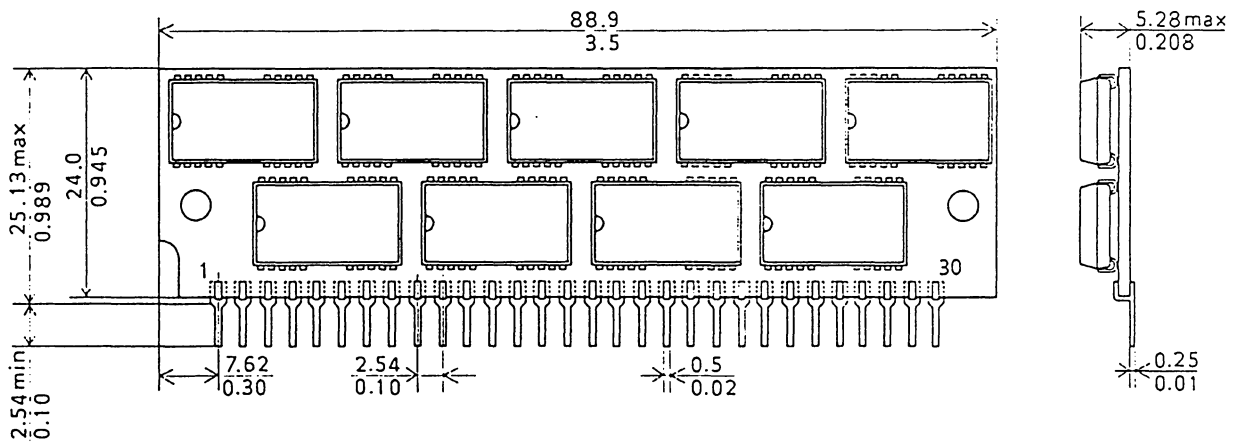
Block Diagram



■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

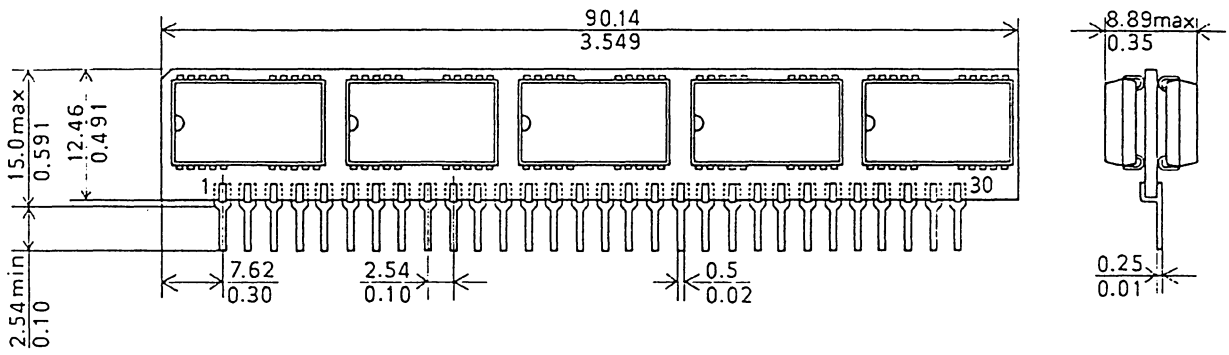
● HB56A49A serie



■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

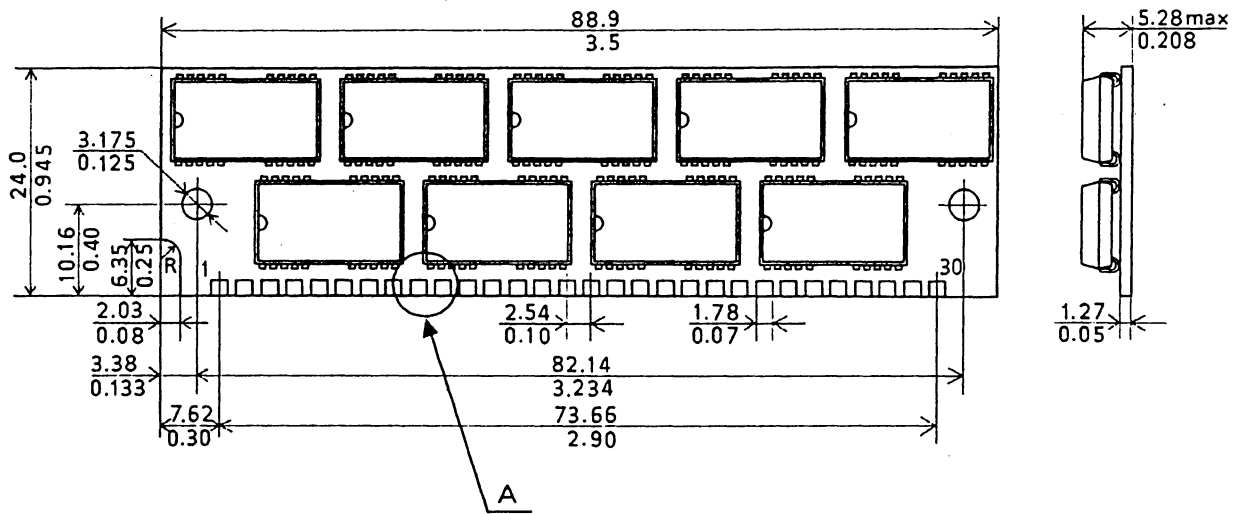
● HB56A49AT serie



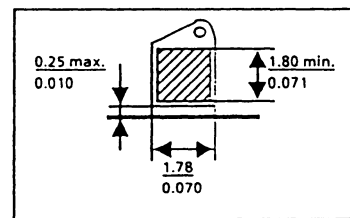
■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

● HB56A49B serie



Note : The plating of the contact finger is solder coat.



Detail A

Rev.0
Nov. 20, 1989

HB56A49A/AT/B-8F

4,194,304-Word × 9-Bit High Density Dynamic RAM Module

Description

The HB56A49 is a 4M×9 dynamic RAM module, mounted nine 4Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A49 is 30-pin single in-line package having lead types (HB56A49A, HB56A49AT), socket type (HB56A49B). Therefore, the HB56A49 makes high density mounting possible without surface mount technology. The HB56A49 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

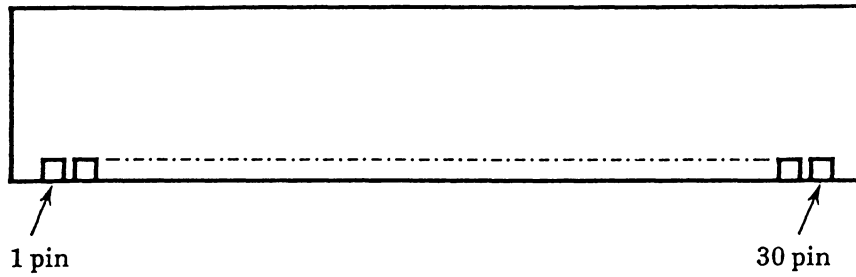
Feature

- 30-pin single in-line package
 - Lead pitch 2.54mm
- Single 5V (±10%) supply
- High speed
 - Access time 80ns (max.)
- Low power dissipation
 - Active mode 4455mW (max.)
 - Standby mode 99mW (max.)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

Ordering Information

	Package		
	30-pin SIP lead type	30-pin SIP Low Profile lead type	30-pin SIP socket type
Access time 80ns	HB56A49A-8F	HB56A49AT-8F	HB56A49B-8F

■ Pinout

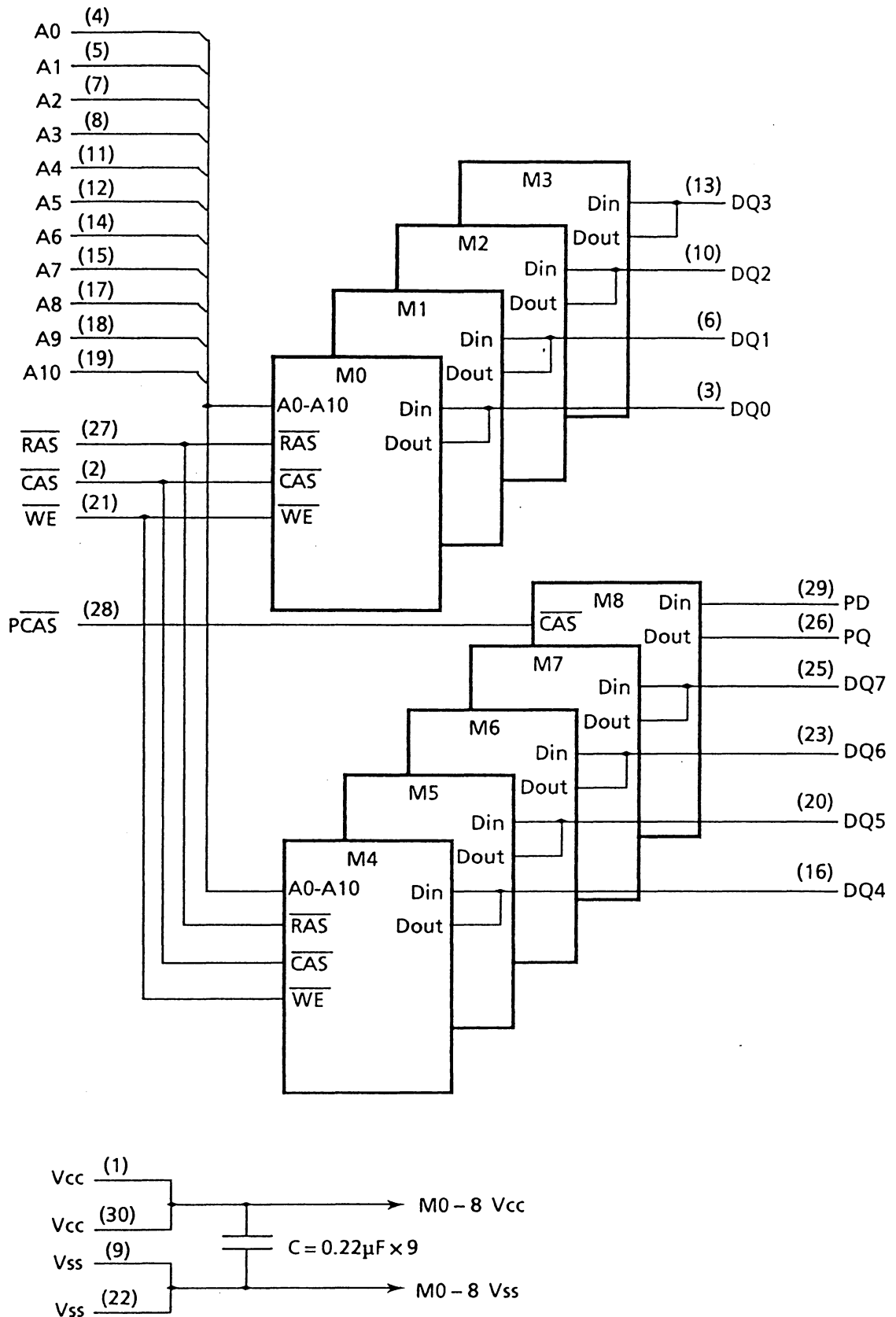


Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ4
2	$\overline{\text{CAS}}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{\text{WE}}$
7	A2	22	V _{SS}
8	A3	23	DQ6
9	V _{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{\text{RAS}}$
13	DQ3	28	$\overline{\text{PCAS}}$
14	A6	29	PD
15	A7	30	V _{CC}

■ Pin Description

Pin Name	Function
A0 – A10	Address Input
A0 – A9	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
DQ0 – DQ7	Data-in / Data-out
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
NC	No connection

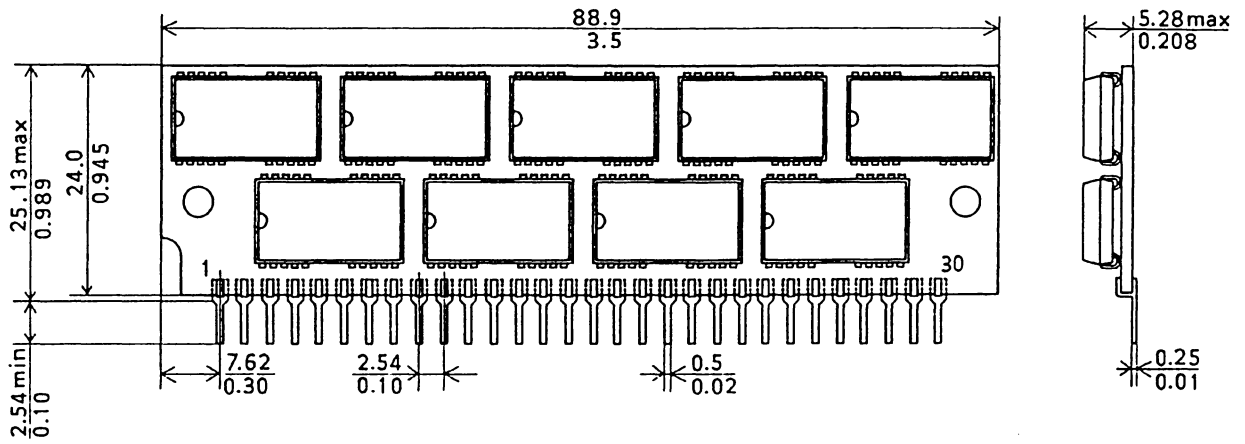
■ Block Diagram



Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

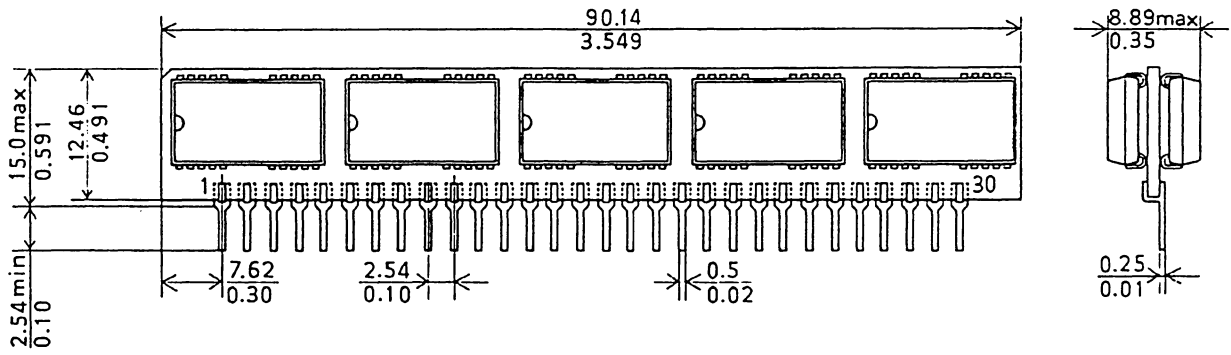
● HB56A49A serie



Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$

● HB56A49AT serise



Rev.0
Dec. 13, 1989

HB56A49BR-8/10/12

4,194,304-Word × 8-Bit High Density Dynamic RAM Module

Description

The HB56A49BR is a 4M × 9 dynamic RAM module, mounted 9 pieces of 4Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A49BR is 30-pin single in-line package. Therefore, the HB56A49BR makes high density mounting possible without surface mount technology. The HB56A49BR provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

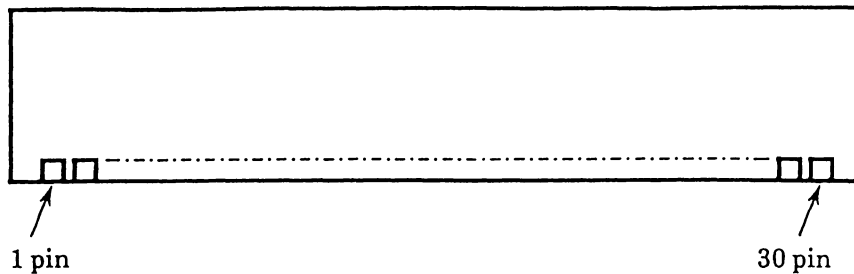
Feature

- 30-pin single in-line package
 - Lead pitch 2.54mm
- Single 5V (±10%) supply
- High speed
 - Access time 80ns/100ns/120ns (max.)
- Low power dissipation
 - Active mode 4455mW/3960mW/3465mW (max.)
 - Standby mode 99mW (max.)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 3 variations of refresh
 - RAS only refresh
 - $\overline{\text{CAS}}$ before RAS refresh
 - $\overline{\text{Hidden refresh}}$
- TTL compatible

Ordering Information

Part No.	Access time	Package
HB56A49BR-8	80ns	30-pin SIP socket type
HB56A49BR-10	100ns	
HB56A49BR-12	120ns	

■ Pinout

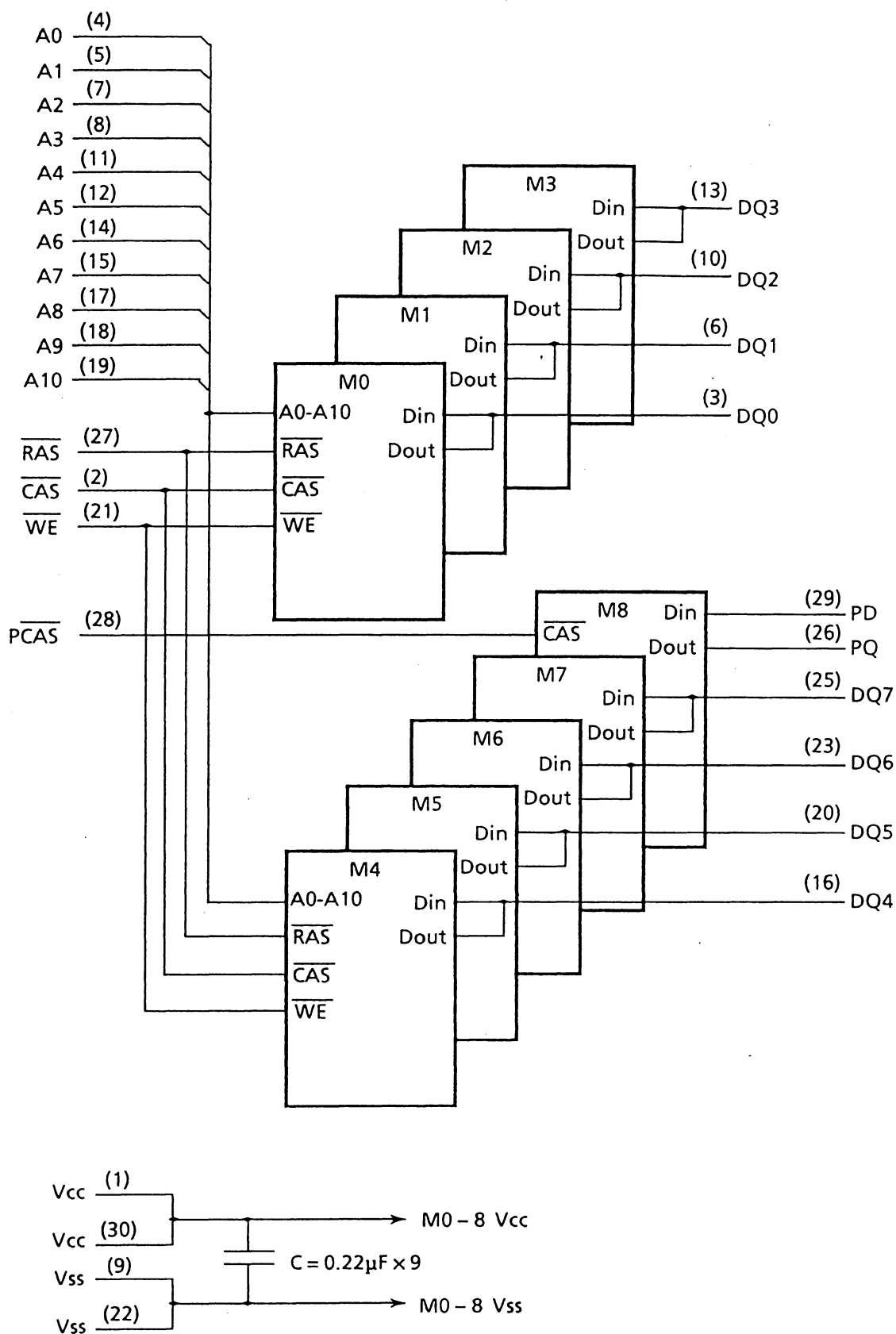


Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ4
2	$\overline{\text{CAS}}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{\text{WE}}$
7	A2	22	V _{SS}
8	A3	23	DQ6
9	V _{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{\text{RAS}}$
13	DQ3	28	$\overline{\text{PCAS}}$
14	A6	29	PD
15	A7	30	V _{CC}

■ Pin Description

Pin Name	Function
A0 – A10	Address Input
A0 – A9	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
DQ0 – DQ7	Data-in / Data-out
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
NC	No connection

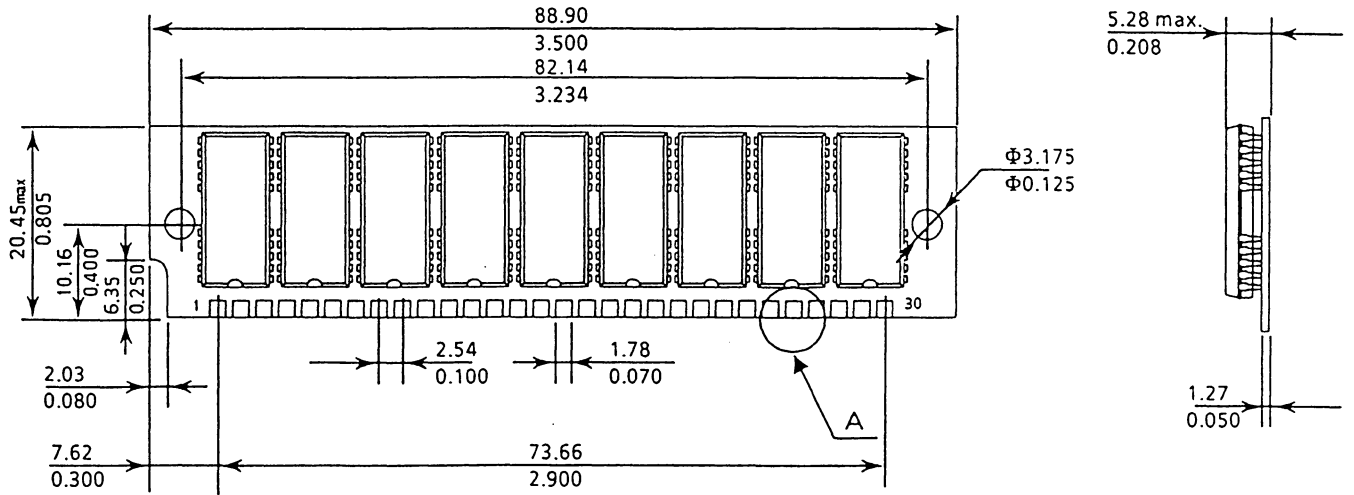
■ Block Diagram



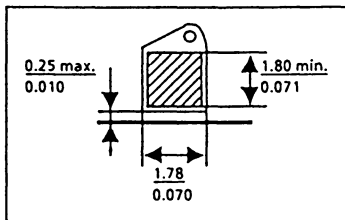
Physical Outline

● HB56A49BR

Unit: $\frac{\text{mm}}{\text{inch}}$



Detail A



Note: The plating of the contact finger is solder coat.

HB56B49A/AT/B-8/10/12

4,194,304-Word × 9-Bit High Density Dynamic RAM Module

Description

The HB56B49 is a 4M×9 dynamic RAM module, mounted nine 4Mbit DRAM (HM514101JP) sealed in SOJ package. An outline of the HB56B49 is 30-pin single in-line package having Lead types (HB56B49A, HB56B49AT), Socket type (HB56B49B). Therefore, the HB56B49 makes high density mounting possible without surface mount technology. The HB56B49 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

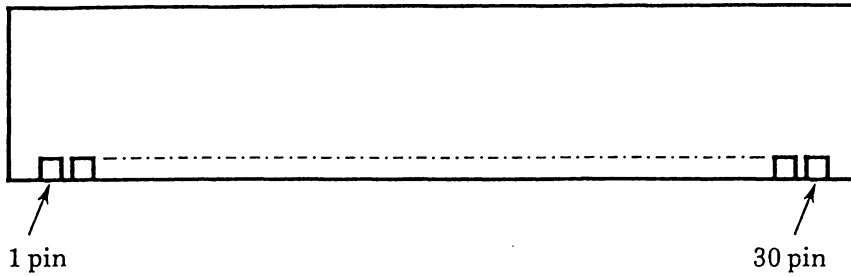
■ Feature

- 30-pin single in-line package
 - Lead pitch 2.54mm
- Single 5V (±10%) supply
- High speed
 - Access time 80ns/100ns/120ns (max.)
- Low power dissipation
 - Active mode 4455mW/3960mW/3465mW (max.)
 - Standby mode 99mW (max.)
- Nibble mode capability
- 1,024 refresh cycle / 16ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - CAS before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

■ Ordering Information

Access time	Package		
	30-pin SIP Lead type	30-pin SIP Low Profile Lead type	30-pin SIP Socket type
80ns	HB56B49A-8	HB56B49AT-8	HB56B49B-8
100ns	HB56B49A-10	HB56B49AT-10	HB56B49B-10
120ns	HB56B49A-12	HB56B49AT-12	HB56B49B-12

■ Pin Out

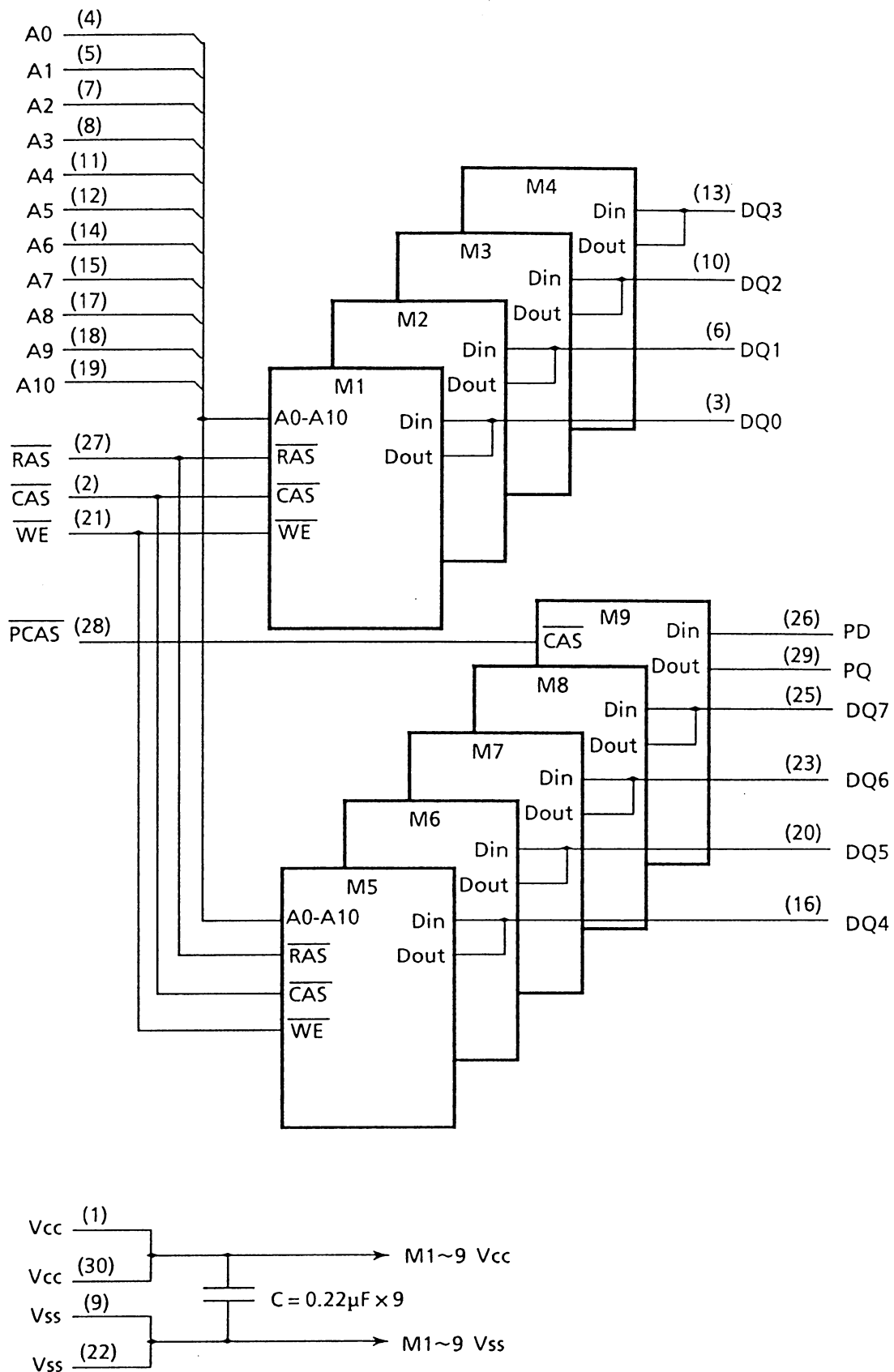


Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ4
2	$\overline{\text{CAS}}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{\text{WE}}$
7	A2	22	V _{SS}
8	A3	23	DQ6
9	V _{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{\text{RAS}}$
13	DQ3	28	$\overline{\text{PCAS}}$
14	A6	29	PD
15	A7	30	V _{CC}

■ Pin Description

Pin Name	Function
A0~A10	Address Input
A0~A9	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}, \overline{\text{PCAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
DQ0~DQ7	Data-in / Data-out
PD	Parity Data-in
PQ	Parity Data-out
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
NC	Non-connection

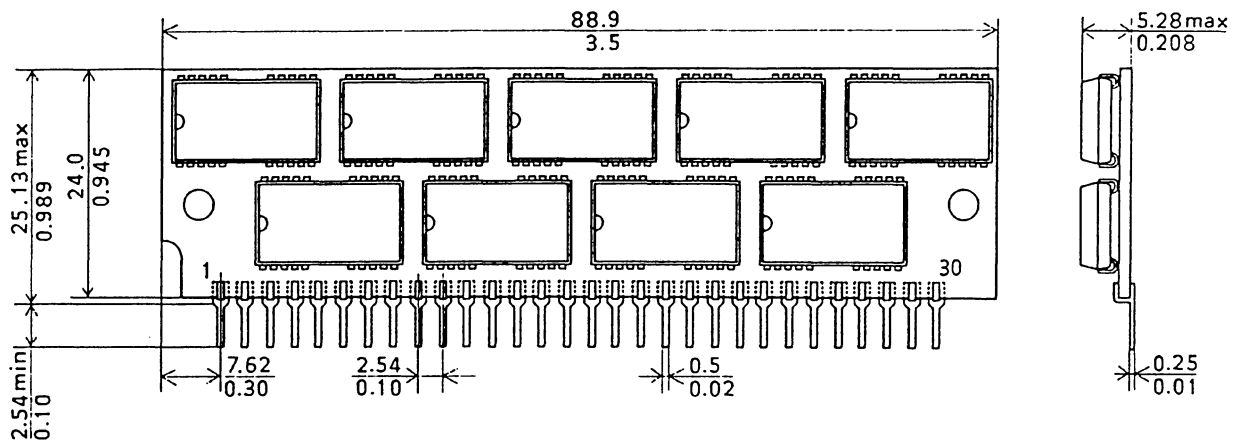
■ Block Diagram



■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

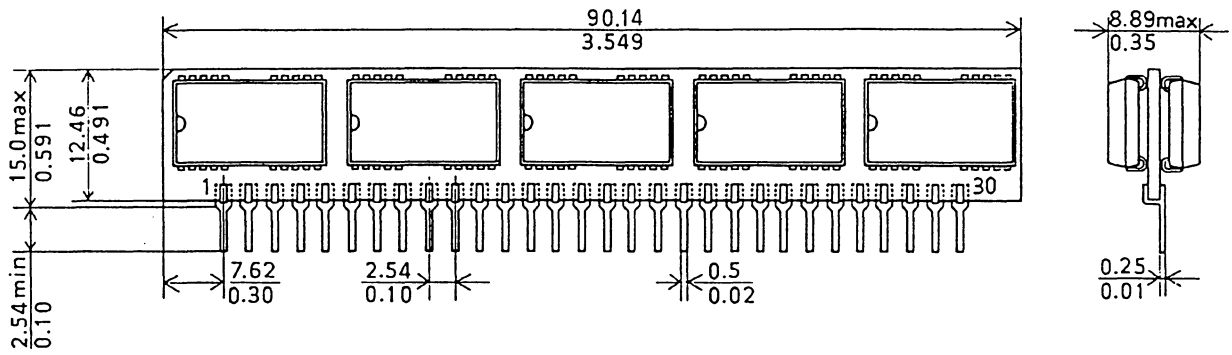
- HB56B49A serie



Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$

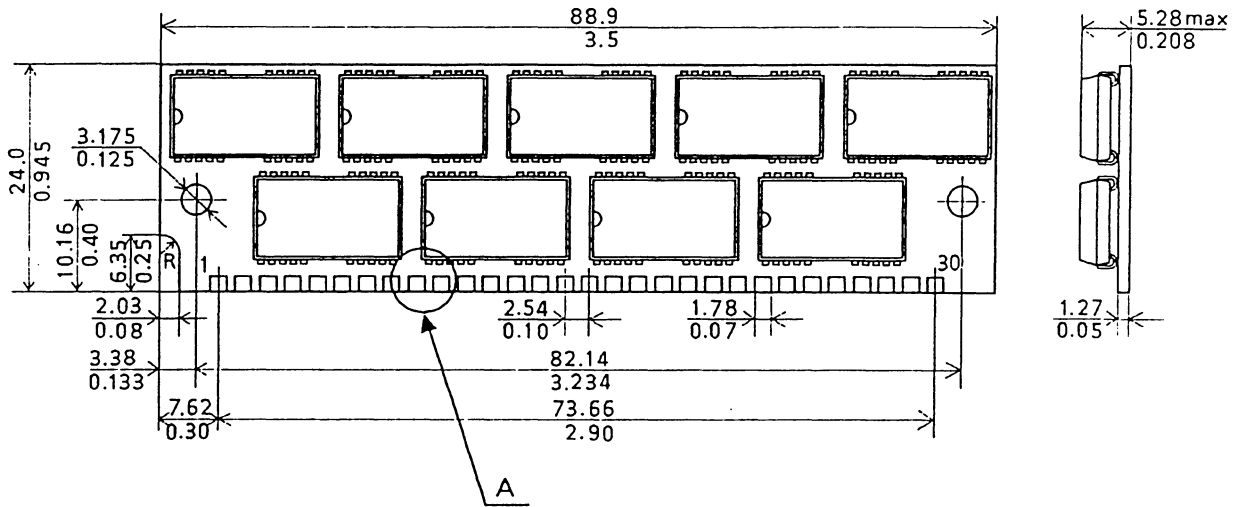
● HB56B49AT serise



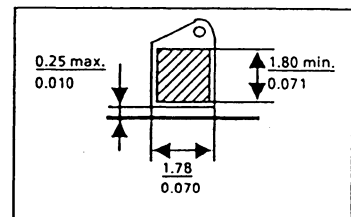
■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

● HB56B49B serie



Note : The plating of the contact finger is solder coat.



Detail A

Rev.0
Oct. 02, 1989

HB56C49A/AT/B-8/10/12

4,194,304-Word × 9-Bit High Density Dynamic RAM Module

Description

The HB56C49 is a 4M×9 dynamic RAM module, mounted nine 4Mbit DRAM (HM514102JP) sealed in SOJ package. An outline of the HB56C49 is 30-pin single in-line package having Lead types (HB56C49A, HB56C49AT), Socket type (HB56C49B). Therefore, the HB56C49 makes high density mounting possible without surface mount technology. The HB56C49 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

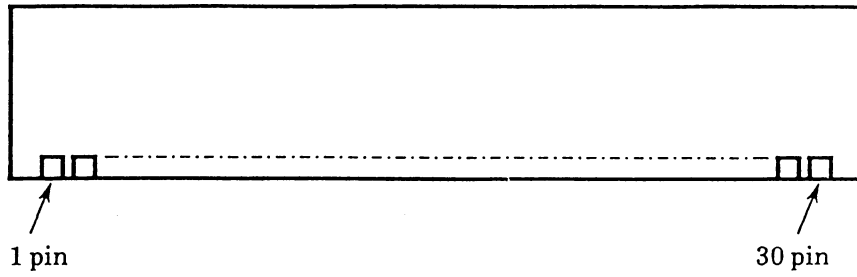
■ Feature

- 30-pin single in-line package
 - Lead pitch 2.54mm
- Single 5V (±10%) supply
- High speed
 - Access time 80ns/100ns/120ns (max.)
- Low power dissipation
 - Active mode 4455mW/3960mW/3465mW (max.)
 - Standby mode 99mW (max.)
- Static column mode capability
- 1,024 refresh cycle / 16ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - CS before RAS refresh
 - Hidden refresh
- TTL compatible

■ Ordering Information

Access time	Package		
	30-pin SIP Lead type	30-pin SIP Low Profile Lead type	30-pin SIP Socket type
80ns	HB56C49A-8	HB56C49AT-8	HB56C49B-8
100ns	HB56C49A-10	HB56C49AT-10	HB56C49B-10
120ns	HB56C49A-12	HB56C49AT-12	HB56C49B-12

■ Pin Out

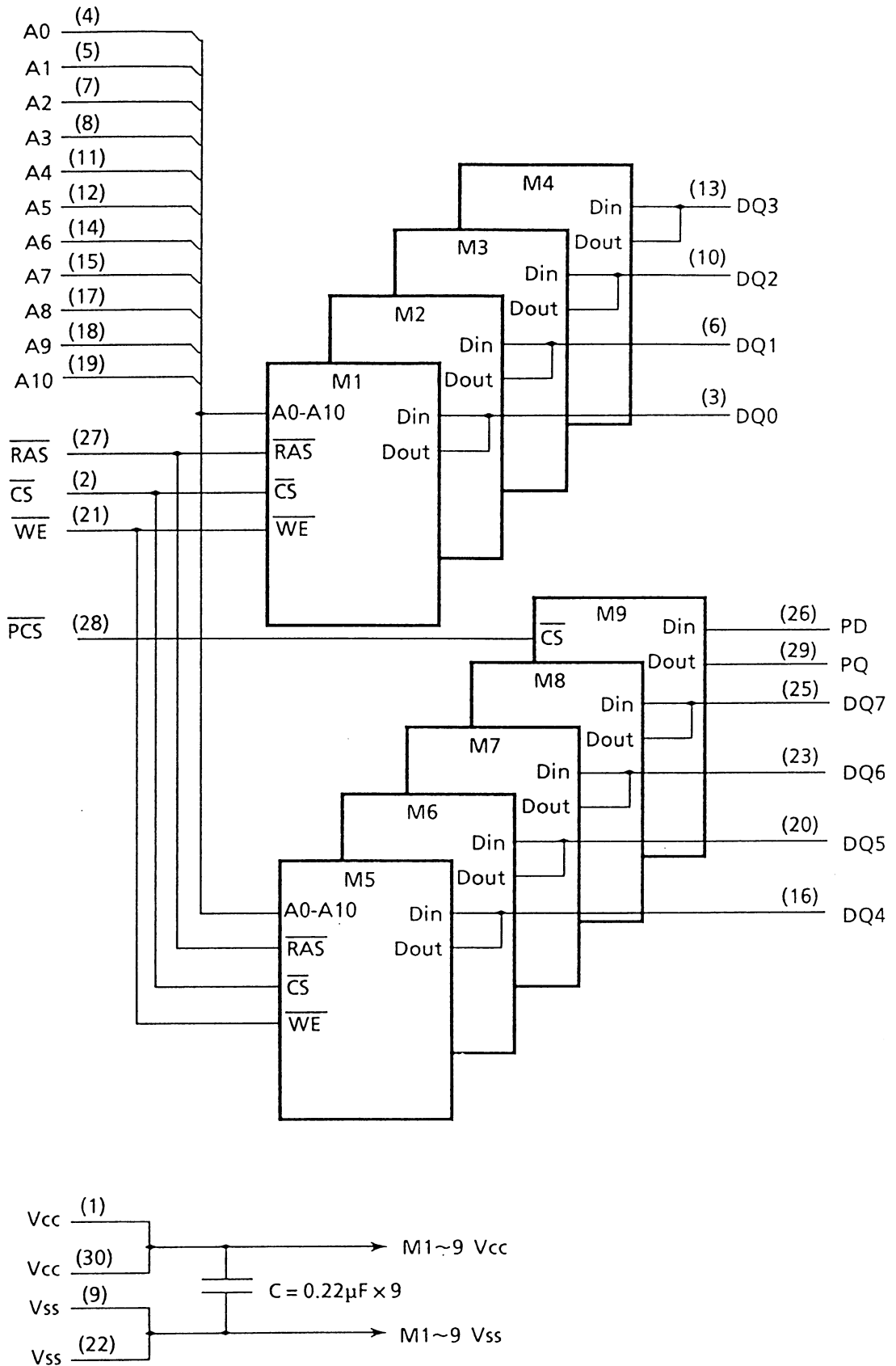


Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ4
2	$\overline{\text{CS}}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{\text{WE}}$
7	A2	22	V _{SS}
8	A3	23	DQ6
9	V _{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{\text{RAS}}$
13	DQ3	28	$\overline{\text{PCS}}$
14	A6	29	PD
15	A7	30	V _{CC}

■ Pin Description

Pin Name	Function
A0~A10	Address Input
A0~A9	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CS}}$, $\overline{\text{PCS}}$	Chip Select
$\overline{\text{WE}}$	Read / Write Enable
DQ0~DQ7	Data-in / Data-out
PD	Parity Data-in
PQ	Parity Data-out
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
NC	Non-connection

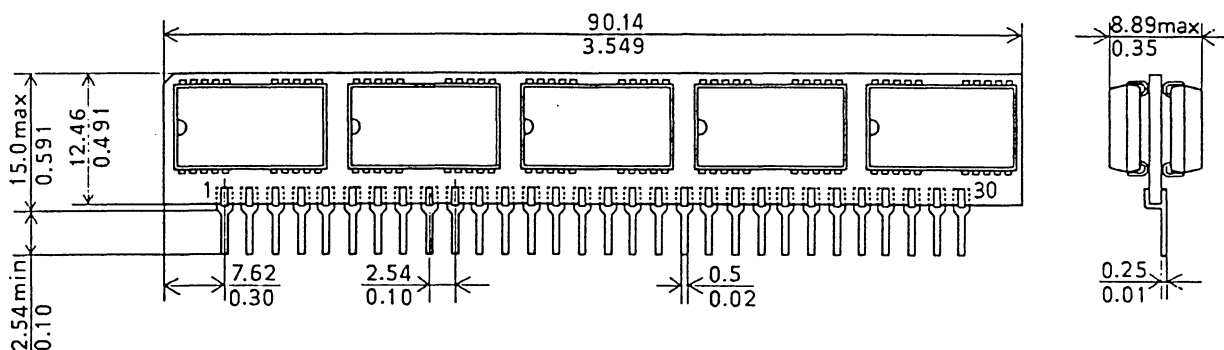
■ Block Diagram



Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

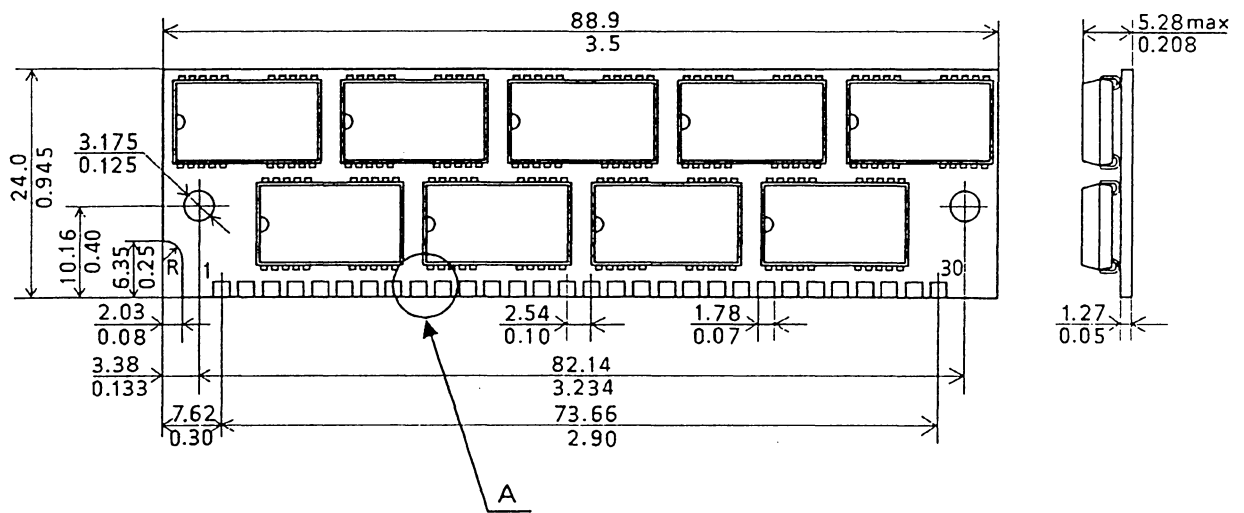
● HB56C49AT serise



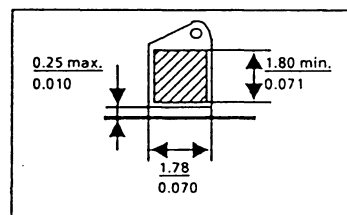
■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$

● HB56C49B serie



Note : The plating of the contact finger is solder coat.



Detail A

Rev.0
Jan. 12, 1990

HB56D132BR-8/10/12

1,048,576-Word × 32-Bit High Density Dynamic RAM Module

Description

The HB56D132BR is a 1M × 32 dynamic RAM module, mounted 8 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package. An outline of the HB56D132BR is 72-pin single in-line package. Therefore, the HB56D132BR makes high density mounting possible without surface mount technology. The HB56D132BR provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

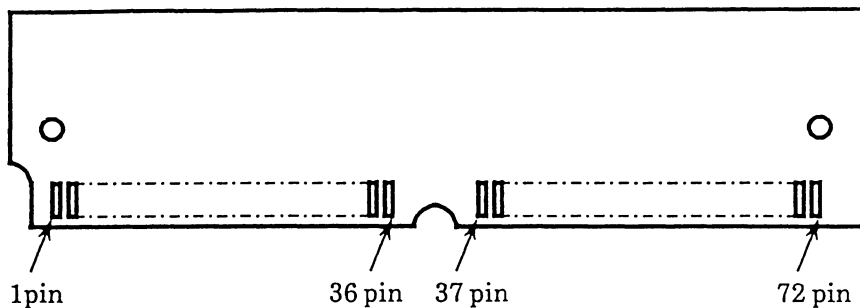
■ Feature

- 72-pin single in-line package
 - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
 - Access time 80ns / 100ns / 120ns (max)
- Low power dissipation
 - Active mode 3.78W / 3.36W / 2.94W (max)
 - Standby mode 84mW (max)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

■ Ordering Information

Part No.	Access time	Package
HB56D132BR-8	80ns	72-pin SIP socket type
HB56D132BR-10	100ns	
HB56D132BR-12	120ns	

■ Pinout



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{\text{CAS1}}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

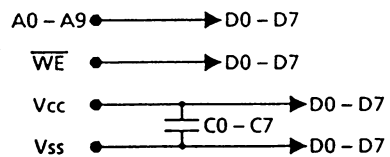
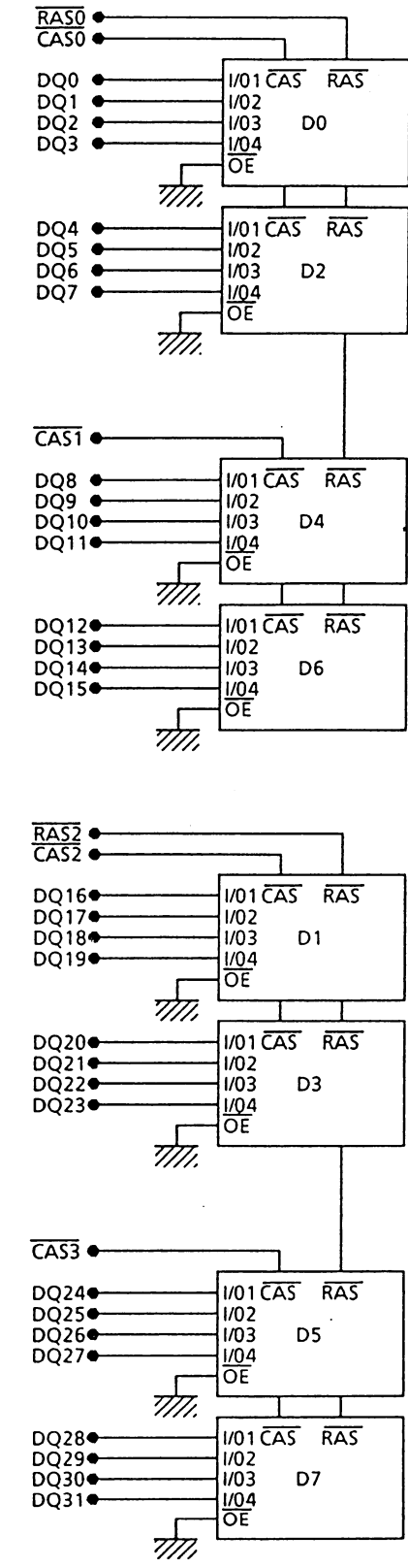
■ Pin Description

Pin Name	Function
A0 – A9	Address Input
A0 – A9	Refresh Address Input
DQ0 – DQ31	Data-in / Data-out
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
PD1 – PD4	Presence Detect Pin
NC	No connection

■ Presence Detect Pinout

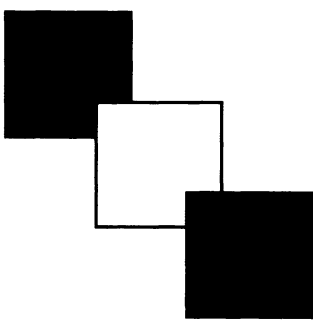
Pin No.	Pin Name	HB56D132BR		
		80ns	100ns	120ns
67	PD1	V _{SS}	V _{SS}	V _{SS}
68	PD2	V _{SS}	V _{SS}	V _{SS}
69	PD3	NC	V _{SS}	NC
70	PD4	V _{SS}	V _{SS}	NC

■ Block Diagram



* D0 - D7 : HM514400JP

Rev.0
Nov. 15. 1989



HB56D232B-8/10/12

2,097,152-Word × 32-Bit High Density Dynamic RAM Module

Description

The HB56D232B is a 2M × 32 dynamic RAM module, mounted 16 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package. An outline of the HB56D232B is 72-pin single in-line package. Therefore, the HB56D232B makes high density mounting possible without surface mount technology. The HB56D232B provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

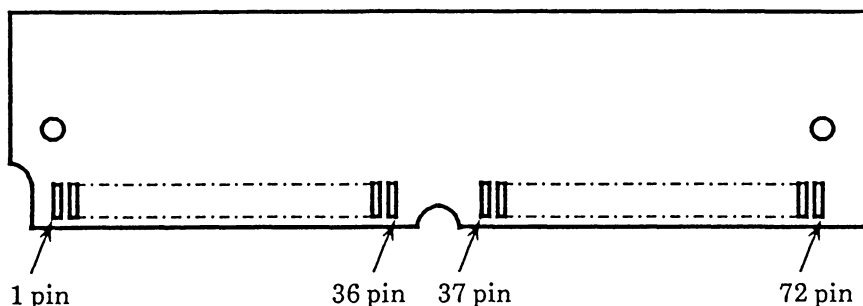
■ Feature

- 72-pin single in-line package
 - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
 - Access time 80ns / 100ns / 120ns (max)
- Low power dissipation
 - Active mode 3.99W / 3.57W / 3.15W (max)
 - Standby mode 168mW (max)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

■ Ordering Information

Part No.	Access time	Package
HB56D232B-8	80ns	72-pin SIP socket type
HB56D232B-10	100ns	
HB56D232B-12	120ns	

■ Pinout



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{\text{CAS1}}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{\text{RAS1}}$	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	$\overline{\text{RAS3}}$	51	DQ9	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

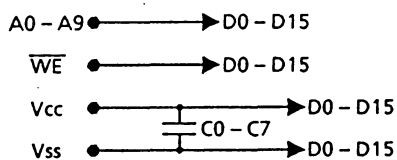
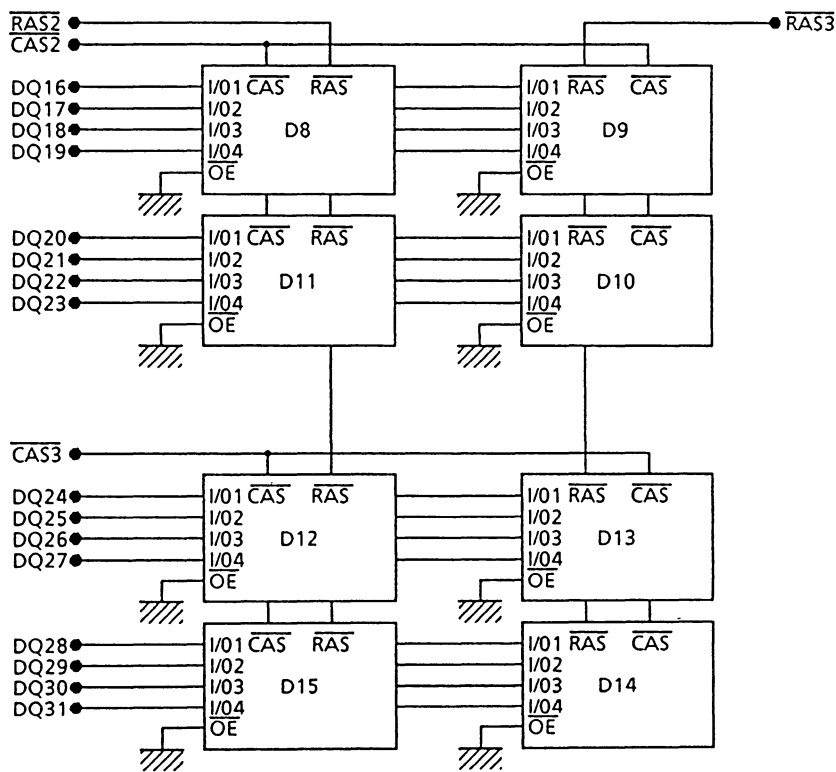
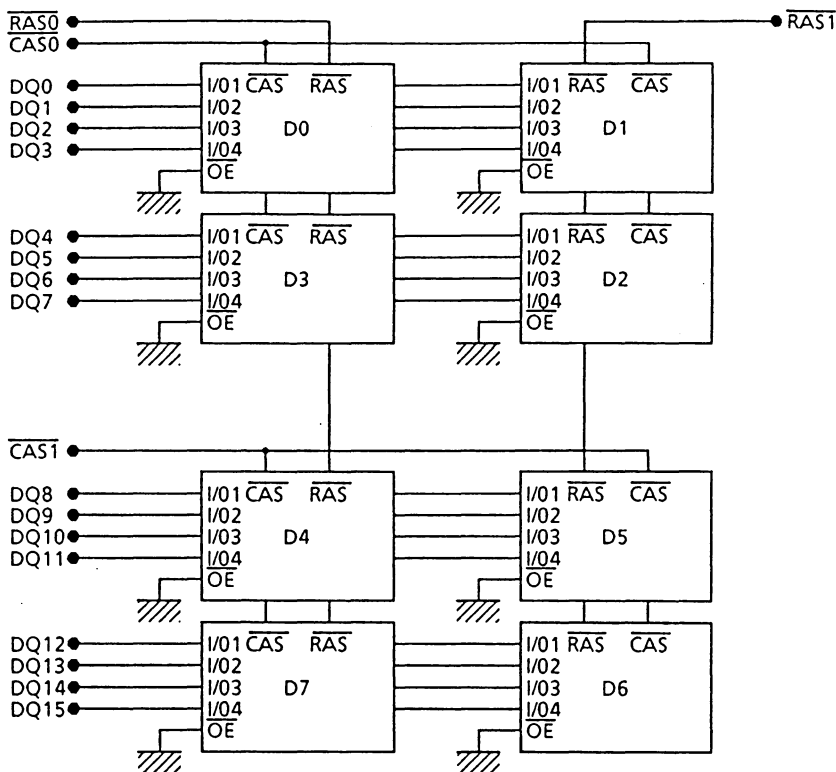
■ Pin Description

Pin Name	Function
A0 – A9	Address Input
A0 – A9	Refresh Address Input
DQ0 – DQ31	Data-in / Data-out
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}} - \overline{\text{RAS3}}$	Row Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
PD1 – PD4	Presence Detect Pin
NC	No connection

■ Presence Detect Pinout

Pin No.	Pin Name	HB56D232B		
		80ns	100ns	120ns
67	PD1	NC	NC	NC
68	PD2	NC	NC	NC
69	PD3	NC	V _{SS}	NC
70	PD4	V _{SS}	V _{SS}	NC

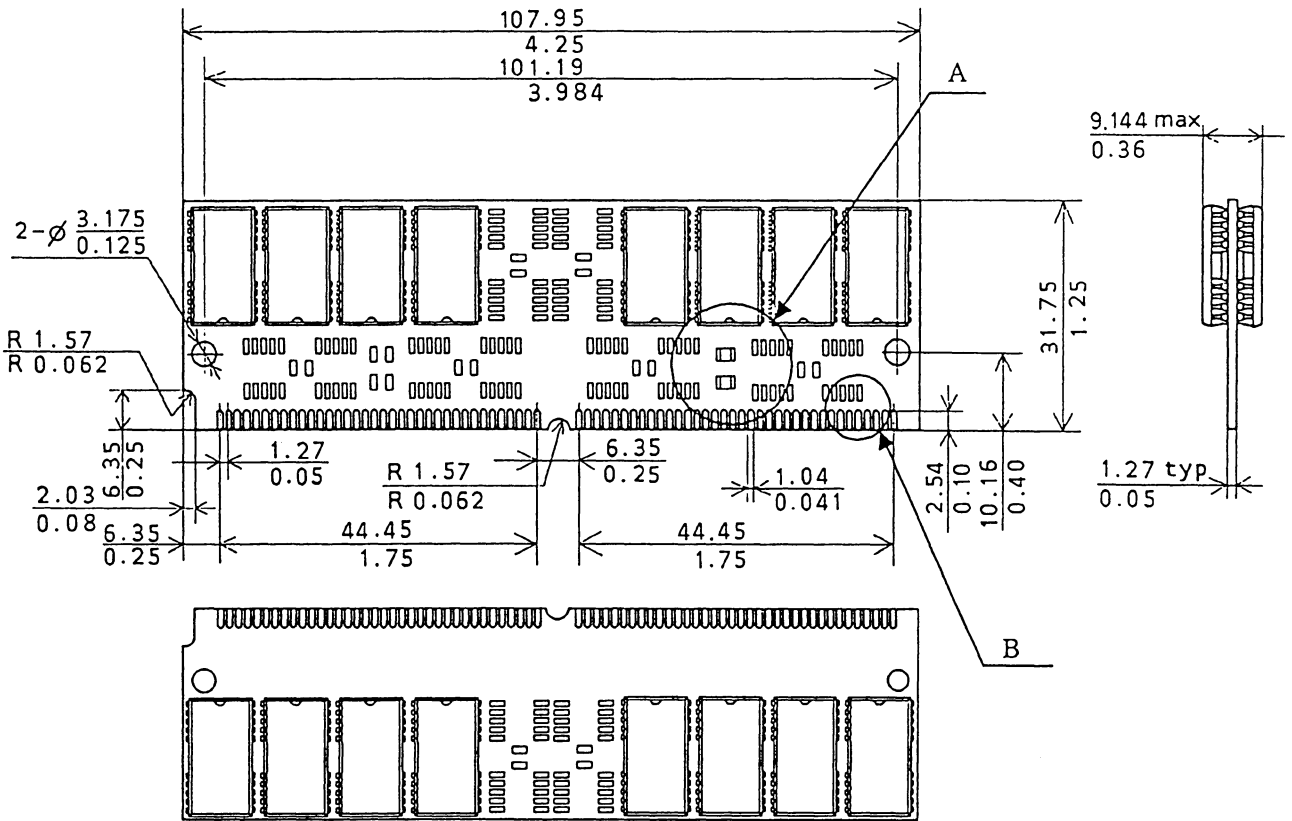
■ Block Diagram



* D0 - D15: HM514400JP

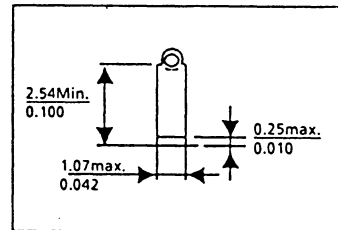
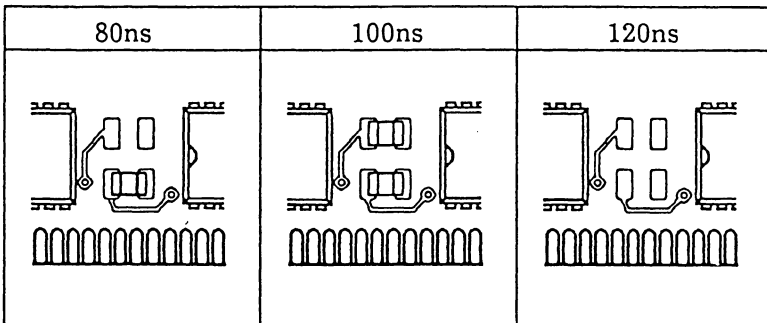
■ Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$



Detail A

Detail B



Note : The plating of the contact finger is gold.

Rev.0
Nov. 15, 1989

HB56D232B-8F

2,097,152-Word × 32-Bit High Density Dynamic RAM Module

Description

The HB56D232B is a 2M × 32 dynamic RAM module, mounted 16 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package. An outline of the HB56D232B is 72-pin single in-line package. Therefore, the HB56D232B makes high density mounting possible without surface mount technology. The HB56D232B provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

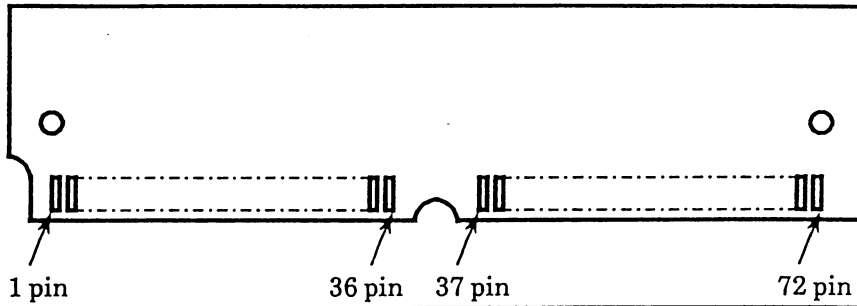
■ Feature

- 72-pin single in-line package
 - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
 - Access time 80ns (max)
- Low power dissipation
 - Active mode 3.99W (max)
 - Standby mode 168mW (max)
- Fast page mode capability
- 1,024refresh cycle / 16ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

■ Ordering information

Part No.	Access time	Package
HB56D232B-8F	80ns	72-pin SIP Socket type

■ Pinout



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{\text{CAS1}}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{\text{RAS1}}$	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	$\overline{\text{RAS3}}$	51	DQ9	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

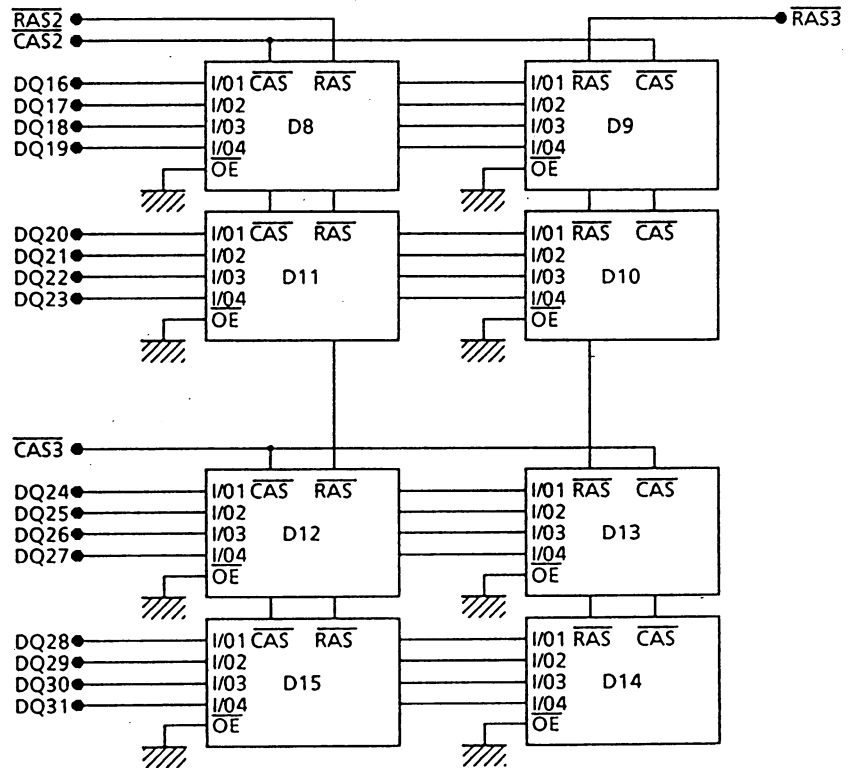
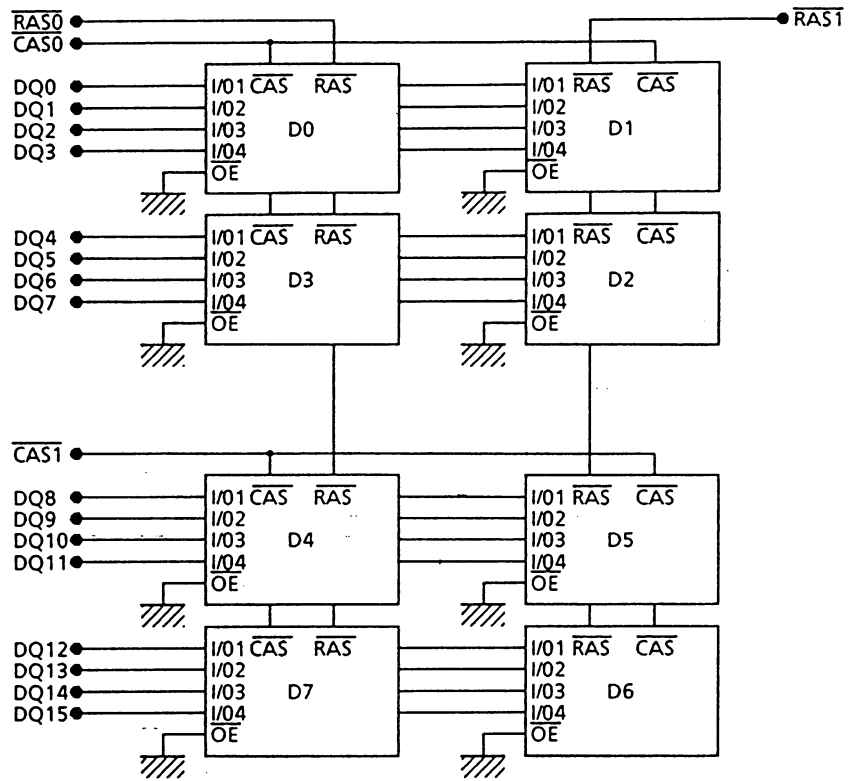
■ Pin Description

Pin Name	Function
A0 – A9	Address Input
A0 – A9	Refresh Address Input
DQ0 – DQ31	Data-in / Data-out
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}} - \overline{\text{RAS3}}$	Row Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
PD1 – PD4	Presence Detect Pin
NC	No connection

■ Presence Detect Pinout

Pin No.	Pin Name	HB56D232B-8F
67	PD1	NC
68	PD2	NC
69	PD3	NC
70	PD4	V _{SS}

Block Diagram



A0 - A9 → D0 - D15

\overline{WE} → D0 - D15

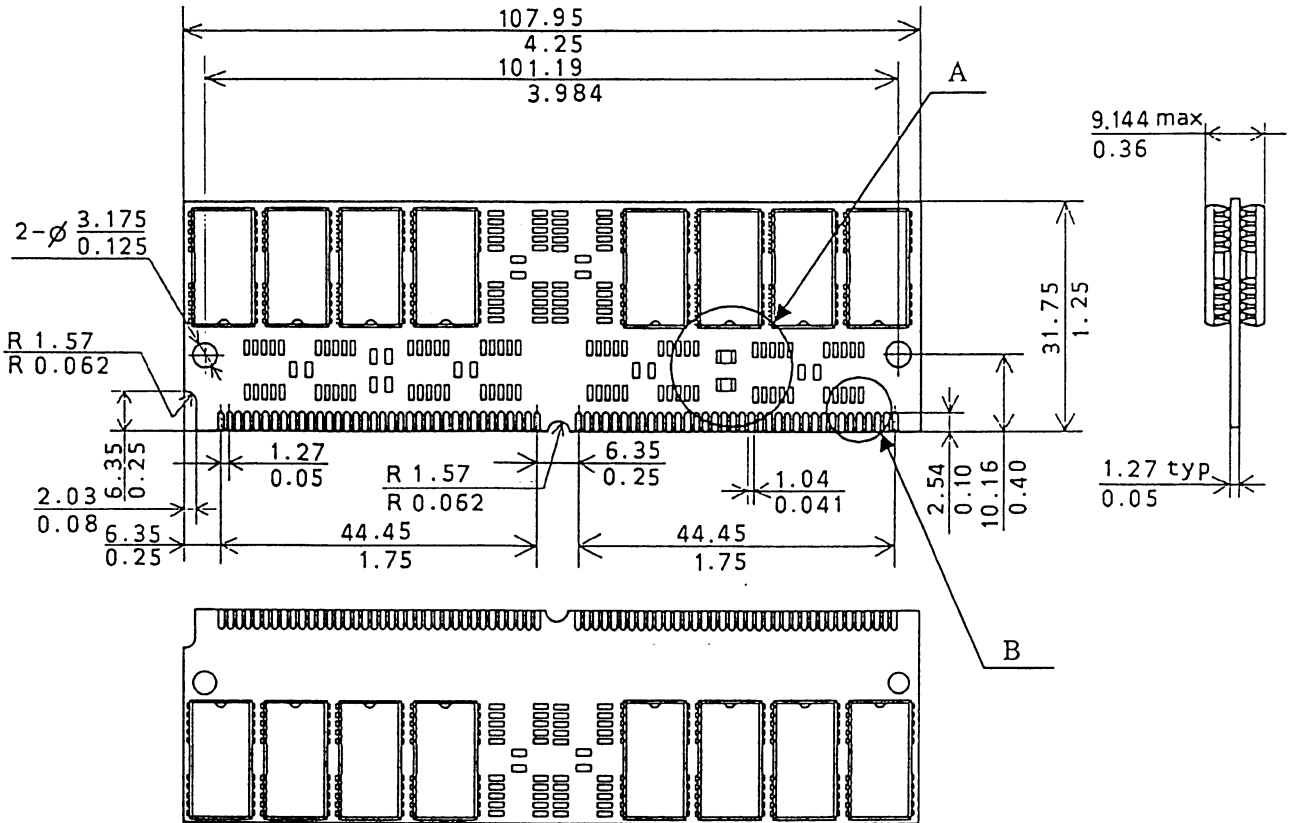
Vcc → D0 - D15

Vss → D0 - D15

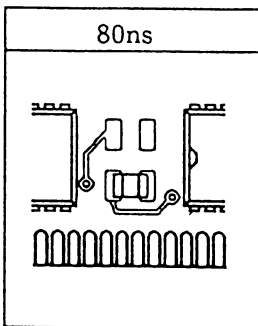
* D0 - D15: HM514400JP

■ Physical Outline

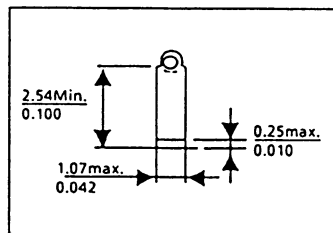
Unit : $\frac{\text{mm}}{\text{inch}}$



Detail A

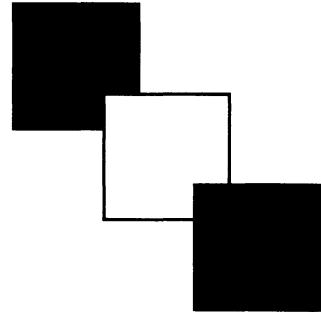


Detail B



Note : The plating of the contact finger is gold.

Rev.1
Jul. 10, 1989



HB56D136B-8/10/12

1,048,576-Word × 36-Bit High Density Dynamic RAM Module

Description

The HB56D136B is a 1M × 36 dynamic RAM module, mounted 8 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package and 4 pieces of 1Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56D136B is 72-pin single in-line package. Therefore, the HB56D136B makes high density mounting possible without surface mount technology. The HB56D136B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

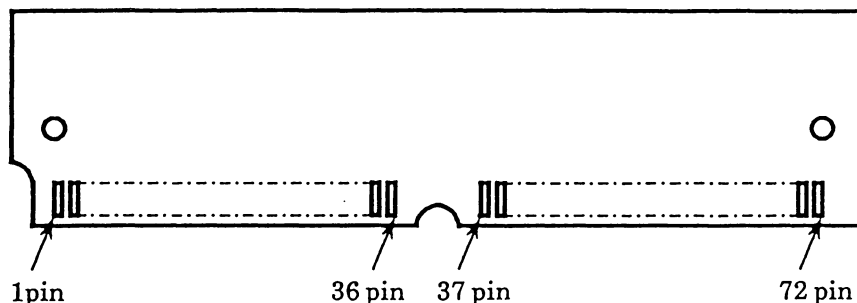
■ Feature

- 72-pin single in-line package
 - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
 - Access time 80ns / 100ns / 120ns (max)
- Low power dissipation
 - Active mode 5.25W / 4.62W / 3.99W (max)
 - Standby mode 126mW (max)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

■ Ordering Information

Part No.	Access time	Package
HB56D136B-8	80ns	72-pin SIP socket type
HB56D136B-10	100ns	
HB56D136B-12	120ns	

■ Pinout



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V _{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V _{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V _{SS}

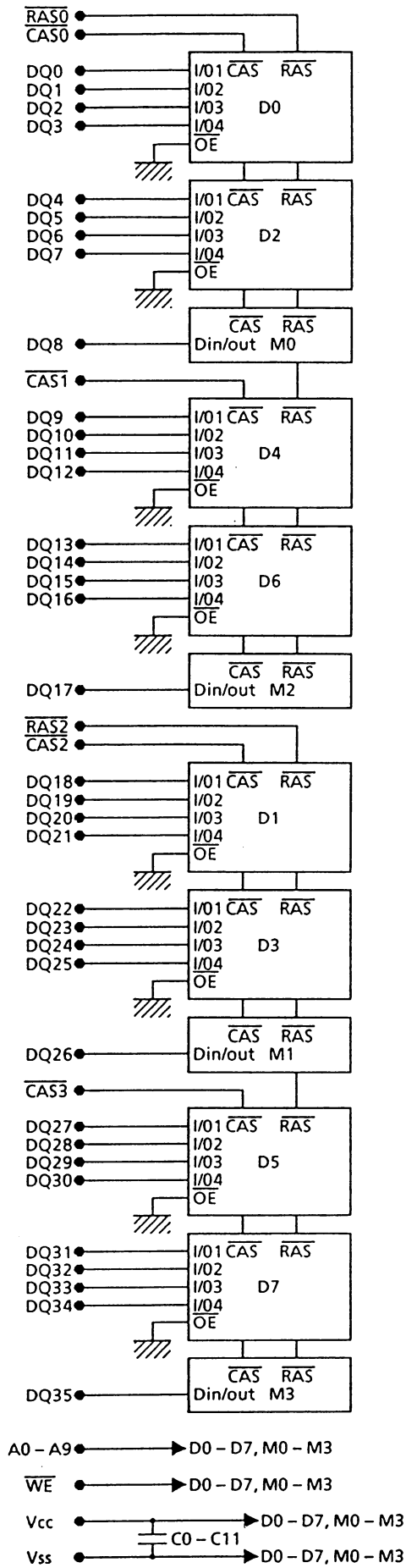
■ Pin Description

Pin Name	Function
A0 – A9	Address Input
A0 – A9	Refresh Address Input
DQ0 – DQ35	Data-in / Data-out
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
PD1 – PD4	Presence Detect Pin
NC	No connection

■ Presence Detect Pinout

Pin No.	Pin Name	HB56D136B		
		80ns	100ns	120ns
67	PD1	V _{SS}	V _{SS}	V _{SS}
68	PD2	V _{SS}	V _{SS}	V _{SS}
69	PD3	NC	V _{SS}	NC
70	PD4	V _{SS}	V _{SS}	NC

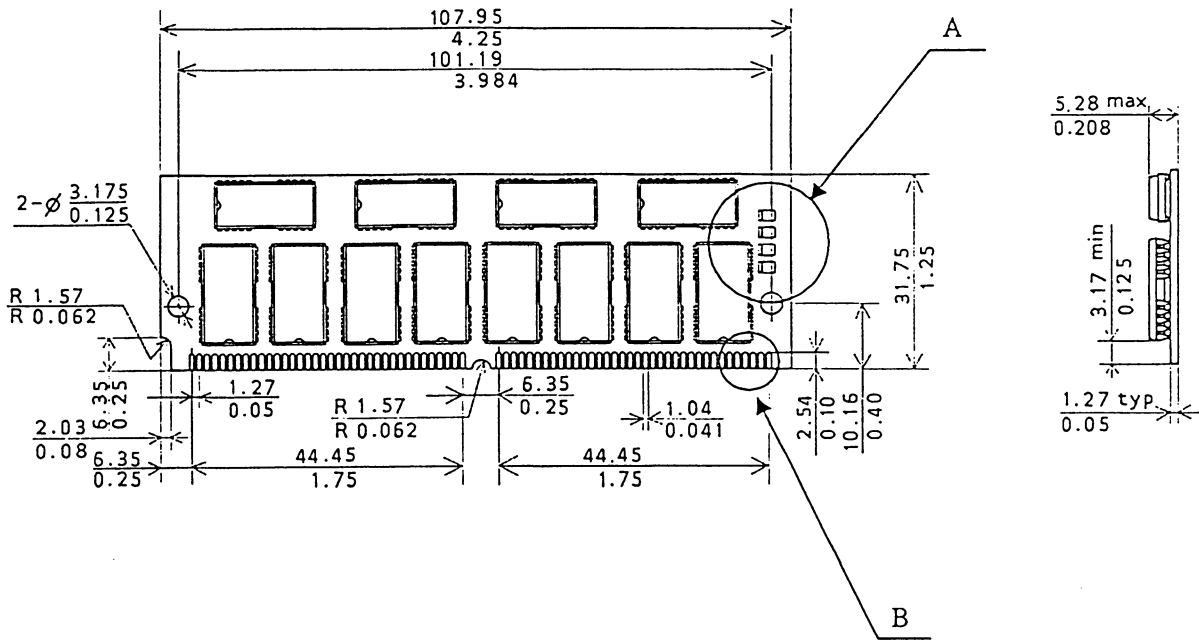
■ Block Diagram



* D0 - D7 : HM514400JP
M0 - M3 : HM511000JP

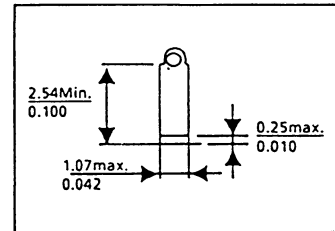
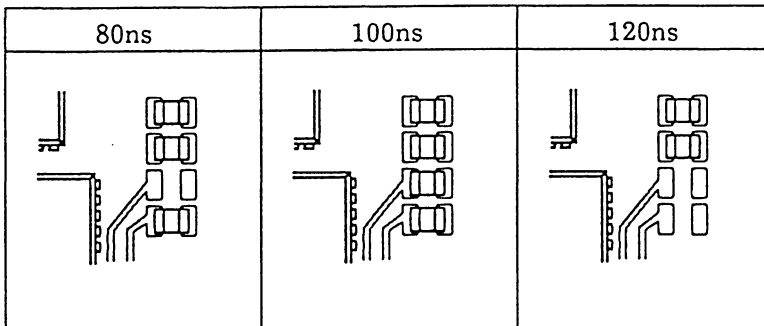
■ Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$

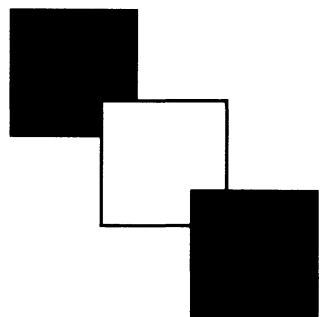


Detail A

Detail B



Note : The plating of the contact finger is gold.



HB56D136BR-8/10/12

1,048,576-Word × 36-Bit High Density Dynamic RAM Module

Description

The HB56D136BR is a 1M×36 dynamic RAM module, mounted 8 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package and 4 pieces of 1Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56D136BR is 72-pin single in-line package. Therefore, the HB56D136BR makes high density mounting possible without surface mount technology. The HB56D136BR provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

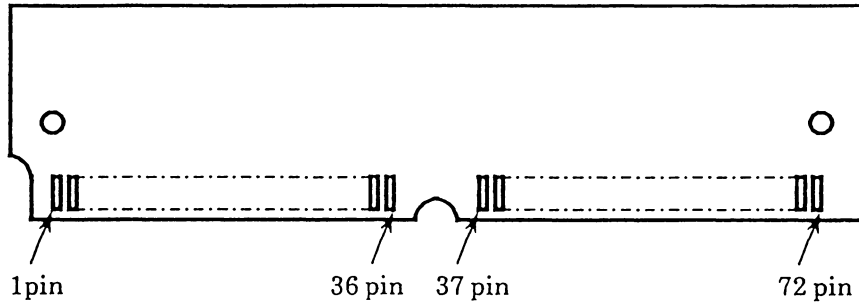
■ Feature

- 72-pin single in-line package
 - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
 - Access time 80ns / 100ns / 120ns (max)
- Low power dissipation
 - Active mode 5.25W / 4.62W / 3.99W (max)
 - Standby mode 126mW (max)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

■ Ordering Information

Part No.	Access time	Package
HB56D136BR-8	80ns	72-pin SIP socket type
HB56D136BR-10	100ns	
HB56D136BR-12	120ns	

■ Pinout



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V _{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V _{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V _{SS}

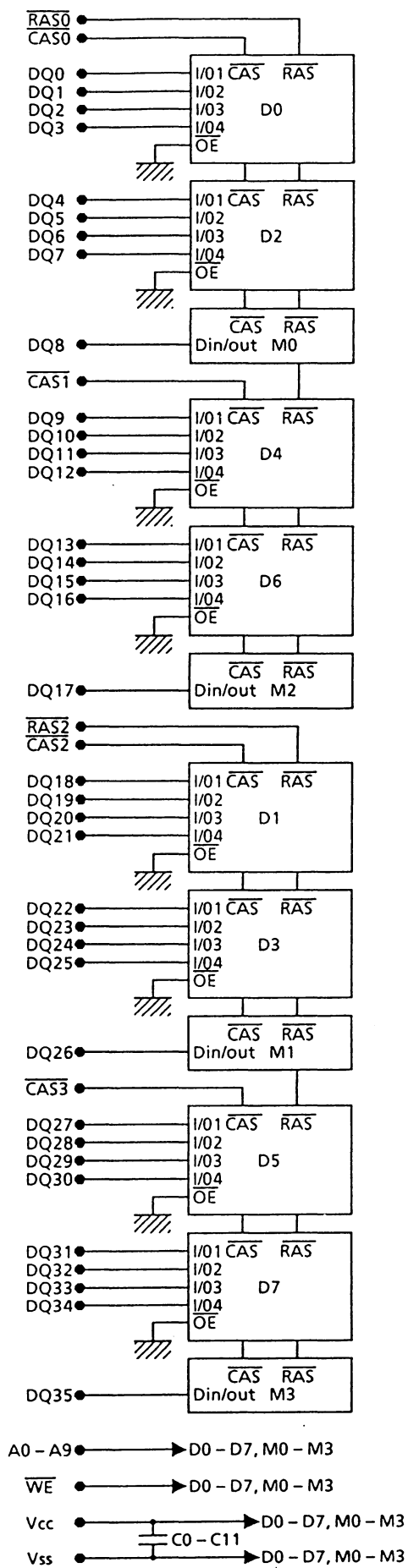
■ Pin Description

Pin Name	Function
A0 – A9	Address Input
A0 – A9	Refresh Address Input
DQ0 – DQ35	Data-in / Data-out
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
PD1 – PD4	Presence Detect Pin
NC	No connection

■ Presence Detect Pinout

Pin No.	Pin Name	HB56D136BR		
		80ns	100ns	120ns
67	PD1	V _{SS}	V _{SS}	V _{SS}
68	PD2	V _{SS}	V _{SS}	V _{SS}
69	PD3	NC	V _{SS}	NC
70	PD4	V _{SS}	V _{SS}	NC

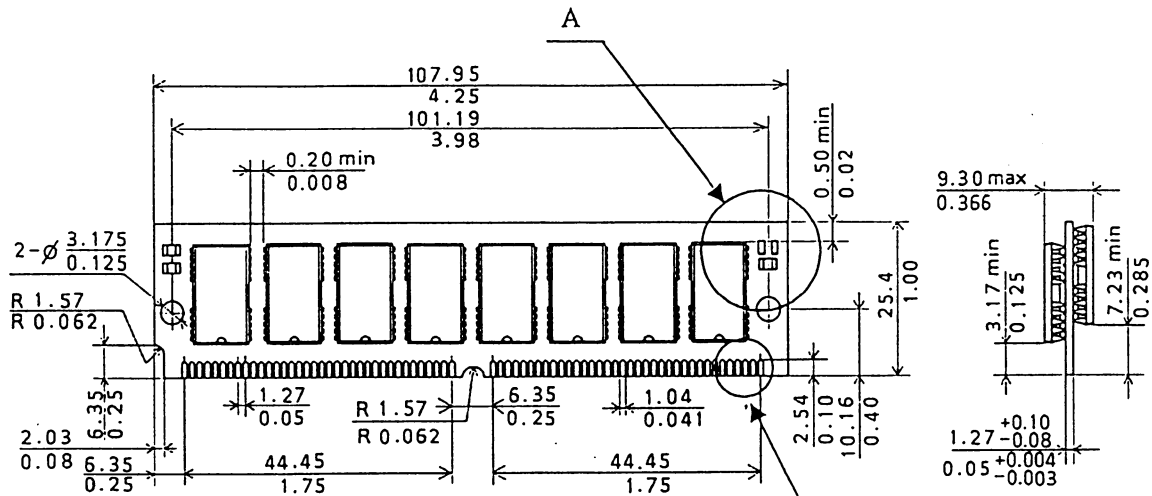
■ Block Diagram



* D0 - D7 : HM514400JP
 M0 - M3 : HM511000JP

Physical Outline

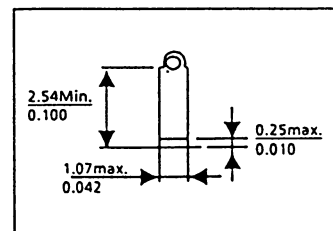
Unit: $\frac{\text{mm}}{\text{inch}}$



Detail A

Detail B

80ns	100ns	120ns



Note : The plating of the contact finger is gold.

Rev.0
Dec. 12, 1989

HB56D136BR-8F

1,048,576-Word × 36-Bit High Density Dynamic RAM Module

Description

The HB56D136BR is a 1M × 36 dynamic RAM module, mounted 8 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package and 4 pieces of 1Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56D136BR is 72-pin single in-line package. Therefore, the HB56D136BR makes high density mounting possible without surface mount technology. The HB56D136BR provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

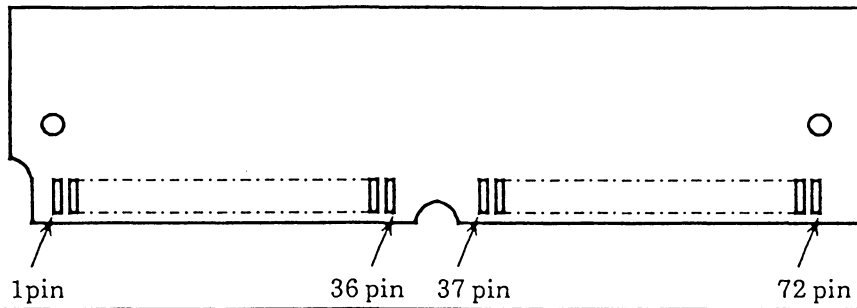
■ Feature

- 72-pin single in-line package
 - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
 - Access time 80ns (max)
- Low power dissipation
 - Active mode 5.25W (max)
 - Standby mode 126mW (max)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

■ Ordering information

Part No.	Access time	Package
HB56D136BR-8F	80ns	72-pin SIP Socket type

■ Pin Out



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V _{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V _{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V _{SS}

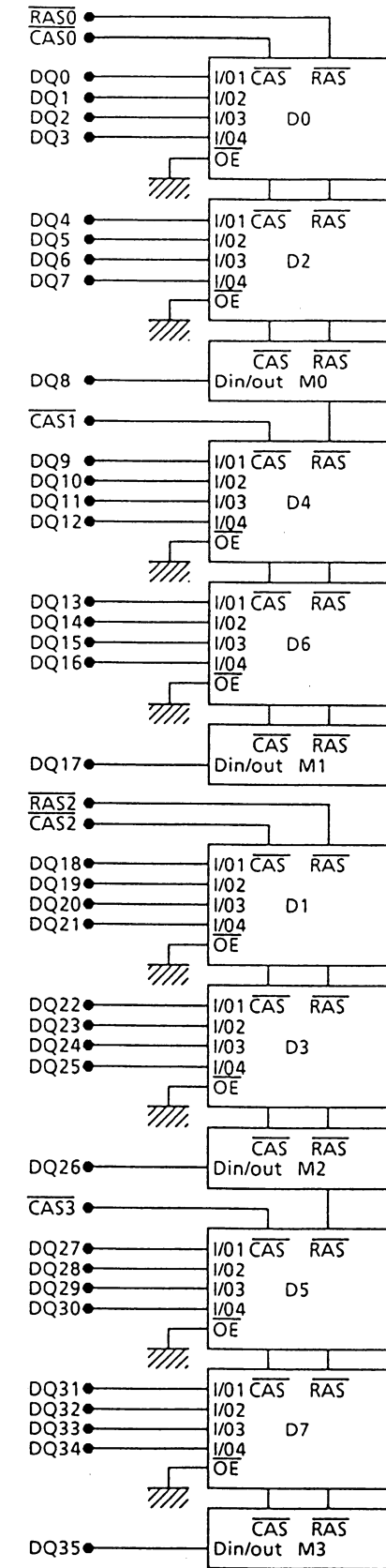
■ Pin Description

Pin Name	Function
A0~A9	Address Input
A0~A9	Refresh Address Input
DQ0~DQ35	Data-in / Data-out
$\overline{\text{CAS0}}\sim\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}},\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
PD1~PD4	Presence Detect Pin
NC	Non-connection

■ Presence Detect Pin Out

Pin No.	Pin Name	HB56D136B-8F
67	PD1	V _{SS}
68	PD2	V _{SS}
69	PD3	NC
70	PD4	V _{SS}

■ Block Diagram



A0~A9 → D0~D7, M0~M3

\overline{WE} → D0~D7, M0~M3

* D0~D7 : HM514400JP

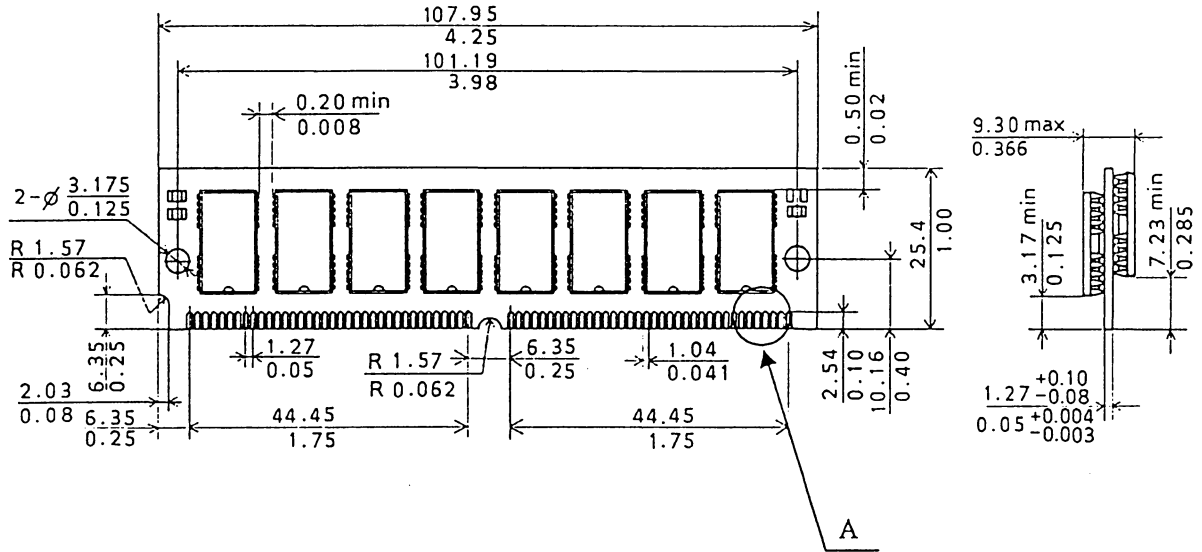
M0~M3 : HM511000JP

Vcc → D0~D7, M0~M3

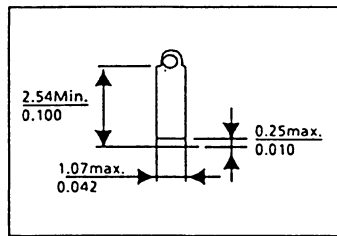
Vss → D0~D7, M0~M3

Physical Outline

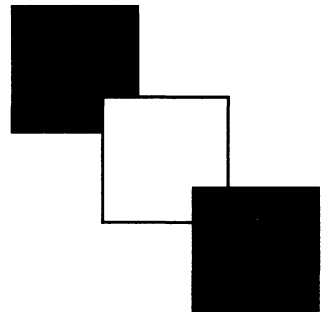
Unit: $\frac{\text{mm}}{\text{inch}}$



Detail A



Note : The plating of the contact finger is gold.



HB56D236B-8/10/12

2,097,152-Word × 36-Bit High Density Dynamic RAM Module

Description

The HB56D236B is a 2M×36 dynamic RAM module, mounted 16 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package and 8 pieces of 1Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56D236B is 72-pin single in-line package. Therefore, the HB56D236B makes high density mounting possible without surface mount technology. The HB56D236B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

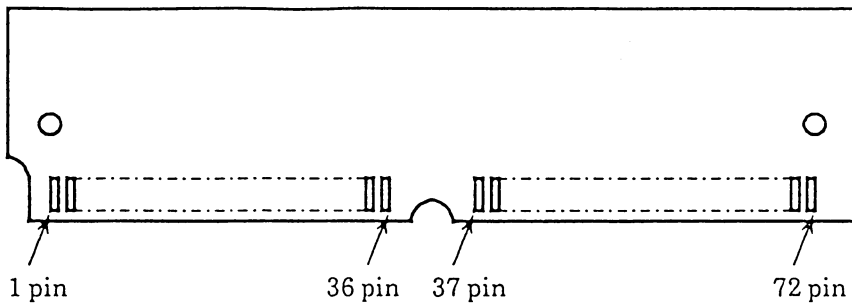
■ Feature

- 72-pin single in-line package
 - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
 - Access time 80ns / 100ns / 120ns (max)
- Low power dissipation
 - Active mode 5.57W / 4.94W / 4.31W (max)
 - Standby mode 252mW (max)
- Fast page mode capability
- 1,024 refresh cycle / 16ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - CAS before $\overline{\text{RAS}}$ refresh
- TTL compatible

■ Ordering information

Part No.	Access time	Package
HB56D236B-8	80ns	72-pin SIP Socket type
HB56D236B-10	100ns	
HB56D236B-12	120ns	

■ Pin Out



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V _{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{\text{RAS1}}$	63	DQ15
10	V _{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	$\overline{\text{RAS3}}$	51	DQ10	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V _{SS}

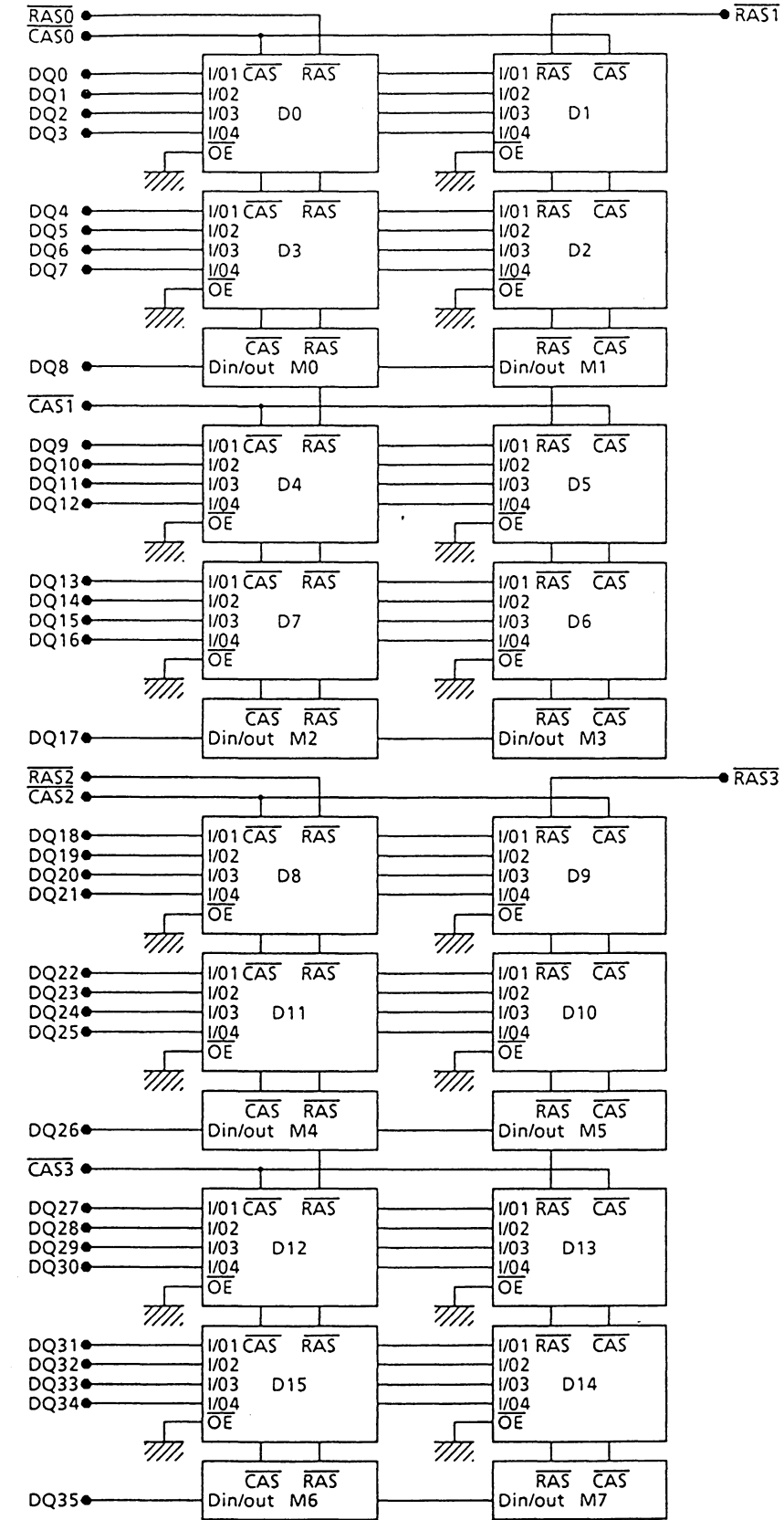
■ Pin Description

Pin Name	Function
A0~A9	Address Input
A0~A9	Refresh Address Input
DQ0~DQ35	Data-in / Data-out
$\overline{\text{CAS0}}\sim\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{RAS0}}\sim\overline{\text{RAS3}}$	Row Address Strobe
$\overline{\text{WE}}$	Read / Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
PD1~PD4	Presence Detect Pin
NC	Nonconnection

■ Presence Detect Pin Out

Pin No.	Pin Name	HB56D236B		
		80ns	100ns	120ns
67	PD1	NC	NC	NC
68	PD2	NC	NC	NC
69	PD3	NC	V _{SS}	NC
70	PD4	V _{SS}	V _{SS}	NC

■ Block Diagram



A0~A9 → D0~D15, M0~M7

\overline{WE} → D0~D15, M0~M7

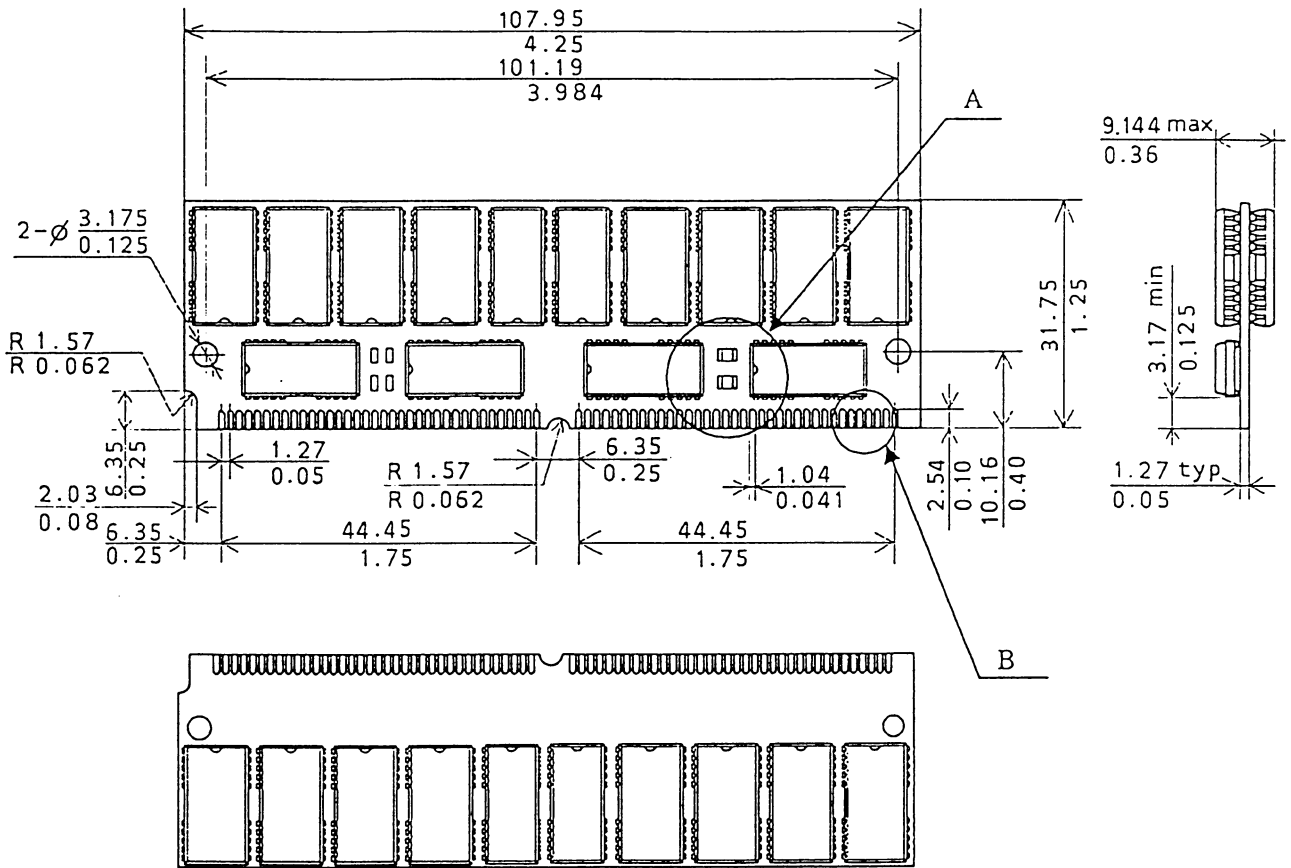
Vcc → D0~D15, M0~M7

Vss → D0~D15, M0~M7

* D0~D15 : HM514400JP
M0~M7 : HM511000JP

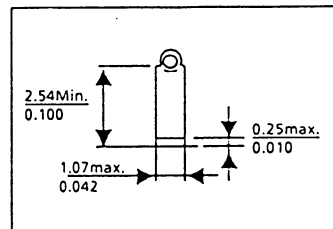
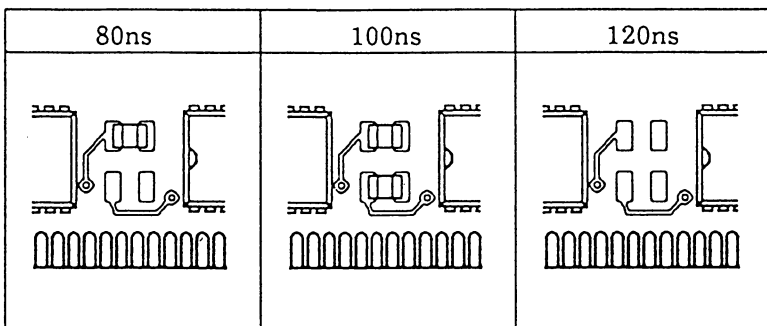
■ Physical Outline

Unit: $\frac{\text{mm}}{\text{inch}}$



Detail A

Detail B



Note : The plating of the contact finger is gold.

Rev. 6
Jan. 18, 1990

HM628128 Series

131072-Word × 8-Bit High Speed Hi-CMOS Static RAM

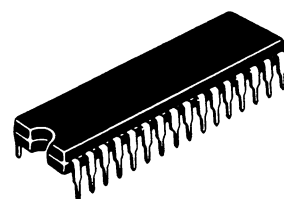
The Hitachi HM628128 is a CMOS static RAM organized 128k-word x 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8μm Hi-CMOS process technology.

It offers low power standby power dissipation, therefore it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460 mil body SOP) or a 600 mil plastic DIP, is available for high density mounting.

Features

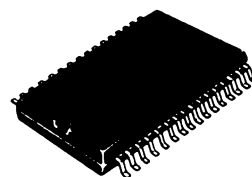
- High speed: Fast Access time 70/85/100/120 ns (max.)
- Low power
Standby: 10 μW (typ.) (L-version)
Operation: 75 mW (typ.)
- Single 5V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output - Three state output
- Directly TTL compatible - All inputs and outputs
- Capability of battery back up operation (L & SL)
2 chip selection for battery back up

HM628128P Series



(DP-32)

HM628128FP Series



(FP-32D)

Pin Arrangement

NC	1	32	VCC
A16	2	31	A15
A14	3	30	CS2
A12	4	29	WE
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CS1
A0	12	21	I/O7
I/O0	13	20	I/O6
I/O1	14	19	I/O5
I/O2	15	18	I/O4
VSS	16	17	I/O3

(Top view)

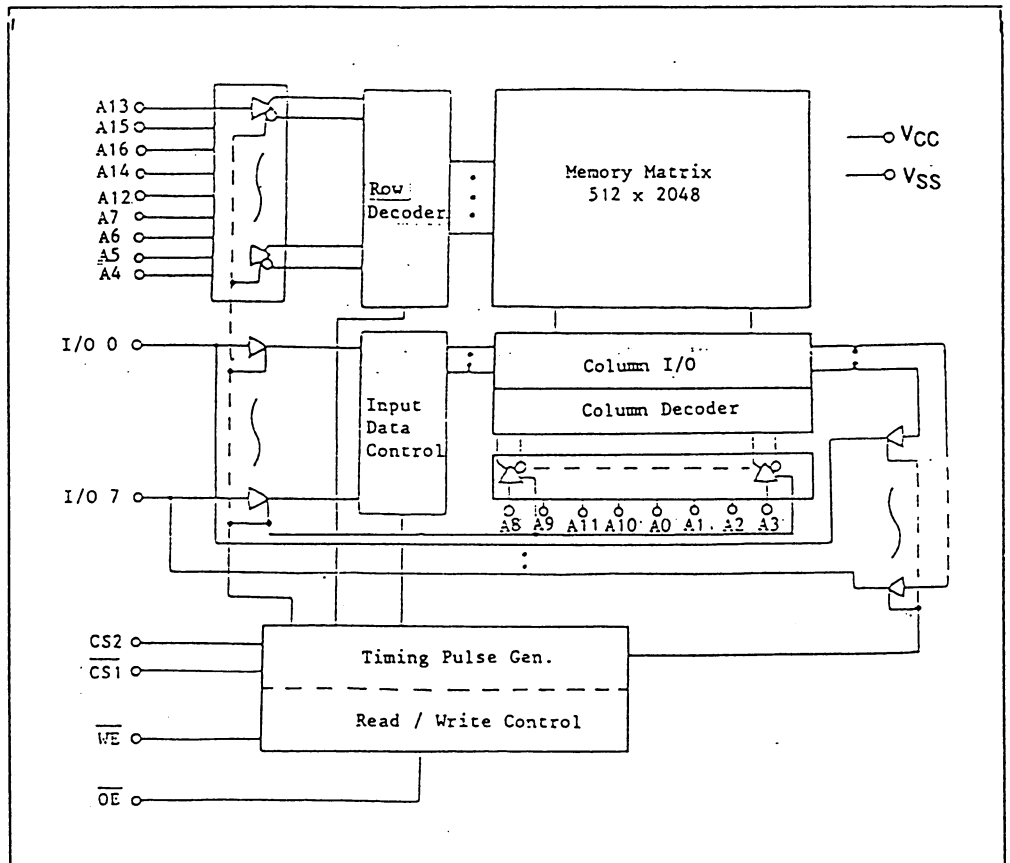
Pin Description

Pin Name	Function
A0 - A16	Address
I/O0 - I/O7	Input/Output
CS1	Chip select
CS2	Chip select
WE	Write enable
OE	Output enable
NC	NO connection
VCC	Power supply
VSS	Ground

Ordering Information

Part No.	Access	Package	Part No.	Access	Package		
HM628128P-7	70ns	600 mil 32 pin Plastic DIP	HM628128LP-7SL	70ns	600 mil 32 pin Plastic DIP		
HM628128P-8	85ns		HM628128LP-8SL	85ns			
HM628128P-10	100ns		HM628128LP-10SL	100ns			
HM628128P-12	120ns		HM628128LP-12SL	120ns			
HM628128LP-7	70ns						
HM628128LP-8	85ns						
HM628128LP-10	100ns						
HM628128LP-12	120ns						
HM628128FP-7	70ns		525 mil 32 pin Plastic SOP	HM628128LFP-7SL		70ns	525 mil 32 pin Plastic SOP
HM628128FP-8	85ns			HM628128LFP-8SL		85ns	
HM628128FP-10	100ns			HM628128LFP-10SL		100ns	
HM628128FP-12	120ns			HM628128LFP-12SL		120ns	
HM628128LFP-7	70ns						
HM628128LFP-8	85ns						
HM628128LFP-10	100ns						
HM628128LFP-12	120ns						

Block Diagram



DC Characteristics (Ta = 0 to +70°C, VCC = 5 V ± 10 %, VSS = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	I _{LI}	-	-	2	µA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	-	-	2	µA	$\overline{CS1} = V_{IH}$ or $\overline{CS2} = V_{IL}$, OE = V _{IH} or WE = V _{IL} , V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	ICC	-	15	35	mA	$\overline{CS1} = V_{IL}$, CS2 = V _{IH} , others = V _{IH} /V _{IL} I _{I/O} = 0 mA
Operating power supply current	ICC1	-	45	70	mA	Min. cycle, duty=100%, CS1 = V _{IL} , CS2 = V _{IH} , others = V _{IH} /V _{IL} I _{I/O} = 0 mA
	ICC2	-	15	30	mA	Cycle time = 1µs, duty = 100%, I _{I/O} = 0 mA CS1 ≤ 0.2V, CS2 ≥ V _{CC} - 0.2V V _{IH} ≥ V _{CC} - 0.2V, V _{IL} ≤ 0.2V
Standby VCC current: DC	ISB	-	1	3	mA	$\overline{CS1} = V_{IH}$, CS2 = V _{IH} or CS2 = V _{IL}
Standby VCC current (1): DC	ISB1	-	0.02	2	mA	V _{in} ≥ 0 V CS1 ≥ V _{CC} - 0.2 V, CS2 ≥ V _{CC} - 0.2 V or
		-	2*2	100*2	µA	0 V ≤ CS2 ≤ 0.2 V
		-	2*3	50*3	µA	
Output low voltage	VOL	-	-	0.4	V	I _{OL} = 2.1 mA
Output high voltage	VOH	2.4	-	-	V	I _{OH} = -1.0 mA

- Note: 1. Typical values are at Vcc=5.0V, Ta=+25°C and specified loading.
 2. This characteristics is guaranteed only for L-version.
 3. This characteristics is guaranteed only for SL-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C _{in}	-	-	8	pF	V _{in} = 0 V
Input/output capacitance	C _{I/O}	-	-	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100 % tested.

Rev. 3
April 9, 1990

HM628128 TSOP Series

131,072-Word × 8-Bit High Speed Hi-CMOS Static RAM

The Hitachi HM628128 is a CMOS static RAM organized 128k-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8μm Hi-CMOS process technology.

It offers low power standby power dissipation, therefore it is suitable for battery back-up systems.

The device, packaged in a 8mm × 20mm TSOP is available for high density mounting.

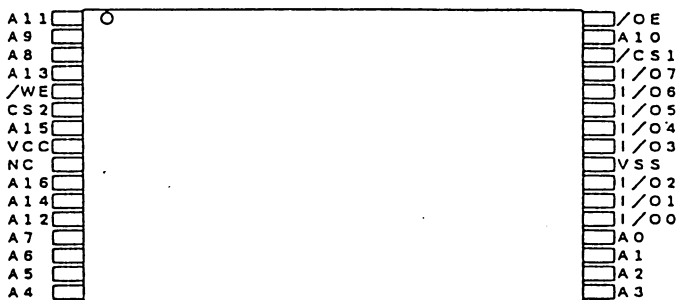
Features

- High speed: Fast Access time 70/85/100/120 ns (max.)
- Low power
Standby: 10 μW (typ.) (L/L-xxL version)
Operation: 75 mW (typ.)
- Single 5V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output - Three state output
- Directly TTL compatible - All inputs and outputs
- Capability of battery back up operation (L/L-xxL version)
2 chip selection for battery back up

Pin Description

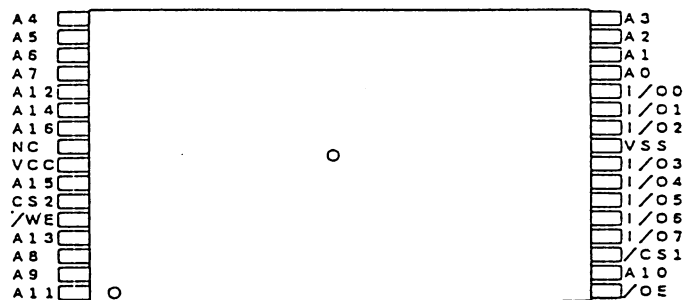
Pin Name	Function
A0 - A16	Address
I/O0 - I/O7	Input/Output
CS1	Chip select
CS2	Chip select
WE	Write enable
OE	Output enable
NC	NO connection
VCC	Power supply
VSS	Ground

Pin Arrangement



(Top View)

(a) Normal Type Pin Arrangement



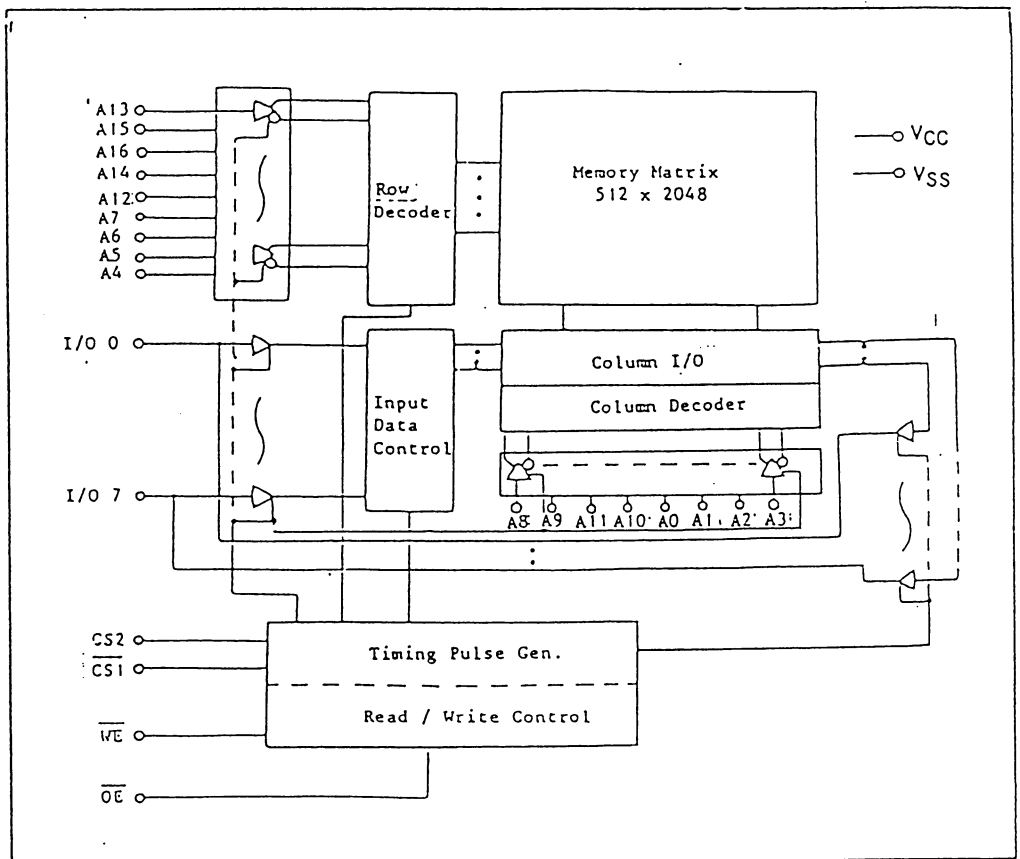
(Top View)

(b) Reverse Type Pin Arrangement

Ordering Information

Part No	Access	Standby Current	Package	Part No	Access	Standby Current	Package
HM628128T-7	70ns	2mA	Normal-Vend	HM628128R-7	70ns	2mA	Reverse Vend
HM628128T-8	85ns	2mA		HM628128R-8	85ns	2mA	
HM628128T-10	100ns	2mA		HM628128R-10	100ns	2mA	
HM628128T-12	120ns	2mA		HM628128R-12	120ns	2mA	
HM628128LT-7	70ns	100 μ A	Type	HM628128LR-7	70ns	100 μ A	Type
HM628128LT-8	85ns	100 μ A	32pin	HM628128LR-8	85ns	100 μ A	32pin
HM628128LT-10	100ns	100 μ A	Plastic	HM628128LR-10	100ns	100 μ A	Plastic
HM628128LT-12	120ns	100 μ A	8mm x 20mm	HM628128LR-12	120ns	100 μ A	8mm x 20mm
HM628128LT-7L	70ns	50 μ A	TSOP	HM628128LR-7L	70ns	50 μ A	TSOP
HM628128LT-8L	85ns	50 μ A		HM628128LR-8L	85ns	50 μ A	
HM628128LT-10L	100ns	50 μ A		HM628128LR-10L	100ns	50 μ A	
HM628128LT-12L	120ns	50 μ A		HM628128LR-12L	120ns	50 μ A	

Block Diagram



DC Characteristics (Ta = 0 to +70°C, VCC = 5 V ± 10 %, VSS = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	I _{LI}	-	-	2	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	-	-	2	μA	$\overline{CS1} = V_{IH}$ or $\overline{CS2} = V_{IL}$, OE = V _{IH} or WE = V _{IL} , V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC}	-	15	35	mA	$\overline{CS1} = V_{IL}$, CS2 = V _{IH} , others = V _{IH} /V _{IL} I _{I/O} = 0 mA
Operating power supply current	I _{CC1}	-	45	70	mA	Min. cycle, duty=100%, CS1 = V _{IL} , CS2 = V _{IH} , others = V _{IH} /V _{IL} I _{I/O} = 0 mA
	I _{CC2}	-	15	30	mA	Cycle time = 1μs, duty = 100%, I _{I/O} = 0 mA CS1 ≤ 0.2V, CS2 ≥ V _{CC} - 0.2V V _{IH} ≥ V _{CC} - 0.2V, V _{IL} ≤ 0.2V
Standby V _{CC} current: DC	I _{SB}	-	1	3	mA	$\overline{CS1} = V_{IH}$, CS2 = V _{IH} or CS2 = V _{IL}
Standby V _{CC} current (I): DC	I _{SB1}	-	0.02	2	mA	V _{in} ≥ 0 V
		-	$\frac{2*2 \cdot 100*2}{2*3 \cdot 50*3}$		μA	CS1 ≥ V _{CC} - 0.2 V, CS2 ≥ V _{CC} - 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		-				
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -1.0 mA

Note: *1: Typical values are at V_{CC}=5.0V, Ta=+25°C and specified loading.

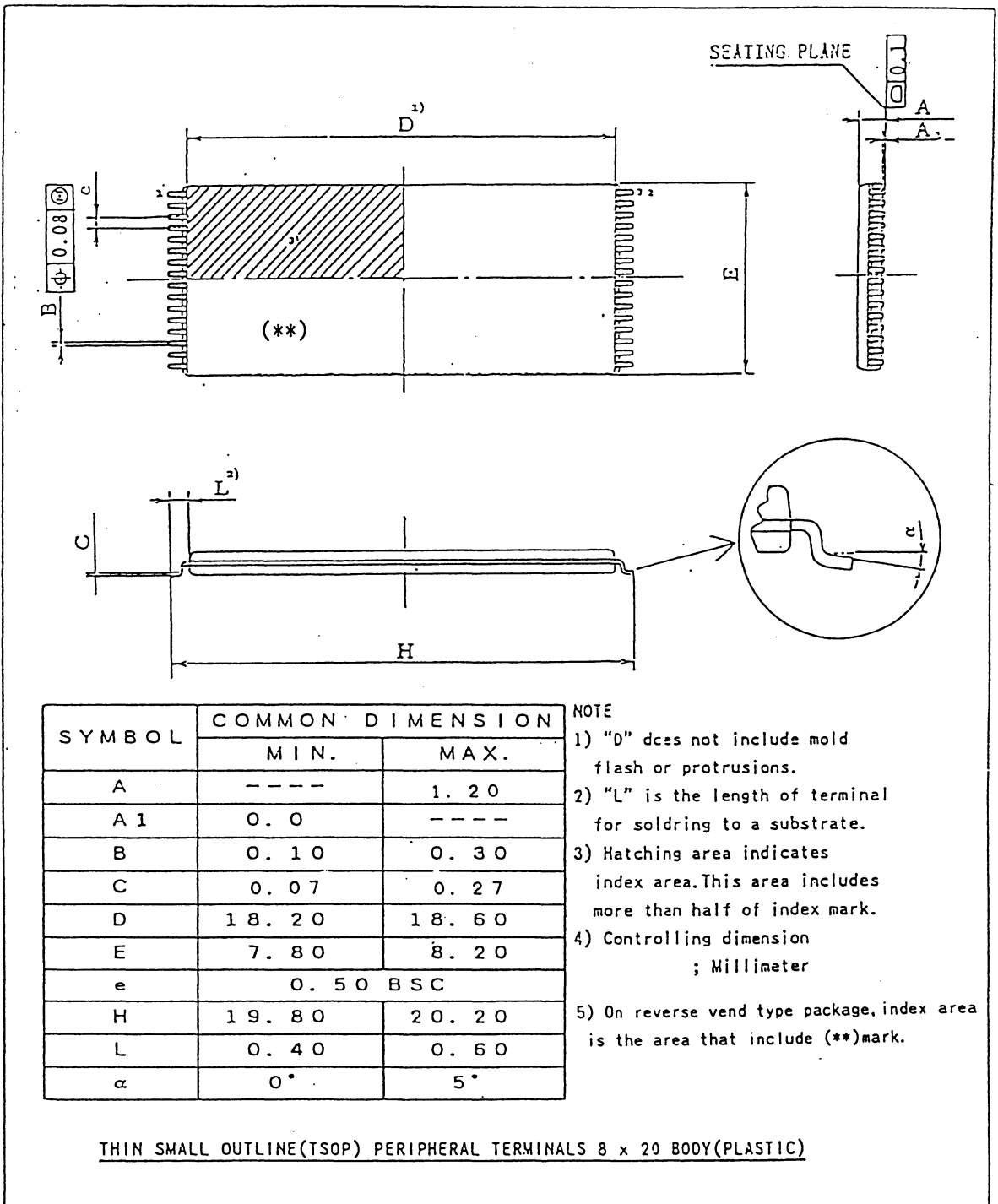
*2: for L-version

*3: for L-xxL version, 13 μA max. at Ta=0 to 40°C.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C _{in}	-	-	8	pF	V _{in} = 0 V
Input/output capacitance	C _{I/O}	-	-	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100 % tested.



Rev. 1, Apr, 20 '90

HM66205L-85/10/12

524,288-Word × 8-Bit High Density CMOS Static RAM Module

The HM66205 is a high density 4M-bit static RAM module consisted of 4 pieces HM628128LTS products (TSOP type 1M static RAM) and a HD74ACT138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66205 is the standard 600 mil width 32 pin dual-inline package. Its pin arrangement is completely compatible with 4M-bit monolithic static RAM.

The HM66205 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66205 makes high density mounting possible with no surface mount technology.

These features make the HM66205 ideally suited for high density compacted memory systems.

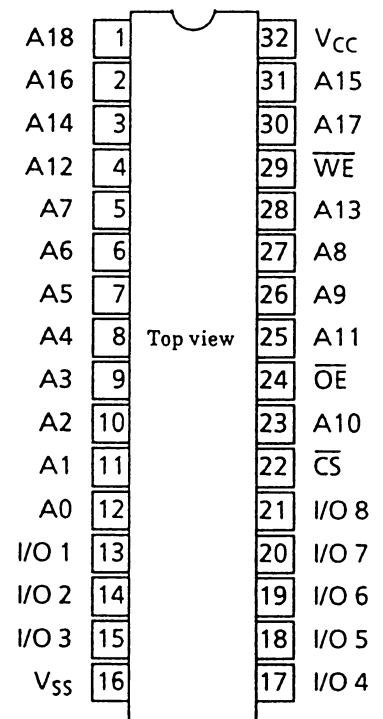
■ Features

- High density 32 pin DIP
 - Mounting 4pcs. of 1M static RAM (TSOP; HM628128LTS) and CMOS decoder logic (SOP; HD74ACT138FP equivalent)
- Pin compatible with 4M monolithic static RAM
- High speed
 - Fast access time 85ns/100ns/120ns (maximum)
- Equal access and cycle time
- Completely static RAM
 - No clock or timing strobe required
- Low Power standby and low power operation
 - Standby 40 μW (typical)
 - Operation 80 mW (typical)
- Common data input and output, three state outputs
- Capable of battery backup operation
- Directry TTL compatible: All inputs and outputs

■ Type of Products

Part No.	Access	Package
HM66205L-85	85ns	600 - mil 32 - pin DIP
HM66205L-10	100ns	
HM66205L-12	120ns	

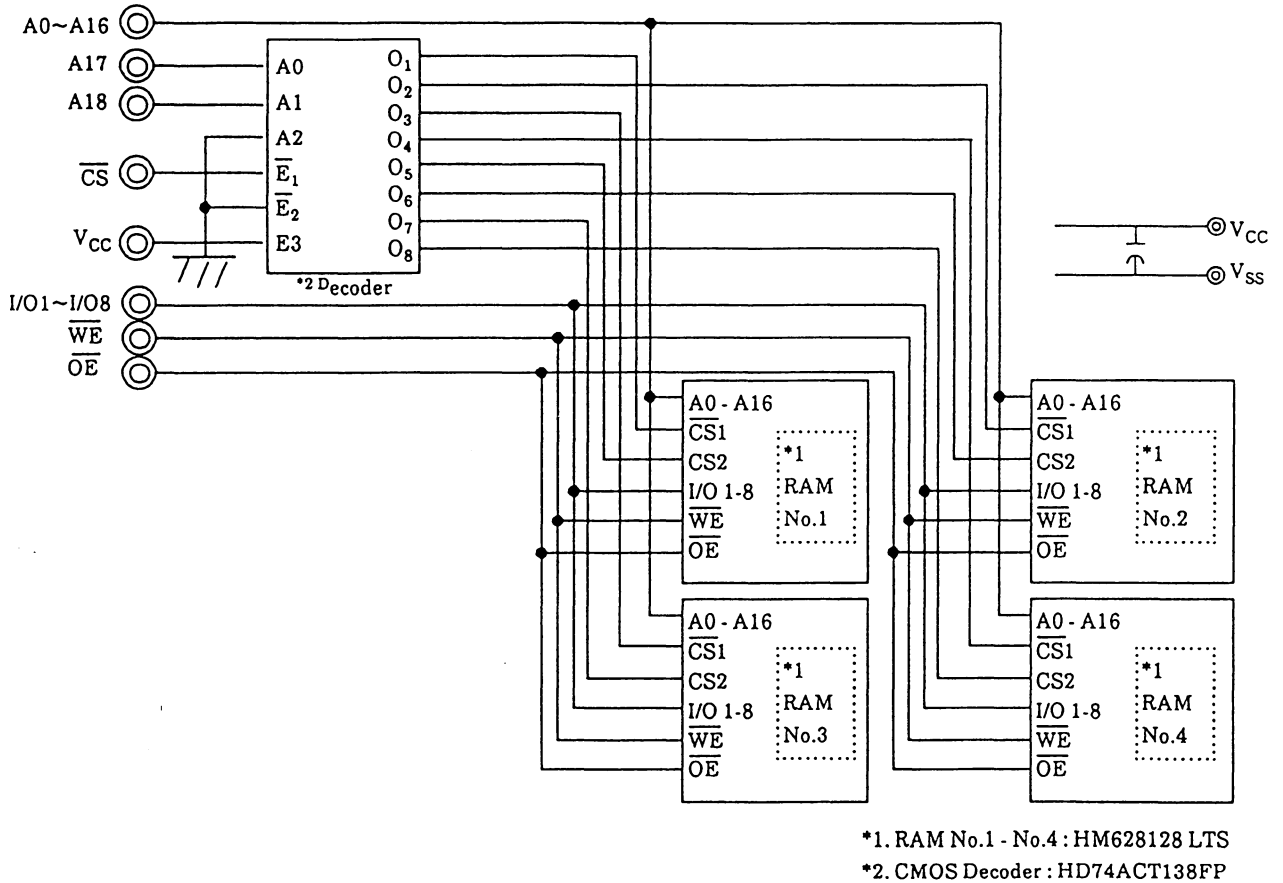
■ Pin Arrangement



■ Pin Description

Pin Name	Function
A0 - A18	Address
I/O1 ~ I/O8	Input / Output
\overline{CS}	Chip Select
\overline{WE}	Write Enable
\overline{OE}	Output Enable
V _{CC}	Power Supply
V _{SS}	Ground

■ Block Diagram



■ Mode Selection

Mode	\overline{CS}	\overline{WE}	\overline{OE}	I/O	Current	Note
Not Selected (Power down)	H	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) - (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

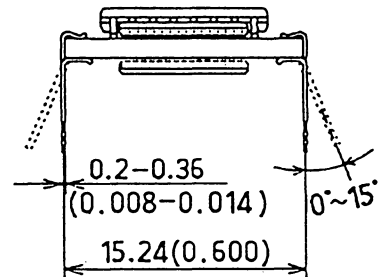
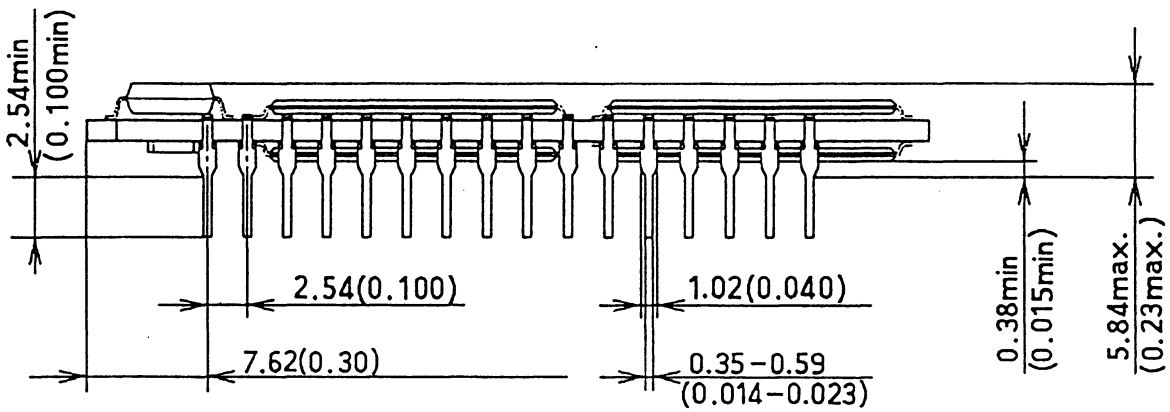
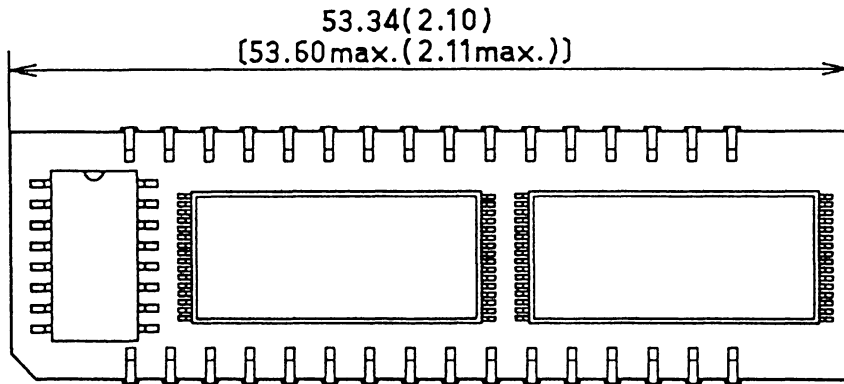
Note : X = Don't care (H or L)

■ Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 ~ +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 ~ +70	°C
Storage temperature range	T_{stg}	-55 ~ +125	°C
Storage temperature range under bias	T_{bias}	-10 ~ +85	°C

■ Package Dimensions

Unit : mm(inch)



Rev. 3 Dec. 1989

HM658512 Series

524,288-Word × 8-Bit High Speed Pseudo Static RAM

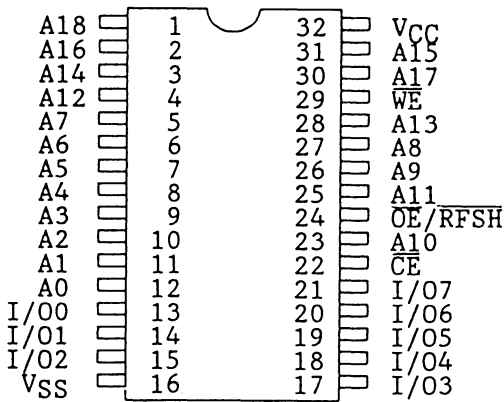
Feature

- Single 5 V (± 10 %)
- High speed
 - Access time
 - CE access time 80/100/120 ns
 - Cycle time
 - Random read/write cycle time...160/180/210 ns
- Low power
 - 250 mW typ. Active
 - 350 μW typ. Standby
- All inputs and outputs TTL compatible
- Package
 - 32-pin dual-in-line plastic package
 - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
 - LP-version...Address refresh DP-version...Address refresh
 - Automatic refresh Automatic refresh
 - Self refresh

Ordering Information

Type No.	Access	Package
HM658512LP-8	80 ns	
HM658512LP-10	100 ns	
HM658512LP-12	120 ns	600 mil
HM658512DP-8	80 ns	32-pin
HM658512DP-10	100 ns	plastic DIP
HM658512DP-12	120 ns	
HM658512LFP-8	80 ns	
HM658512LFP-10	100 ns	
HM658512LFP-12	120 ns	32-pin
HM658512DFP-8	80 ns	plastic
HM658512DFP-10	100 ns	SOP
HM658512DFP-12	120 ns	

Pin Arrangement

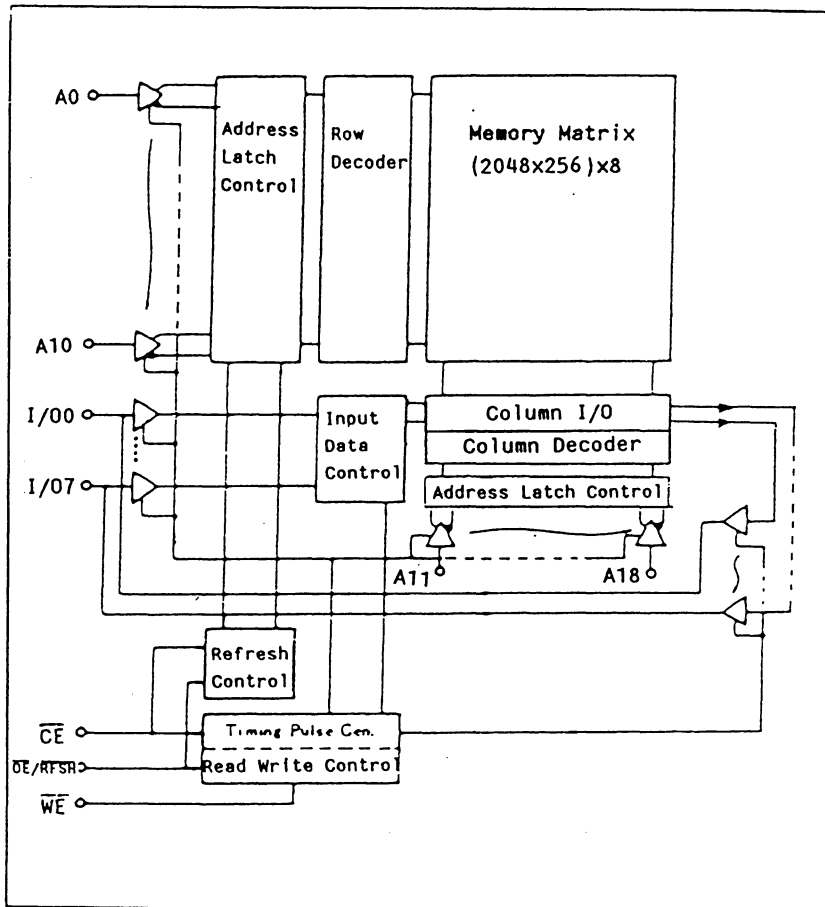


(Top View)

Pin Description

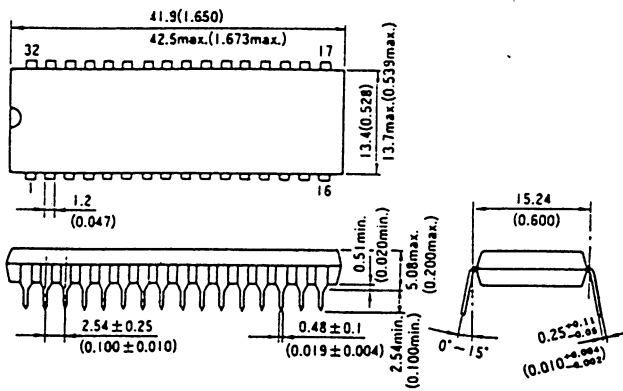
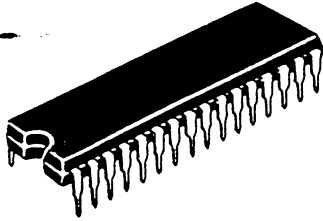
Pin Name	Function
A0 - A18	Address
I/O0 - I/O7	Input/output
\overline{CE}	Chip enable
$\overline{OE/RFSH}$	Output enable/Refresh
\overline{WE}	Write enable
VCC	Power supply
VSS	Ground

Block Diagram



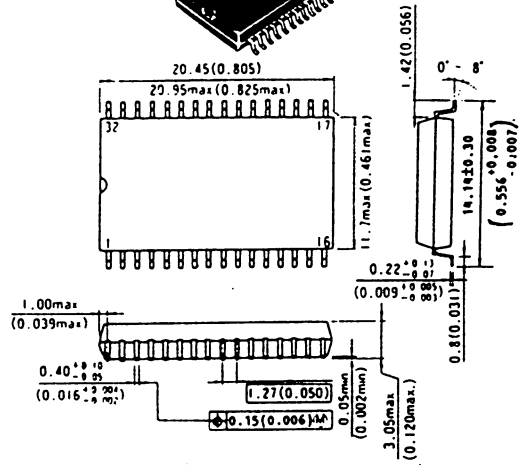
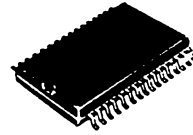
Package Dimensions, Unit: mm (inch)
HM658512P Series

DP-32



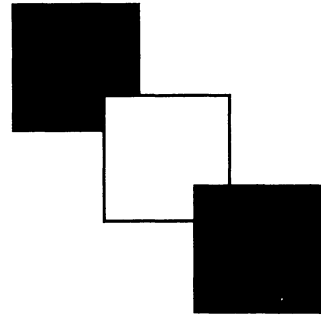
HM658512FP Series

FP-32D



HN27C4096 Series

262,144-Word × 16-Bit CMOS UV ERasable and Programmable ROM



The Hitachi HN27C4096G/CC is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation. Fabricated on advanced fine process and high speed circuitry technique, the HN27C4096 makes high speed access time possible. Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 80286 and 68020. The HN27C4096 offers high speed programming using page programming mode. This device has the package variation of cerdip-40pin and JLCC-44pin.

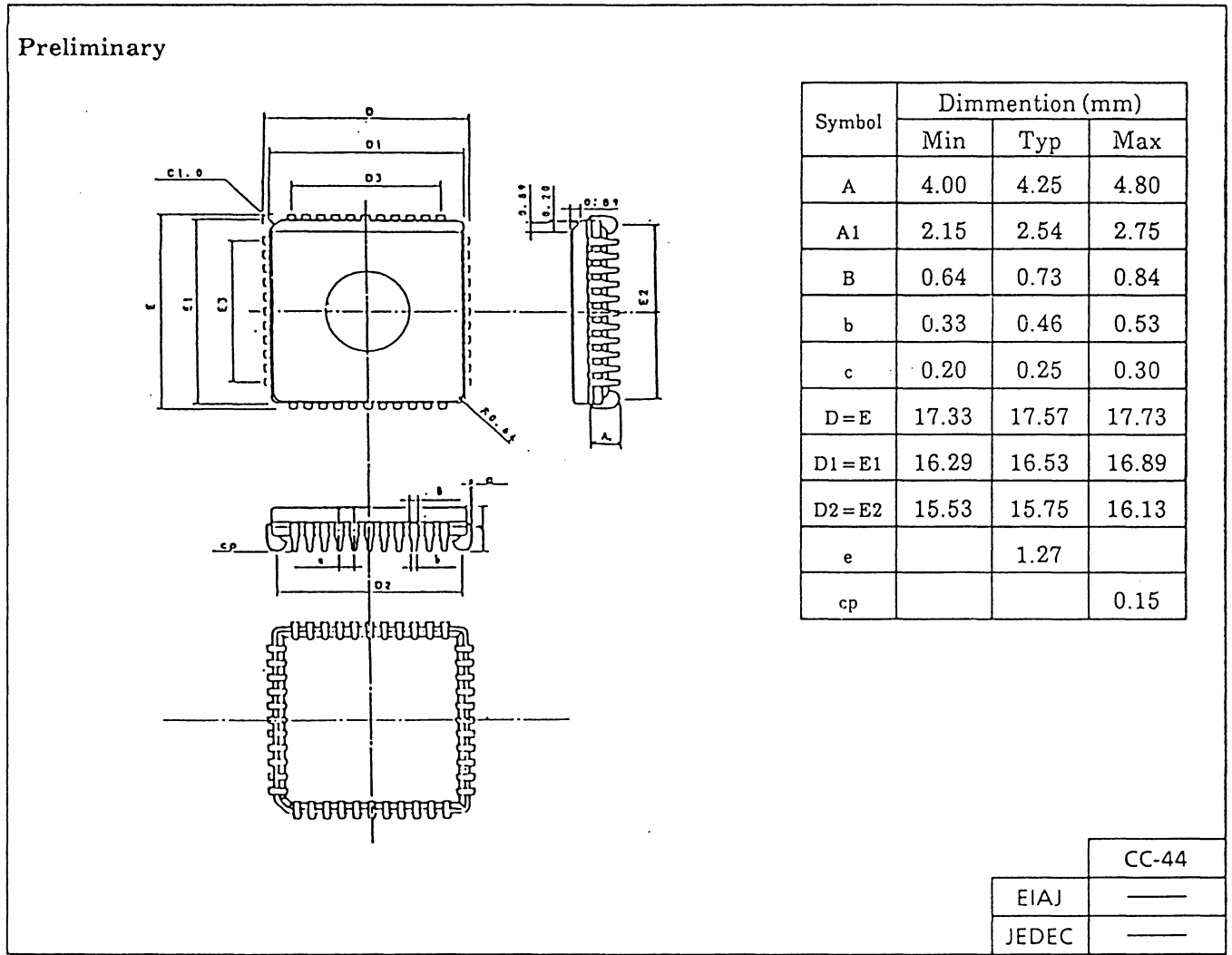
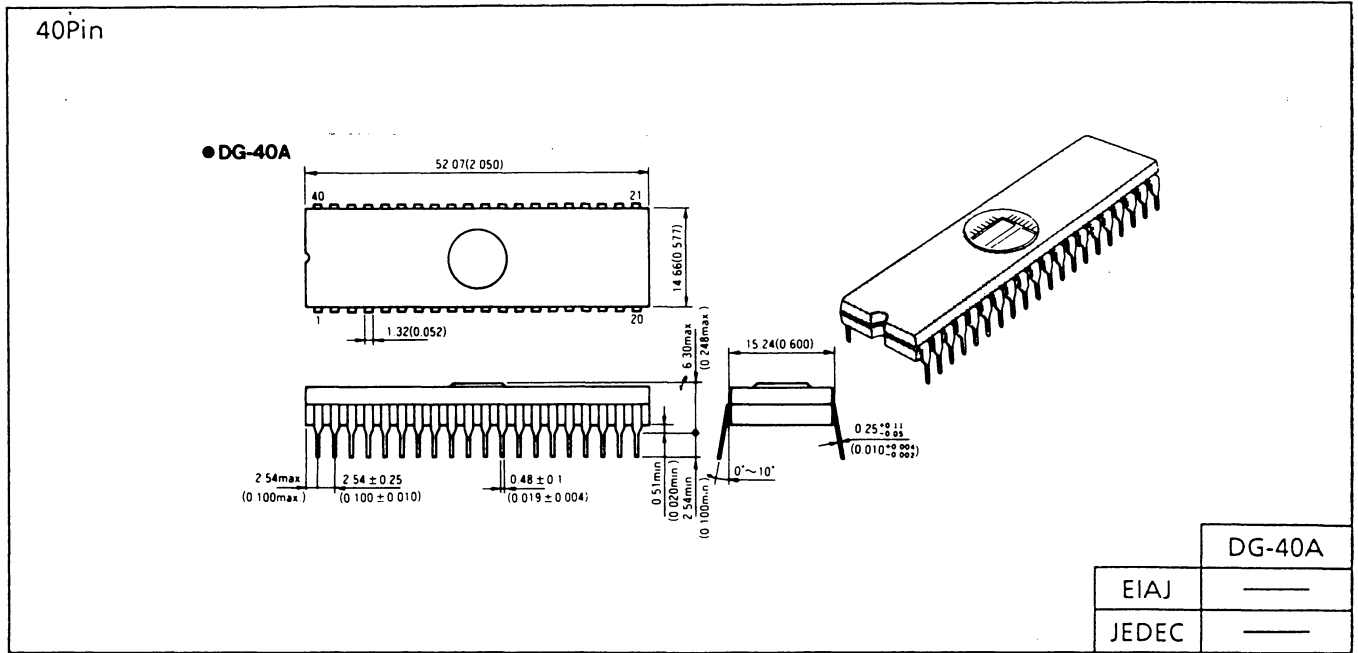
Features

- High speed Access time 100ns / 120ns / 150ns(max)
- Low power dissipation Standby mode: 5 μ W (typ), Active mode: 35mW / MHz (typ)
- Fast high reliability page programming and fast high-reliability programming
..... Programming voltage : +12.5V D.C.
..... Program time: 3.5sec (min) (Theoretical in Page programming)
- Inputs and outputs TTL compatible during both read and program modes
- Pin arrangement 40-pin JEDEC standard, 44-pin JLCC JEDEC standard
- Device identifier mode Manufacturer code and device code

Ordering Information

Type No.	Access Time	Package
HN27C4096G-10	100ns	600mil
HN27C4096G-12	120ns	40-pin Cerdip
HN27C4096G-15	150ns	(DG-40A)
HN27C4096CC-10	100ns	44-pin JLCC
HN27C4096CC-12	120ns	(CC-44)
HN27C4096CC-15	150ns	

Package Outline Unit : mm (inch)



HN29C101 Series

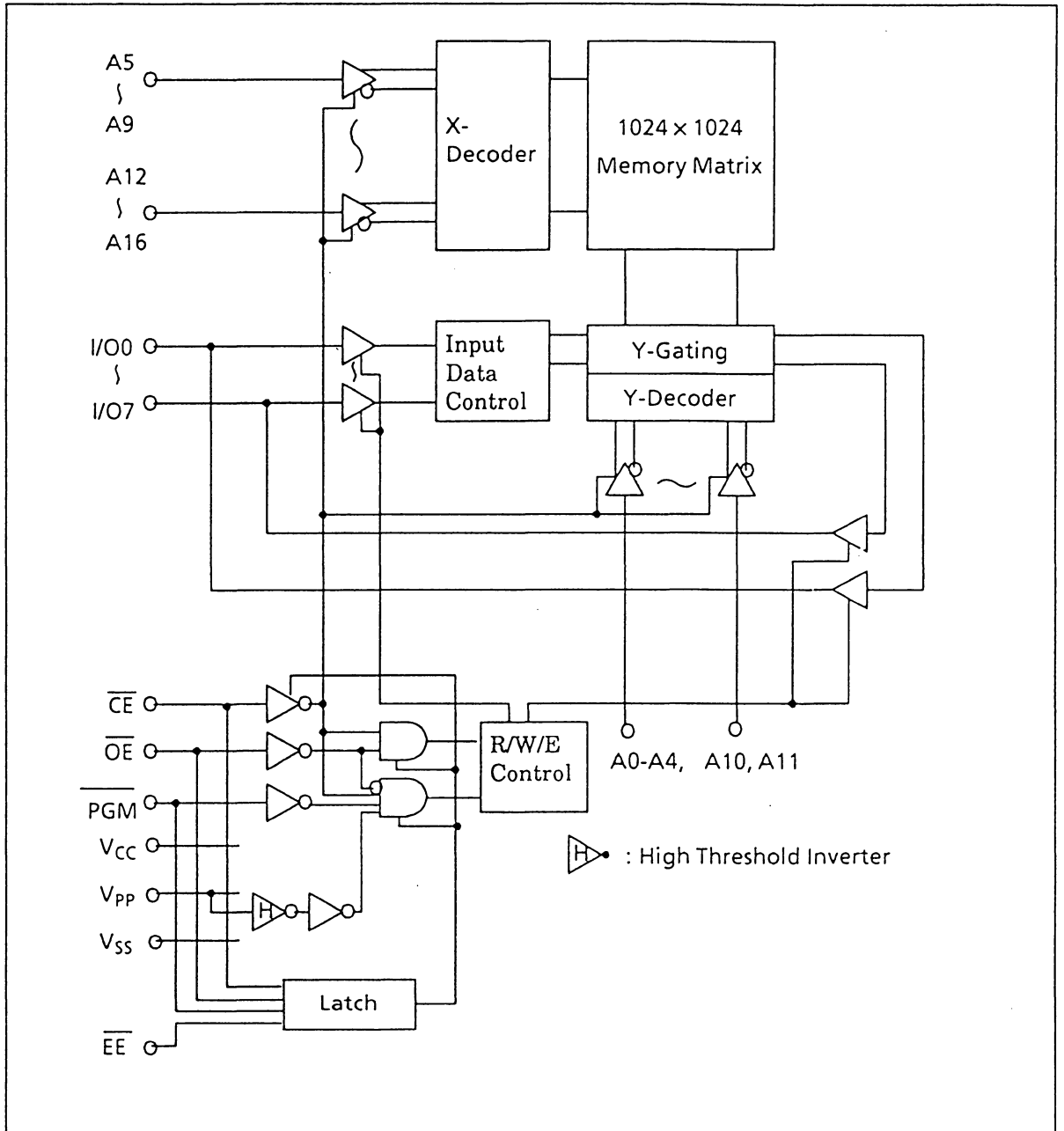
131,072-Word × 8-Bit CMOS Flash Erase Type EEPROM

The Hitachi HN29C101 is a 131072-word x 8-bit CMOS flash erase type EEPROM, realizing on-board programming. It programs or erases data only on on-board power supply (V_{CC}/V_{PP}). The logic level of V_H (12 V) is unnecessary for address pins and control pins and command inputs are unnecessary because it provides an erase control pin (\overline{EE}). When erasing, its control pins, address bus and data bus become free, by control latch. It also provides the status polling function to inform the erase completion to CPU.

Features

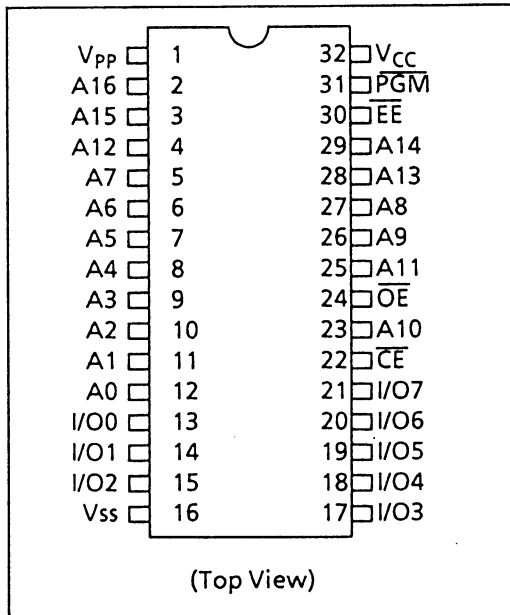
- On-board power supply (V_{CC}/V_{PP})... $V_{CC} = 5\text{ V} \pm 10\%$
 $V_{PP} = V_{CC} - 1\text{ V to } V_{CC}$ (Read)
 $V_{PP} = 12.0\text{ V} \pm 0.4\text{ V}$ (Erase/Program)
- High speed Access time 120ns / 150ns / 200ns (max)
- Single high speed programming ... Byte program
Program time: (200 μs typ.) single pulse
- On-board erase function Chip erase
Erase time: (2s typ)
Address, data, control latch function
Status polling function
- Low power dissipation $I_{CC} = 30\text{ mA typ}$ (Read)
 $I_{CC} = 20\mu\text{A max}$ (Standby)
 $I_{PP} = 30\text{ mA typ}$ (Erase/Program)
 $I_{PP} = 20\mu\text{A max}$ (Read/Standby)
- Erasing endurance More than 100 times
(Please do not over-program on the programmed bits.)
- Pin arrangement 32-pin JEDEC standard
- Package 32-pin DIP
32-pin TSOP

Block Diagram



Pin Arrangement

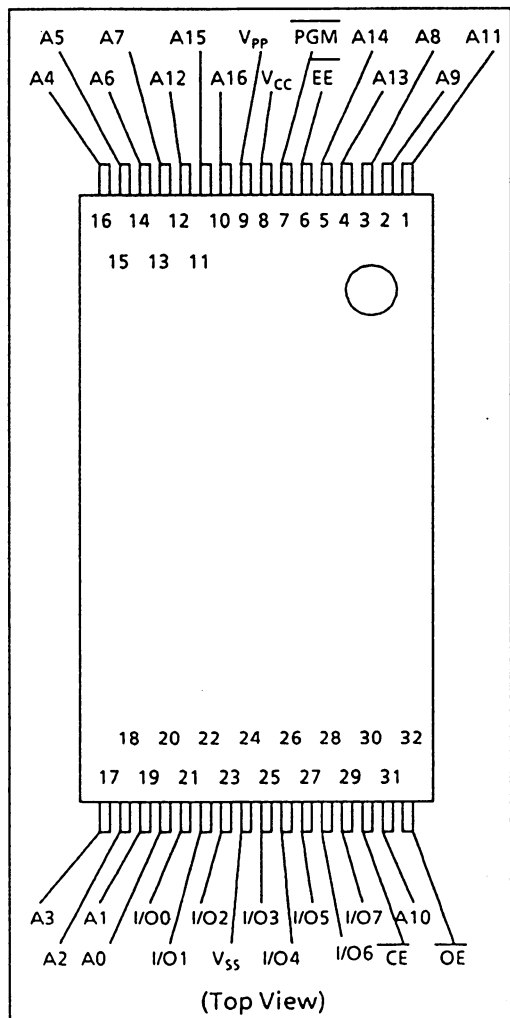
HN29C101P



Pin Description

Pin Name	Function
A0-A16	Address
I/O0-I/O7	Input/output
CE	Chip enable
OE	Output enable
PGM	Programming enable
EE	Erase enable
V _{CC}	Power supply
V _{PP}	Programming power supply
V _{SS}	Ground

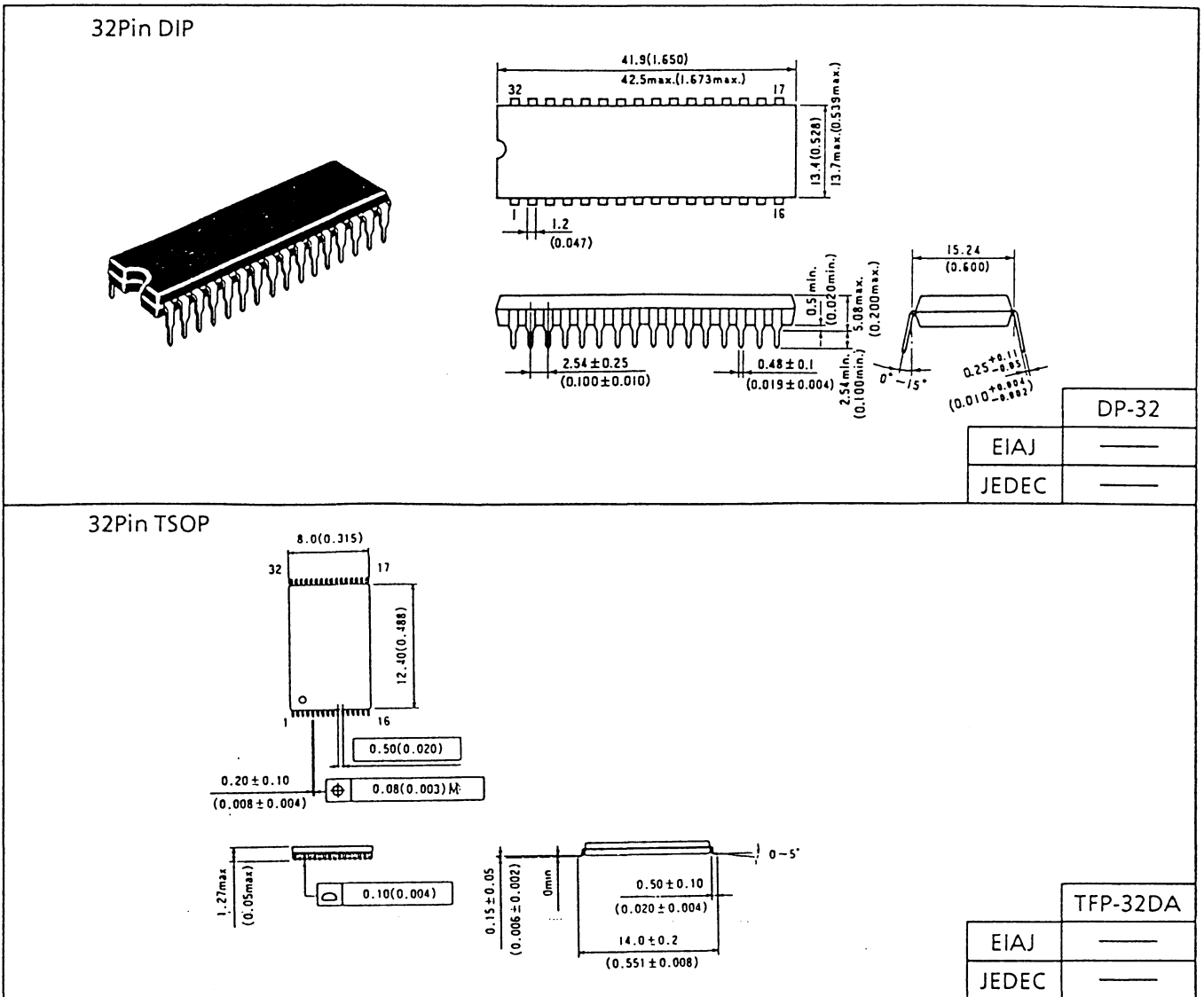
HN29C101TS



Ordering Information

Type No.	Access Time	Package
HN29C101P-12	120ns	32-pin Plastic
HN29C101P-15	150ns	DIP
HN29C101P-20	200ns	(DP-32)
HN29C101TS-12	120ns	32-pin Thin
HN29C101TS-15	150ns	Small Outline
HN29C101TS-20	200ns	Package
		(TFP-32DA)

■ Package Outline Unit : mm (inch)



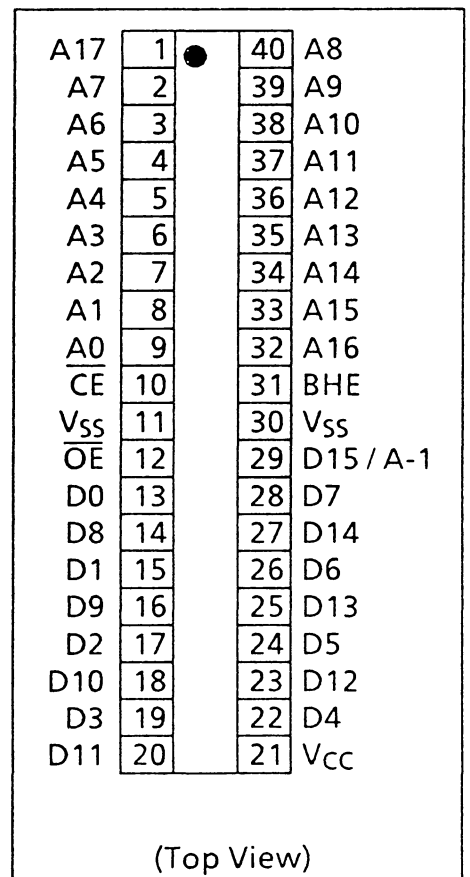
Rev.1 89-07-11

HN62444 Series

262,144 × 16-Bit / 524,288 × 8-Bit CMOS MASK
PROGRAMMABLE READ ONLY MEMORY

The HN62444 is a 4-Mbit CMOS mask-programmable ROM organized either as 262144 words by 16 bits or as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62444, which provides large capacity of 4M bits, is ideally suited for kanji character generators.

Pin Arrangement

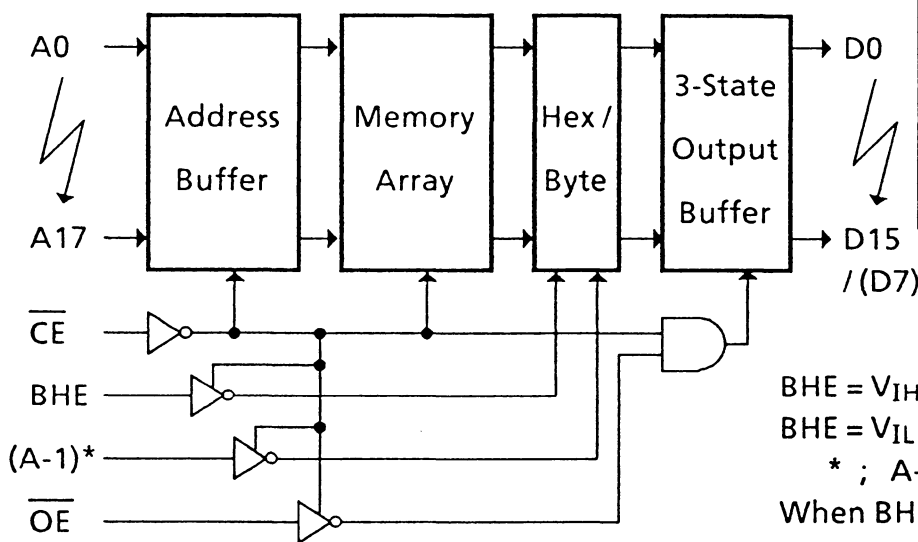


HN62444P

Features

- Single + 5 V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time : 100 ns (Max.)
- Low Power Consumption : 150mW (Typ.) active
5μW (Typ.) standby
- Byte-wide or Word-wide Data Organization with BHE

Block Diagram



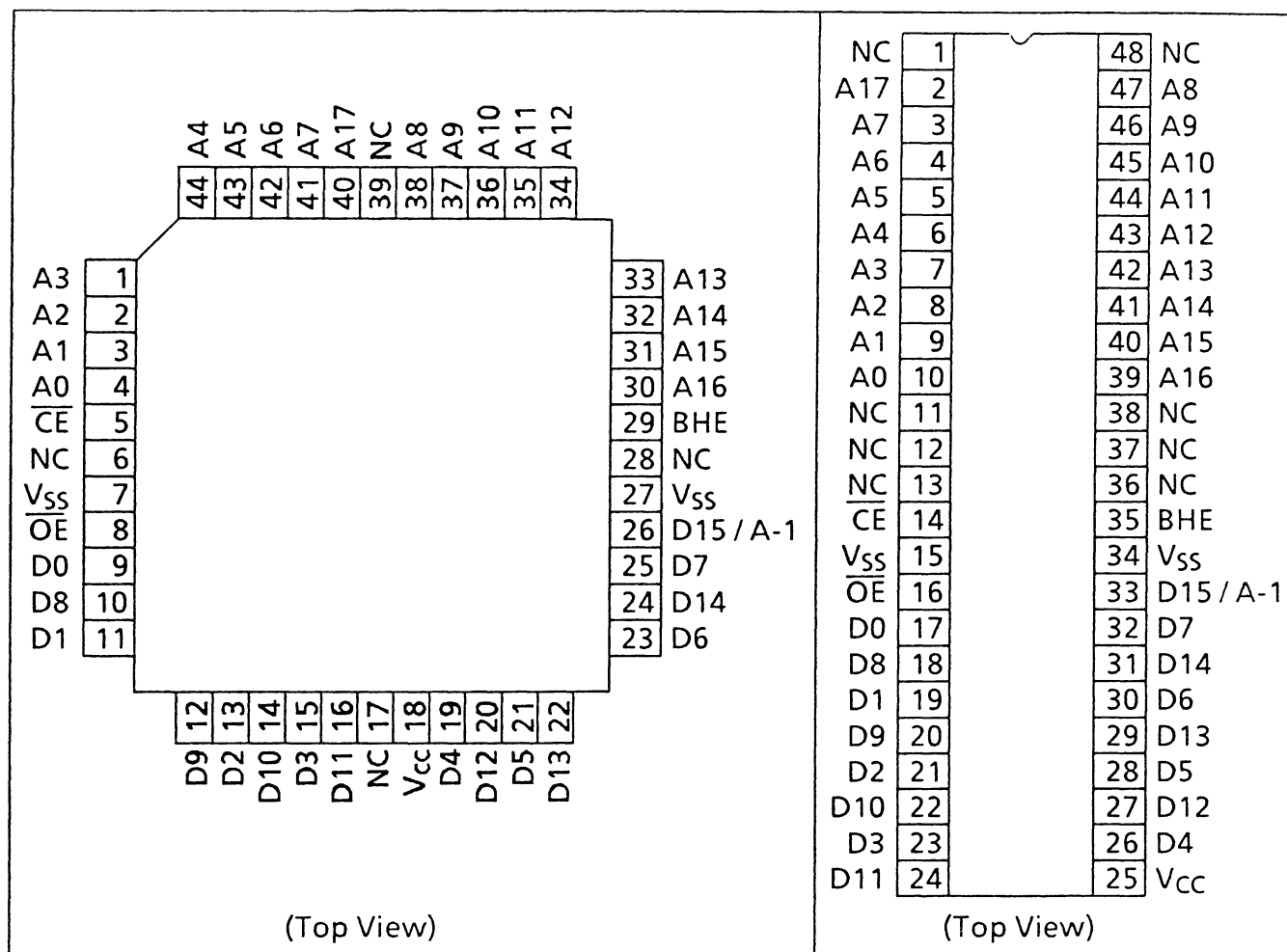
BHE = V_{IH} ; 16-bit (D15~D0)

BHE = V_{IL} ; 8-bit (D7~D0)

* ; A-1 is least significant address.

When BHE is 'low', D14~D8 goes the high impedance state.

Pin Arrangement



HN62444FP

HN62444F

11-12-13 pin and 36-37-38 pin are connected to inner lead frame.

Orderling Information

Type No.	Access Time	Package
HN62444P	100 ns	600 mil 40-pin plastic DIP
HN62444FP	100 ns	44-pin plastic QFP
HN62444F	100 ns	48-pin plastic SOP

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V _{CC}	-0.3 ~ +7.0	V	1
All Input and Output Voltage	V _T	-0.3 ~ V _{CC} + 0.3	V	1
Operating Temperature Range	T _{opr}	0 ~ +70	°C	
Storage Temperature Range	T _{stg}	-55 ~ +125	°C	
Temperature Under Bias	T _{bias}	-20 ~ +85	°C	

Note) 1 : With respect to VSS.

HN62408 Series

524,288 × 16-Bit / 1,048,576 × 8-Bit CMOS MASK PROGRAMMABLE READ ONLY MEMORY

The HN62408 is a 8-Mbit CMOS mask-program-mable ROM organized either as 524288 words by 16 bits or as 1048576 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62408, which provides large capacity of 8M bits, is ideally suited for kanji character generators.

Pin Arrangement

A18	1	42	NC
A17	2	41	A8
A7	3	40	A9
A6	4	39	A10
A5	5	38	A11
A4	6	37	A12
A3	7	36	A13
A2	8	35	A14
A1	9	34	A15
A0	10	33	A16
CE	11	32	BHE
V _{SS}	12	31	V _{SS}
OE	13	30	D15 / A-1
D0	14	29	D7
D8	15	28	D14
D1	16	27	D6
D9	17	26	D13
D2	18	25	D5
D10	19	24	D12
D3	20	23	D4
D11	21	22	V _{CC}

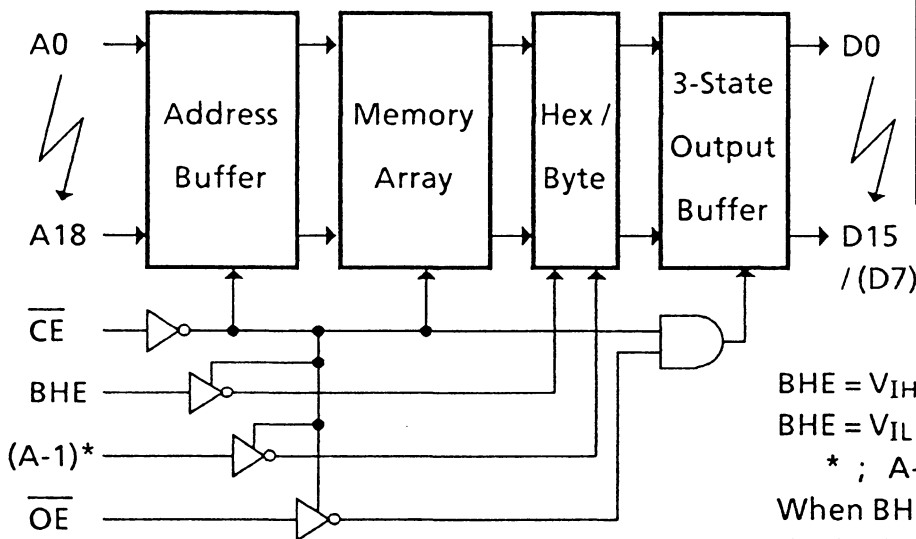
(Top View)

HN62408P

Features

- Single + 5 V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time : 200 ns (Max.)
- Low Power Consumption : 100mW (Typ.) active
5μW (Typ.) standby
- Byte-wide or Word-wide Data Organization with BHE

Block Diagram



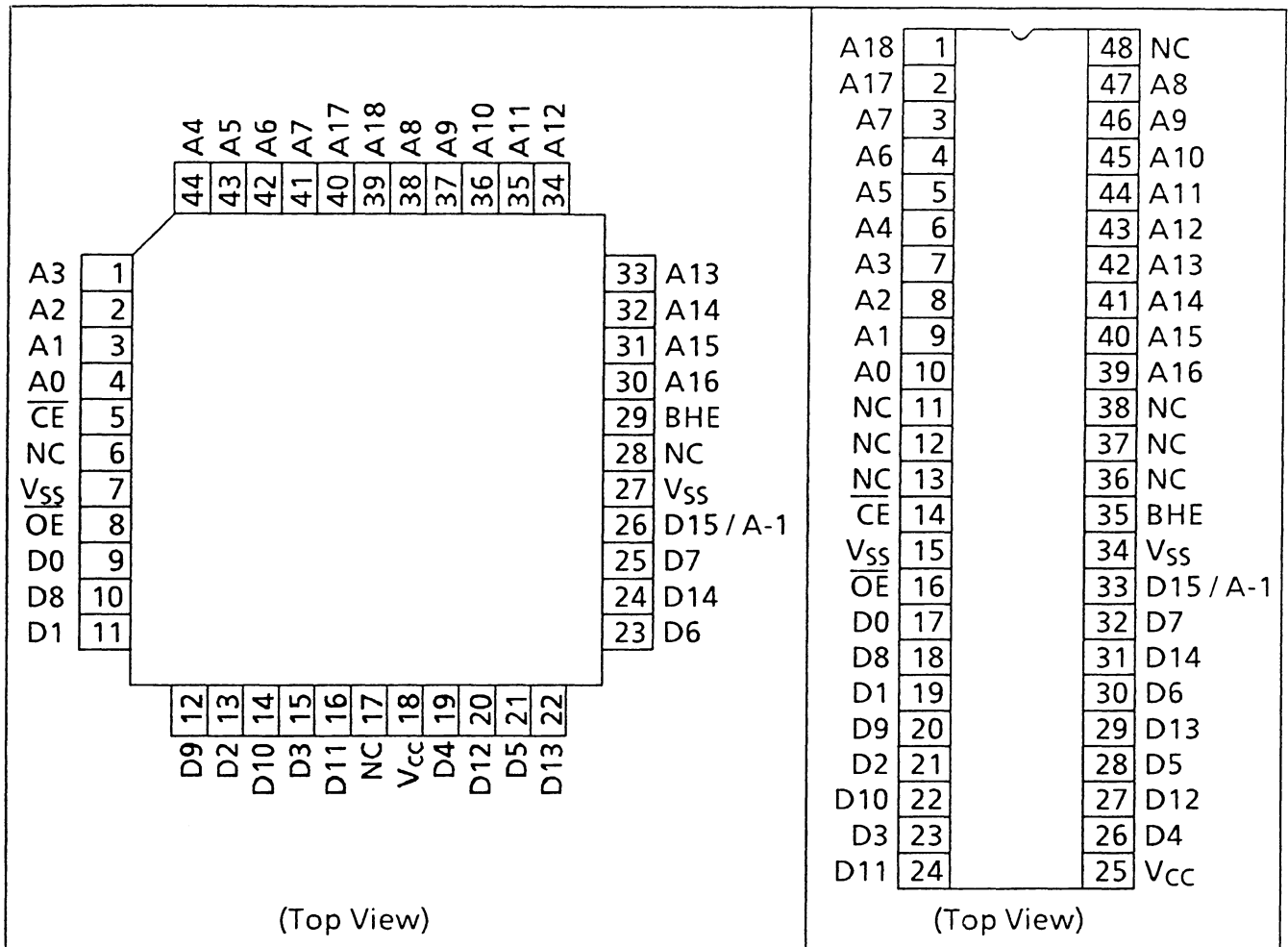
BHE = V_{IH} ; 16-bit (D15~D0)

BHE = V_{IL} ; 8-bit (D7~D0)

* ; A-1 is least significant address.

When BHE is 'low', D14~D8 goes the high impedance state.

Pin Arrangement



12-13 pin and 36-37 pin are connected to inner lead frame.

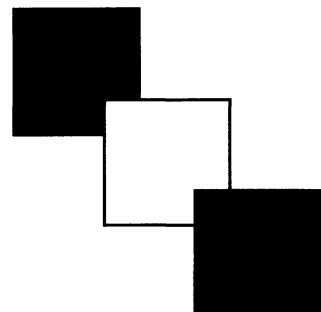
Ordering Information

Type No.	Access Time	Package
HN62408P	200 ns	600 mil 42-pin plastic DIP
HN62408FP	200 ns	44-pin plastic QFP
HN62408F	200 ns	48-pin plastic SOP

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V _{CC}	-0.3 ~ +7.0	V	1
All Input and Output Voltage	V _T	-0.3 ~ V _{CC} +0.3	V	1
Operating Temperature Range	T _{opr}	0 ~ +70	°C	
Storage Temperature Range	T _{stg}	-55 ~ +125	°C	
Temperature Under Bias	T _{bias}	-20 ~ +85	°C	

Note) 1 : With respect to V_{SS}.



HN624016 Series

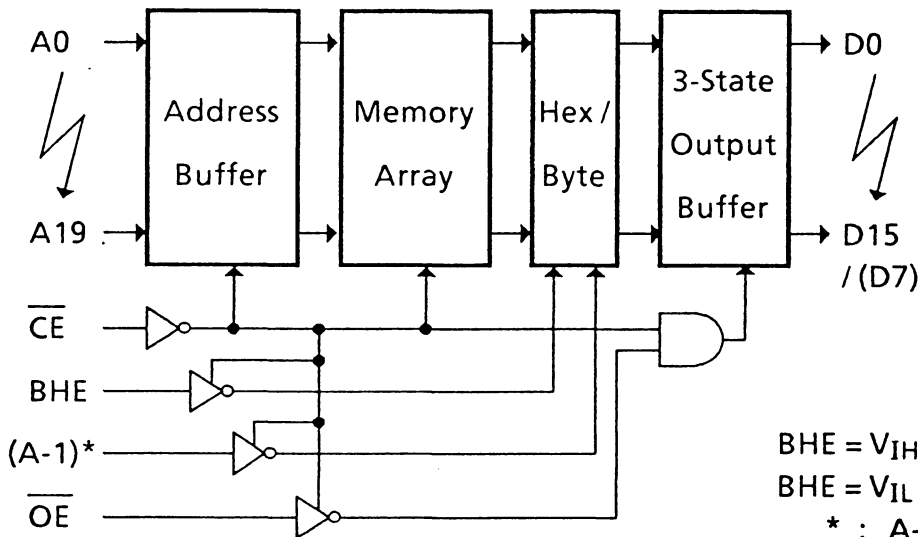
1,048,576 × 16-Bit / 2,097,152 × 8-Bit CMOS MASK
PROGRAMMABLE READ ONLY MEMORY

The HN624016 is a 16-Mbit CMOS mask-programmable ROM organized either as 1048576 words by 16 bits or as 2097152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN624016, which provides large capacity of 16M bits, is ideally suited for kanji character generators.

■ Features

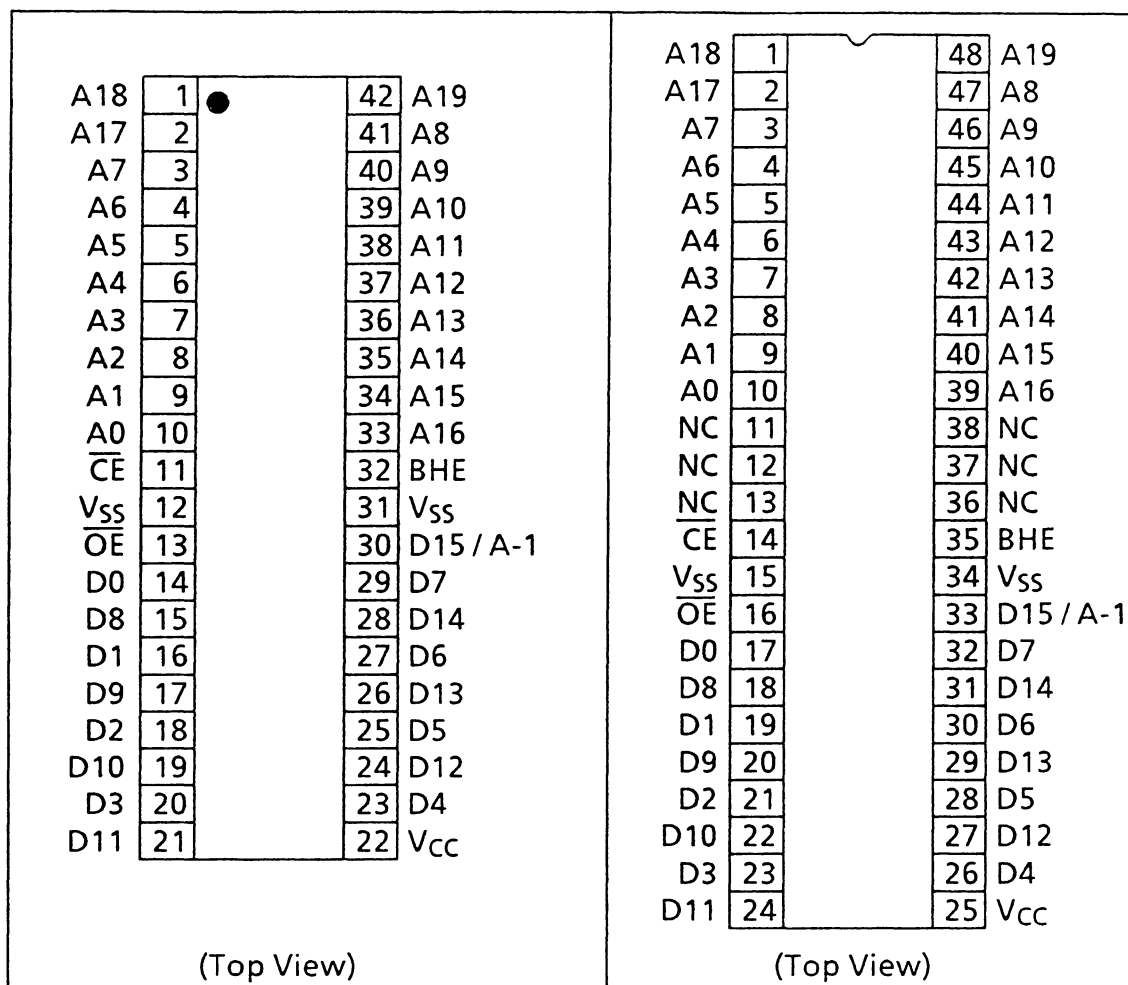
- Single + 5 V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time : 200 ns (Max.)
- Low Power Consumption : 100mW (Typ.) active
5μW (Typ.) standby
- Byte-wide or Word-wide Data Organization with BHE

■ Block Diagram



BHE = V_{IH} ; 16-bit (D15~D0)
 BHE = V_{IL} ; 8-bit (D7~D0)
 * ; A-1 is least significant address.
 When BHE is 'low', D14~D8 goes
 the high impedance state.

■ Pin Arrangement



HN624016P

HN624016F

12-13 pin and 36-37 pin are connected to inner lead frame.

■ Ordering Information

Type No.	Access Time	Package
HN624016P	200 ns	600 mil 42-pin plastic DIP
HN624016F	200 ns	48-pin plastic SOP

■ Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V _{CC}	-0.3 ~ +7.0	V	1
All Input and Output Voltage	V _T	-0.3 ~ V _{CC} + 0.3	V	1
Operating Temperature Range	T _{opr}	0 ~ +70	°C	
Storage Temperature Range	T _{stg}	-55 ~ +125	°C	
Temperature Under Bias	T _{bias}	-20 ~ +85	°C	

Note) 1 : With respect to VSS.

Notice:

Notice:

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