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IC MEMORY DATA BOOK

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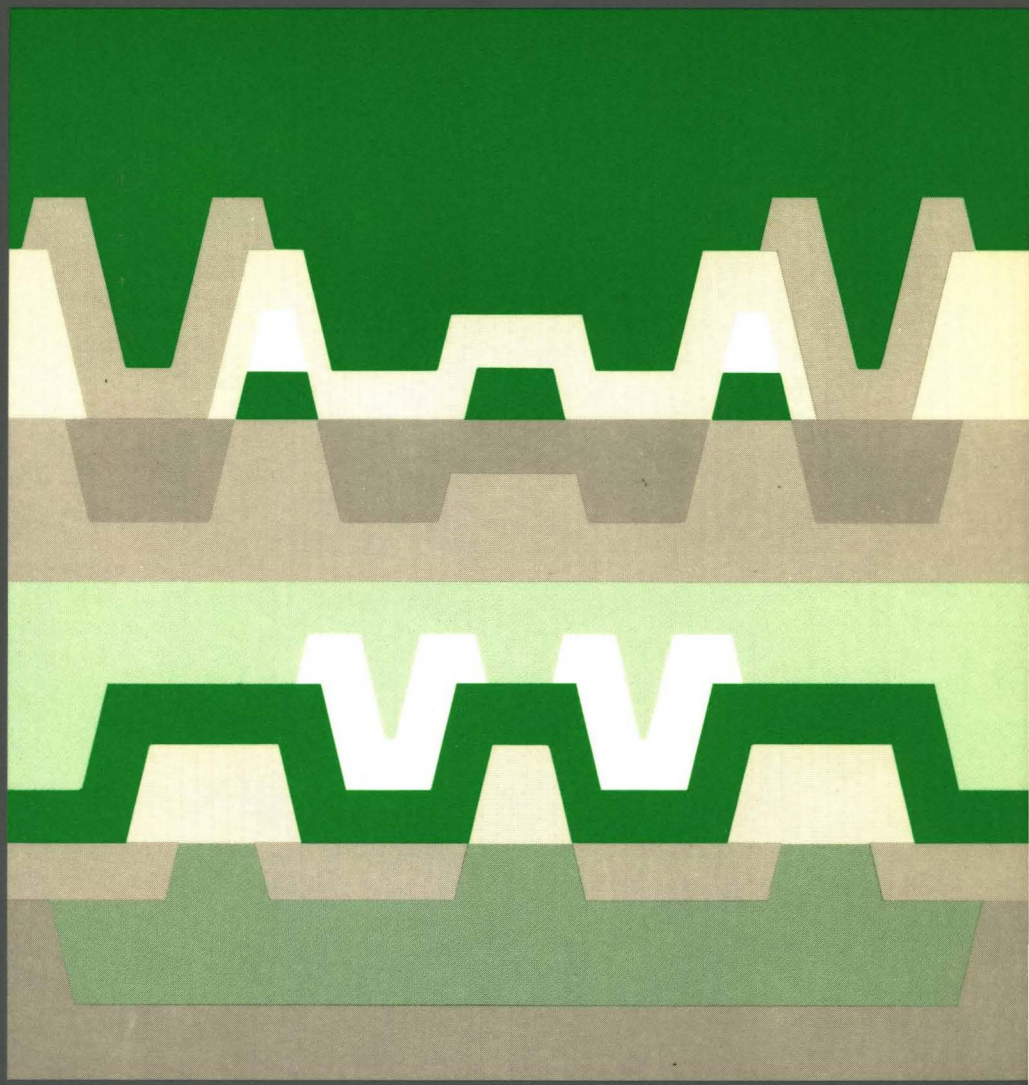

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■QUICK REFERENCE GUIDE TO HITACHI MEMORIES

■MOS RAM

Mode	Total Bit	Type No.	Process	Organization (word×bit)	Access Time (ns) max	Cycle Time (ns) min	Supply Voltage (V)	Power Dissipation (W)	Package*1										Page
									Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	
Static	4k-bit	HM6147H-35*2	CMOS	4096×1	35	35	+5	0.1m/0.15	18		●								63
		HM6147H-45*2			45	45					●								63
		HM6147H-55*2			55	55					●								63
		HM6147HL-35*2			35	35					●								63
		HM6147HL-45*2			45	45					●								63
		HM6147HL-55*2			55	55					●								63
		HM6116-2*2		2048×8	120	120		0.1m/0.2	24		●	●							70
		HM6116-3*2			150	150		0.1m/0.18			●	●							70
		HM6116-4*2			200	200					●	●							70
		HM6116L-2*2			120	120		10μ/0.18			●	●							70
		HM6116L-3*2			150	150		10μ/0.16			●	●							70
		HM6116L-4*2			200	200					●	●							70
		HM6116A-12*2			120	120		0.1m/15m			●		●						77
		HM6116A-15*2			150	150					●		●						77
		HM6116A-20*2			200	200					●		●						77
		HM6116AL-12*2			120	120		5μ/10m			●		●						77
		HM6116AL-15*2			150	150					●		●						77
		HM6116AL-20*2			200	200					●		●						77
		HM6716-25	Bi-CMOS		25	25		0.28					●						85
		HM6716-30			30	30							●						85
	16k-bit	HM6168H-45*2	CMOS	4096×4	45	45		0.1m/0.2	20		●								90
		HM6168H-55*2			55	55					●								90
		HM6168H-70*2			70	70					●								90
		HM6168HL-45*2			45	45		5μ/0.2			●								90
		HM6168HL-55*2			55	55					●								90
		HM6168HL-70*2			70	70					●								90
		HM6268-25			25	25		0.1m/0.25					●						97
		HM6268-35			35	35							●						97
		HM6268L-25			25	25		5μ/0.25					●						97
		HM6268L-35			35	35							●						97
		HM6167-6*2		16384×1	85	85		0.1m/0.15			●								104
		HM6167-8*2			100	100					●								104
		HM6167L-6*2			85	85		5μ/0.15			●								104
		HM6167L-8*2			100	100					●								104
		HM6167H-55*2			55	55		0.1m/0.2			●								111
		HM6167H-70*2			70	70					●								111
		HM6167HL-55*2			55	55		5μ/0.2			●								111
		HM6167HL-70*2			70	70					●								111
		HM6267-35			35	35		0.1m/0.2					●						118
		HM6267-45			45	45							●						118
		HM6267L-35			35	35		5μ/0.2					●						118
		HM6267L-45			45	45							●						118
	18k-bit	HM6719-25*2	Bi-CMOS	2048×9	25	25		0.28	24	●									85
		HM6719-30*2			30	30				●									85

Mode	Total Bit	Type No.	Process	Organization (word×bit)	Access Time (ns) max	Cycle Time (ns) min	Supply Voltage (V)	Power Dissipation (W)	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	64k-bit	HM6264-10*2	CMOS	8192×8	100	100	+5	0.1m/0.2	28		●	●							125
		HM6264-12*2			120	120					●	●							125
		HM6264-15*2			150	150					●	●							125
		HM6264L-10*2			100	100		10μ/0.2			●	●							125
		HM6264L-12*2			120	120					●	●							125
		HM6264L-15*2			150	150					●	●							125
		HM6264L-10L			100	100		10μ/0.2			●	●							125
		HM6264L-12L			120	120					●	●							125
		HM6264L-15L			150	150					●	●							125
		HM6264A-12			120	120		0.1m/15m			●	●	●						133
		HM6264A-15			150	150					●	●	●						133
		HM6264AL—12			120	120		10μ/15m			●	●	●						133
		HM6264AL-15			150	150					●	●	●						133
		HM6264AL-12L			120	120		10μ/15m			●	●	●						133
		HM6264AL-15L			150	150					●	●	●						133
		HM6288-25		16384×4	25	25		0.1m/0.3	22				●				●		145
		HM6288-35			35	35							●				●		145
		HM6288-45			45	45							●				●		145
		HM6288L-25			25	25		0.1m/0.3					●				●		145
		HM6288L-35			35	35							●				●		145
		HM6288L-45			45	45							●				●		145
		HM6788-25	Bi-CMOS	16384×4	25	25		10m/0.23	22				●						150
		HM6788-35			35	35							●						150
		HM6788H-15			15	15							●						154
		HM6788H-20			20	20							●						154
		HM6789-25			25	25		10m/0.23	24				●				●		160
		HM6789-30			30	30							●				●		160
		HM6789H-15			15	15							●				●		167
		HM6789H-20			20	20							●				●		167
		HM6287-45	CMOS	65536×1	45	45		0.1m/0.3	22				●						175
		HM6287-55			55	55							●						175
		HM6287-70			70	70							●						175
		HM6287L-45			45	45		10μ/0.3					●						175
		HM6287L-55			55	55							●						175
		HM6287L-70			70	70							●						175
		HM6287H-25			25	25		0.1m/0.3					●				●		182
		HM6287H-35			35	35							●				●		182
		HM6287HL-25			25	25							●				●		182
		HM6287HL-35			35	35							●				●		182
		HM6787-25	Bi-CMOS		25	25		38m/0.15					●		●				190
		HM6787-35			30	30							●		●				190
		HM6787H-15			15	15		10m/0.28					●						195
		HM6787H-20			20	20							●						195
	256k-bit	HM62256-8	CMOS	32768×8	85	85		0.2m/40m	28		●	●							201
		HM62256-10			100	100					●	●							201
		HM62256-12			120	120					●	●							201
		HM62256-15			150	150					●	●							201
		HM62256L-8			85	85		10μ/40m			●	●							201
		HM62256L-10			100	100					●	●							201
		HM62256L-12			120	120					●	●							201
		HM62256L-15			150	150					●	●							201

Mode	Total Bit	Type No.	Process	Organization (word×bit)	Access Time (ns) max	Cycle Time (ns) min	Supply Voltage (V)	Power Dissipation (W)	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	256k-bit	HM62256SL-10	CMOS	32768×8	100	100	+5	10μ/40m	28		●	●							201
		HM62256SL-12			120	120					●	●							201
		HM62256SL-15			150	150					●	●							201
		HM6208-35		65536×4	35	35		0.1m/0.3	24		●								209
		HM6208-45			45	45					●								209
		HM6208L-35			35	35		10μ/0.3			●								209
		HM6208L-45			45	45					●								209
		HM6708-20			20	20		10m/0.175	24				●				●		215
		HM6708-25			25	25							●				●		215
		HM6207-35		262144×1	35	35		0.1m/0.3					●						221
		HM6207-45			45	45							●						221
		HM6207L-35			35	35		10μ/0.3					●						221
		HM6207L-45			45	45							●						221
		HM6707-20	Bi-CMOS		20	20		10m/0.175					●				●		227
		HM6707-25			25	25							●				●		227
Static RAM Module	1M-bit	HM66203-10	CMOS	131072×8	100	100		0.8m/40m	32									●	233
		HM66203-12			120	120												●	233
		HM66203-15			150	150												●	233
		HM66203L-10			100	100		40μ/40m										●	233
		HM66203L-12			120	120												●	233
		HM66203L-15			150	150												●	233
		HM66204-12*3		131072×8 (With Decoder)	120	120		10m/50m										●	239
		HM66204-15*3			150	150												●	239
		HM66204L-12*3			120	120		40μ/50m										●	239
		HM66204L-15*3			150	150												●	239
		HM628128-7		131072×8	70	70		5m/75m			●	●							245
		HM628128-8			85	85					●	●							245
		HM628128-10			100	100					●	●							245
		HM628128-12			120	120					●	●							245
		HM628128L-7			70	70		10μ/75m			●	●							245
		HM628128L-8			85	85					●	●							245
		HM628128L-10			100	100					●	●							245
		HM628128L-12			120	120					●	●							245
Pseudo Static	256k-bit	HM6526A-12	CMOS	32768×8	120	190		2m/0.175	28		●		●						259
		HM6526A-15			150	235					●		●						259
		HM6526A-20			200	310					●		●						259
		HM65256B-10			100	180					●	●	●						265
		HM65256B-12			120	190					●	●	●						265
		HM65256B-15			150	235					●	●	●						265
		HM65256B-20			200	310					●	●	●						265
		HM65256BL-10			100	180					●	●	●						265
		HM65256BL-12			120	190					●	●	●						265
		HM65256BL-15			150	235					●	●	●						265
		HM65256BL-20			200	310					●	●	●						265

Mode	Total Bit	Type No.	Process	Organization (word×bit)	Access Time (ns) max	Cycle Time (ns) min	Supply Voltage (V)	Power Dissipation (W)	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Pseudo Static	1M-bit	HM658128-10	CMOS	131072×8	100	180	+5	5m/0.2	32		●	●							272
		HM658128-12			120	210					●	●							272
		HM658128-15			150	250					●	●							272
		HM658128L-10			100	180		0.3m/0.2			●	●							272
		HM658128L-12			120	210					●	●							272
		HM658128L-15			150	250					●	●							272
Video Memory	16k-bit	HM63021-28	CMOS	2048×8 Line Memory	20	28		0.25	28				●						321
		HM63021-28			25	34							●						321
	256k-bit	HM53461-10		65536×4 Multi-port	100	190		40m/0.38	24		●			●					289
		HM53461-12			120	220					●			●					289
		HM53461-15			150	260					●			●					289
		HM53462-10			100	190					●			●					302
		HM53462-12			120	220					●			●					302
		HM53462-15			150	260					●			●					302
	1M-bit	HM53051*3		262144×4 Frame Memory	40	60		0.3	18		●								280
Dynamic	256k-bit	HM50464-12	NMOS	65536×4	120	220		20m/0.35	18		●					●			336
		HM50464-15			150	260					●					●			336
		HM50464-20			200	330					●					●			336
		HM50465-12			120	220					●								344
		HM50465-15			150	260					●								344
		HM50465-20			200	330					●								344
		HM50256-12		262144×1	120	220		20m/0.35	16		●			●		●			352
		HM50256-15			150	260					●			●		●			352
		HM50256-20			200	330					●			●		●			352
		HM50257-12			120	220					●			●		●			360
		HM50257-15			150	260					●			●		●			360
		HM50257-20			200	330					●			●		●			360
		HM51256-8	CMOS		85	155		5m/0.2	16		●			●		●			368
		HM51256-10			100	180					●			●		●			368
		HM51256-12			120	210					●			●		●			368
		HM51256-15			150	250					●			●		●			368
		HM51256L-8			85	155		0.3m/0.2			●			●		●			368
		HM51256L-10			100	180					●			●		●			368
		HM51256L-12			120	210					●			●		●			368
		HM51256L-15			150	250					●			●		●			368
		HM51258-8			85	155		5m/0.2			●								376
		HM51258-10			100	180					●								376
		HM51258-12			120	210					●								376
		HM51258-15			150	250					●								376
	1M-bit	HM514256-10*3		262144×4	100	180		10m/0.3	20		●			●			●		384
		HM514256-12*3			120	210					●			●			●		384
		HM514256-15*3			150	250					●			●			●		384
		HM514258-10*4			100	180		11m/0.3			●			●			●		393
		HM514258-12*4			120	210					●			●			●		393
		HM514258-15*4			150	250					●			●			●		393
		HM511000-10		1048576×1	100	180		10m/0.3	18	●	●			●			●		395
		HM511000-12			120	210				●	●			●			●		395

Mode	Total Bit	Type No.	Process	Organization (word×bit)	Access Time (ns) max	Cycle Time (ns) min	Supply Voltage (V)	Power Dissipation (W)	Package*1										Page
									Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	
Dynamic RAM Module	1M-bit	HM511000-8S*3	CMOS	1048576×1	80	160	+5	11m/0.33	18		●			●			●		404
		HM511000-10S*3			100	190					●			●			●		404
		HM511000-12S*3			120	220					●			●			●		404
		HM511001-10			100	180		10m/0.3		●	●			●			●		414
		HM511001-12			120	210				●	●			●			●		414
		HM511001-8S*3			80	160		11m/0.33			●			●			●		423
		HM511001-10S*3			100	190					●			●			●		423
		HM511001-12S*3			120	220					●			●			●		423
		HM511002-8S*3			80	160		10m/0.3			●			●			●		432
		HM511002-10S*3			100	190					●			●			●		432
		HM511002-12S*3			120	220					●			●			●		432
	2M-bit	HB561008-12	NMOS	262144×8	120	220		0.12/2.42	30									●	470
		HB561008-15			150	260		0.12/1.92										●	470
		HB561008-20			200	330		0.12/1.51										●	470
		HB561003-12			120	220		0.135/2.55										●	444
		HB561003-15			150	260		0.135/2.16										●	444
		HB561003-20			200	330		0.135/1.70										●	444
		HB561409-10	CMOS		100	180		90m/2.7										●	452
		HB561409L-10			100	180		90m/2.7										●	460
		HB561409L-12			120	210												●	460
	8M-bit	HB56A18-10		1048576×8	100	180		20m/0.18										●	479
		HB56A18-12			120	210												●	479
		HB56A18-15			150	250												●	479
	9M-bit	HB56A19-10*3		1048576×9	100	180		22m/2.0										●	486
		HB56A19-12*3			120	210												●	486
		HB56A19-15*3			150	250												●	486

Notes) *1. The package codes of G to M are applied to the package materials as follows.
G: Cerdip, P: Plastic DIP, FP: Plastic Flat Package(SOP), SP: Skinny Type Plastic DIP, ZP: Plastic ZIP, CG: Ceramic Leadless Chip Carrier, CP: Plastic Leaded Chip Carrier, JP: Plastic Small Outline J-bend Package, M: Module
*2. Maintenance Only. This device is not available for new application.
*3. Preliminary.
*4. Under Development.

■MOS ROM

Program	Total Bit	Type No.	Process	Organization (word×bit)	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (W)	Package*1 PinNo.	G	P	FP	Page
Mask	256k-bit	HN623257	CMOS	32768×8	150		5μ/0.1	28		●	●	494
	1M-bit	HN62321		131072×8	150		5μ/0.1			●		497
		HN62321B			200					●		500
		HN62321E								●		503
	2M-bit	HN62412		131072×16 or 262144×8	200		5μ/0.1	40		●		506
	4M-bit	HN62404		262144×16 or 524288×8	200					●		508
UV Erasable & Electrically	128k-bit	HN27128A-17	NMOS	16384×8	170		80m/0.3	28	●			529
		HN27128A-20			250				●			529
		HN27128A-25			250				●			529
		HN27128A-30			300				●			529
	256k-bit	HN27256-25		32768×8	350		50m/0.2		●			543
		HN27256-30			300				●			543
		HN27C256-17	CMOS		170		5μ/20m		●			553
		HN27C256-20			200				●			553
		HN27C256-25			250				●			553
		HN27C256-30			300		5μ/25m		●			553
		HN27C256H-70*3			70				●			564
		HN27C256H-85*3			85	+5			●			564
	512k-bit	HN27512-25	NMOS	65536×8	250		50m/0.2		●			570
		HN27512-30			300				●			570
	1M-bit	HN27C101-17	CMOS	131072×8	170		5μ/50m	32	●			585
		HN27C101-20			200				●			585
		HN27C101-25			250				●			585
		HN27C301-17			170				●			600
		HN27C301-20			200				●			600
		HN27C301-25			250				●			600
One Time	128k-bit	HN27128A-20	NMOS	16384×8	200		35m/0.15	28		●		536
		HN27128A-25			250					●		536
	256k-bit	HN27256-25		32768×8	250		50m/0.225			●		548
		HN27256-30			300					●		548
		HN27C256-25	CMOS		250		5μ/20m				●	559
		HN27C256-30			300						●	559
	512k-bit	HN27512-25	NMOS	65536×8	250		40m/0.225			●		577
		HN27512-30			300					●		577
	1M-bit	HN27C101-20	CMOS	131072×8	200		5μ/50m	32		●	●	593
		HN27C101-25			250					●	●	593
		HN27C301-20			200					●	●	609
		HN27C301-25			250					●	●	609
Electricall Erasable & Programmable	64k-bit	HN58064-25	NMOS	8192×8	250		0.1/0.2	28		●	●	514
		HN58064-30			300	+5				●		514
		HN58C65-25	CMOS		250		5μ/20m			●	●	520

Notes) *1. The package cades of G, P and FP are applied to the package material as follows.
G: cerdip, P: Plastic DIP, FP: Plastic Flat Package(FPP and SOP)
*2. Maintenance Only. This device not available for new aplication.
*3. Preliminary
*4. Under Development

■ECL RAM

Level	Total Bit	Type No.	Organization (word×bit)	Output	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (W)	Package*1 PinNo.	G	F	CG	Replacement	Page
ECL 10K	1k-bit	HM10422	256×4	Open Emitter	10	−5.2	0.8	24	●			F10422	618
		HM10422-7			7		1.0		●				623
		HM2112	1024×1		10		0.8	16	●				626
		HM2112-1			8				●				626
	4k-bit	HM10474	1024×4		25		0.8	24	●			F10474	631
		HM10474-8			8		1.2		●				636
		HM10474-10			10				●				636
		HM10470	4096×1		25		0.8	18	●			F10470	639
		HM10470-1			15				●				639
		HM10470-20			20		1.0		●				644
		HM2142			10		1.2	20	●				647
	16k-bit	HM10484-10*3	4096×4		10		0.8	28	●				650
		HM10480	16384×1		25		0.8	20	●	●		F10480	654
		HM10480-15			15		1.0		●	●			657
		HM10480L			25		0.35		●				660
	64k-bit	HM10494L*3	16384×4		25		0.5	28			●		663
		HM10490-15*3	65536×1		15		0.42	22	●				669
ECL 100K	1k-bit	HM100422	256×4		10	−4.5	0.8	24	●	●	●	F100422	672
		HM100415	1024×1		10		0.6	16			●	F100415	675
	4k-bit	HM100474	1024×4		25		0.8	24	●	●		F100474	678
		HM100474-8			8		1.0		●	●			683
		HM100474-10			10				●	●			683
		HM100470	4096×1		25		0.8	18	●			F100470	686
	16k-bit	HM100484-10*3	4096×4		10		0.8	28	●				689
		HM100480-15	16384×1		15		0.8	20	●	●			693
	64k-bit	HM100490-15*3	65536×1		15		0.42	22	●	●	●		696

Notes) *1. The package cades of G, F and CG are applied to the package material as follows.
G; cerdip, F; Flat Package, CG; Ceramic Leadless Chip Carrier
*2. Maintenance Only. This device is not available for new aplication.
*3. Preliminary
*4. Under Development

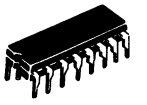
PACKAGE INFORMATION

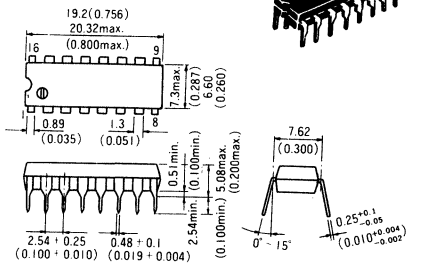
■ PACKAGE INFORMATION

● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

● DP-16B





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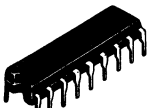

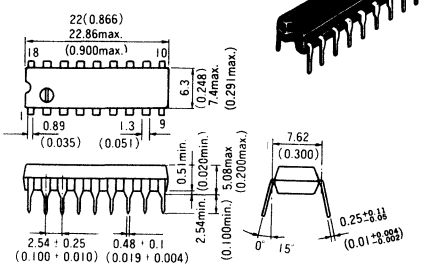

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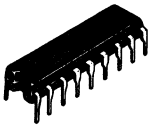

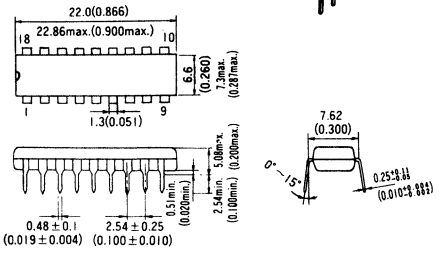

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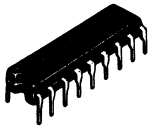

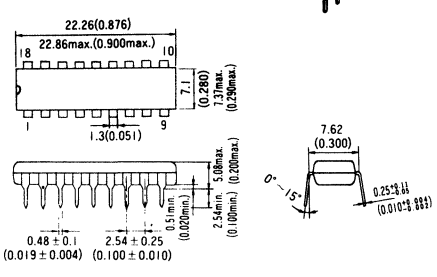

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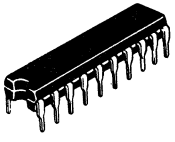

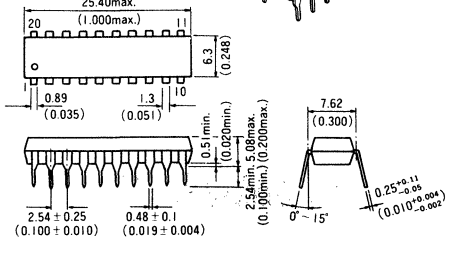

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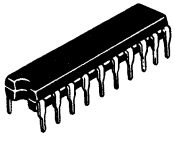

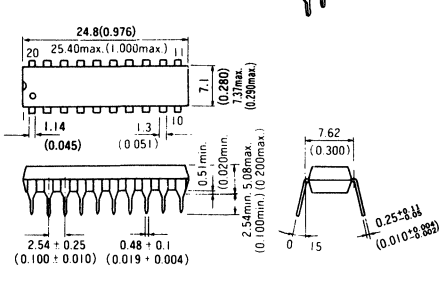

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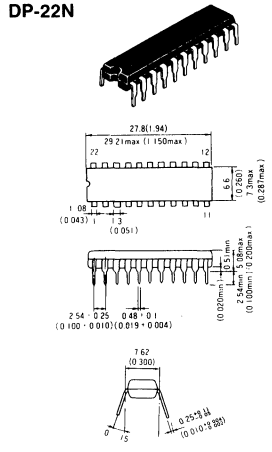
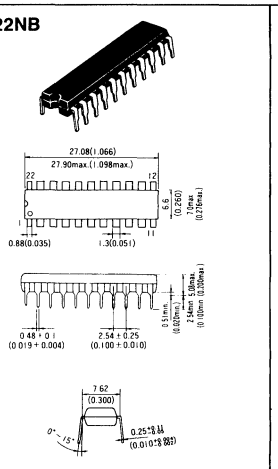
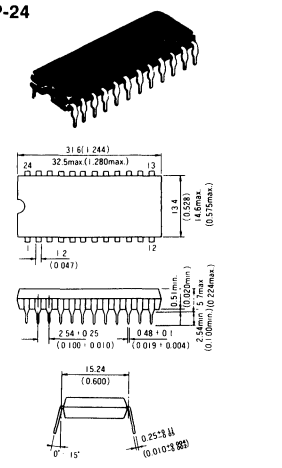


• DP-22NB



• DP-24



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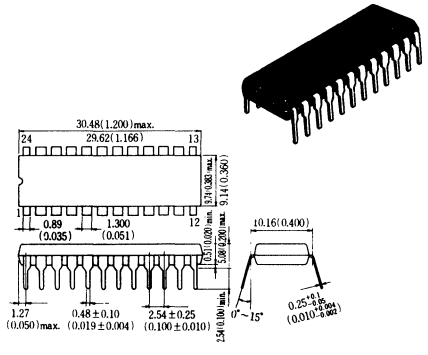

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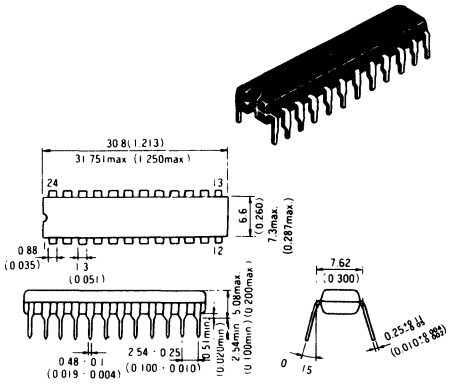

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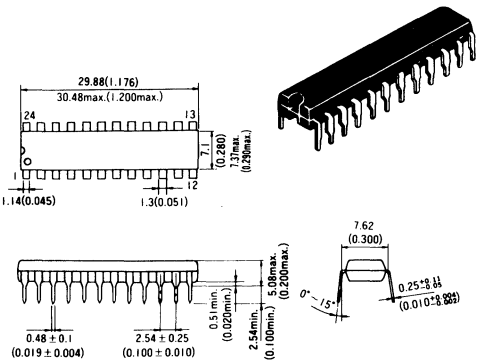
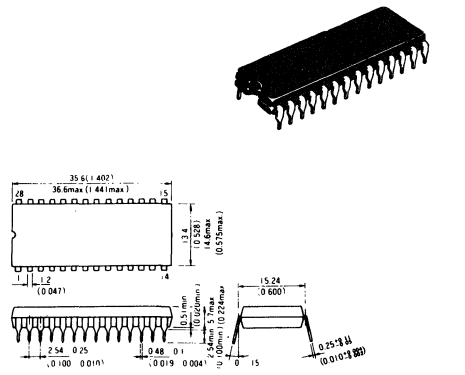


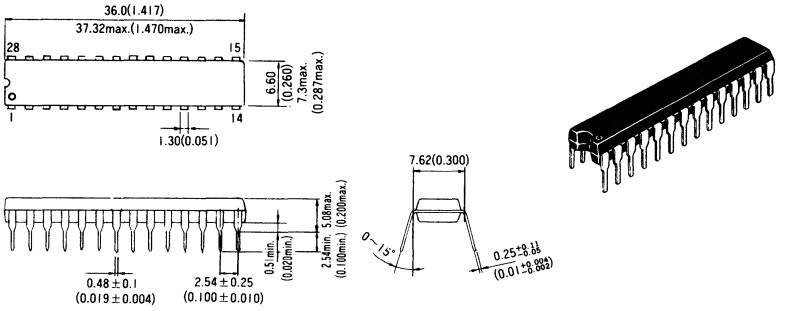
• DP-28



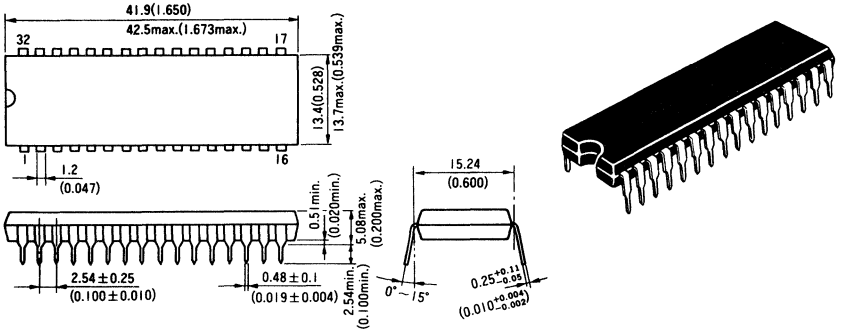
PACKAGE INFORMATION

Unit: mm (inch) Scale 1/1

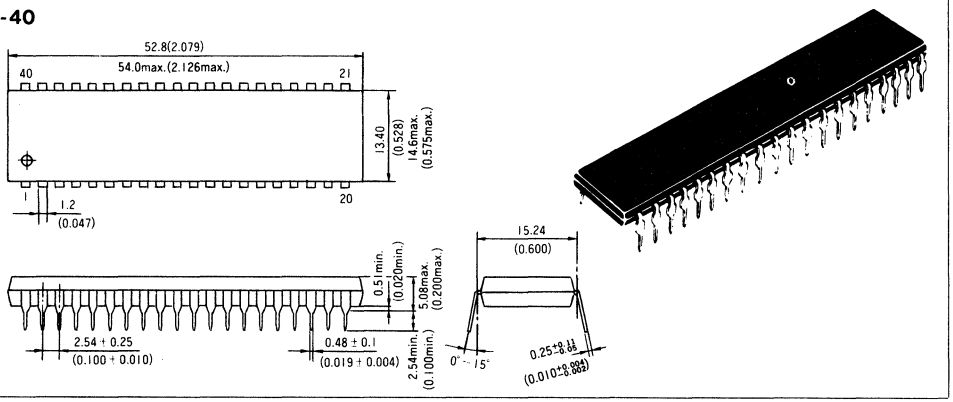
● DP-28N



● DP-32



● DP-40



Applicable ICs

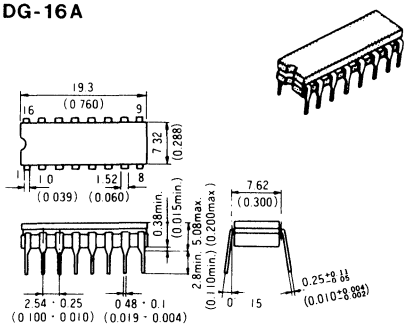
DP-16B	HM50256P Series, HM50257P Series, HM51256P Series, HM51256LP Series,HM51258P Series
DP-18	HM6148HP Series, HM6148HLP Series, HM6147HP Series, HM6147HLP Series
DP-18B	HM50464P Series, HM50465P Series, HM53051P
DP-18C	HM511000P Series, HM511000SP Series, HM511001P Series, HM511001SP Series, HM511002SP Series,
DP-20N	HM5168HP Series, HM6168HLP Series, HM6268P Series, HM6268LP Series, HM6167P Series, HM6167LP Series, HM6167HP Series, HM6167HLP Series, HM6267P Series, HM6267LP Series
DP-20NA	HM614256p Series, HM514258P Series
DP-22N	HM6287P Series, HM6287LP Series, HM6787P, Series, HM6288P Series, HM6788P Series
DP-24	HM6116P Series, HM6116LP Series, HM6116AP Series, HM6116ALP Series, HN61365P, HM61366P
DP-24A	HM53461P Series, HM53462P Series

DP-24N	HM6116ASP Series, HM6116ALSP Series, HM6208P Series, HM6208LP Series, HM6207P Series, HM6207LP Series
DP-28	HM6264P Series, HM6264LP Series, HM6264LP-L Series, HM6264AP Series, HM6264ALP Series, HM6264ALP-L Series, HM62256P Series, HM62256LP Series, HM65256AP Series, HM65256BP Series, HM65256BLP Series, HN61364P, HN613128P, HN623257P, HN62321P, HN62321BP, HN62321EP, HN27128AP Series, HN27256P Series, HN27C256AP Series, HN27512P Series, HN58064P Series, HN58C65P Series
DP-28N	HM6264ASP Series, HM6264ALSP Series, HM6264ALSP-L Series, HM65256ASP Series, HM65256BSP Series, HM65256BLSP Series, HM63021P Series
DP-32	HM658128P Series, HM658128LP Series, HN27C101P Series, HN27C301P Series
DP-40	HN62412P, HN62404P

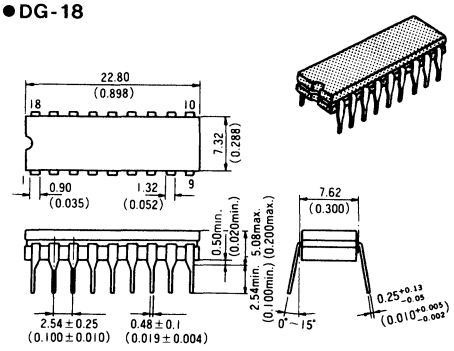
●CERDIP

Unit: mm (inch) Scale 1/1

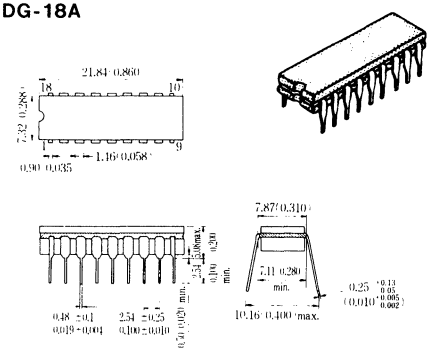
●DG-16A



●DG-18



●DG-18A



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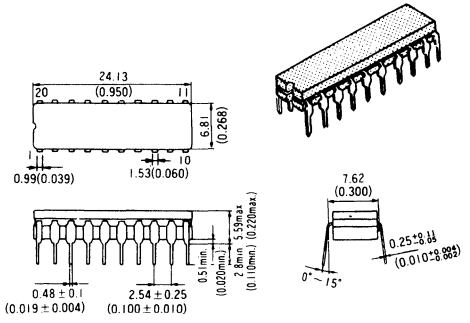

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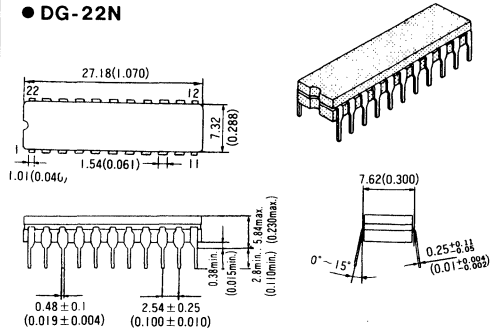
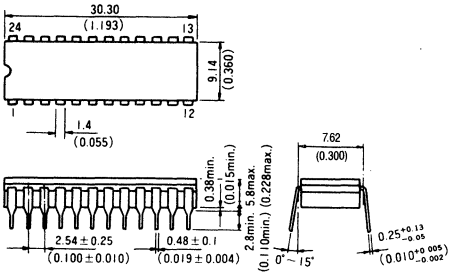
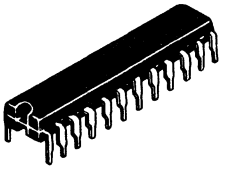


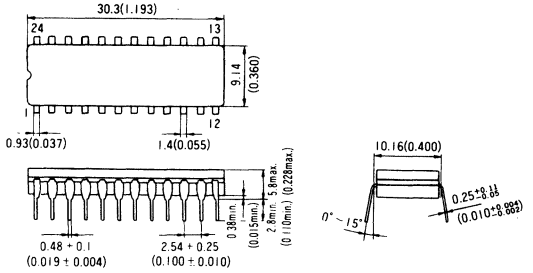
Unit: mm (inch) Scale 1/1

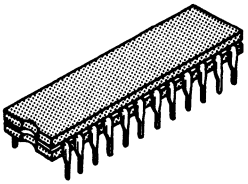
●DG-24A



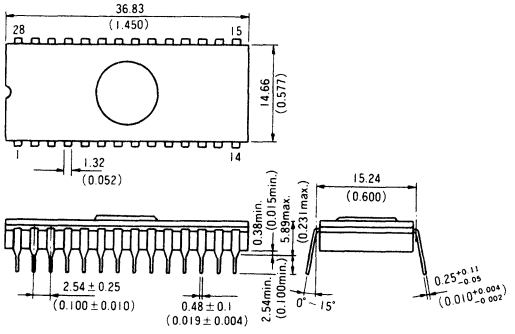


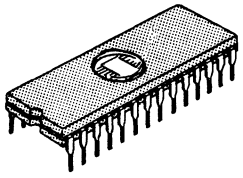
●DG-24N



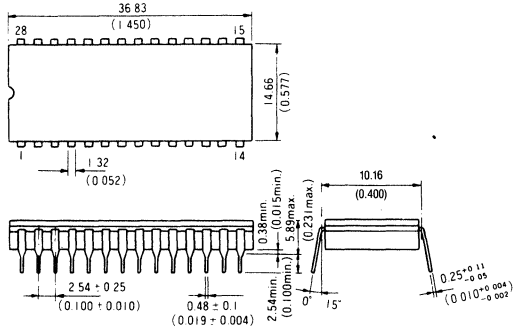


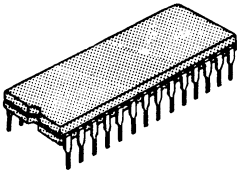
●DG-28



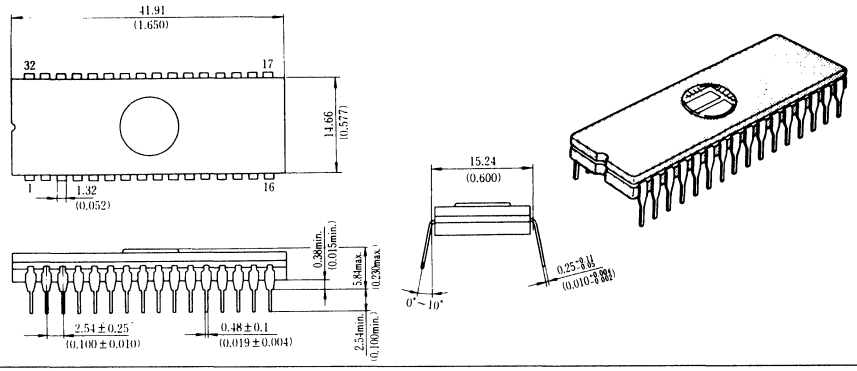


●DG-28A





● DG-32

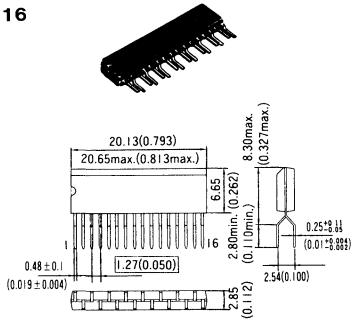


Applicable ICs

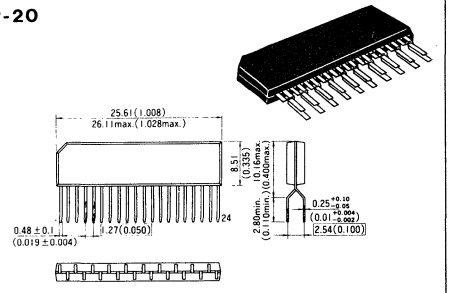
DG-16A	HM2112 Series, HM100415
DG-18	HM10470 Series, HM100470
DG-18A	HM511000 Series, HM511001 Series
DG-20NA	HM2142, HM10480 Series, HM10480L, HM100480
DG-22N	HM10490, HM100490
DG-24A	HM10422 Series, HM104747 Series, HM100422, HM100474 Series
DG-24N	HM6716 Series, HM6719 Series, HM6789 Series
DG-28	HN27128AG Series, HN27256G Series, HN27C256G Series, HN27C256AG Series, HN27C256HG Series, HN27512G Series
DG-28A	HM10484, HM100484
DG-32	HN27C101G Series, HN27C301G Series

● **Zigzag-in-line Plastic**

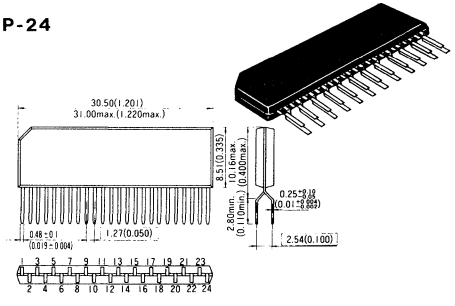
● ZP-16



● ZP-20



● ZP-24



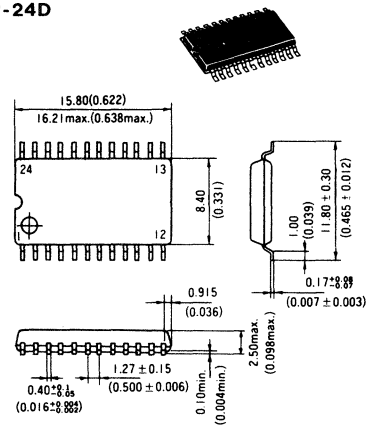
Applicable ICs

ZP-16	HM50256ZP Series, HM50257ZP Series, HM51256LZP Series, HM51256LZP Series
ZP-20	HM511000ZP Series, HM511000SZP Series, HM511001ZP Series, HM511001SZP Series, HM511002SZP Series, HM514256ZP Series, HM514258ZP Series
ZP-24	HM53461ZP Series, HM53462ZP Series

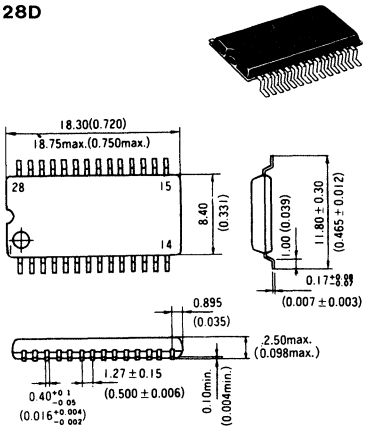
● Flat Package

Unit: mm (inch) Scale 1½

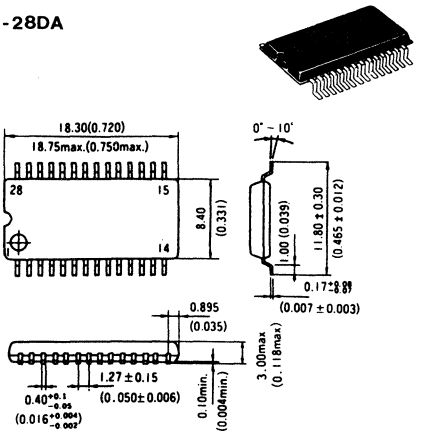
●FP-24D



●FP-28D



●FP-28DA



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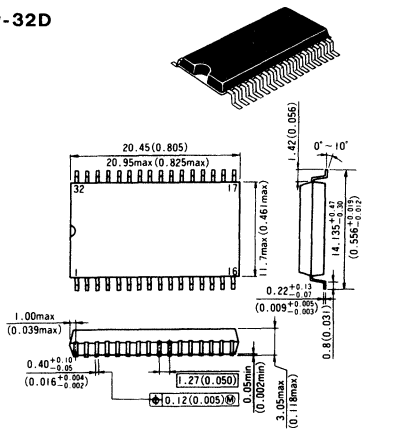
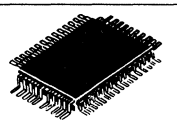
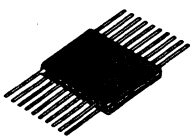


●FP-54

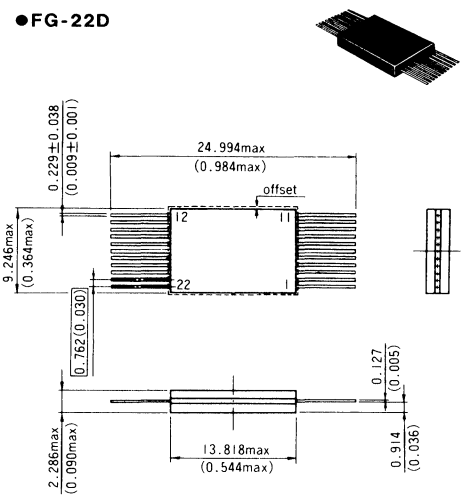


●FG-20D

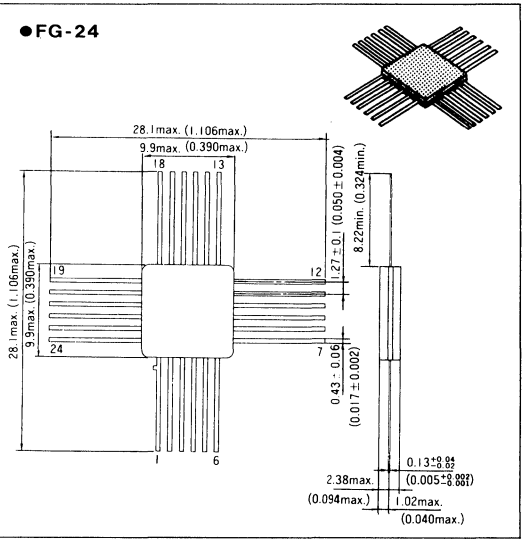


Unit: mm (inch) Scale 1½

●FG-22D



●FG-24

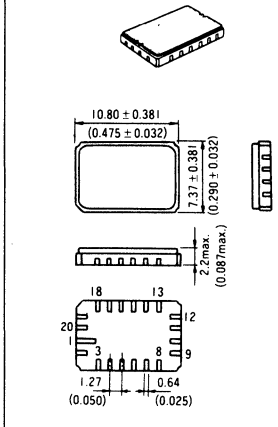


Applicable ICs

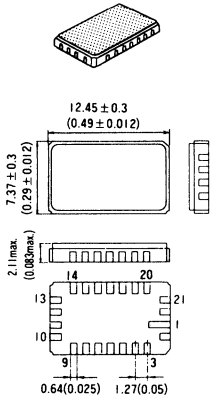
FP-24D	HM6116FP Series, HM6116LFP Series
FP-28D	HM6264FP Series, HM6264LFP Series, HM6264LFP-L Series, HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series
FP-28DA	HM6264FP Series, HM6264LFP Series, HM6264LFP-L Series, HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series, HM62256FP Series, HM62256LFP Series, HM65256BFP Series, HM65256BLFP Series, HN58C65FP, HN27C256FP Series
FP-32D	HM658128FP Series, HM658128LFP Series, HN27C101FP Series, HN27C301FP Series, HM628128FP Series, HM628128LFP Series
FP-54	HN61364FP, HN613128FP
FG-20D	HM10480F Series, HM100480F
FG-22D	HM10490F, HM100490F
FG-24	HM100422F, HM100474F Series

● CHIP CARRIER

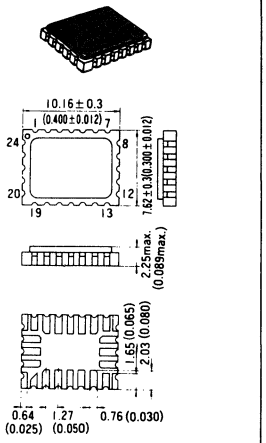
●CG-20



●CG-22A



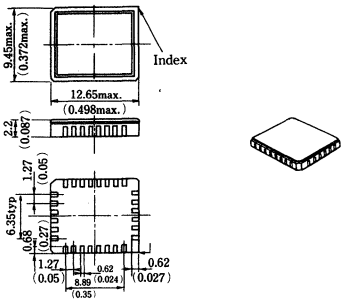
●CG-24



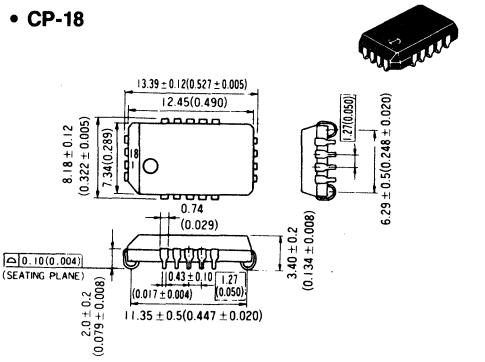
PACKAGE INFORMATION

Unit: mm (inch) Scale 1½

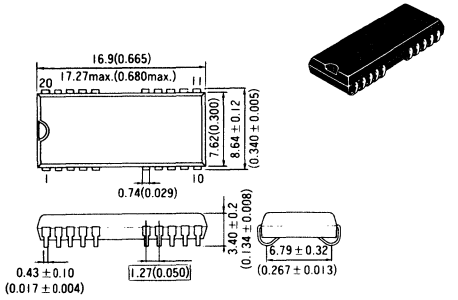
• **CG-28**



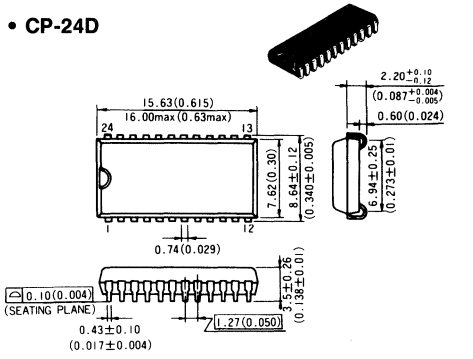
• **CP-18**



• **CP-20D**



• **CP-24D**



Applicable ICs

CG-20	HM6267CG Series
CG-22A	HM6287CG Series, HM6787CG Series, HM100490CG
CG-24	HM100422CG, HM100415CG
CG-28	HM10494LCG
CP-18	HM50464CP Series, HM50256CP Series, HM50257CP Series, HM51256CP Series, HM51256LCP Series, HM51258CP Series
CP-20D	HM511000JP Series, HM511000SJP Series, HM511001JP Series, HM511001SJP Series, HM511002SJP Series, HM514256JP Series, HM514258JP Series
CP-24D	HM6288JP Series, HM6789JP Series, HM6789HJP Series, HM6287HJP Series, HM67075JP Series, HM6708JP Series

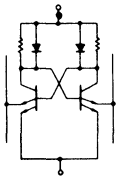
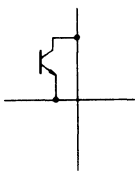
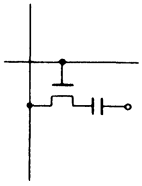
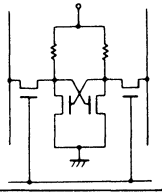
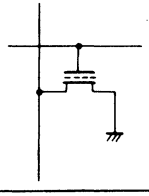
■ RELIABILITY OF HITACHI IC MEMORIES

1. STRUCTURE

IC memories are basically classified into bipolar type and MOS type and utilized effectively by their characteristics. The characteristic of bipolar memories is high speed but small capacity, instead, MOS memories have large capacity. There are also differences in circuit design, layout pattern, degree of integration, and manufacturing process. These memories have been produced with the standardized concept of design and inspection all through the processes of designing, manufacturing and inspection.

IC memories are constituted by the unit patterns called cells, which are integrated in high density. The knowhows based on our experience have been applied in every production stage. In addition, reliability has been ensured using TEG (Test Element Group) evaluation. Examples of cell circuits of bipolar and MOS memories are shown in Table 1.

● **Table 1 Basic Cell Circuit of IC Memories**

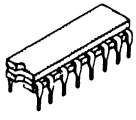
Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

Dies of IC memories are produced in various packages. In this process of packaging, Hitachi has also innovated new techniques and ensured to high level. As packages for IC memories, cerdip (glass-sealed) packages and plastic packages are currently used. Also such packages as LCC (Leadless Chip Carrier) or SOP (Small Outline Package) have been developed for high density packaging. Cerdip packages sealed hermetically are suitable for equipment requiring high reliability. Plastic packages are widely applied to many kinds of equipment. Hitachi plastic packages have been improved the reliability level as highly as that of the hermetically sealed packages. Table 2 shows the outlines of the Hitachi packages.

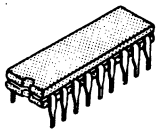
● **Table 2 IC Memory Package Outline**

■ Cerdip

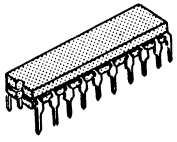
● 16 pin



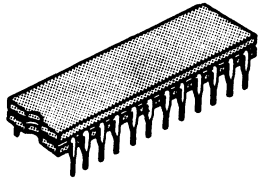
● 18 Pin



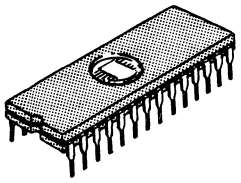
● 20 Pin



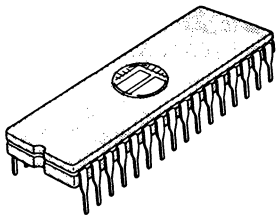
● 24 Pin



- 28 Pin with Lid

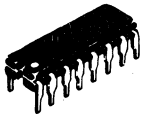


- 32 Pin with Lid

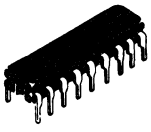


■ Plastic DIP

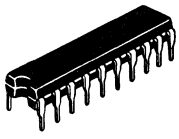
- 16 Pin



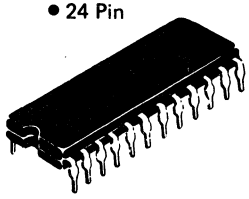
- 18 Pin



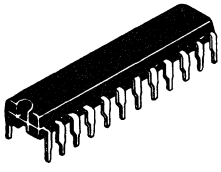
- 20 Pin



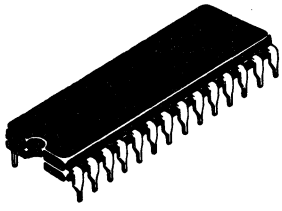
- 24 Pin



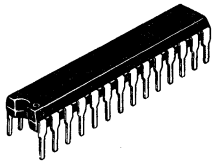
- 24 Pin



- 28 Pin



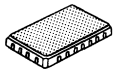
- 28 Pin



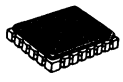
■ Leadless Chip Carrier

- 20 Pin

- 22 Pin

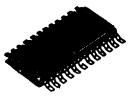


- 24 Pin

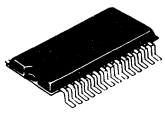


■ SOP

- 24 Pin

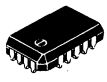


- 28 Pin



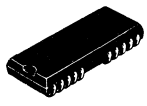
■ PLCC

- 18 Pin

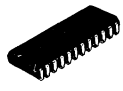


■ SOJ

- 26/20 Pin



- **24 Pin**



2. RELIABILITY Results of reliability tests are listed below.

2.1 Reliability Test Data on Bipolar Memories

The reliability test data on the bipolar memories are shown in Table 3 and 4. Since they are manufactured under the standardized design rules and quality control, there is no difference in reliability among the various types. And the larger the capacity is, the higher the reliability per bit becomes.

● **Table 3 Results on Bipolar Memory Reliability Test (1)**

Test item	HM10480 (Cerdip)					HM10470 (Cerdip)					HM100422 (Flat Package)				
	Test condition	samples	Total component hours	Failures	Failure rate* (1/hr)	Test condition	samples	Total component hours	Failures	Failure rate* (1/hr)	Test condition	samples	Total component hours	Failures	Failure rate* (1/hr)
High-temperature (Operating)	Ta=125°C V_{EE}=4.5V	40	C.H. 4.0×10^4	0	2.3×10^{-5}	Ta=125°C V_{EE}=-5.2V	125	C.H. 4.0×10^5	0	2.3×10^{-5}	Ta=150°C V_{EE}=-5.0V	80	C.H. 8.0×10^4	0	1.2×10^{-5}
	Ta=150°C V_{EE}=-4.5V	40	4.0×10^4	0	2.3×10^{-5}	Ta=150°C V_{EE}=-5.2V	80	2.7×10^5	0	3.4×10^{-2}					
High-temp. storage	Ta=150°C	80	8.0×10^4	0	1.2×10^{-5}	Ta=150°C	120	1.2×10^5	0	7.7×10^{-5}	Ta=150°C	80	8.0×10^4	0	1.2×10^{-5}

※Confidence level 60%

● **Table 4 Results on Bipolar Memory Reliability Test (2)**

Test item	Test condition	HM10480 (Cerdip)		HM10470 (Cerdip)		HM100422 (Flat Package)	
		Samples	Failure	Samples	Failures	Sample	Failures
Temperature cycling	−65°C~+150°C, 10 cycles	40	0	120	0	40	0
Soldering heat	260°C, 10 seconds	22	0	22	0	–	–
Thermal shock	0°C~+100°C, 10 cycles	30	0	36	0	20	0
Mechanical shock	1500G, 0.5ms, Three times each for X, Y and Z	30	0	30	0	60	0
Variable frequency	100~2000Hz, 200G, Three times each for X, Y and Z	40	0	40	0	60	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	40	0	60	0

2.2 Reliability test data on MOS memories

2.2.1 Reliability test data on MOS DRAM and SRAM

Table 5 and table 6 shows the reliability test data on the representative types of 256k DRAM (HM50256P), 1M DRAM (HM511000P), 64K SRAM (HM6264P), 256k SRAM (HM62256P).

The life test is performed at high temperature and high voltage to evaluate the reliability of products using fewer samples. All failures are caused in manufacturing process, so we feedback the data into manufacturing process to improve the quality and reliability.

● **Table 5 Reliability Data on 256K and 1M DRAM**

Test item	Test condition	HM50256P (Plastic)				HM511000P (Plastic)				Remaks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total test time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	150°C/8V	180	0.44×10^6	2*1	7.05×10^{-6}	–	–	–	–	*1 Oxide film Failure ×2
	150°C/7V	300	0.60×10^6	0	1.53×10^{-6}	150	0.3×10^6	0	3.07×10^{-6}	*2 Oxide film Failure ×3 PSG failure ×2
	125°C/8V	1100	1.28×10^6	5*2	4.89×10^{-6}	–	–	–	–	*3 Al corrosion ×1
	125°C/7V	15477	1.66×10^6	0	5.53×10^{-7}	2338	0.70×10^6	1*4	2.89×10^{-6}	*4 Oxide film Failure ×1
	125°C/5.5V	380	1.32×10^6	0	6.96×10^{-7}	300	0.60×10^6	0	1.53×10^{-6}	
Moisture endurance	85°C 85% RH5.5V	680	1.92×10^6	1*3	1.05×10^{-6}	300	0.60×10^6	0	1.53×10^{-6}	
Pressure cooker	121°C/100% RH	260	0.13×10^6	0	7.07×10^{-6}	100	0.03×10^6	0	3.07×10^{-5}	

● **Table 6. Reliability Data on 64K and 256K SRAM**

Test item	Test condition	HM6264P (plastic)				HM62256P (plastic)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total test time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	150°C/7V	100	0.10×10^{6}	1*1	2.02×10^{-5}	206	0.41×10^{6}	1*4	4.90×10^{-6}	* 1-3 Foreign material ×2 PSG failure ×1 crystal failure ×1 *4 PSG failure ×1 *5 PSG failure ×1 Foreign material ×1
	125°C/8V	162	0.20×10^{6}	2*2	1.55×10^{-5}	1394	0.84×10^{6}	3*5	4.96×10^{-6}	
	125°C/7V	1014	1.16×10^{6}	2*3	2.67×10^{-6}	2578	0.69×10^{6}	0	1.34×10^{-6}	
	125°C/5.5V	–	–	–	–	12748	0.61×10^{6}	0	1.50×10^{-6}	
Moisture endurance	85°C/85% RH 7V	304	0.30×10^{6}	0	3.07×10^{-6}	540	1.08×10^{6}	0	5.52×10^{-7}	
Pressure cooker	121°C/ 100%RH	55	2.20×10^{4}	0	4.18×10^{-5}	180	5.40×10^{4}	0	1.70×10^{-5}	

* Confidence level 60%

2.2.2 Reliability Test Data on EPROM

EPROM has two types; conventional EPROM with transparent window and one time programmable ROM (OTPROM) packaged in plastic package. Table 7 shows reliability test data on the representative EPROM types of 256k EPROM (HN27256, HN27256P), 1M EPROM (HN27C101, HN27C301).

● **Table 7. Reliability Data on 256K and 1M EPROM**

Test item	Test condition	HN27256 (Cerdip/Plastic)				HN27C101/HN27C301				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total test time	Failures	Failure rate* (1/hr)	
High-temp. pulse operation	125°C/5.5V	240	0.32×10^{6}	0	2.88×10^{-6}	–	–	–	–	*1 Data dissipation ×67
	125°C/7V	832	0.52×10^{6}	0	1.78×10^{-6}	206	0.16×10^{6}	0	5.90×10^{-6}	
High-temperature bake	200°C	280	2.80×10^{5}	1*1	7.21×10^{-6}	80	1.05×10^{5}	0	8.76×10^{-6}	
	250°C	220	2.20×10^{5}	9*1	4.75×10^{-5}	80	1.05×10^{5}	4*1	4.99×10^{-5}	
	300°C	86	0.43×10^{5}	53*1	1.23×10^{-3}	–	–	–	–	
Moisture endurance	85°C/85% RH 5V	225	0.23×10^{6}	0	4.09×10^{-6}	–	–	–	–	Data of 256k OTPROM
Pressure cooker	121°C/ 100% RH	60	0.12×10^{5}	0	7.67×10^{-5}	–	–	–	–	

* Confidence level 60%.

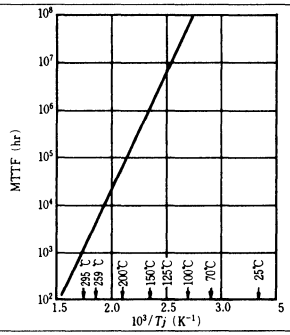
The failure shown in table 7 is due to the data dissipation in memory cells. Getting thermal energy, electrons in memory cells are activated and go through the floating gate. In actual usage, however, it has no problem because this phenomenon dependes on temperature (about 1.0eV of activated energy) greatly. The moisture resistance of OTPROM is also satisfactory.

Table 8 shows the example of PROM derating. When derating, the parameter is generally only the temperature because other operating conditions are specified. Especially to lower the junction temperature during mounting is important for stabilizing the operation relative to access time, refresh time and other characteristics.

- **Table 8 Example of EPROM Derating**

Factor	Temperature
Failure criteria	Electrical Characteristics, Function Test
Failure mechanism	Increase of leak current and others

Results:
The result from high temperature baking of PROM is shown in the right figure.



Note: Decreasing junction temperature shown in the figure will promise the higher reliability. The junction temperature can be calculated by a formula : $T_j = T_a + \theta_{ja} \cdot P_d$ θ_{ja} in about 100°C/W with no air flow and about 60 to 70°C/W with 2.5 m/s air flow.

2.2.3 Reliability Data on MASK ROM

Table 9 shows the reliability test data on 256k and 1M bit MASK ROM. MASK ROM is patterned according to ROM information in manufacturing process, so data dissipation isn't occurred in high temperature like EPROM and EEPROM.

- **Table 9. Reliability Data on 256K and 1M MASK ROM**

Test item	Test condition	HN613256P (Plastic)				HN62301P (Plastic)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total test time	Failures	Failure rate* (1/hr)	
High-temp. pulse operaton	125°C/5.5V	90	0.9×10^5	0	1.02×10^{-5}	–	–	–	–	
	125°C/7V	50	0.5×10^5	0	1.84×10^{-5}	246	2.46×10^5	0	3.74×10^{-6}	
Moisture endurance	85°C/85% RH 5V	120	1.2×10^5	0	7.67×10^{-5}	120	1.20×10^5	0	7.67×10^{-6}	
Pressure cooker	121°C/ 100% RH	80	0.8×10^4	0	1.15×10^{-4}	78	1.56×10^4	0	5.90×10^{-5}	

* Confidence level 60%.

2.2.4 Reliability Data on MOS Memory (The result of environment test)

Table 10 shows examples of each environment test data. They show good results without any failure even in severe environment.

V_{TH} of MOS transistor is one of the basic process parameters in MOS memory, which has almost no change using surface stabilization technology and clean process. Table 2 shows the examples of time changes for 256K DRAM; Vcc min. (V_{min}) and access time (t_{RAC}) in high temperature pulse test.

- **Table 10 Reliability Data on MOS Memories**

Test item	Test condition	HM50256P (Plastic)		EPROM (Cerdip)		HM511000P (Plastic)		HM6264P (Plastic)		HM62256P (Plastic)		Remarks
		Samples	Failure	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	-55°C~150°C 10 cycle	4680	0	2334	0	2238	0	3315	0	828	0	
Temperature cycling	-55°C~150°C 500 cycle	540	0	260	0	200	0	150	0	318	0	
Thermal shock	-65°C~150°C 15 cycle	38	0	210	0	50	0	76	0	55	0	
Soldering heat	260°C, 10 seconds	22	0	50	0	50	0	76	0	77	0	
Mechanical shock	1,500G, 0.5ms	–	–	38	0	–	–	–	–	–	–	
Variable frequency	100~2,000Hz 20G	–	–	38	0	–	–	–	–	–	–	
Constant-acceleration	20,000G	–	–	38	0*	–	–	–	–	–	–	*6,000G

2.3 Change of Electrical Characteristics on IC Memory

The degradation of I_{CBO} and h_{FE} are the main factors of degradation in inner cell transistor of bipolar memory. In actual element designing, however, it is designed to operate in the range at which no degradation happen. Therefore no change of characteristics including access time are observed. Time dependence in access time for HM10470 are shown in Fig. 1.

Fig. 1 Time Dependence in Access Time for HM10470

Example	
Device name	HM10470
Test condition	Ta=125°C, V_{EE}=-5.2V
Failure criteria	t_{AA}=25ns
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Example of time change in access time for Bipolar memory

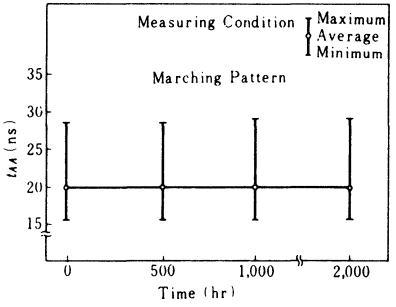


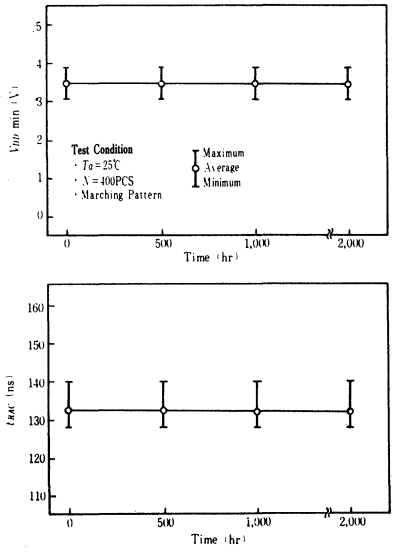
Fig. 2 Time Dependence in V_{DD} min and t_{RAC} for HM50256

Example	
Device name	HM511000P
Test condition	V_{CC}=7V, T_a=125°C, all bit scanning
Failure criteria	V_{DD}=4.5V, ΔV_{BB}=1.0V
Failure mechanism	Surface degradation

Results:
Both of V_{DD} (min) and t_{RAC} are stabilized.

Note: Test accuracy is 0.2V, 2ns.

Examples of time change in access timer for MOS memory



2.4 Failure Mode Rate

Figure 3 and 4 show examples of failure mode happened in users' application. Since IC memories require the finest pattern process technology, the percentage of failures, such as pinholes, defects on photoresist and foreign materials, tends to increase. To eliminate the defects in the manufacturing process, Hitachi has improved the process and performed 100% burn in screening under high tem-

perature. Hitachi has been collecting and checking customers' process-data and marketing data for higher reliability of our products. To analyze them is very helpful for the improvement of designing and manufacturing.

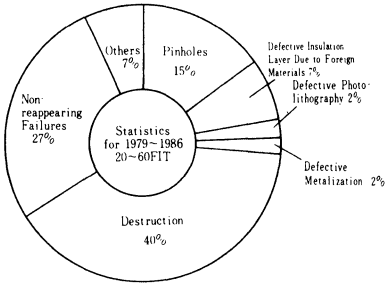


Fig. 3 Failure Mode Rate of Bipolar Memory

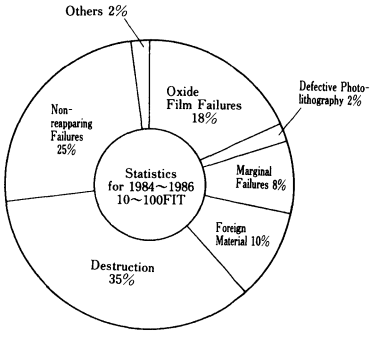


Fig. 4 Failure Mode Rate of MOS Memory

3. SOFT ERROR

3.1. Reliability Characteristics for Semiconductor Devices

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along proper environmental conditions. This section describes reliability characteristics, failure types and their mechanisms in terms of devices. First, semiconductor device characteristics are examined in light of their reliability.

(1) Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.

(2) Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

(3) Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.

(4) Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data cannot be used in some cases.

(5) Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.

(6) Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should be also reviewed when electrode and package materials are not suited for particular environmental conditions.

(7) Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

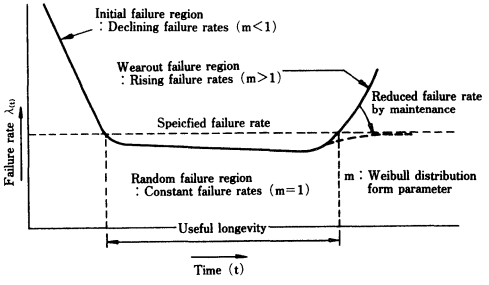


Fig. 5 Typical failure rate curve

Device reliability is generally represented by the failure rate. 'Failure' means that a device loses its function, including intermittent degradation as well as complete destruction.

Generally, the failure rate of electric components and equipment is represented by the

bathtub curve shown in Fig. 5. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

3.2 Failure Types and Their Mechanisms

3.2.1 Failure physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering". It is used to examine the physical mechanism of failures in terms of atoms and molecules to improve device reliability. This physical approach was introduced to the reliability field with the demand for minimized development cost and period, as technology rapidly developed and system performance increased, requiring more complex and higher levels of reliability. These conditions derived from the development of solid state physics (semiconductor physics) after World War II and associated device development.

Failure physics have been employed to:

1) Detect failed devices as soon as possible
2) Establish models and equation used for failure prediction
3) Evaluate reliability in short periods by accelerated life test

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage and usage by adding physics as a basic technology to conventional experimental and statistical approaches.

3.2.2 Failure types and their mechanism

Device failures are physically discussed in this section. Semiconductor device failures are basically categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These failures and their causes are summarized in Table 11. Typical failure mechanisms are reviewed next.

(1) Surface Deterioration

The pn junction has a charge density of 10^{14} – 10^{20}/cm^3. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to a depletion layer, electric characteristics of the junction tend to be easily varied. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model.

One example of recent failures is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS} by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 3 μm to 1.3 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have employed improved design and process techniques to prevent these problems. However, as process becomes finer, surface deterioration may possibly become a serious problem.

(2) Electrode-related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticeable failures include electromigration and Al wiring corrosion in plastic sealed packages.

① Electromigration

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with current of about scattering electrons, an 'electron wind' is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

② Multi-metal line related failures

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

③ Al line corrosion and disconnection

When Plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Fig. 6). Under high-temperature and high-humidity, corrosions are randomly

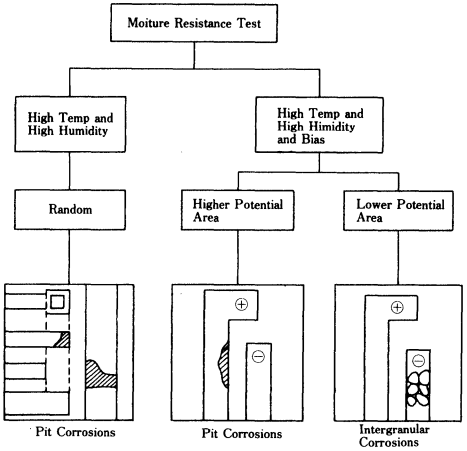


Fig. 6 Categorized Al corrosion mode

generated over the element surface. However, after an extended period of time, the corrosions have not significantly increased. Accordingly, this failure is possibly due to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-appllied, high-temperature, high-humidity condition, on the other hand, corrosions are generated in higher potential areas while in lower potential areas, grain corrosion

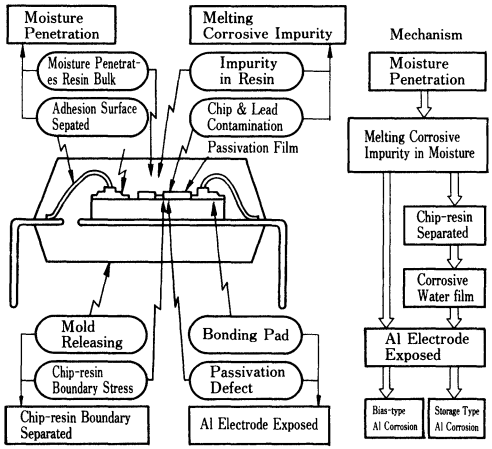


Fig. 7 Plastic package cross section and Al corrosion mechanism

occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Fig. 7.

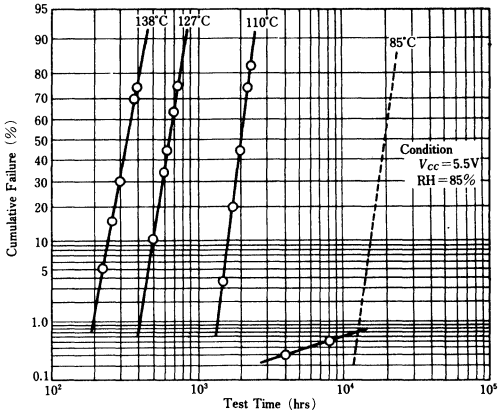


Fig. 8 An Example of Moisture Resistance by High temp. and High humidity and bias

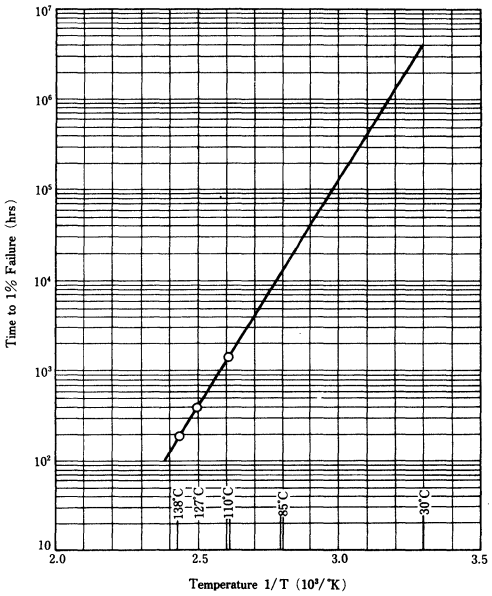


Fig. 9 Relationship between temperature and Time to 1% failure

(3) Bonding related failures

① Degradation caused by intermetallic formation

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi

products are subjected to a lower-temperature, shorter-period bonding whenever possible.

② Wire creep

Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

③ Chip crack

With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

④ Reduced maximum power dissipations

For power devices, heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance. This results in decreased maximum power dissipations.

(4) Sealing related failures

Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between the different ionized materials.
2. Intermittent moving foreign metals short
3. Al line corrosion due to extraneous H_2O caused by hermetic failure

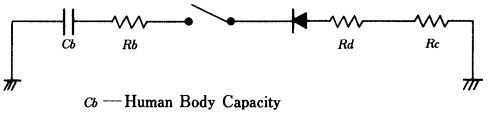
Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parastic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying.

(5) Disturbance

①Electrostatic discharge destruction

Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure; the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Fig. 10. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged with 2000V, the dissipated energy is obtained as follows: With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.



Cb — Human Body Capacity
Rb — Human Body Resistance
Rd — Device Resistance
Rc — Resistance Between Device and Ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} J$$

Fig. 10 Equivalent circuit of human body model

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Fig. 11. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction. 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high-frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

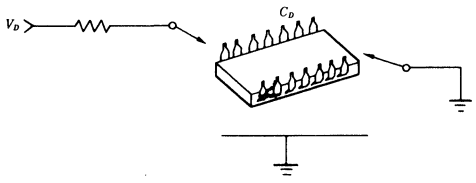


Fig. 11 Equivalent circuit of charging model

2 Latch up

Latch up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply and noise is applied, or when a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parasitic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is off or the flowing current is forced to be reduced to a certain level. Once latch up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch up. Latch up triggering input or output currents start to flow under the following conditions.

Vin <Vcc or Vin < GND for input level

Vout > Vcc or Vout < GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

③ Soft errors

When α particles are generated from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating nodes, causing temporary soft errors. This phenomenon is shown in Fig. 12. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, organic material, PIQ, is applied to the surface of the device.

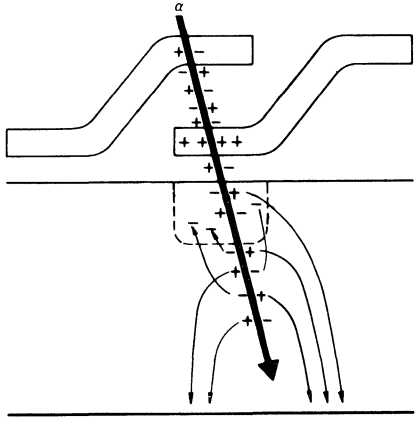


Fig. 12 Soft error caused by α particles in dynamic memory

Table 11 Failure causes and mechanism

Failure related causes		Failure mechanisms	Failure modes
Passivation	Surface oxide film, Insulating film between wires	Pin hole, Crack, Uneven thickness, Contamination, Surface inversion, Hot carrier injected	Withstanding voltage reduced, Short, Leak current increased, h_{FE} degraded, Threshold voltage variation, Noise
Metallization	Interconnection, Contact, Through hole	Flaw, Void, Mechanical damage, Break due to uneven surface, Non-ohmic contact, Insufficient adhesion strength, Improper thickness, Electromigration, Corrosion	Open, Short, Resistance increased

Failure related causes		Failure mechanisms	Failure modes
Connection	Wire bonding, Ball bonding	Bonding runout, Compounds between metals, Bonding position mismatch, Bonding damaged	Open, Short Resistance increased
Wire lead	Internal connection	Disconnection, Sagging, Short	Open, Short
Diffusion, Junction	Junction diffusion, Isolation	Crystal defect, Crystallized impurity, Photo resist mismatching	Withstanding voltage reduced, Short
Die bonding	Connection between die and package	Peeling chip, Crack	Open, Short, Unstable operation, Thermal resistance increased
Package sealing	Packaging, Hermetic Seal, Lead plating, Hermetic pakage & plastic package, Filler gas	Integrity, moisture ingress, Impurity gas, High temperature, Surface contamination, Lead rust, Lead bend, break	Short, Leak current Increased, Open, Corrosion disconnection, Soldering failure
Foreign matter	Foreign matter in package	Dirt, Conducting foreign matter, Organic carbide	Short, Leak current increased
Input/output pin	Electrostatistics, Excessive Voltage, Surge	Electron destroyed	Short, Open, Fusing
Disturbance	α particle	Electron hole generated	Soft error
	High electric field	Surface inversion	Leak current increased

(6) Fine geometry related problems

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 5 μm → 3 μm → 1.3 μm. However power supply has not been scaled down used for 5V, only line dimensions have been fined increasingly. Problems associated with finer geometry are shown in Table 12.

Table 12 Finer geometry related problems

Item	Problems	Countermeasure
5V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering • Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical & horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

■ QUALITY ASSURANCE OF IC MEMORY

1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are to meet individual users' purpose and their required quality level and also to maintain the satisfied level for general application. Hitachi has made efforts to assure the standardized reliability of our IC memories in actual usage. To meet users' requests and to cover expanding application, Hitachi performs the followings;

(1) Establish the reliability in design at the stage of new product development.
(2) Establish the quality at all steps in manufacturing process.
(3) Intensify the inspection and the assurance of reliability of products.
(4) Improve the product quality based on marketing data.

Furthermore, to get higher quality and reliability, we cooperate with our research laboratories.

With the views and methods mentioned above, Hitachi makes the best efforts to meet the users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Target

Establishment of reliability target is important in manufacturing and marketing as well as function and price. It is not practical to determine the reliability target based on the failure rate under single common test condition. So, the reliability target is determined based on many factors such as each characteristics of equipment, reliability target of system, derating applied in design, operating condition and maintenance.

2.2 Reliability Design

Timely study and execution are essential to achieve the reliability based on reliability targets. The main items are the design standardization, device design including process and structural design, design review and reliability test.

(1) Design Standardization
Design standardization needs establishing design rules and standardizing parts, material, and process. When design rules are established on circuit, cell, and layout design, critical items about quality and reliability should be examined. Therefore, in using standardized process or material, even newly developed products would have high reliability, with the exception of special requirement on function.

(2) Device Design
It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in case of applying new process or new material, we study the technology prior to development of the device in detail.

(3) Reliability Test by Test Site
Test site is sometimes called Test Pattern. It is useful method for evaluating reliability of designing and processing ICs with complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode;
   - Analysis of relation between failure mode and manufacturing process condition.
   - Analysis of failure mechanism.
   - Establishment of QC point in manufacturing.
2. Effects of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and compared with the process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

2.3 Design Review

Design review is a method to confirm systematically whether or not design satisfies the performance required including by users, follows the specified ways, and whether or not the technical items accumulated in test data and application data are effectively applied.

In addition, from the standpoint of competition with other products, the major purpose of design review is to insure quality and reliability of the product. In Hitachi, design review is performed in designing new products and also in changing products.

The followings are the items to consider at design review.

(1) Describe the products based on specified design documents.
(2) Considering the documents from the standpoint of each participant, plan and execute the subprogram such as calculation, experiments and

investigation if unclear matter is found.

(3) Determine the contents and methods of reliability test based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Arrange the preparation for production.

(6) Plan and execute the sub-programs of design changes proposed by individual specialists, for tests, experiments and calculation to confirm the design change.

(7) Refer to the past failure experiences with similar devices, confirm the prevention against them, and plan and execute the test program for confirmation of them.

In Hitachi, these study and decision at design review are made using the individual check lists according to its objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

The following items are the general views of overall quality assurance in Hitachi;

(1) Problems is solved in each process so that even the potential failure factors will be removed at final stage of production.

(2) Feedback of information is made to insure satisfied level of process ability.

As the result, we assure the reliability.

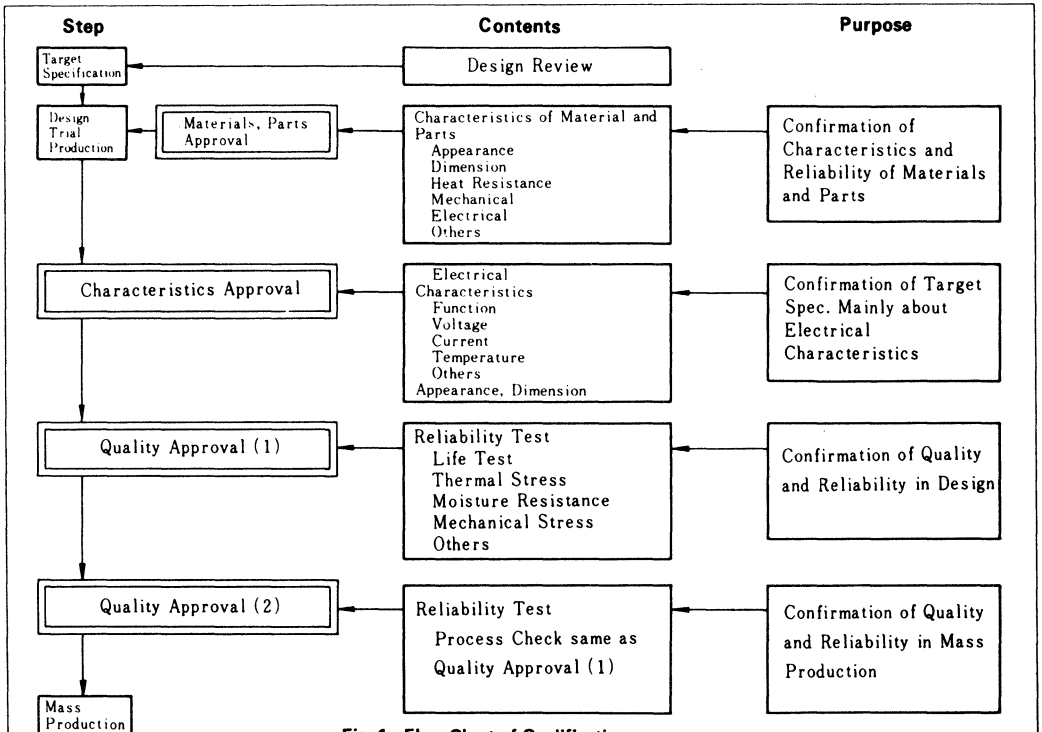


Fig. 1 Flow Chart of Qualification

3.2 Qualification

To assure the quality and reliability, the qualification tests are done at each stage of trial production and mass production based on the reliability design described in section 2.

The followings are the views on qualification in Hitachi:

(1) From the standpoint of customers, qualify the products objectively by a third party.
(2) Consider the failure experiences and data from customers.
(3) Qualify every change in design and work.
(4) Qualify intensively on parts and materials and process.
(5) Considering the process ability and factor of manufacturing fluctuation, establish the control points in mass production.

Considering the views mentioned above, qualification shown in Fig. 1 is done.

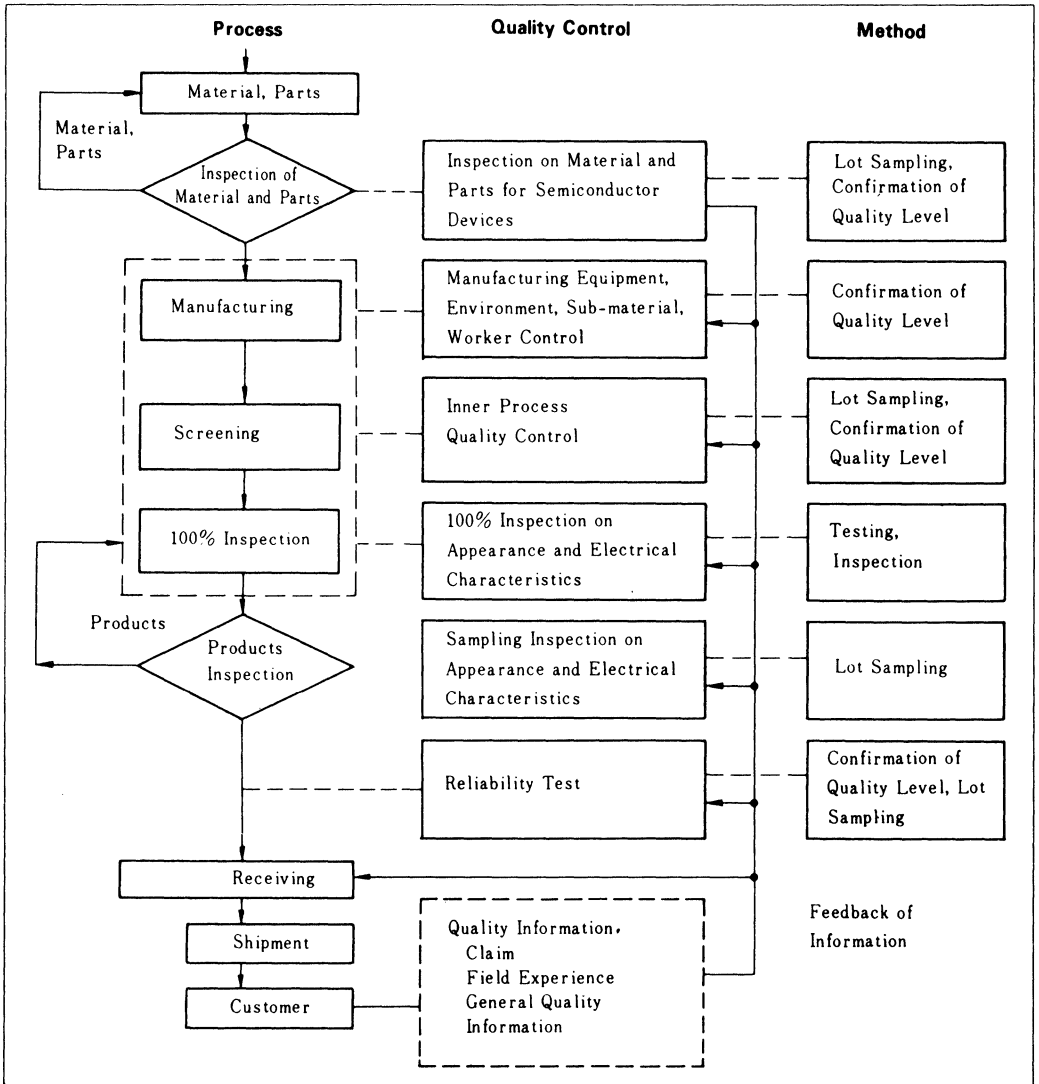


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

3.3 Quality and Reliability Control in Mass Production

To assure quality in mass production, quality is controlled functionally by each department, mainly by manufacturing department and quality assurance department. The total function flow is shown in Fig. 2.

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, quality control of parts and materials becomes more important. The items such as crystal, lead frame, fine wire for wire bonding, package and materials required in manufacturing process like mask pattern and chemicals, are all subject to inspection and control.

Besides qualification of parts and materials stated in 3.2, quality control of parts and materials is defined in incoming inspection. Incoming inspection is performed based on its purchase specification, drawing and mainly sampling test based on MIL-STD-105D. The other activities for quality assurance are as follows.

- **Table 1. Quality Control Check Points of Parts and Material (example)**

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

(1) Technology Meeting with Vendors
(2) Approval and Guidance of Vendors
(3) Analysis and tests of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

To control inner process quality is very significant for quality assurance of devices. The quality control of products in every stage of production is explained below. Fig. 3 shows inner process quality control.

(1) Quality Control of Products in Every Stage of Production

Potential failure factors of devices should be removed in manufacturing process. Therefore, check points are set up in each process so as not to move the products with failure factors to the next process. Especially, for high reliability devices, manufacturing lines are rigidly selected in order to control the quality in process. Additionally we perform rigid check per process or per lot, 100% inspection in proper processes so as to remove failure factors caused by manufacturing fluctuation, and screenings depending on high temperature aging or temperature cycling. Contents of controlling quality under processing are as follows:

- Control of conditions of equipment and workers and sampling test of uncompleted produsts.
- Proposal and execution of working improvement.
- Education of workers
- Maintenance and improvement of yield
- Picking up of quality problems and execution of countermeasures toward them.
- Communication of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing facilities have been developed with the need of higher devices in performance and the automated production. It is also important to determine quality and reliability.

In Hitachi, automated manufacturing is promoted to avoid manufacturing fluctuation, and the operation of high performance equipment is controlled to function properly.

As for maintenance inspection for quality control, daily and periodically inspections are performed based on specification on every check point.

As for adjustment and maintenance of measuring equipment, the past data and specifications are clearly checked to keep and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-material.

Quality and reliability of devices are affected especially by manufacturing process. Therefore, we thoroughly control the manufacturing circumstances such as temperature, humidity, dust, and the sub-materials like gas or pure water used in manufacturing process.

Dust control is essential to realize higher integration and higher reliability of devices. To maintain and improve the clearness of manufacturing site, we take care buildings, facilities, air-conditioning system, materials, clothes and works. Moreover, we periodically check on floating dust in the air, fallen dust or dirtiness on floor.

Process		Control Point		Purpose of Control
	▽ Purchase of Material			
Wafer		Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
	○ Surface Oxidation	Oxidation		Assurance of Resistance
	○ Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
	○ Photo Resist	Photo Resist		
	○ Inspection on Photo Resist		Dimension, Appearance	Dimension Level
	◇ PQC Level Check			Check of Photo Resist
	○ Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
	○ Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
	◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	
	○ Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
	○ Inspection on Evaporation			
	◇ PQC Level Check			
	○ Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
	○ Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
	○ Chip Scribe		Appearance of Chip	
	○ Inspection on Chip Appearance			
	◇ PQC Lot Judgement			
Frame				
	○ Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
			Appearance after Wire Bonding	Quality Check of Wire Bonding
	◇ PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
	○ Inspection after Assembling		Appearance after Assembling	
	◇ PQC Lot Judgement			
Package				
	○ Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
	◇ PQC Level Check	Marking	Marking Strength	
	○ Final Electrical Inspection			
	◇ Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
	○ Appearance Inspection			
	△ Sampling Inspection on Products			
	○ Receiving			
	Shipment			

Fig. 3 Example of Inner Process Quality Control

3.3.3 Final Tests and Reliability Assurance

(1) Final Tests

Lot inspection is done by quality assurance department for the product passed in 100% test in final manufacturing process. Though 100% of passed products is expected, sampling inspection is subjected to prevent mixture of failed products by mistake. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Our lot inspection is based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability, the reliability tests are performed periodically, and performed on each manufacturing lot if user requires.

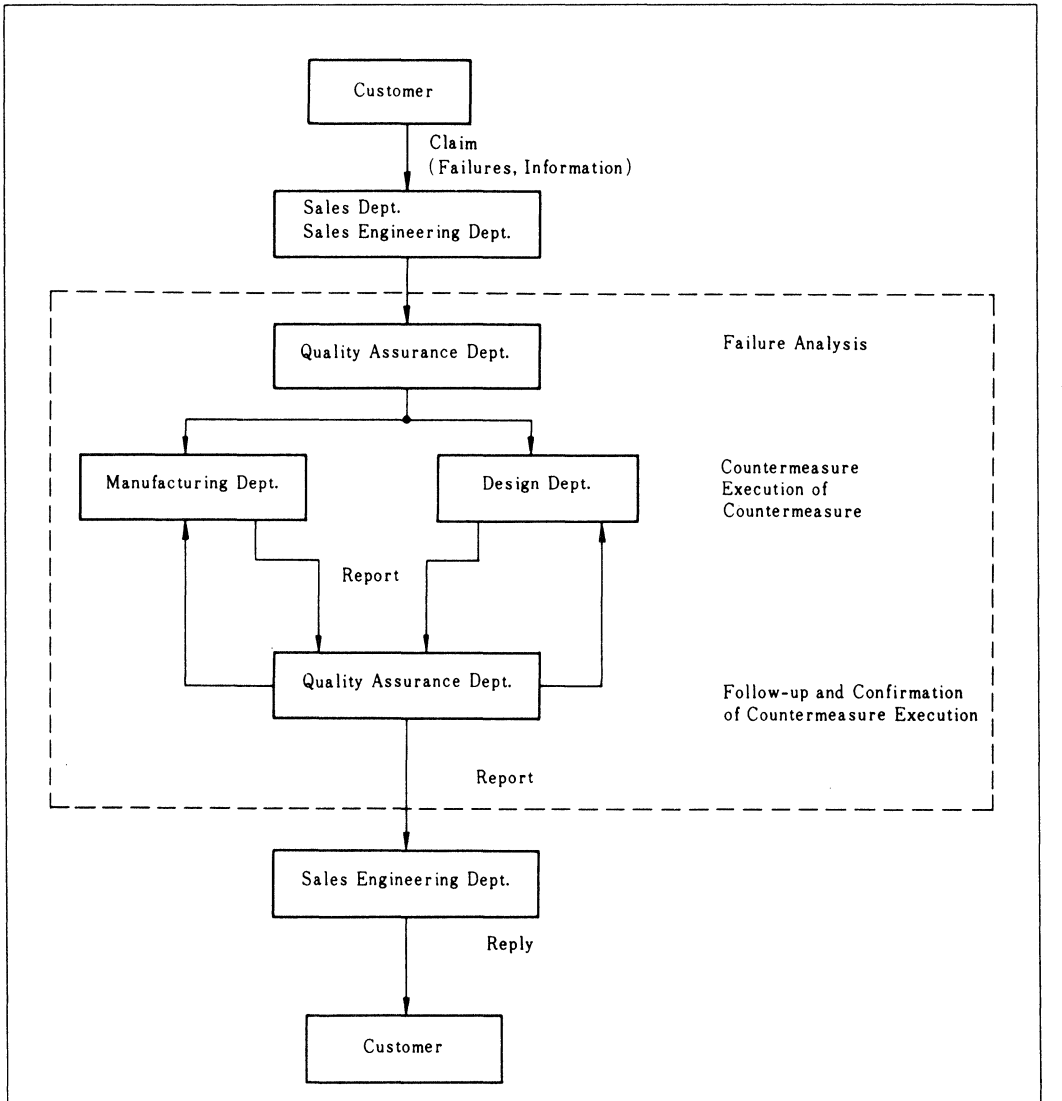


Fig. 4 Process Flow Chart of Coping with Failure to a Cutomer

■ OUTLINE OF TESTING METHOD

1. INSPECTION METHOD

Compared to conventional core memories, IC memories contain all peripheral circuits, such as the decoder circuit, write circuit and read circuit. As a result, assembly and electrical inspection of ICs are all performed by IC manufacturers. Consequently, as the electrical inspection of IC memories are becoming more systematic, conventional IC inspection facilities are becoming useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a simple DC parameter facility. However, when the address input becomes multiplexed as in 16K, 64K and 256K memory, even the generation of the function test pattern becomes a serious problem.

In the memory IC inspection, its quality cannot be judged by DC test on external pins only, because the number of the element such as transistor which can be judged in the DC test is only 1/1000 of all elements. The followings are the address patterns proposed to inspect whether the internal circuits are functioning correctly.

(1) All "Low", All "High"
(2) Checker Flag
(3) Stripe Pattern
(4) Marching Pattern
(5) Galloping
(6) Waling
(7) Ping-Pong

Those are not all, but only representative ones. There are the pattern to check the mutual interference of bits and the pattern for the maximum power dissipation. Among the above mentioned patterns, those of (1) to (4) are called N pattern, which can check one sequence of N bit IC memory with the several times of N patterns at most. Those of (5) to (7) are called N^2 pattern, which need several times of N^2 patterns to check one sequence of N bit IC memory. Serious problem arises in using N^2 pattern in a large-capacity memory. For example, inspection of 16K memory with galloping pattern takes a lot of time – about 30 minutes. (1), (2) and (3) are rather simple and good methods, however, they are not perfect to find any failure in decoder circuits. Marching is the most simple and necessary pattern to check the function of IC memories.

2. MARCHING PATTERN

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits of "0"s. For example, a simple addressing of 16 bit memory is described below.

(1) Clear all bits . . . . . See Fig. 1 (a)
(2) Read "0" from 0th address and check that the read data is "0". Hereafter, "Read" means "checking and judging data"
(3) Write "1" on 0th address. . . . . See Fig. 1(b)
(4) Read "0" from 1st address.
(5) Write "1" on 1st address.
(6) Read "0" from nth address.
(7) Write "1" on nth address . . . . . See Fig. 1(c)
(8) Repeat (6) to (7) to the last address. Finally, all data will be "1".
(9) After all data become "1", repeat from (2) to (8) replacing "0" and "1".

In this method, 5N address patterns are necessary for the N-bit memory.

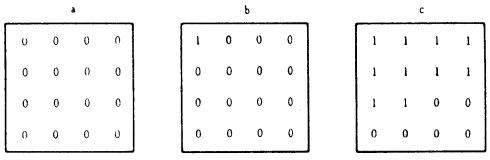


Fig. 1 Addressing method of for 16 bit memory in the Marching pattern

3. GENERATION OF MARCHING PATTERN

The simple method of generating the marching pattern and displaying failure bits of the memory on the braun tube will be introduced. Fig. 2 shows the block diagram. The address pattern is generated using four synchronous 4 bit counters. Fig. 4 shows the entire pulse relations. This example is for 16K bit memory and shows that A14, which has a half frequency of A13, is the same as the data inputs. A15 signal, together with the carrier signal of HD74161, is used to determine the termination of the sequence.

As shown in Fig. 2, in the read and write cycles after clearing all bits, addressing is twice the period of clearing. This switching is performed at the binary gate, following the reference pulse generating circuit. Output of HD74161 is input to D/A converter and input to the oscilloscope as an analogue signal of X-Y matrix. The output of the comparator circuit is input to the Z axis and performed lumi-

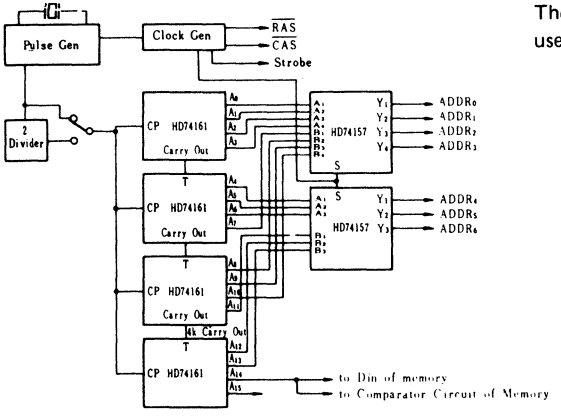


Fig. 2 Marching Pattern Generating Circuit

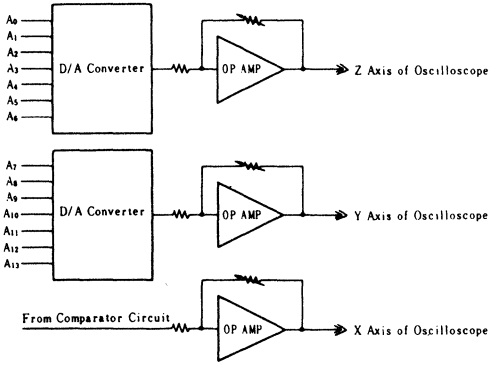


Fig. 3 Fail Bit Map Dilplay Circuit

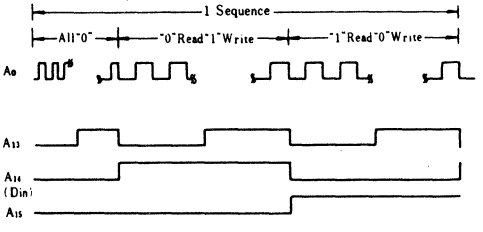
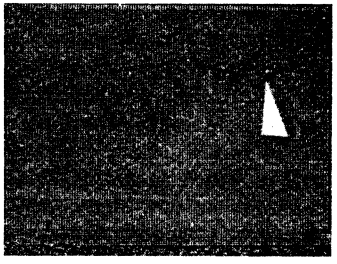


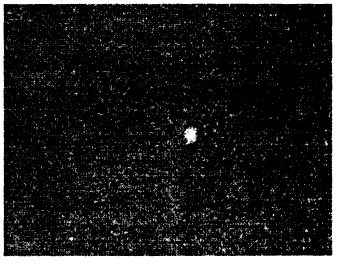
Fig. 4 Entire Pulse Relation

nous intensity modulation. In this way, the fail bit map is displayed on the CRT. Compared with others like TTL, the operation of IC memories is too complicated to understand only by pulse waveform observed with an ordinary oscilloscope.

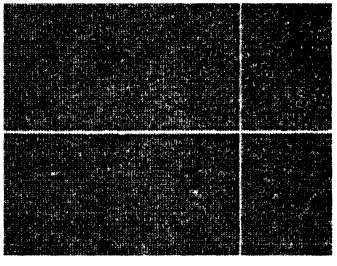
Therefore, the fail bit map as shown in Fig. 5 is very useful for observing the operation of IC memories.



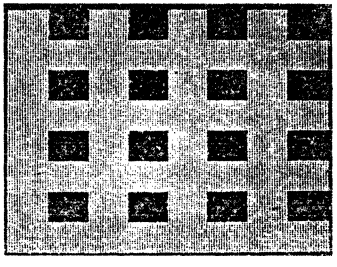
(A)



(B)



(C)



(D)

Fig. 5 Example of 1 bit Solid Failure

4. FAILURE MODE

Generally, 70% – 90% of failures at users are called solid failures. This failure mode has no relation with access time, voltage margin or timing. In this mode, a certain specified bit is stuck in "0" or "1". The simple methods previously mentioned is useful to detect such failures. Therefore, high-precision measurements such as those performed in memory IC manufactures are not necessary except any special cases.

Hitachi performs 100% inspection on the worst conditions for devices so as to guarantee sufficient operations under all power voltage conditions and timing conditions specified.

An extremely accurate memory tester is necessary to perform high-precision inspection considering 1ns accuracy. Hitachi has been developing testers to supply excellent memory ICs in characteristics and quality to users, and establishing the system capable of developing further high-efficiency memory ICs.

1. Static RAM

1.1. Static RAM Memory Cell

The static RAM memory cell consists of flip-flops organized as 4 NMOS transistors and 2 load resistors as shown in figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

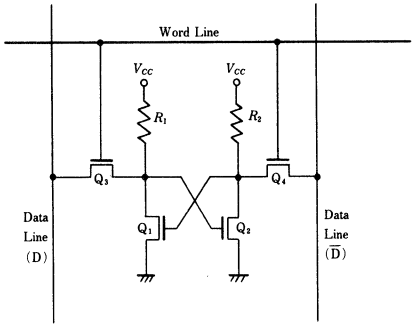


Figure 1-1. Static RAM Memory Cell

1.2. Data Retention Mode and Battery Back-up System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. So, it enables a battery back-up system to retain data during power failure.

Data Retention Mode: The important point in designing a battery back-up system is the timing relation between the memory power supply during the change (ordinal source → battery) and the chip select signal. If the timing for the change is missed, the data in memory might be destroyed.

Figure 1-2. shows the timing for switching the power supply. The following explains the technical terms related to the data retention mode.

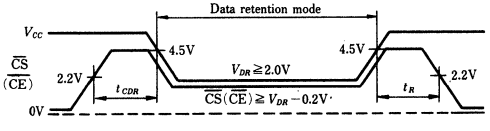


Figure 1-2. Timing for Battery Back-up Application

Data retention mode: The period that the power supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS} = V_{DR} - 0.2V$).

t_{CDR} (time for chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (Operation recovery time): The minimum time needed to change from data retention mode to operating mode. Normally, it is the same as the cycle time of the memory.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally, the minimum supply voltage needed to retain memory data is 2 V.

I_{CCDR} (data retention current): The current consumption in data retention mode. It depends on memory power supply voltage and ambient temperature. It is specified at supply voltage (V_{DR}) = 3.0 V.

Battery Back-up System: battery back-up sequence is described in the following:

1. External circuit detects failure of system power supply.
2. External circuit changes RAM to standby mode.
3. External circuit separates RAM from system power supply.
4. External circuit switches to Back-up power supply.

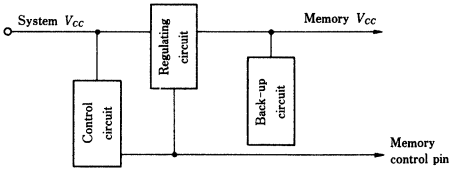


Figure 1-3. Example of Battery Back-up System

The control circuit detects the power failure and cuts off the power after switching memories to standby mode. On recovery, it confirms power supply and after some delay, returns memories to operating mode. The memory control signals depend on the types of memories used in the system.

* Using memory with only one $\overline{CS}$. NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. As the level of $\overline{CS}$ in data retention mode must be higher than V_{DR} − 0.2V, the power supply for this NAND gate must either be shared with the memory power supply, or be pulled up to the memory power supply.
* Using memory with two $\overline{CS}$. Basically, the signals are the same as mentioned above. In general use, two pins should be used for the control signal and the chip select signal respec-

tively. $\overline{CS}$, which can intercept current path of other pins in the input buffers, is for control signal input of data retention mode.

* Using memory with $\overline{CS}$ and CS. As CS selects the chips at high level, it is better to use CS than $\overline{CS}$ as control signal input for data retention mode. As soon as power down is detected, signals should be brought to low level. So a pull-up to the memory power supply level is not needed and circuit organization is simplified.

Figure 1-4 shows an example of a battery back-up system circuit. Hitachi recommends using CMOS logic for gate G_1 in control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch regulating circuit from system power supply to back-up power supply.

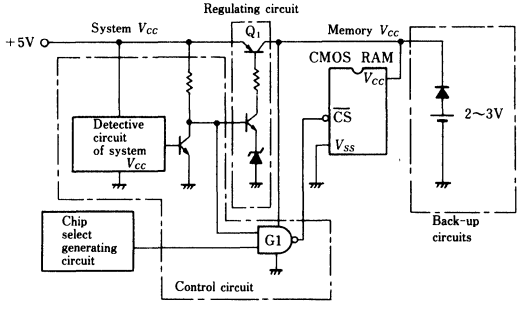


Figure 1-4. Example of Battery Back-up System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

A new type of memory, pseudo-static RAM has been developed providing the advantages of dynamic RAM (low cost, high density), and static RAM (easy usage). IC memory consists of memory cells for data storage, and input/output circuits for interfacing to the external circuits. PSRAM provides the memory cell and peripheral circuits of DRAM and the external control circuits, which includes a part of the refresh control circuits not provided by dynamic RAM, and interface circuits similar to that of static RAM, on a chip, as shown in table 2-1. Address input is not multiplexed and data input/output is byte-wide like standard static RAM. With PSRAM x 8 organization, medium density memory system can be designed easily. PSRAM provides address refresh, automatic refresh and self refresh.

Figure 2-1 shows examples of system design using PSRAM and DRAM. Using PSRAM, the circuits interfacing CPU to DRAM can be drastically reduced.

Figure 2-2 shows block diagram of pseudo static RAM.

Table 2-1. PSRAM Features

	SRAM	PSRAM	DRAM
Memory Cell	4 Tr + 2 R	1 Tr + 1 C	
Organization	x1, x4, x8	x8	x1, x4
Address	Single Address		Multiplexed Address
Refresh	Nor Necessary	Necessary	
External Circuits	Simple ⟺ Complexed		

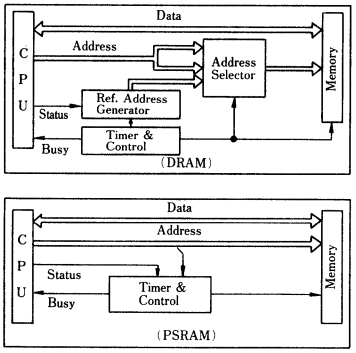


Figure 2-1. System Organization

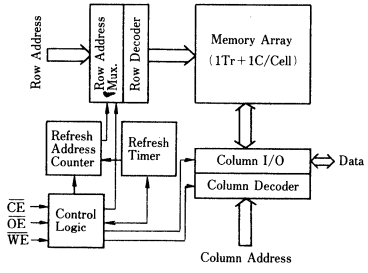


Figure 2-2. Block Diagram (PSRAM)

2.2. 1 Mbit Pseudo-Static RAM Function

Read/Write Cycle: Figure 2-3 and figure 2-4 show the timing chart for the read/write cycle of 1 Mbit pseudo-static RAM HM658128. The HM658128 can perform 2 types of access in a read cycle, $\overline{CE}$ access (Figure 2-3 (a)) and $\overline{OE}$ access figure 2-3 (b)). It writes the data at the rising edge of $\overline{WE}$ (figure 2-4 (a)) or at the rising edge of $\overline{CE}$ (figure 2-4 (b)). The $\overline{CS}$ pin should be brought high when the address is latched at the falling edge of $\overline{CE}$ in the read/write cycle. The HM658128 has no $\overline{OE}$ specification at the falling edge of $\overline{CE}$ as it provides both $\overline{OE}$ pin and $\overline{RFSH}$ pin.

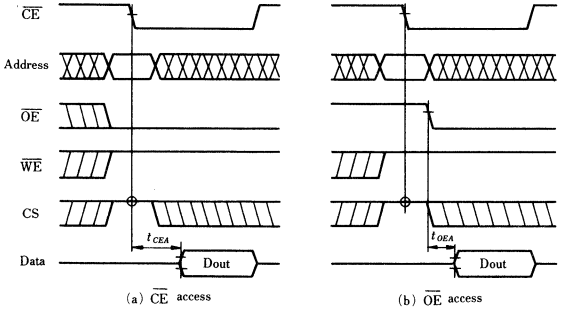


Figure 2-3. Read Cycle

CS Standby Mode: The HM658128 enters CS standby mode for one cycle if CS turns to low at the falling edge of $\overline{CE}$ (figure 2-5).

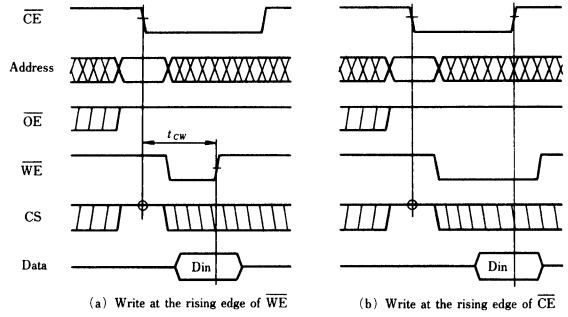


Figure 2-4. Write Cycle

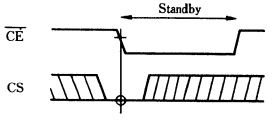


Figure 2-5. CS Standby Mode

Address Refresh: Address refresh mode performs refresh by access to row address (A0 – A8) 0 – 511 sequentially within 8 ms, as shown in figure 2-6 (in distributed mode). In this mode, CS should be high at falling edge of $\overline{CE}$.

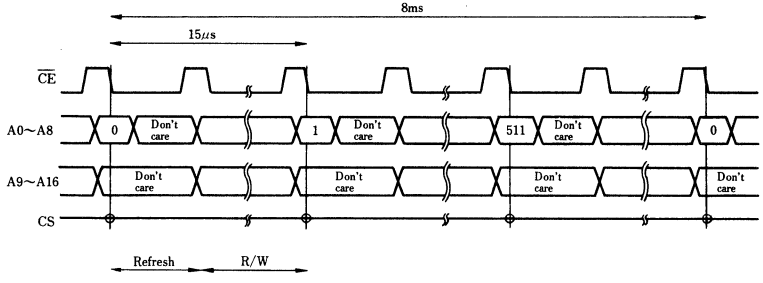


Figure 2-6. Address Refresh

Automatic Refresh: The HM658128 goes to automatic refresh mode if $\overline{RFSH}$ falls while $\overline{CE}$ is high and it is kept low for more than 180 ns.
It is not required to input the refresh address from address pins A0 – A8, as it is generated internally. Figure 2-7 shows the timing chart for distributed refresh. In automatic refresh mode, the timing for only $\overline{CE}$ and $\overline{RFSH}$ are specified.

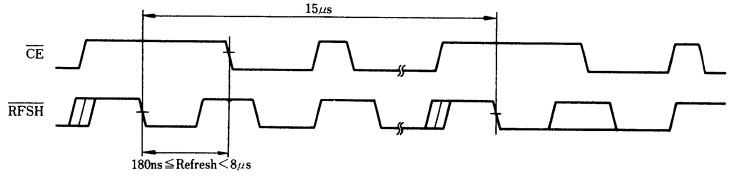


Figure 2-7. Automatic Refresh

Self Refresh: Self refresh mode performs refresh at the internally determined interval. The HM658128 enters the mode when the internal refresh timer is enabled by keeping $\overline{CE}$ high and $\overline{RFSH}$ low for more than 8 μs (figure 2-8).

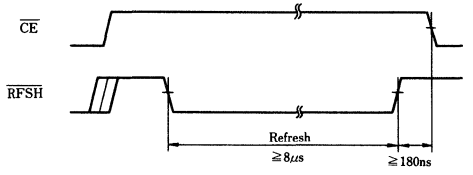


Figure 2-8. Self Refresh

Considerations on Using HM658128: The following should be considered when using the HM658128.

- Data retention. The HM658128 can retain the data with a battery (but not for long time). The HM658128L, low power version, offers typical self-refresh or standby current of 100μA.
  A 1-Mbyte system (using eight HM658128Ls) can retain the data for about 1.5 months with battery of 100 mAh current. V_{CC} = 5 V ± 10% must be maintained for data retention.
- Power on. Start HM658128 operation by executing more than eight initial cycles (dummy cycles) more than 100 μs after power voltage reaches 4.5 V – 5.5 V after power on.
- Bypass capacitor. Hitachi recommends inserting 1 bypass capacitor per RAM.

2.3 Pseudo-Static RAM Data Retention

PSRAM with self refresh retains data $\overline{CE}$ and $\overline{OE}$ are fixed for more than defined period. The following explains considerations for PSRAM data retention.

First, PSRAM cannot retain the data at low supply voltage.

They employ 1 MOS type memory cell as shown in figure 2-9. The charge is stored on the capacitor C as memory data. The data 1, written at low supply

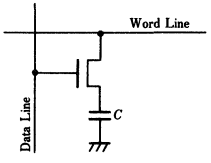


Figure 2-9. Memory Cell of PSRAM

voltage, cannot be read as 1 at high supply voltage.

Figure 2-10 indicates the operation voltage for self refresh and subsequent read of PSRAM. If the data is read out at more than 5 V of V_{CC}, for example, after self refresh is performed at V_{CC} = 3.7 V, it is destroyed.

PSRAM must be used at supply voltage from 4.5V to 5.5V.

Second self refresh current increases at low supply voltage.

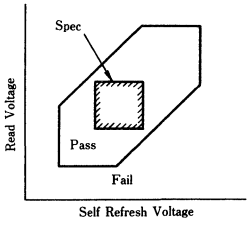


Figure 2-10. PSRAM Operating Voltage

PSRAM provides the voltage level detector circuit to reduce self refresh current. However, it should be noted that the circuit increases the current with low supply voltage in self refresh (figure 2-11). Self refresh current also increases at low temperature (figure 2-12).

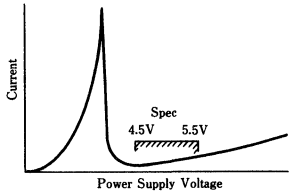


Figure 2-11. Self Refresh Current vs. Voltage

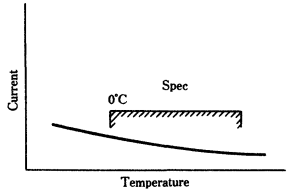


Figure 2-12. Self-Refresh Current vs Temperature

Please use PSRAM within the recommended operation range (V_{CC} more than 4.5 V, temperature more than 0°C) for data retention, especially using a battery.

3. Video RAM

3.1. Multi-Port Video RAM

Figure 3-1 shows general idea of video RAM. Multi-port video RAM provides an internal data register (SAM) with the memory (RAM). Both of them can be accessed asynchronously. Effective graphic display memory is realized by using the random port of RAM for graphic processor drawing and the serial port of the SAM part for CRT display.

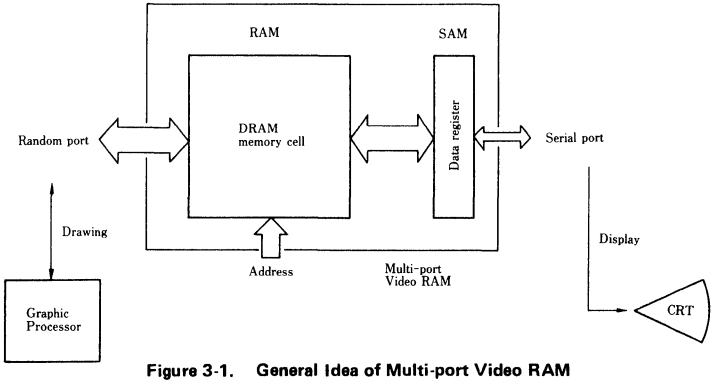


Figure 3-1. General Idea of Multi-port Video RAM

Figure 3-2 shows the block diagram of the 256-kbit multi-port video RAM HM53461, and table 3-1 shows the operation modes of the HM53461.

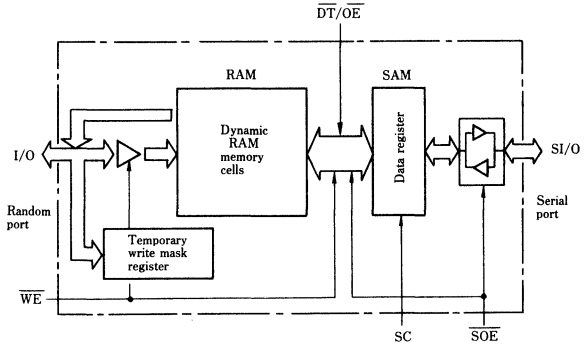


Figure 3-2. Block Diagram of HM53461

The operation modes shown in table 3-1 are described as follows.

Table 3-1. Operation Modes of HM53461

At the falling edge of RAS				RAM modes	SAM modes	
CAS	DT/OE	WE	SOE		SI/O direction	Notes
H	H	H	X	Read/write	Sin/Sout	1, 2, 3
H	H	L	X	Temporary write mask data program	Sin/Sout	1, 2, 3
H	L	H	X	Read transfer	Sout	2
H	L	L	L	Write transfer	Sin	
H	L	L	H	Pseudo transfer	Sin	
L	X	X	X	CBR refresh	Sin/Sout	1,2

H: High
L: Low
X: Don't Care

Notes: 1. Transfer cycle executed previously defines SI/O direction.
2. SI/O is in high impedance state with SOE high, even if the direction is Sout.
3. The HM53461 starts write operation if WE is low at the falling edge of CAS or become low between the falling edge of CAS and the rising edge of RAS.

Read/Write Operation: Read/write is performed on the random port in the same sequence as for a dynamic RAM (figure 3-3). The HM53461 starts the read operation with $\overline{WE}$ high and the write operation at the falling edge of $\overline{WE}$.

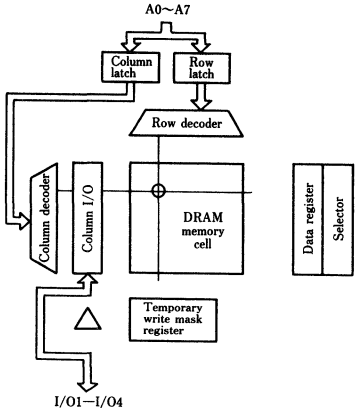


Figure 3-3. Read/Write Operation

Temporary Write Mask Set and Temporary Masked Write Operation: The HM53461 provides temporary masked write operation which inhibits to write data bit-by-bit (write mask) during one $\overline{RAS}$ cycle. Temporary write mask set function defines the bits to be inhibited (figure 3-4). This operation puts the data on I/O1 – I/O4 into the internal temporary write mask register. When 0 is programmed to the register, writing to the corresponding bit is inhibited.

The temporary write mask register is reset at the rising edge of $\overline{RAS}$.

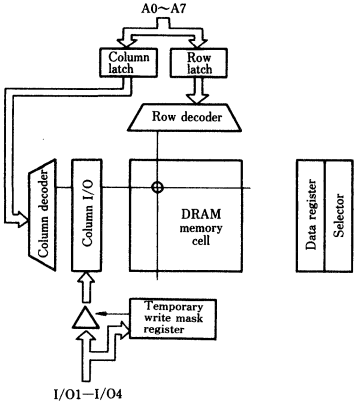


Figure 3-4. Temporary Masked Write Operation

Read Transfer Operation: In this cycle, the HM53461 transfers the data of one row in RAM (1024 bits), which address is specified at the falling edge of $\overline{RAS}$, to SAM (figure 3-5). The start address in SAM can be programmed at the falling edge of $\overline{CAS}$ in this cycle. After data transfer, the serial port turns to serial read mode at the rising edge of $\overline{DT/OE}$.

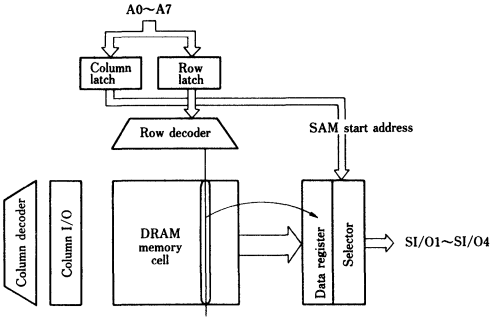


Figure 3-5. Read Transfer Operation

Write Transfer Operation: In this cycle, the HM53461 transfers the data in the SAM data register (1024 bits) to one row in RAM, which address is specified at the falling edge of $\overline{RAS}$ (figure 3-6). The start address in SAM can be programmed in this cycle. After data transfer, serial port turns to serial write mode.

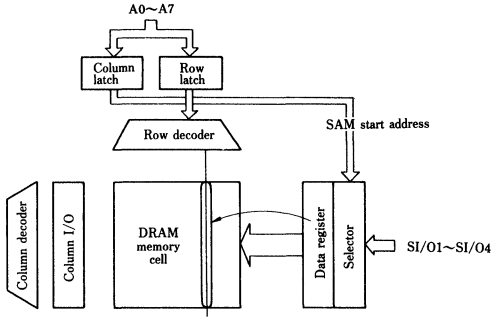


Figure 3-6. Write Transfer Operation

Pseudo Transfer Operation: This operation switches the serial port to serial write mode (figure 3-7). It does not perform data transfer between RAM and SAM. SAM start address can be programmed in this cycle.

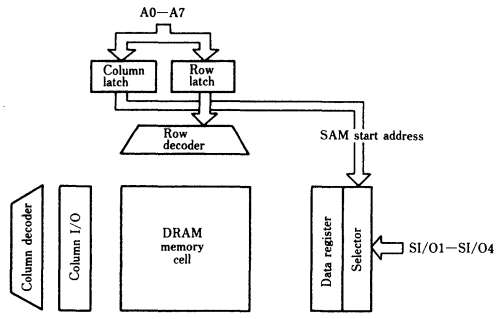


Figure 3-7. Pseudo Transfer Operation

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Operation: The HM53461 performs refresh by using the internal address counter in this operation (figure 3-8).

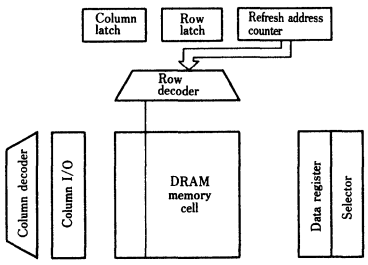


Figure 3-8. $\overline{CAS}$ Before $\overline{RAS}$ Refresh

Serial Read/Write Operation: The HM53461 reads/writes the contents of the SAM data register in serial at the rising edge of SC (serial clock input) (figure 3-9). The address for serial access is generated by the internal address pointer, independently of random port operation. It should be considered that serial access is restricted in transfer cycles. The SAM, employing static-type data registers, requires no refresh.

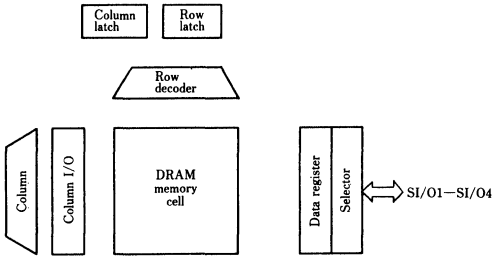


Figure 3-9. Serial Read/Write Operation

The HM53462 is a multi-port video RAM, adding logic operation capability to the advantages of HM53461.
Figure 3-10 shows the block diagram. Table 3-2 describes the operation modes.

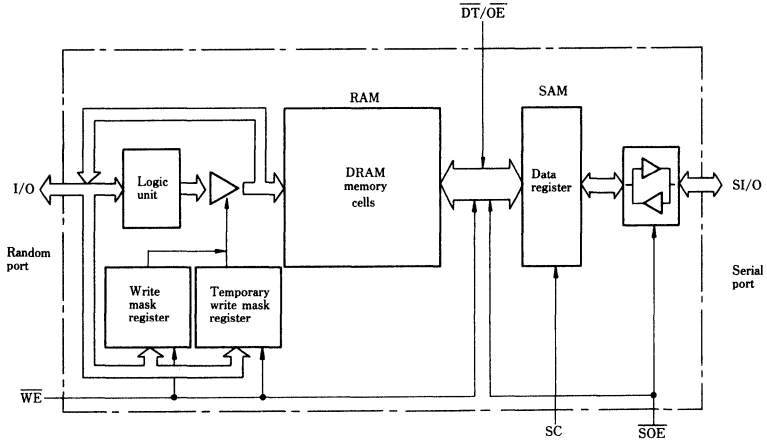


Figure 3-10. Block Diagram of HM53462

Table 3-2. Operation Modes of HM53462

At the falling edge of $\overline{RAS}$				RAM modes	SAM modes	
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SOE}$		SI/O direction	Notes
H	H	H	X	Read/write	Sin/Sout	1, 2, 3
H	H	L	X	Temporary masked write	Sin/Sout	1, 2, 3
H	L	H	X	Read transfer	Sout	2
H	L	L	L	Write transfer	Sin	
H	L	L	H	Pseudo transfer	Sin	
L	X	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh	Sin/Sout	1,2
L	X	L	X	Logic operation program (CBR Refresh)	Sin/Sout	1,2

H: High L: Low X: Don't Care

Note: 1. Transfer cycle previously executed defines SI/O direction.
2. SI/O is in high impedance with $\overline{SOE}$ high, even if SI/O direction is Sout.
3. HM53462 writes if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of RAS.

Logic Operation Programming: This function programs a logic operation (figure 3-11). The logic operation is available until re-programmed or reset. In logic operation mode, HM53462 performs read-modify-write internally when data is written into random port. The result of the logic operation between memory data and written data is put into the address from which the memory data is transferred.

In the logic operation programming cycle, the mask register, which differs from the temporary mask register, is also programmed. It is available until re-programmed.

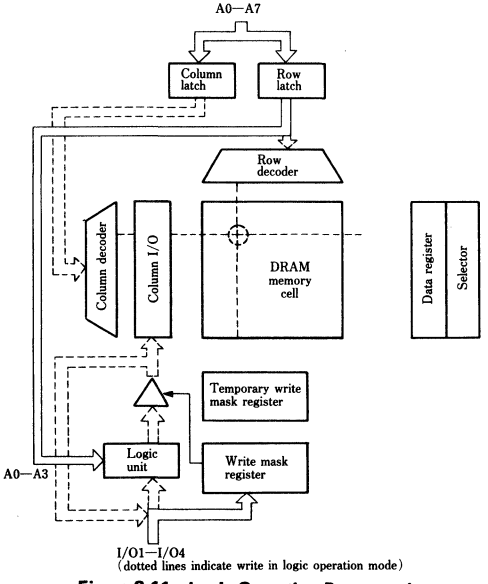


Figure 3-11. Logic Operation Programming

Notes: Notes on using HM53461/HM53462 are as follows.

- Dummy $\overline{RAS}$ cycle. Devices should be initialized by 8 dummy $\overline{RAS}$ cycles (minimum) before access to random port. Refresh cycle can be inserted for initialization. It is recommended that the system be initialized by dummy $\overline{RAS}$ cycle in the automatic reset time of the processor.
- Bypass capacitor. One bypass capacitor should be inserted between V_{CC} and V_{SS} to each device. The V_{CC} pin should be connected to the capacitor by the shortest path. A capacitor of several μF is suitable.
- Negative voltage input. Negative polarity input level to input pin or I/O pin should be under −1 V. In this range, it has no effect on device characteristics or RAM/SAM data retention.
- Initialization of logic operation mode (HM53462). The logic operation programming cycle should be executed before access to the random port to initialize logic operation mode after power on. At this time, the operation codes (0101) and all 1 write mask data are recommended.

3.2. Line Memory

Hitachi has produced a line memory for line buffers with simple circuits, providing specific functions as described below.

The line buffer can improve picture quality by storing 1 horizontal line data. It has following features.

- Capacity to store 1 horizontal line data
- High-speed operation matching the sampling speed of PAL TV signal (4 fsc/8fsc) or NTSC TV signal (4 fsc/8fsc).

- Data inputs/outputs separated and capability of serial data inputs and outputs.

The conventional line buffer composed of high speed static RAMs requires separate input/output for double buffer organization. It also requires interleaving for high speed operation, matching 4fsc/8fsc of the subcarrier frequency. In addition, external circuits are needed for serial address scan.

The line memory provides all of these functions. Figure 3-12 shows the standard organization of a conventional memory buffer and figure 3-13 shows the standard organization of line memory.

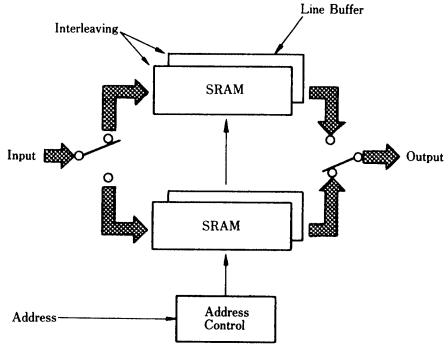


Figure 3-12. Standard Organization of Conventional Line Buffer

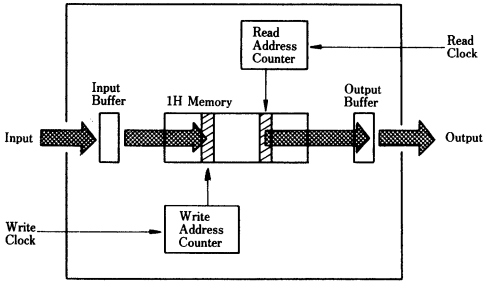


Figure 3-13. Standard Organization of Line Memory

The Hitachi HM63021 is a 2048-word x 8-bit line memory storing 2 horizontal lines of data.

It has five different modes for various video graphic system applications. It realizes high speed operations for PAL and NTSC TV signals, and dissipates little power employing 1.3 μm CMOS technology and static-type memory cells.

The features of the HM63021 are described as follows:

- Five modes for various video graphic system applications
  - Delay line mode
  - Alternate 1H/2H delay mode
  - TBC (Time-Base Corrector) mode
  - Double speed conversion mode
  - Time-base compression/expansion mode
- High speed cycle time
  - HM63021-34: 34 ns min (corresponds to 8fsc of NTSC TV signal)
  - HM63021-28: 28 ns min (corresponds to 8fsc of PAL TV signal).

Line memory in the system using digital signal processing technologies offers following applications:

1. comb filter
2. double-speed conversion (non-interlace)
3. compression/expansion of graphics (picture-in-picture)
4. dropout canceller
5. time-base corrector
6. noise reducer

4. Dynamic RAM

4.1. Dynamic RAM Memory Cell

The dynamic RAM memory cell consists of 1 MOS transistor and 1 capacitor, as shown in figure 4-1. It detects the data in the cell (1 or 0) by the charge stored in capacitor. Dynamic RAM offers higher density than that of static RAM because of fewer components per chip.

However, Dynamic RAM must rewrite data, called refresh, in a defined cycle because the charge stored in the capacitor leaks.

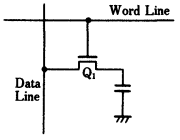


Figure 4-1. Memory Cell of Dynamic RAM

4.2. Power On Procedure

After turning on power, to set the internal memory circuitry, hold for more than 500 μs, then apply eight or more dummy cycles before operation. The dummy cycle may be either a normal read/write cycle or a refresh cycle. When using an internal refresh counter, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required as dummy cycles.

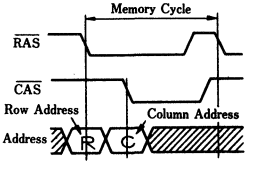
4.3 Address Multiplexing

Dynamic RAMs are used to increase capacity because of their smaller cell area. In using dynamic RAMs in systems, however, it is desirable to increase the memory density by using smaller packages. To reduce the number of pins and the package size, address multiplexing is used.

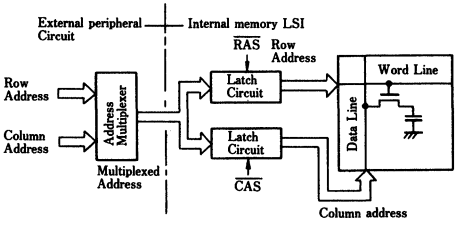
Using a 1-Mbit dynamic RAM, 20-address signals are necessary to select one of 1048,576 memory cells. Address multiplexing allows address signals to be applied to each address pin. Thus only 10-address input pins are required to select one of 1048,576 addresses. Multiplexed address inputs are latched as follows: $\overline{RAS}$ (Row Address Strobe) selects one of word lines according to the row address signal, and one of column decoders is selected by $\overline{CAS}$ (column address strobe) following column address signal. Although two extra signals, $\overline{RAS}$ and $\overline{CAS}$, are required, the number of address pins is reduced to half. Figure 4-2 shows the pin arrangement, address latch waveform, and the block diagram of address-multiplexed 1-Mbit dynamic RAM. Systems need an address multiplexer in order to latch the multiplexed address signals into the device.

A0 – A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 – A8	Refresh Address Inputs

(a) Pin Arrangement



(b) Address Latch

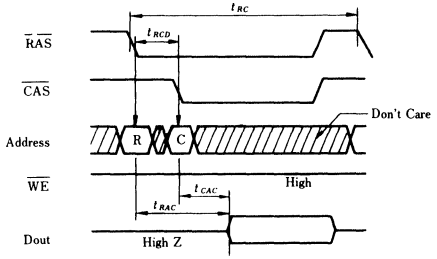


(c) Block diagram of Address Multiplexing

Figure 4-2 Address Multiplexing of Dynamic RAMs

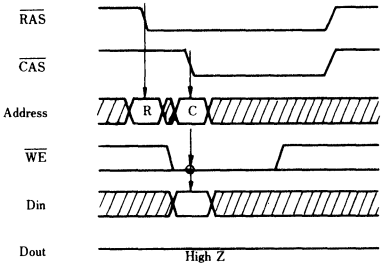
4.4. Dynamic RAM Function

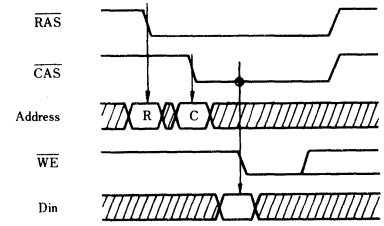
Figure 4-3 shows the normal function of Dynamic RAM.



(a) Read Cycle

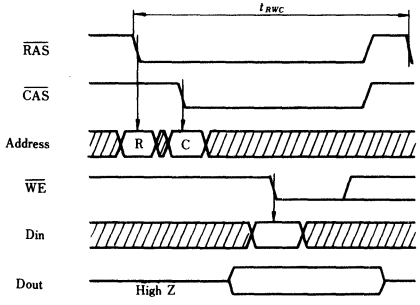
t_{RC}: Random Read or Write Cycle Time
t_{RCD}: RAS to CAS Delay Time
t_{RAC}: Access Time from RAS
t_{CAC}: Access Time from CAS
R: Row Address
C: Column Address





(Delayed Write)

(b) Write Cycle (Early Write)



t_{RWC}: Read-Write Cycle Time

(c) Read Modify Write Cycle

Figure 4-3 Normal Function of Dynamic RAM

Read Cycle: In the read cycle, a row address is latched at the falling edge of RAS, and a column address is latched at the falling edge of CAS after the RAS falling edge. If WE is high, the data is read out from Dout depended on the later of t_{CAC} (Access time from CAS) or t_{RAC} (Access time from RAS).

The t_{RCD} maximum (RAS to CAS delay time) is specified only to guarantee the specified minimum values of other timings such as the cycle time, RAS/CAS pulse width. Therefore, when using these timings with more than the specified minimum value, there is no need to limit the t_{RCD} to the specified maximum value. The t_{RCD} maximum depends on the other timings being at minimum in its application.

Write Cycle: Dynamic RAM provides two write cycle modes: early write cycle and delayed write cycle. In the early write cycle, when WE is low, data is written into Din at the falling edge of CAS. In delayed write cycle, when WE is high, data is written into Din at the falling edge of WE after CAS falling.

Read-Modify-Write Cycle: The read-modify-write

cycle is initiated by taking $\overline{WE}$ high. Data is read out from Dout at the falling edge of $\overline{CAS}$ with $\overline{WE}$ high. Then, when $\overline{WE}$ goes low, data is written into the same address from Din in the same cycle.

The cycle time in the read-modify-write mode (t_{RWC}) is longer than the cycle time in read/write mode (t_{RC}).

4.5 High Speed Access Mode

Dynamic RAM access time is typically longer than that of static RAMs. To realize higher speed operation, they have high speed access modes.

The read operation in dynamic RAM is performed as follows:

When a word line is selected by row address, all data in the memory cells connected to the selected word line is transferred to sense amplifiers. One of these sense amplifiers is selected by the column address, and its contents are output.

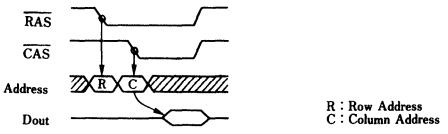
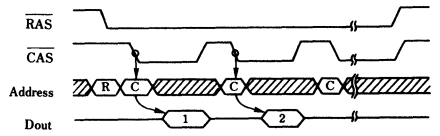
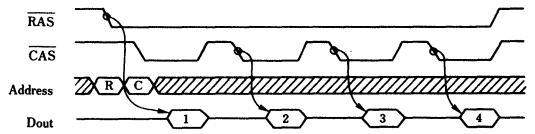
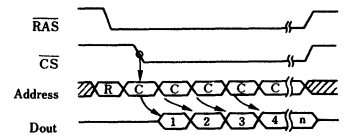
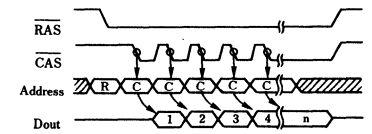
The output of data from other sense amplifiers is controlled only by the column address.

Access controlled only by column address with the row address fixed is called high speed access mode. Table 4-1 compares each mode.

Page Mode: This is the most typical access mode in dynamic RAM. The column address is switched synchronized with $\overline{CAS}$ falling.

Nibble Mode: In a nibble mode dynamic RAM,

Table 4-1. Comparison of Dynamic RAM High Speed Access Modes

Normal Mode	
Page Mode	
Nibble Mode	
Static Column Mode	
High-Speed Page Mode	

data from 4 sequential addresses is stored in the 4-bit output latch circuits. Output is provided by the $\overline{CAS}$ signal, which controls the latch circuits.

When 4 addresses are accessed sequentially, the row addresses on and after second bit need not be selected. Therefore, it facilitates the timing design. In nibble mode, the operation is limited to 4 addresses, however, it enables faster access (t_{NAC}) than that in page mode.

Static Column Mode: In static column mode, the row address is switched without the synchronized signal by high-speed static RAM technology in the peripheral circuits.

High Speed Page Mode: This mode is the advanced mode of static column mode, with $\overline{CAS}$ providing the address latch function.

4.6 Refresh

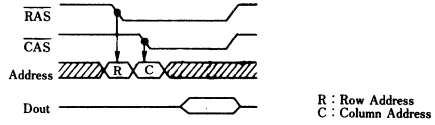
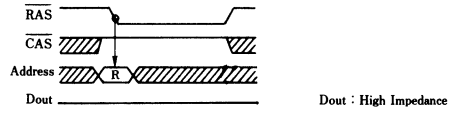
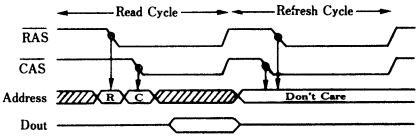
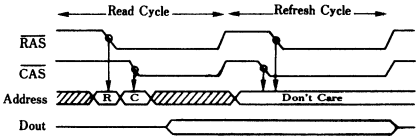
Refresh operation is performed by accessing every word line within the specified time (refresh cycle). Table 4-2 compares the following refresh modes in dynamic RAM.

$\overline{RAS}$ Only Refresh: In $\overline{RAS}$ only refresh mode, refresh can be completed by selecting only row addresses synchronized with $\overline{RAS}$.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh: This mode refreshes by the $\overline{CAS}$ falling edge before $\overline{RAS}$ in the period defined by the internal refresh address generator. This mode simplifies the external address multiplexer.

Hidden Refresh: In hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh is performed while output data is valid.

Table 4-2. Comparison of Dynamic RAM Refresh Modes

Read	
$\overline{RAS}$ Only Refresh	
$\overline{CAS}$ before $\overline{RAS}$ Refresh	
Hidden Refresh	

5. EPROM

5.1. EPROM Memory Cell

EEPROM is electrically erasable and programmable ROM, which can be erased or written remotely while the system is in operation.

The Hitachi EEPROM memory cell is MNOS (Metal Nitride Oxide Semiconductor) type, as shown in figure 5-1.

An MNOS memory cell consists of two layers of oxide film and nitride film. The thickness of oxide film is about 20 Å and that of nitride film is 300 to 500 Å. There are traps in the boundary of the oxide and nitride films to catch electrons. Electrons move by the tunneling phenomenon between the substrate and traps.

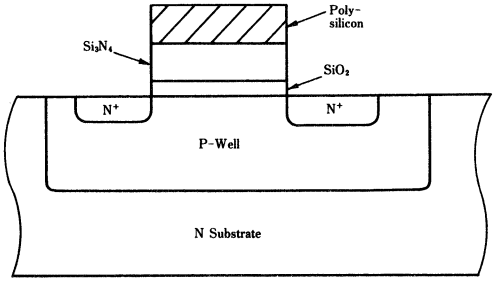


Figure 5-1. MNOS Type Memory Transistor

5.2. 64-kbit CMOS EEPROM Function

Page Write Function: The 64-kbit HN58C65 can latch 32 bytes (max) and write them in one write cycle. Write cycle time is specified as 10 ms (typ.). The effective byte write speed of HN58C65 in page write mode is:

10 ms/32 bytes = 0.31 ms/byte

Thus it takes only 2.56 seconds to write the whole HN58C65. Figure 5.2 shows internal operation. The following describes operation sequence:

1. 32-byte memory cell data at the row address selected by address pins A5 – A12 is latched.
2. Latched data at the column address specified by address pins A0 – A4 is altered with write data, which is put into Din buffer from I/O pins I/O0 – I/O7.
   The 32 bytes (max) of latched data are altered by repeating this operation 32 times.
3. 32-bytes memory cell data in the selected row (1) are erased (All 1).
4. Latched data is written into the selected row (3).
5. CPU acknowledges the completion of write cycle by the internal timer. The HN58C65 provides RDY/$\overline{\text{BUSY}}$ and $\overline{\text{Data}}$ polling to indicate the write completion.

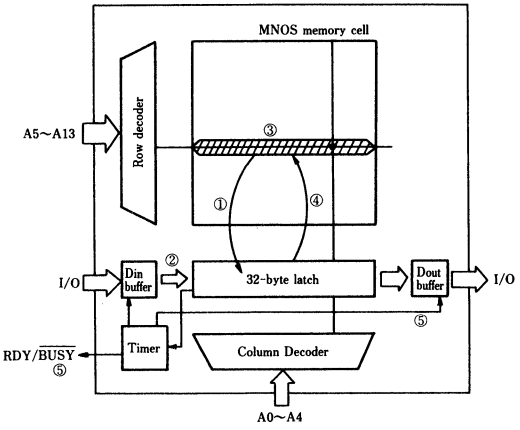


Figure 5-2. HN58C65 Page Write

Internal Timer: The HN58C65 indicates the completion of data write to the CPU by using the internal timer. The HN58C65 enters next cycle as soon as detecting the completion of write. This function offers high system throughput as the CPU can access other devices during write cycle. The HN58C65 has two functions, RDY/$\overline{\text{BUSY}}$ and $\overline{\text{Data}}$ polling, to indicate the completion of data write.

The RDY/$\overline{\text{BUSY}}$ approach indicates the completion of data write by using pin 1. It is low when the HN58C65 is in data write operation ($\overline{\text{BUSY}}$) and turns to high impedance state at the end of data write (RDY). RDY/$\overline{\text{BUSY}}$ pin should be pulled up as it uses open drain output. The RDY/$\overline{\text{BUSY}}$ pins can be writed-OR when using several HN58C65s.

The $\overline{\text{Data}}$ polling approach, implemented by software, indicates the completion of data write through pin 19 (I/O7). While the data write is not completed, I/O7 shows the inverted data of what was written in the last cycle. In using this approach, RDY/$\overline{\text{BUSY}}$ pin should be opened or grounded. The $\overline{\text{Data}}$ polling approach can acknowledge the completion of data write in an individual HN58C65, even if several HN58C65s are used in the system.

Data Protection: EEPROM performs data write

with a higher voltage (V_{PP}) than power supply voltage (V_{CC}). The HN58C65 internally generates V_{PP} by a high voltage generator with the combination of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$). It supports the following functions to avoid accidental data write (data protection).

1. Data protection against the noise on the control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during operation.
2. Data protection against the noise at power-on/ power-off.

6. EPROM/OTPROM

6.1. EPROM Programming

Figure 6-1 shows the sectional structure of an EPROM memory cell. The upper gate, one of the gates made of two-layered polycrystalline silicon, is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected. This memory cell is programmed as follows: With substrate and source grounded, apply high voltage between drain and control gate. Then, an electric potential incline occurs between source and drain so that intensity of the electric field becomes high near the drain. Because of this electric field, electrons are accelerated and so-called hot electrons are generated, which jump over the energy barrier of SiO_2 film. Hot electrons are pulled by the electric potential of the control gate and pour into the floating gate. Electrons stored in the floating gate remain stable, as they fall into a well surrounded by an energy barrier of SiO_2 film. Therefore, it is evident that the quality of SiO_2 film surrounding the floating gate is essential for good data retention characteristics. To keep data retention in the 5- or 10-year range, high quality SiO_2 film is needed.

Figure 6-2. shows the fundamental characteristics of the EPROM transistor. While I_D in a non-programmed transistor begins to flow with V_G of about 1V, the current in a programmed transistor does not flow until V_G rises to 7 V – 10 V. Therefore, if the voltage of word line applied to the control gate is about 5 V in readout, the non-programmed memory transistor will be on, and the programmed one will be off. This means that the data can be read out by means of the same structure as NOR-type mask ROM.

6.2. Erasing EPROM

When shipped, all bits of the EPROM are at logic 1 with all electrons in the floating gate released (erase). Changing the logic 1 to logic 0 through the application of the specified waveform and voltage, programs the necessary information. The higher the V_{PP} voltage and the longer the program pulse width t_{pw}, the more electrons can be programmed in, as shown in Figure 6-3. If V_{PP} exceeds the rated value, such as by overshoot, the p-n junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and reduce the yield voltage.

Hitachi's EPROMs can usually be written and erased more than 100 times.

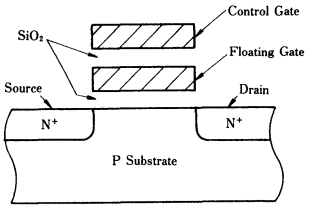


Figure 6-1. Cross Section of EPROM Memory Cell

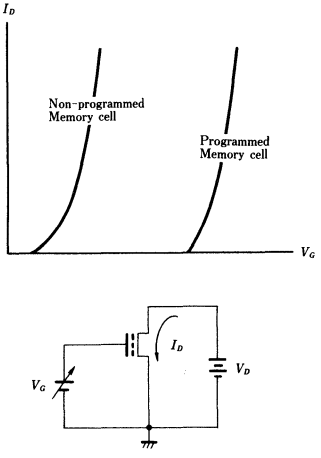


Figure 6-2. Fundamental Characteristic of EPROM Memory Cell

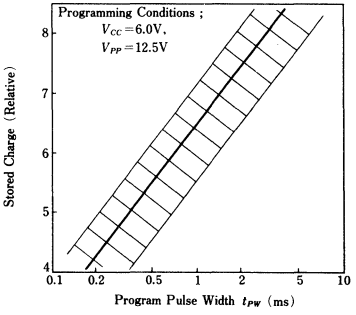


Figure 6-3. Standard Programming Characteristics of EPROMs

EPROMs are erased by ultraviolet light exposure through a transparent window on the package. Electrons in the floating gate get energy from photons and become hot electrons again with enough energy to go over the energy barrier of SiO_2

film. The hot electrons go through to the control gate or the substrate and erasure is completed. Therefore, light with enough energy to get the electrons over the energy barrier of SiO_2 film is needed for erasure. Light energy is proportional to its frequency, and described as $E = h\nu$. E means the energy of light, h is Planck's constant, ν is light frequency. Erasure isn't caused by light over certain wavelengths, and under certain wavelengths, erasure does occur. However, erasure time depends upon the quantity of photons, therefore erasure time cannot be shortened by shorter wavelength. Figure 6-4 shows the relation between wavelength and erasure effectiveness. Erasure starts at about 4000 Å, and is saturated at about 3000Å.

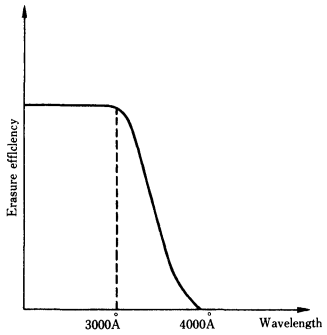


Figure 6-4. Erasure Efficiency of EPROM

For erasure, the wavelength and minimum irradiation rate of ultraviolet light must be 2,537Å and 15 $W \cdot s/cm^2$ respectively. These conditions can be met by placing the device 2 – 3 cm below a 12,000 W/cm^2 UV lamp for about 20 minutes.

The UV transmittance of the transparent lid materials is about 70%. However, it is influenced by contamination or foreign materials on the lid surface. Contamination or foreign materials should be removed with a solvent such as alcohol that does not damage the package.

Figure 6-5 shows EPROM standard erasure characteristics.

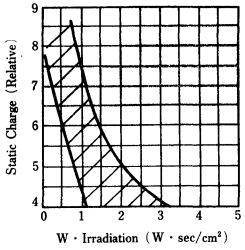


Figure 6-5. Standard Erasure Characteristics

6.3. EPROM Data Retention Characteristic

About 2 to 20×10^{-14} coulomb of electrons are accumulated in the floating gate when programmed. However, these electrons dissipate with time. Then the data may be inverted. The mechanism of electron dissipation is generally explained as follows.

Data Dissipation by Heat: The electrons at the floating gate are in a non-equilibrium state, so the dissipation of electrons by thermal energy is unavoidable. Therefore, the data retention time depends on temperature. Figure 6-6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

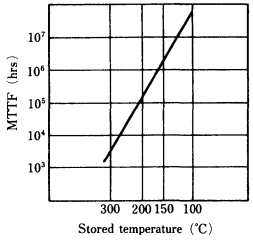


Figure 6-6. EPROM's Data Rentention Characteristic

Data Dissipation by Ultraviolet Light: Ultraviolet rays at a wavelength of not greater than 3,000 – 4000Å is capable of releasing the electric charge at

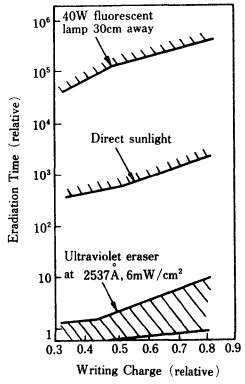


Figure 6-7. EPROM's Data Retention Time

floating gate of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet light, and so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Figure 6-7 shows the standard, data retention time under an ultraviolet eraser, sunlight and fluorescent lighting.

6.4 High-Performance EPROM Programming

As EPROM density increases, the time for programming becomes more important. High-performance programming method has been developed and put to practical use.

Generally, EPROM programming has been performed by a pulse of 50 ± 5 ms. Yet, to program within an optimum time, it is best to monitor the programming condition from time to time rather than accomplish the entire programming with a uniform pulse of 50 ms. Figure 6-8 shows how such high-performance programming is implemented.

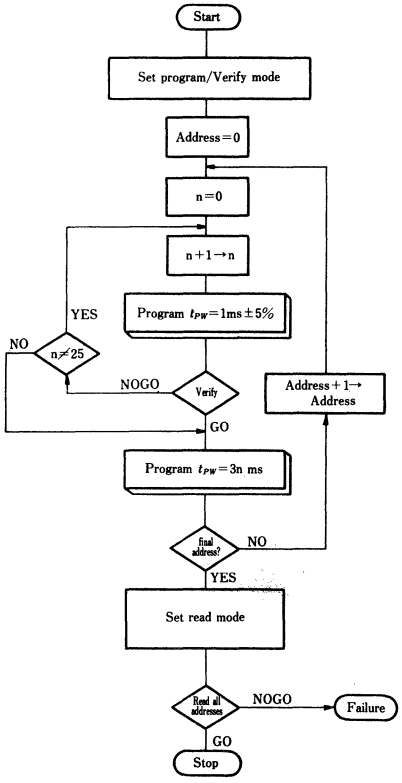


Figure 6-8. High-Performance Programming Flow Chart

This method has two key points. The first attempt at programming consists of a short pulse (approximately 1 ms), repeating programming and reading (verifying) until data is programmed correctly (i.e. until data transcription is verified). This programs the EPROM efficiently according to memory capacity. Second, after verification, data is programmed using three times as long a pulse before proceeding to the next address. This provides a safety margin in the amount of electric charge programmed (or poured into the floating gate). Figure 6-9 shows the comparison of programming times between using this high-performance programming method and using the conventional method.

The reliability of this high-performance programming method should be mentioned. The programming is performed with optimum program time depending on the capability of each memory cell. Therefore, it is the same as or a little superior to the conventional method. The data retention characteristic is unaffected by the programming method, though it depends upon the quantity of electric charge stored in the floating gate. Their data retention time does not heavily depend upon the amount of electric charge in the floating gate. Adequate data retention is achieved so long as a minimum necessary amount of electric charge is provided.

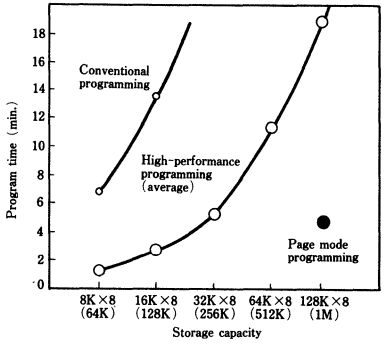


Figure 6-9. Shortened Program Time by High-Performance Programming Algorithm

6.5 Device Indentifier Code

EPROM programming conditions depend on EPROM manufacturers and device types, confusion may cause miss operation. As a countermeasure some EPROMs provide device identifier code including such information as manufacture and device type. Some newly developed commercial EPROM programmers can set write conditions automatically by recognizing this code.

Different programming conditions are as follows: (1) program voltage, (2) program timing, (3) high-performance programming algorithm, (4) pin configuration. The Hitachi EPROM has a device identifier code area besides the memory access area, as shown in figure 6-10.

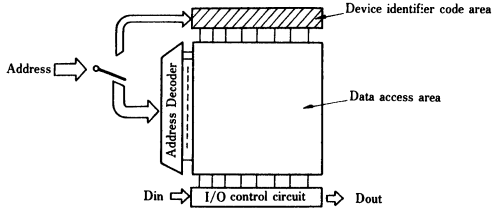


Figure 6-10. Device Identifier Code

Table 6-1 describes how to use the device identifier code. Setting A9 at 12 V and A1 – A8, A10 – A13 at V_{IL} access the device identifier code area and O0 – O7 output the programming condition code with V_{IL} or V_{IH} of A0.

Tablel 6-1. Hitach EPROM Device Identifier Code

		A0	07	06	05	04	03	02	01	00	Hex Data	
Manu-fac-turer code	Hitachi	V_{IL}	0	0	0	0	0	1	1	1	0	7
ROM code	HN27128A	V_{IH}	0	0	0	0	1	1	0	1	0	D
	HN27256		0	0	0	1	0	0	0	0	1	0
	HN27C256		1	0	1	1	0	0	0	0	3	0
	HN27512		1	0	0	1	0	1	0	0	9	4

A9: 12V
A1 -A8, A10 -A13: V_{IL}
A14, A15: Don't care

6.6 Shielding Label

When using an EPROM in an environment where it can be exposed to ultraviolet light, Hitachi recommends putting a shielding label on its transparent lid to absorb ultra-violet light. In choosing a shielding label, the following points should be carefully checked.

★ Adhesiveness (mechanical strength). Avoid repeated attaching or exposure to dust that may reduce the adhesive strength. Ultraviolet erasing and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to put a new one on over the old one since peeling may create a static charge.)

★ Allowable temperature range. Use the shielding label in an environment whose temperature falls within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too fast. When it hardens, the label may come off easily. When it sticks too fast, the paste may remain on the window glass after the label has been removed.

★ Moisture resistance. Use the shielding label in an environment whose humidity falls within the specified allowable humidity range.

6.7 EPROM Programmer

The EPROM programmer stores the user's program in its internal RAM and writes the program in the EPROM. For this programming, 3 functions at least are necessary: blank check function prior to programming, programming function, and the verify function after programming. Figure 6-11 shows the programming flow chart. Some programmers check for pin contact failure or the reverse insertion before the blank check.

The outline of each block is as follows.

1. Pin contact check
   In the ROM pin and socket connection test, checking is normally performed by detecting the forward current at each EPROM pin. Care is necessary as this forward biased resistance differs in products of each company.
2. Reverse insertion check
   This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.
3. Blank check
   This check is performed before programming. It checks whether the device is an erased EPROM, or it preventing EPROM reprogramming. Since the output data in the erased condition are 1 (high level), check whether or not data in EPROM are all 1. It will fail-stop even when one bit is 0 (low level). Normally, it is designed to provide warning with a lamp or buzzer.
4. Programming
   The function of programming the data in the internal RAM of the programmer into EPROM will fail-stop when programming cannot be done. The normal flow is as shown in figure 6-12. The EPROM data will be read out prior to programming and compared with programming data. If they coincide, programming will be skipped and if they differ, programming will be per-

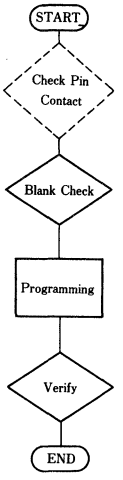


Figure 6-11. Programming Flow Chart of EPROM Programmer (1)

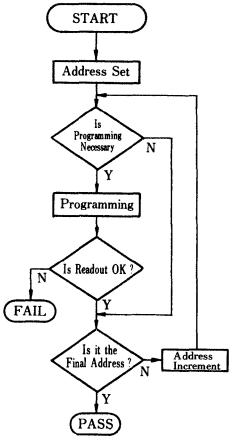


Figure 6-12. Programming Flow Chart of EPROM Programmer (2)

formed. Then, the data will be read out again and compared with the programming data, and if they coincide, the programmer will progress to the next address.

5. Verify
   This function checks after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer. It performs fail-stop when they do not coincide. Normally, when it fails, it lights the fail lamp and displays the address and data.
6. How to input the program
   Table 6-2 shows several methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are prefered options.

Table 6-2. EPROM Data Input

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch on the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction, and list preparation of the program can be made.

6.8 Handling EPROMs

Touched with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give the false impression that information has been correctly written in. As already reported at the international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from the static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges by irradiating with ultraviolet rays for a short time. The EPROM should be reprogrammed after this irradiation since it reduces the electric charges in the floating gate, too. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods as in the prevention of common static breakdown of ICs.

1. Ground operators who handle the EPROM. Avoid using things such as gloves that may generate static electricity.
2. Refrain from rubbing the glass window with plastic or other materials that may generate static electricity.
3. Avoid the use of coolant sprays which contain some ions.
4. Use shielding labels (especially those containing conductive substances) that can evenly distribute established charge.

6.9 Ensuring OTPROM Reliability

One time electrically programmable ROM (OTPROM) has two kinds of packages: standard dual in-line package (DIP) and small outline package (SOP). It is one time only programmable because it has no window for ultraviolet light exposure; testing by programming and erasure cannot be performed after it is assembled.

So, Hitachi performs screening test for programming, access time, and data retention on wafers at proving test.

However, rare defects may occur in the assembly process cannot be completely removed in final test screening which is only a reading test.

Therefore, Hitachi recommends that users perform high temperature baking after programming devices to ensure high reliability.

Detailed conditions and procedures for screening are shown in figure 6-13. First, program and verify devices. Then, leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, check read-out function and remove the chips with data retention failures.
From the results of devices in which the recommended screening test is properly performed, we confirm that the data retention characteristics of OTPROMs are equal to general EPROMs.

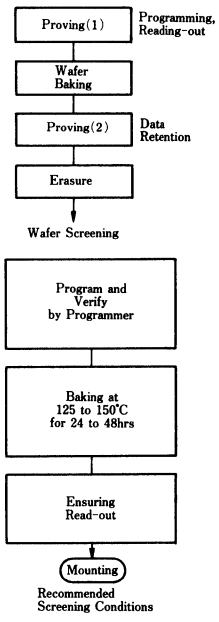


Figure 6-13. Screening Flow Chart of OTPROM

7. MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into mask ROMs is performed by the CAD system on a large-sized computer. ROM code data should conform to specifications given below, using either paper tape, EPROM, or magnetic tape. Additional instructions, such as chip select and customers' part number, should be given in the "ROM Specification Identification Sheet"

7.1 Specification of EPROM

1. Submit the three sets of the EPROM-stored data. Specify the address of the EPROM in the case of two or four EPROMs.
2. The ROM code data is input from the start address to Final Address in the EPROM.
3. Type of EPROM
   HN482764 (8-kword x 8-bit, 2764 Compatible)
   HN4827128 (16-kword x 8-bit, 27128 Compatible)
   HN27256 (32-kword x 8-bit, 27256 Compatible)
   HN27C256 (32-kword x 8-bit, 27C256 Compatible)

7.2 Specification of Magnetic Tape

1. Use the following type of magnetic tape which can be used by a magnetic tape device compatible with the IBM magnetic tape device.
   Length . . . . . 2,400 feet, 1,200 feet or 600 feet
   Width . . . . . 1/2 inch
   Channel . . . . . 9 channels
   Bit density . . . . 800 BPI or 1,600 BPI (Clearly state which it is in the "ROM Specification Indetification Sheet".)
2. Use EBCDIC as the use code.
3. Follow the format of the magnetic tape as described below
   No leading tape mark
   No label
   Record size . . . . . 80 byte/1 record
   Block size . . . . . 10 records/1 block
   The end of the file should be indicated by 2 successive tape marks (TM) (figure 7-1).
4. HMCS6800 load module data mode. This mode is the object mode output from the assembler HMCS6800.
   Divide the 8-bit code into the upper and lower 4-bit codes, and convert each into hexadecimal notation.
   Example: The code 1100 0110 is as follows under binary notation.

(Upper 4-bits)	(Low 4-bits)	Bit weight
D7 D6 D5 D4	D3 D2 D1 D0	(ROM output
1 1 0 0	0 1 1 0	equivalence)

   The actual load module mode is shown in figure 7-2.

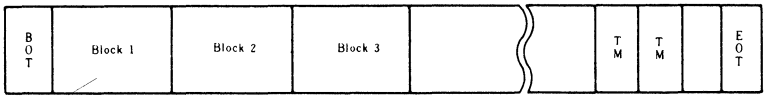


Figure 7-1. Magnetic Tape Format

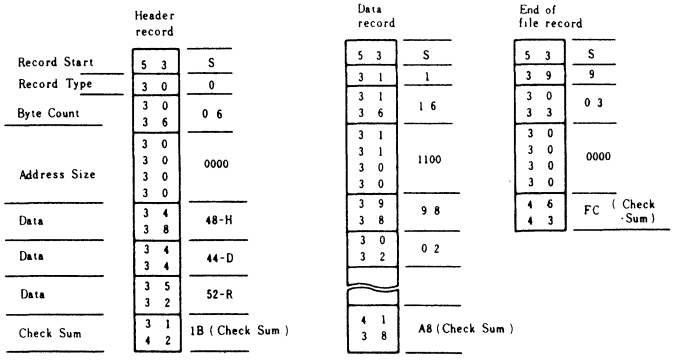


Figure 7-2. HMCS68000 Load Module Data Format

S0 indicates the head of the file and S9 indicates the end of the file. The actual data starts following S1. This means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by counting in increments of 1 byte of the data and checking whether it is sequential or not. The printed example of the HMCS6800 load module mode is as shown in figure 7-3.

```
Header Record  →S00B000058204558414D504CB5
Data Record    →S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data Record    →S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of
File Record    →S9030000FC
```

Figure 7-3. HMCS6800 Load Module Example

If an address is skipped, enter the skipped address into the "ROM Specification Identification Sheet" and the data (00 or FF) entered into the skipped address.

5. BNPF mode

   One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F.

   The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.

   (Example) The code of AA (hexadecimal) is symbolized as shown in figure 7-4.

   It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specification Identification Sheet" always becomes 0.

   B . . . . . Indicates start of 1 word.
   N . . . . . Indicates 1 bit data.
   P . . . . . Indicates 1 bit of 1 data.
   F . . . . . Indicates end of 1 word.

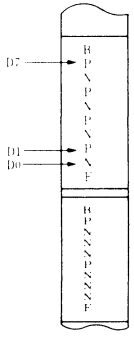


Figure 7-4. BNPF Mode Example

7.3 Specification of Floppy Disk

1. Use the following type of floppy disk (figure 7-5):

   Type. . . . 8 Inch Single Sided and Single Density
   Number of Sectors 26
   Number of Tracks 77

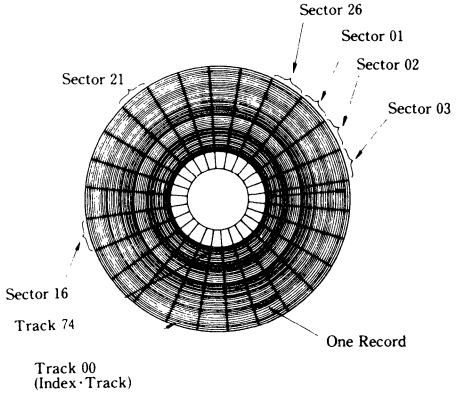


Figure 7-5. Floppy Disk Format

2. Use EBCDIC as the use code.
3. Format the floppy disk as described below. Composition is described in table 7-1.

   Record size . . . . . 80 byte/1 record

Table 7-1. Floppy Disk Composition

No.	Item	Location	
		Track	Sector
1	Standard Volume Label	00	07
2	Standard Head Label	00	08 – 26
3	Data Area	01 – 73	01 – 26
4	Alternal Track	75, 76	01 – 26
5	Spare Track	00 74	01 – 06 01 – 26

Use the sectors as in figure 7-6. Use one sector for one record, that is, 80 bytes out of 128 bytes used for one record.

4. Data Mode. See data mode for magnetic tape.

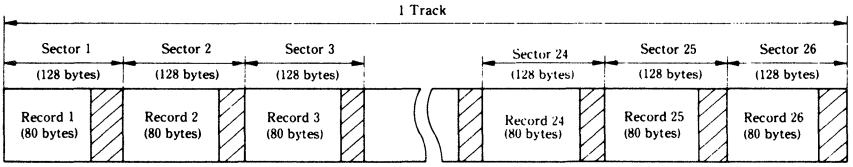


Figure 7-6. Floppy Disk Sector Format

: unused

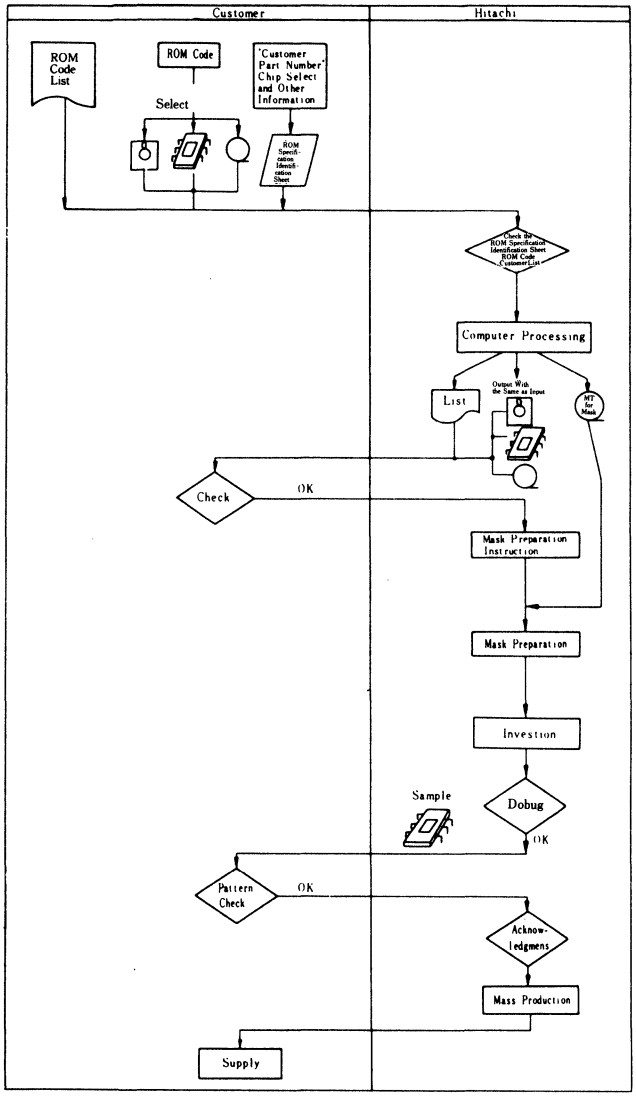


Figure 7-7. Mask ROM Development Flowchart

8. INSTRUCTIONS FOR USING MEMORY DEVICES

8.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled according to the following instructions:

1. In transporting and storing memory devices, put them in conductive magazine or put all pins of each device into a conductive mat so that they are kept at the same potential. Manufacturers should give enough consideration to packing when shipping their products.
2. When devices touch a human body in mounting or inspection, the handler must be grounded. Do not forget to insert a resistor (1MΩ approx is desirable) in series to protect the handles from electrical shock.
3. Keep the relative ambient humidity at about 50% in process.
4. For working clothes, cotton is preferrable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.
6. In transporting the board with memory devices mounted on it, cover it with conductive sheets.
7. Use conductive sheets of high resistance (about 10^9 ohm/□) to protect devices from electrostatic discharge. For, if dropped onto conductive materials like a metal sheet, devices may deteriorate or even breakdown owing to sudden discharge of the charge stored on the surface.
8. Never set the system to which memory devices are applied near anything that generates high voltage (e.g. CRT Anode electrode, etc.).

8.2 Using CMOS Memories

As shown in figure 8-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 8-2 shows the relationship between the input voltage and current in this inverter. The top and bottom transistors turn ON and make current flown when the input voltage becomes intermediate level. Therefore, it is necessary to keep the input voltage below 0.2 V or above V_{CC} − 0.2 V in order to minimize power consumption. The data sheet specifies the stand-by current for both the cases of input level with minimum V_{IH} and maximum V_{IL} and that with 0.2 V or V_{CC} − 0.2 V, and the difference in value is remarkably great. Some memory devices are designed to cut off such current flow in standby mode by the control of input signals, but it depends on device type. This should be confirmed in data sheets for each device type.

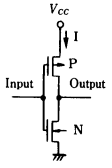


Figure 8-1. CMOS Inverter

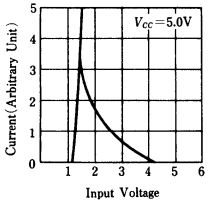


Figure 8-2. Relationship between Input Voltage & Current In CMOS Inverter

Another problem particular to CMOS devices is latch-up. Figure 8-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in figure 8-4. When positive DC current or pulse noise is applied (figure 8-4 (a)), TR3 is turned on owing to the bias voltage generated between base and emitter. And trigger current flows into GND through R_P, the base resistance of TR2. As a result, TR2 becomes conductive and current flows from power supply (V_{CC}) through the base resistance of TR1 (R_N), which puts TR1 into conduction, too. Then, as the base of TR2 is rebiased by collector current from TR1, the closed loop consisting of TR1 and TR2 reacts. Thus current flows constantly between power supply (V_{CC}) and GND even without trigger current caused by outside noise.

Latch-up can be caused by a negative pulse, too (figure 8-4 (bb)). Most of semiconductor memory manufacturers are trying to improve latch-up immunity of their products. Hitachi provides enough guard band by applying diffusion layer around inputs and outputs, taking care not to connect input to p^+ diffusion layer. Input voltage for 64 kbit

static RAM HM6264A, for example, is specified as follows:

V_{IH} max 6.0 V (not depending on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
−0.3 V (DC level)

Thus almost no consideration for latch-up is required in system design.

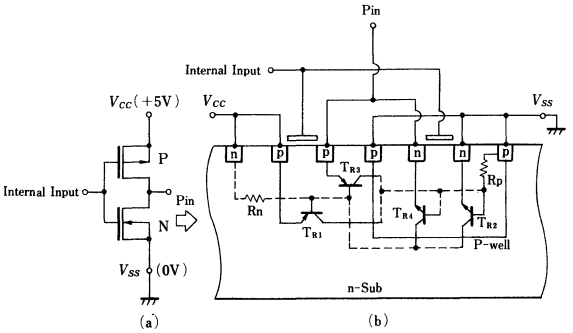


Figure 8-3. Cross Section Structure of CMOS Inverter

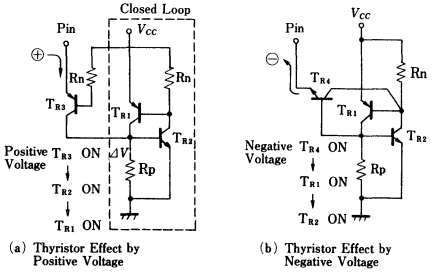


Figure 8-4. Equivalent Circuit of Parasitic Thyristor

8.3 Noise Prevention

Noise in semiconductor memories is roughly classified into input signal noise and power supply noise.

8.3.1 Input Signal Noise

Input signal noise is caused by overshoot and undershoot. If either of them is out of recommended DC operating conditions, normal operation is hindered, and voltage over absolute maximum rating will break the device. In operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohm into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because it is often caused by unstable reference voltage (GND level).

8.3.2 Power Supply Noise

The power source noise can be classed as low-frequency noise and high-frequency noise as shown in figure 8-5. To assure stable memory operation, the peak-to-peak power supply voltage in the presence of low-or high-frequency noise should be held below 10 percent of its standard level.

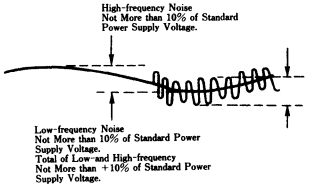


Figure 8-5. Power Source Noise

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1 – 0.01 μF should be inserted near the device. The following points must be considered in designing pattern of the board:

★ For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.

★ Bypass capacitors must be applied as near to the power supply pin of memory devices as possible, and inductance in the path from V_{CC} pin to V_{SS} pin through the bypass capacitor must be as little as possible.

★ The line connected to the power supply on the board should be as wide as possible.

★ It is preferrable for the power supply line to be at right angles to devices selected at the same time, lest too much peak current should flow through one power supply line at a time.

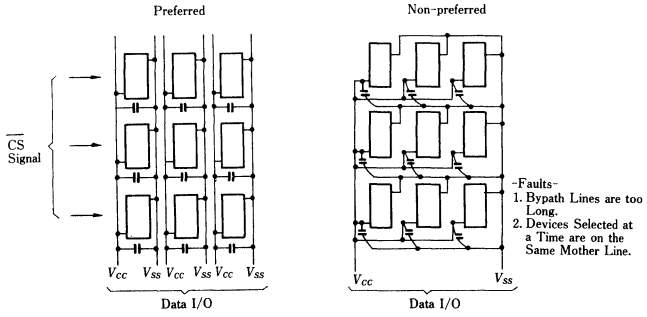


Figure 8-6. Examples of Power Supply Board Pattern

DATA SHEETS

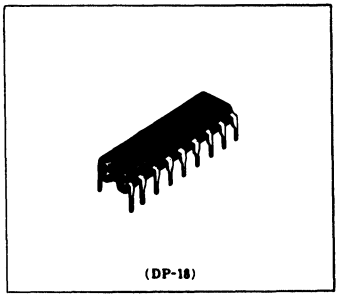
MOS STATIC RAM

HM6147H Series——Maintenance Only

4096-word x 1-bit High Speed CMOS Static RAM

■FEATURES

- High Speed: Fast Access Time 35ns/45ns/55ns (max.)
- Low Power Standby and Low Power Operation,
  Standby: 100μW (typ.)/5μW (typ.) (L-version),
  Operation: 150mW typ.
- Single 5V Supply and High Density 18 Pin Package
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capability of Battery Back Up Operation (L-version)

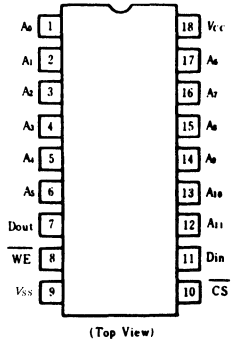


(DP-18)

■ORDERING INFORMATION

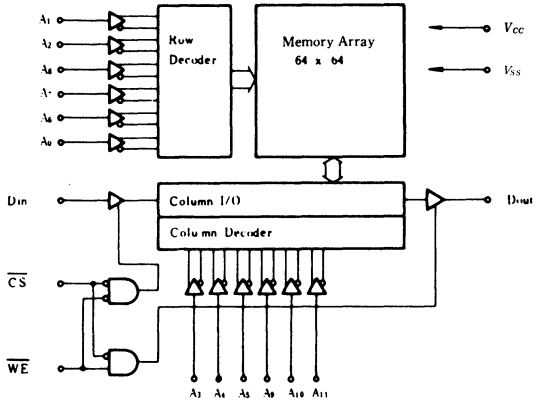
Type No.	Access Time	Package
HM6147HP-35 HM6147HP-45 HM6147HP-55	35ns 45ns 55ns	300mil 18pin Plastic DIP
HM6147HLP-35 HM6147HLP-45 HM6147HLP-55	35ns 45ns 55ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to V_{SS}	V_T	−0.5*1 to +7.0	V
DC Output Current	I_o	20	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature under bias	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note) *1 −3.5V for pulse width≤20ns

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq Ta \leq 70°C$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

Note) *1. −3.0V for pulse width≦20ns

■DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	Test Condition	min	typ*2	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, V_{SS} to V_{CC}	—	—	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{out}=V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current (1)	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current (2)	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current (1)	I_{SB}	$\overline{CS}=V_{IH}$, V_{CC}=Min to Max	—	8	20	mA
			—	5*3	15*3	
Standby Power Supply Current (2)	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	20	800	μA
			—	1*3	100*3	
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.40	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Notes) *1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute.
*2. Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and Specified loading.
*3. This characteristics are guaranteed only for L-version.

■CAPACITANCE ($Ta=25°C$, $f=1.0MHz$)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	6	pF

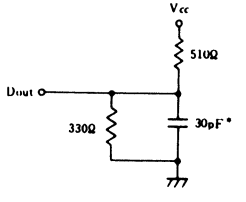
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%)

• AC TEST CONDITIONS

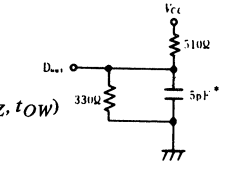
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels: 1.5V (HM6147H-35)
  0.8 to 2.0V (HM6147H-45/55)

Output Load A



* Including scope & jig capacitance

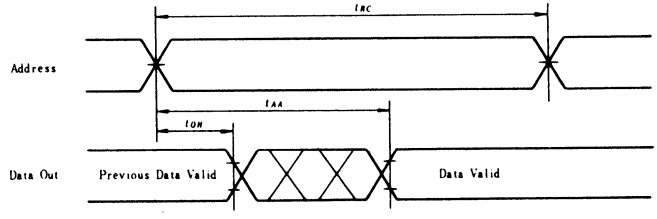
Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})



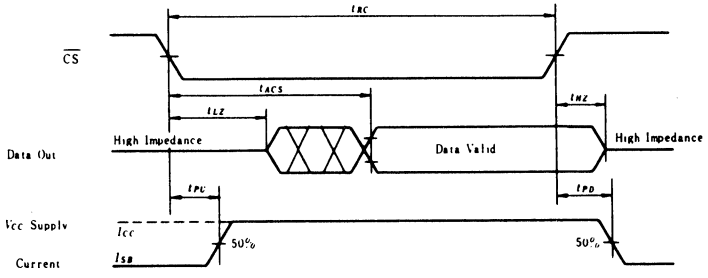
● READ CYCLE

Parameter	Symbol	HM6147H-35		HM6147H-45		HM6147H-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns	(1)
Address Access Time	t_{AA}	—	35	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	(2), (3), (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	20	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1 (4) (5)



● TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)

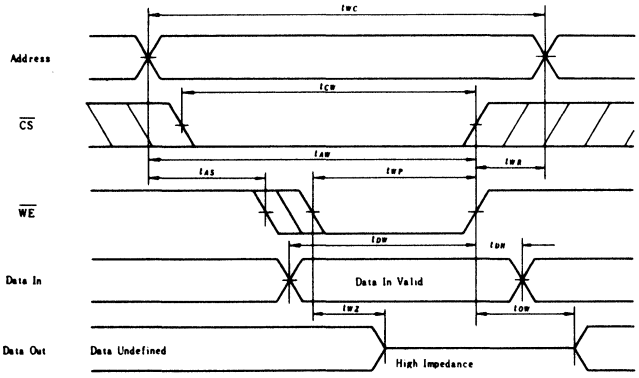


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, $\overline{CS}=V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

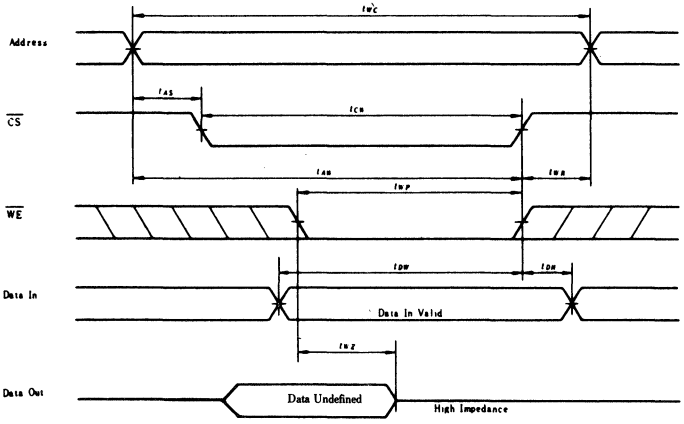
● WRITE CYCLE

Parameter	Symbol	HM6147H-35		HM6147H-45		HM6147H-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns	[2]
Chip Selection to End of Write	t_{CW}	35	—	45	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	10	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	30	ns	[3], [4]
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	[3], [4]

● TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.
5. $\overline{CS}$ or $\overline{WE}$ is high for address transition.

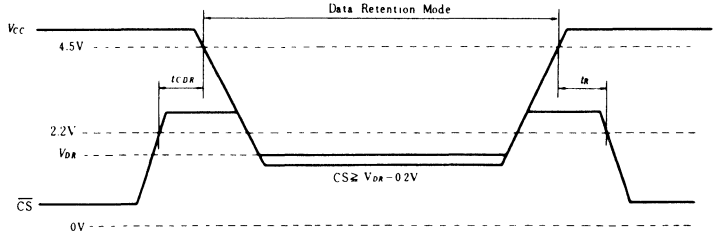
■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0℃ to +70℃)

This characteristics are guaranteed only for L-version.

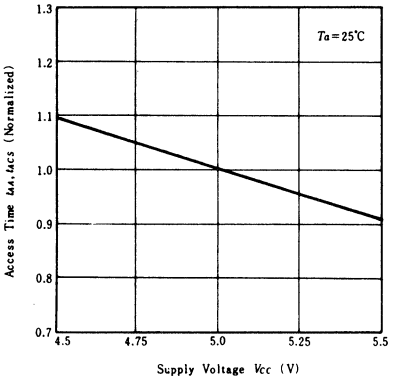
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS} \geq 2.8V$ $V_{IN} \geq 2.8V$ or $V_{IN} \leq 0.2V$	—	—	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*1	—	—	ns

Note) *1. t_{RC}= Red Cycle Time.

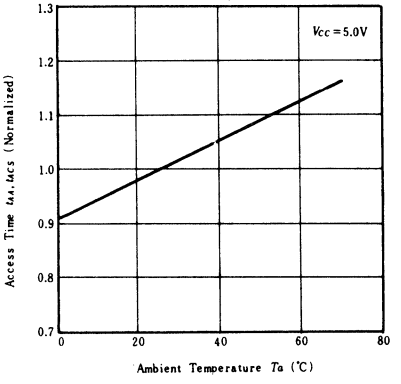
●LOW V_{CC} DATA RETENTION WAVEFORM



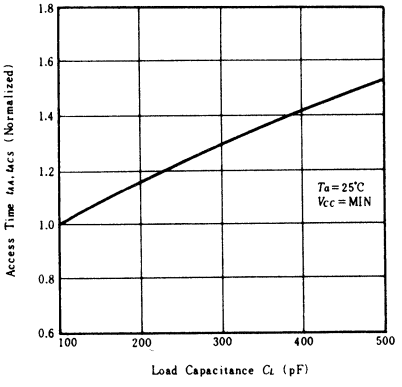
ACCESS TIME VS. SUPPLY VOLTAGE



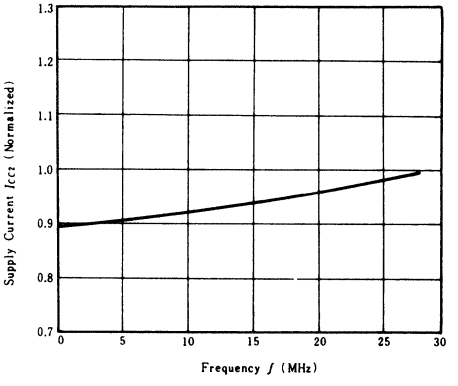
ACCESS TIME VS. AMBIENT TEMPERATURE



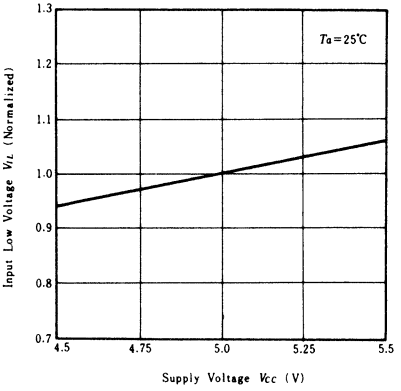
ACCESS TIME VS. LOAD CAPACITANCE



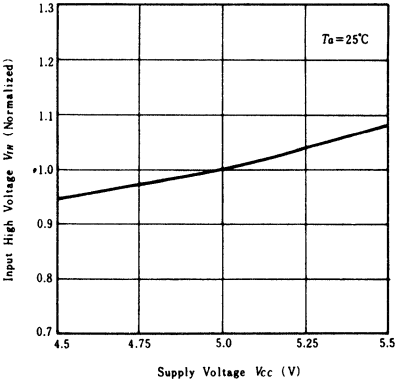
SUPPLY CURRENT VS. FREQUENCY



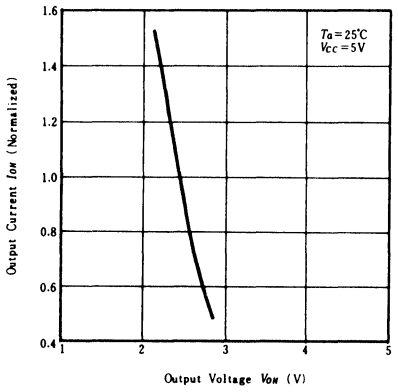
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



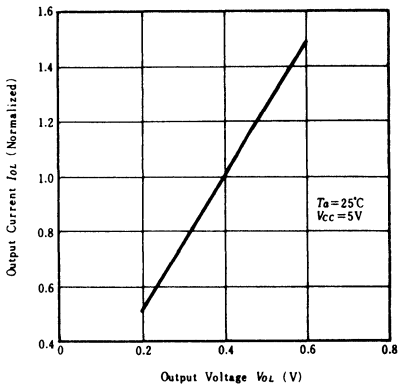
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



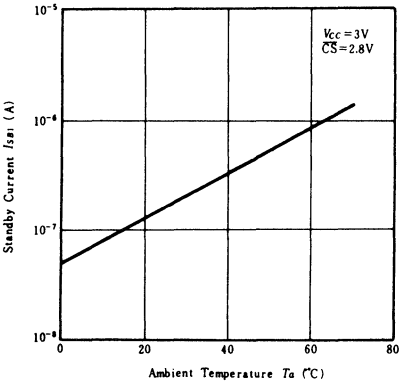
OUTPUT CURRENT VS. OUTPUT VOLTAGE



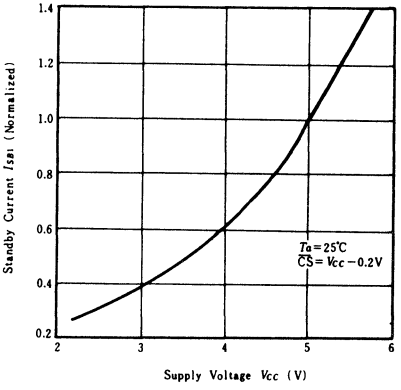
OUTPUT CURRENT VS. OUTPUT VOLTAGE



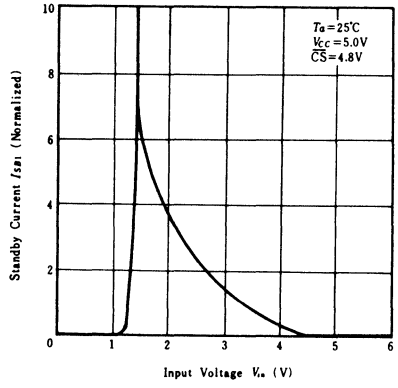
STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE



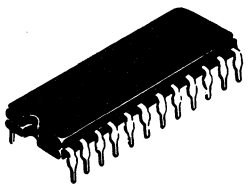
HM6116 Series —— Maintenance Only

2048-word x 8-bit High Speed CMOS Static RAM

■FEATURES

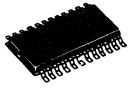
- Single 5V Supply
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.), 10μW (typ.) (L-version)
  - Operation: 180mW (typ.), 160mW (typ.) (L-version)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116P Series



(DP-24)

HM6116FP Series

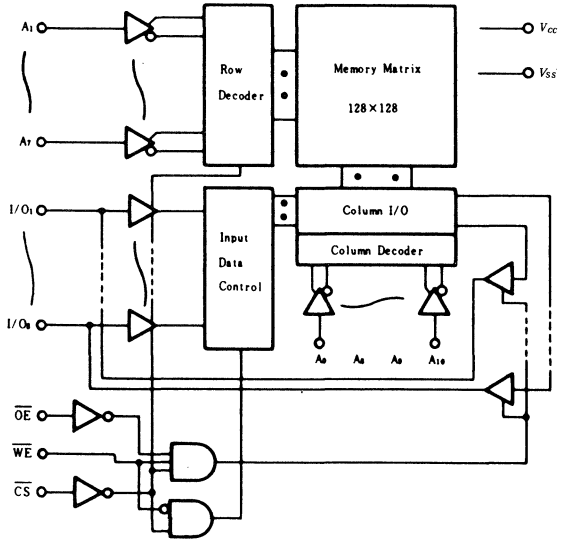


(FP-24D)

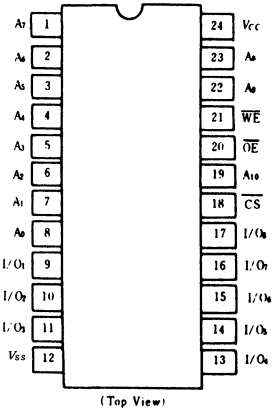
■ORDERING INFORMATION

Type No.	Access Time	Package
HM6116P-2 HM6116P-3 HM6116P-4	120ns 150ns 200ns	600mil 24pin Plastic DIP
HM6116LP-2 HM6116LP-3 HM6116LP-4	120 ns 150 ns 200 ns	
HM6116FP-2 HM6116FP-3 HM6114FP-4	120 ns 150 ns 200 ns	24pin Plastic SOP
HM6116LFP-2 HM6116LFP-3 HM6116LFP-4	120 ns 150 ns 200 ns	

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

Note) This device is not available for new application.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.5V for pulse width≦50ns

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−0.3*1	—	0.8	V

Note) *1. −3.0V for pulse width≦50ns.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116-2			HM6116-3/-4			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	—	—	10	—	—	10	μA
			—	—	2*3	—	—	2*3	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	—	—	10	—	—	10	μA
			—	—	2*3	—	—	2*3	
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
			—	35*3	70*3	—	30*3	60*3	
	I_{CC1}*2	$V_{I/O}$=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
			—	30*3	—	—	25*3	—	
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
			—	35*3	70*3	—	30*3	60*3	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	5	15	—	5	15	mA
			—	4*3	12*3	—	4*3	12*3	
	I_{SB1}	$\overline{CS}$≧V_{CC}−0.2V, V_{in}≧V_{CC}−0.2V or V_{in}≦0.2V	—	0.02	2	—	0.02	2	μA
			—	2*3	50*3	—	2*3	50*3	
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

Notes) *1. V_{CC}=5V, Ta=25°C
*2. Reference Only
*3. This characteristics are guaranteed only for L-version.

■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

●READ CYCLE

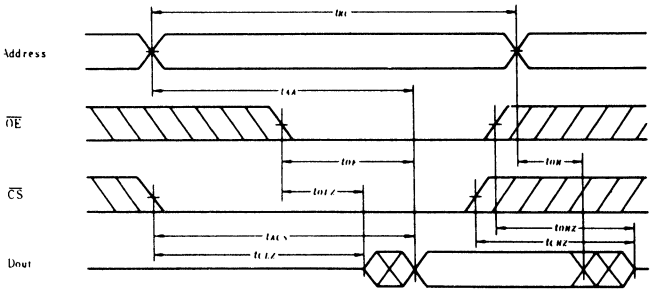
Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

●WRITE CYCLE

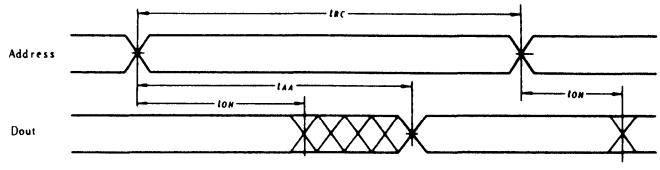
Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■TIMING WAVEFORM

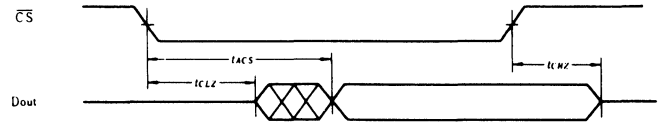
●READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]

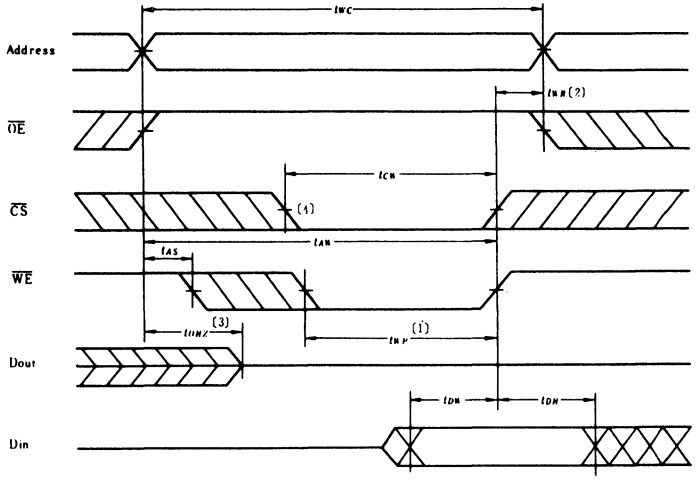


● READ CYCLE (3)[1][3][4]

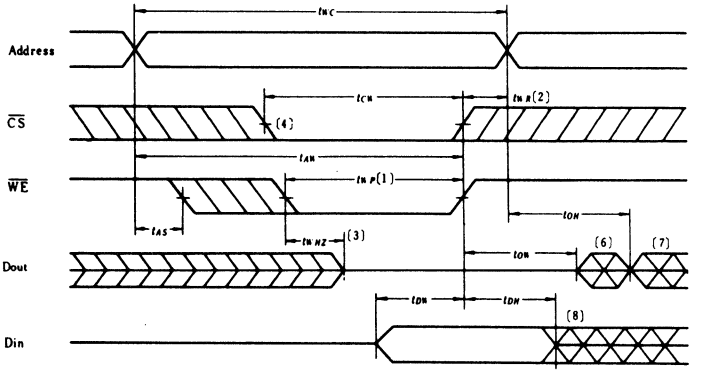


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE (1)



● WRITE CYCLE (2)[5]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

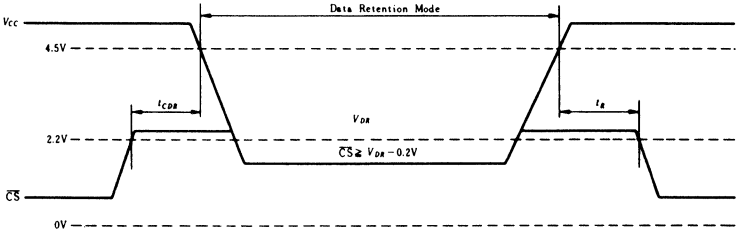
■ LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

This characteristics are guaranteed only for L-version.

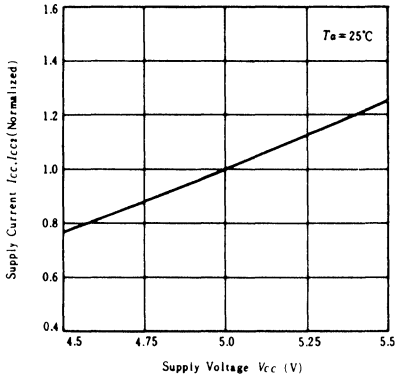
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{in} \geq V_{CC} - 0.2V$ or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR} *1	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$, $V_{in} \geq 2.8V$ or $V_{in} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *2	—	—	ns

Notes) *1. 10μA max at $Ta = 0°C$ to $+40°C$, V_{IL} min $= -0.3V$
*2. t_{RC} = Real Cycle Time.

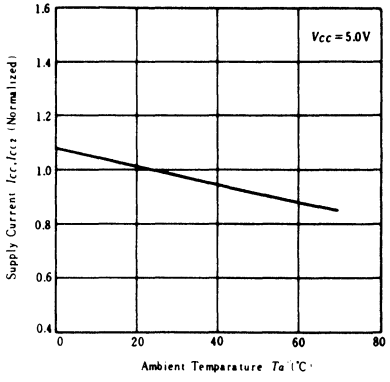
● Low Vcc Data Retention Waveform



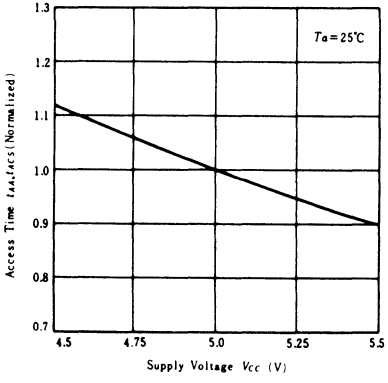
SUPPLY CURRENT vs. SUPPLY VOLTAGE



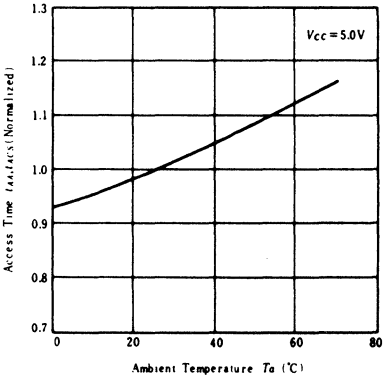
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



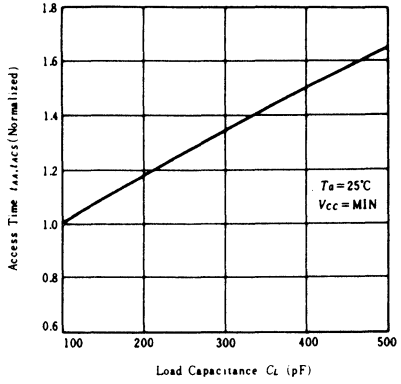
ACCESS TIME vs. SUPPLY VOLTAGE



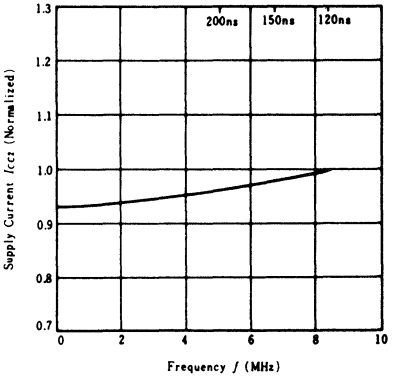
ACCESS TIME vs. AMBIENT TEMPERATURE



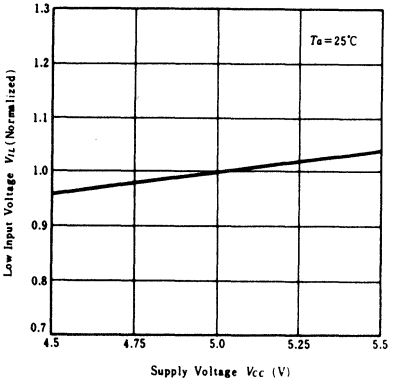
ACCESS TIME vs. LOAD CAPACITANCE



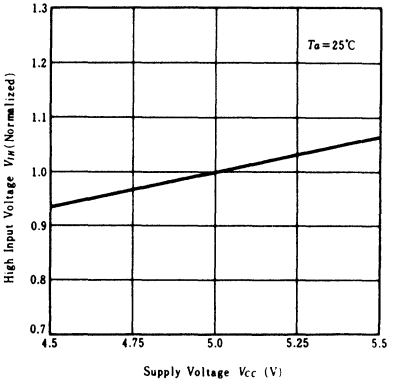
SUPPLY CURRENT vs. FREQUENCY



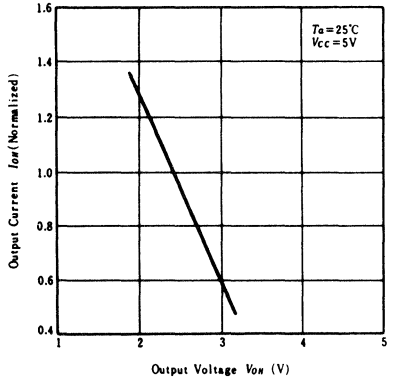
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



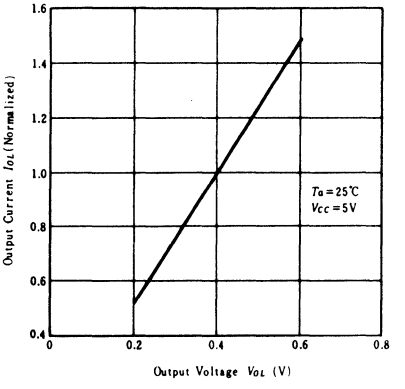
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



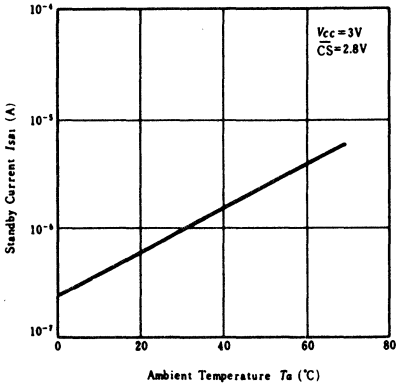
OUTPUT CURRENT vs. OUTPUT VOLTAGE



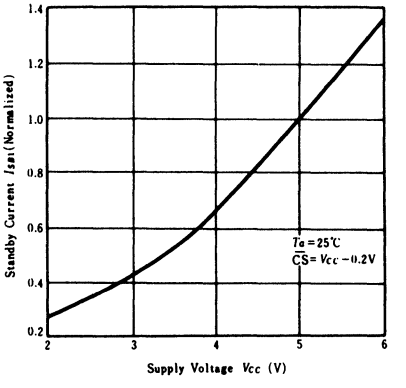
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



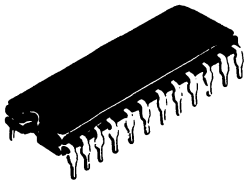
HM6116A Series ——— Maintenance Only

2048-word × 8-bit High Speed Static CMOS RAM

■ FURTURES

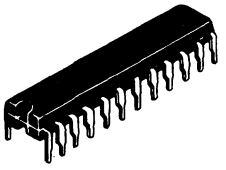
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.)
    5μW (typ.) (L-version)
  - Operation: 15mW (typ.) (f = 1 MHz)
    10 mW (typ.) (L-version)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116AP Series



(DP-24)

HM6116ASP Series

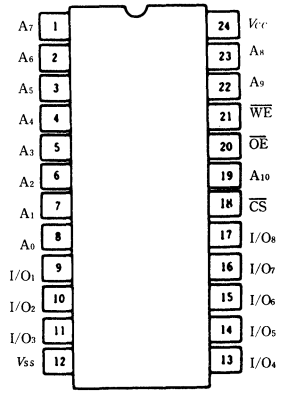


(DP-24N)

■ ORDERING INFORMATION

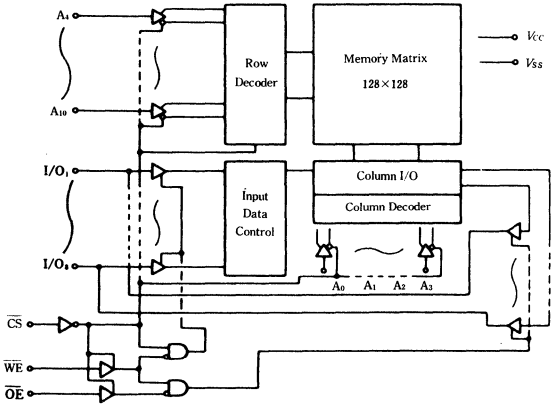
Type No.	Access Time	Package
HM6116AP-12	120ns	600mil 24pin Plastic DIP
HM6116AP-15	150ns	
HM6116AP-20	200ns	
HM6116ALP-12	120ns	
HM6116ALP-15	150ns	
HM6116ALP-20	200ns	
HM6116ASP-12	120ns	300mil 24pin Plastic DIP
HM6116ASP-15	150ns	
HM6116ASP-20	200ns	
HM6116ALSP-12	120ns	
HM6116ALSP-15	150ns	
HM6116ALSP-20	200ns	

■ PIN ARRANGEMENT



(Top View)

■ FUNCTIONAL BLOCK DIAGRAM



Note) This device is not available for new application.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5^{*1} to $+7.0$	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.5V for pulse width≦50ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-0.3^{*1}	—	0.8	V

Note) *1. −3.0V for pulse width≦50ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	HM6116A-12			HM6116A-15			HM6116A-20			Unit
			min	typ*1	max	min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=V_{SS} to V_{CC}	–	–	2	–	–	2	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2	–	–	2	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	5	15	–	5	15	–	5	15	mA
		V_{in}=V_{IH} or V_{IL}	–	4*2	12*2	–	4*2	12*2	–	4*2	12*2	
	I_{CC1}	V_{IH}=V_{CC}, V_{IL}=0V, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, f=1MHz	–	3	6	–	3	6	–	3	6	mA
			–	2*2	5*2	–	2*2	5*2	–	2*2	5*2	
Average Operating Current	I_{CC2}	min. cycle duty = 100%	–	35	60	–	25	45	–	20	35	mA
			–	30*2	50*2	–	20*2	40*2	–	15*2	30*2	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	1	4	–	1	4	–	1	4	mA
			–	0.5*2	3*2	–	0.5*2	3*2	–	0.5*2	3*2	
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V	–	0.02	2	–	0.02	2	–	0.02	2	mA
			–	1*2	50*2	–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 4mA	–	–	0.4	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	2.4	–	–	2.4	–	–	V

Notes) *1. V_{CC}=5V, T_a=25°C
*2. This characteristics is guaranteed only for L-version.

■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

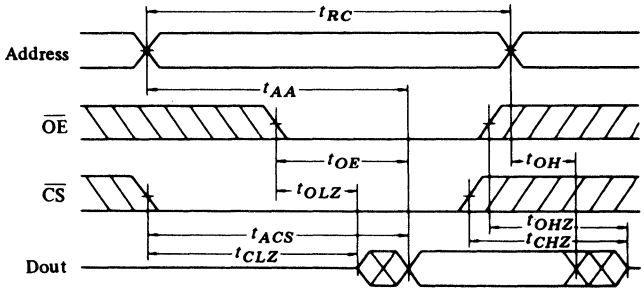
Item	Symbol	HM6116A-12		HM6116A-15		HM6116A-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	–	150	–	200	–	ns
Address Access Time	t_{AA}	–	120	–	150	–	200	ns
Chip Select Access Time	t_{ACS}	–	120	–	150	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	ns
Output Enable to Output Valid	t_{OE}	–	55	–	60	–	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	–	15	–	20	–	ns

● WRITE CYCLE

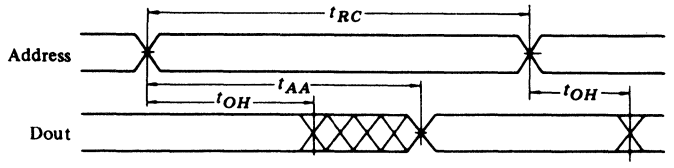
Item	Symbol	HM6116A-12		HM6116A-15		HM6116A-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	70	–	80	–	100	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	10	–	10	–	10	–	ns

■TIMING WAVEFORM

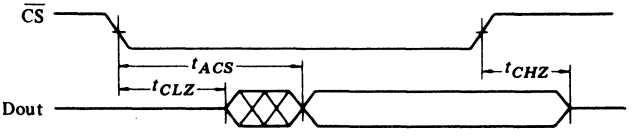
●READ CYCLE (1)[1]



● READ CYCLE (2) [1][2][4]

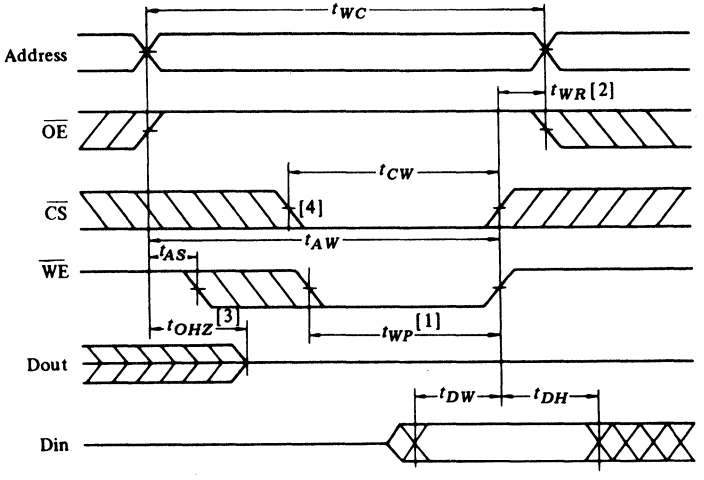


● READ CYCLE (3) [1][3][4]

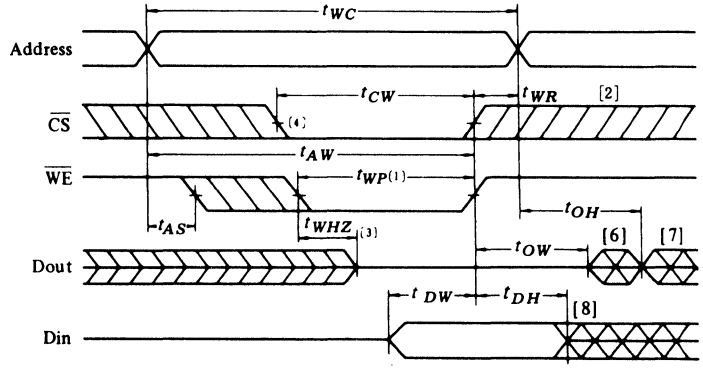


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE(1)



● **WRITE CYCLE (2)** [5]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

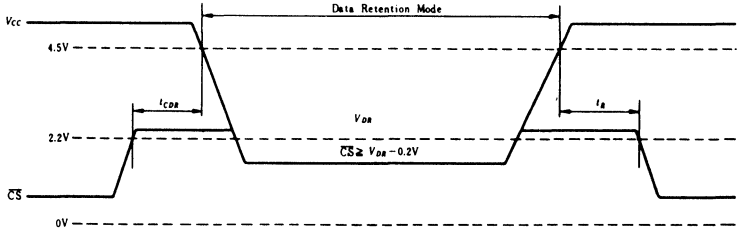
■ LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

This characteristics is guaranteed only for L-version.

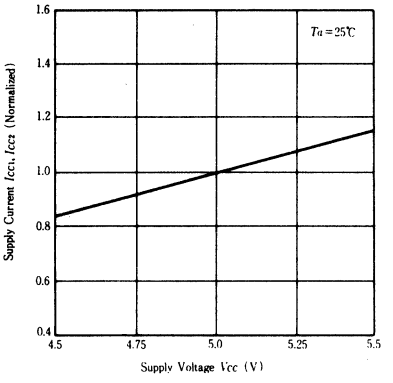
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*1	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*2	—	—	ns

Notes) *1. 10μA max at $Ta = 0°C$ to $+40°C$, V_{IL} min $= -0.3V$
*2. t_{RC} = Read Cycle Time.

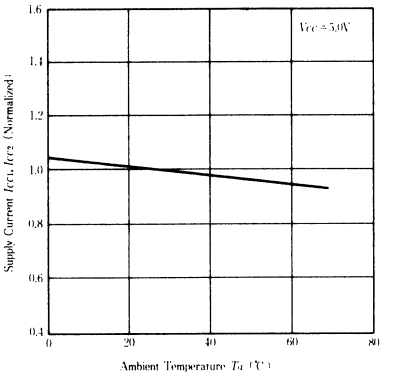
● **Low Vcc Data Retention Waveform**



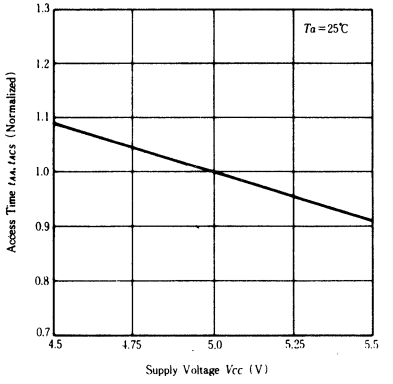
SUPPLY CURRENT VS. SUPPLY VOLTAGE



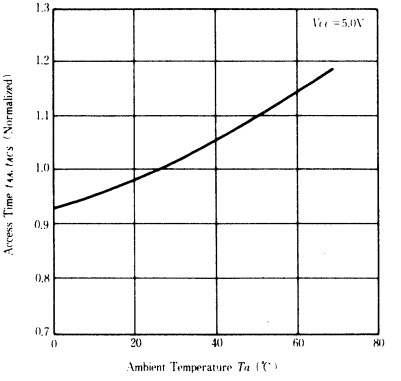
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



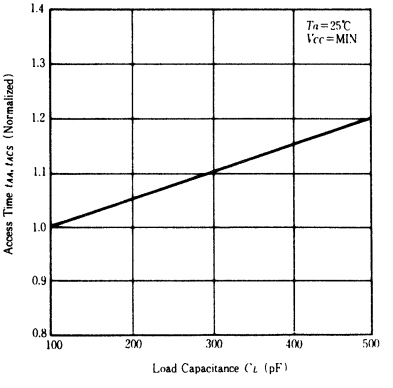
ACCESS TIME VS. SUPPLY VOLTAGE



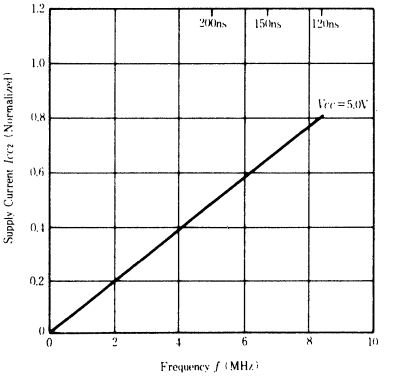
ACCESS TIME. VS. AMBIENT TEMPERATURE



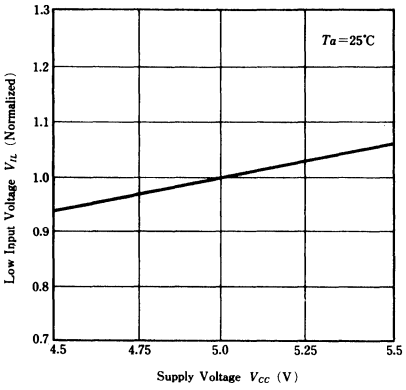
ACCESS TIME VS. LOAD CAPACITANCE



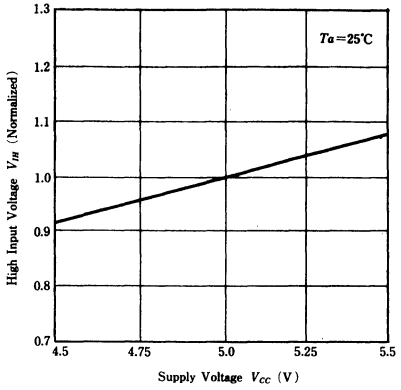
SUPPLY CURRENT VS. FREQUENCY



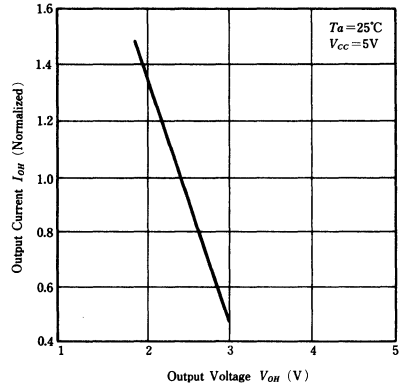
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



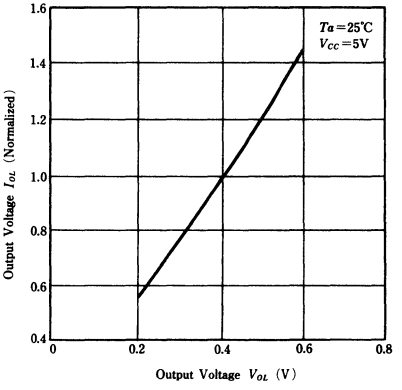
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



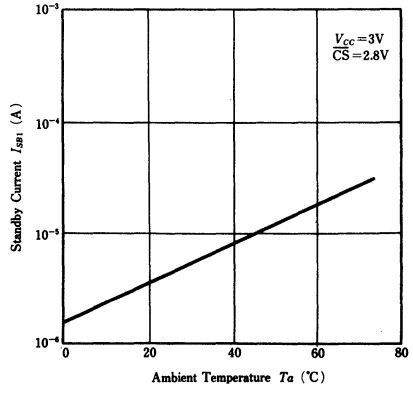
OUTPUT CURRENT VS. OUTPUT VOLTAGE



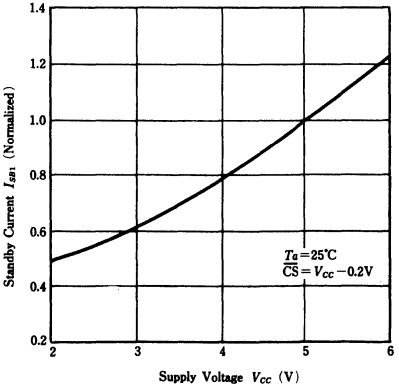
OUTPUT CURRENT VS. OUTPUT VOLTAGE



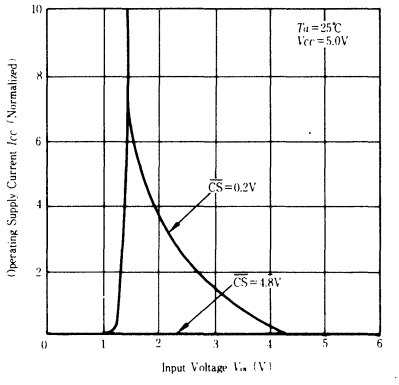
STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE

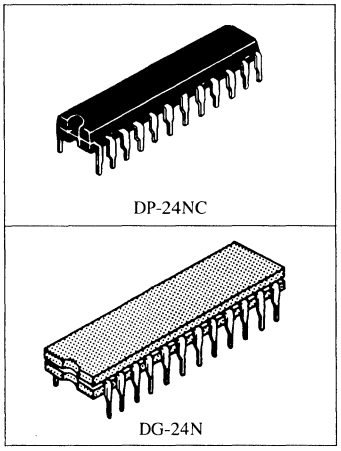


OPERATING SUPPLY CURRENT VS. INPUT VOLTAGE



HM6716 Series
HM6719 Series

2048-word x 8-bit High Speed Static RAM
2048-word x 9-bit High Speed Static RAM



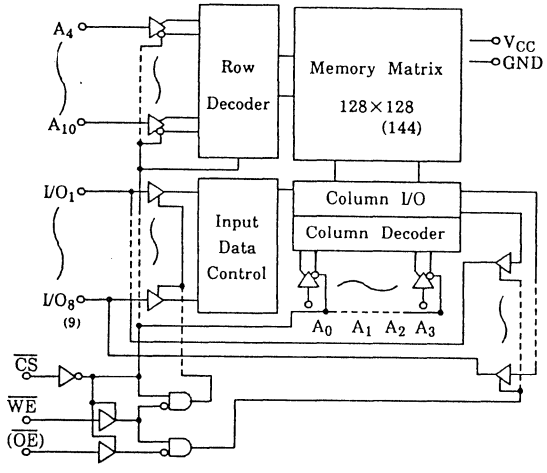
■ Features

- Fast Access Time: 25/30ns (max)
- Low Power Dissipation (DC): 280mW (typ.)
- +5V Single Supply
- Completely Static Memory No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- Skinny 24-pin Cerdip (300mil) and Plastic DIP (300mil)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6716-25	25ns	300 mil 24 Pin Cerdip and Plastic DIP
HM6716-30	30ns	
HM6719-25	25ns	
HM6719-30	30ns	

■ Block Diagram

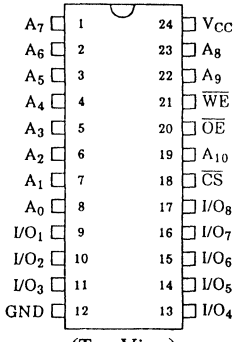


■ Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to GND Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

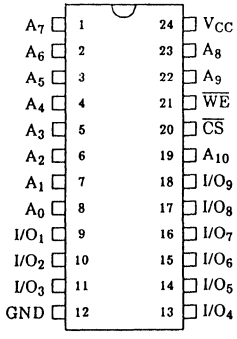
■ PIN ARRANGEMENT

● **HM6716**



(Top View)

● **HM6719**



(Top View)

■ Truth Table

● HM6716

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

● HM6719

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (2) (3)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

■ Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}*)	−3.0	–	0.8	V

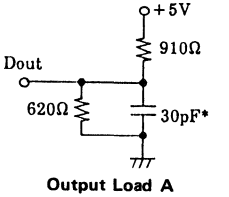
*) Pulse Width: 20ns, DC: −0.5V

■ DC and Operating Characteristics (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

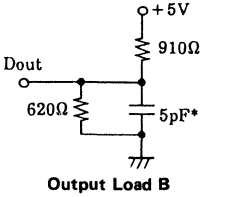
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=0V to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	–	120	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	–	–	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, $I_{I/O}$=0mA	–	–	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	I_{OL}=4mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1mA	2.4	–	–	V

■ AC Test Conditions

Input pulse levels: GND to 3.0V
Input and Output reference levels: 1.5V ±200mV from steady level (Output Load B)
Input rise and fall time: 4ns
Output Load: See Figure



Output Load A



Output Load B
(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW})

*including scope and jig

■ **Capacitance** (T_a = 25°C, f = 1.0 MHz)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	–	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	8	pF

Note) This parameter is sampled and not 100%, tested.

■ **AC Characteristics** (V_{CC} 5V ± 10%, T_a = 0 to +70°C, unless otherwise noted.)

● **READ CYCLE**

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	–
Address Access Time	t_{AA}	–	25	–	30	ns	–
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	–
Chip Selection to Output in Low Z	t_{CLZ}	0	–	0	–	ns	*2
Output Enable to Output Valid	t_{OE}	0	20	0	20	ns	*1
Output Enable to Output in Low Z	t_{OLZ}	0	–	0	–	ns	*1, *2
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns	*2
Chip Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–

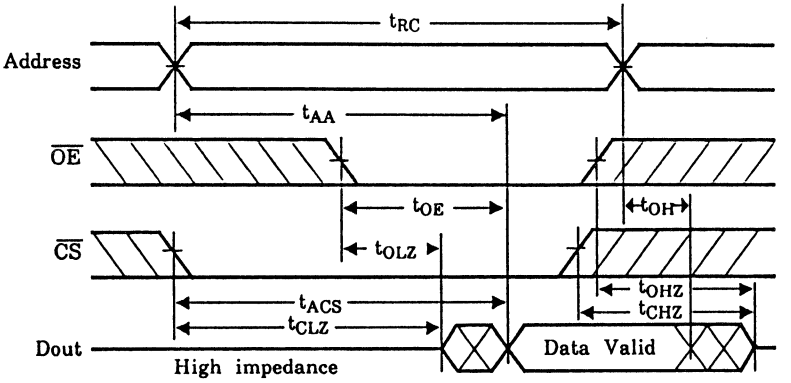
● **Write Cycle**

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	25	–	30	–	ns	–
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	–
Write Pulse Width	t_{WP}	20	–	25	–	ns	–
Write Recovery Time	t_{WR}	0	–	0	–	ns	–
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Write to Output in High Z	t_{WHZ}	0	10	0	12	ns	*2
Data Valid to End of Write	t_{DW}	15	–	15	–	ns	–
Data Hold Time	t_{DH}	5	–	5	–	ns	–
Output Active from End of Write	t_{OW}	0	–	0	–	ns	–

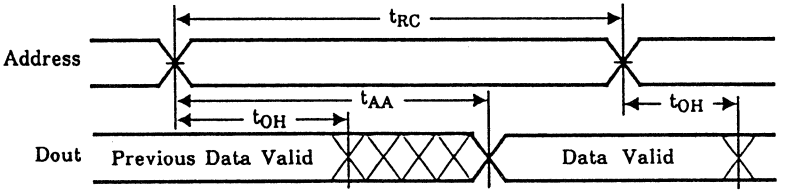
Notes) *1. These parameters are for HM6716.
*2. Transition is measured ±200mV from steady state voltage with Load(B).
This parameter is sampled and not 100% tested.

■ Timing Waveforms

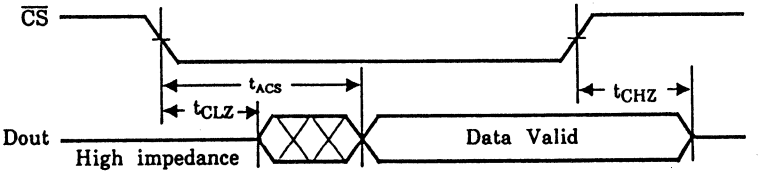
● Read Cycle (1)*1



● Read Cycle (2)*1,*2,*4

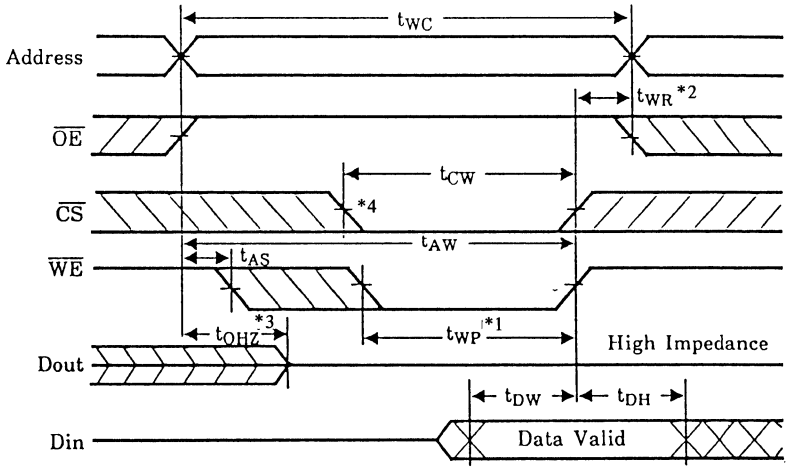


● Read Cycle (3)*1,*3,*4

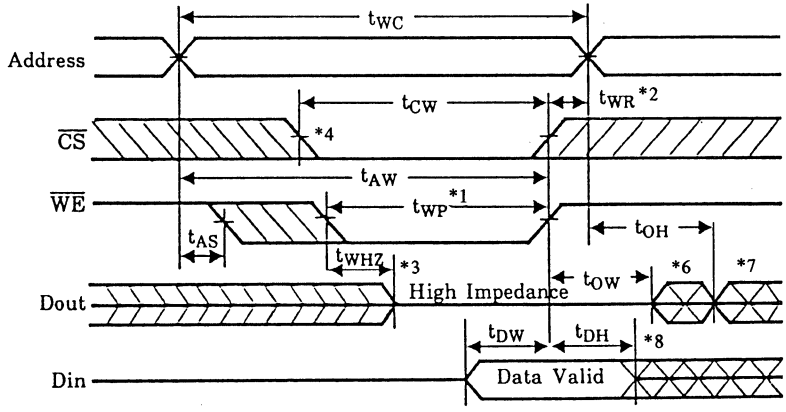


Notes) *1. $\overline{WE}$ is High for Read Cycle.
*2. Device is continuously selected, $\overline{CS}=V_{IL}$.
*3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
*4. $\overline{OE}=V_{IL}$.

- **Write Cycle (1)**



- **Write Cycle (2)** *5



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL}).
*6. Dout is the same phase of write data of this write cycle.
*7. Dout is the read data of next address.
*8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

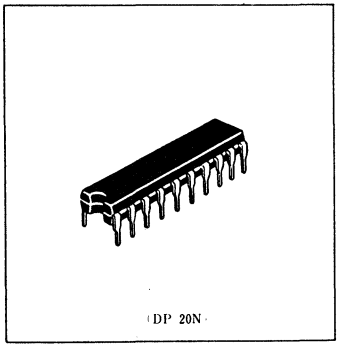
HM6168H Series — Maintenance Only

(Substitute HM6268P)

4096-word x 4-bit High Speed CMOS Static RAM

■FEATURES

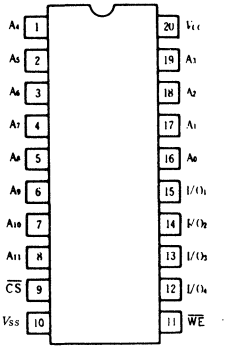
- High Speed: Fast Access Time 45/55/70 ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby: 100μW typ, 5μW typ. (L-version)
  Active: 200mW typ.
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)



■ORDERING INFORMATION

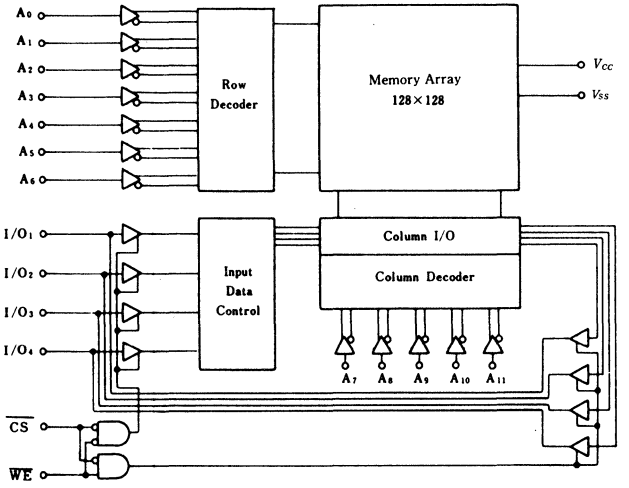
Type No.	Access Time	Package
HM6168HP-45	45ns	300mil 20pin Plastic DIP
HM6168HP-55	55ns	
HM6168HP-70	70ns	
HM6168HLP-45	45ns	
HM6168HLP-55	55ns	
HM6168HLP-70	70ns	

■PIN ARRANGEMENT



(Top View)

■FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. 3.5V for pulse width≦20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to + 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}= V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ =V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$= V_{IL}, $I_{I/O}$=0mA	–	40	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$= V_{IH}	–	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\overline{CS}$= V_{CC}−0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	–	0.02	2.0	mA
			–	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (Ta=25°C, f=1MHz)

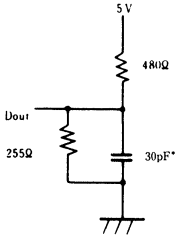
Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note: This parameters are sampled and not 100% tested.

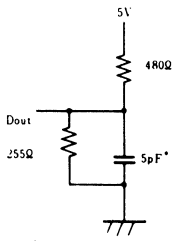
■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to + 70°C, unless otherwise noted.)

• AC TEST CONDITION

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure



Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

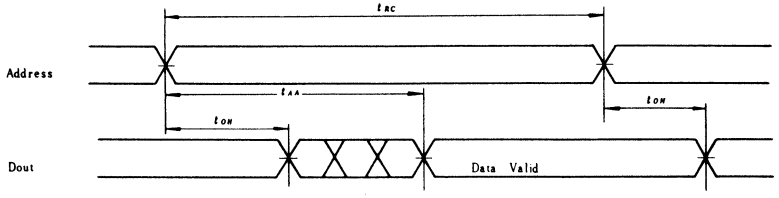
* Including scope and jig.

• READ CYCLE

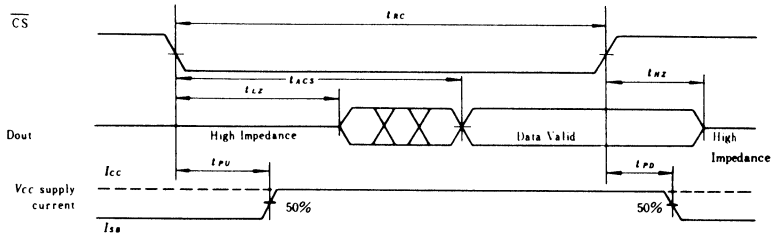
Item	Symbol	HM6168H-45		HM6168H-55		HM6168H-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns
Address Access Time	t_{AA}	–	45	–	55	–	70	ns
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns
Chip Selection to Output in Low Z*1	t_{LZ}	20	–	20	–	20	–	ns
Chip Deselection to Output in High Z*1	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	–	30	ns

Note) *1. Transition is measured ±500mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1(1), (2)



• TIMING WAVEFORM OF READ CYCLE NO. 2[1], [3]



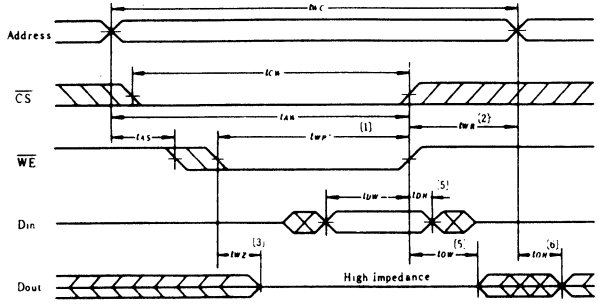
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE

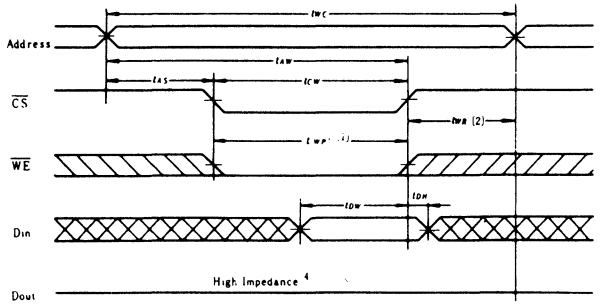
Item	Symbol	HM6168H-45		HM6168H-55		HM6168H-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns
Chip Selection to End of Write	t_{CW}	40	–	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	40	–	50	–	60	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	35	–	45	–	55	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	25	–	30	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns
Write Enabled to Output in High Z*1	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*1	t_{OW}	0	–	0	–	0	–	ns

Note) *1. Transition is measured ±500mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$, (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of Write data of this write cycle, if t_{WR} is long enough.

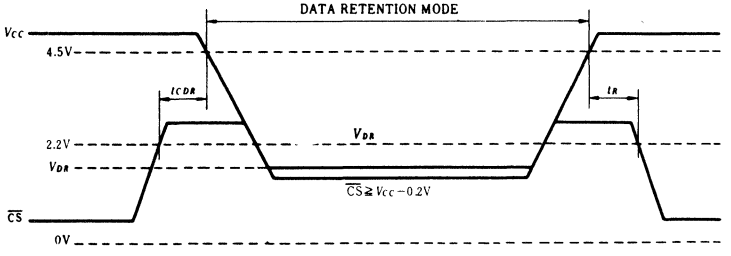
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics is guaranteed only for L-version.

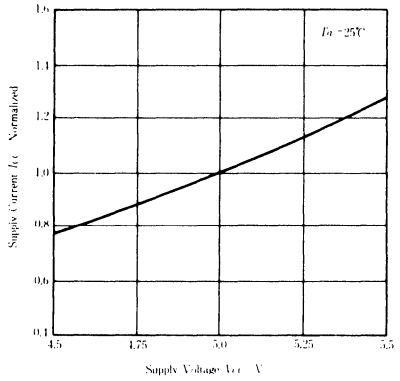
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time.
*2. V_{CC} = 3.0V
*3. V_{CC} = 2.0V

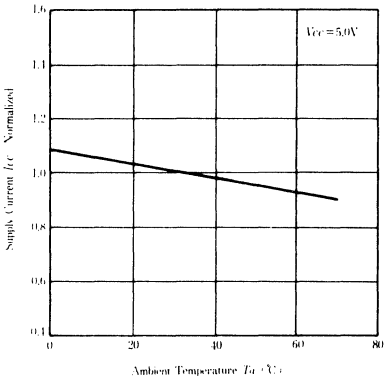
●LOW V_{CC} DATA RETENTION WAVEFORM



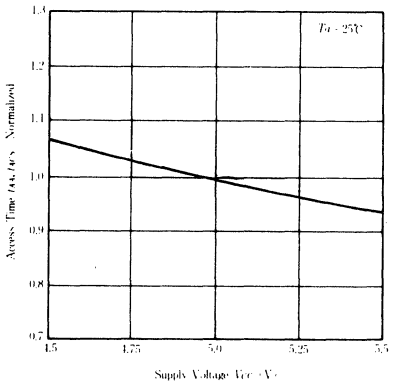
SUPPLY CURRENT VS. SUPPLY VOLTAGE



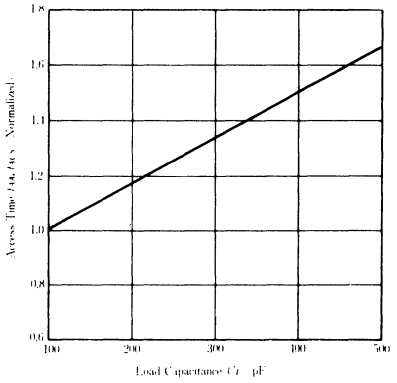
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



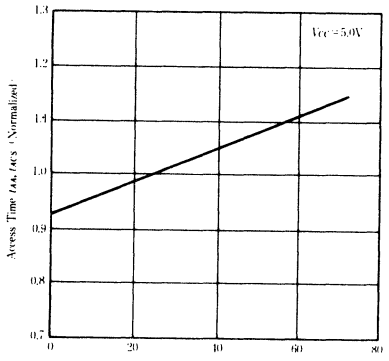
ACCESS TIME VS. SUPPLY VOLTAGE



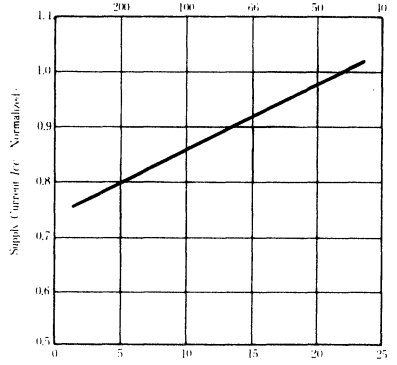
ACCESS TIME VS. LOAD CAPACITANCE



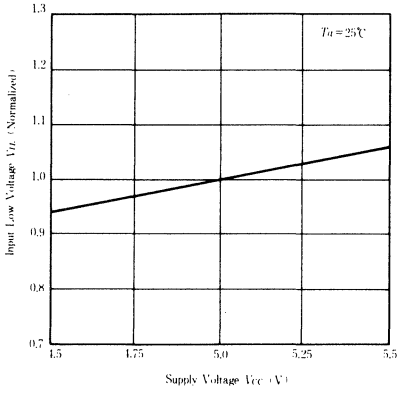
ACCESS TIME VS. AMBIENT TEMPERATURE



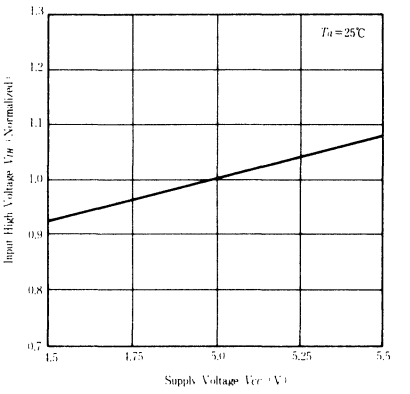
SUPPLY CURRENT VS. FREQUENCY



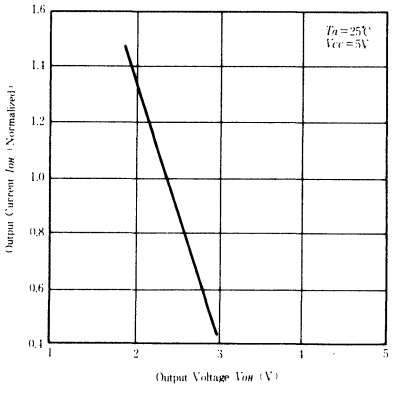
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



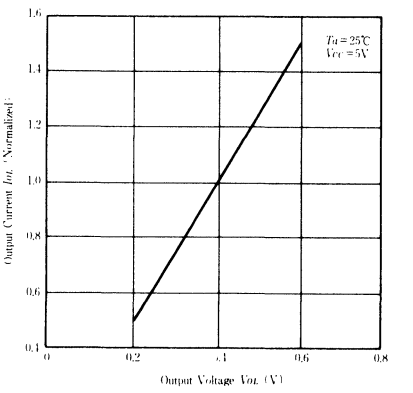
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



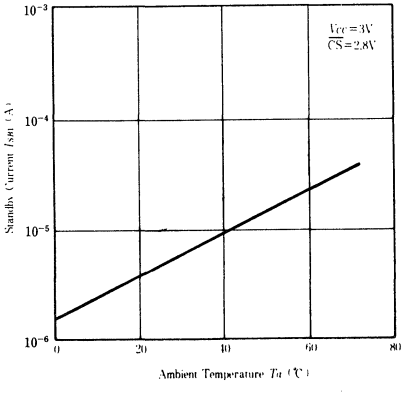
OUTPUT CURRENT VS. OUTPUT VOLTAGE



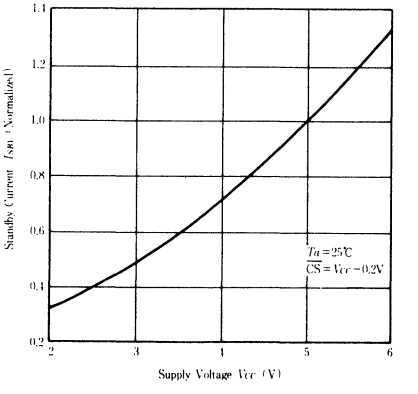
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE

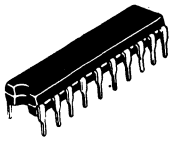


STANDBY CURRENT VS. SUPPLY VOLTAGE



HM6268P Series

4096-word x 4-bit High Speed CMOS Static RAM



(DP-20N)

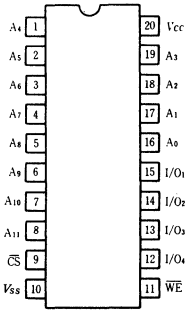
■FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35ns (max.)
- Low Power Standby: 100μW typ, 5μW typ (L-version)
  Active: 250mW typ.
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

■ORDERING INFORMATION

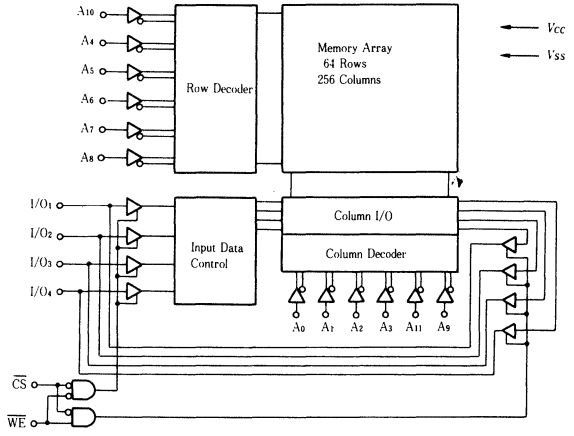
Type No.	Access Time	Package
HM6268P-25 HM6268P-35	25ns 35ns	300mil 20pin Plastic DIP
HM6268LP-25 HM6268LP-35	25ns 35ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width≧10ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED OPERATING CONDITIONS (Ta=0 to +70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width≦10ns.

■DC AND OPERATING CHARACTERISTICS (Vcc=5V±10%, Vss=0V, Ta=0 to +70℃)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}= V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$= V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$= V_{IL}, $I_{I/O}$=0mA	–	50	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$= V_{IH}	–	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$≧ V_{CC}−0.2V, V_{IN}≦0.2V or V_{IN}≧ V_{CC}−0.2V	–	0.02	2.0	mA
			–	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

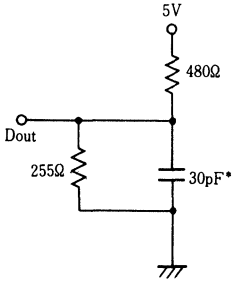
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	9	pF

Note: This parameter is sampled and not 100% tested.

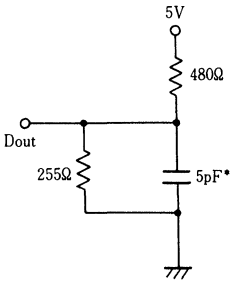
■AC CHARACTERISTICS (Vcc=5V±10%, Ta=0 to +70℃, unless otherwise noted.)

- AC Test Conditions
  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



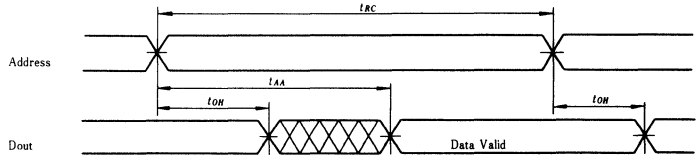
*Including scope and jig.

● READ CYCLE

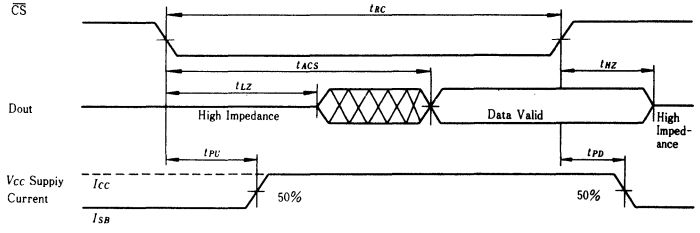
Parameter	Symbol	HM6268-25		HM6268-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	ns
Address Access Time	t_{AA}	–	25	–	35	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ} *1	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{HZ} *1	0	15	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	25	–	25	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1 (1),(2)



● Timing Waveform of Read Cycle No. 2 (1),(3)



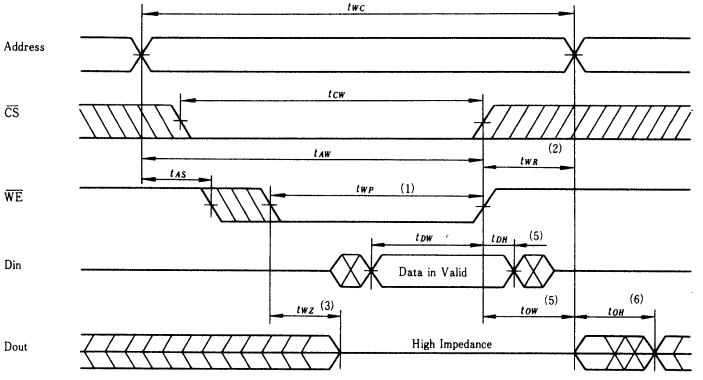
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

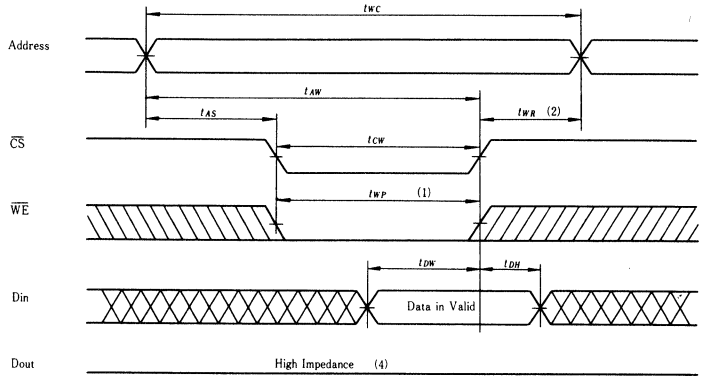
Parameter	Symbol	HM6268-25		HM6268-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	12	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WZ} *1	0	8	0	10	ns
Output Active from End of Write	t_{OW} *1	0	–	0	–	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

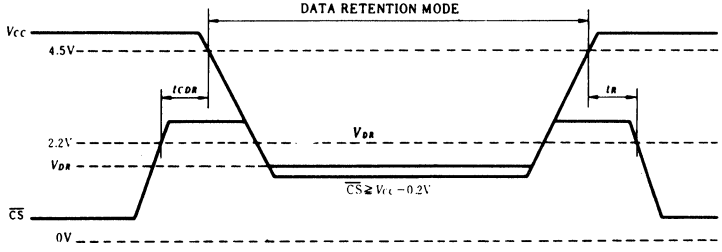
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristice is guaranteed only for L-version.

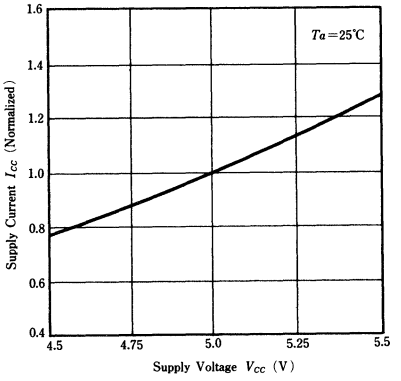
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time.
*2. V_{CC} = 3.0V
*3. V_{CC} = 2.0V

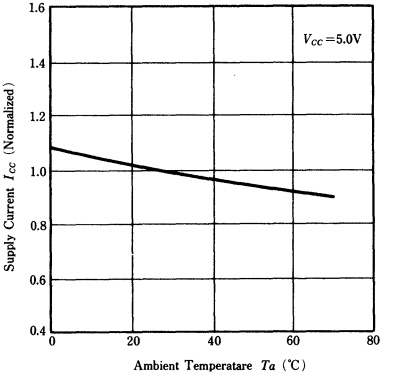
●LOW V_{CC} DATA RETENTION WAVEFORM



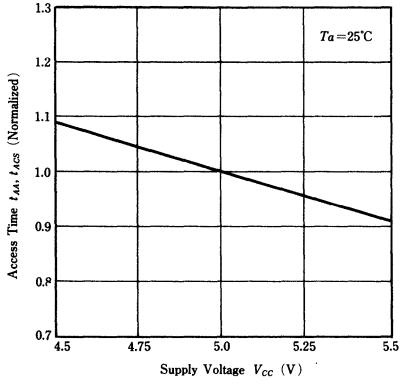
SUPPLY CURRENT VS. SUPPLY VOLTAGE



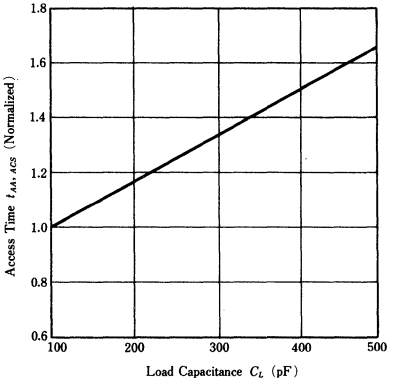
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



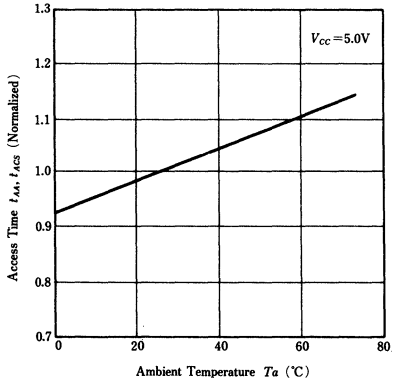
ACCESS TIME VS. SUPPLY VOLTAGE



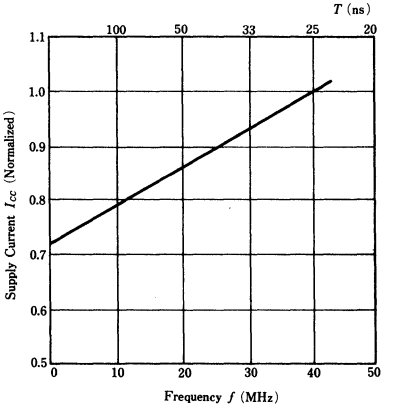
ACCESS TIME VS. LOAD CAPACITANCE



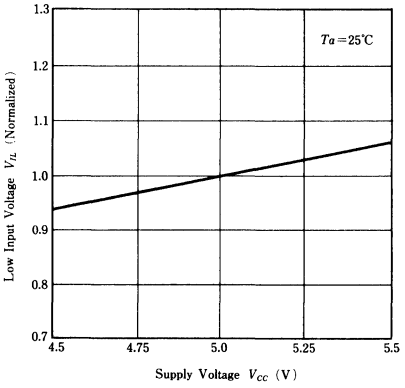
ACCESS TIME VS. AMBIENT TEMPERATURE



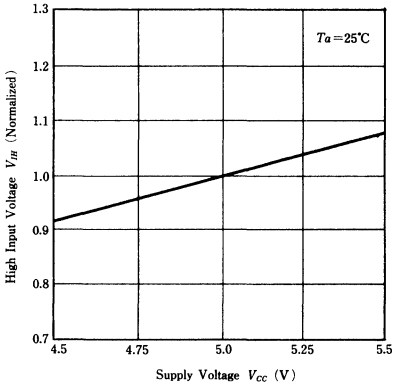
SUPPLY CURRENT VS. FREQUENCY



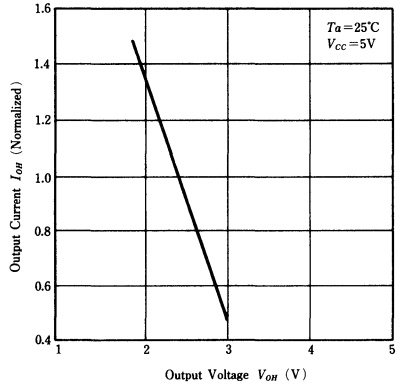
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



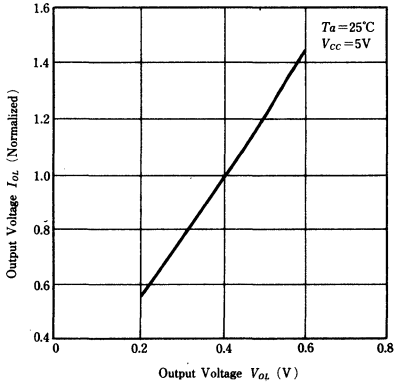
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



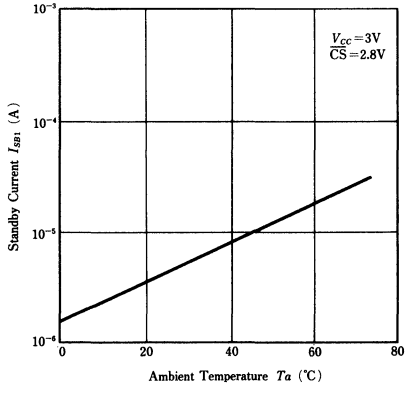
OUTPUT CURRENT VS. OUTPUT VOLTAGE



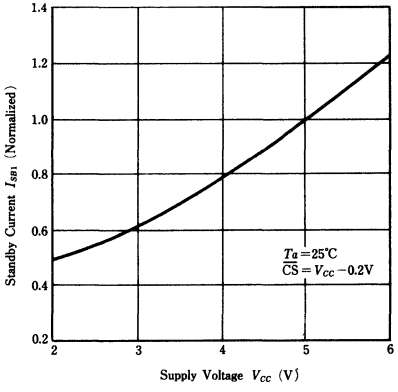
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



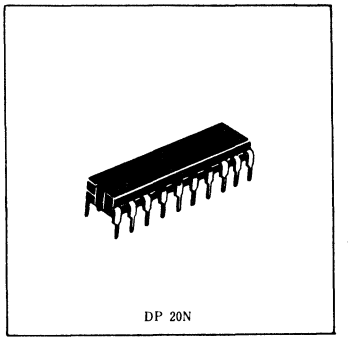
HM6167 Series — Maintenance Only

(Substitute HM6267P)

16384-word x 1-bit High Speed CMOS Static RAM

■FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time – 85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 100μW typ./5μW typ. (L-version)
  and Operating 150mW typ.
- Completely Static Memory . . . . . No Clock nor Refresh Required
- Fully TTL Compatible – All Inputs and Output
- Separate Data Input and Output . . . . . Three State Output
- Pin-Out Compatible with Intel 2167 Series
- Capability of Battery Back Up Operation (L-version)

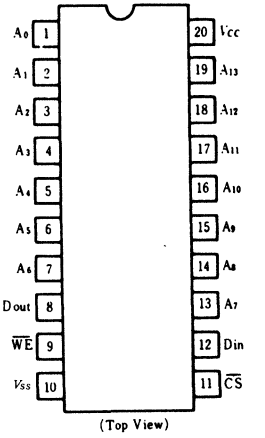


DP 20N

■ORDERING INFORMATION

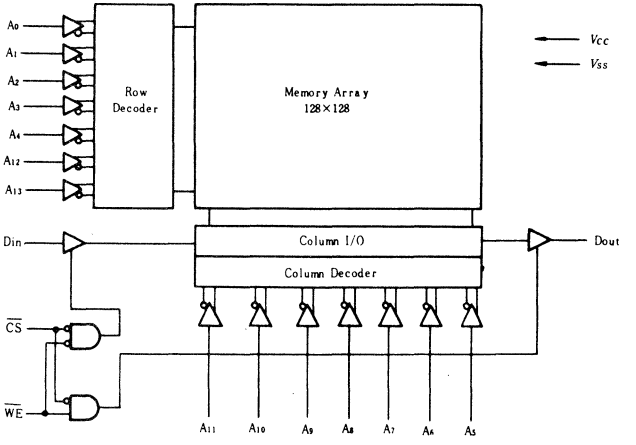
Type No.	Access Time	Package
HM6167P-6 HM6167P-8	85ns 100ns	300mil 20pin Plastic DIP
HM6167LP-6 HM6167LP-8	85ns 100ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature under bias	$T_{stg(bias)}$	−10 to +85	°C

Note) *1. −3.5V for pulse width≤20ns.

■RECOMMENDED DC OPERATING CONDITIONS

(0℃ ≦ Ta ≦ 70℃)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−0.3*1	—	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

■DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0℃ to +70℃)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = 0V ~ V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V ~ V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	5	20	mA
	I_{SB1}	$\overline{CS}$ = V_{CC} − 0.2V	—	0.02	2	mA
		V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} − 0.2V	—	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, Ta = 25℃ and specified loading.
*2. This characteristics is guaranteed only for L-version.

■CAPACITANCE (Ta = 25℃, f = 1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	6	pF	V_{OUT} = 0V

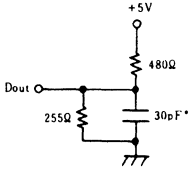
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 to +70℃, unless otherwise noted)

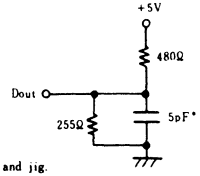
●AC TEST CONDITIONS

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

●READ CYCLE

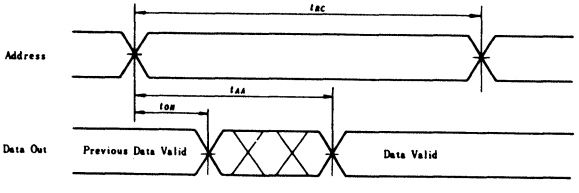
Item	Symbol	HM6167-6		HM6167-8		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	85	–	100	–	ns
Address Access Time	t_{AA}	–	85	–	100	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	40	–	45	ns

●WRITE CYCLE

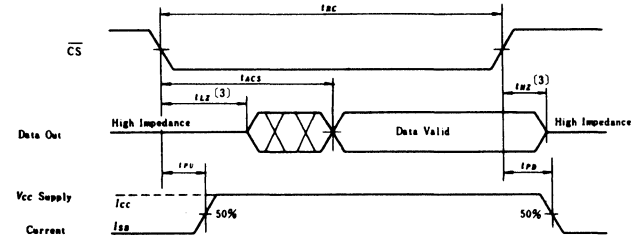
Item	Symbol	HM6167-6		HM6167-8		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	85	–	100	–	ns	2
Chip Selection to End of Write	t_{CW}	65	–	80	–	ns	
Address Valid to End of Write	t_{AW}	65	–	80	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	45	–	55	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	35	–	40	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Notes) 1. If $\overline{CS}$ goes high simultaneouly with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO.1 [1)]

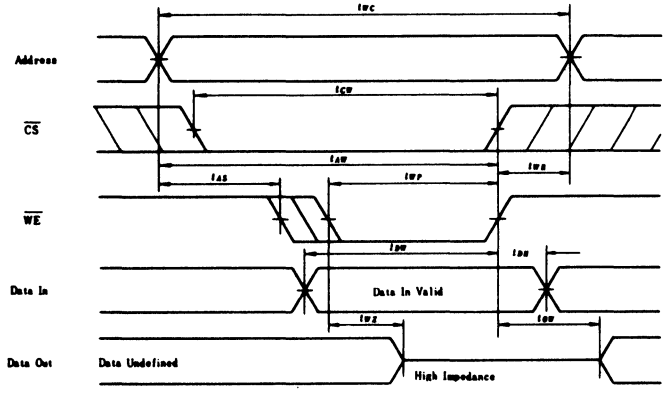


● TIMING WAVEFORM OF READ CYCLE NO. 2 [1), 3)]

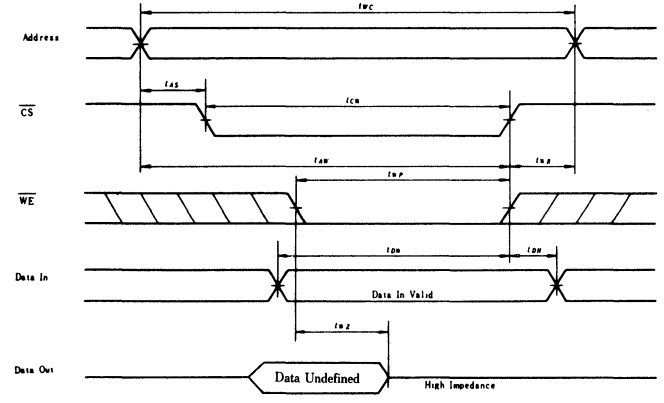


NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{CS}$ Controlled)



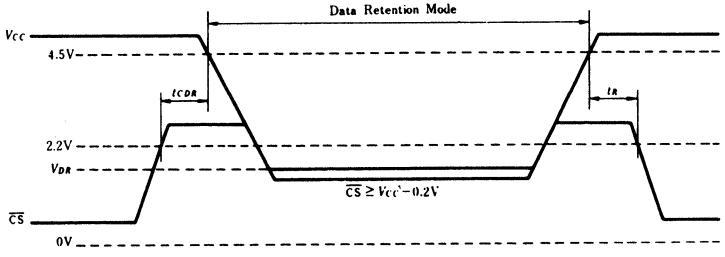
■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

This characteristics is guaranteed only for L-version.

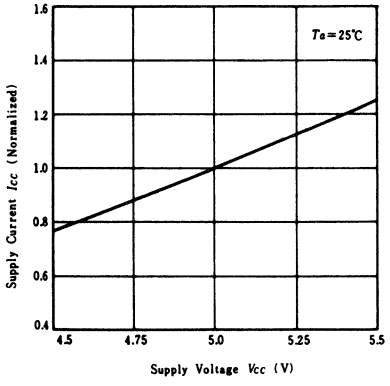
Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}		2.0	—	—	V
Data Retention Current	I_{CCDR}	$\overline{CS} \geq V_{CC}-0.2V$	—	—	20*2	μA
		$V_{in} \geq V_{CC}-0.2V$ or	—	—	30*3	
Chip Deselect to Data Retention Time	t_{CDR}	$0V \leq V_{in} \leq 0.2V$	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*1	—	—	ns

Notes) *1. t_{RC}=Read Cycle Time *2. V_{CC}=2.0V
*3. V_{CC}=3.0V

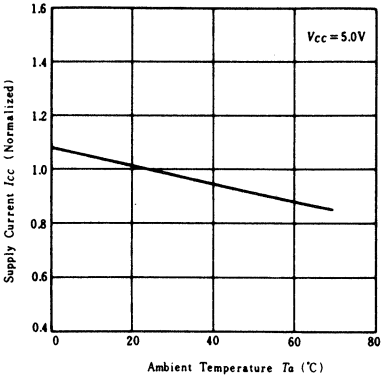
● LOW V_{CC} DATA RETENTION WAVEFORM



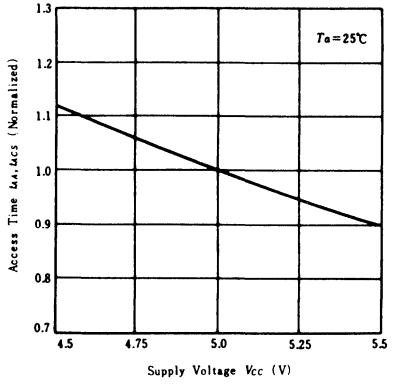
SUPPLY CURRENT vs. SUPPLY VOLTAGE



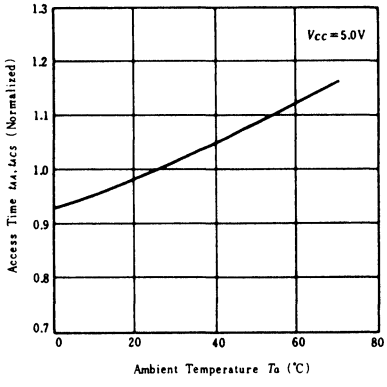
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



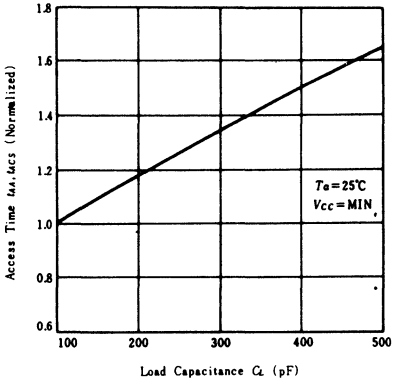
ACCESS TIME vs. SUPPLY VOLTAGE



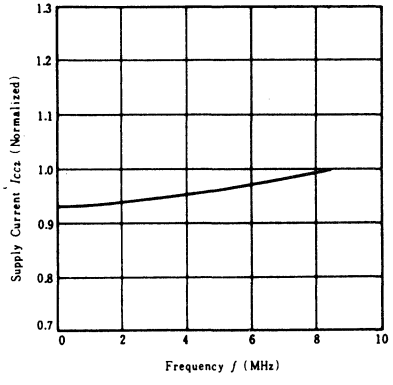
ACCESS TIME vs. AMBIENT TEMPERATURE



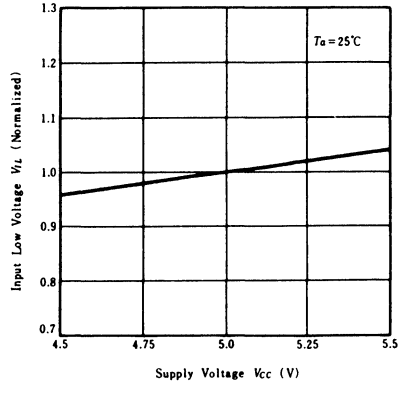
ACCESS TIME vs. LOAD CAPACITANCE



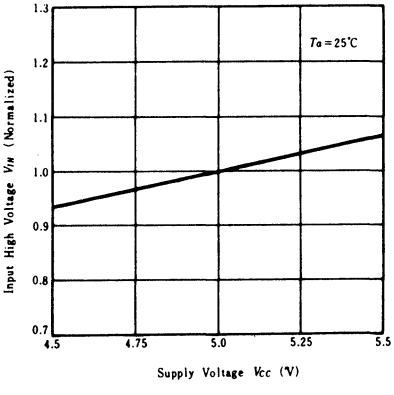
SUPPLY CURRENT vs. FREQUENCY



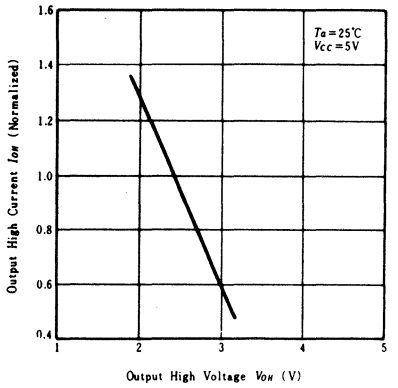
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



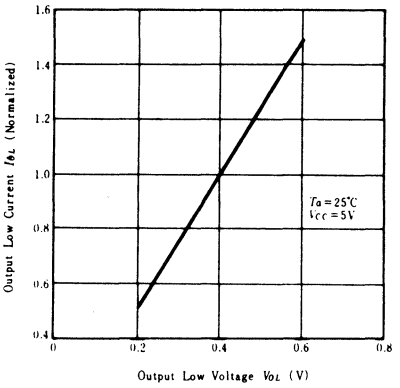
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



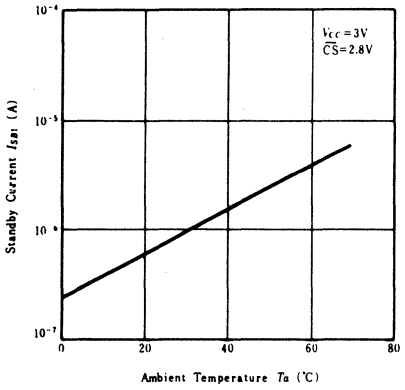
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



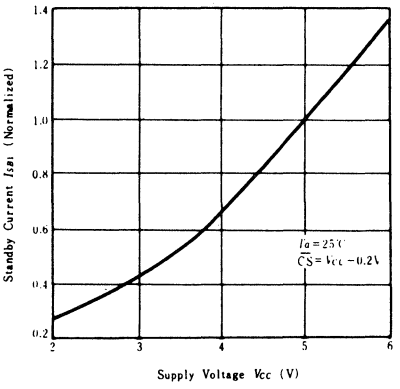
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



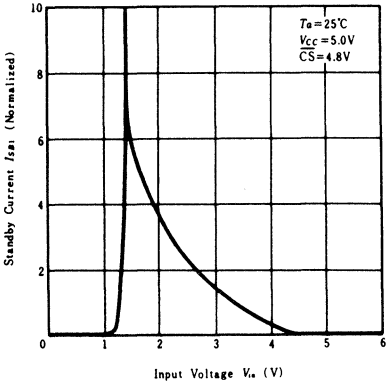
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



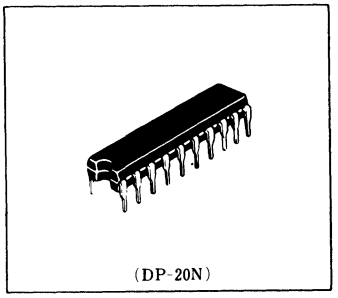
STANDBY CURRENT vs. INPUT VOLTAGE



HM6167H Series

Maintenance Only
(Substitute HM6267P)

16384-word x 1-bit High Speed CMOS Static RAM


(DP-20N)

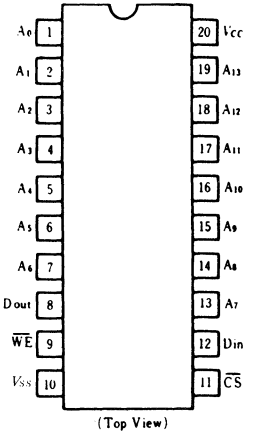
■ FEATURES

- Fast Access Time. . . . . 55/70ns (max)
- Low Power Standby and Low Power Operation
  Standby 100μW (typ)/5μW (typ) (L-version),
  Operating 200mW (typ)
- Single +5V Supply and High Density 20 Pin Package
- Completely Static Memory . . . .No Clock nor Refresh Required
- Fully TTL Compatible . . . . . .All Inputs and Output
- Separate Data Input and Output. . . . . .Three State Output
- Capability of Battery Back Up Operation (L-version)

■ ORDERING INFORMATION

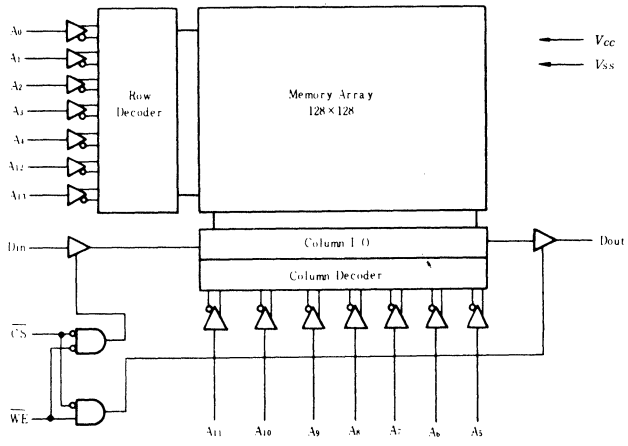
Type No.	Access Time	Package
HM6167HP-55	55ns	300 mil 20 pin plastic DIP
HM6167HP-70	70ns	
HM6167HLP-55	55ns	
HM6167HLP-70	70ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature under bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width ≦ 20ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 20ns

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0°C to +70°C)

Item	Symbol	Test Conditions	HM6167H-55			HM6167H-70			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	–	–	2	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	–	–	2	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, Output Open	–	40	80	–	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	10	20	–	5	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} – 0.2V	–	0.02	2	–	0.02	2	mA
		V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} – 0.2V	–	1*1	50*2	–	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (Ta = 25°C, f = 1.0MHz)

Item	Symbol	typ	max	Unit	Conditions
Input Capacitance	C_{IN}	–	5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	–	7	pF	V_{OUT} = 0V

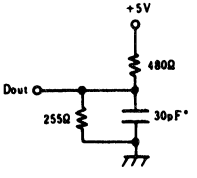
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 to +70°C, unless otherwise noted)

AC TEST CONDITIONS

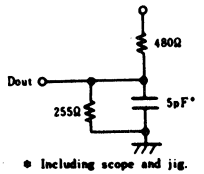
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



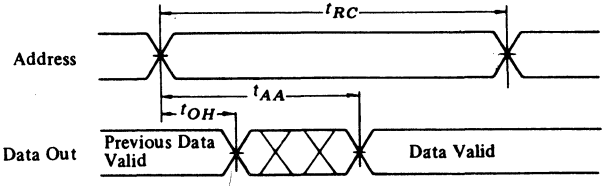
* Including scope and jig.

●READ CYCLE

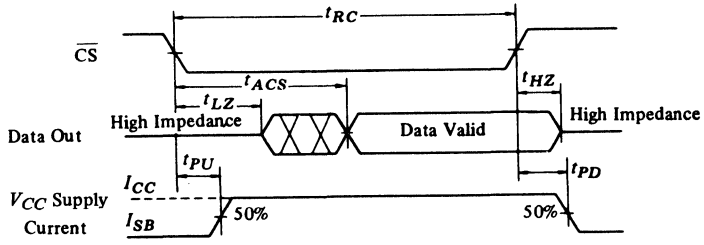
Item	Symbol	HM6167H-55		HM6167H-70		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	55	–	70	–	ns	(1)
Address Access Time	t_{AA}	–	55	–	70	ns	
Chip Select Access Time	t_{ACS}	–	55	–	70	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	(2) (3) (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	35	ns	(2) (3) (7)
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	30	–	35	ns	

Notes) 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO.1 4), 5)



●TIMING WAVEFORM OF READ CYCLE NO.2 4), 6)

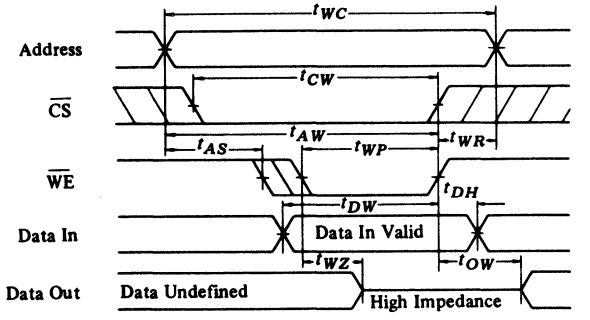


• WRITE CYCLE

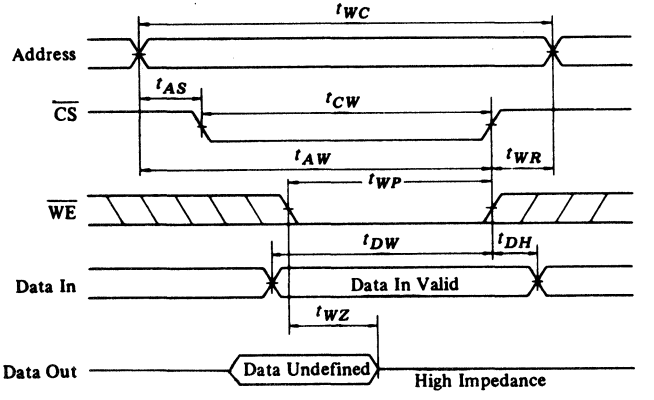
Item	Symbol	HM6167H-55		HM6167H-70		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	55	–	70	–	ns	(2)
Chip Selection to End of Write	t_{CW}	50	–	55	–	ns	
Address Valid to End of Write	t_{AW}	50	–	55	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	35	–	40	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	30	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	30	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	–	0	–	ns	(3) (4)

Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



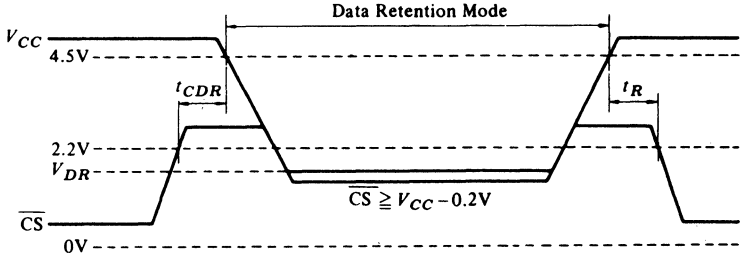
■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

This characteristics is guaranteed only for L-version.

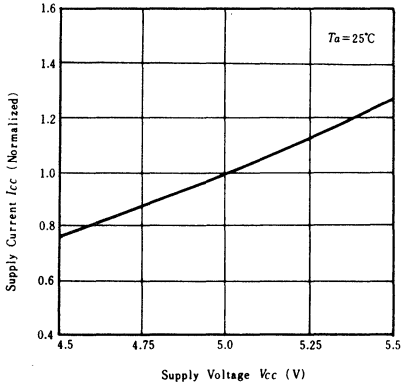
Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	20*2	μA
			—	—	30*3	
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*1	—	—	ns

Notes) *1. t_{RC}=Read Cycle Time *2. V_{CC}=2.0V *3. V_{CC}=3.0V

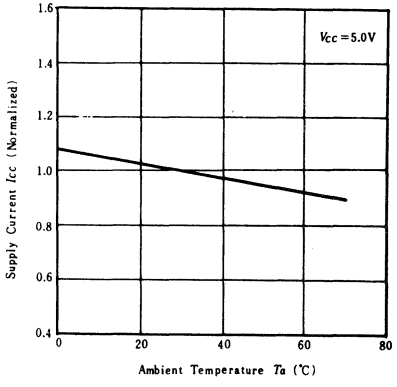
●LOW V_{CC} DATA RETENTION WAVEFORM



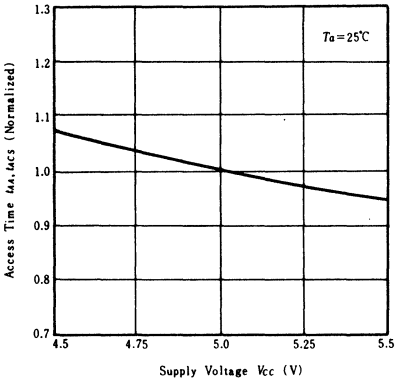
SUPPLY CURRENT vs. SUPPLY VOLTAGE



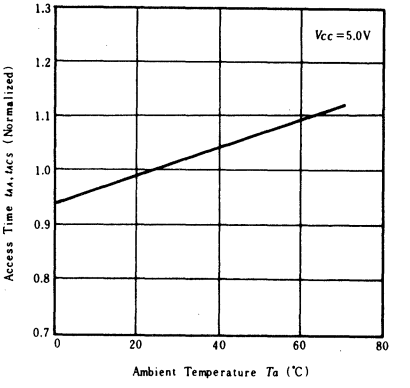
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



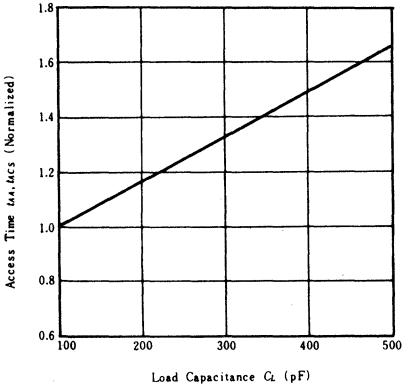
ACCESS TIME vs. SUPPLY VOLTAGE



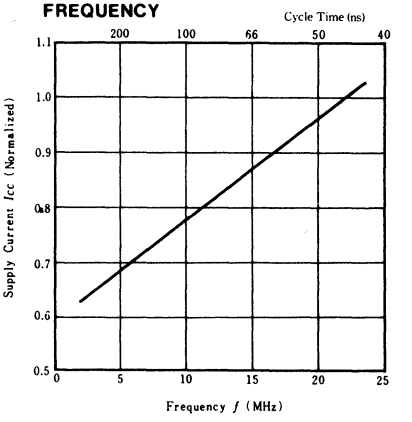
ACCESS TIME vs. AMBIENT TEMPERATURE



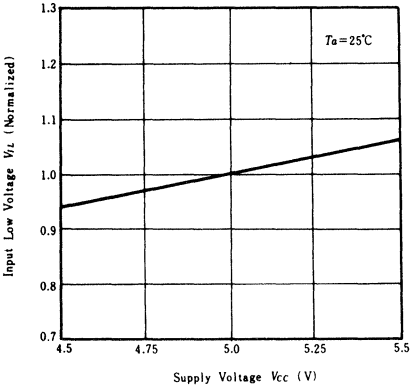
ACCESS TIME vs. LOAD CAPACITANCE



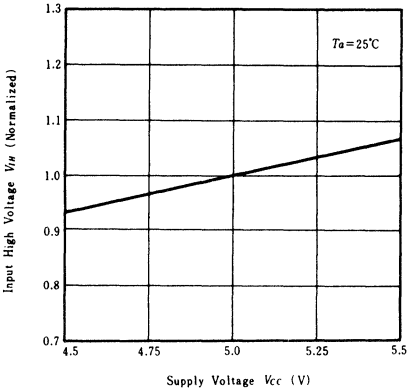
SUPPLY CURRENT vs. FREQUENCY



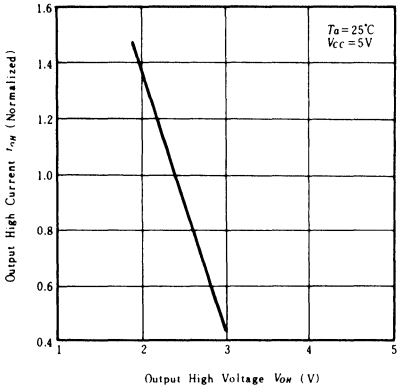
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



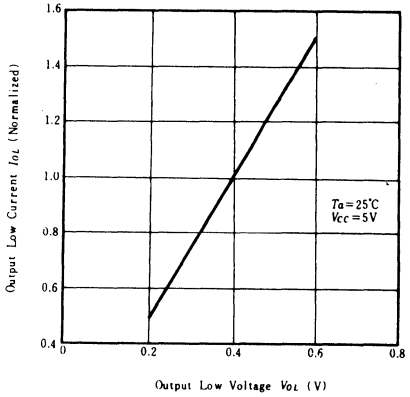
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



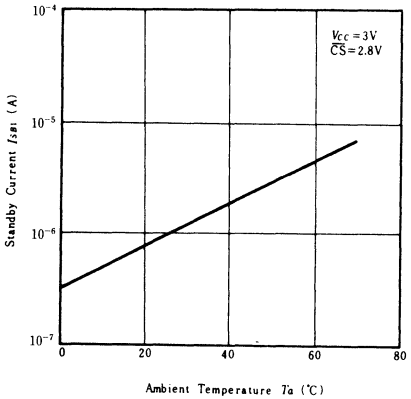
OUTPUT CURRENT vs. OUTPUT VOLTAGE



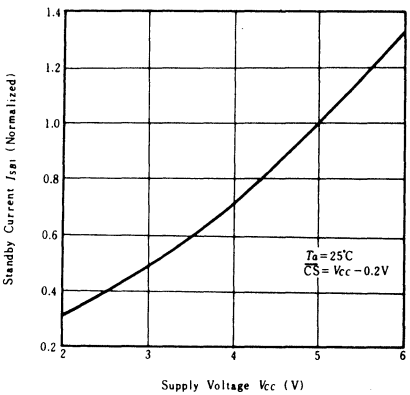
OUTPUT CURRENT vs. OUTPUT VOLTAGE



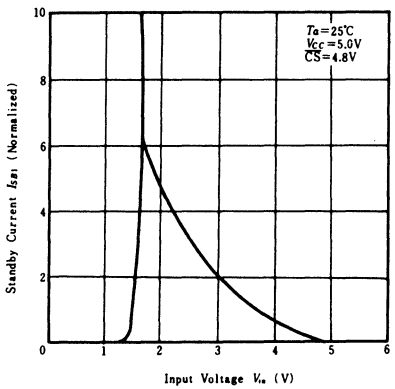
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



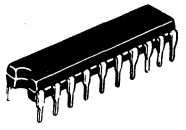
STANDBY CURRENT vs. INPUT VOLTAGE



HM6267 Series

16384-word x 1-bit High Speed CMOS Static RAM

HM6267P Series



(DP-20N)

■ FEATURES

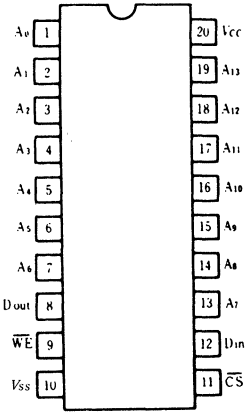
- High Speed: Fast Access Time 35/45 ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.)/5μW (typ.) (L-version),
  Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plastic DIP
HM6267P-45	45ns	
HM6267LP-35	35ns	
HM6267LP-45	45ns	

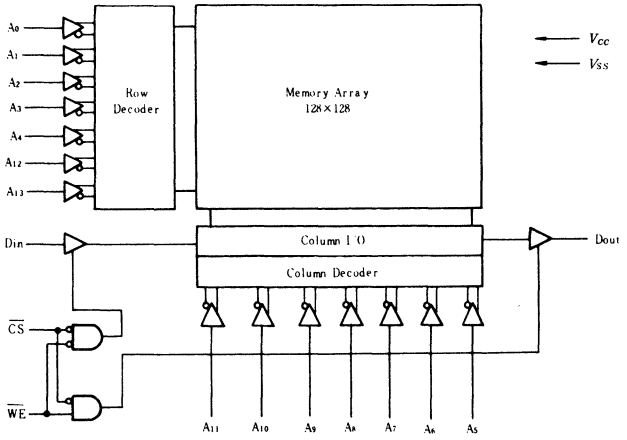
■ PIN ARRANGEMENT

- HM6267P Series



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Voltage on Any Pin*1		V_T	-0.5*2 to +7.0	V
Power Dissipation		P_T	1.0	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature	HM6267P Series	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias		T_{bias}	-10 to +85	°C

Notes: *1. With respect to V_{SS}.
*2. -3.5V for pulse width ≤ 20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6267-35			HM6267-45			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, Output Open	–	40	100	–	40	80	mA
Stand by Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	10	20	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}-0.2V,	–	0.02	2	–	0.02	2	mA
		V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} -0.2V	–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = -4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limts are at V_{CC} = 5V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	—	7	pF	V_{OUT}=0V

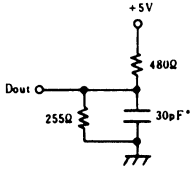
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

● AC TEST CONDITIONS

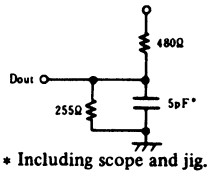
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

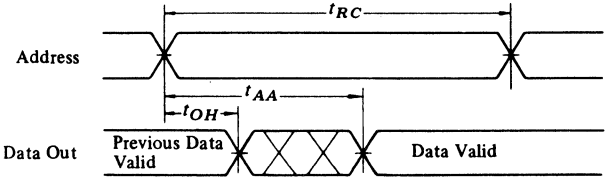


* Including scope and jig.

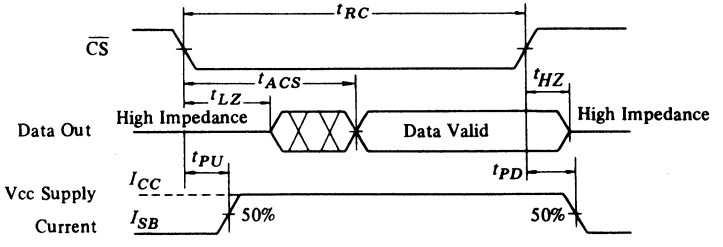
• Read Cycle

Item	Symbol	HM6267-35		HM6267-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	ns	1
Address Access Time	t_{AA}	—	35	—	45	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	30	ns	

• TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



• TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

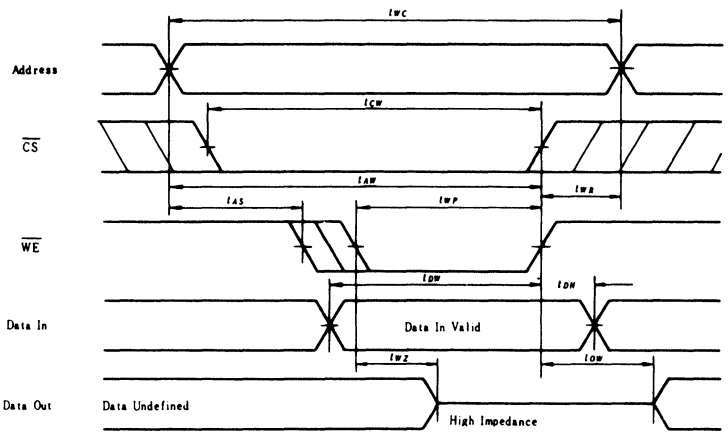


Notes) 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

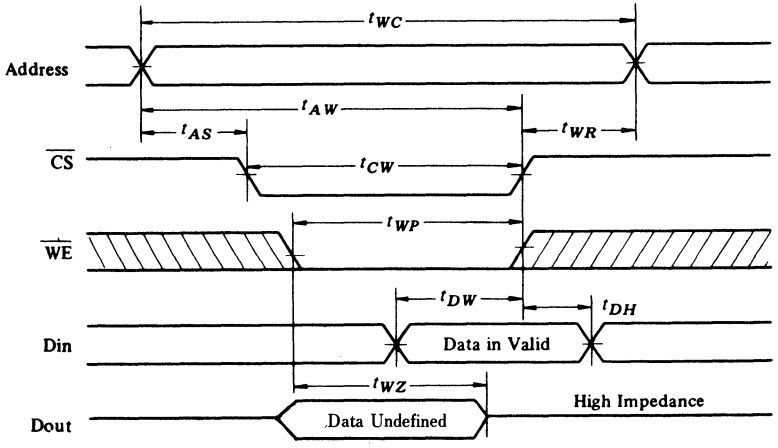
• Write Cycle

Item	Symbol	HM6267-35		HM6267-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	ns	2
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns	
Address Valid to End of Write	t_{AW}	30	—	40	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

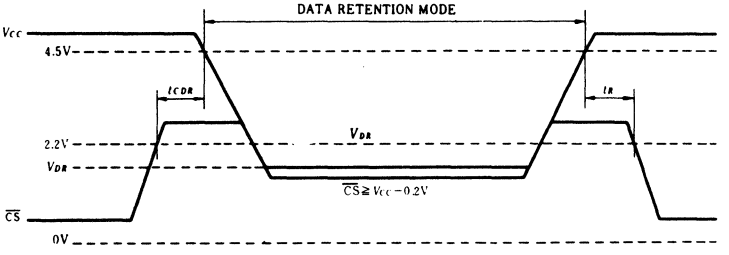
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics is guaranteed only for L-version.

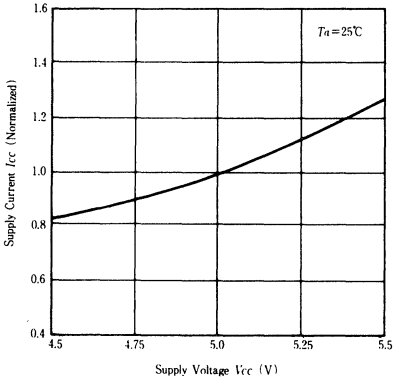
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30*2 20*3	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. V_{CC} = 3.0V *3. V_{CC} = 2.0V

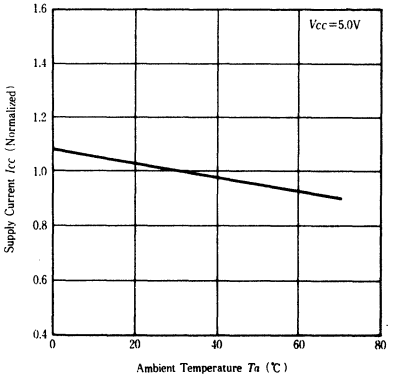
●LOW V_{CC} DATA RETENTION WAVEFORM



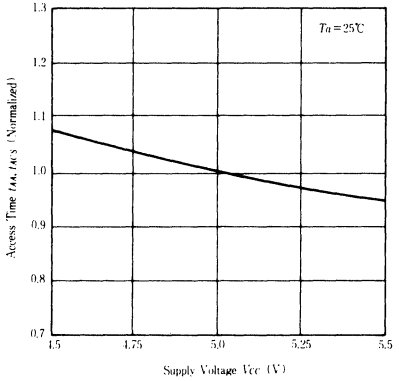
SUPPLY CURRENT VS. SUPPLY VOLTAGE



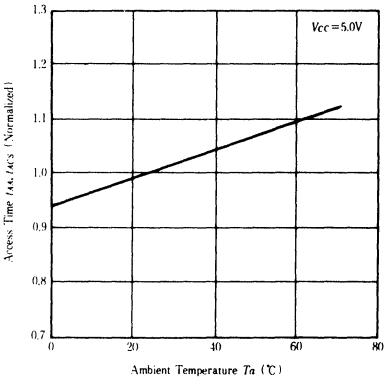
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



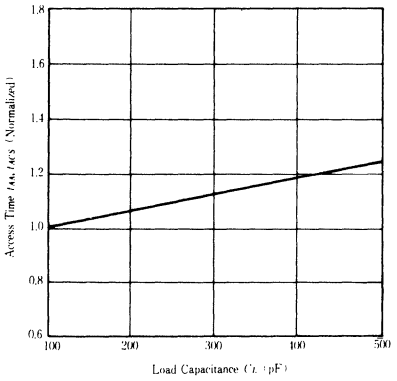
ACCESS TIME VS. SUPPLY VOLTAGE



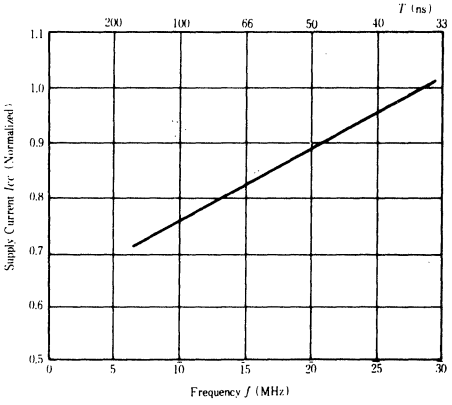
ACCESS TIME VS. AMBIENT TEMPERATURE



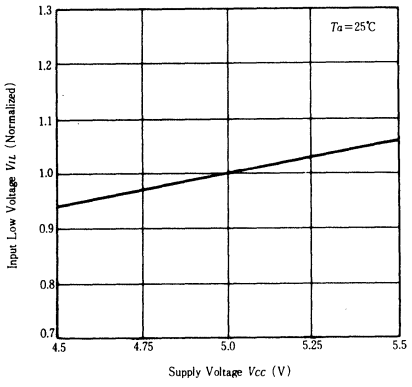
ACCESS TIME VS. LOAD CAPACITANCE



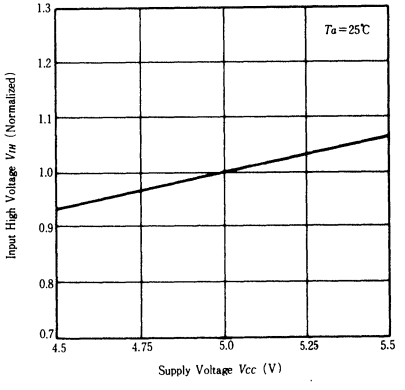
SUPPLY CURRENT VS. FREQUENCY



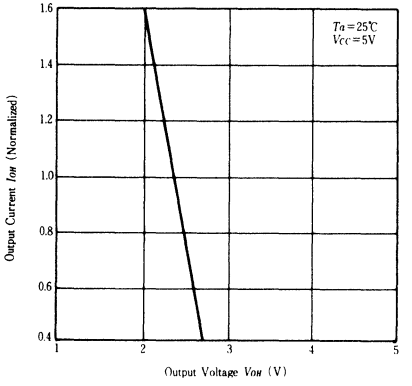
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



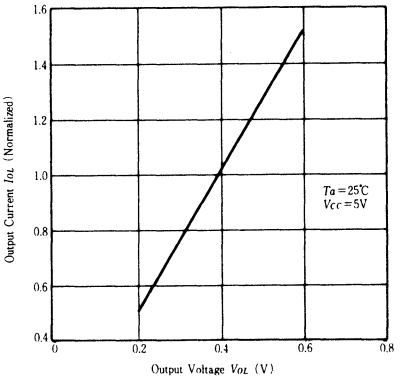
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



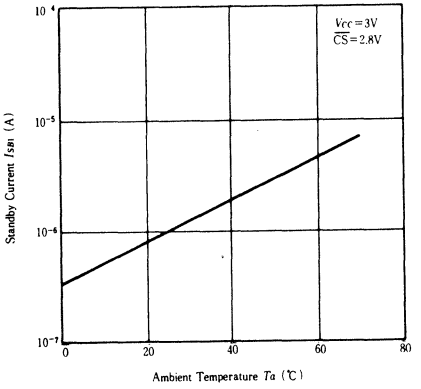
OUTPUT CURRENT VS. OUTPUT VOLTAGE



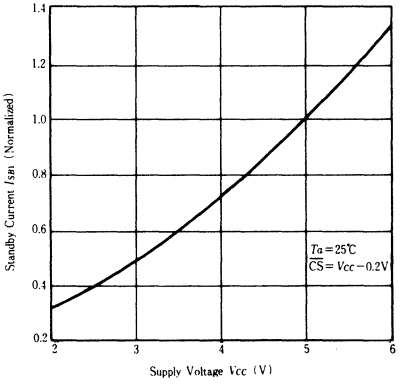
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



HM6264 Series

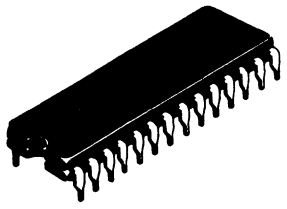
Maintenance Only
(Substitute HM6264A)

8192-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

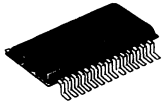
- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.1mW (typ.)
  10μW (typ.) L-/LL-version
  Low Power Operation — Operating: 200mW/MHz (typ.)
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764
- Capability of Battery Back Up Operation (L-/LL-version)

HM6264P Series



(DP-28)

HM6264FP Series



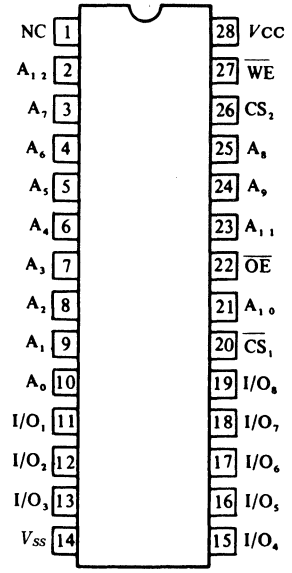
(FP-28D/DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6264P-10	100ns	600 mil 28 pin Plastic DIP
HM6264P-12	120ns	
HM6264P-15	150ns	
HM6264LP-10	100ns	
HM6264LP-12	120ns	
HM6264LP-15	150ns	
HM6264LP-10L	100ns	
HM6264LP-12L	120ns	
HM6264LP-15L	150ns	
HM6264FP-10	100ns	28 pin Plastic SOP (Note)
HM6264FP-12	120ns	
HM6264FP-15	150ns	
HM6264LFP-10	100ns	
HM6264LFP-12	120ns	
HM6264LFP-15	150ns	
HM6264LFP-10L	100ns	
HM6264LFP-12L	120ns	
HM6264LFP-15L	150ns	

Note) A character T is added to the end of type No. for SOP of 3.00 mm (max.) thickness.

■ PIN ARRANGEMENT



(Top View)

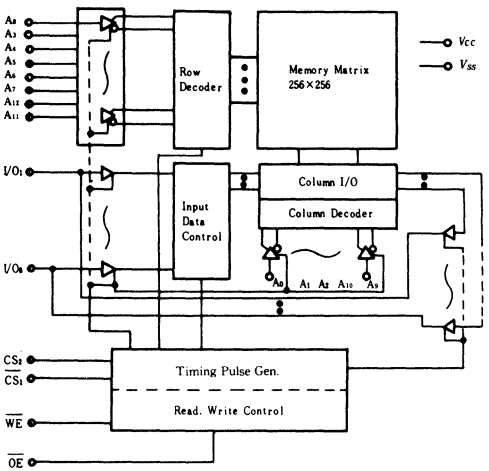
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *1	V_T	−0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

Notes) *1. With respect to V_{SS}
*2. −3.0V for pulse width ≦ 50ns

Note) This device is not available for new application.

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X : H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{in}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}	–	1	3	mA
	I_{SB1}*2	$\overline{CS1}\geqq V_{CC}-0.2V$, CS2$\geqq V_{CC}-0.2V$ or CS2≦0.2V	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
	I_{SB2}*2	CS2≦0.2V	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
	V_{OH}	I_{OH} = −1.0 mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. V_{IL} min=−0.3V
*3. This characteristics is guaranteed only for L-version.
*4. This charactoristics is guaranteed only for LL-version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

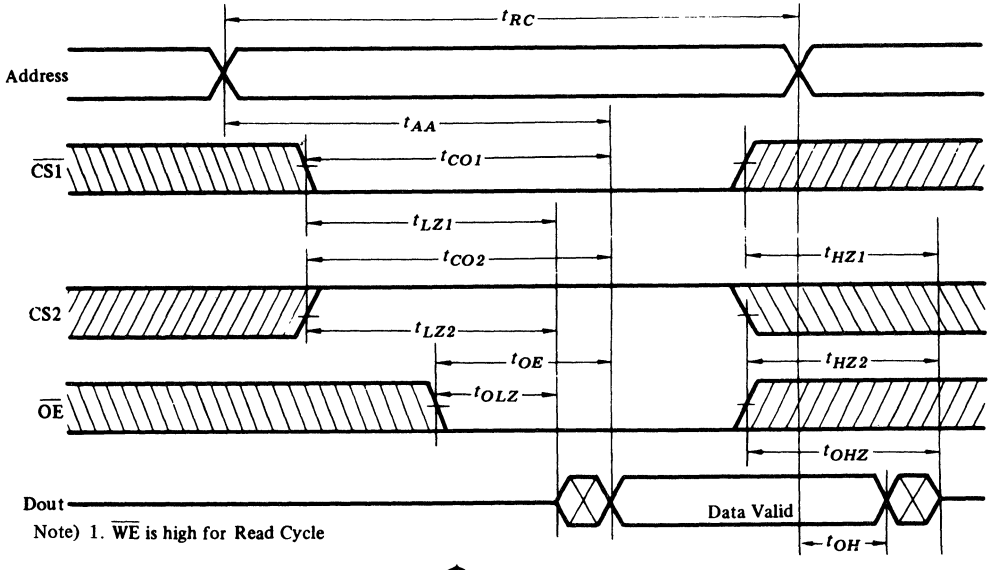
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264-10		HM6264-12		HM6264-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

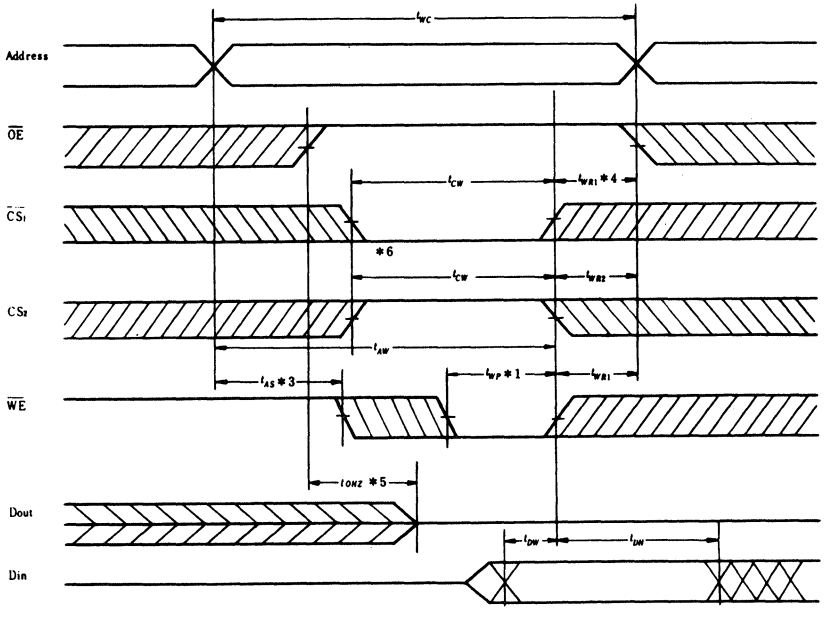


Note) 1. $\overline{WE}$ is high for Read Cycle

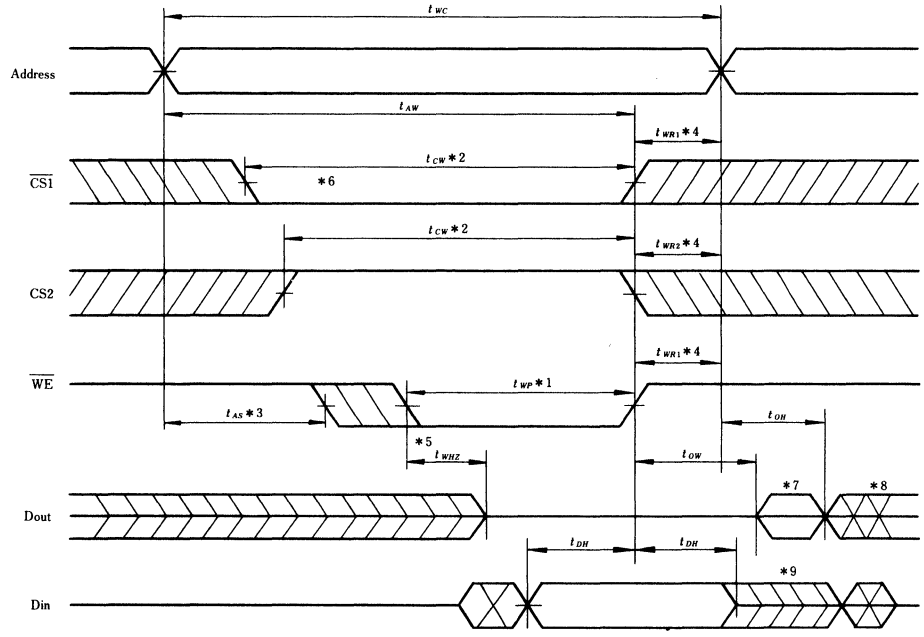
• WRITE CYCLE

Item		Symbol	HM6264-10		HM6264-12		HM6264-15		Unit
			min	max	min	max	min	max	
Write Cycle Time		t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	80	–	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width		t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	0	–	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	5	–	10	–	ns

• WRITE CYCLE (1) ($\overline{OE}$ clock)



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



Notes) 1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the begininng of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

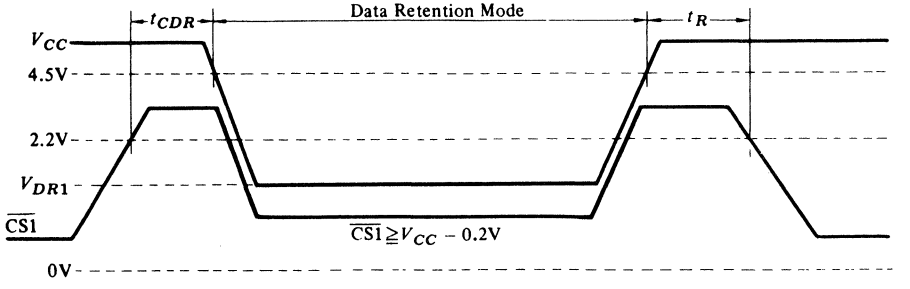
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L/LL-version.

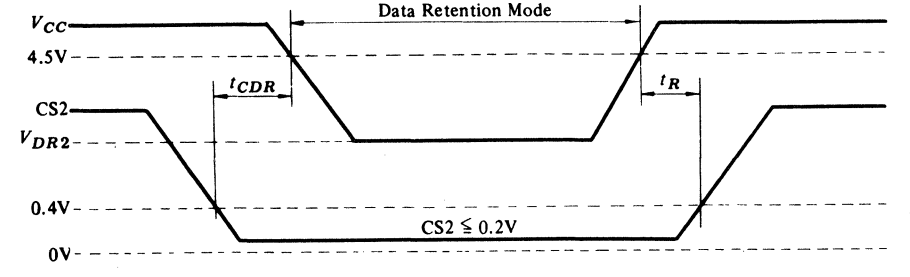
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC}$ -0.2V, CS2$\geq V_{CC}$-0.2V or CS2$\leq$0.2V	2.0	–	–	V
	V_{DR2}	CS2$\leq$0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS1} \geq V_{CC}$ -0.2V	–	1*1	50*1	μA
		CS2 $\geq V_{CC}$ -0.2V or CS2 $\leq$ 0.2V	–	1*2	25*2	
	I_{CCDR2}	V_{CC} = 3.0V, CS2 $\leq$ 0.2V	–	1*1	50*1	μA
			–	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*3	–	–	ns

Notes) *1. V_{IL} min = –0.3V, 20μA max at T_a=0 to 40°C. This characteristics is guaranteed only for L-version.
*2. V_{IL} min = –0.3V, 10μA max at T_a=0 to 40°C. This characteristics is guaranteed only for LL-version.
*3. t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

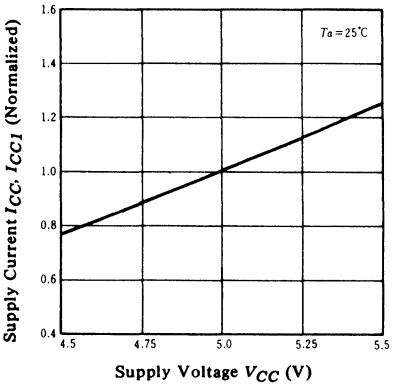


• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)

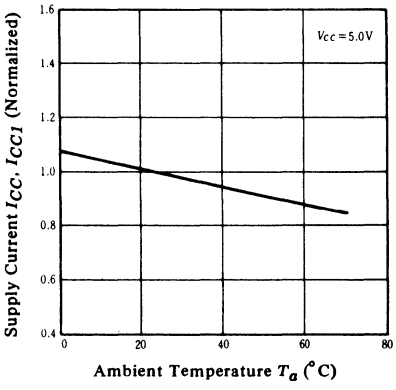


NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2 $\geq$ Vcc–0.2V or CS2 $\leq$ 0.2V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/$\overline{O}$) can be in the high impedance state.

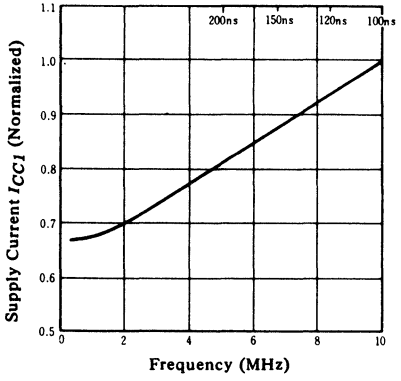
SUPPLY CURRENT vs. SUPPLY VOLTAGE



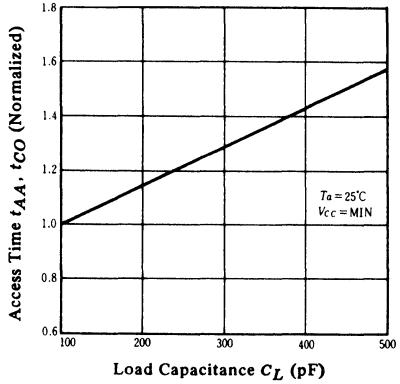
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



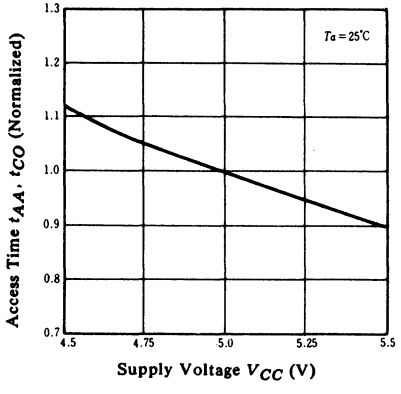
SUPPLY CURRENT vs. FREQUENCY



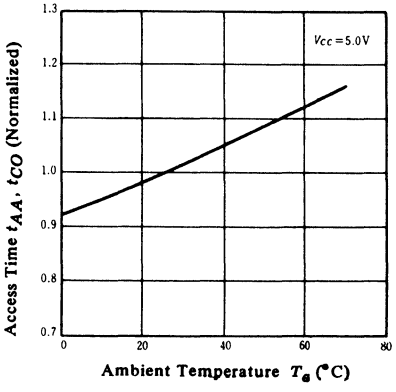
ACCESS TIME vs. LOAD CAPACITANCE



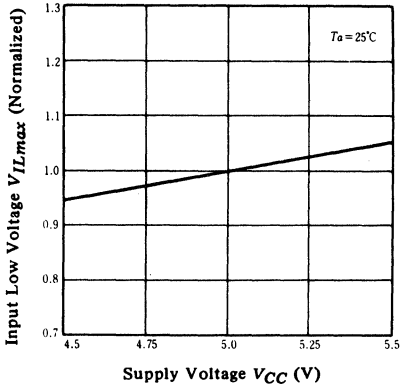
ACCESS TIME vs. SUPPLY VOLTAGE



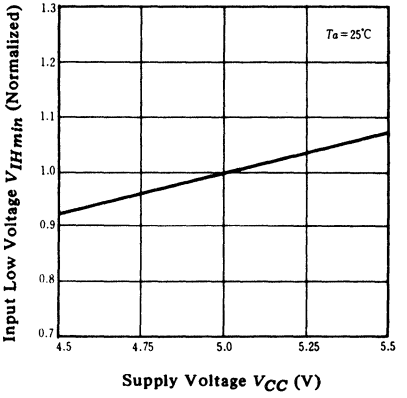
ACCESS TIME vs. AMBIENT TEMPERATURE



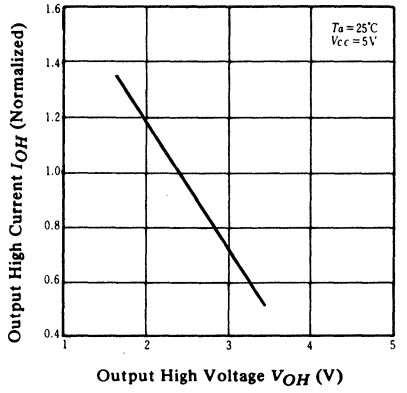
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



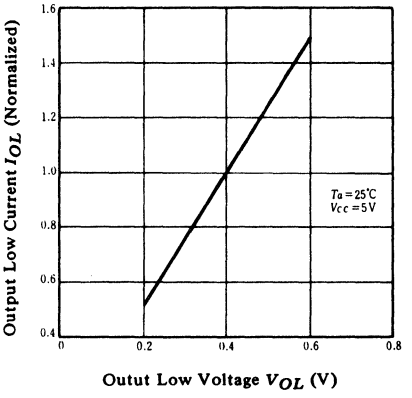
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



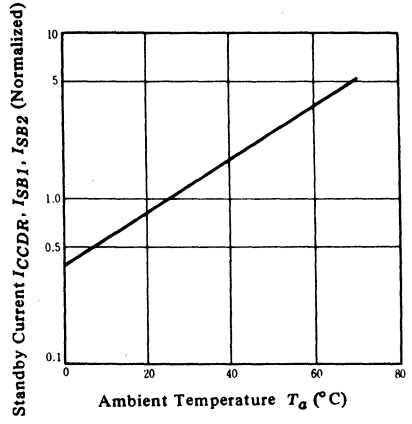
OUTPUT CURRENT vs. OUTPUT VOLTAGE



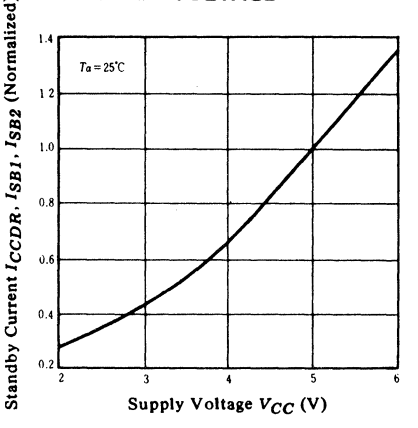
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



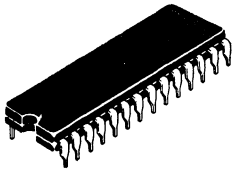
STANDBY CURRENT vs. SUPPLY VOLTAGE



HM6264A Series

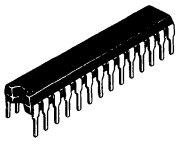
8192 × 8 Bit Low Power Static Hi-CMOS Ram

HA6264AP Series



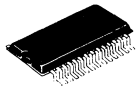
(DP-28)

HA6264ASP Series



(DP-28N)

HA6264AFP Series



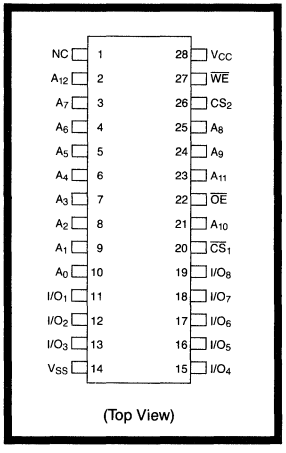
(FP-28D/DA)

■ FEATURES

- Various package types
  - 600 mil 28 pin plastic DIP
  - 300 mil 28 pin plastic DIP
  - SOP 28 pin
- Low power dissipation
  - Active mode 15 mW (typical) (f = 1 MHz)
  - Standby mode 100 μW (typical)
    - 10 μW (typical) (L version/LL version)
    - Two chip selection for battery back up.
  - Capability of battery back up operation (L version/LL version)
- High speed
  - Access time 100/120/150 ns (maximum)
  - (Equal access and cycle time)
- Single 5V supply
- Directly TTL compatible
  - All input and output
- Common data input and output, three state output
- Completely static RAM

  No clock or timing strobe required

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

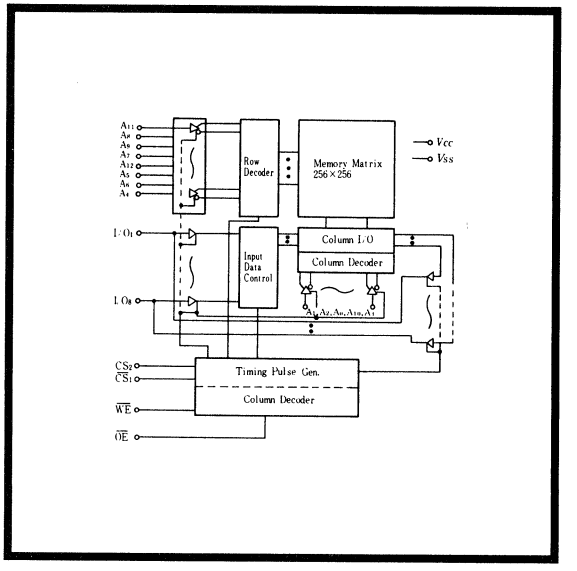
Pin Name	Function
A_0–A_{12}	Address
I/O_1–I/O_8	Input/Output
$\overline{CS}_1$	Chip Select
CS_2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ ORDERING INFORMATION

Type No.	Access	Package
HM6264AP-10	100 ns	600 mil 28 pin Plastic DIP (DP-28)
HM6264AP-12	120 ns	
HM6264AP-15	150 ns	
HM6264ALP-10	100 ns	
HM6264ALP-12	120 ns	
HM6264ALP-15	150 ns	
HM6264ALP-10L	100 ns	
HM6264ALP-12L	120 ns	
HM6264ALP-15L	150 ns	
HM6264ASP-10	100 ns	300 mil 28 pin Plastic DIP (DP-28N)
HM6264ASP-12	120 ns	
HM6264ASP-15	150 ns	
HM6264ALSP-10	100 ns	
HM6264ALSP-12	120 ns	
HM6264ALSP-15	150 ns	
HM6264ALSP-10L	100 ns	
HM6264ALSP-12L	120 ns	
HM6264ALSP-15L	150 ns	
HM6264AFP-10	100 ns	28 pin Plastic SOP (FD-28D/DA)
HM6264AFP-12	120 ns	
HM6264AFP-15	150 ns	
HM6264ALFP-10	100 ns	
HM6264ALFP-12	120 ns	
HM6264ALFP-15	150 ns	
HM6264ALFP-10L	100 ns	
HM6264ALFP-12L	120 ns	
HM6264ALFP-15L	150 ns	

SOP whose thickness is 3.00 mm (max.) has "T" in its typename's end.

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	Mode	I/O	Current	Note
*	H	*	*	Not Selected (Power Down)	High-Z	I_{SB}, I_{SB1}	
*	*	L	*		High-Z	I_{SB}, I_{SB1}	
H	L	H	H	Output Disabled	High-Z	I_{CC}	
H	L	H	L	Read	D_{OUT}	I_{CC}	
L	L	H	H	Write	D_{IN}	I_{CC}	Write Cycle[1]
L	L	H	L		D_{IN}	I_{CC}	Write Cycle[2]

*Don't Care (H or L)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage[1]	V_T	−0.5[2] to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

NOTES: 1. With respect to V_{SS}.
2. −3.0V for pulse width ≤ 50 ns.

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	D_{OUT}	I_{CC}	Read Cycle
L	L	H	H	Write	D_{IN}	I_{CC}	Write Cycle[1]
L	L	H	L		D_{IN}	I_{CC}	Write Cycle[2]

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-3.0[1]	—	0.8	V

NOTE: 1. -3.0V for pulse width ≤ 50 ns.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V + 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{IN} = V_{SS}$ to V_{CC}	—	—	± 2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$ $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}	—	—	± 2	μA
Operating Power Supply Current: DC	I_{CCDC}	$\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ Other input = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	—	7	15	mA
Operating Power Supply Current	I_{CC1}	Min. Cycle, Duty = 100% $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ Other input = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	—	30	45 55[3]	mA
	I_{CC2}	Cycle = 1 μs Duty = 100% $I_{I/O}$ = 0 mA, $CS_1 \leq 0.2V$, $CS_2 \geq V_{CC}$ -0.2V $V_{IH} \geq V_{CC}$ -0.2V, $V_{IL} \leq 0.2V$	—	3	5	mA
Standby Current (1)	I_{SB}	$\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$	—	1	3	mA
Standby Current (2): DC[2]	I_{SB1}	$\overline{CS}_1 \geq V_{CC}$ -0.2V, $CS_2 \geq V_{CC}$ -0.2V or $CS_2 \leq 0.2V$	— — —	0.02 2 2	2 100 50	mA μA[4] μA[5]
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4	—	—	V

NOTES: 1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C and specified loading.
2. V_{IL} min. = -0.3V
3. -12/-15 = 45 mA, -10 = 55 mA
4. Available for L version
5. Available for LL version

■ CAPACITANCE (f = 1 MHz, T_A = 25°C)

Item	Symbol	Typ	Max.	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	—	7	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, unless otherwise noted)

AC Test Conditions

Input pulse levels:	0.8V/2.4V
Input rise and fall times:	10 ns
Input timing reference levels:	1.5V
Output timing reference levels:	0.8V/2.0V (1.5V/1.5V)[1]
Output load:	1 TTL gate and CL = 100 pF (including scope and jig)

NOTE: 1. Available for 100 ns version.

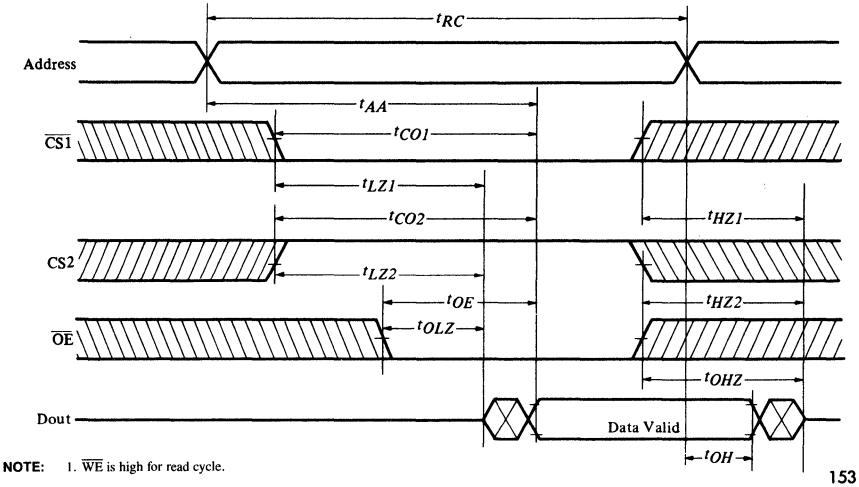
• Read Cycle

Parameter	Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	—	120	—	150	—	ns
Address Access Time	t_{AA}	—	100	—	120	—	150	ns
Chip Selection ($\overline{CS}_1$) To Output Valid	t_{CO1}	—	100	—	120	—	150	ns
Chip Selection ($\overline{CS}_2$) to Output Valid	t_{CO2}	—	100	—	120	—	150	ns
Output Enable ($\overline{OE}$) to Output Valid	t_{OE}	—	50	—	60	—	70	ns
Chip Selection ($\overline{CS}_1$) to Output in Low Z	t_{LZ1}	10	—	10	—	15	—	ns
Chip Selection (CS_2) to Output in Low Z	t_{LZ2}	10	—	10	—	15	—	ns
Output Enable ($\overline{OE}$) to Output in Low Z	t_{OLZ}	5	—	5	—	5	—	ns
Chip Deselection ($\overline{CS}_1$) to Output in High Z	t_{HZ1}	0	35	0	40	0	50	ns
Chip Deselection (CS_2) to Output in High Z	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable ($\overline{OE}$) to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Hold From Address Change	t_{OH}	10	—	10	—	10	—	ns

NOTE: 1. t_{HZ} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage level.

2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.

• Read Cycle



NOTE: 1. $\overline{WE}$ is high for read cycle.

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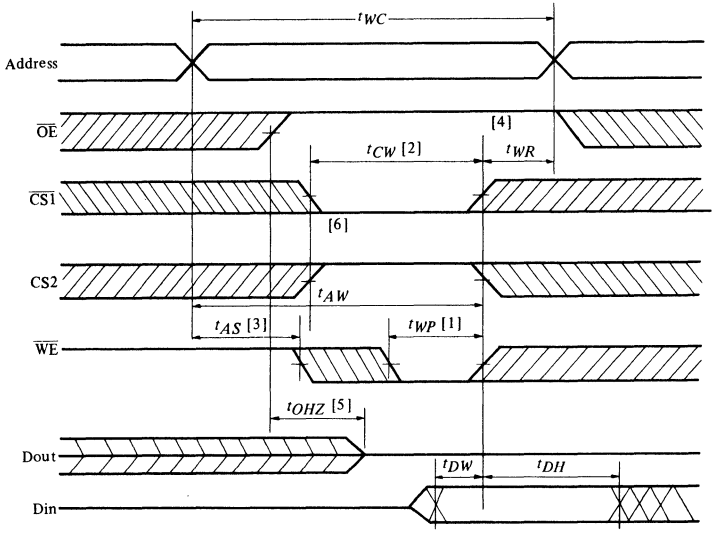
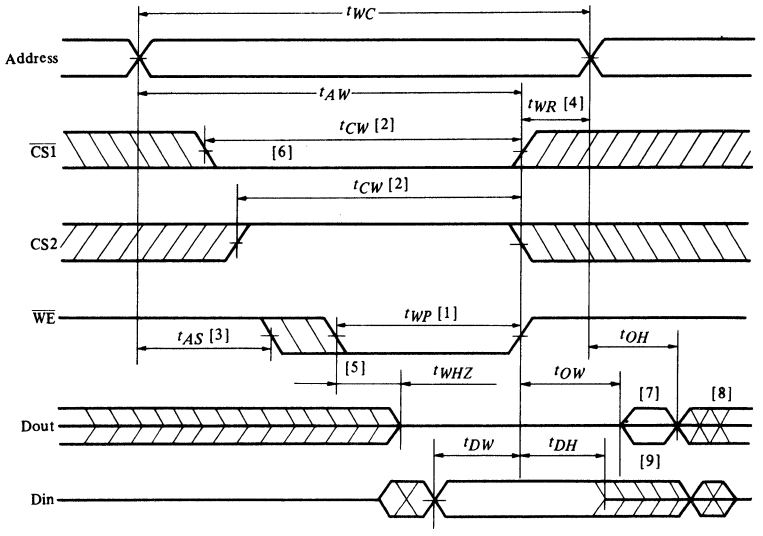
■ Write Cycle

Parameter	Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100	—	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	80	—	85	—	100	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	80	—	85	—	100	—	ns
Write Pulse Width	t_{WP}	60	—	70	—	90	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	—	40	—	50	—	ns
Data Hold From Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Active From End of Write	t_{OW}	5	—	5	—	5	—	ns

• Write Cycle No. 1 ($\overline{OE}$ Clock)



• Write Cycle No. 2 ($\overline{OE}$ Low Fix)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_1 going low, CS_2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS_1}$ going low of CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS_1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C)

This characteristics is guaranteed for L/LL-version.

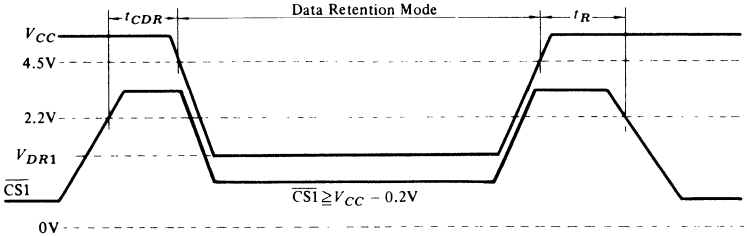
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS}_1 \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$
Data Retention Current	I_{CCDR}	—	1[1]	50[1]	μA	V_{CC} = 3.0V, $\overline{CS}_1 \geq V_{CC} - 0.2V$ $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$
		—	1[2]	25[1]		
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation Recovery Time	t_R	t_{RC}[3]	—	—	ns	

NOTES: 1. V_{IL} min. = -0.3V, 20 μA max. at T_A = 0 to 40°C, this characteristics is guaranteed ony for L-version.

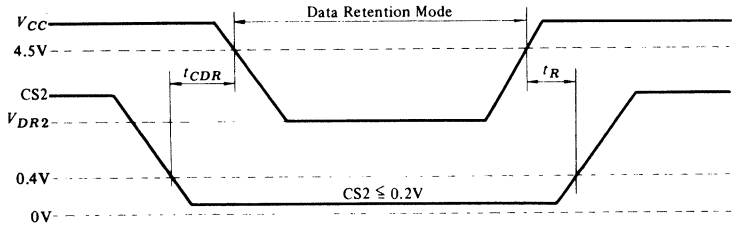
2. V_{IL} min. = -0.3V, 10 μA max. at T_A = 0 to 40°C, this characteristics is guaranteed only for LL-version.

3. t_{RC} = Read Cycle Time

• Low V_{CC} Data Retention Waveform No. 1 ($\overline{CS}_1$Controlled)

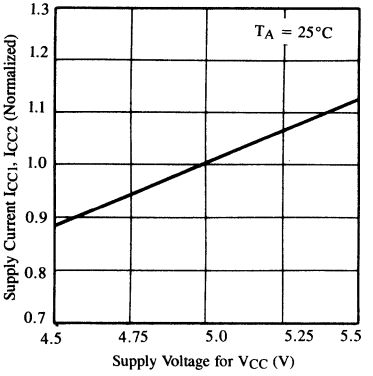


• Low V_{CC} Data Retention Waveform No. 2 (CS_2Controlled)

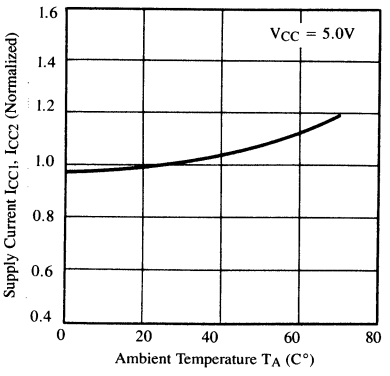


NOTE: In Data Retention Mode, CS_2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and D_{IN} buffer. If CS_2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If CS_1 controls the data retention mode, CS_2 must satifsy either $\overline{CS}_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$. The other input levels address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

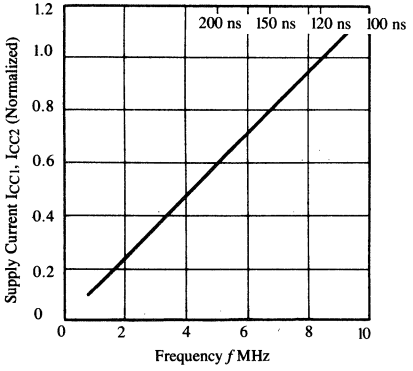
SUPPLY CURRENT VS. SUPPLY VOLTAGE



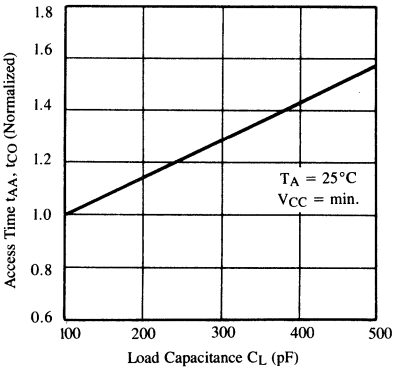
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



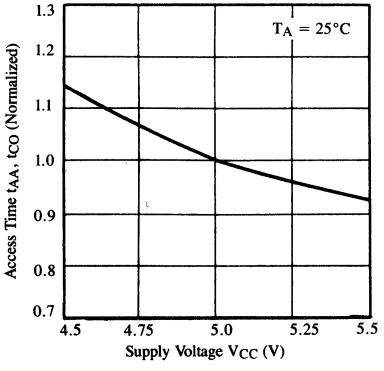
SUPPLY CURRENT VS. FREQUENCY



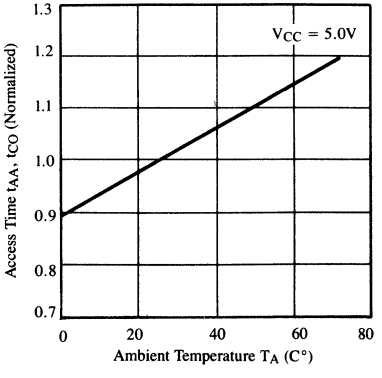
ACCESS TIME VS. LOAD CAPACITANCE



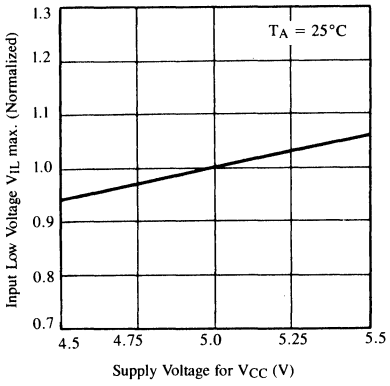
ACCESS TIME VS. SUPPLY VOLTAGE



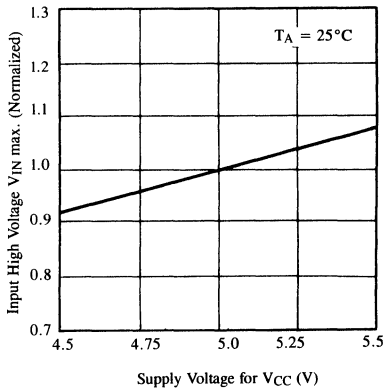
ACCESS TIME VS. AMBIENT TEMPERATURE



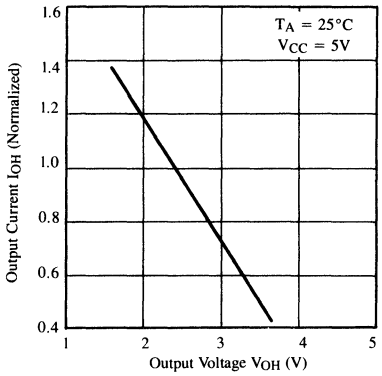
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



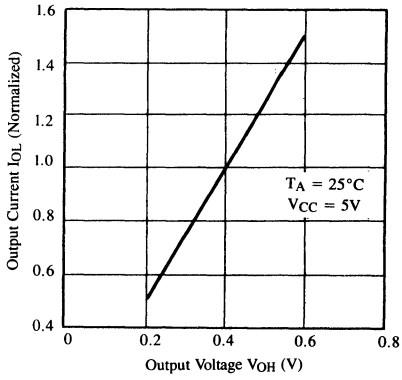
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



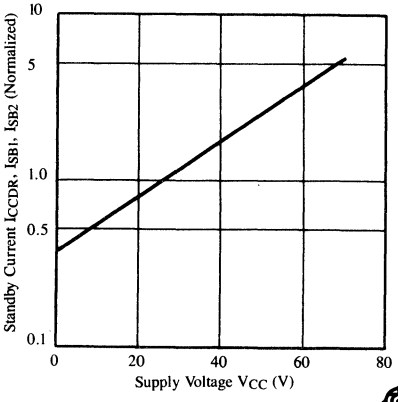
OUTPUT CURRENT VS. OUTPUT VOLTAGE



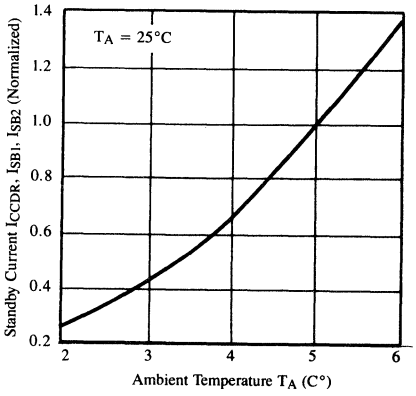
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



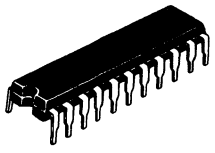
HM6288 Series

16384-word×4-bit High Speed CMOS Static RAM

■FEATURES

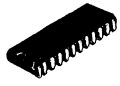
- Single 5V Supply and High Density 22 Pin Package.
- High Speed: Fast Access Time 25/35/45 ns (max.)
- Low Power dissipation
  - Active made 300mW (typ.)
  - Standby mode 100μW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

HM6288P Series



DP-22NB

HM6288JP Series



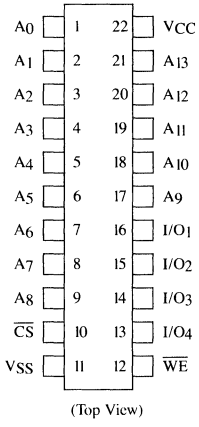
CP-24D

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM6288P-25 HM6288P-35 HM6288P-45	25ns 35ns 45ns	300 mil 22-pin Plastic DIP
HM6288LP-25 HM6288LP-35 HM6288LP-45	25ns 35ns 45ns	
HM6288JP-25 HM6288JP-35 HM6288JP-45	25ns 35ns 45ns	300 mil 24-pin Plastic SOJ

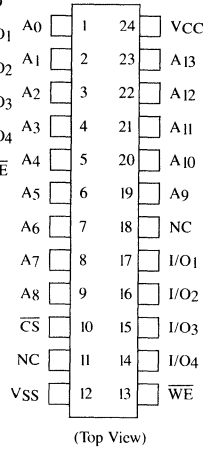
■ PIN ARRANGEMENT

HM6288P



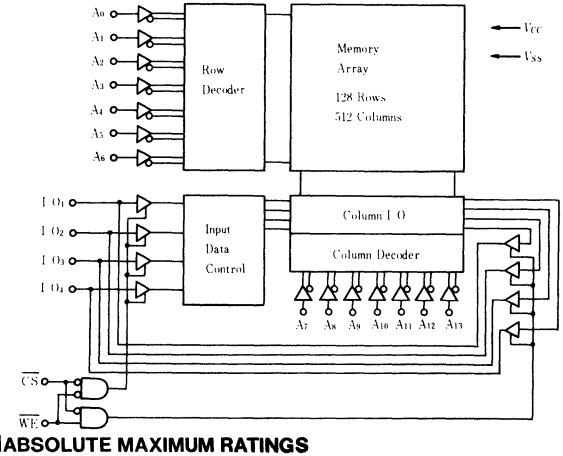
(Top View)

HM6288JP



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5[1] to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_T min. = −3.5V for pulse width≦10ns

■Pin Description

Pin Name	Function
A0 - A13	Address
I/O_1 -I/O_4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High Z	-
L	H	Read	I_{CC}	Dout	Read'Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note: *1. V_{IL} min.: 3.0V for pulse width≦10ns

■DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=MAX. V_{IN}=0V to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V to V_{CC}	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	60	120	mA
Standby V_{CC} Current	I_{SB}	$\overline{CS}$=V_{IH}	–	15	30	mA
Standby V_{CC} Current 1	I_{SB1}*2	$\overline{CS}$=V_{CC}−0.2V	–	0.02	2.0	mA
	I_{SB1}*3	V_{in}≦0.2V or V_{in}≧V_{CC}−0.2V	–	0.02	0.1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Notes: *1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
*2. P version
*3. LP version

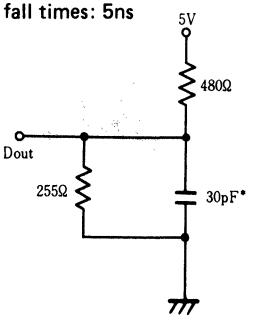
■CAPACITANCE (Ta=25°C, f=1.0MHz)

Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note: This parameter is sampled and not 100% tested

■AC CHARACTERISTICS

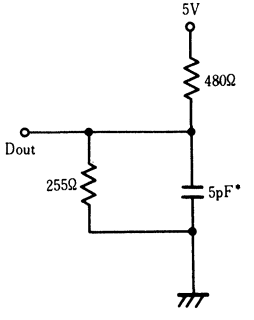
- **AC Test Conditions**
  Input pulse levels: 0V to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure



Output Load (A)

*Including scope & jig.

Output Load (A)



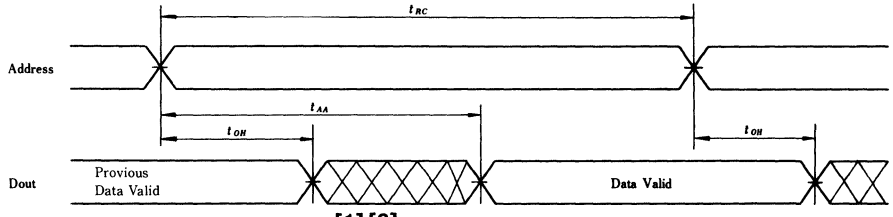
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ} & t_{OW})

■ READ CYCLE (T_a=0 to +70°C, V_{CC}=5V ± 10%, unless otherwise noted.)

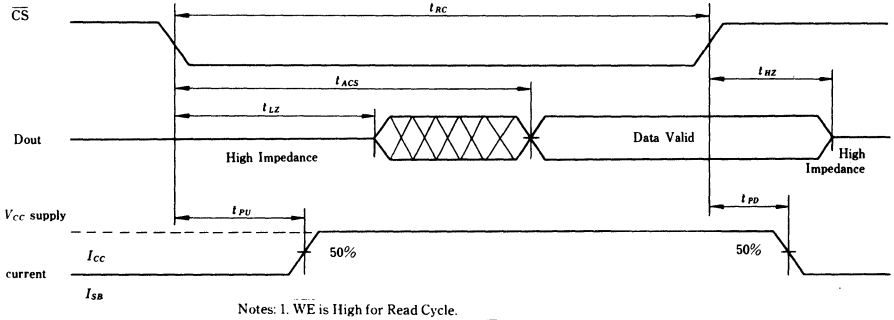
Parameter	Symbol	HM6288-25		HM6288-35		HM6288-45		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	45	–	ns
Address Access Time	t_{AA}	–	25	–	35	–	45	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	–	45	ns
Output Hold from Address Change	t_{OH}	3	–	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*	5	–	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	12	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Seselection to Power Down Time	t_{PD}	–	25	–	30	–	30	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No.1 [1] [2]



● Timing Waveform of Read Cycle No.2 [1] [3]



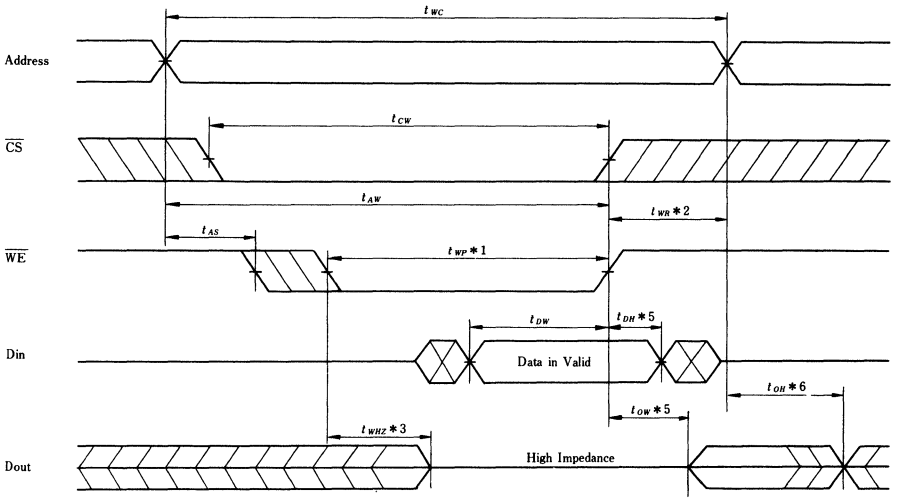
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

■ WRITE CYCLE

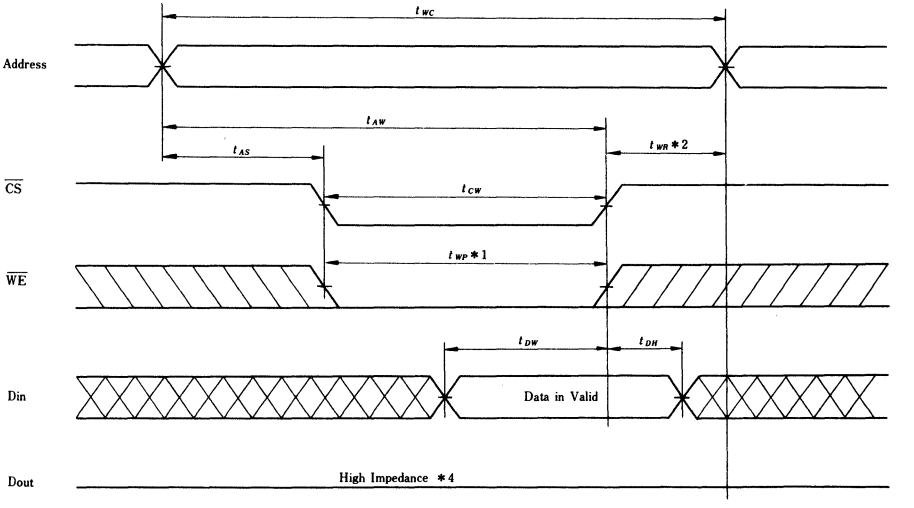
Parameter	Symbol	HM6288-25		HM6288-35		HM6288-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	45	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	40	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	40	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	35	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Date Valid to End of Write	t_{DW}	12	–	20	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WHZ}*	0	8	0	10	0	15	ns
Output Active from End of Write	t_{OW}*	5	–	5	–	5	–	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 ($\overline{WE}$ Controlled)



● Timing Waveform of Write Cycle No.2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

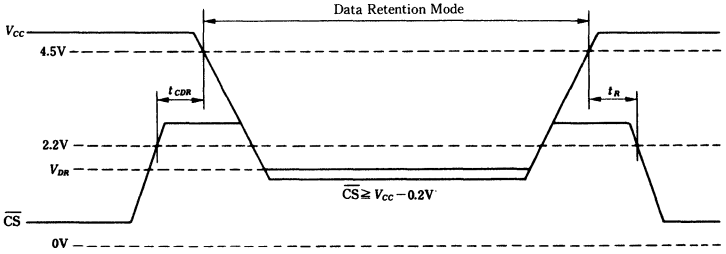
● Low *Vcc* Data Retention Characteristics ($Ta = 0$ to $+70°C$)

(This Characteristics is guaranteed only for L version.)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	
Data retention current	I_{CCDR}	–	–	50[2] 35[3]	μA	$\overline{CS} \geqq V_{CC} - 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	$V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Operation recovery time	t_R	t_{RC}[1]	–	–	ns	

NOTE : 1. t_{RC} = *Read cycle time*
2. $V_{CC} = 3.0V$
3. $V_{CC} = 2.0V$

Low *Vcc* Data Retention Waveform

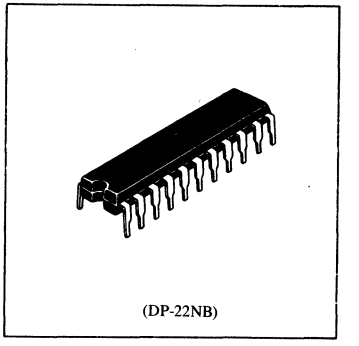


HM6788 Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

■FEATURES

- Super Fast Access Time: 25/35 ns (max.)
- Low power Operation
  Operating: 230mW (typ), Standby: 10mW (typ)
- +5V Single Supply
- Completely Static Memory —
  No Clock or Timing Strobe required
- Balanced Read and Write Cycle Time
- Fully TTL compatible Input and Output

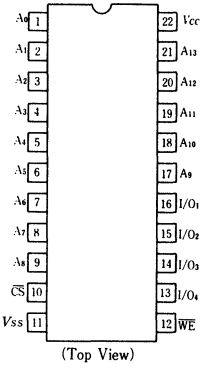


(DP-22NB)

■ ORDERING INFORMATION

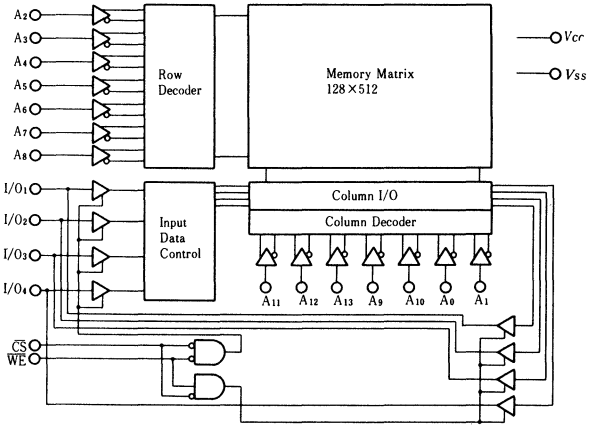
Type No.	Access Time	Package
HM6788P-25	25ns	300 mil 22 pin Plastic DIP
HM6788P-35	35ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2)

×: H or L

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 20ns pulse width.

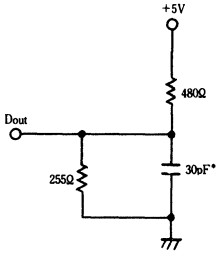
■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ± 10%, Ta=0°C to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{IN}= V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$= V_{IH}, V_I/o= V_{SS} to V_{CC}	–	–	2	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}$= V_{IL}, I_I/o=0mA	–	–	80	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$= V_{IH}, I_I/o=0mA	–	–	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.5	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	–	–	V

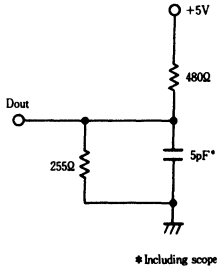
■AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

Input pulse levels: V_{SS} to 3.0V
Input rise and fall time: 4ns
Input and Output reference levels: 1.5V
Output Load: See Figure



Output Load A



*Including scope and jig.

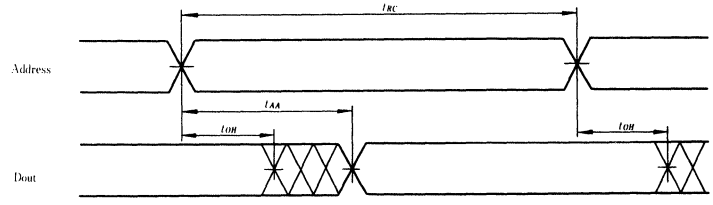
Output Load B
(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW})

● READ CYCLE

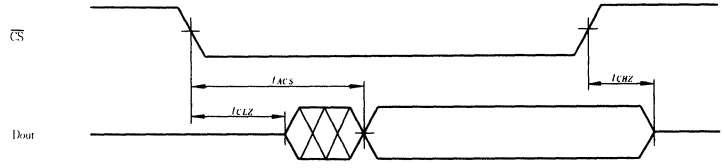
Item	Symbol	HM6788-25		HM6788-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	ns
Chip Selection to Output in Low Z	t_{CLZ}	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time*1	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time*1	t_{PD}	—	20	—	30	ns

Note) *1. This parameter is sampled and not 100% tested.

● Timing waveform of Read Cycle No. 1 *1,*2



● Timing waveform of Read Cycle No. 2*1,*3

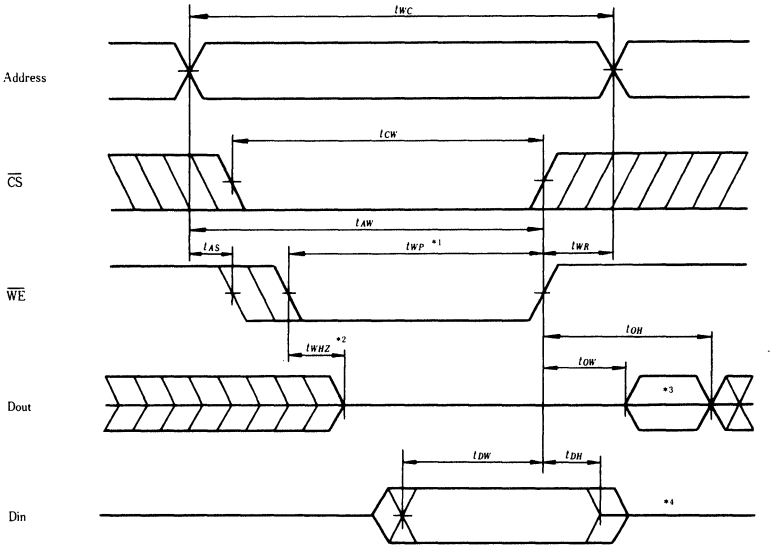


Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

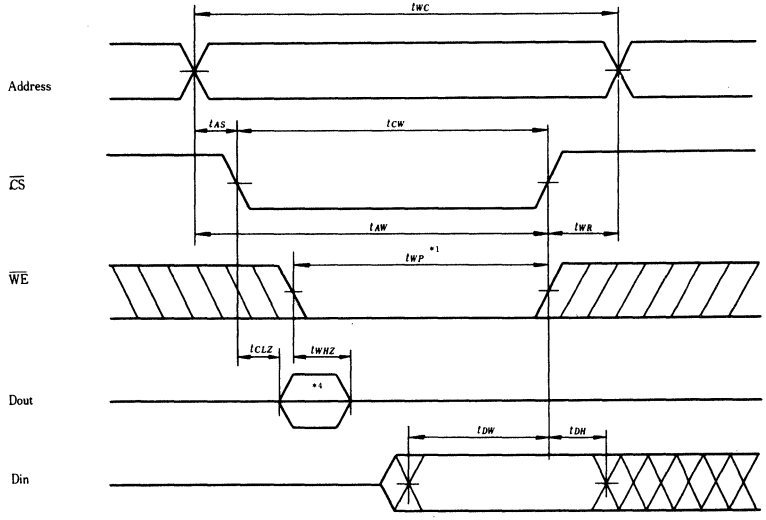
● WRITE CYCLE

Item	Symbol	HM6788-25		HM6788-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	20	—	25	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	20	—	25	—	ns
Write Pulse Width	t_{WP}	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High Z	t_{WHZ}	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	—	15	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Output Active from End of Write	t_{OW}	0	—	0	—	ns

- Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Dout is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

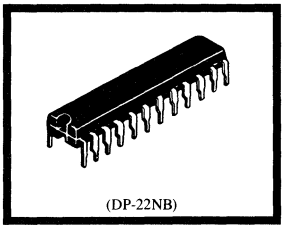
■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	8.0	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

HM6788H Series

16384-word × 4-bit High Speed Static RAM


(DP-22NB)

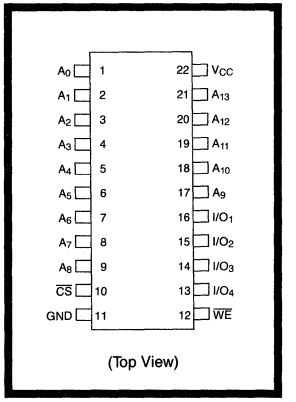
■ FEATURES

- Super fast access time: 15/20 ns (max.)
- +5V Single supply
- Low power dissipation (DC) operating: 280 mW (typ.)
- Completely static memory
  No clock or timing strobe required
- Balanced read and write cycle time
- Fully TTL compatible—all inputs and outputs

■ ORDERING INFORMATION

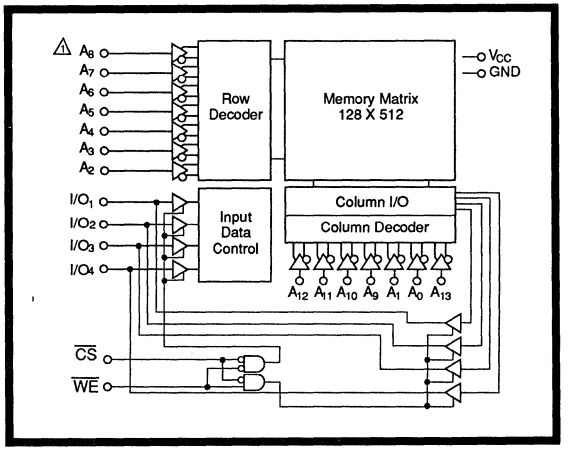
Type No.	Access Time	Package
HM6788HP-15	15ns	300 mil 22 pin Plastic DIP
HM6788HP-20	20ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	$T_{stg\ (bias)}$	-10 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input High (logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

*Pulse width ≤ 10 ns, DC: -0.5V

■ TRUTH TABLE

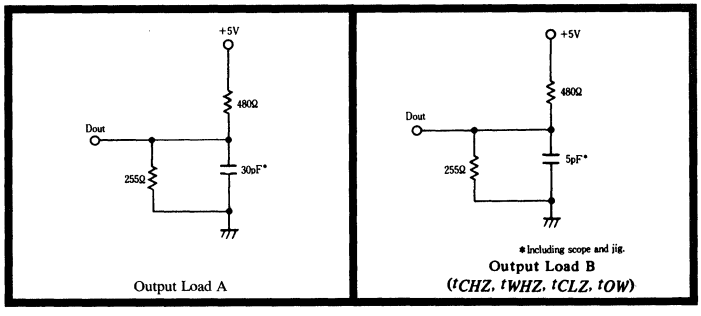
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	D_{OUT}	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	D_{IN}	Write Cycle (1), (2)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, GND = 0V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}$ = 0 mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	30	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ ≥ V_{CC} -0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} -0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4	—	—	V

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input timing reference levels: 1.5V
Input rise and fall times: 4 ns
Output load: See figure
Output reference levels: 1.5V



Output Load A

Output Load B
(*tCHZ, tWHZ, tCLZ, tOW*)

*including scope and jig capacitance

■ CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	V_{OUT} = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6788HP-15		HM6788HP-20		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	ns	—
Output Hold from Address Change	t_{OH}	3	—	3	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

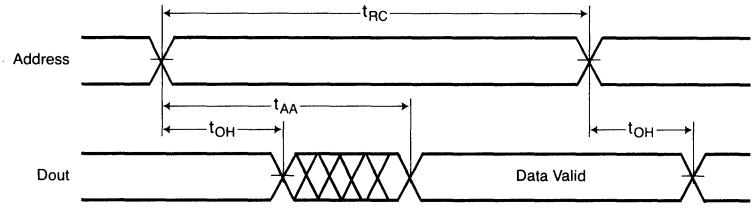
• Write Cycle

Item	Symbol	HM6788HP-15		HM6788HP-20		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	ns	2
Chip Selection to End of Write	t_{CW}	10	—	15	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	3	—	3	—	ns	—
Data Valid to End of Write	t_{DW}	9	—	12	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

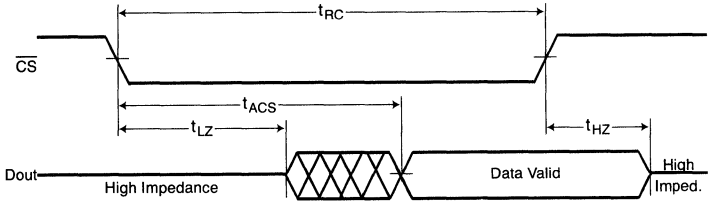
NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1)[1] [2]

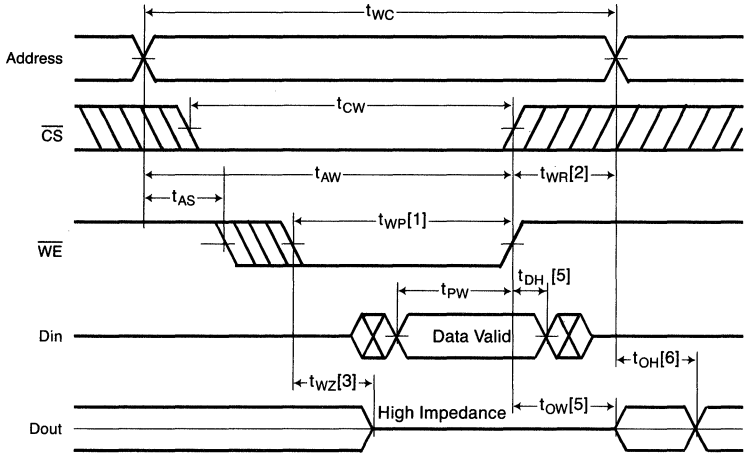


• Read Cycle (2)[1] [3]

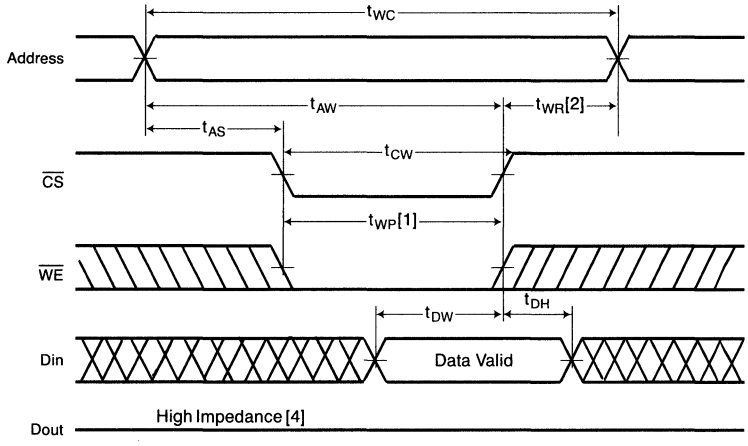


NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

- **Write Cycle (1) ($\overline{WE}$ Controlled)**



• Write Cycle (2) ($\overline{CS}$ Controlled)



NOTES:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{OUT} is the same phase of write data of this write cycle.

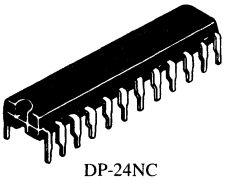
HM6789 Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with OE)

Features

- Super Fast Access Time:. . . . . 25/30 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 230 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789P Series



DP-24NC

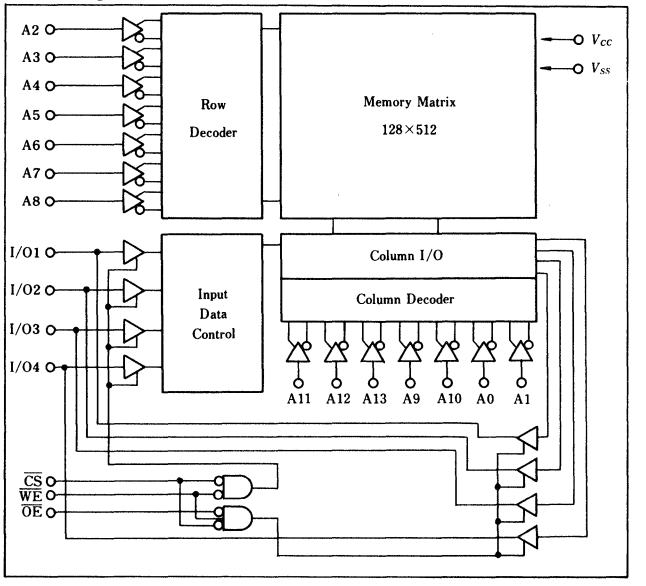
HM6789JP Series

CP-24D

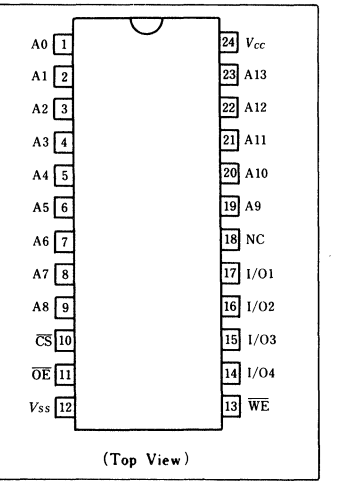
Ordering Information

Type No.	Access Time	Package
HM6789P-25 HM6789P-30	25ns 30ns	300 mil 24 pin Plastic DIP
HM6789JP-25 HM6789JP-30	25ns 30ns	300 mil 24 pin SOJ

Block Diagram



Pin Arrangement



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	$T_{stg\ (bias)}$	-10 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns.

Function Table

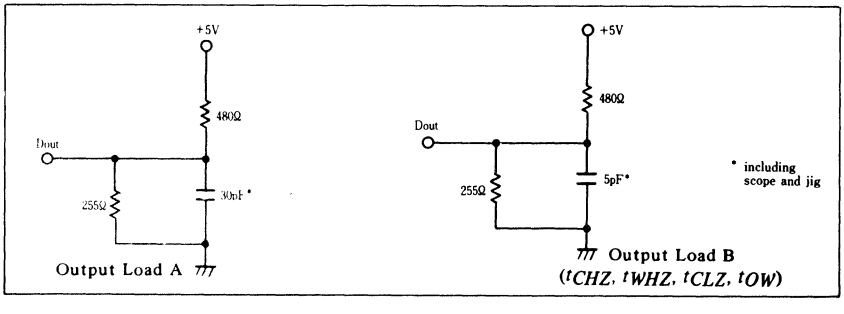
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Din	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, $I_{I/O}$ = 0mA
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} − 0.2V, V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} − 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
  ±200 mV from steady level (Output Load B)
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	8	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	0	–	0	–	ns
Output Enable to Output Valid	t_{OE}	0	15	0	15	ns
Output Enable to Output in Low Z	t_{OLZ}*1	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns

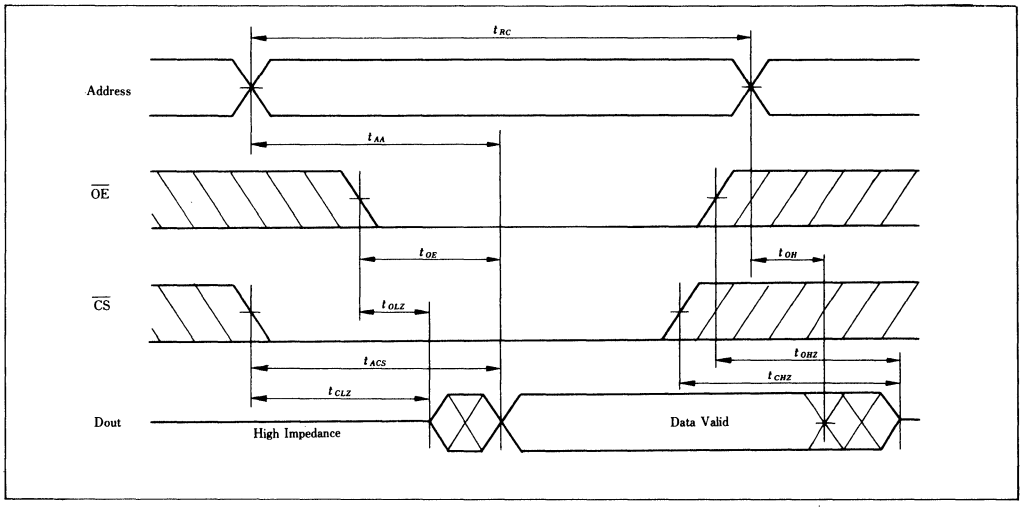
Write Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	30	–	ns
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	20	–	25	–	ns
Write Pulse Width	t_{WP}	20	–	25	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}*1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	–	20	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Output Disable to Output in Hihg Z	t_{OHZ}*1	0	10	0	10	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

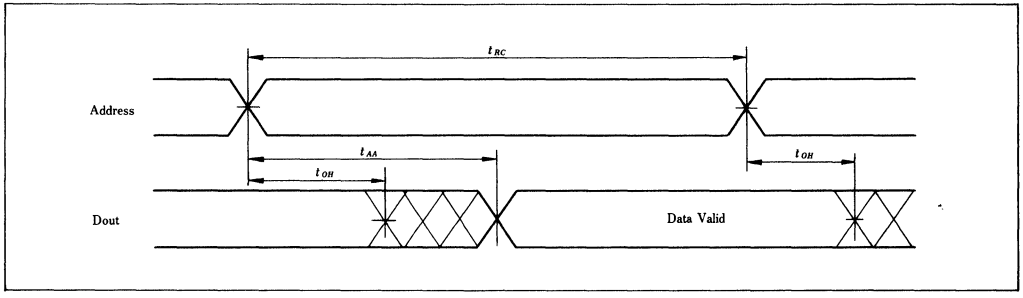
Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested

Timing Waveform

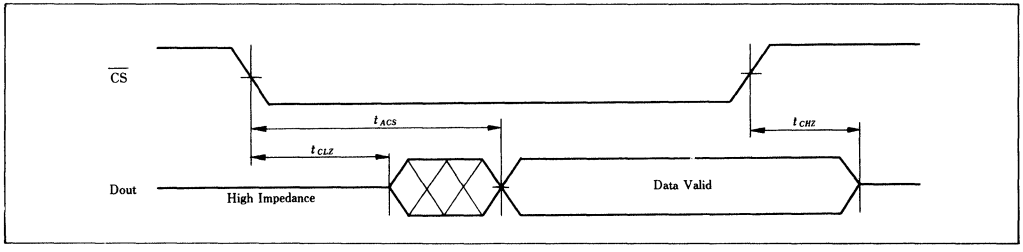
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

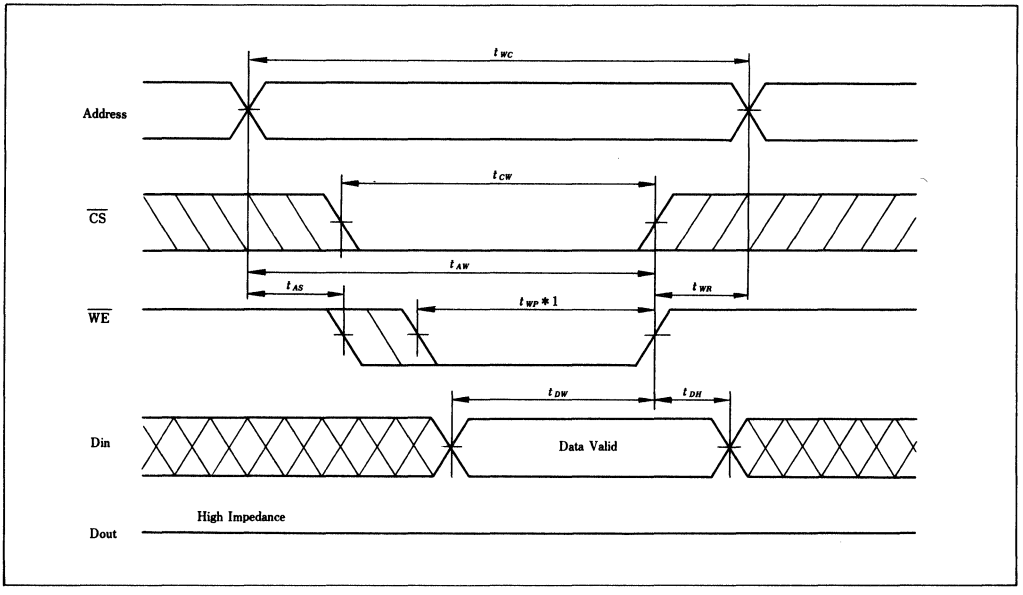


Read Cycle (3) *1, *3, *4

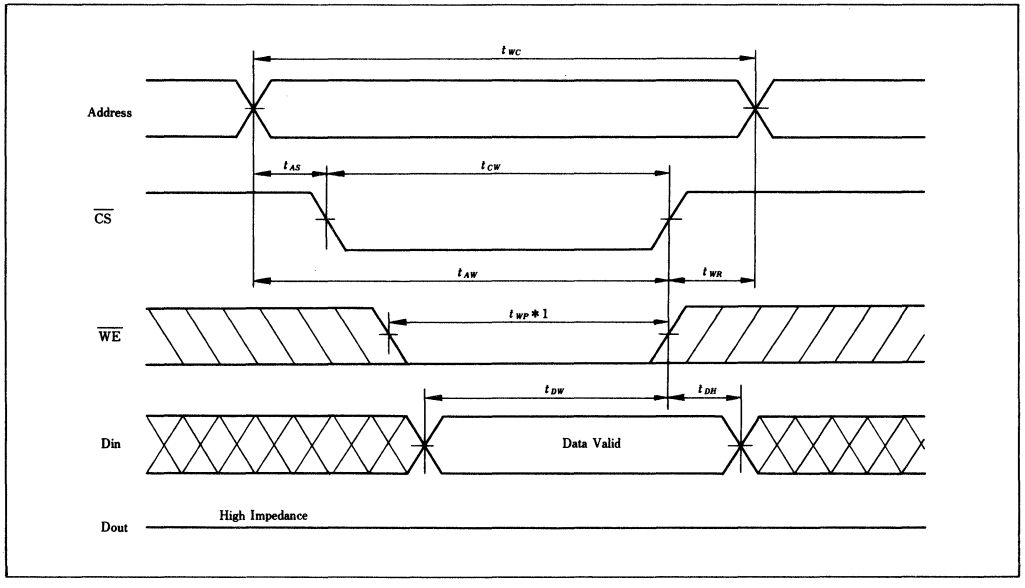


Notes) *1. $\overline{WE}$ = V_{IH}
*2. $\overline{CS}$ = V_{IL}
*3. $\overline{OE}$ = V_{IL}
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

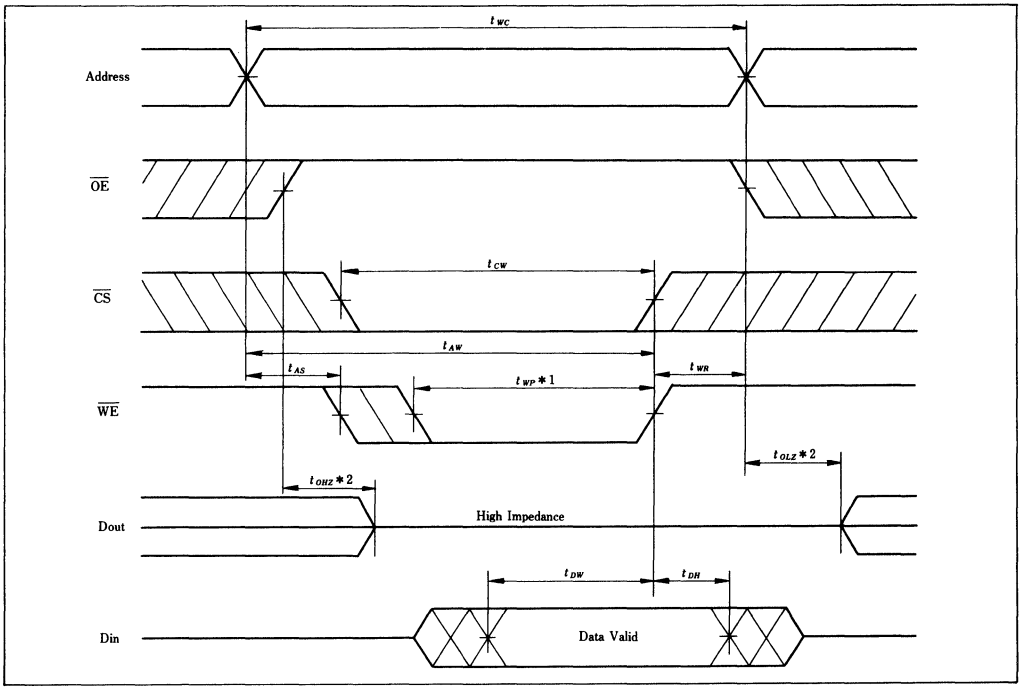
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



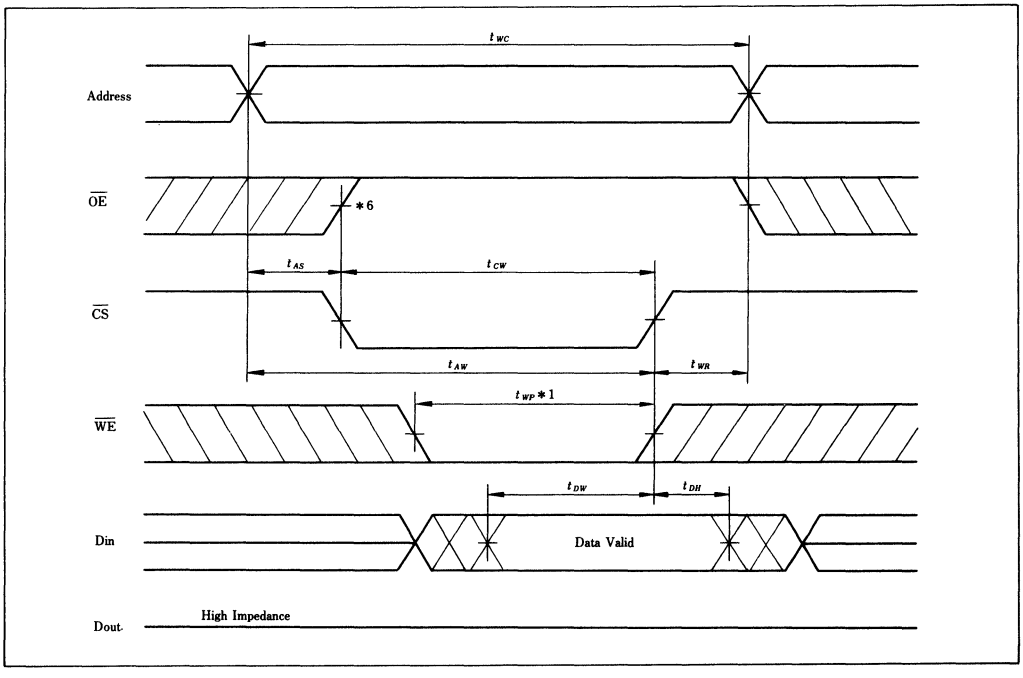
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



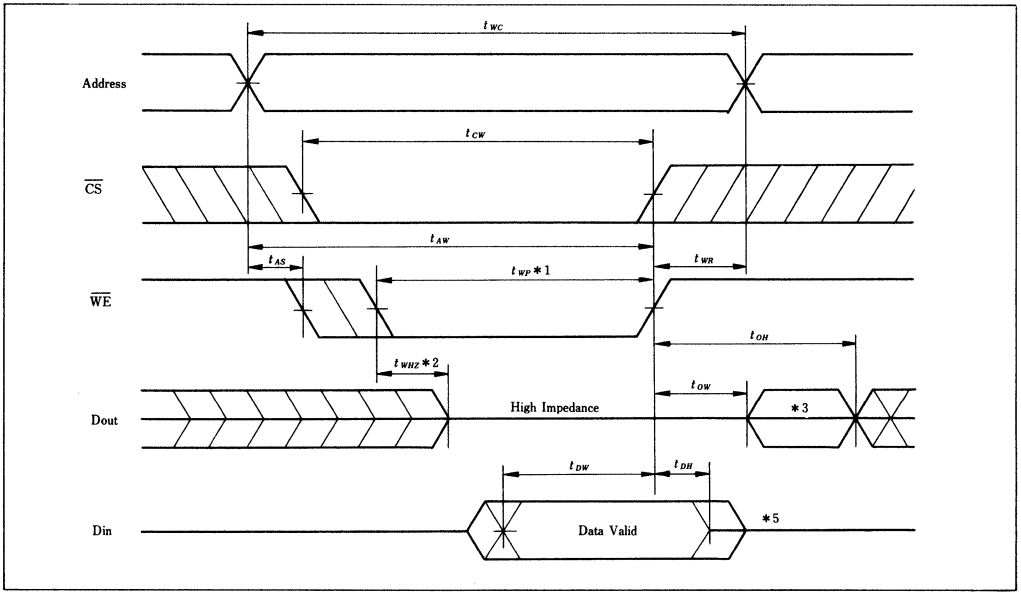
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



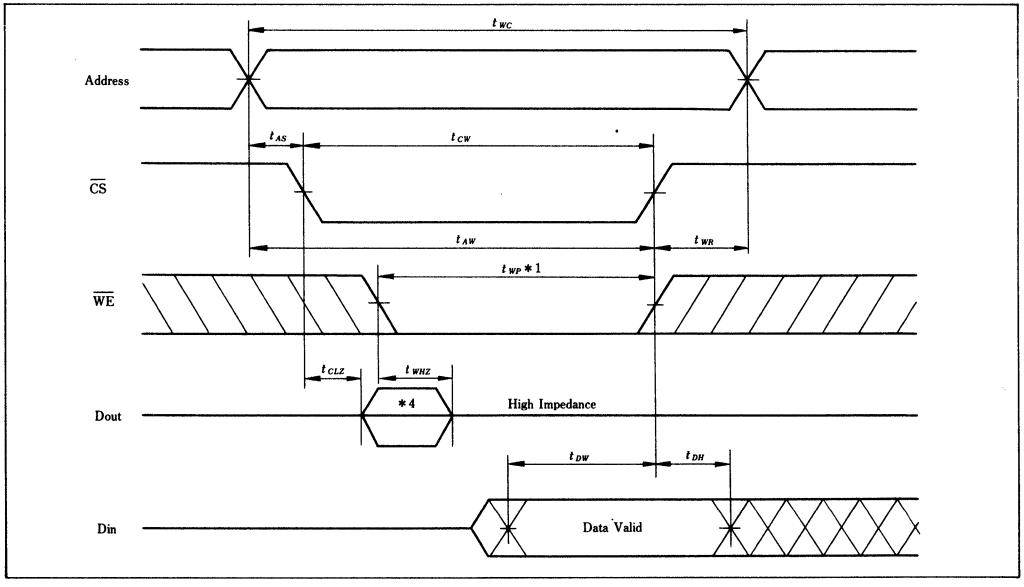
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3. Dout is the same phase of write data of this write cycle.

*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

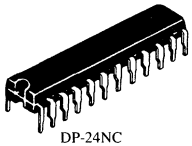
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6789H Series

16384-word × 4-bit High Speed Static RAM (with $\overline{OE}$)

HM6789HP Series



DP-24NC

HM6789HJP Series

CP-24D

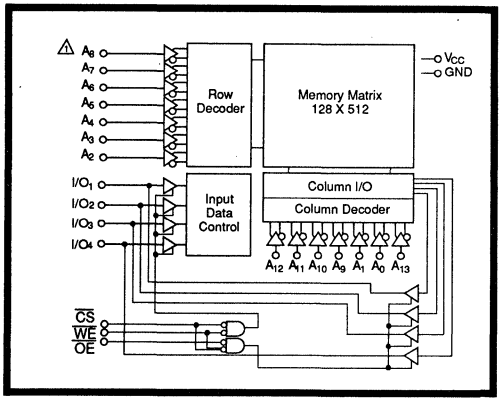
■ FEATURES

- Super fast access time: 15/20 ns (max.)
- Low power dissipation (DC) operating: 280 mW (typ.)
- +5V Single supply
- Completely static memory
  No clock or timing strobe required
- Balanced read and write cycle time
- Fully TTL compatible input and output

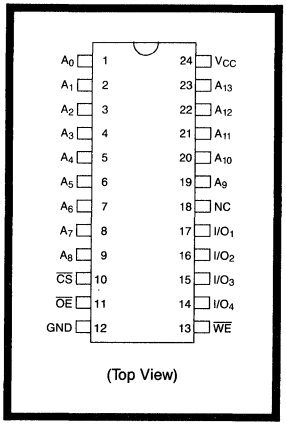
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6789HP-15	15ns	300 mil 24 pin Plastic DIP
HM6789HP-20	20ns	
HM6789HJP-15	15ns	300 mil 24 pin SOJ
HM6789HJP-20	20ns	

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	$T_{stg\ (bias)}$	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	-3.0	—	0.8	V

*Pulse width ≤ 10 ns, DC: -0.5V

■ TRUTH TABLE

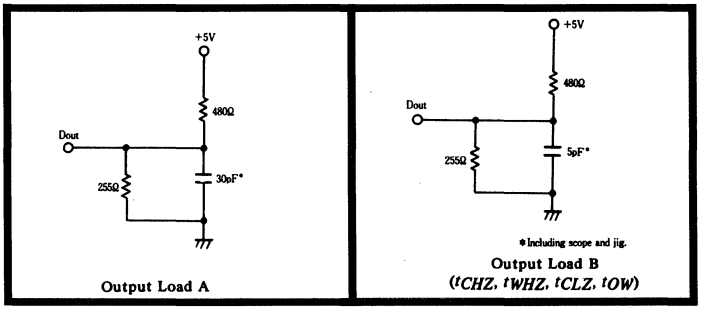
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	D_{OUT}	Read Cycle (1), (2), (3)
L	H	L	Write	I_{CC}, I_{CC1}	D_{IN}	Write Cycle (1), (2), (3), (4)
L	L	L		I_{CC}, I_{CC1}	D_{IN}	Write Cycle (5), (6)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0 mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} -0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} -0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4	—	—	V

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input and output reference levels: 1.5V
± 200 mV from steady level
(Output Load B)
Input rise and fall time: 4 ns
Output load: See figure



Output Load A

Output Load B
(*tCHZ, tWHZ, tCLZ, tOW*)

*including scope and jig capacitance

■ CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitance	C_{IN}	—	—	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	ns	—
Chip Selection to Output in Low Z	t_{CLZ}	3	—	3	—	ns	1
Output Enable to Output Valid	t_{OE}	0	12	0	15	ns	—
Output Enable to Output in Low Z	t_{OLZ}	3	—	3	—	ns	1
Chip Deselection to Output in High Z	t_{CHZ}	0	6	0	8	ns	1
Output Hold from Address Change	t_{OH}	3	—	3	—	ns	—

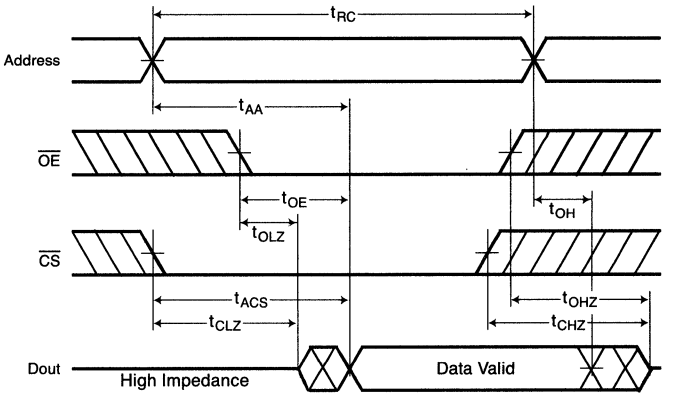
• Write Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	ns	—
Chip Selection to End of Write	t_{CW}	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	3	—	3	—	ns	—
Write to Output in High Z	t_{WHZ}	0	6	0	8	ns	1
Data Valid to End of Write	t_{DW}	9	—	12	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	0	6	0	8	ns	1
Output Active from End of Write	t_{OW}	0	—	0	—	ns	1

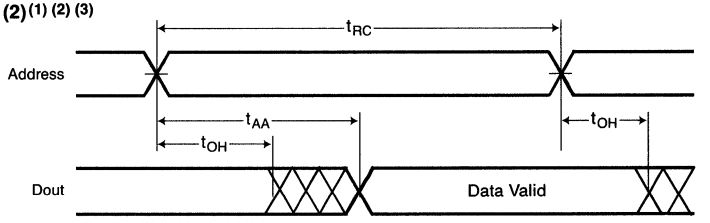
NOTE: 1. Transition is measured ± 200 mV from steady state voltage Load B. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

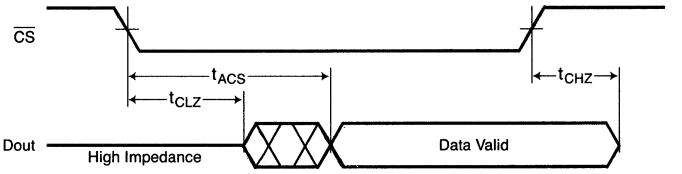
• Read Cycle (1)[1]



• Read Cycle (2)[1] [2] [3]

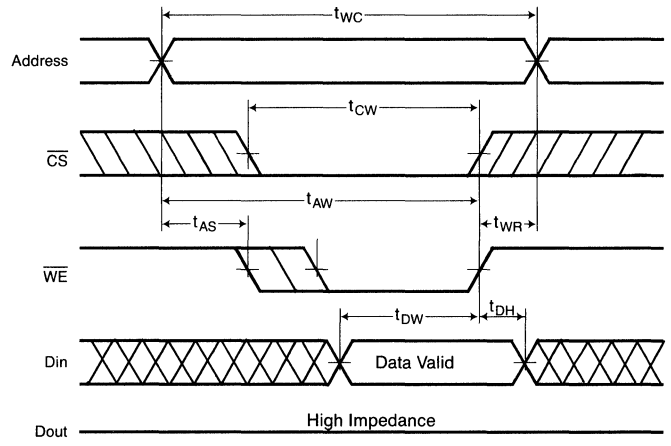


• Read Cycle (3)[1] [3] [4]

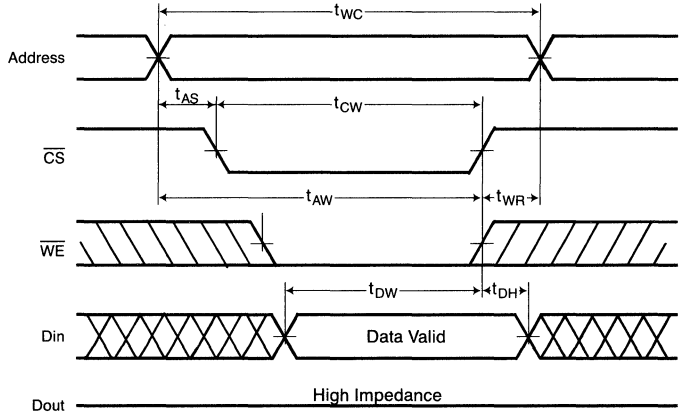


NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

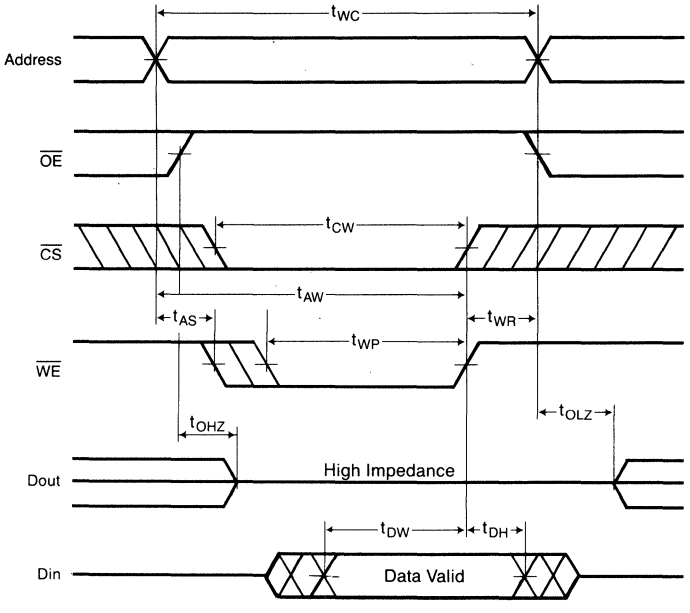
• **Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)**



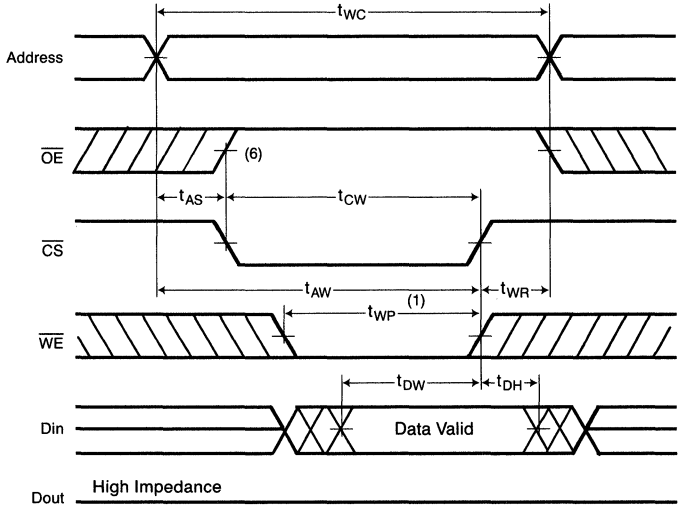
• **Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)**



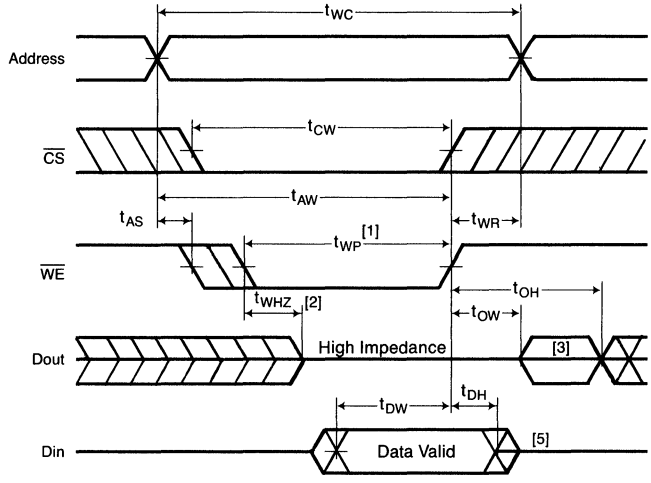
• **Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)**



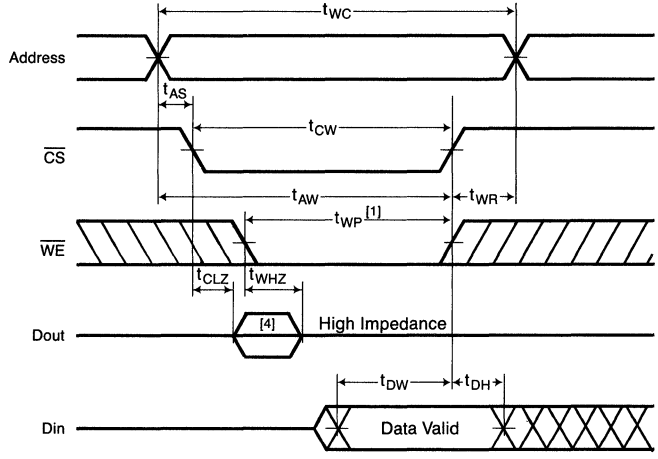
• **Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)**



• **Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)**



• **Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)**



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. D_{OUT} is the same phase of write date of this write cycle.
4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition of after the $\overline{OE}$ transition, output remain in high impedance state.

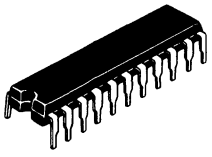
HM6287 Series

6553-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
  Standby: 100μW (typ.)/10μW (typ.) (L-version)
  Operation: 300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output
- Capability of Battery Back Up Operation (L-version)

HM6287P Series

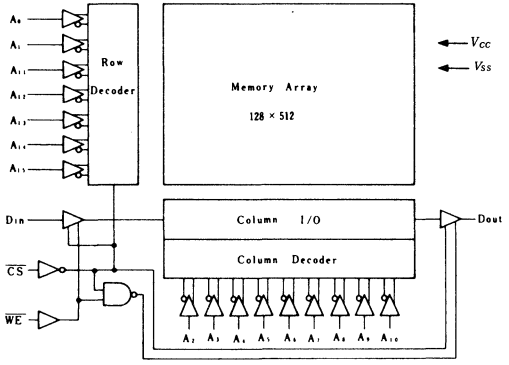


(DP-22N)

■ ORDERING INFORMATION

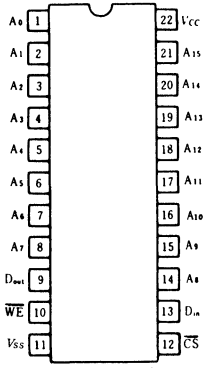
Type No.	Access Time	Package
HM6287P-45	45ns	300 mil 22 pin Plastic DIP
HM6287P-55	55ns	
HM6287P-70	70ns	
HM6287LP-45	45ns	
HM6287LP-55	55ns	
HM6287LP-70	70ns	

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

- HM6287P Series



(Top View)

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_T	−0.5*1 to +7.0	V
Power Dissipation		P_T	1.0	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature	Plastic	T_{stg}	−55 to +125	°C
	Ceramic		−65 to +150	
Temperature Under Bias		T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width ≦ 20ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{out} = 0mA	–	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	10	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V, V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V	–	0.02	2.0	mA
			–	2*2	100*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = −4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	5	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	7.5	pF

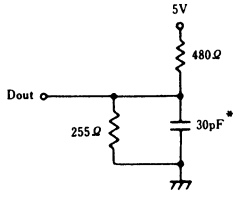
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

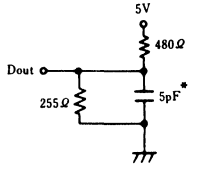
Input Pulse Levels: V_{SS} to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

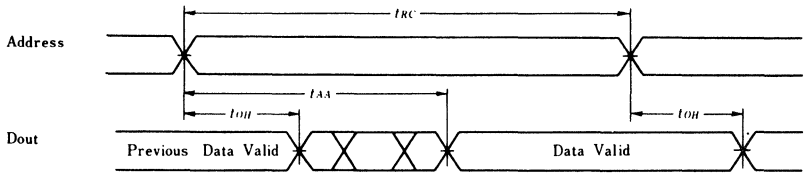


*Including scope & jig capacitance

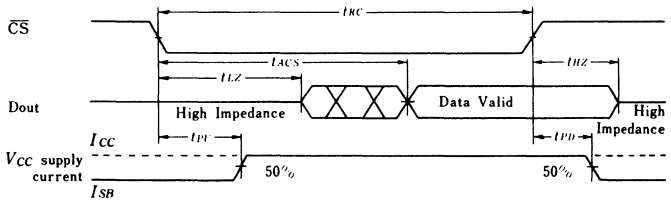
• READ CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns	1
Address Access Time	t_{AA}	–	45	–	55	–	70	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	7
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	–	40	ns	7

• Timing Waveform of Read Cycle No. 1[4][5]



• Timing Waveform of Read Cycle No. 2[4][6]

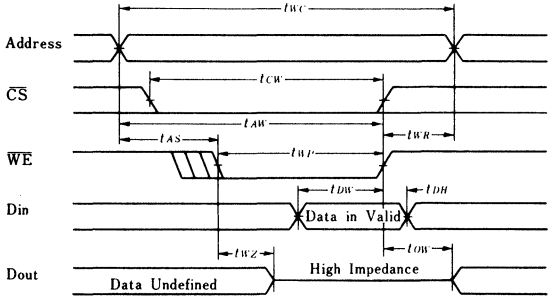


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

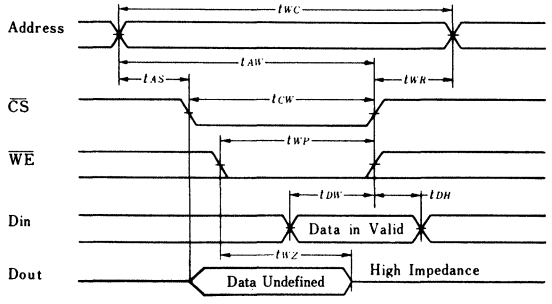
• WRITE CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns	2
Chip Selection to End of Write	t_{CW}	40	–	50	–	55	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	55	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	40	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	30	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3, 4

• Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



• Timing Waveform of Write Cycle No. 1 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high Simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

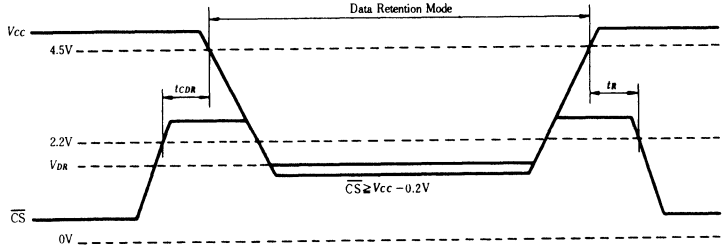
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L-version.

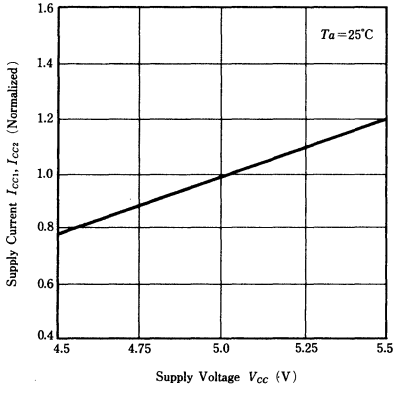
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}$ - 0.2V, $V_{in} \geqq V_{CC}$-0.2V or 0V $\leqq V_{in} \leqq$ 0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR}		–	1	50*2	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

Note) *1. t_{RC} = Read Cycle Time
*2. V_{CC} = 3.0V

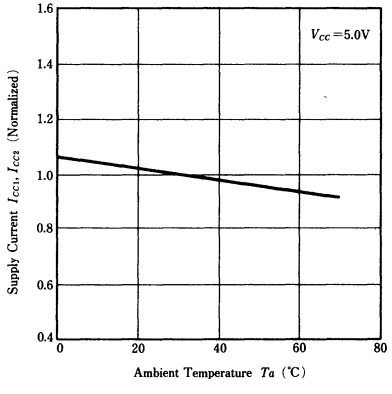
● LOW V_{CC} DATA RETENTION WAVEFORM



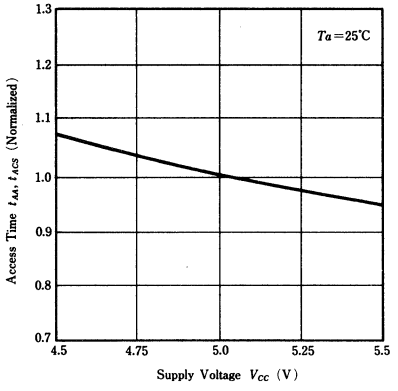
SUPPLY CURRENT vs. SUPPLY VOLTAGE



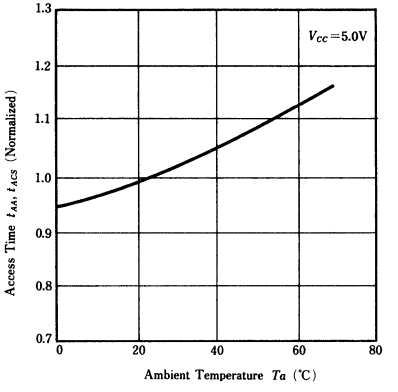
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



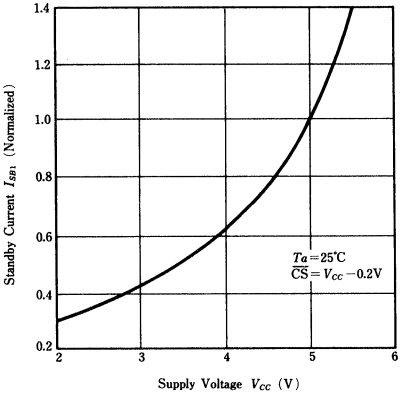
ACCESS TIME vs. SUPPLY VOLTAGE



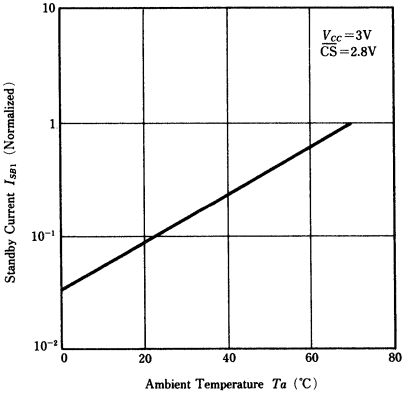
ACCESS TIME vs. AMBIENT TEMPERATURE



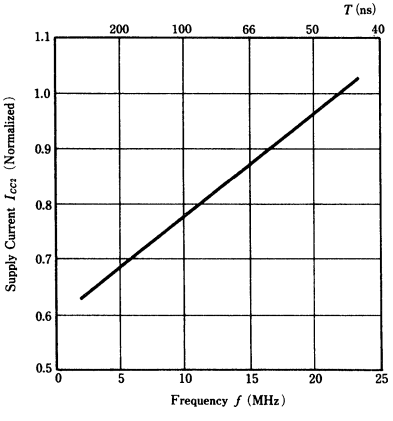
STANDBY CURRENT vs. SUPPLY VOLTAGE



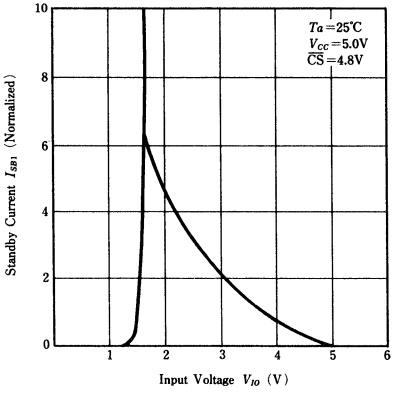
STANDBY CURRENT vs. AMBIENT TEMPERATURE



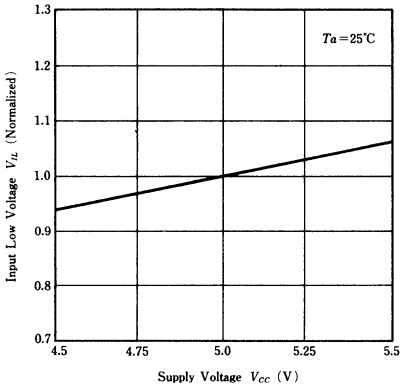
SUPPLY CURRENT vs. FREQUENCY



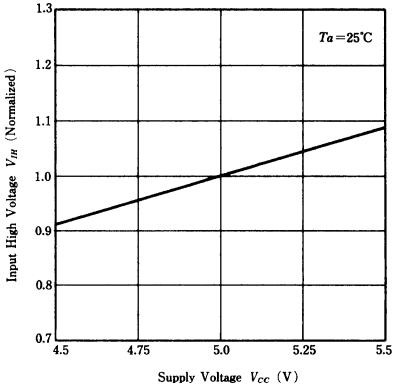
STANDBY CURRENT vs. INPUT VOLTAGE



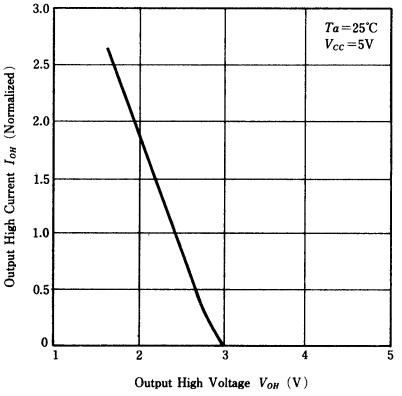
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



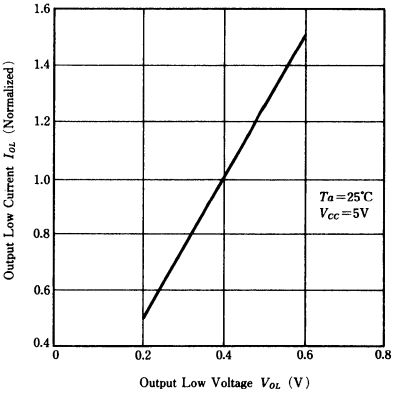
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



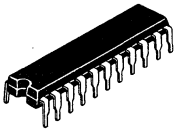
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



HM6287H Series

65536-word × 1-bit High Speed Static C-MOS RAM

HM6287HP Series



(DP-22NB)

HM6287HJP Series

(CP-24D)

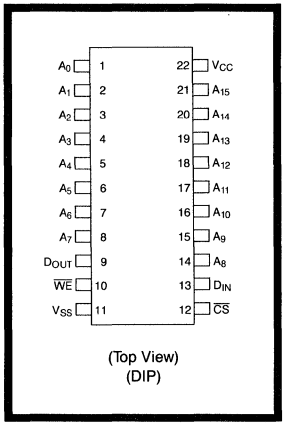
■ FEATURES

- Single 5 V supply and high density 22 pin DIP and 24 pin SOJ
- High Speed
  Access time 25/35 ns (max.)
- Low power
  Active mode 300 mW (typical)
  Standby mode 100 μW (typical)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible—all inputs and outputs

■ ORDERING INFORMATION

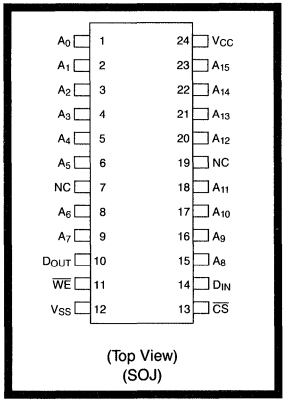
Part No.	Access	Package
HM6287HP-25	25 ns	300 mil 22 pin Plastic DIP
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300 mil 24 pin SOJ
HM6287HJP-35	35 ns	

■ PIN ARRANGEMENT



(Top View)
(DIP)

■ PIN ARRANGEMENT

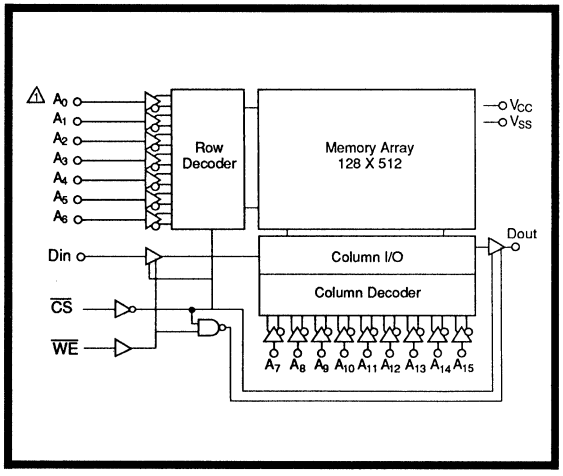


(Top View)
(SOJ)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{15}	Address
D_{IN}	Input
D_{OUT}	Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5[1] to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. V_T min = -2.0V for pulse width ≤ 10 ns.

■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Standby	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}	D_{OUT}	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0.0	0.0	0.0	V	
Input High (logic 1) Voltage	V_{IH}	2.2	—	6.0	V	
Input Low (logic 0) Voltage	V_{IL}	-0.5[1]	—	0.8	V	

NOTE: 1. V_{IL} min = -2.0V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*[1]	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max., V_{IN} = 0V to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}
Operating V_{CC} Current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Standby V_{CC} Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}
Standby V_{CC} Current[1]	I_{SB1}[2]	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} - 0.2V
	I_{SB1}[3]	—	0.02	2.0	mA	
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

NOTE: 1. This parameter is sampled and not 100% tested.

■ CAPACITANCE (T_A = 25°C, f = 1.0 MHz)[1]

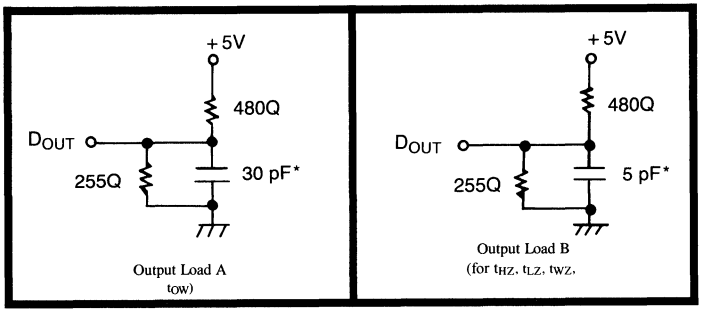
Parameter	Symbol	Min.	Typ	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}	—	—	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	—	—	8	pF	V_{OUT} = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Test Conditions

Input pulse levels:	0.0V to 3.0V
Input rise and fall times:	5 ns
Output load:	see figure
Input and output timing reference levels:	1.5V



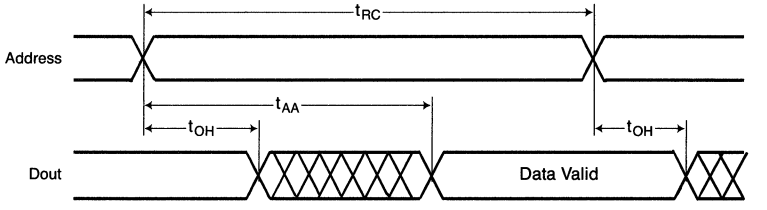
*including scope and jig capacitance

• Read Cycle

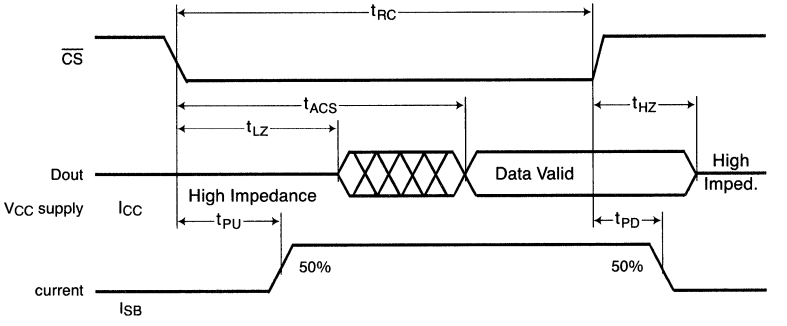
Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold from Address Change	t_{OH}	3	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}[1]	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}[1]	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}[1]	0	—	0	—	ns
Chip Deselection to Output in Down Time	t_{PD}	—	25	—	30	ns

NOTE: 1. Transition is measured ± 200 mV from steady state voltage with Load B. This parameter is sampled and not 100% tested.

• Timing Waveform of Read Cycle No. 1 (1), (2), (4)



• Timing Waveform of Read Cycle No. 2 (1), (3)



NOTES: 1. $\overline{WE}$ is high for read cycle.

2. Device is continuously, $\overline{CS}$ = V_{IL}.

3. Address valid prior to or coincident with $\overline{CS}$ transition low.

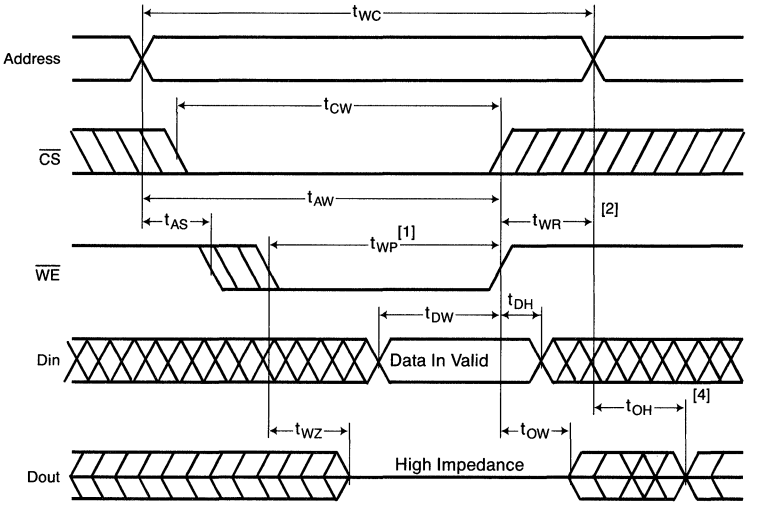
4. All read cycle timing are referenced from last valid address to the first transitioning address.

■ Write Cycle

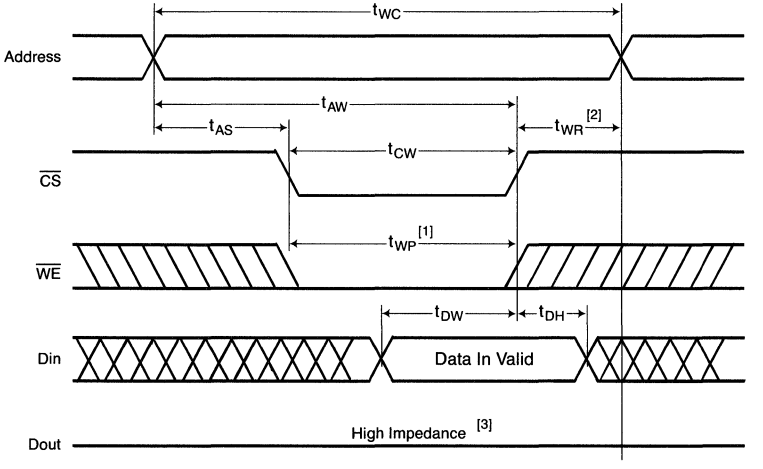
Parameter	Symbol	HM6287H-25		HM6287H-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[1]	0	8	0	10	ns
Output Active From End of Write	t_{OW}[1]	5	—	5	—	ns

NOTE: 1. Transition is measured ± 200 mV from steady state voltage with Load B. This parameter is sampled and not 100% tested.

- **Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)**



- **Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)**



NOTES: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

3. If the $\overline{CS}$ low transition occurs simultaneously with the buffers remain in a high impedance state.

4. D_{OUT} is the same phase of write data of this write cycle, if t_{WR} is long enough.

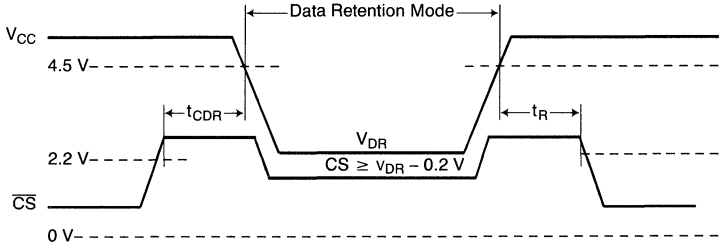
■ Low V_{CC} Data Retention Characteristics (T_A = 0 to +70°C)

(This specification is guaranteed only for L-version.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $0V \leq V_{IN} \leq 0.2V$
Data Retention Current	I_{CCDR}	—	—	50[2], 35[3]	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	t_{RC}[1]	—	—	ns	

NOTES: 1. t_{RC} = Read cycle time.
2. V_{CC} = 3.0V.
3. V_{CC} = 2.0V.

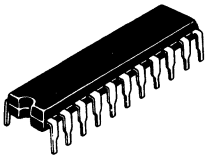
• Low V_{CC} Data Retention Waveform



HM6787 Series

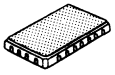
65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

HM6787P Series



(DP-22N)

HM6787CG Series



(CG-22A)

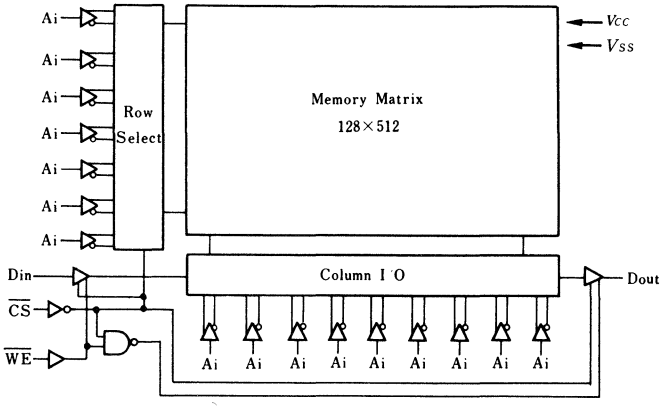
■ FEATURES

- Super Fast Access Time: 25ns/30ns (max.)
- Low Power Dissipation (DC):
  Operating 180mW (typ)
- High Driving Capability: I_{OL} 16mA
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

■ ORDERING INFORMATION

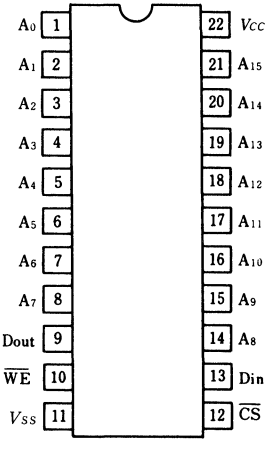
Type No.	Access Time	Package
HM6787P-25 HM6787P-35	25ns 35ns	300 mil 22 pin Plastic DIP
HM6787CG-25 HM6787CG-30	25ns 30ns	22 pin ceramic Chip Carrier

■ BLOCK DIAGRAM



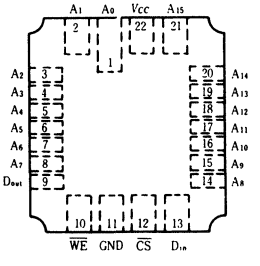
■ PIN ARRANGEMENT

- HM6787P Series



(Top View)

- HM6787CG Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}	Dout
L	L	Write	I_{CC}	High Z

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

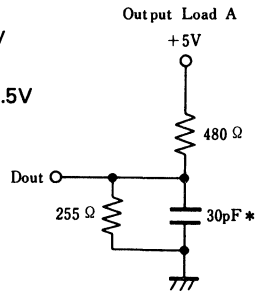
Note) *1. −3.0V for pulse width ≦ 20ns.

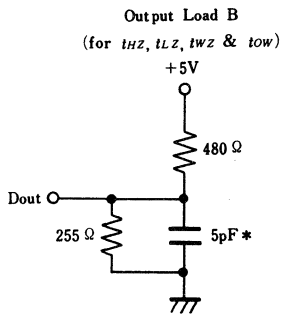
■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to +70°C)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, $I_{I/O}$ = 0mA	–	–	40	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$	–	–	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 16mA	–	–	0.5	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	–	–	V

■ AC TEST CONDITIONS

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure





* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	typ.	Unit	Conditions
Input Capacitance	C_{IN}	2.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	3.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

• READ CYCLE

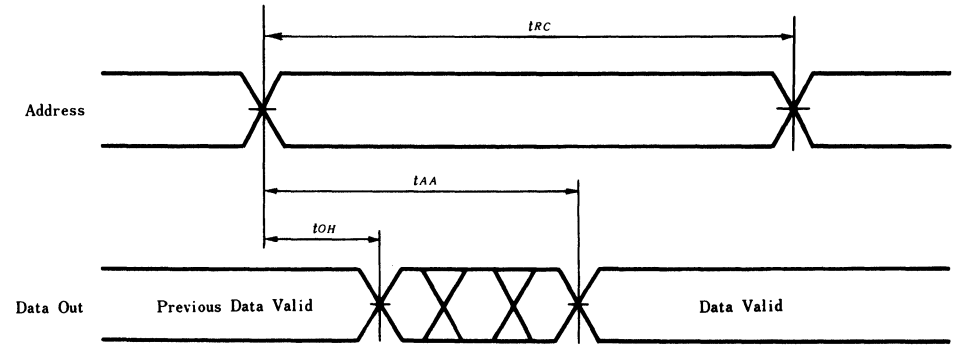
Item	Symbol	HM6787-25		HM6787-30/35		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	25	–	30	ns

• WRITE CYCLE

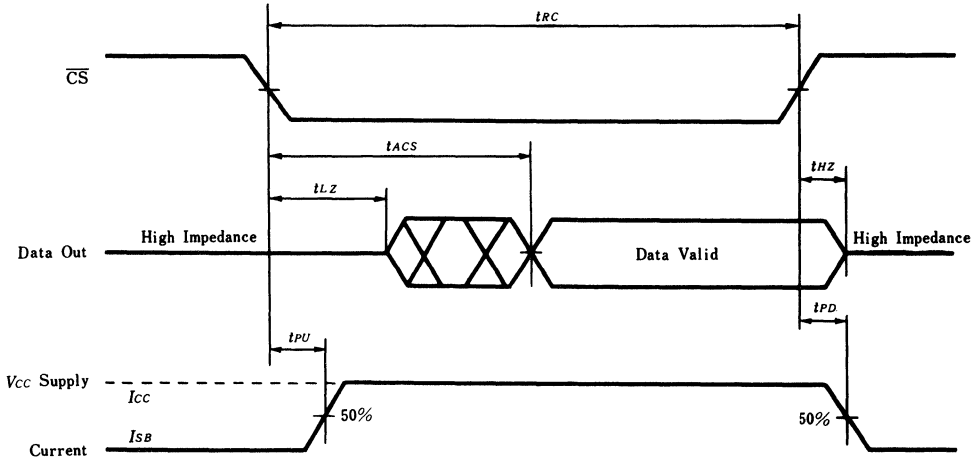
Item	Symbol	HM6787-25		HM6787-30/35		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	25	–	30	–	ns	2
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	5	–	5	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1[1), 2)]

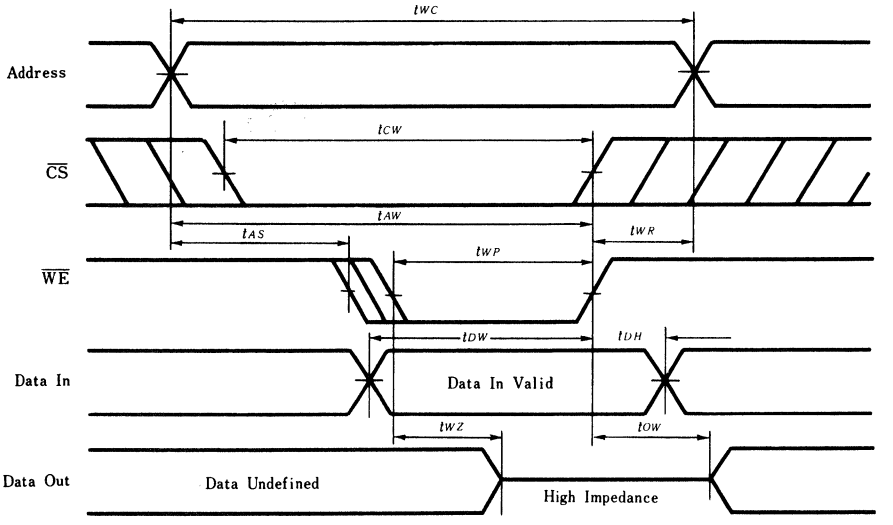


• TIMING WAVEFORM OF READ CYCLE NO. 2[1), 3)]



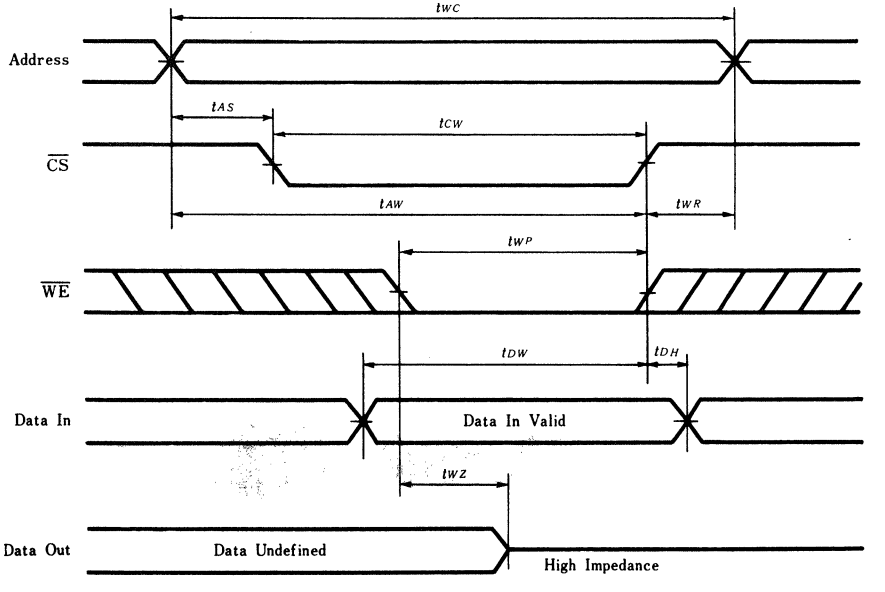
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



Note: 1. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)

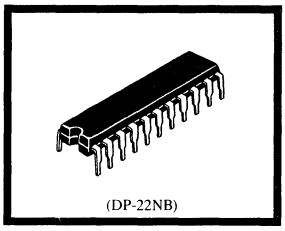


Note: 1. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

HM6787H Series

65536-word × 1-bit High Speed Static RAM


(DP-22NB)

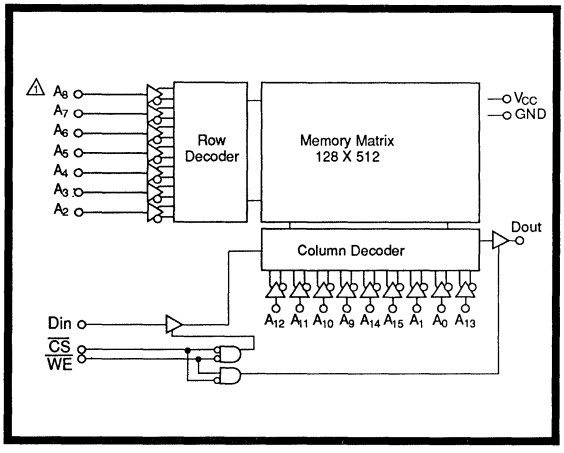
■ FEATURES

- Super fast access time: 15/20 ns (max.)
- Low power dissipation (DC) operating: 280 mW (typ.)
- +5V Single supply
- Completely static memory
  No clock or timing strobe required
- Balanced read and write cycle time
- Fully TTL compatible input and output

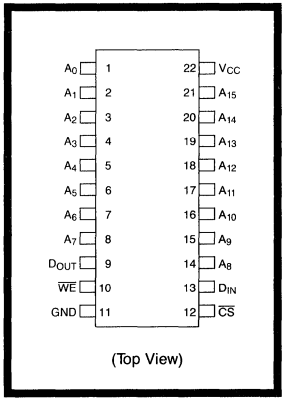
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6787HP-15	15ns	300 mil 22 pin
HM6787HP-20	20ns	Plastic DIP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to GND Pin	V_T	-0.5 to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-3.0*	—	0.8	V

*Pulse width ≤ 10 ns, DC: -0.5V

■ TRUTH TABLE

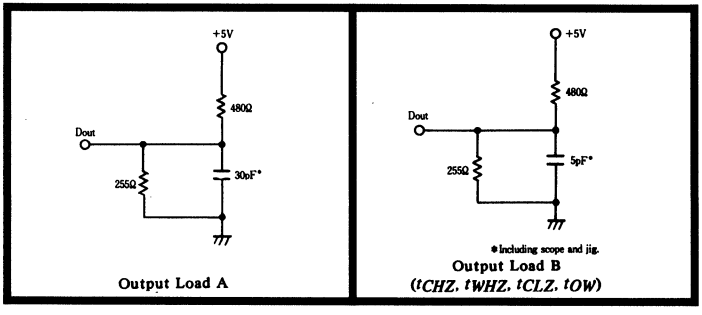
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	I_{CC}, I_{CC1}	D_{OUT}
L	L	Write	I_{CC}, I_{CC1}	I_{CC}, I_{CC1}	High Z

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, GND = 0V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% I_{OUT} = 0 mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} -0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} -0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4	—	—	V

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input timing reference levels: 1.5V
Output load: See figure
Input rise and fall times: 4 ns
Output reference levels: 1.5V



Output Load A

Output Load B
(tCHZ, tWHZ, tCLZ, tOW)

*including scope and jig capacitance

■ CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6787HP-15		HM6787HP-20		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	ns	—
Output Hold from Address Change	t_{OH}	3	—	3	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6787HP-15		HM6787HP-20		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	ns	2
Chip Selection to End of Write	t_{CW}	10	—	15	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	3	—	3	—	ns	—
Data Valid to End of Write	t_{DW}	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

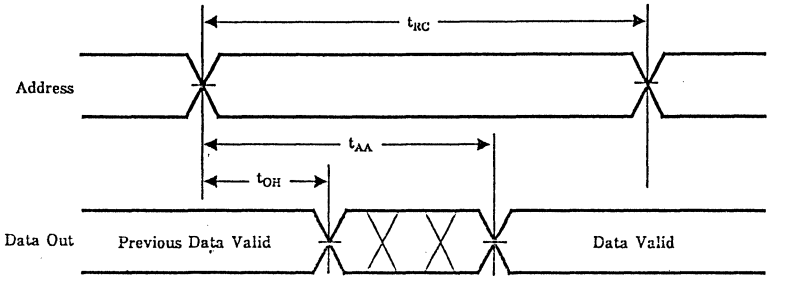
2. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

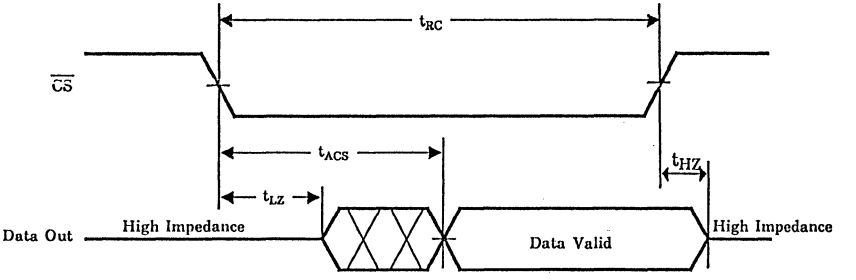
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1)[1] [2]



• Read Cycle (2)[1] [3]



NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.

2. Address valid prior to or coincident with $\overline{CS}$ transition low.

3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

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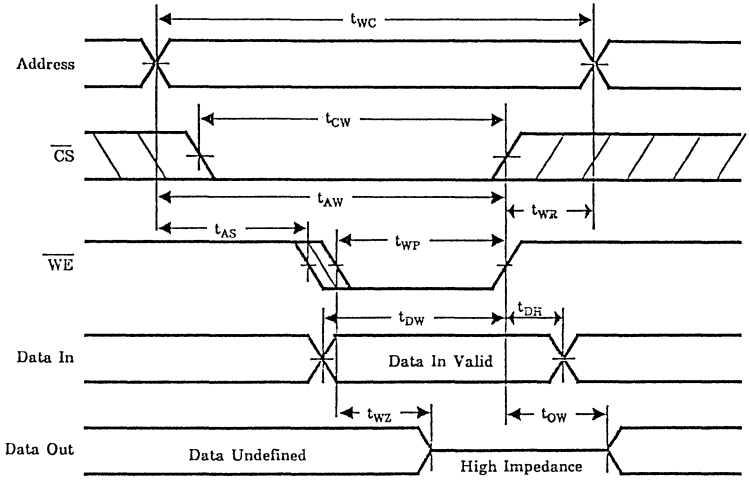
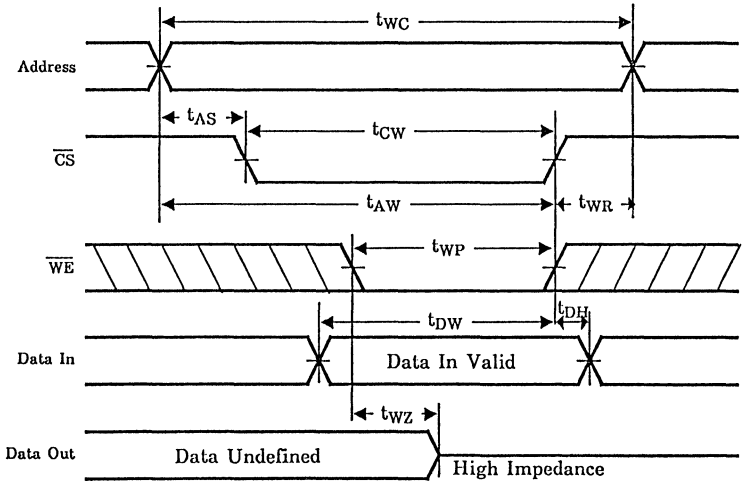
• Write Cycle (1) ($\overline{WE}$ Controlled)



NOTE: 1. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

• Write Cycle (2) ($\overline{CS}$ Controlled)



NOTE: 1. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

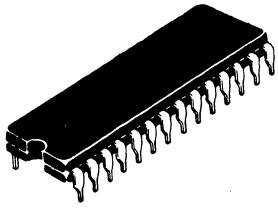
HM62256 Series

32768-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

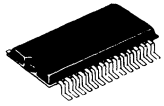
- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 200μW (typ)/10μW (typ) (L-version),
  Operation: 40mW (typ.) (f = 1MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/L-SL version)

HM62256P Series



(DP-28)

HM62256FP Series

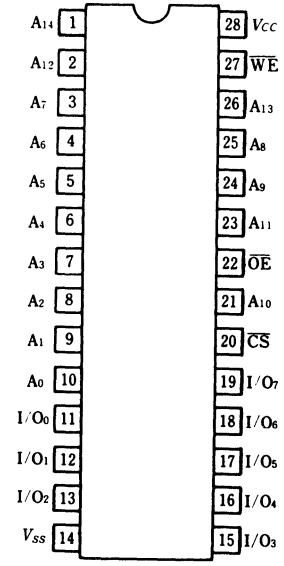


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62256P-8	85ns	600 mil 28 pin Plastic DIP
HM62256P-10	100ns	
HM62256P-12	120ns	
HM62256P-15	150ns	
HM62256LP-8	85ns	
HM62256LP-10	100ns	
HM62256LP-12	120ns	
HM62256LP-15	150ns	
HM62256LP-10SL	100ns	
HM62256LP-12SL	120ns	
HM62256LP-15SL	150ns	
HM62256FP-8T	85ns	28 pin Plastic SOP
HM62256FP-10T	100ns	
HM62256FP-12T	120ns	
HM62256FP-15T	150ns	
HM62256LFP-8T	85ns	
HM62256LFP-10T	100ns	
HM62256LFP-12T	120ns	
HM62256LFP-15T	150ns	
HM62256LFP-10SLT	100ns	
HM62256LFP-12SLT	120ns	
HM62256LFP-15SLT	150ns	

■ PIN ARRANGEMENT



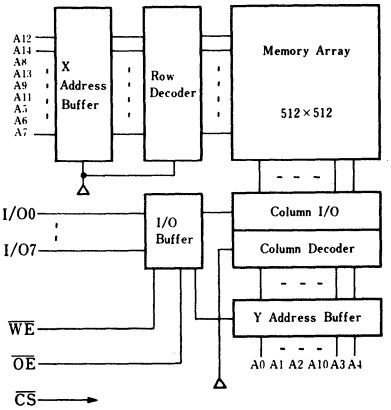
(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.0V for pulse width ≦ 50ns

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item		Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current		$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current		$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	8	15	mA
Average Operating Power Supply Current	HM62256-8	I_{CC1}	Min. Cycle, duty=100%, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	50	70	mA
	HM62256-10			–	40	70	
	HM62256-12			–	35	70	
	HM62256-15			–	33	70	
		I_{CC2}	$\overline{CS}$=V_{IL}, V_{IH}=V_{CC}, V_{IL}=0V, $I_{I/O}$=0mA, f=1MHz	–	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS}$=V_{IH}	–	0.5	3	mA
		I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V	–	0.04	2	mA
				–	2*2	100*2	μA
				–	2*3	50*3	
Output Voltage		V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
		V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

Notes) *1. Typical values are at V_{CC}=5.0V, T_a= 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

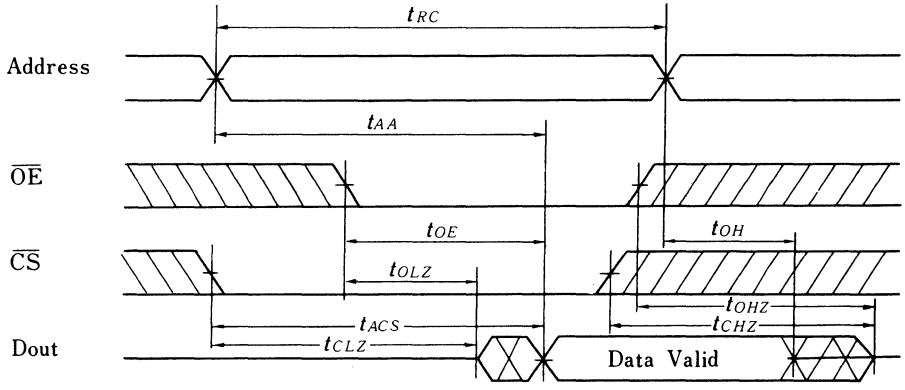
■ AC CHARACTERISTICS (V_{CC}=5V± 10%, T_a=0 to +70°C unless otherwise noted)

- **AC Test Conditions**
  - ○ Input pulse levels: 0.8V to 2.4V
  - ○ Input rise and fall times: 5ns
  - ○ Input and Output timing reference levels: 1.5V
  - ○ Output load: 1TTL Gate and C_L (100pF) (Including scope and jig)

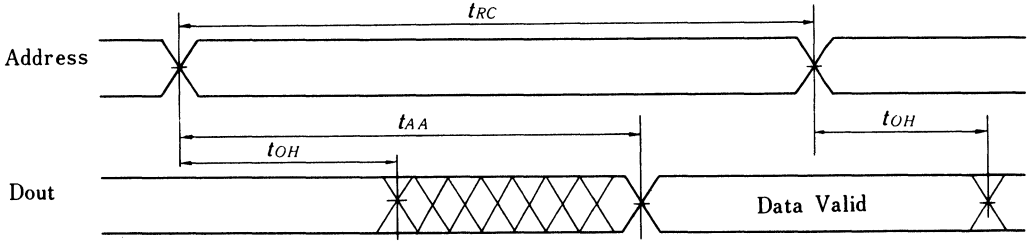
- **Read Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	–	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	85	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	45	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

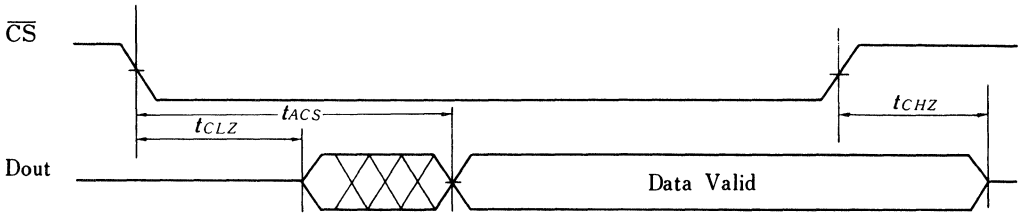
- **Timing Waveform of Read Cycle No. 1[1]**



- **Timing Waveform of Read Cycle No. 2[1][2][4]**



- **Timing Waveform of Read Cycle No. 3[1][3][4]**

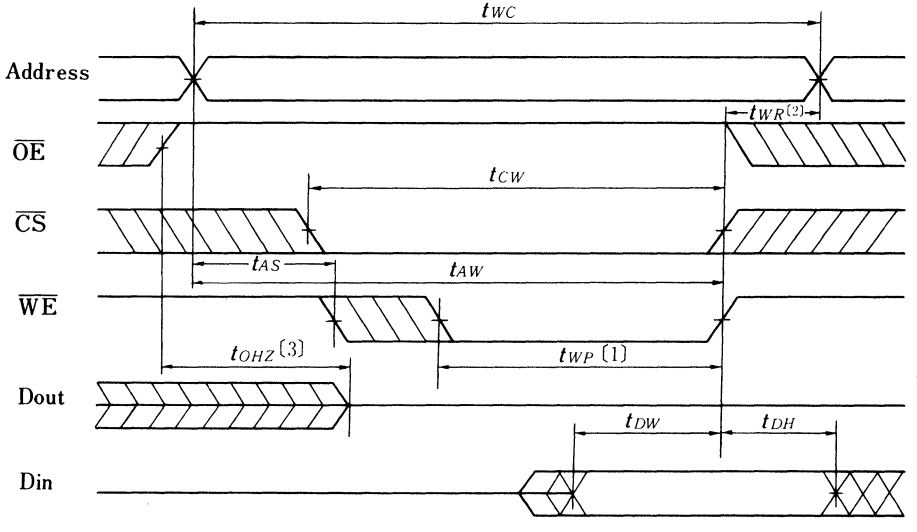


Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

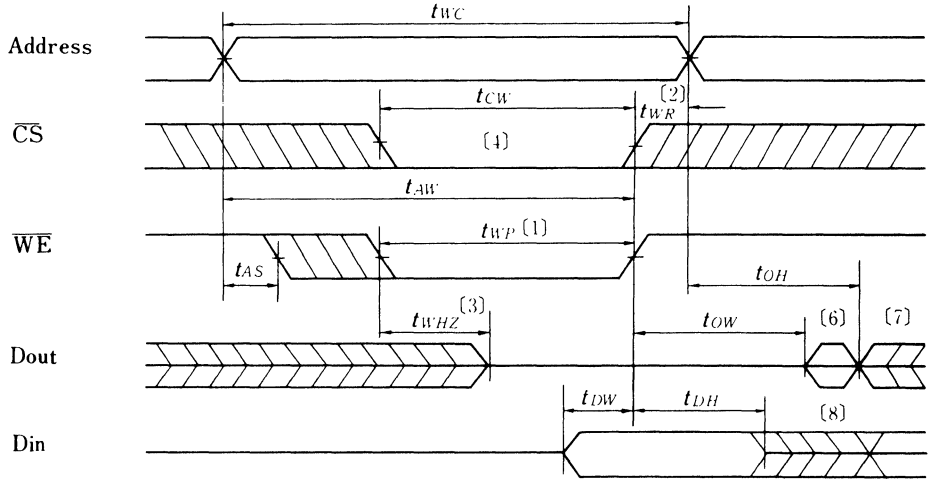
- **Write Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	–	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	75	–	80	–	85	–	100	–	ns
Address Valid to End of Write	t_{AW}	75	–	80	–	85	–	100	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	60	–	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns

- **Timing Waveform of Write Cycle No. 1 ($\overline{OE}$ Clock)**



- **Timing Waveform of Write Cycle No. 2[5] ($\overline{OE}$ Low Fixed)**



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

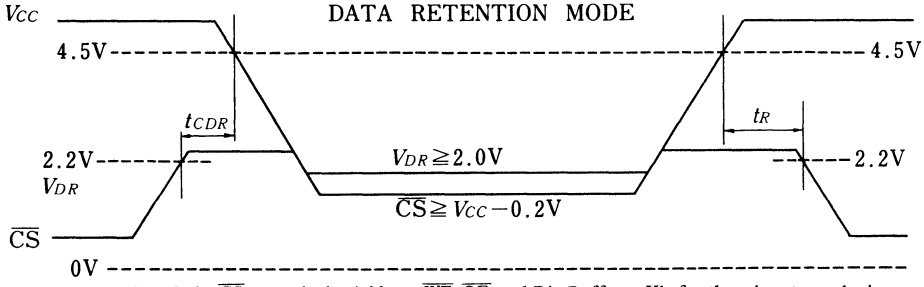
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

(This characteristics is guaranteed only for L-and L-SL version)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Date Retention	V_{DR}	$\overline{CS} \geqq V_{CC}$ −0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geqq$ 2.8V	–	–	50*2	µA
			–	–	10*3	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

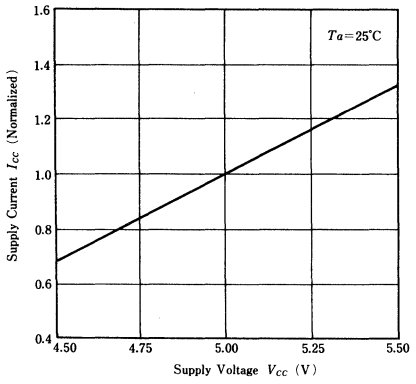
Note) *1. t_{RC} = Read Cycle Time
*2. This characteristic is guaranteed only for L-version, 20µA max. at T_a = 0 to 40°C.
*3. This characteristic is guaranteed only for L-SL version, 3µA max. at T_a = 0 to 40°C.

- **Low V_{CC} Data Retention Waveform**

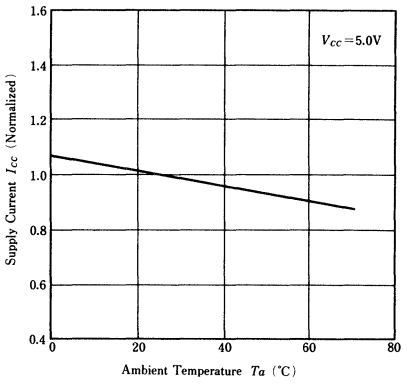


Note) In Data Retention Mode, $\overline{CS}$ controls the Address, $\overline{WE}$, $\overline{OE}$, and Din Buffers. *Vin* for these inputs can be in high impedance state in data retention mode.

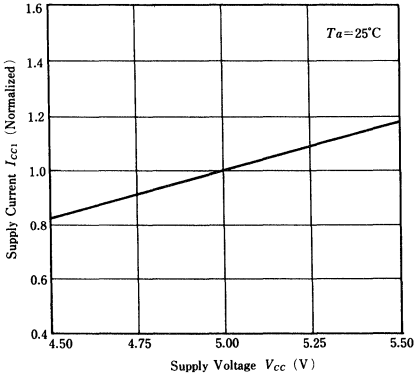
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1)



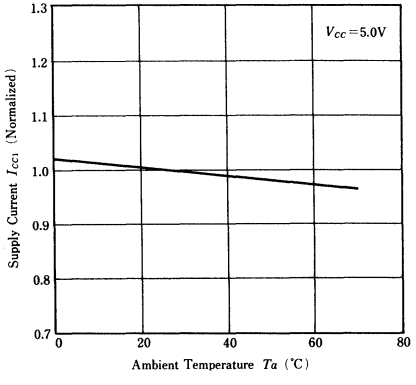
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (1)



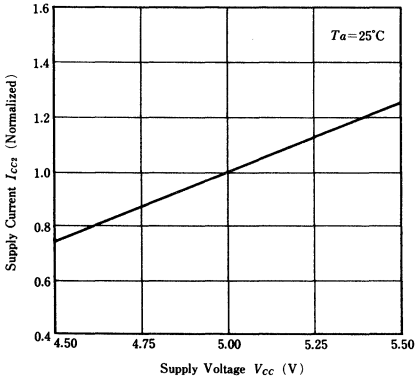
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2)



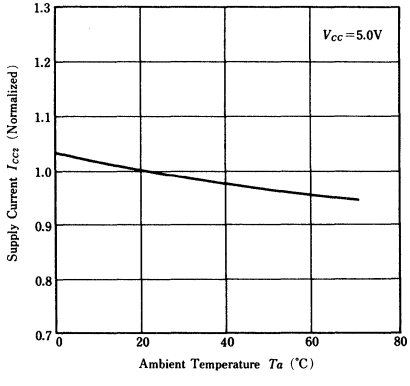
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (2)



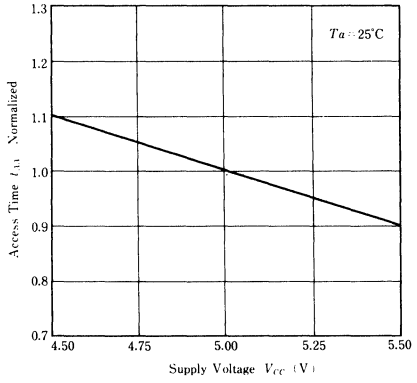
SUPPLY CURRENT vs. SUPPLY VOLTAGE (3)



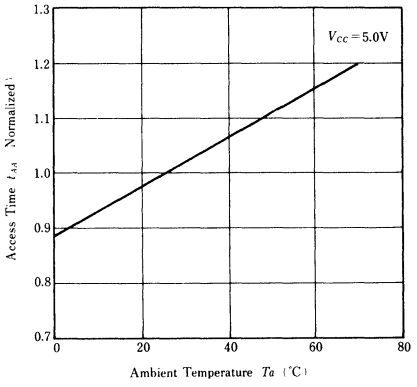
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (3)



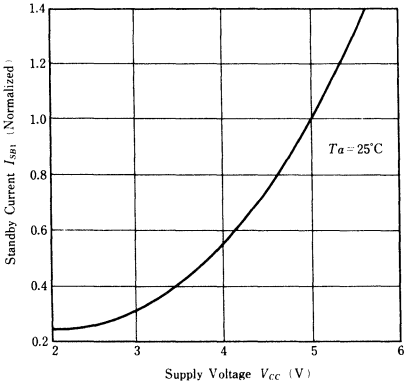
ACCESS TIME vs. SUPPLY VOLTAGE



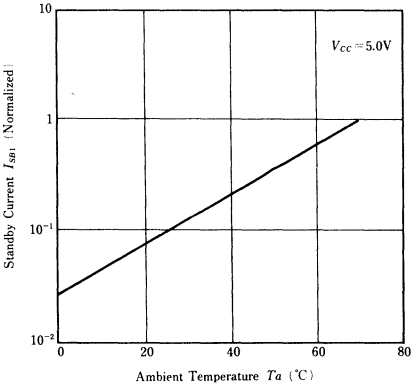
ACCESS TIME vs. AMBIENT TEMPERATURE



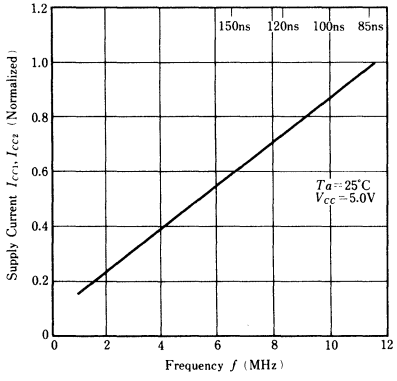
STANDBY CURRENT vs. SUPPLY VOLTAGE



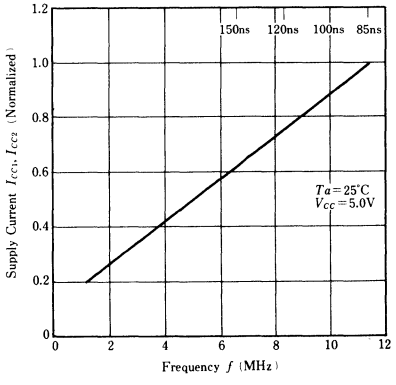
STANDBY CURRENT vs. AMBIENT TEMPERATURE



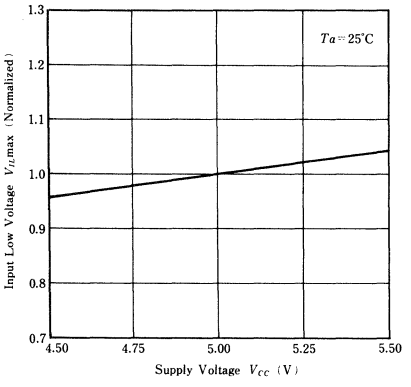
SUPPLY CURRENT vs. FREQUENCY (READ)



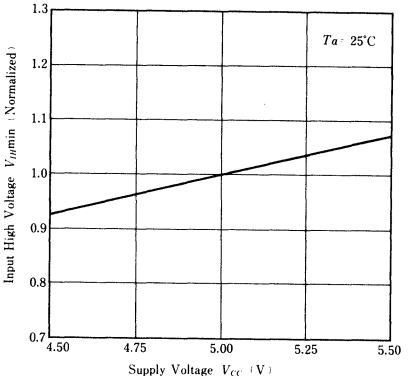
SUPPLY CURRENT vs. FREQUENCY (WRITE)



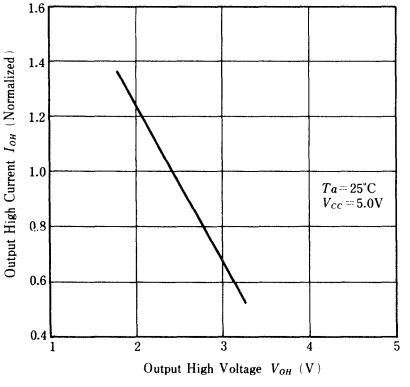
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



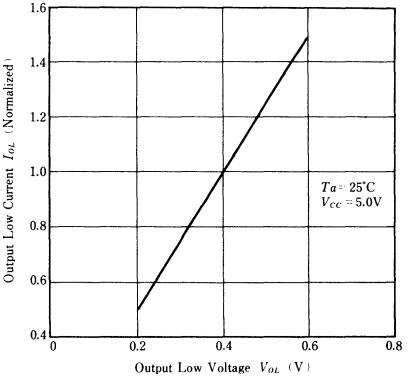
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



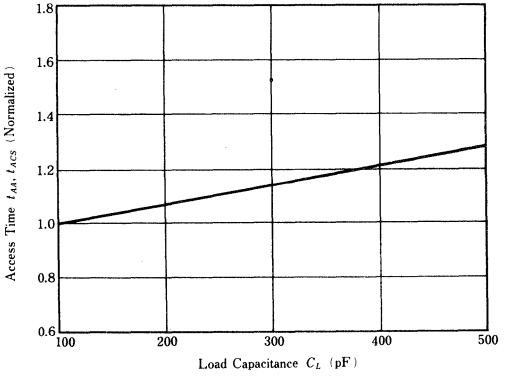
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME vs. LOAD CAPACITANCE



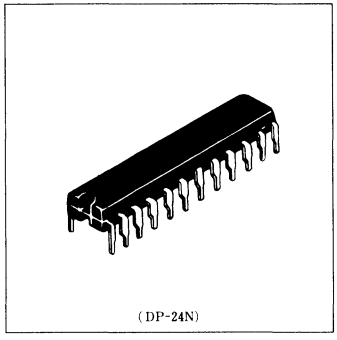
HM6208 Series

65536-word x 4-bit High Speed CMOS Static RAM

The Hitachi HM6208 is a high speed 256k static RAM organized as 64-k word × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6208, packaged in a 300 mil plastic DIP, is available for high density mounting. Low power version retains the data with battery back up.



(DP-24N)

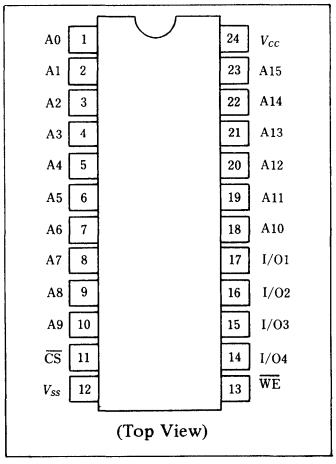
Features

- High Speed: Fast Access Time 35/45 ns (max.)
- Low Power
  - Standby: 100 μW (typ.)/10 μW (typ.) (L-version)
  - Operation: 300 mW (typ.)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static Memory:
  - No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6208P-35 HM6208P-45	35ns 45ns	300 mil 24 pin Plastic DIP
HM6208LP-35 HM6208LP-45	35ns 45ns	

Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

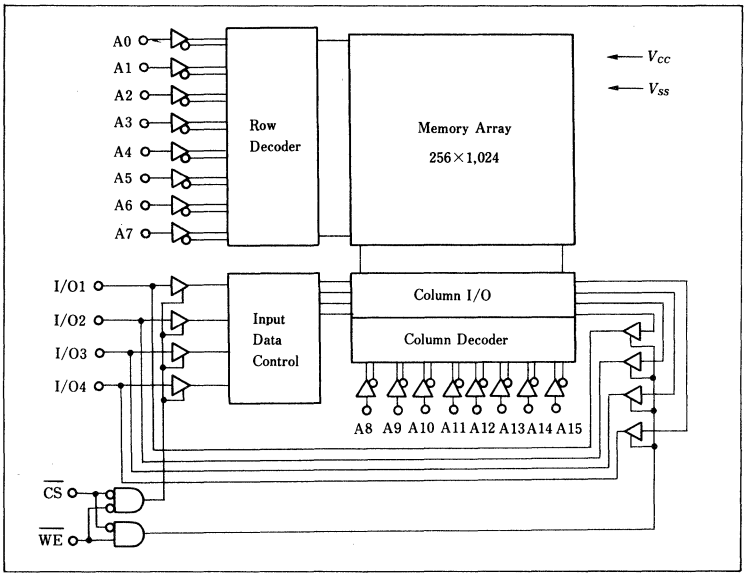
Note) *1. −3.5V for pulse width ≦ 10 ns

Pin Description

Pin Name	Function
A0 - A15	Address
I/O1 - I/O4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. Dept. regarding specifications.

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	NOT SELECTED	I_{SB}, I_{SB1}	HIGH Z	— — —
L	H	READ	I_{CC}	Dout	READ CYCLE
L	L	WRITE	I_{CC}	Din	WRITE CYCLE

Note) X means don't care.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 10 ns

DC and Operating Characteristics (Ta = 0 to +70°C, Vcc = 5V ± 10%, Vss = 0V)

Parameter	Symbol	min	typ*1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	2.0	μA	V_{CC} = MAX. V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	60	100	mA	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0mA
Standby Power Supply Current	I_{SB}	–	15	30	mA	$\overline{CS}$ = V_{IH}
Standby Power Supply Current (1)	I_{SB1}	–	0.02	2.0	mA	$\overline{CS}$ ≧ V_{CC}−0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V
		–	0.002*2	0.1*2		
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4.0mA

Note) *1. Typical limits are at V_{CC} = 5.0V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0MHz)

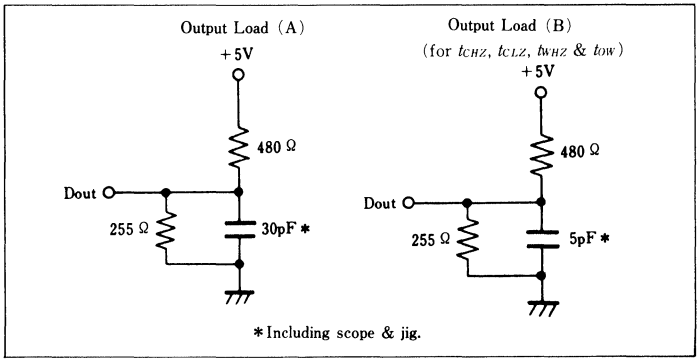
Parameter	Symbol	min	max	Unit	Conditions
Input Capacitance	C_{IN}	–	6	pF	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	10	pF	$V_{I/O}$=0V

Note) This parameter is sampled and not 100% tested.

AC characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

AC Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figure

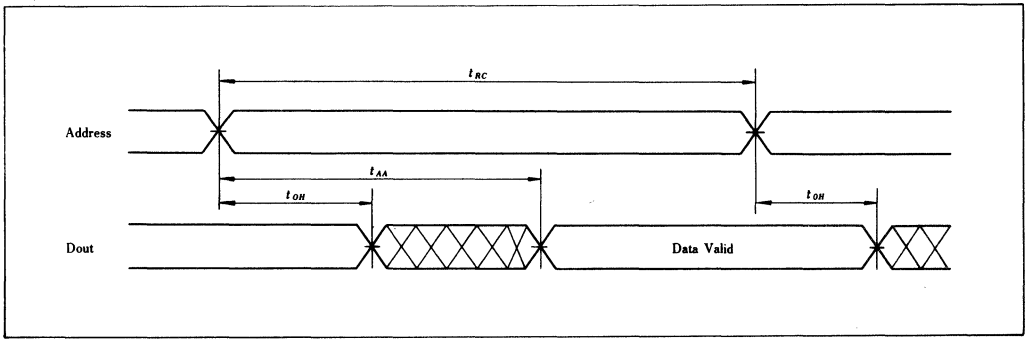


Read Cycle

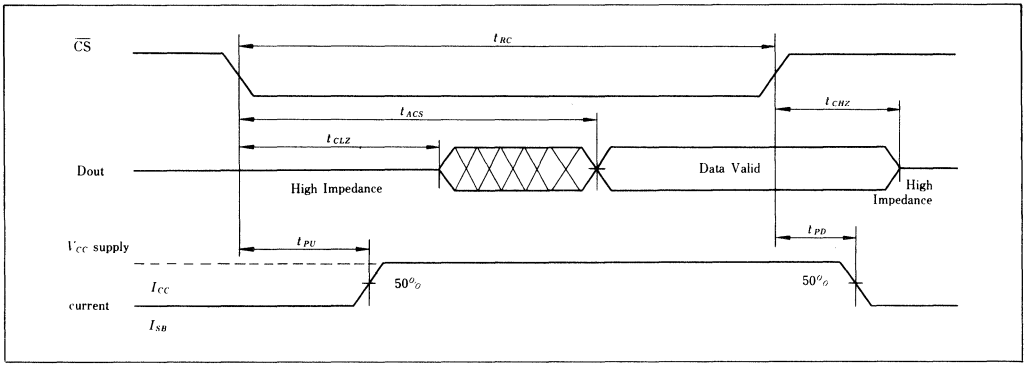
Parameter	Symbol	HM6208-35		HM6208-45		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

Note) *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Timing Waveform of Read Cycle No. 1 *1, *2



Timing Waveform of Read Cycle No. 2*1,*3



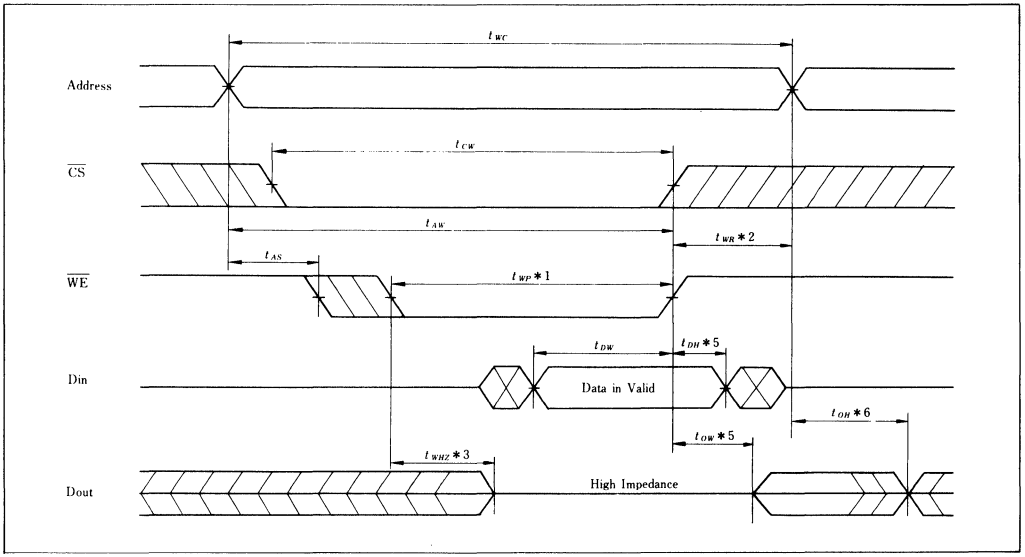
Note) *1. $\overline{WE}$ is High for Read Cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

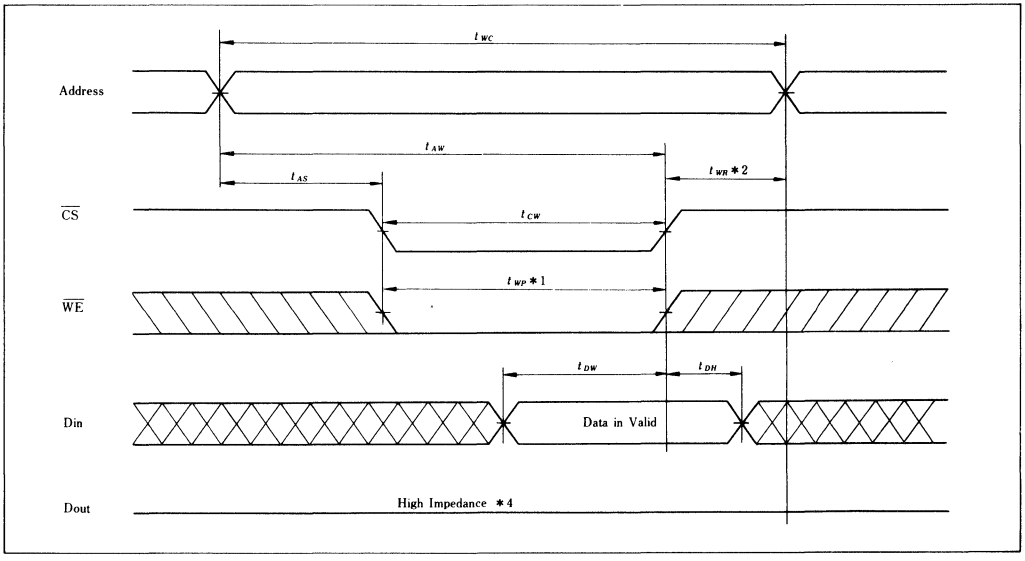
Parameter	Symbol	HM6208-35		HM6208-45		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width*1	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}*7	0	10	0	15	ns
Output Active from End of Write	t_{OW}*7	0	—	0	—	ns

Notes) *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state.
The input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle.
*7. Transition is measured ±200mV from steady state voltage with load (B). This parameter is sampled and not 100% tested.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

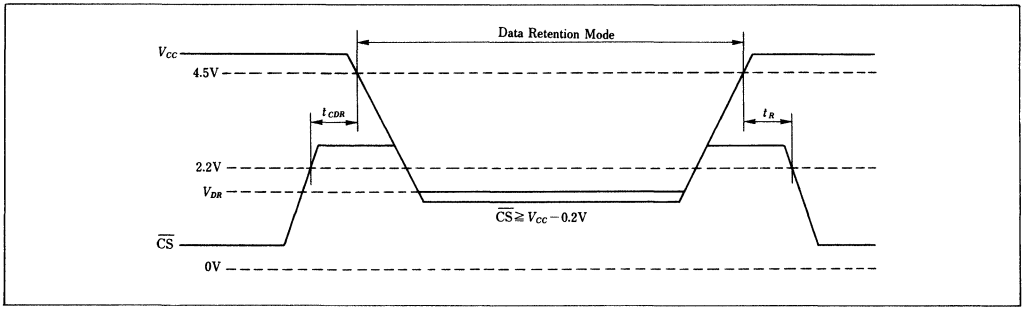
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	min	typ.	max.	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$, $Vin \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Data Retention Current	I_{CCDR}	–	1	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	
Operation Recovery Time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time *2. V_{CC}=3.0V

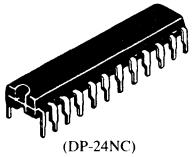
Low V_{CC} Data Retention Waveform



HM6708 Series — Preliminary

65536-word × 4-bit High Speed Static RAM

HM6708P Series



(DP-24NC)

HM6708JP Series

(CP-24D)

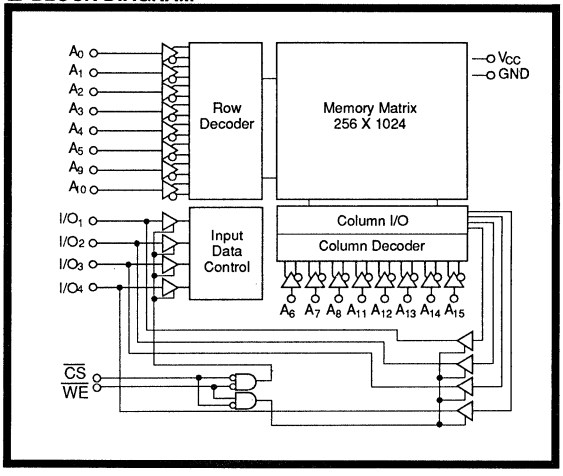
■ FEATURES

- Super fast access time: 20/25 ns (max.)
- Low power dissipation (DC) operating: 250 mW (typ.)
- +5V Single supply
- Completely static memory
  No clock or timing strobe required
- Balanced read and write cycle time
- Fully TTL compatible input and output

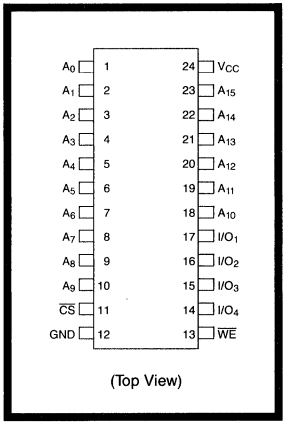
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6708P-20	20ns	300 mil 24 pin Plastic DIP
HM6708P-25	25ns	
HM6708JP-20	20ns	
HM6708JP-25	25ns	

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to GND Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg\ (bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input High (logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

*Pulse width ≤ 20 ns, DC: -0.5V

■ TRUTH TABLE

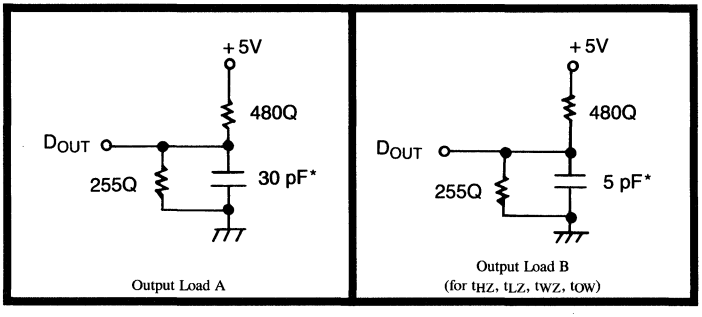
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	D_{OUT}	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	D_{IN}	Write Cycle (1), (2)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, GND = 0V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}$ = 0 mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} -0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} -0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	mA
Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4	—	—	V

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input timing reference levels: 1.5V
Output load: See figure
Input rise and fall times: 4 ns
Output reference levels: 1.5V



*including scope and jig capacitance

■ CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	20	—	25	ns	—
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	0	—	0	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	10	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	15	—	20	—	ns	—
Address Valid to End of Write	t_{AW}	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	3	—	3	—	ns	—
Data Valid to End of Write	t_{DW}	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	ns	2, 3

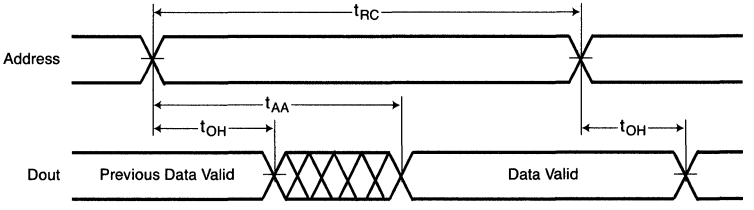
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

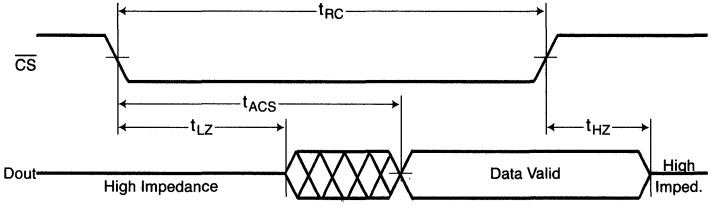
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1)[1] [2]



• Read Cycle (2)[1] [3]

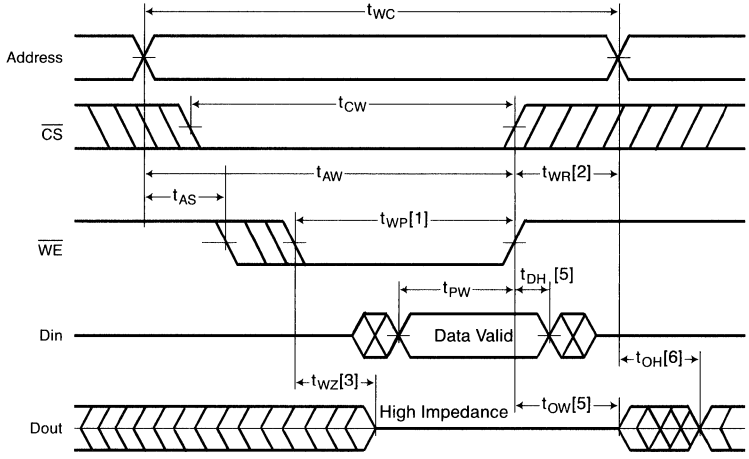


NOTES: 1. $\overline{WE}$ is high for read cycle.

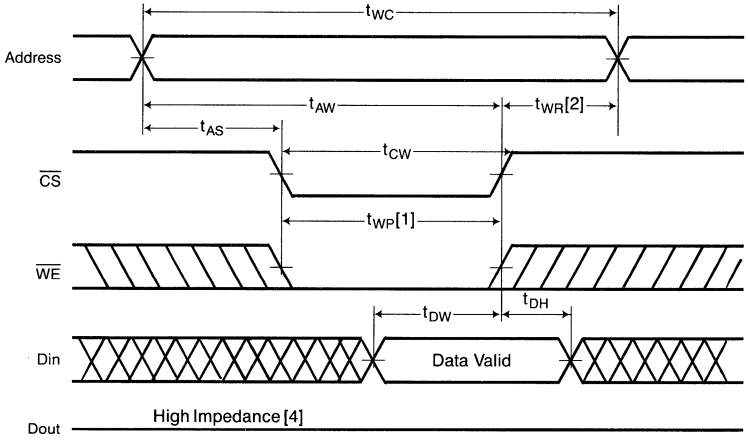
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

3. Address valid prior to or coincident with $\overline{CS}$ transition low.

- **Write Cycle (1) ($\overline{WE}$ Controlled)**



- **Write Cycle (2) ($\overline{CS}$ Controlled)**



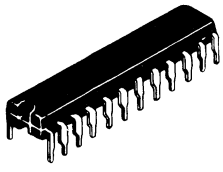
NOTES:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Output data is the same phase of write data of this write cycle.

HM6207 Series

262144-word x 1-bit High Speed CMOS Static RAM

The Hitachi HM6207 is a high speed 256k static RAM organized as 256-k word × 1-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6207, packaged in a 300 mil plastic DIP, is available for high density mounting.

Low power version retains the data with battery back up.



DP-24N

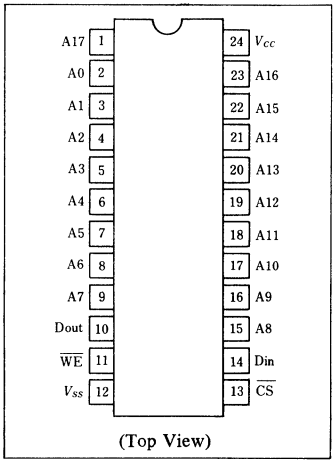
Features

- High Speed: Fast Access Time 35/45 ns (max.)
- Low Power
  - Standby: 100 μW (typ.)/10 μW (typ.) (L-version)
  - Operation: 300 mW (typ.)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static Memory:
  - No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6207P-35	35ns	300 mil 24 pin Plastic DIP
HM6207P-45	45ns	
HM6207LP-35	35ns	
HM6207LP-45	45ns	

Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

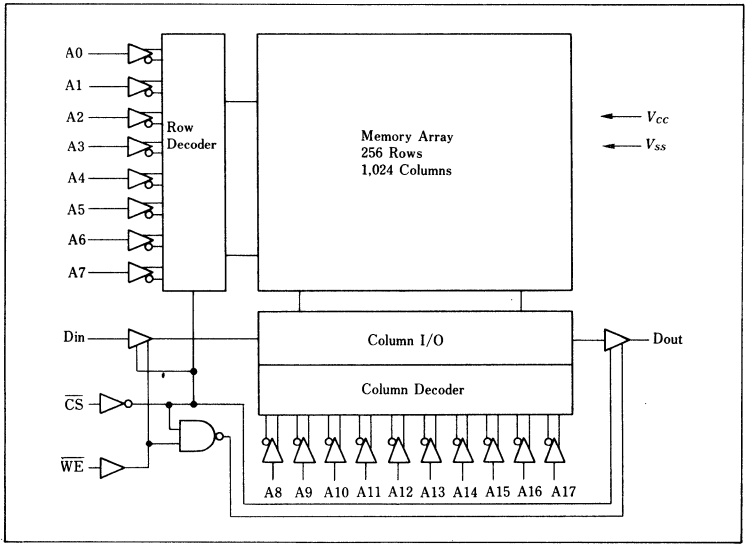
Note) *1. −3.5V for pulse width ≦ 10ns.

Pin Description

Pin Name	Function
A0 - A17	Address
Din	Data Input
Dout	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	NOT SELECTED	I_{SB}, I_{SB1}	HIGH Z	---
L	H	READ	I_{CC}	Dout	READ CYCLE
L	L	WRITE	I_{CC}	Din	WRITE CYCLE

Note) X means don't care.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 10 ns

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	min	typ*1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	2.0	μA	V_{CC} = MAX. V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10.0	μA	$\overline{CS}$ = V_{IH} Vout = V_{SS} to V_{CC}
Operating Power Supply Current: DC	I_{CC}	–	60	TBD	mA	$\overline{CS}$ = V_{IL} Iout = 0mA
Standby Power Supply Current: DC	I_{SB}	–	15	TBD	mA	$\overline{CS}$ = V_{IH}
Standby Power Supply Current (1): DC	I_{SB1}	–	0.02	2.0	mA	$\overline{CS}$ ≧ V_{CC}−0.2V, V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V
		–	0.002*2	0.1*2		
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4.0mA

Note) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0MHz)

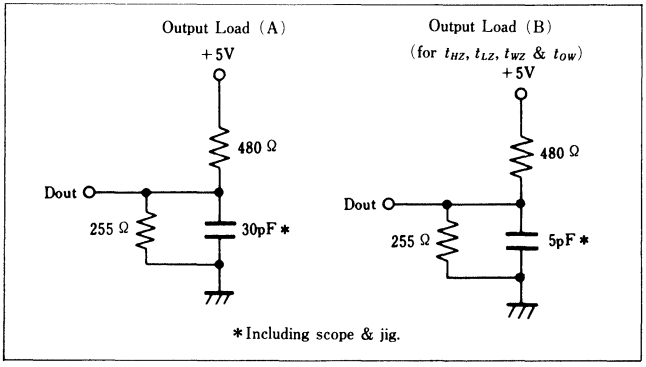
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance	Cin	–	–	6.0	pF	Vin = 0V
Input/Output Capacitance	Cout	–	–	10	pF	Vout = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

AC Test Conditions

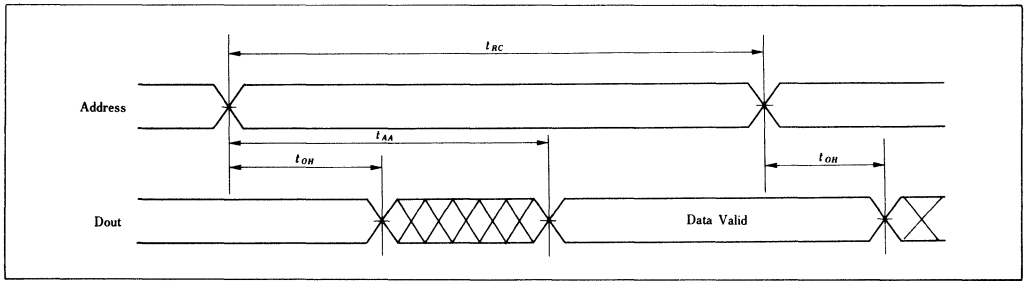
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figures.



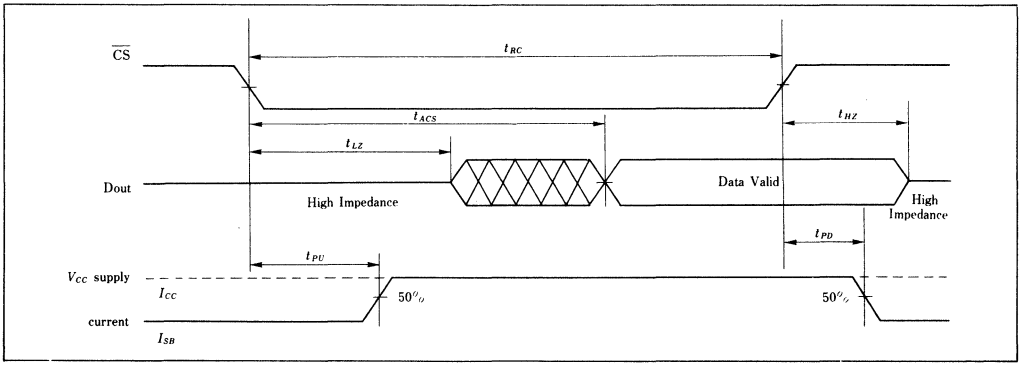
Read Cycle

Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	ns	*1
Address Access Time	t_{AA}	—	35	—	45	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	*2, *3, *7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	*2, *3, *7
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	*7
Chip Deselection to Power Down Time	t_{PD}	—	30	—	40	ns	*7

Timing Waveform of Read Cycle No. 1 *4, *5



Timing Waveform of Read Cycle No. 2*4, *6



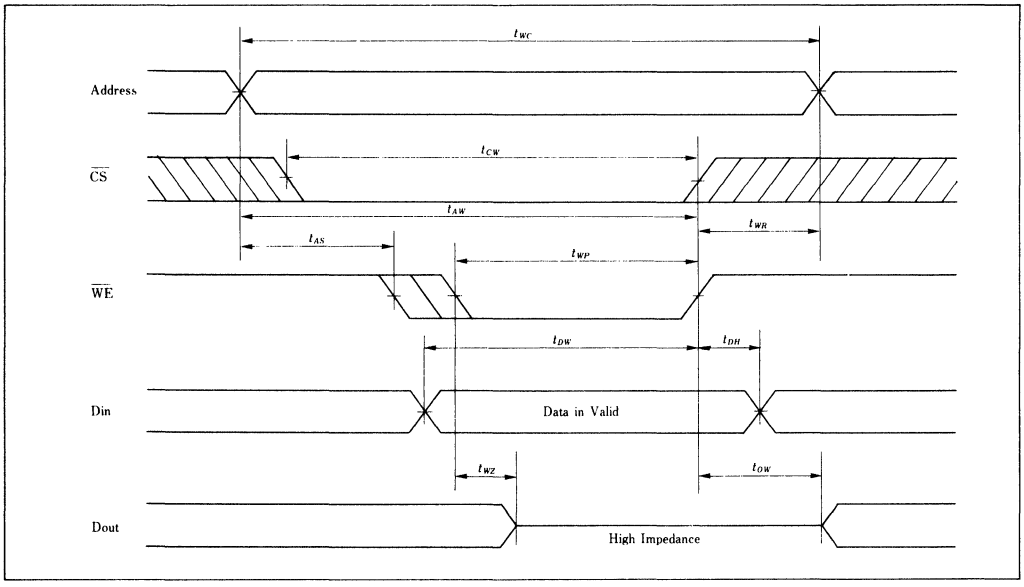
Notes) *1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
*2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. $\overline{WE}$ is high for READ Cycle.
*5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
*6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
*7. This parameter is sampled and not 100% tested.

Write Cycle

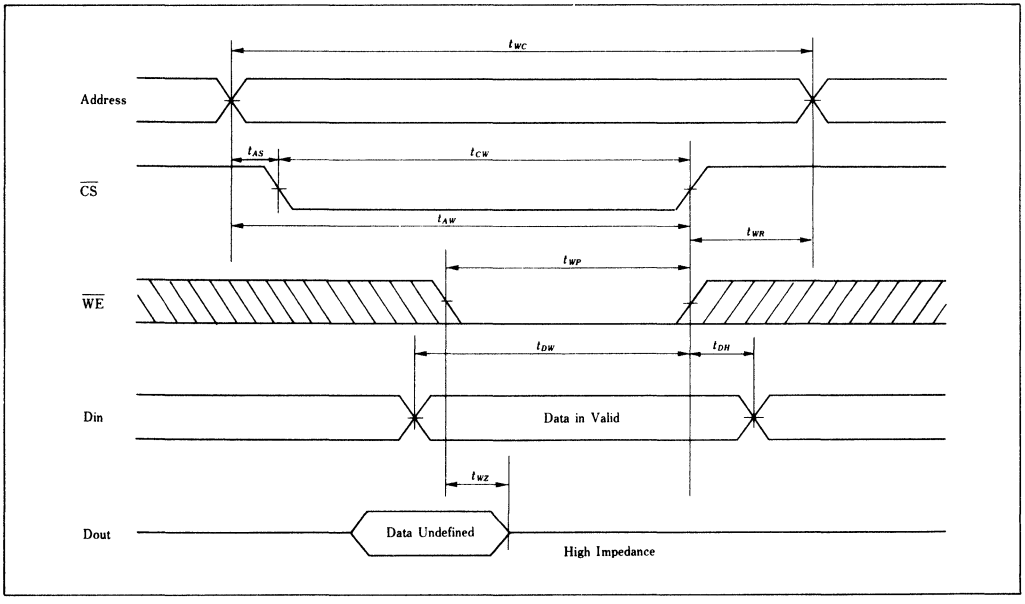
Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	ns	*2
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns	
Address Valid to End of Write	t_{AW}	30	—	40	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	25	—	25	—	ns	
Write Recovery Time	t_{WR}	TBD	—	TBD	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	ns	*3, *4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	*3, *4

Notes) *1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
*2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. This parameter is sampled and not 100% tested.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)

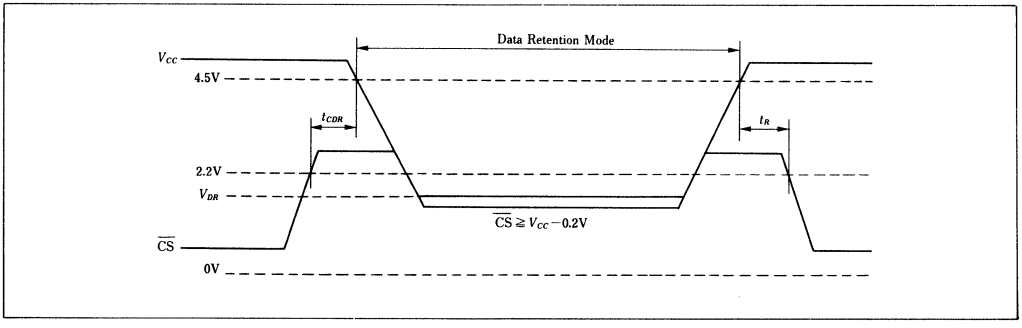


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)
(This characteristics is guaranteed only for L-version)

Parameter	Symbol	min	typ.	max.	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Data Retention Current	I_{CCDR}	–	1	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	
Operation Recovery Time	t_R	t_{RC}*1	–	–	ns	

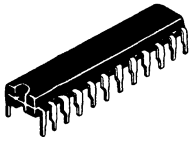
Note) *1. t_{RC} = Read Cycle Time *2. V_{CC} = 3.0V

Low V_{CC} Data Retention Waveform



262144-word × 1-bit High Speed Static RAM

HM6707P Series



(DP-24NC)

HM6707JP Series

(CP-24D)

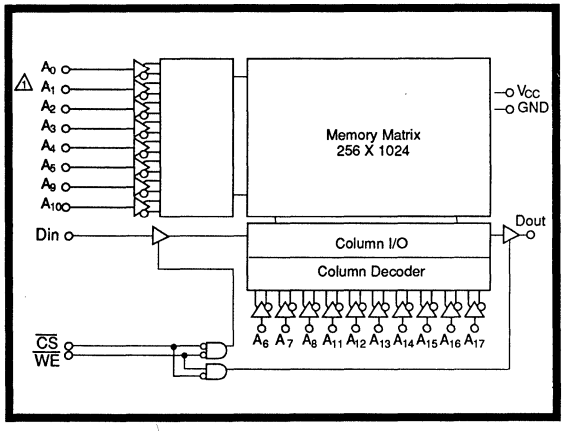
■ FEATURES

- Super fast access time: 20/25 ns (max.)
- Low power dissipation (DC) operating: 175 mW (typ.)
- +5V Single supply
- Completely static memory
  No clock or timing strobe required
- Balanced read and write cycle time
- Fully TTL compatible input and output
- Skinny 24 pin DIL plastic package (300 mil) and 24 pin SOJ (300 mil)

■ ORDERING INFORMATION

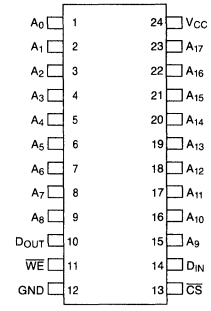
Type No.	Access Time	Package
HM6707P-20	20ns	300 mil 24 pin Plastic DIP
HM6707P-25	25ns	
HM6707JP-20	20ns	
HM6707JP-25	25ns	

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

(24 pin DILP)



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to GND Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg\ (bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-3.0*	—	0.8	V

*Pulse width 20 ns, DC: -0.5V

■ TRUTH TABLE

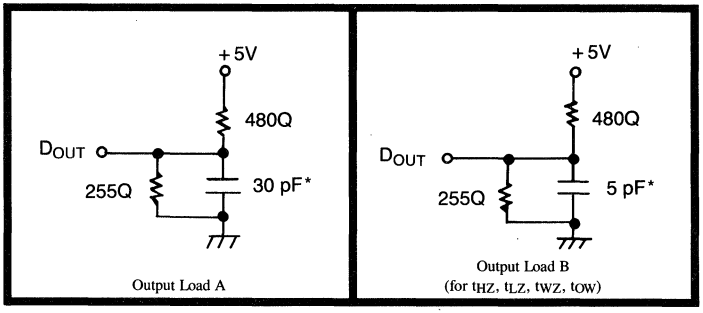
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	D_{OUT}
L	L	Write	I_{CC}, I_{CC1}	High Z

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $70°C$, GND = 0V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = 0V$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$, $V_{OUT} = 0V$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{OUT} = 0$ mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{OUT} = 0$ mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8$ mA	—	—	0.4	mA
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4	—	—	V

■ AC TEST CONDITIONS

Input pulse levels:	GND to 3.0V
Input timing reference levels:	1.5V
Output load:	See figure
Input rise and fall times:	4 ns
Output reference levels:	1.5V



*including scope and jig capacitance

■ CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	$C_{I/O}$	10.0	pF	V_{OUT} = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6707-20		HM6707-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	20	—	25	ns	—
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	15	—	20	—	ns	—
Address Valid to End of Write	t_{AW}	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	3	—	3	—	ns	—
Data Valid to End of Write	t_{DW}	15	—	20	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	ns	2, 3

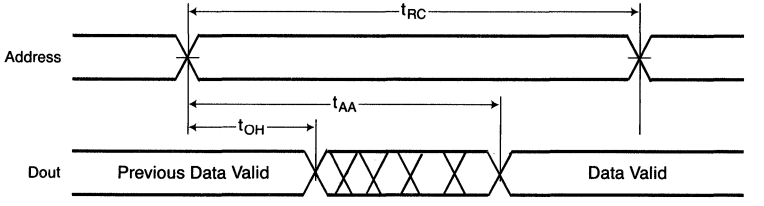
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

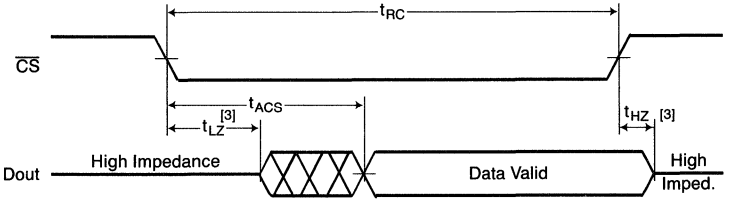
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1)[1]



• Read Cycle (2)[2]

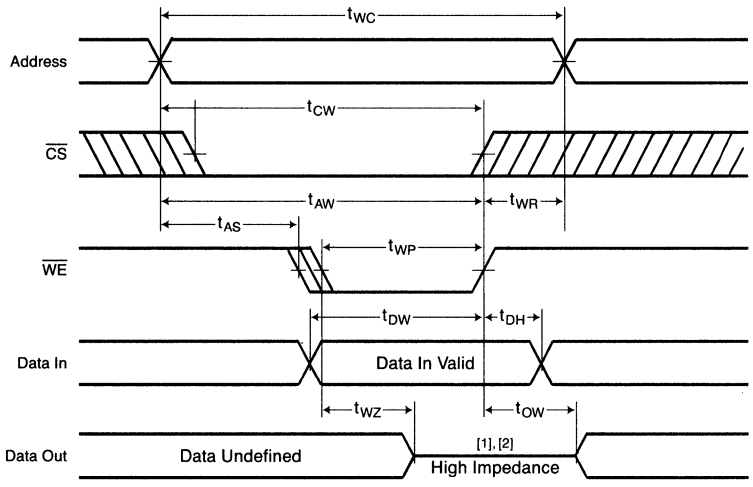


NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for read cycle.

2. Address valid prior to or coincident with $\overline{CS}$ transition low.

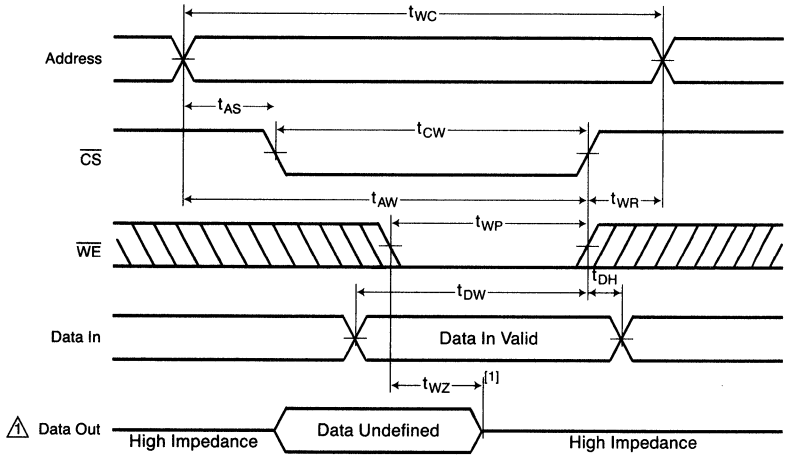
3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

• Write Cycle (1) ($\overline{WE}$ Controlled)



NOTE: 1. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.

• Write Cycle (2) ($\overline{CS}$ Controlled)



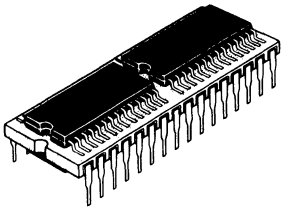
NOTES: 1. Transition is measured ± 200 mV from steady state voltage with specified loading in Load B.
2. If the $\overline{CS}$ goes simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

HM66203 Series — Maintenance Only

131072-word x 8-bit High Density Static RAM Module

Features

- High Density Industry Standard 32 Pin DIP Mounting 4pcs of 256k Static RAM (SOP).
- Single +5V Supply.
- High speed: Fast Access Time 100/120/150ns max.
- Equal Access and Cycle Time.
- Completely Static RAM: No Clock or Timing Strobe Required.
- Low Power
  - Standby: 40μW typ. (L-version)
  - Operation: 50mW typ. (f = 1MHz)
- Capability of Battery Back-up Operation (L-version).
- Common Data Input and Output, Three State Outputs.
- Directly TTL Compatible: All Inputs and Outputs.

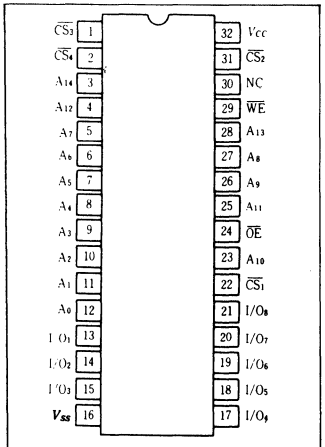


(DM-32)

Ordering Information

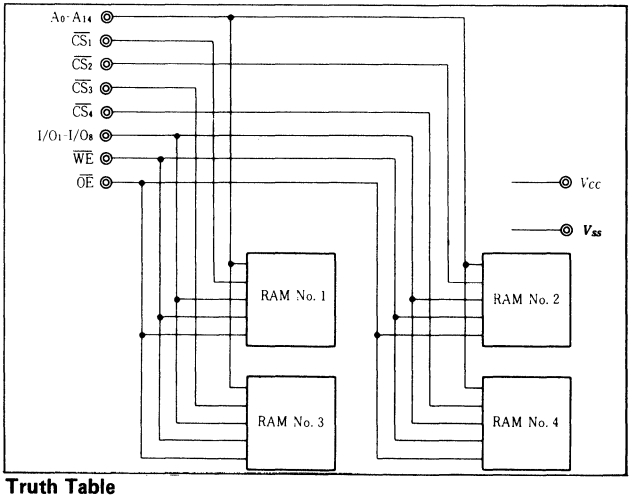
Type No.	Access Time	Package
HM66203-10	100ns	600 mil 32 pin DIP
HM66203-12	120ns	
HM66203-15	150ns	
HM66203L-10	100ns	
HM66203L-12	120ns	
HM66203L-15	150ns	

Pin Arrangement



(Top View)

Functional Block Diagram



Truth Table

Mode	$\overline{CSi}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not Selected (Power Down)	H*1	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L*2	H	L	D_{out}	I_{CC}	Read Cycle (1) to (3)
Write	L*2	L	H	D_{in}	I_{CC}	Write Cycle (1)
	L*2	L	L	D_{in}	I_{CC}	Write Cycle (2)

Note) *1. X: Don't Care (H or L); i = 1, 2, 3, 4 All chips are not selected.
*2. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding.
Only one chip should be selected.
Two or more chips must not be selected at one time.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.0V for pulse width ≦ 50ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	min.	typ. *1	max.	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	$V_{IN} = V_{SS}$ to V_{CC}	–	–	2	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CSn} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	–	–	2	μA	*2
Operating Power Supply Current: DC	I_{CC}	$\overline{CSN} = V_{IL}$ $I_{I/O}$ = 0mA	–	10	25	mA	*3
Average Operating Power Supply Current (1)	I_{CC1}	MIN. cycle	–	42	80	mA	HM66203/L −10
		duty = 100%	–	37	80		HM66203/L −12
		$I_{I/O}$ = 0mA	–	35	80		HM66203/L −15
Average Operating Power Supply Current (2)	I_{CC2}	$\overline{CSN} = V_{IL}$ $V_{IH} = V_{CC}$ V_{IL} = 0V $I_{I/O}$ = 0mA f = 1MHz	–	10	15	mA	*3
Standby Power Supply Current: DC	I_{SB}	$\overline{CSn} = V_{IH}$	–	2	12	mA	*2
Standby Power Supply Current (1): DC	I_{SB1}	$\overline{CSn} \geqq V_{CC} - 0.2V$	–	8	400	μA	HM66203L Series
			–	0.16	8	mA	HM66203 Series
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V	
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V	

Note) *1. Typical values are at V_{CC} = 5.0V, T_a = +25°C and specified loading.
*2. $\overline{CSn}$; All chips are not selected.
*3. $\overline{CSN}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	45	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	–	50	pF

Note) This parameter is sampled and not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

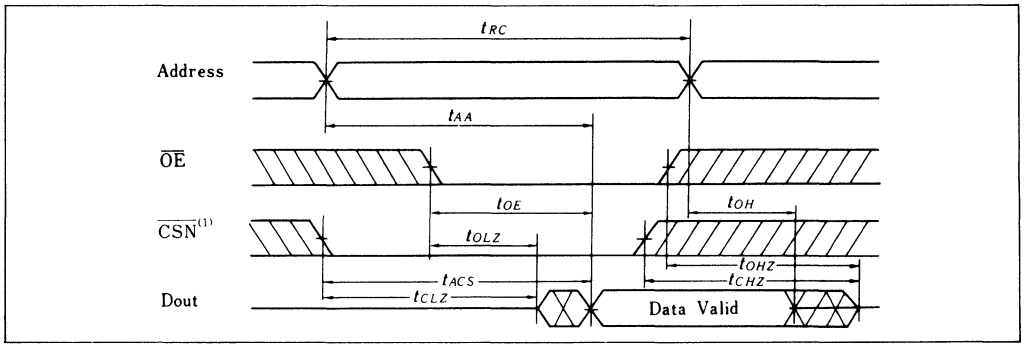
AC Test Conditions

- Input pulse levels . . . . . 0.8V to 2.4V
- Input rise and fall times 5ns
- Input and Output timing reference level 1.5V
- Output load . . . . . 1 TTL Gate and C_L (100pF) (Including scope & jig)

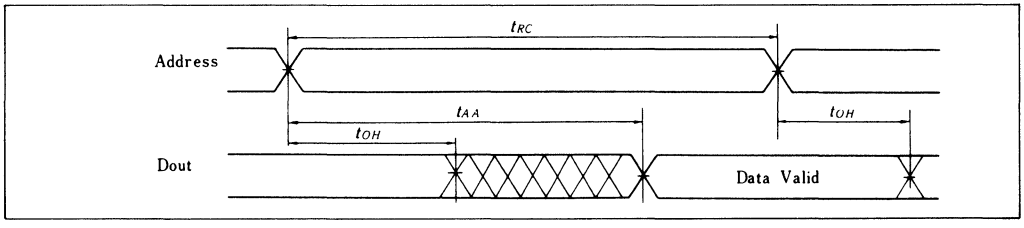
Read Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns

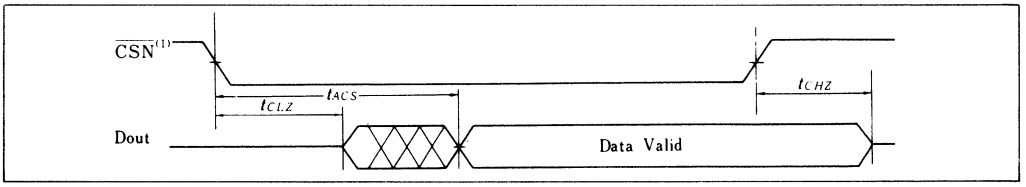
Timing Waveform of Read Cycle No. 1 *2



Timing Waveform of Read Cycle No. 2 *1,*2,*3,*5



Timing Waveform of Read Cycle No. 3 *2,*4,*5

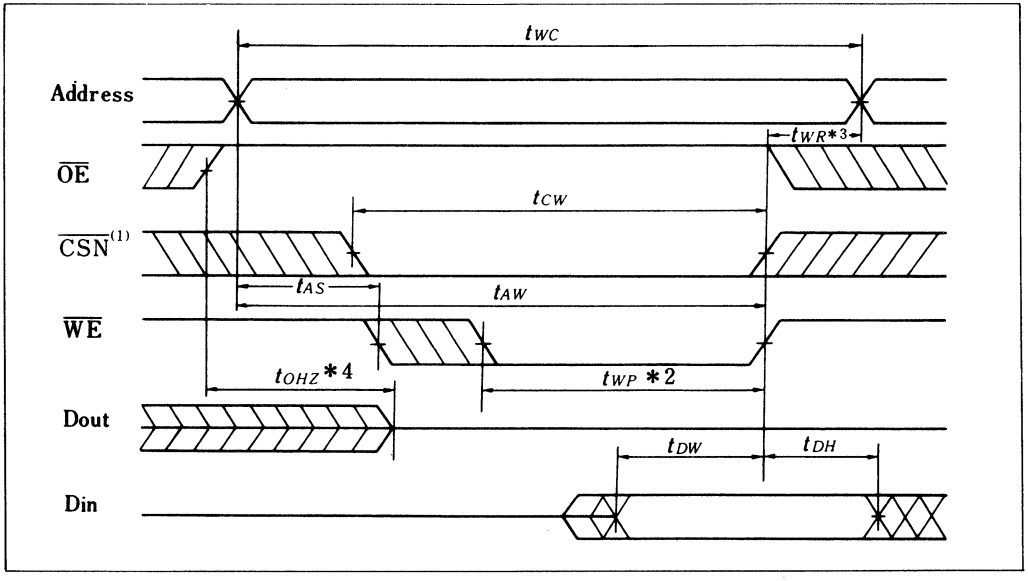


Note) *1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CSN} = V_{IL}$.
*4. Address should be valid prior to or coincident with $\overline{CSN}$ transition low.
*5. $\overline{OE} = V_{IL}$

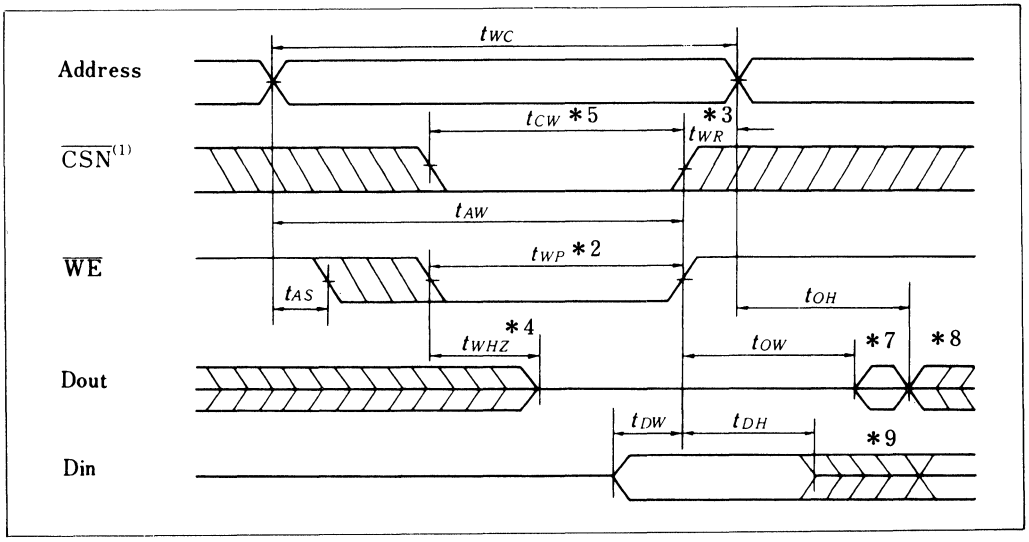
Write Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	90	–	100	–	120	–	ns
Address Valid to End of Write	t_{AW}	90	–	100	–	120	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	75	–	90	–	110	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

Timing Waveform of Write Cycle (1) ($\overline{OE}$ Clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ Low Fixed)*6



Notes)
*1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. A write occurs during the overlap (t_{WP}) of a low $\overline{CSN}$ and a low $\overline{WE}$.
*3. t_{WR} is measured from the earlier of $\overline{CSN}$ or $\overline{WE}$ going high to the end or write cycle.
*4. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
*5. If the $\overline{CSN}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
*6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*7. Dout should be held in phase of the written data during this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CSN}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

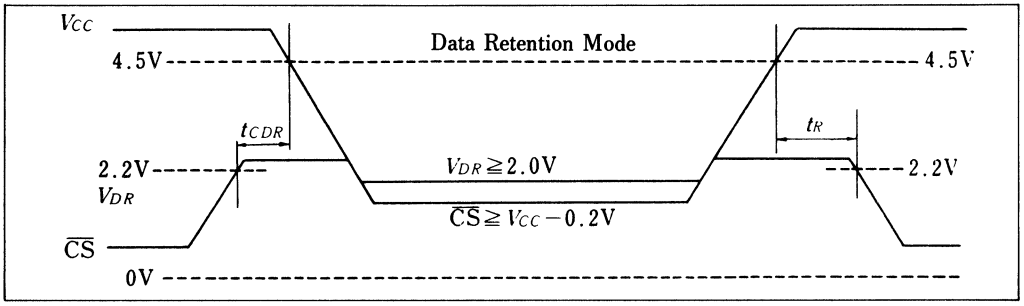
Low V_{CC} Data Retention Characteristics (T_a = 0°C to +70°C)

(Data retention characteristics is guaranteed only for HM66203L Series.)

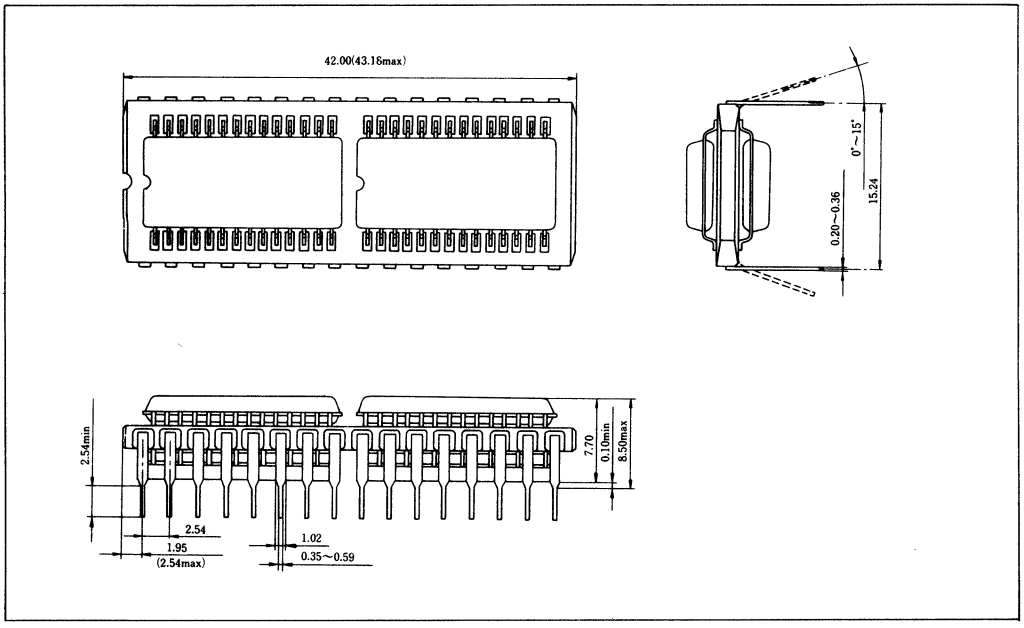
Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CSn} \geqq V_{CC} - 0.2V$
Data Retention Current	I_{CCDR}	–	–	200	μA	V_{CC} = 3.0V $\overline{CSn} \geqq 2.8V$*2
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See Retention Waveform
Operation Recovery Time	t_R	[1] t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.
*2. $\overline{CSn}$: All chips are not selected.

Low V_{CC} Data Retention Waveform



Package Outline (Unit: mm)



HM66204 Series

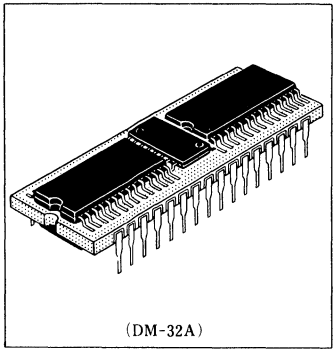
131072-word x 8-bit High Density Static RAM Module

The HM66204 is a high density 1 M-bit static RAM module consisted of 4 pieces of HM62256FP/LFP products (SOP type 256k static RAM) and a HD74HC138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66204 is the standard 600 mil width 32 pin dual-in-line package. Its pin arrangement is completely compatible with 1 M-bit monolithic static RAM.

The HM66204 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66204 makes high density mounting possible with no surface mount technology.

These features make the HM66204 ideally suited for high density compacted memory systems.

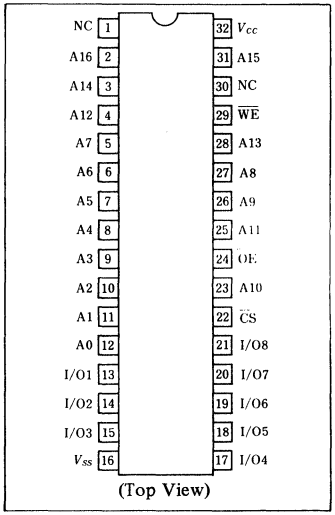


(DM-32A)

Features

- High density 32 pin DIP
  - Mounting 4 pcs. of 256k static RAM (SOP; HM62256FP/LFP) and CMOS decoder logic (SOP; HD74HC138FP equivalent)
- Pin compatible with 1M monolithic static RAM
- High speed
  - Fast access time 120 ns/150 ns (maximum)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby 40 μW (typical) (L-version)
  - Operation 50 mW (typical) (f = 1 MHz)
- Common data input and output, three state outputs
- Capable of battery backup operation (L-version)

Pin Arrangement



(Top View)

Ordering Information

Part No.	Access Time	Package
HM66204-12	120 ns	600 mil 32-pin DIP
HM66204-15	150 ns	
HM66204L-12	120 ns	
HM66204L-15	150 ns	

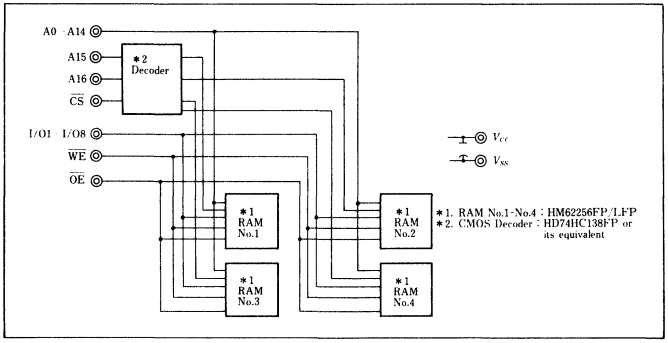
Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C
Power dissipation	P_T	1.0	W

Pin Description

Pin Name	Function
A0 - A16	Address
I/O1 - I/O8	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Mode Selection

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not selected (Power down)	H	X	X	High-Z	I_{BS}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note) X = Don't care (H or L)

Electrical Characteristics

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) Voltage	V_{IH}	3.85	–	6.0	V	A15, A16, $\overline{CS}$
		2.2	–	6.0	V	Others except A15, A16, $\overline{CS}$
Input low (logic 0) Voltage	V_{IL}	–0.5	–	0.8	V	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions	Notes
Input leakage current	$\|I_{LI}\|$	–	–	2	μA	$V_{IN} = V_{SS}$ to V_{CC}	
Output leakage current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	
Operating power supply current: DC	I_{CC}	–	10	25	mA	$\overline{CS} = V_{IL}$ $I_{I/O}$ = 0mA	
Average operating power supply current (1)	I_{CC1}	–	37	80	mA	MIN. cycle duty = 100%	–12
		–	35	80		$I_{I/O}$ = 0mA	–15
Average operating power supply current (2)	I_{CC2}	–	10	15	mA	$\overline{CS} = V_{IL}$, $V_{IH} = V_{CC}$ V_{IL} = 0V, $I_{I/O}$ = 0mA f = 1MHz	
Standby power supply current: DC	I_{SB}	–	2	12	mA	$\overline{CS} = V_{IH}$	
Standby power supply current (1): DC	I_{SB1}	–	8	400	μA	$\overline{CS} \geq V_{CC}-0.2V$ A15, A16 $\geq V_{CC}-0.2V$	HM66204L Series
		–	0.16	8	mA	or A15, A16 $\leq$ 0.2V	
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 2.1 mA	
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = –1.0 mA	

Note) *1. Typical values are at V_{CC} = 5.0V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	–	45	pF	Vin = 0V
Input/output capacitance	$C_{I/O}$	–	–	50	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

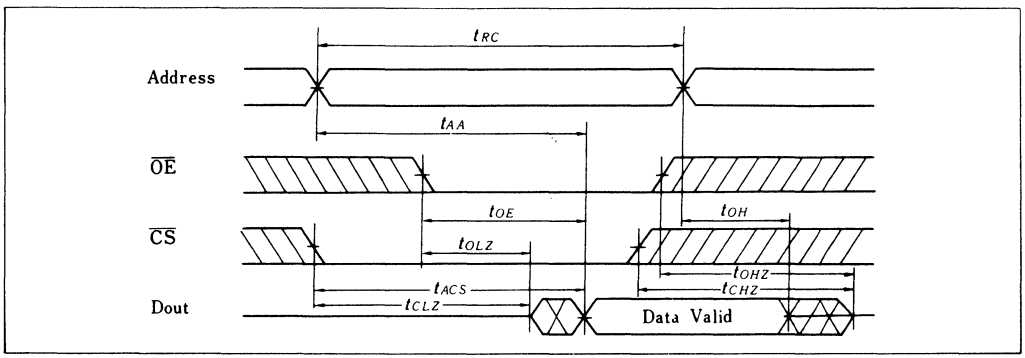
AC Test Conditions

- Input pulse levels:
  0.8V to 4.0V . . . $\overline{CS}$, A15, A16
  0.8V to 2.4V . . . Other pin except $\overline{CS}$, A15, A16
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5V
- Output load: 1 TTL Gate and C_L (100pF) (Including scope & jig)

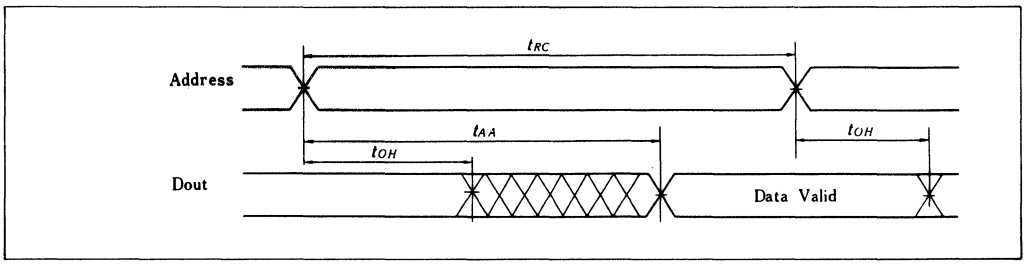
Read Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Read cycle time	t_{RC}	120	–	150	–	ns
Address access time	t_{AA}	–	120	–	150	ns
Chip select access time	t_{ACS}	–	120	–	150	ns
Output enable to output valid	t_{OE}	–	60	–	70	ns
Output hold from address change	t_{OH}	10	–	10	–	ns
Chip selection to output in low Z	t_{CLZ}	10	–	10	–	ns
Output enable to output in low Z	t_{OLZ}	5	–	5	–	ns
Chip deselection to output in high Z	t_{CHZ}	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns

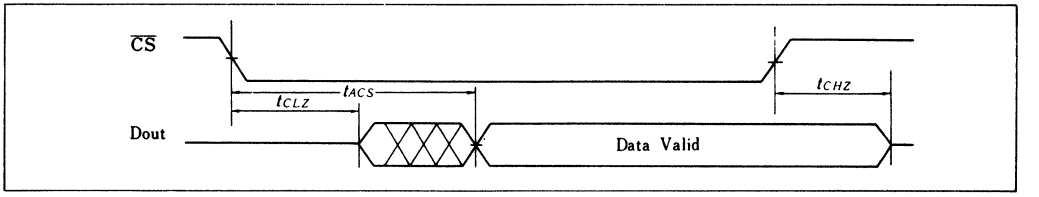
Read Cycle Timing No. 1 *1



Read Cycle Timing No. 2 *1,*2,*4



Read Cycle Timing No. 3 *1, *3, *4

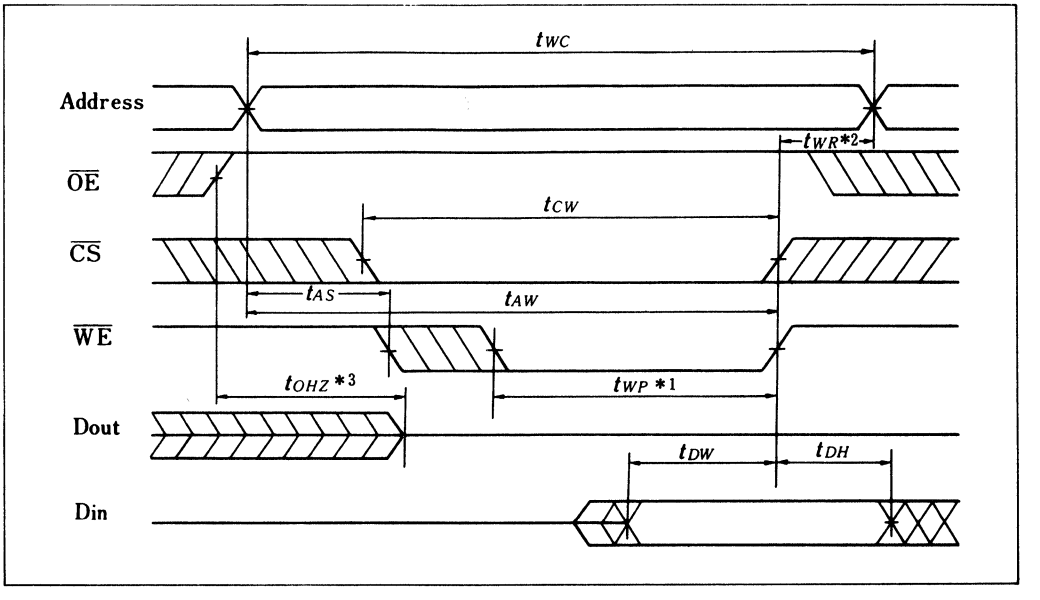


Notes) *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

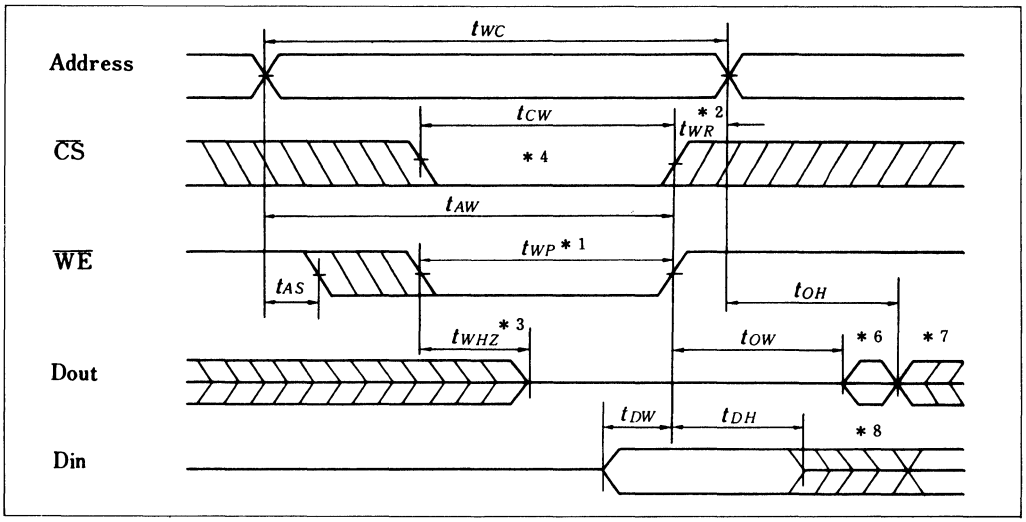
Write Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Write cycle time	t_{WC}	120	–	150	–	ns
Chip selection to end of write	t_{CW}	100	–	120	–	ns
Address valid to end of write	t_{AW}	100	–	120	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	90	–	110	–	ns
Write recovery time	t_{WR}	5	–	5	–	ns
Write to output in high Z	t_{WHZ}	0	40	0	50	ns
Data to write time overlap	t_{DW}	50	–	60	–	ns
Data hold from write time	t_{DH}	0	–	0	–	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns
Output active from end of write	t_{OW}	5	–	5	–	ns

Write Cycle Timing No. 1 ($\overline{OE}$ Clock)



Write Cycle Timing No. 2*5 ($\overline{OE}$ Low Fixed)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state.
The input signals out of phase must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*6. D_{out} should be held in phase of the written data during this write cycle.
*7. D_{out} is the read data of next address.
*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

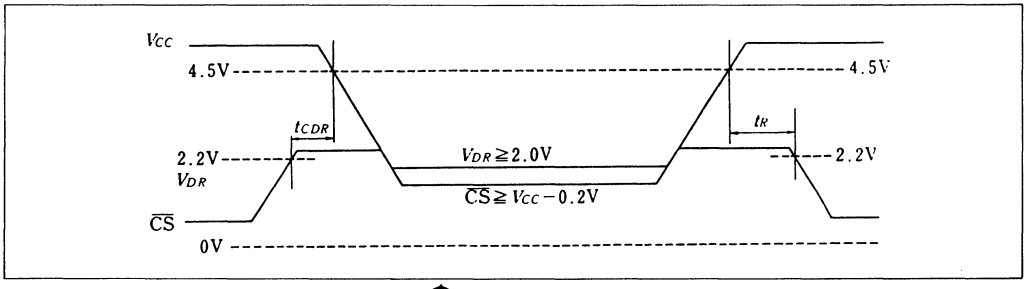
Low V_{CC} Data Retention Characteristics (Ta = 0°C to +70°C)

Data retention characteristics is guaranteed only for L version.

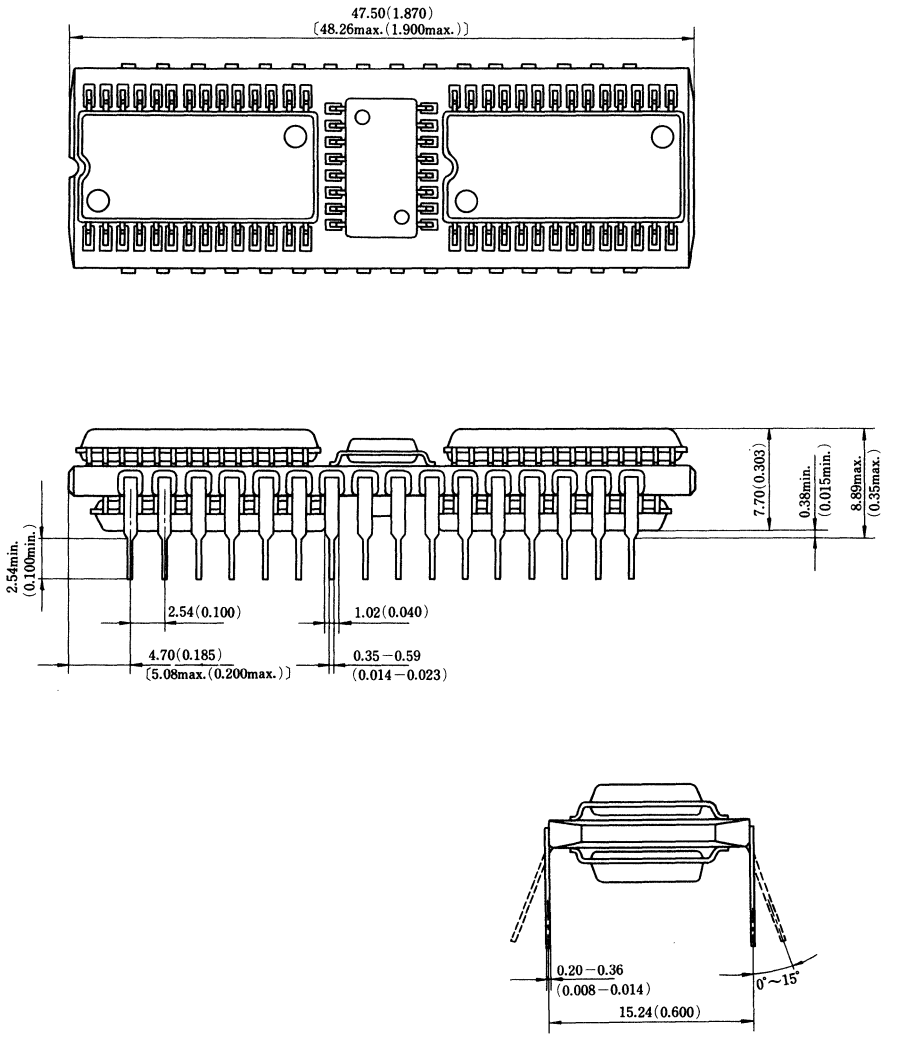
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC}$ -0.2V A15, A16 $\geq V_{CC}$ -0.2V or A15, A16 $\leq$ 0.2V
Data retention current	I_{CCDR}	–	–	200	µA	V_{CC} = 3.0V, $\overline{CS} \geq$ 2.8V A15, A16 $\geq$ 2.8V or A15, A16 $\leq$ 0.2V
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Package Dimensions; Unit: mm (inch)



HM628128 Series

■ DESCRIPTION

The Hitachi HM628128 is a CMOS static RAM organized 128k-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation, therefore it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460 mil body SOP) or a 600 mil plastic DIP, is available for high density mounting.

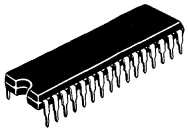
■ FEATURES

- High speed: Fast Access time 70/85/100/120 ns (max.)
- Low power
  Standby: 10 μW (typ.) (L-version)
  Operation: 75 mW (typ.)
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output—Three state output
- Directly TTL compatible—All inputs and outputs
- Capability of battery back up operation (L-version)
  2 chip selection for battery back up

■ PIN DESCRIPTION

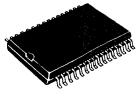
Pin Name	Function
A_0–A_{16}	Address
I/O_0–I/O_7	Input/Output
$\overline{CS_1}$	Chip Select
CS_2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
NC	No Connection
V_{CC}	Power Supply
V_{SS}	Ground

HM628128P Series



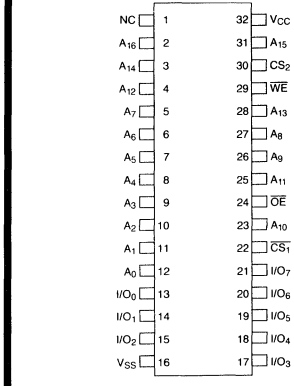
(DP-32)

HM628128FP Series



(FP-32D)

■ PIN ARRANGEMENT

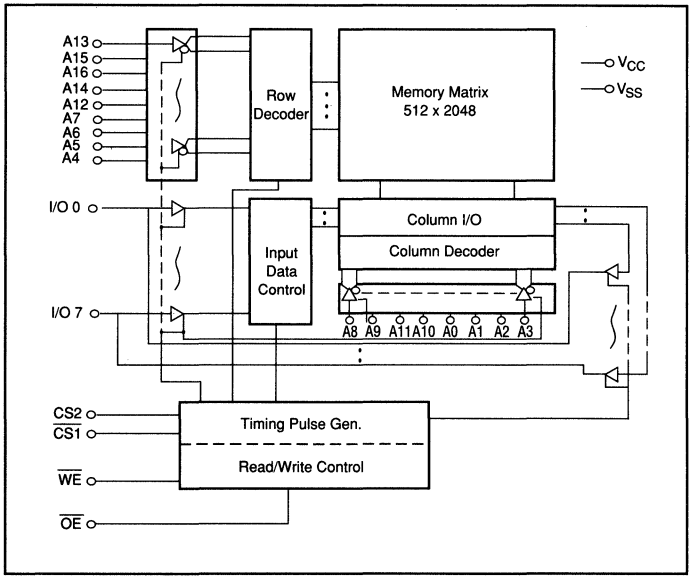


(Top View)

■ ORDERING INFORMATION

Part No.	Access	Package
HM628128P-7	70 ns	600 mil 32 pin Plastic DIP
HM628128P-8	85 ns	
HM628128P-10	100 ns	
HM628128P-12	120 ns	
HM628128LP-7	70 ns	
HM628128LP-8	85 ns	
HM628128LP-10	100 ns	
HM628128LP-12	120 ns	
HM628128FP-7	70 ns	525 mil 32 pin Plastic SOP
HM628128FP-8	85 ns	
HM628128FP-10	100 ns	
HM628128FP-12	120 ns	
HM628128LFP-7	70 ns	
HM628128LFP-8	85 ns	
HM628128LFP-10	100 ns	
HM628128LFP-12	120 ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	-0.5^{*1} to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. -3.0 V for pulse half-width ≤ 30 ns

■ FUNCTION TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
X	H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	
X	X	L	X		I_{SB}, I_{SB1}	High Z	
H	L	H	H	Output Disable	I_{CC}	High Z	
H	L	H	L	Read	I_{CC}	D_{out}	Read Cycle
L	L	H	H	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	H	L		I_{CC}	D_{in}	Write Cycle(2)

NOTE: 1. X : H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V	
Input Low (Logic 0) Voltage	V_{IL}	-0.3^{*1}	—	0.8	V	

NOTE: 1. -3.0V for pulse half-width ≤ 30 ns

■ DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2	μA	V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL}, $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current: DC	I_{CCDC}	—	15	35	mA	$\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating Power Supply Current	I_{CC1}	—	45	70	mA	Min. cycle, duty = 100%, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
	I_{CC2}	—	15	30	mA	Cycle time = 1μs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS_1}$ ≤ 0.2V, CS_2 ≥ V_{CC} - 0.2V, V_{IH} ≥ V_{CC} - 0.2V, V_{IL} ≤ 0.2V
Standby V_{CC} Current: DC	I_{SB}	—	1	3	mA	$\overline{CS_1}$ = V_{IH}, CS_2 = V_{IH} or CS_2 = V_{IL}
Standby V_{CC} Current (1): DC	I_{SB1}	—	0.02	2	mA	V_{in} ≥ 0V, $\overline{CS_1}$ ≥ V_{CC} - 0.2V, CS_2 ≥ V_{CC} - 0.2V or 0V ≤ CS_2 ≤ 0.2V
		—	2*2	100*2	μA	
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -1.0 mA

NOTE: 1. Typical values are at V_{CC} = 5.0V, T_A = +25°C and specified loading.
2. This characteristic is guaranteed only for L-version.

■ CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	8	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

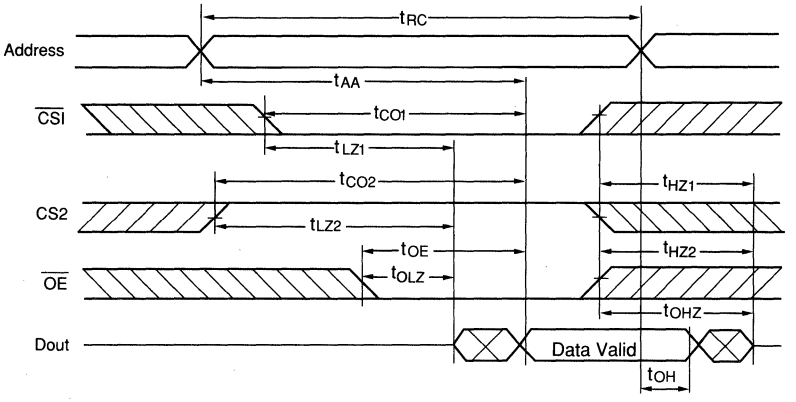
Test Conditions

Input pulse levels:	0.8V to 2.4V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5V
Output load:	1 TTL Gate and CL (100 pF) (Including scope & jig)

■ Read Cycle

Parameter	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip Selection ($\overline{CS_1}$) to Output Valid	t_{CO1}	—	70	—	85	—	100	—	120	ns
Chip Selection (CS_2) to Output Valid	t_{CO2}	—	70	—	85	—	100	—	120	ns
Output Enable ($\overline{OE}$) to Output Valid	t_{OE}	—	35	—	45	—	50	—	60	ns
Chip Selection ($\overline{CS_1}$) *1, *2 to Output in Low Z	t_{LZ1}	10	—	10	—	10	—	10	—	ns
Chip Selection (CS_2) *1, *2 to Output in Low Z	t_{LZ2}	10	—	10	—	10	—	10	—	ns
Output Enable ($\overline{OE}$) *1, *2 to Output in Low Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip Deselection ($\overline{CS_1}$) *1, *2 to Output in High Z	t_{HZ1}	0	25	0	30	0	35	0	45	ns
Chip Deselection (CS_2) *1, *2 to Output in High Z	t_{HZ2}	0	25	0	30	0	35	0	45	ns
Output Disable ($\overline{OE}$) *1, *2 to Output in High Z	t_{OH2}	0	25	0	30	0	35	0	45	ns
Output Hold From Address Change	t_{OH}	10	—	10	—	10	—	10	—	ns

Read Cycle Timing



NOTE: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

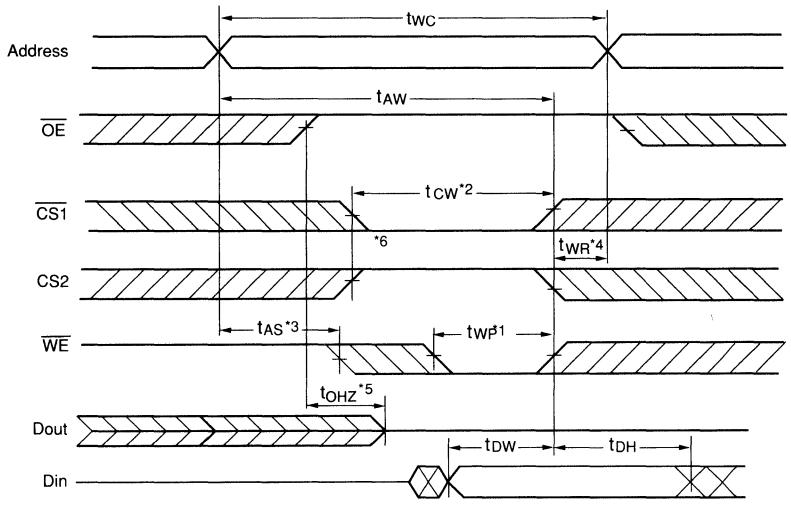
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

3. $\overline{WE}$ is high for read cycle.

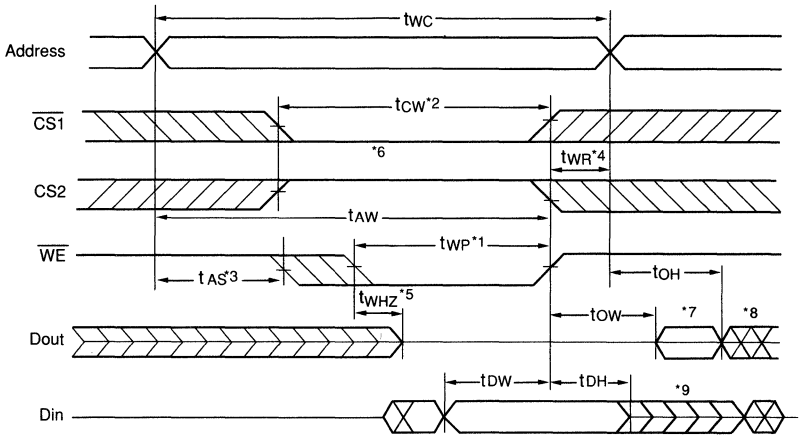
■ Write Cycle

Parameter	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	70	—	85	—	100	—	120	—	ns
Chip Selection to End of Write	t_{CW}	60	—	75	—	90	—	100	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	60	—	75	—	90	—	100	—	ns
Write Pulse Width	t_{WP}	55	—	65	—	75	—	85	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	5	—	10	—	ns
		10*11	—	10*11	—	10*11	—	15*11	—	ns
Write to Output in*10 High Z	t_{WHZ}	0	25	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30	—	35	—	40	—	45	—	ns
Write Hold From Write Time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output Active From*10 End of Write	t_{OW}	5	—	5	—	5	—	5	—	ns

Write Cycle Timing (1) ($\overline{OE}$ Clock)



Write Cycle Timing (2) ($\overline{OE}$ Low Fix)



NOTE:

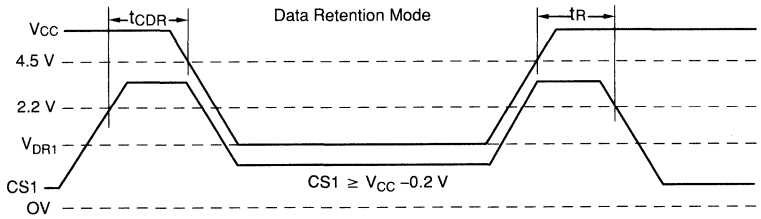
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ going low, CS_2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS_1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{out} is the same phase of the latest written data in this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. This value is measured from CS_2 going low to the end of write cycle.

■ Low V_{CC} Data Retention Characteristics (T_A = 0 to +70°C)

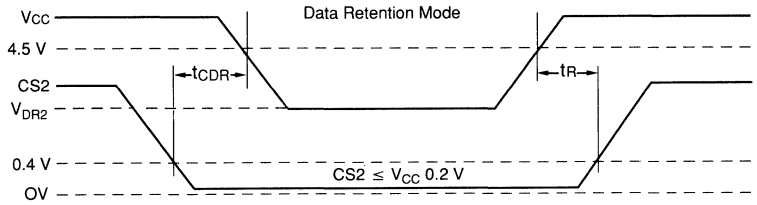
(These characteristics are guaranteed only for L-version.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions*2
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ or $0V \leq CS_2 \leq 0.2V$ $V_{in} \geq 0V$
Data Retention Current	I_{CCDR}	—	1	50*1	μA	V_{CC} = 3.0V, $V_{in} \geq 0V$, $\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ or $0V \leq CS_2 \leq 0.2V$
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation Recovery Time	t_R	5	—	—	ms	

Low V_{CC} Data Retention Waveform (1) ($\overline{CS_1}$ Controlled)



Low V_{CC} Data Retention Waveform (2) (CS_2 Controlled)

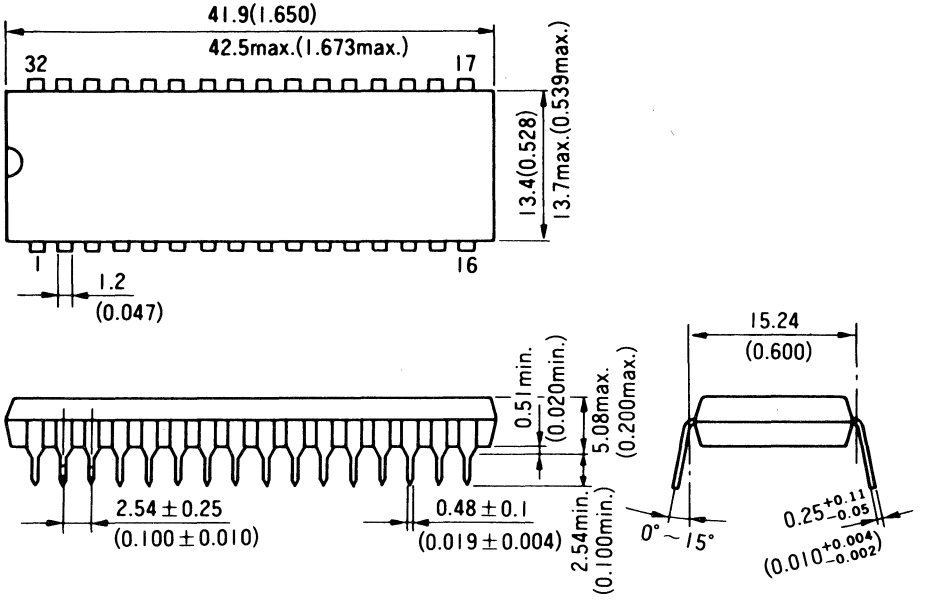


NOTE: 1. 20 μA max. at T_A = 0 to 40°C.

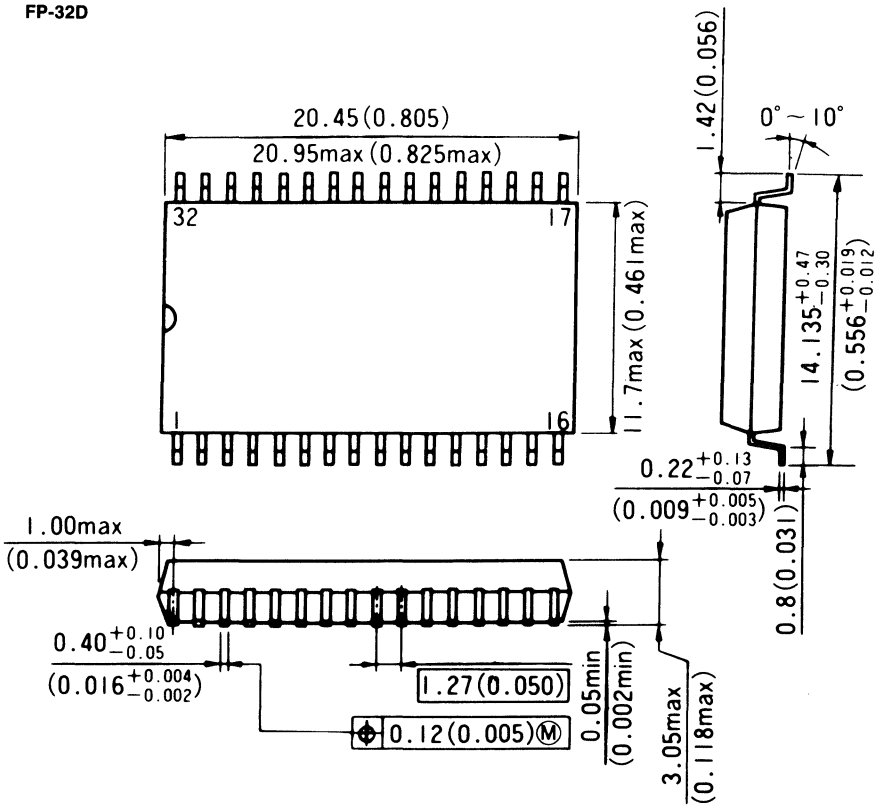
2. CS_2 controls address buffer, WE buffer, $\overline{CS_1}$ buffer and $\overline{OE}$ buffer and D_{in} buffer. If CS_2 controls data retention mode, V_{in} levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS_1}$, I/O) can be in the high impedance state. If $\overline{CS_1}$ controls data retention mode, CS_2 must be $CS_2 \geq V_{CC} - 0.2V$ or $0V \leq CS_2 \leq 0.2V$. The other input levels (addresses, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Package Outline

DP-32



FP-32D


20.45(0.805)
20.95max(0.825max)
32
17
1
16
11.7max(0.461max)
1.42(0.056)
0°~10°
14.135+0.47 −0.30
(0.556+0.019 −0.012)
0.22+0.13 −0.07
(0.009+0.005 −0.003)
0.8(0.031)
1.00max
(0.039max)
0.40+0.10 −0.05
(0.016+0.004 −0.002)
1.27(0.050)
0.12(0.005)M
0.05min
(0.002min)
3.05max
(0.118max)

MOS PSEUDO STATIC RAM

HM65256A Series — Maintenance Only

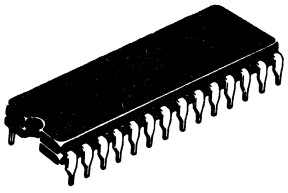
(Substitute HM65256B)

32768-word x 8-bit High Speed CMOS Pseudo Static RAM

■ FEATURES

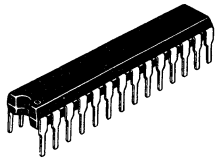
- Single 5V (±10%)
- High Speed
  - Access Time
    - $\overline{CE}$ Access Time 120/150/200ns
    - Address Access Time 60/75/100ns
    - (in static column mode)
  - Cycle Time
    - Random Read/Write Cycle Time 190/235/310ns
    - Static Column Mode Cycle Time 65/80/105ns
- Low Power
  - 175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  - Address Refresh
  - Automatic Refresh
  - Self Refresh
  - Hidden Refresh

HM65256AP Series



(DP-28)

HM65256ASP Series

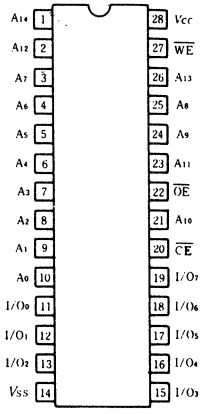


(DP-28N)

■ ORDERING INFORMATION

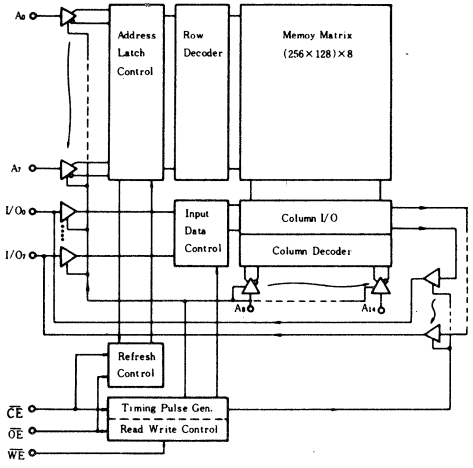
Type No.	Access Time	Package
HM65256AP-12 HM65256AP-15 HM65256AP-20	120ns 150ns 200ns	600 mil 28 pin Plastic DIP
HM65256ASP-12 HM65256ASP-15 HM65256ASP-20	120ns 150ns 200ns	300 mil 28 pin Plastic DIP

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



HITACHI

Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$ at $\overline{CE}$ going Low	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Notes
L	H	L	H	Low Z	Read	
L	H	H	L	High Z	Write	
L	H	H	H	High Z	–	
L	L	L	X	Low Z	Hidden Refresh	Output Buffers must keep Low Impedance State in previous Precharge Cycle.
L	L	X	X	High Z	Auto-matic Refresh	Output Buffers must turn off in previous Precharge Cycle.
L	X	X	X	High Z	Self Refresh	$\overline{CE}$ Pulse Width $\geq$ 300μ sec.
H	X	H	X	High Z	Standby	
H	X	L	X	X	–	Once Dout Buffers turn off, Output Buffers remain in High Impedance State.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−1.0	–	0.8	V

■ DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, T_a=0 to +70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0 t_{cyc} = min.	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	–	1	2	mA
Standby Power Supply Current	I_{SB2}	$\overline{CE}$ $\geq$ V_{CC} − 0.2V $\overline{OE}$ $\geq$ V_{CC} − 0.2V	–	0.4	0.6	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IL}	–	0.6	1	mA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	−10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	V
	V_{OH}	I_{OH} = −1 mA	2.4	–	–	V

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

• AC TEST CONDITIONS

- ○ Input Pulse Levels . . . 0.4 to 2.4V
- ○ Input Rise and Fall Times . . . 5 ns
- ○ Input Timing Reference Levels . . . 0.8V, 2.2V
- ○ Output Timing Reference Levels . . . V_{OH} = 2.0V, V_{OL} = 0.8V
- ○ Output Load . . . 1TTL Gate and C_L = 100pF (including jig and scope)

• READ AND WRITE MODE

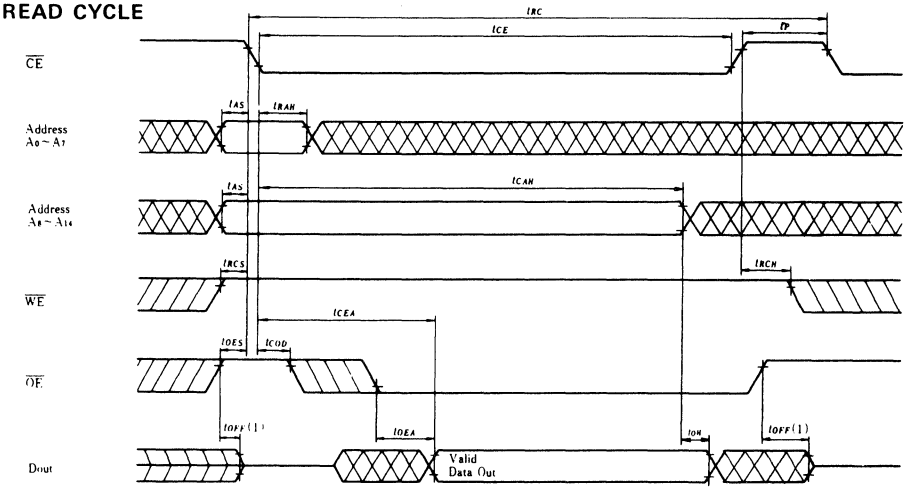
Item	Symbol	HM65256A-12		HM65256A-15		HM65256A-20		Unit	Note
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	190	–	235	–	310	–	ns	
Read Modify Write Cycle Time	t_{RWC}	265	–	325	–	425	–	ns	
Chip Enable Access Time	t_{CEA}	–	120	–	150	–	200	ns	
Address Access Time	t_{AA}	–	60	–	75	–	100	ns	
Output Enable Access Time	t_{OEA}	–	50	–	60	–	75	ns	
Output Buffer Turn-off Delay	t_{OFF}	5	20	5	25	5	35	ns	(1)
Chip Enable Pulse Width	t_{CE}	120	10000	150	10000	200	10000	ns	
Chip Enable Precharge Time	t_p	60n	4m	75n	4m	100n	4m	s	
Address Set-up Time	t_{AS}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	30	–	ns	
Column Address Hold Time	t_{CAH}	120	–	150	–	200	–	ns	
Column Address Hold Time from $\overline{CE}$ going High	t_{AH}	0	–	0	–	0	–	ns	
Static Mode Read or Write Cycle Time	t_{RSC}	65	–	80	–	105	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Output Enable Set-up Time	t_{OES}	0	–	0	–	0	–	ns	
Chip Enable to Output Enable Delay Time	t_{COD}	20	–	25	–	30	–	ns	
Output Hold Time from Column Address	t_{OH}	5	–	5	–	10	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	30	–	35	–	40	–	ns	
Write Command Pulse Width	t_{WP}	20	–	25	–	30	–	ns	
Write Command to Chip Enable Lead Time	t_{WCL}	45	–	55	–	70	–	ns	
Column Address Set-up Time for Write	t_{ASW}	0	–	0	–	0	–	ns	
Write Command to Column Address Lead Time	t_{WAL}	45	–	55	–	70	–	ns	
Data In Set-up Time	t_{DS}	0	–	0	–	0	–	ns	
Data In Hold Time for Early Write	t_{DHC}	30	–	35	–	40	–	ns	
Data In Hold Time for Late Write	t_{DHW}	20	–	25	–	30	–	ns	
Output Enable to Data In Delay Time	t_{ODD}	20	–	25	–	35	–	ns	(4)
Data In Floating to Output Enable Delay Time	t_{DFO}	0	–	0	–	0	–	ns	(4)
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	(7)
Refresh Command Set-up Time	t_{RFS}	0	–	0	–	0	–	ns	
Refresh Command Hold Time	t_{RFH}	20	–	25	–	30	–	ns	
Chip Enable Pulse Width for Self Refresh	t_{CEF}	300	–	300	–	300	–	μs	

(to be continued)

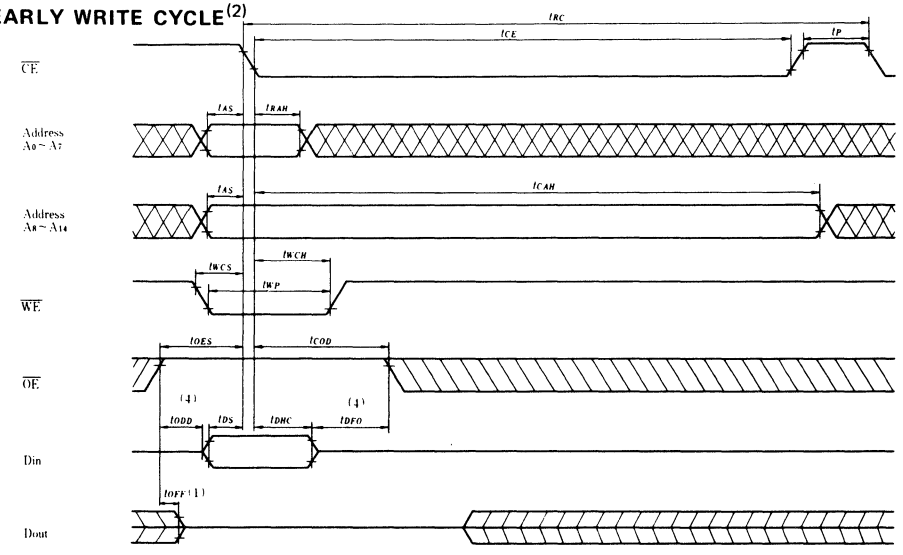
Item	Symbol	HM65256A-12		HM65256A-15		HM65256A-20		Unit	Note
		min	max	min	max	min	max		
Chip Enable Pre-charge Time after Self Refresh	t_{PF}	190	–	235	–	310	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	256 cycle

Notes:
1. t_{OFF} (max) defines the time at which the output achieves the open circuit condition.
2. Write starts with the later of $\overline{CE}$ or $\overline{WE}$ going low (exept during a refresh cycle).
3. If the first write pulse is applied within t_{CE} (min), the second write pulse must be applied after t_{CE} (min).
4. If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ turning on output buffers.
5. Once $\overline{OE}$ goes high and output buffers turn off in precharge cycle, automatic refresh cycle can start. Output buffers remain in high impedance state in automatic refresh cycle.
6. Output buffers are in high impedance state, and not controlled by $\overline{OE}$ in self refresh mode.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

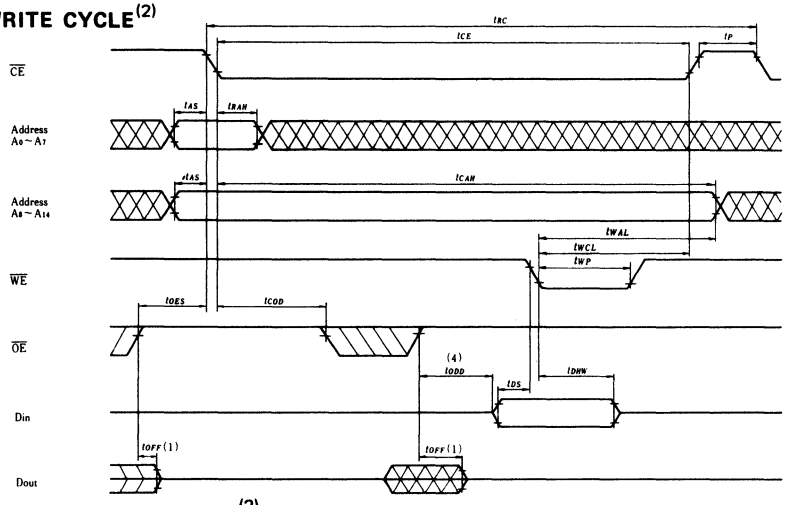
• READ CYCLE



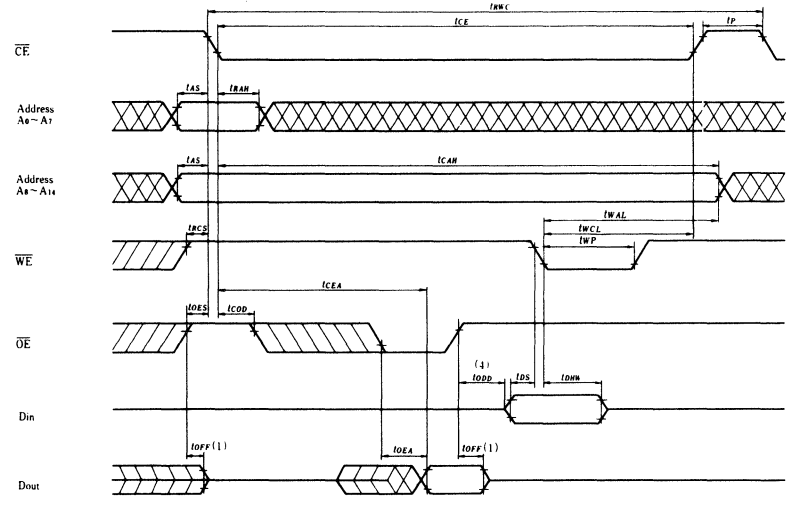
• EARLY WRITE CYCLE(2)



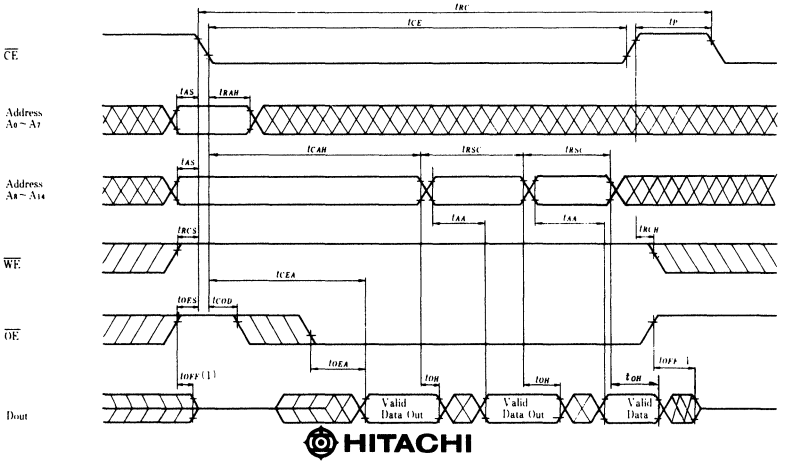
• LATE WRITE CYCLE(2)



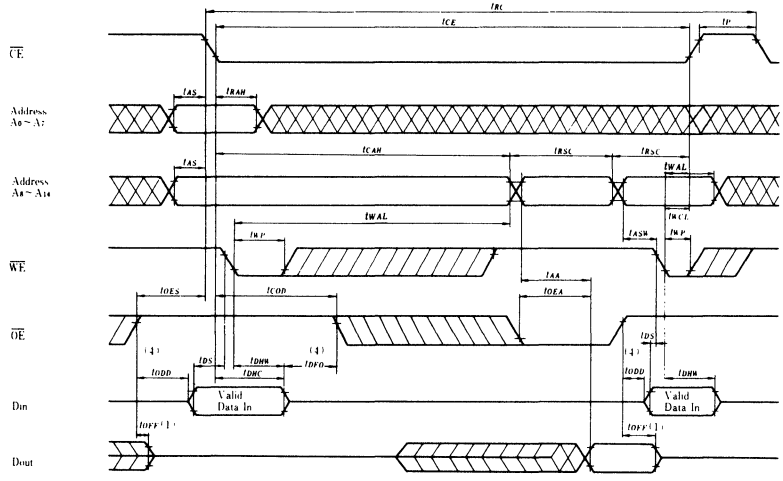
• READ MODIFY WRITE CYCLE(2)



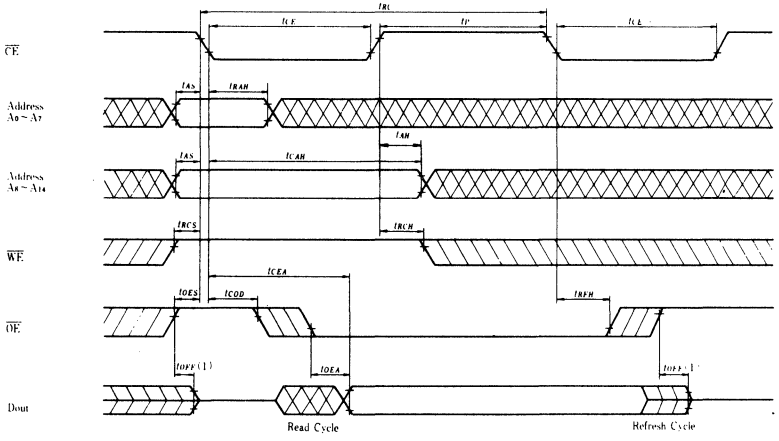
• STATIC COLUMN MODE READ CYCLE



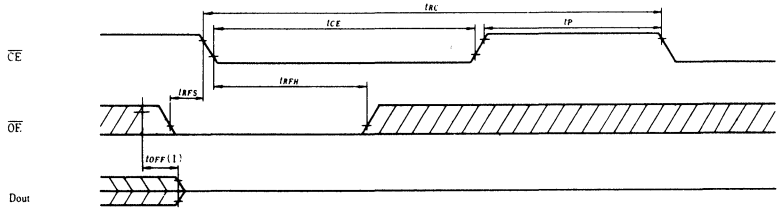
• STATIC COLUMN MODE WRITE CYCLE[2],[3]



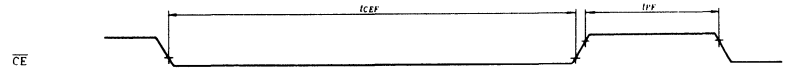
• HIDDEN REFRESH CYCLE



• AUTOMATIC REFRESH CYCLE[5]



• SELF REFRESH CYCLE[6]



• CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	min	typ	max	Unit	Conditions
Input Pin Capacitance	C_{in}	–	–	5	pF	V_{in} = 0 V
I/O Pin Capacitance	$C_{I/O}$	–	–	7	pF	$V_{I/O}$ = 0 V

Note) These parameters are not 100% tested.

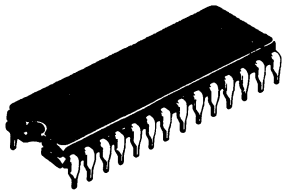
HM65256B Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

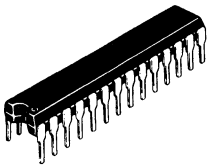
- Single 5V (±10%)
- High Speed
  Access Time
  $\overline{CE}$ Access Time 100/120/150/200ns
  Address Access Time 50/60/75/100ns
  (in Static Column Mode)
  Cycle Time
  Random Read/Write Cycle Time 160/190/235/310ns
  Static Column Mode Cycle Time 55/65/80/105ns
- Low Power
  175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh

HM65256BP Series



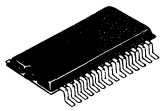
(DP-28)

HM65256BSP Series



(DP-28N)

HM65256BFP Series

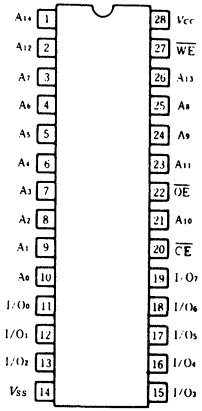


(FP-28DA)

■ ORDERING INFORMATION

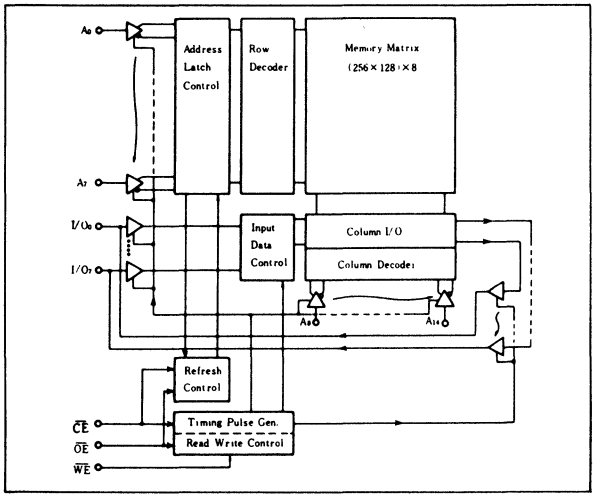
Type No.	Access Time	Package
HM65256BP-10	100ns	600 mil 28 pin Plastic DIP
HM65256BP-12	120ns	
HM65256BP-15	150ns	
HM65256BP-20	200ns	
HM65256BLP-10	100ns	
HM65256BLP-12	120ns	
HM65256BLP-15	150ns	
HM65256BLP-20	200ns	
HM65256BSP-10	100ns	300 mil 28 pin Plastic DIP
HM65256BSP-12	120ns	
HM65256BSP-15	150ns	
HM65256BSP-20	200ns	
HM65256BLSP-10	100ns	
HM65256BLSP-12	120ns	
HM65256BLSP-15	150ns	
HM65256BLSP-20	200ns	
HM65256BFP-10T	100ns	28 pin Plastic SOP
HM65256BFP-12T	120ns	
HM65256BFP-15T	150ns	
HM65256BFP-20T	200ns	
HM65256BLFP-10T	100ns	
HM65256BLFP-12T	120ns	
HM65256BLFP-15T	150ns	
HM65256BLFP-20T	200ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	–
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	− 1.0	–	0.8	V

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Conditions	HM65256B Series			HM65256BL Series			Unit
			min.	typ.	max.	min.	typ.	max.	
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0mA t_{cyc} = min.	–	35	65	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	–	1	2	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \geq V_{CC}-0.2V$	–	–	–	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	–	1	2	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \leq 0.2V$	–	–	–	–	50	100	µA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V Vin = V_{SS} to V_{CC}	–10	–	10	–10	–	10	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	–10	–	10	µA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = –1 mA	2.4	–	–	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	Cin	Vin = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level . . . . . V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load . . . . . 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Radom Read or Write Cycle Time	t_{RC}	160	–	190	–	235	–	310	–	ns
Static Column Mode Read or Write Cycle	t_{RSC}	55	–	65	–	80	–	105	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	–	200	ns
Address Access Time	t_{AA}	–	50	–	60	–	75	–	100	ns
Output Enable Access Time	t_{OEA}	–	40	–	50	–	60	–	75	ns
Chip Disable to Output in High Z	t_{CHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	30	–	35	–	40	–	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable Pulse Width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	50	–	60	–	75	–	100	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	20	–	20	–	25	–	30	–	ns
Column Address Hold Time	t_{CAH}	100	–	120	–	150	–	200	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns
Output Enable Hold Time	t_{OHC}	0	–	0	–	0	–	0	–	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	–	0	–	0	–	0	–	ns
Output Hold Time from Column Address	t_{OH}	5	–	5	–	5	–	10	–	ns
Write Command Pulse Width	t_{WP}	25	–	25	–	30	–	35	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	200	–	ns
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	0	–	ns

(to be continued)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Column Address Hold Time after Write	t_{AHW}	0	–	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	20	–	25	–	30	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	50	–	60	–	75	–	100	–	ns
Refresh Precharge Time	t_{FP}	30	–	30	–	30	–	30	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	160	–	190	–	235	–	310	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	–	10000	–	10000	–	10000	–	ns
Refresh Reset Time for Self Refresh	t_{FRS}	160	–	190	–	235	–	310	–	ns
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit conditions.

(2) t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T=5ns, and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

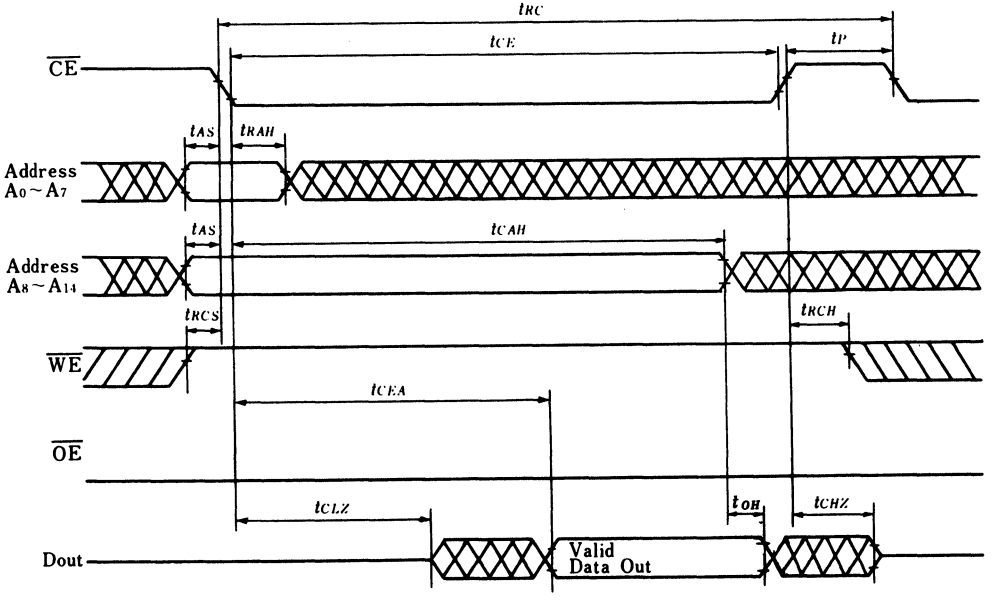
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

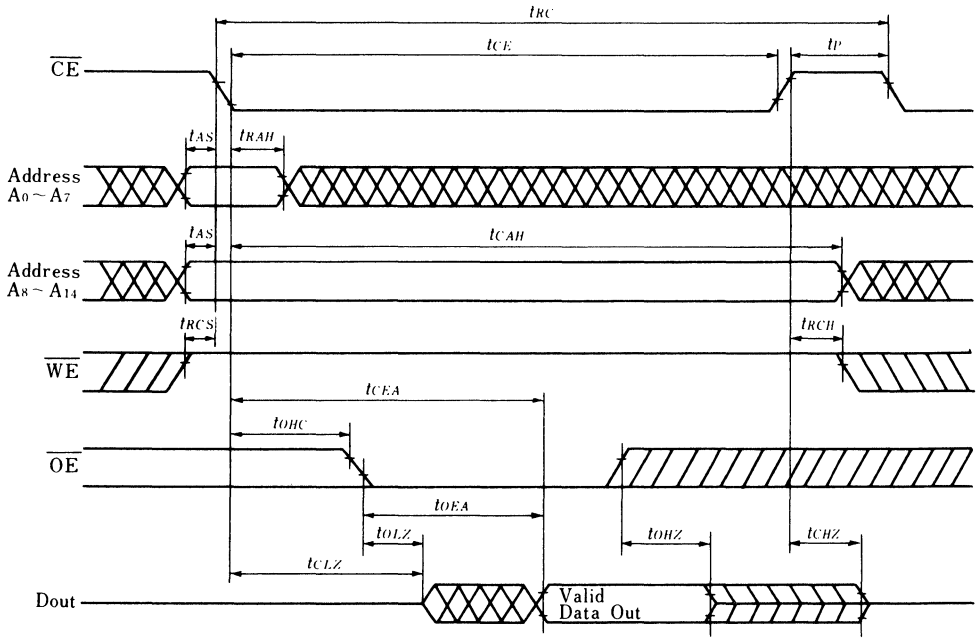
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

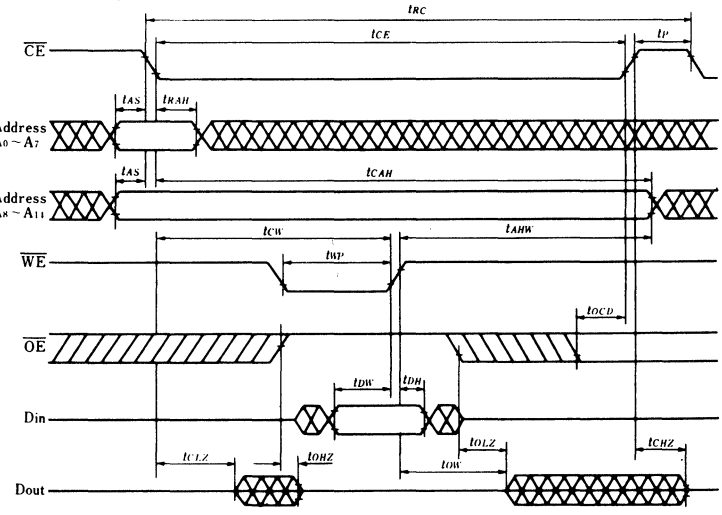
• Read Cycle No. 1 ($\overline{CE}$ controlled)



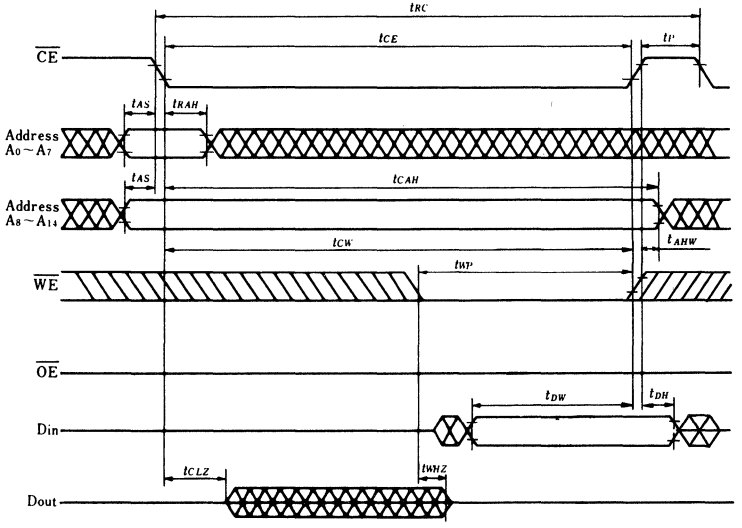
- **Read Cycle No. 2 ($\overline{OE}$ controlled)**



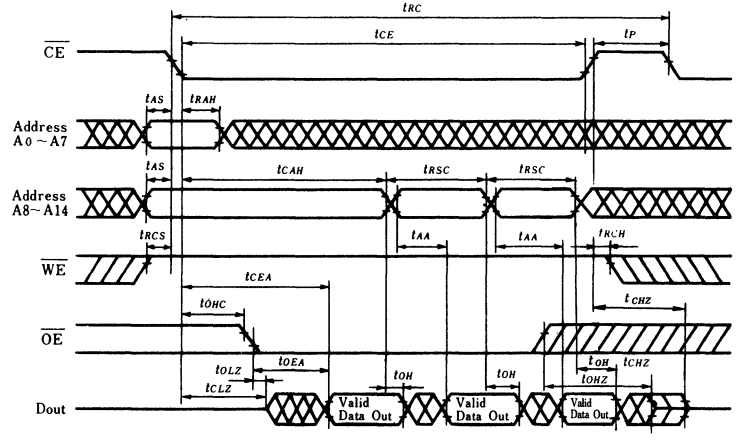
- **Write Cycle No. 1 ($\overline{OE}$ Clock)**



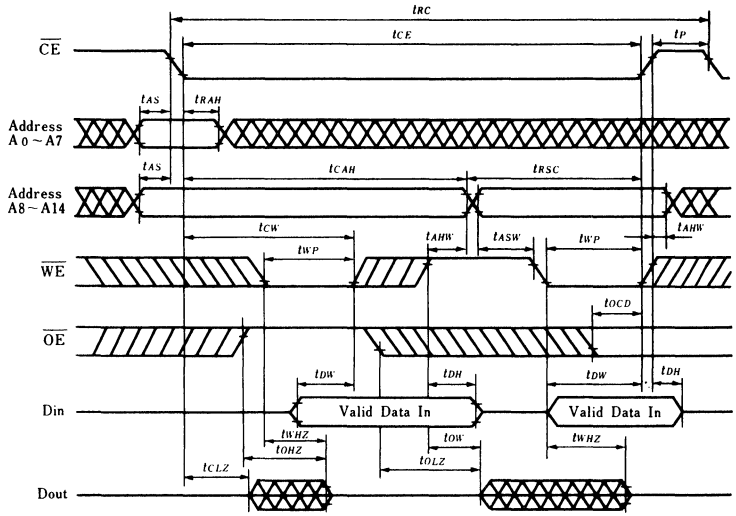
- **Write Cycle No. 2 ($\overline{OE}$ low fix)**



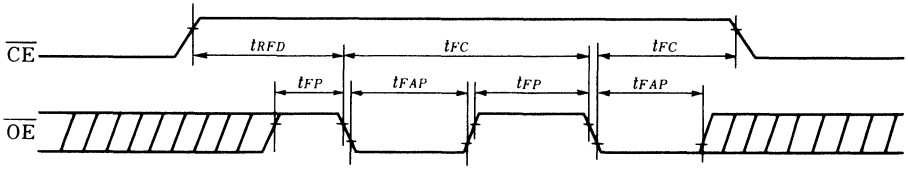
- **Static Column Mode Read Cycle**



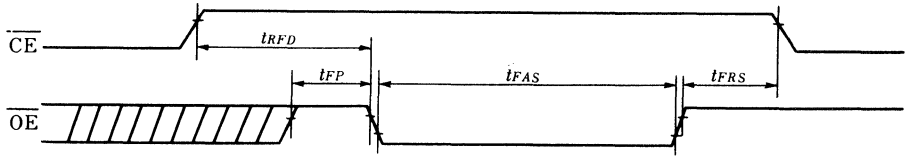
- **Static Column Mode Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



HM658128 Series

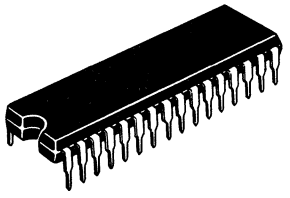
131072-word x 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128 is a pseudo-static RAM organized as 131,072-word x 8-bit. HM658128 realizes low power consumption and high speed access time by employing 1.3μm CMOS process technology.

The HM658128 supports 3 refresh functions: Address Refresh, Auto Refresh and Self Refresh. Low power version dissipates only 0.5mW (typ.) in Self Refresh Mode and retains the data with battery backup for short time.

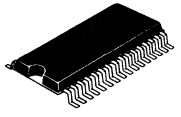
The HM658128 is pin-compatible with 256k-bit PSRAM and static RAM.

HM658128P Series



(DP-32)

HM658128FP Series



(FP-32D)

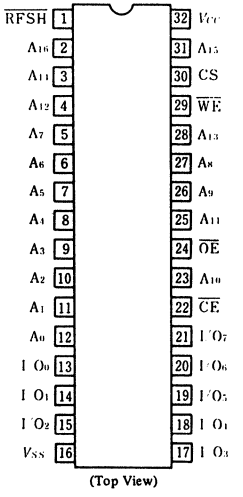
■ FEATURES

- Single 5V (±10%)
- High Speed
  - ○ Access Time
    $\overline{CE}$ Access Time . . . 100/120/150ns
  - ○ Cycle Time
    Random Read/Write Cycle Time . . . 180/210/250ns
- Low Power . . . 200mW typ. (Active)
  0.5mW (standby) (L-version)
- All inputs and outputs TTL compatible
- Non Multiplexed Address
- 512 Refresh Cycles (8ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658128P-10 HM658128P-12 HM658128P-15	100ns 120ns 150ns	600 mil 32 pin Plastic DIP
HM658128LP-10 HM658128LP-12 HM658128LP-15	100ns 120ns 150ns	
HM658128FP-10 HM658128FP-12 HM658128FP-15	100ns 120ns 150ns	32 pin Plastic SOP
HM658128LFP-10 HM658128LFP-12 HM658128LFP-15	100ns 120ns 150ns	

■ PIN ARRANGEMENT

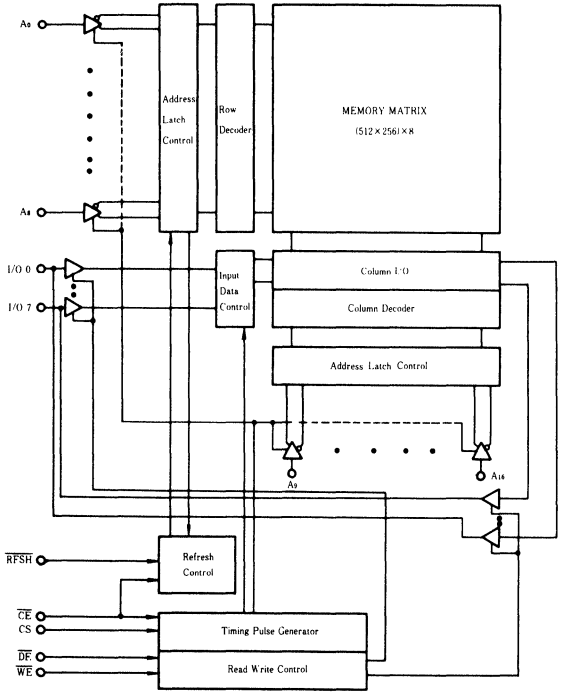


(Top View)

■ PIN DESCRIPTION

Symbol	Pin Name
A0 – A16	Address Inputs
I/O – I/O7	Data Input/Output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
CS	Chip Select
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low Z	Read
L	H	X	X	L	High Z	Write
L	H	X	H	H	High Z	–
L	L	X	X	X	High Z	CS Standby
H	X	L	X	X	High Z	Refresh
H	X	H	X	X	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	–1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +125	°C
Storage Temperature Under Bias	T_{bias}	–10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	– 1.0	–	0.8	V

■ DC CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0 t_{cyc} = min.	–	40	75	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	–	1	2	mA
Standby Power Supply Current	I_{SB2} *1	$\overline{CE} \geq V_{CC}$ –0.2V $\overline{RFSH} \geq V_{CC}$ –0.2V	–	100	200	μA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	–	1	2	mA
	I_{CC3} *1	$\overline{CE} \geq V_{CC}$ –0.2V $\overline{RFSH} \leq$ 0.2V	–	100	200	μA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	–10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
	V_{OH}	I_{OH} = –1mA	2.4	–	–	V

Note) *1. This characteristics is guranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	10	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level ..... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load ..... 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	180	–	210	–	250	–	ns
Random Read Modify Write Cycle Time	t_{RWC}	240	–	280	–	330	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	ns
Output Enable Access Time	t_{OEA}	–	30	–	40	–	50	ns
Chip Disable to Output in High Z	t_{CHZ}	–	30	–	35	–	40	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	35	–	40	–	ns
Output Disable to Output in HighZ	t_{OHZ}	–	25	–	30	–	35	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Enable Pulse Width	t_{CE}	100n	1μ	120n	1μ	150n	1μ	s
Chip Enable Precharge Time	t_P	70	–	80	–	90	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	30	–	35	–	40	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns
$\overline{RFSH}$ Hold Time	t_{RHC}	15	–	15	–	15	–	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	–	5	–	5	–	5	ns

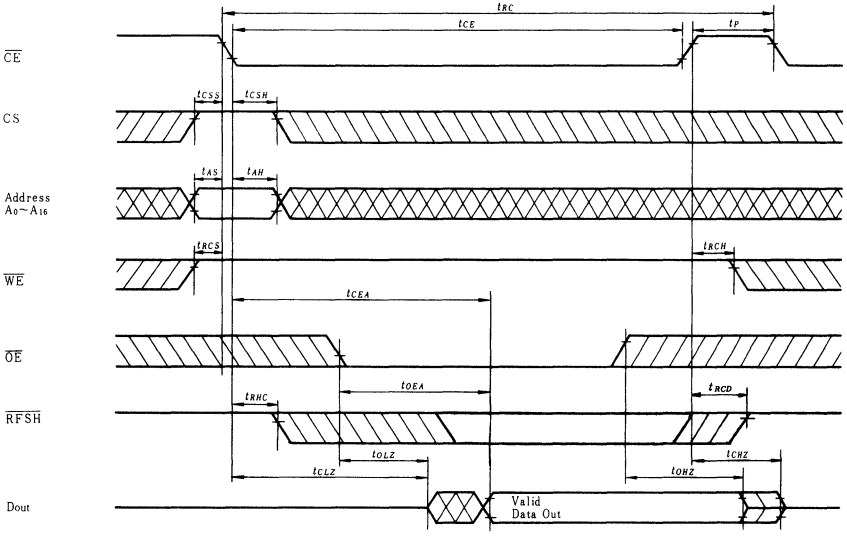
(to be continued)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Chip Select Set-up Time	t_{CSS}	0	–	0	–	0	–	ns
Chip Select Hold Time	t_{CSH}	30	–	35	–	40	–	ns
Write Command Pulse Width	t_{WP}	30	–	35	–	40	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	ns
Data In to End of Write	t_{DW}	25	–	30	–	35	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	70	–	80	–	90	–	ns
Refresh Precharge Time	t_{FP}	40	–	40	–	40	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	180	–	210	–	250	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	8	–	8	–	8	–	μs
Refresh Reset Time for Self Refresh	t_{RFS}	180	–	210	–	250	–	ns
Refresh Reset Time for Automatic Refresh	t_{RFA}	0	–	0	–	0	–	ns
Refresh Period (512 cycles)	t_{REF}	–	8	–	8	–	8	ns

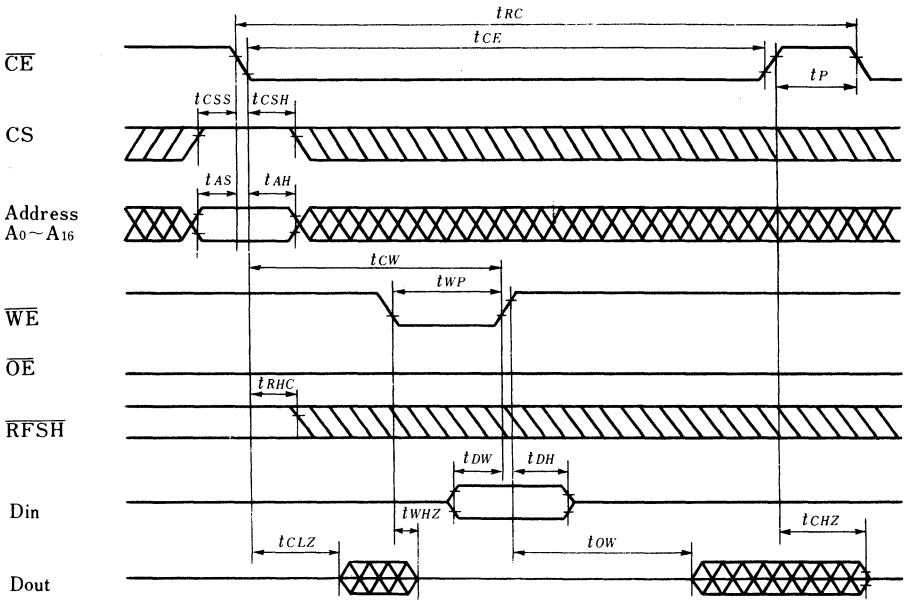
Notes:
(1) t_{CHZ}, t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit conditions under the condition of t_T = 5ns and not 100% tested.
(2) t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5ns and not 100% tested.
(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$. Write end is defined at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.
(8) After Self Refresh, Auto Refresh should be started within 15μs.

■ TIMING WAVEFORMS

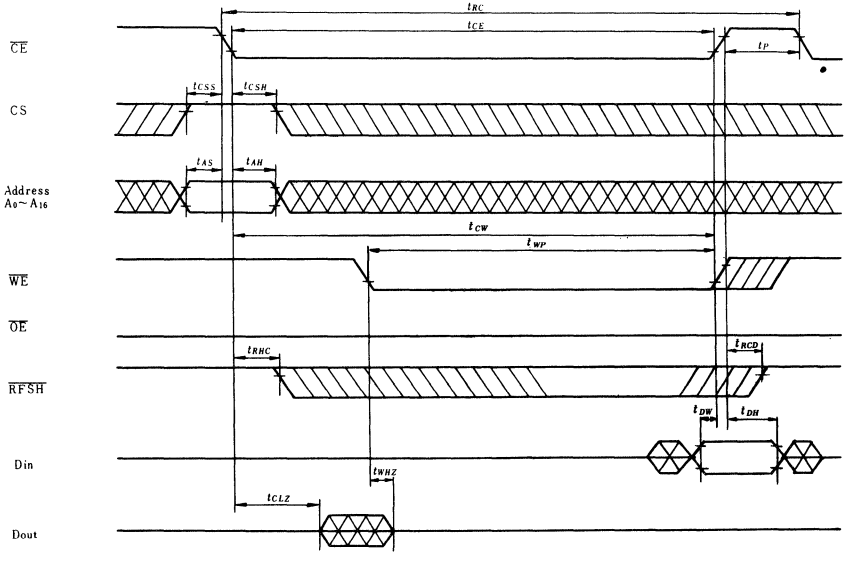
● Read Cycle



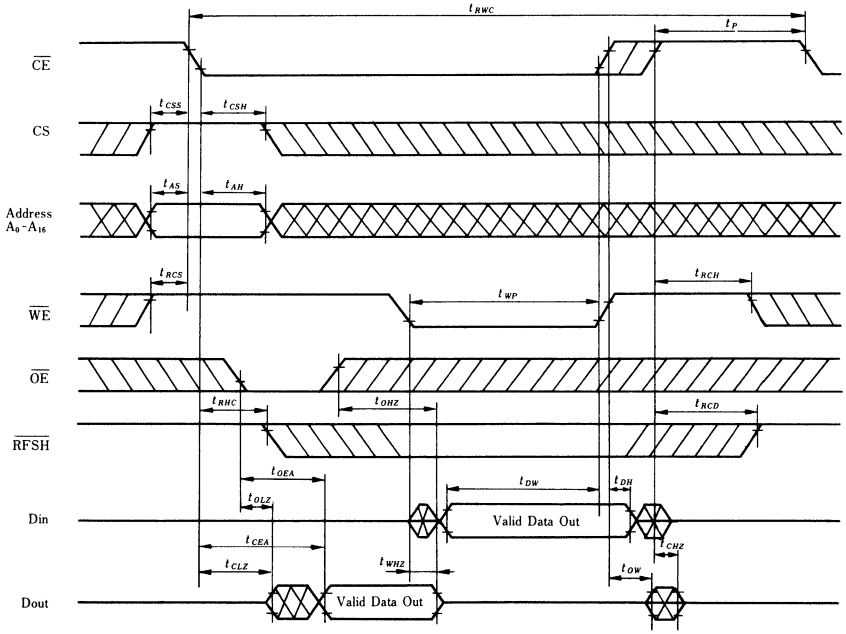
- **Write Cycle-1 ($\overline{OE}$ Clock)**



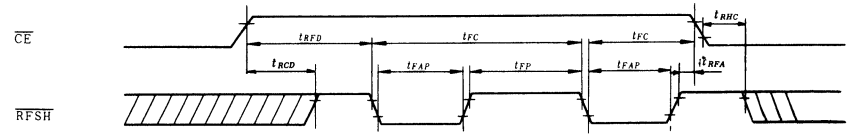
Write Cycle-2 ($\overline{OE}$ Low Fix)



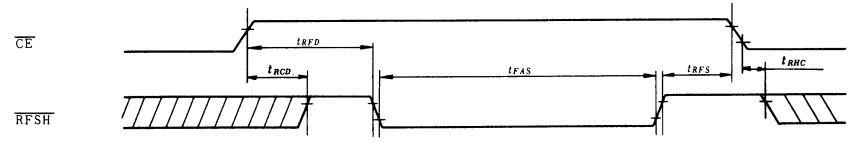
- **Read Modify Write Cycle**



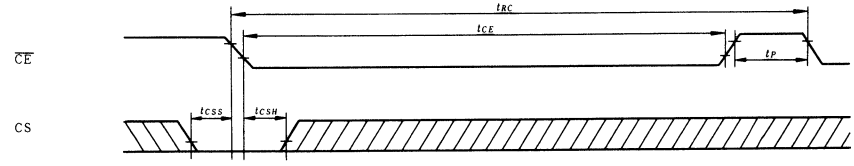
- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



- **CS Standby Mode**

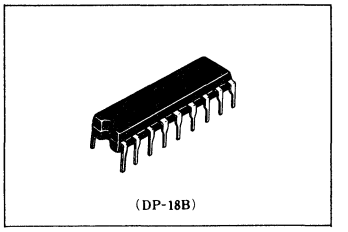


VIDEO MEMORY

262144-word x 4-bit Frame Memory

HM53051P is a 262,144-word x 4-bit frame memory, using most advanced 1.3μm CMOS process. It performs serial access by internal address generator.

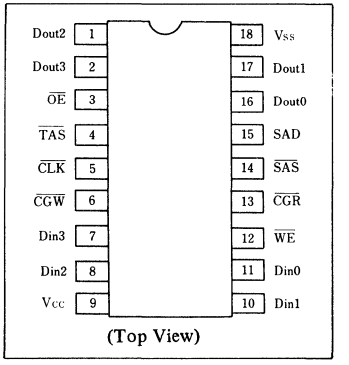
It offers high speed cycle time, 60 ns (min). As input data and output data are written or read in any cycle synchronized with a system clock, and the delay between them is arbitrary, Y/C separation or freezed picture is realized easily in 4fsc NTSC digital TV or VTR systems. Also, it performs random access by 32-word x 4-bit data block. By this function, picture in picture or multiplexed picture is displayed with ease.



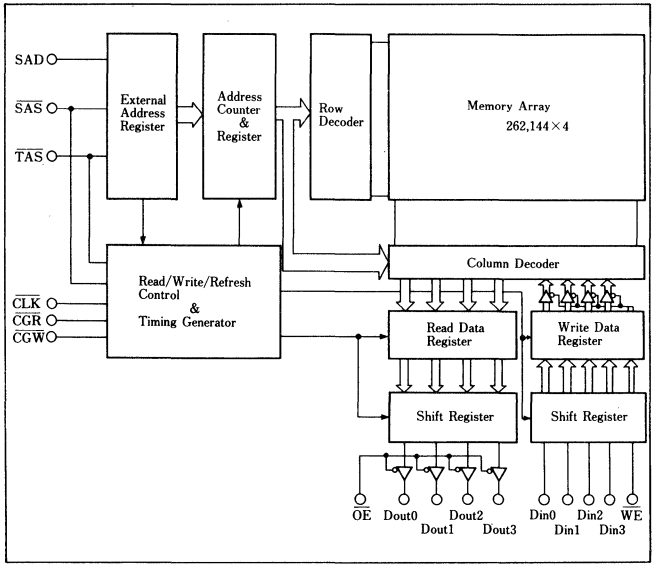
Features

- 262,144-word x 4-bit serial access memory
- Organized with dual ports
  - Serial input x 4-bit
  - Serial output x 4-bit
- High Speed
  - Read/Write Cycle Time. . . . . 60ns (min)
  - Access Time . . . . . 40ns (max)
- Semi-synchronous Read/Write Cycle
- Low Power
  - Active . . . . . 200mW (typ)
- Random Access per 32-word x 4-bit
- External Refresh Control is unnecessary

Pin Arrangement



Block Diagram



Pin Description

Din	Data Input
Dout	Data Output
$\overline{OE}$	Output Enable
$\overline{TAS}$	Transfer Address Strobe
$\overline{CLK}$	System Clock
$\overline{CGW}$	Clock Gate (Write)
$\overline{CGR}$	Clock Gate (Read)
SAD	Serial Address
$\overline{SAS}$	Serial Address Strobe
$\overline{WE}$	Write Enable

Note) The specifications of this device are subject to change without notice. Please contact Hitachi's Sales Dept. regarding specifications.

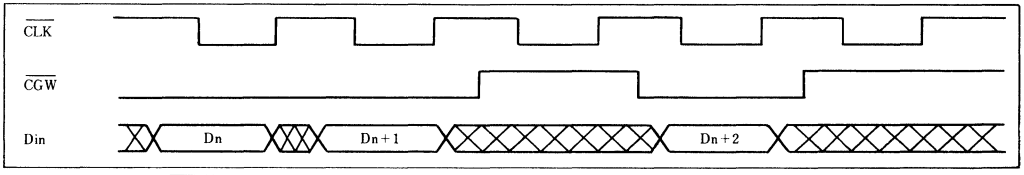
Functional Description

Serial access memory with I/O separated

Read cycle and write cycle of HM53051 can be operated independently synchronized with a system clock. It realizes time compression or expansion for picture in picture in digital TV, for example.

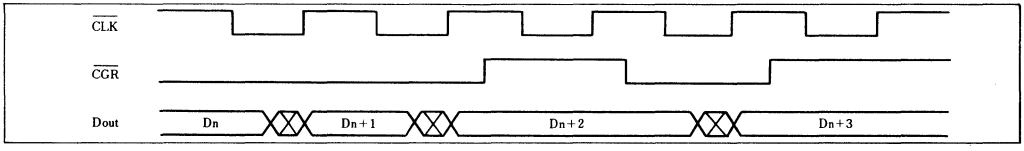
- **Write cycle by $\overline{CGW}$**

Write data are taken in at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGW}$ is low. If $\overline{CGW}$ is high, HM53051 does not enter write cycle (cycle time is defined by system clock cycle time). Time compression is realized easily with $\overline{CGW}$.



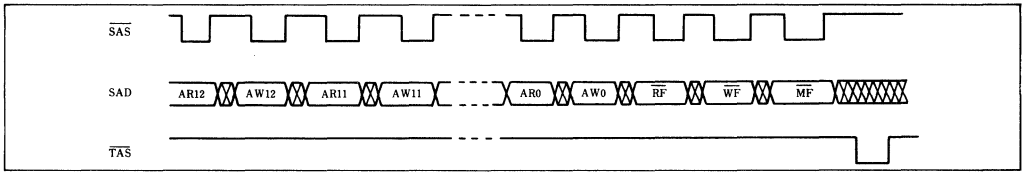
- **Read Cycle by $\overline{CGR}$**

Read data are put out at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGR}$ is low. If $\overline{CGR}$ is high, HM53051 does not enter read cycle (cycle time is defined by system clock time). Time expansion is realized easily with $\overline{CGR}$.



Random Access

The HM53051 is also capable of random access by serial address input, SAD. Random access by the unit of 32-word x 4-bit is performed, when $\overline{TAS}$ is low after read address (AR0 – AR12), write address (AW0 – AW12) and mode setting flags, $\overline{RF}$ (Read Flag), $\overline{WF}$ (Write Flatg) and $\overline{MF}$ (Mode Flag) are read into by SAD synchronized with $\overline{SAS}$. In order to output data continuously, the address specified by SAD incrments automatically.



Mode Programming

Operation mode in HM53051 is programmed by the combination of SAD 5-bit.

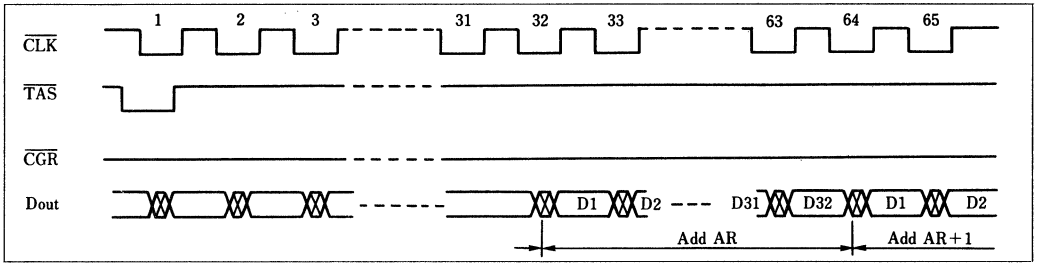
$\overline{MF}$	$\overline{WF}$	$\overline{RF}$	AW0	AR0	Mode
0	0	0	x	x	Write/read address asynchronous transfer
0	0	1	x	x	Write address asynchronous transfer
0	1	0	x	x	Read address asynchronous transfer
0	1	1	x	x	–
1	0	0	x	x	Write/read address synchronous transfer
1	0	1	x	x	Write address synchronous transfer
1	1	0	x	x	Read address synchronous transfer
1	1	1	1	1	System reset
1	1	1	0	0	
1	1	1	0	1	Inhibit
1	1	1	1	0	

Note) x means Don't care.

Read/Write Address Asynchronous Transfer Mode

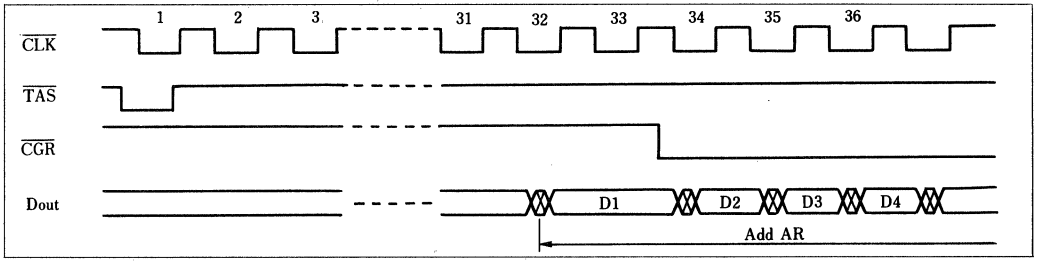
- **Read address asynchronous transfer mode**

(1) Read address asynchronous transfer mode (1) ($\overline{CGR}$: Low)



Note) The data block at read address AR, specified by SAD, is put out starting from the 32-nd system clock after the falling of $\overline{TAS}$.

(2) Read address asynchronous transfer mode (2) ($\overline{CGR}$: High)

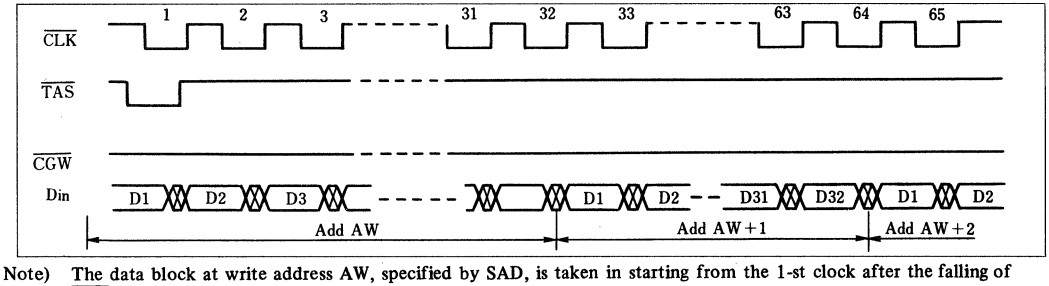


Notes) *1. The data block at read address AR, specified by SAD, is put out starting from the 32-nd system clock after the falling of $\overline{TAS}$.

*2. If $\overline{CGR}$ is turned to low after 33-rd clock from the falling edge of $\overline{TAS}$, the data at read address AR (D2, D3, D4 . .) are put out synchronously with $\overline{CLK}$ while $\overline{CGR}$ is low.

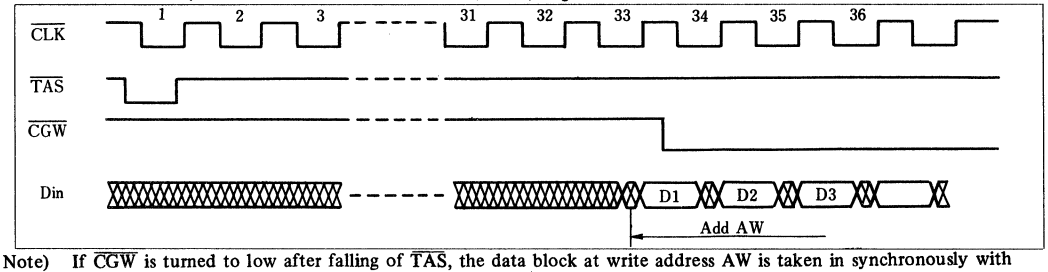
- **Write address asynchronous transfer mode**

(1) Write address asynchronous transfer mode (1) ($\overline{CGW}$: Low)



Note) The data block at write address AW, specified by SAD, is taken in starting from the 1-st clock after the falling of $\overline{TAS}$.

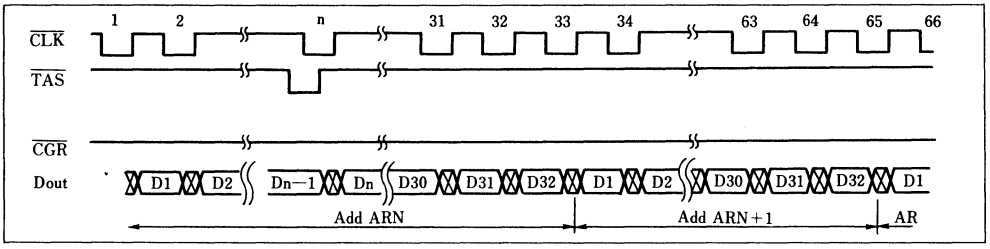
(2) Write address asynchronous transfer mode (2) ($\overline{CGW}$; High)



Note) If $\overline{CGW}$ is turned to low after falling of $\overline{TAS}$, the data block at write address AW is taken in synchronously with $\overline{CLK}$.

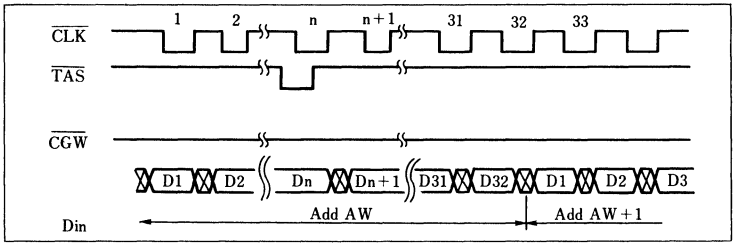
Read/Write Address Synchronous Transfer Mode

- Read address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block at read address AR, specified by SAD, is put out after the data block at the present read address ARN, and the next address ARN+1 is put out.

- Write address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block being written is taken into write address AW.

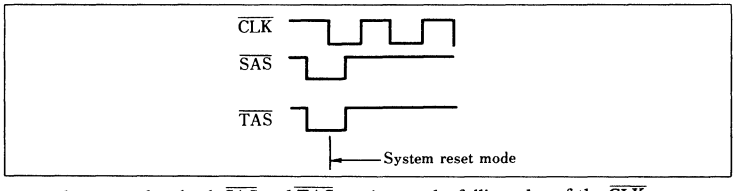
System Reset Mode

System reset mode is the same as read/write address asynchronous transfer mode except that read/write address are reset to 0.

- System reset by SAD

Note) System reset mode starts when $\overline{MF}$, $\overline{WF}$, $\overline{RF}$, AW0 and AR0 are all high.

- System reset by $\overline{SAS}$ and $\overline{TAS}$



Note) System reset mode starts when both $\overline{SAS}$ and $\overline{TAS}$ are low at the falling edge of the $\overline{CLK}$.

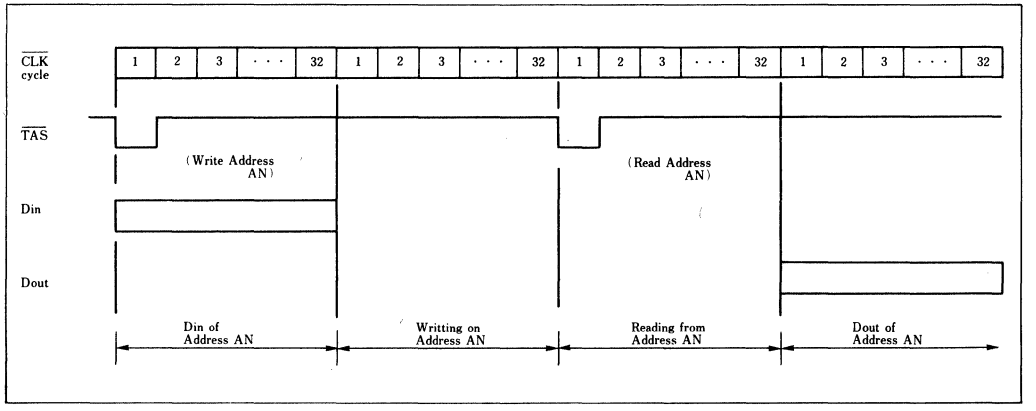
- 1 field delay

Note) 1. Field-delayed data are put out, when $\overline{CGR}$ and $\overline{CGW}$ turn to high before system reset at the beginning of every field, and turn to low simultaneously after 33-rd clock from system reset.

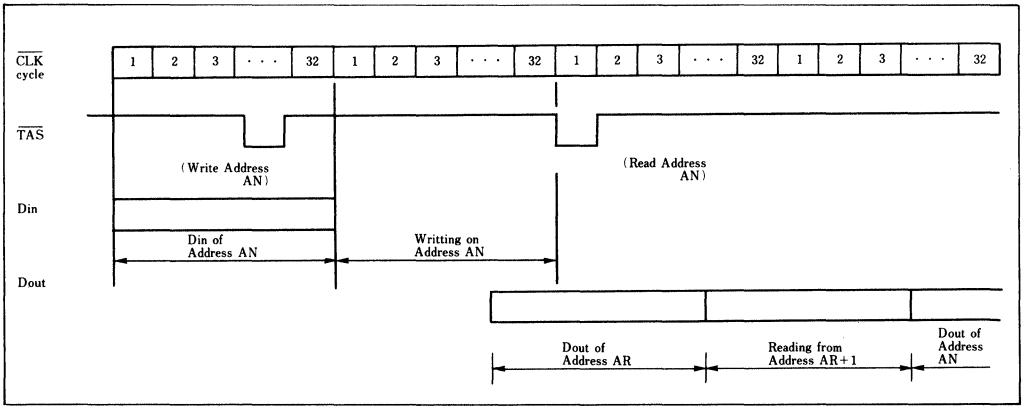
Considerations on Using HM53051

- Input/output data of less than 32-word, in read/write address asynchronous transfer mode or system reset, are not written or read out. The data are written or read out by the block of 32-word x 4-bit. Input data of less than 32-word are not written in write address asynchronous transfer mode or system reset. When asynchronous read address transfer mode or system reset mode is activated, output from present data block will continue. When output data from present data block are over, next data block of less than 32-word is not read out.
- The input data are not read out immediately. The data (32-word x 4-bit) are written into the memory array in the following 32-cycle after they are taken in.
  They can be read out only after writing into memory array is completed. If read address transfer mode is programmed after 33-rd clock from input data block, new data can be read out. If mode is programmed before 33-rd clock, new data or old data are put out.

(1) Read/write address asynchronous transfer mode



(2) Read/write address synchronous transfer mode



- Mode programming
  Mode should not be reprogrammed with in 32 clocks from previous mode programming or system reset.
- Address should be set by read/write address asynchronous transfer or system reset after 100 μs from power on.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature (under bias)	Tbias	−10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	–	6.5	V
	V_{IL}	−1.0	–	0.8	V

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Operating Power Supply Current	I_{CC}	Min. cycle, Iout = 0 mA	–	40	60	mA
Input Leakage Current	I_{LI}	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, Vout = V_{SS} to V_{CC}	−10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 4.2 mA	–	–	0.4	V
	V_{OH}	I_{OH} = −2 mA,	2.4	–	–	V

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	Cin	Vin = 0 V	–	–	5	pF
Output Capacitance	Cout	Vout = 0 V	–	–	7	pF

Note) This parameter is sampled and not 100% tested.

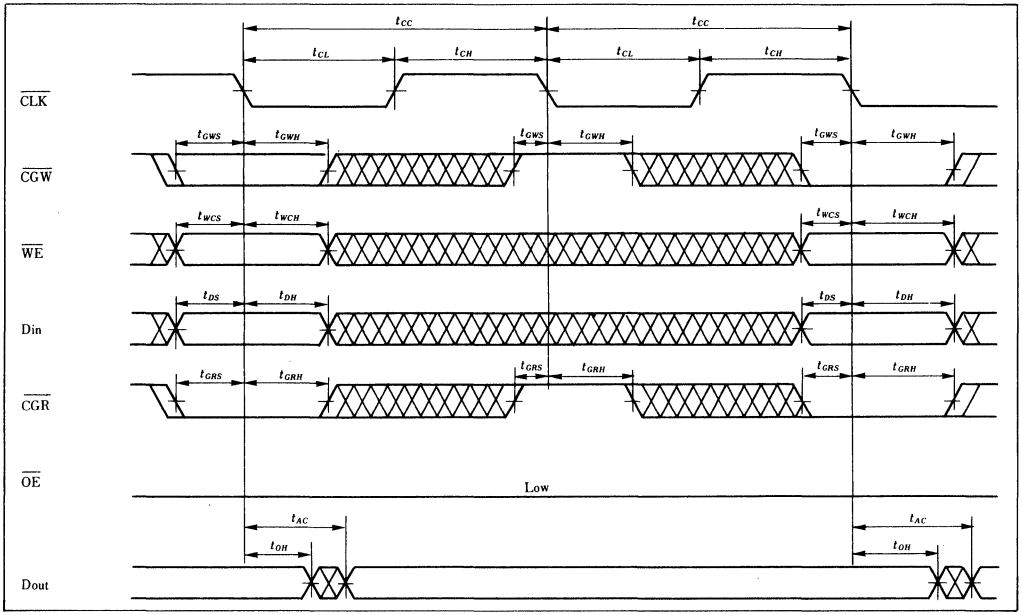
AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

AC Test Conditions

- Input and output timing reference levels: 1.5 V
- Input pulse levels: V_{SS} to 3 V
- Input rise and fall times: 5 ns
- Output Load: 2 TTL + 50 pF
  (Including scope and jig)

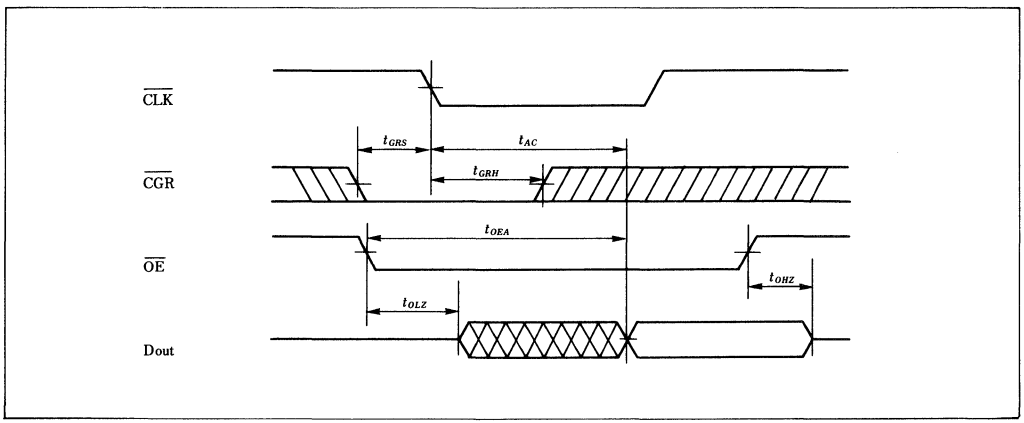
Parameter	Symbol	min	max	Unit
System Clock Cycle Time	t_{CC}	60	300	ns
$\overline{CLK}$ Pulse Width	t_{CL}	15	–	ns
	t_{CH}	15	–	ns
Access Time from $\overline{CLK}$	t_{AC}	–	40	ns
Output Hold Time	t_{OH}	5	–	ns
Output Enable Access Time	t_{OEA}	–	30	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	20	ns
$\overline{CGR}$ Setup Time	t_{GRS}	15	–	ns
$\overline{CGR}$ Hold Time	t_{GRH}	5	–	ns
$\overline{CGW}$ Setup Time	t_{GWS}	15	–	ns
$\overline{CGW}$ Hold Time	t_{GWH}	5	–	ns
Write Command Setup Time	t_{WCS}	15	–	ns
Write Command Hold Time	t_{WCH}	5	–	ns
Data Input Setup Time	t_{DS}	15	–	ns
Data Input Hold Time	t_{DH}	5	–	ns
$\overline{SAS}$ Cycle Time	t_{SC}	60	–	ns
$\overline{SAS}$ Pulse Width	t_{SL}	15	–	ns
	t_{SH}	15	–	ns
Serial Address Setup Time	t_{SAS}	15	–	ns
Serial Address Hold Time	t_{SAH}	5	–	ns
$\overline{SAS}$ Setup Time during Mode Programming	t_{SSH}	15	–	ns
$\overline{SAS}$ Hold Time during Mode Programming	t_{SHH}	5	–	ns
$\overline{TAS}$ Setup Time	t_{TS}	15	–	ns
$\overline{TAS}$ Hold Time	t_{TH}	5	–	ns
$\overline{SAS}$ Setup Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SSL}	15	–	ns
$\overline{SAS}$ Hold Time during System Reset by $\overline{SAS}$/$\overline{TAS}$	t_{SHL}	5	–	ns

Read/Write Cycle



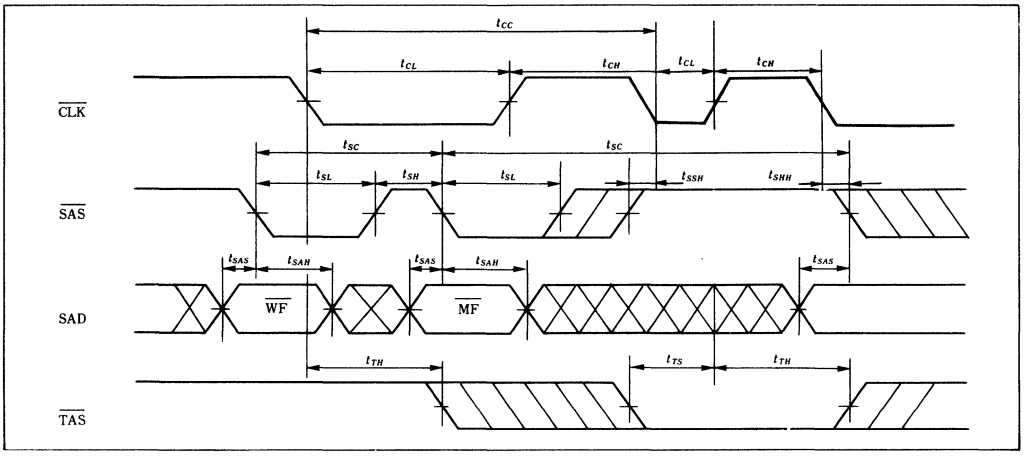
Notes) *1. Write Cycle starts when $\overline{CGW}$ is low and $\overline{WE}$ is low. Data are not written when $\overline{WE}$ is high. Time-compression mode is realized by controlling $\overline{CGW}$.
*2. Read cycle starts when $\overline{CGR}$ is low. Time-expansion mode is realized by controlling $\overline{CGR}$.

Read Cycle ($\overline{OE}$ control)



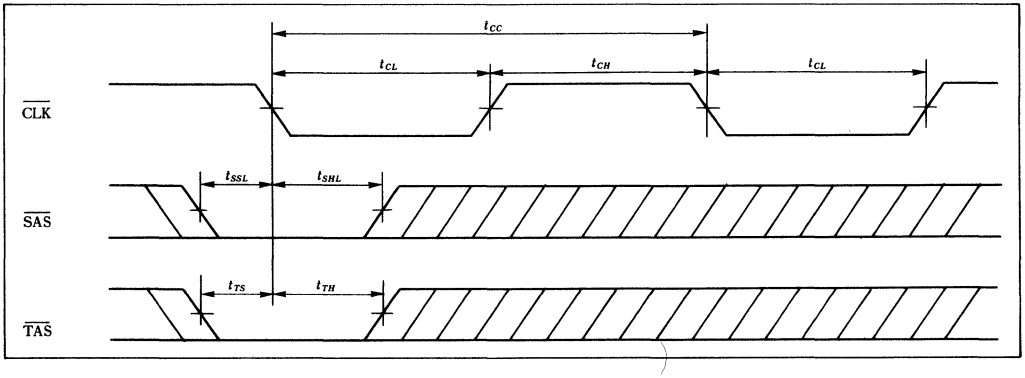
Notes) *1. t_{OHZ} is defined by the time at which the output achieves the open circuit condition.
*2. t_{OLZ} and t_{OHZ} are sampled and not 100% tested.

Mode Selection



Note) SAS operates asynchronously with $\overline{CLK}$. When $\overline{TAS}$ is low at the falling edge of the $\overline{CLK}$, the address transfer cycle starts. SAS should be high during the address transfer cycle.

$\overline{SAS}$, $\overline{TAS}$ Reset Mode



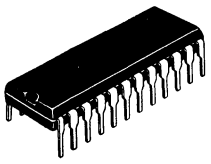
HM53461 Series

65,536-word x 4 bit Multi Port CMOS Dynamic Random Access Memory

The HM53461P is a 262, 144 bit multi port memory equipped with a 64k word x 4 bit Dynamic RAM port and a 256 word x 4 bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024 bit data register through a 256 word x 4 bit serial read or write access control. In the read data transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

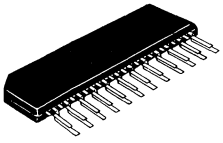
Utilizing the Hitachi 2μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

HM53461P Series



(DP-24A)

HM53461ZP Series



(ZP-24)

■ FEATURES

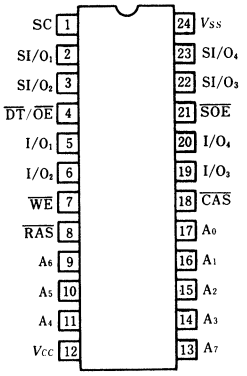
- Multi port organization
  (RAM; 64k word x 4 bit and SAM; 256 word x 4 bit)
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V (±10%)
- Low power Active RAM; 380mW max.
  SAM; 220mW max.
  Standby 40mW max.
- Access Time RAM; 100ns/120ns/150ns
  SAM; 40ns/40ns/60ns
- Cycle Time Random read or write cycle time (RAM)
  190ns/220ns/260ns
  Serial read or write cycle time (SAM)
  40ns/40ns/60ns
- TTL compatible
- 256 refresh cycles 4ms
- Refresh function $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh
- Data transfer operation (RAM⇄SAM)
- Fast serial access operation asynchronous from RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM53461P-10	100ns	400 mil 24 pin Plastic DIP
HM53461P-12	120ns	
HM53461P-15	150ns	
HM53461ZP-10	100ns	24 pin Plastic ZIP
HM53461ZP-12	120ns	
HM53461ZP-15	150ns	

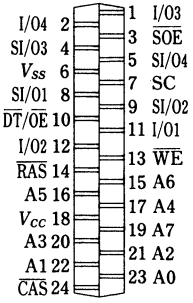
■ PIN ARRANGEMENT

● HM53461P Series



(Top View)

● HM53461ZP Series

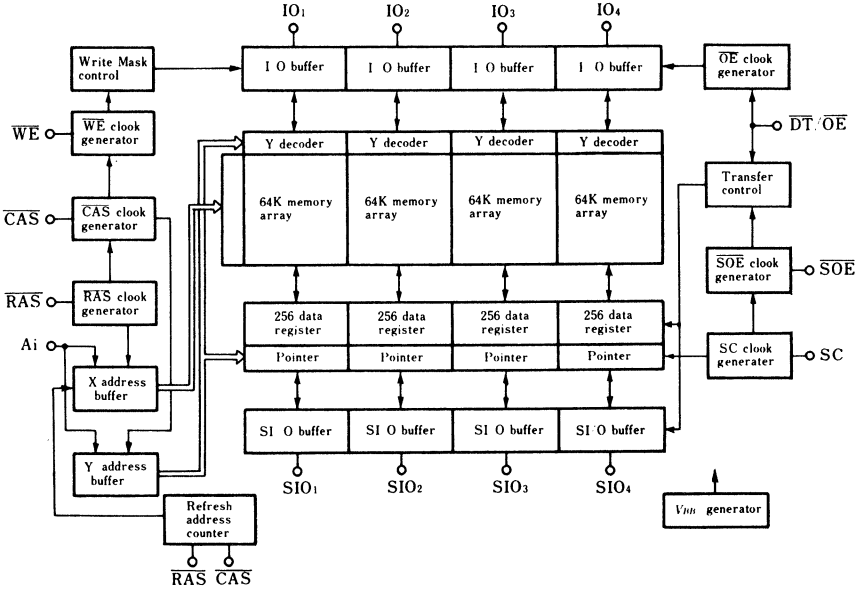


(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A0 – A7	Address Inputs
I/O1 – I/O4	RAM Port Data Input/Output
SI/O1 – SI/O4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



HITACHI

Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Power supply voltage relative to V_{SS} . . . . . -0.5V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	-1.0	–	0.8	V

Note: All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

RAM PORT	Symbol	SAM PORT		HM53461 -10	HM53461 -12	HM53461 -15	Unit
		Standby	Active				
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	O	X	70	60	50	mA
	I_{CC7}	X	O	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	O	X	7	7	7	mA
	I_{CC8}	X	O	40	40	30	mA
$\overline{RAS}$ only refresh current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min.	I_{CC3}	O	X	60	50	40	mA
	I_{CC9}	X	O	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	I_{CC4}	O	X	50	40	35	mA
	I_{CC10}	X	O	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	O	X	60	50	40	mA
	I_{CC11}	X	O	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	O	X	75	65	55	mA
	I_{CC12}	X	O	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{LI}	-10	10	μA
Output leakage	I_{LO}	-10	10	μA
Output high voltage I_{OH}=-2mA	V_{OH}	2.4	–	V
Output low voltage I_{OL}=4.2mA	V_{OL}	–	0.4	V

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	CI1	–	5	pF
Clocks	CI2	–	5	pF
I/O, SI/O	CI3	–	7	pF

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)[1), 10), 11)]

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
Read Modify Write Cycle Time	t_{RWC}	260	–	300	–	355	–	ns	
Page Mode Cycle Time	t_{PC}	70	–	85	–	105	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{RAS}$ Pulse Width (Read Modify Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	8
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	–	15	–	20	–	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	–	0	–	0	–	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	–	40	–	45	–	ns	
Serial Clock Cycle Time	t_{SCC}	40	–	40	–	60	–	ns	
Access Time from SC	t_{SCA}	–	40	–	40	–	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	–	25	–	30	–	40	ns	10
SC Pulse Width	t_{SC}	10	–	10	–	10	–	ns	

(to be continued)

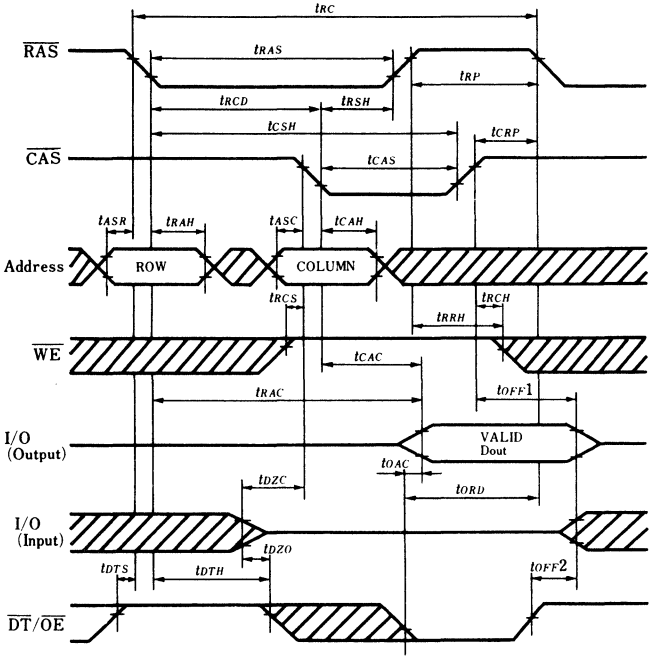
Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
SC Precharge Width	t_{SCP}	10	–	10	–	10	–	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	–	10	–	10	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Set-up Time	t_{SIS}	0	–	0	–	0	–	ns	
Serial Data-in Hold Time	t_{SIH}	15	–	20	–	25	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Set-up Time	t_{DTS}	0	–	0	–	0	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time(Read Data Transfer Cycle)	t_{RDH}	80	–	90	–	110	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	–	15	–	20	–	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	–	30	–	45	–	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	–	5	–	10	–	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	–	25	–	30	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	–	10	–	10	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Set-up Time	t_{WS}	0	–	0	–	0	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	–	15	–	20	–	ms	
I/O to $\overline{RAS}$ Set-up Time	t_{MS}	0	–	0	–	0	–	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	–	15	–	20	–	ns	
Serial Output Buffer Turn off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
$\overline{SC}$ to $\overline{RAS}$ Set-up Time	t_{SRS}	30	–	40	–	45	–	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	–	30	–	35	–	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	–	60	–	75	–	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Set-up Time	t_{ES}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	–	15	–	20	–	ns	
Serial Write Enable Set-up Time	t_{SWS}	0	–	0	–	0	–	ns	
Serial Write Enable Hold Time	t_{SWH}	35	–	35	–	55	–	ns	
Serial Write Disable Set-up Time	t_{SWIS}	0	–	0	–	0	–	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	–	35	–	55	–	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	–	10	–	10	–	ns	

Notes)

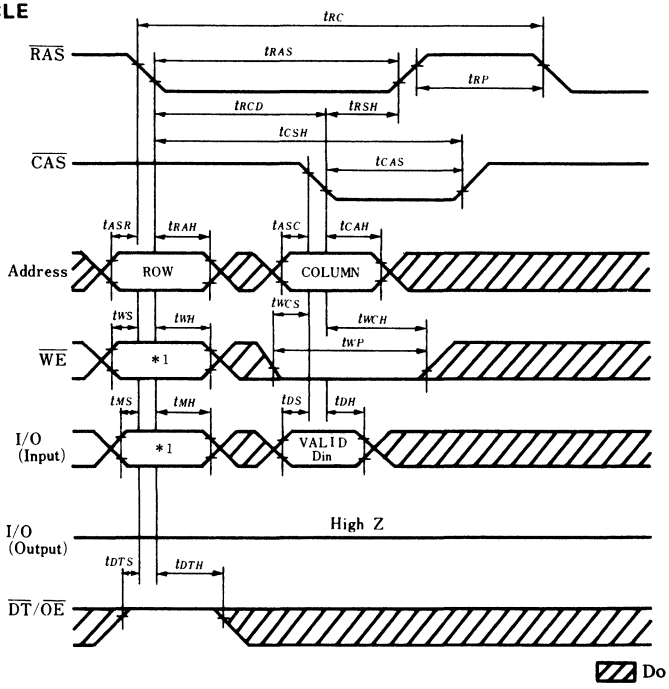
1. AC measurements assume t_T=5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
5. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD}(max) limit insures that t_{RAC} (max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50pF.
11. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

■ WAVE FORMS

• READ CYCLE

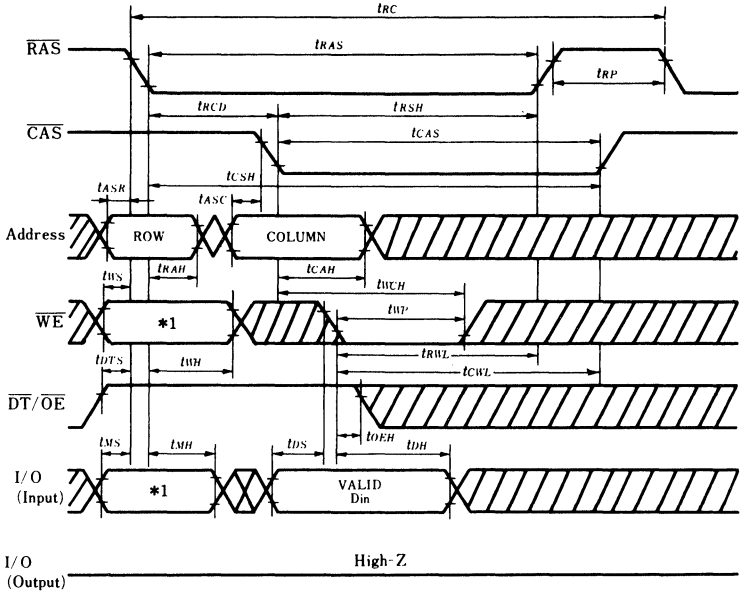


• EARLY WRITE CYCLE



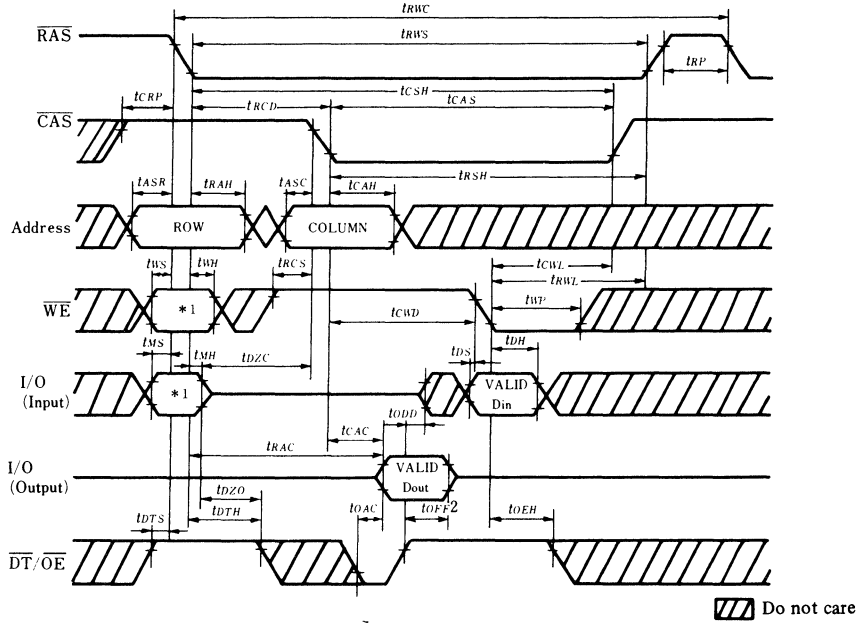
Note) *1. When $\overline{WE}$ is "H" level, the all data on the I/O can be written into the cell.
When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

• DELAYED WRITE CYCLE



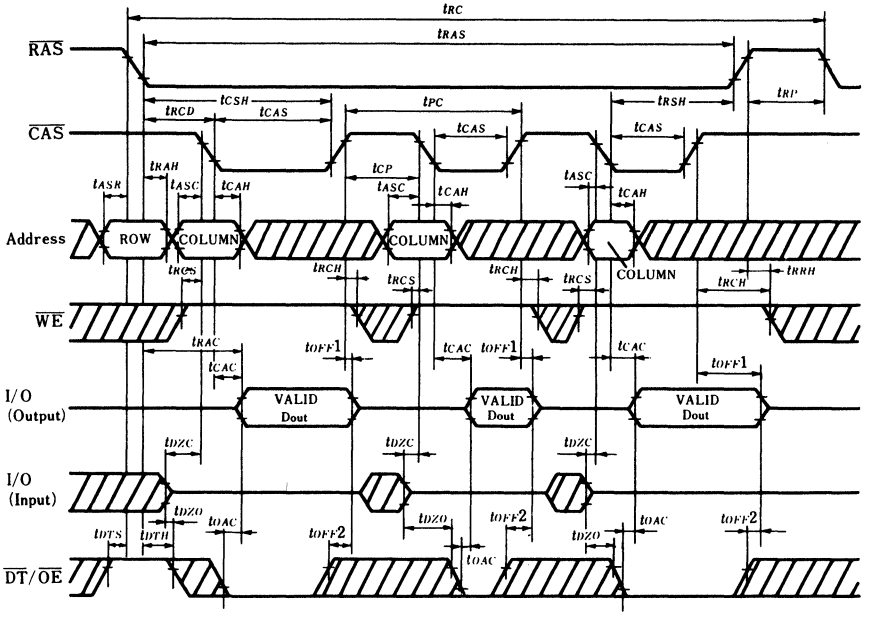
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written exept for when I/O="H" at the falling edge of $\overline{RAS}$.

• READ MODIFY WRITE CYCLE

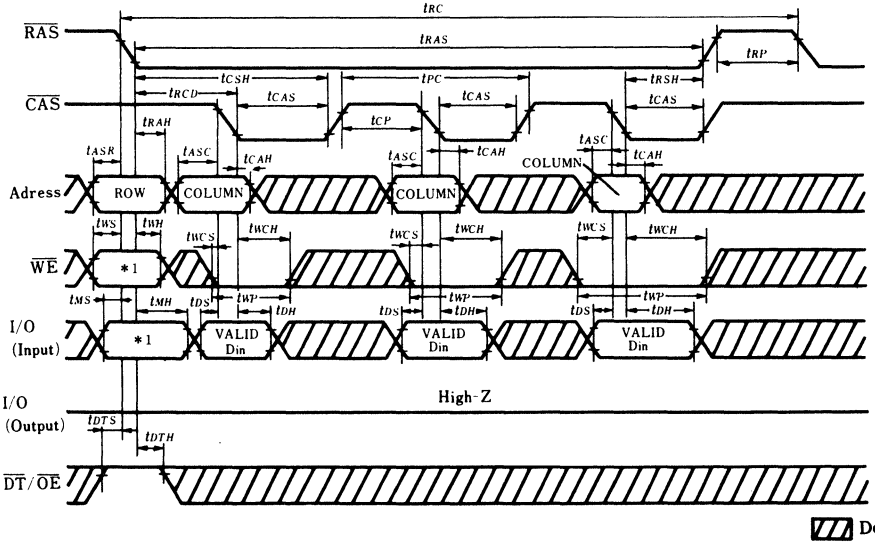


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE READ CYCLE

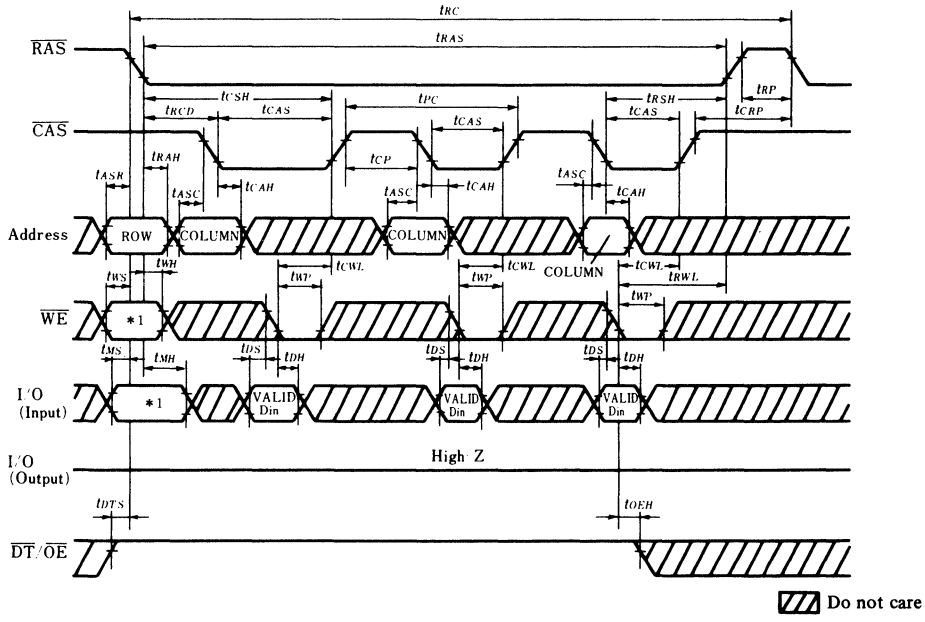


• PAGE MODE WRITE CYCLE (Early Write)



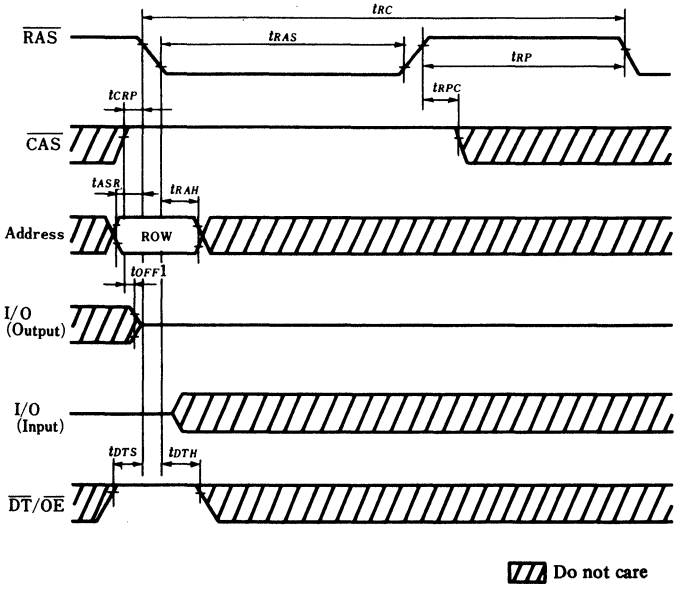
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Delayed Write)

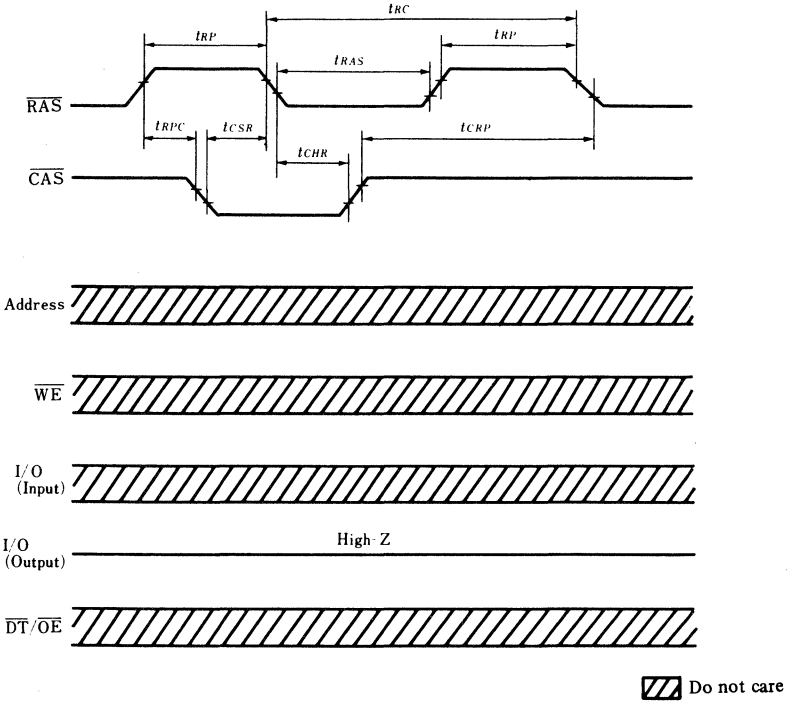


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

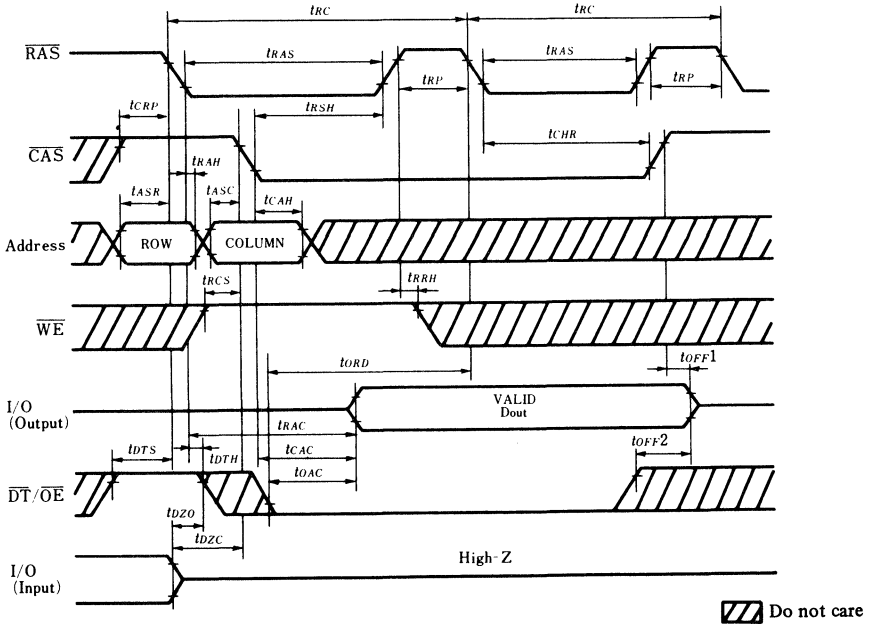
• $\overline{RAS}$ ONLY REFRESH CYCLE



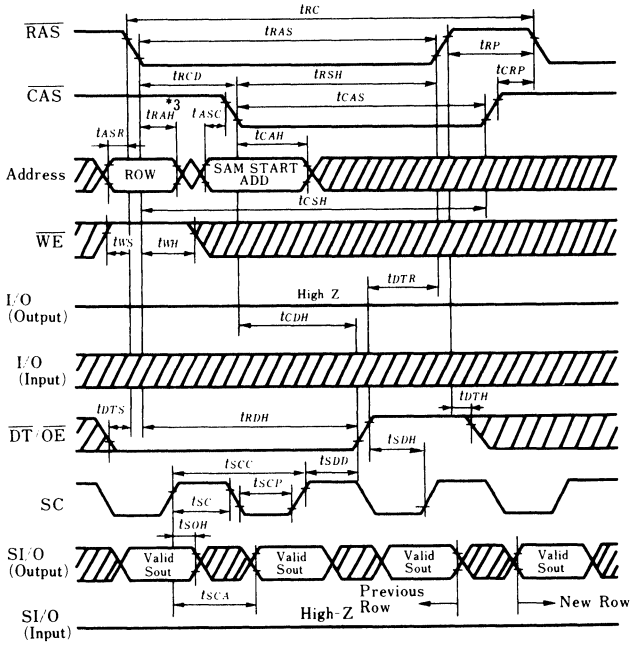
• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH



• HIDDEN REFRESH CYCLE



• READ DATA TRANSFER CYCLE (1)*1 *2



Note

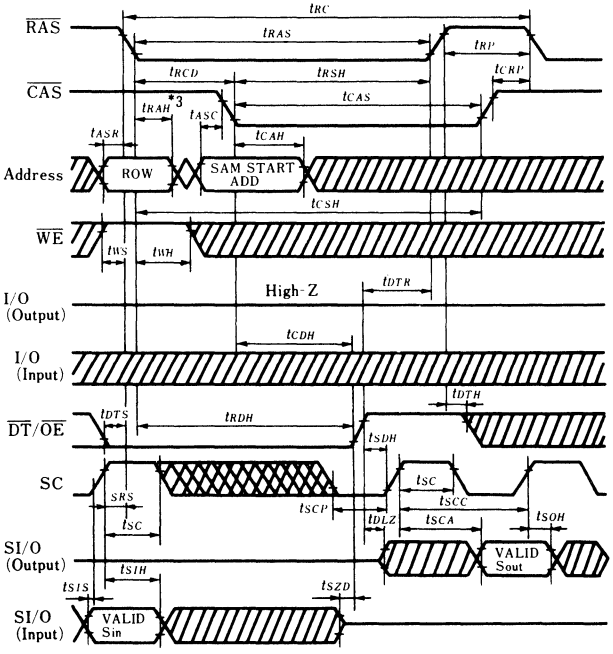
*1) In the case that the previous data transfer cycle was read data transfer.

*2) Assume that $\overline{SOE}$ is "L" level.

*3) $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

Do not care

• READ DATA TRANSFER CYCLE (2)*1,*2



Do not care

Inhibit rising transient

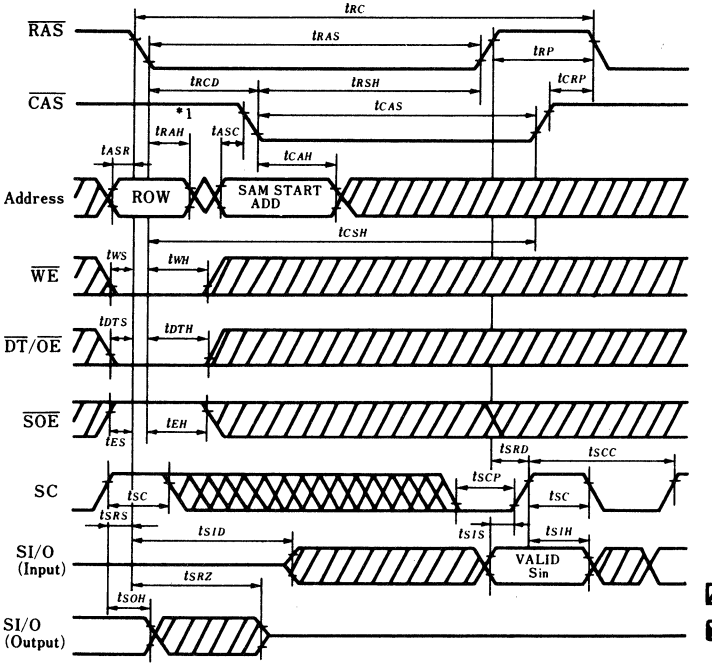
Note)

*1) In the case that the previous data transfer cycle was write data transfer or pseudo data transfer.

*2) Assume that $\overline{SOE}$ is "L" level,

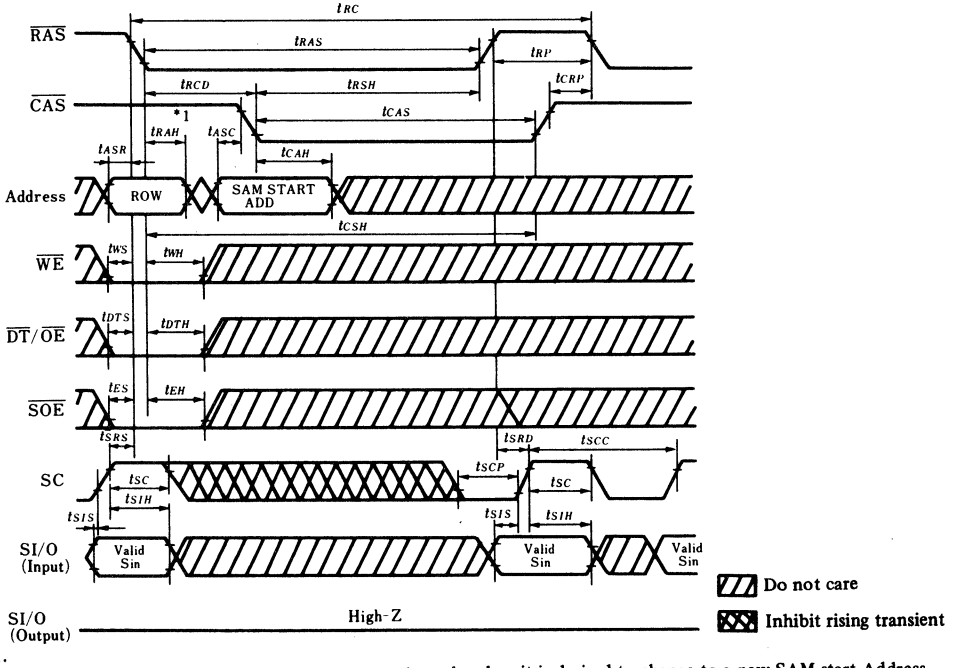
*3) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• PSEUDO DATA TRANSFER CYCLE



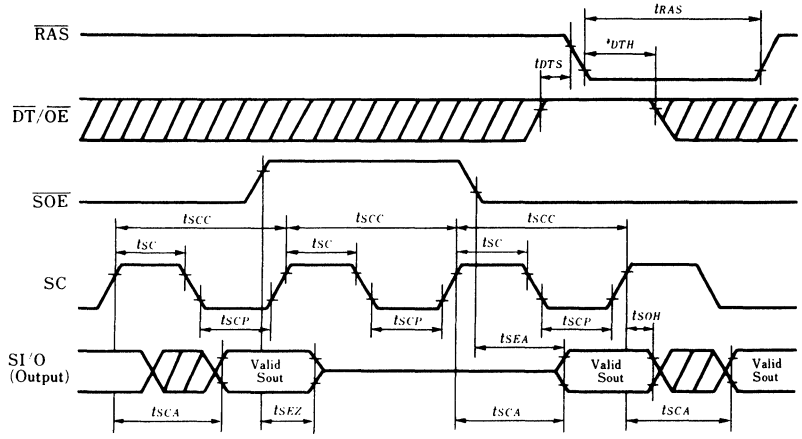
Note) *1.
$\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• WRITE DATA TRANSFER CYCLE



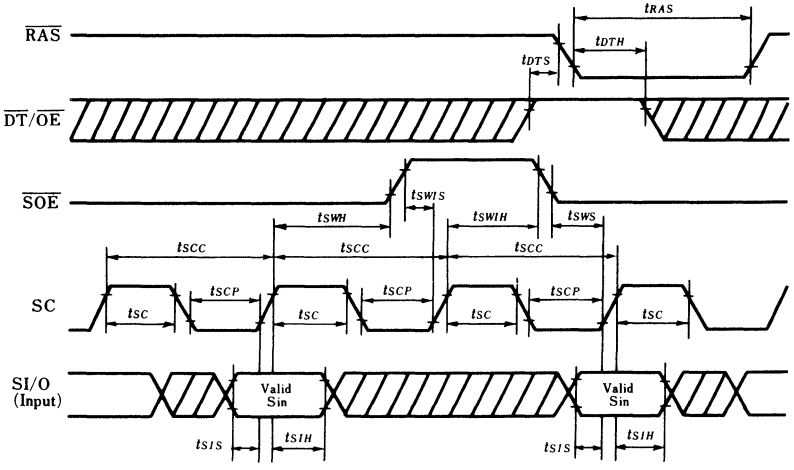
Note) *1.
$\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• SERIAL READ CYCLE



▨ Do not care

• SERIAL WRITE CYCLE



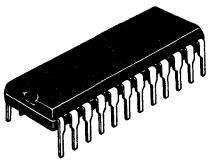
▨ Do not care

HM53462 Series

65,536-word x 4 bits Multi Port DRAM (with Logic operation mode)

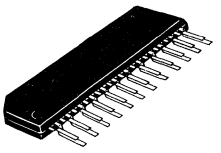
The HM53462P is a 262,144 bit multi port memory equipped with a 64k word x 4 bit Dynamic RAM port and a 256 word x 4 bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024 bit data register through a 256 word x 4 bit serial read or write access control. In the read data transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. RAM port has another new function, logic operation capability. By this function logic operation between memory data and input data can be done in one cycle. Utilizing the Hitachi 2μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

HM53462P Series



(DP-24A)

HM53462ZP Seires



(ZP-24)

■ FEATURES

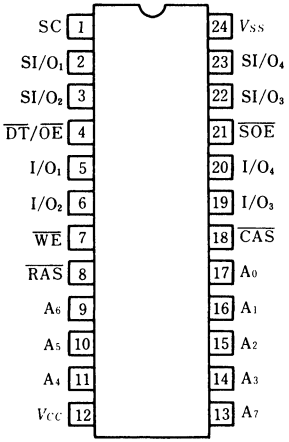
- Multi port organization
  (RAM; 64k word x 4 bit and SAM; 256 word x 4 bit)
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V (±10%)
- Low powr Active RAM; 380 mW max.
  SAM; 220 mW max.
  Standby 40 mW max.
- Access Time RAM; 100ns/120ns/150ns
  SAM; 40ns/40ns/60ns
- Cycle Time Random read or write cycle time (RAM)
  190ns/220ns/260ns
  Serial read or write cycle time (SAM)
  40ns/40ns/60ns
- TTL compatible
- 256 refresh cycles . . 4ms
- Refresh function $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh
- Bidirectional data transfer operation (RAM $\rightleftarrows$ SAM)
- Fast serial access operation asynchronous from RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability
- Logic operation capability between Din and Dout
- SAM organization can be changed to 1024 x 1

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM53462P-10 HM53462P-12 HM53462P-15	100ns 120ns 150ns	400 mil 24 pin Plastic DIP
HM53462ZP-10 HM53462ZP-12 HM53462ZP-15	100ns 120ns 150ns	24 pin Plastic ZIP

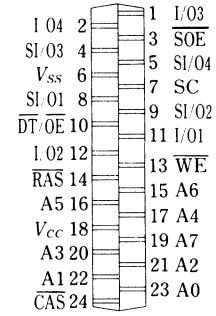
■ PIN ARRANGEMENT

● HM53462P Series



(Top View)

● HM53462ZP Series

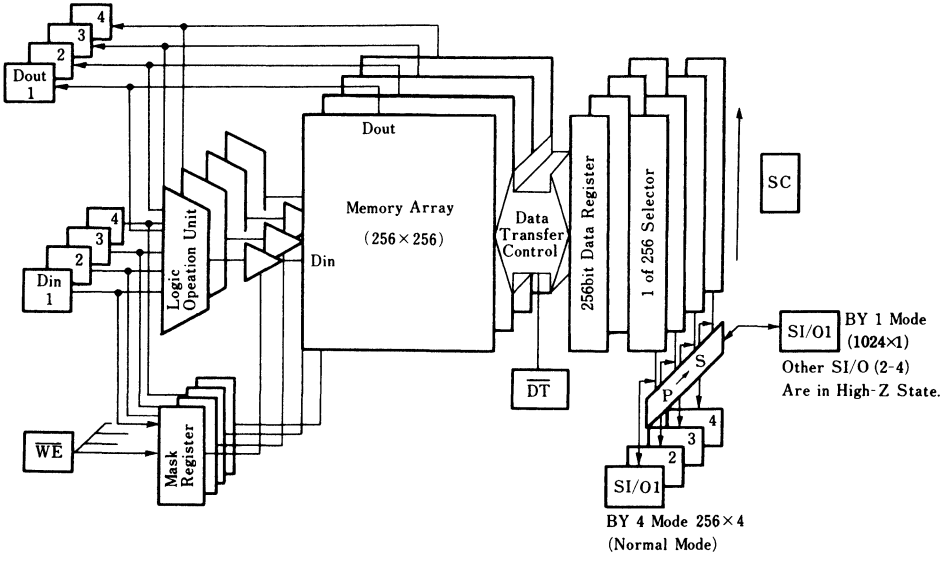


(Buttom View)

■ PIN DESCRIPTION

Pin Name	Function
A0 – A7	Address Inputs
I/O1 – I/O4	RAM Port Data Input/Output
SI/O1 – SI/O4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Power supply voltage relative to V_{SS} . . . . . -0.5V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	CI_1	–	5	pF
Clocks	CI_2	–	5	pF
I/O, SI/O	CI_3	–	7	pF

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

RAM PORT	Symbol	SAM PORT		HM53462 −10	HM53462 −12	HM53462 −15	Unit
		Standby	Active				
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	○	×	70	60	50	mA
	I_{CC7}	×	○	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	○	×	7	7	7	mA
	I_{CC8}	×	○	40	40	30	mA
RAS only refresh current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min.	I_{CC3}	○	×	60	50	40	mA
	I_{CC9}	×	○	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	I_{CC4}	○	×	50	40	35	mA
	I_{CC10}	×	○	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	○	×	60	50	40	mA
	I_{CC11}	×	○	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	○	×	75	65	55	mA
	I_{CC12}	×	○	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{LI}	−10	10	μA
Output leakage	I_{LO}	−10	10	μA
Output high voltage I_{OH} = −2 mA	V_{OH}	2.4	–	V
Output low voltage I_{OL} = 4.2 mA	V_{OL}	–	0.4	V

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1), 10), 11)]

Parameter	Symbol	HM53462 −10		HM53462 −12		HM53462 −15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
Read Modify Write Cycle Time	t_{RWC}	260	–	300	–	355	–	ns	
Page Mode Cycle Time	t_{PC}	70	–	85	–	105	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{RAS}$ Pulse Width (Read Modify Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	8
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	–	15	–	20	–	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	–	0	–	0	–	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	–	40	–	45	–	ns	

(to be continued)

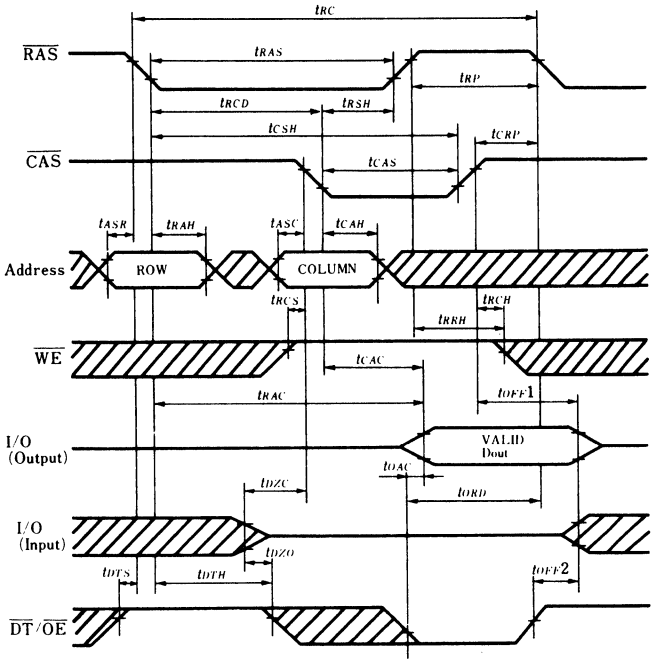
Parameter	Symbol	HM53462 -10		HM53462 -12		HM53462 -15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Serial Clock Cycle Time	t_{SCC}	40	–	40	–	60	–	ns	
Access Time from SC	t_{SCA}	–	40	–	40	–	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	–	25	–	30	–	40	ns	10
SC Pulse Width	t_{SC}	10	–	10	–	10	–	ns	
SC Precharge Width	t_{SCP}	10	–	10	–	10	–	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	–	10	–	10	–	ns	
Serial Output Buffer Turn-off Delay from SOE	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Set-up Time	t_{SIS}	0	–	0	–	0	–	ns	
Serial Data-in Hold Time	t_{SIH}	15	–	20	–	25	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Set-up Time	t_{DTS}	0	–	0	–	0	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Data Transfer Cycle)	t_{RDH}	80	–	90	–	110	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	–	15	–	20	–	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	–	30	–	45	–	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	–	5	–	10	–	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	–	25	–	30	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	–	10	–	10	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Set-up Time	t_{WS}	0	–	0	–	0	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	–	15	–	20	–	ns	
I/O to $\overline{RAS}$ Set-up Time	t_{MS}	0	–	0	–	0	–	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	–	15	–	20	–	ns	
Serial Output Buffer Turn off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
SC to $\overline{RAS}$ Set-up Time	t_{SRS}	30	–	40	–	45	–	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	–	30	–	35	–	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	–	60	–	75	–	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Set-up Time	t_{ES}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	–	15	–	20	–	ns	
Serial Write Enable Set-up Time	t_{SWS}	0	–	0	–	0	–	ns	
Serial Write Enable Hold Time	t_{SWH}	35	–	35	–	55	–	ns	
Serial Write Disable Set-up Time	t_{SWIS}	0	–	0	–	0	–	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	–	35	–	55	–	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	–	10	–	10	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50 pF.
11. After power-up, pause for more than 100μs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of $\overline{RAS}$, $\overline{WE}$ = "Low" and I/O1 – I/O = "High"), and execute one or more transport cycle for initiation of SAM port.

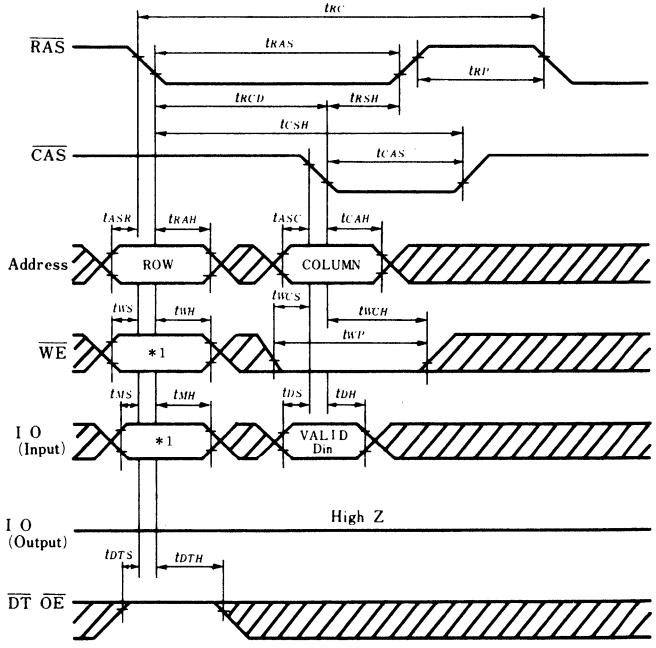
■ WAVE FORMS

• READ CYCLE



▨ Do not care

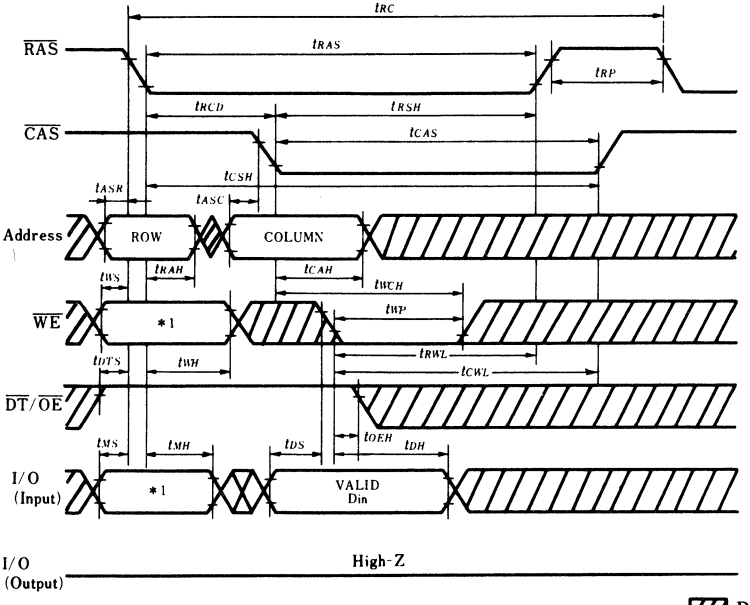
• EARLY WRITE CYCLE



▨ Do not care

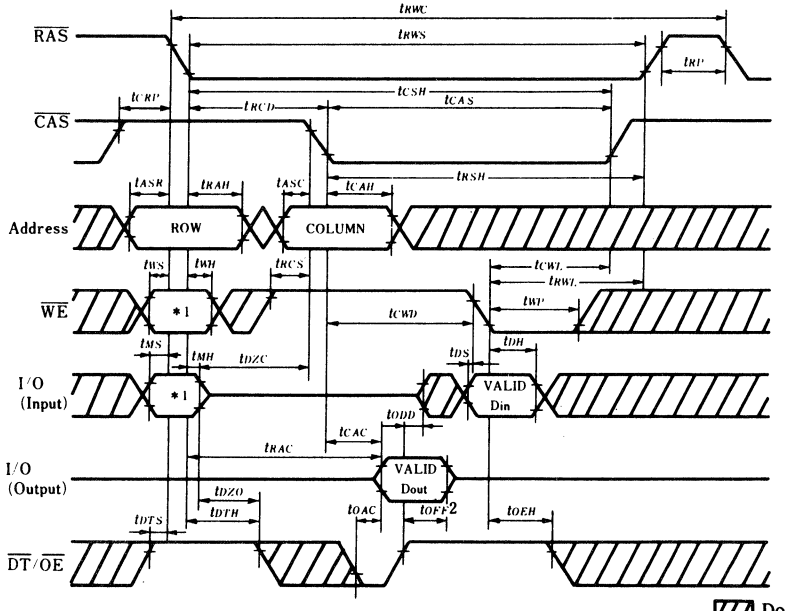
Note) *1. When $\overline{WE}$ is "H" level, the all data on the I/O can be written into the cell. When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is "H" level at the falling edge of $\overline{RAS}$.

• DELAYED WRITE CYCLE



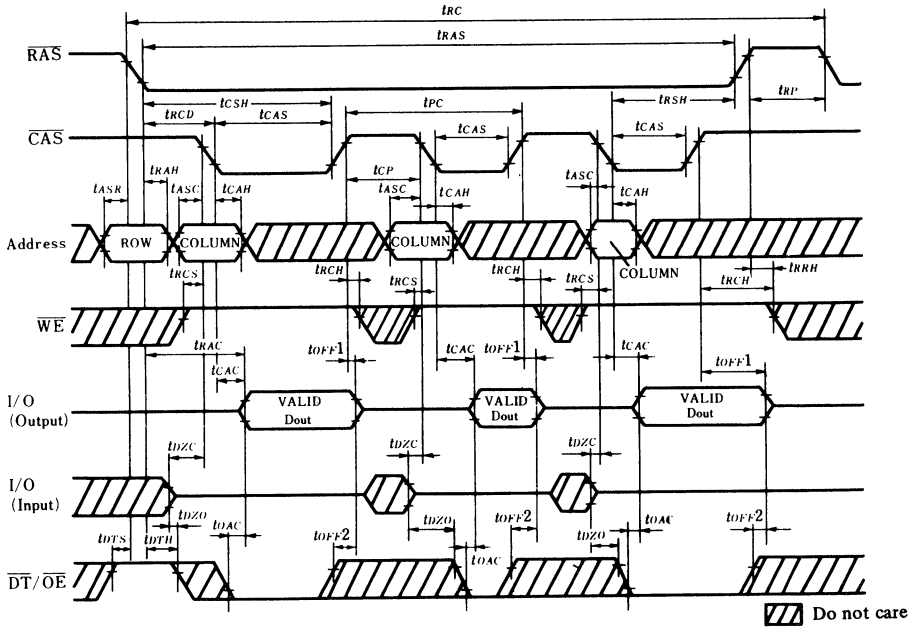
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• READ MODIFY WRITE CYCLE

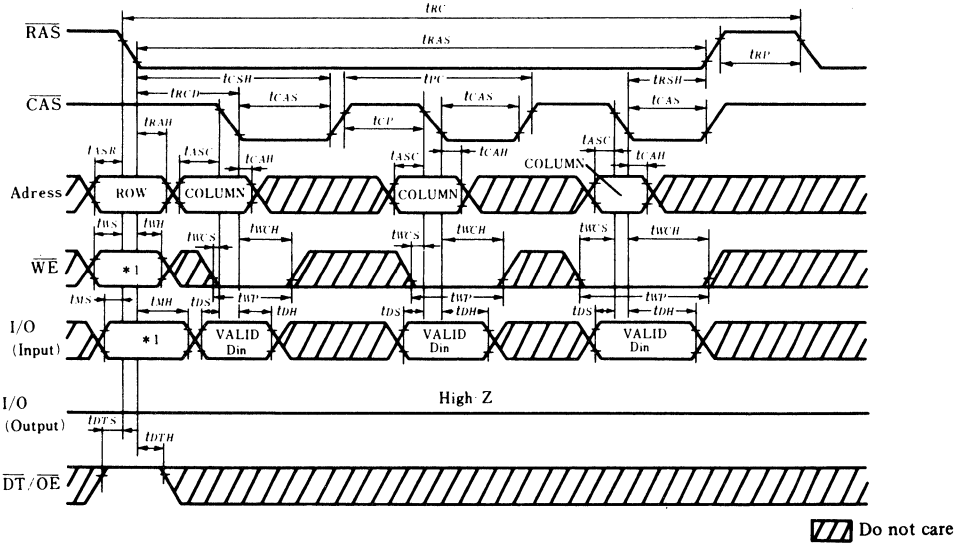


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• PAGE MODE READ CYCLE

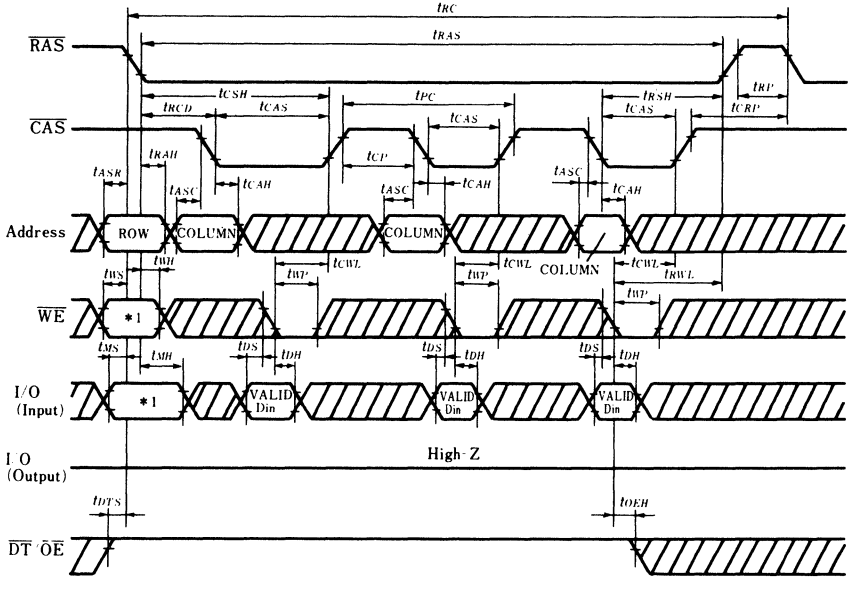


• PAGE MODE WRITE CYCLE (Early Write)



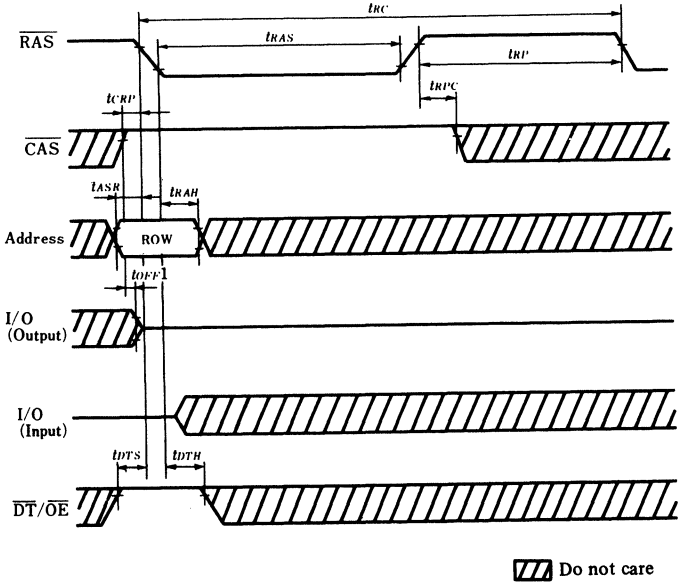
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Delayed Write)

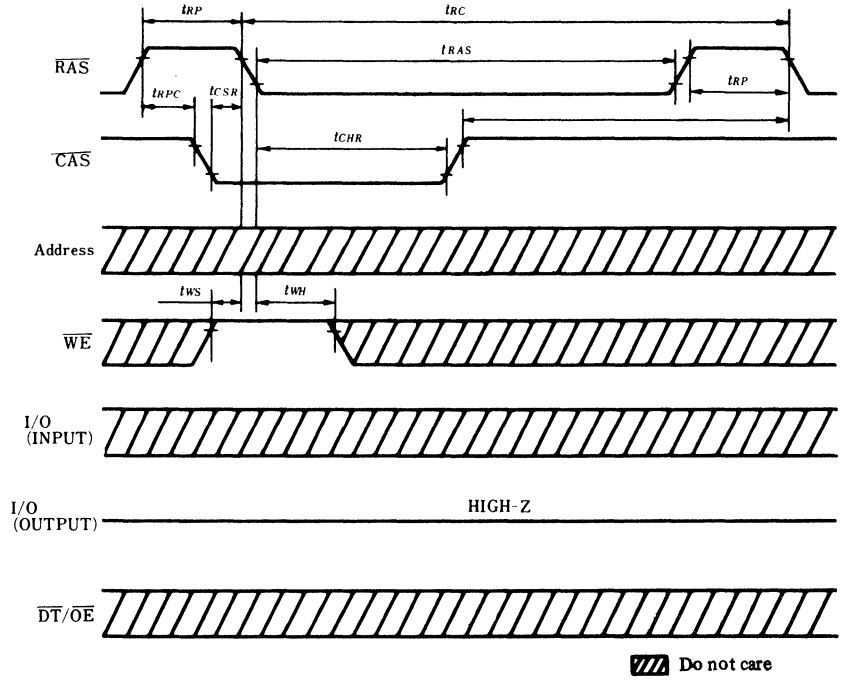


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

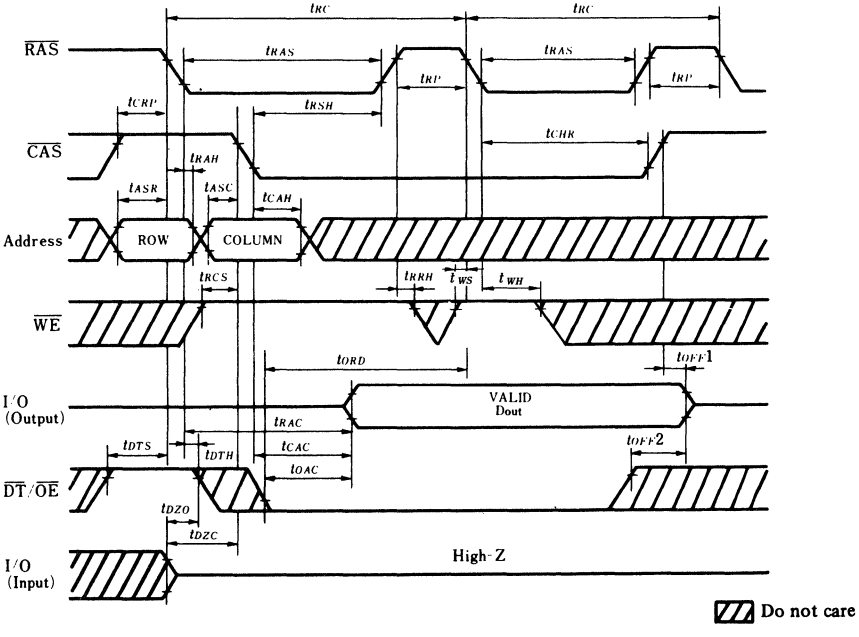
• $\overline{RAS}$ ONLY REFRESH CYCLE



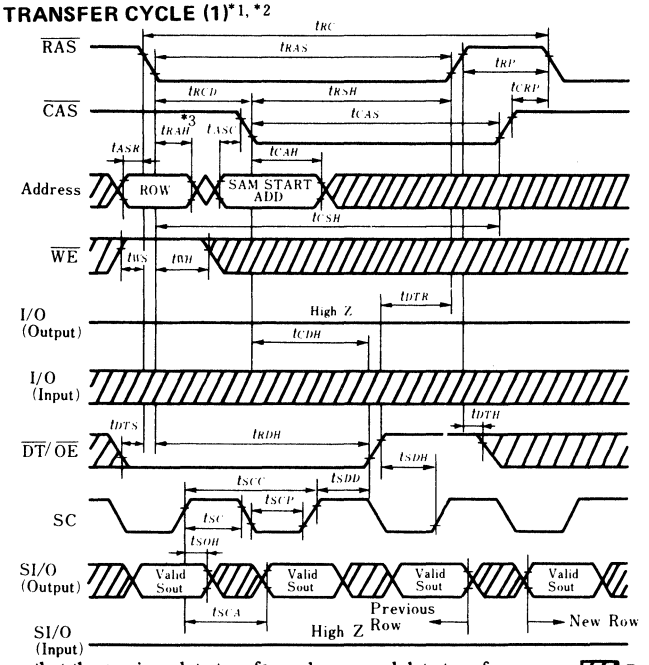
• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



• HIDDEN REFRESH CYCLE



• READ DATA TRANSFER CYCLE (1)*1, *2

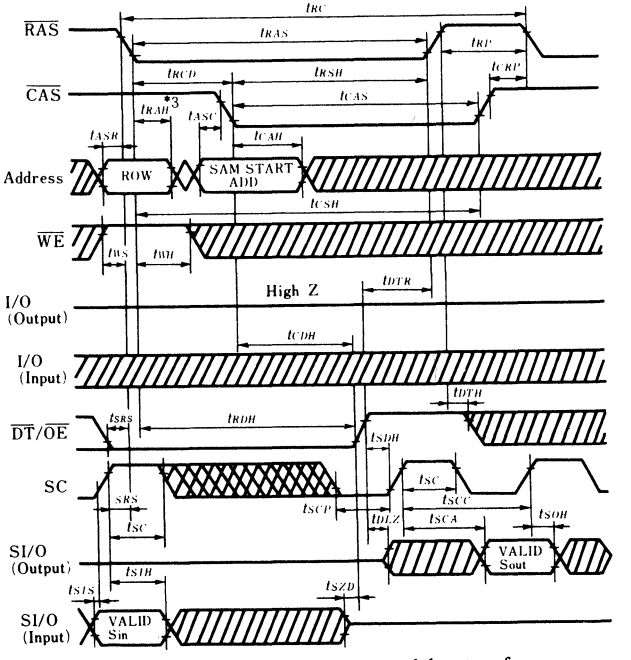


NOTE *1) In the case that the previous data transfer cycle was read data transfer. ▨ Do not care

*2) Assume that $\overline{SOE}$ is "Low".

*3) $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• READ DATA TRANSFER CYCLE (2)*1, *2



▨ Do not care

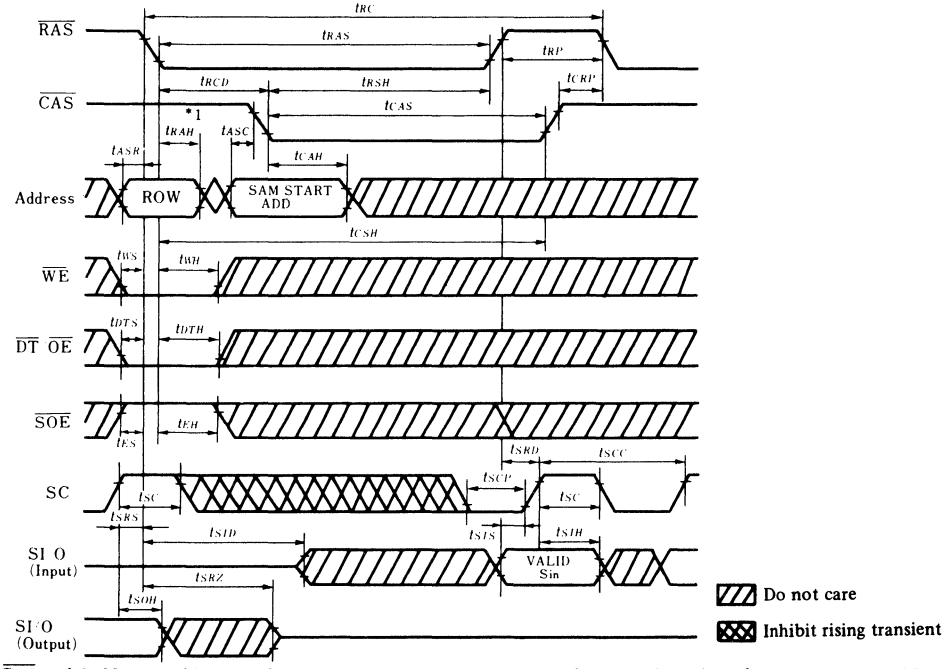
▩ Inhibit rising transient

NOTE *1) In the case that the previous data transfer cycle was read data transfer.

*2) Assume that $\overline{SOE}$ is "Low"

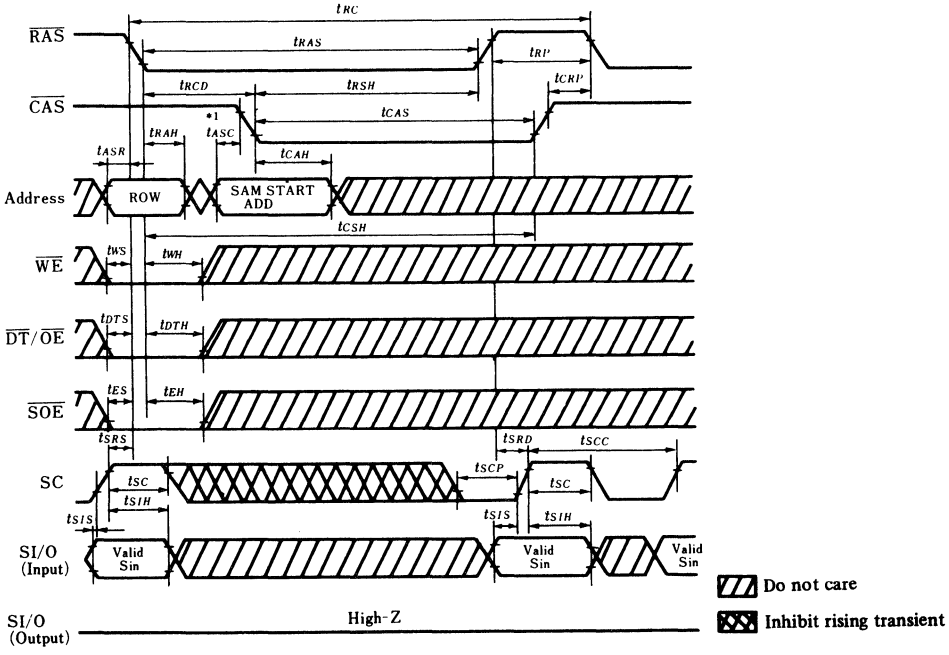
*3) $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new $\overline{SAM}$ start Address.

• PSEUDO DATA TRANSFER CYCLE



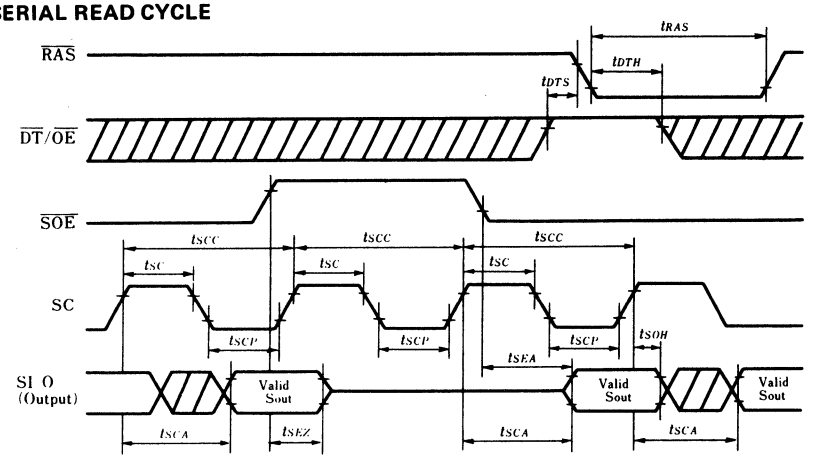
*1) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• WRITE DATA TRANSFER CYCLE

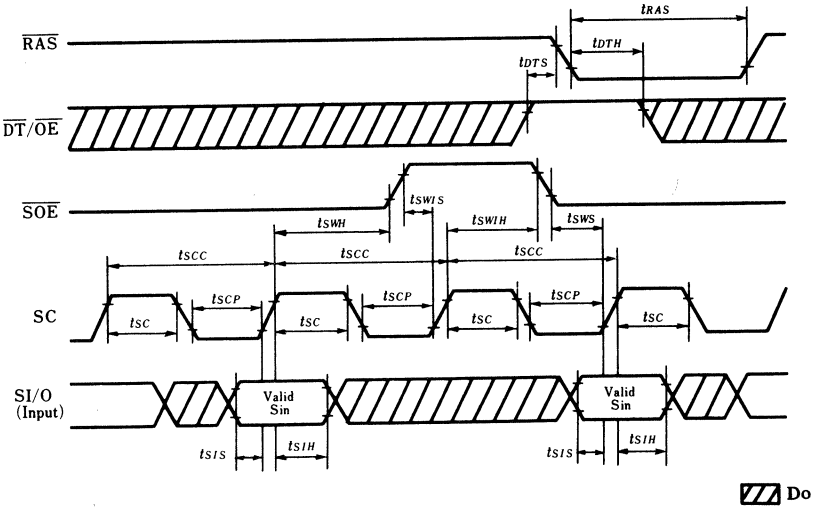


*1) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• SERIAL READ CYCLE



• SERIAL WRITE CYCLE



■ ELECTRICAL AC CHARACTERISTICS (Logic operation mode)

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{FRC}	230	–	265	–	310	–	ns
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	165	10000	200	10000	ns
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	80	10000	95	10000	105	10000	ns
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	–	165	–	200	–	ns
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	80	–	95	–	105	–	ns
Page mode cycle time (Write cycle)	t_{FPC}	100	–	120	–	135	–	ns
$\overline{CAS}$ hold time (Logic operation set/reset cycle)	t_{FCHR}	90	–	100	–	120	–	ns
$\overline{CAS}$ hold time from RAS precharge ($X_4 \rightarrow X_1$ set cycle)	t_{PSCH}	0	–	0	–	0	–	ns

■ LOGIC CODE (FC0 ~ 3 are AX0 ~ AX3 in Logic Operation Set Cycle)

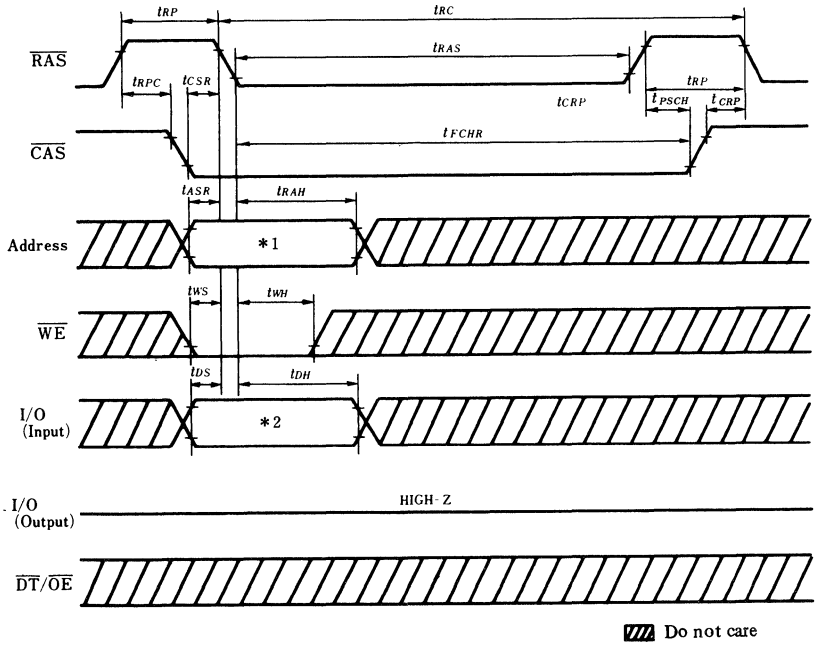
FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	X4 →X1	–
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

Di : External Data-in
Mi : The data of the memory cell

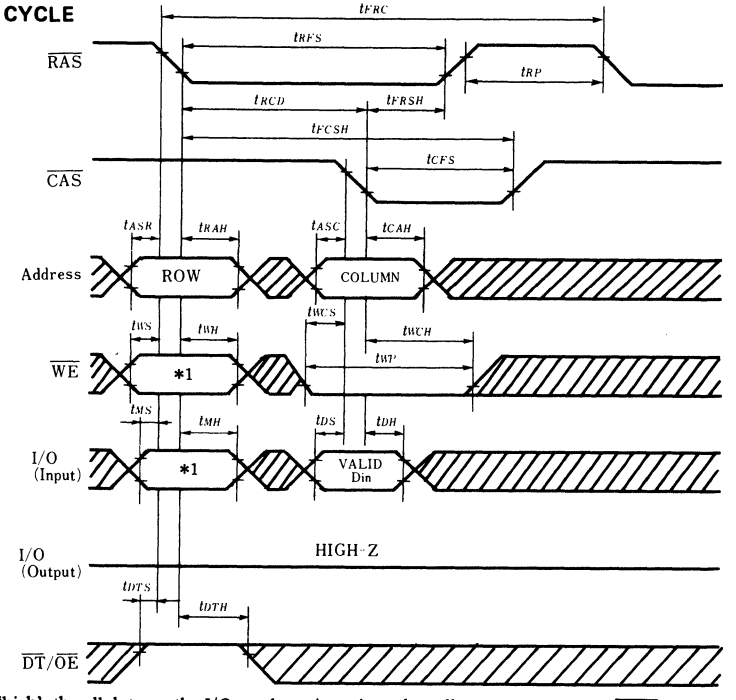
● LOGIC OPERATION SET/RESET CYCLE (With $\overline{CAS}$ before $\overline{RAS}$ refresh)



*1) Logic code A0-A3 (A4-A7: don't care)
*2) Write mask data

■ LOGIC OPERATION MODE

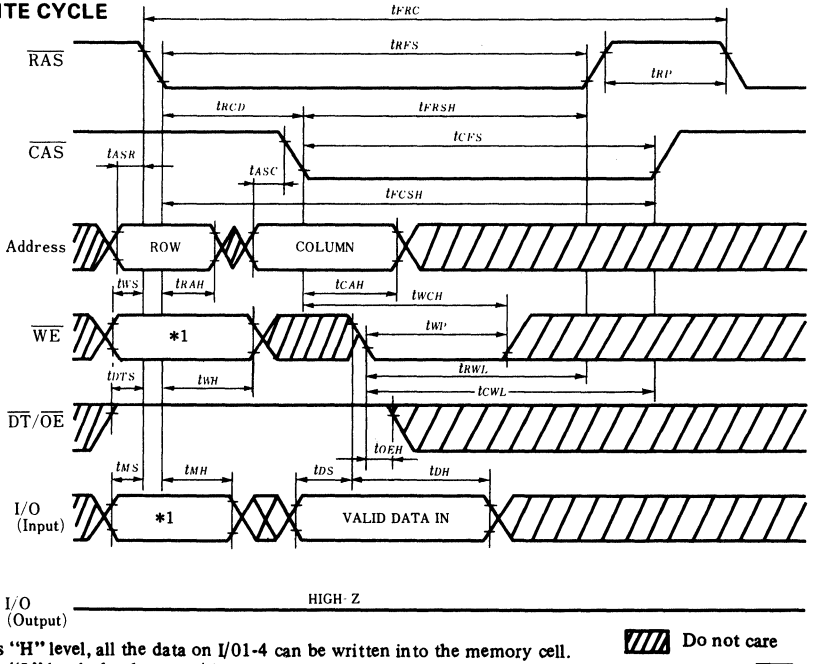
• EARLY WRITE CYCLE



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

▨ Do not care

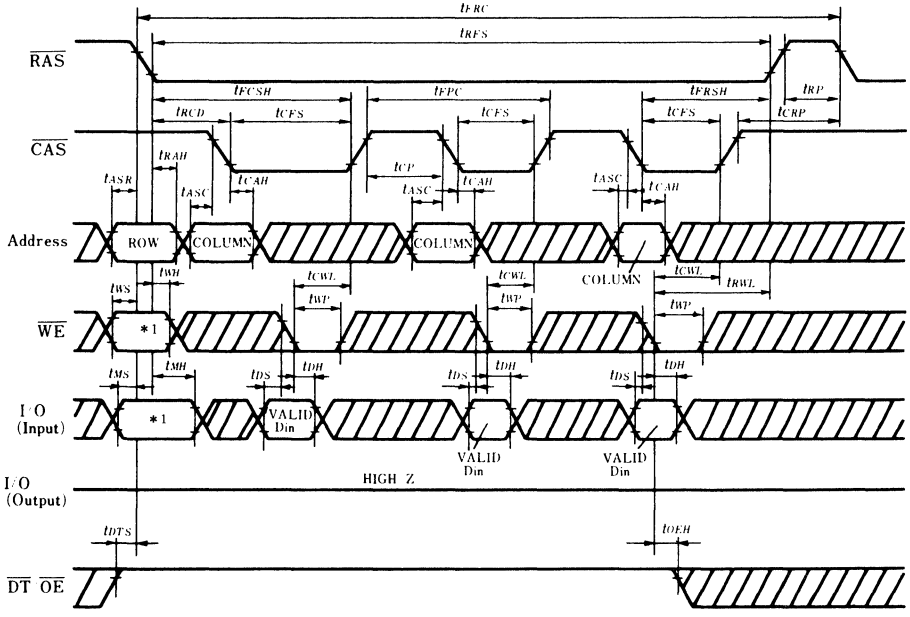
• DELAYED WRITE CYCLE



NOTE 1) When $\overline{WE}$ is "H" level, all the data on I/01-4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

▨ Do not care

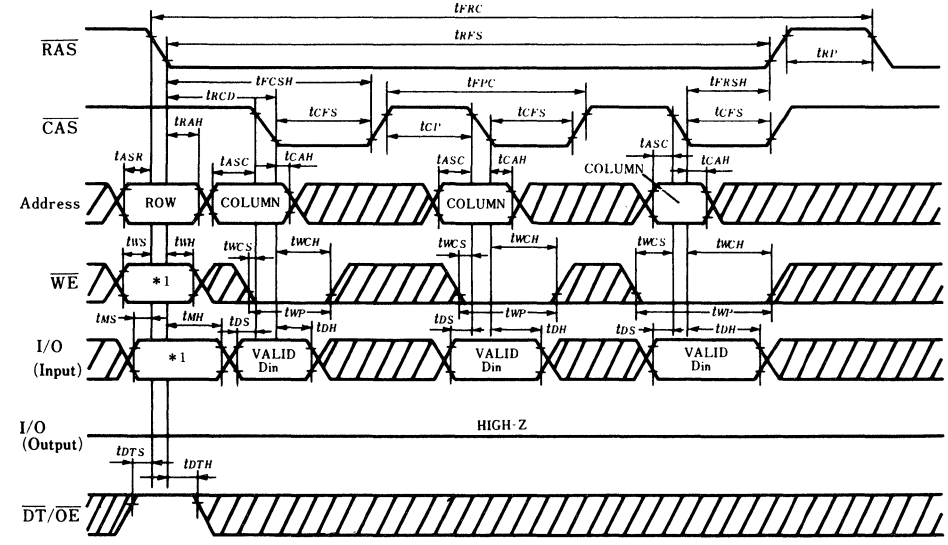
- **PAGE MODE WRITE CYCLE** (Delayed Write)



Do not care

Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

- **PAGE MODE WRITE CYCLE** (Early Write)



Do not care

Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

■ DESCRIPTION

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between Din and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (Fig. 1). The logic code and the bits to be masked are determined respectively by Ax0-3 state and I/01-4 state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle $\overline{CAS}$ before $\overline{RAS}$ refresh operation is executed, too. In the case of executing the conventional $\overline{CAS}$ before $\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

2.1. Logic code

The logic code is shown in Table 1. When power is turned on, the logic code is initialized to "THROUGH". If the logic code is (Ax3, Ax2, Ax1, Ax0) = (0, 0, 1, 1), the SAM organization is changed to 1,024 x 1 using the internal parallel to serial converter (Fig. 2). In the case that the SAM organization is changed to 1,024 x 1, one data transfer cycle is needed to initialize the SAM selector.
Once the SAM organization is changed to 1024 x 1, this code is maintained unless power is turned off.

2.2. Write mask

HM35462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

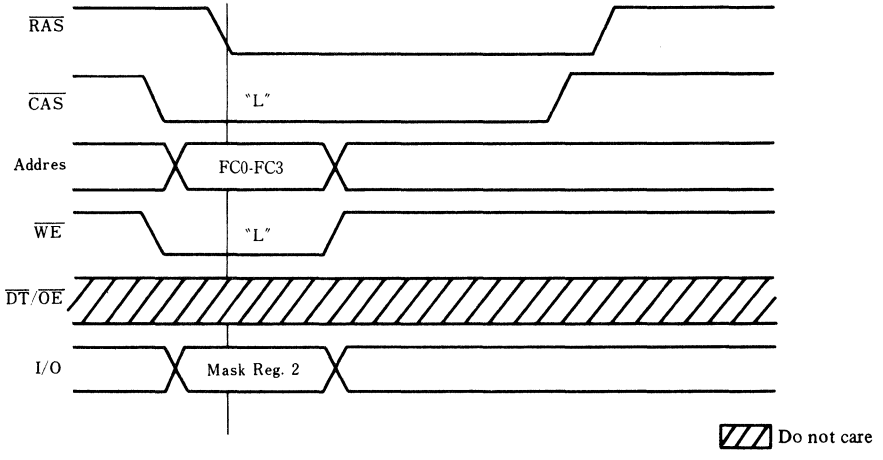


Fig. 1 LOGIC OPERATION SET/RESET CYCLE

Table 1. LOGIC CODE (FC0 – FC3 are AX0 – AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	X4 →X1	–
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + Di \cdot Mi$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

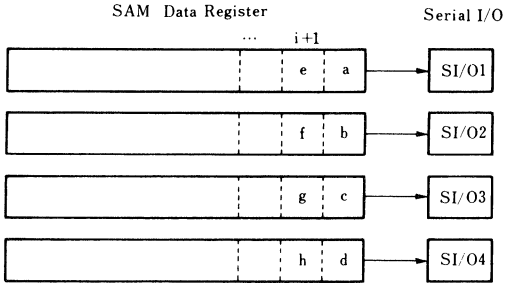
→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

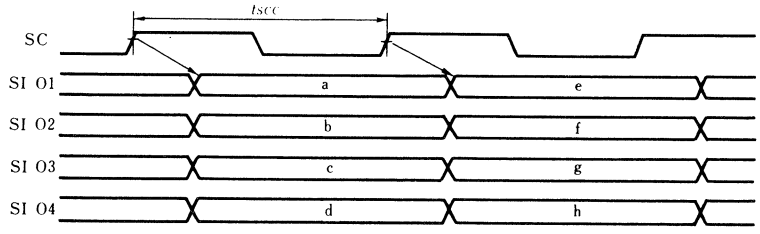
Di : External Data-in

Mi : The data of the memory cell

Fig. 2 THE SHIFT WAY OF SAM DATA



1) By 4 mode (SAM organization: 256 x 4)



2) By 1 mode (SAM organization: 1024 x 1)

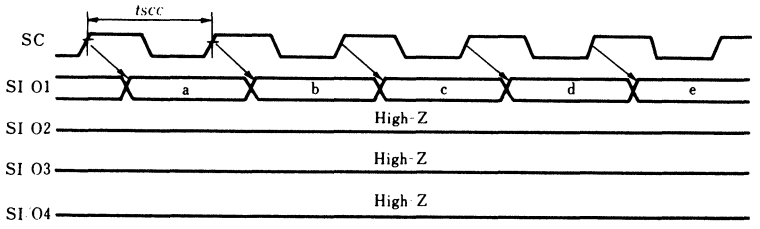


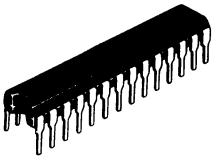
Fig. 3 EXAMPLE OF LOGIC OPERATION MODE

	Logic operation set/reset cycle	Write cycle	Write cycle	Write cycle	Write cycle
$\overline{RAS}$					
$\overline{CAS}$	"L"	"H"	"H"	"H"	"H"
$\overline{WE}$	"L"	"H"	"L"	"H"	"H"
I/O1		"0" Write	Masked	"1" Write	"0" Write
I/O2		Masked	"1" Write	Masked	Masked
I/O3		Masked	"0" Write	Masked	Masked
I/O4		"1" Write	Masked	"0" Write	"1" Write
Logic	—	AND1		AND1	AND1
	Mask reg.2 is set I O2,3 :Masked Assume that the logic is set to "AND1".		Mask reg.1 is set, and valid only in this cycle. I O1,4:Masked		

HM63021 Series

2048-word x 8-bit Line Memory

HM63021 is a 2048-word x 8-bit static Serial Access Memory (SAM) with separate data inputs and outputs. Owing to internal address counter, no address signal from outside is required and internal addresses are scanned serially. Using five different address scan modes, it is applicable to FIFO memory, double speed conversion, 1H delay line and 1H/2H delay line for digital TV signals. The minimum cycle times are 28 ns and 34 ns, each of which corresponds to 8 fsc of PAL TV signal and NTSC TV signal. All inputs and outputs are compatible with TTL. This device is packaged in 300 mil dual-in-line plastic package.



(DP-28N)

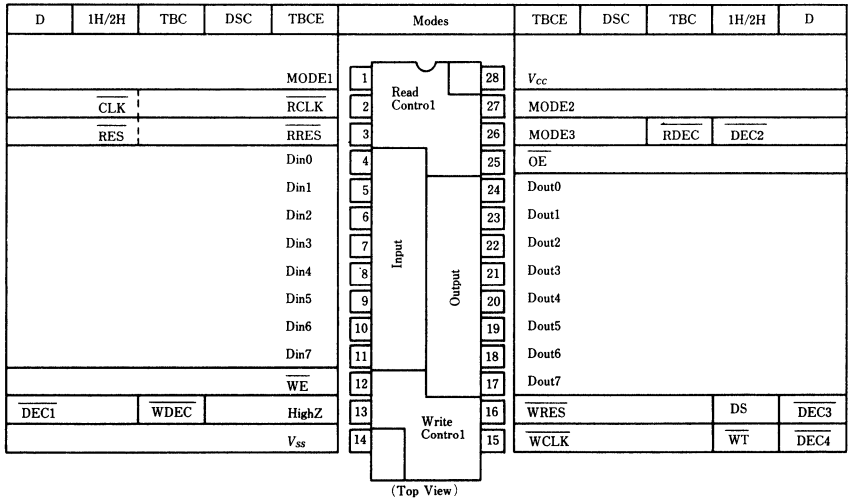
Features

- Five modes for various applications
- Corresponding to Digital TV system of 4 fsc sampling (PAL, NTSC)
- Decoder signal output pin; Fewer external circuits
- Asynchronous Read/Write operation;
  Separate address counters for Read/Write
  No Address Input required
- High Speed; Cycle Time 28/34 ns (min)
- Completely Static Memory; No refresh required
- x8-bit SAM with separate I/O
- Low Power; 250 mW typ. Active
- Single 5 V supply
- TTL compatible

Ordering Information

Type No.	Cycle Time	Package
HM63021P-28	28 ns	300 mil 28 pin Plastic DIP
HM63021P-34	34 ns	

Pin Arrangement



(Top View)

Pin Description

Pin No.	Pin Name	Functions
1	MODE1	Mode Input 1 (All Modes)
2	$\overline{\text{RCLK}}/\overline{\text{CLK}}$	Read Clock Input (TBCE, DSC, TBC) Clock Input (1H/2H, D)
3	$\overline{\text{RRES}}/\overline{\text{RES}}$	Read Reset Input (TBCE, DSC, TBC) Reset Input (1H/2H, D)
4-11	Din 0 – Din 7	Data Inputs (All Modes)
12	$\overline{\text{WE}}$	Write Enable Input (All Modes)
13	High Z/$\overline{\text{WDEC}}/\overline{\text{DEC1}}$	High Impedance (TBCE, DSC) Write Decode Pulse Output (TBC) Decode Pulse Output 1 (1H/2H, D)
14	V_{SS}	Ground (All Modes)
15	$\overline{\text{WCLK}}/\overline{\text{WT}}/\overline{\text{DEC4}}$	Write Clock Input (TBCE, DSC, TBC) Write Timing Input (1H/2H) Decode Pulse Output 4 (D)
16	$\overline{\text{WRES}}$/DS/$\overline{\text{DEC3}}$	Write Reset Input (TBCE, DSC, TBC) Delay Select Input (1H/2H) Decode Pulse Output 3 (D)
17-24	Dout 0 – Dout 7	Data Outputs (All Modes)
25	$\overline{\text{OE}}$	Output Enable Input (All Modes)
26	MODE3/$\overline{\text{RDEC}}/\overline{\text{DEC2}}$	Mode Input 3 (TBCE) Read Decode Pulse Output (TBC) Decode Pulse Output 2 (1H/2H, D)
27	MODE2	Mode Input 2 (All Modes)
28	V_{CC}	Power Supply (+5V) (All Modes)

Mode Table

Mode Signals			Mode	Application Example
MODE1	MODE2	MODE3		
H	H	H	Time base compression/expansion (TBCE)	Picture in Picture
H	H	L	Double speed conversion (DSC)	Non interlace
H	L	– *1	Time base correction (TBC)	Time Base Corrector
L	H	– *1	1H/2H delay (1H/2H)	Vertical filter
L	L	– *1	Delay line (D)	Delay line

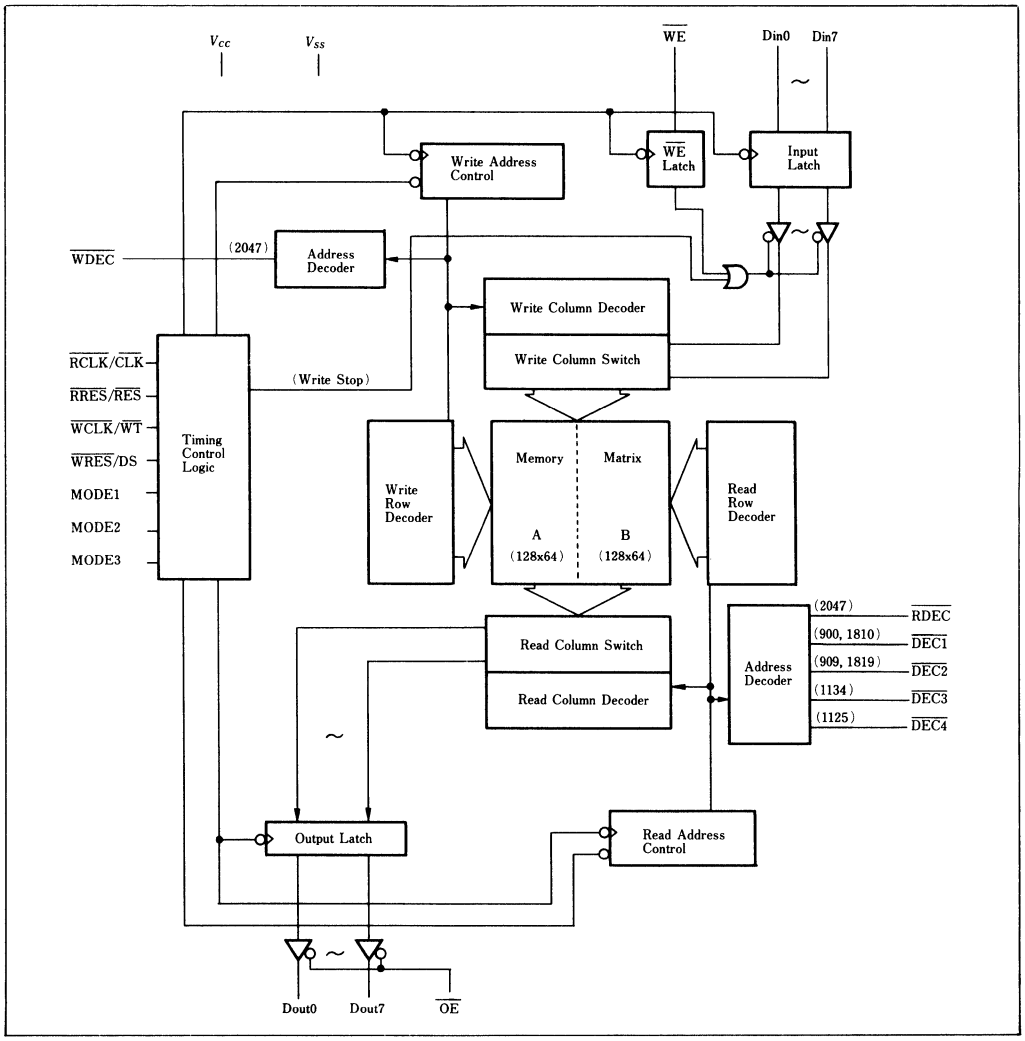
Note) *1. Decoder Output Signal ($\overline{\text{RDEC}}$, $\overline{\text{DEC2}}$)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal Voltage relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C

Note) *1. −3.5V for pulse width $\leqq$ 10 ns

Block Diagram



Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≤ 10 ns

DC and Operating Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	10	μA	$V_{CC} = 5.5$ V $V_{in} = V_{SS}$ to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{OE} = V_{IH}$ $V_{out} = V_{SS}$ to V_{CC}
Operating Power Supply Current	I_{CC}	–	50	90	mA	Min. cycle, Iout = 0 mA
Output Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA, Dout 0 to Dout 7, $\overline{DEC}$ Output pin
	V_{OH}	2.4	–	–	V	I_{OL} = -4 mA, Dout 0 to Dout 7 pin
		2.4	–	–	V	I_{OH} = -1 mA, $\overline{DEC}$ Output pin

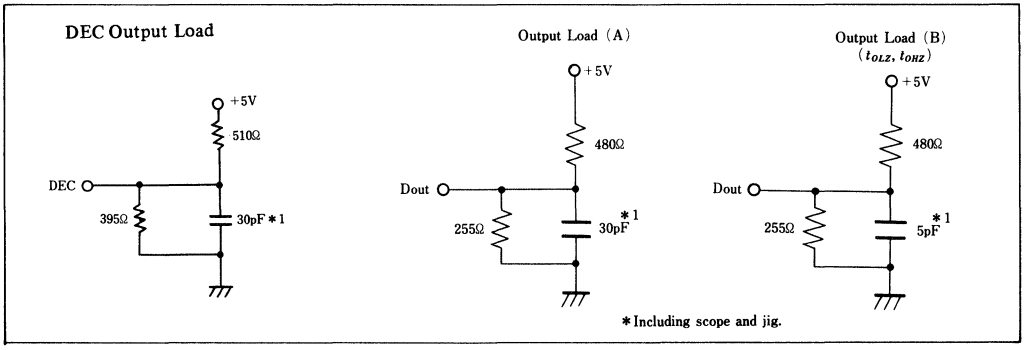
Capacitance ($Ta = 25°C$, $f = 1.0$ MHz)

Parameter	Symbol	min	typ	max	Unit	Conditions
Input Capacitance	Cin	–	–	6	pF	Vin = 0V
Output Capacitance*2	Cout	–	–	9	pF	Vout = 0V

Notes) *1. This parameter is sampled and not 100% tested.
*2. 13, 15 – 24, 26 pin

AC Characteristics ($V_{CC} = 5V \pm 10\%$, $Ta = 0$ to $+70°C$)

- AC Test Conditions
  Input and Output timing reference levels: 1.5V
  Input pulse levels: V_{SS} to 3V
  Input rise and fall times: 5 ns



Read Cycle

Parameter		Symbol	HM63021-28		HM63021-34		Unit
			min	max	min	max	
Read Cycle Time		t_{RC}	28	–	34	–	ns
Read Clock Width		t_{RWL}	10	–	10	–	ns
		t_{RWH}	10	–	10	–	ns
Access Time		t_{AC}	–	20	–	25	ns
Decode Output Access Time	(fall)	t_{DA1}	–	20	–	25	ns
	(rise)	t_{DA2}	–	40	–	50	ns
Output Hold Time		t_{OH}	5	–	5	–	ns
Decode Output Hold Time	(fall)	t_{DOH1}	5	–	5	–	ns
	(rise)	t_{DOH2}	5	–	5	–	ns
Output Enable Access Time		t_{OE}	–	20	–	25	ns
Output Disable to Output in High Z		t_{OHZ}	0	15	0	20	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	ns

Write Cycle

Parameter	Symbol	HM63021-28		HM63021-34		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	28	–	34	–	ns
	t_{WC}(1H/2H Mode)	56	–	68	–	ns
Write Clock Width	t_{WWL}	10	–	10	–	ns
	t_{WWH}	10	–	10	–	ns
Input Data Setup Time	t_{DS}	5	–	5	–	ns
Input Data Hold Time	t_{DH}	5	–	5	–	ns
$\overline{WE}$ Setup Time	t_{WESL}	5	–	5	–	ns
	t_{WESH}	5	–	5	–	ns
$\overline{WE}$ Hold Time	t_{WEHL}	5	–	5	–	ns
	t_{WEHH}	5	–	5	–	ns
$\overline{WT}$ Setup Time	t_{WTSL}	5	–	5	–	ns
	t_{WTSH}	5	–	5	–	ns
$\overline{WT}$ Hold Time	t_{WTHL}	5	–	5	–	ns
	t_{WTHH}	5	–	5	–	ns

Reset Cycle

Parameter	Symbol	HM63021-28		HM63021-34		Unit
		min	max	min	max	
Reset Setup Time	t_{RES}	8	–	9	–	ns
Reset Hold Time	t_{REH}	5	–	5	–	ns
Clock Setup Time Before Reset	t_{REPS}	8	–	9	–	ns
Clock Hold Time Before Reset	t_{REPH}	5	–	5	–	ns

Mode Description

- Time base compression/expansion Mode
  This mode turns HM63021 to 2048-word x 8-bit FIFO memory with input/output asynchronized. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$) each for read and write. The internal address counters increase 1 address by 1 clock and turn to address 0 by reset. Write stop function in HM63021 stops writing automatically after the data is written into all addresses 0 to 2047. Write stop function is released by reset using $\overline{WRES}$ and the HM63021 restarts writing into address 0.
- Double Speed Conversion Mode
  This mode turns HM63021 to 1024-word x 8-bit x 2 memory with input/output asynchronized. It is used for generating non-interlaced TV signals. When the original signal and the interpolation signal (1 field delay) of interlaced signals are put into the HM63021, being multiplexed per dot, it outputs non-interlaced signals per line. 8 fsc should be put into $\overline{RCLK}$ and $\overline{WCLK}$. Standard H synchronizing signal and non-interlace H synchronizing signal are put into $\overline{WRES}$ and $\overline{RRES}$ respectively. Write stop function is provided in this mode. Using write stop function, this mode is also applicable to PAL TV, where extra data (1135-1024 = 111 bits) are neglected.
- TBC Mode
  This mode turns HM63021 to 2048-word x 8-bit FIFO memory with input/output asynchronized. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$) each for read and write. The internal address counters increase 1 address by 1 clock and turn to 0 address by reset. The internal address counters return to 0 address after they reached address 2047. The HM63021 outputs write decode pulse from $\overline{WDEC}$, synchronizing with address 2047 in the write address counter and read decode pulse from $\overline{RDEC}$, synchronizing with address 2047 in the read address counter. Using these pulses, memory area can be extended easily (multi-HM63021s are used with ease).
- 1H/2H Delay Mode
  This mode turns HM63021 to 1024-word x 8-bit x 2 delay line with input/output synchronized. Delay time is defined by reset period of $\overline{RES}$. As the HM63021 outputs 901 decode pulse ($\overline{DEC1}$)

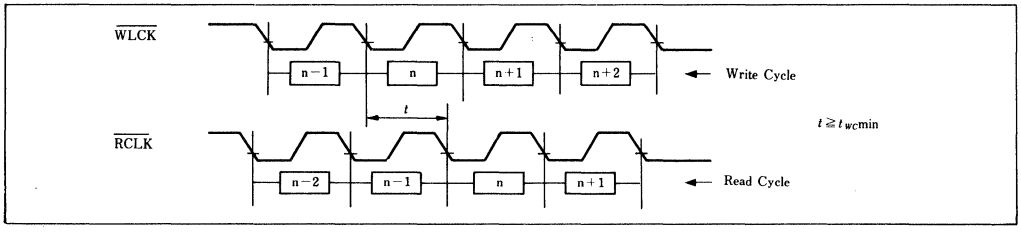
and 910 decode pulse ($\overline{DEC2}$), for example, connecting $\overline{DEC2}$ to $\overline{RES}$ outputs 1H and 2H delayed signal alternately at 8 fsc cycle when original signal is put into at 4 fsc cycle. Write stop function is provided in this mode. Using write stop function, this mode is also applicable to PAL TV, where extra data (1135-1024 = 111 bits) are neglected.

- Delay Line Mode
  This mode turns HM63021 to 2048-word x 8-bit delay line with input/output synchronized. Delay time (3 – 2048-bit) is defined by reset period of $\overline{RES}$. 2048-bit is delayed when $\overline{RES}$ is fixed High. Signals delayed by 910, 1126 or 1135 bits for example, can be easily obtained without external circuits by connecting selected decoded pulses on $\overline{DEC1}$ – $\overline{DEC4}$ to $\overline{RES}$.

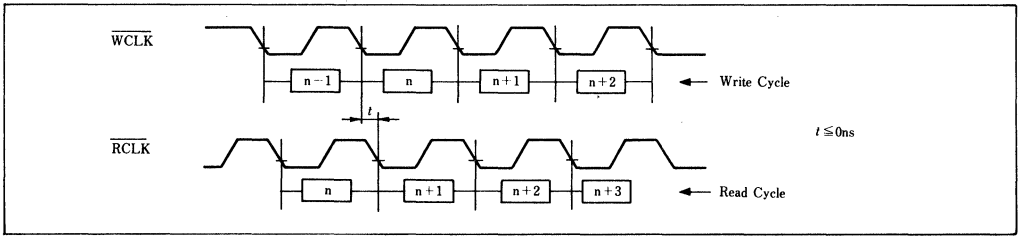
Considerations on Using HM63021

- It is recommended that pin. No. 13 (High Impedance) is pulled up or pulled down with the resistor (several kΩ) in TBC or DSC mode.
- It is recommended that mode signal input pins are pulled up or pulled down with the resistor (several kΩ).
- Data integrity is not guaranteed when mode is changed in the operation.
- When read address coincides with write address in TBCE, TBC and DSC modes, the data is written correctly but is not always assured to be read correctly.

(1) Read after Write (3 bits delay)



(2) Write after Read (2048 bits delay)



Decode Signal

When internal address counter reaches the specified address as shown below, Decode outputs become low.

Mode	Pin No.	Pin Name	Internal Address counter	Timing of the Output Signal	Operation
TBC	13	$\overline{\text{WDEC}}$	Write 2047	After Write 2047	Completion of Writing on all bits is detected.
	26	$\overline{\text{RDEC}}$	Read 2047	Output of 2046	Completion of Reading from all bits is detected.
1H/2H	13	$\overline{\text{DEC1}}$	Read 900 (2H)	Output of 900 (1H)	By inputting this signal to pin #3, 901/1802 bits delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909 (2H)	Output of 909 (1H)	By inputting this signal to pin #3, 910/1820 bits delay output is obtained.
Delay line	13	$\overline{\text{DEC1}}$	Read 900	Output of 899	By inputting this signal to pin #3, 901 bits delay output is obtained.
			Read 1810	Output of 1809	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC1}}$ is devided into two, 1811 bits delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909	Output of 908	By inputting this signal to pin #3, 910 bits delay output is obtained.
			Read 1819	Output of 1818	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC2}}$ is devided into two, 1820 bits delay output is obtained.
	16	$\overline{\text{DEC3}}$	Read 1134	Output of 1133	By inputting this signal to pin #3, 1135 bits delay output is obtained.
	15	$\overline{\text{DEC4}}$	Read 1125	Output of 1124	By inputting this signal to pin #3, 1126 bits delay output is obtained.

Note) When counter is reset by Reset Signal ($\overline{\text{RRES}}$, $\overline{\text{RES}}$, $\overline{\text{WRES}}$), address becomes 0.

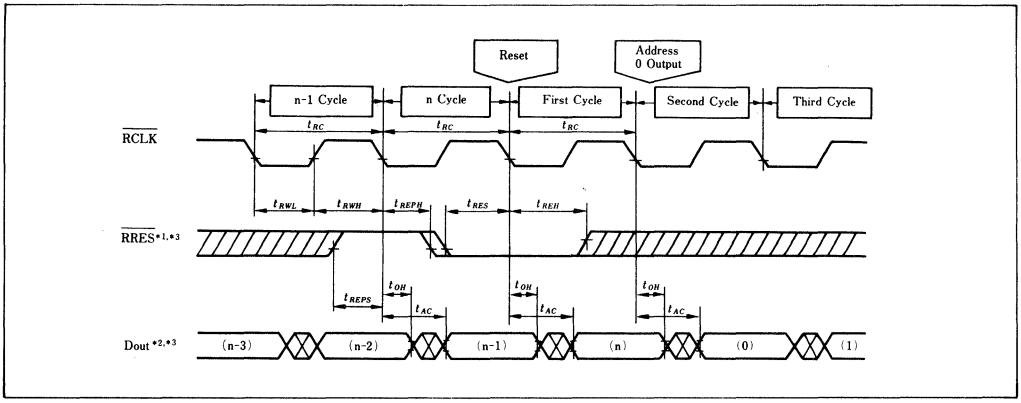
Write Stop Function

When internal counter address is as follows, writing is stopped automatically for the next cycle. The write stop is cancelled by reset through $\overline{\text{WRES}}$ or $\overline{\text{RES}}$.

Mode	Write Stop Function (internal counter address)
TBCE	Write stop after address 2047
DSC	Write stop after address 1023 x 2
TBC	No function
1H/2H	Write stop after address 1023
D	No function

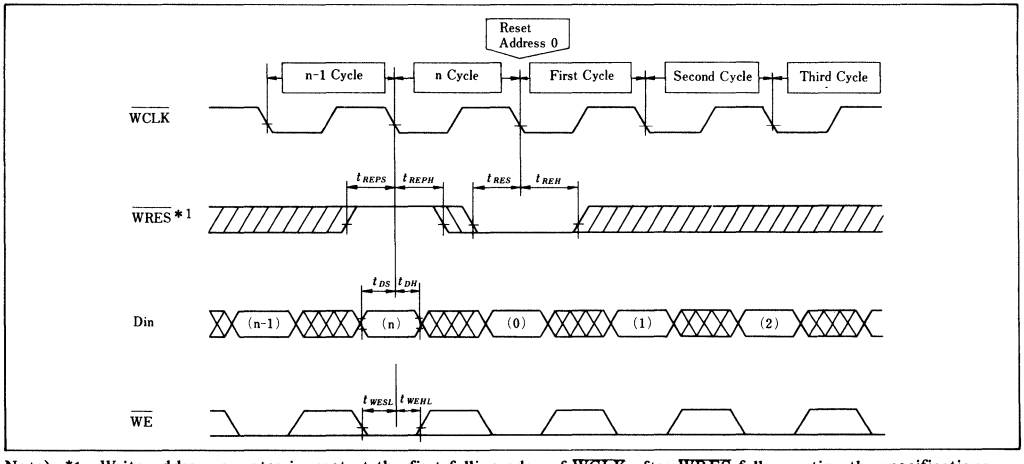
Note) When address counter is reset by $\overline{\text{WRES}}$ or $\overline{\text{RES}}$, address becomes 0.

Read Reset Cycle (TBCE, TBC Modes)



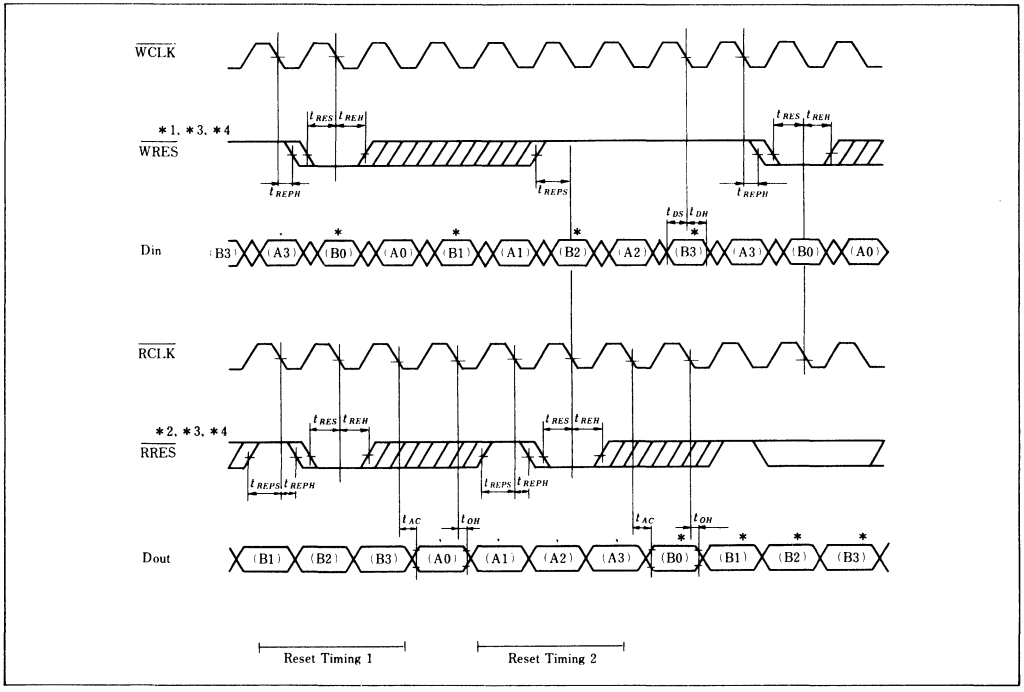
Notes) *1. Read address counter is reset at the first falling edge of RCLK after RRES falls meeting the specifications t_{REPS} and t_{REPH}, and is not reset at the next falling edge of RCLK even if RRES keeps low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, reset operation is not guaranteed.
*2. Output is read address of previous cycle.
*3. When RRES is fixed high, the data at the read address counter is reset after the data of address 2047 outputs, and then circulates.

Write Reset Cycle (TBCE, TBC Modes)



Note) *1. Write address counter is reset at the first falling edge of WCLK after WRES falls meeting the specifications t_{REPS} and t_{REPH}, and is not reset at the next falling edge of WCLK even if WRES keeps low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, reset operation is not guaranteed.

Reset Cycle (DSC Mode)



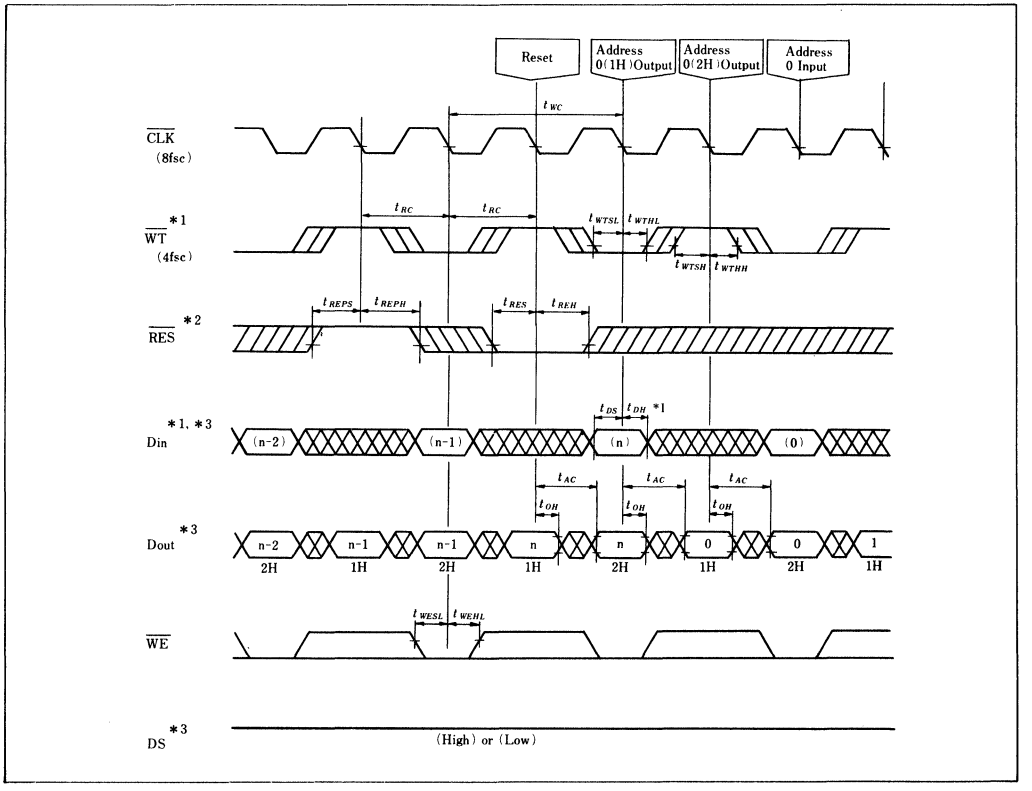
Notes) *1. Write address counter is reset at the first falling edge of WCLK after WRES falls meeting specifications t_{REPS} and t_{REPH}, and is not reset at the next falling edge of WCLK even if WRES keeps low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, reset operation is not guaranteed.

*2. Read address counter is reset at the first falling edge of RCLK after RRES falls meeting specifications t_{REPS} and t_{REPH}, and is not reset at the next falling edge of RCLK even if RRES keeps low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, reset operation is not guaranteed.

*3. When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, output of video signal A is not guaranteed. (Reset Timing I).

*4. When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, interpolation signal B is not guaranteed. (Reset Timing II)

Reset Cycle (1H/2H Mode)

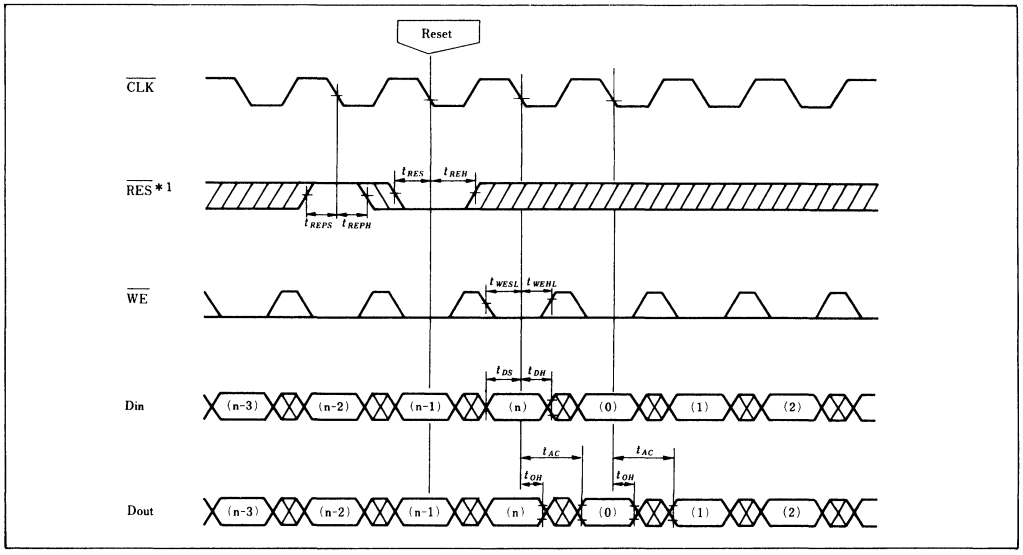


Notes) *1. WT is input in a half cycle of $\overline{CLK}$ meeting specification t_{WTSL}, t_{WTHL}, t_{WTSH} and t_{WTHH}. Data is written when $\overline{WT}$ is Low. Reset is possible when $\overline{WT}$ is High.

*2. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls meeting specifications t_{REPS} and t_{REPH}, and is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ keeps low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, reset operation is not guaranteed.

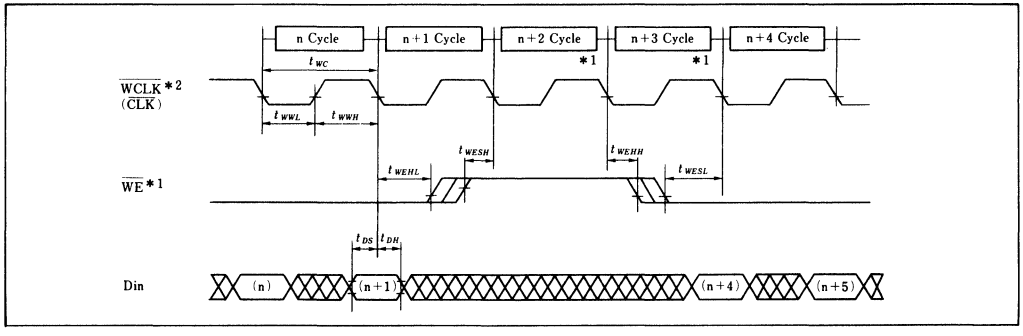
*3. When DS is fixed high, 1H output data is delayed by n bits and 2H output data is delayed by 2n bits where 2n is the reset cycle of $\overline{RES}$.
When DS is fixed low, 1H output data is delayed by n-5 bits and 2H output data is delayed by 2n-5 bits.

Reset Cycle (D Mode)



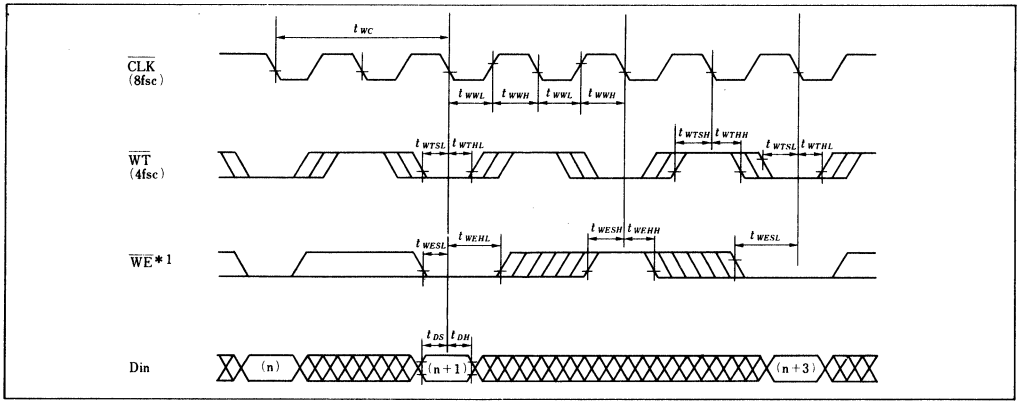
Note) *1. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls meeting specifications t_{REPS} and t_{REPH}, and is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ keeps low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} can not meet the specifications, reset operation is not guaranteed.

Write Enable (TBCE, DSC, TBC, D Modes)



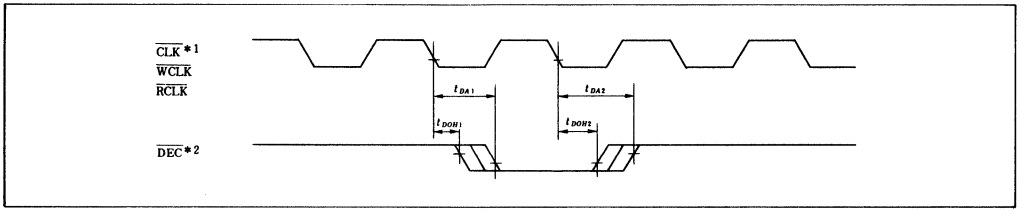
Notes) *1. When t_{WEHL}, t_{WESH}, t_{WEHH} and t_{WESL} can not meet this specifications, Write Enable operation is not guaranteed.
*2. In delay line mode, $\overline{CLK}$ takes the place of $\overline{WCLK}$.

Write Enable (1H/2H Mode)



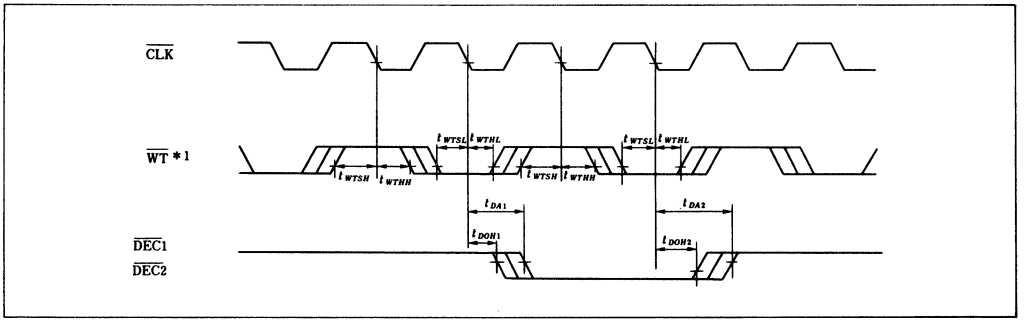
Note) *1. When t_{WTSL}, t_{WTHL}, t_{WEHL} and t_{WEHH} can not meet the specifications, Write Enable operation is not guaranteed.

Decode Output (TBC, D Modes)



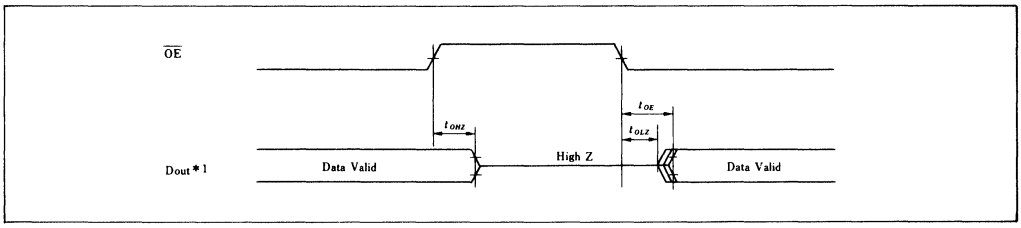
Notes) *1. In TBC mode, WCLK or RCLK takes the place of CLK.
*2. DEC is WDEC or RDEC in TBC, DEC1, DEC2, DEC3 or DEC4 in D.

Decode Output (1H/2H Modes)



Note) *1. When t_{WTSL}, t_{WTHL}, t_{WTSH}, t_{WTHH} can not meet the specifications, decode output operation is not guaranteed.

Output Enable (All Modes)



Note) *1. Transition of t_{OHZ} and t_{WLZ} is measured ±200 mV from steady state voltage with Output Load B. This parameter is sampled and not 100% tested.

MOS DYNAMIC RAM

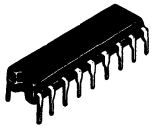
HM50464 Series

65536-word x 4-bit Dynamic Random Access Memory

■ FEATURES

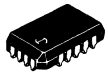
- Page mode capability
- Single 5V (±10%)
- On chip substrate bias generator
- Low power: 350 mW active, 20 mW standby
- High speed: Access Time 120ns/150ns/200ns
- Output data controlled by $\overline{CAS}$ or $\overline{OE}$
- TTL compatible
- 256 refresh cycles . . . . . 4 ms
- 3 variations of refresh . . . . . $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

HM50464P Series



(DP-18B)

HM50464CP Series

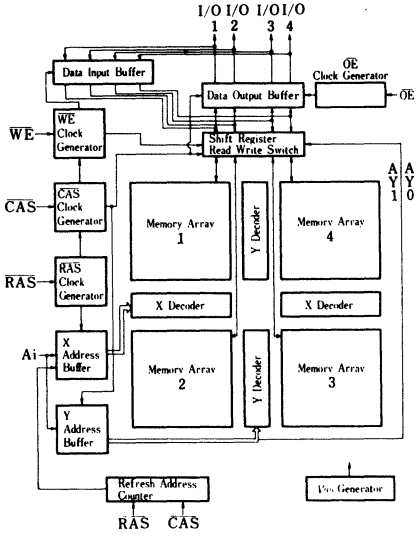


(CP-18)

■ ORDERING INFORMATION

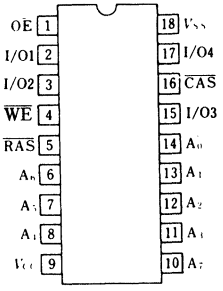
Type No.	Access Time	Package
HM50464P-12	120ns	300 mil 18 pin Plastic DIP
HM50464P-15	150ns	
HM50464P-20	200ns	
HM50464CP-12	120ns	18 pin PLCC
HM50464CP-15	150ns	
HM50464CP-20	200ns	

■ BLOCK DIAGRAM



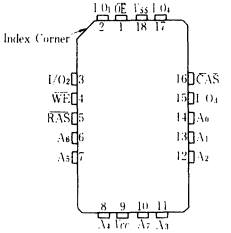
■ PIN ARRANGEMENT

● HM50464P Series



(Top View)

● HM50464CP Series



(Top View)

$A_0 - A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O1 – I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_7$ (Row)	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1 to +7	V
Supply Voltage relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature (Ambient)	*Topr*	0 to +70	°C
Storage Temperature (Ambient)	*Tstg*	−55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	*Iout*	50	mA

■ RECOMMENDED DC OPERATING CONDITION (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	–	6.5	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (Vcc = 5V ±10%, Vss = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Operating Current (t_{RC} = min.)	I_{CC1}	–	83	–	70	–	55	mA	1
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Disable)	I_{CC2}	–	4.5	–	4.5	–	4.5	mA	
Refresh Current ($\overline{RAS}$ only refresh, t_{RC} = min.)	I_{CC3}	–	62	–	53	–	42	mA	
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Enable)	I_{CC5}	–	10	–	10	–	10	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = min.)	I_{CC6}	–	69	–	58	–	45	mA	1
Operating Current (Page mode, t_{PC} = min.)	I_{CC7}	–	57	–	48	–	37	mA	1
Input Leakage Current (0 < *Vin* < 7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage Current (0 < *Vout* < 7V, Dout = Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output High Voltage (*Iout* = −5 mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage (*Iout* = 4.2 mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (V_{CC} = 5V ±10%, Ta = 25°C)

Parameter		Symbol	typ.	max.	Unit	Note
Input Capacitance	Address	$CI1$	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	$CI2$	–	10	pF	1
Output Capacitance	Data In/Data Out	CI/O	–	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Vcc = 5V ±10%, Vss = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	60	–	75	–	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	30	–	40	–	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	–	260	–	330	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	

(to be continued)

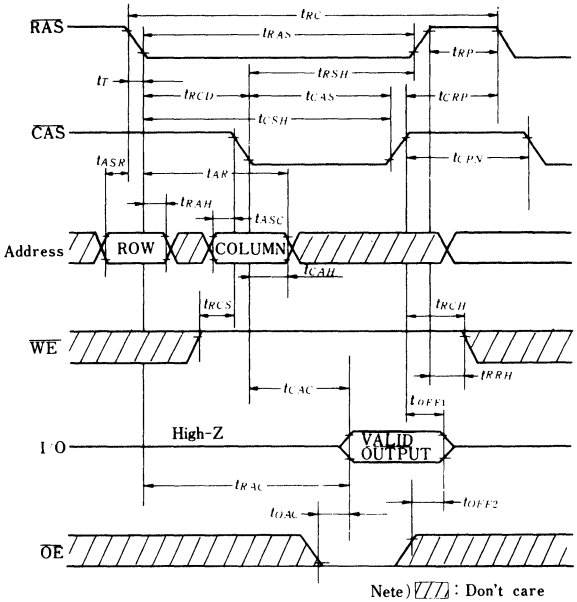
Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	25	–	30	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	–	100	–	130	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	40	–	45	–	55	–	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	–	120	–	155	–	ns	
Write Command Pulse Width	t_{WP}	40	–	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	–	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	–	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	40	–	45	–	55	–	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
Read-Write Cycle Time	t_{RWC}	305	–	360	–	450	–	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	100	–	125	–	160	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	160	–	200	–	260	–	ns	8
$\overline{CAS}$ Precharge Time	t_{CPN}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	120	–	150	–	200	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	45	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	30	–	40	–	50	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	30	–	40	–	50	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	25	–	30	–	40	–	ns	
Page Mode Cycle Time	t_{PC}	120	–	145	–	190	–	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Read-modify-write Cycle Time (Page-mode)	t_{PCM}	205	–	245	–	310	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assume that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization of cycles.
11. Minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh is required before using internal refresh counter.
12. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

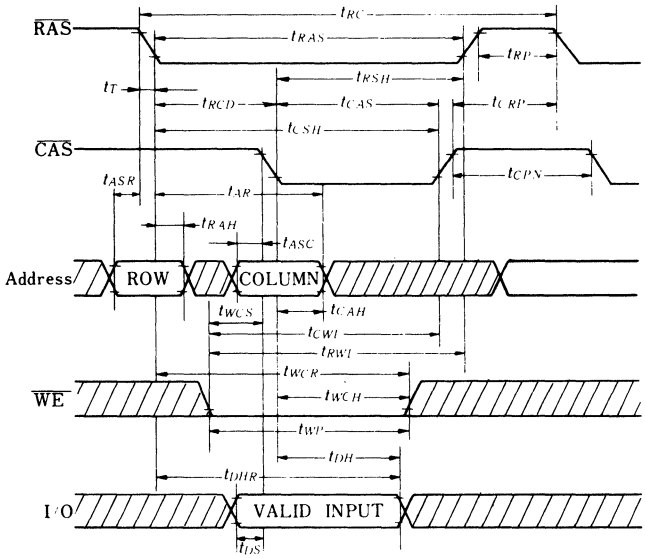
■ TIMING WAVEFORMS

• READ CYCLE

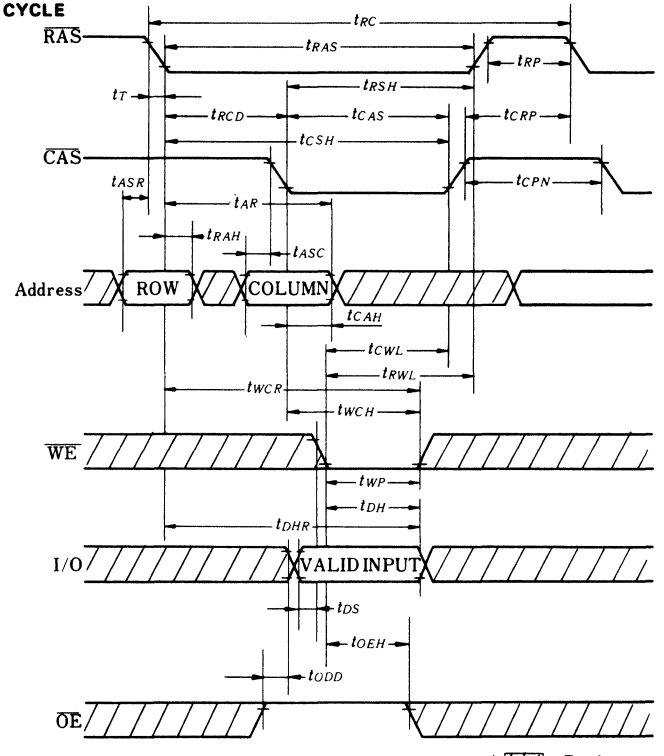


Nete) ▨ : Don't care

• EARLY WRITE CYCLE

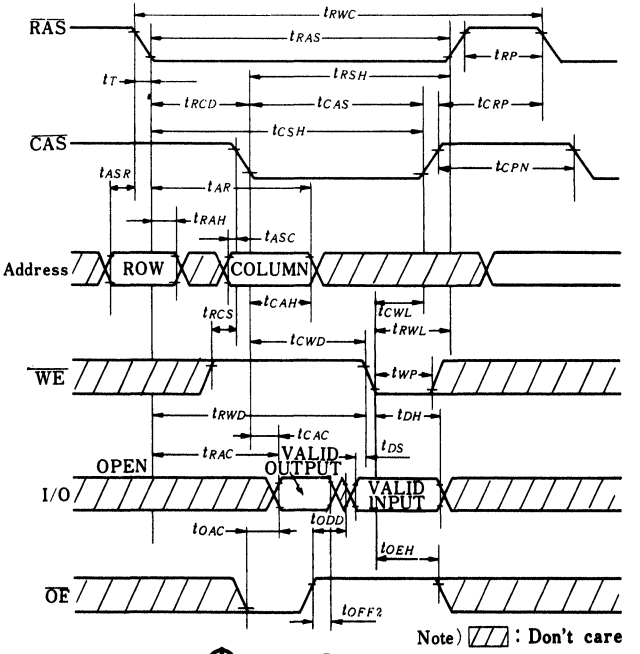


- **DELAYED WRITE CYCLE**



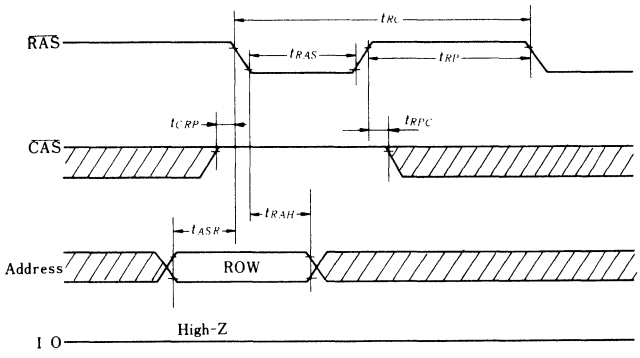
Note) ▨ : Don't care

- **READ MODIFY WRITE CYCLE**



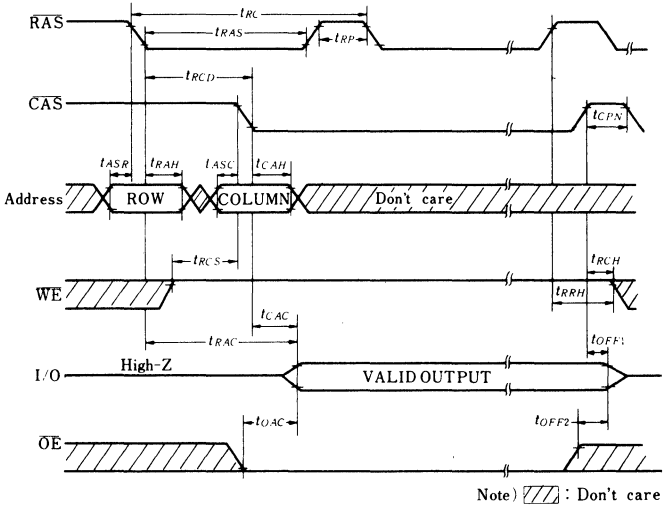
Note) ▨ : Don't care

- **$\overline{RAS}$ ONLY REFRESH CYCLE**



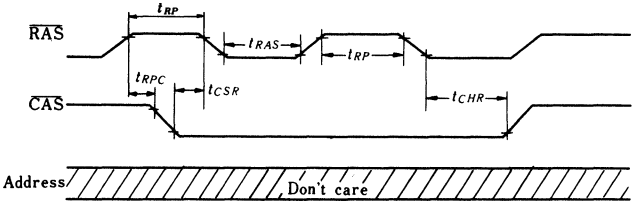
Notes) 1. $\overline{OE}$, $\overline{WE}$: Don't care
2. ▨ : Don't care

- **HIDDEN REFRESH CYCLE**

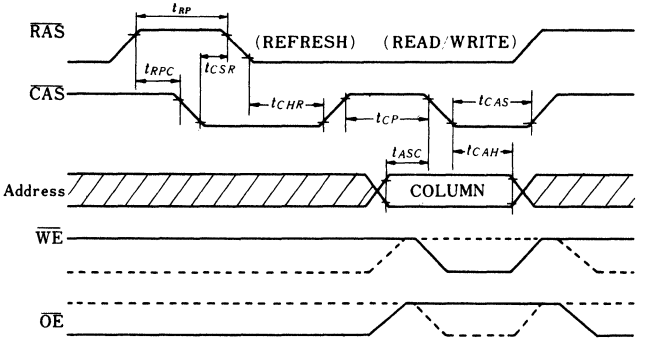


Note) ▨ : Don't care

- **$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE**

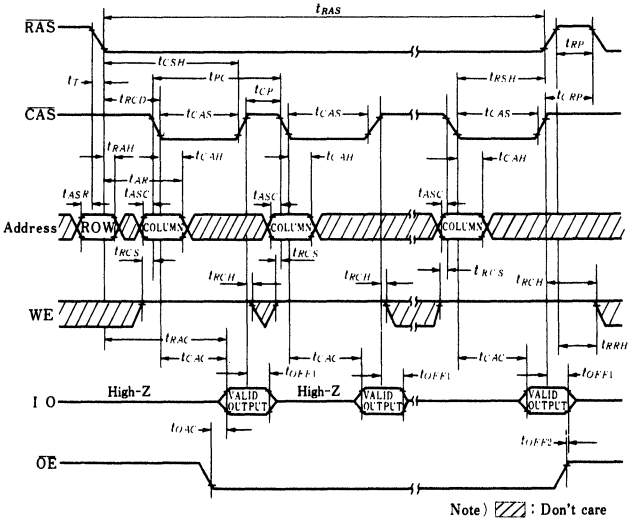


- **COUNTER TEST**



Notes) 1. Dotted-line Means Read Cycle. 2. ▨ : Don't care

- **PAGE MODE READ CYCLE**



Note) ▨ : Don't care

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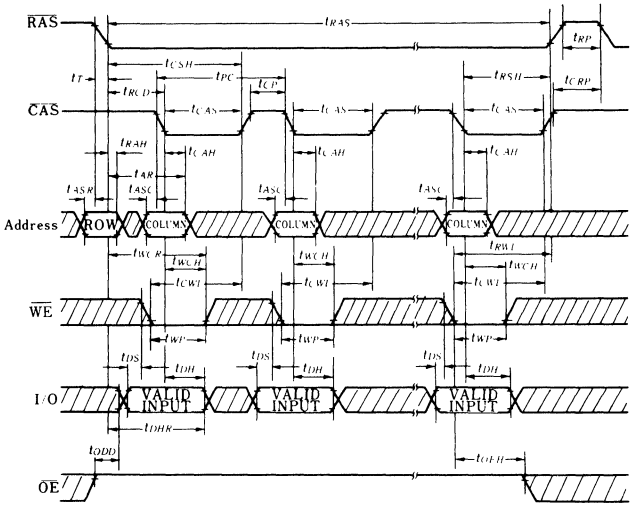
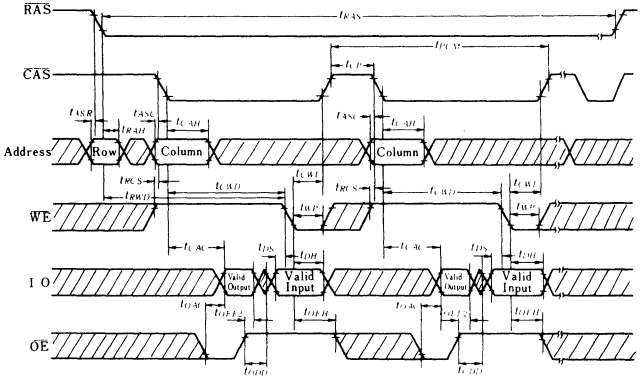
- **PAGE MODE WRITE CYCLE**



Note) ▨ : Don't care

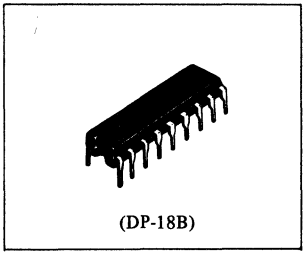
- **PAGE MODE READ MODIFY WRITE CYCLE**



Note) ▨ : Don't care

HM50465 Series

65536-word x 4-bit Dynamic Random Access Memory


(DP-18B)

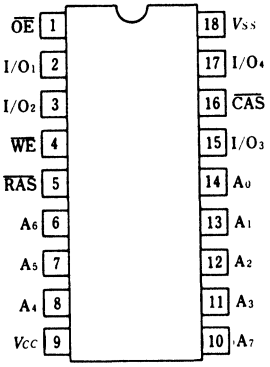
■ FEATURES

- Nibble mode capability
- Single 5V (±10%)
- On chip substrate bias generator
- Low power; 350 mW active, 20 mW standby
- High Speed: Access time 120 ns/150 ns/200 ns (max.)
- Output data controlled by $\overline{CAS}$ or $\overline{OE}$
- TTL compatible
- 256 refresh cycles . . . . . 4 ms
- 3 variations of refresh . . . . $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

■ ORDERING INFORMATION

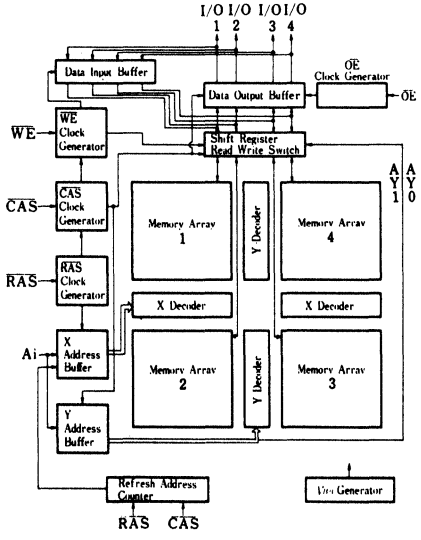
Type No.	Access Time	Package
HM50465P-12	120ns	300 mil 18 pin Plastic DIP
HM50465P-15	150ns	
HM50465P-20	200ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



$A_0 - A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O1 – I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_7$ (Row)	Refresh Address Inputs
A_0, A_1 (Column)	Nibble Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1 to +7	V
Supply Voltage relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature (Ambient)	*Topr*	0 to +70	°C
Storage Temperature (Ambient)	*Tstg*	−55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	*Iout*	50	mA

■ RECOMMENDED DC OPERATING CONDITION (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	–	6.5	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50465-12		HM50465-15		HM50465-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Operating Current (t_{RC} = min.)	I_{CC1}	–	83	–	70	–	55	mA	1
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Disable)	I_{CC2}	–	4.5	–	4.5	–	4.5	mA	
Refresh Current ($\overline{RAS}$ only refresh, t_{RC} = min.)	I_{CC3}	–	62	–	53	–	42	mA	
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Enable)	I_{CC5}	–	10	–	10	–	10	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh, tRC = min.)	I_{CC6}	–	69	–	58	–	45	mA	1
Operating Current (Nibble mode, t_{NC} = min.)	I_{CC8}	–	57	–	48	–	37	mA	1
Input Leakage Current (0 < *Vin* < 7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage Current (0 < *Vout* < 7V, Dout = Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output High Voltage (*Iout* = −5 mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage (*Iout* = 4.2 mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	typ.	max.	Unit	Note
Input Capacitance	Address	*CI1*	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	*CI2*	–	10	pF	1
Output Capacitance	Data In/Data Out	*CI/O*	–	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50465-12		HM50465-15		HM50465-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	60	–	75	–	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	30	–	40	–	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	–	260	–	330	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	

(to be continued)

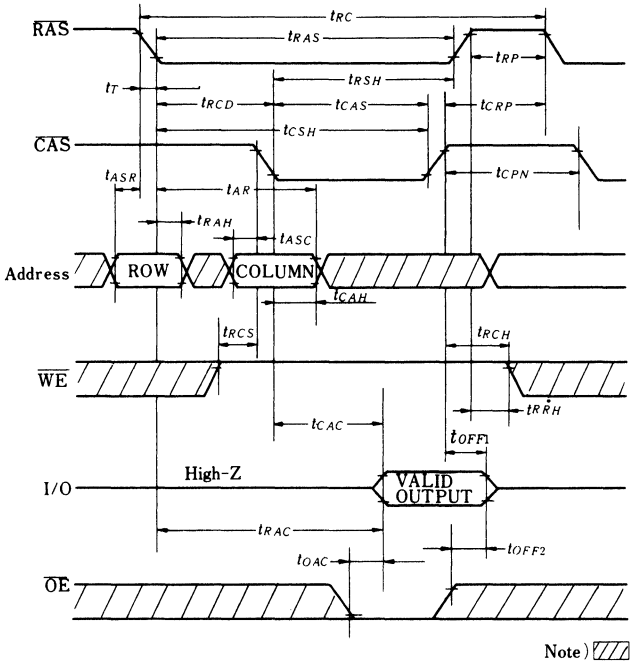
Parameter	Symbol	HM50465-12		HM50465-15		HM50465-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	25	–	30	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	–	100	–	130	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	40	–	45	–	55	–	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	–	120	–	155	–	ns	
Write Command Pulse Width	t_{WP}	40	–	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	–	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	–	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	40	–	45	–	55	–	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
Read-Write Cycle Time	t_{RWC}	305	–	360	–	450	–	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	100	–	125	–	160	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	160	–	200	–	260	–	ns	8
$\overline{CAS}$ Precharge Time	t_{CPN}	50	–	60	–	80	–	ns	
$\overline{CAS}$ set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	120	–	150	–	200	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	45	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	30	–	40	–	50	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	30	–	40	–	50	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WRITE}$	t_{OEH}	25	–	30	–	40	–	ns	
Nibble Mode Access Time	t_{NAC}	–	30	–	35	–	45	ns	
Nibble Mode $\overline{RAS}$ Cycle Time	t_{NRC}	410	–	480	–	610	–	ns	
Nibble Mode $\overline{RAS}$ Pulse Width	t_{NRA}	310	–	370	–	480	–	ns	
Nibble Mode Cycle Time	t_{NC}	60	–	70	–	90	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	20	–	25	–	35	–	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	30	–	35	–	45	–	ns	
Nibble Mode Write Command Hold Time	t_{NWCH}	30	–	35	–	45	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	40	–	45	–	55	–	ns	
Nibble Mode Read-Write Cycle Time	t_{NRWC}	135	–	160	–	200	–	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay	t_{NCWD}	70	–	85	–	105	–	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	30	–	35	–	45	–	ns	
Nibble Mode Write Command Pulse Width	t_{NWP}	30	–	35	–	45	–	ns	

Notes)

1. AC measurements assume $tT = 5$ ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference level for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write on read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization of cycles.
11. Minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh is required before using internal refresh counter.
12. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

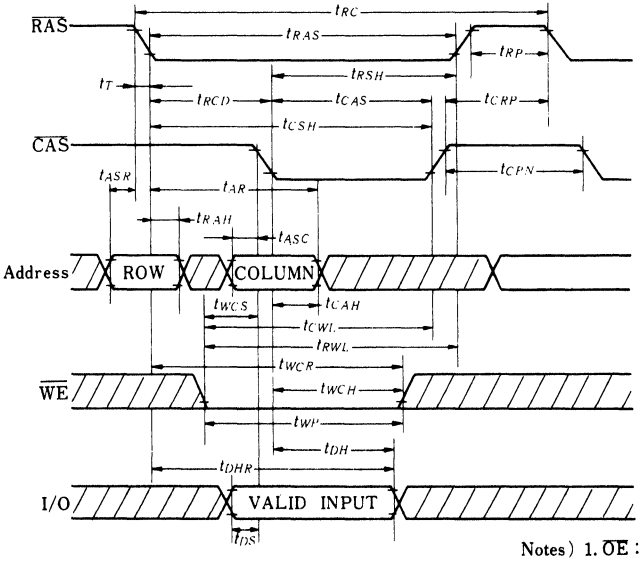
■ TIMING WAVEFORMS

• Read Cycle



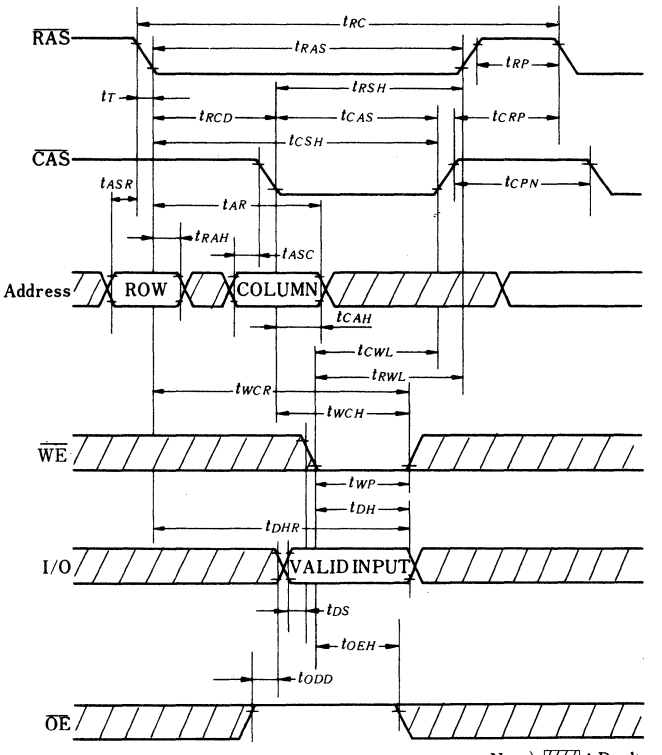
Note) ▨ : Don't care

• Early Write Cycle



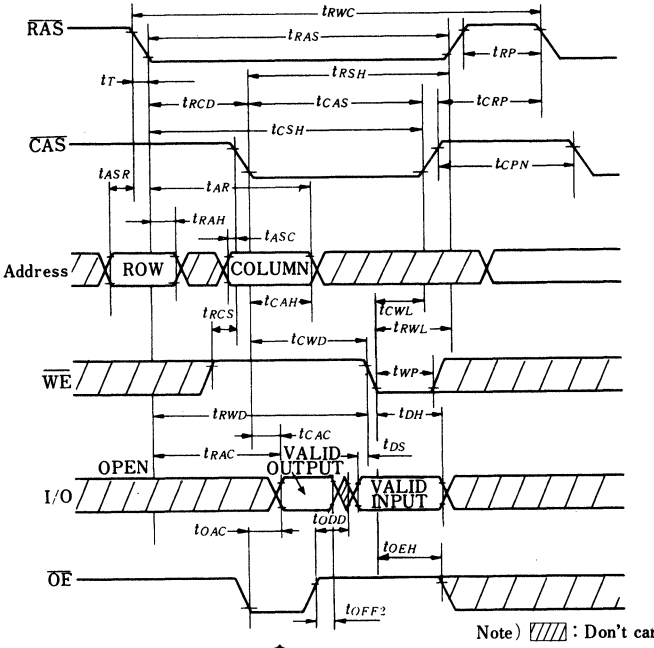
Notes) 1. $\overline{OE}$: Don't care
2. ▨ : Don't care

- **Delayed Write Cycle**



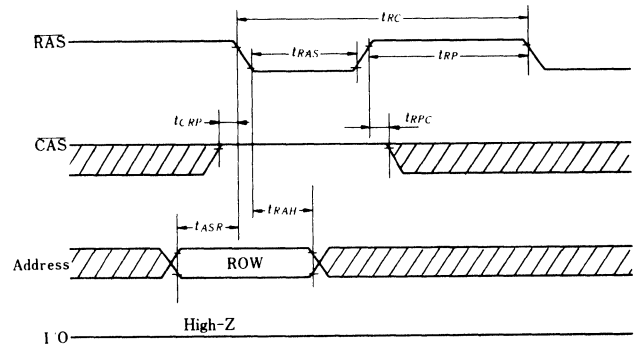
Note) ▨ : Don't care

- **Read Modify Write Cycle**



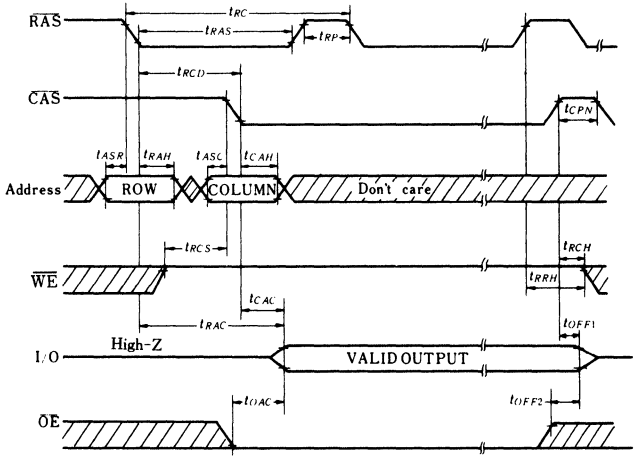
Note) ▨ : Don't care

- **$\overline{RAS}$ Only Refresh Cycle**



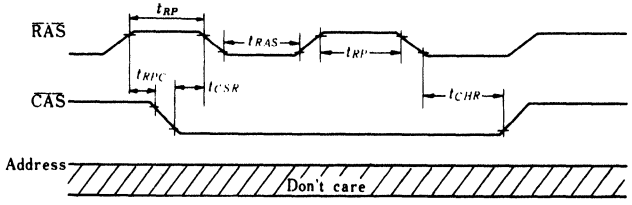
Notes) 1. $\overline{OE}$, $\overline{WE}$: Don't care
2. ▨: Don't care

- **Hidden Refresh Cycle**

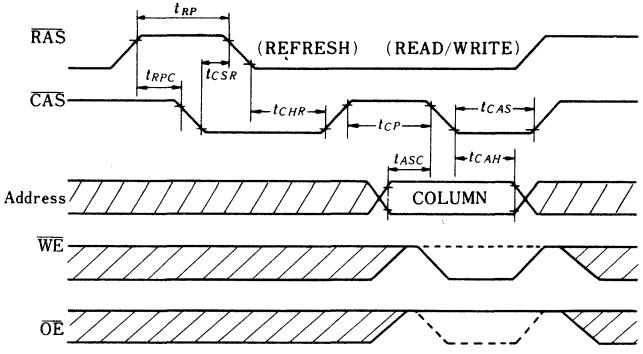


Note) ▨: Don't care

- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**

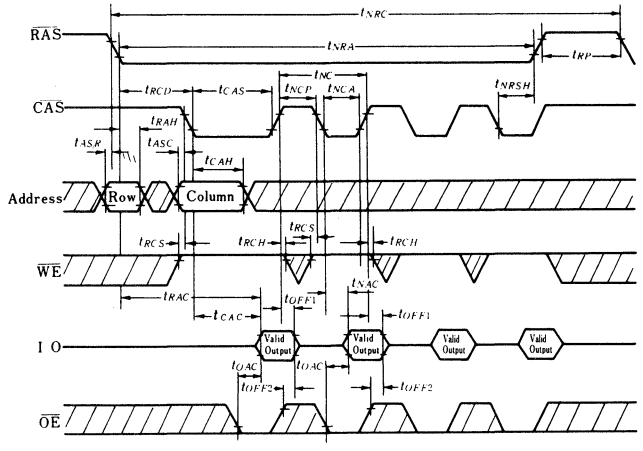


- **Counter Test**



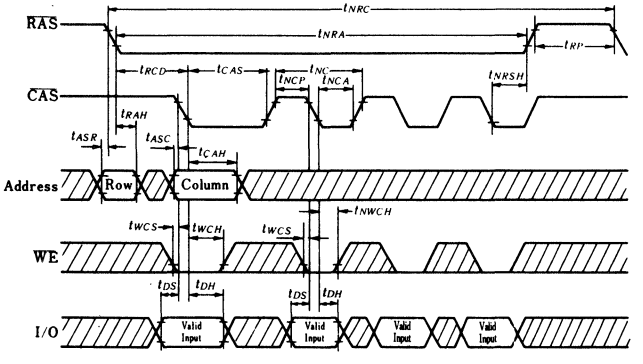
Notes) 1. Dotted Line Means Read Cycle.
2. ▨ : Don't care

- **Nibble Mode Read Cycle**



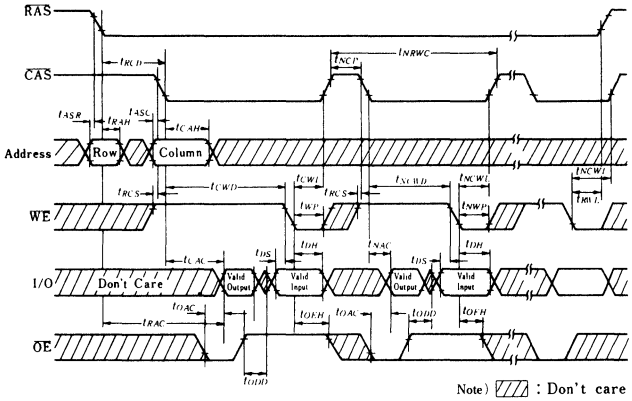
Note) ▨ : Don't care

- **Nibble Mode Write Cycle**



Notes) 1. OE : Don't care
2. ▨ : Don't care

- **Nibble Mode Read Modify Write Cycle**



Note) ▨ : Don't care

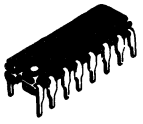
HM50256 Series

262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

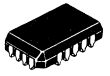
- Industry Standard 16-Pin DIP, 18-Pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles · · · (4ms)
- 3 variations of refresh · · · $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

HM50256P Series



(DP-16B)

HM50256CP Series



(CP-18)

HM50256ZP Series

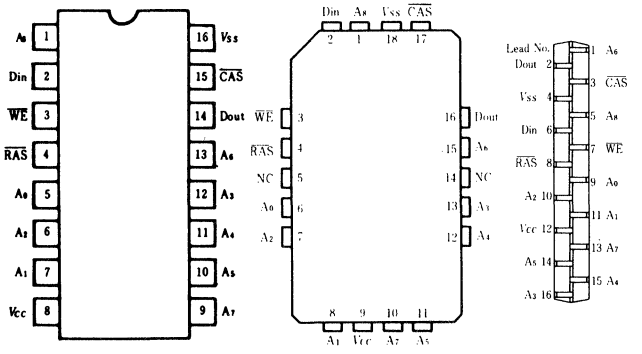
(ZP-16)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM50256P-12 HM50256P-15 HM50256P-20	120ns 150ns 200ns	300 mil 16 pin Plastic DIP
HM50256ZP-12 HM50256ZP-15 HM50256ZP-20	120ns 150ns 200ns	16 pin Plastic ZIP
HM50256CP-12 HM50256CP-15 HM50256CP-20	120ns 150ns 200ns	18 pin PLCC

■ PIN ARRANGEMENT

● HM50256P Series ● HM50256CP Series ● HM50256ZP Series

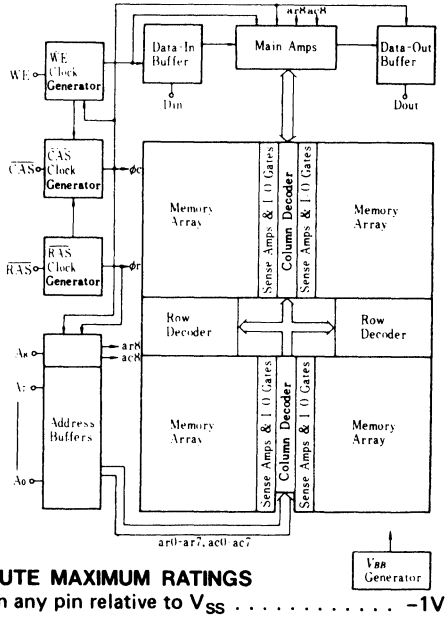


(Top View) (Top View) (Bottom View)

■ PIN DESCRIPTION

$A_0 \sim A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$	Refresh Address Inputs

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . −55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$, $\overline{CAS}$ =Cycling ; t_{RC}=min)	I_{CC1}	—	83	—	70	—	55	mA	1
Standby Current($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current($\overline{RAS}$=V_{IH}, Dout =Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Page Mode Supply Current($\overline{RAS}$=V_{IL}, $\overline{CAS}$ =Cycling, t_{PC}=min)	I_{CC7}	—	57	—	48	—	37	mA	
Input leakage(0<V_{in}<7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage(0<V_{out}<7V, Dout=Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7		1, 2
Output Capacitance	Data-out	C_O	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1), 10), 11)]

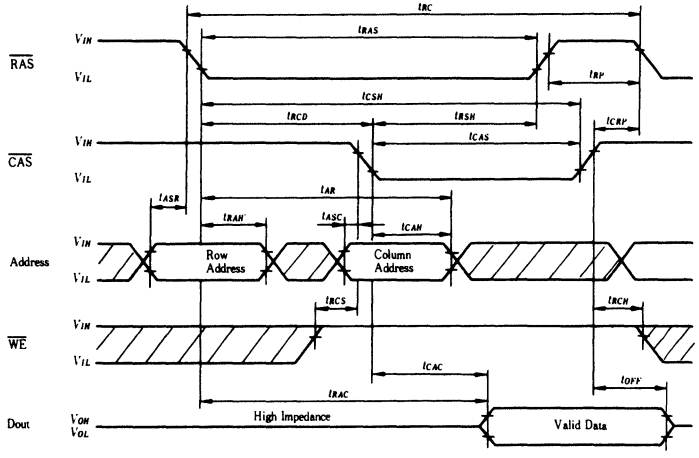
Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
Access Time from $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0		0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15		15		20	—	ns	
Column Address Set-up Time	t_{ASC}	0		0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20		25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read Command Set-up Time	t_{RCS}	0		0		0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0		0	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0		0		ns	8
Write Command Hold Time	t_{WCH}	40		45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45		55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60		75	—	100	—	ns	8
Page Mode Read or Write Cycle	t_{PC}	120		145	—	190		ns	
Page Mode Read Modify Write Cycle	t_{PCM}	165	—	195	—	250	—	ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4		4	—	4	ms	
$\overline{CAS}$ Set-up Time	t_{CSR}	10		10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

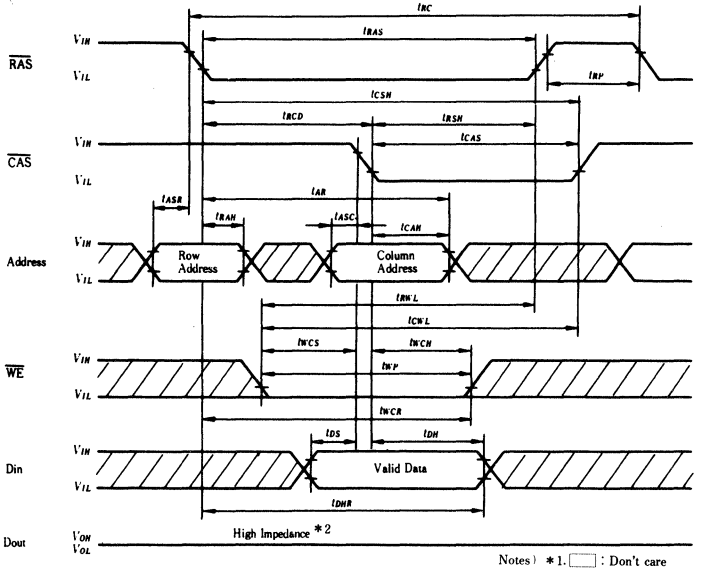
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refesh cycles are required before using internal refresh counter.

■ TIMING WAVEFORMS

● READ CYCLE

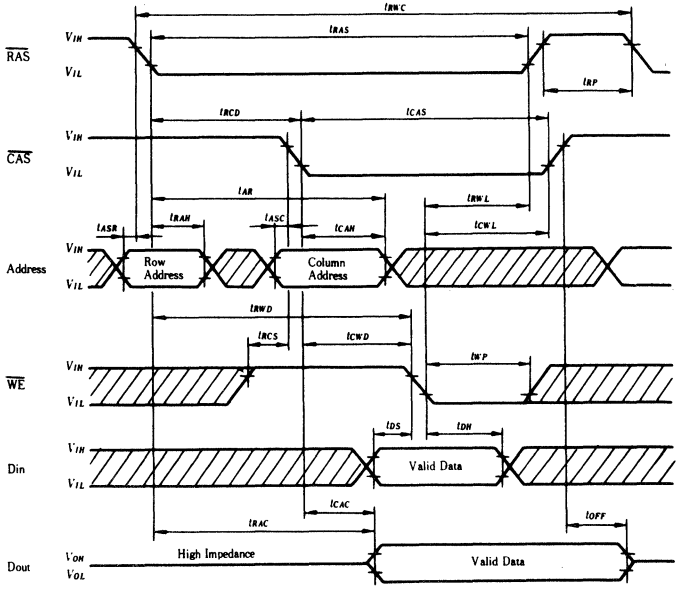


● WRITE CYCLE



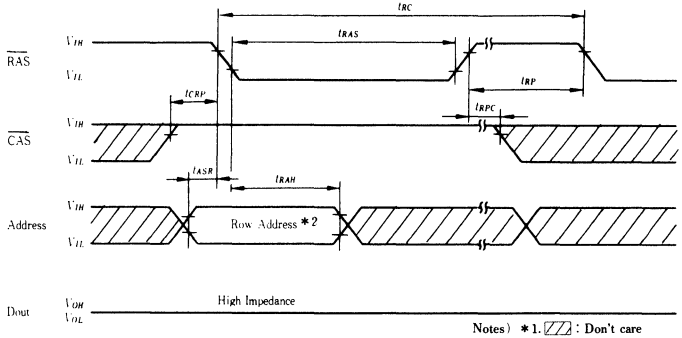
Notes) *1. ▭ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$ (min)

● READ MODIFY WRITE CYCLE



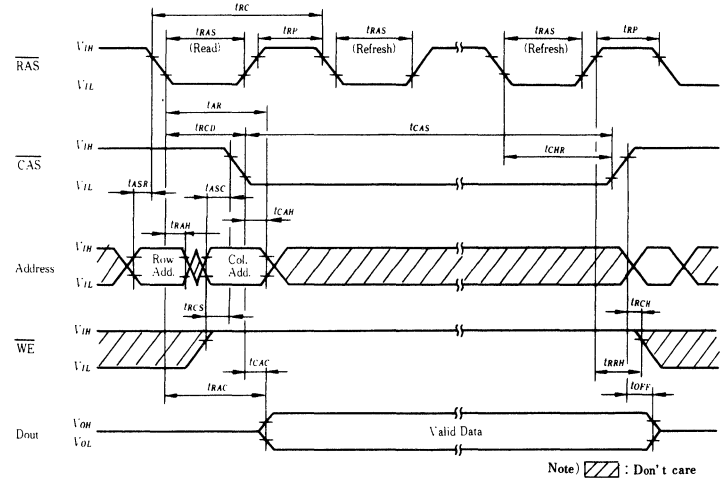
Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$ (min)
$t_{CWD} \geqq t_{CWD}$ (min)

● $\overline{RAS}$ ONLY REFRESH CYCLE



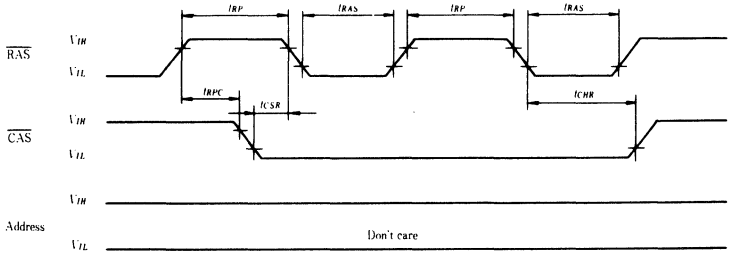
Notes) *1. ▨ : Don't care
*2. Refresh Address A0-A7(AX0-AX7)

● HIDDEN REFRESH CYCLE

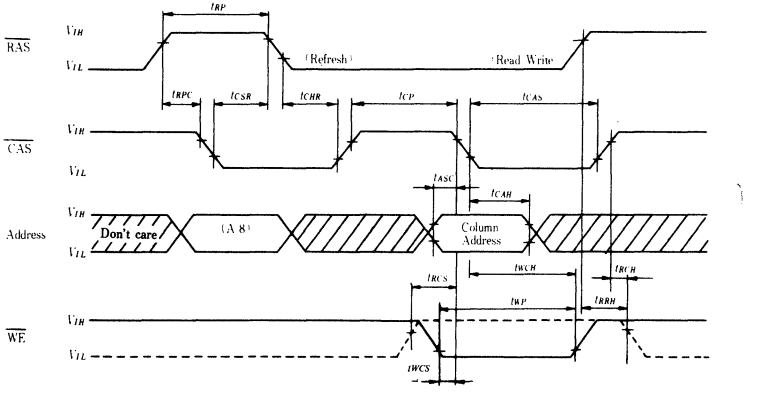


Note) ▨ : Don't care

● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

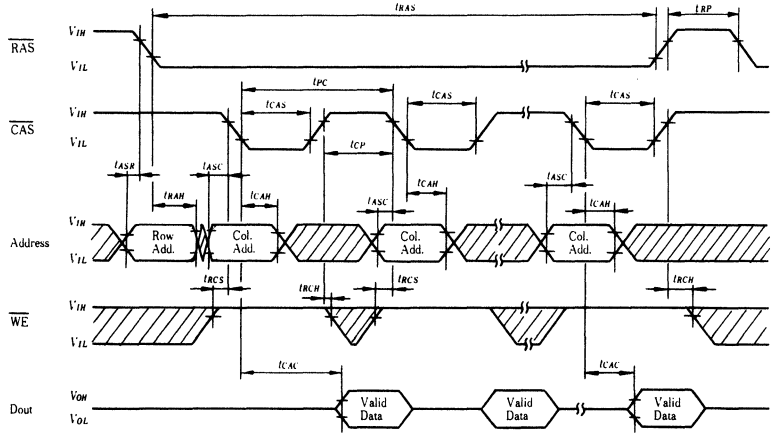


● COUNTER TEST



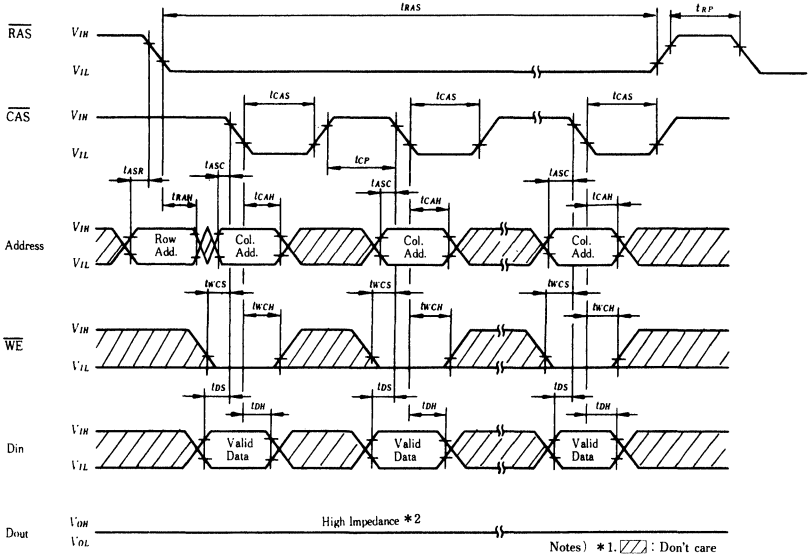
Notes) *1. ▨ : Don't care
*2. Dotted Line Means Read Cycle.

● PAGE MODE READ CYCLE



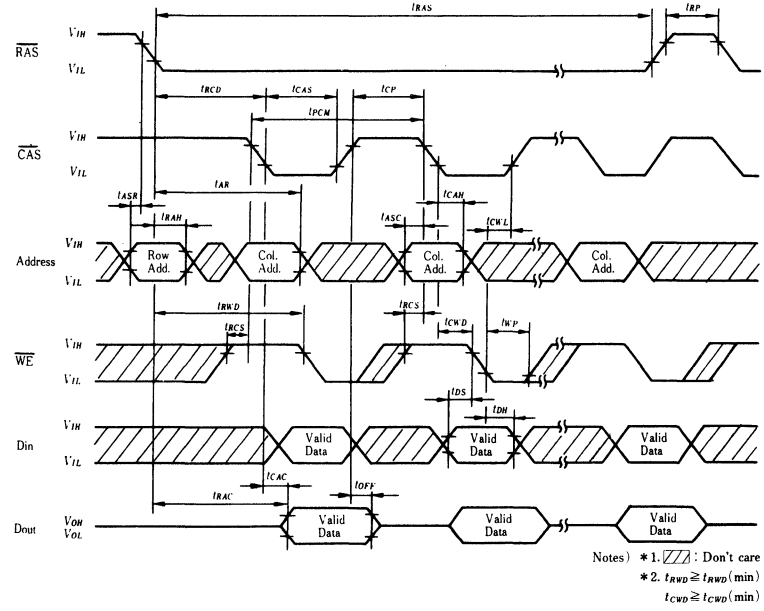
Note) ▨ : Don't care

● PAGE MODE WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$(min)

● PAGE MODE READ MODIFY WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)

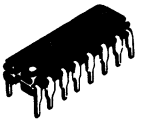
HM50257 Series

262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

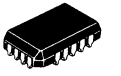
- Industry standard 16-pin DIP, 18-pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- TTL compatible
- 256 refresh cycles . . . . . (4ms)
- 3 Variations of refresh; $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

HM50257P Series



(DP-16B)

HM50257CP Series



(CP-18)

HM50257ZP Series

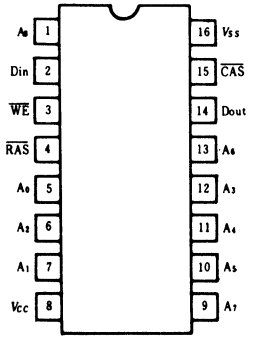
(ZP-16)

■ ORDERING INFORMATION

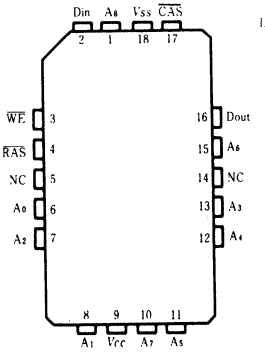
Type No.	Access Time	Package
HM50257P-12	120ns	300 mil 16 pin Plastic DIP
HM50257P-15	150ns	
HM50257P-20	200ns	
HM50257ZP-12	120ns	16 pin Plastic ZIP
HM50257ZP-15	150ns	
HM50257ZP-20	200ns	
HM50257CP-12	120ns	18 pin PLCC
HM50257CP-15	150ns	
HM50257CP-20	200ns	

■ PIN ARRANGEMENT

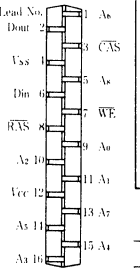
- HM50257P Series
- HM50257CP Series
- HM50257ZP Series



(Top View)



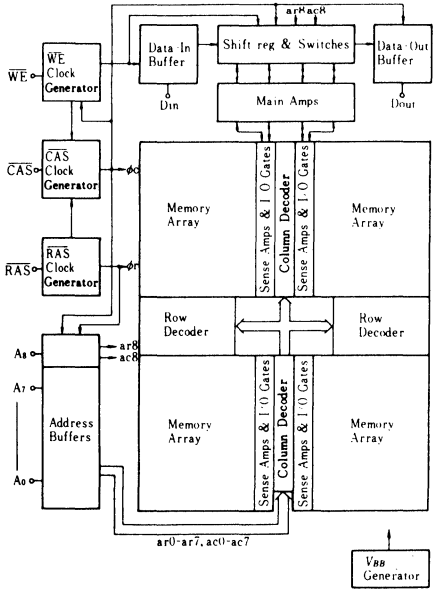
(Top View)



(Bottom View)

$A_0 \sim A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$	Refresh Address Inputs

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note 1) All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	—	83	—	70	—	55	mA	1
Stand by Current ($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current ($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current ($\overline{RAS}$=V_{IH}, Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Nibble Mode Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling, t_{NC}=min)	I_{CC8}	—	57	—	48	—	37	mA	
Input leakage (0<V_{in}<7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage (0<V_{out}<7V, Dout=Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High (I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-In	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7		1, 2
Output Capacitance	Data-Out	C_O	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}=V_{IH}$ to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1), 10), 11)]

Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
Access Time from $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rice and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Rrite Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	75	—	100	—	ns	8
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
$\overline{CAS}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	
Nibble Mode Access Time	t_{NAC}	—	25	—	25	—	35	ns	
Nibble Mode $\overline{RAS}$ Cycle Time	t_{NRC}	390	—	460	—	590	—	ns	
Nibble Mode $\overline{RAS}$ Pulse Width	t_{NRA}	290	—	350	—	460	—	ns	
Nibble Mode Cycle Time	t_{NC}	55	—	60	—	80	—	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	20	—	25	—	35	—	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	25	—	25	—	35	—	ns	

(to be continued)

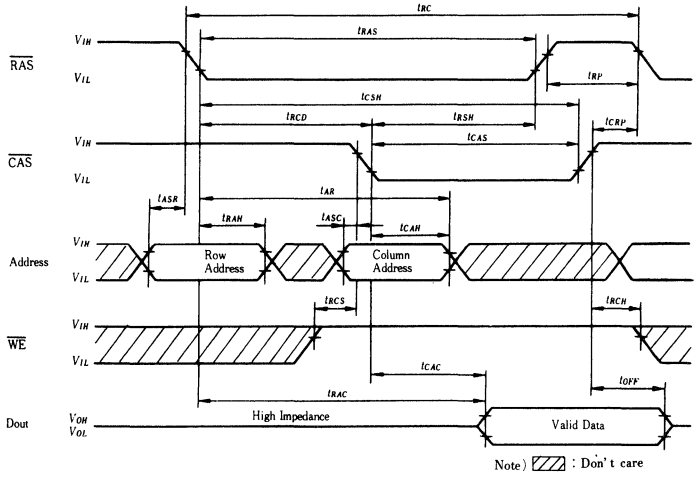
Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Nibble Mode RAS Hold Time	t_{NRSH}	40		45		55		ns	
Nibble Mode CAS to WE Delay	t_{NCWD}	20		25		35		ns	
Nibble Mode Write Command to CAS Lead Time	t_{NCWL}	20		25		35		ns	
Nibble Mode Write Command to RAS Lead Time	t_{NRWL}	40		45		55		ns	
Nibble Mode Write Command Pulse Width	t_{NWP}	20		25		35		ns	
Nibble Mode Read Write Cycle Time	t_{NRWC}	75		90		120		ns	
Nibble Mode Read Write CAS Pulse Width	t_{NCAS}	45		55		75		ns	

Notes

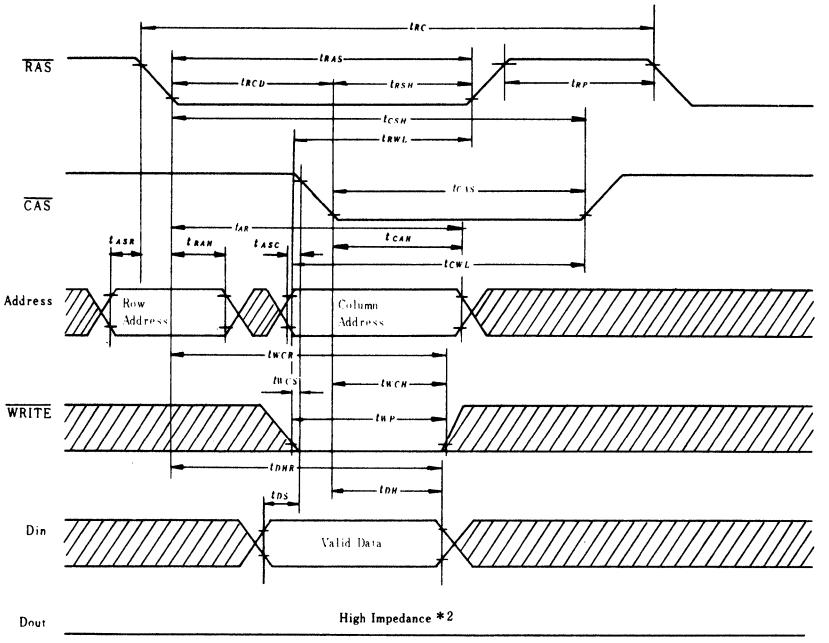
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then excute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

● READ CYCLE

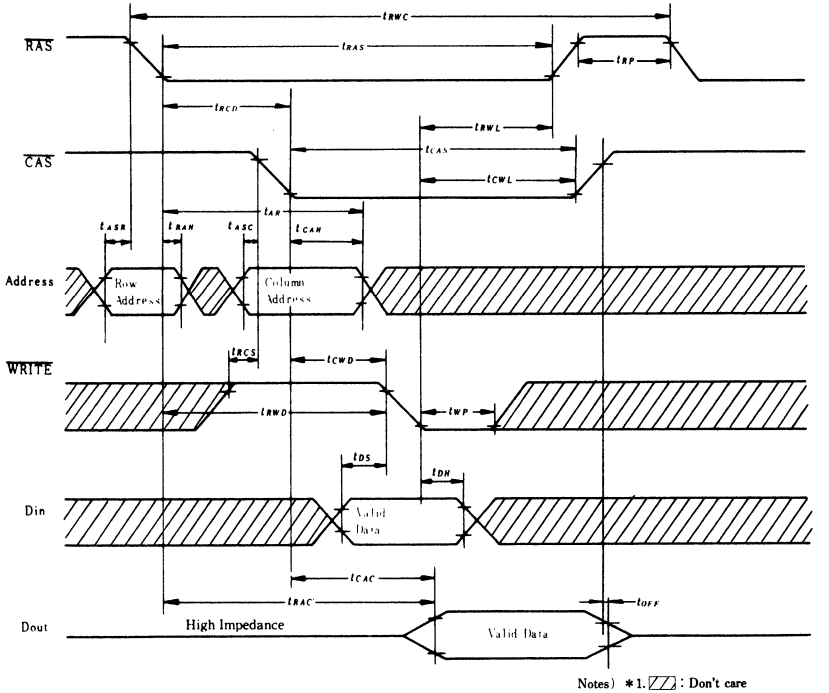


● WRITE CYCLE



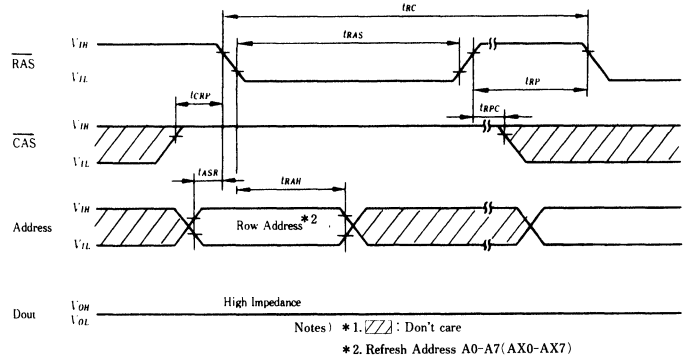
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$(min)

● READ MODIFY WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)

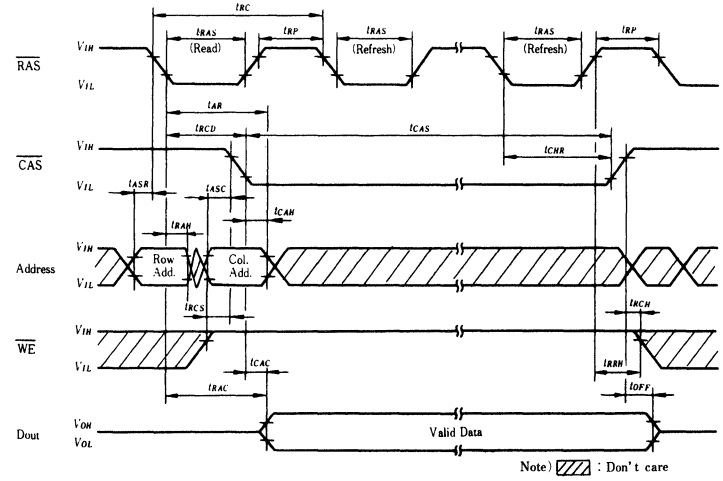
● $\overline{RAS}$ ONLY REFRESH CYCLE



Notes) *1. ▨ : Don't care

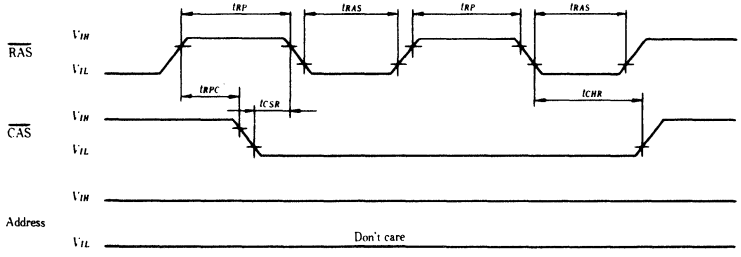
*2. Refresh Address A0-A7(AX0-AX7)

● HIDDEN REFRESH CYCLE

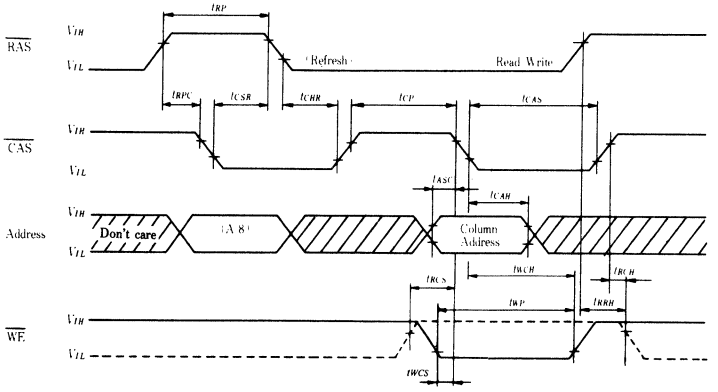


Note) ▨ : Don't care

● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

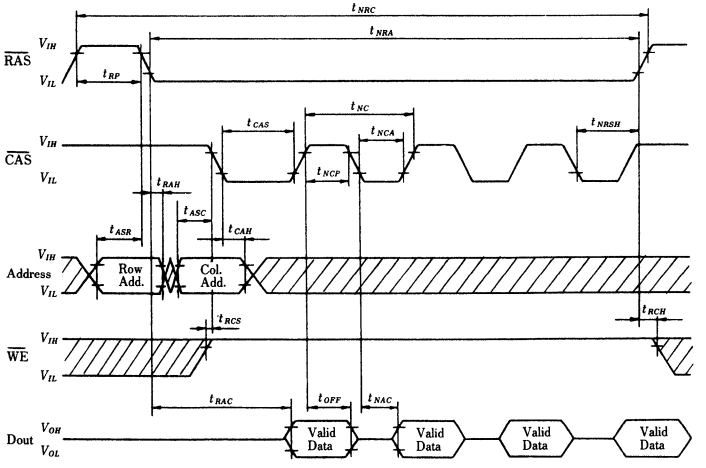


● COUNTER TEST



Notes) *1. ▨ : Don't care
*2. Dotted Line Means Read Cycle.

● NIBBLE MODE READ CYCLE



Note) ▨ : Don't care

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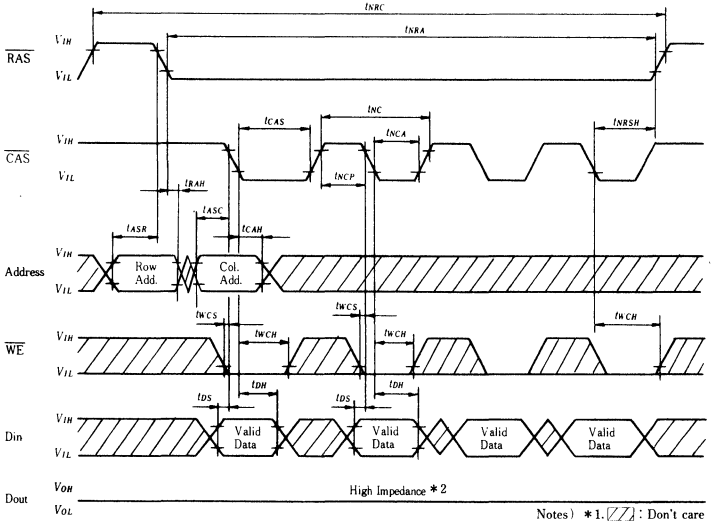
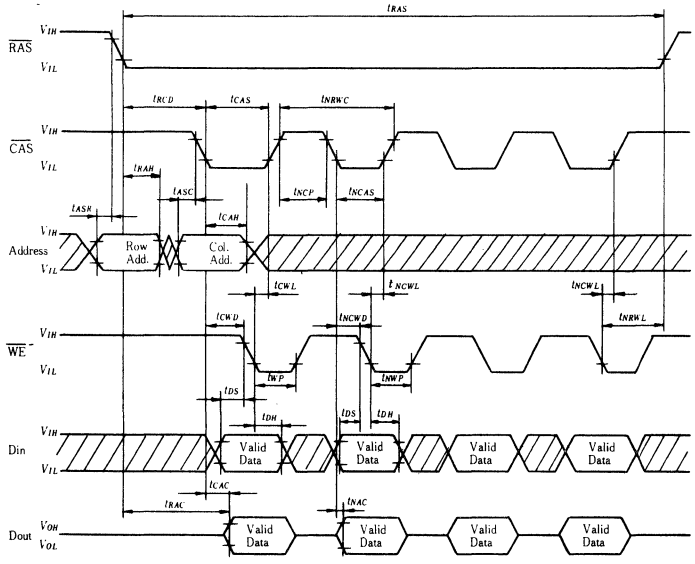
● NIBBLE MODE WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$(min)

● NIBBLE MODE READ MODIFY WRITE CYCLE

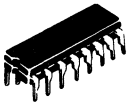


Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)

HM51256 Series

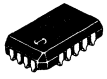
262144-word × 1-bit CMOS Dynamic Random Access Memory

HM51256P Series



(DP-16B)

HM51256CP Series



(CP-18)

HM51256ZP Series

(ZP-16)

■FEATURE

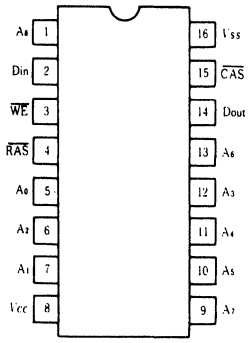
- 262, 144 word x 1 bit DRAM
- Plastic 16 pin DIP & 18 pin PLCC
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage: 5V ± 10%
- Access time
  - Row access time: 85/100/120/150ns
  - Address access time: 40/45/55/70ns
- Cycle time
  - Random read/write cycle time: 155/180/210/250ns
  - High speed page mode cycle time: 50/55/65/80ns
- Lower power
  - Standby: 11mW (TTL Level)
    1.1mW (CMOS Level: L-version)
  - Active: 385/330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
  256 cycles/32ms (L-version)
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast $\overline{CAS}$ output control

■ ORDERING INFORMATION

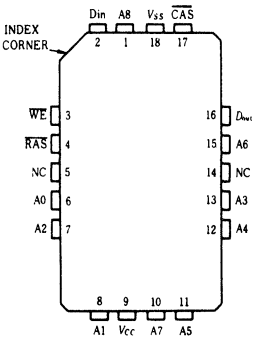
Type No.	Access Time	Package
HM51256P-8	85ns	300 mil 16 pin Plastic DIP
HM51256P-10	100ns	
HM51256P-12	120ns	
HM51256P-15	150ns	
HM51256CP-8	85ns	18 Pin PLCC
HM51256CP-10	100ns	
HM51256CP-12	120ns	
HM51256CP-15	150ns	
HM51256LP-8	85ns	300 mil 16 pin Plastic DIP
HM51256LP-10	100ns	
HM51256LP-12	120ns	
HM51256LP-15	150ns	
HM51256LCP-8	85ns	18 pin PLCC
HM51256LCP-10	100ns	
HM51256LCP-12	120ns	
HM51256LCP-15	150ns	
HM51256ZP-8	85ns	16 pin Plastic ZIP
HM51256ZP-10	100ns	
HM51256ZP-12	120ns	
HM51256ZP-15	150ns	
HM51256LZP-8	85ns	
HM51256LZP-10	100ns	
HM51256LZP-12	120ns	
HM51256LZP-15	150ns	

■ PIN ARRANGEMENT

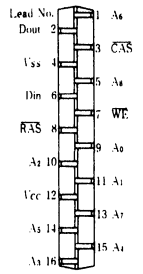
- HM51256P Series
- HM51256CP Series
- HM51256ZP Series



(Top View)



(Top View)



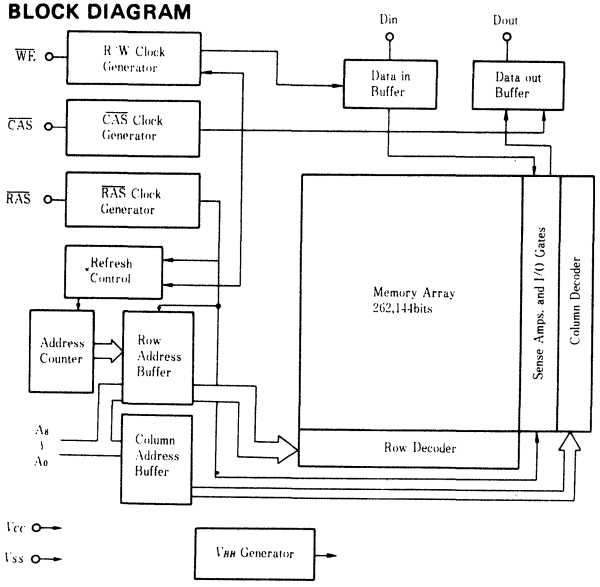
(Bottom View)

$A_0 - A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_7$	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	–	70	–	60	–	50	–	40	mA	1
Standby Current ($\overline{RAS}$= V_{IH}, Dout=High Impedance)	I_{CC2}	–	2	–	2	–	2	–	2	mA	
Refresh Current ($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	–	70	–	60	–	50	–	40	mA	
Standby Current ($\overline{RAS}$= V_{IH}, Dout Enable)	I_{CC4}	–	6	–	6	–	6	–	6	mA	1
Refresh Current ($\overline{CAS}$ before RAS Refresh, t_{RC}=min)	I_{CC5}	–	60	–	55	–	45	–	35	mA	
High Speed Page Mode Supply Current ($\overline{RAS}$= V_{IL}, $\overline{CAS}$ Cycling, t_{PC}=min.)	I_{CC6}	–	70	–	60	–	50	–	40	mA	1
Standby Current ($\overline{RAS}$, $\overline{CAS}$= V_{CC}−0.2V)	I_{CC7}	–	200	–	200	–	200	–	200	μA	2
Input leakage (0< V_{in}<7V)	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage (0< V_{out}<7V, Dout=Distable)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA	
Output levels High (I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. This specification is guaranteed only for L-version.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1
Output Capacitance	Data-out	C_O	–	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	–	25	–	30	–	35	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	–	75	–	90	–	110	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms	
		–	32	–	32	–	32	–	32	ms	21

● Read Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6

● Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

● Read-Modify-Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10

● Refresh Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Prechange to $\overline{CAS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

● High Speed Page Mode Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time	t_{PC}	50	–	55	–	65	–	80	–	ns	18, 20
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RAPC}	55	75000	65	75000	75	75000	95	75000	ns	19
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	20	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	
Access Time from Column Precharge Time	t_{CAP}	–	45	–	50	–	60	–	75	ns	20

● High Speed Page Mode Read-Modify-Write Cycle

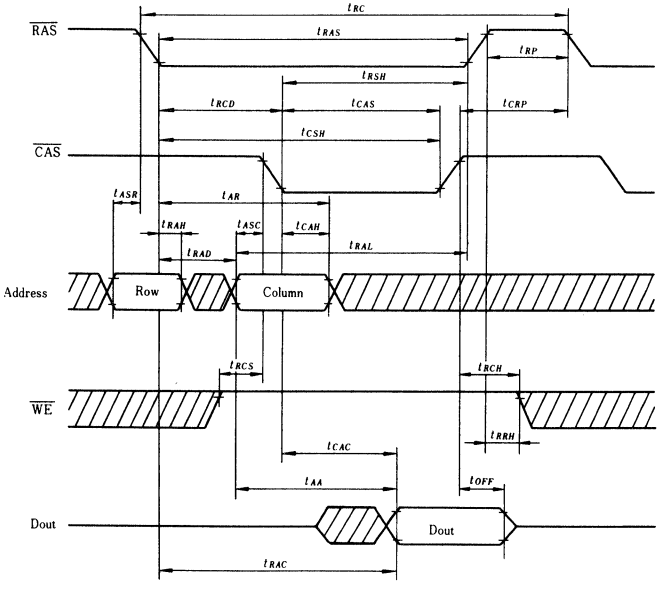
Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time on Read-Write	t_{RWPC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15

Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value show in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a Reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWPC} (min) = t_{AWD} (min) + t_{WAD} (max) + t_T.
13. Assumes that $t_{WAD} \leqq t_{WAD}$ (max). If t_{WAD} is greater than the maximum recomended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$ (max).
15. Operation with the t_{WAD} (max) limit insures that t_{PWA} (max) can be met, t_{WAD} (max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. An intial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
17. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.
18. Assumes that $t_{ASC} = t_{CP} - 5$ ns.
19. t_{RAPC} defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
20. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
21. This specification is guaranteed only for L-version.

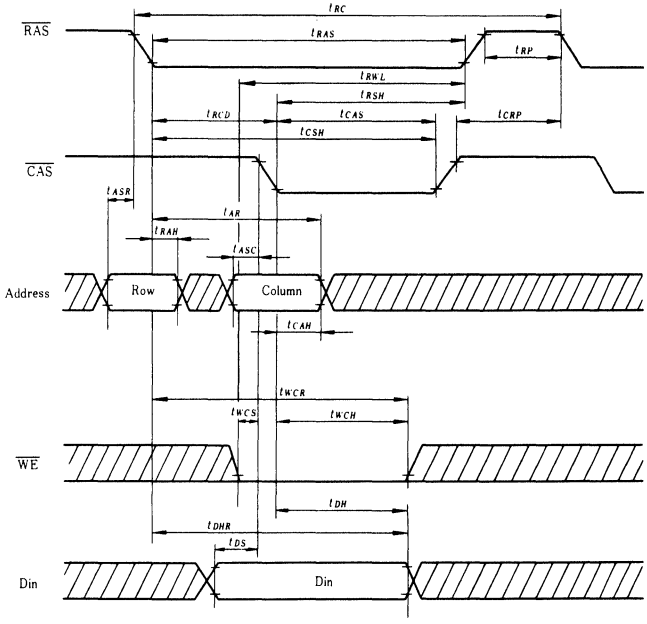
■TIMING WAVEFORMS

●Read Cycle



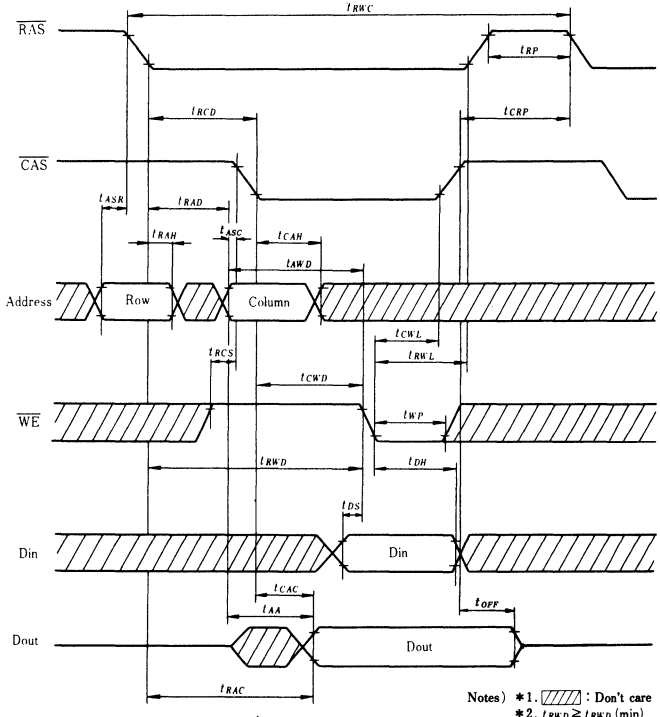
Note) ▨ : Don't care

● Write Cycle



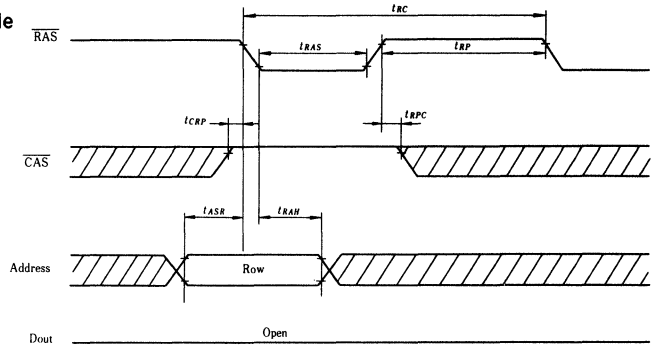
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$(min)

● Read Modify Write Cycle



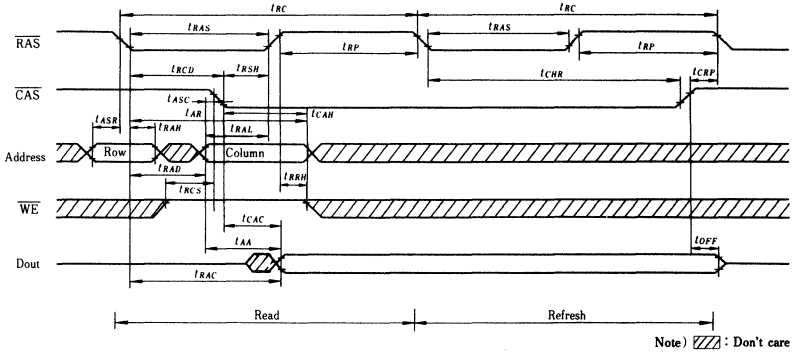
Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)
$t_{AWD} \geqq t_{AWD}$(min)

● $\overline{RAS}$ Only Refresh Cycle



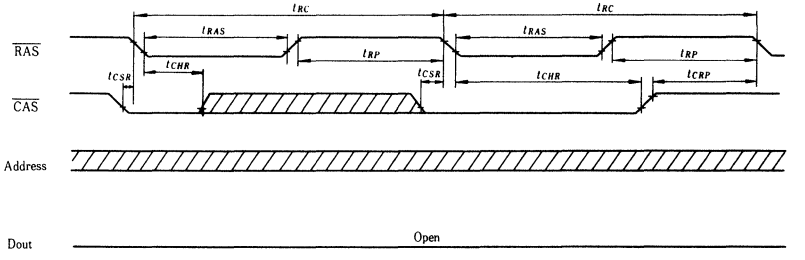
Note) ▨ : Don't care

● Hidden Refresh Cycle



Note) ▨ : Don't care

● $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note) ▨ : Don't care

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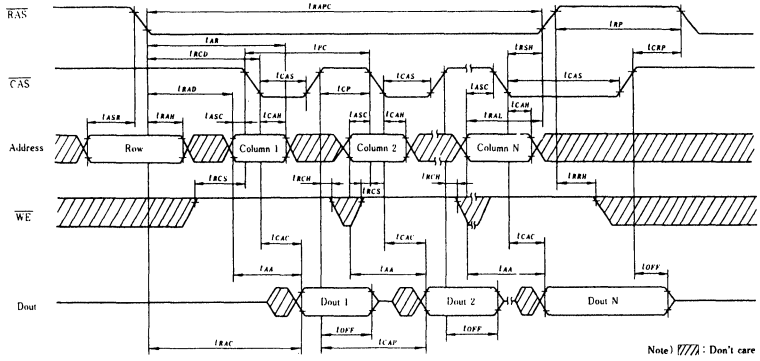
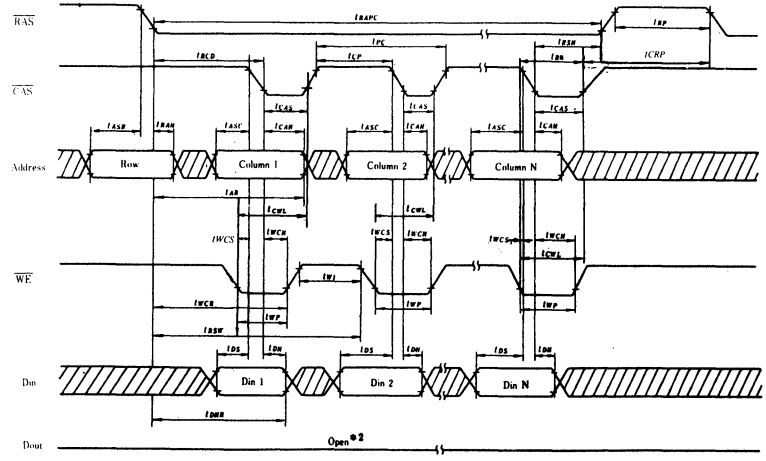
● High Speed Page Mode Read Cycle



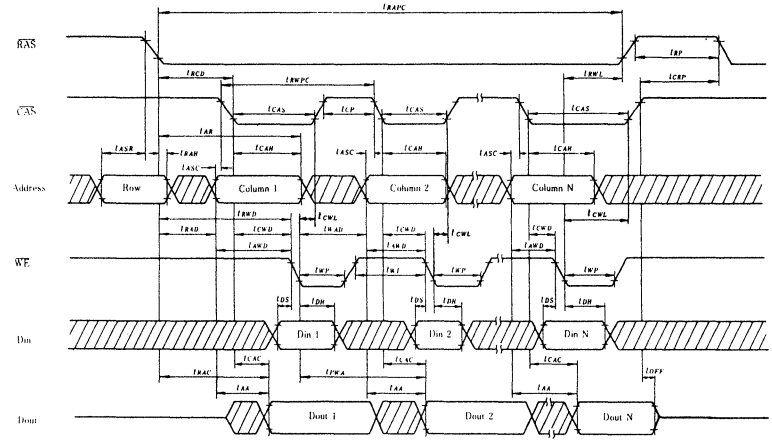
Note) ▨ : Don't care

● High Speed Page Mode Write Cycle



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

● High Speed Page Mode Read Modify Write Cycle

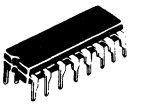


Note) ▨ : Don't care

HM51258 Series

262144-word x 1-bit Static Column CMOS Dynamic RAM

The HM51258 is the 262,144 word by 1 bit static column dynamic random access memory utilizing the Hitachi 2μm CMOS process.
This device has static column circuit and it is good for high performance main storage or for page access applications.
While the row circuitry is still dynamic, and it controls the power consumed in the static circuitry. It realizes very low power dissipation.
Multiplexed address and the 16 pin pinout are compatible with the fully dynamic 256K DRAM HM50256.

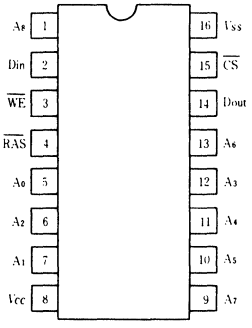


(DP-16B)

■ FEATURES

- 262,144 word x 1 bit SCRAM
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage 5V ± 10%
- Access time
  Row access time: 85/100/120/150ns
  Address access time: 40/45/55/70ns
- Cycle time
  Random Read&Write cycle time: 155/180/210/250ns
  Static Column cycle time: 45/50/60/75ns
- Lower power
  Standby: 11mW
  Active: 385/330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh
- Static column mode capability
- Edge triggered write capability
- Fast $\overline{CS}$ output control

■PIN ARRANGEMENT

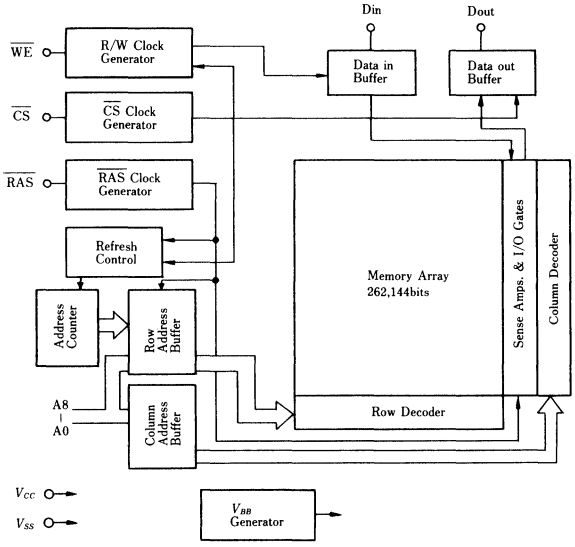


(Top View)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM51258P-8	85ns	300 mil 16 pin Plastic DIP
HM51258P-10	100ns	
HM51258P-12	120ns	
HM51258P-15	150ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=0 to +70°C)

Parameter	Sybmol	Test conditions	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Note
			min	max	min	max	min	max	min	max		
Operating current	I_{CC1}	RAS, CS Cycling; t_{RC}=min.	–	70	–	60	–	50	–	40	mA	1
Standby current	I_{CC2}	RAS=V_{IH}, Dout=High Impedance	–	2	–	2	–	2	–	2	mA	
Refresh current	I_{CC3}	RAS only Refresh, t_{RC}=min	–	70	–	60	–	50	–	40	mA	
Standby current	I_{CC4}	RAS=V_{IH}, Dout Enable	–	6	–	6	–	6	–	6	mA	1
Refresh current	I_{CC5}	CS before RAS Refresh, t_{RC}=min	–	60	–	55	–	45	–	35	mA	
Operating current	I_{CC6}	Static Column Mode, t_{RSC}, t_{WSC}=min	–	70	–	60	–	50	–	40	mA	1
Input leakage	I_{LI}	V_{in}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage	I_{LO}	V_{out}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{out}=−5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{out}=4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.

■ CAPACITANCE (V_{CC}=5V±10%, T_a=25°C)

Parameter		Symbol	typ	max	Unit	Note
Input capacitance	Address, Data-In	C_{I1}	–	5	pF	1
	Clock	C_{I2}	–	7	pF	1
Output capacitance	Data-Out	C_O	–	7	pF	1, 2

Note) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%)

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
$\overline{CS}$ Pulse Width	t_{CS}	25	–	25	–	30	–	35	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
$\overline{CS}$ Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-Up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms	
• Read Cycle											
Access Time from $\overline{RAS}$	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CS}$	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Column Address Hold Time to $\overline{RAS}$ on Read	t_{AR}	85	–	100	–	120	–	150	–	ns	
Read Command Set-Up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
$\overline{RAS}$ to Column Address Hold Time	t_{AH}	10	–	15	–	15	–	20	–	ns	16
Output Hold Time from Address	t_{OH}	5	–	5	–	5	–	5	–	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6
• Write Cycle											
Column Address Set-Up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to $\overline{RAS}$ on Write	t_{AWR}	60	–	75	–	90	–	110	–	ns	
Write Command Set-Up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

(to be continued)

• Read-Modify-Write Cycle

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10
Output Hold Time from $\overline{WE}$	t_{OHW}	25	–	25	–	25	–	25	–	ns	

• Refresh Cycle

$\overline{CS}$ Set-up Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

• SC Mode Cycle

SC Mode Cycle Time on Read	t_{RSC}	45	–	50	–	60	–	75	–	ns	
SC Mode Cycle Time on Write	t_{WSC}	45	–	50	–	60	–	75	–	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
SC Mode $\overline{RAS}$ Pulse Width	t_{RASC}	55	75000	65	75000	75	75000	95	75000	ns	
$\overline{CS}$ Precharge Time	t_{CP}	10	–	10	–	15	–	15	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	

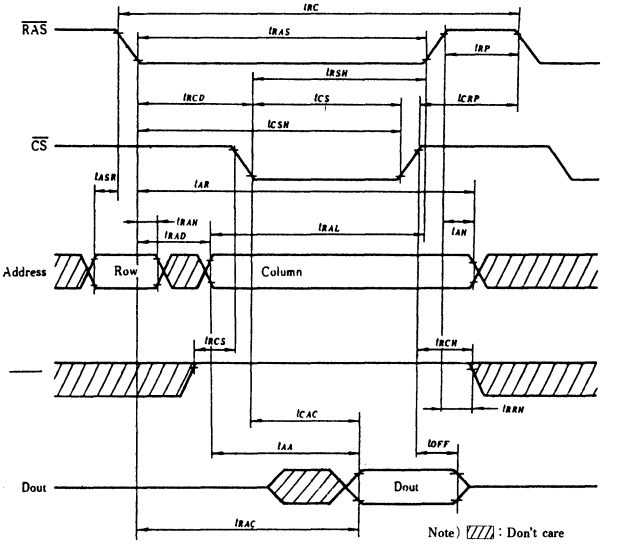
• SC Mode Read-Modify-Write and Mixed Cycle

SC Mode Cycle Time on Read-Write	t_{RWSC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15
Column Address Hold Time to Previous $\overline{WE}$	t_{PWH}	80	–	90	–	110	–	140	–	ns	

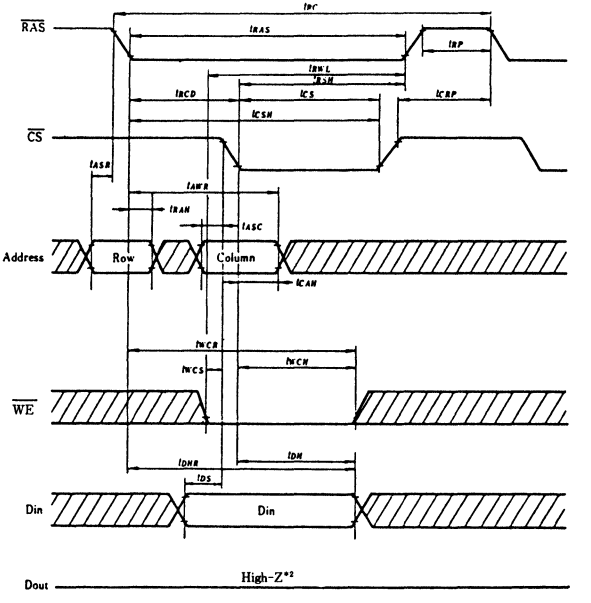
Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \leqq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max), $t_{RAD} \leqq t_{RAD}$(max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \geqq t_{RAD}$(max).
6. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$(min), $t_{CWD} \geqq t_{CWD}$(min) and $t_{AWD} \geqq t_{AWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWSC}(min) = t_{AWD}(min) + t_{WAD}(max) + t_T
13. Assumes that $t_{WAD} \leqq t_{WAD}$(max). If t_{WAD} is greater than the maximum recomended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$(max).
15. Operation with the t_{WAD}(max) limit insures that t_{PWA}(max) can be met, t_{WAD}(max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD}(max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} defines the time at which the column address hold.
17. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
18. At least, 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

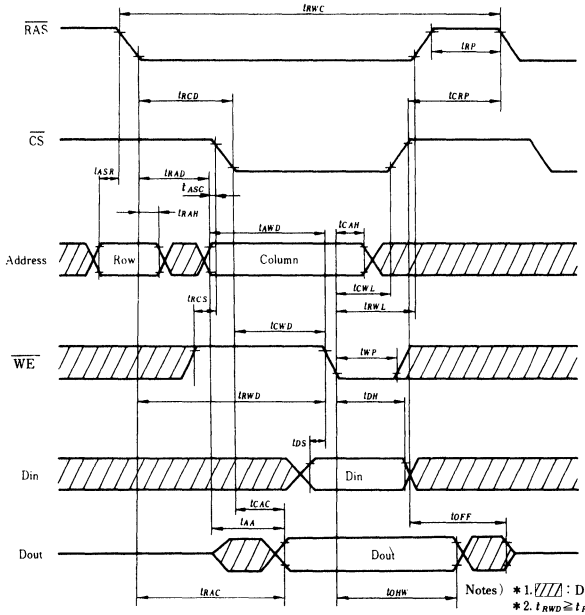
● Read Cycle



● Write Cycle

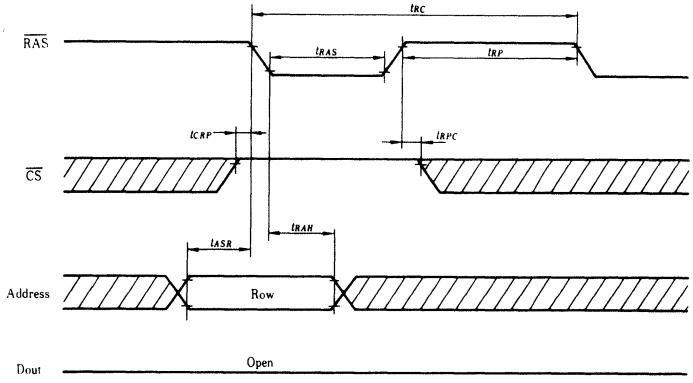


• Read-Modify-Write Cycle



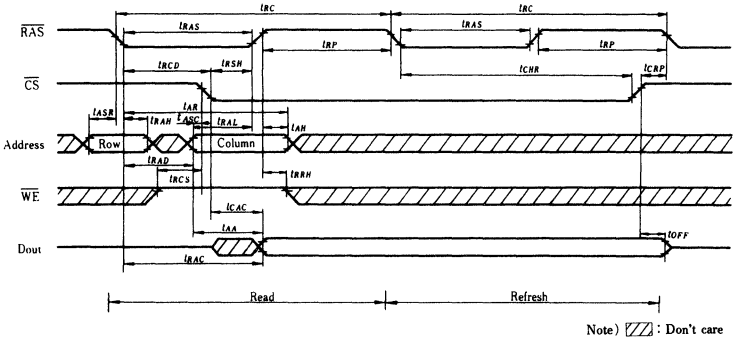
Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)
$t_{AWD} \geqq t_{AWD}$(min)

• $\overline{RAS}$ Only Refresh Cycle



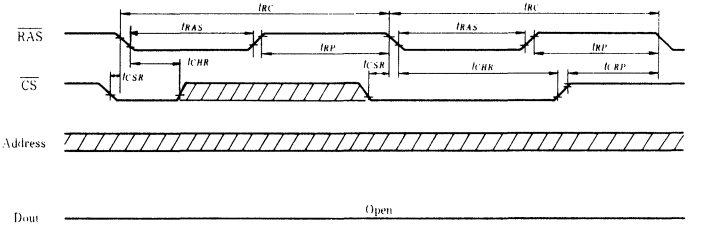
Note) ▨ : Don't care

• Hidden Refresh Cycle



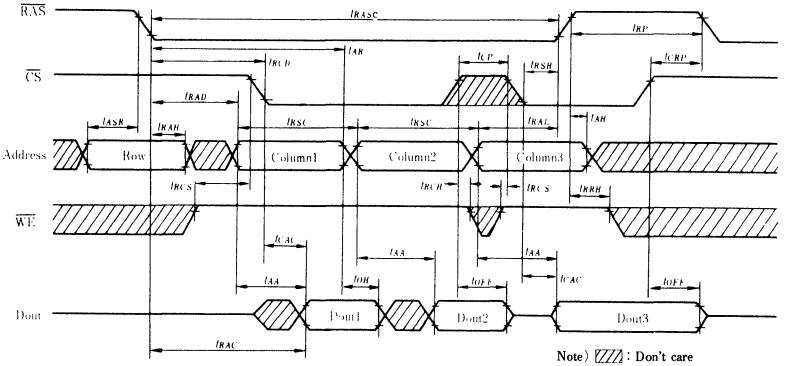
Note) ▨ : Don't care

• $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle



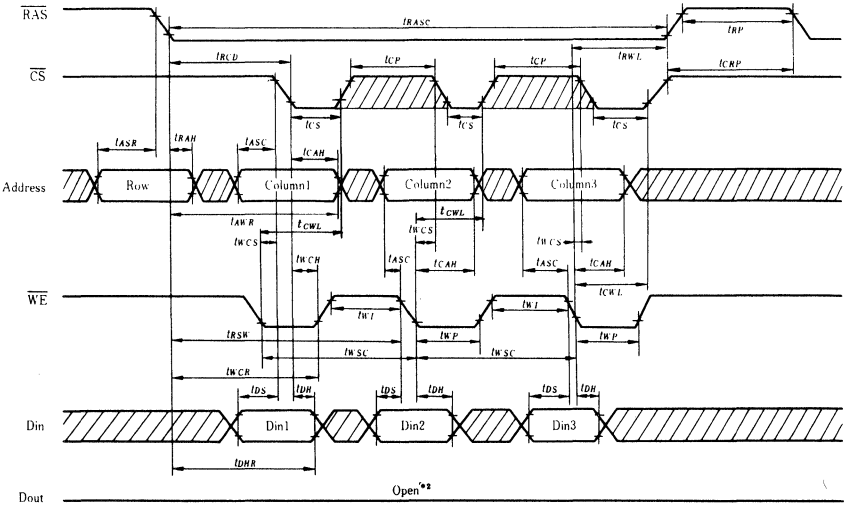
Note) ▨ : Don't care

• Static Column Mode Read Cycle



Note) ▨ : Don't care

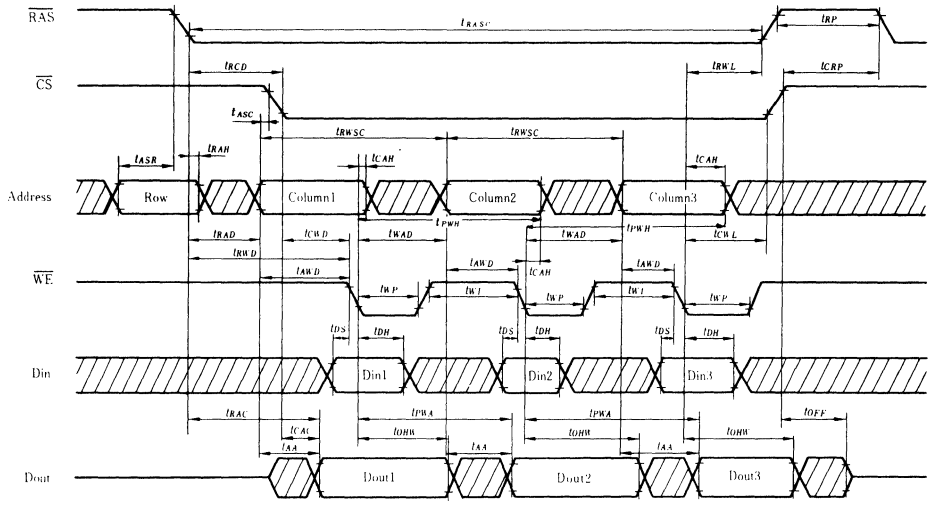
• Static Column Mode Write Cycle



Notes) *1. ▨ : Don't care

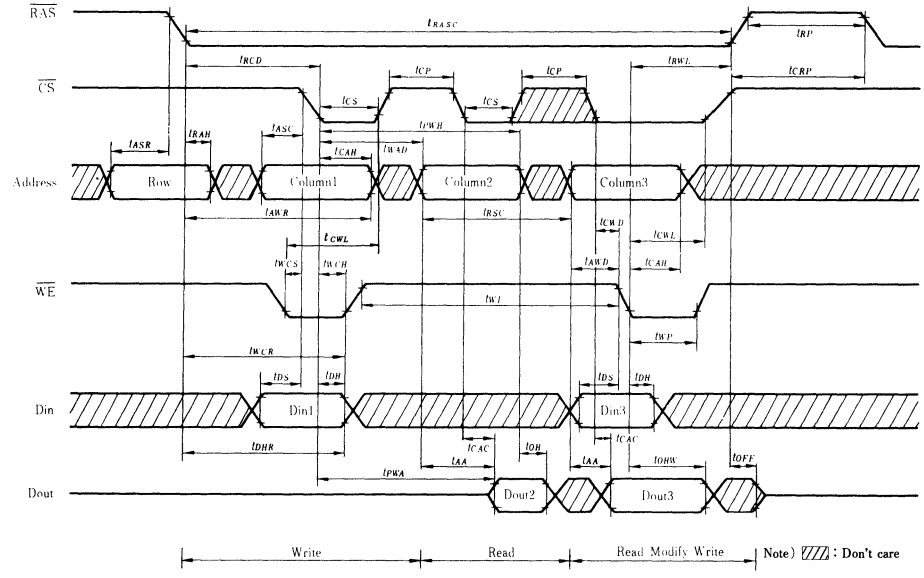
*2. $t_{WCS} \geqq t_{WCS}$(min)

• Static Column Mode Read-Modify-Write Cycle



Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)
$t_{AWD} \geqq t_{AWD}$(min)

• Static Column Mode Mixed Cycle



Note) ▨ : Don't care

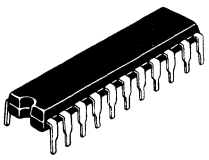
HM514256 Series — Preliminary

262144-word x 4-bit CMOS Dynamic Random Access Memory

The Hitachi HM514256 Series is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514256 has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM514256 offers Page Mode as a high speed access mode.

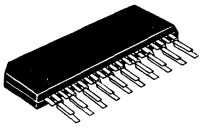
Multiplexed address input permits the HM514256 to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514256P Series



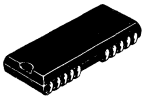
(DP-20NA)

HM514256ZP Series



(ZP-20)

HM514256JP Series



(CP-20D)

Features

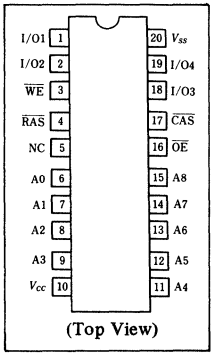
- High Speed . . . . . Access Time 100/120/150 ns (max)
- Lower Power . . . . Active 300 mW, Standby 11mW
- Single 5V (±10%)
- Page Mode
- 512 refresh cycle . . . . . 8 ms
- 2 variations of refresh . . . . . $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh

Ordering Information

Type No.	Access Time	Package
HM514256P-10	100 ns	
HM514256P-12	120ns	300 mil 20 pin Plastic DIP
HM514256P-15	150ns	
HM514256ZP-10	100ns	
HM514256ZP-12	120ns	20 pin Plastic ZIP
HM514256ZP-15	150ns	
HM514256JP-10	100ns	
HM514256JP-12	120ns	20 pin Plastic SOJ
HM514256JP-15	150ns	

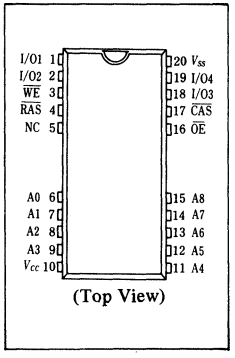
Pin Arrangement

HM514256P Series



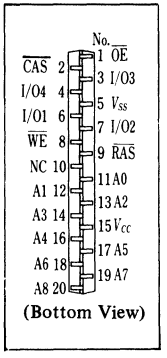
(Top View)

HM514256JP Series



(Top View)

HM514256ZP Series



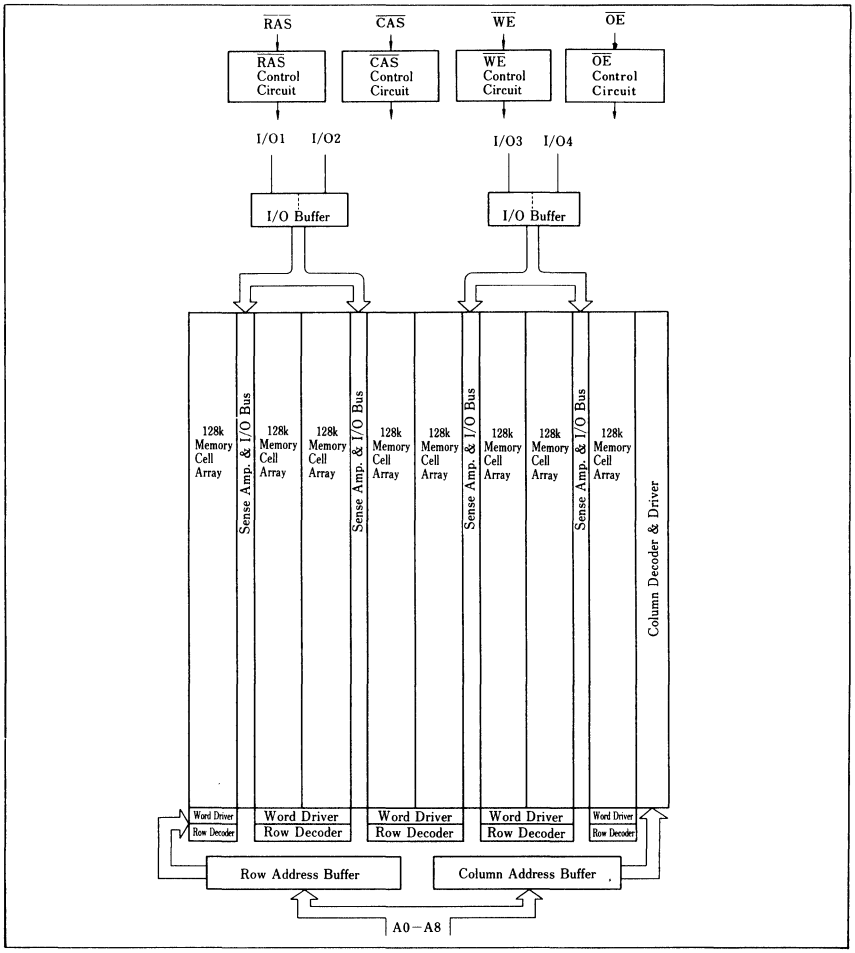
(Bottom View)

Pin Description

A0 - A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O - I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 - A8	Refresh Address Input

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . -55°C to +125°C
Power dissipation . . . . . 1 W
Short circuit output current . . . . . 50 mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	−2.0	–	0.8	V

Note) 1. All voltages referenced to V_{SS}.
2. V_{IL} (min) = −1.0V on I/O1-I/O4.

DC Electrical Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	Min	Max	Unit	Notes
Operating current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	I_{CC1}	–	40 47 55	mA	*1, *4
Standby current	I_{CC2}	–	2	mA	TTL Interface
		–	1	mA	CMOS Interface
Refresh current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	I_{CC3}	–	40 47 55	mA	$\overline{RAS}$ only Refresh *1
Standby current (Dout Enable) $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$	I_{CC5}	–	5	mA	*1
Refresh current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	I_{CC6}	–	40 47 55	mA	$\overline{CAS}$ before $\overline{RAS}$ Refresh
Operating current t_{RC} = 105 ns t_{RC} = 85 ns t_{RC} = 70 ns	I_{CC7}	–	40 47 55	mA	*1, *5 Page mode
Input leakage $0 < Vin < 7V$	I_{LI}	–10	10	μA	
Output leakage $0 < Vout < 7V$	I_{LO}	–10	10	μA	Dout is disabled
Output levels High Iout = –5 mA	V_{OH}	2.4	V_{CC}	V	
Low Iout = 4.2 mA	V_{OL}	0	0.4	V	

Capacitance

Parameter	Symbol	Typ	Max	Unit	Notes
Address	C_{I1}	–	5	pF	*2
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	–	7	pF	*2
Data-In/Data-Out	$C_{I/O}$	–	10	pF	*2, *3

Notes) *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
*2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*3. $\overline{CAS} = V_{IH}$ to disable Dout.
*4. Address can be changed less than 3 times while $\overline{RAS}$ is V_{IL}.
*5. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Electrical Characteristics and Recommended AC Operating Conditions

($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$)*1,*10,*11

Parameter	Symbol	HM514256-10		HM514256-12		HM514256-15		Unit	Notes
		min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	*2,*3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	*3,*4
Output Buffer Turn-off Delay	t_{OFF1}	–	25	–	30	–	40	ns	*5
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	25	–	30	–	40	ns	*5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	*6
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	

(to be continued)

Parameter	Symbol	HM514256-10		HM514256-12		HM514256-15		Unit	Notes
		min	max	min	max	min	max		
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	*7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	25	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	*8
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	*9
Data-in Hold Time	t_{DH}	20	–	25	–	30	–	ns	*9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	8	–	8	–	8	ms	
Read-Write Cycle Time	t_{RWC}	265	–	305	–	360	–	ns	
Read Modify Write Cycle Time	t_{RWS}	175	–	205	–	250	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	135	–	160	–	200	–	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	*8
$\overline{CAS}$ Setup Time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
Page Mode Read or Write Cycle	t_{PC}	70	–	85	–	105	–	ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	10	–	15	–	20	–	ns	
Page Mode Read Modify Write Cycle	t_{PCM}	145	–	170	–	205	–	ns	
Page Mode CAS Pulse Width (Read Modify Write Cycle)	t_{CRW}	125	–	145	–	175	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	25	–	30	–	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{CAS}$ to Data-in Delay Time	t_{CDD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time reference to Write	t_{OEH}	25	–	30	–	35	–	ns	
$\overline{OE}$ Delay Time from Din	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Delay Time from Din	t_{DZC}	0	–	0	–	0	–	ns	

Notes) *1. AC measurements assume t_T = 5 ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).

*5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

*7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.

*8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

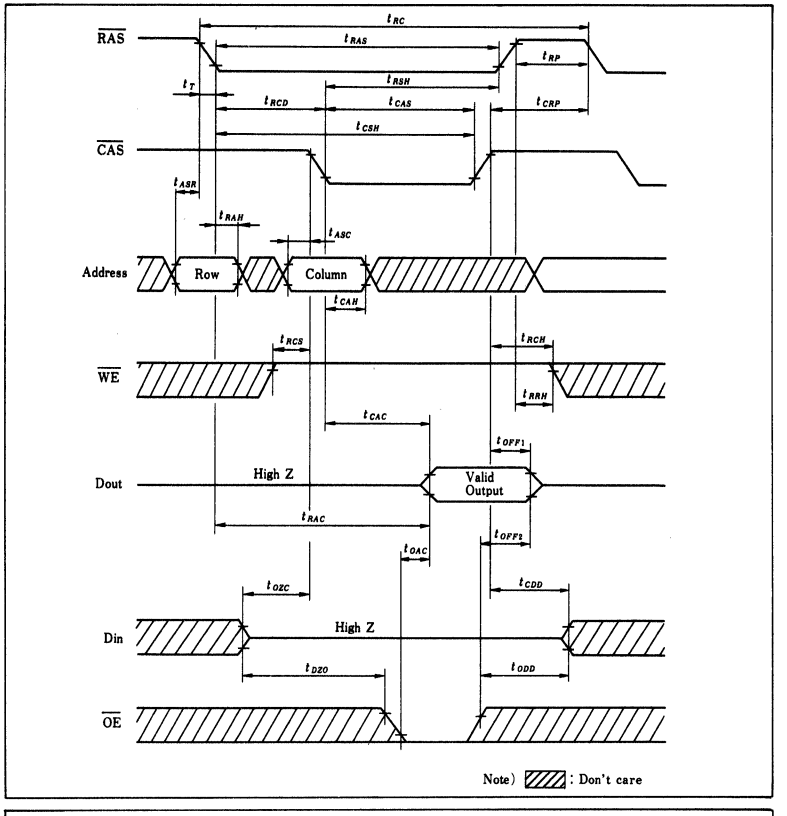
*9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

*10. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

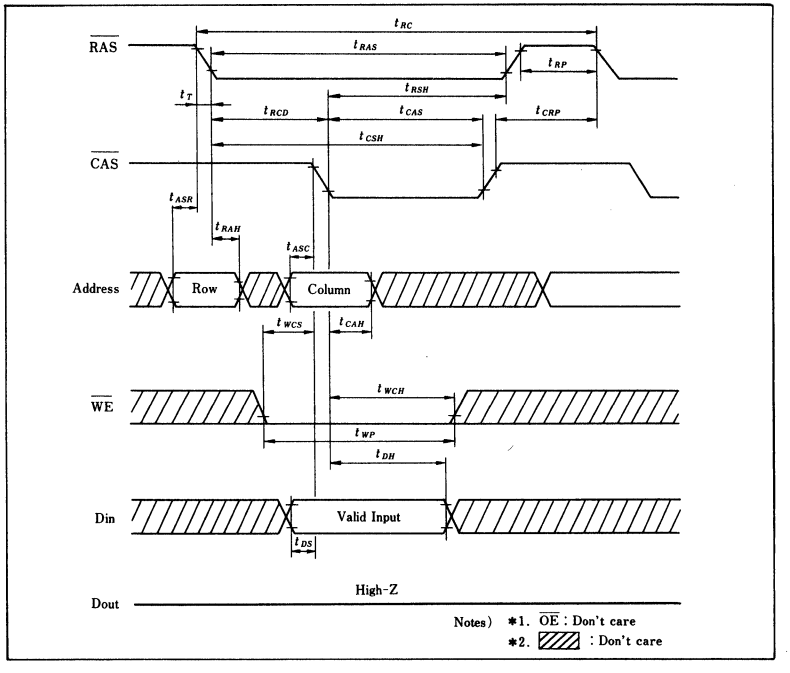
*11. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

Timing Waveforms

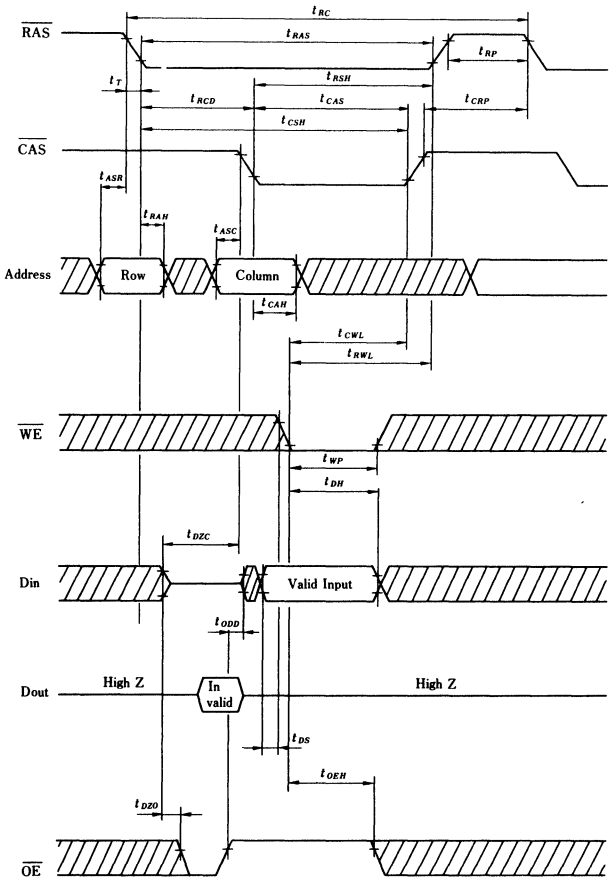
Read Cycle



Early Write Cycle

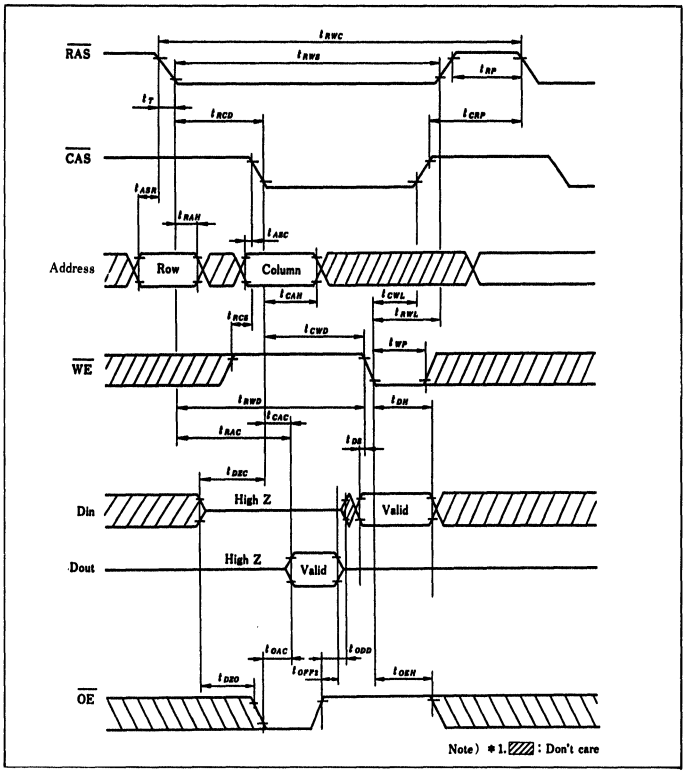


Delayed Write Cycle

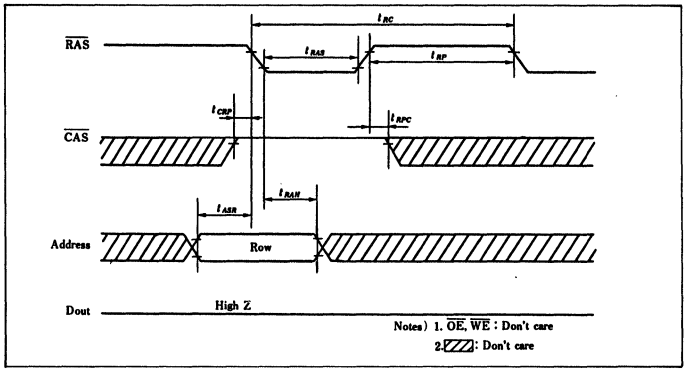


Note) *1. ▨ : Don't care

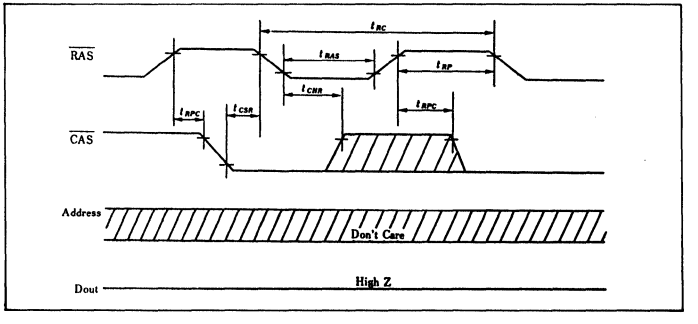
Read Modify Write Cycle



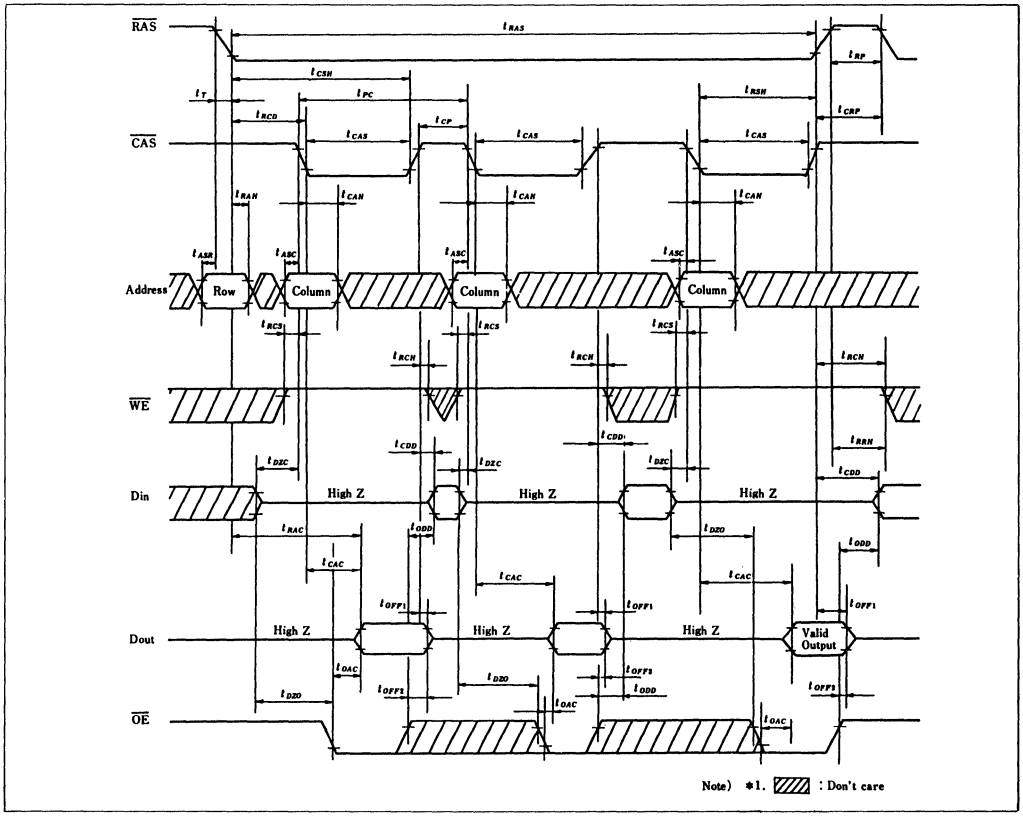
RAS Only Refresh Cycle



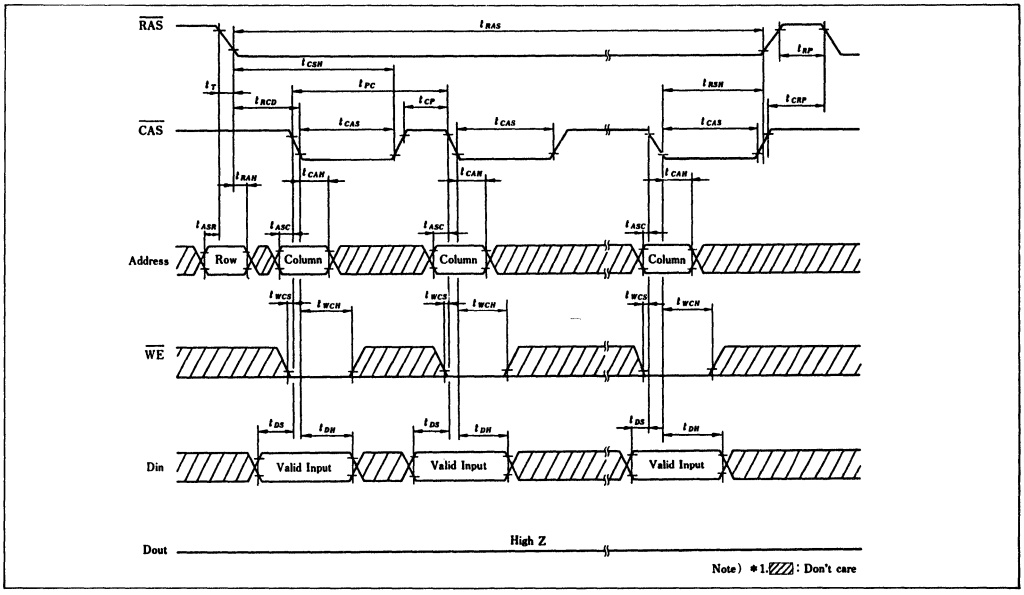
CAS before RAS Refresh Cycle



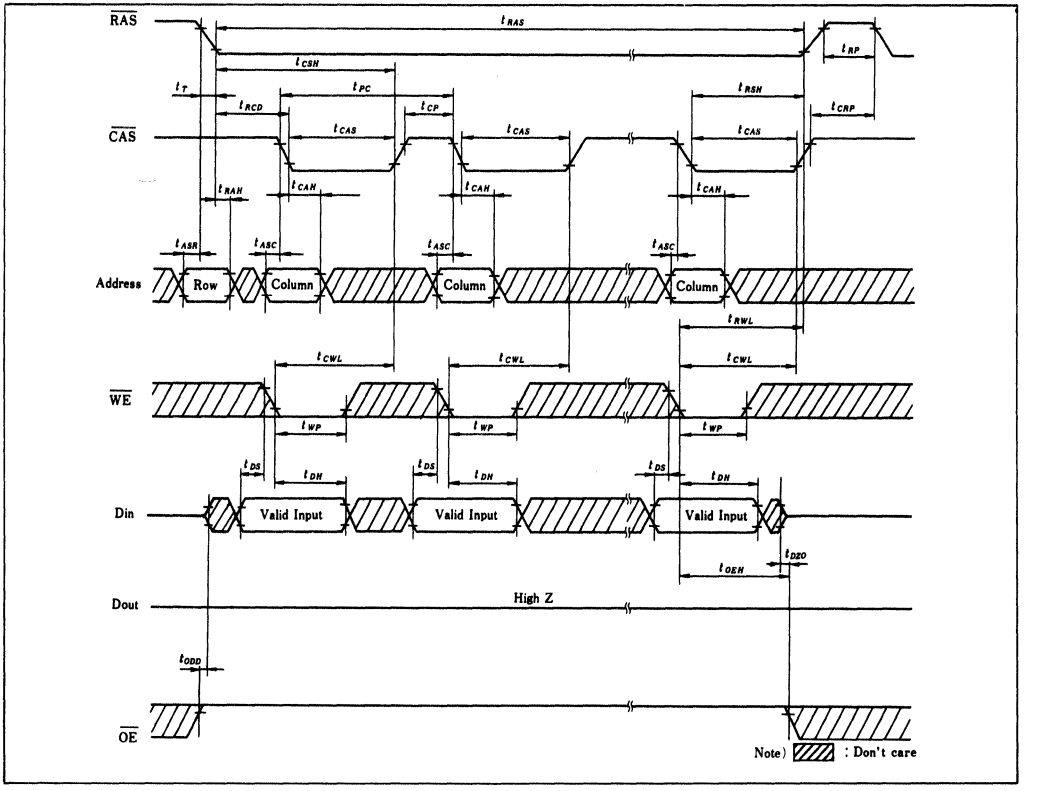
Page Mode Read Cycle



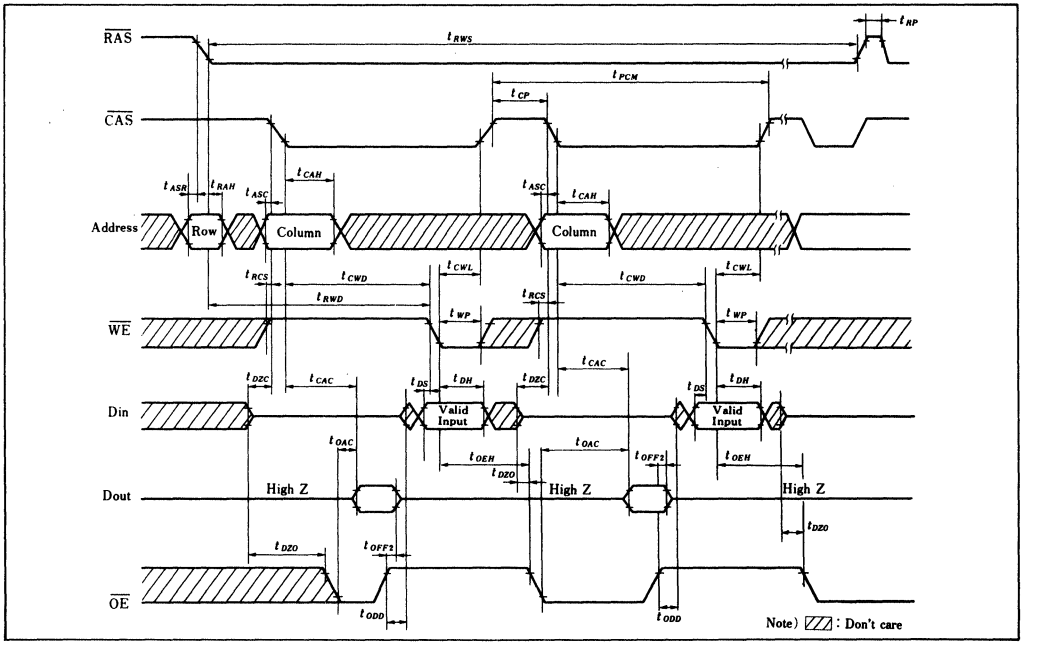
Page Mode Early Write Cycle



Page Mode Delayed Write Cycle



Page Mode Read Modify Write Cycle



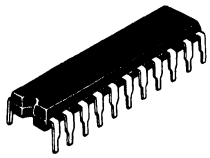
HM514258S Series —Under Development

262144-word x 4-bit CMOS Dynamic Random Access Memory

The Hitachi HM514258 Series is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514258 has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM514258 offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM514258 to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514258P Series

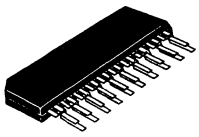


(DP-20NA)

HM514258JP Series

(CP-20D)

HM514258ZP Series



(ZP-20)

Features

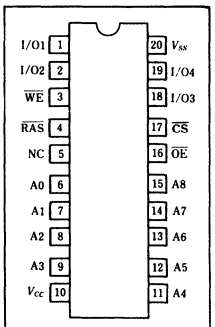
- High speed . . . . . Access Time 100/120/150 ns (max.)
- Low power . . . . . Active 302.5 mW, Standby 11 mW
- Static Column mode capability
- Single 5 V (±10%)
- 512 refresh cycle . . . . . 8 ms
- 2 variations of refresh . . . . . $\overline{RAS}$ only refresh
  $\overline{CS}$ before $\overline{RAS}$ refresh

Ordering Information

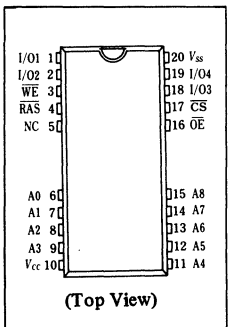
Type No.	Access Time	Package
HM514258P-8S	80ns	300 mil 20 pin Plastic DIP
HM514258P-10S	100ns	
HM514258P-12S	120ns	
HM514258ZP-8S	80ns	20 pin Plastic ZIP
HM514258ZP-10S	100ns	
HM514258ZP-12S	120ns	
HM514258JP-8S	80ns	20 pin Plastic SOJ
HM514258JP-10S	100ns	
HM514258JP-12S	120ns	

Pin Arrangement

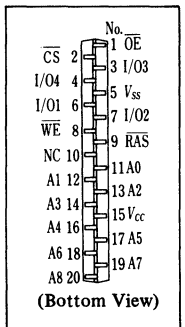
- HM514258P Series
- HM514258JP Series
- HM514258ZP Series



(Top View)



(Top View)

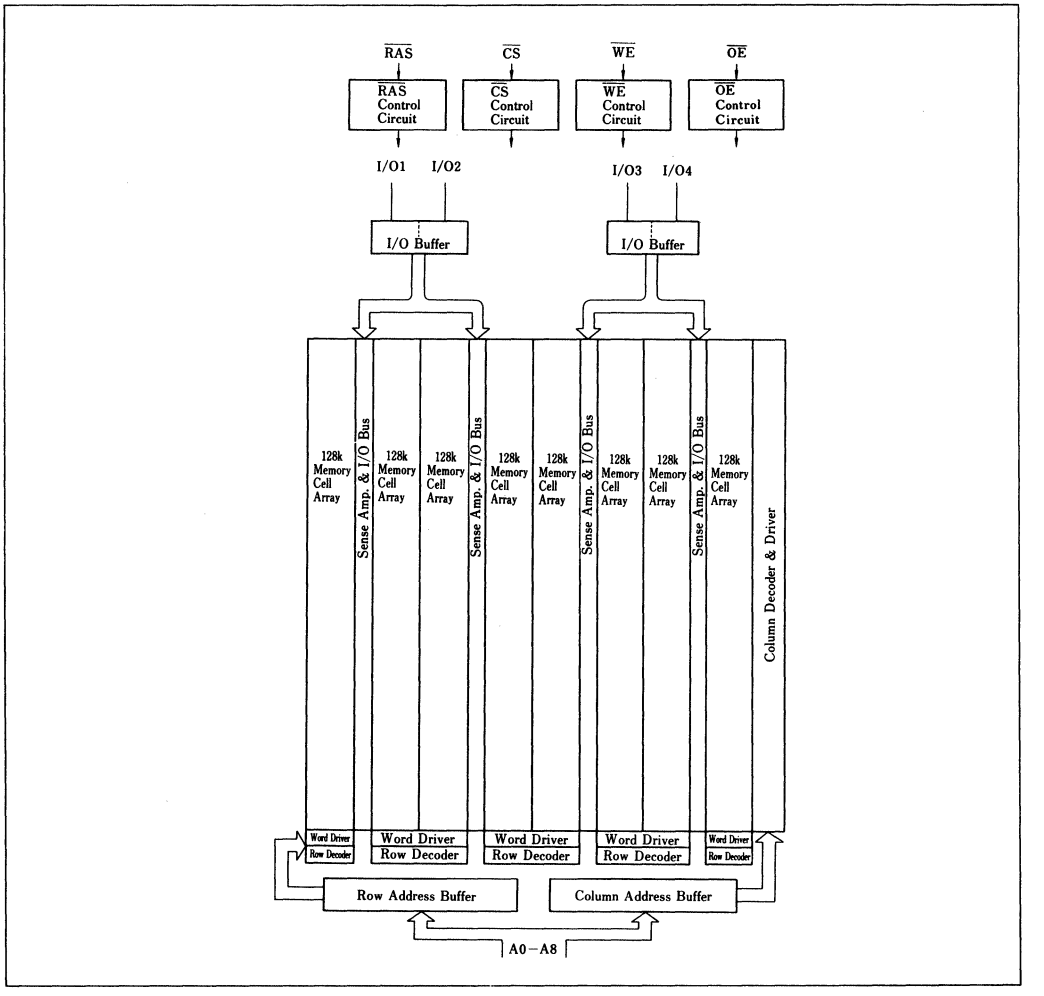


(Bottom View)

Pin Description

A0 – A8	Address Inputs
$\overline{CS}$	Chip Select
I/O1 – I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 – A8	Refresh Address Inputs

Functional Block Diagram



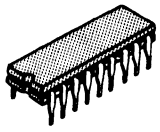
HM511000 Series

1048576-word x 1-bit CMOS Dynamic Random Access Memory

The Hitachi HM511000 Series is a CMOS dynamic RAM organized 1,048,576-word x 1-bit. HM511000 has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM511000, offers Page Mode as a high speed access mode.

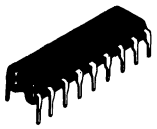
Multiplexed address input permits the HM511000 to be packaged in standard 18-pin plastic DIP, CERDIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM511000 Series



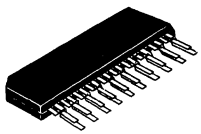
(DG-18A)

HM511000P Series



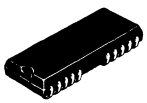
(DP-18C)

HM511000ZP Series



(ZP-20)

HM511000JP Series



(CP-20D)

■ FEATURES

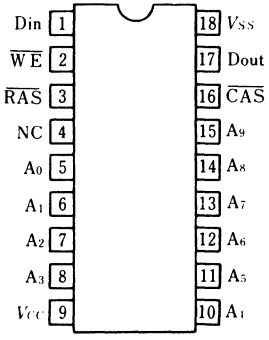
- High Speed: Access Time 100/120ns (max.)
- Low Power: 300mW (active), 10mW (standby)
- High speed page mode capability
- 512 refresh cycles . . . (8ms)
- 3 variations of refresh: $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511000-10 HM511000-12	100ns 120ns	300 mil 18 pin CERDIP
HM511000P-10 HM511000P-12	100ns 120ns	300 mil 18 pin Plastic DIP
HM511000ZP-10 HM511000ZP-12	100ns 120ns	20 pin Plastic ZIP
HM511000JP-10 HM511000JP-12	100ns 120ns	20 pin Plastic SOJ

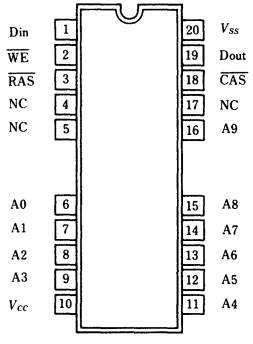
■ PIN ARRANGEMENT

- HM511000, HM511000P Series



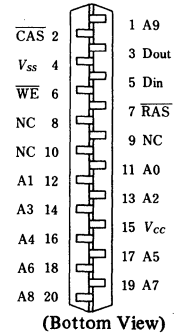
(Top View)

- HM511000JP Series



(Top View)

- HM511000ZP Series



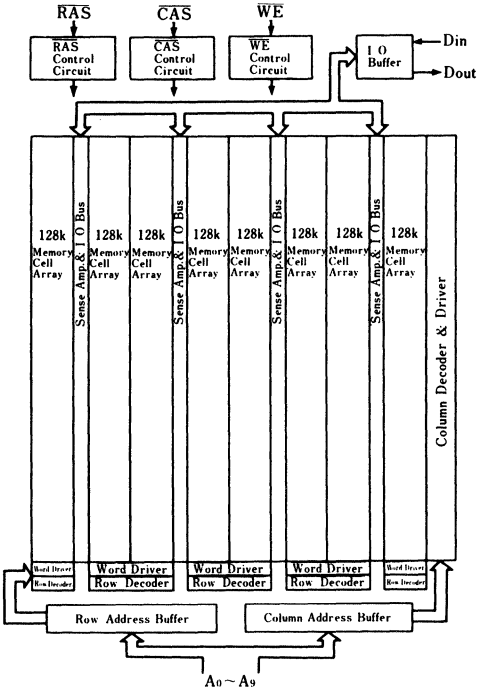
(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, T_a (Ambient) . . . . . 0 to +70°C
Storage temperature (Plastic) . . . . . −55 to +125°C
Storage temperature (Cerdip) . . . . . −65 to +150°C
Power dissipation 1W
Short circuit output current 50mA

$A_0 - A_9$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_8$	Refresh Address Inputs

■ BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	–	6.5	V	1
Input Low voltage	V_{IL}	−2.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Parameter	Symbol	Test Condition		HM511000-10 min.	HM511000-10 max.	HM511000-12 min.	HM511000-12 max.	Unit	Note
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = min.		–	60	–	50	mA	1
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	TTL interface	–	2	–	2	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC}-0.2V, Dout = High-Z	CMOS interface	–	1	–	1		
Refresh Current	I_{CC3}	$\overline{RAS}$ only Refresh, t_{RC} = min.		–	50	–	40	mA	
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout Enable		–	5	–	5	mA	1
Refresh Current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC} = min.		–	50	–	40	mA	
Page Mode Supply Current	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = min.		–	50	–	45	mA	
Input Leakage	I_{LI}	V_{in} = 0 to +7V		-10	10	-10	10	μA	
Output Leakage	I_{LO}	V_{out} = 0 to +7V, Dout is disabled		-10	10	-10	10	μA	1
Output Levels	V_{OH}	I_{out} = -5 mA		2.4	V_{CC}	2.4	V_{CC}	V	
	V_{OL}	I_{out} = 4.2 mA		0	0.4	0	0.4	V	

Note) *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (V_{CC}=5V ±10%, T_a=25°C)

Parameter		Symbol	typ.	max.	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1, 2
Output Capacitance	Data-out	C_o	–	7		

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (V_{CC}=5V ±10%, V_{SS}=0V, T_a=0 to +70°C)[1),10)]

Parameter	Symbol	HM511000-10 min.	HM511000-10 max.	HM511000-12 min.	HM511000-12 max.	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	–	25	–	30	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	ns	

(to be continued)

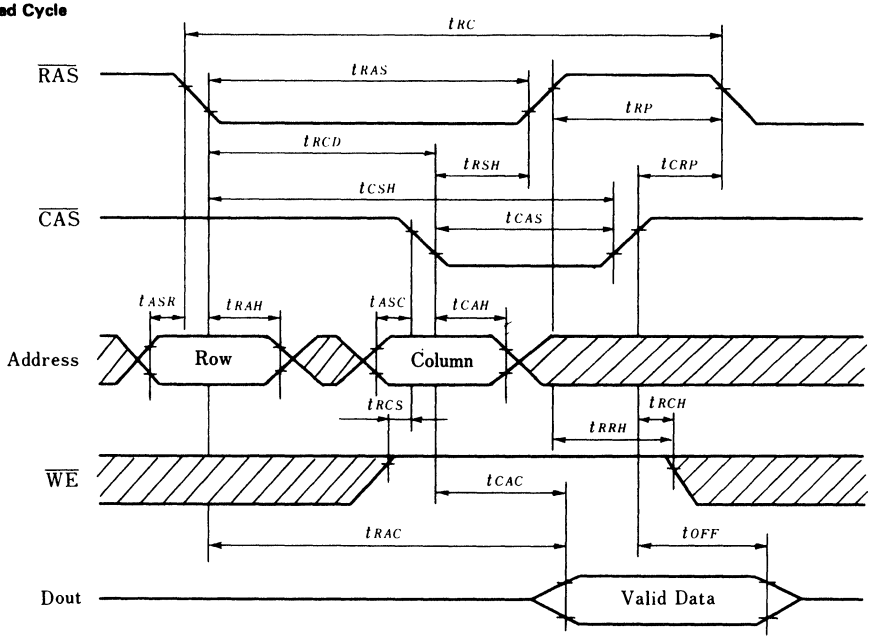
Parameter	Symbol	HM511000-10		HM511000-12		Unit	Note
		min.	max.	min.	max.		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	ns	
Data-in-Setup Time	t_{DS}	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	ns	9
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	
Refresh Period	t_{REF}	–	8	–	8	ms	
Read-Write Cycle Time	t_{RWC}	220	–	255	–	ns	
Read Modify Write Cycle Time	t_{RWS}	140	–	165	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	90	–	110	–	ns	8
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	–	50	–	ns	8
$\overline{CAS}$ Setup Time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	–	25	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	ns	
Page Mode Read or Write Cycle	t_{PC}	70	–	85	–	ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	10	–	15	–	ns	
Page Mode Read Modify Write Cycle	t_{PCM}	100	–	120	–	ns	
Page Mode $\overline{CAS}$ Pulse Width (Read Modify Write Cycle)	t_{CRW}	80	–	95	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
5. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

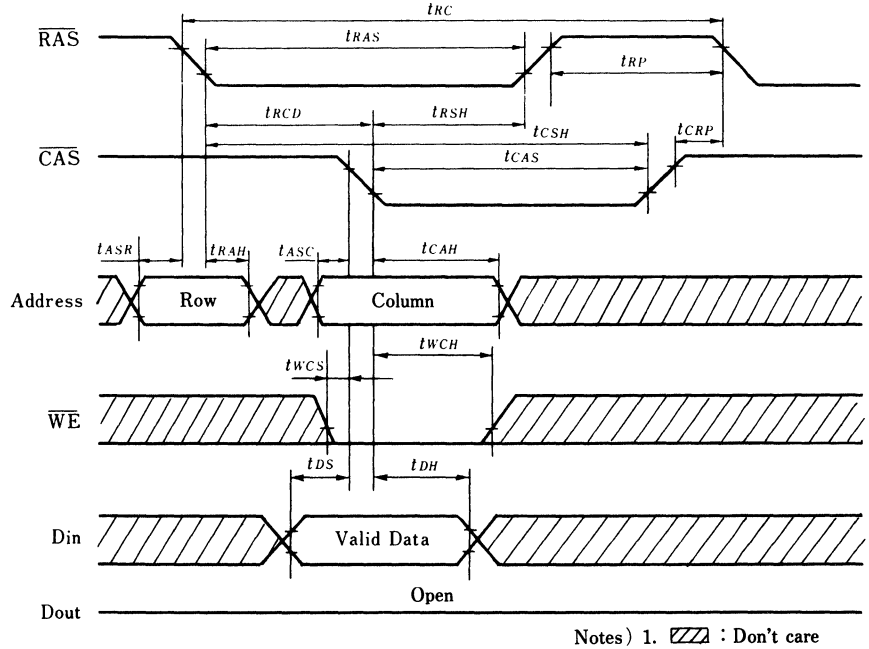
■ TIMING WAVEFORMS

• Read Cycle



Note) ▨ : Don't care

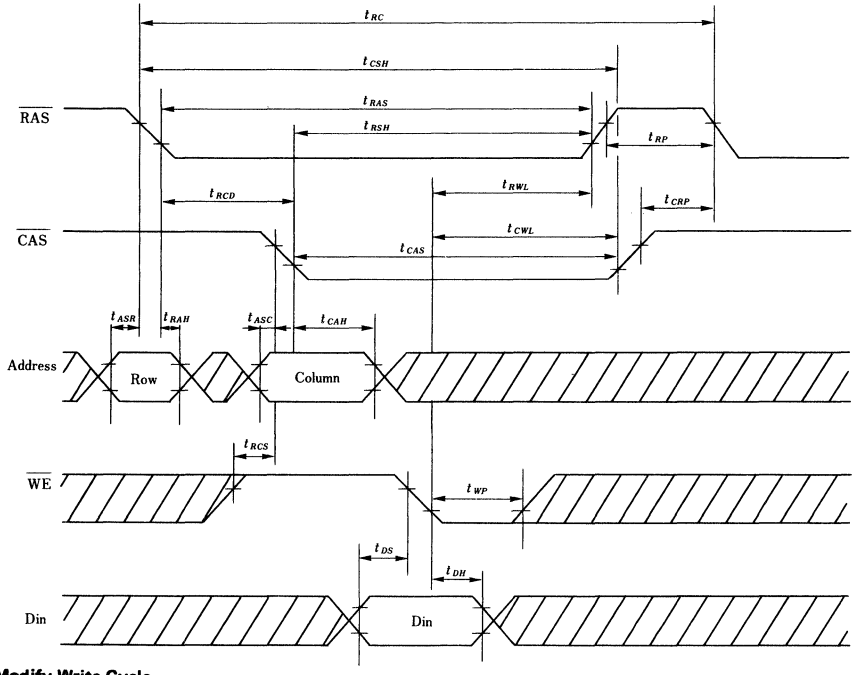
• Early Write Cycle



Notes) 1. ▨ : Don't care

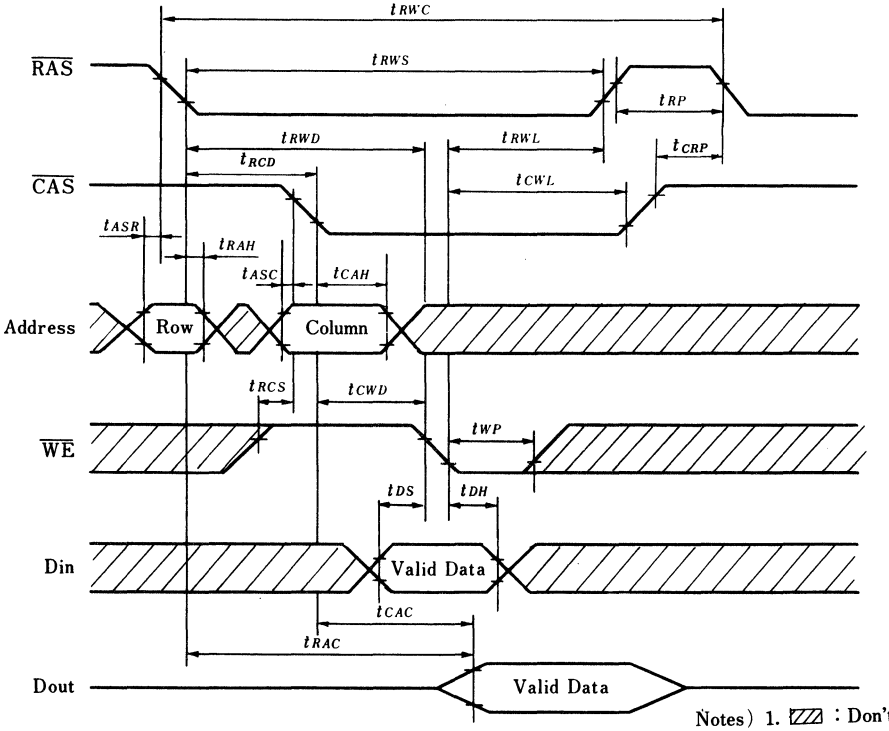
2. $t_{WCS} \geqq t_{WCS}(\min)$

- **Write Cycle (Delayed Write)**



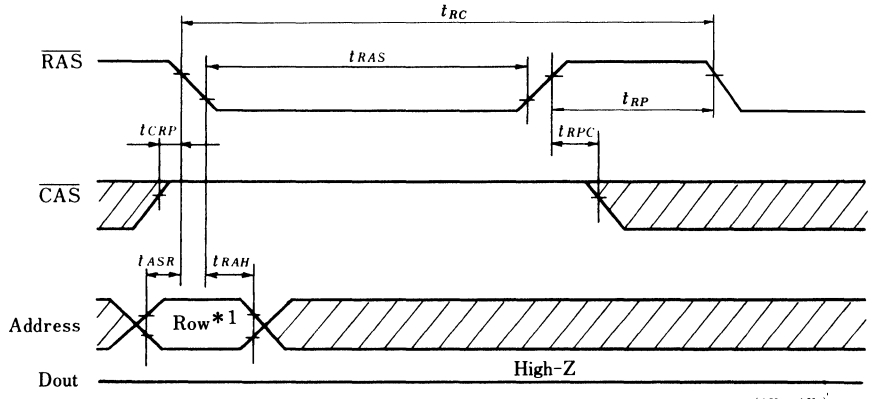
- **Read-Modify-Write Cycle**

Note) ▨ : Don't care



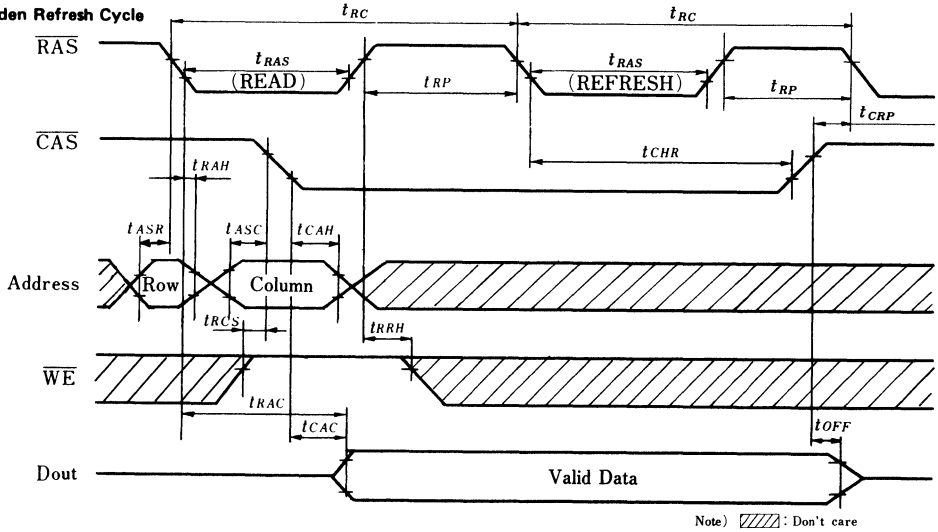
Notes) 1. ▨ : Don't care
2. $t_{RWD} \geqq t_{RWD}$(min)
3. $t_{CWD} \geqq t_{CWD}$(min)

- **$\overline{RAS}$ Only Refresh Cycle**



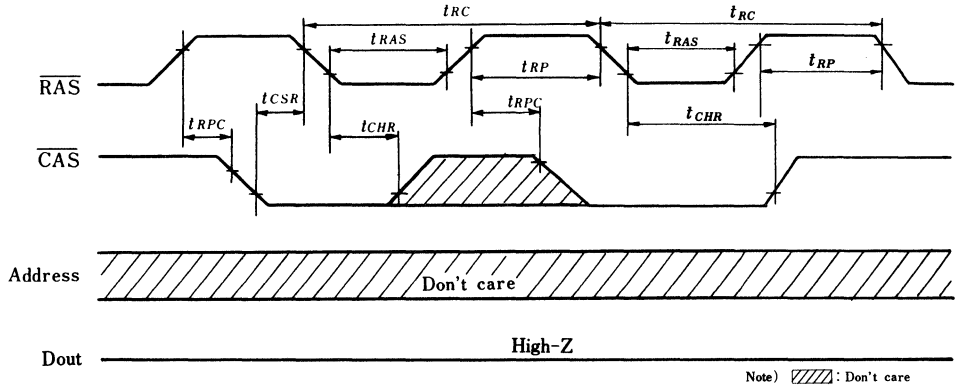
Notes) 1. Refresh Address A_0~A_8 (AX_0~AX_8)
2. ▨: Don't care

- **Hidden Refresh Cycle**



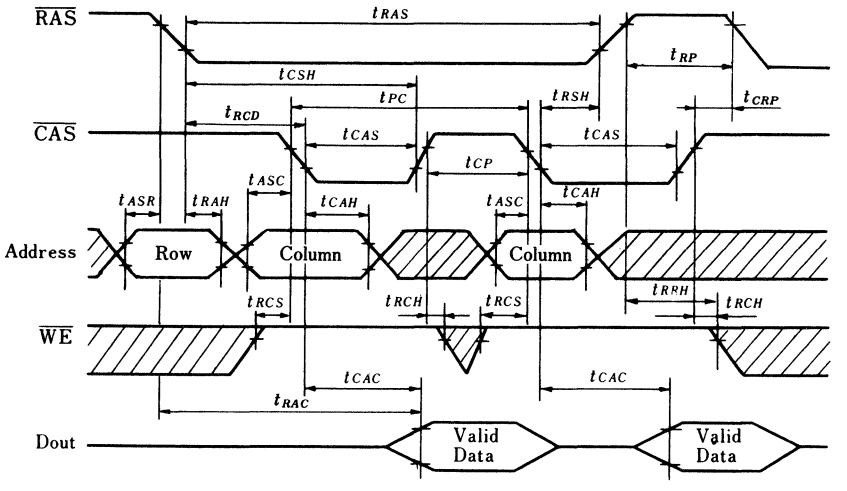
Note) ▨: Don't care

- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



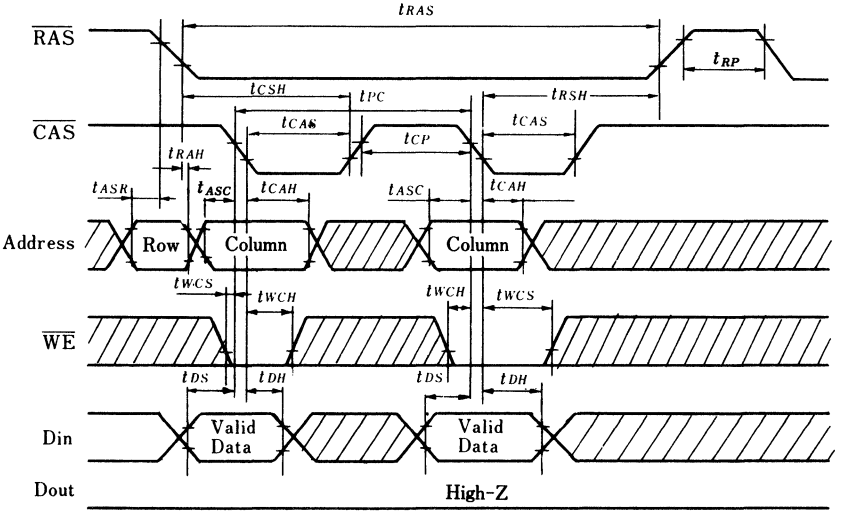
Note) ▨: Don't care

- **Page Mode Read Cycle**



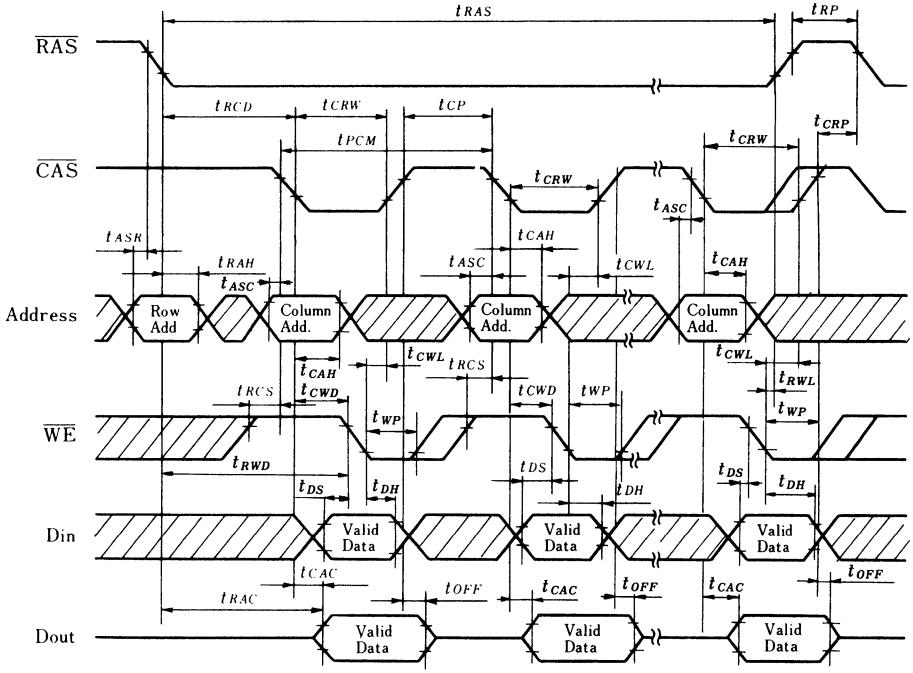
Note) ▨ : Don't care

- **Page Mode Write Cycle**



Note) ▨ : Don't care

- **Page Mode Read Modify Write Cycle**



Note) ▨ : Don't care

HM511000S Series — Preliminary

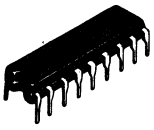
1048576-word x 1-bit CMOS Dynamic Random Access Memory

The Hitachi HM511000S series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511000S has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511000S offers Page Mode as a high speed access mode.

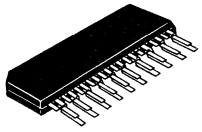
Multiplexed address input permits the HM511000S to be packaged in standard 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511000SP Series



(DP-18C)

HM511000SZP Series



(ZP-20)

HM511000SJP Series

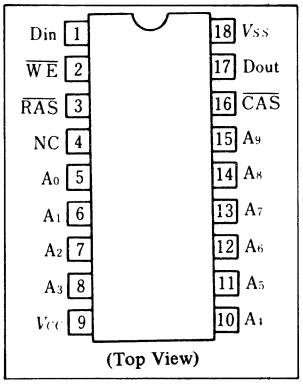
(CP-20D)

Features

- High speed; Access time 80/100/120 ns (max)
- Low power; 11 mW standby, 385/330/275 mW active
- Single 5V supply (±10%)
- Fast page mode capability
- 512 refresh cycle; (8 ms)
- 3 variations of refresh; $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh

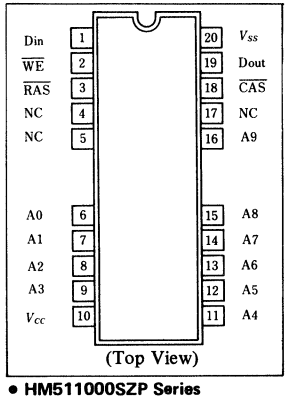
Pin Arrangement

• **HM511000SP Series**



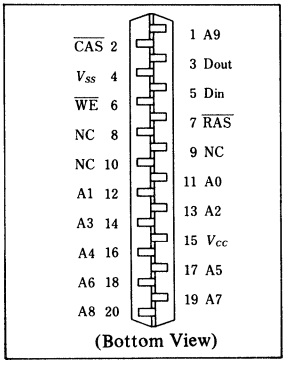
(Top View)

• **HM511000SJP Series**



(Top View)

• **HM511000SZP Series**



(Bottom View)

Pin Description

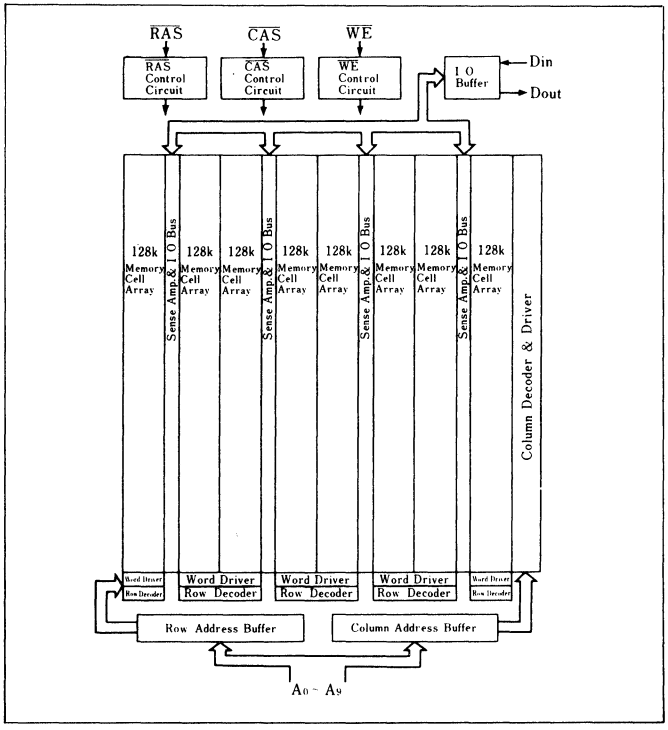
Symbol	Function
A0 - A9	Address inputs
$\overline{CAS}$	Column address strobe
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/Write input
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 - A8	Refresh address input

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Ordering Information

Type No.	Access Time	Package
HM511000P-8S	80ns	300 mil 18 pin Plastic DIP
HM511000P-10S	100ns	
HM511000P-12S	120ns	
HM511000ZP-8S	80ns	20 pin Plastic ZIP
HM511000ZP-10S	100ns	
HM511000ZP-12S	120ns	
HM511000JP-8S	80ns	20 pin Plastic SOJ
HM511000JP-10S	100ns	
HM511000JP-12S	120ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-1 to +7	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Test condition	Note
		min	max	min	max	min	max			
Operating current	I_{CC1}	–	70	–	60	–	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min	*1,*2
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2V Dout = High-Z CMOS interface	
Refresh current	I_{CC3}	–	60	–	50	–	45	mA	$\overline{RAS}$ only refresh, t_{RC} = Min	*2
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout enable	*1
Refresh current	I_{CC6}	–	70	–	60	–	50	mA	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = Min.	
Fast page mode current	I_{CC7}	–	50	–	50	–	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min	*1,*3
Input leakage	I_{LI}	–10	10	–10	10	–10	10	μA	V_{IN} = 0 to +7V	
Output leakage	I_{LO}	–10	10	–10	10	–10	10	μA	V_{OUT} = 0 to +7V, Dout is disabled	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = –5mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2mA	

Notes) *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data-in	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data-out	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

Electrical Characteristics and Recommended AC Operating Conditions ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Note
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	12	–	15	–	15	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	*8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	*9
$\overline{RAS}$ Hold Time	t_{RSH}	25	–	25	–	30	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	*7
Refresh Period	t_{REF}	–	8	–	8	–	8	ms	

Read Cycle

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Note
		min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	*2,*3
Access Time from $\overline{CAS}$	t_{CAC}	–	25	–	25	–	30	ns	*3,*4
Access Time from Address	t_{AA}	–	40	–	45	–	55	ns	*3,*5
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	ns	
Output Buffer Turn-off Time	t_{OFF}	–	20	–	25	–	30	ns	*6

Write Cycle

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Note
		min	max	min	max	min	max		
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	*10
Write Command Hold Time	t_{WCH}	20	–	20	–	25	–	ns	
Write Command Pulse Width	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	–	25	–	30	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	–	25	–	30	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	*11
Data-in Hold Time	t_{DH}	20	–	20	–	25	–	ns	*11

Read-Modify-Write Cycle

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Note
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	190	–	220	–	255	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	–	100	–	120	–	ns	*10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	–	25	–	30	–	ns	*10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	ns	*10

Refresh Cycle

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Note
		min	max	min	max	min	max		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	

High Speed Page Mode Cycle

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Note
		min	max	min	max	min	max		
High Speed Page Mode Cycle Time	t_{PC}	55	–	55	–	65	–	ns	*14
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	15	–	ns	
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	–	100000	–	100000	–	100000	ns	*13
Access Time from $\overline{CAS}$ precharge	t_{ACP}	–	50	–	50	–	60	ns	*14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	–	50	–	60	–	ns	

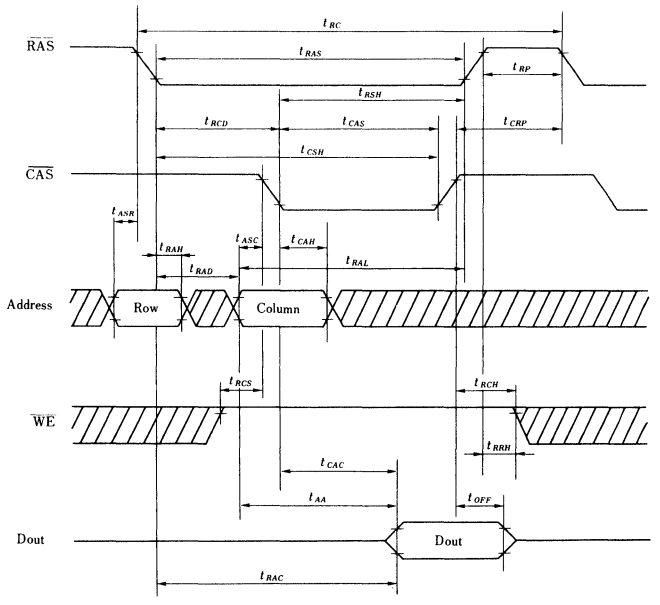
High Speed Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511000-8S		HM511000-10S		HM511000-12S		Unit	Note
		min	max	min	max	min	max		
High Speed Page Mode Read-Write Cycle Time	t_{PCM}	85	–	85	–	100	–	ns	

Notes) *1. AC measurements assume t_T = 5ns.
*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
*5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
*6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
*7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
*9. Operation with the t_{RAC} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
*12. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
*13. t_{RASC} defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
*14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.

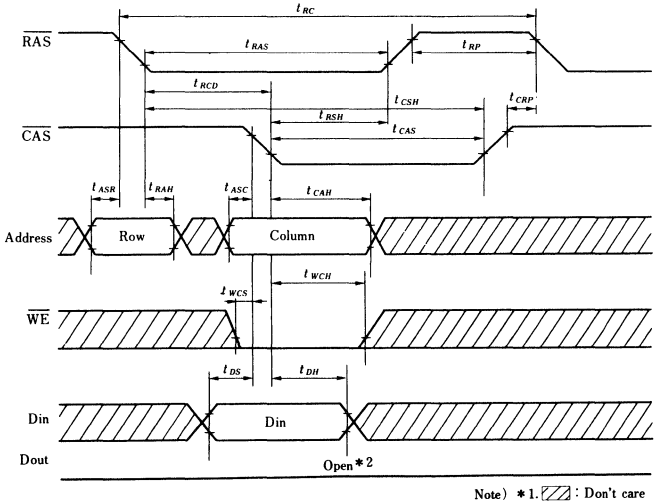
Timing Waveforms

Read Cycle



Note) ▨ : Don't care

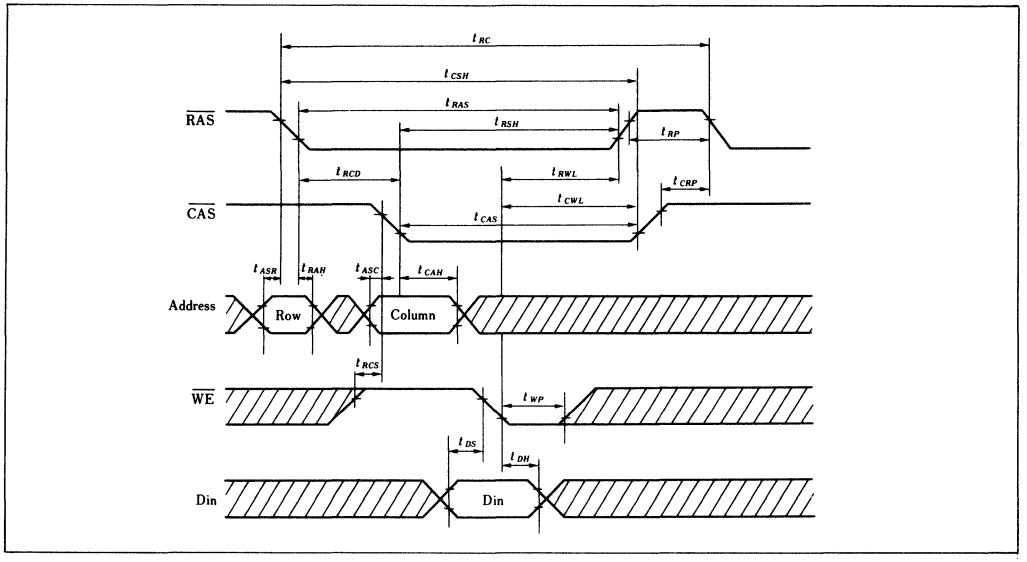
Early Write Cycle



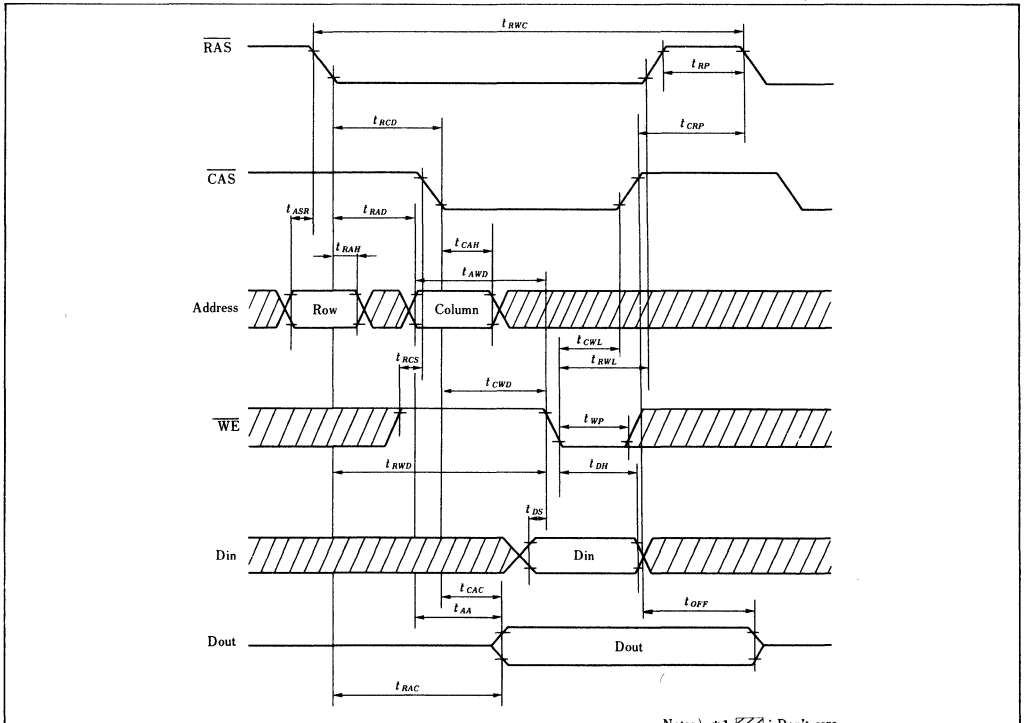
Note) *1. ▨ : Don't care

*2. $t_{WCS} \geqq t_{WCS}$(min)

Delayed Write Cycle

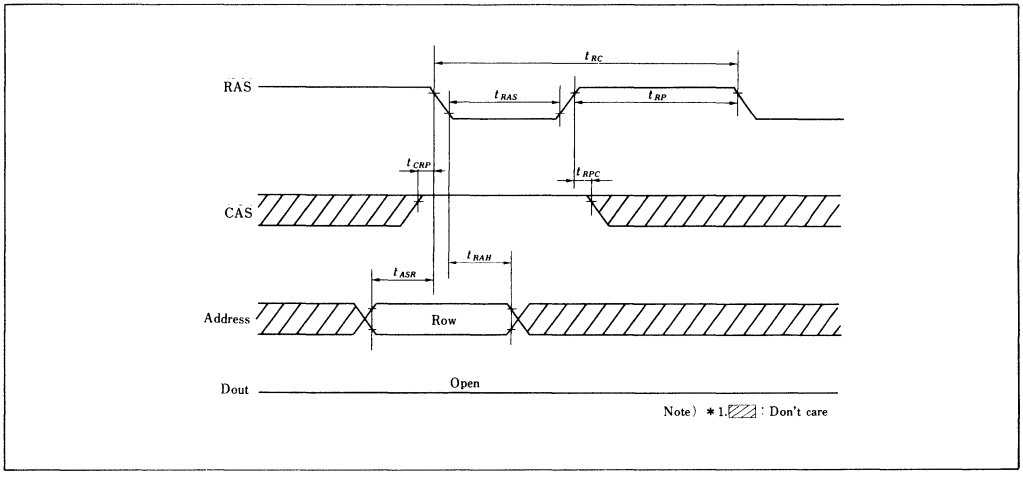


Read-Modify-Write Cycle

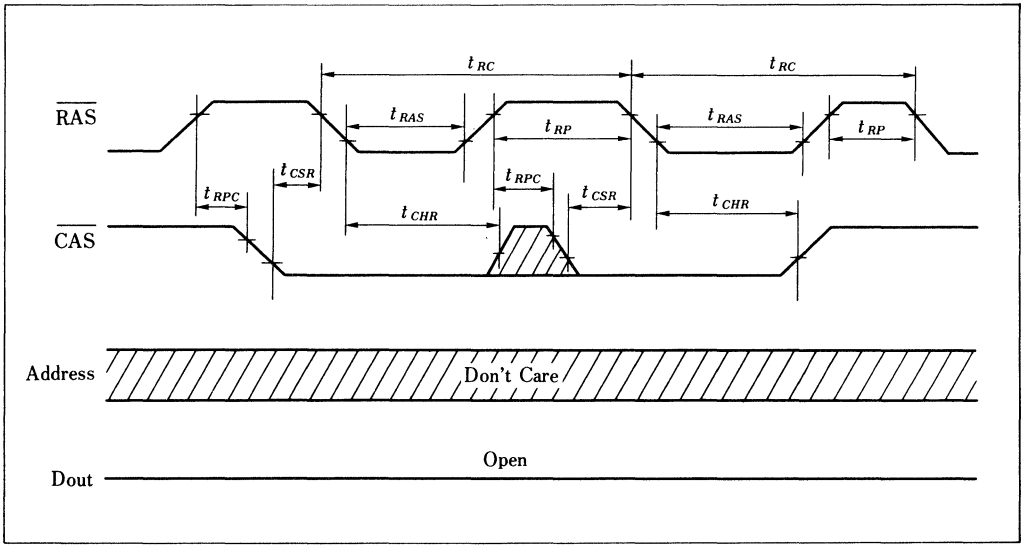


Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)
$t_{AWD} \geqq t_{AWD}$(min)

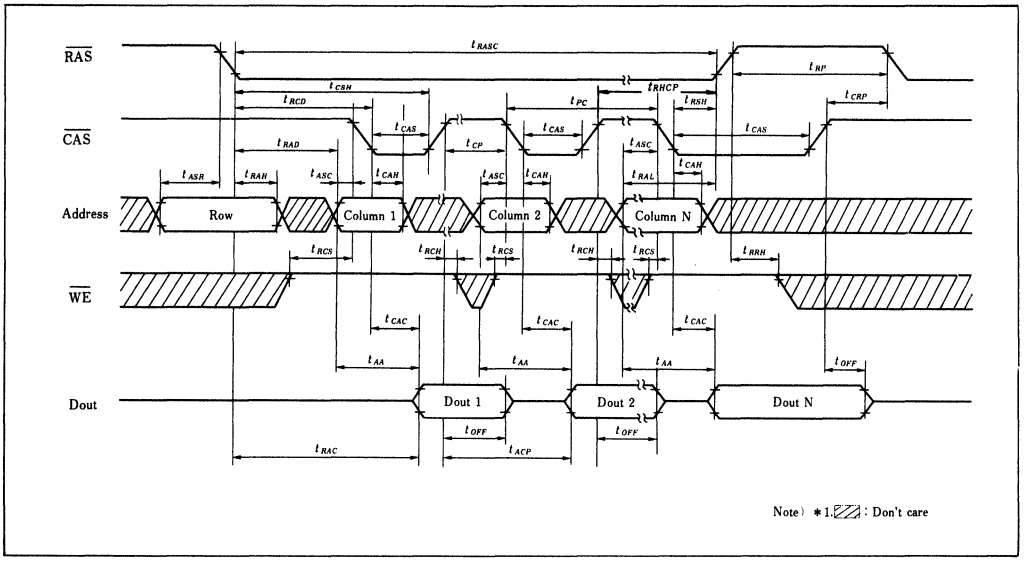
$\overline{RAS}$ Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

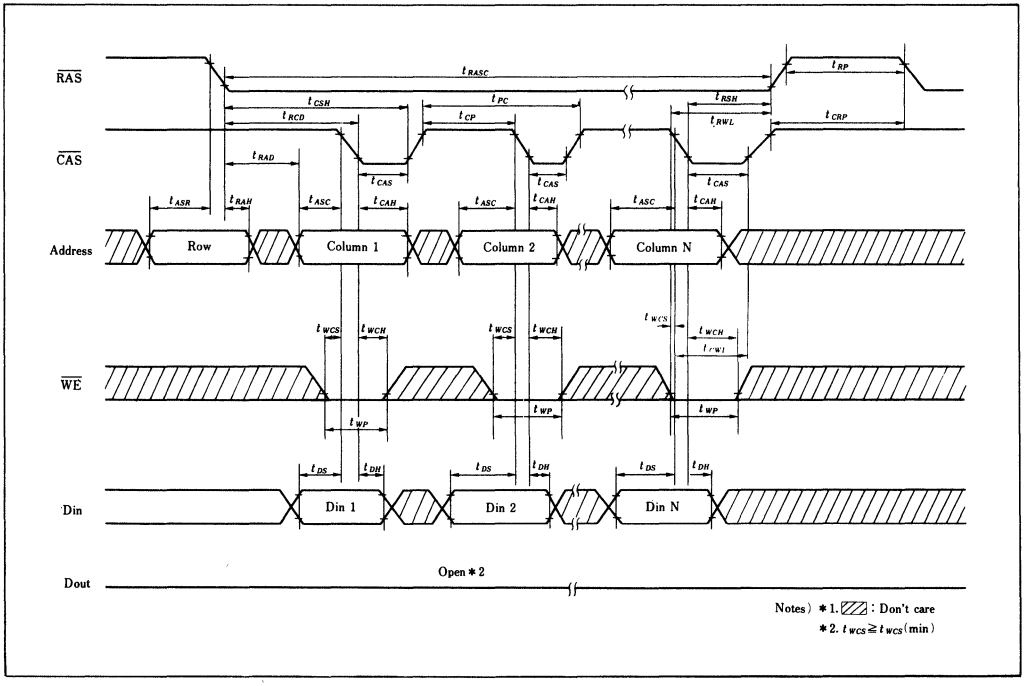


High Speed Page Mode Read Cycle



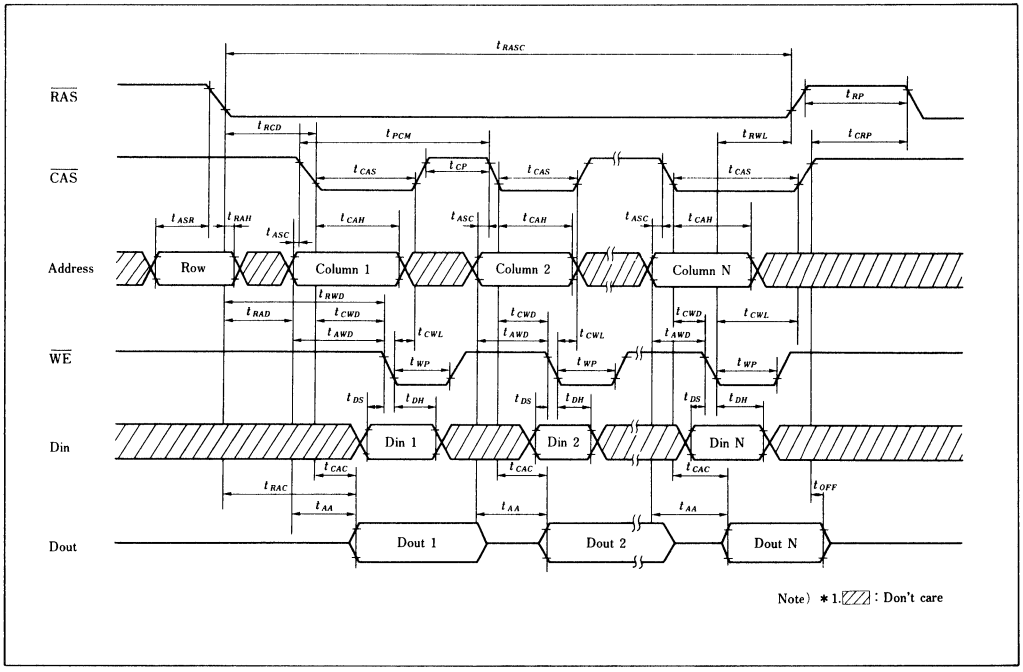
Note) *1. ▨ : Don't care

High Speed Page Mode Write Cycle



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$(min)

High Speed Page Mode Read Modify Write Cycle



Note) ∗1. ▨ : Don't care

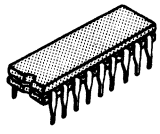
HM511001 Series

1048576-word x 1-bit CMOS Dynamic Random Access Memory

The Hitachi HM511001 Series is a CMOS dynamic RAM organized 1,048,576-word x 1-bit. HM511001 has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM511001, offers Nibble Mode as a high speed access mode.

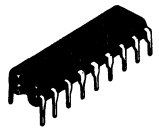
Multiplexed address input permits the HM511001 to be packaged in standard 18-pin plastic DIP, CERDIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM511001 Series



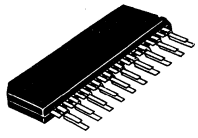
(DG-18A)

HM511001P Series



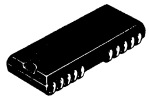
(DP-18C)

HM511001ZP Series



(ZP-20)

HM511001JP Series



(CP-20D)

■ FEATURES

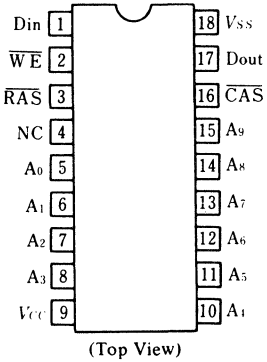
- High Speed: Access Time 100/120ns (max.)
- Low Power: 300mW (active), 10mW (standby)
- Nibble mode capability
- 512 refresh cycles . . . (8ms)
- 3 variations of refresh: $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM511001-10 HM511001-12	100ns 120ns	300 mil 18 pin CERDIP
HM511001P-10 HM511001P-12	100ns 120ns	300 mil 18 pin Plastic DIP
HM511001ZP-10 HM511001ZP-12	100ns 120ns	20 pin plastic ZIP
HM511001JP-10 HM511001JP-12	100ns 120ns	20 pin Plastic SOJ

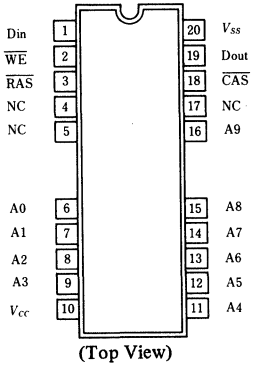
■ PIN ARRANGEMENT

- HM511001 Series,
  HM511001P Series



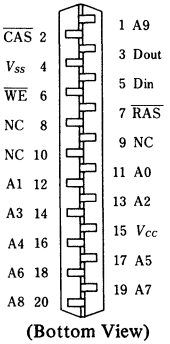
(Top View)

- HM511001JP Series



(Top View)

- HM511001ZP Series



(Bottom View)

HITACHI

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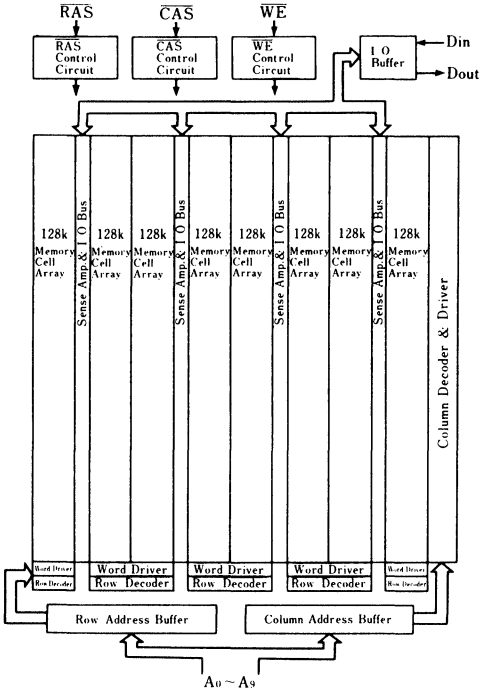
■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, T_a (Ambient) . . . . . 0 to +70°C
Storage Temperature (Plastic) . . . . . −55 to +125°C
Storage Temperature (Cerdip) . . . . . −65 to +150°C
Power dissipation 1W
Short circuit output current 50mA

$A_0 - A_9$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_8$	Refresh Address Inputs

■ BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	–	6.5	V	1
Input Low voltage	V_{IL}	−2.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	Test Condition		HM511001-10 min.	HM511001-10 max.	HM511001-12 min.	HM511001-12 max.	Unit	Note
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = min.		–	60	–	50	mA	1
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	TTL interface	–	2	–	2	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC}-0.2V, Dout = High-Z	CMOS interface	–	1	–	1		
Refresh Current	I_{CC3}	$\overline{RAS}$ only Refresh, t_{RC} = min.		–	50	–	40	mA	
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout Enable		–	5	–	5	mA	1
Refresh Current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC} = min.		–	50	–	40	mA	
Nibble Mode Supply Current	I_{CC8}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{NC} = min.		–	50	–	45	mA	
Input Leakage	I_{LI}	V_{in} = 0 to +7V		-10	10	-10	10	μA	
Output Leakage	I_{LO}	V_{out} = 0 to +7V, Dout is disabled		-10	10	-10	10	μA	
Output Levels	V_{OH}	I_{out} = -5 mA		2.4	V_{CC}	2.4	V_{CC}	V	
	V_{OL}	I_{out} = 4.2 mA		0	0.4	0	0.4	V	

Note) *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (V_{CC} = 5V ±10%, T_a = 25°C)

Parameter		Symbol	typ.	max.	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1, 2
Output Capacitance	Data-out	C_o	–	7		

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (V_{CC}=5V ±10%, V_{SS} = 0V, T_a = 0 to +70°C)[1),10)]

Parameter	Symbol	HM511001-10 min.	HM511001-10 max.	HM511001-12 min.	HM511001-12 max.	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	2, 3
Output Buffer Turn-off Delay	t_{OFF}	–	25	–	30	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	ns	7
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	ns	

(to be continued)

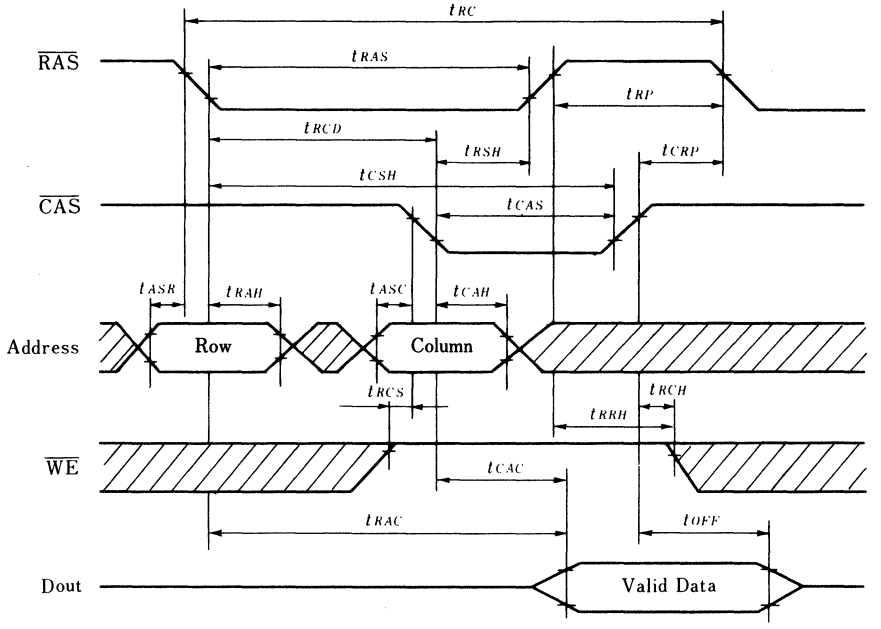
Parameter	Symbol	HM511001-10		HM511001-12		Unit	Note
		min.	max.	min.	max.		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	ns	
Data-in-Setup Time	t_{DS}	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	ns	9
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	
Refresh Period	t_{REF}	–	8	–	8	ms	
Read-Write Cycle Time	t_{RWC}	220	–	255	–	ns	
Read Modify Write Cycle Time	t_{RWS}	140	–	165	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	90	–	110	–	ns	8
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	–	50	–	ns	8
$\overline{CAS}$ Setup Time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	–	25	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	ns	
Nibble Mode Access Time	t_{NAC}	–	30	–	35	ns	
Nibble Mode Cycle Time	t_{NC}	50	–	55	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	–	10	–	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	30	–	35	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	40	–	50	–	ns	
Nibble Mode Read Modify Write Cycle Time	t_{NRWC}	65	–	75	–	ns	
Nibble Mode Write Command $\overline{CAS}$ Read Time	t_{WCWL}	20	–	25	–	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{NCWD}	20	–	25	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
5. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

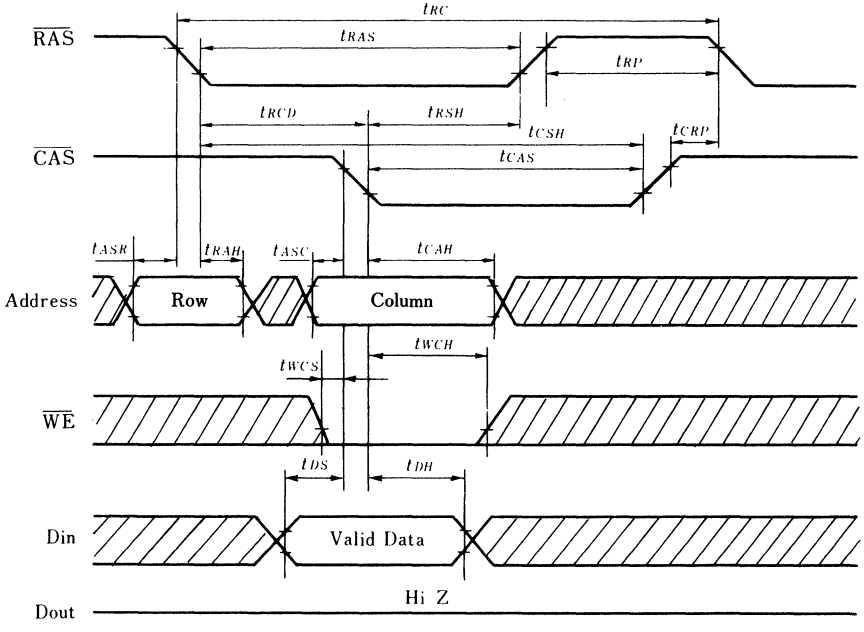
■ TIMING WAVEFORMS

• Read Cycle



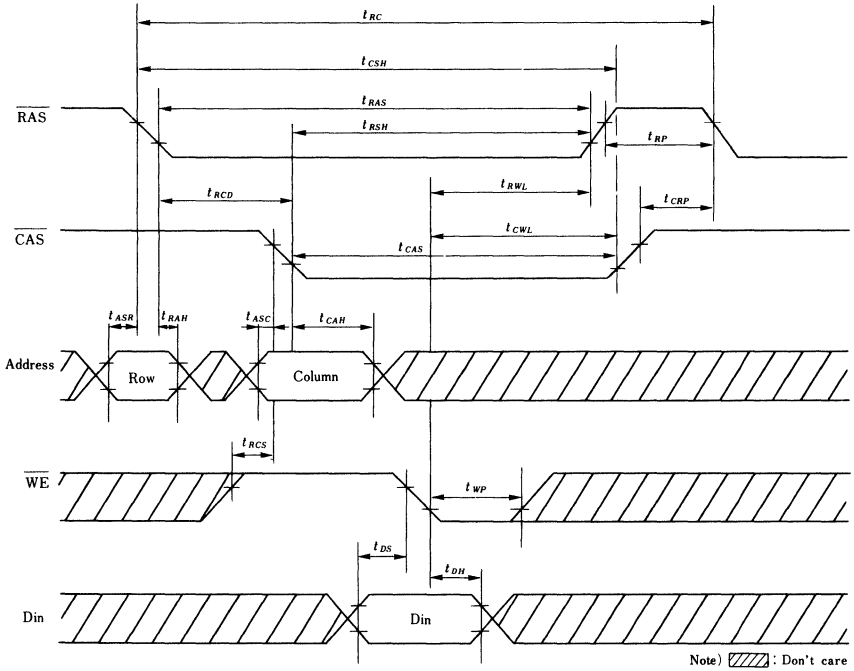
Note) ▨: Don't care

• Early Write Cycle

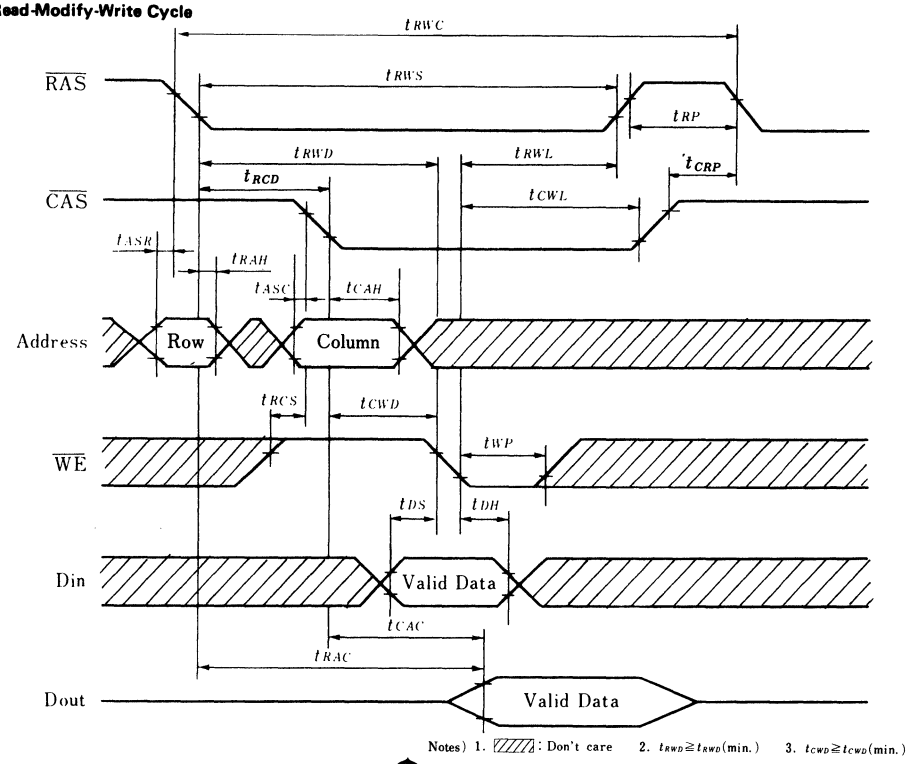


Notes) 1. ▨: Don't care
2. $t_{WCS} \geq t_{WCS}$(min.)

- Delayed Write Cycle

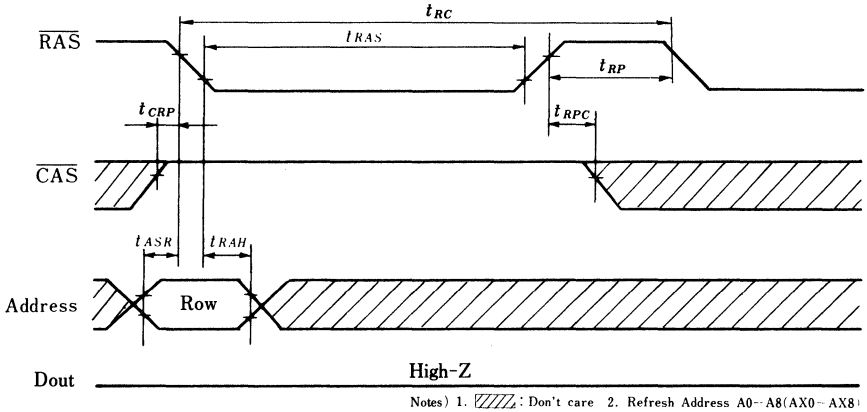


- **Read-Modify-Write Cycle**



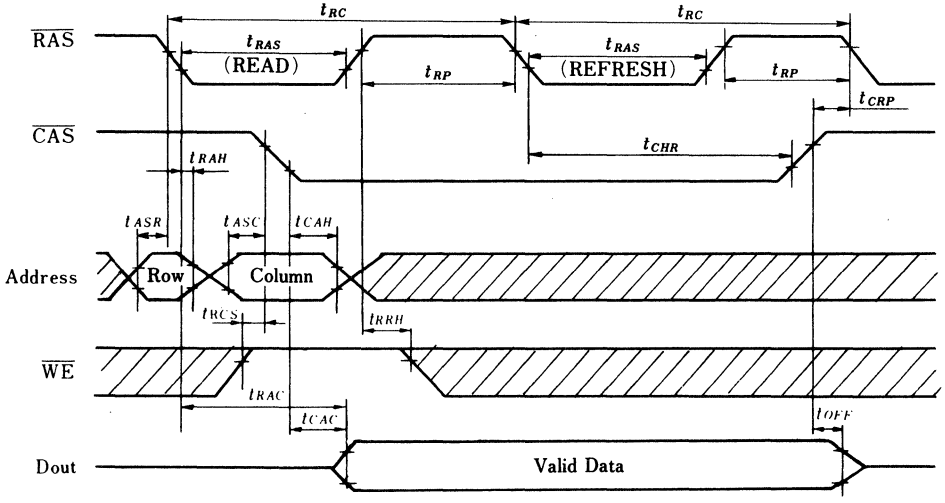
Notes) 1. ▨: Don't care 2. $t_{RWD} \geqq t_{RWD}$(min.) 3. $t_{CWD} \geqq t_{CWD}$(min.)

- **$\overline{RAS}$ Only Refresh Cycle**



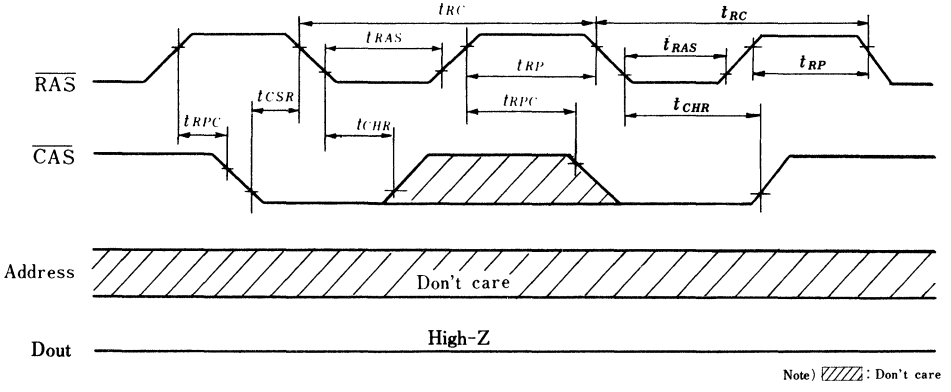
Notes) 1. ▨: Don't care 2. Refresh Address A0–A8(AX0–AX8)

- **Hidden Refresh Cycle**



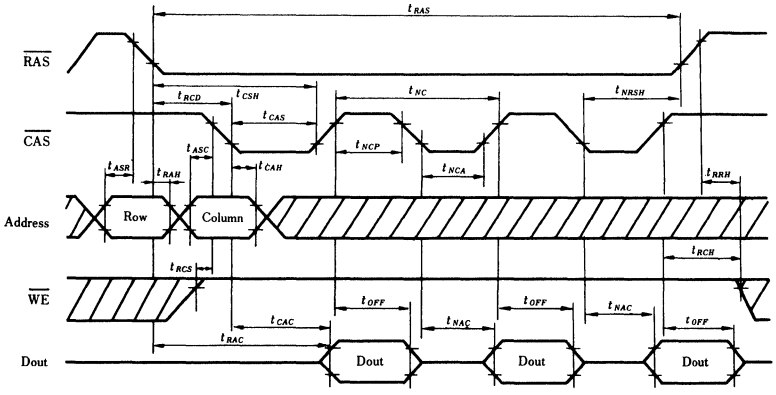
Note) ▨: Don't care

- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



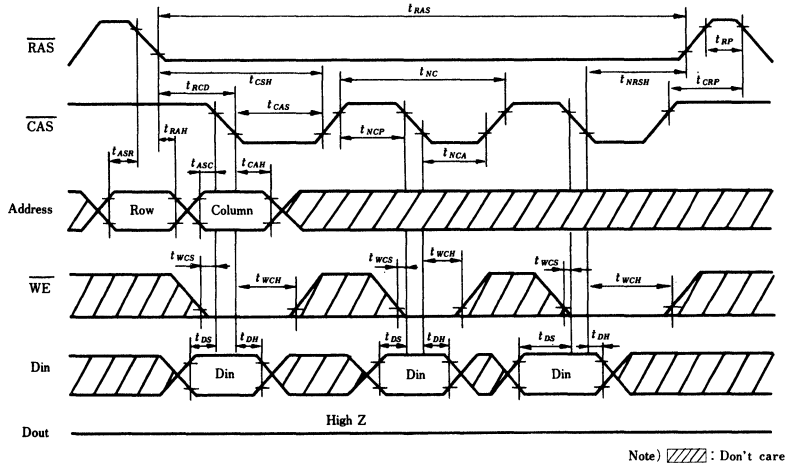
Note) ▨: Don't care

- **Nibble Mode Read Cycle**



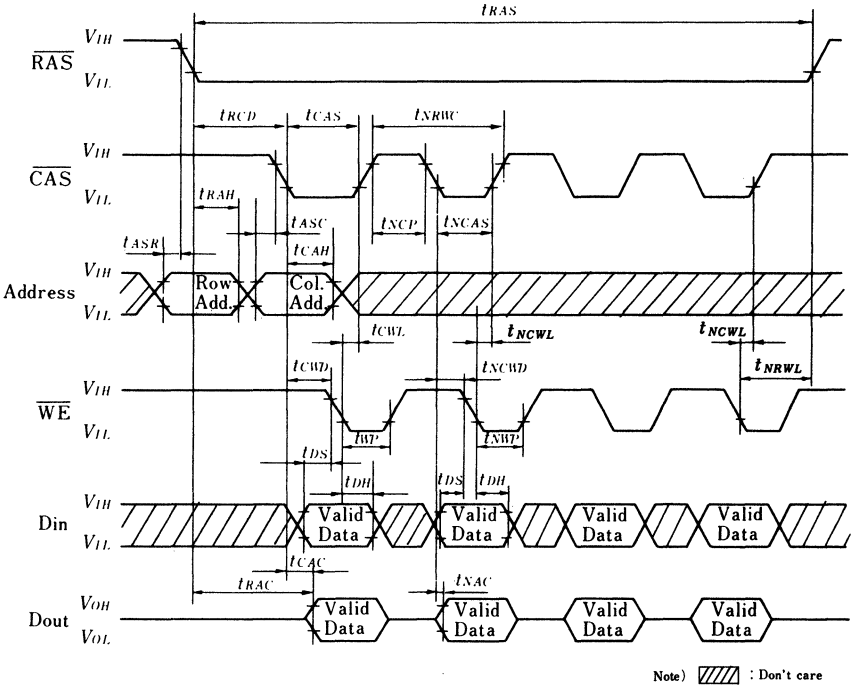
Note) ▨: Don't care

- **Nibble Mode Write Cycle**



Note) ▨: Don't care

- **Nibble Mode Read Modify Write Cycle**



HM511001S Series — Preliminary

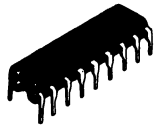
1048576-word x 1-bit CMOS Dynamic Random Access Memory

The Hitachi HM511001S series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511001S has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511001S offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM511001S to be packaged in standard, 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511001SP Series

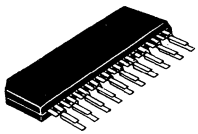


(DP-18C)

HM511001SJP Series

(CP-20D)

HM511001SZP Series



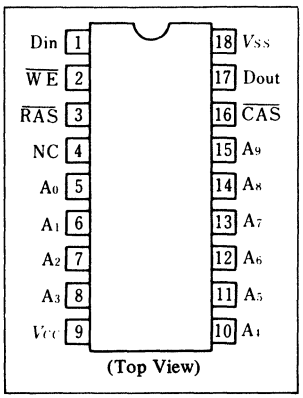
(ZP-20)

Features

- High speed; Access time 80/100/120 ns (max)
- Low power; 11 mW standby, 385/330/275 mW active
- Single 5V supply (±10%)
- Fast nibble mode capability
- 512 refresh cycle; (8 ms)
- 2 variations of refresh; $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh

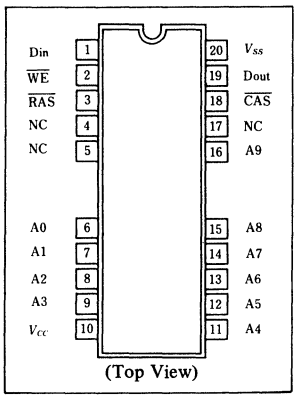
Pin Arrangement

• **HM511001SP Series**



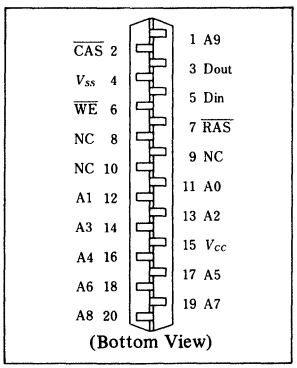
(Top View)

• **HM511001SJP Series**



(Top View)

• **HM511001SZP Series**



(Bottom View)

Pin Description

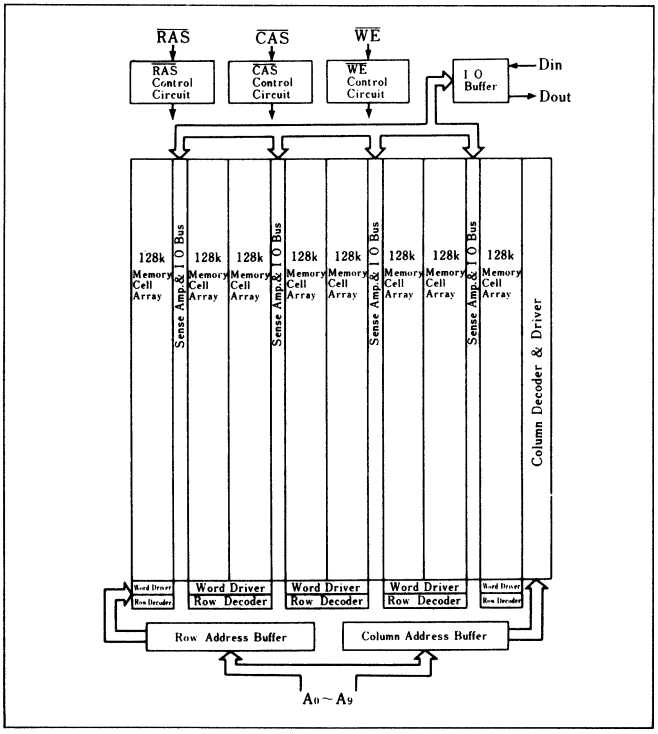
Symbol	Function
A0 - A9	Address inputs
$\overline{CAS}$	Column address strobe
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/Write input
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 - A8	Refresh address input

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sale Dept. regarding specifications.

Ordering Information

Type No.	Access Time	Package
HM511001P-8S	80ns	300 mil 18 pin Plastic DIP
HM511001P-10S	100ns	
HM511001P-12S	120ns	
HM511001ZP-8S	80ns	20 pin Plastic ZIP
HM511001ZP-10S	100ns	
HM511001ZP-12S	120ns	
HM511001JP-8S	80ns	20 pin Plastic SOJ
HM511001JP-10S	100ns	
HM511001JP-12S	120ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1 to +7	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Test condition	Note
		min	max	min	max	min	max			
Operating current	I_{CC1}	–	70	–	60	–	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min	*1,*2
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CAS}$=V_{IH} Dout=High-Z TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$,$\overline{CAS}$≧V_{CC}–0.2V Dout=High-Z CMOS interface	
Refresh current	I_{CC3}	–	60	–	50	–	45	mA	$\overline{RAS}$ only refresh, t_{RC} = Min	*2
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout enable	*1
Refresh current	I_{CC6}	–	70	–	60	–	50	mA	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = Min.	
Nibble mode current	I_{CC8}	–	60	–	50	–	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{NC} = Min	*1,*3
Input leakage	I_{LI}	–10	10	–10	10	–10	10	μA	V_{IN} = 0 to +7V	
Output leakage	I_{LO}	–10	10	–10	10	–10	10	μA	V_{OUT} = 0 to +7V, Dout is disabled	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2mA	

Notes) *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data-in	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data-out	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

Electrical Characteristics and Recommended AC Operating Conditions

(Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)*1,*10

Parameter	Symbol	HM511001-8S		HM511001-10S		HM511001-12S		Unit	Notes
		min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	*2,*3
Access Time from $\overline{CAS}$	t_{CAC}	–	40	–	50	–	60	ns	*3,*4
Output Buffer Turn-off Delay	t_{OFF}	–	20	–	25	–	30	ns	*5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	*6
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	40	10000	50	10000	60	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	40	25	50	25	60	ns	*7
$\overline{RAS}$ Hold Time	t_{RSH}	40	–	50	–	60	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	12	–	15	–	15	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	*8
Write Command Hold Time	t_{WCH}	20	–	20	–	25	–	ns	
Write Command Pulse Width	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	–	25	–	30	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	–	25	–	30	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	*9
Data-in Hold Time	t_{DH}	20	–	20	–	25	–	ns	*8,*9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	8	–	8	–	8	ms	
Read-Write Cycle Time	t_{RWC}	190	–	220	–	255	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	80	–	100	–	120	–	ns	*8
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	–	50	–	60	–	ns	*8
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
Nibble Mode Access Time	t_{NAC}	–	25	–	25	–	30	ns	
Nibble Mode Cycle Time	t_{NC}	45	–	45	–	55	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	–	10	–	15	–	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	25	–	25	–	30	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	25	–	25	–	30	–	ns	
Nibble Mode Read Modify Write Cycle Time	t_{NRWC}	70	–	75	–	85	–	ns	
Nibble Mode Write Command $\overline{CAS}$ Lead Time	t_{NCWL}	20	–	25	–	25	–	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay	t_{NCWD}	30	–	30	–	30	–	ns	

Notes)

*1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}(max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}(max)$.

*5. $t_{OFF}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*6. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

*7. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.

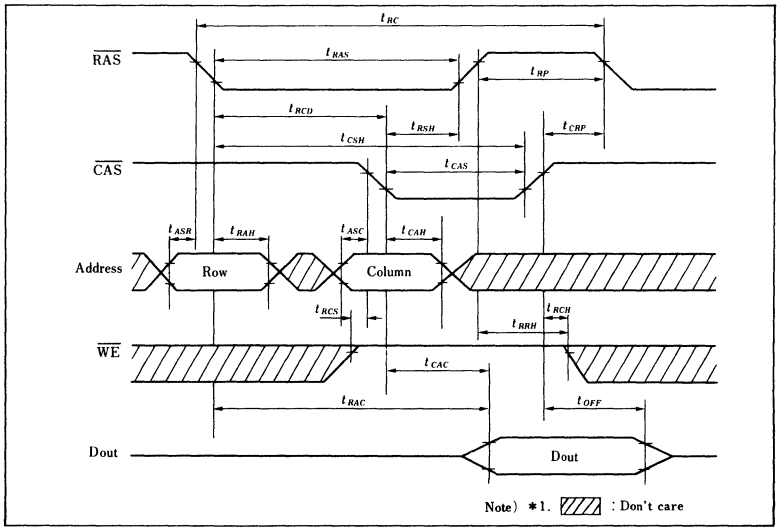
*8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}(min)$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

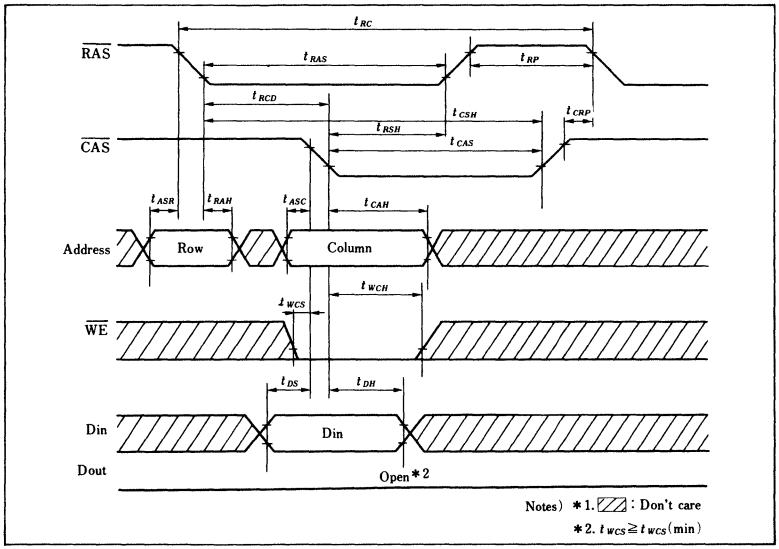
*10. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

Timing Waveforms

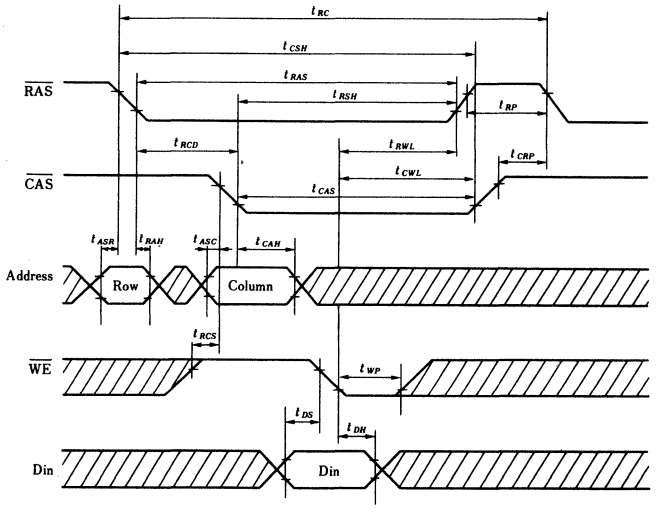
Read Cycle



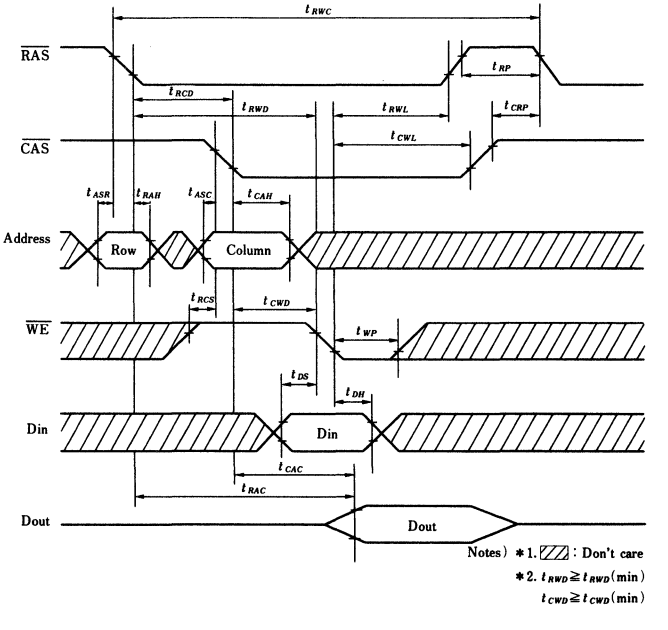
Early Write Cycle



Delayed Write Cycle

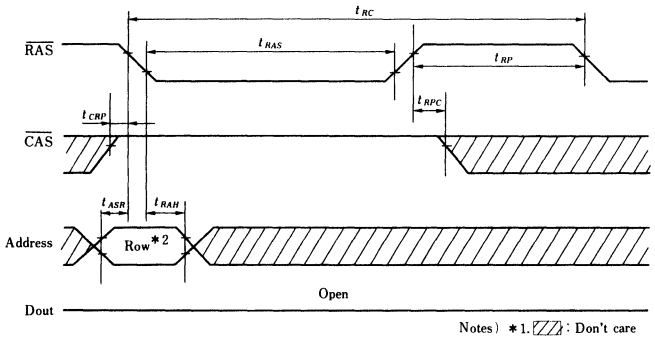


Read-Modify-Write Cycle

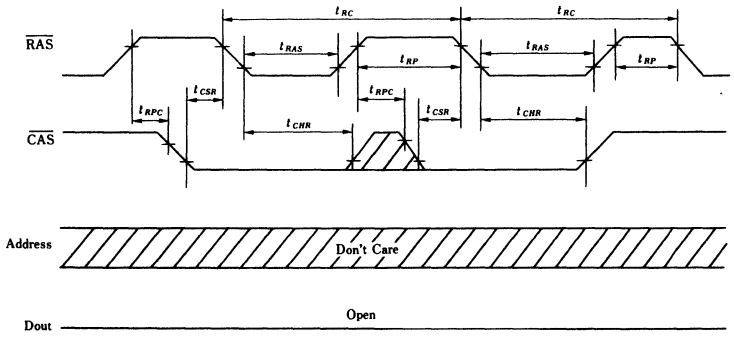


Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geqq t_{RWD}$(min)
$t_{CWD} \geqq t_{CWD}$(min)

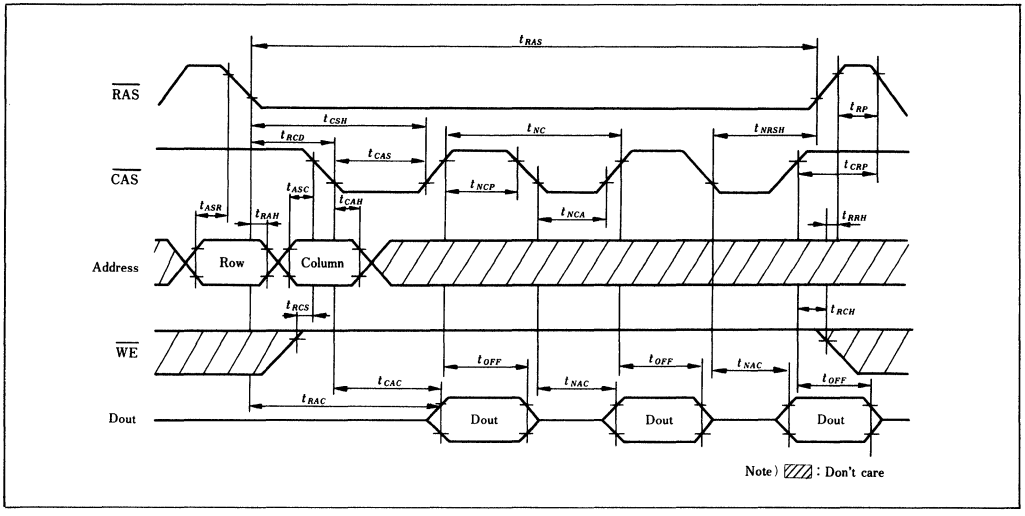
$\overline{RAS}$ Only Refresh Cycle



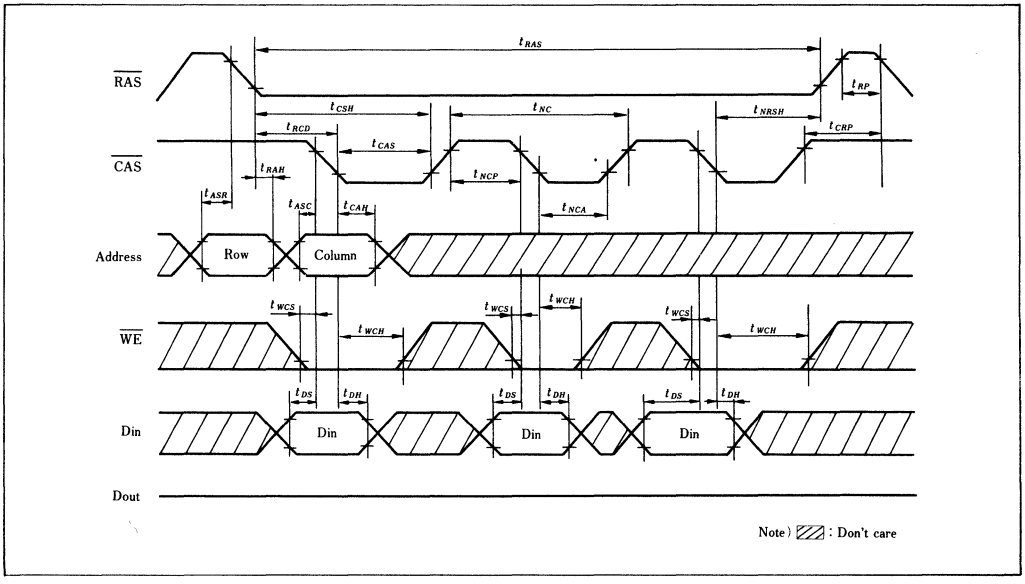
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



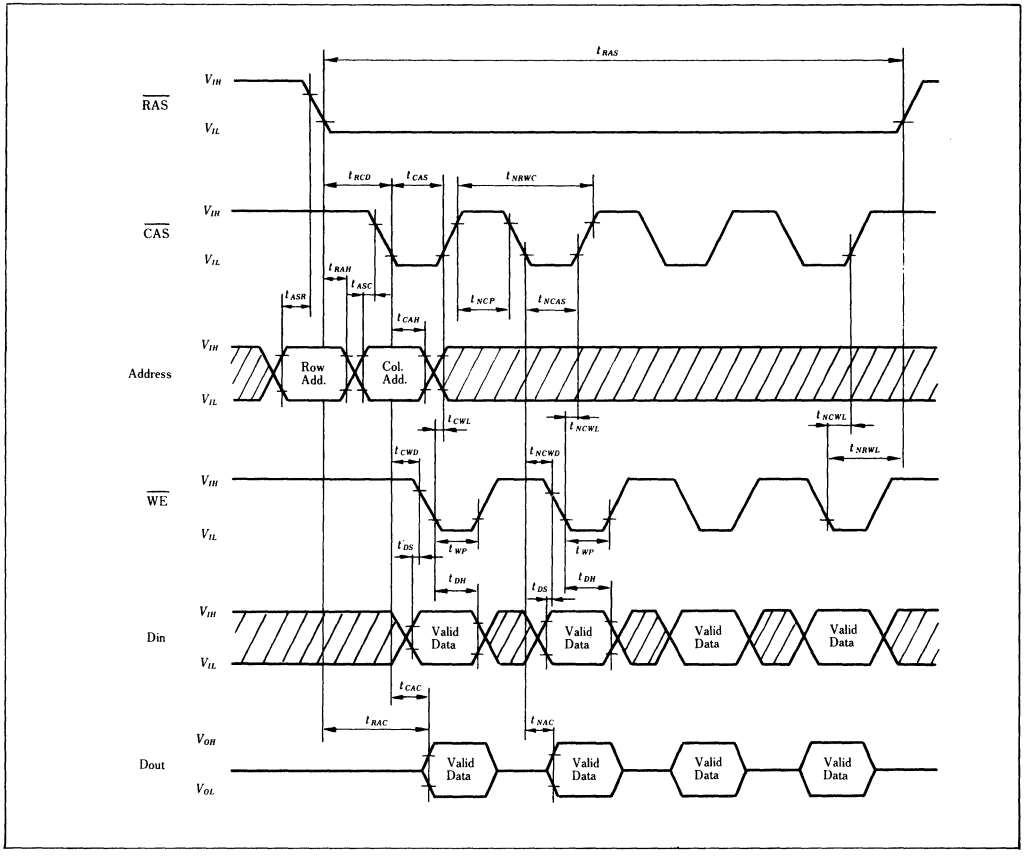
Nibble Mode Read Cycle



Nibble Mode Write Cycle



Nibble Mode Read Modify Write Cycle



HM511002S Series — Preliminary

1048576-word x 1-bit CMOS Dynamic Random Access Memory

The Hitachi HM511002S Series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511002S has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM511002S offers Static Column Mode as a high speed access mode.

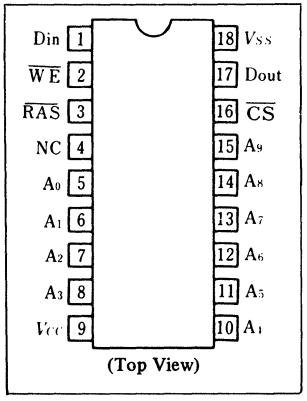
Multiplexed address input permits the HM511002S to be packaged in standard 18-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

Features

- High speed; Access time 80/100/120 ns (max)
- Low power; 11mW Standby, 385/330/275mW Active
- Single 5V supply (±10%)
- Static column mode capability
- 512 refresh cycles; (8 ms)
- 2 variations of refresh; $\overline{RAS}$ only refresh
  $\overline{CS}$ before $\overline{RAS}$ refresh

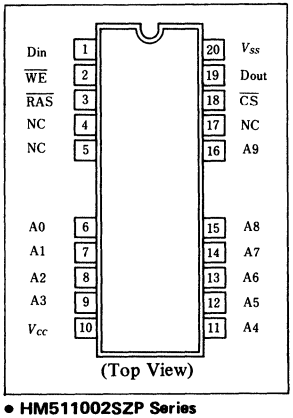
Pin Arrangement

• HM511002SP Series



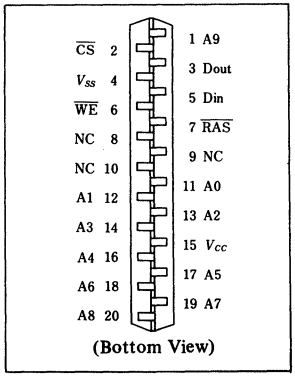
(Top View)

• HM511002SJP Series



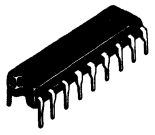
(Top View)

• HM511002SZP Series



(Bottom View)

HM511002SP Series

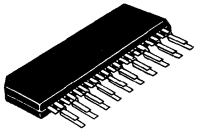


(DP-18C)

HM511002SJP Series

(CP-20D)

HM511002SZP Series



(ZP-20)

Pin Description

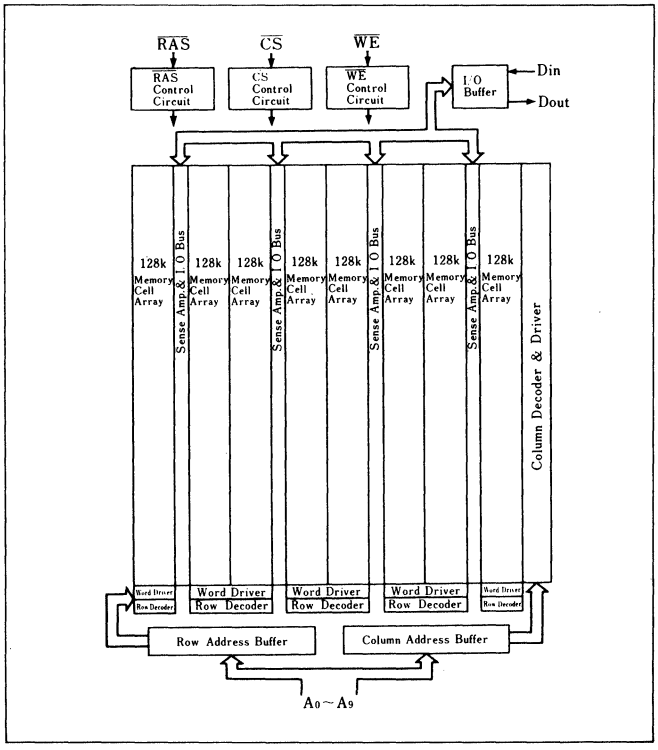
Pin Name	Function
A0 - A9	Address inputs
$\overline{CS}$	Chip select
Din	Data-in
Dout	Data-out
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 - A8	Refresh address inputs

Note) The specifications of this device are subject to change without notice. Please contact your nearest Higachi's Sales Dept. regarding specifications.

Ordering Information

Type No.	Access Time	Package
HM511002P-8S	80 ns	300 mil 18 pin Plastic DIP
HM511002P-10S	100ns	
HM511002P-12S	120ns	
HM511002ZP-8S	80ns	20 pin Plastic ZIP
HM511002ZP-10S	100ns	
HM511002ZP-12S	120ns	
HM511002JP-8S	80ns	20 pin Plastic SOJ
HM511002JP-10S	100ns	
HM511002JP-12S	120ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1 to +7	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511002-8S		HM511002-10S		HM511002-12S		Unit	Test condition		Note
		min	max	min	max	min	max				
Operating current	I_{CC1}	–	70	–	60	–	50	mA	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = Min		*1
Standby current	I_{CC2}	–	2	–	2	–	2	mA	$\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z	TTL interface	
		–	1	–	1	–	1		$\overline{RAS}$, $\overline{CS}$ ≥ V_{CC}–0.2V Dout = High-Z	CMOS interface	
Refresh current	I_{CC3}	–	70	–	60	–	50	mA	$\overline{RAS}$ only refresh, t_{RC} = Min		*1
Standby current	I_{CC5}	–	5	–	5	–	5	mA	$\overline{RAS}$ =V_{IH}, $\overline{CS}$ = V_{IL}, Dout enable		*1
Refresh current	I_{CC6}	–	70	–	60	–	50	mA	$\overline{CS}$ before $\overline{RAS}$ refresh, t_{RC} = Min.		
Static column mode current	I_{CC9}	–	60	–	50	–	40	mA	t_{SC} = Min		*1
Input leakage	I_{LI}	–10	10	–10	10	–10	10	μA	V_{IN} = 0 to +7V		
Output leakage	I_{LO}	–10	10	–10	10	–10	10	μA	V_{OUT} = 0 to +7V, Dout is disabled		
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = –5mA		
	V_{OL}	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2mA		

Note) *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data-in	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data-out	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CS}$ = V_{IH} to disable Dout.

Electrical Characteristics and Recommended AC Operating Conditions

($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)*1,*17,*18

Parameter	Symbol	HM511002-8S		HM511002-10S		HM511002-12S		Unit	Note
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	220	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ Pulse Width	t_{SP}	25	10000	25	10000	30	10000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	*8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	*9
$\overline{RAS}$ Hold Time	t_{RSL}	25	–	25	–	30	–	ns	
$\overline{CS}$ Hold Time	t_{CSH}	80	–	100	–	120	–	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{SRS}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	12	–	15	–	15	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	*7
Refresh Period	t_{REF}	–	8	–	8	–	8	ms	
Access Time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	120	ns	*2,*3
Access Time from $\overline{CS}$	t_{ACS}	–	25	–	25	–	30	ns	*3,*4
Access Time from Address	t_{AA}	–	40	–	45	–	55	ns	*3,*5,*14
Column Address Hold Time to $\overline{RAS}$ on Read	t_{AR}	80	–	100	–	120	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	ns	
$\overline{RAS}$ to Column Address Hold Time	t_{AHR}	15	–	15	–	15	–	ns	*16
Output Hold Time from Address	t_{AOH}	5	–	5	–	5	–	ns	
Output Buffer Turn-off Time	t_{OFF}	–	20	–	25	–	30	ns	*6
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{AHW}	20	–	20	–	25	–	ns	
Column Address Hold Time to $\overline{RAS}$ on Write	t_{AWR}	60	–	75	–	90	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	*10
Write Command Hold Time	t_{WCH}	20	–	20	–	25	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	60	–	75	–	90	–	ns	
Write Command Pulse Width	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	–	25	–	30	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	25	–	25	–	30	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	*11
Data-in Hold Time	t_{DH}	20	–	20	–	25	–	ns	*11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	ns	
Read-Write Cycle Time	t_{RWC}	190	–	220	–	255	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	–	100	–	120	–	ns	*10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	–	25	–	30	–	ns	*10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	ns	*10
Output Hold Time from $\overline{WE}$	t_{WOH}	0	–	0	–	0	–	ns	
$\overline{CS}$ Set-up Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	–	20	–	25	–	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ Hold Time	t_{ZRH}	10	–	10	–	10	–	ns	

• SC Mode Cycle

Parameter	Symbol	HM511002-8S		HM511002-10S		HM511002-12S		Unit	Note
		min	max	min	max	min	max		
SC Mode Cycle Time on Read	t_{SC}	45	–	50	–	60	–	ns	
SC Mode $\overline{RAS}$ Pulse Width	t_{RASC}	–	144000	–	144000	–	144000	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSWD}	80	–	100	–	120	–	ns	
$\overline{CS}$ Precharge Time	t_{SI}	10	–	10	–	15	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	ns	

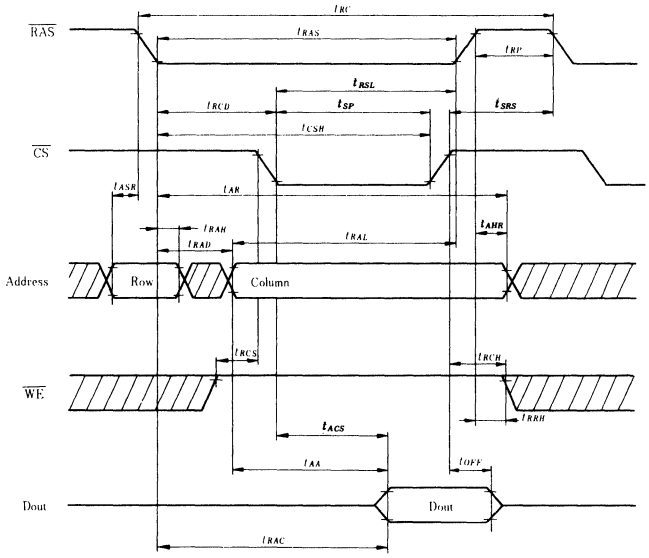
• SC Mode Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM511002-8S		HM511002-10S		HM511002-12S		Unit	Note
		min	max	min	max	min	max		
SC Mode Cycle Time on Read-Write	t_{SRW}	90	–	100	–	120	–	ns	*12
Access Time from Previous $\overline{WE}$	t_{ALW}	–	85	–	95	–	115	ns	*3,*13
Previous $\overline{WE}$ to Column Address Delay Time	t_{LWAD}	25	45	25	50	30	60	ns	*15
Column Address Hold Time to Previous $\overline{WE}$	t_{AHLW}	85	–	95	–	115	–	ns	
Output enable time from $\overline{WE}$	t_{OW}	–	30	–	30	–	35	ns	

Notes) 1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference lvels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insure that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a Reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T.
13. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geqq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{SRW} (max) can be met, t_{LWAD} (max) is specified as a Reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} defines the time at which the column address hold.
17. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
18. At least, 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

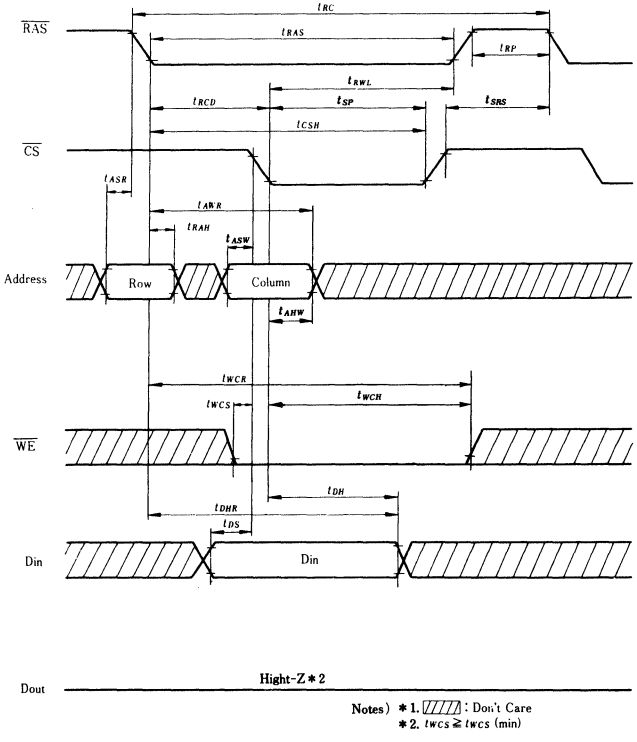
Timing Waveforms

● Read Cycle



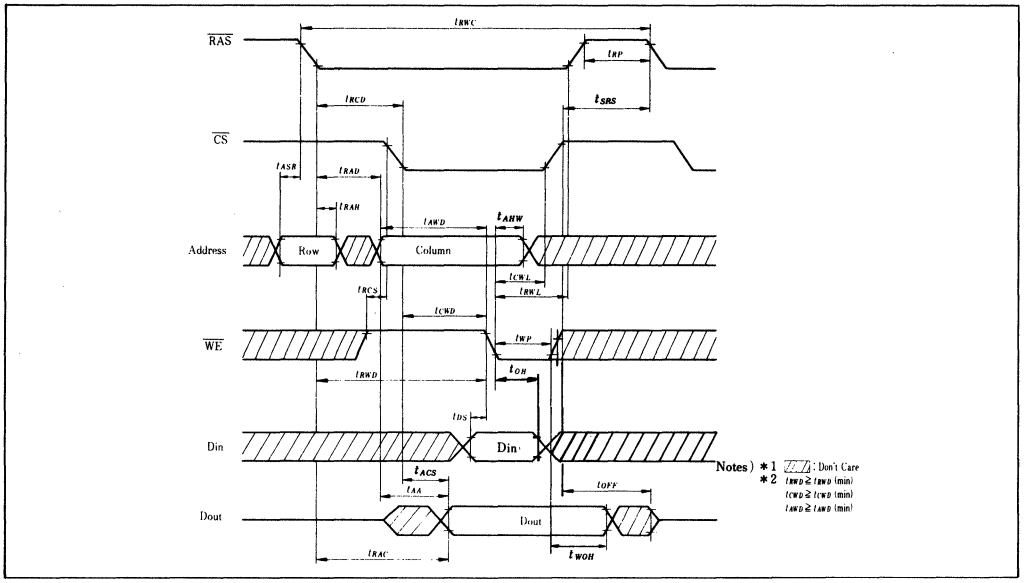
Note) ✱1. ▨ : Don't Care

● Write Cycle

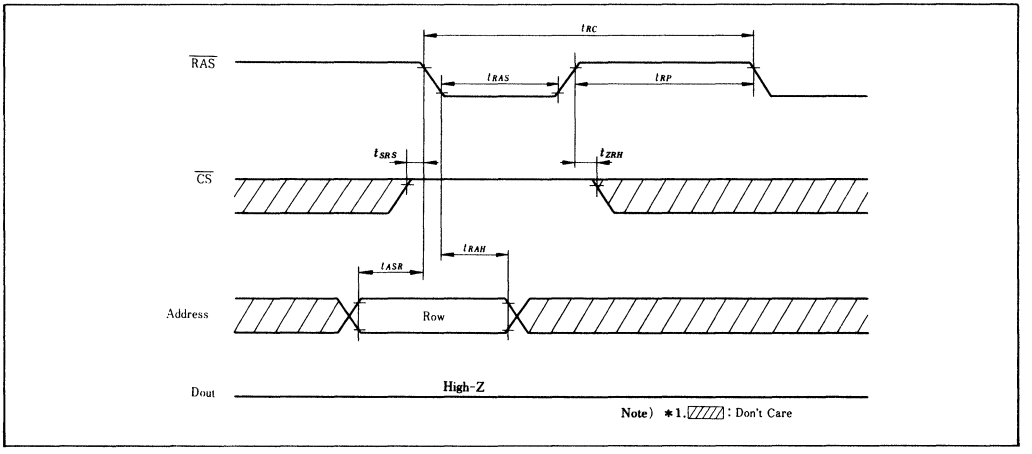


Notes) ✱1. ▨ : Don't Care
✱2. $t_{WCS} \geqq t_{WCS}$ (min)

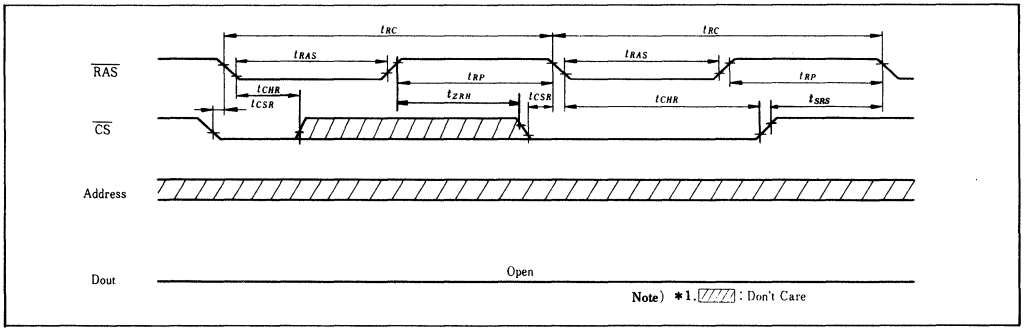
• Read Modify Write Cycle



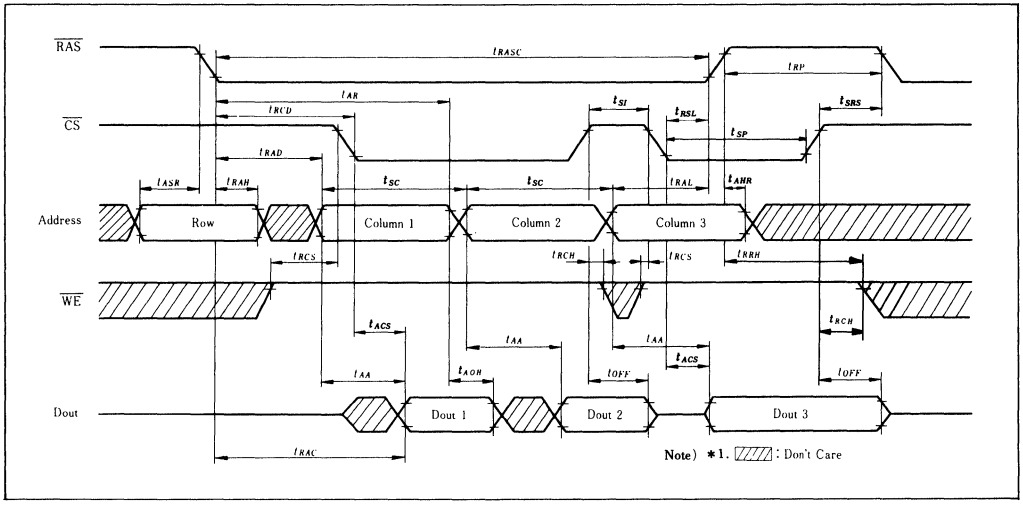
• RAS Only Refresh Cycle



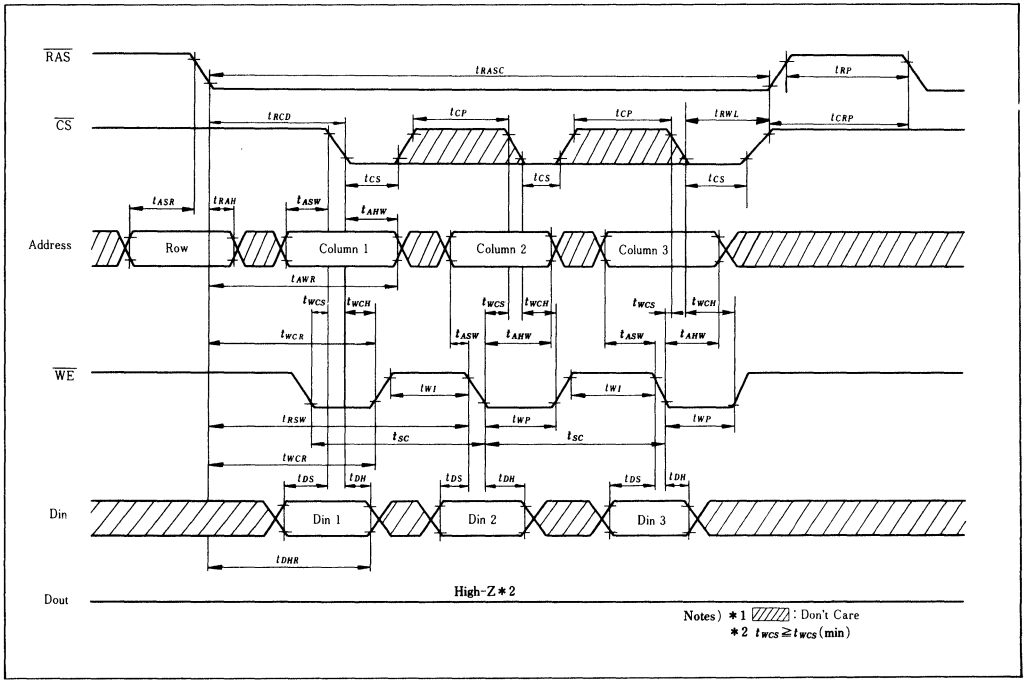
• CS before RAS Refresh Cycle



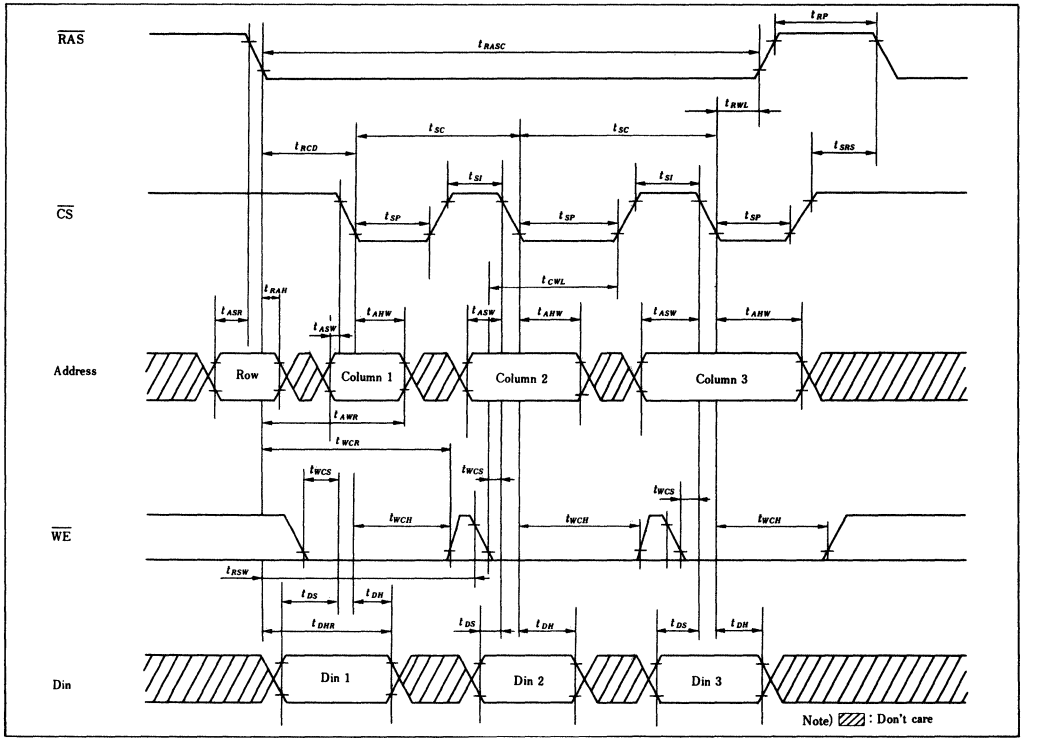
• Static Column Mode Read Cycle



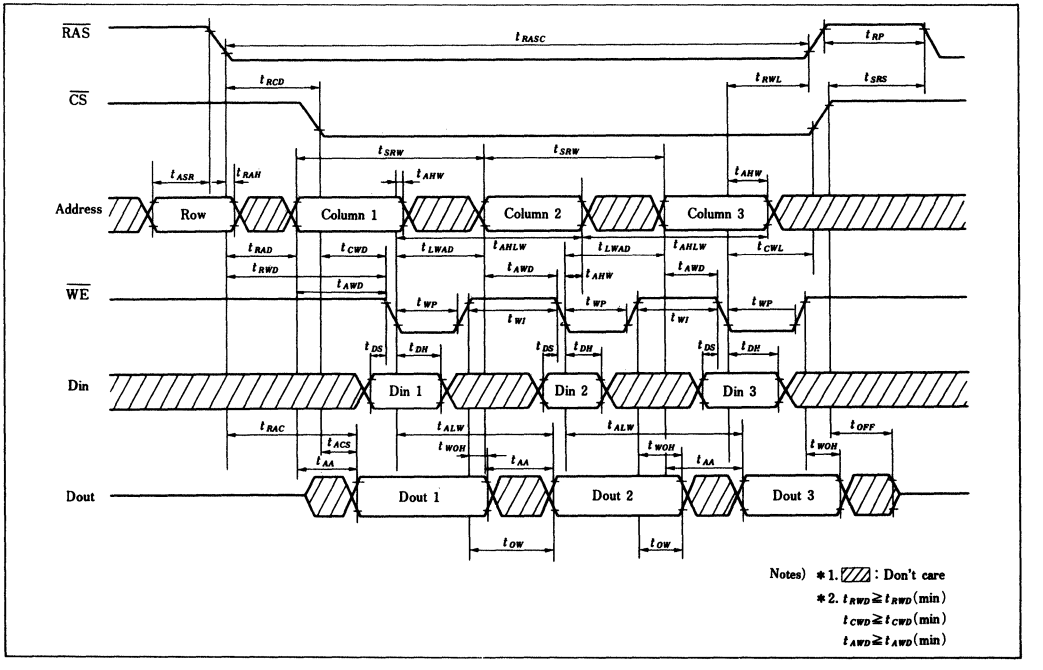
• Static Column Mode Write Cycle-1



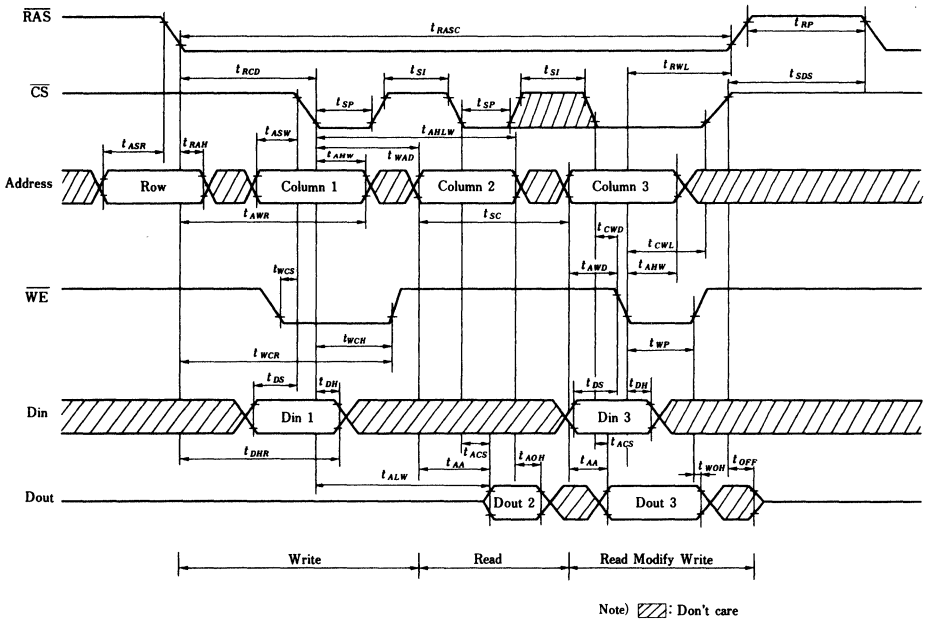
• Static Column Mode Write Cycle-2



• Static Column Mode Read-Modify-Write Cycle



• Static Column Mode Mixed Cycle



MOS DYNAMIC RAM MODULE

HB561003 Series

262,144-word x 9-bit Dynamic Random Access Memory Module

The HB561003 is a 2.25M dynamic random-access memory module organized as 262,144 x 9 bits [bit nine (PD, PQ) is generally used for parity and is controlled by $\overline{PCAS}$] in a 30-pin single-in-line package comprising nine HM50256CP, 262,144 x 1 bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on a substrate together with decoupling capacitors.

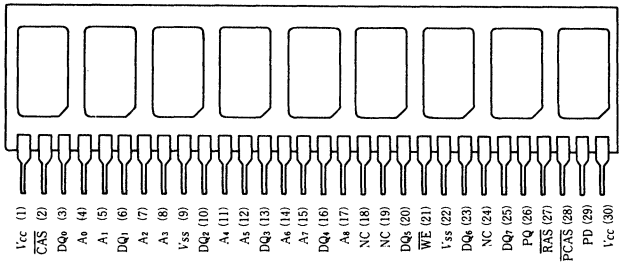
■FEATURES

- 262,144 words x 9 bits Organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561003 operates as nine HM50256CP as shown in the functional block diagram.
- Low Power; Operating: 2,160mW typ. (t_{RC} = 260ns)
  Standby: 135mW typ.
- High speed:

	Access Time from $\overline{RAS}$ (max)	Access Time from $\overline{CAS}$ (max)	Read or Write Cycle (min)
HB561003A/AR/B-12	120ns	70ns	220ns
HB561003A/AR/B-15	150ns	75ns	260ns
HB561003A/AR/B-20	200ns	100ns	330ns

- Page mode capability
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
  $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature: 0°C to +70°C
- HB561003A/AR is leaded type
- HB561003B is leadless type (socket type)

■PIN ARRANGEMENT



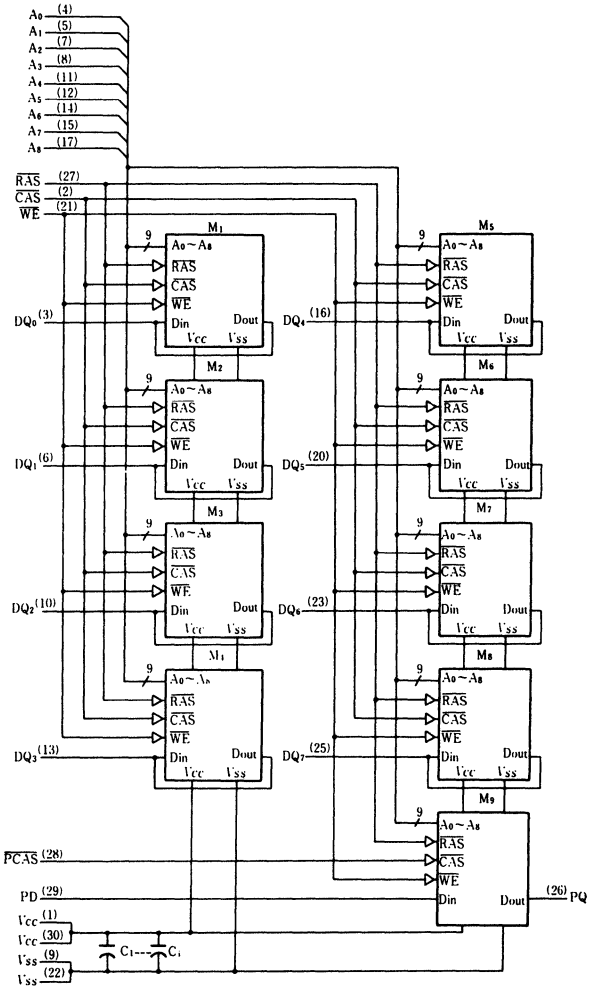
Note) HB561003B's pin arrangement is same as HB561003A/AR. (Side View)

- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
- Separate $\overline{CAS}$ control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

■ PIN DESCRIPTION

A0-A8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobes
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobes
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground

■FUNCTIONAL BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}: −1V to +7V
Operating temperature, T_a (Ambient): 0°C to +70°C
Storage temperature (Ambient): −55°C to +125°C
Power dissipation: 9W
Short circuit output current: 50mA

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Test Conditions		Symbol	min.	max.	Unit	Notes
Operating current	$\overline{RAS}$, $\overline{CAS}$=cycle t_{RC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC1}	–	495 630 747	mA	1
Standby current	$\overline{RAS}$=V_{IH}, D_{out}=High Z		I_{CC2}	–	40	mA	
Refresh current	$\overline{RAS}$ only refresh t_{RC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC3}	–	378 477 558	mA	
Standby current	$\overline{RAS}$=V_{IH}, D_{out}=enable		I_{CC5}	–	90	mA	1
Refresh current	$\overline{CAS}$ before $\overline{RAS}$ refresh t_{RC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC6}	–	405 522 621	mA	
Page made supply current	$\overline{RAS}$=V_{IL}, $\overline{CAS}$=cycle, t_{PC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC7}	–	333 432 513	mA	
Input leakage	0< V_{in} <7V		I_{LI}	−10	10	μA	
Output leakage	0< V_{out} <7V, D_{out}=disable		I_{LO}	−10	10	μA	
Output levels	High (I_{out}=−5mA)		V_{OH}	2.4	V_{CC}	V	
	Low (I_{out}=4.2mA)		V_{OL}	0	0.4	V	

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	–	60	pF	2
Clocks	C_{I2}	–	75	pF	2, 3
DQ	$C_{I/O}$	–	17	pF	2, 3
PQ	C_O	–	12	pF	2, 3
PD	C_{I3}	–	10	pF	2

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)[1), 10), 11)]

Parameter	Symbol	HB561003-12		HB561003-15		HB561003-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	70	–	75	–	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	–	30	–	40	–	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	–	260	–	330	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	70	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	35	50	35	75	35	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	70	–	75	–	100	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	25	–	25	–	30	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	75	–	100	–	130	–	ns	
Read Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	45	–	45	–	55	–	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	155	–	ns	
Write Command Pulse Width	t_{WP}	45	–	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	–	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	–	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9

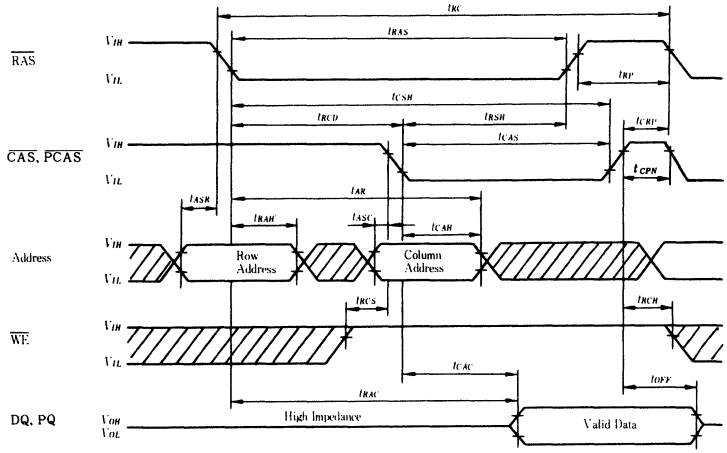
(to be continued)

Parameter	Symbol	HB561003-12		HB561003-15		HB561003-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Data-in Hold Time	t_{DH}	45	–	45	–	55	–	ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{CAS}$ Precharge Time	t_{CPN}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Set-up Time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	120	–	150	–	200	–	ns	
$\overline{RAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Page Mode Read or Write Cycle	t_{PC}	130	–	145	–	190	–	ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	50	–	60	–	80	–	ns	

Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. Early write cycle only ($t_{WCS} \geqq t_{WCS}$ (min)).
9. These parameters are referenced to $\overline{CAS}$ leading edge.
10. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.
11. At least 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.

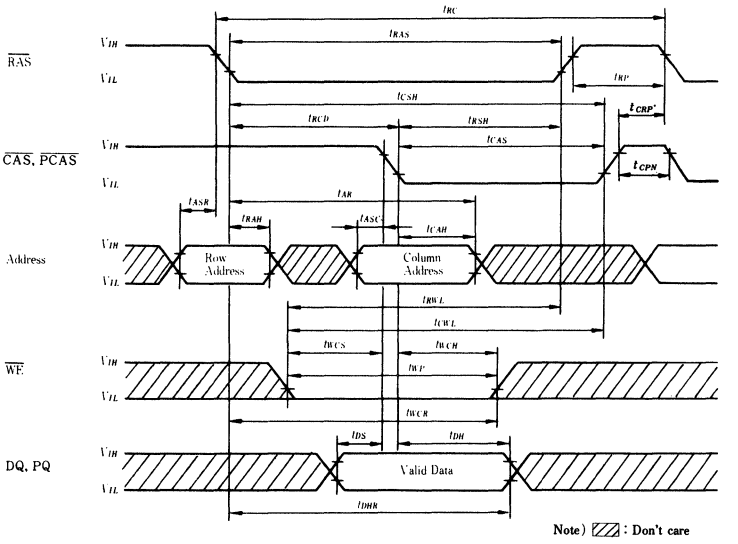
■WAVE FORMS

●Read Cycle

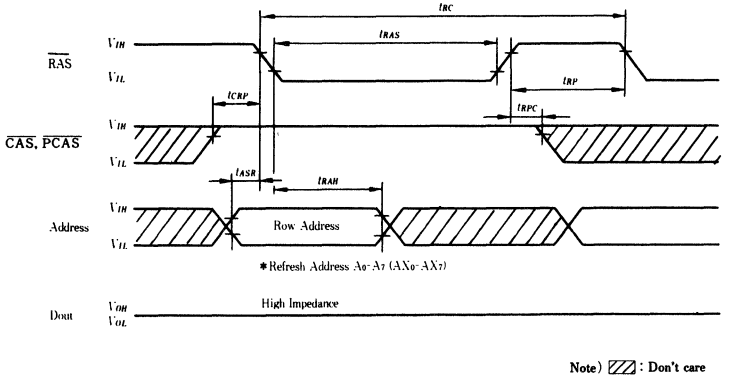


Note) ▨ : Don't care

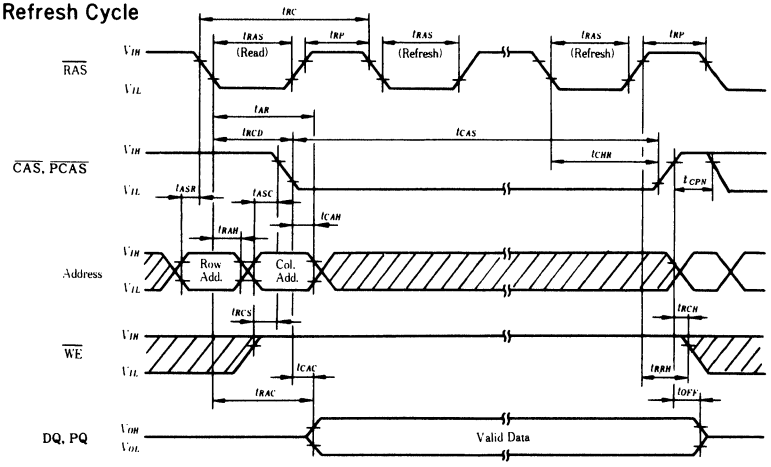
● Write Cycle



● $\overline{\text{RAS}}$ Only Refresh Cycle

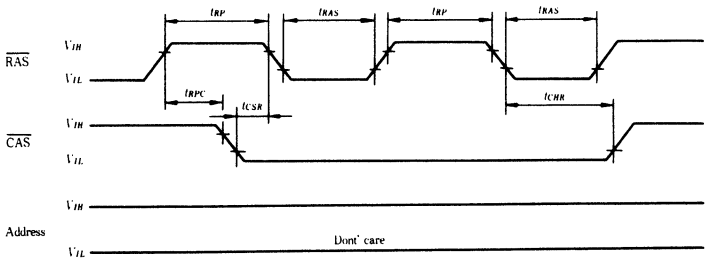


● Hidden Refresh Cycle

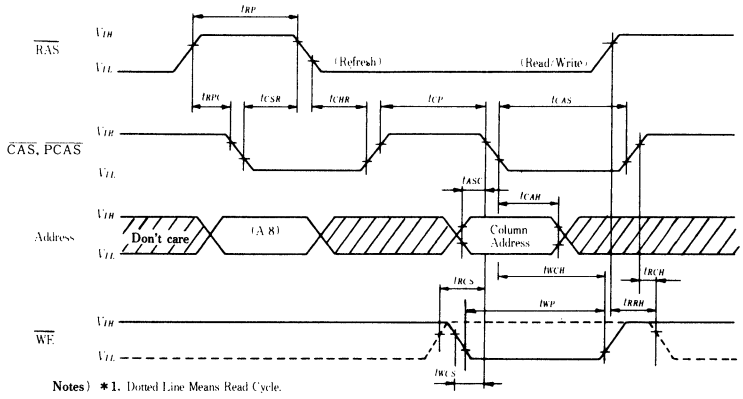


Note) ▨ : Don't care

● CAS Before RAS Refresh Cycle

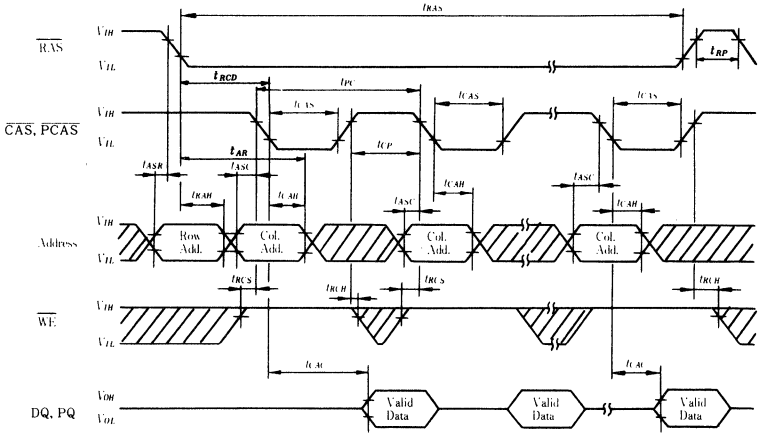


● Counter Test



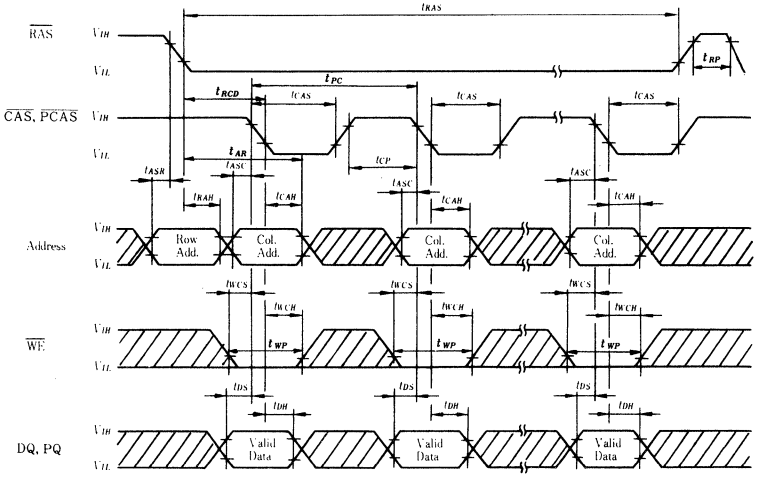
Notes) *1. Dotted Line Means Read Cycle.
*2. ▨ : Don't care

● Page Mode Read Cycle



Note) ▨ : Don't care

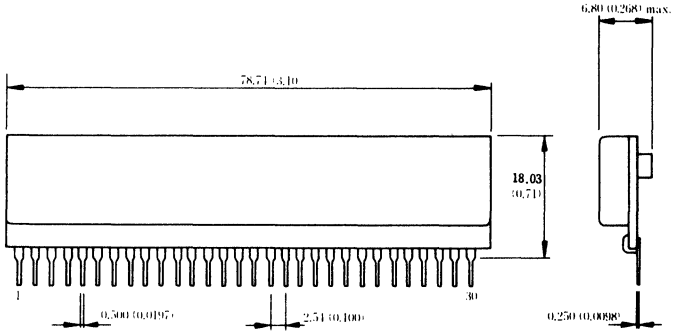
● Page Mode Write Cycle



Note) ▨ : Don't care

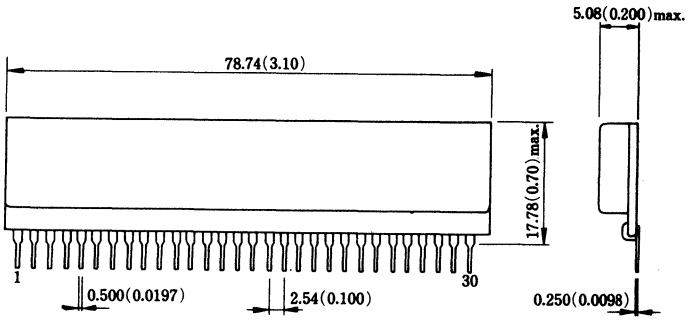
■PACKAGE OUTLINE

● HB561003A Series



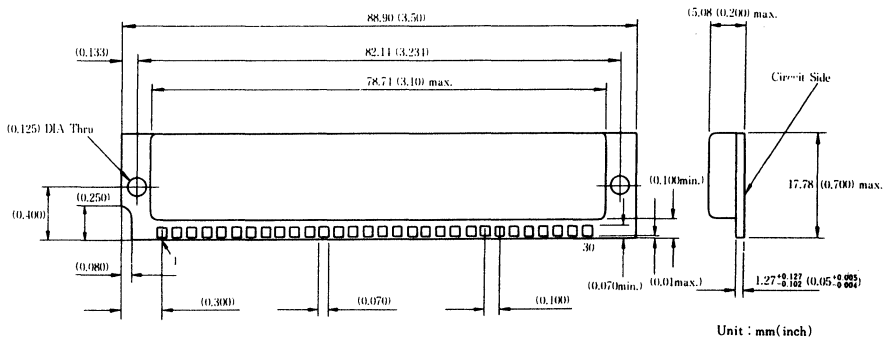
Unit : mm(inch)

● HB561003AR Series



Unit : mm(inch)

● HB561003B Series



Unit : mm(inch)

HB561409 Series

262,144-word x 9-bit Dynamic Random Access Memory Module

The HB561409 is a 256k x 9 dynamic RAM module, mounted 9 pieces of 256k-bit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB561409 is 30-pin single-in-line package having two types; Lead type (HB561409A) and Socket type (HB561409B). Therefore, the HB561409 makes high density mounting possible without surface mount technology.
The HB561409 provides common data input and output, and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors to reduce noise.

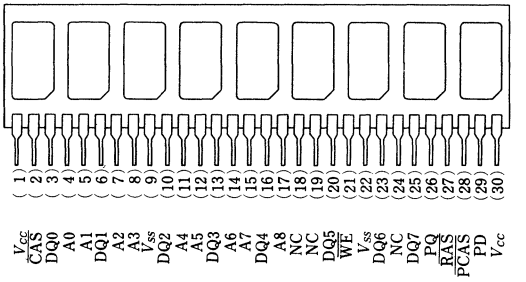
Features

- 262,144 words x 9 bits organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM51256CP)
- HB561409A/B operates as nine HM51256CPs as shown in the functional block diagram
- Low Power: Operating . . . . . 1,800mW (typ) (t_{RC} = 180ns)
  Standby . . . . . 60mW (typ)
- High speed: Access time from $\overline{RAS}$ (max) = 100ns
  Access time from address (max) = 55ns
  Read or write cycle (min) = 180ns
- High speed page mode capability (t_{PC} = 65ns)
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
  $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature . . . . . 0°C to +70°C.

Ordering Information

Type No.	Access Time	Package
HB561409A-10	100ns	30 pin Lead Type
HB561409B-10	100ns	30 pin Socket Type

Pin Arrangement



(Side View)

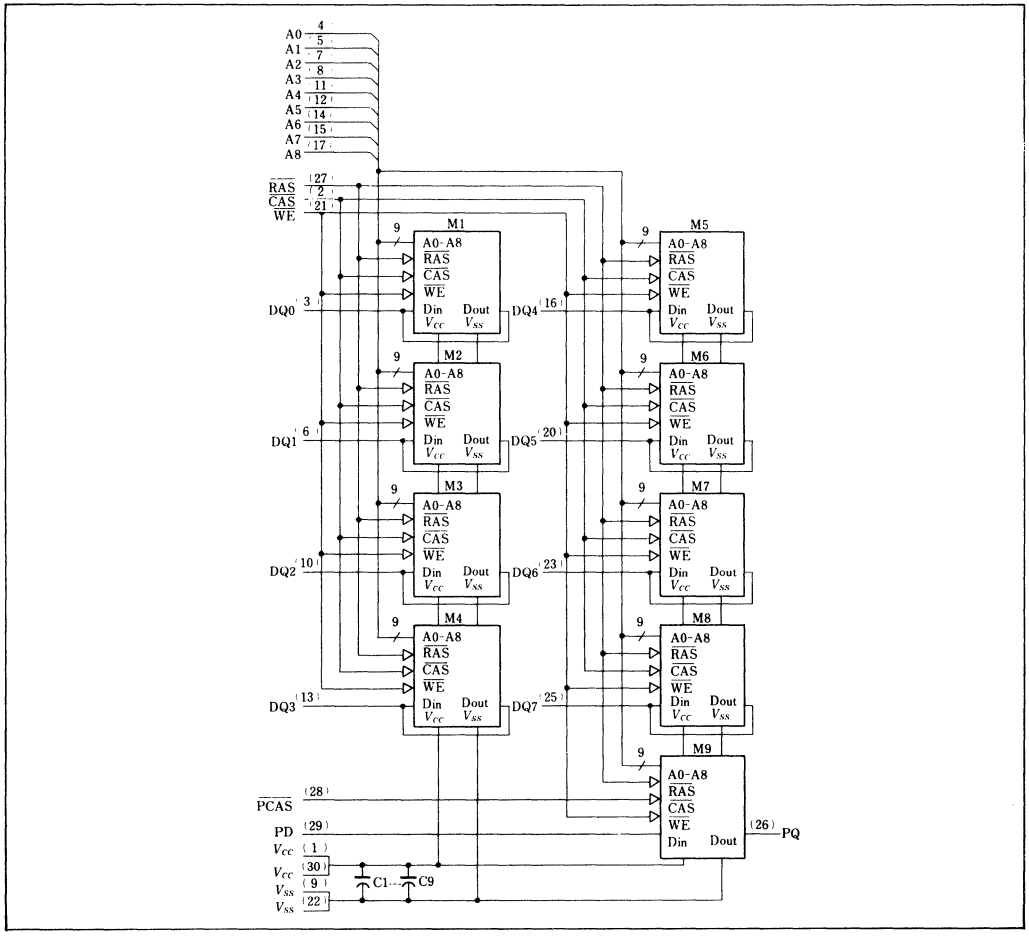
Note) HB561409B's pin arrangement is same as HB561409A.

- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
- Separate $\overline{CAS}$ control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

Pin Description

A0-A8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobe
Vcc	+5V Supply
Vss	Ground
$\overline{WE}$	Write Enable

Functional Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, T_a (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . −55°C to +125°C
Power dissipation 9W
Short circuit output current 50mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	—	5.5	V	1
Input Low voltage	V_{IL}	−1.0	—	0.8	V	1

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Operating current t_{RC}=180ns	Icc1	—	540	mA	*1
Standby current	Icc2	—	18	mA	
Refresh current t_{RC}=180ns	Icc3	—	540	mA	$\overline{RAS}$ only refresh
Standby current (Dout Enable)	Icc4	—	54	mA	*1
Refresh current t_{RC}=180ns	Icc5	—	495	mA	$\overline{CAS}$ before $\overline{RAS}$ refresh
Operating current t_{PC}=65ns	Icc6	—	540	mA	*1, High speed page mode
Input leakage 0<Vin<7V	I_{LI}	−10	10	μA	
Output leakage 0<Vout<7V	I_{LO}	−10	10	μA	Dout is disabled
Output levelsHigh Iout=−5mA	V_{OH}	2.4	Vcc	V	
Low Iout = 4.2mA	V_{OL}	0	0.4	V	

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Type	Max	Unit	Notes
Address	C_{I1}	—	60	pF	*2
Clocks	C_{I2}	—	75	pF	*2,3
DQ	$C_{I/O}$	—	17	pF	*2,3
PQ	C_O	—	12	pF	*2,3
PD	C_{I3}	—	10	pF	*2

Notes) ***1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.**
***2. Capacitance measured with Boonton Meter or effective capacitance measuring method.**
***3. $\overline{CAS}$ = V_{IH} to disable Dout.**

Electrical Characteristics and Recommended AC Operating Conditions

Read, Write and Refresh Cycles (Common Parameter) (Ta = 0 to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RC}	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	75	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CAH}	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	80	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	ns	*8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	45	ns	*9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	ns	*7
Refresh Period	t_{REF}	—	4	ms	

• Read Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Access Time from $\overline{RAS}$	t_{RAS}	—	100	ns	*2, *3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	ns	*3, *4
Access Time from Address	t_{AA}	—	55	ns	*3, *5
Read Command Set-up Time	t_{RCS}	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	30	ns	*6

• Write Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Write Command Set-up Time	t_{WCS}	0	—	ns	*10
Write Command Hold Time	t_{WCH}	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	85	—	ns	
Write Command Pules Width	t_{WP}	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	ns	
Data-in Set-up Time	t_{DS}	0	—	ns	*11
Data-in Hold Time	t_{DH}	25	—	ns	*11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	80	—	ns	

• Refresh Cycle

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	ns	

• High Speed Page Mode Cycle

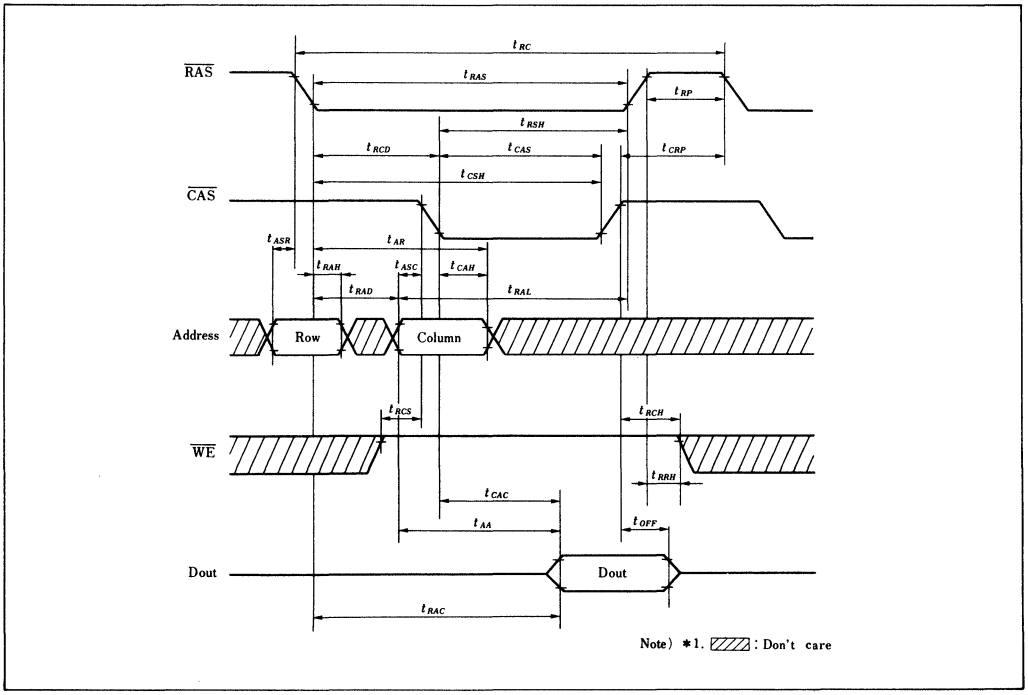
Parameter	Symbol	Min	Max	Unit	Notes
High Speed Page Mode Cycle Time	t_{PC}	65	—	ns	*12
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RAPC}	75	75000	ns	*13
$\overline{CAS}$ Precharge Time	t_{CP}	20	—	ns	
Write Invalid Time	t_{WI}	15	—	ns	
Access Time from Column Precharge Time	t_{CAP}	—	60	ns	*14

Notes) *1. AC measurements assume t_T = 5ns.
*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).
*5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max.)
*6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage level.
*7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

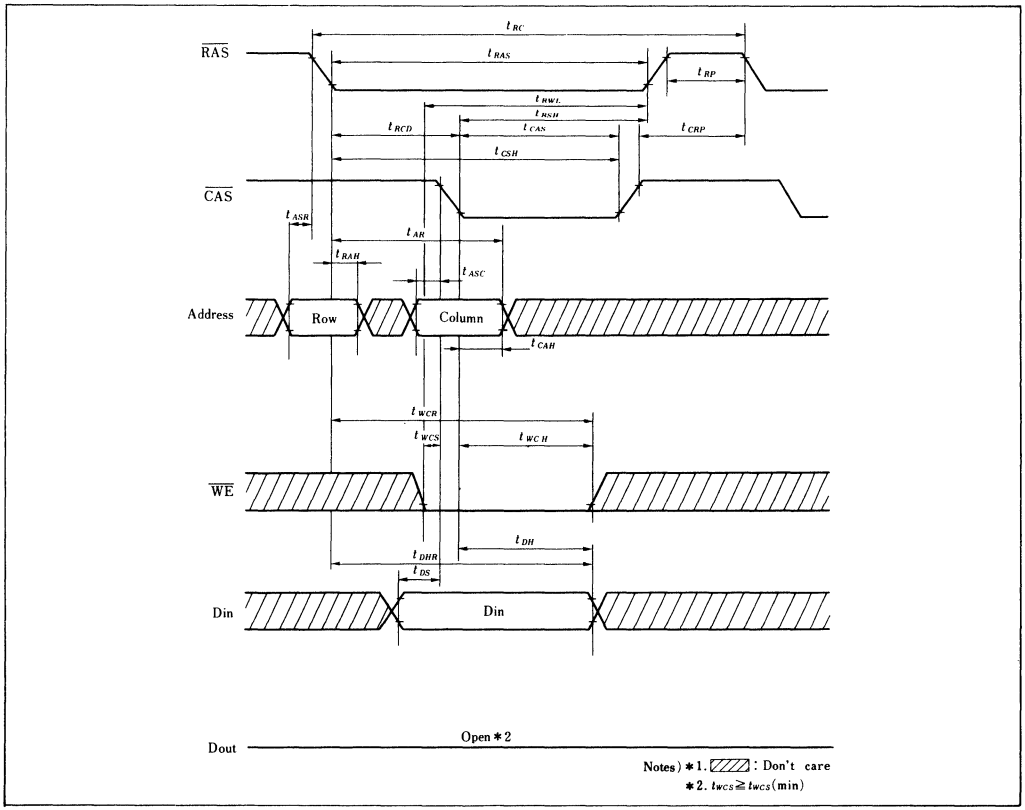
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. Only early write cycle to prevent contention on Data in and out ($t_{WCS} \geqq 0$).
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle.
12. Assumes that $t_{ASC} = t_{CP}$-5ns.
13. t_{RAPC} defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
15. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
16. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using an internal refresh counter.

Timing Waveforms

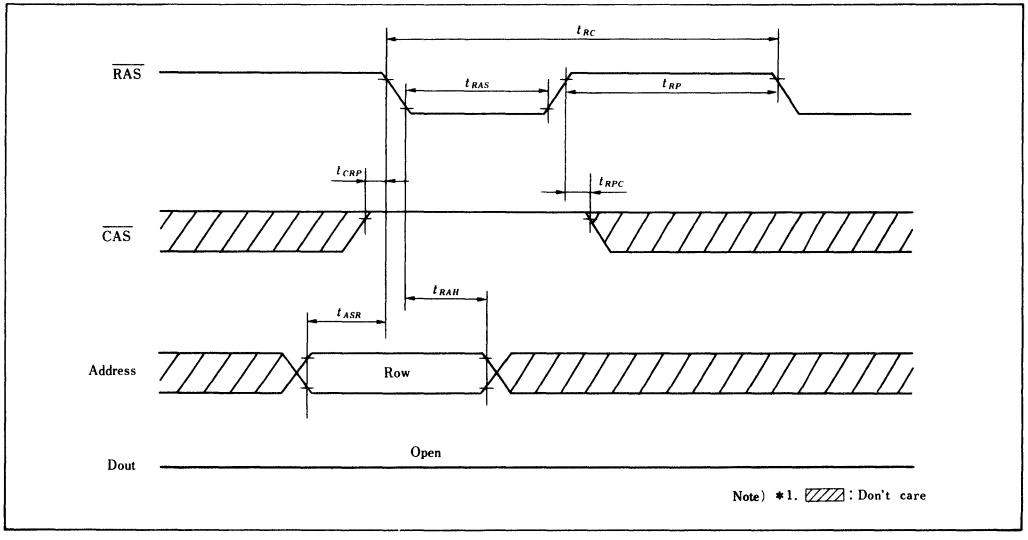
Read Cycle



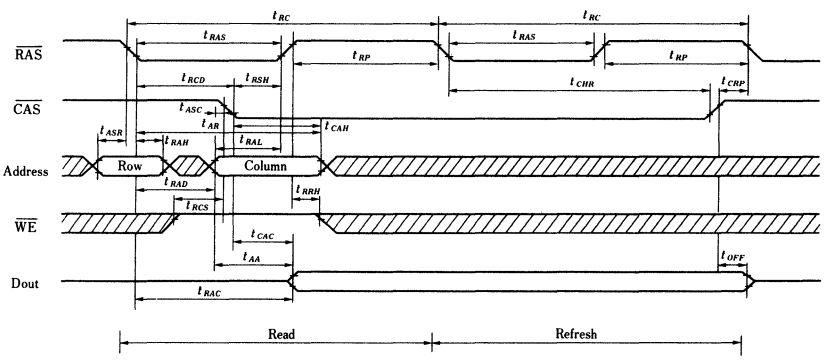
Write Cycle



RAS Only Refresh Cycle

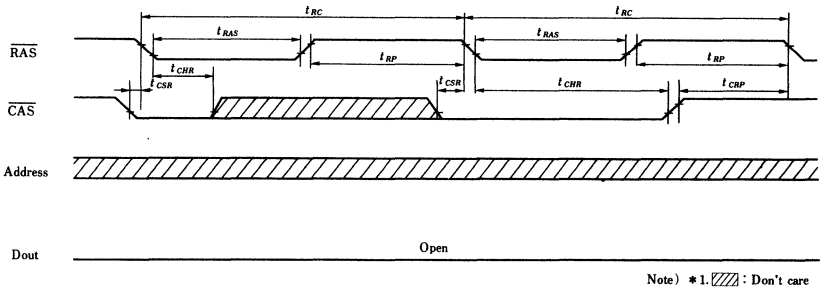


Hidden Refresh Cycle



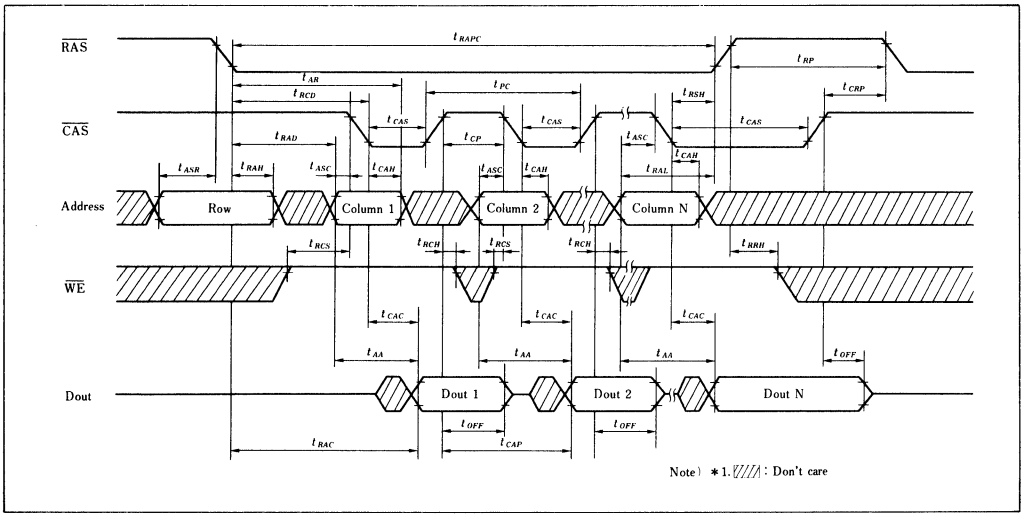
Note) *1. ▨ : Don't care

CAS before RAS Refresh Cycle



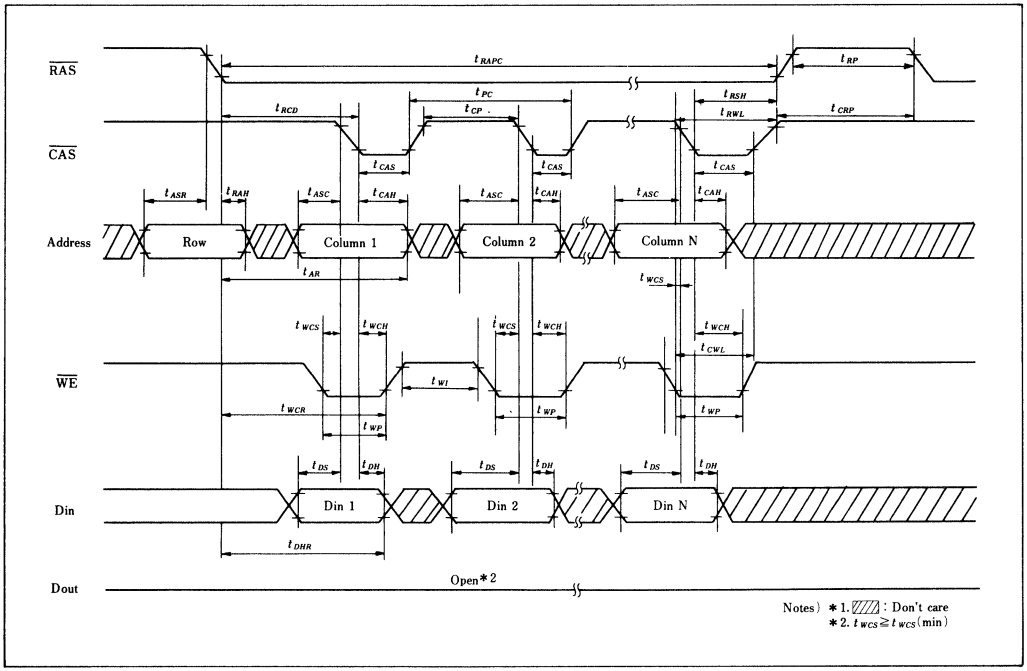
Note) *1. ▨ : Don't care

High Speed Page Mode Read Cycle



Note) ∗1. ▨: Don't care

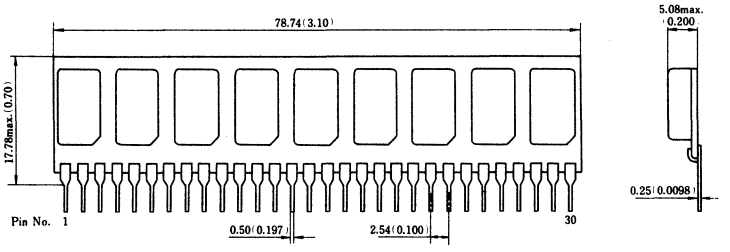
High Speed Page Mode Write Cycle



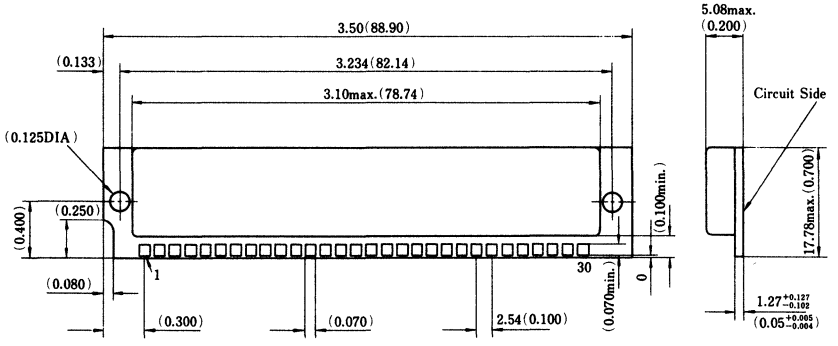
Notes) ∗1. ▨: Don't care
∗2. $t_{WCS} \geq t_{WCS}$(min)

Package Outline, Unit; mm (inch)

HB561409A



HB561409B



Note) Copper contact pads are overcoated with Tin/Lead.

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HB561409L Series

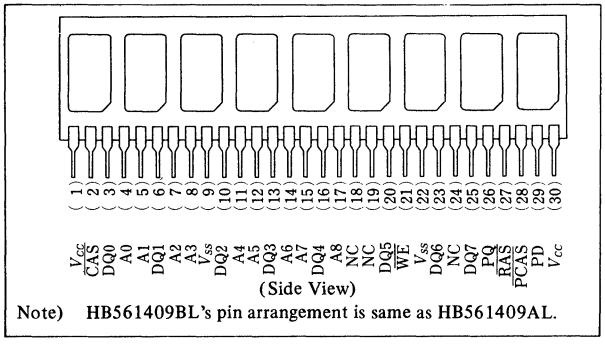
262,144 x 9 bit Dynamic Random Access Memory Module

The HB561409L is a 256k x 9 dynamic RAM module, mounted 9 pieces of 256k-bit low power DRAM (HM51256LCP) sealed in PLCC package. An outline of HB561409L is 30-pin single-in-line package having two types; Lead type (HB561409AL) and Socket type (HB561409BL). Therefore, the HB561409L makes high density mounting possible without surface mount technology. The HB561409L provides common data input and output, and also provides separate I/O on partity bit for parity check. Its module board has decoupling capacitors to reduce noise.

Features

- Utilizes nine low power CMOS 256K dynamic RAMs in PLCC (HM51256LCP)
- 262,144 words x 9 bits organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- HB561409AL/BL operates as nine HM51256LCPs as shown in the functional block diagram
- Low Power: Operating 1.8W/1.6W
  Standby . . . . . 60mW (TTL level);
  9mW (CMOS level)
- Data retention current: 2.7mA/t_{REF} = 32ms
- High speed: Access time from $\overline{RAS}$ (max) = 100ns/120ns
  Access time from address (max) = 55ns/65ns
  Read or write cycle (min) = 180ns/210ns
- High speed page mode capability (t_{PC} = 65ns/75ns)
- Edge triggered write capability
- TTL compatible
- 256 refresh cycles/32ms
- 3 variations of refresh
  $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh
- Operating ambient air temperature . . . . . 0°C to +70°C

Pin Arrangement (HB561409AL)



(Side View)

Note) HB561409BL's pin arrangement is same as HB561409AL.

- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
- Separate $\overline{CAS}$ control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

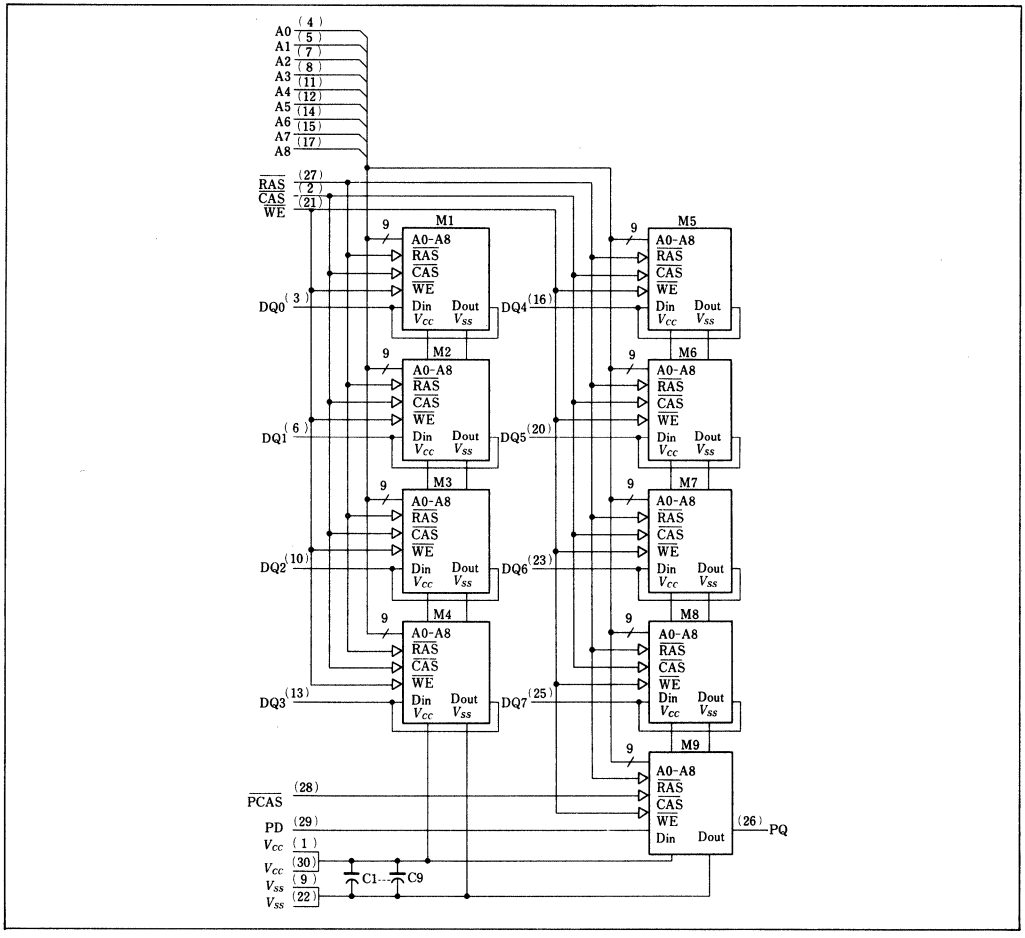
Ordering Information

Type	Access Time	Package
HB561409AL-10	100ns	30pin
HB561409AL-12	120ns	Lead Type
HB561409BL-10	100ns	30pin
HB561409BL-12	120ns	Socket Type

Pin Description

A0-A8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobe
V_{CC}	+5V Supply
V_{SS}	Ground
$\overline{WE}$	Write Enable

Functional Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . −55°C to +125°C
Power dissipation 9W
Short circuit output current 50mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	max	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	—	5.5	V	1
Input Low voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	Min	Max	Unit	Notes
Operating current $t_{RC}=210ns$ $\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=180ns$	Icc1	—	450 540	mA	1
Standby current $\overline{RAS}=V_{IH}$ Dout = High Impedance.	Icc2	—	18	mA	
Refresh current $t_{RC}=210ns$ $t_{RC}=180ns$	Icc3	—	480 540	mA	$\overline{RAS}$ only refresh
Standby current $\overline{RAS}=V_{IH}$ Dout Enable	Icc4	—	54	mA	1
Standby current $\overline{RAS}$, $\overline{CAS} \geqq Vcc-0.2V$	Icc5	—	1.8	mA	
Refresh current $t_{RC}=210ns$ $t_{RC}=180ns$	Icc6	—	430 495	mA	$\overline{CAS}$ before $\overline{RAS}$ refresh
Operating current $t_{PC}=75ns$ $t_{PC}=65ns$	Icc7	—	400 450	mA	1 High speed page mode
Input leakage $0<Vin<7V$	I_{LI}	−10	10	μA	
Output leakage $0<Vout<7V$	I_{LO}	−10	10	μA	Dout is disabled
Output levels High Iout = −5mA	V_{OH}	2.4	Vcc	V	
Output levels Low Iout = 4.2mA	V_{OL}	0	0.4	V	

Capacitance ($V_{CC} = 5V \pm 10\%$, $Ta = 25°C$)

Parameter	Symbol	Type	Max	Unit	Notes
Address	C_{I1}	—	60	pF	2
Clocks	C_{I2}	—	75	pF	2,3
DQ	$C_{I/O}$	—	17	pF	2,3
PQ	C_O	—	12	pF	2,3
PD	C_{I3}	—	10	pF	2

Notes) 1. Icc depends on output loading condition when the device is selected, Icc max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable Dout.

Electrical Characteristics and Recommended AC Operating Conditions

Read, Write and Refresh Cycles (Common Parameter) ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	HB561409L-10		HB561409L-12		Unit	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	180	—	210		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	75	10000	85	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	—	35		ns	
Column Address Set-up Time	t_{ASC}	0	—	0		ns	
Column Address Hold Time	t_{CAH}	25	—	25		ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	80	—	95		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	85	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	45	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	35		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120		ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10		ns	

(to be continued)

Parameter	Symbol	HB561409L-10		HB561409L-12		Unit	Notes
		Min	Max	Min	Max		
ROW Address Set-up Time	t_{ASR}	0	–	0		ns	
ROW Address Hold Time	t_{RAH}	15	–	15		ns	
Transion Time (Rise and Fall)	t_T	3	50	3	50	ns	7
Refresh Period	t_{REF}	–	32		32	ns	

• Read Cycle

Parameter	Symbol	HB561409L-10		HB561409L-12		Unit	Notes
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	–	30	–	35	ns	3,4
Accces Time from Address	t_{AA}	–	55	–	65	ns	3,5
Read Command Set-up Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	55	–	65	–	ns	
Output Buffer Turn-Off Time	t_{OFF}	0	30	0	35	ns	6

• Write Cycle

Parameter	Symbol	HB561409L-10		HB561409L-12		Unit	Notes
		Min	Max	Min	Max		
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	30	—	35	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	85	—	90	—	ns	
Write Command Pulse Width	t_{WP}	25	—	30	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	25	—	30	—	ns	11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	80	—	95	—	ns	

• Refresh Cycle

Parameter	Symbol	HB561409L-10		HB561409L-12		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	ns	

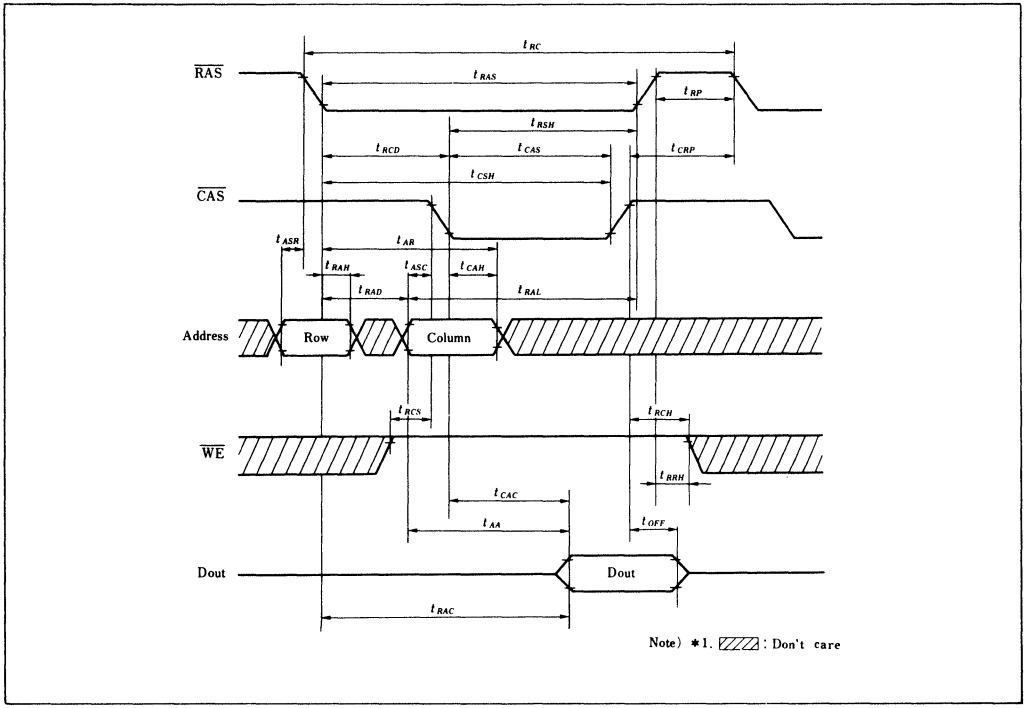
• High Speed Page Mode Cycle

Parameter	Symbol	HB561409L-10		HB561409L-12		Unit	Notes
		Min	Max	Min	Max		
High Speed Page Mode Cycle Time	t_{PC}	65	—	75	—	ns	12
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RAPC}	75	75000	85	75000	ns	13
$\overline{CAS}$ Precharge Time	t_{CP}	20	—	25	—	ns	
Write Invalid Time	t_{WI}	15	—	15	—	ns	
Access Time from Column Precharge Time	t_{CAP}	—	60	—	70	ns	14

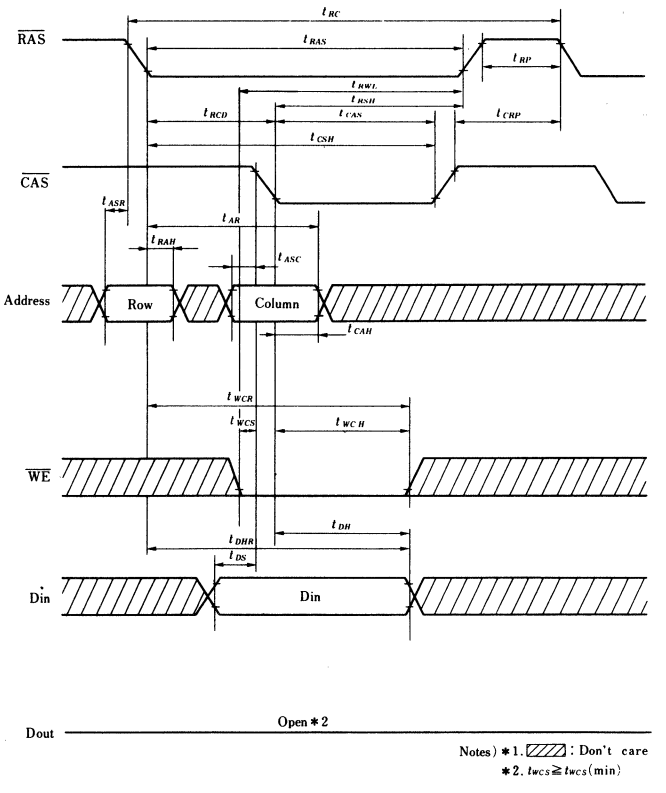
Notes) 1. AC measurement assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage level.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Only early write cycle to prevent contention on Data in and out ($t_{WCS} \geqq 0$).
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle.
12. Assumes that $t_{ASC} = t_{CP}$-5ns.
13. t_{RAPC} defines $\overline{RAS}$ pulse width in High Speed Page mode cycle.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
15. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
16. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using an internal refresh counter.

Timing Waveforms

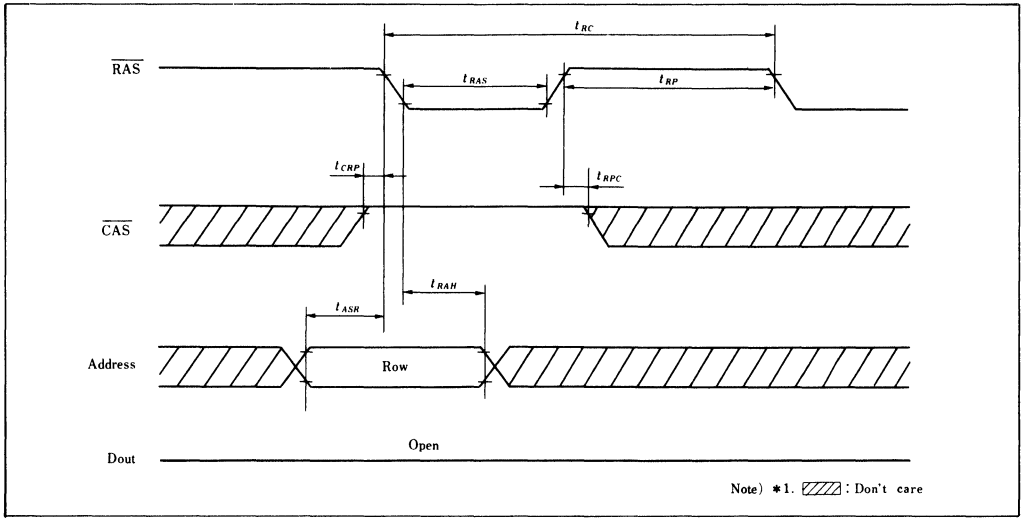
Read Cycle



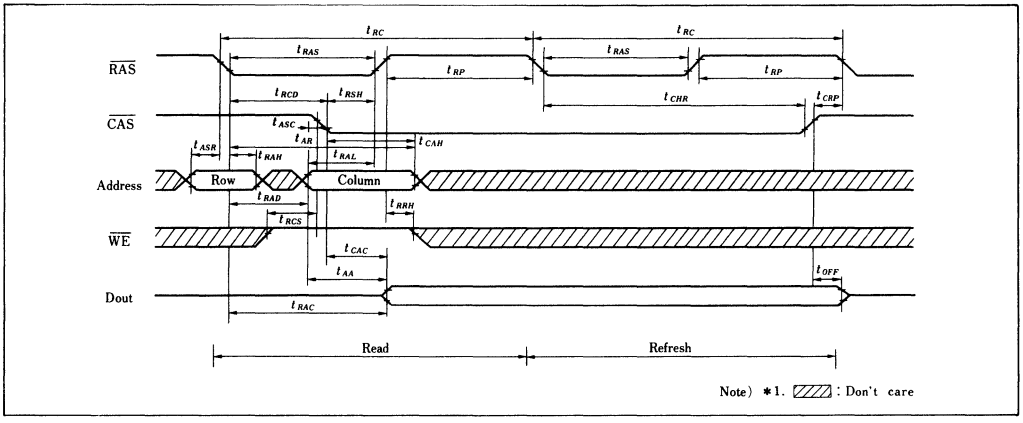
Write Cycle


t_{RC}
RAS
t_{RAS}
t_{RP}
t_{RWL}
t_{RSH}
t_{RCD}
t_{CAS}
t_{CRP}
t_{CSH}
CAS
t_{ASR}
t_{AR}
t_{RAH}
t_{ASC}
Address
Row
Column
t_{CAH}
t_{WCR}
t_{WCS}
t_{WCH}
WE
t_{DH}
t_{DHR}
t_{DS}
Din
Din
Dout
Open *2
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geqq t_{WCS}$(min)

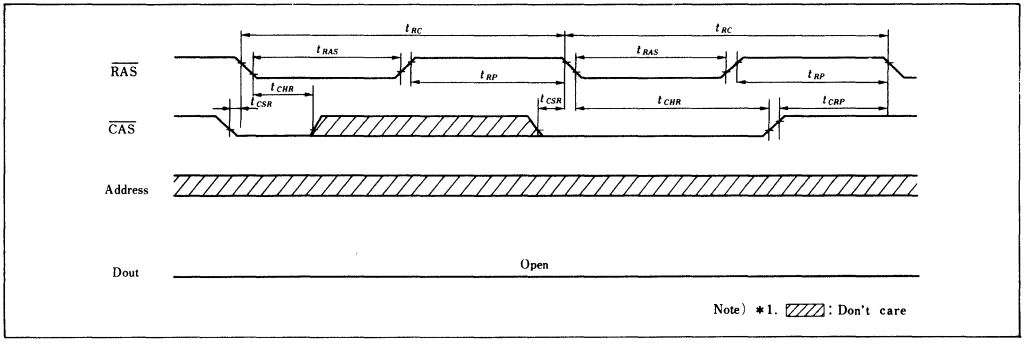
$\overline{RAS}$ Only Refresh Cycle



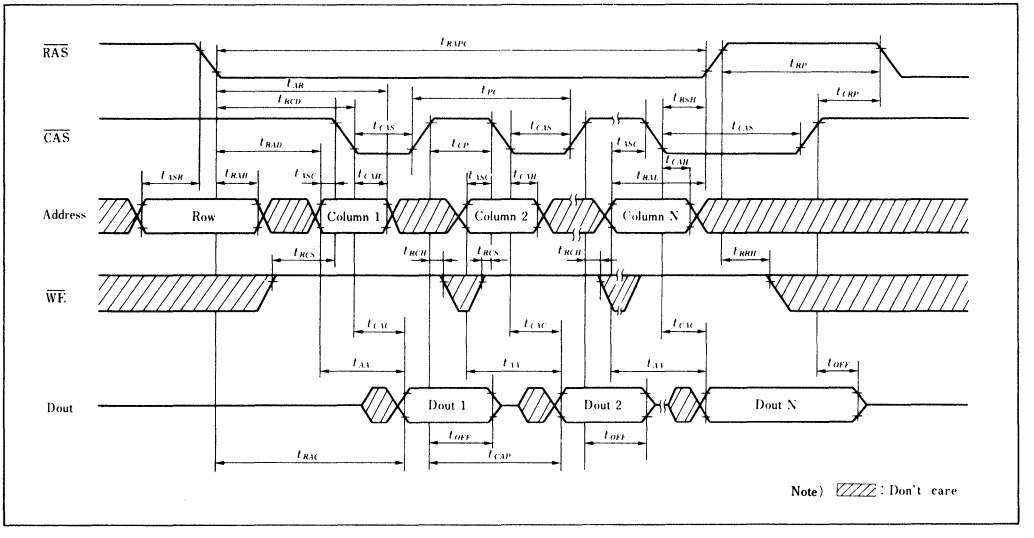
Hidden Refresh Cycle



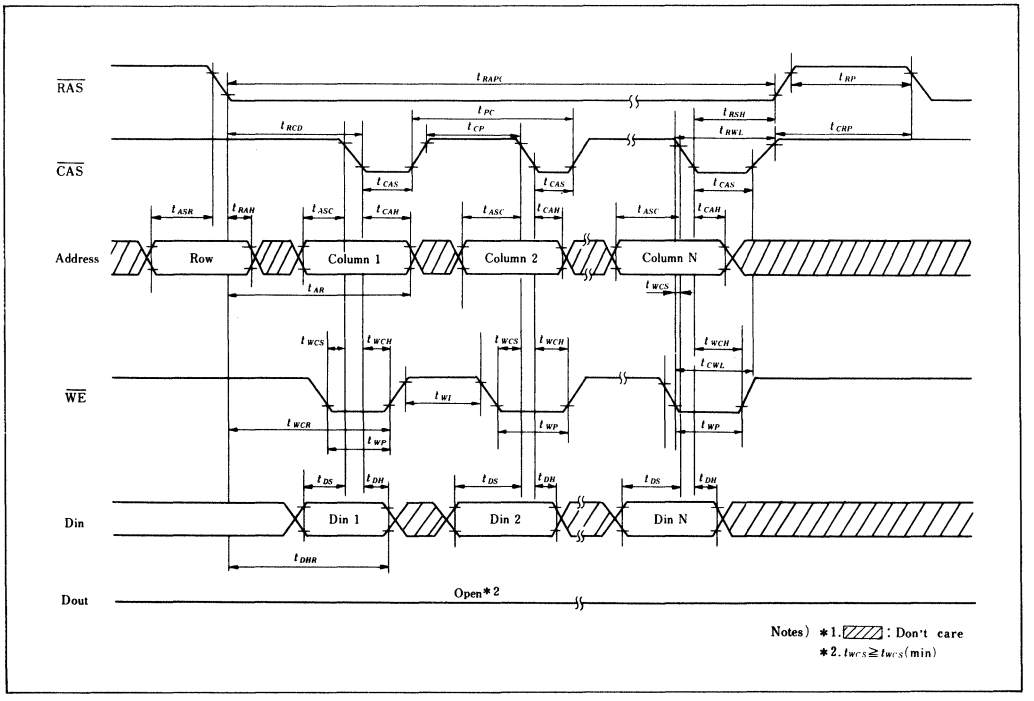
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



High Speed Page Mode Read Cycle

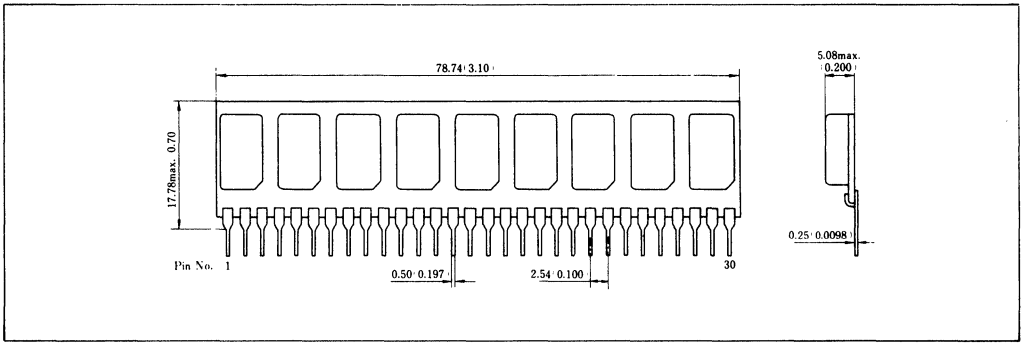


High Speed Page Mode Write Cycle

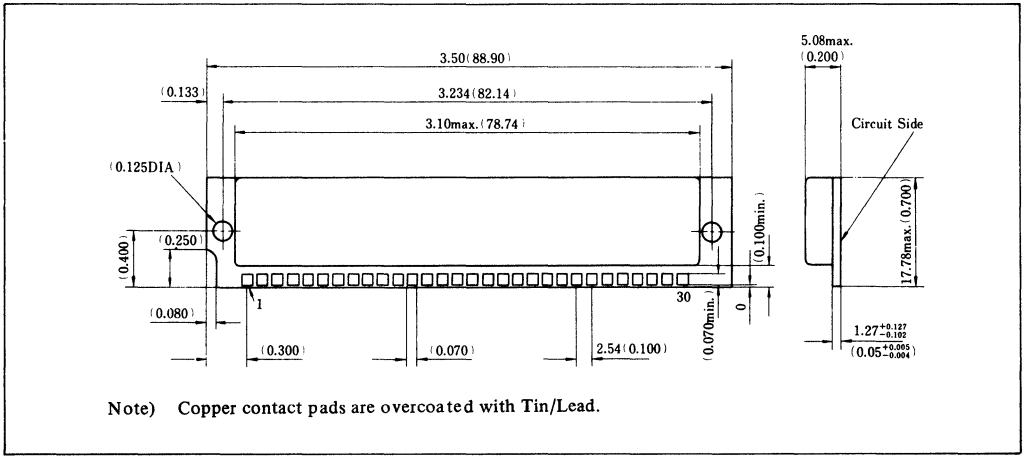


Package Outline; Unit: mm (inch)

HB561409AL Series



HB561409BL Series



Note) Copper contact pads are overcoated with Tin/Lead.

HB561008 Series

262,144-word x 8-bit Dynamic Random Access Memory Module

The HB561008A/AR/B is a 2M dynamic random-access memory module organized as 262,144 x 8 bits in a leadless 30-pin single-in-line package comprising eight HM50256CP, 262,144 x 1 bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on top of a substrate together with decoupling capacitors mounted together with the chip carriers.

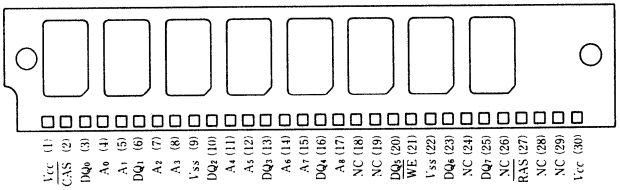
■FEATURES

- 262,144 words 8 bits Organization
- Industry standard 30-Pin Single Inline Package Memory Module
- Single 5V (±10%)
- Utilizes eight 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561008A/AR/B operates as eight HM50256CP as shown in the functional block diagram.
- Low Power; Operating: 1,920mW typ. (t_{RC} = 260ns)
  Standby: 120mW typ.
- High speed:

	Access Time from $\overline{RAS}$ (max)	Access Time from $\overline{CAS}$ (max)	Read or Write Cycle (min)
HB561008A/AR/B-12	120ns	70ns	220ns
HB561008A/AR/B-15	150ns	75ns	260ns
HB561008A/AR/B-20	200ns	100ns	330ns

- Page mode capability
- TTL compatible
- 256 refresh cycles: (4ms)
- 3 variations of refresh
  $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature: 0 to +70°C
- HB561008A/AR . . . . . Leaded type
- HB561008B . . . . Leadless type (socket type)

■PIN ARRANGEMENT



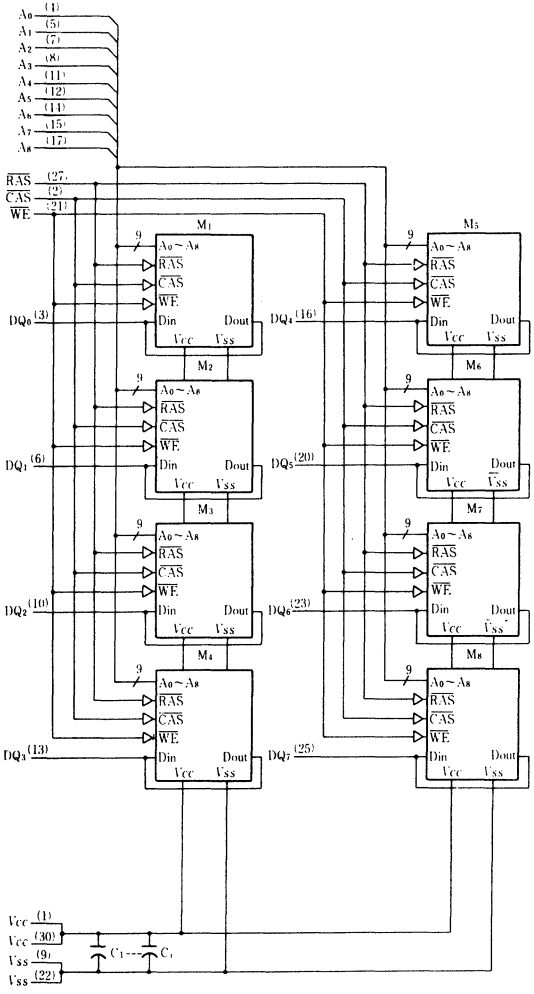
(Side View)

- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operations to prevent contention on D and Q.

■ PIN DESCRIPTION

A0-A8	Address Inputs
$\overline{CAS}$	Column Address Strobes
DQ0-DQ7	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row Address Strobes
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

Voltage on any pin relative to V_{SS}: −1V to +7V
Operating temperature, T_a (Ambient): 0°C to +70°C
Storage temperature (Ambient): −55°C to +125°C
Power dissipation: 8W
Short circuit output current: 50mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V ±10%, V_{SS}=0V)

Parameter	Test Conditions		Symbol	min.	max.	Unit	Notes
Operating current	$\overline{RAS}$, $\overline{CAS}$=cycle t_{RC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC1}		440 560 660	mA	1
Standby current	$\overline{RAS}$=V_{IH}, D_{out}=High Z		I_{CC2}	—	36	mA	
Refresh current	$\overline{RAS}$ only refresh t_{RC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC3}	—	335 425 495	mA	
Standby current	$\overline{RAS}$=V_{IH}, D_{out}=enable		I_{CC5}	—	80	mA	1
Refresh current	$\overline{CAS}$ before $\overline{RAS}$ refresh t_{RC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC6}	—	360 465 550	mA	
Page made supply current	$\overline{RAS}$=V_{IL}, $\overline{CAS}$=cycle, t_{PC}=min	t_{RC}=330ns t_{RC}=260ns t_{RC}=220ns	I_{CC7}	—	295 385 455	mA	
Input leakage	0< V_{in} <7V		I_{LI}	−10	10	μA	
Output leakage	0< V_{out} <7V, D_{out}=disable		I_{LO}	−10	10	μA	
Output levels	High (I_{out}=−5mA)		V_{OH}	2.4	V_{CC}	V	
	Low (I_{out}=4.2mA)		V_{OL}	0	0.4	V	

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	—	55	pF	2
Clocks	C_{I2}	—	70	pF	2, 3
DQ	$C_{I/O}$	—	17	pF	2, 3

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V ±10%, V_{SS}=0V) [1), 10), 11)]

Parameter	Symbol	HB561008-12		HB561008-15		HB561008-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	70	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	2000	150	2000	200	2000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	70	2000	75	2000	100	2000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	35	50	35	75	35	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	70	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	25	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	75	—	100	—	130	—	ns	
Read Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	45	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	95	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	45	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9

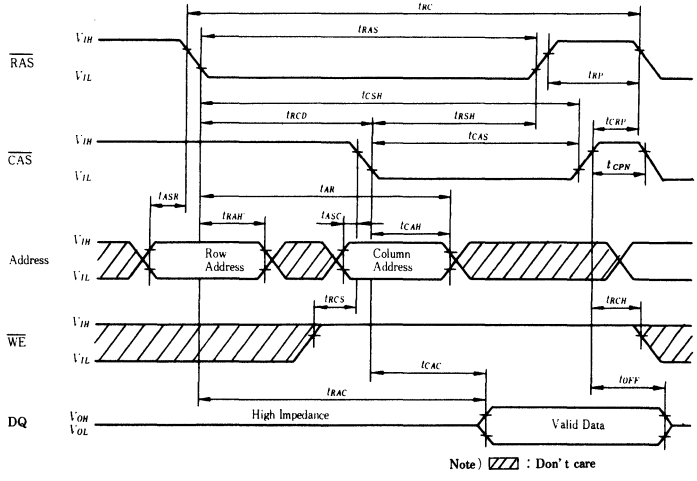
(to be continued)

Parameter	Symbol	HB561008-12		HB561008-15		HB561008-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Data-in Hold Time	t_{DH}	45	–	45	–	55	–	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{CAS}$ Precharge Time	t_{CPN}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Set-up Time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	120	–	150	–	200	–	ns	
$\overline{RAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Page Mode Read or Write Cycle	t_{PC}	130	–	145	–	190	–	ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	50	–	60	–	80	–	ns	

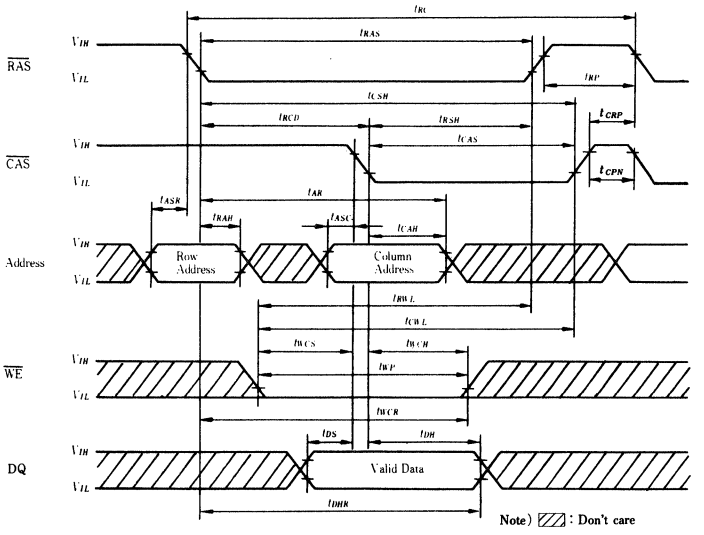
Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
9. These parameters are referenced to $\overline{CAS}$ leading edge.
10. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.
11. At least 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.

■WAVE FORMS

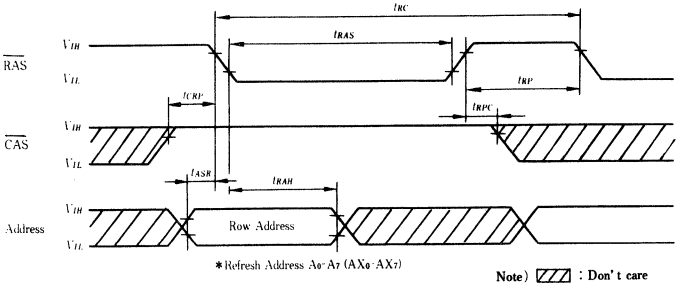
● Read Cycle



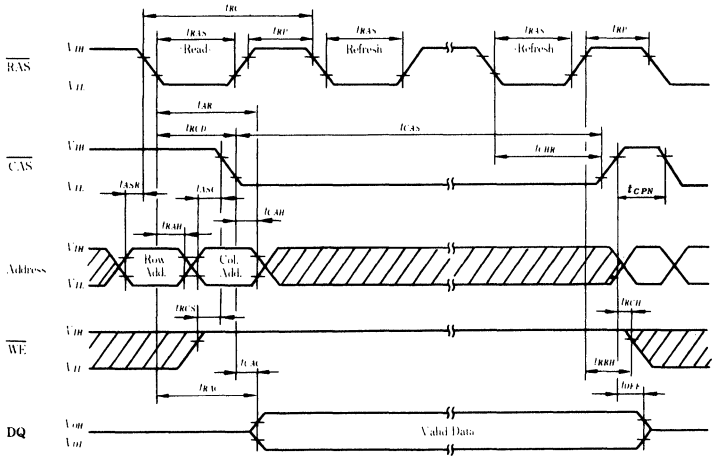
● Write Cycle



● RAS Only Refresh Cycle

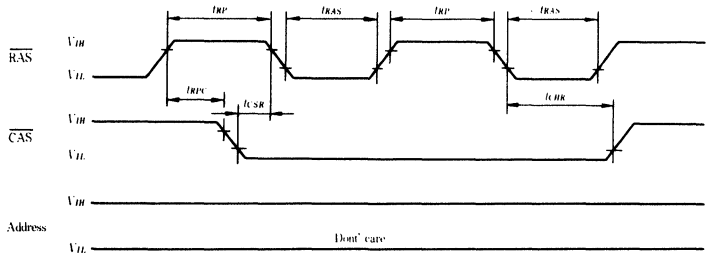


● Hidden Refresh Cycle

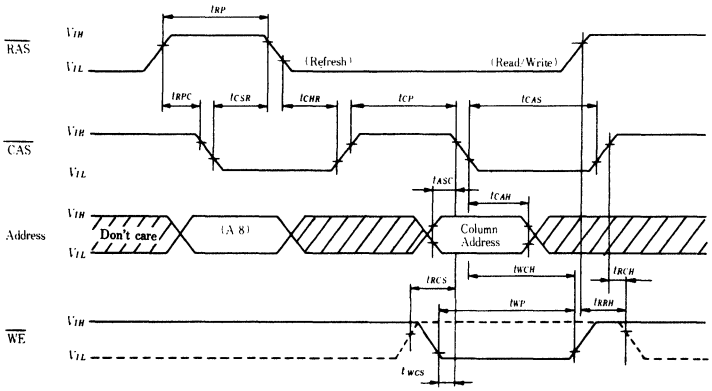


Note) ▨ : Don't care

● $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

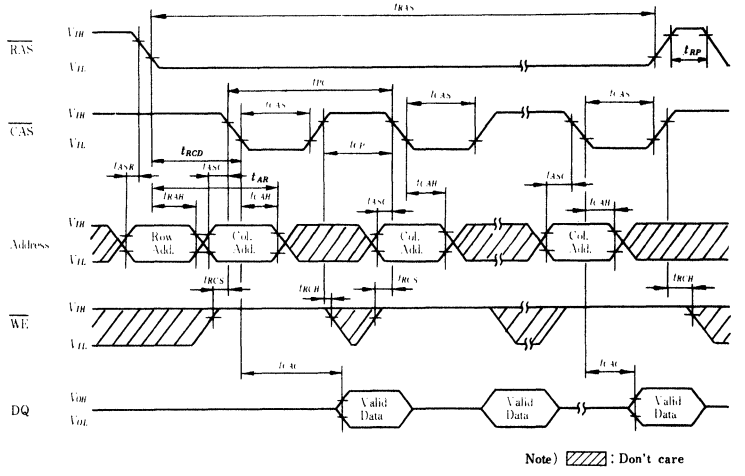


● Counter Test

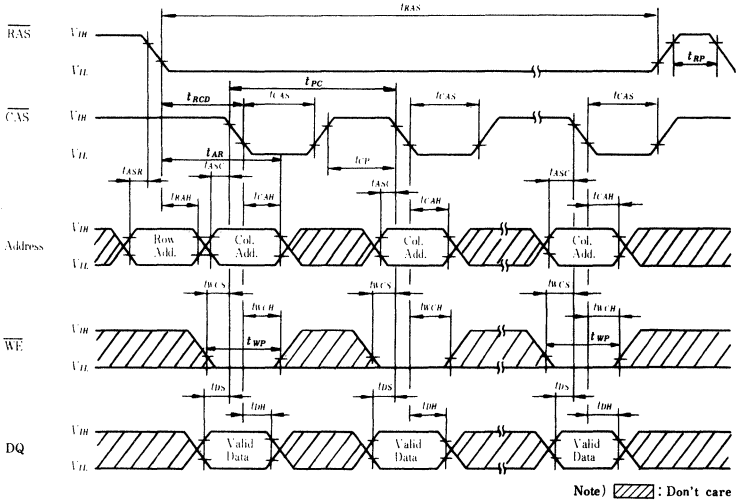


Notes) *1. ▨ : Don't care
*2. Dotted Line Means Read Cycle.

● Page Mode Read Cycle



● Page Mode Write Cycle



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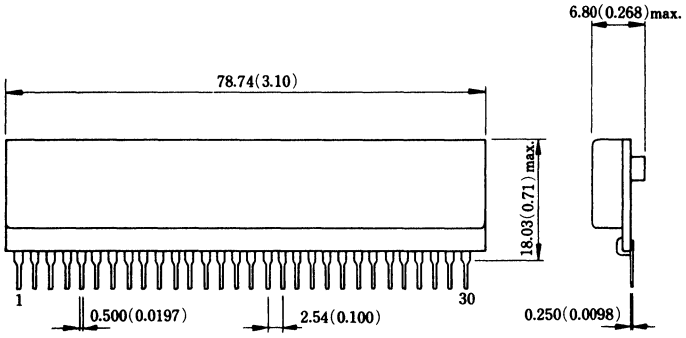
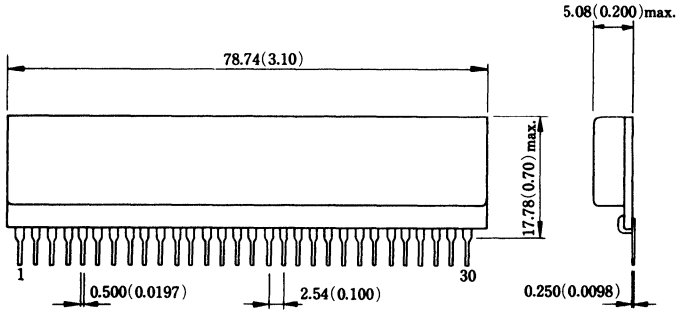
■PACKAGE OUTLINE; Unit: mm (inch)

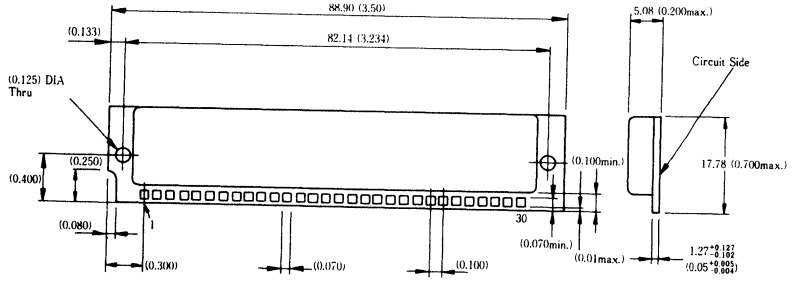
● HB561008A Series



● HB561008AR Series



● HB561008B Series



Unit : mm(inch)

HB56A18 Series

1,048,576 words x 8 bits High Density Dynamic RAM Module

The HB56A18 is a 1M x 8 dynamic RAM module, mounted 8 pieces of 1M-bit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A18 is 30-pin single-in-line package having two types; Lead type (HB56A18A) and Socket type (HB56A18B). Therefore, the HB56A18 makes high density mounting possible without surface mount technology. The HB56A18 provides common data input and output. Its module board has decoupling capacitors to reduce noise.

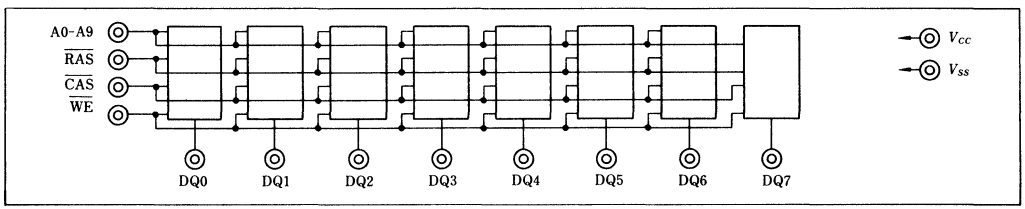
Features

- High Density Industry Standard 30-pin SIP
  Mounting 8 pcs of 1M Dynamic RAM HM511000JP (J-bend SO)
- Single +5V Supply
- High speed;
  Fast Access Time from $\overline{RAS}$ . . 100 ns/120ns/150ns (max.)
  Fast Access Time from $\overline{CAS}$ . . . . . 50ns/60ns/75ns (max.)
  Fast Access Cycle time (Read or Write)
  . . . . . 190ns/220ns/260ns (min.)
- Low Power Operation and Low Power Standby;
  Operation . . . . . 1.4W (typ.)
  Standby . . . . . 20mW (typ.)
- Page Mode Capability
- 3 Variations of Refresh Capability
  $\overline{RAS}$ Only Refresh
  $\overline{CAS}$ before $\overline{RAS}$ Refresh
  Hidden Refresh
- Directly TTL Compatible: All Inputs and Outputs

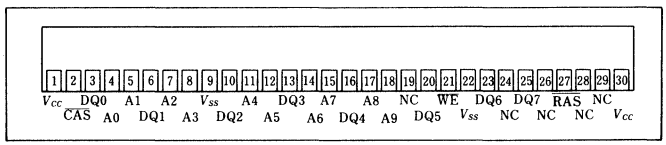
Ordering Information

Type No.	Access time	package
HB56A18A-10	100ns	30-pin SIP Leaded type
HB56A18A-12	120ns	
HB56A18A-15	150ns	
HB56A18B-10	100ns	30-pin SIP Socket type
HB56A18B-12	120ns	
HB56A18B-15	150ns	

Functional Block Diagram



Pin Arrangement



Pin Description

Pin Name	Function
A0-A9	Address
DQ0-DQ7	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
Vcc	Power Supply(+5V)
Vss	GND
Nc	Non Connection

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . −55°C to +125°C
Power dissipation 8W
Short circuit output current 50mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	—	5.5	V	1
Input Low voltage	V_{IL}	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to Vss

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Operating current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	Icc1	—	320 400 480	mA	1
Standby current	Icc2	—	16	mA	TTL Interface
		—	8	mA	CMOS Interface
Refresh current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	Icc3	—	280 320 400	mA	$\overline{RAS}$ only Refresh
Standby current (Dout Enable) $\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL}	Icc5	—	40	mA	1
Refresh current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	Icc6	—	280 320 400	mA	$\overline{CAS}$ before $\overline{RAS}$ Refresh
Page mode current t_{PC} = 105 ns t_{PC} = 85 ns t_{PC} = 70ns	Icc7	—	320 360 400	mA	1
Input leakage 0 < Vin < 7V	I_{LI}	−10	10	μA	
Output leakage 0 < Vout < 7V	I_{LO}	−10	10	μA	Dout is disabled
Output level High Iout = −5 mA	V_{OH}	2.4	Vcc	V	
Output level Low Iout = 4.2 mA	V_{OL}	0	0.4	V	

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Typ	Max	Unit	Notes
Address	C_{I1}	—	55	pF	2
Clocks	C_{I2}	—	70	pF	2,3
Data I/O	$C_{I/O}$	—	17	pF	2,3

Notes) 1. Icc depends on output loading condition when the device is selected. Icc max specified at the output open condition.
2. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable Dout.

Electrical Characteristics and Recommended AC Operating Conditions

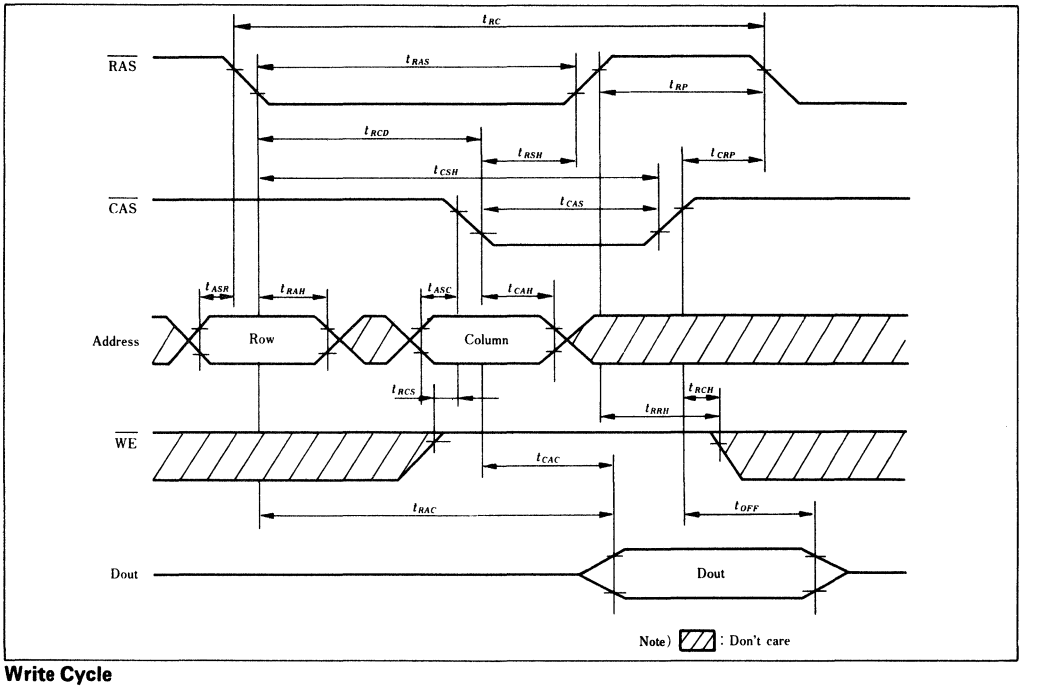
(Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1),9),10)]

Parameter	Symbol	HB56A18-10		HB56A18-12		HB56A18-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	3,4
Output Buffer Turn-off Delay	t_{OFF}	—	25	—	30	—	40	ns	5
Transition Time(rise and fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Read Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{CAS}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
Page Mode Read or Write Cycle	t_{PC}	70	—	85	—	105	—	ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	10	—	15	—	20	—	ns	

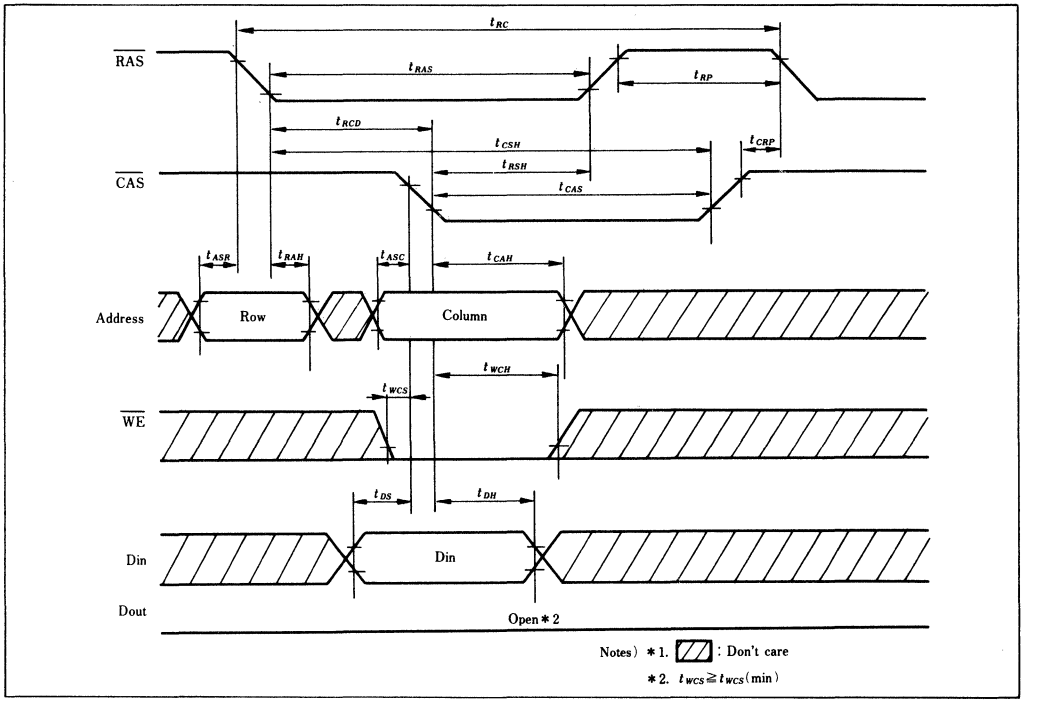
Notes) 1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage level.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures the t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. Early write cycle only $t_{WCS} \geq t_{WCS}$ (min)).
9. An initial pause of 100μs is required after power-up. Then execute at least eight initialization cycles.
10. At least, eight CAS before RAS refresh cycles are required before using the internal refresh counter.

Timing Waveforms

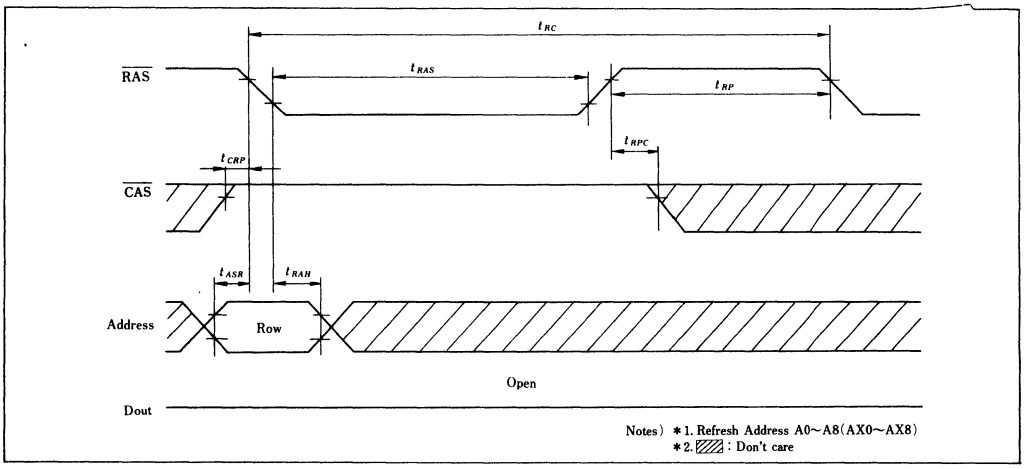
Read Cycle



Write Cycle

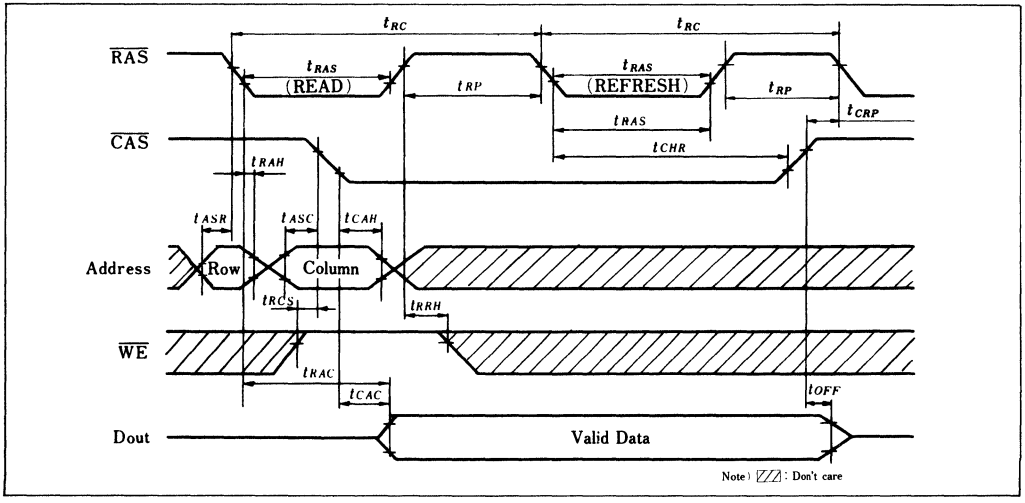


• $\overline{RAS}$ Only Refresh Cycle



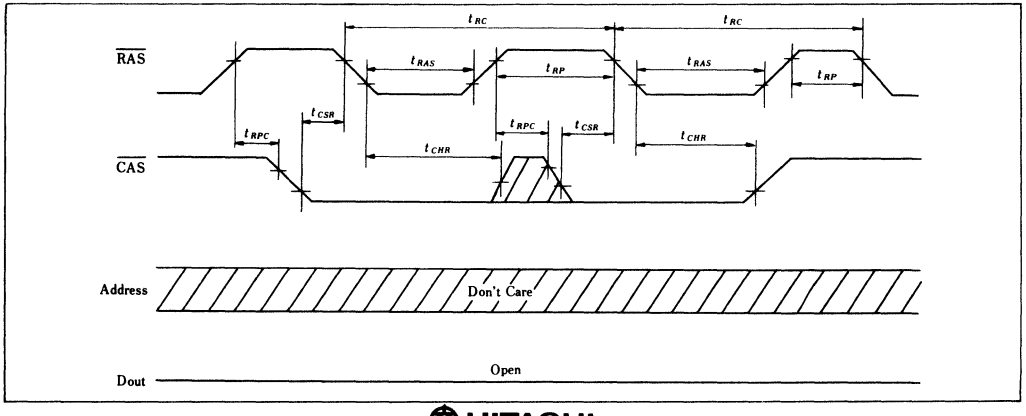
Notes) *1. Refresh Address A0~A8(AX0~AX8)
*2. ▨ : Don't care

• Hidden Refresh Cycle

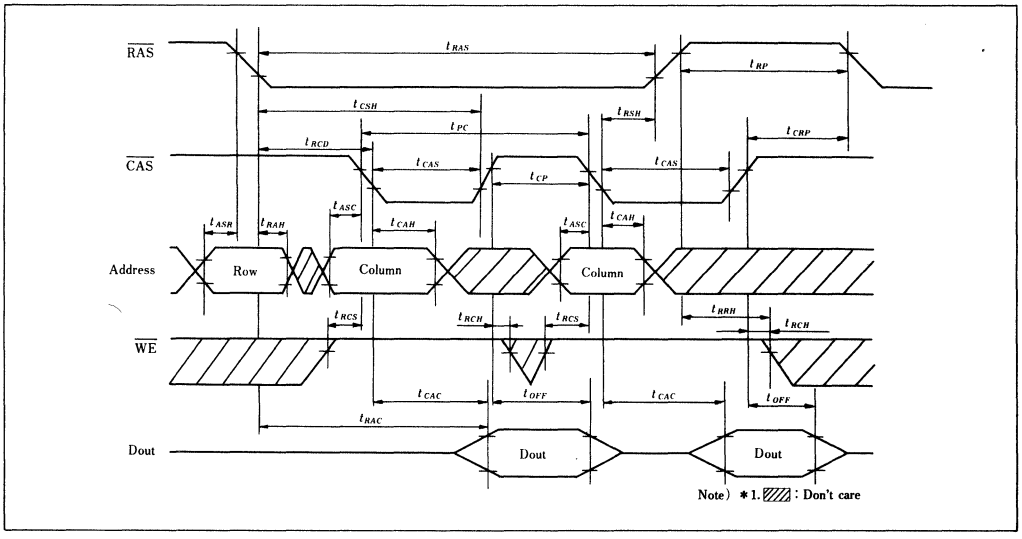


Note) ▨ : Don't care

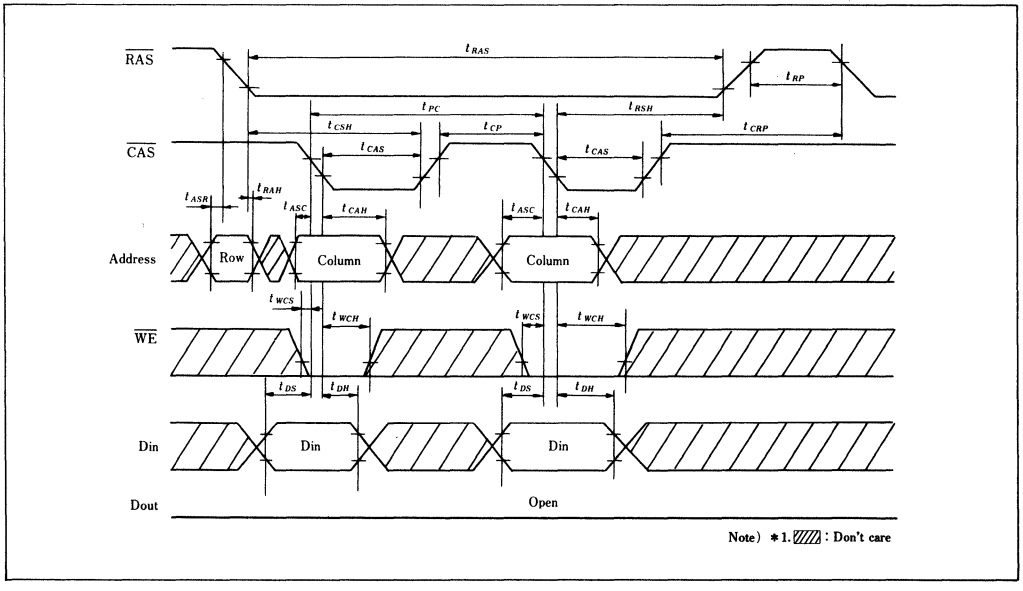
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Page Mode Read Cycle



• Page Mode Write Cycle



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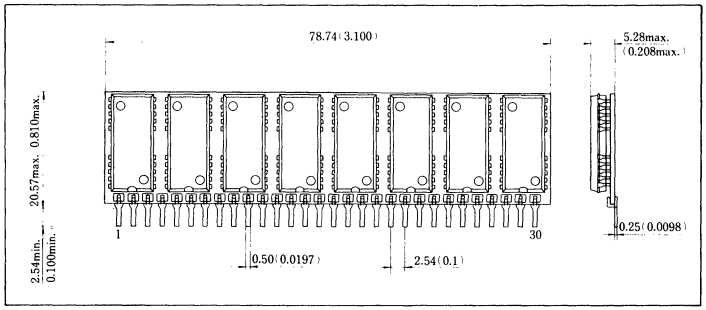
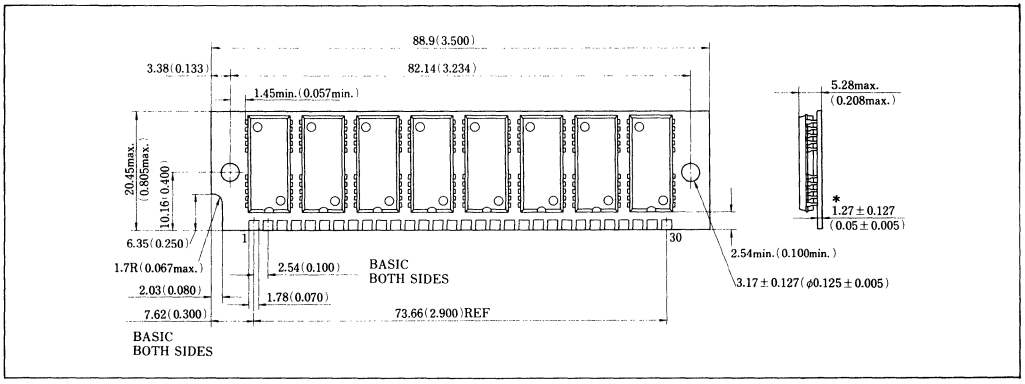
Package Outline, Unit: mm (inch)

HB56A18A Series



Pin No	Name	Pin No	Name
1	*Vcc*	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	*Vss*
8	A3	23	DQ6
9	*Vss*	24	NC
10	DQ2	25	DQ7
11	A4	26	NC
12	A5	27	$\overline{RAS}$
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	*Vcc*

HB56A18B Series



Pin No	Name	Pin No	Name
1	Vcc	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	Vss
8	A3	23	DQ6
9	Vss	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCAS}$
14	A6	29	PD
15	A7	30	Vcc

HB56A19 Series

1,048,576-words x 9 bits High Density Dynamic RAM Module

The HB56A19 is a 1M x 9 dynamic RAM module, mounted 9 pieces of 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A19 is 30-pin single-in-line package having two types; Lead type (HB56A19A) and Socket type (HB56A19B). Therefore, the HB56A19 makes high density mounting possible without surface mount technology. The HB56A19 provides common data input and output, and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors to reduce noise.

Features

- High Density Industry Standard 30-pin SIP
  Mounting 9 pcs of 1M Dynamic RAM HM511000JP (J-bend SO)
- Single +5V Supply
- High speed;
  Fast Access Time from $\overline{RAS}$
  . . . . . 100ns/120ns/150ns (max)
  Fast Access Time from $\overline{CAS}$
  . . . . . 50ns/60ns/75ns (max)
  Fast Access Cycle Time (Read or Write)
  . . . . . 190ns/220ns/260ns (min)
- Low Power Operation and Low Power Standby;
  Operation . . . . . 1.6W (typ)
  Standby . . . . . 22mW (typ)
- Page Mode Capability
- 3 Variations of Refresh Capability
  $\overline{RAS}$ Only Refresh
  $\overline{CAS}$ before $\overline{RAS}$ Refresh
  Hidden Refresh
- Directly TTL Compatible: All Inputs and Outputs

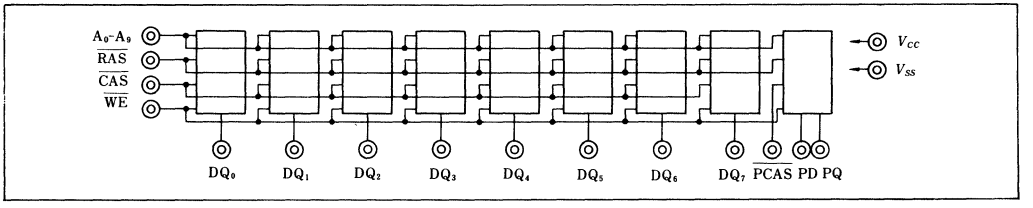
Ordering Information

Type No.	Access time	Package
HB56A19A-10	100ns	30-pin SIP Lead type
HB56A19A-12	120ns	
HB56A19A-15	150ns	
HB56A19B-10	100ns	30-pin SIP Socket type
HB56A19B-12	120ns	
HB56A19B-15	150ns	

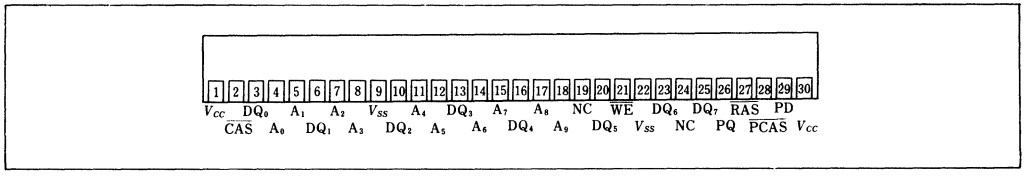
Pin Description

Pin Name	Function
A0-A9	Address
DQ0-DQ7	Data in/Data out
$\overline{CAS}$	Column Address Strobe
$\overline{PCAS}$	$\overline{CAS}$ for parity
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
PD	Data in for parity
PQ	Data out for parity
Vcc	Power Supply(+5V)
Vss	GND
NC	Non Connection

Functional Block Diagram



Pin Arrangement



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . −55°C to +125°C
Power dissipation 9W
Short circuit output current 50mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	—	5.5	V	1
Input Low voltage	V_{IL}	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to Vss

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Operating current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	Icc1	—	 360 450 540	mA	1
Standby current	Icc2	— —	18 9	mA mA	TTL Interface CMOS Interface
Refresh current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	Icc3	—	 315 360 450	mA	$\overline{RAS}$ only Refresh
Standby current (Dout Enable) $\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL}	Icc5	—	45	mA	1
Refresh current t_{RC} = 260 ns t_{RC} = 220 ns t_{RC} = 190 ns	Icc6	—	 315 360 450	mA	$\overline{CAS}$ before $\overline{RAS}$ Refresh
Page mode current t_{PC} = 105 ns t_{PC} = 85 ns t_{PC} = 70ns	Icc7	—	 360 405 450	mA	1
Input leakage 0 < Vin < 7V	I_{LI}	−10	10	μA	
Output leakage 0 < Vout < 7V	I_{LO}	−10	10	μA	Dout is disabled
Output level High Iout = −5 mA	V_{OH}	2.4	Vcc	V	
Output level Low Iout = 4.2 mA	V_{OL}	0	0.4	V	

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Typ	Max	Unit	Notes
Address	C_{I1}	—	60	pF	2
Clocks	C_{I2}	—	75	pF	2,3
Data I/O	$C_{I/O}$	—	17	pF	2,3
Date-in	C_{I3}	—	10	pF	2
Date-out	C_O	—	12	pF	2,3

Notes) 1. Icc depends on output loading condition when the device is selected, Icc max specified at the output open condition.
2. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = VIH to disable Dout.

Electrical Characteristics and Recommended AC Operating Conditions

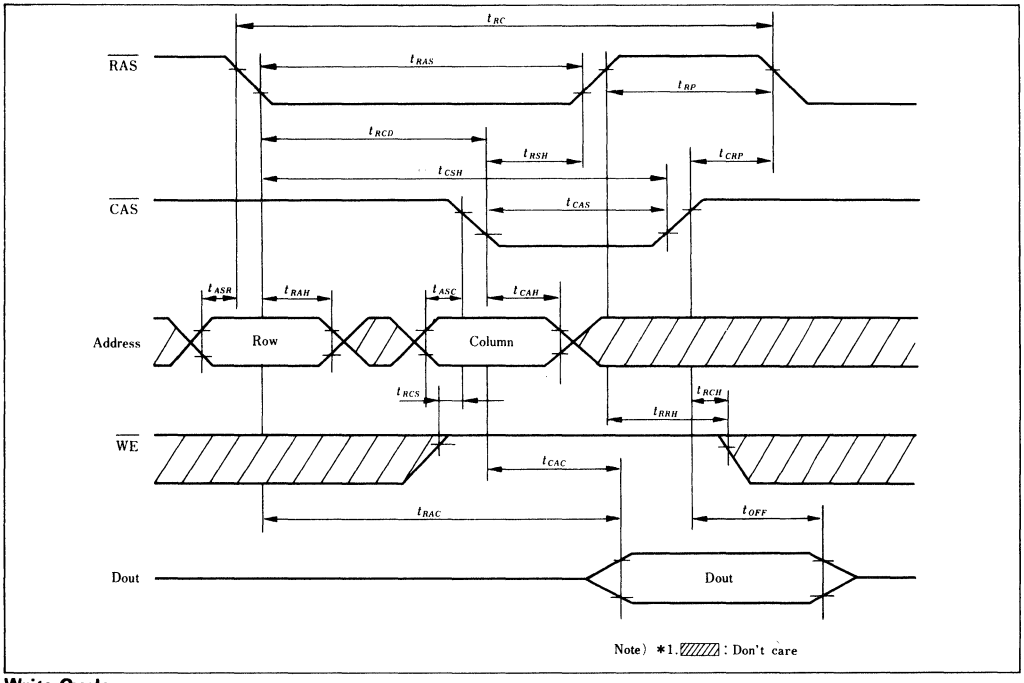
(Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1),9),10)]

Parameter	Symbol	HB56A19-10		HB56A19-12		HB56A19-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	3,4
Output Buffer Turn-off Delay	t_{OFF}	—	25	—	30	—	40	ns	5
Transition Time(rise and fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Read Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{CAS}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
Page Mode Read or Write Cycle	t_{PC}	70	—	85	—	105	—	ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	10	—	15	—	20	—	ns	

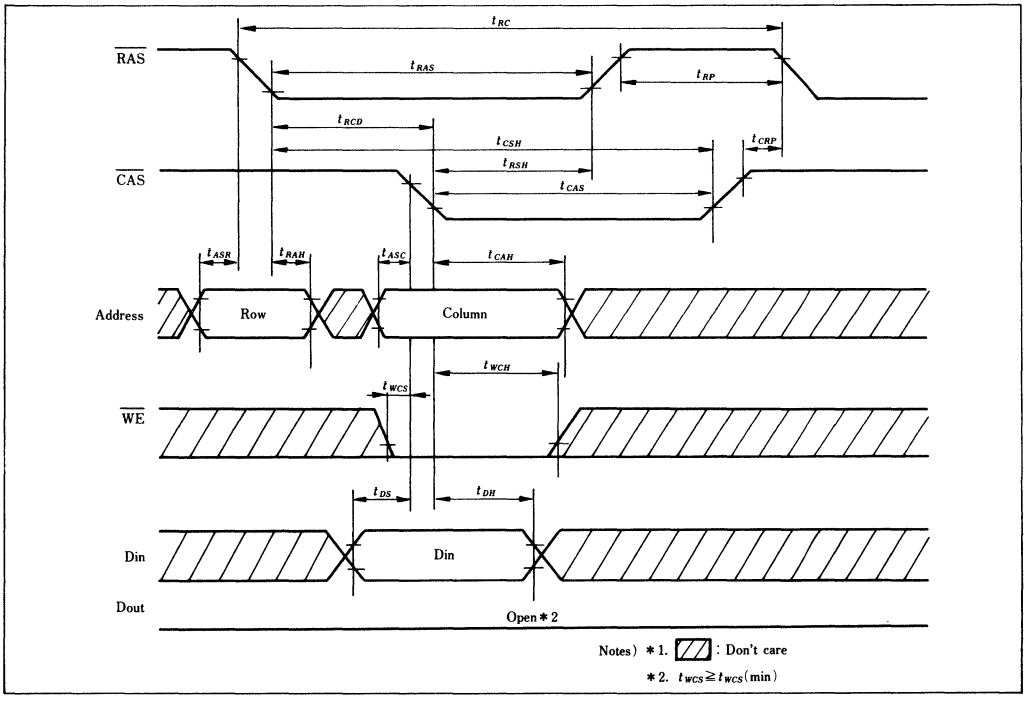
Notes) 1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage level.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures the t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. Early write cycle only $t_{WCS} \geq t_{WCS}$ (min)).
9. An initial pause of 100μs is required after power-up. Then execute at least eight initialization cycles.
10. At least, eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using the internal refresh counter.

Timing Waveforms

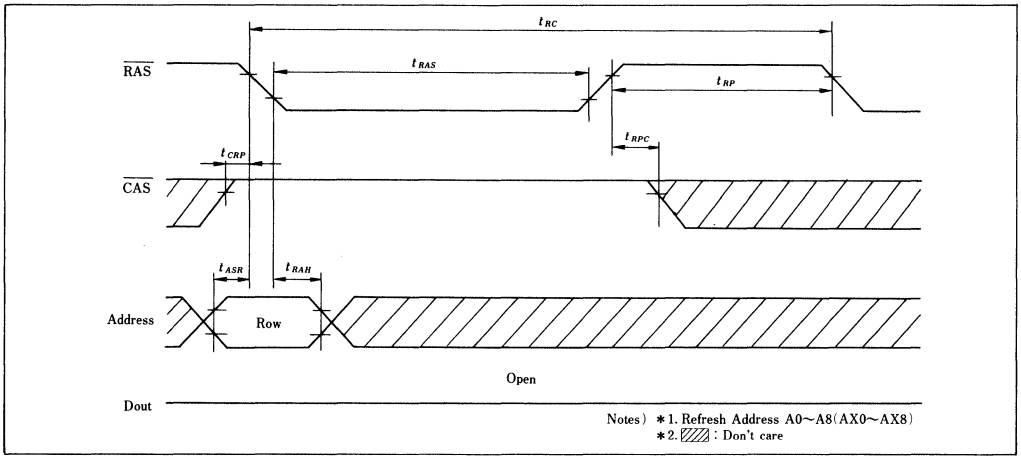
Read Cycle



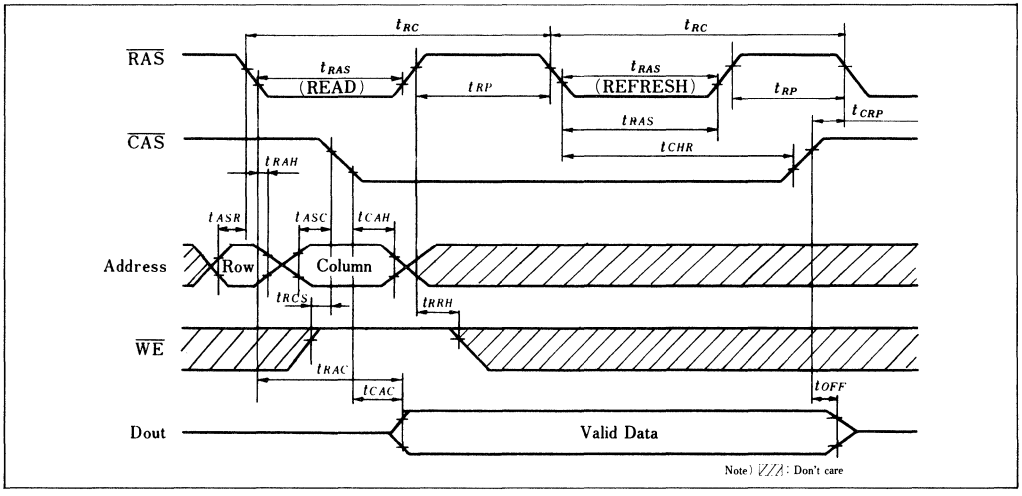
Write Cycle



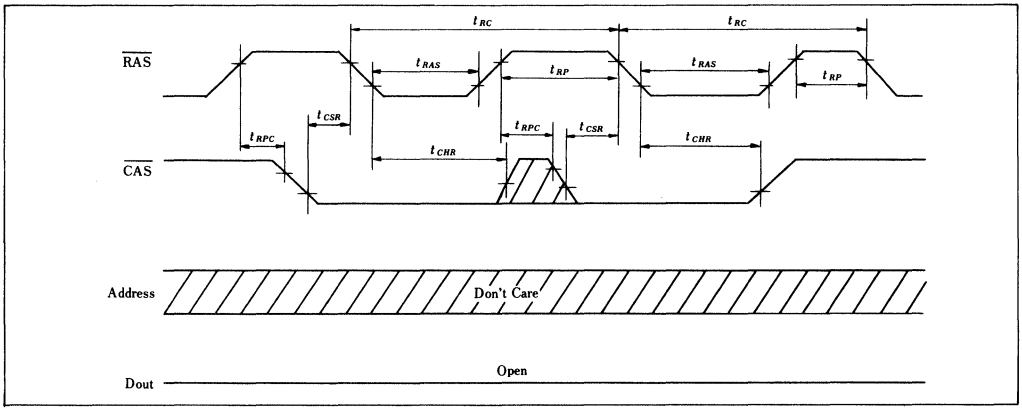
$\overline{RAS}$ Only Refresh Cycle



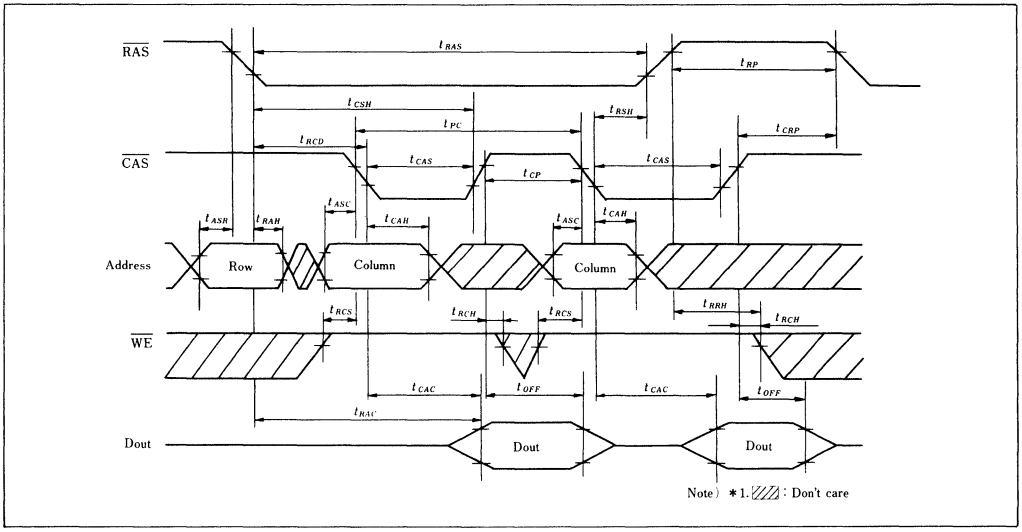
Hidden Refresh Cycle



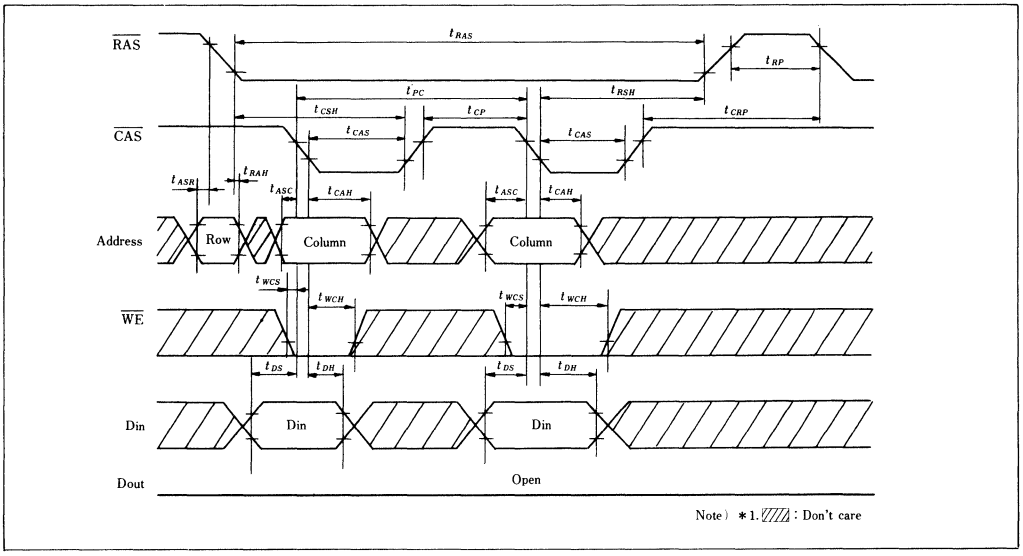
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Page Mode Read Cycle

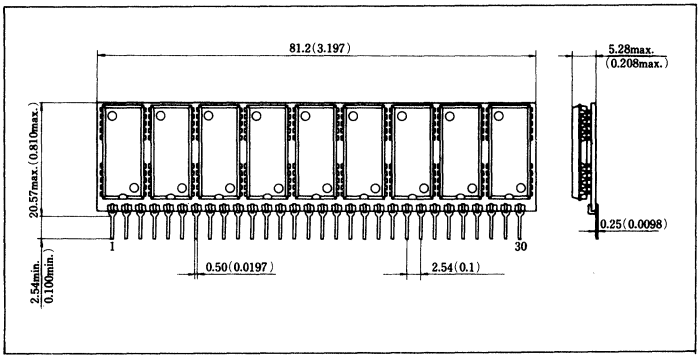


Page Mode Write Cycle



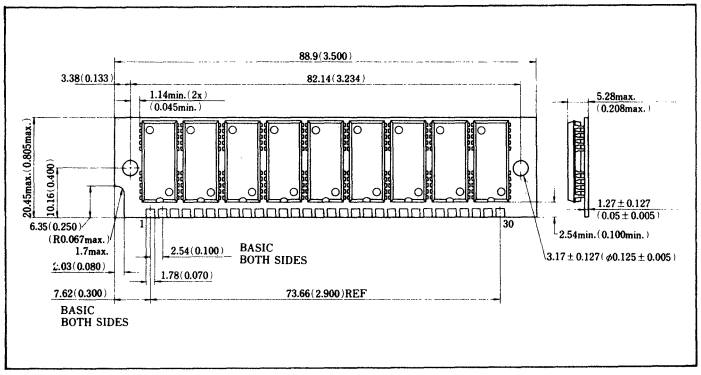
Package Outline, Unit: mm (inch)

HB56A19A Series



Pin No	Name	Pin No	Name
1	Vcc	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	Vss
8	A3	23	DQ6
9	Vss	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCAS}$
14	A6	29	PD
15	A7	30	Vcc

HB56A19B Series



Pin No	Name	Pin No	Name
1	*Vcc*	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	*Vss*
8	A3	23	DQ6
9	*Vss*	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCAS}$
14	A6	29	PD
15	A7	30	*Vcc*

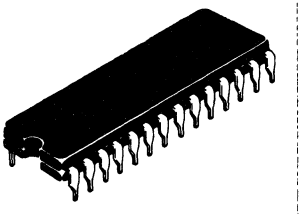
MOS MASK ROM

HN623257P, HN623257F

32768-word x 8-bit CMOS Mask Programmable Read Only Memory

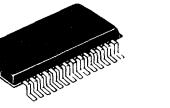
The HN623257P/F is a 256-kbit CMOS mask-programmable ROM organized as 32768 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

HN623257P



(DP-28)

HN623257F

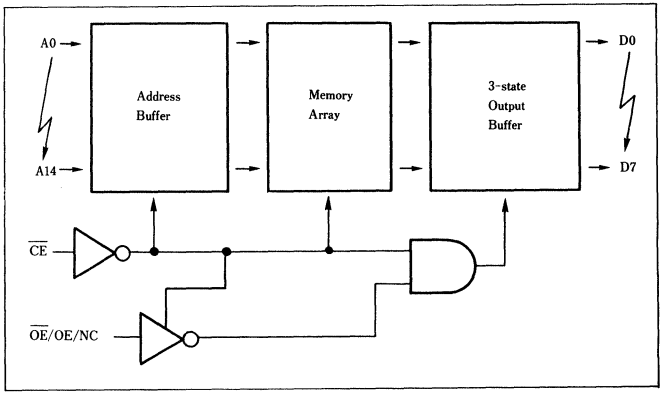


(FP-28D)

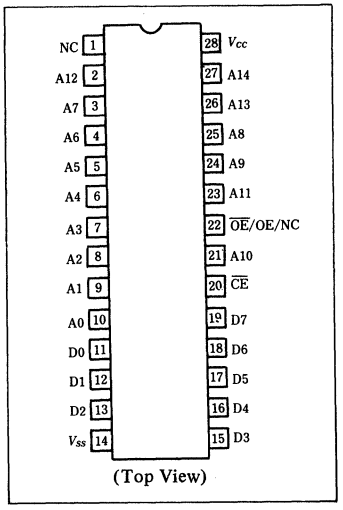
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time: 150ns (Max.)
- Low Power Consumption: 100mW (typ.) active
  5μW (typ.) standby
- Byte-Wide Data Organization

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage*1	Vcc	−0.3 to +7.0	V
All Input or Output Voltage*1	VT	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	−20 to +75	℃
Storage Temperature Range	Tstg	−55 to +125	℃
Temperature Under Bias	Tbias	−20 to +85	℃

Note) *1. With respect to Vss.

Recommended Operating Conditions (V_{SS} = 0V, Ta = –20 to +75°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = –20 to +75°C)

Item		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	45	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
	Standby	I_{SB}	—	30	μA	V_{CC}=5.5V, $\overline{CE} \geqq V_{CC}-0.2V$
Input Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	Vin=0 to 5.5V
Output Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	I_{OH}=−205μA
		V_{OL}	—	0.4	V	I_{OL}=3.2mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Item	Symbol	min	max	Unit
Input Capacitance	Cin	—	10	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics

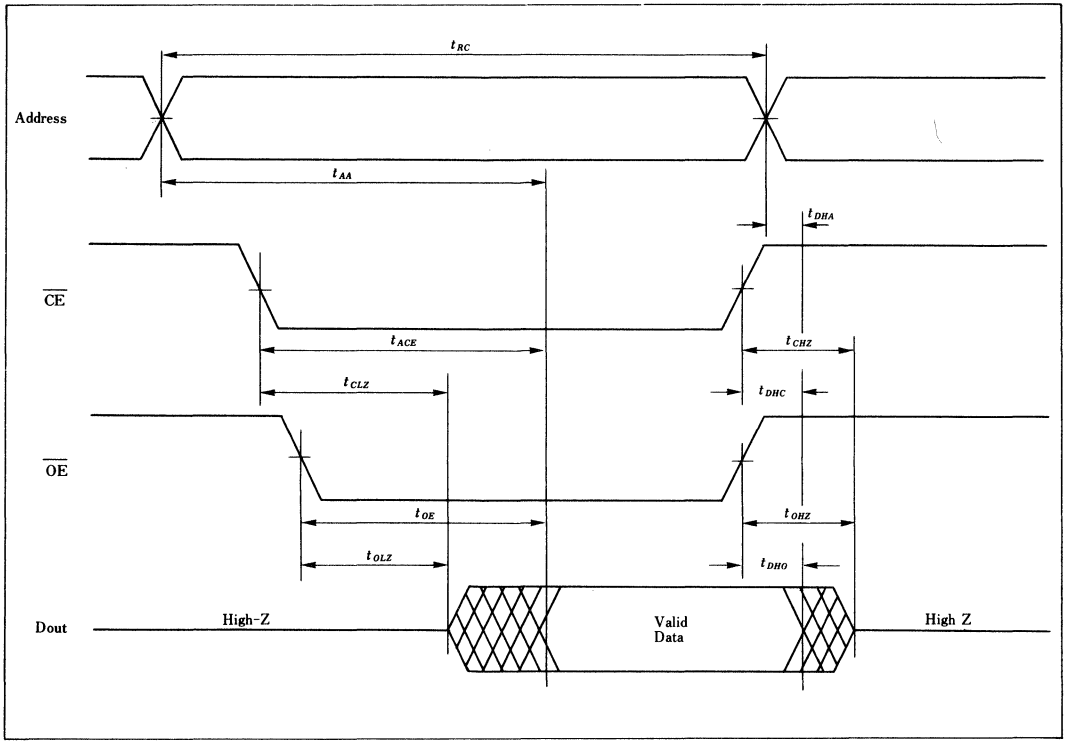
(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = –20 to +75°C)

- Input Pulse Level . . . . . 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load . . . . . 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	150	—	ns
Address Access Time	t_{AA}	—	150	ns
$\overline{CE}$ Access Time	t_{ACE}	—	150	ns
Data Setup Time $\overline{CE}$	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Data Hold Time from $\overline{CE}$*1	t_{CHZ}	—	70	ns
Output Hold Time $\overline{CE}$	t_{DHC}	0	—	ns
OE Access Time	t_{OE}	—	70	ns
Data Setup Time OE	t_{OLZ}	10	—	ns
Data Hold Time from OE*1	t_{OHZ}	—	70	ns
Output Hold Time from OE	t_{DHO}	0	—	ns

Note) *1. t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Diagram

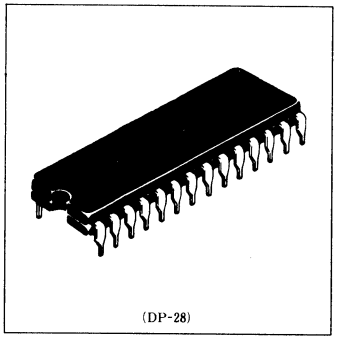


Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA}, t_{DHC} or t_{DHO}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA}, t_{ACE} or t_{OE}, whichever occurs last.
3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ}, whichever occurs last.

HN62321P

131072-word x 8-bit CMOS Mask Programmable Read Only Memory

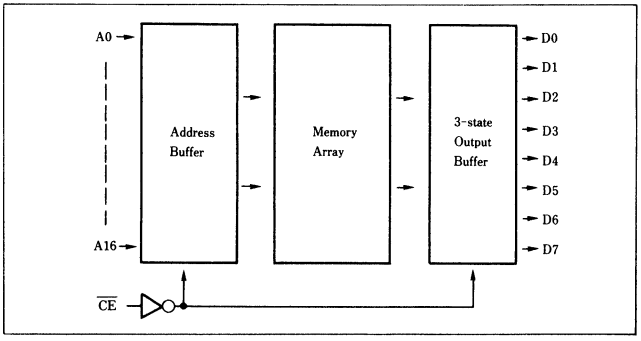
The HN62321P is a 1-Mbit CMOS mask-programmable ROM organized as 131072 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62321P, which provides large capacity of 1M bits, is ideally suited for kanji character generators.


(DP-28)

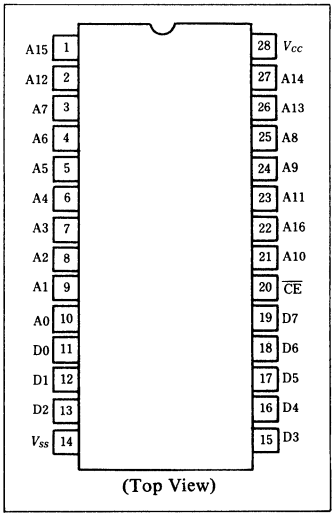
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . 150ns (max.)
- Low Power Consumption . . . . . 100mW (typ.) active
  5μW (typ.) standby
- Byte-Wide Data Organization

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage*1	Vcc	−0.3 to +7.0	V
All Input or Output Voltage*1	V_T	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	0 to +70	℃
Storage Temperature Range	Tstg	−55 to +125	℃
Temperature Under Bias	Tbias	−20 to +85	℃

Note) *1. With respect to Vss.

Recommended Operating Conditions
(V_{SS} = 0V, Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Item		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	50	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
	Standby	I_{SB}	—	30	μA	V_{CC}=5.5V, $\overline{CE} \geqq V_{CC}-0.2V$
Input Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	Vin=0 to 5.5V
Output Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	I_{OH}=−205μA
		V_{OL}	—	0.4	V	I_{OL}=3.2mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Item	Symbol	min	max	Unit
Input Capacitance	Cin	—	10	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

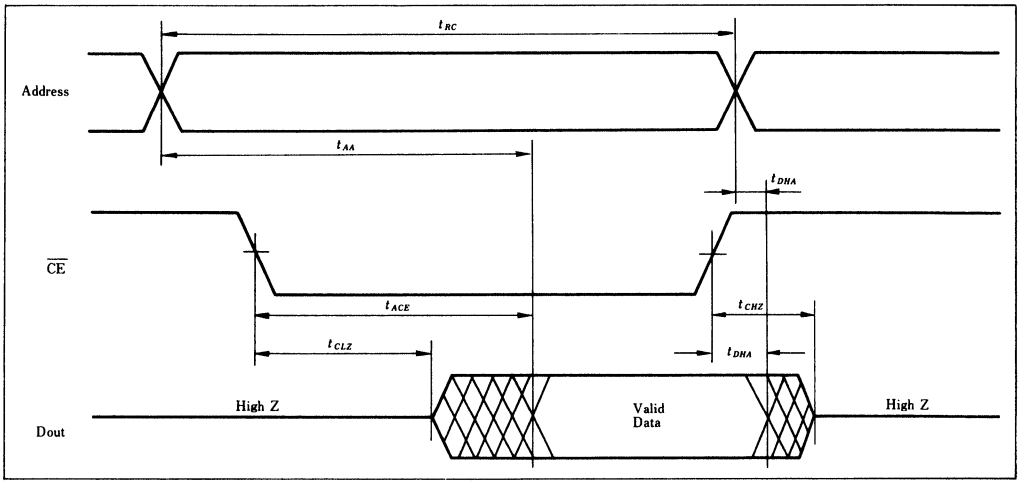
AC Electrical Characteristics
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

- Input Pulse Level . . . . . 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load . . . . . 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	150	—	ns
Address Access Time	t_{AA}	—	150	ns
$\overline{CE}$ Access Time	t_{ACE}	—	150	ns
Data Setup Time $\overline{CE}$	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Data Hold Time from $\overline{CE}$ *1	t_{CHZ}	—	70	ns
Output Hold Time $\overline{CE}$	t_{DHC}	0	—	ns

Note) *1. t_{CHZ} and t_{OHZ} defines the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Diagram

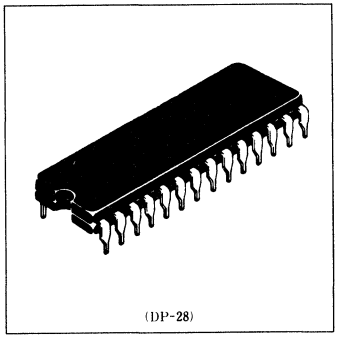


Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA} or t_{DHC}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA} or t_{ACE}, whichever occurs last.

HN62321BP

131072-word x 8-bit CMOS Mask Programmable Read Only Memory

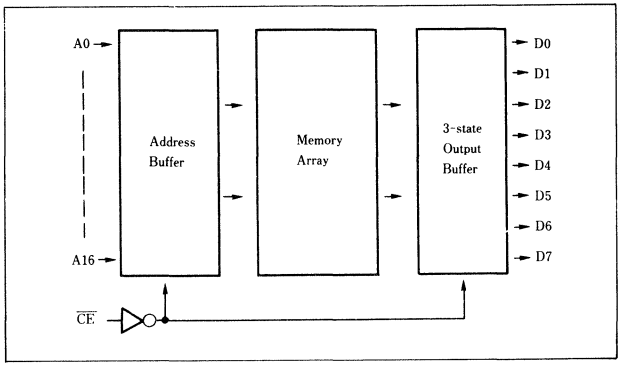
The HN62321BP is a 1-Mbit CMOS mask-programmable ROM organized as 131072 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62321BP, which provides large capacity of 1M bits, is ideally suited for kanji character generators.



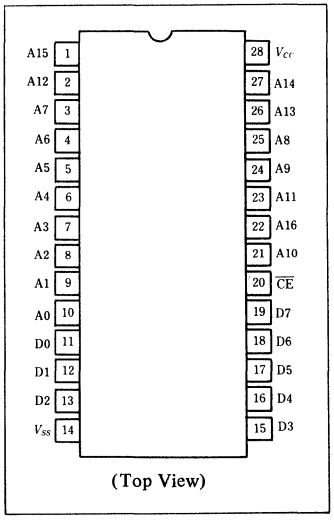
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . 200ns (max.)
- Low Power Consumption . . . . . 100mW (typ.) active
  5μW (typ.) standby
- Byte-Wide Data Organization

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage *1	V_{CC}	−0.3 to +7.0	V
All Input or Output Voltage *1	V_T	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	0 to +70	℃
Storage Temperature Range	Tstg	−55 to +125	℃
Temperature Under Bias	Tbias	−20 to +85	℃

Note) *1. With respect to Vss.

Recommended Operating Conditions

(V_{SS} = 0V, Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Item		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5V, I_{DOUT} = 0mA, t_{RC} = min
	Standby	I_{SB}	—	30	μA	V_{CC} = 5.5V, $\overline{CE} \geqq V_{CC} - 0.2V$
Input Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	Vin = 0 to 5.5V
Output Leakage Current		$\lvert I_{LO} \rvert$	—	10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	I_{OH} = −205μA
		V_{OL}	—	0.4	V	I_{OL} = 3.2mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Item	Symbol	min	max	Unit
Input Capacitance	Cin	—	10	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics

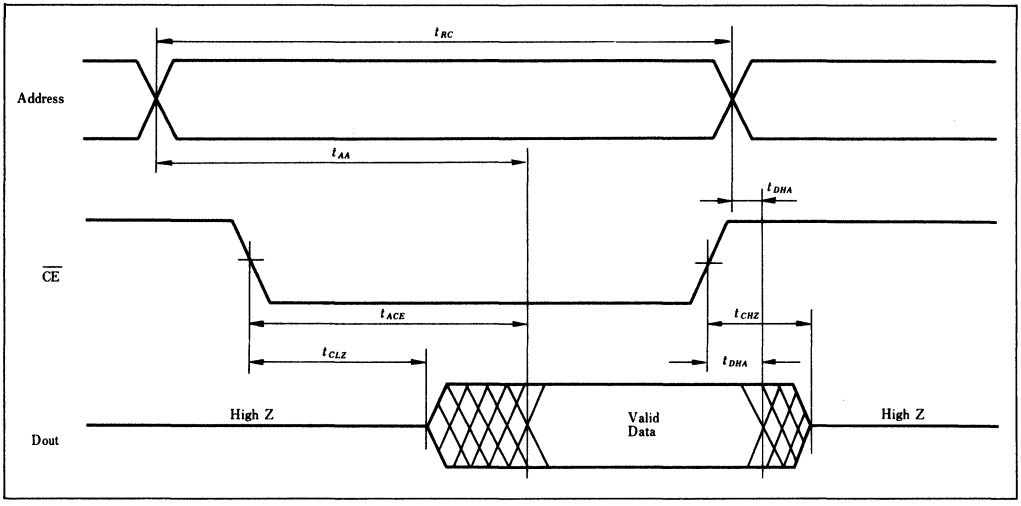
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

- Input Pulse Level . . . . . 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load . . . . . 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
$\overline{CE}$ Access Time	t_{ACE}	—	200	ns
Data Setup Time $\overline{CE}$	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Data Hold Time from $\overline{CE}$ *1	t_{CHZ}	—	100	ns
Output Hold Time $\overline{CE}$	t_{DHC}	0	—	ns

Note) *1. t_{CHZ} defines the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Diagram

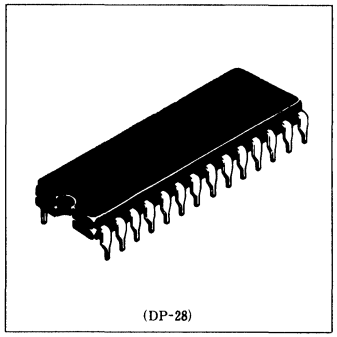


Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA} or t_{DHC}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA} or t_{ACE}, whichever occurs last.

HN62321EP

131072-word x 8-bit CMOS Mask Programmable Read Only Memory

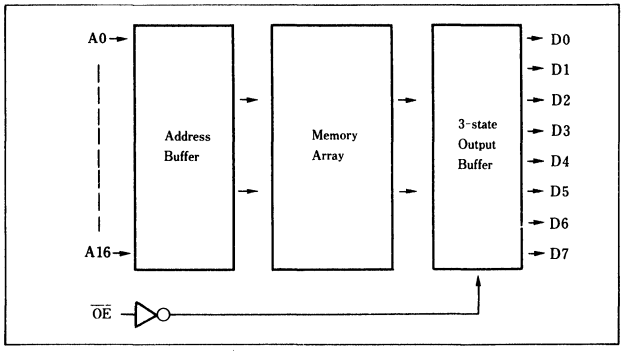
The HN62321EP is a 1-Mbit CMOS mask-programmable ROM organized as 131072 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62321EP, which provides large capacity of 1M bits, is ideally suited for kanji character generators.



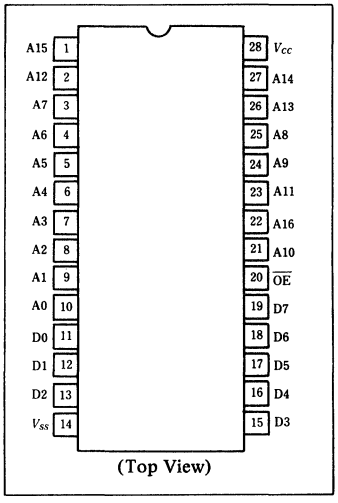
■ FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time . . . . . 200ns (max.)
- Low Power Consumption . . . . . 100mW (typ.)
- Byte-Wide Data Organization
- $\overline{OE}$ Access Time . . . . . 100ns (max.)

Block Diagram



Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	−0.3 to +7.0	V
All Input or Output Voltage*1	V_T	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	0 to +70	℃
Storage Temperature Range	Tstg	−55 to +125	℃
Temperature Under Bias	Tbias	−20 to +85	℃

Note) *1. With respect to Vss.

Recommended Operating Conditions

(V_{SS} = 0V, Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
	V_{IL}	−0.3	–	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Item	Symbol	min	max	Unit	Test Condition
Supply Current	I_{CC}	–	50	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
Input Leakage Current	$\|I_{LI}\|$	–	10	μA	Vin=0 to 5.5V
Output Leakage Current	$\|I_{LO}\|$	–	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage	V_{OH}	2.4	–	V	I_{OH}=−205μA
	V_{OL}	–	0.4	V	I_{OL}=3.2mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Item	Symbol	min	max	Unit
Input Capacitance	Cin	–	10	pF
Output Capacitance	Cout	–	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics

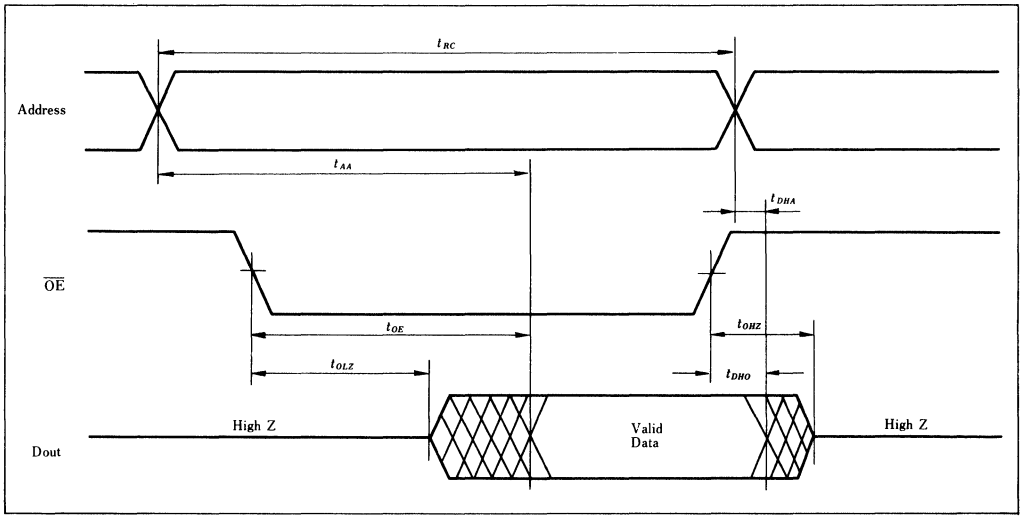
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

- Input Pulse Level ..... 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load ..... 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
$\overline{CE}$ Access Time	t_{OE}	—	100	ns
Data Setup Time $\overline{OE}$	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Data Hold Time from $\overline{OE}$ *1	t_{OHZ}	—	100	ns
Output Hold Time $\overline{OE}$	t_{DHO}	0	—	ns

Note) *1. t_{OHZ} defines the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Diagram

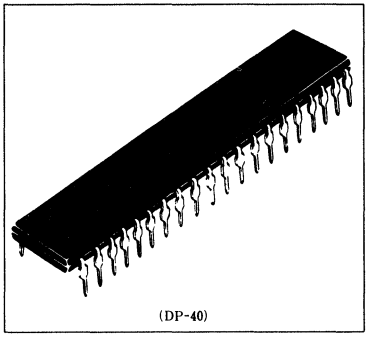


Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA} or t_{DHO}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA} or t_{OE}, whichever occurs last.

HN62412P

131072-word x 16-bit/262144-word x 8-bit CMOS Mask Programmable Read Only Memory

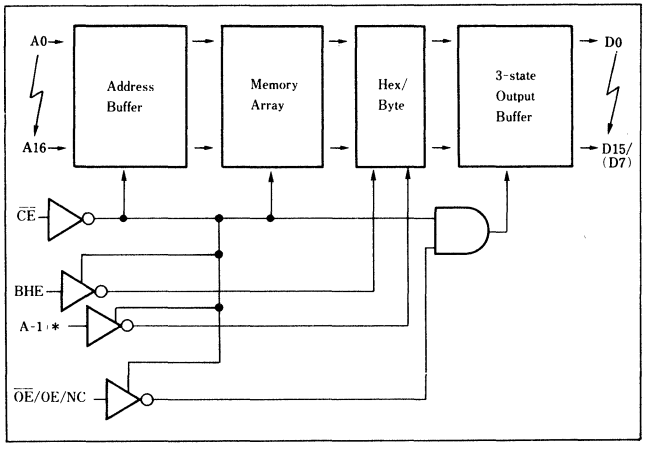
The HN62412P is a 2-Mbit CMOS mask-programmable ROM organized either as 131072 words by 16 bits or as 262144 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62412P, which provides large capacity of 2M bits, is ideally suited for kanji character generators.


(DP-40)

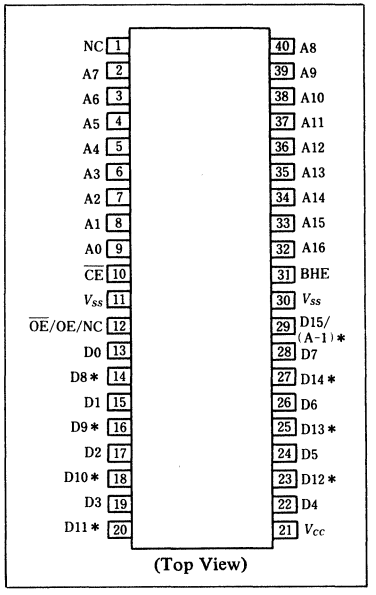
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Comatible
- Maximum Access time: 200ns (max.)
- Low Power Consumption: ..... 100mW (typ.) active
  5μW (typ.) standby
- Byte-Wide or Word-Wide Data Organization with BHE

Block Diagram



Pin Arrangement



(Top View)

BHE = V_{IH}; 16-bit (D15 – D0)
BHE = V_{IL}; 8-bit (D7 – D0)

* A-1 is least significant address.
When BHE is 'low', D14 – D8 goes the high impedance state.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	−0.3 to +7.0	V
All Input or Output Voltage*1	V_T	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	0 to +70	℃
Storage Temperature Range	Tstg	−55 to +125	℃
Temperature Under Bias	Tbias	−20 to +85	℃

Note) *1. With respect to Vss.

Recommended Operating Conditions

(V_{SS} = 0V, Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Item		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	50	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
	Standby	I_{SB}	—	30	μA	V_{CC}=5.5V, $\overline{CE} \geqq V_{CC}-0.2V$
Input Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	Vin=0 to 5.5V
Output Leakage Current		$\lvert I_{LO} \rvert$	—	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	I_{OH}=−205μA
		V_{OL}	—	0.4	V	I_{OL}=1.6mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Item	Symbol	min	max	Unit
Input Capacitance	Cin	—	15	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics

(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

- Input Pulse Level . . . . . 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall time 10ns
- Output Load . . . . . 1 TTL gate + C_L = 100pF (including jig capacitance)

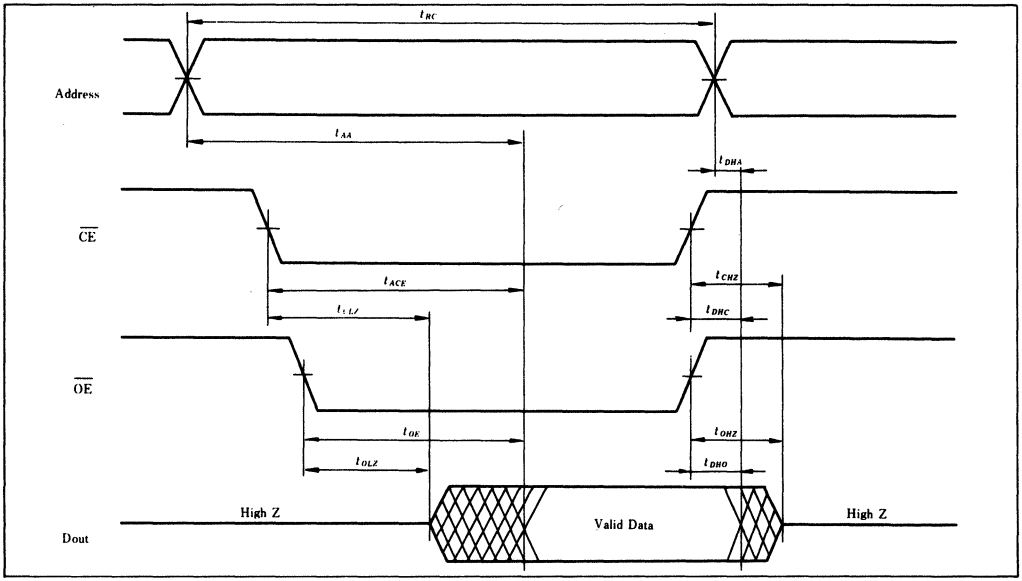
Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
$\overline{CE}$ Access Time	t_{ACE}	—	200	ns
OE Access Time	t_{OE}	—	70	ns
BHE Access Time	t_{BHE}	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time from OE	t_{DHO}	0	—	ns
Output Hold Time from BHE	t_{DHB}	0	—	ns
Data Hold Time from $\overline{CE}$	t_{CHZ}*	—	70	ns
Data Hold Time from OE**	t_{OHZ}*	—	70	ns
Data Hold Time from BHE	t_{BHZ}*	—	70	ns
Data Setup Time from $\overline{CE}$	t_{CLZ}	10	—	ns
Data Setup Time from OE	t_{OLZ}	10	—	ns
Data Setup Time from BHE	t_{BLZ}	10	—	ns

Note) *1. t_{CHZ} and t_{OHZ} and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

***2. In the case of $\overline{OE}$ pin being non-connected, this item is not applied.**

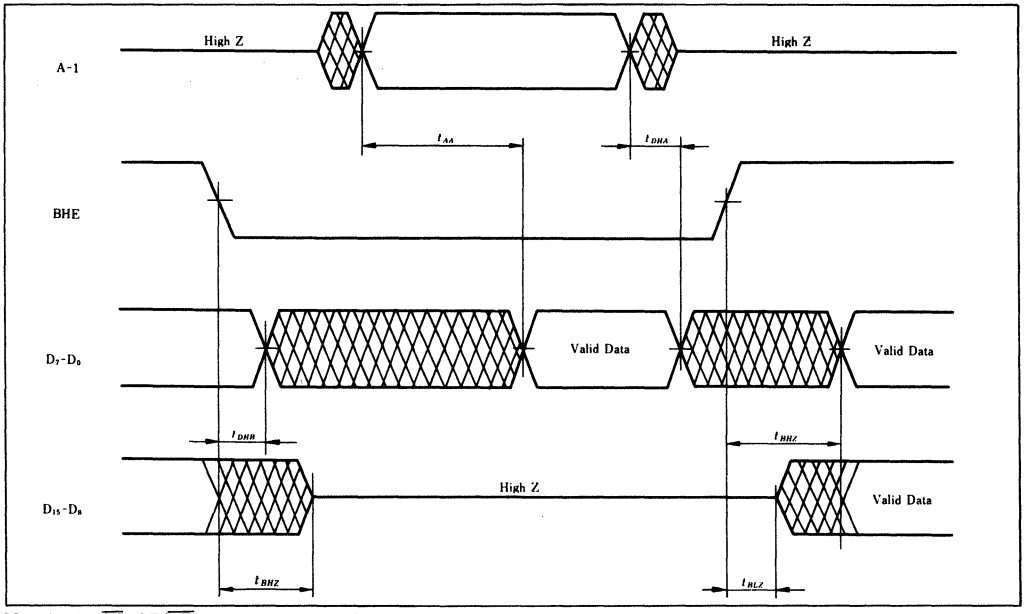
Timing Diagram

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA}, t_{DHC} or t_{DHO}, whichever occurs. first.
2. The time at which the data output becomes valid is defined by t_{AA}, t_{ACE} or t_{OH}, whichever occurs last.
3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ}, whichever occurs last.

Word Mode, Byte Mode Switch

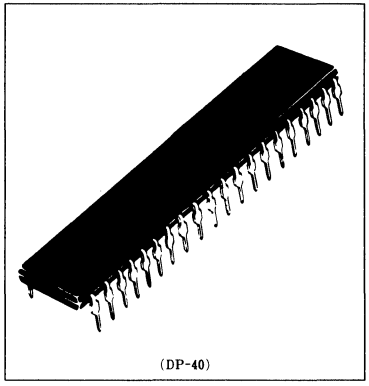


Notes) 1. $\overline{CE}$, OE/$\overline{OE}$ is enable, A16 – A0 is valid.
2. If BHE is high and $\overline{CE}$, $\overline{OE}$ is enable D15/A-1 pin is in the output state.
Therefore, the input signals of opposite phase to the outputs must not be applied to them.

HN62404P

262144-word x 16-bit/524288-word x 8-bit CMOS Mask Programmable Read Only Memory

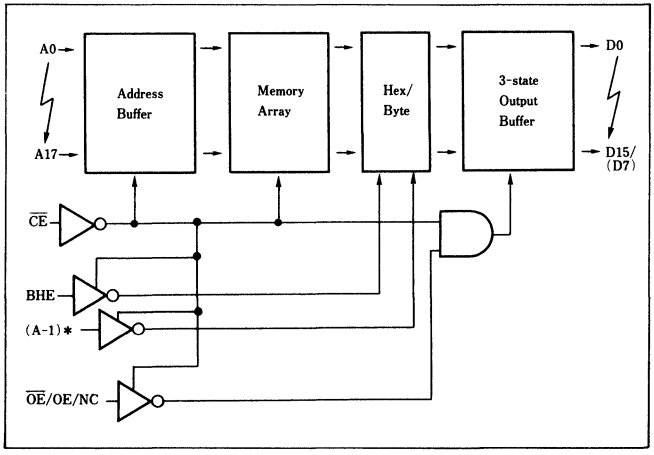
The HN62404P is a 4-Mbit CMOS mask-programmable ROM organized either as 262144 words by 16 bits or as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62404P, which provides large capacity of 4M bits, is ideally suited for kanji character generators.



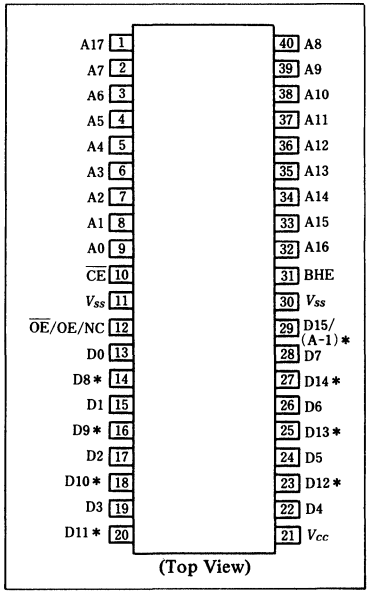
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time: 200ns (max.)
- Low Power Consumption . . . . . 100mW (typ.) active
  5μW (typ.) standby
- Byte-wide or Word-wide Data Organization with B_{HE}

Block Diagram



Pin Arrangement



BHE = V_{IH}; 16-bit (D15 – D0)
BHE = V_{IL}; 8-bit (D7 – D0)

* A-1 is least significant address. When BHE is 'low', D14 – D8 goes the high impedance state.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	−0.3 to +7.0	V
All Input or Output Voltage*1	V_T	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tstg	−55 to +125	°C
Temperature Under Bias	Tbias	−20 to +85	°C

Note) *1. With respect to Vss.

Recommended Operating Conditions
(V_{SS} = 0V, Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Item		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	50	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
	Standby	I_{SB}	—	30	μA	V_{CC}=5.5V, $\overline{CE} \geqq V_{CC}-0.2V$
Input Leakage Current		$\lvert I_{LI} \rvert$	—	10	μA	Vin=0 to 5.5V
Output Leakage Current		$\lvert I_{LO} \rvert$	—	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	I_{OH}=−205μA
		V_{OL}	—	0.4	V	I_{OL}=1.6mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Item	Symbol	min	max	Unit
Input Capacitance	Cin	—	15	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

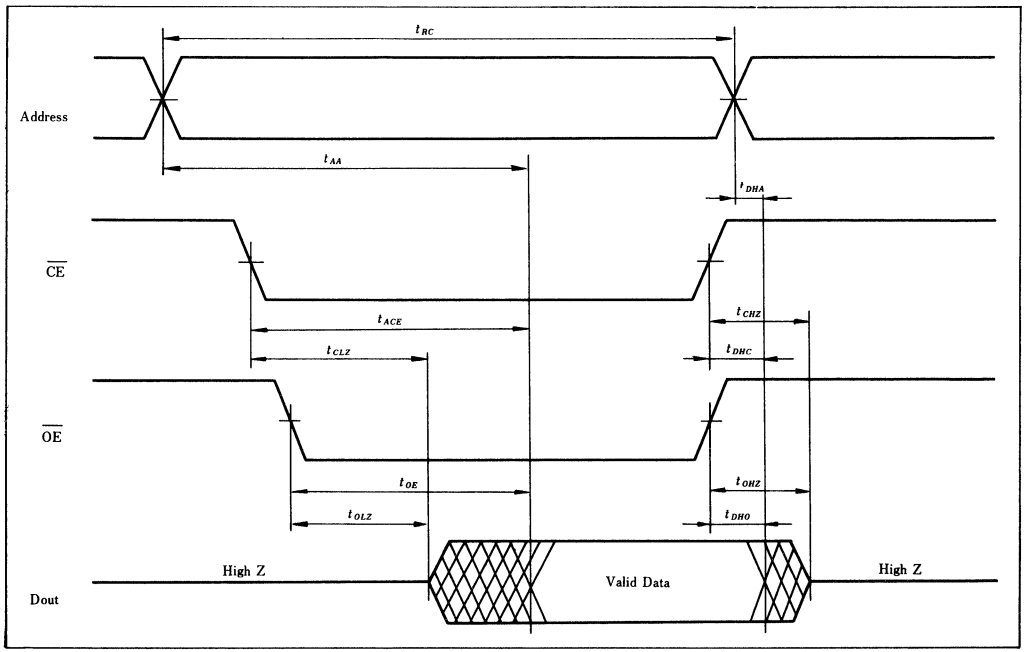
- Input Pulse Level . . . . . 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load . . . . . 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
$\overline{CE}$ Access Time	t_{ACE}	—	200	ns
OE Access Time	t_{OE}	—	70	ns
BHE Access Time	t_{BHE}	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time from OE	t_{DHO}	0	—	ns
Output Hold Time from BHE	t_{DHB}	0	—	ns
Data Hold Time from $\overline{CE}$	t_{CHZ} *	—	70	ns
Data Hold Time from OE * *	t_{OHZ} *	—	70	ns
Data Hold Time from BHE	t_{BHZ} *	—	70	ns
Data Setup Time from $\overline{CE}$	t_{CLZ}	10	—	ns
Data Setup Time from OE	t_{OLZ}	10	—	ns
Data Setup Time from BHE	t_{BLZ}	10	—	ns

Note) *1. t_{CHZ} and t_{OHZ} and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.
*2. In the case of OE pin being non-connected, this item is not applied.

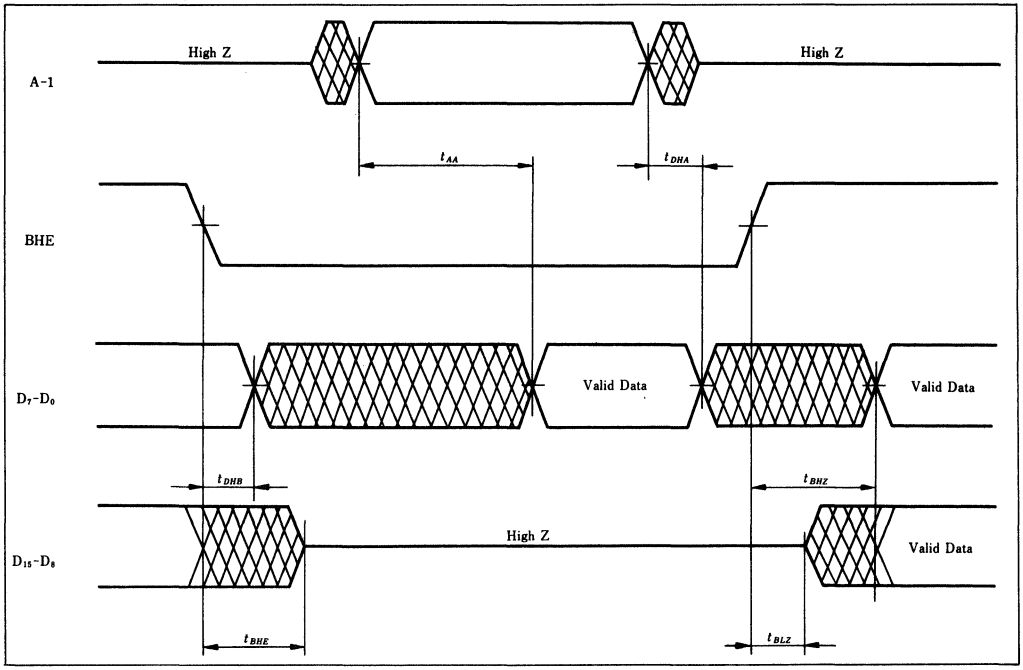
Timing Diagram

(1) Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA}, t_{DHC} or t_{DHO}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA}, t_{ACE} or t_{OE}, whichever occurs last.
3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ}, whichever occurs last.

(2) Word Mode, Byte Mode Switch



Notes) 1. $\overline{CE}$, $\overline{OE}$/OE is enable A17 – A0 is valid.
2. If BHE is high and $\overline{CE}$, $\overline{OE}$ is enable D15/A-1 pin is in the output state.
Therefore, the input signals of opposite phase to the outputs must not be applied to them.

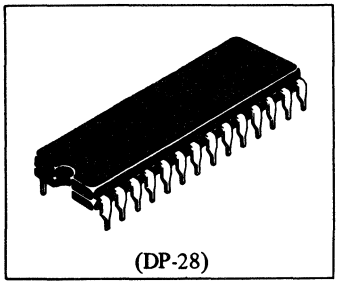
EEPROM, EPROM, OTPROM

HN58064 Series

8192-word x 8-bit Electrically Erasable and Programmable ROM.

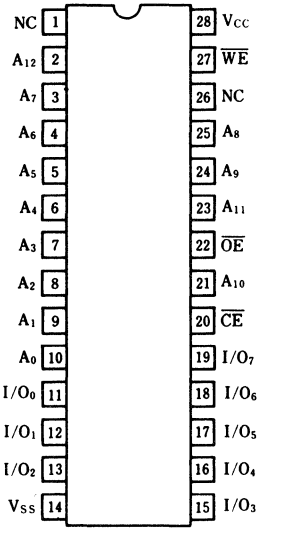
■ FEATURES

- Single 5V Supply
- Address, Data, $\overline{CE}$, $\overline{OE}$ Latches
- Byte Erase / Byte Write Time. . . . . 10 ms typ.
- Chip Erase Time . . . . . 20 ms typ.
- Fast Access Time. . . . . 250/300ns max.
- Low Power Dissipation. . . . . 300mW typ. (Active)
  . . . . . 125mW typ. (Standby)
- Comforms to JEDEC Byte-Wide Standard
- Reliable N-channel MNOS Technology
- 10000 Erase/Write Cycles



(DP-28)

■ PIN ARRANGEMENT

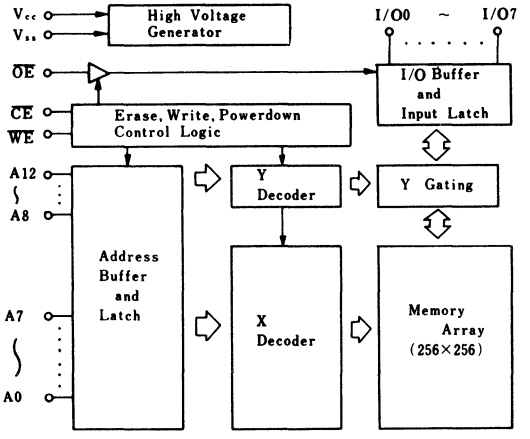


(Top View)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58064P-25	250ns	600 mil 28 pin Plastic
HN58064P-30	300ns	DIP

■ BLOCK DIAGRAM



A0 – A12	Address Input
I/O0 – I/O7	Data in / Data out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
Vcc	Power (+5V)
Vss	GND
NC	No Connect

■ MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	Dout
Standby	V_{IH}	X	X	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IL}	Din = V_{IH}
Byte Write	V_{IL}	V_{IH}	V_{IL}	Din
Chip Erase	V_{IL}	V_{IL}	V_{IL}	Din = V_{IH}
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z

X: V_{IH} or V_{IL}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	−0.6 to +7.0	V
Input Voltage*1	V_{in}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Note) *1. With Respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.1	–	0.8	V
	V_{IH}	2.0	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (Ta = 0 to 70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{in} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V, V_{out} = 5.5/0.4V	–	–	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	25	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	60	100	mA
Input Low Voltage	V_{IL}		−0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V

■ CAPACITANCE (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	12	pF

■ AC TEST CONDITIONS

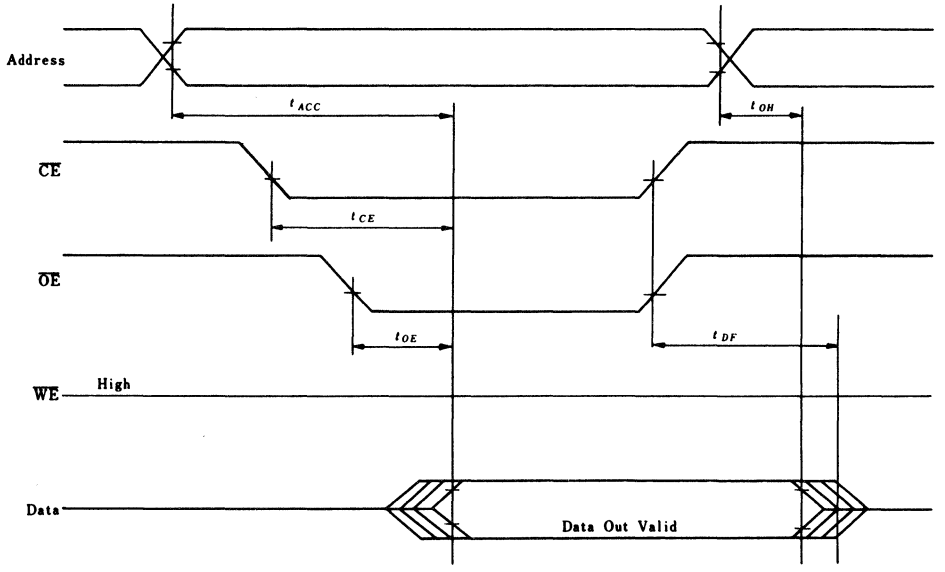
Input Pulse Levels: 0.4V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1TTL Gate + 100pF
Reference Level for Measuring Timing: 0.8V and 2.0V

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• READ OPERATION

Parameter	Symbol	Test Condition	HN58064P-25		HN58064-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	100	–	150	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	0	–	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	0	90	0	130	ns

• WAVE FORM ..... READ CYCLE



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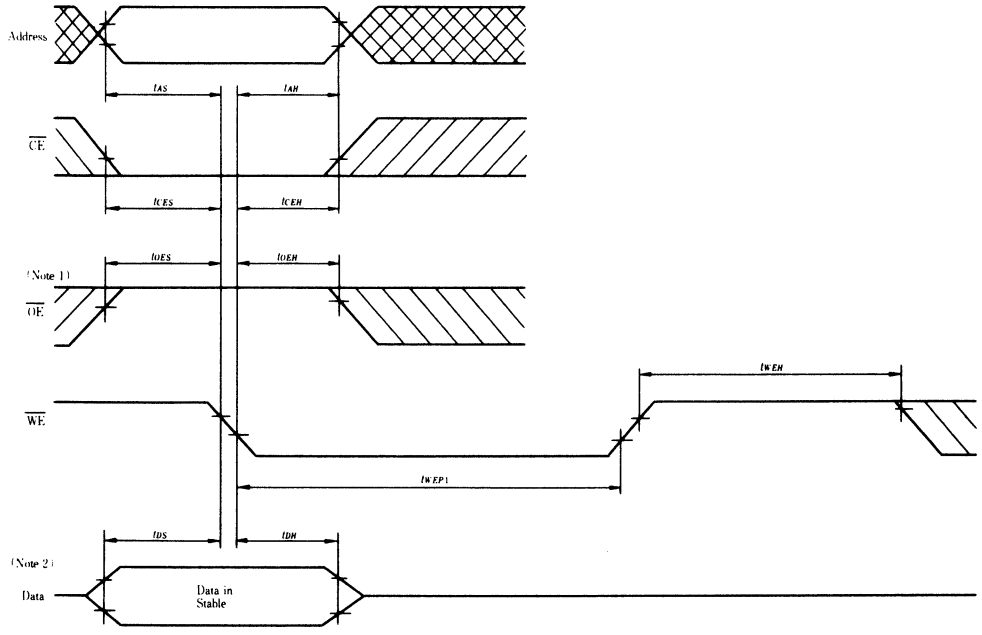
• BYTE ERASE AND BYTE WRITE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		0	–	–	ns
Address Hold Time	t_{AH}		100	–	–	ns
$\overline{CE}$ Setup Time	t_{CES}		0	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		100	–	–	ns
$\overline{OE}$ Setup Time	t_{OES}		0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}		100	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP1}		8	10	15	ms
$\overline{WE}$ High Time	t_{WEH}		1000	–	–	ns
Data Setup Time	t_{DS}		0	–	–	ns
Data Hold Time	t_{DH}		100	–	–	ns

• WAVE FORM ..... ERASE AND WRITE CYCLE

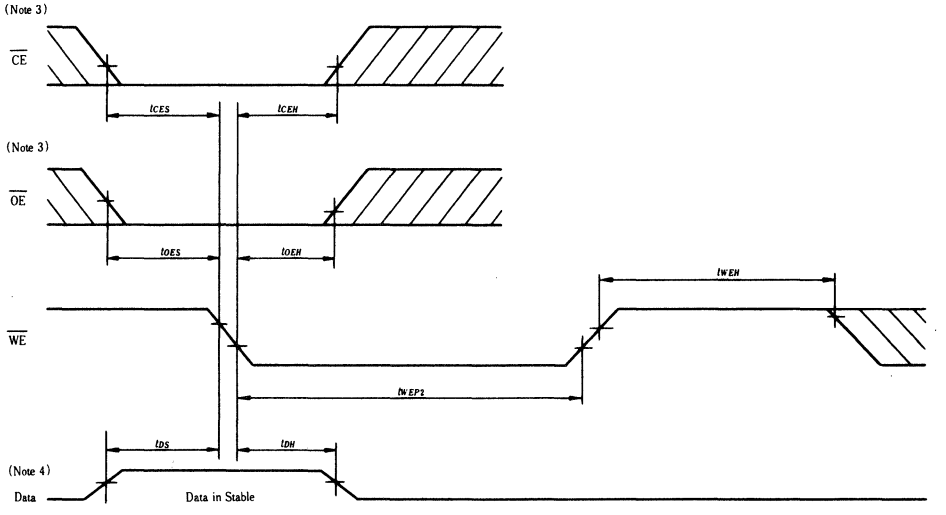


Notes) 1. $\overline{CE}$ or $\overline{OE}$ should be "1" and in Standby Mode or Deselect Mode before Write/Erase operation.
2. I/O_0 to I/O_7 must be "1" in Byte Erase.

• CHIP ERASE OPERATION I

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{CE}$ Setup Time	t_{CES}		0	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		100	–	–	ns
$\overline{OE}$ Setup Time	t_{OES}		0	–	50	ns
$\overline{OE}$ Hold Time	t_{OEH}		100	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP2}		15	20	25	ms
$\overline{WE}$ High Time	t_{WEH}		1000	–	–	ns
Data Setup Time	t_{DS}		0	–	–	ns
Data Hold Time	t_{DH}		100	–	–	ns

• WAVE FORM ..... CHIP ERASE I

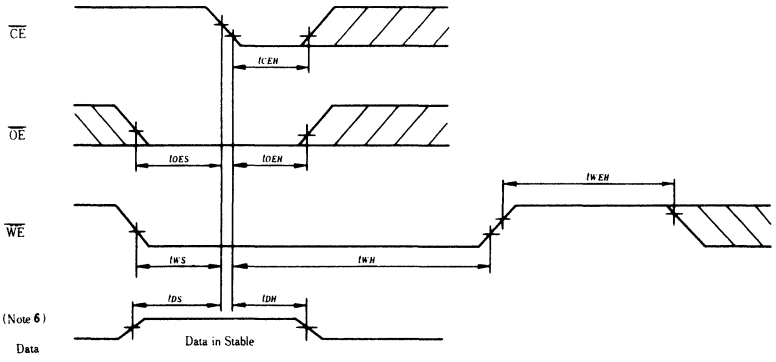


Notes) 3. $\overline{CE}$ or $\overline{OE}$ should be "1" and in Standby Mode or Deselect Mode before Chip Erase operation.
4. I/O_0 to I/O_7 must be "1" in Chip Erase operation.
5. Don't Care about Address.

• CHIP ERASE OPERATION II

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{CE}$ Hold Time	t_{CEH}		100	–	–	ns
$\overline{OE}$ Setup Time	t_{OES}		0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}		100	–	–	ns
$\overline{WE}$ Setup Time	t_{WS}		0	–	–	ns
$\overline{WE}$ Pulse Width	t_{WH}		15	20	25	ms
$\overline{WE}$ High Time	t_{WEH}		1000	–	–	ns
Data Setup Time	t_{DS}		0	–	–	ns
Data Hold Time	t_{DH}		100	–	–	ns

• WAVE FORM ..... CHIP ERASE II



Notes) 6. I/O 0 ~ 7 must be "1" in Chip Erase Operation.
7. Don't Care about Address.

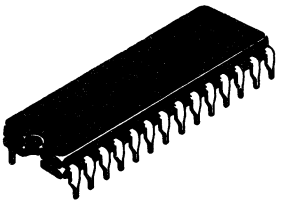
HN58C65 Series

8192-word x 8-bit Electrically Erasable and Programmable CMOS ROM

■ FEATURES

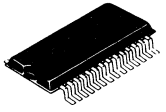
- Single 5V Supply
- On Chip Latches; Address, Data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic Byte Write . . . . . 10ms typ.
- Automatic Page Write
  (32byte) . . . . . 10ms typ.
- Fast Access Time . . . . . 250ns max.
- Low Power Dissipation . . . 20mW/MHz typ. (Active)
  . . . 2mW typ. (Standby)
- $\overline{Data}$ Polling and Ready/$\overline{Busy}$
- Data Protection Circuity on Power On/Power Off
- Conforms to JEDEC Byte-Wide Standard
- Reliable CMOS with MNOS Cell Technology
- 10000 Erase/Write Cycles and 10 year Data Retention

HN58C65P Series



(DP-28)

HN58C65FP Series

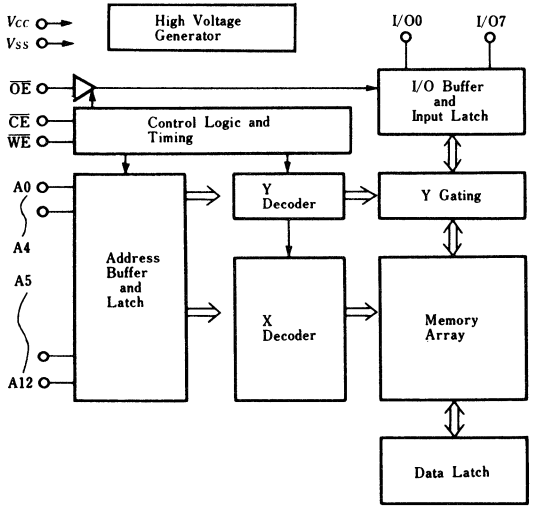


(FP-28DA)

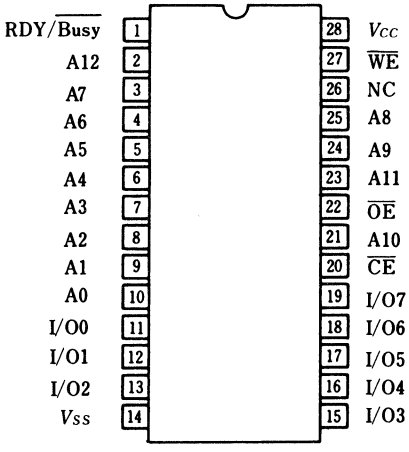
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C65P-25	250ns	600 mil 28 pin Plastic DIP
HN58C65FP-25T	250ns	28 pin Plastic SOP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

A0 – A12	Address Input
I/O1 – I/O7	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No Connect

■ MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	RDY/$\overline{Busy}$ (1)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	V_{IH}	High Z	Dout
Standby	V_{IH}	X	X	High Z	High Z
Write	V_{IL}	V_{IH}	V_{IL}	High Z→ V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Write Inhibit	X	X	V_{IH}	High Z	–
Write Inhibit	X	V_{IL}	X	High Z	–
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data Out (I/O7)

Note) X: V_{IL} or V_{IH}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	–0.6 to +7.0	V
Input Voltage*1	V_{in}	–0.5*2 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Notes) *1. With respect to V_{SS}.
*2. –3.0V for pulse width ≦ 50ns.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	–0.3	–	0.8	V
	V_{IH}	2.2	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = 5.5V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V V_{out} = 5.5/0.4V	–	–	2	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	1	mA
V_{CC} Current (Active)	I_{CC2}	Iout=0mA, duty=100%, cycle 1μs	–	–	8	mA
		Iout=0mA, duty=100%, Min. Cycle	–	–	25	mA
Input Low Voltage	V_{IL}		–0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400μA	2.4	–	–	V

Note) *1. –1.0V for pulse width ≦ 50ns

■ CAPACITANCE (T_a=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}= 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{out}=0V	–	–	12	pF

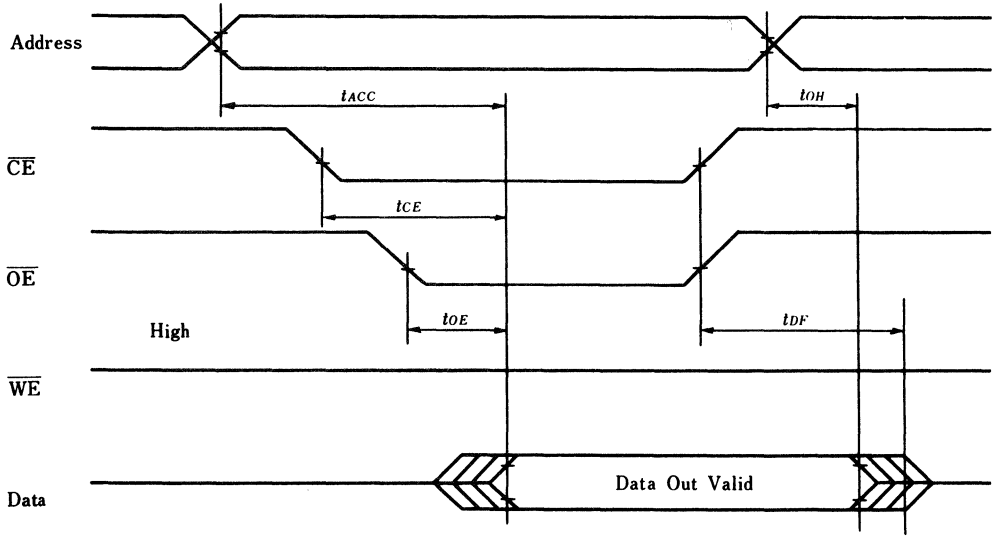
■ AC CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±10%)

• AC Test Conditions

Input Pulse Levels:	0.40V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1TTL Gate + 100pF
Reference Levels for Measuring Timing Inputs Outputs:	0.8V and 2V

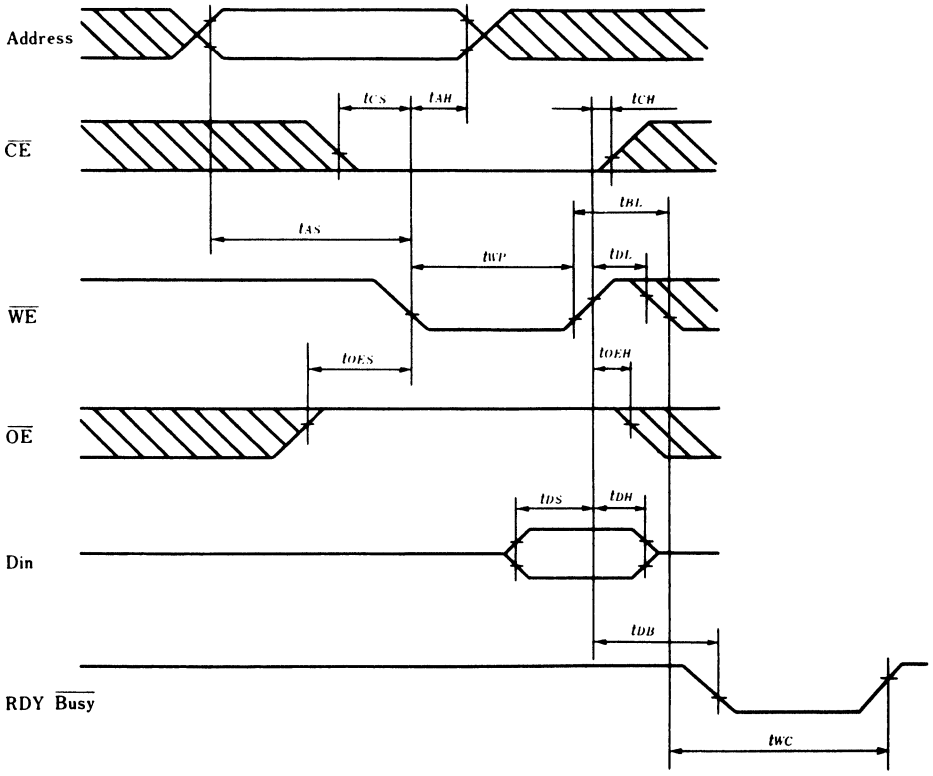
• Read Operation

Parameter	Symbol	Test Condition	HN58C65-25		Unit
			min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	10	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IH} $\overline{WE}$ = V_{IH}	0	90	ns



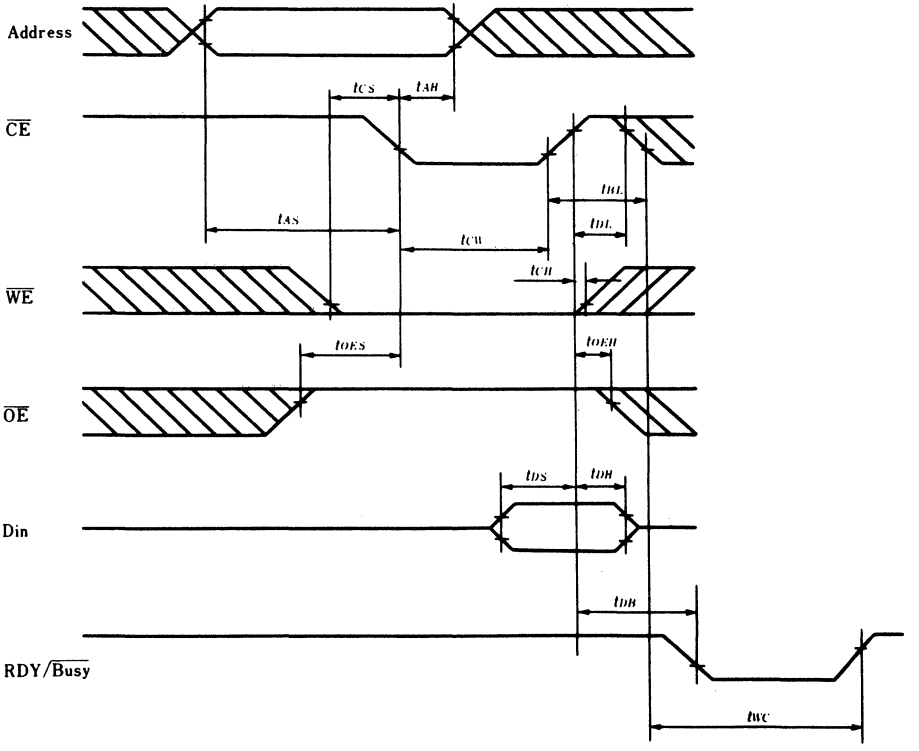
• Byte Erase and Byte Write Operation ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	μs



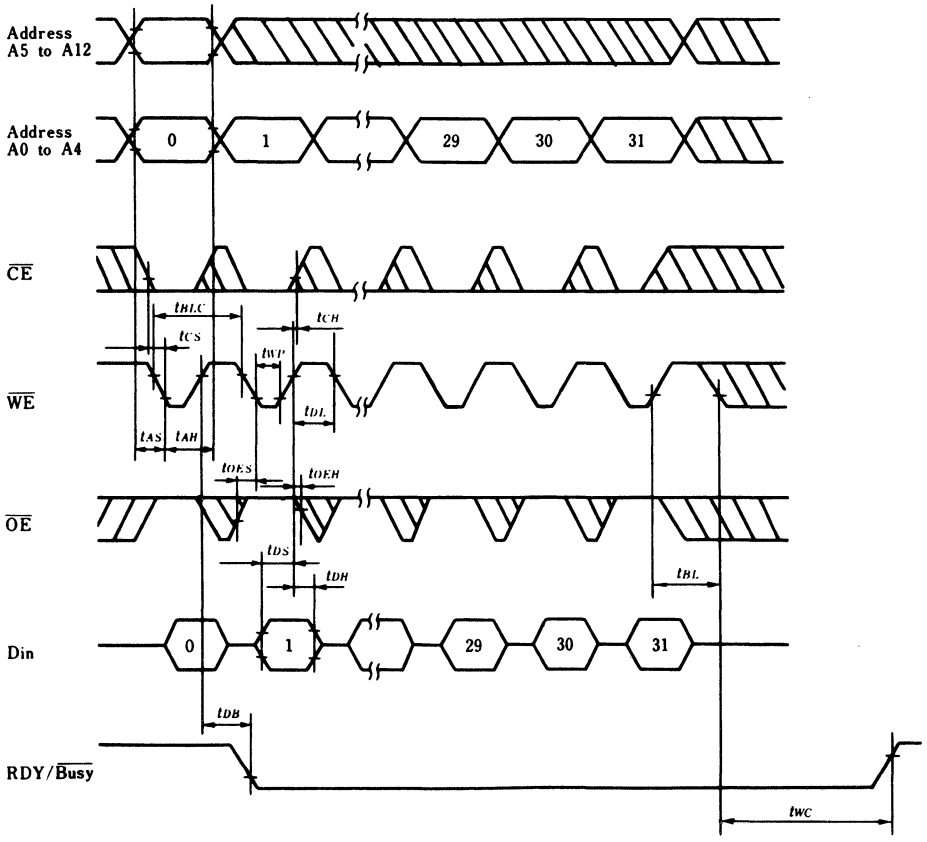
• Byte Erase and Byte Write Operation ($\overline{CE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	•μs



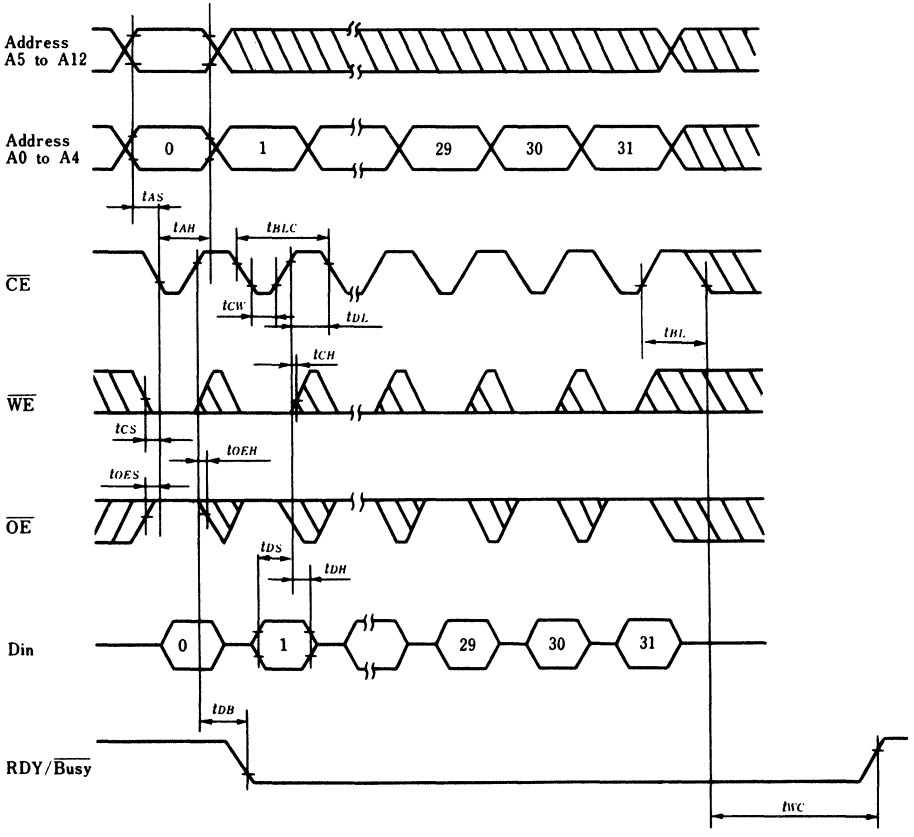
- **Page Erase and Page Write Operation** ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	μs
Byte Load Cycle	t_{BLC}	0.3	–	30	μs



• Page Erase and Page Write Operation ($\overline{CE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	15	ms
Byte Load Window	t_{BL}	30	–	100	μs
Byte Load Cycle	t_{BLC}	0.3	–	30	μs



- **Automatic Page Write**

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner as the first byte was written. Each additional byte load cycle must be started within 30μs of the preceding rising edge of the $\overline{WE}$.

- **$\overline{Data}$ Polling**

$\overline{Data}$ polling allows comparison operation to determine the status of the EEPROM. During a write cycle, an attempted read of the last byte written in the EEPROM results in the complement data of that byte at I/O7.

- **Ready/$\overline{Busy}$ Signal**

RDY/$\overline{Busy}$ signal also allows to determine the status of the EEPROM, RDY/$\overline{Busy}$ signal has high impedance except in a write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, RDY/$\overline{Busy}$ signal changes its state to high impedance.

- **$\overline{WE}$, $\overline{CE}$ Pins Operation**

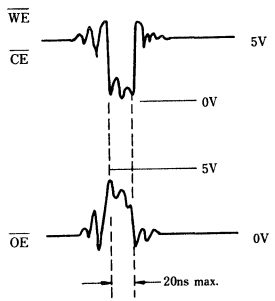
During a write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$: data are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$.

- **Data Protection**

To protect the data during operation and turning on/off, HN58C65 internally provides the following function.

1. Data Protection against the Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During reading out or standby, the noise on control pins may become trigger and turn EEPROM to program mode by error.
To prevent this phenomenon, HN58C65 has the noise cancell function of cutting the noise if its width is 20ns or less in program mode.
Care should be taken not to exist the noise whose width is more than 20ns on control pins.



2. Data Protection on Turning On/Off the V_{CC}

2-1 Prevention of unintentional programming on turning on/off the V_{CC}

On turning on/off V_{CC}, the noise on control pins generated by outer circuits (CPU, etc) may become trigger and turn the EEPROM to program mode by error. To prevent this unintentional programming, the EEPROM should be kept in unprogrammable state while CPU is in unstable state.

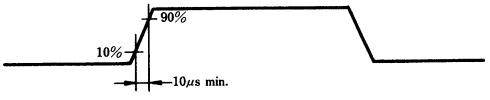
In addition, on turning on/off V_{CC}, the input level on control pins should be held as shown in the table below.

$\overline{CE}$	V_{CC}	X	X
$\overline{OE}$	X	V_{SS}	X
$\overline{WE}$	X	X	V_{CC}

X: Don't care.

2-2 Specifications of *tr* min. for V_{CC}

On turning on V_{CC}, if *tr* for *VCC* is shorter than 1μs, the EEPROM turns into program mode regardless of the input level on control pins and results in data destruction.

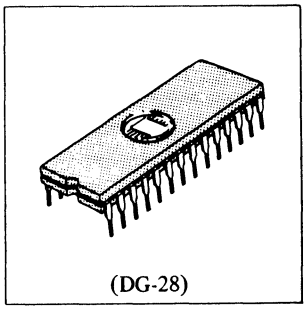


Since the actual minimum value of *tr* for proper operation is about 1μs, to take into account the timing margin, please keep tr longer than 10μs.

HN27128AG Series

16384-word × 8-bit UV Erasable and Programmable ROM

The HN27128AG is a 16384-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin, dual-in-line package with transparent window. The transparent window allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.



(DG-28)

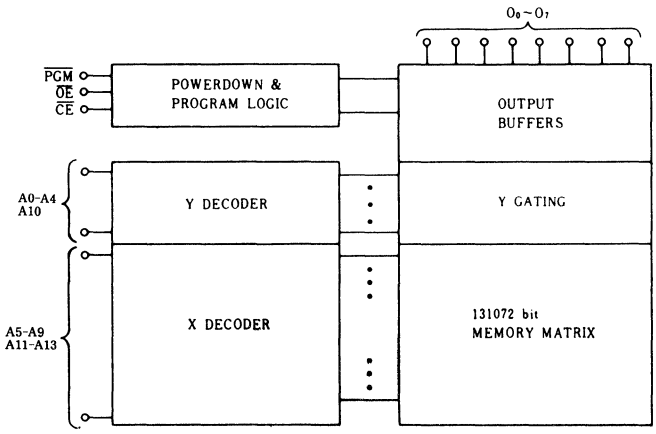
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 170/200/250/300ns(max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V Max.
- Low Stand-by Current . . . . . 35mA Max. (stand-by)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code

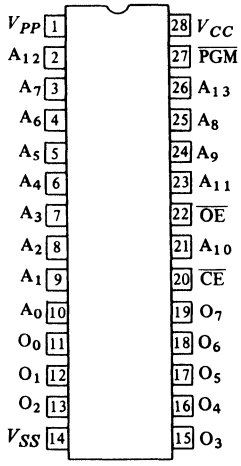
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27128AG-17	170ns	600 mil 28 pin Cerdip
HN27128AG-20	200ns	
HN27128AG-25	250ns	
HN27128AG-30	300ns	

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

MODE \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	X	V_{IL}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_{IH}	V_H*2	V_{CC}	V_{CC}	Code

Note) *1. X . . . Don't care
*2. V_H = 12.0V ±0.5V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6 to +13.5	V
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. With respect to V_{SS}

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.25V	–	–	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	40	100	mA
Input Low voltage	V_{IL}		−0.1*1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–	V

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

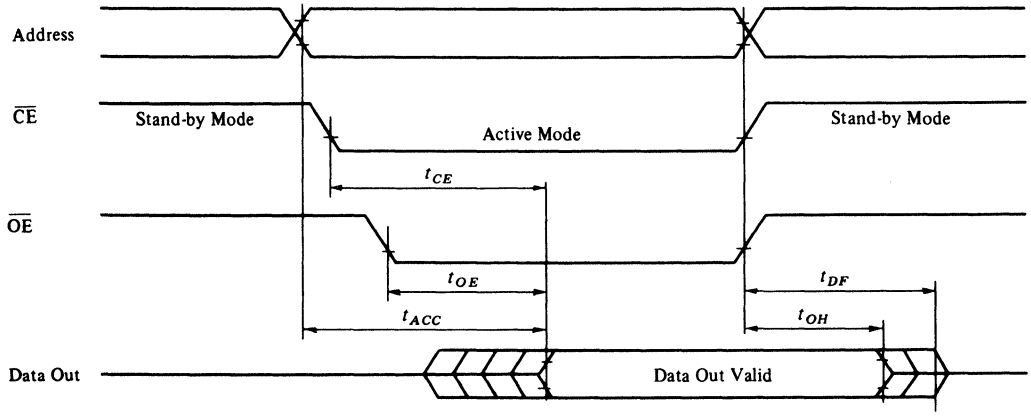
• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC}=5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Condition	HN27128AG-17		HN27128AG-20		HN27128AG-25		HN27128AG-30		Unit
			min.	max.	min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	–	170	–	200	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	–	170	–	200	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	–	75	–	75	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	55	0	55	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	–	0	–	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Output Load: 1 TTL Gate +100pF
Reference Level for Measuring Timing: 0.8V and 2.0V

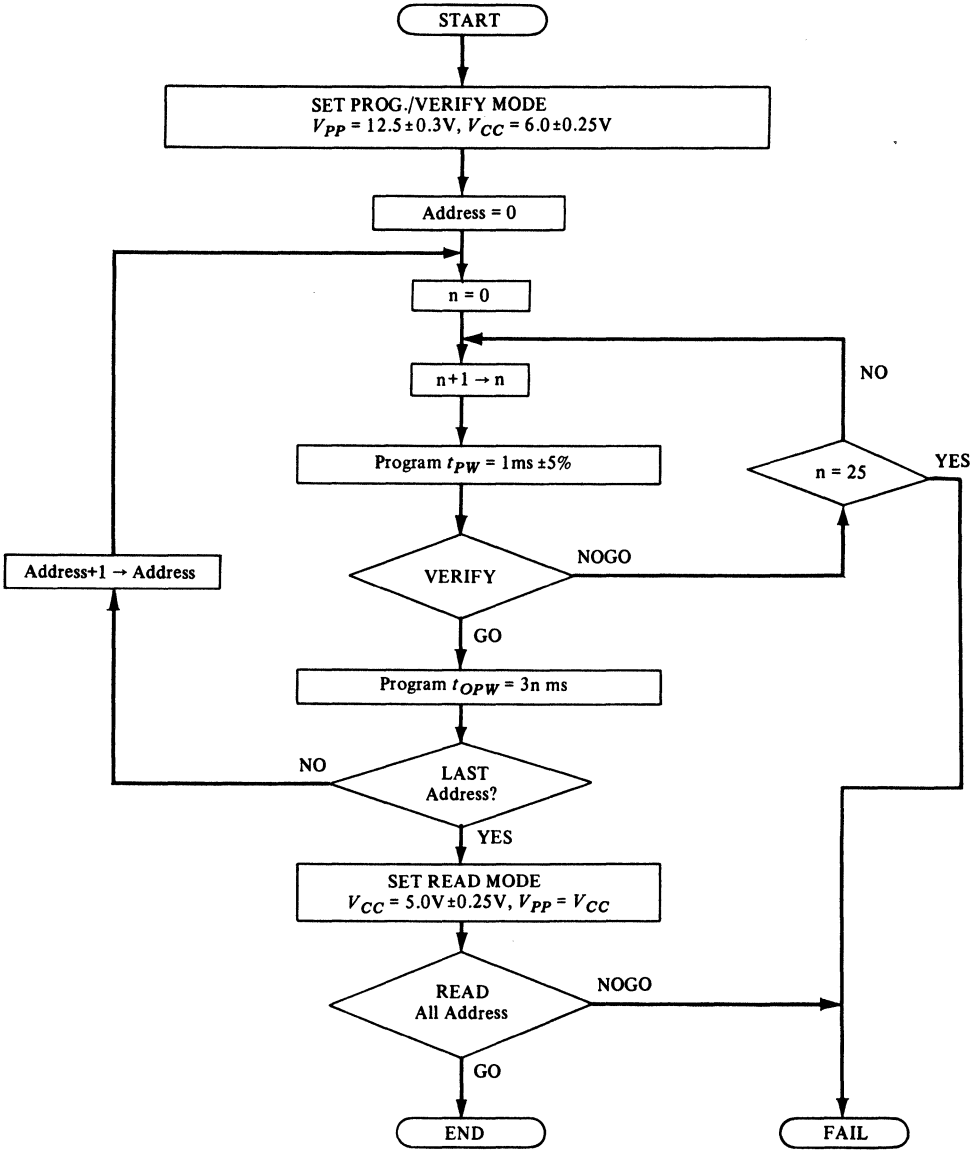


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$ = PGM = V_{IL}	–	–	50	mA

Notes) *1. −6.0V for pulse width ≤ 20ns.
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

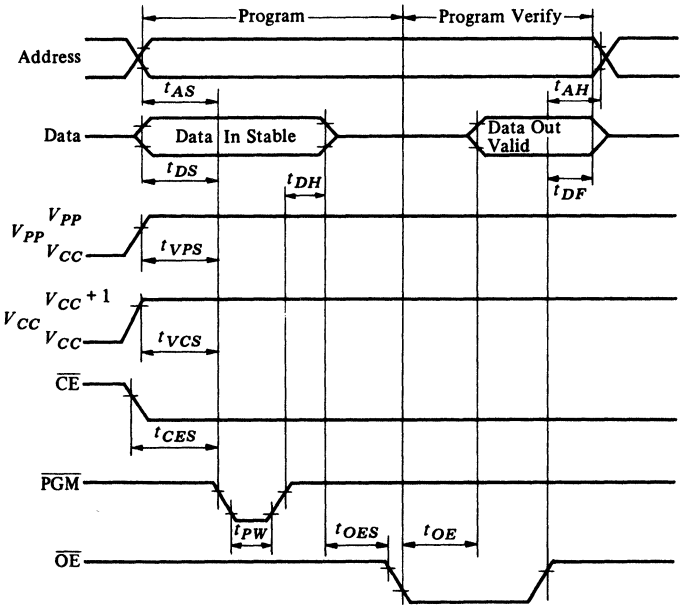
• AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

Notes) *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flow chart.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ ERASE

Erasure of HN27128AG is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W.sec/cm^2.

■ DEVICE IDENTIFIER MODE

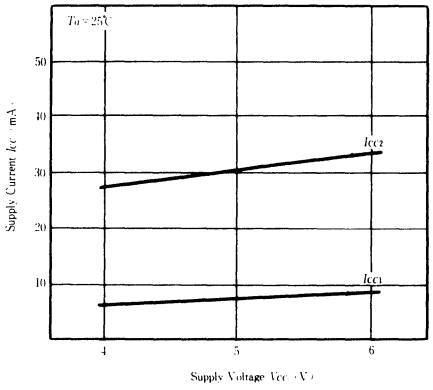
The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

• HN27128AG SERIES IDENTIFIER CODE

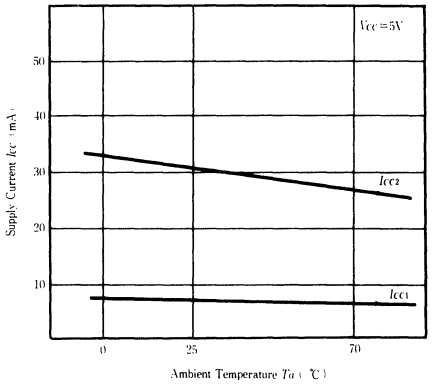
Pins / Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	0	0	1	1	0	1	0D

Notes: 1. A_9 = 12.0V ± 0.5V
2. A_1 – A_8, A_{10} – A_{13}, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}.

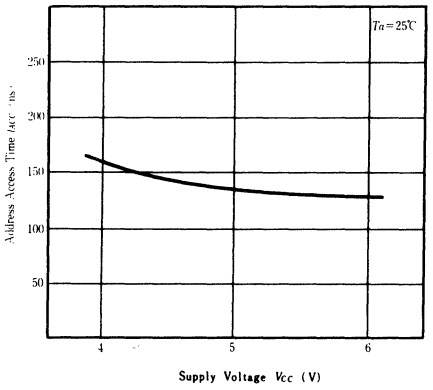
SUPPLY CURRENT VS. SUPPLY VOLTAGE



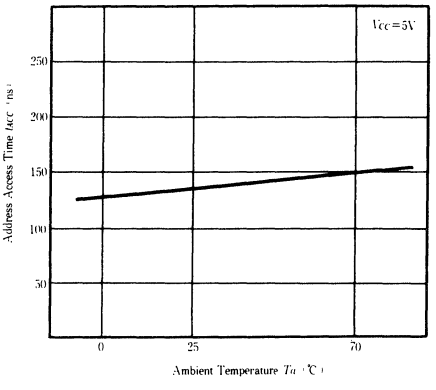
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



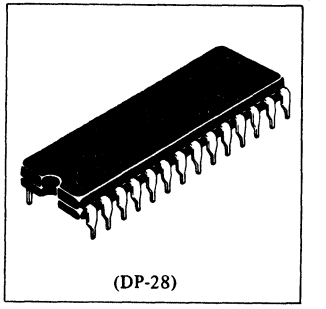
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



HN27128AP Series

16384-word x 8-bit One Time Electrically Programmable Read Only Memory

The HN27128AP is a 16384-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27128AP are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic dual-in-line package. Therefore, this device can not be re-written.

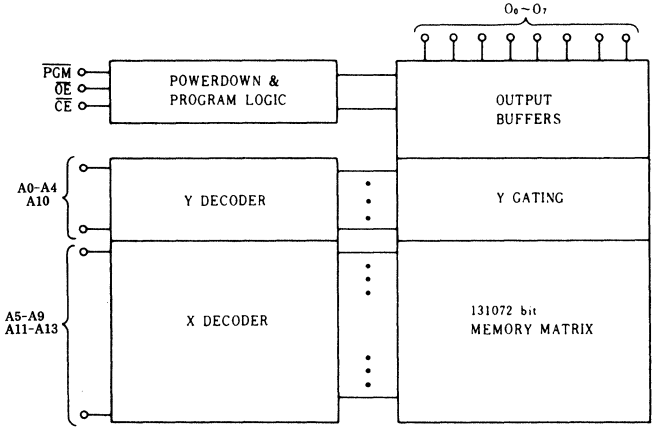


(DP-28)

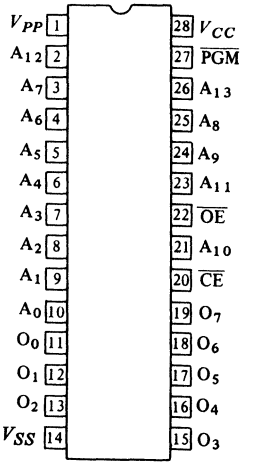
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 200/250ns (max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V Max.
- Low Standby Current . . . . . 35mA Max. (stand-by)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

MODE \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	X	V_{IL}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_{IH}	V_H*2	V_{CC}	V_{CC}	Code

Notes) *1. X . . . Don't care
*2. V_H = 12.0V ±0.5V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	–10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	–0.6 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	–0.6 to + 13.5	V
V_{PP} Voltage*1	V_{PP}	–0.6 to +14.0	V
V_{CC} Voltage *1	V_{CC}	–0.6 to +7	V

Note) *1. With respect to V_{SS}

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.25V	–	–	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	40	100	mA
Input Low voltage	V_{IL}		–0.1*1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = –400μA	2.4	–	–	V

Notes) *1. –0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

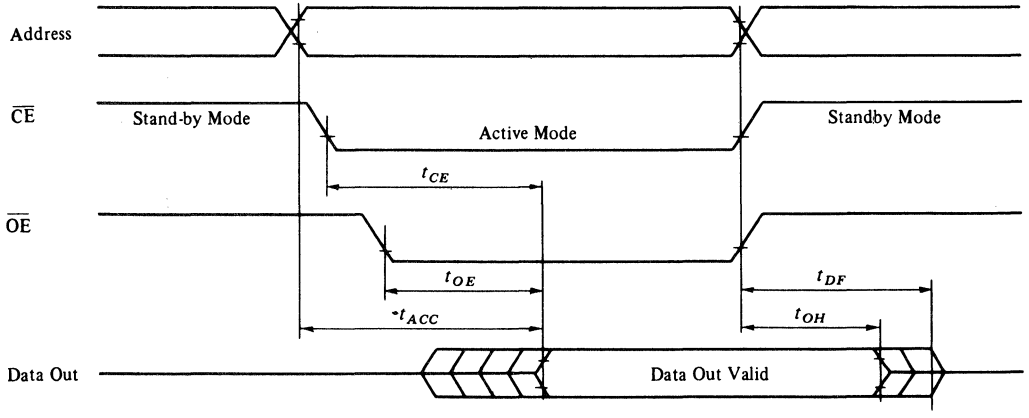
• AC CHARACTERISTICS (T_a = 0 to + 70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Condition	HN27128AP-20		HN27128AP-25		
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	200	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	200	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	75	–	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	55	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note) t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Output Load: 1 TTL Gate +100pF
Reference Level for Measuring Timing: 0.8V and 2.0V

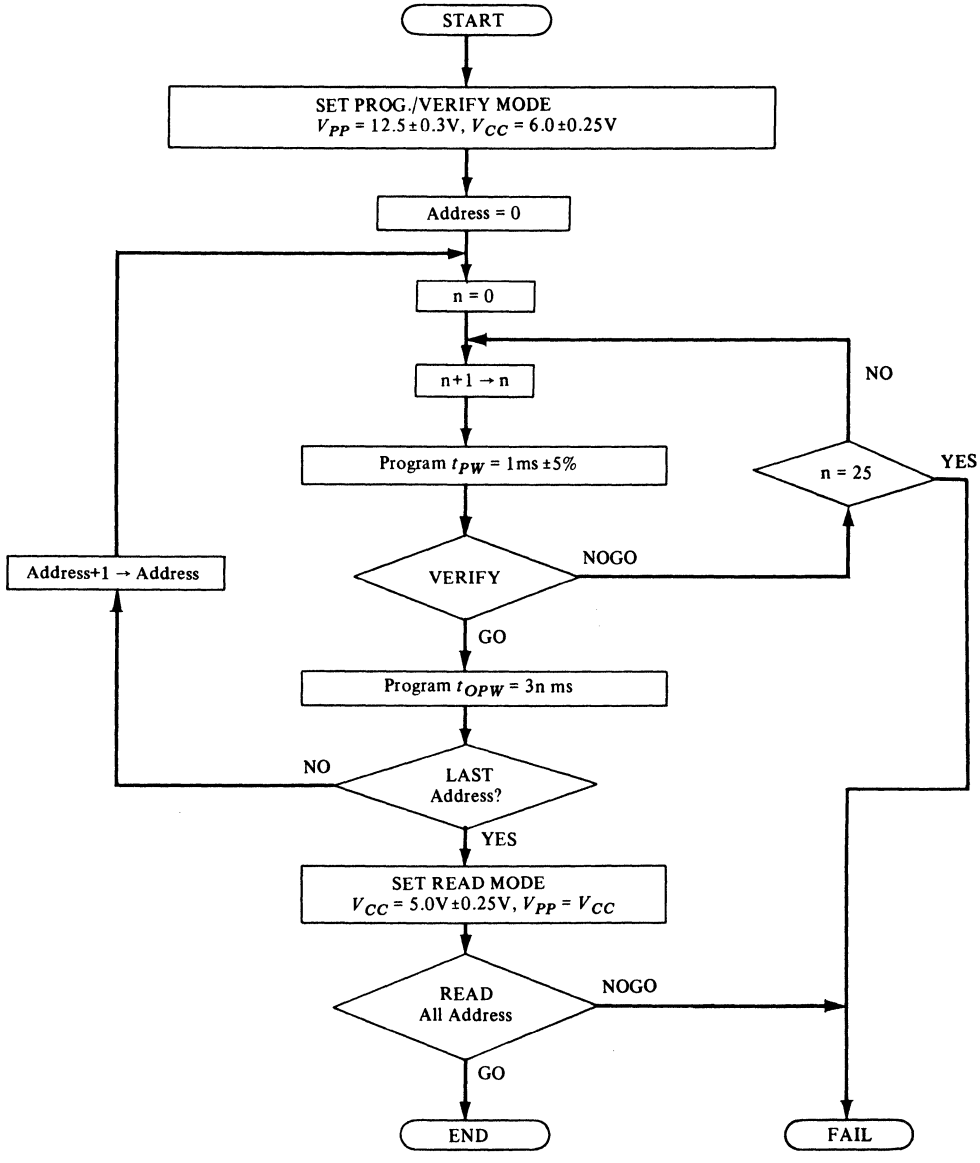


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns.
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

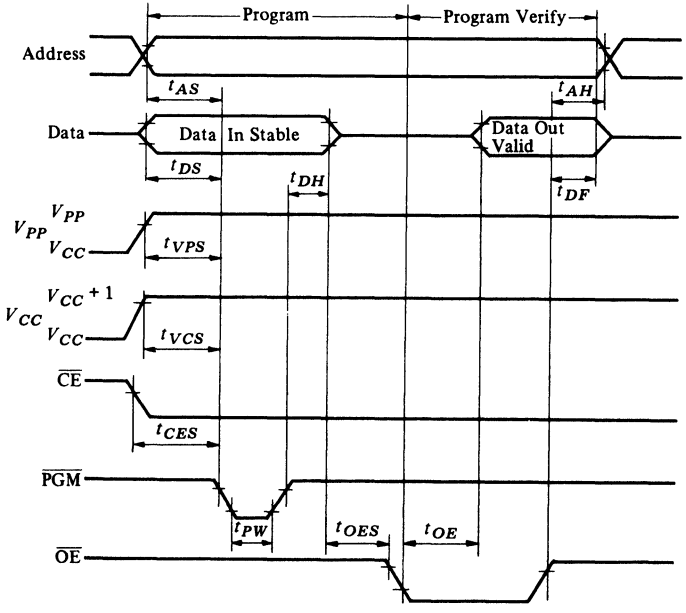
• AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

Notes: *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flow chart.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of OTPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

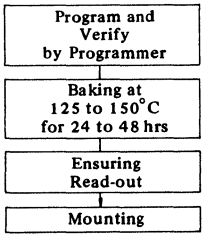
• HN27128AP SERIES IDENTIFIER CODE

Identifier \ Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	0	0	1	1	0	1	0D

Notes: 1. $A_9 = 12.0V \pm 0.5V$.
2. $A_1 - A_8, A_{10} - A_{13}, \overline{CE}, \overline{OE} = V_{IL}, \overline{PGM} = V_{IH}$.

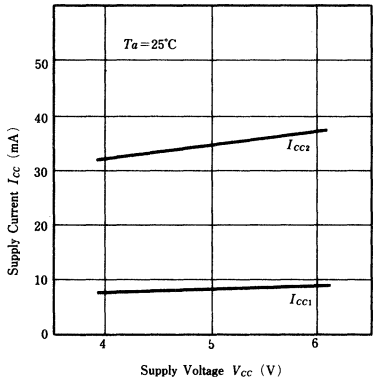
■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.

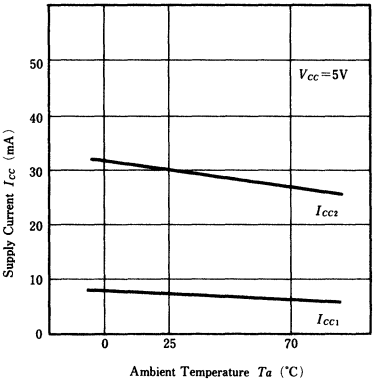


Recommended Screening conditions

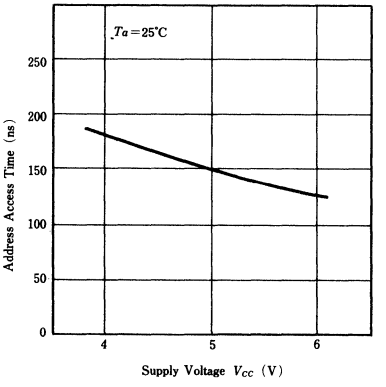
SUPPLY CURRENT vs. SUPPLY VOLTAGE



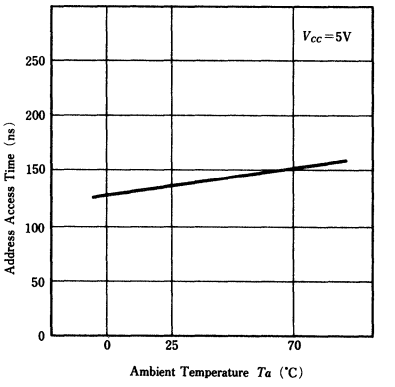
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE

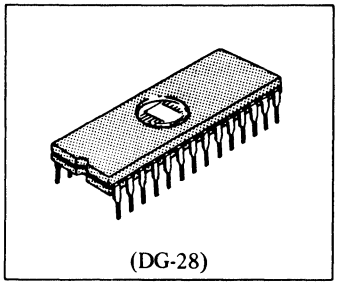


HN27256G Series

32768-word x 8-bit UV Erasable and Programmable ROM

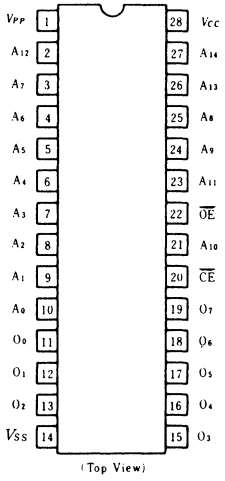
■ FEATURES

- Single Power Supply . . . . . +5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V D.C.
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . HN27256G-25:250ns(max.) HN27256G-30:300ns(max.)
- Absolute Max. Rating of V_{pp} pin . . 14.0V
- Low Stand-by Current . . . . . 40mA max. (stand-by)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code



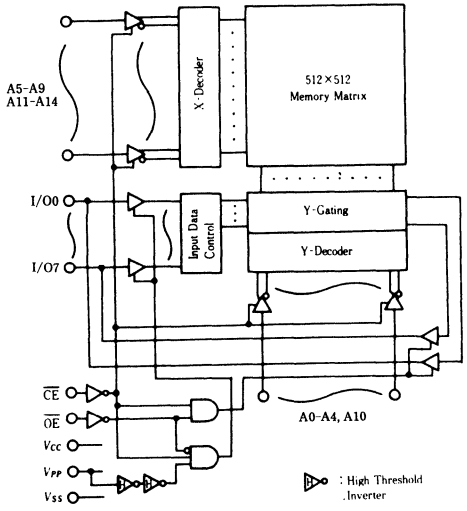
(DG-28)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	CE (20)	OE (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes) *1. X: Don't care.
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	− 65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	− 10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
A9 Input Voltage*1	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. with respect to V_{SS}.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ±5%, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5 V	–	–	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	45	100	mA
Input Low Voltage	V_{IL}		−0.1*1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC} + 1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V

*: V_{IL} min. = −0.6V for pulse width ≦ 20ns.
**: V_{IH} max. = V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

● AC CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V ±5%, $V_{PP} = V_{CC}$)

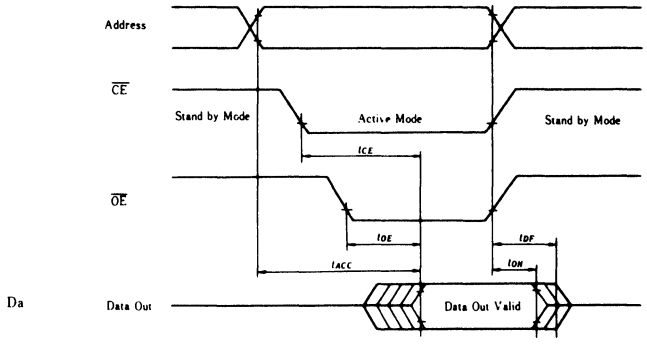
Parameter	Symbol	Test Condition	HN27256G-25		HN27256G-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
Input rise and fall time: ≤20ns
Output load: 1 TTL Gate +100pF
Reference level for measuring timing: 0.8V and 2V

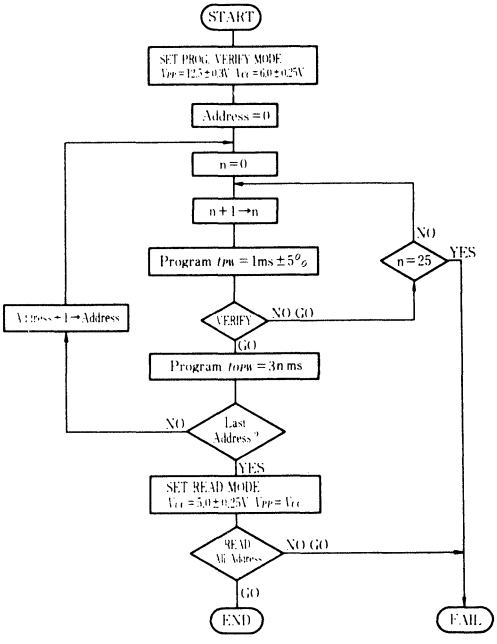


■ CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	V_{in} = 0 V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25 V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns.
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

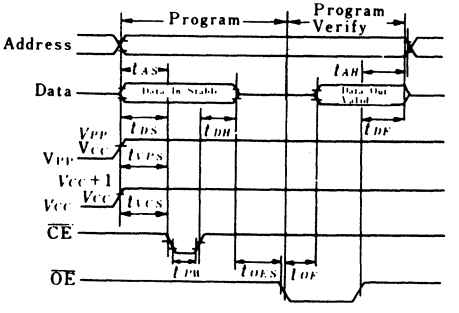
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{OE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*1		2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

Note) *1. t_{OPW} is defined as mentioned in flow chart. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition

Input pulse level: 0.45 to 2.4V
Input rise and fall time: ≦ 20ns
Reference level for measuring time: 0.8V and 2V



■ ERASE

Erasure of HN27256G is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm^2.

■ DEVICE IDENTIFIER MODE

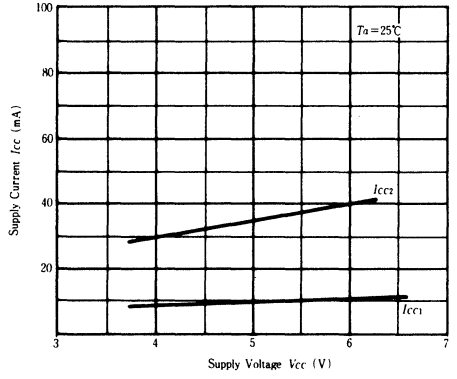
The Identifier Mode allows the reading out of binary codes that identify Manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

● HN27256G SERIES IDENTIFIER CODE

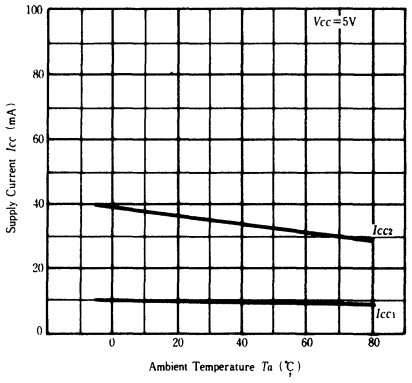
Pins / Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	0	1	0	0	0	0	10

Notes: 1. $A_9 = 12.0V \pm 0.5V$.
2. $A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$.

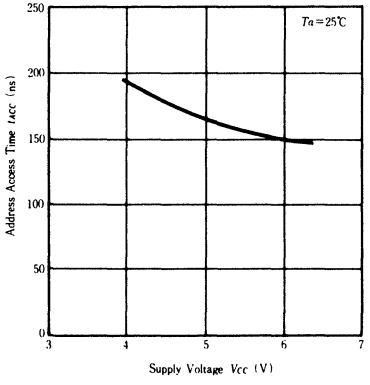
SUPPLY CURRENT VS. SUPPLY VOLTAGE



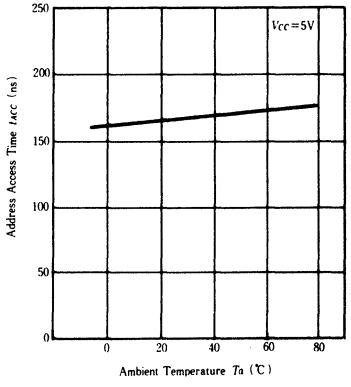
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



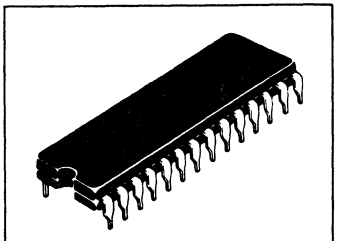
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



HN27256P Series

32768-word x 8-bit One Time Electrically Programmable ROM

The HN27256P is a 32768-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27256P are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28-pin, dual-in-line plastic package, therefore, this device can not be rewritten.



(DP-28)

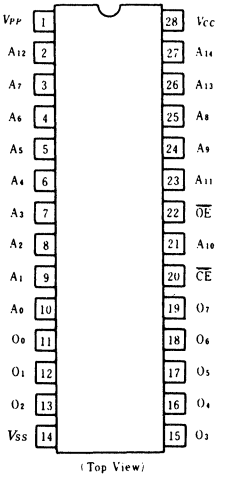
■ FEATURES

- Single Power Supply . . . . . +5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V D.C.
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 250/300ns (max.)
- Absolute Max. Rating of V_{pp} pin . . 14.0V
- Low Standby Current . . . . . 40mA max. (stand-by)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code

■ ORDERING INFORMATION

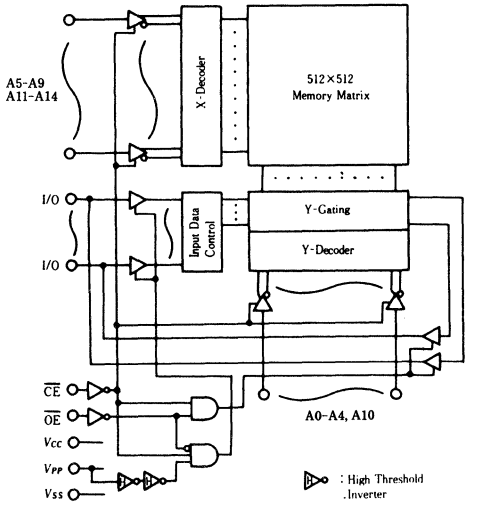
Type No.	Access Time	Package
HN27256P-25	250ns	600 mil Plastic DIP
HN27256P-30	300ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Note) *1. X: Don't care.
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	– 10 to +80	°C
All Input and Output Voltage*1	V_{IN}, V_{out}	–0.6 to +7	V
A9 Input Voltage*1	V_{ID}	–0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	–0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	–0.6 to +7	V

Note) *1. With respect to V_{SS}.

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5 V	–	–	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	45	100	mA
Input Low Voltage	V_{IL}		–0.1*1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = –400 μA	2.4	–	–	V

Notes) *1. V_{IL} min. = –0.6V for pulse width less than 20ns.
*2. V_{IH} max. = V_{CC} +1.5V for pulse width less than 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC})

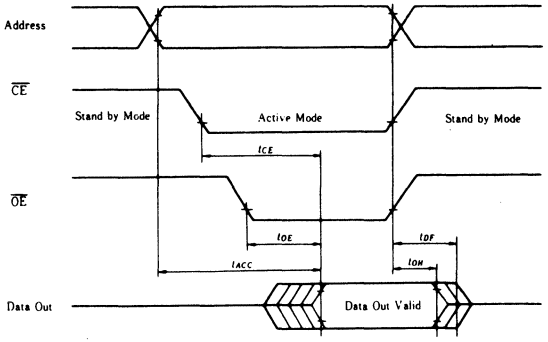
Parameter	Symbol	Test Condition	HN27256P-25		HN27256P-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High to Output Float	t_{DF}*1	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note) *1. t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

■ SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
Input rise and fall time: ≤20ns
Output load: 1 TTL Gate +100pF
Reference level for measuring timing: 0.8V and 2V

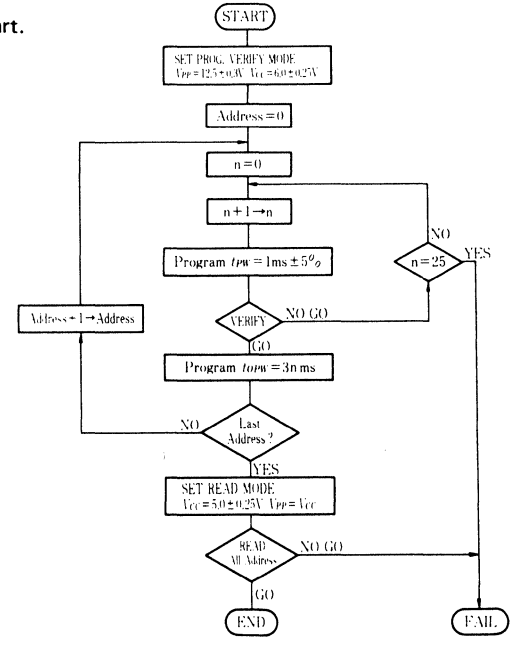


■ CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	V_{in} = 0 V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25 V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns.
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

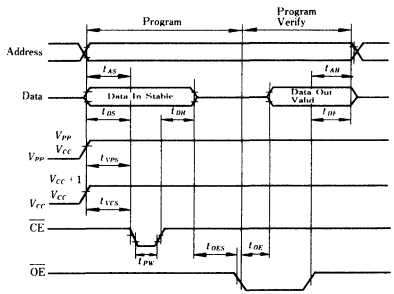
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{OE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

Notes) *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flow chart.

• SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse level: 0.45V to 2.4V
Input rise and fall time: ≤ 20ns
Reference level for measuring time: 0.8V and 2V



■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify Manufacturer and type of device from outputs of OTPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

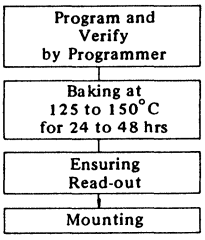
• HN27256P SERIES IDENTIFIER CODE

Pins / Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	0	1	0	0	0	0	10

Notes: 1. A_9 = 12.0V ± 0.5V.
A_1 – A_8, A_{10} – A_{14}, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.



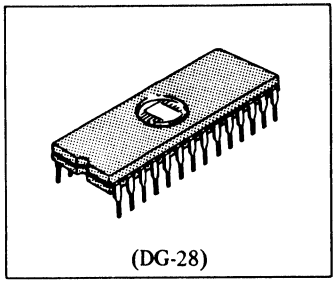
Recommended Screening conditions

HN27C256G Series

32768-word x 8-bit CMOS UV Erasable and Programmable ROM

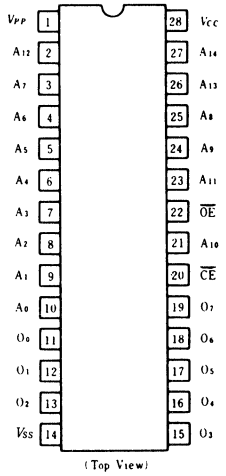
■ FEATURES

- Low Power Dissipation . . . . . 40mW/MHz max. (Active Mode)
  110μW max. (Stand-by Mode)
- Access Time . . . . . 170/200/250/300ns (max.)
- Single Power Supply . . . . . 5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V DC
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Absolute Max. Rating of V_{PP} pin. . . 14.0V
- Device Identifier Mode . . . . . Manufacturer Code and Device Code
- Compatible with INTEL 27256

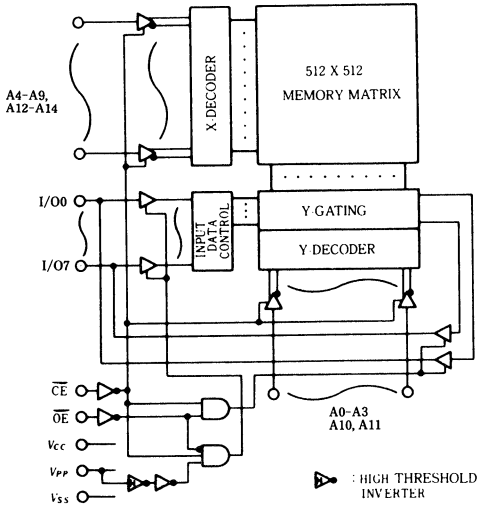


(DG-28)

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes) *1. X: Don't care.
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltage*1	V_{IN}, V_{OUT}	−0.6*2 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6*2 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Notes: *1. With respect to V_{SS}.
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5V	–	1	20	μA
V_{CC} Current (Standby)	I_{SB1}	$\overline{CE}$ = V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$ = V_{CC} ± 0.3V	–	1	20	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{out} = 0 mA	–	–	30	mA
	I_{CC2}	f = 5 MHz, I_{out} = 0 mA	–	–	30	mA
	I_{CC3}	f = 1 MHz, I_{out} = 0 mA	–	–	8	mA
Input Voltage	V_{IL}		−0.3*1	–	0.8	V
	V_{IH}		2.2	–	V_{CC}+1.0*2	V
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
	V_{OH1}	I_{OH} = −400 μA	2.4	–	–	V
	V_{OH2}	I_{OH} = −100 μA	V_{CC}−0.7	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC})

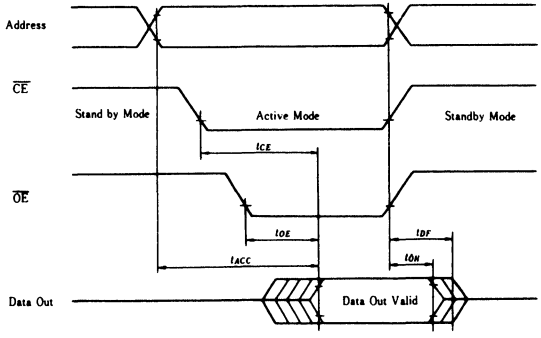
Parameter	Symbol	Test Condition	HN27C256G-17		HN27C256G-20		HN27C256G-25		HN27C256G-30		Unit
			min.	max.	min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	–	170	–	200	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	–	170	–	200	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	10	60	10	70	10	100	10	120	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	50	0	50	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	–	0	–	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

- **SWITCHING CHARACTERISTICS**

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
Input rise and fall time: ≤20ns
Output load: 1 TTL Gate +100pF
Reference level for measuring timing: 0.8V and 2.0V

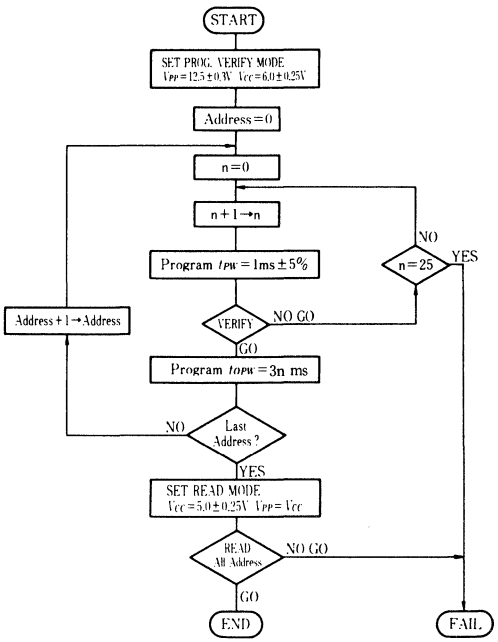


■ CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	V_{in} = 0 V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 6.25V/0.45V	–	–	2	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	30	mA
Input Low Level	V_{IL}		−0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 14V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. −0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

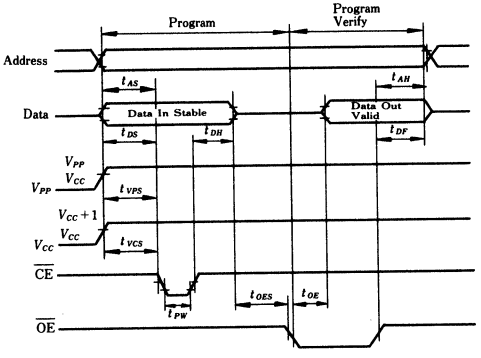
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}		2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes: t_{OPW} is defined as mentioned in flow chart.
t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition

Input pulse level: 0.45V to 2.4V
Input rise and fall time: ≦ 20ns
Reference level for measuring time: 0.8V and 2V



■ ERASE

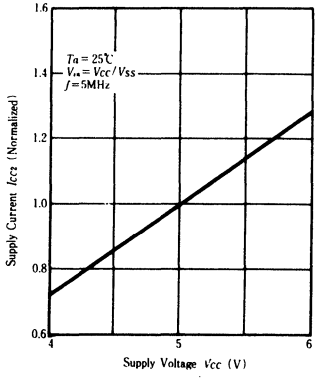
Erasure of HN27C256G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm^2

• HN27C256G IDENTIFIER CODES

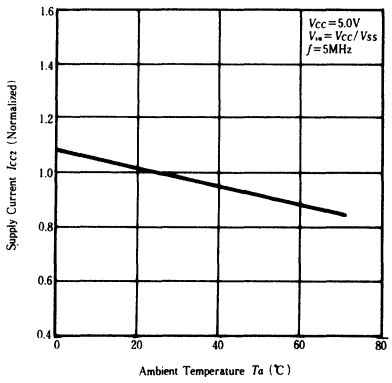
Pins / Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	1	1	0	0	0	0	B0

Notes: 1. A_9 = 12.0V ± 0.5V.
2. $A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$.

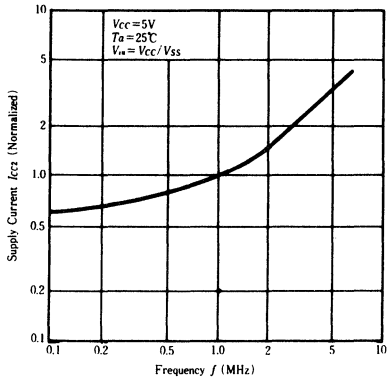
SUPPLY CURRENT VS. SUPPLY VOLTAGE



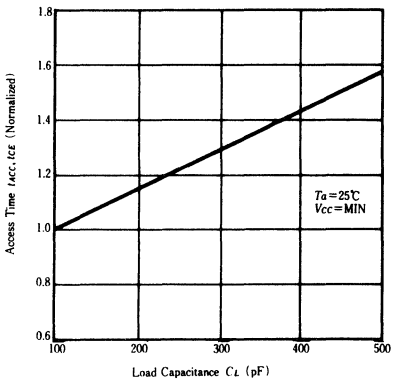
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



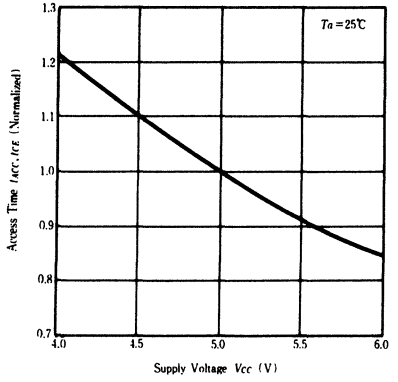
SUPPLY CURRENT VS. FREQUENCY



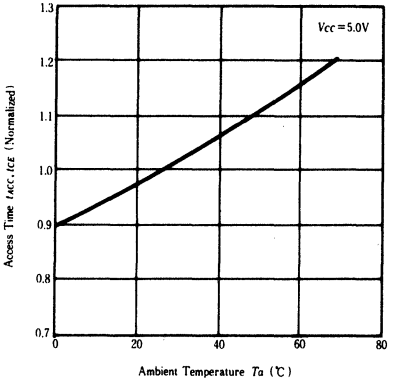
ACCESS TIME VS. LOAD CAPACITANCE



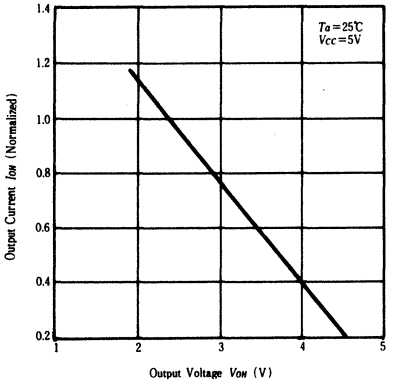
ACCESS TIME VS. SUPPLY VOLTAGE



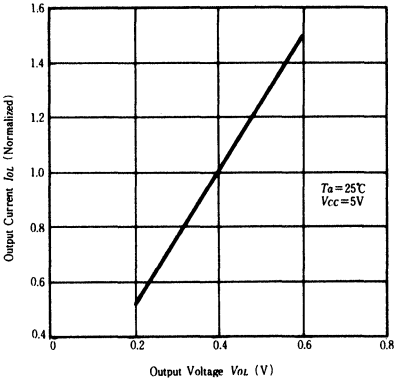
ACCESS TIME VS. AMBIENT TEMPERATURE



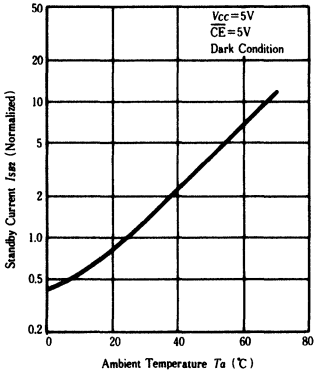
OUTPUT CURRENT VS. OUTPUT VOLTAGE



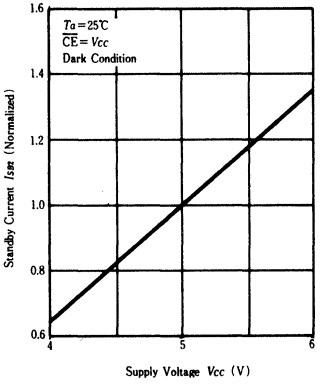
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



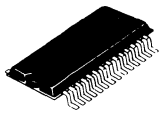
STANDBY CURRENT VS. SUPPLY VOLTAGE



HN27C256FP Series

32768-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C256FP is a 32768-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C256FP are in the "1" State (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic fiat package (SOP). Therefore, this device cannot be re-written.

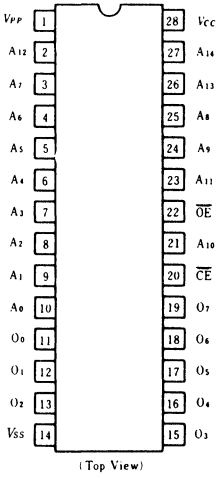


(FP-28DA)

■ FEATURES

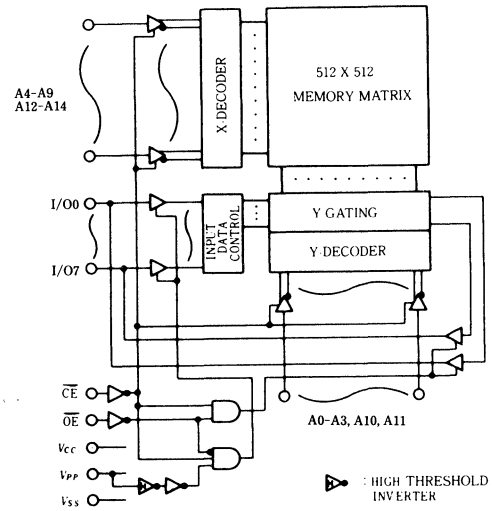
- Low Power Dissipation . . . . . .40 mW/MHz max. (Active Mode)
  110 μW max (Standby Mode)
- Access Time . . . . . .250 ns max. (HN27C256FP-25T)
  300 ns max. (HN27C256FP-30T)
- Single Power Supply . . . . . .5V ± 5%
- High Performance Programming . .Program Voltage: + 12.5V DC
- Static . . . . . .No Clock Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Absolute Max. Rating of V_{PP} pin . . 14.0V
- Device Identifier Mode. . . . . .Manufacturer Code and Device Code

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H *2	V_{CC}	V_{CC}	Code

Notes) *1. X: Don't care.
*2. V_H: 12.0 ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltage*1	V_{IN}, V_{OUT}	−0.6*2 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6*2 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Notes) *1. With respect to V_{SS}.
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (T_a = 0 ~ +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5V	–	1	20	μA
V_{CC} Current (Standby)	I_{SB1}	$\overline{CE}$ = V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$ = V_{CC} ± 0.3V	–	1	20	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{out} = 0 mA	–	–	30	mA
	I_{CC2}	f = 5 MHz, I_{out} = 0 mA	–	–	30	mA
	I_{CC3}	f = 1 MHz, I_{out} = 0 mA	–	–	8	mA
Input Voltage	V_{IL}		−0.3*1	–	0.8	V
	V_{IH}		2.2	–	V_{CC}+1.0*2	V
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
	V_{OH1}	I_{OH} = −400 μA	2.4	–	–	V
	V_{OH2}	I_{OH} = −100 μA	V_{CC}−0.7	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

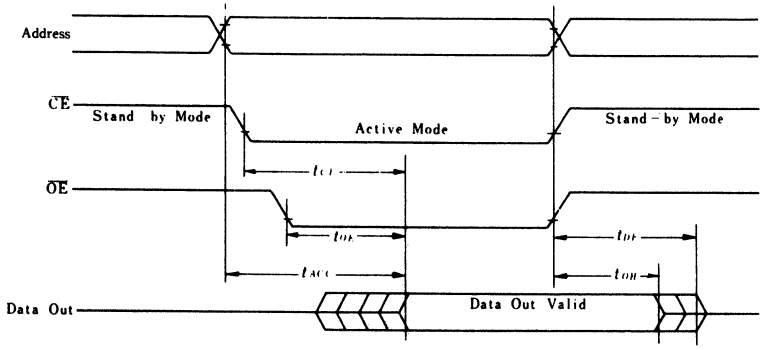
Parameter	Symbol	Test Conditions	HN27C256FP-25		HN27C256FP-30		Unit
			min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	—	250	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	—	250	—	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	100	10	120	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	—	0	—	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
Input rise and fall time: ≤20ns
Output load: 1 TTL Gate +100pF
Reference level for measuring timing: 0.8V and 2.0V

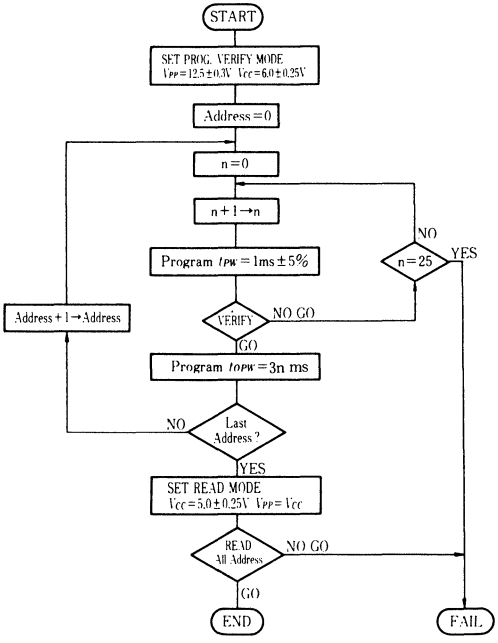


• CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit.
Input Capacitance	C_{in}	V_{in} = 0 V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 6.25V/0.45V	–	–	2	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	30	mA
Input Low Level	V_{IL}		−0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 14V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. −0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

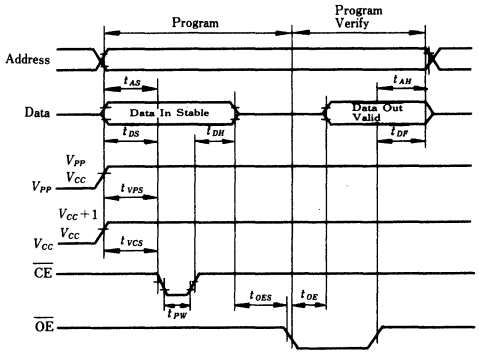
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes: *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flow chart.

• SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse level: 0.45V to 2.4V
Input rise and fall time: ≤20ns
Reference level for
measuring timing: 0.8V and 2V



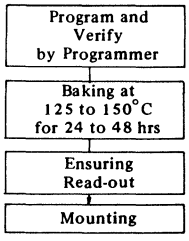
• HN27C256FP IDENTIFIER MODES

Pins / Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	1	1	0	0	0	0	B0

Notes: 1. A_9 = 12.0V ± 0.5V.
2. A_1 – A_8, A_{10} – A_{14}, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

HN27C256HG Series — Preliminary

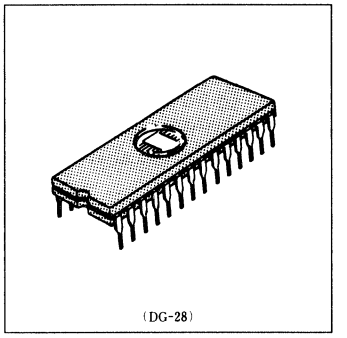
32768-word x 8-bit CMOS UV Erasable and Programmable ROM

The Hitachi HN27C256HG is a 256k-bit ultraviolet erasable and electrically programmable ROM, featuring high speed access time.

The HN27C256HG's maximum access time of 70 ns and 85 ns are the fastest in the 256-kbit EPROMs by the new advanced fine 256-kbit EPROMs by the new advanced fine process and high speed circuitry technique.

The timing conditions such as access time or output hold time are designed as same as our byte-wide SRAMs, allowing to use with SRAMs on the same memory board by the same read timings. So its board design in 16 bit microprocessor systems is easy.

Pin arrangement, pin configuration and programming voltage are compatible with our 256-kbit EPROM series, therefore existing programmers can be used with the HN27C256HG.

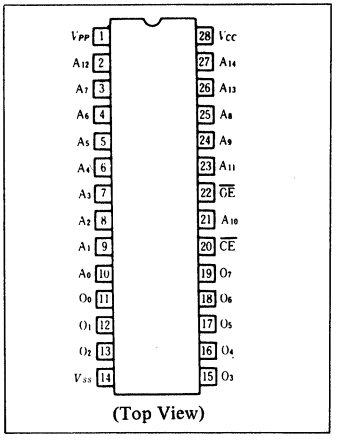


(DG-28)

Features

- High speed . . . . . Access time 70/85 ns (max.)
- Low power dissipation
  Active mode . . . . . 30 mW (typ.) (f = 1 MHz)
- Programming mode . . . . . Programming voltage: +12.5 V DC
- Device identifier mode
  Manufacturer code and device code

Pin Arrangement



(Top View)

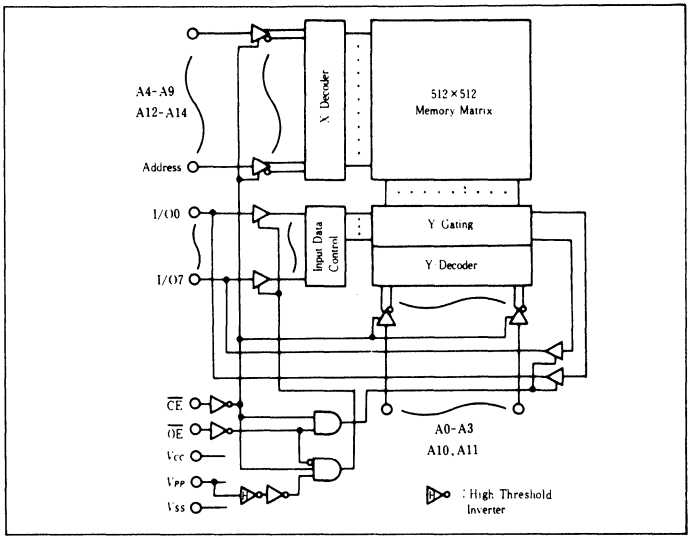
Ordering information

Type No.	Access Time	Package
HN27C256HG-70	70ns	600 mil 28 pin Cerdip
HN27C256HG-85	85ns	

Pin Description

Pin Name	Function
A0 – A14	Address
O0 – O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	Mode	CE (20)	OE (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 – 13, 15 – 19)
Read		V_{IL}	V_{IL}	x	V_{CC}	V_{CC}	Dout
Output disable		V_{IL}	V_{IH}	x	V_{CC}	V_{CC}	High Z
Standby		V_{IH}	x	x	V_{CC}	V_{CC}	High Z
High performance program		V_{IL}	V_{IH}	x	V_{PP}	V_{CC}	Din
Program verify		V_{IH}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Optional verify		V_{IL}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Program inhibit		V_{IH}	V_{IH}	x	V_{PP}	V_{CC}	High Z
Identifier		V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes) *1. x = Don't care.
*2. V_H = 12.0V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output Voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
A9 input voltage *1	V_{ID}	−0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	−0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	−0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−65 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +80	°C

Notes) *1. Relative to V_{SS}
*2. V_{in}, V_{out}, V_{ID} min = −1.0 V for pulse width ≦ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	4	8	pF	V_{in} = 0 V
Output capacitance	Cout	–	8	12	pF	Vout = 0 V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	V_{in} = 0 V to V_{CC}
Output leakage current	I_{LO}	–	–	2	μA	V_{out} = 0 V to V_{CC}
Vpp current	I_{PP1}	–	1	100	μA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB}	–	–	15	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, I_{out} = 0 mA
	I_{CC2}	–	–	50	mA	f = 15 MHz, I_{out} = 0 mA
	I_{CC3}	–	5	15	mA	f = 1 MHz, I_{out} = 0 mA
Input low voltage*3	V_{IL}	–0.3*1	–	0.8	V	
Input high voltage*3	V_{IH}	2.2	–	V_{CC}+1.0*2	V	
Output low voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH1}	2.4	–	–	V	I_{OH} = –1.0 mA
	V_{OH2}	V_{CC}–0.7	–	–	V	I_{OH} = –100 μA

Notes) *1. V_{IL} min = –1.0 V for Pulse width ≤50 ns
*2. V_{IH} max = V_{CC} + 1.5 V for Pulse width ≤ 20ns
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
*3. Only defined for DC and long cycle Function Test.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{PP} = V_{CC})

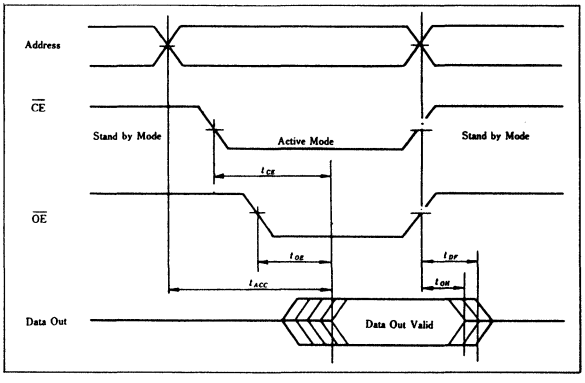
Parameter	Symbol	HN27C256 HG-70		HN27C256 HG-85		Unit	Test Conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	70	–	85	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	70	–	85	ns	$\overline{OE}$= V_{IL}
$\overline{OE}$ to output delay	t_{OE}	–	40	–	45	ns	$\overline{CE}$= V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	30	0	30	ns	$\overline{CE}$= V_{IL}
Address to output hold	t_{OH}	5	–	5	–	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}

Note: t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

Switching Characteristics

Test condition

Input pulse levels . . . . . 0.45 V to 2.4 V
Input rise and fall times . . . . . ≤ 10 ns
Output load . . . . . 1 TTL Gate +100 pF
Reference levels for measuring timing.
Input; 1.5 V
Outputs; 1.5 V



Programming Operation

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0 V to V_{CC}
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = –400 μA
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	–0.1*5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13 V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
*4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
*5. V_{IL} min = –0.6 V.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	–	–	μs	
$\overline{OE}$ setup time	t_{OES}	2	–	–	μs	
Data setup time	t_{DS}	2	–	–	μs	
Address hold time	t_{AH}	0	–	–	μs	
Data hold time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to output float delay	t_{DF}*1	–	–	130	ns	
V_{PP} setup time	t_{VPS}	2	–	–	μs	
$\overline{CE}$ initial programming pulth width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ overprogramming pulse width	t_{OPW}*2	2.85	–	78.75	ms	
V_{CC} setup time	t_{VCS}	2	–	–	μs	
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns	

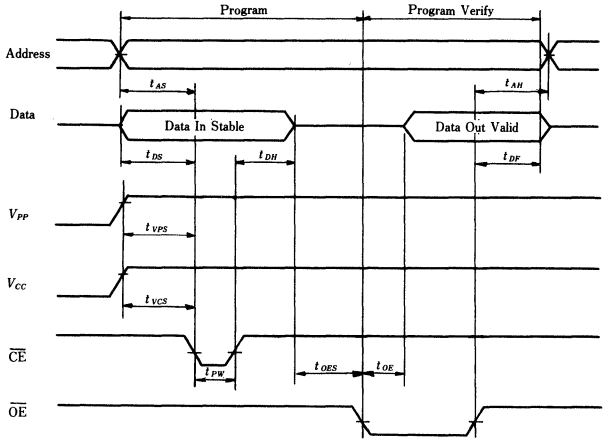
Notes) *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Switching Characteristics

Test condition

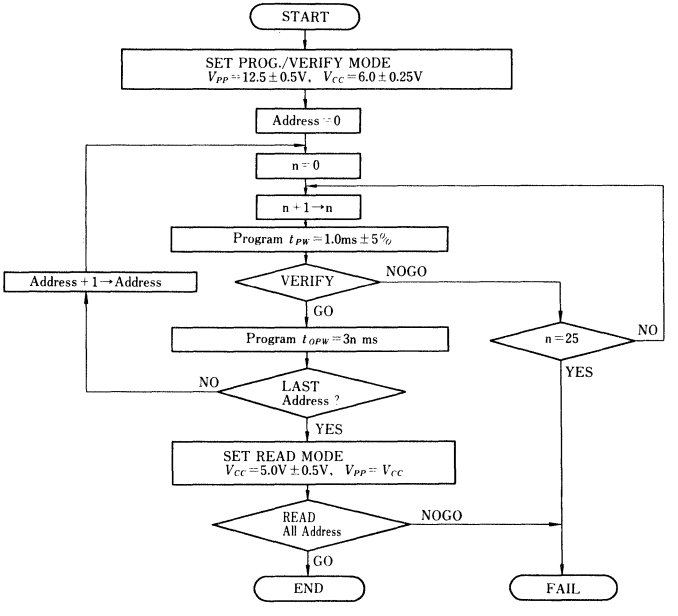
Input pulse levels . . . . . 0.45 V to 2.4 V
Input rise and fall times . . . . . ≤ 20 ns
Reference levels for measuring timing:
Inputs; 1.5 V
Outputs; 1.5 V

Programming Waveforms



High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

Erase

Erasure of HN27C256HG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W.sec/cm^2.

Mode Description

Device Identifier Mode

Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers set write condition by recognizing this code. This function enables effective program.

HN27C256HG Series Identifier Code

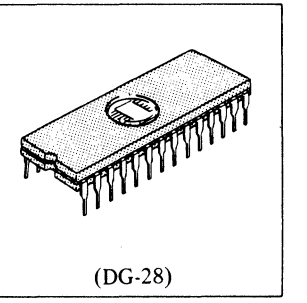
Identifier	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. $A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$

HN27512G Series

65536-word x 8-bit UV Erasable and Programmable ROM

The HN27512G is a 65536-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin, dual-in-line package with transparent window. The transparent window allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.



(DG-28)

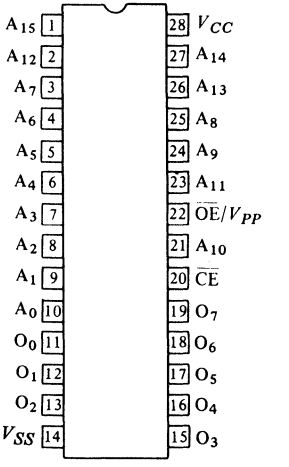
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 250/300ns (max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V (max.)
- Low Stand-by Current . . . . . 40mA (max.)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code

■ ORDERING INFORMATION

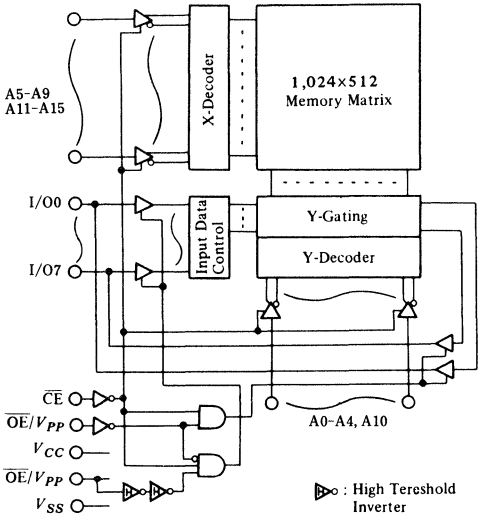
Type No.	Access Time	Package
HN27512G-25	250ns	600 mil 28 pin Cerdip
HN27512G-30	300ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H *2	V_{CC}	Code

Notes) *1. X . . . Don't care
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. with respect to V_{SS}.

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	−	−	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	−	−	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	−	45	100	mA
Input Low voltage	V_{IL}		−0.1*1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	−	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	−	−	V

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

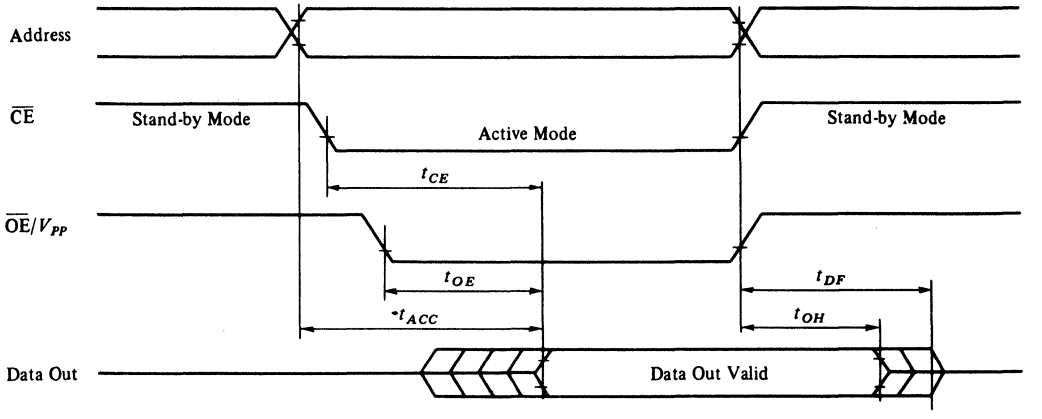
Parameter	Symbol	Test Condition	HN27512G-25		HN27512G-30		Unit
			min.	max.	min.	max.	
Addres to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1 TTL Gate +100pF
Reference Level for Measuring Timing:	0.8V and 2.0V

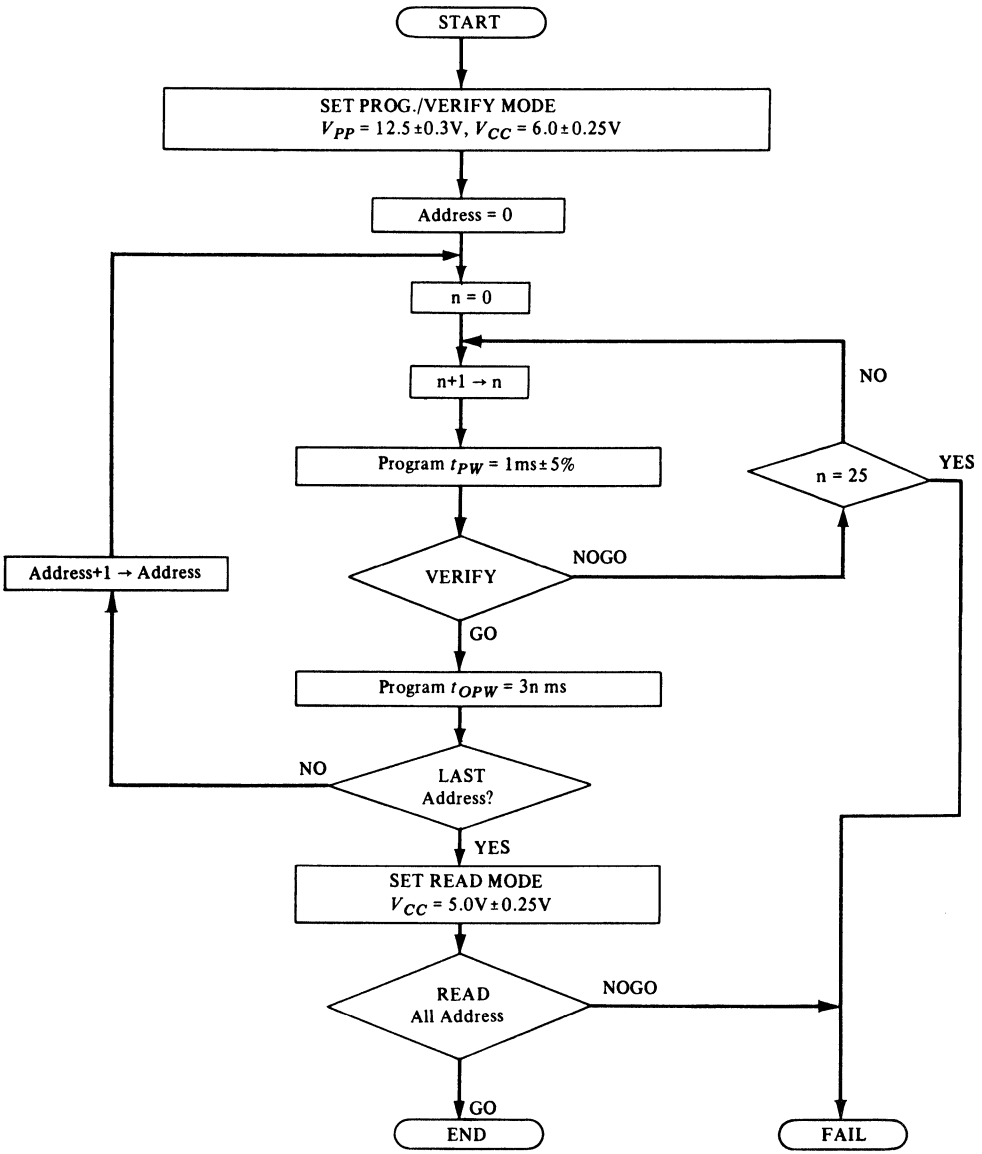


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter		Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	except $\overline{OE}/V_{PP}$	C_{in1}	V_{in} = 0V	–	4	6	pF
	$\overline{OE}/V_{PP}$ Pin	C_{in2}	V_{in} = 0V	–	12	20	pF
Output Capacitance		C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns.
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

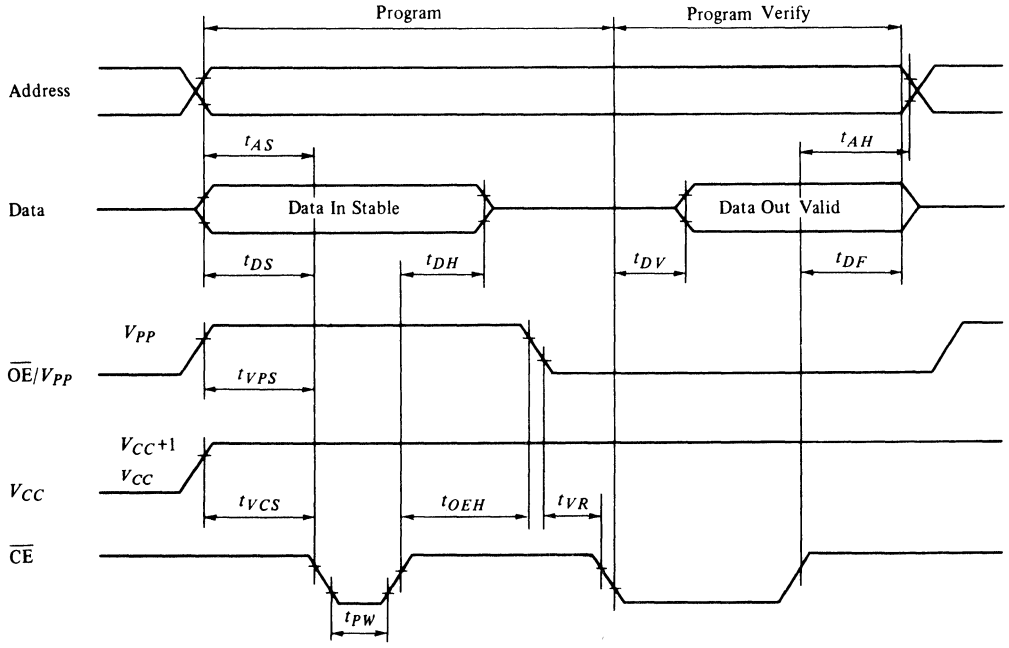
• AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs
$\overline{CE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
V_{PP} Recovery Time	t_{VR}		2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}		–	–	1	μs

Notes) *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flow chart.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ ERASE

Erasure of HN27512G is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W. sec/cm^2.

■ DEVICE IDENTIFIER MODE

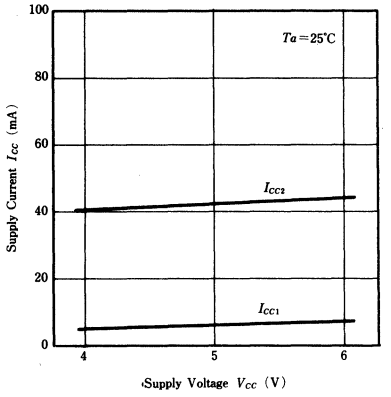
The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

• HN27512G SERIES IDENTIFIER CODE

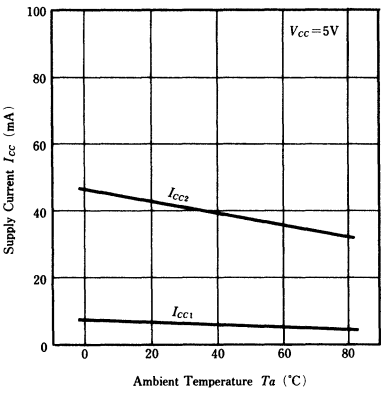
Pins / Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	1	0	1	0	0	94

Notes: 1. A_9 = 12.0 ± 0.5V.
2. A_1 – A_8, A_{10} – A_{15}, $\overline{CE}$, $\overline{OE}/V_{PP}$ = V_{IL}.

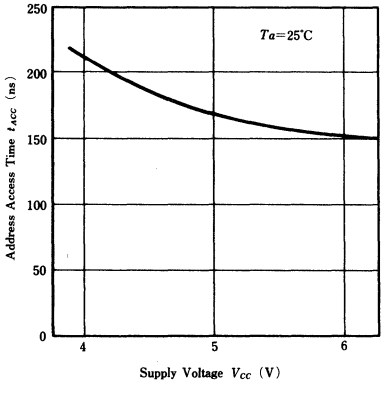
SUPPLY CURRENT vs. SUPPLY VOLTAGE



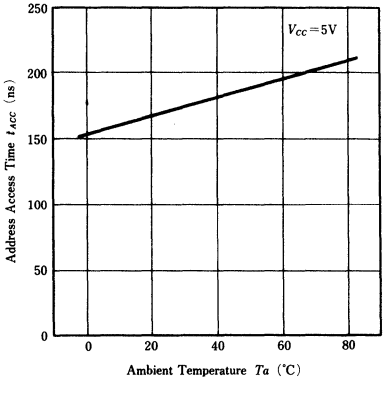
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



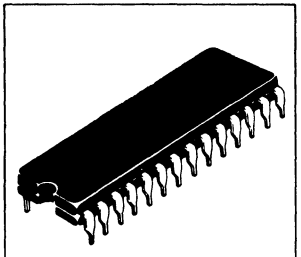
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HN27512P Series

65536-word x 8-bit One Time Electrically Programmable Read Only Memory

The HN27512P is a 65536-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27512P are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic dual-in-line package. Therefore, this device can not be re-written.



(DP-28)

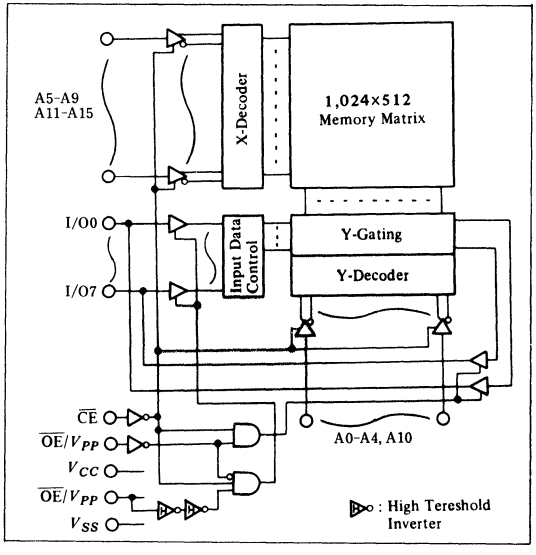
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 250/300ns (max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V (max.)
- Low Stand-by Current . . . . . 40mA (max.)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code.

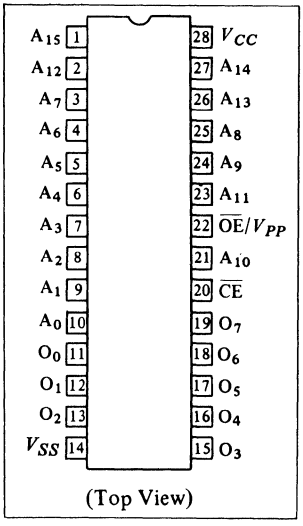
Ordering Information

Part No.	Access	Package
HN27512P-25	250ns	600 mil 28-pin Plastic DIP
HN27512P-30	300ns	

Block Diagram



Pin Arrangement



(Top View)

Pin Description

Pin Name	Function
A0 – A15	Address
O0 – O7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Power Supply
V_{SS}	Ground

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	Code

Notes) *1. X . . . Don't care
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. With respect to V_{SS}

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25/0.45V	−	−	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	−	−	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	−	45	100	mA
Input Low voltage	V_{IL}		−0.1*1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	−	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	−	−	V

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Condition	HN27512P-25		HN27512P-30		Unit
			min.	max.	min.	max.	
Addres to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

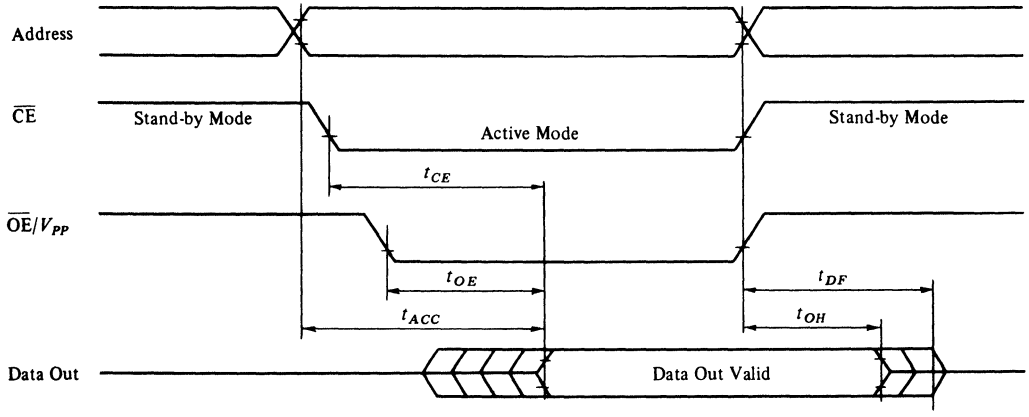
Test Condition

Input Pulse Levels: 0.45V to 2.4V

Input Rise and Fall Time: ≤ 20ns

Output Load: 1 TTL Gate +100pF

Reference Level for Measuring Timing: 0.8V and 2.0V

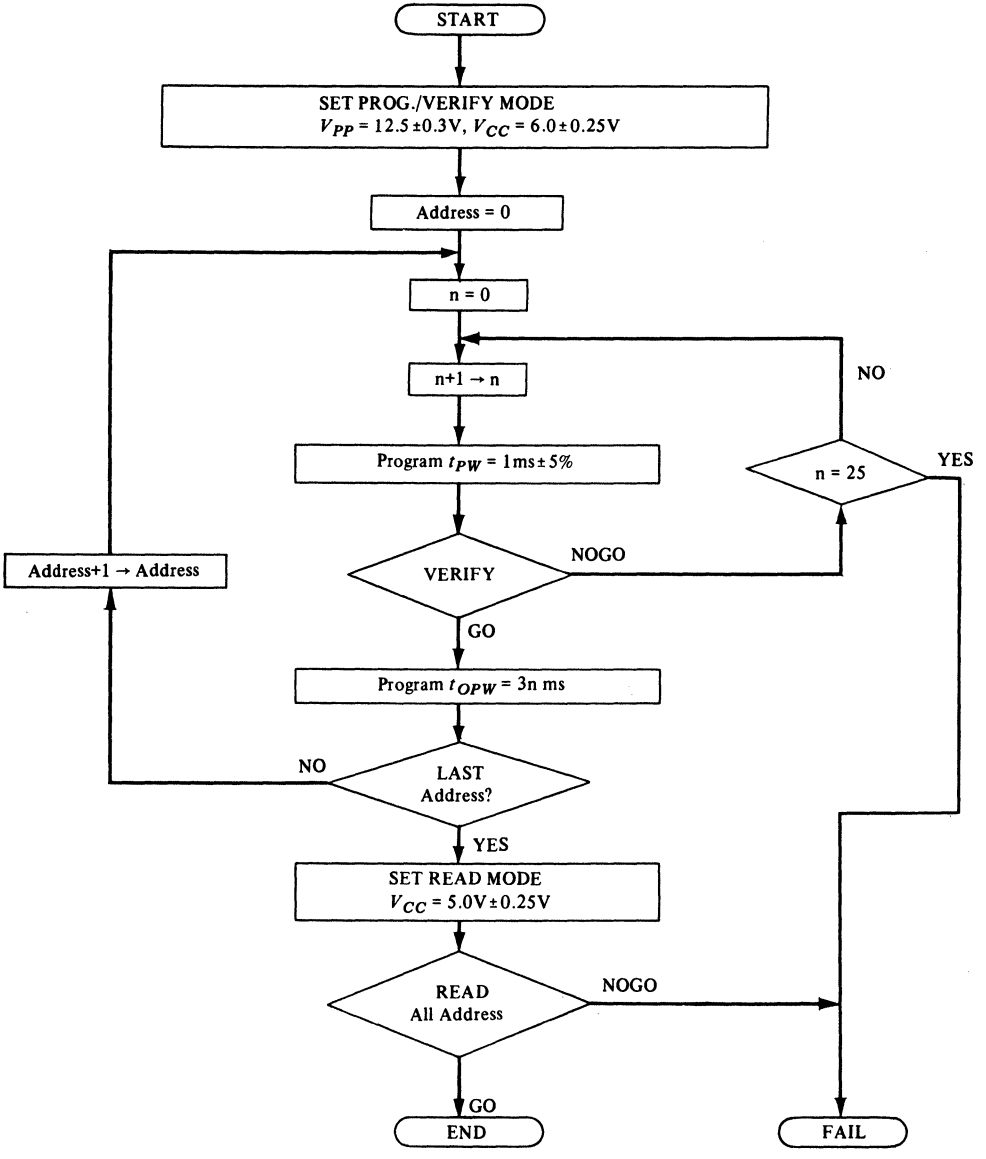


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter		Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	except $\overline{OE}/V_{PP}$	C_{in1}	V_{in} = 0V	–	4	6	pF
	$\overline{OE}/V_{PP}$ Pin	C_{in2}	V_{in} = 0V	–	12	20	pF
Output Capacitance		C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

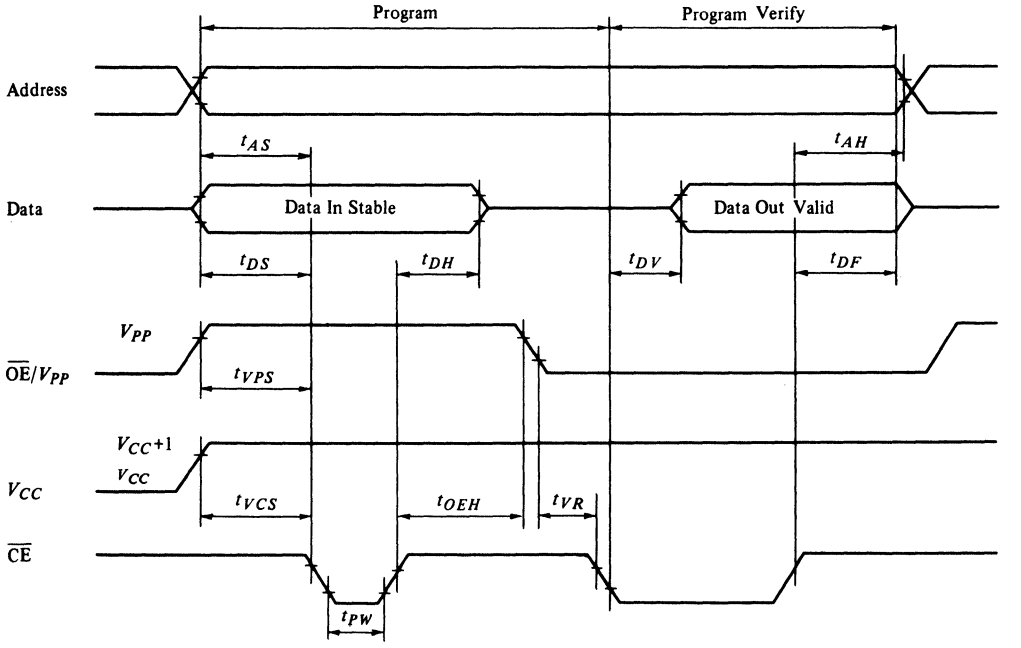
• AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs
$\overline{CE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
V_{PP} Recovery Time	t_{VR}		2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}		–	–	1	μs

Notes) *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flow chart.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

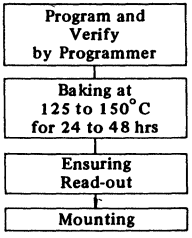
• HN27512P SERIES IDENTIFIER CODE

Identifier \ Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IL}	1	0	0	1	0	1	0	0	94

Notes: 1. $A_9 = 12.0V \pm 0.5V$.
2. $A_1 - A_8, A_{10} - A_{15}, \overline{CE}, \overline{OE}/V_{PP} = V_{IL}$.

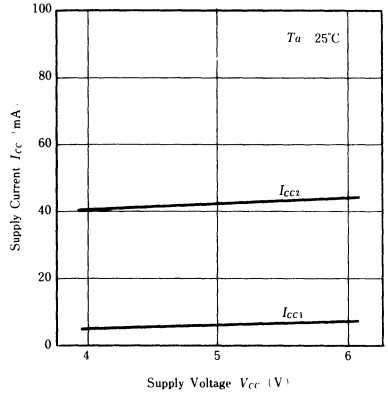
■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.

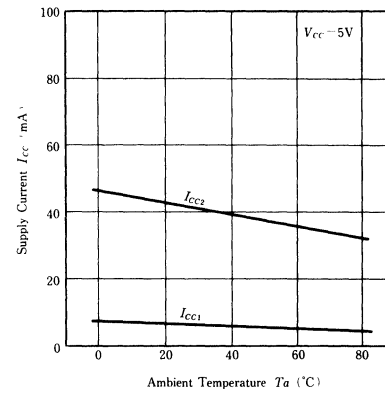


Recommended Screening conditions

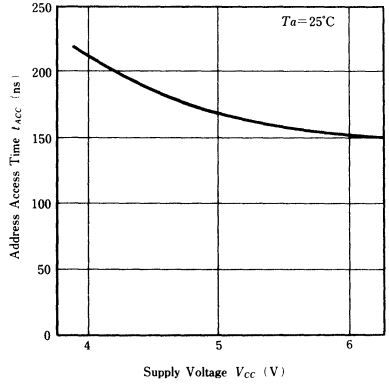
SUPPLY CURRENT vs. SUPPLY VOLTAGE



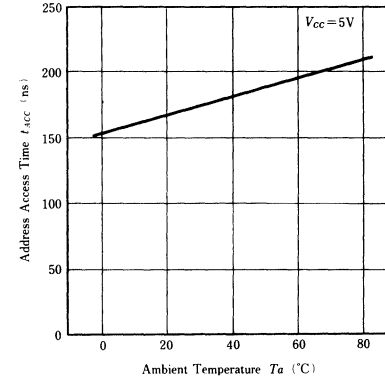
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



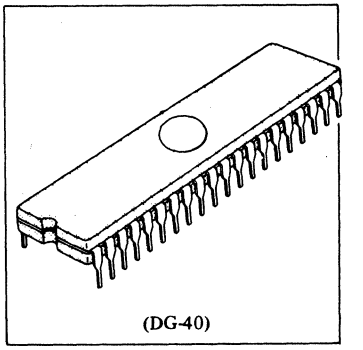
HN27C1024G Series —Under Development

65536-word x 16-bit CMOS UV Erasable and Programmable ROM

The Hitachi HN27C1024G is a 1-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation.

Fabricated on new advanced fine process and high speed circuitry technique, the HN27C1024G with 65536 word x 16 bit organization makes high speed access time possible. Therefore, it is suitable for 16 bit micro-computer systems such as the 8086 and 68000.

The HN27C1024G offers high speed programming using page programming mode.

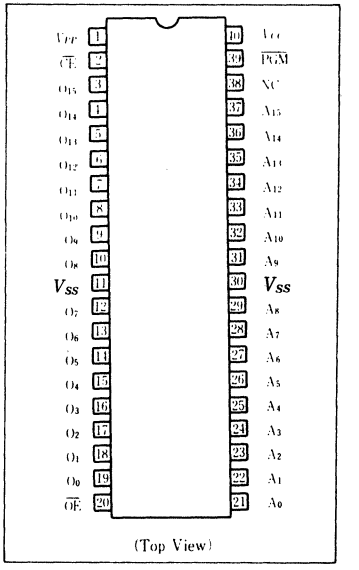


(DG-40)

Features

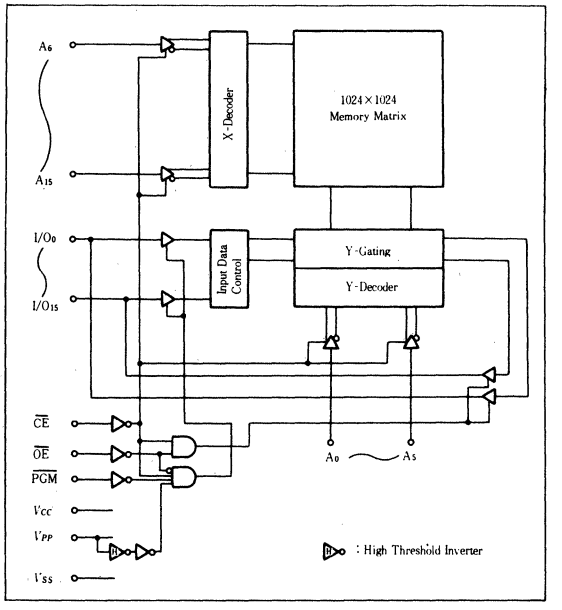
- High performance programming mode and
  High performance page programming mode
  - Programming voltage +12.5 V DC
  - High speed page programming
  - 14 sec typical
- High speed
  - Access time 100/120ns (maximum)
- Inputs and Outputs TTL compatible during both read and program
- Low power dissipation
  - 60mW/MHz typical
- JE DEC standard

Pin Arrangement



(Top View)

Block Diagram



Pin Description

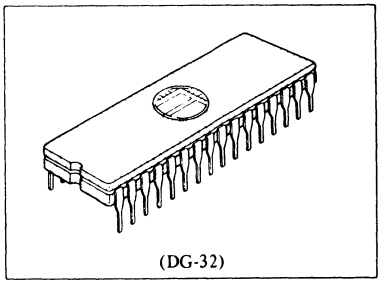
Pin Name	Punction
A0 – A15	Address
O0 – O15	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Power Supply
V_{SS}	Ground
$\overline{PGM}$	Programming Enable
NC	No Connection

HN27C101G Series

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Program Mode and High Performance Page Program Mode . . . . . Program Voltage: +12.5V DC . . . . . High Performance Programming Available
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 170/200/250ns (max.)
- Low power Dissipation . . 50mW/MHz typ. (Active Mode) 5μW typ. (Standby Mode)
- Pin Arrangement . . . . . 32 Pin JEDEC Standard

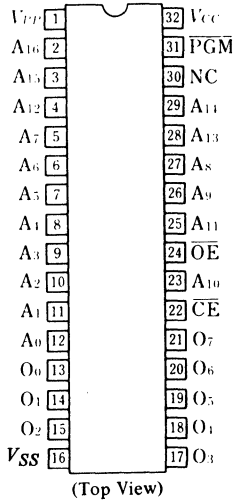


(DG-32)

■ ORDERING INFORMATION

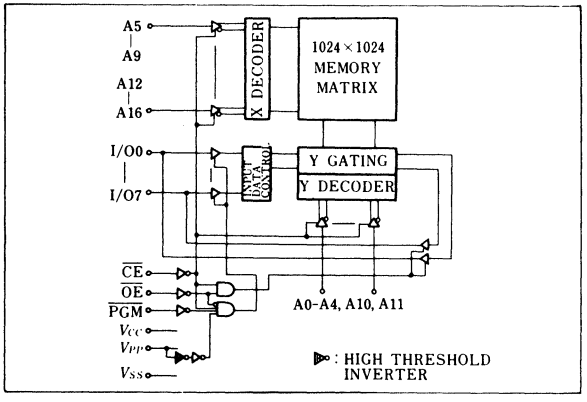
Type No.	Access Time	Package
HN27C101G-17	170ns	600 mil 32 pin Cerdip
HN27C101G-20	200ns	
HN27C101G-25	250ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13~15, 17~21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Notes) 1. X: Don't care
2. 30 pin should be connected to 32 pin.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

• DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.5V	–	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE}$=V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$=V_{CC} ±0.3V	–	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{out}=0mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0mA	–	–	30	mA
	I_{CC3}	f=1MHz, I_{out}=0mA	–	–	15	mA
Input Low Voltage	V_{IL}		−0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

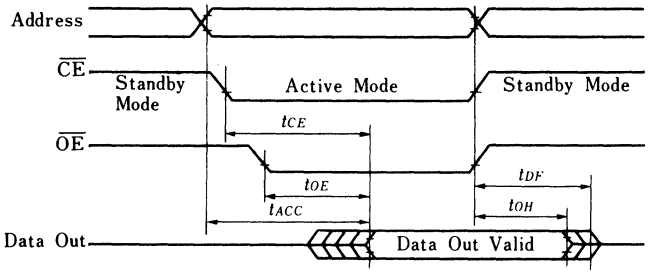
Parameter	Symbol	Test Conditions	HN27C101G-17		HN27C101G-20		HN27C101G-25		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	70	10	70	10	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	0	–	ns

Note) t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

• Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

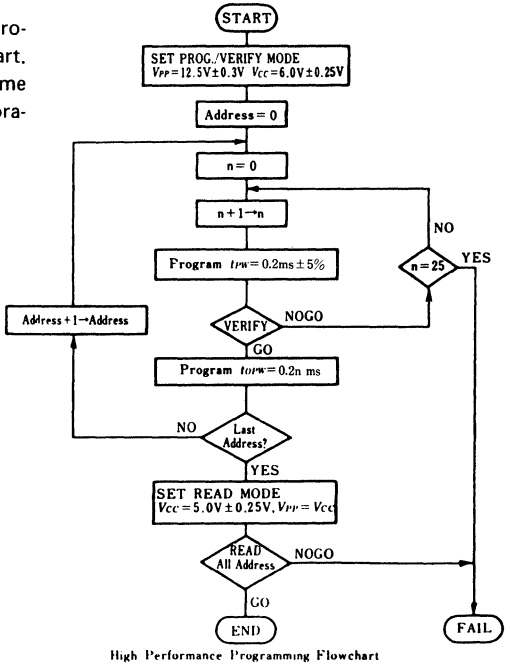


- **CAPACITANCE** (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	10	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	15	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$=V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

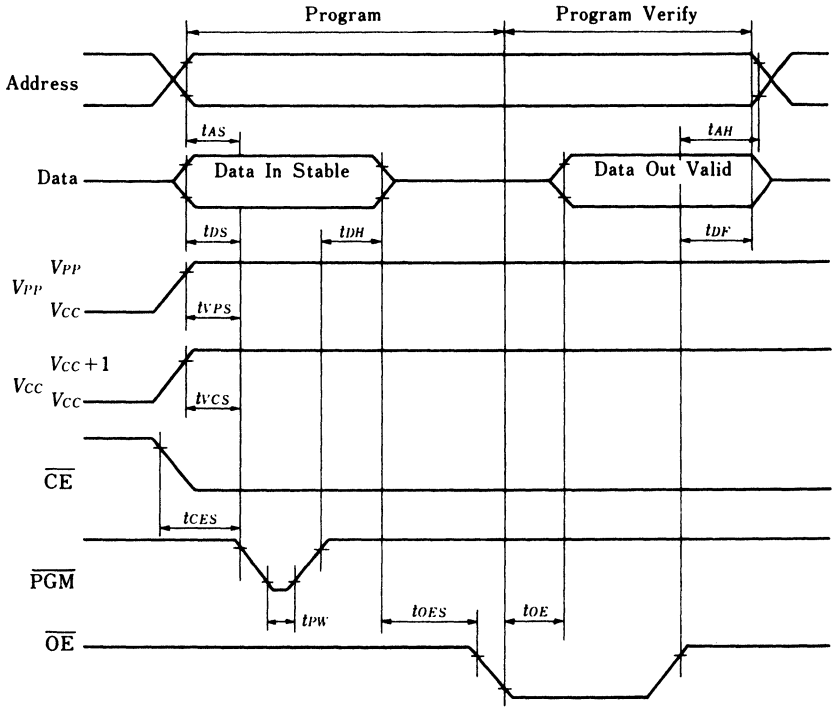
• AC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

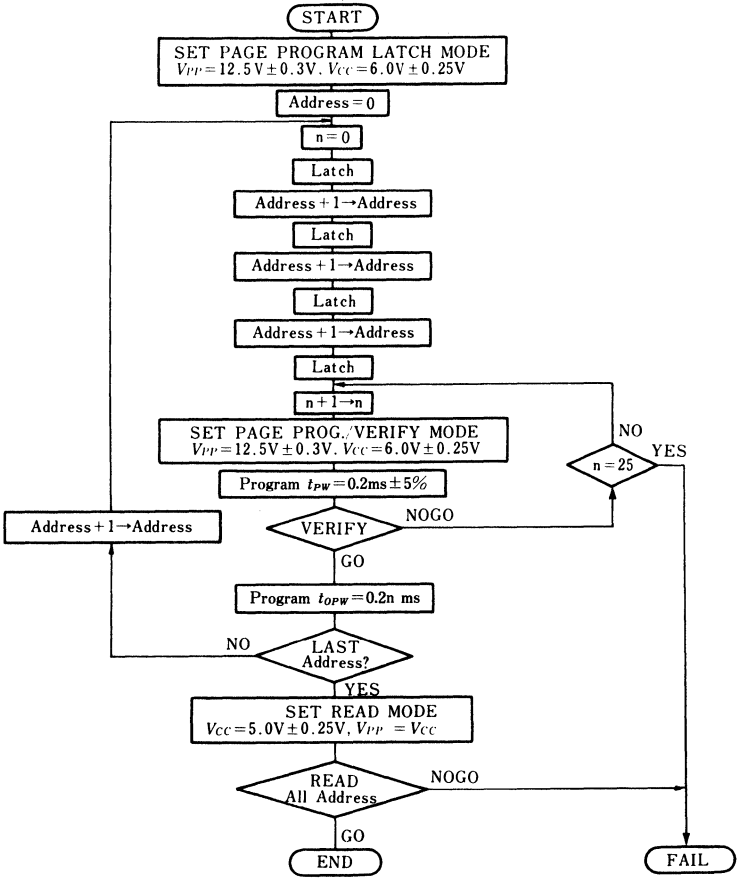
• SWITCHING CHARACTERISTICS

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



■ HIGH PERFORMANCE PAGE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

● DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH}= –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{OE}$=V_{IH}, $\overline{PGM}$=V_{IL}	–	–	50	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS

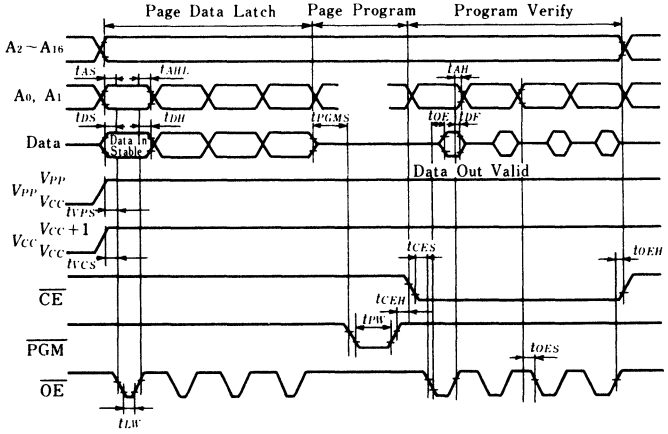
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	µs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	µs
Data Setup Time	t_{DS}		2	–	–	µs
Address Hold Time	t_{AH}		0	–	–	µs
	t_{AHL}		2	–	–	µs
Data Hold Time	t_{DH}		2	–	–	µs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	µs
V_{CC} Setup Time	t_{VCS}		2	–	–	µs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	µs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}		1	–	–	µs
$\overline{PGM}$ Setup Time	t_{PGMS}		2	–	–	µs
$\overline{CE}$ Hold Time	t_{CEH}		2	–	–	µs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	µs

Notes) *1. t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

• SWITCHING CHARACTERISTICS

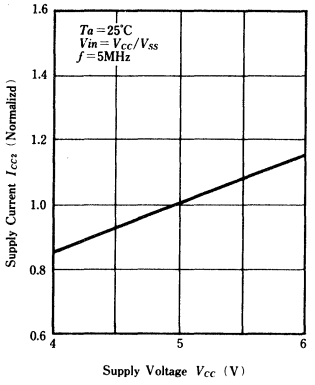
• **Test Condition** Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



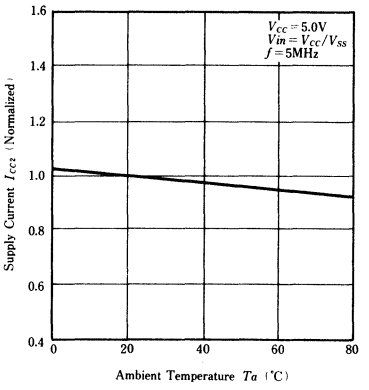
■ ERASE

Erasure of HN27C101G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W•sec/cm^2

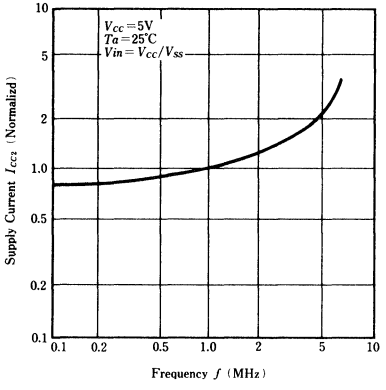
SUPPLY CURRENT vs. SUPPLY VOLTAGE



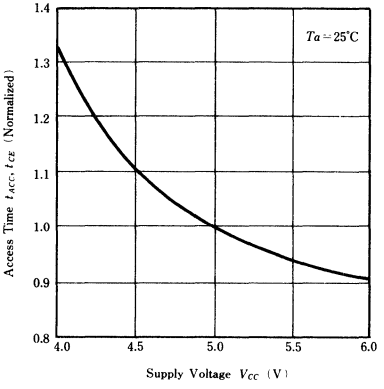
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



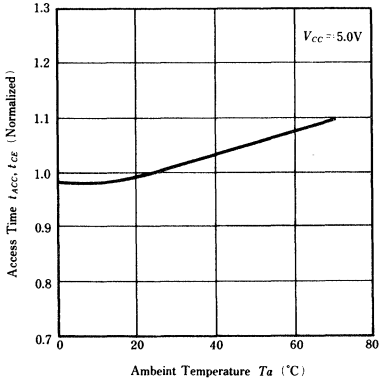
SUPPLY CURRENT vs. FREQUENCY



ACCESS TIME vs. SUPPLY VOLTAGE



ACCESS TIME vs. AMBIENT TEMPERATURE



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

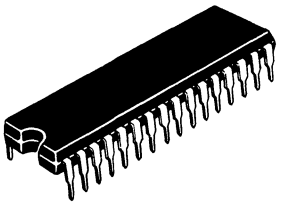
HN27C101P Series

131072-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C101P Series are 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C101P/FP series are in the "1" state (output high).

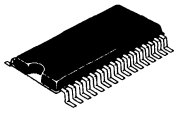
Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in 32 pin plastic package, therefore, this device cannot be rewritten and erased.

HN27C101Pシリーズ



(DP-32)

HN27C101FPシリーズ



(FP-32D)

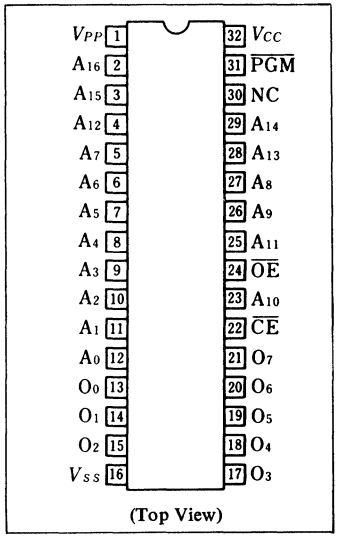
Features

- High speed
  - Access time . . . . . 200/250 ns (max.)
- Low power dissipation
  - Active mode 50 mW/MHz (typ.)
  - Standby mode 5 μW (typ.)
- Single power supply . . . . . +5 V ± 5%
- High performance program mode and high performance page program mode
  - Program voltage: +12.5 V DC
  - High performance programming available
- Static . . . . . No clocks required
- Inputs and outputs TTL compatible during both read and program modes

Ordering Information

Type No.	Access time	Package
HN27C101P-20	200ns	600 mil 32 pin
HN27C101P-25	250ns	Plastic DIP
HN27C101FP-20	200ns	32 pin
HN27C101FP-25	250ns	Plastic SOP

Pin Arrangement

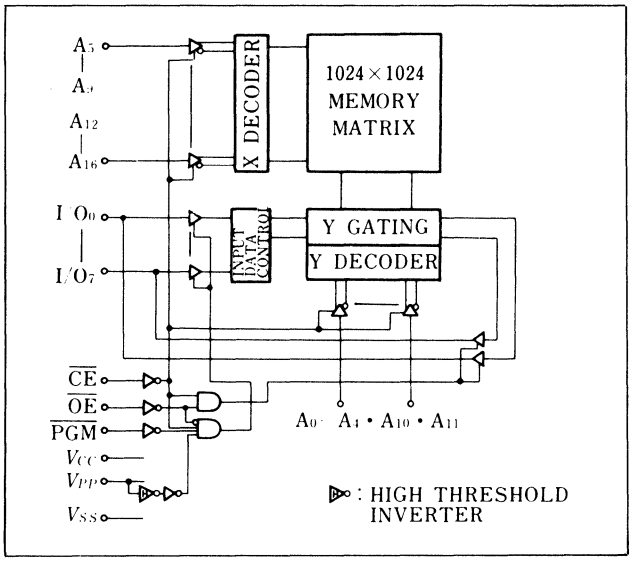


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
O0 – O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



■ Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Notes) 1. X: Don't care.
2. 30 pin should be connected to 32 pin.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} voltage*1	V_{CC}	−0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0 V for pulse width ≦ 50 ns

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 5.25V
Output Leakage Current	I_{LO}	–	–	2	μA	V_{out} = 5.25V/0.45V
V_{PP} Current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
V_{CC} Current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ±0.3V
V_{CC} Current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, I_{out} = 0mA
	I_{CC2}	–	–	30	mA	f = 5 MHz, I_{out} = 0mA
	I_{CC3}	–	–	15	mA	f = 1 MHz, I_{out} = 0mA
Input Low Voltage	V_{IL}	–0.3*1	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	V_{CC}+1*2	V	
Output Low Voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –400μA

Notes) *1. –1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

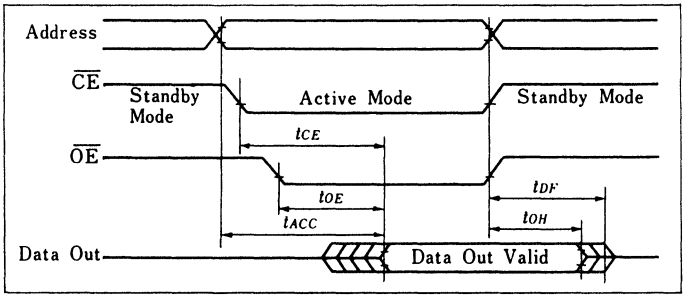
Item	Symbol	HN27C101-20		HN27C101-25		Unit	Test conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	200	–	250	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	200	–	250	ns	$\overline{OE}$=V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	70	10	100	ns	$\overline{CE}$=V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	60	ns	$\overline{CE}$=V_{IL}
Address to output hold	t_{OH}	0	–	0	–	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}

Note) t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

Switching Characteristics

Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

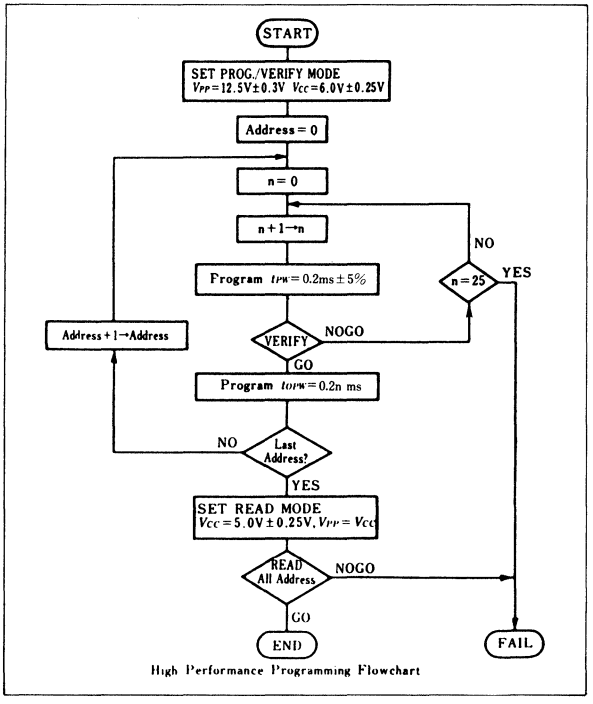


Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Capacitance	C_{in}	–	–	10	pF	V_{in} = 0V
Output Capacitance	C_{out}	–	–	15	pF	V_{out} = 0V

High Performance Programming

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5 V ± 0.3V)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

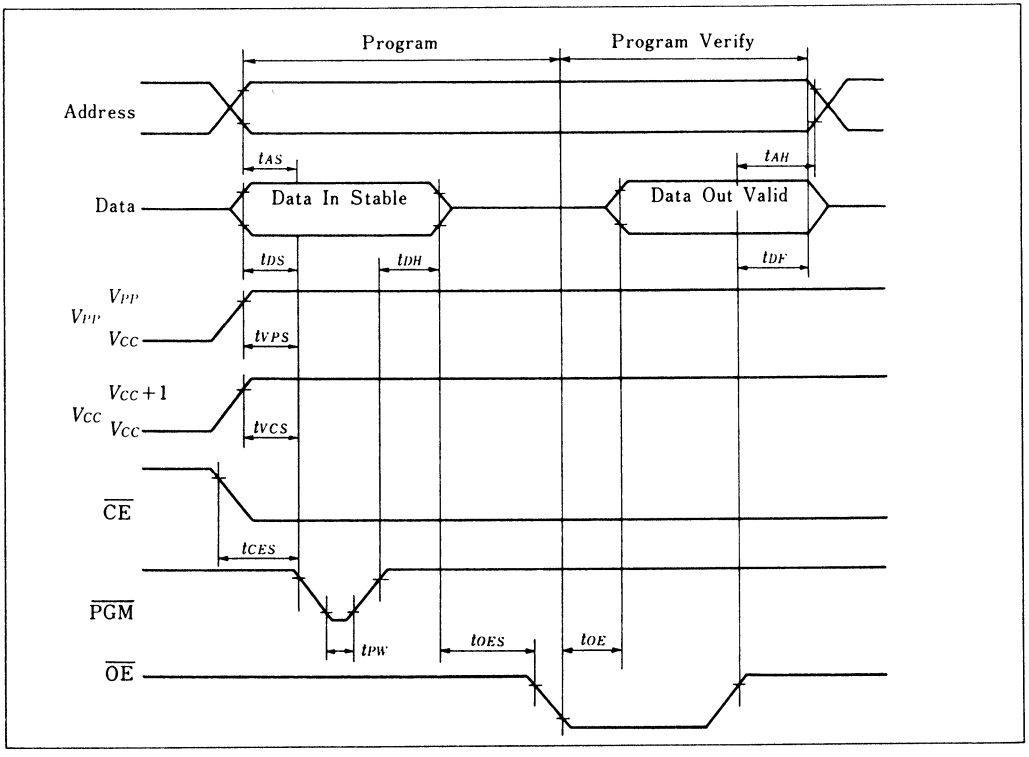
($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from OE	t_{OE}	0	–	150	ns	

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

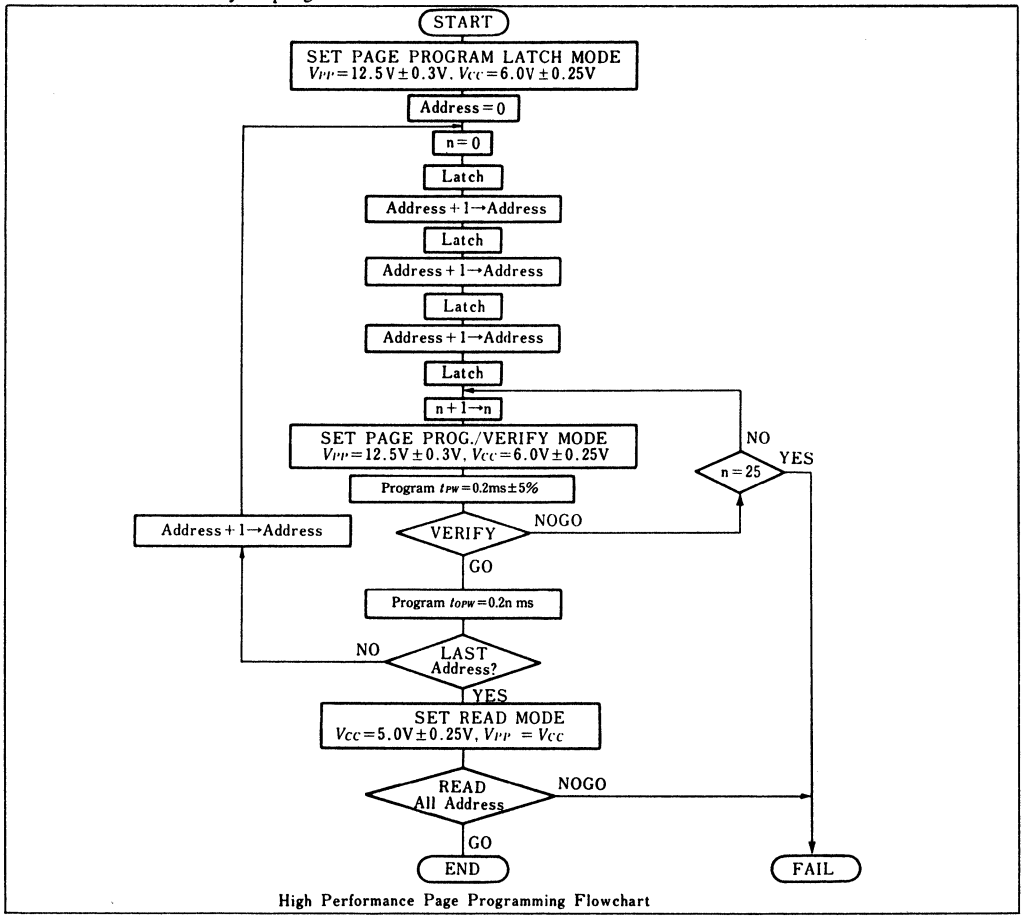
Switching Characteristics

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



High Performance Page Programming

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

DC Programming Characteristics ($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	50	mA	$\overline{CE} = \overline{OE} = V_{IH}$, PGM = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

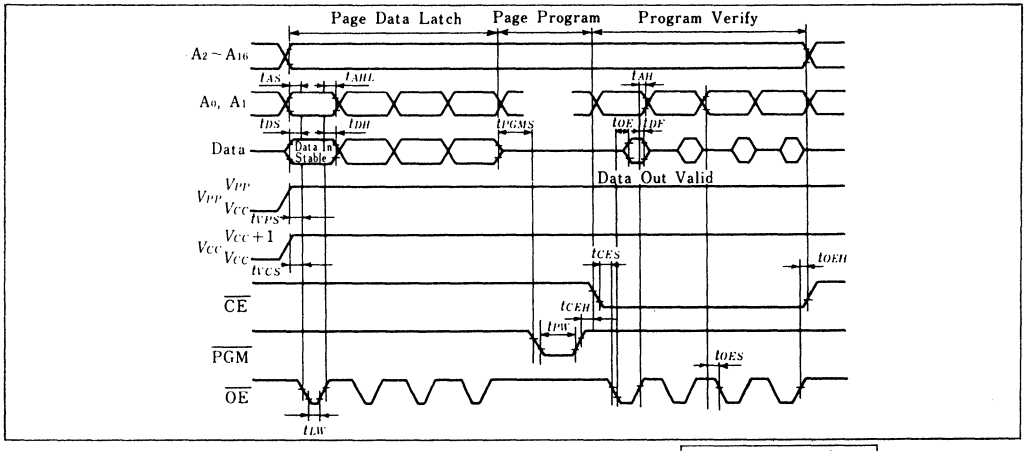
Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
	t_{AHL}	2	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from $\overline{OE}$	t_{OE}	0	–	150	ns	
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}	1	–	–	μs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	–	–	μs	
$\overline{CE}$ Hold Time	t_{CEH}	2	–	–	μs	
$\overline{OE}$ Hold Time	t_{OEH}	2	–	–	μs	

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

Switching Characteristics

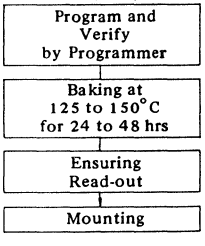
Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



Recommended Screening Conditions

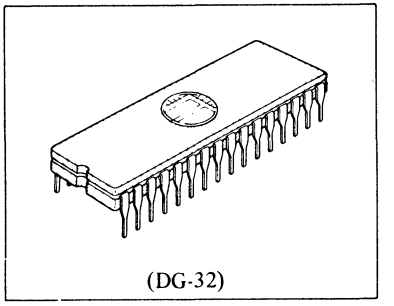
Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

HN27C301G Series

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM


(DG-32)

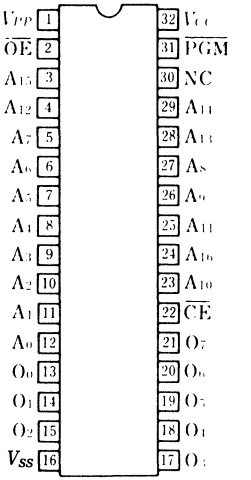
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Program Mode and High Performance Page Program Mode . . . . . Program Voltage: +12.5V DC . . . . . High Performance Programming Available
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 170/200/250ns (max.)
- Low power Dissipation . . 50mW/MHz typ. (Active Mode) 5μW typ. (Standby Mode)
- Pin Compatible with 1Mbit MASK ROM (28pin type)

■ ORDERING INFORMATION

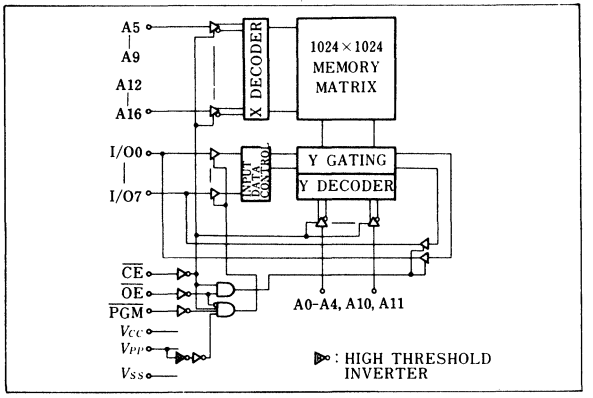
Type No.	Access Time	Package
HN27C301G-17	170ns	600 mil 32 pin Cerdip
HN27C301G-20	200ns	
HN27C301G-25	250ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (2)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32, 30)*	Outputs (13~15, 17~21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Notes) *1. X: Don't care
*2. 30 pin should be connected to 32 pin.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}.
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

● DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.5V	–	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE}$=V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$=V_{CC} ±0.3V	–	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{out}=0mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0mA	–	–	30	mA
	I_{CC3}	f=1MHz, I_{out}=0mA	–	–	15	mA
Input Low Voltage	V_{IL}		−0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

● AC CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

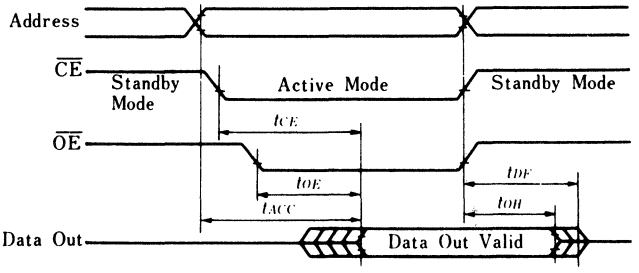
Parameter	Symbol	Test Conditions	HN27C301G-17		HN27C301G-20		HN27C301G-25		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	10	70	10	70	10	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = OE = V_{IL}	0	–	0	–	0	–	ns

Note) t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

● **Test Condition**

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

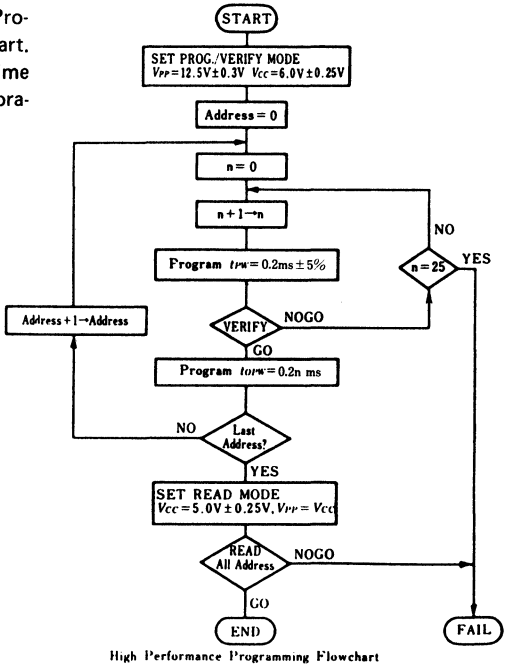


- **CAPACITANCE** (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	10	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	15	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$=V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

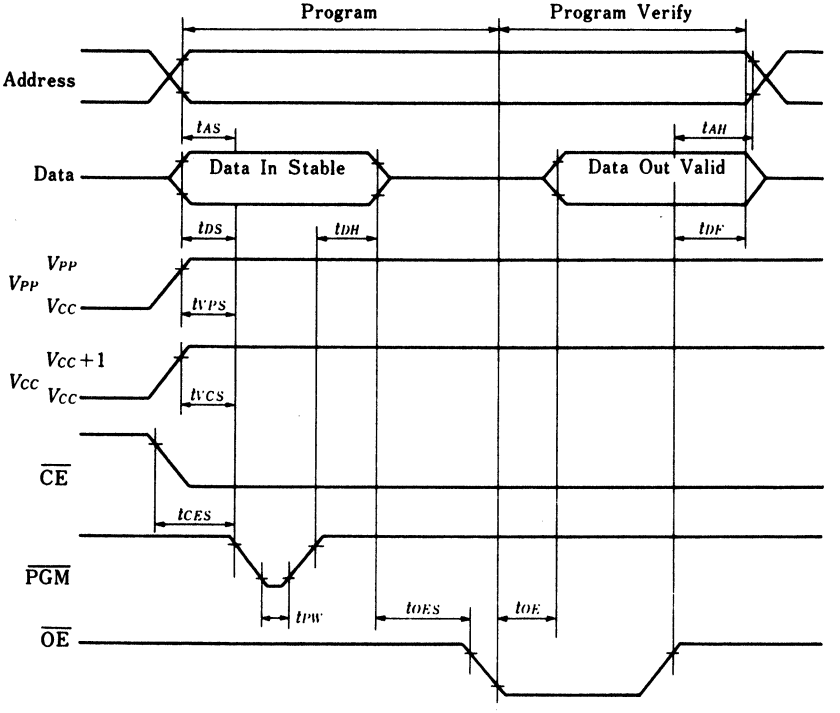
• AC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

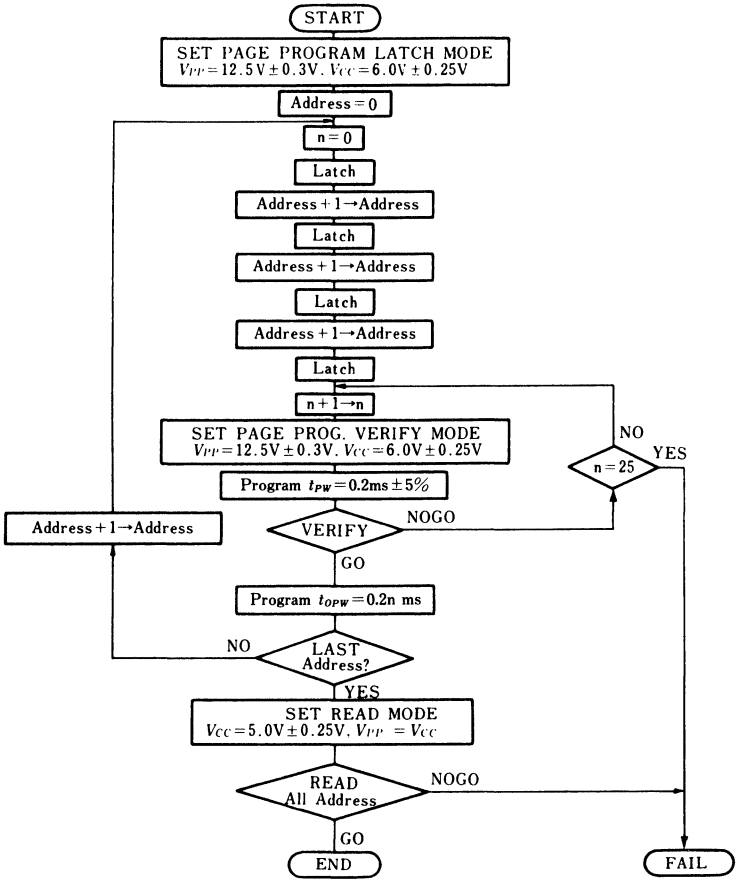
• SWITCHING CHARACTERISTICS

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



■ HIGH PERFORMANCE PAGE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH}= –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{OE}$=V_{IH}, $\overline{PGM}$=V_{IL}	–	–	50	mA

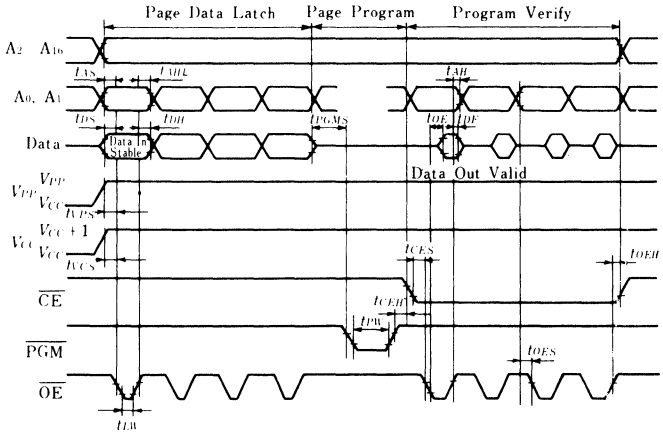
Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS (High Performance Page Programming)
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Adress Hold Time	t_{AH}		0	–	–	μs
	t_{AHL}		2	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}		1	–	–	μs
$\overline{PGM}$ Setup Time	t_{PGMS}		2	–	–	μs
$\overline{CE}$ Hold Time	t_{CEH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

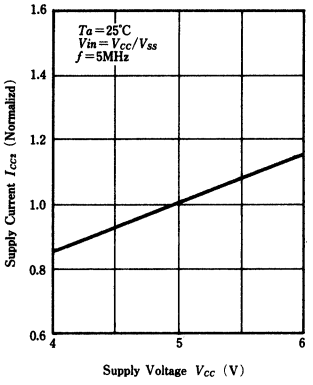
- **SWITCHING CHARACTERISTICS**
- **Test Condition** Input Pulse Levels: 0.45V to 2.4V
  Input Rise and Fall Time: ≤ 20ns
  Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V



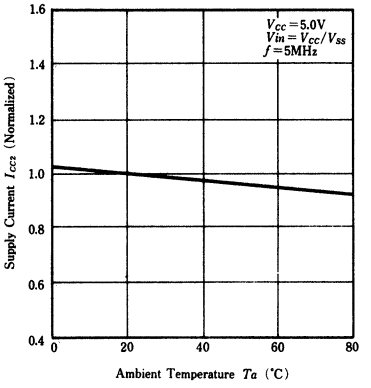
■ ERASE

Erasure of HN27C301G is performed by exposure to ultraviolet light of 2537 Å and all the output data data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm^2

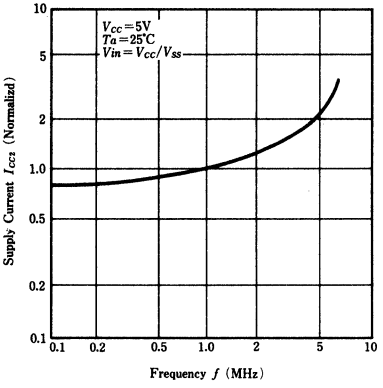
SUPPLY CURRENT vs. SUPPLY VOLTAGE



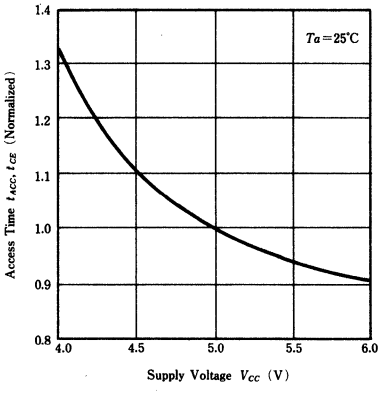
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



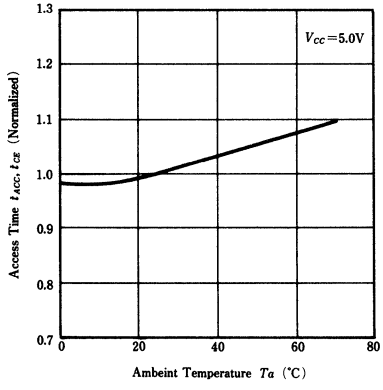
SUPPLY CURRENT vs. FREQUENCY



ACCESS TIME vs. SUPPLY VOLTAGE



ACCESS TIME vs. AMBIENT TEMPERATURE



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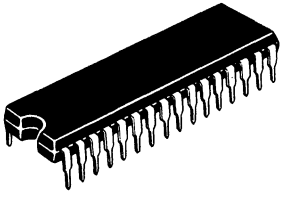
HN27C301P

131072-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C301P Series are 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C301P/FP Series are in the "1" state (output high).

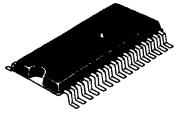
Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32 pin plastic package, therefore, this device cannot be rewritten and erased.

HN27C301P Series



(DP-32)

HN27C301FP Series



(FP-32D)

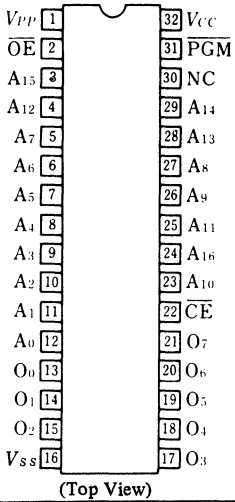
Features

- High speed
  - Access time . . . . . 200/250 ns (max.)
- Low power dissipation
  - Active mode 50 mW/MHz (typ.)
  - Standby mode 5 μW (typ.)
- Single power supply +5V ± 5%
- High performance program mode and high performance page program mode
  - Program voltage: +12.5 V DC
  - High performance programming available
- Static . . . . . No clocks required
- Inputs and output TTL compatible during both read and program modes.

Ordering Information

Type No.	Access time	Package
HN27C301P-20	200ns	600 mil 32 pin
HN27C301P-25	250ns	Plastic DIP
HN27C301FP-20	200ns	32 pin
HN27C301FP-25	250ns	Plastic SOP

Pin Arrangement

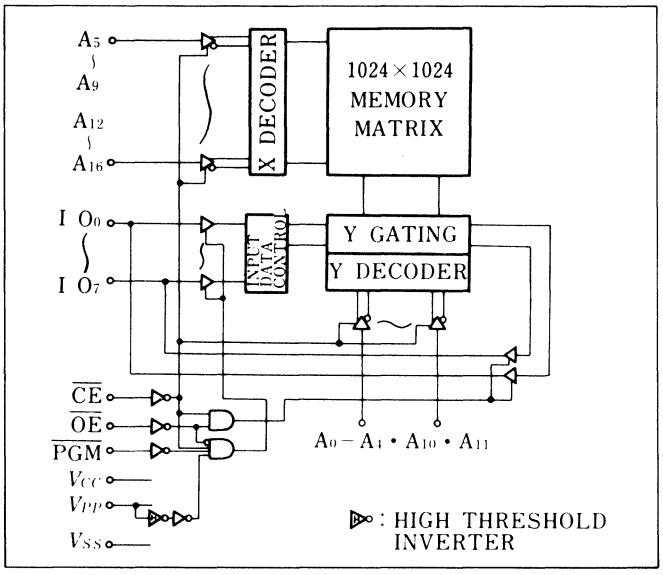


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
O0 – O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



■ Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Notes) 1. X: Don't care.
2. 30 pin should be connected to 32 pin.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	V_{in}, V_{out}	–0.6*2 to +7.0	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.0	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	–55 to +125	°C
Storage temperature range under bias	T_{bias}	–10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. –1.0 V for pulse width ≦ 50 ns

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Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 5.25V
Output Leakage Current	I_{LO}	–	–	2	μA	V_{out} = 5.25V/0.45V
V_{PP} Current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
V_{CC} Current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ±0.3V
V_{CC} Current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = $\overline{V_{IL}}$, I_{out} = 0mA
	I_{CC2}	–	–	30	mA	f = 5 MHz, I_{out} = 0mA
	I_{CC3}	–	–	15	mA	f = 1 MHz, I_{out} = 0mA
Input Low Voltage	V_{IL}	−0.3*1	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	V_{CC}+1*2	V	
Output Low Voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −400μA

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

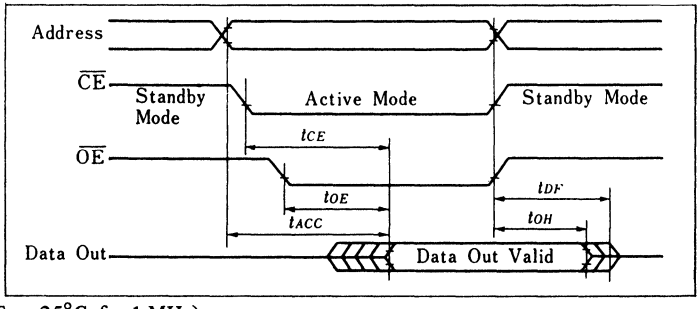
Item	Symbol	HN27C301P-20		HN27C301P-25		Unit	Test conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	200	–	250	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	200	–	250	ns	$\overline{OE}$= V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	70	10	100	ns	$\overline{CE}$= V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	60	ns	$\overline{CE}$= V_{IL}
Address to output hold	t_{OH}	0	–	0	–	ns	$\overline{CE}$=$\overline{OE}$= V_{IL}

Note) t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

Switching Characteristics

Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

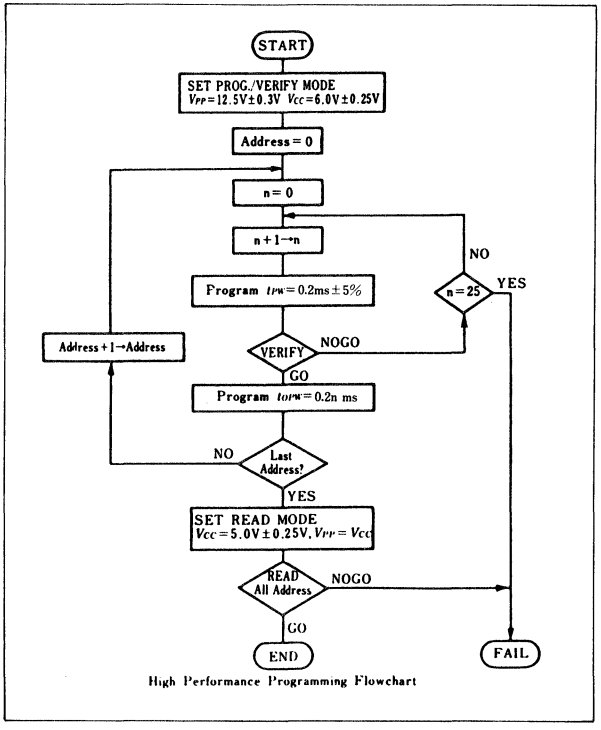


Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Capacitance	C_{in}	–	–	10	pF	V_{in} = 0V
Output Capacitance	C_{out}	–	–	15	pF	V_{out} = 0V

High Performance Programming

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1 *5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5 *6	V	
V_{PP} Supply Current	I_{PP}	–	–	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

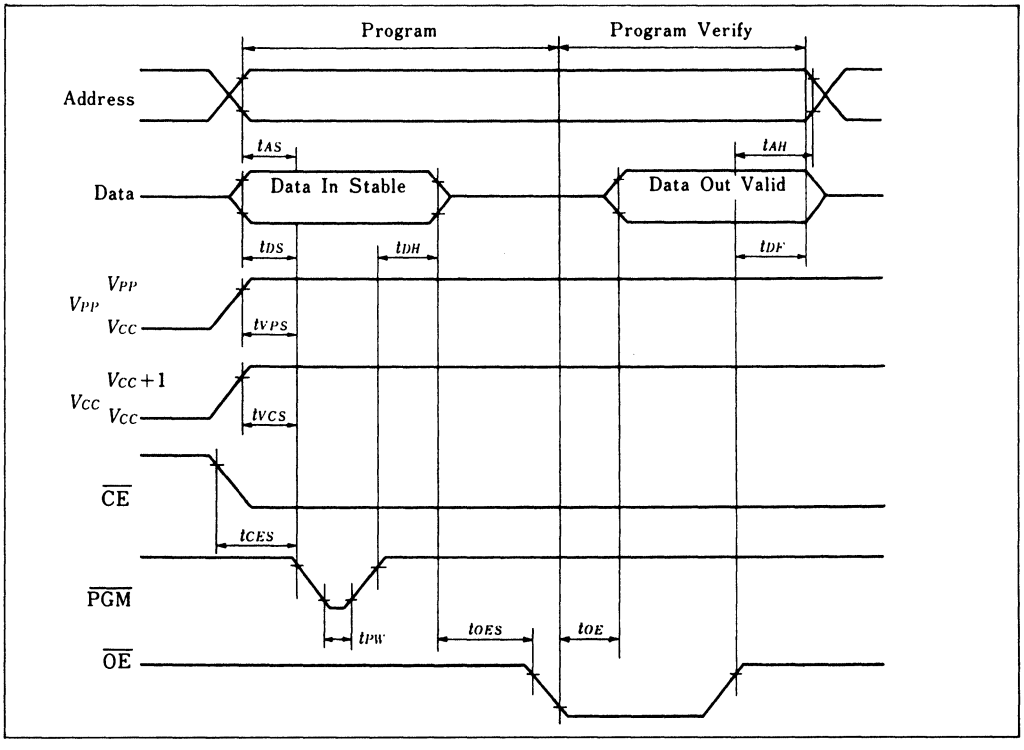
($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from OE	t_{OE}	0	–	150	ns	

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

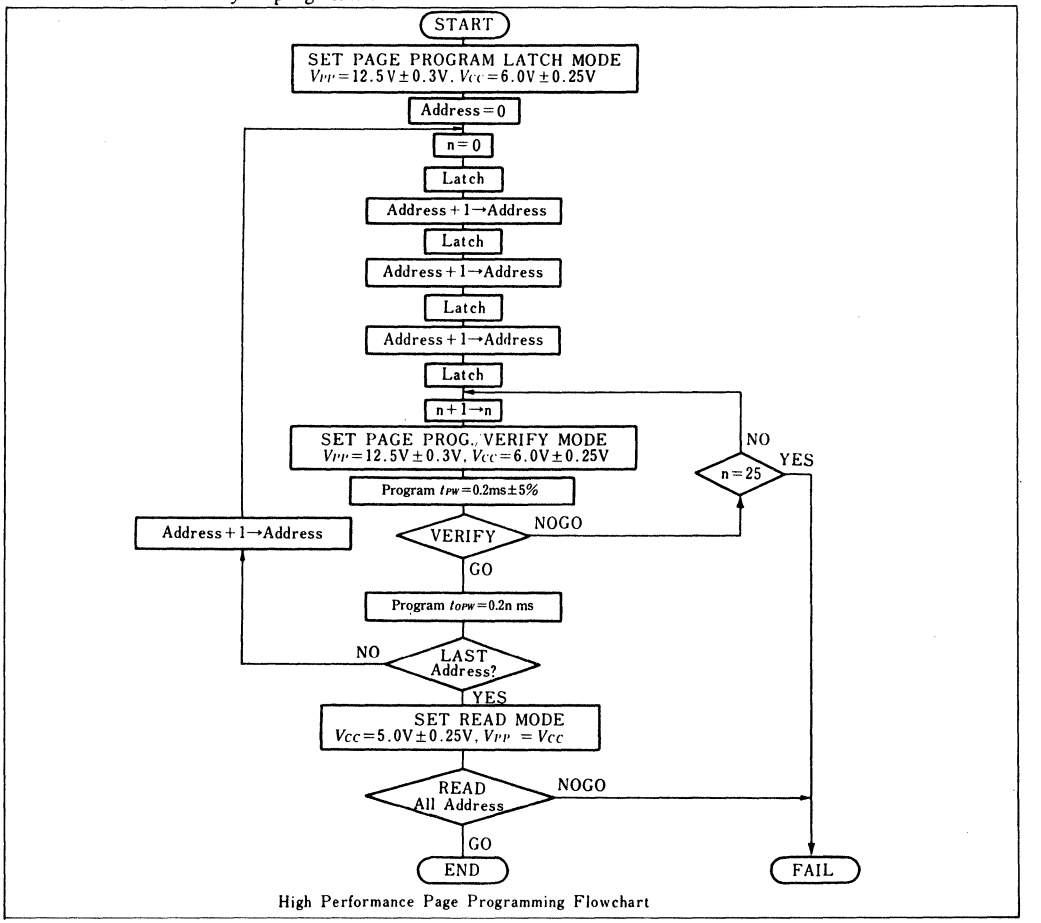
Switching Characteristics

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



High Performance Page Programming

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

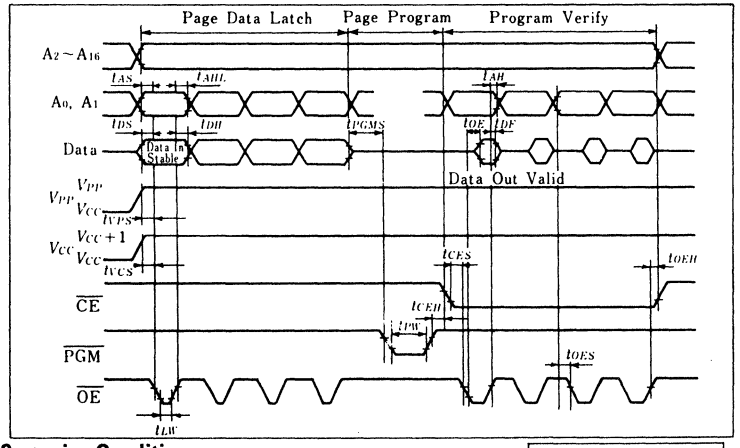
Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
	t_{AHL}	2	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from $\overline{OE}$	t_{OE}	0	–	150	ns	
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}	1	–	–	μs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	–	–	μs	
$\overline{CE}$ Hold Time	t_{CEH}	2	–	–	μs	
$\overline{OE}$ Hold Time	t_{OEH}	2	–	–	μs	

Notes) *1. t_{DF} defines the time at which the output acheives the open circuit condition and data is no longer driven.
*2. t_{OPW} is defined as mentioned in flowchart.

Switching Characteristics

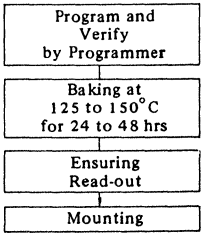
Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.



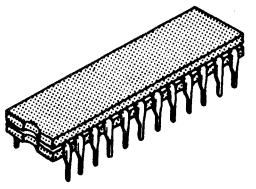
Recommended Screening conditions

ECL RAM

HM10422

256-word×4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.
Four active Low Block Select lines are provided to select each block independently.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

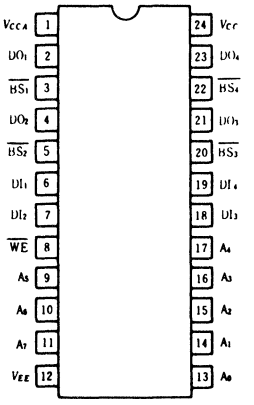


(DG-24N)

■FEATURES

- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



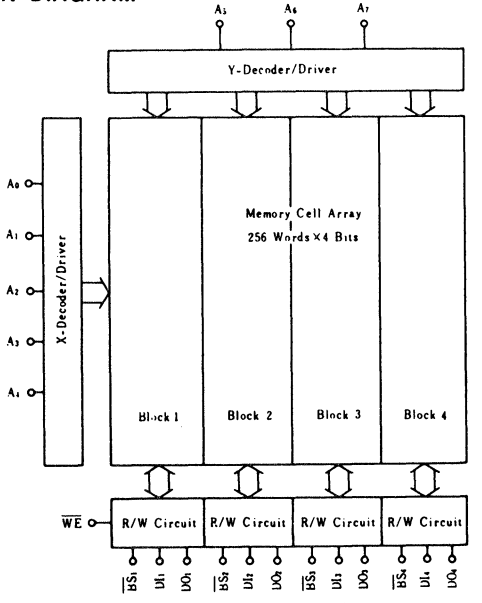
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read out noninvert

■BLOCK DIAGRAM



HITACHI

Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−200	−160	—	mA
			Ta = 75°C	—	−145	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} − 2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W − 6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	12	ns

3. RISE/FALL TIME

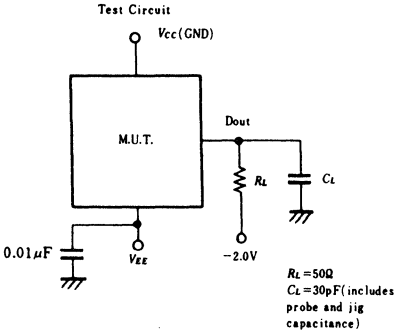
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

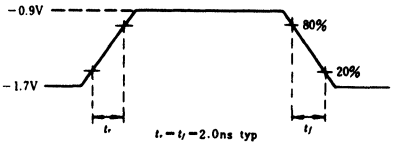
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

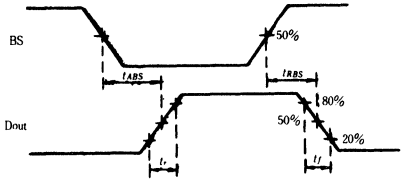
1. LOADING CONDITION

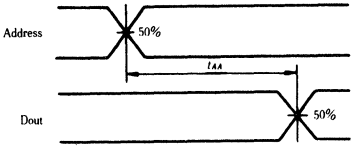


2. INPUT PULSE

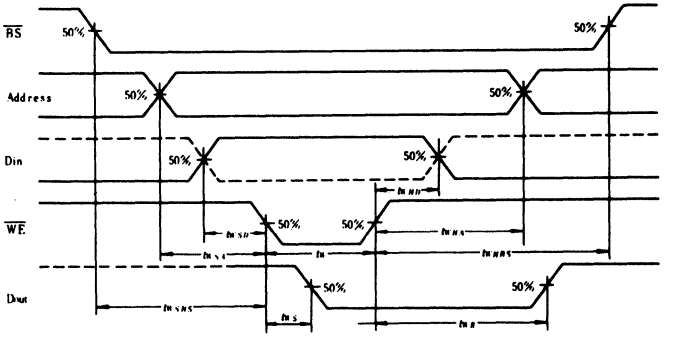


3. READ MODE

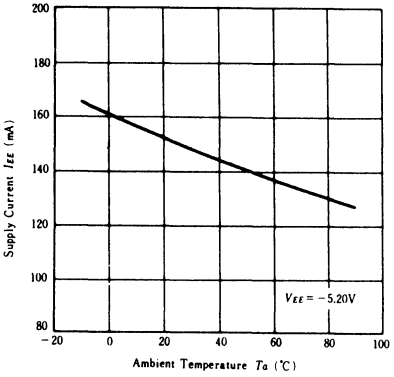




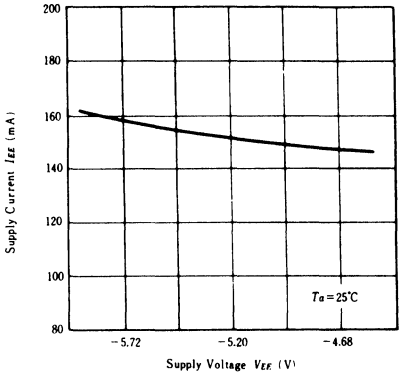
4. WRITE MODE



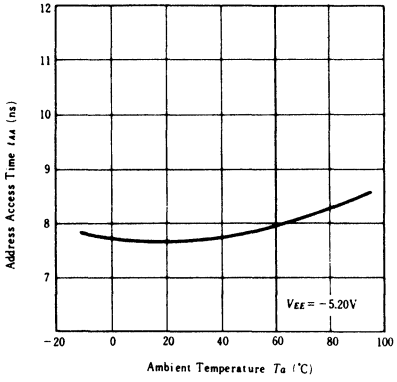
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



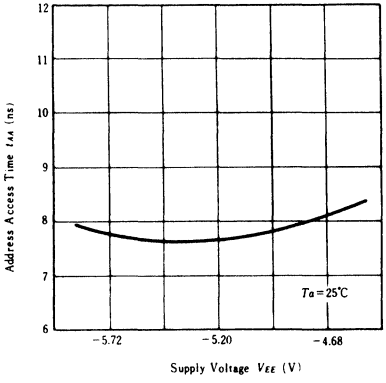
SUPPLY CURRENT vs. SUPPLY VOLTAGE



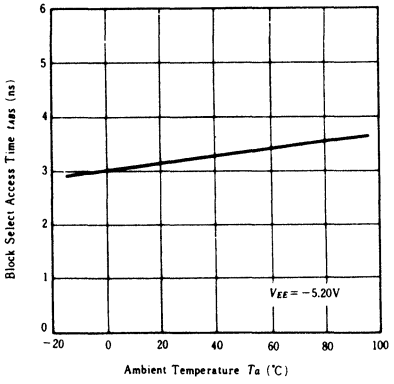
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



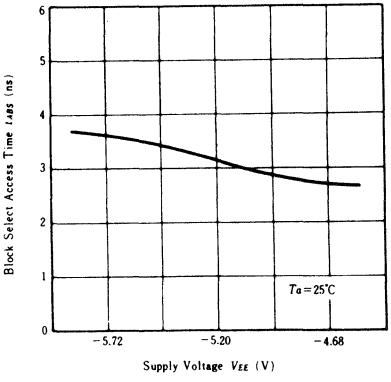
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



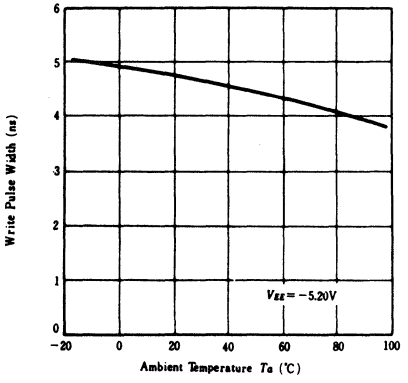
BLOCK SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



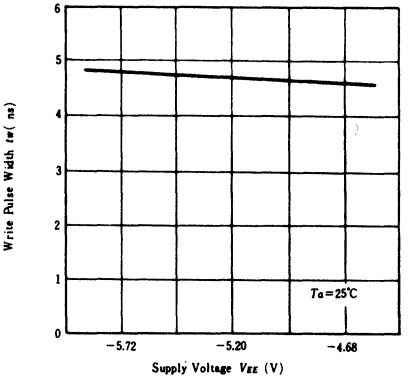
BLOCK SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



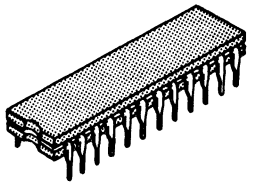
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422-7

256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.
Four active Low Block Select lines are provided to select each block independently.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.



(DG-24N)

■ FEATURES

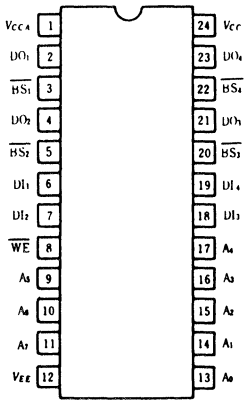
- 256-word x 4 bit organization
- Fully compatible with 10K ECL level
- Address access time: 7ns (max)
- Write pulse width: 4ns (min)
- Power dissipation: 1.0 mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

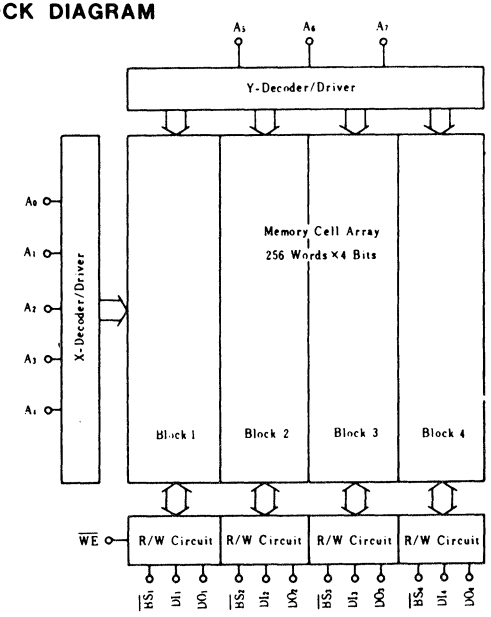
Notes) × : Irrelevant
* : Read out noninvert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−240	−200	—	mA
			Ta = 75°C	—	−180	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	4	7	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	4	3	—	ns
Data Setup Time	t_{WSD}		1		—	ns
Data Hold Time	t_{WHD}		1		—	ns
Address Setup Time	t_{WSA}	t_W = 4ns	2		—	ns
Address Hold Time	t_{WHA}		1		—	ns
Block Select Setup Time	t_{WSBS}		1		—	ns
Block Select Hold Time	t_{WHBS}		1		—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	8	ns

3. RISE/FALL TIME

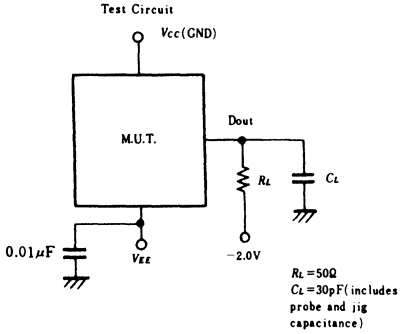
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

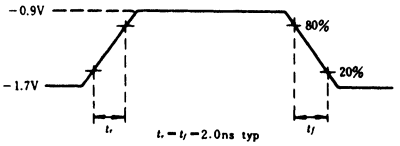
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

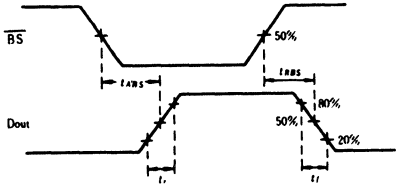
1. LOADING CONDITION

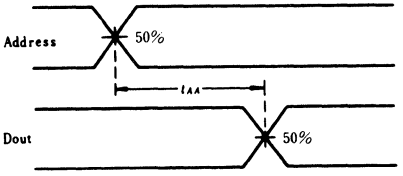


2. INPUT PULSE

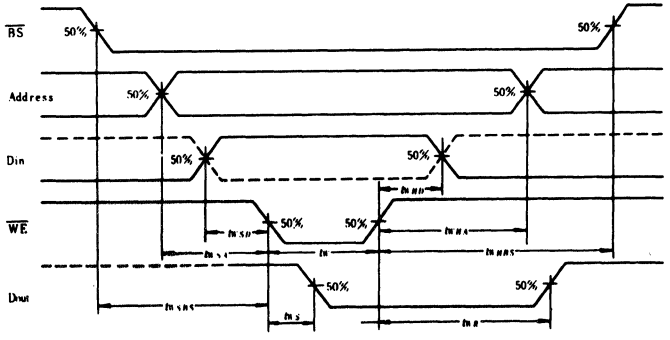


3. READ MODE





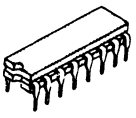
4. WRITE MODE



HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.



(DG-16A)

■ FEATURES

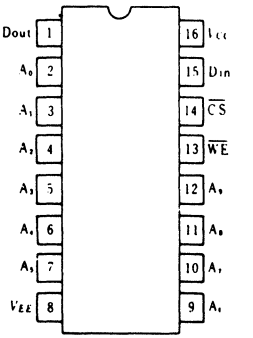
- Level ..... 10k ECL Compatible
- Construction ..... 1024-word by 1-bit
- Address Access Time ..... HM2112 10ns (max.)
  HM2112-1 8ns (max.)
- Chip Select Access Time ..... 6ns (max.)
- Power Consumption ..... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

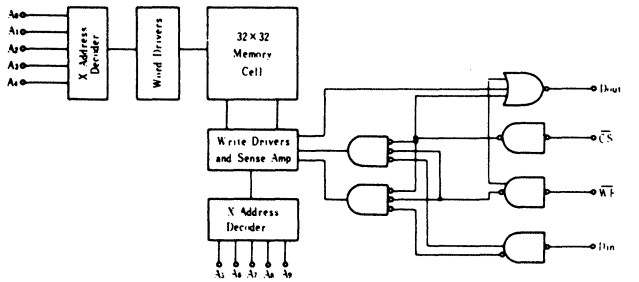
× : Irrelevant
* : Read out noniverted

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

●DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IL}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	Ta=0°C	−240	—	—	mA
			Ta=75°C	−200	—	—	

●AC CHARACTERISTICS

(V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		1	3	6	1	3	6	ns
Chip Select Recovery Time	t_{RCS}		1	3	5	1	3	5	ns
Address Access Time	t_{AA}		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	7	2	—	7	2	—	ns
Data Setup Time	t_{WSD}		1	0	—	1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	1	0	—	ns
Address Setup Time	t_{WSA}	t_W = 7ns	3	0	—	3	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	1	0	—	ns
Chip Select Hold Time	t_{WHCS}		1	0	—	1	0	—	ns
Write Disable Time	t_{WS}		1	3	5	1	3	5	ns
Write Recovery Time	t_{WR}		1	3	10	1	3	12	ns

3. RISE/FALL TIME

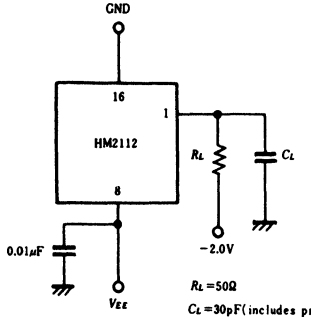
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		0.8	1.5	2.5	ns
Output Fall Time	t_f		0.8	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		1	3	5	pF
Output Capacitance	C_{out}		3	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

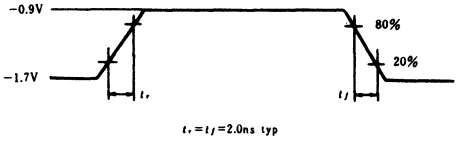
1. LOADING CONDITION



R_L=50Ω

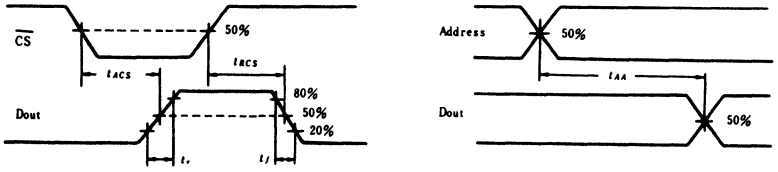
C_L=30pF(includes probe and jig capacitance)

2. INPUT PULSE

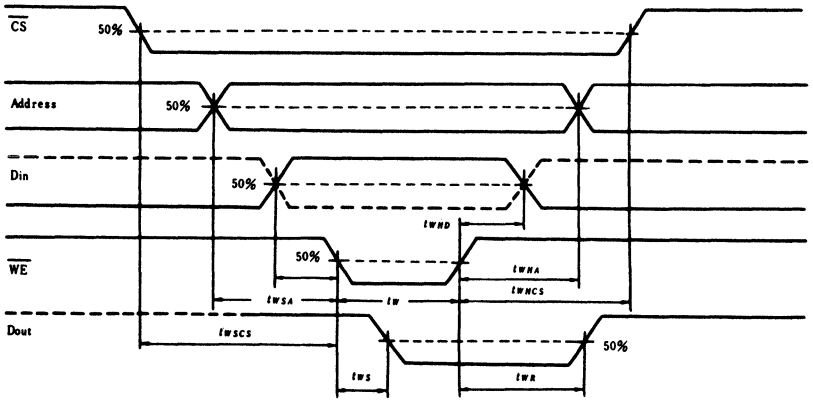


$t_r = t_f$=2.0ns typ

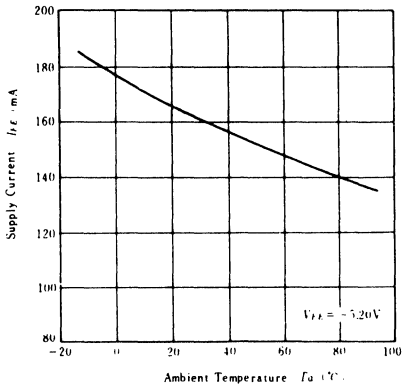
3. READ MODE



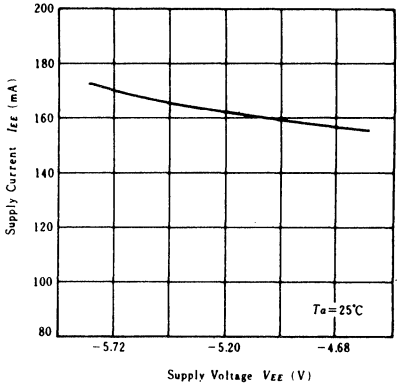
4. WRITE MODE



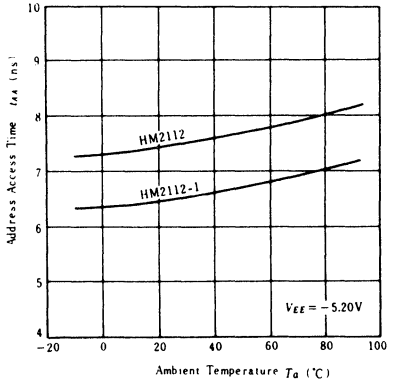
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



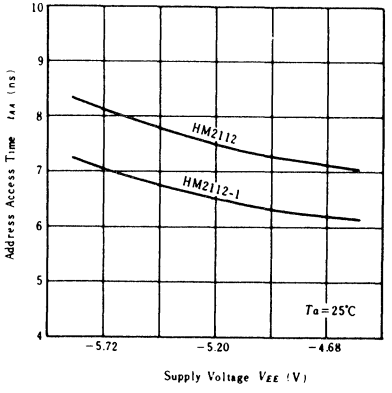
SUPPLY CURRENT vs. SUPPLY VOLTAGE



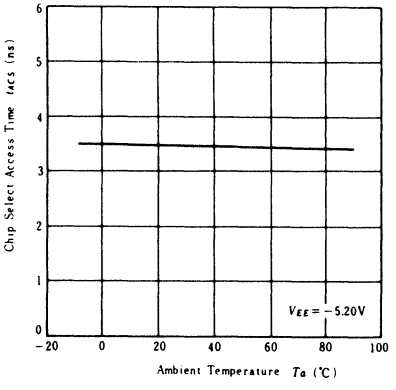
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



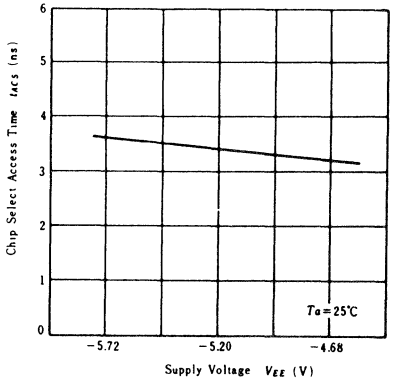
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



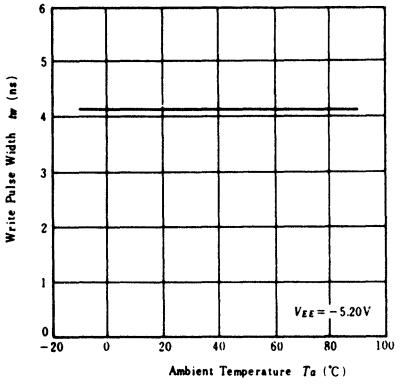
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



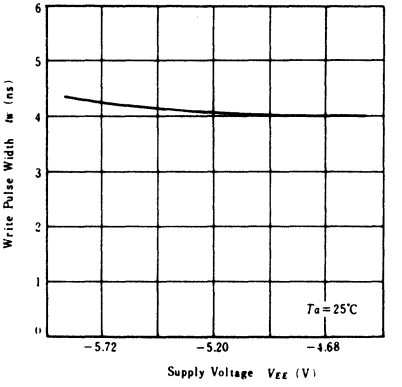
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

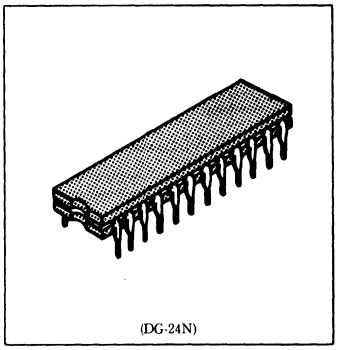
HM10474

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

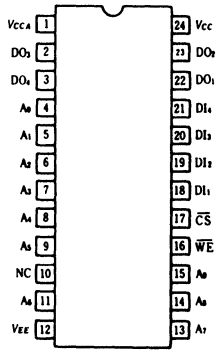


(DG-24N)

■FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



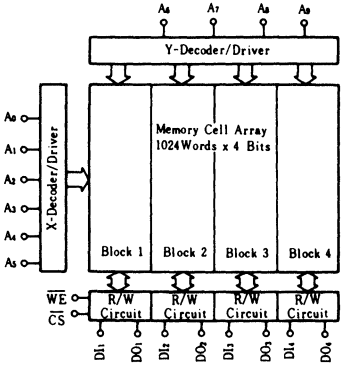
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{INA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{INB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{INA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−200	−160	—	mA
			Ta = 75°C	—	−145	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = $t_{W\,min}$	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	27	ns

3. RISE/FALL TIME

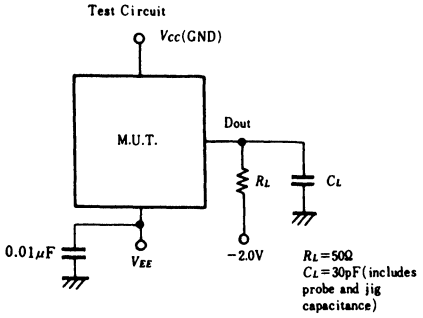
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

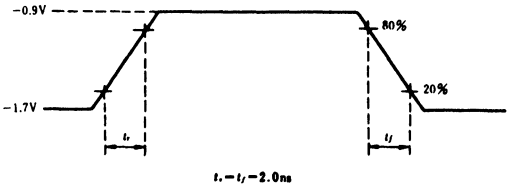
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

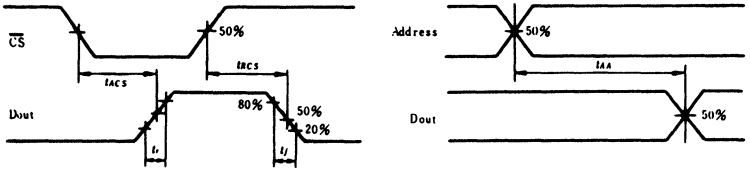
1. LOADING CONDITION



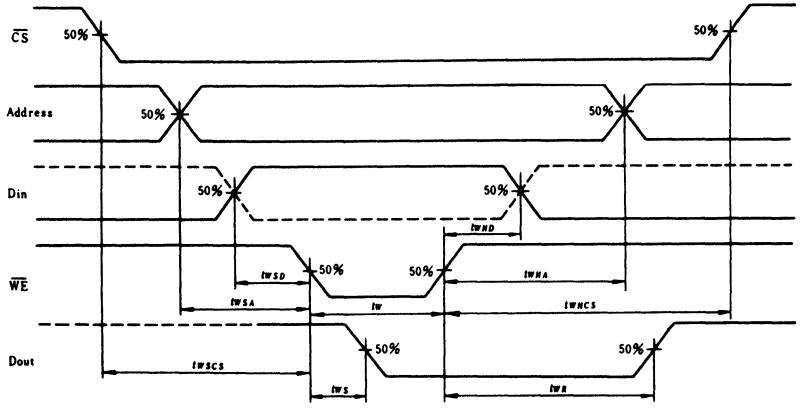
2. INPUT PULSE



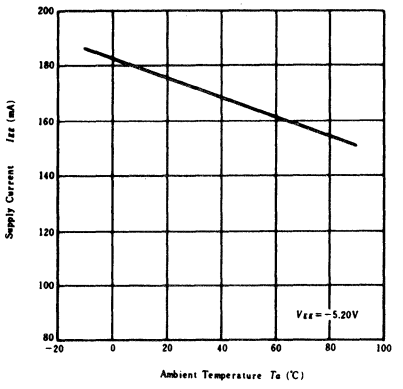
3. READ MODE



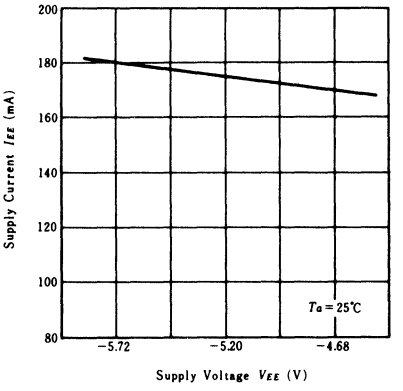
4. WRITE MODE



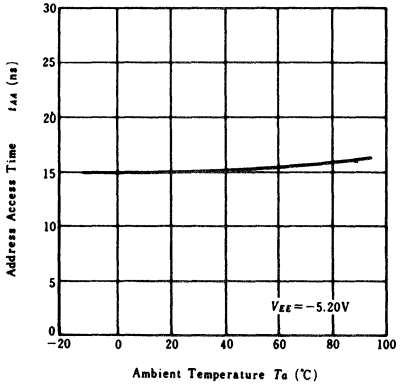
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



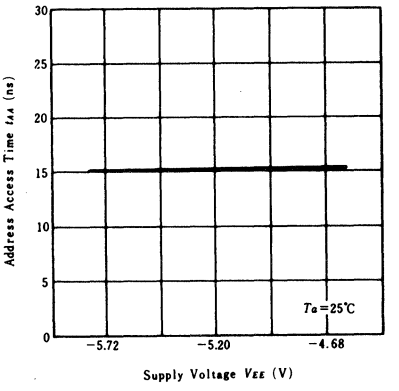
SUPPLY CURRENT vs. SUPPLY VOLTAGE



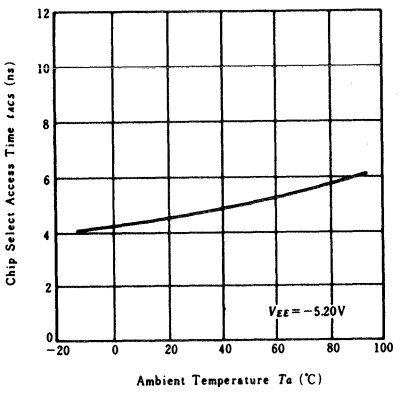
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



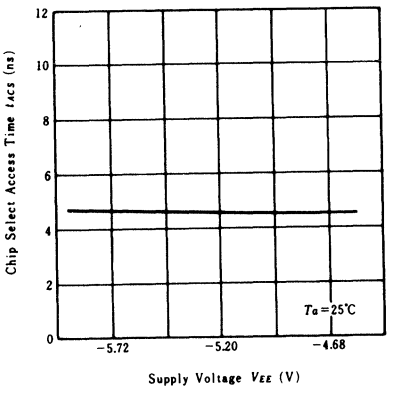
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



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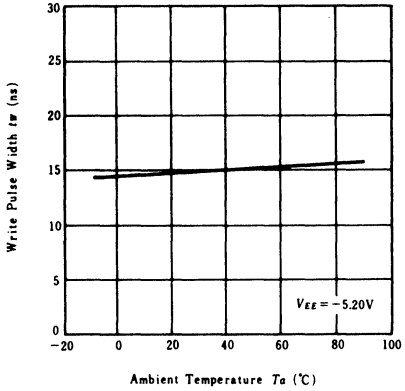
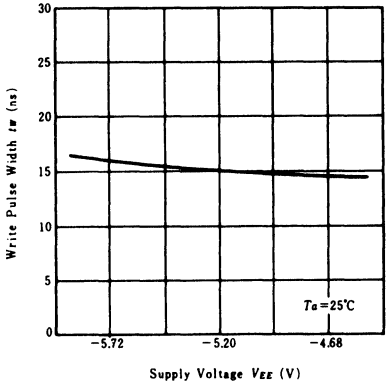
WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



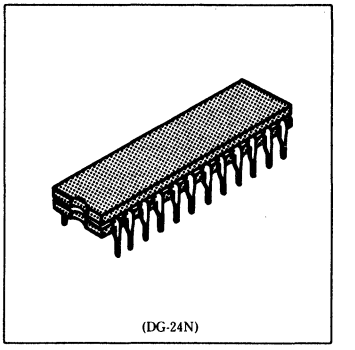
HM10474-8,HM10474-10

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

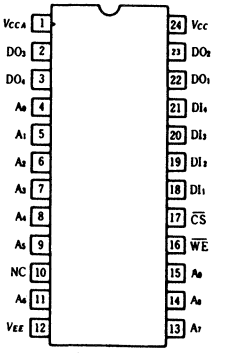


(DG-24N)

■FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474-8 8ns (max)
  HM10474-10 10ns (max)
- Write pulse width: HM10474-8 5ns (min)
  HM10474-10 5ns (min)
- Low power dissipation: 0.3mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



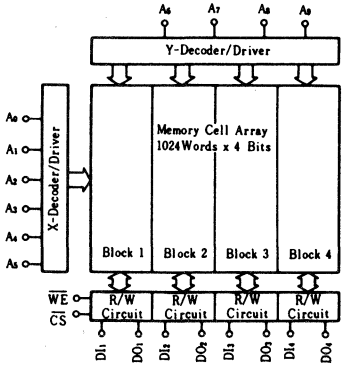
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{INA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{INB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{INA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta=0°C	−240	−220	—	mA
			Ta=75°C	—	−205	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	6	ns
Address Access Time	t_{AA}		—	—	8	—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 2ns	5	—	—	5	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_{W\,min}$	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		1	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	6	ns
Write Recovery Time	t_{WR}		—	—	9	—	—	12	ns

3. RISE/FALL TIME

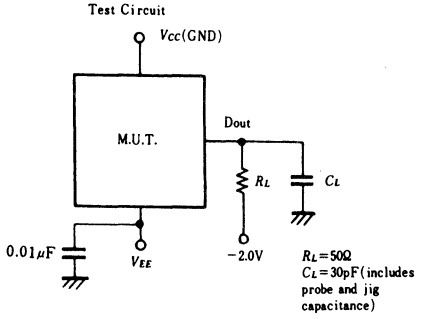
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

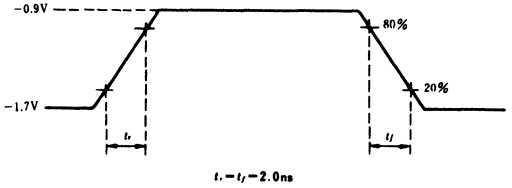
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

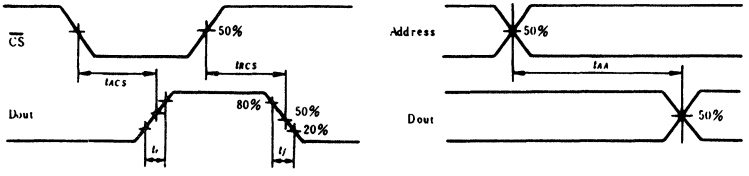
1. LOADING CONDITION



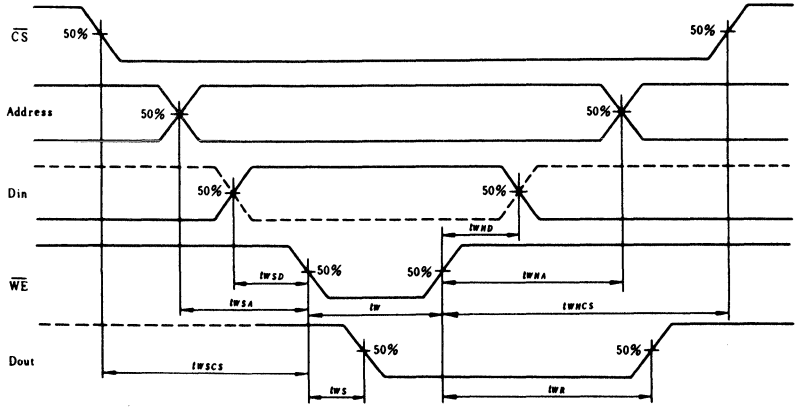
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



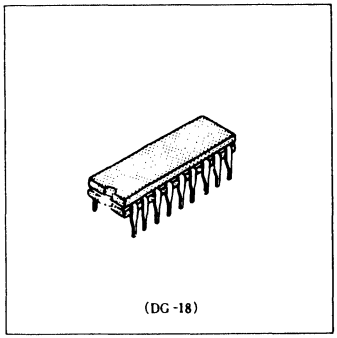
HM10470, HM10470-1

4096-word x 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.

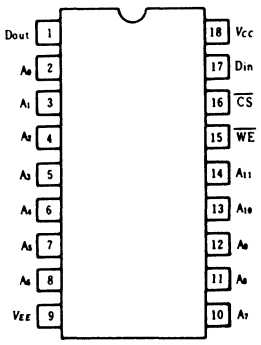


(DG-18)

■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10470 25ns (max)
  HM10470-1 15ns (max)
- Write pulse width: HM10470 25ns (min)
  HM10470-1 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



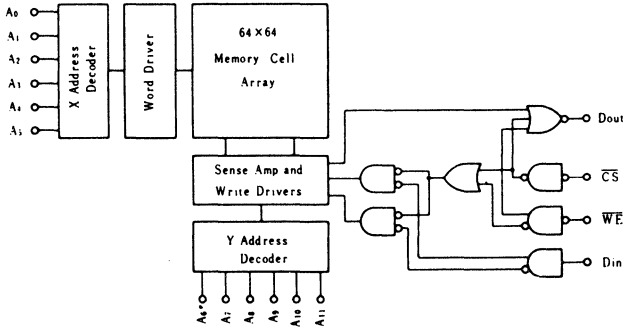
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 9	Ta = 0°C	−200*	−160*	—	mA
				−280**	−200**	—	
			Ta = 75°C	—	−145	—	

* HM10470
** HM10470-1

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	—	—	8	ns
Address Access Time	t_{AA}		—	15	25	—	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	25	—	—	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_{W\,min}$	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	27	—	—	17	ns

3. RISE/FALL TIME

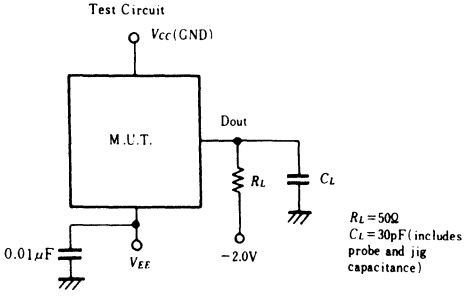
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

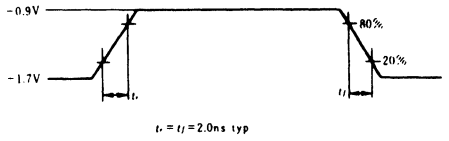
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

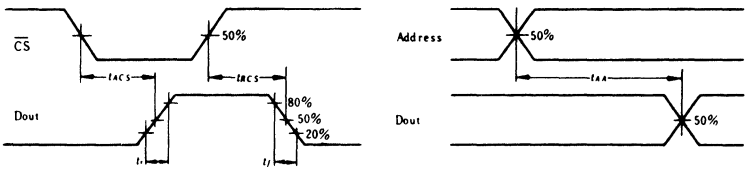
1. LOADING CONDITION



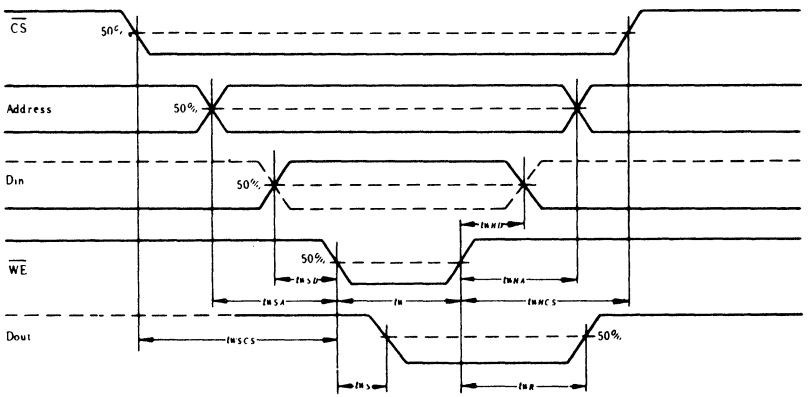
2. INPUT PULSE



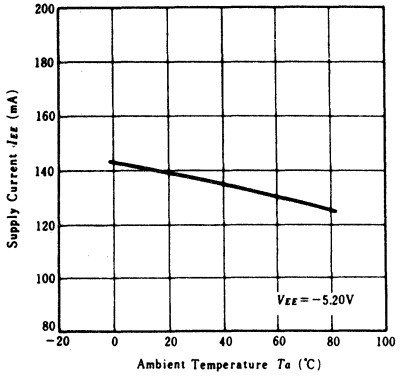
3. READ MODE



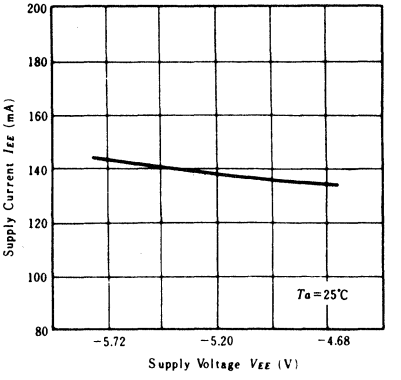
4. WRITE MODE



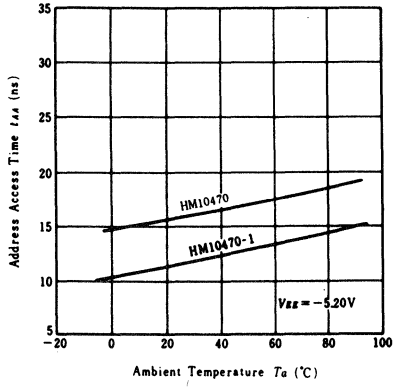
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



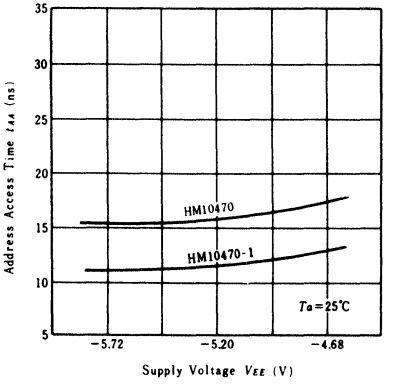
SUPPLY CURRENT vs. SUPPLY VOLTAGE



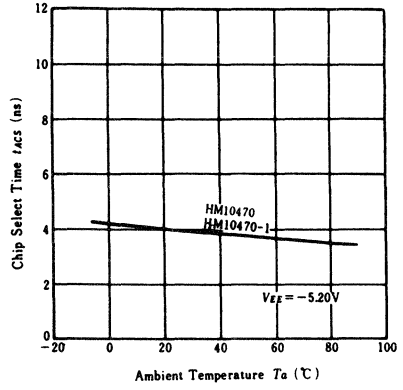
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



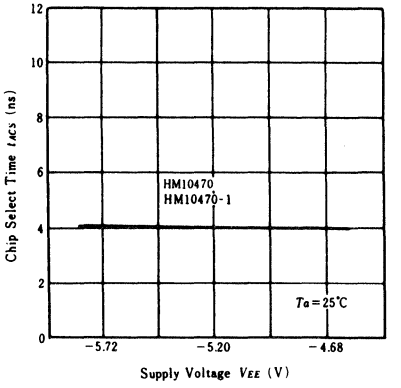
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



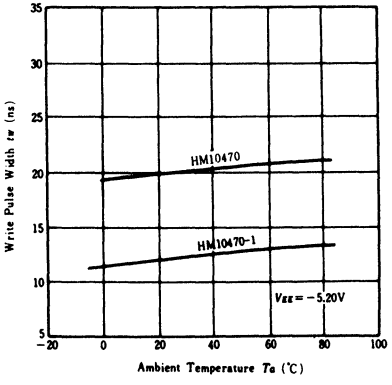
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



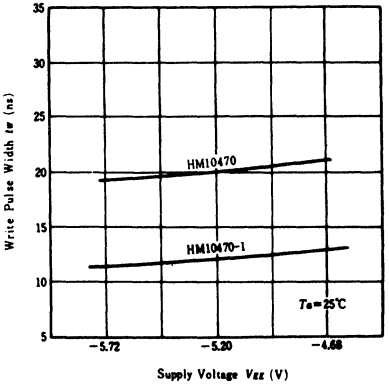
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



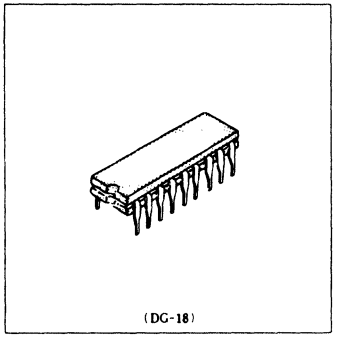
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10470-20

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.


(DG-18)

■ FEATURES

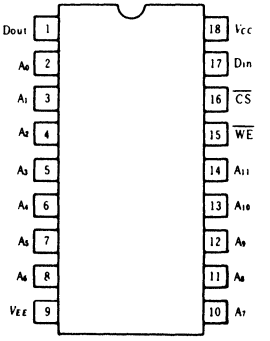
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 20ns (max)
- Write pulse width: 20ns (min)
- Low power dissipation: 0.25 mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

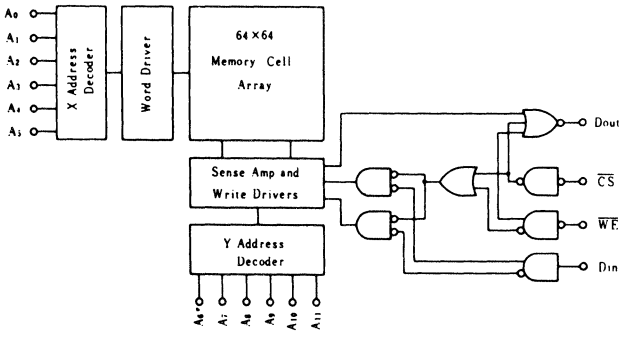
Notes) × : Irrelevant
* : Read Out Nonivert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IN}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−260	−220	—	mA
			Ta = 75°C	—	−210	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	ns
Address Access Time	t_{AA}		—	—	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = 20ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	ns
Write Recovery Time	t_{WR}		—	—	22	ns

3. RISE/FALL TIME

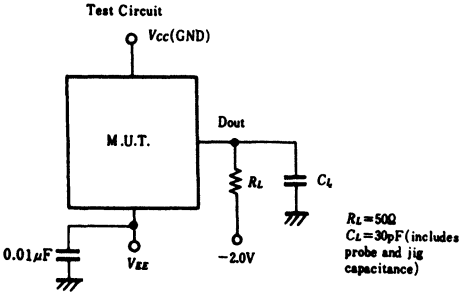
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

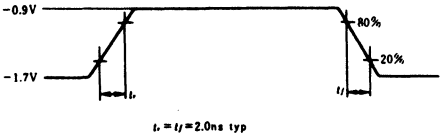
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

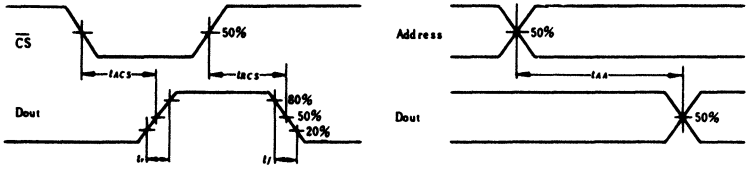
1. LOADING CONDITION



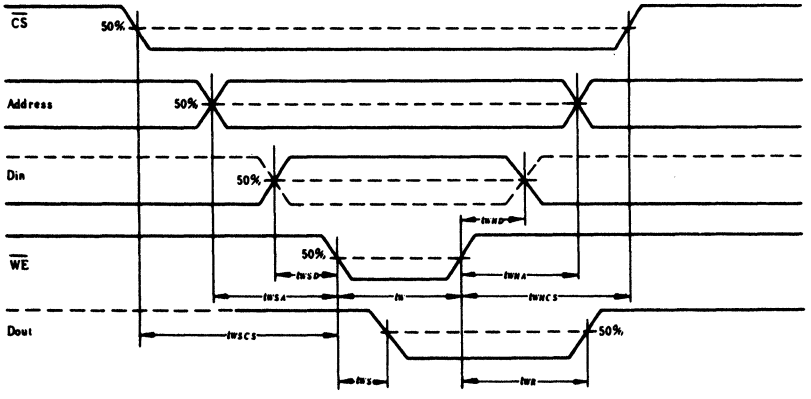
2. INPUT PULSE



3. READ MODE



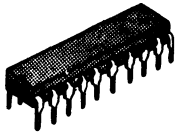
4. WRITE MODE



HM2142

4096-words × 1-bit Very High Speed Random Access Memory

The HM2142 is 4096-words x 1-bit very high speed read/write, random access memory developed for high speed systems such as pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM2142 is encapsulated in cerdip-20 pin package.



(DG-20N)

■ FEATURES

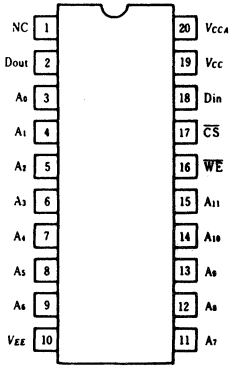
- 4096-words x 1 bit organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 10ns (min)
- Power dissipation: 0.3 mW/bit
- Output obtainable by wired-OR

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

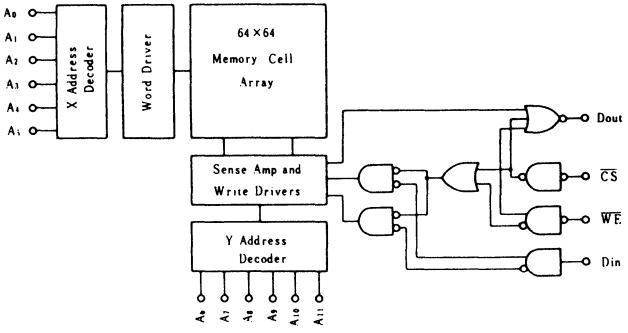
Notes) × : Irrelevant
* : Read Out Noninvert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IH}=V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−980	—	−810	
			+75°C	−950	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IH}=V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1165	—	−880	mV
			+25°C	−1165	—	−880	
			+75°C	−1165	—	−880	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1810	—	−1560	
			+25°C	−1810	—	−1560	
			+75°C	−1810	—	−1560	
Input Current	I_{IH}	V_{IH}=V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IH}=V_{ILB}	0 to +75°C	0.5	—	170	
		Others / V_{IH}=V_{ILB}	0 to +75°C	−50	—	—	
Supply Current	I_{EE}	All Input and Output Open.	Ta=0°C	−270	−240	—	mA
			Ta=75°C	—	−220	—	

● AC CHARACTERISTICS (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	ns
Address Access Time	t_{AA}		—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=3ns	10	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	ns
Address Setup Time	t_{WSA}	t_W=10ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	ns
Write Disable Time	t_{WS}		—	—	6	ns
Write Recovery Time	t_{WH}		—	—	12	ns

3. RISE/FALL TIME

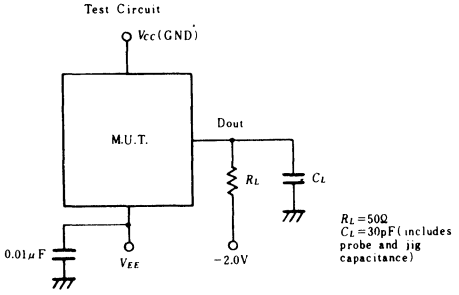
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

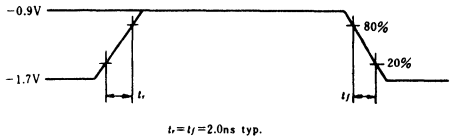
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

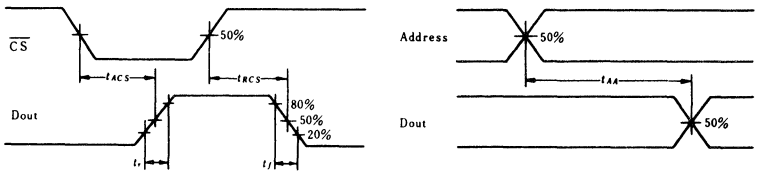
1. LOADING CONDITION



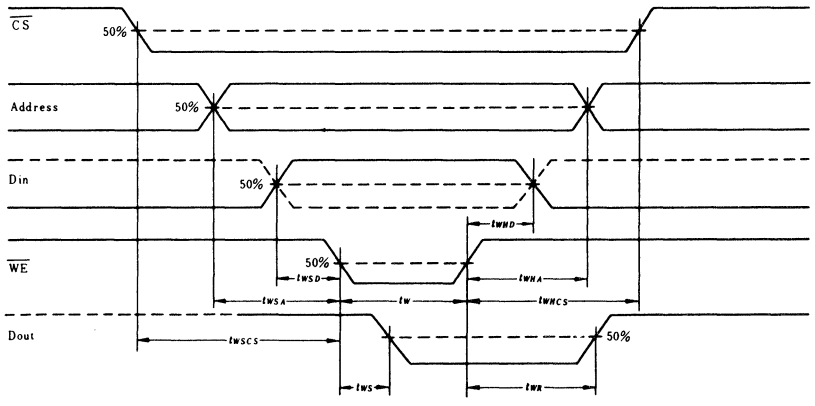
2. INPUT PULSE



3. READ MODE



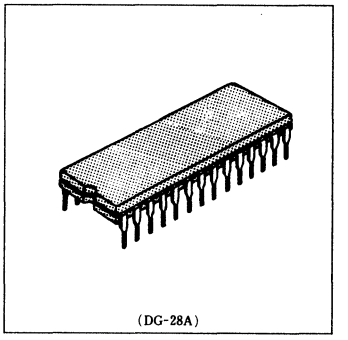
4. WRITE MODE



HM10484-10 — Preliminary

4096-words x 4-bit Fully Decoded Random Access Memory

The HM10484 is ECL 10K compatible, 4096-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.


(DG-28A)

Features

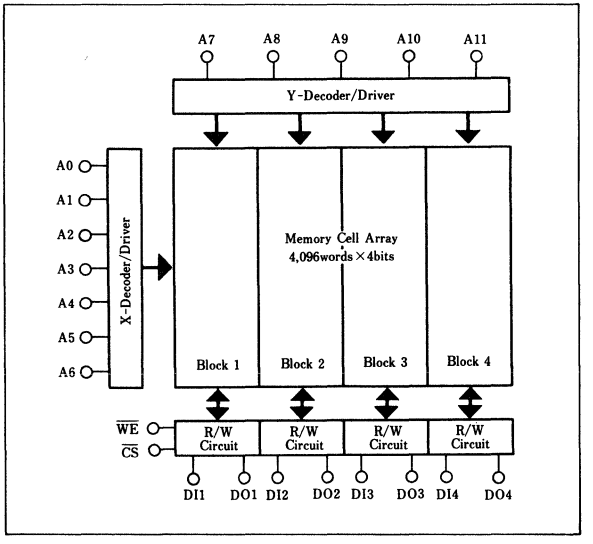
- 4096-word x 4-bits organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 7ns (min)
- Power dissipation: 840mW
- Output obtainable by wired-OR

Function Table

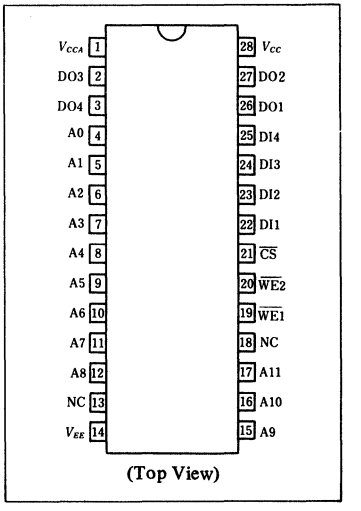
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

Notes) ×: Irrelevant
*: Read Out Nonivert

Block Diagram



Pin Arrangement



(Top View)

Note) The specifications of this device are subject to change without notice. Please contact your nearest Higachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	℃
Storage Temperature	Tstg(Bias)*	−55 to +125	℃

*Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition	
Output Voltage	V_{OH}	−1000	—	−840	mV	V_{IN}=V_{IHA} or V_{ILB}	0℃
		−960	—	−810			+25℃
		−900	—	−720			+75℃
	V_{OL}	−1870	—	−1665			0℃
		−1850	—	−1650			+25℃
		−1830	—	−1625			+75℃
Output Threshold Voltage	V_{OHC}	−1020	—	—	mV	V_{IN}=V_{IHB} or V_{ILA}	0℃
		−980	—	—			+25℃
		−920	—	—			+75℃
	V_{OLC}	—	—	−1645			0℃
		—	—	−1630			+25℃
		—	—	−1605			+75℃
Input Voltage	V_{IH}	−1145	—	−840	mV	Guaranteed Input Voltage High for All Inputs	0℃
		−1105	—	−810			+25℃
		−1045	—	−720			+75℃
	V_{IL}	−1870	—	−1490		Guaranteed Input Voltage Low for All Inputs	0℃
		−1850	—	−1475			+25℃
		−1830	—	−1450			+75℃
Input Current	I_{IH}	—	—	220	μA	V_{IN}=V_{IHA}	0 to +75℃
	I_{IL}	0.5	—	170		$\overline{CS}$ — V_{IN}=V_{ILB}	0 to +75℃
		−50	—	—		Others	
Supply Current	I_{EE}	−210	—	—	mA	All Inputs and Outputs Open. Test Pin 11	0℃
		−210	—	—			+75℃

AC Characteristics

(V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	6	ns	
Chip Select recoverry Time	t_{RCS}	—	—	6	ns	
Address Access Time	t_{AA}	—	—	10	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	tw	7	—	—	ns	$t_{WSA}=t_{WSA}$ min
Data Setup Time	t_{WSD}	1	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	ns	
Address Setup Time	t_{WSA}	1	—	—	ns	tw=tw min
Address Hold Time	t_{WHA}	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	1	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	ns	
Write Recovery Time	t_{WR}	—	—	12	ns	

Rise/Fall Time

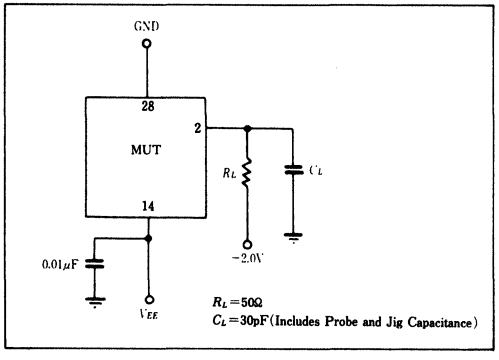
Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

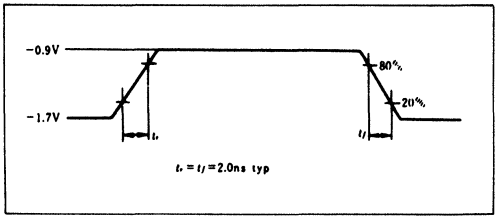
Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

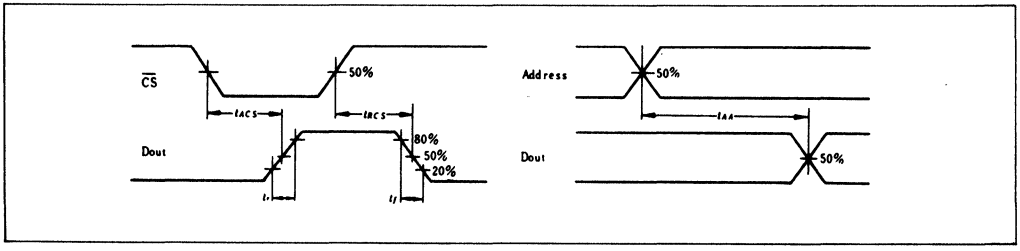
Loading Condition



Input Pulse



Read Mode



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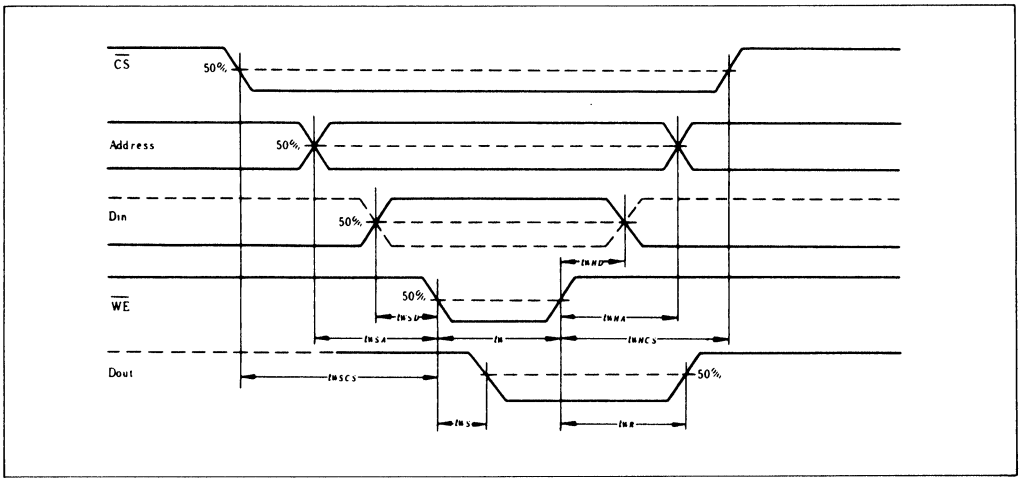
Write Mode

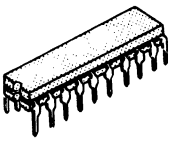


HM10480,HM10480F

16,384-words × 1-bit Fully Decoded Random Access Memory

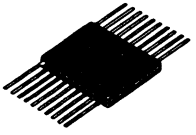
The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

HM10480



(DG-20N)

HM10480F



(FG-20D)

■FEATURES

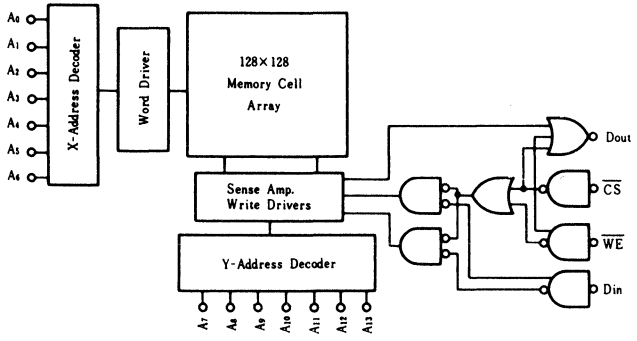
- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

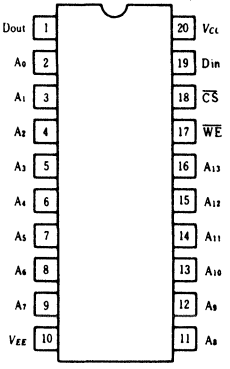
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−200	−140	—	mA
			Ta = 75°C	—	−130	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	15	ns
Chip Select Recovery Time	t_{RCS}		2	—	15	ns
Address Access Time	t_{AA}		3	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 5ns	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	ns
Address Setup Time	t_{WSA}	t_W = 25ns	5	—	—	ns
Address Hold Time	t_{WHA}		5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	ns
Write Disable Time	t_{WS}		—	—	15	ns
Write Recovery Time	t_{WR}		—	—	30	ns

3. RISE/FALL TIME

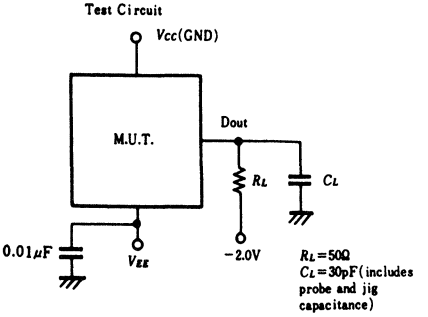
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

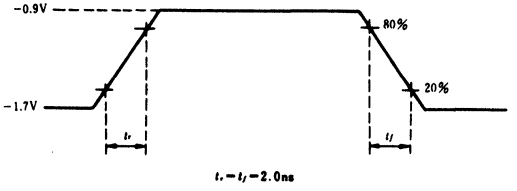
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

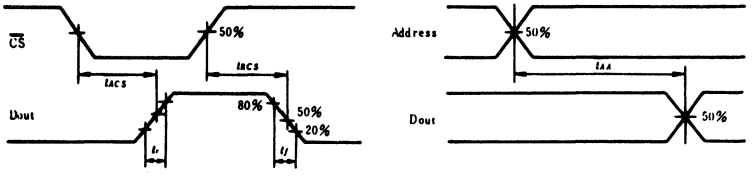
1. LOADING CONDITION



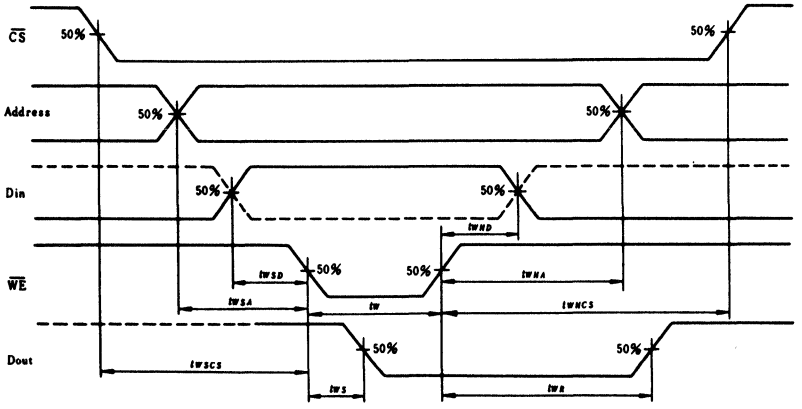
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

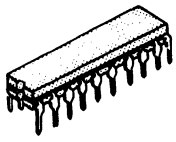


HM10480-15,HM10480F-15

16,384-words × 1-bit Fully Decoded Random Access Memory

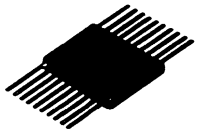
The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

HM10480-15



(DG-20N)

HM10480F-15



(FG-20D)

■FEATURES

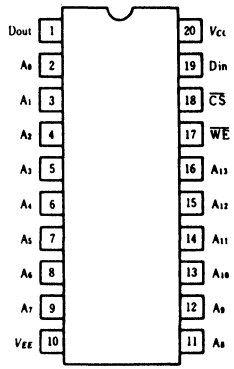
- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 15ns (max)
- Write pulse width: 15ns (min)
- Low power dissipation: 0.06mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

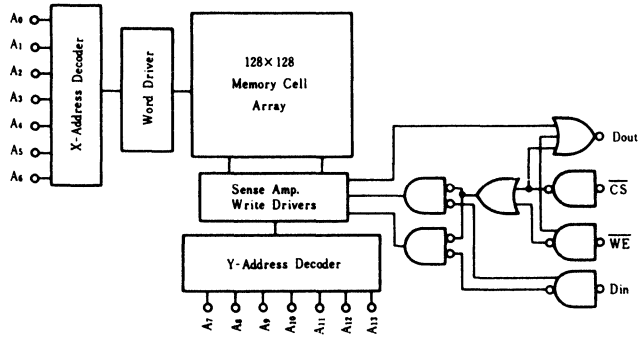
Notes) × : Irrelevant
* : Read Out Noninvert

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−240	−220	—	mA
			Ta = 75°C	—	−200	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	8	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	ns
Address Access Time	t_{AA}		3	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		3	—	—	ns
Address Setup Time	t_{WSA}	t_W = 15ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	ns
Chip Select Hold Time	t_{WHCS}		3	—	—	ns
Write Disable Time	t_{WS}		—	—	12	ns
Write Recovery Time	t_{WR}		—	—	17	ns

3. RISE/FALL TIME

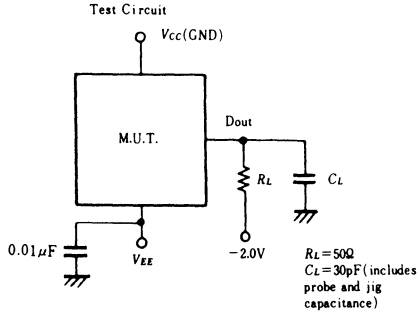
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

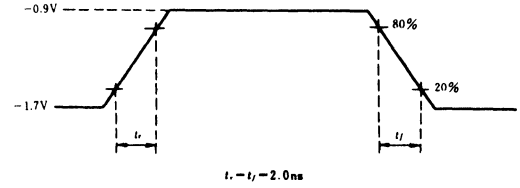
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

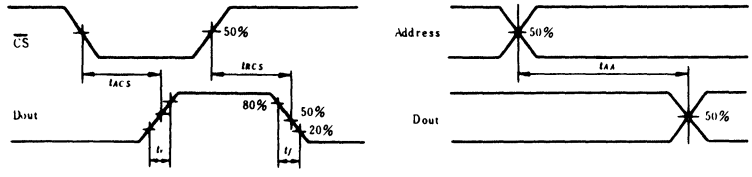
1. LOADING CONDITION



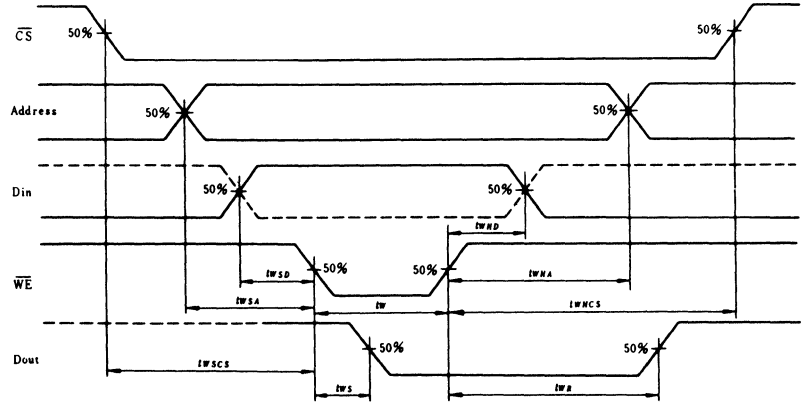
2. INPUT PULSE



3. READ MODE



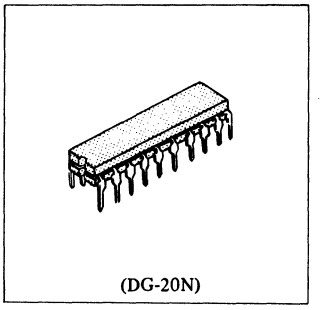
4. WRITE MODE



HM10480L

16,384-words X 1-bit Fully Decoded Random Access Memory

The HM10480L is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed and low power systems such as control/buffer and main storages.
The HM10480L is encapsulated in cerdip-20 pin package.



(DG-20N)

■ FEATURES

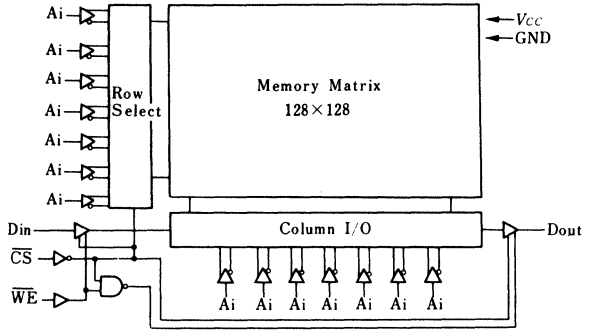
- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 20ns (min)
- Low power dissipation: Standby 220mW (typ.), Operation 350mW (typ.)
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

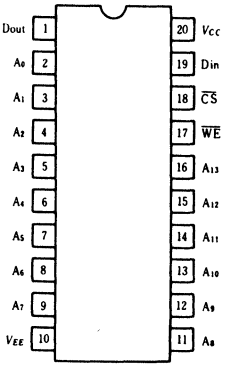
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta=0°C	−120	−70	—	mA
			Ta=75°C	−110	−61	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	15	25	ns
Chip Select Recovery Time	t_{RCS}		—	9	25	ns
Address Access Time	t_{AA}		3	17	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} − 3ns	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W − 20ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	25	ns

3. RISE/FALL TIME

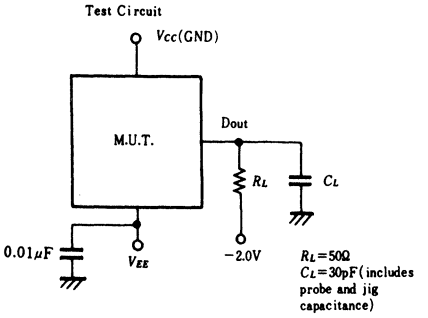
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

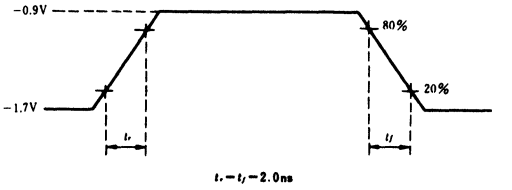
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	5	—	pF
Output Capacitance	C_{out}		—	6.5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

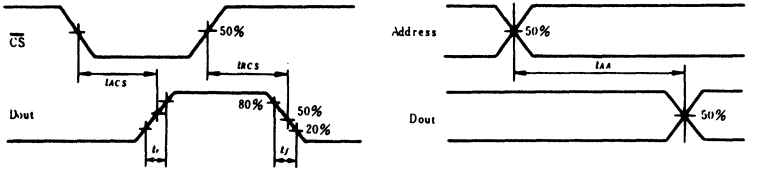
1. LOADING CONDITION



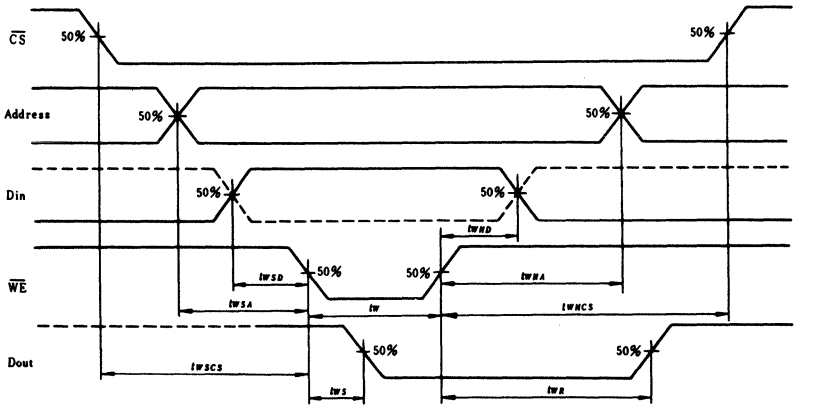
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

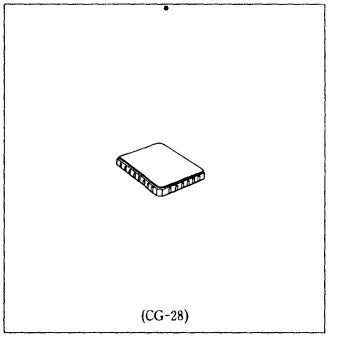


HM10494LCG

16384-word x 4-bit ECL RAM

Features

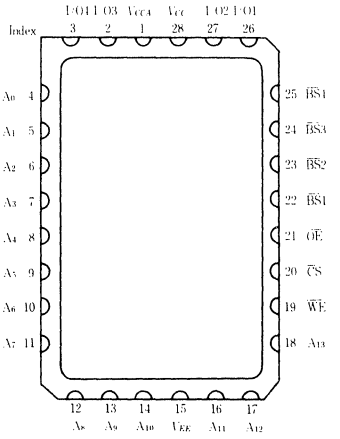
- 16k-word × 4-bit organization
- Low Power Dissipation; Operation 500mW (typ.)
  Standby 350mW (typ.)
- Address Access Time; 25ns (max.)
- Write Pulse Width; 17ns (min.)
- Balanced Read and Write Cycle Time
- I/O common



Truth Table

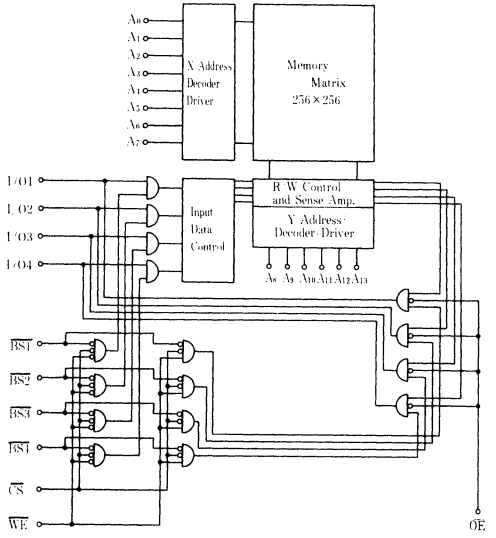
Input				I/O		Mode	Remarks
$\overline{CS}$	$\overline{BS}$	$\overline{WE}$	$\overline{OE}$	DI	DO		
H	×	×	×	×	L	Not Selected	Power Down
×	H	×	×	×	L	Not Selected	
L	L	L	L	L	L	Write "0"	
L	L	L	L	H	L	Write "1"	
L	L	L	H	L	L	Write "0"	
L	L	L	H	H	L	Write "1"	
L	L	H	L	L	DO	Read	Write Data = Read Data
L	L	H	H	×	L	Not Selected	

Pin Arrangement



(Top View)

Block Diagram



■ Absolute Maximum Ratings (T_a = 25°C)

Item	symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ Electrical Characteristics

• DC Characteristics

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_a = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1040	−	−840	mV
			+25°C	−1010	−	−820	
			+75°C	−980	−	−780	
	V_{OL}		0°C	−1860	−	−1630	
			+25°C	−1850	−	−1625	
			+75°C	−1845	−	−1590	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1060	−	−	mV
			25°C	−1030	−	−	
			+75°C	−1000	−	−	
	V_{OLC}		0°C	−	−	−1610	
			+25°C	−	−	−1605	
			+75°C	−	−	−1590	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	−	−840	mV
			+25°C	−1105	−	−810	
			+75°C	−1045	−	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	−	−1490	
			+25°C	−1850	−	−1475	
			+75°C	−1830	−	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	−	−	220	μA
	I_{IL}	$\overline{CS}$, $\overline{BS}$, $\overline{OE}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	−	170	
		Ad, $\overline{WE}$		−50	−	−	
Supply Current	I_{EE}	All Input V_{IH} or V_{IL} except $\overline{CS}$ = V_{IL}	0 to +75°C	−140	−	−	mA
Stand by Supply Current	I_{SB}	All Input V_{IH} or V_{IL} except $\overline{CS}$ = V_{IH}	0 to +75°C	−100	−	−	mA

- **AC Characteristics** (V_{EE} = -5.2V ±5%, T_a = 0 to +75°C, air flow exceeding 2m/sec)

READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Address Access Time	t_{AA}		–	–	25	ns
Chip Select Access Time	t_{ACS}		–	–	25	ns
Chip Select Recovery Time	t_{RCS}		–	–	15	ns
Block Select Access Time	t_{ABS}		–	–	15	ns
Block Select Recovery Time	t_{RBS}		–	–	15	ns
Out put Enable Access Time	t_{AOE}		–	–	7	ns
Out put Enable Recovery Time	t_{ROE}		–	–	7	ns

Write Mode

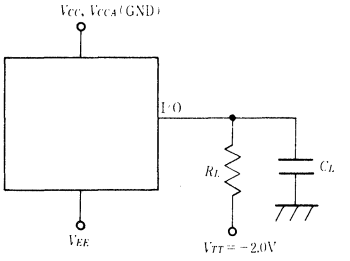
Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W		17	–	–	ns
Address Setup Time	t_{WSA}		5	–	–	ns
Address Hold Time	t_{WHA}		3	–	–	ns
Chip Select Pulse Width	t_{CW}		17	–	–	ns
Chip Select Address Setup Time	t_{CSA}		5	–	–	ns
Chip Select Address Hold Time	t_{CHA}		3	–	–	ns
Block Select pulse Width	t_{BW}		17	–	–	ns
Block Select Address Setup Time	t_{BSA}		5	–	–	ns
Block Select Address Hold Time	t_{BHA}		3	–	–	ns
Data Setup Time	t_{WSD}		17	–	–	ns
Data Hold Time	t_{WHD}		1	–	–	ns
Write Disable Time	t_{WS}		–	–	7	ns
Write Recovery Time	t_{WR}		–	–	28	ns

Write Disable Mode

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Setup Time	t_{WSCS}		1	–	–	ns
Chip Select Hold Time	t_{WHCS}		1	–	–	ns
Block Select Seoup Time	t_{WSBS}		1	–	–	ns
Block Select Hold Time	t_{WHBS}		1	–	–	ns

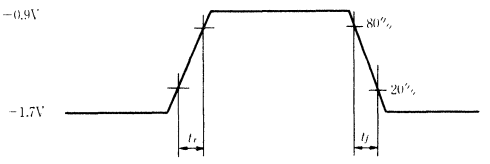
■ Test Circuit and Waveforms

● Loading Condition



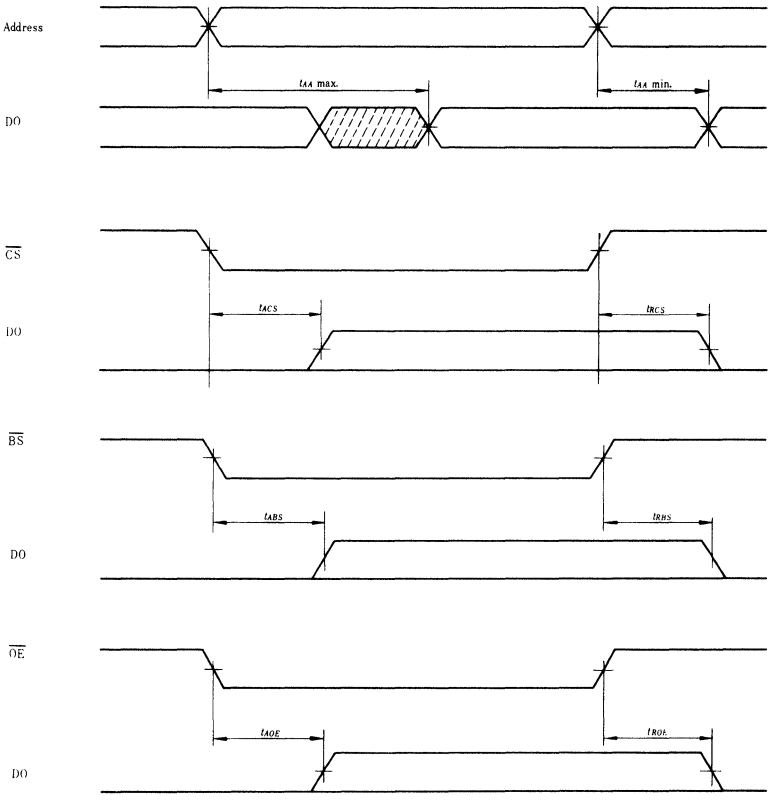
$R_L = 50\Omega$
$C_L = 30pF$ (includes probe and jig capacitance)

● Input Pulse



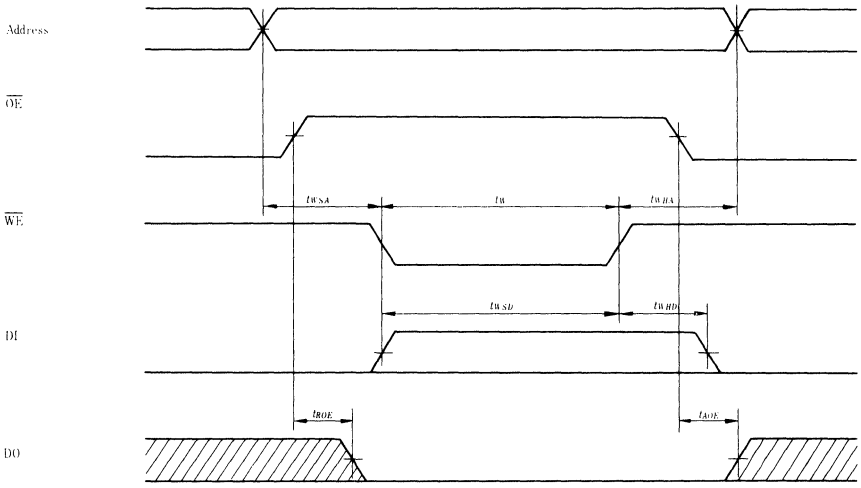
$t_r = t_f = 1.5ns$ typ.

● Read Mode

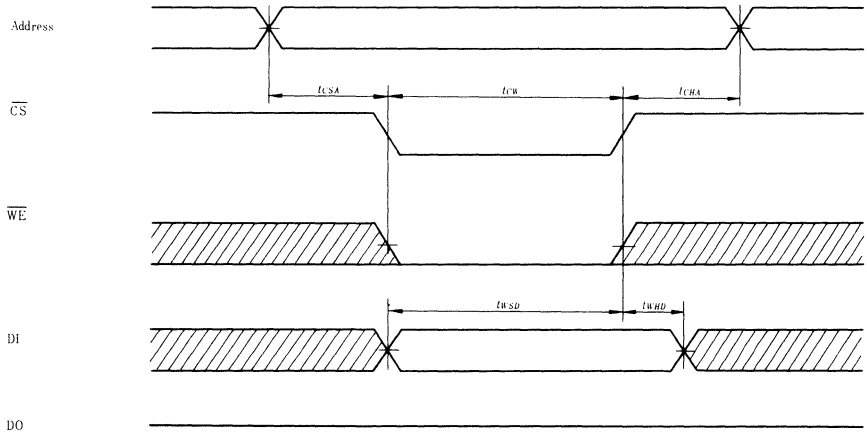


• Write Mode

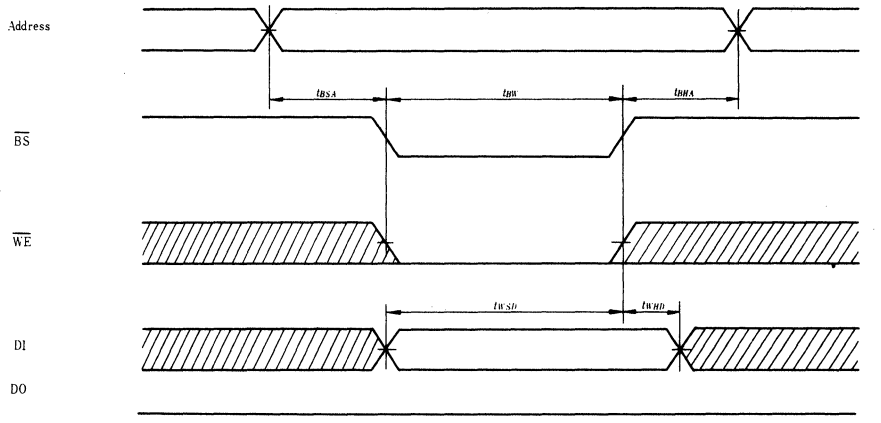
$\overline{OE}$ Control



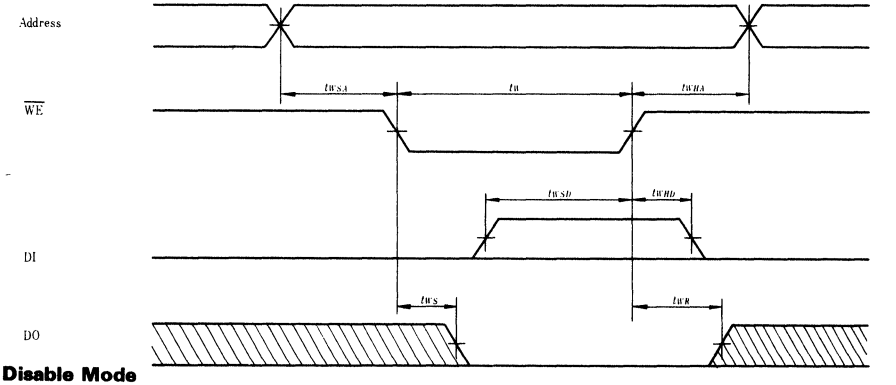
$\overline{CS}$ Control



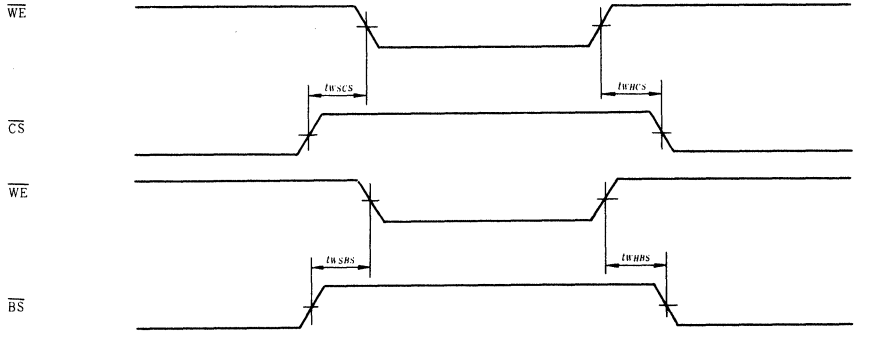
$\overline{BS}$ Control



$\overline{WE}$ Control



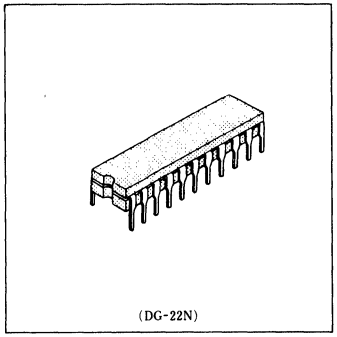
• Write Disable Mode



HM10490-15 — Preliminary

65536-words x 1-bit Fully Decoded Random Access Memory

HM10490-15 is ECL 10k compatible, 65536-words x 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.



Features

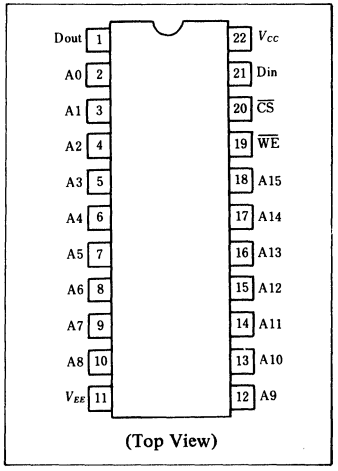
- 65,536-words x 1-bit organization
- Fully compatible with 10k ECL level
- Address access time . . . . . 15ns (max.)
- Write pulse width . . . . . 10ns (min.)
- Low power dissipation . . . . . 420mW (typ.)
- Output obtainable by wired-OR (open emitter)

Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

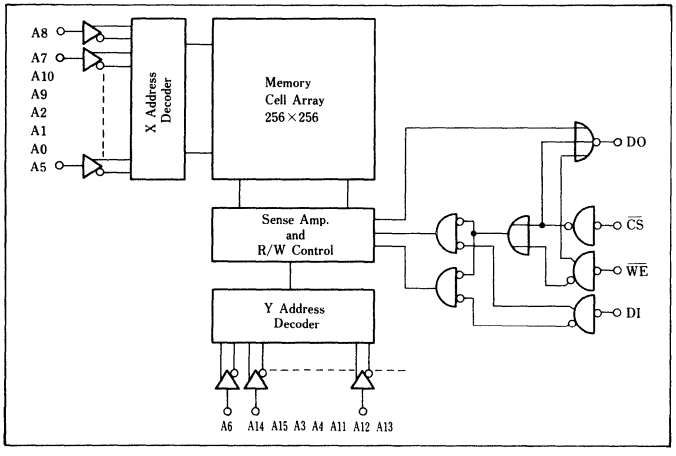
Notes) ×: Irrelevant
*: Read Out Nonivert

Pin Arrangement



Note) The specifications of this device are subject to change without notice. Please contact your nearest Higachi's Sales Dept. regarding specifications.

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

*Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition	
Output Voltage	V_{OH}	−1000	—	−840	mV	V_{in} = V_{IHA} or V_{ILB}	0°C
		−960	—	−810			+25°C
		−900	—	−720			+75°C
	V_{OL}	−1870	—	−1665			0°C
		−1850	—	−1650			+25°C
		−1830	—	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	—	—	mV	V_{in} = V_{IHB} or V_{ILA}	0°C
		−980	—	—			+25°C
		−920	—	—			+75°C
	V_{OLC}	—	—	−1645			0°C
		—	—	−1630			+25°C
		—	—	−1605			+75°C
Input Voltage	V_{IH}	−1145	—	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1105	—	−810			+25°C
		−1045	—	−720			+75°C
	V_{IL}	−1870	—	−1490		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	—	−1475			+25°C
		−1830	—	−1450			+75°C
Input Current	I_{IH}	—	—	220	μA	V_{in} = V_{IHA}	0 to +75°C
	I_{IL}	0.5	—	170		$\overline{CS}$ — V_{in} = V_{ILB}	0 to +75°C
		−50	—	—		Others	
Supply Current	I_{EE}	−140	—	—	mA	All Inputs and Outputs Open. Test Pin 11	0°C
		−140	—	—			+75°C

AC Characteristics (V_{EE} = -5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	10	ns	
Chip Select Recoverry Time	t_{RCS}	—	—	10	ns	
Address Access Time	t_{AA}	—	—	15	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	10	—	—	ns	t_{WSA} = 2ns
Data Setup Time	t_{WSD}	2	—	—	ns	
Data Hold Time	t_{WHD}	3	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	ns	t_W = 10ns
Address Hold Time	t_{WHA}	3	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	3	—	—	ns	
Write Disable Time	t_{WS}	—	—	10	ns	
Write Recovery Time	t_{WR}	—	—	18	ns	

Rise/Fall Time

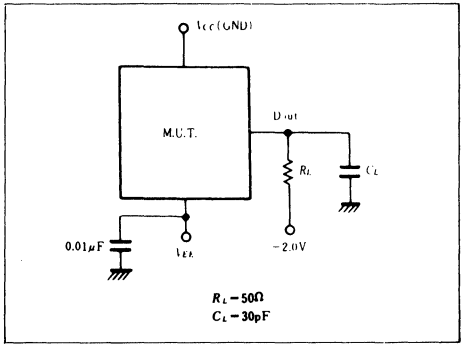
Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

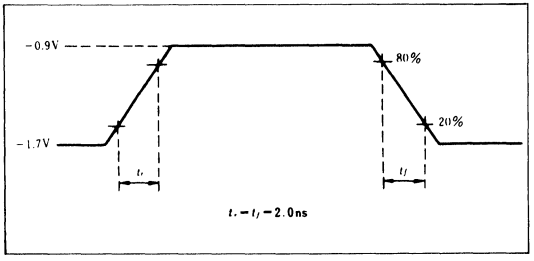
Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{out}	—	5	—	pF	

Test Circuit and Waveforms

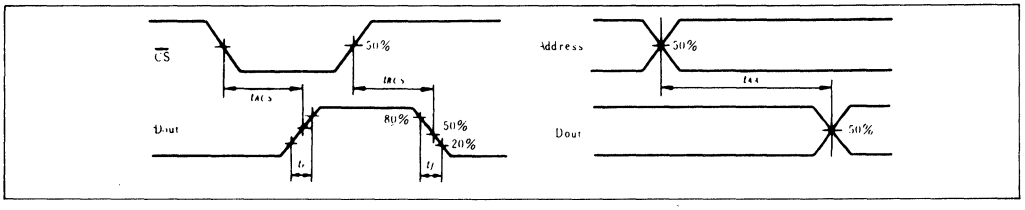
Loading Condition



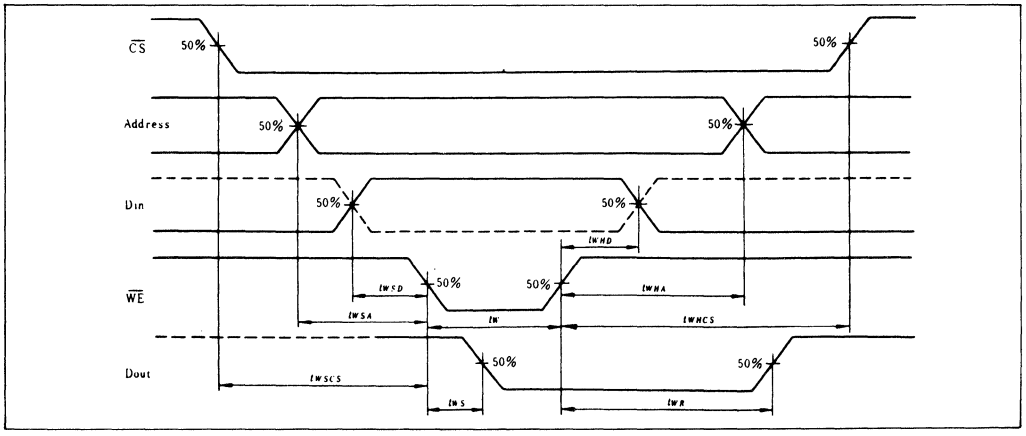
Input Pulse



Read Mode



Write Mode



HM100422,HM100422F
HM100422CG

256-word×4-bit Fully Decoded Random Access Memory

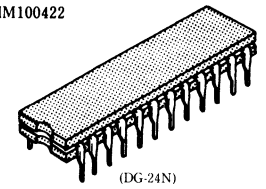
The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

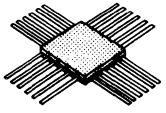
The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

HM100422



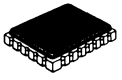
(DG-24N)

HM100422F



(FG-24)

HM100422CG



(CG-24)

■FEATURES

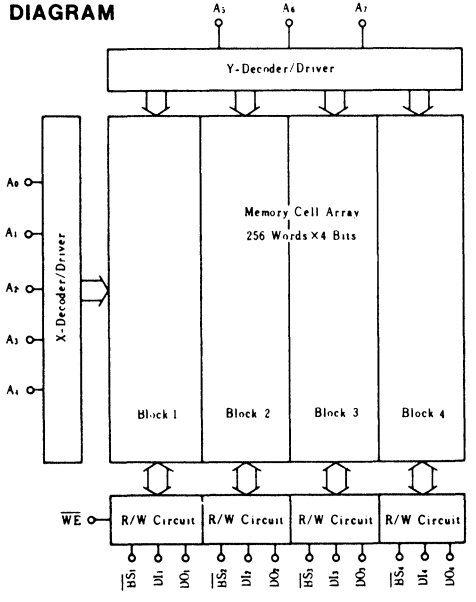
- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

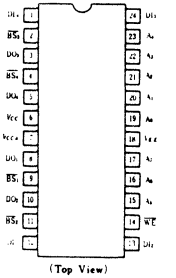
Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



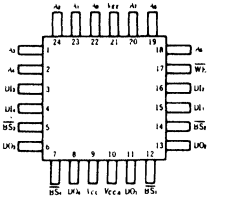
■PIN ARRANGEMENT

●HM100422



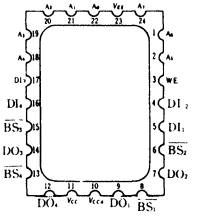
(Top View)

●HM100422F



(Top View)

●HM100422CG



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■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{BS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

● AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	6	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	6	ns
Write Recovery Time	t_{WR}		—	4.5	12	ns

3. RISE/FALL TIME

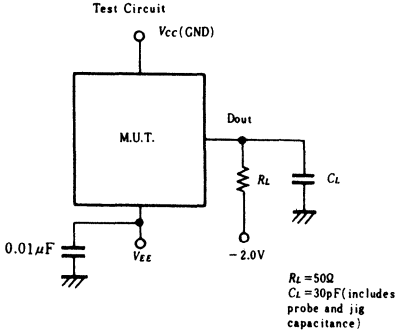
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

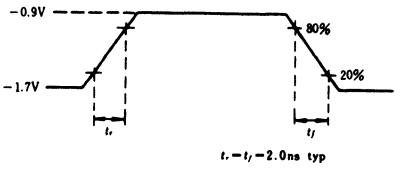
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

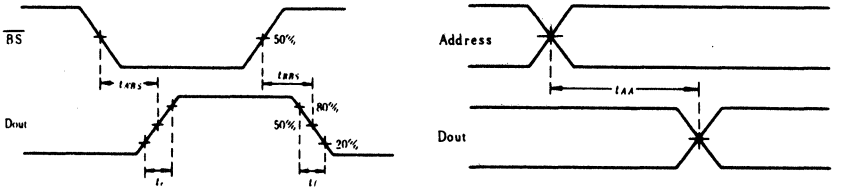
1. LOADING CONDITION



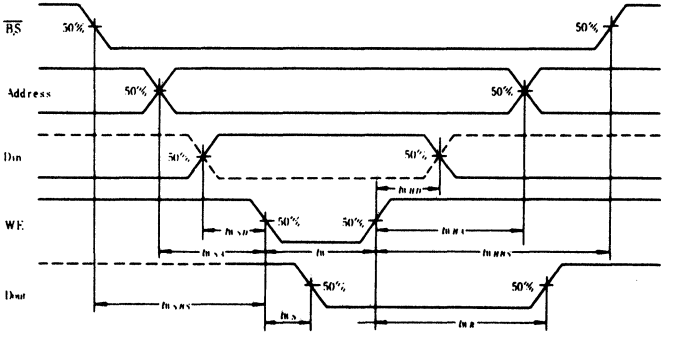
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



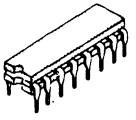
HM100415,HM100415CG

1024-word×1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.

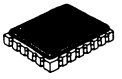
The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

HM100415



(DG-16A)

HM100415CG



(CG-24)

■ FEATURES

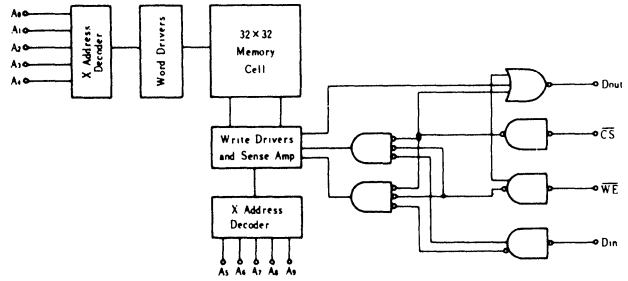
- Level ..... 100K ECL Compatible
- Organization ..... 1024-word by 1-bit
- Address Access Time ..... 10ns (max)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

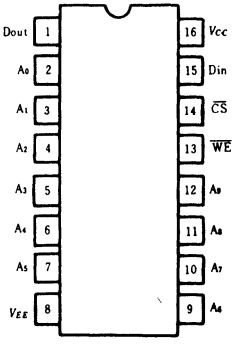
Notes) × : Irrelevant
* : Read Out NonInvert

■ BLOCK DIAGRAM



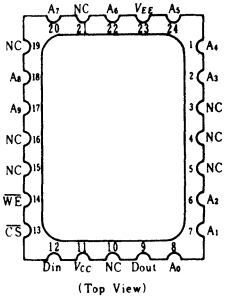
■ PIN ARRANGEMENT

● HM100415



(Top View)

● HM100415CG



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−150	—	mA

● AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	3	5	ns
Chip Select Recovery Time	t_{RCS}		—	3	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	6	4	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W = 6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		2	0	—	ns
Chip Select Hold Time	t_{WHCS}		2	0	—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	12	ns

3. RISE/FALL TIME

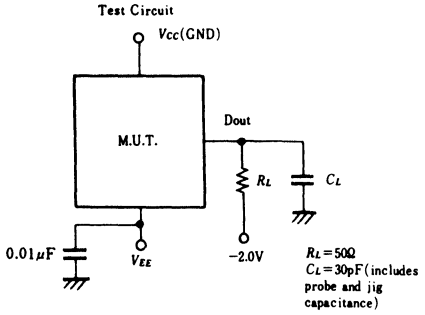
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

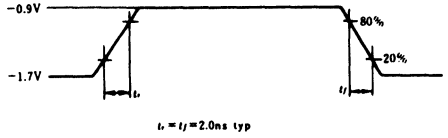
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

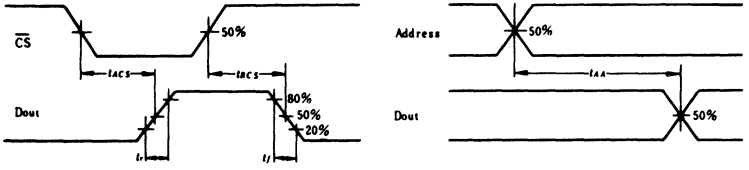
1. LOADING CONDITION



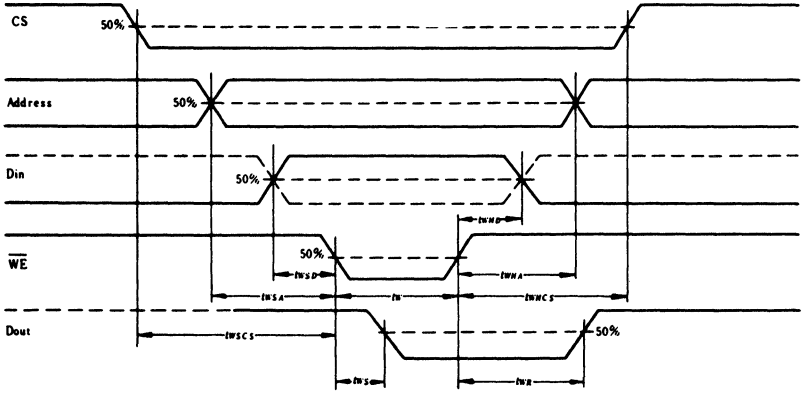
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100474, HM100474F

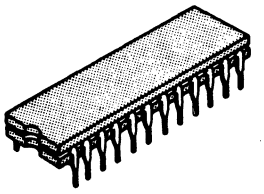
1024-word×4-bit Fully Decoded Random Access Memory

The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

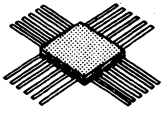
The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

HM100474



(DG-24N)

HM100474F



(FG-24)

■ FEATURES

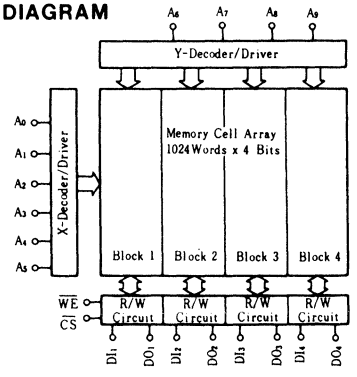
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 25ns(max)
- Write pulse width: 25ns(min)
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



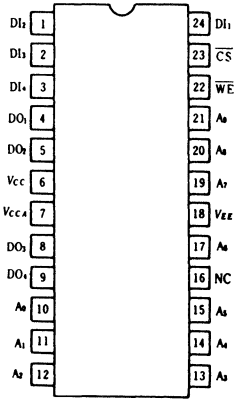
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

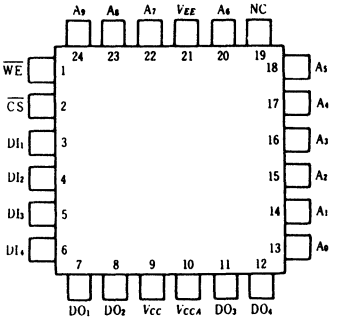
■ PIN ARRANGEMENT

● HM100474



(Top View)

● HM100474F



(Top View)

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■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = $t_W$min	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	27	ns

3. RISE/FALL TIME

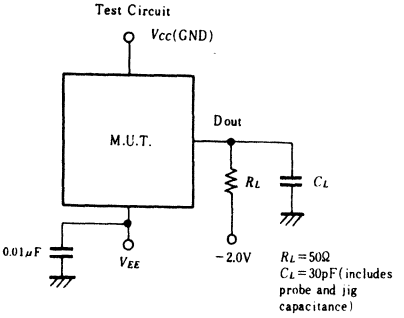
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

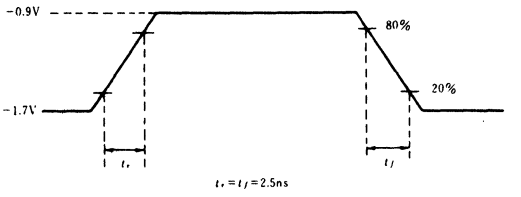
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

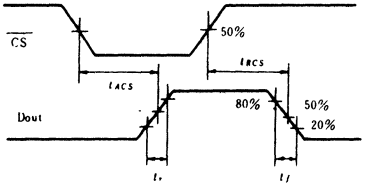
1. LOADING CONDITION

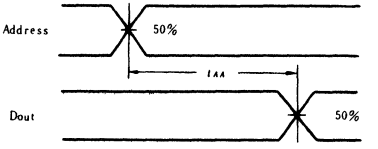


2. INPUT PULSE

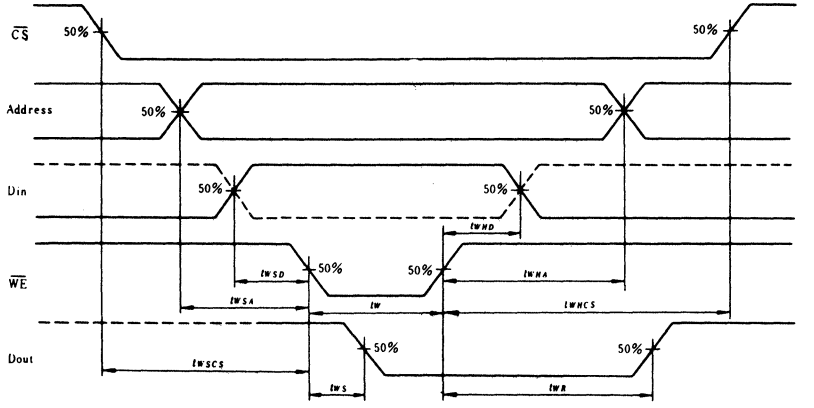


3. READ MODE





4. WRITE MODE



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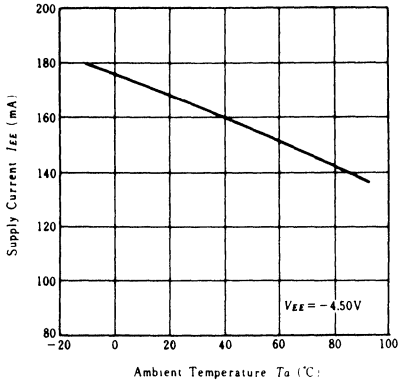
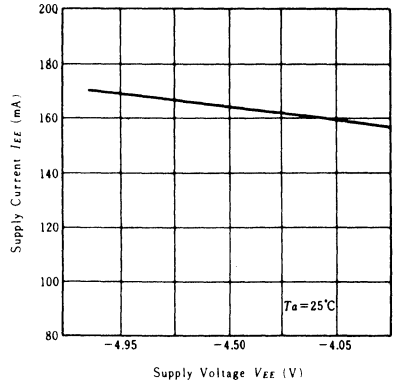
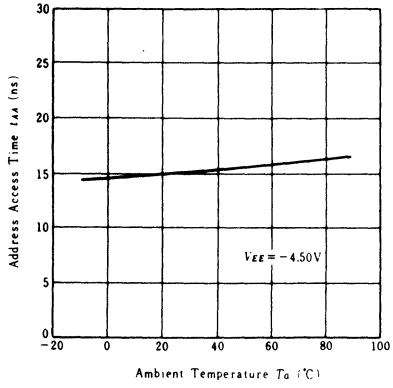
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



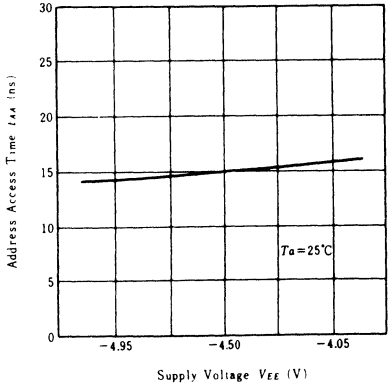
SUPPLY CURRENT vs. SUPPLY VOLTAGE



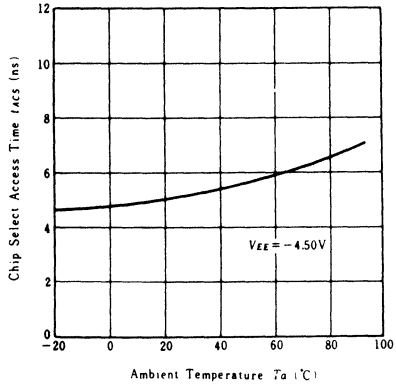
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



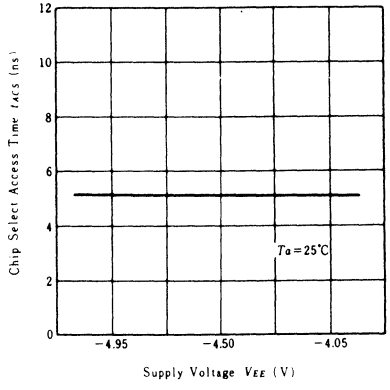
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



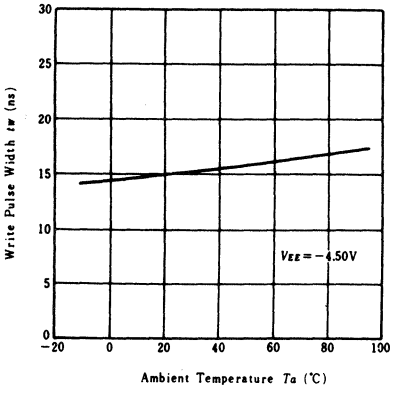
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



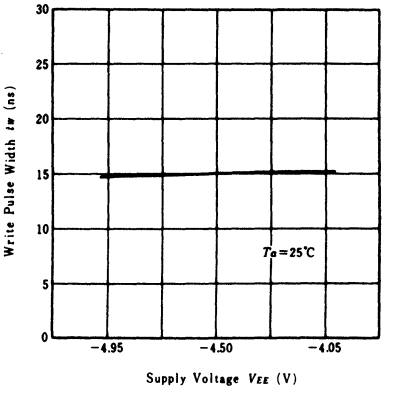
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

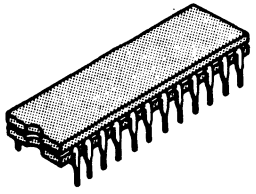


HM100474-8, HM100474-10
HM100474F-8, HM100474F-10

1024-word × 4-bit Fully Decoded Random Access Memory

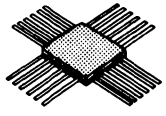
The HM100474 is ECL 100k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process is the Hitachi's U-groove isolation method.
The HM100474 is encapsulated in cerdip-24 pin and flat 24 pin package, compatible with Fairchild's F100474.

HM100474-8, HM100474-10



(DG-24A)

HM100474F-8, HM100474F-10



(FG-24)

■FEATURES

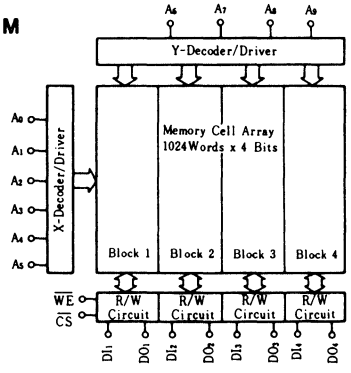
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474-8 8ns (max)
  HM100474-10 10ns (max)
- Write pulse width: HM100474-8 5ns (min)
  HM100474-10 5ns (min)
- Low poer dissipation: 0.3mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

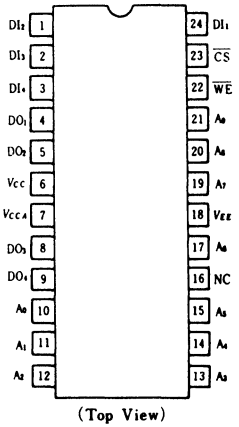
Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



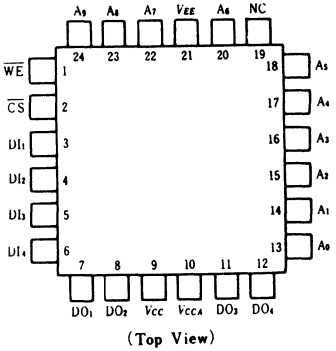
■PIN ARRANGEMENT

- HM100474-8, HM100474-10



(Top View)

- HM100474F-8, HM10047F-10



(Top View)

■ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−240	−220	—	mA

● AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100474/F-8			HM100474/F-10			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	6	s
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	6	ns
Address Access Time	t_{AA}		—	—	8	—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100474/F-8			HM100474/F-10			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 2ns	5	—	—	5		—	ns
Data Setup Time	t_{WSD}		1	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	2	—	—	ns
Address Steup Time	t_{WSA}	t_W = t_W min	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		1	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	6	ns
Write Recovery Time	t_{WR}		—	—	9	—	—	12	ns

3. RISE/FALL TIME

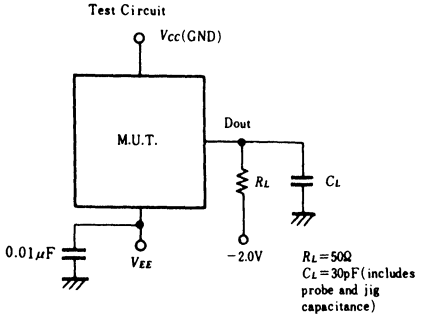
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

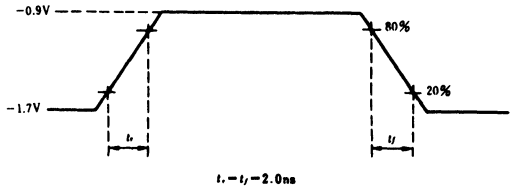
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

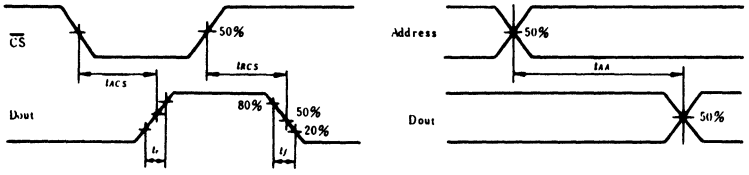
1. LOADING CONDITION



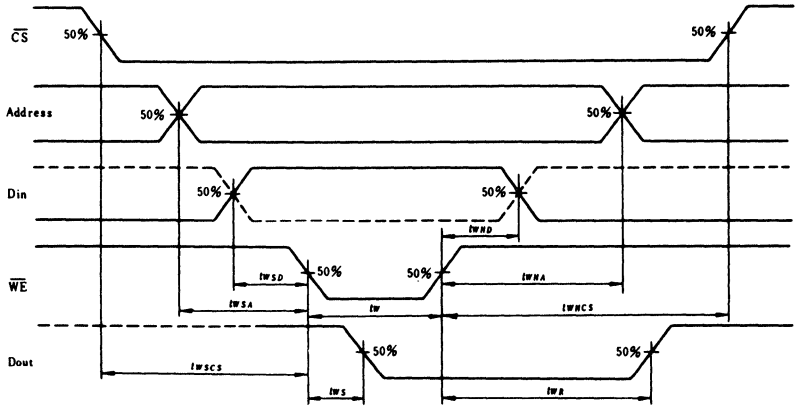
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



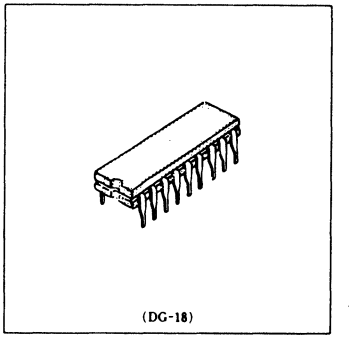
HM100470

4096-word×1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.



(DG-18)

■ FEATURES

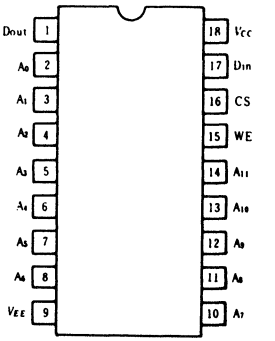
- 4096-word x 1-bit organization
- Full compatible with 100K ECL level
- Address access time: 25ns(max)
- Write pulse width: 25ns (min)
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
CS	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

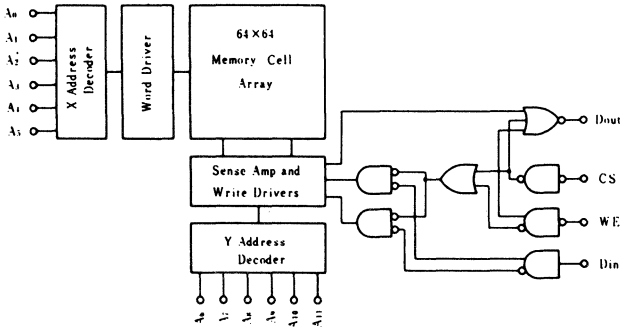
Notes) × : Irrelevant
* : Read Out Nonivert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}			—	10	ns
Chip Select Recovery Time	t_{RCS}			—	10	ns
Address Access Time	t_{AA}			—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	25	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—		ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	27	ns

3. RISE/FALL TIME

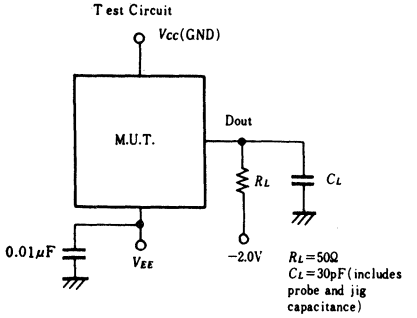
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

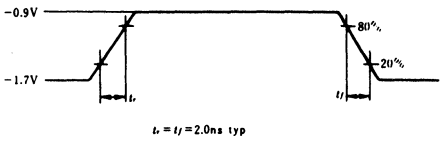
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

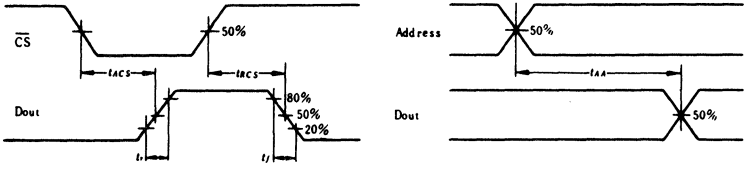
1. LOADING CONDITION



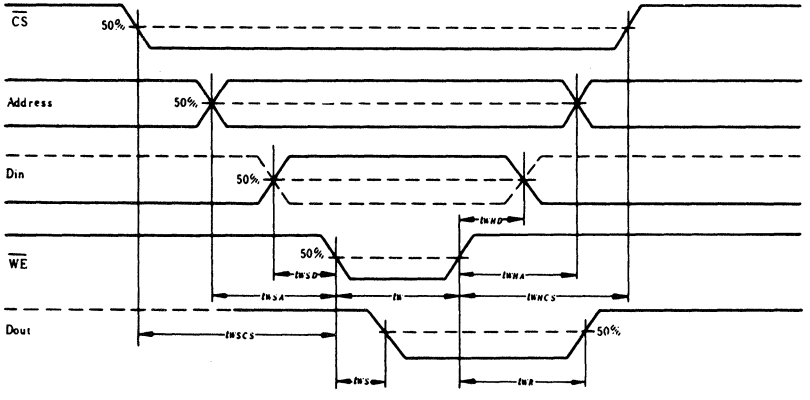
2. INPUT PULSE



3. READ MODE



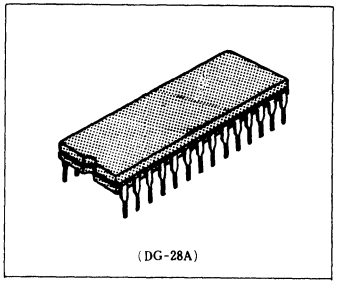
4. WRITE MODE



HM100484-10 — Preliminary

4096-wrod x 4-bit Fully Decoded Random Access Memory

The HM100484 is ECL 100k compatible, 4096-words by 4-bits read/write random access memory developed for high speed systems such as acratch pads and control/buffer storage.



Features

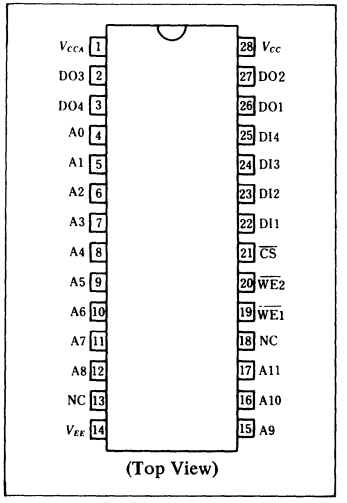
- 4096-word x 4-bits organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 7ns (min)
- Power dissipation: 630mW
- Output obtainable by wired-OR

Function Table

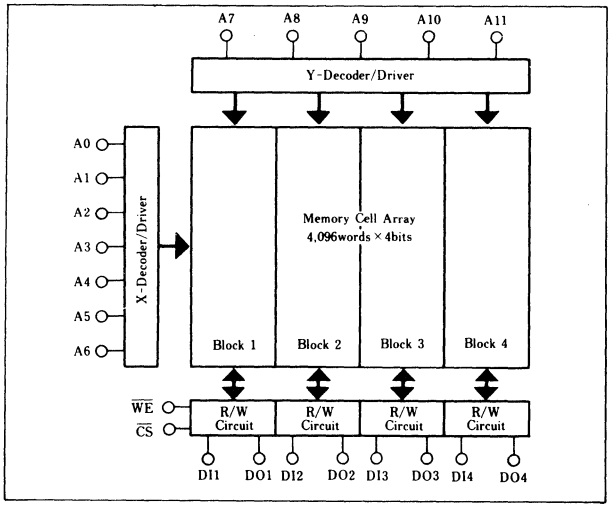
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

Notes) ×: Irrelevant
*: Read Out Nonivert

Pin Arrangement



Block Diagram



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

* Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	V_{in}=V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	V_{in}=V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Inputs Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	μA	V_{in}=V_{IHA}
	I_{IL}	0.5	—	170	μA	$\overline{CS}$ — V_{in}=V_{ILB}
		−50	—	—		Others
Supply Current	I_{EE}	−180	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	6	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	ns	
Address Access Time	t_{AA}	—	—	10	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	7	—	—	ns	t_{WSA}=t_{WSA} min
Data Setup Time	t_{WSD}	1	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	ns	
Address Setup Time	t_{WSA}	1	—	—	ns	t_W=t_W min
Address Hold Time	t_{WHA}	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	1	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	ns	
Write Recovery Time	t_{WR}	—	—	12	ns	

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Rise/Fall Time

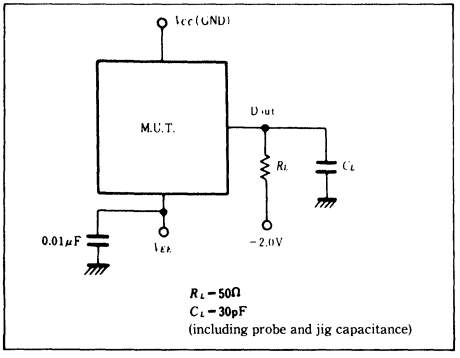
Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

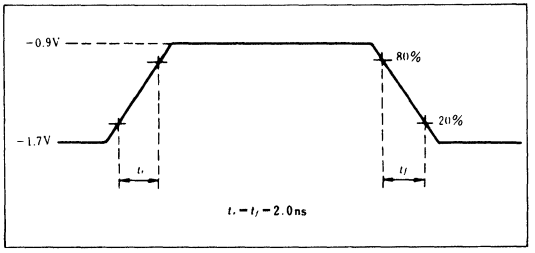
Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

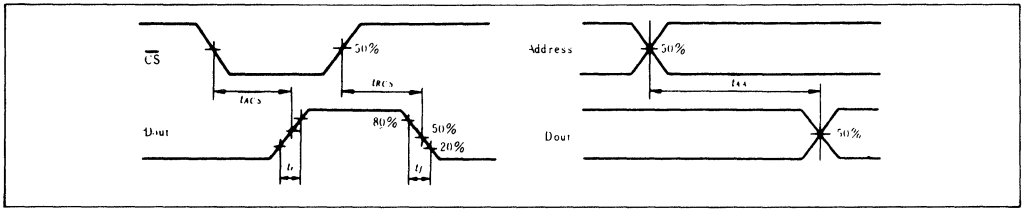
Loading Condition



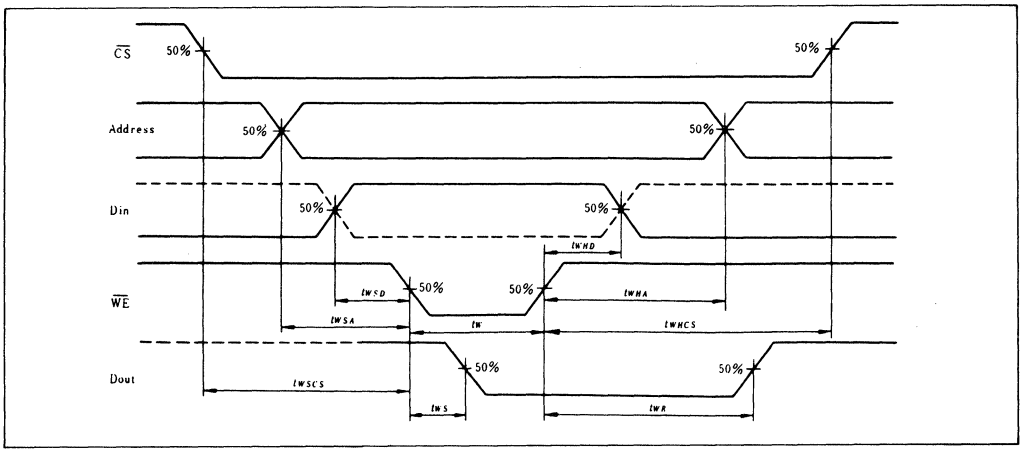
Input Pulse



Read Mode



Write Mode

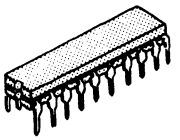

$\overline{CS}$
Address
Din
$\overline{WE}$
Dout
50%
t_{WHD}
t_{WSD}
t_{WHA}
t_{WSA}
t_W
t_{WHCS}
t_{WSCS}
t_{WS}
t_{WR}

HM100480-15, HM100480F-15

16,384-words × 1-bit Fully Decoded Random Access Memory

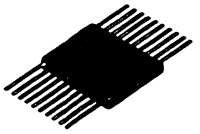
The HM100480-15 is ECL 100K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's U-groove isolation method.
The HM100480-15 is encapsulated in cerdip-20 pin and flat-20 pin package, compatible with Fairchild's 100480.

HM100480-15



(DG-20N)

HM100480F-15



(FG-20D)

■FEATURES

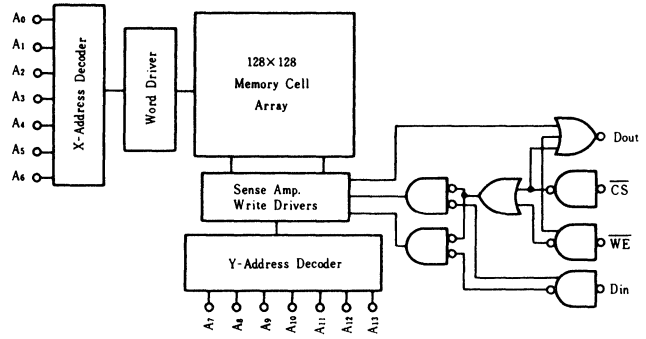
- 16,384-words x 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 15ns (max)
- Write pulse width: 15ns (min)
- Low power dissipation: 0.06mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

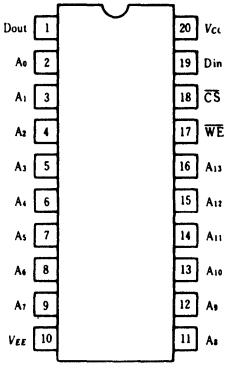
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Input		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−220	—	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ± 5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	8	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	ns
Address Access Time	t_{AA}		3	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min	3	—	—	ns
Address Hold Time	t_{WHA}		3	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	12	ns
Write Recovery Time	t_{WR}		—	—	17	ns

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3. RISE/FALL TIME

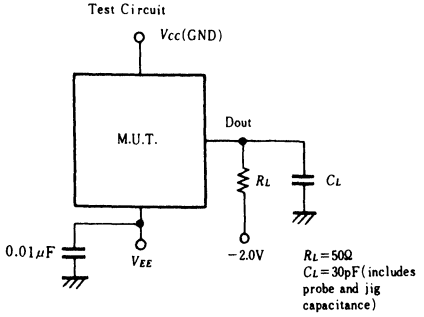
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

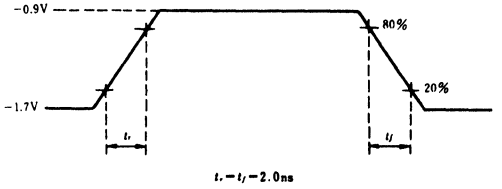
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

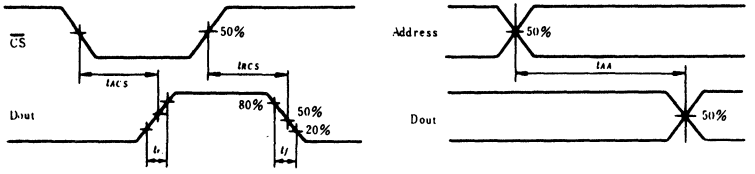
1. LOADING CONDITION



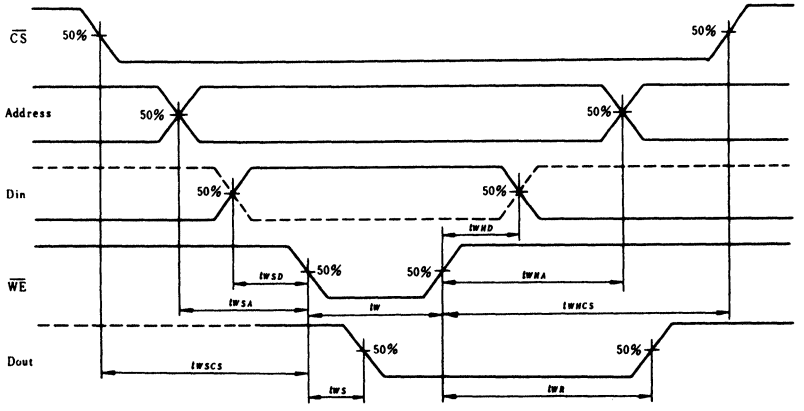
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

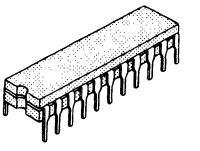


HM100490-15 — Preliminary

65536-words x 1-bit Fully Decoded Random Access Memory

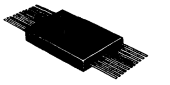
HM100490-15 is ECL 100k compatible, 65536-words x 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

HM100490-15



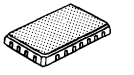
(DG-22N)

HM100490F-15



(FG-22D)

HM100490CG-15



(CG-22A)

Features

- 65,536-words x 1-bit organization
- Fully compatible with 100k ECL level
- Address access time . . . . . 15ns (max.)
- Write pulse width . . . . . 10ns (min.)
- Low power dissipation . . . . . 320mW (typ.)
- Output obtainable by wired-OR (open emitter)

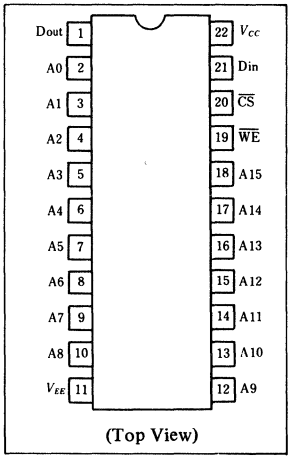
Function Table

Iuput			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

Notes) ×: Irrelevant
*: Read Out Noninvert

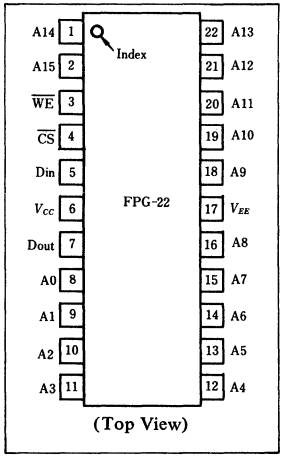
Pin Arrangement

- HM100490-15



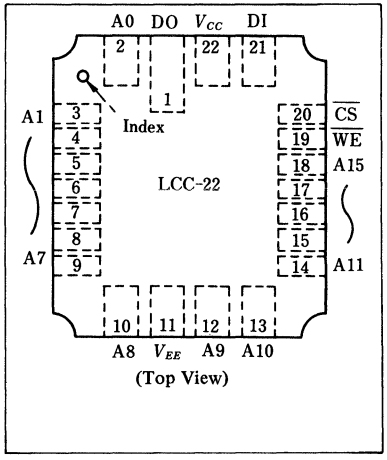
(Top View)

- HM100490F-15



(Top View)

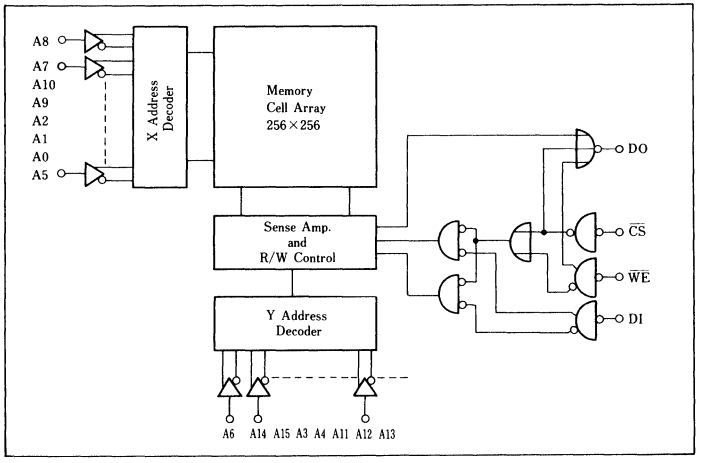
- HM100490CG-15



(Top View)

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to −3.0	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

*Under Bias

Electrical Characteristics

DC Characteristics

(V_{EE} = -4.5V, R_L = 50Ω to -2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	V_{in}=V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	V_{in}=V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Inputs Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	μA	V_{in}=V_{IHA}
	I_{IL}	0.5	—	170	μA	V_{in}=V_{ILB} $\overline{CS}$
		−50	—	—		Others
Supply Current	I_{EE}	−120	—	—	mA	All Inputs and Outputs Open

AC Characteristics

(V_{EE} = -4.5V ± 5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	10	ns	
Chip Select Recovery Time	t_{RCS}	—	—	10	ns	
Address Access Time	t_{AA}	—	—	15	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	10	—	—	ns	t_{WSA}=2ns
Data Setup Time	t_{WSD}	2	—	—	ns	
Data Hold Time	t_{WHD}	3	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	ns	t_W=10ns
Address Hold Time	t_{WHA}	3	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	ns	
Chip Select Hold Time	t_{WRCS}	3	—	—	ns	
Write Disable Time	t_{WS}	—	—	10	ns	
Write Recovery Time	t_{WR}	—	—	18	ns	

Rise/Fall Time

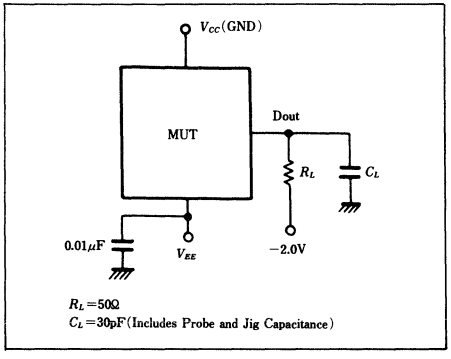
Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

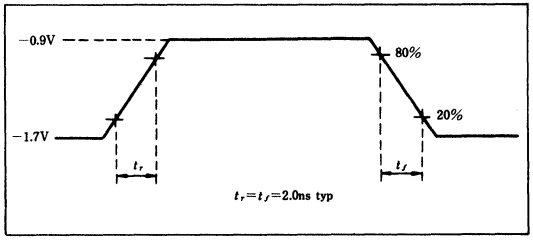
Test Circuit and Waveforms

Loading Condition

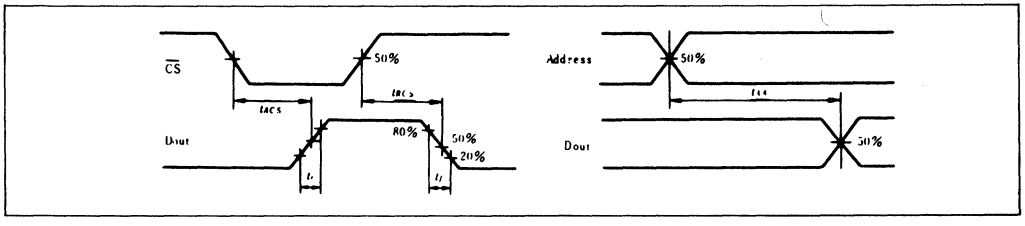


R_L=50Ω
C_L=30pF(Includes Probe and Jig Capacitance)

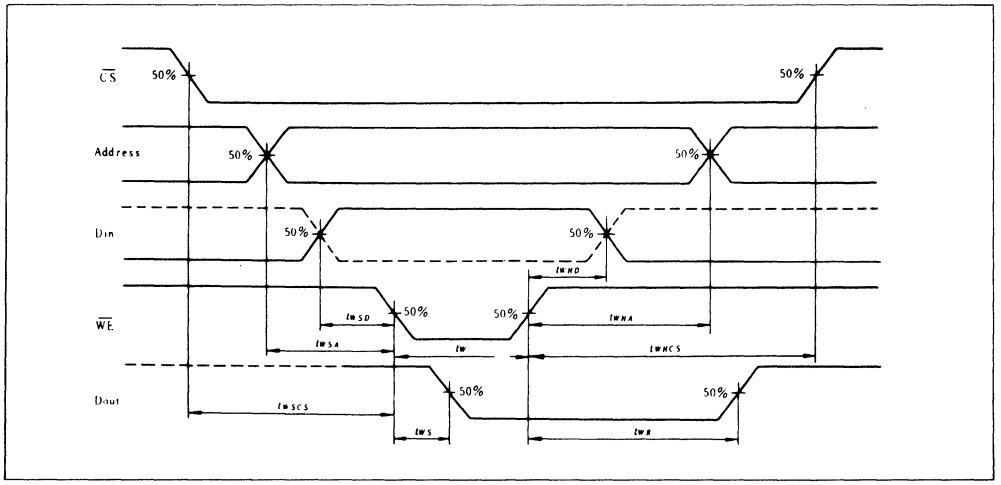
Input Pulse



Read Mode



Write Mode


CS
Address
Din
WE
Dout
50%
tWHD
tWSD
tWHA
tWSA
tW
tWHCS
tWSCS
tWS
tWR

NOTES

NOTES

NOTES

NOTES

HITACHI AMERICA, LTD.
SEMICONDUCTOR AND IC DIVISION

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Fax: 408-435-2782

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