ASSP

COMMUNICATION CONTROL SCSI-2 PROTOCOL CONTROLLER

MB86603

DESCRIPTION

The MB86603 is a SCSI-2 protocol controller (SPC) that facilitates interface control between the host computer (medium/small) and peripheral devices. The specifications conform to the SCSI-2 standard but have an improved baud rate and extended functions.

The MB86603 supports high-speed synchronous transfer, wide transfer (16 bits), the MPU/DMA stand-alone system bus, and programmable commands, to enable configuration of high-performance systems.

The MB86603 (SPC hereafter) is applicable to both single-end and differential transmissions and has a driver/receiver that can drive single-end heavy current (48 mA).

It can also have the phase-to-phase sequence control function to reduce the program overhead of the host MPU. For the abbreviations in this data sheet, see the next page.

FEATURES

SCSI Bus Interface

- **Operable as initiator and target**

- **Two types of data transfer**
    - Synchronous transfer: Max. 20 Mbytes/s, max. 32 offsets, 32-level baud rate
    - Asynchronous transfer: Max. 10 Mbytes/s
- **Transfer parameters (transfer mode, baud rate, transfer offset for 15 connected devices)**

- **Single-end and differential transmissions**
    Driver/receiver capable of driving 48-mA single-end heavy current

- **Tristate bidirectional buffers for transfer control signals ($\overline{REQ}$, $\overline{ACK}$)**

**176-Lead Plastic SQFP Package
FPT-176P-M01**
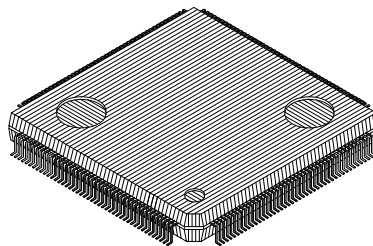
Transfer Operation

- **Automatic response to selection/reselection**

  Prespecified receiving performed automatically at selection or reselection
  Initiator: Automatically responds to reselection from target and operable until message received
  Target: Automatically responds to selection from initiator and can operate until command received

- **Automatic receiving**

  Initiator: Can automatically receive information for new phase to which target shifted
  Target: Can perform automatic receiving in response to attention condition generated by initiator

- **64-byte data register (FIFO) for data phase**

- **Two (send-only and receive-only) 32-byte memory data buffers for message, command, and status phases**

- **16-bit transfer block and 24-bit transfer byte registers enabling 1Tbyte transfer (1Tbyte: 16 Mbytes x 64 Kblocks)**

- **Independent data transfer bus enabling microprocessor to operate during data transfer**

- **Selection between parity through and generate**

System Bus Interface

- **16-bit MPU/DMA stand-alone system bus**

- **Direct connection with 68 series/80 series 16-bit MPUs**

- **Two types of transfer**

  Program transfer
  DMA transfer (burst mode)
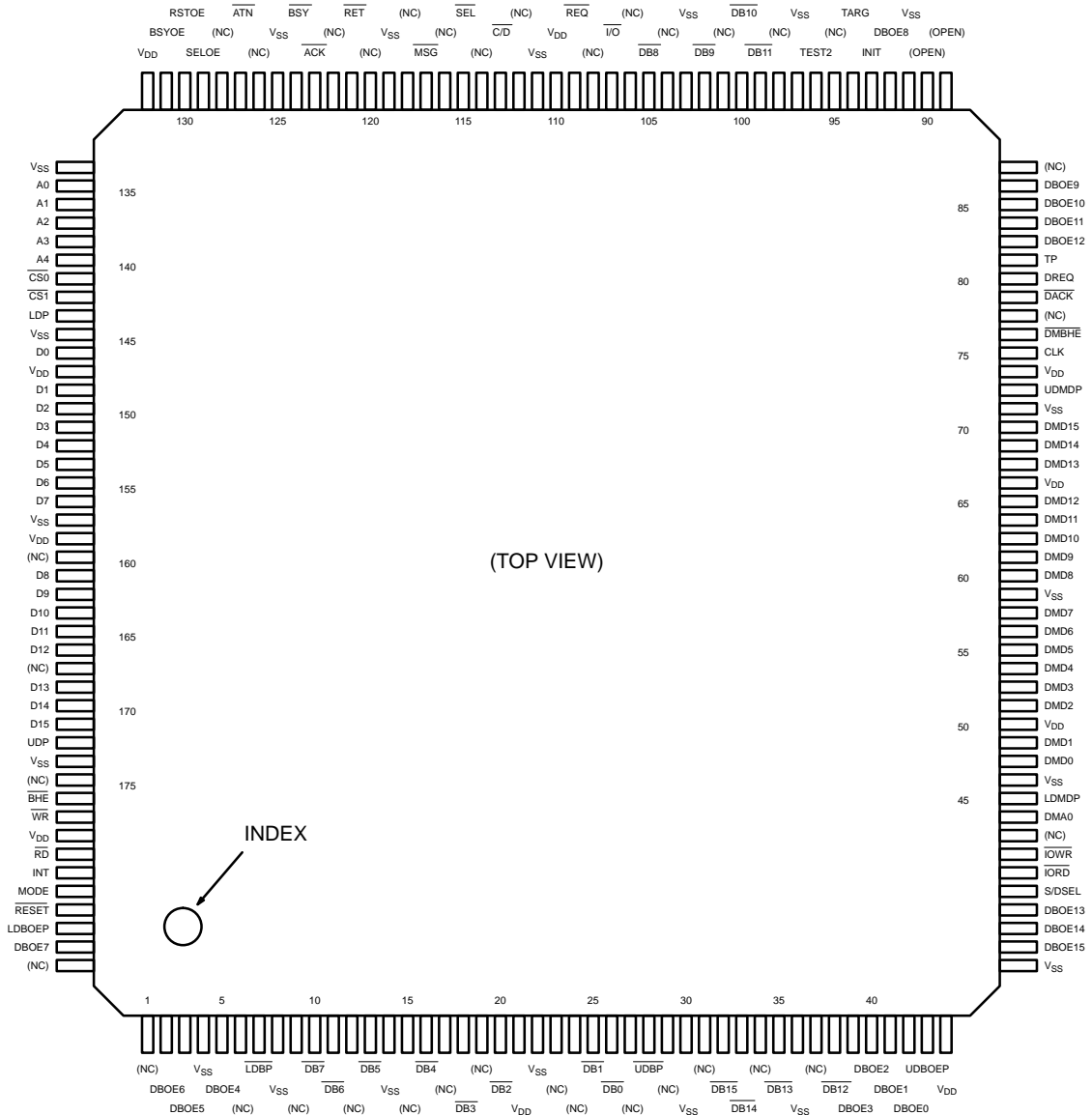
Commands

- **Sequential command for sequential operation and programmable command for programming, including ordinary commands**

- **Command queuing**

  Commands can be tagged in the command phase for continuous issuing.

- **512-byte memory as command program memory and command queue buffer**

Others

- **CMOS**

- **System clock frequency: 12 MHz to 32 MHz**

- **+5 V single power supply**

  SCSI-2: Enhanced Small Computer System Interface
  ANSI: American National Standard Institute
  SPC: SCSI-2 Protocol Controller
  MPU: Micro-Processing Unit
  DMA: Direct Memory Access
  FIFO: First-In First-Out
  ID: Identifier (identification number assigned to each device connected to SCSI bus)
  80 series: General term for MPU based on command system of 8080A developed by Intel
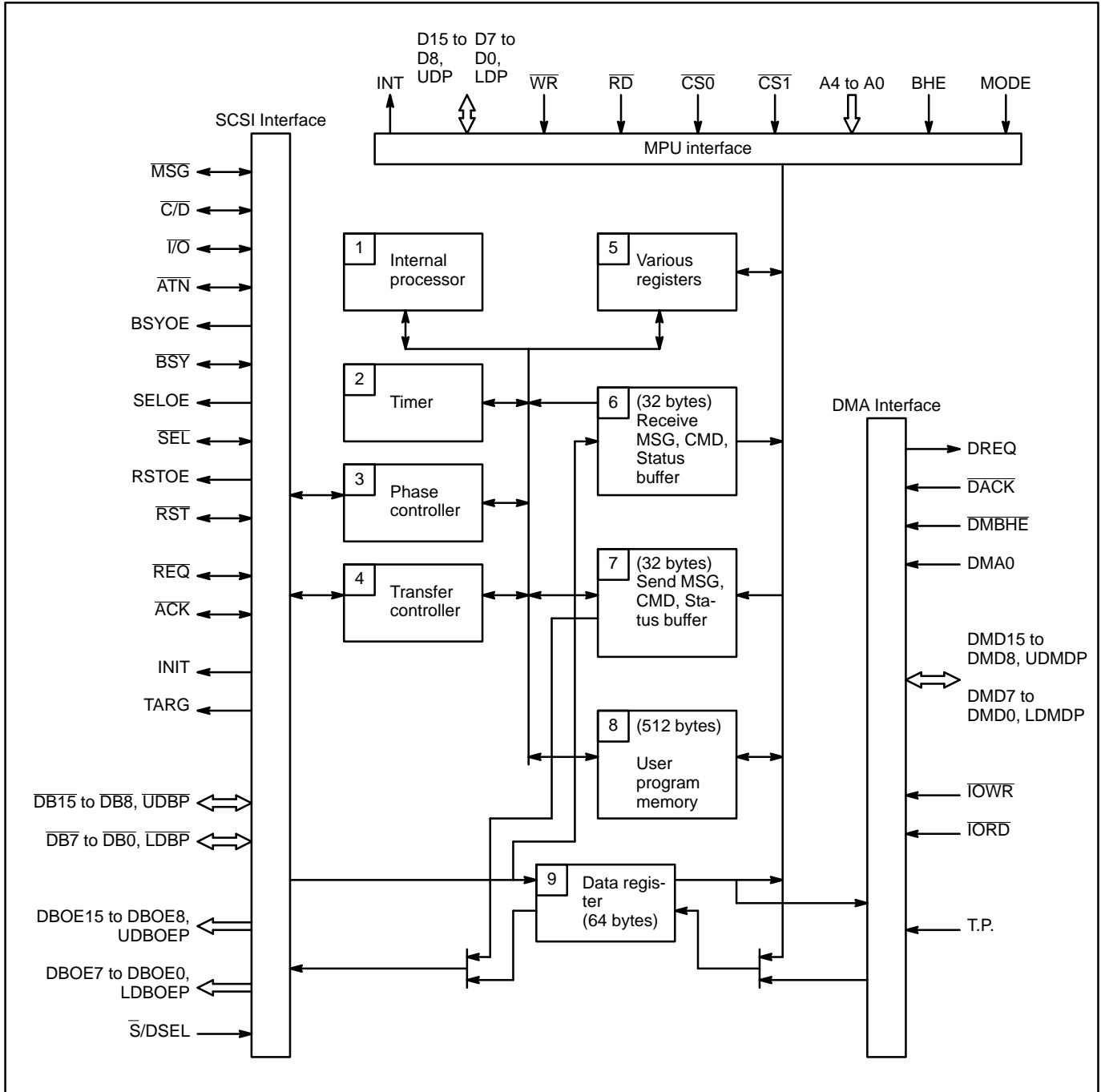 68 series: General term for MPU developed by Motorola

PIN ASSIGNMENT

RSTOE ATN BSY RET (NC) SEL (NC) REQ (NC) VSS DB10 VSS TARG VSS

BSYOE (NC) VSS (NC) VSS (NC) C/D VDD I/O (NC) (NC) (NC) (NC) DBOE8 (OPEN)

VDD SELOE (NC) ACK (NC) MSG (NC) VSS (NC) DB8 DB9 DB11 TEST2 INIT (OPEN)

130   125   120   115   110   105   100   95   90

(TOP VIEW)

INDEX

Left side (pins 135–176):
VSS, A0, A1, A2, A3, A4, CS0, CS1, LDP, VSS, D0, VDD, D1, D2, D3, D4, D5, D6, D7, VSS, VDD, (NC), D8, D9, D10, D11, D12, (NC), D13, D14, D15, UDP, VSS, (NC), BHE, WR, VDD, RD, INT, MODE, RESET, LDBOEP, DBOE7, (NC)

Right side (pins 85–45):
(NC), DBOE9, DBOE10, DBOE11, DBOE12, TP, DREQ, DACK, (NC), DMBHE, CLK, VDD, UDMDP, VSS, DMD15, DMD14, DMD13, VDD, DMD12, DMD11, DMD10, DMD9, DMD8, VSS, DMD7, DMD6, DMD5, DMD4, DMD3, DMD2, VDD, DMD1, DMD0, VSS, LDMDP, DMA0, (NC), IOWR, IORD, S/DSEL, DBOE13, DBOE14, DBOE15, VSS

Bottom numbers: 1   5   10   15   20   25   30   35   40

(NC) VSS LDBP DB7 DB5 DB4 (NC) VSS DB1 UDBP (NC) (NC) (NC) DBOE2 UDBOEP

DBOE6 DBOE4 VSS DB6 VSS (NC) DB2 (NC) DB0 (NC) DB15 DB13 DB12 DBOE1 VDD

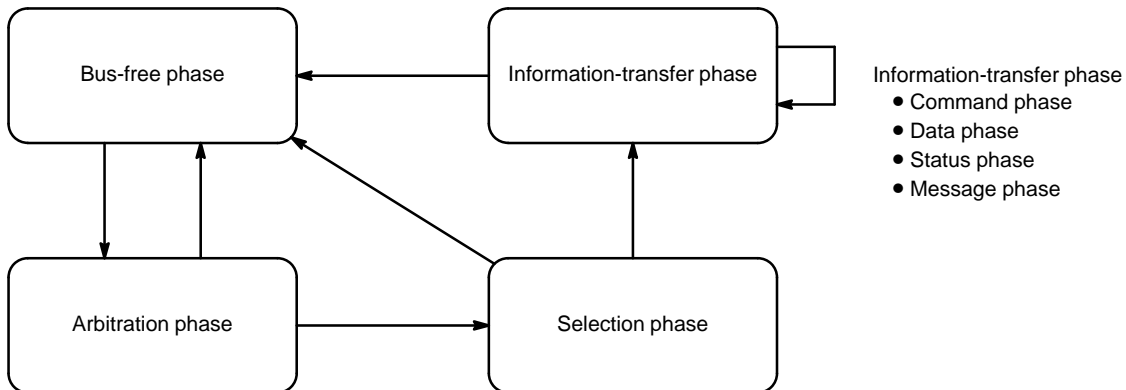DBOE5 (NC) (NC) (NC) (NC) DB3 VDD (NC) (NC) VSS DB14 VSS DBOE3 DBOE0

(FPT-176P-M01)

3

BLOCK DIAGRAM

BLOCK DESCRIPTION

1. Internal processor (sequensor)

This processor provides sequence control between each phase.

```
┌──────────────────┐              ┌──────────────────────────┐        Information-transfer phase
│                  │◄─────────────│                          │◄──┐       ● Command phase
│  Bus-free phase  │              │ Information-transfer phase│───┘       ● Data phase
│                  │              │                          │           ● Status phase
└──────────────────┘              └──────────────────────────┘           ● Message phase
      │   ▲      ▲                          ▲
      ▼   │        ╲                        │
┌──────────────────┐    ╲          ┌──────────────────┐
│                  │      ╲         │                  │
│ Arbitration phase│──────────────►│  Selection phase │
│                  │                │                  │
└──────────────────┘                └──────────────────┘
```

2. Timer

This timer manages timing specified by the SCSI and the following timing.

- $\overline{REQ}/\overline{ACK}$ assertion time for data at asynchronous transfer
- Selection/reselection retry time
- Selection/reselection timeout time
- $\overline{REQ}/\overline{ACK}$ timeout time during transfer

  Asynchronous transfer (target): Time required for initiator to assert $\overline{ACK}$ signal after asserting $\overline{REQ}$ signal

  Asynchronous transfer (initiator): Time required for target to negate $\overline{REQ}$ signal after asserting $\overline{ACK}$ signal

  Synchronous transfer (target only):   Time required for target to send $\overline{REQ}$ signal and then receive $\overline{ACK}$ signal for setting offset to 0 from
  initiator

3. Phase Controller

This controller controls the arbitration, selection/reselection, data in/out, command, status, and message in/out phases executed on the SCSI bus.

4. Transfer Controller

This controller controls the information (data, command, status, message) transfer phase executed on the SCSI bus.

There are two transfer types for executing the information transfer phase.

- Asynchronous transfer: Control by interlocking $\overline{REQ}$ and $\overline{ACK}$ signals
- Synchronous transfer: Control with maximum of 32-byte offset value in data in/out phase

There are two types of modes depending on the data movement as follows:

- Program transfer: Performed via MPU interface using data registers
- DMA transfer: Performed via DMA interface using DREQ and $\overline{DACK}$ pins

At synchronous transfer, the transfer parameters (transfer mode, minimum cycle period of $\overline{REQ}$ or $\overline{ACK}$ signal sent from SPC in synchronous transfer, and maximum $\overline{REQ}/\overline{ACK}$ offset value in synchronous transfer) can be saved for each ID and automatically set when the data phase is started. The transfer byte count is determined by block length x number of blocks.

5. Various Registers

The main registers are as follows:

- Command register
  This register specifies each command with an 8-bit code.
  If the user program is used, the starting address of the program assigned to the user program memory is specified.

- Nexus status register
  This register indicates the chip's operating condition, linked partner's ID, and data register status.

- SCSI control signal status register
  This register indicates the status of the SCSI control signals.

- Interrupt status register
  This register indicates the interrupt status with an 8-bit code.

- Command step register
  This register indicates the execution status of each command with an 8-bit step code.
  Referencing the interrupt status register and this register permits analysis of error causes.

- Group 6/7 command-length setting register
  This register sets the group 6/7 command length not defined in the SCSI standard.
  Setting this register permits group 6/7-command length decisions.

6. Receive MSG, CMD, Status Buffer (RECEIVE MCS Buffer)

This is a 32-byte receive-only information buffer that holds the message, command, and status information received from the SCSI bus.

7. Send MSG, CMD, Status Buffer (SEND MCS Buffer)

This is a 32-byte send-only information buffer that holds the message, command, and status information sent on the SCSI bus.

8. User Program Memory

This is a 512-byte program memory that stores programmable commands. It consists of two 256-byte banks.

9. Data Register

This is a 64-byte FIFO-type data register that holds data when the data phase is executed on the SCSI bus.

PIN DESCRIPTION

1. SCSI Interface

There are two types of SCSI interface corresponding to two types of transmission systems; each type operates differently.

Pin No.	Pin Symbol	Pin Name	I/O	Function
109	$\overline{\text{REQ}}$	Request	I/O	**This is used for transfer request signals from the target to the initiator in the information-transfer phase.** The input signal is used as a data transfer sequence timing control signal. The signal is Active Low.
123	$\overline{\text{ACK}}$	Acknowledge	I/O	**This is used for response signals from the initiator to the target in response to the $\overline{\text{REQ}}$ signal in the information-transfer phase.** The input signal is used as a data transfer sequence timing control signal. The signal is Active Low.
127	$\overline{\text{ATN}}$	Attention	I/O	**This is used for request signals for the message-transfer phase from the initiator to the target.** The signal is Active Low.
117	$\overline{\text{MSG}}$*	Message	I/O	**This is used for signals specifying the type of information transmitted on the data bus.** The signal is Active Low and goes Low when specifying the message phase.
113	$\overline{\text{C/D}}$*	Controll/Date	I/O	**This is used for signals for specifying the type of information transmitted on the data bus.** The signal is Active Low and goes Low when specifying the command, status, and message phases.
107	$\overline{\text{I/O}}$*	Input/Output	I/O	**This is used for signals for specifying the transfer direction of information transferred on the data bus.** The signal is Active Low. At Low, information is transferred from the target to the initiator. At High, information is transferred from the initiator to the target.
124	$\overline{\text{BSY}}$	Busy	I/O	**This indicates that the SCSI bus is busy.** In the arbitration phase, this pin is used for signals requesting bus acquisition. The signal is Active Low.
115	$\overline{\text{SEL}}$	Select	I/O	**This is used for input of signals that are output and detected by the initiator and target in the selection phase (the initiator selects the target) and reselection phase (the target reselects the initiator).** The signal is Active Low.
121	$\overline{\text{RST}}$	Reset	I/O	**This is used for output of reset signals to other SCSI devices and for input of reset signals from other SCSI devices.** The signal is Active Low.
131	BSYOE**	Busy Output Enable	O	**This is used for output control of $\overline{\text{BSY}}$ signals.** In the differential mode, this pin should be used for control signals for the external differential driver/receiver. The signal is Active High.

(Continued)

Pin No.	Pin Symbol	Pin Name	I/O	Function
129	SELOE**	Select Output Enable	O	**This is used for output control of $\overline{\text{SEL}}$ signals.** In the differential mode, this pin should be used for control signals for the external differential driver/receiver. The signal is Active High.
130	RSTOE**	Reset Output Enable	O	**This is used for output control of $\overline{\text{RST}}$ signals.** In the differential mode, this pin should be used for control signals for the external differential driver/receiver. The signal is Active High.
32, 33, 35 38, 99, 100, 102, 105, 28, 10, 11, 13 16, 18, 20 25, 26, 7	$\overline{\text{DB15}}$ to $\overline{\text{DB8}}$, $\overline{\text{UDBP}}$, $\overline{\text{DB7}}$ to $\overline{\text{DB0}}$, $\overline{\text{LDBP}}$	Data Bus 15 to Data Bus 8, Upper Data Bus Parity, Data Bus 7 to Data Bus 0, Lower Data Bus Parity	I/O	**These are bidirectional SCSI data buses made up of 2-byte data and each odd parity bit of the upper/lower byte.**
46, 47, 48 84, 85, 86 87, 92, 43, 175, 2, 3, 5, 39, 40, 41, 42, 174	DBOE15 to DBOE8, UDBOEP, DBOE7 to DBOE0, LDBOEP**	Data Bus 15 to 8 Output Enable, Upper Data Bus Output Enable Parity, Data Bus 7 to 0 Output Enable, Lower Data Bus Output Enable Parity	O	**These are used for output control of $\overline{\text{DB15}}$ to $\overline{\text{DB8}}$, $\overline{\text{UDBP}}$, $\overline{\text{DB7}}$ to $\overline{\text{DB0}}$, $\overline{\text{LDBP}}$ signals.** In the differential mode, these pins should be used for control signals for the external differential driver/receiver. The signal is Active High.
93	INIT** ***	Initiator	O	**These are used for signals for indicating the operation or connection condition of the SPC.** These pins should be used for control signals for the external differential driver/receiver. The signal is Active High.
94	TARG** ***	Target	O	
49	$\overline{\text{S}}$/DSEL**	Single-End Differential Select	I	**This is used for input of signals for selecting the chip operation mode.** SINGLE-ENDED: Enter –0. DIFFERENTIAL: Enter –1.

*The correspondence between the $\overline{\text{C/D}}$, $\overline{\text{C/D}}$, $\overline{\text{I/O}}$ signals and phase is given on the next page.

**For the connection example of the external differential driver/receiver circuit, see SYSTEM CONFIGURATION, 5.

***The operation or connection condition of the SPC is given on the next page.

Note: I/O pins for the SCSI interface can be connected directly to the single-end SCSI bus.

Phase Name	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	Transfer Direction	
				Initiator	Target
Data-out phase	H	H	H	$\rightarrow$	
Data-in phase	H	H	L	$\leftarrow$	
Command phase	H	L	H	$\rightarrow$	
Status phase	H	L	L	$\leftarrow$	
Message-out phase	L	L	H	$\rightarrow$	
Message-in phase	L	L	L	$\leftarrow$	

INIT	TARG	Condition
L	L	Not connected to SCSI
L	H	Executing reselection phase or in connection as target
H	L	Executing reselection phase or in connection as initiator

2. MPU Interface

Pin No.	Pin Symbol*	Pin Name	I/O	Function
139	$\overline{CS0}$	Chip Select 0	I	**This is used for signals for the MPU to select the SPC as the I/O device.** The signal is Active Low.
140	$\overline{CS1}$	Chip Select 1	I	**This is used for select signals for the MPU to input and output DMA-bus data via the SPC.** The signal is Active Low.
163 to 161, 159 to 155	D15 to D8	Data 15 to Data 8	I/O	**These are used for the upper-byte and parity-bit signals of the data bus.** When the $\overline{CS0}$ input is valid, these pins serve as I/O ports for the registers in the SPC.
164	UDP	Upper Data Parity		When the $\overline{CS1}$ input is valid, these pins serve as data I/O ports for the DMA bus.
151 to 145, 143	D7 to D0	Data 7 to Data 0	I/O	**These are used for lower-byte and parity-bit signals of the data bus.** When the $\overline{CS0}$ input is valid, these pins serve as I/O ports for the registers in the SPC.
141	LDP	Lower Data Parity		When the $\overline{CS1}$ input is valid, these pins serve as data I/O ports for the DMA bus.
138 to 134	A4 to A0	Address 4 to Address 0	I	**These are used to input addresses for selecting the internal register.**
170	$\overline{RD}$ (R/$\overline{W}$)	Read (Read/Write)	I	**In the 80-series mode, this is used for input of signals ($\overline{IORD}$ or $\overline{RD}$) for the read operation from the SPC to the MPU. The signal is Active Low.** In the 68-series mode, this is used for input of control signals (R/$\overline{W}$) for the read and write operations from the MPU to the SPC. The signal is Active High at the read operation and Active Low at the write operation.
168	$\overline{WR}$ ($\overline{LDS}$)	Write (Lower Data Strobe)	I	**In the 80-series mode, this is used for input of signals ($\overline{IOWR}$ or $\overline{WR}$) for the write operation from the MPU to the SPC.** In the 68-series mode, this is used for input of $\overline{LDS}$ signals output by the MPU when the lower bytes of the data bus are valid. The signal is Active Low in both modes.
167	$\overline{BHE}$ ($\overline{UDS}$)	Bus High Enable (Upper Data Strobe)	I	**In the 80-series mode, this is used for input of $\overline{BHE}$ signals output by the MPU when the upper bytes of the data bus are valid.** In the 68-series mode, this is used for input of $\overline{UDS}$ signals output by the MPU when the upper bytes of the data bus are valid. The signal is Active Low in both modes.
171	INT ($\overline{INT}$)	Interrupt Request	O	**This is used for output of interrupt request signals.** In the 80-series mode, the signal is Active High. In the 68-series mode, the signal is Active Low. When SPC BSY = 1 (bit 6 of SPC status register = 1), this signal is not active. Therefore, this signal becomes inactive when a command is issued to the SPC at active, or when the SPC BSY goes to 1 after automatically starting the operation. This signal becomes inactive as soon as the first interrupt code is read, even if more than one interrupt is held.
172	MODE	Mode	I	**This is used to input signals specifying the type of MPU and DMA buses.** A High level is input in the 80-series mode. A Low level is input in the 68-series mode.

*The pin symbols in parentheses are the ones when the MODE input is Low.

3. DMA Interface

Like the MPU interface, the DMA interface has input/output signals for the 68 series and 80 series.

Pin No.	Pin Symbol*	Pin Name	I/O	Function
82	DREQ	DMA Request	O	**This is used for output of DMA transfer request signals to the DMA controller.** A request is made for data transfer between the SPC and the memory over the DMA bus. The signal is Active High.
81	$\overline{\text{DACK}}$	DMA Acknowledge	I	**This is used for input of DMA acknowledge signals from the DMA controller.** When this input pin is active, the DMA cycle (read/write) is executed. The signal is Active Low.
74 to 72, 70 to 66	DMD15 to DMD8	DMA Data 15 to DMA Data 8	I/O	**These are used for input and output of the upper-byte and parity signals of the DMA data bus.** When the CS1 input is valid, these pins are connected directly to the MPU bus.
76	UDMDP	Upper DMA Data Parity		
64 to 59, 57, 56	DMD7 to DMD0	DMA Data 7 to DMA Data 0	I/O	**These are used for input and output of the lower-byte and parity signals of the DMA data bus.** When the CS1 input is valid, these pins are connected directly to the MPU bus.
54	LDMDP	Lower DMA Data Parity		
50	$\overline{\text{IORD}}$ ($\text{DMR}/\overline{\text{W}}$)	I/O Read (DMA Read/Write)	I	**In the 80-series mode, this is used for input of signals ($\overline{\text{IORD}}$ or $\overline{\text{RD}}$) for outputting data from the SPC to the DMA bus.** The signal is Active Low. In the 68-series mode, this is used for input of control signals ($\text{DMR}/\overline{\text{W}}$) for inputting and outputting data from the DMA controller to the SPC. The signal is Active High for output and Active Low for input.
51	$\overline{\text{IOWR}}$ ($\overline{\text{DMLDS}}$)	I/O Write (DMA Lower Data Strobe)	I	**In the 80-series mode, this is used for input of signals ($\overline{\text{IOWR}}$ or $\overline{\text{WR}}$) for inputting data from the DMA bus to the SPC.** In the 68-series mode, this is used for input of LDS signals output by the DMA controller when the lower bytes of the DMA data bus are valid. The signal is Active Low in both modes.
79	$\overline{\text{DMBHE}}$ ($\overline{\text{DMUDS}}$)	DMA Bus High Enable (Upper Data Strobe)	I	**In the 80-series mode, this is used for input of $\overline{\text{BHE}}$ signals output by the DMA controller when the upper bytes of the DMA data bus are valid.** **In the 68-series mode, this is used for input of UDS signals output by the DMA controller when the upper bytes of the DMA data bus are valid.** The signal is Active Low in both modes.
53	DMA0	DMA Address 0	I	**In the 80-series mode, this is used for input of address data A0 signals output by the DMA controller.** In the 68-series mode, this is connected to the power supply (VDD).
83	TP	Transfer Permission	I	**This is used for input of DMA transfer permission signals.** When this signal is active, the SPC performs the DMA transfer. When this signal becomes inactive during DMA transfer, transfer is temporarily stopped at the block boundary. The signal is Active High.

*The pin symbols in parentheses are the ones when the MODE input is Low.

4. Others

Pin No.	Pin Symbol	Pin Name	I/O	Function
173	$\overline{\text{RESET}}$	Reset	I	**This is used for input of system-reset signals.** At input, the reset signals must be kept active for four or more clock cycles. The signal is Active Low.
78	CLK	Clock	I	**This is used for input of clock pulse signals.** The clock frequency ranges from 12 MHz to 32 MHz.
21, 44, 58, 71, 77, 110, 132, 144, 153, 169	V_{DD}	Power Supply	—	**These are used for the +5 V power supply.**
4, 8, 14, 22, 30, 36, 45, 55, 65, 75, 91, 97, 103, 111, 119, 125, 133, 142, 152, 165	V_{SS}	Ground	—	**These are used for grounding.**
96	TEST2	Test	I	**Must be grounded**
89, 90	(OPEN)	(Open)	—	**Must be open. Do not connect.**
1, 6, 9, 12 15, 17, 19 23, 24, 27 29, 31, 34 37, 52, 80 88, 95, 98 101, 104 106, 108, 112, 114, 116, 118, 120, 122, 126, 128, 154, 160, 166, 176	(NC)	(Non Connection)	—	**Not connected internally. As a general rule, do not connect.**

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage*	V_{DD}	$V_{SS} - 0.5$ to $+6.0$	V
Input voltage*	V_I	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Output voltage*	V_O	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Operating ambient temperature	Top	-25 to $+85$	°C
Storage temperature	Tstg	-40 to $+125$	°C

*The voltages are based on V_{SS} (= 0 V).

Note: Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter			Symbol	Requirements			Unit
				Min.	Typ.	Max.	
Supply voltage*			V_{DD}	4.75	5.0	5.25	V
High-level input voltage*	Non-SCSI pins	$\overline{RESET}$	V_{IH}	2.4	—	—	V
		Others		2.2	—	—	V
	SCSI pins			2.0	—	—	V
Low-level input voltage*			V_{IL}	—	—	0.8	V
High-level output current**	Non-SCSI pins		I_{OH}	—	—	–2.0	mA
	SCSI pins	In single-end mode	$\overline{REQ}$, $\overline{ACK}$	—	—	–8.0	mA
			Others	—	—	—	mA
	In differential mode			—	—	–8.0	mA
Low-level output current**	Non-SCSI pins		I_{OL}	—	—	+3.2	mA
	SCSI pins			—	—	+48	mA
Operating ambient temperature			T_A	0	—	+70	°C

*The voltages are based on V_{SS} (= 0 V).
**SCSI pins can be $\overline{UDBP}$, $\overline{DB15}$, to $\overline{DB8}$, $\overline{LDBP}$, $\overline{DB7}$ to $\overline{DB0}$, $\overline{BSY}$, $\overline{SEL}$, $\overline{RST}$, $\overline{ATN}$, $\overline{REQ}$, $\overline{ACK}$, $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/D}$ pins.

Note: The recommended operating conditions are the recommended values for assuring normal logic operation of the LSI. Requirements in electrical characteristics (DC and AC characteristics) are assured within the range of the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

$(V_{DD} = 5 \text{ V} \pm 5\%, V_{SS} = 0 \text{ V}, T_A = 0^\circ C \text{ to } +70^\circ C)$

Parameter			Symbol	Measurement Conditions	Requirements Min.	Requirements Max.	Unit
High-level input voltage*	Non-SCSI pins	$\overline{\text{RESET}}$	V_{IH}	—	2.4	—	V
		Others			2.2	—	V
	SCSI pins				2.0	—	V
Low-level input voltage			V_{IL}	—	—	0.8	V
SCSI-pin input hysteresis			V_{HW}	—	0.2	—	V
High-level output voltage*	Non-SCSI pins		V_{OH}	$I_{OH} = -2.0$ mA	4.2	V_{DD}	V
	SCSI pins — In single-end mode	$\overline{\text{REQ}}, \overline{\text{ACK}}$		$I_{OH} = -8.0$ mA	2.5	—	V
		Others		—	—	—	V
	In differential mode			$I_{OL} = -8.0$ mA	2.5	—	V
Low-level output voltage	Non-SCSI pins		V_{OL}	$I_{OL} = +3.2$ mA	V_{SS}	0.4	V
	SCSI pins			$I_{OL} = +3.2$ mA	V_{SS}	0.4	V
				$I_{OL} = +48.0$ mA	—	0.5	V
Input leakage current			I_{LI}	$V_{IN} = 0$ to V_{DD}	−10	+10	μA
Input/output leakage current**			I_{LOZ}	$V_{IN} = 0$ to V_{DD}	−10	+10	
Supply voltage			I_{DD}	Output open Clock: 32 MHz (operating)	—	70	mA

*SCSI pins can be $\overline{\text{UDBP}}$, DB15, to $\overline{\text{DB8}}$, $\overline{\text{LDBP}}$, DB7 to $\overline{\text{DB0}}$, $\overline{\text{BSY}}$, $\overline{\text{SEL}}$, $\overline{\text{RST}}$, $\overline{\text{ATN}}$, $\overline{\text{REQ}}$, $\overline{\text{ACK}}$, $\overline{\text{MSG}}$, $\overline{\text{C/D}}$, and $\overline{\text{I/D}}$ pins.

**These are leakage currents when the output impedance of tristate-output and bidirectional bus pins is high.
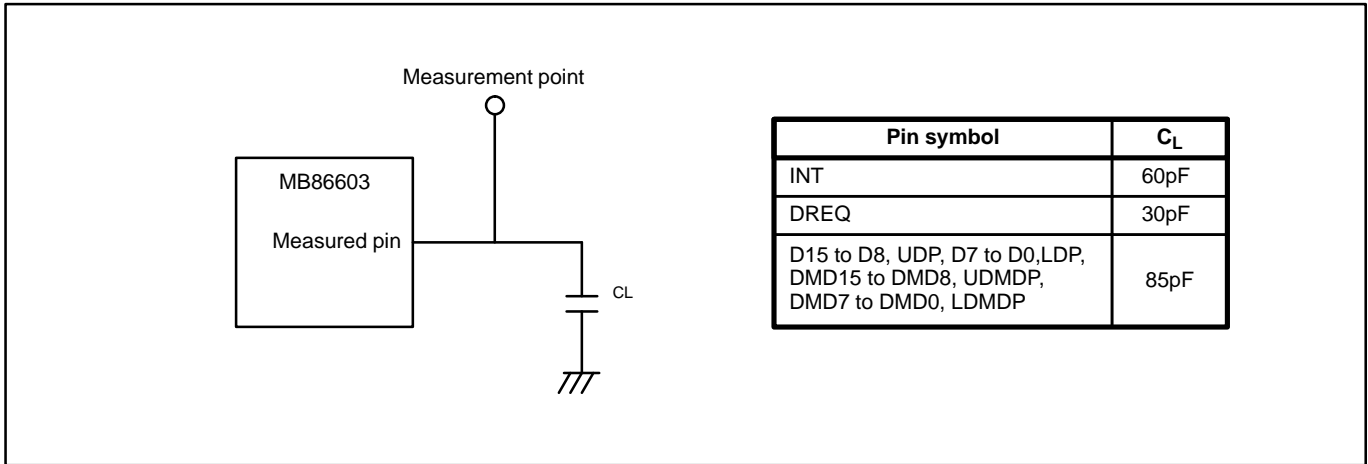
2. Pin Capacitance

$(T_A = +25^\circ C)$

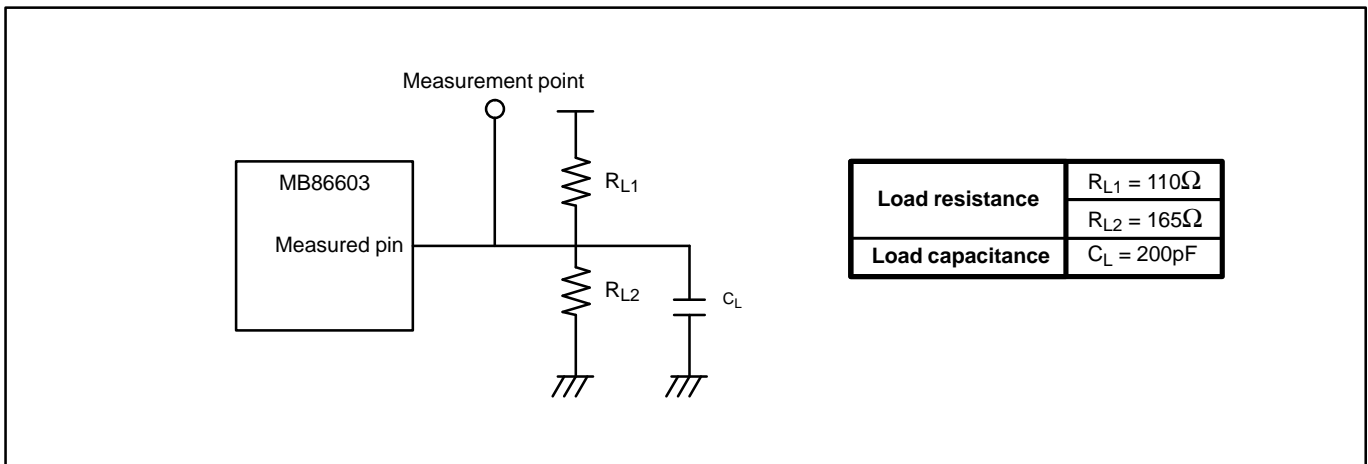| Parameter		Symbol	Measurement Conditions	Requirements Min.	Requirements Max.	Unit
Input-pin capacitance		C_{IN}	$V_{DD} = V_{IN} = 0$ V f = 1 MHz	—	16	pF
Output-pin capacitance		C_{OUT}		—	16	pF
Input/output-pin capacitance	Non-SCSI pins	$C_{I/O}$		—	16	pF
	SCSI pins			—	32	pF

3. Loading Conditions for Measurement of AC Characteristics

(1) Non-SCSI pins

$(V_{DD} = 5 \text{ V} \pm 5\%, V_{SS} = 0 \text{ V}, T_A = 0^{\circ}\text{C to} +70^{\circ}\text{C})$

Measurement point

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Measured pin

CL

Pin symbol	C_L
INT	60pF
DREQ	30pF
D15 to D8, UDP, D7 to D0,LDP, DMD15 to DMD8, UDMDP, DMD7 to DMD0, LDMDP	85pF

(2) SCSI pins

Measurement point

MB86603

Measured pin

R_{L1}

R_{L2} C_L

Load resistance	$R_{L1} = 110\Omega$
	$R_{L2} = 165\Omega$
Load capacitance	$C_L = 200\text{pF}$

4. AC Characteristics

(1) System clock

Parameter	Symbol	Limits			Unit
		Min.	**Typ.**	**Max.**	
Clock frequency	t_{CLF}	31.25	—	83.26	ns
Clock pulse duration (Low)	t_{CLCL}	10.0	—	—	
Clock pulse duration (High)	t_{CLCH}	10.0	—	—	
Clock pulse rise time	t_{CR}	—	—	10.0	
Clock pulse fall time	t_{CF}	—	—	10.0	

Clock signal
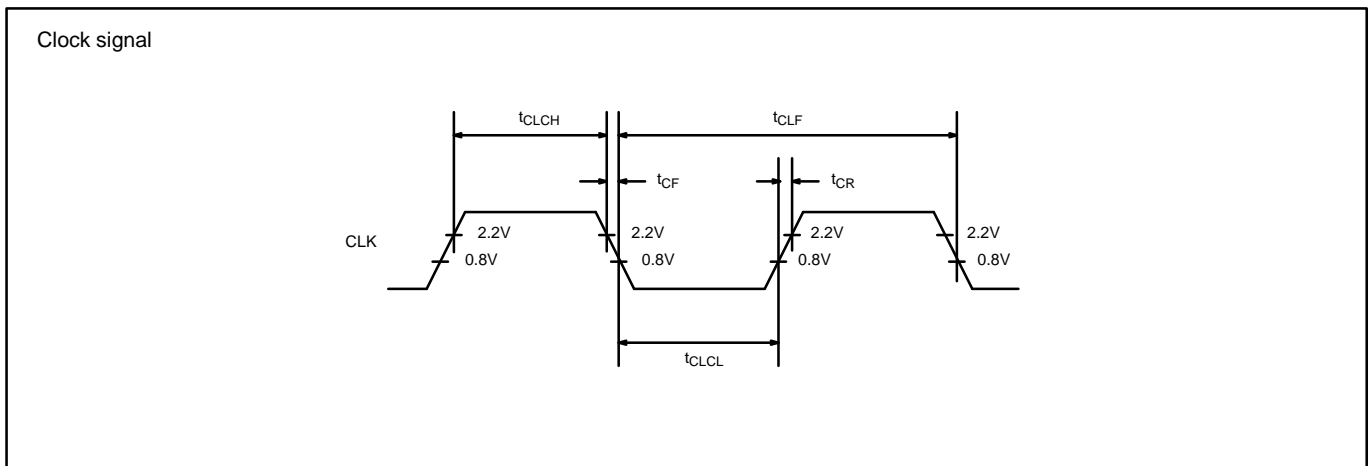
(2) System reset

Parameter	Symbol	Limits			Unit
		Min.	**Typ.**	**Max.**	
Reset ($\overline{RESET}$) pulse duration at Low	t_{WRSL}	$4t_{CLF}$	—	—	ns

Reset signal

16
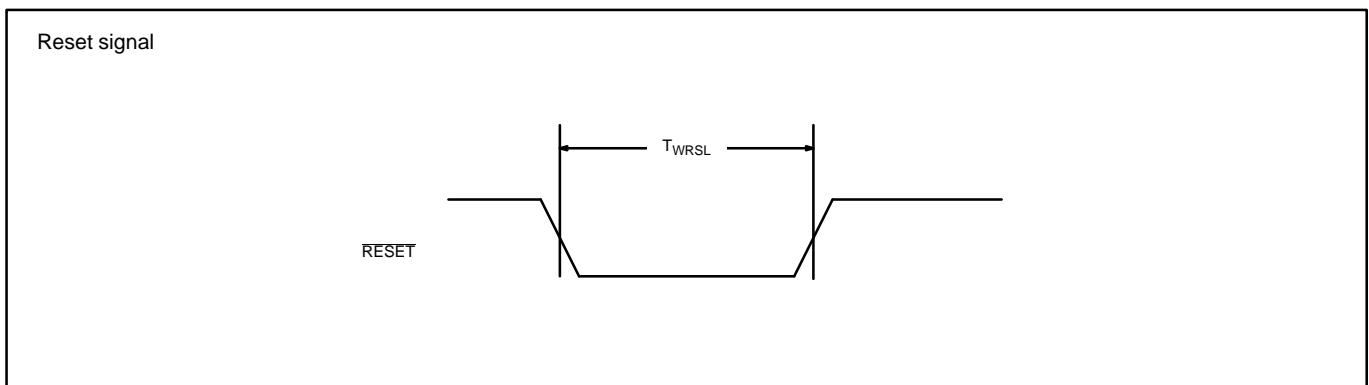
(3) MPU Interface (80 Series)

● Register write timing

Parameter	Symbol	Limits		Unit
		Min.	Max.	
Address (A4 to A0), $\overline{BHE}$ setup time	t_{AWS}	40	—	ns
Address (A4 to A0) hold time	t_{AWH}	20	—	
$\overline{CS0}$ setup time	t_{CWS}	20	—	
$\overline{CS0}$ hold time	t_{CWH}	10	—	
Data setup time	t_{DWS}	40	—	
Data hold time	t_{DWH}	20	—	
$\overline{WR}$ pulse duration at Low	t_{WR}	70	—	

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● Register read timing

Parameter	Symbol	Limits		Unit
		Min.	Max.	
Address (A4 to A0), $\overline{BHE}$ setup time	t_{ARS}	40	—	ns
Address (A4 to A0) hold time	t_{ARH}	20	—	
$\overline{CS0}$ setup time	t_{CRS}	20	—	
$\overline{CS0}$ hold time	t_{CRH}	10	—	
$\overline{RD}$ set Low → data output defined time	t_{RLD}	—	70	
$\overline{RD}$ set High → data output disable time	t_{RHD}	5	—	
$\overline{RD}$ pulse duration at Low	t_{RD}	70	—	
INT signal clear time	t_{DL}	—	50	
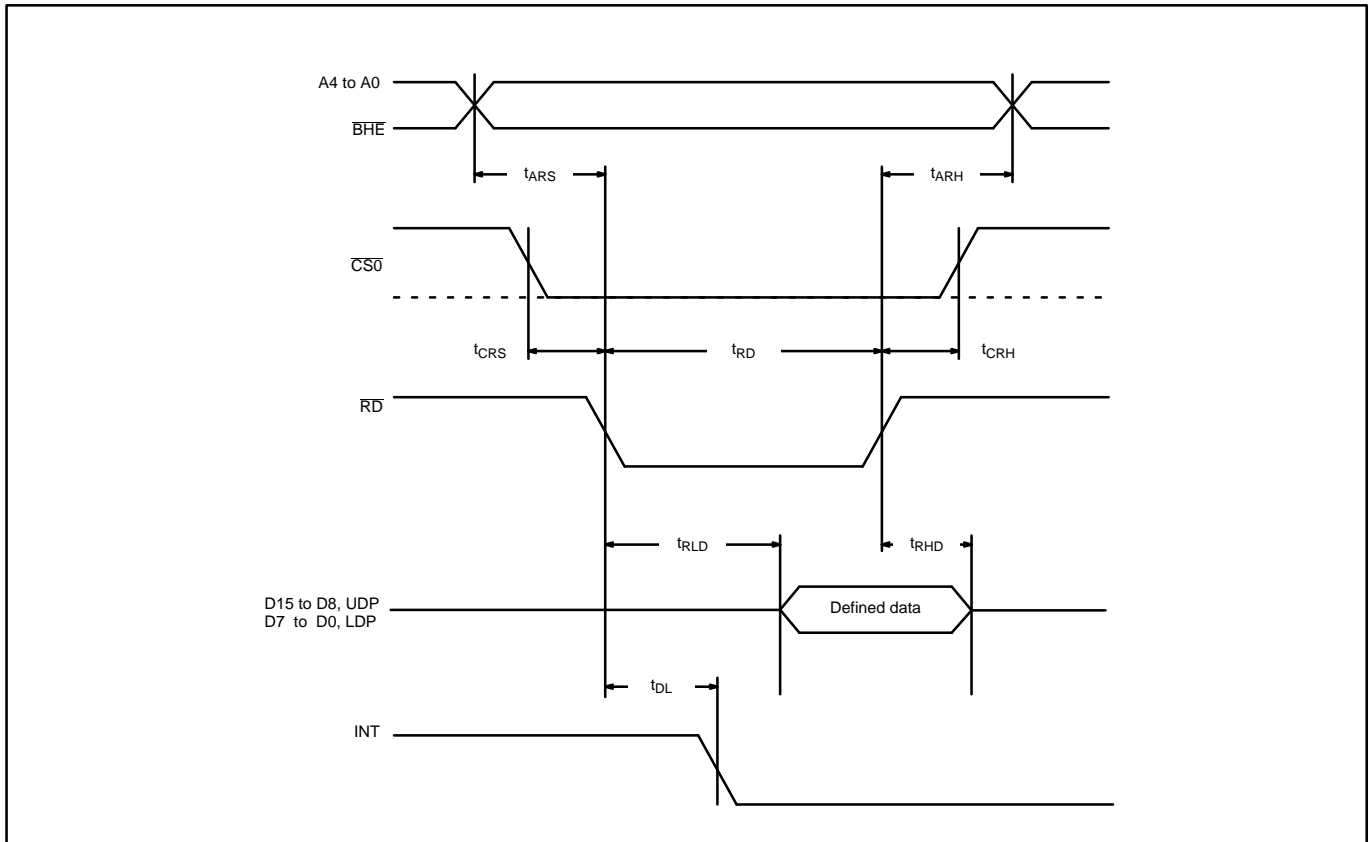
● Register write timing (for external access)

Parameter	Symbol	Limits		Unit
		Min.	Max.	
Address (A0), $\overline{\text{BHE}}$ setup time	t_{AWSE}	40	—	ns
Address (A0), $\overline{\text{BHE}}$ hold time	t_{AWHE}	20	—	
$\overline{\text{CS1}}$ setup time	t_{CWSE}	20	—	
$\overline{\text{CS1}}$ hold time	t_{CWHE}	10	—	
$\overline{\text{WR}}$ set Low → DMA bus output delay time	t_{WLHD}	—	70	
$\overline{\text{WR}}$ set High → DMA bus output undefined time	t_{WHHD}	5	—	
MPU data bus → DMA bus output delay time	t_{DHD}	—	40	
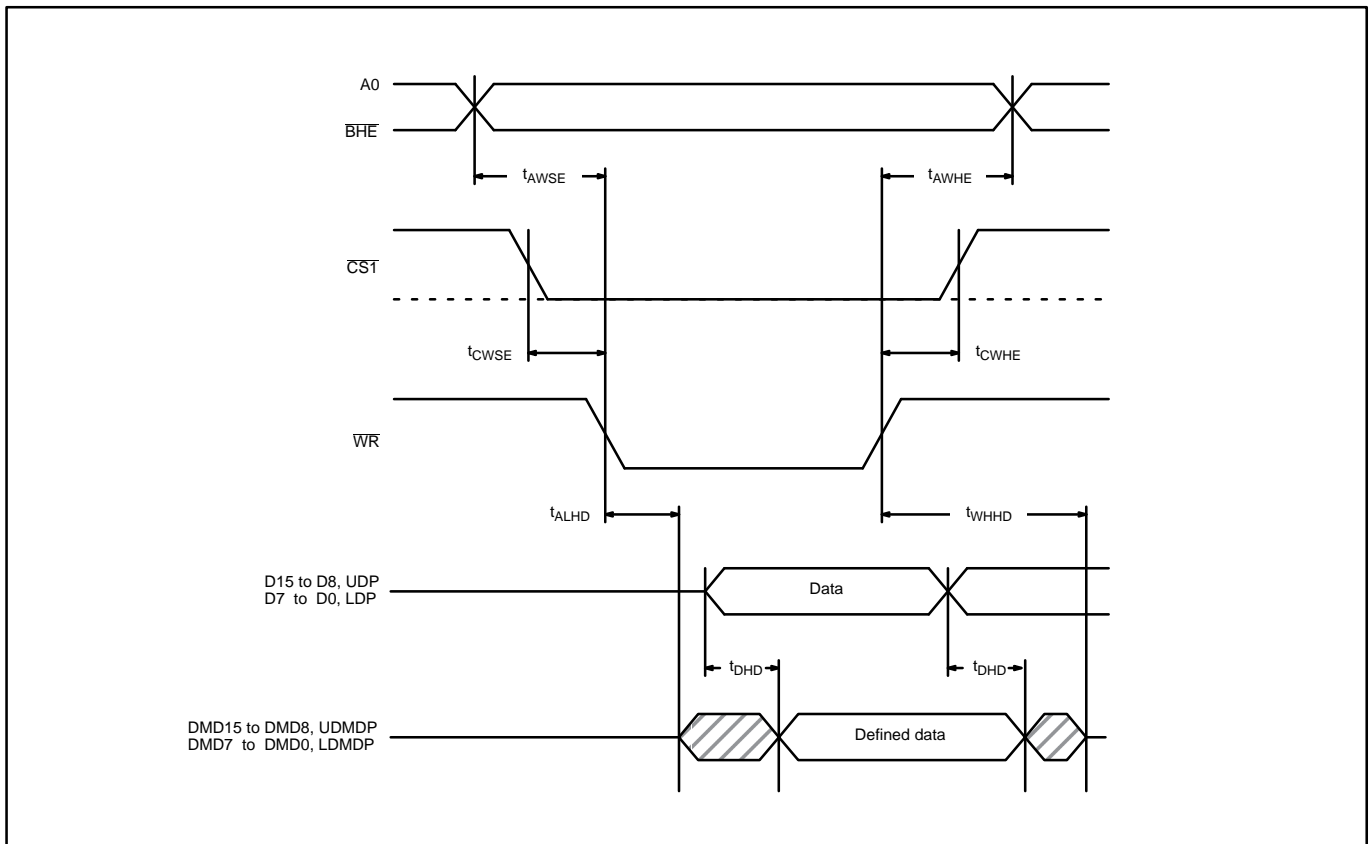
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● Register read timing (for external access)

Parameter	Symbol	Limits		Unit
		Min.	Max.	
Address (A0), $\overline{BHE}$ setup time	t_{ARSE}	40	—	ns
Address (A0), $\overline{BHE}$ hold time	t_{ARHE}	20	—	
$\overline{CS1}$ setup time	t_{CRSE}	20	—	
$\overline{CS1}$ hold time	t_{CRHE}	10	—	
$\overline{RD}$ set Low → MPU data bus output enable time	t_{RLNZ}	—	70	
$\overline{RD}$ set High → MPU data bus output disable time	t_{RHHZ}	5	—	
DMA bus → MPU data bus output delay time	t_{HDD}	—	40	
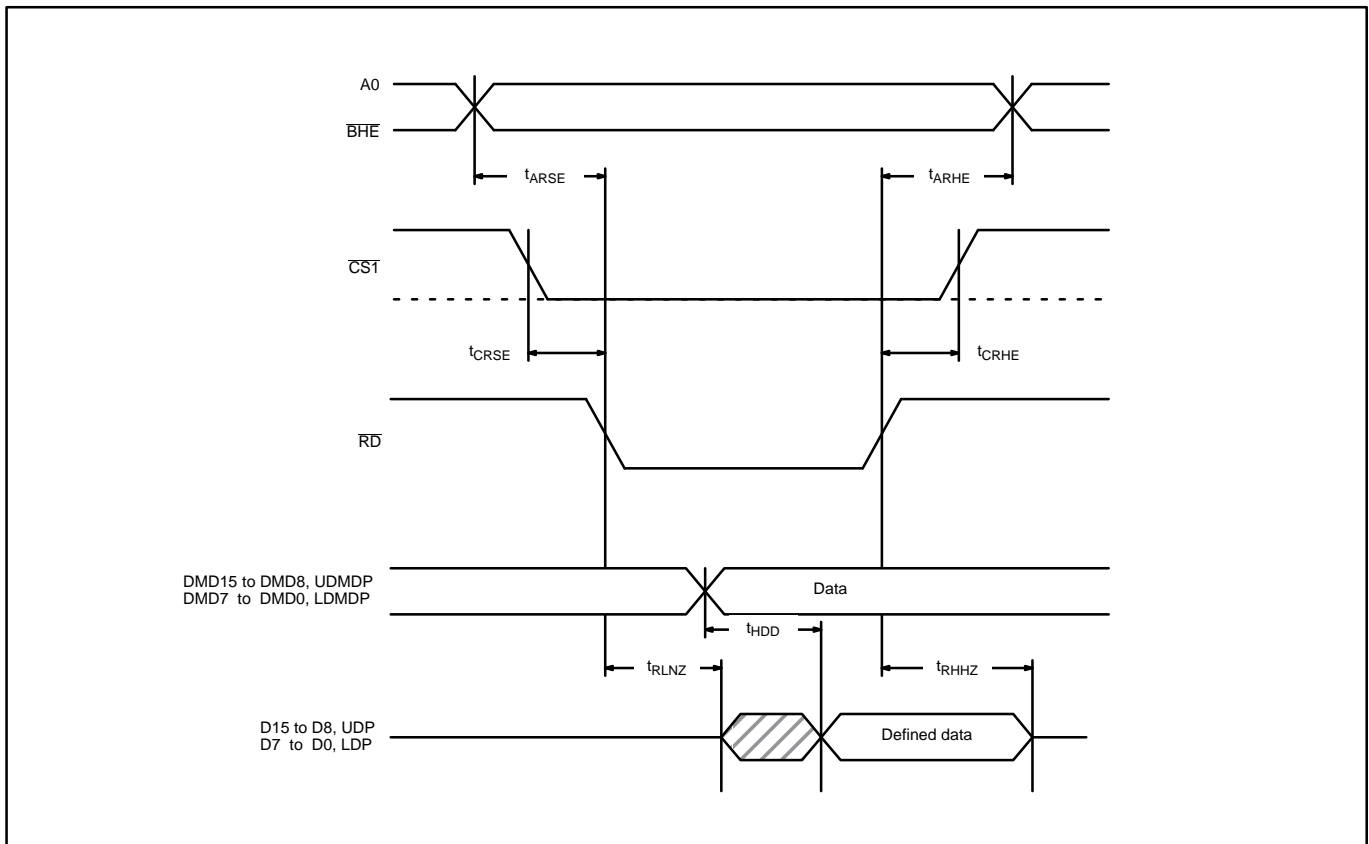
(4) MPU Interface (68 Series)

• Register write timing

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
Address (A4 to A0) setup time	t_{AWS}	40	—	ns
Address (A4 to A0) hold time	t_{AWH}	20	—	
$\overline{CS0}$ setup time	t_{CWS}	20	—	
$\overline{CS0}$ hold time	t_{CWH}	10	—	
Data setup time	t_{DWS}	40	—	
Data hold time	t_{DWH}	20	—	
$\overline{UDS}/\overline{LDS}$ pulse duration at Low	t_{DS}	70	—	
R/$\overline{W}$ setup time	t_{RWS}	20	—	
R/$\overline{W}$ hold time	t_{RWH}	20	—	
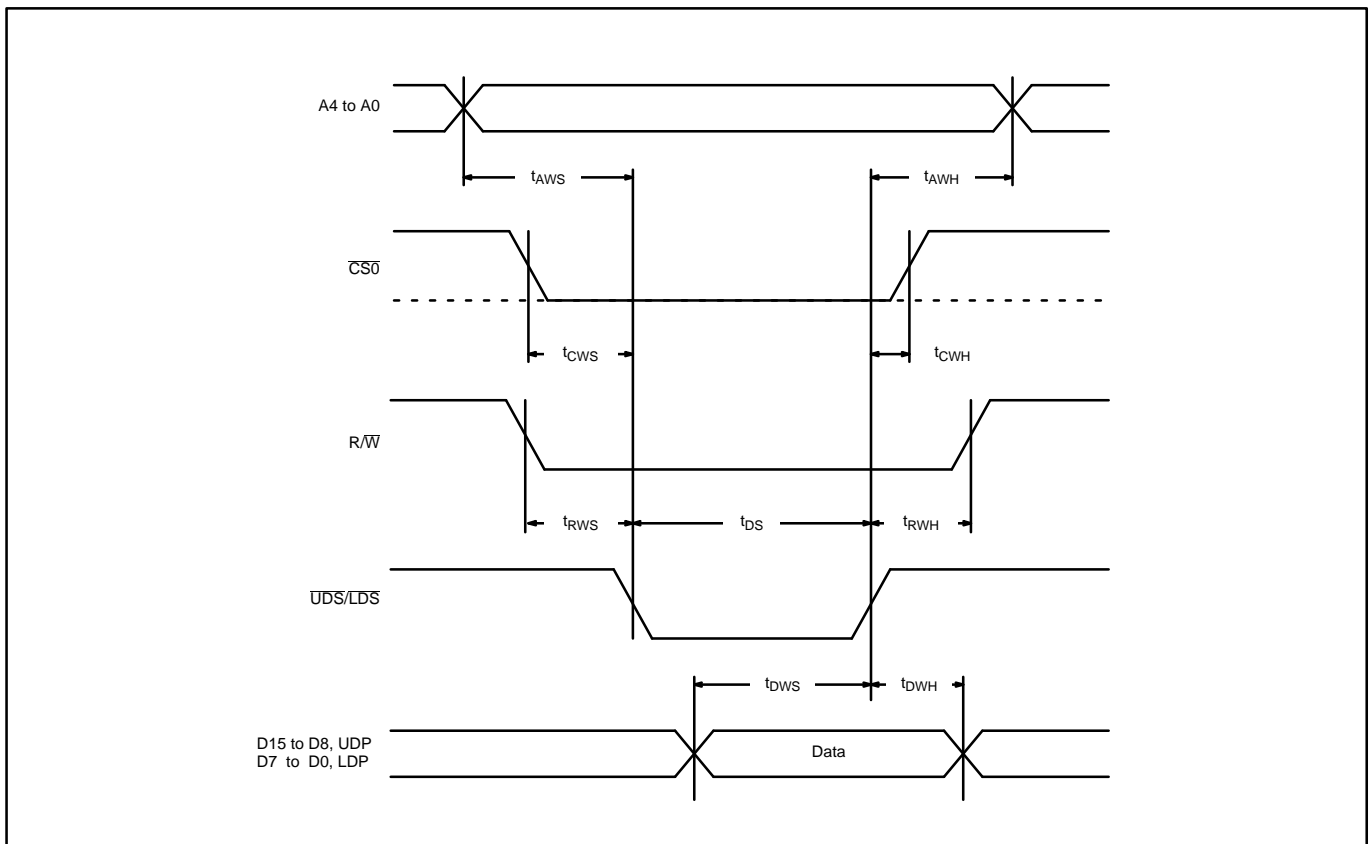
● Register read timing

Parameter	Symbol	Limits		Unit
		Min.	Max.	
Address (A4 to A0) setup time	t_{ARS}	40	—	ns
Address (A4 to A0) hold time	t_{ARH}	20	—	
CS0 setup time	t_{CRS}	20	—	
CS0 hold time	t_{CRH}	10	—	
Data output defined time	t_{RLD}	—	70	
Data output disable time	t_{RHD}	5	—	
UDS/LDS pulse duration at Low	t_{DS}	70	—	
R/W setup time	t_{RWS}	20	—	
R/W hold time	t_{RWH}	20	—	
INT signal clear time	t_{DH}	—	50	
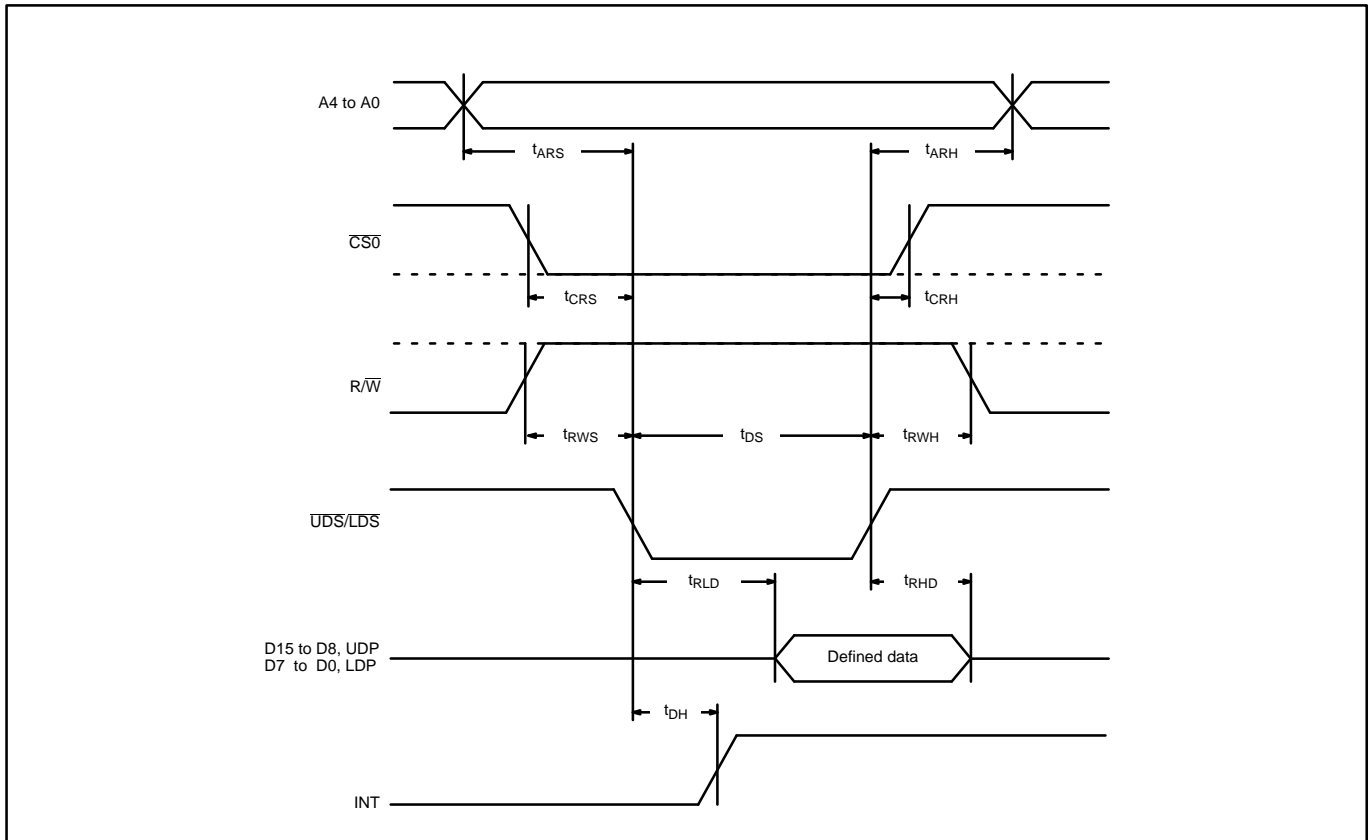
● Register write timing (for external access)

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
Address (A0) setup time	t_{AWSE}	40	—	ns
Address (A0) hold time	t_{AWHE}	20	—	
$\overline{CS1}$ setup time	t_{CWSE}	20	—	
$\overline{CS1}$ hold time	t_{CWHE}	10	—	
$\overline{UDS}/\overline{LDS}$ set Low → DMA bus output delay time	t_{WLHD}	—	70	
$\overline{UDS}/\overline{LDS}$ set High → DMA bus output undefined time	t_{WHHD}	5	—	
MPU data bus → DMA bus output delay time	t_{DHD}	—	40	
R/$\overline{W}$ setup time	t_{RWS}	20	—	
R/$\overline{W}$ hold time	t_{RWH}	20	—	
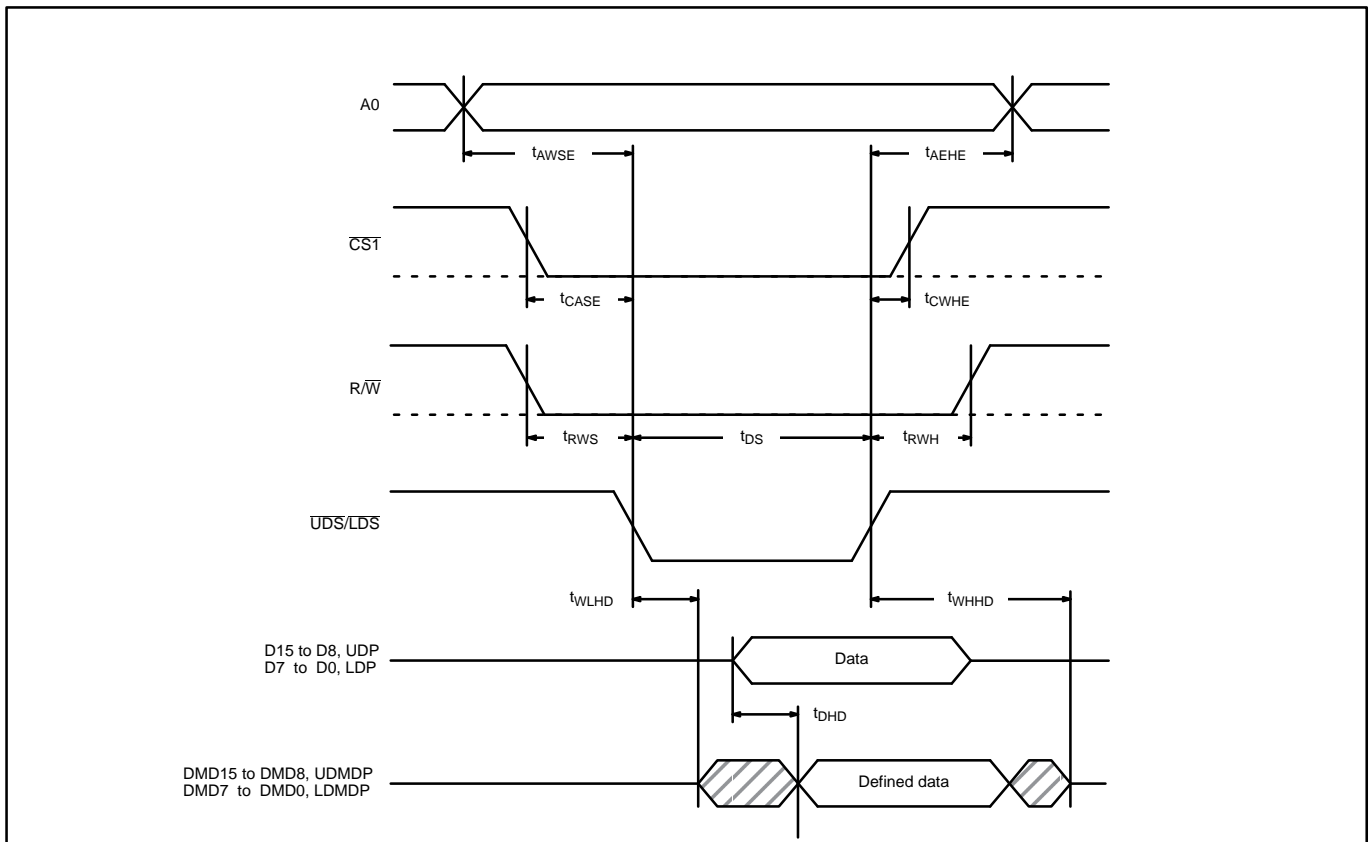
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• Register read timing (for external access)

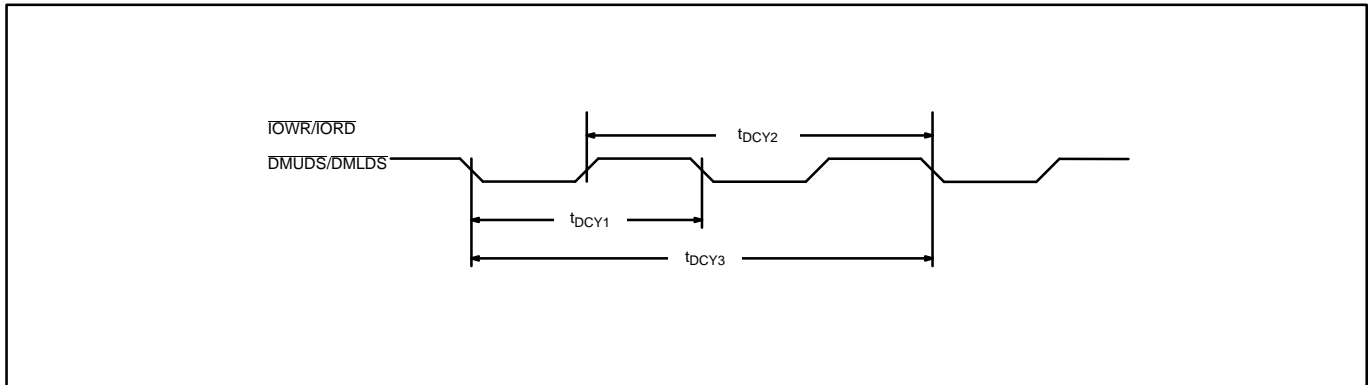| Parameter	Symbol	Limits		Unit
		Min.	Max.	
Address (A0) setup time	t_{ARSE}	40	—	
Address (A0) hold time	t_{ARHE}	20	—	
$\overline{CS1}$ setup time	t_{CRSE}	20	—	
$\overline{CS1}$ hold time	t_{CRHE}	10	—	
$\overline{UDS}/\overline{LDS}$ set Low → MPU data bus output enable time	t_{RLNZ}	—	70	ns
$\overline{UDS}/\overline{LDS}$ set High → MPU data bus output disable time	t_{RHHZ}	5	—	
DMA bus → MPU data bus output delay time	t_{HDD}	—	40	
R/$\overline{W}$ setup time	t_{RWS}	20	—	
R/$\overline{W}$ hold time	t_{RWH}	20	—	
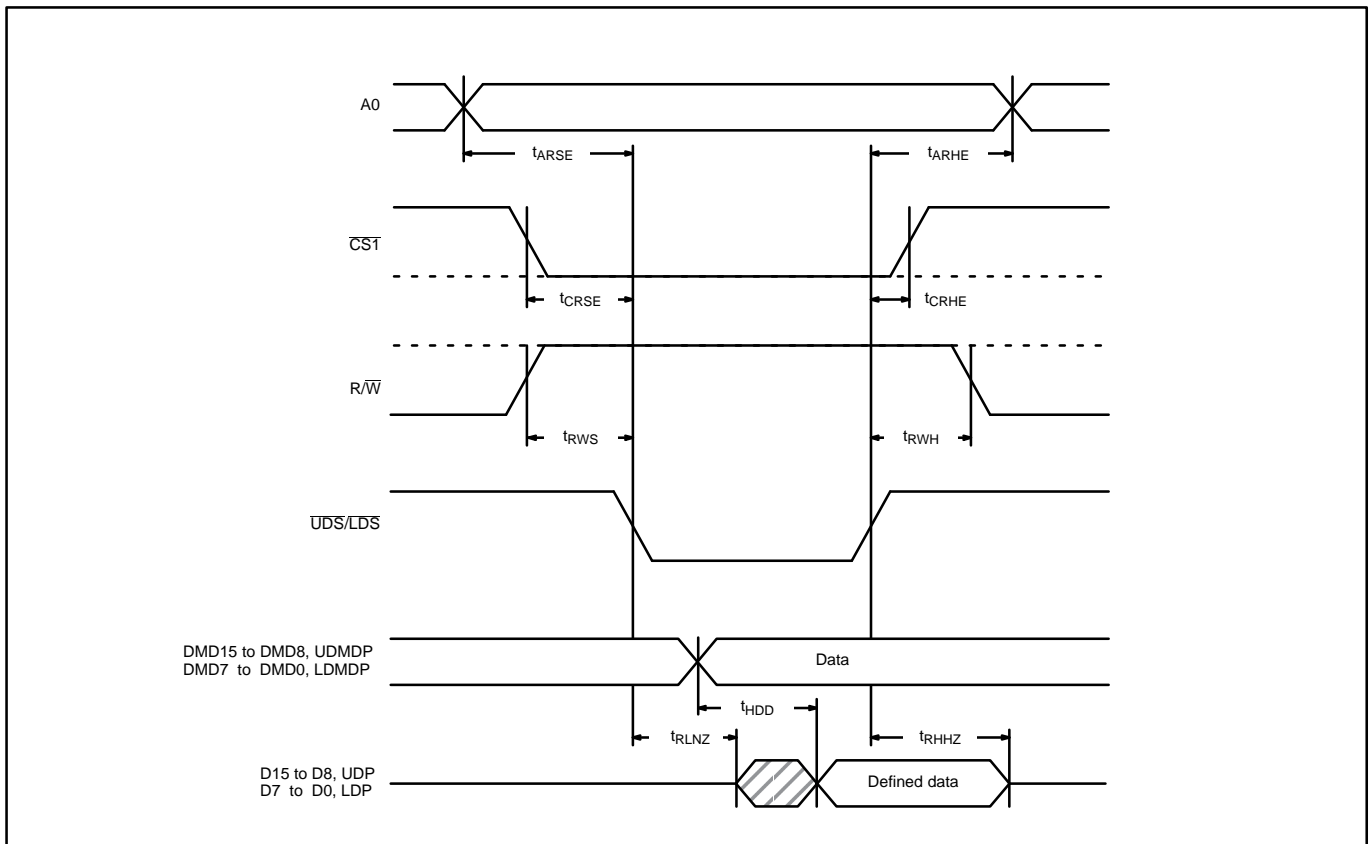
(5) DMA Interface

DMA access timing

The time regulations are not applicable in the following cases:

- During SCSI input and when data buffer EMPTY, or when one byte held
- During SCSI output and when data buffer FULL, or when 63 bytes held
- When parity error detected (target)
- When error stopping transfer occurs in SCSI interface

[Burst mode (for 80 series and 68 series)]

- Access cycle time

Parameter	Symbol	Limits		Unit
		Min.	Max.	
Access cycle time 1	t_{DCY1}	$2t_{CLF}$	—	ns
Access cycle time 2	t_{DCY2}	$3t_{CLF}$	—	
Access cycle time 3	t_{DCY3}	$4t_{CLF}$	—	

[Burst mode for 80 series]

● Write timing

Parameter	Symbol	Limits		Unit
		Min.	Max.	
DREQ set High → $\overline{\text{DACK}}$ set Low	t_{DHAL}	0	—	ns
$\overline{\text{IOWR}}$ set Low → DREQ set Low	t_{ALDL}	—	35	
DREQ set Low → DREQ set High	t_{DLDH}	0	—	
$\overline{\text{DACK}}$ set Low → $\overline{\text{IOWR}}$ set Low	t_{ALWL}	0	—	
$\overline{\text{DMBHE}}$, DMA0 setup time	t_{DAWS}	20	—	
$\overline{\text{IOWR}}$ pulse duration at Low	t_{DWR}	40	—	
$\overline{\text{IOWR}}$ set High → $\overline{\text{DACK}}$ set High	t_{WHAH}	0	—	
$\overline{\text{DMBHE}}$, DMA0 hold time	t_{DAWH}	20	—	
Input data setup time	t_{DDWS}	30	—	
Input data hold time	t_{DDWH}	10	—	
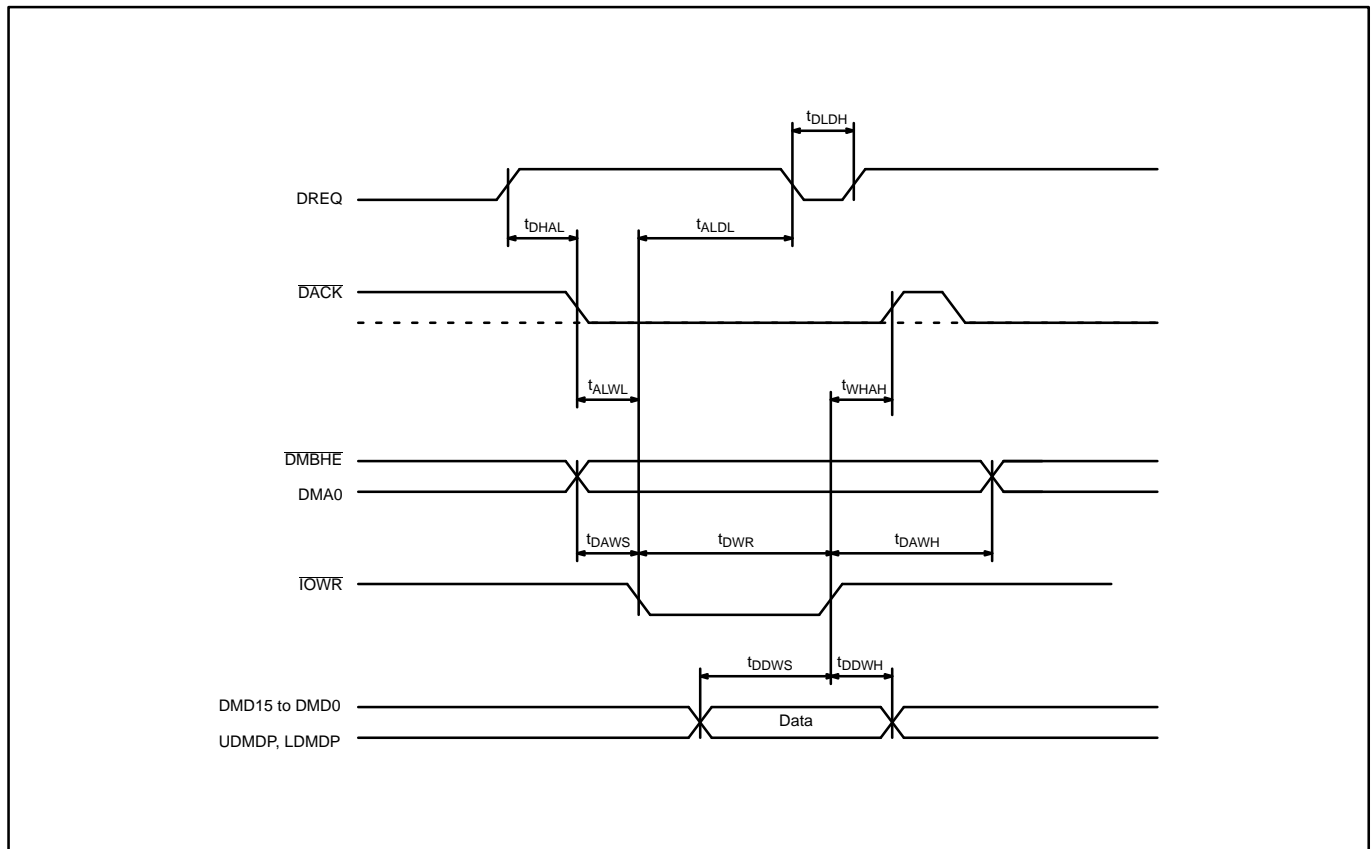
● Read timing

Parameter	Symbol	Limits		Unit
		Min.	Max.	
DREQ set High → $\overline{\text{DACK}}$ set Low	t_{DHAL}	0	—	ns
$\overline{\text{IORD}}$ set Low → DREQ set Low	t_{ALDL}	—	35	
DREQ set Low → DREQ set High	t_{DLDH}	0	—	
$\overline{\text{DACK}}$ set Low → $\overline{\text{IORD}}$ set Low	t_{ALRL}	0	—	
$\overline{\text{DMBHE}}$, DMA0 setup time	t_{DARS}	20	—	
$\overline{\text{IODR}}$ pulse duration at Low	t_{DRD}	40	—	
$\overline{\text{IODR}}$ set High → $\overline{\text{DACK}}$ set High	t_{RHAH}	0	—	
$\overline{\text{DMBHE}}$, DMA0 hold time	t_{DARH}	20	—	
Data output defined time	t_{DRLD}	—	40	
Data output hold time	t_{DRHD}	5	—	
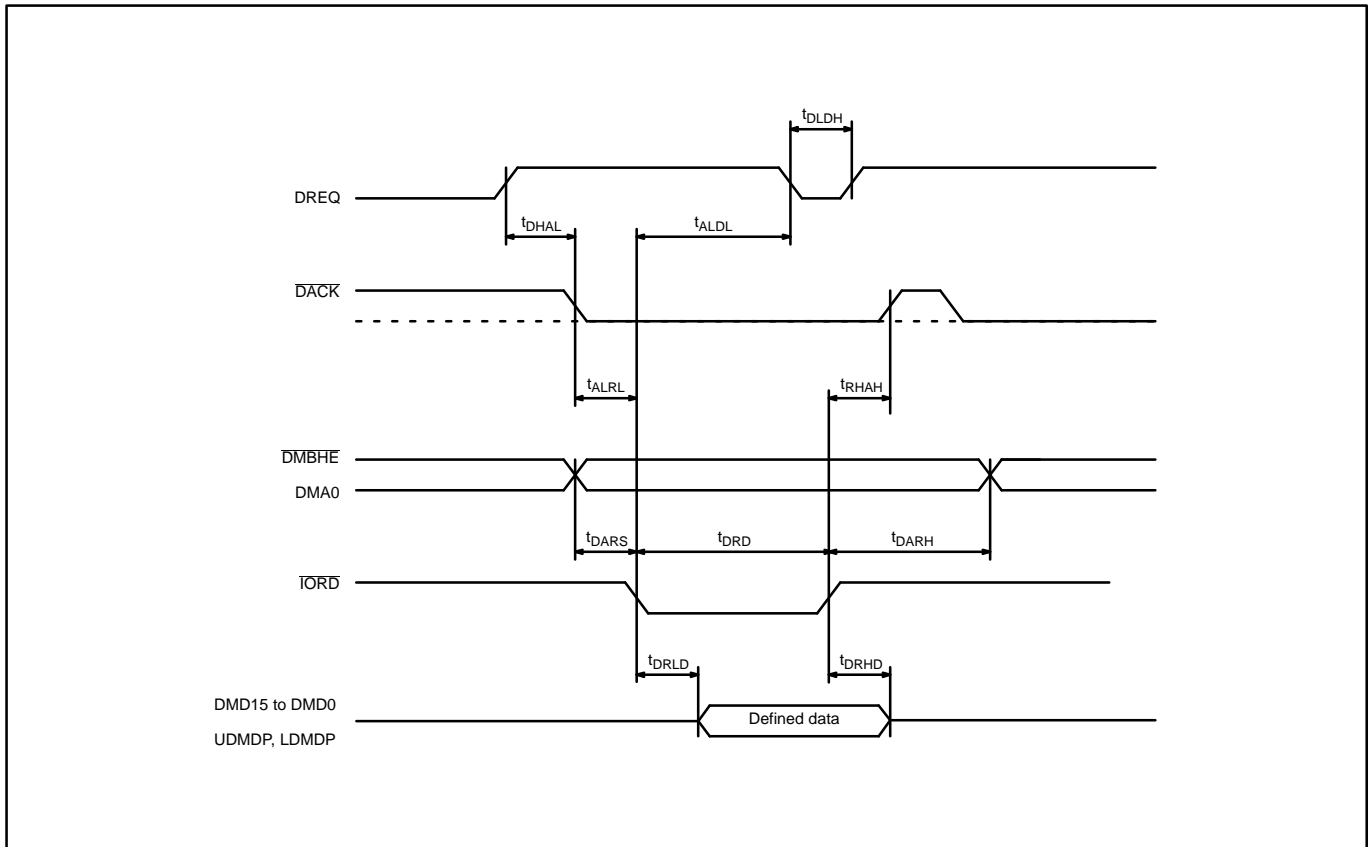
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[Burst mode for 68 series]

• Write timing

Parameter	Symbol	Limits		Unit
		Min.	Max.	
DREQ set High → $\overline{\text{DACK}}$ set Low	t_{DHAL}	0	—	ns
$\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low → DREQ set Low	t_{ALDL}	—	35	
DREQ set Low → DREQ set High	t_{DLDH}	0	—	
$\overline{\text{DACK}}$ set Low → $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low	t_{ALDL}	10	—	
DMR/$\overline{\text{W}}$ setup time	t_{DRWS}	20	—	
$\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ pulse duration at Low	t_{DDS}	40	—	
$\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set High → $\overline{\text{DACK}}$ set High	t_{DHAH}	0	—	
DMR/$\overline{\text{W}}$ hold time	t_{DRWH}	20	—	
Input data setup time	t_{DDWS}	30	—	
Input data hold time	t_{DDWH}	10	—	

● Read timing

Parameter	Symbol	Limits		Unit
		Min.	Max.	
DREQ set High → $\overline{\text{DACK}}$ set Low	t_{DHAL}	0	—	ns
$\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low → DREQ set Low	t_{ALDL}	—	35	
DREQ set Low → DREQ set High	t_{DLDH}	0	—	
$\overline{\text{DACK}}$ set Low → $\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set Low	t_{ALDL}	10	—	
DMR/$\overline{\text{W}}$ setup time	t_{DRWS}	20	—	
$\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ pulse duration at High	t_{DDS}	40	—	
$\overline{\text{DMUDS}}/\overline{\text{DMLDS}}$ set High → $\overline{\text{DACK}}$ set High	t_{DHAH}	0	—	
DMR/$\overline{\text{W}}$ hold time	t_{DRWH}	20	—	
Output data defined time	t_{DRLD}	—	40	
Output data hold time	t_{DRHD}	5	—	

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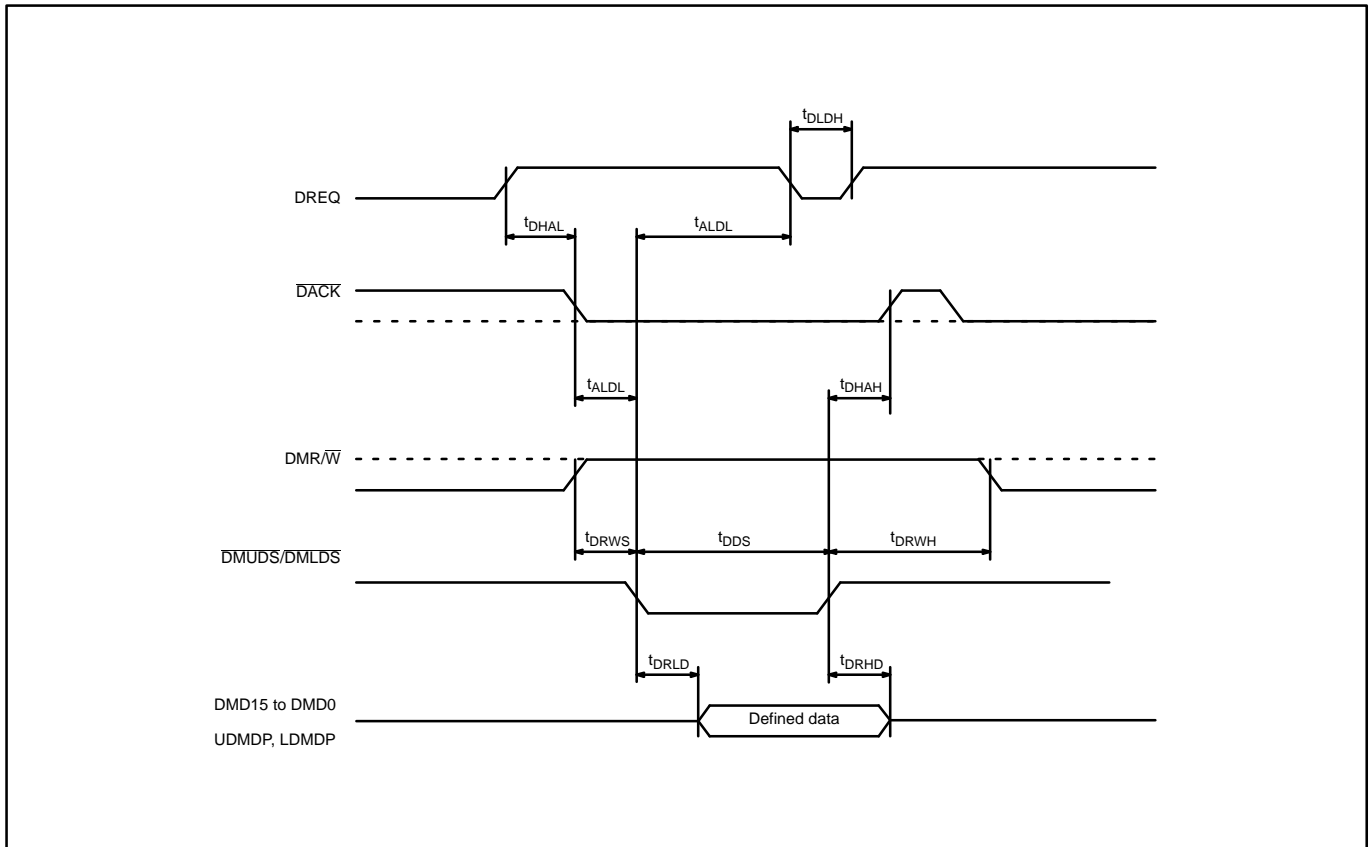
(6) SCSI Interface (Initiator)

[Asynchronous transfer mode]

● Input timing (target → initiator)

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
$\overline{ACK}$ set Low → $\overline{REQ}$ set High	t_{AOLR}	0	—	ns
$\overline{REQ}$ set High → $\overline{ACK}$ set High	t_{RAOH}	—	60	
$\overline{ACK}$ set High → $\overline{REQ}$ set Low	t_{AOHR}	10	—	
Data bus defined → $\overline{REQ}$ set Low	t_{DTSU}	10	—	
$\overline{REQ}$ set Low → data bus hold time	t_{DHLD}	20	—	
$\overline{REQ}$ set Low → $\overline{ACK}$ set Low	t_{RAOL}	—	40	
$\overline{REQ}$ set High → $\overline{ACK}$ set Low*	t_{RACY}	—	$3t_{CLF} + 40$	

*The time (t_{RACY}) of $\overline{REQ}$ set High → $\overline{ACK}$ set Low is set to the longer time compared to ($t_{RAOH} + t_{AOHR} + t_{RAOL}$).

Note: The input timing regulations are not applicable in the following cases.
- When data register FULL in data phase
- When last byte transferred

● Output timing (initiator → target)

Parameter	Symbol	Limits		Unit
		Min.	Max.	
$\overline{ACK}$ set Low → $\overline{REQ}$ set High	t_{AOLR}	0	—	ns
$\overline{REQ}$ set High → $\overline{ACK}$ set High	t_{RAOH}	—	60	
$\overline{ACK}$ set High → $\overline{REQ}$ set Low	t_{AOHR}	10	—	
Data bus output defined → $\overline{ACK}$ set Low*	t_{DVLD}	$S \bullet t_{CLF}$ - 10	—	
$\overline{REQ}$ set High → data bus hold time	t_{DIVD}	$2t_{CLF}$	—	
$\overline{REQ}$ set Low → $\overline{ACK}$ set Low	t_{RAOL}	—	40	

*The value of S varies with the setting condition of the asynchronous setup time register (address 23).

Note: The output timing regulations are not applicable when the data register is EMPTY in the data phase.
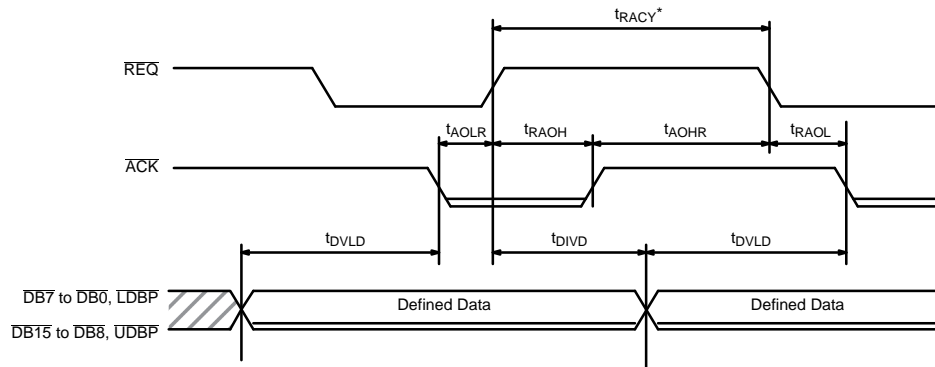
*The time (t_{RACY}) of $\overline{REQ}$ set High → $\overline{ACK}$ set Low is set to the longer time of either (t_{RAOH} + t_{AOHR} + t_{RAOL}) or (t_{DIVD} + t_{DVLD}).

[Synchronous transfer mode]

● REQ/ACK signal synchronization

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
$\overline{\text{ACK}}$ Assertion Period*	t_{AKAP}	$A \bullet t_{CLF} - 3$	—	ns
$\overline{\text{ACK}}$ Negation Period*	t_{ANAP}	$N \bullet t_{CLF} - 3$	—	
$\overline{\text{REQ}}$ Assertion Period	t_{RQAP}	20	—	
$\overline{\text{REQ}}$ Negation Period	t_{RNAP}	20	—	
$\overline{\text{REQ}}$ input cycle time (1)	t_{RQF1}	$1t_{CLF}$	—	
$\overline{\text{REQ}}$ input cycle time (2)	t_{RQF2}	$3t_{CLF}$	—	

*The values of A and N vary with the setting condition of the transfer period register (address 13).
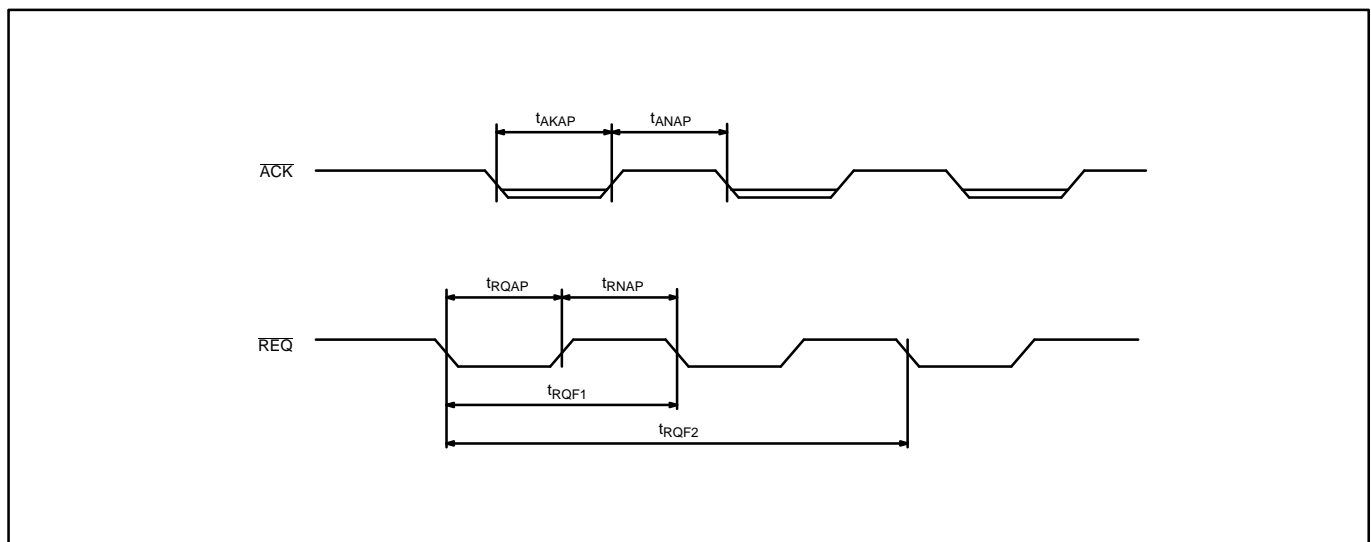
● Input timing (target → initiator)

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
Data bus defined → $\overline{REQ}$ set Low	t_{DTSU}	10	—	ns
$\overline{REQ}$ set Low → data bus hold time	t_{DHLD}	20	—	
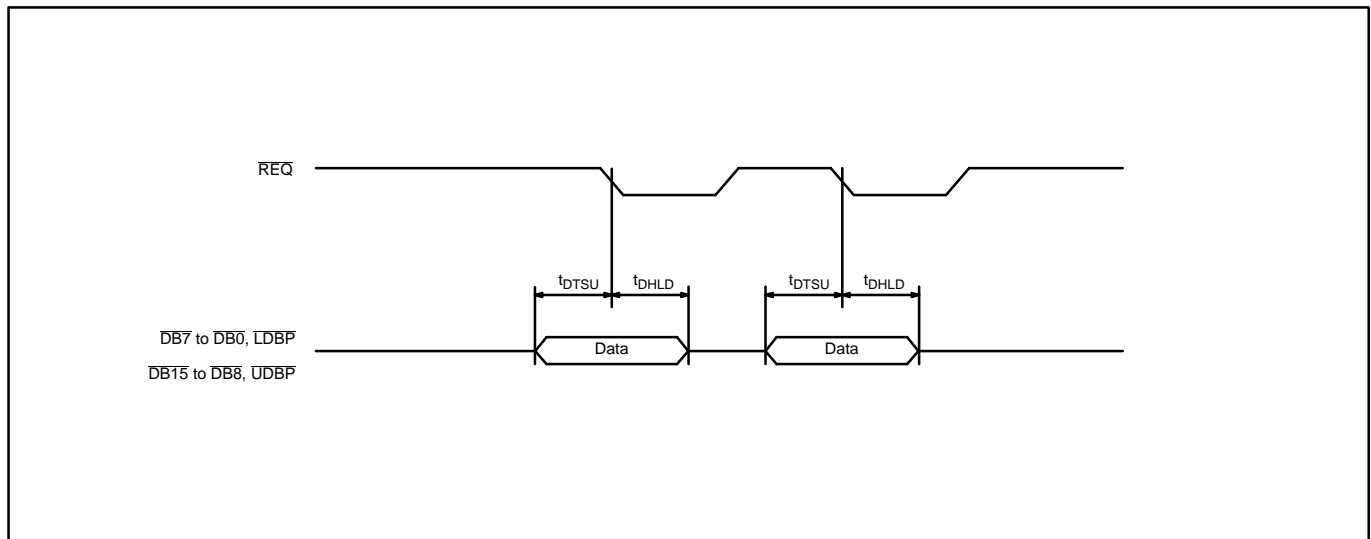
● Output timing (initiator → target)

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
Data bus defined → $\overline{ACK}$ set Low*	t_{DVAK}	$N \bullet t_{CLF} - 5$	—	ns
$\overline{ACK}$ set Low → data bus hold time*	t_{AKDH}	$A \bullet t_{CLF} - 5$	—	

*The values of A and N vary with the setting condition of the transfer period register (address 13).
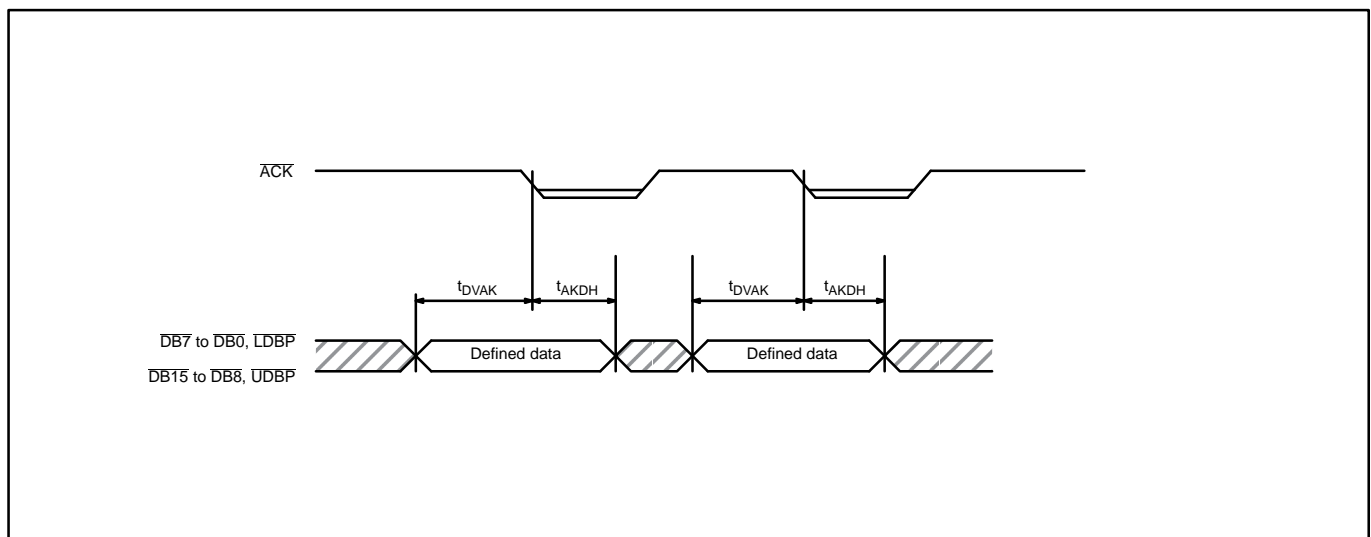
(7) SCSI Interface (Target)

[Asynchronous transfer mode]

● Input timing (initiator → target)

Parameter	Symbol	Limits		Unit
		Min.	Max.	
$\overline{REQ}$ set Low → $\overline{ACK}$ set Low	t_{RDLA}	0	—	ns
$\overline{ACK}$ set Low → $\overline{REQ}$ set High	t_{AKOH}	—	60	
$\overline{REQ}$ set High → $\overline{ACK}$ set Low	t_{ROHA}	0	—	
Data bus defined → $\overline{ACK}$ set Low	t_{VTSU}	10	—	
$\overline{ACK}$ set Low → data bus hold time	t_{DHLD}	20	—	
$\overline{ACK}$ set High → $\overline{REQ}$ set Low	t_{AROL}	—	40	
$\overline{ACK}$ set Low → $\overline{REQ}$ set Low*	t_{RACY}	—	$3t_{CLF} + 40$	

*The time (t_{RACY}) of $\overline{ACK}$ set Low → $\overline{REQ}$ set Low is set to the longer time compared with ($t_{AROH} + t_{ROHA} + t_{AROL}$).

Note: The input timing regulations are not applicable when the data register is FULL in the data phase.
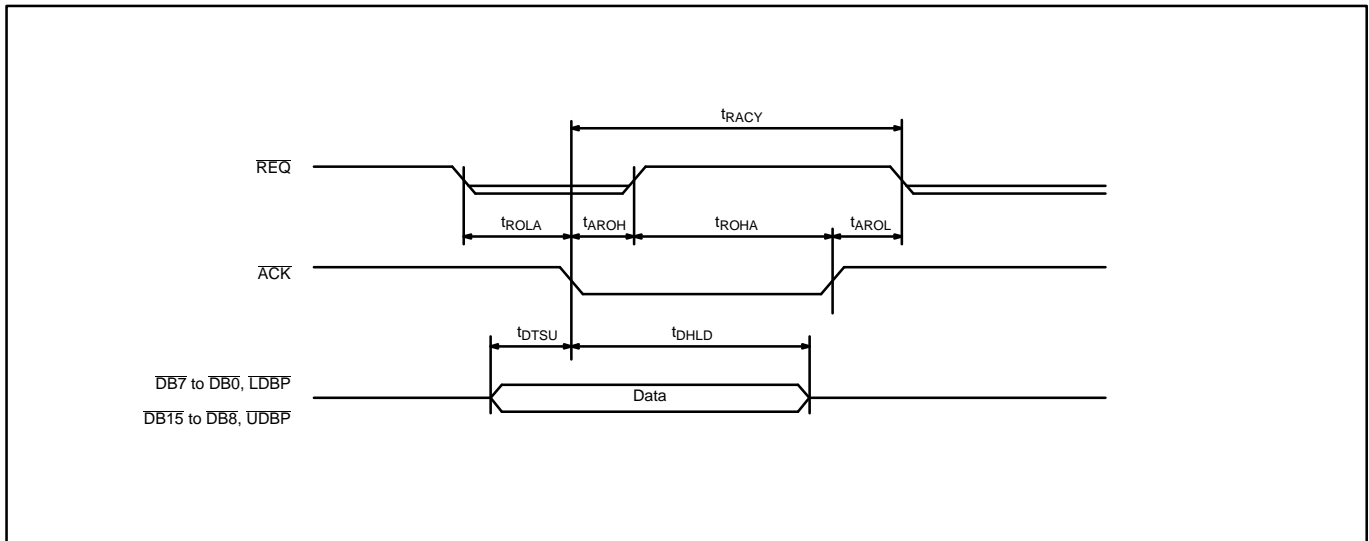
● Output timing (target → initiator)

Parameter	Symbol	Limits		Unit
		Min.	Max.	
$\overline{REQ}$ set Low → $\overline{ACK}$ set Low	t_{ROLA}	0	—	ns
$\overline{ACK}$ set Low → $\overline{REQ}$ set High	t_{AROH}	—	60	
$\overline{REQ}$ set High → $\overline{ACK}$ set High	t_{ROHA}	0	—	
Data bus output defined → $\overline{REQ}$ set Low*	t_{DVLD}	$S{\bullet}t_{CLF} - 10$	—	
$\overline{ACK}$ set Low → data bus hold time	t_{DIVD}	$2t_{CLF}$	—	
$\overline{ACK}$ set High → $\overline{REQ}$ set Low	t_{AROL}	—	40	

*The value of S varies with the setting condition of the asynchronous setup time register (address 23).

Note: The output timing regulations are not applicable when the data register is EMPTY in the data phase.

*The time (t_{RACY}) of $\overline{ACK}$ set Low → $\overline{REQ}$ set Low is set to the longer time of either ($t_{AROH} + t_{ROHA} + t_{AROL}$) or ($t_{DIVD} + t_{DVLD}$).
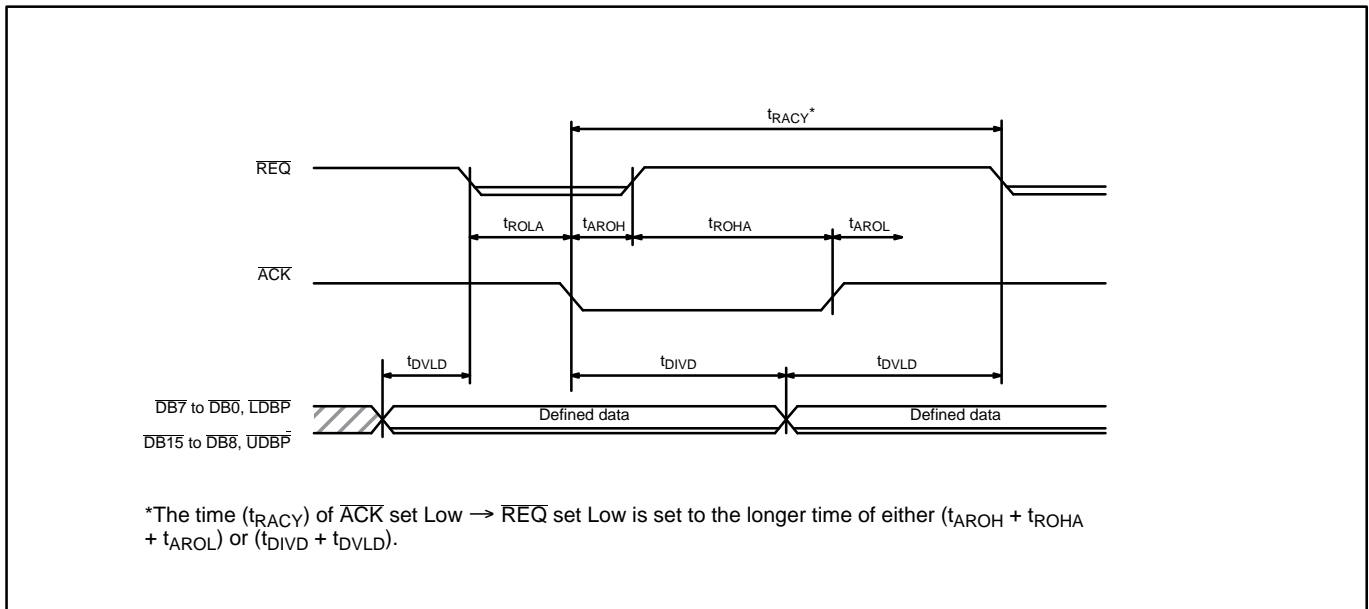
[Synchronous transfer mode]

● REQ/ACK signal synchronization

Parameter	Symbol	Limits		Unit
		Min.	Max.	
$\overline{REQ}$ Assertion Period*	t_{RQAP}	$A \bullet t_{CLF} - 3$	—	ns
$\overline{REQ}$ Negation Period*	t_{RNAP}	$N \bullet t_{CLF} - 3$	—	
$\overline{ACK}$ Assertion Period	t_{AKAP}	20	—	
$\overline{ACK}$ Negation Period	t_{ANAP}	20	—	
$\overline{ACK}$ input cycle time (1)	t_{AKF1}	$1t_{CLF}$	—	
$\overline{ACK}$ input cycle time (2)	t_{AKF2}	$3t_{CLF}$	—	

*The values of A and N vary with the setting condition of the transfer period register (address 13).
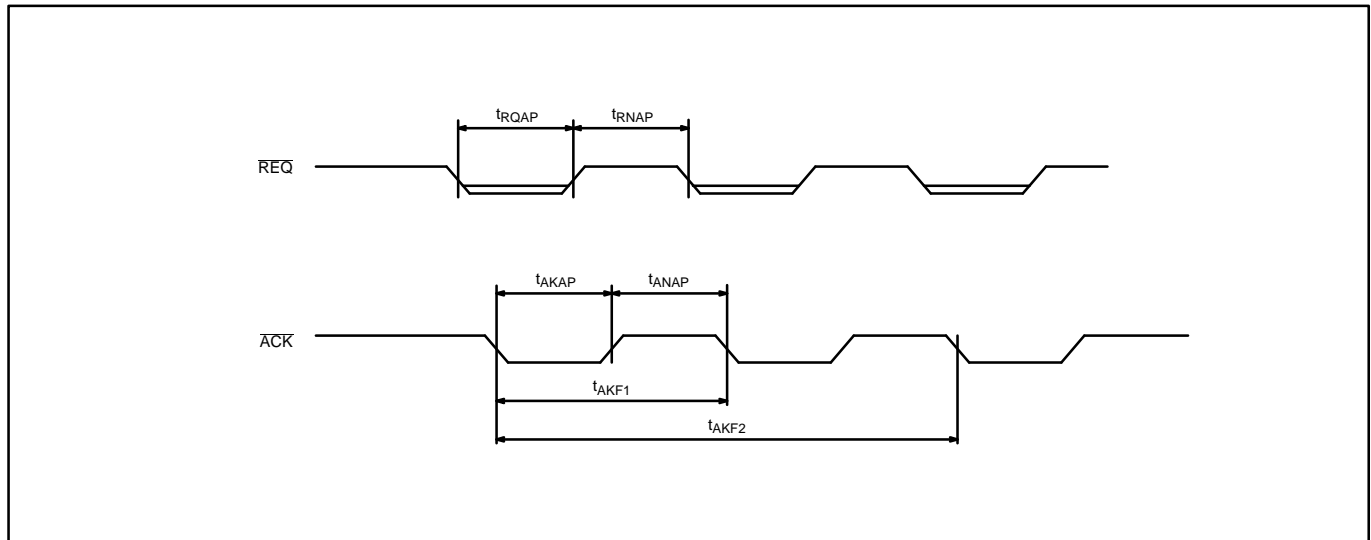
● Input timing (initiator → target)

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
Data bus defined → $\overline{ACK}$ set Low	t_{DTSU}	10	—	ns
$\overline{ACK}$ set Low → data bus hold time	t_{DHLD}	20	—	
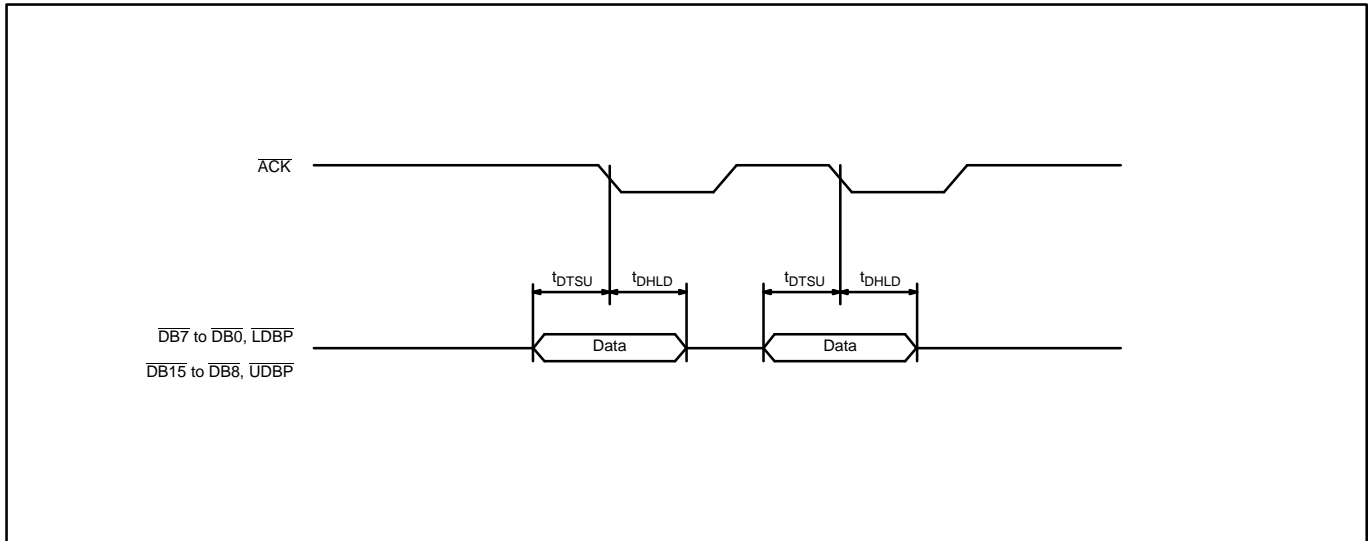
● Output timing (target → initiator)

Parameter	Symbol	Limits		Unit
		Min.	**Max.**	
Data bus defined → $\overline{REQ}$ set Low*	t_{DVRQ}	$N \bullet t_{CLF} - 5$	—	ns
$\overline{REQ}$ set Low → data bus hold time*	t_{RQDH}	$A \bullet t_{CLF} - 5$	—	

*The values of A and N vary with the setting condition of the transfer period register (address 13).
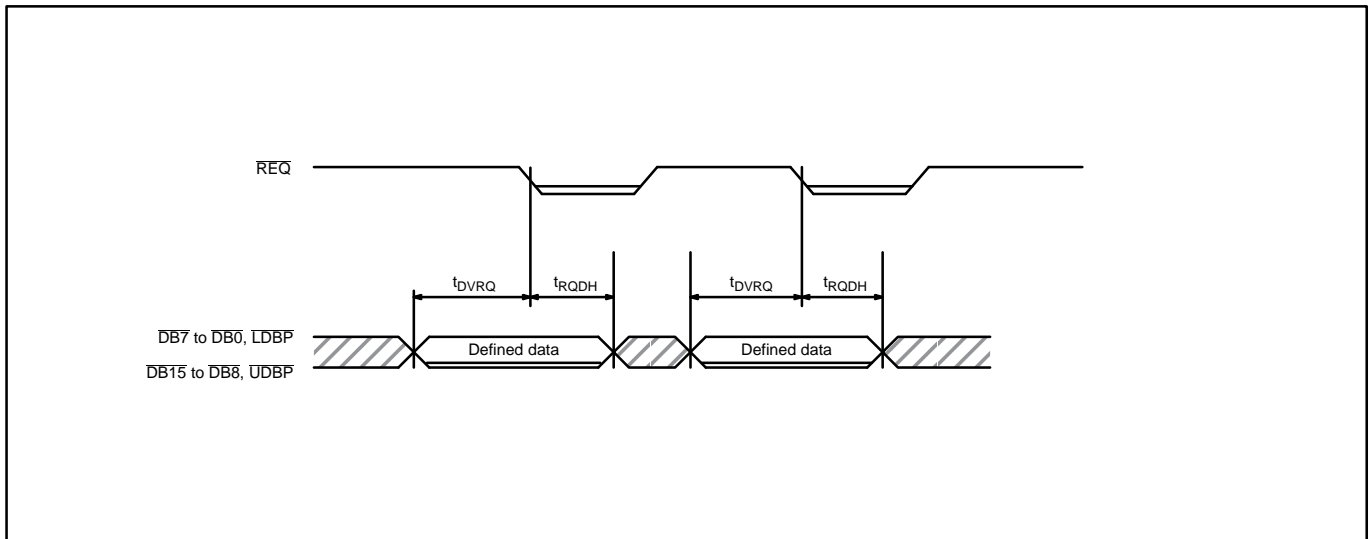
(8) A, N, and S Values in SCSI Interface Timing Specifications

● Set values and A and N values of transfer period register

Transfer period register					A	N	Transfer period register					A	N
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0	0	0	0	1	(Inhibited)	(Inhibited)	1	0	0	0	1	9	8
0	0	0	1	0	1	1	1	0	0	1	0	9	9
0	0	0	1	1	2	1	1	0	0	1	1	10	9
0	0	1	0	0	2	2	1	0	1	0	0	10	10
0	0	1	0	1	3	2	1	0	1	0	1	11	10
0	0	1	1	0	3	3	1	0	1	1	0	11	11
0	0	1	1	1	4	3	1	0	1	1	1	12	11
0	1	0	0	0	4	4	1	1	0	0	0	12	12
0	1	0	0	1	5	4	1	1	0	0	1	13	12
0	1	0	1	0	5	5	1	1	0	1	0	13	13
0	1	0	1	1	6	5	1	1	0	1	1	14	13
0	1	1	0	0	6	6	1	1	1	0	0	14	14
0	1	1	0	1	7	6	1	1	1	0	1	15	14
0	1	1	1	0	7	7	1	1	1	1	0	15	15
0	1	1	1	1	8	7	1	1	1	1	1	16	15
1	0	0	0	0	8	8	0	0	0	0	0	16	16

The A and N values in the register setting represent the assertion and negation periods (in clock-cycle units).

The numerical value is applicable to the A and N values in AC characteristics.

● Set values and S values of asynchronous setup time setting register

Asynchronous setup time setting register				S
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15
0	0	0	0	16

The S (setup time) value of the setup time setting register in asynchronous data transfer represents the time required to assert the $\overline{REQ}$ or $\overline{ACK}$ signal after setting data at the data bus (in clock-cycle units).

The numerical value is applicable to the S value in AC characteristics.

REGISTER LIST

1. BASIC Control Register (At Write)

Address						Registe Name	Bit Assignment							
Decimal	A4	A3	A2	A1	A0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	SCSI output data register	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
1	0	0	0	0	1	SCSI output data register	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
2	0	0	0	1	0	Direct control register	DC7	×	×	×	×	×	×	DC0
3	0	0	0	1	1	(Reserved)	×	×	×	×	×	×	×	×
4	0	0	1	0	0	SEL/RESEL-ID register	SI7	×	×	×	SI3	SI2	SI1	SI0
5	0	0	1	0	1	Command register	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
6	0	0	1	1	0	Data block register (MSB)	BL15	BL14	BL13	BL12	BL11	BL10	BL9	BL8
7	0	0	1	1	1	Data block register (LSB)	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
8	0	1	0	0	0	Data byte register (MSB)	BY23	BY22	BY21	BY20	BY19	BY18	BY17	BY16
9	0	1	0	0	1	Data byte register	BY15	BY14	BY13	BY12	BY11	BY10	BY9	BY8
10	0	1	0	1	0	Data byte register (LSB)/MC byte register	BY7	BY6	BY5	BY4	BY3	BY2	BY1	BY0
11	0	1	0	1	1	Diagnostic control signal register	DG7	DG6	DG5	×	DG3	DG2	DG1	DG0
12	0	1	1	0	0	Transfer mode register	TM7	TM6	×	×	×	×	×	×
13	0	1	1	0	1	Transfer period register	×	×	×	TP4	TP3	TP2	TP1	TP0
14	0	1	1	1	0	Transfer offset register	×	×	×	TO4	TO3	TO2	TO1	TO0
15	0	1	1	1	1	Window address register	WA7	WA6	×	WA4	WA3	WA2	WA1	WA0

2. BASIC Control Register (At Read)

Address						Registe Name	Bit Assignment							
Decimal	A4	A3	A2	A1	A0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	SCSI input data register	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	0	0	1	SCSI input data register	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
2	0	0	0	1	0	SPC status register	SS7	SS6	SS5	×	SS3	SS2	SS1	SS0
3	0	0	0	1	1	Nexus status register	NS7	NS6	×	×	NS3	NS2	NS1	NS0
4	0	0	1	0	0	Interrupt status register	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
5	0	0	1	0	1	Command step register	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
6	0	0	1	1	0	Data block register (MSB)	BL15	BL14	BL13	BL12	BL11	BL10	BL9	BL8
7	0	0	1	1	1	Data block register (LSB)	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
8	0	1	0	0	0	Data byte register (MSB)	BY23	BY22	BY21	BY20	BY19	BY18	BY17	BY16
9	0	1	0	0	1	Data byte register	BY15	BY14	BY13	BY12	BY11	BY10	BY9	BY8
10	0	1	0	1	0	Data byte register (LSB)/MC byte register	BY7	BY6	BY5	BY4	BY3	BY2	BY1	BY0
11	0	1	0	1	1	SCSI control signal status register	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
12	0	1	1	0	0	Transfer mode register	TM7	TM6	×	×	×	×	×	×
13	0	1	1	0	1	Transfer period register	×	×	×	TP4	TP3	TP2	TP1	TP0
14	0	1	1	1	0	Transfer offset register	×	×	×	TO4	TO3	TO2	TO1	TO0
15	0	1	1	1	1	Modifier byte register	×	MB6	MB5	MB4	MB3	MB2	MB1	MB0

3. Initialization Window (At Write and Read)

Address					Registe Name	Bit Assignment							
Decimal	A4	A3	A2	A1	A0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16	1	0	0	0	0	Clock conversion setting register	×	×	×	×	CC3	CC2	CC1	CC0
17	1	0	0	0	1	Self-ID setting register	×	×	×	×	OI3	OI2	OI1	OI0
18	1	0	0	1	0	Response operation mode setting register	AM7	AM6	AM5	AM4	×	×	AM1	AM0
19	1	0	0	1	1	SEL/RESEL operation mode setting register	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0
20	1	0	1	0	0	SEL/RESEL retry setting register	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
21	1	0	1	0	1	SEL/RESEL timeout setting register	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
22	1	0	1	1	0	REQ/ACK timeout setting register	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
23	1	0	1	1	1	Asynchronous setup time setting register	×	×	×	×	AT3	AT2	AT1	AT0
24	1	1	0	0	0	Parity error detection setting register	PE7	PE6	PE5	PE4	PE3	×	PE1	PE0
25	1	1	0	0	1	Interrupt enable setting register	IE7	×	IE5	IE4	IE3	IE2	IE1	IE0
26	1	1	0	1	0	Group 6/7 command-length setting register	GL7	GL6	GL5	GL4	GL3	GL2	GL1	GL0

4. MCS Buffer Window

Address						At Write	At Read
Decimal	A4	A3	A2	A1	A0		
16	1	0	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
17	1	0	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
18	1	0	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
19	1	0	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
20	1	0	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
21	1	0	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
22	1	0	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
23	1	0	1	1	1	SEND MCS buffer	RECEIVE MCS buffer
24	1	1	0	0	0	SEND MCS buffer	RECEIVE MCS buffer
25	1	1	0	0	1	SEND MCS buffer	RECEIVE MCS buffer
26	1	1	0	1	0	SEND MCS buffer	RECEIVE MCS buffer
27	1	1	0	1	1	SEND MCS buffer	RECEIVE MCS buffer
28	1	1	1	0	0	SEND MCS buffer	RECEIVE MCS buffer
29	1	1	1	0	1	SEND MCS buffer	RECEIVE MCS buffer
30	1	1	1	1	0	SEND MCS buffer	RECEIVE MCS buffer
31	1	1	1	1	1	SEND MCS buffer	RECEIVE MCS buffer

5. User Program Memory Window

Address					At Write	At Read
Decimal	A4	A3	A2	A1	A0		
16	1	0	0	0	0	User program memory	User program memory
17	1	0	0	0	1	User program memory	User program memory
18	1	0	0	1	0	User program memory	User program memory
19	1	0	0	1	1	User program memory	User program memory
20	1	0	1	0	0	User program memory	User program memory
21	1	0	1	0	1	User program memory	User program memory
22	1	0	1	1	0	User program memory	User program memory
23	1	0	1	1	1	User program memory	User program memory
24	1	1	0	0	0	User program memory	User program memory
25	1	1	0	0	1	User program memory	User program memory
26	1	1	0	1	0	User program memory	User program memory
27	1	1	0	1	1	User program memory	User program memory
28	1	1	1	0	0	User program memory	User program memory
29	1	1	1	0	1	User program memory	User program memory
30	1	1	1	1	0	User program memory	User program memory
31	1	1	1	1	1	User program memory	User program memory

COMMAND LIST

The SPC commands can be set to the command register and user program memory.

The commands can be classified as follows depending on the setting methods.

- Sequential command
  This command performs the continuous sequential operations (including phase changes). It can be set only at the command register.

- Discrete command
  This command performs the discrete operations of the sequential command. It can be set at both the command register and user program memory.

- Special command
  This command is used to perform operations with the user program. It can be set only at the user program memory.

Setting / Common type	Setting at command register	Setting at command register
Sequential command	○ (1-byte command)	✕
Discrete command	○ (1-byte command)	○ (1- or 2-byte command)
Special command	✕	○ (1- or 2-byte command)

○ : Setting possible ✕ : Setting impossible

1. Initiator Command

(1) Sequential command

No		Command Code								Operand (When program executed)	Command Name
1	00H	0	0	0	0	0	0	0	0	(Impossible)	SELECT & CMD
2	01H	0	0	0	0	0	0	0	1	(Impossible)	SELECT & 1-MSG & CMD
3	02H	0	0	0	0	0	0	1	0	(Impossible)	SELECT & N-Byte-MSG & CMD
4	03H	0	0	0	0	0	0	1	1	(Impossible)	SELECT & 1-MSG
5	04H	0	0	0	0	0	1	0	0	(Impossible)	SELECT & N-Byte-MSG
6	05H	0	0	0	0	0	1	0	1	(Impossible)	SEND N-Byte-MSG
7	06H	0	0	0	0	0	1	1	0	(Impossible)	SEND N-Byte-CMD
8	07H	0	0	0	0	0	1	1	1	(Impossible)	RECEIVE N-Byte-MSG

(2) Discrete command

No		Command Code								Operand (When program executed)	Command Name
9	08H	0	0	0	0	1	0	0	0	—	SELECT
10	09H	0	0	0	0	1	0	0	1	—	SELECT with ATM
11	0AH	0	0	0	0	1	0	1	0	—	SET ATN
12	0BH	0	0	0	0	1	0	1	1	—	RESET ATN
13	0CH	0	0	0	0	1	1	0	0	—	SET ACK
14	0DH	0	0	0	0	1	1	0	1	—	RESET ACK
15	10H	0	0	0	1	0	0	0	0	—	SEND DATA from MPU
16	11H	0	0	0	1	0	0	0	1	—	SEND DATA from DMA
17	12H	0	0	0	1	0	0	1	0	—	RECEIVE DATA to MPU
18	13H	0	0	0	1	0	0	1	1	—	RECEIVE DATA to DMA
19	14H	0	0	0	1	0	1	0	0	—	SEND DATA from MPU (Padding)
20	15H	0	0	0	1	0	1	0	1	—	SEND DATA from DMA (Padding)
21	16H	0	0	0	1	0	1	1	0	—	RECEIVE DATA to MPU (Padding)
22	17H	0	0	0	1	0	1	1	1	—	RECEIVE DATA to DMA (Padding)
23	18H	0	0	0	1	1	0	0	0	Address of issued message	SEND 1-MSG
24	19H	0	0	0	1	1	0	0	1	Address of issued message	SEND 1-MSG with ATN
25	1AH	0	0	0	1	1	0	1	0	Address where message written	RECEIVE MSG
26	1BH	0	0	0	1	1	0	1	1	Address of issued command	SEND CMD
27	1CH	0	0	0	1	1	1	0	0	Address where status written	RECEIVE STATUS

2. Target Command

(1) Sequential command

No	Command Code									Operand (When program executed)	Command Name
1	20H	0	0	1	0	0	0	0	0	(Impossible)	RESELECT & 1-MSG
2	21H	0	0	1	0	0	0	0	1	(Impossible)	RESELECT & N-Byte-MSG
3	22H	0	0	1	0	0	0	1	0	(Impossible)	RESELECT & 1-MSG & TERMINATE
4	23H	0	0	1	0	0	0	1	1	(Impossible)	RESELECT & 1-MSG & LINK TERMINATE
5	24H	0	0	1	0	0	1	0	0	(Impossible)	TERMINATE
6	25H	0	0	1	0	0	1	0	1	(Impossible)	LINK TERMINATE
7	26H	0	0	1	0	0	1	1	0	(Impossible)	DISCONNECT SEQUENCE
8	27H	0	0	1	0	0	1	1	1	(Impossible)	SEND N-Byte-MSG
9	28H	0	0	1	0	1	0	0	0	(Impossible)	RECEIVE N-Byte-CMD
10	29H	0	0	1	0	1	0	0	1	(Impossible)	RECEIVE N-Byte-MSG
11	2AH	0	0	1	0	1	0	1	0	(Impossible)	RESELECT & N-Byte-MSG & TERMINATE
12	2BH	0	0	1	0	1	0	1	1	(Impossible)	RESELECT & N-Byte-MSG & LINK TERMINATE
13	2CH	0	0	1	0	1	1	0	0	(Impossible)	DISCONNECT SEQUENCE 2

(2) Discrete command

No	Command Code									Operand (When program executed)	Command Name
14	30H	0	0	1	1	0	0	0	0	—	RESELECT
15	31H	0	0	1	1	0	0	0	1	—	SET REQ
16	32H	0	0	1	1	0	0	1	0	—	RESET REQ
17	33H	0	0	1	1	0	0	1	1	—	DISCONNECT
18	34H	0	0	1	1	0	1	0	0	—	SEND DATA from MPU
19	35H	0	0	1	1	0	1	0	1	—	SEND DATA from DMA
20	36H	0	0	1	1	0	1	1	0	—	RECEIVE DATA to MPU
21	37H	0	0	1	1	0	1	1	1	—	RECEIVE DATA to DMA
22	38H	0	0	1	1	1	0	0	0	Address of issued message	SEND 1-MSG
23	39H	0	0	1	1	1	0	0	1	Address where message written	RECEIVE MSG
24	3AH	0	0	1	1	1	0	1	0	Address of issued status	SEND STATUS
25	3BH	0	0	1	1	1	0	1	1	Address where CDB* written	RECEIVE CMD

*CDB = Command Descriptor Block

3. Common Command

No	Command Code									Operand (When program executed)	Command Name
1	40H	0	1	0	0	0	0	0	0	(Impossible)	SOFYWARE RESET
2	41H	0	1	0	0	0	0	0	1	(Impossible)	TRANSFER RESET
3	42H	0	1	0	0	0	0	1	0	(Impossible)	SCSI RESET
4	43H	0	1	0	0	0	0	1	1	(Impossible)	SET UP REG
5	44H	0	1	0	0	0	1	0	0	(Impossible)	INIT DIAG START
6	45H	0	1	0	0	0	1	0	1	(Impossible)	TARG DIAG START
7	46H	0	1	0	0	0	1	1	0	(Impossible)	DIAG END
8	47H	0	1	0	0	0	1	1	1	(Impossible)	COMMAND PAUSE

4. Programmable Command

The user program is preset to the user program memory and starts operation when the starting address of the user program memory is written to the command register.

The programmable command has discrete and special commands and is 1- or 2-bytes long.

The command field assignment is given in the following table.

● Command field assignment

|	Command Code (First Byte)	Operand (Second Byte)
Discrete command	Send command in message, command, and status phases	Memory address where sent data exists
	Receive command in message, command, and status phases	Memory address where received data stored
	Command for disallowing receive/send command and transfer in data phase	—
Special command	AND command	Data for AND operation or memory address where data for AND operation exists
	TEST AND command	Data for AND operation or memory address where data for AND operation exists
	COMPARE command	Data for comparison operation or memory address where data for comparison operation exists
	Conditional-branch IF-GOTO command	Jump address
	MOVE command	Memory address to be moved
	STOP command	User status code
	NOP command	—

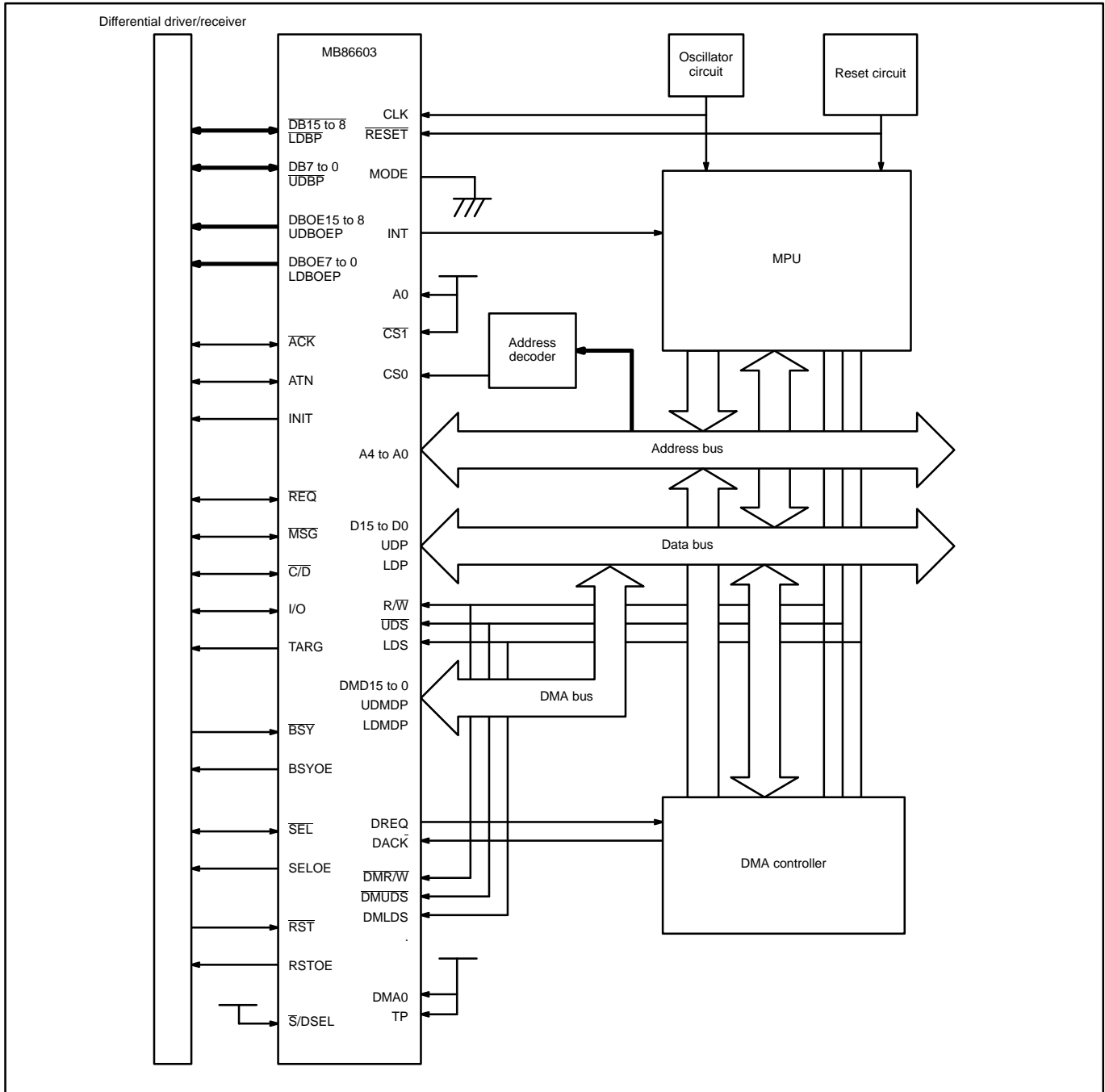# SYSTEM CONFIGURATION

1. 80-Series Separate Bus Type
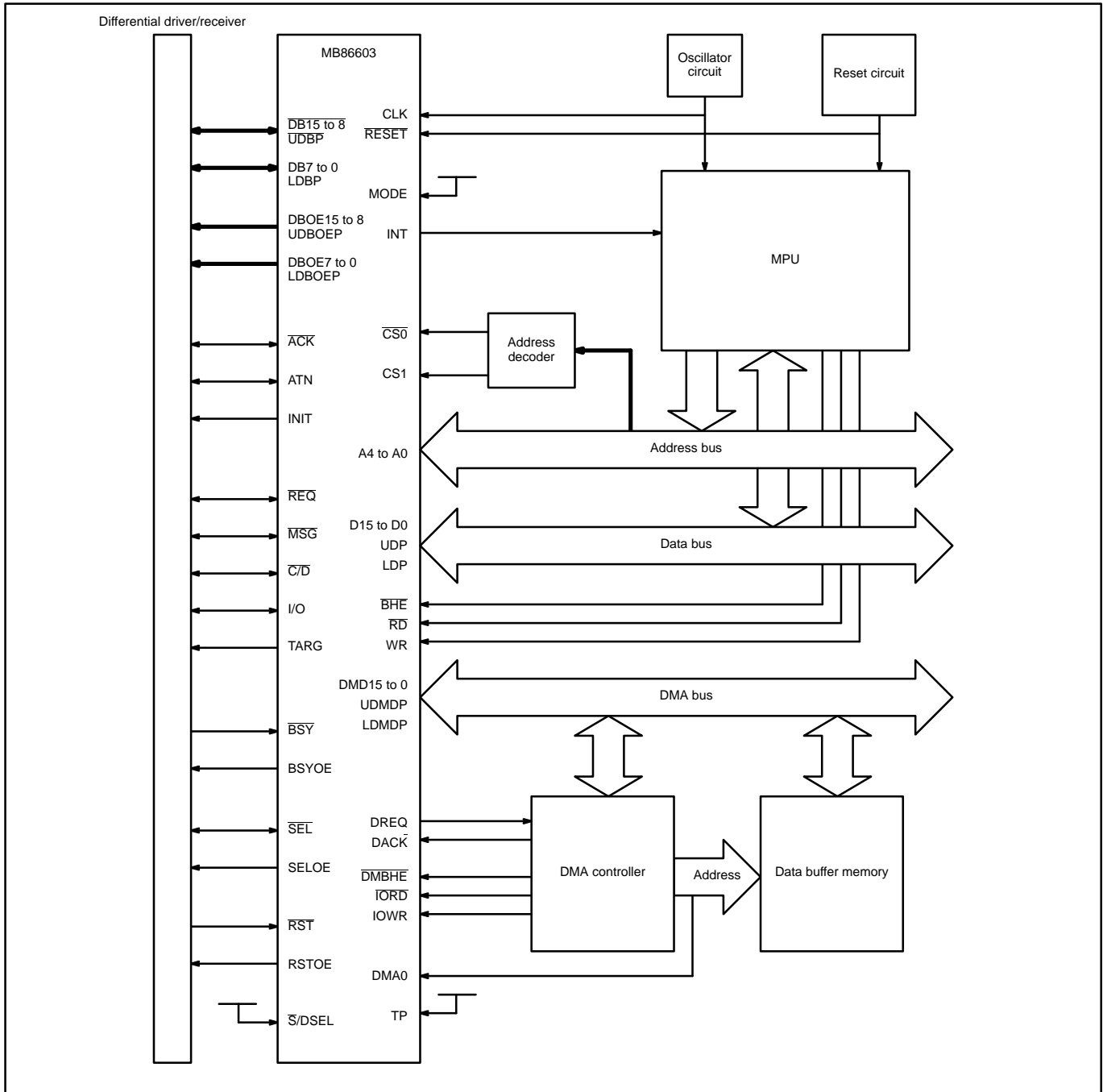
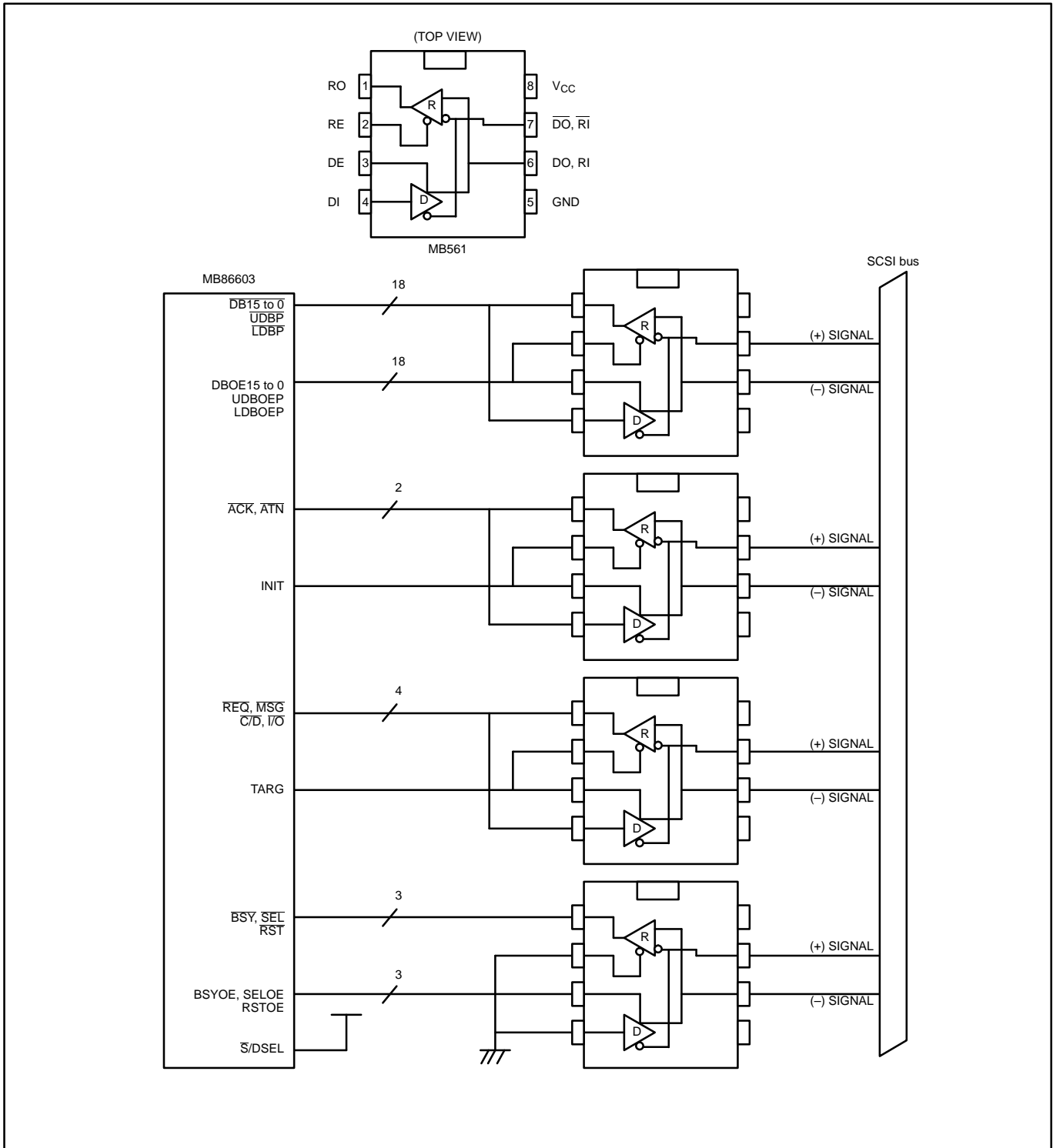## 2. 80-Series Common Bus Type
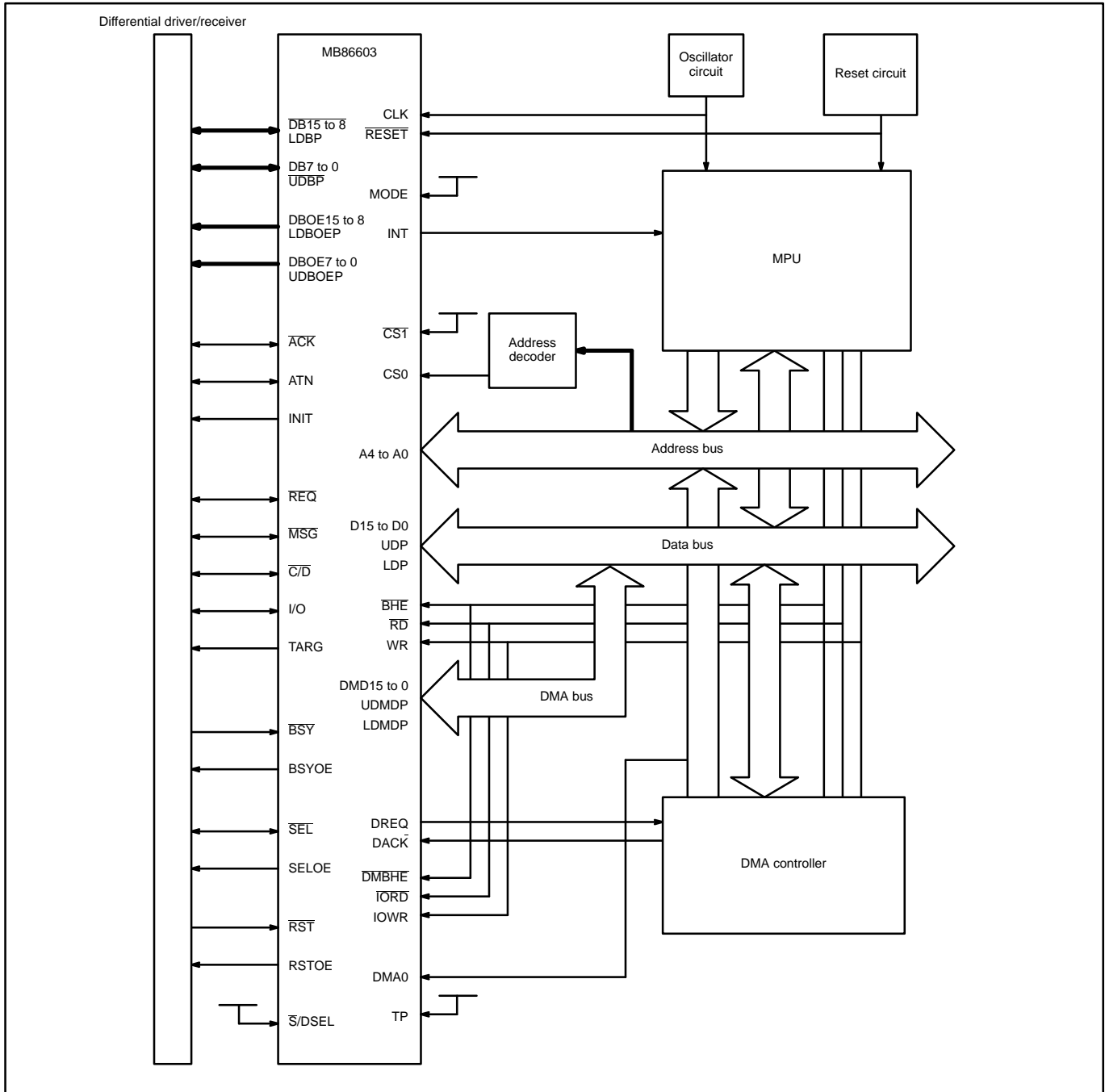
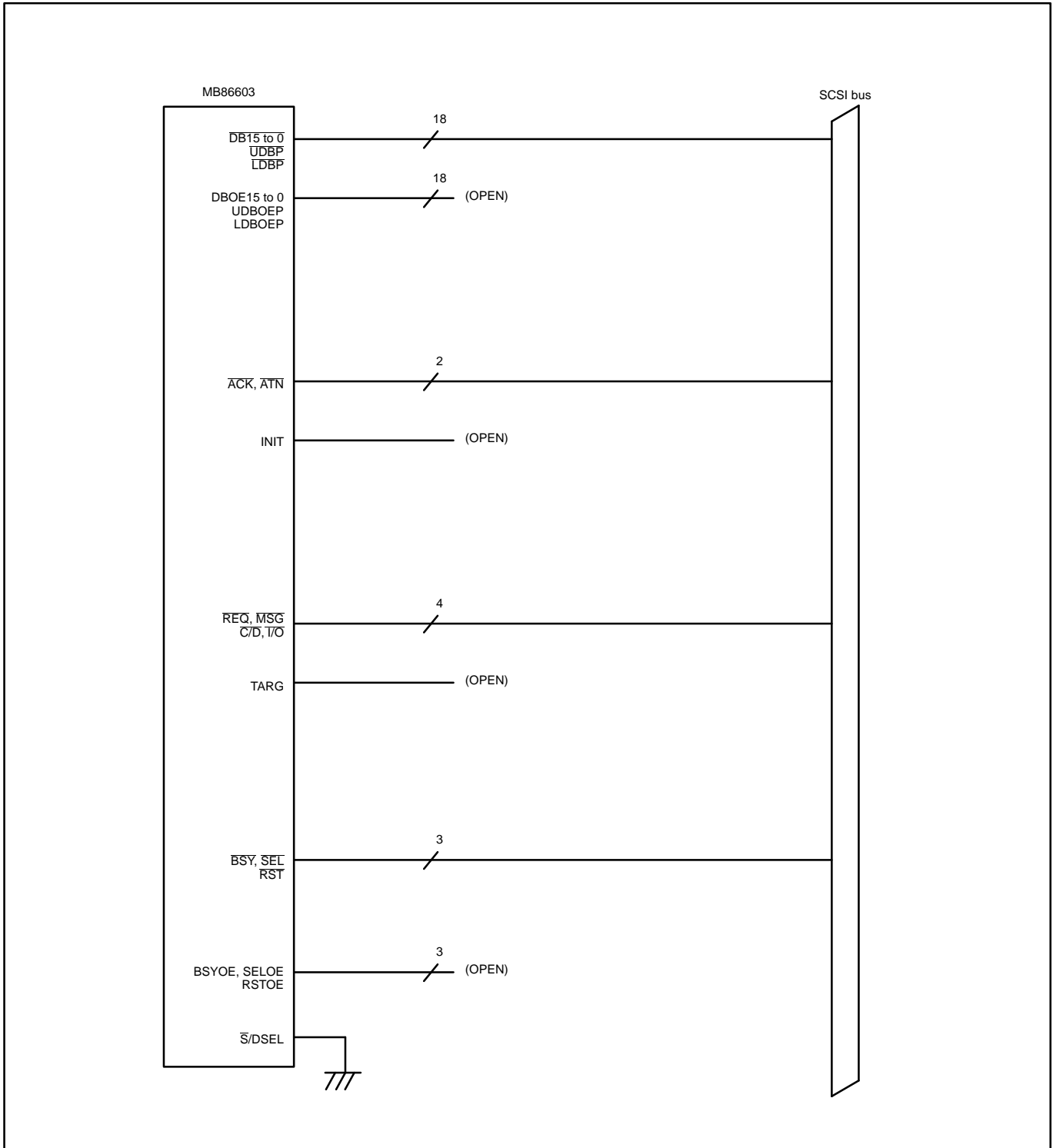## 3. 68-Series Separate Bus Type
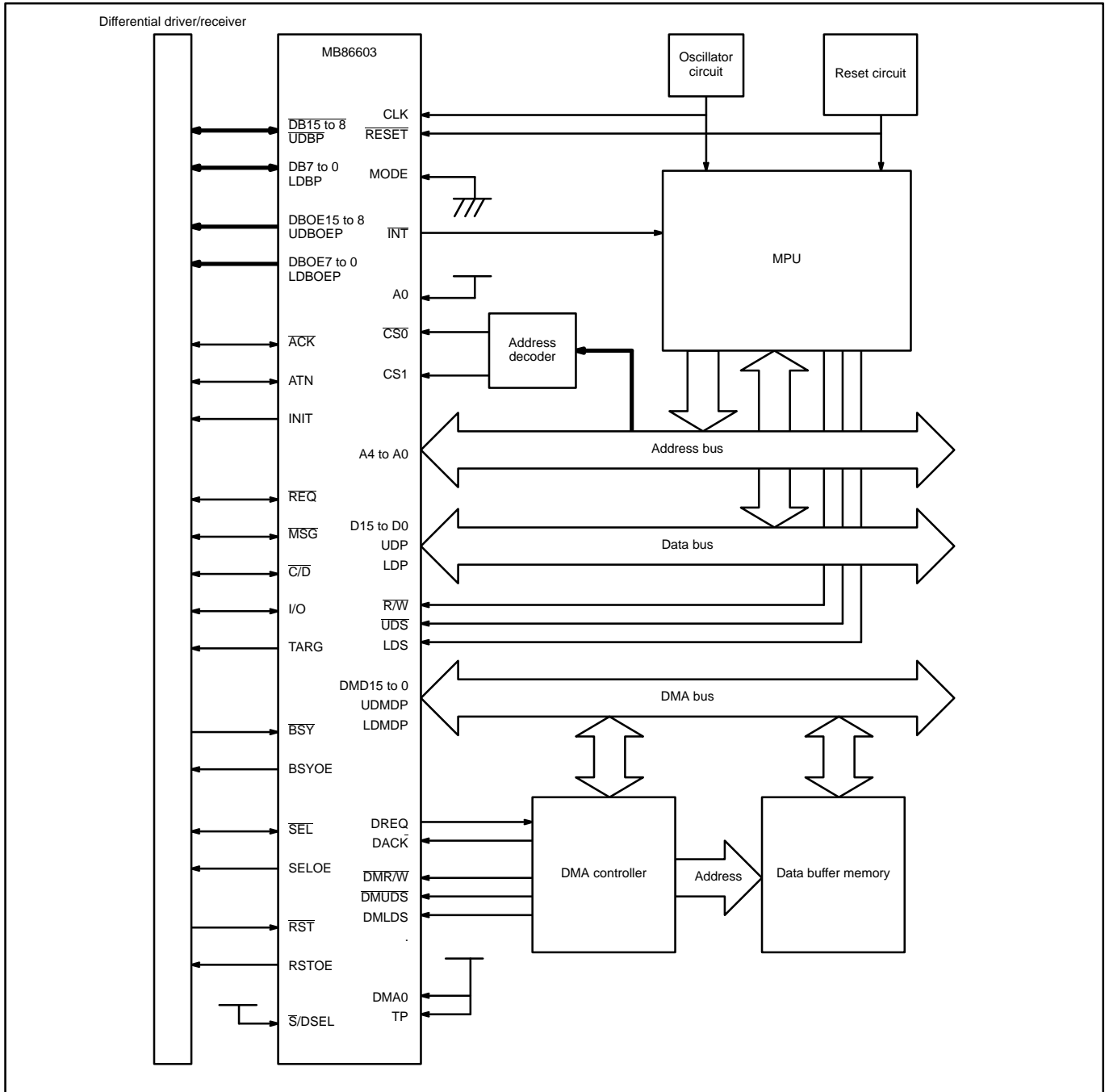
4. 68-Series Common Bus Type

5. Example of Connection in Differential Mode (Example of Driver/Receiver Connection)
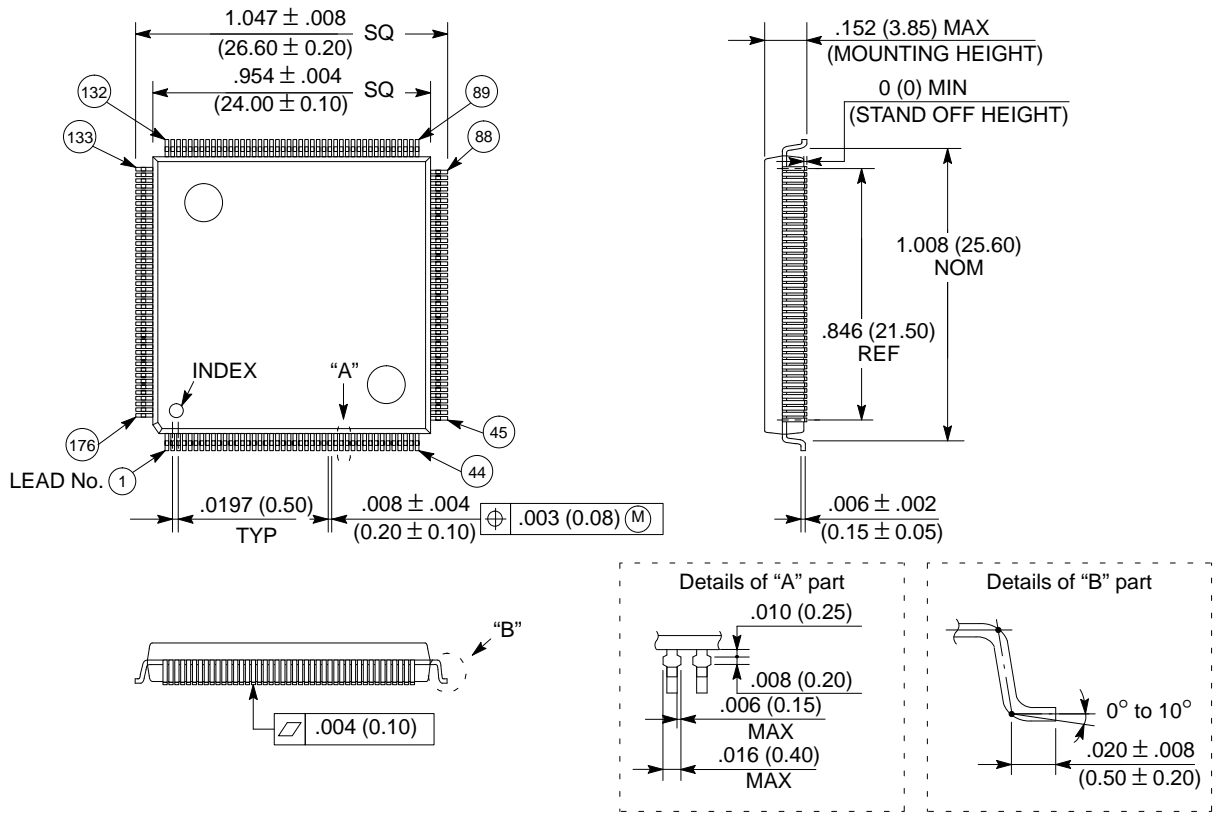
6. Example of Connection in Single-end Mode

PACKAGE DIMENSIONS

176-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-176P-M01)

1.047 ± .008
(26.60 ± 0.20) SQ

.954 ± .004
(24.00 ± 0.10) SQ

132
133
89
88

INDEX   "A"

176
45
44

LEAD No. 1

.0197 (0.50)
TYP

.008 ± .004
(0.20 ± 0.10)

⊕ .003 (0.08) Ⓜ

.152 (3.85) MAX
(MOUNTING HEIGHT)

0 (0) MIN
(STAND OFF HEIGHT)

1.008 (25.60)
NOM

.846 (21.50)
REF

.006 ± .002
(0.15 ± 0.05)

"B"

▱ .004 (0.10)

Details of "A" part

.010 (0.25)

.008 (0.20)

.006 (0.15)
MAX

.016 (0.40)
MAX

Details of "B" part

0° to 10°

.020 ± .008
(0.50 ± 0.20)

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Dimensions in
inches (millimeters)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Electronic Devices
International Operations Department
KAWASAKI PLANT, 1015 Kamikodanaka,
Nakahara–ku, Kawasaki–shi,
Kanagawa 211, Japan
Tel: (044) 754–3753
FAX: (044) 754–3332

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922–9000
FAX: (408) 432–9044/9045

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10,
63303 Dreieich-Buchschlag,
Germany
Tel: (06103) 690-0
FAX: (06103) 690-122

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
No.51 Bras Basah Road,
Plaza By The Park,
#06-04 to #06-07
Singapore 0718
Tel: 336-1600
FAX: 336-1609