FUJITSU

Wireless Communications Products

Including Power Management

Data Book

1996 Rev. 1.0

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Fujitsu Limited
Tokyo, Japan

Fujitsu Microelectronics, Inc.
San Jose, California, U.S.A.

This document is published by the Product Communications Department, Fujitsu Microelectronics, Inc., 3545 North First Street, San Jose, California, U.S.A 95134–1804

Printed in the U.S.A.

PREFACE

This data book contains the latest product information which is part of the vast line of Fujitsu's Telecommunications Products that supports the rapidly growing markets for Wireless Communications products and services. This edition includes Prescalers, CMOS PLLs, Super PLLs, Super Analog RF Devices, high performance Piezoelectric Bandpass SAW Filters, and Power Management Switches. All of these products are manufactured to meet the high standard of quality and reliability that is found in all of Fujitsu's products.

Fujitsu Microelectronics, Inc. (FMI), is further committing to higher levels of product support and information responsiveness to its valued customers through the establishment of a Customer Response Center (CRC) and a site on the Internet World Wide Web (WWW). The CRC, planned to be operational in Oct, 1995, will give you the convenience of calling one number (1–800–866–8608) for support of your product questions and information needs. In addition, the Internet WWW site for FMI (www.fmi.fujitsu.com) is in the process of being registered and will be brought on–line to give you quick and easy access to the vast array of information covering the large number of product lines supported by FMI. Our goal is to provide all of our customers the best possible support and attention they deserve.

Contents and Alphanumeric Product List

SECTION 4 – Super PLLs (Single Chip PLLs/Prescalers)

SECTION 5 – Super Analog RF Devices — *At a Glance* 5-1

SECTION 6 – BiCMOS LSI RF Integrated Circuits — *At a Glance* 6-1

SECTION 1

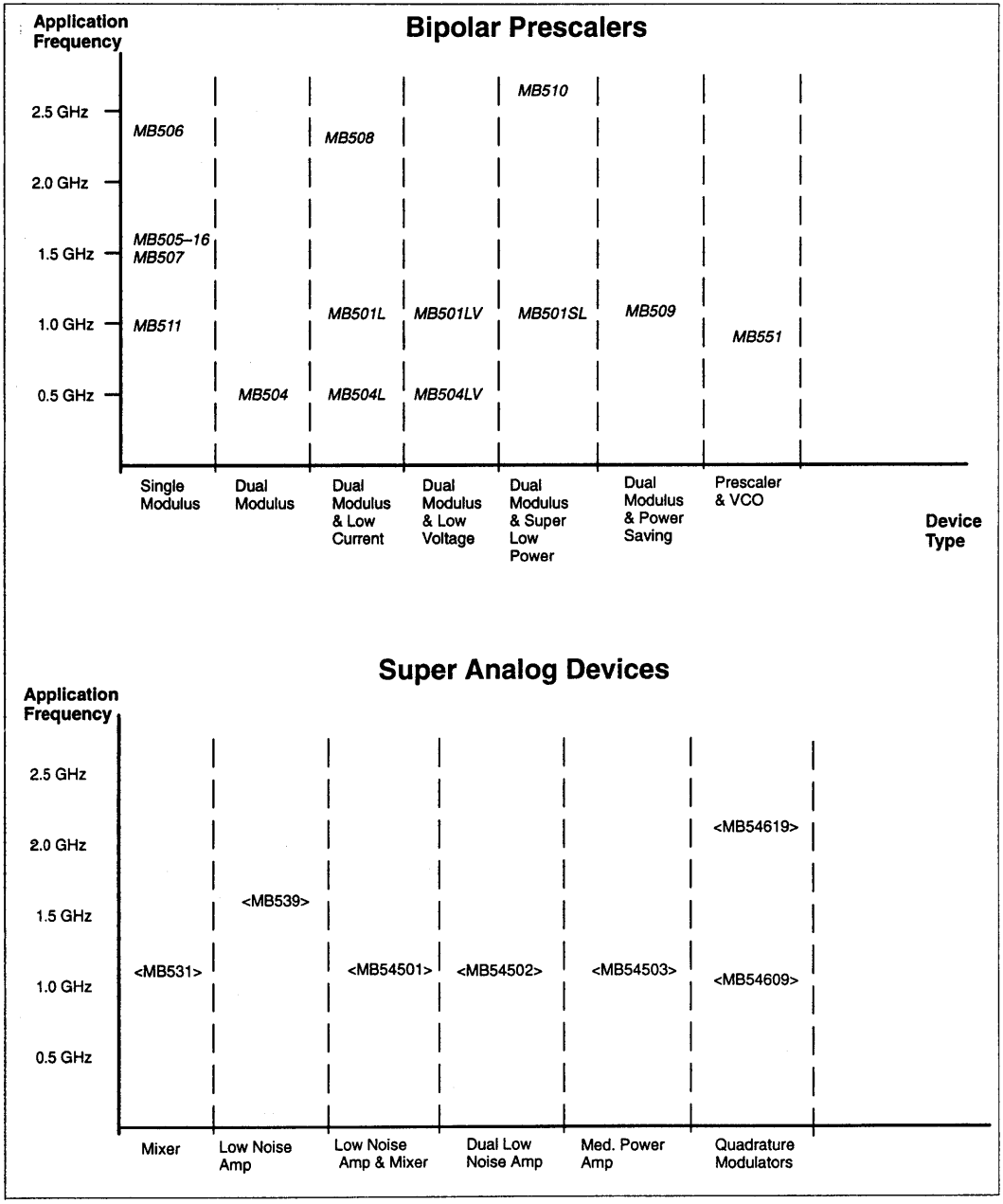
Introduction and Quick Selection Guide

Telecommunication Devices

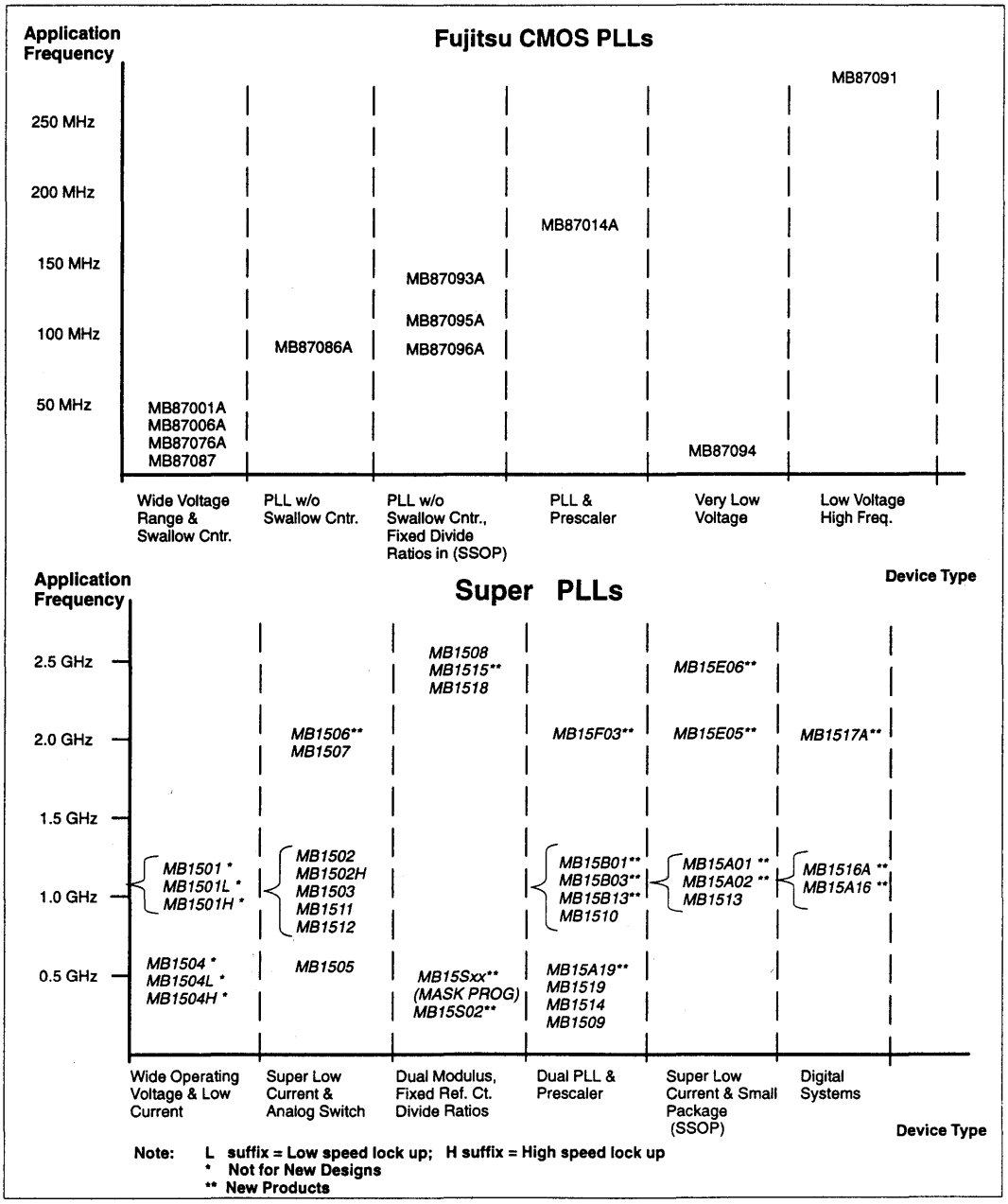
Fujitsu's Telecom IC product offering includes a wide range of leading edge RF/Wireless parts for use in diverse applications such as cellular telephones, cordless telephones, PCS/PCN systems, wireless PBX systems, wireless LAN/WAN systems, pagers, cable television converter boxes and a variety of portable wireless communication devices. The core product families for RF/Wireless applications include Prescalers, Phase–Locked Loops (PLLs), SingleChip PLL/Prescalers (Super PLLs), RF Analog Devices (Super Analog), and Piezoelectric Devices (SAW Filters and VCOs/Modulators). These products are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

- **Prescalers**
  Fujitsu offers a wide range of prescaler devices capable of satisfying the technical requirements of today's applications. Features include devices covering the 200 MHz to 2.7 GHz range, low power consumption, and a multitude of divide ratios.
- **PLLs**
  The Fujitsu family of PLLs offers a wide range of operation frequencies with low supply current and voltages to meet many diverse design requirements. A serial input programming capability is a feature of all Fujitsu's PLLs.
- **Super PLLs**
  Fujitsu is one of only a few semiconductor manufacturers to offer single–chip PLL/Prescaler devices and was the creator of the industry standard MB1501. These devices are manufactured using an advanced BiCMOS process that combines high speed and low power consumption in a single chip. With the increased emphasis on board space reduction to improve cost, reliability, and overall end product size for portable applications, these single–chip devices are an ideal solution for wireless systems designers.
- **Super Analog**
  Included are a series of highly integrated Analog RF devices such as Low Noise Amplifiers (LNA), Modulators, Demodulators and Mixers that are typically used in the front ends of mobile and portable wireless communication systems. These include single and multi–function devices based on Fujitsu's advanced RF BiCMOS and Bipolar processes which are second to none.
- **Piezoelectric Devices**
  Fujitsu's lithium tantalate piezoelectric bandpass SAW Filters provide sharp roll–off characteristics and excellant stability over temperature in very small 3.8 mm x 3.8 mm or 5 mm x 5 mm surface mount packages. Standard transmit and receive frequencies are available for AMPS, NTACS, ETACS, NMT/GSM, NTT, PDC and ISM/USA. This family of devices also includes a series of Voltage Controlled Oscillators (VCOs) and Modulators

Quick Selection Guide – Prescaler, Super Analog



Quick Selection Guide – CMOS PLLs, Super PLLs



Note: L suffix = Low speed lock up; H suffix = High speed lock up
* Not for New Designs
** New Products

Bipolar Prescalers – 200 MHz to 2.7 GHz

Device Part No.	Frequency (Maximum)	Divide Ratio	I_{CC} (Typ.)	V_{CC}	Package
MB501L	1.1 GHz	64/65, 128/129	10 mA	5 V	8-pin DIP, SOP
MB501LV	1.1 GHz	64/65, 128/129	12 mA	3 V	8-pin DIP, SOP
MB501SL	1.1 GHz	64/65, 128/129	5 mA	5 V	8-pin DIP, SOP
MB504	520 MHz	32/33, 64/65	10 mA	5 V	8-pin DIP, SOP
MB504L	520 MHz	32/33, 64/65	5 mA	5 V	8-pin DIP, SOP
MB504LV	520 MHz	32/33, 64/65	6 mA	3 V	8-pin DIP, SOP
MB505-16	1.6 GHz	128, 256	9 mA	5 V	8-pin DIP, SOP
MB506	2.4 GHz	64, 128, 256	18 mA	5 V	8-pin DIP, SOP
MB507	1.6 GHz	128/129, 256/257	18 mA	5 V	8-pin DIP, SOP
MB508	2.3 GHz	128/129, 256/257, 512/514	24 mA	5 V	8-pin DIP, SOP
MB509	1.1 GHz	64/65, 128/129	12 mA	5 V	8-pin DIP, SOP
MB510	2.7 GHz	128/144, 256/272	10 mA	5 V	8-pin DIP, SOP
MB511	1.0 GHz	1, 2, 8	23 mA	5 V	8-pin DIP, SOP

Prescaler/VCO

Device Part No.	Frequency (Maximum)	Divide Ratio	I_{CC} (Typ.)	V_{CC}	Package
MB551	1.0 GHz	128/129	16 mA	5 V	8-pin SOP

Super Analog Devices

Device Part No.	Frequency (Maximum)	Features	I_{CC} (Typ.)	V_{CC}	Package
MB531	1.1 GHz	Tx Mixer	12.7 mA	5 V	8-pin SSOP
MB539	1.6 GHz	Low Noise Amp	8 mA	5 V	8-pin SSOP
MB54501	1.1 GHz	LNA/Mixer	6 mA	3 V	16-pin SSOP
MB54502	1.1 GHz	Dual LNAs	4 mA	3 V	16-pin SSOP
MB54503	1.1 GHz	PA Driver Amp	26 mA	3.6 V	16-pin SSOP
MB54609	1.0 GHz	I/Q Modulator	20 mA	3 V	20-pin SSOP
MB54619	2.0 GHz	I/Q Modulator	25 mA	3 V	20-pin SSOP

Low Power CMOS Phase Locked Loops (PLLs)

Device Part No.	f_{IN} MHz @ 3V/5V (max)	Divide Ratio			I_{DD} mA @ 3V/5V	V_{DD}	Package
		N Prog. Ct.	A Swal-low	R Refer. Ct.			
MB87001A	10/13	5–1023	0–127	8–2048	2.0/3.0	2.7 – 5.5 V	16-pin DIP, SOP
MB87006A	10/17	5–1023	0–127	Binary 5–16383	2.5/3.5	3.0 – 6.0 V	16-pin DIP, SOP
MB87014A	–/180	5–1023	0–63	Binary 5–65535	–/ 8.0	4.5 – 5.5 V	16-pin DIP, SOP
MB87076	10/10	5–2047	0–127	Binary 5–16383	2.5/3.0	2.7 – 5.5 V	16-pin DIP, SOP
MB87086A	–/95	5–1023	–	Binary 5–65535	–/ 8.0	4.5 – 5.5 V	16-pin DIP, SOP
MB87087	10/17	5–1023	0–127	Binary 5–16383	2.5/3.5	3.0 – 6.0 V	16-pin DIP, SOP
MB87091	300/–	5–4095	0–63	Binary 5–16383	8.0/–	2.7 – 3.3 V	16-pin DIP, SOP, SSOP
MB87093A	–/145	725	–	64	–/10	4.5 – 5.5 V	16-pin SSOP
MB87094	15 @ 1.1 V	5–2047	0–127	Binary 5–4095	1 @ 1.1 V	1.1 –1.7 V	16-pin SSOP
MB87095A	–/110	550	–	64	–/10	4.5 – 5.5 V	16-pin SSOP
MB87096A	–/90	750	–	128	–/10	4.5 – 5.5 V	16-pin SSOP

BiCMOS Single-Chip PLL/Prescalers (Super PLLs)

Device Part No.	Prescaler		PLL			I_{CC} (typ)	V_{CC}	Package
	f_{IN} (max)	Divide Ratio	N Prog. Ct.	A Swallow Ct.	R Refer. Ct.			
MB15A01	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 6-16383	6.5 mA	3 V	16-pin SSOP
MB15B01**	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	13 mA	3 V	20-pin SSOP
MB1501*	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	15 mA	3–5 V	16-pin DIP, SOP
MB1501H*	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	15 mA	3–5 V	16-pin SOP
MB1501L*	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	15 mA	3–5 V	16-pin SOP
MB15A02	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 6-16383	7 mA	5 V	16-pin SSOP
MB1502	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	8 mA	5 V	16-pin SOP
MB1502H	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	8 mA	5 V	16-pin SOP
MB15B03**	1.1 GHz 0.3 GHz	64/65, 128/129 16/17, 32/33	Binary 5–2047	Binary 0–127	Binary 6–16383	10 mA	3 V	16-pin SSOP
MB15F03**	2.0 GHz 0.5 GHz	64/65, 128/129 16/17, 32/33	Binary 5–2047	Binary 0–127	Binary 6–16383	9 mA	3 V	16-pin SSOP
MB1503	1.1 GHz	128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	8 mA	5 V	16-pin SOP
MB1504*	520 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	Binary 8-16383	10 mA	3–5 V	16-pin SOP
MB1504H*	520 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	Binary 8-16383	10 mA	3–5 V	16-pin SOP
MB1504L*	520 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	Binary 8-16383	10 mA	3–5 V	16-pin SOP
MB15E05	2.0 MHz	64/65 128/129	Binary 5–2047	Binary 0–255	Binary 8-16383	6 mA	3 V	16-pin SSOP
MB1505	600 MHz	32/33 64/65	Binary 16–2047	Binary 0–63	Binary 8-16383	6 mA	5 V	16-pin SOP
MB15E06	2.5 GHz	64/65 128/129	Binary 5–2047	Binary 0–255	Binary 8-16383	7 mA	3 V	16-pin SSOP
MB1506	2.0 GHz	128/129 256/257	Binary 5–2047	Binary 0–255	Binary 8-16383	18 mA	5 V	20-pin SSOP

* Not for New Designs
** Dual PLL/prescaler set

BiCMOS Single-Chip PLL/Prescalers (Super PLLs) continued

MB1507	2.0 GHz	128/129 256/257	Binary 16–2047	Binary 0–255	Binary 8-16383	18 mA	5 V	16-pin SOP
MB1508	2.5 GHz	256/272 512/528	Binary 32–4095	Binary 0–31	256/512 1024/2048	16 mA	5 V	20-pin SOP
MB1509**	400 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	512, 1024	8 mA	3 V	20-pin SOP
MB15U10**	1.1 GHz	NA	Binary 1024– 131071	NA	Binary 6–4095	7 mA	3 V	20–pin SSOP
MB1510**	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	512, 1024	15 mA	3–5 V	20–pin SOP
MB15B11**	1.1 GHz 0.4 GHz	64/65, 128/129 32/33, 64/65	Binary 16–2047	Binary 0–127	Binary 8–16383	9.5 mA	3 V	20-pin SSOP
MB1511	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	7 mA	3–5 V	20-pin SSOP
MB1512	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	7 mA	3–5 V	20-pin SSOP
MB15B13**	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	13 mA	3 V	20-pin SSOP
MB1513	1.1 GHz	128/129	Binary 16–2047	Binary 0–127	Binary 8-16383	7 mA	3–5 V	20-pin SSOP
MB1514**	400 MHz	64/65	Binary 16–2047	Binary 0–127	1700	8 mA	3 V	20-pin SOP
MB1515	2.5 GHz	256/272 512/528	Binary 32–4095	Binary 0–31	256, 512 1024, 2048	6.5 mA	5 V	20-pin SSOP
MB15A16	1.1 GHz	NA	Binary 5–2047	Binary 0–127	Binary 6-16383	6.5 mA	3 V	16-pin SSOP
MB1516A	1.1 GHz	64/65 128/129	Binary 5–2047	Binary 0–127	Binary 6-16383	6.5 mA	3 V	16-pin SSOP
MB1517A	2.0 GHz	64/65 128/129	Binary 16–2047	Binary 0–255	Binary 6-16383	14 mA	3 V	16-pin SSOP
MB1518	2.5 GHz	512/528	Binary 32–511	Binary 0–31	512	16 mA	5 V	16-pin SOP
MB15A19**	600 MHz	64/65	Binary 16–2047	Binary 0–127	256, 2048	11 mA	3 V	20-pin SOP
MB1519**	600 MHz	64/65	Binary 16–2047	Binary 0–127	512, 1024	11 mA	3 V	20-pin SOP
MB15Sxx Series	300 MHz	16/17	Binary 5–4095	Binary 0–31	Binary 5–4095	3.5 mA	3 V	8-pin SSOP
MB15S02	284 MHz 116 MHz	16/17	Fixed 17 Fixed 7	Fixed12 Fixed 4	Fixed13 Fixed 13	3.5 mA	3 V	8-pin SSOP

* Not for New Designs
** Dual PLL/prescaler set

RF/WIRELESS PRODUCTS

F5CB Series SAW Filters for Mobile Communications

The F5CB series are wide bandpass Surface Acoustic Wave (SAW) filters for use in the 700 MHz to 1 GHz range. The F5CB series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) which has a high electromechanical coupling coefficient. The $LiTaO_3$ also provides wide bandwidths and exceptional stability. Fujitsu's exclusive mounting technology makes the F5CB series very compact and surface mountable. The F5CB is suitable for use in handheld cellular phones.

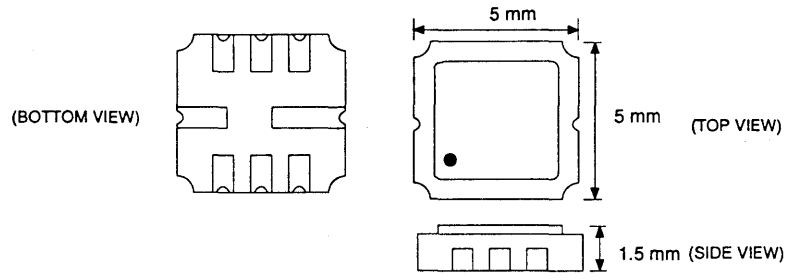
- Considerably smaller and lighter than a ceramic filter
- Surface mount package (SMT)
- High stopband attenuation types available
- Wide variety of bandwidths for world-wide systems
- Low insertion loss
- High power rating: 0.2 W guaranteed
- External impedance matching
- Package : 8-pad ceramic LCC (5.0 mm x 5.0 mm x 1.5 mm)

Product Line-up

Part Number	System	Use	Center Frequency (MHz)	Bandwidth (MHz)	Comment
FAR-F5CB-836M50-G201	AMPS/ADC	Tx	836.5	25	
FAR-F5CB-881M50-G201	AMPS/ADC	Rx	881.5	25	
FAR-F5CB-881M50-G211	AMPS/ADC	Rx	881.5	25	High stopband attenuation
FAR-F5CB-888M50-G201	ETACS	Tx	888.5	33	
FAR-F5CB-933M50-G202	ETACS	Rx	933.5	33	
FAR-F5CB-933M50-G212	ETACS	Rx	933.5	33	High stopband attenuation
FAR-F5CB-902M50-G201	NMT/GSM	Tx	902.5	25	
FAR-F5CB-947M50-G201	NMT/GSM	Rx	947.5	25	
FAR-F5CB-947M50-G211	NMT/GSM	Rx	947.5	25	High stopband attenuation
FAR-F5CB-911M50-G201	NTACS	Tx	911.5	27	
FAR-F5CB-933M50-G201	NTT	Tx	933.5	17	
FAR-F5CB-878M50-G201	NTT	Rx	878.5	17	

Package

8 Pad Ceramic LCC



F5CC (L2) Series SAW Filters – 50Ω Matched for Mobile Communication

The F5CC series are wide bandpass Surface Acoustic Wave (SAW) filters for use in the 700 MHz to 1 GHz range. The F5CC series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) which has a high electromechanical coupling coefficient. The $LiTaO_3$ also provides wide bandwidths and exceptional stability. The F5CC(L2) series is ultra compact and surface mountable which makes it suitable for use in hand held cellular phones

- Ultra compact, light weight
- No external matching circuitry necessary
- Lower insertion loss
- SMT Package
- Wide variety of standard products for all the world's major telecommunications systems
- High power rating: 0.2 W
- Package : 6-pad ceramic LCC (3.8 mm x 3.8 mm x 1.5 mm)

Product Line-up – Standard Version

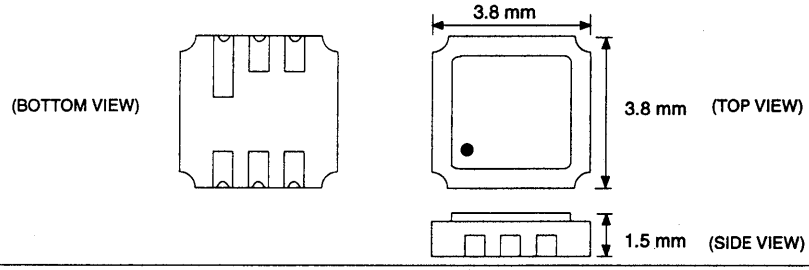
Part Number	System	Part Symbol	Center Frequency (MHz)	Bandwidth (MHz)
FAR-F5CC-836M50-L2AA	AMPS/ADC (Tx)	AA	836.5	25
FAR-F5CC-881M50-L2AB	AMPS/ADC (Rx)	AB	881.5	25
FAR-F5CC-933M50-L2BA	NTT (Tx)	BA	933.5	17
FAR-F5CC-878M50-L2BB	NTT (Rx)	BB	878.5	17
FAR-F5CC-888M50-L2CA	ETACS (TX)	CA	888.5	33
FAR-F5CC-933M50-L2CB	ETACS (RX)	CB	933.5	33
FAR-F5CC-911M50-L2DA	NTACS (Tx)	DA	911.5	27
FAR-F5CC-856M50-L2DB	NTACS (Rx)	DB	856.5	27
FAR-F5CC-902M50-L2EA	NMT/GSM (Tx)	EA	902.5	25
FAR-F5CC-947M50-L2EB	NMT/GSM (Rx)	EB	947.5	25
FAR-F5CC-897M50-L2KA	E-GSM (Tx)	KA	897.5	35
FAR-F5CC-942M50-L2KB	E-GSM (Rx)	KB	942.5	35
FAR-F5CC-950M00-L2FA	PDC (Tx)	FA	950.0	20
FAR-F5CC-820M00-L2FB	PDC (Rx)	FB	820.0	20
FAR-F5CC-915M00-L2JA	ISM/USA	JA	915.0	26
FAR-F5CC-935M00-L2LA	2-Way Pager	LA	935.0	12

Product Line-up – High Attenuation Version

Part Number	System	Part Symbol	Center Frequency (MHz)	Bandwidth (MHz)
FAR-F5CC-836M50-L2AZ	AMPS/ADC (Tx)	AZ	836.5	25
FAR-F5CC-881M50-L2AY	AMPS/ADC (Rx)	AY	881.5	25
FAR-F5CC-902M50-L2EZ	NMT/GSM (Tx)	EZ	902.5	25
FAR-F5CC-947M50-L2EY	NMT/GSM (Rx)	EY	947.5	25
FAR-F5CC-947M50-L2EX	NMT/GSM (Rx)	EX	947.5	25
FAR-F5CC-942M50-L2KY	E-GSM (Rx)	KY	942.5	35
FAR-F5CC-915M00-L2JZ	ISM/USA	JZ	915.0	26

Package

6 Pad Ceramic LCC



F6Cx (L2) Series SAW Filters – 50Ω Matched for Mobile Communication

The F6Cx series are wide bandpass Surface Acoustic Wave (SAW) filters for use in the 1 GHz to 2.5 GHz range. The F6Cx series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) which has a high electromechanical coupling coefficient. The $LiTaO_3$ also provides wide bandwidths and exceptional stability. The F6Cx(L2) series is ultra compact and surface mountable which makes it suitable for use in hand held cellular and PCS phones. Several new standard devices for PCS/PCN Systems have recently been added to the F6Cx Series SAW Filters.

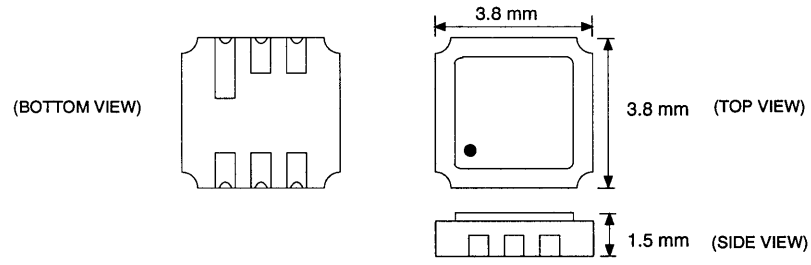
- Ultra compact, light weight
- No external matching circuitry necessary
- Lower insertion loss
- SMT Package
- Wide variety of standard products for all the world's major telecommunications systems
- High power rating: 0.2 W
- Packages:
  F6CC (L2): 6-pad ceramic LCC (3.8 mm x 3.8 mm x 1.5 mm)
  F6CE (L2): 6-pad ceramic LCC (3.0 mm x 3.0 mm x 1.2 mm)

Product Line-up – Standard Version

Part Number	System	Part Symbol	Center Frequency (MHz)	Bandwidth (MHz)
FAR–F6CC–1G4410–L2ZA	PDC (Tx)	ZA	1441.0	24
FAR–F6CC–1G4890–L2ZB	PDC (Rx)	ZB	1489.0	24
FAR–F6CC–1G6190–L2ZN	PDC (Lo)	ZN	1619.0	24
FAR–F6CE–1G7475–L2YA	DCS (Tx)	YA	1747.5	75
FAR–F6CE–1G8425–L2YB	DCS (Rx)	YB	1842.5	75
FAR–F6CE–1G8800–L2XA	PCS (Tx)	XA	1880.0	60
FAR–F6CE–1G9600–L2XB	PCS (Rx)	XB	1960.0	60
FAR–F6CE–2G4500–L2WA	ISM/WLAN	WA	2450.0	100

Package

6 Pad Ceramic LCC for F6CC (L2) Series



M2 Series (D100) General Purpose Voltage Controlled Oscillators

The M2 series (D100) voltage controlled oscillators (VCO) operate in the frequency range of 4 to 30 MHz. The M2 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) which has a high electromechanical coupling coefficient. The $LiTaO_3$ also provides a wide variable frequency range and exceptional stability.

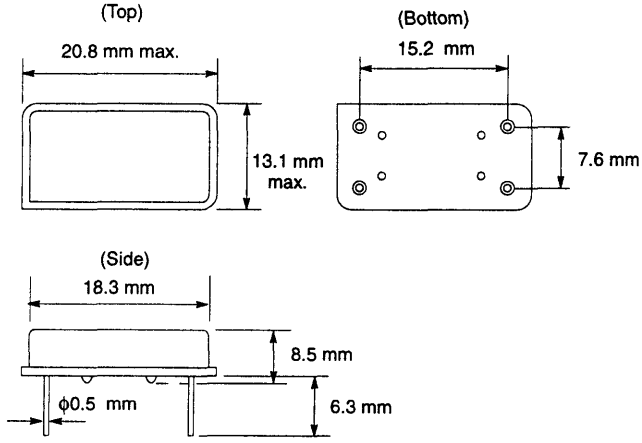
- Wide variable frequency width: ± 0.2%
- High precision oscillation frequency, ready for use without adjustment
- High reliability due to hermetically sealed package
- Custom frequencies also available
- Package: 4 pin metal case compatible with 14 pin DIP IC package

Standard Frequencies (MHz)

8.192	13.500	16.934	21.053	27.338
9.408	14.318	17.734	21.477	28.224
11.290	16.000	18.432	22.579	28.322
11.580	16.257	18.816	24.576	26.636
12.288	16.384	20.480	25.175	33.868

Package

Metal Case DIP 14



M2 Series (D300) Voltage Controlled Oscillators for Digital Audio

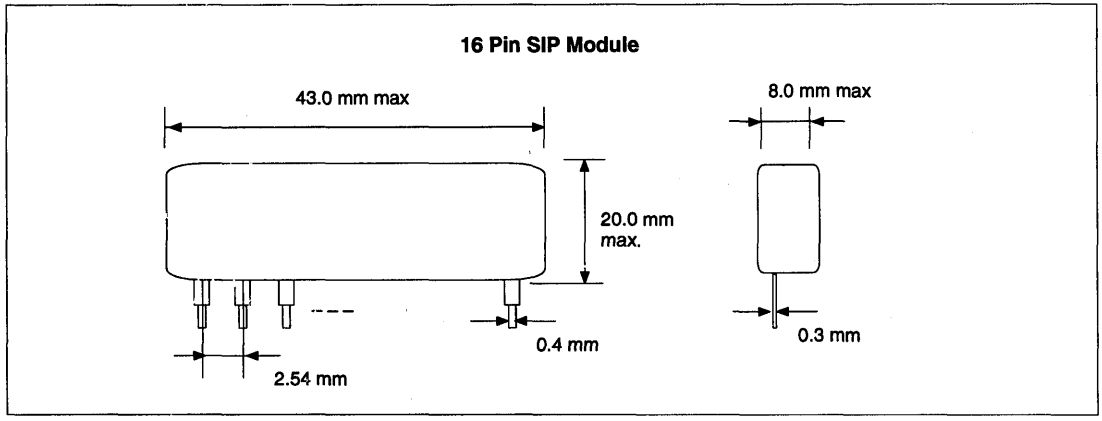
The M2 series (D300) voltage controlled oscillators (VCO) operate in the frequency range of 4 to 30 MHz. They use a single lithium tantalate piezoelectric crystal ($LiTaO_3$) which has a high electromechanical coupling coefficient. The $LiTaO_3$ also provides a wide variable frequency range and exceptional stability. The D300 module contains 3 VCOs for the three sampling frequencies used in digital audio equipment (32, 44.1, and 48 kHz). The frequencies are selected by external signals.

- Clock replay in response to 3 sampling frequencies (32, 44.1 and 48 kHz)
- Wider variable frequency width than in quartz crystals: ± 0.1 % or more
- Excellent stability for signal noise reproduced by high quality of the lithium tantalate
- 100 times more stable than VCOs of LC and TTL IC configuration
- 3 sampling frequencies controlled at CMOS logic level
- Compatible with the Electronic Industry Association of Japan (EIAJ) digital I/O standard type II (consumer digital audio equipment), Level I (high resolution mode and Level II (standard resolution mode)
- Package: 16 pin Single in Line Package for high density mounting

Standard Combinations of Frequencies

Type A	f_{01} (L)	8.192 MHz	32 kHz x 256
	f_{02} (M)	11.290 MHz	44.1 kHz x 256
	f_{03} (H)	12.288 MHz	48 kHz x 256
Type B	f_{01} (L)	12.288 MHz	32 kHz x 384
	f_{02} (M)	16.934 MHz	44.1 kHz x 384
	f_{03} (H)	18.432 MHz	48 kHz x 384
Type C	f_{01} (L)	16.384 MHz	32 kHz x 512
	f_{02} (M)	22.579 MHz	44.1 kHz x 512
	f_{03} (H)	24.576 MHz	48 kHz x 512

Package



M3 Series (D001) General Purpose SAW Voltage Controlled Oscillators

The M3 series (D001) voltage controlled oscillators (VCO) operate in the frequency range of 50 to 300 MHz. They use a single lithium tantalate ($LiTaO_3$) SAW resonator. The M3 series VCOs oscillate directly in the VHF band up to 300 MHz and have a wide variable frequency range and high temperature stability.

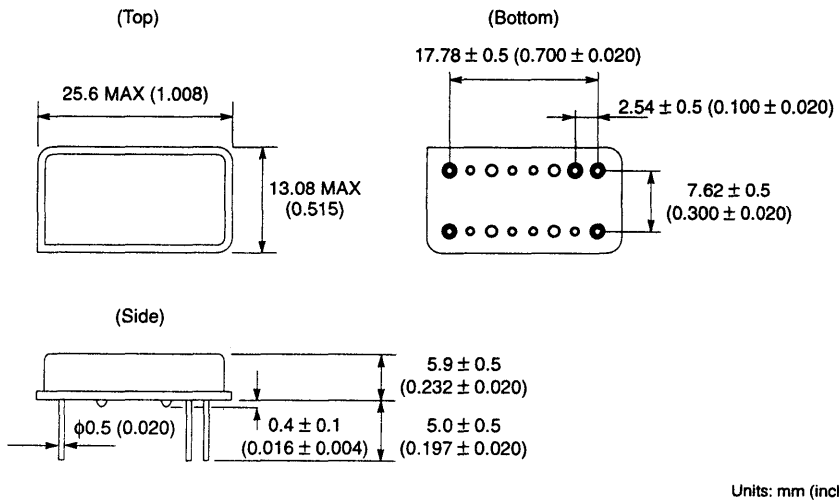
- Direct oscillation at high frequencies: 50 to 300 MHz
- Wider variable frequency range: 800 ppm/V or more (0.5 to 4.5 V)
- Superb temperature characteristics: ±200 ppm (0 to 60°C) or less
- High-precision oscillation frequency, ready for use without adjustment
- High reliability due to hermetically sealed package
- High carrier noise ratio: –90 dB or less (12.5 kHz detuning, 8 kHz band)
- Frequency offset by built–in offset terminal
- Package: 5 pin metal case compatible with 16 pin DIP IC package

Standard Frequencies

Frequency	Application	Part Number
74.25 MHz	Professional HDTV	M3DA–74M250–D001
97.20 MHz	Transmission Standard HDTV	M3DA–97M200–D001
115.52 MHz	Broad–band ISDN	M3DA–155M52–D001

Package

Metal Case DIP 16



Units: mm (inches)

M3 Series (D101) SAW Modulators

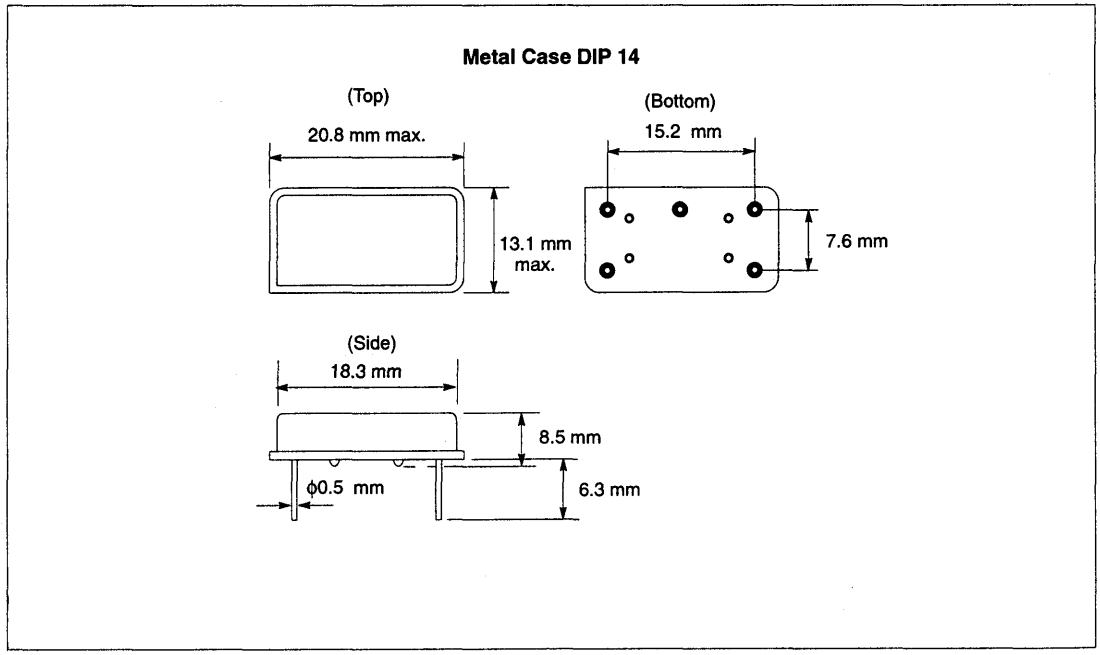
The M3 series (D101) SAW modulators contain direct oscillators (50 MHz to 300 MHz). They use a single lithium tantalate ($LiTaO_3$) SAW resonator. The M3 series modulators can be used in direct modulation applications requiring high modulation sensitivity and a high signal to noise ratio in the VHF band (up to 300 MHz)

- High frequency direct modulation: 50 to 300 MHz
- High modulation sensitivity: 800 ppm/V min. (0.5 to 4.5 V)
- Excellent modulation distortion ratio: 40 dB max. (1 kHz to 1.75 kHz dev.)
- Excellent signal to noise ratio: –50 dB max.
- Excellent temperature characteristic: + 200 ppm max. (–20 to 70°C)
- Highly reliable hermetically sealed package
- Package: 5 pin metal case compatible with 14 pin DIP IC package

Standard Frequency

Standard Frequency	Application	Part Number
145.0 MHz	Mobile Phone	M3DA–145M00–D101

Package



MB3802 — Power Management Switch

- Enhance PC Notebook Battery Life With This Power–saving Switch

The notebook PC typifies the recent trend in electronic devices towards compact, lightweight, battery-driven products that can be used anywhere, anytime. Use of this IC facilitates the contribution to the "green computer."

A major problem with such battery-driven devices is brief or insufficient battery life. This has focused attention on the issues of reducing power consumption and simultaneously extending battery life. Notebook PCs and other small computers switch off power to peripheral devices (hard or floppy disk drives, PCMCIA Cards, etc.) that are not operating. The circuits that control the switches, however, are either 3V or 5V circuits and operate constantly, consuming energy.

To control power lines to peripheral devices, FUJITSU has developed the MB3302 low-voltage input switch (V_{IN} > 2.2V typ.), which consumes no current when the switches are turned off.

MB3807A – Flash Memory Power Management Switch

Fujitsu has specifically developed the MB3807A to efficiently control Flash Memory devices, however it is also ideally suited for power control of other battery powered portable applications. The MB3807A consists of two SPDT switches, with each switch consisting of one pole suited for higher current requirements (.5 Amps) at typically 12 Volts and the other pole suited for lower current requirements (.1 Amps) typically from 3/5 Volt sources.

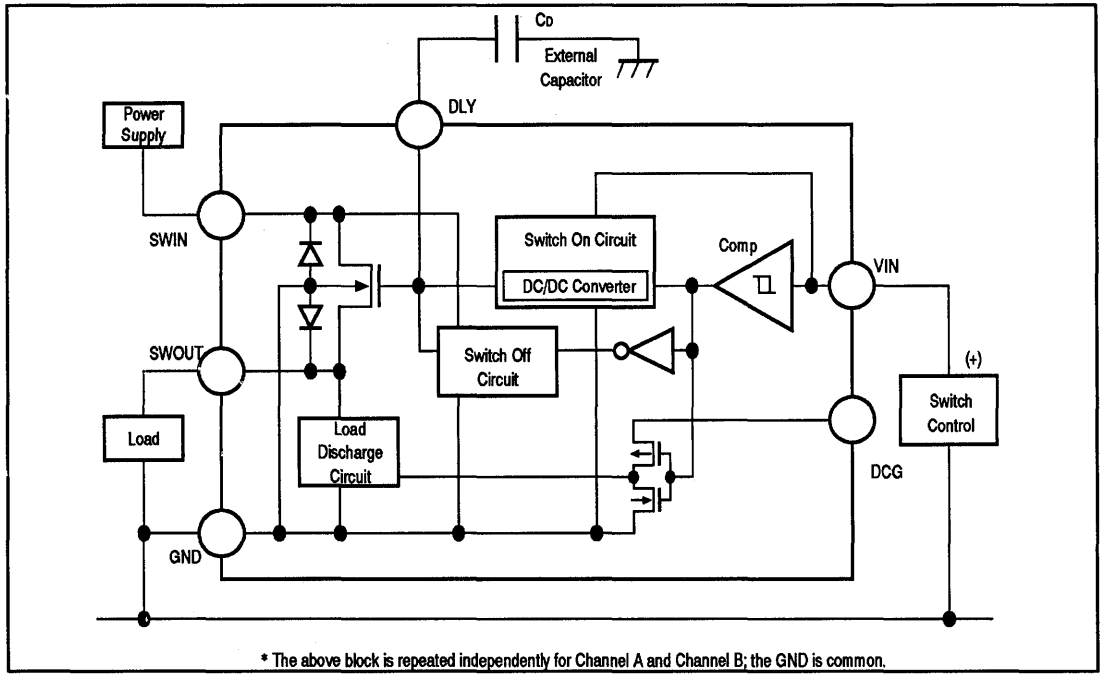
MB3802 – Power Management Switch

- Controls power lines to peripheral devices
- Greatly extends use of battery-driven notebook PCs
- Operates on low input voltage, ideal for use in 3V systems
- Low On Resistance : 120mΩ x 2 channels
  (Power NMOS FET Included)
- Low Leak Current : < 1 μA (Both Directions)
- Small Supply Current : ON State 100 μA
  OFF State 0 μA
- Low Control Voltage : 2.5V ~ 6V
- Rush Current Protection
- Small Package : Narrow SOP16

Product Line-up – Power Management Switches

Part Number	Number of Channels	ON Resistance	Handling DC Current	Handling Voltage	Switch Mode	Applications
MB3802	2	0.12 Ω	1.2A	< 7V	SPST	Notebooks Laptops Handhelds Portables PCMCIA Cards
MB3807A	2	0.3 Ω 6 Ω	0.5A 0.1A	< 15V	SPDT	Flash Memory PCMCIA Cards

MB3802 Block Diagram and External Connections



* The above block is repeated independently for Channel A and Channel B; the GND is common.

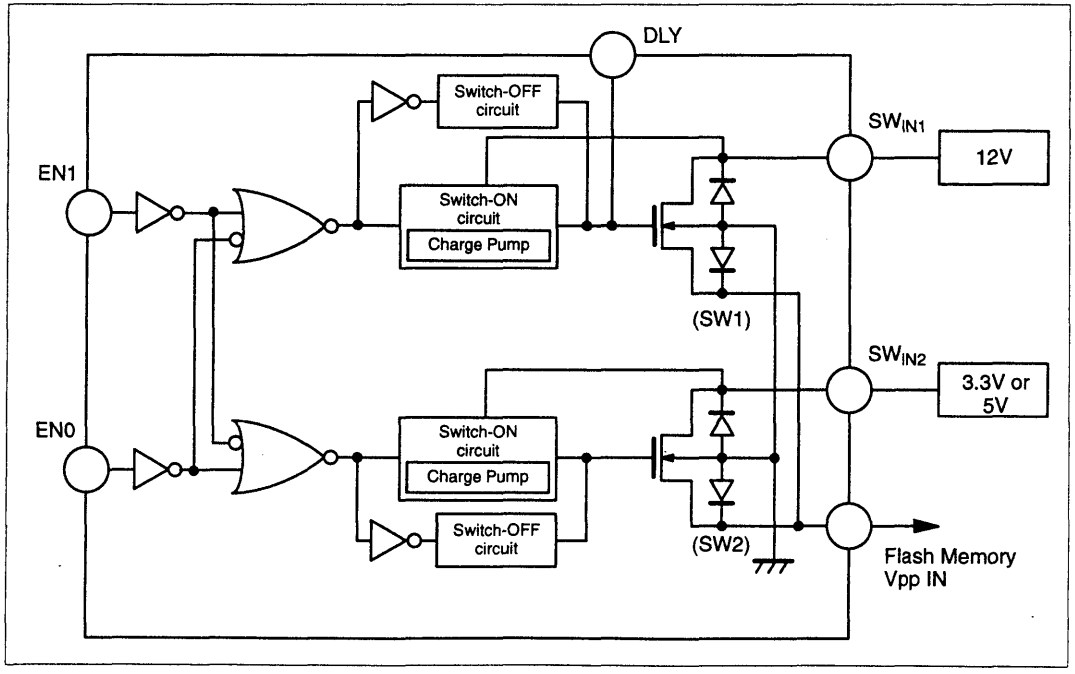
MB3807A – Power Management Switch for Flash Memory

- Power Management Switch for Flash Memory
- Compatibility for a PCMCIA Digital Interface
- Controls Two PCMCIA Card Slots
- Low On Resistance : 12V Port 0.3Ω
  5V Port 6Ω
- 5V Port Supports 3.3V and 5V Operation
- Small Package : Narrow SOP16

Product Line-up – Power Management Switches

Part Number	Number of Channels	ON Resistance	Handling DC Current	Handling Voltage	Switch Mode	Applications
MB3802	2	0.12 Ω	1.2A	< 7V	SPST	Notebooks Laptops Handhelds Portables PCMCIA Cards
MB3807A	2	0.3 Ω 6 Ω	0.5A 0.1A	< 15V	SPDT	Flash Memory PCMCIA Cards

MB3807A Block Diagram and External Connections



POWER MANAGEMENT DEVICES

SECTION 2

Prescalers – *At a Glance*

2

Fujitsu offers a wide range of prescaler devices capable of satisfying the technical requirements of today's applications. Features include devices covering the 200 MHz to 2.7 GHz range, low power consumption, and a multitude of divide ratios.

Page Number	Device Part Number	f_{IN} (max)	Divide Ratio	I_{CC} (typ)	V_{CC}	Package
2-3	MB501L	1.1 GHz	64/65, 128/129	10 mA	5 V	8-pin, DIP, SOP
2-15	MB501LV	1.1 GHz	64/65, 128/129	12 mA	3 V	8-pin, DIP, SOP
2-25	MB501SL	1.1 GHz	64/65, 128/129	5 mA	5 V	8-pin, DIP, SOP
2-3	MB504	520 MHz	32/33, 64/65	10 mA	5 V	8-pin, DIP, SOP
2-3	MB504L	520 MHz	32/33, 64/65	5 mA	5 V	8-pin, DIP, SOP
2-15	MB504LV	520 MHz	32/33, 64/65	6 mA	3 V	8-pin, DIP, SOP
2-35	MB505–16	1.6 GHz	128, 256	9 mA	5 V	8-pin, DIP, SOP
2-39	MB506	2.4 GHz	64, 128, 256	18 mA	5 V	8-pin, DIP, SOP
2-43	MB507	1.6 GHz	128/129, 256/257	18 mA	5 V	8-pin, DIP, SOP
2-51	MB508	2.3 GHz	128/129, 256/257	24 mA	5 V	8-pin, DIP, SOP
2-59	MB509	1.1 GHz	64/65, 128/129	12 mA	5 V	8-pin, DIP, SOP
2-67	MB510	2.7 GHz	128/144, 256/272	10 mA	5 V	8-pin, DIP, SOP
2-73	MB511	1.0 GHz	1, 2, 8	23 mA	5 V	8-pin, DIP, SOP
2-81	MB551	1.0 GHz	128/129	16 mA	5 V	8-pin, SOP

August 1995
Edition 6.0b

FUJITSU

DATA SHEET

MB501L/504/504L

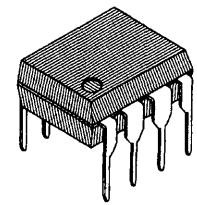
TWO MODULUS PRESCALERS

2

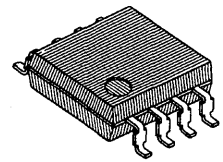
TWO MODULUS PRESCALERS

The Fujitsu MB501L/504/504L are two modulus prescalers, which are use with a frequency synthesizer to make a PLL (Phase Locked Loop). They will divide the input frequency by the modulus of 64/65 or 128/129 for the MB501L, and 32/33 or 64/65 for the MB504/MB504L. The MB501L and MB504L are low-power versions. The output of 1.6V peak to peak on ECL level applies to all.

- High Operating Frequency, Low Power Operation:
  1.1GHz at 50mW typ. (MB501L)
  520MHz at 50mW typ. (MB504)
  520MHz at 25mW typ. (MB504L)
- Pulse Swallow Function
- Wide Operation Temperature T_A = –40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6Vp-p
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package



PLASTIC PACKAGE
DIP-08P-M01



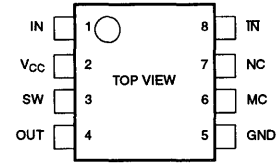
PLASTIC PACKAGE
FPT-08P-M01

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	V_O	10	mA
Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	– 55 to +125	°C

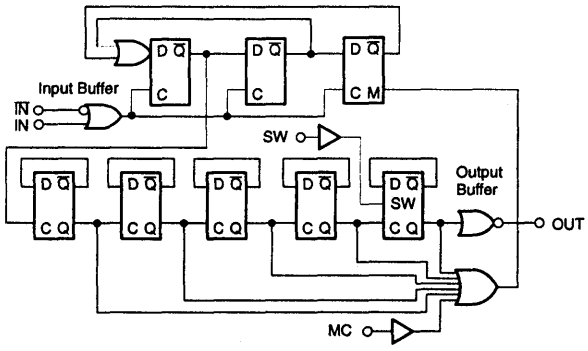
Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

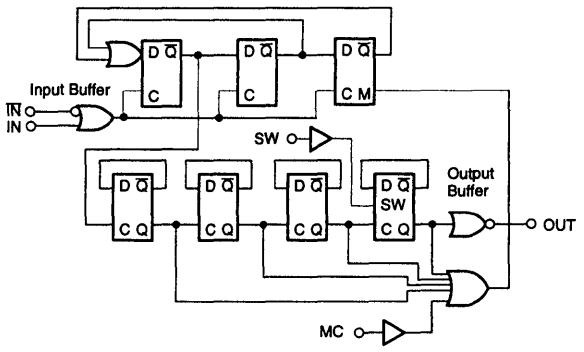
a) MB501L



	SW	MC	Divide Ratio
MB501/ MB501L	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = OPEN
MC: H = 2.0V to V_{CC},
L = GND to 0.8V

b) MB504/MB504L



	SW	MC	Divide Ratio
MB504/ MB504L	H	H	1/32
	H	L	1/33
	L	H	1/64
	L	L	1/65

Note: SW: H = V_{CC}, L = OPEN
MC: H = 2.0V to V_{CC},
L = GND to 0.8V

Figure 1. Block Diagrams

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS
(Recommended Operating Conditions unless otherwise noted)

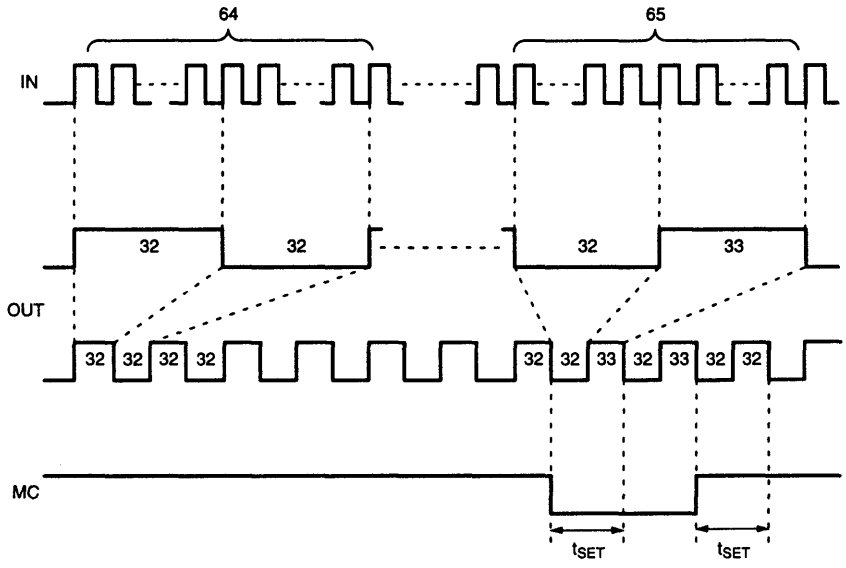
Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power Supply Current	MB501L	I_{CC}	I/O pins are open		10	14*	mA
	MB504				10	14*	mA
	MB504L				5	7*	mA
Output Amplitude		V_O		1.0	1.6		V_{P-P}
Input Frequency	MB501L	f_{IN}	With input coupling capacitor 1000pF	10		1100	MHz
	MB504			10		520	MHz
	MB504L			10		520	MHz
Input Signal Amplitude for IN	MB501L	P_{IN}		–4		5.5	dBm
	MB504			–12		10	dBm
	MB504L			–12		10	dBm
High Level Input Voltage for MC		V_{IHM}		2.0			V
Low Level Input Voltage for MC		V_{ILM}				0.8	V
High Level Input Voltage for SW		V_{IHS}**		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW		V_{ILS}		OPEN			V
High Level Input Current for MC		I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC		I_{ILM}	V_{IL} = 0.8V	–0.2			mA
Modulus Set-up Time MC to OUT	MB501L	t_{SET}			16	26	ns
	MB504				20	30	ns
	MB504L				18	28	ns

Note: * V_{CC} = 5V, T_A = 25°C
** Design Guarantee

2

MB501L TIMING CHART (2 MODULUS)

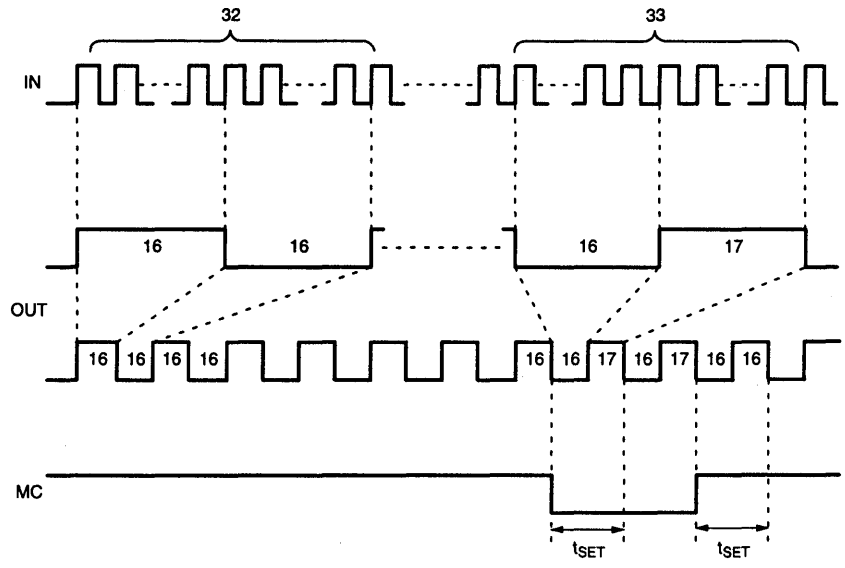
Example: Divide Ratio of 64/65



Note: When divide ratio of 65 is selected, positive pulse is applied by one to 33.
The typical set up time is 16ns (MB501L) from the MC signal input to the timing of change of prescaler divide ratio.

MB504/MB504L TIMING CHART (2 MODULUS)

Example: Divide Ratio of 32/33



Note: When divide ratio of 33 is selected, positive pulse is applied by one to 17.
The typical set up time is 20ns (MB504), 18ns (MB504L) from the MC signal input to the timing of change of prescaler divide ratio.

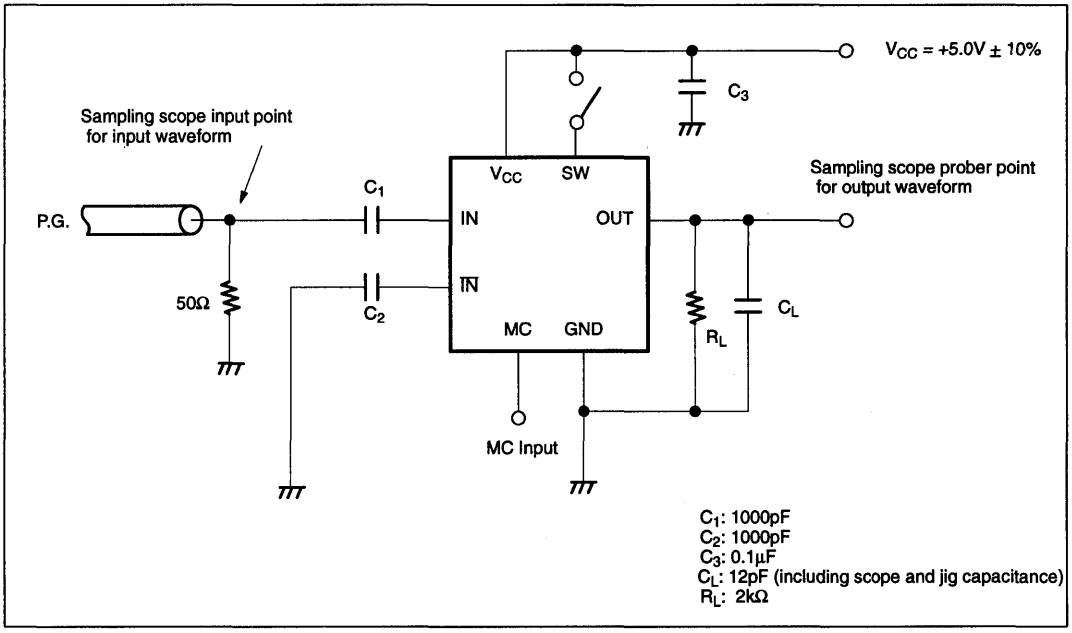


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS CURVES

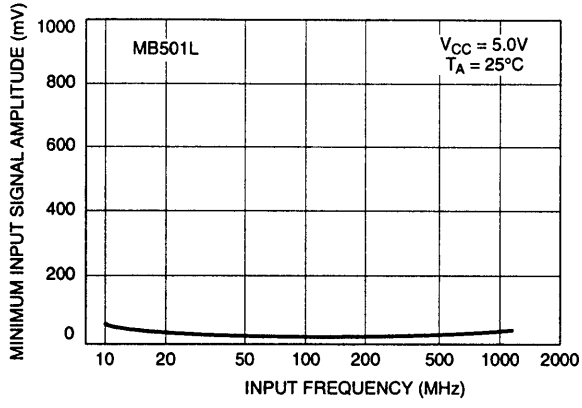


Figure 3. Input Signal Amplitude vs. Input Frequency

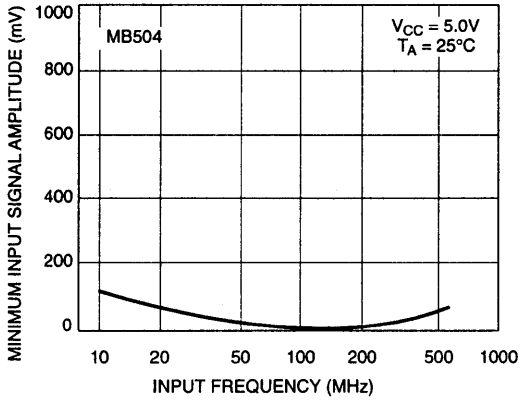


Figure 4. Input Signal Amplitude vs. Input Frequency

TYPICAL CHARACTERISTICS CURVES (Continued)

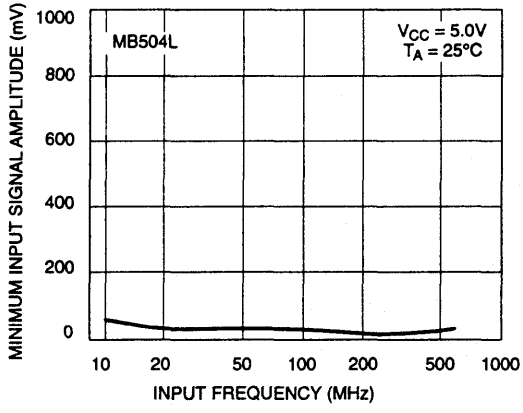
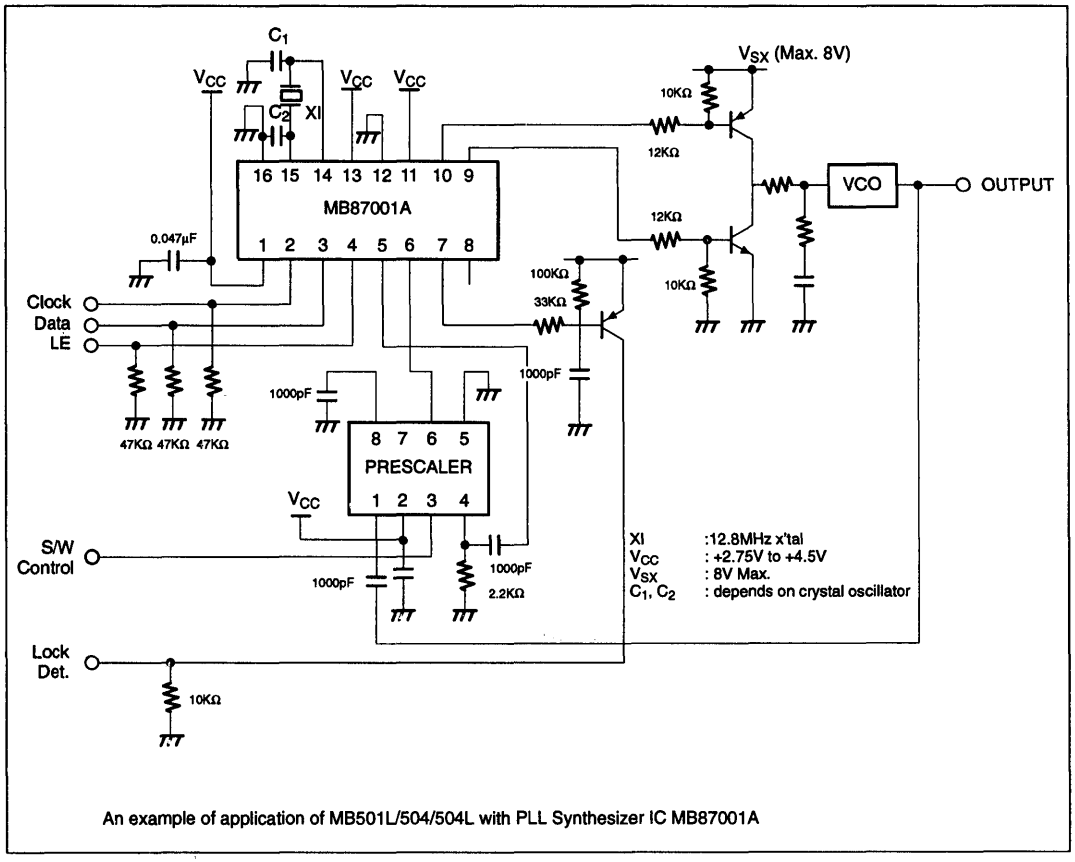


Figure 5. Input Signal Amplitude vs. Input Frequency



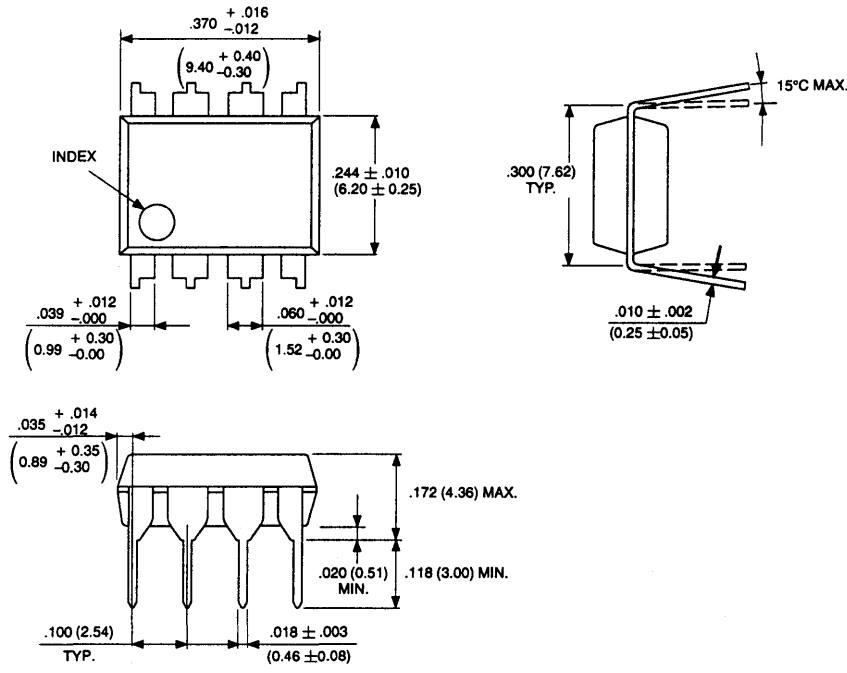
An example of application of MB501L/504/504L with PLL Synthesizer IC MB87001A

Figure 6. Typical Application Example

2

PACKAGE DIMENSIONS

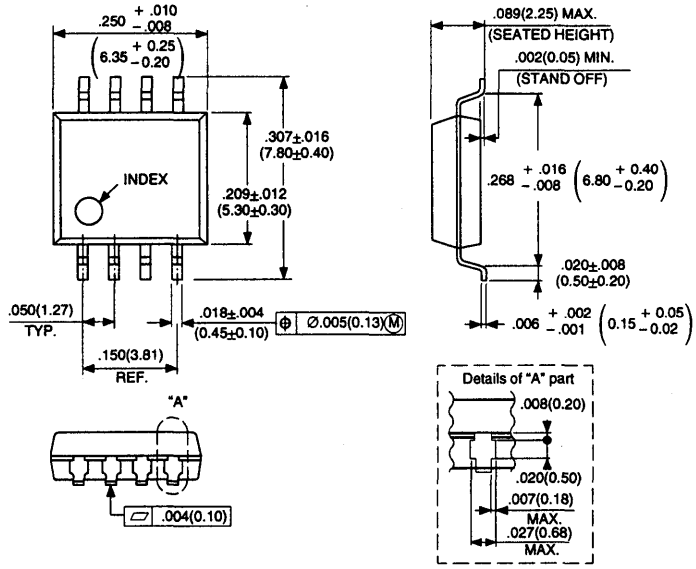
8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters).

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in inches (millimeters).

Sept. 1995
Edition 4.0a

FUJITSU

DATA SHEET

MB501LV/504LV

LOW VOLTAGE/LOW POWER TWO MODULUS PRESCALERS

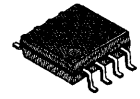
2

LOW VOLTAGE/LOW POWER TWO MODULUS PRESCALERS

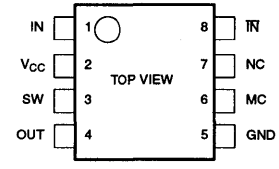
The Fujitsu MB501LV/504LV are low power and low voltage versions of MB501/504, two modulus prescalers used with a frequency synthesizer to make a Phase Locked Loop (PLL). They will divide the input frequency by the modulus of 64/65 or 128/129 for the MB501LV, and 32/33 or 64/65 for the MB504LV. The output level is 1.1V peak to peak on ECL level.

- Wide Low Voltage Operation 3.0V typ., +2.7 to 4.5V
- High Frequency Operation, Low Power Operation (V_{IN} = –12dBm min.)
  1.1 GHz at 36mW typ. (MB501LV)
  520MHz at 18mW typ. (MB504LV)
- Pulse Swallow Function
- Wide Operation Temperature T_A = –40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.1Vp-p typ.
- Built-in a termination resistor
  Stable output amplitude is obtained up to output load capacitance of 8pF.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01



ABSOLUTE MAXIMUM RATINGS (see NOTE)

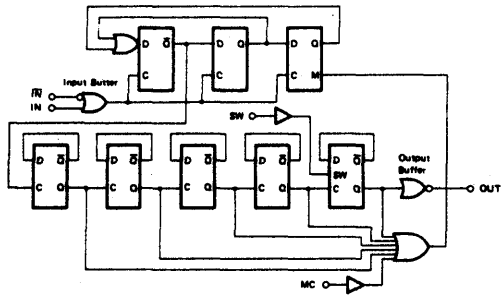
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to + V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	– 55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAMS

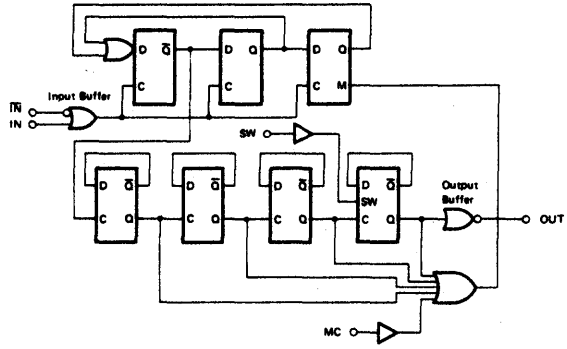
a) MB 501LV



SW	MC	Divide Ratio
H	H	1/64
H	L	1/65
L	H	1/128
L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{IHM} = \frac{1}{2}V_{CC} + 0.3V$

b) MB 504LV



SW	MC	Divide Ratio
H	H	1/32
H	L	1/33
L	H	1/64
L	L	1/65

Note: SW: H = V_{CC}, L = open
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{IHM} = \frac{1}{2}V_{CC} + 0.3V$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	2.7	3.0	4.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40	-	+85	°C
Load Capacitance	C_L			8	pF

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

ELECTRICAL CHARACTERISTICS
(Recommended Operating Conditions unless otherwise noted)

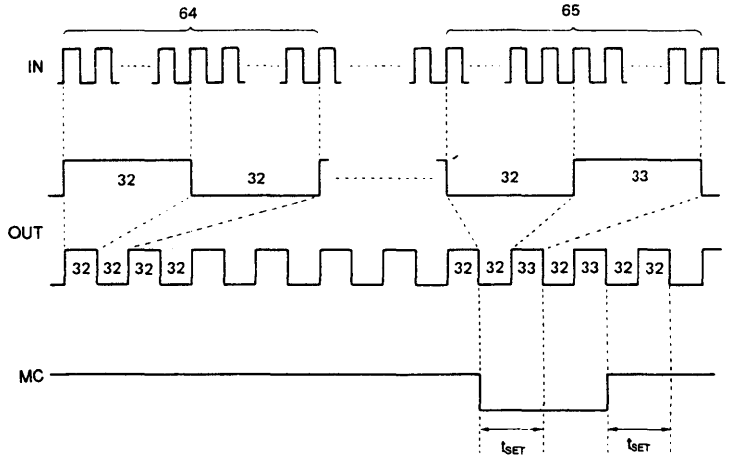
Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power Supply Current	MB501LV	I_{CC}	V_{CC} = 3.0V		12		mA
	MB504LV				6		mA
Output Amplitude		V_O		0.8	1.1		V_{P-P}
Input Frequency	MB501LV	f_{IN}	With input coupling capacitor 1000pF	10		1100	MHz
	MB504LV			10		520	MHz
Input Signal Amplitude		P_{IN}		−12		5.5	dBm
High Level Input Voltage for MC Input		V_{IHM}	$V_{IHM} = 1/2\ V_{CC} + 0.3$	V_{IHM}			V
Low Level Input Voltage for MC Input		V_{ILM}				0.8	V
High Level Input Voltage for SW Input		V_{IHS}*		V_{CC} −0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW Input		V_{ILS}		OPEN			V
High Level Input Current for MC Input		I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input		I_{ILM}	V_{IL} = 0.8V	−0.2			mA
Modulus Set-up Time MC to OUT	MB501LV	t_{SET}			16	26	ns
	MB504LV				18	28	ns

Note: * Design Guarantee

2

MB501LV TIMING CHART (2 MODULUS)

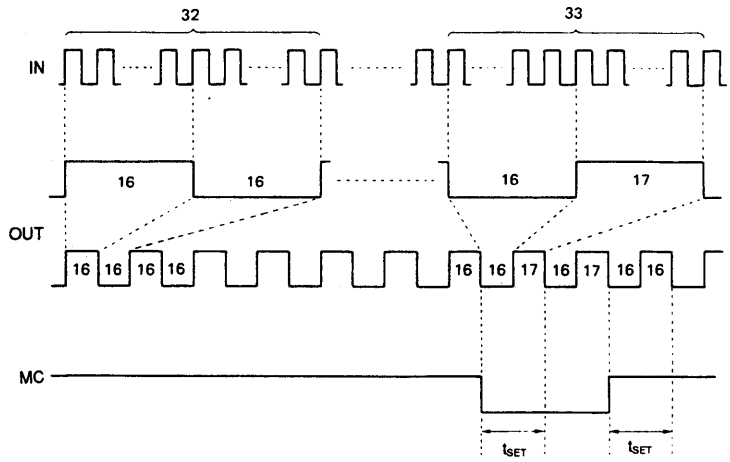
Example: Divide ratio = 64/65



Note: When divide ratio of 65 is selected, positive pulse is applied by one to 33.
The typical set up time is 16 ns from the MC signal input to the timing of change of prescaler divide ratio.

MB504LV TIMING CHART (2 MODULUS)

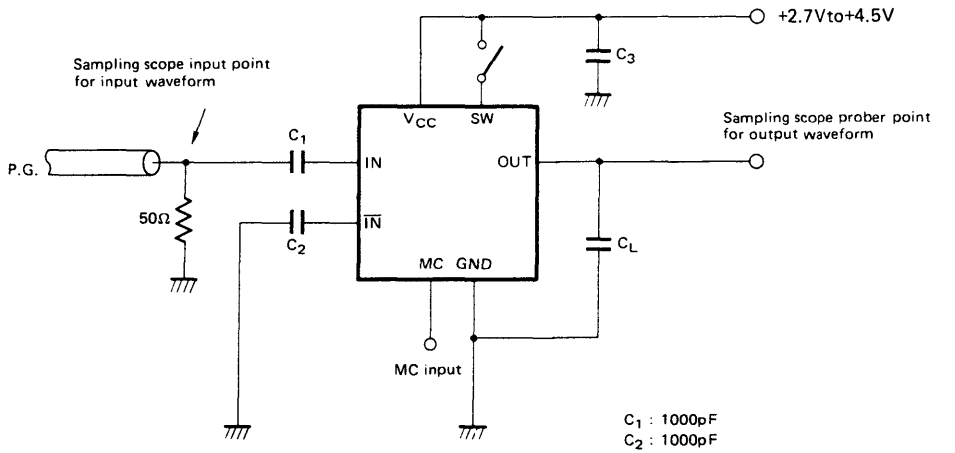
Example: Divide ratio = 32/33



Note: When divide of 33 is selected, positive pulse is applied by one to 17.
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.

2

Fig. 2 – TEST CIRCUIT



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

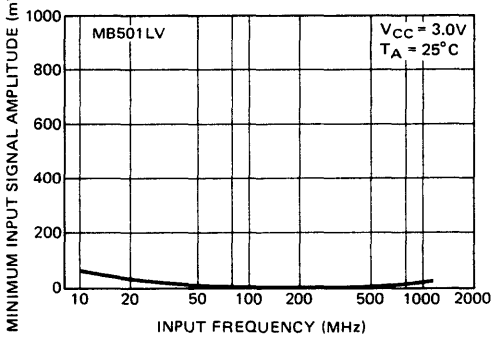


Fig. 4 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

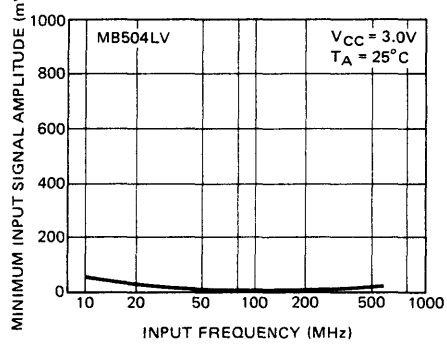
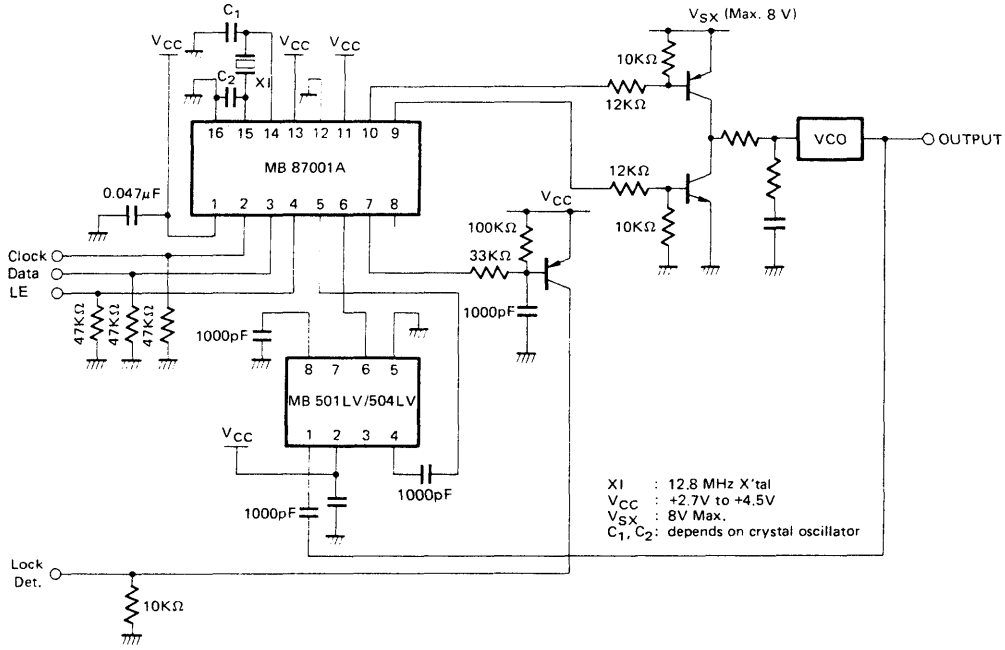


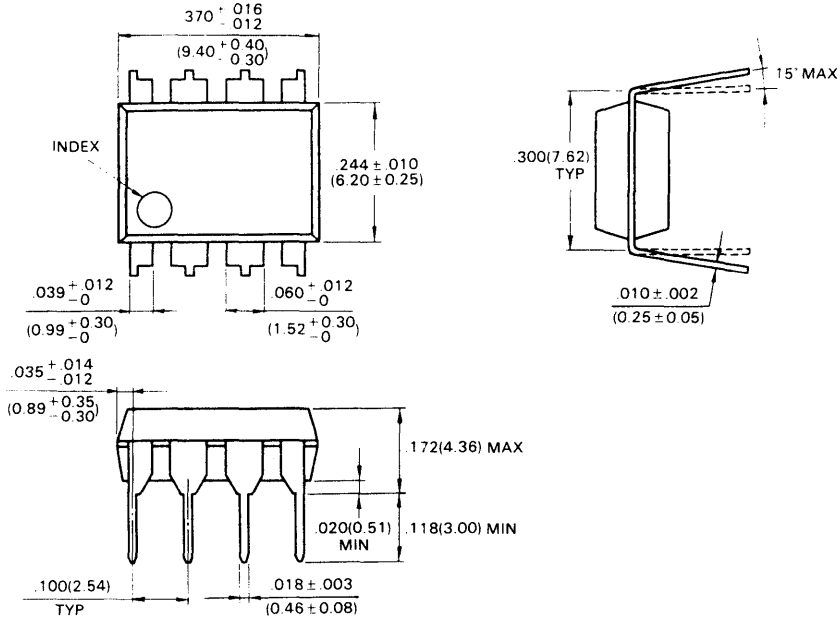
Fig. 5 – TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

2

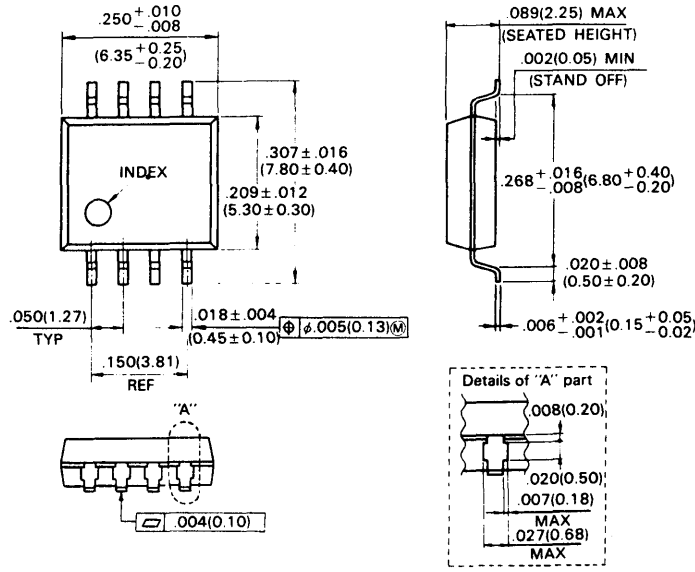
8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

Sept. 1995
Edition 3.0a

FUJITSU

DATA SHEET

MB501SL

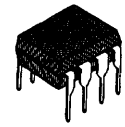
SUPER LOW POWER TWO MODULUS PRESCALER

2

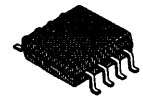
SUPER LOW POWER TWO MODULUS PRESCALER

The Fujitsu MB501SL is a super low power version of the MB501 two modulus prescaler used with a frequency synthesizer to make a Phase Locked Loop (PLL). It divides the input frequency by the modulus of 64/65 or 128/129, respectively. The MB501SL achieves extremely small stray capacitance by the use of Fujitsu's Advanced Process Technology. High speed operation is achieved with low power supply current of 5mA which is about half of the current value of the MB501L.

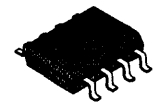
- High Frequency Operation: fmax = 1.1GHz max.(P_{IN} = −14bBm)
- Pulse Swallow Function: 64/65, 128/129
- Low Power Supply Current: 5.0mA typ.
- Stable Output Amplitude: V_O = 1.6Vp-p typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Dual-In-Line Package
- Plastic 8-pin Mini Flat Package
- Built-in Termination Resistor
- Stable output amplitude is obtained up to output load capacitance of 8pF.



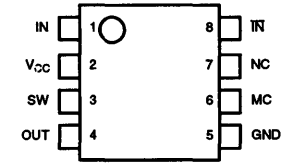
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01



PLASTIC PACKAGE
FPT-08P-M02



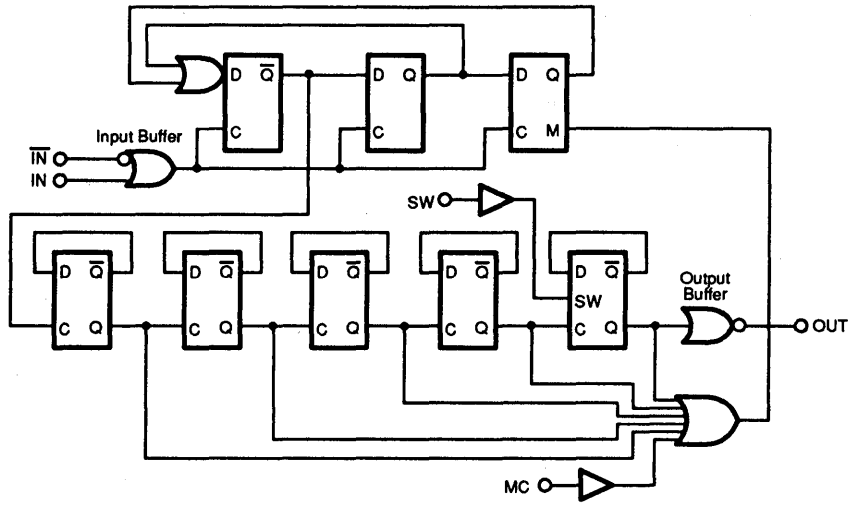
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to + V_{CC}	V
Output Voltage	I_O	10	mA
Storage Temperature	T_{STG}	− 55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB501SL BLOCK DIAGRAM



	SW	MC	Divide Ratio
MB501SL	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0V to V_{CC},
L = GND to 0.8V

PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	–40	—	+85	°C
Load Capacitance	CL	—	—	8	pF

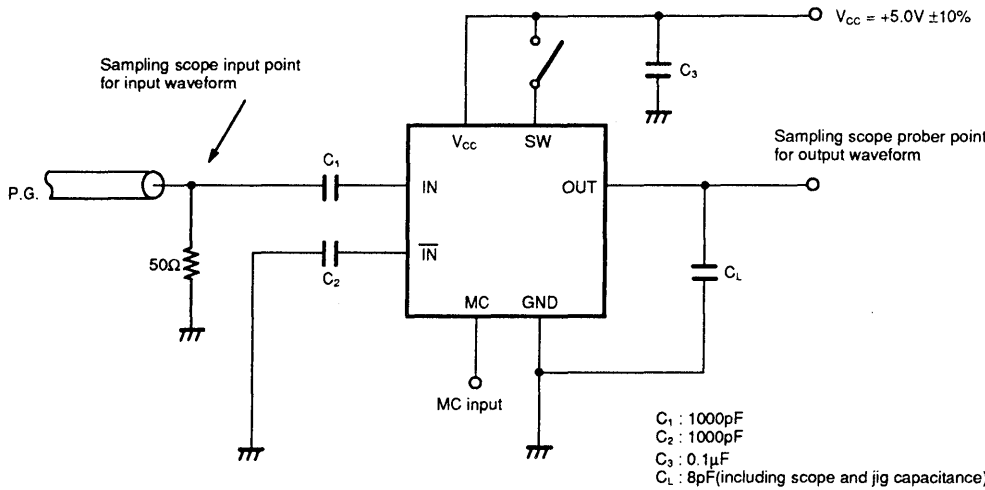
ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Power Supply Current	I_{CC}	—	—	5.0	7.0	mA
Output Amplitude	V_O	Built-in a termination resistor. Load capacitance = 8pF	1.0	1.6	—	V_{P-P}
Input Frequency	fin	With input coupling capacitor 1000pF	10	—	1100	MNz
Input Signal Amplitude	P_{IN}	—	–14	—	0	dBm
High Level Input Voltage for MC	V_{IHM}	—	2.0	—	—	V
Low Level Input Voltage for MC	V_{ILM}	—	—	—	0.8	V
High Level Input Voltage for SW	V_{IHS}*	—	V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW	V_{ILS}	—	OPEN			V
High Level Input Current for MC	I_{IHM}	V_{IH} = 2.0V	—	—	0.4	mA
Low Level Input Current for MC	I_{ILM}	V_{IL} = 0.8V	–0.2	—	—	mA
Modulus Set-up Time MC to Output	t_{SET}	—	—	16	26	ns

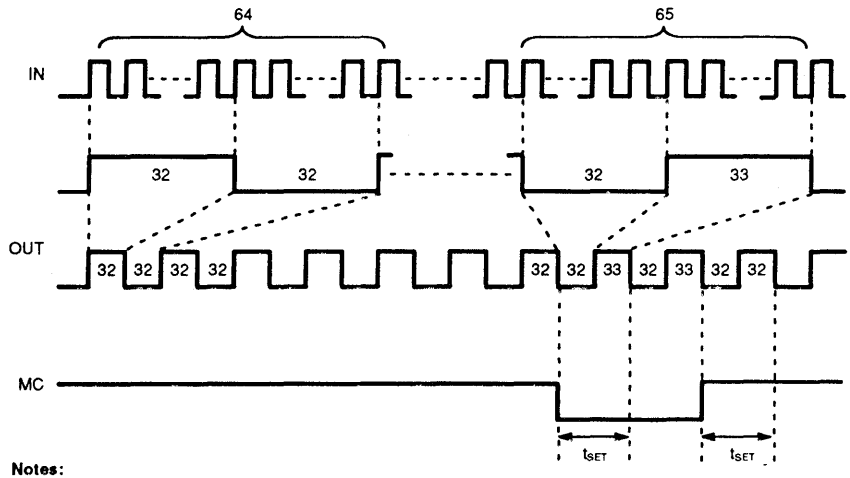
Note: * Design Guarantee

Fig. 2 –TEST CIRCUIT



TWO MODULUS OPERATING TIMING CHART

Example. Divide Ratio of 64/65



Notes:
When divide ratio of 129 is selected, positive pulse is added by one to 65.
The typical set up time(t_{SET}) is 16 ns from MC signal input to the timing of change of prescaler divide ratio.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

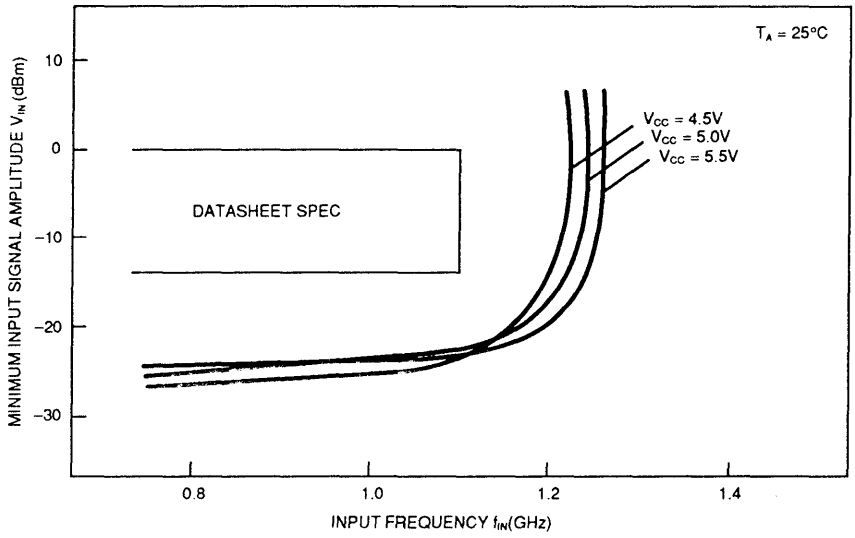


Fig. 4 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

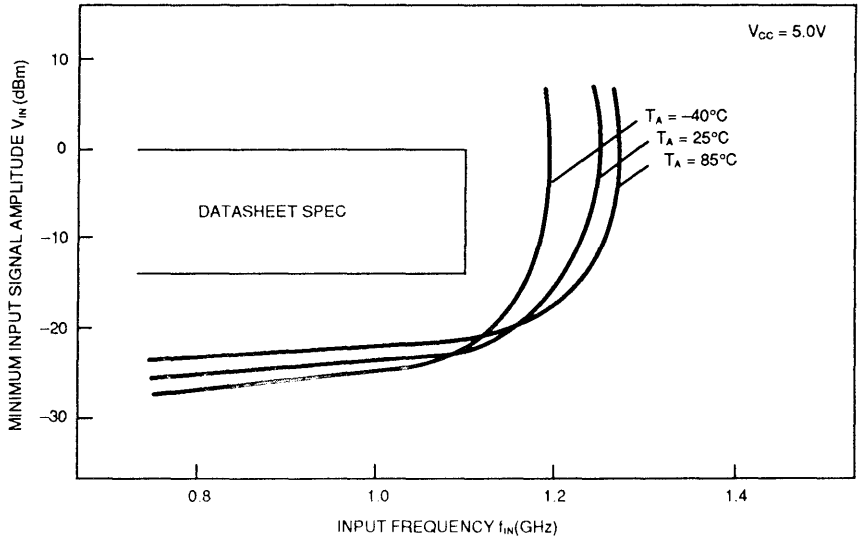


Fig. 5 – POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE

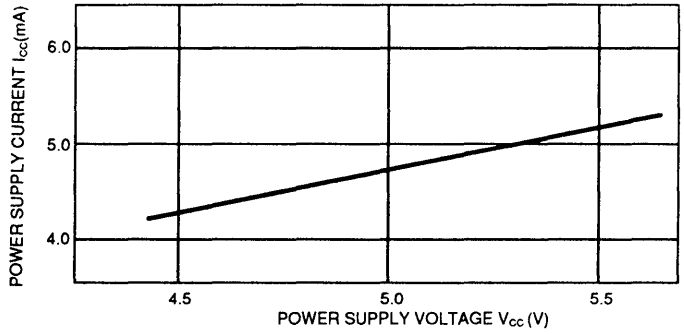


Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

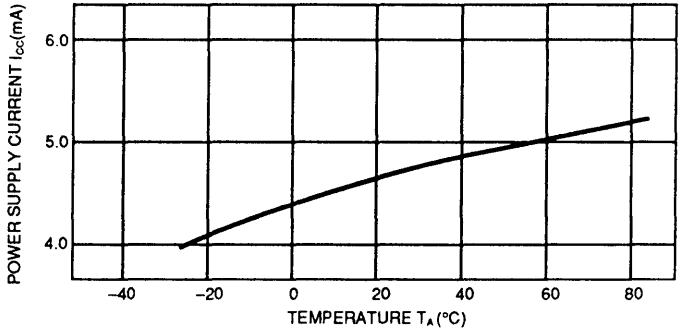


Fig. 7 – INPUT SIGNAL vs. INPUT FREQUENCY

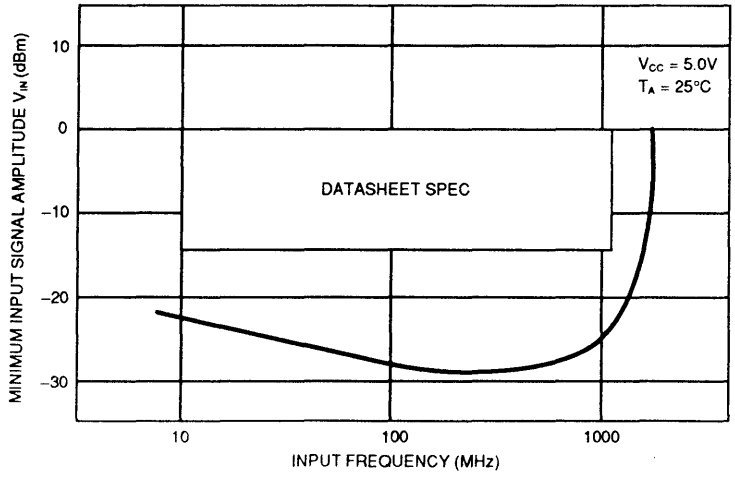
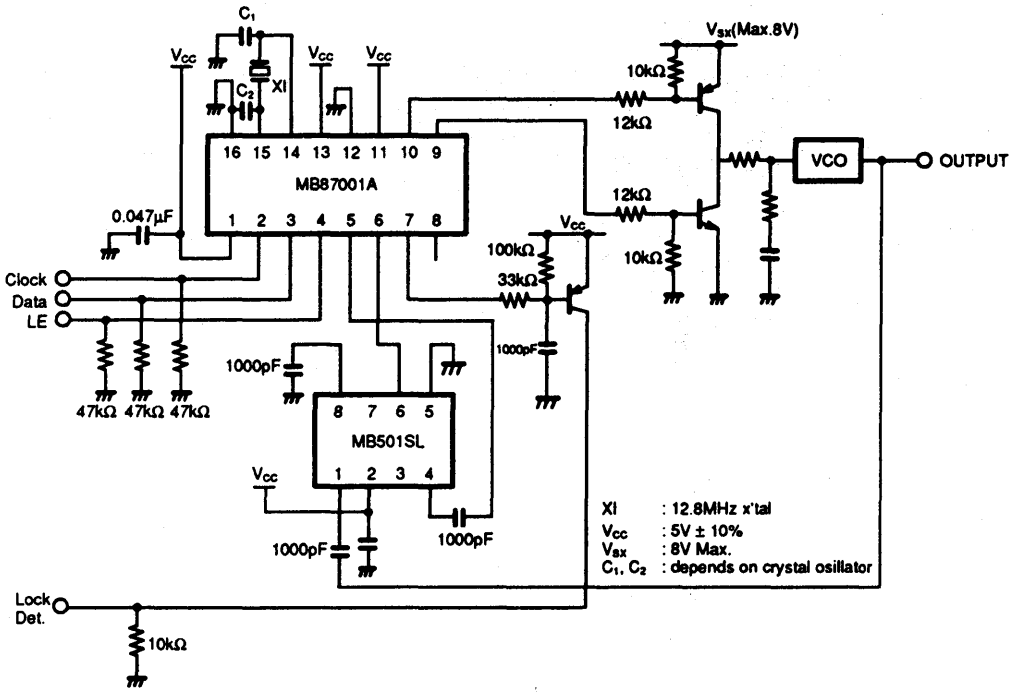
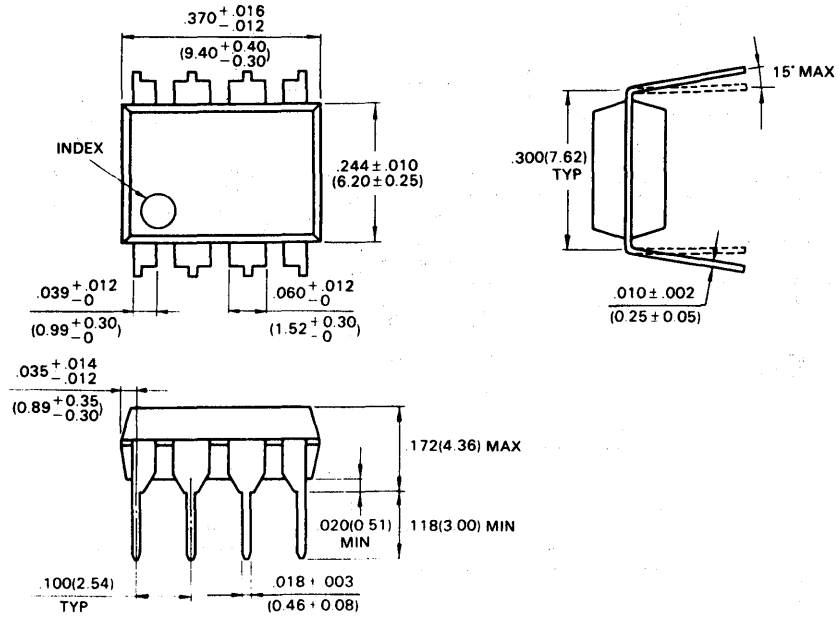


Fig. 8 –TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

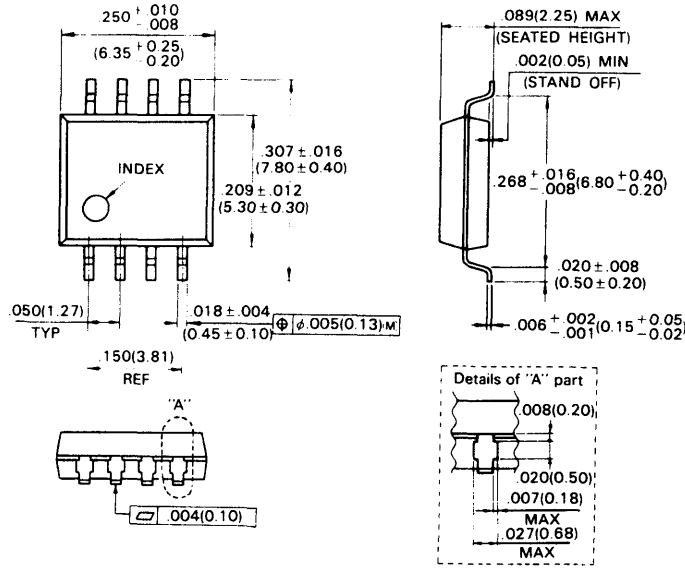
8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

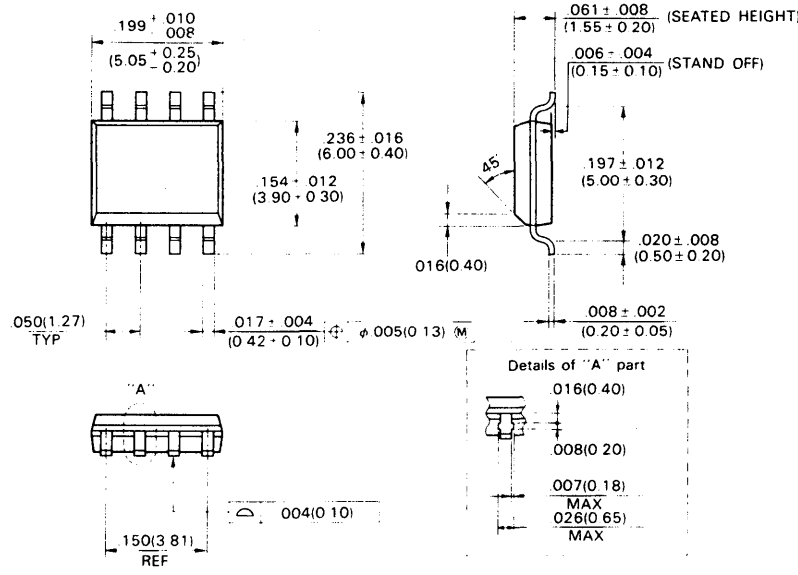
8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M02)



Dimensions in inches (millimeters)

Sept. 1995
Edition 4.0a

FUJITSU

DATA SHEET

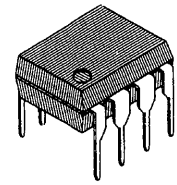
MB505-16
ULTRA HIGH FREQUENCY PRESCALER

2

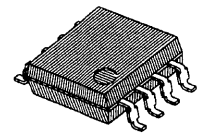
ULTRA HIGH FREQUENCY PRESCALER

The Fujitsu MB505 is a high frequency, up to 1.6GHz, prescaler used with a frequency synthesizer to form a Phase Locked Loop (PLL). It will divide the input frequency by the modulus of 128 or 256 and the cutput level is 1.6V peak to peak on ECL level.

Operation in the 1.6GHz range meets the specification for applications in Direct Broadcasting Satellite Systems (DBS), CATV systems, and UHF Transceivers.



PLASTIC PACKAGE
DIP-08P-M01

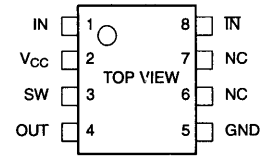


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation — 1.6GHz max.
- Low Power Dissipation — 45mW typ.
- Wide Operation Temperature — -40°C to +85°C
- Stable Output Amplitude — $V_{OUT} = 1.6V_{p-p}$
- Complete PLL synthesizer circuit with the Fujitsu MB87006A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or Flat Package

PIN ASSIGNMENT



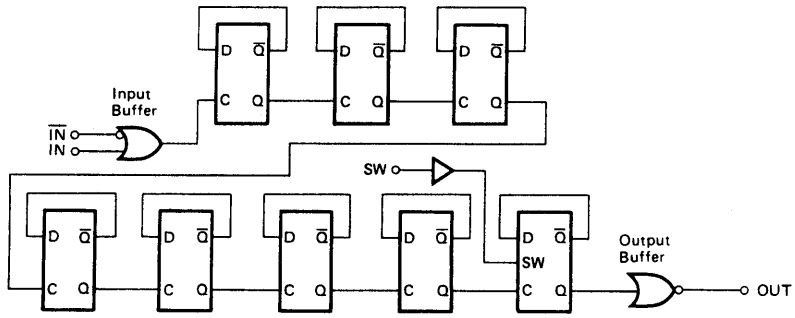
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 505 BLOCK DIAGRAM



SW	Divide Ratio
H	1/128
L	1/256

Note: SW: H = V_{CC}, L = open

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	Power Supply Voltage
3	SW	Divide Ratio Control Input Selecting divide ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	NC	No Connection
7	NC	No Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Curent	I_{CC}			9		mA
Output Amplitude	V_O		1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000pF	100		1600	MHz
Input Signal Amplitude	P_{IN}		–12		5.5	dBm
High Level Input Voltage for SW	V_{IHS}*		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW	V_{ILS}		Open			V

Note: *Design Guarantee

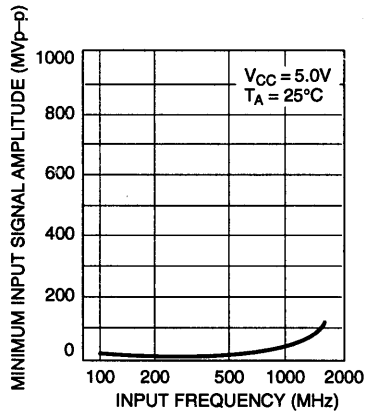
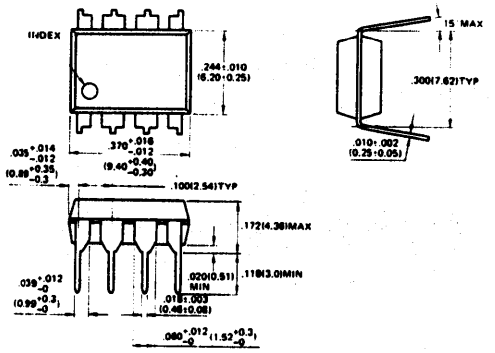


Figure 2. Input Signal Amplitude vs. Input Frequency

PACKAGE DIMENSIONS

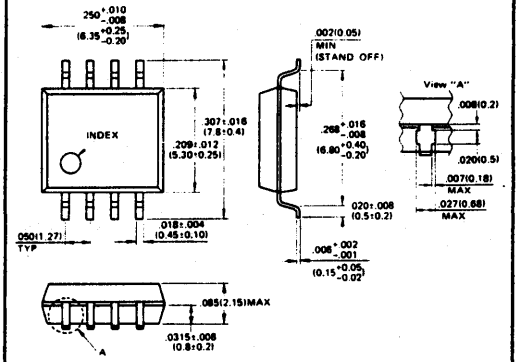
(Suffix: -P) (Suffix: -PF)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACJAGE
(CASE No.: FPT-08P-M01)



Dimensions in inches (millimeters)

Sept. 1995
Edition 3.0a

FUJITSU

DATA SHEET

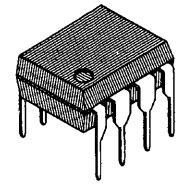
MB506

ULTRA HIGH FREQUENCY PRESCALER

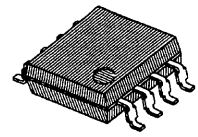
2

ULTRA HIGH FREQUENCY PRESCALER

The Fujitsu MB506 is a high frequency, up to 2.4GHz, prescaler used with a frequency synthesizer to form a Phase Locked Loop (PLL). It will divide the input frequency by the modulus of 128 or 256 and the output level is 1.6V peak to peak on ECL level.Operation in the 1.6GHz range meets the specification for applications in Direct Broadcasting Satellite Systems (DBS), CATV systems, and UHF Transceivers.



PLASTIC PACKAGE
DIP-08P-M01

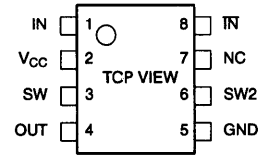


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation — 2.4GHz max.
- Power Dissipation — 90mW typ.
- Wide Operation Temperature — -40°C to +85°C
- Stable Output Amplitude — $V_{OUT} = 1.6V_{p-p}$
- Complete PLL synthesizer circuit with the Fujitsu MB87006A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or Flat Package

PIN ASSIGNMENT



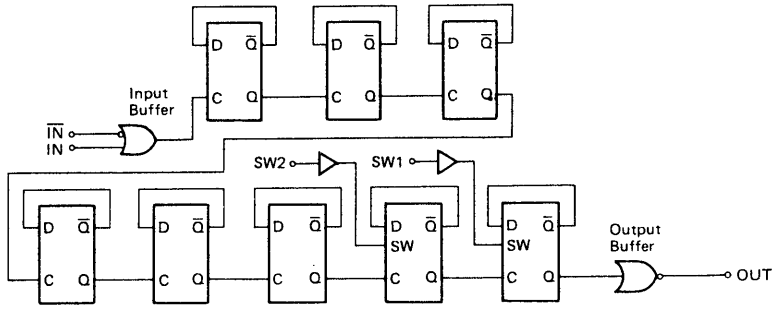
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 506 BLOCK DIAGRAM



SW1	SW2	Divide Ratio
H	H	1/64
L	H	1/128
H	L	1/128
L	L	1/256

Note: H = V_{CC}, L = open

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	Power Supply Voltage
3	SW1	Divide Ratio Control Input Selecting divide ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	SW2	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
7	NC	No Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Supply Curent	I_{CC}				18		mA
Output Amplitude	V_O			1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000pF	T_A = –40°C to 85°C	100		2200	MHz
			T_A = –40°C to 60°C	100		2400	
Input Signal Amplitude	P_{IN}	f_{IN} = 100MHz to 1.3GHz		–16		5.5	dBm
		f_{IN} = 1.3MHz to 2.4GHz		–4		5.5	
High Level Input Voltage for SW	V_{IHS}*			V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW	V_{ILS}			Open			V

Note: *Design Guarantee

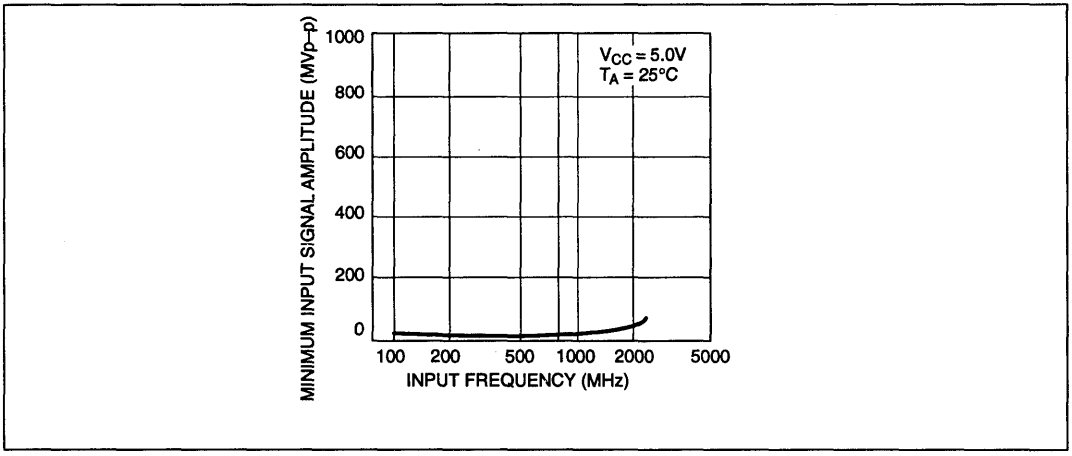
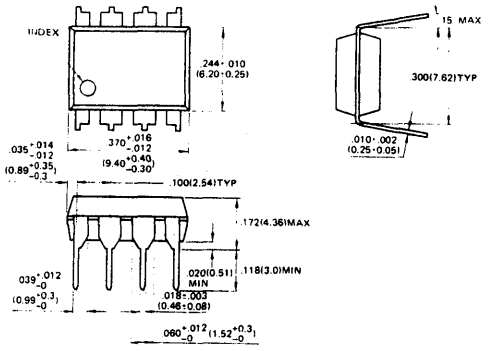


Figure 2. Input Signal Amplitude vs. Input Frequency

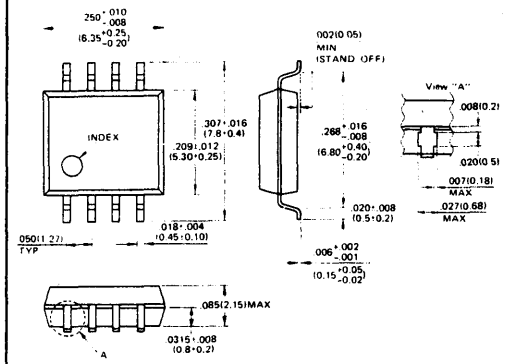
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACJAGE
(CASE No.: FPT-08P-M01)



Dimensions in inches (millimeters)

Sept. 1995
Edition 4.0a

FUJITSU

DATA SHEET

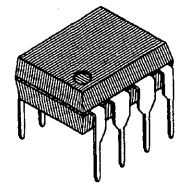
MB507

1.6GHz TWO MODULUS PRESCALER

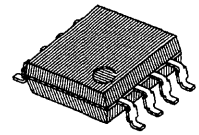
2

1.6GHz TWO MODULUS PRESCALER

The Fujitsu MB507 is a 1.6GHz two modulus prescaler used with a frequency synthesizer to form a Phase Locked Loop (PLL). It will divide the input frequency by the modulus of 128/129 or 256/257 and has an output level of 1.6V peak to peak on ECL level.



PLASTIC PACKAGE
DIP-08P-M01

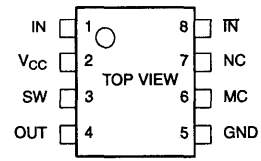


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation — 1.6GHz max.
- Power Dissipation — 90mW typ.
- Pulse Swallow Function
- Wide Operation Temperature — -40°C to +85°C
- Stable Output Amplitude — $V_{OUT} = 1.6V_{p-p}$
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Package
  Standard 8-pin Dual-In-Line Package (Suffix: –P)
  Standard 8-pin Flat Package (Suffix: –PF)

PIN ASSIGNMENT



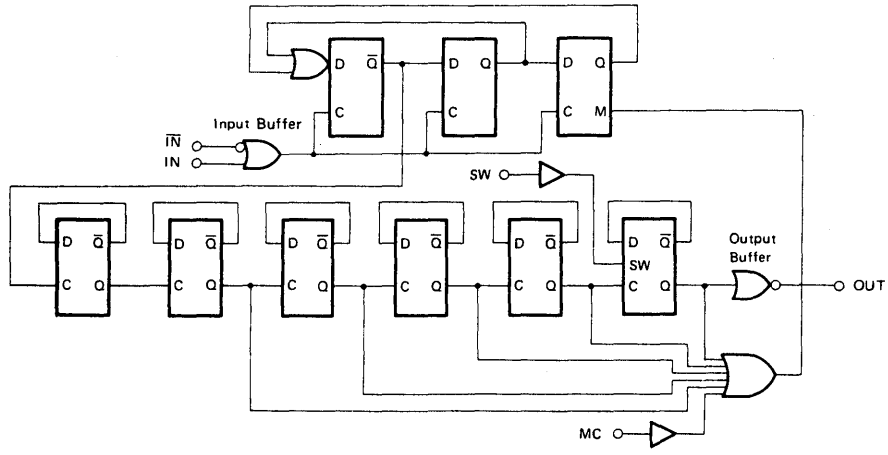
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditicns as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB507 BLOCK DIAGRAM



	SW	MC	Divide Ratio
MB 507	H	H	1/128
	H	L	1/129
	L	H	1/256
	L	L	1/257

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			12	pF

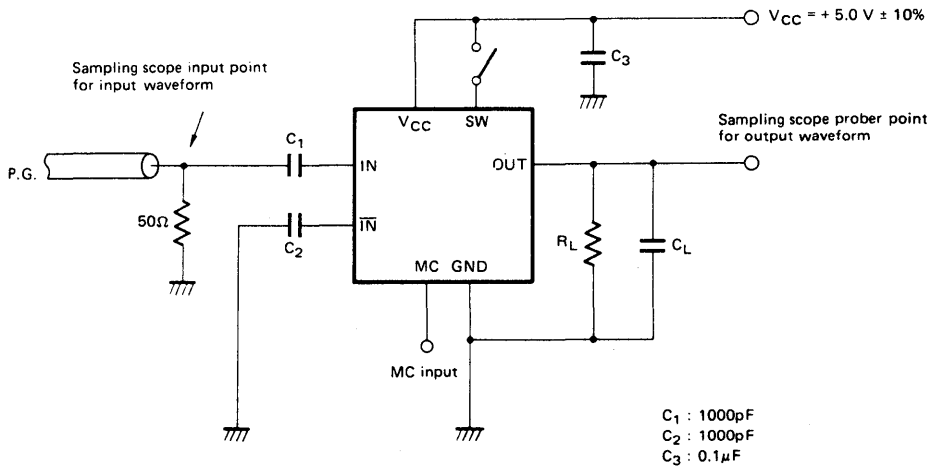
ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Curent	I_{CC}			18		mA
Output Amplitude	V_O		1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000pF	100		1600	MHz
Input Signal Amplitude	P_{IN}		–4		10	dBm
High Level Input Voltage for MC Input	V_{IHM}		2.0			V
Low Level Input Voltage for MC Input	V_{ILM}					V
High Level Input Voltage for SW Input	V_{IHS}*		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW Input	V_{ILS}			Open		V
High Level Input Current for MC Input	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input	I_{ILM}	V_{IL} = 0.8V	–0.2			mA
Modulus Set-up Time MC to OUT	t_{SET}	1.6GHz Operation		18	28	ns

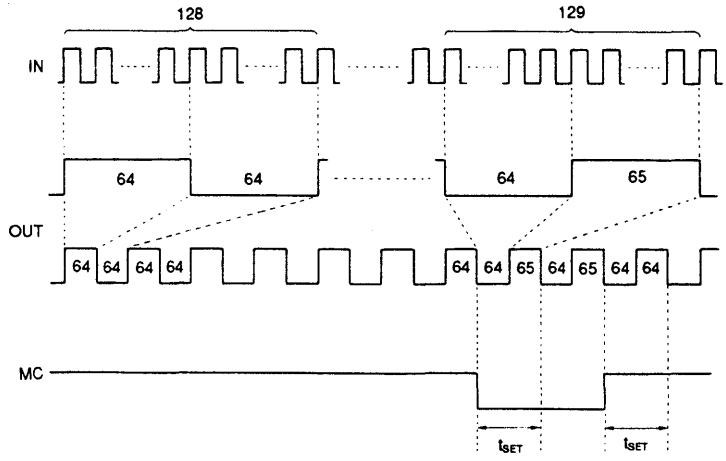
Note: *Design Guarantee

Fig. 2 – TEST CIRCUIT



TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/129



Note: When divide of 129 is selected, positive pulse is applied by one to 65.
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.

2

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

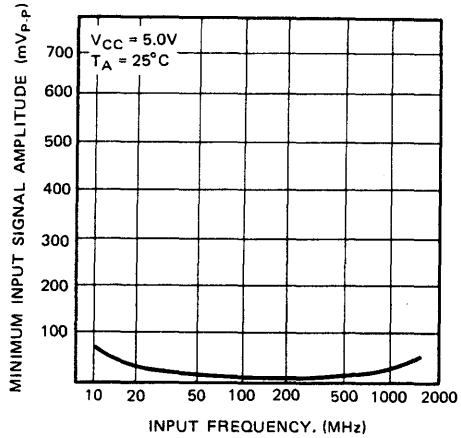
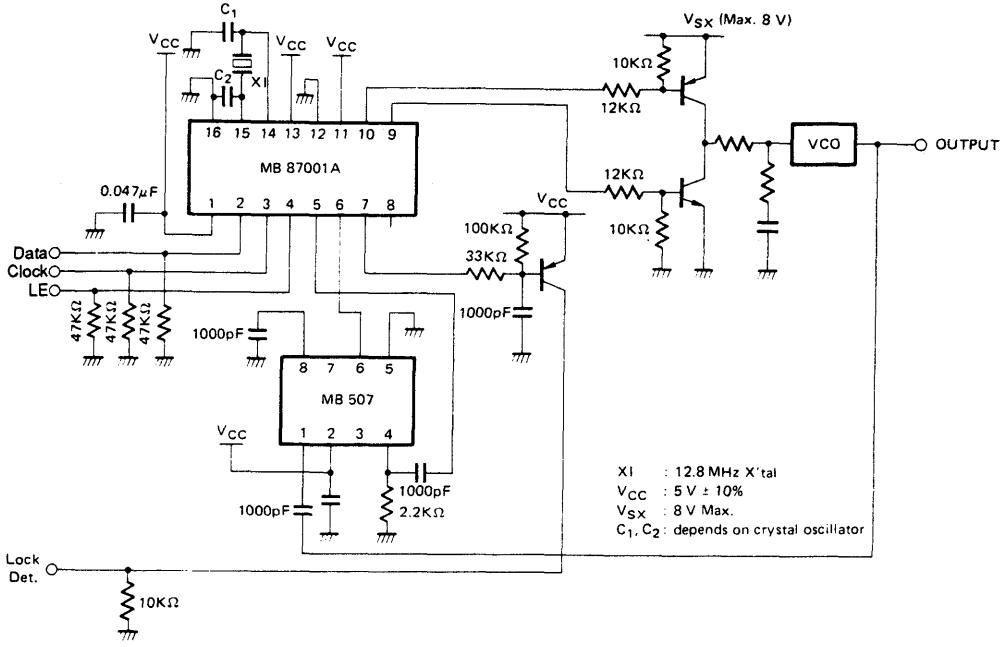


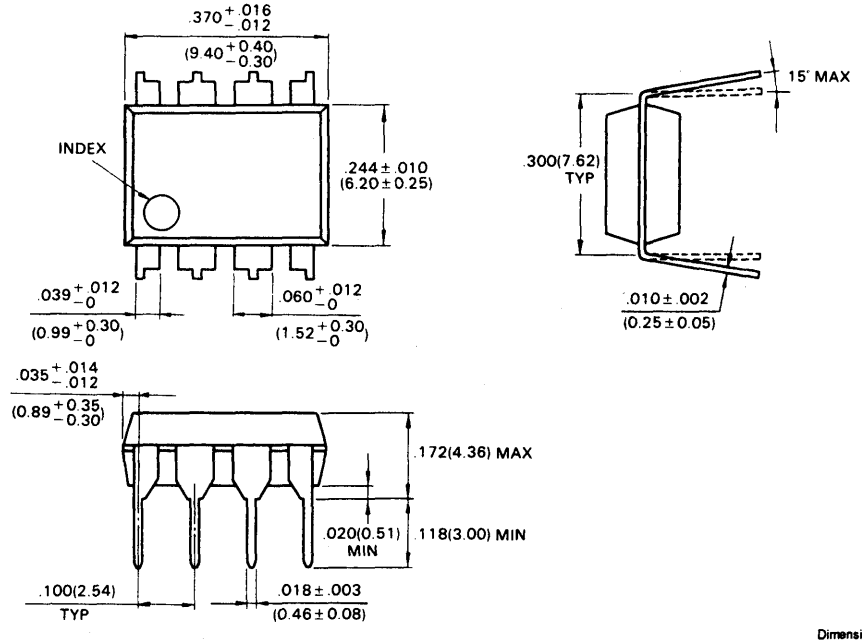
Fig. 4 – TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

(Suffix: P)

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



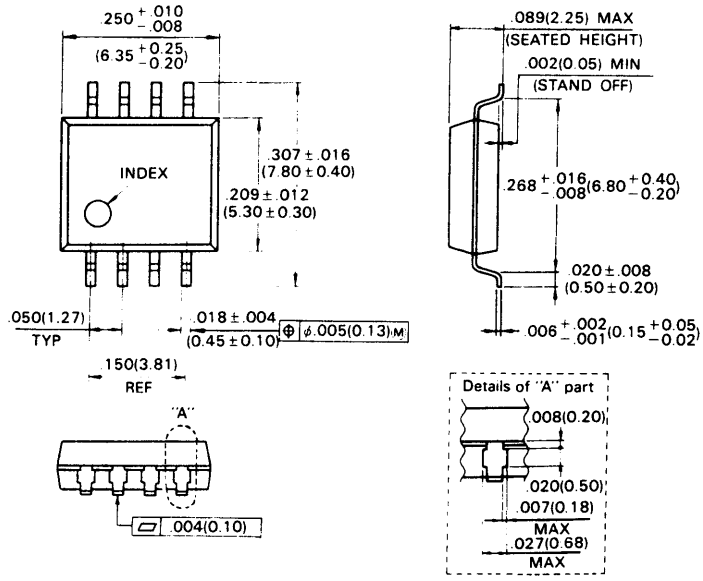
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PF)

2

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

Sept. 1995
Edition 3.0a

FUJITSU

DATA SHEET

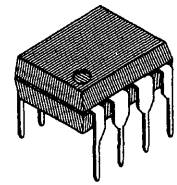
MB508

2.3GHz TWO MODULUS PRESCALER

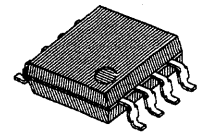
2

2.3GHz TWO MODULUS PRESCALER

The Fujitsu MB508 is a 2.3GHz two modulus prescaler used with a frequency synthesizer to form a Phase Locked Loop (PLL) and divides the input frequency by a modulus of 128/130, 256/258 or 512/514. The output level is 1.6V peak to peak ECL level. The ultra high frequency operation provides wide application, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.



PLASTIC PACKAGE
DIP-08P-M01

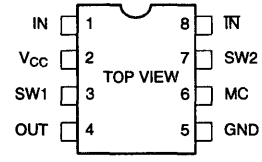


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation: f = 2.3GHz max. (P_{IN} = –4dBm min.)
- Input Signal Amplitude: V_{IN} = 100mV_{p-p} (f_{IN} = 100MHz to 1.8GHz)
- Pulse Swallow Function: 128/130, 256/258, 512/514
- Power Dissipation: 120mW typ.
- Wide Operation Temperature: -40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6V_{p-p} typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer system block IC
- Standard Plastic 8-pin Dual-In-Line Package or Flat Package

PIN ASSIGNMENT



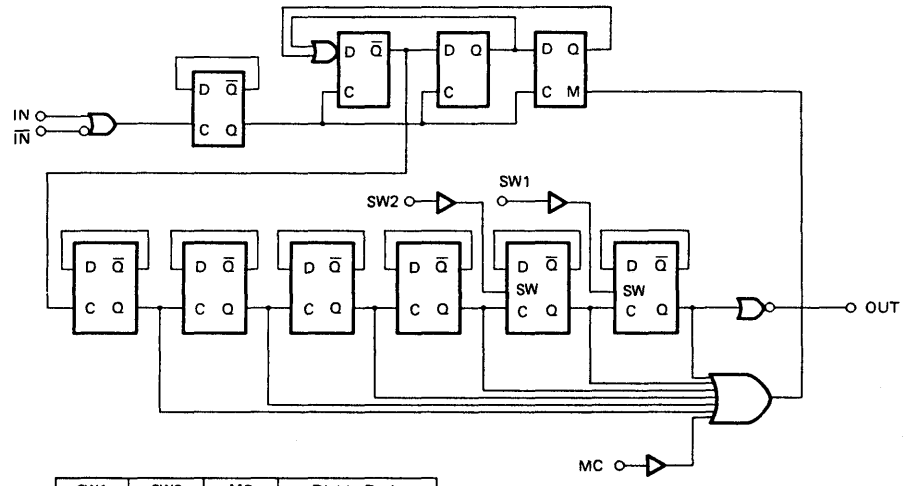
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB508 BLOCK DIAGRAM



SW1	SW2	MC	Divide Ratio
H	H	H	1/128
H	H	L	1/130
H	L	H	1/256
L	H	H	1/256
H	L	L	1/258
L	H	L	1/258
L	L	H	1/512
L	L	L	1/514

Note: SW: H=V_{CC}, L=Open
MC: H=2.0V to V_{CC}, L=GND to 0.8V

PIN DESCRIPTION

Pin Number	Symbol	Descriptions
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW1	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	SW2	Divide Ratio Control Input (See Divide Ratio Table)
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Operating Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			12	pF

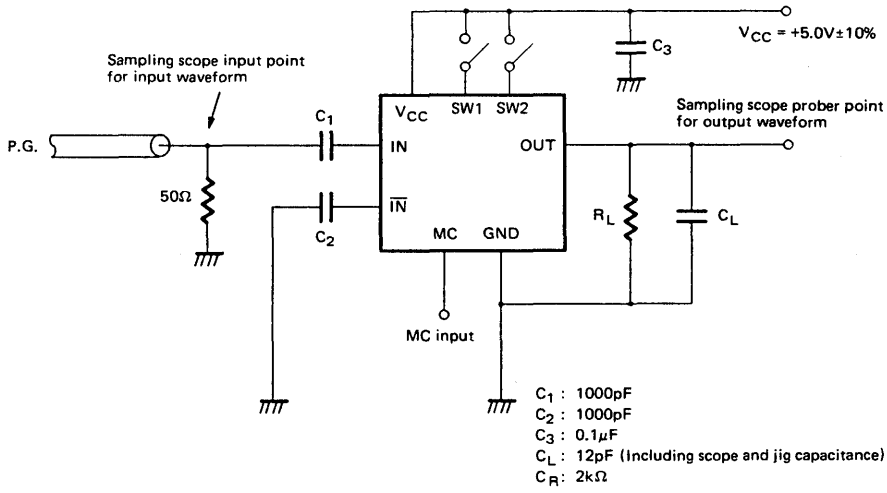
ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Power Supply Current	I_{CC}			24		mA
Output Amplitude	V_O		1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000pF	100		2300	MHz
Input Signal Amplitude	P_{INA}	f_{IN} = 1800MHz to 2300MHz	–4		5.5	dBm
	P_{INB}	f_{IN} = 100MHz to 1800MHz	–16		10	
High Level Input Voltage for MC	V_{IHM}		2.0			V
Low Level Input Voltage for MC	V_{ILM}				0.8	V
High Level Input Voltage for SW	V_{IHS}*		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW	V_{ILS}		Open			V
High Level Input Current for MC	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC	I_{ILM}	V_{IL} = 0.8V	–0.2			mA
High Level Input Current for SW	I_{IHS}	$V_{IH} = V_{CC}$			250	µA
Modulus Set-up Time MC to Output at 2.3GHz Operation	t_{SET}			18	28	ns

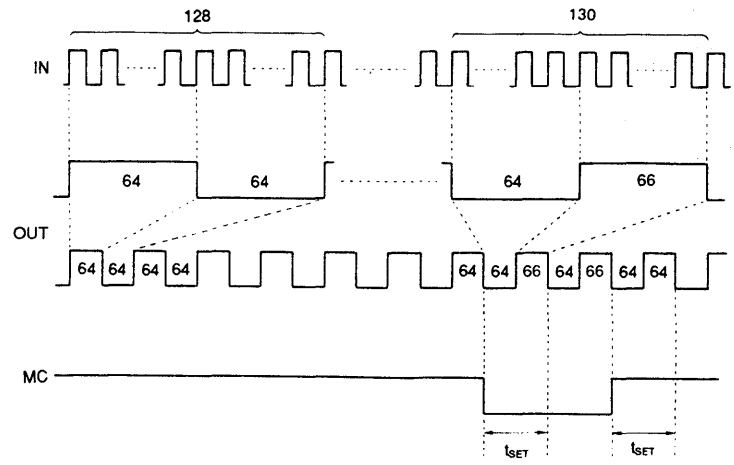
Note: *Design Guarantee

Fig. 2 – TEST CIRCUIT



TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/130



Note: When divide ratio of 130 is selected, positive pulse is applied by two to 66.
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.

2

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

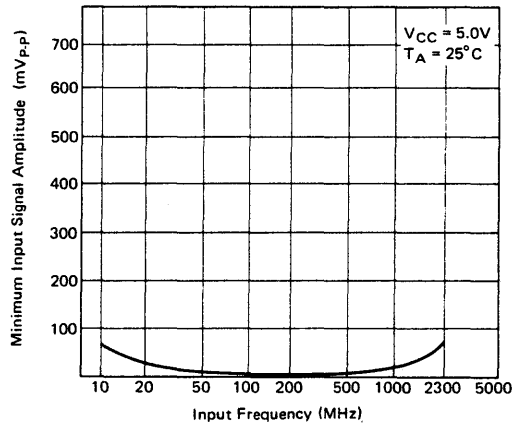
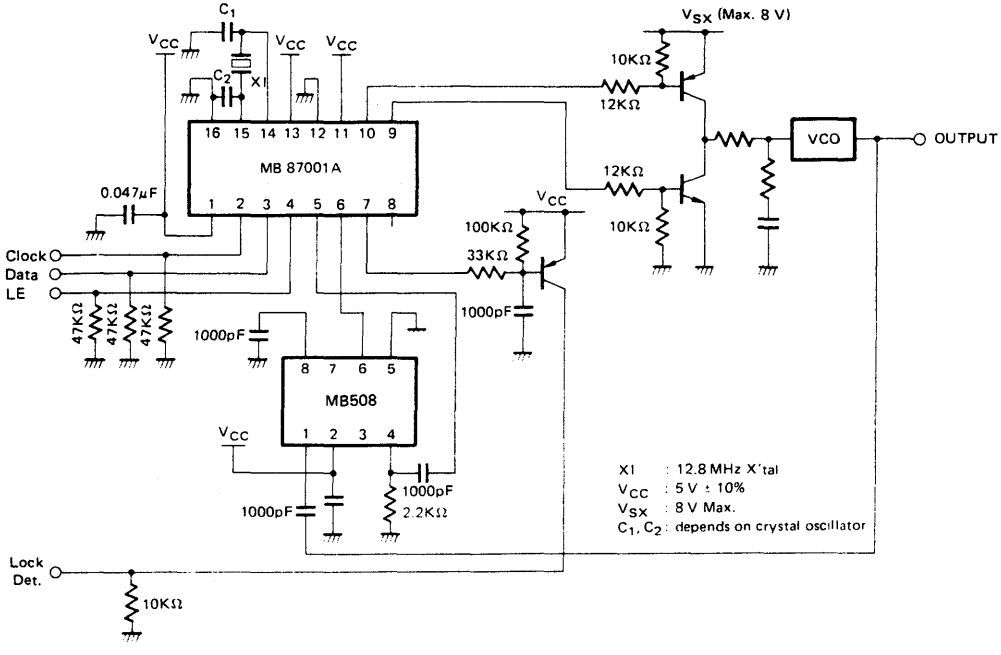


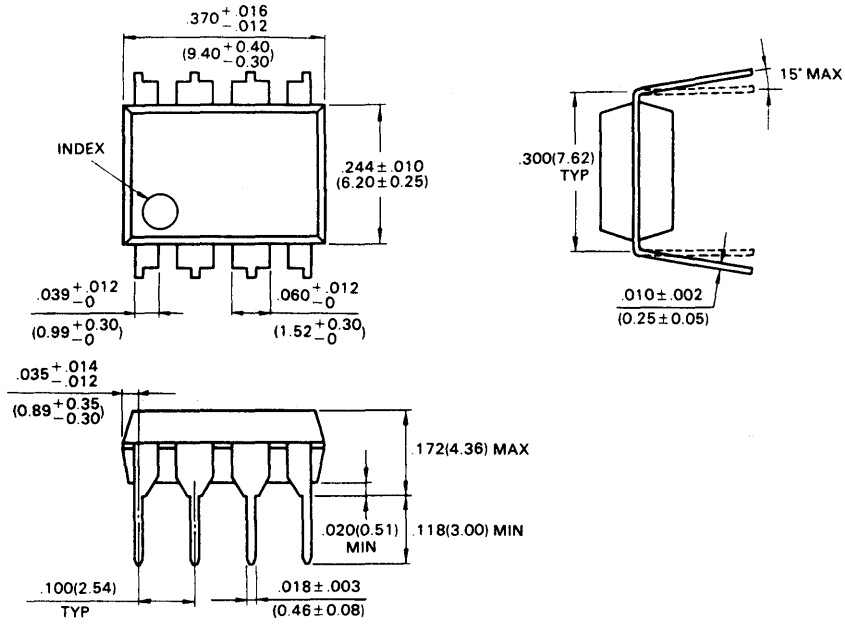
Fig. 4 – TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

(Suffix: -P)

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



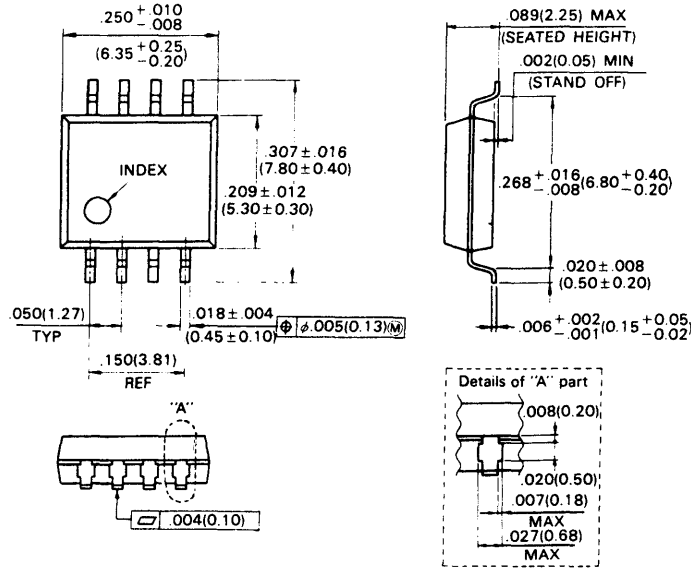
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PF)

2

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in inches (millimeters)

Sept. 1995
Edition 3.0a

FUJITSU

DATA SHEET

MB509

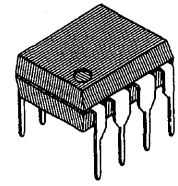
TWO MODULUS PRESCALER WITH STAND-BY MODE

2

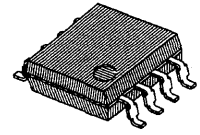
TWO MODULUS PRESCALER WITH STAND-BY MODE

The Fujitsu MB509 is a low power, two modulus prescaler equipped with the standby mode. The MB509 is used in conjunction with a frequency synthesizer to form a Phase Locked Loop (PLL) and will divide the input frequency by the modulus of 65/65 or 128/129.

Power consumption is typically 11.5mA at 5.0V. under normal operation, with the current reduced to180μA in standby mode. By using MB509 with the MB87076, intermittent operating mode can be achieved.



PLASTIC PACKAGE
DIP-08P-M01

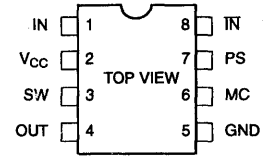


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation: fmax = 1.1GHz max. (P_{IN} = –4dBm min.)
- Pulse Swallow Function: 64/65, 128/129
- Power Supply Consumption: 58mW typ.
- Stand-by Current: 180μA typ.
- Stable Output Amplitude: $V_O = 1.6V_{p-p}$ typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87076, PLL frequency synthesizer IC
- Plastic 8-pin Dual-In-Line Package (Suffix: –P)
  Plastic 8-pin Mini Flat Package (Suffix: –PF)
- Built-in a Termination Resistor
  Stable output amplitude is obtained up to output load capacitance of 8pF

PIN ASSIGNMENT



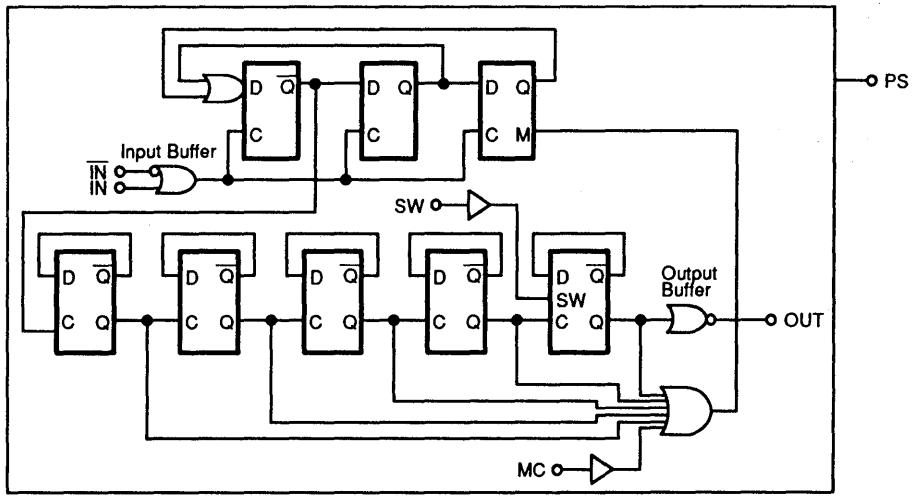
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB509 BLOCK DIAGRAM



PS	SW	MC	Divide Ratio
H	H	H	1/64
H	H	L	1/65
H	L	H	1/128
H	L	L	1/129
L	–	–	Stand-by mode

Note: SW: H=V_{CC}, L=open
MC: H=3.0V to V_{CC}, L=GND to 0.8V
PS: H=2.0V to V_{CC}, L=GND to 0.4V

PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	PS	Stand-by Control Input (See Divide Ratio Table)
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	–40	—	+85	°C
Load Capacitance	C_L	—	—	8	pF

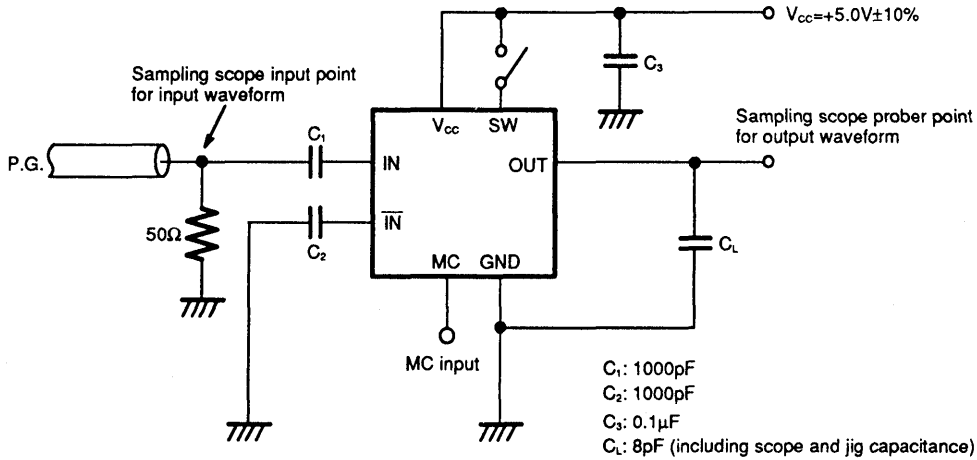
ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

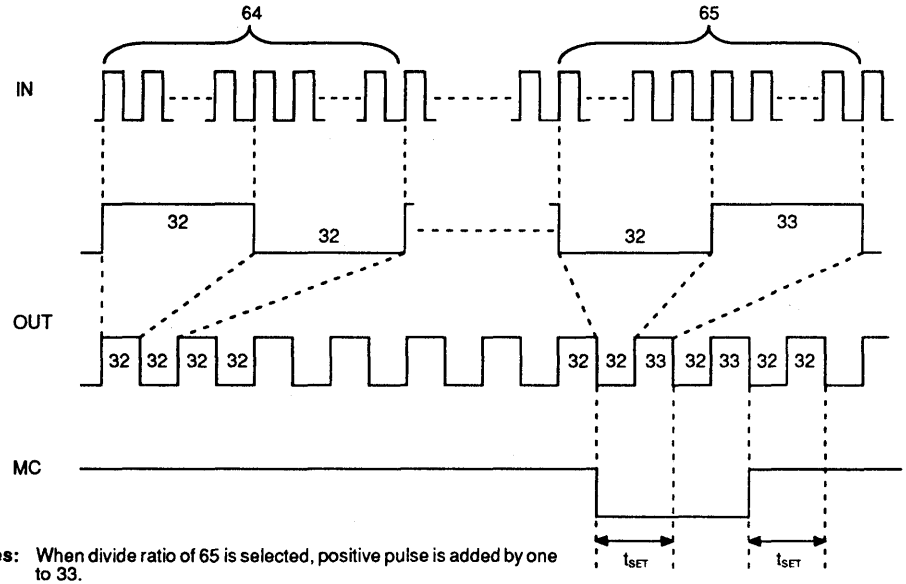
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power Supply Curent	I_{CC}		—	11.6	—	mA
	I_{PS}	Stand-by mode	—	180	—	µA
Output Amplitude	V_O	Built-in a Termination Resistor. Load Capacitance=8pF	1.0	1.6	—	V_{P-P}
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10	—	1100	MHz
Input Signal Amplitude	P_{IN}	—	–4	—	5.5	dBm
High Level Input Voltage for MC	V_{IH}	—	3.0	—	—	V
Low Level Input Voltage for MC	V_{IL}	—	—	—	0.8	V
High Level Input Voltage for SW	V_{IHS}*		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW	V_{ILS}		Open			V
High Level Input Voltage for PS	V_{IH}	—	2.0	—	—	V
Low Level Input Voltage for PS	V_{IL}	—	—	—	0.4	V
High Level Input Current for MC	I_{IH}	V_{IH} = 3.0V	—	—	0.4	mA
Low Level Input Current for MC	I_{IL}	V_{IL} = 0.8V	–0.2	—	—	mA
Modulus Set-up Time MC to Output	t_{SET}	—	—	16	26	ns

Note: *Design Guarantee

Fig. 2 – TEST CIRCUIT



TWO MODULUS OPERATING TIMING CHART (64/65 DIVIDE RATIO)



Notes: When divide ratio of 65 is selected, positive pulse is added by one to 33.
The typical set up time is 16ns from the MC signal input to the timing of change of prescaler divide ratio.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

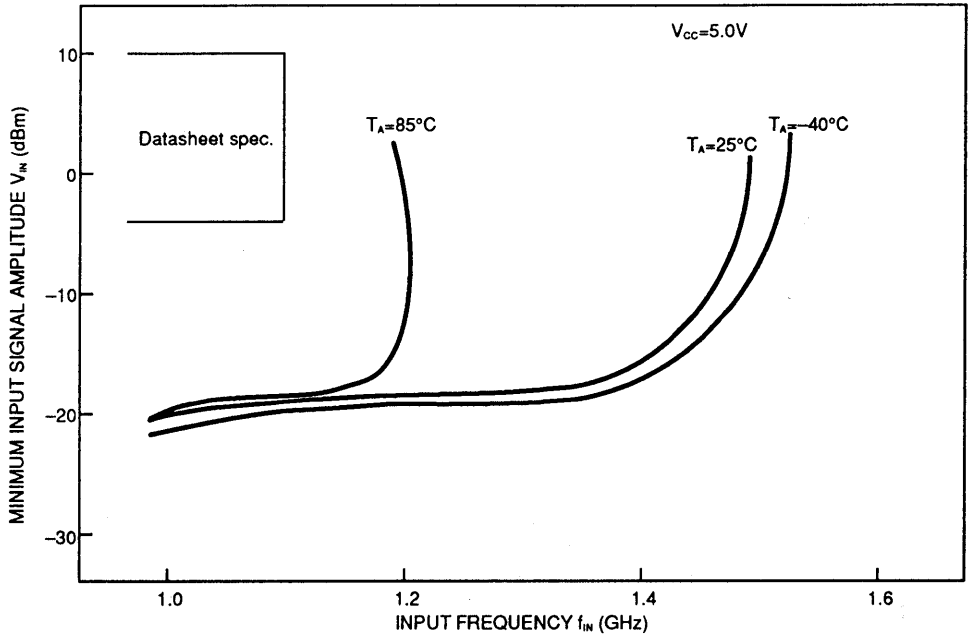
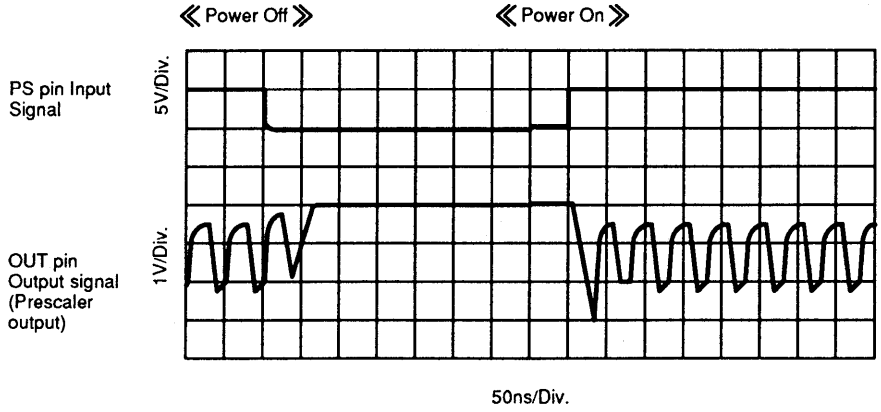
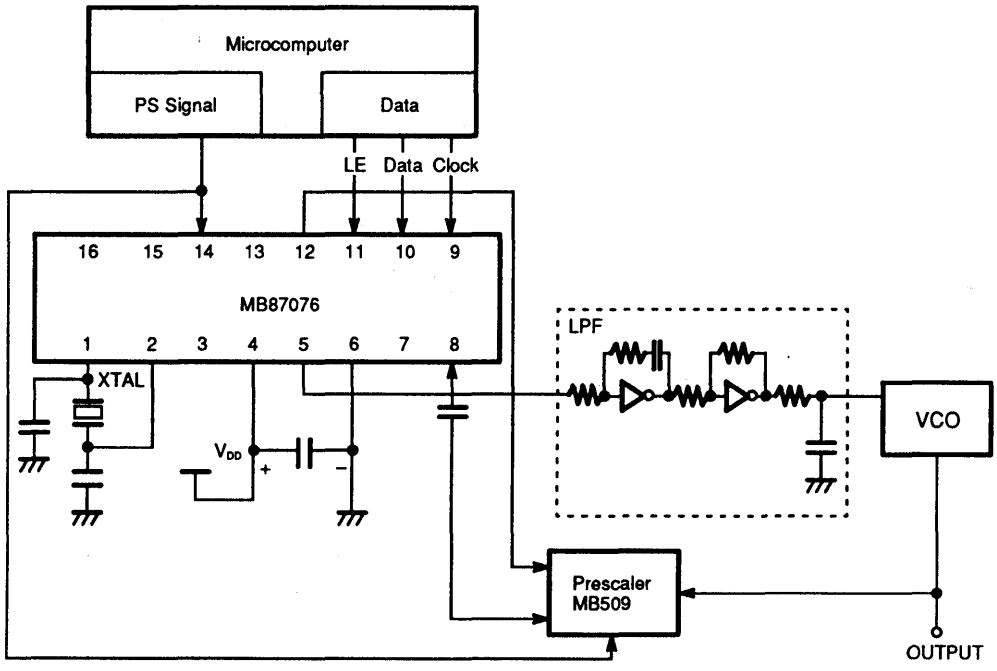


Fig. 4 – WAVEFORM OF STAND BY MODE



Note: About 50 ns of set up time is required both power on/off.

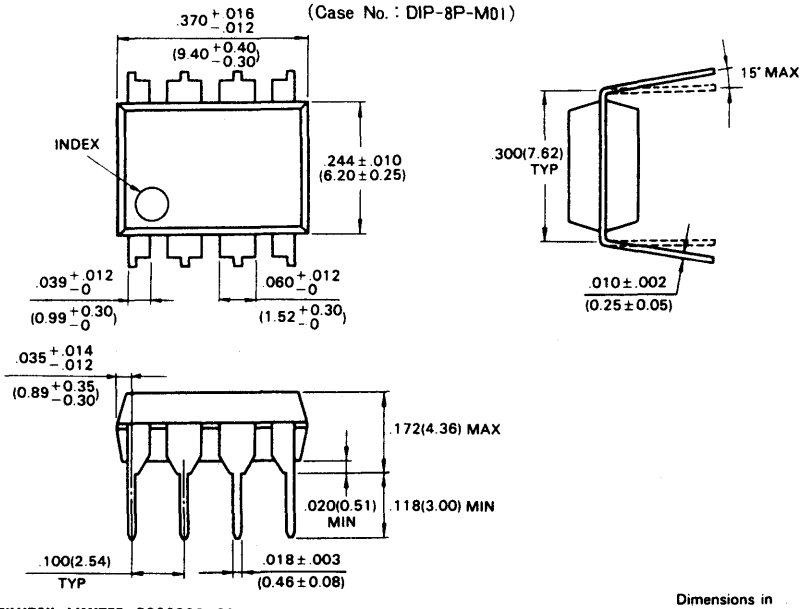
Fig. 5 – TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-8P-M01)

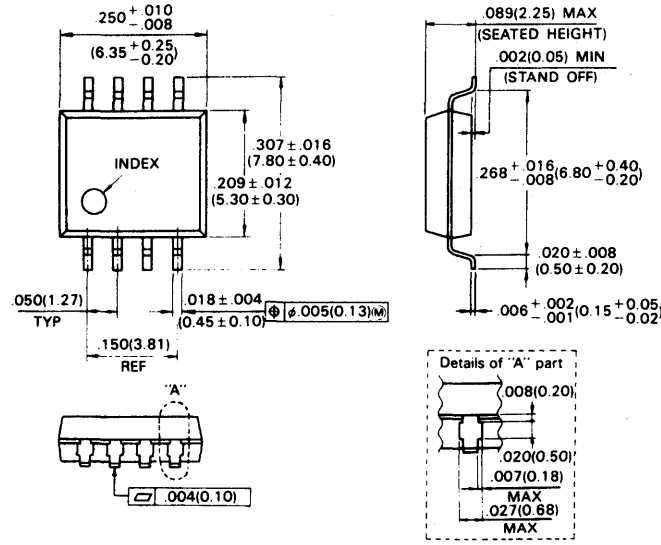


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-8P-M01)



Dimensions in inches (millimeters)

Sept. 1995
Edition 3.0b

FUJITSU

DATA SHEET

MB510

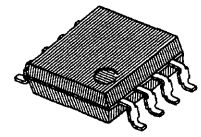
2.7GHz TWO MODULUS PRESCALER

2

2.7GHz TWO MODULUS PRESCALER

The Fujitsu MB510 is an ultra high speed, two modulus prescaler that forms a Phase Locked Loop (PLL) when combined with a frequency synthesizer such as the Fujitsu MB87001A. It divides the input frequency by the modulus of 128/144 or 256/272, and operates at a low power supply current of 10mA at 5.0V.

Through the use of Fujitsu's Advanced Process Technology, the MB510 achieves extremely small stray capacitance from its internal elements.

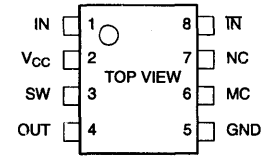


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation: 2.7GHz max.
- Power Dissipation: 50mW typ.
- Pulse Swallow Function: 128/144, 256/272
- Wide Operation Temperature: -40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6V_{p-p} typ.
- Built-in Termination Resistor
- Complete PLL synthesizer circuit with the Fujitsu MB87001A PLL synthesizer IC
- Package
  Standard 8-pin Flat Package (Suffix: -PF)

PIN ASSIGNMENT

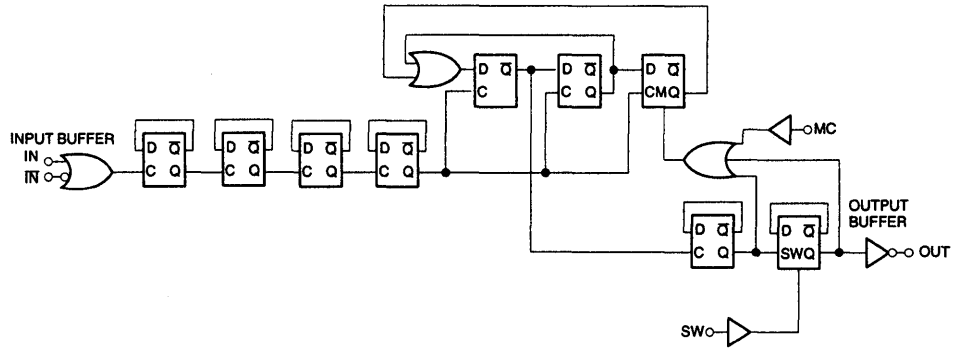


ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



SW	MC	Divide Ratio
H	H	1/128
H	L	1/144
L	H	1/256
L	L	1/272

Note: SW: H = V_{CC}, L = open
MC: H = 2.0V to V_{CC}, L = GND to 0.8V

Figure 1. MB510 Block Diagram

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			8	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply Curent	I_{CC}			10.0	15.0	mA
Output Amplitude	V_O	Built-in a termination resistor. Load capacitance = 8pF	1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10		2700	MHz
Input Signal Amplitude	P_{IN}	f_{IN} = 10 to 2200MHz	–10		10	dBm
		f_{IN} = 2200 to 2700MHz	–4		10	
High Level Input Voltage for MC Input	V_{IHM}		2.0			V
Low Level Input Voltage for MC Input	V_{ILM}				0.8	V
High Level Input Voltage for SW Input	V_{IHS}*		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW Input	V_{ILS}		Open			V
High Level Input Current for MC Input	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input	I_{ILM}	V_{IL} = 0.8V	–0.2			mA
Modulus Set-up Time MC to OUT	t_{SET}			16	26	ns

Note: *Design Guarantee

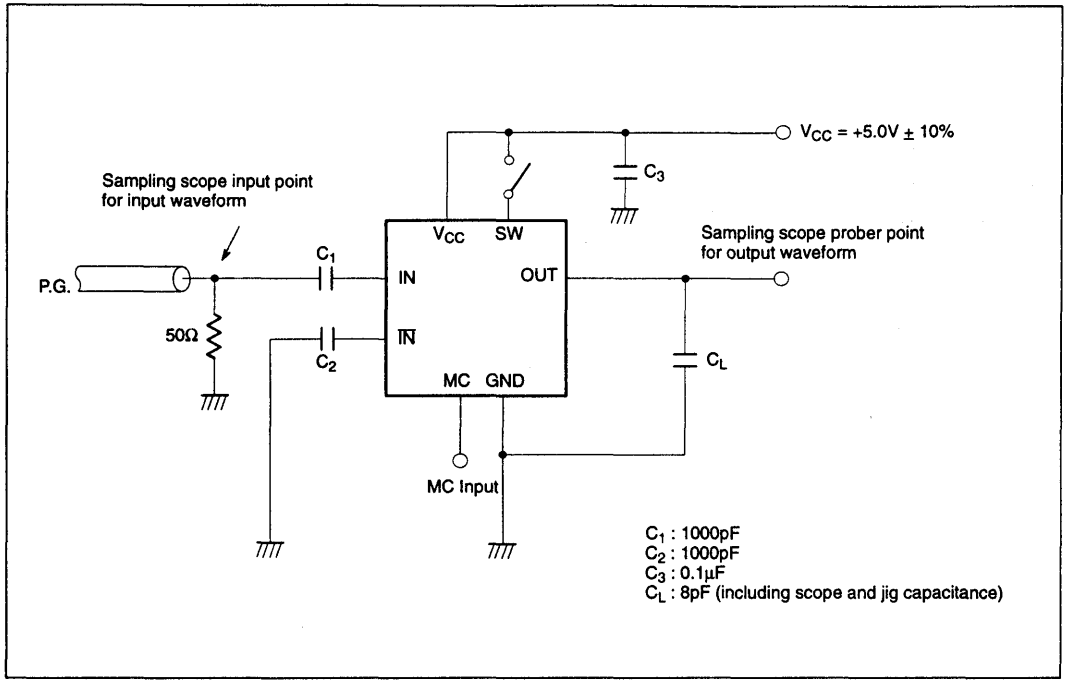


Figure 2. Test Circuit

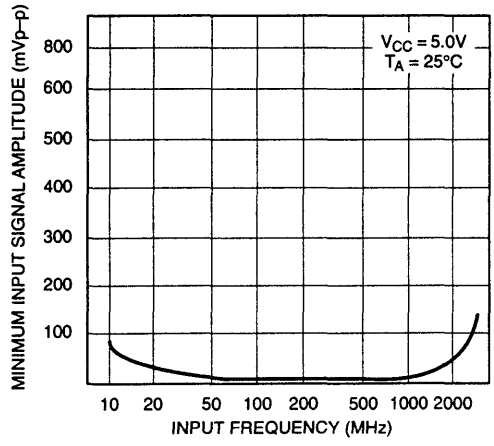
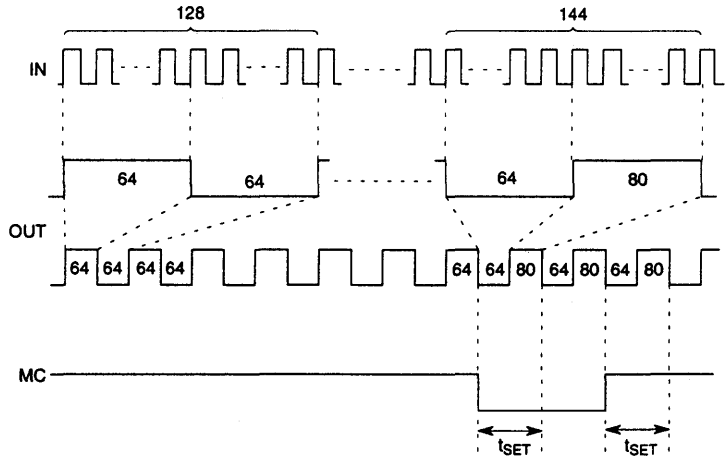


Figure 3. Input Signal Amplitude vs. Input Frequency

TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/144



Note: When divide of 144 is selected, positive pulse is applied by 16 to 80.
The typical set up time is 16 ns from the MC signal input to the timing of change of prescaler divide ratio.

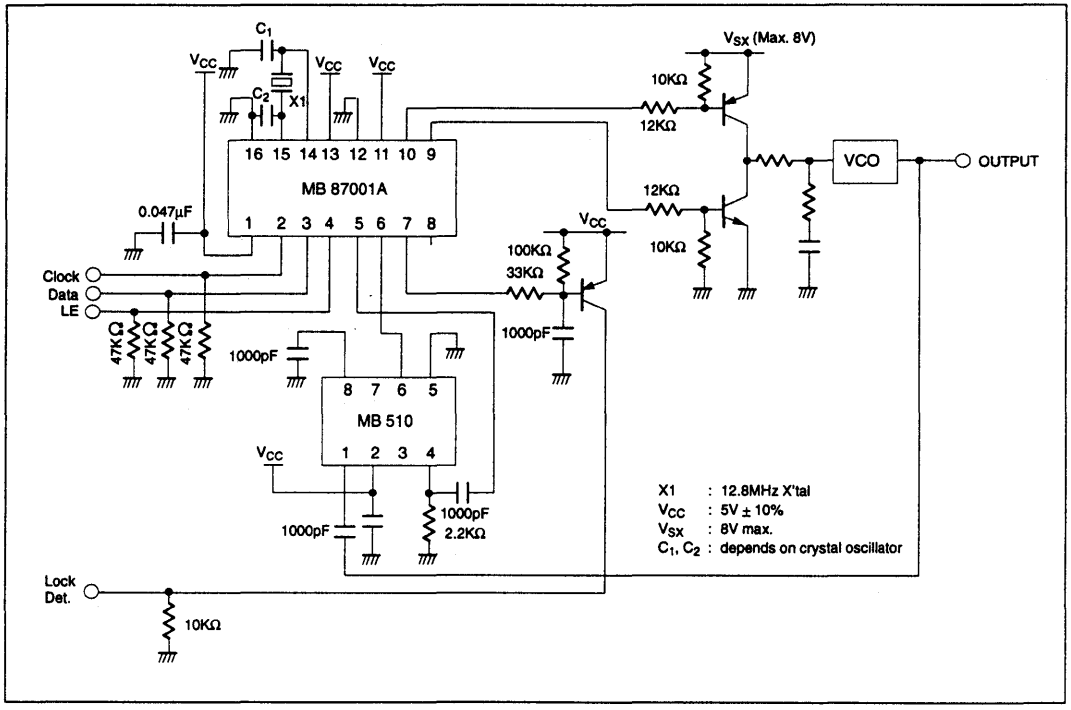
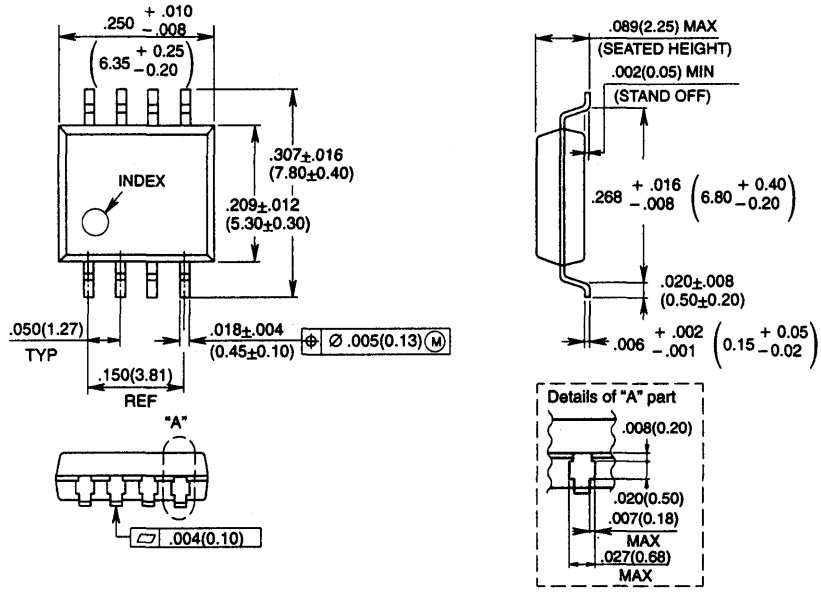


Figure 4. Typical Application Example

PACKAGE DIMENSIONS

(Suffix: –PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No: FPT-08P-M01)



Dimensions in
inches (millimeters)

Sept. 1995
Edition 2.0a

FUJITSU

DATA SHEET

MB511

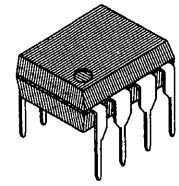
1GHz HIGH SPEED PRESCALER

2

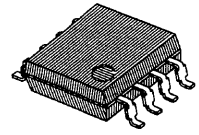
HIGH SPEED PRESCALER

The Fujitsu MB511 is a 1.0GHz high speed prescaler that forms a Phase Locked Loop (PLL) circuit when combined with a Fujitsu frequency synthesizer.Based on Fujitsu's advanced Bipolar processing, the MB511 maintains a consistent low power consumption of 23mA @ 5V. In addition, it can detect low amplitude input signals with a sensitivity of –20dBm min.

The MB511 will divide the input frequency a modulus of 1, 2, or 8, and is well suited for applications in CATV and electronically tuned TV.



PLASTIC PACKAGE
DIP-08P-M01

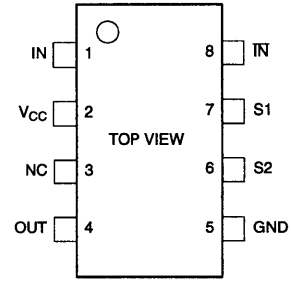


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- Wide operating frequency range:
  f_{in} = 50 to 1000MHz (v_{in} = –20dBm)
- Maximum operating frequency depends upon the divide ratio:
  1/1: 250MHz max. (Buffer through)
  1/2: 500MHz max.
  1/8: 1000MHz max.
- Low supply current: 23mA @5V
- High input sensitivity: –20dBm min.
- Stable Output Amplitude: 800mVp–p ($C_L \leq 5pF$)
- Wide temperature range: T_A = –40 to +85°C
- Plastic 8-pin Dual-In-Line package (Suffix: –P)
  Plastic 8-pin Flat package (Suffix: –PF)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

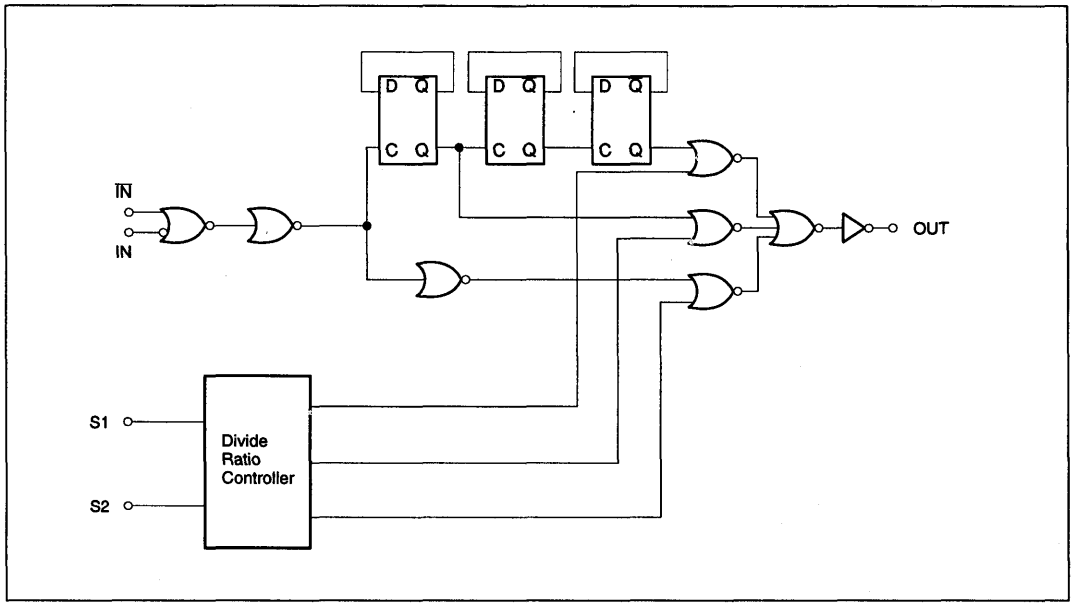


Figure 1. MB511 Block Diagram

FUNCTION TABLE

S1	S2	Divide Ratio	Operating Frequency
L	L	Not used	—
L	H	1	250MHz
H	L	2	500MHz
H	H	8	1000MHz

H = V_{CC}
L = OPEN

PIN DESCRIPTIONS

Pin Number	Symbol	I/O	Descriptions
1	IN	I	Input. The connection with VCO should be an AC connection.
2	V_{CC}	–	Power supply voltage input.
3	NC	–	No connection.
4	OUT	O	Output. Termination resistor is necessary due to emitter follower output.
5	GND	–	Ground.
6	S2	I	Divide ratio control input.
7	S1	I	Divide ratio control input.
8	$\overline{IN}$	I	Complementary Input.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Operating Temperature	T_A	–40		+85	°C	
Load Capacitance	C_L			5	pF	Termination resistor 500Ω

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Current		I_{CC}	15	23	32	mA	Except termination output current.
Output Amplitude		V_O	0.4	0.8	1.2	V_{p-p}	500Ω termination, C_L = 5pF max.
Input Frequency	1/1	f_1	50		250	MHz	Min. value is measured with coupling capacitor of 1000pF.
	1/2	f_2	50		500	MHz	
	1/8	f_3	50		1000	MHz	
Input Signal Amplitude		P_{IN}	–20		+10	dBm	50Ω
High Level Input Voltage	S1, S2	V_{IH}	V_{CC} –0.7	V_{CC}	V_{CC} +0.5	V	
Low Level Input Voltage		V_{IL}		OPEN		V	
Low Level Input Current	S1, S2	I_{IH}	40		160	μA	V_{CC} = 5V

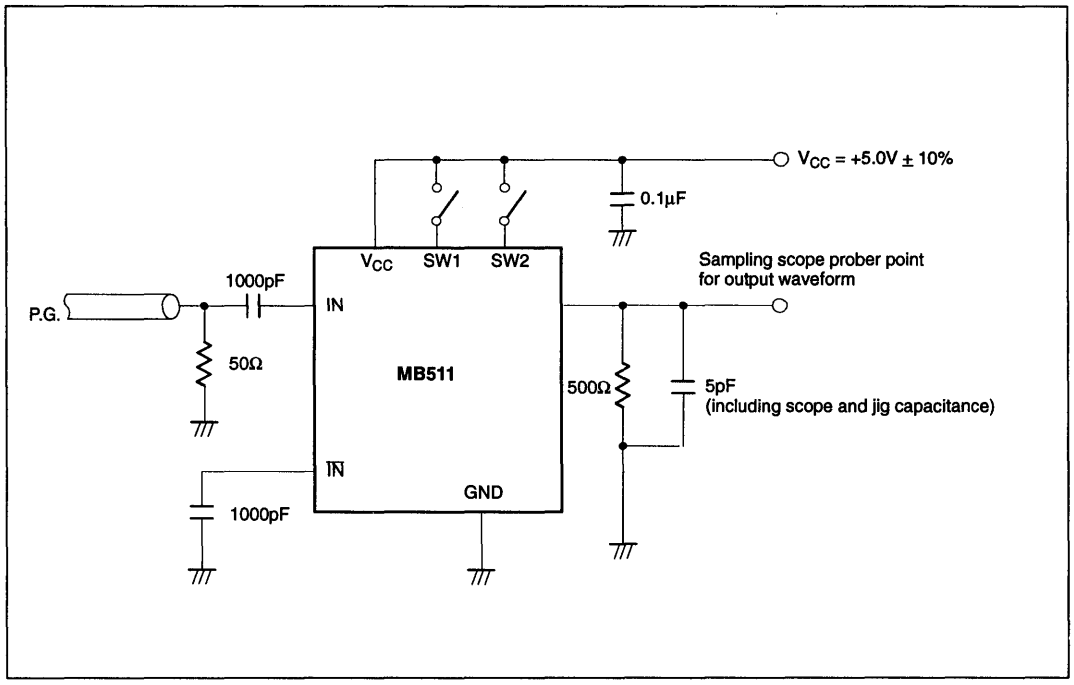


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS CURVES

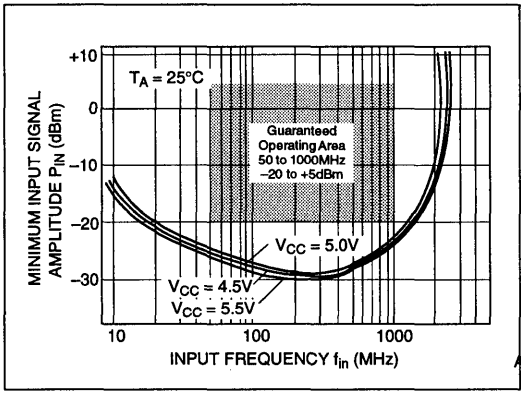


Figure 3. Input Sensitivity Curve (1/8 Divide Ratio) Power Supply Voltage Dependency

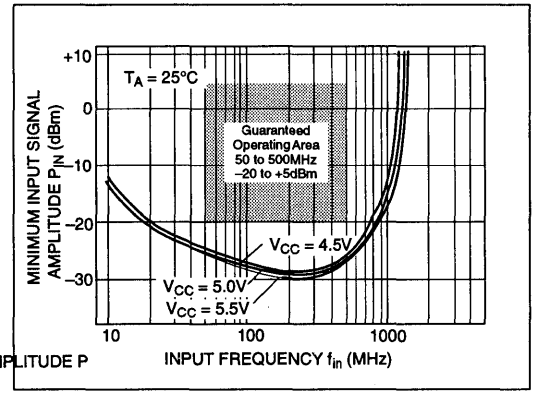


Figure 4. Input Sensitivity Curve (1/2 Divide Ratio) Power Supply Voltage Dependency

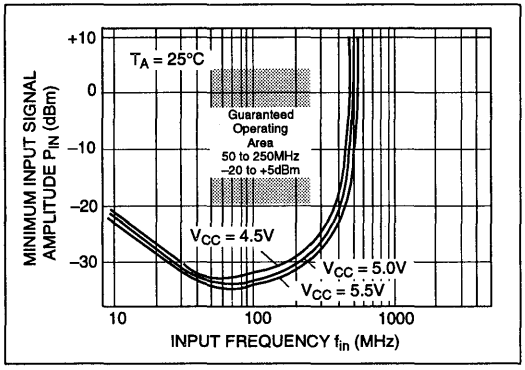


Figure 5. Input Sensitivity Curve (1/1 Divide Ratio) Power Supply Voltage Dependency

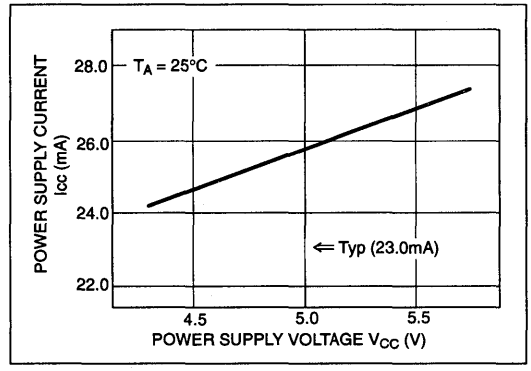


Figure 6. Power Supply Current vs. Power Supply Voltage

TYPICAL CHARACTERISTICS CURVES (Continued)

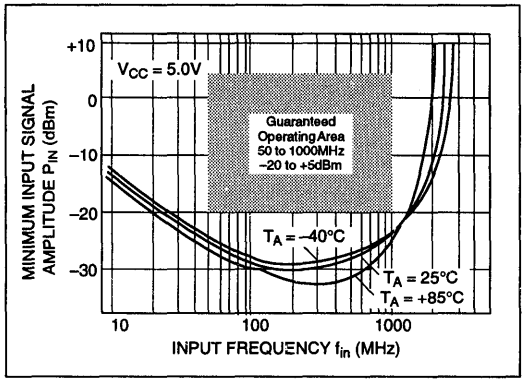


Figure 7. Input Sensitivity Curve (1/8 Divide Ratio) Temperature Dependency

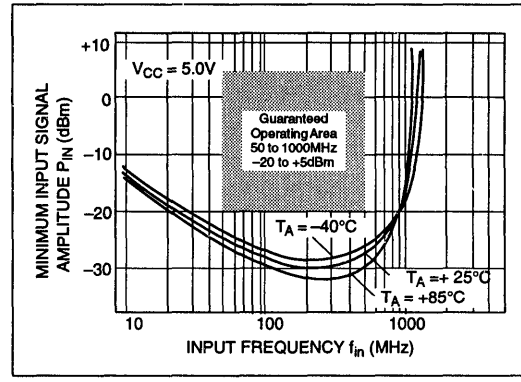


Figure 6. Input Sensitivity Curve (1/2 Divide Ratio) Temperature Dependency

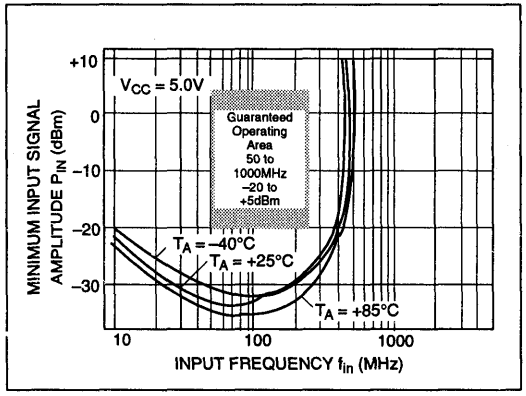


Figure 9. Input Sensitivity Curve (1/1 Divide Ratio) Temperature Dependency

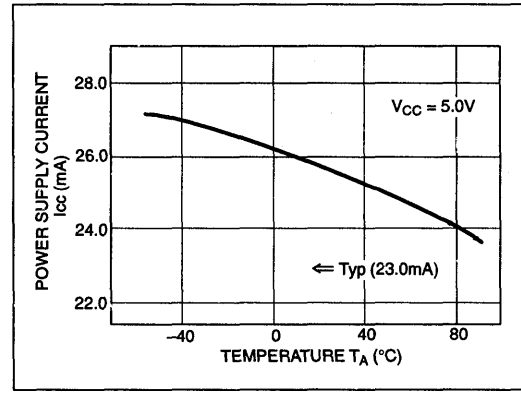
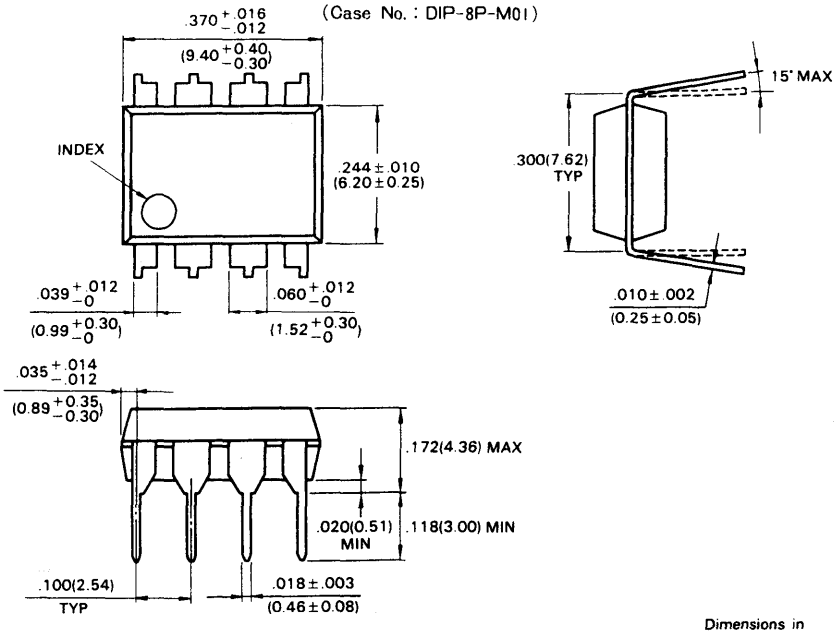


Figure 10. Power Supply Current vs. Temperature

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE

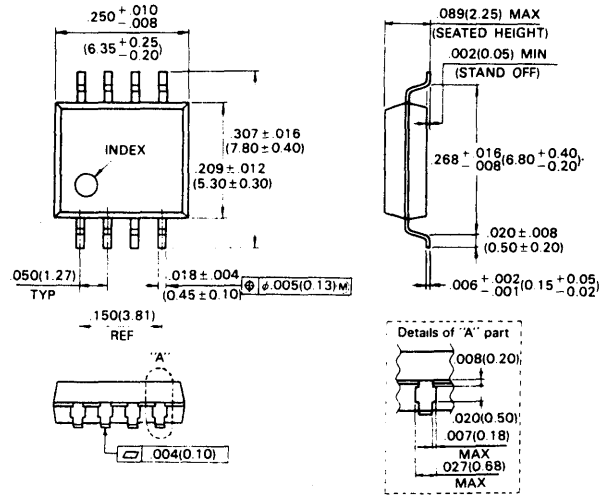
(Case No. : DIP-8P-M01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-8P-M01)



Dimensions in
inches (millimeters)

DS04-21600-3E

FUJITSU

DATA SHEET

MB551 *ASSP for DTS BIPOLAR*
Prescaler with VCO (Dual-Modulus, 1.0 GHz)

2

■ DESCRIPTION

The MB551 is a dual-modulus prescaler incoporating a voltage controlled oscillator (VCO) and is used with 900-MHz band frequency synthesizers. The MB551 consists of: a Colpitts oscillator with grounded base capacitor, a buffer amplifier with open collector output, a prescaler interface circuit, and a dual-modulus prescaler operating at frequencies divided by 128/129. The oscillator block accommodates external components such as a capacitor, a dielectric oscillator (resonator), and a variable capacitor. These components combined with the circuitry on the MB551 chip makes up the VCO.

The VCO and the prescaler are connected by an internal circuit. This minimizes the effects of prescaler input load variation on critical VCO characteristics, such as C/N ratio.

The MB551 typically operates at 5 V and draws 16 mA of current.

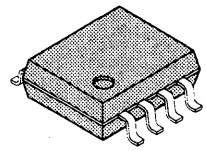
■ FEATURES

- Oscillator frequency: 1 GHz (Max)
- Low power consumption: Icc = 16 mA (Typical)
- Oscillator output power: 0 dBm (Typical)
- C/N ratio: 70 dB (Typical) Measurement conditions: Δf = 50 kHz, BW = 15 kHz
  65 dB (Typical) Measurement conditions: Δf = 25 kHz, BW = 15 kHz
- S/N ratio: 45 dB (Typical) Measurement conditions: BW = 0.3 to 3 kHz, 3 kHz.Dev, 1 kHz Tone
- Stable oscillator output
  Supply voltage dependence: ±200 kHz/V (Typical)
  Frequency stability: 35 ppm/°C (Typical)

(Continued)

■ PACKAGE

8 pin Plastic SOP

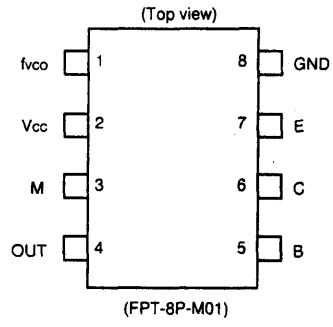


(FPT-8P-M01)

(Continued)

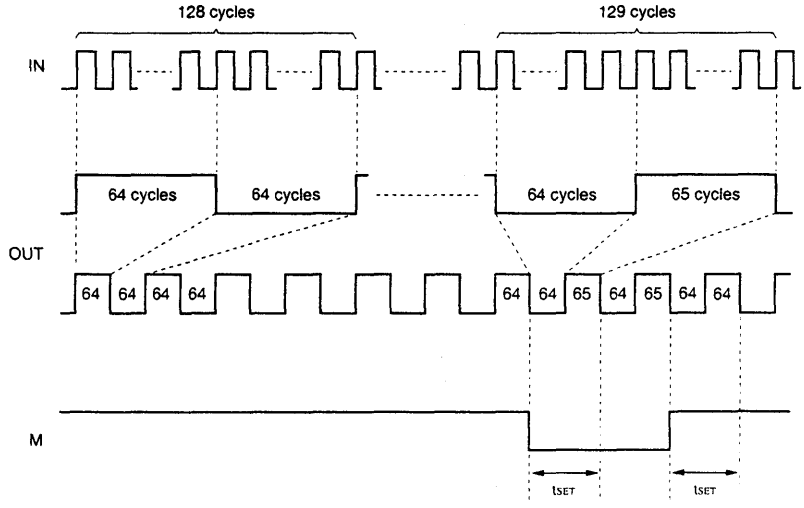
- Pulse swallow method: Division-by-128/129 prescaler
- Prescaler output with termination circuit: V_I = 1.6 V_{P-P}

■ PIN ASSIGNMENT



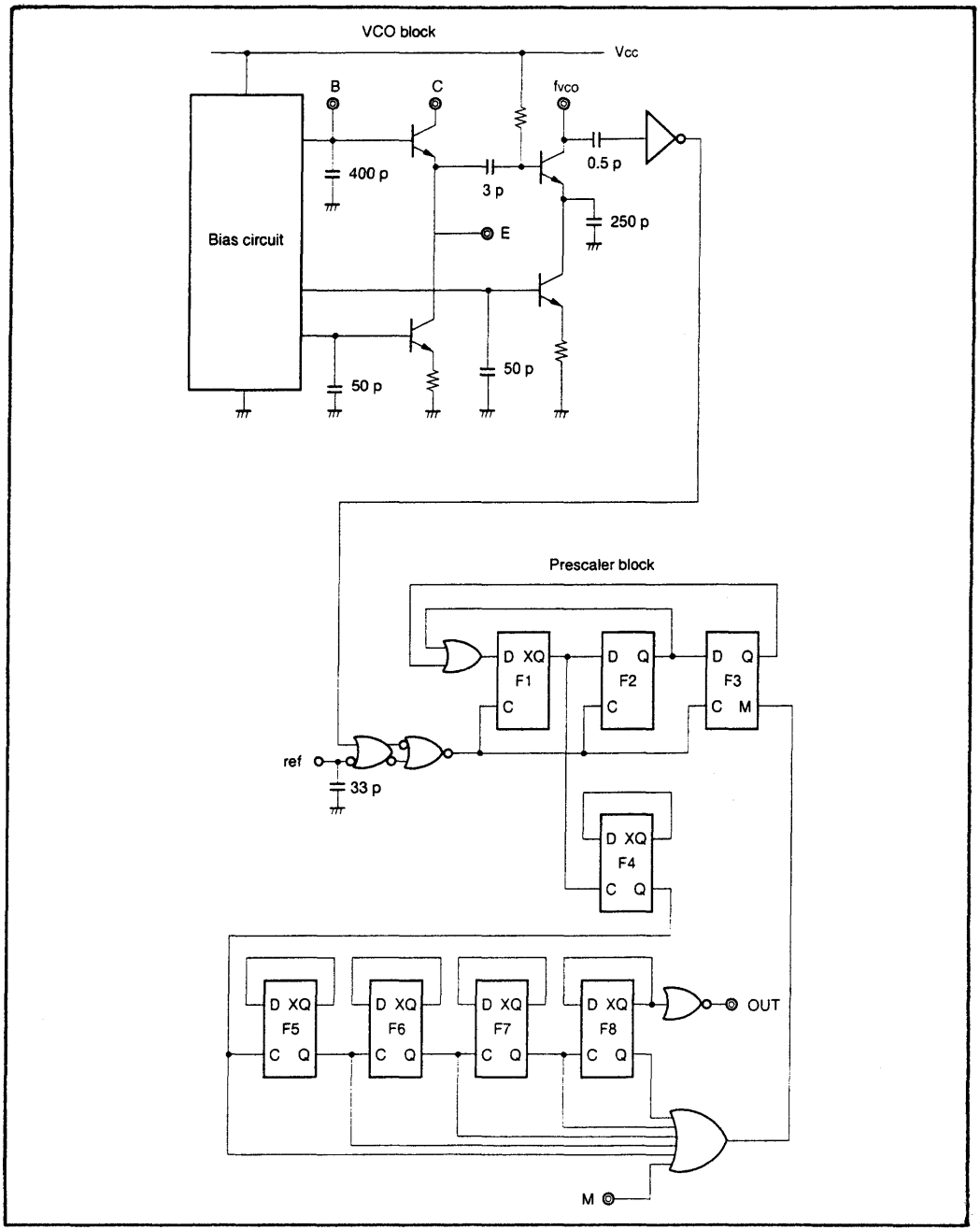
Pin No.	Symbol	Function
1	fvco	VCO signal pin
2	Vcc	Power supply pin
3	M	Module setting pin
4	OUT	Prescaler output pin
5	B	Oscillator transistor base pin
6	C	Oscillator transistor collector pin
7	E	Oscillator transistor emitter pin
8	GND	Ground pin

■ TIMING DIAGRAM (Example of Dual-modulus, division-by-128/129 type)



- M pin = High: Division by 128
  M pin = Low: Division by 129
  (V_{IH} = 2.0 V min, V_{IL} = 0.8 V max.)
- Division plus one makes the high-to-low transition longer by one cycle of the frequency-divided signal.
- Setup time (t_{SET}) from input of the M signal to change in the divide ratio of the prescaler is 16 ns (typical).

■ BLOCK DIAGRAM



■ MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	V_{CC}	−0.5 to +7.0	V	
Oscillator transistor base/ emitter applied voltage	V_B, V_E	—	—	Do not apply external DC voltage to the base or emitter pin.
M/OUT (Pin 3/4) applied voltage	V_{P1}	−0.5 to V_{CC} + 0.5	V	
fvco/C (Pin 1/6) applied voltage	V_{P2}	$V_{CC} \leq V_{P2} < +7.0$	V	
Applied current	I_P	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
External variable capacitor control voltage	V_T	1.5	—	4.5	V	
Operating temperature	Ta	−40	—	+85	°C	
Prescaler output load	CL	—	—	8	pF	

■ ELECTRICAL CHARACTERISTICS

1. VCO Block

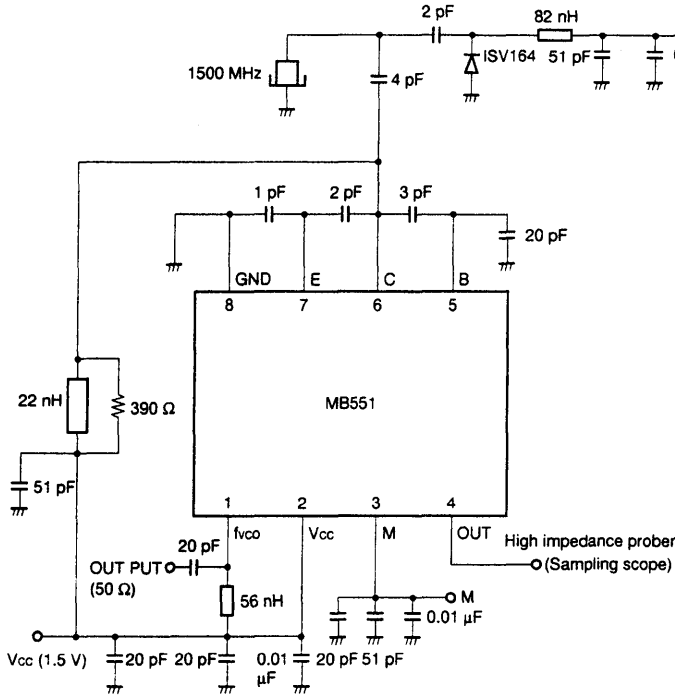
Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Oscillator frequency	fosc	—	—	1000	MHz	
Oscillator output	Pout	—	0	—	dBm	
C/N ratio	C/N	—	70	—	dB	Df = 50 kHz, BW = 15 kHz
			65	—	dB	Df = 25 kHz, BW = 15 kHz
S/N ratio	S/N	—	45	—	dB	BW = 0.3 to 3 kHz, 3 kHz, Dev, Tone 1 kHz
Fundamental/1st harmonic ratio	SP–1	—	–10	—	dB	
Frequency stability	Δft	—	35	—	ppm/°C	–40 to 85°C, 25°C (Typical)
Supply voltage variation	Δfr	—	±200	—	kHz/V	5 V ± 10 %
Mod Sense	Δfosc	—	4	—	MHz/V	Control range: 1.0 to 4.0 V

Note: Electrical characteristics depend on external components and mounting conditions. These values are reference values assuming the test circuit examples on pages 6 and 7.

2. Prescaler Block

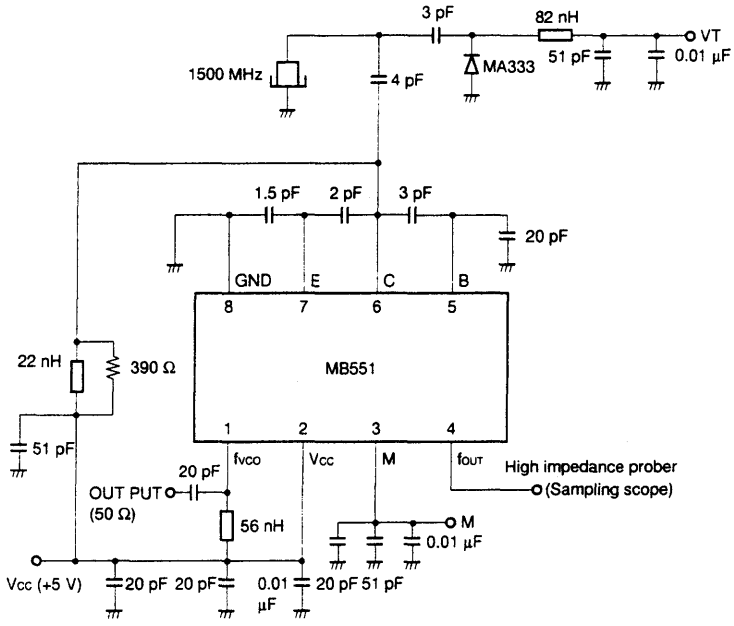
Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply current	I_{CC}	—	16.0	—	mA	
Output amplitude	V_{OUT}	1.0	1.6	—	V_{P-P}	Load capacitance when internal termination pin is used: 8 pF or less
Response frequency	f_{in}	—	—	1000	MHz	
Allowable input power	P_{in}	–4	—	+10	dBm	
High-level input voltage (MC)	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
High-level input current (MC)	I_{IH}	—	—	0.4	mA	
	I_{IL}	–0.2	—	—	mA	
Module setup time	t_{SET}	—	16	26	ns	

■ TEST CIRCUIT EXAMPLE 1



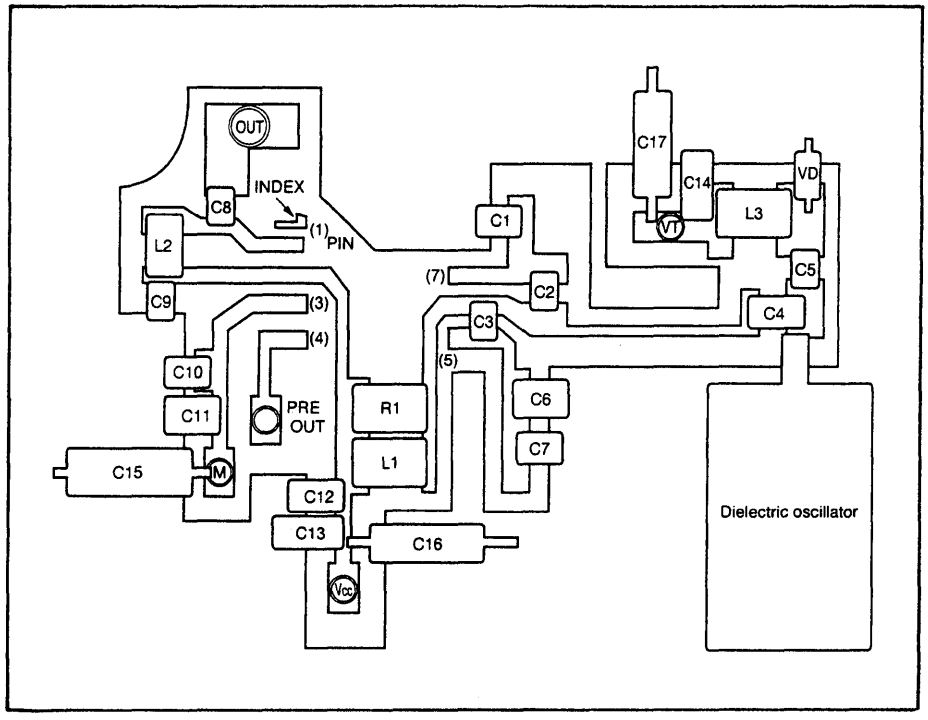
Chip capacitor: UMK316C, UMK212C, UCN103C Series (Taiyo Yuden)
Chip coil: LQN2A Series (Murata Works)
Dielectric oscillator: DRR060UE (Murata Works)
Varicap: ISV164 (NEC)

■ TEST CIRCUIT EXAMPLE 2



Chip capacitor: UMK316C Series (Taiyo Yuden)
Chip coil: LQN2A Series (Murata Works)
Dielectric oscillator: DRR060UE (Murata Works)
Varicap: MA333 (Mitsubishi Electric)

■ RECOMMENDED PC BOARD PATTERN



[Mounted component list]

C1: 1 pF (Taiyo Yuden UMK212C)
C2: 2 pF (Taiyo Yuden UCN103C)
C3: 3 pF (Taiyo Yuden UMK212C)
C4: 4 pF (Taiyo Yuden UMK212C)
C5: 2 pF (Taiyo Yuden UMK212C)
C6: 20 pF (Taiyo Yuden UMK316C)
C7: 51 pF (Taiyo Yuden UMK212C)
C8: 20 pF (Taiyo Yuden UMK316C)
C9: 20 pF (Taiyo Yuden UMK316C)
C10: 51 pF (Taiyo Yuden UMK212C)
C11: 20 pF (Taiyo Yuden UMK316C)
C12: 51 pF (Taiyo Yuden UMK212C)
C13: 20 pF (Taiyo Yuden UMK316C)
C14: 51 pF (Taiyo Yuden UMK212C)

C15: 0.01 µF (Film capacitor)
C16: 0.01 µF (Film capacitor)
C17: 0.01 µF (Film capacitor)

R1: 390 Ω (Rohm MCR25)

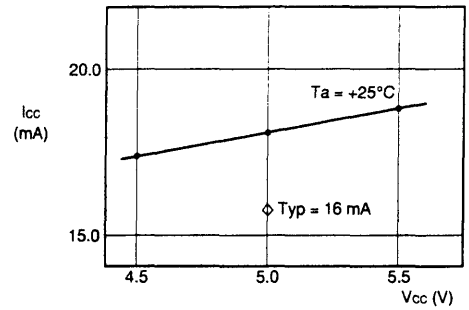
L1: 22 nH (Murata Works LQN2A)
L2: 56 nH (Murata Works LQN2A)
L3: 82 nH (Murata Works LQN2A)

VD: 1SV164 (NEC)

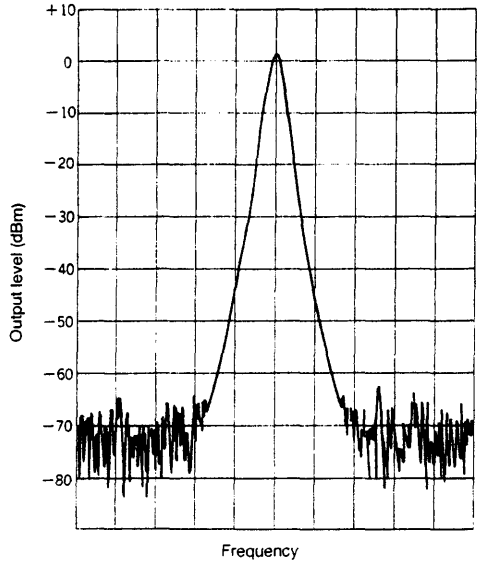
Dielectric oscillator: (Murata Works DRR060 Series, 1.5 GHz)

■ MEASUREMENT RESULTS

(1) Supply Current

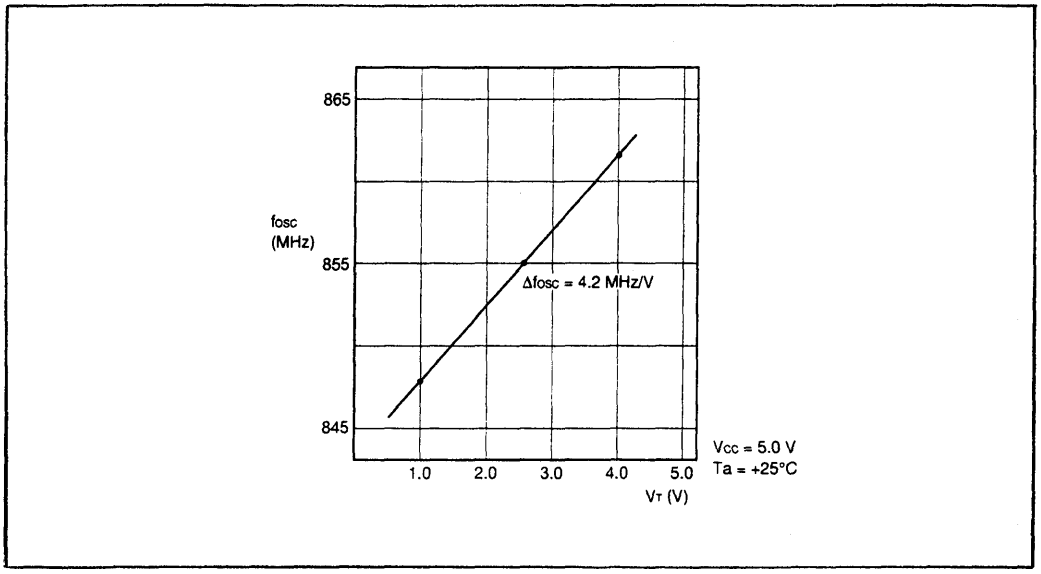


(2) Oscillation Waveform (50-kHz span)

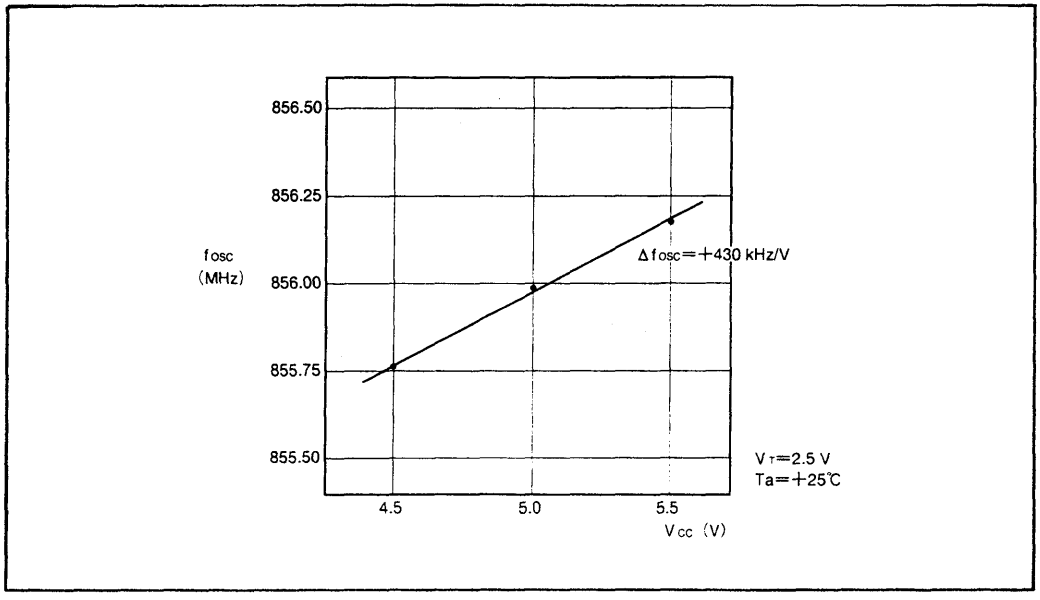


■ MEASUREMENT RESULTS (TEST CIRCUIT 1 ON RECOMMENDED PC BOARD)

(1) Conversion Gain

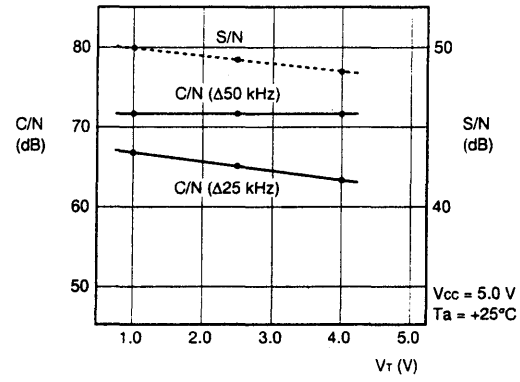


(2) Supply Voltage Variation

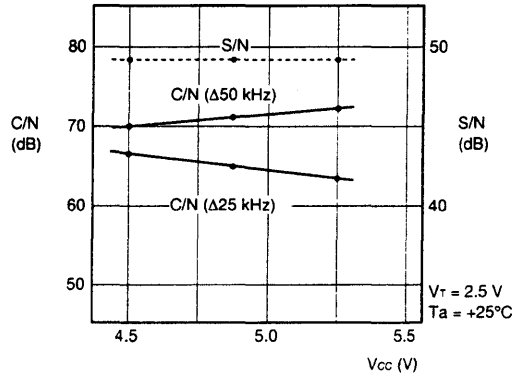


(3) C/N, S/N

• Control Voltage Dependence



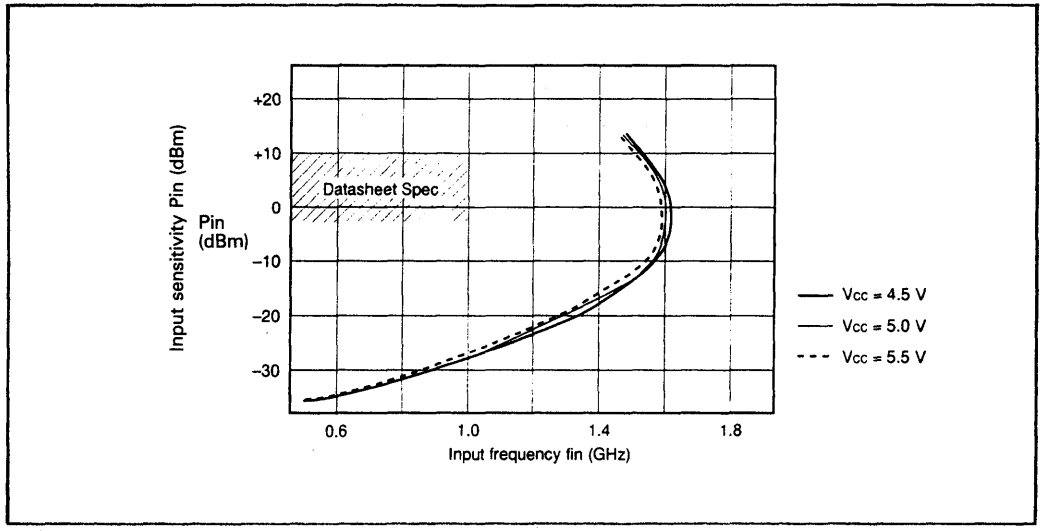
• Supply Voltage Dependence



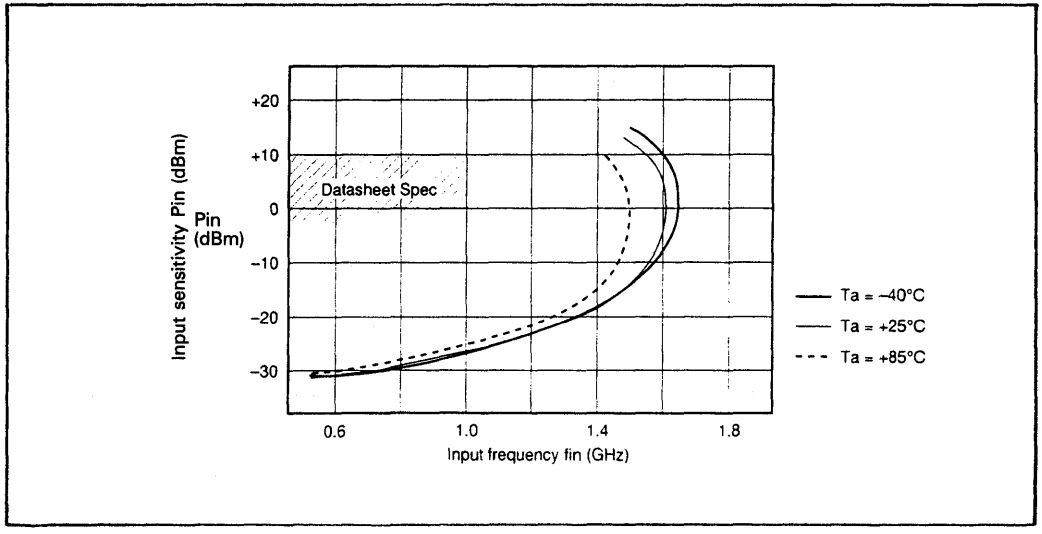
■ MEASUREMENT RESULTS

(1) Prescaler Input Sensitivity Curve

- **Supply voltage dependence (Ta = +25°C)**

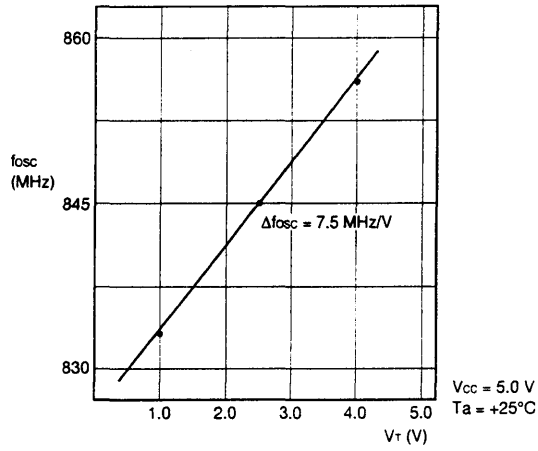


- **Temperature dependence (Vcc = 5 V)**



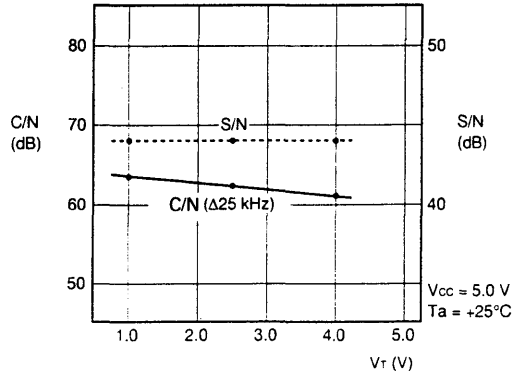
■ MEASUREMENT RESULTS (TEST CIRCUIT 2)

(1) Conversion Gain

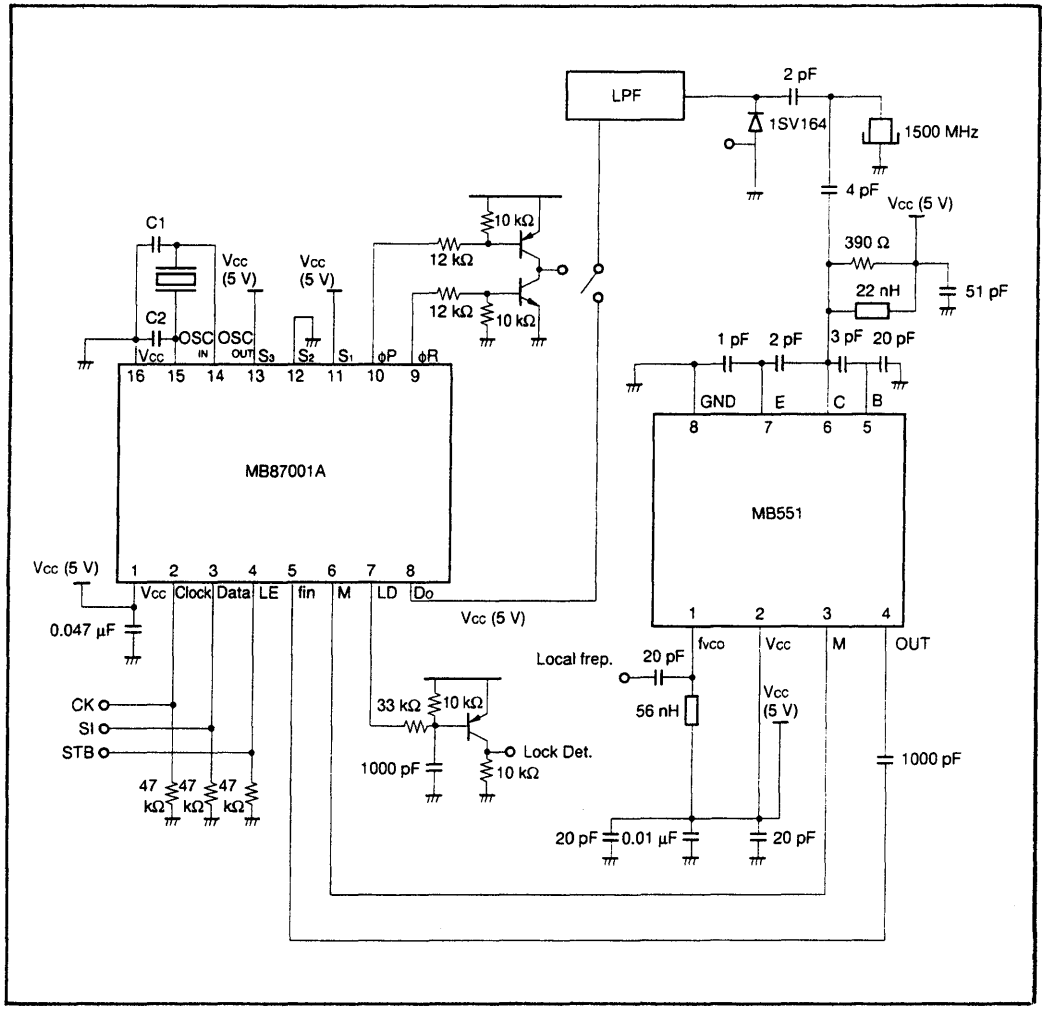


(2) C/N, S/N

- **Control voltage dependence**



■ SAMPLE APPLICATION CIRCUIT

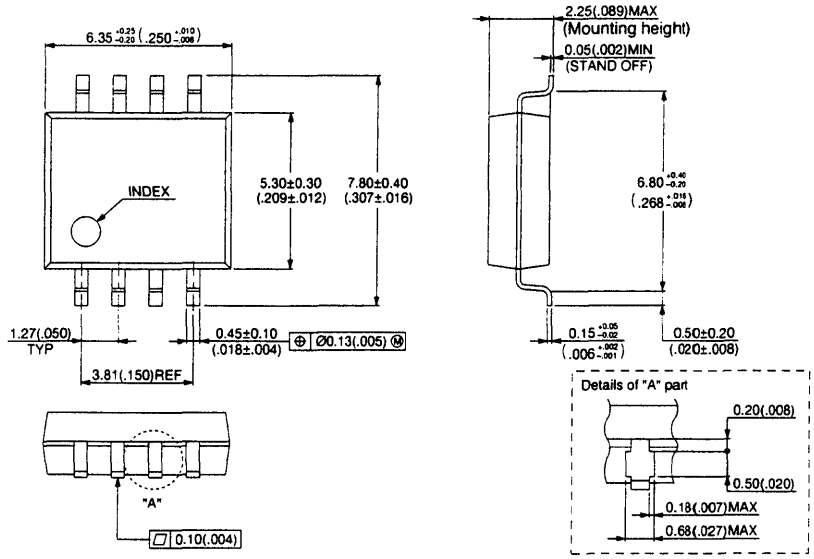


■ ORDERING INFORMATION

Part number	Package	Remarks
MB551PF	8 pin Plastic SOP (FPT-8P-M01)	

■ PACKAGE DIMENSIONS

8 pin Plastic SOP
(FPT-8P-M01)



Dimensions in mm (inches)

SECTION 3

CMOS Phase–Locked Loops (PLLs) – *At a Glance*

The Fujitsu family of CMOS PLLs offers a wide range of operating frequencies with low supply current and voltages to meet many diverse design requirements. A serial input programming capability is a feature of all Fujitsu's PLLs.

Page Number	Device Part Number	f_{IN} (max) MHz @3v/5v	N Program Counter	A Swallow Counter	R Reference Counter	I_{DD} mA @3v/5v	V_{DD}	Package
3-3	MB87001A	10/13	Binary 5–1023	Binary 0–127	Binary 8–2048	2.0/3.0	2.7–5.5V	16–pin DIP, SOP
3-15	MB87006A	10/17	Binary 5–1023	Binary 0–127	Binary 5–16383	2.5/3.5	3.0–6.0V	16–pin DIP, SOP
3-27	MB87014A	–/180	Binary 5–1023	Binary 0–63	Binary 5–65535	–/8.0	4.5–5.5V	16–pin DIP, SOP
3-37	MB87076	10/10	Binary 5–2047	Binary 0–127	Binary 5–16383	2.5/3.0	2.7–5.5V	16–pin DIP, SOP
3-49	MB87086A	–/95	Binary 5–1023	none	Binary 5–65535	–/8.0	4.5–5.5V	16–pin DIP, SOP
3-59	MB87087	10/17	Binary 5–1023	Binary 0–127	Binary 5–16383	2.5/3.5	3.0–6.0V	16–pin DIP, SOP
3-71	MB87091	300/–	Binary 5–4095	Binary 0–63	Binary 5–16383	8.0/–	2.7–3.3V	16–pin DIP, SOP, SSOP
3-89	MB87093A	–/145	725	none	64	–/10	4.5–5.5V	16–pin SSOP
3-99	MB87094	15@1.1V	Binary 5–2047	Binary 0–127	Binary 5–4095	1@1.1V	1.1–1.7V	16–pin SSOP
3-89	MB87095A	–/110	550	none	64	–/10	4.5–5.5V	16–pin SSOP
3-89	MB87096A	–/90	750	none	128	–/10	4.5–5.5V	16–pin SSOP

Sept. 1995
Edition 8.0a

FUJITSU

DATA SHEET

MB87001A
CMOS PLL FREQUENCY SYNTHESIZER

3

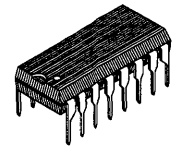
CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87001A, fabricated in CMOS technology, is a serial input PLL frequency synthesizer.

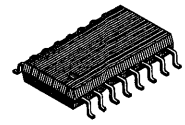
The MB87001A contains an inverter for connection to an external oscillator, a programmable reference divider, a divide factor of programmable reference divider control circuit, a phase detector, a charge pump, a 17-bit shift register, a 17-bit latch, a programmable divider (a binary 7-bit swallow counter, a binary 10-bit programmable counter), and a control generator for an external dual modulus prescaler.

When supplemented with a loop filter and VCO, the MB87001A contains the necessary circuitry to make up a Phase Locked Loop (PLL). Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1 GHz.

- Single power supply voltage: V_{DD} = 2.7V to 5.5V
- Wide temperature range: T_A = –40 to 85°C
- 13MHz typical input capability @5V (fin input)
- On-chip inverter for oscillator
- 8 divide factors for programmable reference divider is selected by S_1, S_2 and S_3 input (1/8, 1/16, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048)
- Programmable 17-bit divider with input amplifier consisting of: Binary 7-bit swallow counter Binary 10-bit programmable counter
- 2 type of phase detector output On-chip charge pump output Output for external charge pump
- Easy interface to Fujitsu dual modulus prescaler

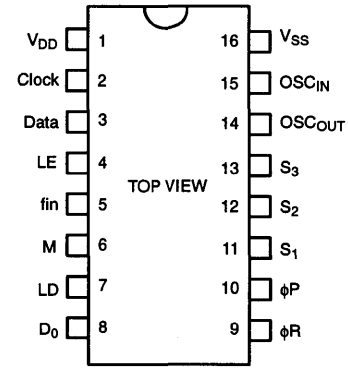


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



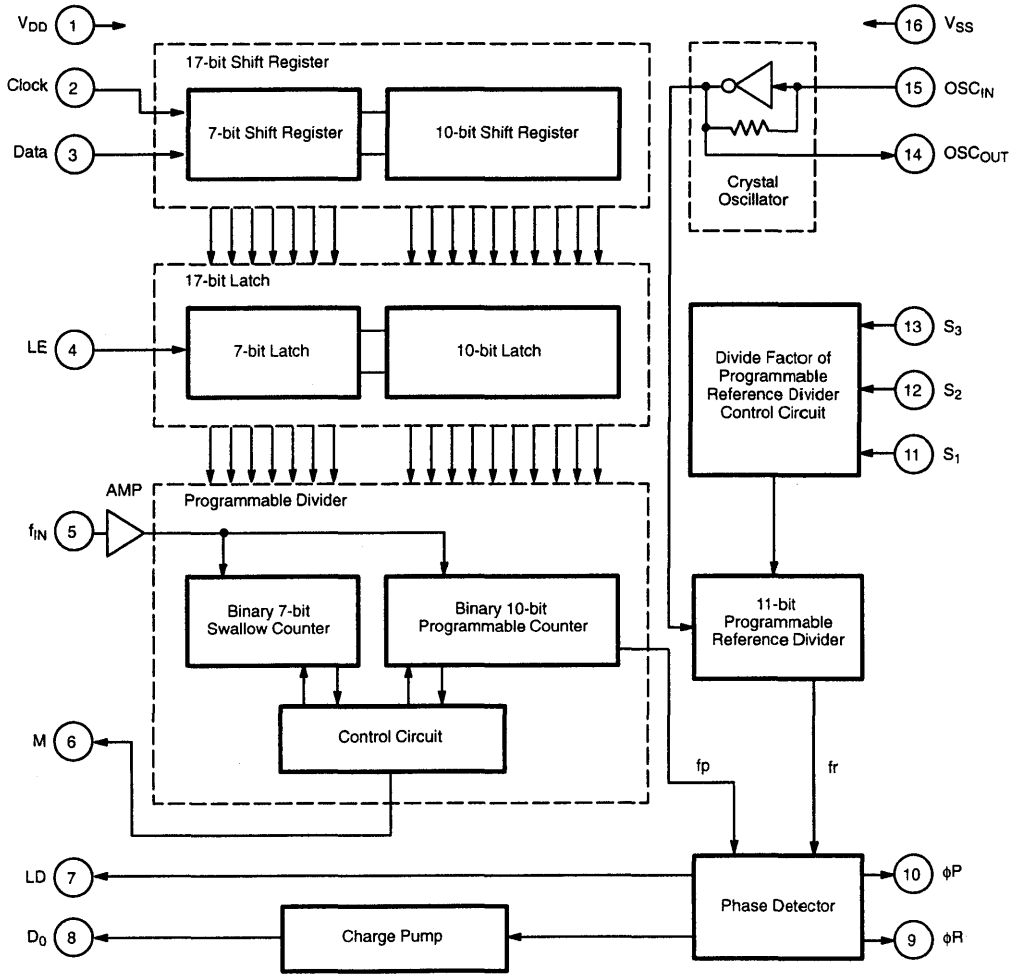
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE) (V_{SS} = 0V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Open-drain Output	V_{OOP}	V_{SS}–0.5 to V_{DD} +3.0	V
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB87001A BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	V_{DD}	–	Power supply voltage input
2	Clock	I	Clock signal input for 17-bit shift register Each rising edge of the clock shifts one bit of the data into the shift register
3	Data	I	Serial data input for 17-bit shift register The data is used for setting the divide factor of the programmable divider
4	LE	I	Load enable input When this pin is high level (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch.
5	f_{IN}	I	Input for programmable divider from VCO or prescaler output This input involves the bias circuit and amplifier. The connection with the external dual modulus prescaler should be an AC connection.
6	M	O	Control output for external dual modulus prescaler The connection to the prescaler should be a DC connection. This output level is synchronized with the falling edge of the f_{IN} input signal (pin #5). Pulse Swallow Function: MB501L M = High: Preset modulus factor 64 or 128 M = Low: Preset modulus factor 65 or 129
7	LD	O	Output of phase detector It is high level when fr and fp are equal, and then the loop is locked. Otherwise it outputs a negative pulse signal.
8	D_O	O	Three-state charge pump output of the phase detector The mode of D_O is changed by the combination of the programmable reference divider output frequency (fr) and the programmable divider output frequency (fp) as listed below: fr > fp: Drive mode (D_O = High level) fr = fp: High-impedance mode fr < fp: Sink mode (D_O = Low level)
9 10	ϕR ϕP	O O	Phase detector outputs for an external charge pump The mode of ϕR and ϕP are changed by the combination of the programmable reference divider output frequency (fr) and the programmable divider output frequency (fp) as listed below: ϕR ϕP fr > fp: Low Low fr = fp: Low High-Impedance fr < fp: High High-Impedance * ϕP is a N-channel open drain output
11 12 13	S_1 S_2 S_3	I I I	Control input for programmable reference divider The combination of these inputs provides 8 kinds of divide factor for the programmable reference divider.

Sn \ Divide Factor	1/8	1/16	1/64	1/128	1/256	1/512	1/1024	1/2048
S_1	0	1	0	1	0	1	0	1
S_2	0	0	1	1	0	0	1	1
S_3	0	0	0	0	1	1	1	1

14	OSC_{OUT}	O	Output pin for crystal oscillator Output of the inverting amplifier This pin should be open when an external oscillator is used.
15	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
16	V_{SS}	–	Ground

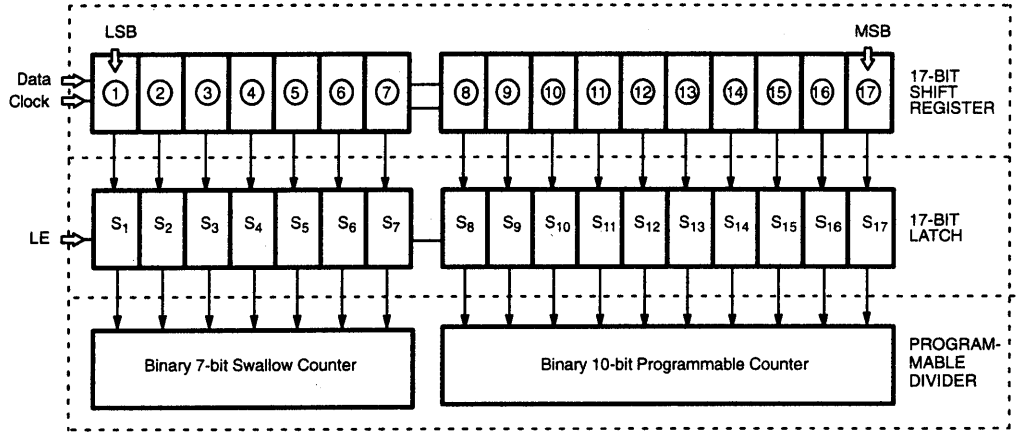
FUNCTIONAL DESCRIPTION

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data of binary code is input to the Data pin. These data are loaded into the 17-bit shift register from the MSB. When the load enable signal (LE) is high, the data stored in the 17-bit shift register is transferred to the 17-bit latch.

The data ① to ⑦ set a divide factor of the binary 7-bit swallow counter and data ⑧ to ⑰ set a divide factor of the binary 10-bit programmable counter. In other words, serial data is equivalent to the divide factor of programmable divider.

Fig. 2 – BLOCK DIAGRAM OF PROGRAMMABLE DIVIDER



Binary 7-bit Swallow Counter Data Input

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows:
Example MB501L
SW = H (64/65): Bit 7 of shift register (7) should be zero

Binary 10-bit Programmable Counter Data Input

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

Note: Divide factor less than 5 is prohibited
Divide factor N: 5 to 1023

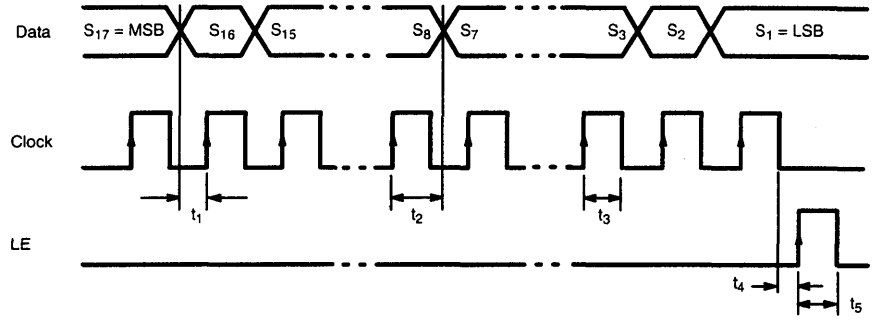
PULSE SWALLOW FUNCTION

$$f_{VCO} = [(N \times M) + A] \times fr$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler (e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit swallow counter (0 to 127)
fr : Output frequency of the programmable reference divider

TIMING CHART

• $t_1 - t_5 \geq 1\mu s$,



Clock : Clock signal input for the 17-bit shift register
Each rising edge of the clock shifts one bit of data into the shift register.

Data : Serial data input for the 17-bit shift register

LE : Load enable input
When LE is high (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch.
The 17-bit data is used for setting a divide factor of the programmable divider.

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7	–	5.5	V
Input Voltage	V_{IN}	V_{SS}	–	V_{DD}	V
Operating Temperature	T_A	–40	–	+85	°C

HANDLING PRECAUTIONS

- *This device should be transported and stored in anti-static containers.*
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = –40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	—	2.1	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	0.9	
Input Sensitivity	f_{IN}	Vf_{IN}	Amplitude in AC coupling, sine wave	0.8	—	—	V_{P-P}
	OCS_{IN}	V_{OSC}		1.0	—	—	
High-level Input Current	Except f_{IN} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	—	1.0	—	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	—	–1.0	—	
Input Current	f_{IN}	If_{IN}	$V_{IN} = V_{SS}$ to V_{DD}	—	±30	—	µA
	OCS_{IN}	I_{OSC}		—	±30	—	
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95	—	—	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	—	—	0.05	
Low-level Output Voltage	ϕP	V_{OLP}	I_{OL} = 0.8mA	—	—	0.8	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	2.50	—	—	
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	—	—	0.50	
High-level Output Current	Except ϕP and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	–0.5	—	—	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	0.5	—	—	
N–channel Open Drain Cut Off Current	ϕP	I_{OFF}	$V_O = V_{DD}$ +3.0V	—	1.0	—	µA
Power Supply Current*1		I_{DD}	—	—	2.0	—	mA
Max. Operating Frequency of Programmable Reference Divider		fMAXd	—	13	20	—	MHz
Max. Operating Frequency of Programmable Divider		fMAXp	—	10	20	—	MHz

Note: *1: f_{IN} = 5.0MHz, 12.8MHz crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are connected to ground except for f_{IN} and OSC_{IN}. Outputs are open.

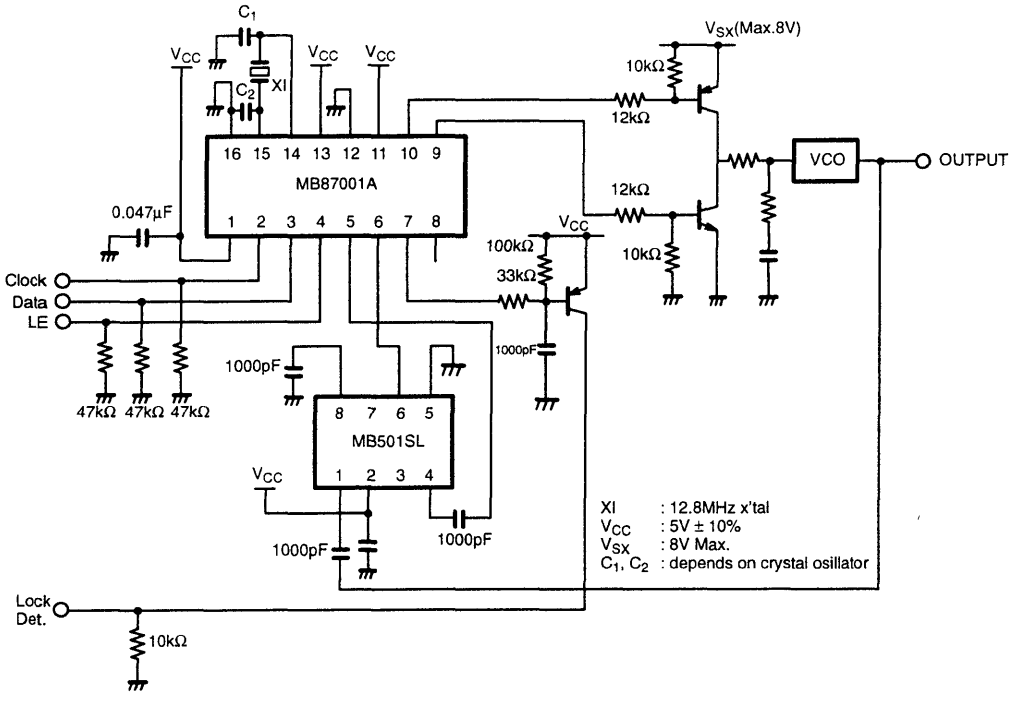
ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = –40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	—	3.5	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	1.5	
Input Sensitivity	f_{IN}	Vf_{IN}	Amplitude in AC coupling, sine wave	1.0	—	—	V_{P-P}
	OCS_{IN}	V_{OSC}		1.5	—	—	
High-level Input Current	Except f_{IN} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	—	1.0	—	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	—	–1.0	—	
Input Current	f_{IN}	If_{IN}	$V_{IN} = V_{SS}$ to V_{DD}	—	±50	—	µA
	OCS_{IN}	I_{OSC}		—	±50	—	
High-level Output Voltage	Except φP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95	—	—	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	—	—	0.05	
Low-level Output Voltage	φP	V_{OLP}	I_{OL} = 0.8mA	—	—	1.0	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	4.50	—	—	
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	—	—	0.50	
High-level Output Current	Except φP and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	–1.0	—	—	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	1.0	—	—	
N–channel Open Drain Cut Off Current	φP	I_{OFF}	$V_O = V_{DD}$ +3.0V	—	1.0	—	µA
Power Supply Current*1		I_{DD}	—	—	2.0	—	mA
Max. Operating Frequency of Programmable Reference Divider		fMAXd	—	15	25	—	MHz
Max. Operating Frequency of Programmable Divider		fMAXp	—	13	25	—	MHz

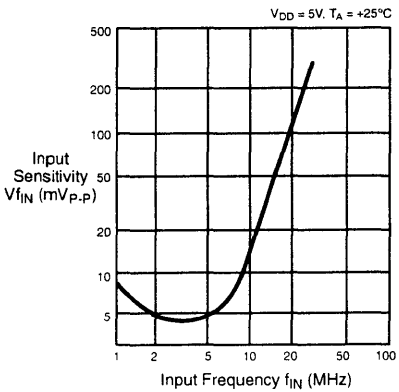
Note: *1: f_{IN} = 5.0MHz, 12.8MHz crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are connected to ground except for f_{IN} and OSC_{IN}. Outputs are open.

Fig. 3 –TYPICAL APPLICATION EXAMPLE

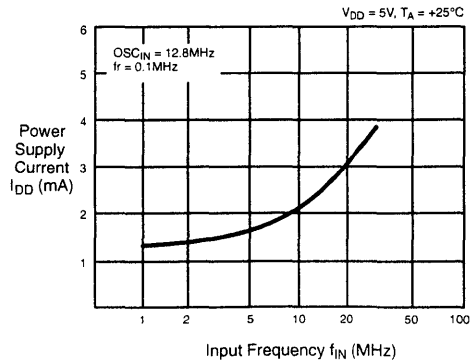


TYPICAL CHARACTERISTICS CURVES

Inupt Sensitivity vs. Input Frequency (fin Section)

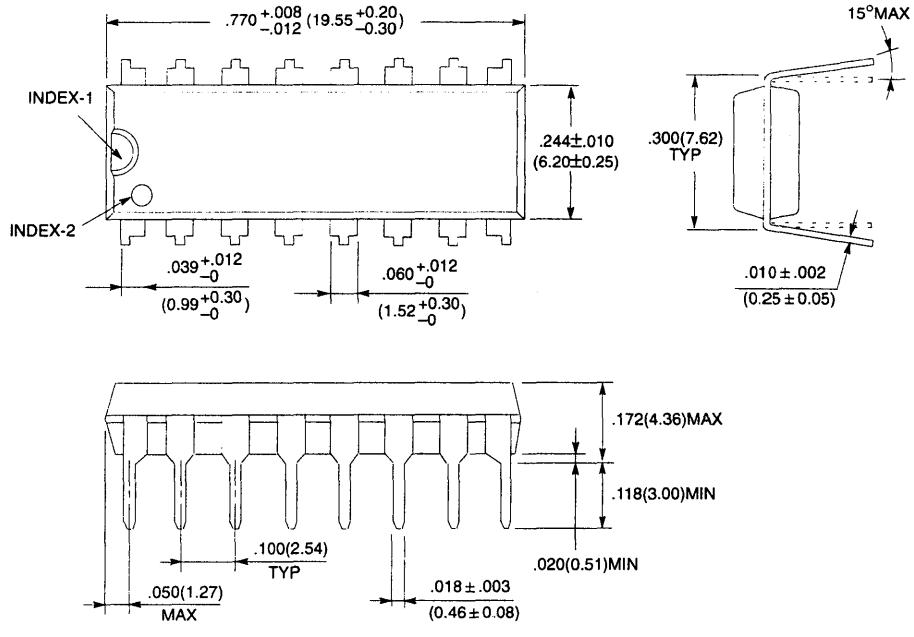


Power Supply Current vs. Input Frequency



PACKAGE DIMENSIONS

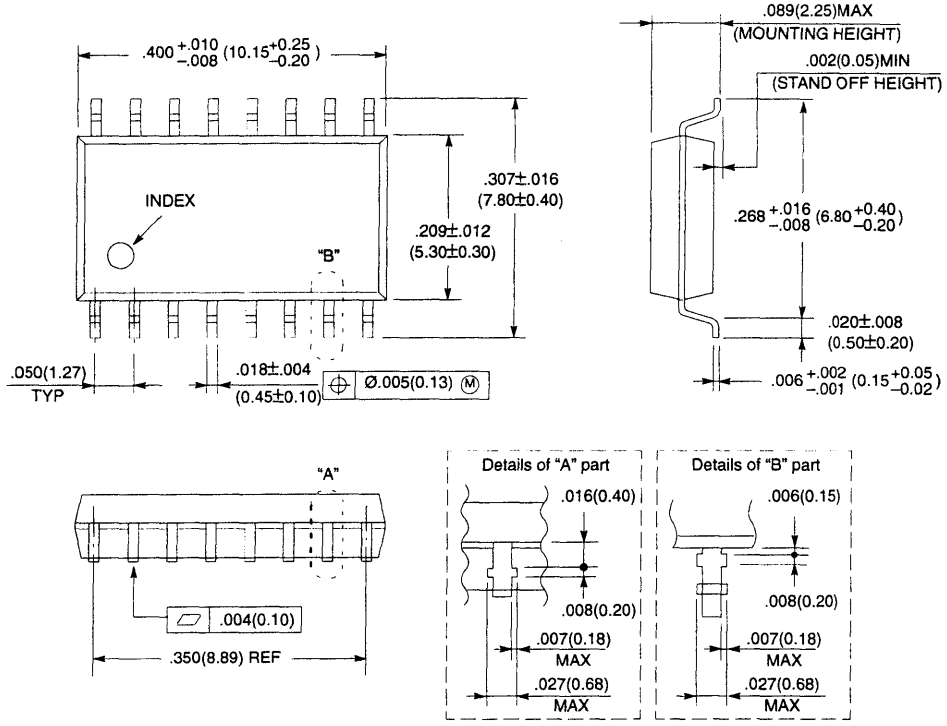
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

DS04–21204–6aE

FUJITSU

DATA SHEET

MB87006A *Frequency Synthesizer*

CMOS Serial Input Phase Locked Loop (PLL)

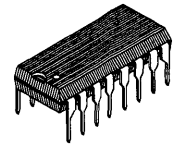
3

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

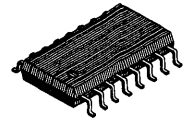
The Fujitsu MB87006A, fabricated in CMOS technology, is a serial input Phase Locked Loop (PLL) frequency synthesizer.

The MB87006A contains an inverter for connection to an external oscillator, programmable reference divider (binary 14-bit programmable reference counter), 14-bit shift register, 14-bit latch, phase detector, charge pump, 17-bit shift register, 17-bit latch, programmable divider (binary 7-bit swallow counter, binary 10-bit programmable counter) and control generator for dual modulus prescaler.
When supplemented with a loop filter and VCO, the MB87006A contains the necessary circuitry to make up a Phase Locked Loop (PLL). Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1GHz.

- Wide range power supply voltage: V_{CC} = 3.0 to 6.0V
- Wide temp range: Ta = –40 to 85°C
- 17MHz typical input capability @5V (fin input)
- On-chip inverter for oscillator
- Programmable divider with input amplifier consisting of:
  - Binary 7-bit swallow counter
  - Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of:
  - Binary 14-bit programmable reference counter
- Divide factor of programmable divider and programmable reference divider are set by serial data input (The last data bit is a control bit)
- 2-types of phase detector output
  - On-chip charge pump output
  - Output for external charge pump
- Easy interface with Fujitsu prescalers
- 16-pin standard dual-in-line package (Suffix: -P)
  16-pin standard flat package (Suffix: -PF)

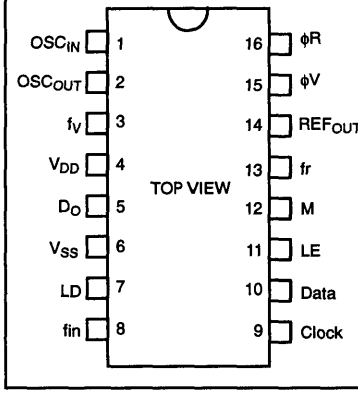


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



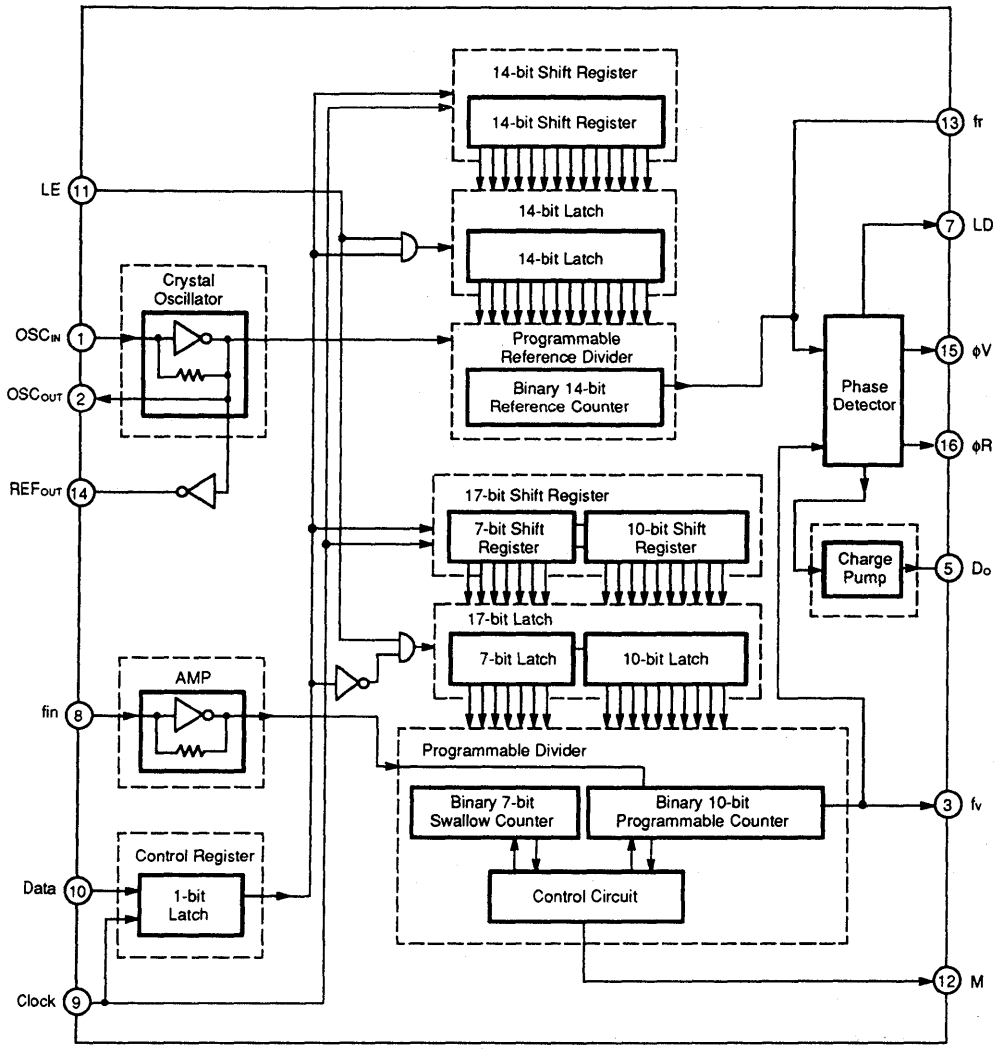
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Operating Temperature	Ta	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB87006A BLOCK DIAGRAM



PIN DESCRIPTION

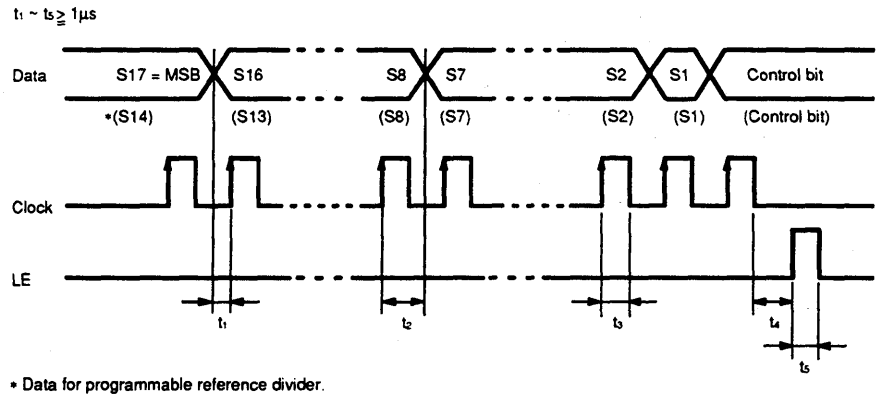
Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.
3	f_V	O	Monitor output of the phase detector. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_O	O	Three-state charge pump output of phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Drive mode (D_O = High level) $f_r = f_V$: High impedance $f_r < f_V$: Sink mode (D_O = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are equal, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	fin	I	Clock input for programmable divider. This input contains internal bias circuit and amplifier. The connection with an external dual-modulus prescaler should be an AC connection.
9	Clock	I	Clock signal input for 17-bit shift register and 14-bit shift register. Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for programmable divider and programmable reference divider. The last bit of the data is the control bit. Control bit determines which latch is activated. The data stored in the shift register is transferred to the 14-bit latch when the bit is high, and to 17-bit latch when low.
11	LE	I	Load enable input with internal pull up resistor. When this pin is high (active high), the data stored in shift register is transferred to 14-bit latch or 17-bit latch depending on the control bit data.
12	M	O	Control output for an external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of fin input signal (pin #8). Pulse swallow function: e.g. MB501L: M = High: Preset modulus factor 64 or 128 M = Low Preset modulus factor 65 to 129

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
13	fr	O	Monitors output of phase detector input. This pin is tied to the programmable reference divider output.
14	REF_{OUT}	O	Monitor output pin of the reference frequency. This output can be used as system clock for microprocessor, or reference oscillator for another PLL frequency synthesizer.
15 16	ϕV ϕR	O O	Output for external charge pump. The mode of ϕR and ϕV are changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency f_V as listed below. ϕR ϕV fr > f_V: Low-level HIgh-level fr = f_V: High-level High-level fr < f_V: High-level Low-level

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT TIMING



* Data for programmable reference divider.

Notes: Data: Serial data input is used for setting divide factor of programmable reference divider and programmable divider.
Data is input from MSB, and last bit data is a control bit.
Control bit is set high when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Data is input to internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data stored in shift register is transferred to 14-bit latch, or 17-bit latch depending on the control bit setting.

PULSE SWALLOW FUNCTION

$$f_{VCO} = [(N \times M) + A] \times f_{OSC} + R \quad (N > A)$$

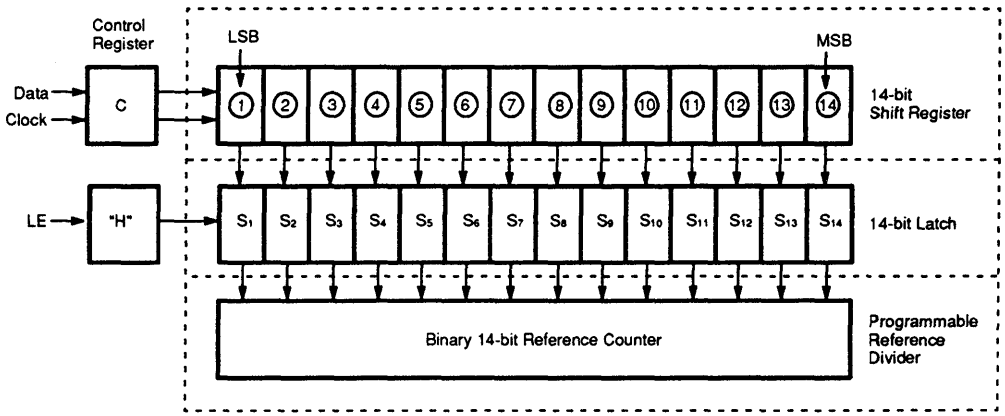
f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler
(e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit programmable counter (0 to 127, A < N)
f_{OSC} : Output frequency of external oscillator
R : Preset divide factor of binary 14-bit programmable reference counter (5 to 16383)

3

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

Serial data consists of 14-bit data, which is used for setting divide factor of programmable reference counter, and 1-bit control data. In this case, control bit is set high level.

The data format is shown below.



BINARY 14-BIT REFERENCE COUNTER DATA INPUT

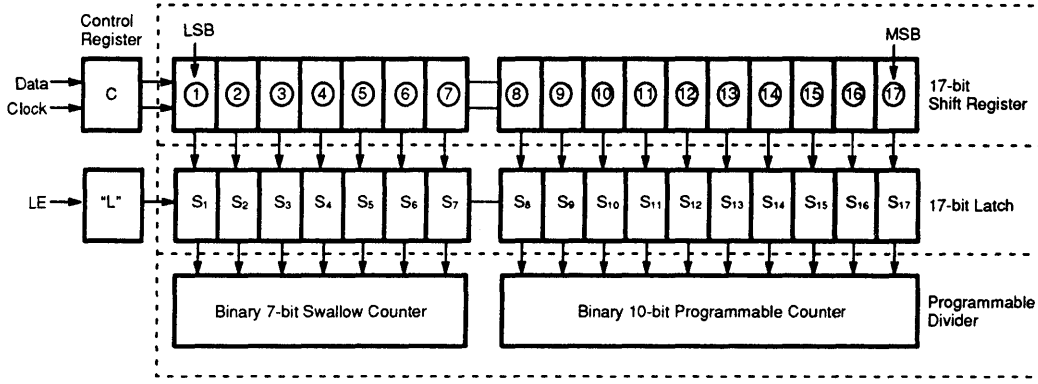
⑭	⑬	⑫	⑪	⑩	⑨	⑧	⑦	⑥	⑤	④	③	②	①	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	16383

Note: Divide factor less than 5 is prohibited.
Divide factor : 5 to 16383

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data consists of 17-bit data, which is used for setting divide factor of programmable divider, and 1-bit control data. In this case, control bit is set low level. The data ① to ⑦ set a divide factor of 7-bit swallow counter and data ⑧ to ⑰ set divide factor of 10-bit programmable counter.

The data format is shown below.



BINARY 7-BIT SWALLOW COUNTER DATA INPUT

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

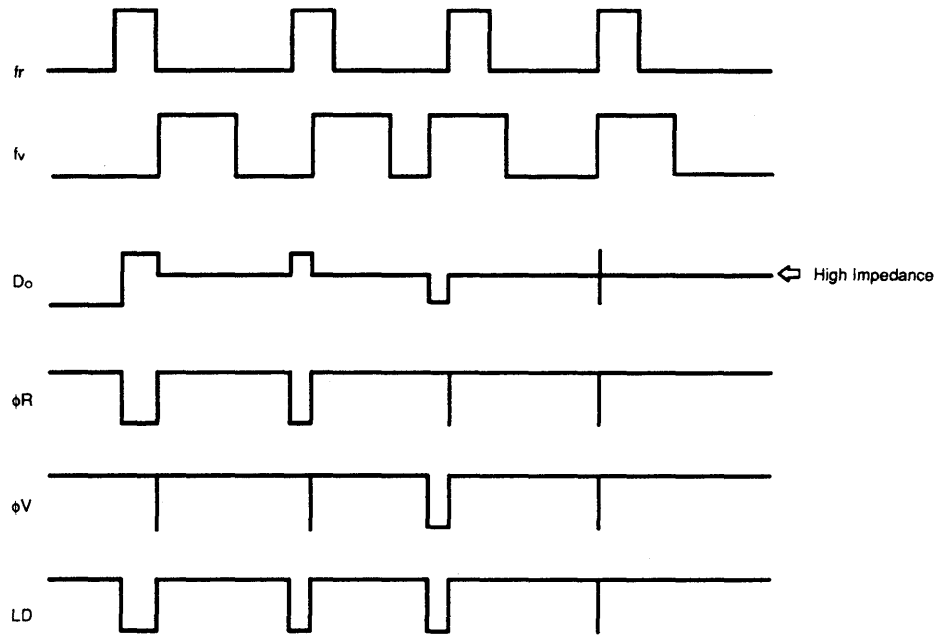
Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
e.g. MB501L (÷65/65)prescaler
SW = H (64/65): Bit 7 to shift register ⑦ should be zero.

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

Note: Divide factor less than 5 is prohibited.
Divide factor N : 5 to 1023

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	3.0		6.0	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	Vsin		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		–1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±30		µA
	OSC_{IN}	I_{OSC}	V_{IN} = V_{SS} to V_{DD}		±30		µA
	LE	I_{LE}	V_{IN} = V_{SS}		–40		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 2.6V	–0.5			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	0.5			
High-level Output Current	M	I_{OHM}	V_{OH} = 2.6V	–0.7			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	1.5			
Power Supply Current *1		I_{DD}			2.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	20		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		10	20		MHz

Notes: *1: fin = 8.0MHz 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are grounded except for fin and OSC_{IN}. Output are open.

ELECTRICAL CHARACTERISTICS (continued)

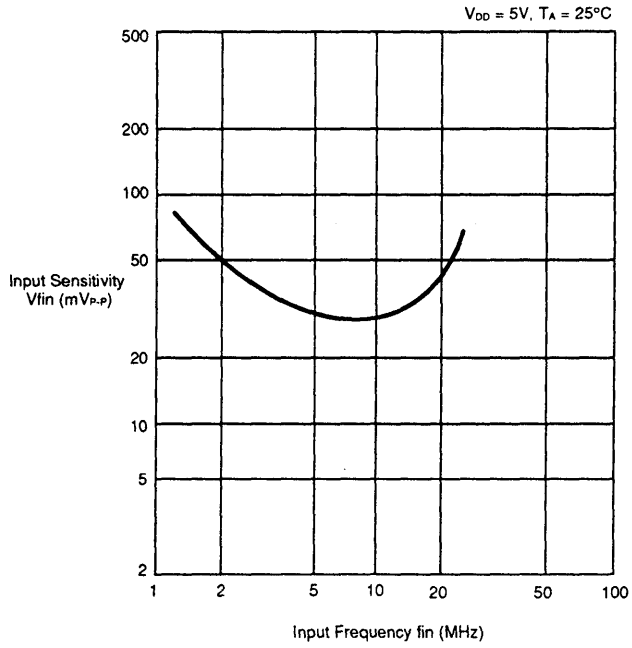
(V_{DD} = 5.0V, V_{SS} = 0V, T_A = −40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	Vsin		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		−1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±50		µA
	OSC_{IN}	Iosc	V_{IN} = V_{SS} to V_{DD}		±50		µA
	LE	I_{LE}	V_{IN} = V_{SS}		−60		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	−1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
High-level Output Current	M	I_{OHM}	V_{OH} = 4.6V	−1.5			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	3.0			
Power Supply Current *1		I_{DD}			3.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	25		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		17	25		MHz

Note: *1. fin = 8.0MHz, 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}
Inputs are ground except for fin and OSC_{IN}. Outputs are open.

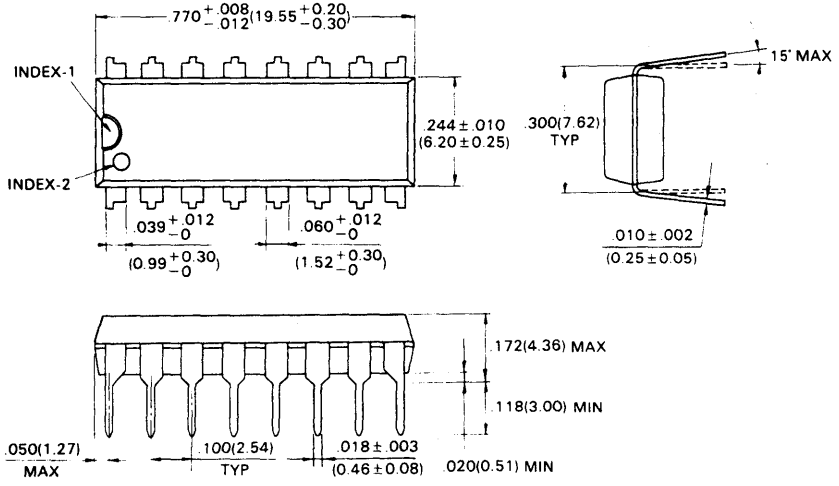
TYPICAL CHARACTERISTICS CURVE

INPUT SEVSITIVITY CHARACTERISTICS (fin Section)



PACKAGE DIMENSIONS

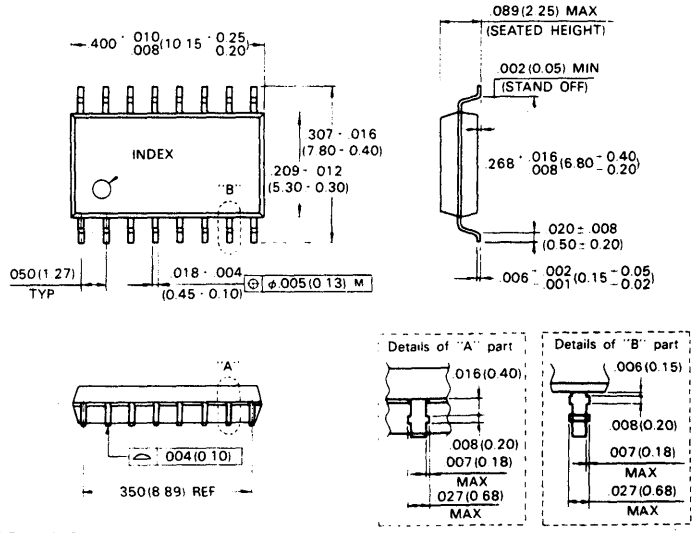
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

DS04–21305–3aE

FUJITSU

DATA SHEET

MB87014A *ASSP*

CMOS PLL Frequency Synthesizer

3

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87014A, fabricated in advanced CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer with an on chip 180MHz dual modulus prescaler.

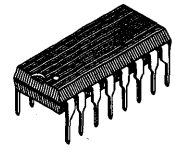
The MB87014A contains a dual modulus prescaler, inverter for an external oscillator, programmable reference divider, control circuit, phase detectors, charge pump, programmable divider (binary 6-bit swallow counter and binary 10-bit programmable counter).

The MB87014A can make up PLL frequency synthesizer operating up to 180MHz.

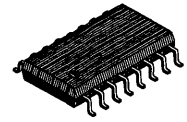
- Single Power Supply Voltage: V_{DD} = 4.5V to 5.5V
- Wide Temperature Range: Ta = –30 to 60°C
- 180MHz input capability @5V (fin input)
- On-chip Inverter for oscillator
- Programmable divider with input amplifier consisting of;
  Binary 6-bit swallow counter
  Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of;
  Binary 16-bit programmable reference counter
- Divide factor of programmable divider and programmable reference divider are set by serial data input. (The last data bit is a control bit.)
- 3-type of phase detector outputs
  On-chip charge pump output for active LPF
  On-chip charge pump output for passive LPF
  Output for external charge pump
- 16-pin Standard Dual-in-line Package (Suffix: -P)
  16-pin Standard Flat Package (Suffix: -PF)
- Pulse Swallow Function

$f_{VCO} = [(N \times M) + A] \times (f_{OSC} \div R)$ $(N > A)$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of internal dual modulus prescaler (64/65)
A : Preset divide factor of binary 6-bit swallow counter (0 to 63)
f_{OSC} : Output frequency of the external oscillator
R : Preset divide factor of binary 16-bit programmable reference counter (5 to 65535)

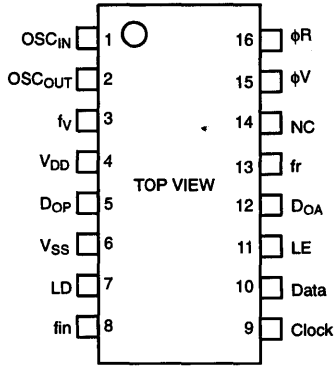


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



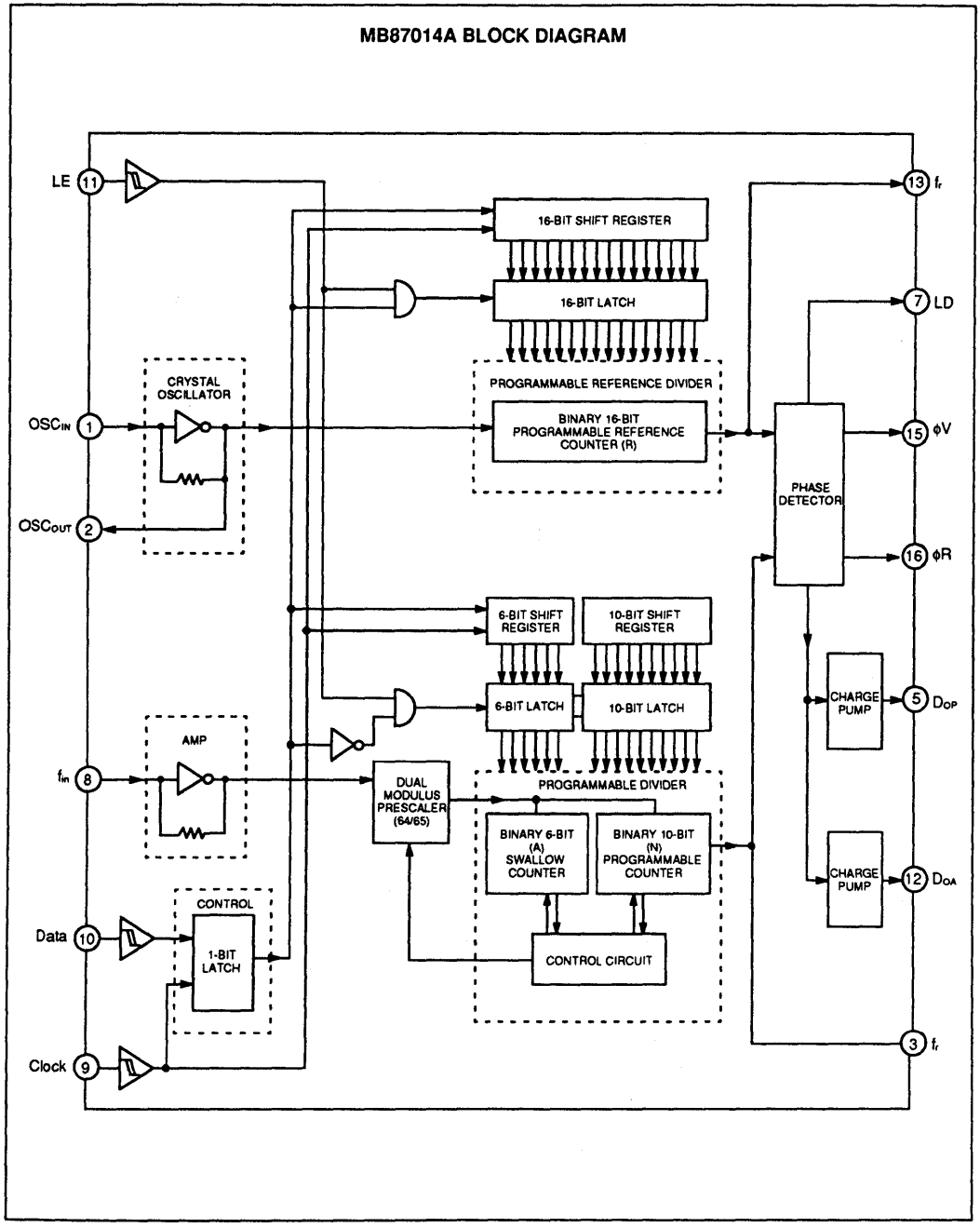
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.3 to V_{SS} +6.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Output Voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Output Current	I_{OUT}	±10	mA
Operating Ambient Temperature	Ta	–30 to +80	°C
Storage Temperature	T_{STG}	–40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB87014A BLOCK DIAGRAM



PIN DESCRIPTION

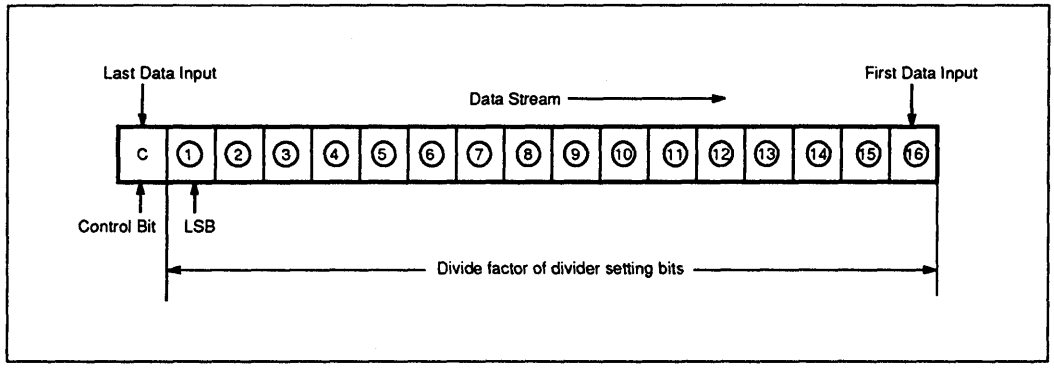
Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be left open when an external oscillator is used.
3	f_V	O	Monitor pin for the phase detector input. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_{OP}	O	Output pin for low pass filter (Passive type). The mode of D_{OP} is changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Drive mode (D_{OP} = High level) $f_r = f_V$: High-impedance $f_r < f_V$: Sink mode (D_{OP} = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when f_r and f_V are coherent, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	f_{in}	I	Frequency input to an internal prescaler from VCO. The connection with VCO should be AC connection.
9	Clock	I	Clock signal input for shift registers. Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	I	Serial data input for shift registers. The last bit of the data is the controlbit The control data determines which latch is activated.
11	LE	I	Load enable input. When this pin is high, the data from shift register is latched into programmable reference divider or programmable divider depending upon a control bit setting.
12	D_{OA}	O	Output pin for low pass filter (Active type). The mode of D_{OA} is changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Sink mode (D_{OA} = Low level) $f_r = f_V$: High-impedance $f_r < f_V$: Drive mode (D_{OA} = High level)
13	f_r	O	Monitor pin for the phase detector input. This pin is tied to the programmable reference divider output.
14	NC	–	No connection.
15 16	ϕV ϕR	O O	Output pins for low pass filter (differential filter type). Outputs for external charge pump are changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below. ϕV ϕR $f_r > f_V$: High level Low level $f_r = f_V$: High level High level $f_r < f_V$: Low level High level

3

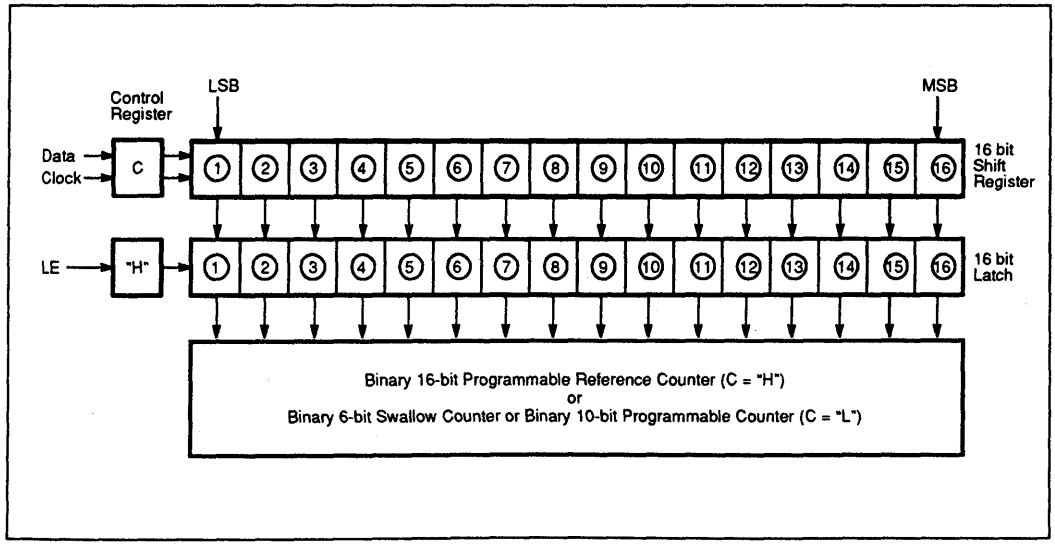
FUNCTIONAL DESCRIPTIONS

DIVIDE FACTOR OF DIVIDER

Serial data of binary code is input to Data pin. On rising edge of clock shifts one bit of data into the shift registers. Input data consists of 16-bit data and 1-bit of control data. The control data determines which latch is activated. When control bit is high, 16-bit latch is selected. When low, 6-bit latch and 10-bit latch is selected.



The serial data is input to 16-bit shift registers and 1-bit control register. When load enable is high, the data from the shift register is latched into the programmable reference divider (binary 16-bit programmable reference counter) or programmable divider (binary 6-bit swallow counter and binary 10-bit programmable counter) depending upon a control bit setting.



FUNCTIONAL DESCRIPTIONS (Continued)

BINARY 6-BIT SWALLOW COUNTER DATA INPUT

Divide Factor	①	②	③	④	⑤	⑥
0	0	0	0	0	0	0
1	1	0	0	0	0	0
2	0	1	0	0	0	0
. .	. .	. .	. .	. .	. .	. .
63	1	1	1	1	1	1

• Divide factor A: 0 to 63

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

Divide Factor	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮	⑯
5	1	0	1	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0
7	1	1	1	0	0	0	0	0	0	0
. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .
1023	1	1	1	1	1	1	1	1	1	1

• Divide factor N: 5 to 1023
• Divide factor less than 5 is prohibited.

BINARY 16-BIT PROGRAMMABLE COUNTER DATA INPUT

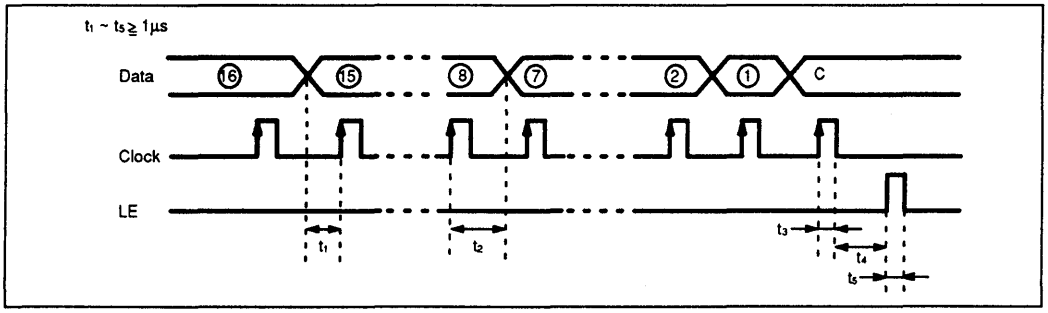
Divide Factor	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮	⑯
5	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .
65535	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

• Divide factor R: 5 to 65535
• Divide factor less than 5 is prohibited.

STAND-BY MODE

When all zero of 16-bit serial data is input, the MB87014A goes to stand-by mode. During stand-by mode, internal circuit stops operation and f_{in} and OSC_{IN} are forced to high level. Thus, low supply current is achieved. Stand-by down mode is release, when the data except all zero data is input.

SERIAL DATA INPUT TIMING

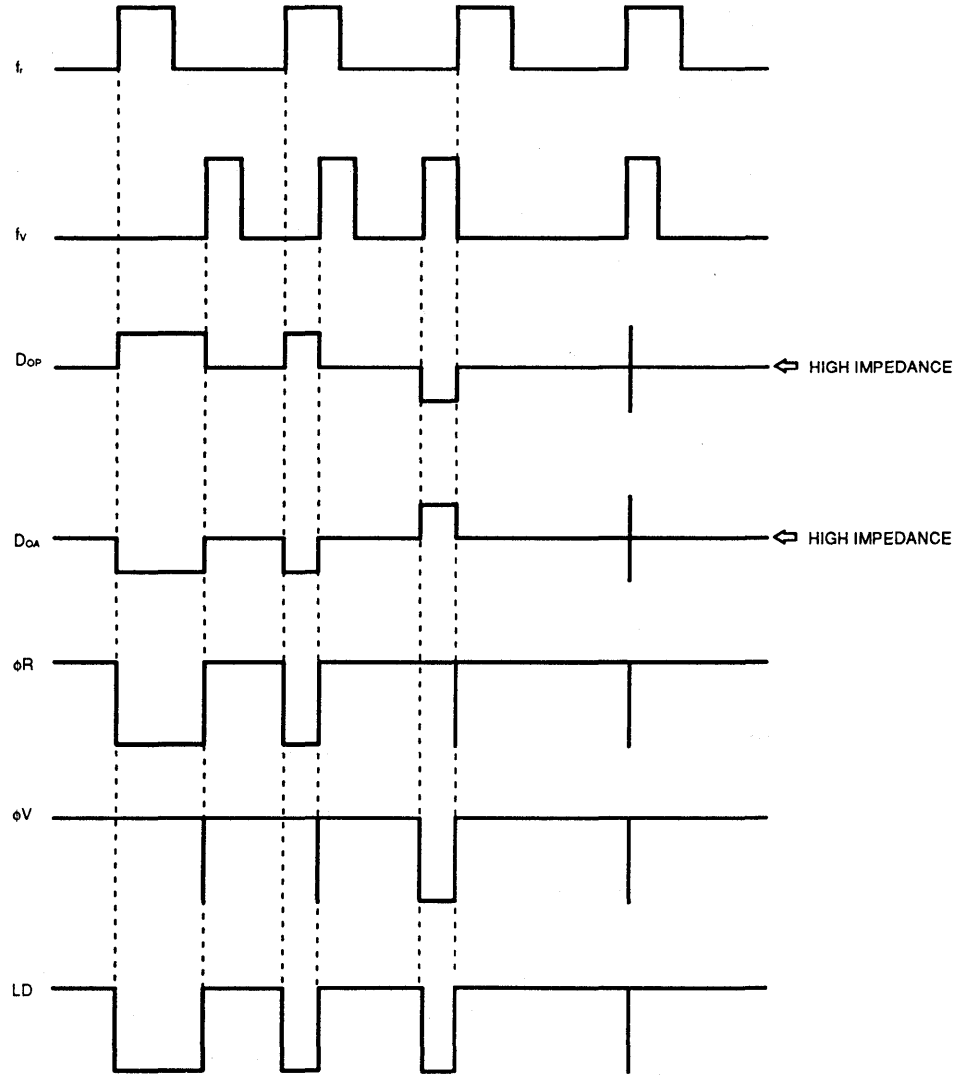


Notes: Data: Serial data input is used for setting divide factor of programmable reference divider or programmable divider.
Data is input from MSB and last bit data is control bit.
Control bit is high level when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Clock input for 16-bit shift registers and control register. Data is input into internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data from shift register is latched into programmable reference divider or programmable divider depending upon the control bit setting.

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	−30		+60	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 5V, T_A = −30 to 60°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	f_{in}	V_{fpp}	Amplitude in AC coupling, Sine wave	1.0			V_{P-P}
	OSC_{IN}	V_{sin}		1.0			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IH} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IL} = V_{SS}$		−1.0		
Input Current	f_{in}	I_{fin}	$V_{IN} = V_{SS}$ to V_{DD}		±50		µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	−1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
Power Dissipation*1		I_{DDP}			8.0		mA
Stand-by Current*2		I_{DDS}			100		µA
Maximum Operating*3 Frequency	REF Section	f_{maxd}		40	60		MHz
	PD Section	f_{maxp}		180	250		MHz

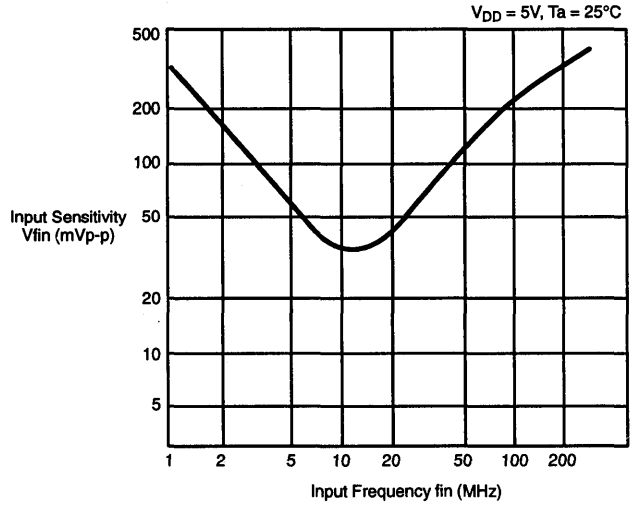
Notes: *1: f_{in} = 180MHz, 22MHz cystal is connected between OSC_{IN} and OSC_{OUT} pins.
Inputs are grounded except f_{in} and OSC_{IN}. Outputs are open.

*2 All serial data is set to zero. Input are grounded except f_{in} and OSC_{IN}. Output are open.

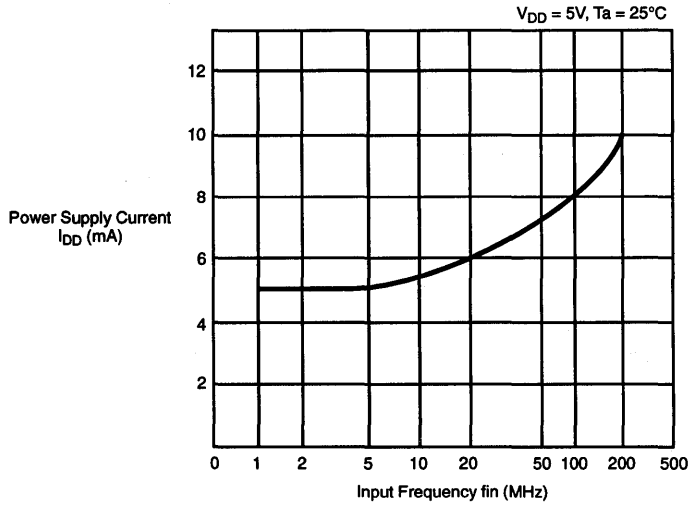
*3 REF Section :Maximum operating frequency of programmable reference divider.
PD Section :Maximum operating frequency of programmable divider.

TYPICAL CHARACTERISTICS CURVES

Input Sensitivity vs. Input Frequency (fin Section)

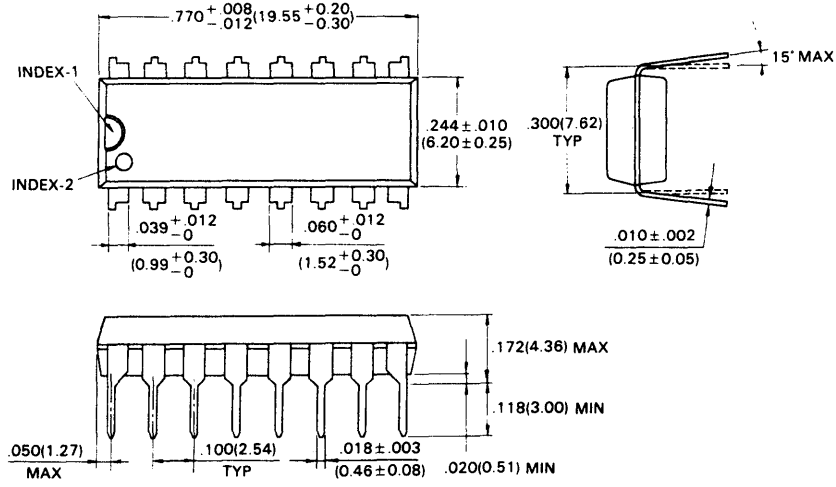


Power Supply Current vs. Input Frequency



PACKAGE DIMENSIONS

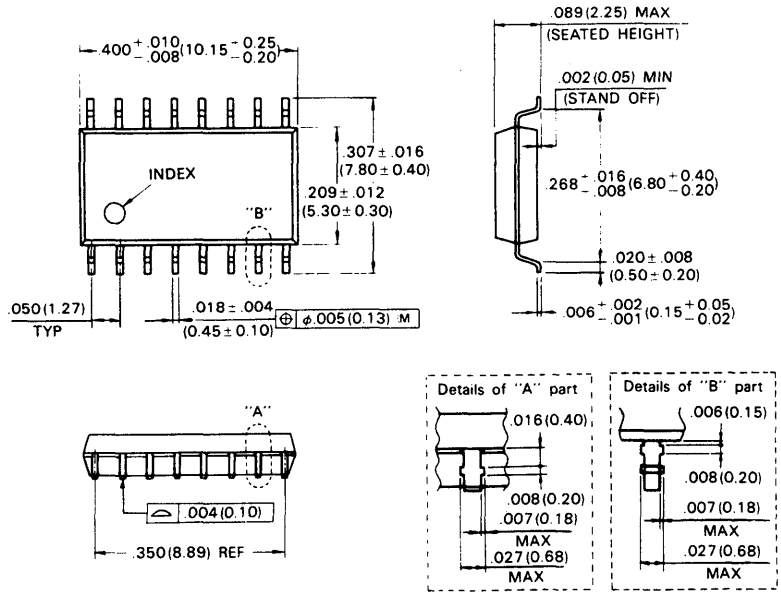
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

DS04–21203–4E

FUJITSU

DATA SHEET

MB87076

CMOS PLL FREQUENCY SYNTHESIZER

3

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER WITH POWER DOWN MODE

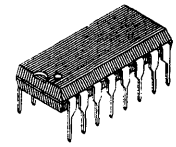
The Fujitsu MB87076, fabricated in CMOS technology, is a serial input PLL frequency synthesizer that features a power down mode.

The MB87076 contains an inverter for the oscillator, 14-bit shift register, 18-bit shift register, 1-bit control register, 14-bit latch, 18-bit latch, programmable divider (binary 11-bit programmable counter and binary 7-bit swallow counter), programmable reference divider (binary 14-bit programmable reference counter), phase detector, charge pump, control generator for two modulus prescaler, and power down circuit.

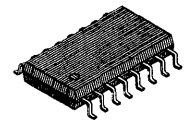
The MB87076 selects either operation mode or power down mode, depending on the PS input signal level. When the device begins operation, phase f_r and f_V are synchronized.

- Single power supply voltage: V_{DD} = 2.7 to 5.5V
- Wide temperature range: T_A = –40 to +85°C
- Low power supply current: 3mA typ, (100µA in power down mode)
- On-chip inverter for oscillator
- Programmable reference divider with input amplifier
  Programmable divider with input amplifier
- 2 Types of phase detector output
  - On-chip charge pump output
  - Output for external charge pump
- On-chip power down circuit
- 16-pin standard dual-in-line package (Suffix: -P)
  16-pin standard flat package (Suffix: -PF)
- Pulse swallow function

  f_{VCO} = [(N x M) +A] x f_{OSC} ÷ R
  f_{VCO} : VCO (Voltage Controlled Oscillator) output frequency
  N : Preset divide factor of binary 11-bit programmable counter (16 to 2047)
  M : Preset modulus factor of external two modulus prescaler (64 in 64/65 mode, 128 in 128/129 mode)
  A : Preset divide factor of binary 7-bit swallow counter (0 to 127)
  f_{OSC} : Output frequency of an external oscillator
  R : Preset divide factor of binary 14-bit programmable reference counter (8 to 16383)

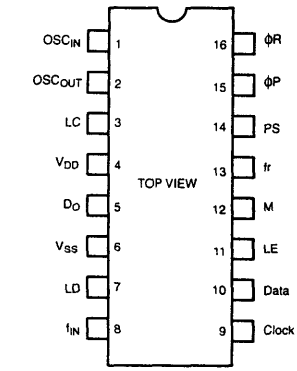


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



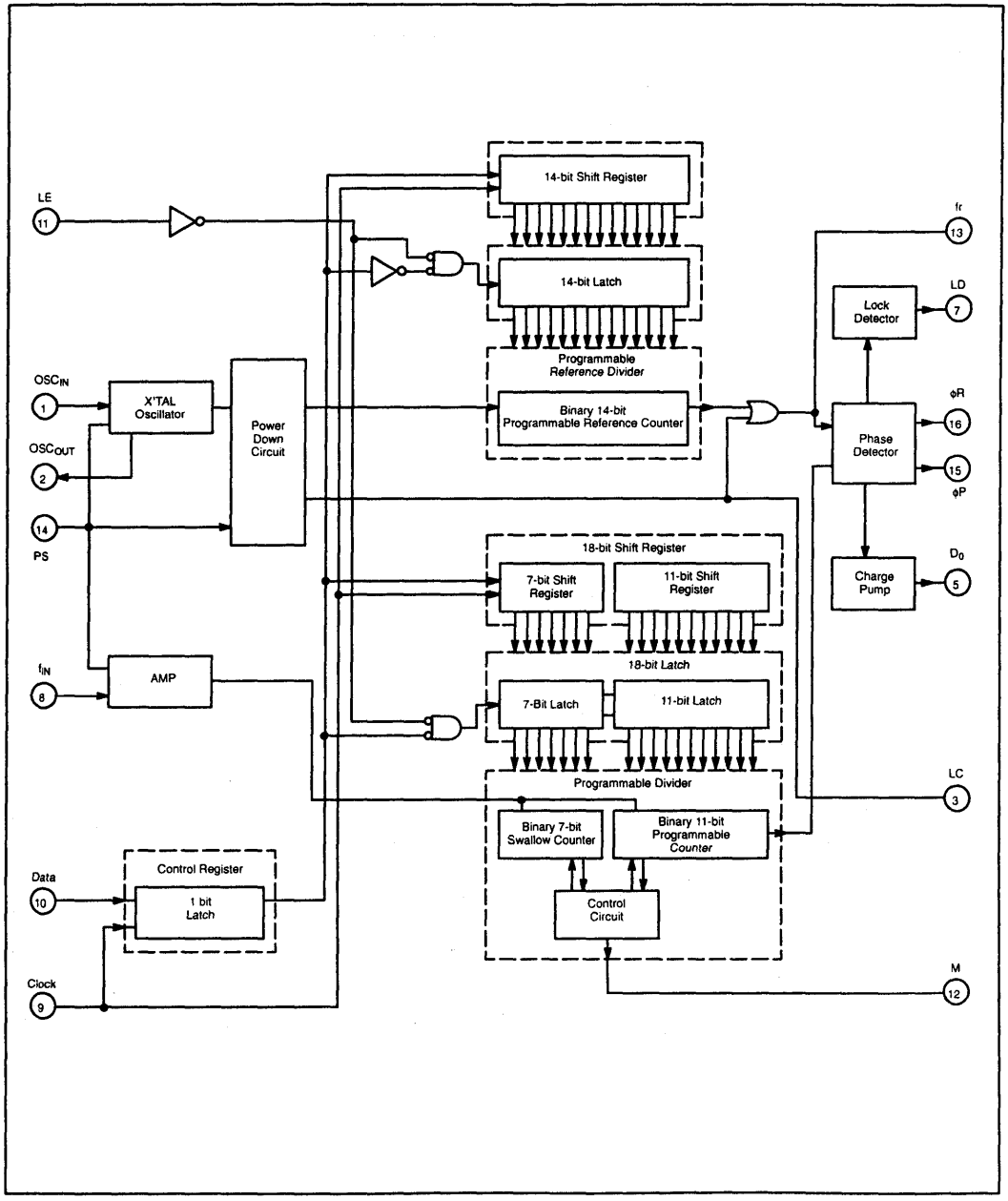
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Open Drain Output	V_{OP}	V_{SS} –0.5 to V_{DD} +3.0	V
Operating Temperature	Ta	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

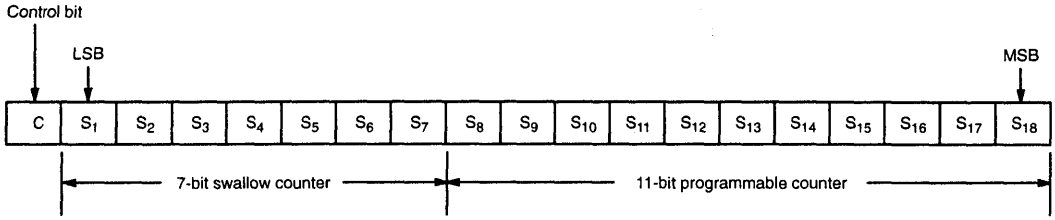
Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Pin for crystal oscillator The input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as an AC coupling when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Pin for crystal oscillator The output of the inverting amplifier. This pin should be connected to ground when an external oscillator is used.
3	LC	O	Output pin for loop control signal This pin is at high level when the operation mode is selected. It is at low level when the power down mode is selected.
4	V_{DD}	–	Power supply voltage
5	D_O	O	Three-state charge pump output The mode of D_O is changed by the combination of the programmable reference divider output frequency (f_r) and the programmable divider output frequency (f_P) as listed below: $f_r > f_P$: D_O = H level $f_r = f_P$: D_O = High-impedance level $f_r < f_P$: D_O = L level
6	V_{SS}	–	Ground
7	LD	O	Output of phase comparator This pin is at low level when f_r and f_P are coherent, and then the loop is locked. Otherwise it outputs high level.
8	f_{IN}	I	Input for binary 7-bit swallow counter and binary 11-bit programmable counter from VCO This input involves the bias circuit and the amplifier. The connection with the dual modulus prescaler should be an AC connection.
9	Clock	I	Clock signal input for 18-bit shift register and 14-bit shift register Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for shift registers This data is the divide ratio of the divider, which is provided from the corresponding shift register. The last bit of the data is the control bit which specified the destination of the shift register. The data is transferred to the 14-bit shift register when the bit is at high level, and to the 18-bit shift register when it is at low level.
11	LE	I	Load enable input When this pin is at high level, the data latched from the shift register is transferred to the programmable reference divider or the programmable divider, depending on the control bit data.
12	M	O	Control output for external dual modulus prescaler The connection should be a DC connection. Pulse swallow function: (Example) MB501: M = High: Preset modules factor 64 or 128 M = Low: Preset modules factor 65 or 129
13	f_r	O	Monitors output of the phase comparator input Also monitors the output of the reference divider.
14	PS	I	Power down control input When this pin is at high level, the operation mode is selected. When this pin is at low level, the power down mode is selected.
15 16	ϕP ϕR	O O	Output for external charge pump ϕR ϕP $f_r > f_P$: Low Low $f_r = f_P$: Low High-impedance $f_r < f_P$: High High-impedance

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT FOR PROGRAMMABLE DIVIDER

Binary serial data is input to the Data pin. Each rising edge of the clock shifts one bit of the data into the shift registers and the control register. Input data consists of 18-bit data and 1-bit of the control bit data. In this case, the control bit is set at low level. S_1 to S_7 is used for setting the divide ratio of the 7-bit swallow counter and S_8 to S_{18} is used for setting the divide ratio of the 11-bit programmable counter.

The data format is shown below.



7-bit Swallow Counter Data Input

Divide Factor A	S_7	S_6	S_5	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide factor: 0 to 127

11-bit Programmable Divider Data Input

Divide Factor N	S_{18}	S_{17}	S_{16}	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

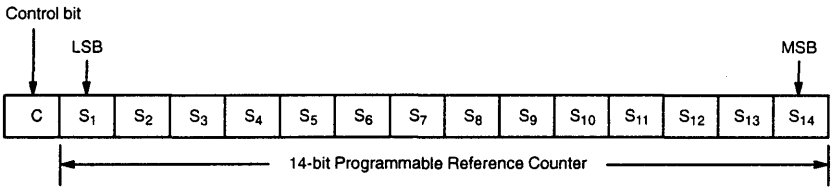
Note: Divide factor less than 5 is prohibited
Divide factor: 5 to 2047

FUNCTIONAL DESCRIPTION (Continued)

SERIAL DATA INPUT FOR PROGRAMMABLE REFERENCE DIVIDER

Binary serial data is input to the Data pin. Each rising edge of the clock shifts one bit of the data into the shift registers and control register. Input data consists of 14-bit data and 1-bit of the control bit data. In this case, the control bit is set at high level.

The data format is shown below.

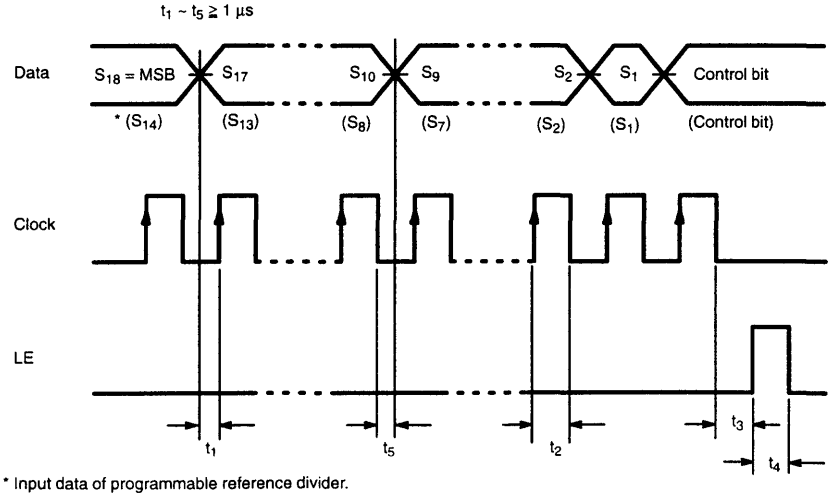


14-bit Programmable Divider Data Input

Divide Factor R	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

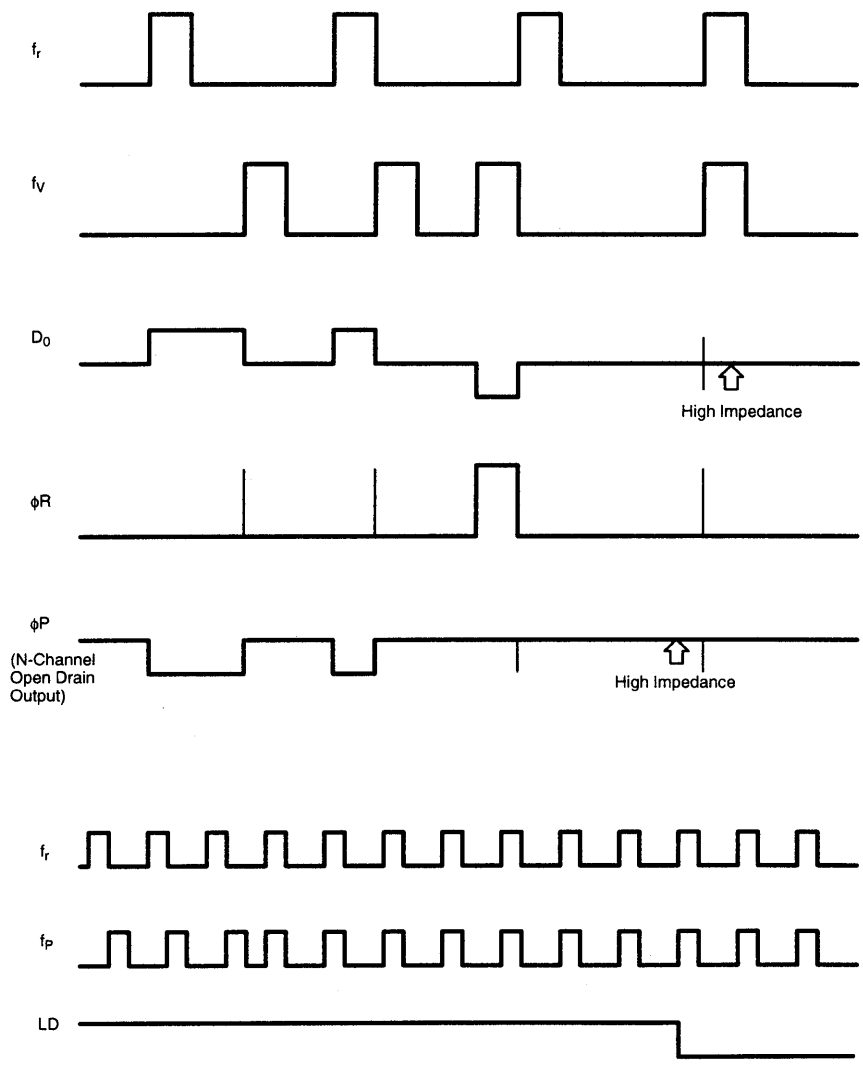
Note: Divide factor less than 8 is prohibited
Divide factor: 8 to 16383

Fig. 1 – SERIAL DATA INPUT TIMING



* Input data of programmable reference divider.

Fig. 2 – PHASE DETECTOR WAVEFORM



Note: LD is set at High level when $f_r \neq f_V$ (unclock condition).
LD is set at Low level when $f_r = f_V$ (lock condition).

POWER DOWN OPERATION DESCRIPTION

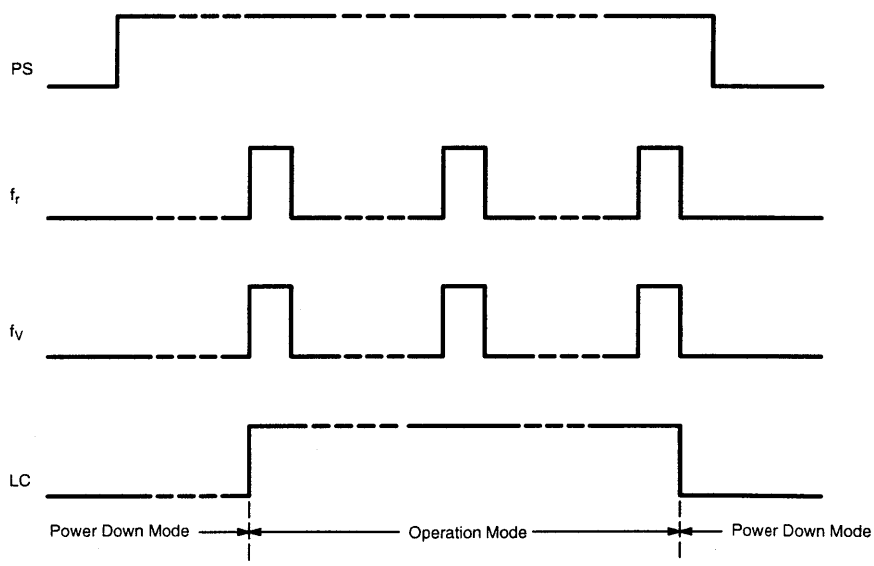
The MB87076 has a power down function which selects the operation mode or power down mode depending on the PS input signal level. When PS is set at low level, the power down mode is selected. During the power down mode, internal dividers stop operation. Thus, very low power supply consumption is achieved and the LC pin is set at Low level.

Then the PS level goes High with the frequency of VCO as almost the same value as that under the condition of phase lock, the following sequence is taken:

1) Programmable divider starts operation
2) f_V is output with some delay
3) Programmable reference divider starts operation when it receives f_V
4) f_r is output
5) LC is forced to set at High level (normal operation mode is selected)

When the f_r outputs immediately after f_P and goes into the phase detector, the phase lock condition is obtained just after the first clock. When PS is set at Low level again, internal dividers stop the operation. The internal condition is then reset.

Fig. 3 – POWER DOWN MODE



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}	—	V_{DD}	V
Output Temperature	T_A	–40	—	+85	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.0V, T_A = –40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	—	2.1	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	0.9	
Input Sensitivity	f_{IN}	Vf_{PP}	Amplitude in AC coupling, sine wave	0.5	—	—	V_{P-P} Sine
	OCS_{IN}	V_{SIN}		0.5	—	—	
High-level Input Current	Except f_{IN} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	—	1.0	—	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	—	–1.0	—	
Input Current	f_{IN}	If_{IN}	$V_{IN} = V_{SS}$ to V_{DD}	—	±30	—	µA
	OCS_{IN}	I_{XIN}		—	±30	—	
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95	—	—	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	—	—	0.05	
Low-level Output Voltage	ϕP	V_{OLV}	I_{OL} = 0.8mA	—	—	0.80	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	2.50	—	—	V
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	—	—	0.50	
High-level Output Current	Except ϕP and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	–0.5	—	—	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	0.5	—	—	
N-channel Open Drain Cut Off Current		I_{OFF}	$V_O = V_{DD}$ +3.0V	—	1.0	—	µA
Power Supply Current*1		I_{DDOP}	Operation mode	—	2.50	—	mA
		I_{DDPS}	Power down mode	—	—	80	µA
Max. Operating Frequency of Programmable Reference Divider		$f_{MAX}d$	—	10	20	—	MHz
Max. Operating Frequency of Programmable Divider		$f_{MAX}p$	—	10	20	—	MHz

Note: *1: f_{IN} = 8.0MHz, 11.5MHz crystal is connected between OSC_{IN} and OSC_{OUT}.
PS is set at high level; all other inputs are set at low level. Outputs are open.

ELECTRICAL CHARACTERISTICS (Continued)

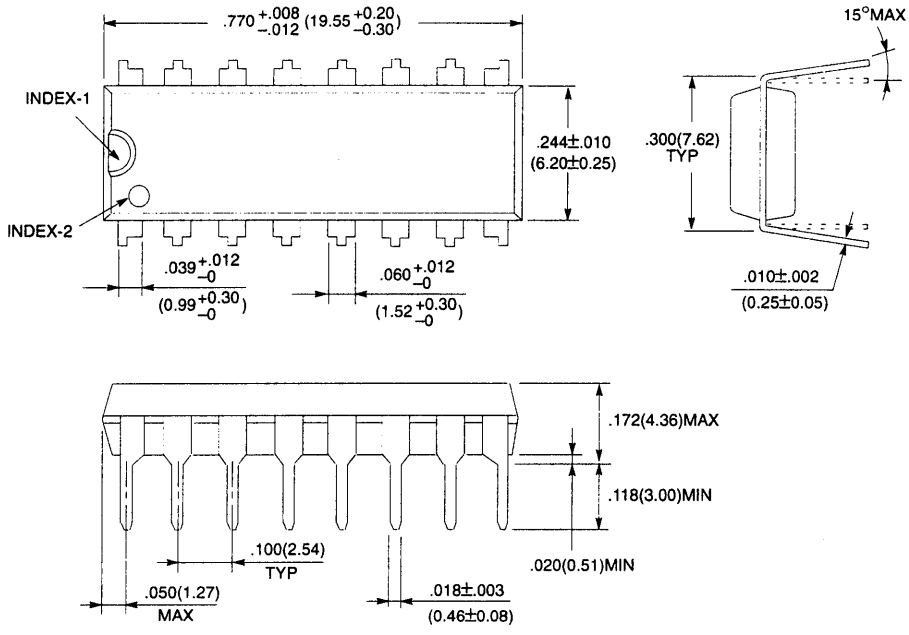
(V_{SS} = 0V, V_{DD} = 5.0V, T_A = –40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	—	3.5	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	1.5	
Input Sensitivity	f_{IN}	Vf_{IN}	Amplitude in AC coupling, sine wave	0.8	—	—	V_{P-P} Sine
	OCS_{IN}	V_{SIN}		1.0	—	—	
High-level Input Current	Except f_{IN} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	—	1.0	—	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	—	–1.0	—	
Input Current	f_{IN}	If_{IN}	$V_{IN} = V_{SS}$ to V_{DD}	—	±50	—	µA
	OCS_{IN}	I_{XIN}		—	±50	—	
High-level Output Voltage	Except φP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95	—	—	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	—	—	0.05	
Low-level Output Voltage	φP	V_{OLV}	I_{OL} = 1mA	—	—	0.50	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	4.50	—	—	V
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	—	—	0.50	
High-level Output Current	Except φP and OSC_{OUT}	I_{OH}	V_{OH} = 4.0V	–1.0	—	—	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	1.0	—	—	
N–channel Open Drain Cut Off Current		I_{OFF}	$V_O = V_{DD}$ +3.0V	—	1.0	—	µA
Power Supply Current*1		I_{DDOP}	Operation mode	—	3.0	—	mA
		I_{DDPS}	Power down mode	—	—	100	µA
Max. Operating Frequency of Programmable Reference Divider		$f_{MAX}d$	—	15	25	—	MHz
Max. Operating Frequency of Programmable Divider		$f_{MAX}p$	—	10	25	—	MHz

Note: *1: f_{IN} = 8.0MHz, 11.5MHz crystal is connected between OSC_{IN} and OSC_{OUT}.
PS is set at high level; all other inputs are set at low level. Outputs are open.

PACKAGE DIMENSIONS

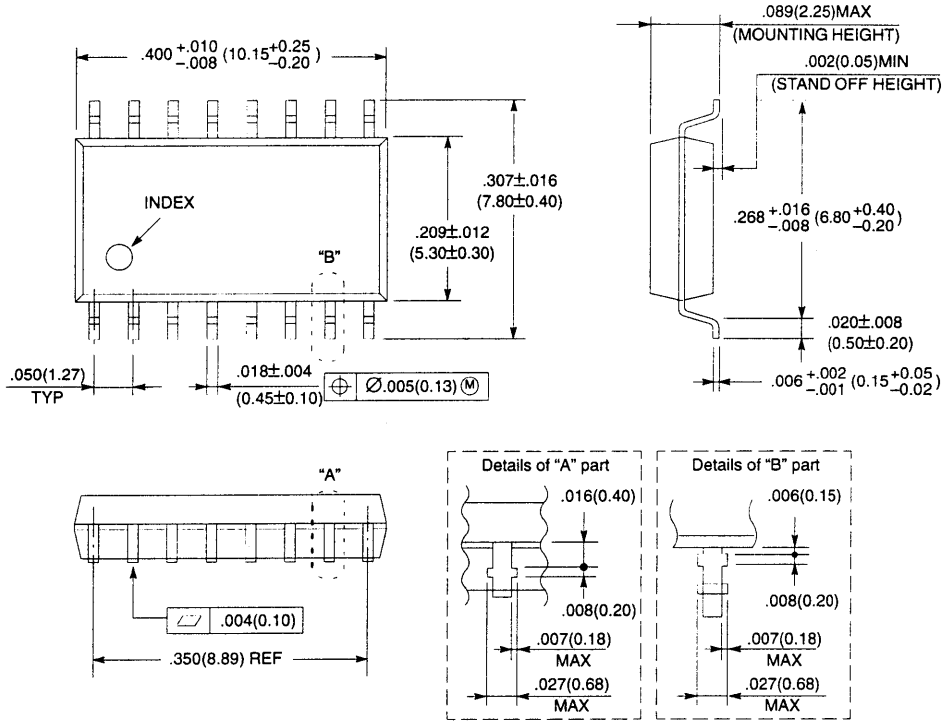
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

November 1990
Edition 3.0

FUJITSU

DATA SHEET

MB87086A
CMOS PLL FREQUENCY SYNTHESIZER

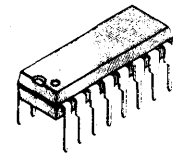
3

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

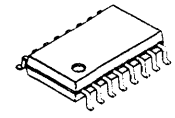
The Fujitsu MB87086A, fabricated in advanced CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer. The MB87086A contains an inverter for oscillator, programmable reference divider (binary 16-bit programmable reference counter), programmable divider (binary 10-bit programmable counter), phase detector and charge pump.

The MB87086A can make up a PLL synthesizer up to 95MHz operation.

- Single Power Supply Voltage: V_{DD} = 4.5V to 5.5V
- Wide Temperature Range: T_A = –30 to 60°C
- On-chip Inverter for oscillator
- Divide factor of programmable divider and programmable divider are set by serial data input. (The last data bit is a control bit.)
- 3-type of phase detector outputs
  On-chip charge pump output for active LPF
  On-chip charge pump output for passive LPF
  Output for external charge pump
- 16-pin Standard Dual-in-line Package (Suffix: -P)
  16-pin Standard Flat Package (Suffix: -PF)
- 95MHz input capability @5V (fin input)
- fin, Clock, Data input circuits involve schmitt circuit
- The divide factor is selected according to the following equation:
  $f_{VCO} = N \times (f_{OSC} \div R)$
  f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
  N : Preset divide factor of programmable divider (5 to 1023)
  f_{OSC} : Output frequency of the external oscillator
  R : Preset divide factor of binary programmable reference divider (5 to 65535)

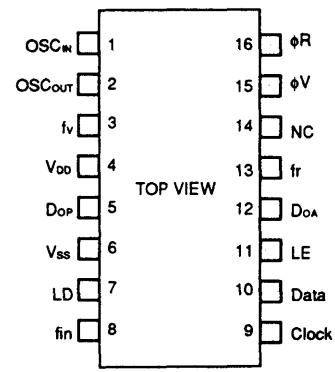


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



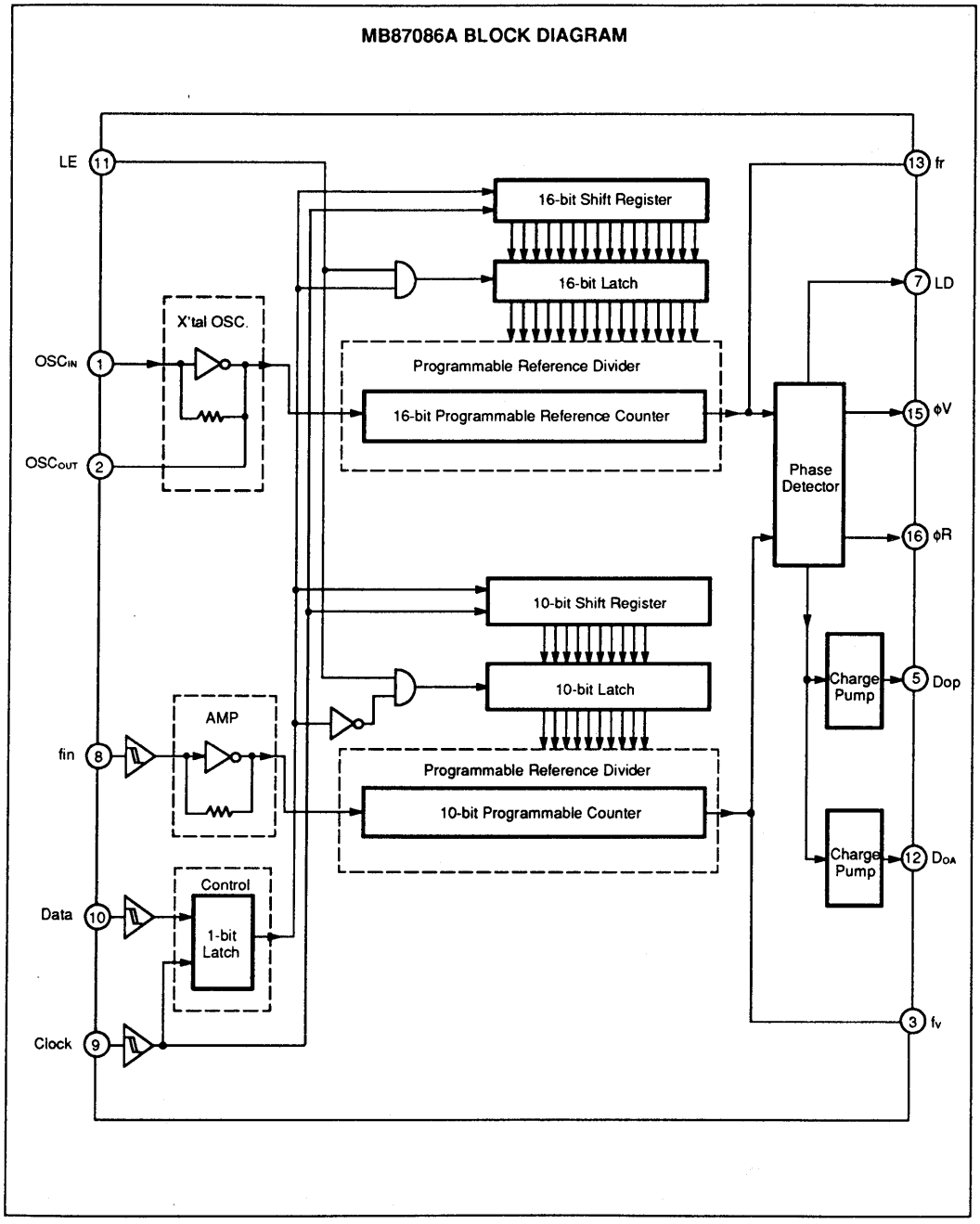
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.3 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Output Voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Output Current	I_{OUT}	±10	mA
Operating Ambient Temperature	T_A	–30 to +80	°C
Storage Temperature	T_{STG}	–40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB87086A BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be connected to open when an external oscillator is used.
3	f_V	O	Monitor pin for the phase detector input. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_{OP}	O	Output pin for low pass filter (Passive type). The mode of D_{OP} is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: fr > fv: Drive mode (D_{OP} – High level) fr = fv: High-impedance fr < fv: Sink mode (D_{OP} = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are coherent, and when the loop is locked. Otherwise it outputs low pulse signal.
8	fin	I	Frequency input to programmable divider from VCO or prescaler output. (This input has an internal feed back resistor.)
9	Clock	I	Clock signal input for shift registers. Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	I	Serial data input for shift registers. The last bit of the data is the control bit. The control data determines which latch is activated.
11	LE	I	Load enable input. When this pin is high level, the data stored in the shift registers is transferred to 16-bit latch, or 10-bit latch depending on the control bit setting.
12	D_{OA}	O	Output pin for low pass filter (Active type). The mode of D_{OA} is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: fr > fv: Drive mode (D_{OA} – Low level) fr = fv: High-impedance fr < fv: Sink mode (D_{OA} = High level)
13	fr	O	Monitor pin for the phase detector input. This pin is tied to the programmable reference divider output.
14	NC	–	No connection.
15 16	ϕV ϕR	O O	Output pins for low pass filter (differential filter type). Outputs for external charge pump are changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below. ϕV / ϕR fr > fv: High level / Low level fr = fv: High level / High level fr < fv: Low level / High level

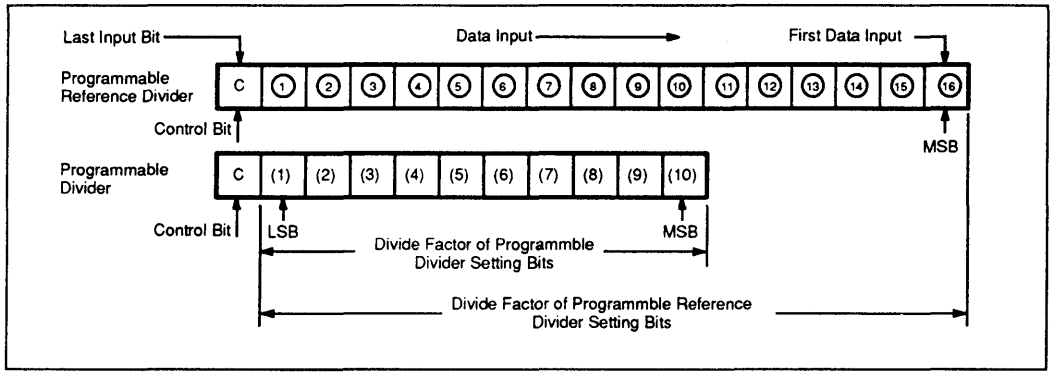
FUNCTIONAL DESCRIPTIONS

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

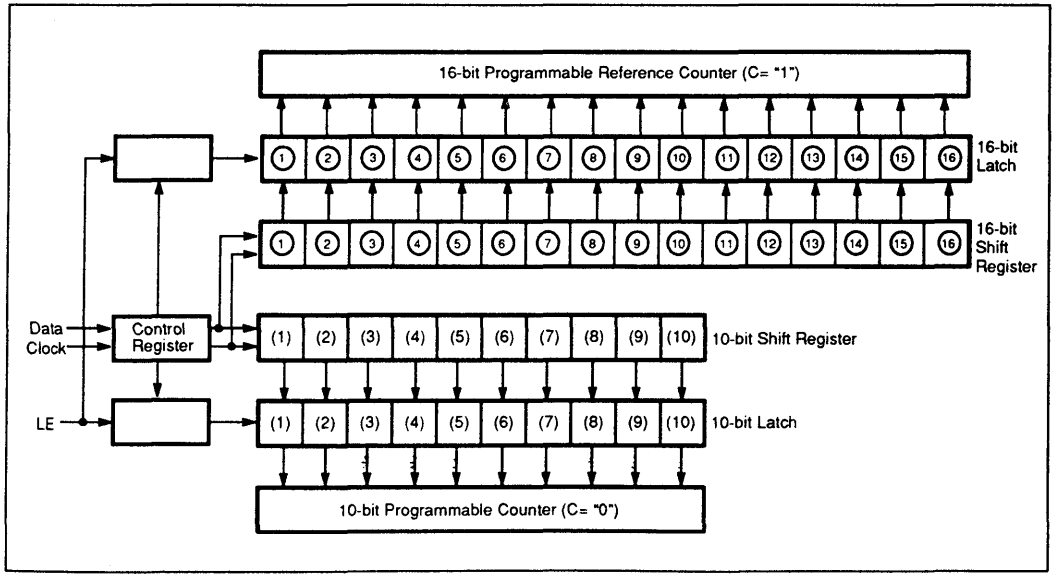
Serial data of binary code is input to Data pin. Each rising edge of clock makes one bit of the data shift into the shift registers and control register. Input data consists of 16-bit or 10-bit data and 1-bit of control bit data. The 16-bit data is used for setting the divide factor of programmable reference divider. The 10-bit data is used for setting the divide factor of programmable divider.

The last bit of the data stored in control register is a control bit. Control data determines which latch is activates. When this bit is at high level, 16-bit latch is selected. when this is at low level, 10-bit latch is selected.

The data format is shown below.



When LE is high level and control bit is high level, the data stored in 16-bit shift register is transferred to 16-bit latch. When LE is high level and control bit is at low level, the data stored in 10-bit shift register is transferred to 10-bit latch.



BINARY 10-BIT PROGRAMMABLE DIVIDER DATA INPUT

(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	Divide Factor
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

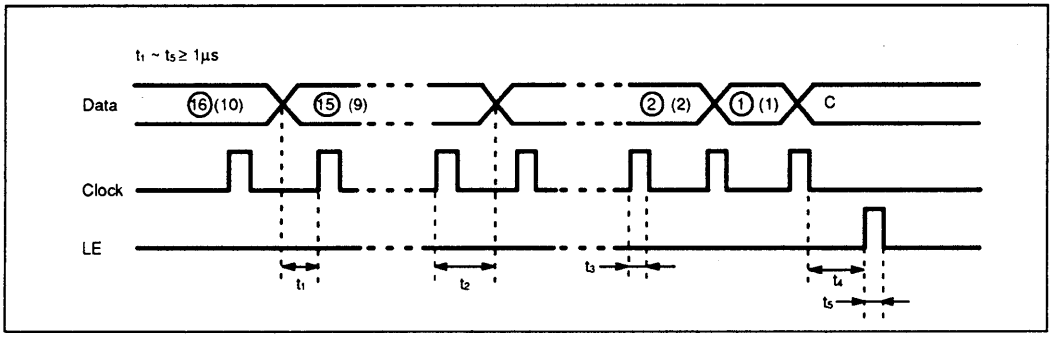
Note: Divide factor less than 5 is prohibited.
Divide factor N: 5 to 1023

BINARY 16-BIT PROGRAMMABLE REFERENCE DIVIDER DATA INPUT

⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	⑦	⑥	⑤	④	③	②	①	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	65535

Note: Divide factor less than 5 is prohibited.
Divide factor R: 5 to 65535

SERIAL DATA INPUT TIMING



Notes: ○ Data input for programmable reference divider.

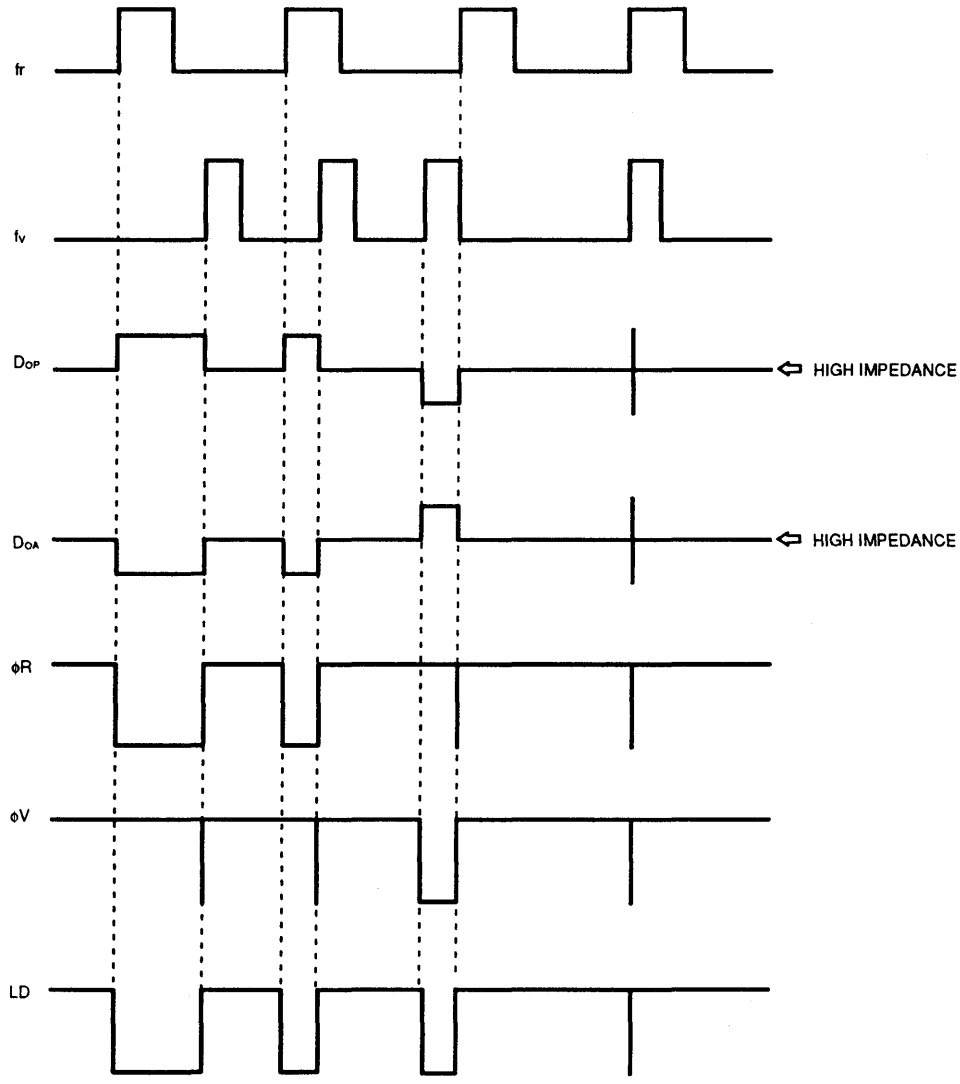
( ) Data input for programmable divider.

Data Serial data input is used for setting divide factor of programmable reference divider or programmable divider.
Data is input from MSB and last bit data is control bit.
Control bit is set high level when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock Clock input for 10-bit shift register, 16-bit shift register and control register. Data is input into internal shift registers by rising edge of the clock.

LE Load enable input:
When LE is high level, the data stored in shift registers is transferred to 16-bit latch, or 10-bit latch depending on the control bit setting.

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	−30		+60	°C

3

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 5V, T_A = −30 to 60°C)

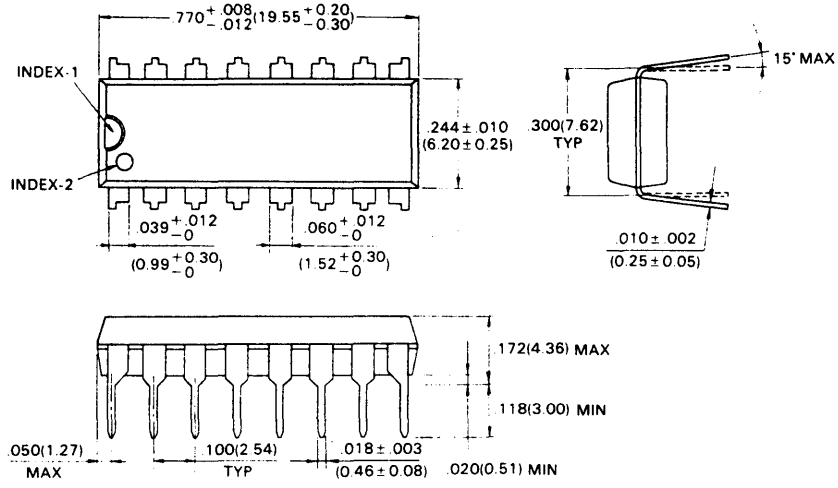
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, Sine wave	1.0			V_{P-P}
	OSC_{IN}	Vsin		1.0			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IH} = V_{DD}$		1.0		μA
Low-level Input Current		I_{IL}	$V_{IL} = V_{SS}$		−1.0		
Input Current	fin	Ifin	$V_{IN} = V_{SS}$ to V_{DD}		±50		μA
	OSC_{IN}	Iosc	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0μA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0μA			0.05	
High-level Output Current	Except OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	−1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
Power Dissipation*1		I_{DD}			8.0		mA
Maximum Operating*2 Frequency	REF Section	fmaxd		40	60		MHz
	PD Section	fmaxp		95	130		MHz

Notes: *1: fin 100MHz, 22MHz cystal is connected between OSC_{IN} and OSC_{OUT} pins.
Inputs are grounded except fin and OSC_{IN}. Outputs are open.

*2 REF Section: Maximum operating frequency of programmable reference divider.
PD Section: Maximum operating frequency or programmable divider.

PACKAGE DIMENSIONS

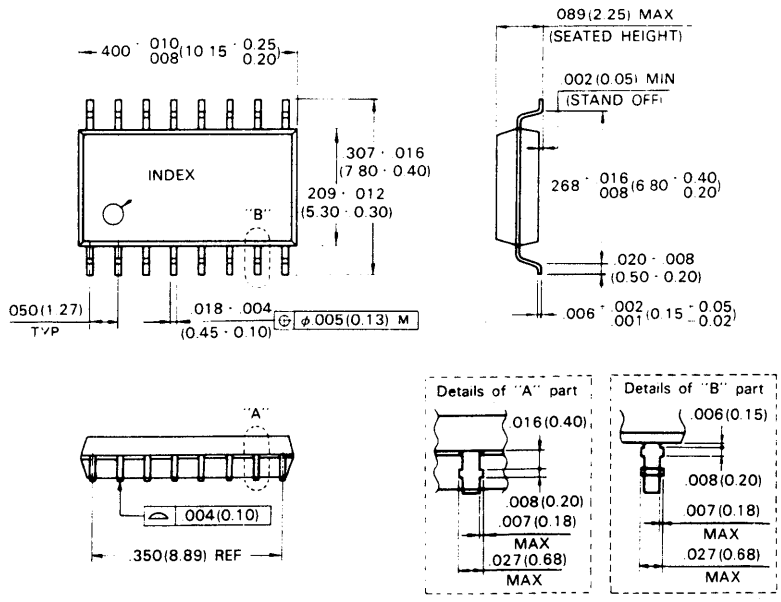
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

January 1991
Edition 3.0

FUJITSU

DATA SHEET

MB87087
CMOS PLL FREQUENCY SYNTHESIZER

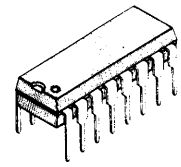
3

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

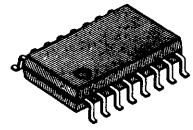
The Fujitsu MB87087, fabricated in CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer.

The MB87087 contains an inverter for oscillator, programmable reference divider (binary 14-bit programmable reference counter), 14-bit shift register, 14-bit latch, phase detector, charge pump, 17-bit shift register, 17-bit latch, programmable divider (binary 7-bit swallow counter, binary 10-bit programmable counter) and control generator for dual modulus prescaler.
When supplemented with a loop filter and VCO, the MB87087 contains the necessary circuit to make up PLL frequency synthesizer. Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1GHz.

- Wide range power supply voltage: V_{CC} = 3.0 to 6.0V
- Wide temperature range: T_A = –40 to 85°C
- 17MHz typical input capability @5V (fin input)
- On-chip inverter for oscillator
- Programmable divider with input amplifier consisting of:
  - Binary 7-bit swallow counter
  - Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of:
  - Binary 14-bit programmable reference counter
- Divide factor of programmable divider and programmable reference divider are set by serial data input (The last data bit is a control bit)
- 2-types of phase detector output
  - On-chip charge pump output
  - Output for external charge pump
- Easy interface with Fujitsu prescalers
- 16-pin standard dual-in-line package (MB87087P)
  16-pin standard flat package (MB87087PF)

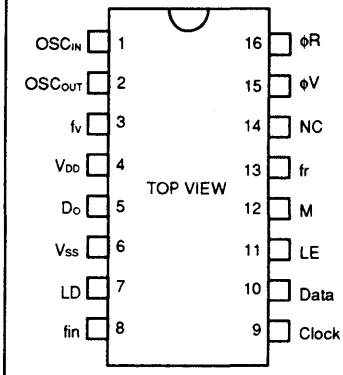


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



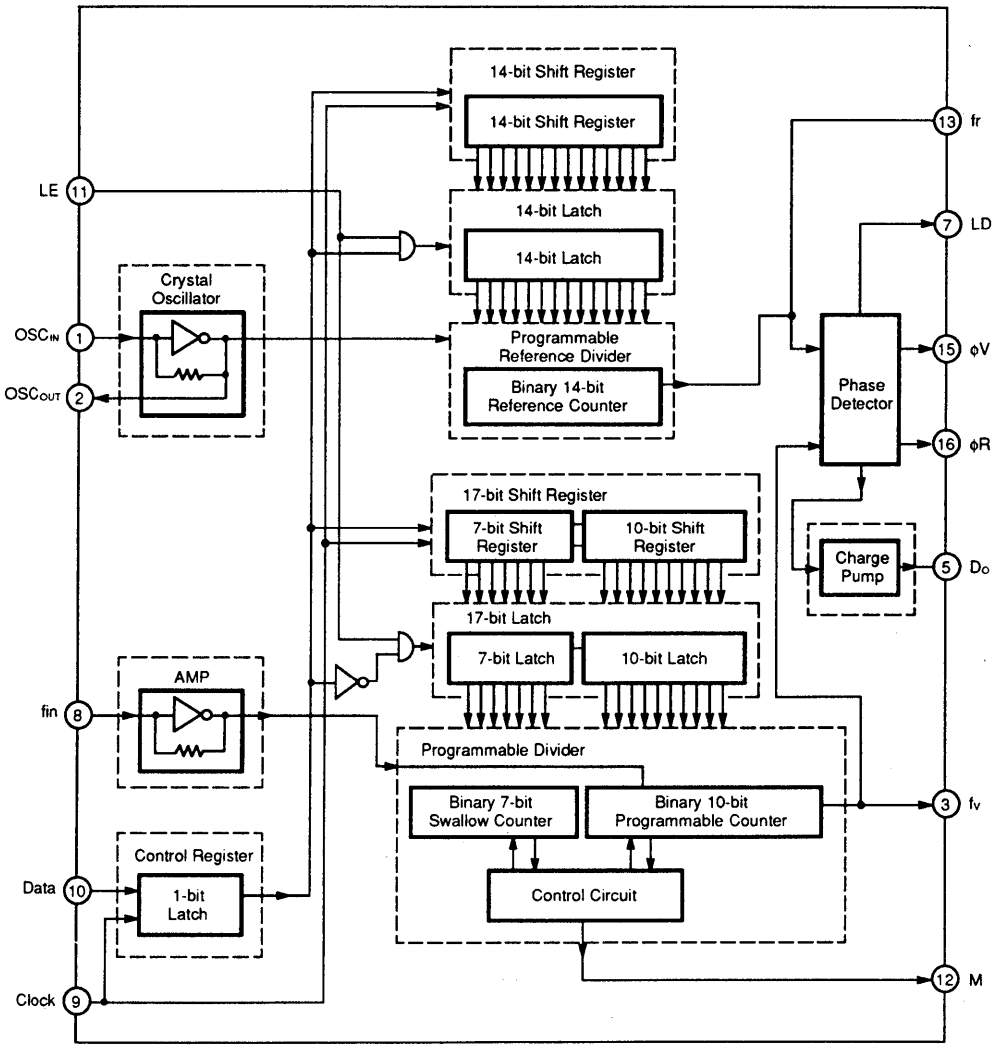
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB87087 BLOCK DIAGRAM



PIN DESCRIPTION

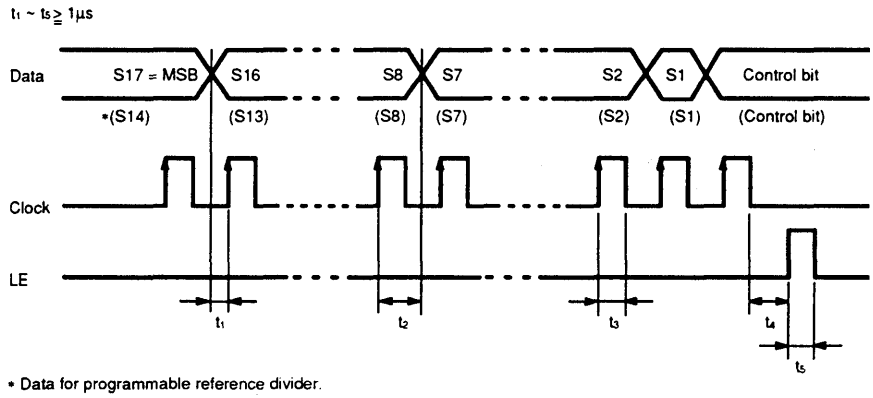
Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.
3	f_V	O	Monitor output of the phase detector. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_O	O	Three-state charge pump output of phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Drive mode (D_O = High level) $f_r = f_V$: High impedance $f_r < f_V$: Sink mode (D_O = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are equal, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	fin	I	Clock input for programmable divider. This input contains internal bias circuit and amplifier. The connection with an external dual-modulus prescaler should be an AC connection.
9	Clock	I	Clock signal input for 17-bit shift register and 14-bit shift register. Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for programmable divider and programmable reference divider. The last bit of the data is the control bit. Control bit determines which latch is activated. The data stored in the shift register is transferred to the 14-bit latch when the bit is high, and to 17-bit latch when low.
11	LE	I	Load enable input with internal pull up resistor. When this pin is high (active high), the data stored in shift register is transferred to 14-bit latch or 17-bit latch depending on the control bit data.
12	M	O	Control output for an external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of input signal fin (pin #8). Pulse swallow function: e.g. MB501L: M = High: Preset modulus factor 64 or 128 M = Low: Preset modulus factor 65 to 129

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
13	fr	O	Monitor output of phase detector input. This pin is tied to the programmable divider output.
14	NC	–	No connection.
15 16	ϕV ϕR	O O	Output for external charge pump. The mode of ϕR and ϕV are changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency f_V as listed below. ϕR ϕV fr > f_V: Low-level High-level fr = f_V: High-level High-level fr < f_V: High-level Low-level

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT TIMING



* Data for programmable reference divider.

Notes: Data: Serial data input is used for setting divide factor of programmable reference divider and progranmable divider. Data is input from MSB, and last bit data is a control bit.
Control bit is set high when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Data is input to internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data stored in shift register is transferred to 14-bit latch, or 17-bit latch depending on the control bit setting.

PULSE SWALLOW FUNCTION

$$f_{VCO} = [(N \times M) + A] \times f_{OSC} + R \quad (N > A)$$

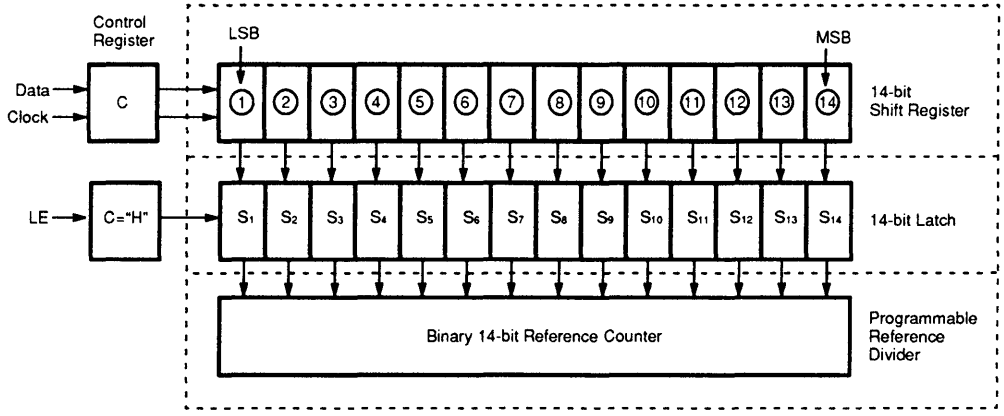
f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler
(e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit programmable counter (0 to 127, A < N)
f_{OSC} : Output frequency of external oscillator
R : Preset divide factor of binary 14-bit programmable reference counter (5 to 16383)

3

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

Serial data consists of 14-bit data, which is used for setting divide factor of programmable reference counter, and 1-bit control data. In this case, control bit is set high level.

The data format is shown below.



BINARY 14-BIT REFERENCE COUNTER DATA INPUT

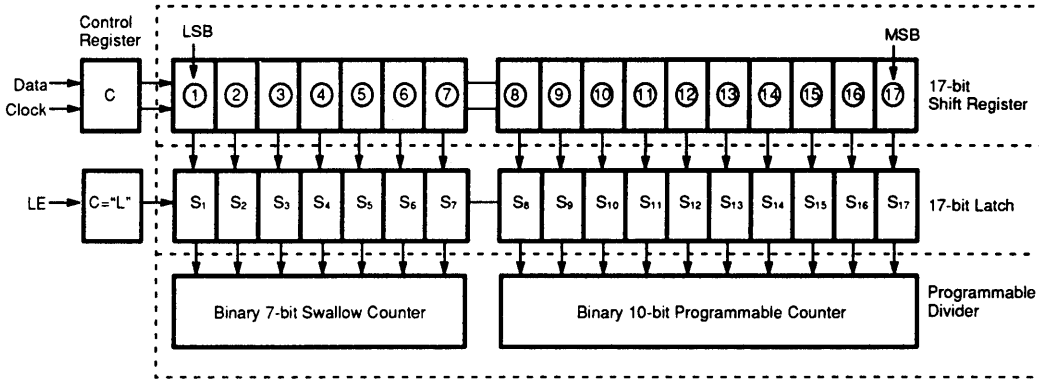
⑭	⑬	⑫	⑪	⑩	⑨	⑧	⑦	⑥	⑤	④	③	②	①	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	16383

Note: Divide factor less than 5 is prohibited.
Divide factor : 5 to 16383

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data consists of 17-bit data, which is used for setting divide factor of programmable divider, and 1-bit control data. In this case, control bit is set low level. The data ① to ⑦ set a divide factor of 7-bit swallow counter and data ⑧ to ⑰ set divide factor of 10-bit programmable counter.

The data format is shown below.



BINARY 7-BIT SWALLOW COUNTER DATA INPUT

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

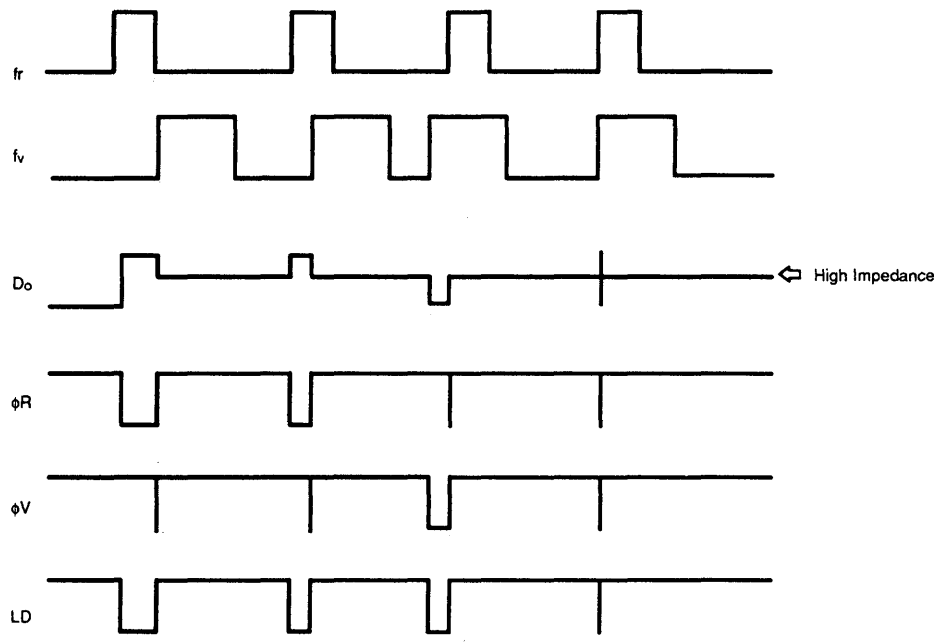
Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
e.g. MB501L (÷65/65)prescaler
SW = H (64/65): Bit 7 to shift register ⑦ should be zero.

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

Note: Divide factor less than 5 is prohibited
Divide factor N : 5 to 1023

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	3.0		6.0	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfin	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	V_{OSC}		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		–1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±30		µA
	OSC_{IN}	I_{OSC}	V_{IN} = V_{SS} to V_{DD}		±30		µA
	LE	I_{LE}	V_{IN} = V_{SS}		–40		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 2.6V	–0.5			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	0.5			
High-level Output Current	M	I_{OHM}	V_{OH} = 2.6V	–0.7			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	1.5			
Power Supply Current *1		I_{DD}			2.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	20		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		10	20		MHz

Notes: *1: fin = 8.0MHz 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are grounded except fin and OSC_{IN}. Output are open.

ELECTRICAL CHARACTERISTICS (Continued)

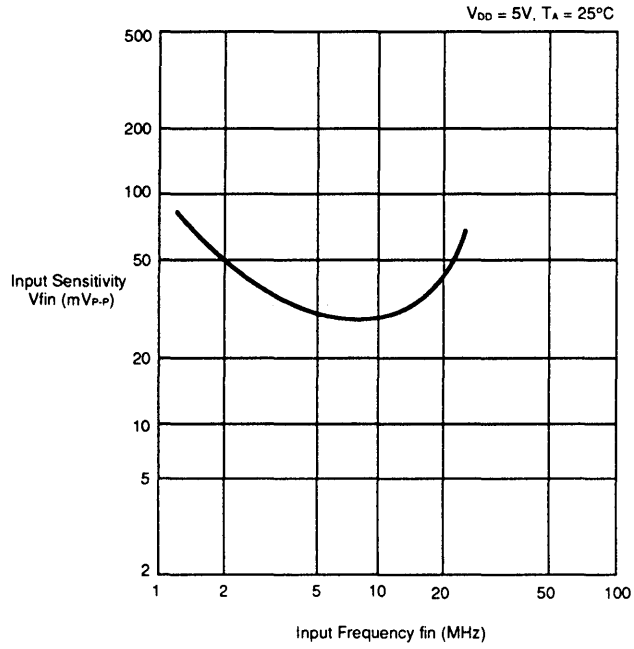
(V_{DD} = 5.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfin	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	V_{OSC}		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		–1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±50		µA
	OSC_{IN}	Iosc	V_{IN} = V_{SS} to V_{DD}		±50		µA
	LE	I_{LE}	V_{IN} = V_{SS}		–60		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	–1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
High-level Output Current	M	I_{OHM}	V_{OH} = 4.6V	–1.5			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	3.0			
Power Supply Current *1		I_{DD}			3.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	25		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		17	25		MHz

Note: *1. fin = 8.0MHz, 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}
Inputs are grounded except fin and OSC_{IN}. Outputs are open.

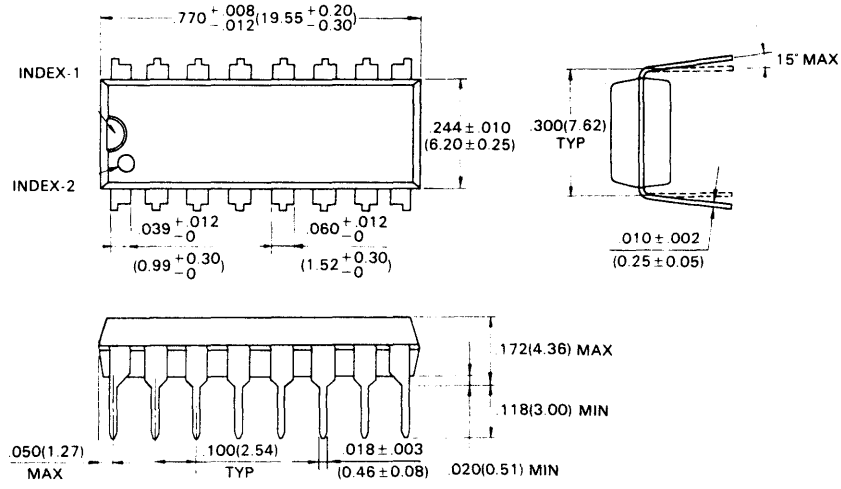
TYPICAL CHARACTERISTICS CURVE

Input Sevsitivity vs. Input Frequency (fin Section)



PACKAGE DIMENSIONS

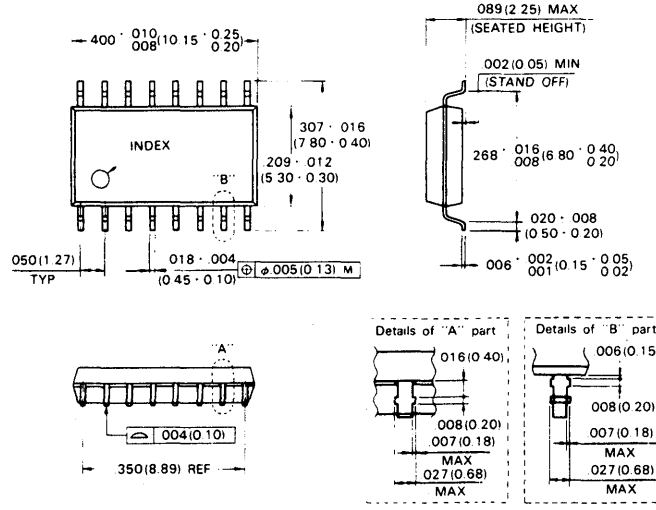
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

Printed in Japan PV0130-911A3

Sept. 1995
Edition 4.0a

FUJITSU

DATA SHEET

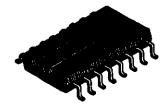
MB87091

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

3

CMOS SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTION

The Fujitsu MB87091 is a CMOS serial input Phase Locked Loop (PLL) frequency synthesizer ideal for use in cordless telephone sets and other radio equipment. It incorporates an inverter for an oscillation circuit, a programmable reference divider (14–bit binary programmable reference counter), a shift register control register, latches, a programmable divider (6–bit binary swallow counter with 12–bit binary programmable counter and dual modulus prescaler: 64/65), a phase comparator, an intermittent mode control circuit, and a constant–current charge pump. The power save control input pin (PS) for the intermittent mode control circuit is used to switch between the stand by and active modes. This is used for phase synchronization at the beginning of operation. The MB87091 permits construction of PLL frequency synthesizers with operating frequencies of up to 300 MHz.



(FPT-16P-M06)

(FPT-20P-M03)

FEATURES

- Single power supply voltage: V_{DD} = 2.7 to 3.3V
- Built–in inverter for an oscillator
- Adjustable output current of the charge pump with an external resistor
- Intermittent mode control circuit
- Two phase comparator outputs (for external and internal charge pumps)
- Wide operating temperature range (T_A) –40°C to 60°C
- Plastic DIP ackage(Suffix: –P), Plastic SOP package(Suffix: –PF), Plastic SSOP package (Suffix: –PFV)
- Setting the divide ratio
  Use the below formula to define the parameters for setting the divide ratio
  $\underline{fvco} = (\underline{N} \times \underline{M} + \underline{A}) \times (\underline{fosc} \div \underline{R})$ (N>A)
  (fvco) Output frequency of the external VCO
  (N) Preset divide ratio of 12–bit binary programmable counter (5 to 4,095)
  (M) Preset modulus of the dual modulus prescaler (64)
  (A) Preset divide ratio of 6–bit binary swallow counter (0 to 63)
  (fosc) Output frequency of the external reference frequency oscillator
  (R) Preset divide ratio of 14–bit binary programmable reference counte (5 to 16,383)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

(V_{SS}=0V)

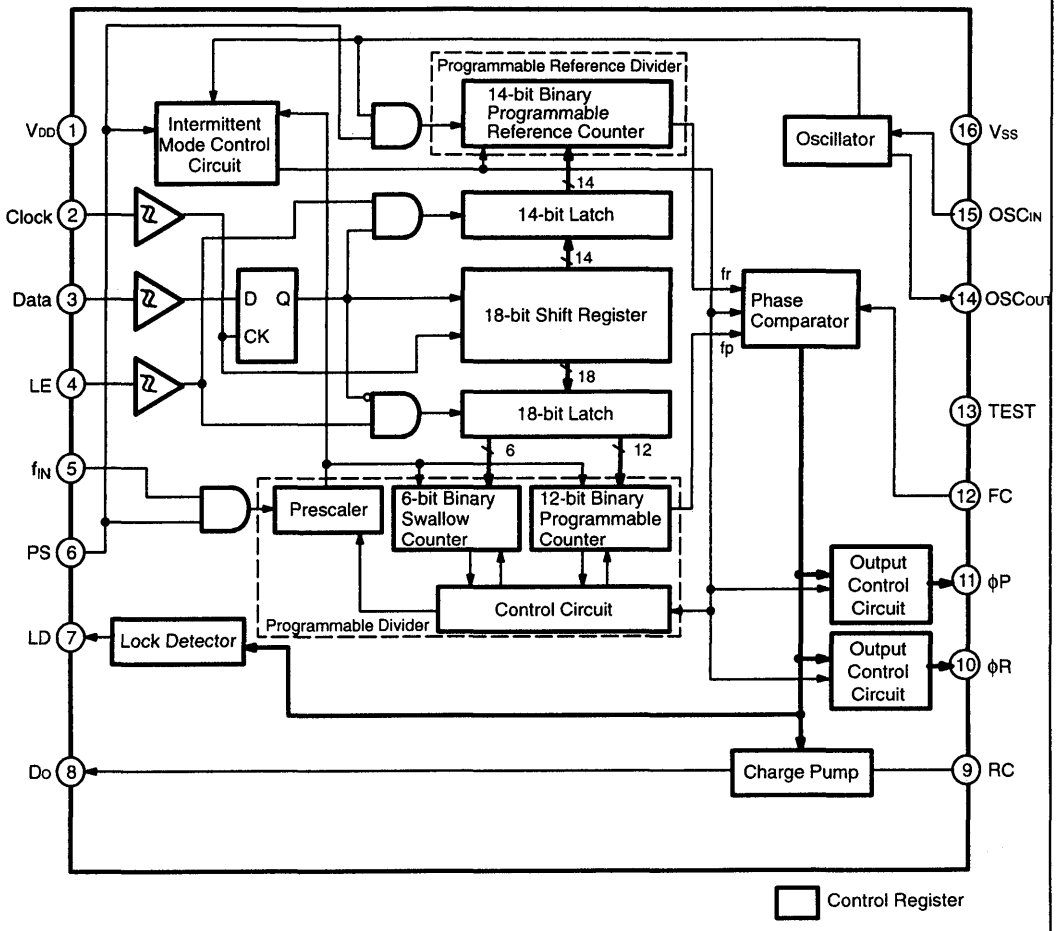
Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	V_{SS}–0.5 to V_{SS}+6.0	V
Input voltage	V_{IN}	V_{SS}–0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	V_{SS}–0.5 to V_{DD}+0.5	V
Output current	I_{OUT}	±10	mA
Ambient temperature	T_A	–40 to +60	°C
Storage temperature	Tstg	–40 to +125	°C
Power dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

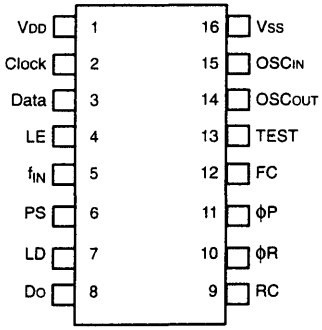
BLOCK DIAGRAM OF MB87091

(This block diagram is for DIP/SOP packages.)



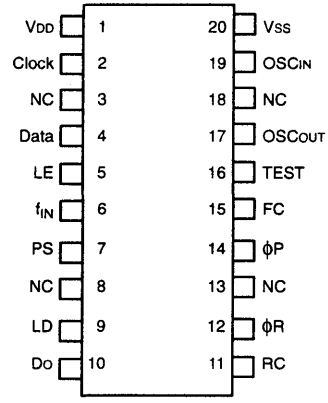
PIN ASSIGNMENT

(TOP VIEW)



(DIP-16P-M04)
(FPT-16P-M06)

(TOP VIEW)



(FPT-20P-M03)

3

PIN DESCRIPTIONS

Pin No.		Pin Name	I/O	Description
DIP/ SOP	SSOP			
1	1	V_{DD}	–	Power supply pin
2	2	Clock	I	Clock input to the shift register Each rising edge of the clock shifts one bit of the data into the shift register. The input portion contains a Schmitt trigger circuit.
–	3	NC	–	No connection
3	4	Data	I	Serial data input for programmable divider and programmable reference divider The input portion contains a Schmitt trigger circuit.
4	5	LE	I	Load Enable signal input pin A high on this pin transfers the contents of the shift register into the latch. The latched data provides the divide ratios of the dividers. The input portion contains a Schmitt trigger circuit.
5	6	f_{IN}	I	Input to the programmable divider The input portion contains a bias circuit and an amplifier. This pin is connected to an external voltage controlled oscillator (VCO) with an AC coupling.
6	7	PS	I	Power save control input pin A high on this pin places the MB87091 into the active mode and a low into the stand by mode. The PS pin has to be set low at power–on time (see Section 1.1, "Intermittent Operation," in "Functional Descriptions").
–	8	NC	–	No connection
7	9	LD	O	Phase comparator output pin The LD pin outputs high when the PLL is locked and low when the PLL is unlocked.
8	10	D_O	O	Phase comparator output pin The output current of this charge pump is adjustable with external resistor R_{RC}. The D_O output may be inverted by the FC input. The relationships between the programmable reference divider output (fr) and the programmable divider output (fp) are shown below: fr > fp: "H" level (FC = "L"), "L" level (FC = "H") fr = fp: High impedance fr < fp: "L" level (FC = "L"), "H" level (FC = "H")
9	11	RC	–	Connect pin with an external resistor R_{RC} (see Section 1.4, "Phase Comparator" in "Functional Descriptions")
10	12	ϕR	O	Phase comparator output pin (for external charge pump) The relationships between the programmable reference divider output (fr) and the programmable divider output (fp) are shown below: When FC = "L" fr > fp: ϕR = "L" level fr = fp: ϕR = "L" level fr < fp: ϕR = "H" level When FC = "H" fr > fp: ϕR = "H" leve fr = fp: ϕR = "L" level fr < fp: ϕR = "L" level
–	13	NC	–	No connection

PIN DESCRIPTIONS (Continued)

Pin No.		Pin Name	I/O	Description
DIP/ SOP	SSOP			
11	14	ϕP	O	Phase comparator output pin (for external charge pump) ϕP is an N-channel, open-drain output. The relationships between the programmable reference divider output (fr) and the programmable divider output (fp) are shown below: When FC = "L" fr > fp: ϕP = "L" level fr = fp: ϕP = High impedance fr < fp: ϕP = High impedance When FC = "H" fr > fp: ϕP = High impedance fr = fp: ϕP = High impedance fr < fp: ϕP = "L" level
12	15	FC	I	Phase comparator input selector pin (see Section 1.4, "Phase Comparator" in "Functional Descriptions")
13	16	TEST	I	This is used to enable test mode A high on this pin places the MB87091 into the test mode. As this pin is provided with a pull-down resistor, it should be left open as a rule. The pin is used for shipping tests and not used for normal operation.
14	17	OSC_{OUT}	O	Crystal oscillator connect pin
–	18	NC	–	No connection
15	19	OSC_{IN}	I	Crystal oscillator connect pin A crystal oscillator is connected between the OSC_{IN} and OSC_{OUT} pins. It can clock input to OSC_{IN} from the external. In this case, the OSC_{IN} pin must be AC coupled and the OSC_{OUT} pin must be left open.
16	20	V_{SS}	–	Ground pin

FUNCTIONAL DESCRIPTIONS

1. Circuit Description

1.1 Intermittent Operation

The intermittent operation of the MB87091 refers to the process of activating and deactivating its internal circuit as necessary thus saving power dissipation otherwise consumed by the circuit. If the circuit is simply restarted from the stand by state, however, the phase relationship between the reference frequency (fr) and the programmable frequency (fp), which are the input to the phase comparator, is not stable even when they are of the same value. This may cause the phase comparator to generate an excessively large error signal, resulting in an out–of–synch lock frequency.

To preclude the occurrence of this problem, the MB87091 has an intermittent mode control circuit which forces the frequencies into phase synchronization with each other when the MB87091 is reactivated, thus minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting the PS pin high provides the normal operation mode and setting the pin low provides the standby mode and places the MB87091 into the standby state. The MB87091 behavior in the active and standby modes is summarized below:

- Active mode (PS = "H")
  All MB87091 circuits are active and provide the normal PLL operation.

- Standby mode (PS = "L")
  The circuits that consume power heavily, and cause little inconvenience when deactivated, run down and the MB87091 enters the low power dissipation state. The Do, ϕR, ϕP, and LD pins take the same state as when the PLL is locked. The Do pin becomes high-impedance state and the input voltage to the voltage controlled oscillator (VCO) is maintained at the same level as in the active mode (lock state) according to a time constant of a low pass filter (LPF). Consequently, the output frequency from the VCO (fvco) is maintained at approximately the lock frequency.

  The MB87091 continues the intermittent mode operation by alternating the active and standby modes. When it switches from standby to active mode, it forces the phase of fr and fp to correspond to minimize the error signal. In this way, the MB87091 can keep the power dissipation of its entire circuitry at the minimum.

  The MB87091 must be placed into the standby mode (PS = "L") when it is powered on.

1.2 Programmable Divider

The fvco input through the f_{IN} pin is divided by the programmable divider and then output to the phase comparator as fp. It consists of a dual modulus prescaler, a 6-bit binary swallow counter, a 12-bit binary programmable counter, and a controller which controls the divide ratio of the prescaler.

Divide ratio range:

- Prescaler: M = 64, M+1 = 65
- Swallow counter: A = 0 to 63
- Programmable counter: N = 5 to 4095

The MB87091 uses the pulse swallow method; consequently, the divide ratios of the swallow and programmable counters must satisfy the relationship N > A.

The total divide ratio of the programmable divider is calculated as follows:

Total divide ratio = (M+1)xA+Mx(N–A) = MxN+A = 64xN+A

When N is set within $5 \leq N \leq 63$, the possible divide ratio A of the swallow counter can take values $0 \leq A \leq N-1$ because N must be greater than A. For example, $0 \leq A \leq 19$ is allowed when N = 20, but $20 \leq A \leq 63$ is not allowed in that case. Consequently, $N \geq 64$ must be satisfied for the total divisor to be set within $0 \leq A \leq 63$.

The fp and f_{IN} pins have the following relationship:

$fp = f_{IN} \div (64 \times N + A)$

1.3 Programmable Reference Divider

The programmable reference divider divides the reference oscillation frequency (fosc) from the crystal oscillator connected between the OSC_{IN} and OSC_{OUT} pins or from the external oscillator input taken in directly through the OSC_{IN} pin. It then sends the resultant fr to the phase comparator. It consists of a 14-bit binary programmable reference counter. When the output from the external oscillator is to be input directly to OSC_{IN}, the pin connection must be AC coupled and the OSC_{OUT} pin is left open. Also, to prevent OSC_{OUT} from malfunctioning, its traces on the printed circuit board must be kept minimal or eliminated entirely; whenever possible, it must be free of any form of load.

The following divisor is used:

- Programmable reference counter: N = 5 to 16383

The fr and fosc have the following relationship:

- fr = fosc ÷ R

1.4 Phase Comparator

The phase comparator detects the phase difference between the outputs fr and fp from the dividers and generates an error signal that is proportional to the phase difference. The outputs from the phase comparator include 1) Do which takes on one of the three states, "L" (low), "H" (high), or "Z" (high impedance), and is sent to the LPF, 2) ϕR, 3) ϕP, and 4) LD which indicates the PLL lock or unlock state.

1.4.1 Phase Comparator

The phase comparator detects the phase difference between fr and fp and generates an error signal that is proportional to the phase difference. The roles of the fr and fp supplied to the phase comparator may be reversed by switching the logical input level on the FC pin; this inverts the logical level on the Do output. The logical level on the Do output may be selected according to the characteristics of the external LPF and the VCO. (Refer to Table 1.)

Table 1. Phase Comparator Inputs/Output Relationships

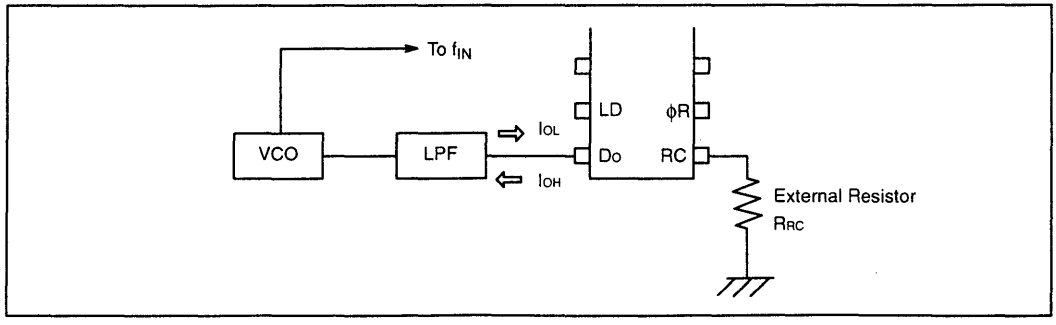
Phase Relationship \ Output	FC="L"			FC="H"		
	Do	ϕR	ϕP	Do	ϕR	ϕP
fr > fp	H	L	L	L	H	Z
fr = fp	Z	L	Z	Z	L	Z
fr < fp	L	H	Z	H	L	L

1.4.2 Charge Pump

The charge pump is available in two forms: internal and external.

- Internal constant–current charge pump output (Do)
- External charge pump outputs (ϕR, ϕP)

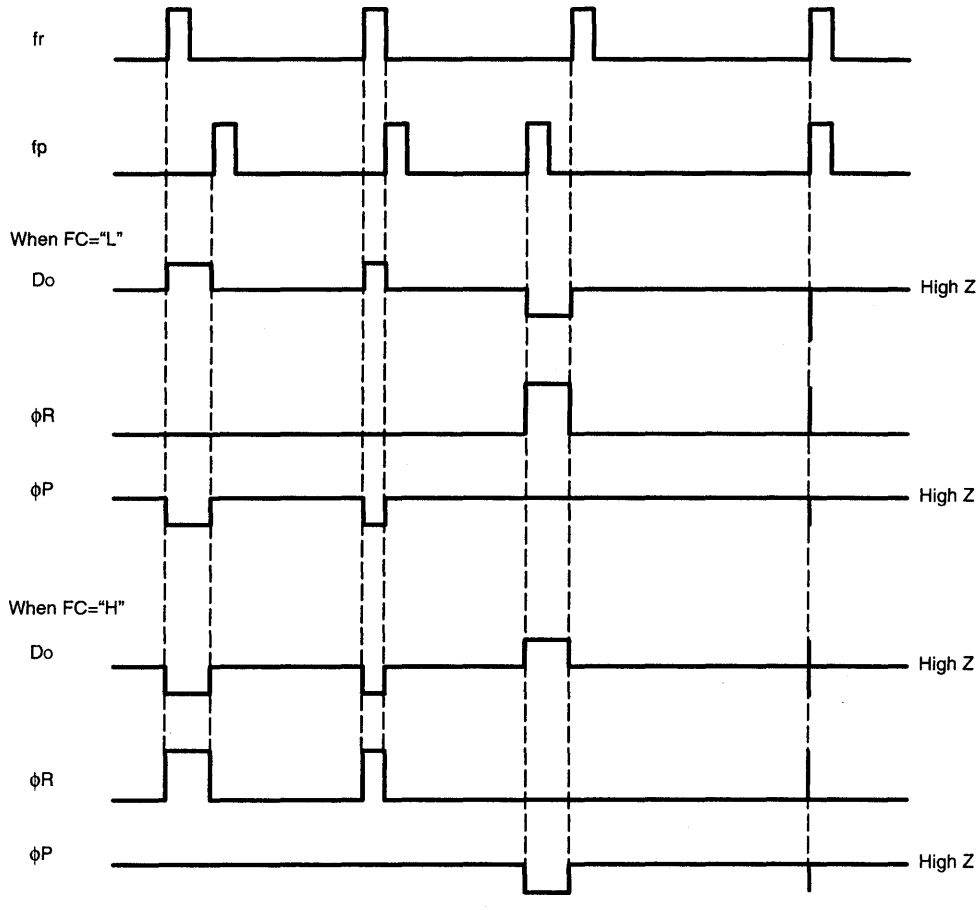
The output current at the Do pin from the internal constant–current charge pump is controlled by varying the external resistance (R_{RC}) connected between RC and GND, as shown in Figure 1.



1.4.3 Phase Comparator Input/Output Waveforms

The phase comparator outputs the logic levels summarized in Table 1, according to the phase difference between the fr and fp phase differences. Note that ϕP is an N–channel open drain output. The pulse width of the phase comparator outputs are identical and equal to the phase difference between fr and fp, as shown in Figure 2.

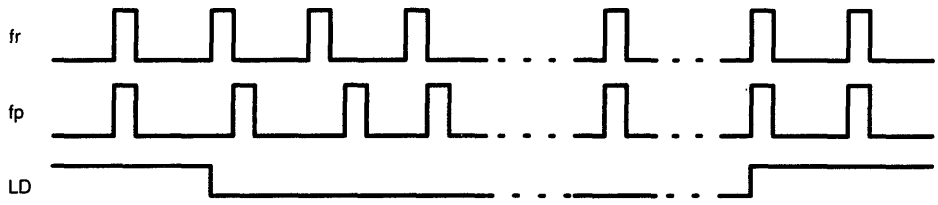
Figure 2. Phase Comparator Input/Output Waveforms (Charge Pump)



1.4.4 Lock Detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs "H" when the PLL enters the lock state and outputs "L" when the PLL enters the unlock state, as shown in Figure 3. When PS = "L", the lock detector outputs "H" compulsorily.

Figure 3. Phase Comparator Input/Output Waveform (Lock Detector)



2. Setting the Divide Ratio

2.1 Serial Data Format

The format of the serial data is shown in Figure 4. The serial data is composed of a control bit and divide ratio setting data. The control bit selects the programmable divider or programmable reference divider.
In case of the programmable divider, serial data consists of 18 bits (6 bits for the swallow counter and 12 bits for the programmable counter) and 1 control bit, as shown in Figure 4.1. In case of the programmable reference divider, the serial data consists of 14 divisor bits and 1 control bit, as shown in Figure 4.2.
The control bit is set to 0 to identify the serial data for the programmable divider and to 1 to select the serial data for the programmable reference divider.

Figure 4. Serial Data Format

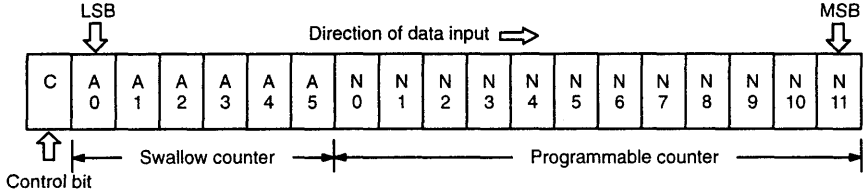


Figure 4.1 Divide ratio for the programmable divider

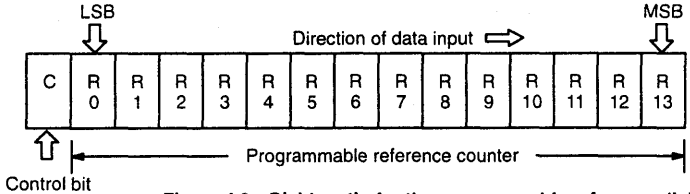
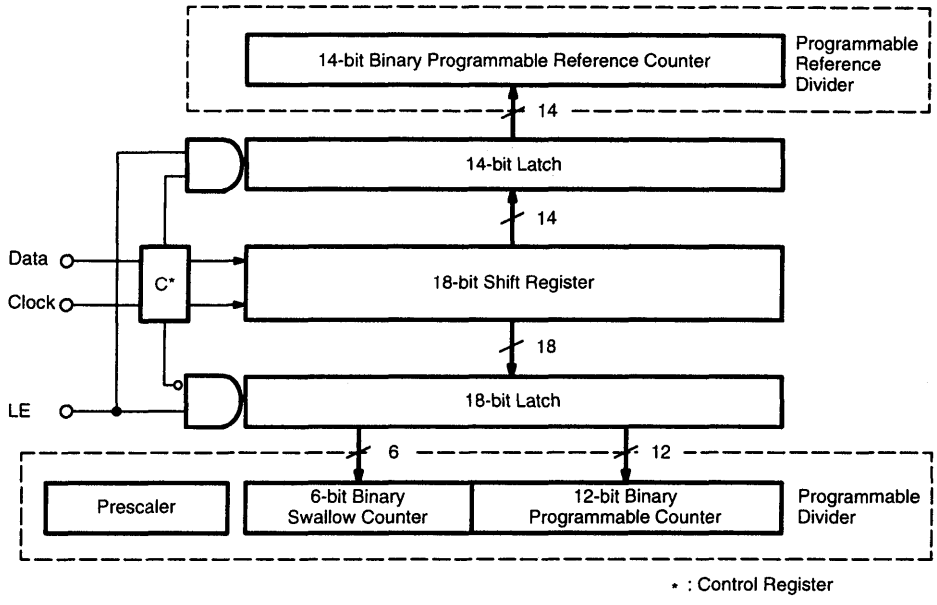


Figure 4.2 Divide ratio for the programmable reference divider

2.2 The Flow of Serial Data

Serial data is received via the data pin in synchronization with the Clock input and loaded into the shift register which contains the divide ratio setting data and into the control register which contains the control bit. The logical product (through the AND gate in Figure 5) of LE and the control register output (i.e., control bit) is fed to the Enable input of the latches. Accordingly, when LE is set high, the latch for the divider identified by the control bit is enabled and the divide ratio data from the shift register is loaded into the selected counter(s).

Figure 5. The Flow of Serial Data



2.3 Setting the Divide Ratio for the Programmable Divider

Columns A0 to A5 of Table 2.1 represent the divide ratio of the swallow counter and columns N0 to N11 of Table 2.2 represent the divide ratio of the programmable counter. The control bit is set to 0.

Table 2. Divide Ratio for the Divider

Table 2.1 Swallow Counter Divisor A

Divide Ratio A	A 0	A 1	A 2	A 3	A 4	A 5
0	0	0	0	0	0	0
1	1	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •
63	1	1	1	1	1	1

Table 2.2 Programmable Counter Divisor N

Divide Ratio N	N 0	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9	N 10	N 11
5	1	0	1	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
4095	1	1	1	1	1	1	1	1	1	1	1	1

2.4 Setting the Divide Ratio for the Programmable Reference Divider

Columns R0–R13 of Table 3 represent the divide ratio of the programmable reference counter. The control bit is set to 1.

Table 3. Divide Ratio for the Reference Divider

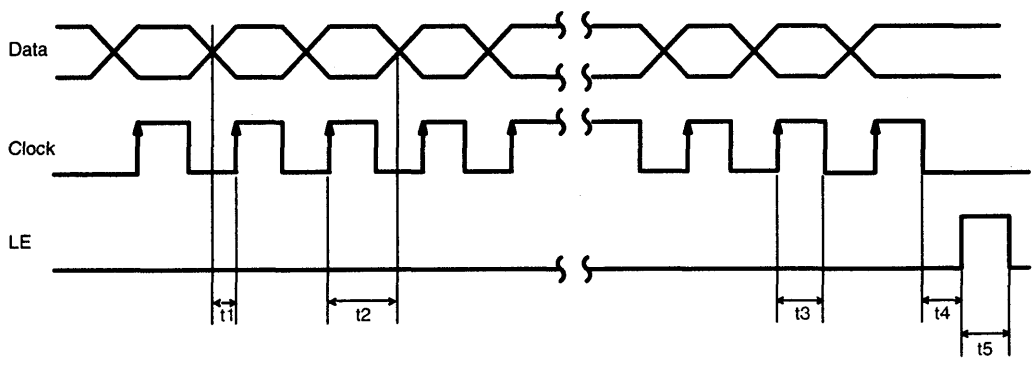
Divide Ratio R	R 0	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	R 12	R 13
5	1	0	1	0	0	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.5 Serial Data Input Timing

The MB87091 uses 19 bits of serial data for the programmable divider and 15 bits for the programmable reference divider. When more bits of serial data than are defined for the target divider are received, only the last valid serial data bits are effective.
To set the divide ratio for the MB87091 dividers, it is necessary to supply the Data, Clock, and LE signals at the timing shown in Figure 6.

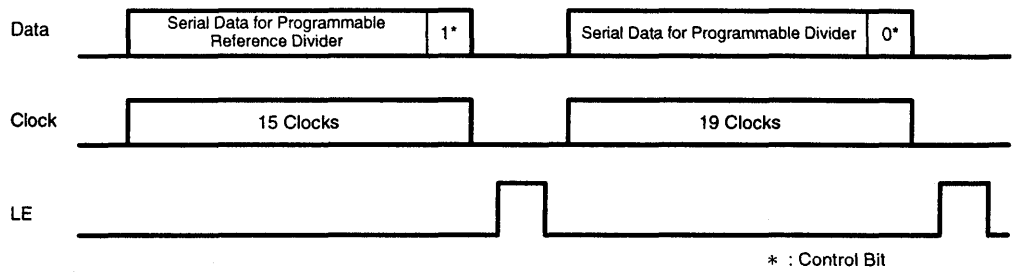
t1 (≥1 µs) : Data setup time
t2 (≥1 µs): Data hold time
t3 (≥1 µs): Clock pulse width
t4 (≥1 µs) : LE setup time to the fall edge of last clock
t5 (≥1 µs): LE pulse width

Figure 6. Serial Data Input Timing



Since the divide ratios are unpredictable when the MB87091 is turned on, it is necessary to initialize the divide ratio for both dividers at power–on time. As shown in Figure 7, after setting the divide ratio for one divider (e.g., programmable reference divider), set LE to the "H" level before setting the divide ratio for the other divider (e.g., programmable divider). To change the divide ratio of one divider after initialization, input the serial data only for that divider (the divide ratio for the other divider is preserved).

Figure 7. Inputting Serial Data (Setting Divisors)



RECOMMENDED OPERATING CONDITIONS

(Vss=0V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	2.7 to 3.3	V
Input Voltage	V_{IN}	Vss to V_{DD}	V
Ambient Temperature	T_A	–40 to +60	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = −40 to +60°C)

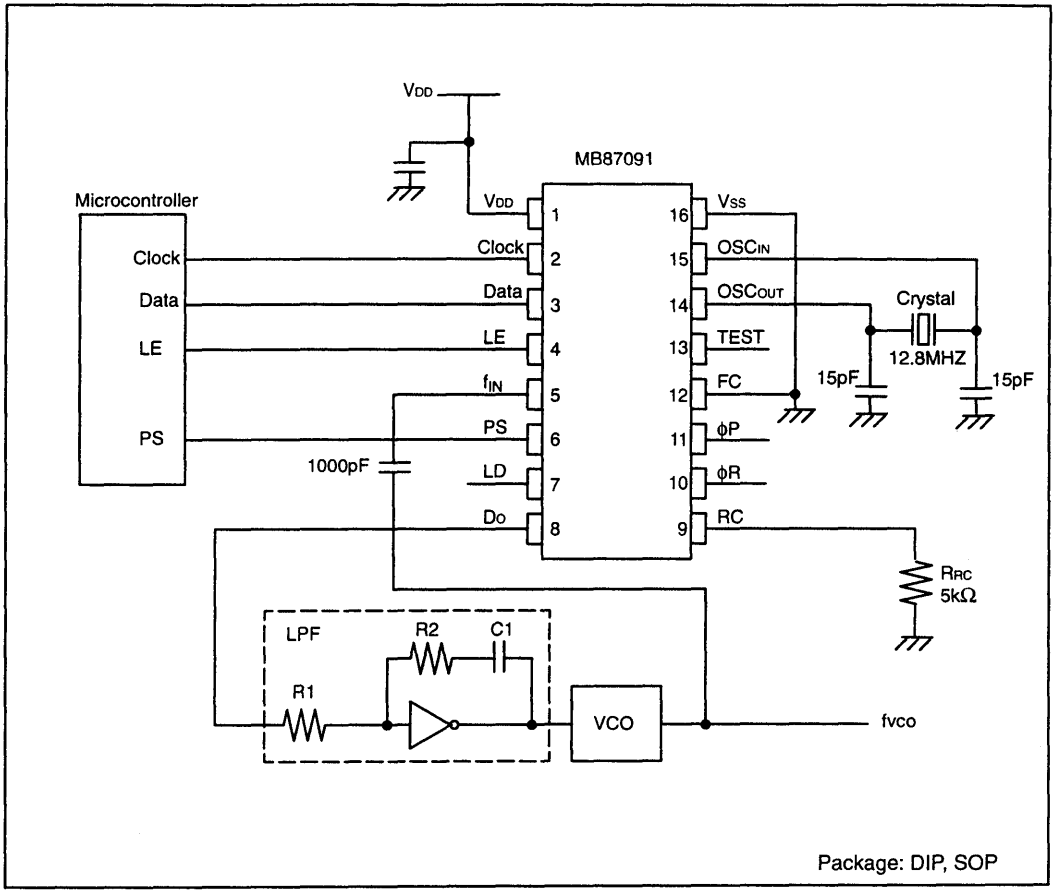
Parameter			Symbol	Conditions	Value			Unit
					Min	Typ	Max	
Input Voltage	Except f_{IN} and OSC_{IN}	H Level	V_{IH}	—	2.1	—	—	V
		L Level	V_{IL}	—	—	—	0.9	
Input Sensitivity	f_{IN}		Vf_{PP}	AC coupling amplitude	1.0	—	—	V_{P-P} Sine
	OCS_{IN}		V_{SIN}	AC coupling amplitude	1.0	—	—	
Input Current	Except f_{IN}, OSC_{IN} & TEST	H Level	I_{IH}	$V_{IN} = V_{DD}$	—	1.0	—	µA
		L Level	I_{IL}	$V_{IN} = V_{SS}$	—	−1.0	—	
	f_{IN}		If_{IN}	$V_{IN} = V_{SS}$ to V_{DD}	—	±30	—	µA
	OCS_{IN}		I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}	—	±30	—	
	TEST		I_{TEST}	$V_{IN} = V_{DD}$	—	50	—	
Output Voltage	Except OSC_{OUT}	H Level	V_{OH}	I_{OH} = 0µA	2.95	—	—	V
		L Level	V_{OL}	I_{OL} = 0µA	—	—	0.05	
	OSC_{OUT}	H Level	V_{OH}	I_{OH} = 0µA	2.50	—	—	V
		L Level	V_{OL}	I_{OL} = 0µA	—	—	0.50	
Output Current	Except OSC_{OUT}, Do & φP	H Level	I_{OH}	V_{OH} = 2.5V	−0.5	—	—	mA
		L Level	I_{OL}	V_{OL} = 0.5V	0.5	—	—	
	Do Only	H Level	I_{OH}	V_{OH} = 2.5V *1	—	−2.0	—	mA
		L Level	I_{OL}	V_{OL} = 0.5V *1	—	2.0	—	
Cutoff Current	φP Only		$I_{OFF}1$	$V_{OUT} = V_{SS}$ to V_{DD}	−1.0	—	1.0	µA
	Do Only		$I_{OFF}2$	$V_{OUT} = V_{DD}$	—	—	1.0	
Supply Current	Active Mode		I_{DDOP}	*2	—	8	16	mA
	Standby Mode		I_{DDS}	*3	—	10	—	µA
Maximum Operating Frequency		REF Section	$f_{MAX}d$	Programmable Reference Divider	40	—	—	MHz
		PD Section	$f_{MAX}p$	Programmable Divider	300	—	—	

*1: R_{RC} = 5 kΩ

*2: f_{IN} = 300 MHz, 12.8 MHz crystal is connected between OSC_{IN} and OSC_{OUT} pins, R_{RC} = 5 kΩ
Inputs are connected to GND, except f_{IN}, OSC_{IN}, and TEST. Outputs are open.

*3: Current consumption at PS = "L". Inputs are connected to GND, except f_{IN}, OSC_{IN}, and TEST pins.
Outputs and the RC pin are open.

TYPICAL APPLICATION EXAMPLE



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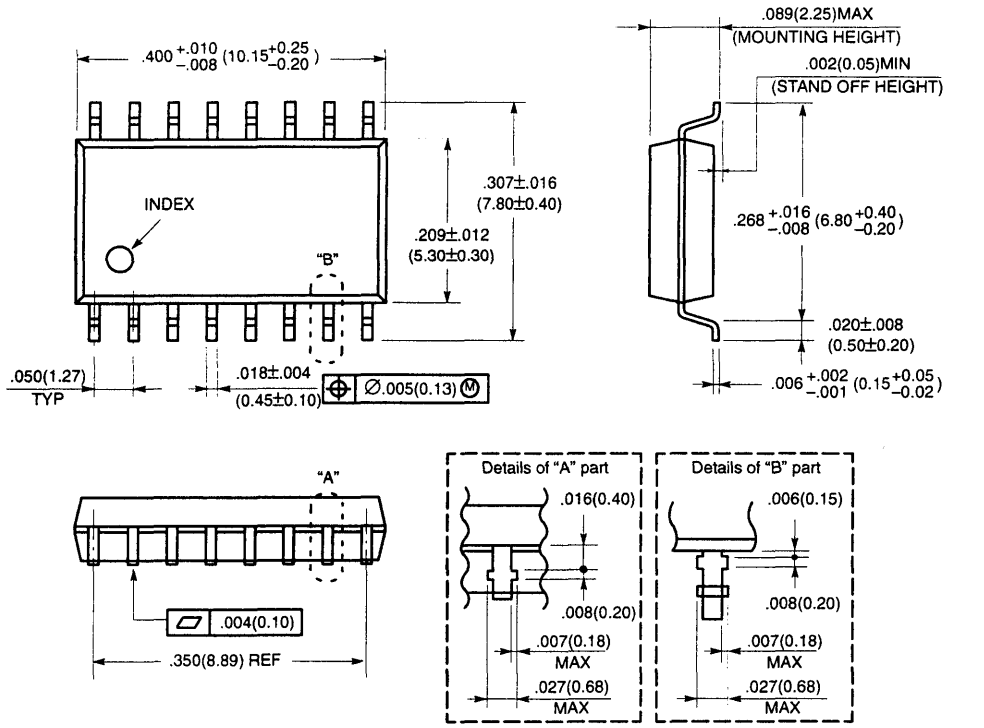
PACKAGE DIMENSIONS (CONTINUED)

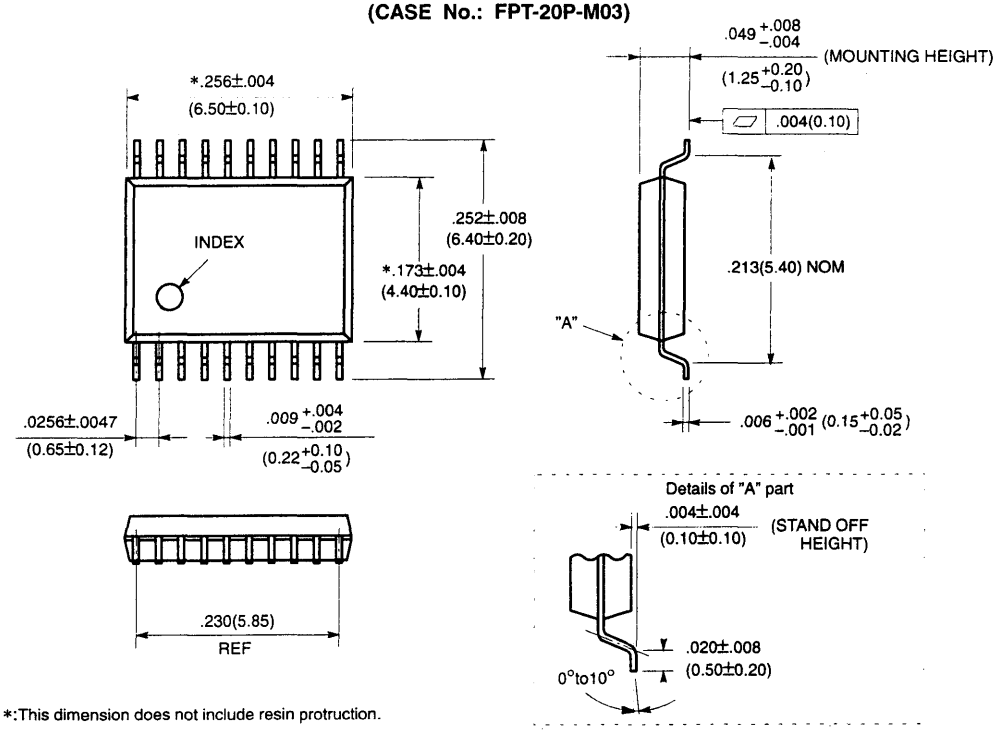
16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (CONTINUED)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0a

FUJITSU

DATA SHEET

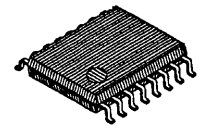
MB87093A/MB87095A/MB87096A
CMOS PLL FREQUENCY SYNTHESIZER

3

CMOS PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTION

The Fujitsu MB87093A/MB87095A/MB87096A are CMOS Phase Locked Loop (PLL) frequency synthesizers, and are suitable for mobile telephone sets or portable telephone sets. They incorporate an N-divider (10-bit counter), a reference divider (R-divider)(6-bit reference counter), a phase comparator, a charge pump, analog switches, and an intermittent mode control circuit.

A power save control input pin (PS) for the intermittent mode control circuit is used to switch between the standby and active modes. This function reduces a system's total power dissipation. On-chip analog switches enable the switching of the time constants of low-pass filters (LPF). The MB87093A/MB87095A/MB87096A have different divide ratios of R-dividers and N-dividers from each other. Other functions and characteristics are common.



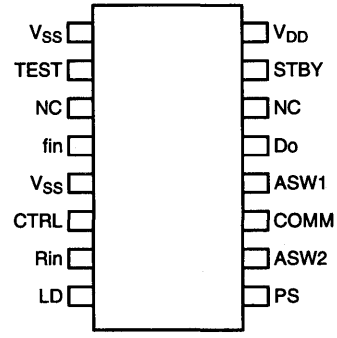
(FPT-16P-M05)

FEATURES

- Single power supply voltage: V_{DD} = 4.5 to 5.5V
- Intermittent mode control circuit
- Wide ambient temperature range: T_A = –40°C to 85°C
- On-chip two analog switches
- Plastic 16-pin SSOP package (Suffix: –PFV)
- fin = (Rin / R) x N
  (fin) Output frequency of an external voltage controlled oscillator (VCO)
  (Rin) Reference frequency
  (R) Divide ratio of R-divider
  (N) Divide ration of N-divider

Part No.	Divide ratio R	Divide ratio N
MB87093A	64	725
MB87095A	64	550
MB87096A	128	750

PIN ASSIGNMENT
(TOP VIEW)



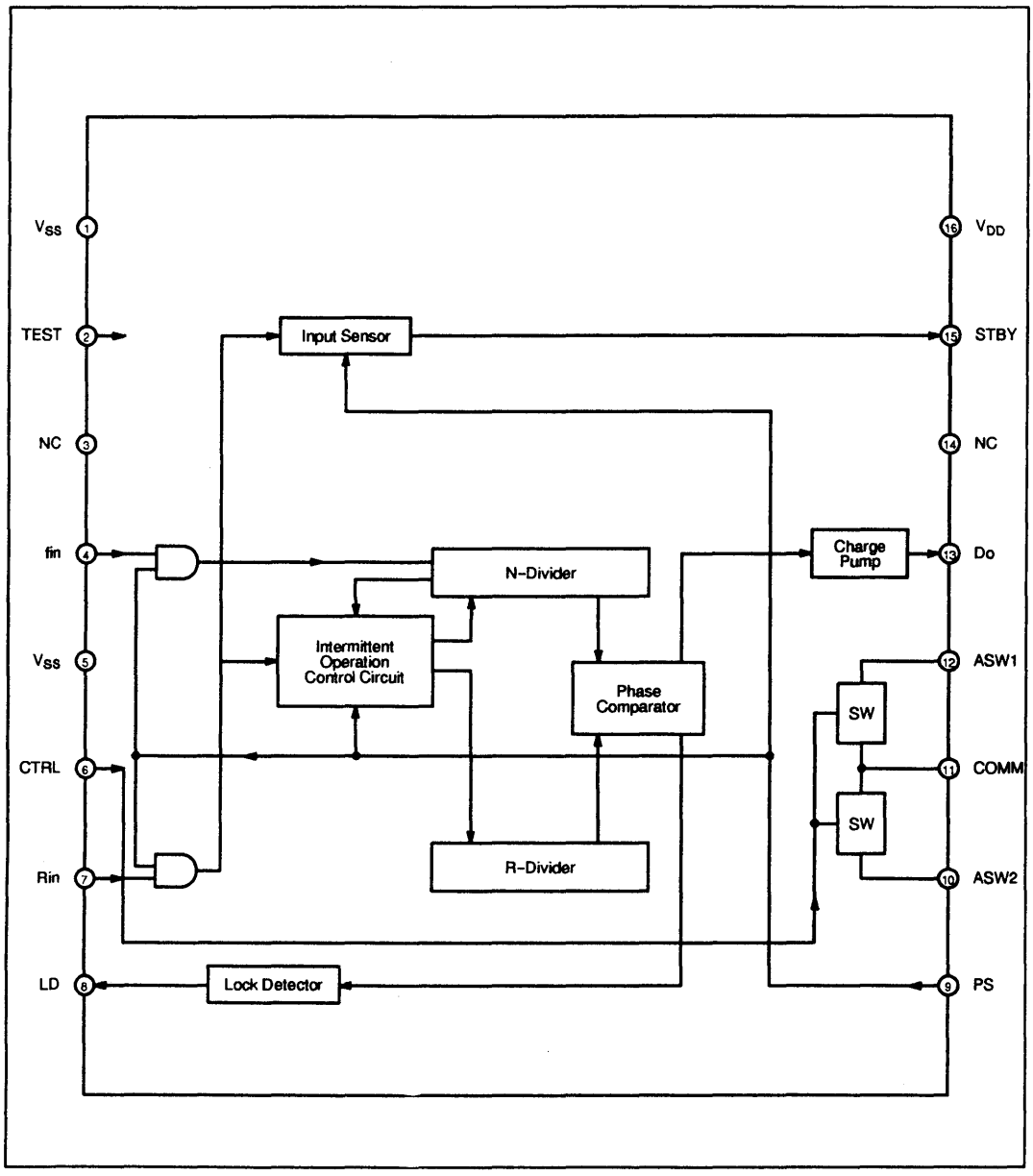
ABSOLUTE MAXIMUM RATINGS (see Note) (V_{SS} = 0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +6.0	V
Input voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output current	I_{OUT}	± 10	mA
Ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{STG}	–40 to +125	°C
Power dissipation	P_D	300	mW

Note : Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Pin Description
1	V_{SS}	–	Ground pin
2	TEST	I	Test mode pin. Leave this pin open for ordinary operation, because pull-down resistor is included.
3	NC	–	No connection
4	fin	I	N-divider input pin, and has a bias circuit and an amplifier. Connection with an external oscillator should be AC coupling.
5	V_{SS}	–	Ground pin
6	CTRL	I	Control signal input pin for the analog switches.
7	Rin	I	Reference divider input pin, and has a bias circuit and an amplifier. Connection with an external oscillator should be AC coupling.
8	LD	O	Lock signal output pin. This pin is high when a loop is locked. This pin is low when the loop is out of lock.
9	PS	I	Power save control pin. When PS is high, an active mode is selected. When PS is low, a standby mode is selected.[1]
10	ASW2	–	Analog switch 2.
11	COMM	–	Common pin of the analog switches.
12	ASW1	–	Analog switch 1.
13	Do	O	Tri-state output pin of the charge pump. The charge pump output level is changed according to combination of the R-divider output frequency fr and the N-divider output frequency fv.
14	NC	–	No connection
15	STBY	O	This pin outputs low when the standby mode is selected. When a signal is input to Rin pin after the active mode is selected, this pin outputs high.
16	V_{DD}	–	Power supply pin.

Note: [1]Refer to an intermittent operation in functional description in page 4.

FUNCTIONAL DESCRIPTIONS

1 Intermittent Operation

The intermittent operation of every MB87093A/MB87095A/MB87096A refers to the process of activating and deactivating its internal circuit for saving power dissipation. If the circuit is simply restarted from the standby state, however, an excessively large error signal might be generated, resulting in an out-of-synch lock frequency. Because the phase relationship between the reference frequency (fr) and the frequency (fv) is not stable even when they are of the same value.

To preclude this problem, every MB87093A/MB87095A/MB87096A has an intermittent mode control circuit which forces the frequencies fr and fv into the same phase other than when the MB87093A/MB87095A/MB87096A are reactivated, this minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting the PS pin high provides the active mode, and setting the PS pin low provides the standby mode and places the MB87093A/MB87095A/MB87096A into the standby state.

The MB87093A/MB87095A/MB87096A must be placed in the standby mode (PS = "L") when power is impressed.

2 Input sensor

The STBY pin outputs in the standby mode, and outputs high after receiving a signal via Rin pin when the mode switches from the standby mode into the active mode.

For example, it is possible to control a VCO by this function.

3 N-divider

The fvco of an external VCO output signal input through fin is divided by the N-divider and then output to the phase comparator as fv. It consists of a binary 10-bit N-counter. The divide ratio N of the N-divider for each MB87093A/MB87095A/MB87096A is shown in Table 1.

Table 1. N-divider's Divide Ratio N

Part Number	Divide Ratio N
MB87093A	725
MB87095A	550
MB87096A	750

4 R-divider

The R-divider divides the reference oscillation frequency (fosc) from an external reference oscillator (TCXO), and output fr to the phase comparator. It consists of a binary 6-bit R-counter. Table 2 shows the R-divider's divide ratio.

Table 2. R-divider's Divide Ratio R

Part Number	Divide Ratio R
MB87093A	64
MB87095A	64
MB87096A	128

5 Phase Comparator

The phase comparator detects the phase difference between the outputs fr and fv and generates an error signal that is proportional to the phase difference. The outputs from the phase comparator include 1) Do which takes one of the three states; namely, "L" (Low), "H" (high), and "Z" (high-impedance), 2) LD which indicates the PLL lock or unlock state.

5.1 Phase Comparator

The phase comparator detects the phase difference between fr and fv and generates an error signal that is proportional to the phase difference. Table 3 shows logical levels of Do and LD according to the phase relationship between fr and fv.

Table 3. Phase Comparator Inputs/Output Relationships

Phase Relationship	Output	
	Do	LD
fr > fv	H	L
fr = fv	High-Impedance	H
fr < fv	L	L

5.2 Phase Comparator Input/Output Waveforms

The phase comparator outputs logical levels summarized in Table 3. The pulse width of the phase comparator outputs are identical and equal to the phase difference between fr and fv as shown in Figure 1.

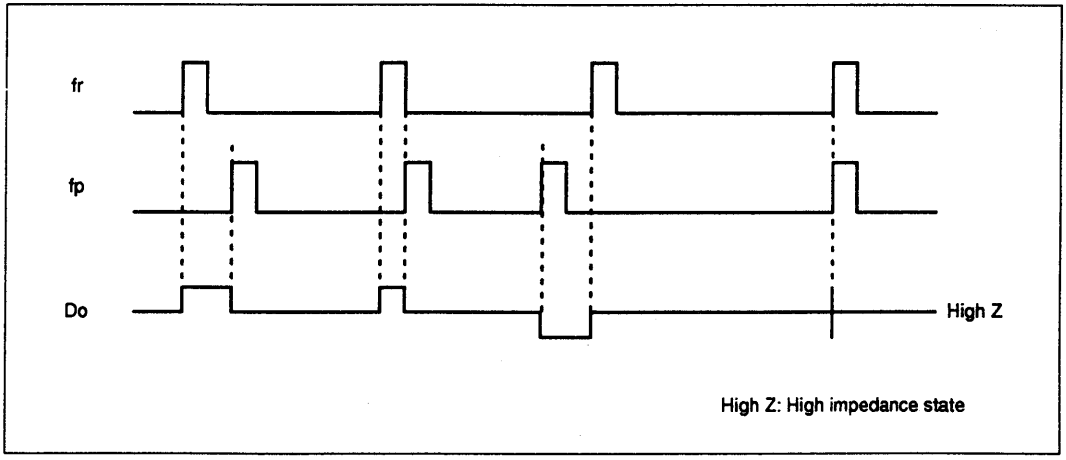


Figure 1. Phase Comparator Input/Output Waveforms (Charge Pump)

5.3 Lock Detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs high when the PLL enters the lock state and outputs low when the PLL enters the unlock state as shown in Figure 2. When pulse width of the error signal is kept zero for four (4) clocks, the lock detector outputs high as a lock signal. When it detects phase difference after the PLL is locked, low is output at once. When PS is low, the lock detector outputs high compulsorily.

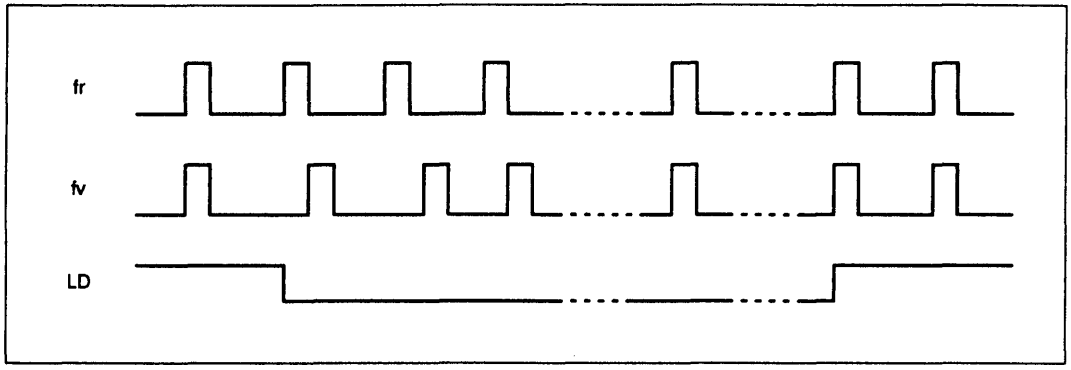


Figure 2. Phase Comparator Input/Output Waveforms (Lock Detector)

6 Analog Switch

The analog switch can be controlled by the CTRL pin. When the CTRL pin is high, each analog switch closes. When low, each analog switch opens. For example, a LPF's time constant can be changed by using a connect, as in Figure 3.

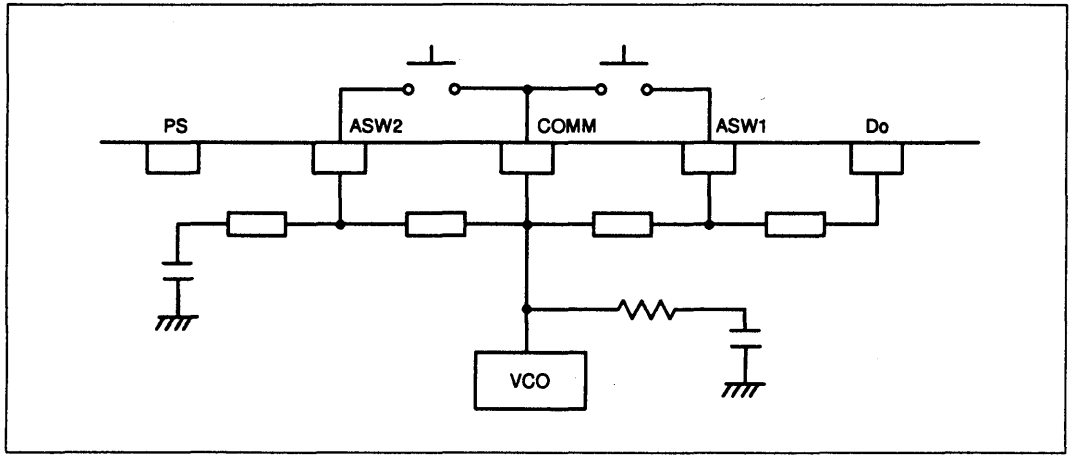


Figure 3. Application Example for Analog Switch

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	4.5 to 5.5	V
Input Voltage	V_{IN}	V_{SS} to V_{DD}	V
Ambient Temperature	T_A	−40 to +85	°C

3

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_A = −40 to +85°C)

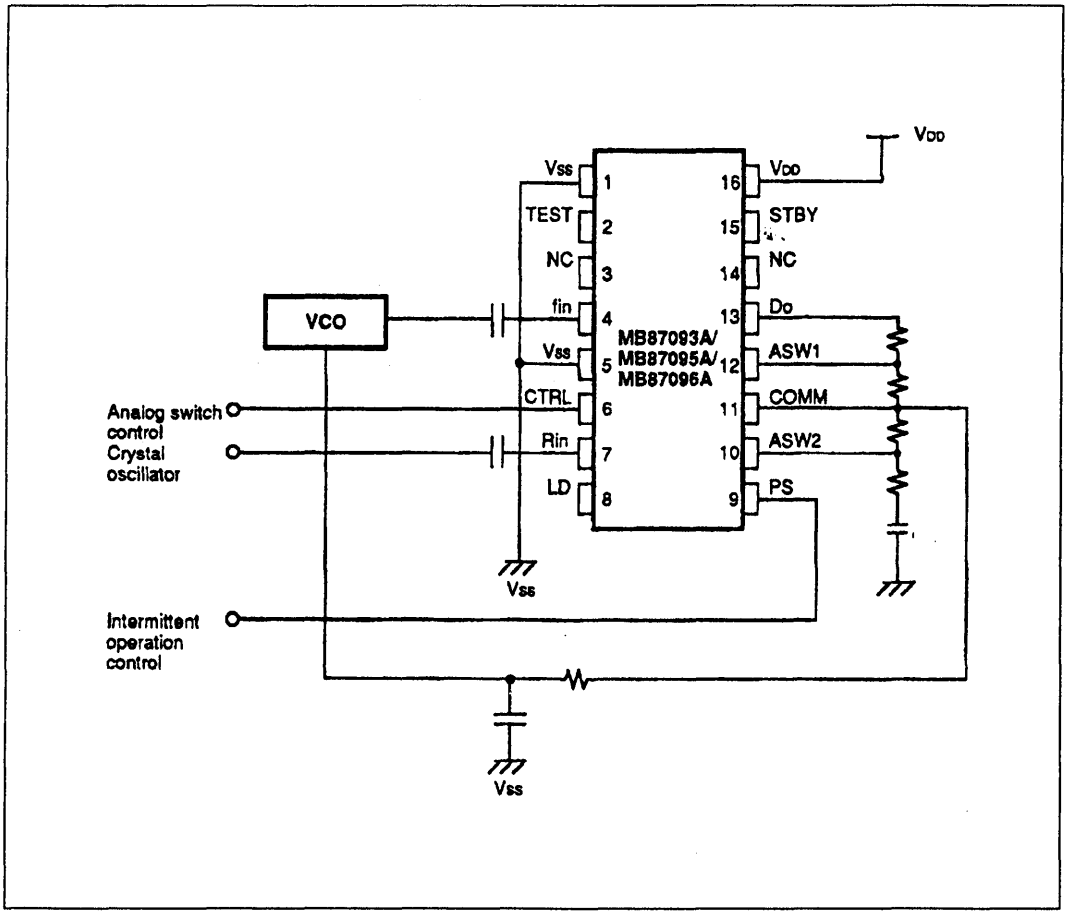
Parameter			Symbol	Conditions	Value			Unit
					Min	Typ	Max	
Input Voltage	Except fin & Rin	H Level	V_{IH}		0.7 x V_{DD}	-	-	V
		L Level	V_{IL}		-	-	0.3 x V_{DD}	
Input Sensitivity	f_{IN}		VVin	AC Coupling Amplitude	0.5	-	-	Vp-p Sine
	R_{IN}		VRin	AC Coupling Amplitude	0.5	-	-	
Input Current	Except Fin, Rin & Test	H Level	I_{IH}	V_{IN} = V_{DD}	-	-	1.0	µA
		L Level	I_{IL}	V_{IN} = V_{SS}	-	-	−1.0	
	fin Rin	H Level	I_{IH}	V_{IN} = V_{DD}	-	30	-	µA
		L Level	I_{IN}	V_{IN} = V_{DD}	-	-30	-	
Output Voltage	All outputs	H Level	V_{OH}	I_{OH} = 0µA	V_{DD} - 0.05	-	-	V
		L Level	V_{OL}	I_{OL} = 0µA	-	-	0.05	
Output Current	All outputs	H Level	I_{OH}	V_{OH} = V_{DD} −0.5V	−1.0	-	-	mA
		L Level	I_{OL}	V_{OL} = 0.5V	1.0	-	-	
Cutoff Current		Do	IZH	V_{OUT} = V_{DD}	-	1.0	-	µA
			IZL	V_{OUT} = V_{SS}	-	-1.0	-	
Supply Current		Active Mode	I_{DDOP}	*1	-	10	-	mA
		Standby Mode	I_{DDS}	*2	-	10	-	µA
Maximum Operating Frequency		REF Section	fmaxd	R-Divider	16	-	-	MHz
	MB87093A	PD Section	fmaxp	N-Divider	145	-	-	
	MB87095A	PD Section	fmaxp	N-Divider	110	-	-	
	MB87096A	PD Section	fmaxp	N-Divider	90	-	-	

Notes:

*1: MB87093A: fin = 145 MHz, Rin = 12.8 MHz, Outputs are opened.
MB87095A: fin = 110 MHz, Rin = 12.8 MHz, Outputs are opened.
MB87096A: fin = 90 MHz, Rin = 15.36 MHz, Outputs are opened.

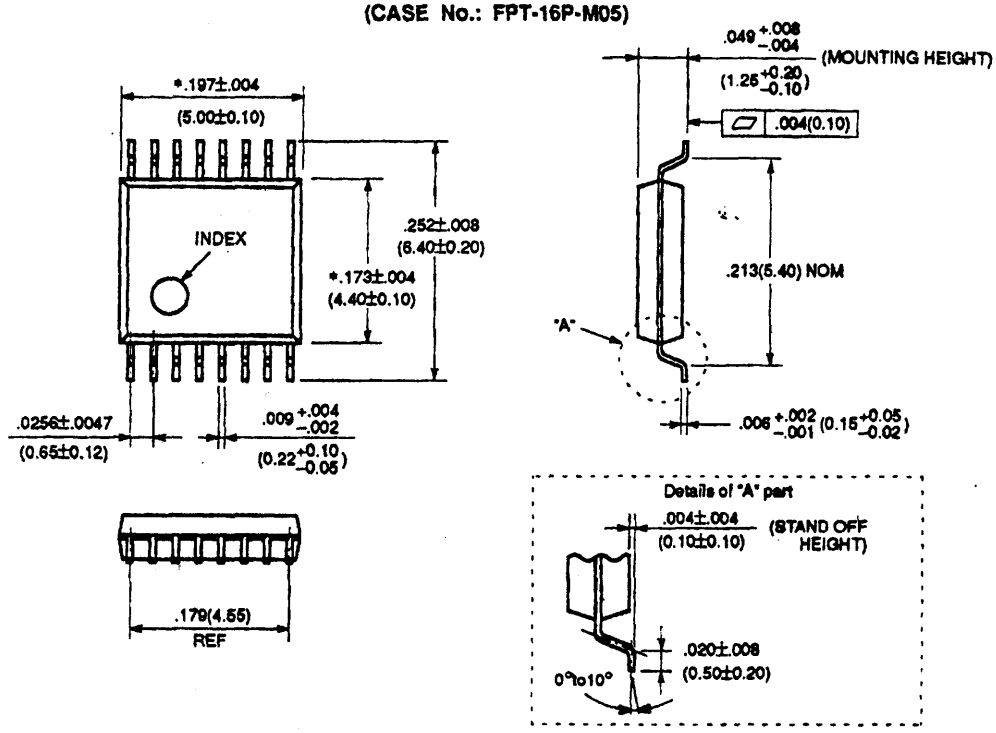
*2: Inputs set low. Outputs are opened.

TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*: This dimension does not include resin protruction.

Dimensions in inches (millimeters)

DS04–21213–1aE

FUJITSU

DATA SHEET

MB87094 *ASSP*

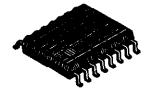
Serial Input PLL Frequency Synthesizer

3

CMOS SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTION

The Fujitsu MB87094 is a CMOS serial input Phase Locked Loop (PLL) frequency synthesizer. It incorporates an input amplifier, a programmable divider (binary 11-bit programmable counter and binary 7-bit swallow counter), a phase comparator, a charge pump, an oscillator circuit, a programmable reference divider (binary 12-bit programmable reference counter), a shift register/control register, a data latch, an intermittent mode control circuit. A power save control input pin (PS) for the intermittent mode control circuit is used to switch between the stand-by and active modes. This is used for phase synchronization at the beginning of operation from a stand-by mode. The MB87094 permits construction of PLL frequency synthesizers with operating frequencies of up to 15 MHz.

PRELIMINARY



(FPT-16P-M05)

FEATURES

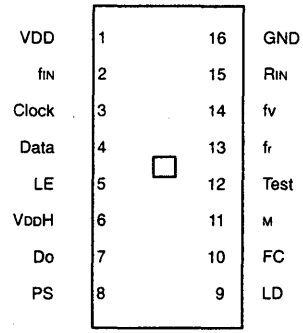
- Low power supply voltage: VDD = 1.1 to 1.7V
  $V_{DD}H$ = 2.6 to 3.3V
- Intermittent mode control circuit
- Ambient temperature range : TA = –10°C to 50°C
- Plastic 16-pin SSOP package (Suffix: –PFV)
- Setting the divide ratio
  Use the below formula to define the parameters for setting the divide ratio

  $\underline{fVCO} = (\underline{N} \times \underline{M} + \underline{A}) \times (\underline{fOSC} \div \underline{R})$ (N>A)

  (fVCO) Output frequency of the external VCO
  (N) Preset divide ratio of binary11-bit programmable counter (5 to 2047)
  (M) Preset modulus of external dual modulus prescaler (M/M+1)
  (A) Preset divide ratio of binary 7-bit swallow counter value (0 to 127)
  (fOSC) Reference oscillator frequency
  (R) Preset divide ratio of binary 12-bit programmable reference counter (5 to 4095)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (See NOTE) (GND=0V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 to +5.0	V
	$V_{DD}H$	−0.5 to +5.0	V
Input Voltage	V_{IN}	−0.5 to V_{DD}+0.5	V
	$V_{IN}H$	−0.5 to $V_{DD}H$+0.5	V
Output Voltage	V_{OUT}	−0.5 to V_{DD}+0.5	V
	$V_{OUT}H$	−0.5 to $V_{DD}H$+0.5	V
Output Current	I_{OUT}	±10	mA
Ambient Temperature	T_A	−10 to +50	°C
Storage Temperature	Tstg	−40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

Pin No	Pin Name	I / O	Interface *1	Description
1	V_{DD}	–	1V	Power supply pin
2	f_{IN}	I	1V	Programmable divider input pin This pin has a bias circuit and an amplifier. Connection with an external voltage controlled oscillator (VCO) should be AC coupling.
3	Clock	I	3V	Clock input pin for the shift register Data are loaded at the rising edge of the clock. A Schmitt trigger circuit is used.
4	Data	I	3V	Serial data input pin for setting divide ratio of dividers A Schmitt trigger is used.
5	LE	I	3V	Load enable signal input pin When LE is set to high, the data in the shift register is sent to the latch. A Schmitt trigger is used.
6	$V_{DD}H$	–	3V	Power supply pin
7	Do	O	3V	Tri-state charge pump output pin A constant-current feed charge pump is used and its output current can be controlled by the external resistor R_{RC}. The Do output level is inverted by FC. The charge pump output level is changed according to the combination of the programmable reference divider output frequency (fr) and the programmable divider output frequency (fv).
8	PS	I	3V	Power save control pin When PS is set to "H", an active mode is selected. When PS is set to "L", a standby mode is selected. *2
9	LD	O	3V	Phase comparator output pin When a PLL is locked, this pin outputs "H". When the PLL is unlocked, it outputs "L".
10	FC	I	3V	Phase comparator input switch pin *3
11	M	O	3V	Control output for external dual modulus prescaler This output level is synchronized with the falling edge of the f_{IN} input signal Pulse swallow function: M = "H" : Preset modulus factor M of an external prescaler M = "L" : Preset modulus factor M+1 of an external prescaler
12	Test	I	1V	Test mode pin The test mode is selected by setting this pin to "H". Leave this pin open for ordinary operation, because a pull-down resistor is used.
13	fr	O	1V	Monitoring pin for the programmable reference divider output
14	fv	O	1V	Monitoring pin for the programmable divider output
15	R_{IN}	I	1V	Connect pin with external reference oscillator (TCXO, etc.). A bias circuit and an amplifier are used. Connection with TCXO should be an AC coupling.
16	GND	–	–	Ground pin

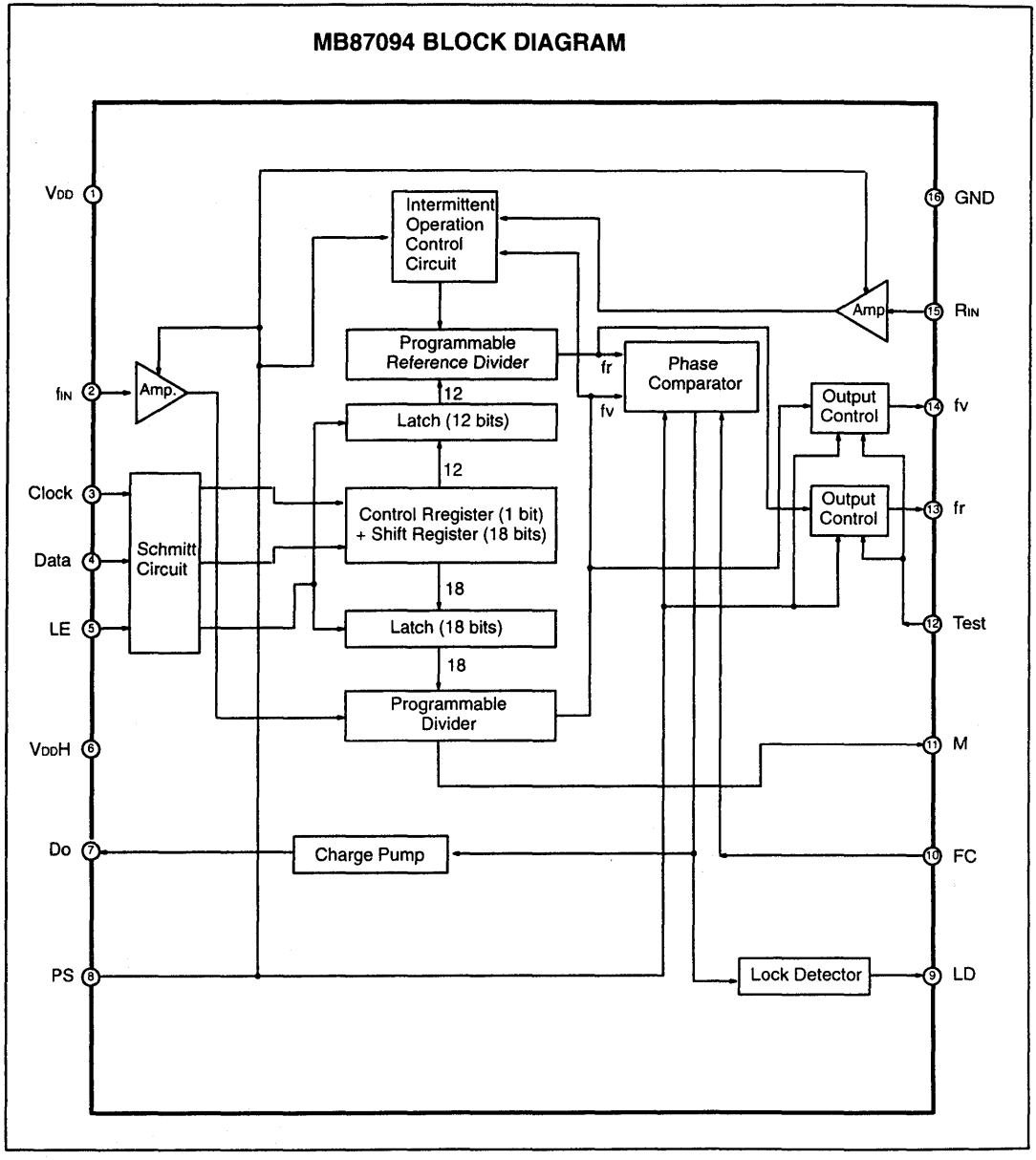
Note:

*1 : In consideration of the interface with external circuits like a microcontroller, each pin is set to either 3V interface or 1V interface.

*2 : When power is impressed, the PS pin has to be set to "L". Refer to an intermittent operation in the functional description.

*3 : Refer to the phase comparator in the functional description.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

1. Circuit Description

1.1 Intermittent Operation

The intermittent operation of the MB87094 refers to the process of activating and deactivating its internal circuit as necessary thus saving electric energy otherwise consumed by the circuit. If the circuit is simply restarted from the standby state, however, the phase relationship between the reference frequency (fr) and the programmable frequency (fv), which are the input to the phase comparator, is not stable even when they are of the same value. This may cause the phase comparator to generate an excessively large error signal, resulting in an out-of-synch lock frequency.

To preclude the occurrence of this problem, the MB87094 has an intermittent mode control circuit which forces the frequencies into phase with each other when the MB87094 is reactivated, thus minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting the PS pin high provides the normal operation mode and setting the pin low provides the standby mode and places the MB87094 into the standby state. The MB87094 behavior in the active and standby modes is summarized below.

- Active mode (PS = "H")
  All MB87094 circuits are active and provide the normal PLL operation.

- Standby mode (PS = "L")
  The MB87094 stops every circuit that consumes power heavily and that causes little inconvenience when deactivated and enters the low-power dissipation state. The Do and LD pins take the same state as when the PLL is locked. The Do pin becomes a high-impedance state and the input voltage to the voltage control oscillator (VCO) is maintained at the same level as in the active mode (that is, lock state) according to a time constant of a low pass filter (LPF). Consequently, the output frequency from the VCO (fvco) is maintained at approximately the lock frequency.

  The MB87094 continues the intermittent mode operation by alternating the active and standby modes. When it switches from standby to active modes, it forces the phase of fr and fp to correspond and minimize the error signal. In this way, the MB87094 can keep the power consumption of its entire circuitry at the minimum.

  The MB87094 must be placed in the standby mode (PS = "L") when power is impressed.

1.2 Programmable Divider

The fvco of an external VCO output signal or the fPSC of a prescaler output signal, input through fIN, are divided by the programmable divider and then output to the phase comparator as fv. It consists of a binary 7-bit swallow counter, binary 11-bit programmable counter, and a controller which controls the divide ratio of the prescaler.

The following are their divide ratios:

- Swallow counter: A = 0 to 127
- Programmable counter: N = 5 to 2047

The MB87094 uses the pulse swallow method; consequently, the divide ratios of the swallow and programmable counters must satisfy the relationship N > A.

On the supposition that the divide ratio of a prescaler is M/M+1 (M=128), the total divide ratio of the programmable divider is calculated as follows:

Total divide ratio = (M+1)xA+Mx(N–A) = MxN+A = 128xN+A

When N is set within $5 \leq N \leq 127$, the divide ratio A of the swallow counter can take values $0 \leq A \leq N-1$ because N must be greater than A. For example, $0 \leq A \leq 19$ is allowed when N = 20 but $20 \leq A \leq 127$ is not allowed in that case. Consequently, $N \geq 128$ must be satisfied for the total divide ratio to be set within $0 \leq A \leq 127$.

1.3 Programmable Reference divider

The programmable reference divider divides the reference oscillation frequency (fosc) from an external reference oscillator (TCXO) connected with AC coupling, and outputs fr to the phase comparator. It consists of a 12–bit binary programmable reference counter. The following divide ratio is used:

- Programmable reference counter: R = 5 to 4095

The fr and f_{OSC} have the following relationship:

- fr = $f_{OSC} \div R$

1.4 Phase Comparator

The phase comparator detects the phase difference between the outputs fr and fv and generates an error signal that is proportional to the phase difference. The outputs from the phase comparator include 1) DO which takes on one of the three states, "L" (low), "H" (high), or "Z" (high impedance), and 2) LD which indicates the PLL lock or unlock state.

1.4.1 Phase Comparator

The phase comparator detects the phase difference between fr and fv and generates an error signal that is proportional to the phase difference. The roles of the fr and fp supplied to the phase comparator may be reversed by switching the logical input level of the FC pin. This inverts the logical level of the DO output. The logical level of DO may be selected according to the characteristics of the external LPF and the VCO. (Refer to Table 1.)

Table 1. Phase Comparator Inputs/Output Relationships

Phase Relationship \ Output	FC="L"	FC="H"
	DO	DO
fr > fv	L	H
fr = fv	High-Impedance	
fr < fv	H	L

1.4.2 Phase Comparator Input/Output Waveforms

The phase comparator outputs logic levels summarized in Table 1, according to the phase difference between fr and fv phase differences. The pulse width of the phase comparator outputs are identical and equal to the phase difference between fr and fv as shown in Figure 1.

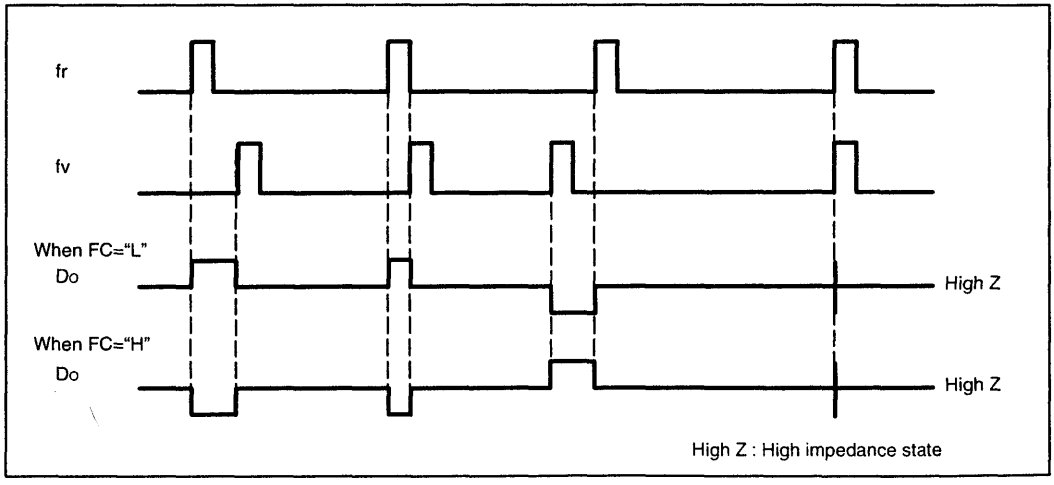


Figure 1. Phase Comparator Input/Output Waveforms (Charge Pump)

1.4.3 Lock Detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs "H" when the PLL enters the lock state and outputs "L" when the PLL enters the unlock state as shown in Figure 2. When the pulse width of the error signal is kept zero for four (4) clocks, the lock detector outputs "H" as a lock signal. When it detects a phase difference after the PLL is locked, "L" is output at once.

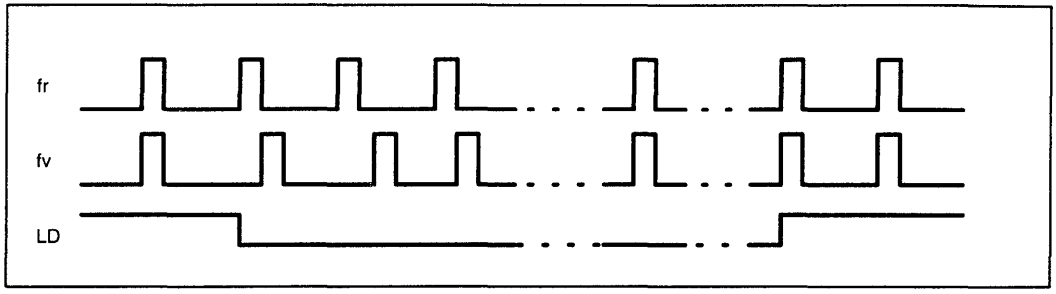


Figure 2. Phase Comparator Input/Output Waveform (Lock Detector)

2. Setting the Divide Ratio

2.1 Serial Data Format

The format of the serial data is shown in Figure 3. The serial data is composed of a control bit and divide ratio setting data. The control bit selects the programmable divider or the programmable reference divider.

In the case of the programmable reference divider, serial data consists of 12 bits for the programmable reference counter and 1 control bit, as shown in Figure 3.1. In the case of the programmable divider, the serial data consists of 18 bits (7 bits for the swallow counter and 11 bits for the programmable counter) and 1 control bit, as shown in Figure 3.2.

The control bit is set to 0 to select the serial data for the programmable divider and to 1 to select the serial data for the programmable reference divider.

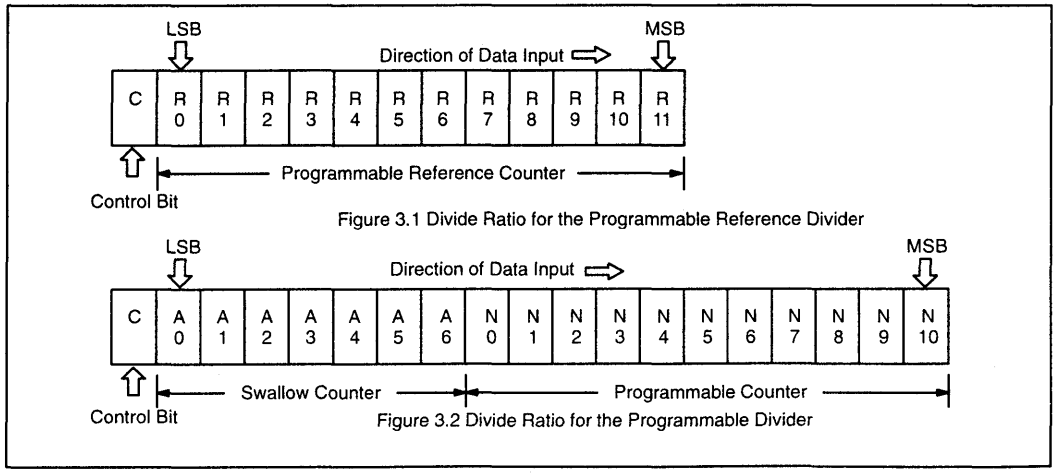


Figure 3. Serial Data Format

2.2 The Flow of Serial Data

Serial data is received via the data pin in synchronization with the Clock input and is loaded into the shift register which contains the divide ratio setting data and into the control register which contains the control bit. The logical product (through the AND gate in Figure 4) of LE and the control register output (i.e., control bit) is fed to the Enable input of the latches. Accordingly, when LE is set high, the latch for the divider identified by the control bit is enabled and the divide ratio data from the shift register is loaded into the selected counter.

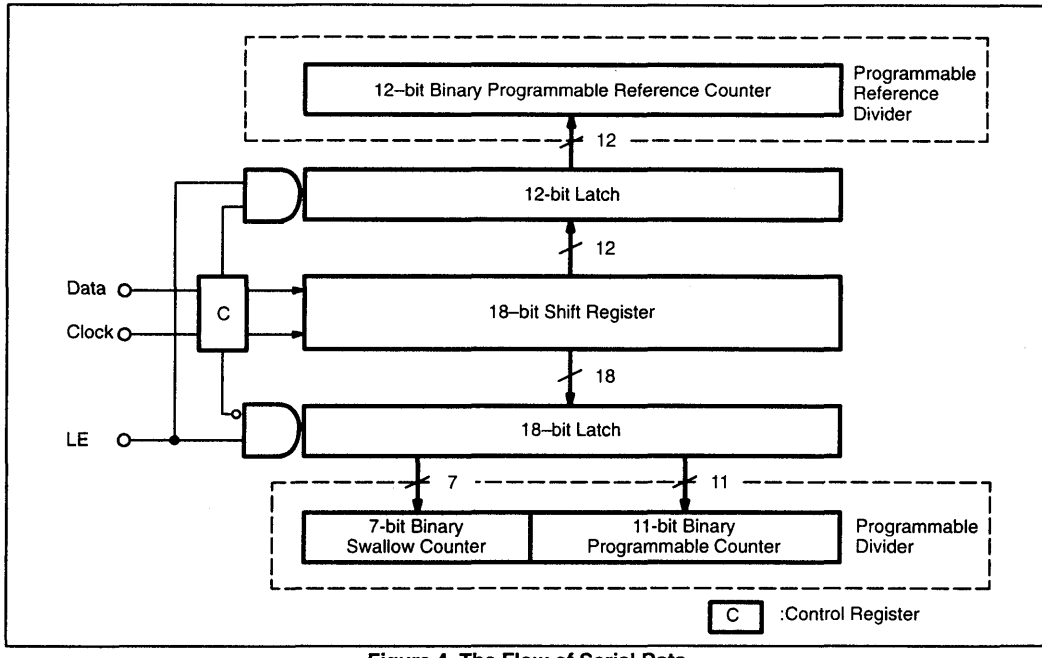


Figure 4. The Flow of Serial Data

2.3 Setting the Divide Ratio for the Programmable Divider

Columns A0 to A6 of Table 2.1 represent the divide ratio of the swallow counter and columns N0 to N10 of Table 2.2 represent the divide ratio of the programmable counter. The control bit is set to 0.

Table 2. Divide Ratio for the Programmable Divider

Table 2.1 Swallow Counter Divide ratio A

Divide Ratio A	A 0	A 1	A 2	A 3	A 4	A 5	A 6
0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •
127	1	1	1	1	1	1	1

Table 2.2 Programmable Counter Divide ratio N

Divide Ratio N	N 0	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9	N 10
5	1	0	1	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
2047	1	1	1	1	1	1	1	1	1	1	1

2.4 Setting the Divide Ratio for the Programmable Reference Divider

Columns R0–R11 of Table 3 represent the divide ratio of the programmable reference counter. The control bit is set to 1.

Table 3. Divide Ratio for the Programmable Reference Divider

Divide Ratio R	R 0	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11
5	1	0	1	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
4095	1	1	1	1	1	1	1	1	1	1	1	1

2.5 Monitor Mode

Setting both the PS pin and TEST pin high, the monitor mode is available. The fr and fv pins typically output low. In the monitor mode, the fr pin outputs signals from the programmable reference divider, and the fv pin outputs signals from the programmable divider.

2.6 Serial Data Input Timing

The MB87094 uses 19 bits of serial data for the programmable divider and 13 bits for the programmable reference divider. When more bits of serial data than are defined for the target divider are received, only the last valid serial data bits are effective.
To set the divide ratio for the MB87094 dividers, it is necessary to supply the Data, Clock, and LE signals at the timing shown in Figure 5.

t1 (≥1 µs) :Data setup time t2 (≥1 µs): Data hold time t3 (≥1 µs): Clock pulse width
t4 (≥1 µs) :LE setup time to the falling edge of the last clock t5 (≥1 µs): LE pulse width

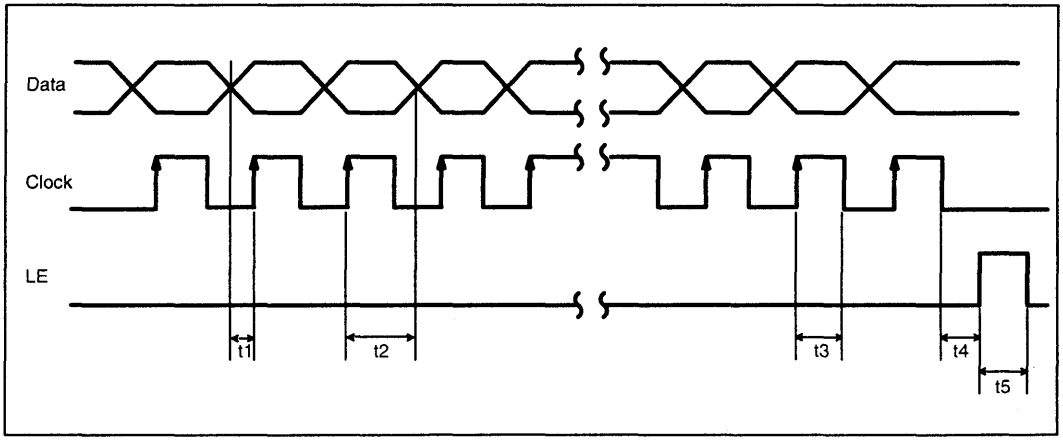


Figure 5. Serial Data Input Timing

Since the divide ratios are unpredictable when the MB87094 is turned on, it is necessary to initialize the divide ratio for both dividers. As shown in Figure 6, after setting the divide ratio for one divider (e.g., programmable reference divider), set LE to the "H" level before setting the divide ratio for the other divider (e.g., programmable divider). To change the divide ratio of one divider after initialization, input the serial data only for that divider (the divide ratio for the other divider is preserved).

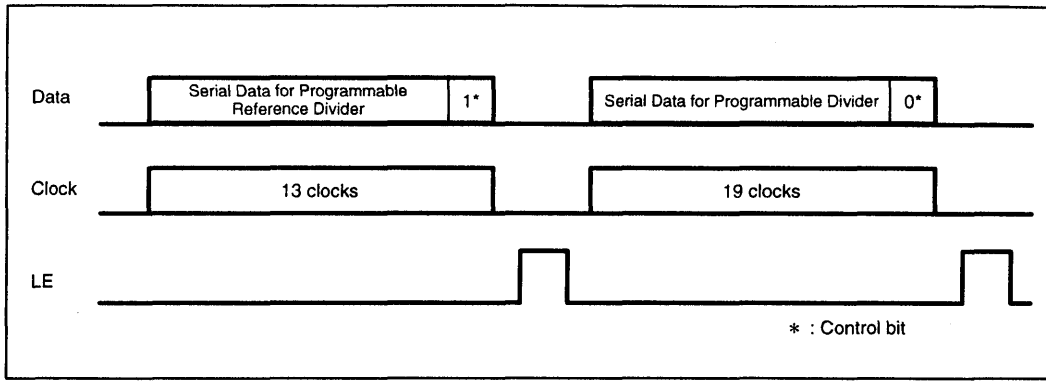


Figure 6. Serial Data Setting Procedure

RECOMMENDED OPERATING CONDITIONS

GND = 0V

Parameter	Symbol	Value	UNIT
Power Supply Voltage	V_{DD}	1.1 to 1.7	V
	$V_{DD}H$	2.6 to 3.3	V
Input Voltage	V_{IN}	GND to V_{DD}	V
	$V_{IN}H$	GND to $V_{DD}H$	V
Ambient Temperature	T_A	−10 to +50	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

(V_{DDH} = 3.0V, V_{DD} = 1.1V, GND = 0V, T_A = −10 to +50°C)

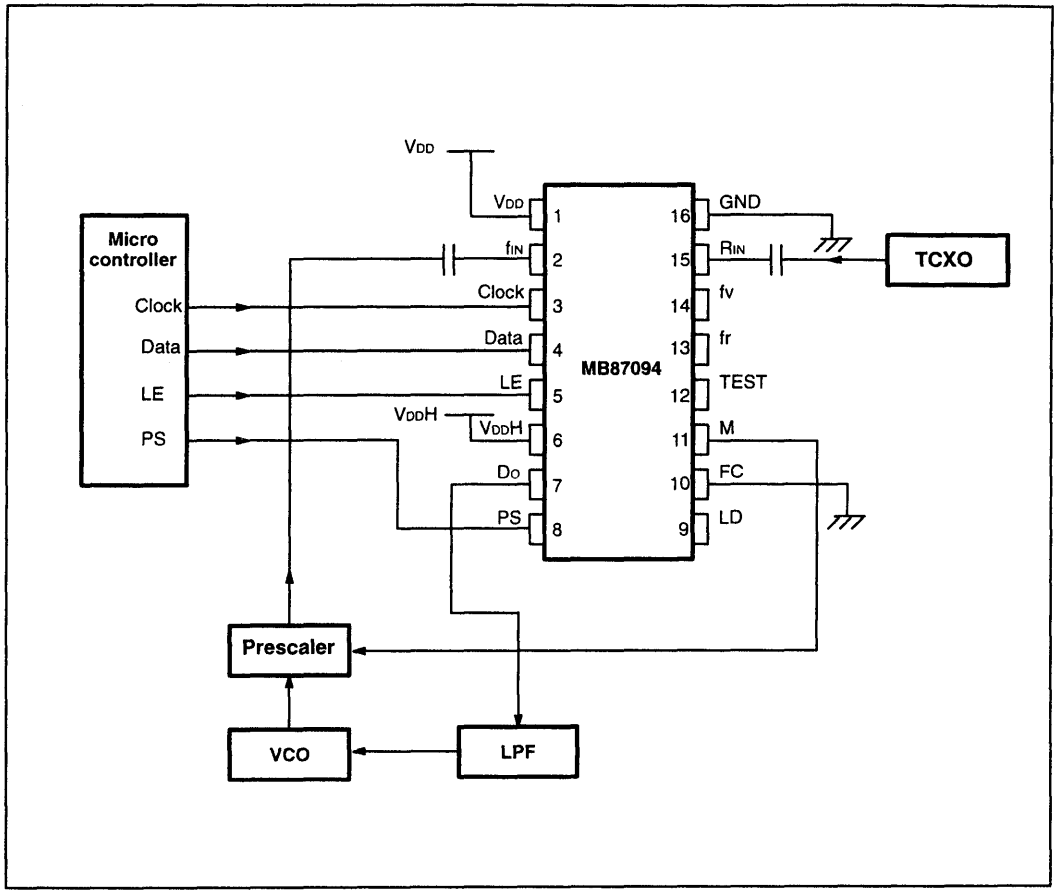
Parameter			Symbol	Conditions	Value			Unit
					Min	Typ.	Max	
Input Voltage	TEST	H Level	V_{IH}	—	0.77	–	–	V
		L Level	V_{IL}	—	–	–	0.33	
	CLK, Data, LE, PS, FC	H Level	V_{IH}	—	2.10	–	–	V
		L Level	V_{IL}	—	–	–	0.90	
Input Sensitivity	f_{IN}		Vfpp	AC Coupling Amplitude	0.5	–	–	Vp–p Sine
	R_{IN}		VSIN	AC Coupling Amplitude	0.5	–	–	
Input Current	CLK, Data, LE, PS, FC	H Level	I_{IH}	V_{IH} = V_{DDH}	–	1.0	–	µA
		L Level	I_{IL}	V_{IL} = GND	–	−1.0	–	
	f_{IN}		I_{fIN}	V_I = GND to V_{DD}	–	±30.0	–	µA
	R_{IN}		I_{OSC}	V_I = GND to V_{DD}	–	±30.0	–	µA
	TEST (pull down pin)		I_{TEST}	V_{IH} = V_{DD}	–	50.0	–	µA
Output Voltage	fr, fv	H Level	V_{OH}	I_{OH} = 0µA	1.05	–	–	V
		L Level	V_{OL}	I_{OL} = 0µA	–	–	0.05	
	Do, LD, M	H Level	V_{OH}	I_{OH} = 0µA	2.95	–	–	V
		L Level	V_{OL}	I_{OL} = 0µA	–	–	0.05	
Output Current	fr, fv	H Level	I_{OH}	V_{OH} = 0.6V	−0.2	–	–	mA
		L Level	I_{OL}	V_{OL} = 0.5V	0.2	–	–	
	Do, LD, M	H Level	I_{OH}	V_{OH} = 2.5V	−0.4	–	–	mA
		L Level	I_{OL}	V_{OL} = 0.5V	0.4	–	–	
Cutoff Current		Do	IOFFH	V_{OH} = V_{DDH}	–	–	100	nA
			IOFFL	V_{OL} = GND	–	–	100	nA
Supply Current		Active Mode	I_{OP}	*1	–	–	1.0	mA
		Stand–by Mode	I_{SB}	*2	–	–	20.0	µA
Maximum Operating Frequency		REF Section	fMAXd	Programmable Reference Divider	15	–	–	MHz
		PD Section	fMAXp	Programmable Divider	15	–	–	

Note;

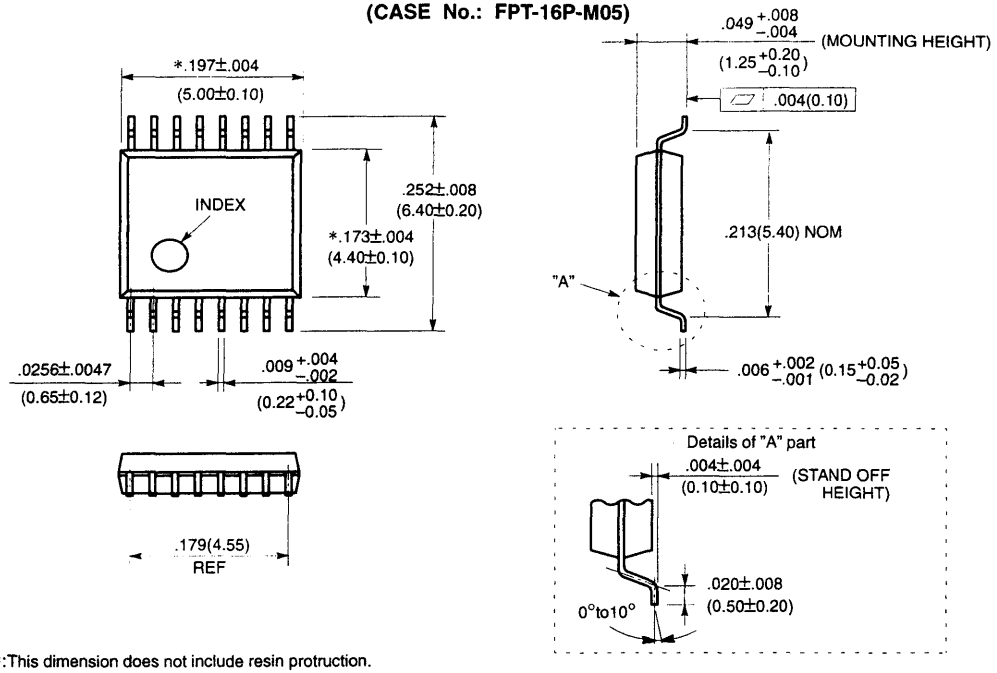
*1: f_{IN} = R_{IN} = 15MHz(0.5Vpp), I_{OP} = I_{DD} (1.4V) + I_{DDH} (3V) x 3.3

*2: Conditions for measuring the standby current (I_{SB}) are the same as the case of the active mode (I_{OP}).

TYPICAL APPLICATION EXAMPLE



16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

SECTION 4

Super PLLs (Single Chip PLLs/Prescalers) – *At a Glance*

Fujitsu is one of only a few semiconductor manufacturers to offer single–chip PLL/Prescaler devices and was the creator of the industry standard MB1501. These devices are manufactured using an advanced BiCMOS process that combines high speed and low power consumption in a single chip. With the increased emphasis on board space reduction to improve cost, reliability, and overall end product size for portable applications, these single–chip devices are ideal solutions for wireless systems designers.

		Prescaler		PLL					
Page Number	Device Part Number	f_{IN} (max)	Divide Ratio	N Program Counter	A Swallow Counter	R Reference Counter	I_{CC} (typ)	V_{CC}	Package
4-5	MB15A01	1.1 GHz	64/65 128/129	Binary 5–2047	Binary 0–127	Binary 6–16383	6.5 mA	3 V	16–pin SSOP
4-19	MB15B01**	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	13 mA	3 V	20–pin SSOP
4-33	MB1501*	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	15 mA	3–5 V	16–pin DIP, SOP
4-33	MB1501H*	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	15 mA	3–5 V	16–pin SOP
4-33	MB1501L*	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	15 mA	3–5 V	16–pin SOP
4-51	MB15A02	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 6–16383	7 mA	5 V	16–pin SSOP
4-67	MB1502	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	8 mA	5 V	16–pin SOP
4-67	MB1502H	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	8 mA	5 V	16–pin SOP
4-81	MB15B03**	1.1 GHz	64/65 128/129	Binary 5–2047	Binary 0–127	Binary 6–16383	10 mA	3 V	16–pin SSOP
		0.3 GHz	16/17 32/33						
4-95	MB15F03**	2.0 GHz	64/65 128/129	Binary 5–2047	Binary 0–127	Binary 6–16383	9 mA	3 V	16–pin SSOP
		0.5 GHz	16/17 32/33						
4-109	MB1503	1.1 GHz	128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	8 mA	5 V	16–pin SOP
4-125	MB1504*	520 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	Binary 8–16383	10 mA	3–5 V	16–pin DIP, SOP
4-125	MB1504H*	520 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	Binary 8–16383	10 mA	3–5 V	16–pin SOP
4-125	MB1504L*	520 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	Binary 8–16383	10 mA	3–5 V	16–pin SOP

* Not for new designs
** Dual PLLs/Prescalers

Super PLLs (Single Chip PLLs/Prescalers) – *At a Glance (Cont.)*

		Prescaler		PLL					
Page Number	Device Part Number	f_{IN} (max)	Divide Ratio	N Program Counter	A Swallow Counter	R Reference Counter	I_{CC} (typ)	V_{CC}	Package
4-143	MB15E05	2.0 GHz	64/65 128/129	Binary 5–2047	Binary 0–255	Binary 8–16383	6 mA	3 V	16–pin SSOP
4-157	MB1505	600 MHz	32/33 64/65	Binary 16–2047	Binary 0–63	Binary 8–16383	6 mA	5 V	16–pin SOP
4-143	MB15E06	2.5 GHz	64/65 128/129	Binary 5–2047	Binary 0–255	Binary 8–16383	7 mA	3 V	16–pin SSOP
4-169	MB1506	2.0 GHz	128/129 256/257	Binary 5–2047	Binary 0–255	Binary 8–16383	18 mA	5 V	20–pin SSOP
4-185	MB1507	2.0 GHz	128/129 256/257	Binary 16–2047	Binary 0–255	Binary 8–16383	18 mA	5 V	16–pin SOP
4-197	MB1508	2.5 GHz	256/272 512/528	Binary 32–4095	Binary 0–31	256, 512 1024, 2048	16 mA	5 V	20–pin SOP
4-207	MB1509**	400 MHz	32/33 64/65	Binary 16–2047	Binary 0–127	512, 1024	8 mA	3 V	20–pin SOP
4-221	MB15U10**	1.1 GHz	NA	Binary 1024– 131071	NA	Binary 6–4095	7 mA	3 V	20–pin SSOP
4-231	MB1510**	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	512, 1024	15 mA	3–5 V	20–pin SOP
4-243	MB15B11**	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	9.5 mA	3 V	20–pin SSOP
		0.4 GHz	32/33 64/65						
4-257	MB1511	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	7 mA	3–5 V	20–pin SSOP
4-269	MB1512	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	8 mA	5 V	20–pin SSOP
4-281	MB15B13**	1.1 GHz	64/65 128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	13 mA	3 V	20–pin SSOP
4-295	MB1513	1.1 GHz	128/129	Binary 16–2047	Binary 0–127	Binary 8–16383	8 mA	5 V	20–pin SSOP
4-309	MB1514**	400 MHz	64/65	Binary 16–2047	Binary 0–127	1700	8 mA	3 V	20–pin SOP
4-323	MB1515	2.5 GHz	256/272 512/528	Binary 32–4095	Binary 0–31	256, 512 1024, 2048	16 mA	5 V	20–pin SSOP

** Dual PLLs/Prescalers

Super PLLs (Single Chip PLLs/Prescalers) – *At a Glance (Cont.)*

		Prescaler		PLL					
Page Number	Device Part Number	f_{IN} (max)	Divide Ratio	N Program Counter	A Swallow Counter	R Reference Counter	I_{CC} (typ)	V_{CC}	Package
4-337	MB15A16	1.2 GHz	64/65 128/129	Binary 5–2047	Binary 0–127	Binary 6–16383	6.5 mA	3 V	16–pin SSOP
4-349	MB1516A	1.1 GHz	64/65 128/129	Binary 5–2047	Binary 0–127	Binary 6–16383	6.5 mA	3 V	16–pin SSOP
4-365	MB1517A	2.0 GHz	64/65 128/129	Binary 5–2047	Binary 0–127	Binary 6–16383	14 mA	3 V	16–pin SSOP
4-391	MB1518	2.5 GHz	512/528	Binary 32–511	Binary 0–31	512	16 mA	5 V	16–pin SOP
4-401	MB15A19**	600 MHz	64/65	Binary 16–2047	Binary 0–127	256, 2048	11 mA	3–5 V	20–pin SOP
4-415	MB1519**	600 MHz	64/65	Binary 16–2047	Binary 0–127	512, 1024	11 mA	3–5 V	20–pin SOP
4-429	MB15Sxx Series	300 MHz	16/17	Binary 5–4095	Binary 0–31	Binary 5–4095	3.5 mA	3 V	8–pin SSOP
4-437	MB15S02	284 MHz 116 MHz	16/17	Fixed 17 Fixed 7	Fixed 12 Fixed 4	Fixed 13 Fixed 13	3.5 mA	3 V	8–pin SSOP

** Dual PLLs/Prescalers

DS04–21234–1aE

FUJITSU

DATA SHEET

MB15A01 ASSP

1.1GHz PLL FREQUENCY SYNTHESIZER

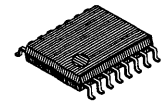
4

Low power serial input PLL frequency synthesizer with 1.1GHz prescaler

The Fujitsu MB15A01, utilizing Bi-CMOS technology, is a single chip serial input PLL frequency synthesizer with pulse swallow function.
The MB15A01 contains a 1.1GHz two modulus prescaler that can select either a 64/65 or 128/129 divide ratio.
The MB15A01 can operate from a single +3 V supply. Fujitsu's advanced technology achieves an Icc of 6.5 mA (typical).

Functions

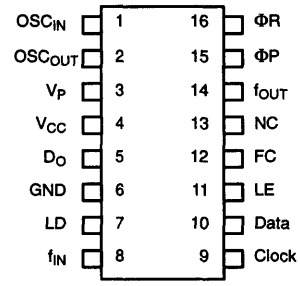
- High operating frequency : f_{IN} = 1.1 GHz max. (P_{IN} = –10 dBm)
- Pulse-swallow function : Dual-modules prescaler with selectable 64/65 and 128/129 divide ratios
- Low power supply current : I_{CC} = 6.5 mA typ. at 3 V
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter: 5 to 2,047
- Serial input 15-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit switch counter sets prescaler divide ratio
- Two types of phase comparator output selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16–pin SSOP package



FPT-16P-M05

PIN ASSIGNMENT

(TOP VIEW)



(FPT–16P–M05)

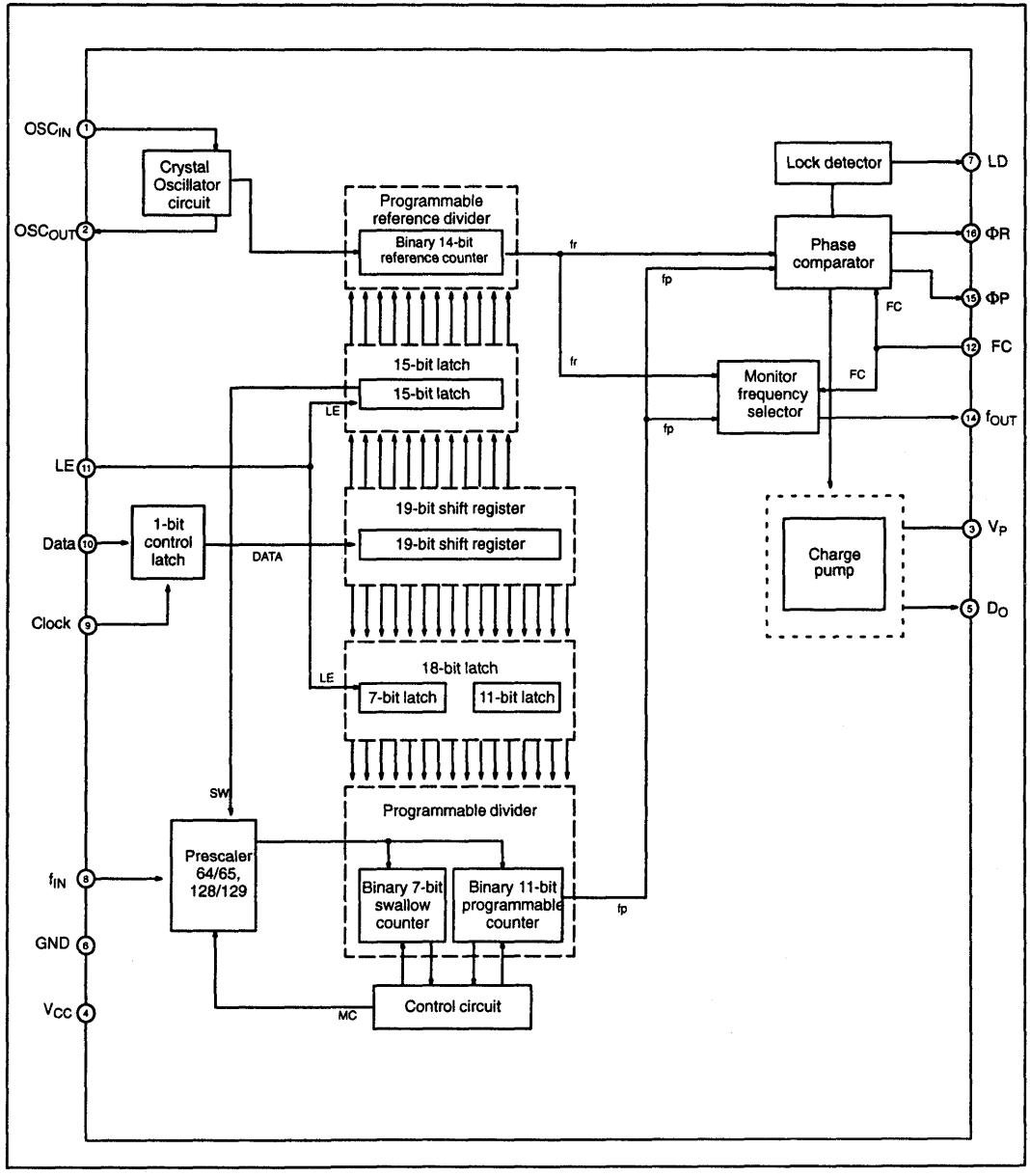
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Ratings	Symbol	Value	Unit	Remark
Supply voltage	V_{CC}	–0.5 to +5.0	V	
	V_P	V_{CC} to 8.0	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	–0.5 to 6.0	V	ΦP
Output current	I_O	±10	mA	
Storage temperature	Tstg	–55 to +125	°C	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output Connection for external crystal.
3	V_P	–	Power supply input for charge pump When the internal charge pump is not used, V_P pin needs to be connected to V_{CC}.
4	V_{CC}	–	Power supply
5	D_O	O	Charge pump output
6	GND	–	Ground
7	LD	O	Lock detector output The output level is usually high. Only when there is a phase error between fr and fp, LD becomes low for the period corresponding to the error.
8	f_{IN}	I	Prescaler input Connection with an external VCO should be done with AC coupled.
9	Clock	I	Clock input for 19-bit shift register Data is shifted into the shift register on the rising edge of the clock.
10	Data	I	Serial data input using binary code The last bit of data is a control bit. When the control bit is high, data is transmitted to the 15-bit latch. When it is low, data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input (with internal pull up resistor) When LE is high, data of the shift register is transferred to a latch, depending on a control bit in serial data.
12	FC	I	Phase switch input for phase comparator (with internal pull-up resistor) When FC is low, the characteristics of phase comparator is reversed. The FC input signal is also used to control f_{OUT} pin (test pin) output (fr or fp).
13	NC	–	No connection
14	f_{OUT}	O	Monitor pin of phase comparator input When FC is high, f_{OUT} outputs programmable reference divider output(fr). When FC is low, f_{OUT} outputs programmable divider output(fp).
15	ΦP	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input. ΦR pin is a C-MOS output.

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R \quad (A < N)$

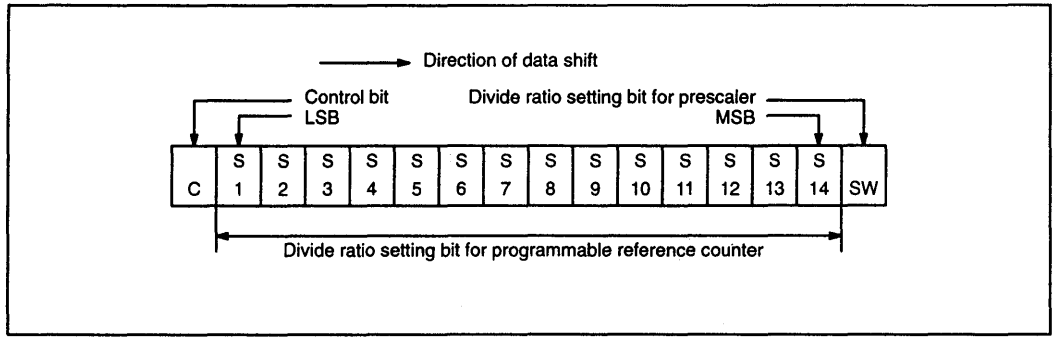
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- P : Preset divide ratio of modules prescaler (64 or 128)

Serial data input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 15-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	15 bit latch
L	18 bit latch

(a) Programmable reference divider
The programmable reference divider consists of a 16-bit shift register, a 15-bit latch and a 14-bit reference counter. The serial 16-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

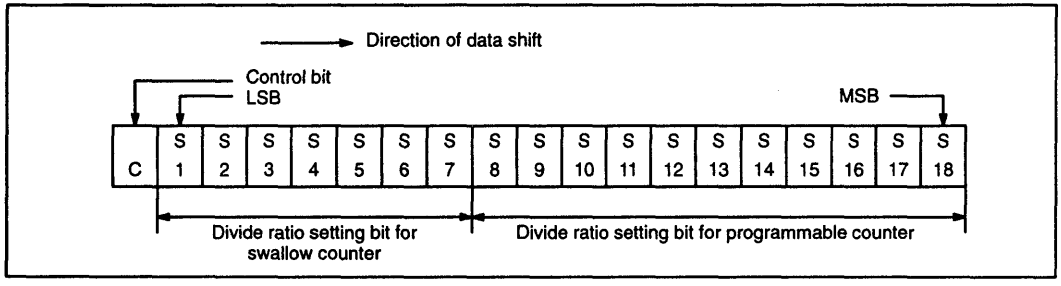
Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
   Low: 128 or 129
   High: 64 or 65
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (6 to 16,383).
4. C: Control bit: Set high.
5. Start data input with MSB first .

(b) Programmable divider divide

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

- 11-bit programmable counter divide ratio

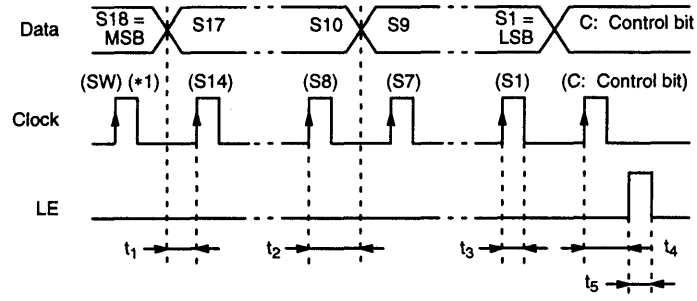
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for 11–bit programmable counter.
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18: These bits select the divide ratio of programmable counter (5 to 2,047).
4. C: Control bit: (Set low)
5. Start data input with MSB first.

Serial data input timing

- t_1 (≥ 100ns) : Data setup time t_2 (≥ 1000ns) : Data hold time t_3 (≥ 300ns) : Clock pulse width
  t_4 (≥ 100ns) : LE setup time to the rising edge of last clock t_5 (≥ 800ns) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Relation between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ΦR, ΦP) are reversed depending on the FC pin input level. Also, the monitor pin (f_{OUT}) output is controlled by the FC pin. The relationship between the FC input level and each of D_O, ΦR, and ΦP is shown below:

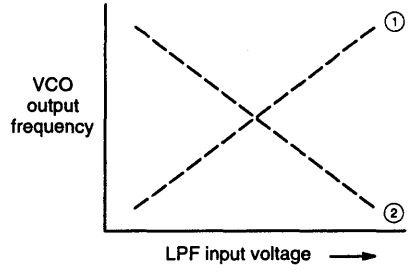
	FC = High or open				FC = Low			
	Do	ΦR	ΦP	f_{OUT}	Do	ΦR	ΦP	f_{OUT}
fr > fp	H	L	L	(fr)	L	H	Z(*1)	(fp)
fr< fp	L	H	Z(*1)	(fr)	H	L	L	(fp)
fr = fp	Z(*1)	L	Z (*1)	(fr)	Z(*1)	L	Z(*1)	(fp)

*1: High impedance

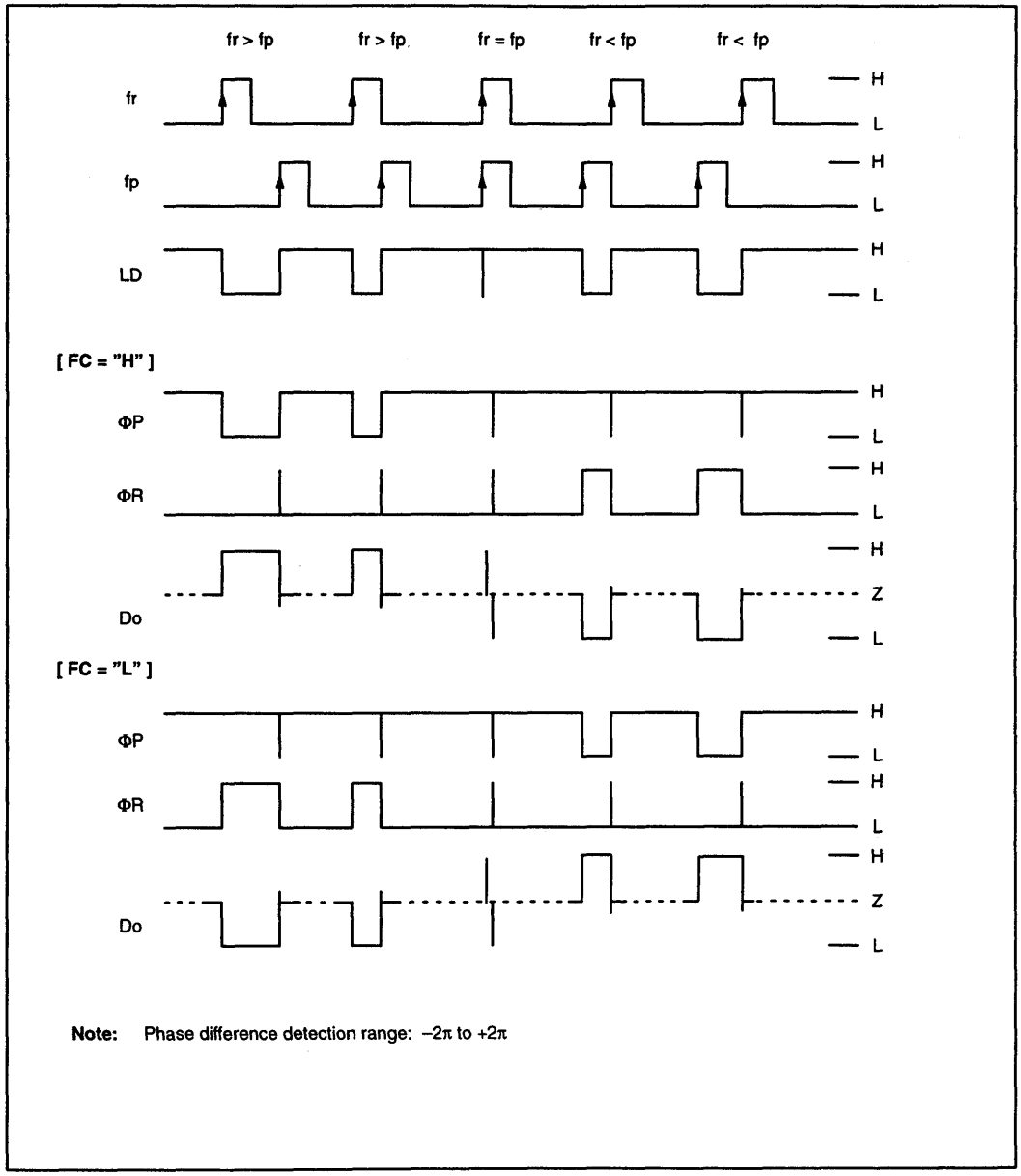
When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

*: When the LPF and VCO characteristics are similar to ①, set FC high or open.

*: When the VCO characteristics are similar to ②, set FC low.



Phase comparator output waveforms



Note: Phase difference detection range: -2π to $+2\pi$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.5	V	
	Vp	Vcc	–	6.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

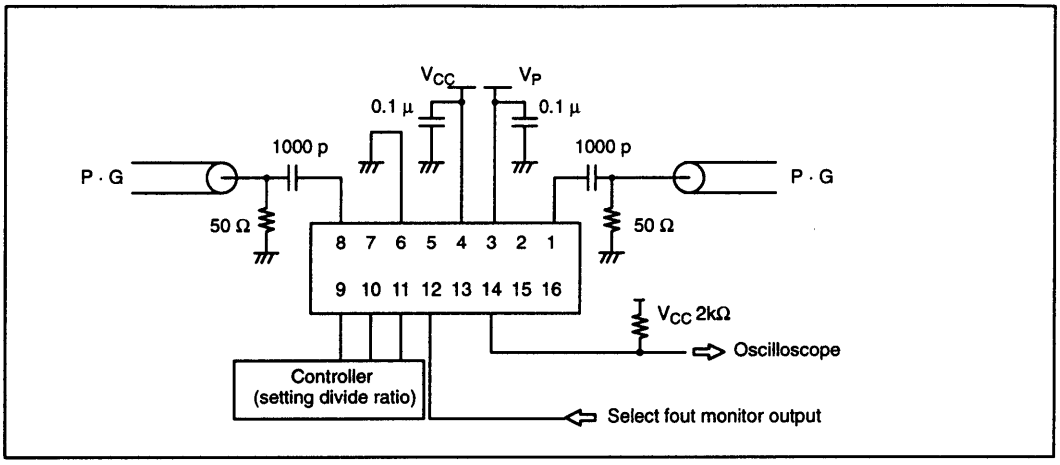
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current		I_{CC}	–	6.5	–	mA	f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Operating frequency	f_{IN}	f_{IN}	10	–	1100	MHz	AC coupling. The minimum operating frequency is measured with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	$P_{f\,IN}$	–10	–	6	dBm	50Ω
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Clock, Data, LE	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–	–	–1.0	µA	
input current	OSC_{IN}	I_{OSC}	–	±50	–	µA	
	FC, LE	I_{LE}	–	–60	–	µA	
High-level output voltage	ΦR, LD	V_{OH}	2.1	–	–	V	V_{CC} = 3 V, I_{OH} = –1.0mA
Low-level output voltage	ΦR/P, LD	V_{OL}	–	–	0.4	V	Vcc = 3V, I_{OL} = 1.0mA
High-impedance Cut off current	D_{O},, ΦP	I_{OFF}	–	–	1.1	µA	V_P = V_{CC} to 6.0V V_{OOP} = GND to 6.0 V
Output current	ΦR, LD	I_{OH}	–1.0	–	–	mA	Vcc = 3V
	ΦR/P, LD	I_{OL}	–	–	1.0	mA	Vcc = 3V

TEST CIRCUIT
(FOR MEASURING INPUT SENSITIVITY fin/OSCin)



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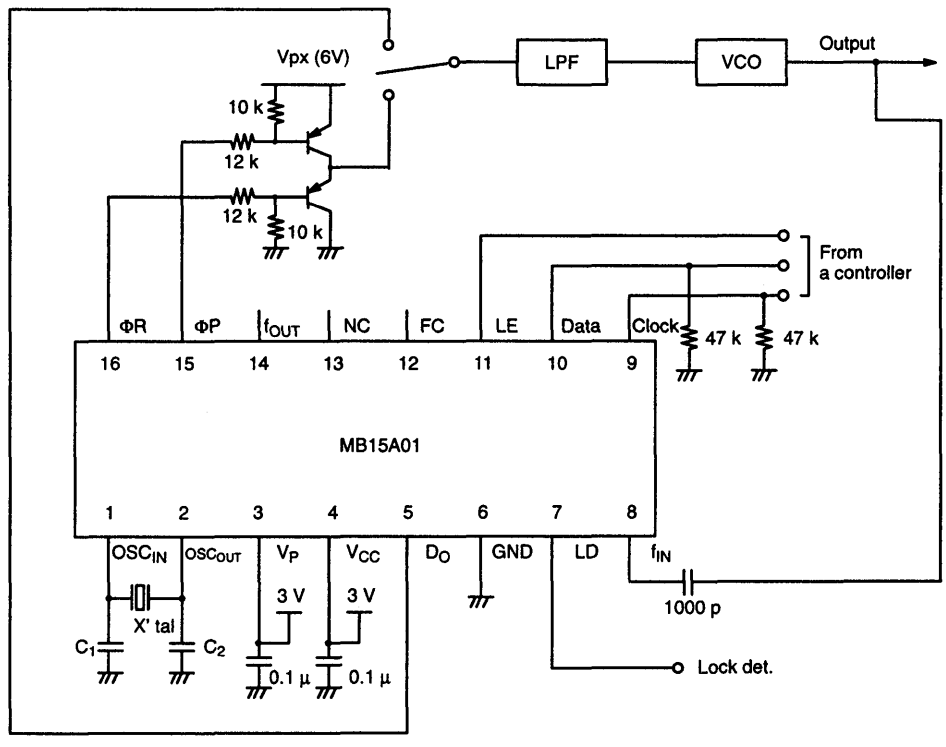
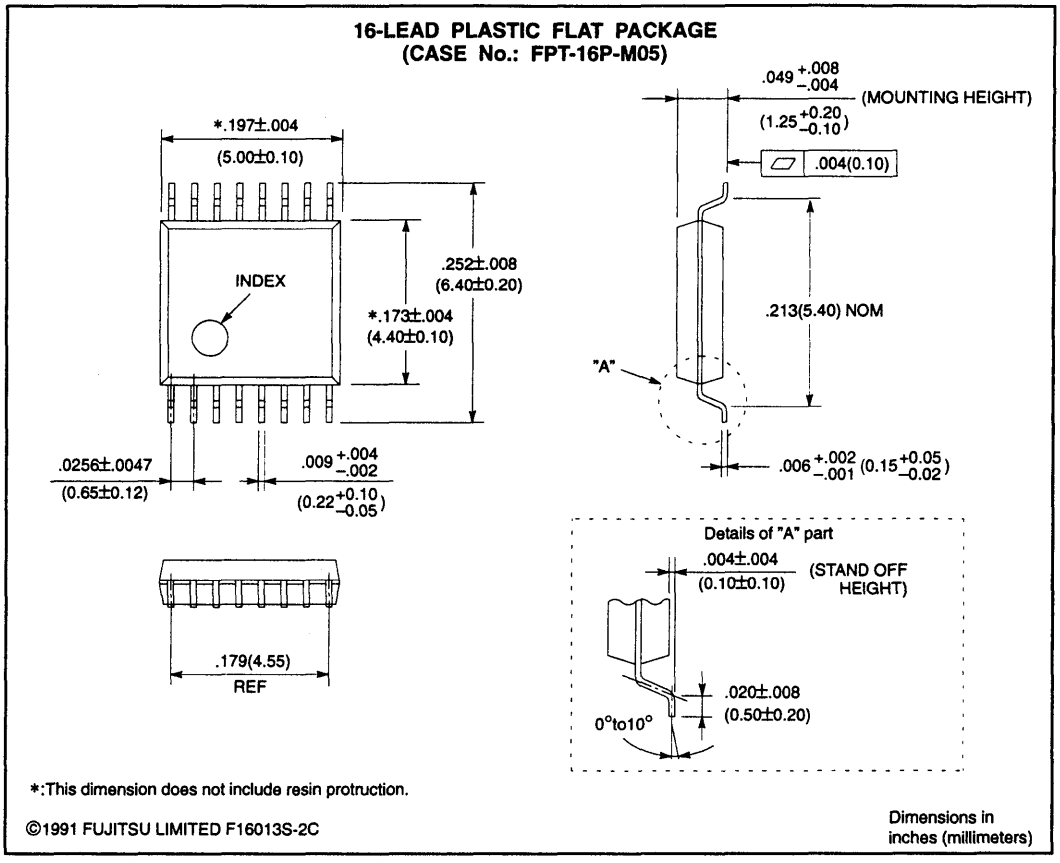
APPLICATION EXAMPLE



V_{PX}	:	Maximum 6 V
V_P	:	When the internal charge pump is not used, please connect to V_{CC}.
C_1, C_2	:	Depend on the crystal parameters
LE, FC	:	With internal pull-up resistor
ΦP, fout	:	N-ch open drain output
ΦR	:	C-MOS output

PACKAGE DIMENSION



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

4

DS04-21322-1aE

FUJITSU

DATA SHEET

MB15B01 ASSP

DUAL INPUT PLL FREQUENCY SYNTHESIZER

4

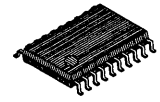
DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

The Fujitsu MB15B01 is a 1.1 GHz dual serial input PLL (Phase Locked Loop) frequency synthesizer designed for cellular phones, cordless phones and other radio applications.

The MB15B01 has two PLL circuits on a single chip: PLL1 and PLL2. An analog switch is provided for each PLL circuit to decrease lock up time. Separate power supply pins are provided for each PLL circuit.

Two 1.1 GHz dual modulus prescalers are included inside and enables a pulse swallow function.

It operates with a supply voltage of 3.0V typ. and dissipates 13 mA typ. of current realized through the use of Fujitsu's unique Bi-CMOS technology.

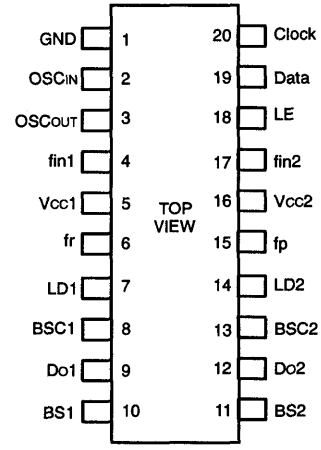


PLASTIC FLAT PACKAGE
FPT-20P-M03

FEATURES

- High operating frequency: fin = 1.1 GHz (Pin = –10 dBm, Vcc = 3V)
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 8 to 16,383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 16 to 2,047
  Each programmable counter can be controlled independently.
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- Low power supply current: I_{CC} (total) = 13 mA typ. (Vcc = 3V)
- Power saving function : $I_{CC1} = I_{CC2}$ = 100 µA typ (Vcc = 3V)
- On-chip analog switches achieve fast lock up time
- Digital lock detector
- Wide operating temperature: Ta = –30 to 80°C
- Plastic 20-pin SSOP package

PIN ASSIGNMENT



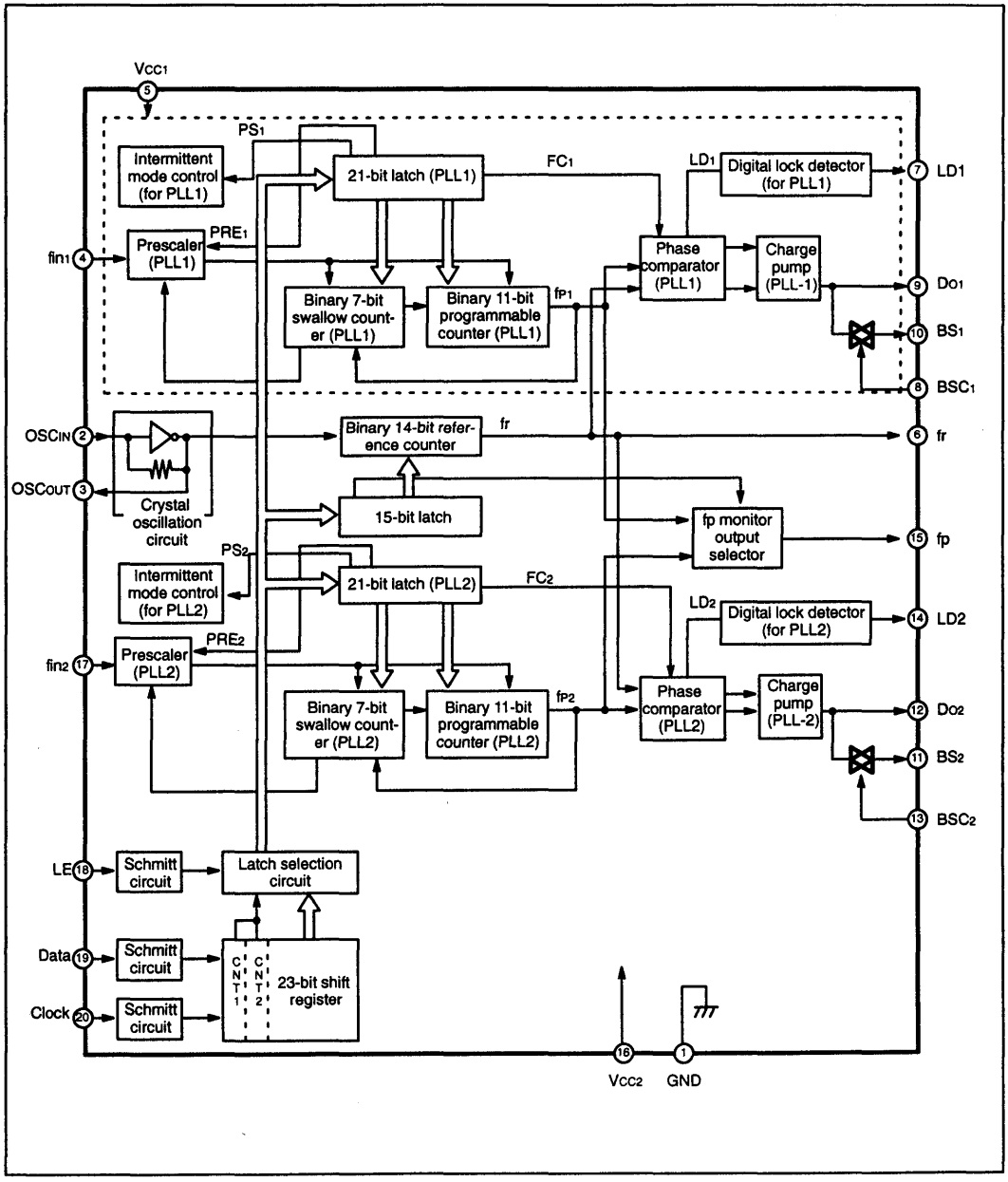
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Remark	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to 5.0	V
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5	V
Open Drain Voltage	V_{OOP}	fr, fp	–0.5 to + 5.0	V
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSCIN
OSCOUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSCIN pin and OSCOUT pin.</td></tr>
<tr><td>4</td><td>fin1</td><td>I</td><td>Prescaler input pin of PLL1 section.
The connection with VCO should be AC.</td></tr>
<tr><td>5</td><td>Vcc1</td><td>–</td><td>Power supply voltage input pin of PLL1 section.
When power is OFF, latched data of PLL1 section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output. (Open drain output)</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of PLL1 section.
<table>
<tr><th>Status</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>BSC1</td><td>I</td><td>Analog switch control pin of PLL1 section.
<table>
<tr><th>BSC1</th><th>BS1 pin output</th></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>9</td><td>Do1</td><td>O</td><td>Charge pump output pin of PLL1 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of PLL1 section, and controlled by BSC1.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of PLL2 section, and controlled by BSC2.</td></tr>
<tr><td>12</td><td>Do2</td><td>O</td><td>Charge pump output pin of PLL2 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>BSC2</td><td>I</td><td>Analog switch control pin of PLL2 section.
<table>
<tr><th>BSC2</th><th>BS2 pin output</th></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detection signal output pin of PLL2 section.
<table>
<tr><th>Status</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output. (Open drain output)
This pin outputs divided frequency of PLL1 section or PLL2 section depending upon FP bit setting.
<table>
<tr><th>FP bit</th><th>Output</th></tr>
<tr><td>H</td><td>PLL1 section (fp1)</td></tr>
<tr><td>L</td><td>PLL2 section (fp2)</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	Vcc2	–	Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of PLL2 section and reference counter is cancelled.
17	fin2	I	Prescaler input pin of PLL2 section. The connection with VCO should be AC.
18	LE	I	Load enable input pin. This pin is followed by a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data.
19	Data	I	Serial data input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. The stored data in the shift register is transferred to one of PLL1 programmable counter, PLL2 programmable counter and programmable reference counter depending upon control data settings.
20	Clock	I	Clock input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. On rising edge of the clock, one bit of data is transferred into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$fvco = \{(P \times N) + A\} \times fosc + R \quad (A < N)$

fvco: Output frequency of external voltage controlled ocillator (VCO)

P: Preset divide ratio of dual modulus prescaler (64 or 128)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

fosc: Reference oscillation frequency

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable counters of PLL1 section and PLL2 section, and programmable reference counter are controlled individually.
Serial data of binary data is entered via Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Control bits		Destination of serial data
CN1	CN2	
L	L	Reference counter
L	H	Programmable counter of PLL1
H	H	Programmable counter of PLL2

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CN1	CN2	FP	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

R1 to R14 : Divide ratio setting bit for the programmable counter (8 to 16,383)
FP : Test purpose bit (monitor output fp1/fp2 selection)
CN1, 2 : Control bit

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	PS	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio setting bit for the programmable counter (16 to 2,047)
A1 to A7 : Divide ratio setting bit for the swallow counter (0 to 127)
FC : Phase control bit for the phase detector
PRE : Divide ratio setting bit for the prescaler (64/65, 128/129)
PS : Power saving control bit
CN1, 2 : Control bit

BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 8 is prohibited.
• Divide ratio (R) range = 8 to 16383

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 16 is prohibited.
• Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

PRESCALER DATA SETTING

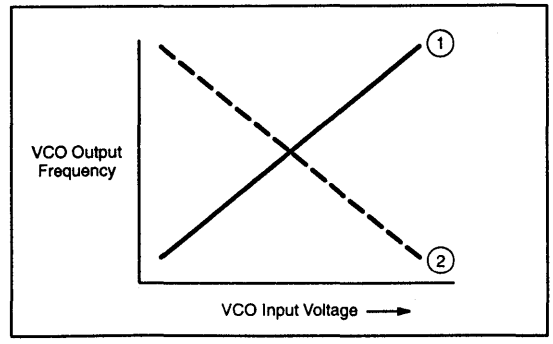
Divide Ratio	PRE
64/65	1
128/129	0

Note: • Divide ratio for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.

PHASE COMPARATOR PHASE CONTROL DATA SETTING

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: • Z = High-impedance
• Depending upon the VCO polarity, FC bit should be set.
• Phase characteristic for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.



POWER SAVING FUNCTION CONTROL (INTERMITTENT OPERATION)

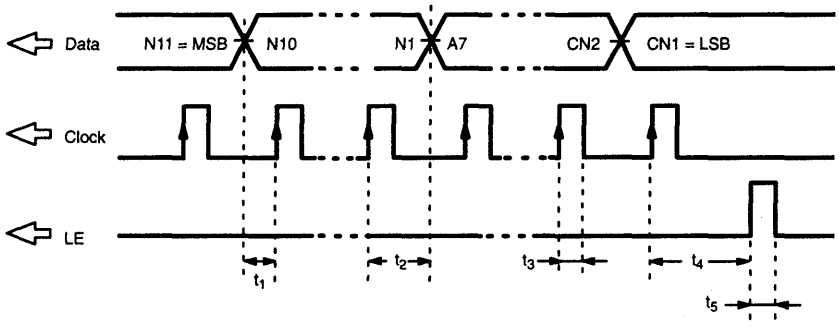
	PS	
	H	L
PLL1's section	ON	OFF
PLL2's section and common section	ON	OFF

Note: • Power saving mode for each PLL1 and PLL2 is selected by the serial data at that time of divide ratio setting for each programmable divider.
• Common section ; Crystal oscillator circuit, reference counter
• Just after powering up, please set PS bit to "L" at first.

Intermittent operation limits power consumption by shutting down or start the internal circuits case by case. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost. To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting phase of both frequencies to limit the error signal output.

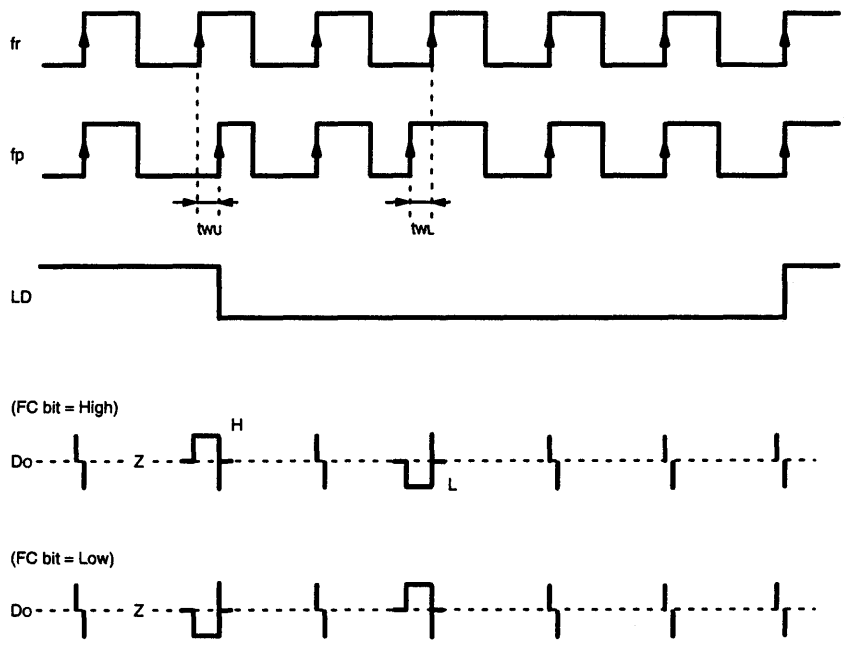
SERIAL DATA INPUT TIMING

t1 (>100ns) : Data set up time t2 (>1000ns) : Data hold time t3 (>300ns) : Clock pulse width
t4 (>100ns) : LE set up time to the rising edge of the last clock t5 (>800ns) : LE pulse width



On rising edge of the clock, one bit of the data is transferred into the shift register.

PHASE DETECTOR OUTPUT WAVEFORM



Note:
- Phase error detection range = -2π to $+2\pi$
- LD output becomes low when phase error is twu or more.
- LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
- twL and twL depend on OSCin input frequency.
  twu $\geq$8/fosc (e. g. twu $\geq$625ns, foscin = 12.8 MHz)
  twL $\leq$16/fosc (e. g. twL $\leq$1250ns, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	Vcc	2.7	3.0	3.5	V	Vcc1 = Vcc2
Input Voltage	VIN	GND	–	Vcc	V	
Operating Temperature	Ta	–30	–	+80	°C	

HANDLING PRECAUTIONS

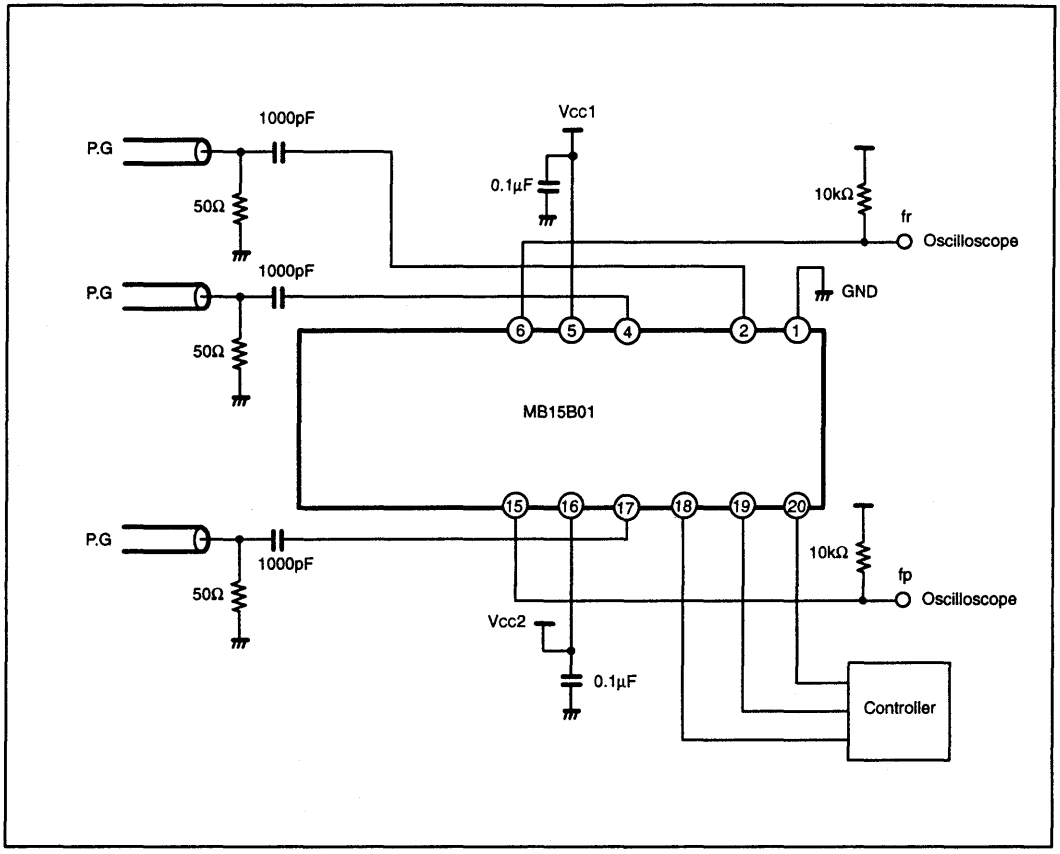
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

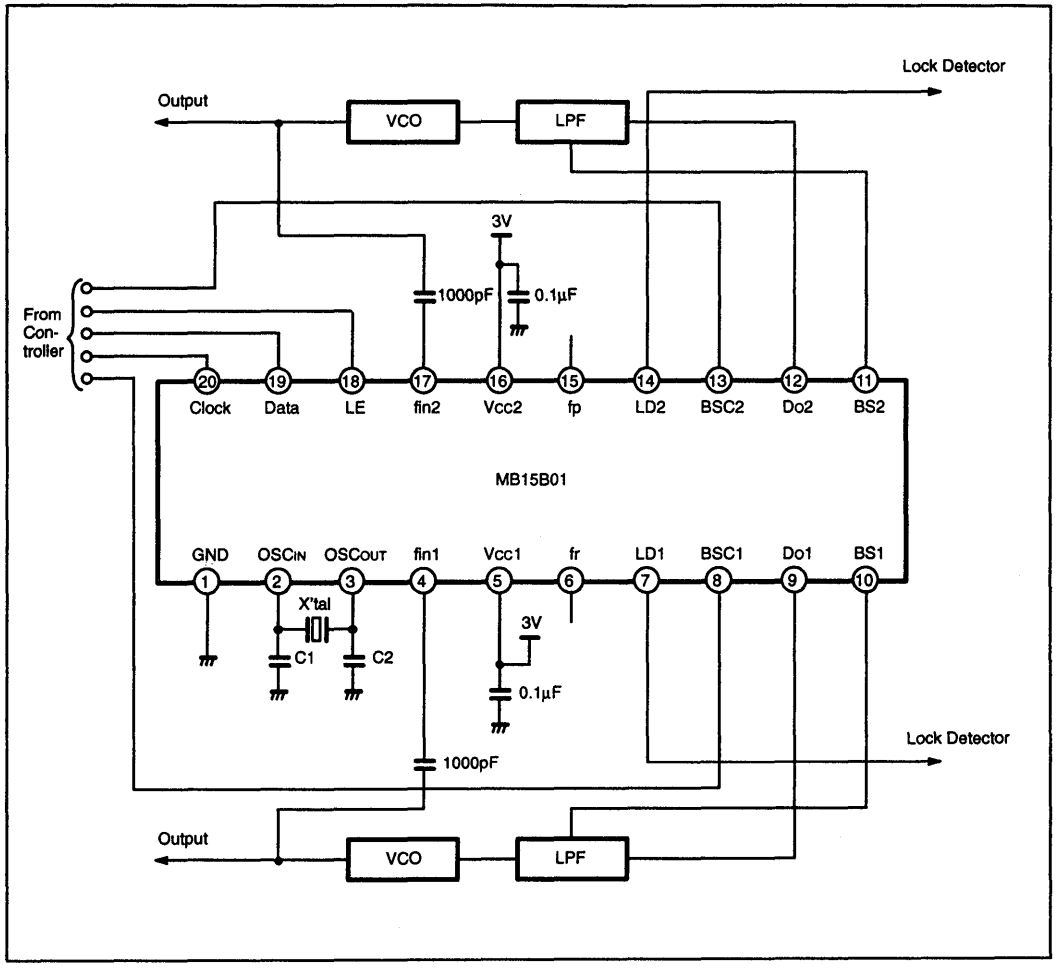
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC1}	PLL1 section	–	6.0 (0.1)*1	–	mA
		I_{CC2}	PLL2 & common sections	–	7.0 (0.1)*1	–	
Operating Frequency	fin	fin		100	–	1100	MHz
	OSC_{IN}	fosc		–	12.8	20.0	
Input Sensitivity	fin	Pfin	50Ω	–10	–	0	dBm
	OSC_{IN}	Vosc		0.5	–	–	Vp-p
High-level Input Voltage	Data, Clock LE, BSC	V_{IH}		Vccx0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	Vccx0.3–0.4	
High-level Input Current	Data, Clock LE, BSC	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	Iosc		–	±50	–	
High-level Output Voltage	LD	V_{OH}	Vcc = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}	Vcc = 3.0V	–	–	0.4	
High-impedance Cutoff Current	Do, BS	I_{OFF}		–	–	1.1	µA
Output Current	LD	I_{OH}		–1.0	–	–	mA
		I_{OL}		–	–	1.0	
	Do1, 2	I_{OH}	Vcc = 3.0V	–	–2.5	–	mA
		I_{OL}	Vcc = 3.0V	–	5.0	–	
Analog Switch ON Resistance		Ron		–	50	–	Ω

*1 : The value in ( ) is power supply current in power saving mode.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)

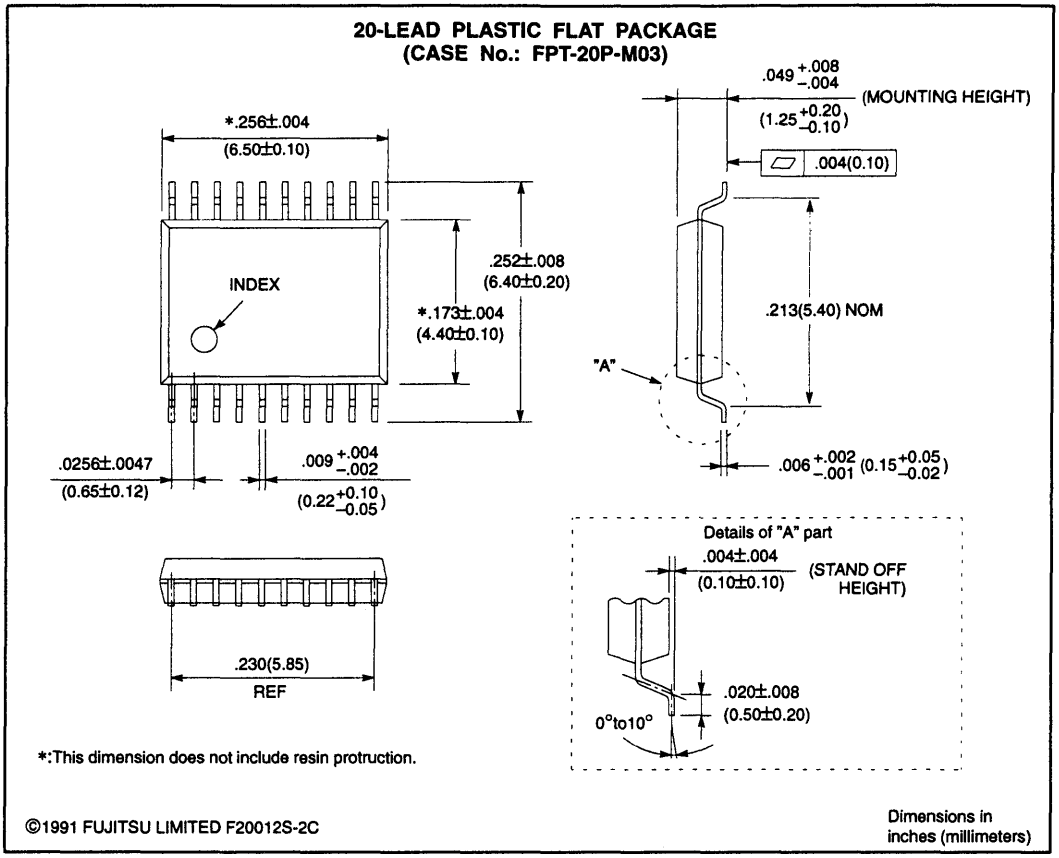


APPLICATION EXAMPLE



Note: C1, C2 : depends on a crystal oscillator.
Clock, Data, LE : involves a schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent oscillation.

PACKAGE DIMENSION



September 1995
Edition 6.0a

FUJITSU

DATA SHEET

MB1501/MB1501H/MB1501L

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

The Fujitsu MB1501/MB1501H/MB1501L, utilizing BI-CMOS technology, is a single chip serial input PLL frequency synthesizer with pulse-swallow function.

The MB1501 series contain a 1.1GHz two modulus prescaler that can select either 64/65 or 128/129 divide ratio; control signal generator; 16-bit shift register; 15-bit latch; programmable reference divider (binary 14-bit programmable reference counter); 1-bit switch counter; phase comparator with phase inverse function; charge pump; crystal oscillator; 19-bit shift register; 18-bit latch; programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).

The MB1501 operates on a low supply voltage (3V typ) and consumes low power (45mW at 1.1GHz).

MB1501 Product Line

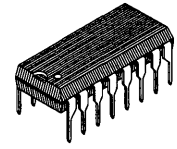
	V_P Voltage	V_{OOP} Voltage	Lock up time	D_O Output Width	High-level Output Current	Low-level Output Current
MB1501	8V max	8.5V max	Middle speed	Middle	Middle	Middle
MB1501H	10V max	10.0V max	High speed	Low	High	Low
MB1501L	8V max	8.5V max	Low speed	High	Low	High

- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($P_{IN\ MIN}$=0.20V_{P-P})
- On-chip prescaler
- Low power supply voltage: 2.7V to 5.5V (3.0V typ)
- Low power supply consumption: 45mW (3.0V, 1.1GHz operation)
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  - Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter (Divide ratio: 8 to 16383)
  - 1-bit switch counter (SW) Sets divide ratio of prescaler
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: T_A=–40°C to +85°C

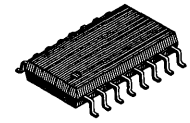
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to +7.0	V
	V_{PH}	MB1501H	V_{CC} to 12.0	V
	V_P,V_{PL}	MB1501/1501L	V_{CC} to 10.0	
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5	V
Open-drain Output	V_{OOPH}	MB1501H	–0.5 to 11.0	V
	V_{OOP},V_{OOPL}	MB1501/1501L	–0.5 to 9.0	
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

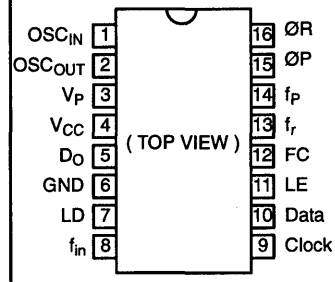


PLASTIC PACKAGE
DIP-16P-M04



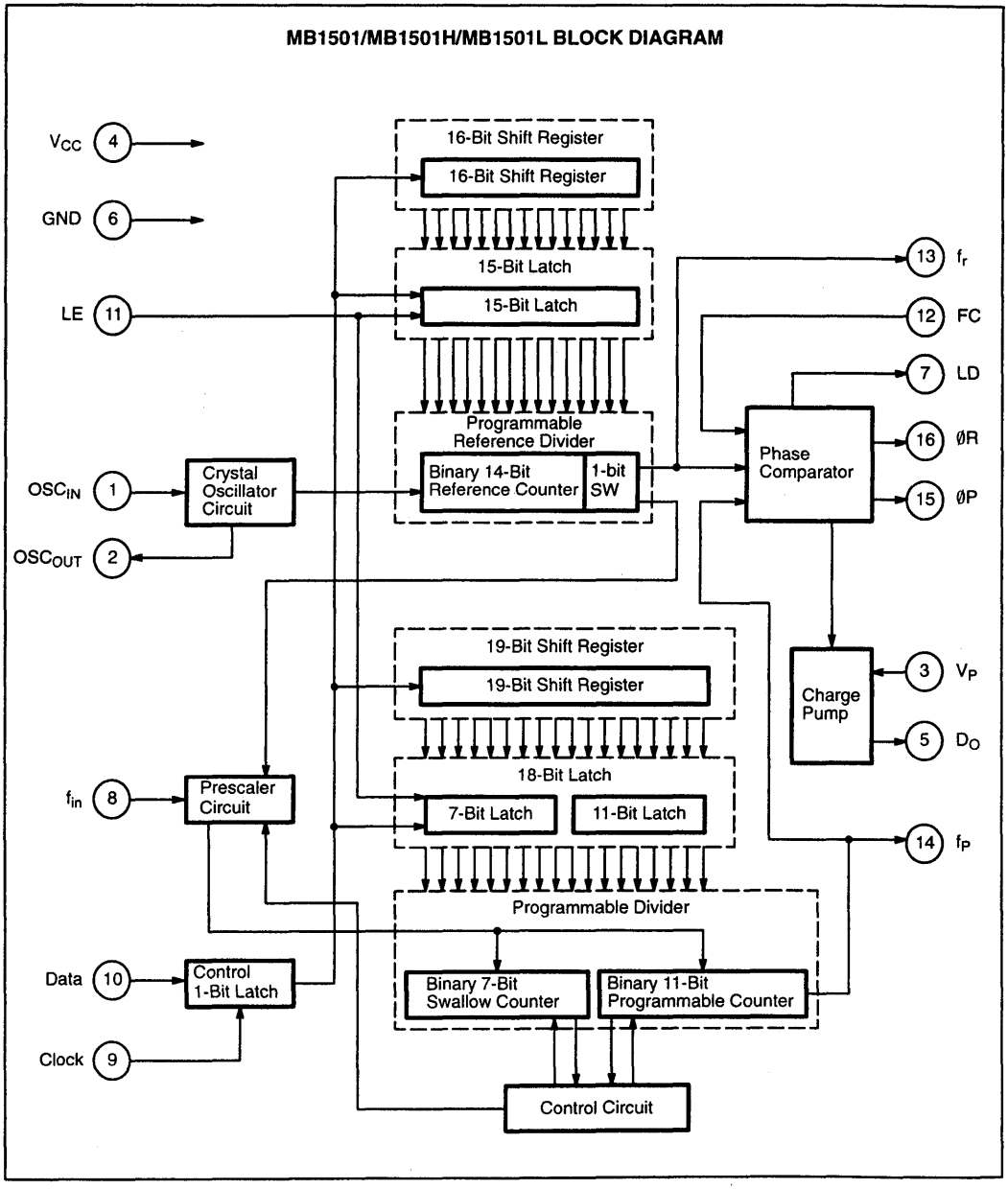
PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1501/MB1501H/MB1501L BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump.
4	V_{CC}	—	Power supply voltage input.
5	D_O	O	Charge pump output. Phase characteristic can be inversed depending upon FC input.
6	GND	—	Ground.
7	LD	O	Phase comparator output. This pin outputs high when the phase is locked. While the phase difference of f_r and f_p exists, the output level goes low.
8	f_{in}	I	Prescaler input. The connection with an external VCO should be an AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Serial data of binary code input. The last bit of the data is a control bit. The last data bit specifies which latch is activated. When the last bit is high level and LE is high-level, data is transferred to 15-bit latch. When the last bit is low level and LE is high level, data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high level (or open), data stored in the shift register is transferred to latch depending on the control data.
12	FC	O	Phase selecting input of phase comparator (with internal pull up resistor). When FC is low level, charge pump and phase detector characteristics can be inversed.
13	f_r	O	Monitor pin of phase comparator input. It is the same as programmable reference divider output.
14	f_P	O	Monitor pin of phase comparator input. It is the same as programmable divider output.
15 16	ØP ØR	O O	Outputs for external charge pump. Phase characteristics can be inversed depending on FC input. ØP pin is an N-channel open-drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is input using Data pin, Clock pin and LE pin, The 15-bit programmable reference divider and 18-bit programmable divider are controlled respectively.

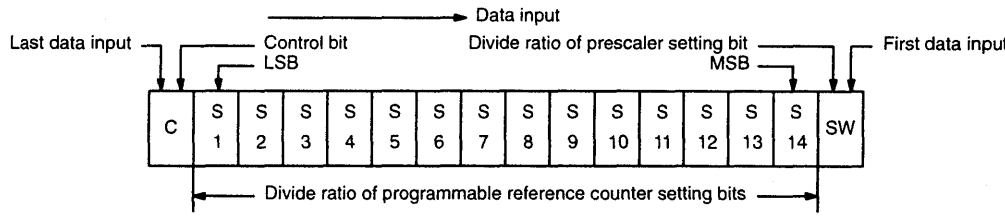
On rising edge of the clock shifts one bit of the data into the internal shift registers.

When load enable (LE) is high level (or open), data stored in shift resisters is transferred to 15-bit latch or 18-bit latch depending upon the control bit level.

Control data "H" ; Data is transferred into 15-bit latch.
Control data "L" ; Data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



◎ 14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

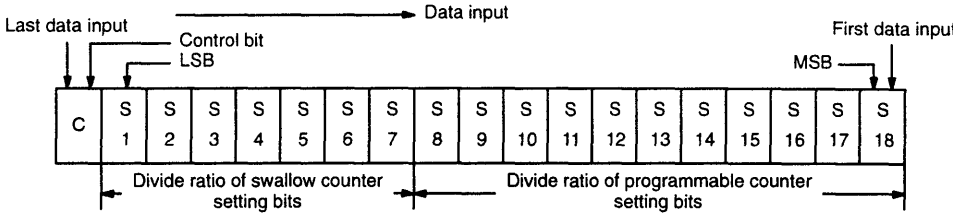
Divide ratio less than 8 is prohibited.
Divide ratio R: 8 to 16383

SW: Divide ratio of prescaler setting bit.
SW="H" : 64
SW="L" : 128
S_1 to S_{14}: Divide ratio of programmable reference counter setting bits (8 to 16383)
C: Control bit (Control bit is set to high.)

FUNCTIONAL DESCRIPTIONS

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown below.



◎ 7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Divide ratio A : 0 to 127

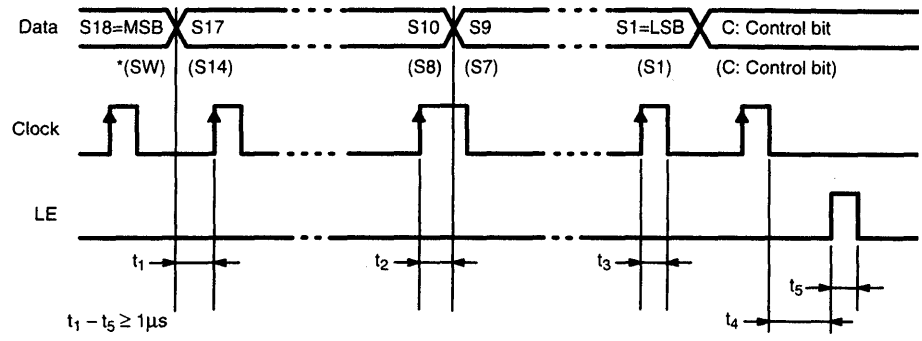
◎ 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Divide ratio less than 16 is prohibited.
Divide ratio N : 16 to 2047

S_8 to S_{18} :Divide ratio of programmable counter setting bits (16 to 2047)
S_1 to S_7 : Divide ratio of swallow counter setting bits (0 to 127)
C: Control bit (Control bit is set to low.)
Dara is input from MSB data.

SERIAL DATA INPUT TIMING



On the rising edge of the clock shifts one bit of the data into the shift registers.
Parenthsis data is used for setting the divide ratio of the programmable reference divider.

PHASE CHARACTERISTICS

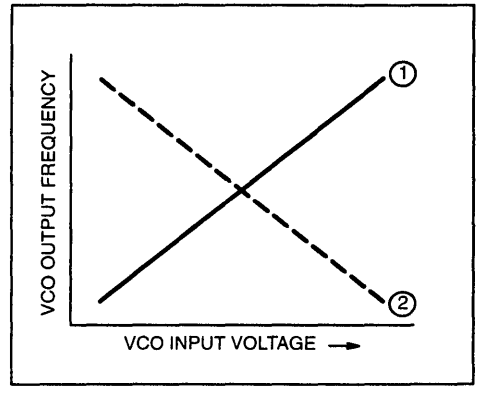
FC pin (pin 12) is provided to inverse the phase comparator characteristics. The characteristics of internal charge pump output (D_O), phase detector outputs (ØR, ØP) can be inversed depending upon FC input data. Outputs are shown below.

	FC=H (or open)			FC=L		
	D_O	ØR	ØP	D_O	ØR	ØP
$f_r > f_p$	H	L	L	L	H	Z
$f_r < f_p$	L	H	Z	H	L	L
$f_r = f_p$	Z	L	Z	Z	L	Z

Note: Z=(High impedance)

Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set high or open circuit;
When VCO characteristics are like ②, FC should be set Low.

VCO CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}		2.7	3.0	5.5	V
	V_{PH}	MB1501H	V_{CC}		10.0	V
	V_P, V_{PL}	MB1501 MB1501L	V_{CC}		8.5	
Open-drain Output	V_{OOPH}	MB1501H	V_{CC}		10.0	V
	V_{OOP}, V_{OOPL}	MB1501 MB1501L	V_{CC}		8.5	
Input Voltage	V_{IN}		GND		V_{CC}	V
Operating temperature	T_A		–40		+85	°C

4

ELECTRICAL CHARACTERISTICS

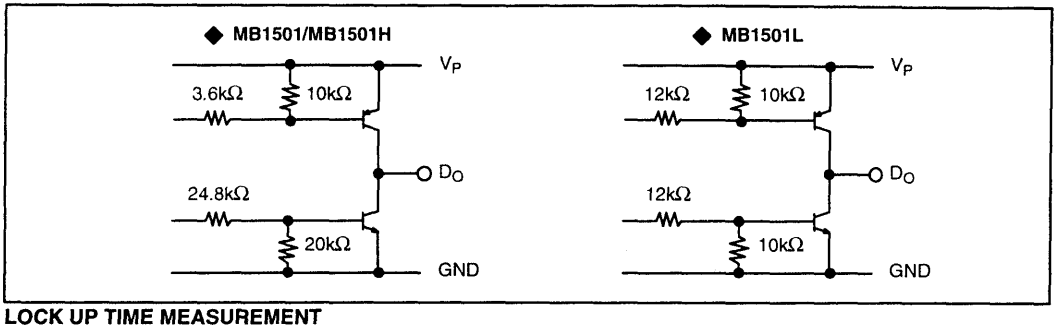
(V_{CC}=2.7 to 5.5V, T_A=−40 to +85°C)

Parameter	Pin Name	Symbol	Condition		Value Min	Value Typ	Value Max	Unit
Power Supply Current	V_{CC}	I_{CC}	*1		—	15	—	mA
Operating Frequency	f_{in}	f_{IN}	*2		10	—	1100	MHz
	OSC_{IN}	f_{OSC}			—	12	20	MHz
Input Sensitivity	f_{in}	P_{fin1}	V_{CC}=2.7 to 4.0V		−10	—	6	dBm
		P_{fin2}	V_{CC}=4.0 to 5.5V		−4	—	6	dBm
	OSC_{IN}	V_{IN}			0.5	—	—	V_{P-P}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}			0.7xV_{CC}	—	—	V
Low-level Input Voltage		V_{IL}			—	—	0.3xV_{CC}	V
High-level Input Current	Data, Clock	I_{IH}			—	1.0	—	µA
Low-level Input Current		I_{IL}			—	−1.0	—	µA
Input Current	OSC_{IN}	I_{IN}			—	±50	—	µA
	LE, FC	I_{LE}			—	−60	—	µA
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=3.0V		2.4	—	—	V
Low-level Output Voltage		V_{OL}			—	—	0.4	V
N-channel Open-drain Cutoff Current	ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$		—	—	1.1	µA
High-level Output Current	Except D_O and OSC_{OUT}	I_{OH}			−1.0	—	—	mA
Low-level Output Current		I_{OL}			1.0	—	—	mA
High-level Output Current	D_O	I_{DOHH}	MB1501H	V_{CC}=3V V_P=12V, T_A=25°C	−2.2	−4.5	—	mA
		I_{DOH}	MB1501	V_{CC}=3V V_P=6V, T_A=25°C	−0.5	−2.0	—	mA
		I_{DOHL}	MB1501L		−0.5	−1.1	−2.2	mA
Low-level Output Current		I_{DOLH}	MB1501H	V_{CC}=3V V_P=12V, T_A=25°C	2.2	6.0	—	mA
		I_{DOL}	MB1501	V_{CC}=3V V_P=6V, T_A=25°C	1.5	6.0	—	mA
		I_{DOLL}	MB1501L		4.5	12.0	—	mA
Leakage Current	D_O, ØP	I_{DOZ}	MB1501H	V_{CC}=3V, V_P=12V T_A=25°C	—		1.0	µA
			MB1501 MB1501L	V_{CC}=3V, V_P=9V T_A=25°C				

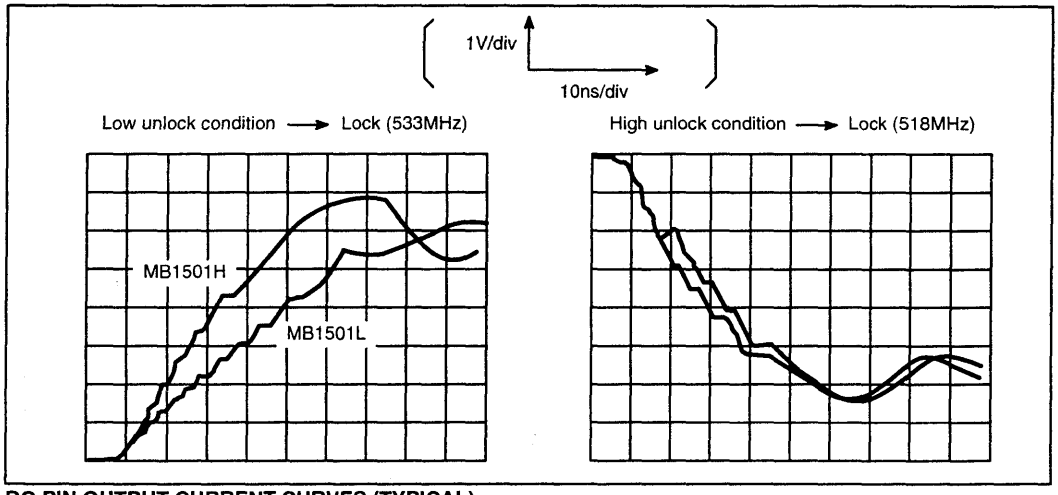
Note: *1 V_{CC}=3.0V, f_{IN}=1.1GHz, f_{OSC}=12MHz crystal.
Inputs are grounded except f_{IN}, and outputs are open.
*2 Input coupling capacitor 1000pF is connected.

TYPICAL CHARACTERISTICS CURVES

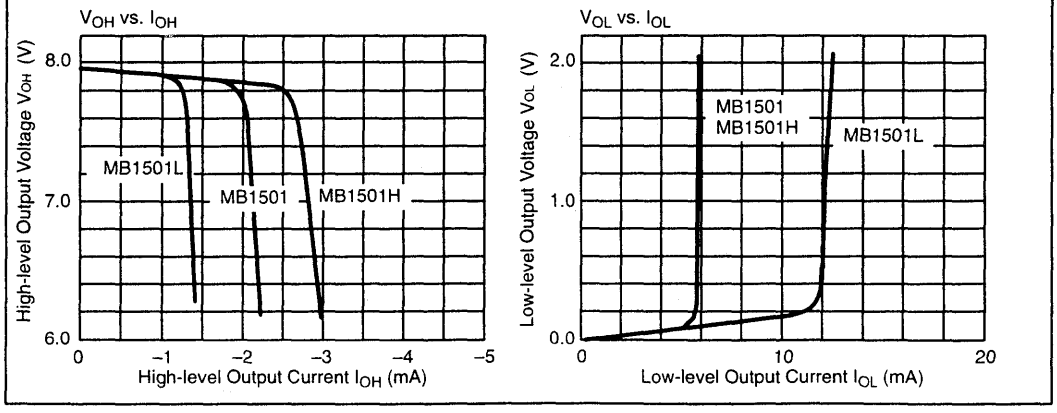
CHARGE PUMP CHARACTERISTICS



LOCK UP TIME MEASUREMENT

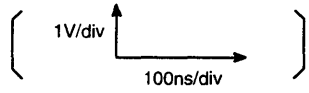


DO PIN OUTPUT CURRENT CURVES (TYPICAL)

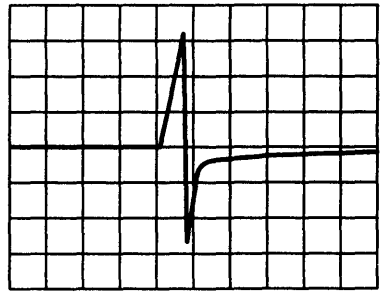


D_O PIN OUTPUT WAVEFORM AT LOCK CONDITION

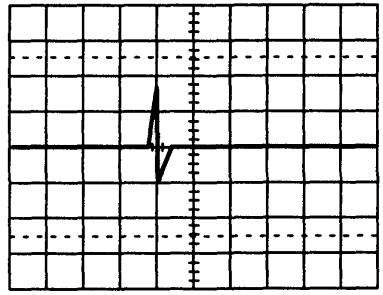
Output Waveform



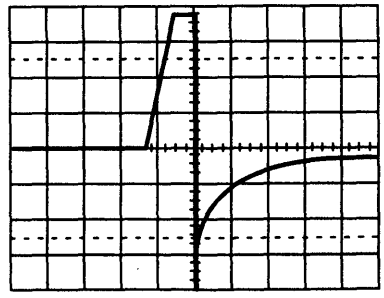
MB1501



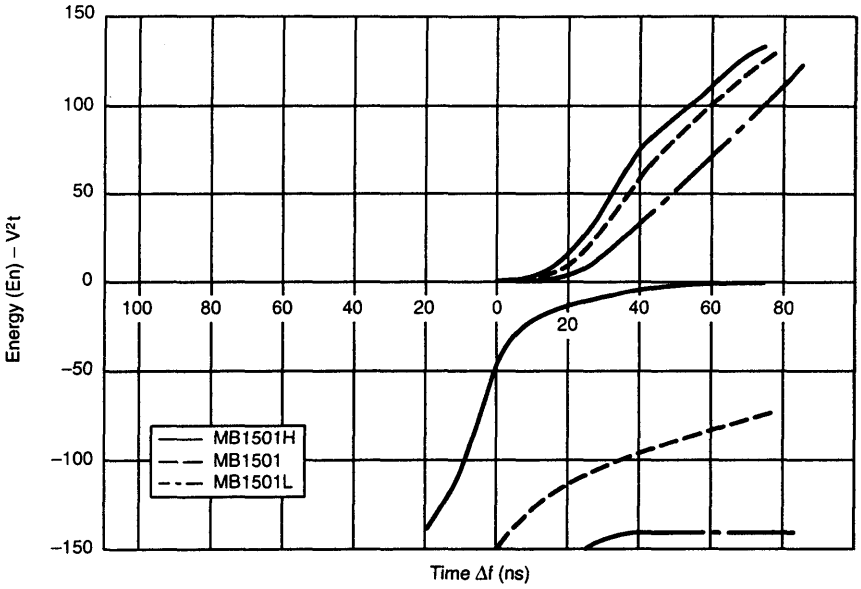
MB1501H

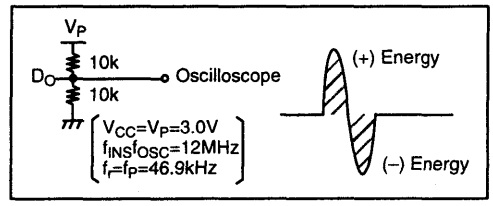


MB1501L



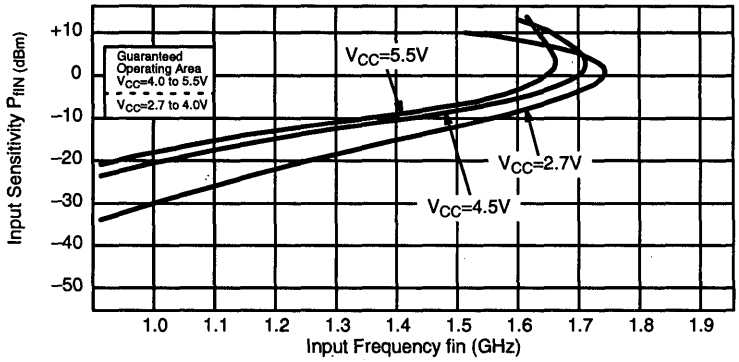
PHASE CHARACTERISTICS (Δf vs. D_O OUTPUT ENERGY)

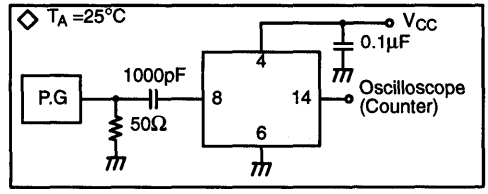




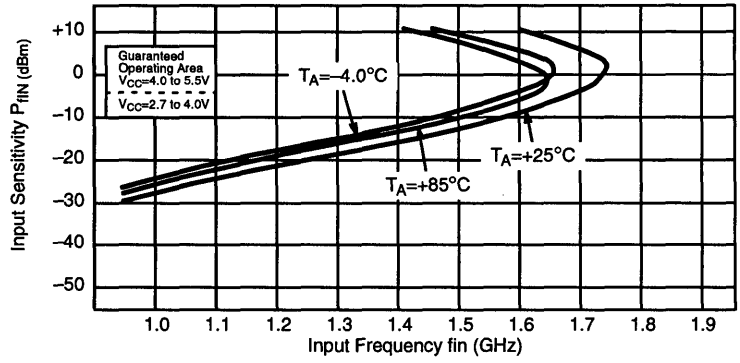
INPUT SENSITIVITY

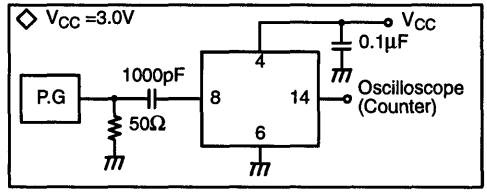
Input Sensitivity vs. Input Frequency (Supply Voltage Dependence)



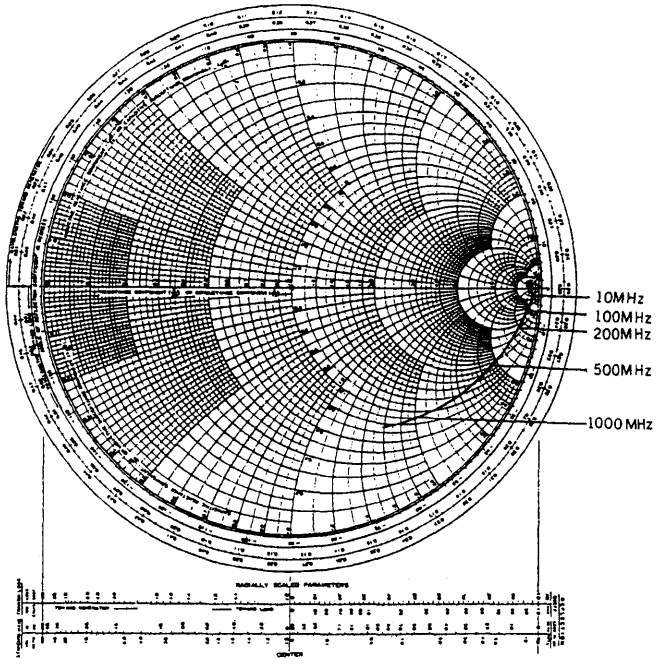


Input Sensitivity vs. Input Frequency (Temperature Dependence)



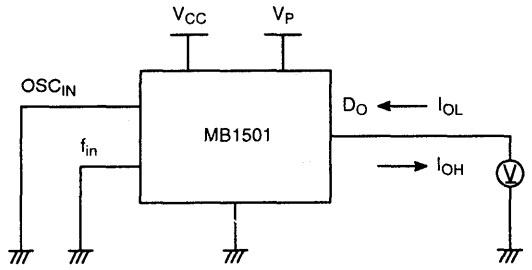


INPUT IMPEDANCE

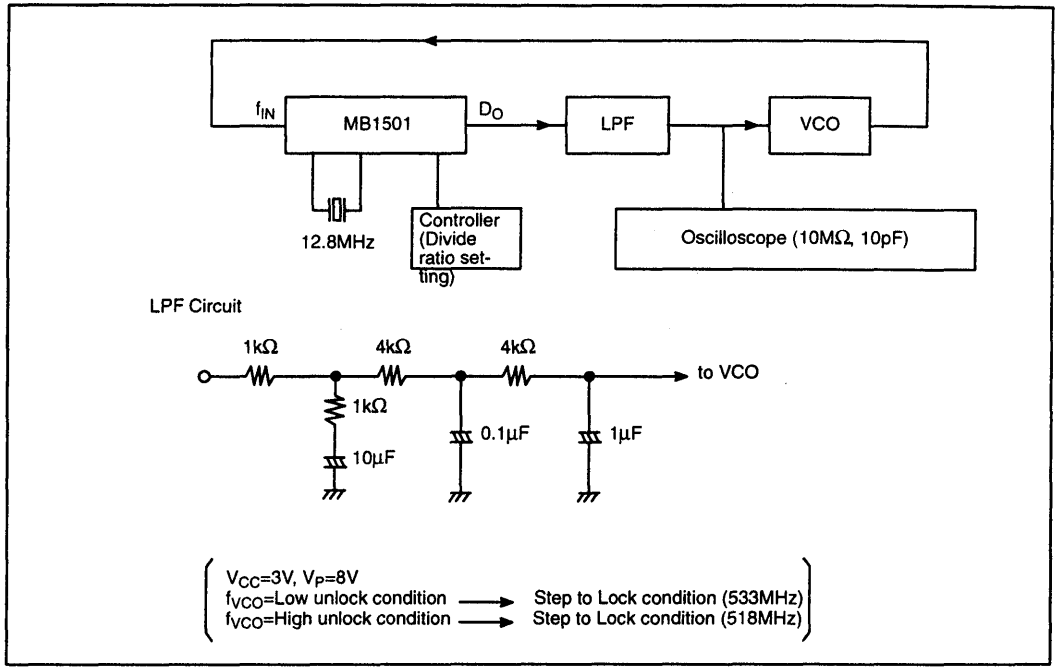


TEST CIRCUIT

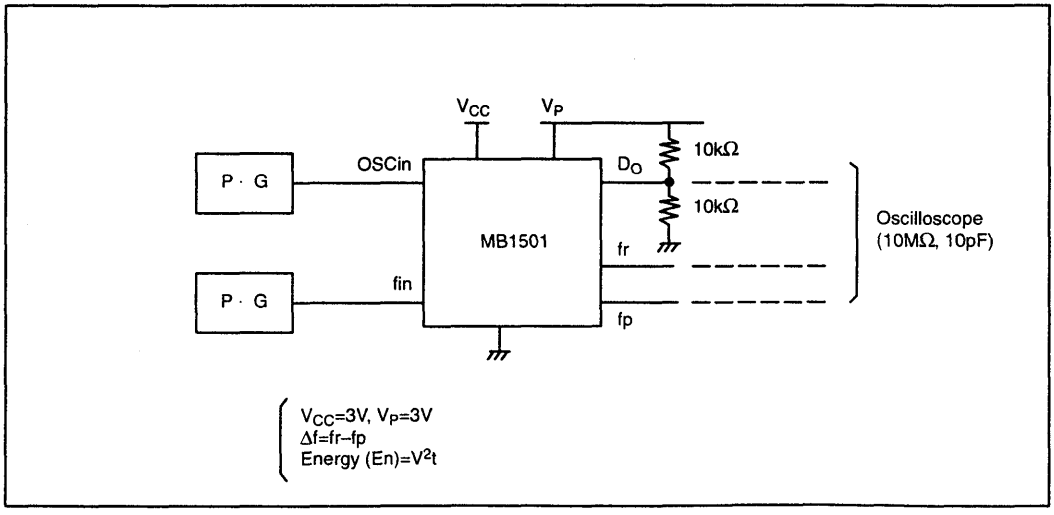
D_O Pin Output Current (I_{OH}, I_{OL}) Measurement



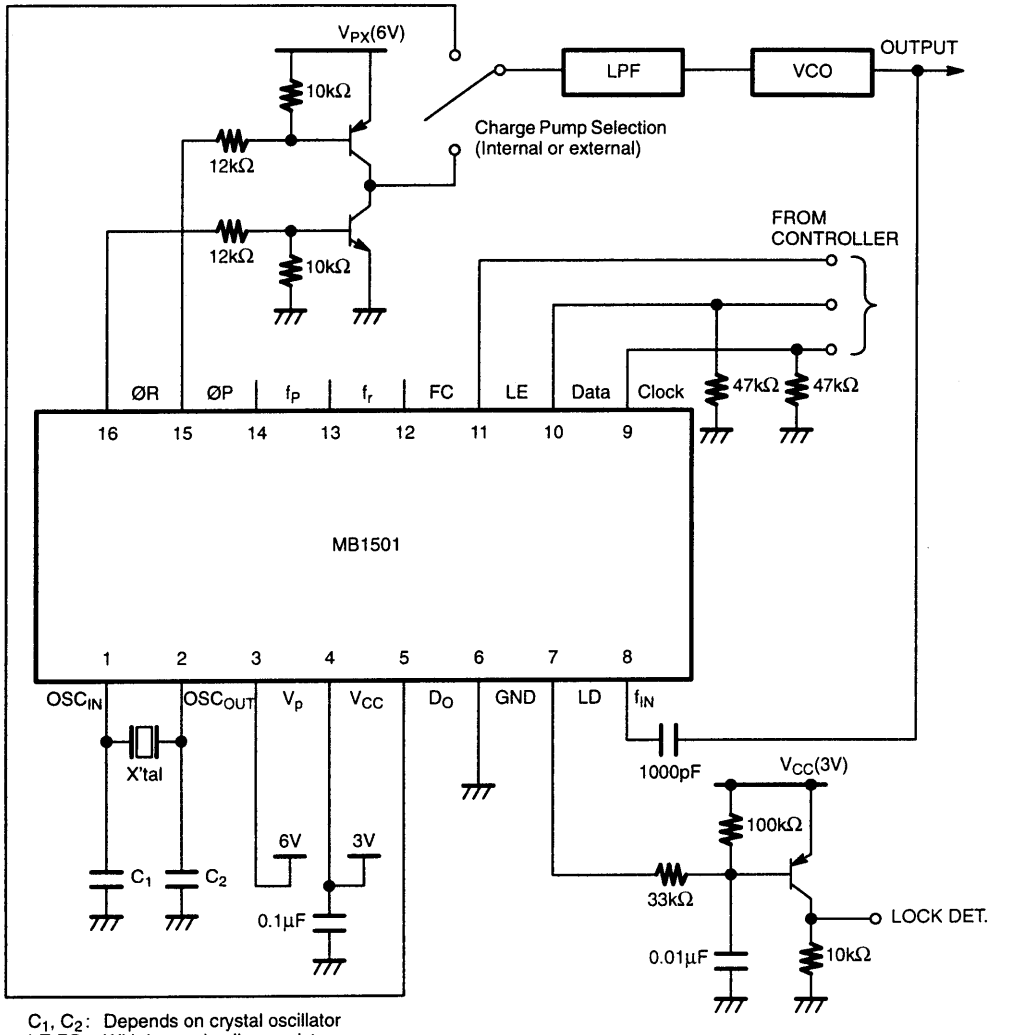
Lock up Time Measurement



Phase Characteristics Measurement



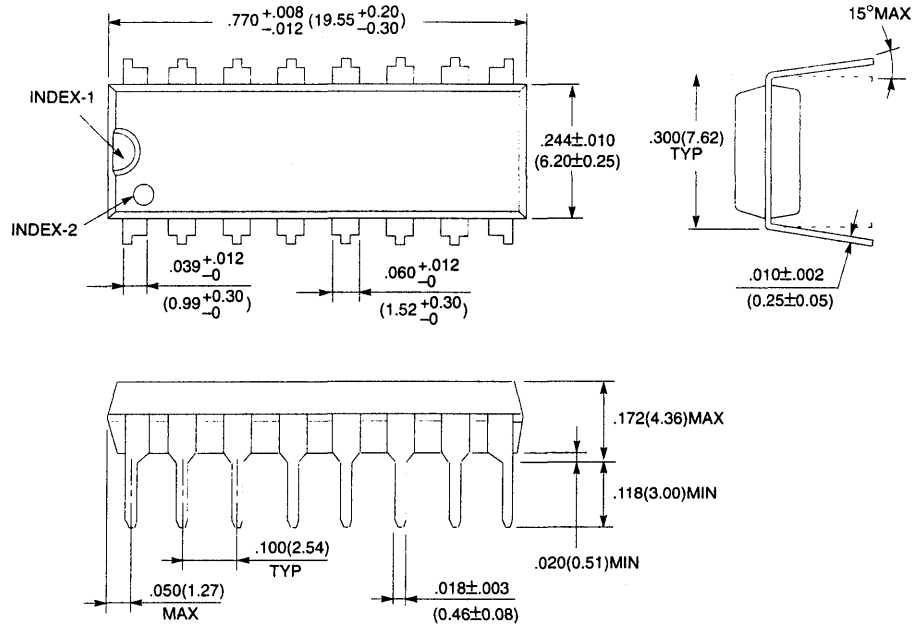
TYPICAL APPLICATION EXAMPLE



C_1, C_2: Depends on crystal oscillator
LE,FC: With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

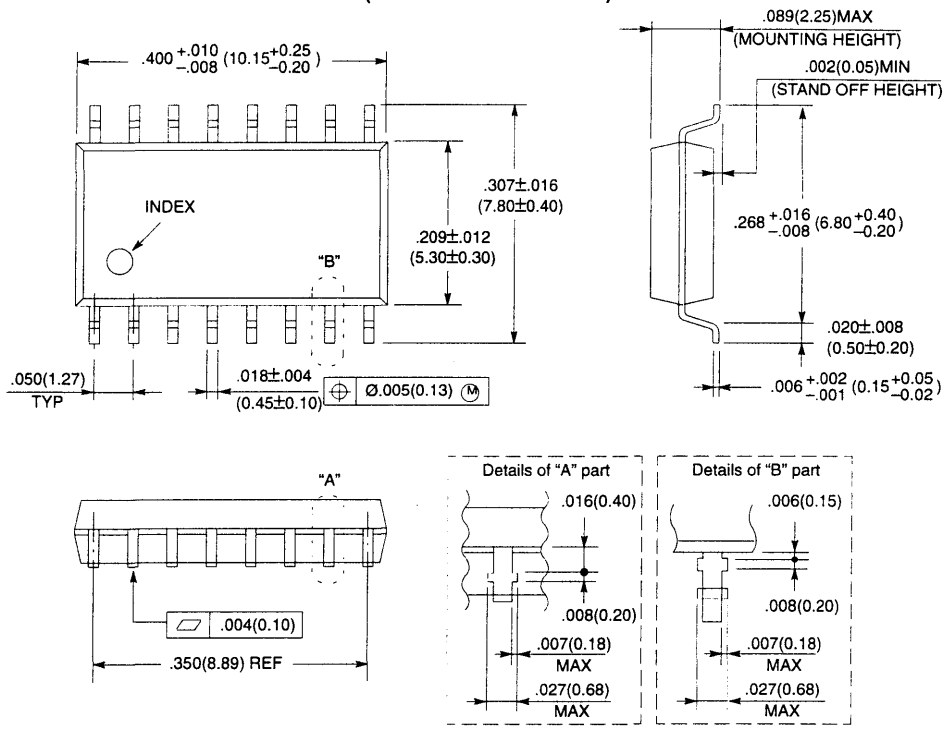
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

4

DS04–21321–1aE

FUJITSU

DATA SHEET

MB15A02 ASSP

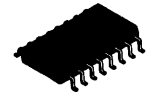
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

4

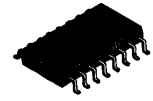
LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 1.1GHZ PRESCALER

The Fujitsu MB15A02, utilizing Bi-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.
The MB15A02 contains a 1.1GHz two modulus prescaler that can select either a 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase reverse function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, and programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).
It operates supply voltage of 5V typ. and achieves very low supply current of 7mA typ. realized through the use of Fujitsu Advanced Process Technology.

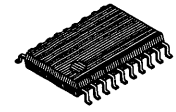
- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($P_{IN\ MIN}$=–10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC}=7mA typ.
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 16 to 2,047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 6 to 16,383
  - 1-bit switch counter (SW) sets divide ratio of prescaler
- Two types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16–pin Plastic SOP Package
  16–pin and 20–pin Plastic SSOP Packages



PLASTIC PACKAGE
FPT-16P–M05



PLASTIC PACKAGE
FPT-16P–M06



PLASTIC PACKAGE
FPT-20P–M03

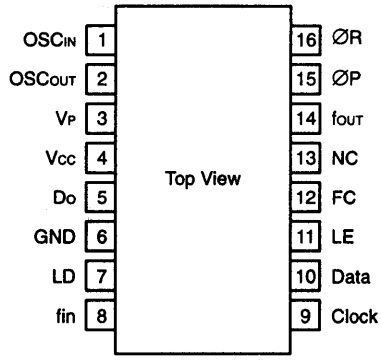
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Rating	Unit	Remark
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V	
	V_P	V_{CC} to 8.0	V	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V	ØP pin
Open-drain Voltage	V_{OOP}	–0.5 to 6.0	V	
Output Current	I_{OUT}	±10	mA	
Storage Temperature	T_{STG}	–55 to +125	°C	

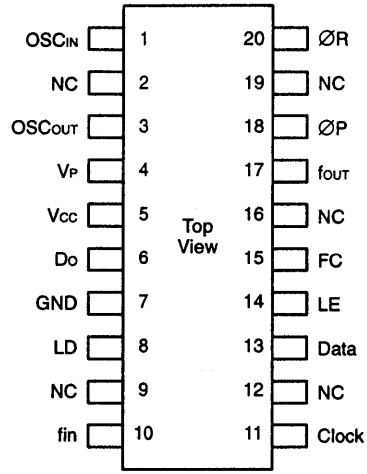
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT

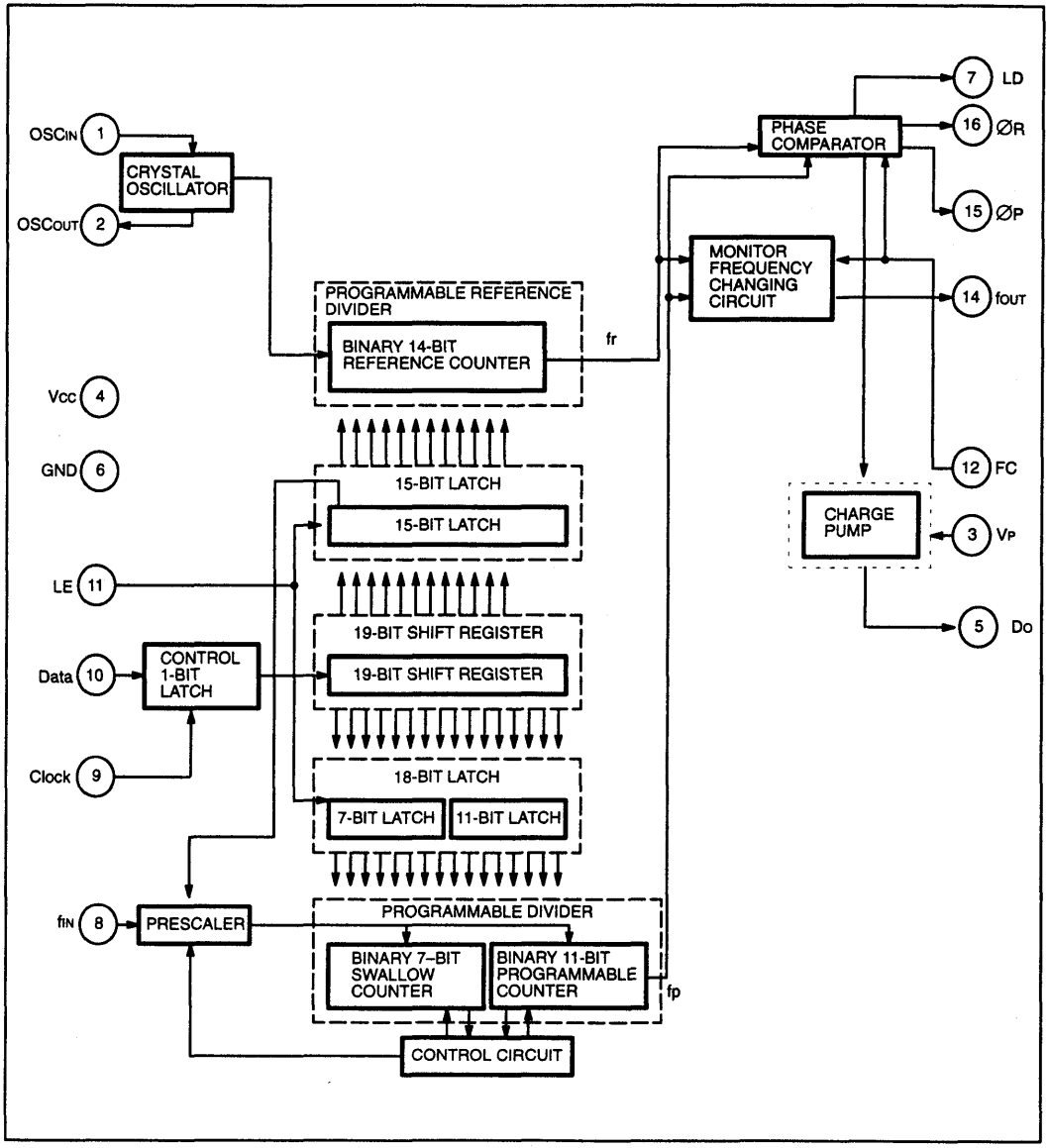


(FPT-16P-M06)
(FPT-16P-M05)



(FPT-20P-M03)

BLOCK DIAGRAM



Note : Pin numbers are based on SOP/SSOP 16–pin packages.

PIN DESCRIPTION

Pin No.		Pin Name	I/O	Description
SOP-16P SSOP-16P	SSOP-20P			
1 2	1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	4	V_P	–	Power supply pin for charge pump. When the internal charge pump is not used, V_P pin needs to be connected to V_{CC}.
4	5	V_{CC}	–	Power supply pin.
5	6	Do	O	Charge pump output.
6	7	GND	–	Ground.
7	8	LD	O	Phase comparator output. Normally this pin outputs high level. When there is a phase error between fr and fp, LD becomes low for the period corresponding to the error.
8	10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into shift register.
10	13	Data	I	Binary serial data input. The last bit of data is a control bit. When this bit is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	14	LE	I	Load enable input (with internal pull up resistor). When LE is high, the data stored in shift register is transferred into latch according to the control bit.
12	15	FC	I	Phse select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of phase comparator is reversed. FC input signal is also used to select fout pin (test pin) output, fr or fp.
13	2,9,12,16,19	NC	–	No connection
14	17	f_{OUT}	O	Minitor pin of phase comparator input. fout pin outputs either programmable reference divider output (fr) or programmable divider output (fp) according to FC pin input level. FC=H: It is the same as fr output level. FC=L: It is the same as fp output level.
15	18	ØP	O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.
16	20	ØR	O	Outputs for external charge pump. ØR pin is CMOS output.

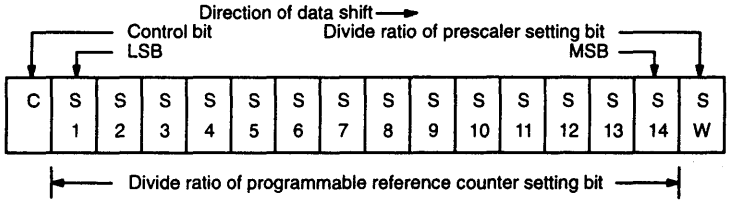
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift register and when load enable pin is high level or open, stored data is transferred into latch according to the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit programmable reference counter. Serial 16-bit data format is shown below.



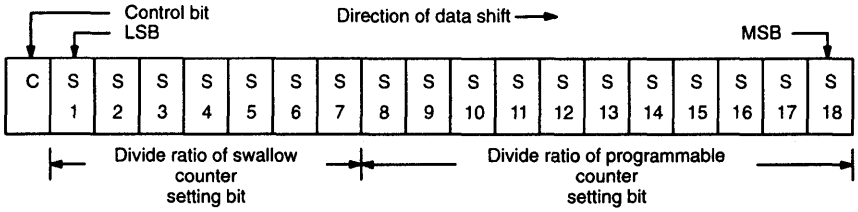
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 6 is prohibited.
Divide ratio: 6 to 16,383
SW: This bit selects divide ratio of prescaler.
SW=H : 64/65
SW=L : 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets at high level).
Start data input with MSB first.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: *Divide ratio less than 16 is prohibited.*
Divide ratio: 16 to 2,047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit.
C: Control bit (sets at low level).
Data input with MSB first.

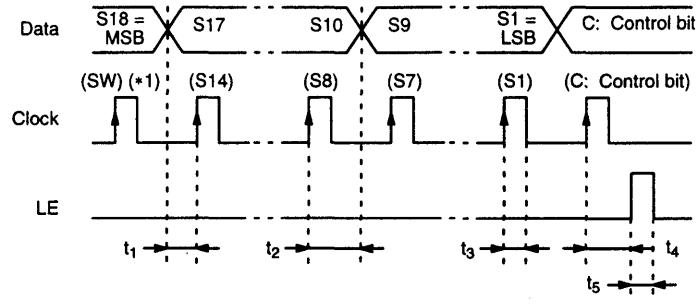
PULSE SWALLOW FUNCTION

$fvco = [(PxN)+A] \times fosc \div R$

fvco: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
fosc: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (6 to16,383)
P: Preset modulus of external dual modulus prescaler (64 or 128)

Serial data input timing

- t_1 (≥ 100ns) : Data setup time t_2 (≥ 1000ns) : Data hold time t_3 (≥ 300ns) : Clock pulse width
  t_4 (≥ 100ns) : LE setup time to the rising edge of last clock t_5 (≥ 800ns) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

4

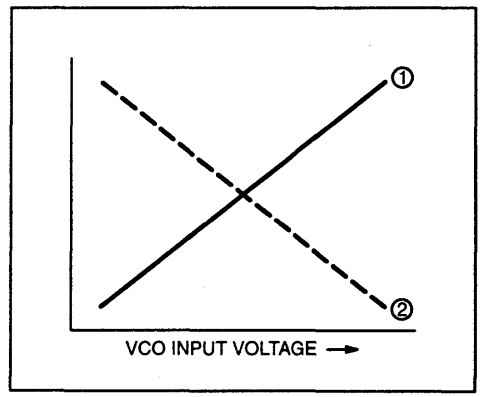
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (Do), phase comparator output level (ØR, ØP) are reversed depending upon FC pin input level. Also, monitor pin (fout) output level of phase comparator is controlled by FC pin input level. The relation between outputs (Do, ØR, ØP) and FC input level are shown below.

	FC=H or open				FC=L			
	DO	ØR	ØP	fout	DO	ØR	ØP	fout
fr>fp	H	L	L	(fr)	L	H	Z	(fp)
fr<fp	L	H	Z	(fr)	H	L	L	(fp)
fr=fp	Z	L	Z	(fr)	Z	L	Z	(fp)

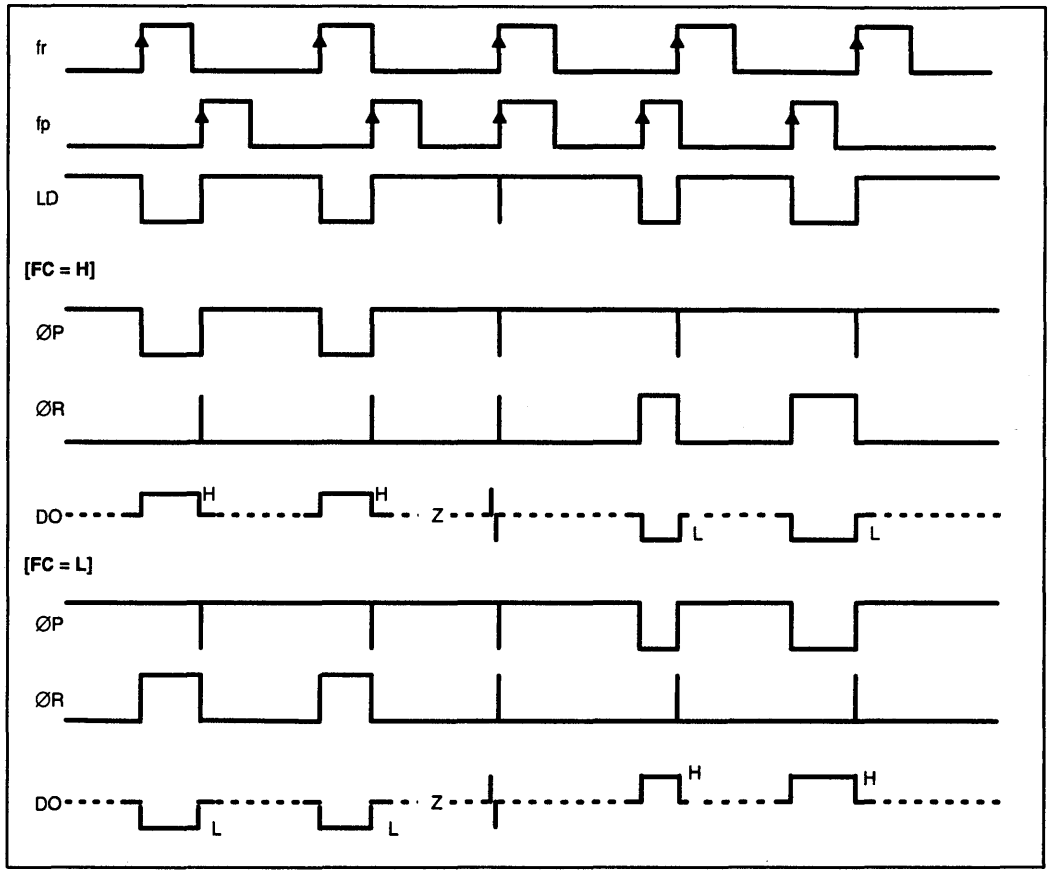
Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set High or open circuit;
When VCO characteristics are like ②, FC should be set Low.

OUTPUT WAVEFORM



NOTE: Phase error detection range: -2π to $+2\pi$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	–	6.0	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	Ta	–40	–	85	°C

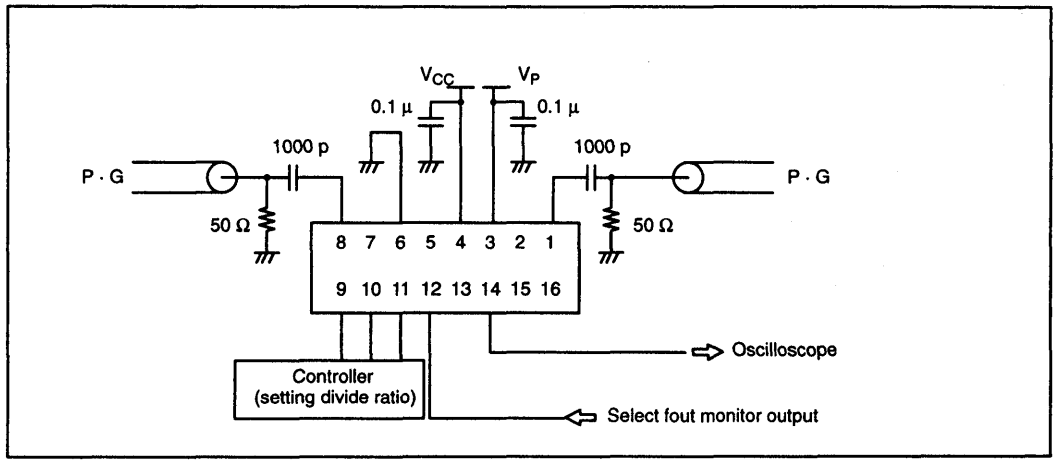
ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Power Supply Current		I_{CC}	–	7.0	–	mA	*1
Operating Frequency	fin	fin	10	–	1100	MHz	*2
	OSC_{IN}	f_{OSC}	–	12	20	MHz	
Input Sensitivity	fin	Pfin	–10	–	6	dBm	50Ω system
	OSC_{IN}	V_{OSC}	0.5	–	–	V_{PP}	
High-level Input Voltage	Clock, Data, LE	V_{IH}	Vccx0.7	–	–	V	
Low-level Input Voltage		V_{IL}	–	–	Vccx0.3	V	
High-level Input Current	Data Clock	I_{IH}	–	–	1.0	µA	
Low-level Input Current		I_{IL}	–	–	–1.0	µA	
Input Current	OSC_{IN}	I_{OSC}	–	±50	–	µA	
	LE, FC	I_{LE}	–	–60	–	µA	
High-level Output Voltage	ØR, LD	V_{OH}	4.4	–	–	V	V_{CC}=5V, I_{OH} = –1.0mA
Low-level Output Voltage	ØR, ØP, LD	V_{OL}	–	–	0.4	V	V_{CC}=5V, I_{OL} = 1.0mA
High impedance Cutoff Current	Do, ØP	I_{OFF}	–	–	1.1	µA	V_P=Vcc to 6V V_{OOP}=GND to 6V
Output Current	ØR, LD	I_{OH}	–1.0	–	–	mA	V_{CC}=5V
	ØR, ØP, LD	I_{OL}	–	–	1.0	mA	V_{CC}=5V

*1: fin=1.1GHz, OSC_{IN}=12MHz, V_{CC}=5V. In locked state.
*2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

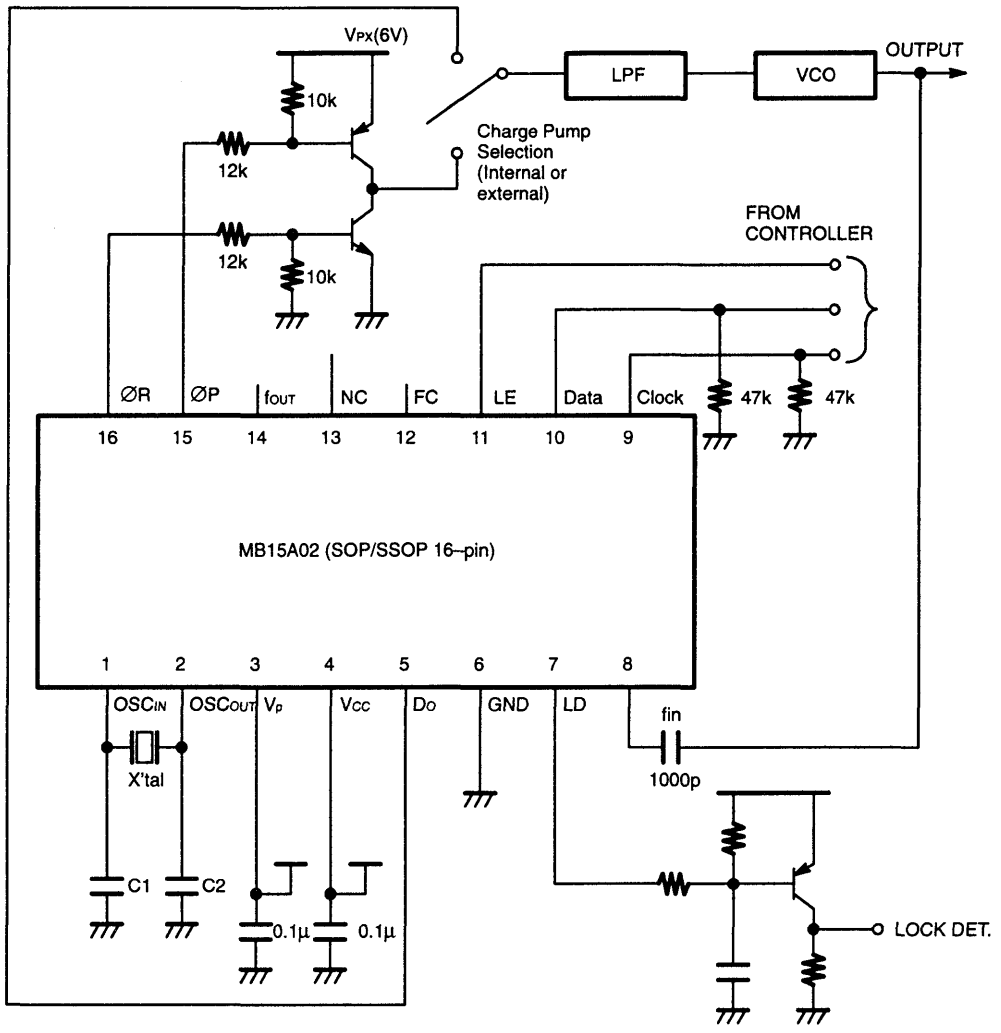
4

TEST CIRCUIT
(FOR MEASURING INPUT SENSITIVITY fin/OSCin)



Note : Pin numbers are based on SOP/SSOP 16–pin packages.

TYPICAL APPLICATION EXAMPLE



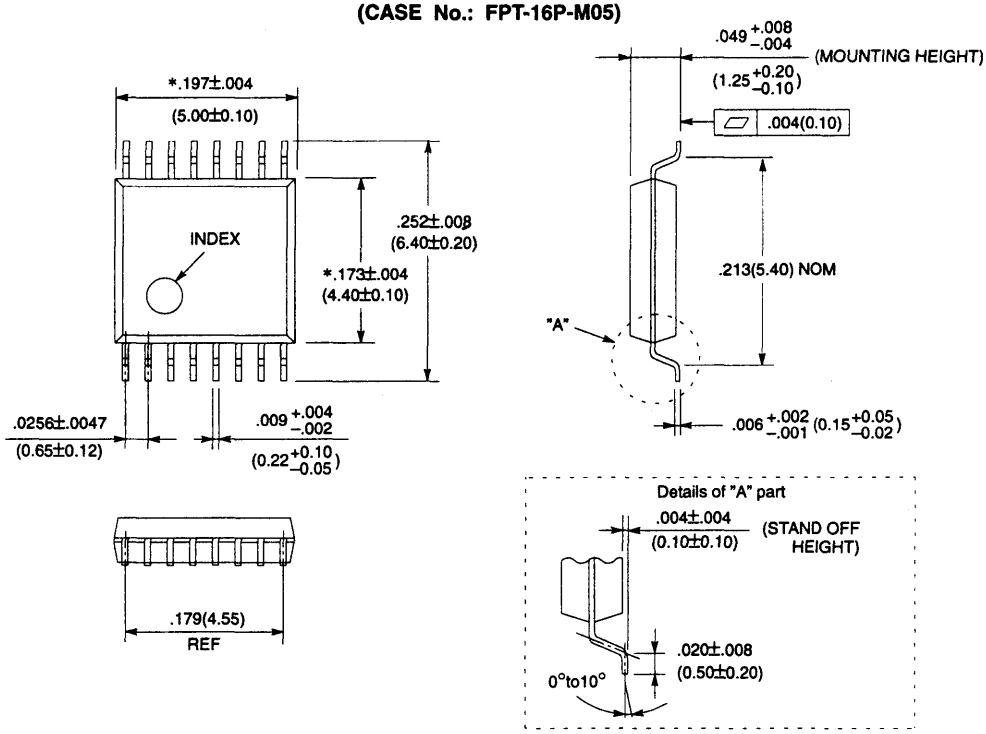
VPX : 6V max.
VP : When internal charge pump is not used, VP pin needs to be connected to VCC.
C1, C2: Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output
ØR : CMOS output

ORDERING INFORMATION

Part Number	Package
MB15A02PF	Plastic SOP, 16–pin FTP–16P–M06
MB15A02PFV1	Plastic SSOP, 16–pin FTP–16P–M05
MB15A02PFV2	Plastic SSOP, 20–pin FTP–20P–M03

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



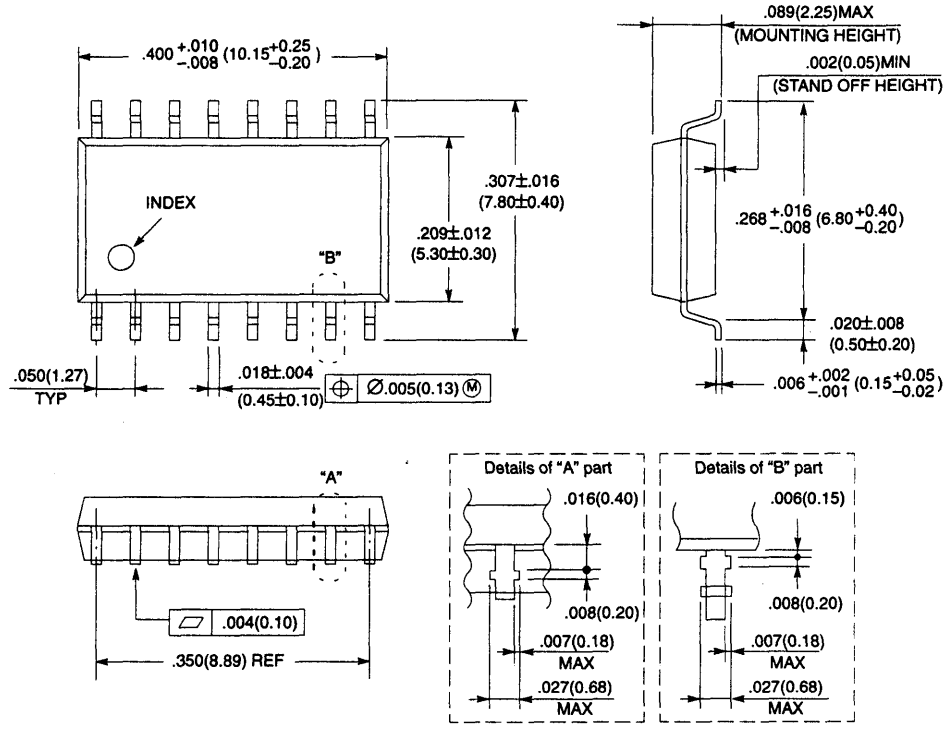
*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

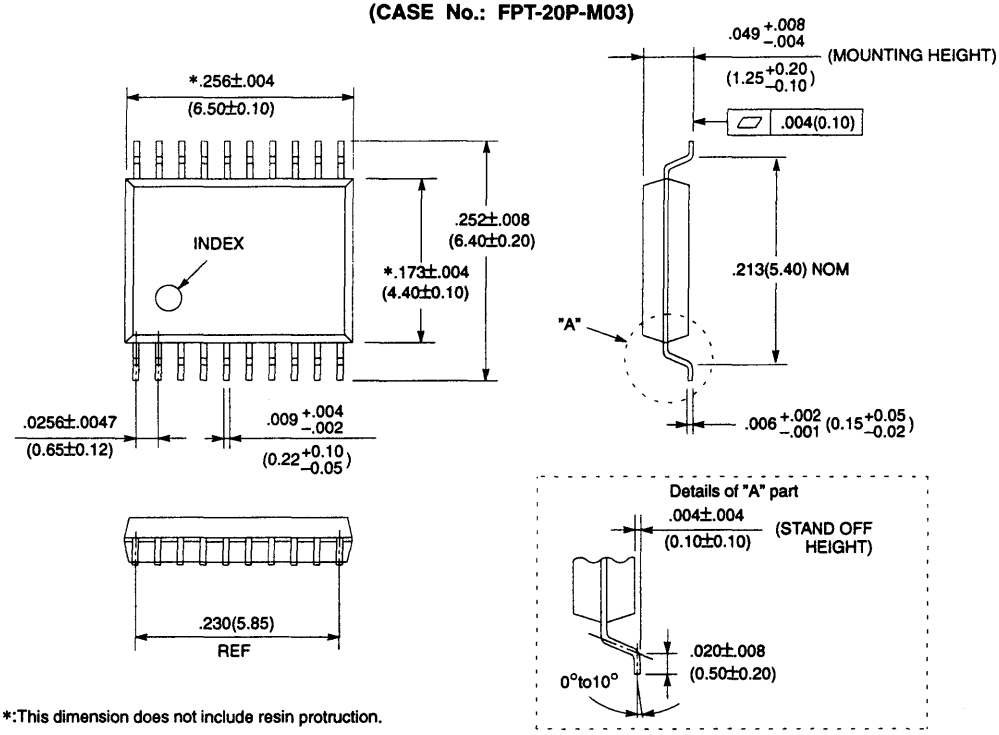
16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

Sept. 1995
Edition 5.0b

DATA SHEET

FUJITSU

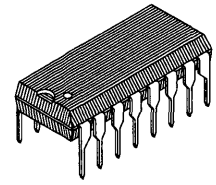
MB1502/MB1502H

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

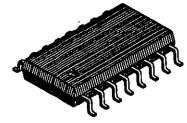
LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 1.1 GHz PRESCALER

The Fujitsu MB1502/MB1502H, utilizing Bi-CMOS technology, are single chip serial input PLL synthesizers with pulse-swallow function. Each MB1502/MB1502H contains a 1.1GHz two modulus prescaler that can select of either 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analog switch to speed up lock up time.

They operate at a supply voltage of 5V typ. and achieves a very low supply current of 8mA typ. realized through the use of Fujitsu Advanced Process Technology.



Plastic Package
DIP-16P-M04



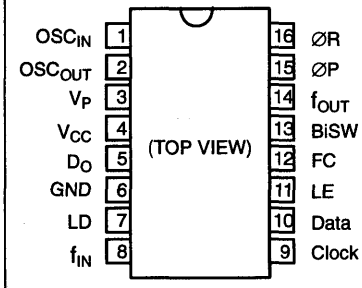
Plastic Package
FPT-16P-M06

4

FEATURES

- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($P_{IN\ MIN}$=10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC}=8mA typ.
- Serial input 18-bit programmable divider consisting of:
  — Binary 7-bit swallow counter: 0 to 127
  — Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  — Binary 14-bit programmable reference counter: 8 to 16383
  — 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2 types of phase detector output
  — On-chip charge pump (Bipolar type)
  — Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic DIP Package (Suffix: —P)
  16-pin Plastic Flat Package (Suffix: —PF)

Pin Assignment

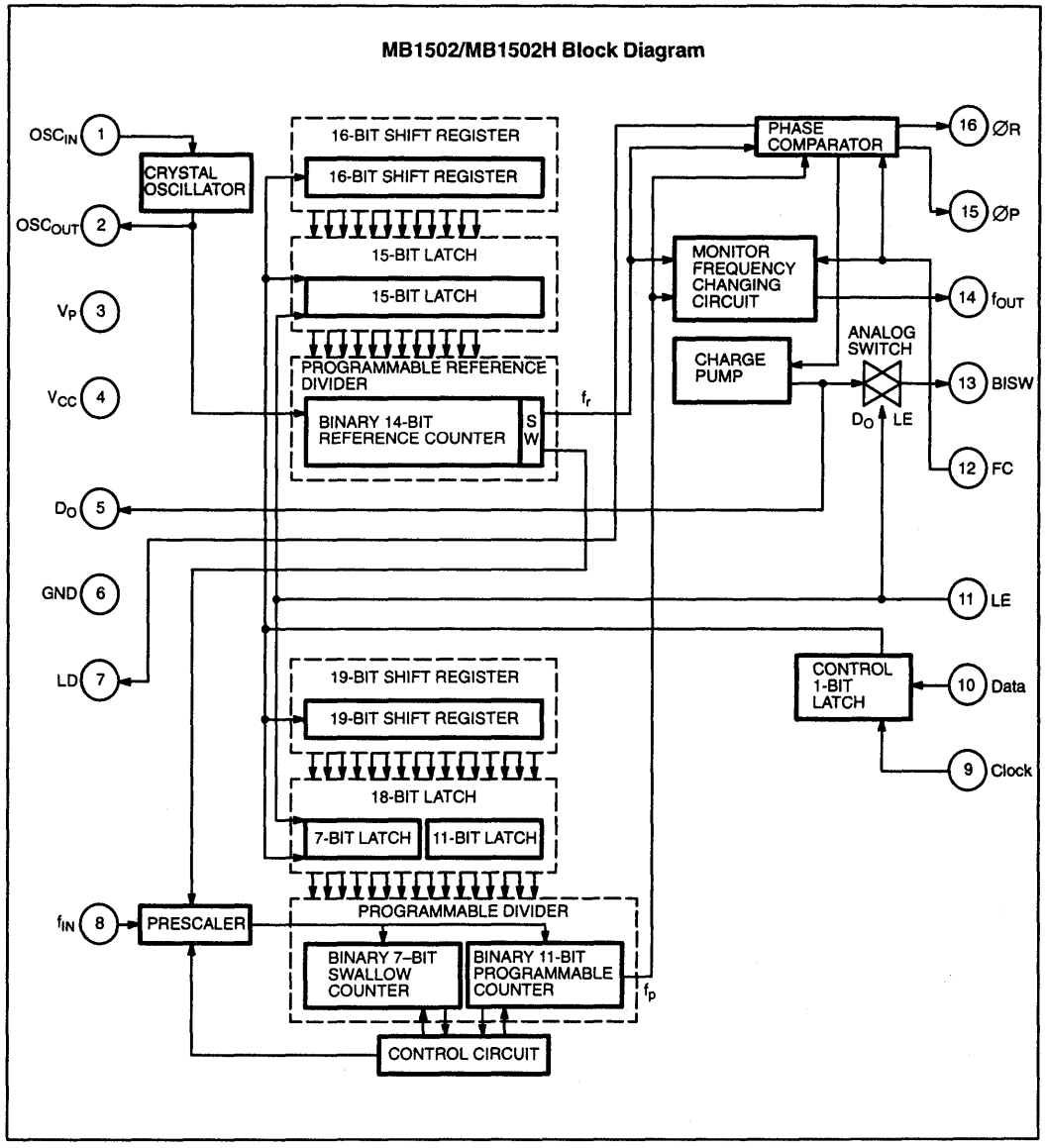


ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 0.8	V
Output Current	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.


MB1502/MB1502H Block Diagram
OSCIN 1
CRYSTAL OSCILLATOR
OSCOUT 2
VP 3
VCC 4
DO 5
GND 6
LD 7
fIN 8
PRESCALER
16-BIT SHIFT REGISTER
16-BIT SHIFT REGISTER
15-BIT LATCH
15-BIT LATCH
PROGRAMMABLE REFERENCE DIVIDER
BINARY 14-BIT REFERENCE COUNTER
S W
fr
19-BIT SHIFT REGISTER
19-BIT SHIFT REGISTER
18-BIT LATCH
7-BIT LATCH
11-BIT LATCH
PROGRAMMABLE DIVIDER
BINARY 7-BIT SWALLOW COUNTER
BINARY 11-BIT PROGRAMMABLE COUNTER
fp
CONTROL CIRCUIT
PHASE COMPARATOR
MONITOR FREQUENCY CHANGING CIRCUIT
CHARGE PUMP
ANALOG SWITCH
DO
LE
CONTROL 1-BIT LATCH
16 ØR
15 ØP
14 fOUT
13 BISW
12 FC
11 LE
10 Data
9 Clock

PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump and analog switch.
4	V_{CC}	—	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
6	GND	—	Ground
7	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r, and f_p exists, this pin outputs low level.
8	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control fOUT pin (test pin) output level for f_r or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
14	f_{OUT}	O	Monitor pin of phase comparator input. f_{OUT} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level.
15 16	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.

Binary serial data is input to Data pin.

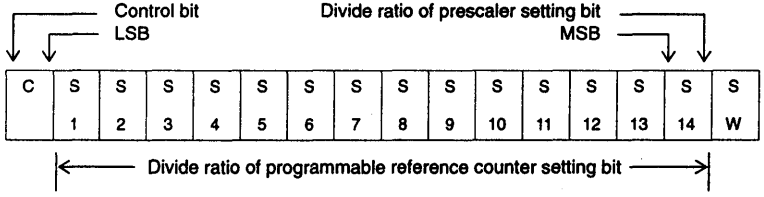
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.

Control data "H" data is transferred into 15-bit latch.

Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

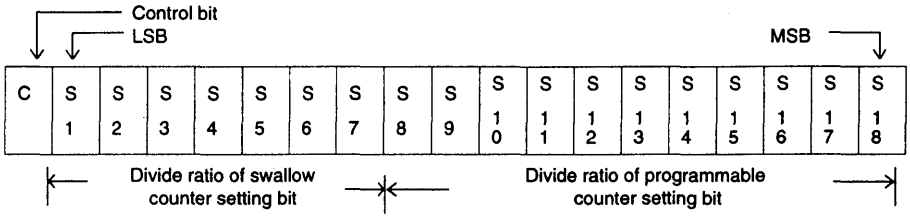
Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64
SW=L :128
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.

Serial 19-bit data format is shown on following page.



4

7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

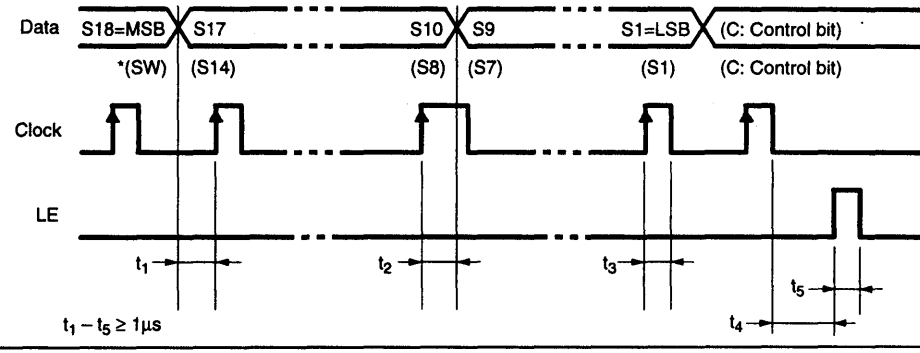
NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times N) + A] \times f_{OSC} + R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)
P: Preset modulus of external dual modulus prescaler (64 or 128)

Serial Data Input Timing



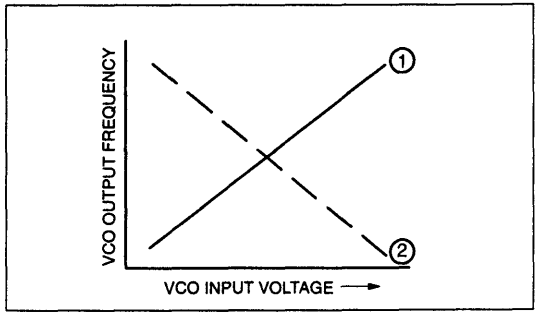
NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (øR, øP) are reversed depending upon FC pin input level. Also, monitor pin (f_{OUT}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, øR, øP) and FC input level are shown below.

	FC=H or open				FC=L			
	D_O	øR	øP	f_{OUT}	D_O	øR	øP	f_{OUT}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

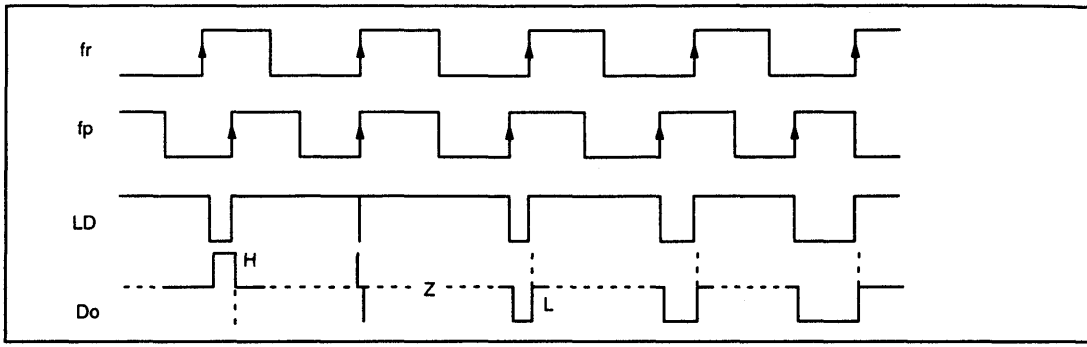
Note: Z = (High impedance)



VCO CHARACTERISTICS
Depending upon VCO characteristics, FC pin should be set accordingly:

— When VCO characteristics are like 1, FC should be set High or open circuit;

— When VCO characteristics are like 2, FC should be set Low.



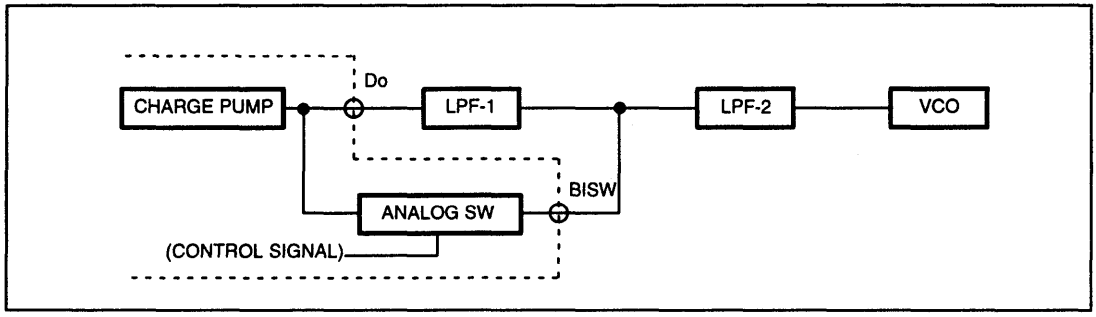
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r > f_p$ or $f_r < f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) to be connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode): Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	V_P	8.0	V
Input Voltage	V_I	GND		V_{CC}	V
Operating Temperature	T_A	–40		85	°C

ELECTRICAL CHARACTERISTICS

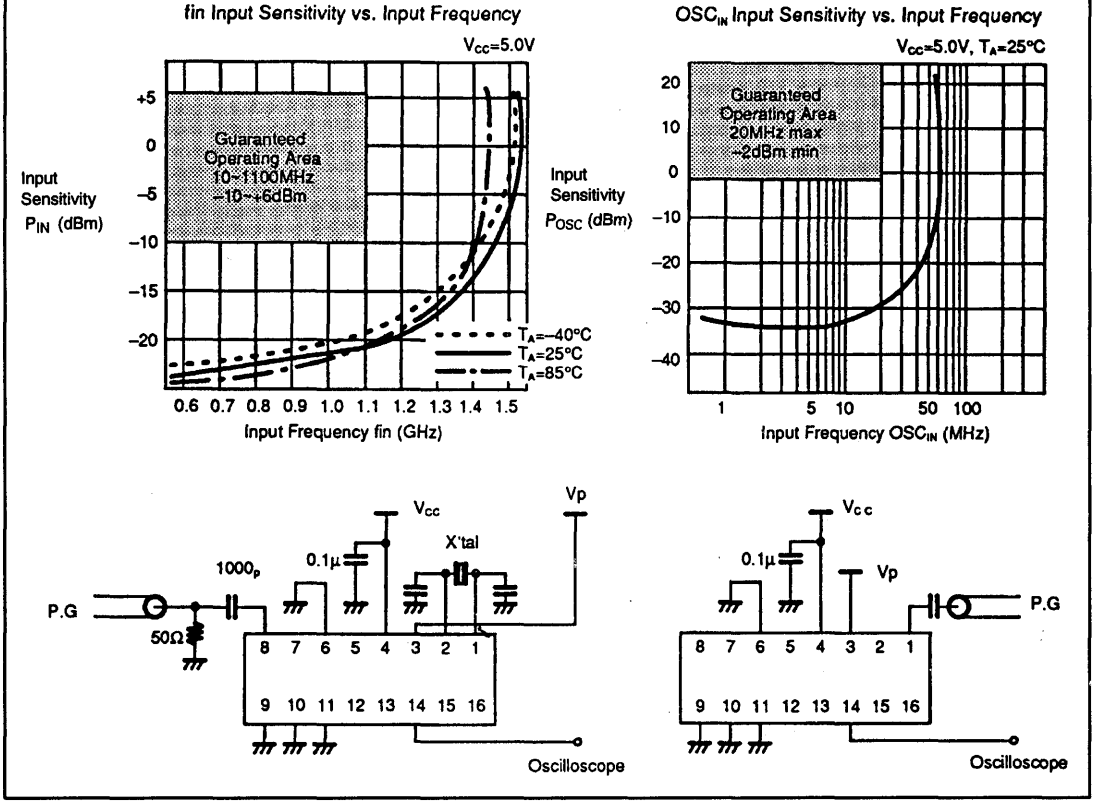
(Vcc=4.5 to 5.5V, TA=–40 to +85°C, unless otherwise noted.)

Parameter		Symbol	Condition		Value			Unit
					Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1			8.0	12.0	mA
Operating Frequency	f_{in}	f_{in}	Note2		10		1100	MHz
	OSC_{IN}	f_{OSC}				12	20	MHz
Input Sensitivity	f_{in}	P_{fin}			–10		6	dBm
	OSC_{IN}	V_{OSC}			0.5			V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}			V_{CC}x0.7			V
Low-level Input Voltage		V_{IL}					V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}				1.0		µA
Low-level Input Current		I_{IL}				–1.0		µA
Input Current	OSC_{IN}	I_{OSC}				±50		µA
	LE, FC	I_{LE}				–60		µA
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 5 V		4.4			V
Low-level Output Voltage		V_{OL}					0.4	V
N-channel Open Drain Cutoff Current	D_O, ØP	I_{OFF}	$V_P = V_{CC}$ to 8V V_{OOP}= GND to 8V				1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}			–1.0			mA
		I_{OL}			1.0			mA
High-level Output Current	Do Do	I_{DDH}	MB1502	V_{CC}=5V, V_P= 8V, T_A=25°C	–0.8	–1.5		mA
Low-level Output Current		I_{DOL}			11	22		mA
High-level Output Current		I_{DOLH}	MB1502H		–1.4	–2.4		mA
Low-level Output Current		I_{DOLH}			4.5	10		mA
Analog Switch On Resistor		R_{ON}				25		Ω

NOTE: 1: f_{in} = 1.1GHz, OSC_{IN}=12MHz, V_{cc}=5V. Inputs are grounded and outputs are open.
2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

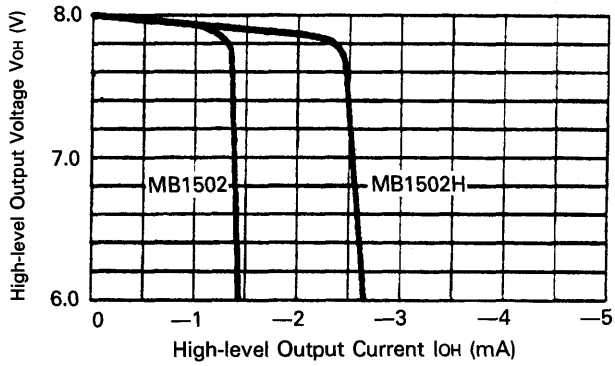
TYPICAL CHARACTERISTICS CURVES

INPUT SENSITIVITY CHARACTERISTICS

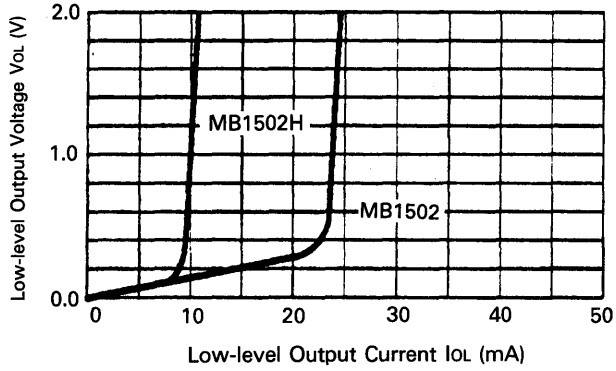


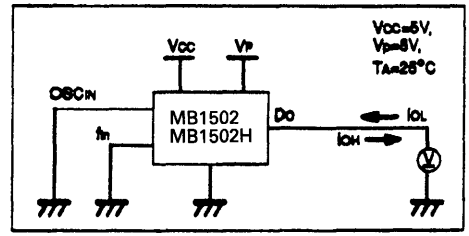
DO PIN OUTPUT CURRENTCURVES (TYPICAL)

V_{OH} vs. I_{OH}

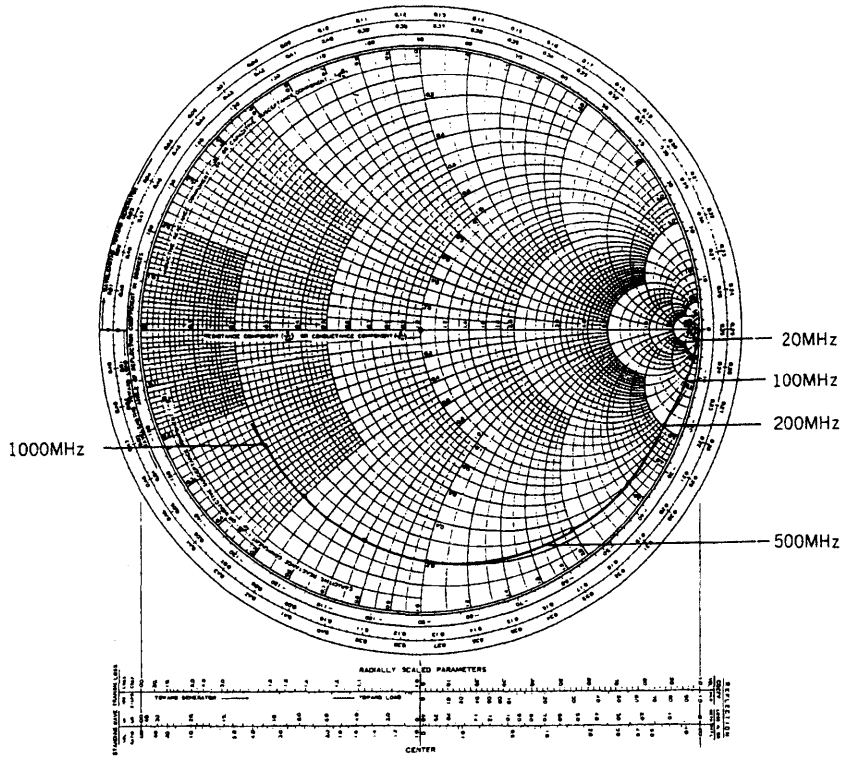


V_{OL} vs. I_{OL}

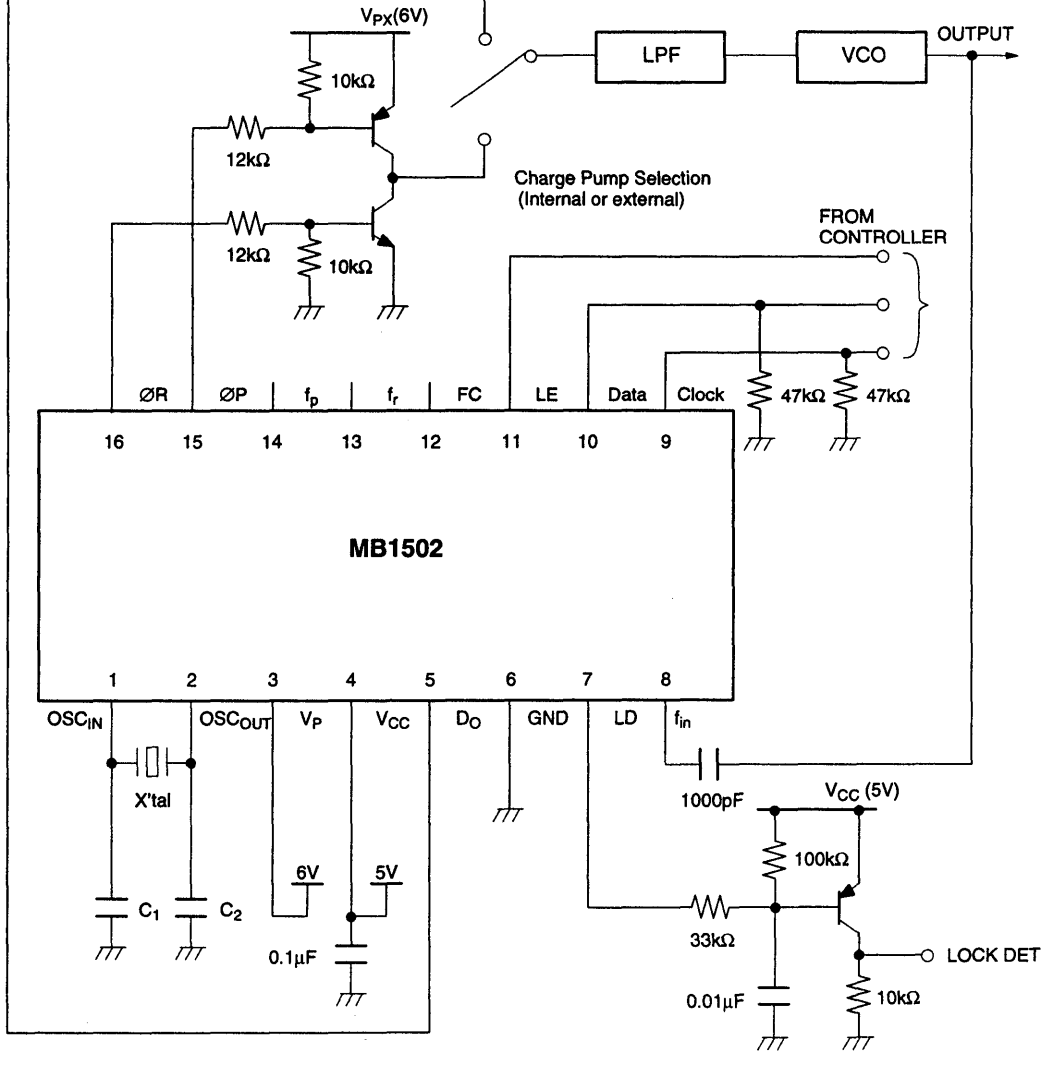




INPUT IMPEDANCE CHARACTERISTICS



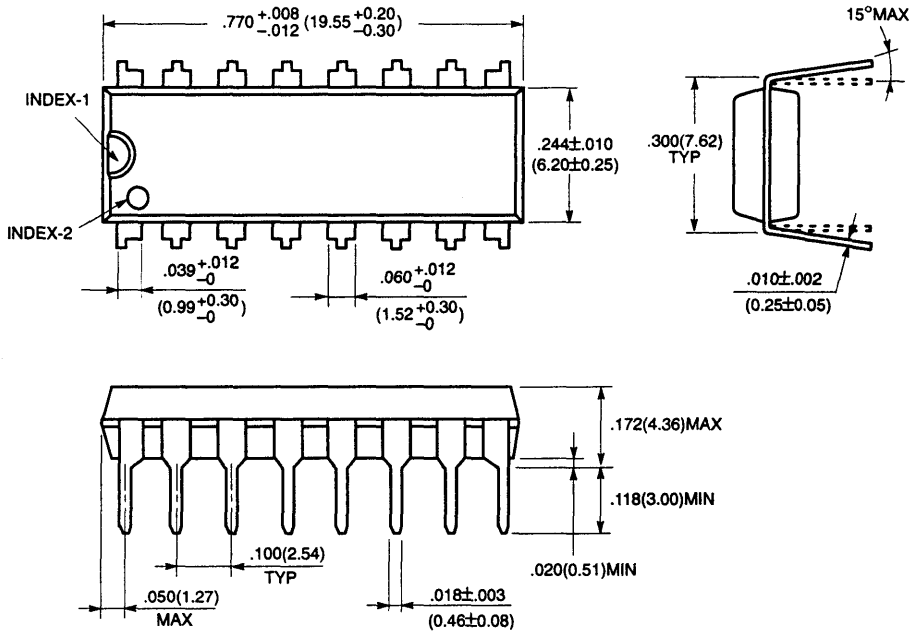
TYPICAL APPLICATION EXAMPLE



VP, VPX : 8V max
C1, C2 : Depends on crystal oscillator
LE, FC : With internal pull up resistor
ØP : Open drain output

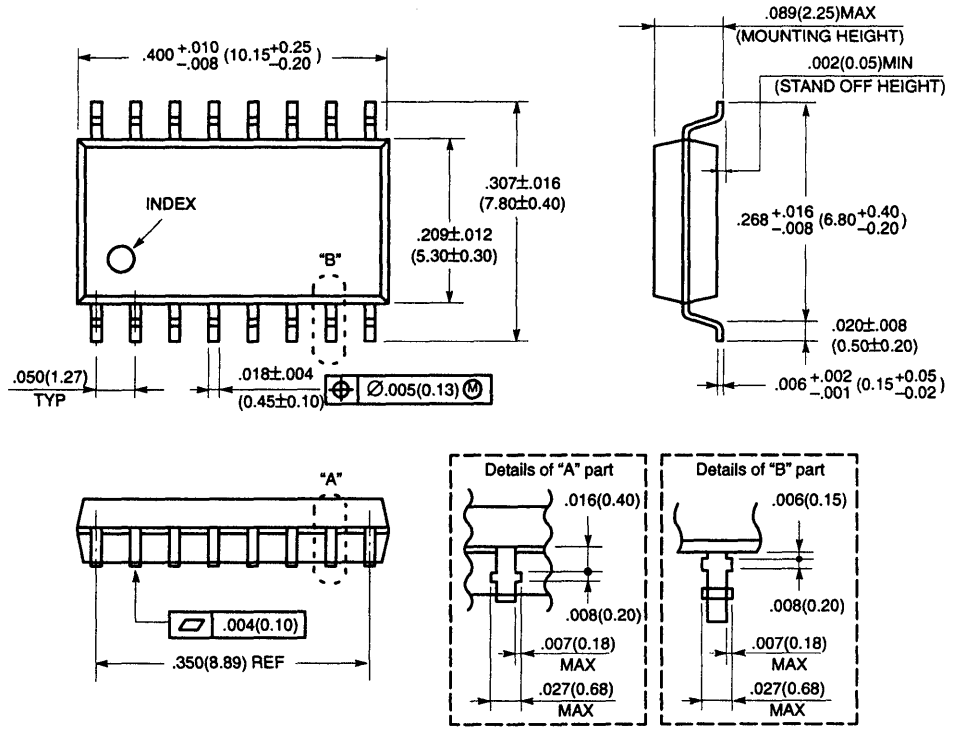
PACKAGE DIMENSIONS

16–Lead Plastic Dual In–Line Package
(Case No.: DIP–16P–M04)



Dimensions in
inches (millimeters)

16–Lead Plastic Flat Package
(Case No.: FPT–16P–M06)



Dimensions in
inches (millimeters)

June 1995
Edition 0.1

FUJITSU

MB15B03 Product Profile Sheet

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

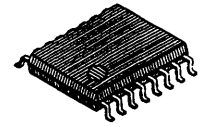
On-chip 1.1GHz & 300MHz PRESCALER

PRELIMINARY

The Fujitsu MB15B03 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 1.1GHz and a 300MHz prescalers. A 64/65 or a 128/129 for the 1.1GHz prescaler, and a 16/17 or a 32/33 for 300MHz prescaler can be selected that enables pulse swallow operation.

Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15B03 is ideally suitable for digital mobile communications, such as GSM.

PACKAGE



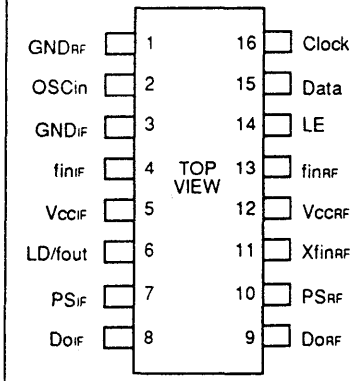
FPT-16P-M05

4

FEATURES

- High frequency operation RF synthesizer : 1.1GHz max.
  IF synthesizer : 300MHz max.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 10 mA typ. (V_{CC} = 3V)
- Power saving function : I_{PS1} = I_{PS2} = 100 µA typ. (V_{CC} = 3V)
- Serial input 14-bit programmable reference counter: R = 6 to 16,383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 5 to 2,047
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Wide operating temperature: T_A = –40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

PIN ASSIGNMENT

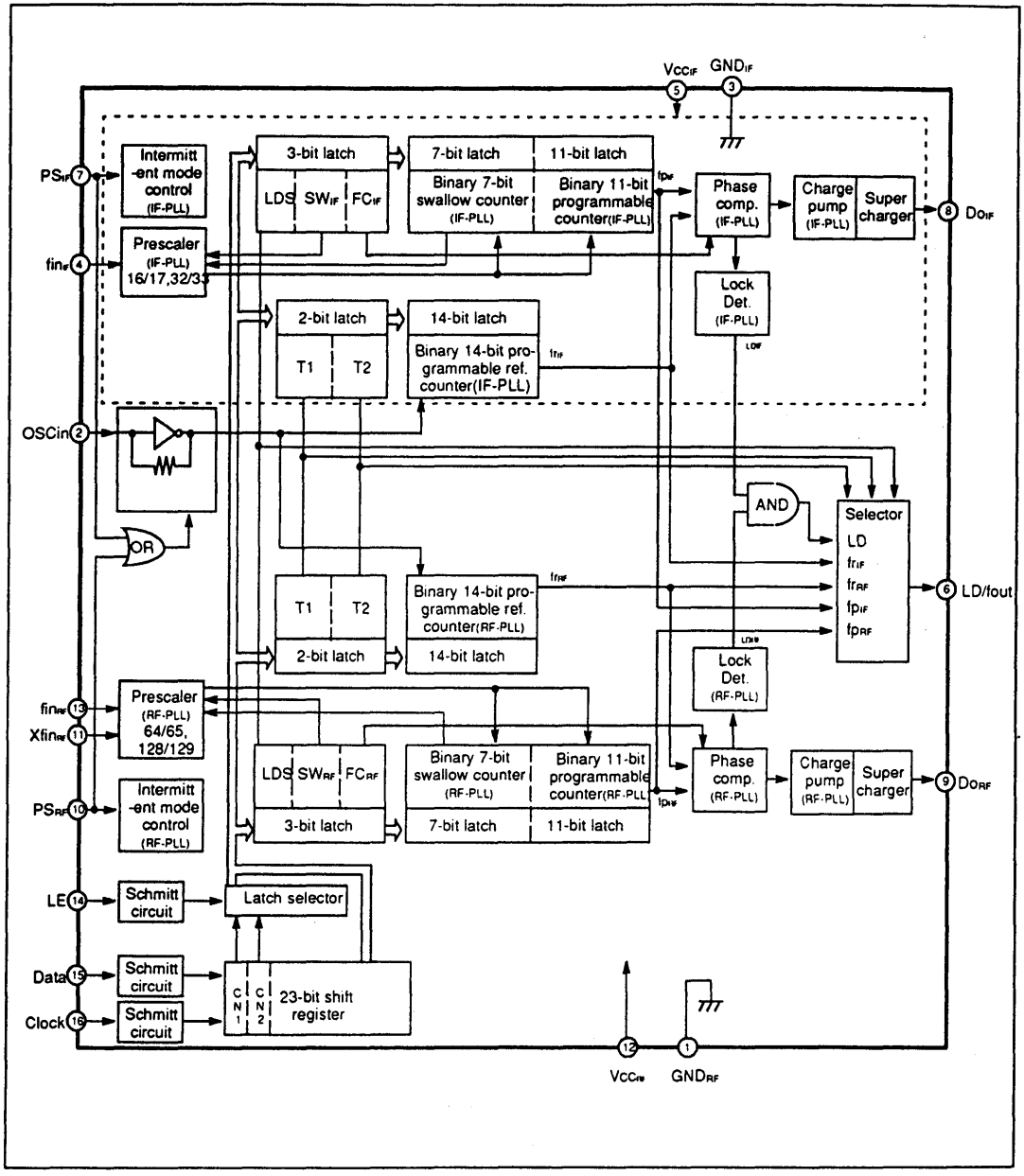


ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Remark	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to 5.0	V
Output Voltage	V_O		–0.5 to V_{CC} +0.5	V
Output Current	I_O		±10	mA
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	GND_{RF}	–	Ground for RF-PLL section.
2	OSCin	I	The programmable reference divider input. TCXO should be connected with a coupling capacitor.
3	GND_{IF}	–	Ground for the IF section.
4	fin_{IF}	I	Prescaler input pin for the IF-PLL. The connection with VCO should be AC coupling.
5	V_{CCIF}	–	Power supply voltage input pin for the IF-PLL section. When power is OFF, latched data of the IF-PLL is cancelled.
6	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout) The output signal is selected by a LDS bit in a serial data. LDS bit = "H" ; outputs fout signal LDS bit = "L" ; outputs LD signal
7	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at "L" at Power–ON. (Open is prohibited.) PS_{IF} = "H" ; Normal mode PS_{IF} = "L" ; Power saving mode
8	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase comparator can be reversed by the FC-bit.
9	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase comparator can be reversed by the FC-bit.
10	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at "L" at Power–ON. (Open is prohibited.) PS_{RF} = "H" ; Normal mode PS_{RF} = "L" ; Power saving mode
11	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
12	V_{CCRF}	–	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled.
13	fin_{RF}	I	Prescaler input pin for the RF-PLL. The connection with VCO should be AC coupling.
14	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
15	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-Prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
16	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a riging edge of the clock.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$fvco = \{(P \times N) + A\} \times fosc + R \quad (A < N)$

fvco: Output frequency of external voltage controlled ocillator (VCO)
P: Preset divide ratio of dual modulus prescaler (16 or 32 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
fosc: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)

SERIAL DATA INPUT

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. CONTROL BIT

Control bits		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the IF-PLL.
H	L	The programmable reference counter for the RF-PLL.
L	H	The programmable counter and the swallow counter for the IF-PLL
H	H	The programmable counter and the swallow counter for the RF-PLL

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

CNT1, 2 : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (6 to 16,383) [Table. 2]
T1, 2 : Test purpose bit [Table. 3]

FUNCTIONAL DESCRIPTIONS

Programmable Counter

LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CN1, 2 : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2047) [Table. 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]
SW : Divide ratio setting bit for the prescaler [Table. 6]
(16/17 or 32/33 for the IF-PLL, 64/65 or 128/129 for the RF-PLL)
FC : Phase control bit for the phase detector [Table. 7]
LDS : LD/fout signal select bit [Table. 8]

Table2. BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 6 is prohibited.

Table.3 TEST PURPOSE BIT SETTING

T1	T2	LD/fout pin state
L	L	Outputs fr_{IF}.
H	L	Outputs fr_{RF}.
L	H	Outputs fp_{IF}.
H	H	Outputs fp_{RF}.

Table.4 BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note:• Divide ratio less than 5 is prohibited.

Table.5 BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note:• Divide ratio (A) range = 0 to 127

Table. 6 PRESCALER DATA SETTING

		SW = "H"	SW = "L"
Prescaler Divide ratio	IF-PLL	16/17	32/33
	RF-PLL	64/65	128/129

Table. 7 PHASE COMPARATOR PHASE SWITCHING DATA SETTING

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: • Z = High-impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

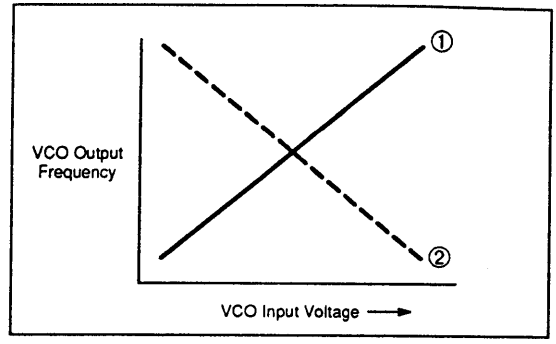
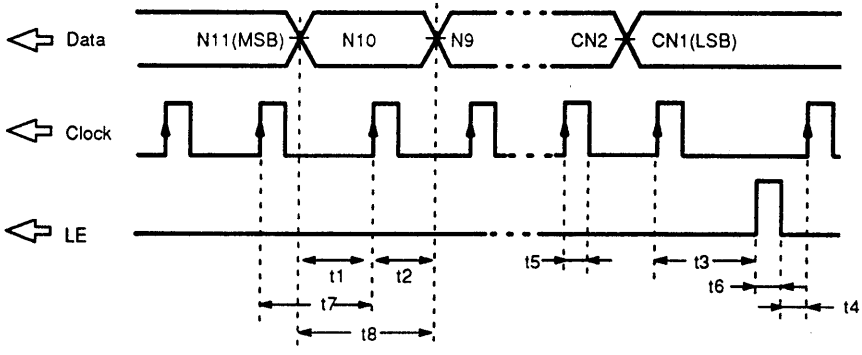


Table. 8 LD/fout OUTPUT SELECT DATA SETTING

LDS	LD/fout output signal
H	fout ($fr_{IF/RF}$, $fp_{IF/RF}$) signals
L	LD signal

SERIAL DATA INPUT TIMING

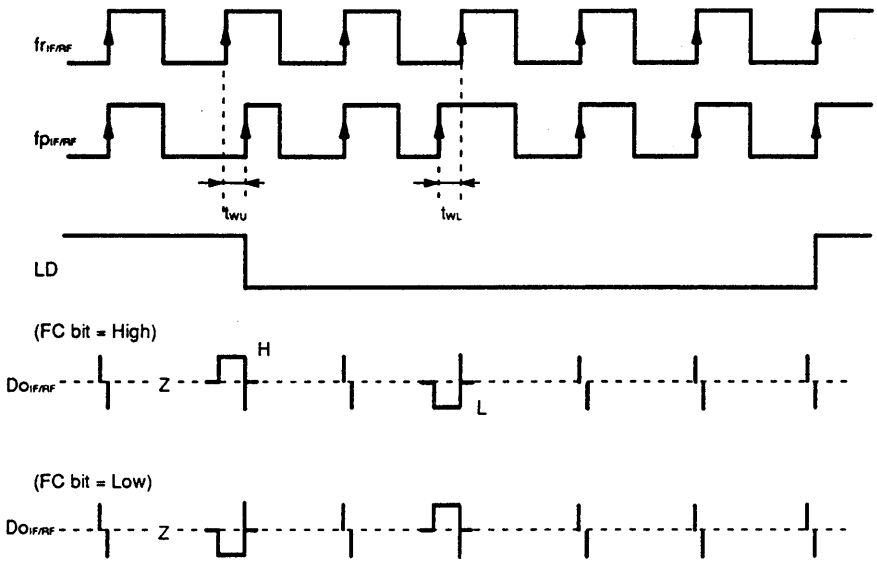


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	30	–	–	ns
t2	30	–	–	ns
t3	30	–	–	ns
t4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	100	–	–	ns
t6	100	–	–	ns
t7	200	–	–	ns
t8	200	–	–	ns

PHASE DETECTOR OUTPUT WAVEFORM



LD OUTPUT LOGIC TABLE

IF-PLL section	RF-PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

Note: • Phase error detection range = -2π to $+2\pi$

- Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{wu} or more.
- LD output becomes high when phase error is t_{wL} or less and continues to be so for three cycles or more.
- t_{wu} and t_{wL} depend on OSCin input frequency as follows.
  $t_{wu} \geq 8/fosc$: i.e. $t_{wu} \geq 625ns$ when foscin = 12.8 MHz
  $t_{wL} \leq 16/fosc$: i.e. $t_{wL} \leq 1250ns$ when foscin = 12.8 MHz

POWER SAVING MODE (INTERMITTENT MODE CONTROL CIRCUIT)

Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL(RF-PLL) enters into power saving mode resultatly current sonsumption can be limited to 100μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
PS pin must be set "L" at Power–ON.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 100μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance. A VCO control voltage is naturally kept at the locking voltage which defined by a LPF"s time constant. As a result of this, VCO's frequency is kept at the locking frequency.

PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	Vcc	2.7	3.0	3.6	V	$V_{CC_{IF}} = V_{CC_{RF}}$
Input Voltage	Vi	GND	–	Vcc	V	
Operating Temperature	Ta	−40	–	+85	°C	

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current *1		$I_{CC_{IF}}$	fin_{IF} = 300MHz, fosc = 12MHz	–	3.5	–	mA
		$I_{CC_{RF}}$	fin_{RF} = 1100MHz, fosc = 12MHz	–	6.5	–	
Power Saving Current *2		$I_{PS_{IF}}$	$V_{CC_{IF}}$ current at PS_{IF} = "L"	–	100	–	μA
		$I_{PS_{RF}}$	$V_{CC_{RF}}$ current at $PS_{IF/RF}$ = "L"	–	100	–	
Operating Frequency	fin_{IF}	fin_{IF}	IF-PLL	50	–	300	MHz
	fin_{RF}	fin_{RF}	RF-PLL	100	–	1100	
	OSCin	f_{OSC}	min. 500mVp-p	–	12.8	23	
Input Sensitivity	fin_{IF}	$Pfin_{IF}$	IF-PLL, 50Ω termination (Refer to the test circuit.)	−10	–	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF-PLL, 50Ω termination (Refer to the test circuit.)	−10	–	+2	dBm
	OSCin	V_{OSC}		500	–	–	mVp-p

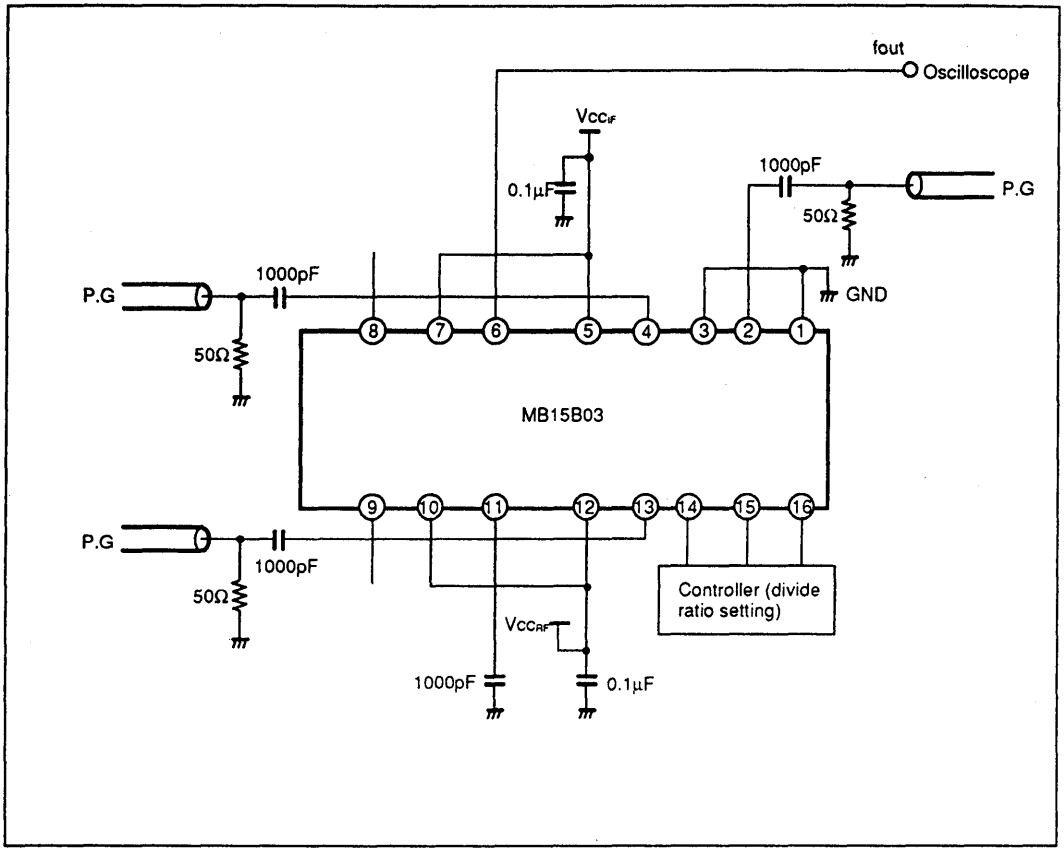
*1: Conditions ; $V_{CC_{IF/RF}}$ = 3V, Ta = 25°C, in locking state.
*2: Conditions ; $V_{CC_{IF/RF}}$ = 3V, Ta = 25°C, in power saving state.

ELECTRICAL CHARACTERISTICS

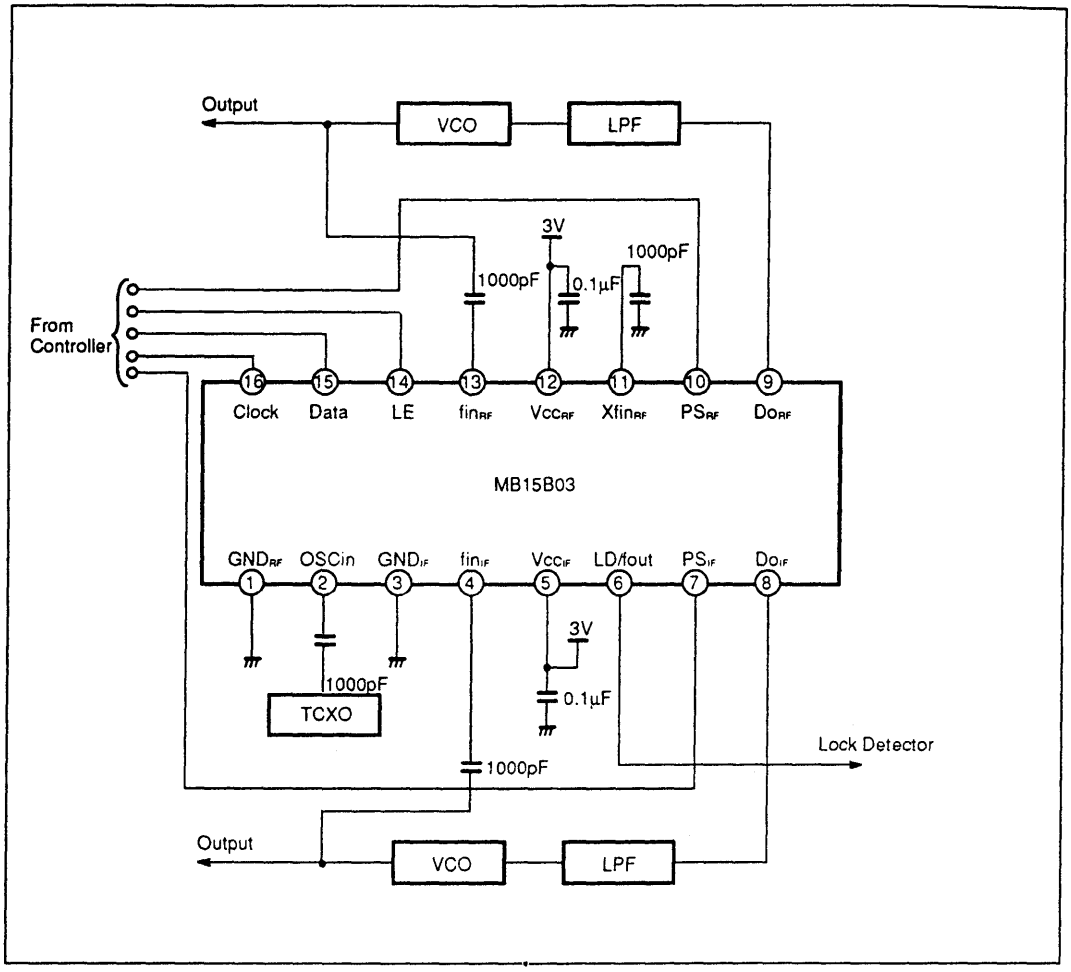
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Input Voltage	Data, Clock, LE, PS	V_{IH}		Vccx0.7+0.4	–	–	V
		V_{IL}		–	–	Vccx0.3–0.4	
Input Current	Data, Clock, LE, PS	I_{IH}		–	–	+1.0	µA
		I_{IL}		–1.0	–	–	
	OSCin	OSCin		–100	–	+100	
Output Voltage	LD	V_{OH}	Vcc = 3.0V, I_{OH} = –1.0mA	2.2	–	–	V
		V_{OL}	Vcc = 3.0V, I_{OL} = 1.0mA	–	–	0.4	
High impedance cutoff current	Do	I_{OFF}		–	–	0.3	µA
Output Current	LD	I_{OH}	Vcc = 3.0V	–1.0	–	–	mA
		I_{OL}	Vcc = 3.0V	–	–	1.0	
	Do	I_{DOH}	Vcc = 3.0V, V_{DOH} = 2.0V, Ta = 25°C	–12	–	–3.5	mA
		I_{DOL}	Vcc = 3.0V, V_{DOL} = 1.0V Ta = 25°C	6	–	18	

4

TEST CIRCUIT (PRESCALER INPUT / PROGRAMMABLE REFERENCE DIVIDER INPUT SENSITIVITY TEST)



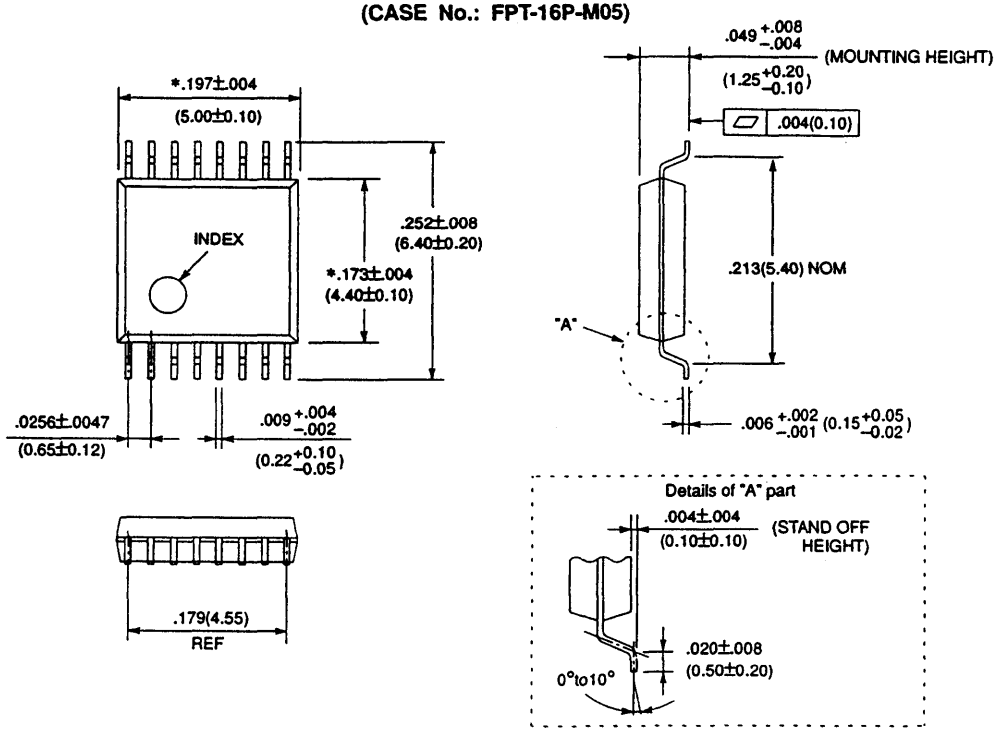
APPLICATION EXAMPLE



Note: Clock, Data, LE : involves a schmitt circuit.
(When inputs are open, pull up/down resistor is necessary to prevent self-oscillation.)

PACKAGE DIMENSION

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

June 1995
Edition 0.1a

FUJITSU

MB15F03 Product Profile Sheet

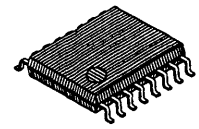
DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

On-chip 2.0GHz & 500MHz PRESCALER

PRELIMINARY

The Fujitsu MB15F03 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2.0GHz and a 500MHz prescalers. A 64/65 or a 128/129 for the 2.0GHz prescaler, and a 16/17 or a 32/33 for 500MHz prescaler can be selected that enables pulse swallow operation.
The latest BiCMOS process technology is used, resulting in a low supply current of 9.0mA typ. at a supply voltage of 3.0V.
Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15F03 is ideally suitable for digital mobile communications, such as PHS (Personal Handy System), PCN (Personal Communication Network) and PCS (Personal Communication Service).

PACKAGE



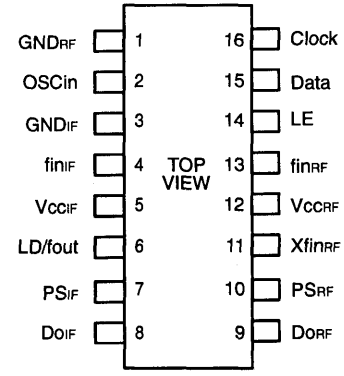
FPT-16P-M05

4

FEATURES

- High frequency operation RF synthesizer : 2.0GHz max.
  IF synthesizer : 500MHz max.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 9.0 mA typ. (Vcc = 3V)
- Power saving function : I_{PS1} = I_{PS2} = 10 µA max. (Vcc = 3V)
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 5 to 2,047
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Wide operating temperature: T_A = –40 to 85°C
- Plastic 16-pin SSOP package (FPT–16P–M05)

PIN ASSIGNMENT

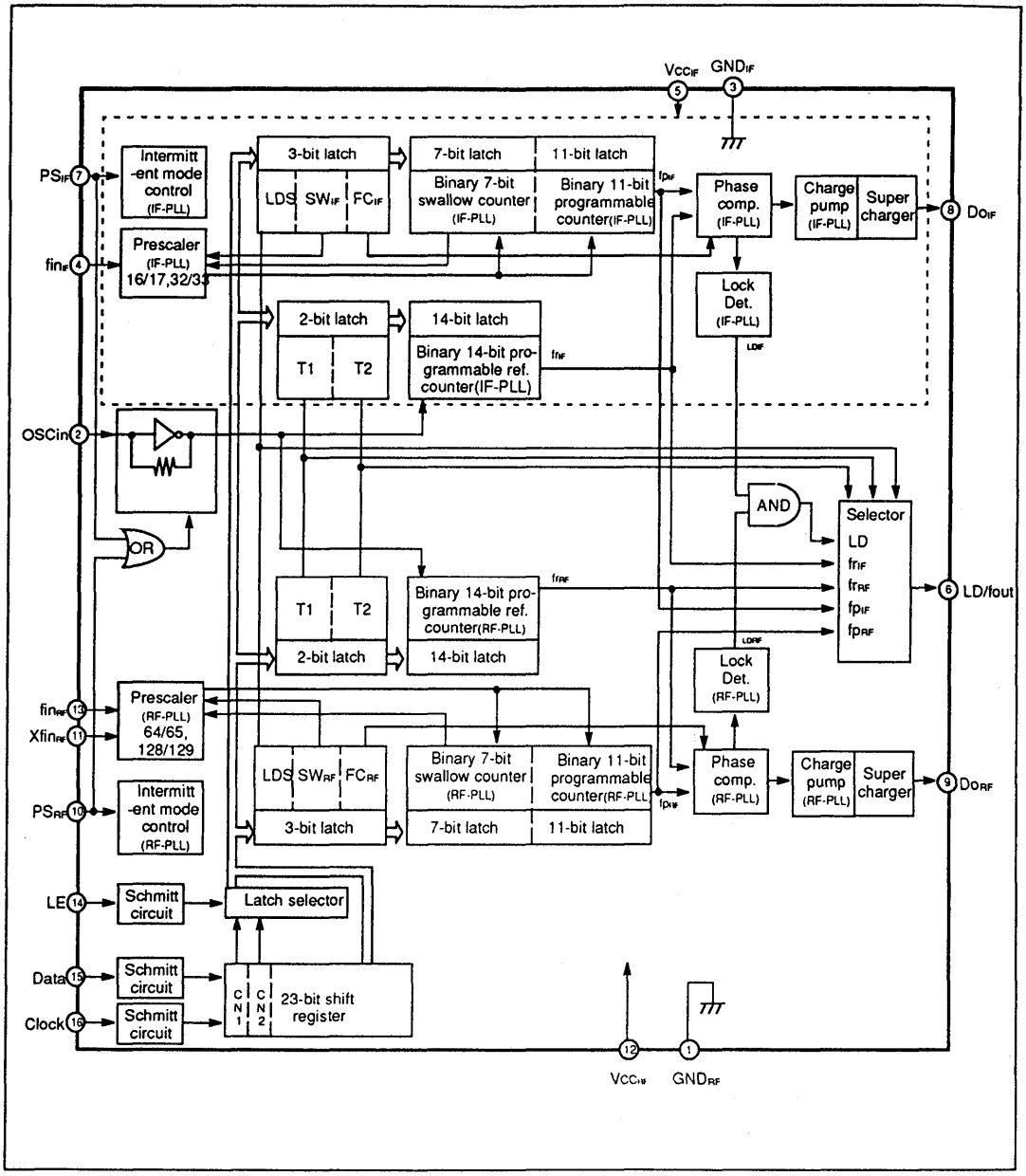


ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Remark	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to 4.0	V
Input Voltage	V_I		–0.5 to V_{CC} +0.5	V
Output Voltage	V_O		–0.5 to V_{CC} +0.5	V
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: *Permanent device damage may occur if the above* **Absolute Maximum Ratings** *are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	GND_{RF}	–	Ground for RF-PLL section.
2	OSCin	I	The programmable reference divider input. TCXO should be connected with a coupling capacitor.
3	GND_{IF}	–	Ground for the IF section.
4	fin_{IF}	I	Prescaler input pin for the IF-PLL. The connection with VCO should be AC coupling.
5	Vcc_{IF}	–	Power supply voltage input pin for the IF-PLL section. When power is OFF, latched data of IF-PLL is cancelled.
6	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout) The output signal is selected by a LDS bit in a serial data. LDS bit = "H" ; outputs fout signal LDS bit = "L" ; outputs LD signal
7	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at "L" at Power–ON. (Open is prohibited.) PS_{IF} = "H" ; Normal mode PS_{IF} = "L" ; Power saving mode
8	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
9	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at "L" at Power–ON. (Open is prohibited.) PS_{RF} = "H" ; Normal mode PS_{RF} = "L" ; Power saving mode
11	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
12	Vcc_{RF}	–	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled.
13	fin_{RF}	I	Prescaler input pin for the RF-PLL. The connection with VCO should be AC coupling.
14	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
15	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-Prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
16	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a riging edge of the clock.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$fvco = \{(P \times N) + A\} \times fosc + R \quad (A < N)$

fvco: Output frequency of external voltage controlled ocillator (VCO)
P: Preset divide ratio of dual modulus prescaler (16 or 32 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
fosc: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)

SERIAL DATA INPUT

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. CONTROL BIT

Control bits		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the IF-PLL.
H	L	The programmable reference counter for the RF-PLL.
L	H	The programmable counter and the swallow counter for the IF-PLL
H	H	The programmable counter and the swallow counter for the RF-PLL

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

CNT1, 2 : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (5 to 16,383) [Table. 2]
T1, 2 : Test purpose bit [Table. 3]

FUNCTIONAL DESCRIPTIONS

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CN1, 2 : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2047) [Table. 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]
SW : Divide ratio setting bit for the prescaler [Table. 6]
(16/17 or 32/33 for the IF-PLL, 64/65 or 128/129 for the RF-PLL)
FC : Phase control bit for the phase detector [Table. 7]
LDS : LD/fout signal select bit [Table. 8]

4

Table2. BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 TEST PURPOSE BIT SETTING

T1	T2	LD/fout pin state
L	L	Outputs $fr_{IF.}$
H	L	Outputs $fr_{RF.}$
L	H	Outputs $fp_{IF.}$
H	H	Outputs $fp_{RF.}$

Table.4 BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note:• Divide ratio less than 5 is prohibited.

Table.5 BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note:• Divide ratio (A) range = 0 to 127

Table. 6 PRESCALER DATA SETTING

		SW = "H"	SW = "L"
Prescaler Divide ratio	IF-PLL	16/17	32/33
	RF-PLL	64/65	128/129

Table. 7 PHASE COMPARATOR PHASE SWITCHING DATA SETTING

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: • Z = High-impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

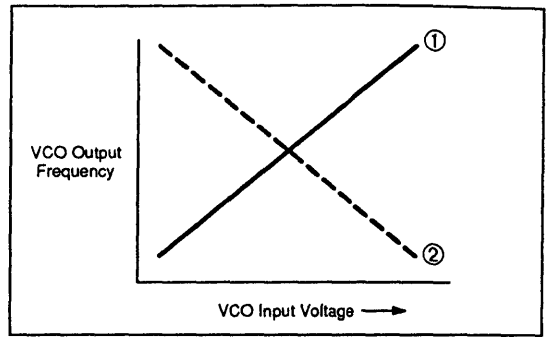
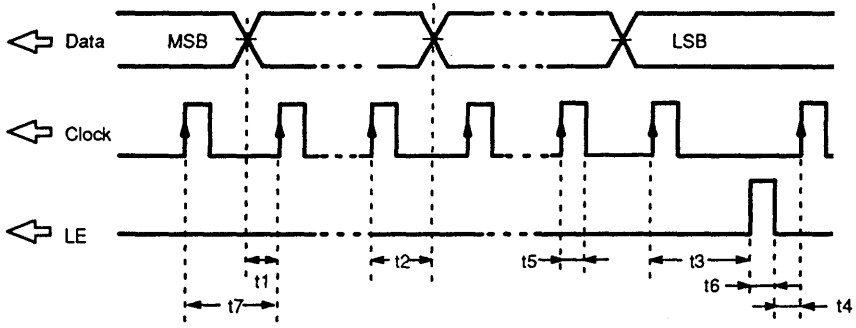


Table. 8 LD/fout OUTPUT SELECT DATA SETTING

LDS	LD/fout output signal
H	fout ($fr_{IF/RF}$, $fp_{IF/RF}$) signals
L	LD signal

SERIAL DATA INPUT TIMING

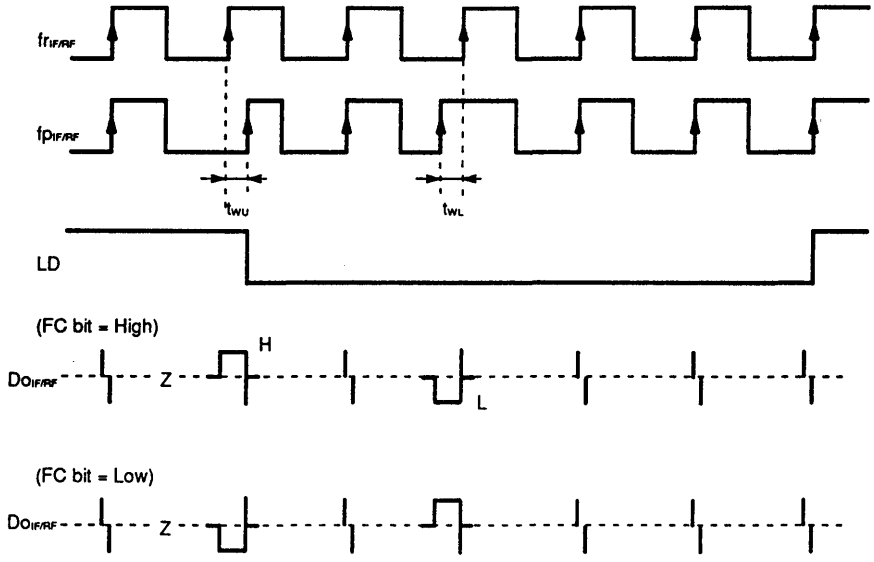


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

PHASE DETECTOR OUTPUT WAVEFORM



LD OUTPUT LOGIC TABLE

IF-PLL section	RF-PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

Note: • Phase error detection range = -2π to $+2\pi$

- Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSCin input frequency as follows.
  $t_{WU} \geq 8/fosc$: i.e. $t_{WU} \geq 625ns$ when foscin = 12.8 MHz
  $t_{WL} \leq 16/fosc$: i.e. $t_{WL} \leq 1250ns$ when foscin = 12.8 MHz

POWER SAVING MODE (INTERMITTENT MODE CONTROL CIRCUIT)

Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL(RF-PLL) enters into power saving mode resultatly current sonsumption can be limited to 10µA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_R) and comparison frequency (f_P) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
PS pin must be set "L" at Power–ON.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10µA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF"s time constant. As a result of this, VCO's frequency is kept at the locking frequency.

PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	Vcc	2.7	3.0	3.6	V	$Vcc_{IF} = Vcc_{RF}$
Input Voltage	Vi	GND	–	Vcc	V	
Operating Temperature	Ta	–40	–	+85	°C	

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current *1		Icc_{IF}	fin_{IF} = 500MHz, fosc = 12MHz	–	3.0	–	mA
		Icc_{RF}	fin_{RF} = 2000MHz, fosc = 12MHz	–	6.0	–	
Power Saving Current *2		Ips_{IF}	Vcc_{IF} current at PS_{IF} ="L"	–	–	10	µA
		Ips_{RF}	Vcc_{RF} current at $PS_{IF/RF}$ ="L"	–	–	10	
Operating Frequency	fin_{IF}	fin_{IF}	IF-PLL	50	–	500	MHz
	fin_{RF}	fin_{RF}	RF-PLL	100	–	2000	
	OSCin	f_{OSC}	min. 500mVp-p	–	12.8	23	
Input Sensitivity	fin_{IF}	$Pfin_{IF}$	IF-PLL, 50Ω termination	–10	–	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF-PLL, 50Ω termination	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	Vcc	mVp-p

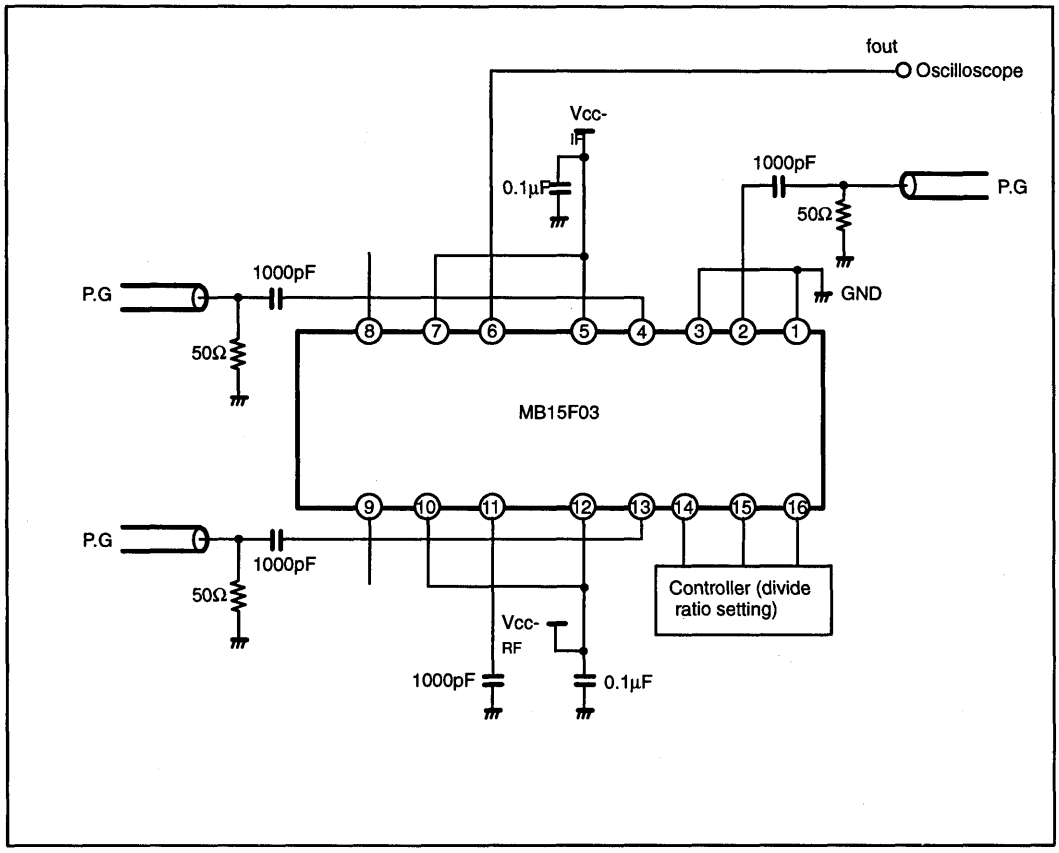
*1: Conditions ; $Vcc_{IF/RF}$ = 3V, Ta = 25°C, in locking state.
*2: Conditions ; $Vcc_{IF/RF}$ = 3V, Ta = 25°C, in power saving state.

ELECTRICAL CHARACTERISTICS

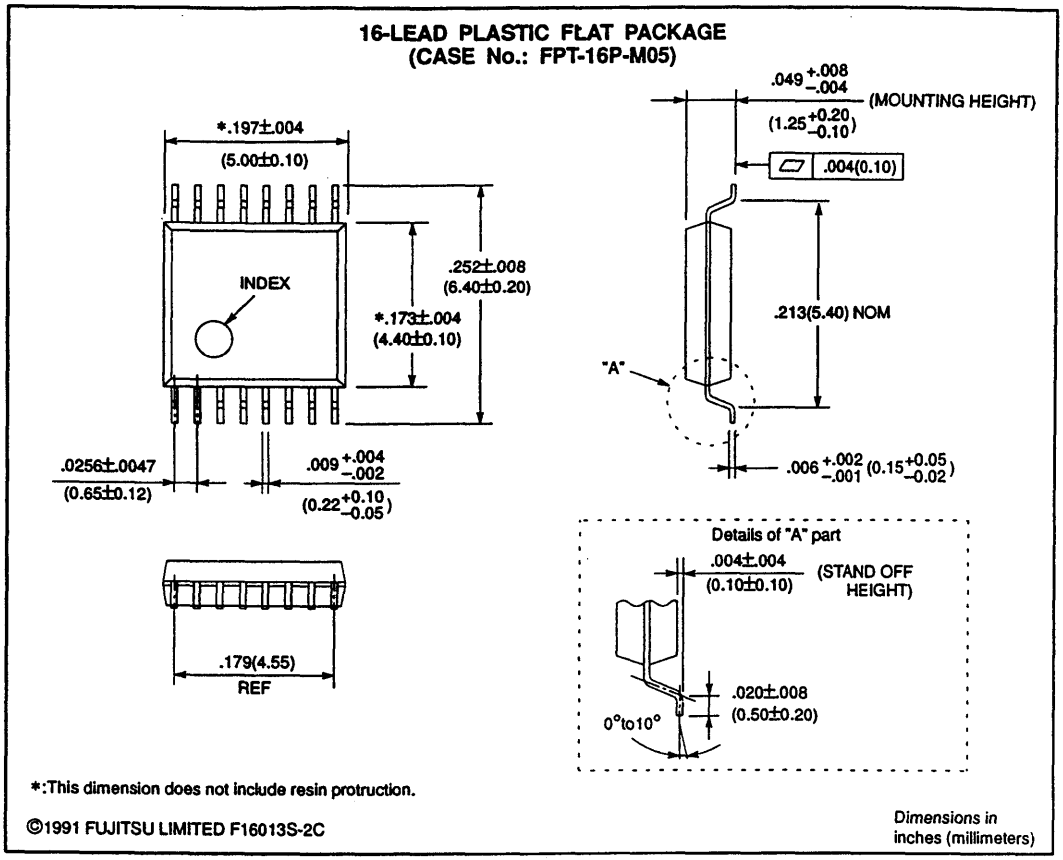
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Input Voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	Vccx0.7+0.4	–	–	V
		V_{IL}	Schmitt trigger input	–	–	Vccx0.3–0.4	
	PS_{IF}, PS_{RF}	V_{IH}		Vccx0.7	–	–	V
		V_{IL}		–	–	Vccx0.3	
Input Current	Data, Clock, LE, PS_{IF}, PS_{RF}	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output Voltage	LD/fout	V_{OH}		Vcc–0.4	–	–	V
		V_{OL}		–	–	0.4	
	DO_{IF}, DO_{RF}	V_{DOH}		Vcc–0.4	–	–	V
		V_{DOL}		–	–	0.4	
High impedance cutoff current	DO_{IF}, DO_{RF}	I_{OFF}		–	–	1.1	µA
Output Current	LD/fout	I_{OH}	Vcc = 3.0V	–	–	–1.0	mA
		I_{OL}	Vcc = 3.0V	1.0	–	–	
	DO_{IF}, DO_{RF}	I_{DOH}	Vcc = 3.0V, V_{DOH} = 2.0V	–	–6.0*1	–	mA
		I_{DOL}	Vcc = 3.0V, V_{DOL} = 1.0V	–	10.0*1	–	

*1: Condition ; Ta = 25°C

TEST CIRCUIT (PRESCALER INPUT / PROGRAMMABLE REFERENCE DIVIDER INPUT SENSITIVITY TEST)



PACKAGE DIMENSION



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0a

FUJITSU

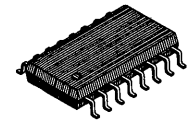
DATA SHEET

MB1503

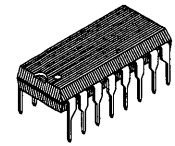
LOW-POWER PLL FREQUENCY SYNTHESIZER WITH POWER SAVE FUNCTION (1.1GHZ)

4

The Fujitsu MB1503 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. A stand-by mode is provided to limit power consumption during intermittent operation.
The MB1503 is configured of a 1.1GHz dual-modulus prescaler with 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter), analog switches, and an intermittent operation control circuit that selects the operating or stand-by mode depending on the power-save control input state (PS).
The MB1503 operates from a single +5 V supply. Fujitsu's advanced technology achieves an Icc of 8mA, typical. The stand-by mode current consumption is just 100µA.



PLASTIC PACKAGE
(FPT-16P-M06)



PLASTIC PACKAGE
(DIP-16P-M04)

Features

- High operating frequency : f_{IN} = 1.1GHz (P_{IN} = –10dBm)
- Pulse-swallow function : High-speed dual-modulus prescaler with 128/129 divide ratio
- Low supply current : I_{CC} = 8mA typ. at 5V
- Power-saving stand-by mode : 100µA
- Serial input, 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter : 0 to 127
  - Binary 11-bit programmable counter: 16 to 2,047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 15-bit programmable reference counter: 8 to 16,383
  - 1-bit switch counter sets prescaler divide ratio
- On-chip analog switch for fast lock-up
- On-chip charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16–pin dual inline package (Suffix : –P)
  Plastic 16–pin small outline package (Suffix : –PF)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

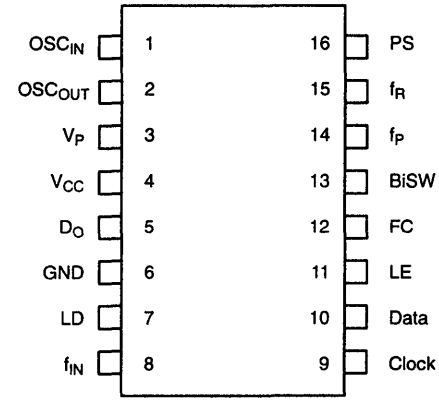
Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	$V_{CC} \le V_P \le 10.0$	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

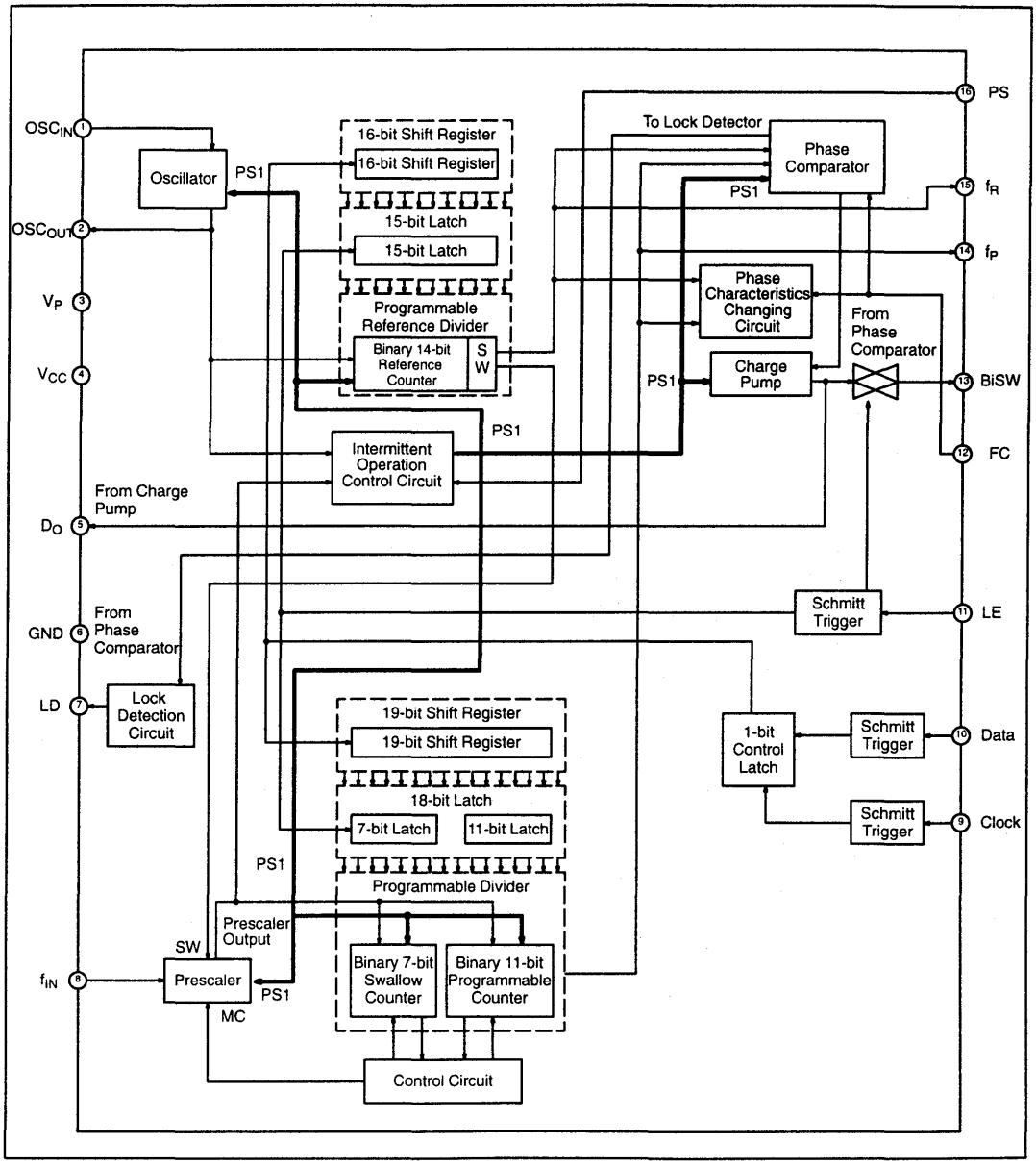
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT

(TOP VIEW)



BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input An external crystal is connected to this pin.
2	OSC_{OUT}	O	Oscillator output An external crystal is connected to this pin.
3	V_P	–	Power supply input for charge pump and analog switch
4	V_{CC}	–	Power supply
5	D_O	O	Charge pump output The phase of the charge pump is reversed depending on the FC input.
6	GND	–	Ground
7	LD	O	Phase comparator output The output level is high when LD is locked. The output level is low when LD is unlocked.
8	f_{IN}	I	Prescaler input Connection with an external VCO should be done by AC coupling.
9	Clock	I	Clock input for 19-bit and 16-bit shift registers Data is shifted into the shift register on the rising edge of the clock.The Schmitt trigger is contained.
10	Data	I	Serial data input using binary code The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 15-bit latch. When it is low, data is transmitted to the 18-bit latch.The Schmitt trigger input is involved.
11	LE	I	Load enable signal input When LE is high, the data of the shift register are transferred to a latch, depending on the control bit in the serial data. At the same time, an internal analog switch turns on and the output of the internal charge pump is connected to the BiSW pin.The Schmitt trigger input is involved.
12	FC	I	Phase select input of phase comparator (with internal pull-up resistor) When FC is low, the characteristics of the charge pump and phase comparator are reversed. The FC input signal is also used to control the f_{OUT} pin (test pin) of f_R or f_P.
13	BiSW	O	Analog switch output BiSW is usually in the high-impedance state. When the switch is turned on (LE is high), the state of the internal charge pump is output.
14	f_P	O	Monitor pin of programmable counter output
15	f_R	O	Monitor pin of reference counter output
16	PS	I	Power save signal input Set PS low while the system is powered (never use pin 16 as it is opened) PS = High : Operation mode PS = Low : Stand-by mode

FUNCTIONAL DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)
- M : Preset divide ratio of modules prescaler (128)

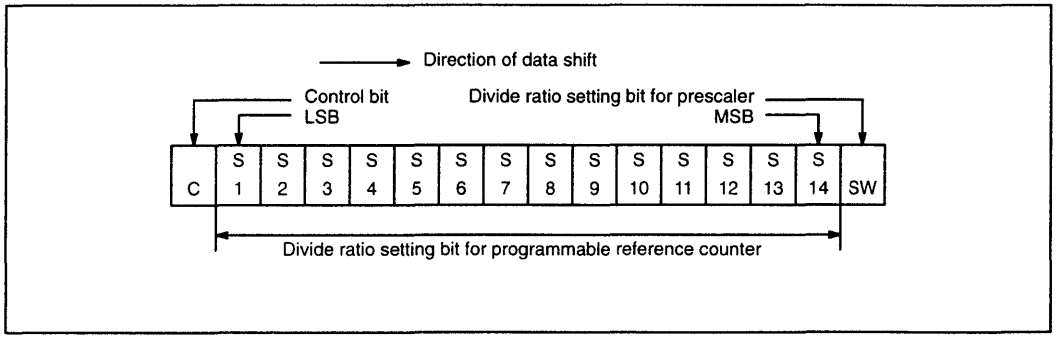
4

Serial data input

Serial data is input using the Data, Clock, and LE pins. Serial data controls the 15-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is input to the Data pin.
One bit of data is shifted into the internal shift registers on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	15-bit latch
L	18-bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 15-bit latch and a 14-bit reference counter. The serial 16-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

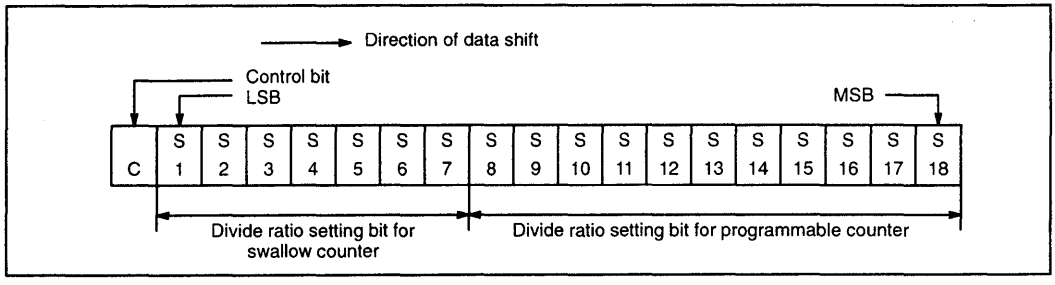
Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 8 to 16,383)

Notes: 1. Divide ratios less than 8 are prohibited
2. SW: This bit selects the divide ratio of the prescaler
   SW Low: 128 or 129 (SW must be always be low)
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (8 to 16,383)
4. C: Control bit: Set high
5. Input MSB data first

(b) Programmable divider divide ratio

The programmable divider consists of a 19-bit shift register, 18-bit latch, 7-bit swallow counter, and 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

- 11-bit programmable counter divide ratio

Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

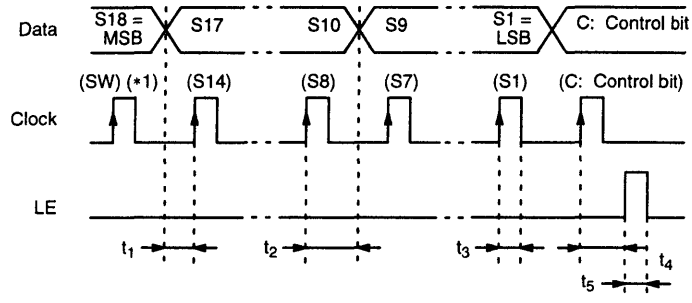
(Divide ratio = 16 to 2,047)

4

Notes: 1. Divide ratios less than 16 are prohibited for the 11–bit programmable counter
2. S1 to S7: These bits select the divide ratio of the swallow counter (0 to 127)
3. S8 to S18: These bits select the divide ratio of the programmable counter (16 to 2,047)
4. C: Control bit: (Set low)
5. Input MSB data first

Serial data input timing

- t_1 (≥ 1µs) : Data setup time t_2 (≥ 1µs) : Data hold time t_3 (≥ 1µs) : Clock pulse width
  t_4 (≥ 1µs) : LE setup time to the rising edge of last clock t_5 (≥ 1µs) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Intermittent operation

Intermittent operation limits power consumption by shutting down or starting the internal circuits according to their necessity. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost.
To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting the phase of both frequencies to limit the error signal output. This is done by the PS control circuit. If PS is set high, the circuit enters the operating mode. If PS is set low, operation stops and the device enters the stand-by mode. Each mode is explained below:

- Operating mode (PS =High Level)
  All circuits are operating, and PLL operation is normal.

- Stand-by mode (PS = Low level)
  Circuits that do not affect operation are powered down to limit current consumption.
  The current in the power save state is typically 100μA.
  At this time, the levels of D_O and LD are the same as when the PLL is locked.
  Since D_O is placed in the high-impedance state and the input voltage of the voltage controlled oscillator (VCO) is set to the voltage in the operating mode (when locked) by the time constant of the low-pass filter, the frequency output from the VCO (f_{VCO}) is kept at the locking frequency.

The operating and stand-by modes alternate repeatedly. This intermittent operation limits the error signal by forcibly correcting the phase of the reference and comparison frequencies to limit power consumption.
The device must be set in the stand-by mode (PS = low) when it is powered up.

Relationship between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. The internal charge pump output level (D_O) is reversed, depending on the FC pin input level. The relationship between the FC input level and D_O is shown below:

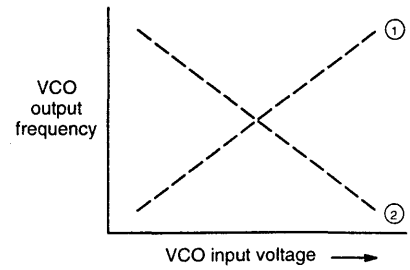
	FC = High or open	FC = Low
$f_R > f_P$	H	L
$f_R < f_P$	L	H
$f_R = f_P$	Z (*1)	Z (*1)

*1: High impedance

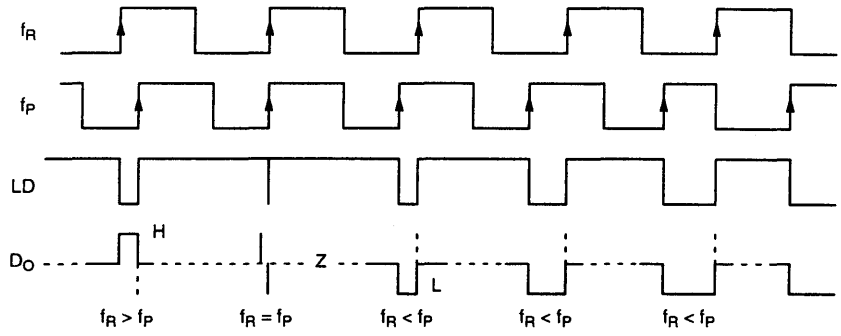
When designing a synthesizer, the FC pin setting depends on the VCO characteristics.

*: When the VCO characteristics are similar to ①, set FC high or open.

*: When the VCO characteristics are similar to ②, set FC low.



Phase comparator output waveform (FC = High)



Notes: 1. Phase difference detection range: -2π to $+2\pi$
2. Spike appearance depends on the charge pump characteristics. Also, the spike is output to diminish dead band.
3. When $f_R > f_P$ or $f_R < f_P$, a spike might not appear depending on the charge pump characteristics.
4. LD is low when the phase difference is tw or more. LD is high when the phase difference is tw or less for three or more cycles (when f_{OSCIN} = 12.8MHz, tw = 625 to 1,250ns).

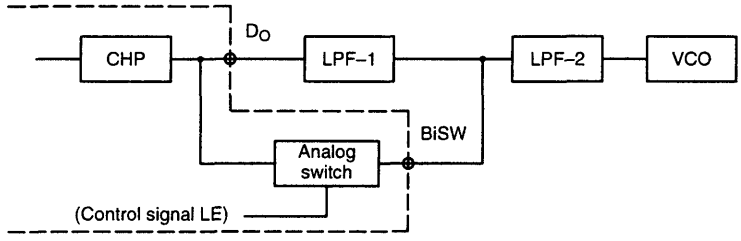
4

Analog switch

The LE signal turns the analog switch on or off. When the analog switch is turned on, the charge pump output (D_O) is output through the BiSW pin. When it is turned off, the BiSW pin is in the high-impedance state.

When LE = high (when the divide ratio of the internal divider is changed): Analog switch = on
When LE = low (normal operating mode): Analog switch = off

The LPF time constant can be decreased by inserting an analog switch between LPF1 and LPF2. This decreases the lock-up time when the PLL channel is changed.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	$V_{CC} \leq V_P \leq 8.0$			V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	–40	–	+85	°C

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

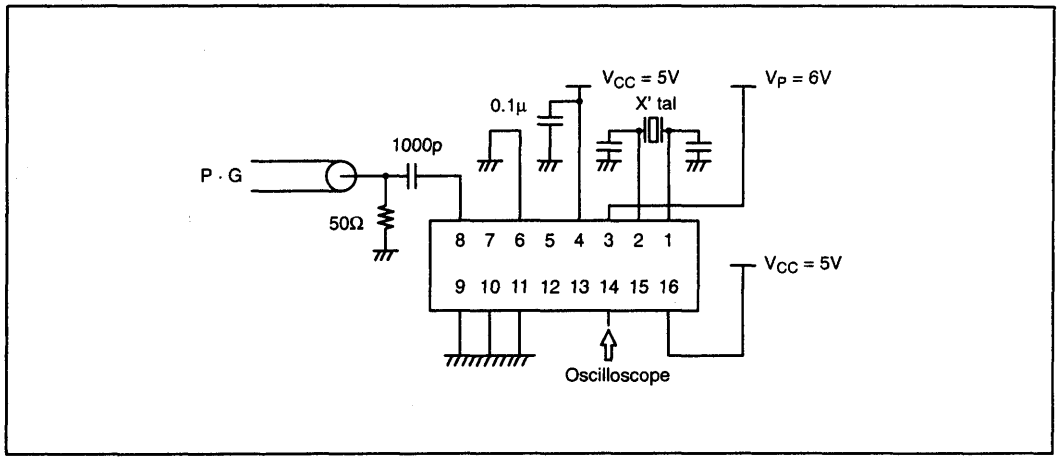
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device a socket.
- Protect leads with conductive sheet, as treatment (transport) a board mounted the device.

ELECTRICAL CHARACTERISTICS

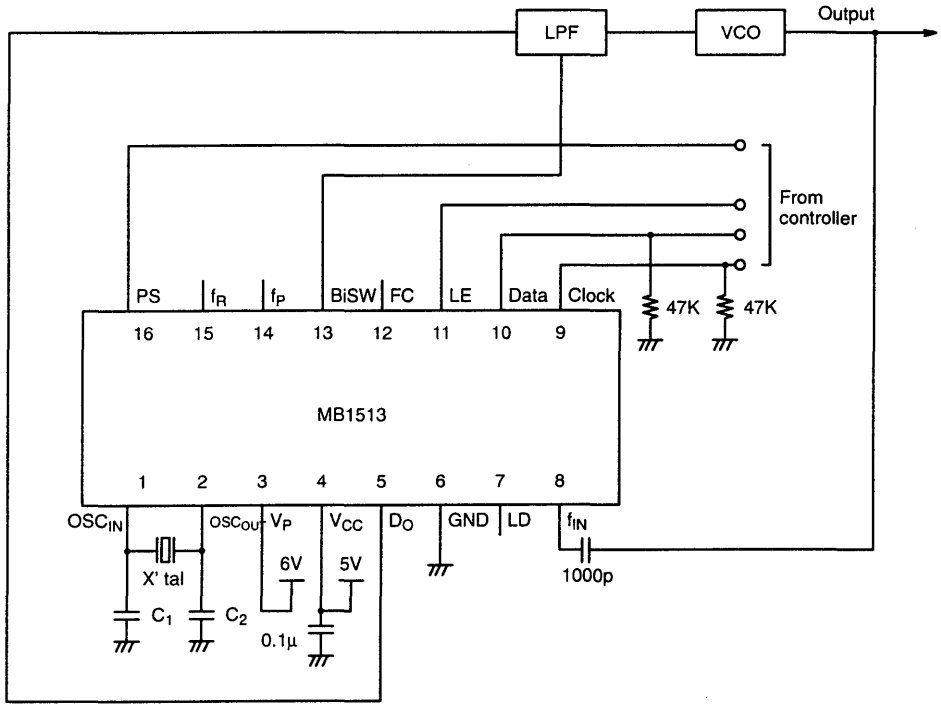
Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply Current		I_{CC}	–	8.0	12.0	mA	With f_{IN} = 1.1GHz, OSC_{IN} = 12MHz, V_{CC} = 5.0V. Inputs are V_{CC} and outputs are open.
Stand-by Current		IPS	–	100	–	μA	With f_{IN} = 1.1GHz, OSC_{IN} = 12MHz, V_{CC} = 5.0V. The PS pin is grounded, remaining inputs are at V_{CC}, and outputs are open.
Operating Frequency	f_{IN}	f_{IN}	10	–	1100	MHz	AC coupling. The minimum operating frequency is measured with a 100pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	20	MHz	—
Input Sensitivity	f_{IN}	$P_{f\,IN}$	–10	–	6	dBm	—
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	—
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7	–	–	V	—
Low-level Input Voltage		V_{IL}	–	–	V_{CC} x 0.3	V	—
High-level Input Current	Data, Clock, LE	I_{IH}	–	1.0	–	μA	—
Low-level Input Current		I_{IL}	–	–1.0	–	μA	—
	FC	I_{FC}	–	–60	–	μA	—
Input Current	OSC_{IN}	I_{OSC}	–	±50	–	μA	—
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	4.4	–	–	V	V_{CC} = 5V
Low-level Output Voltage		V_{OL}	–	–	0.4	V	—
High-impedance Cut off Current	D_O	I_{OFF}	–	–	1.1	μA	V_{DO} = GND to 8V $V_{CC} \leq V_P \leq 8V$
Output Current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	—
		I_{OL}	1.0	–	–	mA	—
Analog Switch ON Resistance		R_{ON}	–	25	–	Ω	—

4

TEST CIRCUIT
(FOR MEASURING PRESCALER INPUT SENSITIVITY)



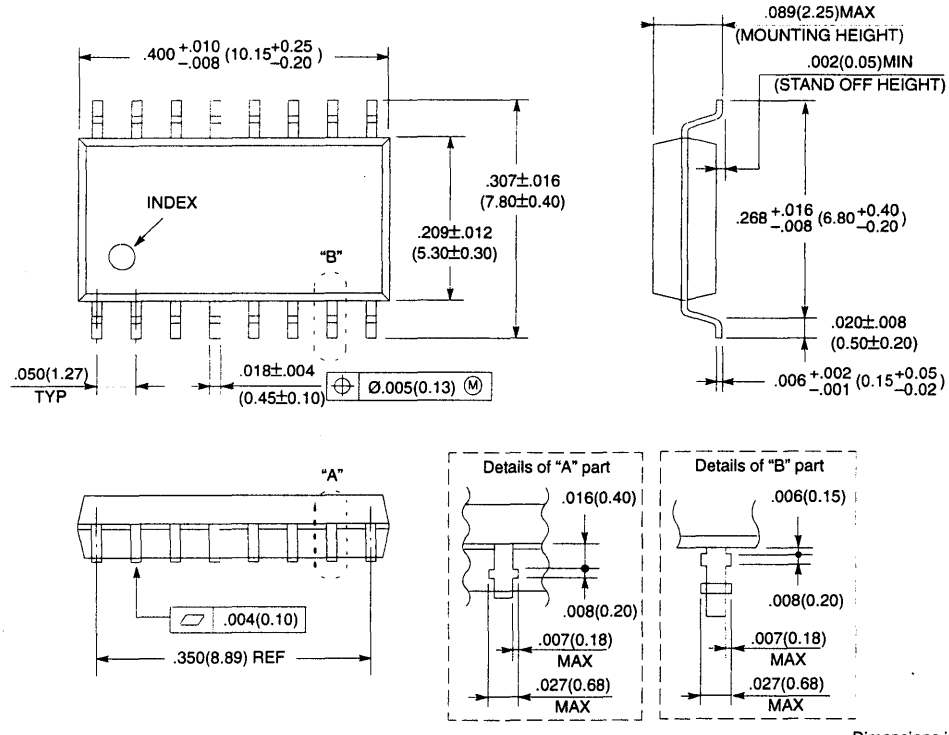
APPLICATION EXAMPLE



V_P, V_{PX} : Maximum 8V
C_1, C_2 : Depends on the crystal parameters

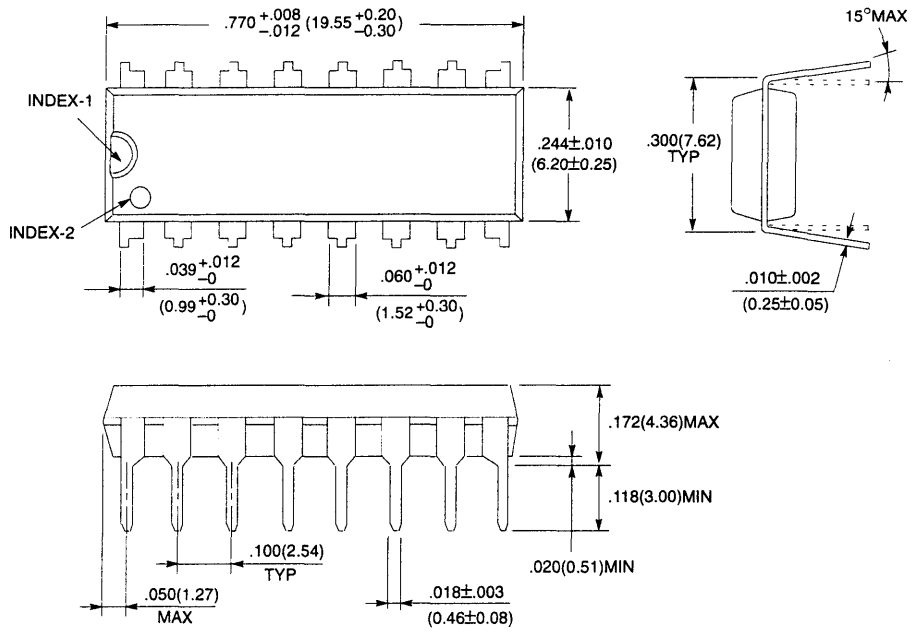
PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

DS04–21301–5E

FUJITSU

DATA SHEET

MB1504/MB1504H/MB1504L

ASSP SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 520MHz PRESCALER

The Fujitsu MB1504/MB1504H/MB1504L, utilizing BI-CMOS technology, is a single chip serial input PLL frequency synthesizer with pulse-swallow function.

The MB1504 series contains a 520MHz two modulus prescaler that can select either 32/33 or 64/65 divide ratio; control signal generator; 16-bit shift register; 15-bit latch; programmable reference divider (binary 14-bit programmable reference counter); 1-bit switch counter; phase comparator with phase inverse function; charge pump; crystal oscillator; 19-bit shift register; 18-bit latch; and a programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).

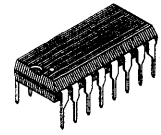
The MB1504 operates from a low supply voltage (3V typ) and consumes low power (30mW at 520MHz).

MB1504 Product Line

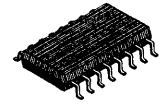
	V_P Voltage	V_{OOP} Voltage	Lock up Time	D_O Output Width	High-level Output Current	Low-level Output Current
MB1504	8V max	8.5V max	Middle speed	Middle	Middle	Middle
MB1504H	10V max	10.0V max	High speed	Low	High	Low
MB1504L	8V max	8.5V max	Low speed	High	Low	High

FEATURES

- High operating frequency: $f_{IN\ MAX}$=520MHz ($V_{IN\ MIN}$=0.20V_{P-P})
- On-chip prescaler
- Low power supply voltage: 2.7V to 5.5V (3.0V typ)
- Low power supply consumption: 30mW (3.0V, 520MHz operation)
- Serial input 18-bit programmable divider consisting of:
  –Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  –Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Serial input 15-bit programmable reference divider consisting of:
  –Binary 14-bit programmable reference counter (Divide ratio: 8 to 16383)
  –1-bit switch counter (SW) Sets divide ratio of prescaler
- 2 types of phase detector output
  –On-chip charge pump (Bipolar type)
  –Output for external charge pump
- Wide operating temperature: T_A=–40°C to +85°C



PLASTIC PACKAGE
DIP-16P-M04

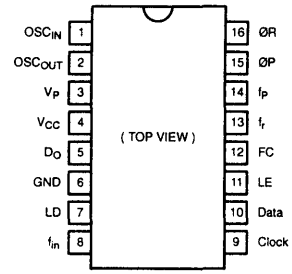


PLASTIC PACKAGE
FPT-16P-M06

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

PIN ASSIGNMENT

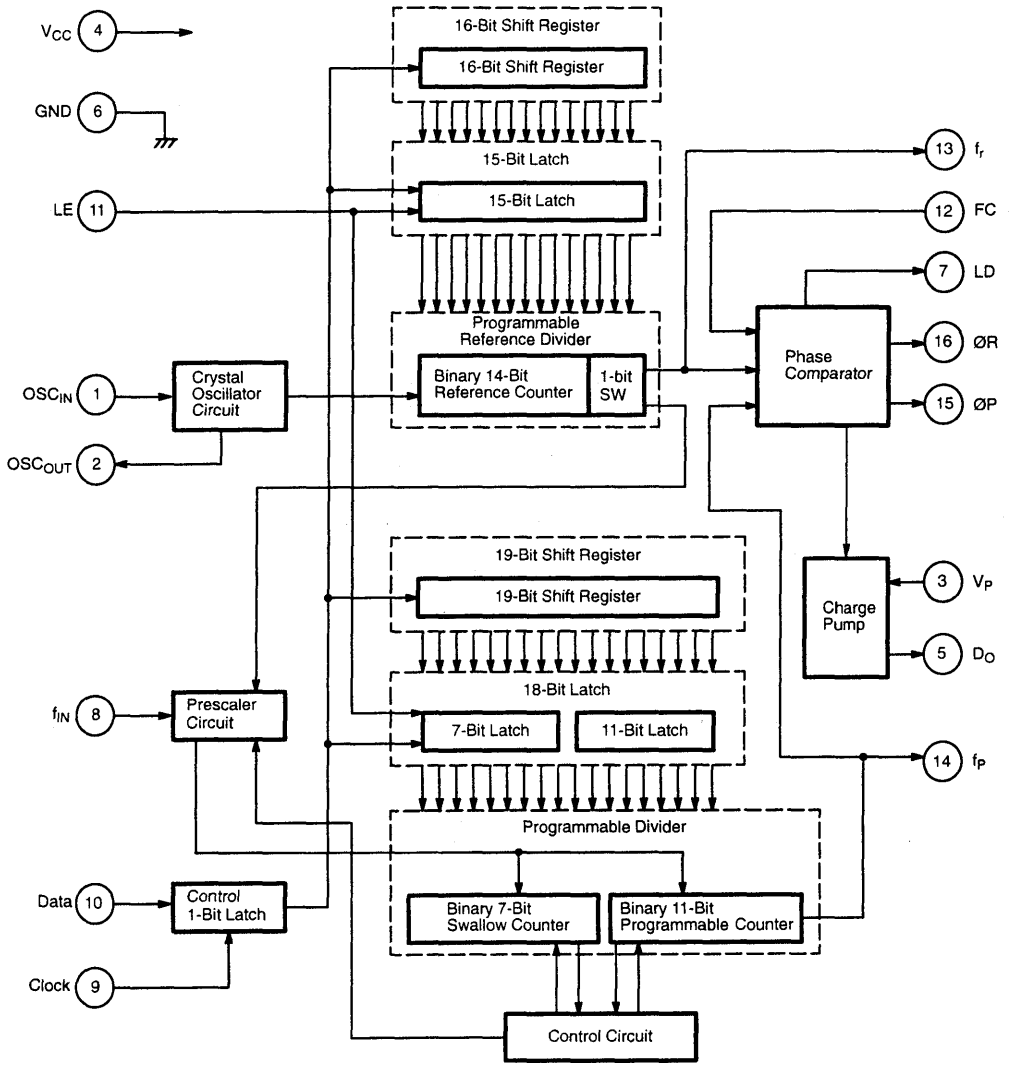


ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}	—	−0.5 to +7.0	V
	V_{PH}	MB1504H	V_{CC} to 12.0	V
	V_P,V_{PL}	MB1504/1504L	V_{CC} to 10.0	
Output Voltage	V_{OUT}	—	−0.5 to V_{CC} +0.5	V
Open-drain Output	V_{OOPH}	MB1504H	−0.5 to 11.0	V
	V_{OOP},V_{OOPL}	MB1504/1504L	−0.5 to 9.0	
Output Current	I_{OUT}	—	+10	mA
Storage Temperature	T_{STG}	—	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB1504/MB1504H/MB1504L BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input Oscillator output A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump
4	V_{CC}	—	Power supply voltage input
5	D_O	O	Charge pump output The phase characteristics can be inversed depending upon the FC input.
6	GND	—	Ground
7	LD	O	Phase comparator output This pin outputs high when the phase is locked. While the phase difference of f_r and f_p exists, the output level goes low.
8	f_{IN}	I	Prescaler input The connection with an external VCO should be an AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Serial data of binary code input The last bit of the data is a control bit. The last data bit specifies which latch is activated. When the last bit is high level and LE is high-level, data is transferred to the 15-bit latch. When the last bit is low level and LE is high level, data is transferred to the 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor) When LE is high level (or open), data stored in the shift register is transferred to the latch depending on the control data.
12	FC	O	Phase selecting input of phase comparator (with internal pull up resistor) When FC is low level, the charge pump and phase detector characteristics can be inversed.
13	f_r	O	Monitor pin of phase comparator input It is the same as the programmable reference divider output.
14	f_P	O	Monitor pin of phase comparator input It is the same as the programmable divider output.
15 16	ØP ØR	O O	Outputs for external charge pump The phase characteristics can be inversed depending on the FC input. The ØP pin is an N-channel open-drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is input using the Data pin, Clock pin and LE pin. The 15-bit programmable reference divider and 18-bit programmable divider are controlled, respectively.

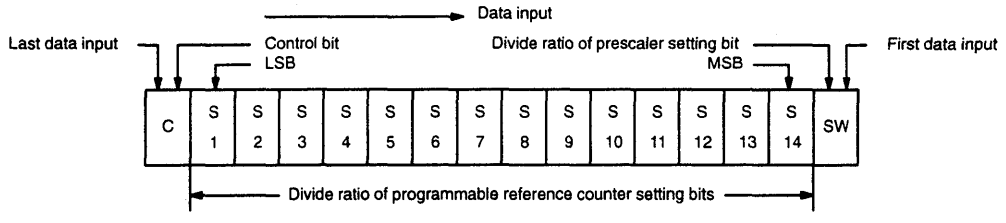
On rising edge of the clock, one bit of the data shifts into the internal shift registers.

When load enable (LE) is high level (or open), data stored in the shift registers is transferred to the 15-bit latch or 18-bit latch depending upon the control bit level.

Control data "H" : Data is transferred into the 15-bit latch.
Control data "L" : Data is transferred into the 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

The programmable reference divider consists of a 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



◎ 14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

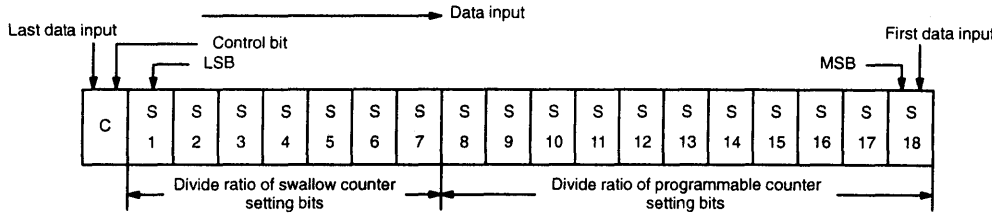
Divide ratio less than 8 is prohibited
Divide ratio R: 8 to 16383

SW: Divide ratio of prescaler setting bit
SW="H": 32
SW="L": 64
S_1 to S_{14}: Divide ratio of programmable reference counter setting bits (8 to 16383)
C: Control bit (control bit is set to high)

FUNCTIONAL DESCRIPTIONS

PROGRAMMABLE DIVIDER

The programmable divider consists of a 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown below.



◎ 7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
63	0	1	1	1	1	1	1

Divide ratio A : 0 to 63

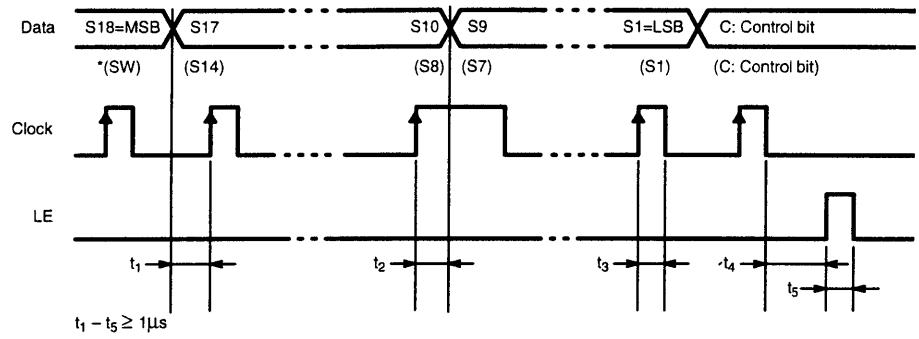
◎ 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Divide ratio less than 16 is prohibited
Divide ratio N : 16 to 2047

S_8 to S_{18} : Divide ratio of programmable counter setting bits (16 to 2047)
S_1 to S_7 : Divide ratio of swallow counter setting bits (0 to 127)
C: Control bit (control bit is set to low)
Data is input from the MSB.

SERIAL DATA INPUT TIMING



On the rising edge of the clock, one bit of the data shifts into the shift registers.
Data in ( ) is used for setting the divide ratio of the programmable reference divider.

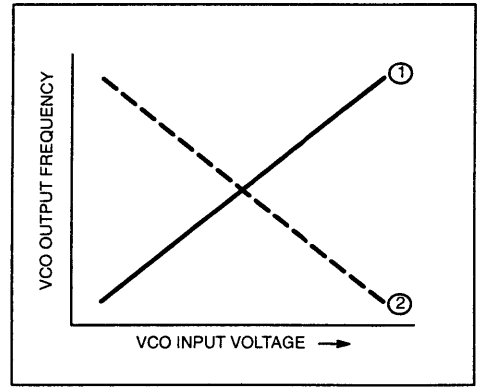
PHASE CHARACTERISTICS

The FC pin (pin 12) is provided to inverse the phase comparator characteristics. The characteristics of the internal charge pump output (D_O), and phase detector outputs (ØR, ØP) can be inversed depending upon the FC input data. Outputs are shown below.

	FC=H (or open)			FC=L		
	D_O	ØR	ØP	D_O	ØR	ØP
$f_r > f_p$	H	L	L	L	H	Z
$f_r < f_p$	L	H	Z	H	L	L
$f_r = f_p$	Z	L	Z	Z	L	Z

Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set high or open circuit;
When VCO characteristics are like ②, FC should be set Low.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}	—	2.7	3.0	5.5	V
	V_{PH}	MB1504H	V_{CC}	—	10.0	V
	V_P, V_{PL}	MB1504 MB1504L	V_{CC}	—	8.5	
Open-drain Output	V_{OOPH}	MB1504H	V_{CC}	—	10.0	V
	V_{OOP}, V_{OOPL}	MB1504 MB1504L	V_{CC}	—	8.5	
Input Voltage	V_{IN}	—	GND	—	V_{CC}	V
Operating Temperature	T_A	—	−40	—	+85	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

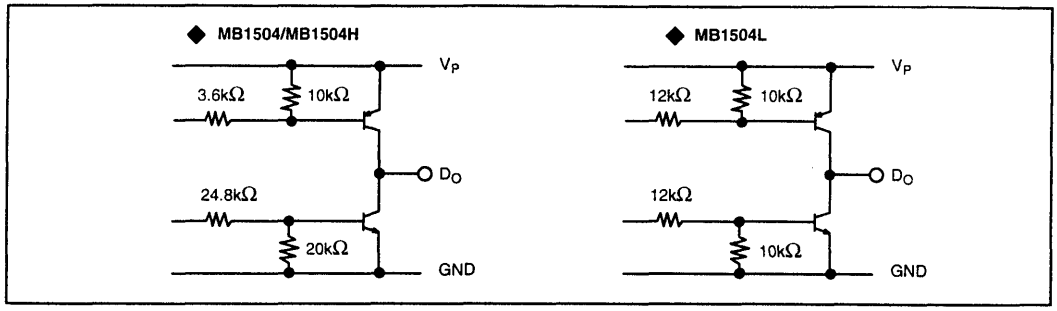
(V_{CC}=2.7 to 5.5V, T_A=–40 to +85°C)

Parameter	Pin Name	Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	V_{CC}	I_{CC}	*1	—	10	16	mA
Operating Frequency	f_{IN}	f_{IN}	*2	10	—	520	MHz
	OSC_{IN}	f_{OSC}		—	12	20	MHz
Input Sensitivity	f_{IN}	$Pf_{IN}1$	V_{CC}=2.7 to 4.0V	–10	—	6	dBm
		$Pf_{IN}2$	V_{CC}=4.0 to 5.5V	–4	—	6	dBm
	OSC_{IN}	V_{IN}	—	0.5	—	—	V_{P-P}
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	—	0.7xV_{CC}	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	0.3xV_{CC}	V
High-level Input Current	Data, Clock	I_{IH}	—	—	1.0	—	µA
Low-level Input Current		I_{IL}	—	—	–1.0	—	µA
Input Current	OSC_{IN}	I_{IN}	—	—	±50	—	µA
	LE, FC	I_{LE}	—	—	–60	—	µA
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=3.0V	2.4	—	—	V
Low-level Output Voltage		V_{OL}		—	—	0.4	V
N-channel Open-drain Cutoff Current	ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$	—	—	1.1	µA
High-level Output Current	Except D_O and OSC_{OUT}	I_{OH}	—	–1.0	—	—	mA
Low-level Output Current		I_{OL}	—	1.0	—	—	mA
High-level Output Current	D_O	I_{DOHH}	MB1504H, V_{CC}=3V, V_P=12V, T_A=+25°C	–2.2	–4.5	—	mA
		I_{DOH}	MB1504, V_{CC}=3V, V_P=6V, T_A=+25°C	–0.5	–2.0	—	mA
		I_{DOHL}	MB1504L, V_{CC}=3V, V_P=6V, T_A=+25°C	–0.5	–1.1	–2.2	mA
Low-level Output Current		I_{DOLH}	MB1504H, V_{CC}=3V, V_P=12V, T_A=+25°C	2.2	6.0	—	mA
		I_{DOL}	MB1504, V_{CC}=3V, V_P=6V, T_A=+25°C	1.5	6.0	—	mA
		I_{DOLL}	MB1504L, V_{CC}=3V, V_P=6V, T_A=+25°C	4.5	12.0	—	mA
Leakage Current	D_O, ØP	I_{DOZ}	V_{CC}=3V, V_P=12V, T_A=+25°C	—		1.0	µA

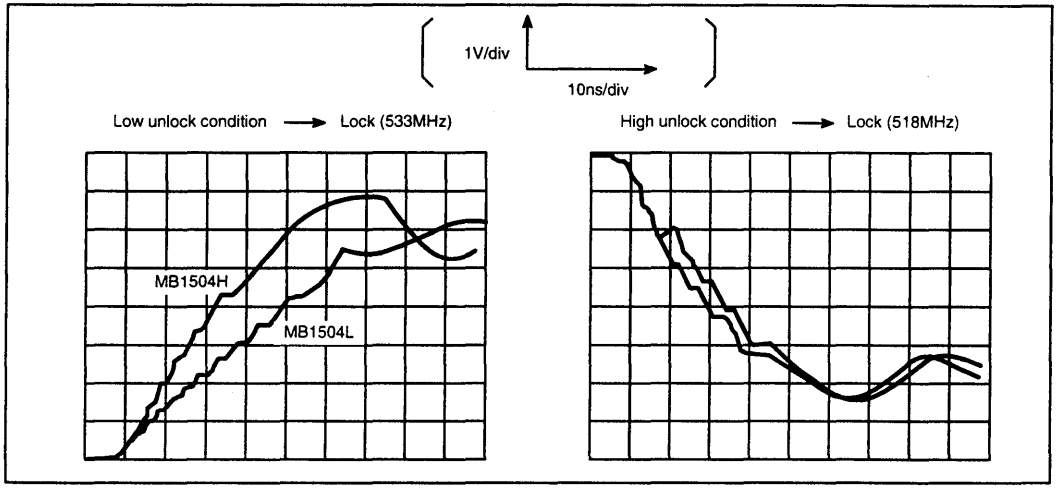
Note: *1 V_{CC}=3.0V, f_{IN}=520MHz, f_{OSC}=12MHz crystal.
Inputs are grounded except f_{IN}, and outputs are open.
*2 Input coupling capacitor 1000pF is connected.

TYPICAL CHARACTERISTICS CURVES

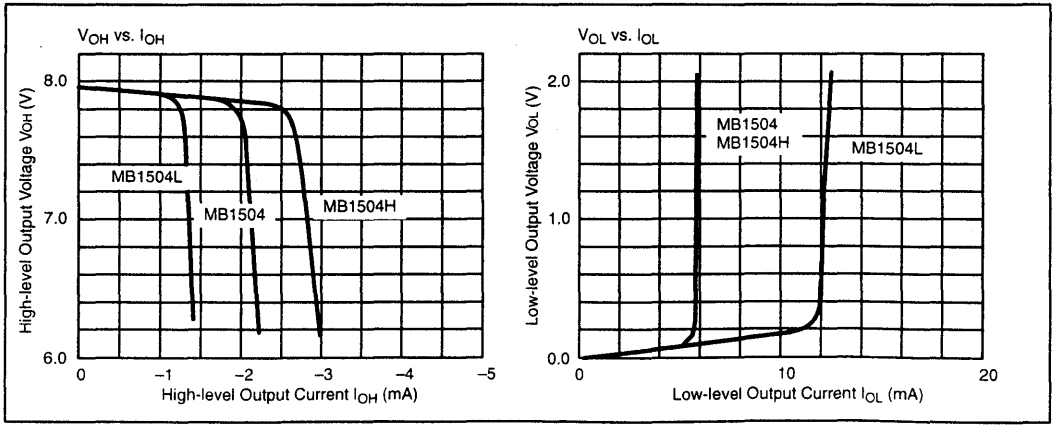
CHARGE PUMP CHARACTERISTICS



LOCK UP TIME MEASUREMENT



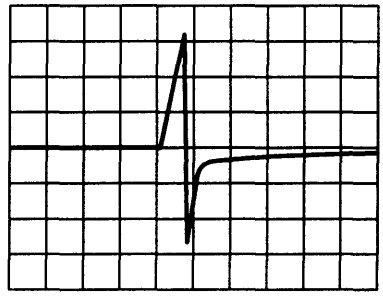
DO PIN OUTPUT CURRENT CURVES (TYPICAL)



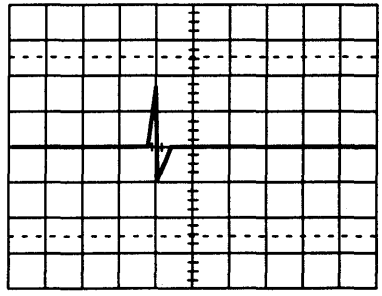
D_O PIN OUTPUT WAVEFORM AT LOCK CONDITION

Output Waveform

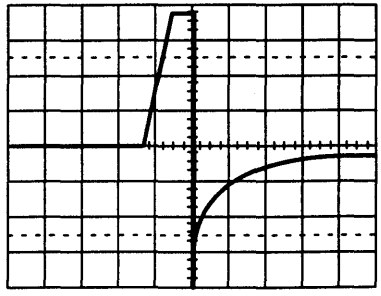
MB1504



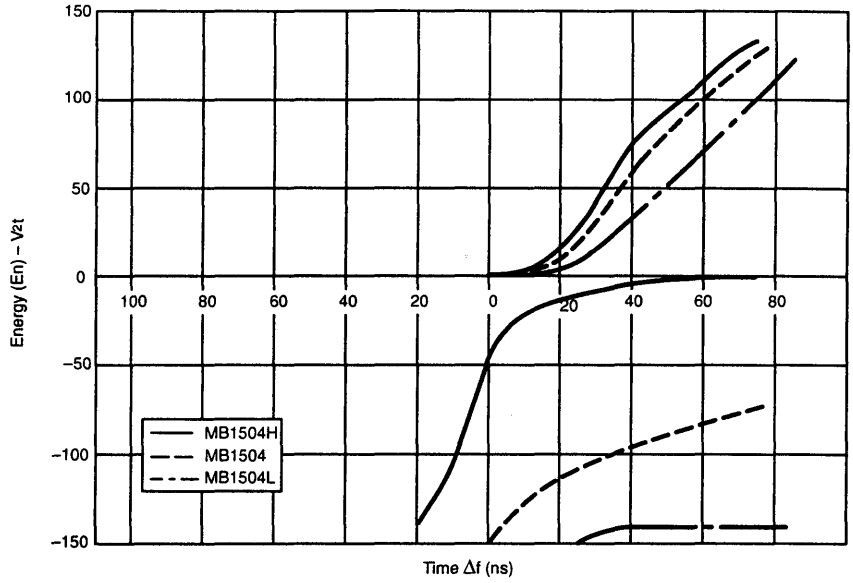
MB1504H

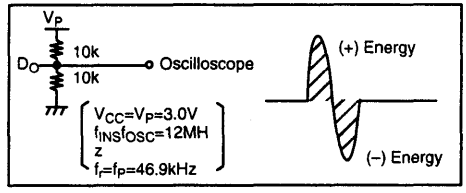


MB1504L



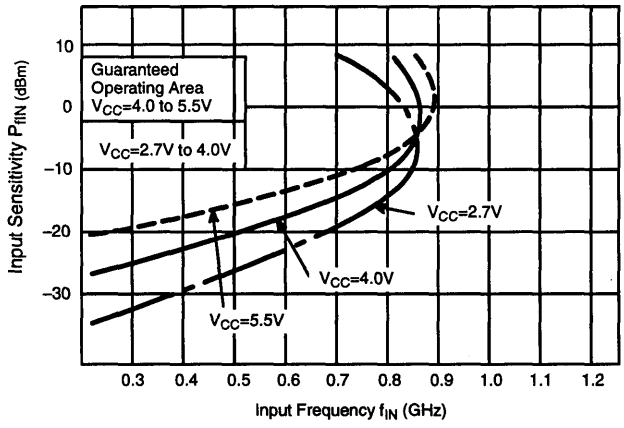
PHASE CHARACTERISTICS (Δf vs. D_O OUTPUT ENERGY)

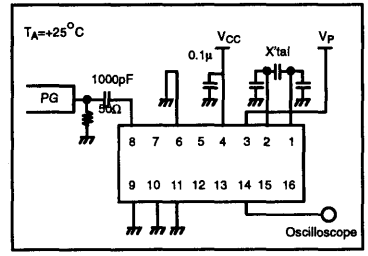




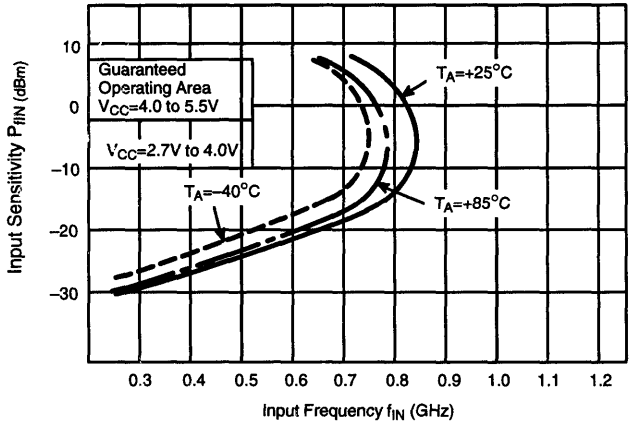
INPUT SENSITIVITY

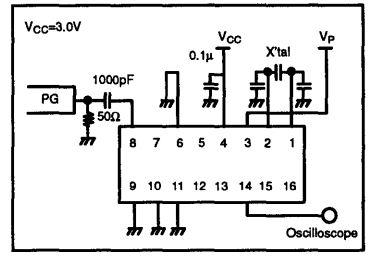
Input Sensitivity vs. Input Frequency (Supply Voltage Dependence)



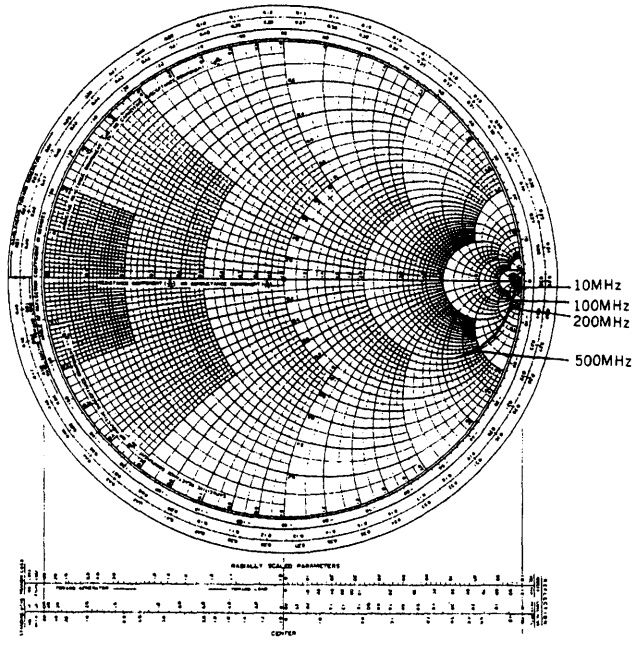


Input Sensitivity vs. Input Frequency (Temperature Dependence)



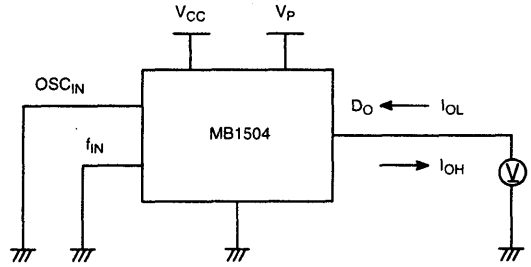


INPUT IMPEDANCE

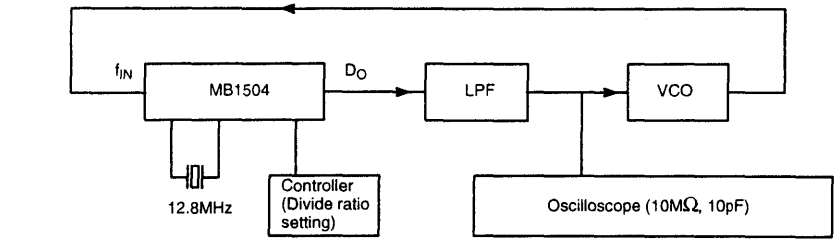


TEST CIRCUIT

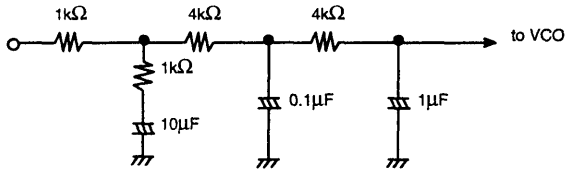
D_O Pin Output Current (I_{OH}, I_{OL}) Measurement



Lock up Time Measurement

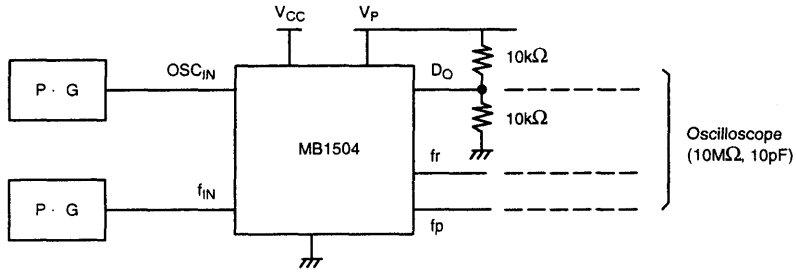


LPF Circuit



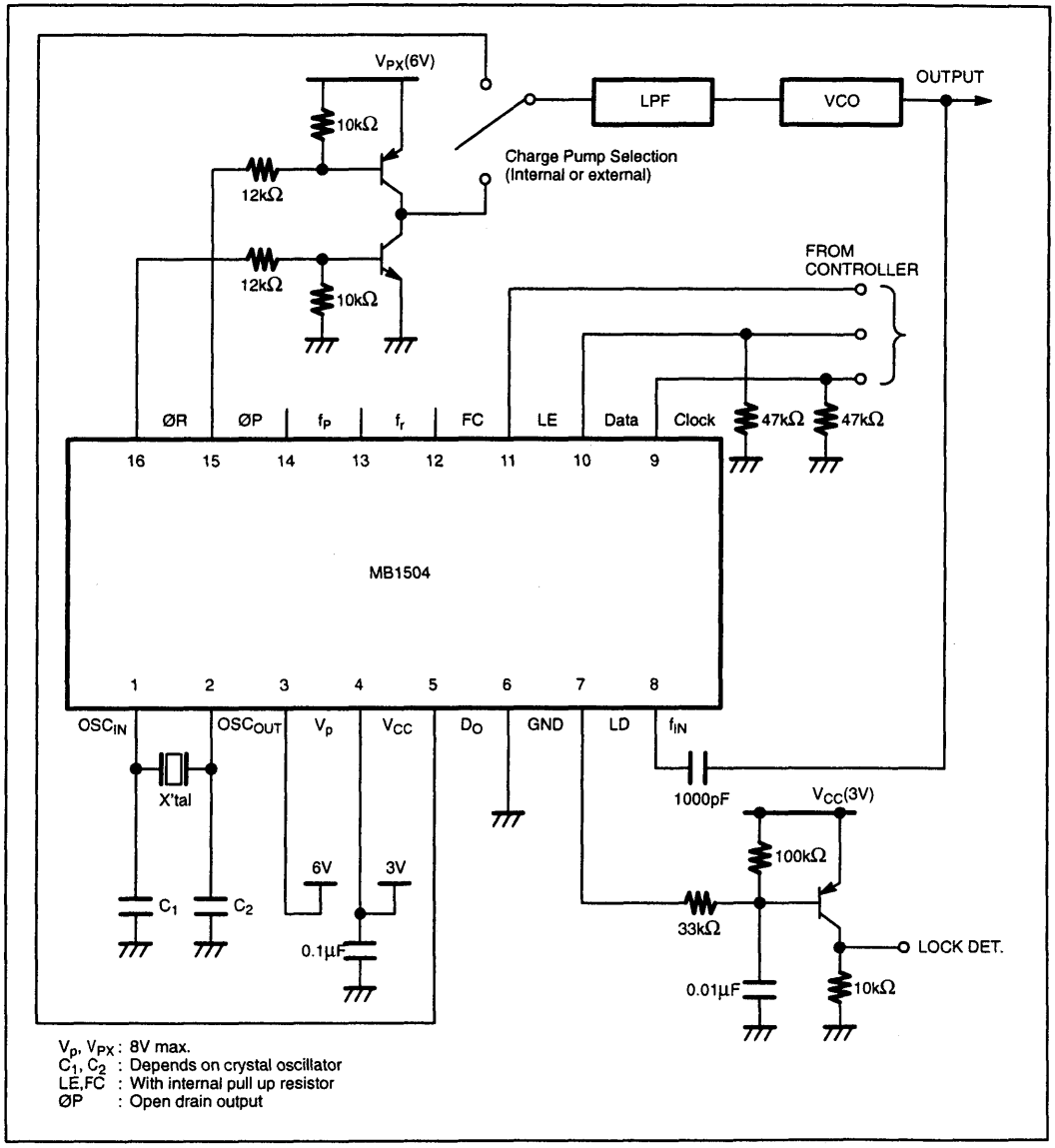
V_{CC}=3V, V_P=8V
f_{VCO}=Low unlock condition ⟶ Step to Lock condition (533MHz)
f_{VCO}=High unlock condition ⟶ Step to Lock condition (518MHz)

Phase Characteristics Measurement



V_{CC}=3V, V_P=3V
Δf=fr−fp
Energy (En)=V^2t

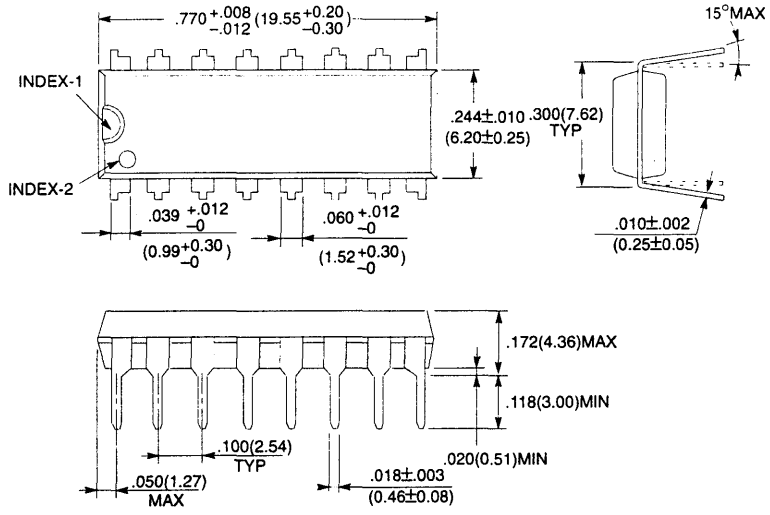
TYPICAL APPLICATION EXAMPLE



V_p, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-16P-M04)

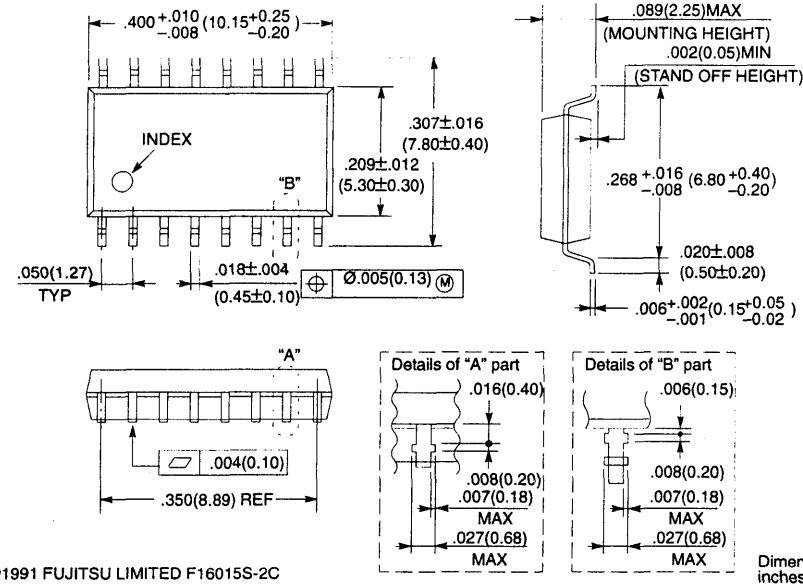


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-16P-M06)



Dimensions in inches (millimeters)

June 1995
Edition 0.2a

FUJITSU

MB15E05/E06 Product Profile Sheet

On-chip 2.0GHz/2.5GHz PRESCALER

The Fujitsu MB15E05/E06 are serial input Phase Locked Loop (PLL) frequency synthesizers with a 2.0GHz (MB15E05) and a 2.5GHz (MB15E06) prescalers. A 64/65 or a 128/129 can be selected for the prescaler that enables pulse swallow operation.

The latest BiCMOS process technology is used, resulting in a supply current of 6mA typ. (MB15E05) and 7mA typ. (MB15E06). They operate with a supply voltage of 3.0V (typ.).

Furthermore, a super charger circuit is included to get a fast tuning as well as low noise performance. As a result of this, MB15E05/E06 are ideally suitable for digital mobile communications, such as PCN(Personal Communication Network), PCS(Personal Communication Service), Wireless LAN etc.

PRELIMINARY

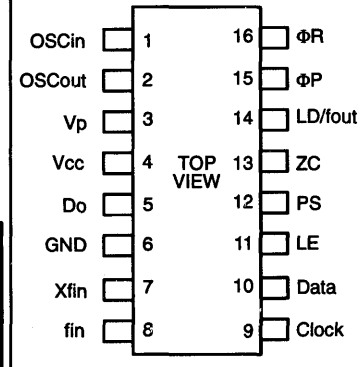
FPT-16P-M05

4

FEATURES

- High frequency operation MB15E05 : 2.0GHz max.
  MB15E06 : 2.5GHz max.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current: MB15E05 : I_{CC} = 6.0 mA typ. (Vcc = 3V)
  MB15E06 : I_{CC} = 7.0 mA typ. (Vcc = 3V)
- Power saving function : I_{PS} = 10 µA max. (Vcc = 3V)
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 5 to 16383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 5 to 2047
- Wide operating temperature: T_A = –40 to 85°C
- Plastic 16-pin SSOP package (FPT–16P–M05)

PIN ASSIGNMENT



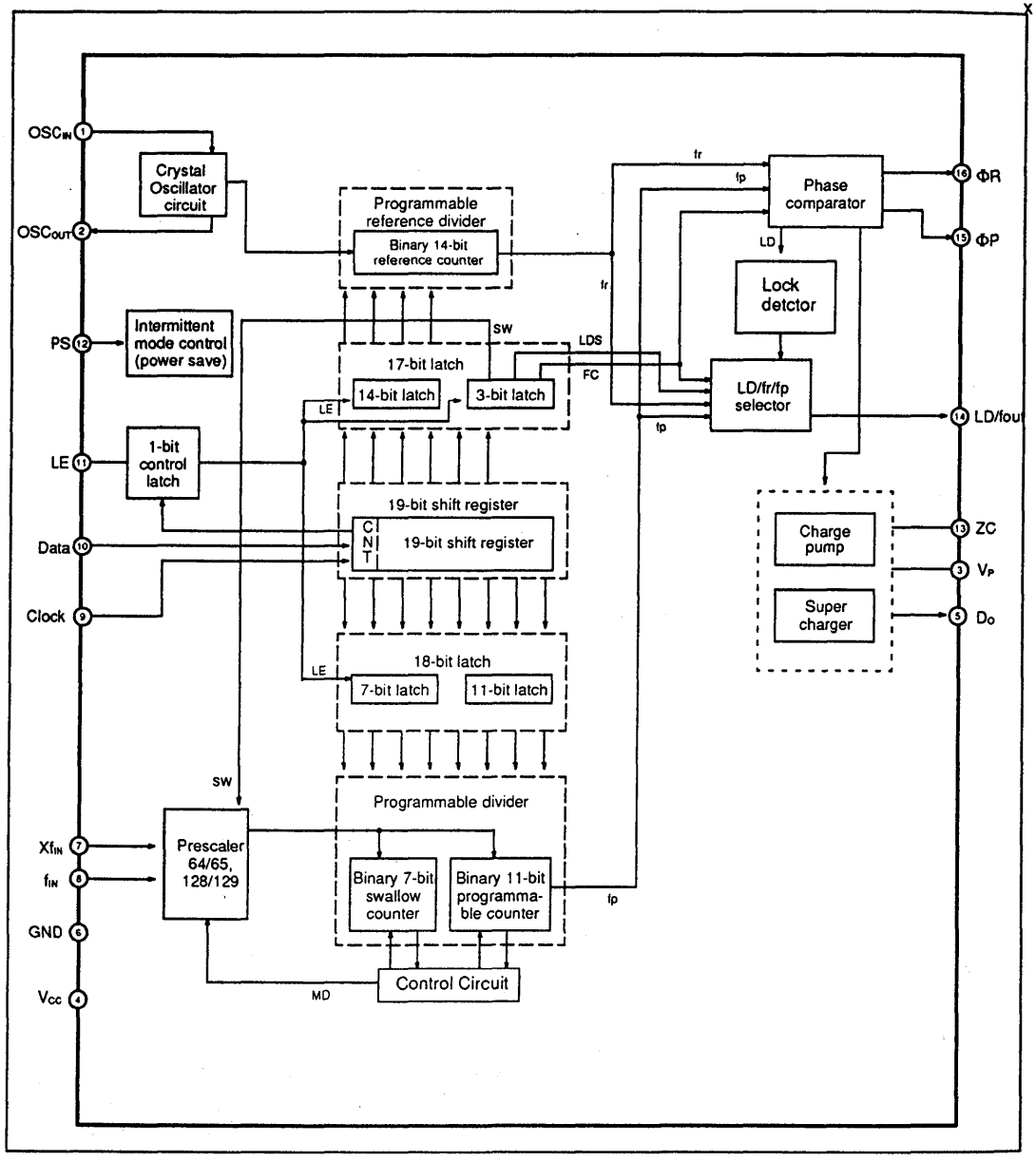
ABSOLUTE MAXIMUM RATINGS (SEE NOTE)

Ratings	Symbol	Value	Unit	Remark
Supply voltage	V_{CC}	–0.5 to +4.0	V	
	V_P	V_{CC} to +6.0	V	
Input voltage	V_I	–0.5 to V_{CC} +0.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Storage temperature	Tstg	–55 to +125	°C	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for an crystal or a TCXO.
2	OSC_{OUT}	O	Oscillator output. Connection for an external crystal.
3	V_P	–	Power supply input for the charge pump.
4	V_{CC}	–	Power supply input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed by FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done with AC coupling.
9	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. *(Open is prohibited.)*
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. *(Open is prohibited.)* Control bit = "H" ; Data is transmitted to the programmable reference counter. Control bit = "L" ; Data is transmitted to the programmable counter.
11	LE	I	Load enable signal input *(Open is prohibited.)* When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving control input. This pin should be set at "L" at Power–ON. *(Open is prohibited.)* PS = "H" ; Normal mode PS = "L" ; Power saving mode
13	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = "H" ; Normal Do output. ZC = "L" ; Do becomes high impedance.
14	LD/f_{OUT}	O	Lock detector output(LD)/Monitor pin of the phase comparator(fout). A LDS bit in a serial data switchs LD/fout pin's output. LDS = "H" ; outputs fout (fr/fp monitoring output) LDS = "L" ; outputs LD ("H" at locking, "L" at unlocking.)
15	ΦP	O	Phase comparator output for an external charge pump.
16	ΦR	O	Phase comparator output for an external charge pump.

FUNCTION DESCRIPTIONS

PULSE SWALLOW FUNCTION

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

SERIAL DATA INPUT

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control bit data as follows:

Table.1 CONTROL BIT

Control bit (CNT)	Destination of serial data
H	17 bit latch (for the programmable reference divider)
L	18 bit latch (for the programmable divider)

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS

CNT : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bit for the programmable reference counter (5 to 16,383) [Table. 2]
SW : Divide ratio setting bit for the prescaler (64/65 or 128/129) [Table. 5]
FC : Phase control bit for the phase comparator [Table. 7]
LDS : LD/fout signal select bit [Table. 6]

Note: Start data input with MSB first.

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 4]

Note: Start data input with MSB first.

4

Table2. BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.
• Divide ratio (N) range = 5 to 2,047

Table.4 BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note:• Divide ratio (A) range = 0 to 127

Table. 5 PRESCALER DATA SETTING

SW	Prescaler Divide ratio
H	64/65
L	128/129

Table. 6 LD/fout OUTPUT SELECT DATA SETTING

LDS	LD/fout output signal
H	fout signal
L	LD signal

Relation between the FC input and phase characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ΦR, ΦP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ΦR, and ΦP is shown below.

Table. 7 FC BIT DATA SETTING (LDS = "H")

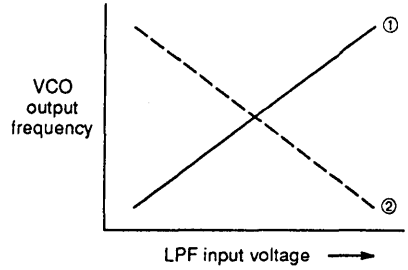
	FC = High				FC = Low			
	Do	ΦR	ΦP	LD/fout	Do	ΦR	ΦP	LD/fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z*	(fp)
$f_r < f_p$	L	H	Z*	(fr)	H	L	L	(fp)
$f_r = f_p$	Z*	L	Z *	(fr)	Z*	L	Z*	(fp)

*: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

*: When the LPF and VCO characteristics are similar to ①, set FC bit high.

*: When the VCO characteristics are similar to ②, set FC bit low.



4

POWER SAVING MODE (INTERMITTENT MODE CONTROL CIRCUIT)

Setting a PS pin to Low, the IC enters into power saving mode resultatly current sonsumption can be limited to 10μA (max.).
Setting PS pin to High, power saving mode is released so that the IC works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from the power saving mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF"s time constant. As a result of this, VCO's frequency is kept at the locking frequency.

Note; • *While the power saving mode is executed, ZC pin should be set at "H" or open. If ZC is set at "L" during power saving mode, approximately 10μA current flows.*
• *PS pin must be set "L" at Power-ON.*

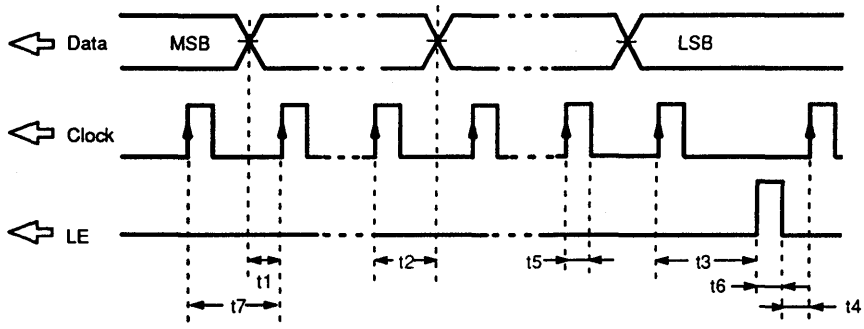
Table.8 PS PIN SETTING

PS pin	Status
H	Normal mode
L	Power saving mode

Table.9 ZC PIN SETTING

ZC pin	Do output
H	Normal output
L	High impedance

SERIAL DATA INPUT TIMING

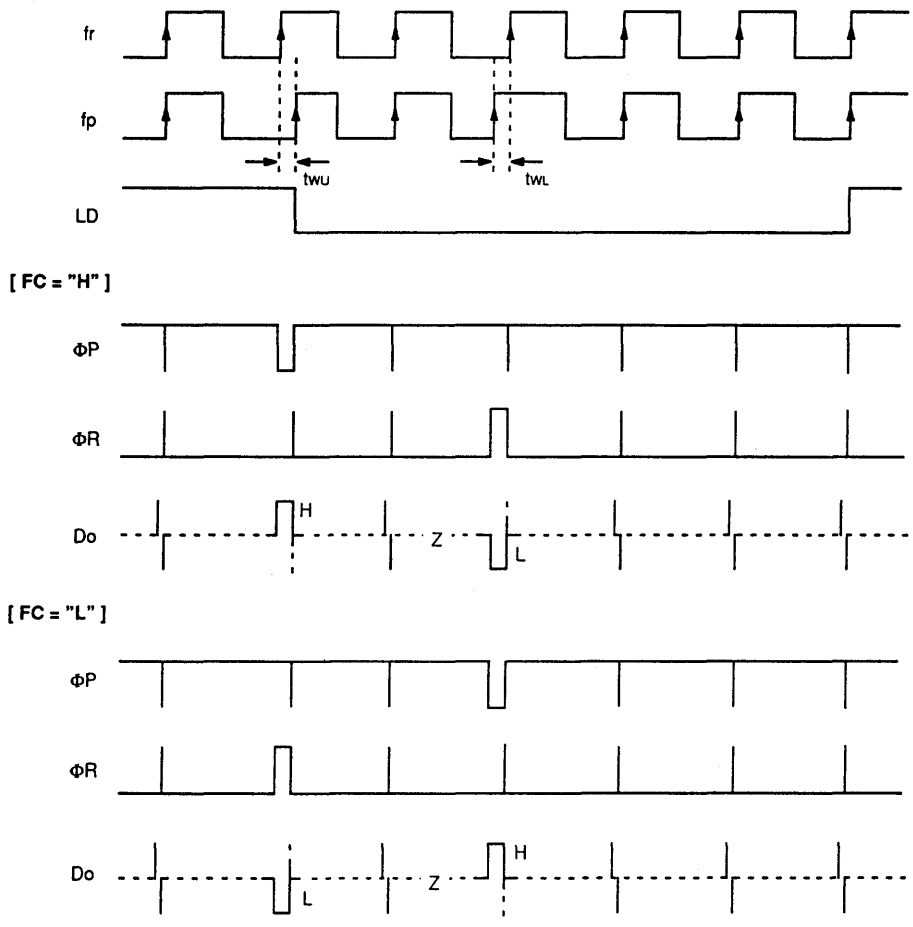


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

PHASE COMPARATOR OUTPUT WAVEFORM



Notes: 1. Phase error detection range: -2π to $+2\pi$
2. Pulses on Do output signal during locked state are output to prevent dead zone.
3. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
4. twu and twL depend on OSCin input frequency.
   twu ≥ 8/fosc (e. g. twu ≥ 625ns, foscin = 12.8 MHz)
   twL ≤ 16/fosc (e. g. twL ≤ 1250ns, foscin = 12.8 MHz)
5. LD becomes high during the power saving mode (PS = "L".)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	Vp	Vcc	–	6.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	T_A	–40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current *1	MB15E05	Icc	fin_{IF} = 2000MHz, fosc = 12MHz	–	6.0	–	mA
	MB15E06	Icc	fin_{RF} = 2500MHz, fosc = 12MHz	–	7.0	–	
Power Saving Current *2		Ips	Vcc current at PS ="L and ZC = "H""	–	–	10	µA
Operating Frequency	MB15E05	fin		100	–	2000	MHz
	MB15E06	fin		100	–	2500	
Crystal Oscillator Operating Frequency		f_{OSC}	min. 500mVp-p	3	–	40	
Input Sensitivity	fin	Pfin	50Ω termination (Refer to the test circuit.)	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	Vcc	mVp-p

*1: Conditions ; Vcc = 3.0V, Ta = 25°C, in locking state.
*2: Conditions ; Vcc = 3.0V, Ta = 25°C, in power saving state.

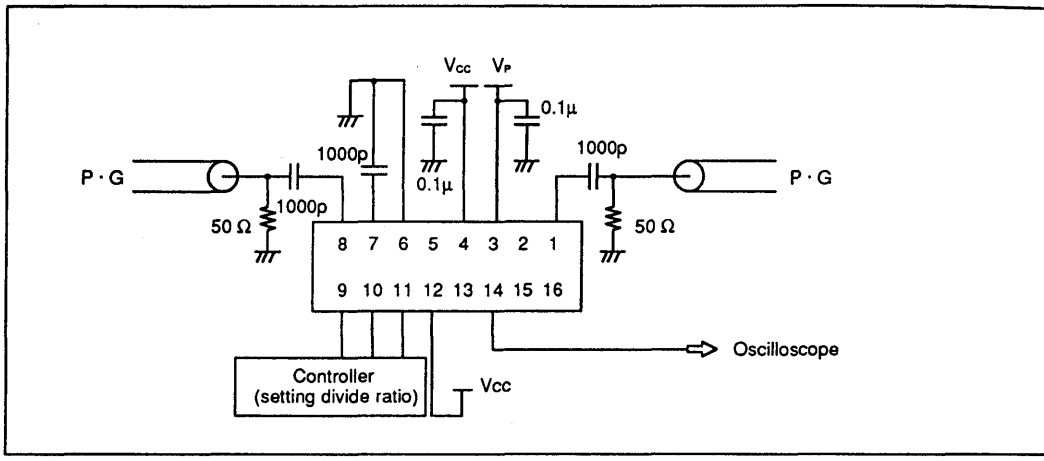
ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Input Voltage	Data, Clock, LE, PS, ZC	V_{IH}		Vccx0.7	–	–	V
		V_{IL}		–	–	Vccx0.3	
Input Current	Data, Clock, LE, PS	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	ZC	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}	Pull up input	–100	–	0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output Voltage	ΦP	V_{OL}	Open drain output	–	–	0.4	V
	ΦR, LD/fout	V_{OH}		Vcc–0.4	–	–	V
		V_{OL}		–	–	0.4	
	Do	V_{DOH}		Vcc–0.4	–	–	V
		V_{DOL}		–	–	0.4	
High Impedance Cutoff Current	Do	I_{OFF}		–	–	1.1	µA
Output Current	ΦP	I_{OL}	Open drain output	1.0	–	–	mA
	ΦR, LD/fout	I_{OH}		–	–	–1.0	mA
		I_{OL}		1.0	–	–	
	Do	I_{DOH}	Vcc = 3.0V, Vp = 5V, V_{DOH} = 4.0V	–	–10.0*1	–	mA
		I_{DOL}	Vcc = 3.0V, Vp = 5V, V_{DOL} = 1.0V	–	10.0*1	–	

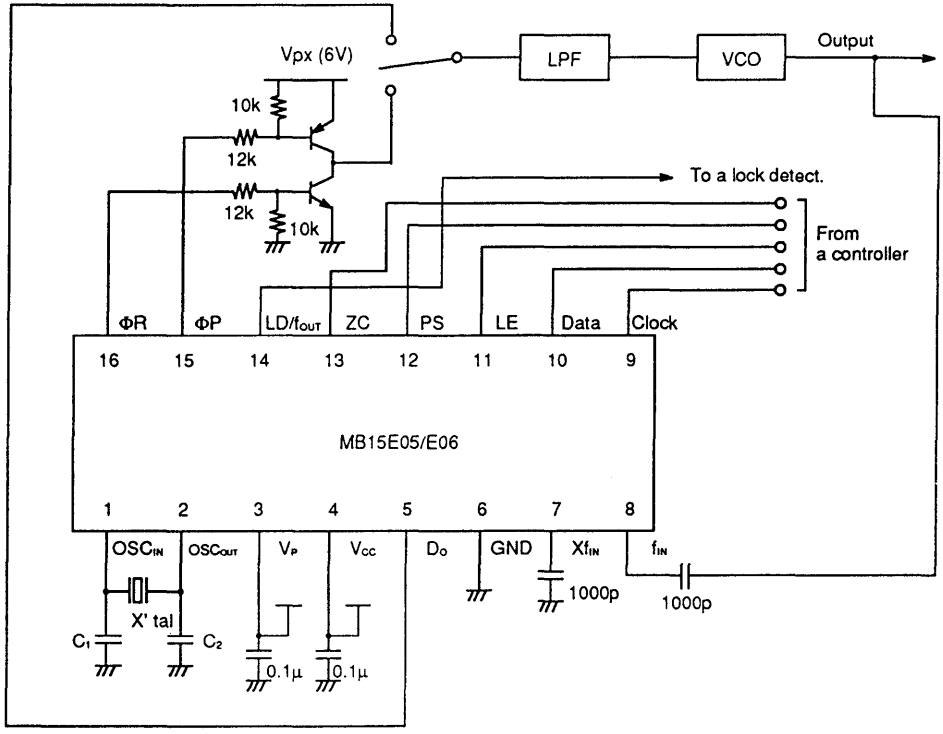
*1: Condition ; Ta = 25°C

4

TEST CIRCUIT
(FOR MEASURING INPUT SENSITIVITY fin/OSCin)



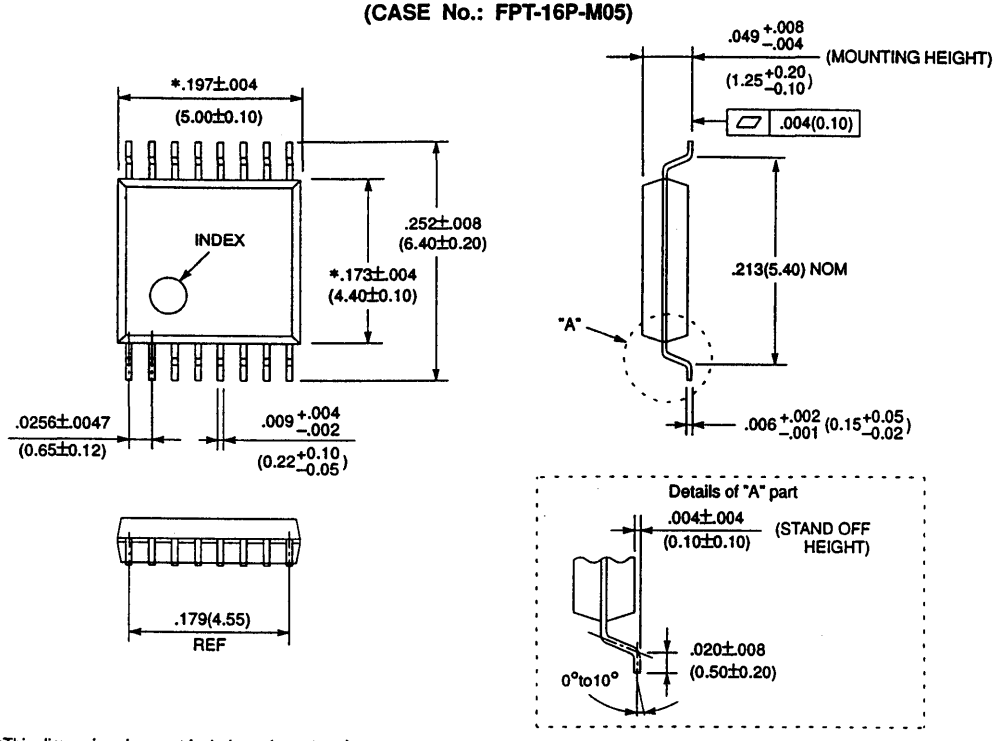
APPLICATION EXAMPLE



V_{PX} : Maximum 6 V
C_1, C_2 : Depend on the crystal parameters

PACKAGE DIMENSION

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0a

FUJITSU

DATA SHEET

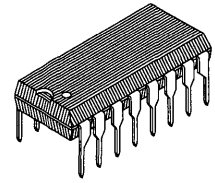
MB1505

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

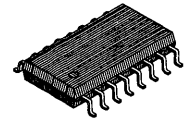
LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 600MHz PRESCALER

The Fujitsu MB1505, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function. The MB1505 contains a 600MHz two modulus prescaler that can select of either 32/33 or 64/65 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analog switch to speed up lock up time.

It operates supply voltage of 5V typ. and achieves very low supply current of 6mA typ. realized through the use of Fujitsu Advanced Process Technology.



Plastic Package
DIP–16P–M04



Plastic Package
DIP–16P–M02

FEATURES

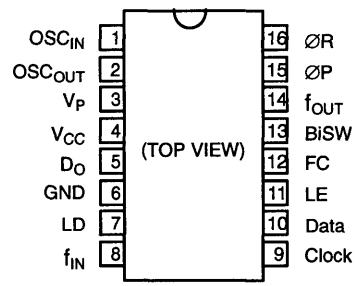
- High operating frequency: $f_{IN\ MAX}$=600MHz ($P_{IN\ MIN}$= –4dBm)
- Pulse swallow function: 32/33 or 64/65
- Low supply current: I_{CC} 6mA typ.
- Serial input 18-bit programmable divider consisting of:
  — Binary 7-bit swallow counter: 0 to 63
  — Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  — Binary 14-bit programmable reference counter: 8 to 16383
  — 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2 types of phase detector output
  — On-chip charge pump (Bipolar type)
  — Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic DIP Package (Suffix: —P)
  16-pin Plastic Flat Package (Suffix: —PF)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 0.8	V
Output Current	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

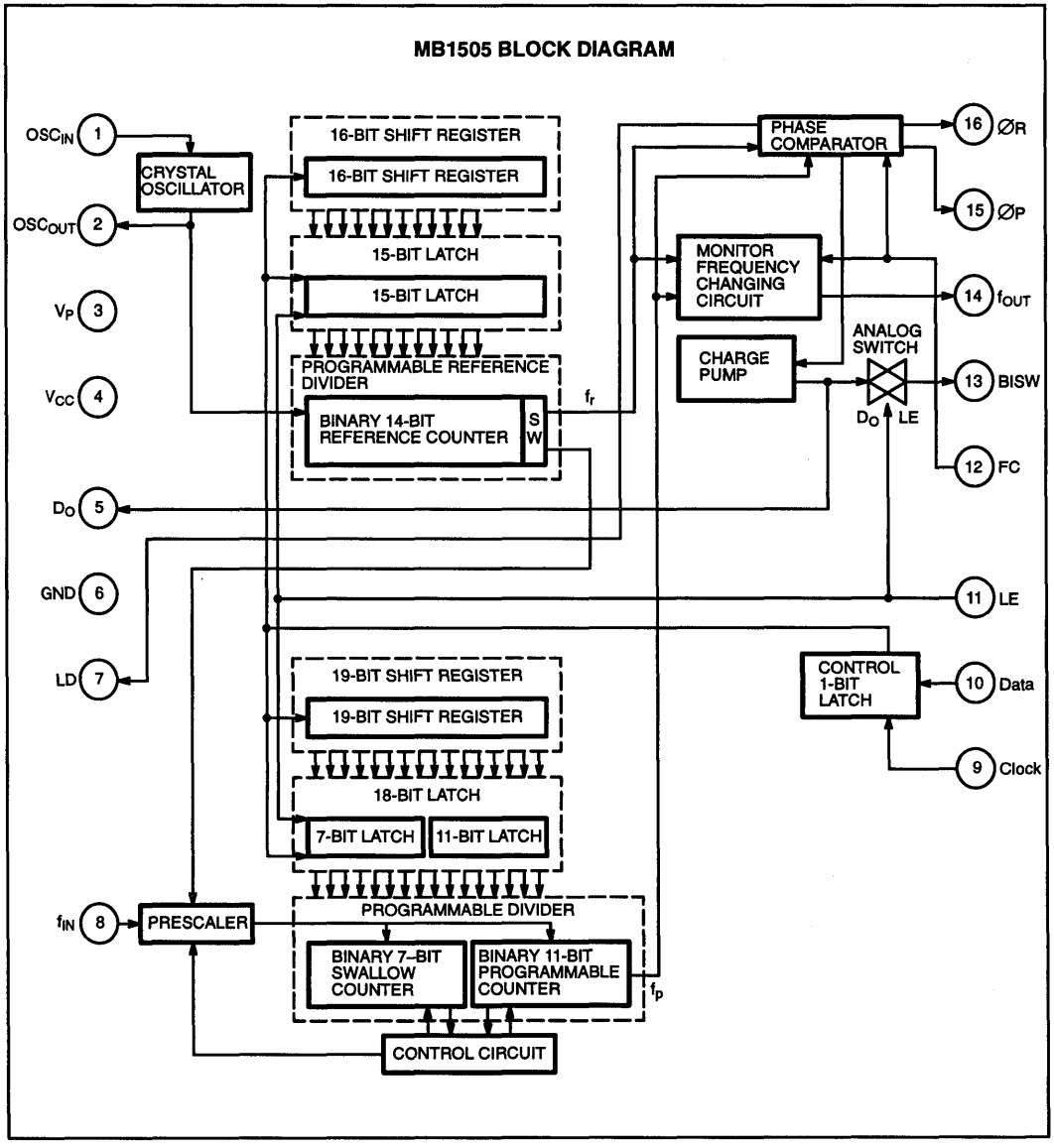
NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1505 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump and analog switch.
4	V_{CC}	—	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
6	GND	—	Ground
7	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r, and f_p exists, this pin outputs low level.
8	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control f_{OUT} pin (test pin) output level for f_r or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
14	f_{OUT}	O	Monitor pin of phase comparator input. f_{OUT} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level.
15 16	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.

Binary serial data is input to Data pin.

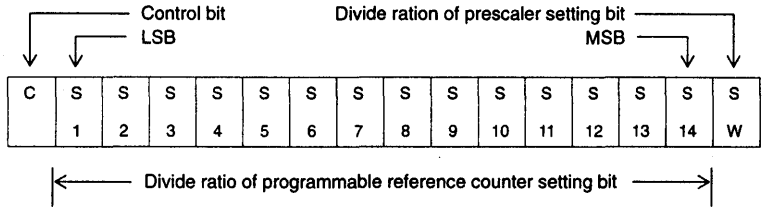
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.

Control data "H" data is transferred into 15-bit latch.

Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

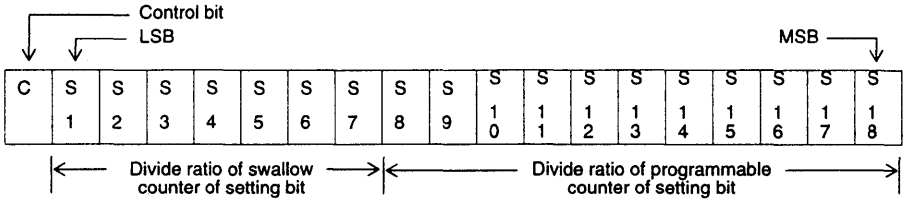
Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 32/33
SW=L :64/65
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.

Serial 19-bit data format is shown on following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 63
S7 should be set to zero

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

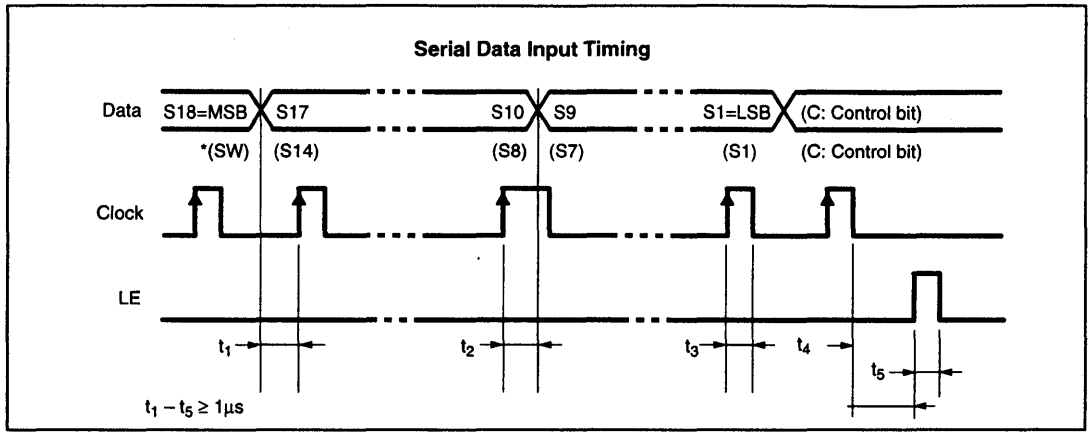
Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 63)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{VCO} = [(PxN)+A] \times f_{OSC} \div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 63$, $A<N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)
P: Preset modulus of external dual modulus prescaler (32 or 64)



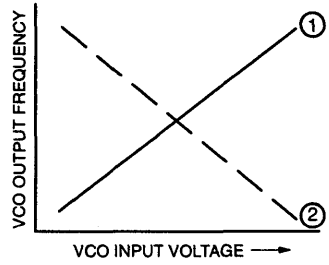
NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (øR, øP) are reversed depending upon FC pin input level. Also, monitor pin (f_{OUT}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, øR, øP) and FC input level are shown below.

	FC=H or open				FC=L			
	D_O	øR	øP	f_{OUT}	D_O	øR	øP	f_{OUT}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

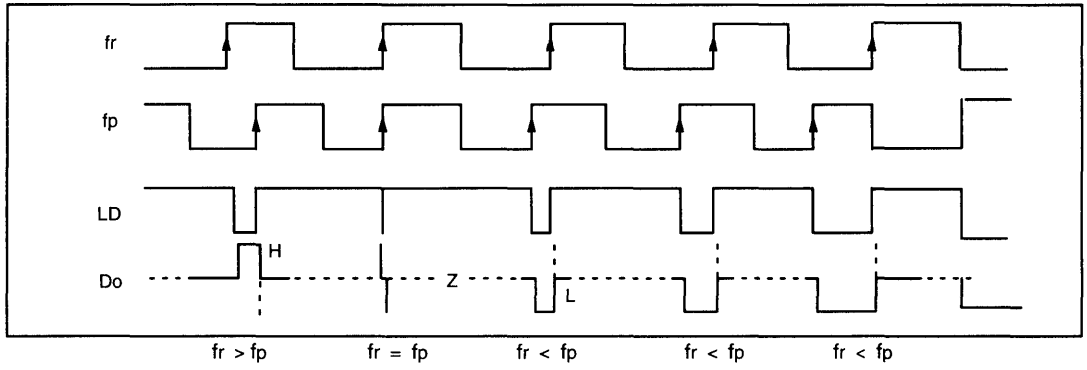
Note: Z = (High impedance)



VCO CHARACTERISTICS
Depending upon VCO characteristics, FC pin should be set accordingly:

— When VCO characteristics are like 1, FC should be set High or open circuit;

— When VCO characteristics are like 2, FC should be set Low.



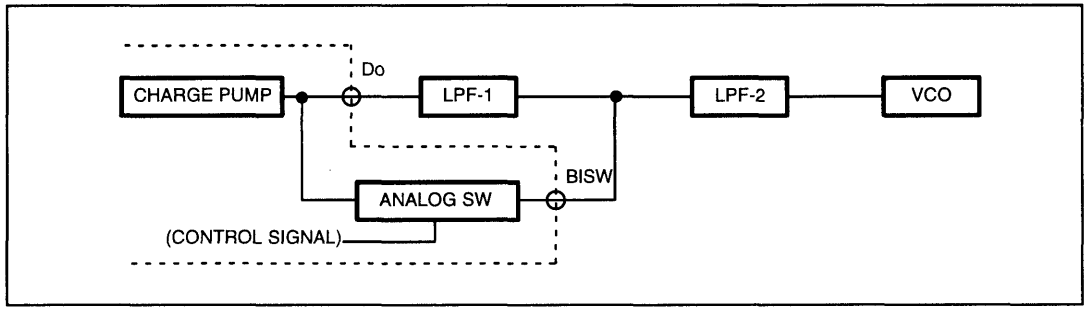
NOTES: Phase difference detection range: —2π to +2π
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r > f_p$ or $f_r < f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) to be connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode): Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

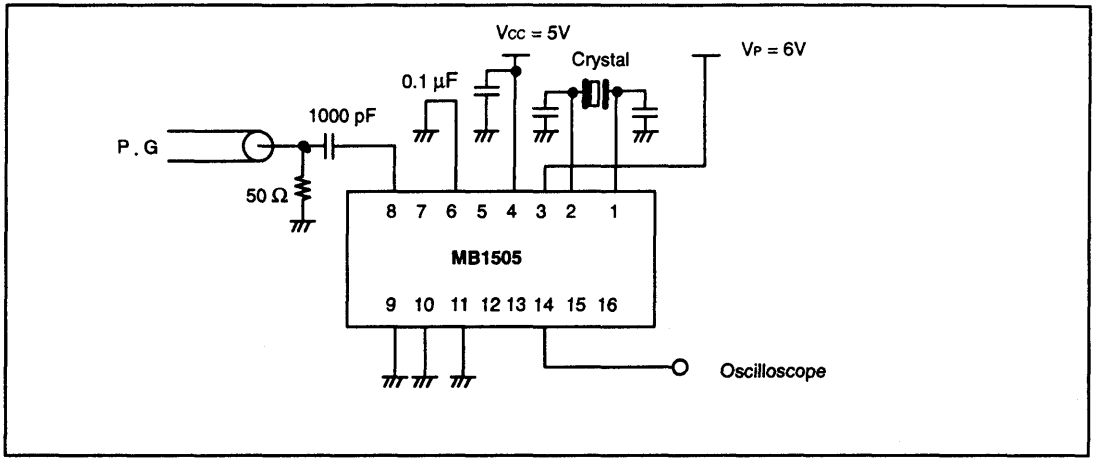
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	V_P	8.0	V
Input Voltage	V_I	GND		V_{CC}	V
Operating Temperature	T_A	–40		85	°C

ELECTRICAL CHARACTERISTICS

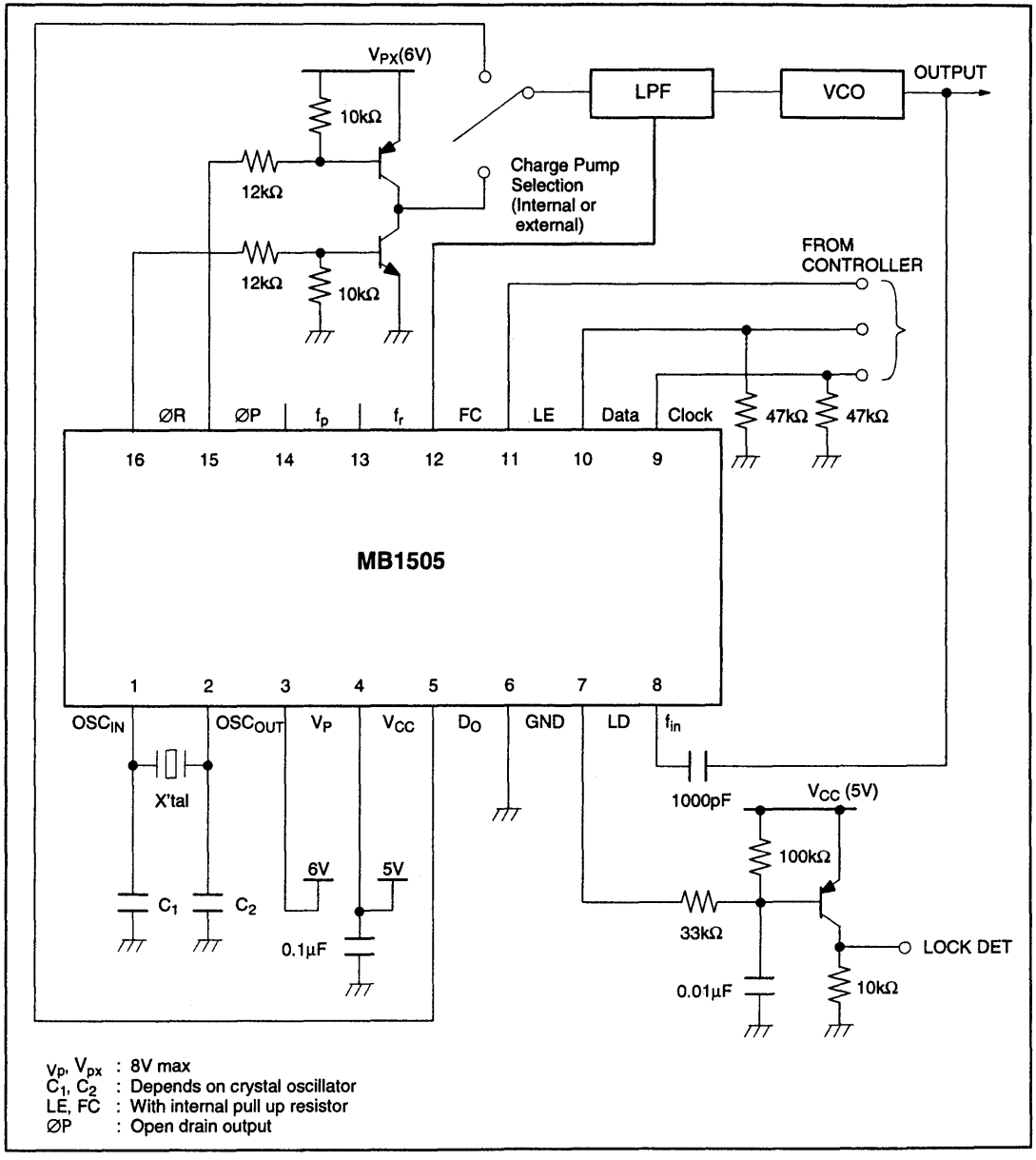
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1		6.0		mA
Operating Frequency	f_{in}	f_{in}	Note2	10		600	MHz
	OSC_{IN}	f_{OSC}			12	20	MHz
Input Sensitivity	f_{in}	P_{fin}		–4		6	dBm
	OSC_{IN}	V_{OSC}		0.5			V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IN}		V_{CC}x0.7			V
Low-level Input Voltage		V_{IL}				V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}			1.0		µA
Low-level Input Current		I_{IL}			–1.0		µA
Input Current	OSC_{IN}	I_{OSC}			±50		µA
	LE, FC	I_{LE}			–60		µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 5 V	4.4			V
Low-level Output Current		V_{OL}				0.4	V
N-channel Open Drain Cutoff Current	D_O, ØP	I_{OFF}	$V_P = V_{CC}$ to 8V V_{OOP}= GND to 8V			1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0			mA
		I_{OL}		1.0			mA
Analog Switch On Resistor		R_{ON}			25		Ω

NOTE: 1: f_{in} = 600MHz, OSC_{IN}=12MHz, V_{cc}=5V. Inputs are grounded and outputs are open.
2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT



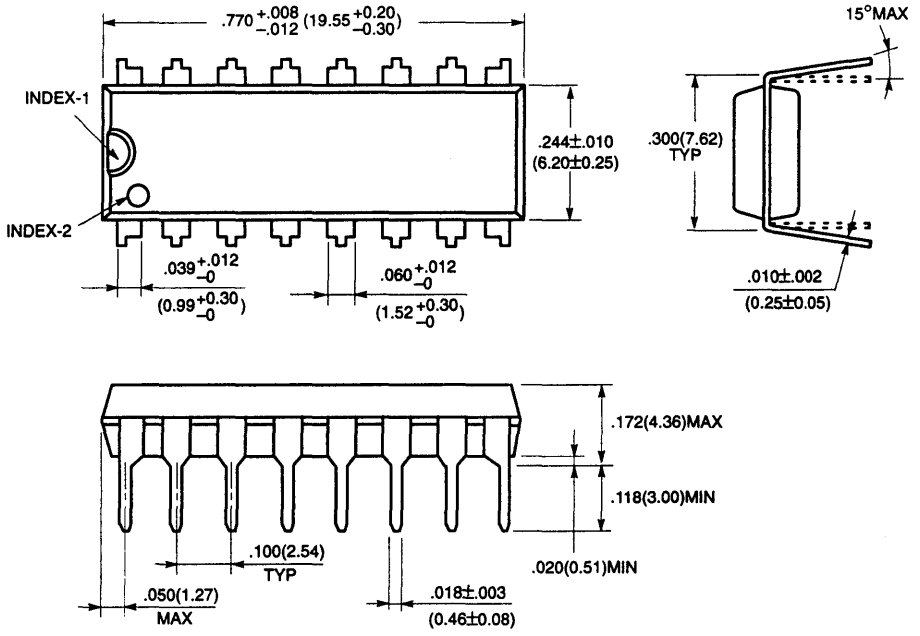
TYPICAL APPLICATION EXAMPLE



V_P, V_{PX} : 8V max
C_1, C_2 : Depends on crystal oscillator
LE, FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

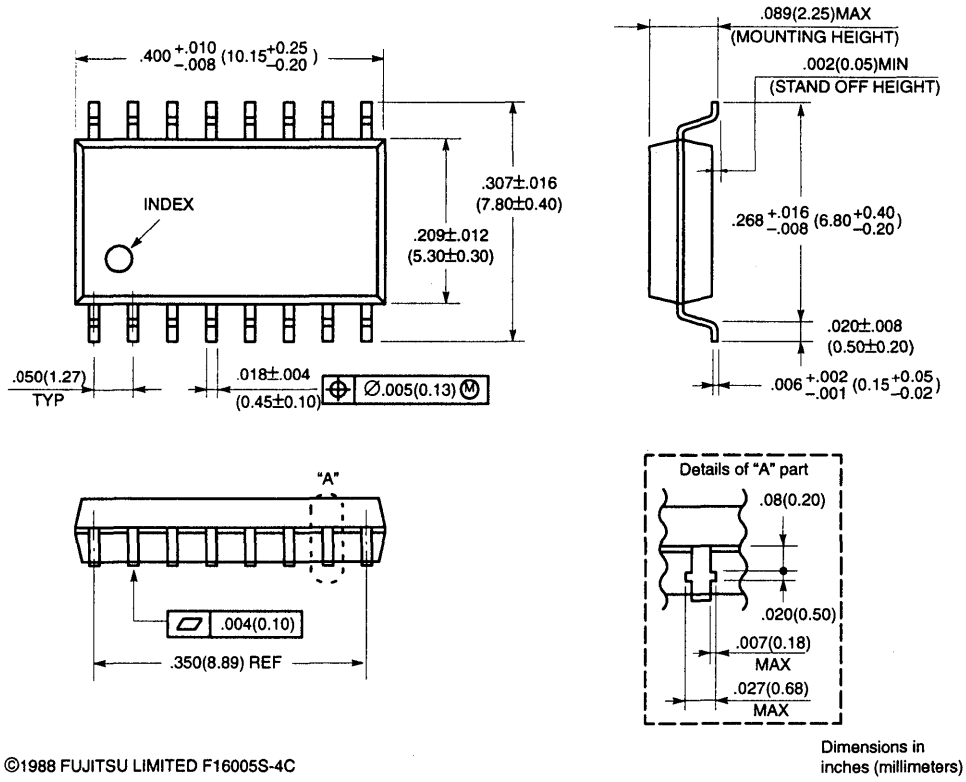
16–Lead Plastic Dual In–Line Package
(Case No.: DIP–16P–M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

16–Lead Plastic Flat Package
(Case No.: FPT–16P–M02)



Dimensions in
inches (millimeters)

DS04–21319–1E

FUJITSU

DATA SHEET

MB1506 *ASSP for DTS* Bi–CMOS (For 2.0 GHz band)

PLL Frequency Synthesizer with Built–in Prescaler

4

■ DESCRIPTION

The Fujitsu MB1506 is a PLL (phase-locked loop) frequency synthesizer, ideally suited for DBS tuner, MCA radio and similar wireless communications devices.

The MB1506 features a 2.0 GHz, two-modulus prescaler to enable pulse-swallow type processing, as well as analog switches for faster lock up time.

Fujitsu's Bi-CMOS process is used for low power consumption of Icc = 18 mA (typ.).

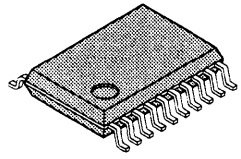
■ FEATURES

- High speed operation: fin = 2.0 GHz
- Low power consumption: Icc = 18 mA (typ.)
- Wide operating temperature range: Ta = –40°C to +85°C
- Two types of phase comparator output (built-in charge pump, external charge pump)
- Built-in functions:
  - 16-bit shift register
  - 15-bit latch
  - Reference frequency divider
    - Binary 14-bit programmable reference counter (divide ratio: 8 to 16383)
    - 1-bit switch counter
  - 19-bit shift register
  - 19-bit latch

(Continued)

■ PACKAGE

Plastic SSOP, 20-pin

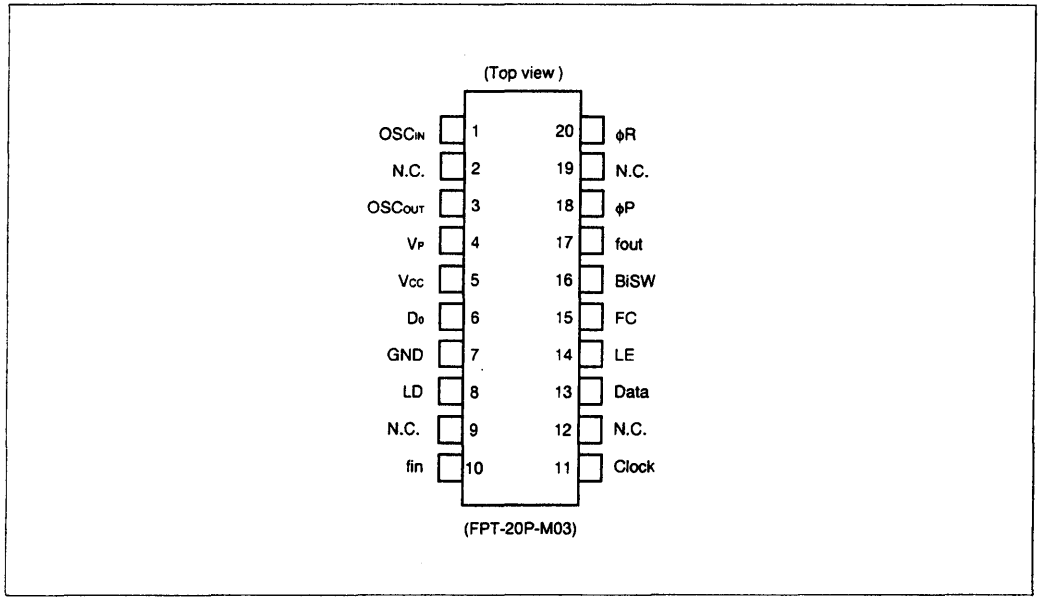


(FPT-20P-M03)

(Continued)

Comparison dividers
Binary 8-bit swallow counter (divide ratio: 0 to 255)
Binary 11-bit programmable counter (divide ratio: 16 to 2047)
Phase comparator with phase conversion function
2.0 GHz band two-modulus prescaler (divide ratios: 128/129, 256/257)
Control signal generator circuit
Crystal oscillator circuit
Monitor frequency switching circuit
Charge pump
1-bit control latch
Analog switch

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

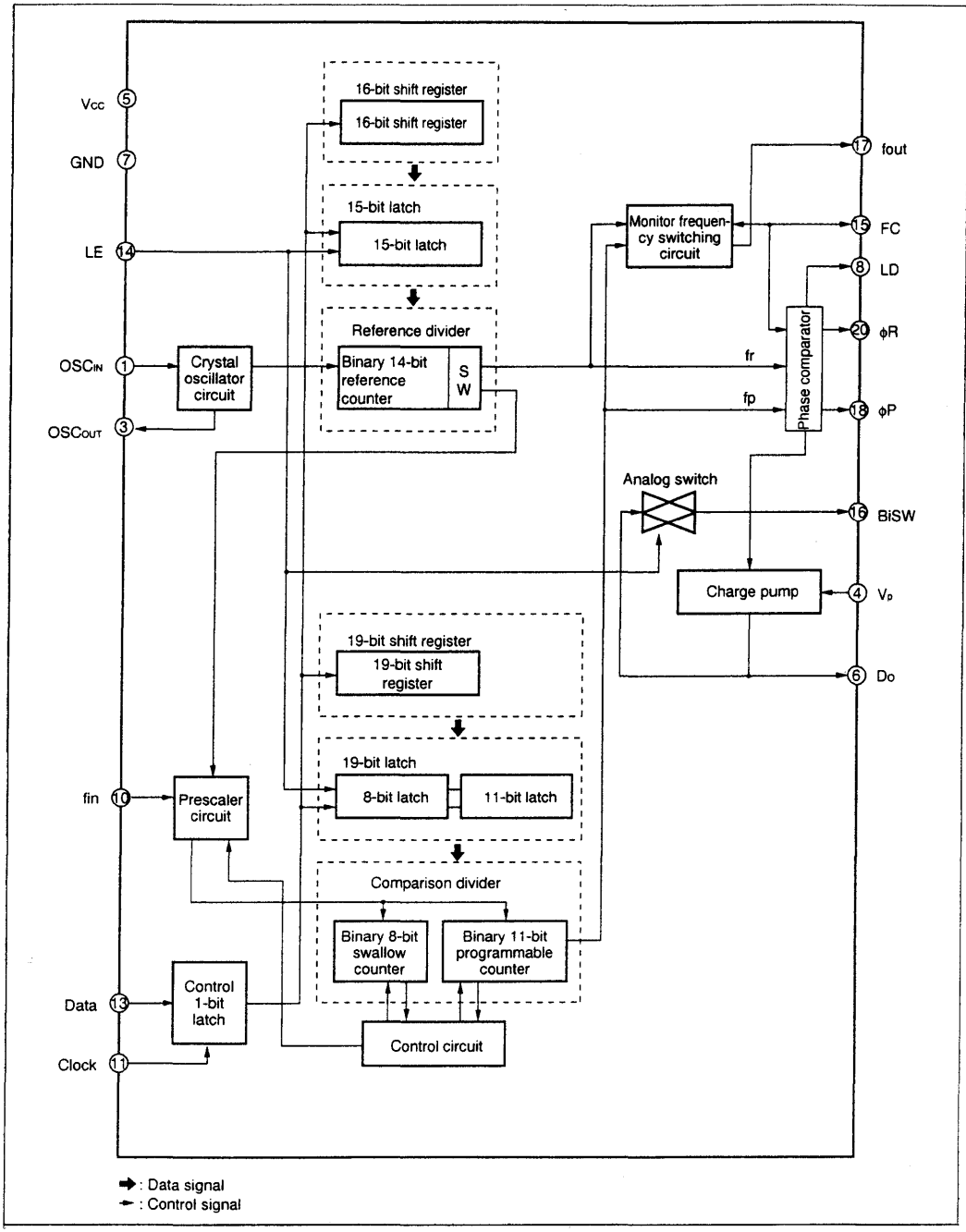
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>OSCIN</td><td>I</td><td rowspan="2">Crystal oscillator connection pin for reference divider (OSCIN = oscillator circuit input pin, and OSCOUT = oscillator circuit output pin)</td></tr>
<tr><td>3</td><td>OSCOUT</td><td>O</td></tr>
<tr><td>4</td><td>VP</td><td>—</td><td>Power supply pin for charge pump output and analog switch output</td></tr>
<tr><td>5</td><td>Vcc</td><td>—</td><td>Power supply pin</td></tr>
<tr><td>6</td><td>Do</td><td>O</td><td>On-chip charge pump output pin
Phase characteristics may be inverted according to the setting of the FC pin.</td></tr>
<tr><td>7</td><td>GND</td><td>—</td><td>GND pin</td></tr>
<tr><td>8</td><td>LD</td><td>O</td><td>Phase comparator output pin
Normal setting is LD = "H" with an output signal LD = "L" equivalent to the duration of the phase error between fr and fp.</td></tr>
<tr><td>10</td><td>fin</td><td>I</td><td>Prescaler input pin
Use in an AC coupled state.</td></tr>
<tr><td>11</td><td>Clock</td><td>I</td><td>Clock signal input pin for 19-bit shift register and 16-bit shift register
Data is read on the rising edge of the clock pulse.</td></tr>
<tr><td>13</td><td>Data</td><td>I</td><td>Serial data input pin for binary coded data
The final data bit is the control bit.
<table>
<tr><th>Control data</th><th>Serial data transfer destination</th></tr>
<tr><td>H</td><td>15-bit latch</td></tr>
<tr><td>L</td><td>19-bit latch</td></tr>
</table></td></tr>
<tr><td>14</td><td>LE</td><td>I</td><td>Load enable signal input pin (with pull-up resistor)
When LE = "H" or LE = "OPEN", the contents of the shift register is transferred to one of the latches according to the combination of serial data control bit settings. Also, when the internal analog switch is "on" at this time, the signal output from the internal charge pump is sent to the BiSW pin.</td></tr>
<tr><td>15</td><td>FC</td><td>I</td><td>Phase comparator phase switching pin (with pull-up resistor)
Enables inversion of the polarity of the phase comparator output, according to the polarity of externally connected LPF or VCO. When FC = "L" the charge pump and phase comparator characteristics are inverted.
Also switches the output of the fout pin, either fr or fp.</td></tr>
<tr><td>16</td><td>BiSW</td><td>O</td><td>Analog switch output pin
Normally in high-impedance state, outputs the status of the internal charge pump only when the switch is turned on (LE = "H").</td></tr>
<tr><td>17</td><td>fout</td><td>O</td><td>Phase comparator input monitor pin
According to the FC pin input level, this pin outputs either the output signal from the reference divider (fr) or the comparison divider (fp).
<table>
<tr><th>FC</th><th>Output signal</th></tr>
<tr><td>H</td><td>fr output equivalent</td></tr>
<tr><td>L</td><td>fp output equivalent</td></tr>
</table></td></tr>
</table>

(Continued)

(Continued)

Pin No.	Pin name	I/O	Descriptions
18	φP	O	Phase comparator output signal pin for external charge pump Phase characteristics may be inverted according to the FC pin setting. The φP pin is N channel open-drain output.
20	φR	O	
2, 9, 12, 19	N.C.	—	No connection.

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. Divide Ratio Settings

Setting values should be determined according to the following formula:

$$fvco = [(M \times N) + A] \times fosc \div R \quad (A < N)$$

fvco: Externally connected VCO output frequency

M: Prescaler frequency division ratio (128 or 256)

N: Binary 11-bit programmable counter setting (16 to 2047)

A: Binary 8-bit swallow counter setting ($0 \leq A \leq 255$)

fosc: Reference oscillator frequency

R: Binary 14-bit programmable reference counter setting (8 to 16383)

2. Serial Data Input Methods

Serial data input uses three pins, the Data pin, Clock pin and LE pin, and is used to separately control the 15-bit reference divider and 19-bit comparison divider.

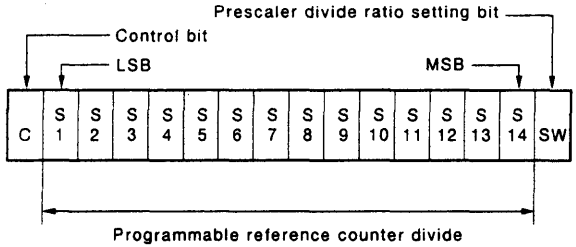
Serial data should be input in binary form at the Data pin.

Serial data is read sequentially by the shift register at the rise edge of the clock signal, and is transferred to a latch together with the appropriate control data when the load enable signal goes to "H" level (or open).

Control data	Serial data transfer destination
H	15-bit latch
L	19-bit latch

(1) Divide Ratios in the Reference Divider

The reference divider is configured with a 16-bit shift register, 15-bit latch and 14-bit reference counter. The serial data configuration has 16 bits, as shown below.



• 14-bit programmable reference counter divide ratios

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio of less than 8 are prohibited.
(Setting value range: 8 to 16383)

Data should be input with the MSB first.

SW: Prescaler divide ratio setting bit.

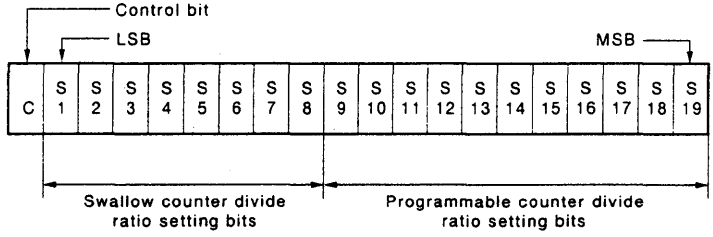
SW	Prescaler divide ratio setting bit
H	128/129
L	256/257

S1 to S14: Divide ratio setting bit (8 to 16383)

C: Control bit (set to "H")

(2) Divide Ratios in the Comparison Divider

The comparison divider is configured with a 19-bit shift register, 19-bit latch, 8-bit swallow counter and 11-bit programmable counter. The serial data configuration has 19 bits, as shown below.



• 7-bit swallow counter divide ratios

Divide ratio A	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:
255	1	1	1	1	1	1	1	1

(Setting value range: 0 to 255)

• 11-bit prgrammable counter divide ratios

Divide ratio N	S 19	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Frequency divide ratios of less than 16 are prohibited. (setting value range: 16 to 2047)

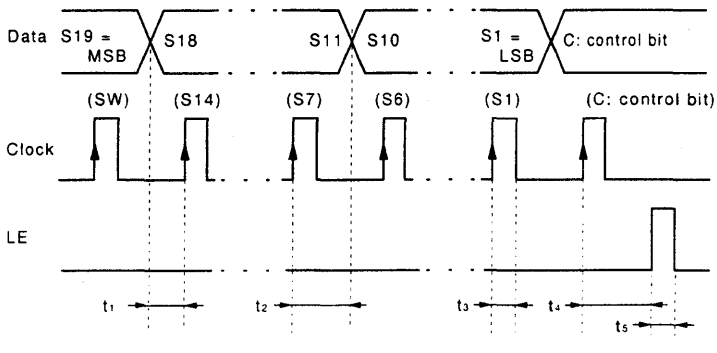
Data should be input with the MSB first.

S1 to S8: Swallow counter divide ratio setting bits (0 to 255)

S9 to S18: Programmable counter divide ratio setting bits (16 to 2047)

C: Control bit (set to "L")

3. Serial Data Input Timing



t_1 to $t_5 \geqq 1\ \mu s$

Items in parentheses ( ) apply when setting divide ratios for the reference divider.
Data is read at the rising of the clock signal.

4. FC Pin Input and Phase Characteristics

The FC pin is used for switching of phase relation in the phase comparator. This pin controls the inversion of phase characteristics in the internal charge pump output (Do) and phase comparator output (φR, φP).

In addition, the output from the phase comparator input monitor pin (fout) can be controlled from the FC pin. The following table shows the relation between FC pin settings and the Do, φR, φP, and fout settings.

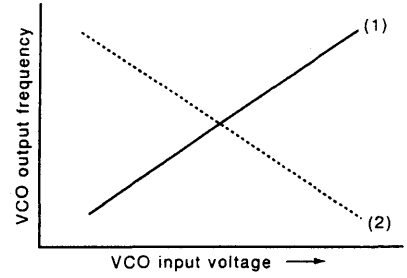
	FC: "H" or open				FC: "L"			
	Do	φR	φP	fout	Do	φR	φP	fout
fr > fp	H	L	L	(fr)	L	H	Z	(fp)
fr = fp	Z	L	Z	(fr)	Z	L	Z	(fp)
fr < fp	L	H	Z	(fr)	H	L	L	(fp)

Z: High impedance

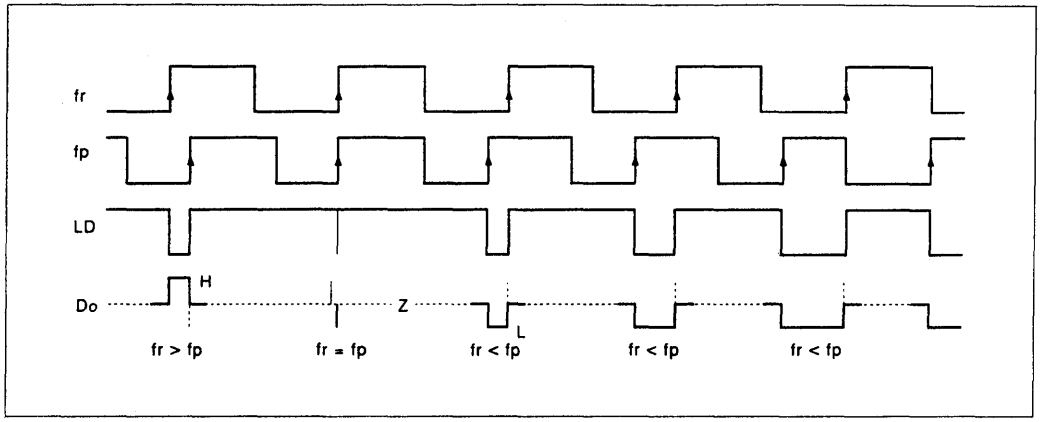
In phase locked loop design, the FC pin should be controlled by VCO polarity.

When VCO polarity is represented by line (1), FC value is "H" or open.

When VCO polarity is represented by line (2), FC value is "L".



The following diagram illustrates the phase comparator output waveform (FC = "H").



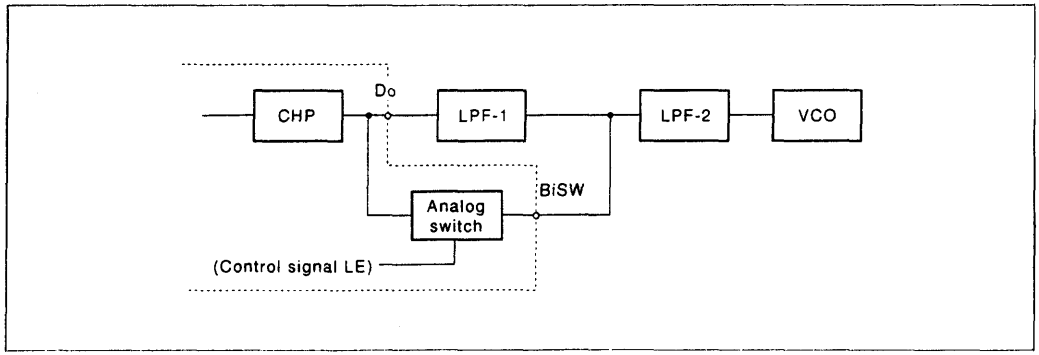
- The phase error detection range is -2π to $+2\pi$.
- Differences in charge pump characteristics may cause slight variation in spikes. The spike is output in order to eliminate dead zones.
- Depending on charge pump characteristics, the spike may not be output when fr > fp, or when fr < fp.

5. Analog Switch

The analog switch is turned on/off by the LE signal. When the switch is on, the output signal from the internal charge pump (Do) is output to the BiSW pin (when off, the pin remains in high impedance state).

LE	Analog switch
H (when internal dividers' setting is changed.)	On
L	Off

As illustrated below, the analog switch can be inserted between the LPF (LPF1 + LPF2) so as to reduce the LPF time constant during PLL channel switching, thereby resulting in faster lock up time.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Power supply voltage	V_{CC}	−0.5	7.0	V
	V_P	V_{CC}	10.0	V
Output voltage	V_{OUT}	−0.5	V_{CC} + 0.5	V
Open drain voltage	V_{OOP}	−0.5	8.0	V
Output current	I_{OUT}	−10	10	mA
Storage temperature	Tstg	−55	+125	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input voltage	V_{IN}	GND	—	V_{CC}	V
Operating temperature	Ta	−40	—	+85	°C

Note: Protection against damage from static electricity has been provided by the addition of anti-static elements and precautionary measures in circuit design, however the following precautions are advised when handling:

- Always place the MB1506 in a conductive case for storage and transporting.
- Before handling, ensure that all operators, fixtures and tools are protected from electrification (grounded), and provide a grounded conductive sheet on the operating floor.
- Always ensure that power is switched off before inserting the device into or removing the device from any socket.
- When handling (or transporting) any circuit board containing an MB1506 device, all leads should be protected with electro-conductive sheeting.

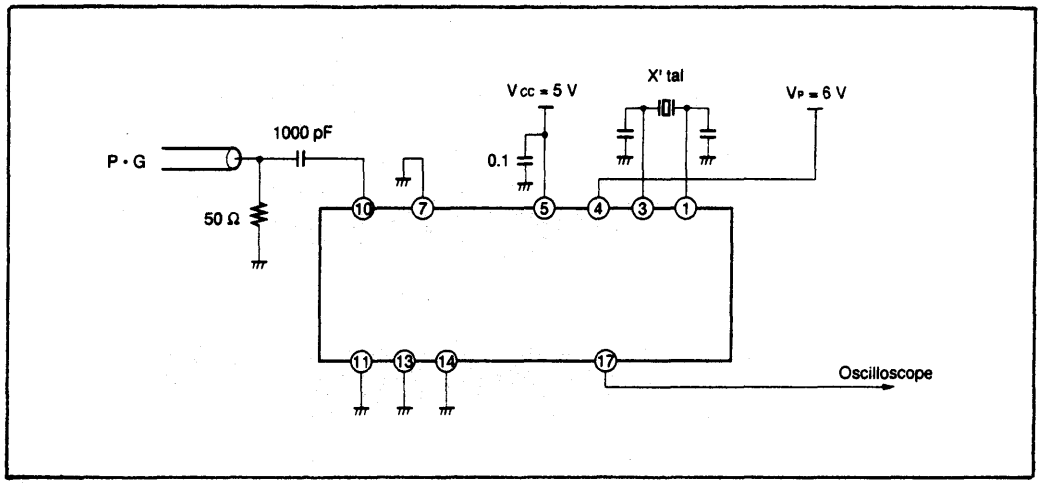
■ ELECTRICAL CHARACTERISTICS

(Vcc = 4.5 V to 5.5, Ta = −40°C to +85°C)

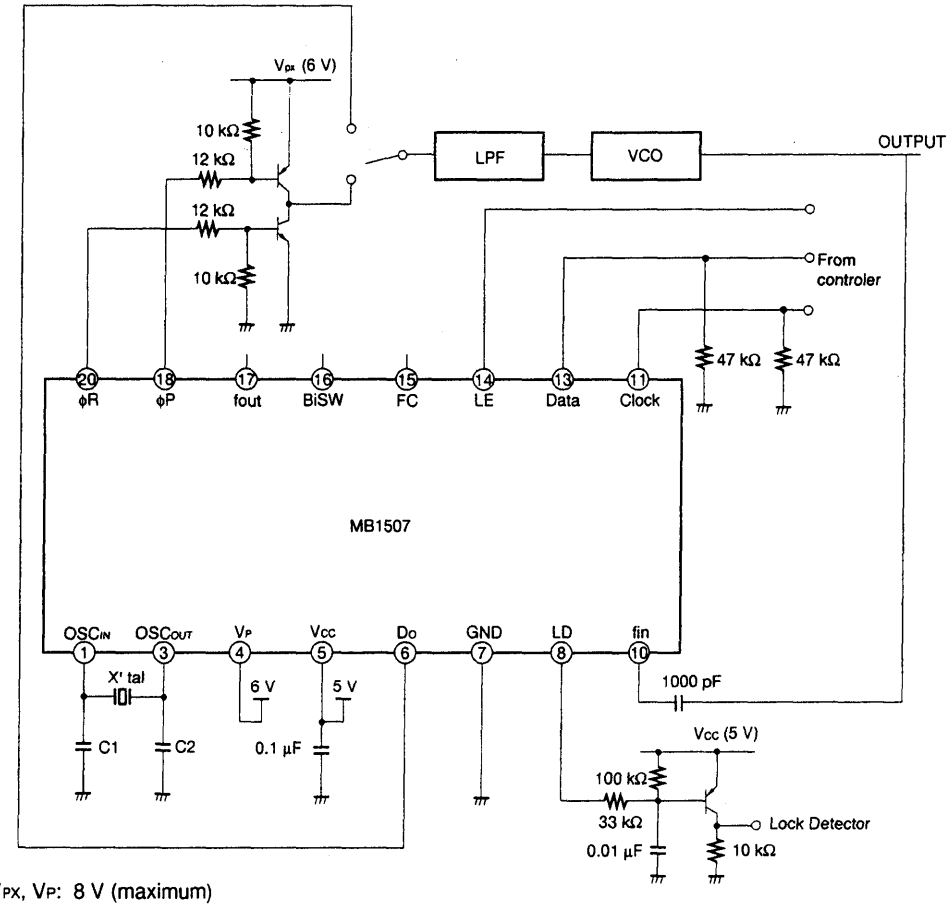
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply current *1		Icc	—	18.0	—	mA
Operating frequency	fin*2	fin	10	—	2000	MHz
	OSCIN	fosc	—	12	20	MHz
Input sensitivity	fin*3	Pfin	−4	—	6	dBm
	OSCIN	Vosc	0.5	—	—	VP-P
H level input voltage	Except fin, OSCIN	VIH	Vcc × 0.7	—	—	V
L level input voltage		VIL	—	—	Vcc × 0.3	V
H level input current	Data, Clock	IIH	—	1.0	—	µA
L level input current		IIL	—	−1.0	—	µA
Input current	OSCI	Iosc	—	±50	—	µA
	LE, FC	ILE	—	−60	—	µA
H level output voltage	Except Do*4, OSCOUT	VOH	4.4	—	—	V
L level output voltage		VOL	—	—	0.4	V
High impedance cutoff current	Do*5, φP	IOFF	—	—	1.1	µA
Output current	Except Do, OSCOUT	IOH	−1.0	—	—	mA
		IOL	1.0	—	—	mA
Analog switch on resistance		RON	—	25	—	Ω

*1: Power supply current measurement conditions: Connection to a crystal with Vcc = 5 V, fIN = 2.0 GHz, fosc = 12 MHz.
*2: AC coupled. Minimum operating frequency is measured with a coupling of 1000 pF.
*3: 50 Ω system
*4: At Vcc = 5 V
*5: VP = Vcc to 8 V, VOOP = GND to 8 V

■ MEASUREMENT CIRCUIT (Prescaler Input Sensitivity Measurement)



■ APPLICATION EXAMPLE



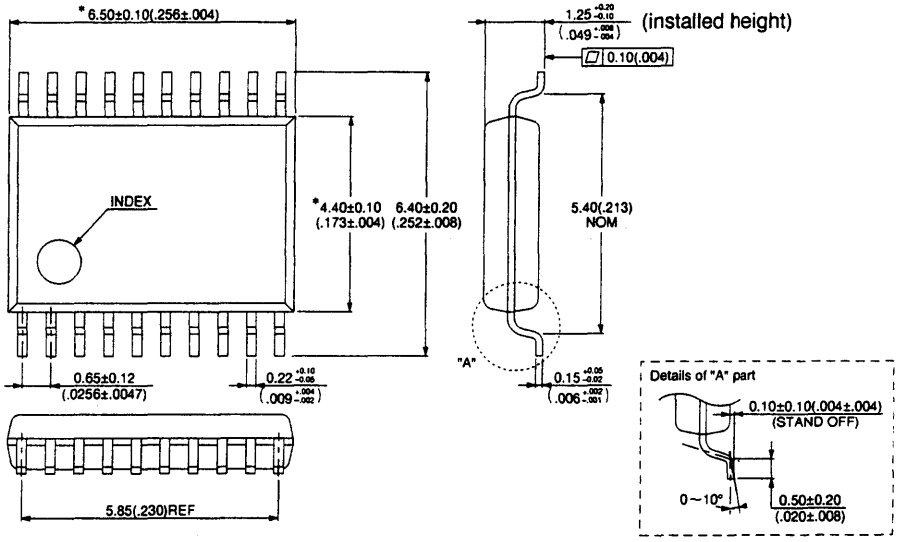
VPX, VP: 8 V (maximum)
C1, C2: determined by crystal oscillator
LE, FC: with pull-up resistor
φP: open-drain output

■ ORDERING INFORMATION

Part number	Package	Remarks
MB1506PFV	20-pin Plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSION

Plastic SSOP, 20 pin
(FPT-20P-M03)



Note: Items with asterisk (*) do not include resin residue.

Dimentions in mm (inches)

4

September 1995
Edition 4.0a

DATA SHEET

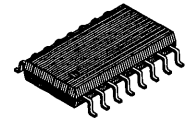
MB1507

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 2.0GHz PRESCALER

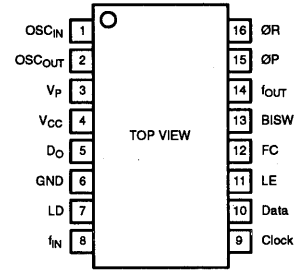
The Fujitsu MB1507 is a single chip serial input PLL frequency synthesizer designed for Broadcast Satelite tuner and cellular telephone applications.
It contains a 2.0 GHz dual modulus prescaler which enables pulse swallow function, and an analog switch to speed up lock up time.
It operates supply voltage of 5.0V typ. and dissipates 18mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: $f_{IN\ MAX}$=2.0GHz ($P_{IN\ MIN}$=–4dBm)
- Pulse swallow function: 128/129 or 256/257
- Low supply current: I_{CC}=18mA typ.
- Serial input 19-bit programmable divider consisting of:
  - Binary 8-bit swallow counter: 0 to 255
  - Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 8 to 16383
  - 1-bit switch counter (SW) Sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic Flat Package (Suffix: –PF)



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



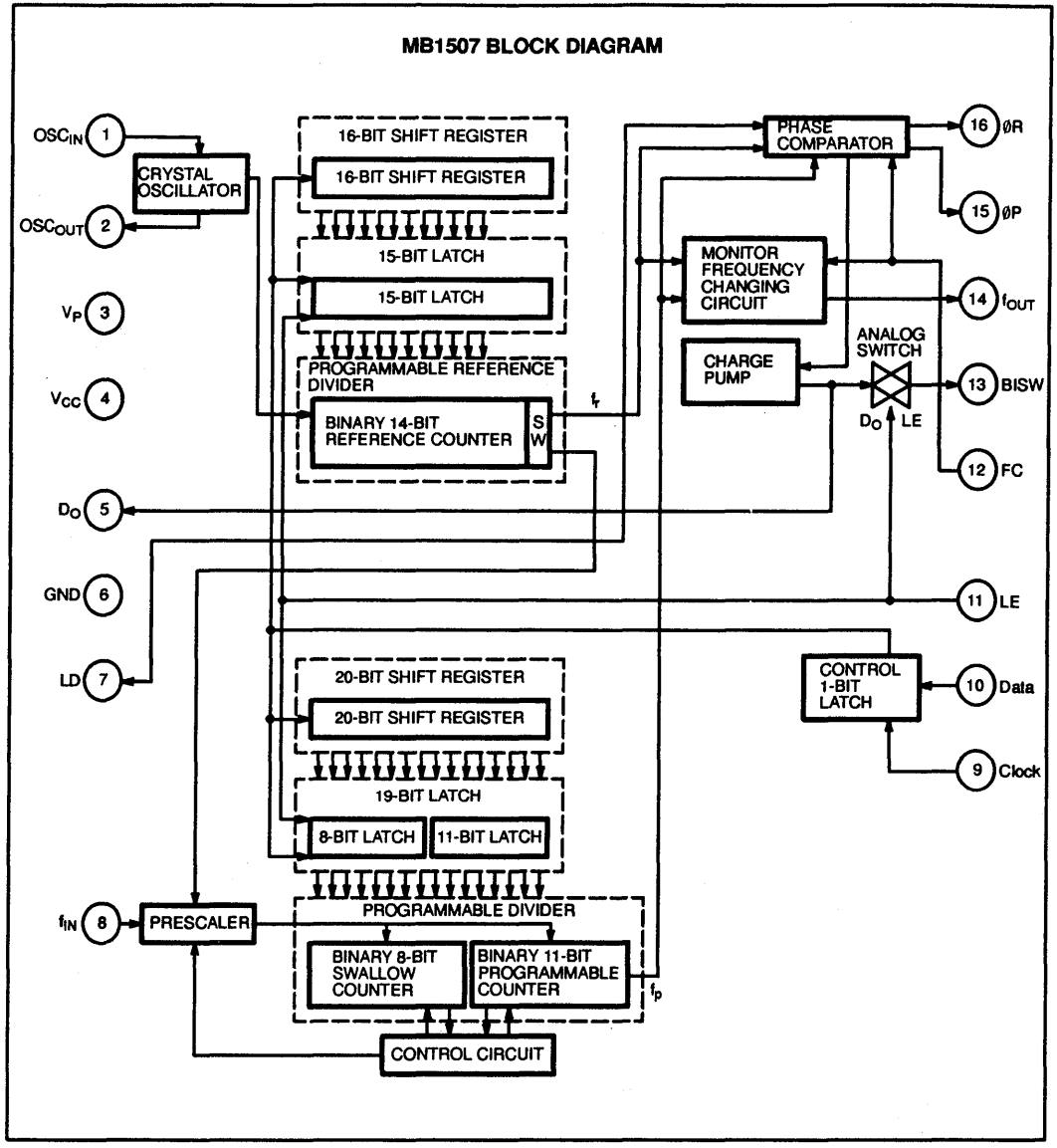
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 8.0	V
Output Current	I_{OUT}	+10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB1507 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	-	Power supply input for charge pump and analog switch.
4	V_{CC}	-	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
6	GND	-	Ground.
7	LD	O	Phase comparator output. Normally the output level is high level. While the phase difference of f_r and f_p exists, the output becomes low level.
8	f_{IN}	I	Prescaler input. The connection with VCO should be AC connection.
9	Clock	I	Clock input for 20-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 19-bit latch.
11	LE	I	Load enable input (with pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phase select input of phase comparator (with pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC pin input signal controls f_{out} pin (test pin) output level, f_r or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump output.
14	f_{OUT}	O	Monitor pin of phase comparator input. f_{out} pin outputs programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
15 16	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 19-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 19-bit latch.

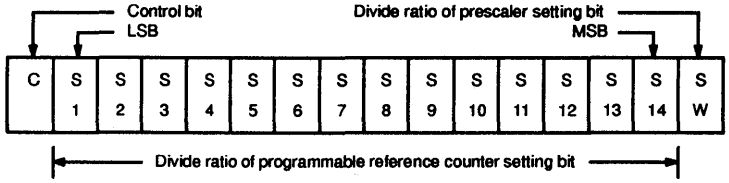
THE DIVIDE RATIO SETTING

$f_{VCO}=[(MxN)+A]xf_{OSC}\div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
M: Preset modulus of external dual modulus prescaler (128 or 256)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 8-bit swallow counter ($0 \leq A \leq 255$, $A < N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



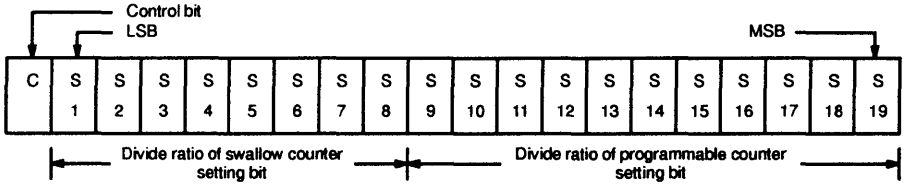
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 128/129
SW=L : 256/257
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 20-bit shift register, 19-bit latch, 8-bit swallow counter and 11-bit programmable counter. Serial 20-bit data format is shown below.



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8-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•
255	1	1	1	1	1	1	1	1

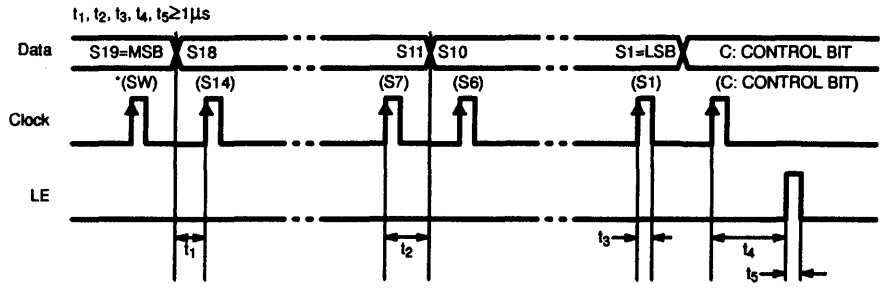
NOTE: Divide ratio: 0 to 255

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 19	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S8: Swallow counter divide ratio setting bit. (0 to 255)
S9 to S19: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets to low level).
Data is input from MSB side.

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data into the shift register.

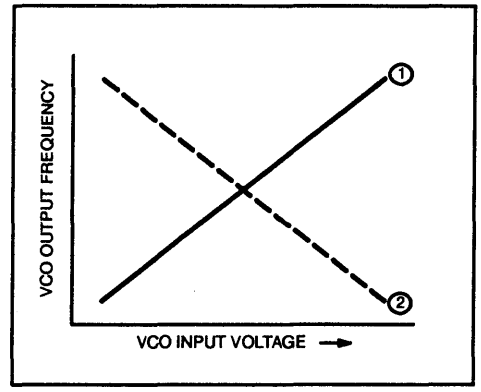
PHASE CHARACTERISTICS

FC pin is provided to change phase polarity of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (ØR, ØP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level.

	FC=H or open				FC=L			
	D_O	ØR	ØP	f_{out}	D_O	ØR	ØP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)

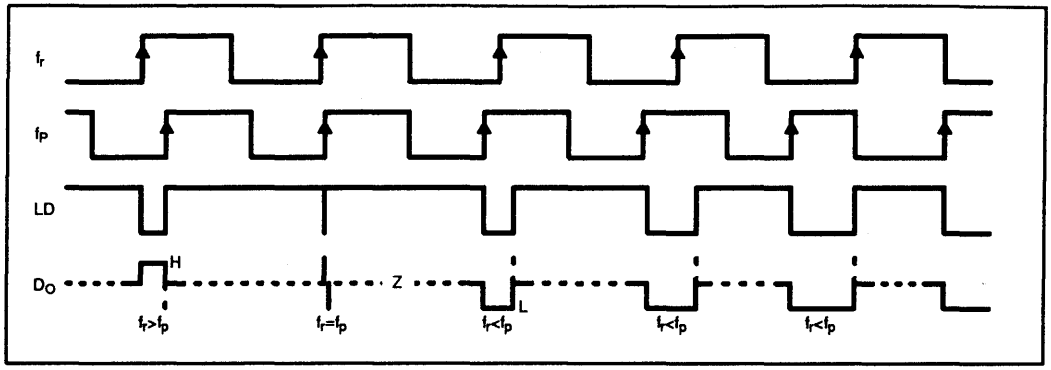
Note: Z=(High impedance)

VCO POLARITY



Depending upon VCO polarity, FC pin should be set accordingly:
When VCO polarity are like ①, FC should be set High or open circuit;
When VCO polarity are like ②, FC should be set Low.

PHASE DETECTOR OUTPUT WAVEFORM (FC=High)



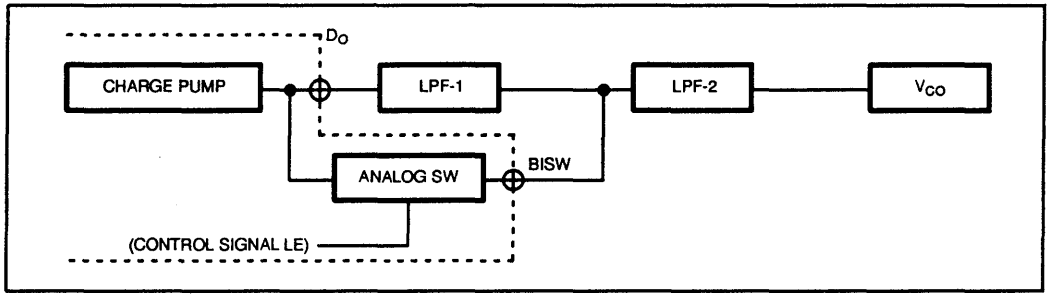
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) is connected to BISW pin. When the analog switch is OFF, BI-SW pin is set to high-impedance state.

LE	Analog Switch
H(Changing the divide ratio of internal prescaler)	ON
L(Normal operating mode)	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input Voltage	V_I	GND	—	V_{CC}	V
Operating Temperature	T_A	-40	—	85	°C

HANDLING PRECAUTIONS

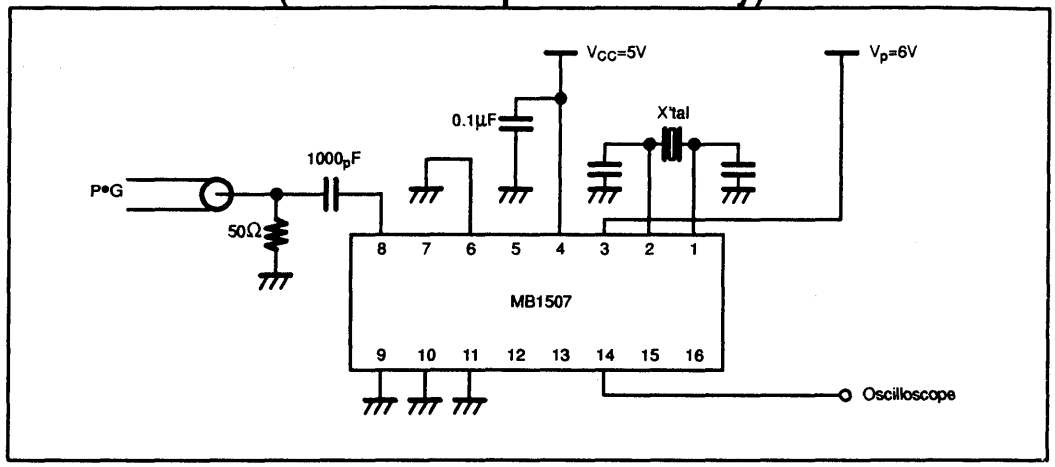
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

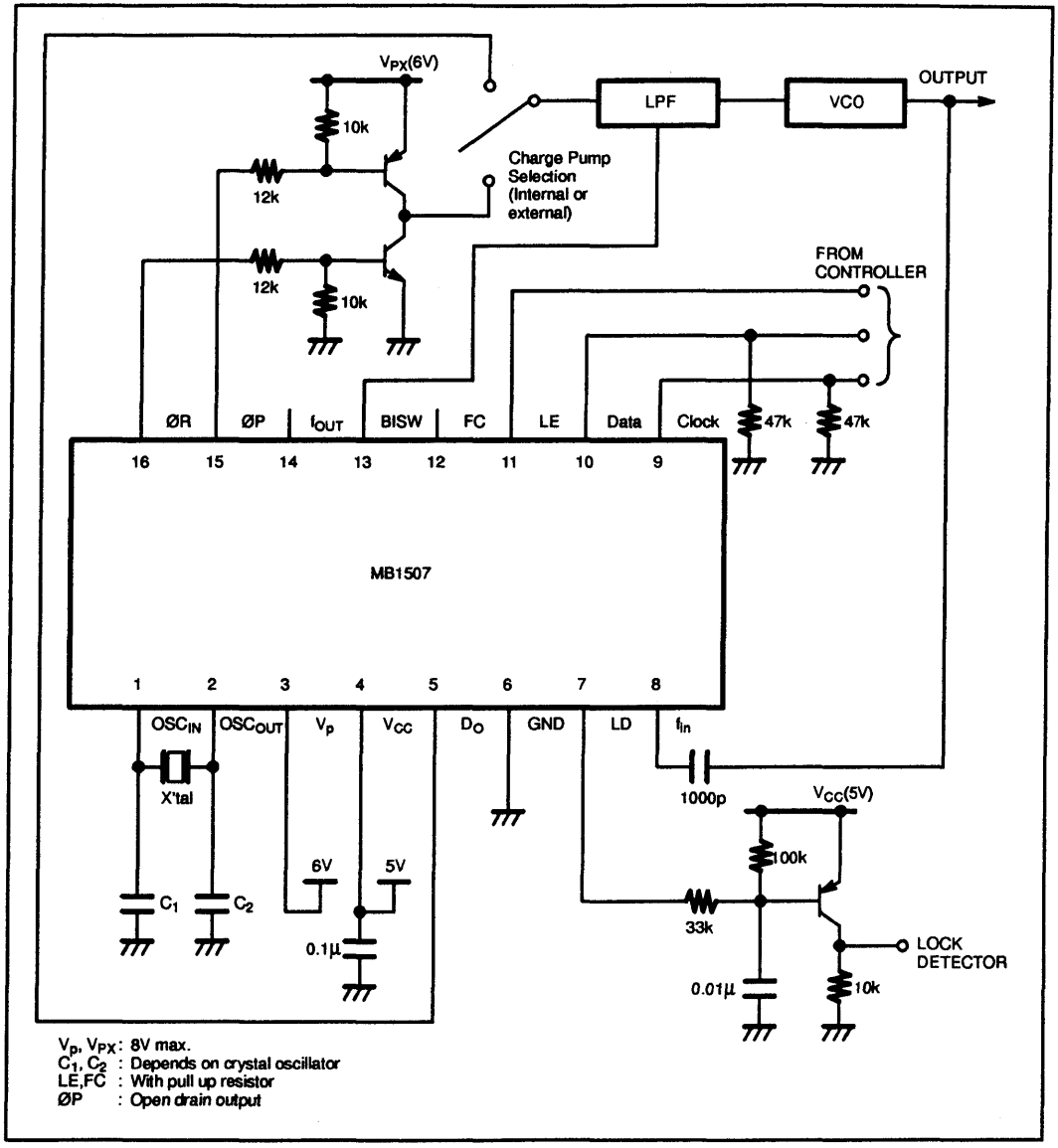
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1	—	18.0	—	mA
Operating Frequency	f_{in}	f_{in}	Note 2	10	—	2000	MHz
	OSC_{IN}	f_{OSC}	—	—	12	20	MHz
Input Sensitivity	f_{in}	P_{fin}	50Ω	−4	—	6	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	—	V_{CC}x0.7	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}	—	—	1.0	—	µA
Low-level Input Current		I_{IL}	—	—	−1.0	—	µA
Input Current	OSC_{IN}	I_{OSC}	—	—	±50	—	µA
	LE, FC	I_{LE}	—	—	−60	—	µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4	—	—	V
Low-level Output Current		V_{OL}		—	—	0.4	V
High Impedance Cutoff Current	D_O, ØP	I_{OFF}	V_P=V_{CC} to 8V V_{OOP}=GND to 8V	—	—	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}	—	−1.0	—	—	mA
		I_{OL}	—	1.0	—	—	mA
Analog Switch On Resistance		R_{ON}	—	—	25	—	Ω

NOTE 1: f_{in}=2.0GHz, f_{OSC} =12MHz X'tal V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

TEST CIRCUIT (Prescaler Input Sensitivity)



TYPICAL APPLICATION EXAMPLE

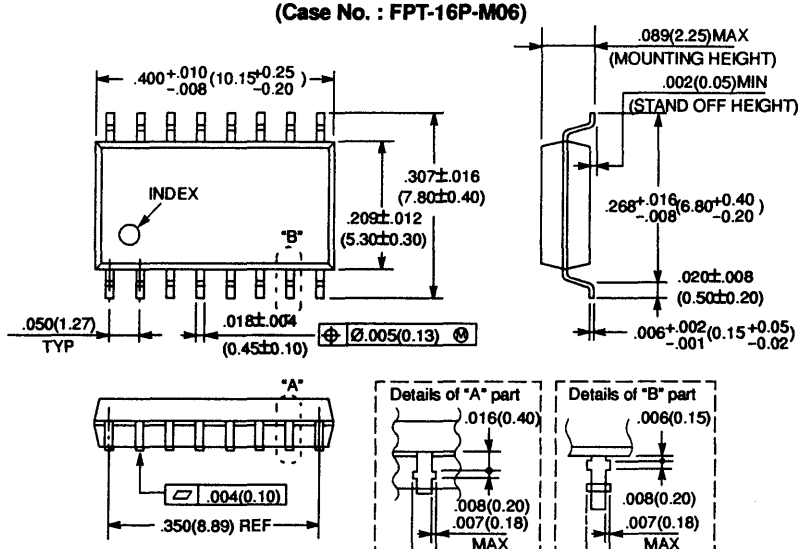


V_P, V_{PX}: 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With pull up resistor
ØP : Open drain output

4

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-16P-M06)



Dimensions in inches (millimeters)

Sept. 1995
Edition 2.0a

DATA SHEET

FUJITSU

MB1508

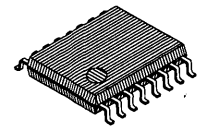
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER ON CHIP 2.5 GHz PRESCALER

DESCRIPTION

The Fujitsu MB1508 with an on chip 2.5 GHz dual modulus prescaler is a serial input PLL (Phase Locked Loop) frequency synthesizer with pulse swallow function. It is well suited for BS tuner, CATV system, and TV tuner applications.

It operates with a supply voltage of 5.0V typ. and dissipates 16mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.



Plastic Package
FPT-20P-M01

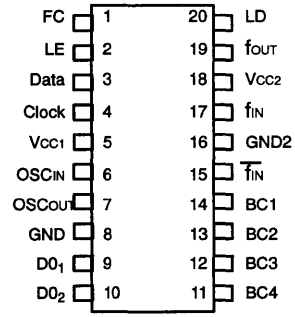
4

FEATURES

- Power supply voltage: V_{CC} = 4.5 to 5.5V
- High operating frequency: f_{IN} = 2.5 GHz (P_{IN} = –4dBm)
- 2.5 GHz dual modulus prescaler: P = 256/272, 512/528
- Low supply current: I_{CC} = 16mA typ.
- Programmable reference divider consisting of:
  Binary 2-bit programmable reference counter (R = 256, 512, 1024, 2048)
- Programmable divider consisting of:
  Binary 5-bit swallow counter (A = 0 to 31)
  Binary 12-bit programmable counter (N = 32 to 4095)
- Wide operating temperature: –40°C to +85°C
- Plastic 20-pin Flat Package (Suffix: —PF)

Pin Assignment

(TOP VIEW)



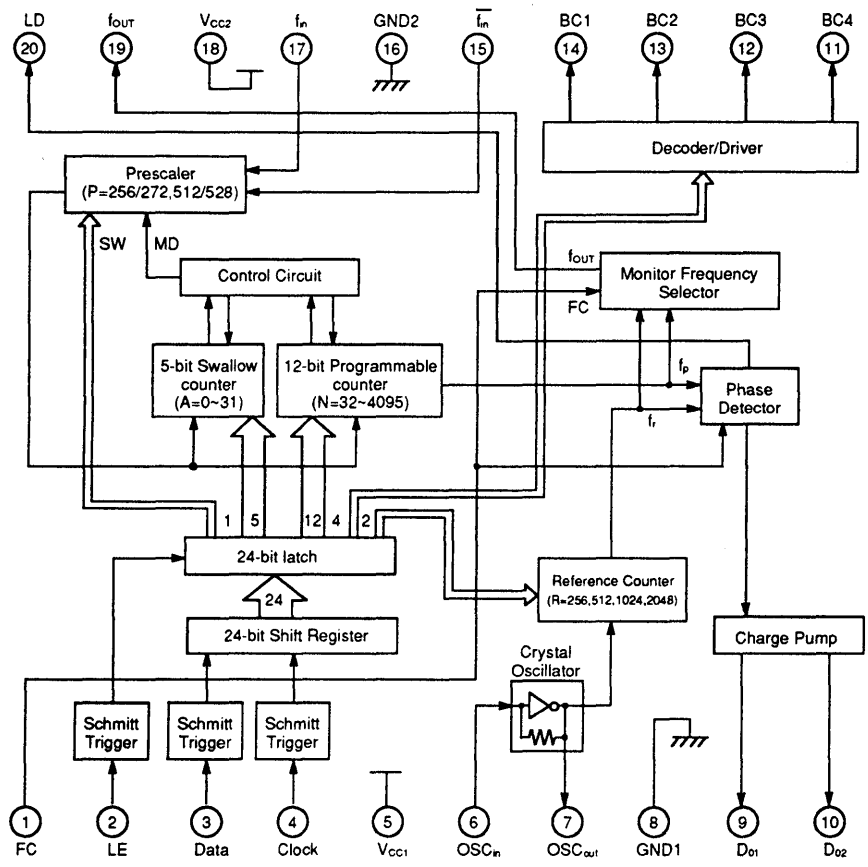
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Output Voltage	V_O	–0.5 to V_{CC} +0.5	V
Output Current	I_O	± 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1508 BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	FC	I	Phase select input pin of the phase detector. This pin involves an internal pull up resistor. When this pin is low, characteristics of the charge pump and phase detector can be reversed. This input also selects f_{OUT} pin output level, either fr or fp. Please see on page 6.
2	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch.
3	Data	I	Serial data of binary code input pin. This pin involves a schmitt trigger circuit.
4	Clock	I	Clock input pin of the 24-bit shift register. This pin involves a schmitt trigger circuit. *On rising edge of the clock shifts one bit of the data into the shift register.*
5	V_{CC1}	–	PLL power supply voltage input pin.
6 7	OSC_{IN} OSC_{OUT}	I O	Oscillator input pin. Oscillator output pin. A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.
8	GND1	–	PLL ground pin.
9 10	D_{O1} D_{O2}	O O	Charge pump output pins. Phase characteristics can be reversed depending upon FC pin input level.
11 12 13 14	BC4 BC3 BC2 BC1	O O O	Band switching output pins. (Open-collector output) Output is controlled by a band bit data, individually. BCX-bit=H : BCX output transistor is ON. BCX-bit=L : BCX output transistor is OFF. (X=1 to 4)
15	$\overline{f_{in}}$	I	Complementary input pin of f_{in}. Please connect to GND through a capacitor.
16	GND2	–	Prescaler ground pin.
17	f_{in}	I	Prescaler input pin, This signal is AC coupled.
18	V_{CC2}	–	Prescaler power supply voltage input pin.
19	f_{OUT}	O	Monitor pin of the phase detector input. f_{OUT} pin outputs either of the programmable reference divider output frequency fr or programmable divider output frequency fp depending upon the FC pin input level.
20	LD	O	Phase detector output pin. Normally this pin outputs high. While the phase difference between fr and fp exists, this pin outputs low.

FC pin	fout output signal
H	fr
L	fp

FUNCTIONAL DESCRIPTIONS

DIVIDE RATIO SETTING

Divide ratio can be set using the following equation:

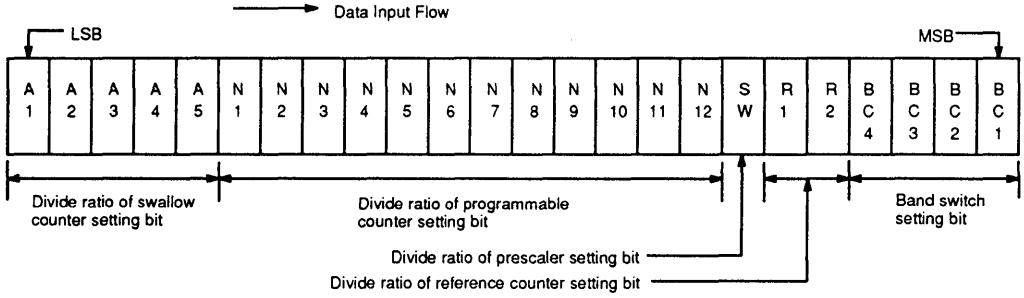
$f_{vco} = \{(P \times N) + (16 \times A)\} \times f_{osc} + R$

f_{vco}: Output frequency of an external voltage controlled oscillator (VCO)
P: Preset divide ratio of an internal dual modulus prescaler (256 or 512)
N: Preset divide ratio of binary 12-bit programmable counter (32 to 4095)
A: Preset divide ratio of binary 5-bit swallow counter (0 to 31)
f_{osc}: Reference oscillator frequency
R: Preset divide ratio of reference counter (256,512,1024,2048)

SERIAL DATA I NPUT

On rising edge of the clock shifts one bit of the data into the shift register.
When the load enable is high, the data stored in the shift register is transferred to the latch.

24 bit of serial data formit is shown below.



5-bit swallow counter divide ratio (A1 to A5)

Divide ratio A	A5	A4	A3	A2	A1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
:	:	:	:	:	:
31	1	1	1	1	1

12-bit programmable counter divide ratio (N1 to N12)

Divide ratio	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
32	0	0	0	0	0	0	1	0	0	0	0	0
33	0	0	0	0	0	0	1	0	0	0	0	1
34	0	0	0	0	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:	:	:	:
4095	1	1	1	1	1	1	1	1	1	1	1	1

FUNCTIONAL DESCRIPTIONS

Reference counter divide ratio (R1 to R2)

Divide ratio	R 2	R 1
256	0	0
512	0	1
1024	1	0
2048	1	1

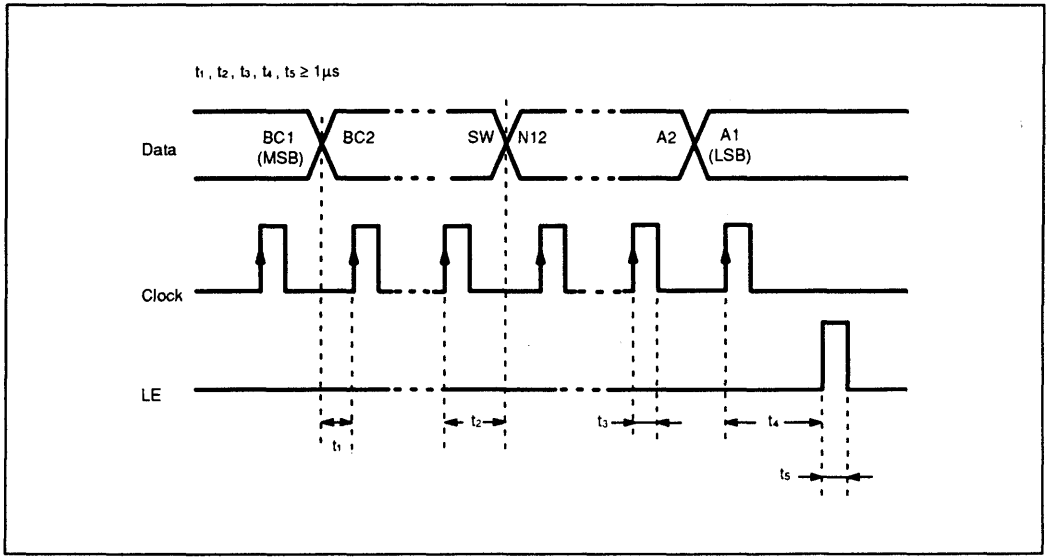
Prescaler divide ratio (SW)

When divide ratio of prescaler setting bit is high, divide ratio of 256/272 is selected.
When divide ratio of prescaler setting bit is low, divide ratio of 512/528 is selected.

Band Switch Setting (BC1 to BC4)

When band switch setting bit is high, output is ON.
When band switch setting bit is low, output is OFF.

SERIAL DATA INPUT TIMING



Note: On rising edge of the clock shifts one bit of the data into the shift register.
When LE is high, the data stored the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

FC pin selects the phase of the phase detector. Phase characteristics (chage pump output) can be reversed depending upon the FC pin input level. Monitor pin (fout) output level is selected by the FC pin input level as well.

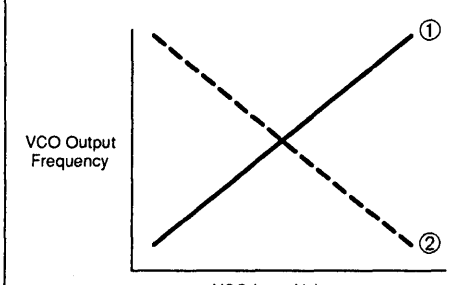
	FC = H (or open)		FC = L	
	D_{o1}, D_{o2}	fout	D_{o1}, D_{o2}	fout
fr > fp	H	Outputs programmable reference divider output frequency fr.	L	Outputs programmable divider output frequency fp.
fr = fp	Z		Z	
fr < fp	L		H	

Note:
Z: High-impedance

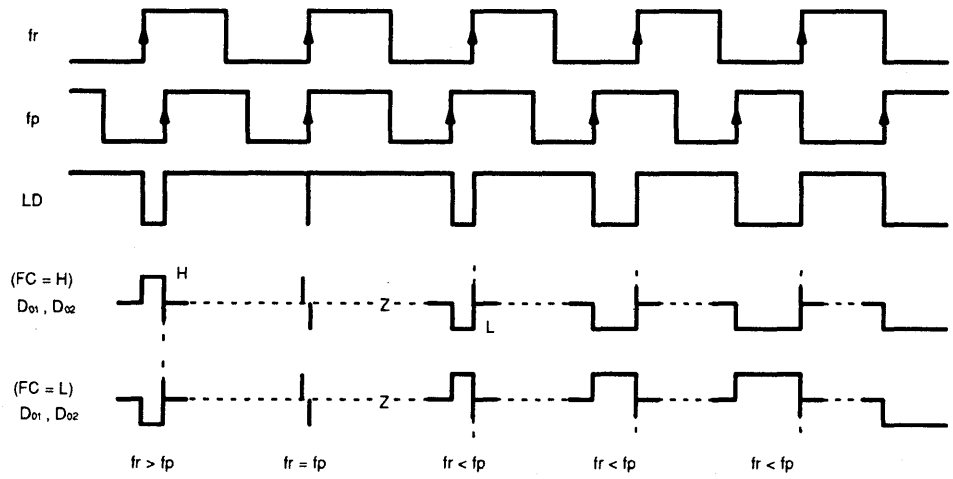
Depending upon the VCO polarity, FC pin should be set accordingly.

When VCO polarity is like 1,
FC should be set high or open.
When VCO polarity is like 2,
FC should be set low.

VCO POLARITY



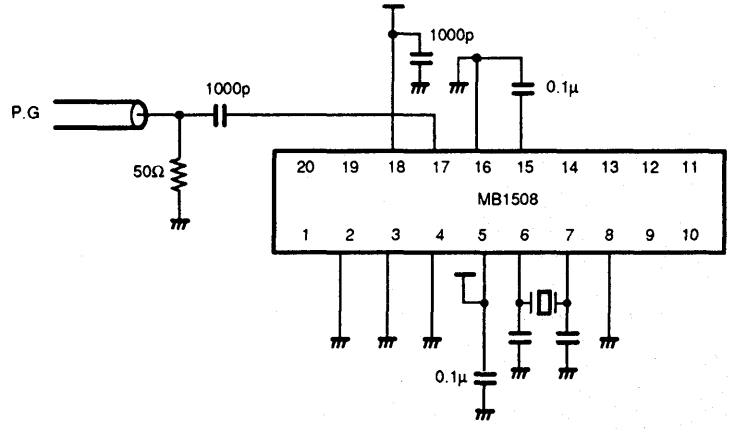
PHASE DETECTOR WAVEFORM



Note: Phase difference detection range : -2π to $+2\pi$

Spike shape depends on the charge pump characteristics.
The spike is output to diminish the dead band.

TEST CIRCUIT (FOR PRESCALER INPUT SENSITIVITY)



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	–40	–	+85	°C

HANDLING PRECAUTIONS

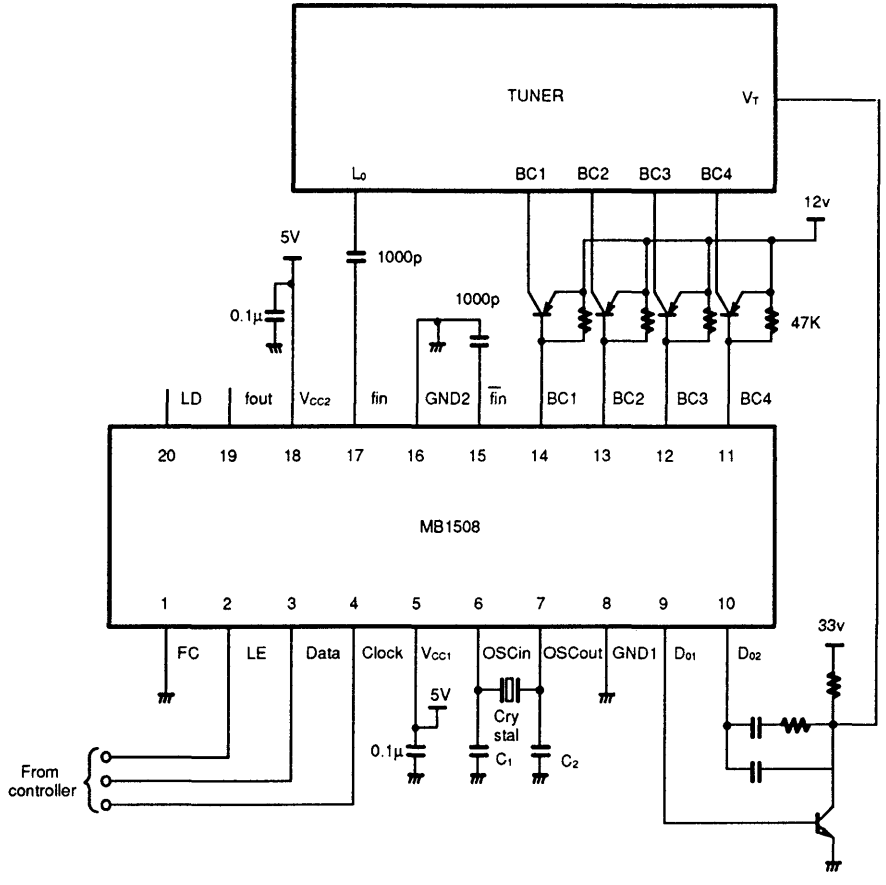
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Power Supply Current		I_{CC}	Note 1	—	16.0	—	mA
Operating Frequency	f_{in}	f_{in}	Note2	10	—	2500	MHz
	OSC_{IN}	f_{OSC}	—	—	4	10	
Input Sensitivity	f_{in}	P_{fin}	2300 to 2500MHz	–4	—	6	dBm
			1900 to 2300MHz	–7	—	6	
			10 to 1900MHz	–10	—	6	
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	—	V_{CC}x 0.7+0.4	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	V_{CC}x0.3–0.4	
High-level Input Current	Data Clock LE	I_{IH}	—	—	1.0	—	µA
Low-level Input Current		I_{IL}	—	—	–1.0	—	
	FC	I_{ILFC}	—	—	–60	—	
Input Current	OSC_{IN}	I_{OSC}	—	—	+50	—	
High-level Output Voltage	Except D_O and BC1 to BC4	V_{OH}	V_{CC} = 5.0 V	4.4	—	—	V
Low-level Output Voltage		V_{OL}		—	—	0.4	
High Impedance Cutoff Current	D_{O1}, D_{O2} BC1 to BC4	I_{OFF}	—	—	—	1.1	µA
High-level Output Current	Except D_O and BC1 to BC4	I_{OH}	—	–1.0	—	—	mA
Low-level Output Current		I_{OL}	—	1.0	—	—	
Withstand Output Voltage	BC1 to BC4	V_B	—	—	—	12	V

NOTE: 1: f_{in} = 2.5GHz, OSC_{IN}=4.0MHz, V_{cc}=5.0V. Inputs are grounded and outputs are open.
2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

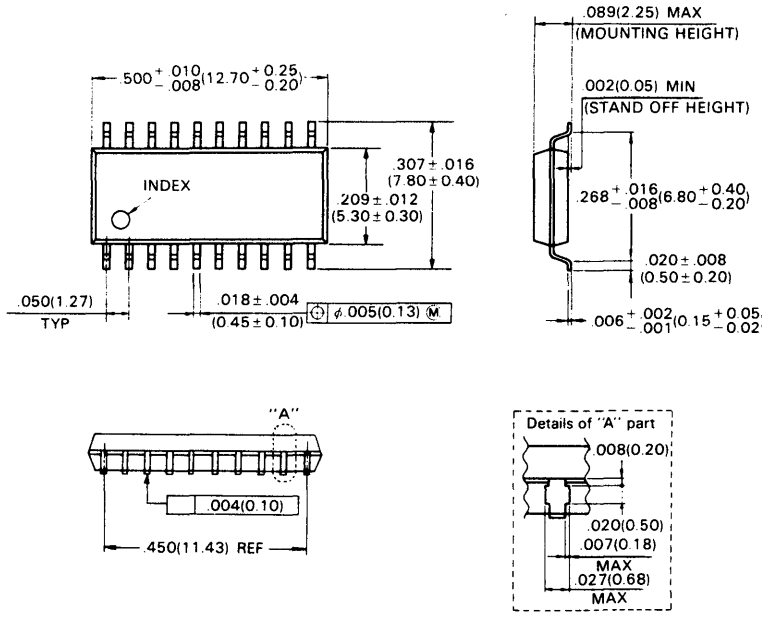
MB1508 APPLICATION CIRCUIT



C_1, C_2 : depends on the crystal oscillator.
FC : with internal pull up resistor.

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



Dimensions in
inches (millimeters)

Sept. 1995
Edition 3.0a

FUJITSU

DATA SHEET

MB1509

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

4

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 400MHz PRESCALER

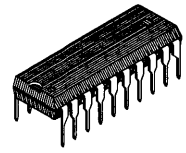
The Fujitsu MB1509 is a 400MHz dual serial input PLL (Phase Locked) frequency synthesizer designed for cordless telephone application.

The MB1509 has two PLL circuits on a single chip: one for transmit and the other for reception. Separate power supply pins are provided for the transmit and reception PLL circuits. Transmit PLL contains a low sensitivity charge pump for ease of modulation and reception PLL contains a high sensitivity charge pump for faster lock up time.

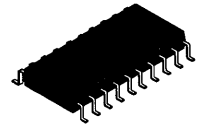
The MB1509 incorporates two 400 MHz dual modulus prescalers to enable implemention of a pulse swallow function.

It operates supply voltage of 3.0V typ. and dissipates 8mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: fin = 400MHz
- Low power supply voltage: V_{CC} = 2.7 to 5.5V
- Low power supply current: I_{CC} = 8mA typ, @3V.
- Wide operating temperature: T_A = –40 to 85°C
- Two charge pumps
  Low sensitivity charge pump for transmit
  High sensitivity charge pump for reception
- Plastic 20-pin dual in line package (Suffix: -P)
  Plastic 20-pin flat package (Suffix: -PF)

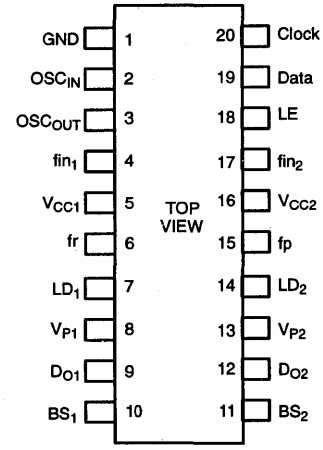


PLASTIC PACKAGE
DIP-20P-M02



PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT



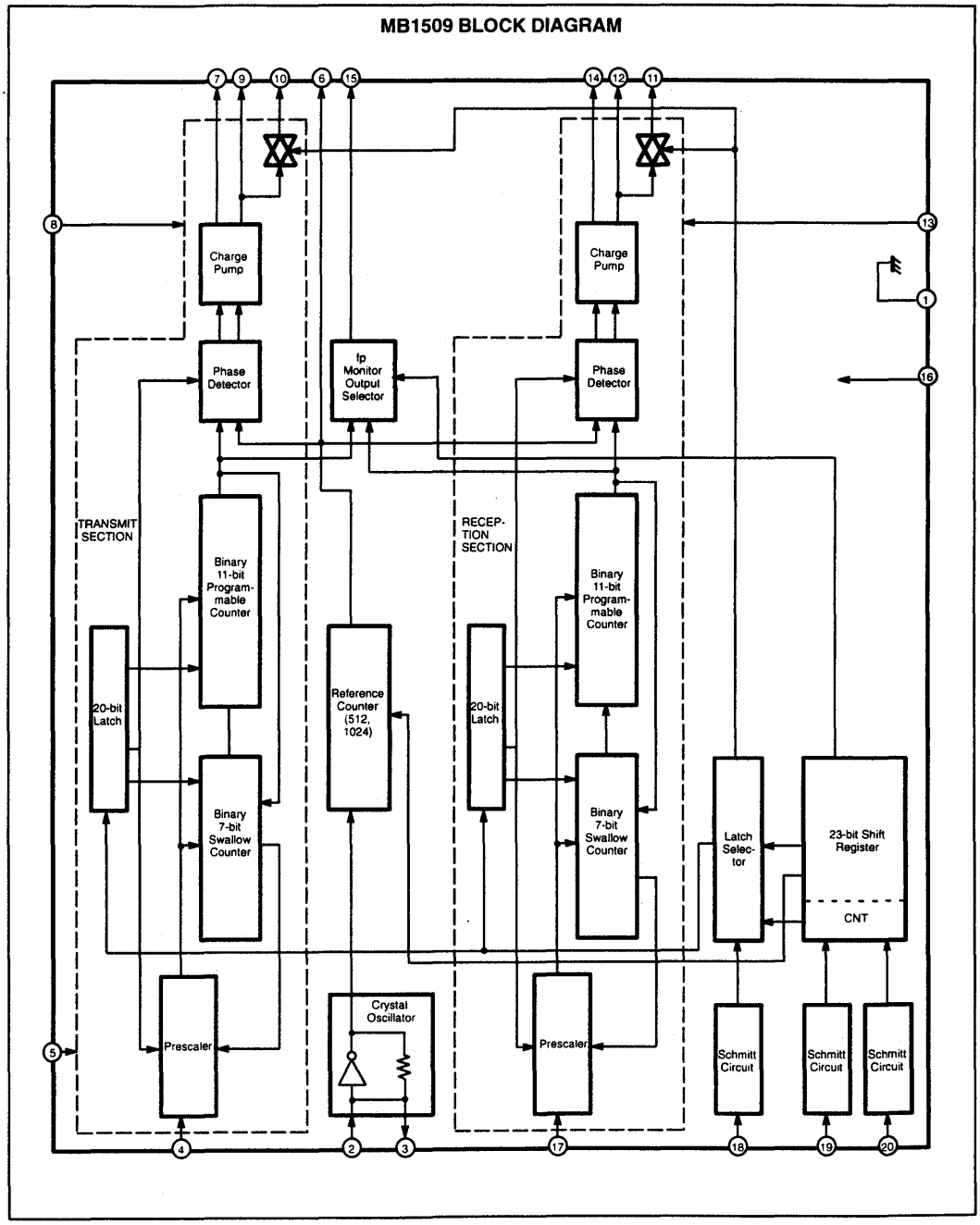
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
	V_P	V_{CC} to 10.0	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1509 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

TRANSMIT/RECEPTION BLOCK

- 20-bit latch
- Programmable divider consisting of:
  –Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  –Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Phase detector with phase polarity change function
- 400MHz dual modulus prescaler (Divide ratio: 32/33, 64/65)
- Charge pump

COMMON BLOCK

- 23-bit shift register
- Programmable divider consisting of:
  –Reference counter (Divide ratio: 512, 1024)
  –(Divide frequency = 25kHz, 12.5kHz (Crystal oscillator frequency = 12.8MHz)
- Crystal oscillator
- fp monitor output selector
- Latch selector
- Schmitt circuits
- Analog switches

PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground</td></tr>
<tr><td>2
3</td><td>OSC_{IN}
OSC_{OUT}</td><td>I
O</td><td>Oscillator input pin
Oscillator output pin
A crystal is connected between the OSC_{IN} pin and the OSC_{OUT} pin.</td></tr>
<tr><td>4</td><td>fIN_1</td><td>I</td><td>Prescaler input pin of transmit section
The connection with VCO should be an AC connection.</td></tr>
<tr><td>5</td><td>V_{CC1}</td><td>–</td><td>Power supply voltage input pin of transmit section
When the power is OFF, the latched data of the transmit section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of transmit section
<table><tr><th>Condition</th><th>LD Pin Output Level</th></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>8</td><td>V_{P1}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of transmit section</td></tr>
<tr><td>9</td><td>D_{O1}</td><td>O</td><td>Charge pump output pin of transmit section
Phase characteristics of the phase detector can be reversed depending upon the FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of transmit section
Usually this pin is in the high-impedance state. When SW is ON (LE = high), the charge pump output is connected to this pin.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of reception section
Usually this pin is in the high-impedance state. When SW is ON (LE = high), the charge pump output is connected to this pin.</td></tr>
<tr><td>12</td><td>D_{O2}</td><td>O</td><td>Charge pump output pin of reception section
Phase characteristics of the phase detector can be reversed depending upon the FC-bit setting.</td></tr>
<tr><td>13</td><td>V_{P2}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of reception section</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detect signal output pin of reception section
<table><tr><th>Condition</th><th>LD Pin Output Level</th></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output
This pin outputs the divided frequency of the transmit section or the reception section, depending upon the FP bit setting.
<table><tr><th>FP Bit</th><th>Output</th></tr><tr><td>H</td><td>Transmit section (fp1)</td></tr><tr><td>L</td><td>Reception section (fp2)</td></tr></table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	V_{CC2}	–	Power supply voltage input pin for reception section, programmable reference divider, shift register, and crystal oscillator When the power is OFF, the latched data of the reception section and the reference counter is cancelled.
17	fin_2	I	Prescaler input pin of reception section The connection with VCO should be an AC connection.
18	LE	I	Load enable input pin This pin involves a Schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on the control data. At this moment, the charge pump output signal is output from the BS pin since the internal analog switch changes to ON.
19	Data	I	Serial data input pin of 23-bit shift register This pin involves a Schmitt trigger circuit. The stored data in the shift register is transferred to either the transmit section or the reception section depending upon the control data. Control Bit Data: H → Destination of Data: Latch of transmit section Control Bit Data: L → Destination of Data: Latch of reception section
20	Clock	I	Clock input pin of 23-bit shift register This pin involves a Schmitt trigger circuit. On the rising edge of the clock, one bit of data shifts into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \ (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)

M: Preset divide ratio of dual modulus prescaler (32 or 64)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillator frequency

R: Preset divide ratio of reference counter (512 or 1024)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins, Data pin, Clock pin, and LE pin. The programmable divider of the transmit section and the programmable divider of the reception section are controlled individually.
Serial data of binary data is input into the Data pin.
On the rising edge of the clock, one bit of serial data shifts into the shift register. When the load enable signal is high, the data stored in the shift register is transferred to either the latch of the transmit section or the latch of the reception section, depending upon the control bit data setting.

Control Data	Destination of Serial Data
H	Latch of transmit section
L	Latch of reception section

SHIFT REGISTER CONFIGURATION

Control bit

LSB

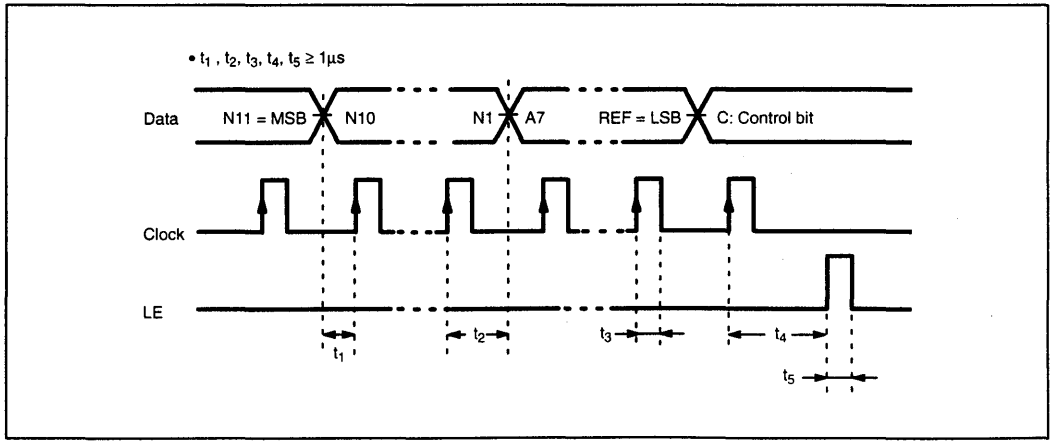
Data Flow →

MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
C	R	F	P	F	A	A	A	A	A	A	A	N	N	N	N	N	N	N	N	N	N	N
N	E	P	R	C	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	9	10	11
T	F		E																			

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
PRE : Divide ratio of the prescaler setting bit (32/33 or 64/65)
FP : Output of the programmable divider control bit (fp1 or fp2)
REF : Divide ratio of the reference counter setting bit (512 to 1024)
CNT : Control bit

SERIAL DATA INPUT TIMING



On the rising edge of the clock, one bit of the data shifts into the shift register.

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 16 is prohibited
Divide ratio (N) range = 16 to 2047

4

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

PRE : DIVIDE RATIO (P) OF THE PRESCALER SETTING BIT
H = 32/33
L = 64/65

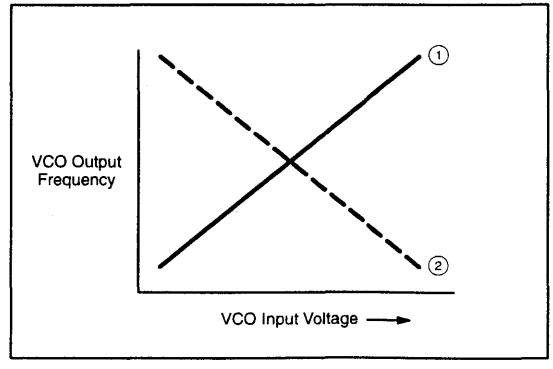
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H = 512 (fr = 25.0 kHz)
L = 1024 (fr = 12.5 kHz)

FP : OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable divider output frequency (fp1) of transmit section
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of reception section

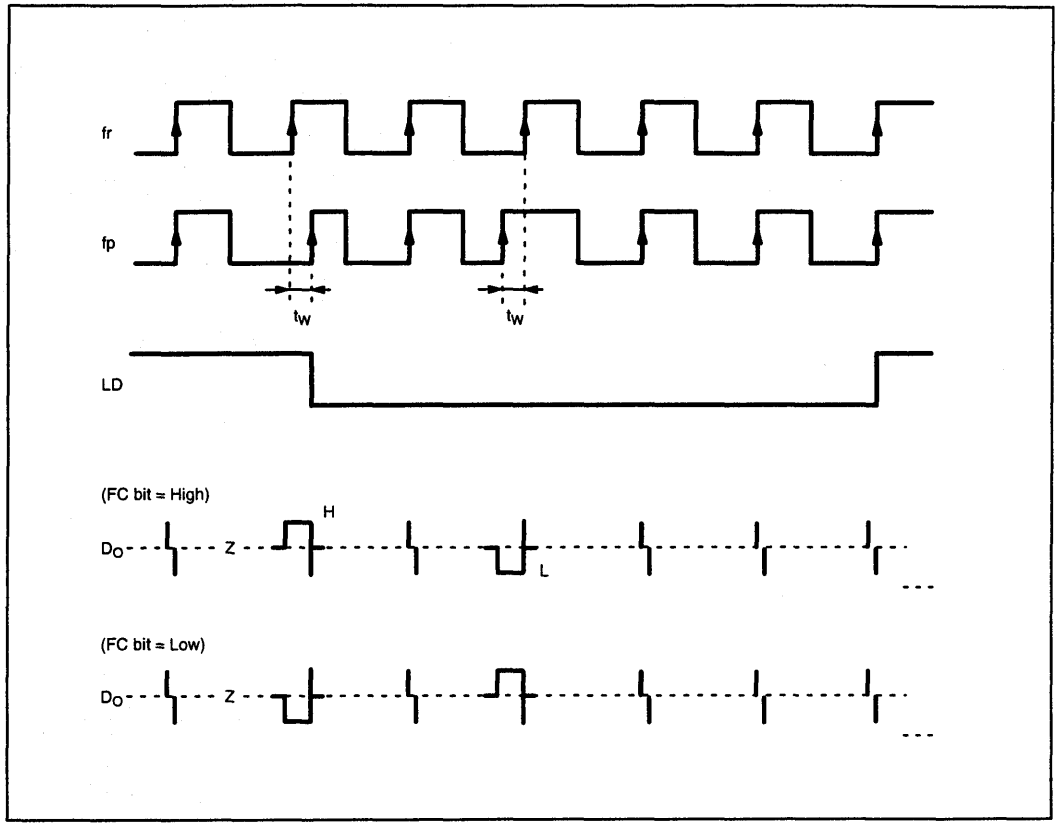
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: Z = High-impedance
Depending upon the VCO polarity, the FC bit should be set.



PHASE DETECTOR OUTPUT WAVEFORM



Note:
- Phase difference detection range = -2π to $+2\pi$
- LD output becomes low when the phase difference is t_W or more.
  LD output becomes high when the phase difference less than t_W is repeated 3 times or more
  (e. g. t_W = 625 to 1250 ns, foscin = 12.8 MHz).
- Spike appearance depends on the charge pump characteristics. The spike is output to diminish the dead band.
- When fr > fp or fr < fp, a spike might not generate depending upon the VCO characteristics.

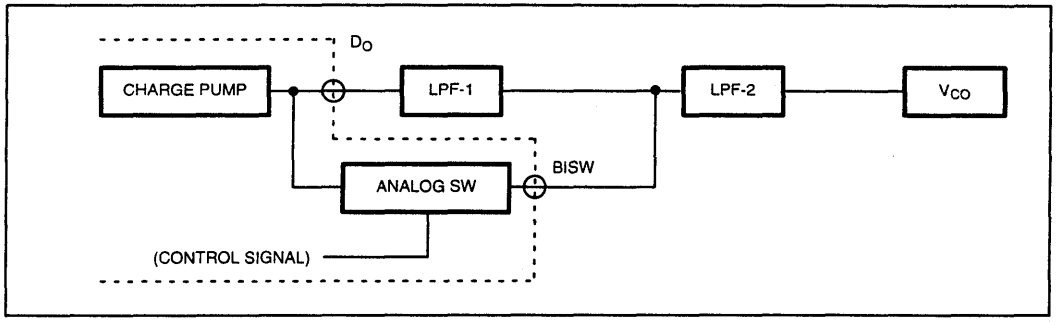
ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, the BS1 and BS2 pins output the charge pump output (D_{01}, D_{02}). When the analog switch is OFF, the BS pin is set to high impedance.

	Control Data = H Divide ratio of transmit section is set		Control Data = L Divide ratio of reception section is set	
	LE = H	LE = L	LE = H	LE = L
Analog switch of transmit section	ON	OFF	OFF	OFF
Analog switch of reception section	OFF	OFF	ON	OFF

4

When an analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce the LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
	V_P	V_{CC}	–	8.0	V	—
Input Voltage	V_{IN}	GND	–	V_{CC}	V	—
Operating Temperature	T_A	–40	–	+85	°C	—

HANDLING PRECAUTIONS

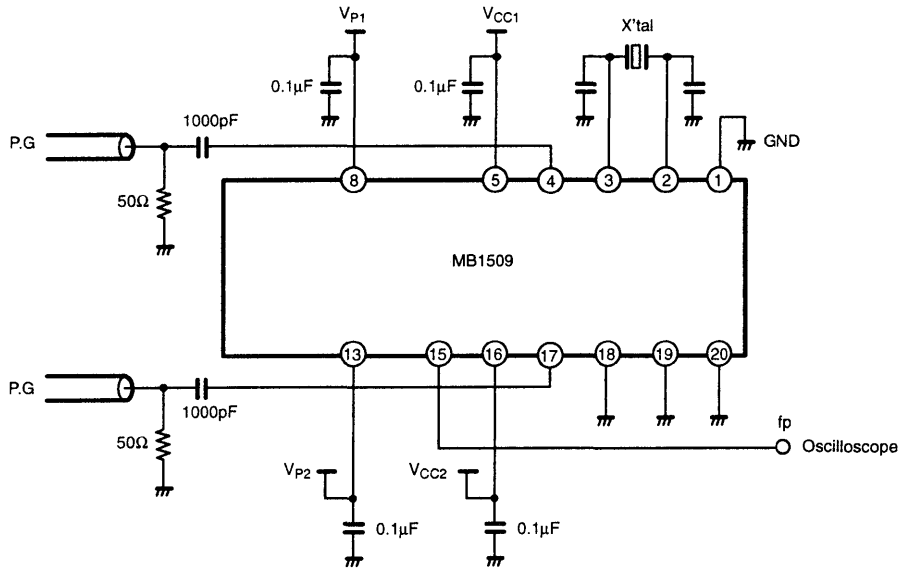
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

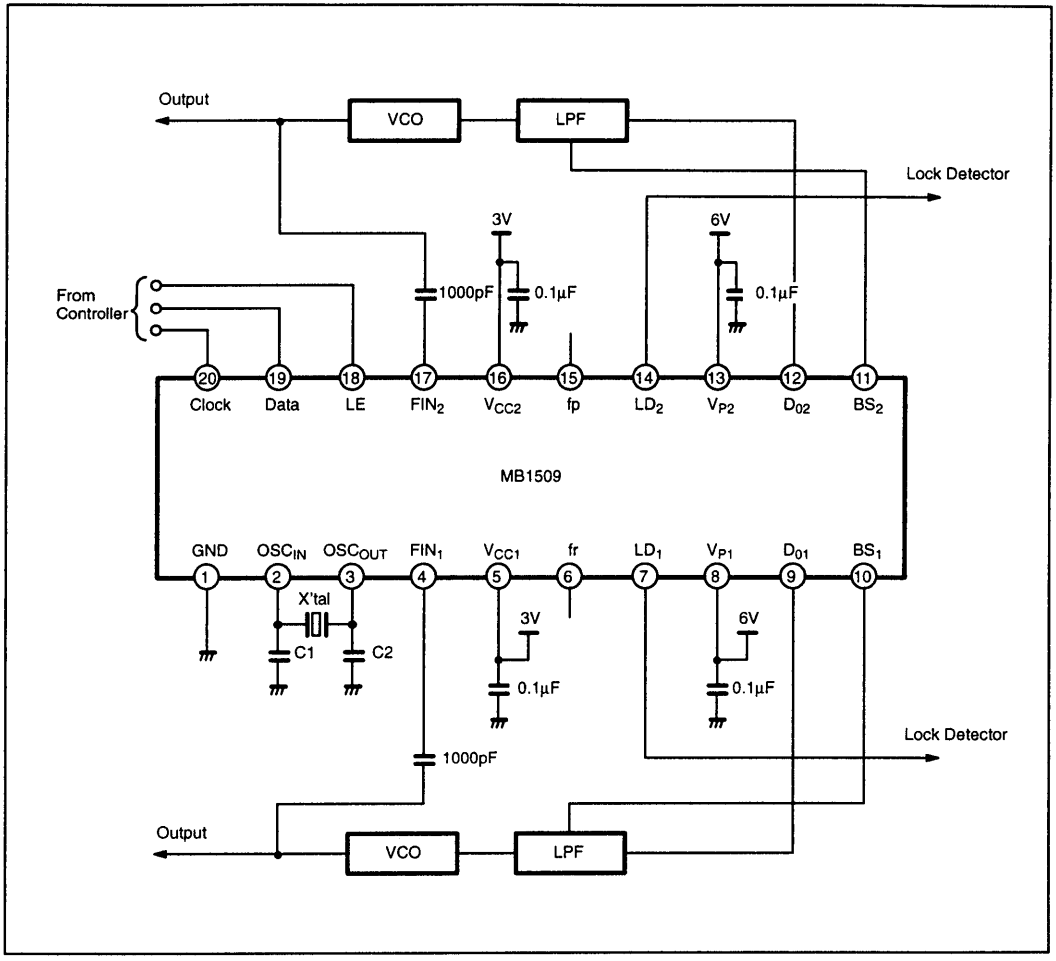
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current*		I_{CC1}	Reception section is active.	–	4.0	–	mA
		I_{CC2}	Transmit/reception section are active.	–	8.0	12.0	
Operating Frequency**	fin	fin1	P = 64/65	10	–	400	MHz
		fin2	P = 32/33	10	–	200	
	OSC_{IN}	f_{OSC}		–	12.8	20	
Input Sensitivity	fin	Pfin	V_{CC} = 2.7 to 4.0V, 50Ω	–10	–	0	dBm
			V_{CC} = 4.0 to 5.5V, 50Ω	–4	–	2	
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High-impedance Cutoff Current	D_O	I_{OFF}	V_P = V_{CC} to 8.0V	–	–	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	D_{O1}	I_{OH}	V_P = 6V	–	–1	–	
		I_{OL}	V_{CC} = 3V	–	12	–	
	D_{O2}	I_{OH}	V_P = 6V	–	–3	–	
		I_{OL}	V_{CC} = 3V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	50	–	Ω

Notes: *: fin = 400MHz, OSC_{IN} = 12.8MHz, V_{CC1} = V_{CC2} = 3.0V. The remaining input pins are grounded and output pins are open.
**: AC coupling. Minimum operating frequency is measured with capacitor 1000pF.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



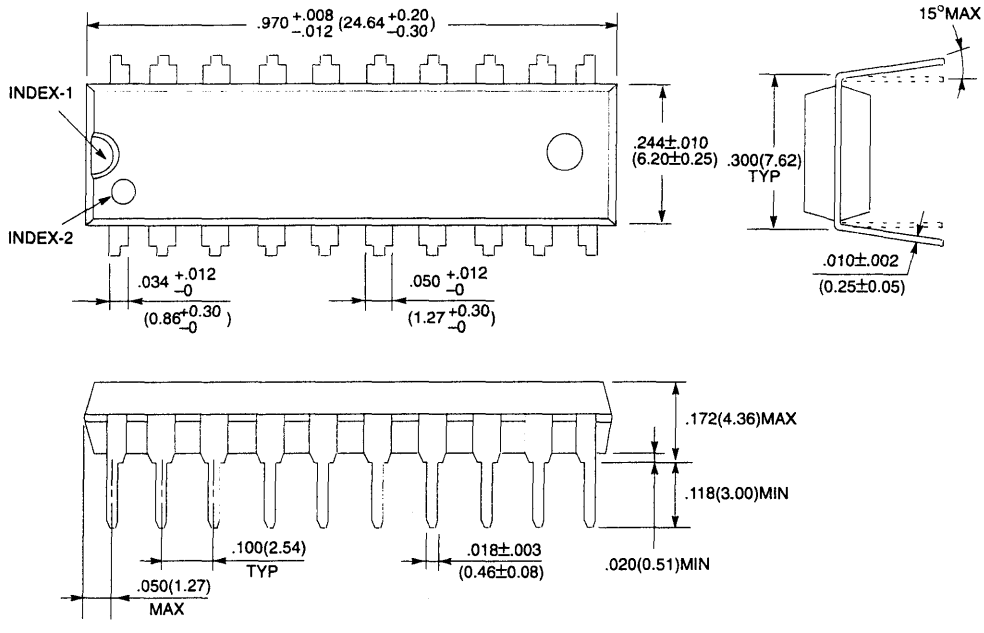
APPLICATION EXAMPLE



Note: V_{P1}, V_{P2} : 8V max
C1, C2 : depends on the crystal oscillator
Clock, Data, LE : involve the Schmitt circuit
When input pins are open, please insert the pull down/up resistor individually to prevent the oscillation.
X'tal : 12.8MHz

PACKAGE DIMENSIONS

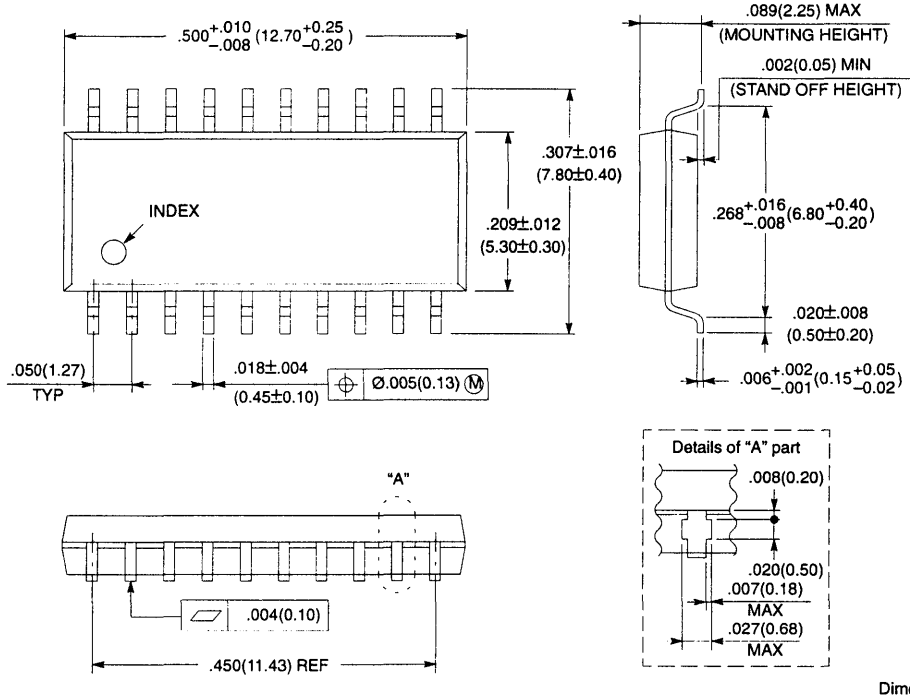
20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



Dimensions in
inches (millimeters)

June 1995
Edition 0.4

FUJITSU

MB15U10

1.1GHz DUAL PLL FREQUENCY SYNTHESIZER

4

INTRODUCTION

The Fujitsu MB15U10 is a dual serial input phase-locked loop (PLL) frequency synthesizer and is ideally suitable for mobile communications such as cellular phones. The MB15U10 has two PLL frequency synthesizer circuits on a single chip: one for transmission and the other for reception (PLL1 and PLL2).
It can operate from a +2.6V to 5.5V supply. Fujitsu's advanced technology achieves an Icc of 7 mA (typical) as well as 10 µA (max.) at power saving mode.

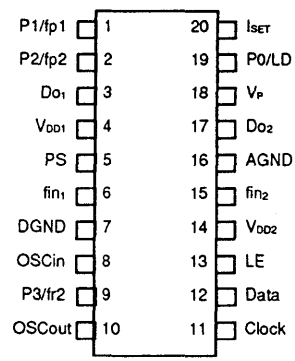
PRELIMINARY

FEATURES

- Two PLLs' for transmission/reception
- Low current consumption : I_{CC} = 7 mA typ. at 3 V
- Power saving funtion : I_{PS} = 10 µA max.
- Divide ratio setting with serial data input :
  Binary 12-bit reference counter : 6 to 4095
  Binary 17-bit main counter : 1024 to 131,071
  *Main counters can be programmed individually each other.
- On-chip constant current source charge pumps
- Adjustable charge pump output current with an external resistor
- Lock detection function
- Phase matching circuit helps fast intermittent operation
- Plastic 20–pin SSOP (shrink small outline) package

PIN ASSIGNMENT

(TOP VIEW)



(FPT–20P–M03)

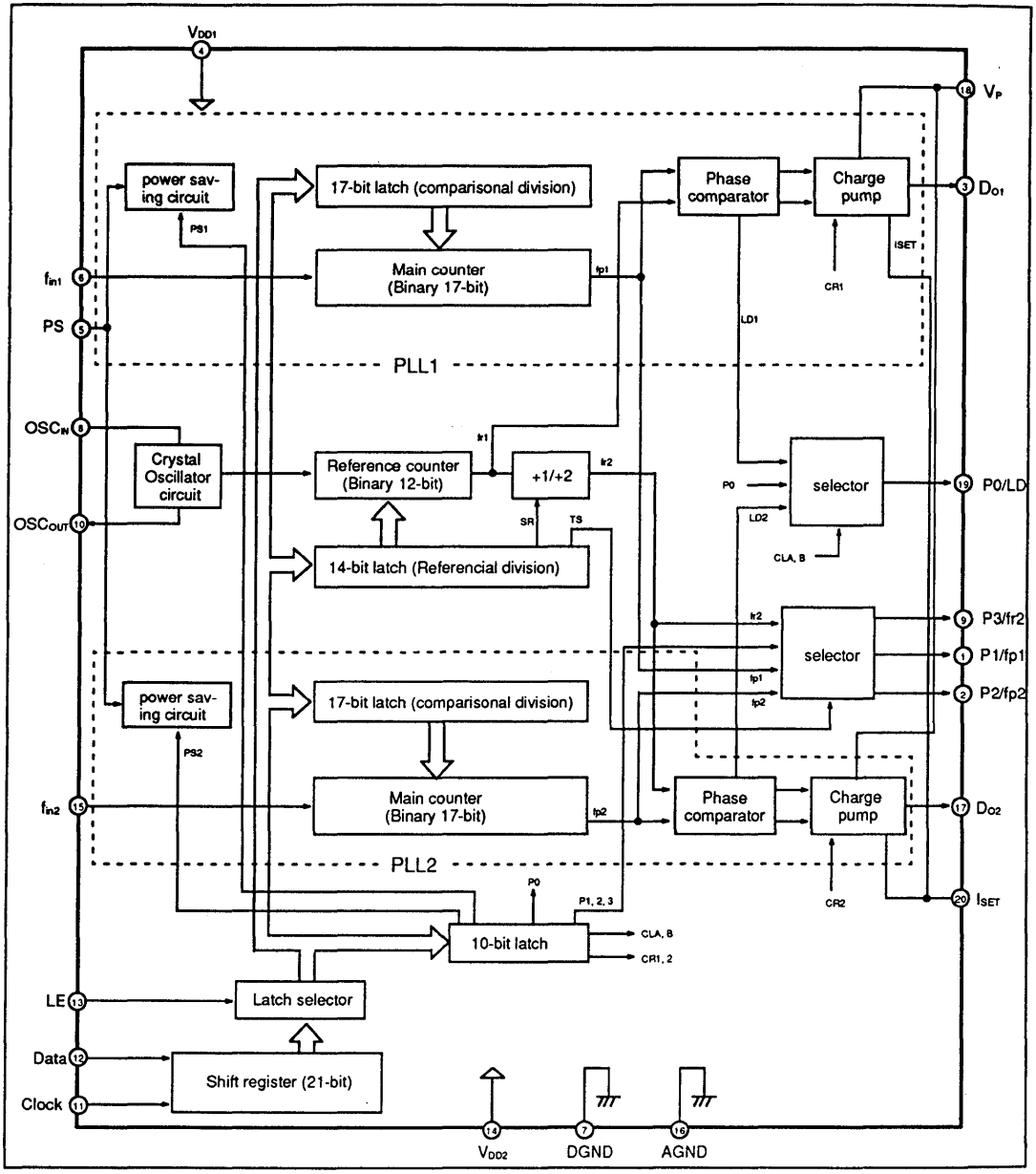
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameters	Symbol	Value	Unit	Remark
Supply voltage	$V_{DD1,2}$	−0.3 to +4.0	V	
	V_P	V_{DD} to 6.0	V	
Output voltage	V_O	−0.3 to V_{DD} +0.3	V	
Output current	I_O	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	Description
1	P1/fp1	Data output / fp1 monitoring output (Open drain output)
2	P2/fp2	Data output / fp2 monitoring output (Open drain output)
3	D_{O1}	Charge pump output (PLL1)
4	V_{DD1}	Power supply for digital blocks (PLL1)
5	PS	Power saving mode control (input "L" : power saving mode)
6	f_{in1}	RF input (PLL1)
7	DGND	Ground for digital blocks
8	OSCin	Crystal oscillator or TCXO input
9	P3/fr2	Data output / fr2 monitoring output (Open drain output)
10	OSCout	Crystal oscillator output
11	Clock	Clock input
12	Data	Data input
13	LE	Load enable of serial input data (input "H" : Data is shifted into a latch.)
14	V_{DD2}	Power supply for digital blocks (PLL2)
15	f_{in2}	RF input (PLL2)
16	AGND	Ground for the charge pumps
17	D_{O2}	Charge pump output (PLL2)
18	V_P	Power supply for charge pump
19	P0/LD	Data output / lock detector output (Open drain output) Output is selected by "OLA" and "OLB" bits in a serial data
20	I_{SET}	Charge pump output current adjustment (A resistor is connected.)

FUNCTION DESCRIPTIONS

Serial data input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider, programmable divider (PLL1) and programmable divider (PLL2) separately by means of address setting.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched.

a)Serial data input format

(MSB) ← Direction of data input → (LSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
X	X	X	P0	OLA	OLB	CR1	CR2	X	X	PS1	PS2	P3	P2	P1	X	X	0	0	0	1
MA16	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	0	1	0	0
0	0	0	TS	SR	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	1	0	1
MB16	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0	0	1	1	0
Auxiliary bit for test (no need at ordinary use)																	0	0	0	0

← Data setting → | ← Address →

MA0 to 16	: Divide ratio setting bits of the main counter (PLL1)	[See Table 1]
MB0 to 16	: Divide ratio setting bits of the main counter (PLL2)	[See Table 2]
R0 to 11	: Divide ratio setting bits of the reference counter	[See Table 3]
SR	: Divide ratio select bit of reference frequency (PLL1 and PLL2)	[See Table 4]
P0 to 3	: Setting bits of P0 to P3 output pins	[See Table 5]
OLA, B	: Select bits of P0/LD pin output	[See Table 6]
CR1, 2	: Select bits of charge pump output current	[See Table 7]
PS1, 2	: Power saving mode control bits	[See Table 8]
TS	: Test bits (Set "0" at ordinary use.)	[See Table 9]
X	: Dummy bits (Set "0" or "1".)	
0	: Set "0"	

b)Data setting description

- Table 1 : MA0 to MA16 : Divide ratio of the binary 17-bit main counter (PLL1)

Divide ratio R	MA 16	MA 15	MA 14	MA 13	MA 12	MA 11	MA 10	MA 9	MA 8	MA 7	MA 6	MA 5	MA 4	MA 3	MA 2	MA 1	MA 0
1024	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1025	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

Notes: Divide ratios less than 1024 are prohibited. (Divide ratio = 1024 to 131,071)

- Table 2 : MB0 to MB16 : Divide ratio of the binary 17-bit main counter (PLL2)

Divide ratio R	MB 16	MB 15	MB 14	MB 13	MB 12	MB 11	MB 10	MB 9	MB 8	MB 7	MB 6	MB 5	MB 4	MB 3	MB 2	MB 1	MB 0
1024	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1025	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

Notes: Divide ratios less than 1024 are prohibited. (Divide ratio = 1024 to 131,071)

- Table 3 : R1 to R11 : Divide ratio of the binary 12-bit reference counter

Divide ratio R	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1	R 0
6	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•

Notes: Divide ratios less than 6 are prohibited. (Divide ratio = 6 to 4095)

- Table 4 : Divide ratio select bit of reference frequency (PLL1 and PLL2)

SR	Divide ratio of reference frequency (PLL1)	Divide ratio of reference frequency (PLL2)
0	R	R
1	R	2R

Notes: R = Programmed value with R0 to R11 bits

4

- Table 5 : P0 to P3 ; P0 to P3 outputs control

PX bit	PX output (19, 1, 2, 9 pins)
0	ON ("L")
1	OFF ("Z")

Notes: X = 0 to 3

- Table 6 : OLA, OLB ; 19–pin output selection

OLA	OLB	19-pin output
0	0	P0 signal
0	1	Lock detect signal (PLL2)
1	0	Lock detect signal (PLL1)
1	1	Lock detect signal (PLL1 and PLL2)

- Table 7 : CR1, CR2 ; Charge pump output current selection

CR1, 2	Charge pump output current
0	Ioo
1	2Ioo

Notes: PLL1 and PL2 can be controlled individually.

- Table 8 : PS ; Power saving control

PS1, 2	Charge pump output current
0	Power saving mode
1	Operation

Notes: PLL1 and PL2 can be controlled individually.

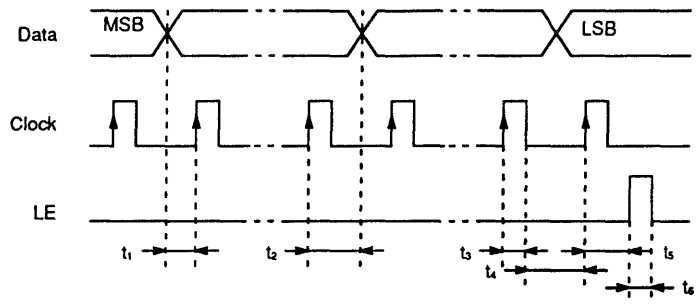
- Table 9 : TS ; Test bit (Set to "0" at ordinary use.)

TS	1-pin	2-pin	9-pin
0	Output P1 signal	Outputs P2 signal	outputs P3 signal
1	outputs fp1	outputs fp2	outputs fr2

Notes: Reference frequency and comparison frequency can be monitored via P1 to P3 pins.

Serial data input timing

- t_1 (≥ 20ns), t_2 (≥ 20ns), t_3 (≥ 50ns), t_4 (≥ 50ns), t_5 (≥ 20ns), t_6 (≥ 1000ns)



Note: One bit of data is shifted into the shift register on the rising edge of the clock.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply Voltage	V_{DD1}, V_{DD2}	2.6	–	5.5	V	
	V_P	V_{DD}	–	6.0	V	
Input voltage	V_I	GND	–	V_{DD}	V	
Operating temperature	T_A	–30	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

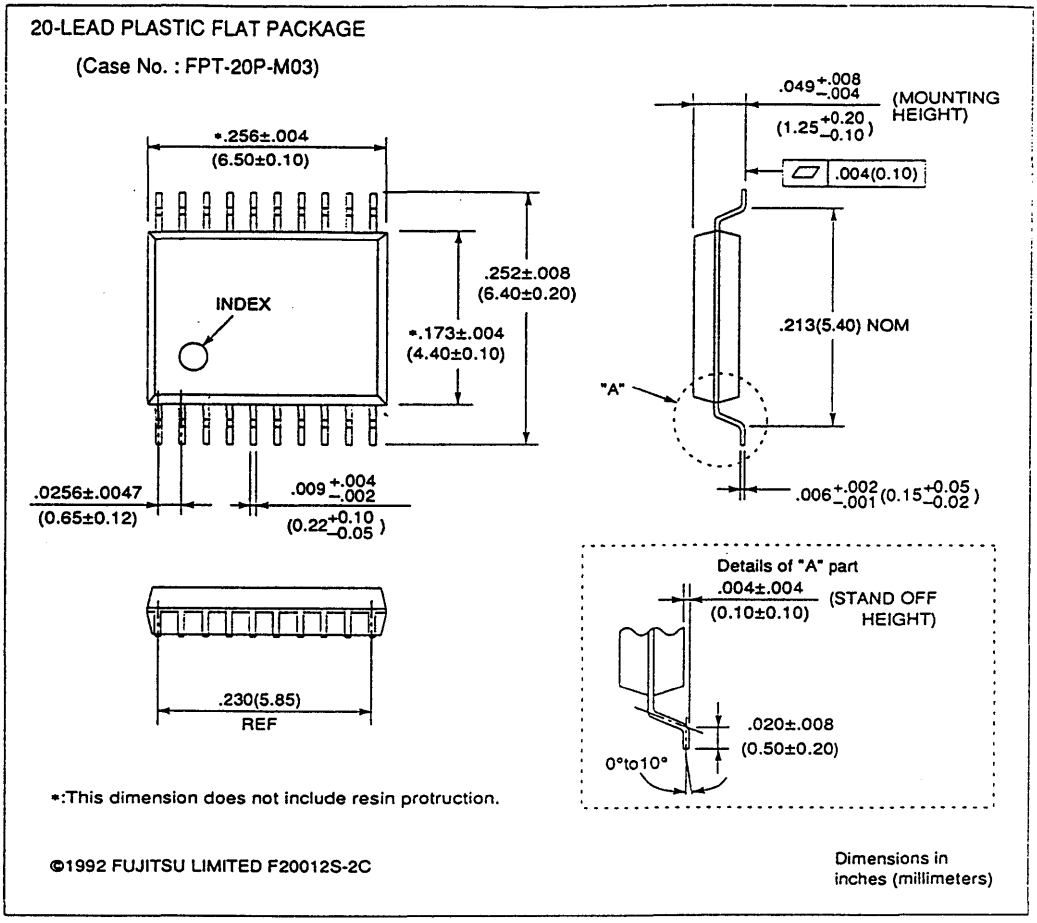
ELECTRICAL CHARACTERISTICS

Ta = 25°C

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current ($I_{DD1} + I_{DD2}$)		I_{DD}	–	7.0	9.0	mA	*1
			–	11.0	–	mA	*2
Stand by current	$V_{DD1, 2}$	I_{PS}	–	–	10	µA	
Operating frequency	$f_{IN1, 2}$	f_{IN}	90	–	1100	MHz	
	OSC_{IN}	f_{OSC}	3	12.8	35	MHz	
Input sensitivity	$f_{IN1, 2}$	$P_{f\,IN}$	–13	–	+1	dBm	50Ω, Vcc=2.6 to 3.5V
	$f_{IN1, 2}$	$P_{f\,IN}$	–7	–	+1	dBm	50Ω, Vcc=3.5 to 5.5V
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Data, Clock, LE, PS	V_{IH}	V_{DD} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{DD} x 0.3	V	
High-level input current	Data, Clock, LE, PS	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{IN}	I_{OSC}	–100	–	100	µA	
Low-level output voltage	P0 to P3	V_{OL}	–	–	0.4	V	Open drain output
Set output voltage	I_{SET}	V_{SET}	–	1.2	–	V	R_{SET} = 5kΩ to 60kΩ
High-impedance Cut off current	D_O,, P0 to P3	I_{OFF}	–	–	1.1	µA	
Output current	$D_{O1, 2}$	I_{DOH1}	1.4	1.9	2.4	mA	R_{SET} = 7kΩ connected. CR1, 2 bits = "1" V_{DD} = 3.0V, V_P = 5.0V
		I_{DOL1}	1.4	1.9	2.4	mA	
	$D_{O1, 2}$	I_{DOH0}	0.7	0.96	1.2	mA	R_{SET} = 7kΩ connected. CR1, 2 bits = "0" V_{DD} = 3.0V, V_P = 5.0V
		I_{DOL0}	0.7	0.96	1.2	mA	
	P0 to P3	I_{OL}	1.0	–	–	mA	Open drain

Note: *1 ; f_{IN} = 1.1 GHz, OSC_{IN} = 12.8 MHz, V_{DD} = 3.0 V. In locked state.
*2 ; f_{IN} = 1.1 GHz, OSC_{IN} = 12.8 MHz, V_{DD} = 5.0 V. In locked state.

PACKAGE AND DIMENSIONS



Sept. 1995
Edition 1.1a

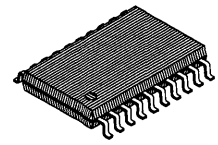
FUJITSU

DATA SHEET

MB1510

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER



Plastic Package
FPT–20P–M01

4

DESCRIPTION

The Fujitsu MB1510 is a 1.1 GHz dual serial input PLL (Phase Locked Loop) frequency synthesizer designed for cellular telephone and cordless telephone applications.

The MB1510 has two PLL circuits on a single chip: PLL1 and PLL2. An analog switch is provided for each PLL circuit decrease lock up time. Separate power supply pins are provided for each PLL circuit as well.

1.1 GHz dual modulus prescalers are on chip and enables a pulse swallow function.

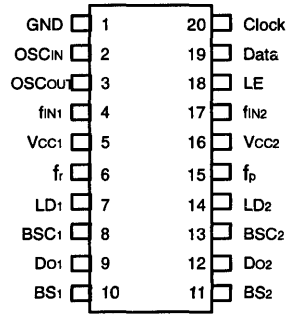
It operates from a supply voltage of 3.0V typ. and dissipates 15 mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

FEATURES

- High operating frequency: f_{in} = 1.1 GHz (P_{in} = –10 dBm, V_{CC} = 3V)
- Pulse swallow function: 64/65 or 128/129
- Low power supply current: I_{CC} = 15 mA typ, @3V.
- Serial input reference divider: R = 512 or 1024
- Serial input 18-bit programmable divider consisting of:
  — Binary 7-bit swallow counter: 0 to 127
  — Binary 11-bit programmable counter: 16 to 2047
  — Tx and Rx programmable counters may be controlled separately.
- Low power supply voltage: V_{CC} = 2.7 to 5.5V
- On-chip analog switches achieve fast lockup time
- Fast lock up by bipolar charge pumps
- Wide operating temperature: T_A = –40 to 85°C
- Plastic 20-pin flat package (Suffix: –PF)

Pin Assignment

(TOP VIEW)



Pin Assignment might be changed to improve the characteristics without notice.

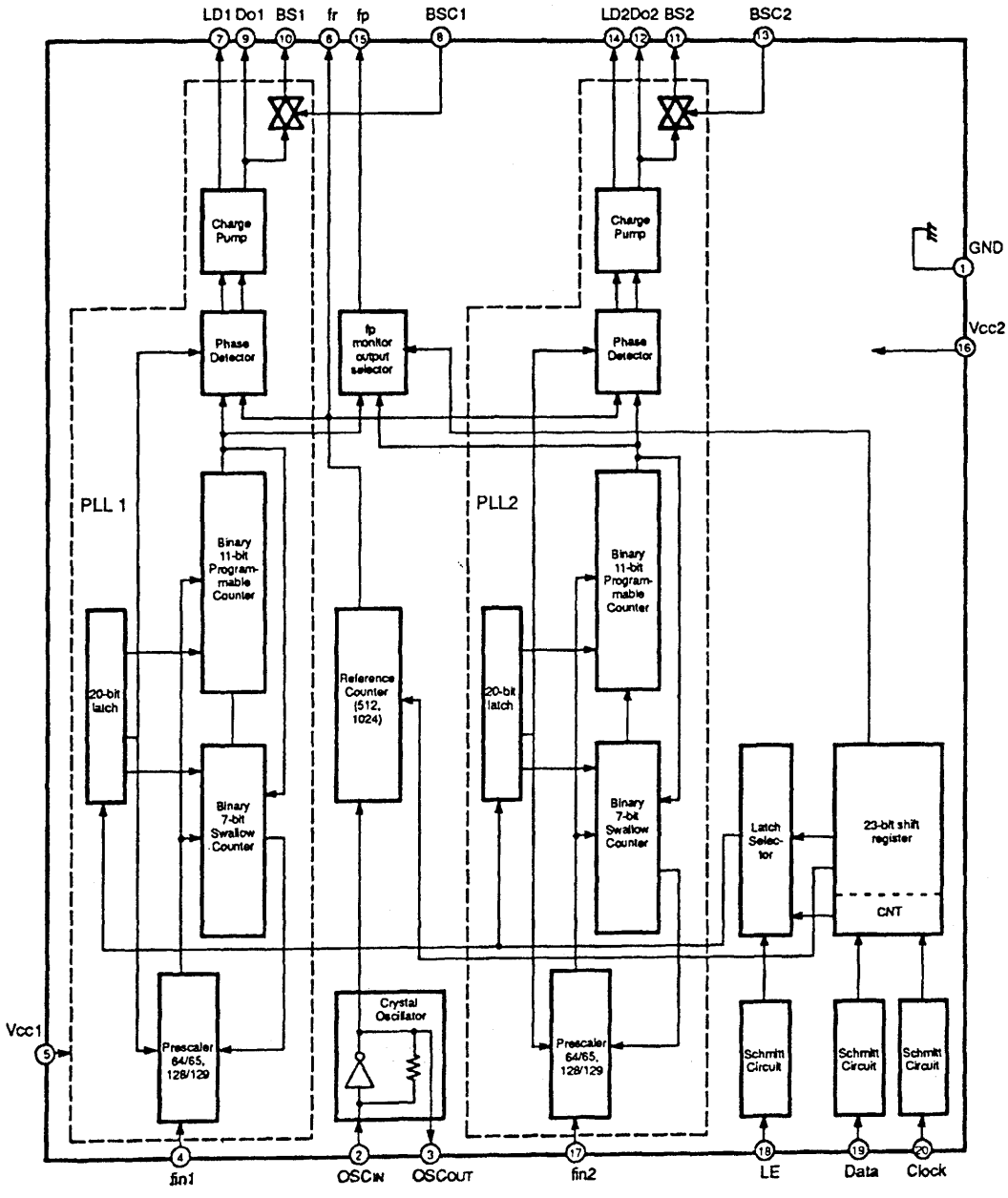
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC}+0.5	V
Output Current	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1510 Block Diagram



PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>—</td><td>Ground</td></tr>
<tr><td>2
3</td><td>OSC_{IN}
OSC_{OUT}</td><td>I
O</td><td>Oscillator input pin
Oscillator output pin
A crystal is connected between OSC_{IN} pin and OS_{OUT} pin.</td></tr>
<tr><td>4</td><td>f_{in1}</td><td>I</td><td>Prescaler input pin of PLL1 section.
The connection with VCO should be AC connection.</td></tr>
<tr><td>5</td><td>V_{CC1}</td><td>—</td><td>Power supply voltage input pin of PLL1 section.
When power is OFF, latched data of PLL1 section is cancelled.</td></tr>
<tr><td>6</td><td>f_r</td><td>O</td><td>Monitor pin for programmable reference divider output</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of PLL1 section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>BSC1</td><td>I</td><td>Analog switch control pin of PLL1 section.
<table>
<tr><th>BSC1</th><th>BS1 pin output</th></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>9</td><td>Do1</td><td>O</td><td>Charge pump output pin of PLL1 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of PLL1 section, and controlled by BSC1.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of PLL2 section, and controlled by BSC2.</td></tr>
<tr><td>12</td><td>Do2</td><td>O</td><td>Charge pump output pin of PLL2 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>BSC2</td><td>I</td><td>Analog switch control pin of PLL2 section.
<table>
<tr><th>BSC2</th><th>BS2 pin output</th></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detect signal output pin of PLL2 section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>f_p</td><td>O</td><td>Monitor pin for programmable divider output.
This pin output divided frequency of PLL1 section or PLL2 section depending upon FP bit setting.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	V_{CC2}	—	Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of PLL2 section and reference counter is cancelled.
17	f_{in2}	I	Prescaler input pin of PLL2 section. The connection with VCO should be AC connection.
18	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data. At this moment, charge pump output signal is output from BS pin since internal analog switch becomes ON.
19	Data	I	Serial data input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either PLL1 section or PLL2 section depending upon a control data. Control bit data: H → The destination of data: Latch of PLL1 section Control bit data: L → The destination of data: Latch of PLL2 section
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of data into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$$f_{vco} = \{(M \times N) + A\} \times f_{osc} \div R \quad (A < N)$$

f_{vco}: Output frequency of external voltage controlled oscillator (VCO)
M: Preset divide ratio of dual modulus prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{osc}: Reference oscillation frequency
R: Preset divide ratio of reference counter (512 or 1024)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins, Data pin, Clock pin, and LE pin. Programmable divider of PLL1 section and programmable divider of PLL2 section are controlled individually.

Serial data of binary data is input into Data pin.

On rising edge of clock shifts one bit of serial data into the shift register. When load enable signal is high. the data stored in the shift register is transferred to either the latch of PLL1 section or the latch of PLL2 section depending upon the control bit data setting.

Control data	Destination of serial data
H	Latch of PLL1 section
L	Latch of PLL2 section

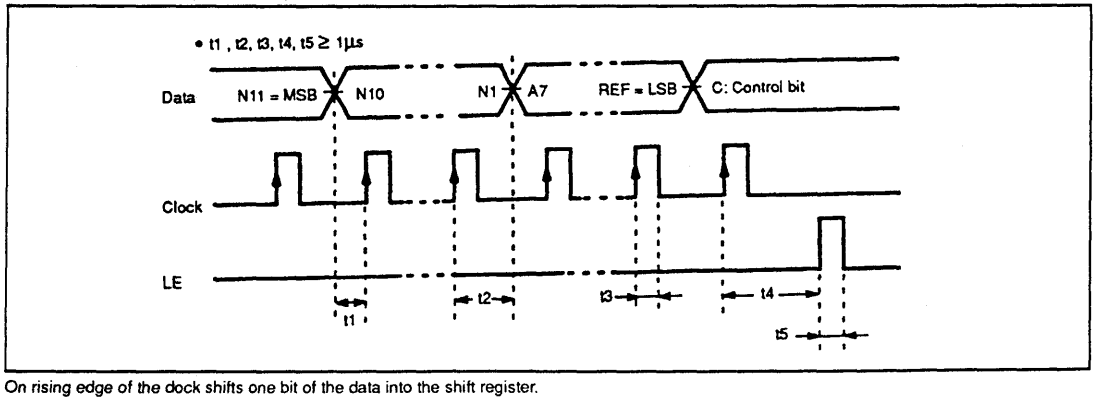
SHIFT REGISTER CONFIGURATION

Control bit ↓ LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CNT	REF	FP	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
PRE : Divide ratio of the prescaler setting bit (64/65,128/129)
FP : Output of the programmable divider control bit (fp1 or fp2)
REF : Divide ratio of the reference counter setting bit (512 to 1024)
CHT : Control bit

SERIAL DATA INPUT TIMING



On rising edge of the dock shifts one bit of the data into the shift register.

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1l	1	1	1	1	1

Note: Divide ratio loss than 16 is prohibited.
Divide ratio (H) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

PRE : DIVIDE RATIO (P) OF THE PRESCALER SETTING BIT
H =64/65
L=128/129

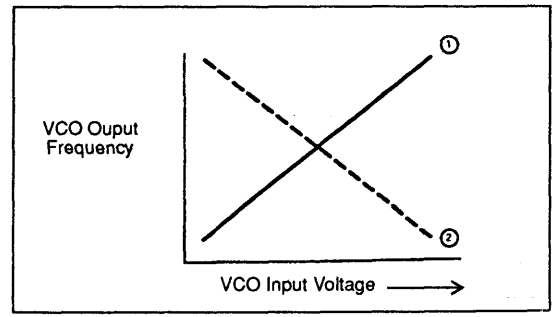
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H=S12 (fr=25.0 kHz)
L= 1024 (fr= 12.5 kHz)

FP: OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable~ divider output frequency (fp1) of PLL1 section.
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of PLL2 section.

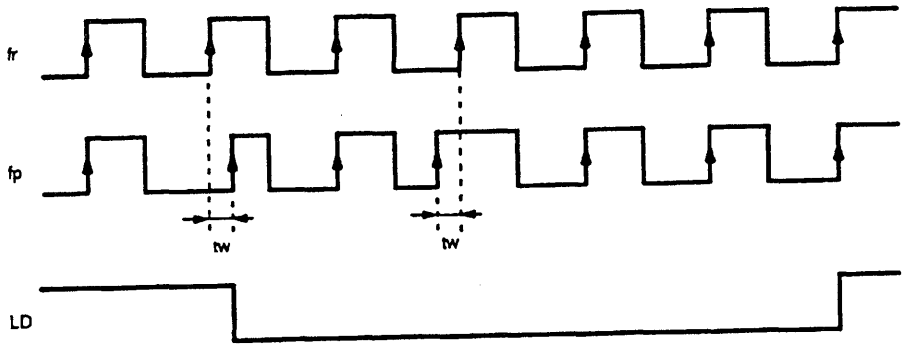
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin.

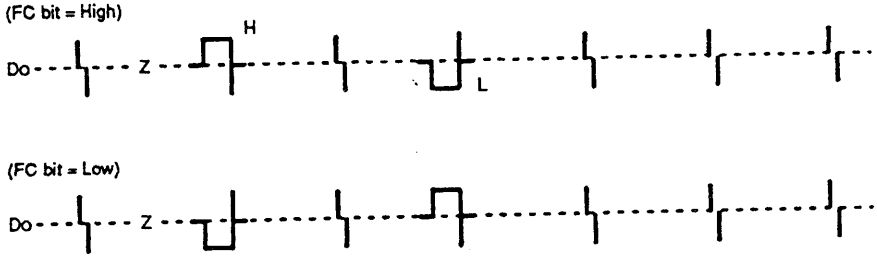
	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: Z = High-impedance
Depending upon the VCO polarity, FC should be bit set.



PHASE DETECTOR OUTPUT WAVEFORM





Note:

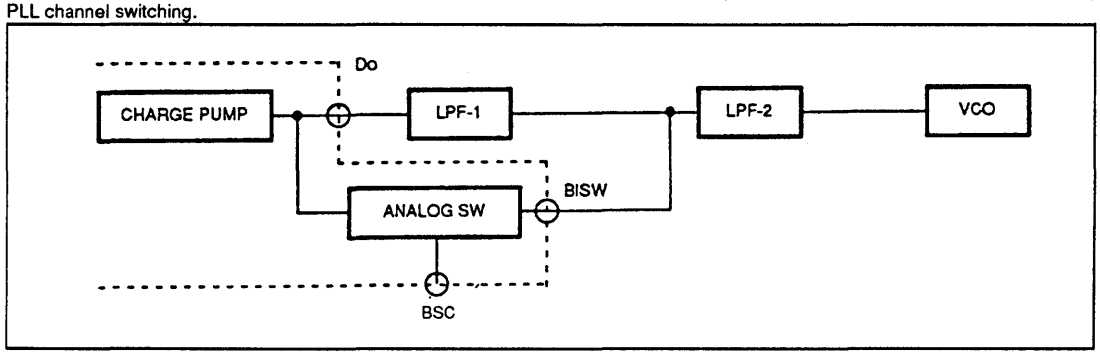
- Phase difference detection range = -2π to $+2\pi$
- LD output becomes low when phase difference is tW or more.
  LD output becomes high when phase difference less than tW is repeated 3 times or more.
  (e. g. tW = 625 to 1250ns, foscin = 12.8 MHz)
- Spike appearance depends on the charge pump characteristics. The spike is output to diminish the dead band.
- When fr > fp or fr < fp, spike might not generate depending on the charge pump characteristics.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by BSC input signal. BSC1 controls the analog switch of the PLL1 circuit, BSC2 controls the analog switch of PLL2. When the analog switch is ON, BS pin output the charge pump output (D01, D02). When analog switch is OFF, BS pin is set to high-impedance.

	BCS1 (2)	
	H	L
Analog switch of PLLI1 (2) section	ON	OFF
BS1 (2) output	Charge pump output Do1 (2)	High-impedance

When an analog switch is inserted between LPF-1 and LPF-2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
Input Voltage	V_{IN}	GHD	—	V_{CC}	V	
Operating Temperature	T_A	-40	—	+85	°C	

HANDLING PRECAUTIONS

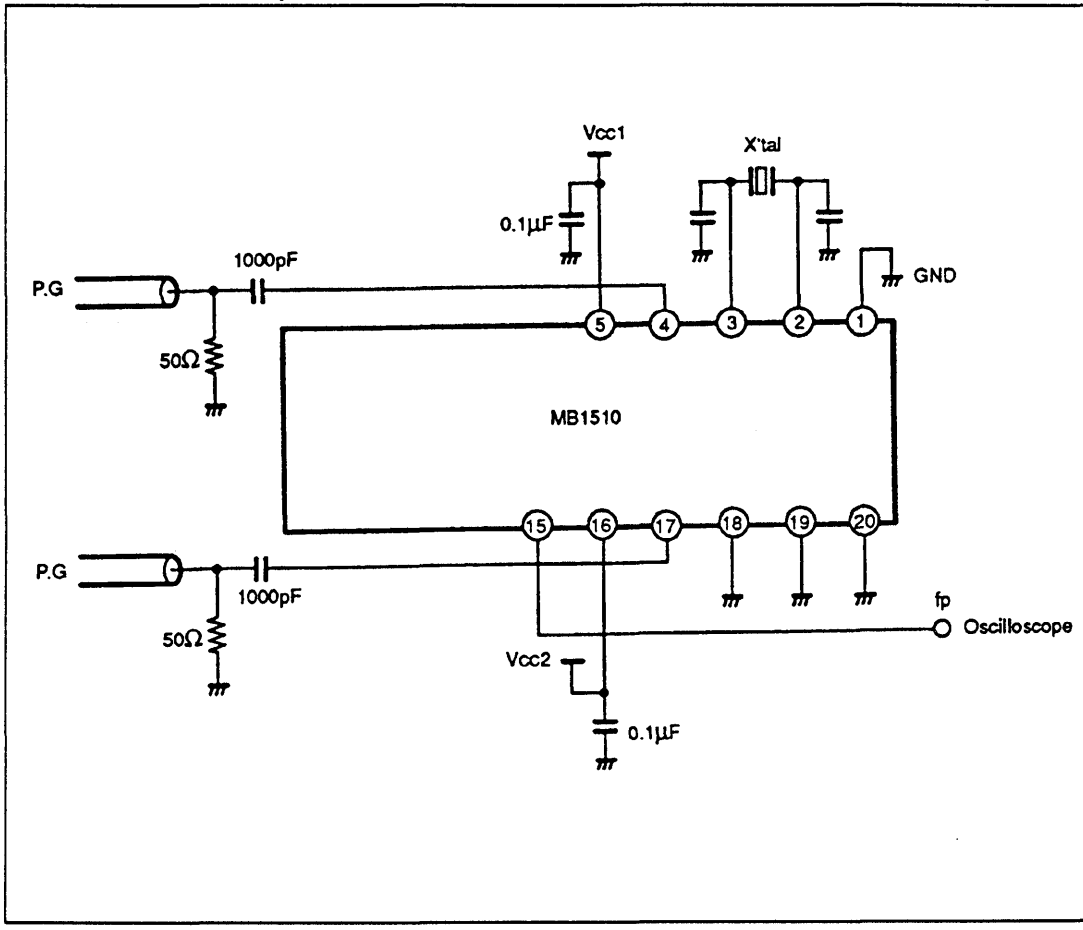
- This device should be transported and stored in anti-static containers.
- This is a static sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded.
- Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket
- Protects leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

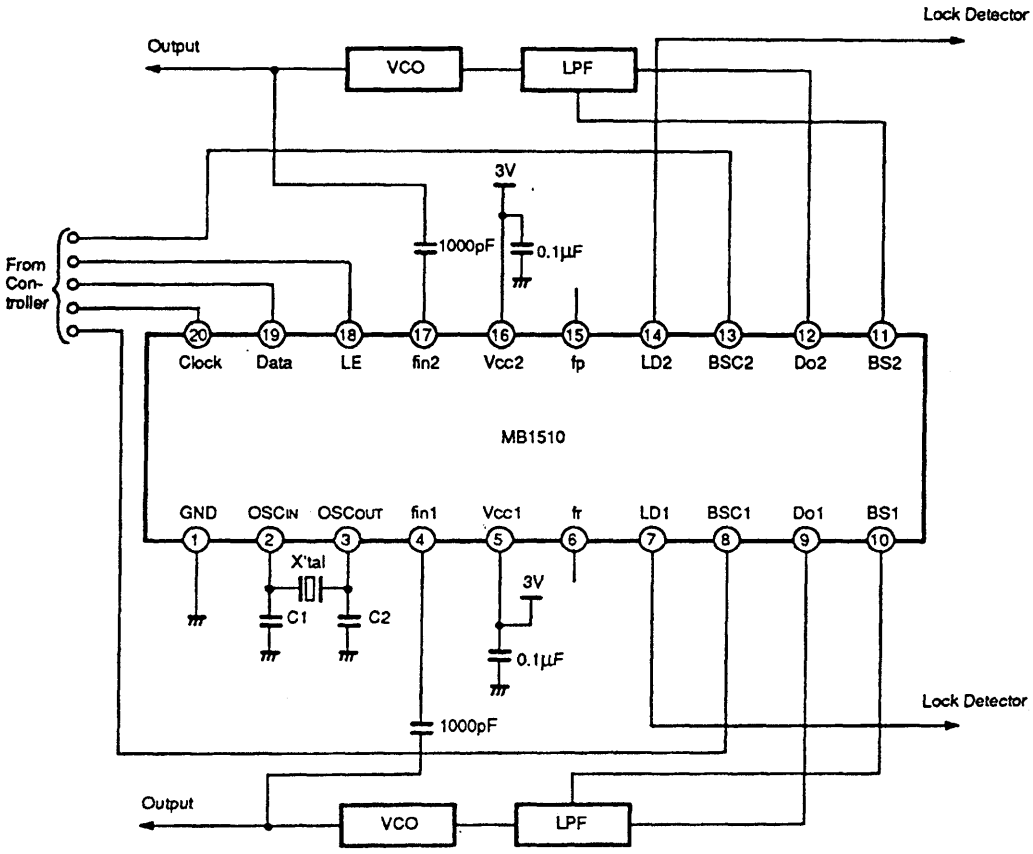
Parameter		Symbol	Condition	Value			Unit
Power Supply Current		I_{CC1}	PLL2 current	—	8.0	—	mA
		I_{CC2}	(PLL1 + PLL2) current	—	15.0	—	
Operating Frequency	f_{in}	f_{in1}	*1	10	—	1100	MHz
		f_{in2}	*2	10			
	OSC_{IN}	f_{osc}		—	12.8	20.0	
Input Sensitivity	f_{in}	P_{fin}	V_{CC} = 2.7 to 4.0V, 50Ω	–10	—	0	dBm
			V_{CC} = 4.0 to 5.5V, 50Ω	–4	—	2	
	OSC_{IN}	V_{OSC}		0.5	—	—	Vp-p
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		V_{CC}x 0.7+0.4	—	—	V
Low-level Input Voltage		V_{IL}		—	—	V^{CC}x0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		—	1.0	—	μA
Low-level Input Current		I_{IL}		—	–1.0	—	
	FC	I_{FC}		—	–60	—	
Input Current	OSC_{IN}	I_{OSC}			± 50	—	
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 3.0 V	2.2	—	—	V
Low-level Output Voltage		V_{OL}		—	—	0.4	
High-Impedance Cutoff Current	D_0, φP	I_{OFF}	V_P = V_{CC} to 8.0 V V_{OOP} = GND to 8.0 V	—	—	1.1	μA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	—	—	mA
		I_{OL}		1.0	—	—	
Analog Switch ON Resistance		R_{ON}		—	50	—	Ω

Notes: *1: Divide ratio of the prescaler is 128/129.
*2: Divide ratio of the prescaler is 64/65.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



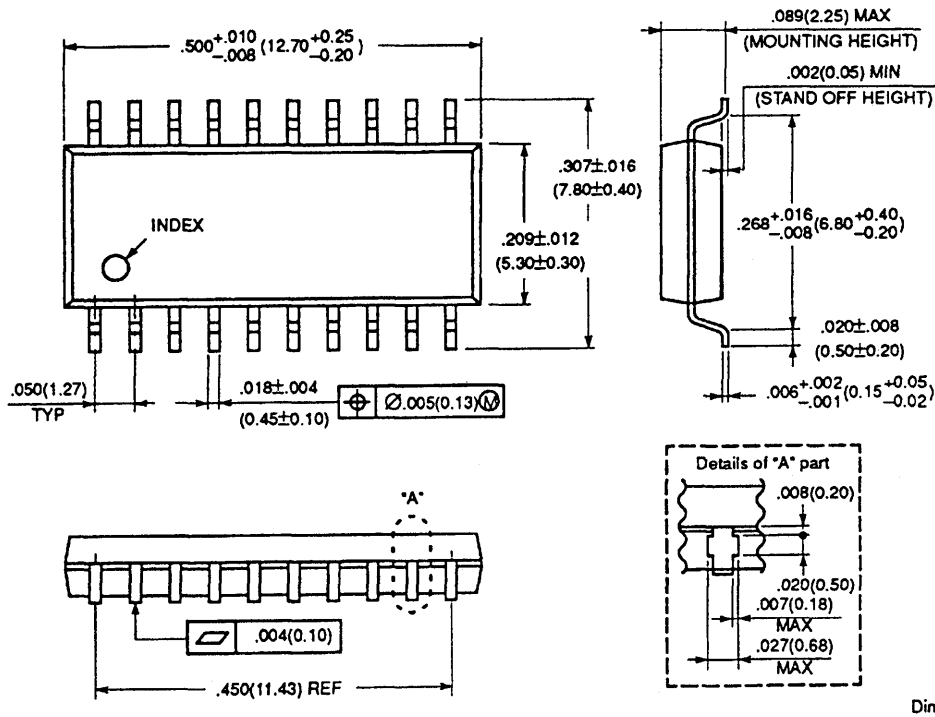
APPLICATION EXAMPLE



Note: X'tal: 12.8MHz
C1, C2: depends on the crystal oscillator.
Clock, Data, LE: involve the schmitt circuit
When input pins are open, please insert the pull down/up resistor individually to prevent the oscillation.

PACKAGE DIMENSIONS

20-Lead Plastic Flat Package
(Case No.: FPT-20P-M01)



Dimensions in inches (millimeters)

January 1995
Edition 0.1

FUJITSU

Product Profile Sheet

MB15B11

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

On-chip 1.1GHz & 400MHz PRESCALER'S

The Fujitsu MB15B11 is a serial input Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. Two synthesizers; 400MHz system has a low sensitivity charge pump for transmit modulation, 1.1GHz system has a high sensitivity charge pump for fast lock up of receive frequency. An analog switch is provided for each PLL circuit for faster lock up.
These various features help compact system designing important in mobile radio applications. Typical applications are cellular phones, cordless phones and other radio applications where IF modulation is adopted.
It operates with a supply voltage of 3.0V typ. and dissipates totally 9.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology. The power saving function maintains current reduction.

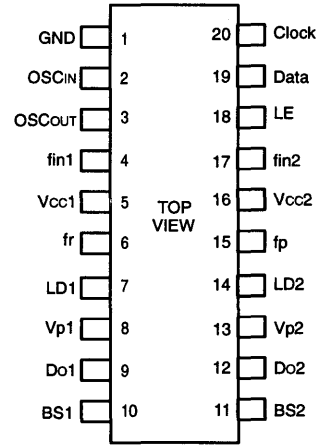
PRELIMINARY

4

FEATURES

- Dual PLL frequency synthesizers; 400MHz (PLL1) & 1.1 GHz (PLL2)
- Low power supply current: I_{CC} (total) = 9.5 mA typ. (Vcc = 3V)
- Power saving function : $I_{CC1} = I_{CC2}$ = 100 µA typ (Vcc = 3V)
- Pulse swallow function;
  – 1.1GHz Prescaler: 64/65 or 128/129
  – 400MHz Prescaler: 32/33 or 64/65
- Serial input 14-bit programmable reference counter: R = 8 to 16383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 16 to 2047
  PLL1 and PLL2 programmable counters can be controlled independently.
- Functionally tuned up charge pumps
  – Transmit (PLL1): Low sensitivity charge pump (for modulation)
  – Receive (PLL2): High sensitivity charge pump (for fast lock up)
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- On-chip analog switches achieve fast lock up time
- Wide operating temperature: T_A = –30 to 80°C
- Plastic 20-pin SSOP package

PIN ASSIGNMENT

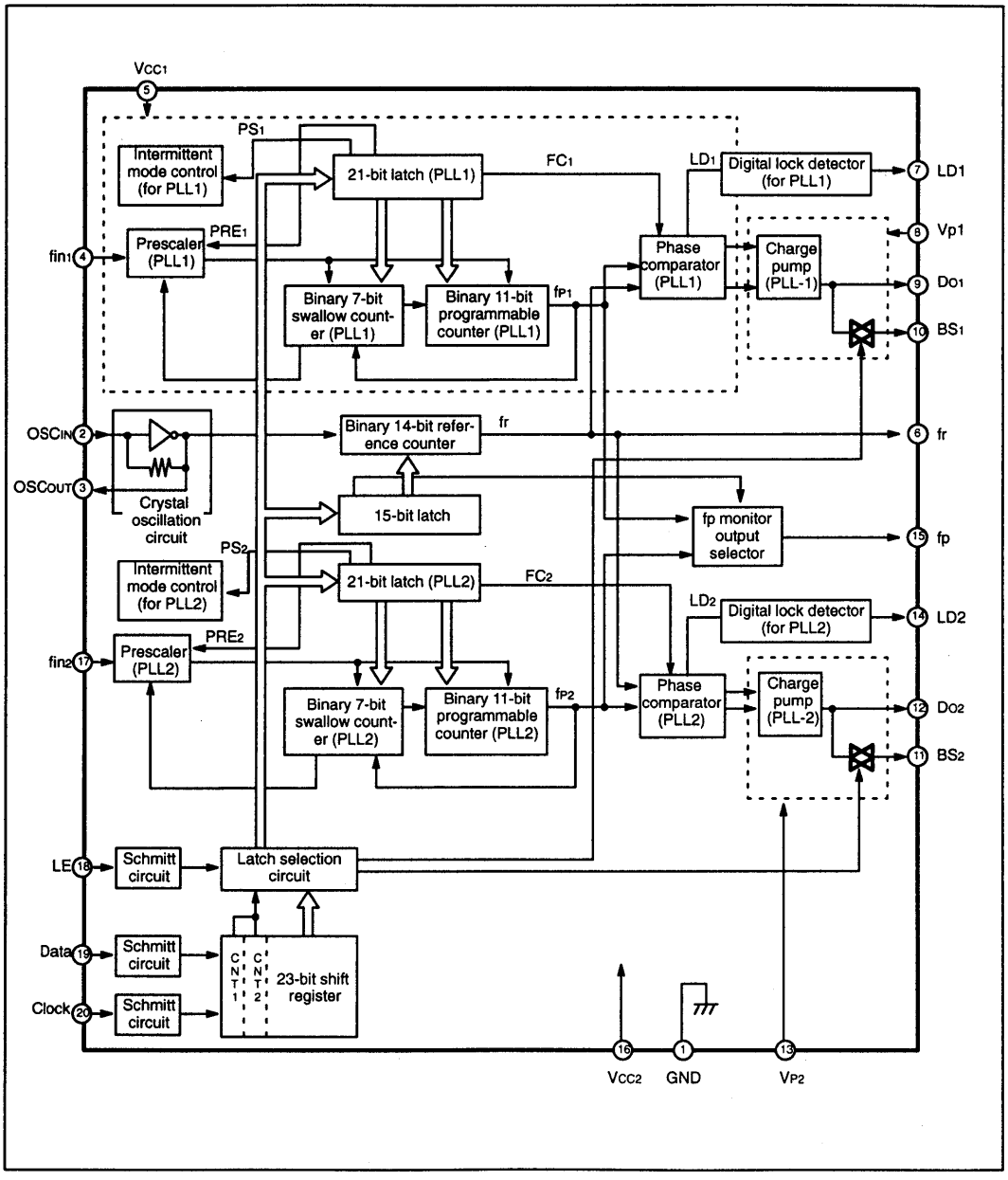


ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Remark	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to 5.0	V
	V_P		V_{CC} to 7.0	V
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



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<tr><td>2
3</td><td>OSCIN
OSCOUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSCIN pin and OSCOUT pin.</td></tr>
<tr><td>4</td><td>fin1</td><td>I</td><td>Prescaler input pin of PLL1 section.
The connection with VCO should be AC.</td></tr>
<tr><td>5</td><td>Vcc1</td><td>–</td><td>Power supply voltage input pin of PLL1 section.
When power is OFF, latched data of PLL1 section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output. (Open drain output)</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of PLL1 section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>Vp1</td><td>–</td><td>Power supply pin for PLL1's charge pump and analog switch</td></tr>
<tr><td>9</td><td>Do1</td><td>O</td><td>Charge pump output pin of PLL1 section.
Phase characteristics of the phase detector can be reversed according to FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of PLL1 section.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of PLL2 section.</td></tr>
<tr><td>12</td><td>Do2</td><td>O</td><td>Charge pump output pin of PLL2 section.
Phase characteristics of the phase detector can be reversed according to FC-bit setting.</td></tr>
<tr><td>13</td><td>Vp2</td><td>–</td><td>Power supply pin for PLL2's charge pump and analog switch</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detection signal output pin of PLL2 section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output. (Open drain output)
This pin outputs divided frequency of PLL1 section or PLL2 section according to FP bit setting.
<table>
<tr><th>FP bit</th><th>Output</th></tr>
<tr><td>H</td><td>PLL1 section (fp1)</td></tr>
<tr><td>L</td><td>PLL2 section (fp2)</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>16</td><td>Vcc2</td><td>–</td><td>Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and crystal oscillator.
When power is OFF, latched data of PLL2 section and reference counter is cancelled.</td></tr>
<tr><td>17</td><td>fin2</td><td>I</td><td>Prescaler input pin of PLL2 section.
The connection with VCO should be AC.</td></tr>
<tr><td>18</td><td>LE</td><td>I</td><td>Load enable input pin. This pin is followed by a schmitt trigger circuit.
When this pin is high, the data stored in the shift register is transferred into the latch according to a control data.</td></tr>
<tr><td>19</td><td>Data</td><td>I</td><td>Serial data input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit.
The stored data in the shift register is transferred to one of PLL1 section, PLL2 section and programmable counter depending upon control data settings.
<table>
<tr><th>Control bit data</th><th>The destination of data</th></tr>
<tr><td>H</td><td>Latch of PLL1 section</td></tr>
<tr><td>L</td><td>Latch of PLL2 section</td></tr>
</table></td></tr>
<tr><td>20</td><td>Clock</td><td>I</td><td>Clock input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit.
On rising edge of the clock, one bit of data is transferred into the shift register.</td></tr>
</table>

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$fvco = \{(P \times N) + A\} \times fosc \div R \quad (A < N)$

fvco: Output frequency of external voltage controlled ocillator (VCO)

P: Preset divide ratio of dual modulus prescaler (32 or 64 for PLL1, 64 or 128 for PLL2)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

fosc: Reference oscillation frequency

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable divider of PLL1 section, programmable divider of PLL2 section and programmable reference divider are controlled individually.
Serial data of binary data is entered into Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Control bits		Destination of serial data
CNT1	CNT2	
L	L	Programmable reference counter
L	H	Programmable counter of PLL1
H	H	Programmable counter of PLL2

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CN1	CN2	FP	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

R1 to R14 : Divide ratio setting bit for the reference programmable counter (8 to 16383)
FP : Test purpose bit (monitor output fp1/fp2 selection)
CN1, 2 : Control bit

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	PS	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio setting bit for the programmable counter (16 to 2047)
A1 to A7 : Divide ratio setting bit for the swallow counter (0 to 127)
FC : Phase control bit for the phase detector
PRE : Divide ratio setting bit for the prescaler (64/65, 128/129)
PS : Power saving control bit
CN1, 2 : Control bit

BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 8 is prohibited.
• Divide ratio (R) range = 8 to 16383

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
V	V	V	V	V	V	V	V	V	V	V	V
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 16 is prohibited.
• Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
V	V	V	V	V	V	V	V
127	1	1	1	1	1	1	1

Note:• Divide ratio (A) range = 0 to 127

PRESCALER DATA SETTING

		PRE = "H"	PRE = "L"
Prescaler Divide ratio	PLL1	32/33	64/65
	PLL2	64/65	128/129

Note: • Divide ratio for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.

POWER SAVING FUNCTION CONTROL

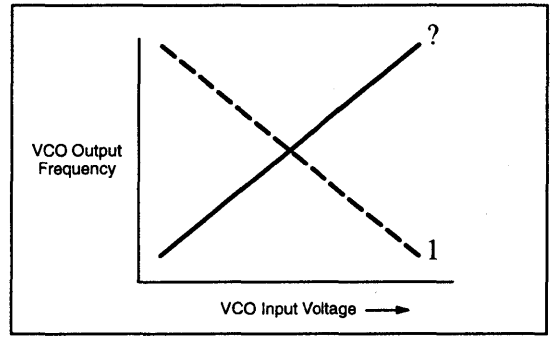
	PS	
	H	L
PLL1's section	ON	OFF
PLL2's section and common section	ON	OFF

Note: • Power saving mode for each PLL1 and PLL2 is selected by the serial data at that time of divide ratio setting for each programmable divider.
• Common section ; Crystal oscillator circuit, programmable reference counter

PHASE COMPARATOR PHASE CONTROL DATA SETTING

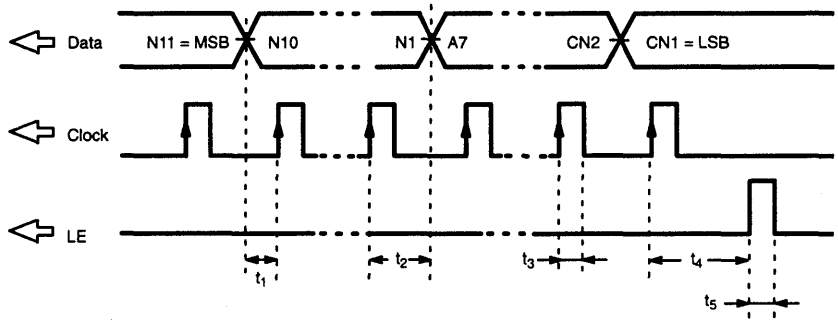
	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	?	1

Note: • Z = High-impedance
• Depending upon the VCO polarity, FC bit should be set.
• Phase characteristic for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.



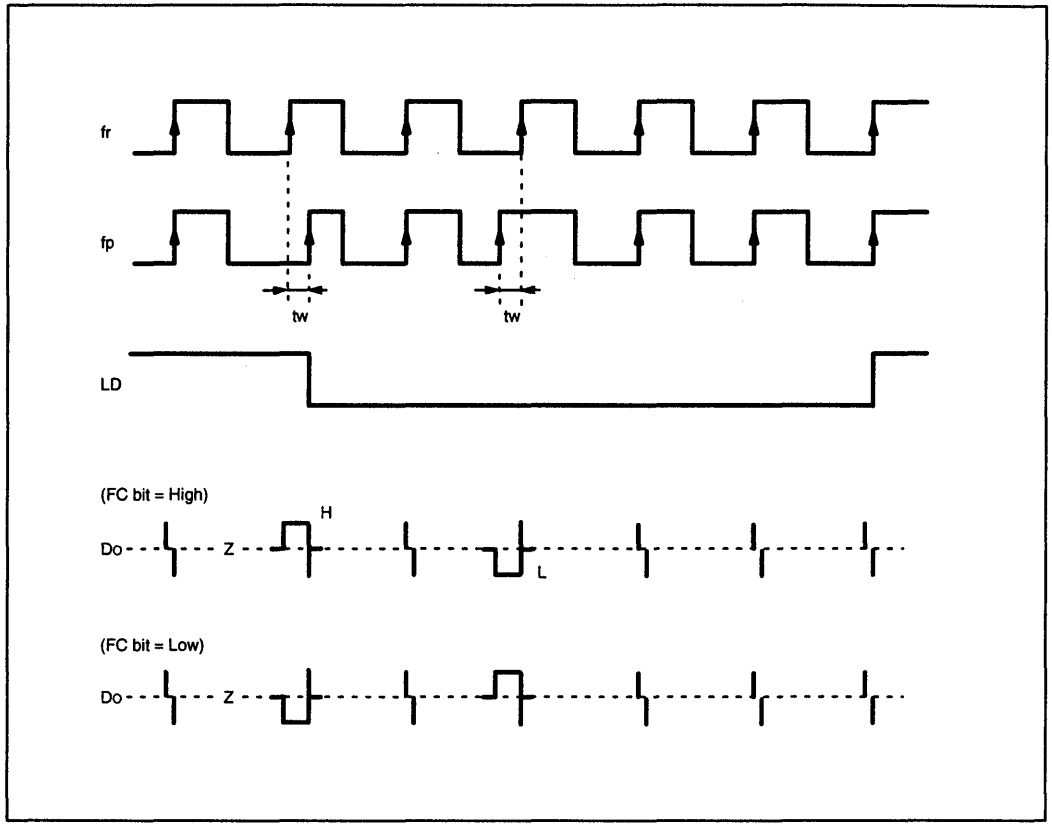
SERIAL DATA INPUT TIMING

t1 (>100ns) : Data set up time t2 (>1000ns) : Data hold time t3 (>300ns) : Clock pulse width
t4 (>100ns) : LE set up time to the rising edge of the last clock t5 (>800ns) : LE pulse width



On rising edge of the clock, one bit of the data is transferred into the shift register.

PHASE DETECTOR OUTPUT WAVEFORM



Note:
- Phase difference detection range = -2π to $+2\pi$
- LD output becomes low when phase difference is tw or more.
- LD output becomes high when phase difference is tw or less and continues to be so for three cysles or more.
- tw depends on OSCin input frequency.
  (e.g. tW635ns to 1250ns when foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	$V_{CC1} = V_{CC2}$
	V_{CC}	V_{CC}	–	6.0	V	
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	T_A	−30	–	+80	°C	

HANDLING PRECAUTIONS

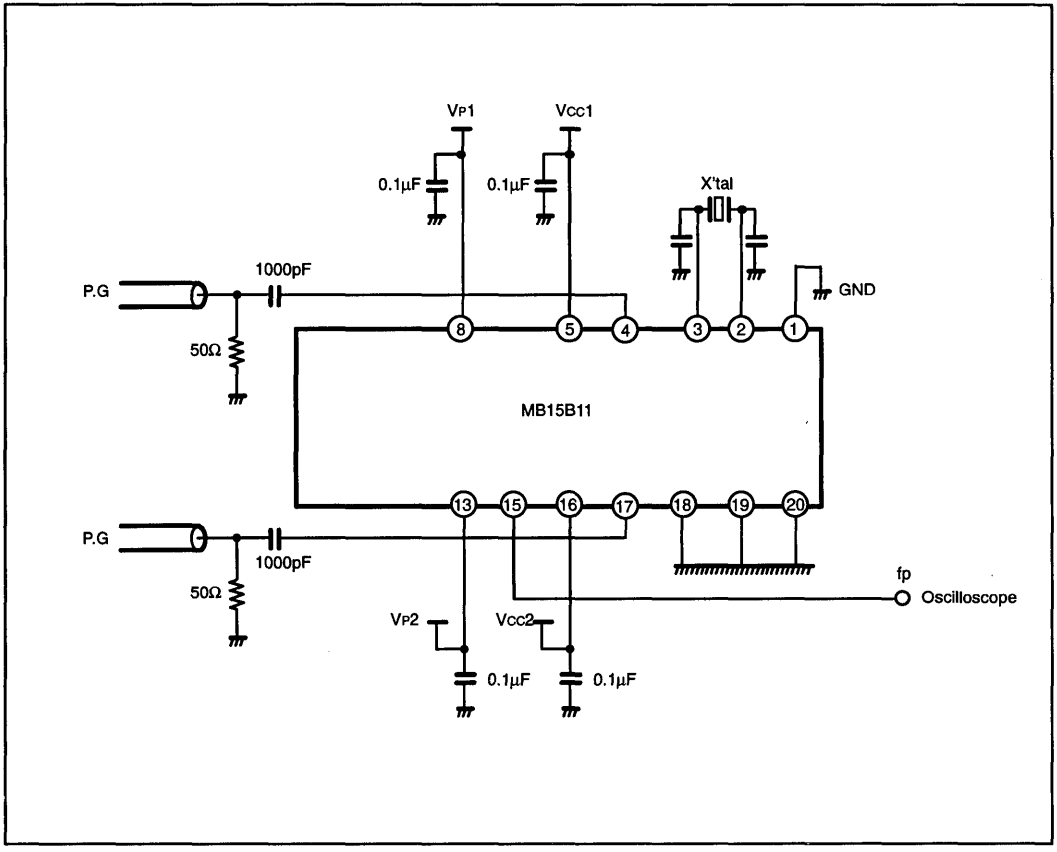
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

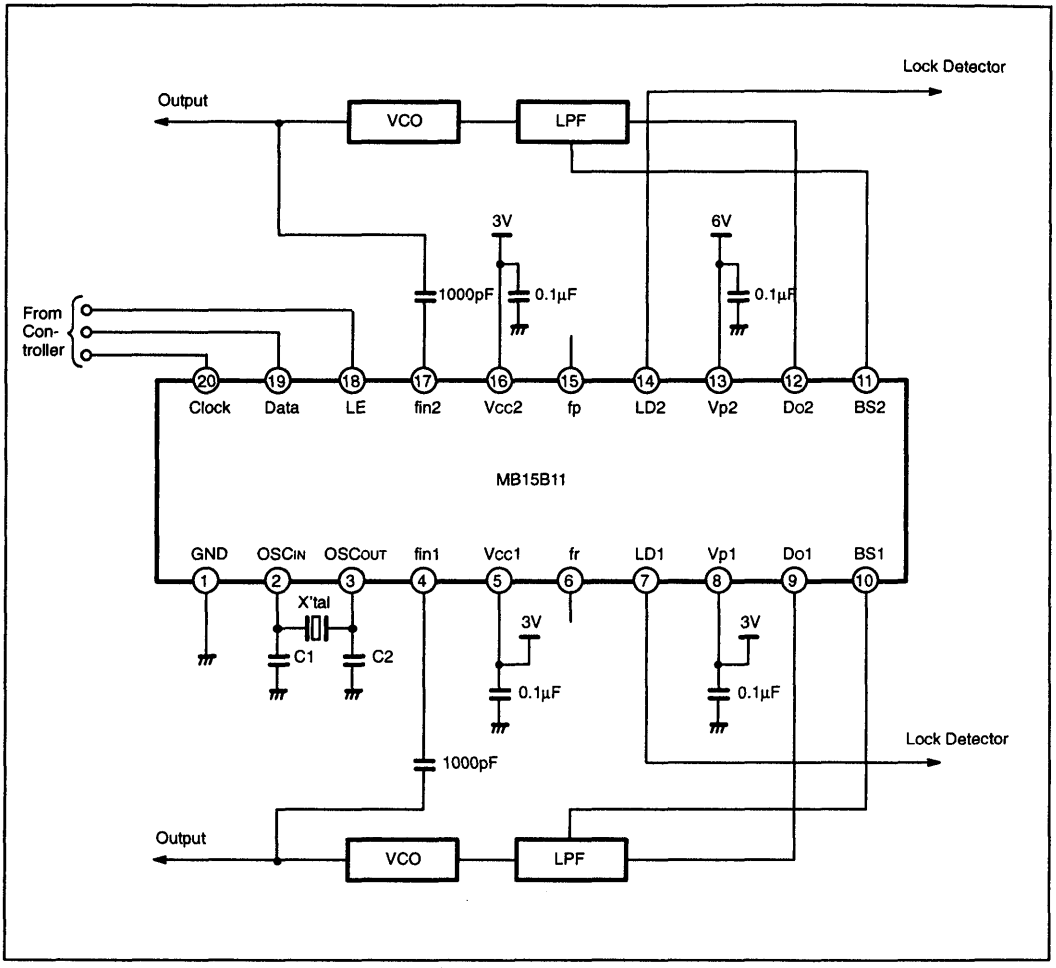
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC1}	PLL1 section	–	3.5(0.1) *1	–	mA
		I_{CC2}	PLL2 section	–	6.0(0.1) *1	–	
Operating Frequency	fin1	fin1		100	–	400	MHz
	fin2	fin2		100	–	1100	
	OSC_{IN}	f_{OSC}		–	12.8	20.0	
Input Sensitivity	fin1	Pfin1	PLL1, 50Ω system	–10	–	4	dBm
	fin2	Pfin2	PLL2, 50Ω system	–10	–	4	dBm
	OSC_{IN}	V_{OSC}		0.5	–	–	Vp-p
High-level Input Voltage	Except fin and OSCin	V_{IH}		Vccx0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	Vccx0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High-level Output Voltage	Except Do and OSCout	V_{OH}	Vcc = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High-impedance Cutoff Current	Do, ΦP	I_{OFF}	Vp = Vcc to 8.0V, Voop = GND to 8.0V	–	–	1.1	µA
Output Current	Except Do and OSCout	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	Do1	I_{OH}	V_P = 6.0V	–	–1	–	mA
		I_{OL}	Vcc = 3.0V	–	12	–	
	Do2	I_{OH}	V_P = 6.0V	–	–3	–	mA
		I_{OL}	Vcc = 3.0V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	50	–	Ω

Notes: *1 : The value in ( ) is power supply current in power saving mode.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)

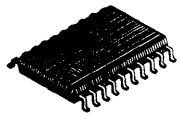


APPLICATION EXAMPLE



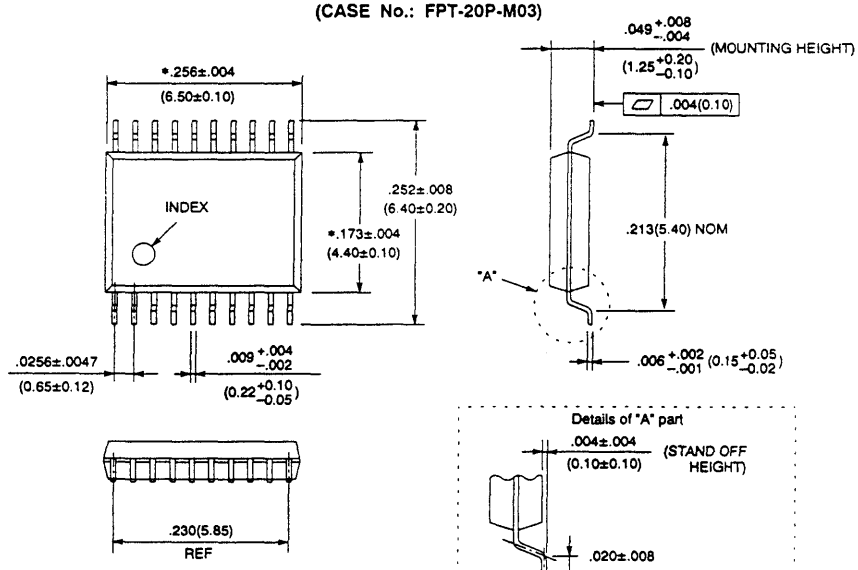
Note: X'tal ; 12.8MHz
C1, C2 : depends on a crystal oscillator.
Clock, Data, LE : involves a schmitt circuit.
(When inputs are open, pull up/down resistor is necessary to prevent self-oscillation.)
Vp1, Vp2 : 6V max.

PACKAGE INFORMATION



FPT-20P-M03

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

April 1995
Edition 2.0

FUJITSU

DATA SHEET

MB1511 ASSP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

4

DESCRIPTION

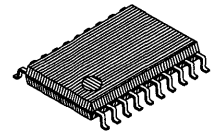
The Fujitsu MB1511 is a single chip serial input PLL frequency synthesizer designed for VHF tuner and cellular telephone applications.

It contains a 1.1 GHz dual modulus prescaler which enables pulse swallow function, and an analog switch to speed up lock up time.

It operates supply voltage of 3.0 V typ. and dissipates 7 mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

FEATURES

- Low power supply voltage: V_{CC} = 2.7 to 5.5 V
- High operating frequency: $f_{IN\ MAX}$ = 1.1 GHz ($P_{IN\ MIN}$ = –10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC} = 7 mA typ.
- Serial input 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter: 0 to 127
  Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 8 to 16383
  1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2 types of phase detector output
  On-chip charge pump (Bipolar type)
  Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 20-pin Plastic Shrink Small Outline Package (Suffix: –PFV)



Plastic Package
(FPT-20P-M03)

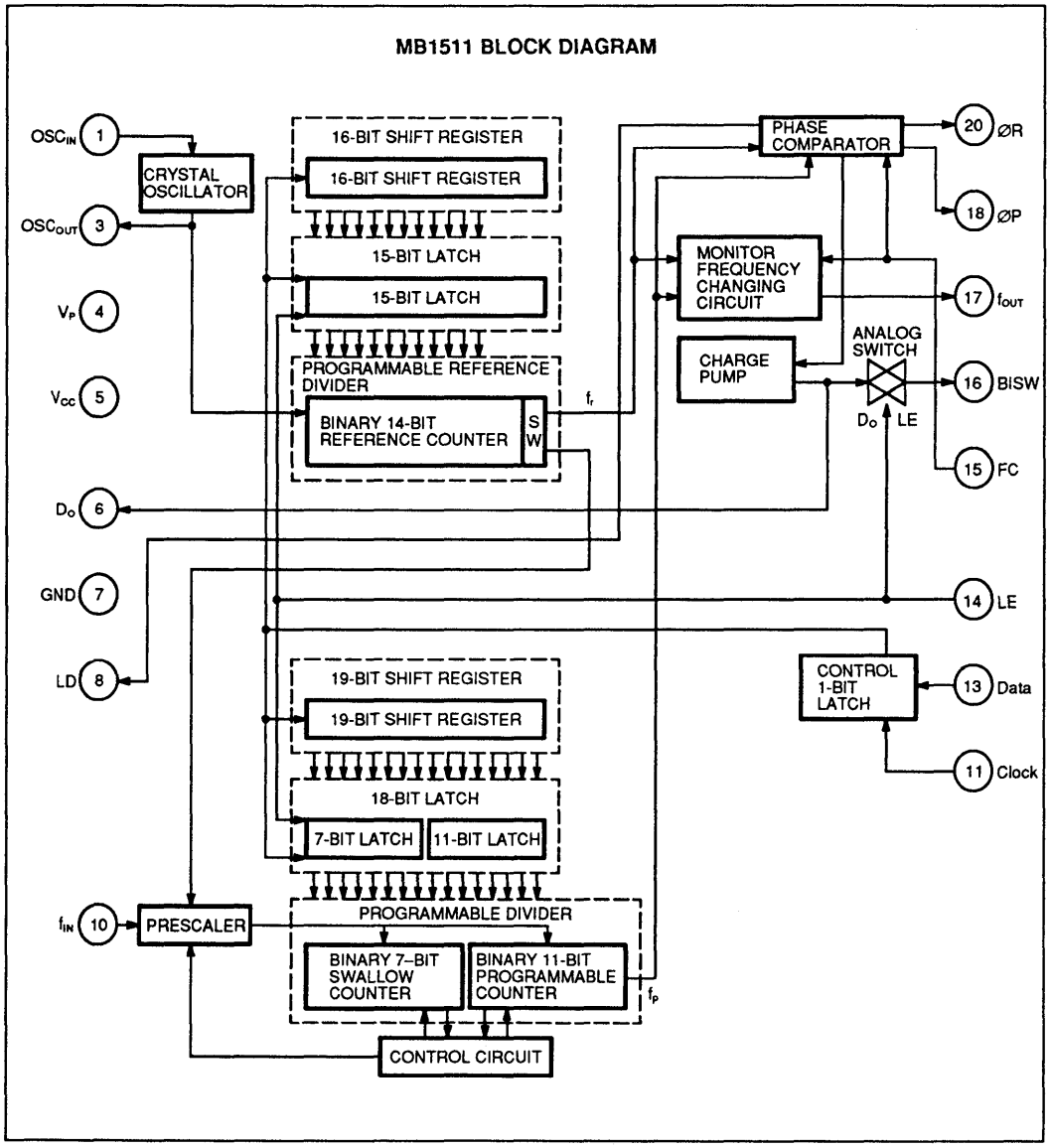
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Power Supply voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output voltage	V_{OUT}	–0.5 to V_{CC}+0.5	V
Open-drain voltage	V_{OOP}	–0.5 to 8.0	V
Output current	I_{OUT}	±10	mA
Storage temperature	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of theis data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1511 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
4	V_P	–	Power supply input for charge pump and analog switch.
5	V_{CC}	–	Power supply voltage input.
6	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
7	GND	–	Ground.
8	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r and f_p exists, this pin outputs low level.
10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
13	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
14	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output is connected to BISW pin because internal analog switch becomes ON state.
15	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal controls f_{out} pin (test pin) output level, f_r or f_p.
16	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump output.
17	f_{OUT}	O	Minitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
18 20	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.
2,9 12,19	NC	–	No connection.

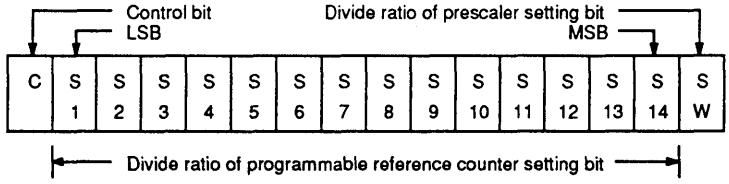
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



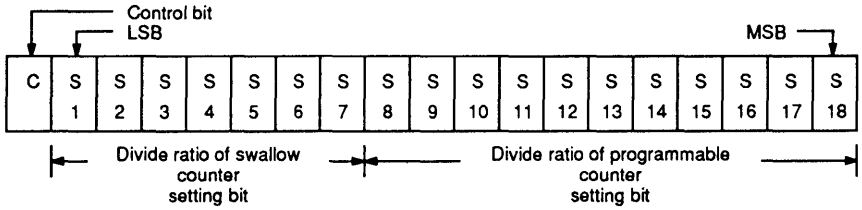
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64/65
SW=L : 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

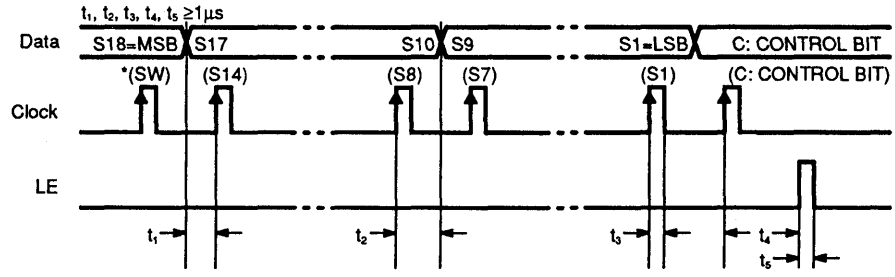
PULSE SWALLOW FUNCTION

The divide ratio is set using the following equation.

$f_{vco} = [MxN)+A] \times f_{osc}+R$

f_{vco}: Output frequency of external voltage controlled oscillator (VCO)
M: Preset modulus of external dual modulus prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{osc}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to16383)

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

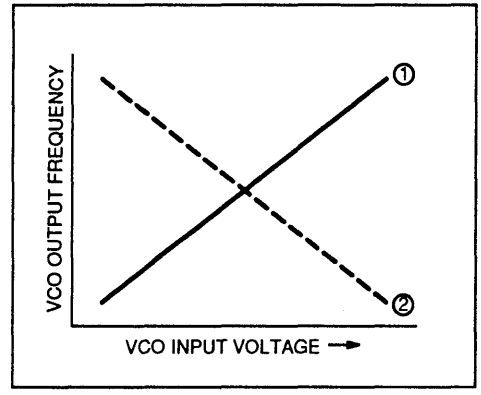
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (ϕR, ϕP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ϕR, ϕP) and FC input level are shown below.

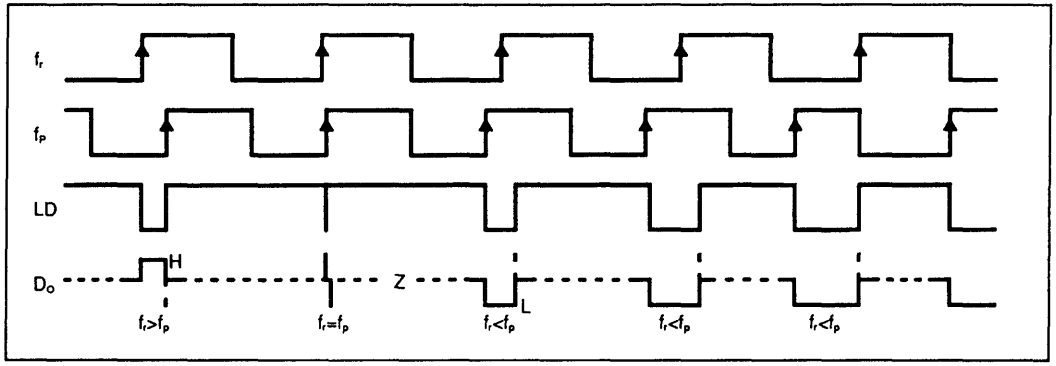
	FC=H or open				FC=L			
	D_O	ϕR	ϕP	f_{out}	D_O	ϕR	ϕP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set High or open circuit;
When VCO characteristics are like ②, FC should be set Low.



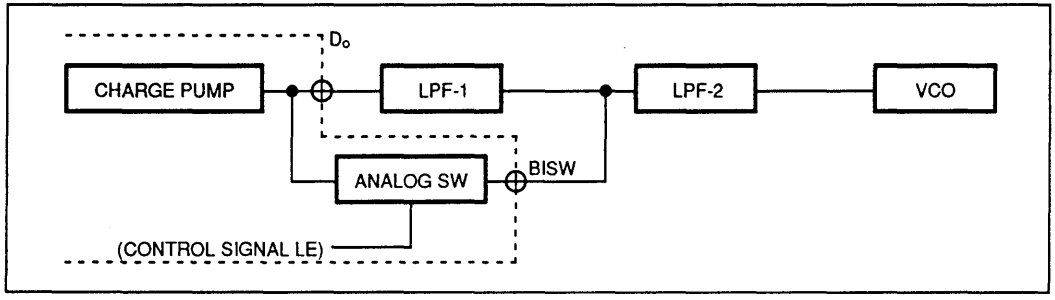
NOTES: Phase *difference detection range:* -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_o) is connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE	Analog Switch
H (Changing the divide ratio of intermal prescaler)	ON
L (Normal operating mode)	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up times is achieved to reduce LPF time constant during PLL channal switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input Voltage	V_I	GND	—	V_{CC}	V
Operating Temperature	T_A	–40	—	85	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off befer inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handing or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

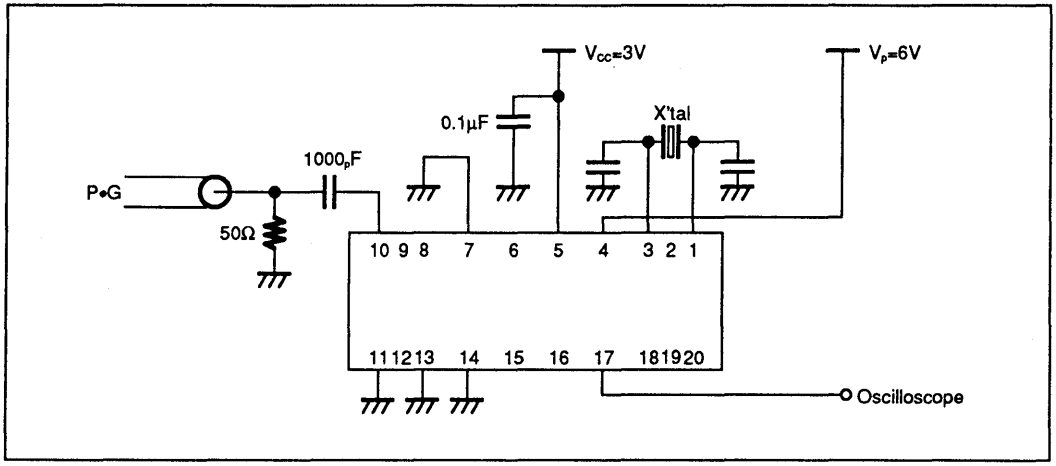
(VCC = 2.7 V to 5.5 V, Ta = -40°C to +85°C)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply current*1		I_{CC}	—	7.0	—	mA
Operating frequency	fin*2	f_{IN}	10	—	1100	MHz
	OSCIN	f_{OSC}	—	12	20	MHz
Input sensitivity	fin-1*3	Pfin1	–4	—	6	dBm
	fin-2*4	Pfin2	–10	—	6	dBm
	OSCIN	V_{OSC}	0.5	—	—	Vp-p
High-level input voltage	Except fin and OSC_{IN}	V_{IH}	VCC×0.7	—	—	V
Low-level input voltage		V_{IL}	—	—	VCC×0.3	V
High-level input current	Data clock	I_{IH}	—	1.0	—	µA
Low-level input current		I_{IL}	—	–1.0	—	µA
Input current	OSC_{IN}	I_{OSC}	—	+50	—	µA
	LE, FC	I_{LE}	—	-60	—	µA
High-level output current	Except DO and OSC_{OUT}	V_{OH}*5	2.2	—	—	V
Low-level output current		V_{OL}	—	—	0.4	V
N-channel open drain cutoff current	DO, Øp*6	I_{OFF}	—	—	1.1	µA
Output current	Except DO and OSC_{OUT}	I_{OH}	–1.0	—	—	µA
		I_{OL}	1.0	—	—	µA
Analog switch on resistance		R_{ON}	—	50	—	Ω

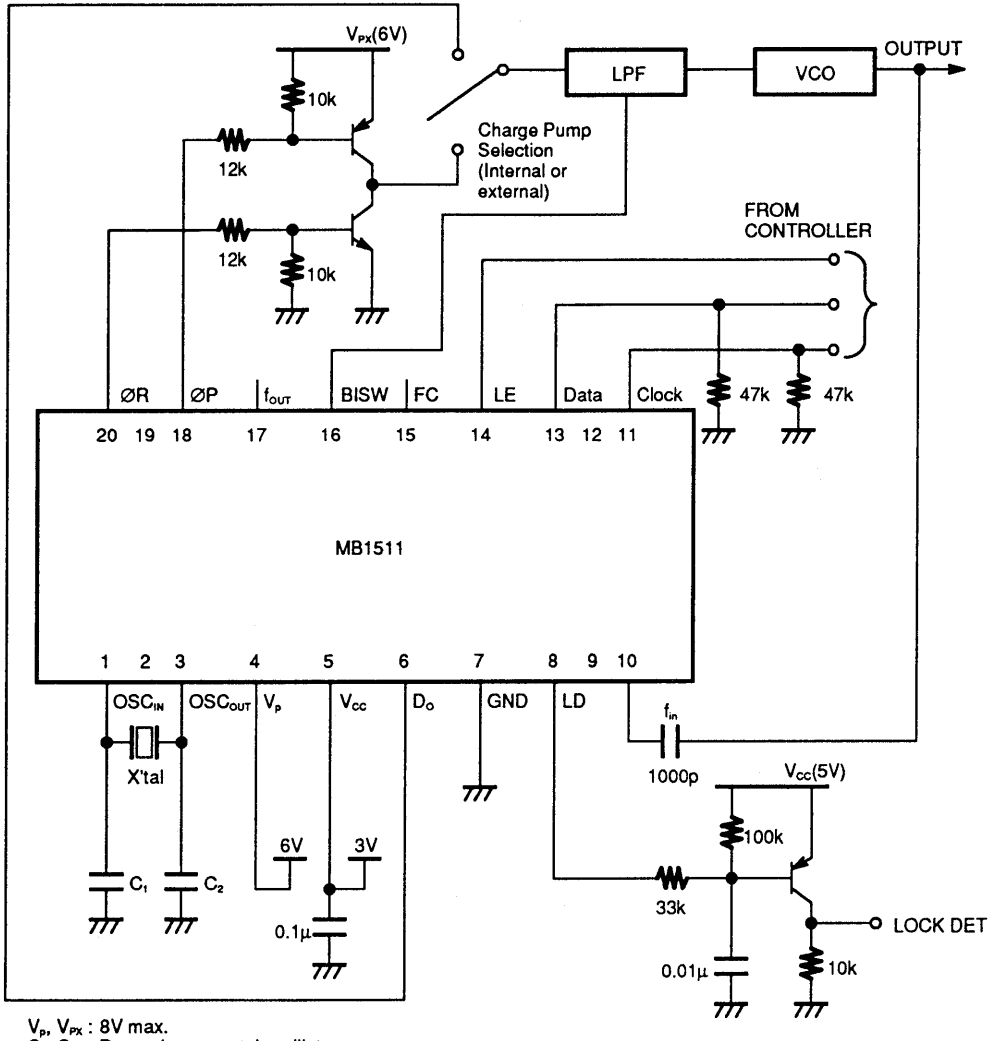
Notes:

1. fin =1.1 GHz, OSCIN=12 MHz, VCC=3V. Inputs are grounded and outputs are open.
2. AC coupling. Minimum operating frequency is measured when a capacitor 1000pF.
3. VCC=4.0 to 5.5V, 50Ω
4. VCC=2.7 to 4.0V, 50Ω
5. VCC=3V
6. VP=VCC to 8V, VOOP=GND to 8V

TEST CIRCUIT



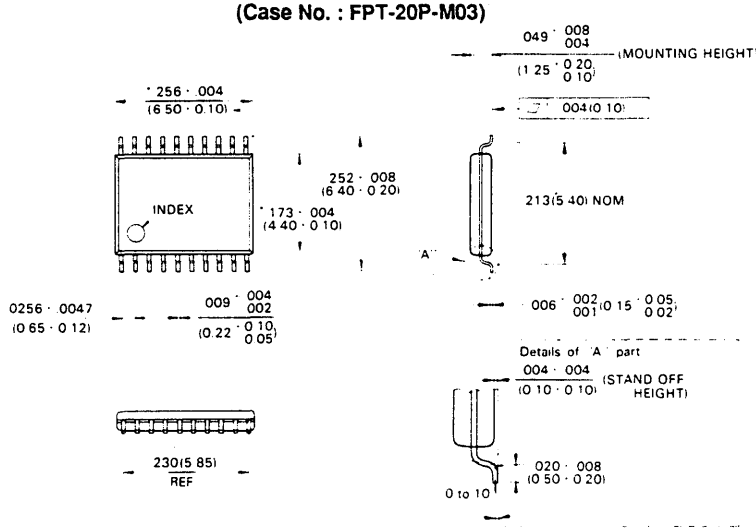
TYPICAL APPLICATION EXAMPLE



V_P, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-20P-M03)



* : This dimension does not include resin protrusion

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0a

FUJITSU

DATA SHEET

MB1512

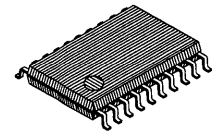
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

4

LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 1.1GHz PRESCALER

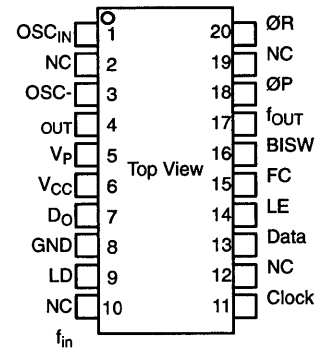
The Fujitsu MB1512, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.
The MB1512 contains a 1.1 GHz two modulus prescaler that can select of either 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analog switch to speed up lock up time.
It operates with a supply voltage of 5V typ. and achieves very low supply current of 8mA typ. realized through the use of Fujitsu Advanced Process Technology.

- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($P_{IN\ MIN}$=–10dBm)
- Pulse swallow function: 64/65 or 128/129
- Power supply voltage: V_{CC}=4.5 to 5.5V
- Low supply current: I_{CC}=8mA typ.
- Serial input 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter: 0 to 127
  Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 8 to 16383
  1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2types of phase detector output
  On-chip charge pump (Bipolar type)
  Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 20-pin Plastic Shrink Small Outline Package



PLASTIC PACKAGE
FPT-20P-M03

PIN ASSIGNMENT



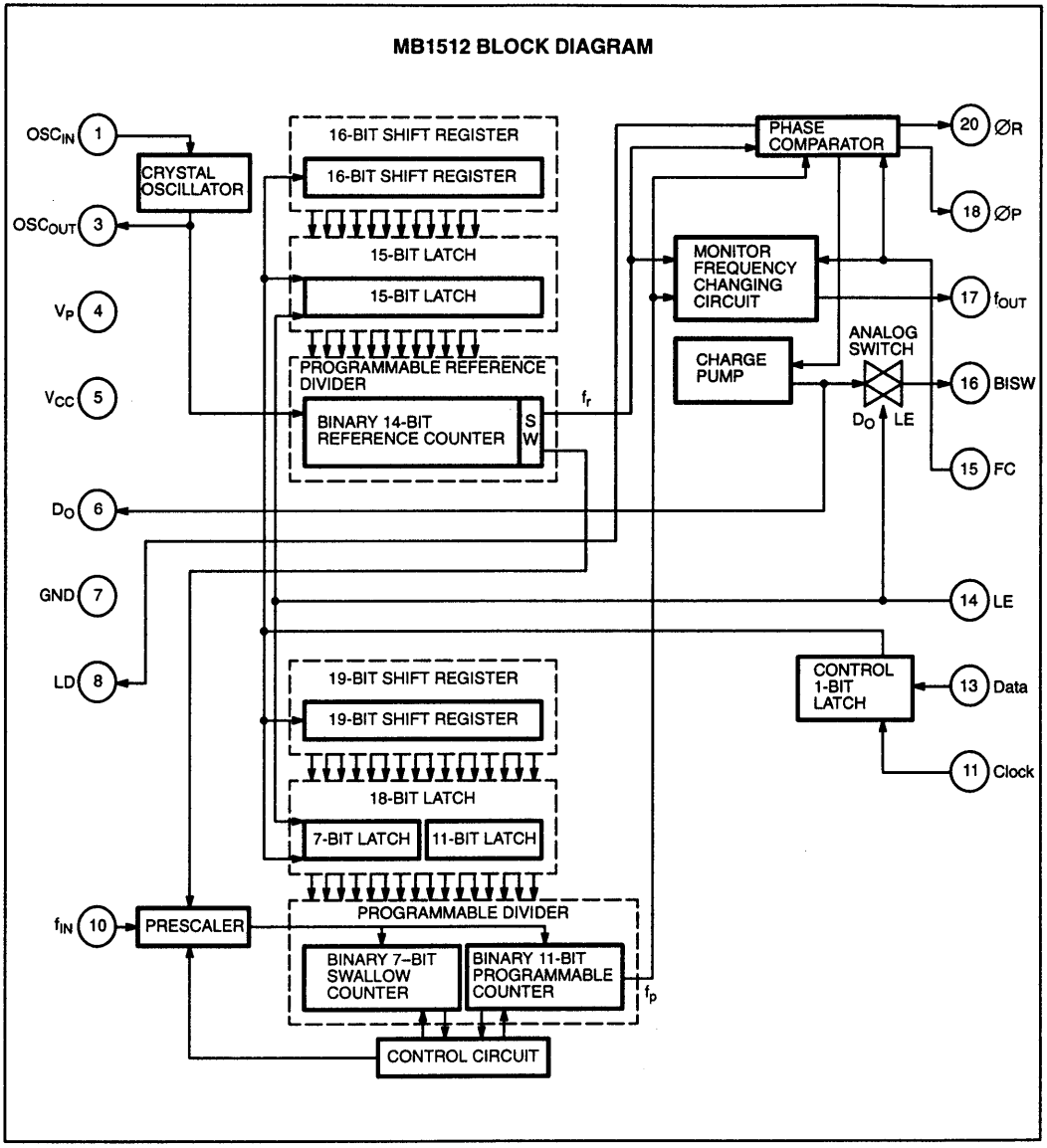
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 0.8	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB1512 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
4	V_P	–	Power supply input for charge pump and analog switch.
5	V_{CC}	–	Power supply voltage input.
6	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
7	GND	–	Ground.
8	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r and f_p exists, this pin outputs low level.
9	NC	–	No connection.
10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
12	NC	–	No connection.
13	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
14	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
15	FC	I	Phse select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control f_{out} pin (test pin) output level, f_r or f_p.
16	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
17	f_{OUT}	O	Minitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
18 20	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.
2 19	NC	–	No connection.

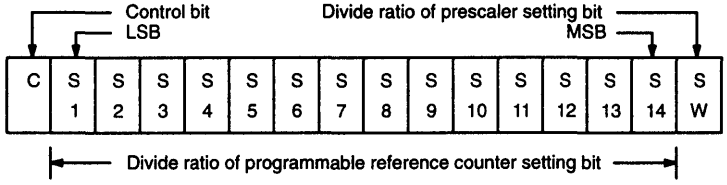
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



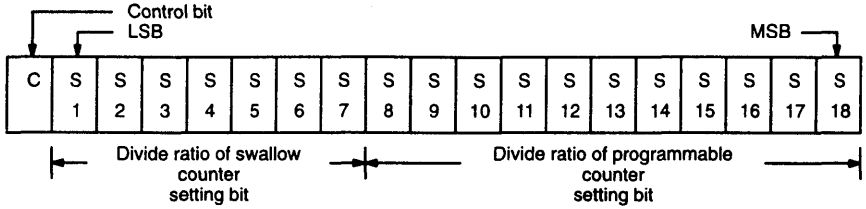
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64/65
SW=L : 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	Ø
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

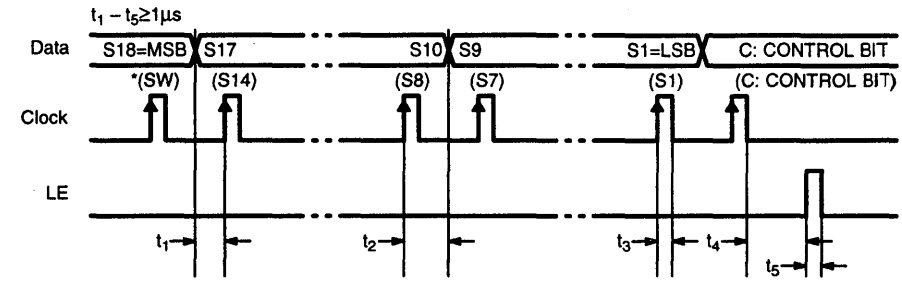
NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{VCO} = [(PxN)+A] \times f_{OSC} + R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to16383)
P: Preset modulus of external dual modulus prescaler (64 or 128)

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

PHASE CHARACTERISTICS

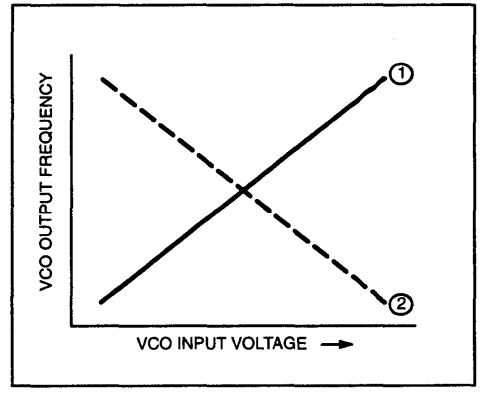
FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (ØR, ØP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ØR, ØP) and FC input level are shown below.

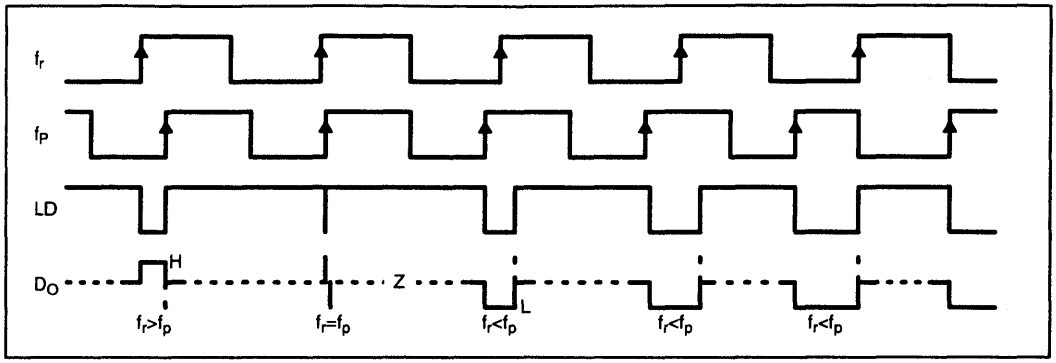
	FC=H or open				FC=L			
	D_O	ØR	ØP	f_{out}	D_O	ØR	ØP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

Note: Z=(High impedance)

Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set high or open circuit;
When VCO characteristics are like ②, FC should be set Low.

VCO CHARACTERISTICS





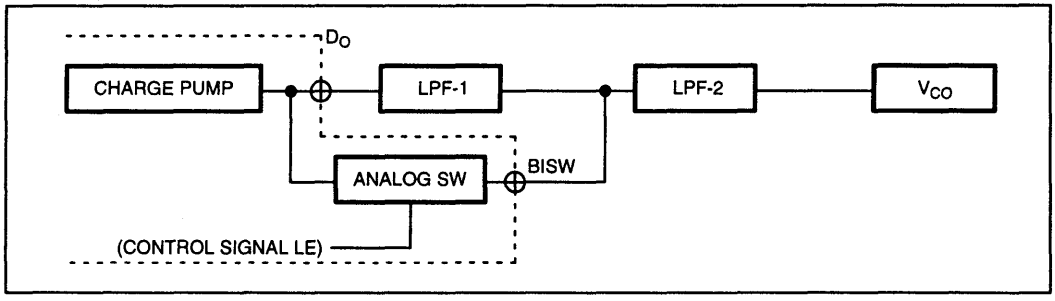
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) to be connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode) : Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

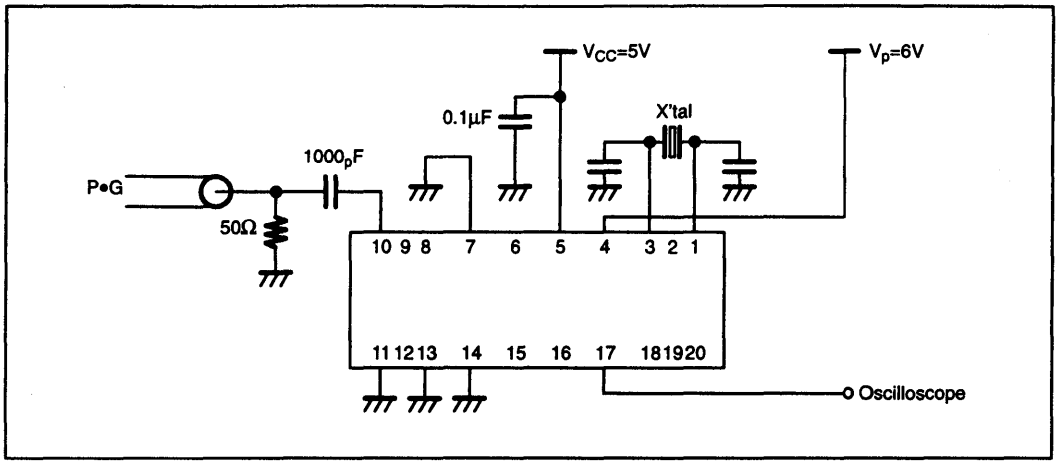
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	–	8.0	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	−40	–	+85	°C

ELECTRICAL CHARACTERISTICS

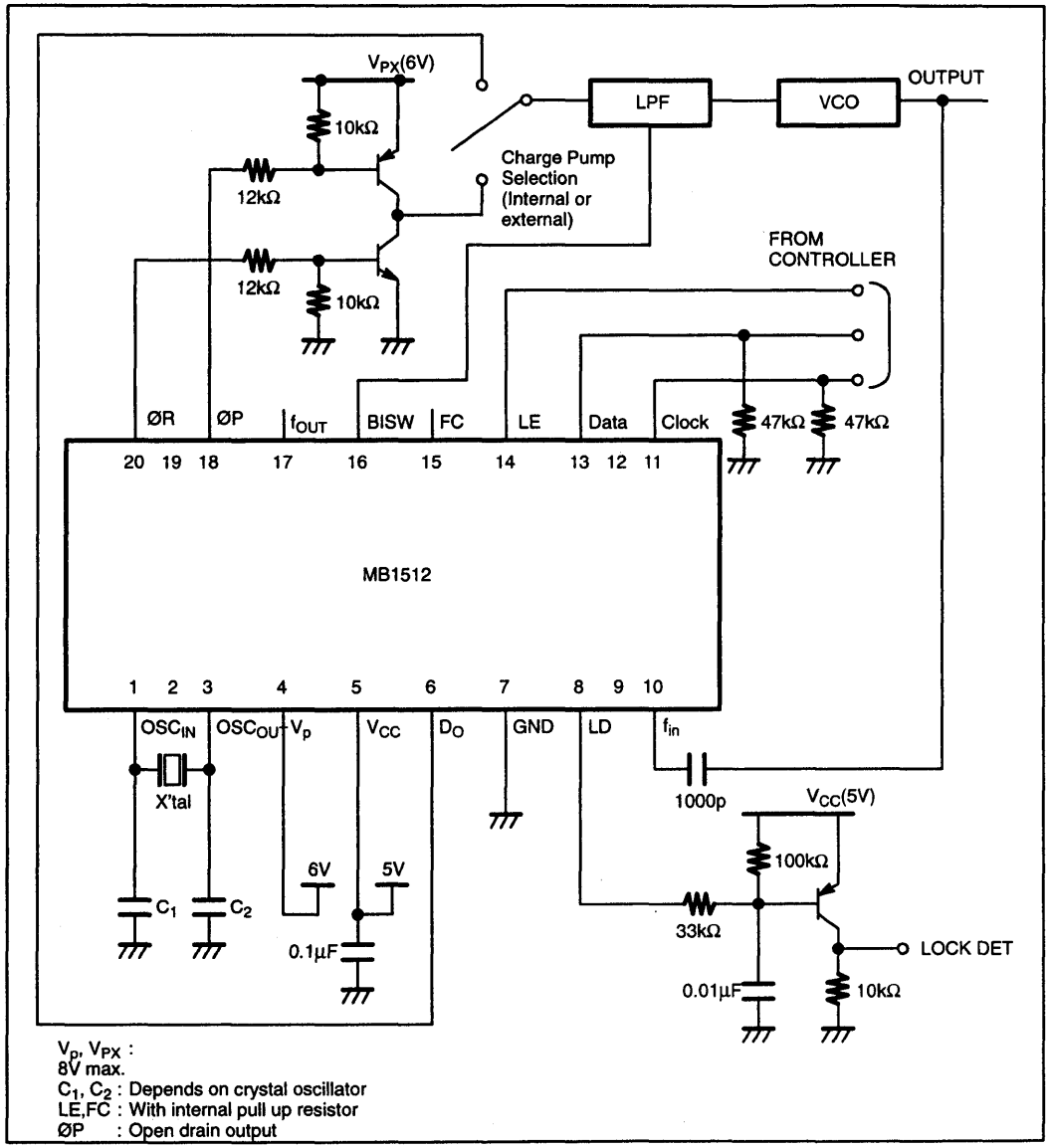
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1	–	8.0	12.0	mA
Operating Frequency	f_{in}	f_{in}	Note 2	10	–	1100	MHz
	OSC_{IN}	f_{OSC}		–	12	20	MHz
Input Sensitivity	f_{in}	Pf_{in}		–10	–	6	dBm
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		V_{CC}x0.7	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	µA
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	µA
	LE, FC	I_{LE}		–	–60	–	µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4	–	–	V
Low-level Output Current		V_{OL}		–	–	0.4	V
N-channel Open Drain Cutoff Current	D_O, ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$	–	–	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	mA
Analog Switch On Resistor		R_{ON}		–	25	–	Ω

NOTE 1: f_{in}=1.1GHz, OSC_{IN}=12MHz, V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT



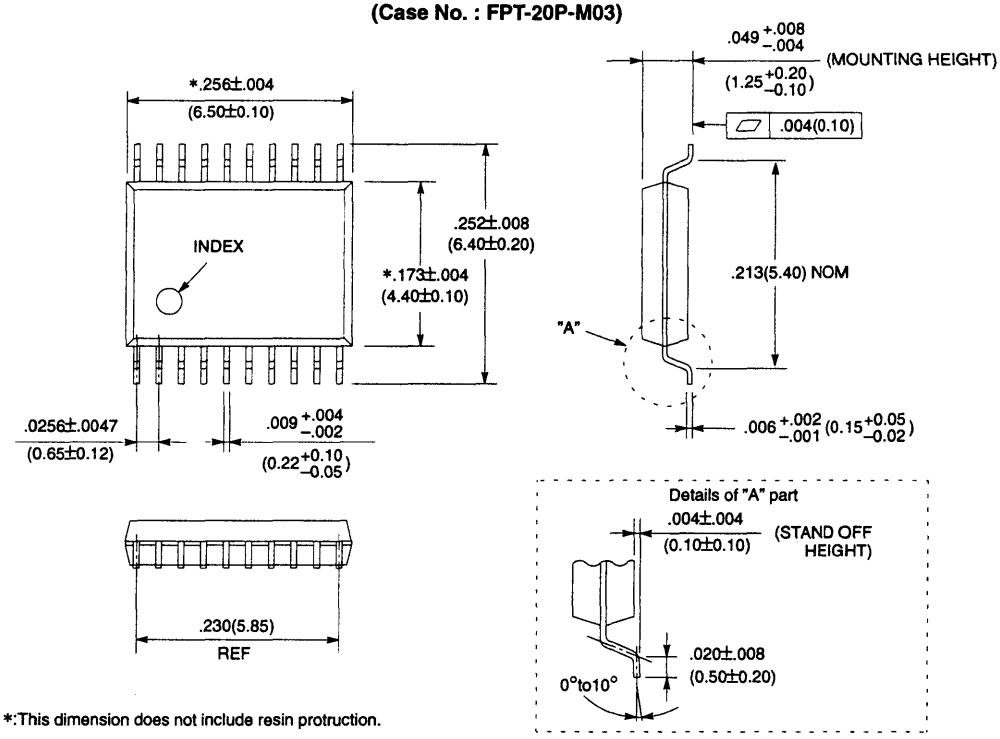
TYPICAL APPLICATION EXAMPLE



V_p, V_{PX} :
8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0b

FUJITSU

DATA SHEET

MB15B13

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

The Fujitsu MB15B13 is a 1.1 GHz dual serial input PLL (Phase Locked Loop) frequency synthesizer designed for cellular phones, cordless phones and other radio applications.
The MB15B13 has two PLL circuits on a single chip: PLL1 and PLL2. An analog switch is provided for each PLL circuit to decrease lock up time. Separate power supply pins are provided for each PLL circuit as well.
Two 1.1 GHz dual modulus prescalers are included inside and enables a pulse swallow function. It operates with a supply voltage of 3.0V typ. and dissipates 13 mA typ. of current realized through the use of Fujitsu's unique Bi-CMOS technology.

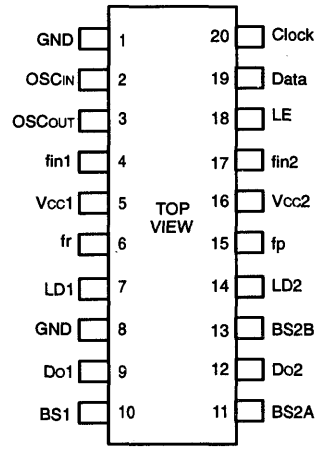
PRELIMINARY

4

FEATURES

- High operating frequency: fin = 1.1 GHz (Pin = −10 dBm, Vcc = 3V)
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 8 to 16383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 16 to 2047
  Tx and Rx programmable counters can be controlled independently.
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- Low power supply current: I_{CC} (total) = 13 mA typ. (Vcc = 3V)
- Power saving function : I_{CC1} = I_{CC2} = 100 µA typ (Vcc = 3V)
- On-chip analog switch to achieve fast lock up time for PLL1
- On-chip programmable switche controlled by PLL2 programming sequence
- Digital lock detector
- Wide operating temperature: T_A = −30 to 80°C
- Plastic 20-pin SSOP package

PIN ASSIGNMENT



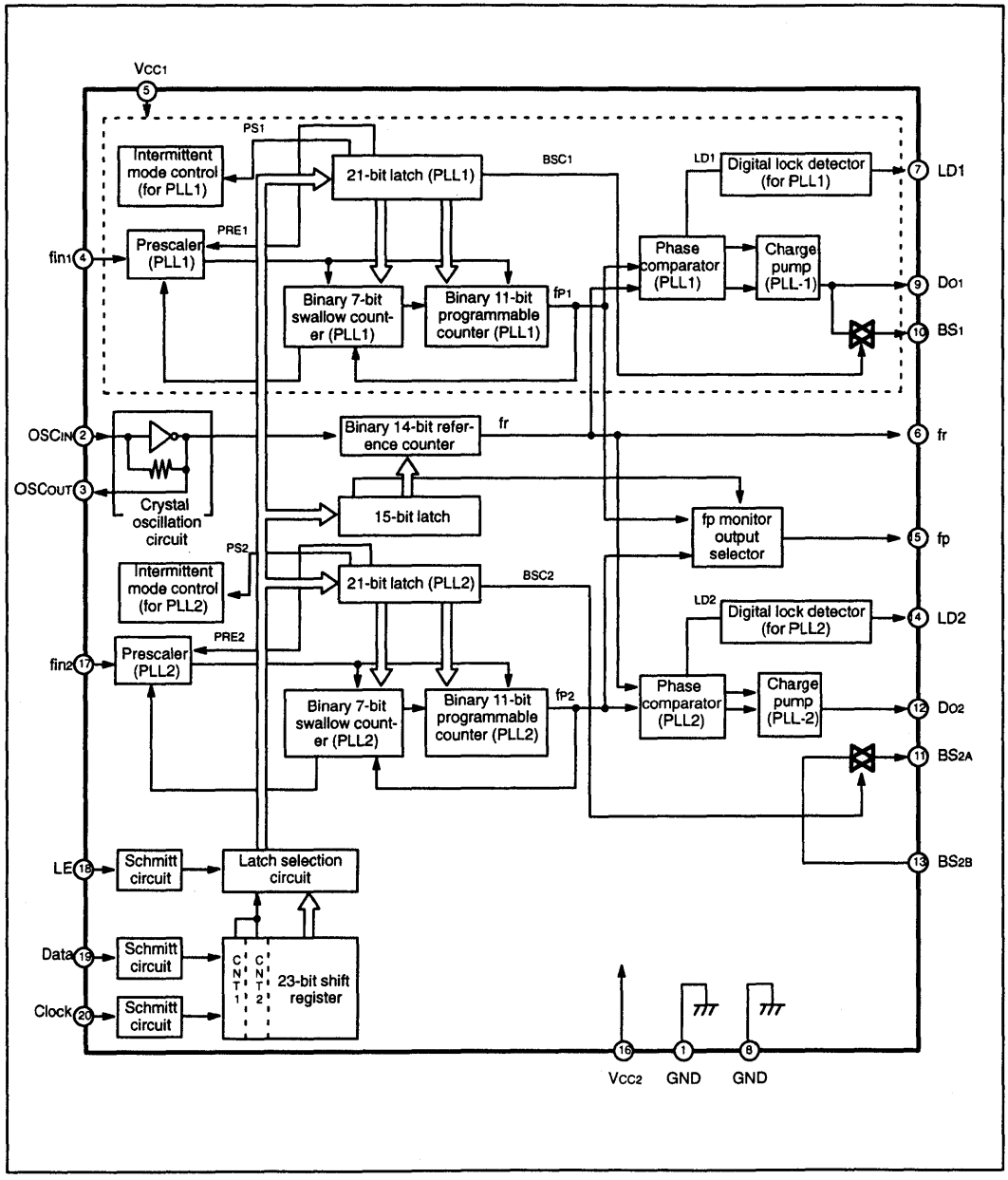
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Remark	Value	Unit
Power Supply Voltage	V_{CC}		−0.5 to 5.0	V
Output Voltage	V_{OUT}		−0.5 to V_{CC} +0.5	V
Open Drain Voltage	V_{OOP}	fr, fp	−0.5 to + 5.0	V
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSCIN
OSCOUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSCIN pin and OSCOUT pin.</td></tr>
<tr><td>4</td><td>fin1</td><td>I</td><td>Prescaler input pin of PLL1 section.
The connection with VCO should be AC.</td></tr>
<tr><td>5</td><td>Vcc1</td><td>–</td><td>Power supply voltage input pin of PLL1 section.
When power is OFF, latched data of PLL1 section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output. (Open drain output)</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of PLL1 section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>GND</td><td>–</td><td>Ground</td></tr>
<tr><td>9</td><td>Do1</td><td>O</td><td>Charge pump output pin of PLL1 section.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of PLL1 section, and controlled by BSC bit.</td></tr>
<tr><td>11</td><td>BS2A</td><td>I/O</td><td>Analog switch I/O pin of PLL2 section</td></tr>
<tr><td>12</td><td>Do2</td><td>O</td><td>Charge pump output pin of PLL2 section.</td></tr>
<tr><td>13</td><td>BS2B</td><td>I/O</td><td>Analog switch I/O pin of PLL2 section</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detection signal output pin of PLL2 section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output. (Open drain output)
This pin outputs divided frequency of PLL1 section or PLL2 section depending upon FP bit setting.
<table>
<tr><th>FP bit</th><th>Output</th></tr>
<tr><td>H</td><td>PLL1 section (fp1)</td></tr>
<tr><td>L</td><td>PLL2 section (fp2)</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	Vcc2	–	Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of PLL2 section and reference counter is cancelled.
17	fin2	I	Prescaler input pin of PLL2 section. The connection with VCO should be AC.
18	LE	I	Load enable input pin. This pin is followed by a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data.
19	Data	I	Serial data input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. The stored data in the shift register is transferred to one of PLL1 section, PLL2 section and programmable counter depending upon control data settings.
20	Clock	I	Clock input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. On rising edge of the clock, one bit of data is transferred into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$fvco = \{(P \times N) + A\} \times fosc \div R \quad (A < N)$

fvco: Output frequency of external voltage controlled ocillator (VCO)

P: Preset divide ratio of dual modulus prescaler (64 or 128)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

fosc: Reference oscillation frequency

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable divider of PLL1 section, programmable divider of PLL2 section and programmable reference divider are controlled individually.
Serial data of binary data is entered into Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Control bits		Destination of serial data
CNT1	CNT2	
L	L	Reference counter
L	H	Programmable counter of PLL1
H	H	Programmable counter of PLL2

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CNT1	CNT2	FP	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

R1 to R14 : Divide ratio setting bit for the programmable counter (8 to 16383)
FP : Test purpose bit (monitor output fp1/fp2 selection)
CNT1, 2 : Control bit

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CNT1	CNT2	PS	PRE	BSC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio setting bit for the programmable counter (16 to 2047)
A1 to A7 : Divide ratio setting bit for the swallow counter (0 to 127)
BSC : Analog switch control bit
PRE : Divide ratio setting bit for the prescaler (64/65, 128/129)
PS : Power saving control bit
CNT1, 2 : Control bit

BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 8 is prohibited.
• Divide ratio (R) range = 8 to 16383

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
V	V	V	V	V	V	V	V	V	V	V	V
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 16 is prohibited.
• Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
V	V	V	V	V	V	V	V
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

PRESCALER DATA SETTING

Divide Ratio	PRE
64/65	1
128/129	0

Note: • Divide ratio for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.

ANALOG SWITCH CONTROL DATA SETTING

BSC	Analog SW (PLL1)	Analog SW (PLL2)
L	High impedance	High impedance
H	Charge pump output	BS2A and BS2B connected

Note: • Selection of PLL1 or PLL2 is done by the control bits of CNT1 and CNT2. And each analog switch can be controlled individually.

POWER SAVING FUNCTION CONTROL (INTERMITTENT OPERATION)

	PS	
	H	L
PLL1's section	ON	OFF
PLL2's section and common section	ON	OFF

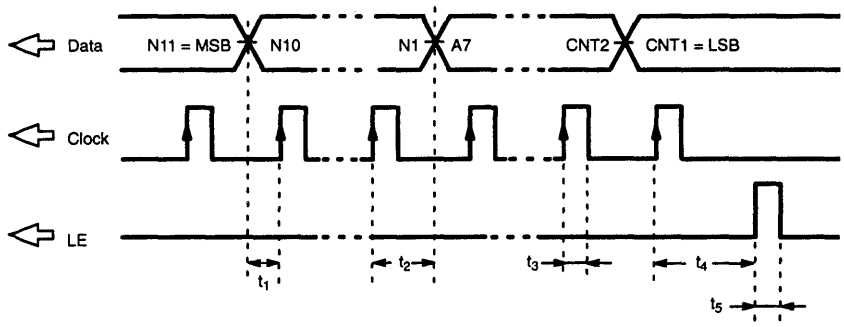
Note: • Power saving mode for each PLL1 and PLL2 is selected by the serial data at that time of divide ratio setting for each programmable divider.
• Common section ; Crystal oscilator circuit, reference counter

Intermittent operation limits power consumption by shutting down or start the internal circuits case by case. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost. To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting phase of both frequencies to limit the error signal output. This is done by the PS control circuit. If PS is set high, the circuit enter the operating mode. If PS is set low, operation stops and the device enters the stand-by mode.

The operating and stand-by modes alternate repeatedly. This intermittent operation limits the error signal by forcibly correcting the phase of the reference and comparison frequencies to limit power consumption.

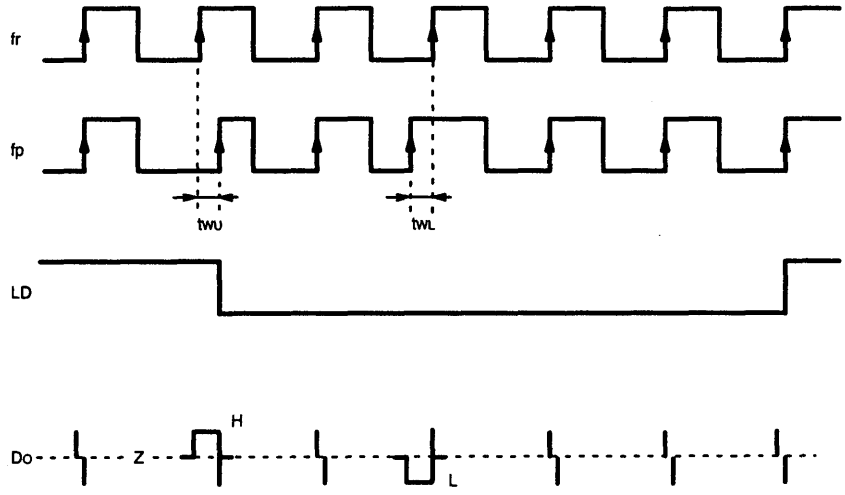
SERIAL DATA INPUT TIMING

t1 (>100ns) : Data set up time t2 (>1000ns) : Data hold time t3 (>300ns) : Clock pulse width
t4 (>100ns) : LE set up time to the rising edge of the last clock t5 (>800ns) : LE pulse width



On rising edge of the clock, one bit of the data is transferred into the shift register.

PHASE COMPARATOR OUTPUT WAVEFORM



Relation between phase comparator and charge pump output

	Do output
fr > fp	H
fr = fp	Z
fr < fp	L

Note: • Phase difference detection range = -2π to $+2\pi$

- LD output becomes low when phase difference is twu or more.
- LD output becomes high when phase difference is twL or less and continues to be so for three cysles or more.
- twL and twL depend on OSCin input frequency.
  twu ≧8/fosc (e. g. twu ≧625ns, foscin = 12.8 MHz)
  twL ≦16/fosc (e. g. twL ≦1250ns, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	Vcc	2.7	3.0	3.5	V	Vcc1 = Vcc2
Input Voltage	VIN	GND	–	Vcc	V	
Operating Temperature	TA	–30	–	+80	°C	
Analog Switch BS2 Current	IBS	–6	–	+6	mA	Vcc = 3.0V

HANDLING PRECAUTIONS

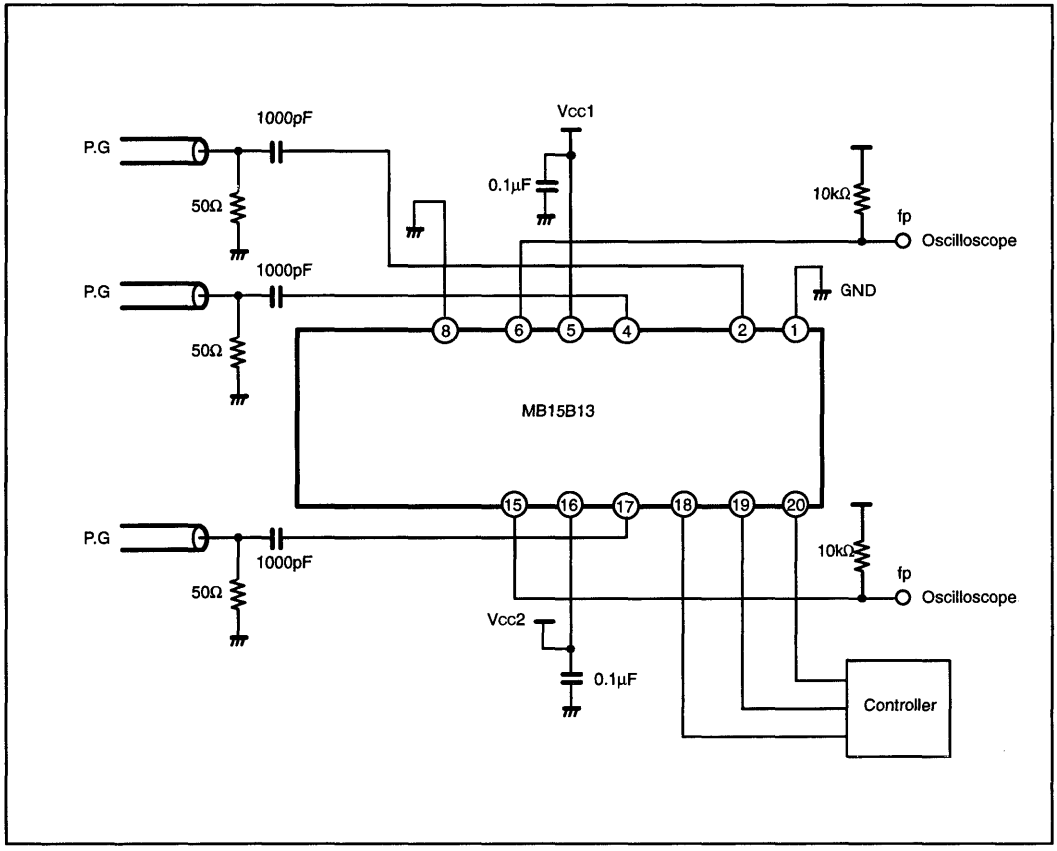
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

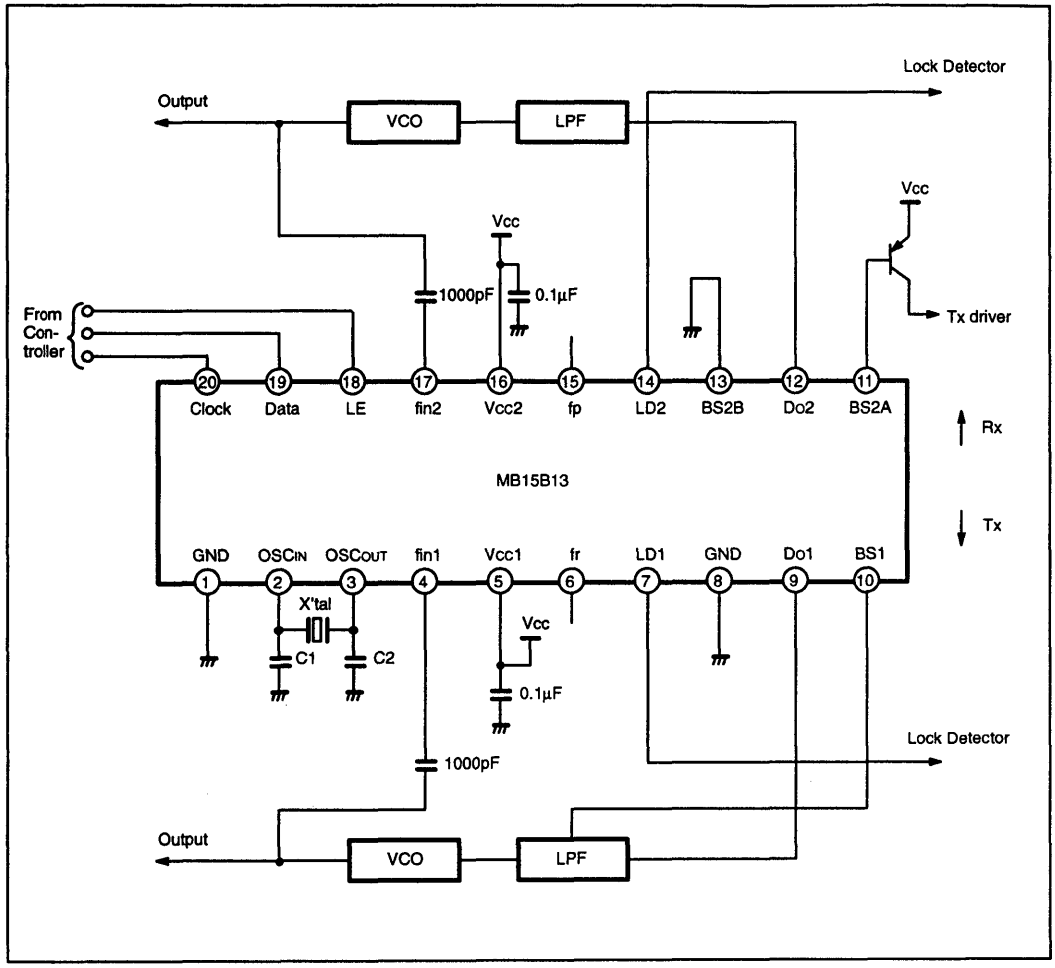
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC1}	PLL1 section	–	6.0 (0.1) *1	–	mA
		I_{CC2}	PLL2 & common sections	–	7.0 (0.1) *1	–	
Operating Frequency	fin	fin		100	–	1100	MHz
	OSCIN	fOSC		–	12.8	20.0	
Input Sensitivity	fin	Pfin	50Ω	–10	–	0	dBm
	OSCIN	VOSC		0.5	–	–	Vp-p
High-level Input Voltage	Data, Clock LE	V_{IH}		Vccx0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	Vccx0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSCIN	IOSC		–	±50	–	
High-level Output Voltage	LD	V_{OH}	Vcc = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}	Vcc = 3.0V	–	–	0.4	
High-impedance Cutoff Current	Do, BS	I_{OFF}		–	–	1.1	µA
Output Current	LD	I_{OH}		–1.0	–	–	mA
		I_{OL}		–	–	1.0	
	Do1, 2	I_{OH}	Vcc = 3.0V	–	–0.6 *2	–	mA
		I_{OL}	Vcc = 3.0V	–	6.0 *2	–	
Analog Switch ON Resistance		RON		–	50	–	Ω

Notes: *1 : The value in ( ) is power supply current in power saving mode.
*2 : L type charge pump which is similar to MB15A31's is used.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY)

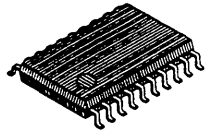


APPLICATION EXAMPLE



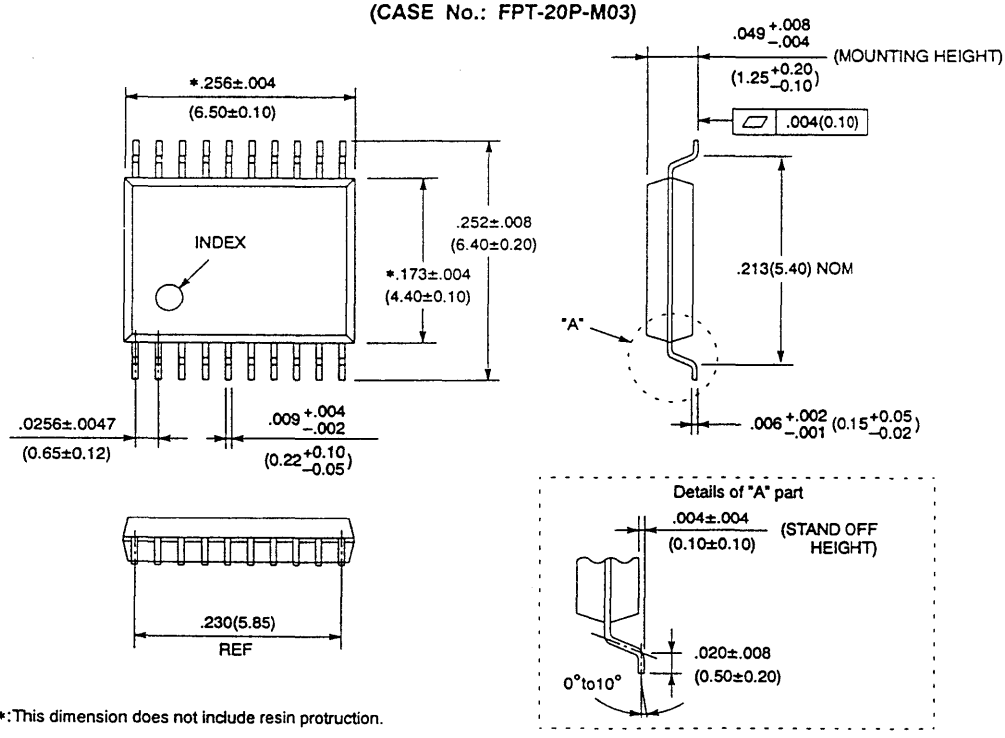
Note: C1, C2 : depends on a crystal oscillator.
Clock, Data, LE : involves a schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent oscillation.

PACKAGE INFORMATION



FPT-20P-M03

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*: This dimension does not include resin protruction.

Dimensions in inches (millimeters)

DS04–21316–1E

FUJITSU

DATA SHEET

MB1513

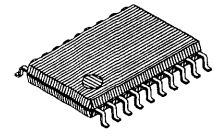
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTIONS (1.1GHz)

The Fujitsu MB1513 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. A stand-by mode is provided to limit power consumption during intermittent operation.

The MB1513 is configured of a 1.1 GHz dual-modulus prescaler with selectable 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter), analog switches, and an intermittent operation control circuit that selects the stand-by or operating mode depending on the power-save control input state (PS).

The MB1513 operates from a single +5 V supply. Fujitsu's advanced process technology achieves an I_{CC} of 8mA, typical. The stand-by mode current consumption is just 100µA.



PLASTIC PACKAGE (FPT-20P-M03)

FEATURES

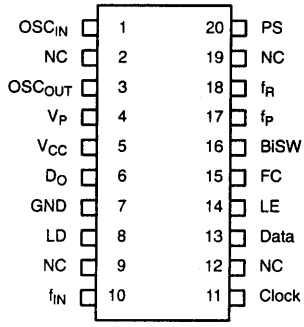
- High operating frequency : f_{IN} = 1.1GHz (P_{IN} = -10 dBm)
- *Pulse-swallow function* : *High-speed dual-modulus prescaler with selectable 128/129 divider ratio*
- Low supply current : I_{CC} = 8 mA typ. at 5V
- Power-saving stand-by mode : 100µA typ.
- Serial input, 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter : 0 to 127
  – Binary 11-bit programmable counter : 16 to 2,047
- Serial input 15-bit programmable reference divider consisting of:
  – Binary 14-bit programmable reference counter: 8 to 16,383
  – 1-bit switch counter sets prescaler divide ratio
- On-chip analog switch for fast lockup
- On-chip charge pump minimizes system component count
- Wide operating temperature range: –40 to +85°C
- Plastic 20–pin shrink small outline package (Suffix: PFV)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

PIN ASSIGNMENT

(TOP VIEW)

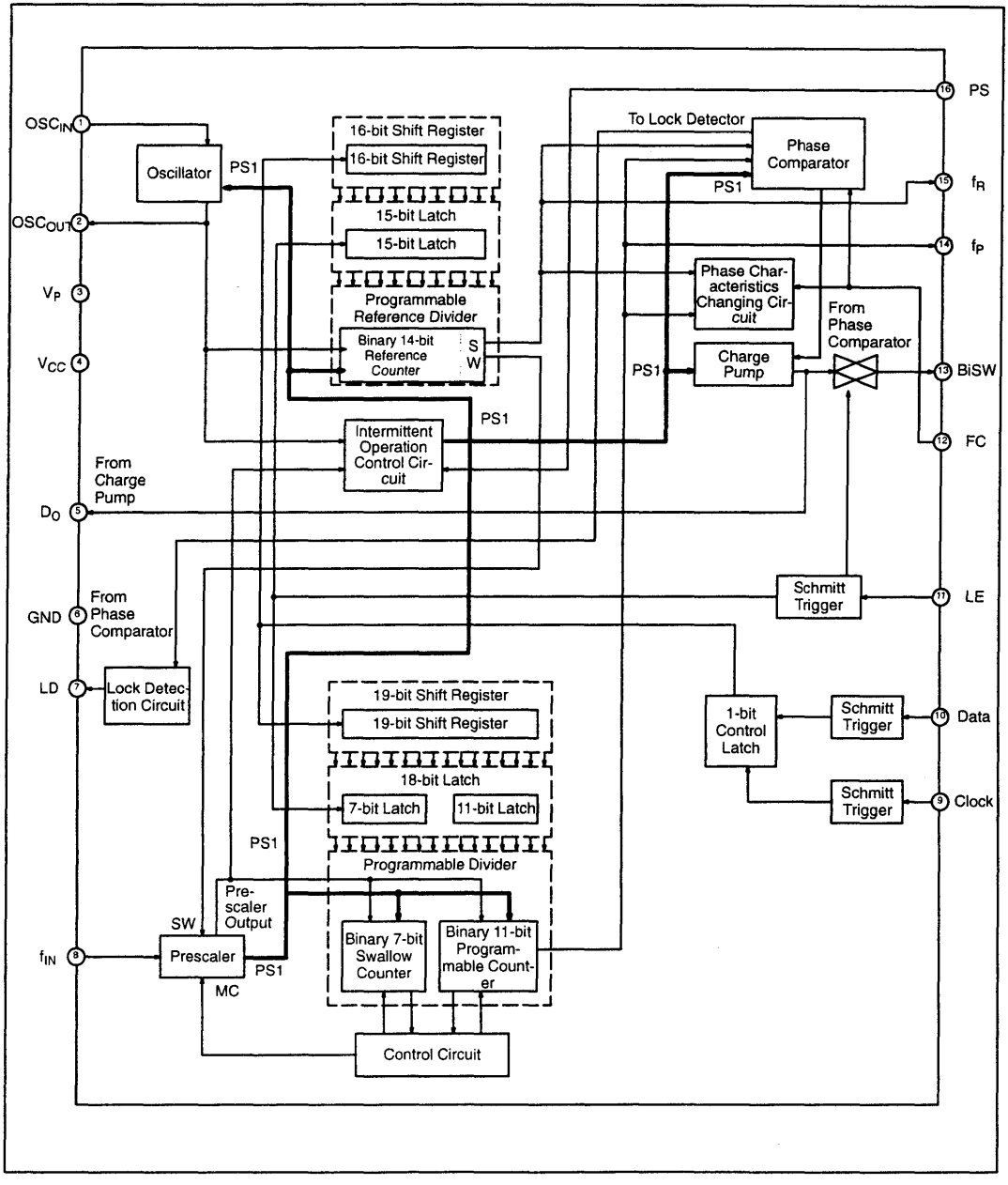


ABSOSUTE MAXIMUM RATINGS(See NOTE)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
	V_P	$V_{CC} \leq V_P \leq 10.0$	V
Output Voltage	V_O	−0.5 to V_{CC} +0.5	V
Output Current	I_O	±10	mA
Storage Temperature	Tstg	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input An external crystal is connected to this pin.
2	NC	–	No connection
3	OSC_{OUT}	O	Oscillator output An external crystal is connected to this pin.
4	V_P	–	Power supply input for charge pump and analog switch
5	V_{CC}	–	Power supply
6	D_O	O	Charge pump output The phase of the charge pump is reversed depending on the FC input.
7	GND	–	Ground
8	LD	O	Phase comparator output The output level is high when LD is locked. The output level is low when LD is unlocked.
9	NC	–	No connection
10	f_{IN}	I	Prescaler input An external VCO is AC-coupled to this pin.
11	Clock	I	Clock input for 19-bit and 16-bit shift registers One bit of data is shifted into the registers on the rising edge of the clock. A Schmitt trigger circuit is involved.
12	NC	–	No connection
13	Data	I	Binary serial data input The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 15-bit latch. When the control bit is low, data is transmitted to the 18-bit latch. A Schmitt trigger circuit is involved.
14	LE	I	Load enable signal input When LE is high, the contents of the shift register are transferred to a latch, depending on the control bit in the serial data. At the same time, an internal analog switch turns on and the output of the internal charge pump is connected to the BiSW pin. A Schmitt trigger circuit is involved.
15	FC	I	Phase select input of phase comparator (with internal pull-up resistor) When FC is low, the characteristics of the charge pump and the phase comparator are reversed. The FC input signal is also used to control the fOUT pin (test pin) of f_R or f_P.
16	BiSW	O	Analog switch output Usually, BiSW is in the high-impedance state. When the switch is on (LE is high), the charge pump is connected to the BiSW pin.
17	f_P	O	Programmable counter output monitor pins
18	f_R	O	Reference counter output monitor pin
19	NC	–	No connection
20	PS	I	Power save signal input Set low when the system is operating (never use pin 20 as it is opened) PS = High : Operation mode PS = Low : Stand-by mode

FUNCTIONAL DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

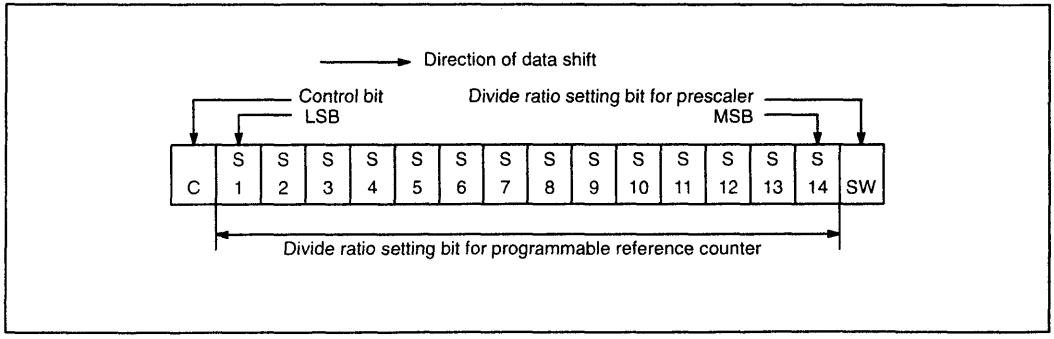
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)
- M : Preset divide ratio of prescaler (128)

Serial data input

Serial data is input using the Data, Clock, and LE pins. Serial data controls the 15-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is input to the Data pin.
One bit of data is shifted into the internal shift registers on the rising edge of the clock. When the load enable pin is high or open, stored data is latched, depending on the control as follows:

Control Data	Destination of Serial Data
H	15-bit latch
L	18-bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 15-bit latch and a 14-bit reference counter. The 16-bit serial data format is shown below:



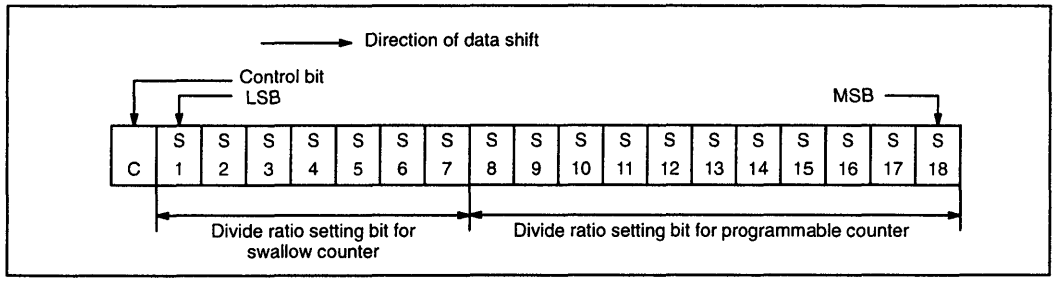
- 14-bit programmable reference counter divide ratio

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 8 to 16,383)

Notes: 1. Divide ratios less than 8 are prohibited
2. SW: This bit selects the divide ratio of the prescaler
SW Low: 128 or 129
(SW must be always be low.)
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (8 to 16,383)
4. C: Control bit: Set high
5. Data is input from the MSB.

(b) Programmable divider divide ratio
The programmable divider consists of a 19-bit shift register, 18-bit latch, 7-bit swallow counter, and an 11-bit programmable counter. The 19-bit serial data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

- 11-bit programmable counter divide ratio

Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

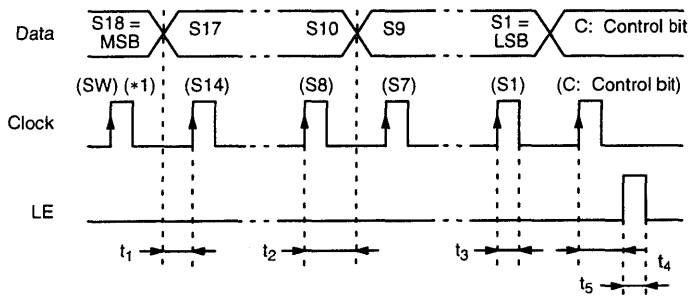
(Divide ratio = 16 to 2,047)

4

Notes: 1. Divide ratios less than 16 are prohibited for 11–bit programmable counters
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127)
3. S8 to S18: These bits select the divide ratio of programmable counter (16 to 2,047)
4. C: Control bit: (Set low)
5. Data is input from the MSB.

Serial data input timing

- t_1 (≥ 1µs) : Data setup time t_2 (≥ 1µs) : Data hold time t_3 (≥ 1µs) : Clock pulse width
  t_4 (≥ 1µs) : LE setup time to the rising edge of last clock t_5 (≥ 1µs) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Intermittent operation

Intermittent operation limits power consumption by shutting down or starting the internal circuits according to their necessity. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost. To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting the phase of both frequencies to limit the error signal output. This is done by the PS control circuit. If PS is set high, the circuit enters the operating mode. If PS is set low, operation stops and the device enters the stand-by mode. Each mode is explained below:

- Operating mode (PS = High)
  All circuits are operating, and PLL operation is normal.

- Stand-by mode (PS = Low)
  Circuits that do not affect operation are powered-down to save power.
  The current in the power save state is typically 100μA.
  At this time, the levels of D_O and LD are the same as when the PLL is locked.
  Since D_O is placed in the high-impedance state and the input voltage of the voltage-controlled oscillator (VCO) is set to the voltage in the operating mode (when locked) by the time constant of the low-pass filter, the frequency output from the VCO (f_{VCO}) is kept at the locking frequency.

The operating and stand-by modes alternate repeatedly. This intermittent operation limits the error signal by forcibly correcting the phase of the reference and comparison frequencies to limit power consumption.
The device must be set in the stand-by mode (PS = low) when it is powered up.

Relationship between FC input and phase characteristics

The FC pin controls the phase characteristics of the phase comparator. The internal charge pump output level (D_O) is reversed depending on the FC pin input level. The relationship between the FC input level and D_O is shown below:

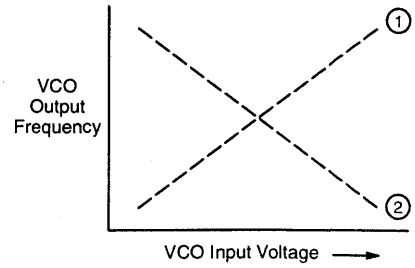
	FC = High or open	FC = Low
$f_R > f_P$	H	L
$f_R < f_P$	L	H
$f_R = f_P$	Z (*1)	Z (*1)

*1: High impedance

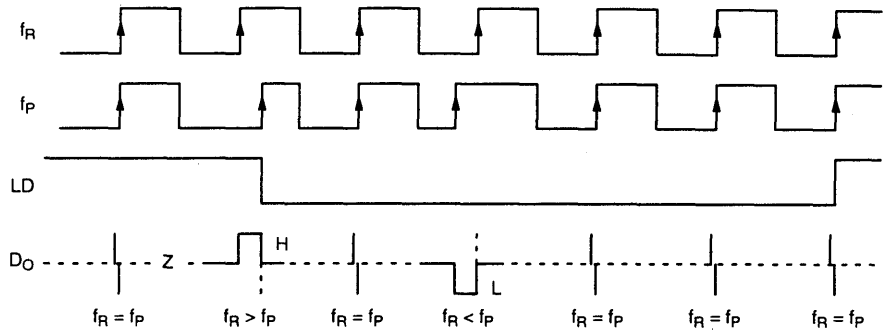
When designing a synthesizer, the FC pin setting depends on the VCO characteristics.

*: When the VCO characteristics are similar to ①, set FC high or open.

*: When the VCO characteristics are similar to ②, set FC low.



Phase comparator output waveform (FC = High)



Notes: 1. Phase difference detection range: -2π to $+2\pi$
2. Spike appearance depends on the charge pump characteristics. The spike is output to diminish dead band.
3. When $f_R > f_P$ or $f_R < f_P$, a spike might not appear, depending on the charge pump characteristics.
4. LD is low when the phase difference is tw or more. LD is high when the phase difference is tw or less for three or more continuous cycles (when f_{OSCIN} = 12.8 MHz, tw = 625 to 1,250 ns).

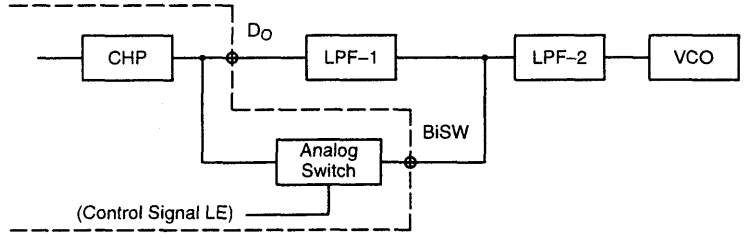
4

Analog switch

The LE signal turns the analog switch on or off. When the analog switch is turned on, the charge pump output (D_O) is output through the BiSW pin. When it is turned off, the BiSW pin is in the high-impedance state.

When LE = high (when the divide ratio of the internal divider is changed): Analog switch = on
When LE = low (normal operating mode): Analog switch = off

The LPF time constant can be decreased by inserting an analog switch between LPF1 and LPF2. This decreases the lock-up time when the PLL channel is changed.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	$V_{CC} \leq V_P \leq 8.0$			V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	–40	–	+85	°C

HANDLING PRECAUTIONS

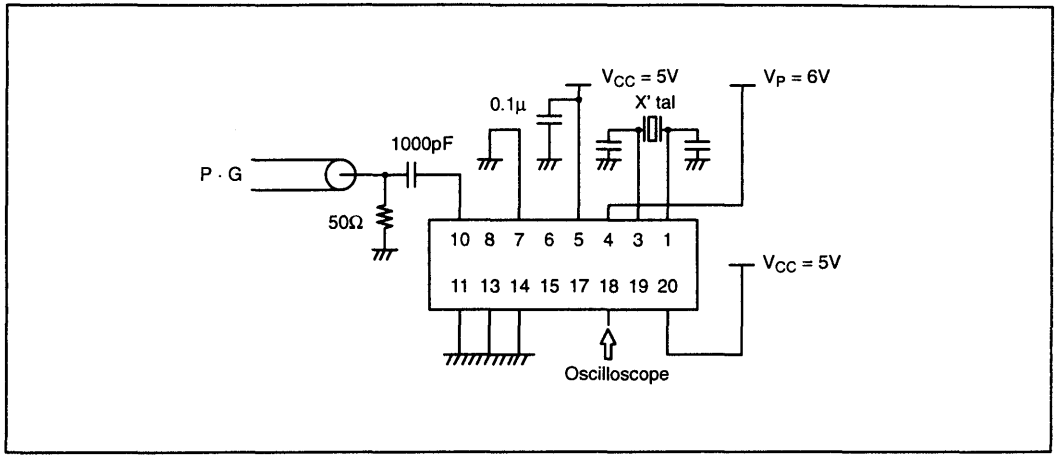
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

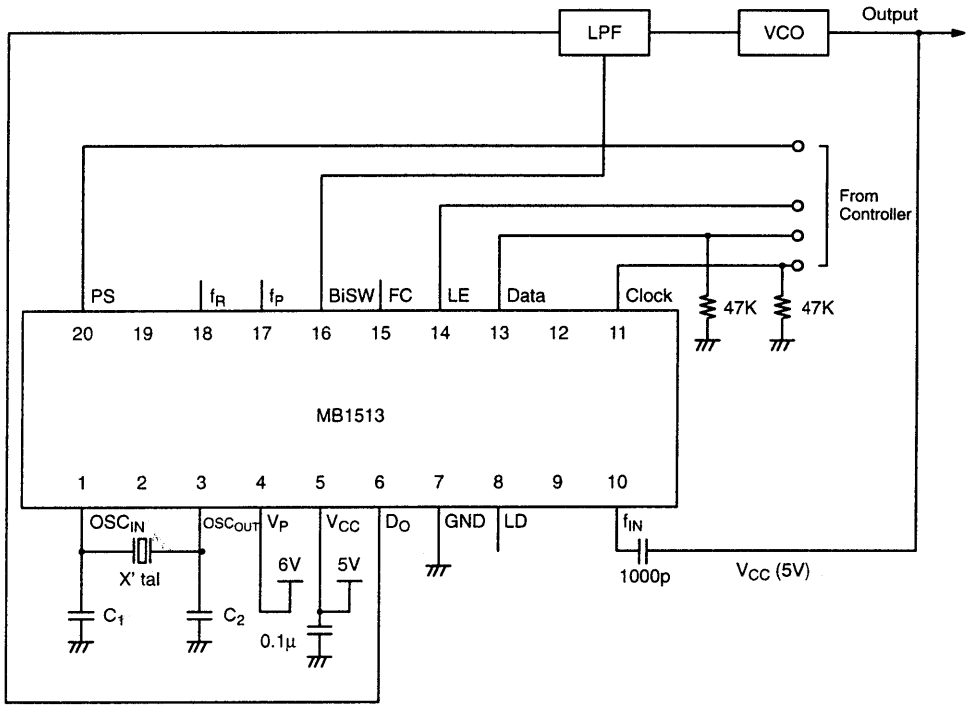
Parameter		Symbol	Value			Unit	Conditions
			Min	Typ	Max		
Supply Current		I_{CC}	–	8.0	–	mA	With f_{IN} = 1.1GHz, OSC_{IN} = 12MHz, V_{CC} = 5.0V
Stand-by Current		IPS	–	100	–	µA	–
Operating Frequency	f_{IN}	f_{IN}	10	–	1100	MHz	AC coupling.The minimum operating frequency is measured with a 1000pF capacitor connected
	OSC_{IN}	f_{OSC}	–	12	20	MHz	–
Input Sensitivity	f_{IN}	P_{fIN}	–10	–	6	dBm	–
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	–
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7+0.4	–	–	V	–
Low-level Input Voltage		V_{IL}	–	–	V_{CC} x 0.3–0.4	V	–
High-level Input Current	Data Clock LE	I_{IH}	–	1.0	–	µA	–
Low-level Input Current		I_{IL}	–	–1.0	–	µA	–
	FC	I_{FC}	–	–60	–	µA	–
Input Current	OSC_{IN}	I_{OSC}	–	±50	–	µA	–
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	4.4	–	–	V	V_{CC} = 5V
Low-level Output Voltage		V_{OL}	–	–	0.4	V	–
High-impedance Cut off Current	D_O	I_{OFF}	–	–	1.1	µA	V_{DO} = GND to 8V $V_{CC} \leq V_P \leq 8V$
Output Current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	–
		I_{OL}	1.0	–	–	mA	–
Analog Switch ON Resistance		R_{ON}	–	25	–	Ω	–

4

TEST CIRCUIT
(FOR MEASURING PRESCALER INPUT SENSITIVITY)



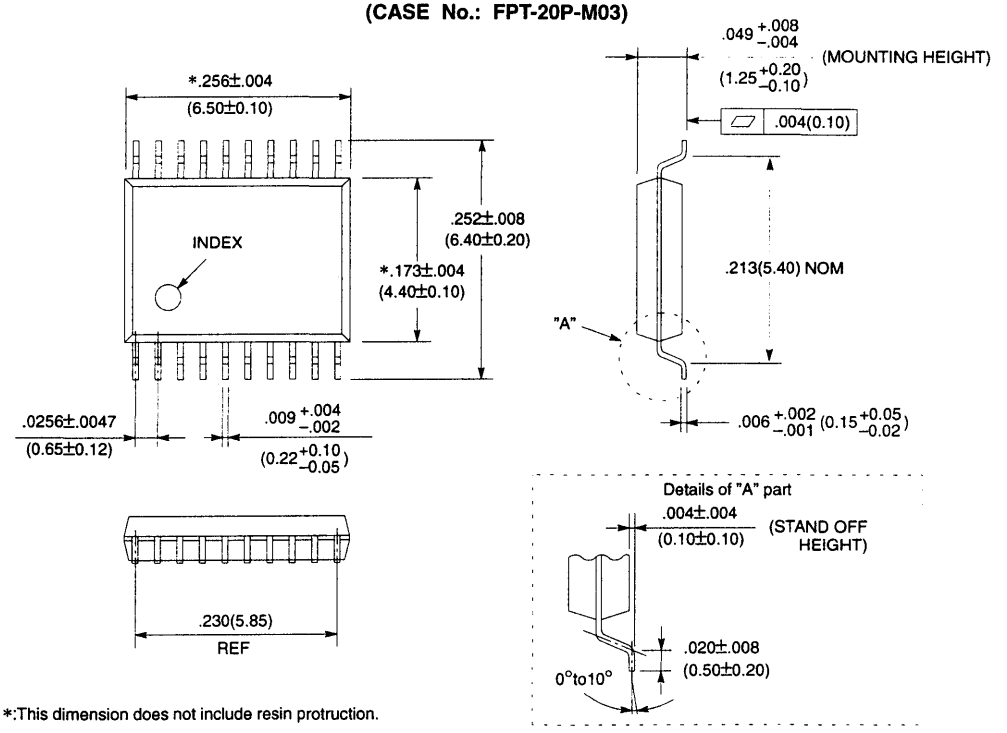
APPLICATION EXAMPLE



V_P, V_{PX} : Maximum 8V
C_1, C_2 : Depend on the crystal parameters

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0a

FUJITSU

DATA SHEET

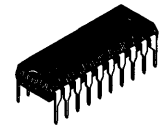
MB1514

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

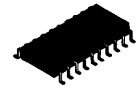
DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 400MHz PRESCALER

The Fujitsu MB1514 is a dual serial input PLL (phase locked loop) frequency synthesizer designed for cordless telephone applications.
The MB1514 has two PLL circuits on a single chip; one for transmission (PLL-1) and the other for reception (PLL-2). Separate power supply pins are provided for each PLL circuit. Transmission PLL contains a low sensitivity charge pump for modulation, and reception PLL contains a high sensitivity charge pump for fast lock-up time. 400MHz dual modulus prescalers are provided and enables a pulse swallow function.

MB1514 operates at 3.0 V typ. power supply voltage and dissipates 8mA typ. of current realized through the use of Bi-CMOS technology.



PLASTIC PACKAGE
DIP–20P–M02

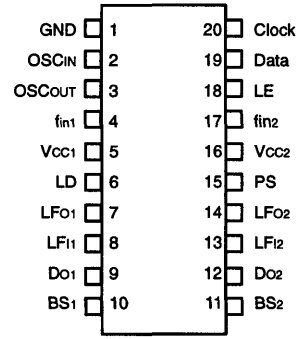


PLASTIC PACKAGE
FPT–20P–M01

FEATURES

- Low voltage operation : Vcc = 2.2V to 4.2V
- High operating frequency : fin = 400MHz (Pin = –10dBm, Vcc = 3.0V)
- Low current consumption : Icc = 8mA typ. (Vcc = 3V)
- Power saving function
- Two charge pumps
  Low sensitivity charge pump for transmission (PLL-1)
  High sensitivity charge pump for reception (PLL-2)
- Plastic 20-pin DIP package (Suffix: -P)
  Plastic 20-pin SOP package (Suffix: -PF)

PIN ASSIGNMENT



DIP–20P–M02/
FPT–20P–M01

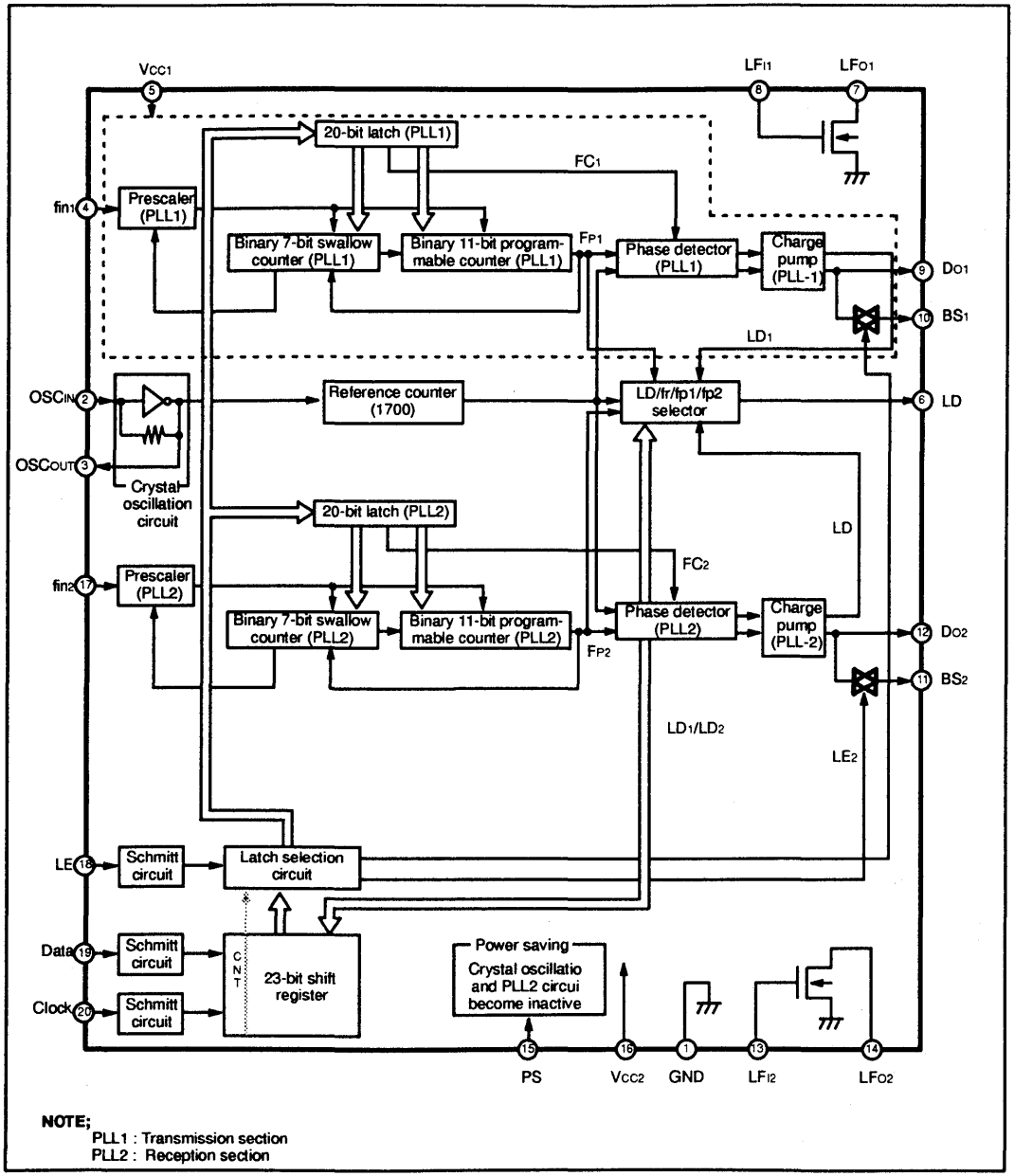
ABSOLUTE MAXIMUM RATINGS

Ratings		Symbol	Value	Unit
Supply Voltage		V_{CC}	–0.5 to +6.0	V
Output Voltage	OSC_{OUT}, Do, BS	V_{O1}	–0.5 to Vcc+0.5	V
	LD, LF_O	V_{O2}	–0.5 to +6.0	V
Output Current		I_O	±10	mA
Storage Temperature		T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



NOTE;
PLL1 : Transmission section
PLL2 : Reception section

BLOCK DESCRIPTIONS

TRANSMISSION/RECEPTION BLOCK

- 20-bit latch
- Programmable divider;
  Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
  The programmable dividers for transmission and reception are able to be controlled independently.
- Phase detectors with phase polarity change function
- 400MHz dual modulus prescalers (Divide ratio: 64/65)
- Charge pumps
- Transistors for LPFs
- Analog swithes

COMMON BLOCK

- 23-bit shift register
- Reference divider;
  Reference counter (Divide ratio: 1700)
  (Divide frequency = 12.5 kHz (Crystal oscillator frequency = 12.8 kHz))
- Crystal oscillation circuit
- Latch selector
- Shmitt circuits
- LD/fr/fp output selector

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Pin Descriptions
1	GND	–	Ground.
2 3	OSC_{IN} OSC_{OUT}	I O	Input and output of a reference divider and a crystal is externally connected between these pins.
4	fin_1	I	Input of a prescaler of PLL-1 (Transmission section). Connection with a VCO should be AC (capacitor) coupling.
5	V_{CC1}	–	Power supply for PLL-1 block. When power is cut off, PLL-1 block's latched data is cancelled.
6	LD	O	Output of lock detectors, a reference divider, and programmable dividers. Output data is selected by data setting of LD bits in the serial data. This is open-drain output.
7	LF_{O1}	O	Output of the transistor, used for transmission LPF.
8	LF_{I1}	I	Input of the transistor, used for transmission LPF.
9	D_{O1}	O	Output of the charge pump(PLL-1). Phase polarity is inverted by FC bit setting in the serial data.
10	BS_1	O	Output of the analog switch(PLL-1). Usually this pin is high-impedance state. When LE is set to high, the state of the internal charge pump is output.
11	BS_2	O	Output of the analog switch(PLL-2: reception section). Usually this pin is high-impedance state. When LE is set to high, the state of the internal charge pump is output.
12	D_{O2}	O	Output of the charge pump(PLL-2). Phase polarity is inverted by FC bit setting in the serial data.
13	LF_{I2}	I	Input of the transistor which is used for reception LPF.
14	LF_{O2}	O	Output of the transistor which is used for reception LPF.
15	PS	I	Power saving control for PLL-2 circuits.

PS	State
H	Active state
L	Power saving state (Crystal oscillation circuit and PLL2 circuits are inactive)

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Pin Descriptions
16	V_{CC2}	–	Power supply for PLL-2 circuits, a reference counter, a shift register, and a crystal oscillation circuit. When power is cut off, PLL-2 block's and reference counter's latched data are cancelled.
17	f_{in2}	I	Input of a prescaler of PLL-2. Connection with a VCO should be AC (capacitor) coupling.
18	LE	I	Load enable signal input. This pin involves a schmitt trigger circuit. When this pin is high (LE="H"), the data stored in a shift register is transferred into the latch according to the control bit in the serial data. And at the moment, internal analog switch is closed(ON), then each charge pump output signal is output through the BS pin.
19	Data	I	Serial data input. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either transmission or reception sections depending upon the control bit as follows. Control bit data: H → The destination of data: Latch of PLL-1 (transmission) Control bit data: L → The destination of data: Latch of PLL-2 (reception)
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. Each rising edge of the clock shifts one bit of data into the shift register.

FUNCTIONAL DESCRIPTIONS

Divide ratio can be set using the following equation:

$f_{VCO} = \{ (M \times N) + A \} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of an external voltage controlled oscillator (VCO)
M: Preset divide ratio of an internal dual modulus prescaler (64)
N: Preset divide ratio of binary 12-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 5-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of reference counter (1700)

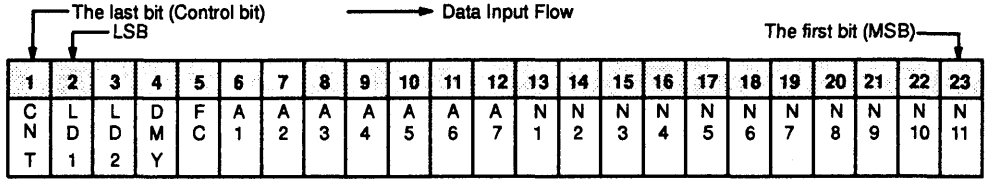
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins; Data, Clock, and LE pins. Programmable dividers of PLL-1 and PLL-2 are controlled individually.
Serial data of binary data is input to the Data pin.
On rising edge of the clock shifts one bit of the data into the shift register.
When the load enable (LE) is high, the data stored in the shift register is transferred to either the latch of the transmission or the reception sections, depending upon the control bit setting.

Control bit data	The destination of data
H	Latch of PLL-1 (transmission)
L	Latch of PLL-2 (reception)

SHIFT REGISTER COSTITUTION



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CNT	LD1	LD2	DMY	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
DMY : Dummy bit (set to "L" as a rule)
LD2 : Select bit of LD output (LD, fr, fp1, fp2)
LD1 : Select bit of LD output (LD, fr, fp1, fp2)
CNT : Control bit

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

11-bit programmable counter divide ratio (N1 to N11)

Divide ratio	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2047	1	1	1	1	1	1	1	1	1	1	1

NOTE: Divide ratio less than 16 is prohibited.

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

7-bit swallow counter divide ratio (A1 to A7)

Divide ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
127	1	1	1	1	1	1	1

LD1, LD2 : LD OUTPUT SELECT

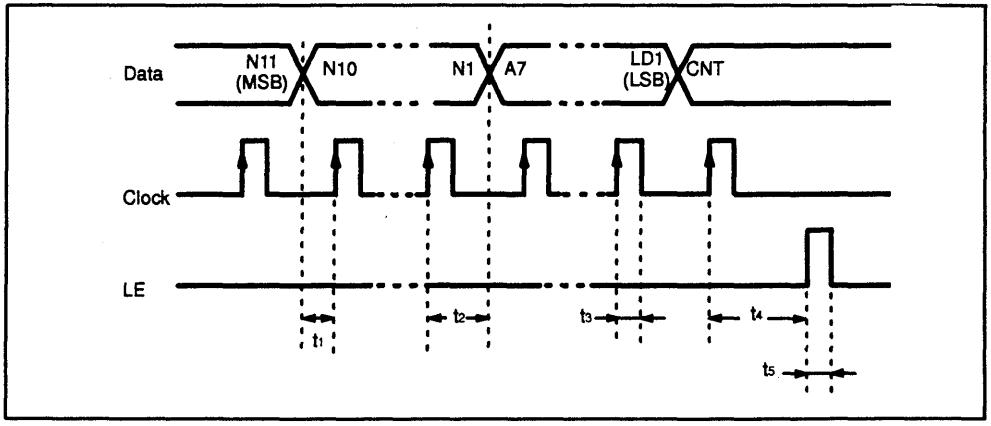
LD1	LD2	LD Output
1	1	Reference frequency (fr)
1	0	PLL-1 programmable frequency (fp1)
0	1	PLL-2 programmable frequency (fp2)
0	0	Lock detector output

DMY: DUMMY BIT

Set to "L" as a rule

SERIAL DATA INPUT TIMING

t_1 (≥ 1 µs) : Data setup time t_2 (≥ 1 µs) : Data hold time t_3 (≥ 1 µs) : Clock pulse width
t_4 (≥ 1 µs) : LE setup time to the rising edge of the last clock t_5 (≥ 1 µs) : LE pulse width



NOTE: On rising edge of the clock shifts one bit of the data into the shift register.
When LE is high, the data stored in the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

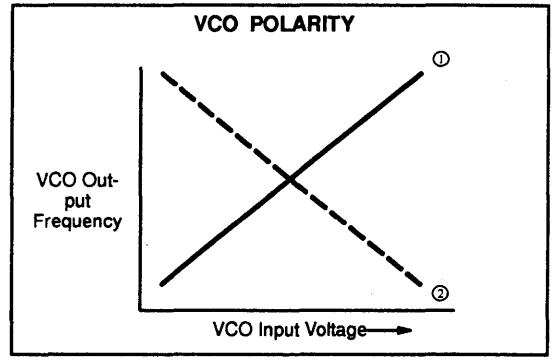
FC bit selects the phase of the phase detector. Phase characteristics (chage pump output) can be reversed depending upon the FC bit of the serial data. The phases of the charge pump outputs through LD pin are reversed depending upon the FC bit as well.

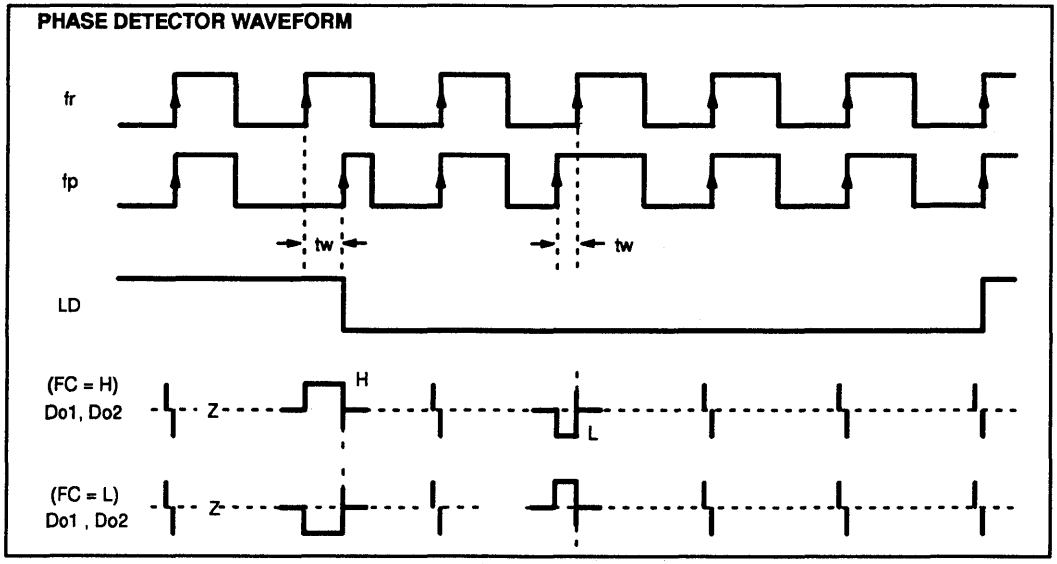
	FC = "H"	FC = "L"
	Do1, Do2, LD(fp1 & fp2) output	Do1, Do2, LD(fp1 & fp2) output
fr > fp	H	L
fr = fp	Z*	Z*
fr < fp	L	H

*Z: High-impedance

Depending upon the VCO polarity, FC pin should be set accordingly.

When VCO polarity is like① , the FC bit should be set at high.
When VCO polarity is like② , the FC bit should be set at low.





Note: Phase difference detection range : -2π to $+2\pi$
Spike shape depends on the charge pump characteristics. The spike is output to diminish the dead band.
LD output is "L" when the phase diference between the fr and fp is tw or more. When the phase difference is tw or less for three or more cycles, LD outputs "H". (When foscin is 21.25MHz, tw is 376ns to 753ns.)

STAND-BY MODE & LOCK DETECTOR (LD)

Setting the power saving control pin input level, the crystal oscillation circuit and PLL-2 circuits become inactive, then MB1514 enters lower current consumption state.

	PS pin	PLL-1	PLL-2	LD output
Transmit/Receive active mode	H	Lock	Lock	H
		Lock	Un-Lock	L
		Un-Lock	Lock	L
Receive active mode		Stand-by V_{CC1} = OFF	Lock	H
			Un-Lock	L
Stand-by mode	L*	Stand-by V_{CC1} = OFF	Stand-by	L

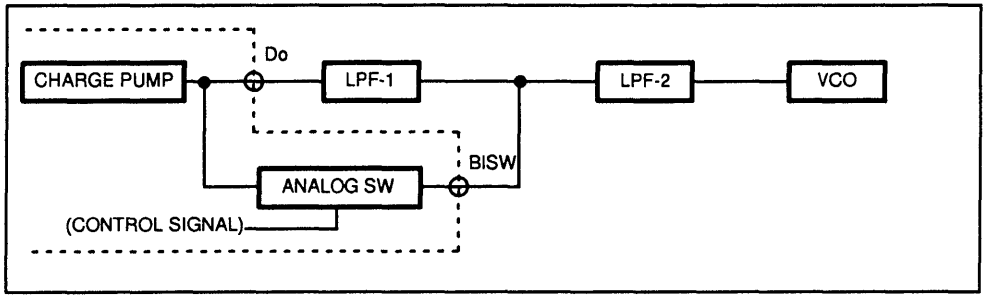
NOTE:When PS is "L", the charge pump (Do2) of the PLL-2 becomes high-impedance state.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, BS1, BS2 pins output the charge pump output (Do1, Do2). When the analog switch is OFF, BS pins are set to high-impedance state.

	Control data = H When the divide ratio of the PLL-1 is set.		Control data = L When the divide ratio of the PLL-2 is set.	
	LE = H	LE = L	LE = H	LE = L
Analog Switch of transmit section	ON	OFF	OFF	OFF
Analog Switch of receive section	OFF	OFF	ON	OFF

When an analog switch is inserted between LPF-1 and LPF-2, fast lock up is achieved by reducing LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc*	2.2	3.0	4.2	V
Input Voltage	V_{IN}	GND	–	Vcc	V
Ambient Temperature	Ta	–10		+70	°C

*: $V_{CC1} = V_{CC2}$

ELECTRICAL CHARACTERISTICS

($V_{CC1} = V_{CC2}$ = 2.2V to 4.2V, Ta = –10°C to + 70°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC1}	PLL-2 Current	–	4.0	–	mA
		I_{CC2}	PLL-1 + PLL-2 Current	–	8.0	–	mA
Operating Frequency	fin	f_{in1}		10	–	400	MHz
	OSC_{IN}	fosc		–	21.25	–	
Input Sensitivity	fin	Pfin	50Ω system	–10	–	0	dBm
	OSC_{IN}	Vosc		0.5	–	–	Vp-p
High–level Input Voltage	Except fin and OSC_{IN}	V_{IH}		Vccx0.7+0. 4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	Vccx0.3–0.4	
High–level Input Current	Data, Clock, LE, PS	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	Iosc			±50		
	LFi	I_{LF}				1.1	
High–level Output Voltage	Except Do, OSC_{OUT}	Vosc	Vcc = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OH}		–	–	0.4	
High–impedance Cutoff Current	Do, LF_O	I_{OFF}		–	–	1.1	µA
	LD			–	–	10.0	
Output Current	Except Do, OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	

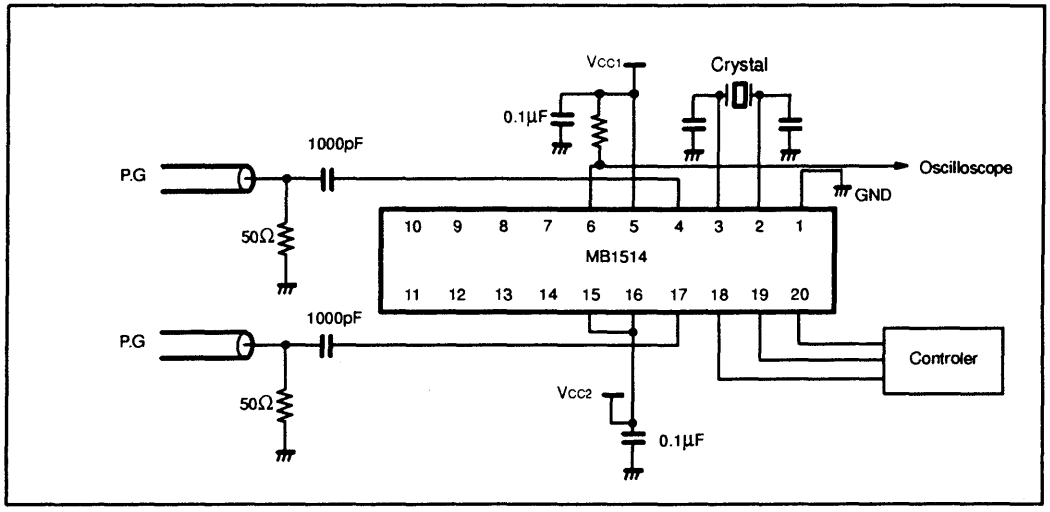
ELECTRICAL CHARACTERISTICS

(V_{CC1} = V_{CC2} = 2.2V to 4.2V, Ta = −10°C to + 70°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Output Current	D_{O1}	I_{OH}	V_{CC} = 3.0V	-	−0.5	-	mA
		I_{OL}	V_{CC} = 3.0V	-	12	-	mA
	D_{O2}	I_{OH}	V_{CC} = 3.0V	-	−1.5	-	mA
		I_{OL}	V_{CC} = 3.0V	-	6	-	mA
Analog Switch ON Resistance		R_{on}		-	50	-	Ω

4

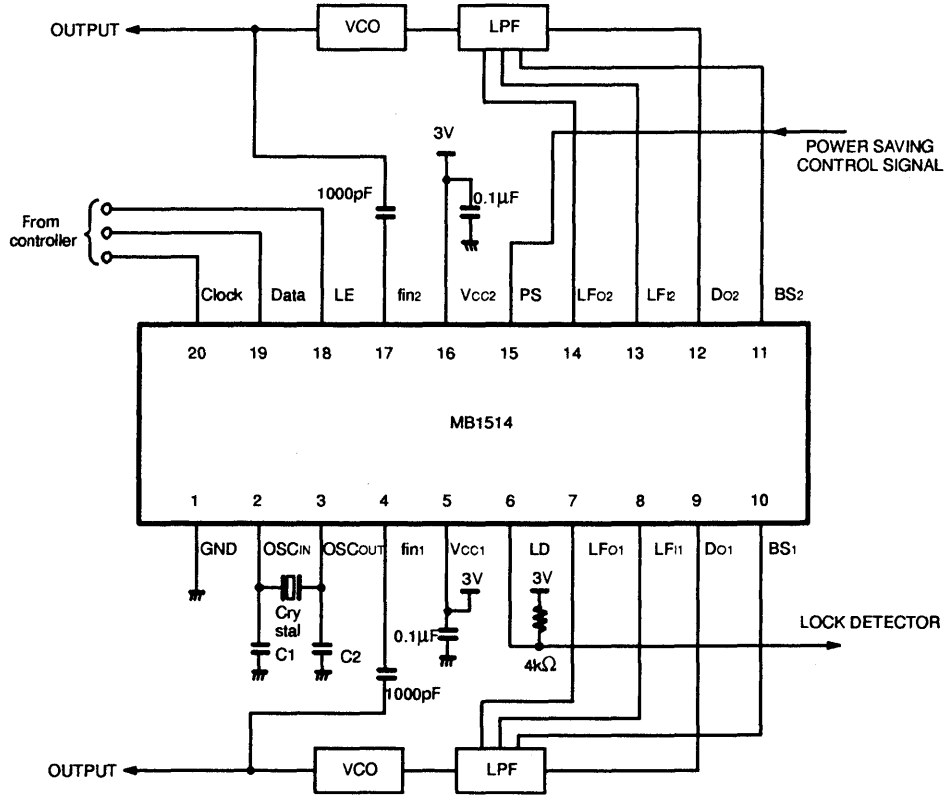
TEST CIRCUIT (FOR PRESCALER INPUT SENSITIVITY)



HANDLING PRECAUTION

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC bords with devices.

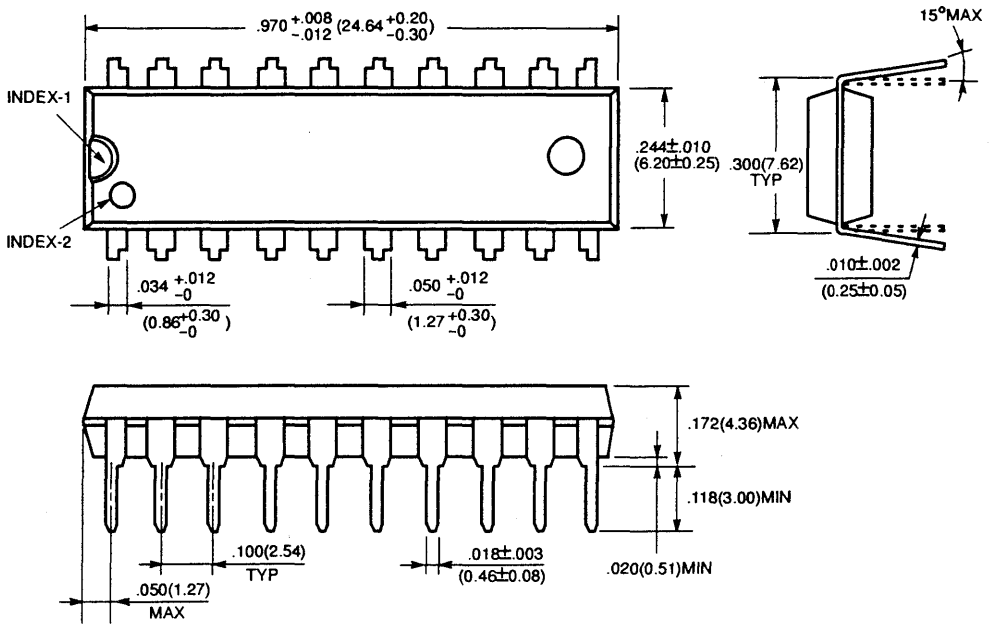
APPLICATION EXAMPLE



NOTE;
C1, C2 : depends on the crystal oscillator.
Clock, Data, LE : Using shmitt trigger circuits (When inputs are left open, pull-down or pull-up resistors are necessary to prevent oscillation.)
Crystal : 21.25MHz
LD : Open drain

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)

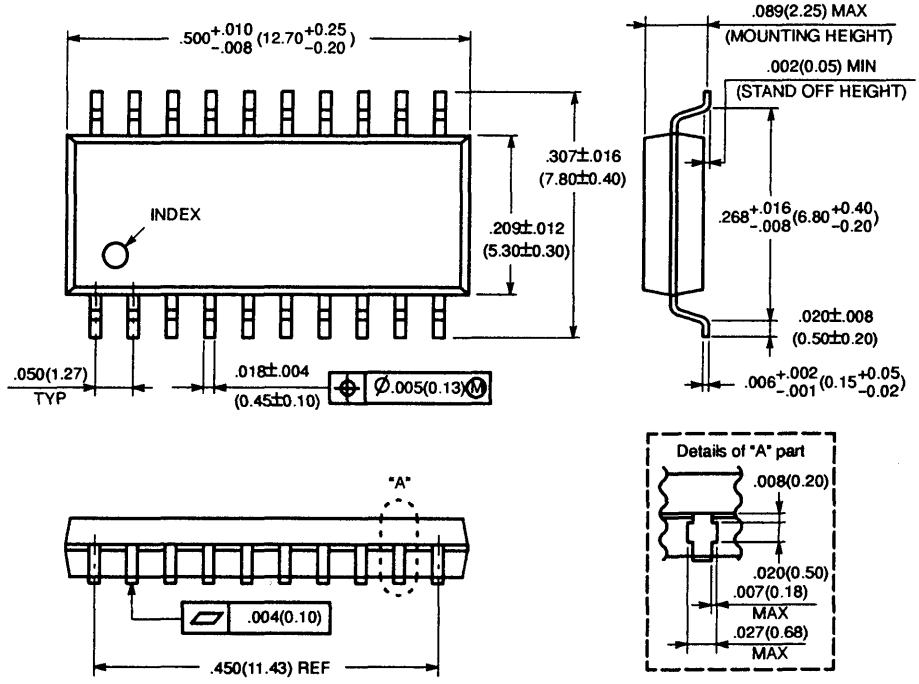


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



Sept. 1995
Edition 2.0a

FUJITSU

DATA SHEET

MB1515 ASSP

BiCMOS 2.5GHz PLL FREQUENCY SYNTHESIZER WITH BUILT-IN PRESCALER

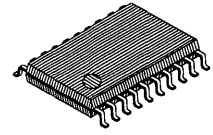
4

DESCRIPTION

The MB1515 is a serial input PLL (Phase-Locked Loop) frequency synthesizer with a built-in prescaler allowing for a pulse swallow system in the two modulus 2.5 GHz band. It is suitable for BS and TV tuners and CATV systems.

The synthesizer is powered by 5 V (typical). Using the latest proprietary process, current consumption has been reduced to Icc = 16 mA (typical).

20–pin Plastic SSOP



(FPT-20P-M03)

FEATURES

- Supply voltage: Vcc = 5 V
- High-speed operation capability: fin = 2.5 GHz (Pin = - 4 dBm)
- Low current consumption: Icc = 16 mA (typical)
- Broad operating temperature range: Ta = - 40°C to +85°C
- Integrated Functions
  24-bit shift register
  24-bit latch
  Reference divider
  Binary 2-bit programmable reference counter (Divide ratios: 256, 512, 1024, and 2048)
  Comparison Divider
  Binary 5-bit swallow counter (Divide ratios: 0 to 31)
  Binary 12-bit bit programmable counter (Divide ratios: 32 to 4095)
  Phase comparator with phase conversion feature
  Two modulus prescaler for 2.5 GHz band (Divide ratios: 256/272 and 512/528)
  4-bit band switching signals
  Control signal generator
  Crystal oscillator
  Charge pump

MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Supply voltage	V_{CC}	–0.5 to +7.0	V
Output voltage	V_O	–0.5 to V cc+0.5	V
Output current	I_O	± 10	mA
Storage temperature	Tstg	–55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

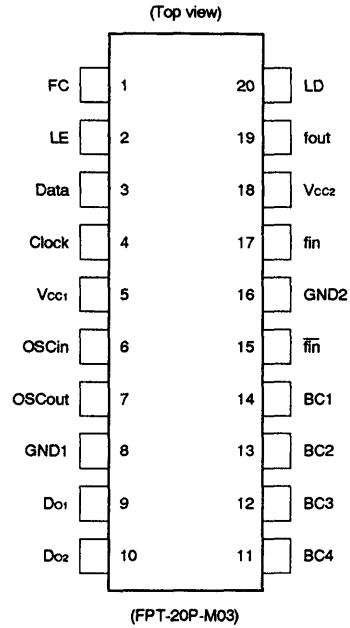
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_I	GND	—	V_{CC}	V
Operating temperature	Ta	–40	—	+85	°C

NOTES:

1. To prevent damage caused by static electricity, an antistatic element is added and antistatic enhancement is also built into the circuit. However, the following handling cautions must be observed:
   - Contain the device in a conductive case when storing or transporting it.
   - Before handling, verify that the person handling the device, fixtures, and tools are not charged (grounded). Use a grounded conductive sheet as the work surface.
   - Turn off power before connecting or disconnecting the device to or from the socket.
   - Protect the lead with a conductive sheet when handling (such as transporting) a board on which this device is mounted.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT

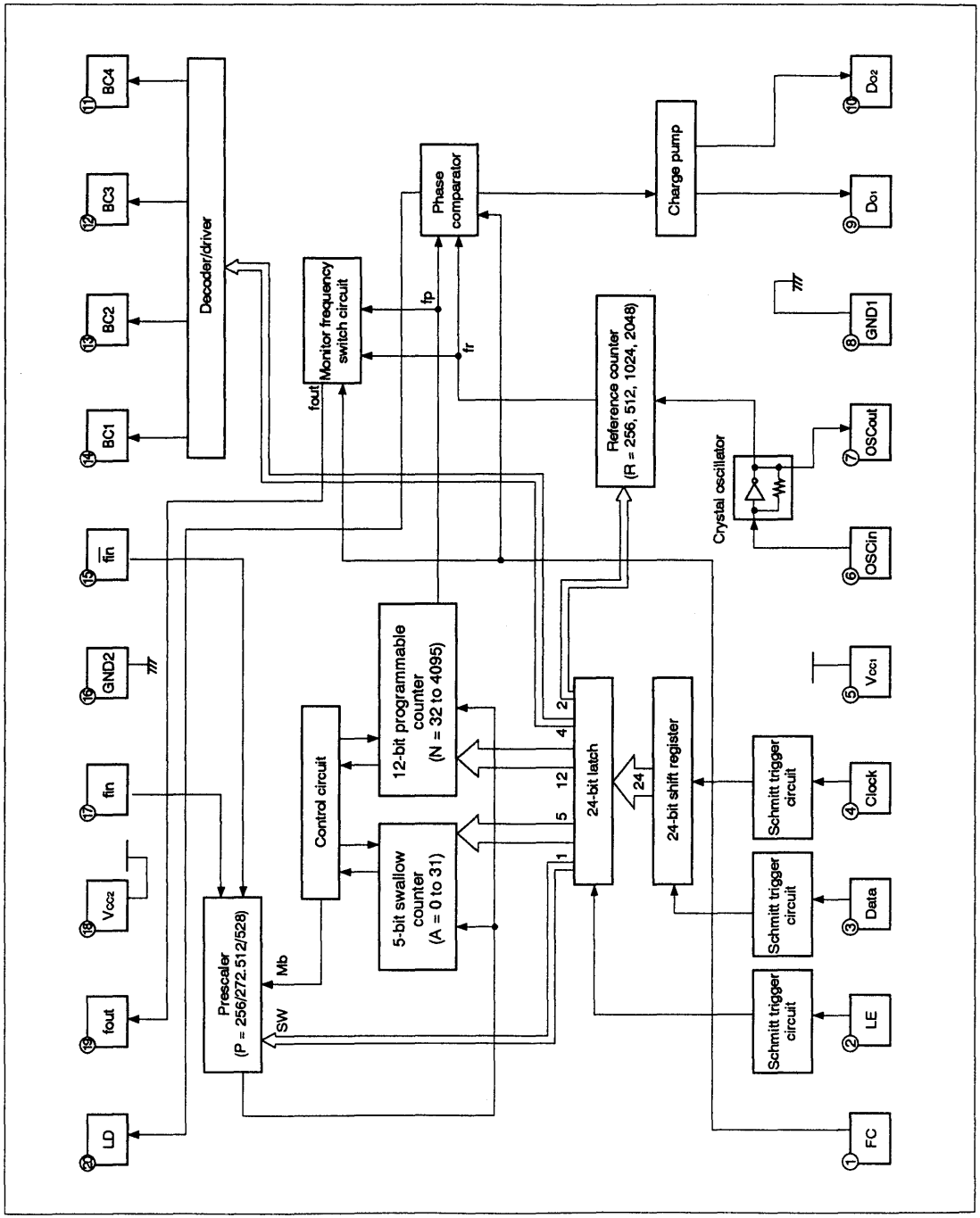


PIN DESCRIPTION

Pin No.	Pin name	I/O	Descriprion		
1	FC	I	Phase switch input pin to the phase comparator (with pull up resistor). This pin allows for inverting the polarity of phase comparator output, according to the polarity of the externally connected LPF and VCO. When FC is at "L" level, charge pump and phase comparator characteristics are reversed. This pin also toggles the output of the fout pin (test pin) between fr and fp.		
2	LE	I	Load enable signal input pin (with Schmitt trigger circuit). The pin sends shift register contents to the latch when LE is at "H" (or open).		
3	Data	I	Serial data input pin using binary codes (with Schmitt trigger circuit).		
4	Clock	I	24-bit shift register clock input pin (with Schmitt trigger circuit). Data is read at the rising edge of the clock pulse.		
5	V_{CC1}	—	Power supply pin (for PLL).		
6	OSCin	I	Cystal oscillator connect pin and reference divider input pin. (OSCin: Oscillator input pin, OSCout: Oscillator output pin)		
7	OSCout	O			
8	GND1	—	Grounding pin (for PLL)		
9	DO1	O	Charge pump output pin. Phase characteristics invert with FC pin settings.		
10	DO2	O			
11	BC4	O	Band switch output pin (open collector output). Output is controlled by the serial data band bit setting. When BCX bit is "H", the BCX output transistor turns ON. When BCX bit is "H", the BCX output transistor turns OFF. (X: 1 to 4)		
12	BC3	O			
13	BC2	O			
14	BC1	O			
15	fin	I	fin's complementary input pin. Connect to ground via a capacitor.		
16	GND2	—	Ground pin (for prescaler).		
17	$\overline{fin}$	I	Prescaler input pin. Input using ac coupling.		
18	V_{CC2}	—	Power supply pin (for prescaler).		
19	fout	O	Phase comparator input monitor pin.Produces either the reference divider output (fr)or the comparison divider output (fp) signal depending on the FC pin's input level.	FC	Output Signal
				"H"	fr
				"L"	fp
20	LD	O	Phase comparator output pin. LD is usually "H", and is set to "L" for the duration equivalent to the phase error between fr and fp.		

4

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Units
				Min.	Typ.	Max.	
Power supply current		I_{CC}	When input at fin=2.5GHz and OSCin= 4MHz, V_{CC}=5V. Other input pins are GND and output pins are open.	—	16.0	—	mA
Operating frequency	fin	fin	Must be AC-coupled. The minimum operating frequency when coupled at 1000 pF.	100	—	2500	MHz
	OSCin	f_{OSC}	—	—	4	10	MHz
Permissible input voltage	fin	Pfin1	2300 to 2500 MHz	–4	—	6	dBm
		Pfin2	1900 to 2300 MHz	–7	—	6	dBm
		Pfin3	1000 to 1900 MHz	–10	—	6	dBm
		Pfin4	100 to 1000 MHz	–20	—	6	dBm
	OSCin	V_{OSC}	—	0.5	—	—	V_{P-P}
High level input voltage	Other the fin and OSCin	V_{IH}		$V_{CC} \times 0.7 + 0.4$			V
Low level input voltage		V_{IL}	—	—	—	$V_{CC} \times 0.3 - 0.4$	V
High level input current	Data, Clock, LE	I_{IH}	—	—	1.0	—	µA
		I_{IL}	—	—	–1.0	—	µA
Low level input current	FC	I_{ILFC}	—	—	–60	—	µA
Input current	OSCin	I_{IOSC}	—	—	±50	—	µA
High level output voltage	Excluding Do and BC	V_{OH}	When V_{CC} = 5 V	4.4	—	—	V
Low level output voltage		V_{OL}	—	—	—	0.4	V
High impedance cutoff current	Do 1, 2 BC 1 to 4	I_{OFF}	—	—	—	1.1	µA
Output current	Excluding Do and BC	I_{OH}	—	–1.0	—	—	mA
		I_{OL}	—	1.0	—	—	mA
Output voltage breakdown	BC1 to 4	V_B	—	—	—	12	V

FUNCTIONAL DESCRIPTIONS

1. Formula for calculation of divide ratio

Set divider's divide ratio according to the following formula:

$$fvco = [(P \times N) + (16 \times A)] \times fosc \div R$$

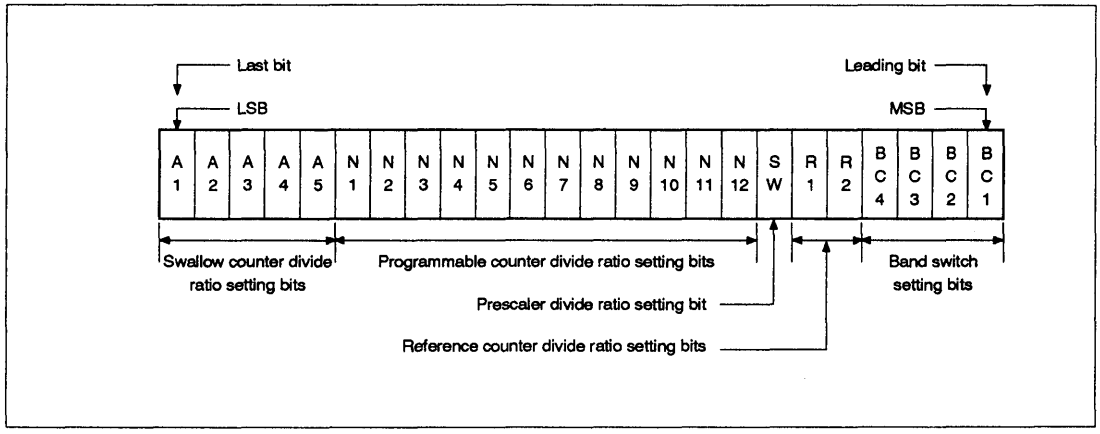
where

- fvco : Externally connected VCO output frequency
- P : Prescaler divide ratio (256 or 512)
- N : Binary 12-bit programmable counter setting (32 to 4095)
- A : Binary 5-bit swallow counter setting (0 to 31)
- fosc : Reference oscillation frequency
- R : Reference counter setting (256, 512, 1024, 2048)

2. Serial data input procedure

Serial data is input from three inputs, Data pin, Clock pin and LE pin, allowing for control of the 4-bit band switch setting, the 3-bit reference divider and the 17-bit comparison divider respectively. The data is sequentially fetched into the internal shift register at the rising edge of the clock and transferred to the latch when load enable is at the "H" level.

The 24-bit shift register is configured as follows:



- **Band switch setting (BC1 to BC4)**
  When data set in the band bits is at "H," output is turned ON. When data is at "L," output is turned OFF.
- **Prescaler divide ratio (SW)**
  Divided by 256/272 when data set in the SW bit is at "H." Divided by 512/528 when data is at "L."

- **Divide ratios for 5-bit swallow counter (A1 to A5)**

Divide ratio A	A5	A4	A3	A2	A1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
• •	• •	• •	• •	• •	• •
31	1	1	1	1	1

- **Reference counter divide ratios (R1 and R2)**

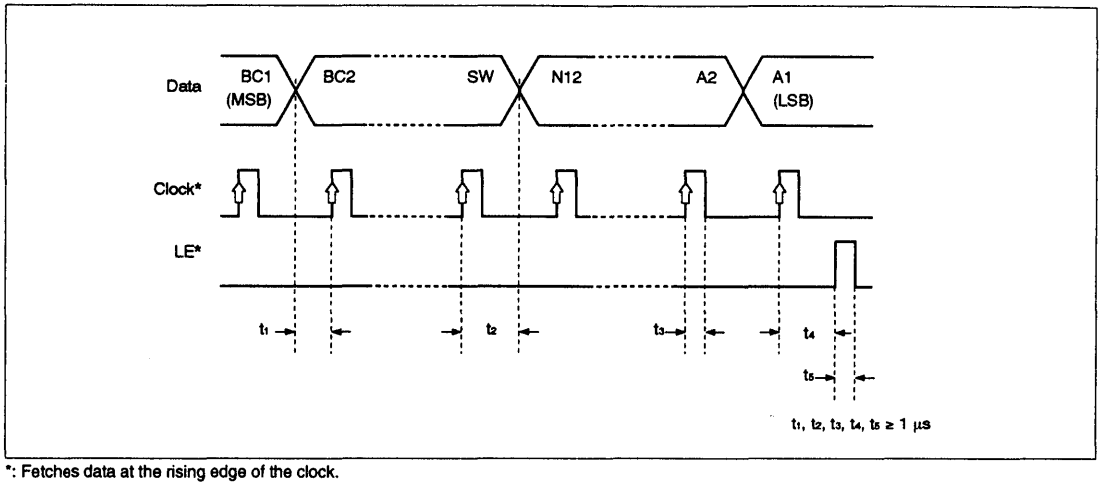
Divide ratio R	R2	R1
256	0	0
512	0	1
1024	1	0
2048	1	1

- **Divide ratios for 12-bit programmable counter (N1 to N12)**

Divide ratios	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0	0	1
2	0	0	0	0	0	0	1	0	0	0	1	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
4095	1	1	1	1	1	1	1	1	1	1	1	1

3. Serial data input timings

When designing the synthesizer, control the FC pin according to the VCO polarity.



*: Fetches data at the rising edge of the clock.
*: Fetches data when LE is at "H" level.

4. FC pin input in relation to phase characteristics

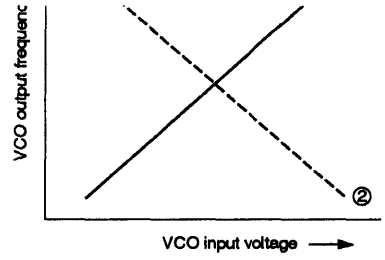
The FC pin switches the phase of the phase comparator. Phase characteristics (charge pump output) are inverted by controlling this pin. Output from the phase comparator input monitor pin (fout) is also controlled by this FC pin. The relation of FC pin input with Do and fout is as follows:

	FC: "H" (or open)		FC: "L"	
	DO1, DO2	fout	DO1, DO2	fout
fr>fp	H	Outputs reference divider output (fr)	L	Outputs comparison divider output (fp)
fr=fp	Z		Z	
fr<fp	L		L	

Z: high impedance

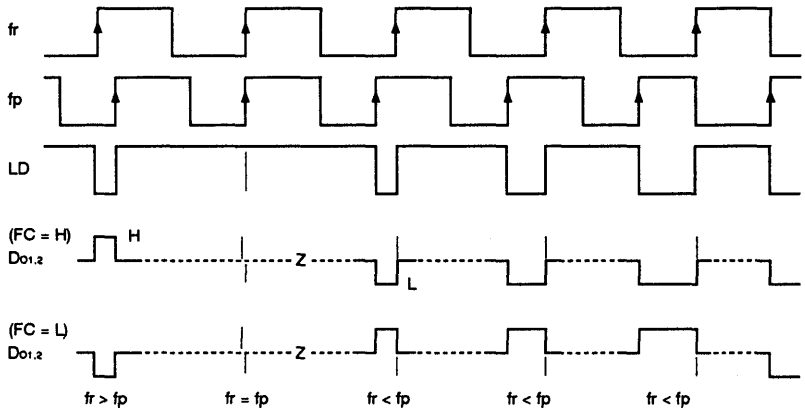
When designing the synthesizer, control the FC pin according to the VCO polarity.

- When the VCO polarity is ① in the figure, the FC pin is either at "H" or open.
- When the VCO polarity is ② in the figure, the FC pin is at "L".



4

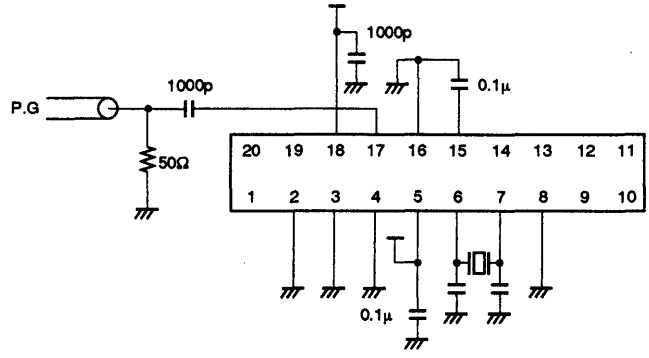
PHASE COMPARATOR OUTPUT WAVEFORMS



Notes:

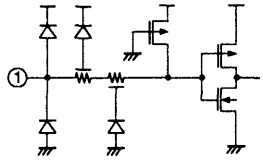
1. The phase error is detected in a range of - 2 π to +2 π.
2. Output of a "glitch" varies slightly with charge pump characteristics. This "glitch" is output to eliminate an dead band.

EXAMPLE MEASUREMENT CIRCUIT (PRESCALER INPUT SENSITIVITY)

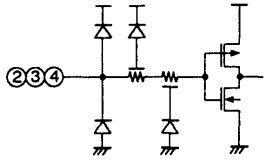


EQUIVALENT CIRCUIT DIAGRAM

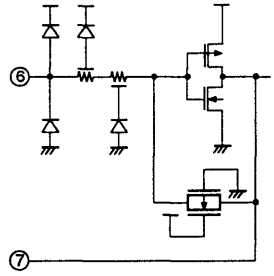
• FC



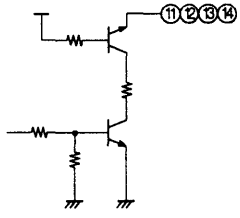
• LE, Data, clock



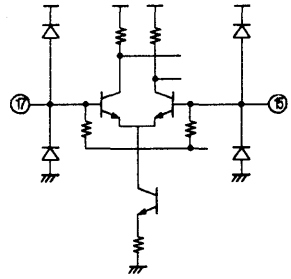
• OSCin, OSCout



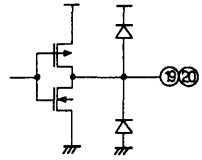
• BC1, BC2, BC3, BC4



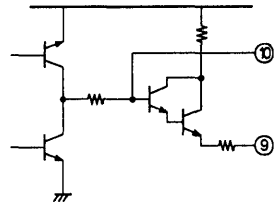
• $\overline{fin}$, fin



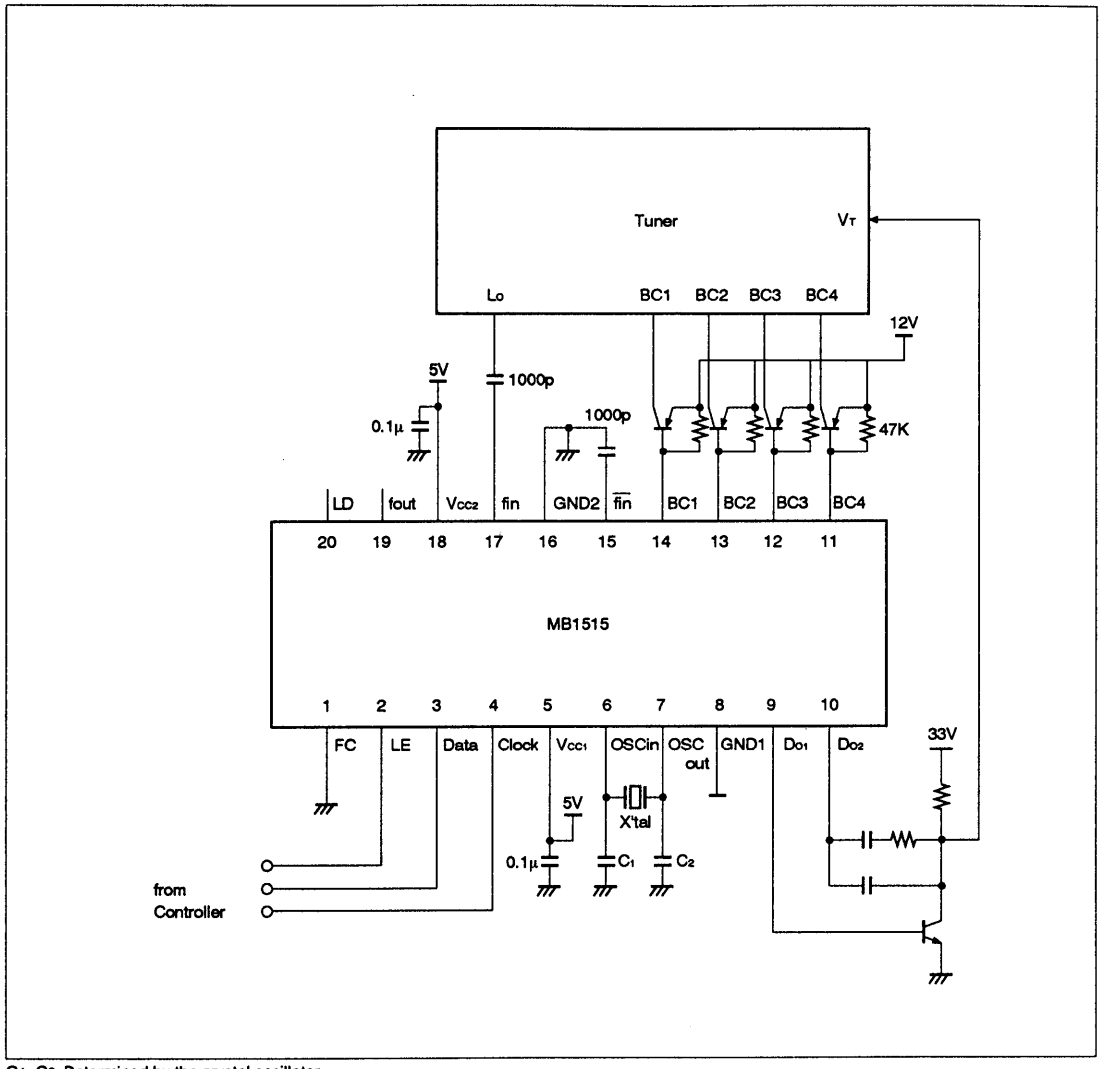
• LE, Data, clock



• LE, Data, clock



EXAMPLE APPLICATION



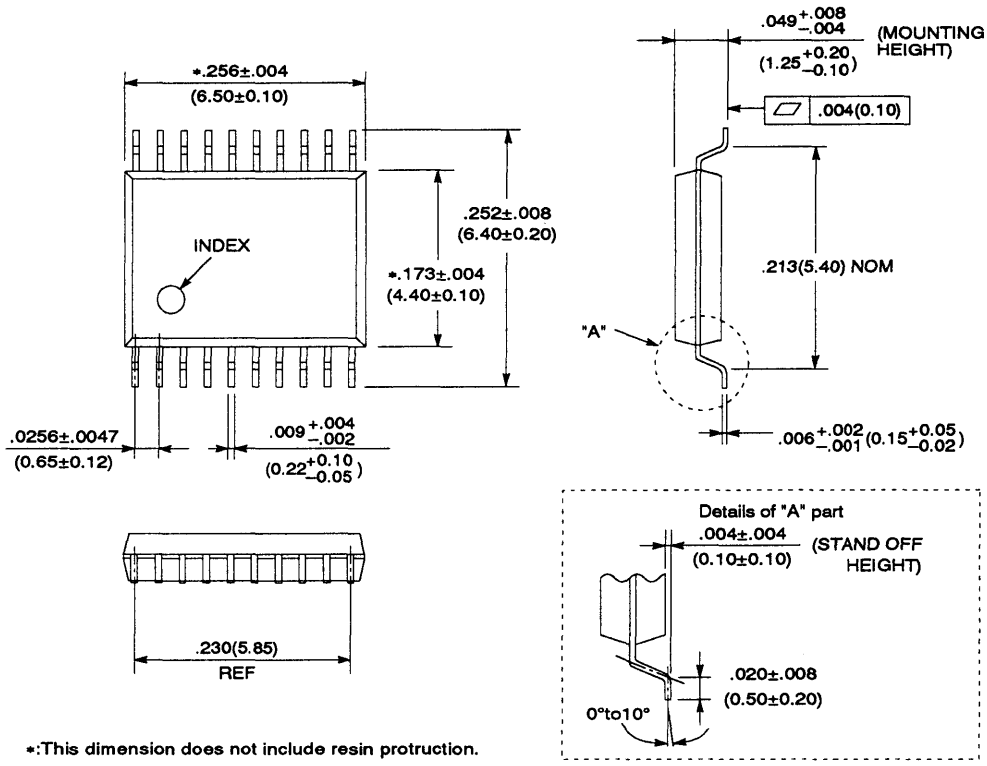
C1, C2: Determined by the crystal oscillator
FC: with pull up resistor

ORDERING INFORMATION

Parts Number	Package	Notes
MB1515PFV	Plastic SSOP, 20 pins (FPT–20P–M03)	

EXTERNAL DIMENSIONS

20-pin plastic SSOP
(FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

June 1995
Edition 0.1

FUJITSU

MB15A16

1.2GHz HIGH-SPEED TUNING PLL FREQUENCY SYNTHESIZER

The Fujitsu MB15A16 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function, and is very suitable for the digital radio applications such as GSM. MB15A16 achieves the low noise performance as well as the high-speed lock-up which is required for digital cellular phones.

The MB15A16 can operate from a single +3 V supply and has an Icc of 7.0 mA (typical).

PRELIMINARY

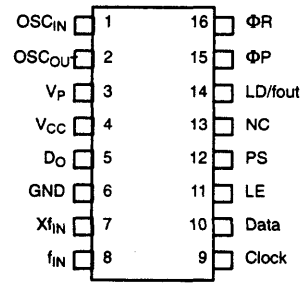
4

FEATURES

- High operating frequency : f_{IN} = 1.2 GHz (P_{IN} = -10 dBm)
- Pulse-swallow function : High-speed dual-modules prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 7.0 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 µA typ. (Controlled with PS pin)
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter: 5 to 2,047
- Serial input 17-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit for setting a prescaler divide ratio (SW bit)
  1-bit for switching a phase polarity (FC bit)
  1-bit for selecting LD/fout (LDS bit)
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16-pin SSOP (shrink small outline) package (Suffix : –PFV)

PIN ASSIGNMENT

(TOP VIEW)



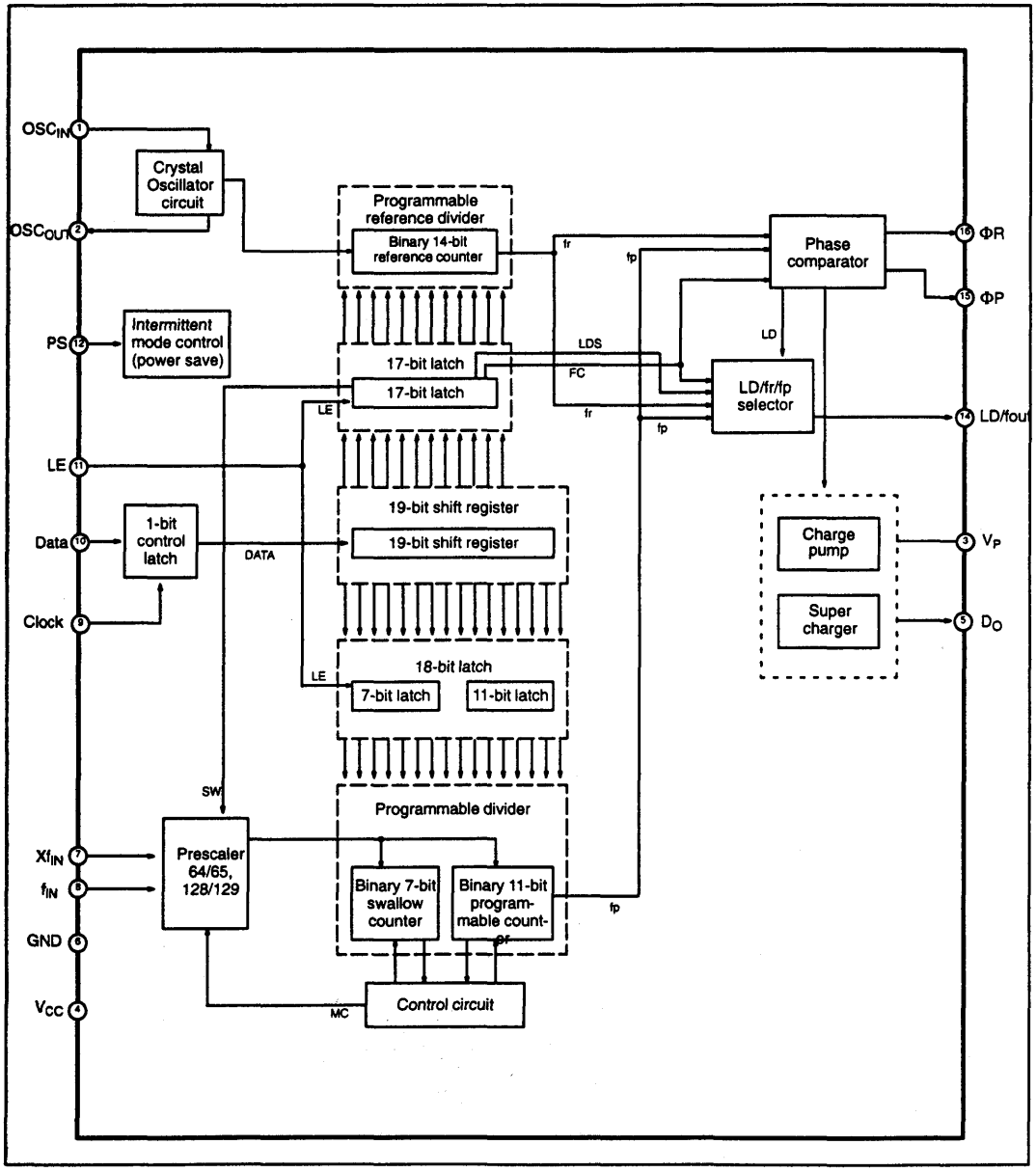
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Ratings	Symbol	Value	Unit	Remark
Supply voltage	V_{CC}	–0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	–0.5 to 6.0	V	ΦP
Output current	I_O	±10	mA	
Storage temperature	Tstg	–55 to +125	°C	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for external a crystal or a TCXO.
2	OSC_{OUT}	O	Oscillator output. Connection for an external crystal.
3	V_P	–	Power supply input for the charge pump.
4	V_{CC}	–	Power supply input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed according FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.) Control bit = "H" ; Data is transmitted to the 17-bit latch. Control bit = "L" ; Data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input (Open is prohibited.) When LE is high, the data of the shift register are transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving control input. This pin must be set at "L" at Power–ON. (Open is prohibited.) PS = "H" ; Normal mode PS = "L" ; Power saving mode
13	NC	–	No connection.
14	LD/f_{OUT}	O	Lock detector output(LD)/Monitor pin of the phase comparator(fout). A LDS bit in a serial data switchs LD/fout pin's output. LDS = "H" ; outputs fout LDS = "L" ; outputs LD
15	ΦP	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦR pin is a C-MOS output.

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} + R \quad (A < N)$

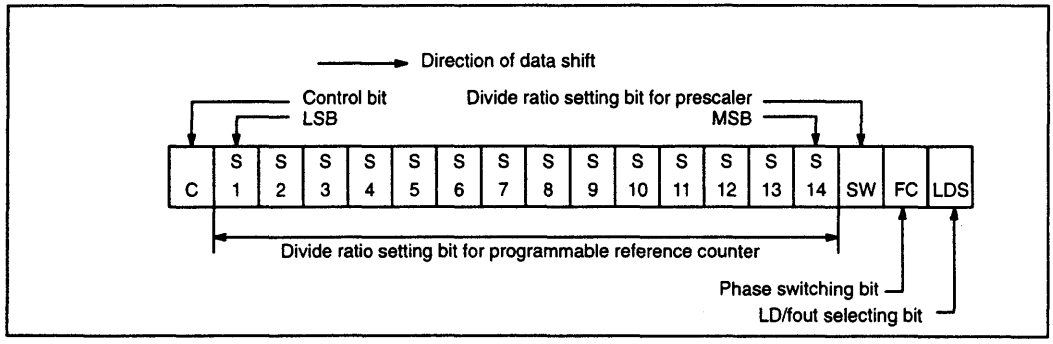
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial data input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 16-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	17 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 17-bit latch and a 14-reference counter. The serial 18-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

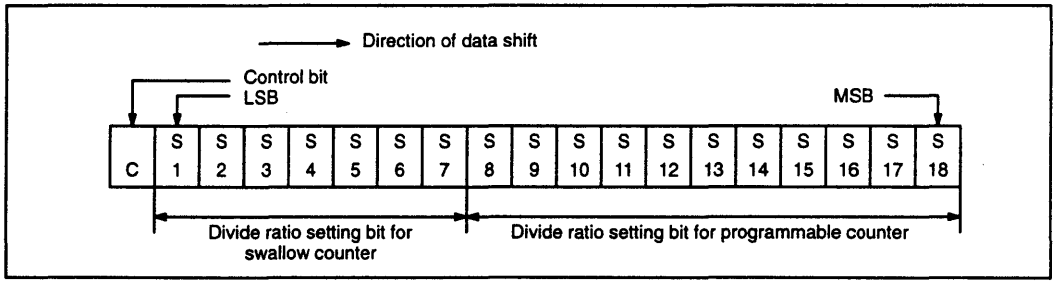
Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
   Low: 128 or 129
   High: 64 or 65
3. LDS: This bit selects LD/fout pin output
   High: outputs phase comparator monitoring signal(fout).
   Low: outputs lock detect signal(LD)
4. FC: This bit selects phase characteristics.
5. S1 to S14: These bits select the divide ratio of the programmable reference counter (6 to 16,383).
6. C: Control bit: Set high.
7. Start data input with MSB first .

(b) Programmable divider divide ratio

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

- 11-bit programmable counter divide ratio

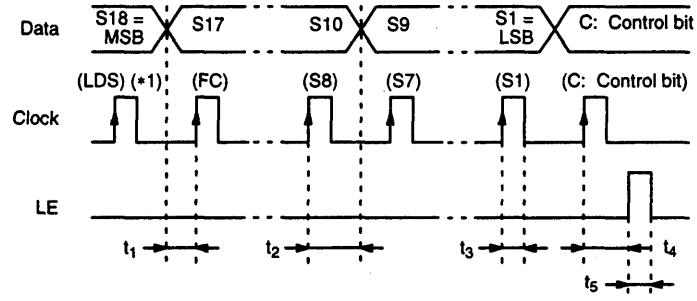
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for 11–bit programmable counter.
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18: These bits select the divide ratio of programmable counter (5 to 2,047).
4. C: Control bit: (Set low)
5. Start data input with MSB first.

Serial data input timing

- t_1 (≥ 100ns) : Data setup time t_2 (≥ 1000ns) : Data hold time t_3 (≥ 300ns) : Clock pulse width
  t_4 (≥ 100ns) : LE setup time to the rising edge of last clock t_5 (≥ 790ns) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Power saving mode (Intermittent operation control circuit)

Setting PS pin to Low, MB15A16 enters into power saving mode resultatly current sonsumption can be limited to 100µA (typ.).
Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop. To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
PS pin must be set "L" at Power–ON.

Relation between the FC input and phase characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ΦR, ΦP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ΦR, and ΦP is shown below:

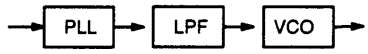
	FC = High				FC = Low			
	Do	ΦR	ΦP	fout	Do	ΦR	ΦP	fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z(*1)	(fp)
$f_r < f_p$	L	H	Z(*1)	(fr)	H	L	L	(fp)
$f_r = f_p$	Z(*1)	L	Z (*1)	(fr)	Z(*1)	L	Z(*1)	(fp)

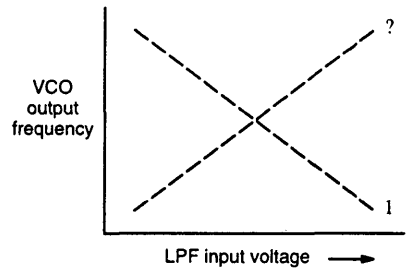
*1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

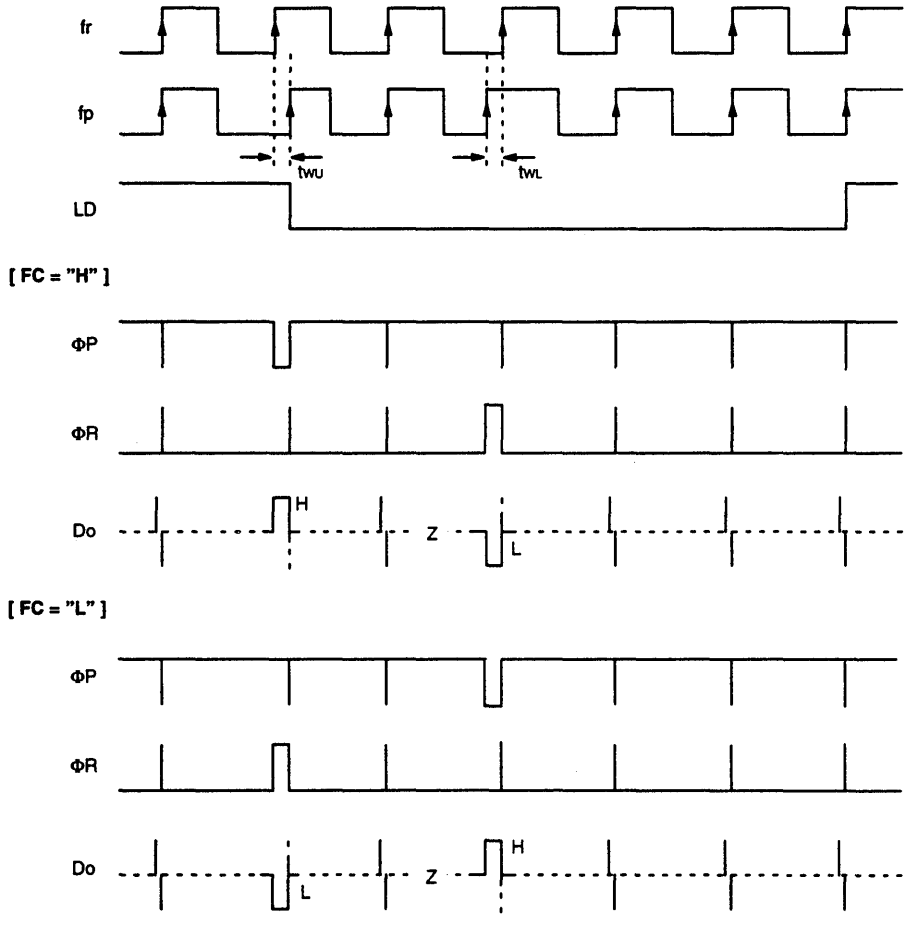
*: When the LPF and VCO characteristics are similar to ?, set FC bit high.

*: When the VCO characteristics are similar to 1, set FC low.





Phase comparator output waveforms



Notes: 1. Phase difference detection range: -2π to $+2\pi$

2. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
3. twu and twL depend on OSCin input frequency.

   twu ≤ 8/fosc (e. g. twu ≤ 625ns, foscin = 12.8 MHz)

   twL ≥ 16/fosc (e. g. twL ≥ 1250ns, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	Vp	Vcc	–	5.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	T_A	–40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

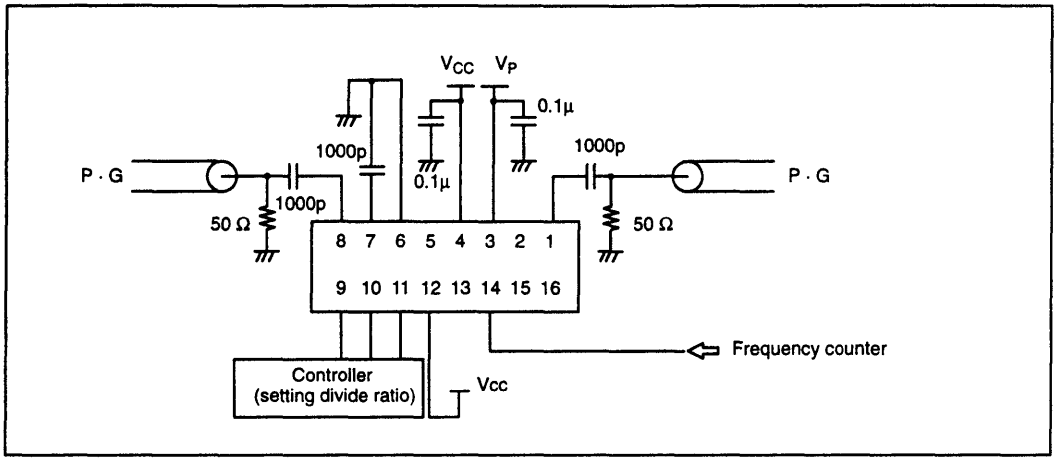
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

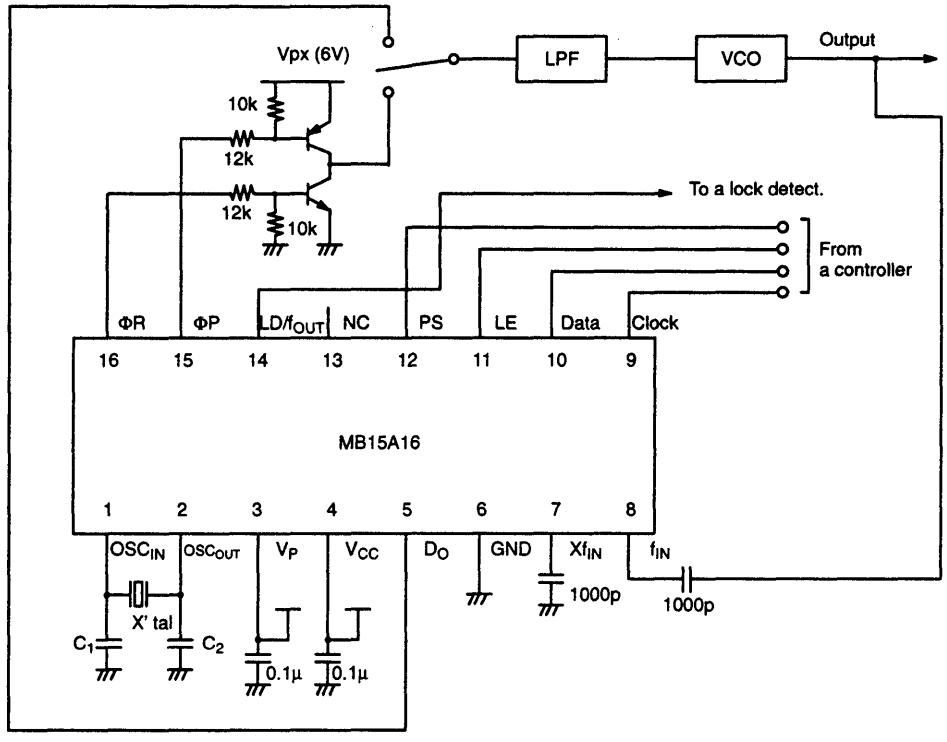
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current (Power saving current)		I_{CC} (I_{PS})	–	7 (0.1)	–	mA	With f_{IN} = 1.2 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Operating frequency	f_{IN}	f_{IN}	300	–	1200	MHz	AC coupling with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	$V_{f\,IN}$	–10	–	6	dBm	50Ω (refer to the test circuit.)
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Data, Clock, LE, PS	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock, LE, PS	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{IN}	I_{OSC}	–100	–	100	µA	
High-level output voltage	ΦR, LD	V_{OH}	2.1	–	–	V	Vcc = 3 V, I_{OH} = –1.0mA
Low-level output voltage	ΦR, ΦP, LD	V_{OL}	–	–	0.4	V	Vcc = 3V, I_{OL} = 1.0mA
High-impedance Cut off current	D_O,, ΦP	I_{OFF}	–	–	0.3	µA	V_P = Vcc to 3.6V V_{OOP} = GND to 6V
Output current V_{DOH} = 4.0V V_{DOL}=1.0V	ΦR, LD	I_{OH}	–1.0	–	–	mA	Vcc = 3V
	ΦR, ΦP, LD	I_{OL}	–	–	1.0	mA	Vcc = 3V
	Do	I_{DOH}	–15	–	–5	mA	Vcc=3V, Vp=5.0V,
		I_{DOL}	6	–	10	mA	Vcc = 3V, Vp = 5.0V,

TEST CIRCUIT
(FOR MEASURING INPUT SENSITIVITY fin/OSCin)



APPLICATION EXAMPLE



V_{PX} : Maximum 6 V
C_1, C_2 : Depend on the crystal parameters
ΦP : N-ch open drain output
ΦR : C-MOS output

DS04–21323–2aE

FUJITSU

DATA SHEET

MB1516A *ASSP*

1.1GHz High-Speed Tuning PLL Frequency Synthesizer

4

DESCRIPTION

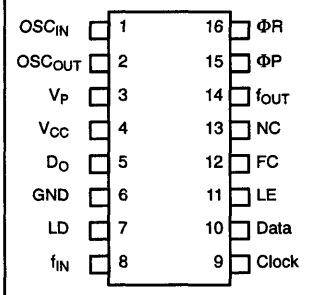
The Fujitsu MB1516A is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. MB1516A achieves the low noise performance as well as the high–speed lock-up which is required for digital mobile communications.
The MB1516A can operate from a single +3 V supply. Fujitsu's advanced technology achieves an Icc of 6.5 mA (typical).

FUNCTION

- High operating frequency : f_{IN} = 1.1 GHz (P_{IN} = –10 dBm)
- Pulse-swallow function : High-speed dual-modulus prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 6.5 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 µA typ.
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter : 5 to 2,047
- Serial input 16-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit switch counter sets prescaler divide ratio
  1-bit power saving function control
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16–pin SSOP (shrink small outline) package (Suffix : –PFV)

PIN ASSIGNMENT

(TOP VIEW)

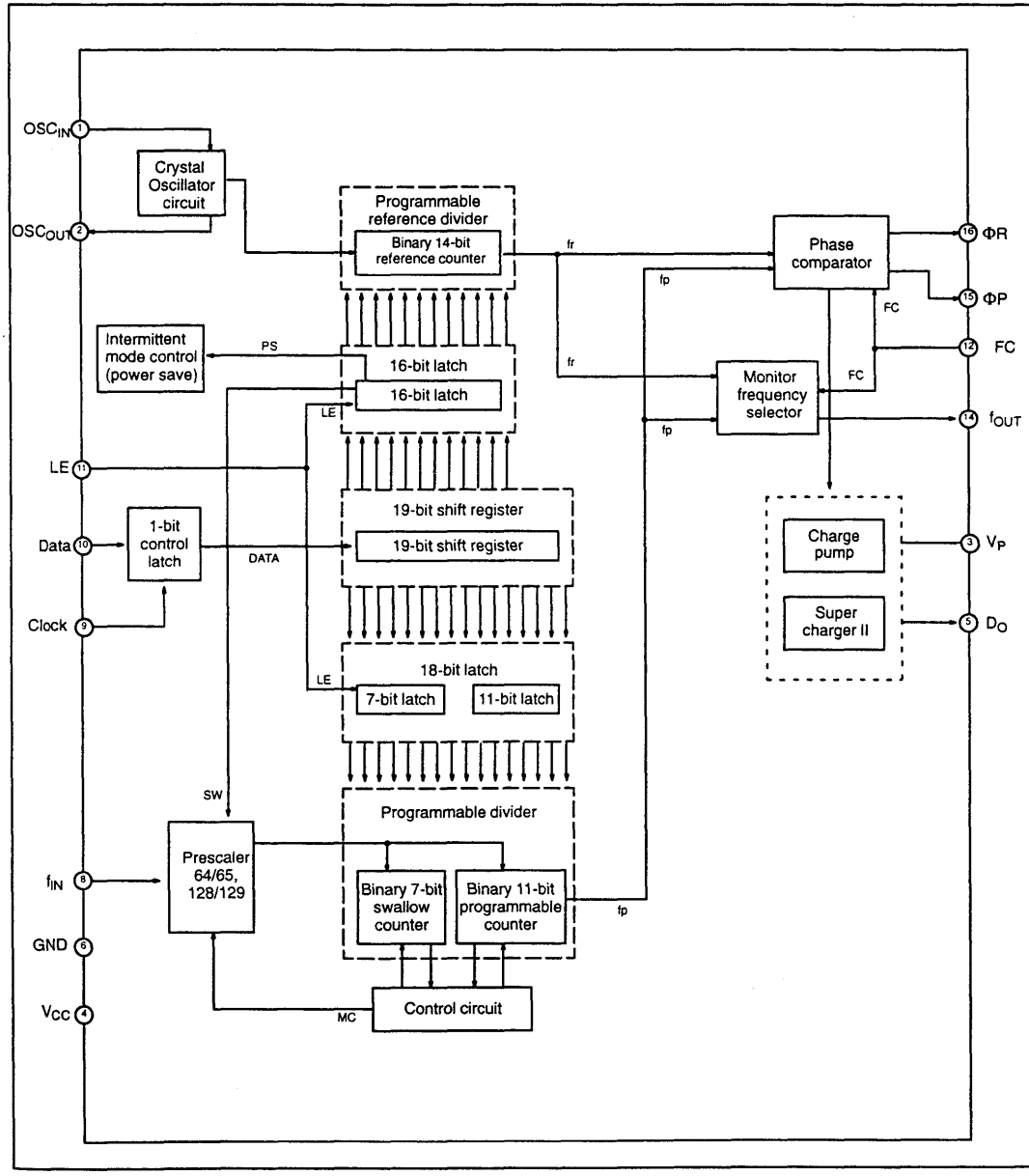


ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating	Unit	Remark
Supply voltage	V_{CC}	–0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	–0.5 to 6.0	V	ΦP, fout
Output current	I_O	±10	mA	
Storage temperature	Tstg	–55 to +125	°C	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output Connection for external crystal.
3	V_P	–	Power supply input for charge pump
4	V_{CC}	–	Power supply
5	D_O	O	Charge pump output Phase of charge pump can be reversed based on FC input.
6	GND	–	Ground
7	LD	O	Lock detector output The output level is usually high. Only when there is a phase error between fr and fp, LD becomes low for the period corresponding to the error.
8	f_{IN}	I	Prescaler input Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register Data is shifted into the shift register on the rising edge of the clock.
10	Data	I	Serial data input using binary code The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 16-bit latch. When it is low, data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input (with internal pull up resistor) When LE is high, the data of the shift register are transferred to a latch, depending on the control bit in the serial data.
12	FC	I	Phase switch input for phase comparator (with internal pull-up resistor) When FC is low, the characteristics of the charge pump and phase comparator are reversed The FC input signal is also used to control the f_{OUT} pin (test pin) output (f_R or f_P).
13	NC	–	No connection
14	f_{OUT}	O	Monitor pin of phase comparator When FC is high, f_{OUT} outputs programmable reference divider output(fr). When FC is low, f_{OUT} outputs programmable divider output(fp).
15	ΦP	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input. ΦR pin is a C-MOS output.

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} + R \quad (A < N)$

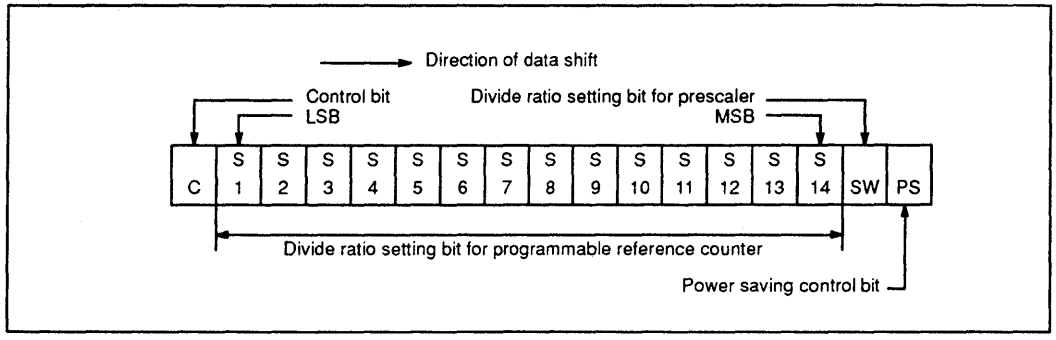
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial data input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 16-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	16 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 16-bit latch and a 14-bit reference counter. The serial 17-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

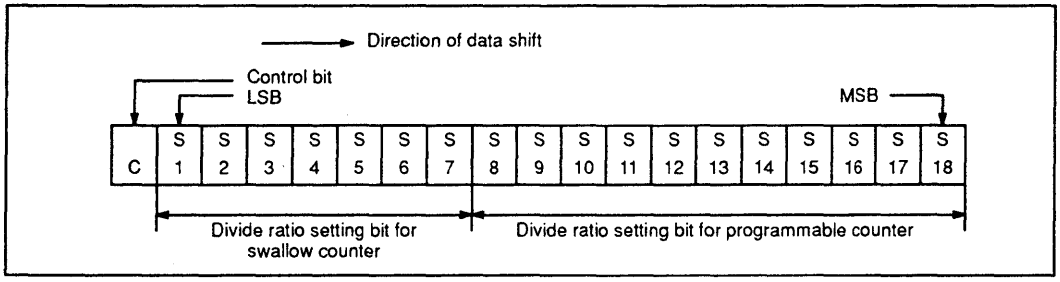
Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
   Low: 128 or 129
   High: 64 or 65
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (6 to 16,383).
4. C: Control bit: Set high.
5. PS: This bit controls stand by mode.
   High : Nomal mode
   Low : Stand by mode
6. Start data input with MSB first .

(b) Programmable divider divide ratio

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

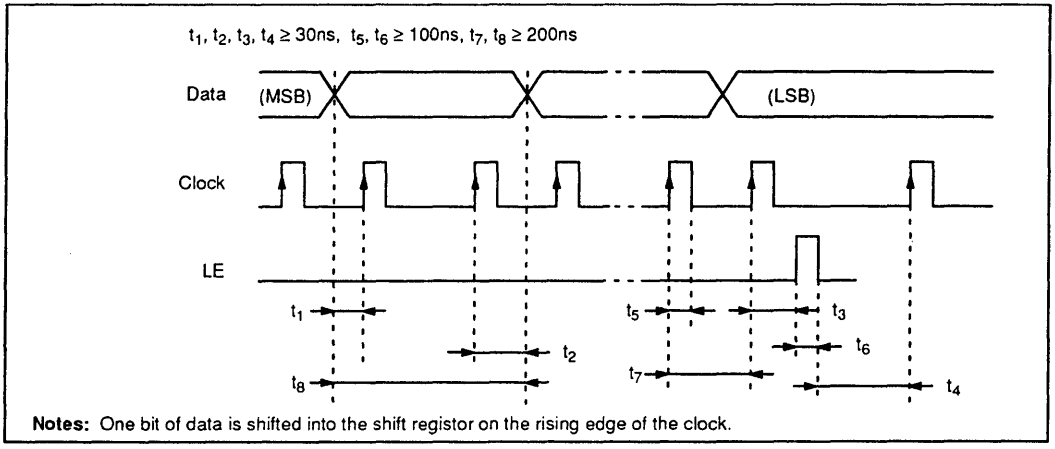
- 11-bit programmable counter divide ratio

Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for 11-bit programmable counter.
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18: These bits select the divide ratio of programmable counter (5 to 2,047).
4. C: Control bit: (Set low)
5. Start data input with MSB first.

Serial data input timing



Notes: One bit of data is shifted into the shift registor on the rising edge of the clock.

Power saving mode (Intermittent operation control circuit)

Setting PS bit to Low, MB1516A enters into power saving mode resultatly current sonsumption can be limited to 100µA (typ.). Setting PS bit to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_R) and comparison frequency (f_P) and may in the worst case take longer time for lock up of the loop. To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

Relation between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ΦR, ΦP) are reversed depending on the FC pin input level. Also, the monitor pin (f_{OUT}) output is controlled by the FC pin. The relationship between the FC input level and each of D_O, ΦR, and ΦP is shown below:

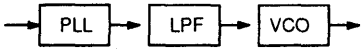
	FC = High or open				FC = Low			
	Do	ΦR	ΦP	f_{OUT}	Do	ΦR	ΦP	f_{OUT}
$f_R > f_P$	H	L	L	(fr)	L	H	Z(*1)	(fp)
$f_R < f_P$	L	H	Z(*1)	(fr)	H	L	L	(fp)
$f_R = f_P$	Z(*1)	L	Z (*1)	(fr)	Z(*1)	L	Z(*1)	(fp)

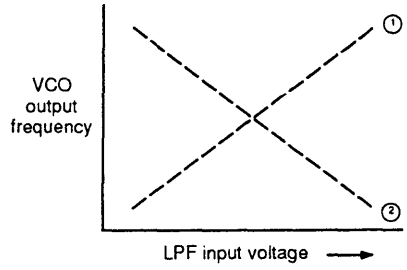
*1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

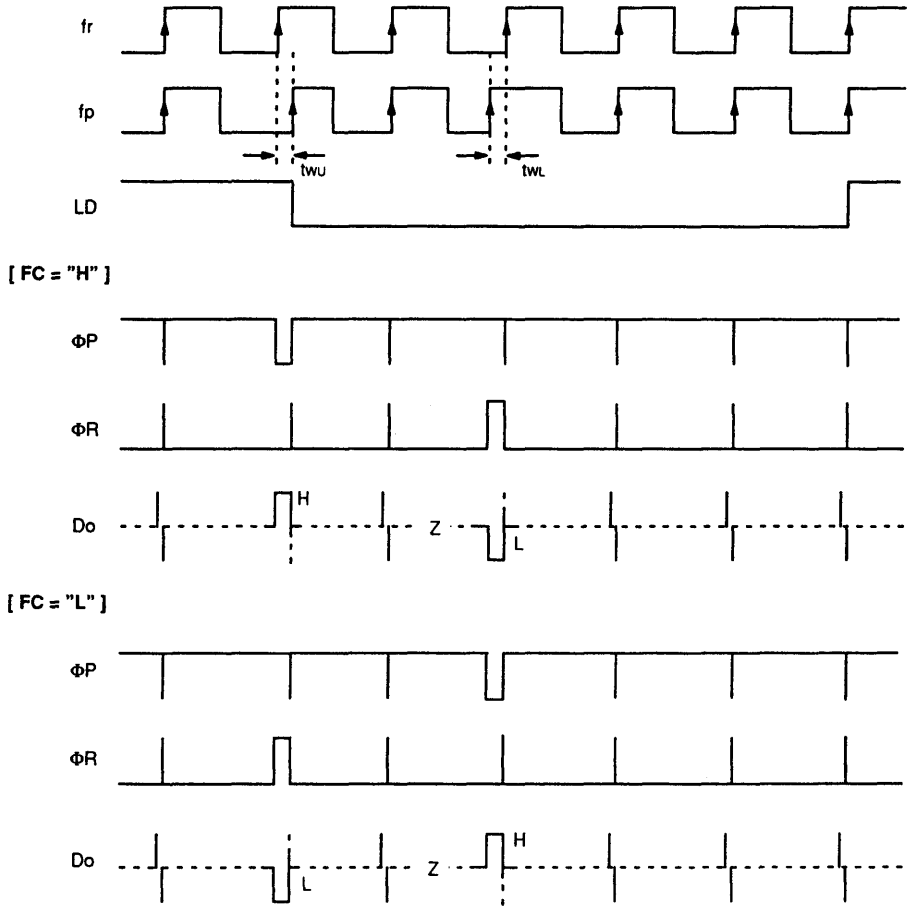
*: When the LPF and VCO characteristics are similar to ①, set FC high or open.

*: When the VCO characteristics are similar to ②, set FC low.





Phase comparator output waveforms



Notes: 1. Phase difference detection range: -2π to $+2\pi$

2. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.

3. twu and twL depend on OSCin input frequency.

   twu ≥ 8/fosc (e. g. twu ≥ 625ns, foscin = 12.8 MHz)

   twL ≤ 16/fosc (e. g. twL ≤ 1250ns, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	Vp	Vcc	–	5.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

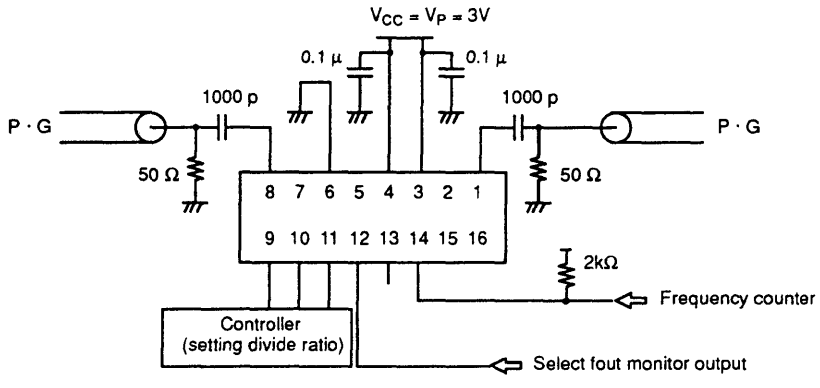
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current		I_{CC}	–	6.5	–	mA	With f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Operating frequency	f_{IN}	f_{IN}	300	–	1100	MHz	AC coupling. The minimum operating frequency is measured with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	$P_{f\,IN}$	–10	–	6	dBm	50Ω
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–	–	–1.0	µA	
Input current	OSC_{IN}	I_{OSC}	–	±50	–	µA	
	FC, LE	I_{LE}	–	–60	–	µA	
High-level output voltage	Except D_O and OSC_{OUT}	V_{OH}	2.1	–	–	V	V_{CC} = 3 V, I_{OH} = –1.0mA
Low-level output voltage		V_{OL}	–	–	0.4	V	Vcc = 3V, I_{OL} = 1.0mA
High-impedance Cut off current	D_O, fout, ΦP	I_{OFF}	–	–	1.1	µA	V_{CC} = 3.6V V_P = 5 V
Output current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	Vcc = 3V
		I_{OL}	–	–	1.0	mA	Vcc = 3V

TEST CIRCUIT
(FOR MEASURING INPUT SENSITIVITY fin/OSCin)

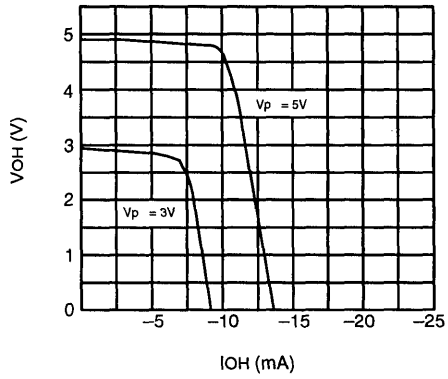


4

TYPICAL CHARACTERISTIC CURVES

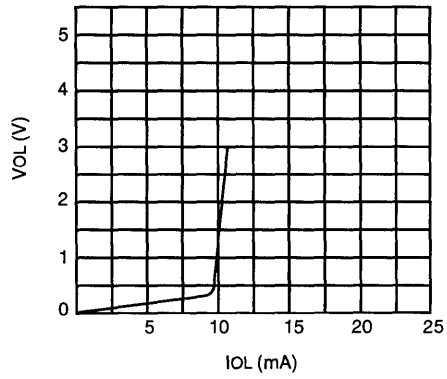
Charge pump current vs. Do voltage

Vcc =3.0V

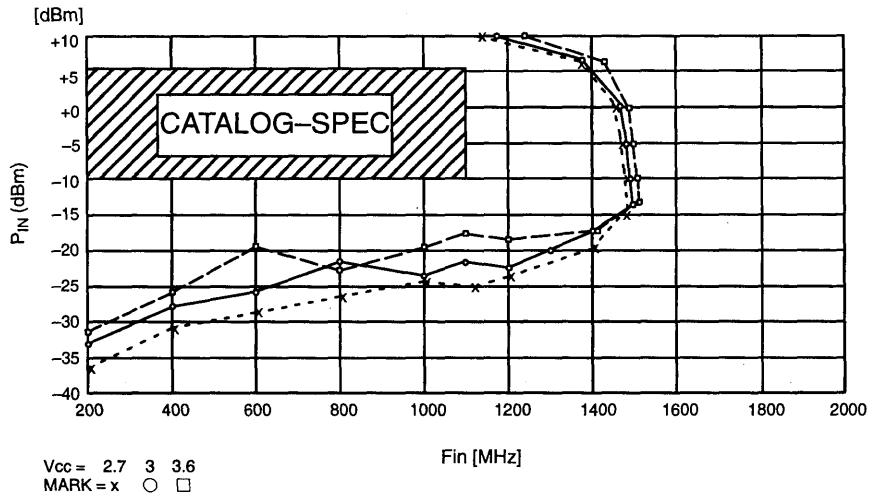


Charge pump current vs. Do voltage

Vcc =3.0V



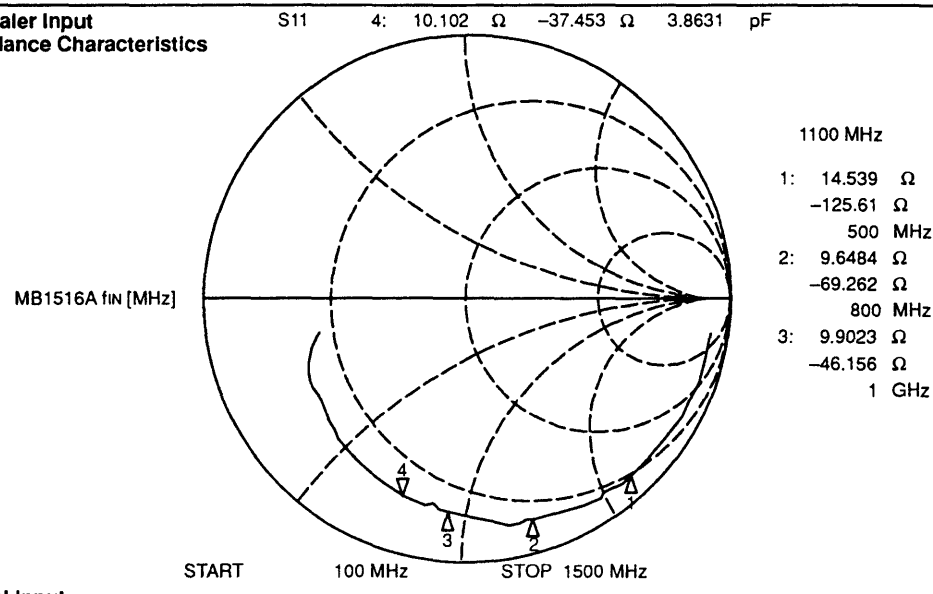
Fin Input sensitivity vs. Input frequency



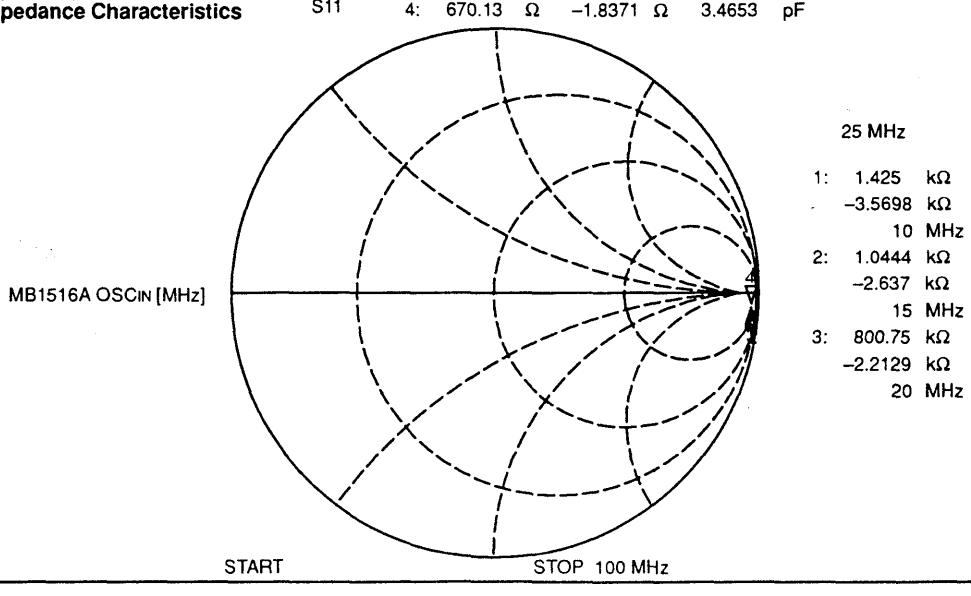
Vcc = 2.7 3 3.6
MARK = x ○ □

TYPICAL CHARACTERISTIC CURVES (Continued)

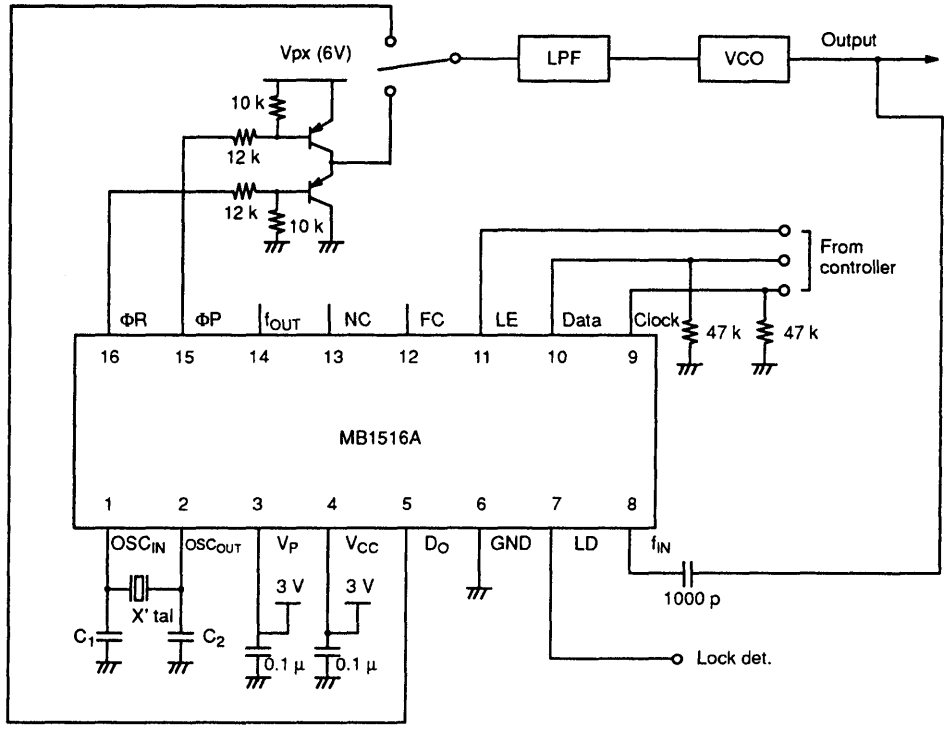
Prescaler Input Impedance Characteristics



Crystal Input Impedance Characteristics



APPLICATION EXAMPLE

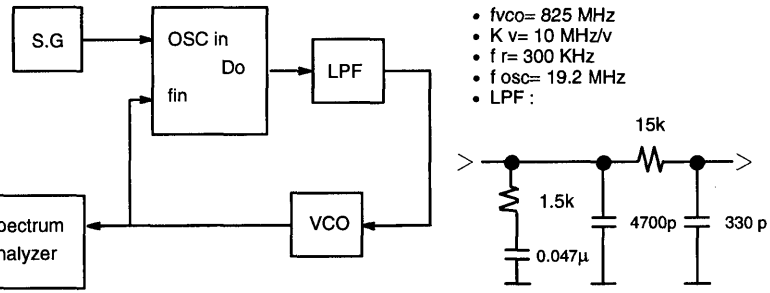


V_{PX} : Maximum 6 V
C_1, C_2 : Depend on the crystal parameters
LE, FC : With internal pull-up resistor
ΦP : N-ch open drain output
ΦR : C-MOS output

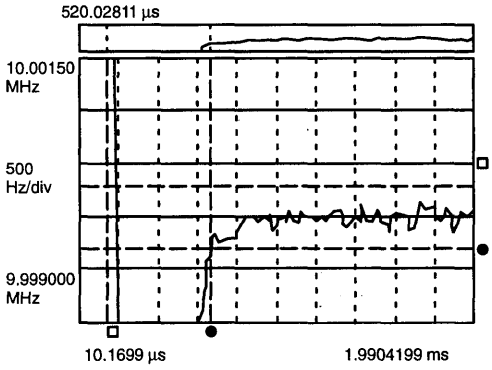
REFERENCE INFORMATION

Typical plots measured with the test circuit shown on the right of this description are shown below. Each plot shows lock up time, phase noise with various span.

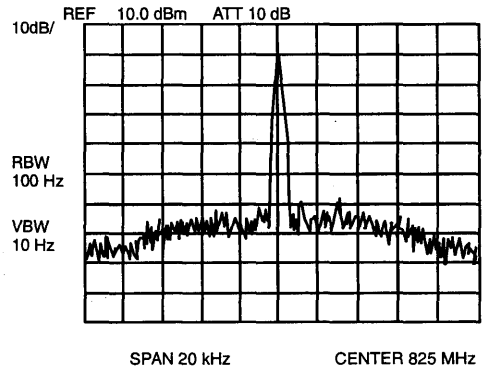
Test Circuit



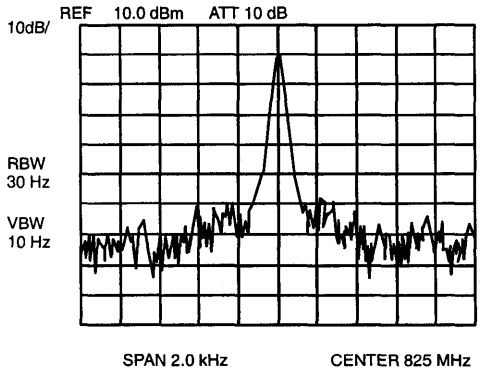
PLL Lock Up Time



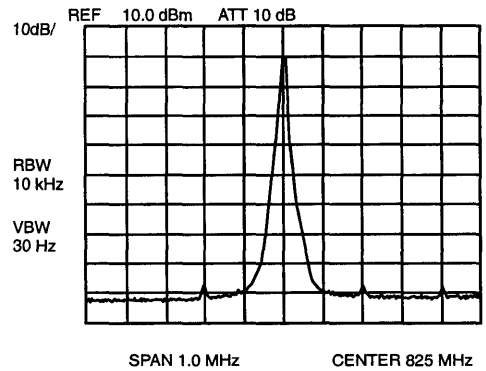
PLL Phase Noise



PLL Phase Noise

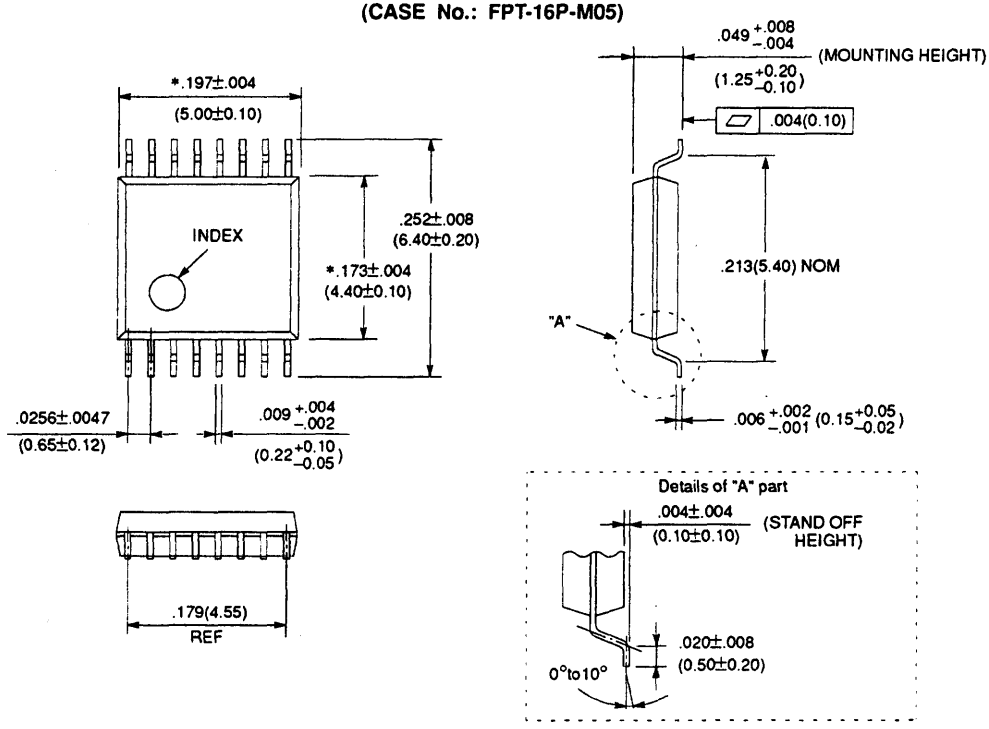


PLL Reference Leakage



PACKAGE AND DIMENSION

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

DS04–21325–1aE

FUJITSU

DATA SHEET

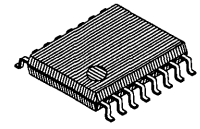
MB1517A *ASSP*

2.0 GHz High–Speed Tuning PLL Frequency Synthesizer

4

The Fujitsu MB1517A is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. MB1517A achieves the low noise performance as well as the high–speed lock-up which is required for digital mobile communications.
The MB1517A can operate from a single +3 V supply. Fujitsu's advanced technology achieves an Icc of 12 mA (typical) as well as 100 µA (typical) at power down mode.

Plastic SSOP, 16 pin



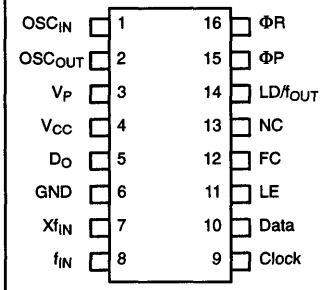
(FPT–16P–M05)

FEATURES

- High operating frequency : f_{IN} = 2.0 GHz (P_{IN} = –10 dBm)
- Pulse-swallow function : High-speed two-modulus prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 12 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 µA typ.
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter: 5 to 2,047
- Serial input 17-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit switch counter sets prescaler divide ratio
  1-bit power saving function control
  1-bit LD/font switch
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16–pin SSOP (shrink small outline) package

PIN ASSIGNMENT

(TOP VIEW)



(FPT–16P–M05)

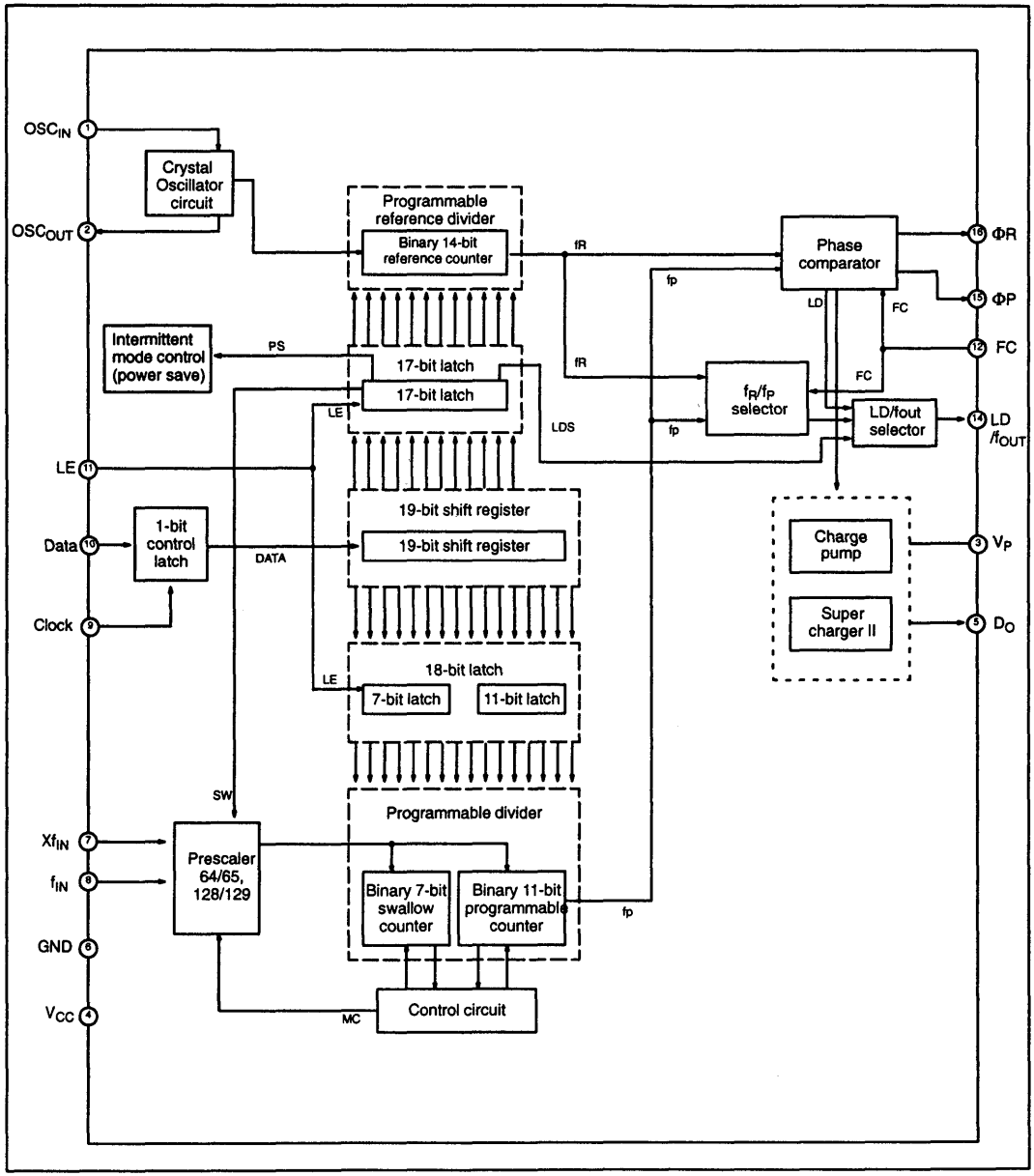
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameters	Symbol	Rating	Unit	Remark
Supply voltage	V_{CC}	–0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	–0.5 to 6.0	V	ΦP, LD/fout
Output current	I_O	±10	mA	
Storage temperature	Tstg	–55 to +125	°C	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output Connection for external crystal.
3	V_P	-	Power supply input for the internal charge pump
4	V_{CC}	-	Power supply
5	D_O	O	Charge pump output Phase characteristics of the charge pump can be reversed by FC input.
6	GND	-	Ground
7	Xfin	I	Complementary input of the prescaler Xfin pin should be grounded via a capacitor.
8	f_{IN}	I	Prescaler input Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register Data is shifted into the shift register on the rising edge of the clock.
10	Data	I	Serial data input using binary code The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 17-bit latch. When it is low, data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input When LE is high, the data of the shift register are transferred to a latch, according to the control bit in the serial data.
12	FC	I	Phase switch input for phase comparator When FC is low, the characteristics of the charge pump and phase comparator are reversed The FC input signal is also used to control the f_{OUT} pin (test pin) output (f_R or f_P).
13	NC	-	No connection
14	LD/f_{OUT}	O	Lock detector output / Phase comparator monitoring output This is a N-ch open drain output. Either of the outputs is selected by LDS bit of the serial data. a)Lock detector output : at lock state .... LD = "H" at unlock stae .. LD = "L" b)Monitoring output : Phase comparator input signals (f_P, f_R) can be monitored.
15	ΦP	O	Phase comparator output for an external charge pump Phase of the output is reversed according to FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input.

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R \quad (A < N)$

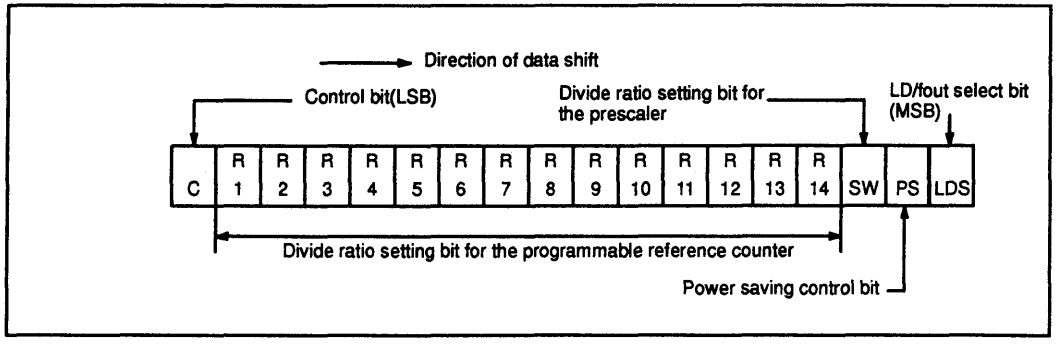
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- P : Preset divide ratio of modules prescaler (64 or 128)

Serial data input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 17-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control data as follows:

Control data	Destination of serial data
H	17 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 18-bit shift register, a 17-bit latch and a 14-bit reference counter. The serial 18-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

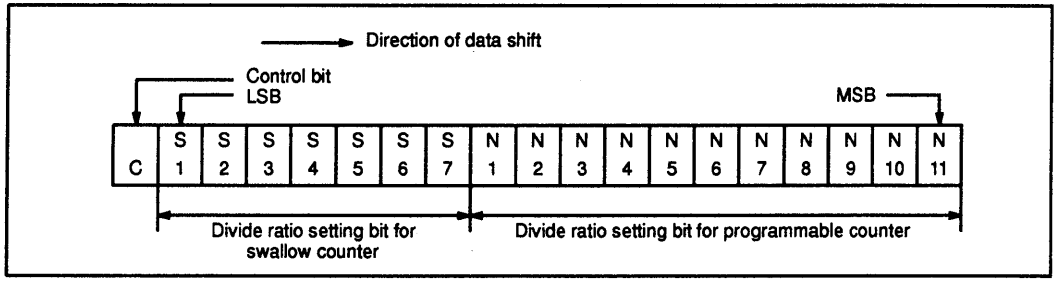
Divide ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
   Low: 128 or 129
   High: 64 or 65
3. R1 to R14: These bits select the divide ratio of the programmable reference counter (6 to 16,383).
4. C: Control bit: Set high.
5. PS: This bit controls power saving mode.
   High : Nomal operation
   Low : Power saving mode
6. LDS: This bit controls LD/fout output signal
   High : fout signal (f_R or f_P) is selected and output via LD/fout pin.
   Low : Lock detect signal is selected and output via LD/fout pin.
7. Start data input with MSB first .

(b) Programmable divider divide ratio

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

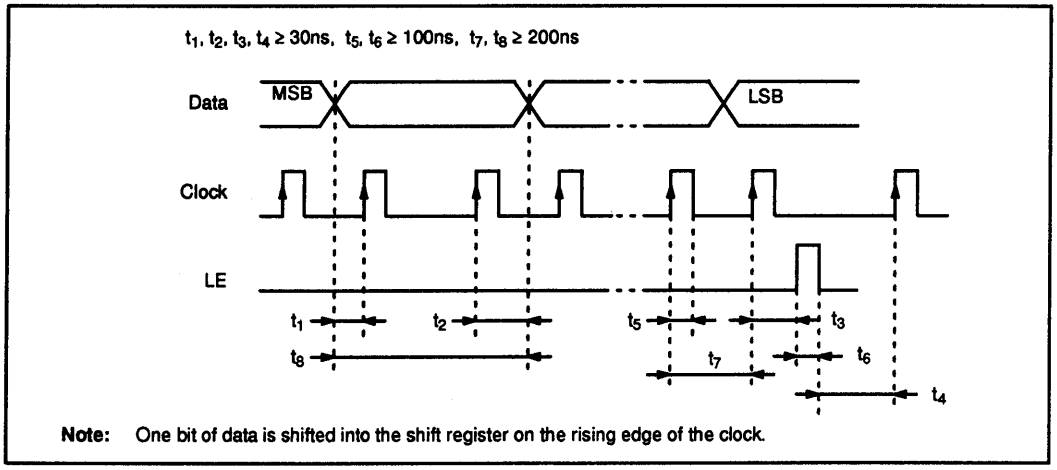
- 11-bit programmable counter divide ratio

Divide ratio N	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for the 11-bit programmable counter.
2. S1 to S7: These bits select the divide ratio of the swallow counter (0 to 127).
3. N1 to N11: These bits select the divide ratio of the programmable counter (5 to 2,047).
4. C: Control bit: (Set low)
5. Start data input with MSB first.

Serial data input timing



Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Power saving mode (Intermittent operation control circuit)

Setting PS bit to Low, MB1517A enters into power saving mode resultatly current sonsumption can be limited to 100µA (typ.).
Setting PS bit to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from power saving mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_R) and comparison frequency (f_P) and may in the worst case take longer time for lock up of the loop. To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

Relation between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ΦR, ΦP) are reversed depending on the FC pin input level. Also, the monitor pin (f_{OUT}) output is controlled by the FC pin. The relationship between the FC input level and each of D_O, ΦR, and ΦP is shown below:

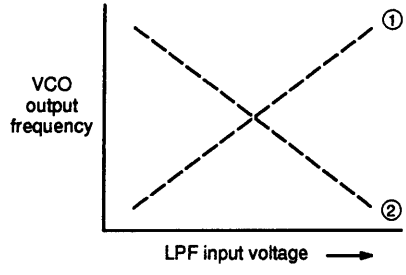
	FC = High				FC = Low			
	Do	ΦR	ΦP	f_{OUT}	Do	ΦR	ΦP	f_{OUT}
$f_R > f_P$	H	L	L	(f_R)	L	H	Z(*1)	(f_P)
$f_R < f_P$	L	H	Z(*1)	(f_R)	H	L	L	(f_P)
$f_R = f_P$	Z(*1)	L	Z (*1)	(f_R)	Z(*1)	L	Z(*1)	(f_P)

*1: High impedance

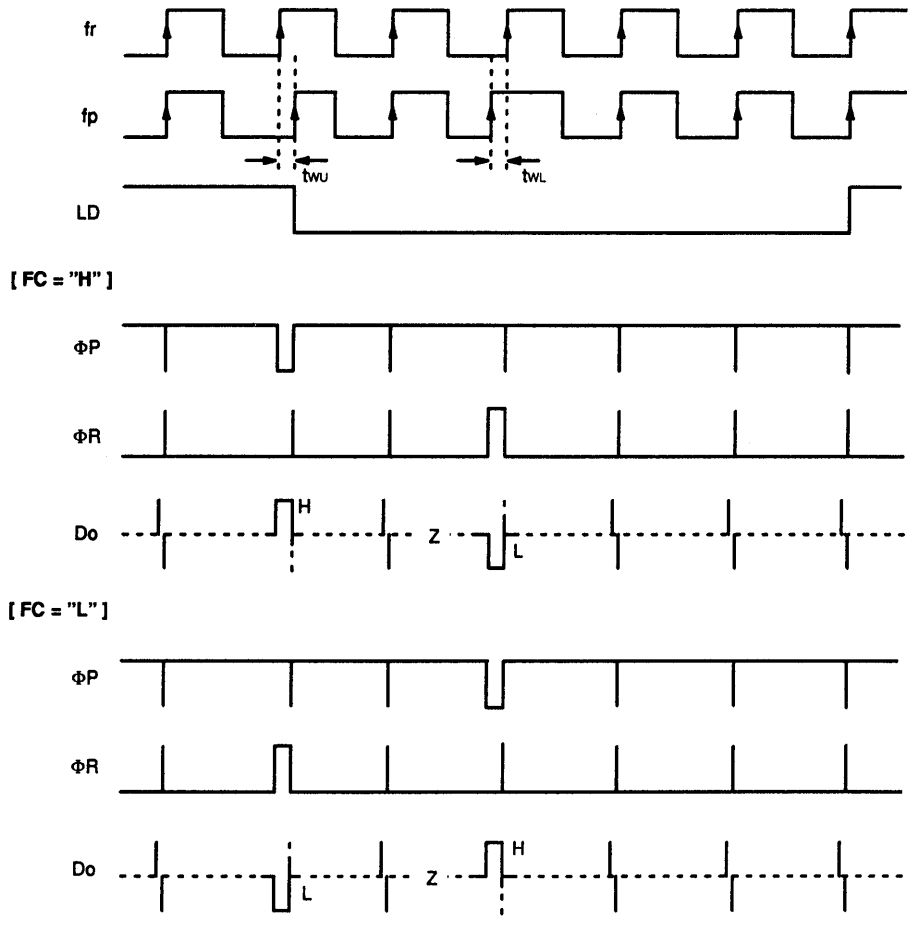
When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

*: When the LPF and VCO characteristics are similar to ①, set FC high.

*: When the VCO characteristics are similar to ②, set FC low.



Phase comparator output waveforms



Notes: 1. Phase difference detection range: -2π to $+2\pi$

2. LD output becomes low when phase error is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cysles or more.

3. t_{WU} and t_{WL} depend on OSCin input frequency.

   $t_{WU} \geq 8/fosc$ (e. g. $t_{WU} \geq 625ns$, foscin = 12.8 MHz)

   $t_{WL} \leq 16/fosc$ (e. g. $t_{WL} \leq 1250ns$, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	Vp	Vcc	-	5.0	V	
Input voltage	V_I	GND	-	V_{CC}	V	
Operating temperature	Ta	-40	-	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

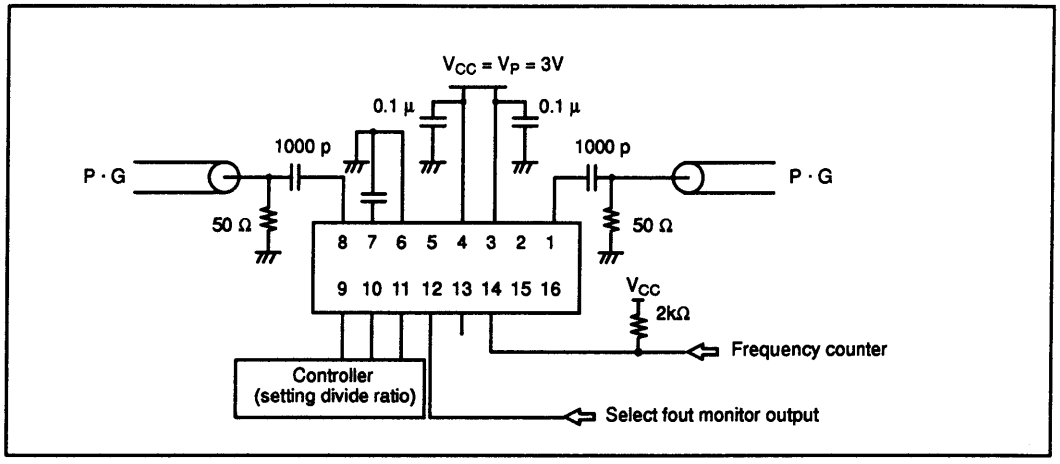
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

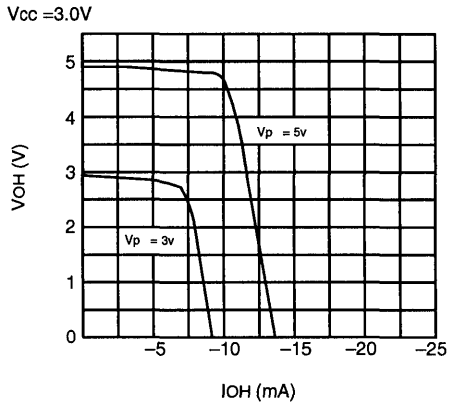
Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current		I_{CC}	–	12	–	mA	With f_{IN} = 2.0 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Stand by current		I_{PS}	–	100	–	µA	PS bit = "L"
Operating frequency	f_{IN}	f_{IN}	1000	–	2000	MHz	AC coupling. The minimum operating frequency is measured with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	$P_{f\,IN}$	–10	–	6	dBm	50Ω System
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock, LE, FC	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{IN}	I_{OSC}	–100		+100	µA	
High-level output voltage	Except D_O and OSC_{OUT}	V_{OH}	2.1	–	–	V	V_{CC} = 3 V, I_{OH} = –1.0mA
Low-level output voltage		V_{OL}	–	–	0.4	V	Vcc = 3V, I_{OL} = 1.0mA
High-impedance Cut off current	D_O, LD/fout, ΦP	I_{OFF}	–	–	1.1	µA	V_{CC} = 3.6V, V_P = 5 .0V V_{OOP} = GND to 6 .0V
Output current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	Vcc = 3V
		I_{OL}	–	–	1.0	mA	Vcc = 3V

TEST CIRCUIT
(for Measuring Input Sensitivity fin/OSCin)

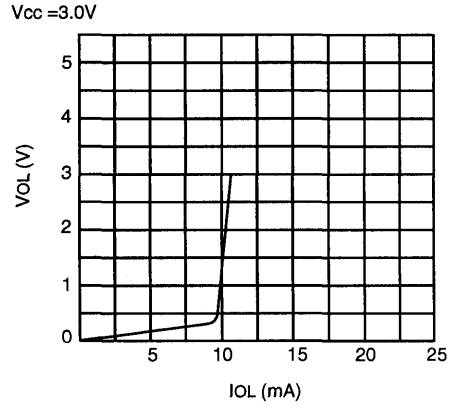


TYPICAL CHARACTERISTIC CURVES

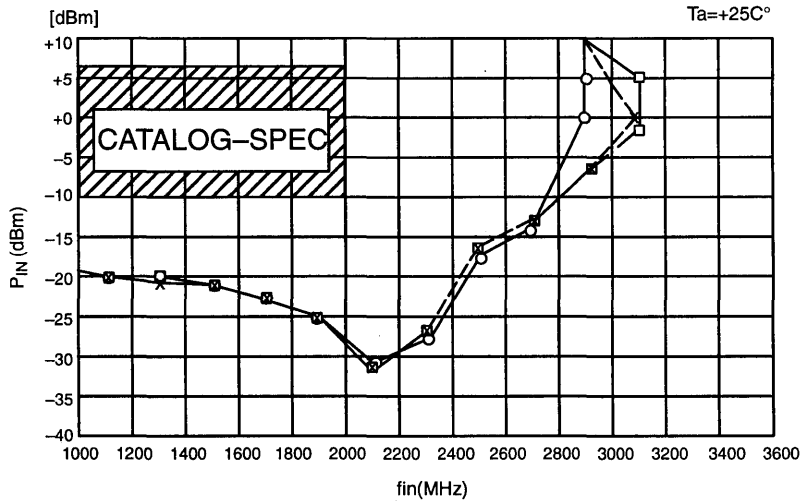
Charge pump current vs. Do voltage



Charge pump current vs. Do voltage



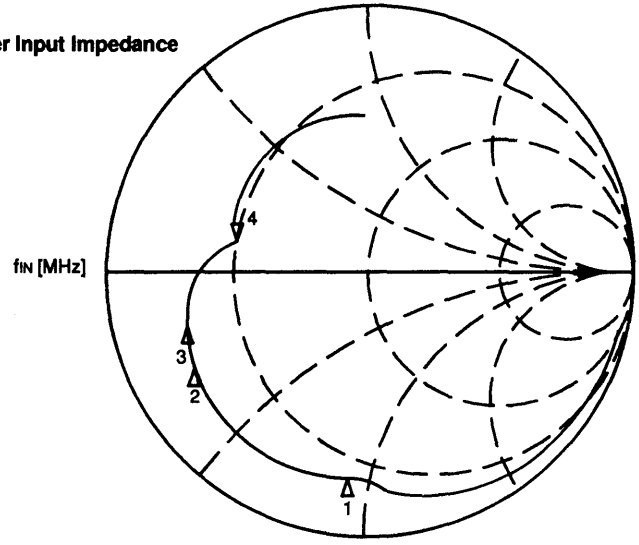
Input sensitivity vs. Input frequency



Vcc = 2.7 3 3.6
MHz = x O □

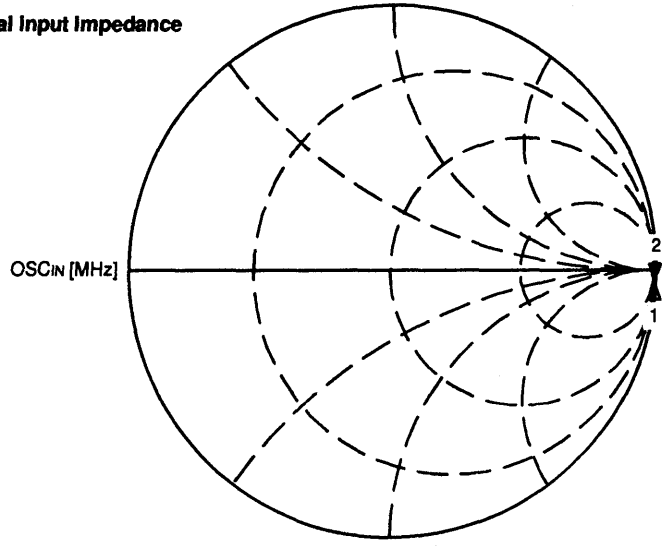
TYPICAL CHARACTERISTIC CURVES (Continued)

Prescaler Input Impedance



1: 11.115 Ω
-45.209 Ω
1 GHz
2: 8.3428 Ω
-12.503 Ω
1.5 GHz
3: 9.2764 Ω
-7.1001 Ω
1.6 GHz
4: 17.173 Ω
5.8379 Ω
2 GHz

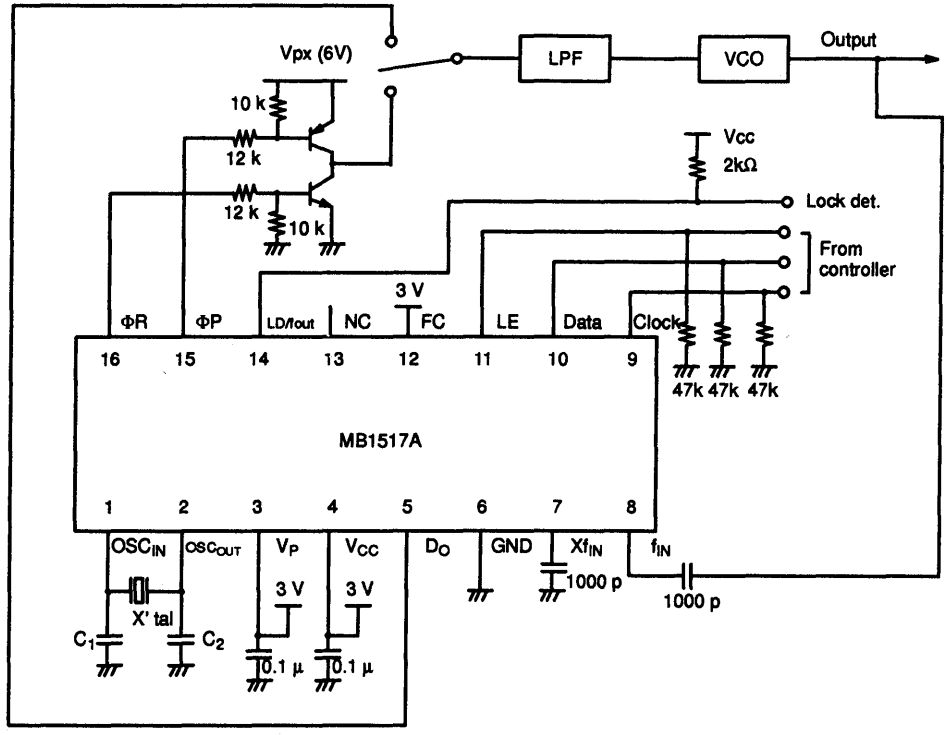
Crystal Input Impedance



1: 2.1155 Ω
-4.4665 Ω
10 MHz
2: 426.63 Ω
-2.201 kΩ
25 MHz

4

TYPICAL APPLICATION EXAMPLE

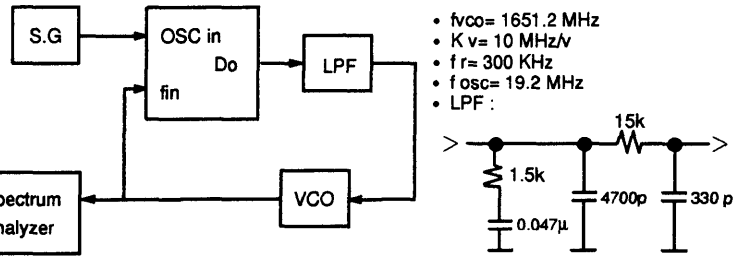


V_{PX} : Maximum 6 V
C_1, C_2 : Depend on the crystal oscillatar
ΦP, LD/fout : N-ch open drain output
ΦR : C-MOS output

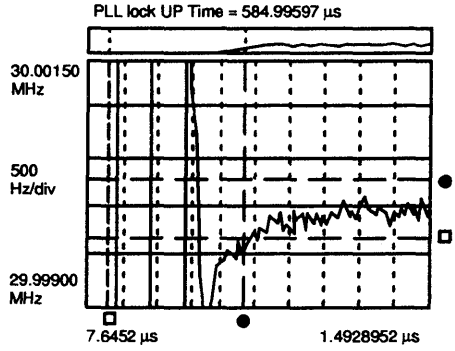
REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below.
Each plot shows lock up time, phase noise, and reference leakage.

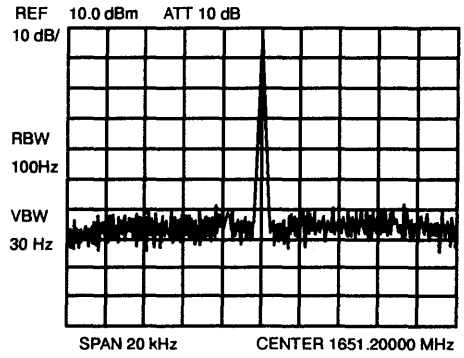
Test Circuit



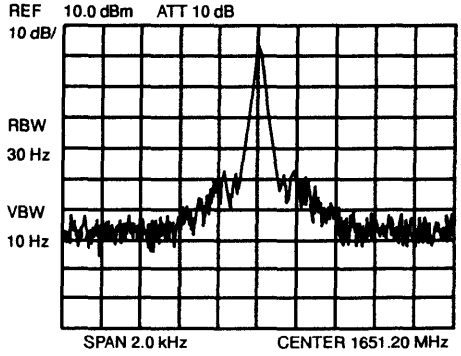
PLL Lock Up Time



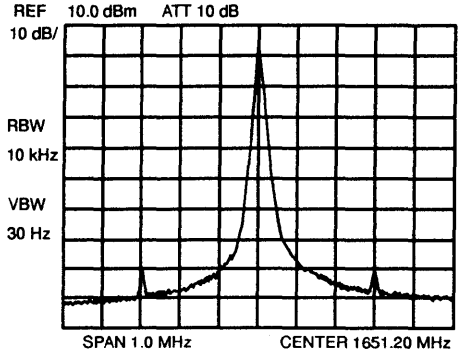
PLL Phase Noise



PLL Phase Noise



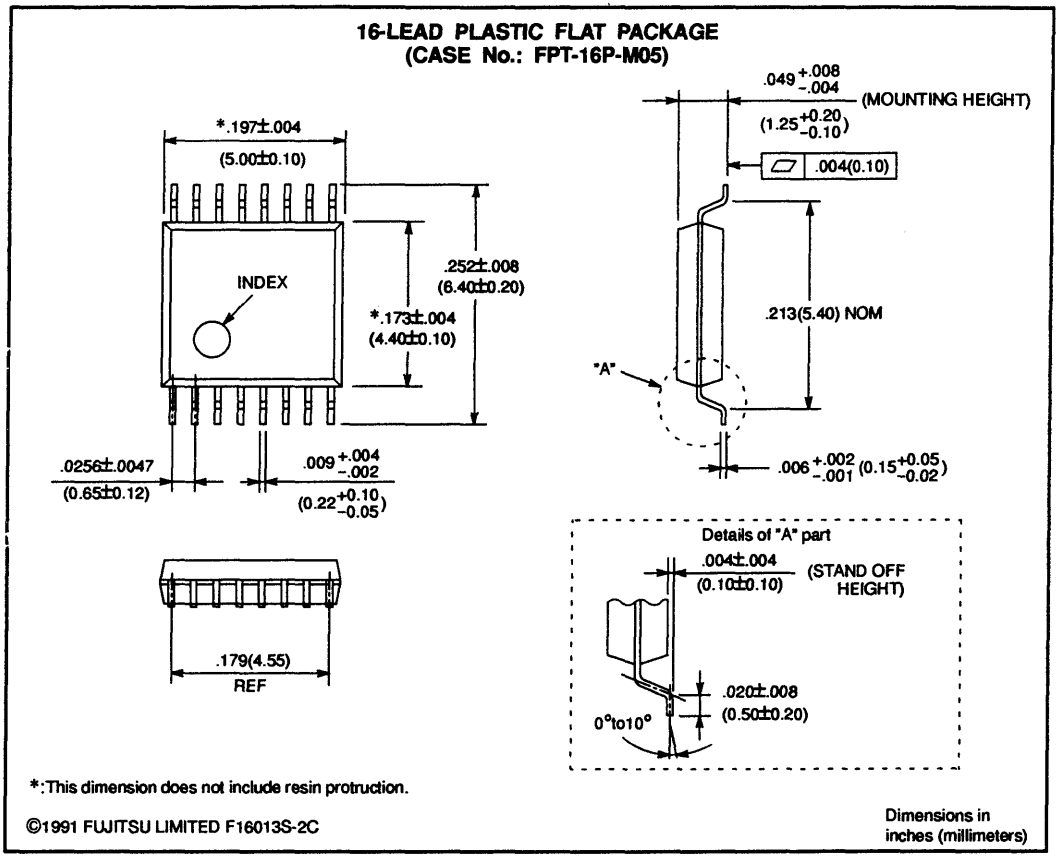
PLL Reference Leakage



ORDERING INFORMATION

Part number	Package	Remarks
MB1517APFV1	Plastic · SSOP, 16-pin (FPT-16P-M05)	

PACKAGE DIMENSION

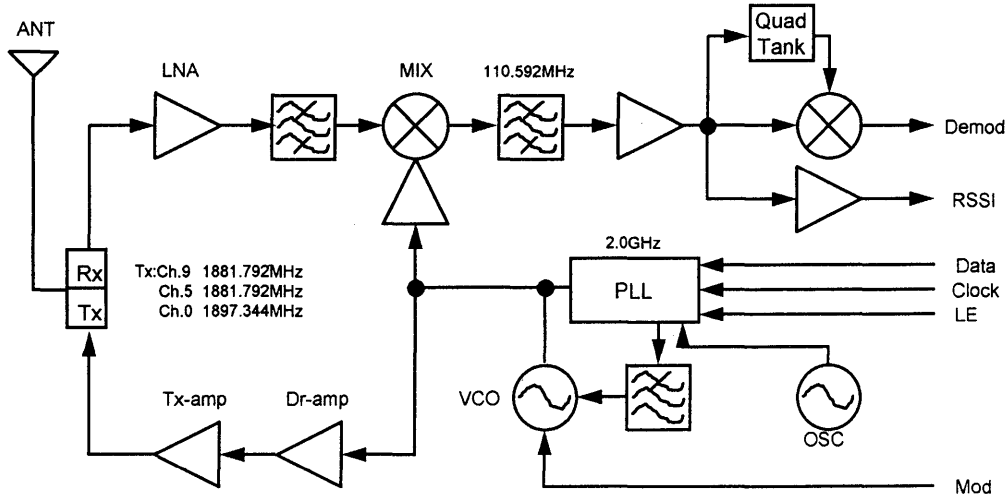


MB1517A Test Data

February 1995

ANALOG LSI DESIGN DEPARTMENT

Block Diagram of DECT RF part



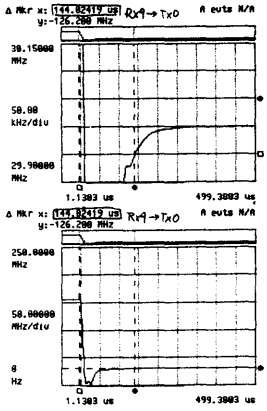
PLL Serial Data Setting (fr=1.728MHz)

	Frequency	PLL Divide Ratio Prescaler(M)	N-Counter(N)	A-Counter(A)
Rx	Ch.9 1771.200MHz	64	16	1
	-	-	-	-
	15.552MHz			
	-	-	-	-
	Ch.0 1786.752MHz	64	16	10
	126.144MHz			
Tx	Ch.9 1881.792MHz	64	17	1
	-	-	-	-
	15.552MHz			
	-	-	-	-
	Ch.0 1897.344MHz	64	17	10

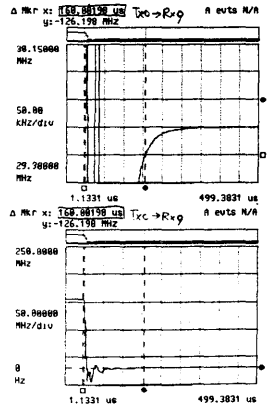
Pulse Swallow Function : fvco = { (M x N) + A } x fr A < N

PLL Hopping Time

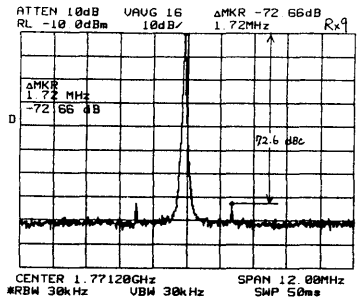
1771.200MHz -> 1897.344MHz,within ± 50KHz
Rx9->Tx0 144 μs



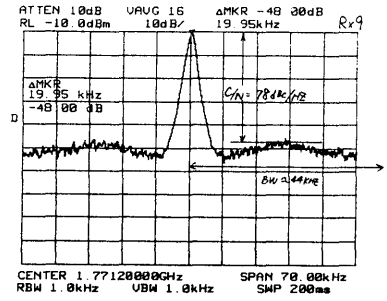
1897.344MHz -> 1771.200MHz,within ± 50KHz
Tx0->Rx9 160 μs



■ Spurious Level



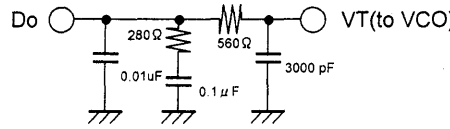
■ Phase Noise / Loop Band Width



■ PLL Characteristics of DECT Application fr=1.728MHz/Vcc=3.0V,Vp=Vvco=3.0V

Parameter		Measured Value	Conditions
Hopping Time	Rx9->Tx0	144 μs	1771.200MHz -> 1897.344MHz,within ± 50KHz
	Tx0->Rx9	160 μs	1897.344MHz -> 1771.200MHz,within ± 50KHz
Spurious Level		72dBc	±1.728MHz offset at 1771.200MHz
Phase Noise		78dBc/Hz	within Loop Bandwidth at 1771.200MHz

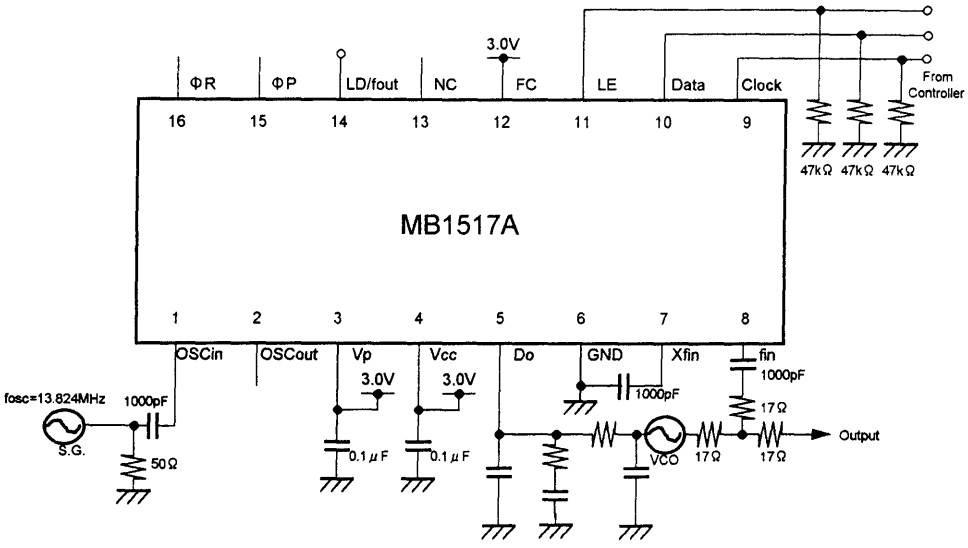
■ Loop filter scamatics



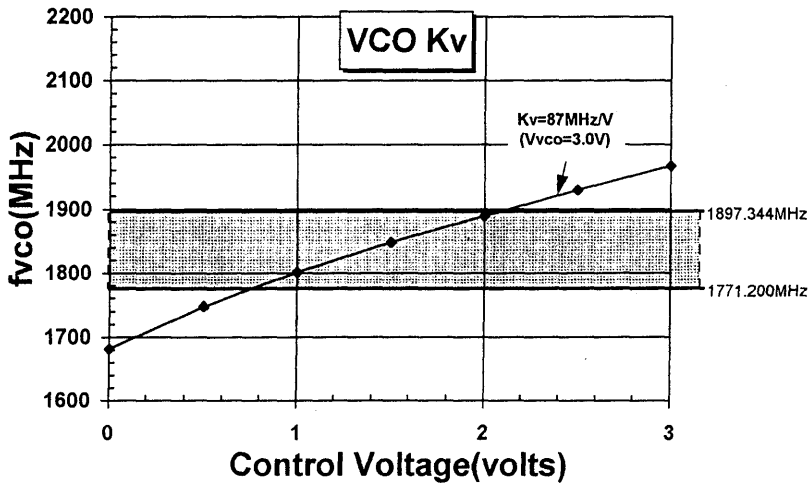
■ VCO; Kv=87MHz/V

(muRata MQE030 - 1835)

APPLICATION EXAMPLE



■ VCO Operating Range



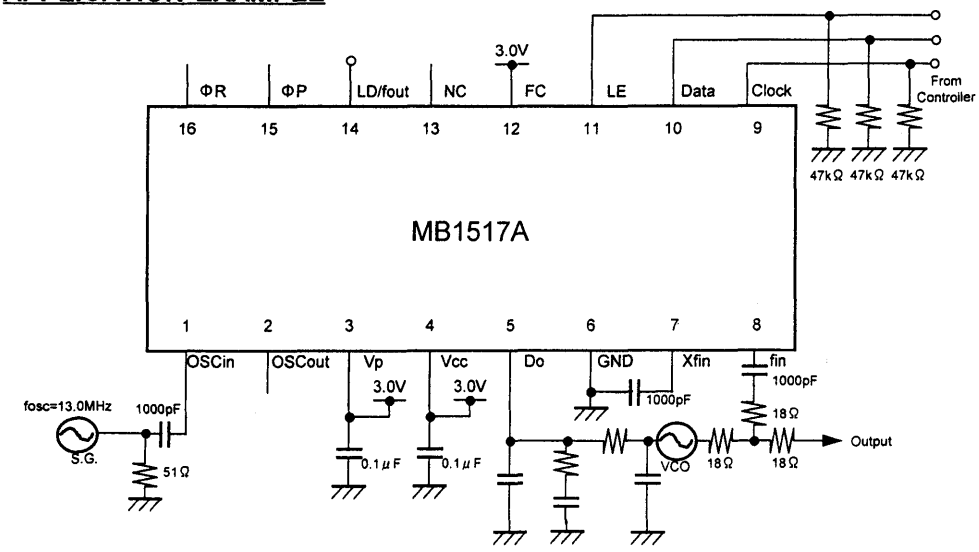
MB1517A Test Data

(PCN Application)

April 1995

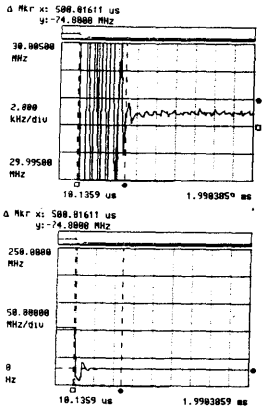
ANALOG LSI DESIGN DEPARTMENT

APPLICATION EXAMPLE

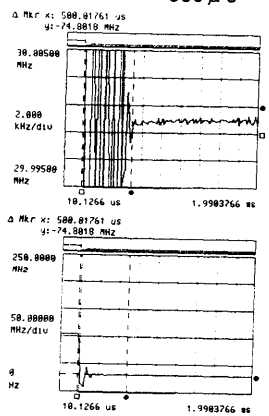


PLL Hopping Time

1797.600MHz -> 1872.400MHz,within ± 1KHz
Lch ->Hch 500 μ s

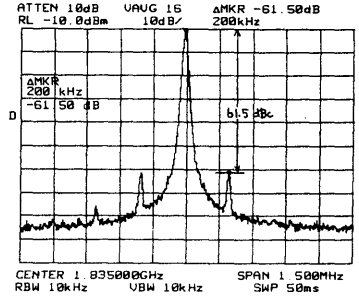


1872.400MHz -> 1797.600MHz,within ± 1KHz
Hch ->Lch 500 μ s

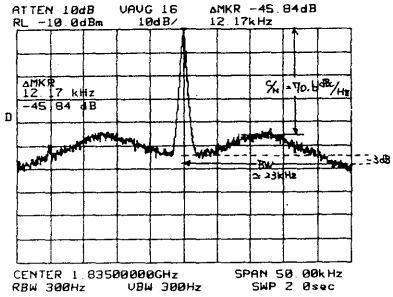


4

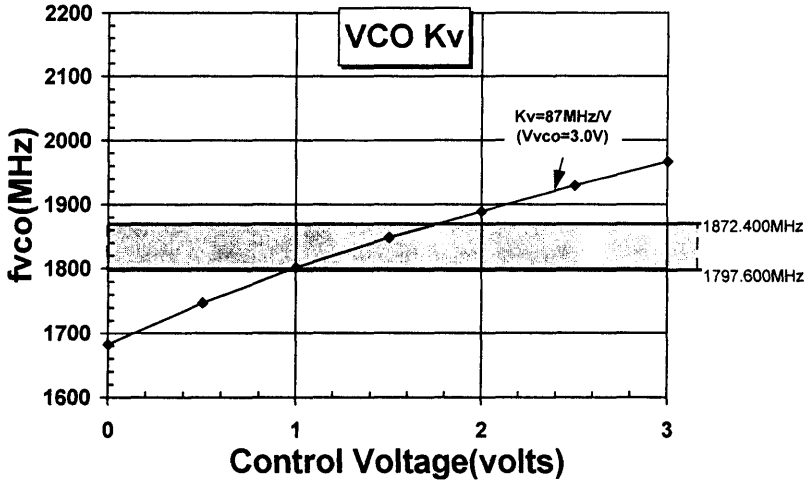
Spurious Level



Phase Noise / Loop Band Width



VCO Operating Range(muRata MQE030-1835)



PLL Serial Data Setting (fr=200kHz)

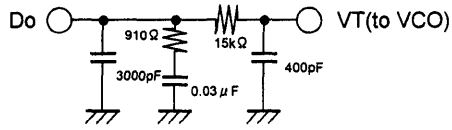
	Frequency		PLL Divide Ratio Prescaler(M)	N-Counter(N)	A-Counter(A)
Rx/Tx	Lo ch 1797.600MHz	74.8MHz	64	140	28
	37.4MHz				
	Mi ch 1835.000MHz		64	143	23
	37.4MHz				
	Hi ch 1872.400MHz		64	146	18

Pulse Swallow Function : fvco = { (M x N) + A } x fr A < N

PLL Characteristics of PCN Application fr=200kHz/Vcc=3.0V,Vp=Vvco=3.0V

Parameter		Measured Value	Conditions
Hopping Time	Lch->Hch	500 μ s	1797.600MHz -> 1872.400MHz,within ± 1KHz
	Hch ->Lch	500 μ s	1872.400MHz -> 1797.600MHz,within ± 1KHz
Spurious Level		61dBc	±200kHz offset at 1835.000MHz
Phase Noise		70dBc/Hz	within Loop Bandwidth at 1835.000MHz

Loop filter scamatics



VCO; Kv=87MHz/V

(muRata MQE030 - 1835)

DS04–21311–2aE

FUJITSU

DATA SHEET

MB1518

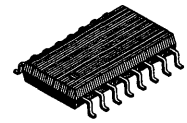
Serial Input PLL Frequency Synthesizer With On–Chip 2.5GHz Prescaler

4

The Fujitsu MB1518 with an on chip 2.5 GHz dual modulus prescaler is a serial input PLL (Phase Locked Loop) frequency synthesizer with pulse swallow function. It is well suited for BS tuner, CATV system applications.

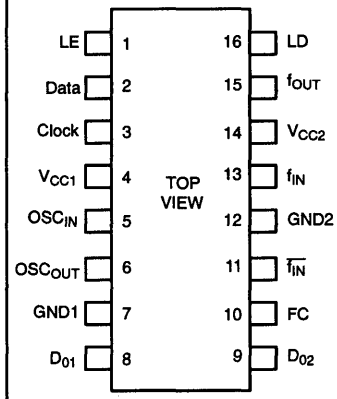
It operates supply voltage of 5.0V typ. and dissipates 16mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- Power supply voltage: V_{CC} = 4.5 to 5.5V
- High operating frequency: f_{in} = 2.5GHz (P_{in} = –4dBm)
- 2.5GHz dual modulus prescaler: P = 512/528
- Low power supply current: I_{CC} = 16mA typ.
- Programmable reference divider : R = 512
- Programmable divider consisting of:
  Binary 5–bit swallow counter (A = 0 to 31)
  Binary 9-bit programmable counter (N = 32 to 511)
- Wide operating temperature: T_a = –40 to +85°C
- Plastic 16-pin flat package (Suffix: –PF)



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



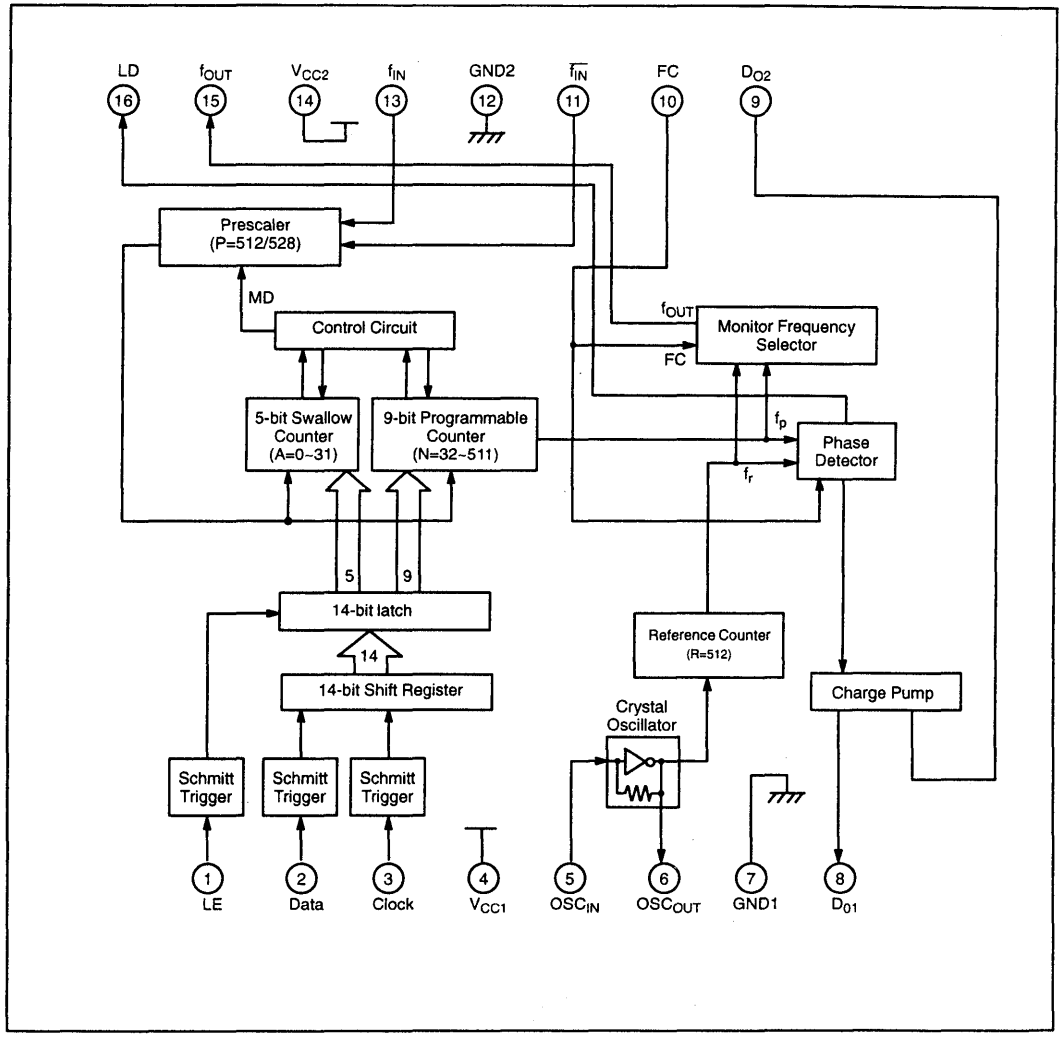
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_O	0.5 to V_{CC} +0.5	V
Output Current	I_O	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	LE	I	Load enable input pin This pin involves a Schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch.
2	Data	I	Serial data of binary code input pin This pin involves a Schmitt trigger circuit.
3	Clock	I	Clock input pin of the 14–bit shift register This pin involves a schmitt trigger circuit. On the rising edge of the clock. one bit of the data shifts into the shift register.
4	V_{CC1}	–	PLL power supply voltage input pin
5 6	OSC_{IN} OSC_{OUT}	I O	Oscillator input pin Oscillator output pin A crystal is connected between the OSC_{IN} pin and the OSC_{OUT} pin.
7	GND1		PLL ground pin
8 9	D_{O1} D_{O2}	O O	Charge pump output pins The phase characteristics can be reversed depending upon the FC pin input level.
10	FC	I	Phase select input pin of the phase detector This pin involves an internal pull up resistor. When this pin is low, characteristics of the charge pump and phase detector can be reversed. This input also selects f_{OUT} pin output level, either fr or fp. Please see page 6.
11	$\overline{f_{IN}}$	I	Complementary input pin of f_{IN} Please connect to GND through a capacitor.
12	GND2	–	Prescaler ground pin
13	f_{IN}	I	Prescaler input pin This signal is input with an AC connection.
14	V_{CC2}	–	Prescaler power supply voltage input pin
15	f_{OUT}	O	Monitor pin of the phase detector input The f_{OUT} pin outputs either the programmable reference divider output frequency fr or programmable divider output frequency fp, depending upon the FC pin input level. FC Pin: H → fOUT Output Signal: fr FC Pin: L → fOUT Output Signal: fp
16	LD	O	Phase detector output pin Normally this pin outputs high. While the phase difference between fr and fp exists, this pin outputs low.

FUNCTIONAL DESCRIPTIONS

DIVIDE RATIO SETTING

Divide ratio can be set using the following equation:

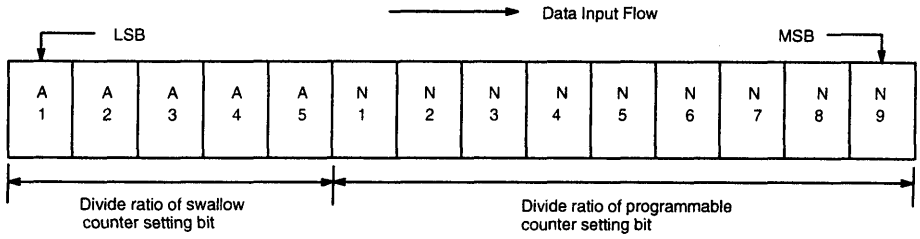
$f_{VCO} = \{(P \times N) + (16 \times A)\} \times f_{OSC} \div R$

f_{VCO}: Output frequency of an external voltage controlled oscillator (VCO)
P: Preset divide ratio of an internal dual modulus prescaler (512)
N: Preset divide ratio of binary 9-bit programmable counter (32 to 511)
A: Preset divide ratio of binary 5-bit swallow counter (0 to 31)
f_{OSC}: Reference oscillator frequency
R: Preset divide ratio of reference counter (512)

SERIAL DATA I NPUT

On the rising edge of the clock, one bit of the data shifts into the shift register.
When the load enable is high, the data stored in the shift register is transferred to the latch.

14-bit serial data format is shown below.



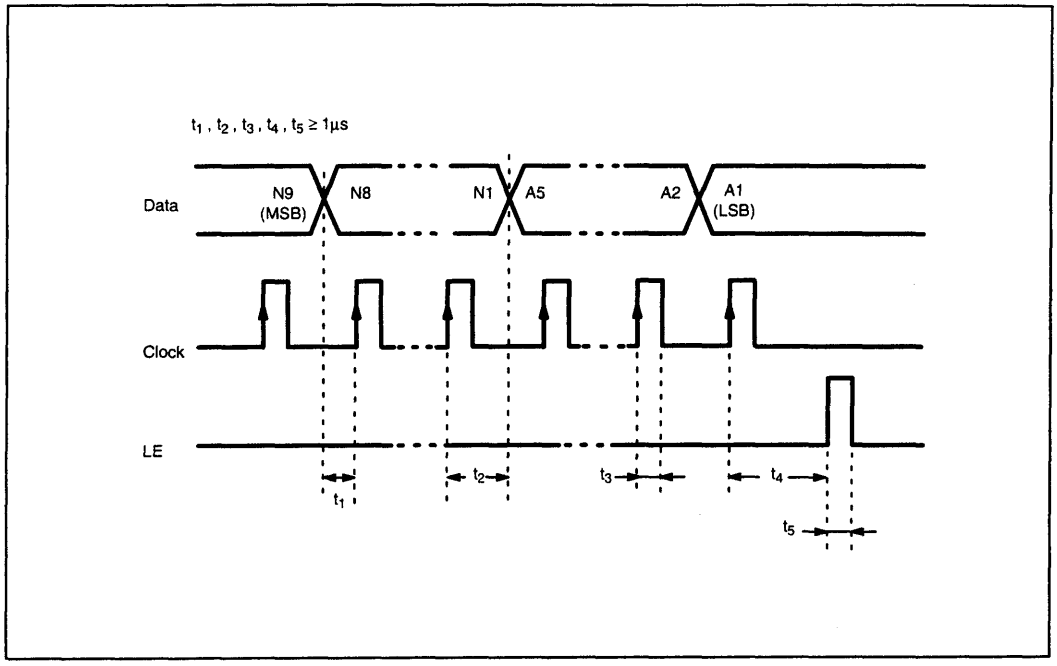
5-bit swallow counter divide ratio (A1 to A5)

Divide Ratio A	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
:	:	:	:	:	:
31	1	1	1	1	1

9-bit programmable counter divide ratio (N1 to N9)

Divide Ratio N	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
32	0	0	0	1	0	0	0	0	0
33	0	0	0	1	0	0	0	0	1
34	0	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:
511	1	1	1	1	1	1	1	1	1

SERIAL DATA INPUT TIMING



Note: On the rising edge of the clock, one bit of the data shifts into the shift register. When LE is high, the data stored the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

The FC pin selects the phase of the phase detector. The phase characteristics (charge pump output) can be reversed depending upon the FC pin input level. The monitor pin (fOUT) output level is selected by the FC pin input level as well.

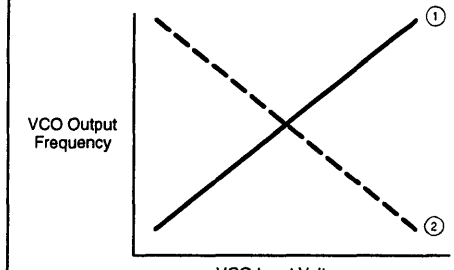
	FC = H (or open)		FC = L	
	D_{01} , D_{02}	fOUT	D_{01} , D_{02}	fOUT
fr > fp	H	Outputs programmable reference divider output frequency (fr)	L	Outputs programmable divider output frequency (fp)
fr = fp	Z		Z	
fr < fp	L		H	

Note:
Z: High-impedance

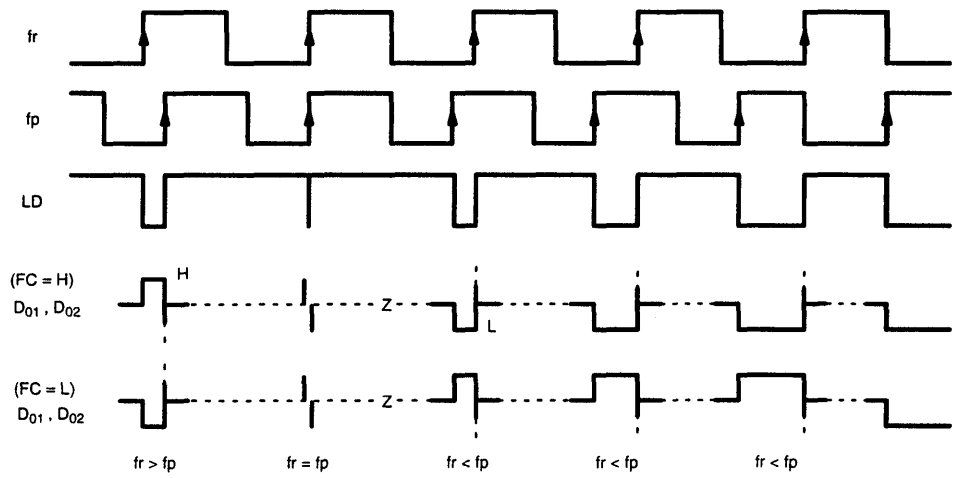
Depending upon the VCO polarity, the FC pin should be set accordingly.

When VCO polarity is like ①,
FC should be set high or open.
When VCO polarity is like ②,
FC should be set low.

VCO POLARITY



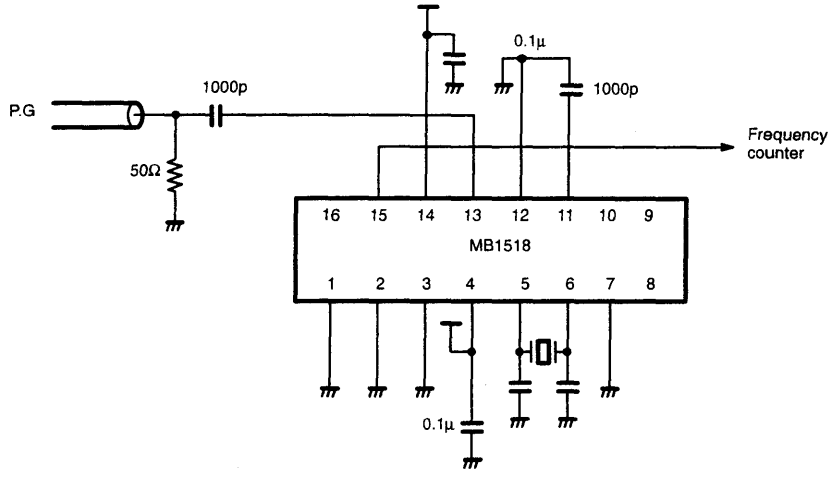
PHASE DETECTOR WAVEFORM



Note: Phase difference detection range : -2π to $+2\pi$

Spike shape depends on the charge pump characteristics.
The spike is output to diminish the dead band.

TEST CIRCUIT (FOR PRESCALER INPUT SENSITIVITY)



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_a	–40	–	+85	°C

HANDLING PRECAUTIONS

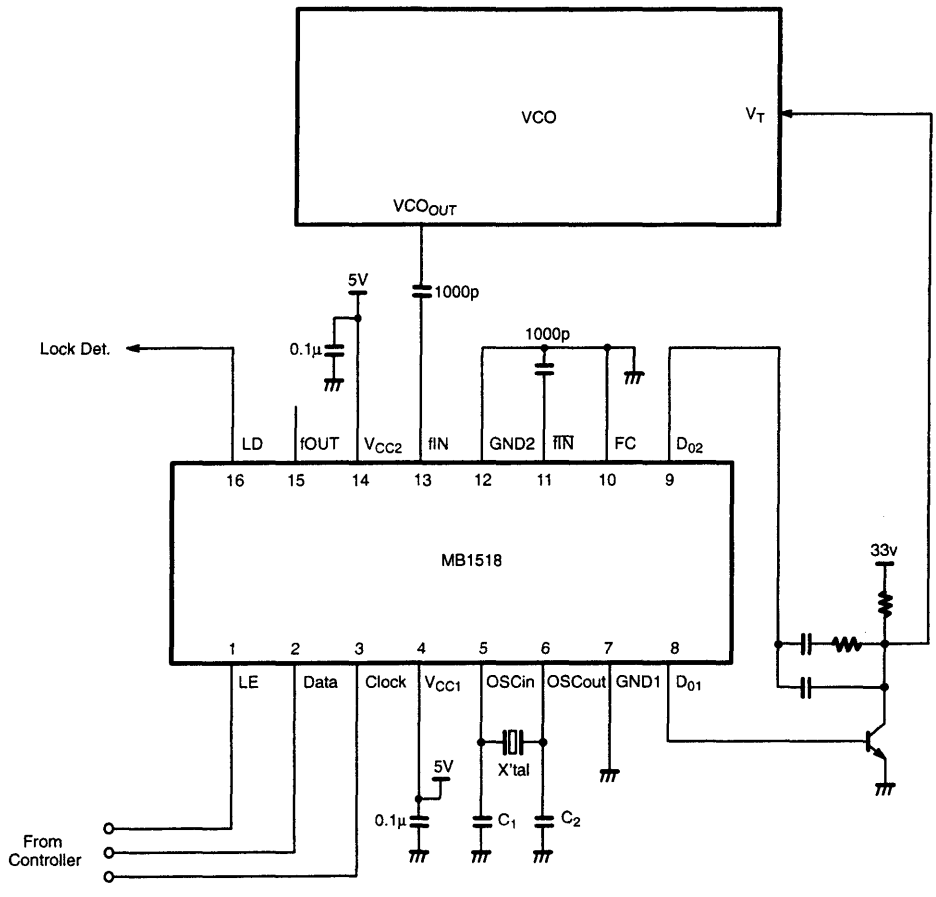
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note1	–	16.0	–	mA
Operating Frequency	f_{in}	f_{in}	Note2	10	–	2500	MHz
	OSC_{IN}	f_{OSC}	–	–	4	10	
Input Sensitivity	f_{in}	Pfin	2300 to 2500MHz	–4	–	6	dBm
			1900 to 2300MHz	–7	–	6	
			10 to 1900MHz	–10	–	6	
	OSC_{IN}	V_{OSC}	–	0.5	–	–	V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	–	V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}	–	–	–	V_{CC}x0.3–0.4	
High-level Input Current	Data, Clock, LE	I_{IH}	–	–	1.0	–	µA
Low-level Input Current		I_{IL}	–	–	–1.0	–	
	FC	I_{ILFC}	–	–	–60	–	
Input Current	OSC_{IN}	I_{IOSC}	–	–	±50	–	
High-level Output Voltage	Except D_O	V_{OH}	V_{CC} = 5.0V	4.4	–	–	V
Low-level Output Voltage		V_{OL}	–	–	–	0.4	
High-impedance Cutoff Current	D_{01},D_{02}	I_{OFF}	–	–	–	1.1	µA
High-level Output Current	Except D_O	I_{OH}	–	–1.0	–	–	mA
Low-level Output Current		I_{OL}	–	1.0	–	–	

Note1: f_{in}=2.5GHz, OSC_{IN}=4.0MHz, V_{cc}=5.0V. Input pins are grounded and output pins are open.
Note2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

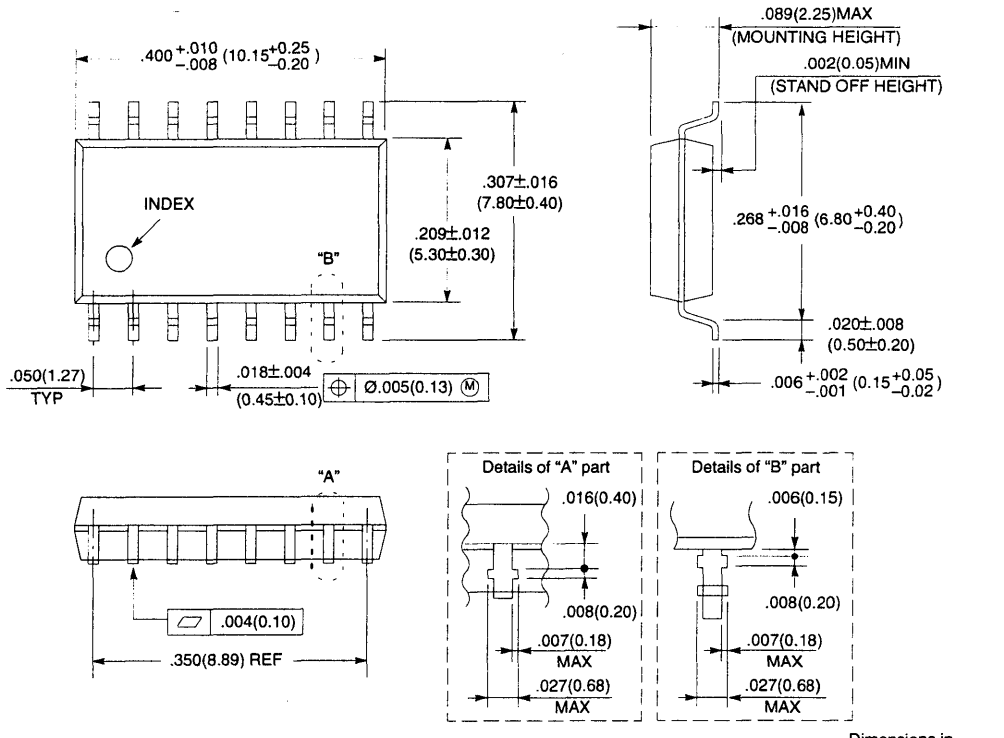
MB1518 APPLICATION CIRCUIT



C_1, C_2 : depends on the crystal oscillator
FC : with internal pull up resistor

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

September 1993
Edition 1.0

FUJITSU

DATA SHEET

MB15A19

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

4

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 600MHz PRESCALER

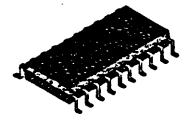
The Fujitsu MB15A19 is a 600MHz dual serial input PLL (Phase Locked) frequency synthesizer designed for cellular telephone and cordless telephone applications.

The MB15A19 has two PLL circuits on a single chip: one for transmit and the other for reception. Separate power supply pins are provided for the transmit and reception PLL circuits. Transmit PLL contains a low sensitivity charge pump for ease of modulation and reception PLL contains a high sensitivity charge pump for faster lock up time.

600 MHz dual modulus prescalers are on chip and enables a pulse swallow function.

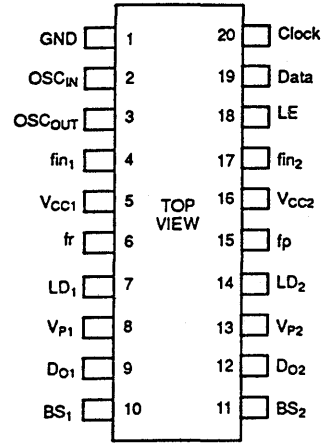
It operates supply voltage of 3.0V typ. and dissipates 11mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: fin = 600MHz
- Low power supply voltage: V_{CC} = 2.7 to 5.5V
- Low power supply current: I_{CC} = 11mA typ. @3V.
- Wide operating temperature: T_A = –40 to 85°C
- Two charge pumps
  Low sensitivity charge pump for transmit
  High sensitivity charge pump for reception
- Plastic 20-pin flat package (Suffix: -PF)



PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT



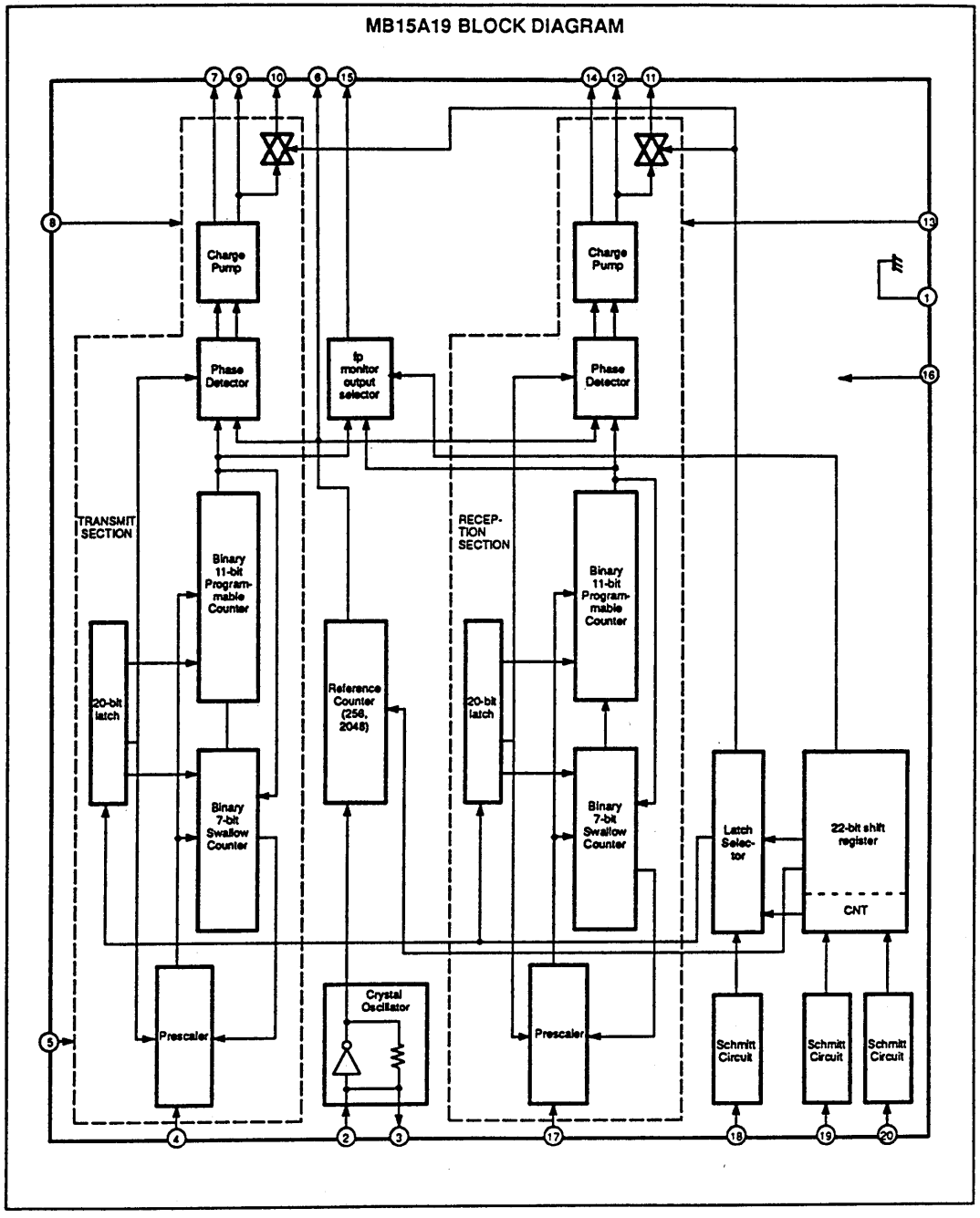
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
	V_P	V_{CC} to 10.0	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB15A19 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

TRANSMIT/RECEPTION BLOCK

- 20-bit latch
- Programmable divider consisting of:
  Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Phase detector with phase polarity change function
- 600MHz dual modulus prescaler (Divide ratio: 64/65)
- Charge pump

COMMON BLOCK

- 22-bit shift register
- Programmable divider consisting of:
  Reference counter (Divide ratio: 256, 2048)
  (Divide frequency = 50kHz, 6.25kHz (Crystal oscillator frequency = 12.8MHz)
- Crystal oscillator
- fp monitor output selector
- Latch selector
- Schmitt circuits
- Analog switches

PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSC_{IN}
OSC-
OUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.</td></tr>
<tr><td>4</td><td>fin_1</td><td>I</td><td>Prescaler input pin of transmit section.
The connection with VCO should be AC connection.</td></tr>
<tr><td>5</td><td>V_{CC1}</td><td>–</td><td>Power supply voltage input pin of transmit section.
When power is OFF, latched data of transmit section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output.</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of transmit section.
<table><tr><th>Condition</th><th>LD pin output level</th></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>8</td><td>V_{P1}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of transmit section.</td></tr>
<tr><td>9</td><td>D_{O1}</td><td>O</td><td>Charge pump output pin of transmit section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of transmit section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of reception section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>12</td><td>D_{O2}</td><td>O</td><td>Charge pump output pin of reception section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>V_{P2}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of reception section.</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detect signal output pin of reception section.
<table><tr><th>Condition</th><th>LD pin output level</th></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output.
This pin outputs divided frequency of transmit section or reception section depending upon FP bit setting.
<table><tr><th>FP bit</th><th>Output</th></tr><tr><td>H</td><td>Transmit section (fp1)</td></tr><tr><td>L</td><td>Reception section (fp2)</td></tr></table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	V_{CC2}	–	Power supply voltage input pin for reception section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of reception section and reference counter is cancelled.
17	fin_2	I	Prescaler input pin of reception section. The connection with VCO should be AC conneciton.
18	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data. At this moment, charge pump output signal is output from BS pin since internal analog swith becomes ON.
19	Data	I	Serial data input pin of 22-bit shift register. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either transmit section or reception section depending upon a control data. Control bit data: H → Latch of transmit section; L → Latch of reception section
20	Clock	I	Clock input pin of 22-bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of data into the shift register.

4

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)

M: Preset divide ratio of dual modulus prescaler (64)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillator frequency

R: Preset divide ratio of reference counter (256 or 2048)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins, Data pin, Clock pin, and LE pin. Programmable divider of transmit section and programmable divider of reception section are controlled individually.
Serial data of binary data is input into Data pin.
On rising edge of clock shifts one bit of serial data into the shift register. When load enable signal is high, the data stored in the shift register is transferred to either the latch of transmit section or the latch of reception section depending upon the control bit data setting.

Control data	Destination of serial data
H	Latch of transmit section
L	Latch of reception section

SHIFT REGISTER CONFIGURATION

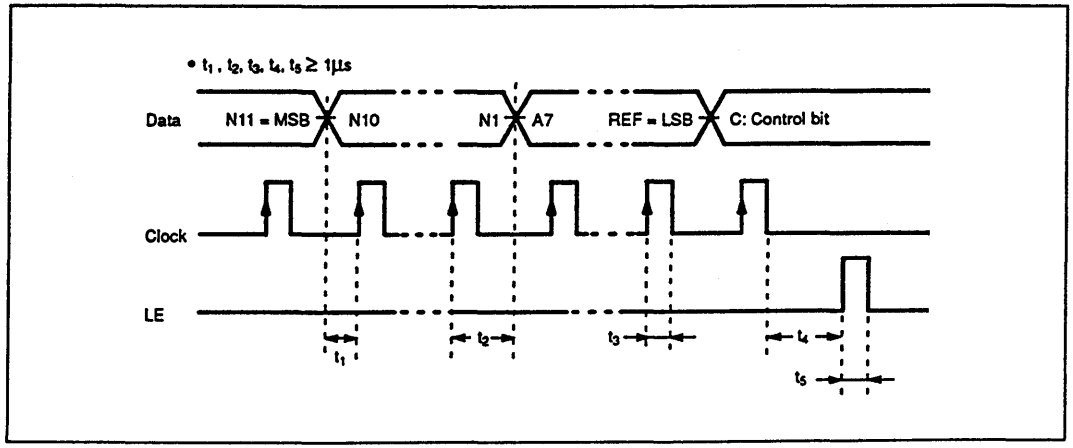
Control bit

LSB — Data Flow → — MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
CNT	REF	FP	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
FP : Output of the programmable divider control bit (fp1 or fp2)
REF : Divide ratio of the reference counter setting bit (256 to 2048)
CNT : Control bit

SERIAL DATA INPUT TIMING



On rising edge of the clock shifts one bit of the data into the shift register.

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 16 is prohibited.
Divide ratio (N) range = 16 to 2047

4

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

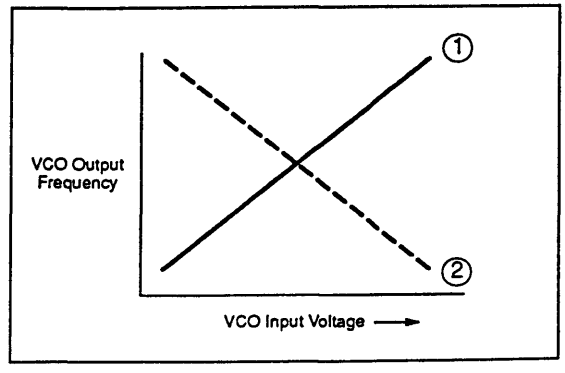
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H = 256 (fr = 50.0 kHz)
L = 2048 (fr = 6.25 kHz)

FP : OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable divider output frequency (fp1) of transmit section.
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of reception section.

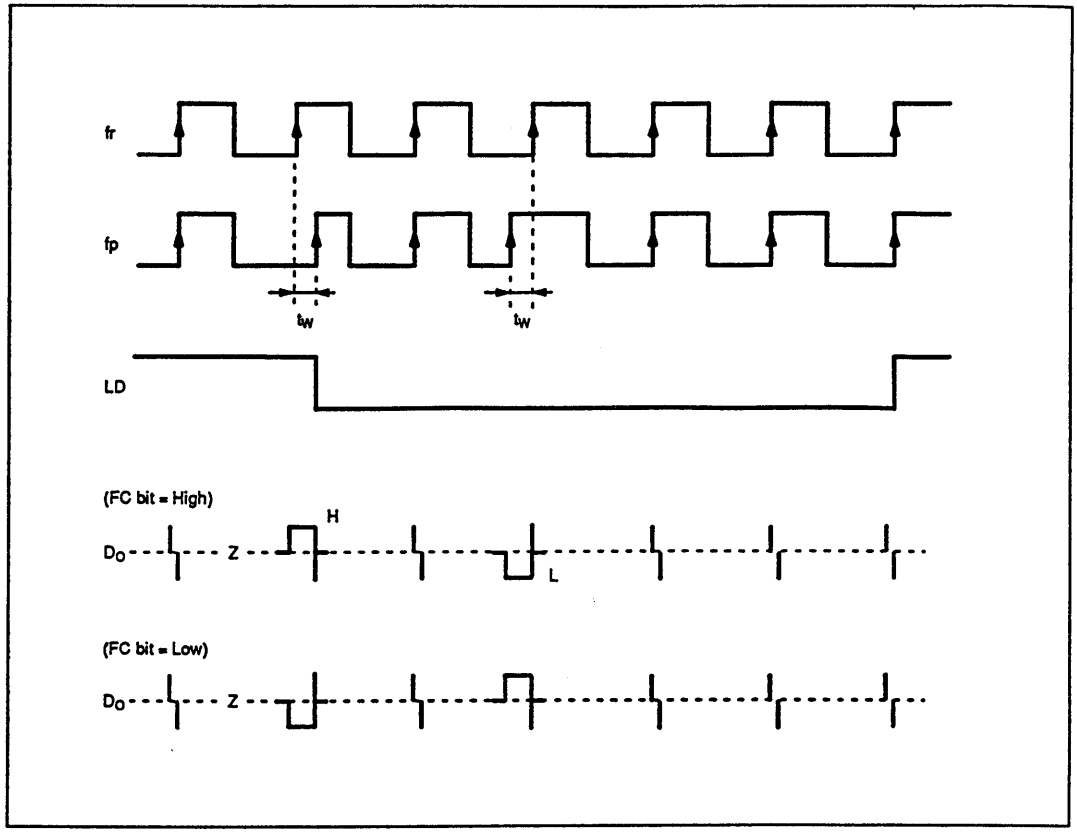
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin.

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: Z = High-impedance
Depending upon the VCO porality, FC bit should be set.



PHASE DETECTOR OUTPUT WAVEFORM



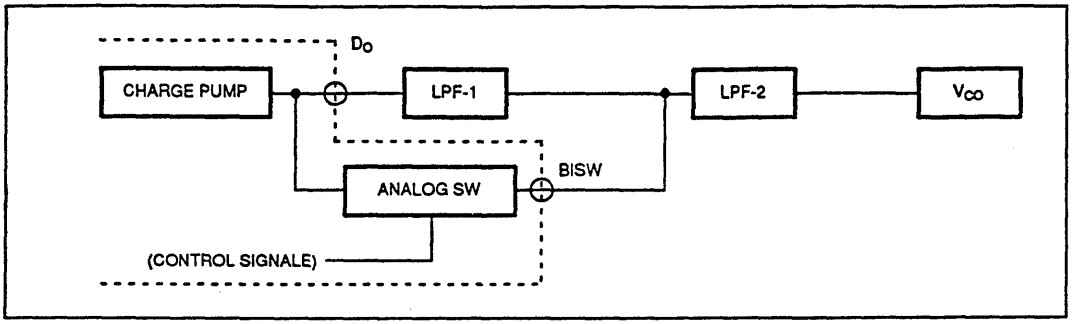
Note:
- Phase difference detection range = -2π to $+2\pi$
- LD output becomes low when phase difference is t_W or more.
  LD output becomes high when phase difference less than t_W is reperated 3 times or more.
  (e. g. t_W = 625 to 1250 ns, foscin = 12.8 MHz)
- Spike apperance depends on the charge pump characteristics. The spike is output to diminish the dead band.
- When fr > fp or fr < fp, spike might not generate depending up the VCO characteristics.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, BS1, BS2 pin output the charge pump output (D_{O1}, D_{O2}). When analog switch is OFF, BS pin is set to high impedance.

	Control data = H Divide ratio of transmit section is set		Control data = L Divide ratio of reception section is set	
	LE = H	LE = L	LE = H	LE = L
Analog switch of transmit section	ON	OFF	OFF	OFF
Analog switch of reception section	OFF	OFF	ON	OFF

When a analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
	V_P	V_{CC}	–	8.0	V	
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	T_A	−40	–	+85	°C	

HANDLING PRECAUTIONS

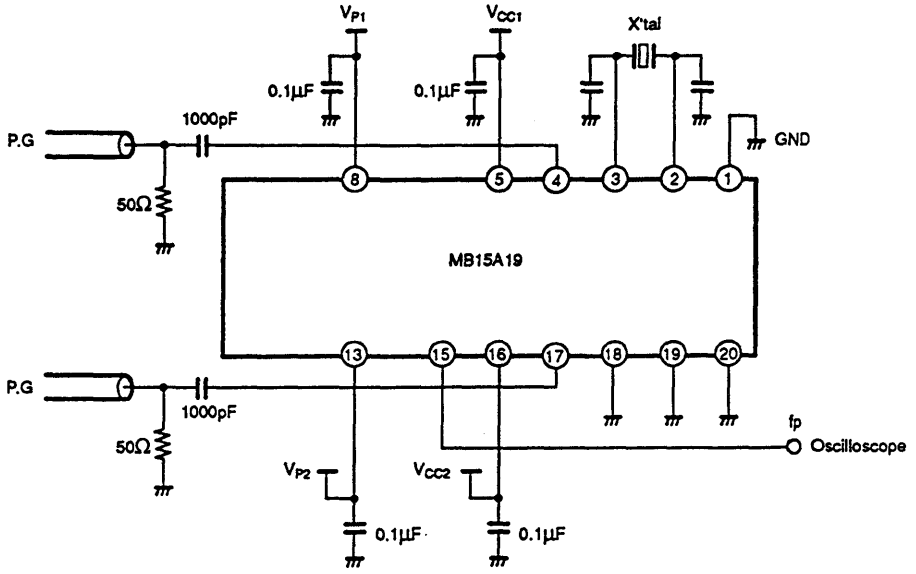
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

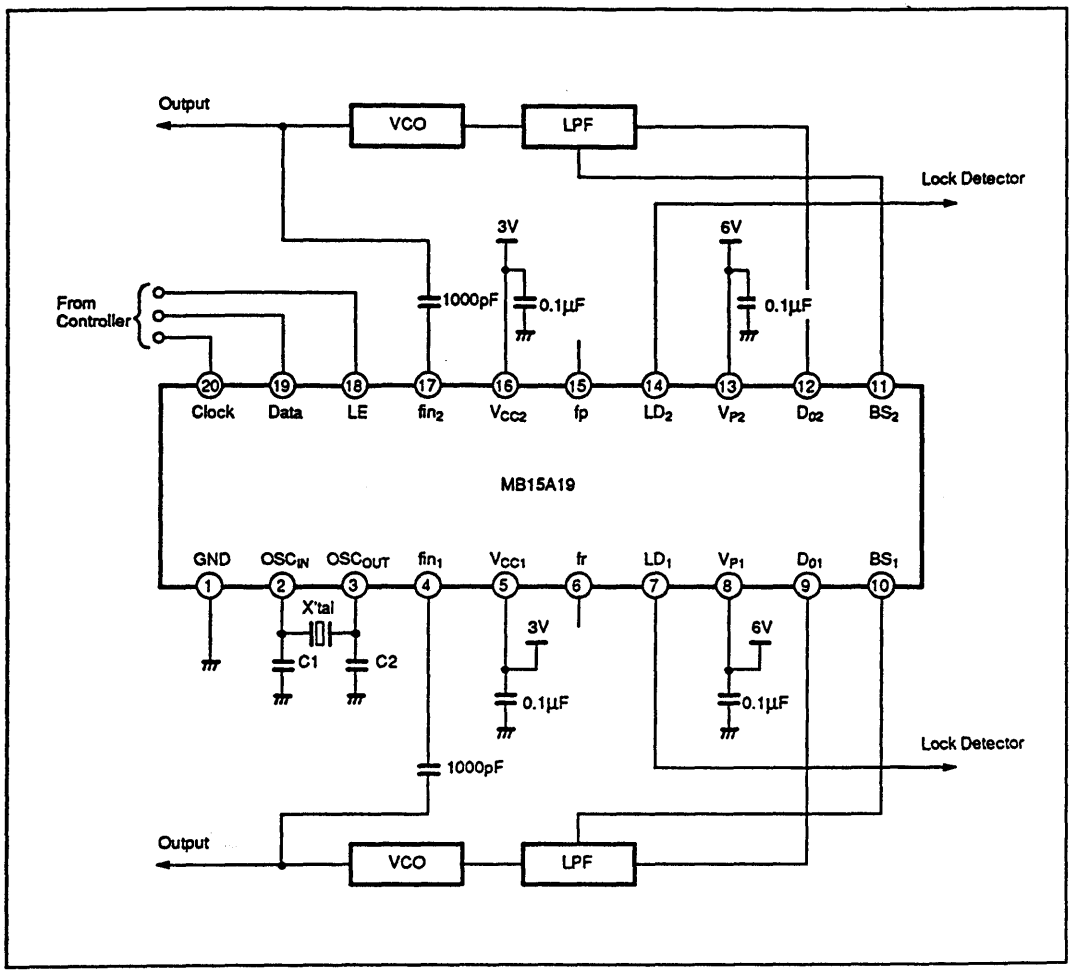
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current*		I_{CC1}	Reception section is active.	–	5.5	–	mA
		I_{CC2}	Transmit/reception section are active.	–	11.0	–	
Operating Frequency**	fin	fin		10	–	600	MHz
	OSC_{IN}	f_{OSC}		–	12.8	20	
Input Sensitivity	fin	P_{fIN}	V_{CC} = 2.7 to 4.0V, 50Ω	–8	–	0	dBm
			V_{CC} = 4.0 to 5.5V, 50Ω	–4	–	2	
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	μA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High-impedance Cutoff Current	D_O	I_{OFF}	V_P = V_{CC} to 8.0V	–	–	1.1	μA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	D_{O1}	I_{OH}	V_P = 6V	–	–1	–	
		I_{OL}	V_{CC} = 3V	–	12	–	
	D_{O2}	I_{OH}	V_P = 6V	–	–3	–	
		I_{OL}	V_{CC} = 3V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	25	–	Ω

Notes: *: fin = 600MHz, OSC_{IN} = 12.8MHz, V_{CC1} = V_{CC2} = 3.0V. The remaining input pins are grounded and output pins are open.
**: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



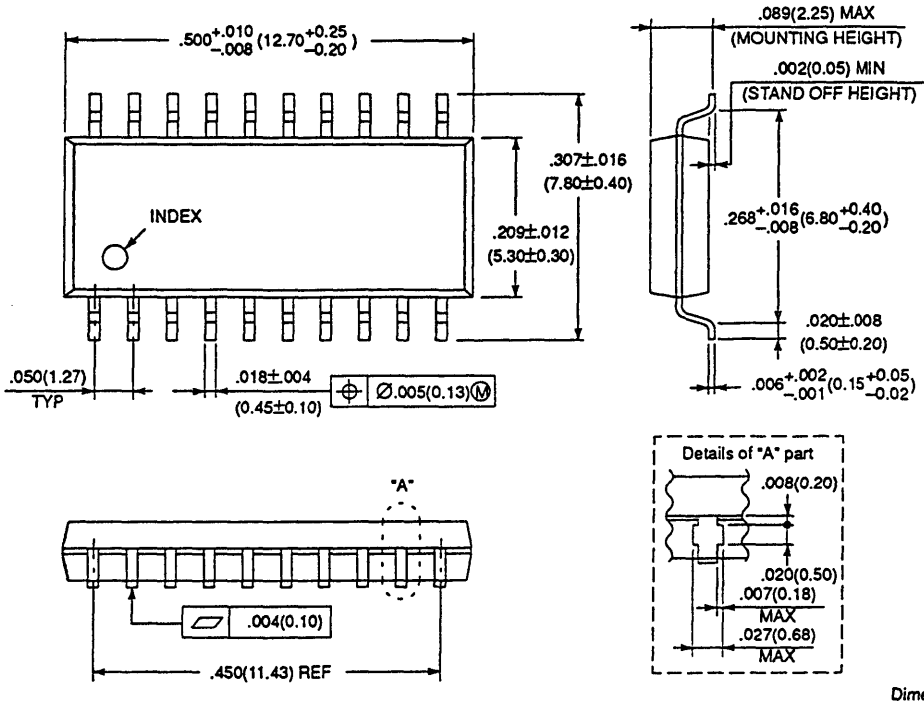
APPLICATION EXAMPLE



Note: V_{P1}, V_{P2} : 8 V max.
C1, C2 : depends on the crystal oscillator.
Clock, Data, LE : involve the schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent the oscillation.
X'tal : 12.8MHz

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



Dimensions in
inches (millimeters)

DS04–21314–1E

FUJITSU

DATA SHEET

MB1519 ASSP

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

4

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 600MHz PRESCALER

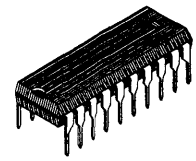
The Fujitsu MB1519 is a 600MHz dual serial input PLL (Phase Locked) frequency synthesizer designed for cellular telephone and cordless telephone applications.

The MB1519 has two PLL circuits on a single chip: one for transmit and the other for reception. Separate power supply pins are provided for the transmit and reception PLL circuits. Transmit PLL contains a low sensitivity charge pump for ease of modulation and reception PLL contains a high sensitivity charge pump for faster lock up time.

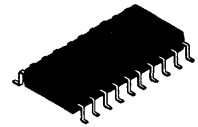
600 MHz dual modulus prescalers are on chip and enables a pulse swallow function.

It operates supply voltage of 3.0V typ. and dissipates 11mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: fin = 600MHz
- Low power supply voltage: V_{CC} = 2.7 to 5.5V
- Low power supply current: I_{CC} = 11mA typ, @3V.
- Wide operating temperature: T_A = –40 to 85°C
- Two charge pumps
  Low sensitivity charge pump for transmit
  High sensitivity charge pump for reception
- Plastic 20-pin dual in line package (Suffix: -P)
  Plastic 20-pin flat package (Suffix: -PF)

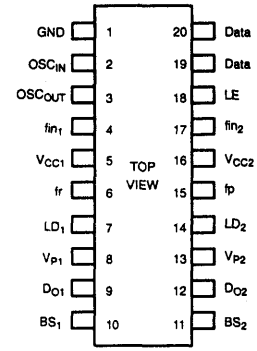


PLASTIC PACKAGE
DIP-20P-M02



PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT



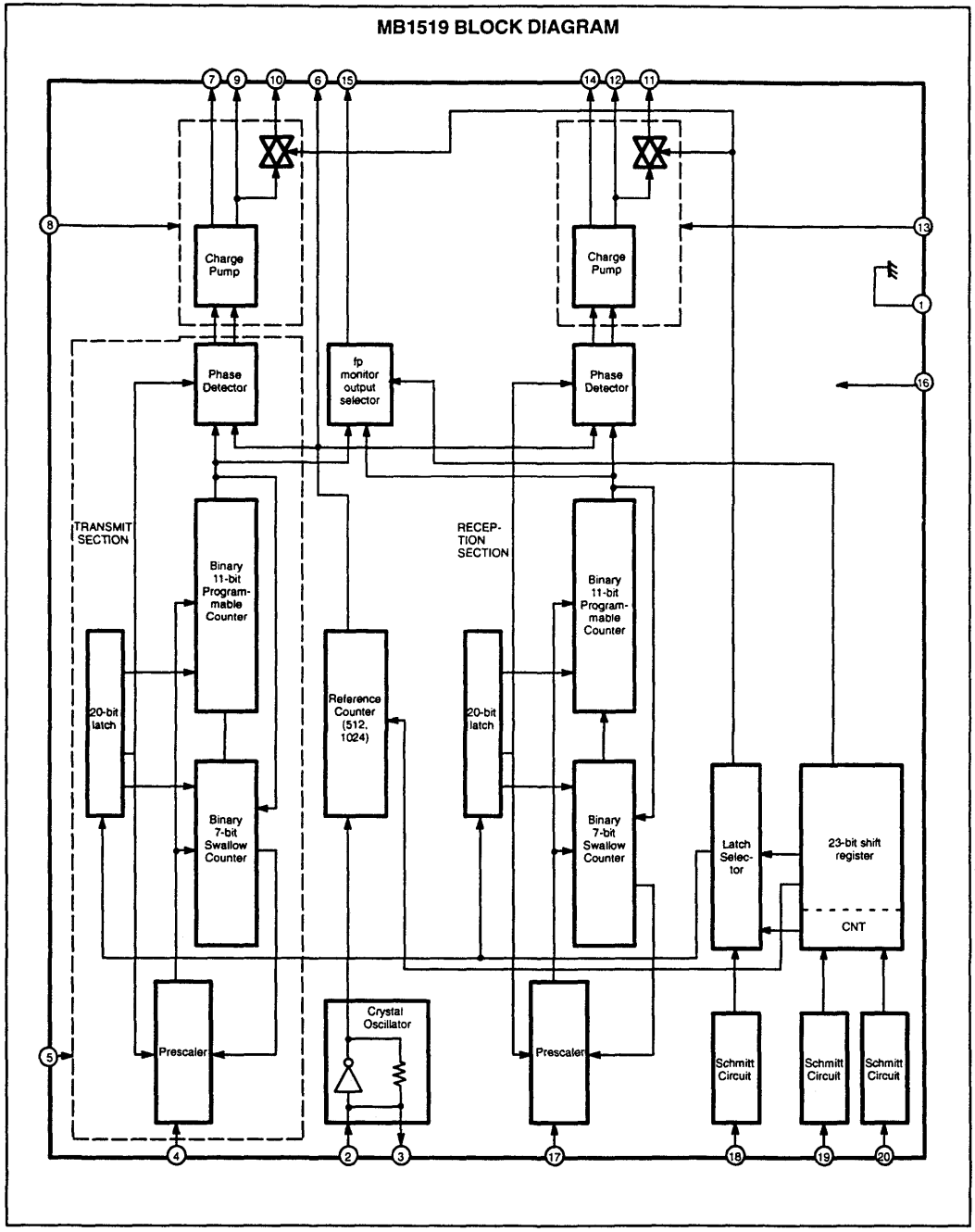
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
	V_P	V_{CC} to 10.0	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB1519 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

TRANSMIT/RECEPTION BLOCK

- 20-bit latch
- Programmable divider consisting of:
  Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Phase detector with phase polarity change function
- 600MHz dual modulus prescaler (Divide ratio: 64/65)
- Charge pump

COMMON BLOCK

- 23-bit shift register
- Programmable divider consisting of:
  Reference counter (Divide ratio: 512, 1024)
  (Divide frequency = 25kHz, 12.5kHz (Crystal oscillator frequency = 12.8MHz)
- Crystal oscillator
- fp monitor output selector
- Latch selector
- Schmitt circuits
- Analog switches

PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>-</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSC_{IN}
OSC-
OUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.</td></tr>
<tr><td>4</td><td>fin_1</td><td>I</td><td>Prescaler input pin of transmit section.
The connection with VCO should be AC connection.</td></tr>
<tr><td>5</td><td>V_{CC1}</td><td>-</td><td>Power supply voltage input pin of transmit section.
When power is OFF, latched data of transmit section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output.</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of transmit section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>V_{P1}</td><td>-</td><td>Power supply voltage input for charge pump and analog switch of transmit section.</td></tr>
<tr><td>9</td><td>D_{O1}</td><td>O</td><td>Charge pump output pin of transmit section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of transmit section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of reception section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>12</td><td>D_{O2}</td><td>O</td><td>Charge pump output pin of reception section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>V_{P2}</td><td>-</td><td>Power supply voltage input for charge pump and analog switch of reception section.</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detect signal output pin of reception section.
<table>
<tr><th>Condition</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output.
This pin outputs divided frequency of transmit section or reception section depending upon FP bit setting.
<table>
<tr><th>FP bit</th><th>Output</th></tr>
<tr><td>H</td><td>Transmit section (fp1)</td></tr>
<tr><td>L</td><td>Reception section (fp2)</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	V_{CC2}	-	Power supply voltage input pin for reception section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of reception section and reference counter is cancelled.
17	fin_2	I	Prescaler input pin of reception section. The connection with VCO should be AC conneciton.
18	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data. At this moment, charge pump output signal is output from BS pin since internal analog swith becomes ON.
19	Data	I	Serial data input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either transmit section or reception section depending upon a control data. Control bit data: H → Latch of transmit section; L → Latch of reception section
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of data into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)

M: Preset divide ratio of dual modulus prescaler (64)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillator frequency

R: Preset divide ratio of reference counter (512 or 1024)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins, Data pin, Clock pin, and LE pin. Programmable divider of transmit section and programmable divider of reception section are controlled individually.
Serial data of binary data is input into Data pin.
On rising edge of clock shifts one bit of serial data into the shift register. When load enable signal is high, the data stored in the shift register is transferred to either the latch of transmit section or the latch of reception section depending upon the control bit data setting.

Control data	Destination of serial data
H	Latch of transmit section
L	Latch of reception section

SHIFT REGISTER CONFIGURATION

Control bit

LSB

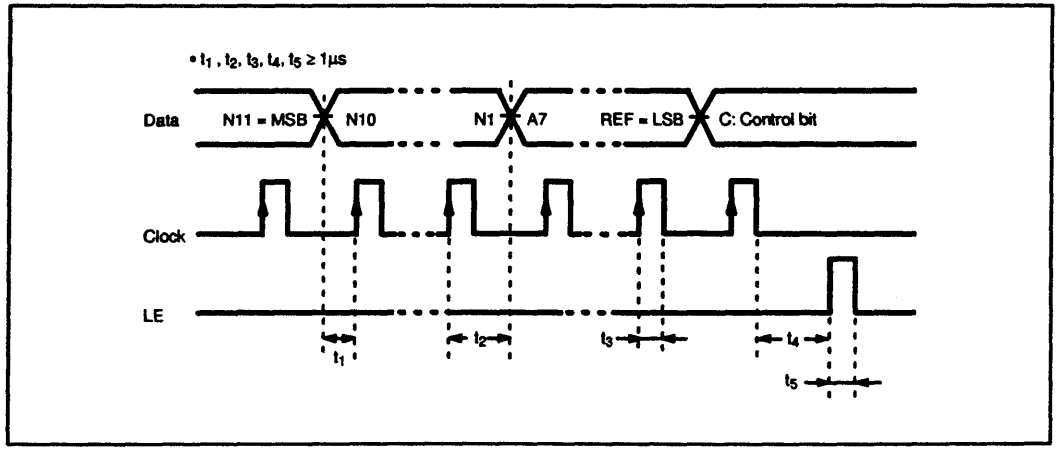
Data Flow →

MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CNT	REF	FP	DMY	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
DMY : Dummy bit (sets to low)
FP : Output of the programmable divider control bit (fp1 or fp2)
REF : Divide ratio of the reference counter setting bit (512 to 1024)
CNT : Control bit

SERIAL DATA INPUT TIMING



On rising edge of the clock shifts one bit of the data into the shift register.

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 16 is prohibited.
Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

DMY : DUMMY BIT INPUT
This bit is set to low in operation.

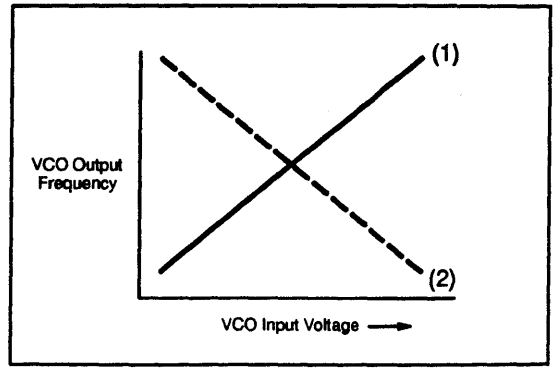
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H = 512 (fr = 25.0 kHz)
L = 1024 (fr = 12.5 kHz)

FP : OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable divider output frequency (fp1) of transmit section.
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of reception section.

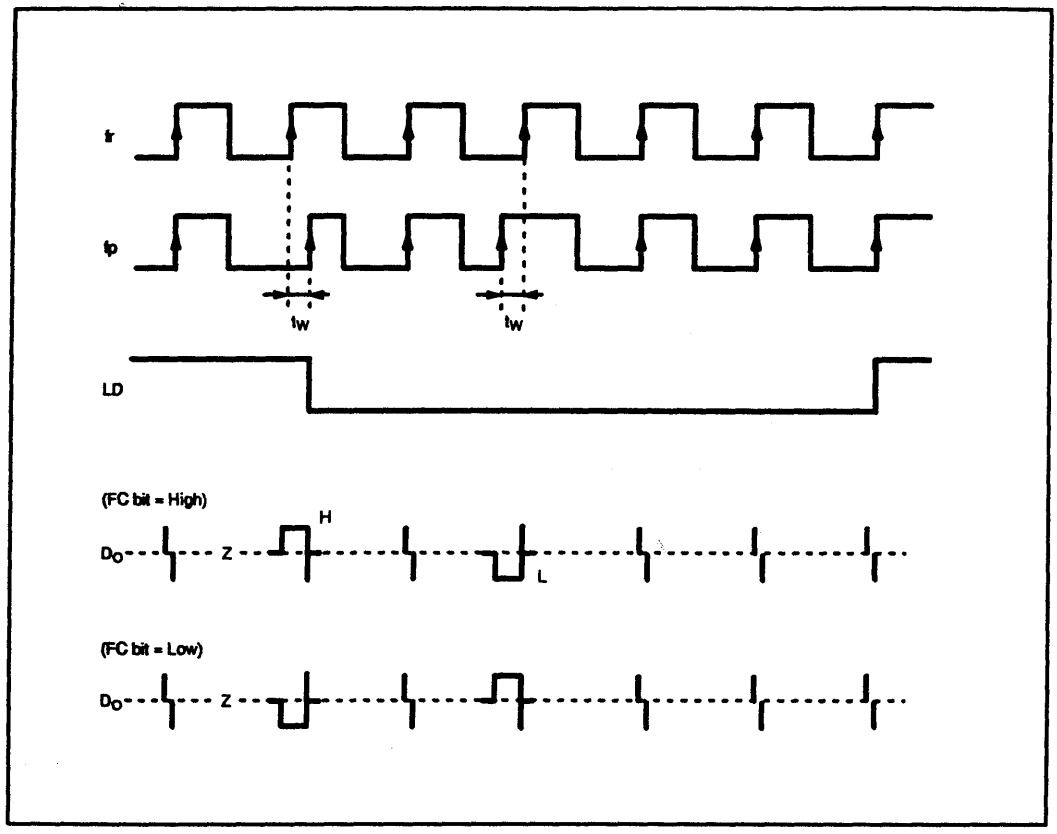
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin.

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	(1)	(2)

Note: Z = High-impedance
Depending upon the VCO porality, FC bit should be set.



PHASE DETECTOR OUTPUT WAVEFORM



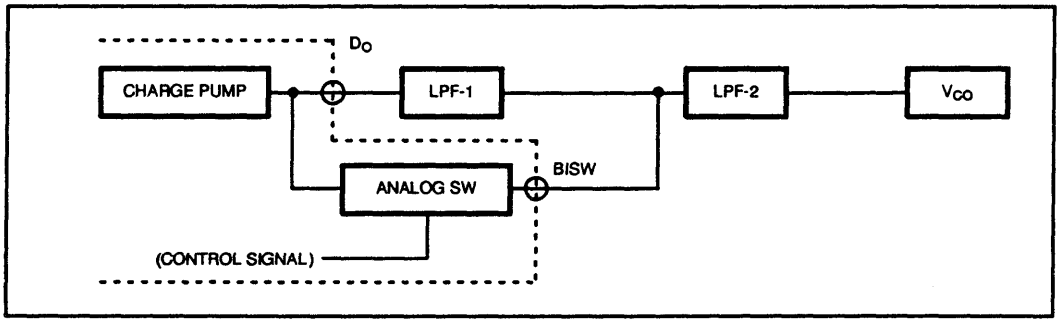
Note:
- Phase difference detection range = -2π to $+2\pi$
- LD output becomes low when phase difference is t_W or more.
  LD output becomes high when phase difference less than t_W is reperated 3 times or more.
  (e. g. t_W = 625 to 1250 ns, foscin = 12.8 MHz)
- Spike apperance depends on the charge pump characteristics. The spike is output to diminish the dead band.
- When fr > fp or fr < fp, spike might not generate depending up the VCO characteristics.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, BS1, BS2 pin output the charge pump output (D_{O1}, D_{O2}). When analog switch is OFF, BS pin is set to high impedance.

	Control data = H Divide ratio of transmit section is set		Control data = L Divide ratio of reception section is set	
	LE = H	LE = L	LE = H	LE = L
Analog switch of transmit section	ON	OFF	OFF	OFF
Analog switch of reception section	OFF	OFF	ON	OFF

When a analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
	V_P	V_{CC}	-	8.0	V	
Input Voltage	V_{IN}	GND	-	V_{CC}	V	
Operating Temperature	T_A	-40	-	+85	°C	

HANDLING PRECAUTIONS

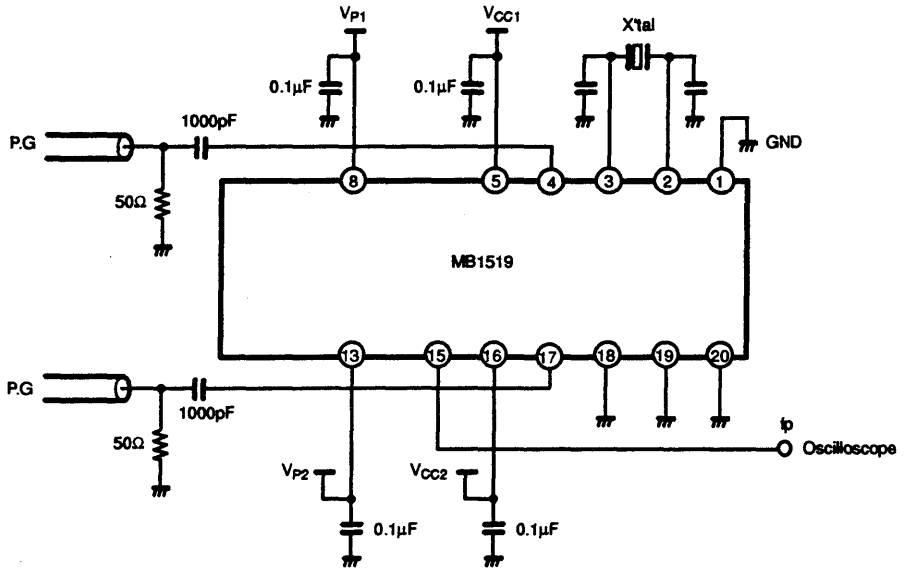
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

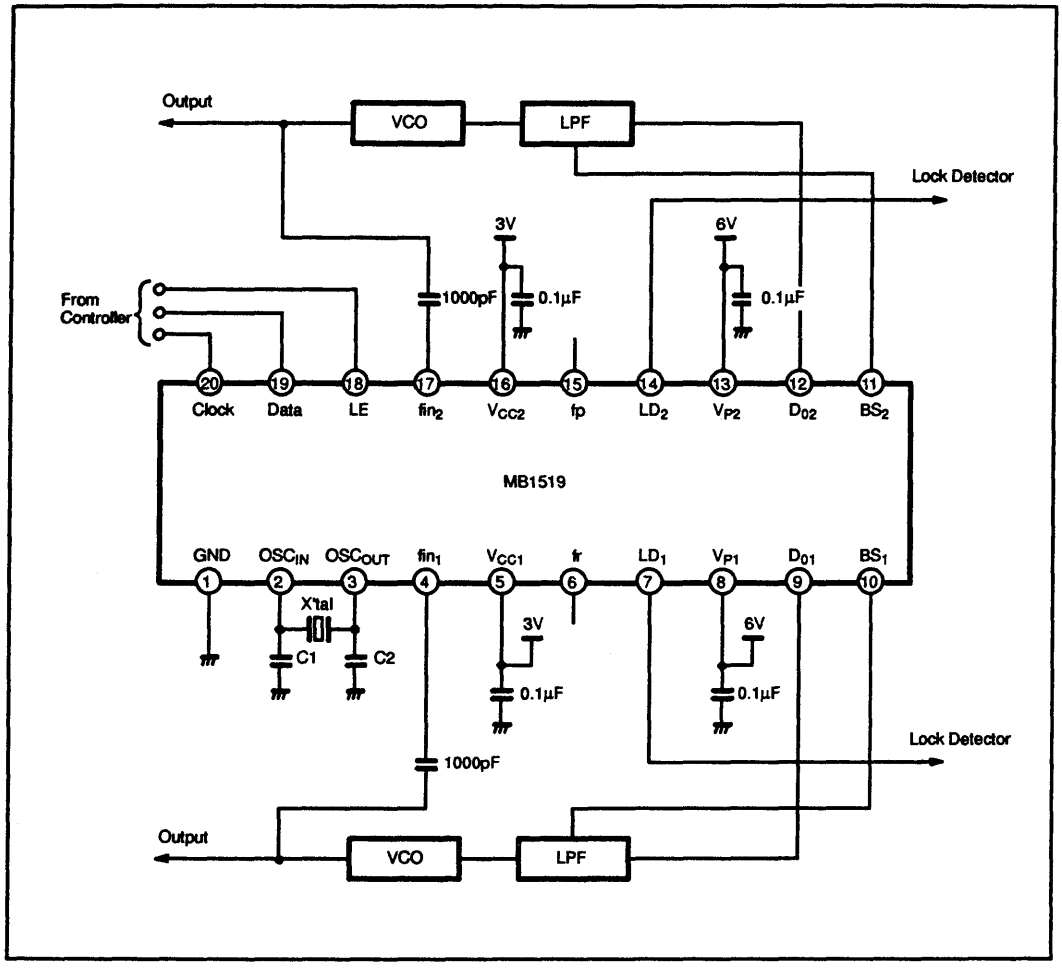
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current*		I_{CC1}	Reception section is active.	–	5.5	8.0	mA
		I_{CC2}	Transmit/reception section are active.	–	11.0	16.0	
Operating Frequency**	fin	fin		10	–	600	MHz
	OSC_{IN}	f_{OSC}		–	12.8	20	
Input Sensitivity	fin	P_{fIN}	V_{CC} = 2.7 to 4.0V, 50Ω	–8	–	0	dBm
			V_{CC} = 4.0 to 5.5V, 50Ω	–4	–	4	
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High-impedance Cutoff Current	D_O	I_{OFF}	V_P = V_{CC} to 8.0V V_{OOP} = GND to 8.0V	–	–	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	D_{O1}	I_{OH}	V_P = 6V	–	–1	–	
		I_{OL}	V_{CC} = 3V	–	12	–	
	D_{O2}	I_{OH}	V_P = 6V	–	–3	–	
		I_{OL}	V_{CC} = 3V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	25	–	Ω

Notes: *: fin = 600MHz, OSC_{IN} = 12.8MHz, V_{CC1} = V_{CC2} = 3.0V. The remaining input pins are grounded and output pins are open.
**: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



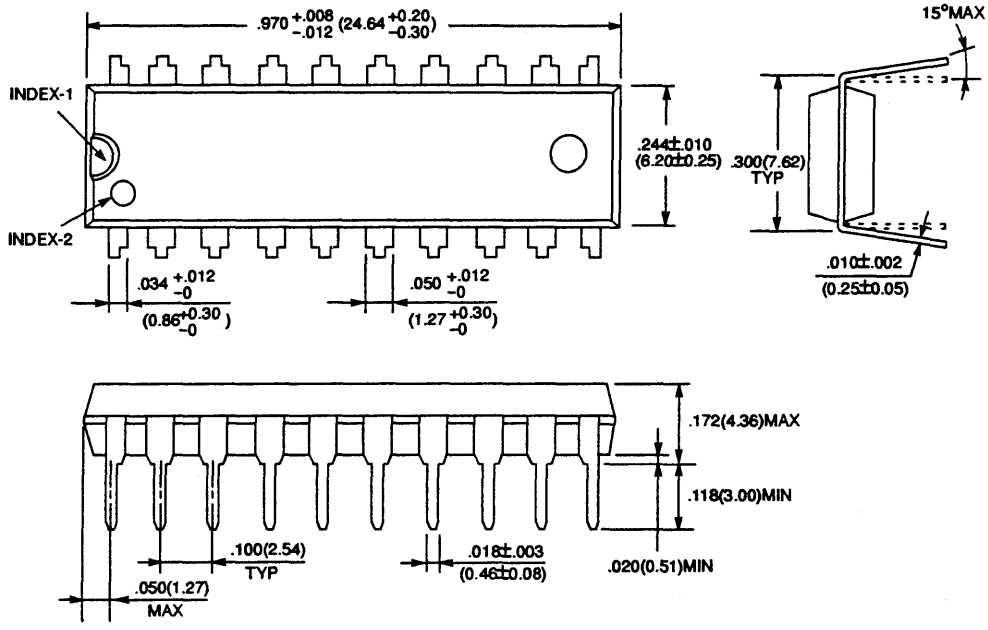
APPLICATION EXAMPLE



Note: V_{P1}, V_{P2} : 8 V max.
C1, C2 : depends on the crystal oscillator.
Clock, Data, LE : involve the schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent the oscillation.
X'tal : 12.8MHz

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)

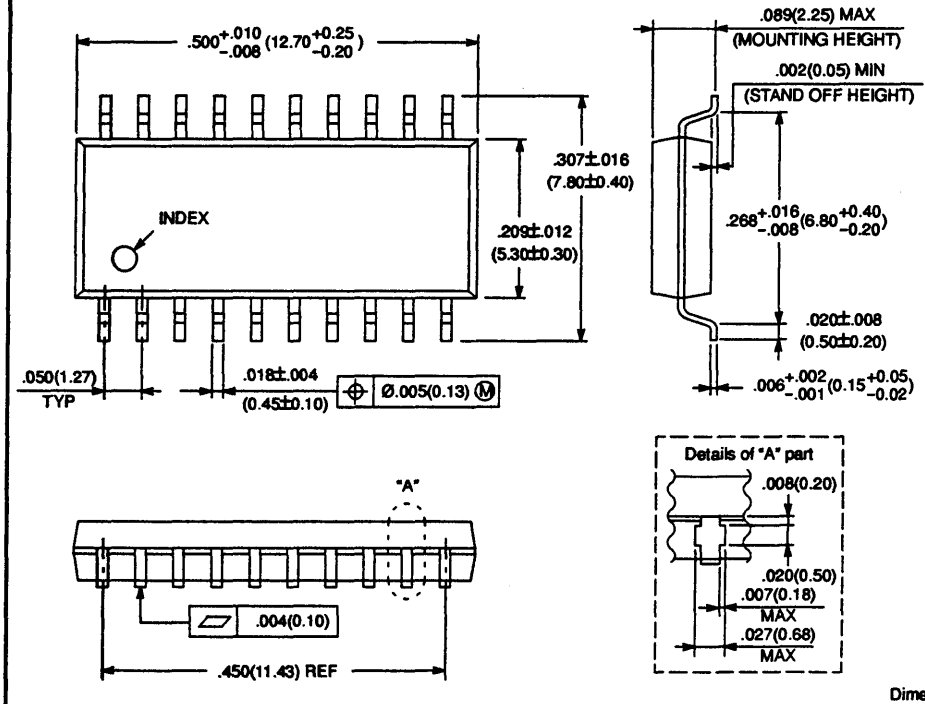


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



Dimensions in
inches (millimeters)

Sept. 1995
Edition 0.1a

FUJITSU

MB15S series — Product Profile Sheet

IF BAND PLL FREQUENCY SYNTHESIZER

Small package and IF band MASK ROM PLL (SIMPLL Series)

The Fujitsu MB15S series is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. It can operate at a maximum of 300MHz.

The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a μcontroller externally. Since the dividers are designed by means of a MASK ROM method, a customer can choose them optionally. SOP and SSOP 8–pin plastic packages are available.

4

It operates with a supply voltage of 3.0V typ. and dissipates 3.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology.

FEATURES

- Operating frequency : 300MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. (Vcc = 3V)
- Pulse swallow function;
  300MHz Prescaler: 16/17 or 32/33
- MASK ROM optional the comparison and reference dividers:
  – Main counter ; 5 to 4095
  – Swallow counter ; 0 to 31
  – Reference counter ; 5 to 4095
- Charge pump options:
  – Analog cellular phones ; Low sensitivity charge pump for direct modulation.
  – Digital cellular phones ; Super charger circuit for High speed tuning.
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- Wide operating temperature: T_A = –40 to 85°C
- Plastic 8-pin SOP and 8–pin SSOP packages

SOP–8P–M01

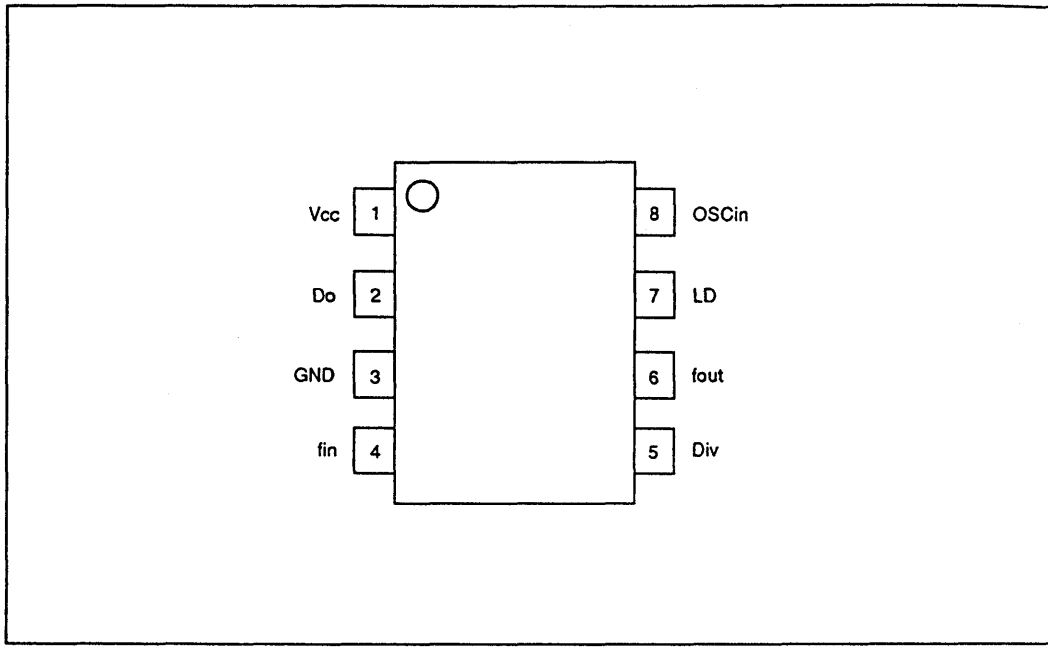
SOP–8P–M03

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 5.0	V
Input voltage	V_I	–0.5 to V_{CC} + 0.5	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	0 to 5	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

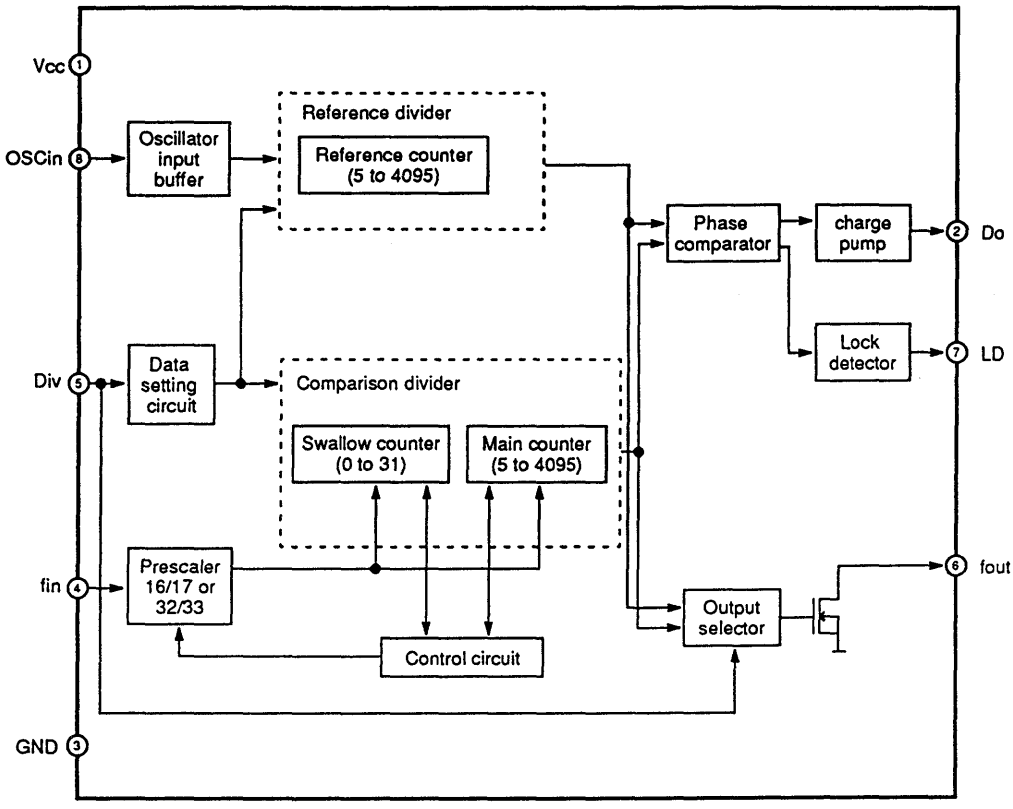
PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin No.	Pin Name	Descriptions
1	Vcc	Power supply voltage input.
2	Do	Charge pump output
3	GND	Ground
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L".
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

Divide ratios of the internal counters can be set optionally according to customer requirements. Two different frequencies can be selected by Div input "H" or "L".
The divide ratio can be calculated using the following equation:

$fvco = \{(P \times N) + A\} \times fosc \div R \quad (A < N)$

fvco: Output frequency of external voltage controlled ocillator (VCO: up to 300MHz)

P: Preset divide ratio of dual modulus prescaler (16/17 or 32/33)

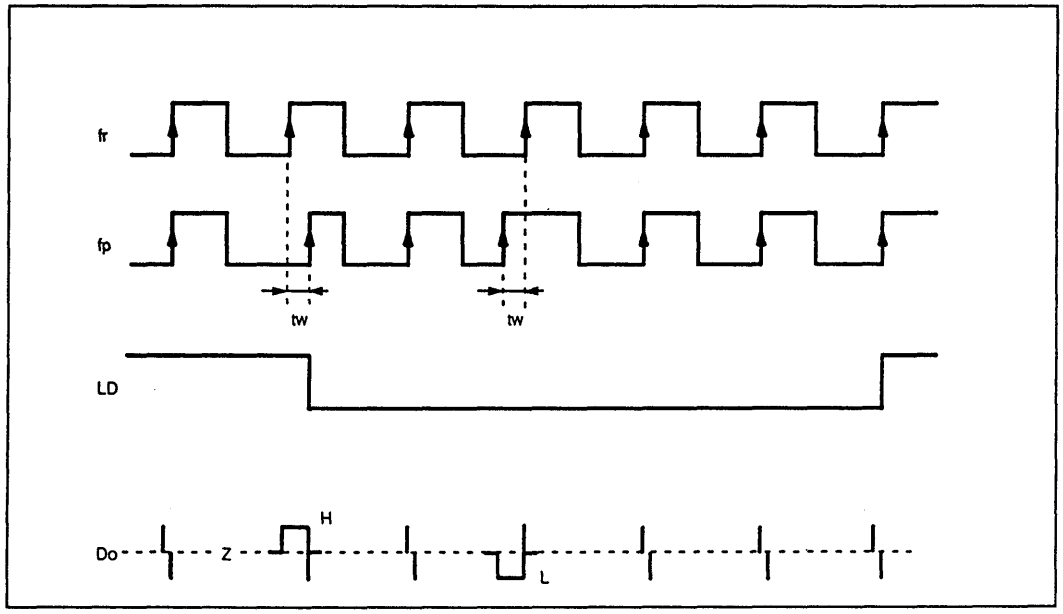
N: Divide ratio of the main counter (5 to 4095)

A: Divide ratio of the swallow counter (0 to 31)

fosc: Reference oscillation frequency (up to 23MHz)

R: Divide ratio of the reference counter (5 to 4095)

PHASE DETECTOR TIME CHART



Note:
- Phase difference detection range = -2π to $+2\pi$
- Spikes on Do pulse during locking state are output to prevent dead zone.
- LD output becomes low when phase difference is tw or more.
- LD output becomes high when phase difference is tw or less and continues to be so for three cysles or more.
- tw depends on OSCin input frequency.
  (e.g. tW635ns to 1250ns when foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	T_A	–40	–	+85	°C	

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

4

ELECTRICAL CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply current	I_{CC}	PLL is locked. Vcc = 3.0V, Ta = 25°C	–	3.5	5.0	mA
Operating frequency	fin	AC coupling by 1000pF capacitor	10	–	300	MHz
Oscillator input frequency	fosc	AC coupling by 1000pF capacitor	–	12	23	MHz
Input sensitivity	Pin	AC coupling by 1000pF capacitor	–10	–	+2	dBm
Oscillator input sensivity	VOSCin	AC coupling by 1000pF capacitor	0.5	–	–	Vpp
Input voltage (Div)	V_{IH}		Vcc x 0.7	–	–	V
	V_{IL}		–	–	Vcc x 0.3	V
Input current (Div)	I_{IH}		–	–	1.0	µA
	I_{IL}		–1.0	–	–	µA
Input current (OSCin)	Iosc		–100		100	µA
Output voltage	V_{OH}	Vcc = 3.0V	2.6	–	–	V
	V_{OL}	Vcc = 3.0V	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	VDo≦ 3.3V	–	–	1.1	µA

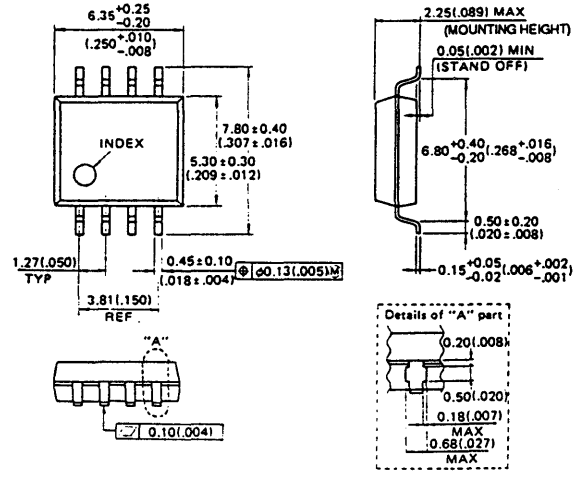
CUSTOMER REQUESTING SPECIFICATIONS

Parameter			Option	Requirements
fvco		VCO output frequency	~ 300MHz fvco = {(P x N) + A} x fr	
fosc		Reference oscillation frequency	~ 23MHz fosc = R x fr	
Comparison divider	N	Main counter divide ratio	5 to 4095	
	A	Swallow counte divide ratio	0 to 31	
Reference divider	R	Reference counter divide ratio	5 to 4095	
	fr	Reference frequency	Option	
P		Prescaler divide ratio	16/17 or 32/33	
Charge pump type			Low sensitivity type or super charger	
Package			SSOP 8–pin or SOP 8–pin	
ES request date/qty.			Typically 6 weeks from spec. fix to the first ES.	
CS request date/qty.			–	
MP request date/qty.			–	
Target price			–	

Customer comments

PACKAGE DIMENTIONS

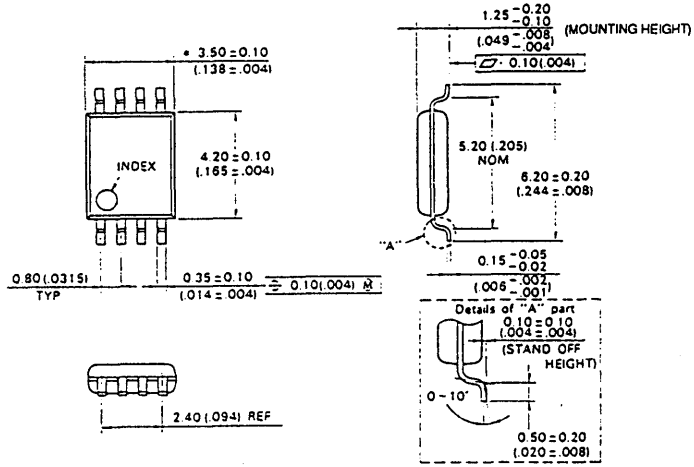
8–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–8P–M01)



Dimensions in millimeters (inches)

8–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–8P–M03)

*: This dimension does not include resin protrusion.



Dimensions in millimeters (inches)

March 1995
Edition 0.1

FUJITSU

MB15S02 Product Profile Sheet

IF BAND PLL FREQUENCY SYNTHESIZER

Small package and IF band MASK ROM PLL (SIMPLL Series)

The Fujitsu MB15S02 is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a microcontroller externally.

It operates with a supply voltage of 3.0V typ. and dissipates 3.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology.

The RF synthesizer block of a digital cellular phone can be easily realized with an MB15S02 and MB1516A (1.1 GHz PLL, SSOP-16), both designed with GSM systems in mind.

4

FEATURES

- Prescaler operating frequency : 300MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. (Vcc = 3V)
- Pulse swallow function; Prescaler: 16/17
- Setting frequency (Selectable by Div input.)
  – fosc = 13.0MHz, fIF = 284.0MHz (Div = "H")
  – fosc = 13.0MHz, fIF = 116.0MHz (Div = "L")
- Rapid synchronization at powering up
  Fujitsu's original charge pump "super charger circuit" is included, that enables rapid synchronization at powering up.
- Lock detector
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- Wide operating temperature: T_A = –40 to 85°C
- Plastic 8–pin SSOP packages

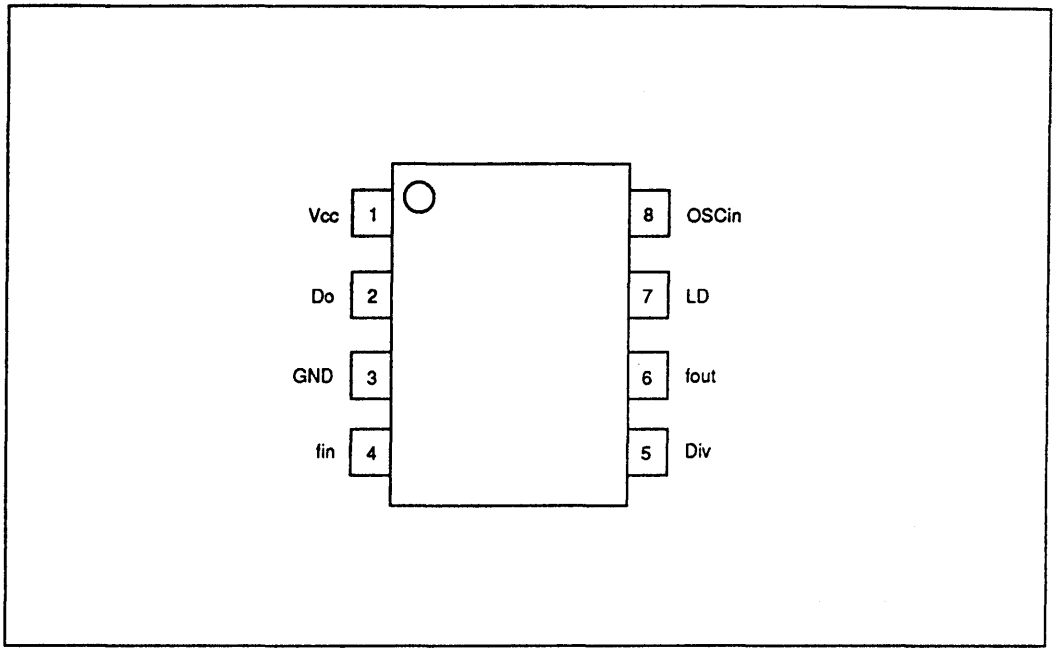
SOP–8P–M03

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 5.0	V
Input Voltage	V_I	–0.5 to V_{CC} + 0.5	V
Output Voltage	V_{OUT}	–0.5 to Vcc +0.5	V
Output Current	I_{OUT}	0 to 5	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

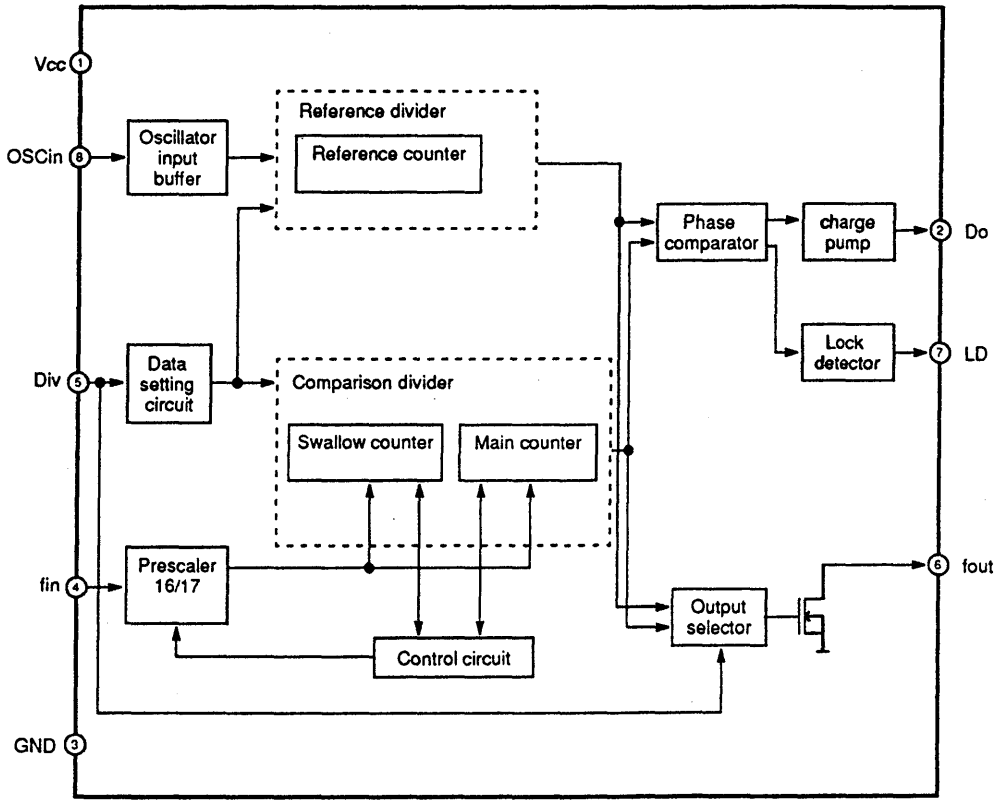
PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin No.	Pin Name	Descriptions
1	Vcc	Power supply voltage input (2.7V to 3.5V).
2	Do	Charge pump output
3	GND	Ground
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L".
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

BLOCK DIAGRAM



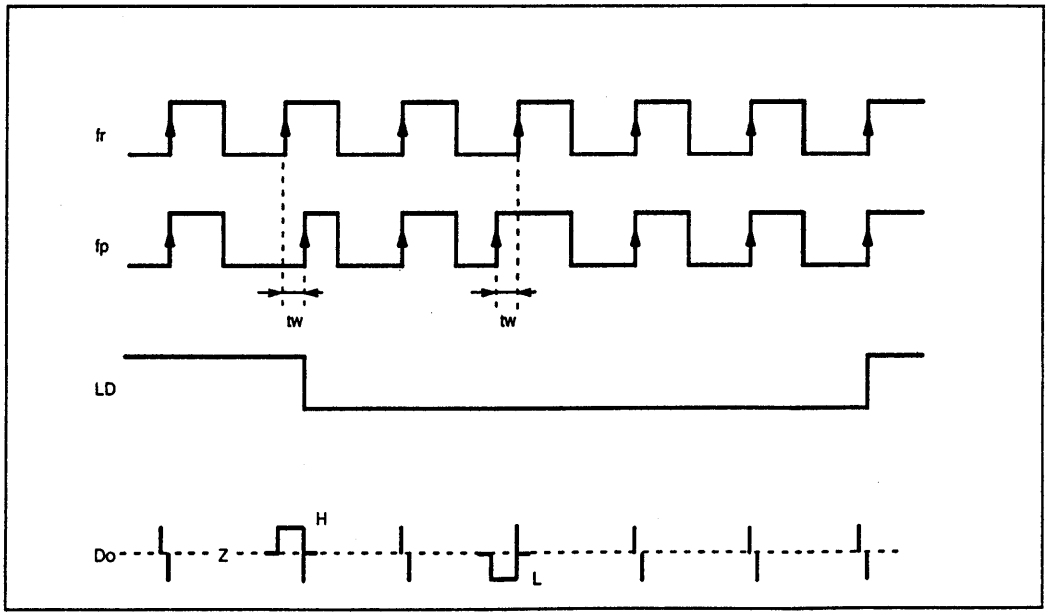
FUNCTIONAL DESCRIPTIONS

Two different frequencies can be selected by Div input "H" or "L".
The divide ratios are calculated using the following equation:

fvco = {(P x N) + A} x fosc ÷ R (A < N)

Symbol	Description	Div = "H"	Div = "L"
fvco	Output frequency of external VCO	284.0 MHz	116.00 MHz
fosc	Reference oscillation frequency	13.0 MHz	13.0 MHz
N	Divide ratio of the main counter	17	7
A	Divide ratio of the swallow counter	12	4
P	Preset divide ratio of dual modulus prescaler	16/17	16/17
R	Divide ratio of the reference counter	13 (fr = 1 MHz)	13 (fr = 1 MHz)

PHASE DETECTOR TIME CHART



Note:
- Phase difference detection range = −2π to +2π
- Spikes on Do pulse during locking state are output to prevent dead zone.
- LD output becomes low when phase difference is tw or more.
- LD output becomes high when phase difference is tw or less and continues to be so for three cycles or more.
- tw depends on OSCin input frequency.
  (e.g. tW635ns to 1250ns when foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	Vcc	2.7	3.0	3.5	V	
Input Voltage	V_{IN}	GND	–	Vcc	V	
Operating Temperature	T_A	–40	–	+85	°C	

HANDLING PRECAUTIONS

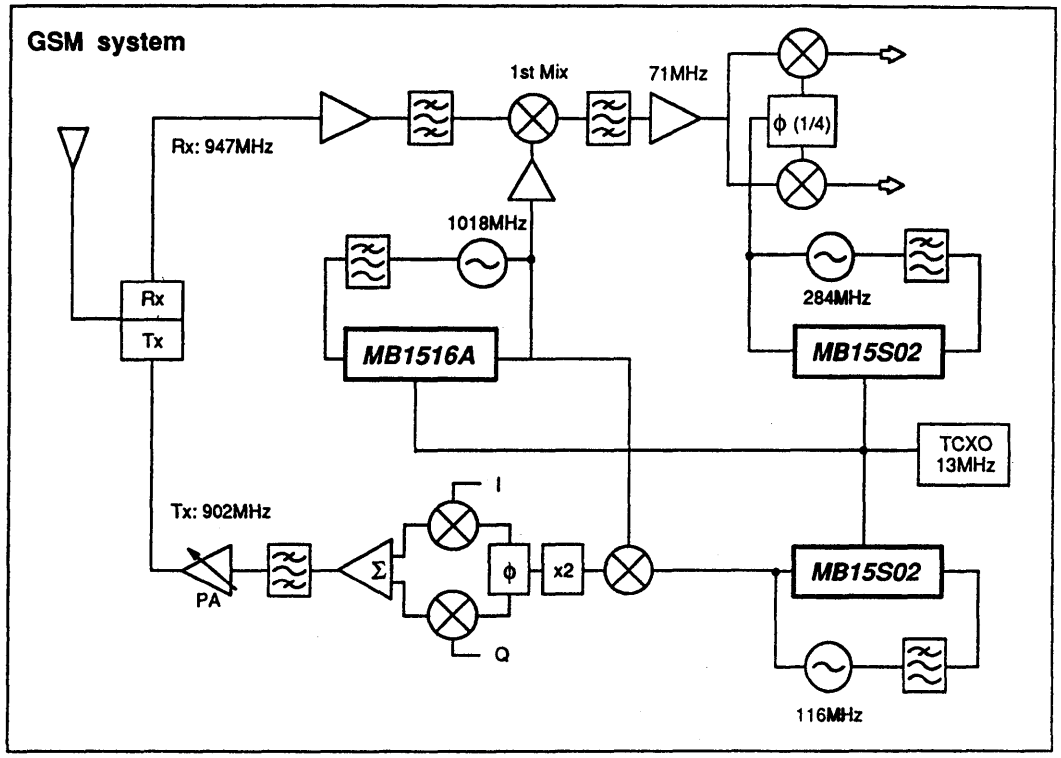
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

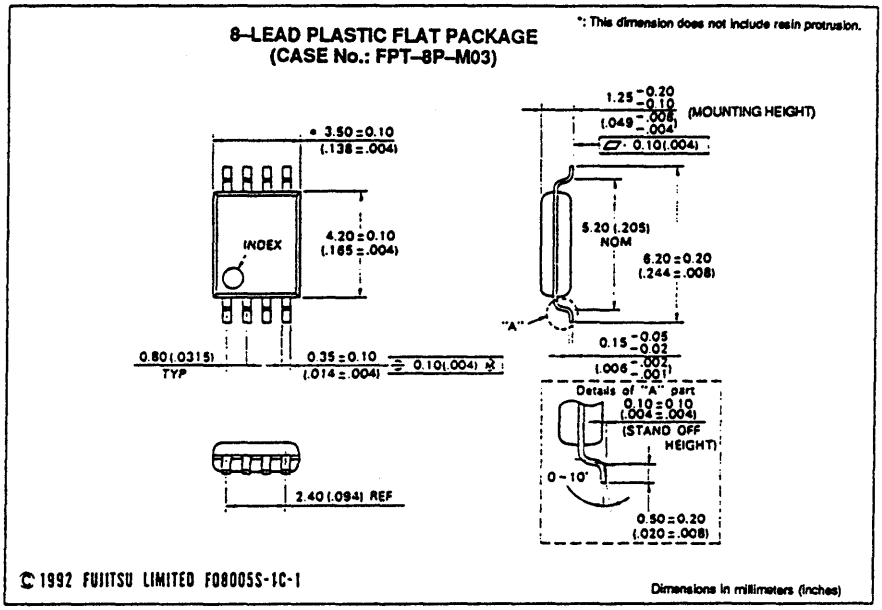
Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply current	Icc	PLL is locked. Vcc = 3.0V, Ta = 25°C	–	3.5	5.0	mA
Operating frequency	fin	AC coupling by 1000pF capacitor	80	–	300	MHz
Oscillator input frequency	fosc	AC coupling by 1000pF capacitor	–	12	23	MHz
Input sensitivity	Pin	AC coupling by 1000pF capacitor	–10	–	+2	dBm
Oscillator input sensitivity	V_{OSCin}	AC coupling by 1000pF capacitor	500	–	–	mVpp
Input voltage (Div)	V_{IH}		Vcc x 0.7	–	–	V
	V_{IL}		–	–	Vcc x 0.3	V
Input current (Div)	I_{IH}		–	–	1.0	µA
	I_{IL}		–1.0	–	–	µA
Input current (OSCin)	Iosc		–100		100	µA
Output voltage	V_{OH}	Vcc = 3.0V	2.6	–	–	V
	V_{OL}	Vcc = 3.0V	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	VDo≦ 3.6V	–	–	1.1	µA

APPLICATION EXAMPLES



PACKAGE DIMENSION



5

SECTION 5

Super Analog RF Devices – *At a Glance*

Introduced are a series of highly integrated Analog RF devices such as Low Noise Amplifiers (LNA), Modulators, Demodulators and Mixers that are typically used in the front ends of mobile and portable wireless communication systems. These include single and multi–function devices based on Fujitsu's advanced RF BiCMOS and Bipolar processes which are second to none.

Page Number	Device Part Number	Frequency (max)	Features	I_{CC} (typ)	V_{CC}	Package
5-3	MB531	1.1 GHz	TX Mixer	12.7 mA	5 V	8–pin SSOP
5-11	MB539	1.6 GHz	LNA	8 mA	5 V	8–pin SSOP
5-19	MB54501	1.1 GHz	LNA/Mixer	6 mA	3 V	16–pin SSOP
5-25	MB54502	1.1 GHz	Dual LNAs	4 mA	3 V	16–pin SSOP
5-31	MB54503	1.1 GHz	PA Driver Amp	26 mA	3.6 V	16–pin SSOP
5-37	MB54609	1.0 GHz	Quadrature Modulator	20 mA	3 V	20–pin SSOP
5-59	MB54619	2.0 GHz	Quadrature Modulator	25 mA	3 V	20–pin SSOP

DS04–23504–1E

FUJITSU

DATA SHEET

MB531 *ASSP BIPOLAR*
Up Conversion Mixer (1.1 GHz)

■ DESCRIPTION

The MB531 is a Up Conversion Mixer ideally suited for car telephones operating on AMPS, TACS and similar frequency bands.

Features include local buffer amp, double balanced mixer and emitter-follower circuit for high conversion gain and high isolation between Lo and RF inputs.

The latest silicon process technology is used to achieve a low power supply current of 13 mA.

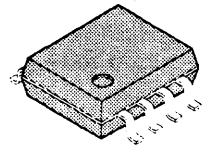
5

■ FEATURES

- Wide input frequency range: up to 1.1 GHz (max)
- High conversion gain: 3.5 dB (typ) Lo: 110 MHz, –5 dBm
  RF: 800 MHz, IF output: 910 MHz
- High isolation: RF–Lo: –28 dB (typ): RF–IF: –13 dB (typ)
  Lo–RF: –37 dB (typ): Lo–IF: –23 dB (typ)

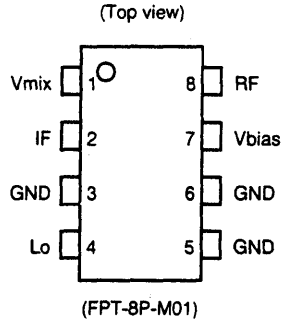
■ PACKAGE

8-pin Plastic SOP



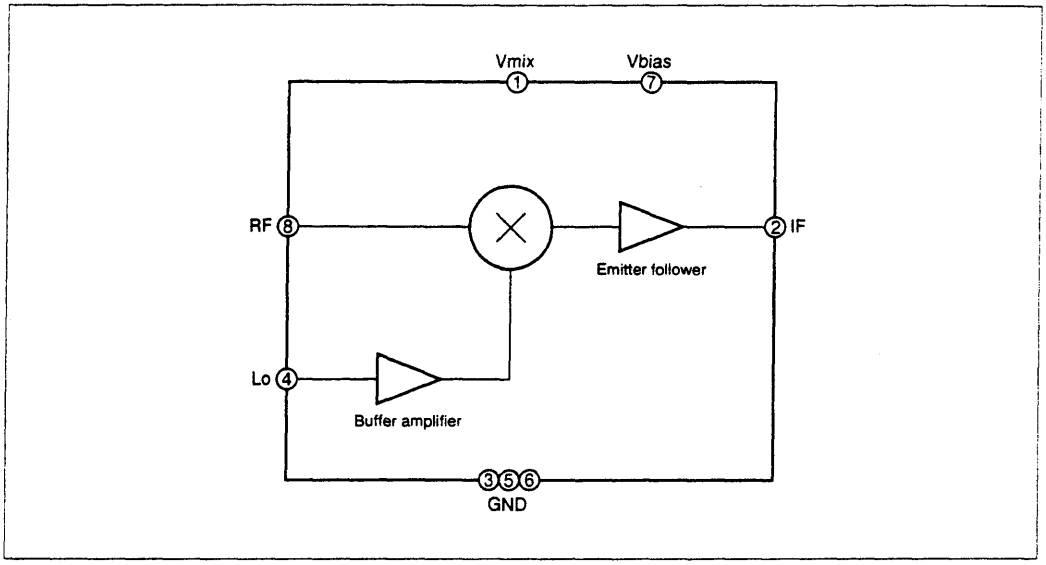
(FPT-8P-M01)

■ PIN ASSIGNMENT



Pin No.	Symbol	Pin description
1	Vmix	Power supply (for mixer circuit)
2	IF	IF output
3	GND	Ground
4	Lo	Lo signal input
5	GND	Ground
6	GND	Ground
7	Vbias	Power supply (for bias circuit)
8	RF	RF signal input

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	V_{IN}	Vcc−3.5 to Vcc−2.5	V
Output current	I_{OUT}	10	mA
Storage temperature	Tstg	−55 to +125	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power supply voltage	Vcc	+4.5 to +5.0	V
Operating temperature	Ta	−40 to +85	°C

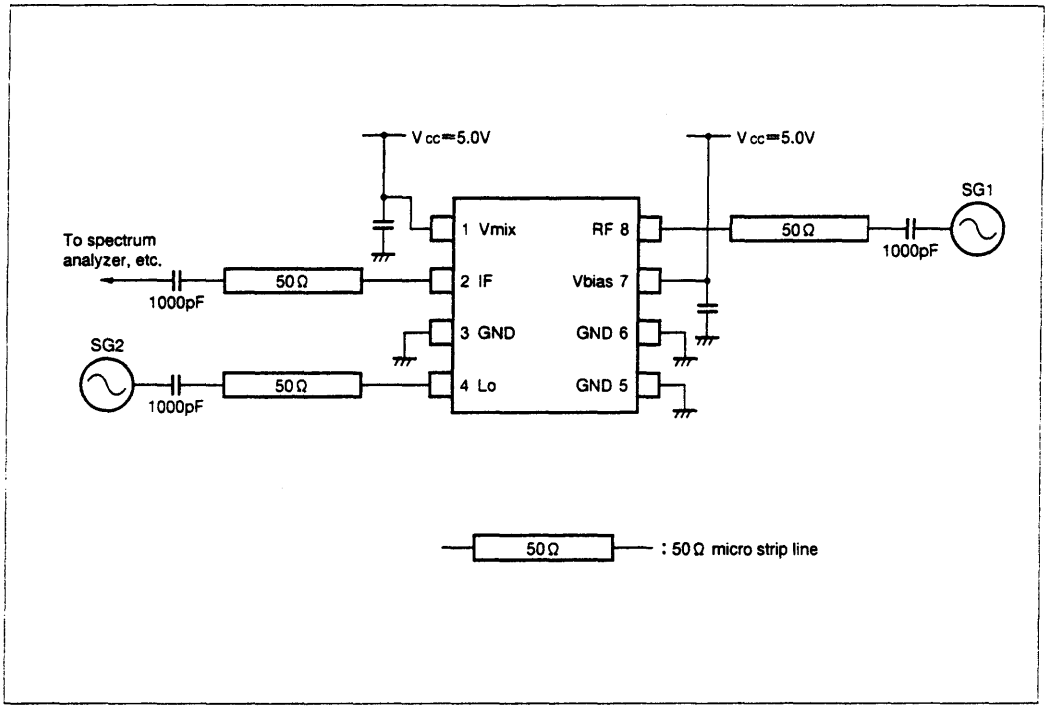
■ ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V, Ta = +25°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply current	Icc	V_{mix} + V_{bias}	9.0	13.0	18.5	mA
Response frequency	f_{RF}	—	—	800	1100	MHz
	f_{LO}	Lo = −10 to 0 dBm	—	110	1100	MHz
Output frequency	f_{IF}	—	—	910	1100	MHz
Conversion gain	Gc	*	—	3.5	—	dB
Maximum output power	P_{OUT}		—	−7.0	—	dBm
Noise figure	NF	DSB measurement value *	—	13.5	—	dB
Third order intercept point	IP3	Input level *	—	−4	—	dBm
1 dB compression point	1dBCP	Output level *	—	−12	—	dBm
Crosstalk attenuation	$X_{RF→LO}$	*	—	−28	—	dB
	$X_{LO→RF}$		—	−37	—	dB
	$X_{RF→IF}$		—	−13	—	dB
	$X_{LO→IF}$		—	−23	—	dB
Open end voltage	V_{RF}	At Vcc = 5V. Pin function verification test (not a condition for operation)	1.5	2.0	2.5	V
	V_{LO}		1.5	2.0	2.5	V
	V_{IF}		2.7	3.2	3.7	V

*: Measurement conditions: RF = 800 MHz, Lo = 110 MHz, −5 dBm, IF = 910 MHz, Vcc = 5V, Ta = +25°C

■ MEASUREMENT CIRCUIT

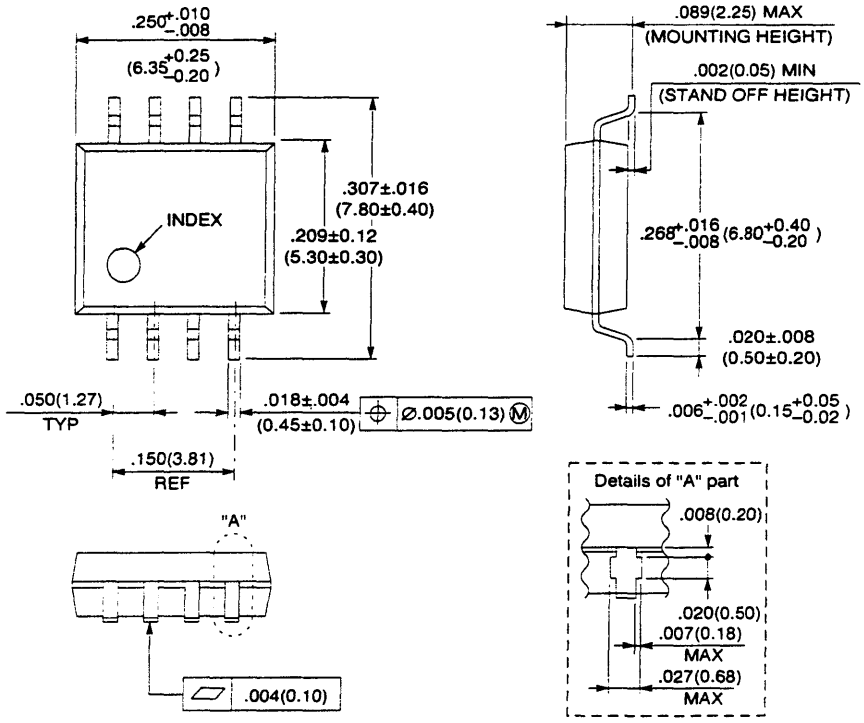


■ ORDERING INFORMATION

Part Number	Package	Remarks
MB531PF	8-pin Plastic SOP (FPT-8P-M01)	

■ PACKAGE DIMENSIONS

8-pin Plastic SOP
(FPT-8P-M01)



Dimensions in inches (mm)

5

DS04-23904-3E

FUJITSU

DATA SHEET

MB539 ASSP BIPOLAR

Low-Noise AMP for High-Frequency Bands (to 1.6 GHz)

5

■ DESCRIPTION

The MB539 is a low-noise amplifier IC (integrated circuit) for high-frequency bands, designed for use in mobile communications systems including portable phones.

The low-noise, high-gain features of the MB539 provide exceptional stability. The IC is capable of operating at frequencies as high as 1.6 GHz.

The latest FUJITSU process technology is used to achieve low power consumption of 9.0 mA (typ).

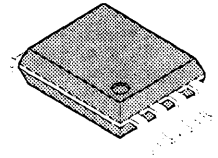
■ FEATURES

- Operating voltage : 5 V (typ.)
- Current consumption : 9.0 mA (typ.)
- Operating frequency : 1.6 GHz (max.)
- Gain : 11 dB
- Noise figure : 4 dB
- Maximum output power : −2 dBm
- 1 dB compression point : −17 dBm (input)
  : −7 dBm (output)
- Third order intercept point : −5 dBm (input)
  : 6 dBm (output)

} at f_{RF} = 1.6 GHz

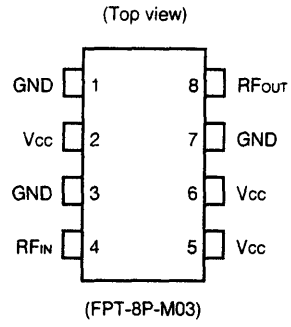
■ PACKAGE

8-pin Plastic SSOP



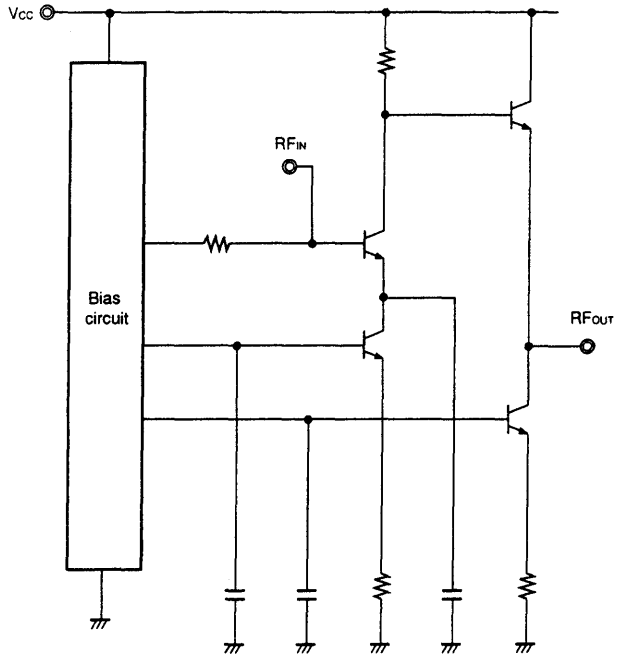
(FPT-8P-M03)

■ PIN ASSIGNMENT



Pin No.	Symbol	Pin description
1	GND	GND
2	Vcc	Power supply
3	GND	GND
4	RFIN	RF AMP input
5	Vcc	Power supply
6	Vcc	Power supply
7	GND	GND
8	RFOUT	RF AMP output

■ EQUIVALENT CIRCUIT DIAGRAM



(Total 9.0 mA)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Remarks
Power supply voltage	V_{CC}	−0.5 to +7.0	V	
Output voltage	V_O	−0.5 to V_{CC}+0.5	V	
Input voltage	V_I	−0.5 to V_{CC}+0.5	V	
Output current	I_O	0 to 10	mA	
Storage temperature	Tstg	−55 to +125	°C	

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating Temperature	Ta	−40	—	+85	°C	

Note: The user should take full precautions to prevent accidental damage from static electricity.

- For storage or transport, place in a conductive case.
- Before handling, verify that all operators, fixtures and tools are free from electrification (grounded), and use an operating platform of grounded conductive sheeting.
- Always switch off the power before this device is inserted into or removed from sockets.
- When handling or transporting circuit boards in which this device is mounted, leads must be protected by conductive sheeting.

■ ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	Vcc	4.5	5.0	5.5	V	
Power supply current	Icc	—	9.0	12.0	mA	Vcc = 5.0V
Operating frequency	fmax	—	1100	1600	MHz	

1. f_{RF} = 1100 MHz

(Vcc = 5.0V, Ta = +25°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Gain	G_{ain}	—	16.0	—	dB	
Noise figure	NF	—	2.5	—	dB	
Maximum output power	P_{OUT}	—	0.0	—	dBm	
1 dB compression point	1dB CP	—	−19.0	—	dBm	Input
		—	−3.0	—	dBm	Output
Intercept point	IP_3	—	−8.0	—	dBm	Input
		—	8.0	—	dBm	Output
In-Out isolation	Iso	—	−25.0	—	dB	

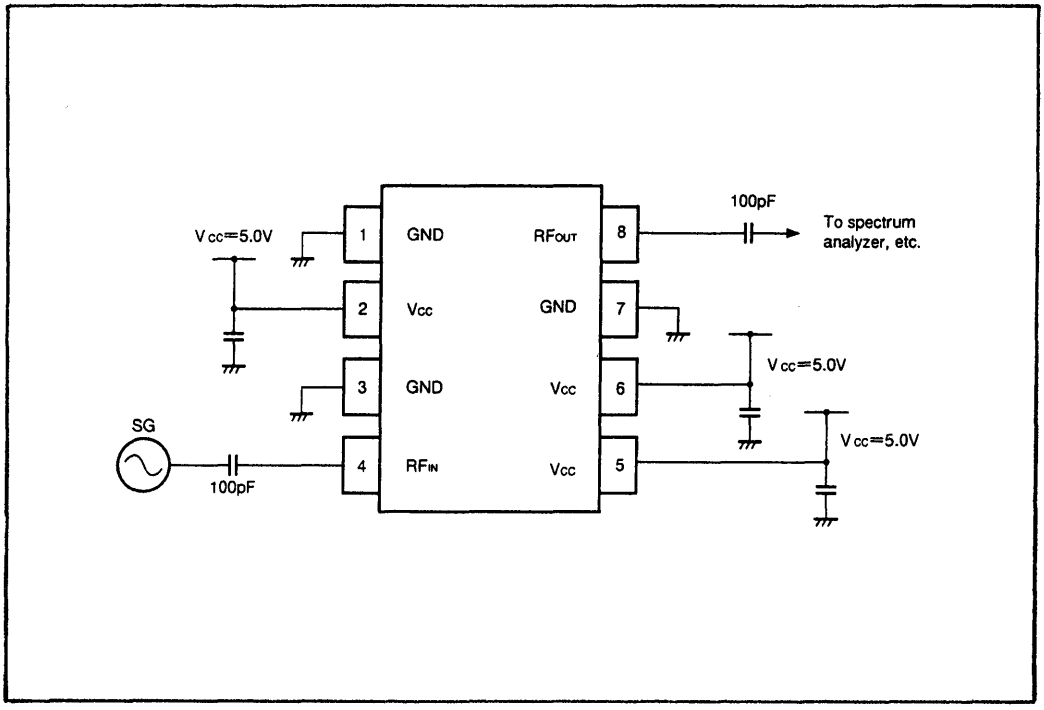
2. f_{RF} = 1600 MHz

(Vcc = 5.0V, Ta = +25°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Gain	G_{ain}	—	11.0	—	dB	
Noise figure	NF	—	4.0	—	dB	
Maximum output power	P_{OUT}	—	−2.0	—	dBm	
1 dB compression point	1dB CP	—	−17.0	—	dBm	Input
		—	−7.0	—	dBm	Output
Intercept point	IP_3	—	−5.0	—	dBm	Input
		—	6.0	—	dBm	Output
In-Out isolation	Iso	—	−20.0	—	dB	

Note: • Electrical characteristics may vary depending on the use of external elements or mounting conditions.
• The above characteristics represent data obtained with the "■ MEASUREMENT CIRCUIT."

■ MEASUREMENT CIRCUIT



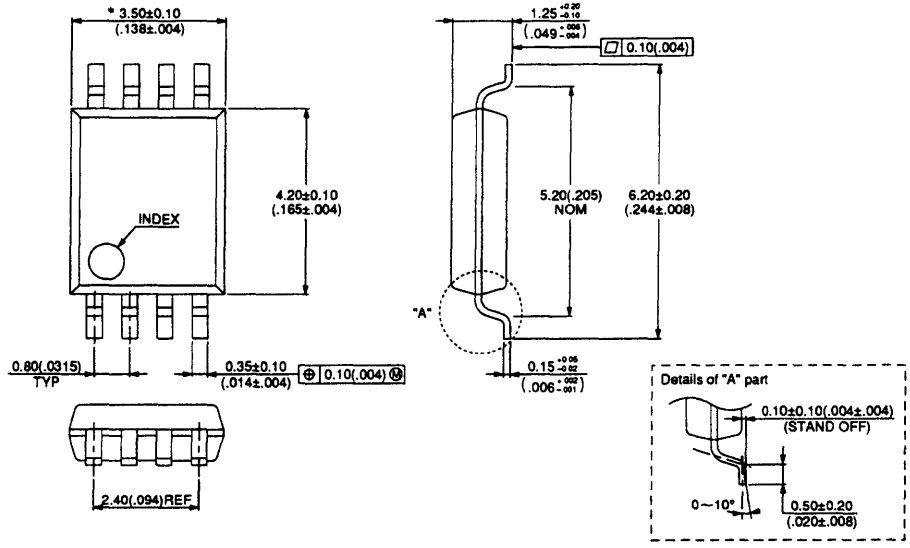
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB539PFV	8-pin Plastic SSOP (FPT-8P-M03)	

■ PACKAGE DIMENSION

8-pin Plastic SSOP
(FPT-8P-M03)

*: This dimension does not include resin protruction.



Dimensions in mm (inches)

5

Sept. 1995
Edition 1.0a

FUJITSU

Data Sheet

MB54501

FRONT–END UP/DOWN CONVERTER

INTRODUCTION

The Fujitsu MB54501 includes a low-noise amplifier and a mixer, which are used for front end of mobile telecommunication systems.
Using Fujitsu's advanced technology, MB54501 achieves an Icc of 6.0mA (typ.).

ELECTRICAL CHARACTERISTICS

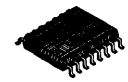
	Amplifier	Mixer
• Supply voltage	3V (typ.)	3V (typ.)
• Current consumption	3mA (typ.)	3mA (typ.)
• Input frequency	1.1GHz(max.)	1.1GHz(max.)
• Gain	14dB (typ.) *1	15dB (typ.) *2
• Noise figure	2.2dB (typ.) *1	5dB (SSB, typ.) *2
• 1dB compression point	–1dBm (typ.) *1	
• Input return loss	8dB (typ.) *1	
• Output return loss	10dB (typ.) *1	

*1 : Measured by the circuit of "measurement circuit example". (fin = 878MHz)

*2 : Measured by the circuit of "measurement circuit example". (IF = 90MHz)

PACKAGE

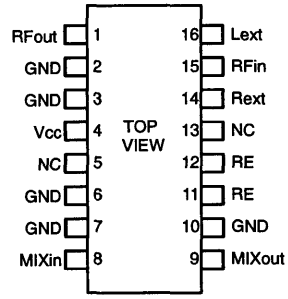
- 16-pin Plastic Shrink Small Outline Package (Suffix: -PFV)



PLASTIC PACKAGE
FP-16P-M05

5

PIN ASSIGNMENT



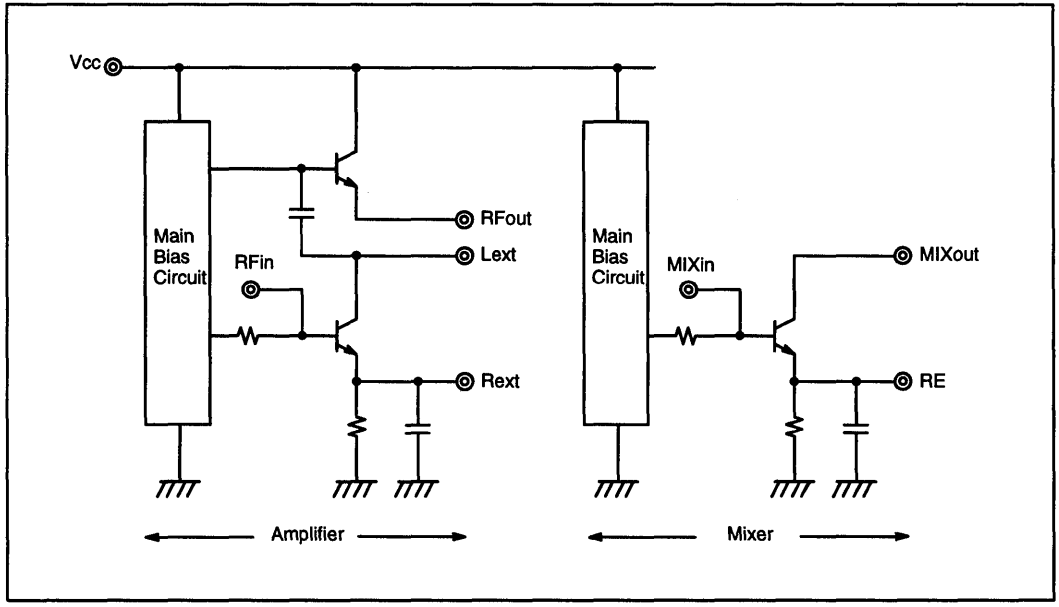
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_O	–0.5 to Vcc+0.5	V
Output Current	I_O	0 to 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

EQUIVALENT CIRCUIT



PIN DESCRIPTIONS

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	RFout	Amplifier output	9	MIXout	Mixer output
2	GND	Ground	10	GND	Ground
3	GND	Ground	11	RE	Emitter of a transistor for mixer
4	Vcc	Power supply	12		
5	NC	No connection	13	NC	No connection
6	GND	Ground	14	Rext	Emitter of a transistor for amplifier
7	GND	Ground	15	RFin	Amplifier input
8	MIXin	Mixer input	16	Lext	Amplifier load connection

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc	2.7	3.0	5.5	V
Input Voltage	V_I	GND	–	Vcc	V
Operating Temperature	Ta	–40	–	+85	°C

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

AMPLIFIER

(Vcc = +3.0V, Ta = 25°C)

Parameter	Symbol	Conditions	Target Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{CC}		2.7	3.0	5.5	V
Supply Current	I_{CC}		–	3.0		mA
Operating Frequency	RF_{IN}		–	878	1100	MHz
Gain	Gain		–	14	–	dB
Noise Figure	NF		–	2.2	–	dB
1dB Compression Point	P_{1dB}	Output	–	–1	–	dBm
Input Return Loss	RL_{IN}		–	8	–	dB
Output Return Loss	RL_{OUT}		–	10	–	dB

Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

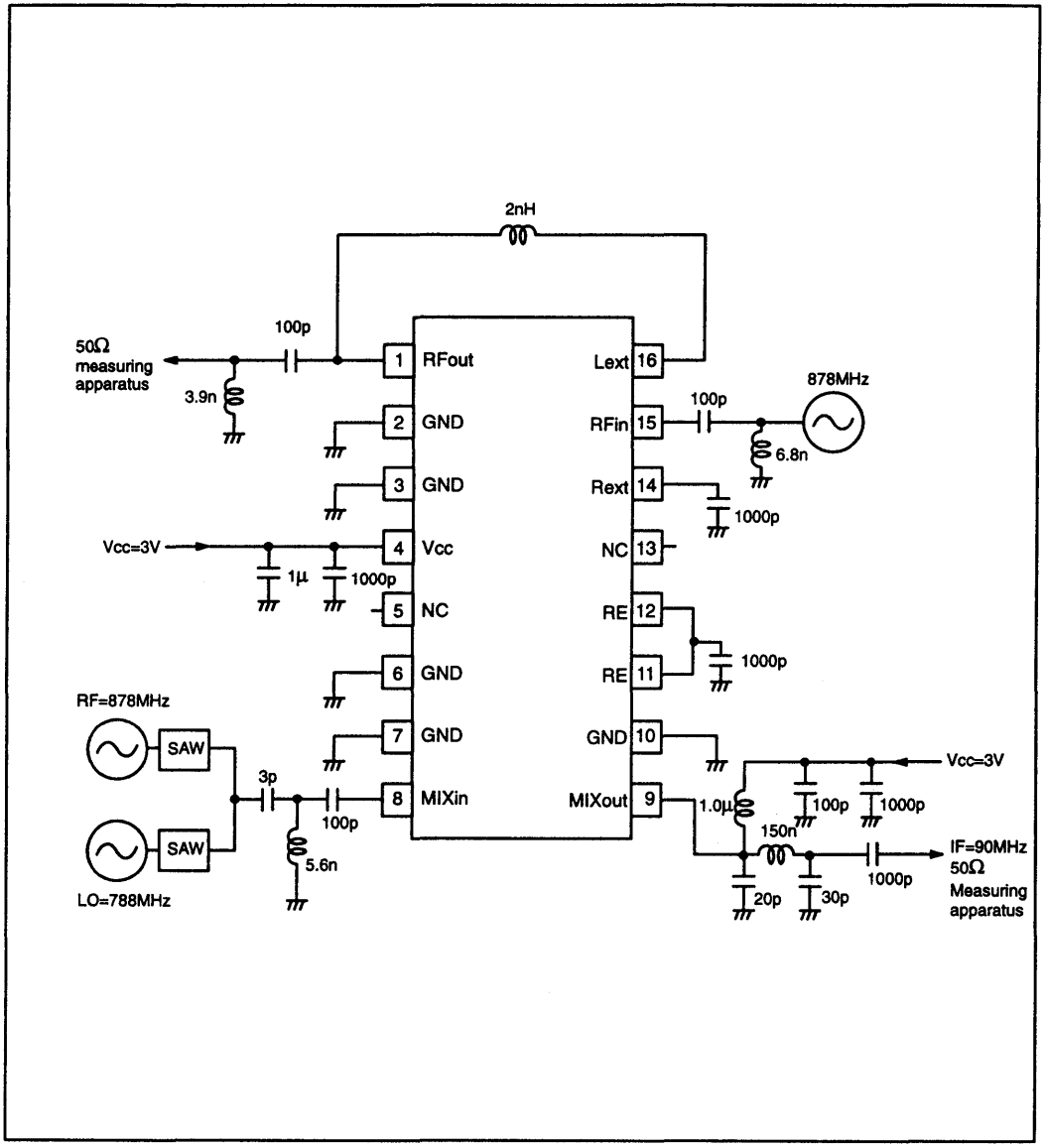
MIXER

(Vcc = +3.0V, Ta = 25°C)

Parameter	Symbol	Conditions		Target Value			Unit
				Min.	Typ.	Max.	
Supply Voltage	V_{CC}			2.7	3.0	5.5	V
Current Consumption	I_{CC}			–	3.0	–	mA
Operating Frequency	MIX_{IN}			–	878	1100	MHz
Gain	S_{21}	Amplifier characteristics		–	9	–	dB
Conversion Gain	Gc	Mixer characteristics IF = 90MHz		–	15	–	dB
Noise Figure	NF		SSB	–	5	–	dB

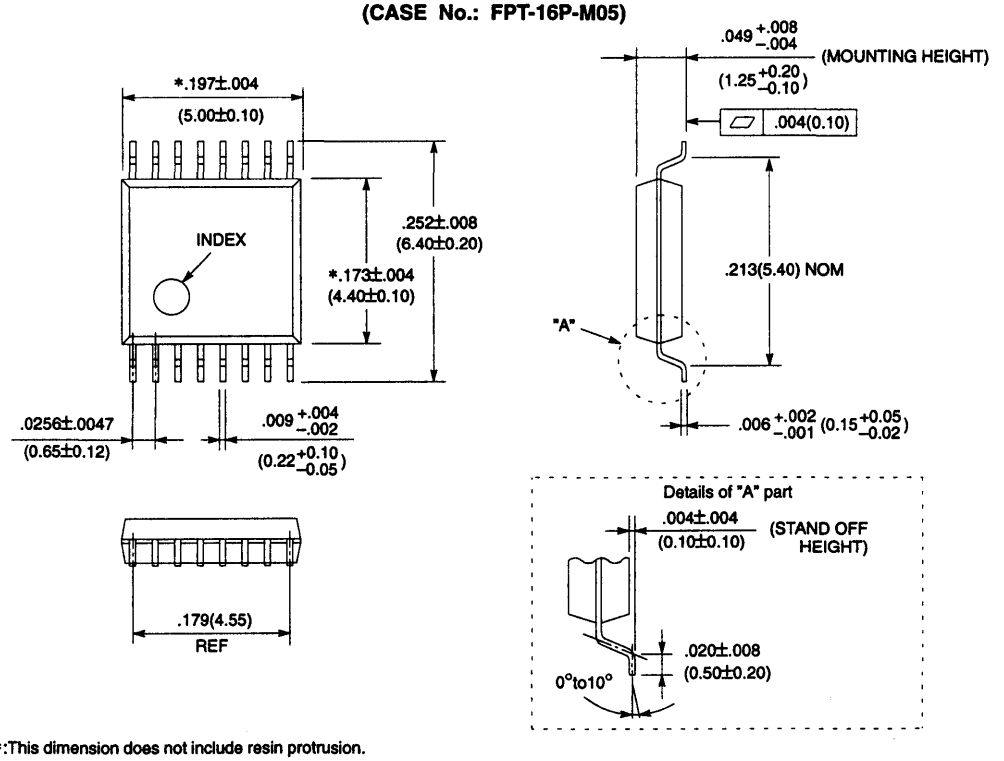
Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

MEASUREMENT CIRCUIT (EXAMPLE)



PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0a

FUJITSU

Data Sheet

MB54502

LOW NOISE AMPLIFIER (2 CIRCUITS)

5

LOW NOISE AND CURRENT AMPLIFIER

INTRODUCTION

The Fujitsu MB54502 includes two independent amplifiers which are used for mobile telecommunication applications such as handy phones and car phones. Both of the amplifiers achieve low current consumption as well as the low noise performance. Using Fujitsu's advanced technology, MB54502 achieves an Icc of 2mA typ. respectively (total 4mA typ.).

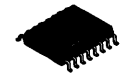
ELECTRICAL CHARACTERISTICS

- Supply voltage 3V (typ.)
- Current consumption 2mA (typ.)
- Input frequency 1.1GHz(max.)
- Gain 14dB (typ.) *1
- Noise figure 2.2dB (typ.) *1
- 1dB compression point –6dBm (typ.) *1
- Amplitude tolerance 2.5dB (typ.) *1
- Input return loss 8dB (typ.) *1
- Output return loss 8dB (typ.) *1

*1 : Measured by the circuit of "measurement circuit example". (fin = 820MHz)

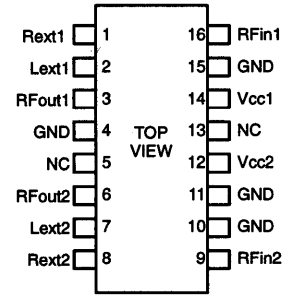
PACKAGE

- 16-pin Plastic Shrink Small Outline Package (Suffix: -PFV)



PLASTIC PACKAGE
FP-16P-M05

PIN ASSIGNMENT



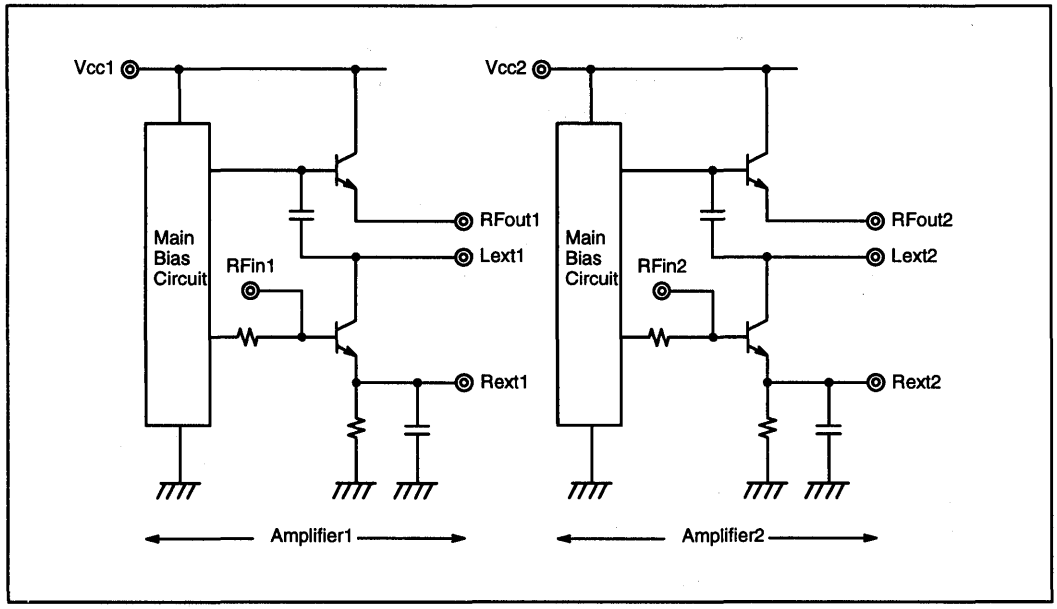
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit
Supply Voltage	Vcc	–0.5 to 7.0	V
Output Voltage	Vo	–0.5 to Vcc+0.5	V
Output Current	Io	0 to 10	mA
Storage Temperature	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

EQUIVALENT CIRCUIT



PIN DESCRIPTIONS

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	Rext1	Emitter (amplifier 1)	9	RFin2	Input (amplifier 2)
2	Lext1	Load connection (amplifier 1)	10	GND	Ground
3	RFout1	Output (amplifier 1)	11	GND	Ground
4	GND	Ground	12	Vcc2	Power supply (amplifier 2)
5	NC	No connection	13	NC	No connection
6	RFout2	Output (amplifier 2)	14	Vcc1	Power supply (amplifier 1)
7	Lext2	Load connection (amplifier 2)	15	GND	Ground
8	Rext2	Emitter (amplifier 2)	16	RFin1	Input (amplifier 1)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc	2.7	3.0	5.5	V
Input Voltage	V_I	GND	–	Vcc	V
Operating Temperature	Ta	–40	–	+85	°C

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

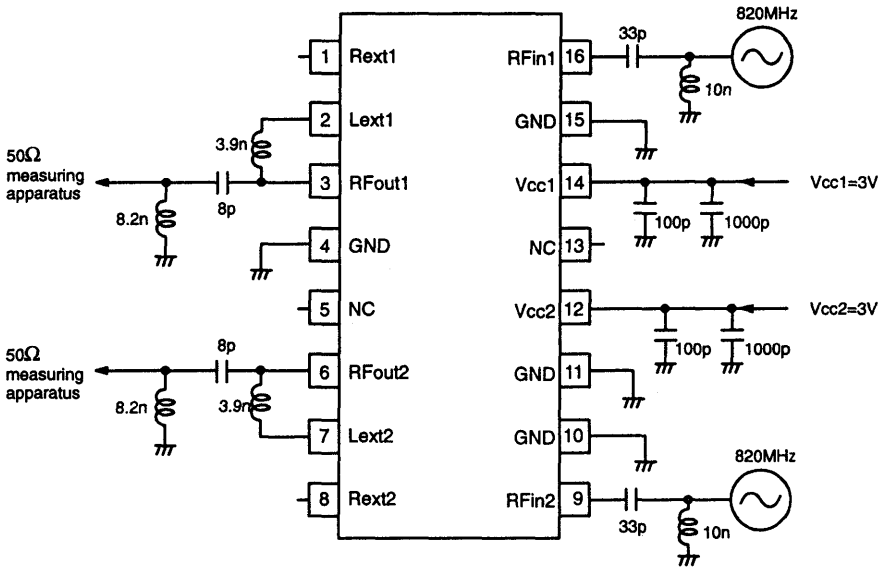
ELECTRICAL CHARACTERISTICS

(Vcc1 = +3.0V, Vcc2=0.0V, Ta = 25°C
or Vcc1 = 0.0V, Vcc2=+3.0V, Ta = 25°C)

Parameter	Symbol	Conditions	Target Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	Vcc		2.7	3.0	5.5	V
Supply Current	Icc	1 amplifier active	–	2.0	–	mA
Operating Frequency	fin		–	820	1100	MHz
Gain	Gain		–	14	–	dB
Noise Figure	NF		–	2.2	–	dB
1dB Compression Point	P_{1dB}	Output	–	–6	–	dBm
Amplitude Tolerance	–	820 ± 50 MHz	–	2.5	–	dB
Input Return Loss	RL_{IN}		–	8	–	dB
Output Return Loss	RL_{OUT}		–	8	–	dB

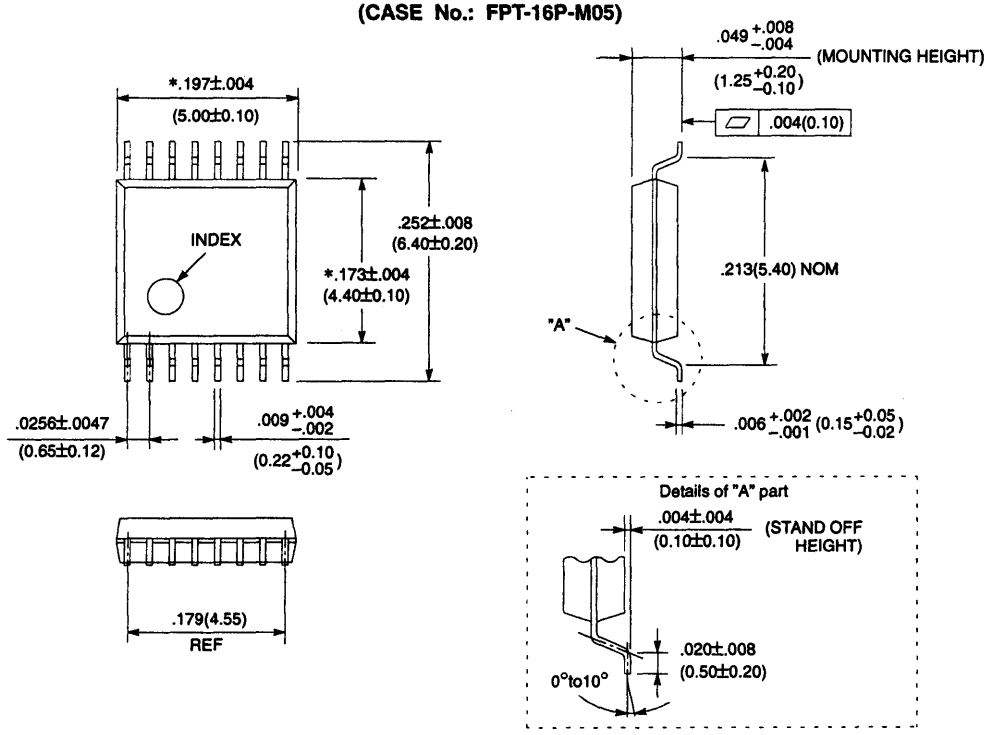
Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

MEASUREMENT CIRCUIT (EXAMPLE)



PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

Sept. 1995
Edition 1.0a

FUJITSU

Data Sheet

MB54503

HIGH-POWER AMPLIFIER

INTRODUCTION

The Fujitsu MB54503 is a high-power amplifier which is used for mobile telecommunication systems such as handy phones and car phones. This device is ideally suitable for power amplifier driver.
Using Fujitsu's advanced technology, MB54503 achieves an Icc of 26.0mA (typ.).

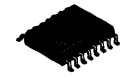
ELECTRICAL CHARACTERISTICS

- Supply voltage 3.6V (typ.)
- Current consumption 26mA (typ.)
- Input frequency 1.1GHz(max.)
- Gain 25dB (typ.) *1
- Output level (@Pin=–8dBm) +13dBm (typ.) *1
- Input return loss 14dB (typ.) *1
- Output return loss 6dB (typ.) *1

*1 : Measured by the circuit of "measurement circuit example". (fin = 933MHz)

PACKAGE

- 16-pin Plastic Shrink Small Ooutline Package (Suffix: -PFV)



PLASTIC PACKAGE
FP-16P-M05

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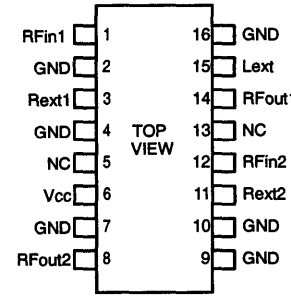
PIN ASSIGNMENT



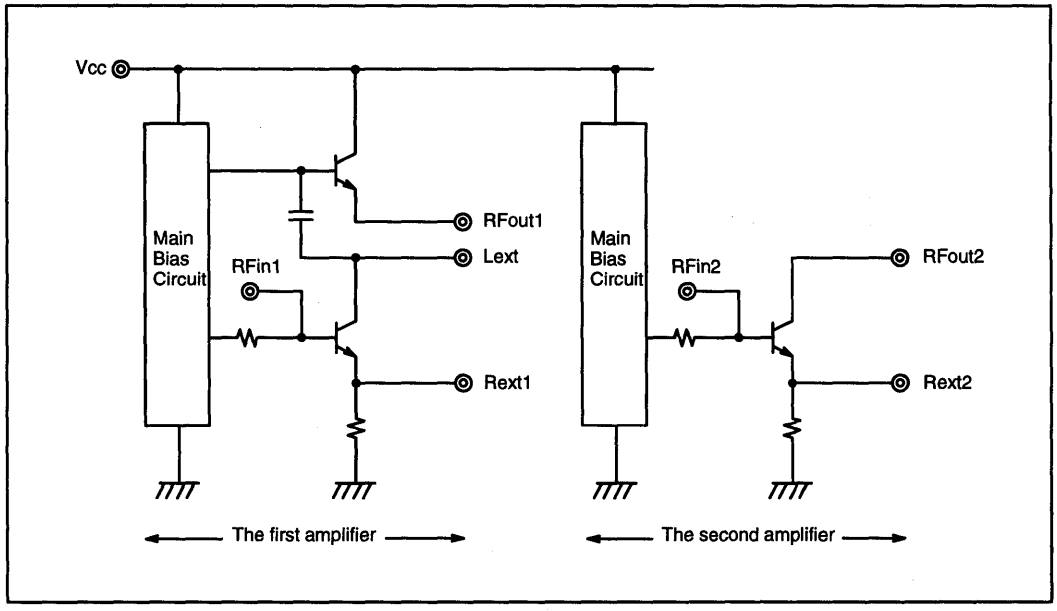
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit
Supply Voltage	Vcc	–0.5 to 7.0	V
Output Voltage	Vo	–0.5 to Vcc+0.5	V
Output Current	Io	0 to 10	mA
Storage Temperature	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

EQUIVALENT CIRCUIT



PIN DESCRIPTIONS

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	RFin1	The first amplier input	9	GND	Ground
2	GND	Ground	10	GND	Ground
3	Rext1	Emitter for the first amplifier	11	Rext2	Emitter for the second amplifier
4	GND	Ground	12	RFin2	The second amplier input
5	NC	No connection	13	NC	No connection
6	Vcc	Power supply	14	RFout1	The first amplifier output
7	GND	Ground	15	Lext	Load connecting for the first amplifier
8	RFout2	The second amplifier output	16	GND	Ground

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc	2.7	3.6	5.0	V
Input Voltage	V_I	GND	–	Vcc	V
Operating Temperature	Ta	–40	–	+85	°C

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

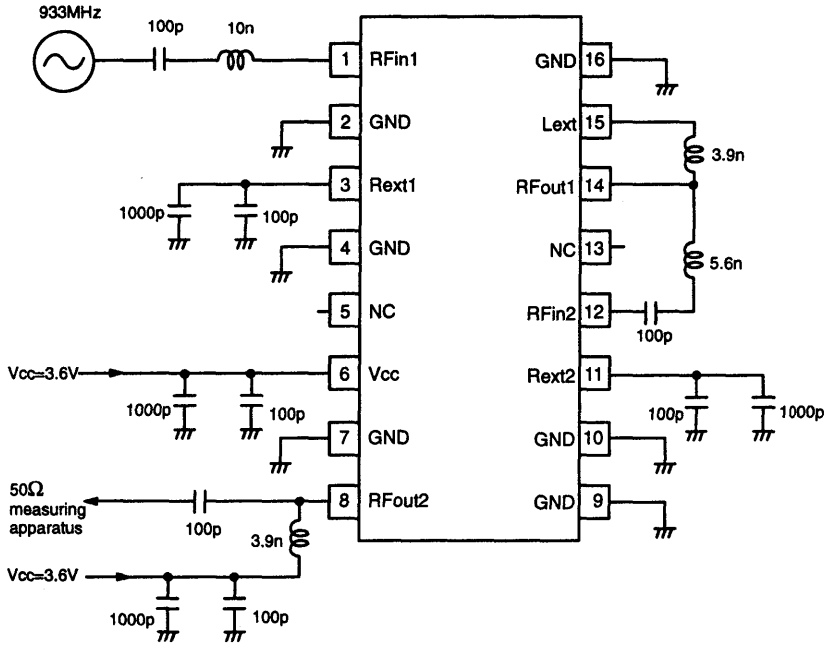
ELECTRICAL CHARACTERISTICS

(Vcc = +3.6V, Ta = 25°C)

Parameter	Symbol	Conditions	Target Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	Vcc		2.7	3.6	5.0	V
Supply Current	Icc		–	26	–	mA
Operating Frequency	fin		–	933	1100	MHz
Gain	Gain		–	25	–	dB
Output Power	Pout	Pin = –8dBm	–	+13	–	dBm
Input Return Loss	R_{LIN}		–	14	–	dB
Output Return Loss	R_{LOUT}		–	6	–	dB

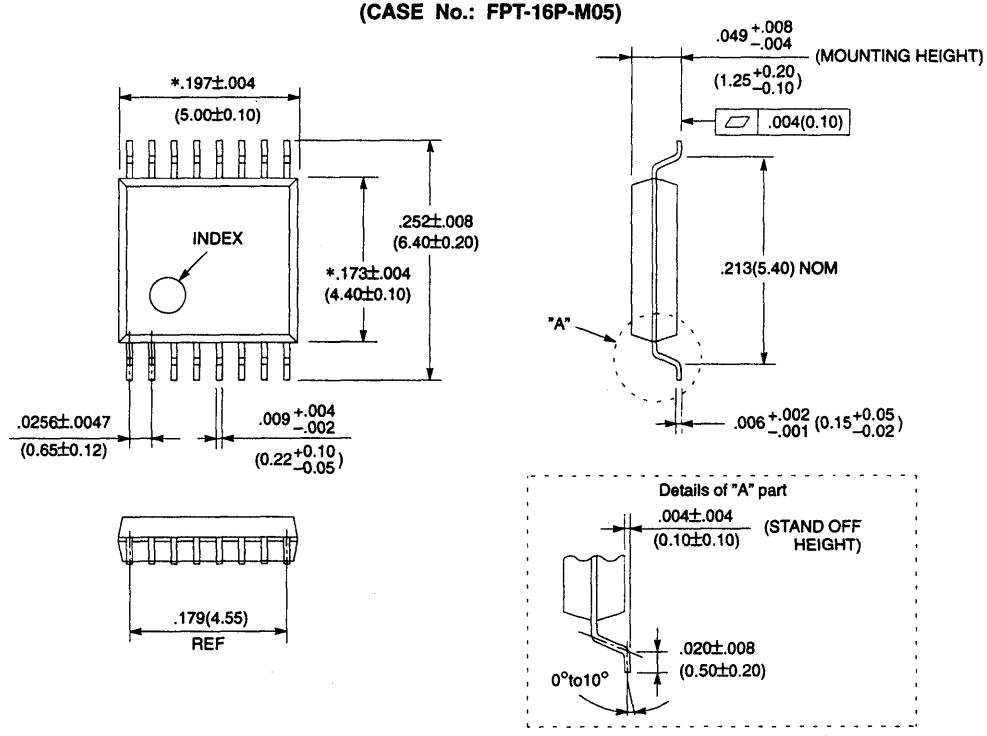
Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

MEASUREMENT CIRCUIT (EXAMPLE)



PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

DS04–23509–1E

FUJITSU

DATA SHEET

MB54609 *ASSP for Telephone*

Quadrature Modulator IC (With 1.0 GHz Up–Converter)

■ DESCRIPTION

The MB54609 is an intermediate-frequency (IF) quadrature modulator IC incorporating a 1.0-GHz up-converter optimized for use in digital mobile telecommunication systems such as GSM and PDC (Personal Digital Cellular).

The MB54609 incorporates a quadrature modulator for IF modulation, a transmission up-convert mixer, and a F/F type phase shifter as well, capable of handing IFs in a broad band.

In addition, the MB54609 operates at a low power supply voltage of 3.0 V and a low power supply current of 18 mA (both as typical values), contributing to saving the power consumption of the device.

5

■ FEATURES

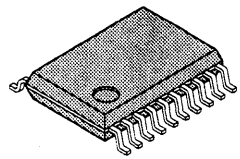
- Incorporating a high-performance transmission mixer covering the entire frequency band of up to 800 MHz used for PDC services (Maximum output frequency of 1.1 GHz)
  Maximum output frequency: 1.1 GHz, Output level: −9 dBm (typical)

- Externally connecting the quadrature modulator with the transmission mixer, allowing a bandpass filter (BPF) to be inserted in between
  The quadrature modulator output can drive a 50 Ω load.

(Continued)

■ PACKAGE

20-pin Plastic SSOP

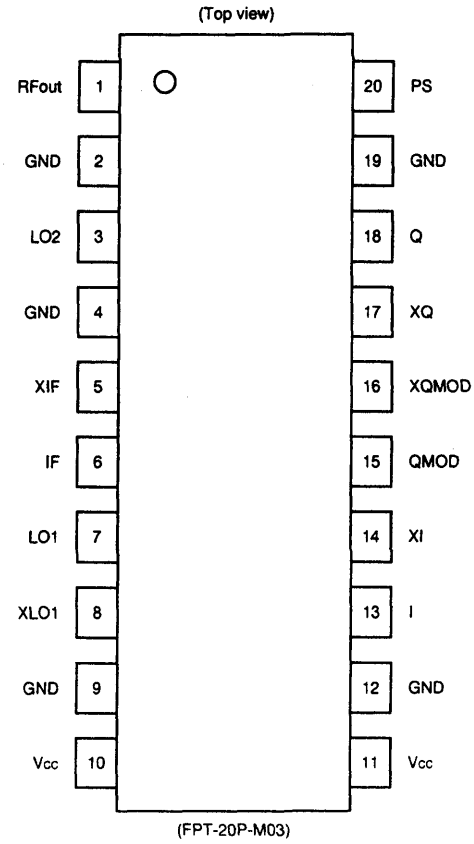


(FPT-20P-M03)

(Continued)

- Flip-flop phase shifter capable of handling intermediate frequencies in the broad band (100 to 800 MHz)
- Operation at low voltage: 2.7 to 3.0 to 3.3 V
- Low current consumption
  During operating: 18.0 mA (typical)
  In power save mode: 0.6 mA (typical)
- Operating temperature range: Ta = –20 to +85°C

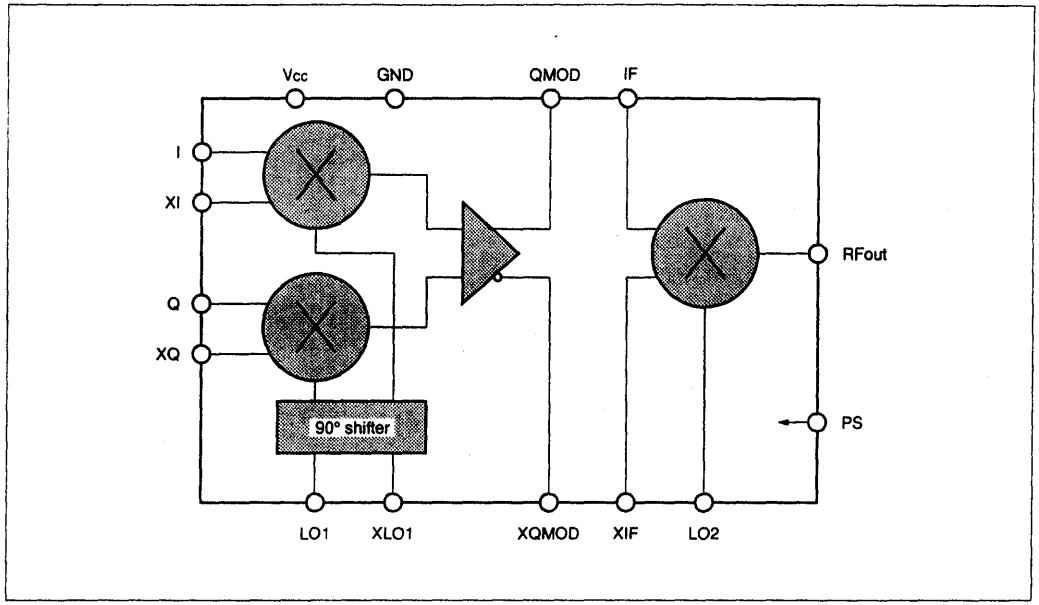
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Pin name	Function	
1	RFout	Up-converter output pin	
2	GND	GND pin	
3	LO2	LO input pin for mixer	
4	GND	GND pin	
5	XIF	IF input complementary pin for mixer	
6	IF	IF input pin for mixer	
7	LO1	LO input pin for quadrature modulator	
8	XLO1	LO input complementary pin for quadrature modulator	
9	GND	GND pin	
10	Vcc	Power supply pin	Power supply voltage must be applied to both pins.
11	Vcc	Power supply pin	
12	GND	GND pin	
13	I	Baseband input (I) pin	
14	XI	Baseband input (I) complementary pin	
15	QMOD	Quadrature modulator IF output pin	
16	XQMOD	Quadrature modulator IF output complementary pin	
17	XQ	Baseband input (Q) complementary pin	
18	Q	Baseband input (Q) pin	
19	GND	GND pin	
20	PS	Power save mode control pin	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Power supply voltage	Vcc	−0.5 to 5.0	V	
Output voltage	Vo	−0.5 to Vcc + 0.5	V	
Input voltage	VI	−0.5 to Vcc + 0.5	V	
Open collector applied voltage	Voc	Vcc ± 0.3 (−0.5 to 5.0)	V	RFout pin Do not leave this pin open.
Output current	Io	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

Note: Although the MB54609 contains an antistatic element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device:

- When storing or carrying the device, put it in a conductive case.
- Before handling the device, check that the jigs and tools to be used have been uncharged (grounded) as well as yourself. Use a conductive sheet on the working bench.
- Before fitting the device into or removing it from the socket, turn the power supply off.
- When handling (such as transporting) the MB54609 mounted board, protect the leads with a conductive sheet.

Precaution: Exceeding any of the above absolute maximum ratings may cause permanent damage to the LSI. For normal operation, the device should be used under the recommended operating conditions. Exceeding any of the recommended conditions may adversely affect LSI reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	Vcc	2.7	3.0	3.3	V	
Input voltage	VI	GND	—	Vcc	V	
Open collector applied voltage	Voc	Vcc - 0.2	—	Vcc + 0.2	V	RFout pin. Do not leave this pin open.
Operating temperature	Ta	−20	—	+85	°C	

5

■ ELECTRICAL CHARACTERISTICS

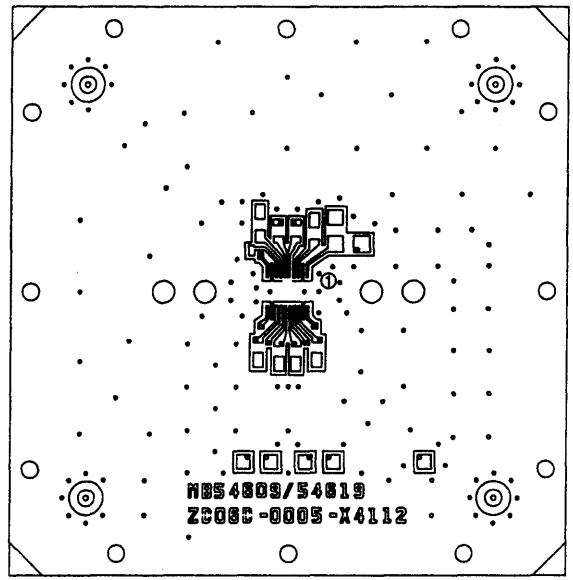
(Vcc = 3.0 V, Ta = +25°C)

Parameter		Symbol	Value			Unit	Remarks	
			Min.	Typ.	Max.			
Power supply current		Icc	—	18.0	23.5	mA	DC current (Input with no AC signal)	
Power supply current in power save mode		IccPS	—	0.6	0.9	mA	DC current (Input with no AC signal)	
Shifter input LO1	Operating band	fLO1	100	400	800	MHz		
	Input level	PLO1	−15	—	−5	dBm		
Baseband input	Operating band	fBB	DC	—	10	MHz		
	Input amplitude	VBB	—	—	1.2	Vpp		
	Offset voltage	Vos	1.5	1.6	1.7	V	External offset voltage value	
	Offset current	Ios	—	3.0	—	μA	Input Imp. converted value = 533 kΩ	
Mixer input LO2	Operating band	fLO2	—	750	1100	MHz		
	Input level	PLO2	—	—	0	dBm		
Mixer output RFout	Operating band	fRF	—	950	1100	MHz	fRF = fLO2 ± fLO1/2	
	Output level	PRF	—	−9	—	dBm	—	fLO1 = 400 MHz (−15 dBm) fLO2 = 750 MHz (−5 dBm) fRF = 950 MHz output QMOD/Mix direct connection VBB = 1 Vpp
Modulation precision	Amplitude deviation	AERR	—	1.3	—	%	RMS value	
	Phase deviation	PERR	—	0.82	—	deg.	RMS value	
	Vector error	VERR	—	1.9	—	%	RMS value	
Carrier suppression		CS	—	−40	−30	dBc	With external offset unadjusted	

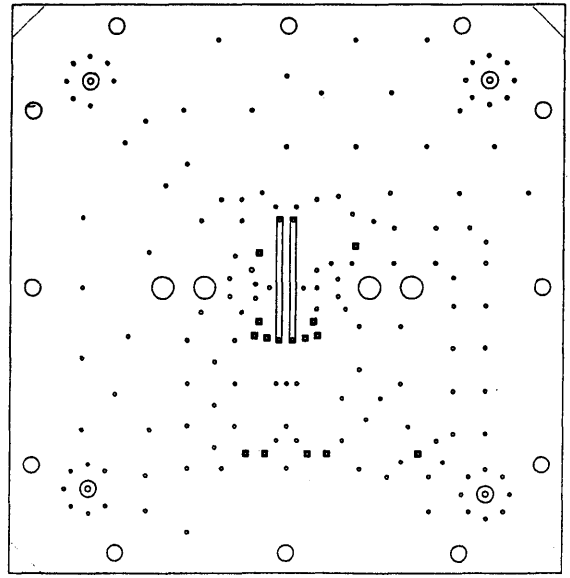
■ EVALUATION BOARD (Reference Example)

- Material: BT resin BT-HL870 (Dielectric constant [1 MHz] = 3.4 to 3.6)
- Thickness: 4 layers, 1.6 mm (Copper thickness: External layer = 18 µm, Internal layer = 70 µm)
- Plating: electroless gold plating

- **Layer 1 (front surface)**



- **Layer 2**



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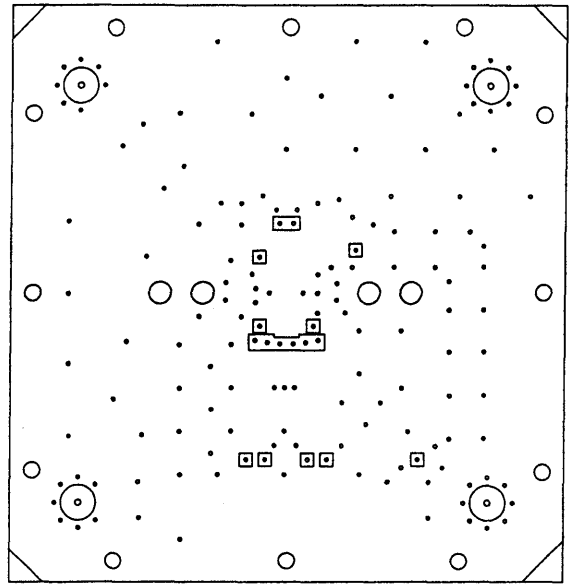
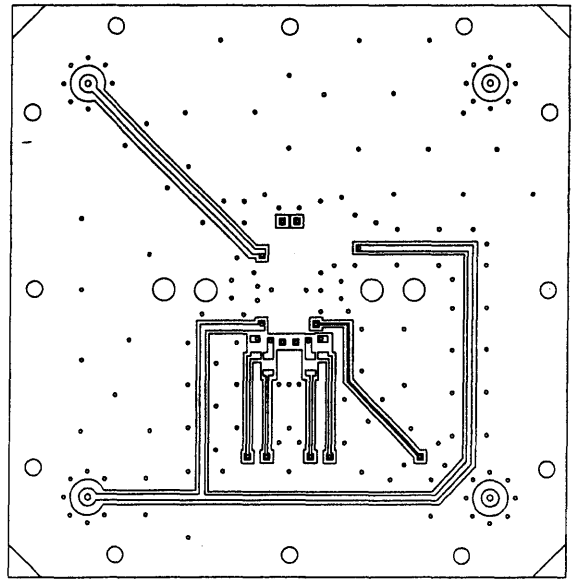
- **Layer 3**



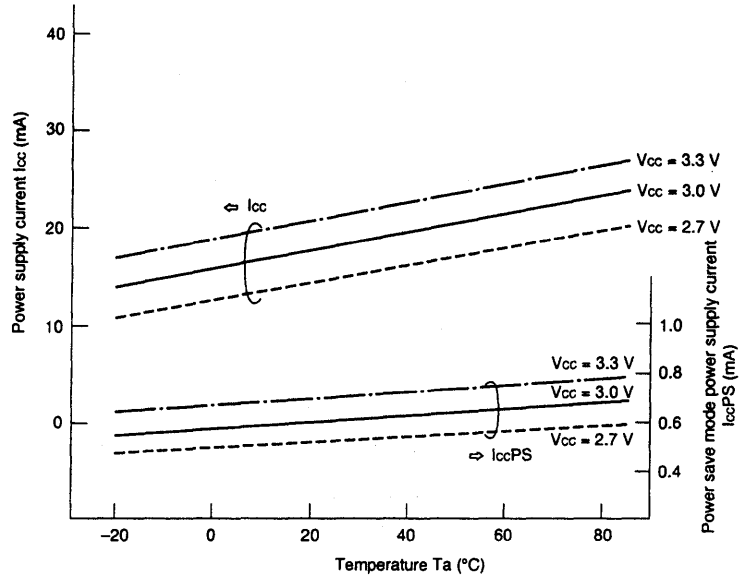
- **Layer 4 (rear surface)**



■ MEASUREMENT DATA (Reference Values)

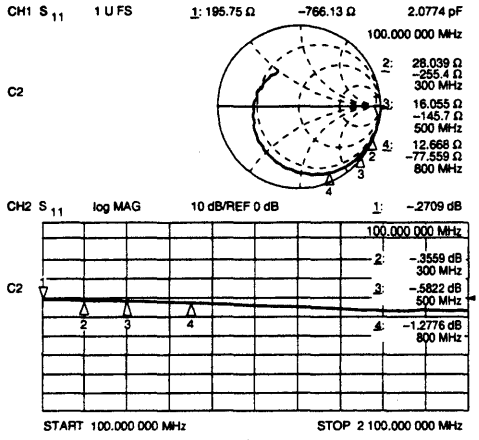
* Application-common characteristics

• **DC characteristics (test circuit 1)**
@ Input with no AC signal

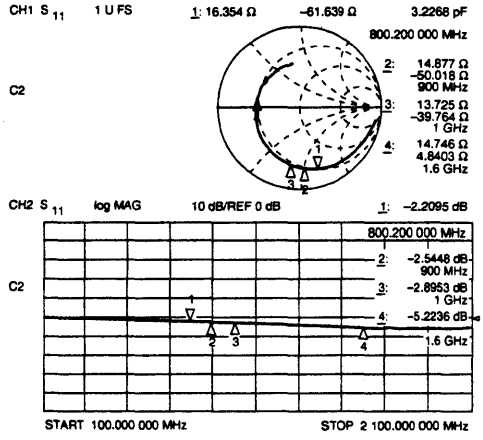


- **Input impedance (Only IC: test circuit 4)**
  @ Impedance from IC pin end

- **LO1**

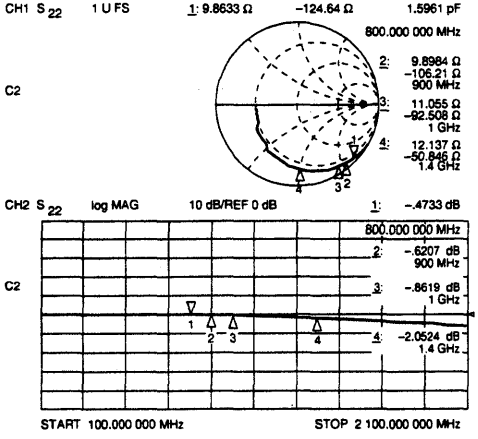


- **LO2**



- **Output impedance (Only IC: test circuit 4)**
  @ Impedance from IC pin end

- **RFout**



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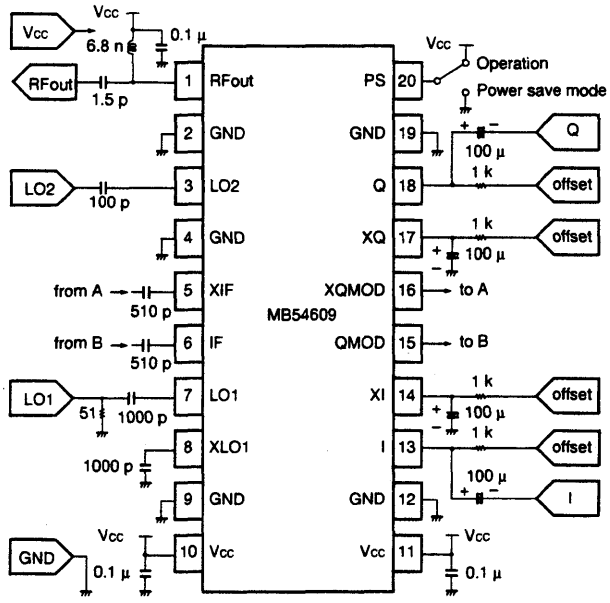
■ 800-MHz PDC APPLICATION MEASUREMENT DATA (Reference Values)

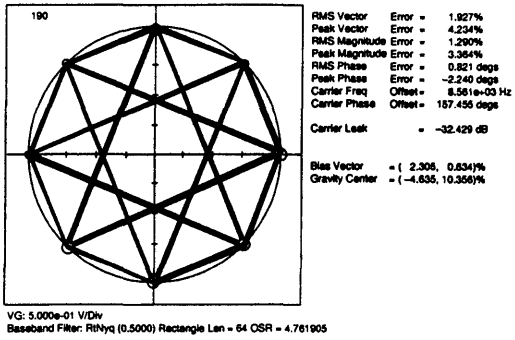
Parameter	Symbol	Measurement result	Unit	Condition	Test circuit
Baseband input signal	f_{BB}	42	kbps	π/4DQPSK, Root-Nyquist filter (α = 0.5)	—
	V_{BB}	1.0	Vpp	Single-end input	—
Shifter input signal LO1	f_{LO1}	400	MHz	—	—
	P_{LO1}	−15	dBm	—	—
Mixer input signal LO2	f_{LO2}	750	MHz	—	—
	P_{LO2}	−5	dBm	—	—
Mixer output signal RFout	f_{RF}	950	MHz	$f_{RF} = f_{LO2} + f_{LO1}/2$	—
	P_{RF}	−8.4	dBm	SSB value	1
Return loss	RL_{LO1}	−17	dB	f_{LO1} = 400 MHz	3
	RL_{LO2}	−2	dB	f_{LO2} = 750 MHz	
	RL_{RF}	−12	dB	f_{RF} = 950 MHz	
Modulation precision	A_{ERR}	1.3	%	RMS Magnitude Error	2
	P_{ERR}	0.82	deg.	RMS Phase Error	
	V_{ERR}	1.9	%	RMS Vector Error	
Carrier suppression	CS	−34.5	dBc	—	2

• **External circuit constants (with the IC mounted on the evaluation board)**

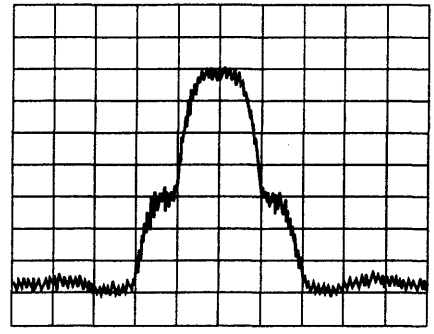


- **Modulation precision and output spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signal: RFout = 950 MHz

- **Modulation precision**



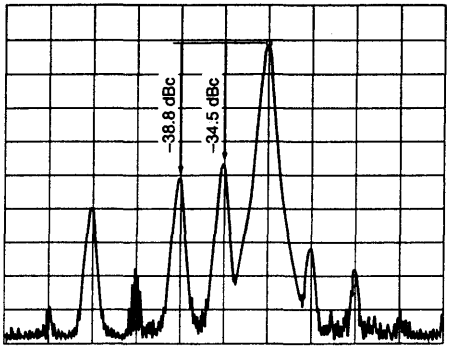
- **Output spectrum**



CENTER = 950 MHz
SPAN = 200 kHz
RBW = 3 kHz VBW = 100 Hz SWP = 3 s
ATT = 10 dB
REF = 0 dBm 10 dB/div.

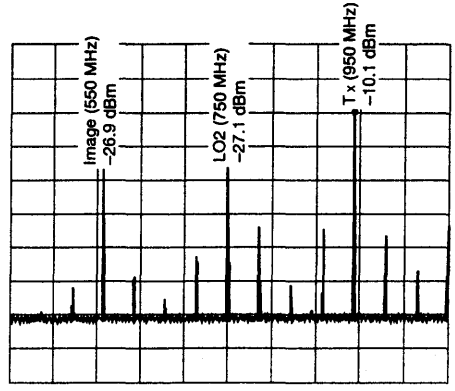
- **Spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, 0000, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signal: RFout = 950 MHz

- **Span = 240 kHz**



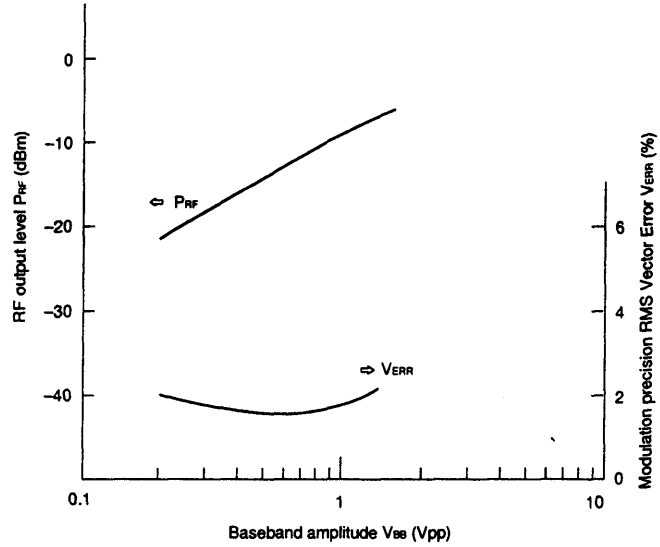
CENTER = 950 MHz
SPAN = 26.2 kHz
RBW = 300 Hz VBW = 300 Hz SWP = 1.3 s
ATT = 10 dB
REF = 0 dBm 10 dB/div.

- **Span = 700 MHz**



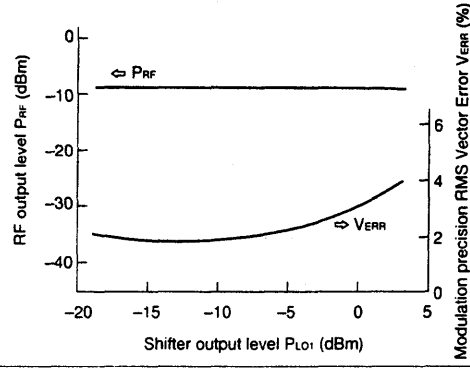
CENTER = 750 MHz
SPAN = 700 MHz
RBW = 1 MHz VBW = 3 kHz SWP = 1.1 s
ATT = 10 dB
REF = 10 dBm 10 dB/div.

- **RF output level dependent on baseband amplitude (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 950 MHz

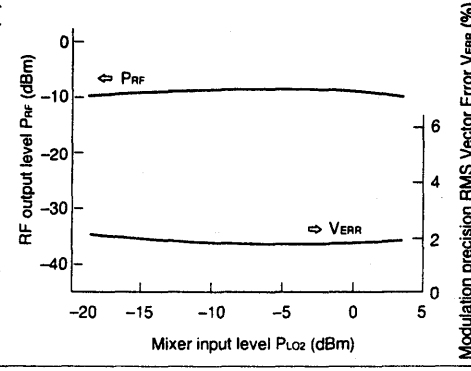


- **RF output level dependent on LO1 and LO2 input levels (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 950 MHz

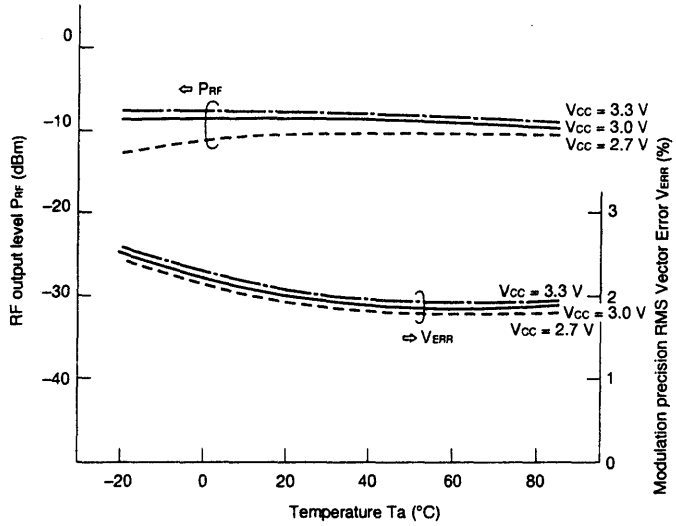
- **RF output level dependent on LO1 input level (@P_{LO2} = –5 dBm)**



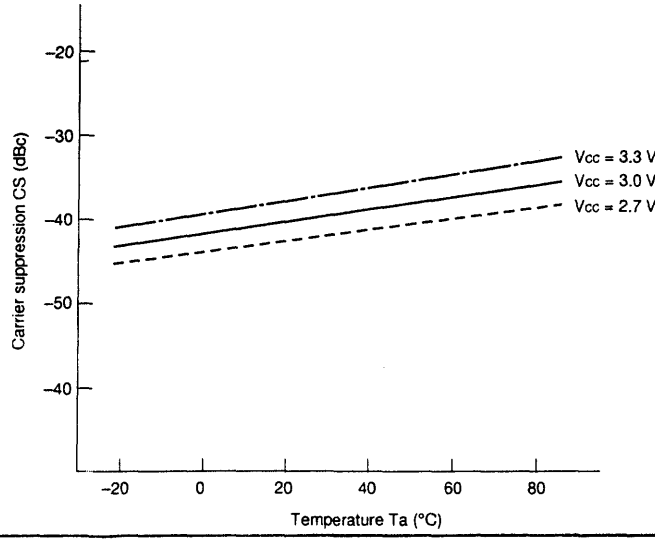
- **RF output level dependent on LO2 input level (@P_{LO1} = –15 dBm)**



- **RF output level dependent on temperature (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 950 MHz

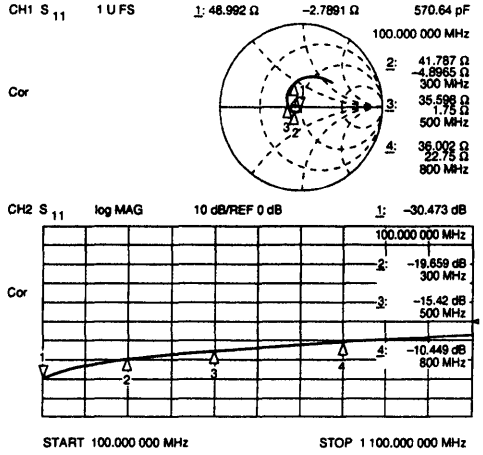


- **Carrier suppression dependent on temperature (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, 0000, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signal: RFout = 950 MHz

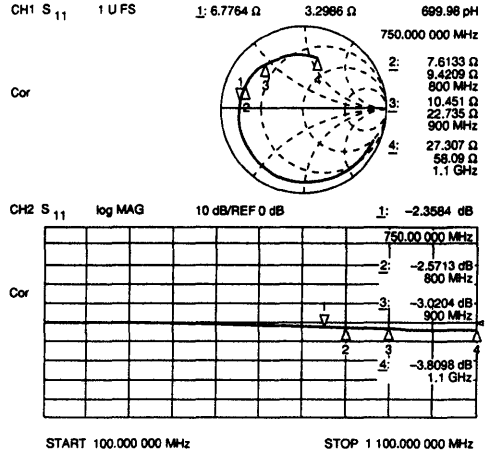


- **Input impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **LO1**

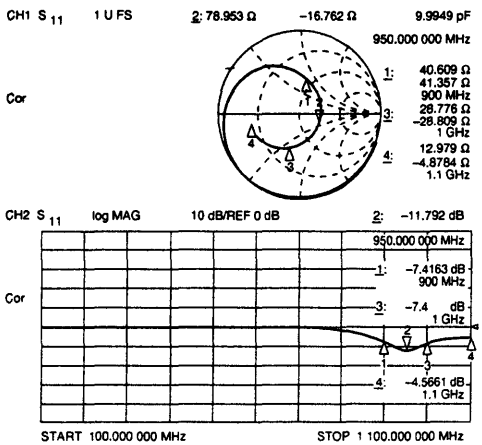


- **LO2**



- **Output impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **RFout**

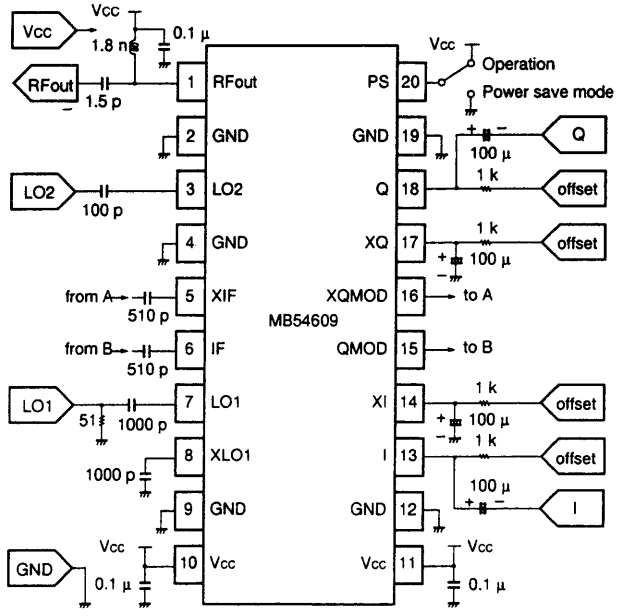


■ 1.5-GHz PDC APPLICATION MEASUREMENT DATA (Reference Values)

- **Measurement results**

Parameter	Symbol	Measurement result	Unit	Condition	Test circuit
Baseband input signal	f_{BB}	42	kbps	π/4 DQPSK, Root-Nyquist filter (α = 0.5)	—
	V_{BB}	1.0	Vpp	Single-end input	—
Shifter input signal LO1	f_{LO1}	356	MHz	—	—
	P_{LO1}	–5	dBm	—	—
Mixer input signal LO2	f_{LO2}	1619	MHz	—	—
	P_{LO2}	–5	dBm	—	—
Mixer output signal RFout	f_{RF}	1441	MHz	$f_{RF} = f_{LO2} + f_{LO1}/2$	—
	P_{RF}	–13.4	dBm	SSB value	1
Return loss	RL_{LO1}	–18	dB	f_{LO1} = 356 MHz	3
	RL_{LO2}	–6	dB	f_{LO2} = 1619 MHz	
	RL_{RF}	–14	dB	f_{RF} = 1441 MHz	
Modulation precision	A_{ERR}	1.6	%	RMS magnitude error	2
	P_{ERR}	0.90	deg.	RMS phase error	
	V_{ERR}	2.2	%	RMS vector error	
Carrier suppression	CS	–39.0	dBc	—	2

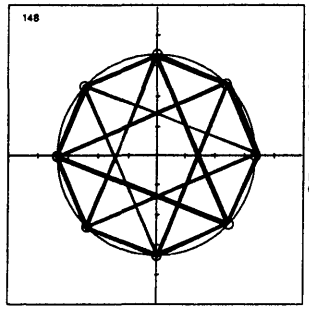
- **External circuit constants (with the IC mounted on the evaluation board)**



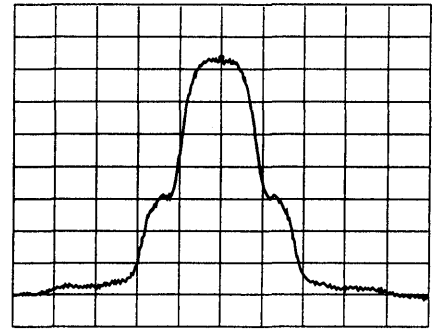
5

- **Modulation precision and output spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signal: RFout = 1441 MHz

- **Modulation precision**



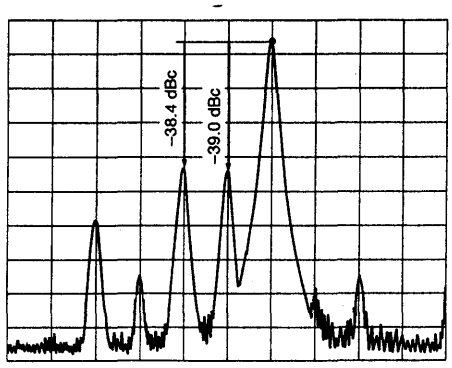
- **Output spectrum**



CENTER = 1441 MHz
SPAN = 200 kHz
RBW = 3 kHz VBW = 3 kHz SWP = 100 ms AVG = 128
ATT = 10 dB
REF = –10 dBm 10 dB/div.

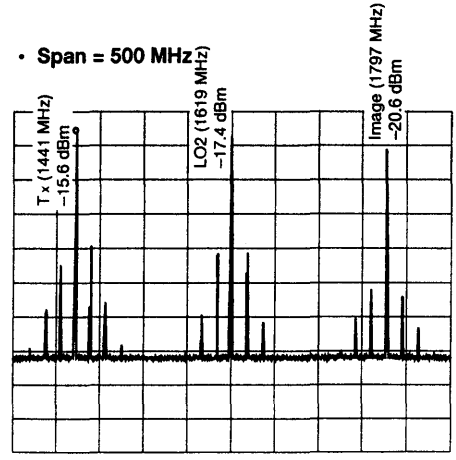
- **Spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, 0000, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signal: RFout = 1441 MHz

- **Span = 26.2 kHz**



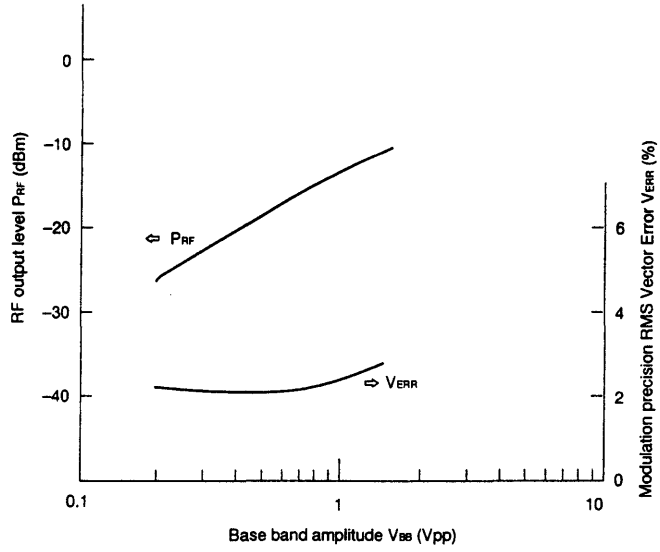
CENTER = 1441 MHz
SPAN = 26.2 kHz
RBW = 300 Hz VBW = 100 Hz SWP = 4 s
ATT = 10 dB
REF = –10 dBm 10 dB/div.

- **Span = 500 MHz**



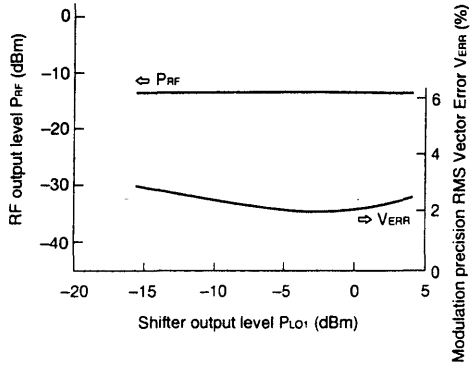
CENTER = 1619 MHz
SPAN = 500 MHz
RBW = 1 MHz VBW = 1 kHz SWP = 3 s
ATT = 10 dB
REF = –10 dBm 10 dB/div.

- RF output level dependent on baseband amplitude (P_{RF}: test circuit 1, Modulation precision: test circuit 2)
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 1441 MHz

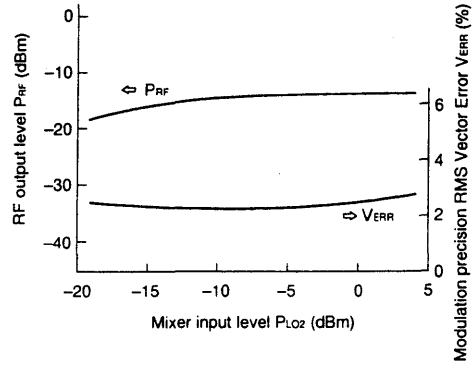


- RF output level dependent on LO1 and LO2 input levels (P_{RF}: test circuit 1, Modulation precision: test circuit 2)
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 1441 MHz

- RF output level dependent on LO1 input level ($@P_{LO2}$ = –5 dBm)



- RF output level dependent on LO2 input level ($@P_{LO1}$ = –5 dBm)



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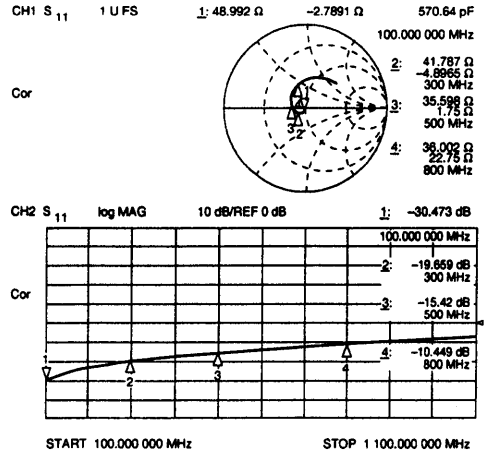
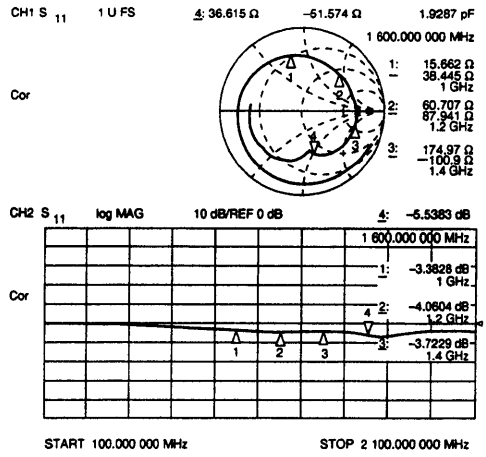
- **Input impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **LO1**

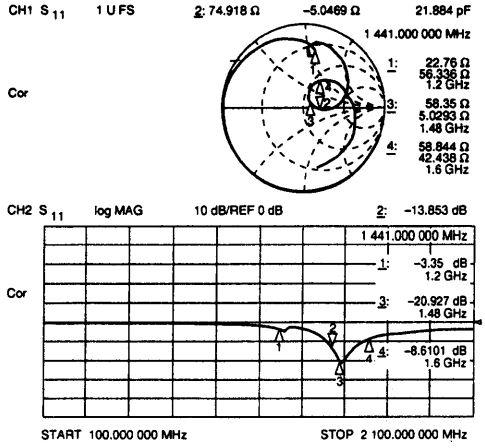


- **LO2**



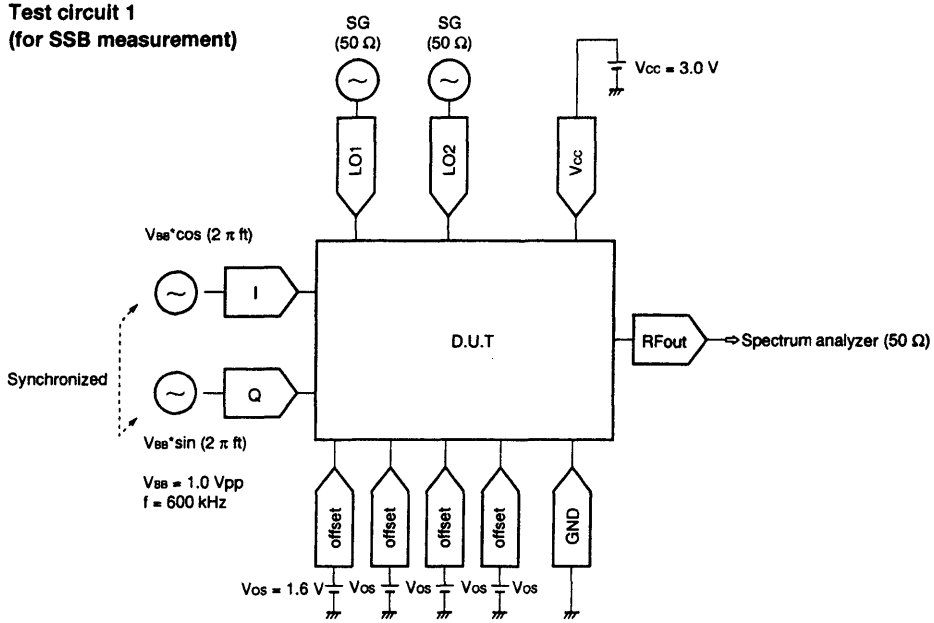
- **Output impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **RFout**

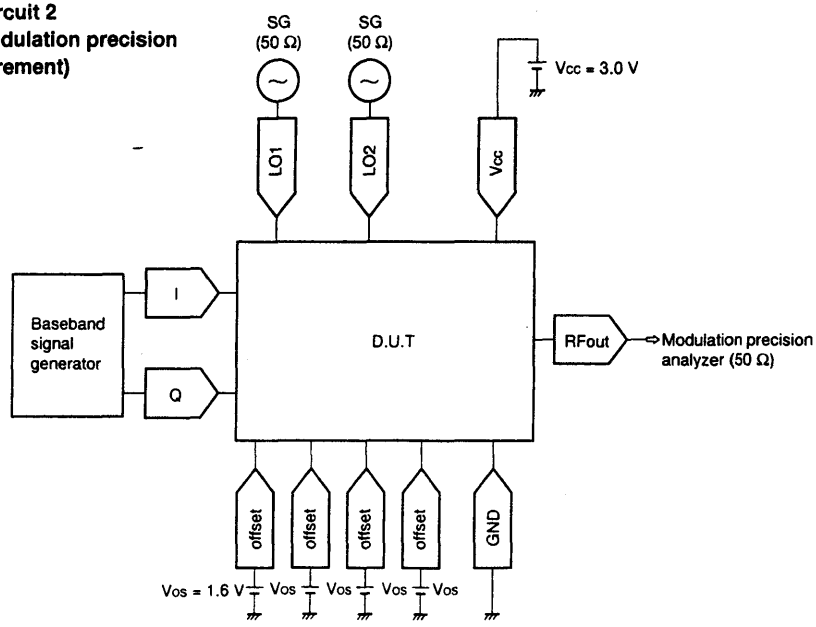


■ TEST CIRCUITS (Reference Examples)

• **Test circuit 1**
(for SSB measurement)



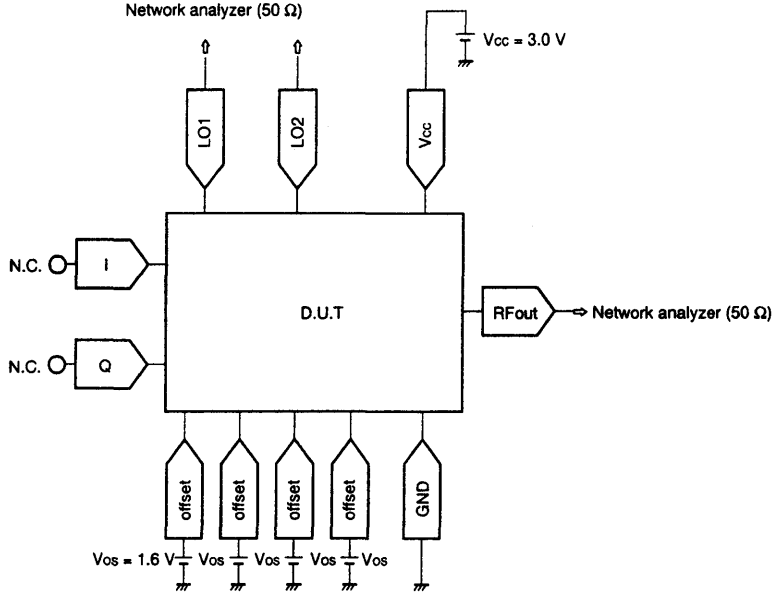
• **Test circuit 2**
(for modulation precision measurement)



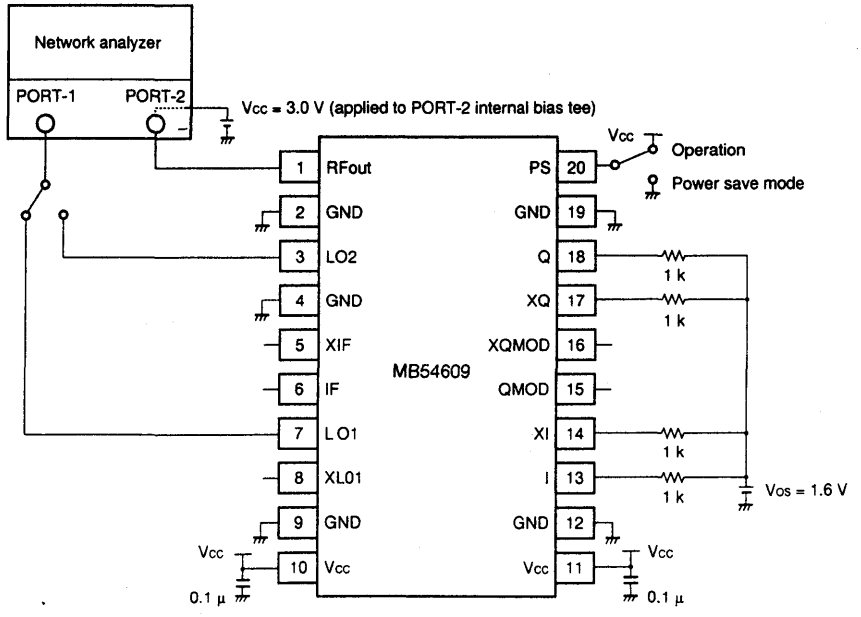
(Continued)

(Continued)

- **Test circuit 3 (for impedance measurement with components mounted)**



- **Test circuit 4 (for measurement of impedance of only IC)**



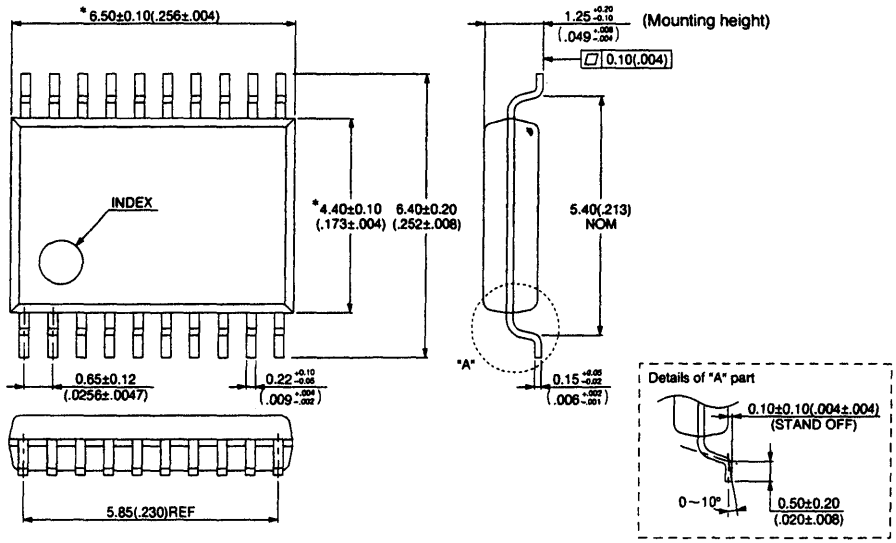
■ ORDERING INFORMATION

Part number	Package	Remarks
MB54609PFV	20-pin Plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSION

20-pin Plastic SSOP
(FPT-20P-M03)

*: These dimensions do not include resin protrusion.



Dimensions in mm (inches)

MB54619

FUJITSU

QUADRATURE MODULATOR (2.0GHz BAND UP CONVERTER BUILT IN)

INTRODUCTION

MB54619 is a quadrature modulator IC for IF modulation. The power consumption is as low as 25mA typ. because of Fujitsu's advanced technology. There is a 2.0GHz band up converter on chip that makes the MB54619 ideally suitable for high frequency mobile communications such as DECT, PCN, GSM and so on. The phase shifter is F/F type and allows a wide IF bandwidth to be achieved.

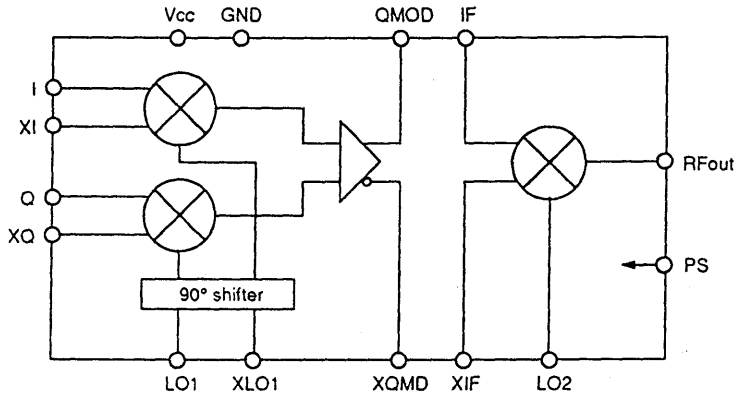
FEATURES

- High performance transmit mixer
  Output frequency : 2.0 GHz max.
  Output level : −14 dBm typ.
- Quadrature modulator and transmit mixer have external pinouts and allows for a BPF to be inserted between them.
  Quadrature modulator output can drive a 50 Ω load.
- F/F type phase shifter allows wide IF band operation
  Operating IF band : 100 MHz to 800 MHz
- Low power supply voltage : Vcc = 2.7 V to 3.3 V
- Low supply current
  Operating : 25.0 mA typ.
  Power down mode : 0.6 mA typ.
- Operating temperature : Ta = −20 °C to +75 °C
- Package : Plastic SSOP 20-pin (FPT-20P-M03)

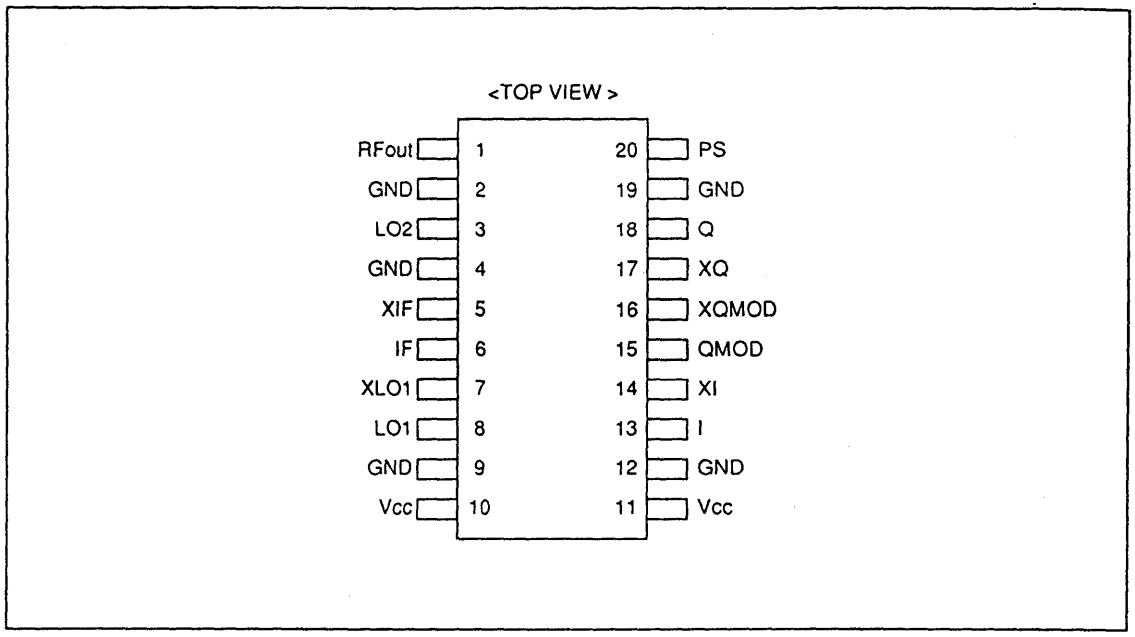
ADVANCED INFORMATION

5

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	RFout	Up converter output	11	Vcc	Power supply
2	GND	Ground	12	GND	Ground
3	LO2	Mixer LO input	13	I	Baseband input (I)
4	GND	Ground	14	XI	Baseband complementary input (I)
5	XIF	Mixer IF complementary input	15	QMOD	Q-modulator IF output
6	IF	Mixer IF input	16	XQMOD	Q-modulator IF complementary output
7	XL01	Q-modulator LO complementary input	17	XQ	Baseband complementary input (Q)
8	LO1	Q-modulator LO input	18	Q	Baseband input (Q)
9	GND	Ground	19	GND	Ground
10	Vcc	Power supply	20	PS	Power down control

ELECTRICAL CHARACTERISTICS

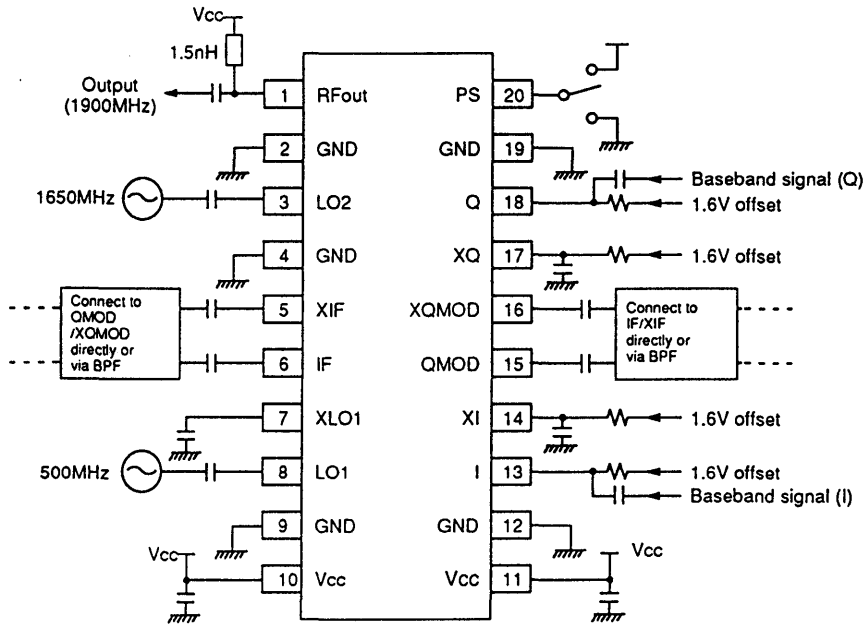
Ta = 25 °C

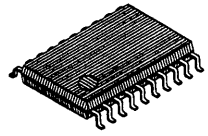
Parameter		Symbol	Target Value			Unit	Note	
			Min.	Typ.	Max.			
Power supply voltage		Vcc	2.7	3.0	3.3	V		
Power supply current		Icc		25.0		mA	DC current	
Power down current		IccPS		0.6		mA	DC current	
Shifter input LO1	Operating band	f_{LO1}	100		800	MHz		
	Input level	P_{LO1}	−15		0	dBm		
Baseband input LO2	Operating band	f_{BB}	DC		1	MHz		
	Input amplitude	V_{BB}			1.2	Vpp		
Mixer input LO2	Operating band	f_{LO2}			1900	MHz		
	Input level	P_{LO2}			−5	dBm		
Mixer output RFout	Operating band	f_{RF}			2000	MHz	$f_{RF} = f_{LO1}/2 + f_{LO2}$	
	Output level	P_{RF}		−14		dBm		Q-MOD & Mixer direct connection, BB = 1Vpp
Modulation precision	Amplitude error	A_{ERR}			2	%	RMS value	
	Phase error	P_{ERR}			1	deg.	RMS value	
	Vector error	V_{ERR}			3	%	RMS value	
Carrier suppression		CS			−30	dBc	External offset, no offset adjustment	

Note; fLO1 = 500MHz (−10dBm), fLO2 = 1650MHz (−10dBm), fRF = 1900MHz output

5

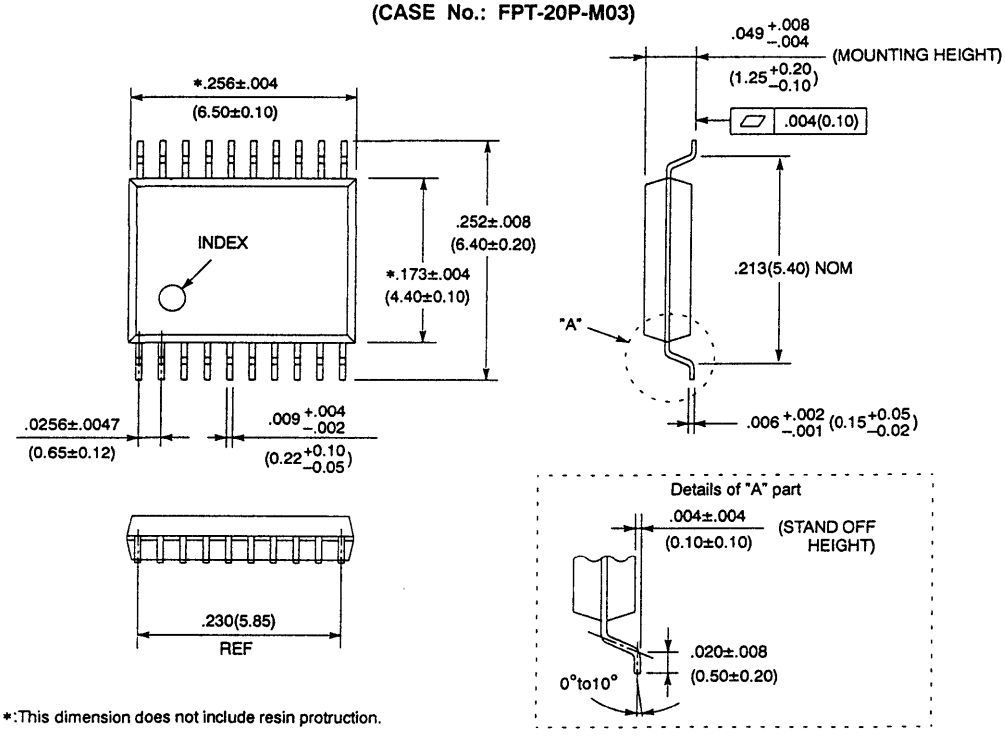
PERIPHERAL CONNECTION EXAMPLE





FPT-20P-M03

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

SECTION 6

Semi–Custom BiCMOS LSI RF Integrated Circuits – *At a Glance*

Fujitsu has an answer for those customers who wish to pursue a semi–custom solution tailored to their design needs for high volume, cost and size critical applications. Fujitsu's advanced Semi–Custom BiCMOS LSI RF IC technology is an array–based methodology used to develop both custom devices and standard devices. This means that many of the standard parts in the SuperPLL and Super Analog product lines have equivalent macros already developed for implementation in a semi–custom solution. This provides a low risk integration path from discrete solutions using standard devices for prototyping or first generation designs to complete, highly integrated solutions. Please contact your nearest Fujitsu representative for further details and engagement requirements.

Page Number	Part Number	Series Number	Frame Number
6-3	MB1520	I	FRAME I
6-3	MB1530	I	FRAME II
6-3	MB1540	I	FRAME III
6-3	MB1550	I	FRAME IV
6-31	MB54500	II	FRAME I
6-45	MB54600	III	FRAME III
6-59	MB1560	IV	FRAME I

Sept. 1995
Edition 3.0b

FUJITSU

DATA SHEET

MB1520/MB1530/MB1540/MB1550 SERIES Bi-CMOS LSI RF IC SPECIFICATION

ADVANCED SEMICUSTOM TECHNOLOGY OF SUPER PLL WITH RF SYSTEM ON LSI

The Fujitsu MB1520/1530/1540/1550 series are semicustom LSI IC's based on a master slice method. Super PLL (PLL and Prescaler) macros and high frequency analog macros, such as VCO's. IF amplifiers , RF amplifiers and mixers can be realized on a single chip in accordance with customer requests. This is achieved by means of predefined blocks (Super PLL's and analog macros) laid out on the respective frames in a number of different combinations. The performance of each block is custom specified.

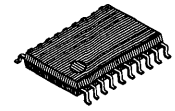
The MB1520/1530/1540/1550 series makes it possible to compose single chip silicon front ends for mobile communication systems. Due to the design process used, development cycles and cost are greatly reduced over standard full custom LSI designs, resulting in lower system cost solutions and reduced time-to-market.

Features

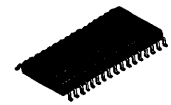
- Super PLL's as well as high frequency analog circuits, such as VCO's, mixers, RF and IF amplifiers.
- Four available frame sizes, offering various combinations of Super PLL's and analog macros.
- Choice of a wide variety of existing Super PLL's and analog functions, as well as custom specifications of the same.
- Choice of power supply voltages between 2.7V and 5.5V. (Minimum 2.0V with some restrictions available.)
- Available high speed lock up circuit for digital mobile communications such as DECT, GSM, PDC, and so on.
- A number of standard features, such as power saving modes, phase shifter circuit, analog switches, charge pumps, depending on the frame size.
- Development cycle is typically 14 weeks.

Application Examples

- MB1520 series: BS tuner, car navigation systems
- MB1530 series: MCA wireless for business use, analog cordless phones
- MB1540 series: Analog cellular phones, trunked radios
- MB1550 series: Digital cellular and digital cordless phones



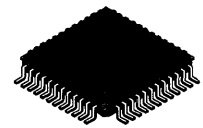
FPT-20P-M03



FPT-34P-M01

[PRINTING]

FPT-34P-M03



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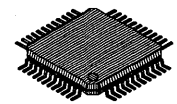
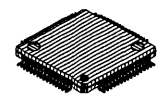


FPT-48P-M05



FPT-64P-M03

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Bi–CMOS LSI RF IC SERIES

Master-slice methodology is that wafers of a particular frame are prefabricated as much as having finished diffusion processes, forming the basic elements, such as transistors, resistors and capacitors. The remaining contact and wiring process steps then determine and configure the function and value of each element according to cases.

This series is based on a master-slice method for which predefined blocks are laid out. Four series, MB1520/1530/1540/1550 are available in accordance with combinations of the predefined blocks. (Please refer to "Chip Layout".) Table 1 shows representative blocks and features of each series.

Table 1. SERIES

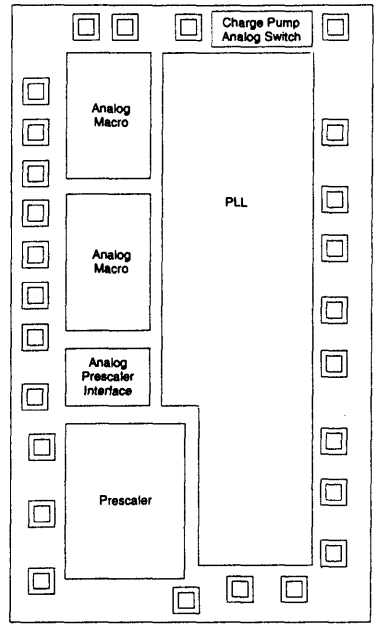
Series Name	Prescaler	PLL	Analog Macro	Operating Frequency (max.)	Package		
					SSOP	QFP	SQFP
MB1520	1 circuit	1 circuit	2 circuits	2.4GHz	20-pin	–	–
MB1530	2 circuits	2 circuits	4 circuits	1.9GHz	34-pin	–	–
MB1540	2 circuits	2 circuits	6 circuits	2.4GHz	–	48-pin	48-pin
MB1550	3 circuits*	3 circuits	8 circuits	2.4GHz	–	48-pin	64-pin

* 1 Prescaler or 90° phase shifter

CHIP LAYOUT

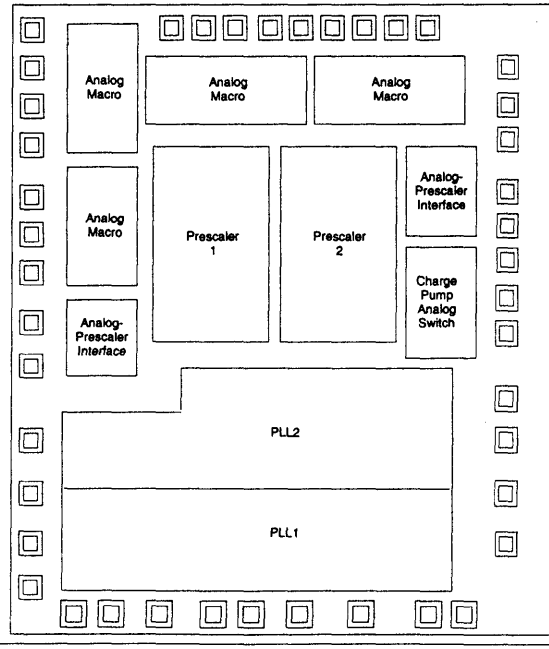
MB1520 Series

1 Prescaler
1 PLL
2 Analog Macros



MB1530 Series

2 Prescaler
2 PLL
4 Analog Macros

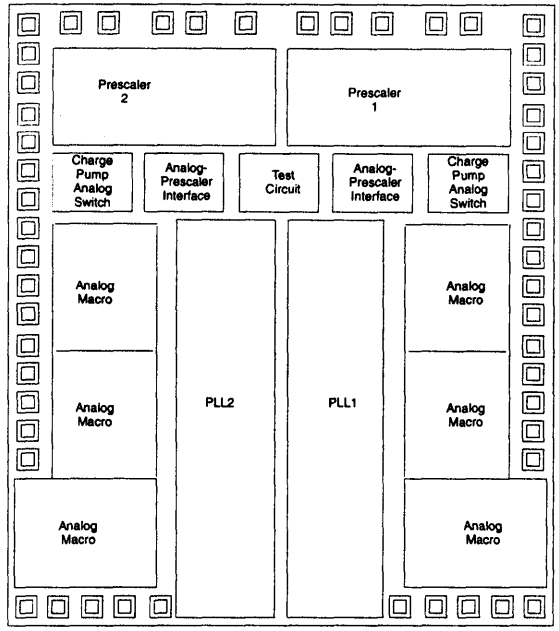


6

CHIP LAYOUT (Continued)

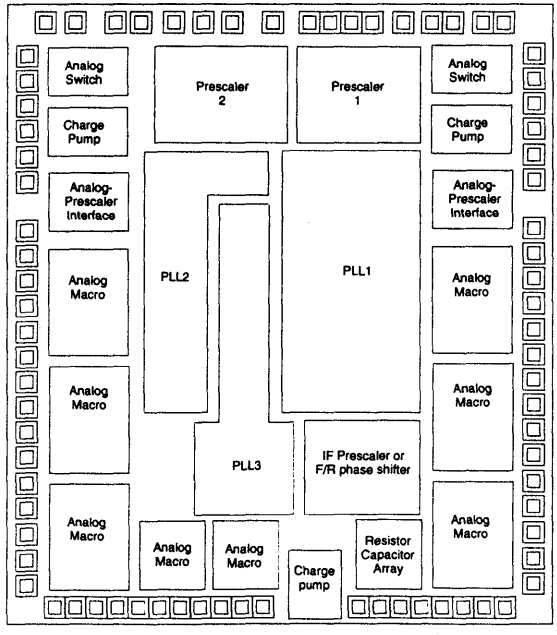
MB1540 Series

2 Prescaler
2 PLL
6 Analog Macros



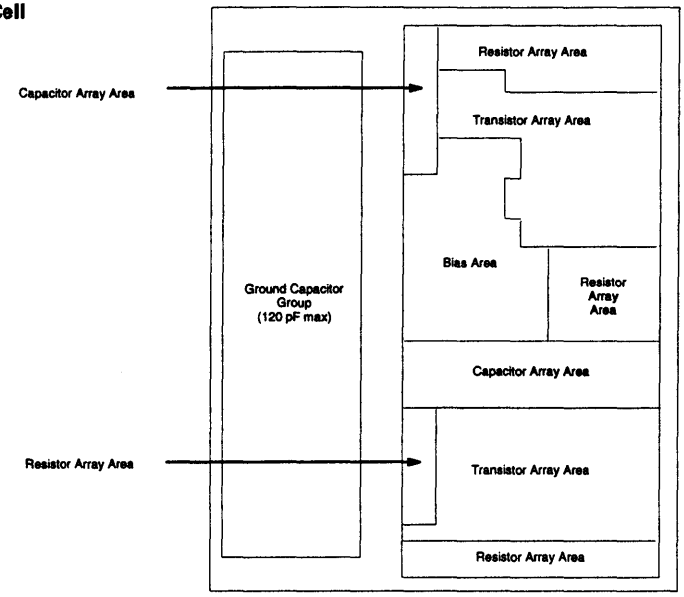
MB1550 Series

2 Prescaler
3 PLL
8 Analog Macros
1 Prescaler or
90° phase shifter



CHIP LAYOUT (Continued)

Analog Cell



6

ABSOLUTE MAXIMUM RATINGS

(Reference voltage is GND.)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	I_{OUT}	±10	mA
Ambient Temperature	T_{STG}	−50 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

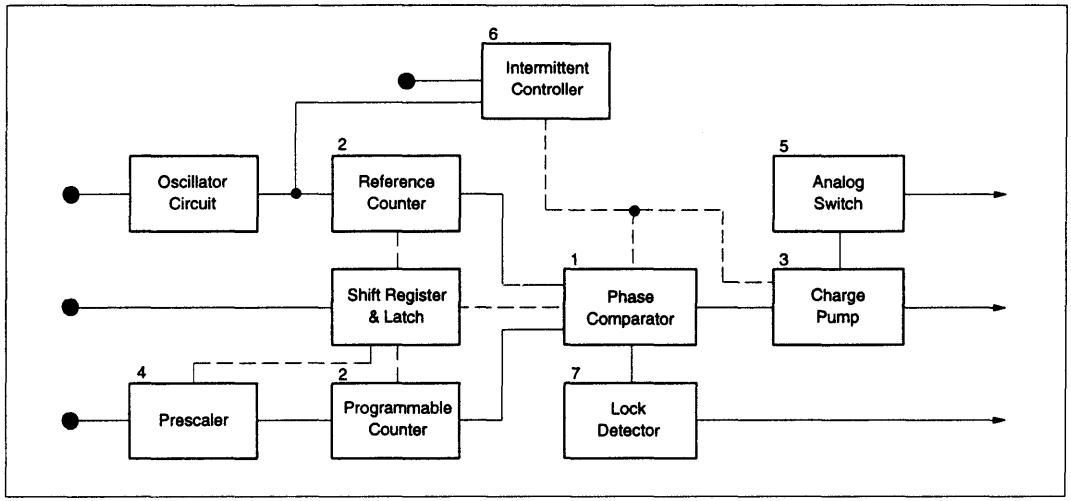
(Reference voltage is GND.)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	2.7*		5.5	V
	GND		0		V
Ambient Temperature	T_A	−40		+85	°C

* The minimum operating voltage is at 2.0V, but some restriction may be required.

MACRO CELLS DESCRIPTIONS

1. Super PLL (PLL and Prescaler)



1.1 Functional Descriptions

In designing "super PLL block", some functions may be restricted depending on kind of series (MB1520/1530/1540/1550). Availability of main functions is summarized in Table 2.

1. **Phase comparator**
   Phase difference detection range is -2π (pi) to $+2\pi$ (pi). In order to minimize the dead zone area, the phase comparator is designed to deliver a minimum signal to the charge pump even when the phase difference is zero. Also, it is possible to choose the characteristics of the phase comparator to meet polarity of VCO.
2. **Counter (Reference Counter and Programmable Counter)**
   Two types of counters are available for PLL1 and PLL2 of all series : programmable and fixed
   Regarding PLL3, one type of counter is available : Fixed
3. **Charge pump**
   All charge pumps are based on bipolar technology. Their voltage levels at "H" depend on the power supply voltage chosen. It is possible to optimize charge pump characteristics individually according to customer needs.
   - High speed lock up circuit
     This circuit is an option to further increase the lock up time of the PLL, and is available for PLL1 and PLL2 (except PLL3). It will mainly be required in the new emerging digital communication standards.
4. **Prescaler**
   Divide ratio can be chosen freely, so can two modulus type and fixed type. However, regarding PLL3, only fixed type is available and the divide ratio can be chosen from 1/2, 1/4, and 1/8.

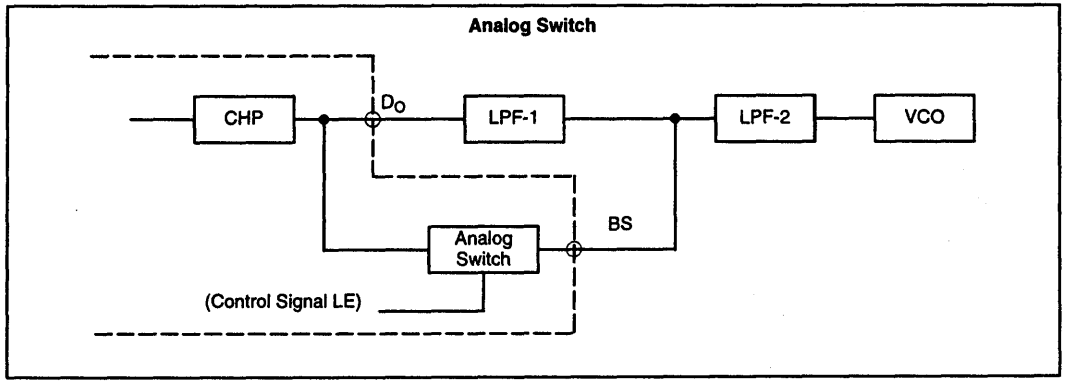
Table 2. SUPER PLL FUNCTION TABLE

		Prescaler	Programmable Counter	Reference Counter	High Speed Lock Up Function	Power Save Mode
MB1520	PLL1	T	P/F	P/F	X	X
MB1530	PLL1	T	P/F	P/F*	X	X
	PLL2	T	P/F		–	–
MB1540	PLL1	T	P/F	P/F	X	X
	PLL2	T	P/F	P/F	–	X
MB1550	PLL1	T	P/F	P/F	X	X
	PLL2	T	P/F	P/F	X	X
	PLL3	S	F	F	–	X

NOTE: T: Two Modulus S: Single Modulus (1/2, 1/4, or 1/8) P/F: Programmable or Fixed F: Fixed X: Available
*: Common for PLL1 and 2

5. Analog switch

This switch is controlled by the LE signal. When LE is at "H", the analog switch is closed (ON). In this mode, the charge pump output (D_O) is fed in parallel to the pin BS. This decreases the time constant of the loop filter and reduces the charge pump load. The result is an increased lock up speed.



6. Intermittent operation control circuit

The intermittent operation reduces the power consumption by powering down or waking up parts of the PLL circuitry. All the transmission, the reception and IF block PLL may be controlled by this circuit.

If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between the reference frequency (fn) and the comparison frequency (fp) and may in the worst case take longer time for lock up of the loop.

To prevent this, the intermittent operation control circuit forces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

The circuit can be controlled externally or internally, depending on customer requirements. If controlled externally, the circuit is activated by an external signal to the PS pin. If controlled internally, the intermittent control circuit follows the power state set by the analog cells. When the power supply for the analog cells is shut down, the stand by state is automatically selected. When the analog cells are supplied with power, the active state is selected.

The charge pump output is in a high impedance state during stand by, so that the VCO control voltage is being clamped at the active state level.

During the stand by state, the latches store the data which they hold at the time of power down. The shift register data, on the contrary, may be renewed during stand by.

NOTE: Powering up for the digital blocks (V_{CCRD}, V_{CCTD}), (after they are disconnected) has to be done in stand by mode.

Table 3. STANDARD STAND BY STATE OF PLL BLOCK

		Circuit State	
		Active Mode	**Stand By Mode**
Rx	Reception circuits	X	PD
	Oscillator circuit	X	X*
	Reference counter	X	–
Tx	Transmission circuits	X	PD
	Oscillator circuit	X	X
	Reference counter	X	–
IF	IF circuits	X	PD
	Oscillator circuit	X	X
	Reference counter	X	–

NOTE: X: Active state PD: Power down mode –: Stop working
*: Oscillator circuit can be stopped in accordance with PK's PD signal.

7. **Lock detector circuit**

LD output is selected by setting the "T" bit. (See 1.2 Serial data format.)
When the phase difference is equal or higher than tw (see diagram below), LD goes into "L". When the phase difference is tw or less and continues to be so for three cycles or more, the LD goes into "H". For example, in case of a 12.8MHz oscillator frequency tw, is 625ns to 1250ns. The relation between LD and PLL circuit is shown in Table 4.

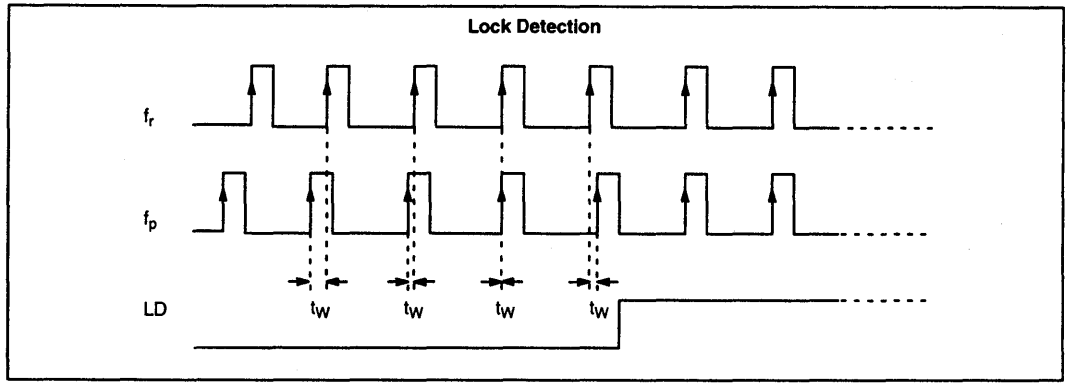


Table 4. RELATIONSHIP BETWEEN LD SIGNAL AND THE CIRCUIT STATE

Operation Mode	PLL circuit	LD Output
Stand-by	Stand-by	L
Active	Unlock	L
	Lock	H

1.2 Serial Data Format

The PLL operation is controlled by serial data inputs. The parameters of the serial data are shown below. The data input starts with the MSB bit. The data length may vary between 22 and 37 bits. The actual data format is being worked out with the customer.

Table 5. SERIAL DATA FORMAT

Name		Function	Typical Bit Number
Control Bit (CNT bit)		Selects direction of data transfer (Rx or Tx)	1 to 2
LD Select Bit (T bit)		Selects the LD output	1 to 2
FC Bit (F bit)		Switches phase of the comparator	1
Programmable Counter Bit (N bit)		Sets programmable counter's divide ratio	11
Swallow Counter Bit (A bit)		Sets swallow counter's divide ratio	7
Reference Counter Bit (R bit)	Fixed	Sets reference counter's divide ratio	1 to 2
	Programmable	Sets reference counter's divide ratio	14

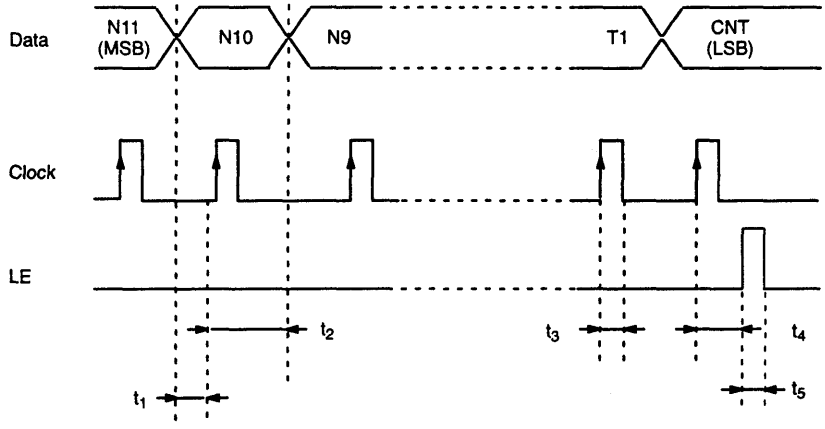
1.3 Serial Data Input Timing

Binary data is entered using the Data, Clock, and LE pins. The serial data separately controls the programmable reference divider as well as the programmable divider.

Each data bit is shifted into the internal shift register at the rising edge of each clock pulse. When the LE pin is "H", stored data is transferred from the shift register into the latch, chosen by the control bit. A schmitt trigger at each input improves noise immunity.

NOTE: 1. One clock pulse always shifts one data bit into the shift register, even during stand by state.
2. Input voltages (Data, Clock, and LE pins) should always be lower than Vcc.

Serial Data Input Timing



t1: Data set up time (≥ 1 µsec)
t2: Data hold time (≥ 1 µsec)
t3: Clock pulse width (≥ 1 µsec)
t4: LE set up time to the rising edge of the last clock (≥ 1 µsec)
t5: LE pulse width (≥ 1 µsec)

Notes: 1. One bit of data is shifted into the shift register on the rising edge of the clock (edge trigger).
2. Data in the shift register is transferred to the latch when LE becomes H.

6

2. Mixer, IF Amplifier

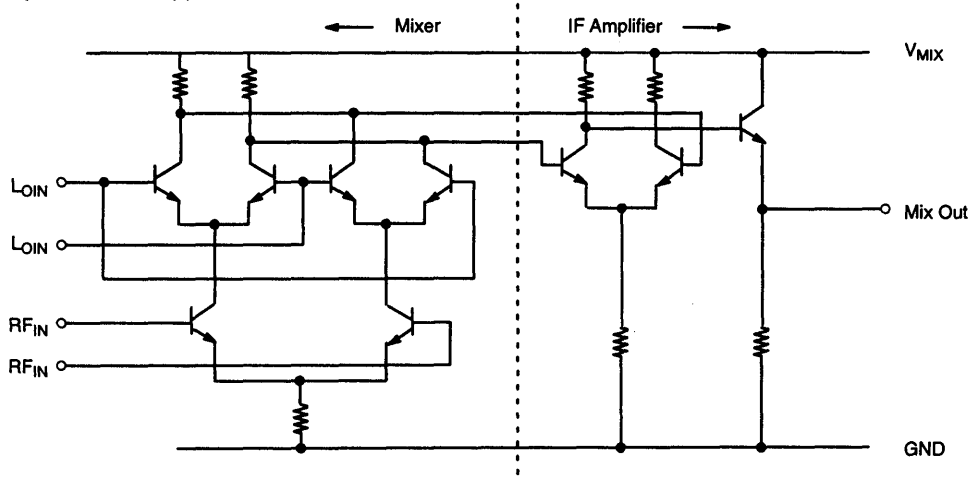
Some basic examples for achievable circuits are shown below. However, concerning circuitry and performance, it is possible to configu each analog macro cell to customer requirements.

2.1 Basic Construction

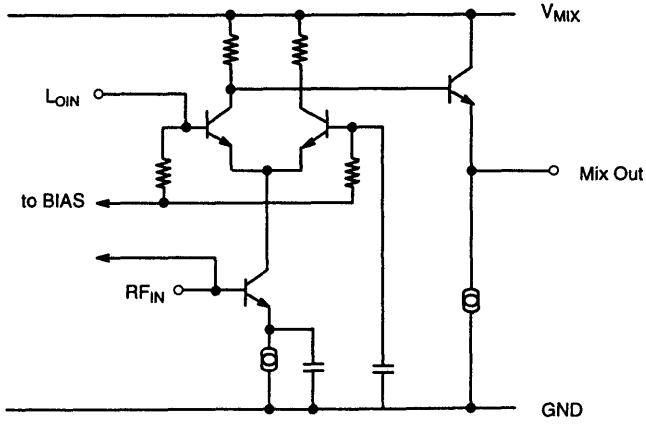
Mixer circuit can either be of DBM (Doubled Balanced Mixer) or SBM (Single Balanced Mixer) type. LO and RF inputs can be connected with the internal bias circuit, if necessary. The mixer output is connected with its own power supply (V_{MIX}) via a load resistor, then connected with the following IF amplifier.

The IF amplifier consists of a differential amplifier and NPN transistor, which forms the emitter follower output.

Basic Equivalent Circuit (1)



Basic Equivalent Circuit (2)

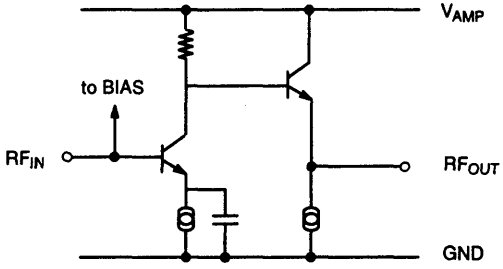


3. RF Amplifier

3.1 Basic Construction

The output signal from the common emitter circuit will be supplied though an emitter follower.

Basic Equivalent Circuit

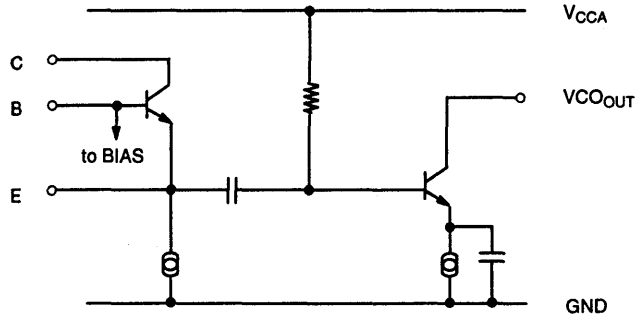


4. VCO

4.1 Basic Construction

The VCO circuit consists of an output buffer transistor and an oscillation transistor, which construct a base grounded colpitts circuit. Resonator and varicap can't be integrated in the chip, so they need to be connected externally.

Basic Equivalent Circuit



EXAMPLES OF AN ANALOG CIRCUIT'S BASIC CHARACTERISTICS

VCO

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Operating Frequency			400	MHz	
C/N		70		dB	Offset frequency = 25kHz, BW = 15kHz
S/N		50		dB	
Output Power		–5		dBm	
Mod Sense		3		MHz/V	

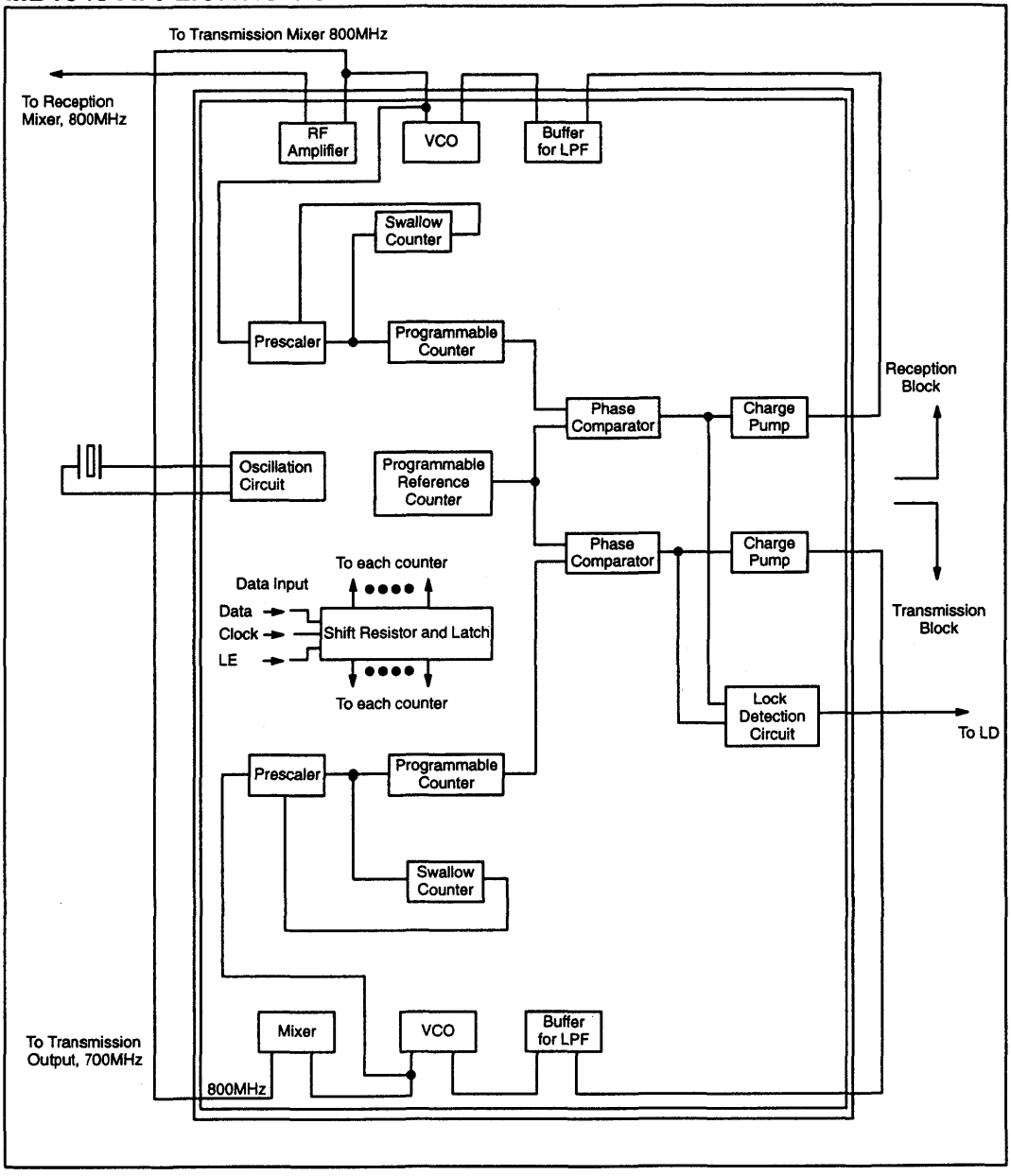
Mixer

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Gain		13		dB	
Maximum Output Power		–5		dBm	
1 dB Compresssion Point		–10		dBm	Output level
Intercept Point		–16		dBm	Input level
Noise Figure		10		dB	DSB measurement
RF-L_O Isolation		20		dB	

Amplifier

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Operating Frequency		400		MHz	
Gain		20		dB	f = 400MHz (small signal input)
Maximum Output Power		–3		dBm	f = 400MHz
1 dB Compresssion Point		–10		dBm	f = 400MHz, Output level
Intercept Point		–19		dBm	f = 400MHz, 400.1MHz, Input level
Noise Figure		3		dB	f = 400MHz

MB1540 APPLICATION CIRCUIT EXAMPLE



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DEVELOPMENT PROCEDURE

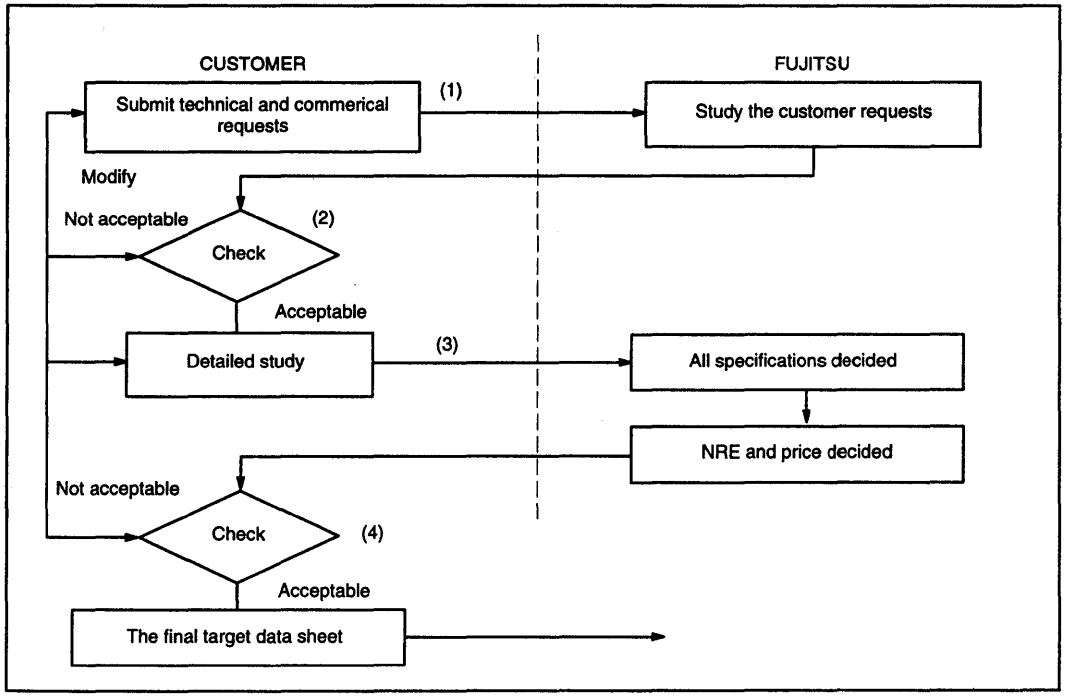
1. Study about product development

(1) The customer submits technical and commercial requests to Fujitsu. Fujitsu reviews the customer requirements, if necessary simulation is done.
[Technical request]
Function: Functional descriptional material, I/O signal descriptional material, Block diagram, etc.
Specifications: Prescaler, PLL, VCO, Mixer, Amplifier, etc.
[Commercial request]
Delivery and price: Development schedule, development assignment plan, demand, NRE, target price, etc.

(2) Fujitsu submits a counter proposal. And the final target specification evolves from the discussions about proposal/counter proposals between the customer and Fujitsu.

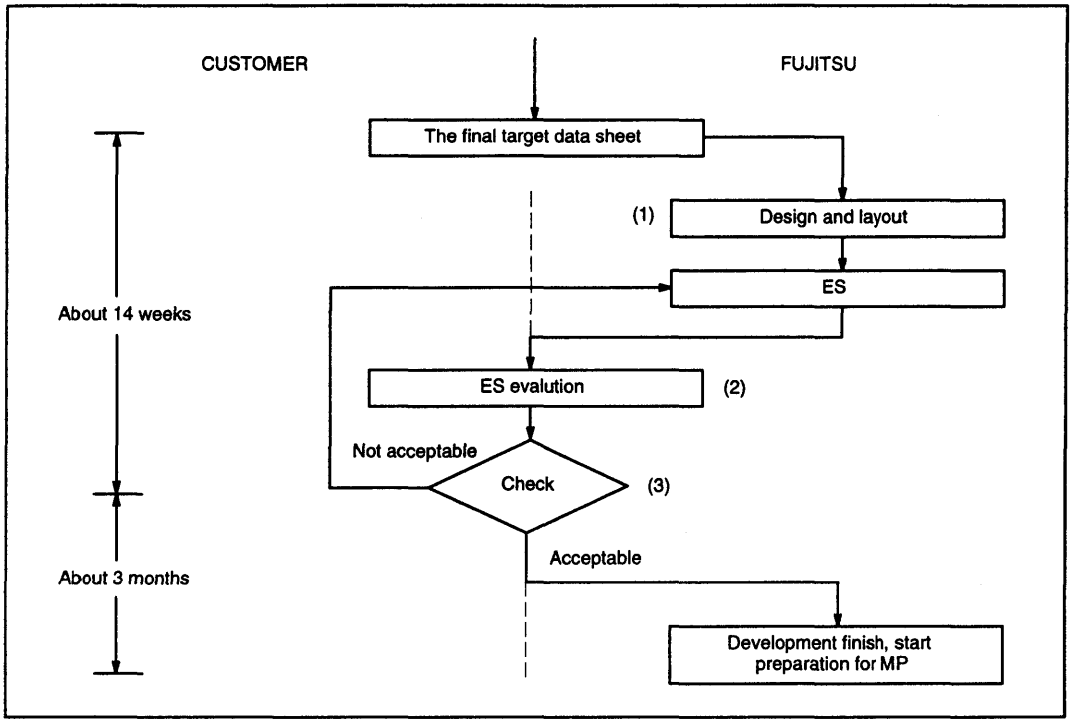
(3) Detailed circuit and test specifications are studied. Then all of the specifications are decided. After that development schedule, NRE, quotation are estimated formally.

(4) After the customer and Fujitsu agree to develop the device, the final specification (data sheet) is submitted to the customer to confirm the specification.



2. Development of IC

(1) Design and layout of the chip starts. First engineering samples become available approximately 14 weeks after the final target data sheet is issued.
(2) ES is evaluated by the customer and Fujitsu.
(3) The final specification sheet of finished product is submitted to the customer from Fujitsu when the customer is satisfied with evaluation result. Then, preparation for mass production is started. Typically 3 months are necessary for the first shipment from when the final specification sheet (for finished products) is issued.



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TARGET SPECIFICATION BLANK

MB1520 Series

Parameter		Symbol	Request Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Current		I_{CCD}				mA	Digital section
		I_{CCA}				mA	Analog section
Power Supply Voltage		V_{CCO}				V	Digital section (PLL, Prescaler)
		V_{CCA}				V	Analog section (VCO)
VCO	Operating Frequency Range	f_{VCO}				MHz	
	Output Power	P_{OUT}				dBm	
	C/N Ratio	C/N				dB	Detuning Δ f :_____kHz Bandwidth: _____kHz
	S/N Ratio	S/N				dB	Reference deviation:_____kHz/dev Bandwidth: _____kHz to _____kHz
	Mod Sense	Δf_{VCO}				MHz/V	Control voltage V_T:_____ to_____V
RF-Amp	Operating Frequency Range	f_{AMP}				MHz	
	Gain	Gain				dB	
	Noise Figure	NF				dB	
	Intercept Point	IP_3				dBm	Input level
	1 dB Compression Point	CP				dBm	Output level
	In-out Isolation	I_{SO}				dB	

MB1520 Series (Continued)

Parameter		Symbol	Request Value			Unit	Note
			Min.	Typ.	Max.		
Mixer	Operating Frequency	f_{RF}				MHz	
		f_{LO}				MHz	
		f_{IF}				MHz	Output frequency
	Gain	GAIN				dB	
	Noise Figure	NF				dB	Measurement method; SSB or DSB measurement value
	Intercept Point	IP_3				dBm	Input level
	1 dB Compression Point	CP				dBm	Output level
	LO-RF Isolation	I_{SO}				dB	
PLL	Oscillation Frequency	f_{OSC}				MHz	Comparison frequency: f_r = _____kHz
	Lock-up Time	T_{LR}				ms	Step frequency: Δf = _____kHz

Memo:

6

* If you have any questions, please fill in the above "Memo" column.

Customer name:

Application:

ES request day:

CS request day:

Planning quantity:

TARGET SPECIFICATION BLANK

MB1530/MB1540 Series

Parameter		Symbol	Request Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Current		I_{CCR}				mA	Reception section
		I_{CCT}				mA	Transmission section
Power Supply Voltage		V_{CCD}				V	Digital section (PLL, Prescaler)
		V_{CCA}				V	Analog section (VCO)
TX-VCO	Operating Frequency Range	f_{VCO}				MHz	
	Output Power	P_{OUT}				dBm	
	C/N Ratio	C/N				dB	Detuning Δ f :_____kHz Bandwidth: _____kHz
	S/N Ratio	S/N				dB	Reference deviation:_____kHz/dev Bandwidth: _____kHz to _____kHz
	Mod Sense	Δf_{VCO}				MHz/V	Control voltage V_T:_____ to_____V
RX-VCO	Operating Frequency Range	f_{VCO}				MHz	
	Output Power	P_{OUT}				dBm	
	C/N Ratio	C/N				dB	Detuning Δ f :_____kHz Bandwidth: _____kHz
	S/N Ratio	S/N				dB	Reference deviation:_____kHz/dev Bandwidth: _____kHz to _____kHz
	Mod Sense	Δf_{VCO}				MHz/V	Control voltage V_T:_____ to_____V
RF-Amp	Operating Frequency Range	f_{AMP}				MHz	
	Gain	Gain				dB	
	Noise Figure	NF				dB	
	Intercept Point	IP_3				dBm	Input level
	1 dB Compression Point	CP				dBm	Output level
	In-out Isolation	I_{SO}				dB	

MB1530/MB1540 Series (Continued)

Parameter		Symbol	Request Value			Unit	Note	
			Min.	Typ.	Max.			
Mixer	Operating Frequency	f_{RF}				MHz		
		f_{LO}				MHz		
		f_{IF}				MHz	Output frequency	
	Gain	GAIN				dB		
	Noise Figure	NF				dB	Measurement method; SSB or DSB measurement value	
	Intercept Point	IP_3				dBm	Input level	
	1 dB Compression Point	CP				dBm	Output level	
	LO-RF Isolation	I_{SO}				dB		
PLL	Oscillation Frequency	f_{OSC}				MHz	Comparison frequency: f_r = _____kHz	
	Lock-up Time	T_{LR}				ms	Reception	Step frequency; Δf = _____kHz
		T_{LT}				ms	Transmission	
Memo:								

* If you have any questions, please fill in the above "Memo" column.

Customer name:

Application:

ES request day:

CS request day:

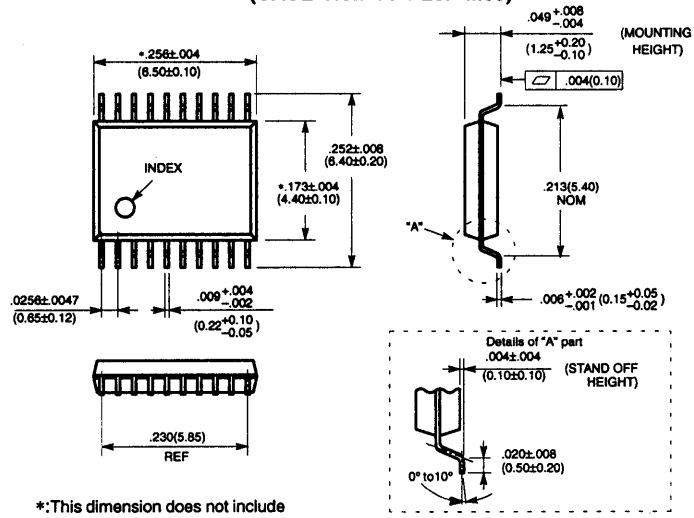
Planning quantity:

6

PACKAGE DIMENSIONS

MB1520 Series

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



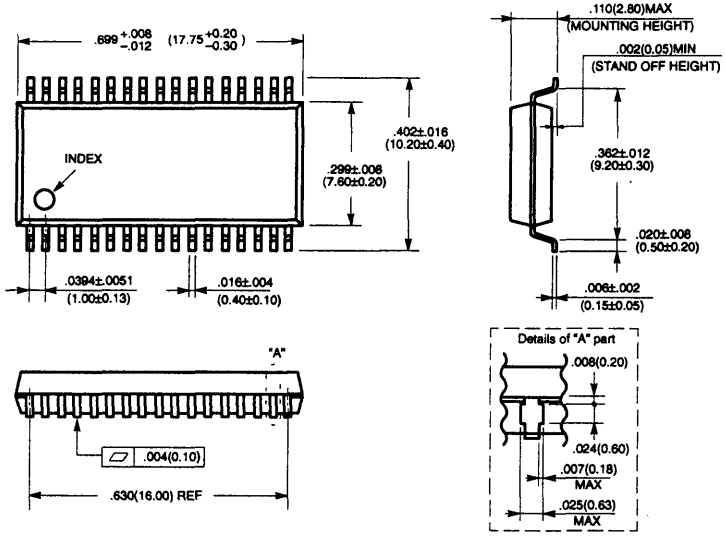
*:This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

MB1530 Series

34-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-34P-M01)



Dimensions in
inches (millimeters)

6

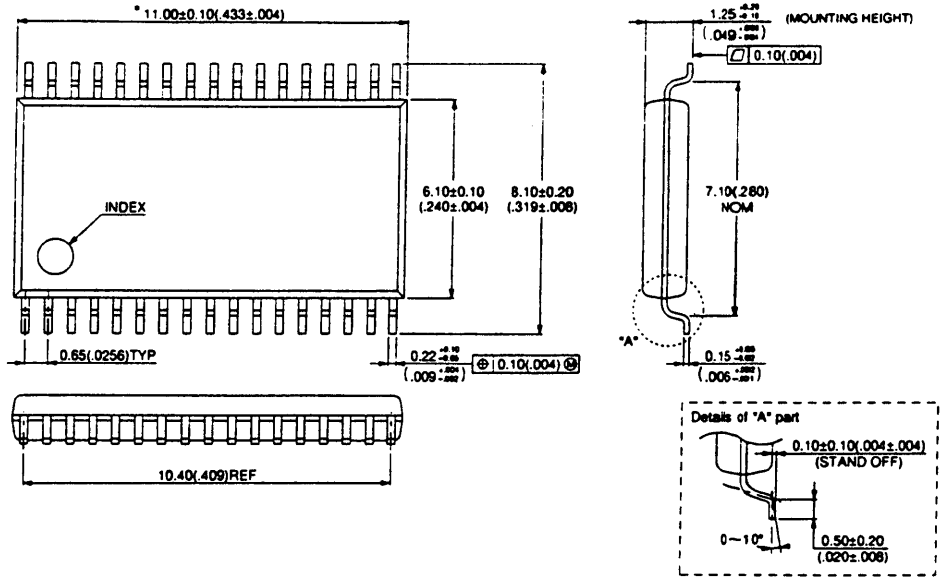
PACKAGE DIMENSIONS (Continued)

MB1530 Series

34-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-34P-M03)

34 pin Plastic SSOP
(FPT-34P-M03)

* : This dimension does not include resin protraction.

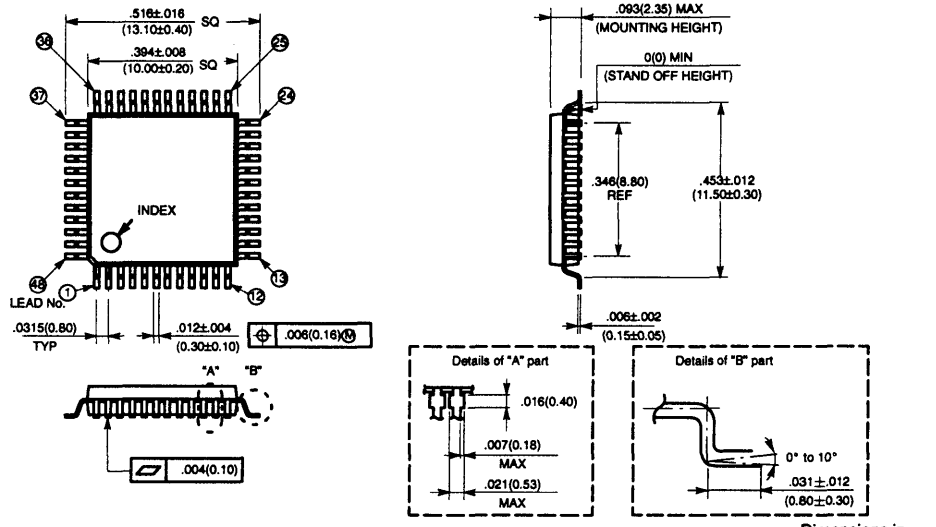


Dimensions in mm (inches)

PACKAGE DIMENSIONS (Continued)

MB1540 Series
MB1550 Series

48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M04)



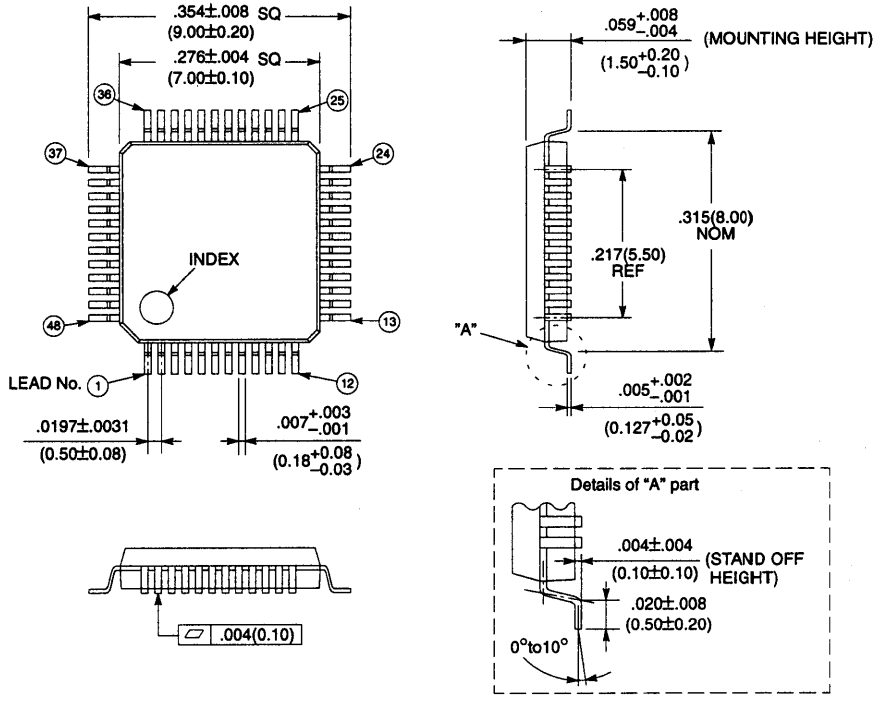
Dimensions in inches (millimeters)

6

PACKAGE DIMENSIONS (Continued)

MB1540 Series

48-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-48P-M05)

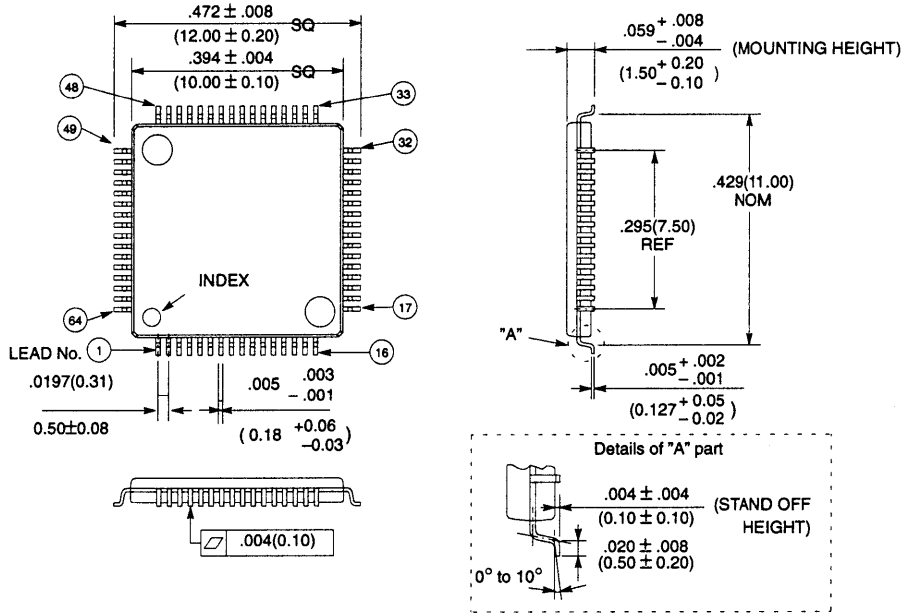


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

MB1550 Series

64-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-64P-M03)



Dimensions in inches (millimeters)

6

January 1994
Edition 1.0

FUJITSU

DATA SHEET

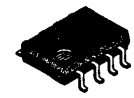
MB54500 SERIES

Bi-CMOS LSI RF IC

ADVANCED SEMICUSTOM TECHNOLOGY FOR RF SYSTEM INTEGRATION ON LSI

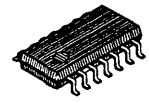
PRELIMINARY

This FUJITSU Series is a semicustom LSI IC based on a master slice method, and is ideally suitable for high frequency analog circuits such as VCO, MB54500 series involves two analog macros, such as VCO's, IF amplifiers, RF amplifiers, and mixers can be realized on a single chip in accordance with customer requests. This is achieved by means of predefined blocks (analog macros) laid out on the frame. The performance of each block is custom specified.
The MB54500 achieves low power dissipation by Fujitsu's advanced technology. Very small flat packages, smallest I/O 8-pin SSOP, are available for this LSI.

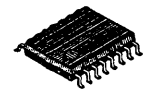


FPT-8P-M01

FPT-8P-M03



FPT-14P-M04



FPT-16P-M05

FEATURES

- High frequency analog circuits for front-end section, such as VCO's, mixers, RF and IF amplifiers can be realized.
- Choice of a wide variety of exsisting and analog functions, as well as custom specifications of the same.
- Maximum operating frequency is at 2GHz.
- Choice of power supply voltages between 2.7V and 5.5V.
- Development cycle is typical 12 weeks.
- Very samll package is available, SSOP 8-pin.
- Power saving circuit can be involved.

ABSOLUTE MAXIMUM RATINGS

(Reference voltage level is GND.)

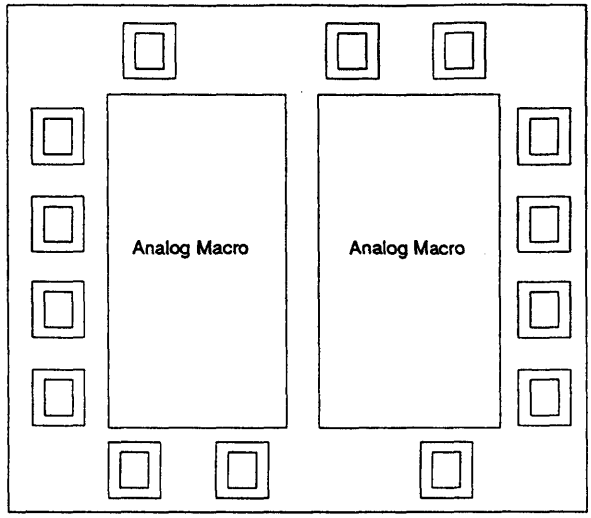
Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to Vcc+0.5	V
Output Current	I_{OUT}	±10	mA
Ambient Temperature	T_{STG}	−50 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

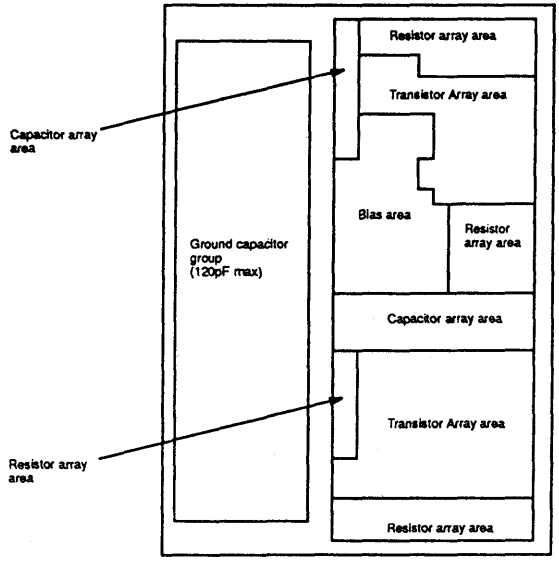
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CHIP LAYOUT

MB54500 Series



Analog cell



MACRO CELLS DESCRIPTIONS

1.High frequency analog cells

1.1 Mixer

Double balanced mixer of active type.

1.2 IF amplifier

IF amplifier consist of a differential amplifier and NPN transistor. Differential amplifier outpt is emitter follower type.

1.3 RF amplifier

Output signal of grounded emitter circuit is emitter follower output. RF input can be connected internal bias circuit.

1.4 VCO

The VCO consists of an output buffer's transistor and an oscillation's transistor which constructs an oscillator circuit of base grounded colpitts. Resonator, varicap and so on are connected externally.

Note;

Circuit design and so on can be optimized in accordance with customer needs.

RECOMMENDED OPERATING CONDITIONS

(Reference voltage level is GND.)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	2.7		5.5	V
	GND		0		V
Ambient Temperature	T_A	–40		+85	°C

ANALOG CIRCUITS BASIC CHARACTERISTICS EXAMPLE

1.VCO

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Operating Frequency			400	MHz	
C / N		70		dB	Offset frequency = 25kHz, BW = 15 kHz
S / N		50		dB	
Output Power		–5		dBm	
Mod Sense		3		MHz/V	

2.Mixer

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Gain		13		dB	
Maximum Output Power		–5		dBm	
1dB Compression Point		–10		dBm	Output Level
Intercept Point		–16		dBm	Input Level
Noise Figure		10		dB	
RF-Lo Isolation		20		dB	

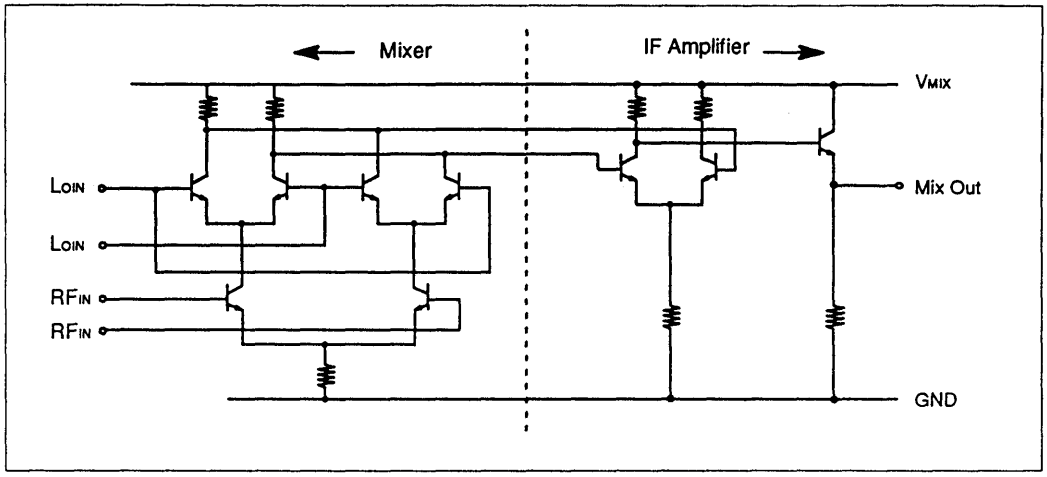
3.Amplifier

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	4.5		5.5	V	
Current Consumption		6		mA	
Operating Frequency		400		MHz	
Gain		20		dB	f = 400MHz (–30dBm in)
Maximum Output Power		–3		dBm	f = 400MHz
1dB Compression Point		–10		dBm	f = 400MHz, Output level
Intercept Point		–19		dBm	f = 400MHz, 400.1MHz, Input level
Noise Figure		3		dB	f = 400MHz (–30dBm in)

BASIC EQUIVALENT CIRCUIT OF ANALOG CIRCUITS

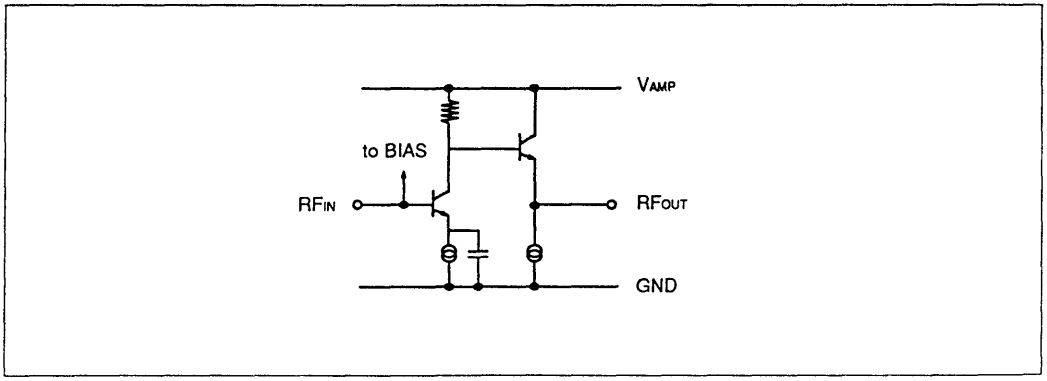
1.Mixer and IF amplifier

The mixer is a DBM (Double-Balanced Mixer) of active type. LO and RF inputs can be connected with internal bias circuit. The mixer output is connected with its own power supply (V_{MIX}) via a load resistor, then connected with next IF amplifier.
The IF amplifier consists of a differential amplifier and NPN transistors, and the differential amplifier's ouput is output through an emitter follower.



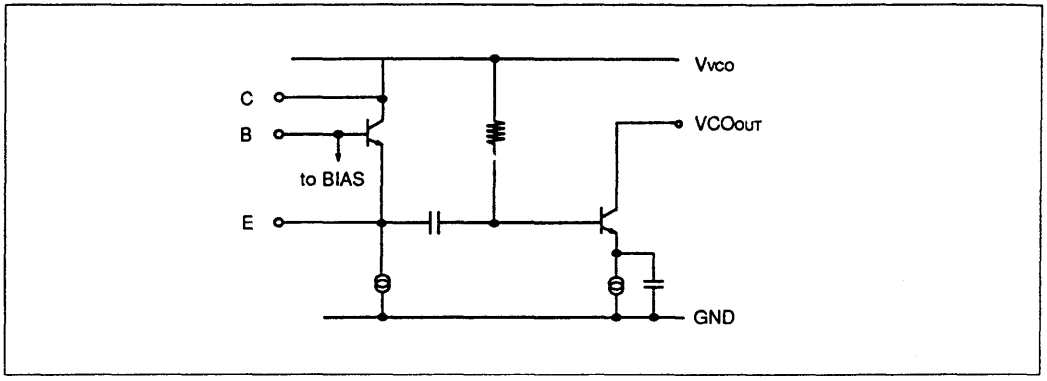
2.RF Amplifier

Output signal from common emitter circuit is output through emitter follower. It is possible to connect RF input with internal bias circuit.



3. VCO

The VCO consists of an output buffer's transistor and an oscillation's transistor which constructs a base grounded colpitts circuit. Resonator, varicap and so on are connected externally.



DEVELOPMENT PROCEDURE

1.Examination about product development

(1)Examination about specifications, and development conditions.

A customer submit target specifications of his idea to Fujitsu. Fujitsu reviews the specifications to judge technological feasibility, by means of simulation if necessay, and cost estimation.

[Products Information]

Functional Information : Functional descriptional material, I/O signal descriptional material, Block diagram, etc.
Specificational information : Prescaler, PLL, VCO, Mixer, Amplifier, etc.

[Development Information]

Delivery related Information : Development schedule, development assignment plan, etc.
Quotation related information : Demand, NRE, target price, etc.

(2)Examination about product development

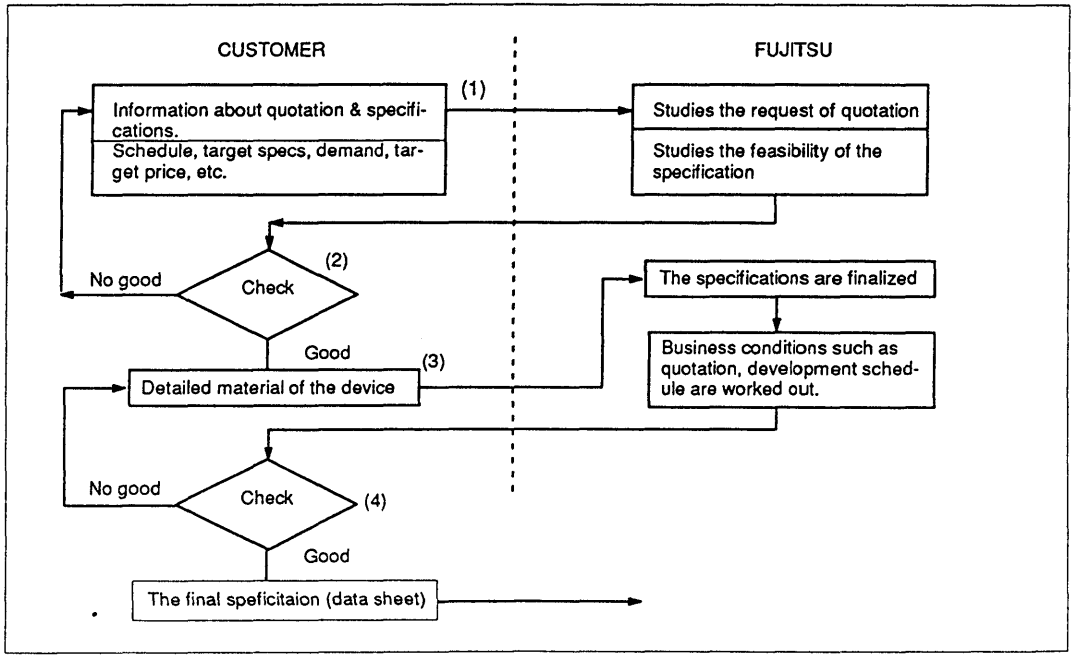
Fujitsu and the customer examine go/no-go of the product develpment in together, based on result of the review.

(3)Examination about product development

Circuits' functions and charateristics are examined in detail so that detailed specifications and test specifications are examined. After the specification is finalized, development schedule, NRE, formal quotation are done.

(4)Confirmation of the final specification (data sheet)

After the customer and Fujitsu agree to develop the device, the final specification (data sheet) is submitted to the customer to confirm the specifications.



2.Development of IC

(1)IC designing and manufacturing by way of trial

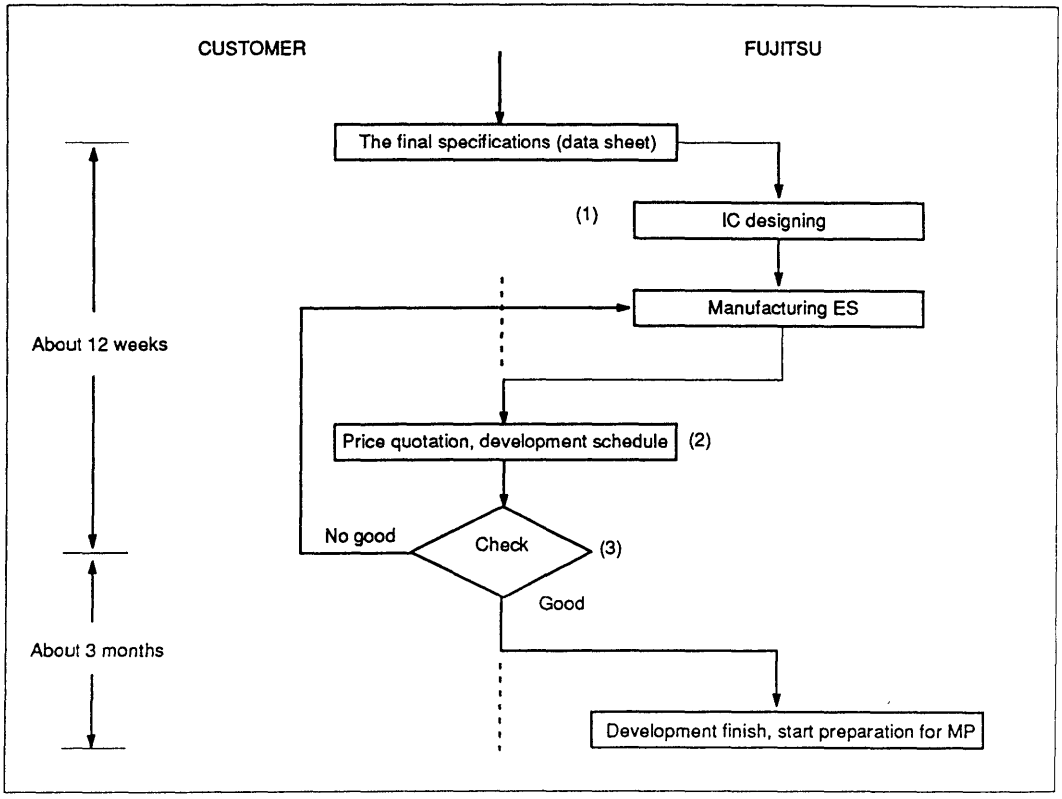
Fujitsu designs the device and manufacture it by way of trial based on the final specifications. It takes about 12 weeks (typ.) from when the final specification sheet is issued to when the first ES (Engineering Sample) are manufactured.

(2)Evaluation of ES

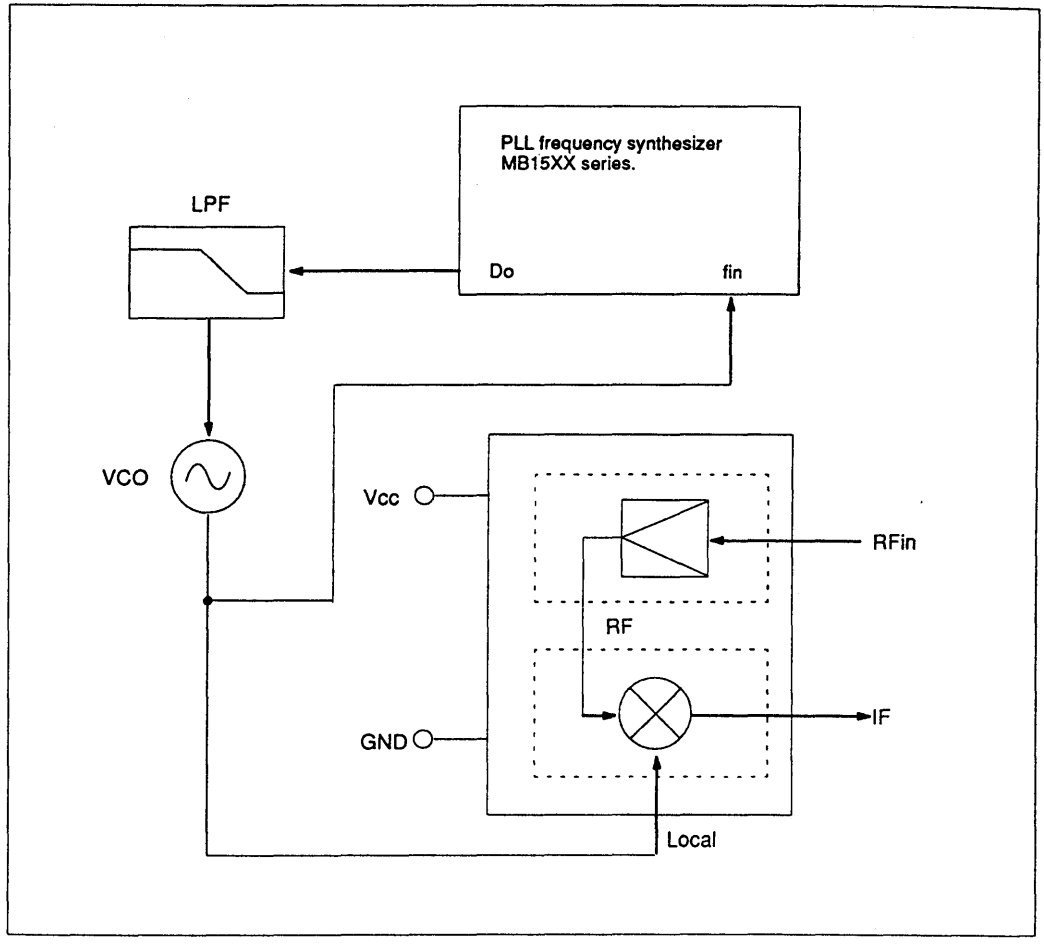
ES is evaluated by both the customer and Fujitsu based on the final specifications.

(3)The final confirmation

A specification sheet of finished product is submitted to the customer from Fujitsu when the customer satisfied with evaluation result, so that preparation for mass production is started by Fujitsu. Typically 3 months are necessary for the first shipment from when the specification sheet (for finished products) is issued.

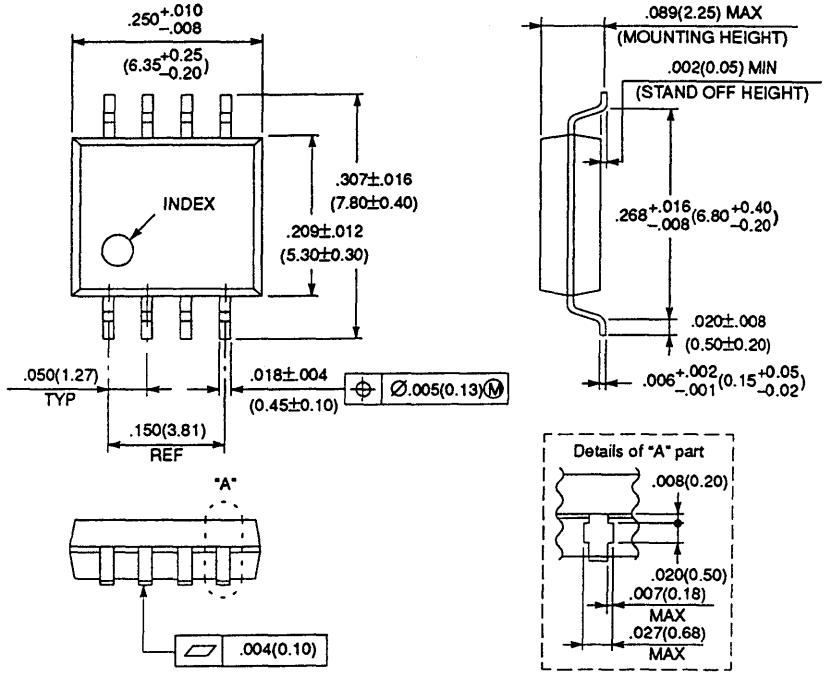


APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-8P-M01)

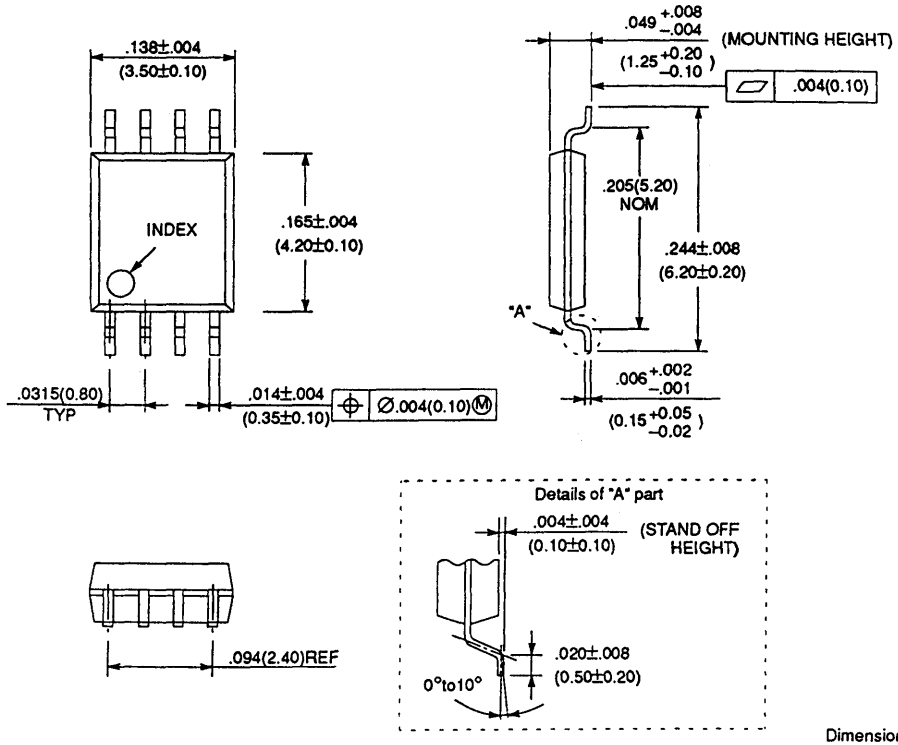


Dimensions in
inches (millimeters)

6

PACKAGE DIMENSIONS (Continued)

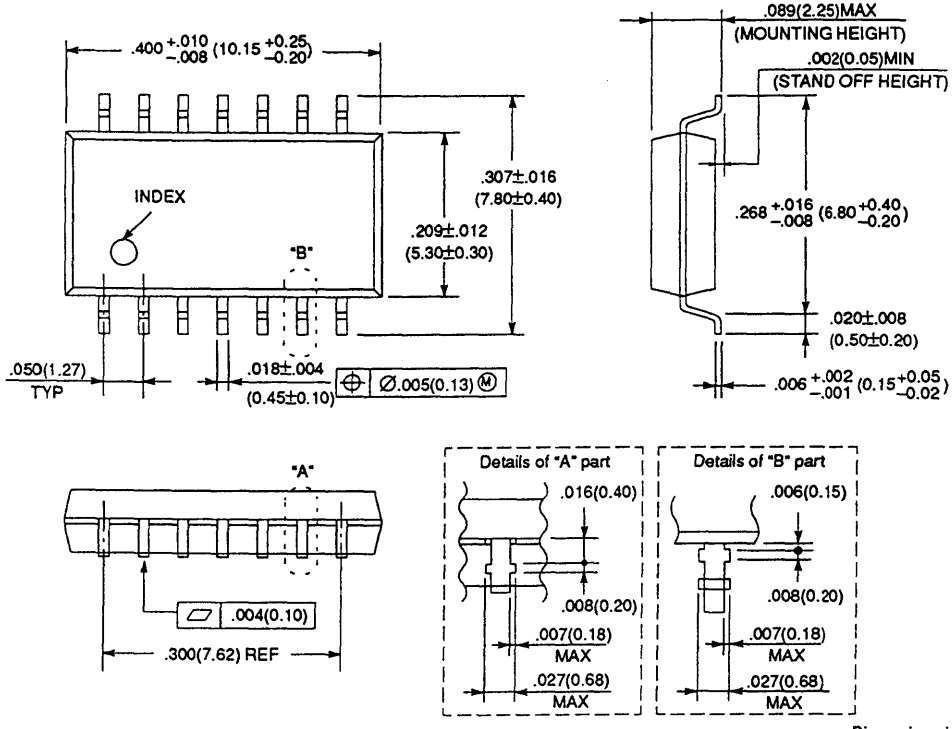
8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-8P-M03)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M04)

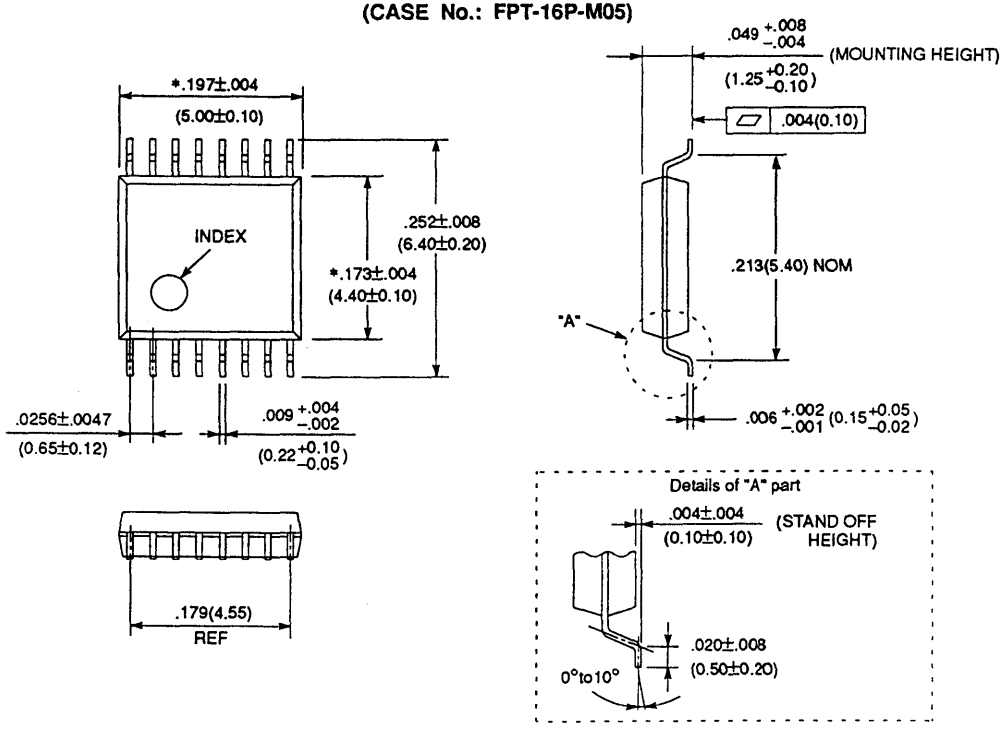


Dimensions in inches (millimeters)

6

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

January 1994
Edition 1.0

FUJITSU

DATA SHEET

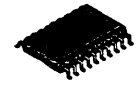
MB54600 SERIES

Bi-CMOS LSI RF IC

ADVANCED SEMICUSTOM TECHNOLOGY FOR RF SYSTEM INTEGRATION ON LSI

This FUJITSU Series is a semicustom LSI IC based on a master slice method, and is ideally suitable for high frequency analog circuits such as VCO.
MB54600 series involves one prescaler circuit and six analog macros, such as VCO's, IF amplifiers, RF amplifiers, and mixers can be realized on a single chip in accordance with customer requests. This is achieved by means of predefined blocks (prescaler macro and analog macros) laid out on the frame. The performance of each block is custom specified.
The MB54600 Series achieves low power dissipation by Fujitsu's advanced technology. Very small flat packages are available for this LSI.

PRELIMINARY



FPT-20P-M03

[Now printing]

FPT-34P-M03

6

FEATURES

- High frequency analog circuits for front-end section, such as VCO's, mixers, RF and IF amplifiers can be realized.
- Choice of a wide variety of exsisting and analog functions, as well as custom specifications of the same.
- Maximum operating frequency is at 2GHz.
- Choice of power supply voltages;
  3V type : 2.7V to 3.3V
  2V type : 2.0V to 2.4V
- Development cycle is typical 12 weeks.
- Very samll package is available, SSOP 20-pin/34-pin.
- Power saving circuit can be involved.

ABSOLUTE MAXIMUM RATINGS

(Reference voltage level is GND.)

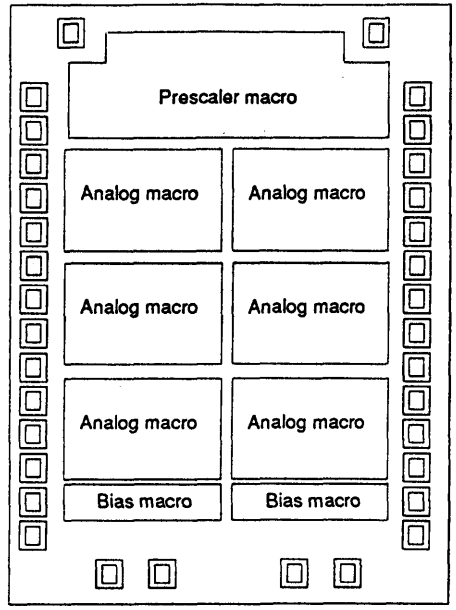
Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +5.0	V
Input Voltage	V_{IN}	−0.5 to Vcc+0.5	V
Output Current	I_{OUT}	±10	mA
Ambient Temperature	T_{STG}	−50 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

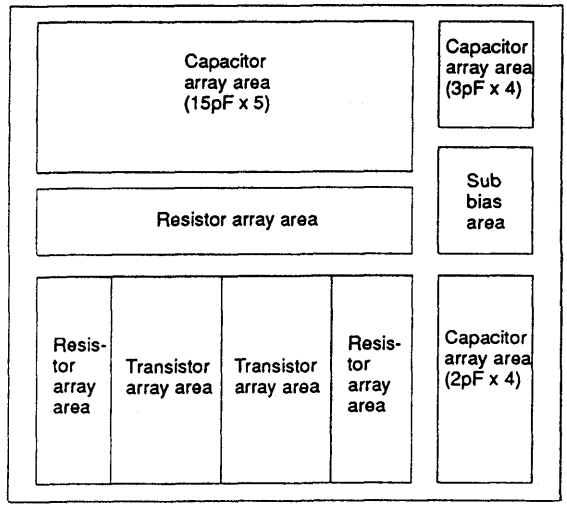
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CHIP LAYOUT

MB54600 Series



Analog cell



MACRO CELLS DESCRIPTIONS

1.High frequency analog cells

1.1 Mixer

Double balanced mixer of active type.

1.2 IF amplifier

IF amplifier consist of a differential amplifier and NPN transistor. Differential amplifier outpt is emitter follower type.

1.3 RF amplifier

Output signal of grounded emitter circuit is emitter follower output. RF input can be connected internal bias circuit.

1.4 VCO

The VCO consists of an output buffer's transistor and an oscillation's transistor which constructs an oscillator circuit of base grounded colpitts. Resonator, varicap and so on are connected externally.

Note;

Circuit design and so on can be optimized in accordance with customer needs.

RECOMMENDED OPERATING CONDITIONS

3V type

(Reference voltage level is GND.)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	2.7		3.3	V
	GND		0		V
Ambient Temperature	T_A	–40		+85	°C

2V type

(Reference voltage level is GND.)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	2.0		2.4	V
	GND		0		V
Ambient Temperature	T_A	–40		+85	°C

ANALOG CIRCUITS BASIC CHARACTERISTICS EXAMPLE

1.VCO

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		11		mA	
Operating Frequency			900	MHz	
C / N		77		dB	Offset frequency = 25kHz, BW = 16 kHz
S / N		44		dB	BW = 0.3 ~ 3kHz, 3kHz/Dev
Output Power		–2		dBm	
Mod Sense		6		MHz/V	

2.Mixer

Parameter		Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply Voltage		2.7	3.0	3.3	V	
Current Consumption			15		mA	
Operating Frequency	RF		800		MHz	$f_{RF} + f_{LO} = f_{IF}$
	Lo		110		MHz	
	IF		910		MHz	
Gain			7		dB	
Maximum Output Power			–9		dBm	
1dB Compression Point			–12		dBm	Output Level
Intercept Point			–9		dBm	Input Level
Noise Figure			11		dB	DSB output
RF-Lo Isolation			20		dB	

6

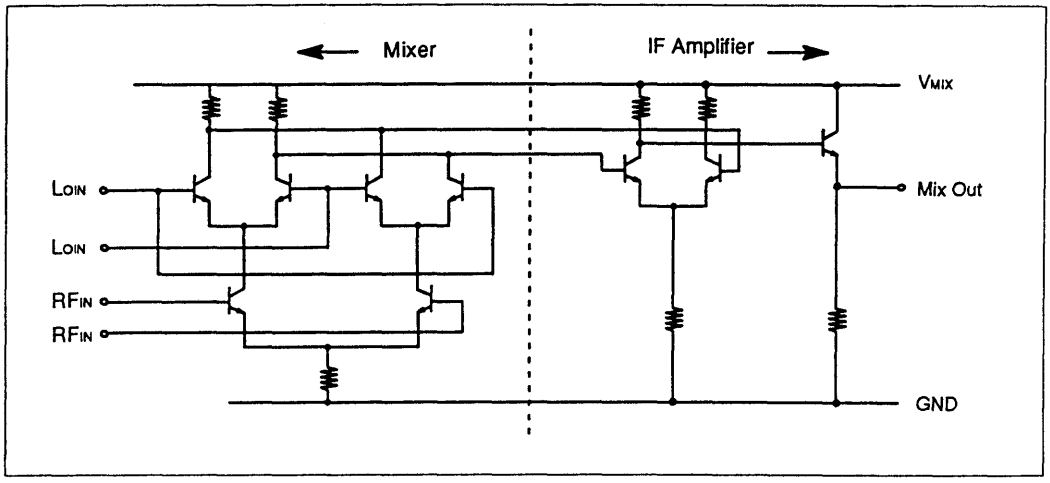
3.Amplifier

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		7.5		mA	
Operating Frequency		900		MHz	
Gain		13		dB	f = 900MHz (–30dBm in)
Maximum Output Power		1		dBm	f = 900MHz
1dB Compression Point		–5		dBm	f = 900MHz, Output level
Intercept Point		–9		dBm	f = 900MHz, 900.1MHz, Input level
Noise Figure		2.5		dB	f = 900MHz

BASIC EQUIVALENT CIRCUIT OF ANALOG CIRCUITS

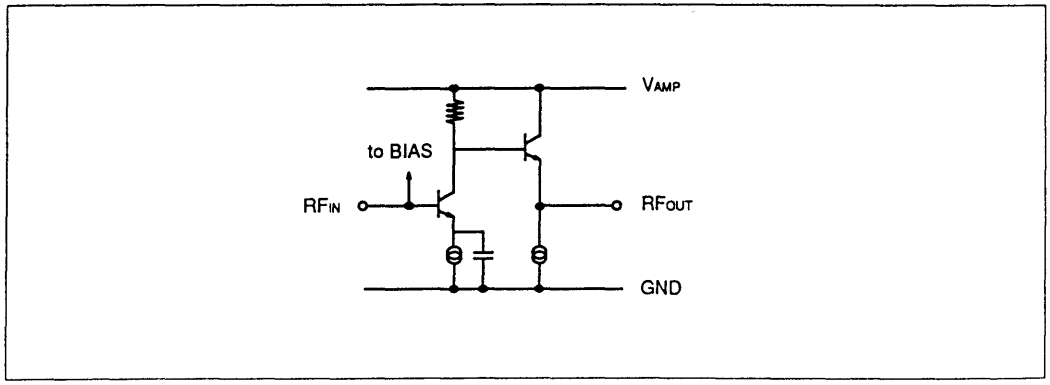
1.MIxer and IF amplifier

The mixer is a DBM (Double-Balanced Mixer) of active type. LO and RF inputs can be connected with internal bias circuit. The mixer output is connected with its own power supply (V_{MIX}) via a load resistor, then connected with next IF amplifier.
The IF amplifier consists of a differential amplifier and NPN transistors, and the differential amplifier's ouput is output through an emitter follower.



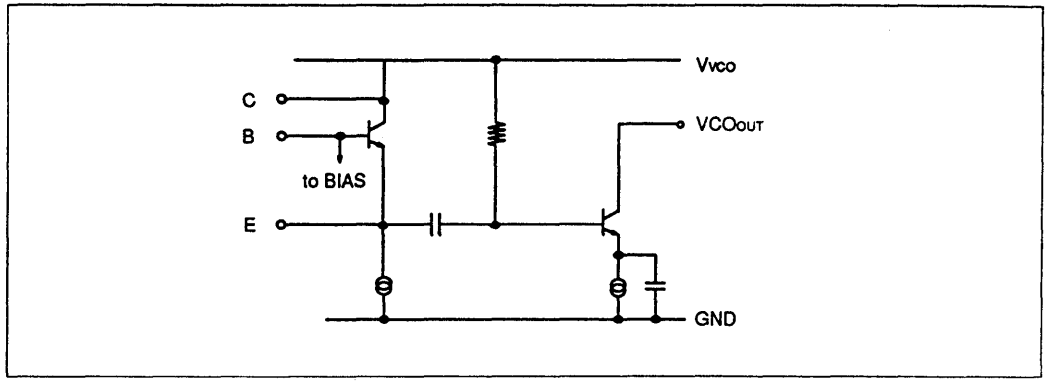
2.RF Amplifier

Output signal from common emitter circuit is output through emitter follower. It is possible to connect RF input with internal bias circuit.



3. VCO

The VCO consists of an output buffer's transistor and an oscillation's transistor which constructs a base grounded colpitts circuit. Resonator, varicap and so on are connected externally.



DEVELOPMENT PROCEDURE

1.Examination about product development

(1)Examination about specifications, and development conditions.

A customer submit target specifications of his idea to Fujitsu. Fujitsu reviews the specifications to judge technological feasibility, by means of simulation if necessay, and cost estimation.

[Products Information]

Functional Information : Functional descriptional material, I/O signal descriptional material, Block diagram, etc.
Specificational information : Prescaler, PLL, VCO, Mixer, Amplifier, etc.

[Development Information]

Delivery related Information : Development schedule, development assignment plan, etc.
Quotation related information : Demand, NRE, target price, etc.

(2)Examination about product development

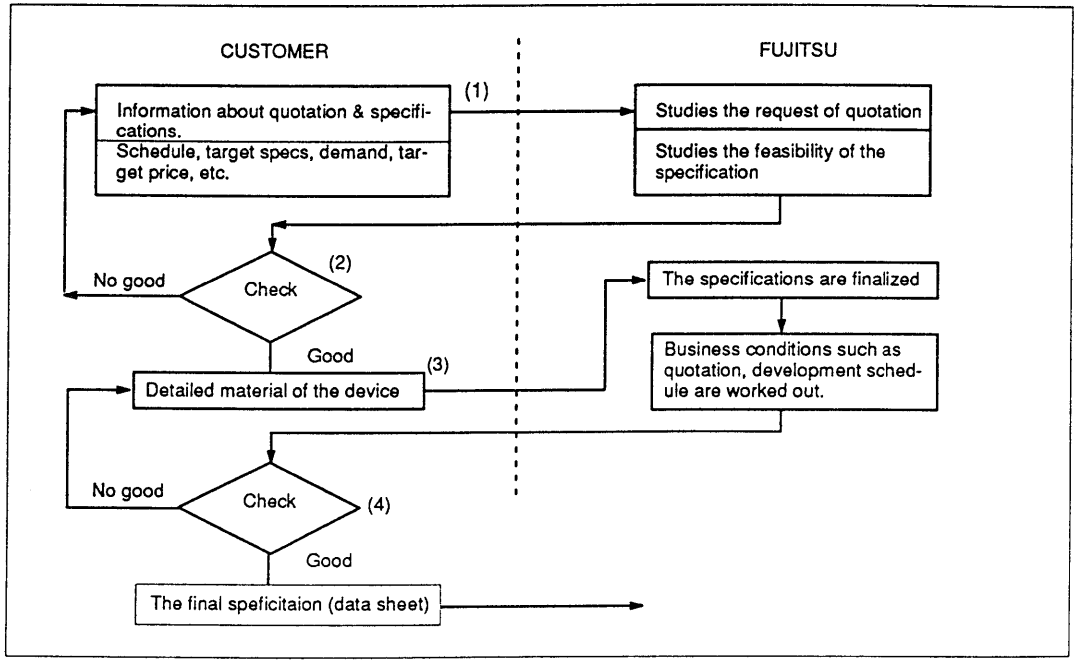
Fujitsu and the customer examine go/no–go of the product develpment in together, based on result of the review.

(3)Examination about product development

Circuits' functions and charateristics are examined in detail so that detailed specifications and test specifications are examined. After the specification is finalized, development schedule, NRE, formal quotation are done.

(4)Confirmation of the final specification (data sheet)

After the customer and Fujitsu agree to develop the device, the final specification (data sheet) is submitted to the customer to confirm the specifications.



6

2.Development of IC

(1)IC designing and manufacturing by way of trial

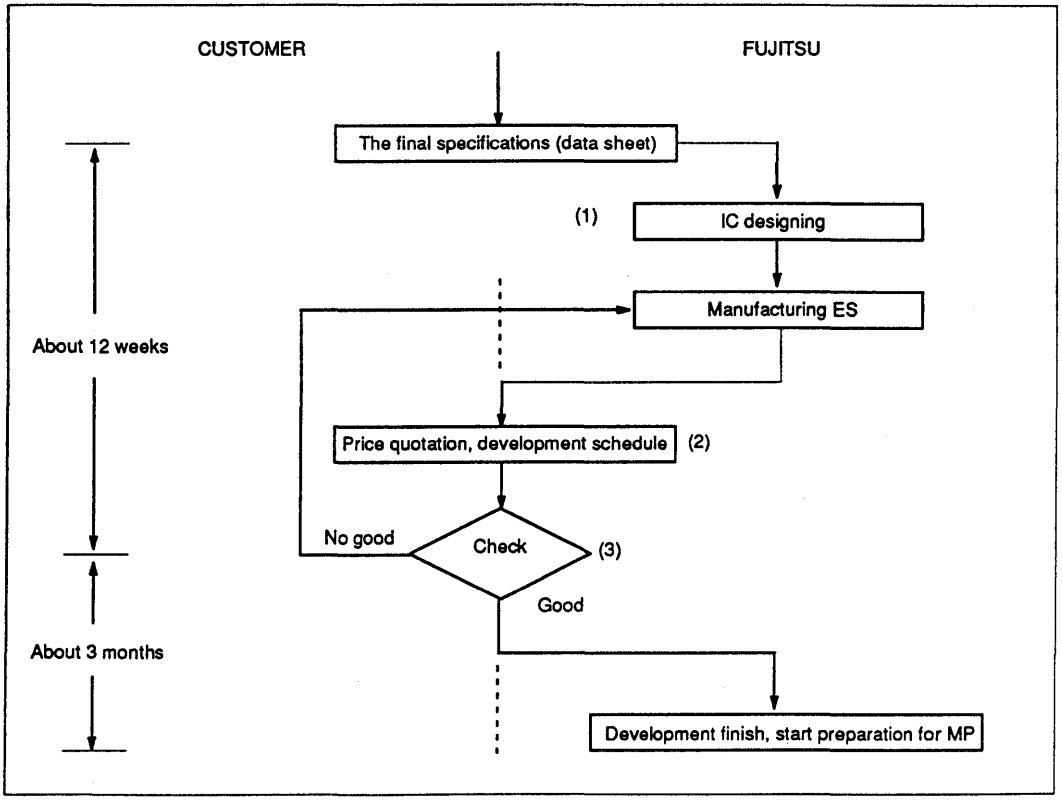
Fujitsu designs the device and manufacture it by way of trial based on the final specifications. It takes about 12 weeks (typ.) from when the final specification sheet is issued to when the first ES (Engineering Sample) are manufactured.

(2)Evaluation of ES

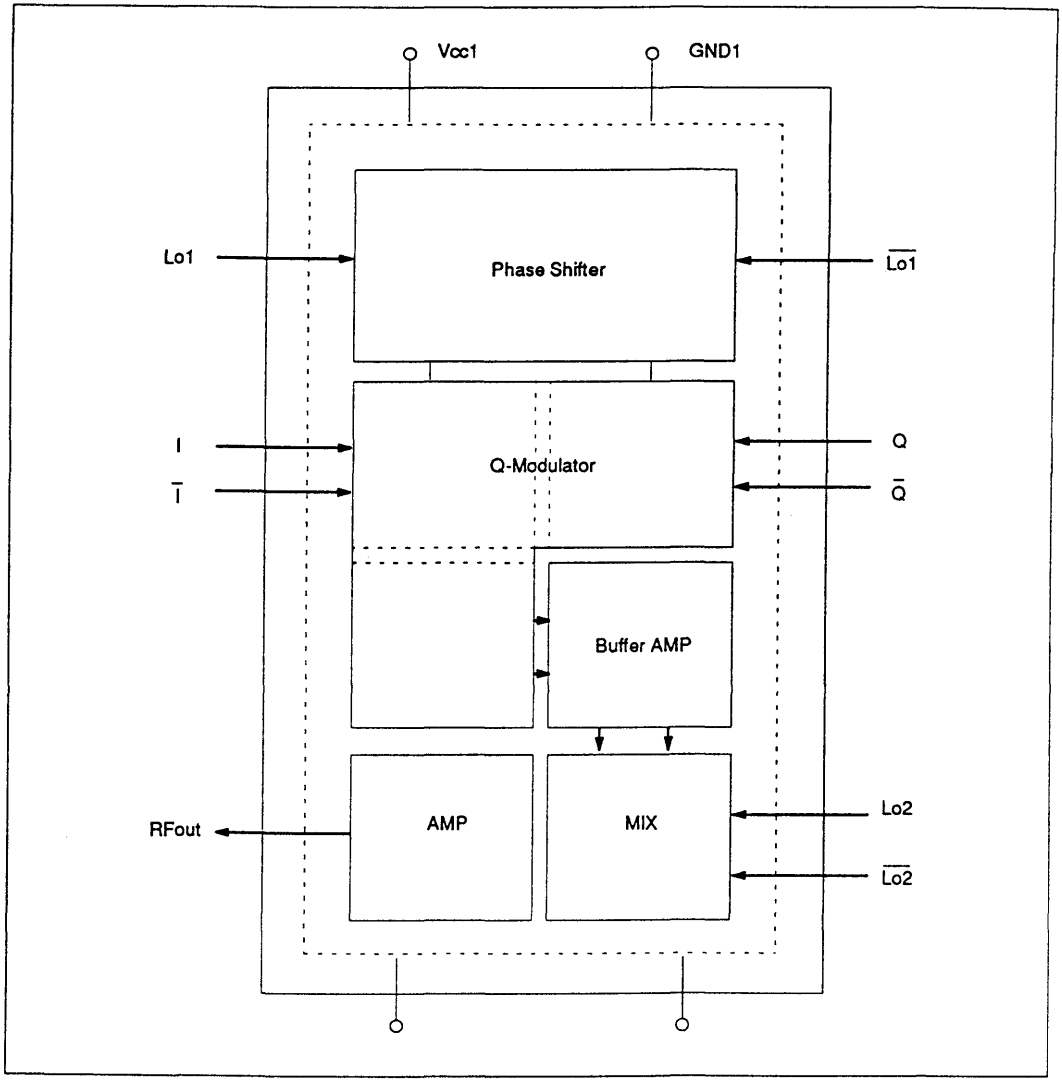
ES is evaluated by both the customer and Fujitsu based on the final specifications.

(3)The final confirmation

A specification sheet of finished product is submitted to the customer from Fujitsu when the customer satisfied with evaluation result, so that preparation for mass production is started by Fujitsu. Typically 3 months are necessary for the first shipment from when the specification sheet (for finished products) is issued.

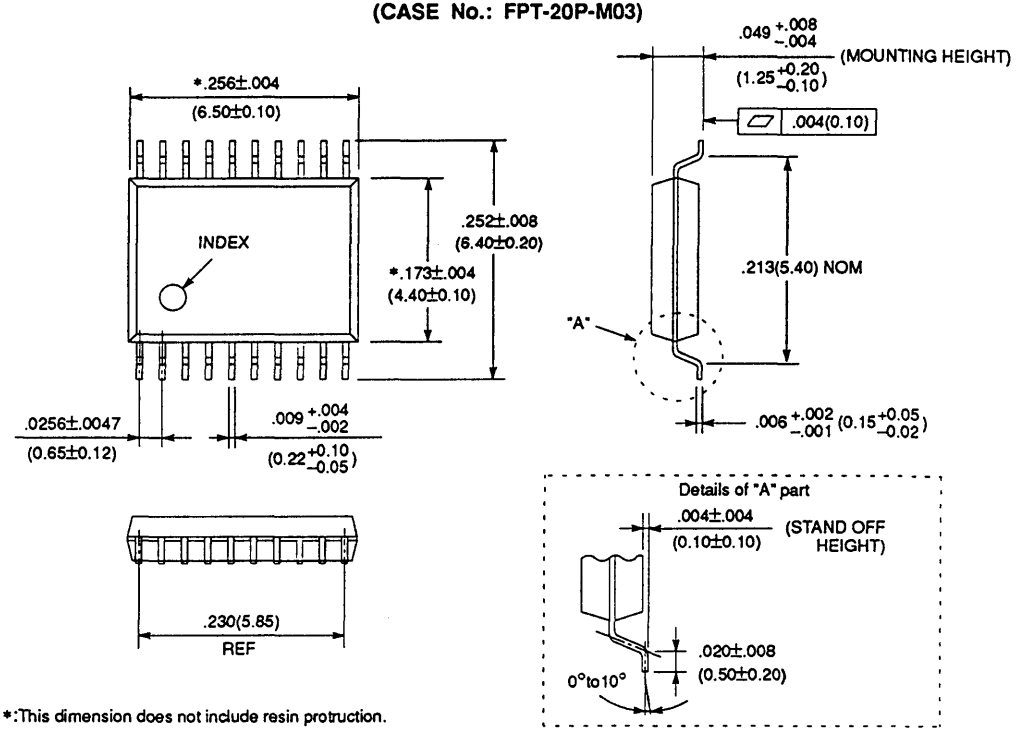


APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

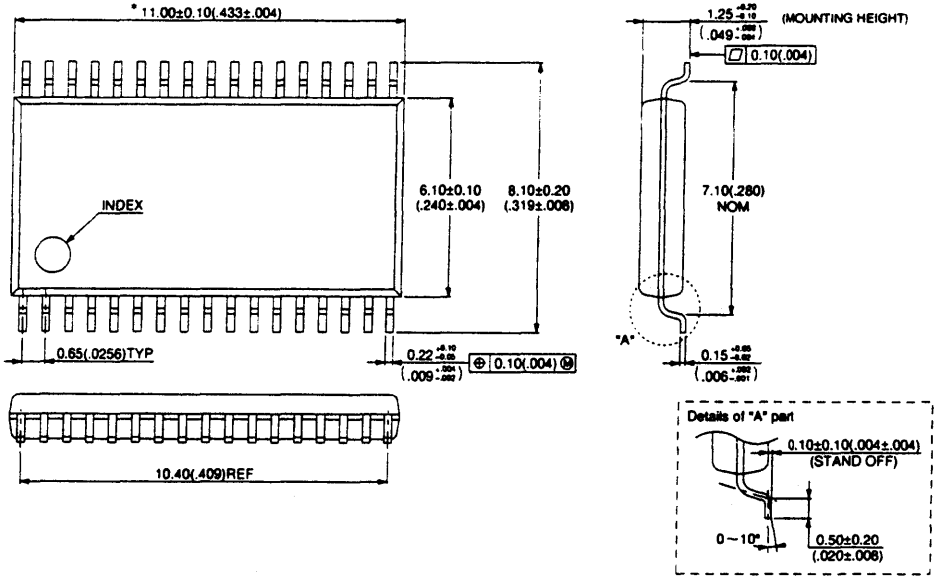
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

34-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-34P-M03)

34 pin Plastic SSOP
(FPT-34P-M03)

* : This dimension does not include resin protraction.



Dimensions in mm (inches)

6

DS06–70104–1E

FUJITSU

DATA SHEET

MB1560 *Semicustom* *(For PLL Frequency Synthesizers)*
Bi–CMOS LSI RF IC Specification

■ DESCRIPTION

This FUJITSU Series is a master-slice type semi-custom LSI ideal for use in high-frequency front-end circuits in VCO, amplifier, mixer and orthogonal modulator devices.

The MB1560 series features an analog circuit unit that is a more highly integrated version of the MB1520 - MB1550 series featuring two analog cell circuits, plus a digital circuit unit with a power-saving prescaler circuit and a PLL1 circuit with pulse-swallow capability.

The PLL, prescaler and high-frequency analog circuits can be designed to users' specifications using FUJITSU's standard macro cell technology.

This LSI series uses FUJITSU's latest wafer process technology for power-saving operation and master-slice semi-custom design to reduce lead times and lower costs. In addition, the ultra-compact flat package helps maintain circuit confidentiality, and contributes to lighter, more compact design by reducing the number of components.

The MB1560 series is ideal for high-frequency applications, particularly mobile communication devices operating on digital specifications such as PCN, DECT, PHS and so on.

6

■ FEATURES

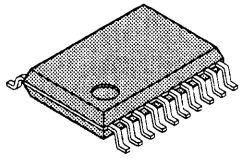
- PLL circuits can be customized for operating frequency, logical circuits, etc.
- High frequency analog circuits with adjustable resistance levels
- High speed operating capacity to 3.0 GHz
- On-chip low-current consumption and power-saving circuits
- On-chip high-speed lockup function
- Supply voltage: 2.7 V to 3.3 V (minimum operating voltage to 2.0 V min.)
- Development time (standard): approx. 10 weeks

■ LINEUP

Series	Prescaler	PLL	Analog circuits	Operating frequency	Package			Remarks
					SSOP	QFP	SQFP	
MB1560	1 circuit	1 circuit	2 circuits	3.0 GHz	20 34	—	—	For single PLL frequency synthesizers

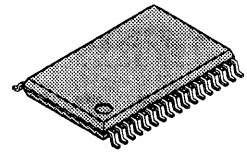
■ PACKAGE

20 pin Plastic SSOP



(FPT-20P-M03)

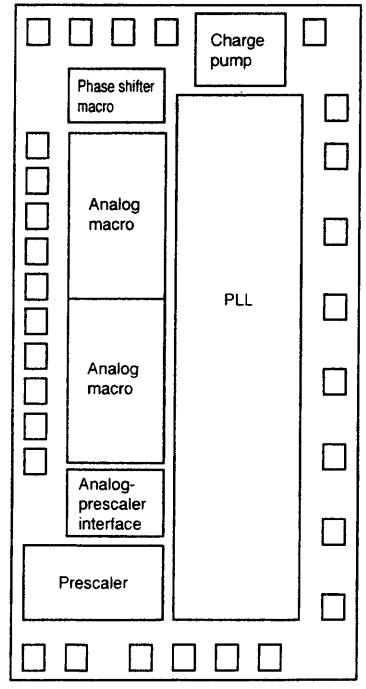
34 pin Plastic SSOP



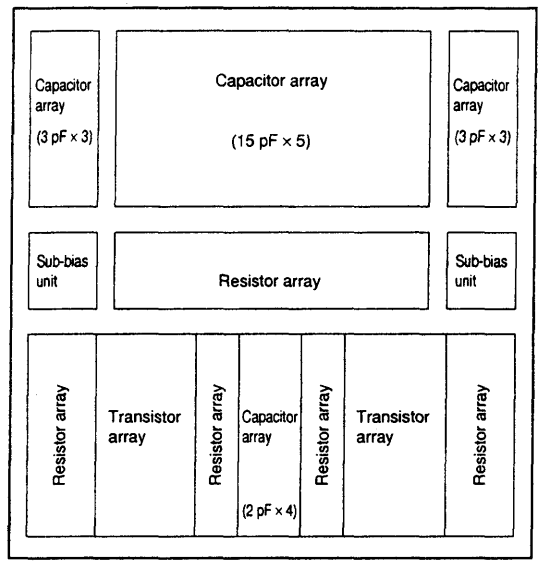
(FPT-34P-M03)

■ CHIP LAYOUT

- **MB1560 Series**



- **Analog Cell**


Capacitor array
(3 pF x 3)
Capacitor array
(15 pF x 5)
Capacitor array
(3 pF x 3)
Sub-bias unit
Resistor array
Sub-bias unit
Resistor array
Transistor array
Resistor array
Capacitor array
(2 pF x 4)
Resistor array
Transistor array
Resistor array

■ MACRO CELL DESCRIPTIONS

1. Prescaler

Divides the reference frequency by any given value and outputs the resulting frequency. Choice of two-modulus or fixed output mode.

2. PLL

- **Phase comparator**

The phase comparator has a phase detection range of -2π to $+2\pi$, and is designed to eliminate blind spots in phase comparison by output of a margin-of-error signal to the charge pump even when the phase difference is zero. Phase comparator characteristics can also be tuned to the polarity of VCO.

- **Counters**

The divide ratios of the comparator-side counter and reference-side counter can be either programmable or fixed.

- **Charge pump**

The "H" level output voltage from the charge pump is determined by power supply voltage. Charge pump characteristics for the sending and receiving systems can be optimized for each specific application.

For example, when FM modulation is applied directly to the VCO signal, charge pump characteristics can be adjusted for lower speeds in order to reduce the sensitivity of the synthesizer loop so that output does not track the modulation.

- **Analog switch**

When switching frequencies, the analog switch can be used to switch the capacitance of the low pass filter, to reduce the time constant in the filter and the load on the charge pump. This enables higher lock-up speed.

Switch control is synchronous with the LE signal, to that the analog switch is on when the LE signal is "high".

- **High speed lock-up circuit**

This circuit is specially designed for faster lock-up speeds.

- **Intermittent operation control circuit**

This on-chip power-saving function reduces circuit current flow in standby status, enabling devices to operate with less power demand. A special circuit is built in to prevent excessive error signal from increasing lock-up delay during the transition from power-saving mode to operating mode.

- **List of standard macro cells**

Type	Vcc	Icc	Operating frequency	Prescaler divide ratio (M)	Comparator counter divide ratio (N)	Swallow counter divide ratio (A)	Reference counter divide ratio (R)
PLL1	3 V	4 mA	1.1 GHz	64/65	16 to 2047	0 to 127	8 to 16383
PLL2		6 mA	2.0 GHz				

Crystal oscillator input frequency: Up to 32 MHz

Standby mode current demand: 100 μA

3. High Frequency Analog Cells

- **Mixer**

Active type double-balanced mixer

- **IF amplifier**

The IF amplifier is configured from a differential amplifier plus an NPN transistor using emitter-follower output from the differential amplifier.

- **RF amplifier**

Provides emitter-follower output of the output signal from the emitter-ground circuit. The RF input side can be connected to an internal bias circuit.

- **VCO**

Configured from an oscillator transistor in a base-ground Colpitts type oscillator circuit, plus a transistor acting as output buffer. Can be connected to external devices such as varicap or resonator.

- **Orthogonal modulator**

An orthogonal modulator is used for IF frequency modulation. In addition, a flip-flop type 90° phase shift circuit can be included in the configuration.

Note: Circuit format and other details can be adjusted to meet customer requirements.

6

■ CIRCUIT OPERATING DESCRIPTIONS

1. Intermittent Operation Control Circuit

The intermittent operation control circuit operates the LSI circuits during communication operations and at all other times places the chip in standby status to reduce power demand.

(1) Circuit operation in operating mode

All circuits are in operating status, and the chip performs normal PLL operations.

(2) Circuit operation in standby mode

All circuits that can be stopped without interfering with operation are shut down, and the chip goes into low-power operating mode.

Latch data:	Saves immediately preceding data
Shift register:	Data input enabled
Charge pump output:	High impedance
VCO input voltage:	Saves voltage level stored in low-pass filter during the last operating mode

<Caution> The digital system power supply must still be applied in standby mode.

2. Phase Lock Detection Circuit

To detect phase lock condition from the LD signal pin output, the T-bit should be selected. When the phase difference is greater than tw, the LD pin will output an L level signal, and when the difference is less than tw for 3 or more cycles, the output will change to H level. The length of the tw time interval can be set in the range of 625 ns to 1250 ns by connection to the crystal oscillator.

- **LD Signal operating status**

Operating status	PLL circuit	LD output
Standby mode	Standby	H
Operating mode	Un-lock	L
	Lock	H

3. High Speed Tuning Circuit

The following high speed tuning circuits are available for use according to specific applications.

- **High speed tuning circuits for ASTRO MASTER IV**

Function	Operation	Optimum applications
Analog switch	Circuit temporarily reduces LPF time constant at lock-up.	Analog portable phone devices (receiving system)
Turbo circuits	For broad-band steps, circuit forcibly switches charge pump on/off	PHS devices
Supercharger circuit	Circuit increases charge pump drive capacity	PHS devices
Hypercharger circuit	Circuit further enhances the drive capacity of the supercharger circuit	PDC, GSM etc.

■ SERIAL DATA

1. Data Bit Configuration

PLL operating settings are made through serial data input. The standard serial data format is shown in the table below. Serial data is entered MSB-first, and the data length is in the range of 22 to 37 bits.

- **Standard format for serial data**

Bit name (abbreviation)		Functional description	Standard bit count
Control bit (CNT bit)		Selects transfer destination (sending or receiving system)	1 to 2
LD select bit (T-bit)		Selects LD output	1 to 2
FC bit (F-bit)		Switches the phase of phase comparator	1
Programmable counter bit (N-bit)		Sets the programmable counter's divide ratio	11
Swallow counter bit (A-bit)		Sets the swallow counter's divide ratio	7
Reference counter bit (R-bit)	Fixed	Sets the reference counter's divide ratio	1 to 2
	Programmable		14

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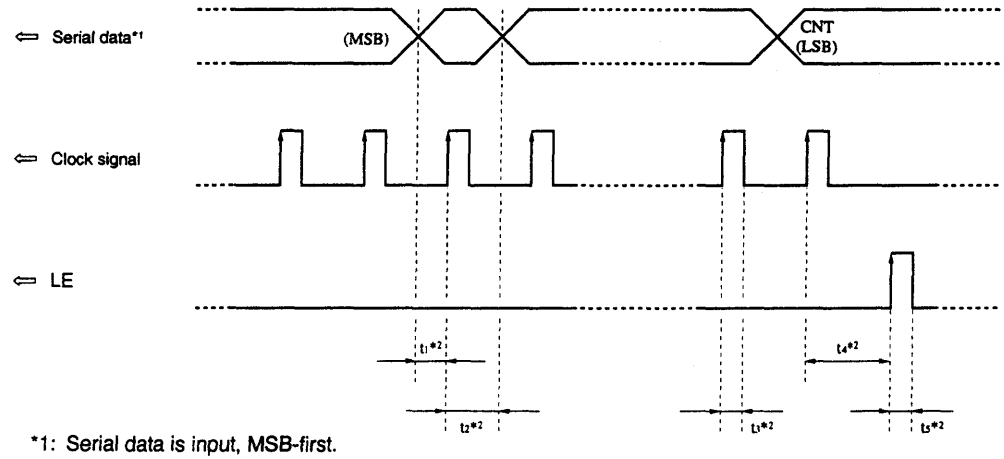
2. Serial Data Input Timing

After the serial data is stored in the shift register, it can be transferred to the latch circuit by means of the LE signal.



*1: Serial data is input, MSB-first.
*2: 100 ns ≤ t_1, t_4 300 ns ≤ t_3 800 ns ≤ t_5 1000 ns ≤ t_2

Notes:
- Data input utilizes the serial data, clock and LE signals at supply voltage or lower levels
- Shift register data is updated sequentially each time the clock signal is input. Data is synchronized with the rising edge of the clock signal, and is read sequentially into the shift register, MSB-first.
- After LSB input, the LE signal is changed from L level to H level.
- Shift register data is transferred to the latch circuit while the LE signal is at H level.
- Each input signal pin has a Schmitt trigger circuit to protect against abnormal operation due to noise.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Supply voltage*	V_{CC}	−0.5	+4.0	V
Input voltage*	V_{IN}	−0.5	V_{CC} + 0.5	V
Output current	I_{OUT}	−10	10	mA
Storage temperature	Tstg	−55	+125	°C

*: Voltage values are based on GND = 0 V.

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage*1	V_{CC}	2.7*2	—	3.3	V
	GND	—	0	—	V
Operating temperature	Ta	−40	—	+85	°C

*1: Voltage values are based on GND = 0 V

*2: Operation is assured to the minimum operating voltage level of 2.0 V min.

■ ANALOG CIRCUIT CHARACTERISTICS

Circuit	Parameter		Conditions	Value (typ.)	Unit
VCO	Supply voltage		—	3.0	V
	Current demand		—	11	mA
	Operating frequency		—	900	MHz
	C/N ratio		Offset frequency = 25 kHz, Band Width = 16 kHz	77	dB
	S/N ratio		BW = 0.3 to 3 kHz, 3 kHz/Dev	44	dB
	Output power		—	−2	dBm
	Mod Sense		—	6	MHz/V
Mixer	Supply voltage		—	3.0	V
	Current demand		—	12	mA
	Operating frequency	IF	—	800	MHz
		LO	P_{LO} = −10 dBm	110	MHz
		RF	$f_{RF} = f_{LO} + f_{IF}$	910	MHz
	Conversion gain		—	6	dB
	Maximum output power		—	−11	dBm
	1 dB compression point		Output level	−15	dBm
	Intercept point		Input level	−8	dBm
	NF		DSB measurement	12	dB
Amplifier	Supply voltage		—	3.0	V
	Current demand		—	6	mA
	Operating frequency		—	900	MHz
	Gain		f = 900 MHz (−30 dBm in)	14	dB
	Maximum output power		f = 900 MHz	−3	dBm
	1 dB compression point		f = 900 MHz, output level	−8	dBm
	Intercept point		f = 900 MHz, 900.1 MHz, input level	−12	dBm
	NF		f = 900 MHz	2.2	dB

(Continued)

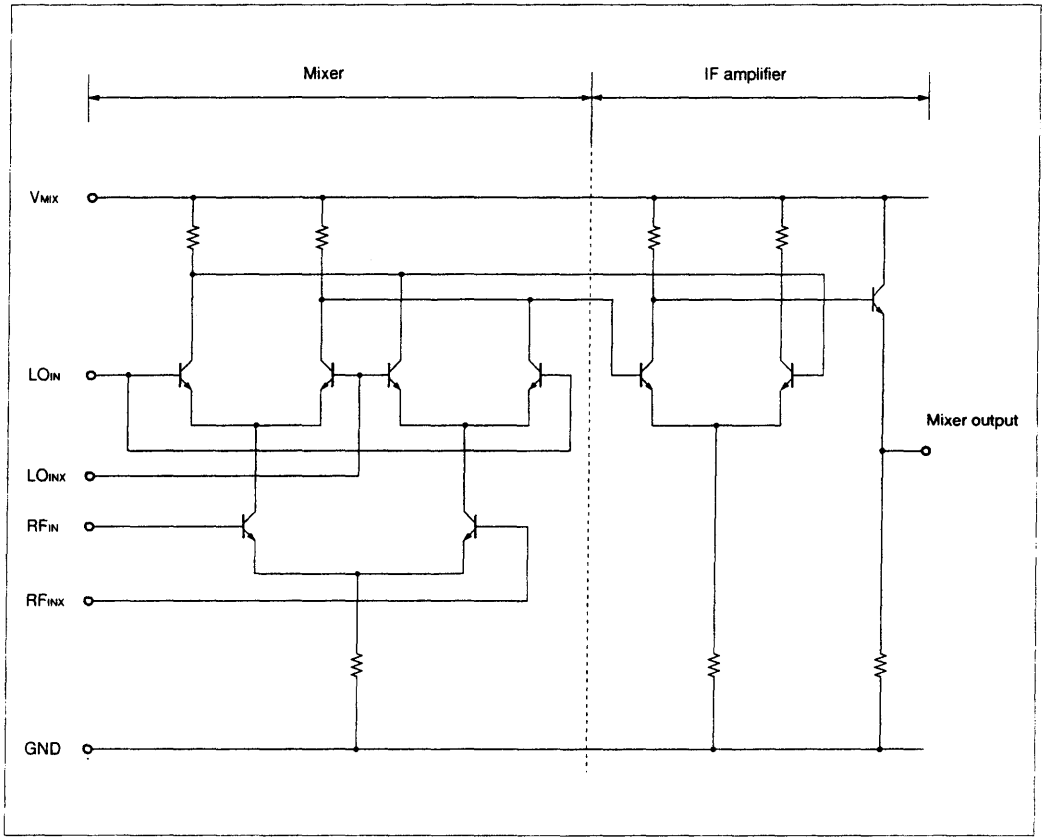
(Continued)

Circuit	Parameter		Conditions	Value (typ.)	Unit
Orthogonal modulator	Supply voltage		—	3.0	V
	Current demand		—	25	mA
	Operating frequency	LO1	P_{LO1} = –5 dBm	500	MHz
		LO2	P_{LO2} = –5 dBm	1650	MHz
		RF	$f_{RF} = f_{LO2} + f_{LO1}/2$	1900	MHz
	Output level		—	–14	dBm
	Modulator precision	Amplitude deviation	RMS Magnitude Error	1.9	%
		Phase deviation	RMS Phase Error	0.9	deg.
		Vector error	RMS Vector Error	2.4	%
	Carrier leak		—	–31	dBc

■ ANALOG SYSTEM: BASIC EQUIVALENT CIRCUITS

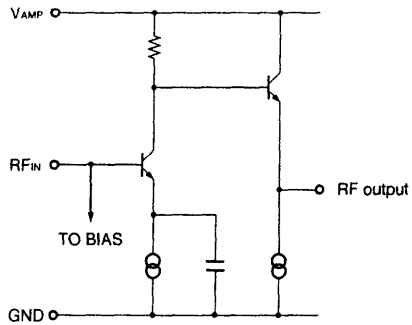
1. Mixer, IF Amplifier

The MB1560 series features an active-type double-balanced mixer. The LO and RF output can be connected to an internal bias circuit. The mixer output is connected through on-chip load resistor to the chip's power supply, and then to the next-stage IF amplifier. The IF amplifier is configured from a differential amplifier and NPN transistor, and provides emitter-follower differential amplifier output.



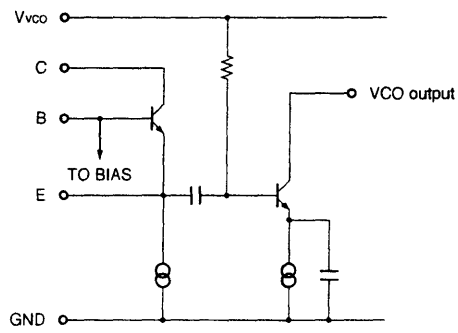
2. RF Amplifier

The emitter-ground circuit output signal is output as an emitter-follower signal. The RF input can be grounded to an internal bias circuit.



3. VCO Amplifier

The VCO amplifier is configured from an oscillator transistor in a base-ground Colpitts type oscillator circuit, plus a transistor acting as output buffer. The VCO amplifier can be connected to external devices such as varicap or resonator.



■ DEVELOPMENT PROCESSES

Each product in the MB1560 Series is developed through the following processes, based on requirement and specifications supplied by the customer.

1. Feasibility Study

(1) Product specifications and development process study

FUJITSU conducts simulations based on documentation provided by the customer, in order to evaluate the technical and economic feasibility of each proposed design.

Product Documentation
- Technical documentation: Functional descriptions, I/O signal descriptions, block diagrams.
- Characteristics documentation: For prescalers, PLL, VCO, mixers, amplifiers, etc.

Development Documentation
- Delivery schedule documentation: Development schedule, division of responsibilities, etc.
- Cost estimates: Volume requirements, development costs, target prices

(2) Product feasibility evaluation

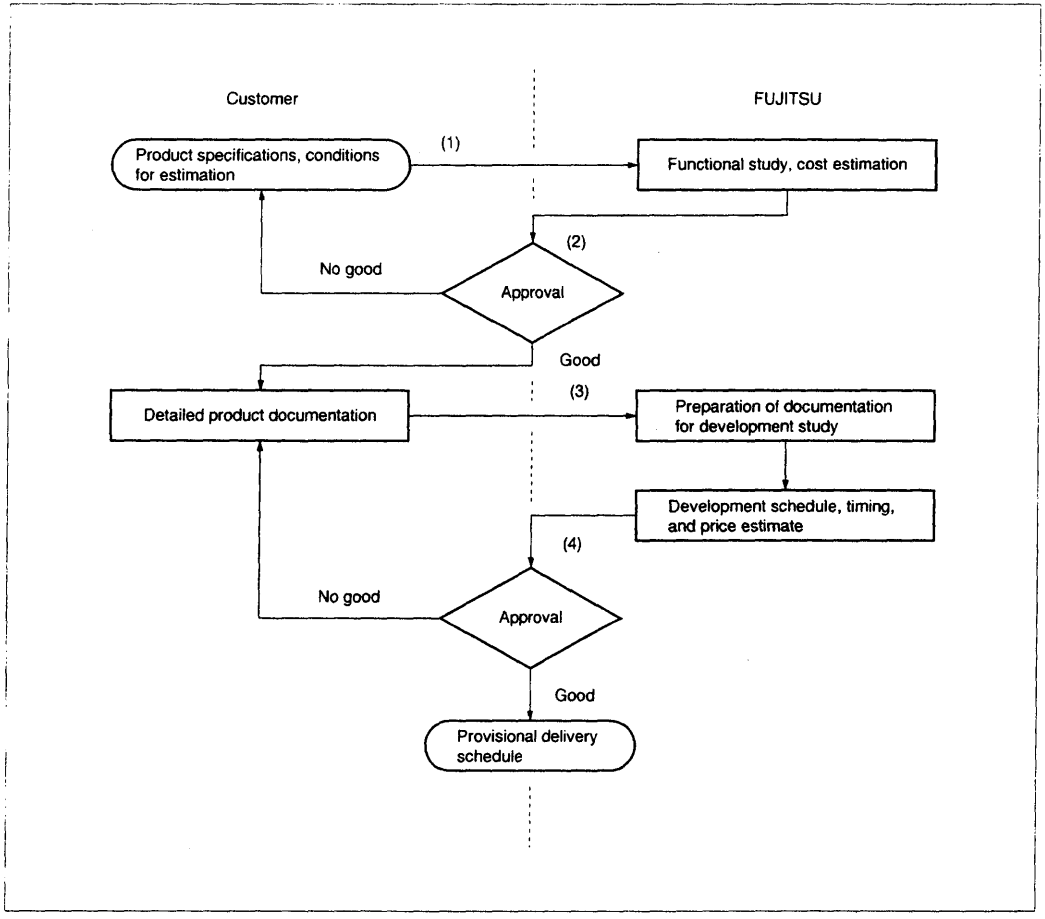
Based on the foregoing studies, FUJITSU and the customer meet to evaluate feasibility.

(3) Development of planned specifications

Circuit functions and characteristics are studied in detail, and circuit specifications and testing specifications are developed. After specifications have been determined, final estimates of the development schedule, timing and cost, and the product price can be produced.

(4) Approval of provisional delivery specifications

After FUJITSU and the customer have determined the feasibility of product development, a provisional delivery schedule is agreed upon.


Customer
FUJITSU
Product specifications, conditions for estimation
(1)
Functional study, cost estimation
(2)
No good
Approval
Good
Detailed product documentation
(3)
Preparation of documentation for development study
Development schedule, timing, and price estimate
(4)
No good
Approval
Good
Provisional delivery schedule

2. LSI Development

(1) LSI design, prototype development

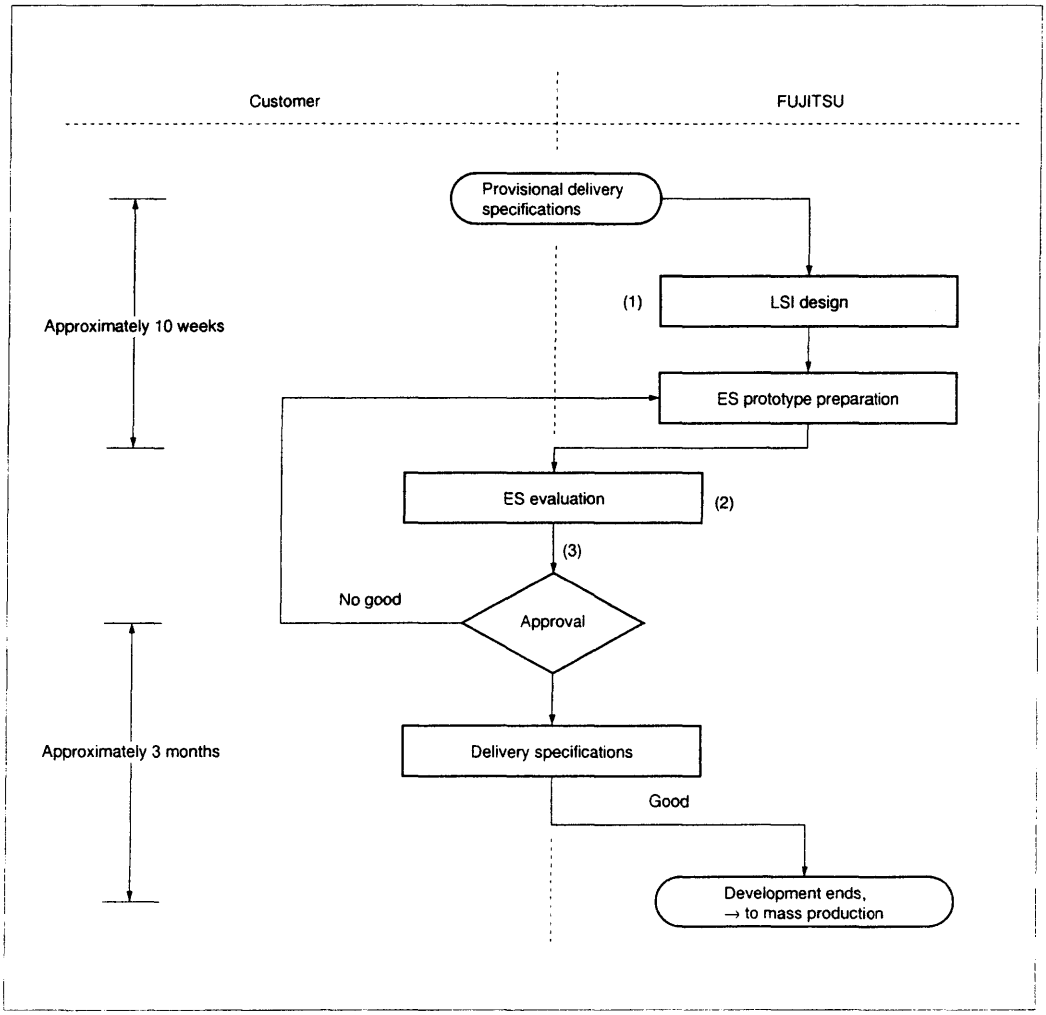
Based on the provisional delivery specifications agreed by the customer and FUJITSU, chip design and prototype work begins. The standard time required for an ES prototype is approximately 10 weeks from the approval of provisional delivery specifications.

(2) ES (engineering sample) evaluation

Both the customer and FUJITSU evaluate the ES prototype based on the provisional delivery specifications.

(3) Final approval

If there are no problems with the evaluation, FUJITSU and the customer agree on final delivery specifications and end development, moving to the mass production stage. The standard lead time for delivery of mass production products is approximately three months.



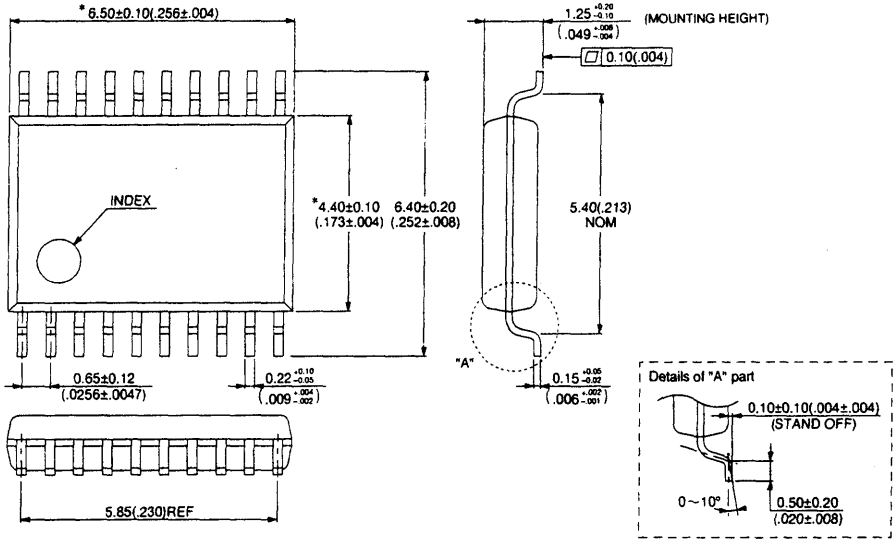
■ ORDERING INFORMATION

Part number	Package	Remarks
MB156XPFV	20 pin Plastic SSOP (FPT-20P-M03)	
MB156XPFV	34 pin Plastic SSOP (FPT-34P-M03)	

■ PACKAGE DIMENSIONS

20 pin Plastic SSOP
(FPT-20P-M03)

* : This dimension does not include resin protraction.



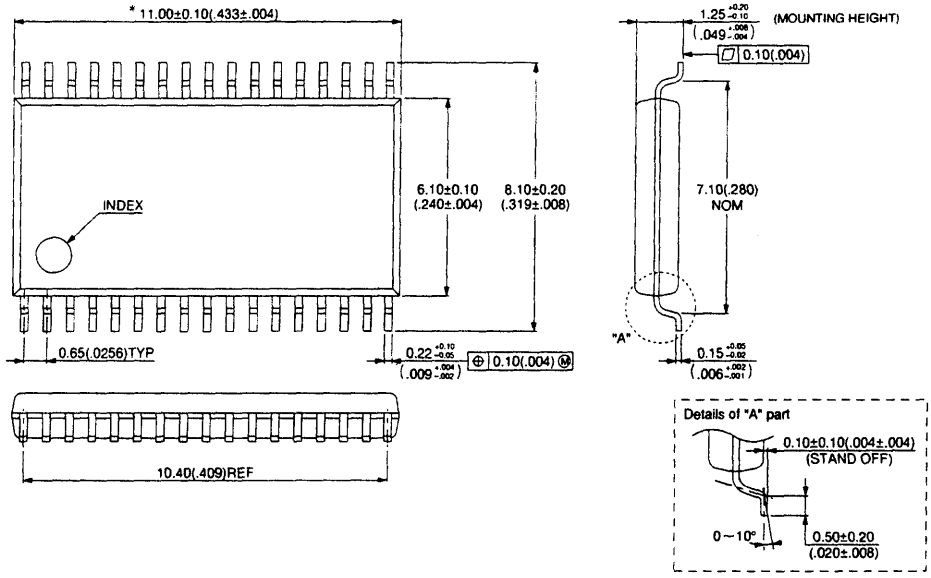
Dimensions in mm (inches)

(Continued)

(Continued)

34 pin Plastic SSOP
(FPT-34P-M03)

* : This dimension does not include resin protraction.



Dimensions in mm (inches)

SECTION 7

Piezoelectric Devices/SAW Filters – *At a Glance*

SECTION 7

F5CC (L2) Series SAW Filters – *At a Glance*

The F5CC (L2) product family is based upon Fujitsu's advanced LiTaO3 technology which provides very sharp roll–off characteristics and excellent temperature stability, with the addition of a 50 Ω impedance matching network integrated into the filter. This is a very popular and cost effective feature, as it reduces the number of external components. In addition to its superior performance compared to other technologies, the F5CC series comes in a smaller 3.8 x 3.8 mm surface mount package for those size and weight sensitive applications.

See Page 7-7.

(* New devices – Data not included in this edition.)

Part Number	Standard	Use	Center Frequency (MHz)	Passband Width (MHz)	Comment
FAR–F5CC–836M50–L2AA	AMPS/ IS–136/IS–95	Tx	836.5	25	
FAR–F5CC–836M50–L2AZ	AMPS/ IS–136/IS–95	Tx	836.5	25	High stopband attenuation
FAR–F5CC–881M50–L2AB	AMPS/ IS–136/IS–95	Rx	881.5	25	
FAR–F5CC–881M50–L2AY	AMPS/ IS—136/IS—95	Rx	881.5	25	High stopband attenuation
FAR–F5CC–933M50–L2BA	NTT	Tx	933.5	17	
FAR–F5CC–878M50–L2BB	NTT	Rx	878.5	17	
FAR–F5CC–888M50–L2CA	ETACS	Tx	888.5	33	
FAR–F5CC–933M50–L2CB	ETACS	Rx	933.5	33	
FAR–F5CC–911M50–L2DA	NTACS	Tx	911.5	27	
FAR–F5CC–856M50–L2DB	NTACS	Rx	856.5	27	
FAR–F5CC–902M50–L2EA	NMT/GSM	Tx	902.5	25	
FAR–F5CC–902M50–L2EZ	NMT/GSM	Tx	902.5	25	High stopband attenuation
FAR–F5CC–947M50–L2EB	NMT/GSM	Rx	947.5	25	
FAR–F5CC–947M50–L2EY FAR–F5CC–947M50–L2EX*	NMT/GSM	Rx	947.5	25	High stopband attenuation
FAR–F5CC–897M50–L2KA*	E–GSM	Tx	897.5	35	
FAR–F5CC–942M50–L2KB*	E–GSM	Rx	942.5	35	
FAR–F5CC–942M50–L2KY*	E–GSM	Rx	942.5	35	High stopband attenuation
FAR–F5CC–950M00–L2FA	PDC	Tx	950.0	20	
FAR–F5CC–820M00–L2FB	PDC	Rx	820.0	20	
FAR–F5CC–915M00–L2JA*	900 MHz ISM	Tx/Rx	915.0	26	
FAR–F5CC–915M00–L2JZ*	900 MHz ISM	Tx/Rx	915.0	26	High stopband attenuation
FAR–F5CC–935M00–L2LA*	2–Way Pager	Tx/Rx	915.0	12	

SECTION 7

F5CB Series SAW Filters – *At a Glance*

The F5CB series of $LiTaO_3$ SAW Filters were Fujitsu's initial entry into the high performance SAW Filter market covering many of the major cellular standards under 1 GHz. The F5CB series requires external 50 Ω impedance matching and are supplied in 5 x 5 mm surface mount packages.

See Page 7-37.

Part Number	Standard	Use	Center Frequency (MHz)	Passband Width (MHz)	Comment
FAR–F5CB–836M50–G201	AMPS/ IS–136/IS–95	Tx	836.5	25	
FAR–F5CB–881M50–G201	AMPS/ IS–136/IS–95	Rx	881.5	25	
FAR–F5CB–881M50–G211	AMPS/ IS–136/IS–95	Rx	881.5	25	High stopband attenuation
FAR–F5CB–888M50–G201	ETACS	Tx	888.5	33	
FAR–F5CB–933M50–G202	ETACS	Rx	933.5	33	
FAR–F5CB–933M50–G212	ETACS	Rx	933.5	33	High stopband attenuation
FAR–F5CB–902M50–G201	NMT/GSM	Tx	902.5	25	
FAR–F5CB–947M50–G201	NMT/GSM	Rx	947.5	25	
FAR–F5CB–947M50–G211	NMT/GSM	Rx	947.5	25	High stopband attenuation
FAR–F5CB–911M50–G201	NTACS	Tx	911.5	27	
FAR–F5CB–933M50–G201	NTT	Tx	933.5	17	
FAR–F5CB–878M50–G201	NTT	Rx	878.5	17	

SECTION 7

F6Cx (L2) Series SAW Filters – *At a Glance*

The F6Cx series is similar to the F5CC series in that both have the 50 Ω impedance matching integrated onto the filter. The F6Cx series of SAW Filters is targeted for applications between 1 GHz and 2.5 GHz. Presently available products support Japan's Personal Digital Cellular (PDC) standard (the F6CC series) and Fujitsu has recently added several new standard devices (the F6CE series) to this product line to meet the needs of the emerging PCS standards in the 1.8 GHz to 2 GHz range and of Wireless LAN applications in the 2.4 GHz ISM Band in the US. The F6CC products are available in 3.8 x 3.8 mm surface mount packages and the F6CE products are housed in very small 3 x 3 mm surface mount packages to meet the demands of future communication handsets for small size and light weight.

See Page 7-65.

Part Number	Standard	Use	Center Frequency (MHz)	Passband Width (MHz)	Comment
FAR-F6CC-1G4410-L2ZA	PDC 1.5 GHz	Tx	1441.0	24	3.8 x 3.8 mm
FAR-F6CC-1G4890-L2ZB	PDC 1.5 GHz	Rx	1489.0	24	3.8 x 3.8 mm
FAR-F6CC-1G6190-L2ZN	PDC 1.5 GHz	Lo	1619.0	24	3.8 x 3.8 mm
FAR-F6CE-1G7475-L2YA	DCS 1800	Tx	1747.5	75	3 x 3 mm
FAR-F6CE-1G8425-L2YB	DCS 1800	Rx	1842.5	75	3 x 3 mm
FAR-F6CE-1G8800-L2XA	PCS (US)	Tx	1880.0	60	3 x 3 mm
FAR-F6CE-1G9600-L2XB	PCS (US)	Rx	1960.0	60	3 x 3 mm
FAR-F6CE-2G4500-L2WA	WLAN (US)		2450.0	100	3 x 3 mm

SECTION 7

M2, M3 Series (Resonators, Modulators, VCOs) – *At a Glance*

The M2 and M3 Series of devices are exclusively distributed and supported by PAL–TECH Electronics, Inc. Please contact PAL–TECH with any inquiries regarding these products at:

PAL–TECH Electronics, Inc.
510 N. First Street, Suite 208
San Jose, CA 95112
Phone: (408) 293–2290
Fax: (408) 293–2291

Page Number	Part Number
7-87	M2 Series (D100)
7-95	M2 Series (D300)
7-105	M3 Series (D001)
7-109	M3 Series (D101)

DS04-2310-3aE

FUJITSU

DATA SHEET

F5 SERIES (L2 Type) ASSP
PIEZOELECTRIC SAW BPF

SAW BANDPASS FILTER (700 to 1000 MHz)

DESCRIPTION

F5 series are wideband bandpass filters for use in the 700MHz to 1000MHz of frequency range.

F5 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) that has large electromechanical coupling coefficient. This provides wide bandwidths and exceptional stability.

Our exclusive mounting technology makes F5 series very compact and surface mountable.

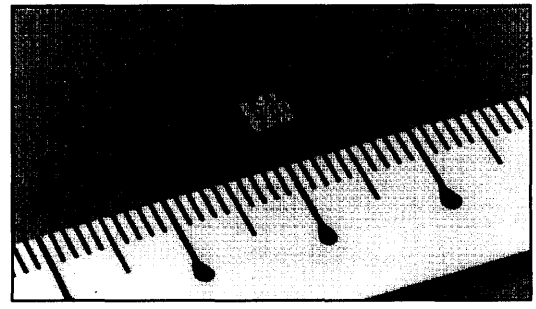
7

The F5 series is most suitable for use in handheld phones of both analog and digital systems.

FEATURES

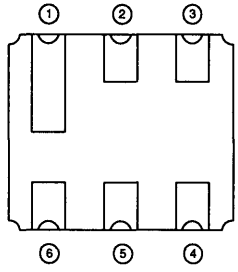
- Ultra compact and light (0.02 cc, 0.1 g)
- Outside matching circuit is unnecessary.
- Surface mount package (SMT)
- Wide variety of bandwidths for worldwide system (AMPS, ADC, ETACS, NMT, GSM, NTT, NTACS, PDC)
- Low insertion loss
- High power rating : 0.2 W garanteed

PACKAGE



PIN ASSIGNMENT

(Bottom view)



Pin No.	Pin name	Description
1	GND	Ground Pin
2	IN	Input Pin
3	GND	Ground Pin
4	GND	Ground Pin
5	OUT	Output Pin
6	GND	Ground Pin

MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	Ta	–30 to +70 *1	°C
Storage temperature	Tstg	–40 to +100	
Maximum input level	Pin	+200	mW
Frequency range	–	700 to 1000	MHz

*1 This is also the Recommended Operating Conditions.

STANDARD FREQUENCIES

STANDARD VERSION

Center frequency (MHz)	Bandwidths (MHz)	System	Part Symbol	Part number
836.5	25	AMPS/ADC (Tx)	A A	FAR-F5CC-836M50-L2AA
881.5	25	AMPS/ADC (Rx)	A B	FAR-F5CC-881M50-L2AB
933.5	17	NTT (Tx)	B A	FAR-F5CC-933M50-L2BA
878.5	17	NTT (Rx)	B B	FAR-F5CC-878M50-L2BB
888.5	33	ETACS (Tx)	C A	FAR-F5CC-888M50-L2CA
933.5	33	ETACS (Rx)	C B	FAR-F5CC-933M50-L2CB
911.5	27	NTACS (Tx)	D A	FAR-F5CC-911M50-L2DA
856.5	27	NTACS (Rx)	D B	FAR-F5CC-856M50-L2DB
902.5	25	NMT/GSM (Tx)	E A	FAR-F5CC-902M50-L2EA
947.5	25	NMT/GSM (Rx)	E B	FAR-F5CC-947M50-L2EB
950.0	20	PDC (Tx)	F A	FAR-F5CC-950M00-L2FA
820.0	20	PDC (Rx)	F B	FAR-F5CC-820M00-L2FB

HIGH ATTENUATION VERSION

Center frequency (MHz)	Bandwidths (MHz)	System	Part Symbol	Part number
836.5	25	AMPS/ADC (Tx)	A Z	FAR-F5CC-836M50-L2AZ
881.5	25	AMPS/ADC (Rx)	A Y	FAR-F5CC-881M50-L2AY
902.5	25	NMT/GSM (Tx)	E Z	FAR-F5CC-902M50-L2EZ
947.5	25	NMT/GSM (Rx)	E Y	FAR-F5CC-947M50-L2EY

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

1. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AA

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	824 to 849 MHz	–	2.0	3.5	dB	
In-band ripple	–	824 to 849 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	869 to 894 MHz	20	27	–	dB	
	–	–	–	–	–	dB	
In-band VSWR	–	824 to 849 MHz	–	1.8	2.0	–	

2. AMPS / ADC system (Rx) Part number : FAR-F5CC-881M50-L2AB

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894 MHz	–	2.5	3.5	dB	
In-band ripple	–	869 to 894 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	DC to 824 MHz	20	23	–	dB	
	–	824 to 849 MHz	20	28	–	dB	
	–	914 to 939 MHz	20	27	–	dB	
	–	939 to 1049 MHz	25	28	–	dB	
	–	1049 to 2000 MHz	20	21	–	dB	
In-band VSWR	–	869 to 894 MHz	–	1.8	2.0	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

3. ETACS system (Tx)

Part number : FAR-F5CC-888M50-L2CA

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	872 to 905 MHz	–	3.0	5.0	dB	
In-band ripple	–	872 to 905 MHz	–	1.5	–	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	917 to 950 MHz	10	15	–	dB	
	–	–	–	–	–	dB	
In-band VSWR	–	872 to 905 MHz	–	2.1	2.5	–	

4. ETACS system (Rx)

Part number : FAR-F5CC-933M50-L2CB

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	917 to 950 MHz	–	3.5	5.5	dB	
In-band ripple	–	917 to 950 MHz	–	2.0	–	dB	
Absolute stopband attenuation	–	DC to 872 MHz	20	32	–	dB	
	–	872 to 900 MHz	25	32	–	dB	
	–	900 to 905 MHz	10	15	–	dB	
	–	1007 to 1040 MHz	30	38	–	dB	
	–	1040 to 2000 MHz	20	26	–	dB	
In-band VSWR	–	917 to 950 MHz	–	2.0	2.5	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

5. NTACS system (Tx)

Part number : FAR–F5CC–911M50–L2DA

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	898 to 925 MHz	–	2.5	3.5	dB	
In–band ripple	–	898 to 925 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	–	–	–	–	–	
	–	843 to 870 MHz	25	29	–	dB	
	–	–	–	–	–	–	
In–band VSWR	–	898 to 925 MHz	–	1.8	2.0	–	

6. NTACS system (Rx)

Part number : FAR–F5CC–856M50–L2DB

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	843 to 870 MHz	–	2.5	3.5	dB	
In–band ripple	–	843 to 870 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	DC to 733 MHz	23	25	–	dB	
	–	733 to 760 MHz	35	40	–	dB	
	–	760 to 815 MHz	25	29	–	dB	
	–	898 to 953 MHz	25	35	–	dB	
	–	953 to 980 MHz	35	40	–	dB	
	–	980 to 1100 MHz	25	30	–	dB	
	–	1100 to 2000 MHz	20	21	–	dB	
In–band VSWR	–	843 to 870 MHz	–	1.9	2.5	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

7. NMT / GSM system (Tx) Part number : FAR-F5CC-902M50-L2EA

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	890 to 915 MHz	–	2.0	3.5	dB	
In-band ripple	–	890 to 915 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	835 to 960 MHz	20	27	–	dB	
	–	–	–	–	–	dB	
In-band VSWR	–	890 to 915 MHz	–	1.8	2.0	–	

8. NMT / GSM system (Rx) Part number : FAR-F5CC-947M50-L2EB

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	935 to 960 MHz	–	2.5	3.5	dB	
In-band ripple	–	935 to 960 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	DC to 800 MHz	20	25	–	dB	
	–	890 to 915 MHz	20	28	–	dB	
	–	980 to 1025 MHz	15	28	–	dB	
	–	1025 to 1070 MHz	35	40	–	dB	
	–	1070 to 1105 MHz	30	35	–	dB	
	–	1105 to 1600 MHz	20	25	–	dB	
	–	1600 to 2000 MHz	15	20	–	dB	
In-band VSWR	–	935 to 960 MHz	–	1.9	2.5	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

9. PDC system (Tx) Part number : FAR-F5CC-950M00-L2FA

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	940 to 960 MHz	–	2.0	3.0	dB	
In-band ripple	–	940 to 960 MHz	–	0.6	1.5	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	810 to 830 MHz	20	25	–	dB	
	–	–	–	–	–	dB	
In-band VSWR	–	940 to 960 MHz	–	1.8	2.0	–	

10. PDC system (Rx) Part number : FAR-F5CC-820M00-L2FB

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	810 to 830 MHz	–	3.0	4.0	dB	
In-band ripple	–	810 to 830 MHz	–	0.5	1.5	dB	
Absolute stopband attenuation	–	DC to 740 MHz	20	25	–	dB	
	–	940 to 960 MHz	25	28	–	dB	
	–	1040 to 1060 MHz	25	30	–	dB	
	–	1060 to 2000 MHz	20	26	–	dB	
In-band VSWR	–	810 to 830 MHz	–	1.8	2.0	–	

ELECTRICAL CHARACTERISTICS (HIGH ATTENUATION VERSION)

11. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AZ

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	824 to 849 MHz	–	3.0	4.0	dB	
In-band ripple	–	824 to 849 MHz	–	1.0	2.0	dB	
Absolute stopband attenuation	–	D.C. to 800MHz	25	28	–	dB	
	–	869 to 894 MHz	30	40	–	dB	
	–	894 to 1049 MHz	30	35	–	dB	
	–	1049 to 2000 MHz	20	26	–	dB	
In-band VSWR	–	824 to 849 MHz	–	2.0	2.5	–	

12. AMPS / ADC system (Rx) Part number : FAR-F5CC-881M50-L2AY

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894 MHz	–	2.8	4.0	dB	
In-band ripple	–	869 to 894 MHz	–	1.0	2.0	dB	
Absolute stopband attenuation	–	DC to 779 MHz	25	31	–	dB	
	–	779 to 804 MHz	35	40	–	dB	
	–	804 to 824 MHz	25	31	–	dB	
	–	824 to 849 MHz	20	31	–	dB	
	–	914 to 939 MHz	20	30	–	dB	
	–	939 to 1049 MHz	35	40	–	dB	
	–	1049 to 2000 MHz	20	26	–	dB	
In-band VSWR	–	869 to 894 MHz	–	2.0	2.5	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

1. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AA

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	824 to 849 MHz	–	2.0	3.5	dB	
In-band ripple	–	824 to 849 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	869 to 894 MHz	20	27	–	dB	
	–	–	–	–	–	dB	
In-band VSWR	–	824 to 849 MHz	–	1.8	2.0	–	

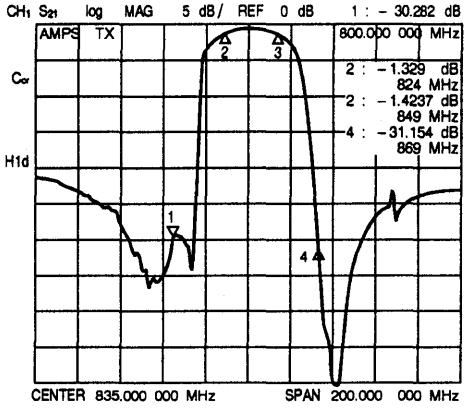
2. AMPS / ADC system (Rx) Part number : FAR-F5CC-881M50-L2AB

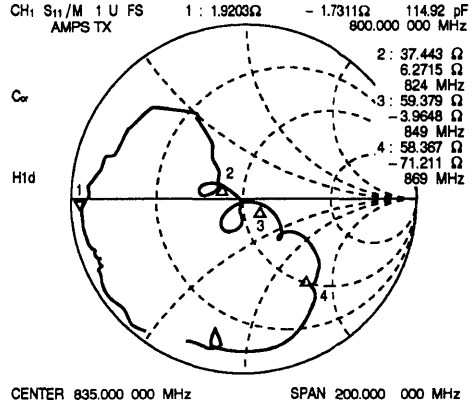
(Ta = -30 to 70°C)

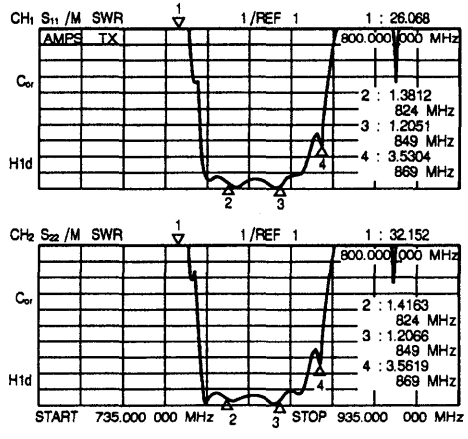
Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894 MHz	–	2.5	3.5	dB	
In-band ripple	–	869 to 894 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	DC to 824 MHz	20	23	–	dB	
	–	824 to 849 MHz	20	28	–	dB	
	–	914 to 939 MHz	20	27	–	dB	
	–	939 to 1049 MHz	25	28	–	dB	
	–	1049 to 2000 MHz	20	21	–	dB	
In-band VSWR	–	869 to 894 MHz	–	1.8	2.0	–	

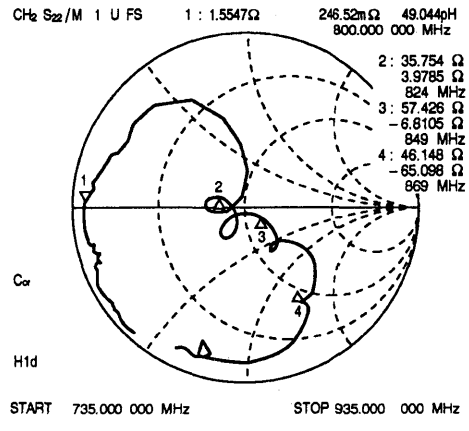
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

1. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AA









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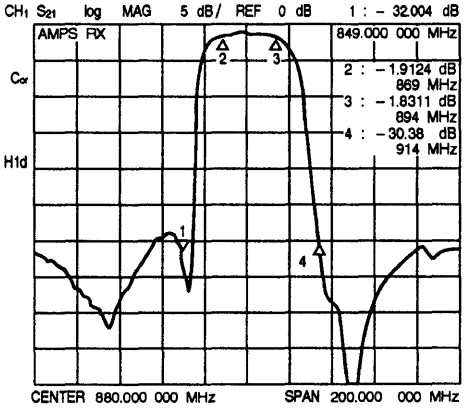
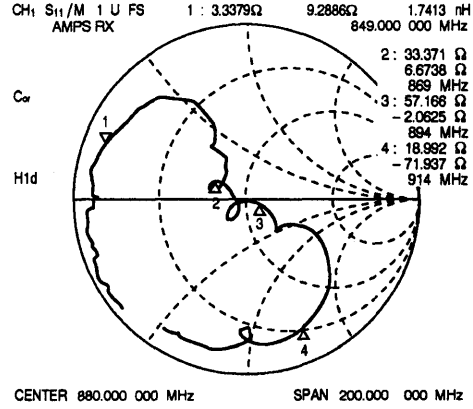
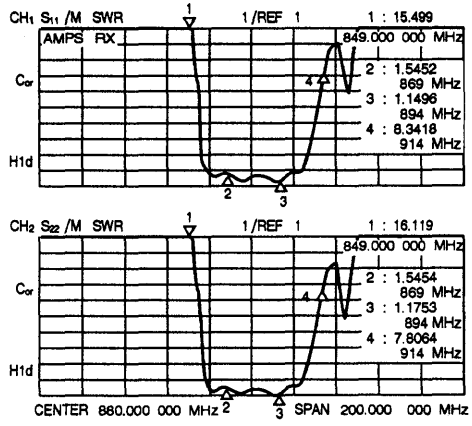
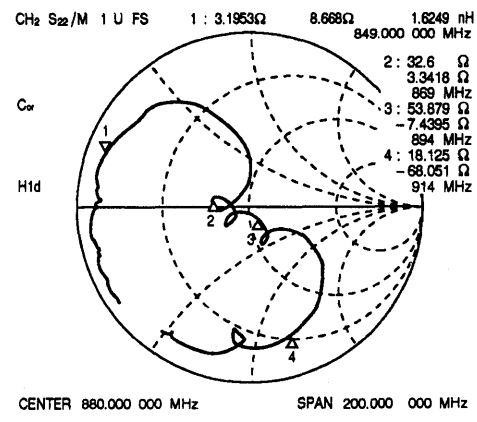
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

2. AMPS / ADC system (Rx) Part number : FAR-F5CC-881M50-L2AB



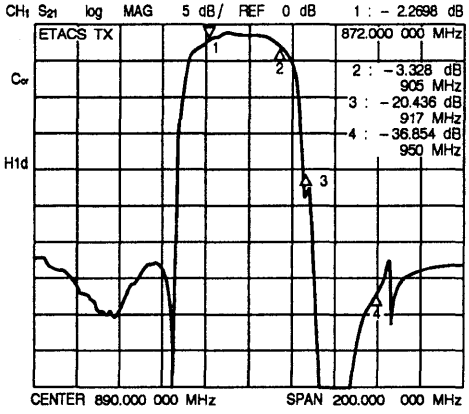


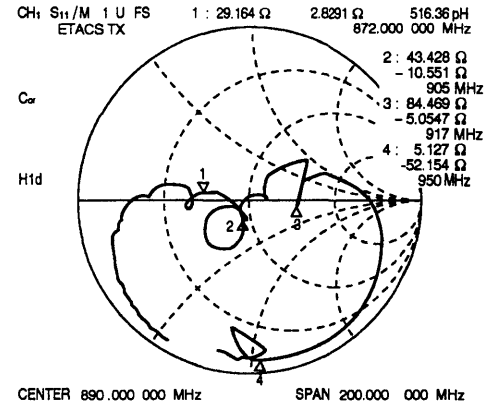


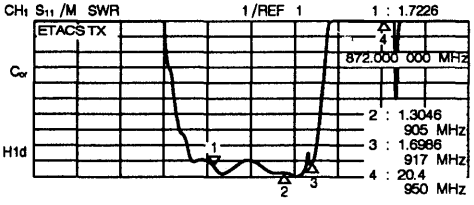


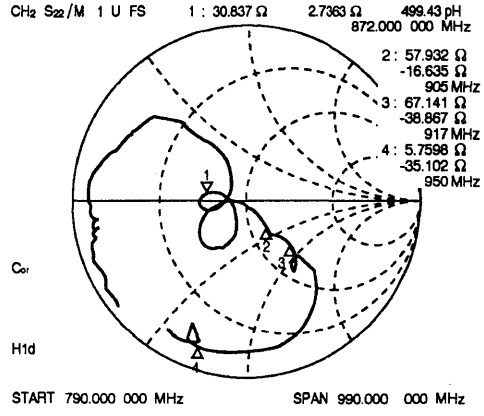
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

3. ETACS system (Tx) Part number : FAR–F5CC–888M50–L2CA









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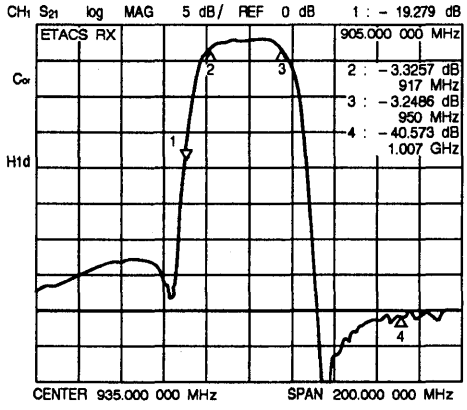
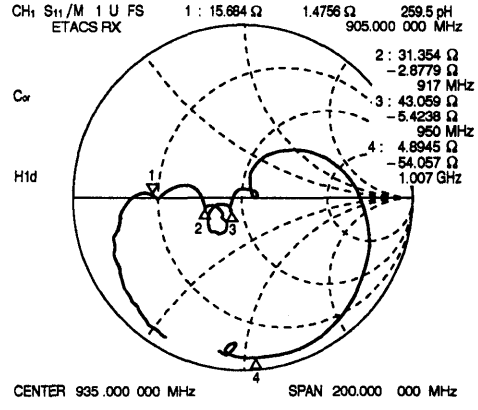
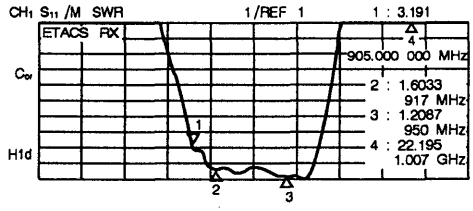
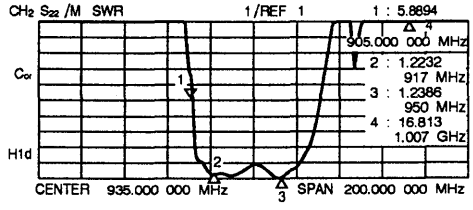
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

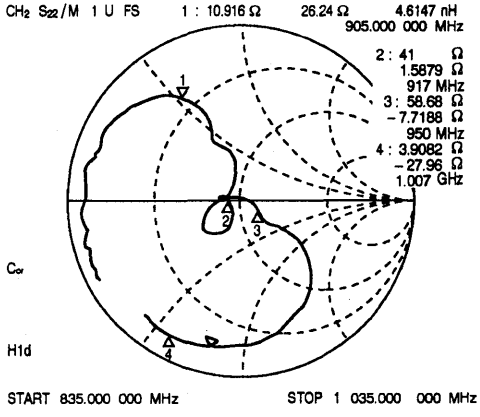
4. ETACS system (Rx) Part number : FAR-F5CC-933M50-L2CB





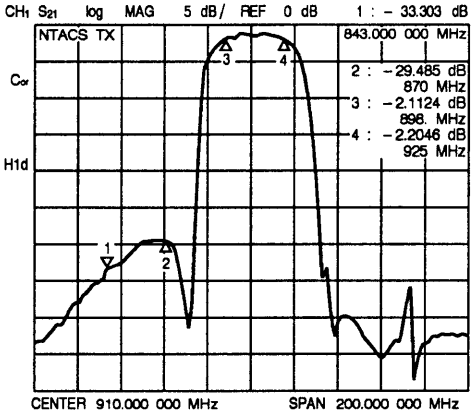


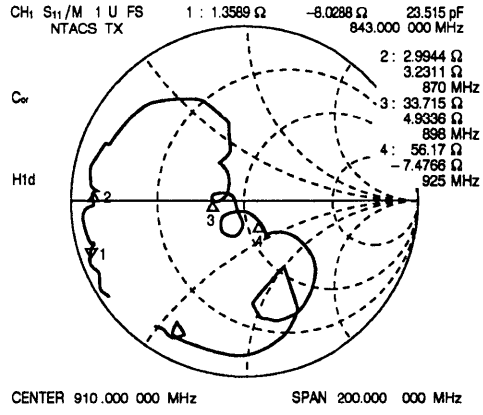


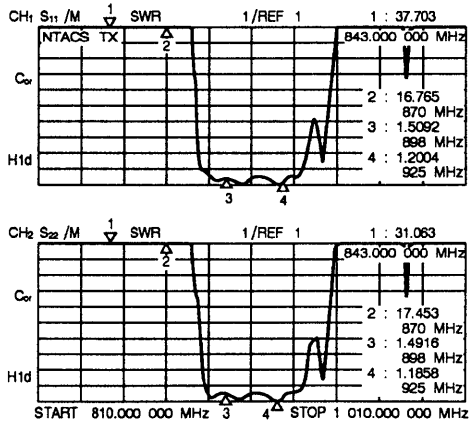


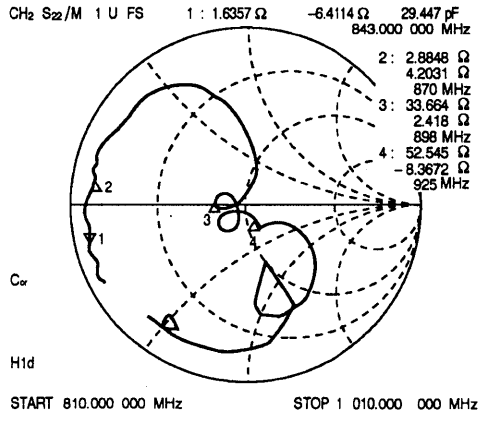
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

5. NTACS system (Tx) Part number : FAR–F5CC–911M50–L2DA









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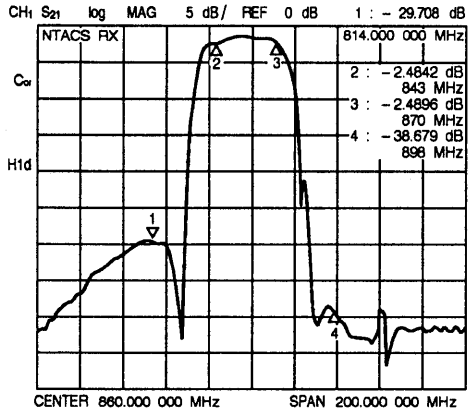
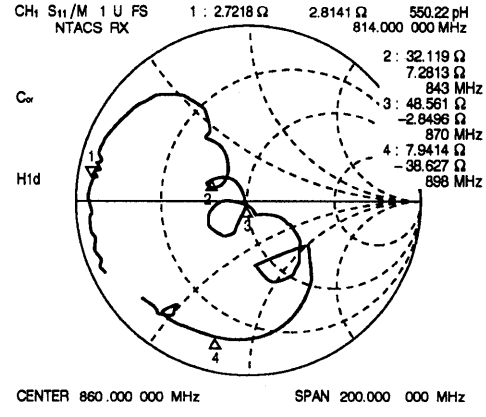
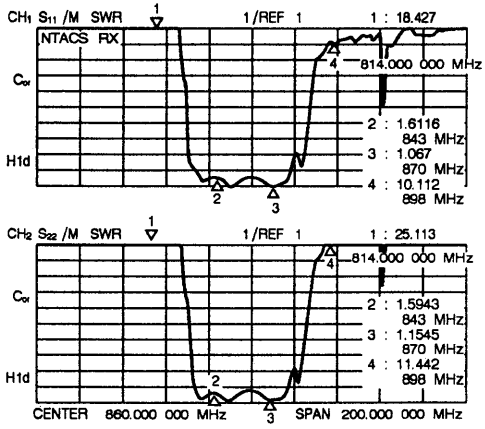
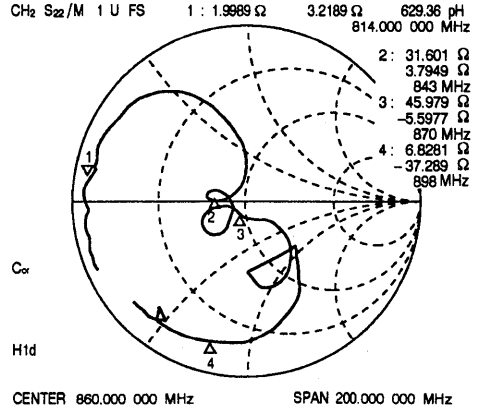
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

6. NTACS system (Rx) Part number : FAR–F5CC–856M50–L2DB



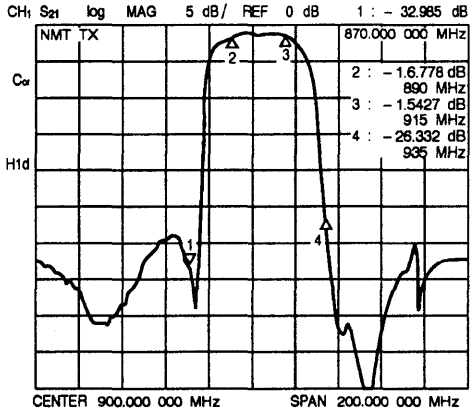


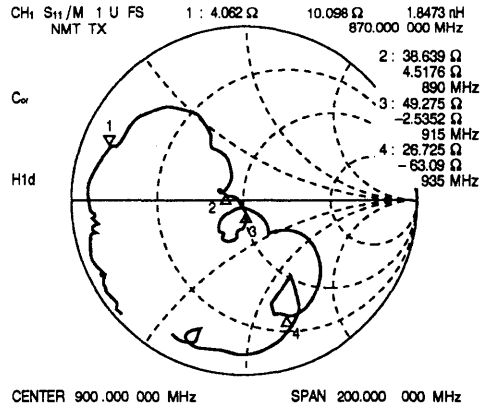


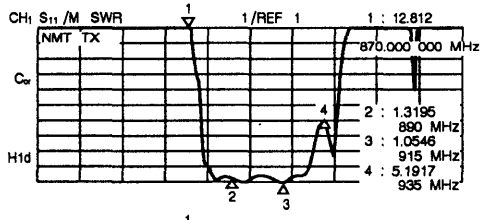


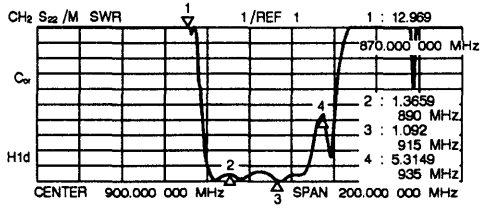
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

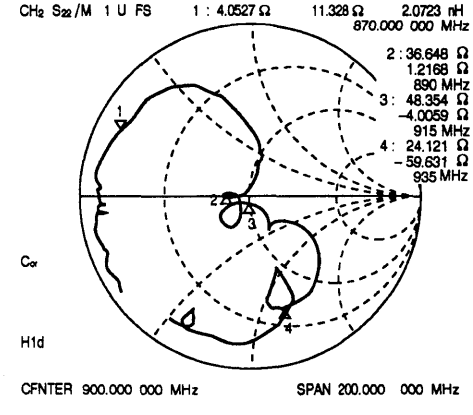
7. NMT / GSM system (Tx) Part number : FAR-F5CC-902M50-L2EA











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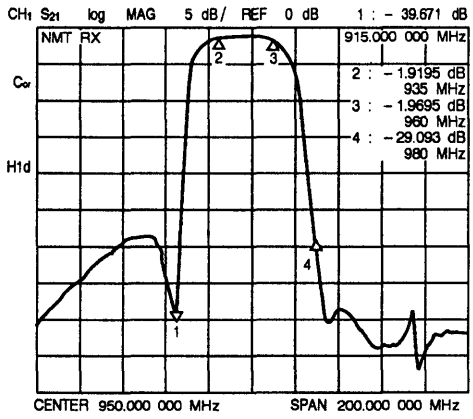
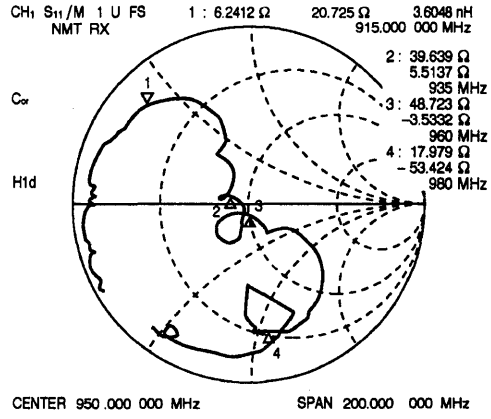
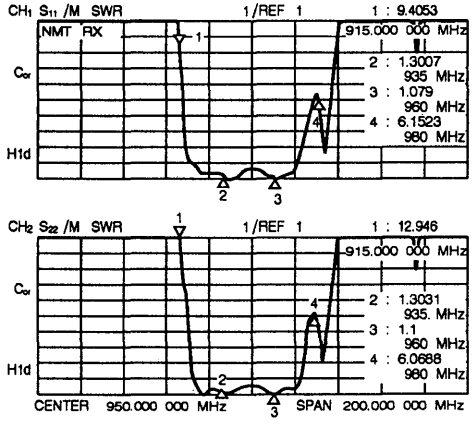
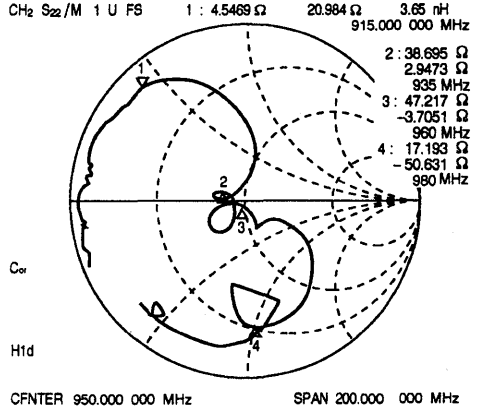
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

8. NMT / GSM system (Rx) Part number : FAR-F5CC-947M50-L2EB



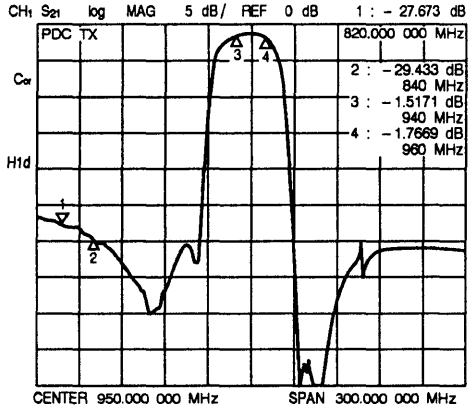


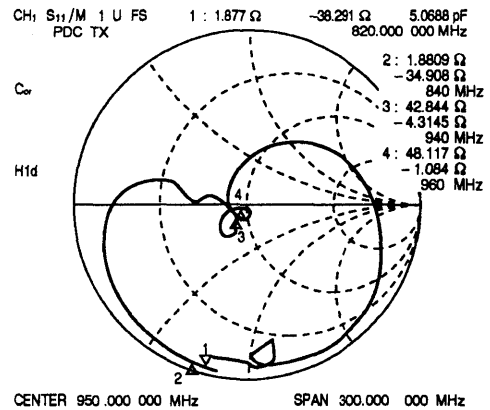


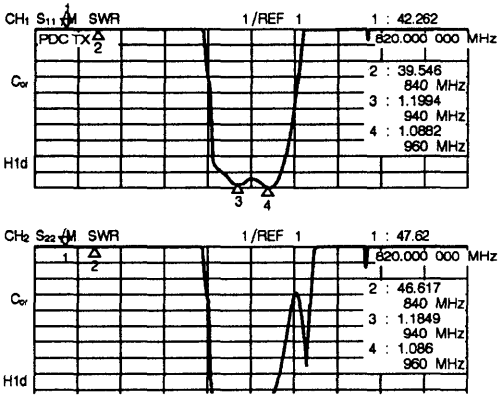


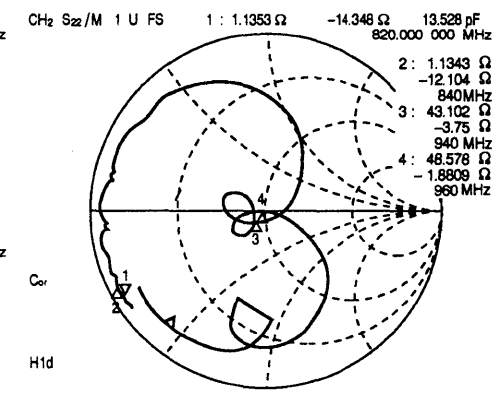
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

9. JDC system (Tx) Part number : FAR-F5CC-950M00-L2FA









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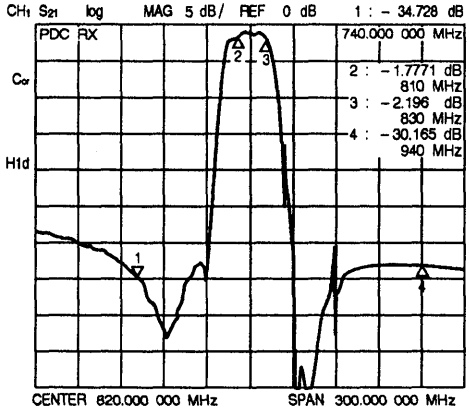
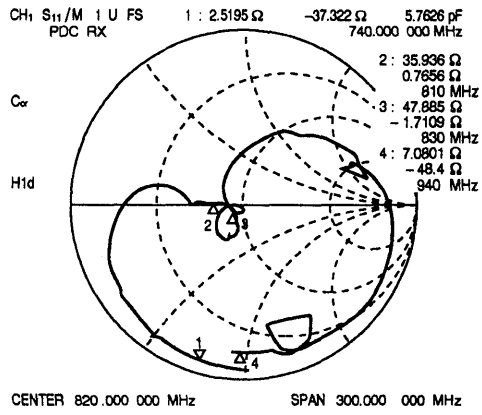
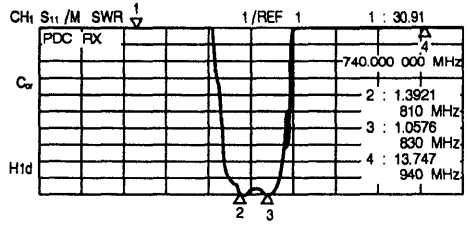
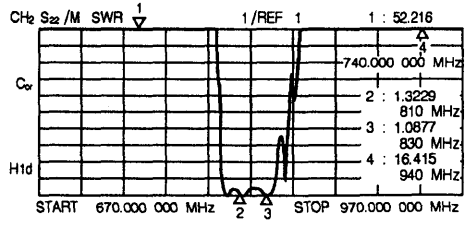
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

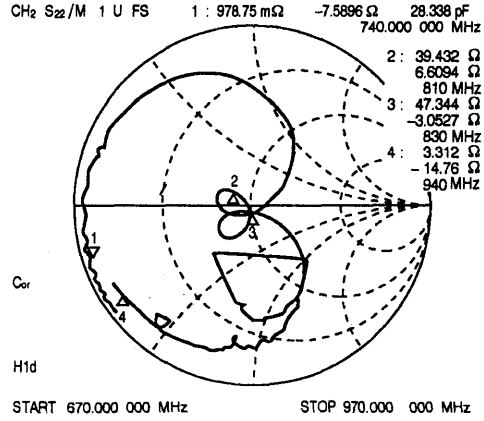
10. JDC system (Rx) Part number : FAR-F5CC-820M00-L2FB





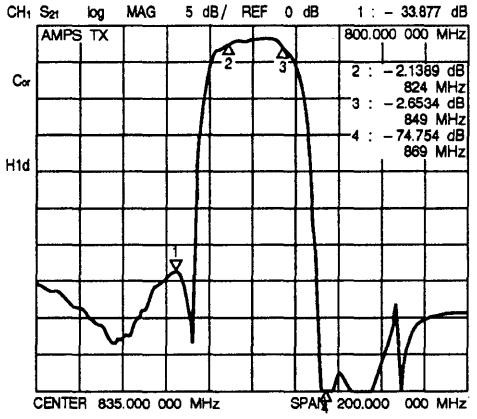


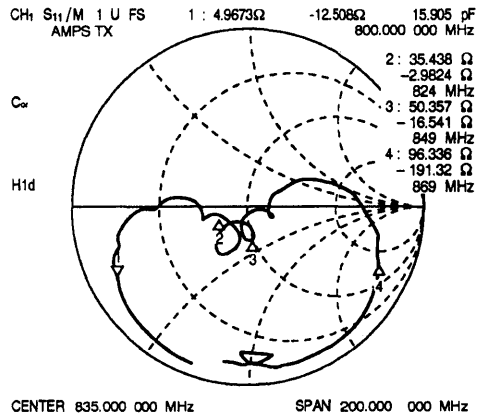


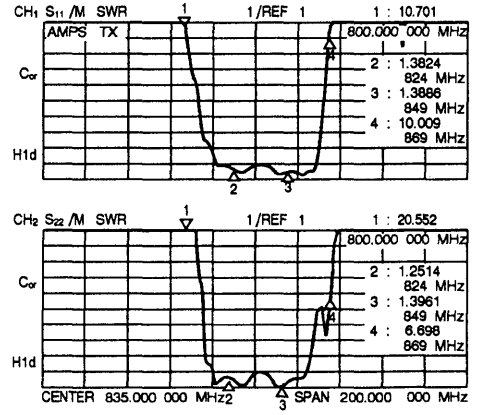


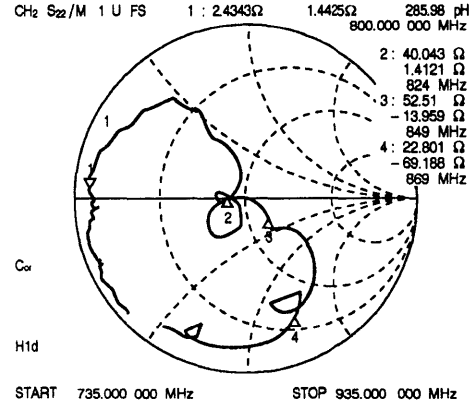
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

11. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AZ









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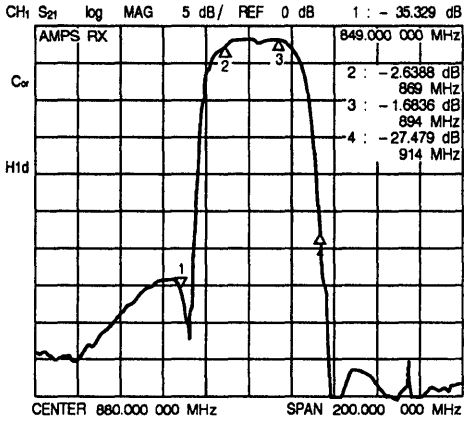
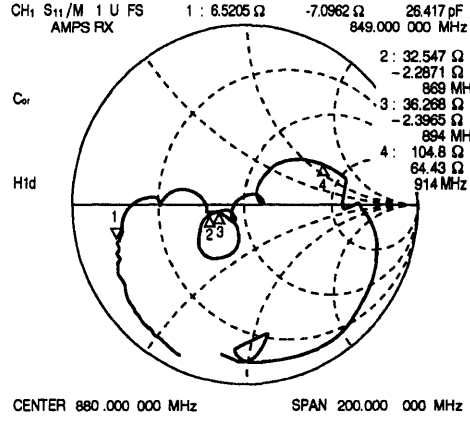
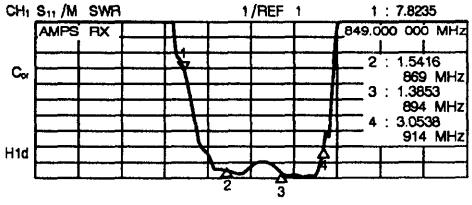
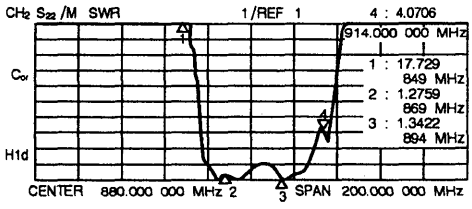
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

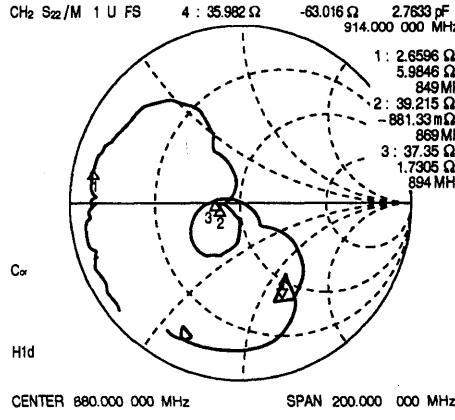
12. AMPS / ADC system (Rx) Part number : FAR-F5CC-881M50-L2AY





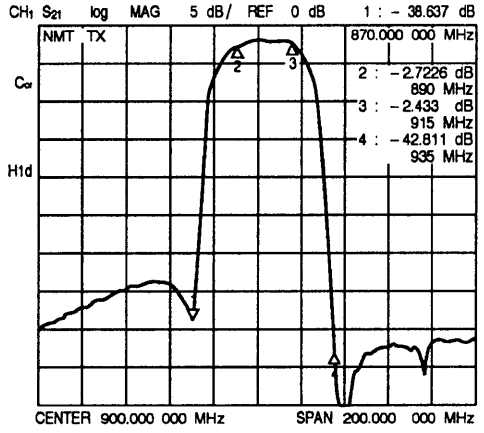


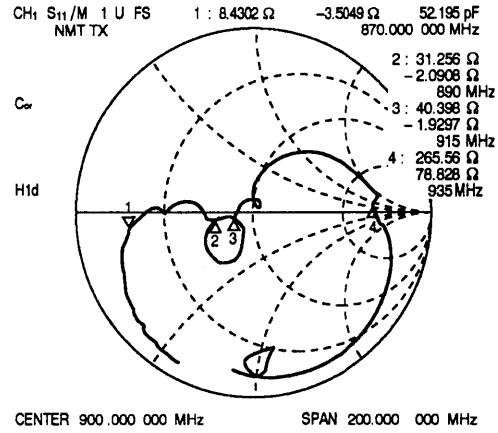


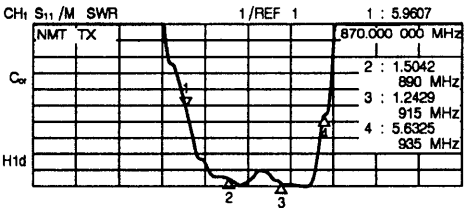


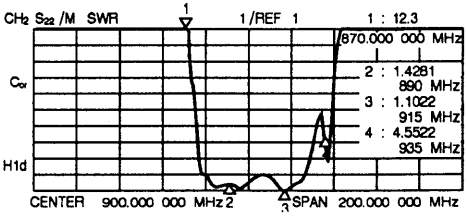
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

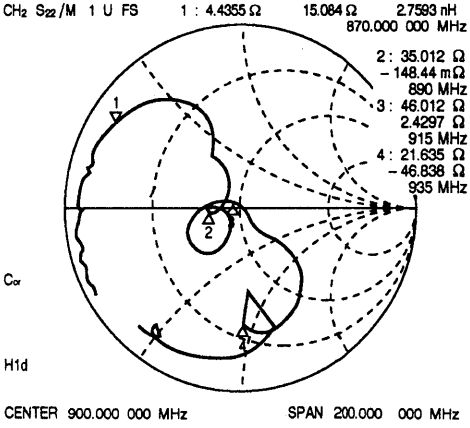
13. NMT / GSM system (Tx) Part number : FAR-F5CC-902M50-L2EZ







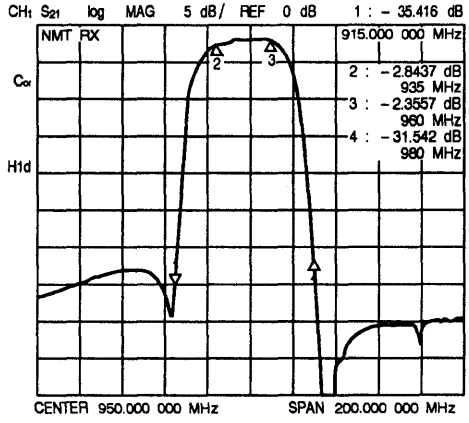


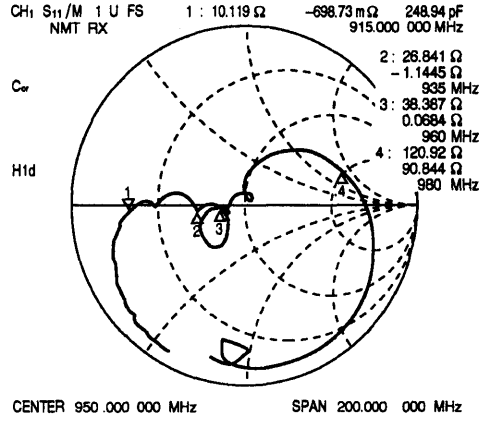


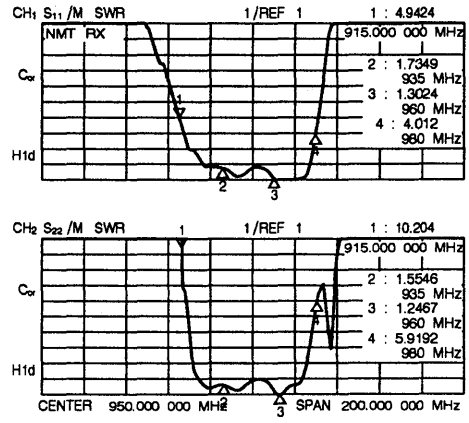
7

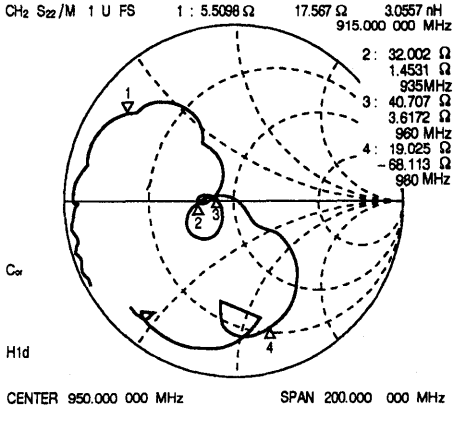
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

14. NMT / GSM system (Rx) Part number : FAR-F5CC-947M50-L2EY

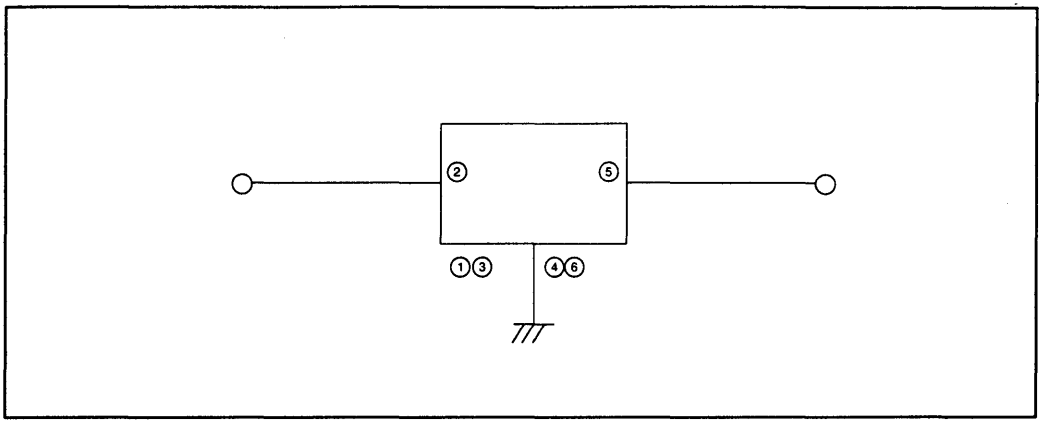








MEASURING CIRCUIT



PART NUMBER DESIGNATION

[Designation example]

FAR-F5CC-□□□□□□ -L2 □□ -□
①　②　③

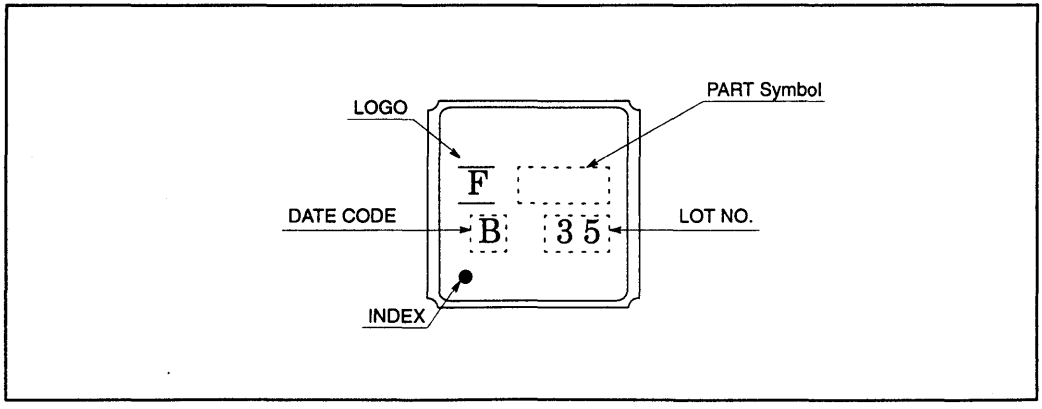
① Frequency designation : Specify the nominal frequency in six alphanumeric characters. Enter M (for MHz) at the decimal point. Refer to STANDARD FREQUENCIES.

② Serial number. : Specify a number from AA to ZZ.

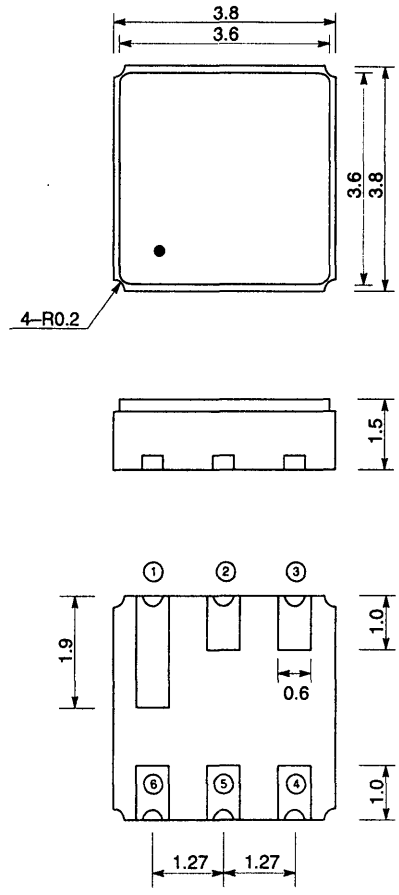
③ Packaging (Reeled tape) : T → 1K pcs/reel
R → 3K pcs/reel

7

MARKING



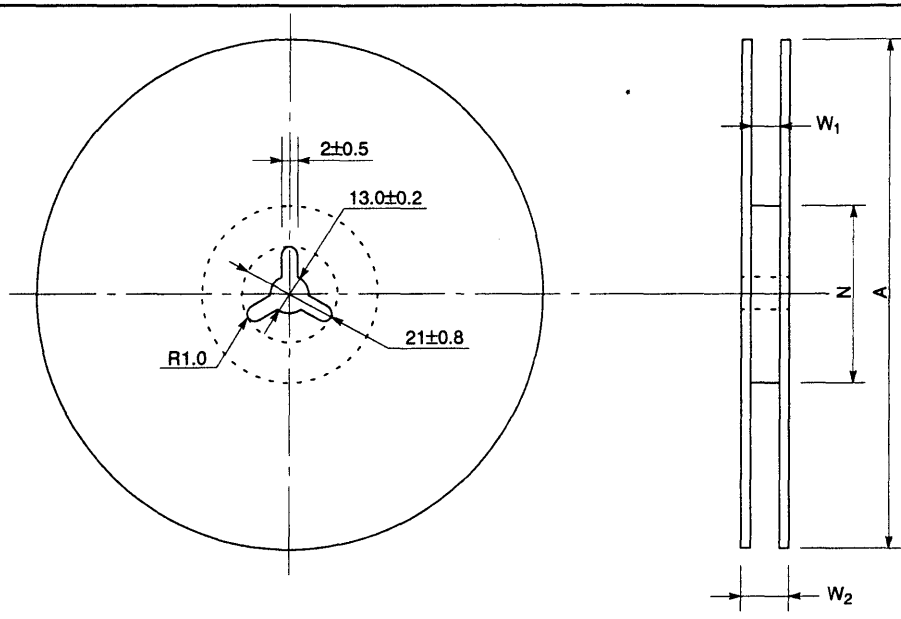
DIMENSIONS



Unit : mm

PACKING : Reel type

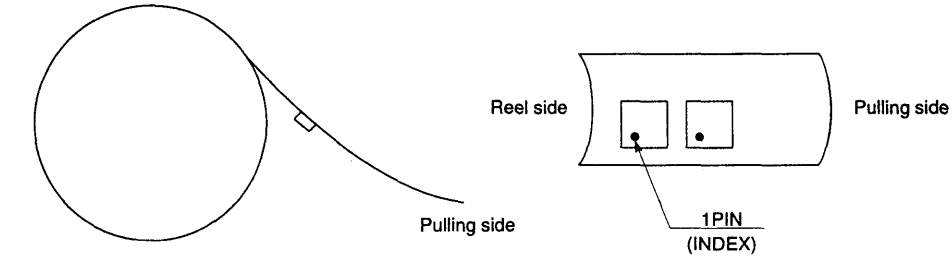
1. Reel dimension



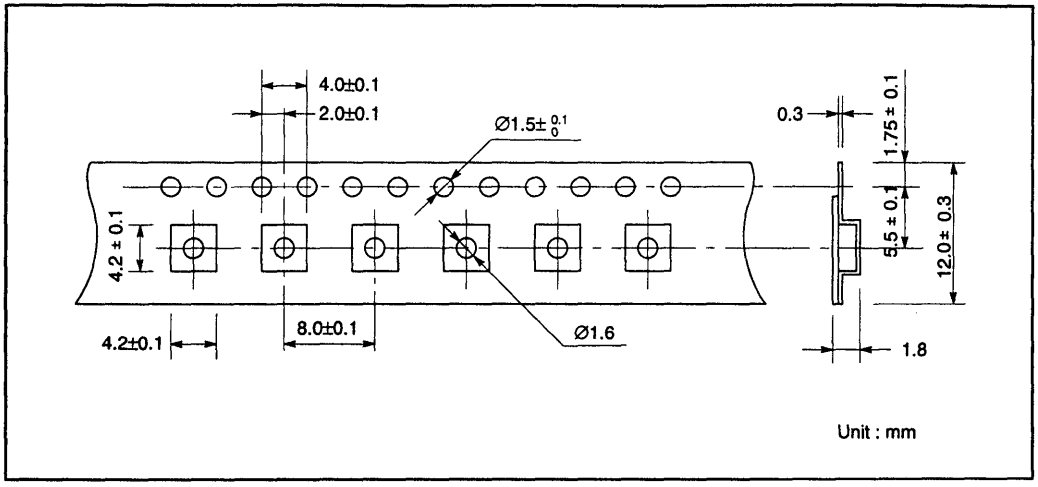
	A	N	W_1	W_2
–T	250	80	$12.4\pm{}^{2.0}_{0.0}$	18.4 or less
–R	330	80	$12.4\pm{}^{2.0}_{0.0}$	18.4 or less

Unit : mm

2. Packing style



3. Tape dimension



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Printed in Japan DS04–23108–3E

June 1992
Edition 2.0A

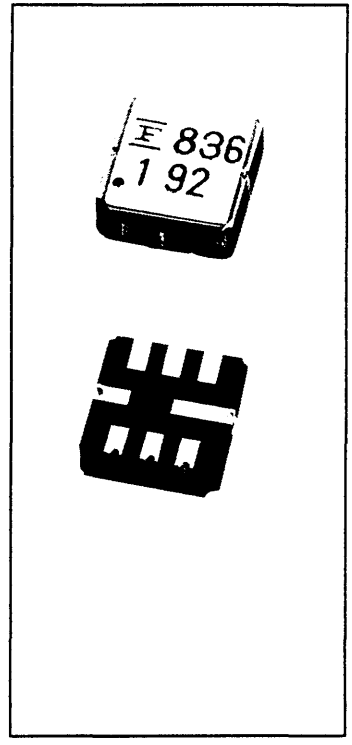
FUJITSU

DATA SHEET

F5CB-***M**-G**-*

F5 Series Piezoelectric SAW Filters SAW-BPF, 700MHz to 1000MHz

The F5 series are wideband bandpass filters for use in the 700MHz to 1000MHz range. The F5 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) with a large electromechanical coupling coefficient that provides wide bandwidths and exceptional stability. Our exclusive mounting technique makes the F5 series very compact and surface mountable. The F5 series is most suitable for use in handheld phones.

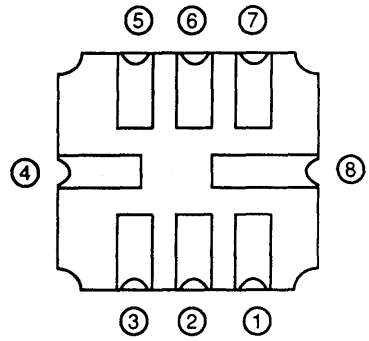


- Considerably smaller and lighter than the dielectric filter (volume and weight are reduced by 1/30)
- Surface mount package (SMT)
- Wide variety of bandwidths for worldwide cellular systems (AMPS, ADC, ETACS, NMT, GSM, NTT, NTACS)
- Low insertion loss
- High power rating: 0.2 W guaranteed
- High stopband attenuation type available for AMPS/ADC, ETACS, NMT/GSM-Rx
- Package and ordering information: – See page 24

7

PIN ASSIGNMENT

(BOTTOM VIEW)



Pin no.	Pin name	Description
1	GND	Ground pin
2	IN	Input pin
3	GND	Ground pin
4	GND	Ground pin
5	GND	Ground pin
6	OUT	Output pin
7	GND	Ground pin
8	GND	Ground pin

MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	T_a	–30 to 70	°C
Storage temperature	T_{stg}	–40 to 100	°C
Maximum input level	P_{in}	200	mW
Frequency range		700 to 1000	MHz

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Operating temperature	t_a	–30 to 70	°C

PART NUMBERS

Tx: Transmitter
Rx: Receiver
Lo: Local Ocillator

No.	Part Number	System	Use	Center Frequency (MHz)	Bandwidth (MHz)	Remarks
1	F5CB-836M50-G201	AMPS/ADC	Tx	836.5	25	
2	F5CB-881M50-G201	AMPS/ADC	Rx	881.5	25	
3	F5CB-881M50-G211	AMPS/ADC	Rx	881.5	25	High stopband attenuation
4	F5CB-888M50-G201	ETACS	Tx	888.5	33	High stopband attenuation
5	F5CB-933M50-G202	ETACS	Rx	933.5	33	
6	F5CB-933M50-G212	ETACS	Rx	933.5	33	High stopband attenuation
7	F5CB-902M50-G201	NMT/GSM	Tx	902.5	25	
8	F5CB-947M50-G201	NMT/GSM	Rx	947.5	25	
9	F5CB-947M50-G211	NMT/GSM	Rx	947.5	25	High stopband attenuation
10	F5CB-911M50-G201	NTACS	Tx	911.5	27	
11	F5CB-856M50-G201	NTACS	Rx	856.5	27	
12	F5CB-933M50-G201	NTT	Tx	933.5	17	
13	F5CB-878M50-G201	NTT	Rx	878.5	17	

ELECTRIC CHARACTERISTICS

1. AMPS/ADC type (Tx)

Part number: F5CB-836M50-G201 T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	824 to 849MHz	—	3.5	4.2	dB	
In-band ripple		824 to 849MHz	—	1.0	1.5	dB	
Stopband attenuation		DC to 800MHz	20	25	—	dB	
		869 to 894MHz	20	25	—	dB	
		894 to 3000MHz	15	20	—	dB	
In-band VSWR		824 to 849MHz	—	1.7	2.0		
Matching constants	C_1			7		pF	
	L_1			9		nH	
	C_2			6		pF	
	L_2			11		nH	

2. AMPS/ADC type (Rx)

Part number: F5CB-881M50-G201 T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894MHz	—	—	4.5	dB	
In-band ripple		824 to 849MHz	—	—	1.5	dB	
Stopband attenuation		DC to 824MHz	20	—	—	dB	
		824 to 849MHz	20	—	—	dB	
		917 to 939MHz	18	—	—	dB	
		947 to 1049MHz	30	—	—	dB	
		1049 to 3000MHz	15	—	—	dB	
In-band VSWR		869 to 894MHz	—	1.8	2.0		
Matching constants	C_1			6		pF	
	L_1			7		nH	
	C_2			7		pF	
	L_2			9		nH	

*: To be determined

3. AMPS/ADC type (Rx)
Part number: F5CB-881M50-G211

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894MHz	—	4.8	5.3	dB	
In-band ripple		869 to 894MHz	—	1.7	2.0	dB	
Stopband attenuation		DC to 824MHz	35	38	—	dB	
		824 to 849MHz	29	35	—	dB	
		914 to 939MHz	20	25	—	dB	
		947 to 1049MHz	40	45	—	dB	
		1049 to 3000MHz	15	—	—	dB	
In-band VSWR		869 to 894MHz	—	1.6	2.0		
Matching constants	C_1			6		pF	
	L_1			8		nH	
	C_2			6		pF	
	L_2			8		nH	

4. ETACS type (Tx)
Part number: F5CB-888M50-G201

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	872 to 900MHz	—	4.5	5.0	dB	
		900 to 905MHz	—	5.5	6.5	dB	
In-band ripple		872 to 905MHz	—	—	2.5	dB	
Stopband attenuation		DC to 847MHz	20	25	—	dB	
		847 to 860MHz	8	12	—	dB	
		917 to 920MHz	10	13	—	dB	
		920 to 922MHz	13	15	—	dB	
		922 to 950MHz	20	23	—	dB	
		962 to 995MHz	30	33	—	dB	
		995 to 3000MHz	15	20	—	dB	
In-band VSWR		872 to 905MHz	—	2.0	2.5		
Matching constants	C_1			7		pF	
	L_1			7		nH	
	C_2			6		pF	
	L_2			9		nH	

7

5. ETACS type (Rx)
Part number: F5CB-933M50-G202

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	917 to 947MHz	—	4.5	5.0	dB	
		947 to 950MHz	—	5.5	6.5	dB	
In-band ripple		917 to 950MHz	—	1.0	2.5	dB	
Stopband attenuation		DC to 872MHz	20	25	—	dB	
		872 to 900MHz	15	18	—	dB	
		900 to 902MHz	13	15	—	dB	
		902 to 905MHz	8	13	—	dB	
		962 to 965MHz	10	15	—	dB	
		965 to 970MHz	15	18	—	dB	
		970 to 995MHz	20	25	—	dB	
		1005 to 1040MHz	30	33	—		
		1040 to 3000MHz	15	20	—		
In-band VSWR		917 to 950MHz	—	2.3	2.5		
Matching constants	C_1			6		pF	
	L_1			6		nH	
	C_2			7		pF	
	L_2			8		nH	

6. ETACS type (Rx)
Part number: F5CB-933M50-G212

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	917 to 950MHz	—	5.5	6.0	dB	
In-band ripple		917 to 950MHz	—	2.0	2.5	dB	
Stopband attenuation		DC to 872MHz	35	40	—	dB	
		872 to 894MHz	35	38	—	dB	
		894 to 905MHz	15	20	—	dB	
		962 to 964MHz	10	15	—	dB	
		964 to 970MHz	15	20	—	dB	
		970 to 995MHz	20	25	—	dB	
		1005 to 1150MHz	40	45	—	dB	
		1150 to 3000MHz	15	—	—	dB	
In-band VSWR		917 to 950MHz	—	2.3	2.5		
Matching constants	C_1			6		pF	
	L_1			8		nH	
	C_2			6		pF	
	L_2			8		nH	

7. NMT type (Tx)

Part number: F5CB-902M50-G201

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	890 to 915MHz	—	4.0	4.5	dB	
In-band ripple		890 to 915MHz	—	1.3	2.0	dB	
Stopband attenuation		DC to 850MHz	20	25	—	dB	
		850 to 870MHz	15	22	—	dB	
		935 to 960MHz	20	28	—	dB	
		1012 to 1058MHz	30	33	—	dB	
		1058 to 3000MHz	15	20	—	dB	
In-band VSWR		890 to 915MHz	—	1.5	2.0		
Matching constants	C_1			5		pF	
	L_1			6		nH	
	C_2			6		pF	
	L_2			9		nH	

8. NMT type (Rx)

Part number: F5CB-947M50-G201

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	935 to 960MHz	—	4.0	4.5	dB	
In-band ripple		935 to 960MHz	—	1.3	2.0	dB	
Stopband attenuation		DC to 890MHz	20	25	—	dB	
		890 to 915MHz	18	22	—	dB	
		980 to 1005MHz	18	30	—	dB	
		1012 to 1058MHz	28	32	—	dB	
		1089 to 1115MHz	30	32	—	dB	
		1115 to 3000MHz	15	20	—	dB	
In-band VSWR		935 to 960MHz	—	1.5	2.0		
Matching constants	C_1			5		pF	
	L_1			6		nH	
	C_2			6		pF	
	L_2			9		nH	

9. NMT type (Rx)

Part number: F5CB-947M50-G211

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	935 to 960MHz	—	4.7	5.0	dB	
In-band ripple		935 to 960MHz	—	1.5	2.0	dB	
Stopband attenuation		DC to 845MHz	40	45	—	dB	
		845 to 890MHz	30	35	—	dB	
		890 to 915MHz	30	33	—	dB	
		976 to 980MHz	15	20	—	dB	
		980 to 1005MHz	20	23	—	dB	
		1012 to 1058MHz	40	45	—	dB	
		1089 to 1140MHz	40	45	—	dB	
		1140 to 3000MHz	15	—	—	dB	
In-band VSWR		935 to 960MHz	—	2.0	2.5		
Matching constants	C_1			6		pF	
	L_1			8		nH	
	C_2			6		pF	
	L_2			8		nH	

10. NTACS type (Tx)

Part number: F5CB-911M50-G201

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	898 to 925MHz	—	4.0	4.5	dB	
In-band ripple		898 to 925MHz	—	1.5	2.0	dB	
Stopband attenuation		DC to 815MHz	25	27	—	dB	
		815 to 870MHz	22	25	—	dB	
		1008 to 1100MHz	30	33	—	dB	
		1100 to 3000MHz	15	20	—	dB	
In-band VSWR		898 to 925MHz	—	1.8	2.0		
Matching constants	C_1			6		pF	
	L_1			7		nH	
	C_2			5		pF	
	L_2			10		nH	

11. NTACS type (Rx)

Part number: F5CB-856M50-G201

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	843 to 870MHz	—	4.0	4.5	dB	
In-band ripple		843 to 870MHz	—	1.5	2.0	dB	
Stopband attenuation		DC to 814MHz	22	25	—	dB	
		898 to 935MHz	22	25	—	dB	
		935 to 1100MHz	30	33	—	dB	
		1100 to 3000MHz	15	20	—	dB	
In-band VSWR		843 to 870MHz	—	1.8	2.0		
Matching constants	C_1			7		pF	
	L_1			8		nH	
	C_2			7		pF	
	L_2			9		nH	

12. NTT type (Tx)

Part number: F5CB-933M50-G201

T_a=–30 ~ 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	925 to 942MHz	—	3.5	4.2	dB	
In-band ripple		925 to 942MHz	—	1.0	1.5	dB	
Stopband attenuation		DC to 780MHz	20	25	—	dB	
		780 to 797MHz	25	30	—	dB	
		797 to 870MHz	20	25	—	dB	
		870 to 887MHz	25	28	—	dB	
		970 to 1070MHz	20	30	—	dB	
		1070 to 1087MHz	25	30	—	dB	
		1087 to 3000MHz	15	20	—	dB	
In-band VSWR		925 to 942MHz	—	1.8	2.0		
Matching constants	C_1			5		pF	
	L_1			7		nH	
	C_2			—			
	L_2			—			

7

13. NTT type (Rx)

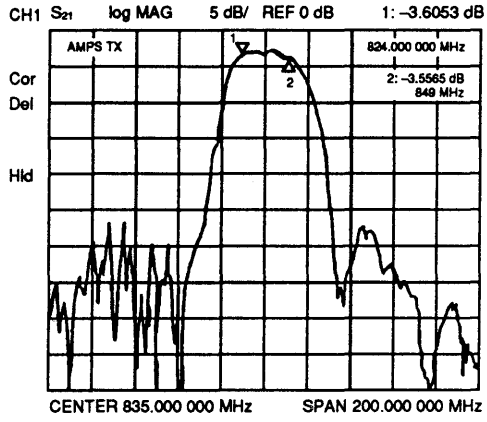
Part number: F5CB-878M50-G201

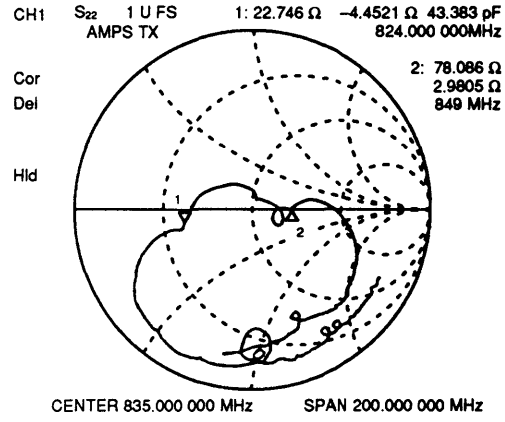
T_a=-30 ~ 70°C

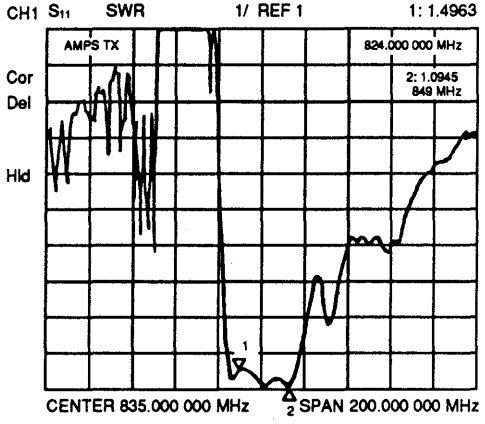
Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	870 to 887MHz	—	3.5	4.2	dB	
In-band ripple		870 to 887MHz	—	1.0	1.5	dB	
Stopband attenuation		DC to 690MHz	20	25	—	dB	
		690 to 707MHz	30	33	—	dB	
		707 to 846MHz	20	25	—	dB	
		925 to 942MHz	25	28	—	dB	
		942 to 3000MHz	15	20	—	dB	
In-band VSWR		870 to 887MHz	—	1.8	2.0		
Matching constants	C_1			5		pF	
	L_1			8		nH	
	C_2			7		pF	
	L_2			10		nH	

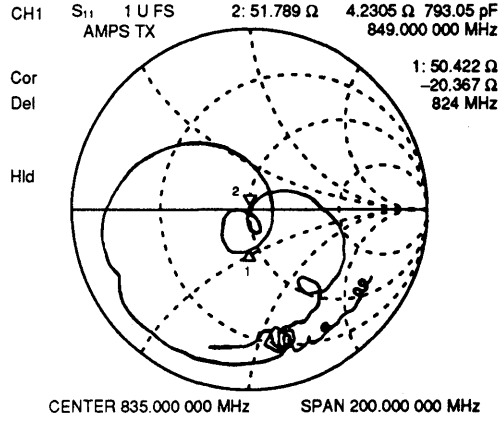
CHARACTERISTIC DATA EXAMPLE

1. AMPS/ADC type (Tx)
   Part number: F5CB-836M50-G201









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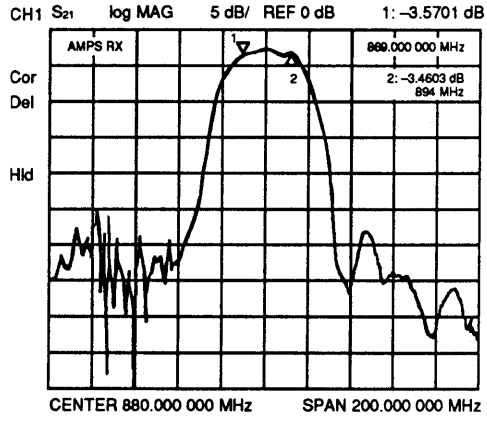
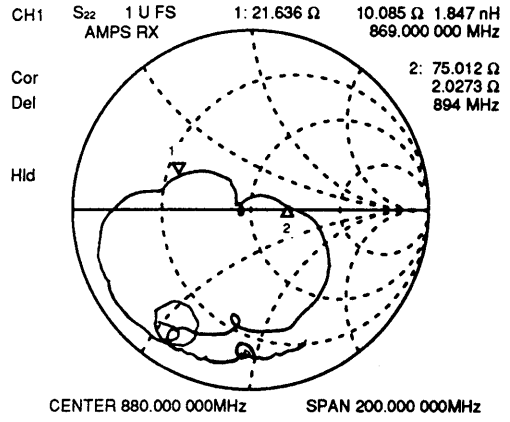
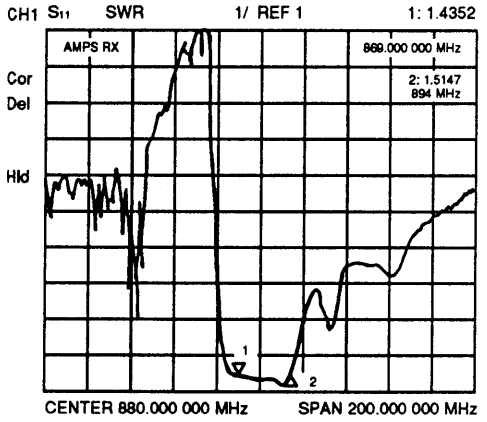
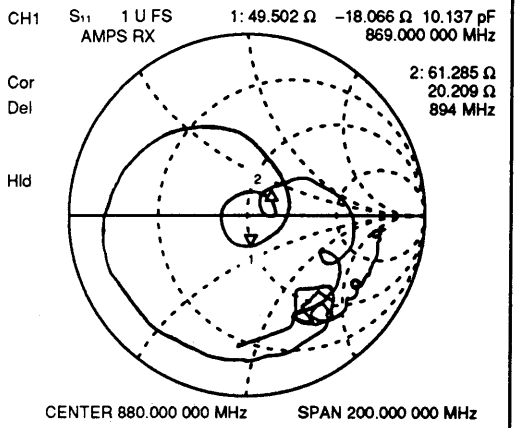
2. AMPS/ADC type (Rx)
   Part number: F5CB-881M50-G201

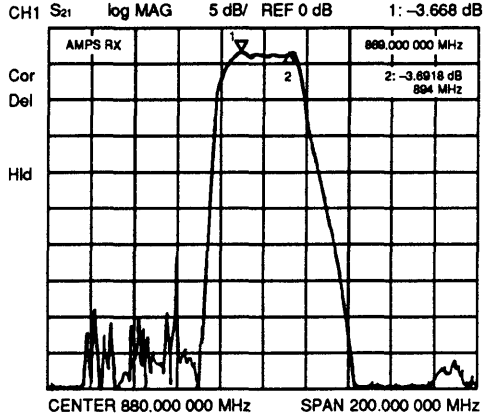


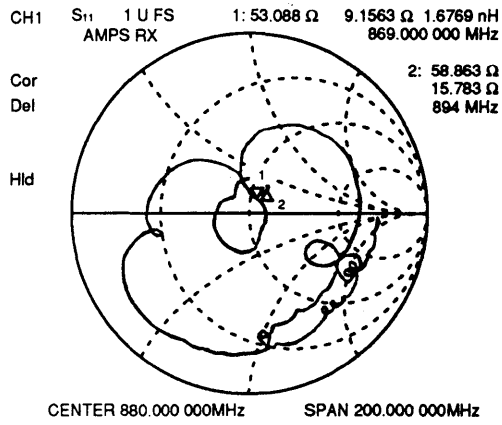


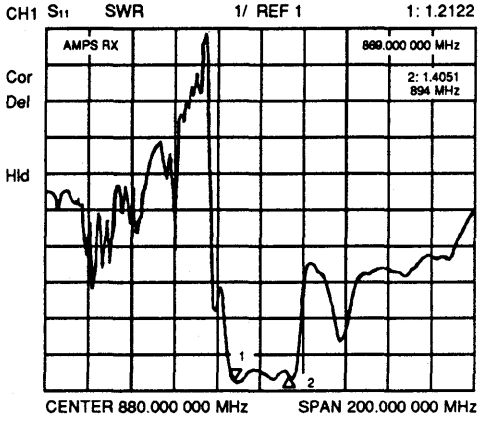


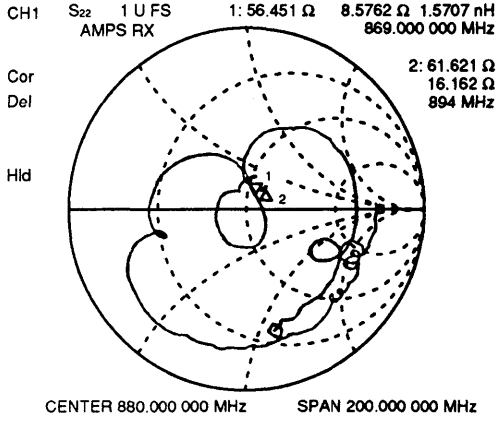


3. AMPS/ADC type (Rx)
Part number: F5CB-881M50-G211



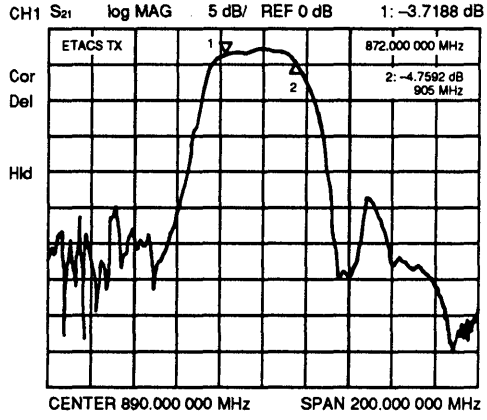


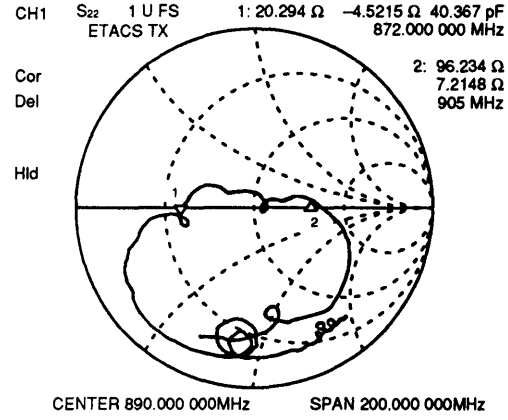


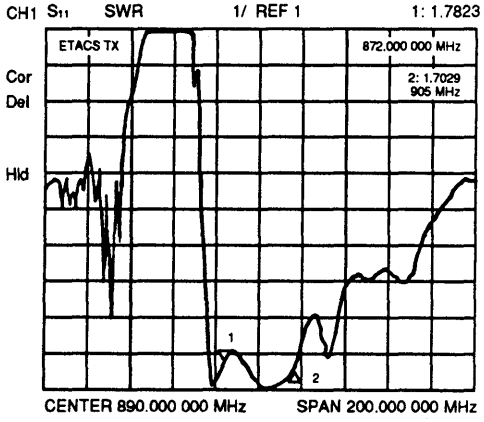


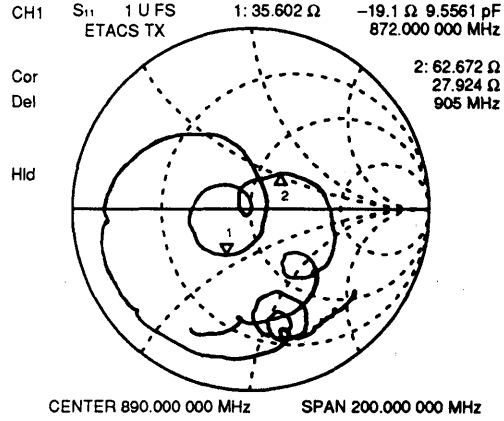
7

4. ETACS type (Tx)
Part number: F5CB-888M50-G201

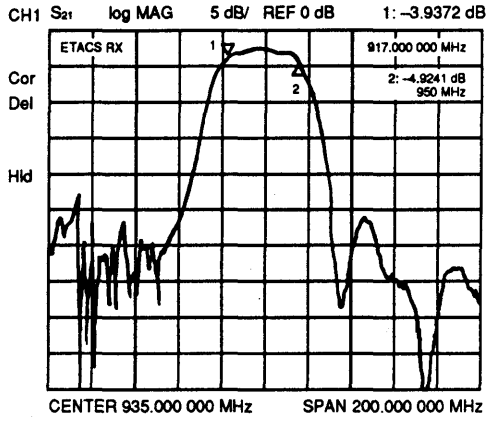


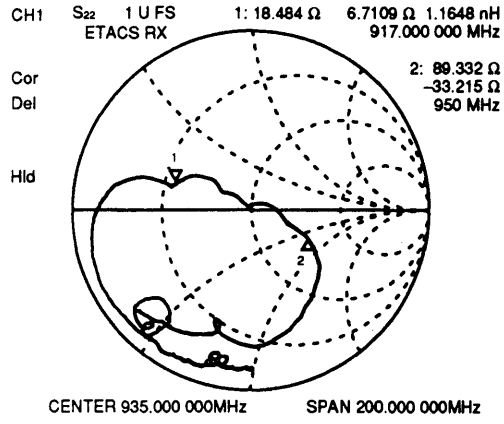


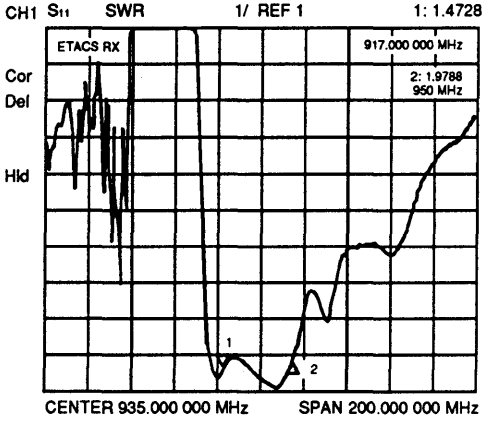


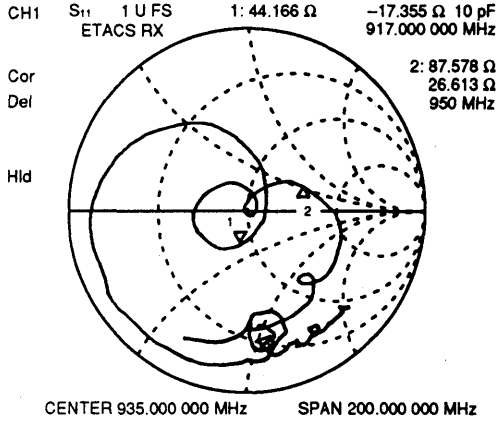


5. ETACS type (Rx)
Part number: F5CB-933M50-G202



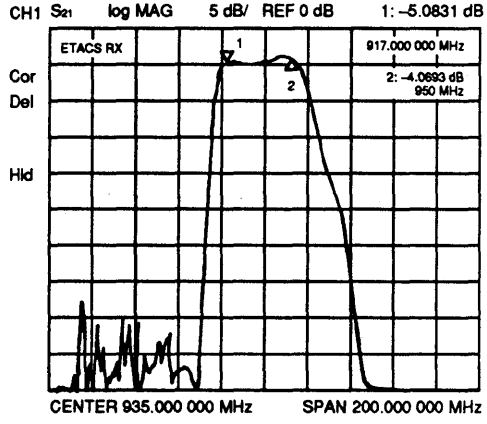


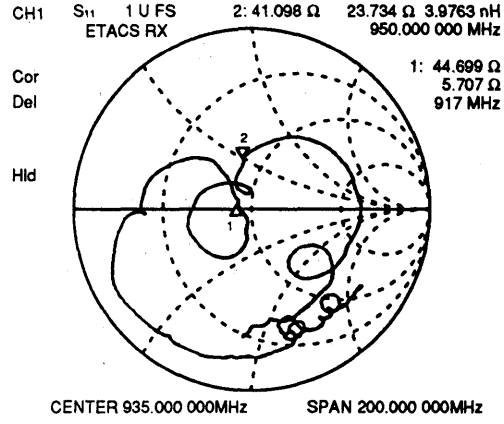


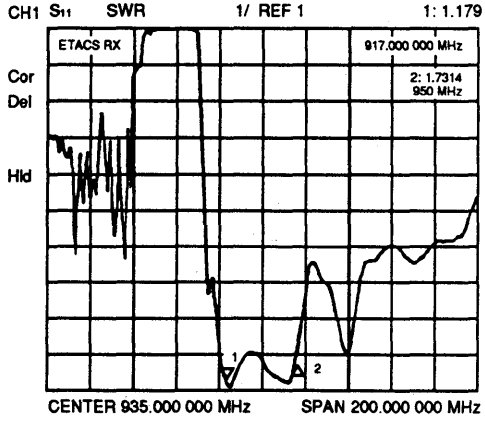


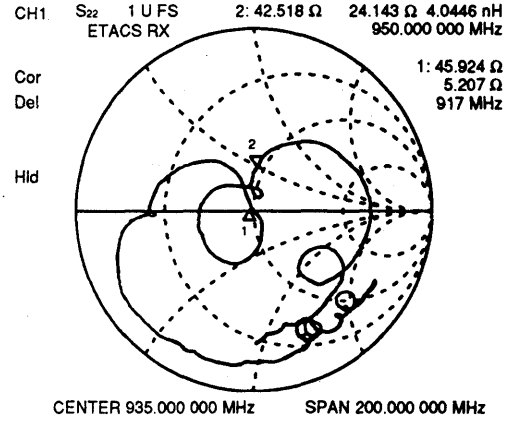
7

6. ETACS type (Rx)
Part number: F5CB-933M50-G212

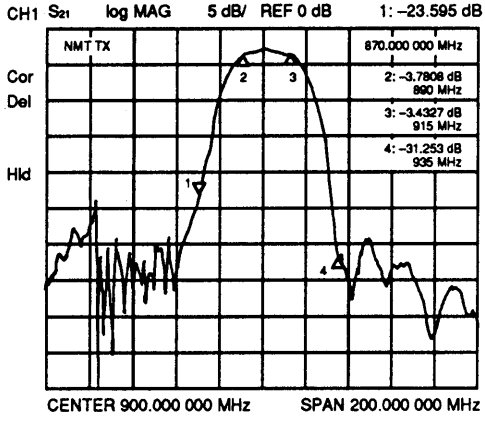


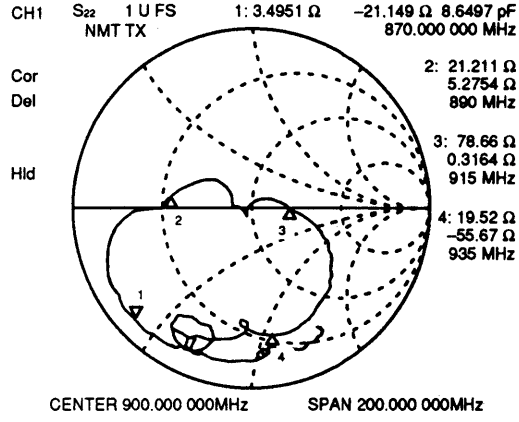


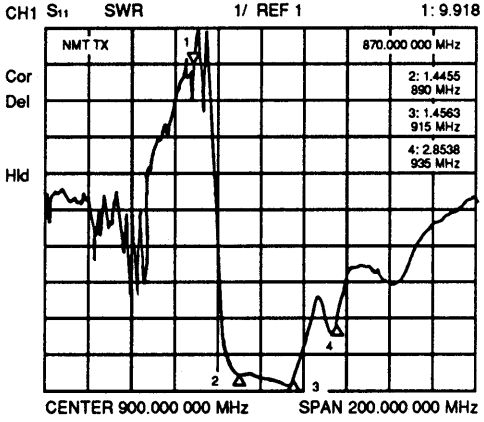


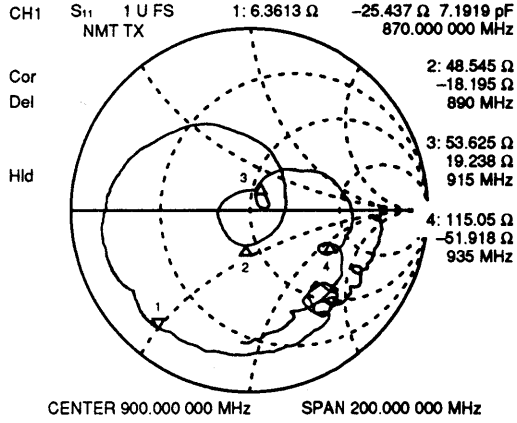


7. NMT/GSM type (Tx)
Part number: F5CB-902M50-G201



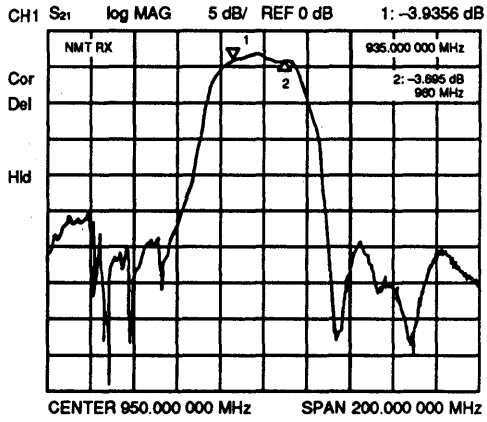


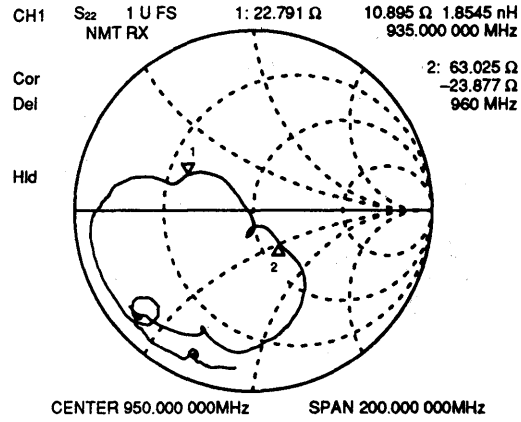


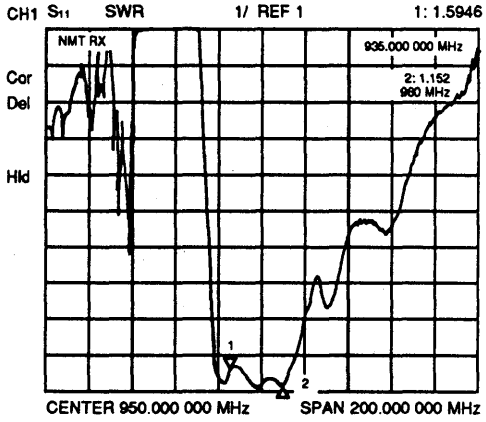


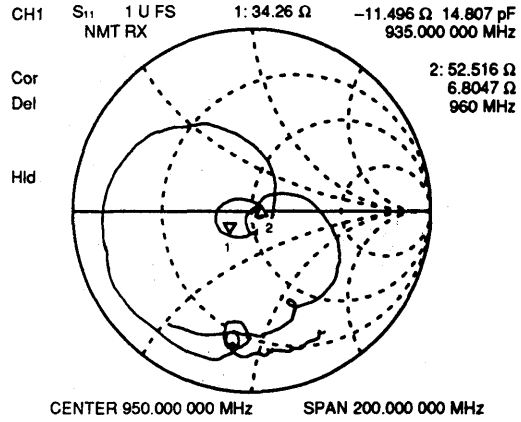
7

8. NMT/GSM type (Rx)
Part number: F5CB-947M50-G201

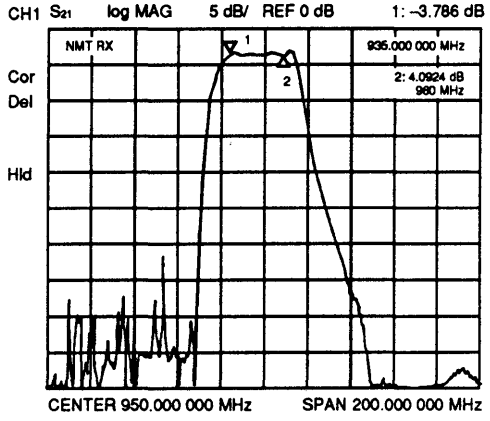


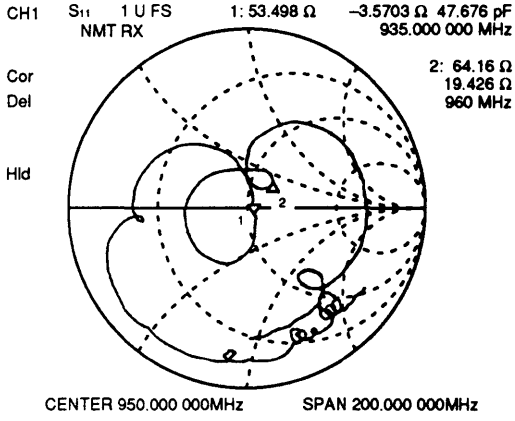


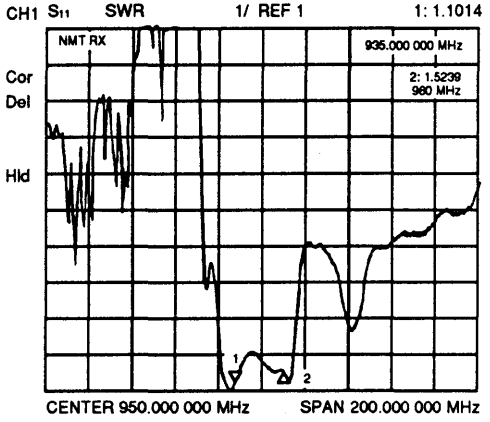


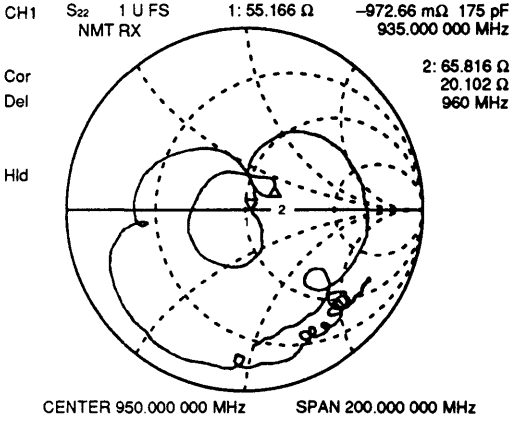


9. NMT/GSM type (Rx)
Part number: F5CB-947M50-G211



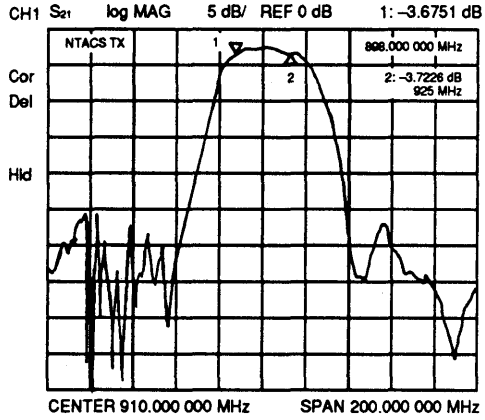


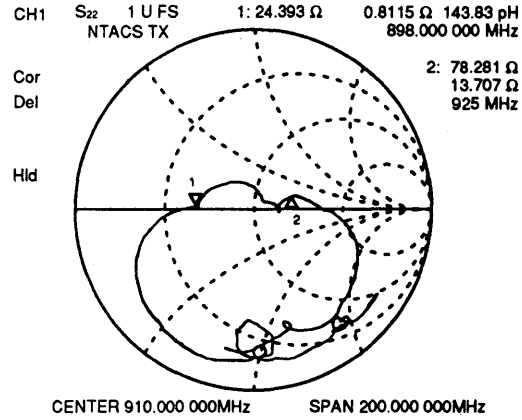


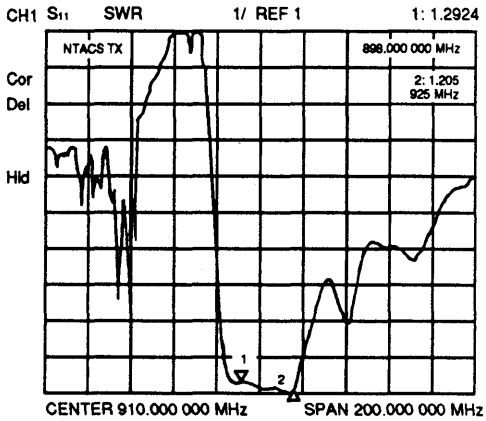


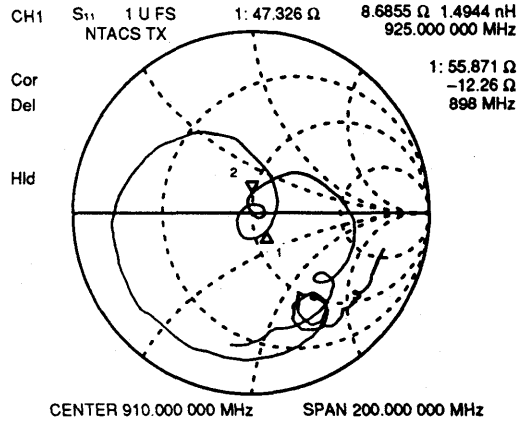
7

10. NTACS type (Tx)
Part number: F5CB-911M50-G201

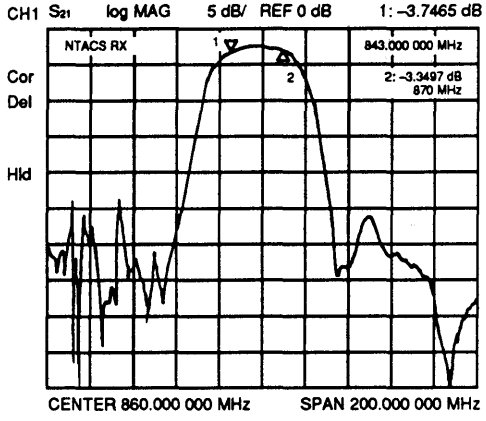


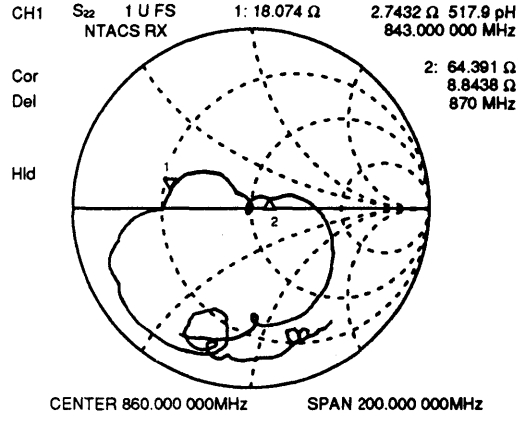


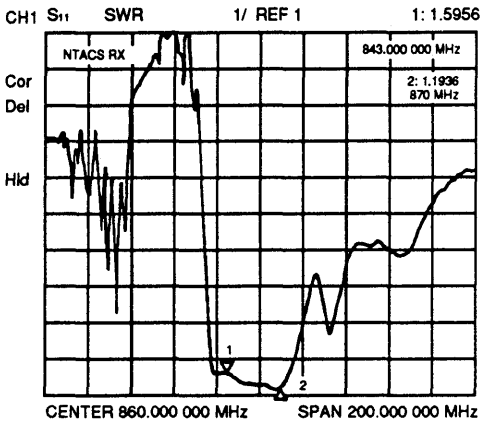


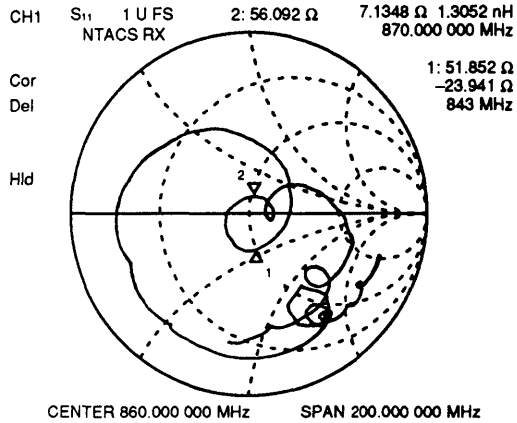


11. NTACS type (Rx)
Part number: F5CB-856M50-G201



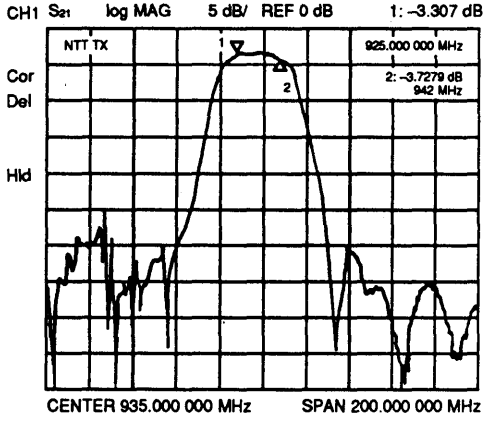


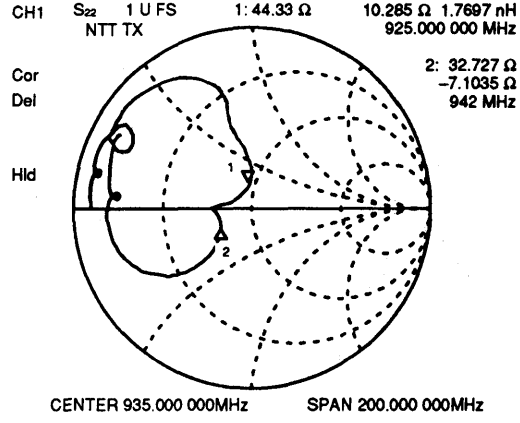


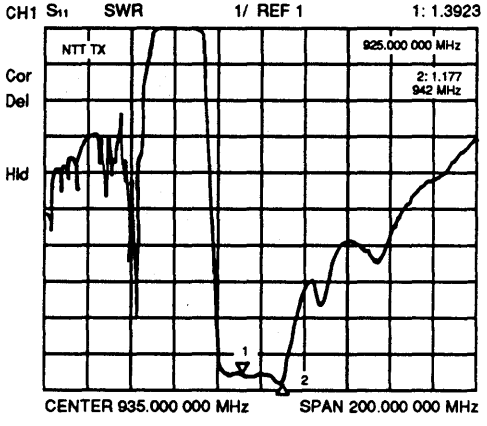


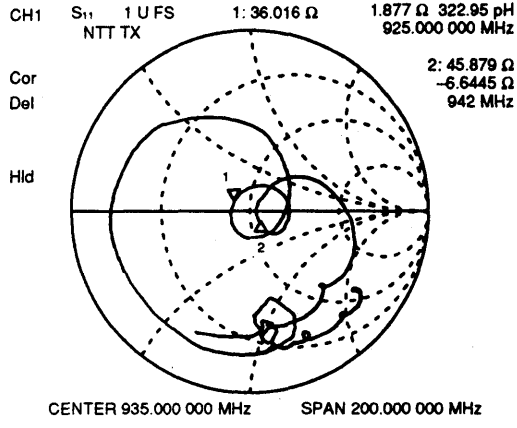
7

12. NTT type (Tx)
Part number: F5CB-933M50-G201

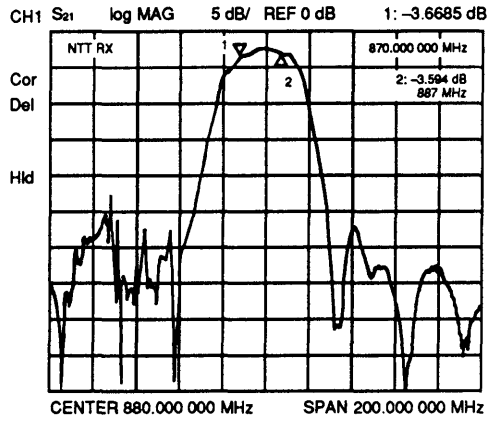


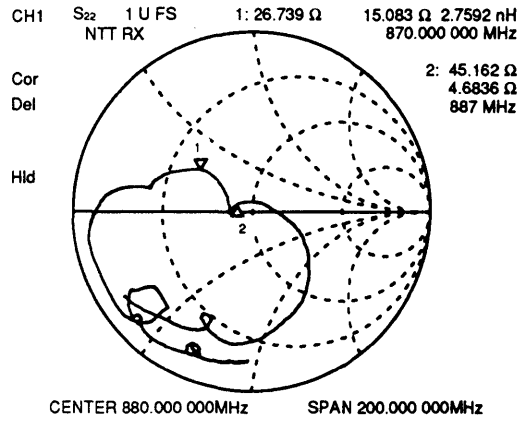


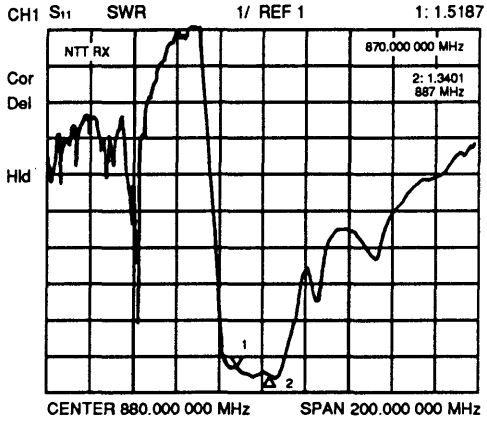


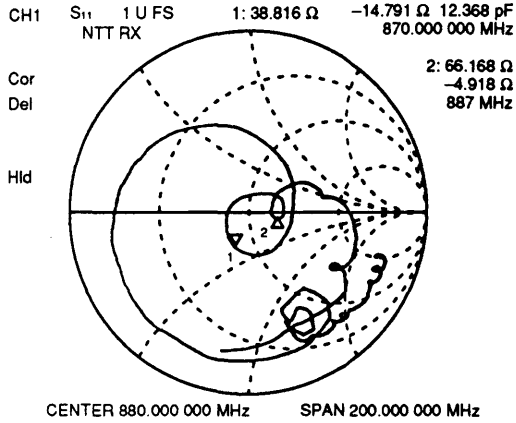


13. NTT type (Rx)
Part number: F5CB-878M50-G201









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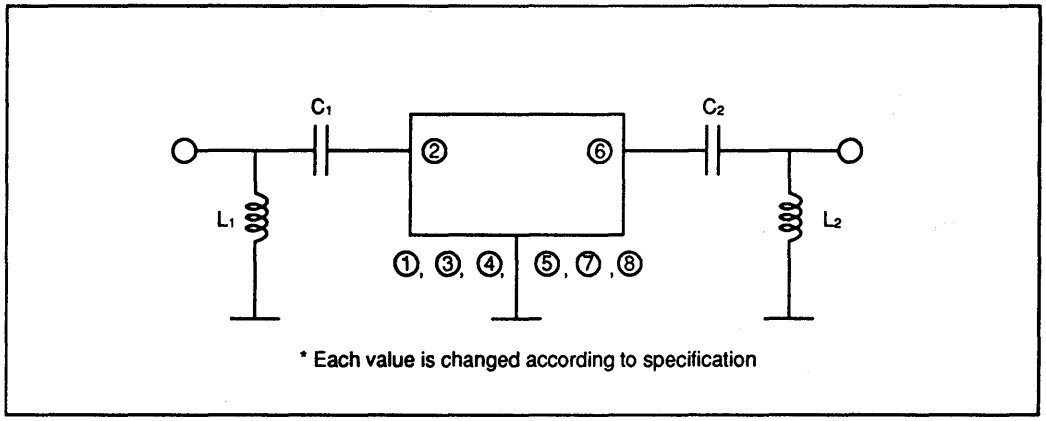
TEST CIRCUIT



* Each value is changed according to specification

PART NUMBER DESIGNATION

Designation example

F5CB-□□□□□□-G□□□-□
① ② ③

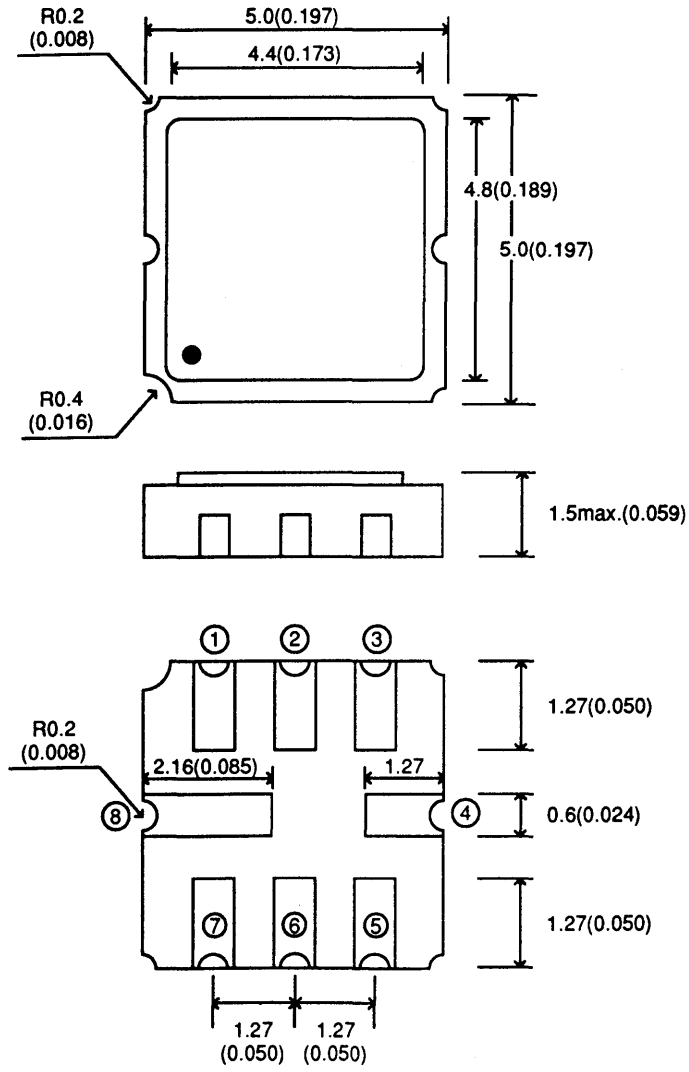
① Frequency designation : Specify the nominal frequency in six alphanumeric characters. Enter M (for MHz) at the decimal point. Refer to "PART NUMBERS".
Example: For an 836.5MHz device, designate as 836M50.

② Serial number : Specify a number from 201 to 299

③ Packaging (Reeled tape) :

Designation	Contents
T	1Kpcs/reel
R	3Kpcs/reel

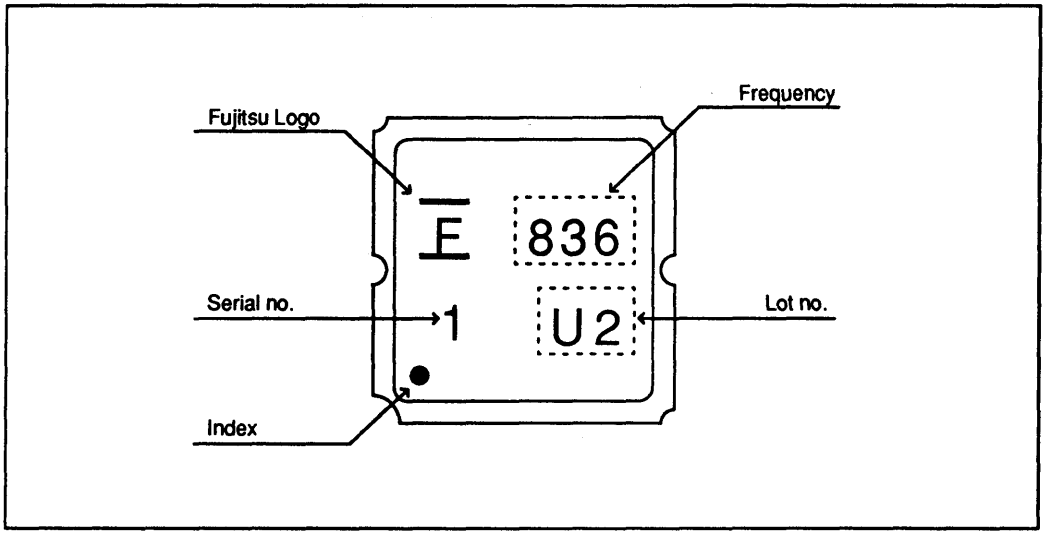
DIMENSIONS



Unit: mm(in.)

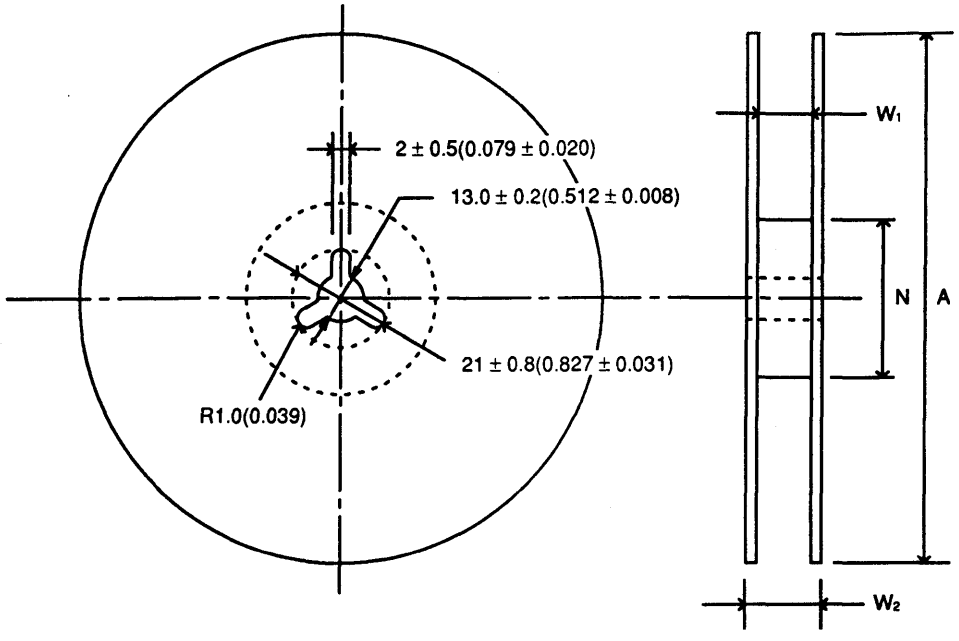
7

MARKING



PACKAGING: Reel type

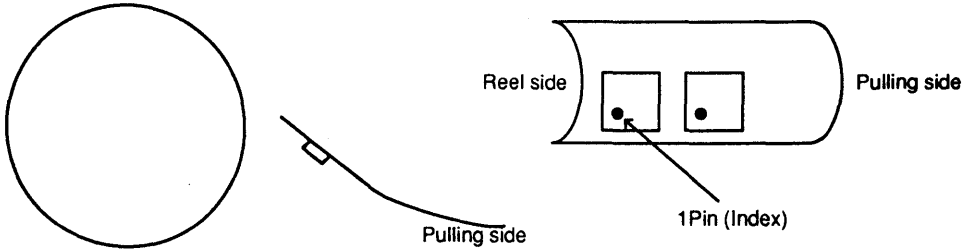
1. Reel dimension



Designation	A	N	W_1	W_2
–T	250 (9.843)	80 (3.150)	$12.4^{+2.0}_{0.0}$ ($0.488^{+0.079}_{0.0}$)	18.4 or less(0.724)
–R	330 (12.972)	80 (3.150)	$12.4^{+2.0}_{0.0}$ ($0.488^{+0.079}_{0.0}$)	18.4 or less(0.724)

Unit: mm(in.)

2. Package style



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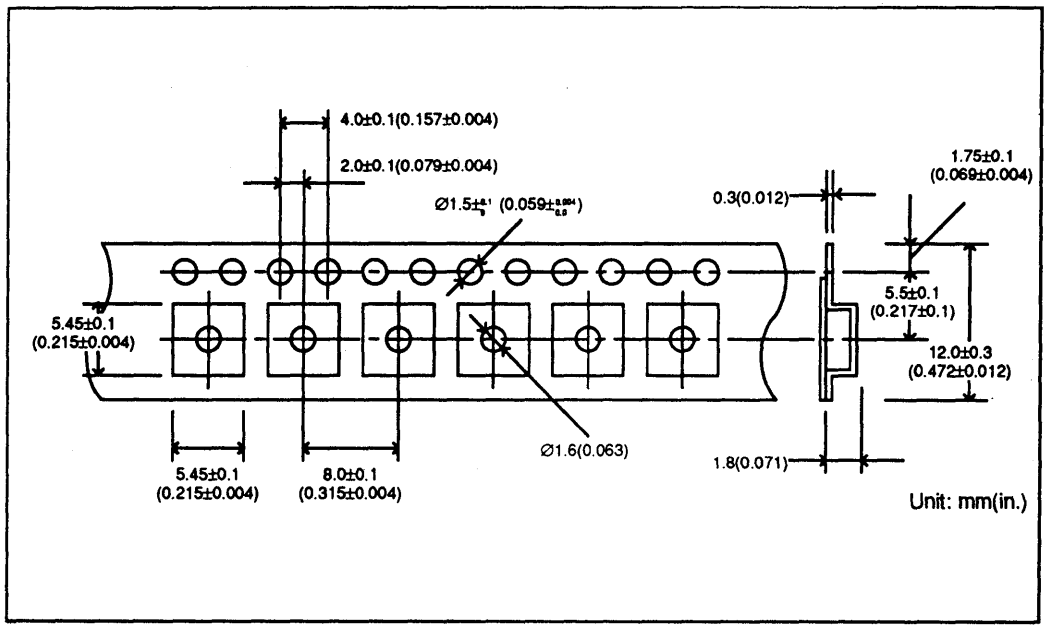
3. Tape dimension



DS04-23109-1E

FUJITSU

DATA SHEET

F6 SERIES (L2 Type) ASSP

PIEZOELECTRIC SAW BPF

DESCRIPTION

The F6 series are wideband bandpass filters for use in the1000 MHz to 2500 MHz range.
The F6 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) that has large electromechanical coupling coefficient. This provides wide bandwidths and exceptional stability.
Our exclusive mounting technology makes the F6 series very compact and surface mountable.
Insertion loss is much lower than other filters and impedance is realized at 50 Ω in passband.
L2 type can be handled without outside matching circuit.
The F6 series is most suitable for use in handheld phones for digital systems.

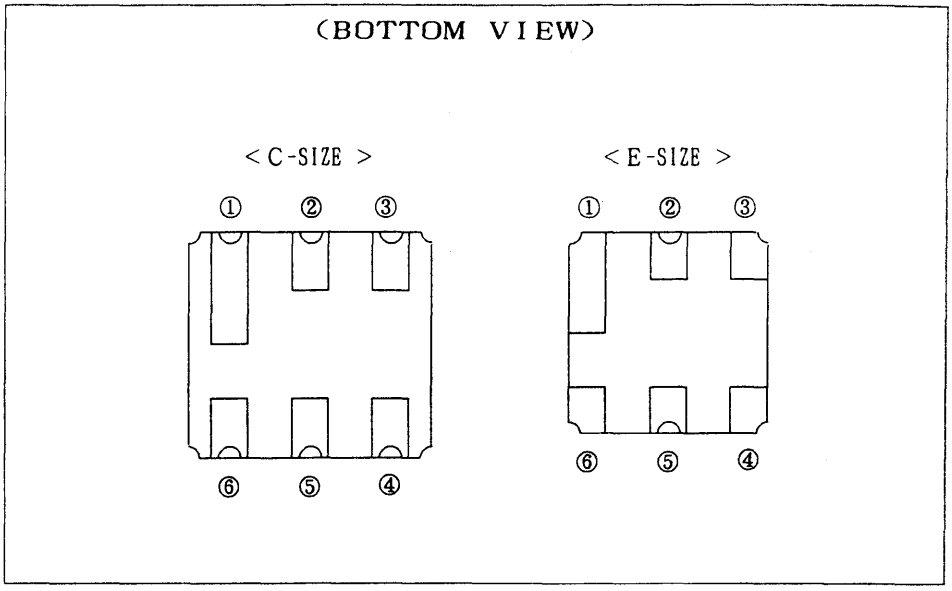
FEATURES

- Ultra compact and light (0.02 cc, 0.1 g)
- Outside matching circuit is unnecessary.
- Surface mount package (SMT)
- Low insertion loss
- High power rating : 0.2 W guaranteed for F6CC Series
  0.1 W guaranteed for F6CE Series

7

PACKAGE

PIN ASSIGNMENT



DESCRIPTION

Pin No.	Pin name	Description
1	GND	Ground Pin
2	IN	Input Pin
3	GND	Ground Pin
4	GND	Ground Pin
5	OUT	Output Pin
6	GND	Ground Pin

MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	T_a	−30～85	℃
Storage temperature	T_{stg}	−40～100	℃
Frequecy range		1000～2500	MHz
Maximum input level	P_{IN}	Refer to electrical characteristics	mW

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Operating temperature	T_a	−30～85*	℃

*Standard Rating for Wireless LAN is 0 ～ 60 ℃

STANDARD FREQUENCIES

Center freq. (MHz)	BW (MHz)	System	Part Symbol	Part number	Package Size
1441.0	24	PDC1.5G (Tx)	ZA	FAR-F6CC-1G4410-L2ZA	C
1489.0	24	PDC1.5G (Rx)	ZB	FAR-F6CC-1G4890-L2ZB	C
1619.0	24	PDC1.5G (Lo)	ZN	FAR-F6CC-1G6190-L2ZN	C
1747.5	75	DCS1800 (Tx)	A	FAR-F6CE-1G7475-L2YA	E
1842.5	75	DCS1800 (Rx)	B	FAR-F6CE-1G8425-L2YB	E
1880.0	60	PCS (Tx)	C	FAR-F6CE-1G8800-L2XA	E
1960.0	60	PCS (Rx)	D	FAR-F6CE-1G9600-L2XB	E
2450.0	100	Wireless LAN	E	FAR-F6CE-2G4500-L2WA	E

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

1. PDC1.5G system (Tx)
Part number : FAR-F6CC-1G4410-L2ZA T_a =−30～85℃

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1429 ～1453 MHz	—	2.5	3.5	dB	
In-band ripple		1429 ～1453 MHz	—	1.0	1.8	dB	
Absolute stopband attenuation		DC ～1200 MHz	20	26	—	dB	
		1200 ～1260 MHz	25	30	—	dB	
		1260 ～1287 MHz	30	34	—	dB	
		1287 ～1380 MHz	25	29	—	dB	
		1477 ～1513 MHz	10	14	—	dB	
		1513 ～1607 MHz	33	39	—	dB	
		1607 ～1631 MHz	35	39	—	dB	
		1631 ～1900 MHz	30	38	—	dB	
		1900 ～2906 MHz	18	20	—	dB	
In-band VSWR		1429 ～1453 MHz	—	1.3	2.0	—	
Max. input power	P_{IN}	1429 ～1453 MHz	—	—	200	mW	

7

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

2. PDC1.5G system (Rx)
Part number : FAR-F6CC-1G4890-L2ZB T_a = −30～85℃

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1477 ～1501 MHz	—	2.9	3.2	dB	
In-band ripple		1477 ～1501 MHz	—	1.2	1.7	dB	
Absolute stopband attenuation		DC ～ 130 MHz	30	38	—	dB	
		130 ～ 958 MHz	20	26	—	dB	
		958 ～1216 MHz	25	27	—	dB	
		1216 ～1241 MHz	30	32	—	dB	
		1241 ～1429 MHz	26	28	—	dB	
		1429 ～1453 MHz	10	17	—	dB	
		1542 ～1566 MHz	20	40	—	dB	
		1566 ～1607 MHz	30	40	—	dB	
		1607 ～1631 MHz	35	40	—	dB	
		1631 ～1737 MHz	30	40	—	dB	
		1737 ～1761 MHz	35	40	—	dB	
		1761 ～1900 MHz	30	37	—	dB	
		1900 ～3000 MHz	15	20	—	dB	
In-band VSWR		1477 ～1501 MHz	—	1.4	2.0	—	
Max. input power	P_{IN}	1477 ～1501 MHz	—	—	200	mW	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

3. PDC1.5G system (Lo)
Part number : FAR-F6CC-1G6190-L2ZN T_a =−30～85℃

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1607 ～1631 MHz	—	3.0	4.0	dB	
In-band deviation		1607 ～1631 MHz	—	1.5	2.0	dB	
Absolute stopband attenuation		DC ～ 130 MHz	30	38	—	dB	
		130 ～1501 MHz	25	28	—	dB	
		1737 ～1809 MHz	30	35	—	dB	
		1809 ～2500 MHz	20	29	—	dB	
		3214 MHz	15	25	—	dB	
In-band VSWR		1607 ～1631 MHz	—	1.6	2.0	—	
Max. input power	P_{IN}	1607 ～1631 MHz	—	—	200	mW	

7

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

4. DCS1800 system (Tx) Preliminary
Part number : FAR-F6CE-1G7475-L2YA T_a =−30～85℃

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1710 ～1785 MHz	—	3.5	4.5	dB	
In-band ripple		1710 ～1785 MHz	—	2.0	3.0	dB	
Absolute stopband attenuation		DC ～1500 MHz	15	17	—	dB	
		1500 ～1670 MHz	20	22	—	dB	
		1805 ～1880 MHz	5	10	—	dB	
		1880 ～2200 MHz	22	24	—	dB	
		3420 ～3570 MHz	25	27	—	dB	
		5130 ～5355 MHz	10	20	—	dB	
In-band VSWR		1710 ～1785 MHz	—	2.0	3.0	—	
Max. input power	P_{IN}	1710 ～1785 MHz	—	—	100	mW	

5. DCS1800 system (Rx) Preliminary
Part number : FAR-F6CE-1G8425-L2YB T_a =−30～85℃

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1805 ～1880 MHz	—	3.9	4.8	dB	
In-band ripple		1805 ～1880 MHz	—	2.0	2.5	dB	
Absolute stopband attenuation		DC ～1500 MHz	21	23	—	dB	
		1600 ～1710 MHz	26	28	—	dB	
		1710 ～1785 MHz	8	24	—	dB	
		1920 ～2400 MHz	22	24	—	dB	
		3610 ～3760 MHz	22	25	—	dB	
In-band VSWR		1805 ～1880 MHz	—	2.0	3.0	—	
Max. input power	P_{IN}	1805 ～1880 MHz	—	—	100	mW	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

6. PCS system (Tx) Preliminary
Part number : FAR-F6CE-1G8800-L2XA T_a = −30 ~ 85°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1850 ~1910 MHz	—	3.5	4.5	dB	
In-band deviation		1850 ~1910 MHz	—	1.5	2.5	dB	
Absolute stopband attenuation		DC ~1500 MHz	22	24	—	dB	
		1500 ~1800 MHz	25	28	—	dB	
		1930 ~1990 MHz	5	8	—	dB	
		3700 ~3820 MHz	20	24	—	dB	
		5550 ~5730 MHz	4	5	—	dB	
In-band VSWR		1850 ~1910 MHz	—	1.8	2.5	—	
Max. input power	P_{IN}	1850 ~1910 MHz	—	—	100	mW	

7. PCS system (Rx) Preliminary
Part number : FAR-F6CE-1G9600-L2XB T_a = −30 ~ 85°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1930 ~1990 MHz	—	4.0	4.8	dB	
In-band deviation		1930 ~1990 MHz	—	2.0	2.8	dB	
Absolute stopband attenuation		DC ~1500 MHz	22	24	—	dB	
		1500 ~1850 MHz	25	28	—	dB	
		1850 ~1910 MHz	10	25	—	dB	
		3920 ~4040 MHz	20	23	—	dB	
In-band VSWR		1930 ~1990 MHz	—	1.8	2.5	—	
Max. input power	P_{IN}	1930 ~1990 MHz	—	—	100	mW	

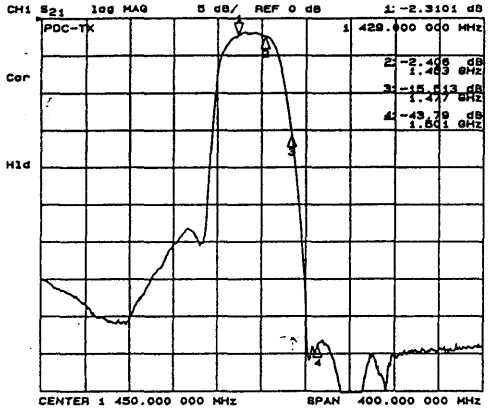
ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

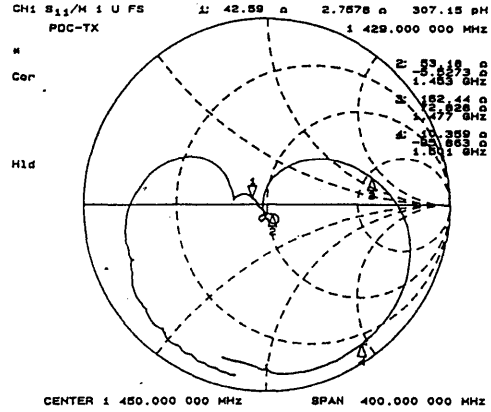
8. Wireless-LAN system Preliminary
Part number : FAR-F6CE-2G4500-L2WA $T_a = 0 \sim 60$℃

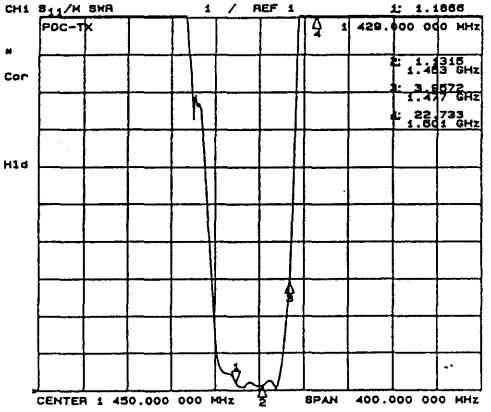
Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	2400 ~2500 MHz	—	4.5	5.5	dB	
In-band ripple		2400 ~2500 MHz	—	2.3	3.5	dB	
Absolute stopband attenuation		DC ~1700 MHz	20	25	—	dB	
		1800 ~2200 MHz	25	28	—	dB	
		2700 ~3100 MHz	30	34	—	dB	
		4800 ~5000 MHz	15	18	—	dB	
In-band VSWR		2400 ~2500 MHz	—	2.0	3.0	—	
Max. input power	P_{IN}	2400 ~2500 MHz	—	—		mW	

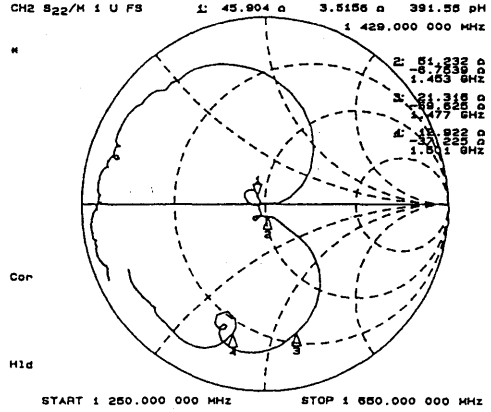
TYPICAL CHARACTERISTICS (STANDARD VERSION)

1. PDC1.5G system (Tx)
   Part number : FAR-F6CC-1G4410-L2ZA



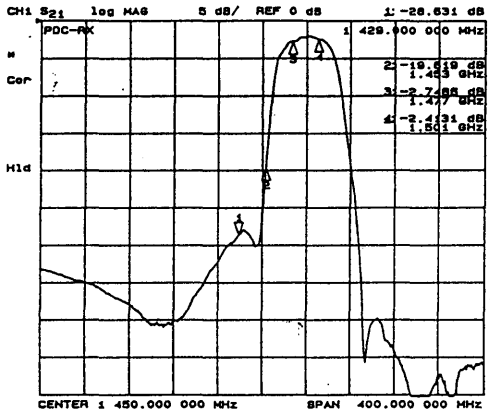


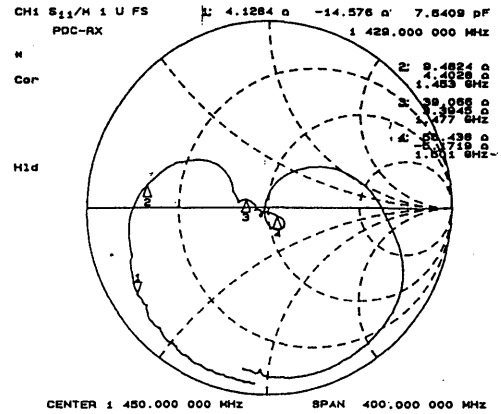


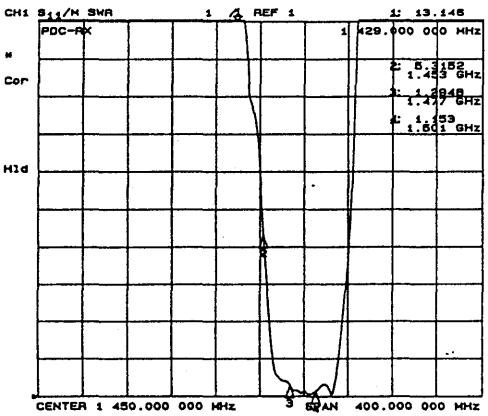


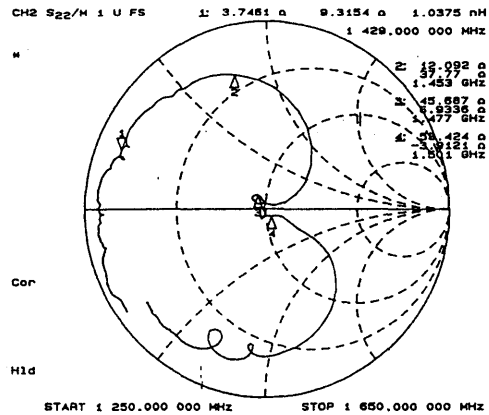
TYPICAL CHARACTERISTICS (STANDARD VERSION)

2. PDC1.5G system (Rx)
Part number : FAR-F6CC-1G4890-L2ZB



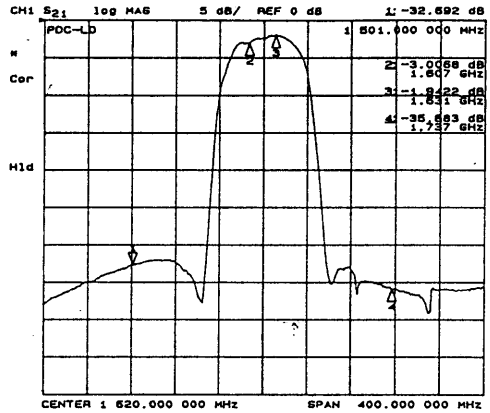


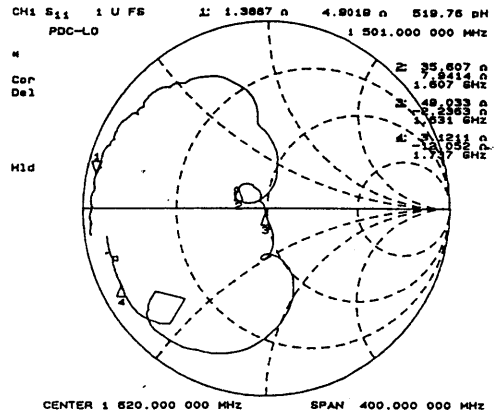


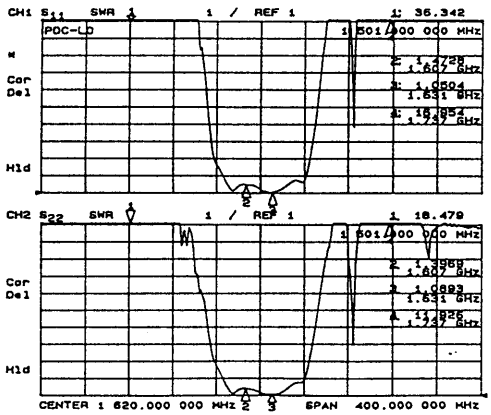


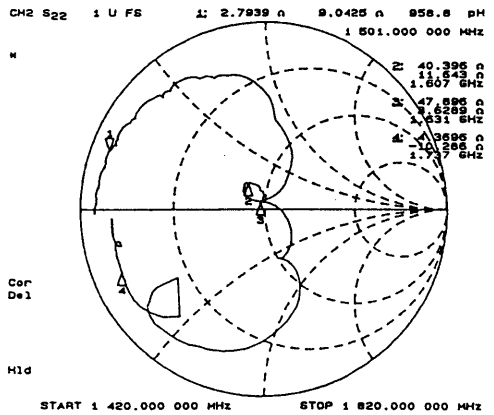
TYPICAL CHARACTERISTICS (STANDARD VERSION)

3. PDC1.5G system (Lo)
Part number : FAR-F6CC-1G6190-L2ZN



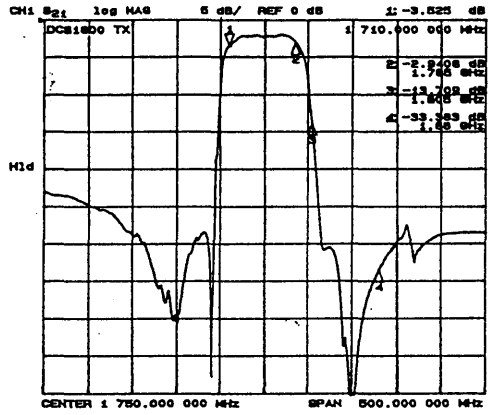


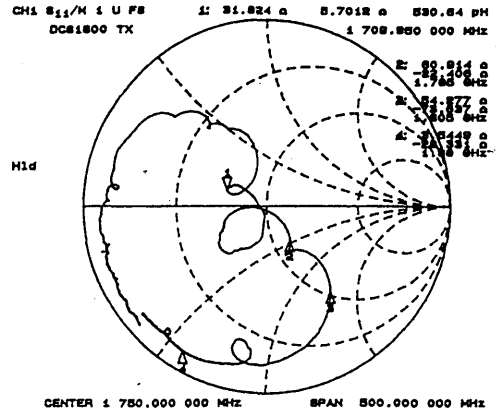


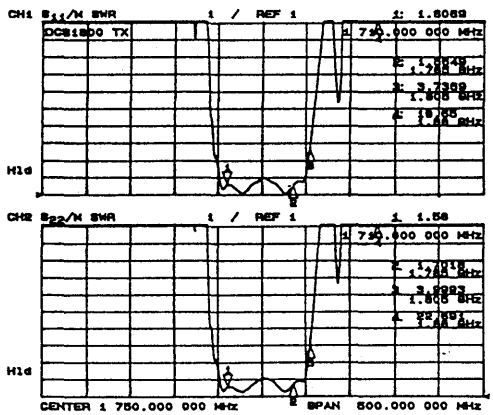


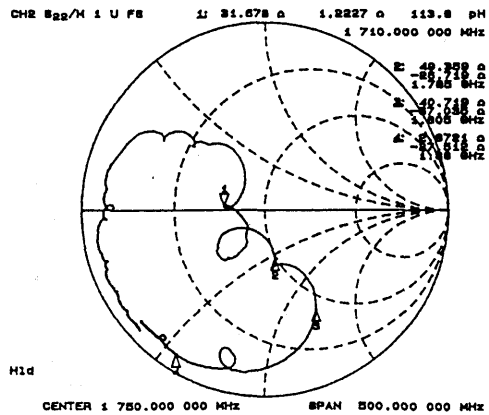
TYPICAL CHARACTERISTICS (STANDARD VERSION)

4. DCS1800 system (Tx) Preliminary
Part number : FAR-F6CE-1G7475-L2YA



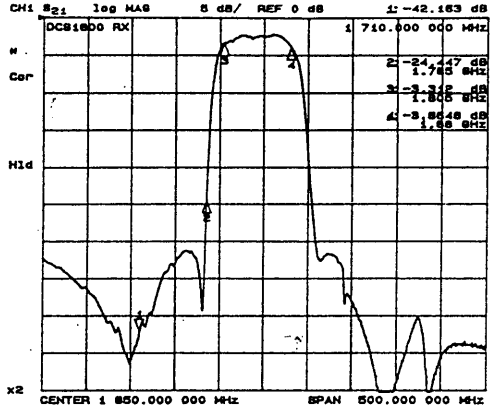


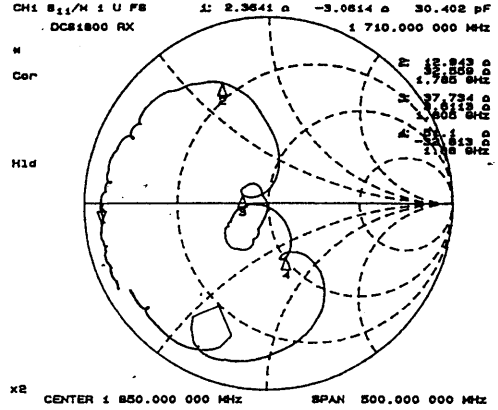


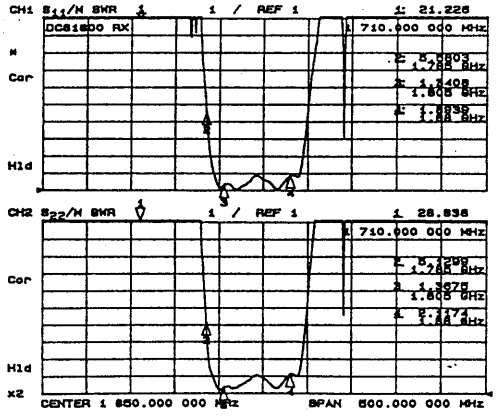


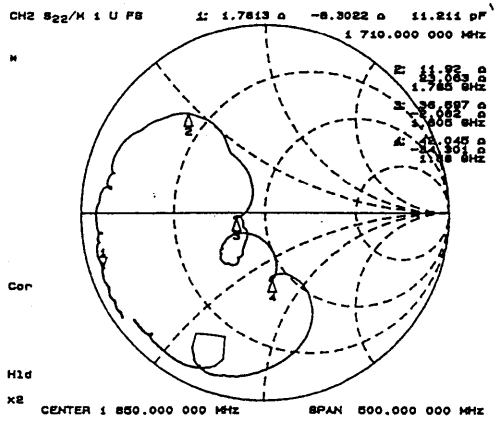
TYPICAL CHARACTERISTICS (STANDARD VERSION)

5. DCS1800 system (Rx) Preliminary
Part number : FAR-F6CE-1G8425-L2YB





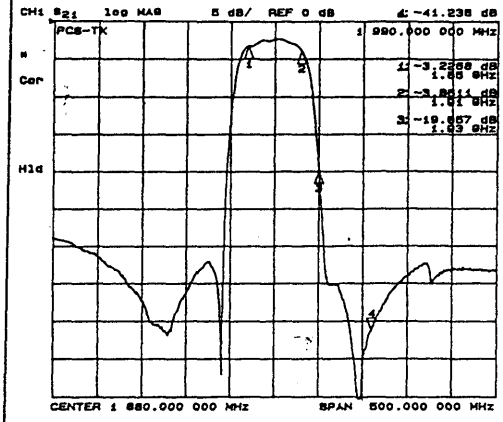


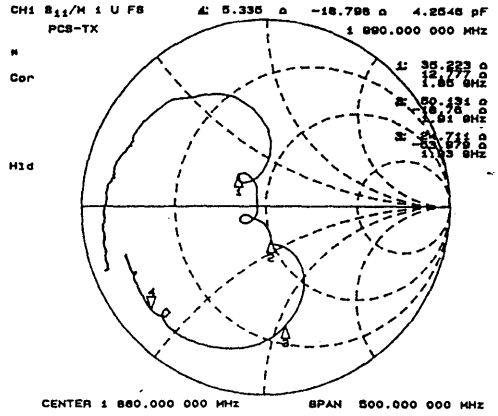


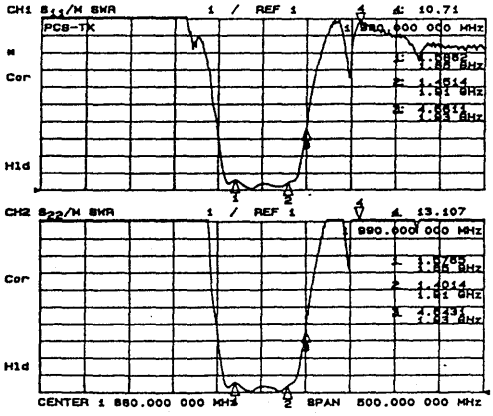
7

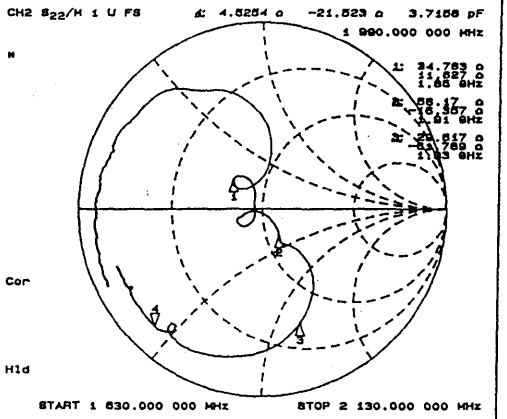
TYPICAL CHARACTERISTICS (STANDARD VERSION)

6. PCS system (Tx) Preliminary
Part number : FAR-F6CE-1G8800-L2XA









TYPICAL CHARACTERISTICS (STANDARD VERSION)

7. PCS system (Rx) Preliminary
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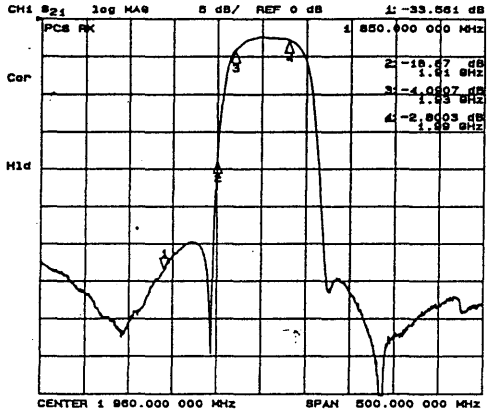
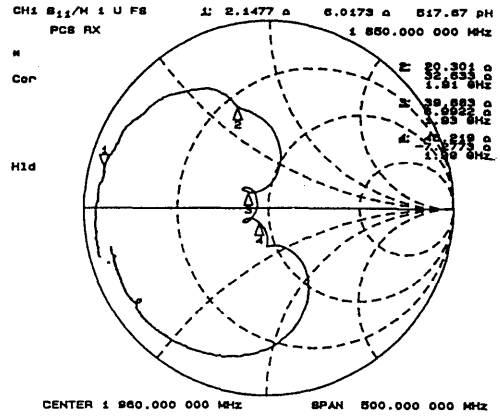
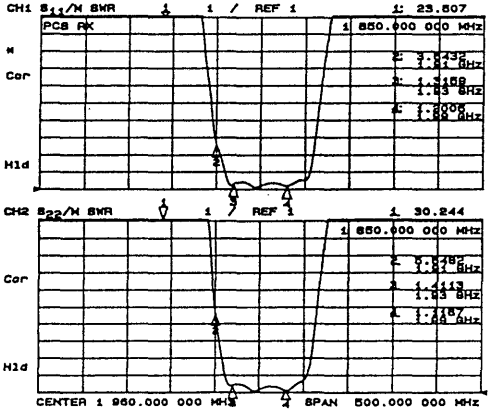
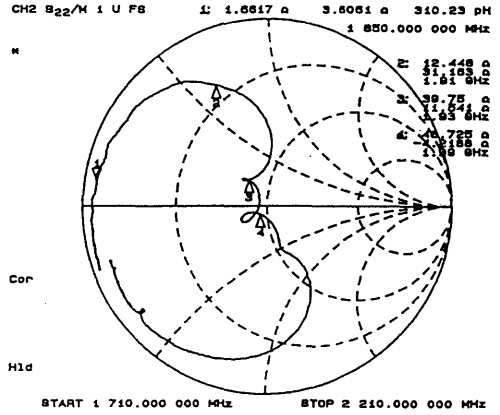


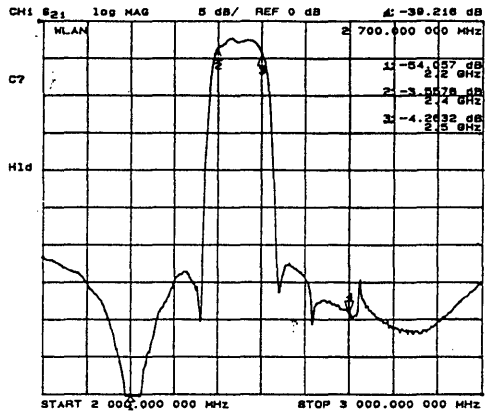


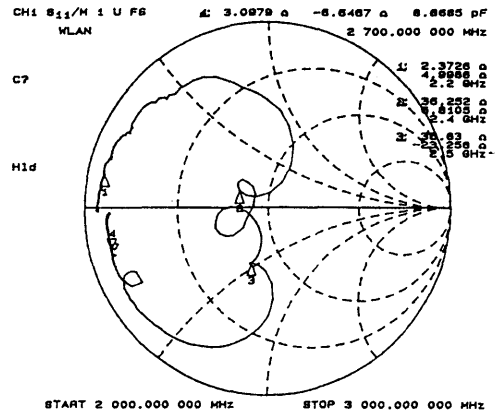


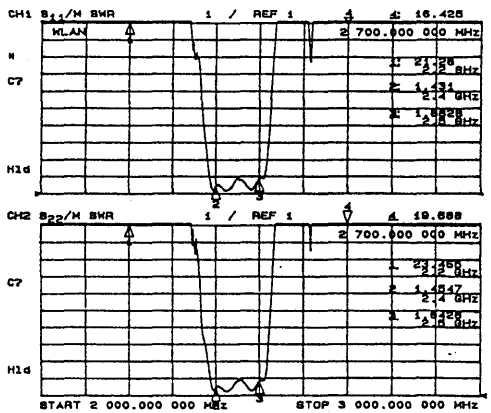


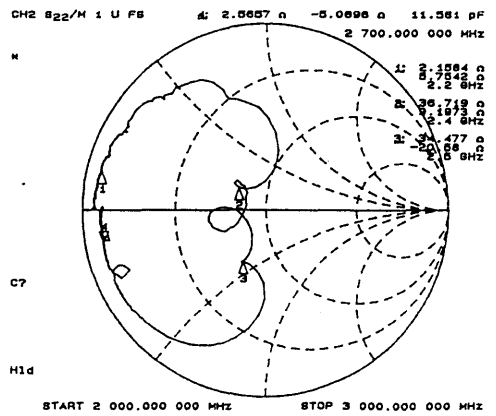
TYPICAL CHARACTERISTICS (STANDARD VERSION)

8. Wireless-LAN system Preliminary
Part number : FAR-F6CE-2G4500-L2WA

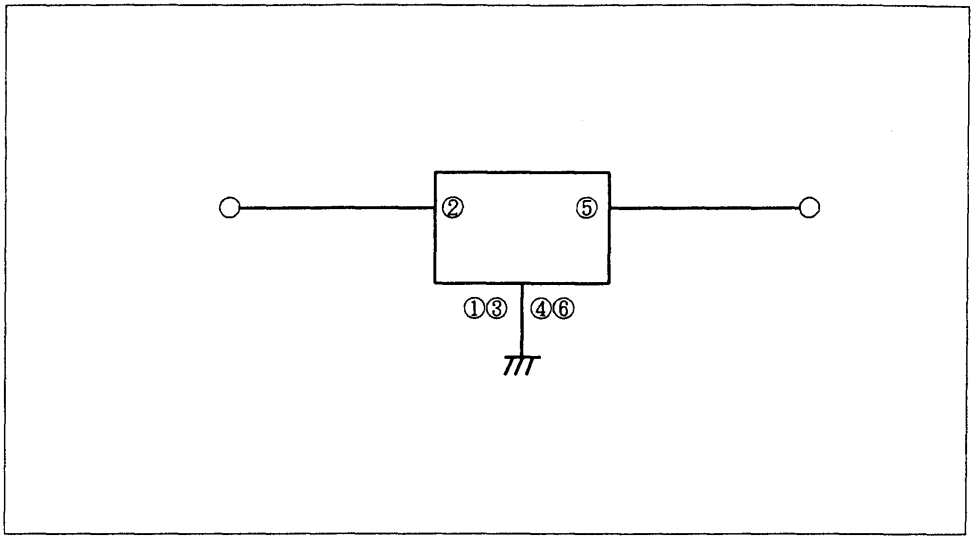








■MEASURING CIRCUIT



■PART NUMBER DESIGNATION

[Designation example]

FAR-F6C□-□□□□□□-L2□□-□

① ② ③ ④

①Package designation: C : 3.8 mm□ × 1.6 mm

E : 3.0 mm□ × 1.2 mm

Refer to "■ standard frequencies.

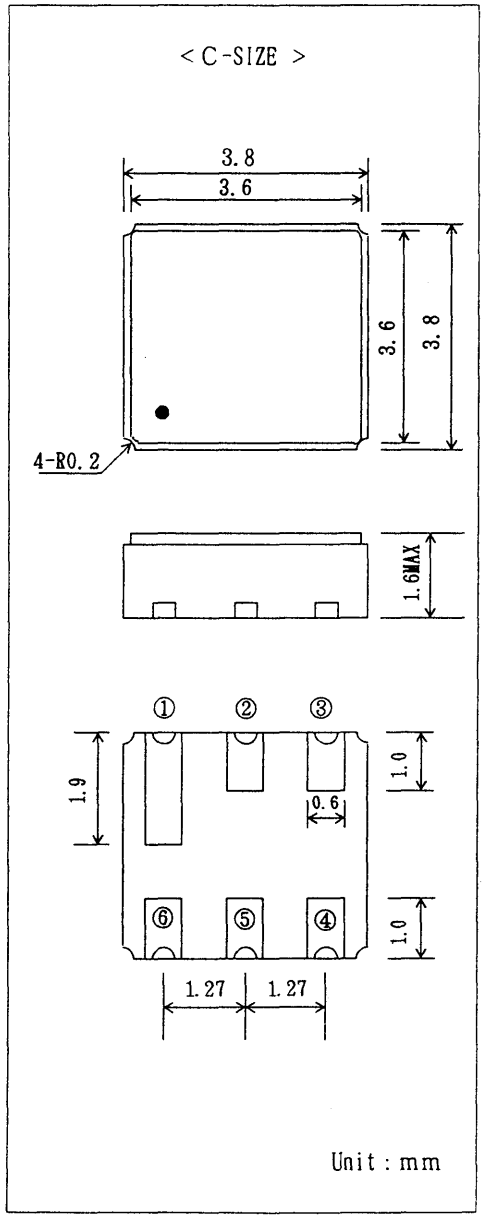
②Frequency designation: Specify the nominal frequency in six alphanumeric characters. Enter G(for GHz) at the decimal point. Refer to standard friquencies.

[Example] 1.4410GHz ⇨ 1G4410

③Serial number: Specify a number from WA to ZZ. Refer to standard friquencies.

④Packing: (Reeled tape)
T : 1K pcs/reel
R : 3K pcs/reel

DIMENSIONS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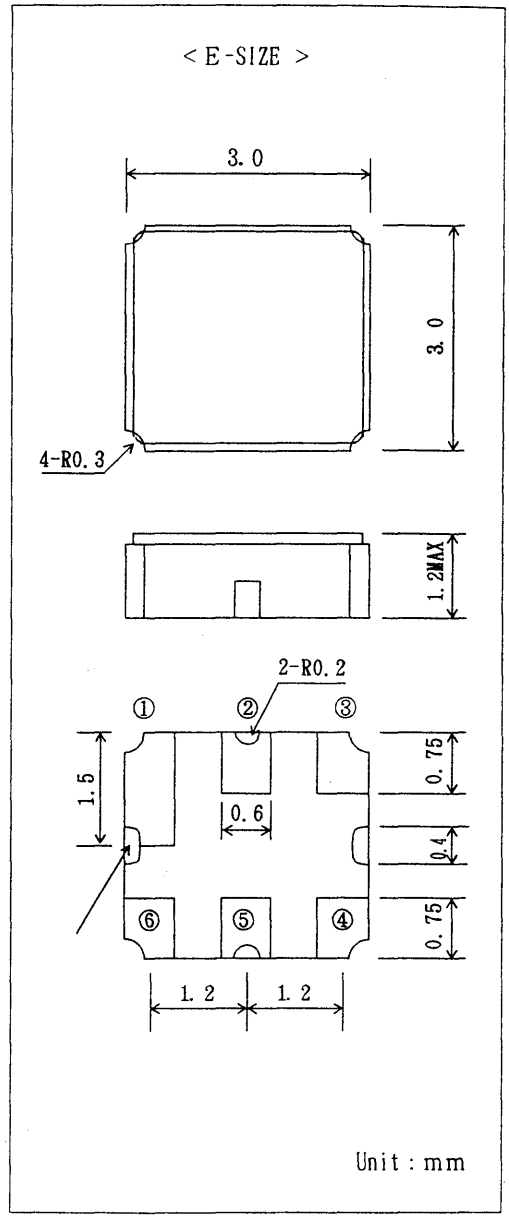
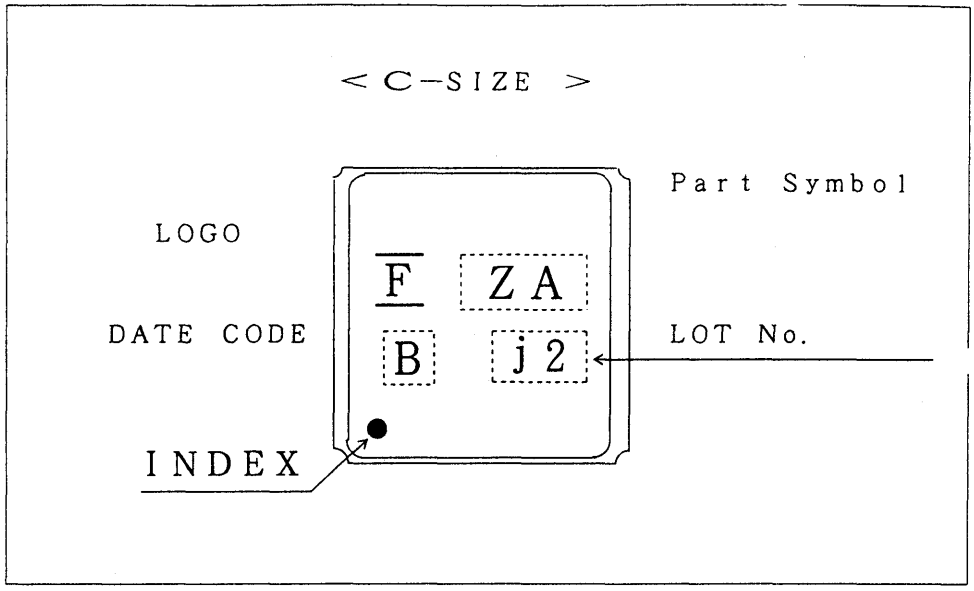
3.6
3.6
3.8
4-R0.2
1.6MAX
①
②
③
1.9
1.0
0.6
⑥
⑤
④
1.0
1.27
1.27
Unit : mm


< E-SIZE >
3.0
3.0
4-R0.3
1.2MAX
2-R0.2
①
②
③
1.5
0.6
0.75
0.4
0.75
⑥
⑤
④
1.2
1.2
Unit : mm

MARKING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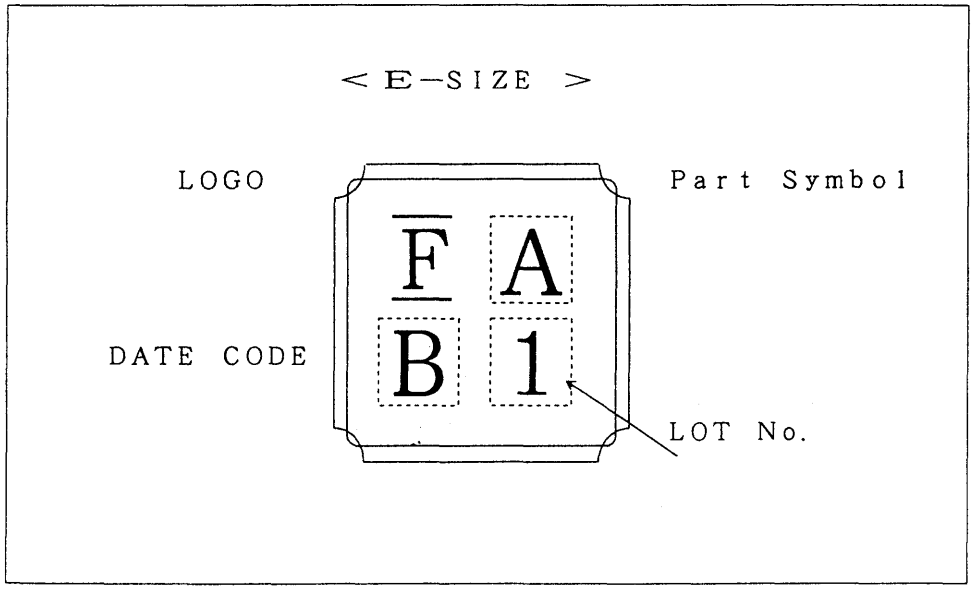
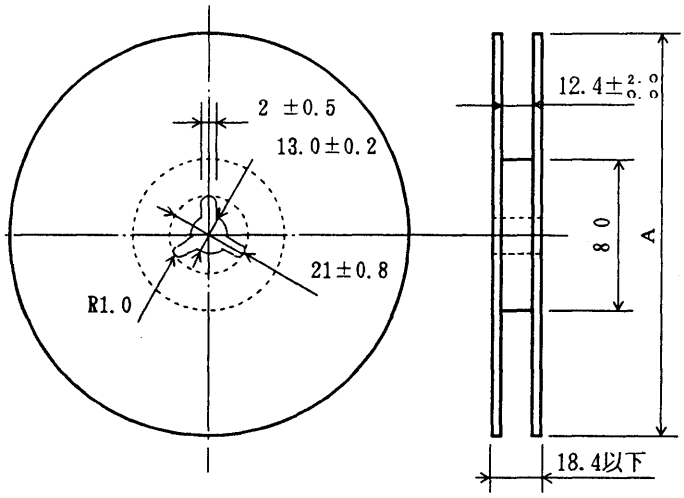
LOGO
DATE CODE
INDEX
F
ZA
B
j2
Part Symbol
LOT No.


< E-SIZE >
LOGO
DATE CODE
F
A
B
1
Part Symbol
LOT No.

PACKING: Reel type

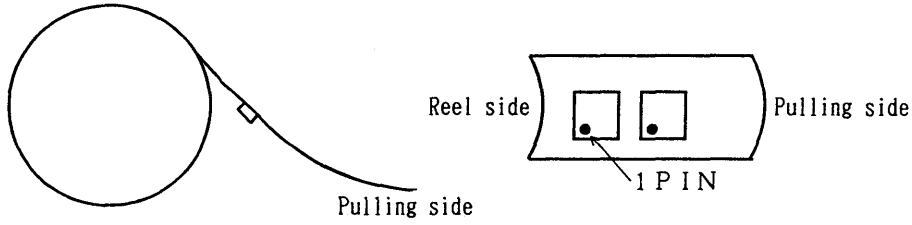
(1)Reel dimension



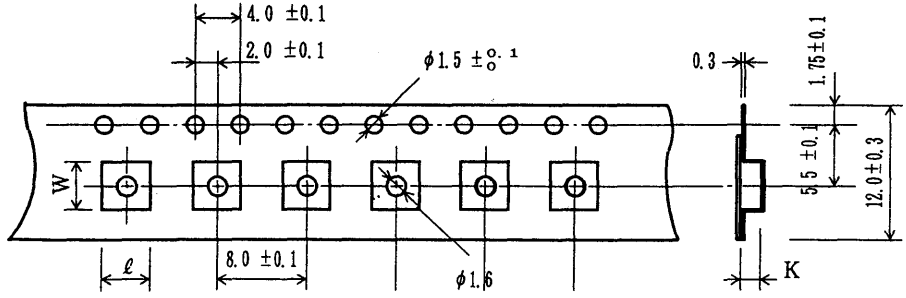
Type	A	Volume
−T	250	1Kpcs
−R	330	3Kpcs

単位：mm

(2)Packing style



(3)Tape dimension



Package	ℓ	W	K
C	4.2±0.1	4.2±0.1	1.8
E	3.4±0.1	3.4±0.1	1.5

Unit:mm

October 1990
Edition 1.0

FUJITSU

DATA SHEET

M2 Series (D100)

PIEZOELECTRIC DEVICE VOLTAGE CONTROLLED OSCILLATOR

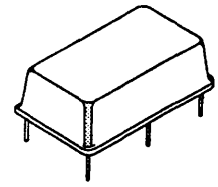
DESCRIPTION

The M2 series (D100) voltage controlled oscillators (VCO) operate in the frequency range of 4 to 30 MHz.

The M2 series VCOs use a single $LiTaO_3$ (lithium tantalate) piezoelectric crystal with a high electromechanical coupling coefficient for stable and wide variable frequency width.

FEATURES

- Wider variable frequency width than quartz crystals: ± 0.2% or more
- High stability (100 times more stable than LC configuration)
- Excellent carrier noise ratio
- Hermetically sealed in a metal case for high reliability in severe environmental conditions
- Compatible with 14-pin DIP IC packages



Metal Case
DIP-14

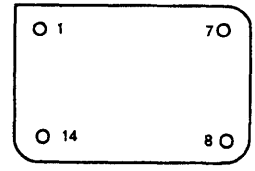
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	-0.5 to 7.0	V
Input Control Voltage	V_{IN}	-0.5 to 10	V
Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	± 25	mA
Operating Temperature	T_a	-30 to +85	°C
Storage Temperature	T_{STG}	-40 to +100	°C
Oscillation Frequency Range		4 to 30	MHz

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	V
Input Control Voltage	V_{IN}	0.5 to 5.0	V
Operating Temperature	T_a	-30 to +85	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Bottom View

Terminal No.	Terminal Name	Description
1	V_{IN1}	Control Voltage Input Terminal
7	GND	Grounding Terminal
8	V_{OUT}	Oscillation Output Terminal
14	V_{CC}	Power Supply Terminal

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

STANDARD FREQUENCIES

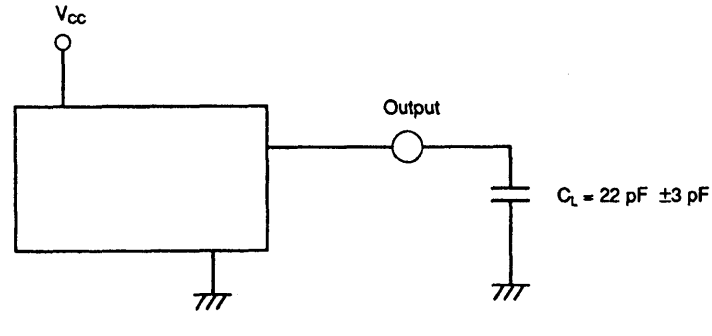
8.192 MHz	14.318 MHz	17.734 MHz	21.053 MHz	25.175MHz
9.408 MHz	16.000 MHz	18.432 MHz	21.477 MHz	27.338 MHz
11.290 MHz	16.257 MHz	18.816 MHz	22.579 MHz	28.224 MHz
11.580 MHz	16.384 MHz	20.480 MHz	24.576 MHz	28.636 MHz
12.288 MHz	I6.934 MHz			

ELECTRICAL CHARACTERISTICS

DC Characteristics

Item	Symbol	Condition	Ratings		Unit
			Minimum	Maximum	
Output Level	V_{OUT}	See the measuring circuit diagram	0.5	—	V_{P-P}
Power Supply Current	I_{CC}	Load open	—	15	mA

Measuring Circuit Diagram



(CL is the value including the measurement probe and the jig capacitance.)

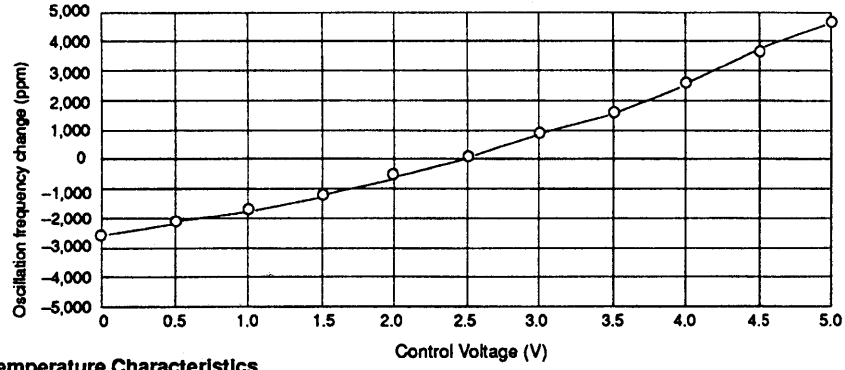
AC Characteristics

Item	Symbol	Condition	Ratings		Unit	Remarks
			Minimum	Maximum		
Oscillation Frequency	f_{OSC}	V_{IN} = 2.5 V	-0.05	+0.05	%	Nominal Frequency reference V_{CC} = 5 V, T_a = 25°C
	f_H	V_{IN} = 4.5 V	+0.15	—	%	
	f_L	V_{IN} = 0.5 V	—	-0.15	%	
Frequency Voltage Stability	$\Delta f, V_{CC}$	V_{CC} = 4.75 V V_{CC} = 5.25 V	-200	200	ppm	5 V reference, V_{IN} = 2.5 V
Frequency Temperature Stability	$\Delta f, T_a$	V_{IN} = 0.5 V V_{IN} = 4.5 V	-500	500	ppm	25°C reference -10° to 70°C, T_A = 25°C

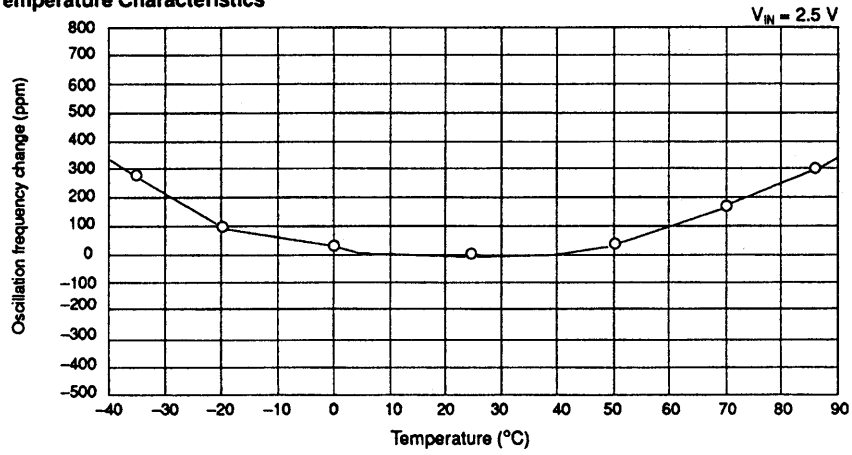
STANDARD CHARACTERISTICS:

Part Number: M2DA-8M1920-D100

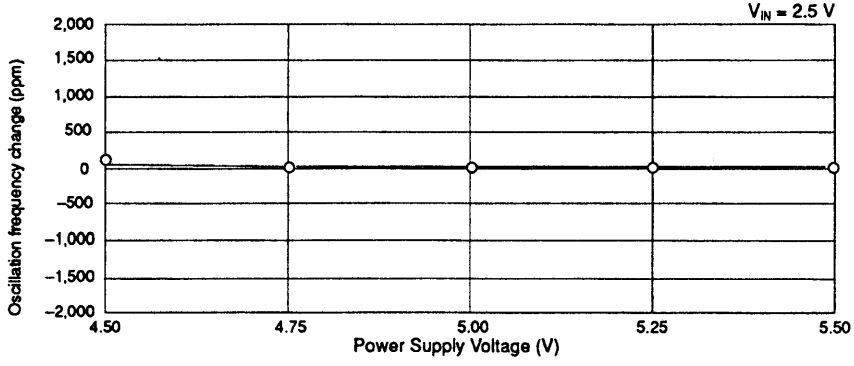
Control Voltage and Oscillation Frequency



Temperature Characteristics



Power Supply Voltage Characteristics

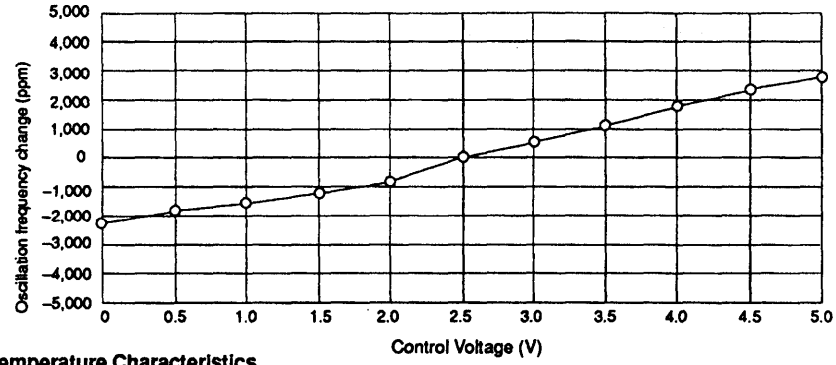


7

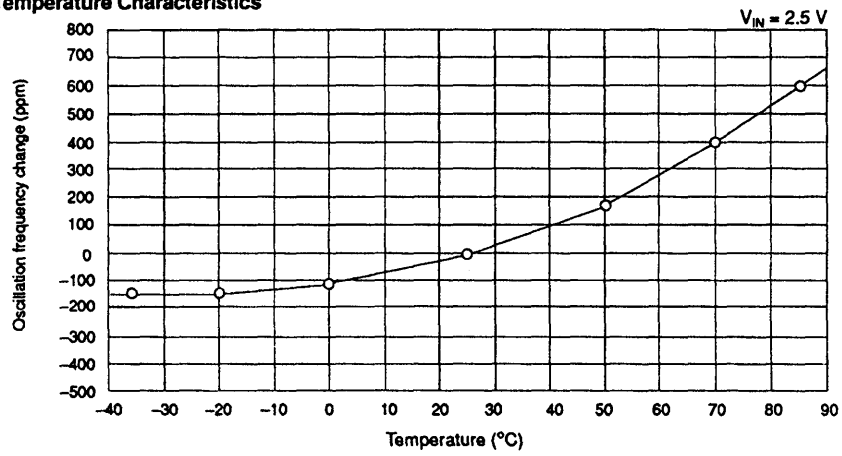
STANDARD CHARACTERISTICS:

Part Number: M2DA-28M636-D100

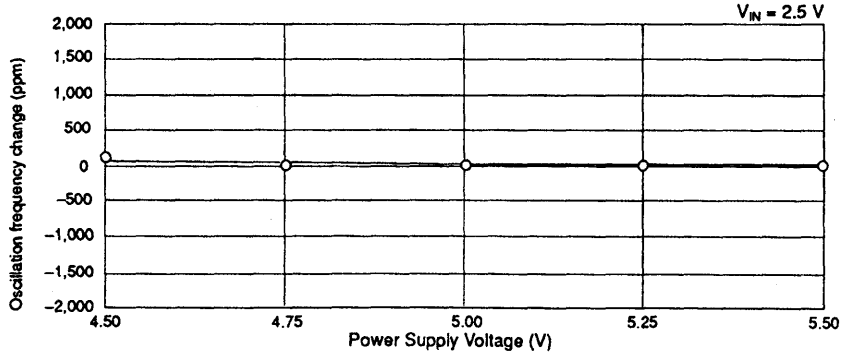
Control Voltage and Oscillation Frequency



Temperature Characteristics



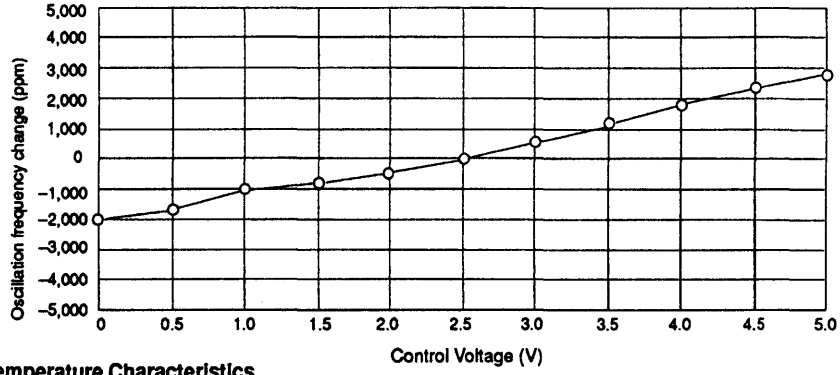
Power Supply Voltage Characteristics



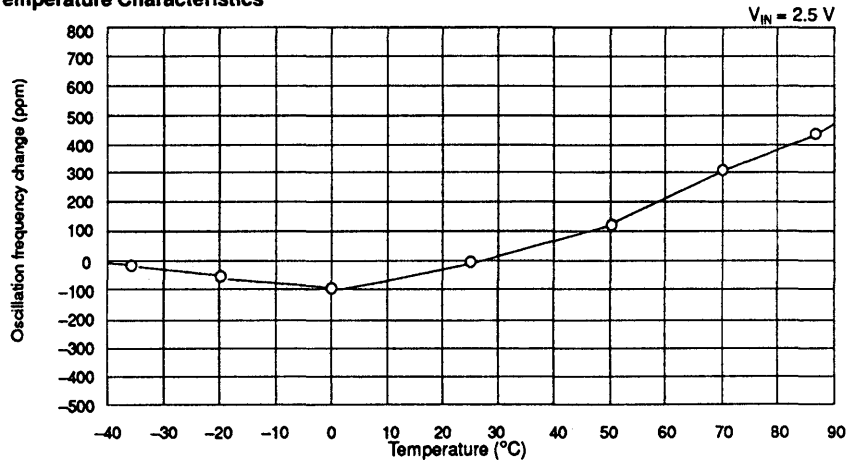
STANDARD CHARACTERISTICS:

Part Number: M2DA-12M288-D100

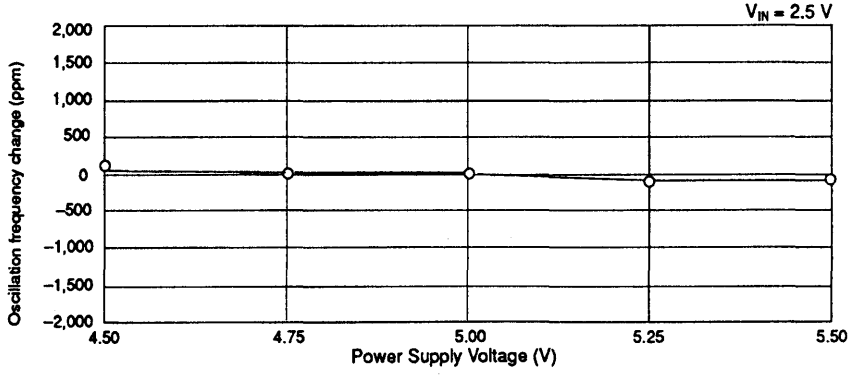
Control Voltage and Oscillation Frequency



Temperature Characteristics

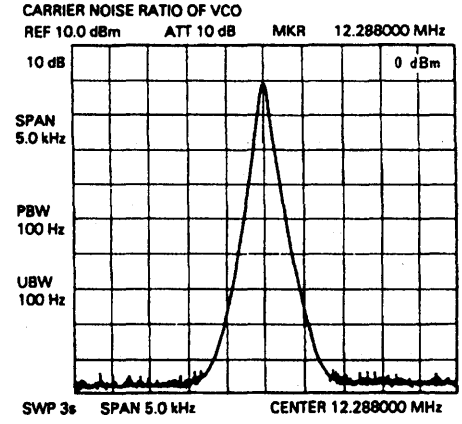


Power Supply Voltage Characteristics



7

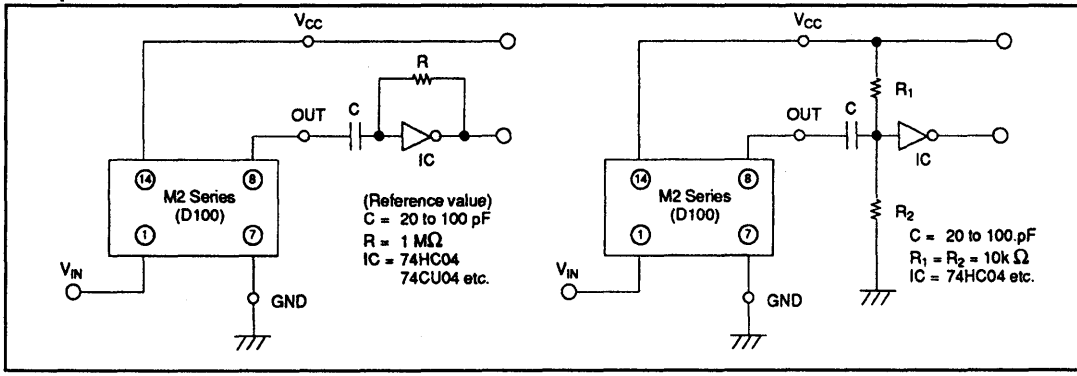
Oscillation Spectrum



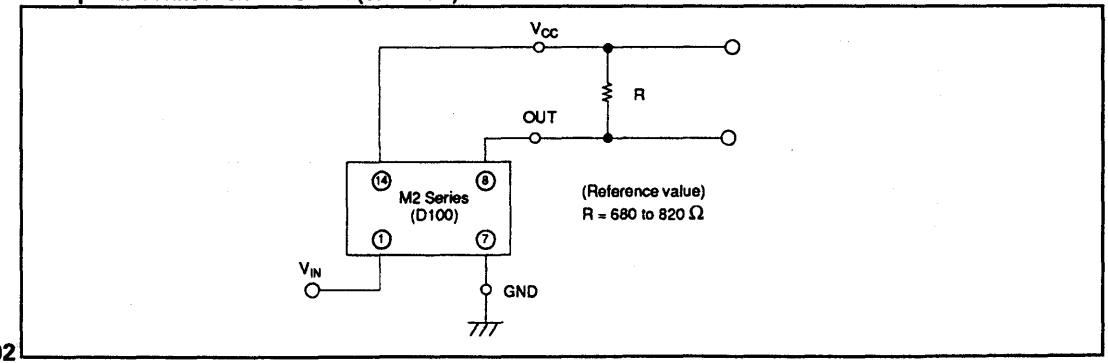
Output signal purity (C/N ratio)

APPLICATION CIRCUIT EXAMPLES

Example 1. Connection to CMOS



Example 2. Connection to LS TTL (or CMOS)



PART NUMBERING SYSTEM

Part Number Example

M2DA - □□□□□□ - D □□□

❶ ❷

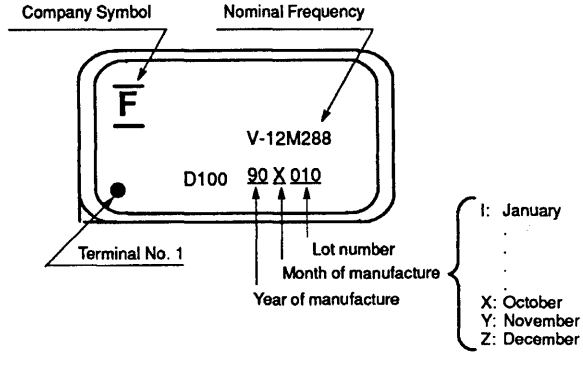
❶ Frequency Designation:Designate the nominal frequency in six alphanumeric characters.
M indicates the decimal point in MHz.

Frequency	Designation
8.192 MHz	8M1920
9.408 MHz	9M4080
11.290 MHz	11M290
11.580MHz	11M580
12.288 MHz	12M288
14.318 MHz	14M318
16.000 MHz	16M000
16.257 MHz	16M257
16.384 MHz	16M384
16.934 MHz	16M934
17.734 MHz	17M734

Frequency	Designation
18.432 MHz	18M432
18.816 MHz	18M816
20.480 MHz	20M480
21.053 MHz	21M053
21.477 MHz	21M477
22.579 MHz	22M579
24.576 MHz	24M576
25.175 MHz	25M175
27.338 MHz	27M338
28.224 MHz	28M224
28.636 MHz	28M636

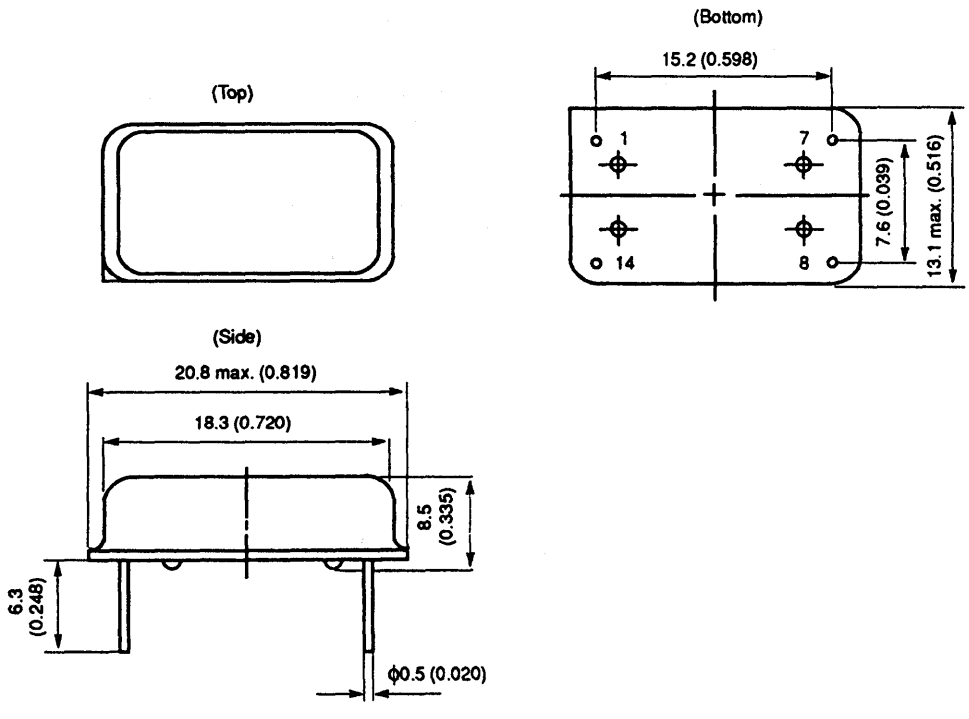
❷ Serial Number (of the Series):Standard: 100
Non-Standard porducts: 001 to 099

MARKING



7

DIMENSIONS



Units: mm (in.)

October 1990
Edition 1.0

FUJITSU

DATA SHEET

M2 Series (D300)
Piezoelectric Device (Voltage Controlled Oscillator)

DESCRIPTION

The M2 series (D300) voltage controlled oscillators (VCO) operate in the frequency range of 4 to 30 MHz. The M2 series VCOs use a single $LiTaO_3$ (lithium tantalate) piezoelectric crystal with a high electromechanical coupling coefficient for stable and wide variable frequency width.

This module incorporates three VCOs for the three sampling frequencies used in digital audio equipment (32, 44.1, and 48 kHz). The frequencies are selected by external signals.

FEATURES

- Clock replay in response to three sampling frequencies (32, 44.1 and 48 kHz), is contained in one module
- Wider variable frequency width than in quartz crystals: ±0.1% or more
- Excellent stability for signal noise reproduced by high quality of the lithium tantalate
- 100 times more stable than VCOs of LC and TTL-IC configuration
- Three sampling frequencies controlled at CMOS logic level
- SIP packaged for high-density mounting of devices
- Compatible with the Electronic Industry Association of Japan (EIAJ) digital I/O Standard Type II (consumer digital audio equipment), Level I (high-resolution mode) and Level II (standard resolution mode)

ABSOLUTE MAXIMUM RATINGS (See Note)

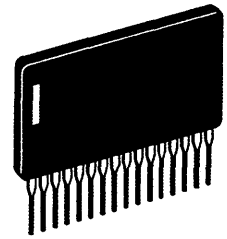
Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	−0.5 to 7.0	V
Input Control Voltage	V_{IN}	−0.5 to 10	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±25	mA
Operating Temperature	T_a	−30 to +85	°C
Storage Temperature	T_{STG}	−40 to +100	°C

Negative value of current means that the current flows from the device.

RECOMMENDED OPERATING CONDITIONS

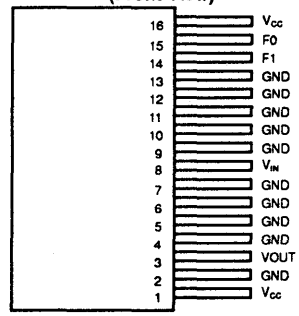
Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	V
Input Control Voltage	V_{IN}	0.5 to 5.0	V
Operating Temperature	T_a	−20 to +70	°C

Note: *Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



Metal Case
SIP-16

(Front View)



Terminal No.	Terminal Name	Description
1, 16	V_{CC}	Power Supply Terminal
3	V_{OUT}	Output Terminal
8	V_{IN}	Control Voltage Intput Terminal
2, 4, 5, 6, 7, 9, 10, 11, 12,13	GND	Grounding Terminal[1]
14	F1	Frequency Switching Terminal[2]
15	F0	Frequency Switching Terminal[2]

1 The GND terminal and the V_{CC} terminals are not connected inside the module. So be sure to route them on the PC board.

2 The F1 and F0 bits switch the oscillation frequencies. The F1 and F0 bits are equivalent to bits 25 and 24 of the EIAJ Digital I/O Standard.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

STANDARD COMBINATION OF FREQUENCIES

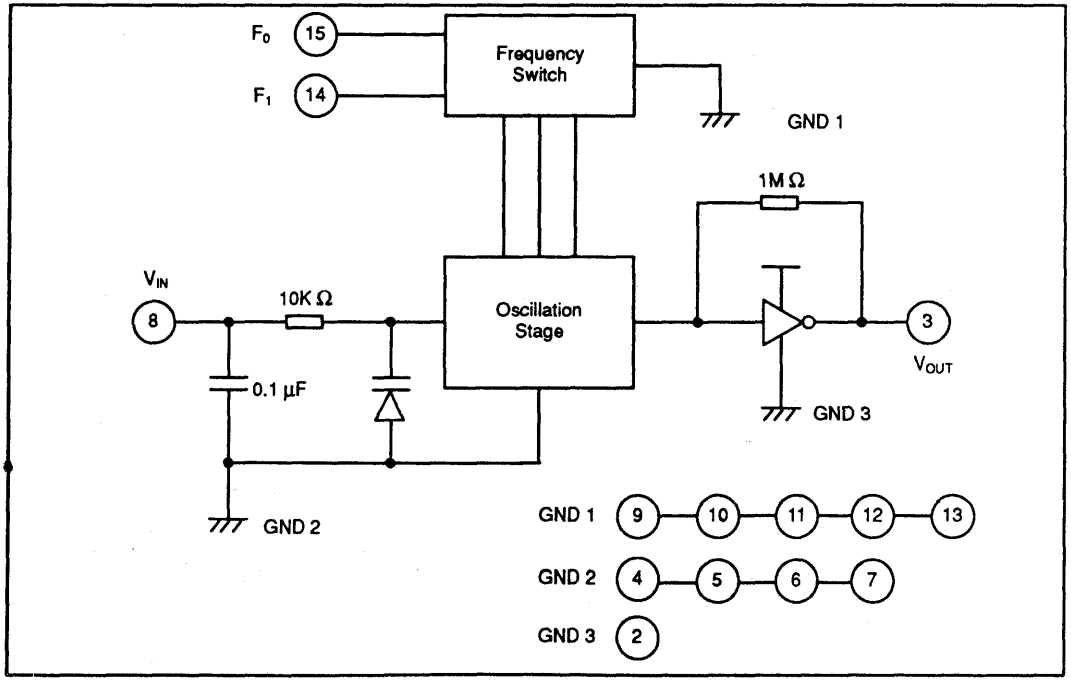
Type A (n = 256)	f_{01} (L)	8.192 MHz	32 kHz x 256
	f_{02} (M)	11.290 MHz	44.1 kHz x 256
	f_{03} (H)	12.288 MHz	48 kHz x 256
Type B (n = 384)	f_{01} (L)	12.288 MHz	32 kHz x 384
	f_{02} (M)	16.934MHz	44.1 kHz x 384
	f_{03} (H)	18.432 MHz	48 kHz x 384
Type C (n = 512)	f_{01} (L)	16.384 MHz	32 kHz x 512
	f_{02} (M)	22.579 MHz	44.1 kHz x 512
	f_{03} (H)	24.576 MHz	48 kHz x 512

SWITCHING BIT DESIGNATION

F1	F0	Oscillation Frequency
H	H	f_{01} (L): 32 kHz x n
L	L	f_{02} (M): 44.1 kHz x n
H	L	f_{03} (H): 48 kHz x n
L	H	Stop

Note: n = 256, 384, 512

BLOCK DIAGRAM

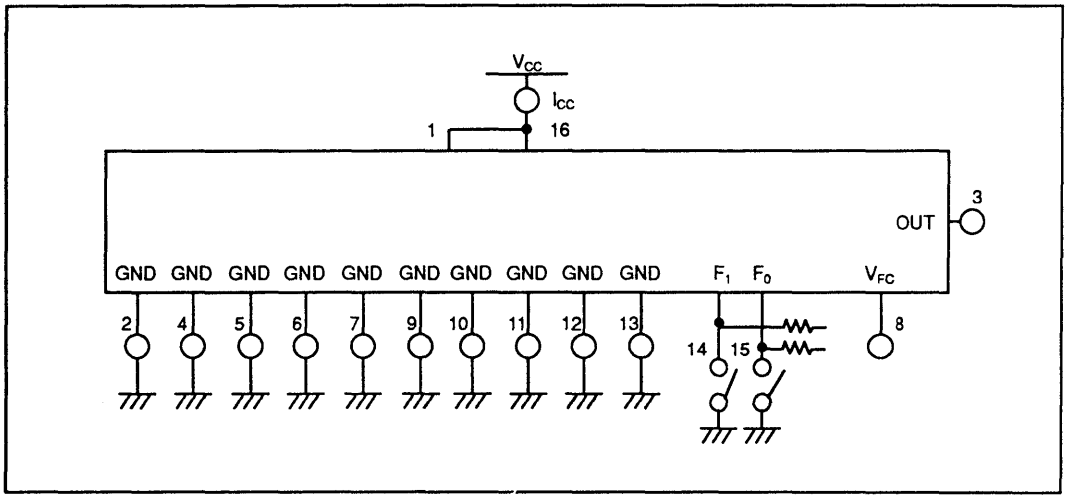


ELECTRICAL CHARACTERISTICS

DC Characteristics

Item		Symbol	Condition	Ratings			Unit
				Minimum	Normal	Maximum	
Output Voltage	H	V_{OH}	I_{OH} = −20 µA	V_{CC} −0.5	5.0	—	V
	L	V_{OL}	I_{OL} = 20 µA	—	0.0	0.5	V
Power Supply Current		I_{CC}	Not Loaded	—	4.6	15	mA

Measuring Circuit Diagram



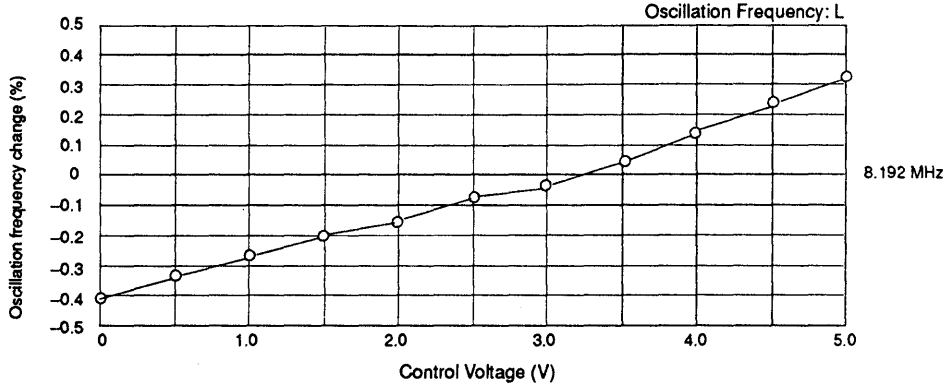
AC Characteristics

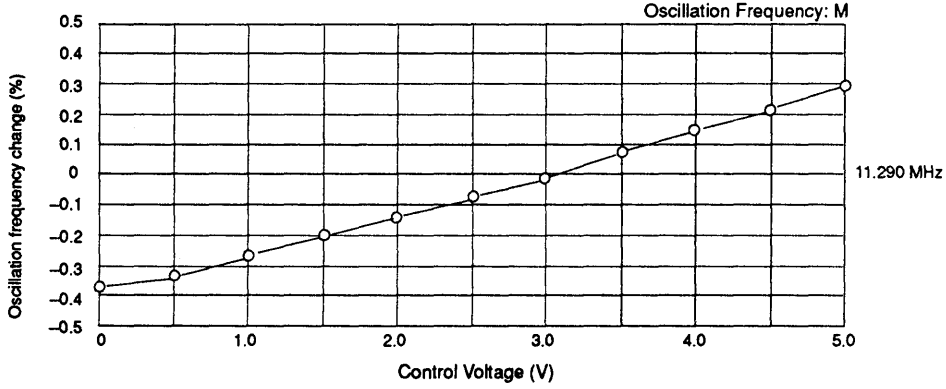
Item	Symbol	Condition	Ratings		Unit	Remarks
			Minimum	Maximum		
Oscillation Frequency One	f_{H1}	V_{IN} = 4.5 V	1.0015f_{01}	—	MHz	Nominal frequency F_0 reference
	f_{L1}	V_{IN} = 0.5 V	—	0.9985f_{01}	MHz	
Oscillation Frequency Two	f_{H2}	V_{IN} = 4.5 V	1.0015f_{02}	—	MHz	
	f_{L2}	V_{IN} = 0.5 V	—	0.9985f_{02}	MHz	
Oscillation Frequency Three	f_{H3}	V_{IN} = 4.5 V	1.0015f_{03}	—	MHz	
	f_{L3}	V_{IN} = 0.5 V	—	0.9985f_{03}	MHz	
Frequency Voltage Stability	Δf (V_{CC})	V_{CC} = 4.75 to 5.25 V	−100	100	ppm	5 V reference, V_{IN} = 0.5, 4.5 V
Frequency Temperature Stability	Δf (T_a)	T_a = −20 to +70°C	−500	500	ppm	25°C reference V_{IN} = 0.5, 4.5 V

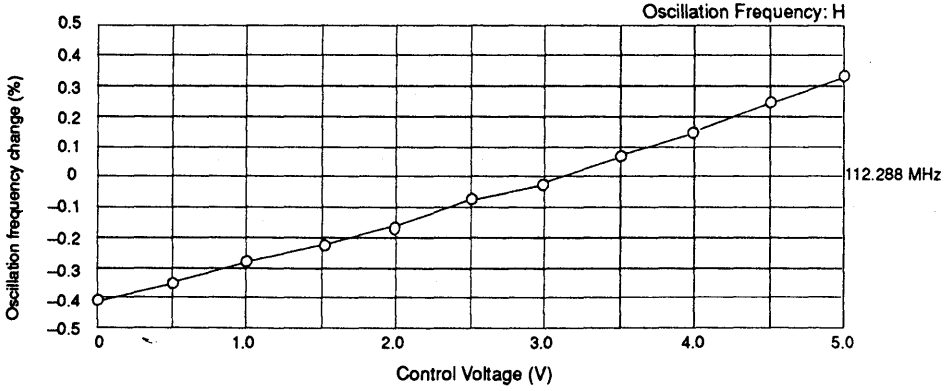
STANDARD CHARACTERISTICS

1A. Control Voltage and Oscillation Frequency Changes

Part Number: M2SC-12M288-D300



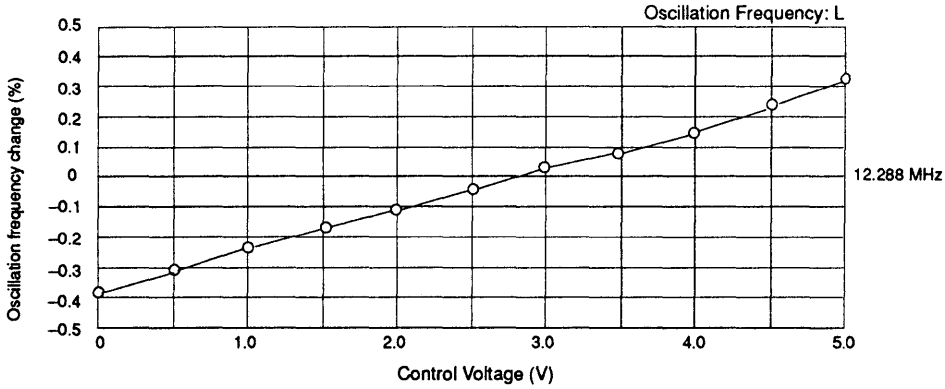


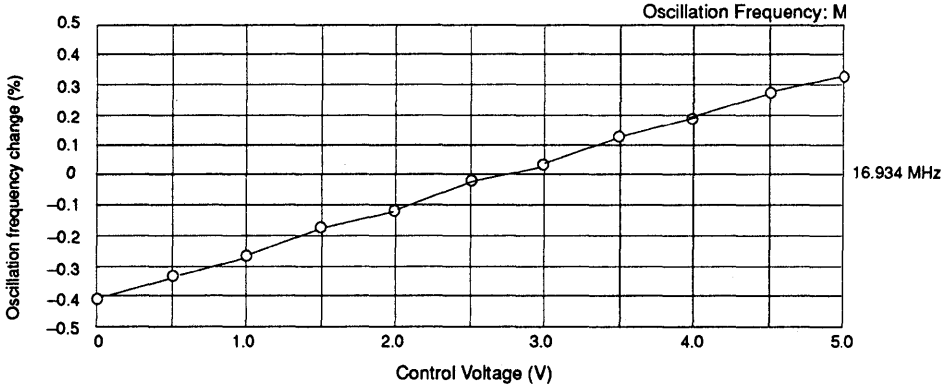


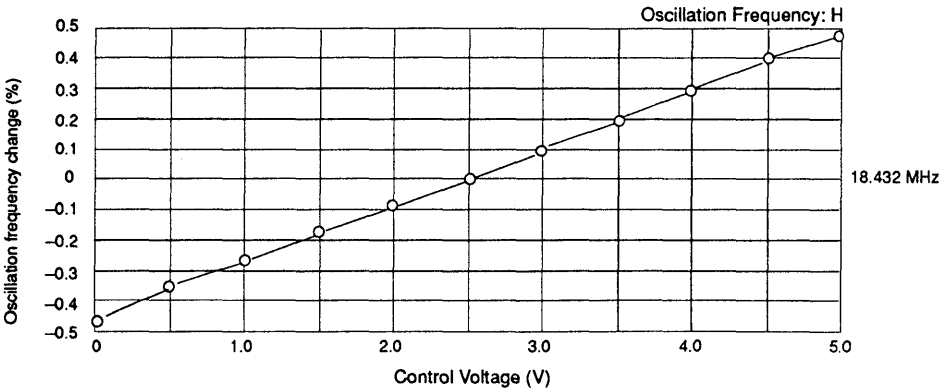
STANDARD CHARACTERISTICS

1B. Control Voltage and Oscillation Frequency Changes

Part Number: M2SC-18M432-D300





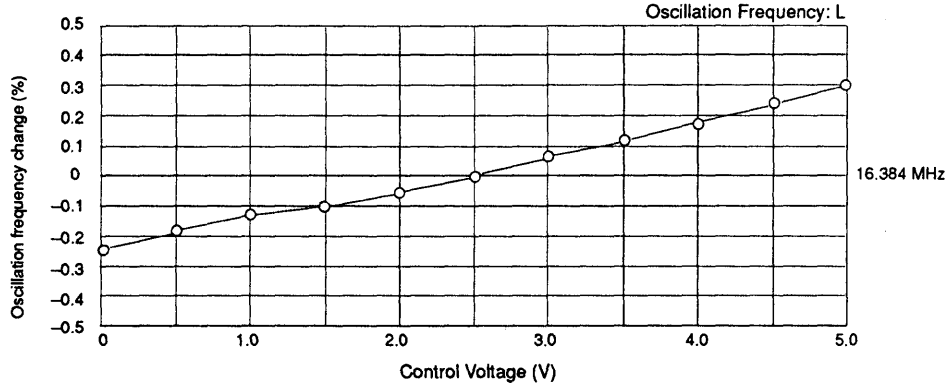


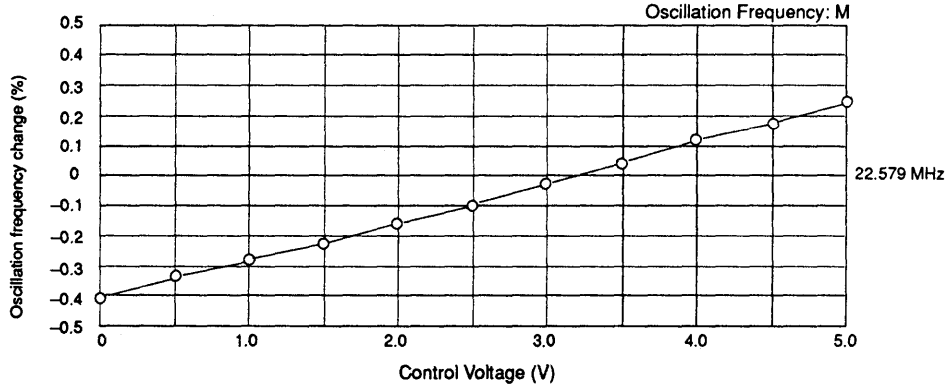
7

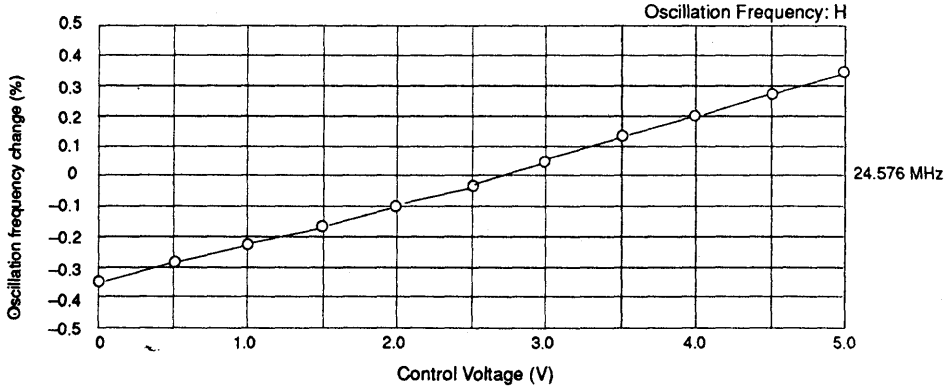
STANDARD CHARACTERISTICS

1C. Control Voltage and Oscillation Frequency Changes

Part Number: M2SC-24M576-D300

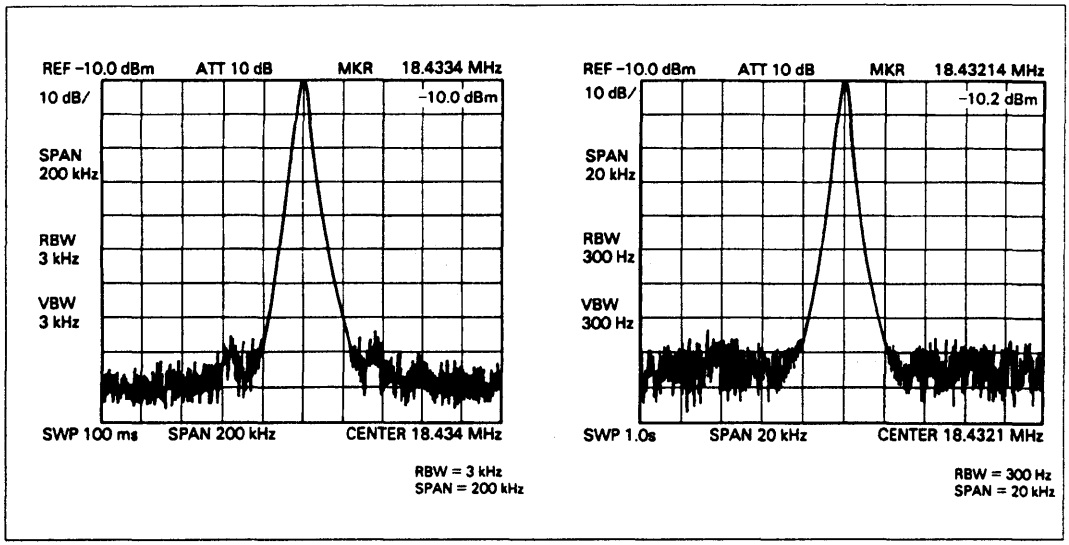






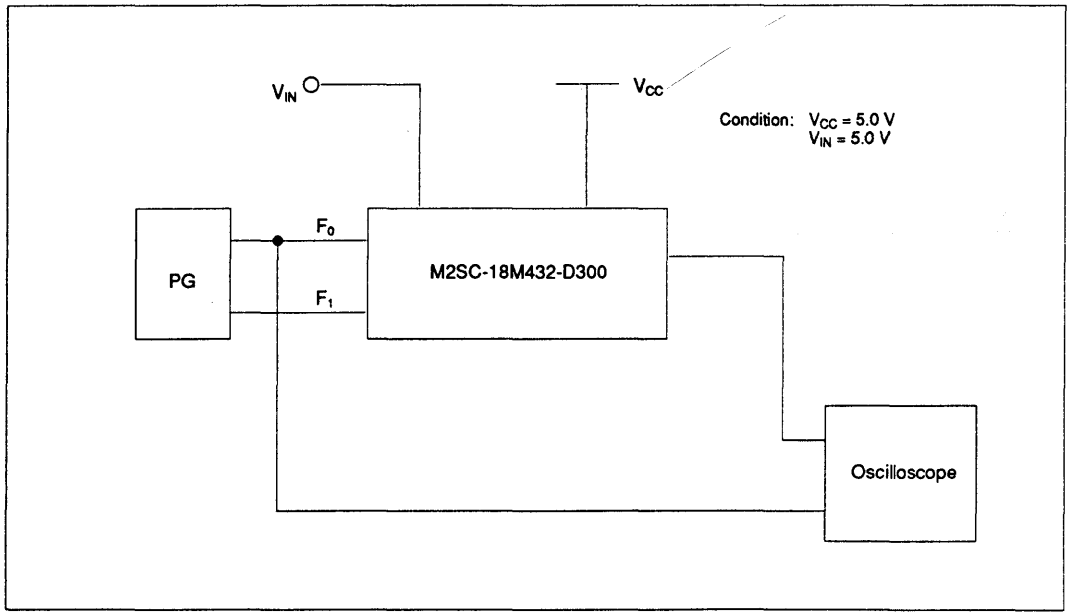
2. Oscillation Spectrum

Part Number: M2SC-18M432-D300
Example of f_{03} = 18.432 MHz



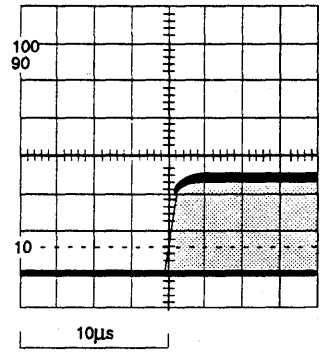
3. Frequency Switch Oscillation Startup Characteristics

The characteristics in the circuit below were measured with V_{CC} = 5.0 V and V_{FC} = 5.0 V.



4. Frequency and Switching Oscillation Startup Characteristics

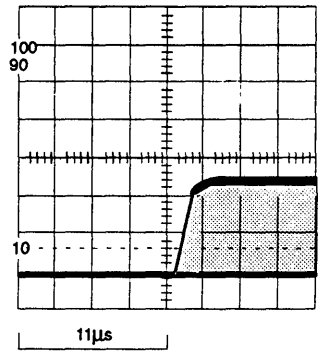
A. Condition: Stop → 12.288 MHz



Stop → 12.288 MHz

2 V/div
2µs/div

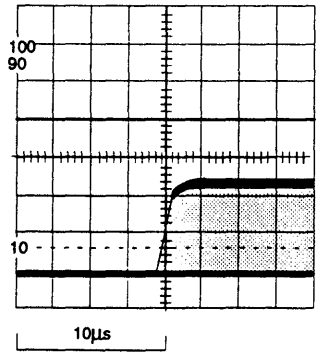
B. Condition: Stop → 16.934 MHz



Stop → 16.934 MHz

2 V/div
2µs/div

C. Condition: Stop → 18.432 MHz



Stop → 18.432 MHz

2 V/div
2µs/div

PART NUMBERING SYSTEM

[Part Number Example]

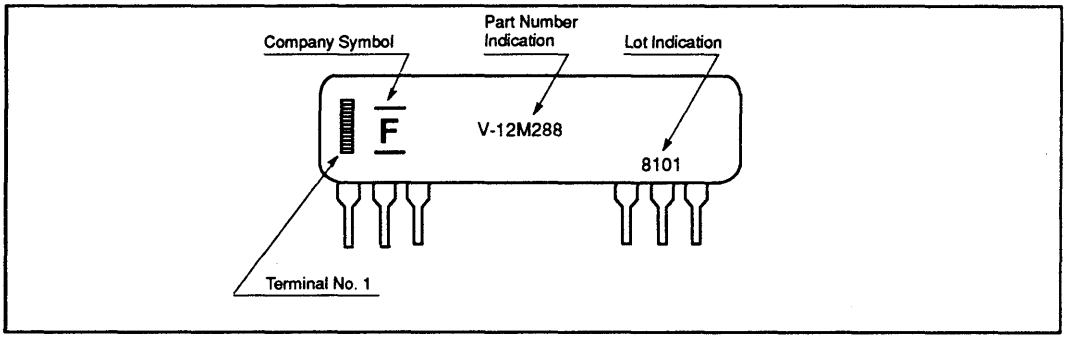
M2SC-□□□□□□ - D □□□
① ②

① Frequency designation: Designates the highest frequency of the combined nominal frequency types in six alphanumeric characters. M indicates the decimal point in MHz.

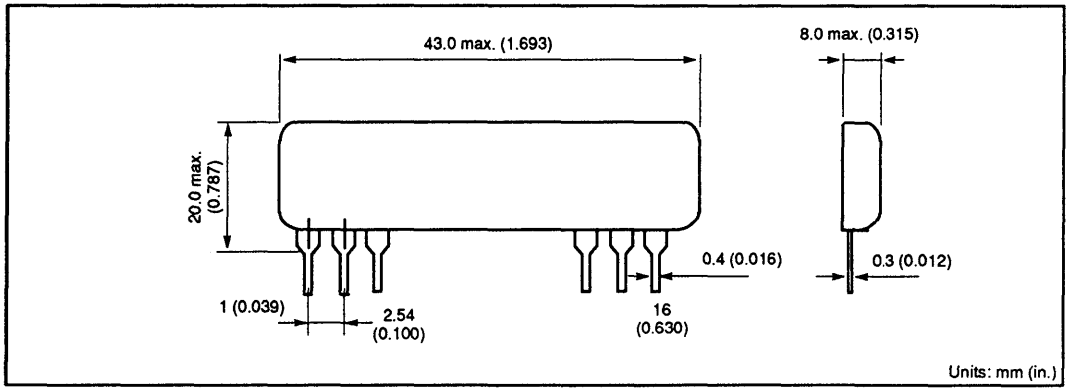
Frequency	Designation
(12.288 MHz)	Type A: 12M288
(18.432 MHz)	Type B: 18M432
(24.576 MHz)	Type C: 24M576

② Serial numbers of the series:
Standard for the M2 series (D300): D300

MARKING



DIMENSIONS



October 1990
Edition 1.0

FUJITSU

DATA SHEET

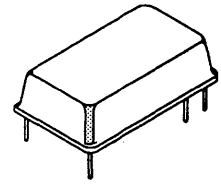
M3 Series (D001)
Piezoelectric Device (Voltage Controlled Oscillator)

DESCRIPTION

The M3 series voltage controlled oscillators (VCO) operate in the frequency range of 50 to 300 MHz. The M3 series VCOs use a single $LiTaO_3$ (lithium tantalate) piezoelectric crystal with a high electromechanical coupling coefficient and a SAW resonator that has an original configuration. The M3 series VCOs oscillate directly in the VHF band up to 300 MHz, and have a wide variable frequency width and high temperature stability.

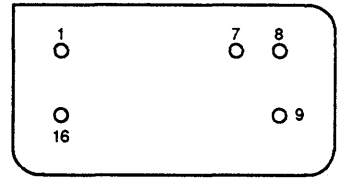
FEATURES

- Direct oscillation at high frequencies: 50 to 300 MHz
- Wide variable frequency width: 800 ppm/V minimum (0.5 to 4.5 V)
- Superb temperature characteristics: Within ±200 ppm (0 to 60°C)
- High-precision oscillation frequency, ready for use without adjustment
- High reliability due to hermetically sealed package
- High carrier noise ratio: –90 dB or less (12.5 kHz detuning, 8 kHz band)
- Compact size: Compatible with 16-pin DIP IC packages
- Frequency offset by built-in offset terminal
- Three types of standard frequencies available



Metal Case
DIP-16

(Bottom View)



Terminal No.	Terminal Name	Description
1	V_{IN1}	Offset Terminal
7	GND	Grounding Terminal
8	V_{OUT}	Oscillation Output Terminal
9	V_{CC}	Power Supply Terminal
16	V_{IN2}	Control Voltage Input Terminal

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Input Control Voltage	V_{IN2}	–0.5 to 7.0	V
Operating Temperature	T_a	0 to 60	°C
Storage Temperature	T_{STG}	–40 to 85	°C
Control Polarity		Positive Polarity	
Oscillation Frequency Range		50 to 300	MHz

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	5.0	V
Input Control Voltage	V_{IN2}	0.5 to 4.5	V
Operating Temperature	T_a	0 to 60	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7

STANDARD FREQUENCIES

Frequency	Application	Part Number
74.25 MHz	Professional HDTV	M3DA-74M250-D001
97.2 MHz	Transmission Standard HDTV	M3DA-97M200-D001
115.52 MHz	Broad-band ISDN	M3DA-155M52-D001

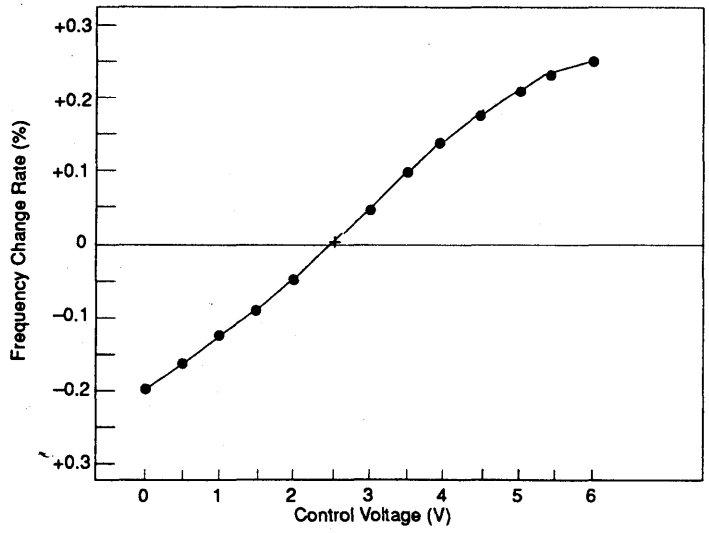
ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Ratings			Unit	Remarks
			Minimum	Typical	Maximum		
Oscillation Frequency Deviation	Δf_o	V_{IN2} = 2.5 V	–500	—	+500	ppm	f_o reference
Variable Width of Oscillation Frequency	$\frac{(f_H - f_L)}{f_o}$	V_{IN2} = 0.5 V V_{IN2} = 4.5 V	800	—	—	ppm/V	
Temprature Stability of Oscillation Frequency	$\Delta f\ (T_a)$	V_{IN2} = 2.5 V	–200	—	+200	ppm	25°C reference, T_a = 0 to 60°C
Output Level	P_{OUT}	V_{IN2} = 2.5 V	0	5	7	dBm	50 Ω termination
Output Level Stability	$\Delta P\ (V_F)$	V_{IN2} = 0.5 V V_{IN2} = 4.5 V	–2	—	+2	dB	V_{IN2} = 2.5 V reference
Output Level Temperature Stability	$\Delta P\ (T_a)$	V_{IN2} = 2.5 V	–2	—	+2	dB	25°C reference, T_a = 0 to 60°C
Current Consumption	I_{CC}	—	—	—	30	mA	
Oscillation Frequency Power Supply Voltage Fluctuation	$\Delta f\ (V_{CC})$	V_{IN2} = 2.5 V	–50	—	+50	ppm	V_{CC} = 5 V reference, ±5%

STANDARD CHARACTERISTICS

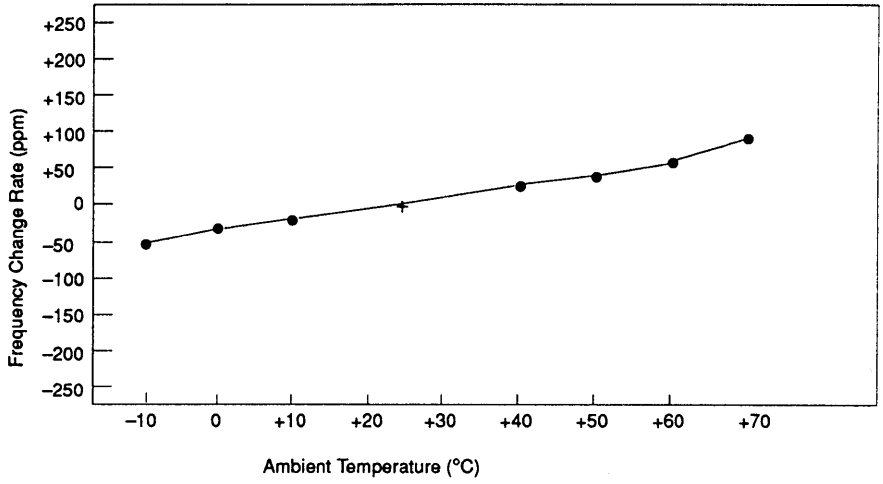
The examples below show characteristics of the M3 VCO devices at 155.52 MHz.

Example 1. Frequency Variable Characteristics

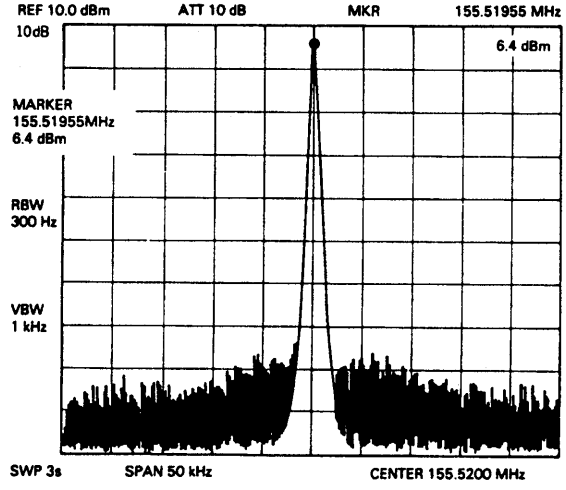


STANDARD CHARACTERISTICS (Continued)

Example 2. Temperature Characteristics



Example 3. Oscillation Spectrum



7

PART NUMBERING SYSTEM

(Part Number Example)

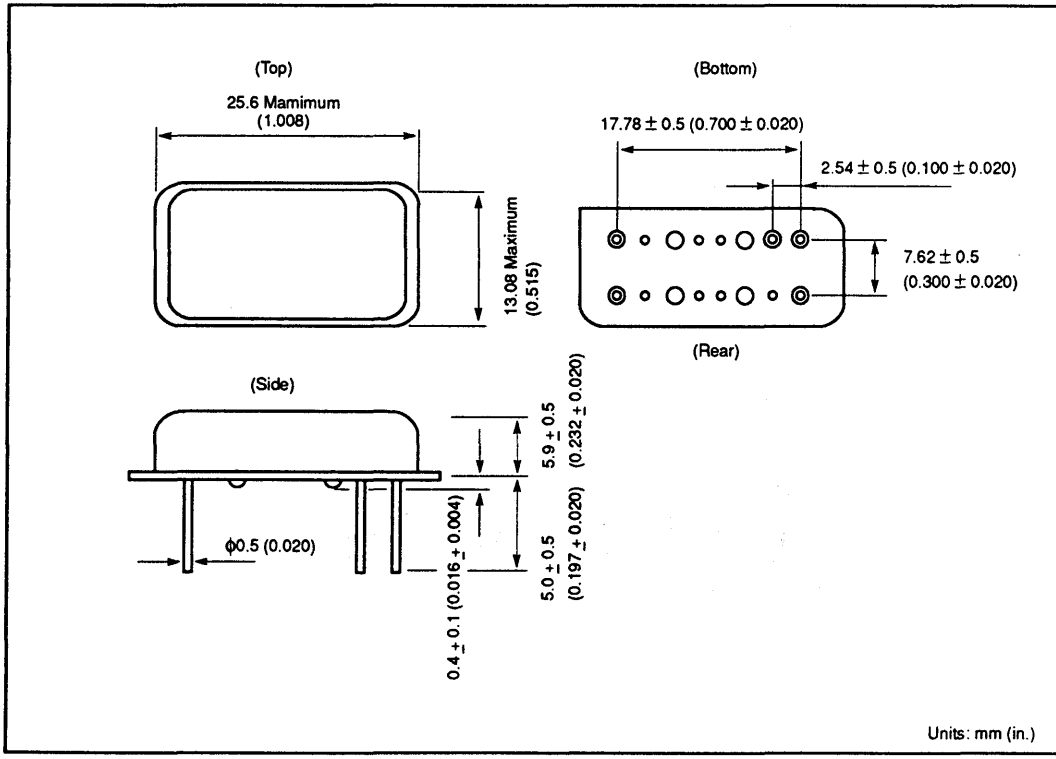
M3DA-□□□□□□ - D □□□
① ②

① Frequency designation: Designates the nominal frequency in six alphanumeric characters. M indicates the decimal point in MHz.

Frequency	Designation
74.25 MHz	74M250
97.2 MHz	97M200
115.52 MHz	115M52

② Serial Number (of the series):
Standard: 001
Non-standard products: 001 to 099

PACKAGE DIMENSIONS



October 1990
Edition 1.0

DATA SHEET

FUJITSU

M3 Series (D101)
Piezoelectric Device

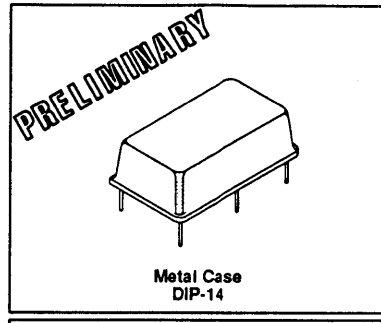
Modulator, 50 MHz to 300 MHz

DESCRIPTION

These piezoelectric modulators feature direct oscillators (50 MHz to 300 MHz). The piezoelectric modulator uses a lithium tantalate piezoelectric single crystal ($LiTaO_3$) with a high electromechanical coupling coefficient. The piezoelectric modulator employs an exclusive SAW resonator. The piezoelectric modulator can be used in direct modulation applications needing high modulation sensitivity and a high signal noise ratio in the VHF band (up to 300 MHz).

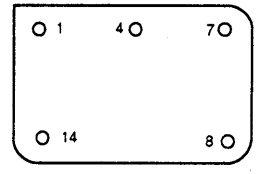
FEATURES

- High frequency direct modulation: 50 to 300 MHz
- High modulation sensitivity: 800 ppm/V min. (0.5 to 4.5 V)
- Excellent modulation distortion ratio: 40 dB max. (1 KHz to 1.75 KHz dev.)
- Excellent signal noise ratio: –50 dB max.
- Excellent temperature characteristic: ±200 ppm max. (–20 to 70°)
- Highly reliable hermetically sealed package
- Compatible with 14-pin DIP IC packages



Metal Case
DIP-14

(Bottom View)



Terminal No.	Terminal Name	Description
1	ML	Control Voltage Input Terminal
4	MM	Modulation Input
7	GND	Grounding Terminal
8	V_{OUT}	Oscillation Output Terminal
14	V_{CC}	Power Supply Terminal

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
ML Pin Input Voltage	V_{ML}	–0.5 to 10	V
MM Pin Input Voltage	V_{MM}	–0.5 to 7.0	V
ML Pin Modulation Polarity		Positive	
MM Pin Modulation Polarity		Negative	
Operating Temperature	T_a	–20 to +85	°C
Storage Temperature	T_{STG}	–40 to +100	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	V
ML Pin Input Voltage	V_{ML}	2.5	V
Operating Temperature	T_a	–20 to 70	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7

STANDARD FREQUENCY

Standard Frequency	Application	Part Number
145.0 MHz	Mobile Phone	M3DA-145M00-D101

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V)

Item		Symbol	Condition	Ratings Min.	Ratings Typ.	Ratings Max.	Unit	Remarks
Oscillation Frequency Deviation		Δf_o	V_{ML} = 2.5 V	–300	—	+300	ppm	f_o reference
Variable Width of Oscillation Frequency		$\frac{(f_H - f_L)}{f_o}$	V_{ML} = 0.5 V V_{ML} = 4.5 V	800	—	—	ppm/V	
Temperature Stability of Oscillation Frequency		Δf (T_a)	V_{ML} = 2.5 V	–200	—	+200	ppm	25°C reference, T_a = –20 to 70°C
Output Level		P_{OUT}	V_{ML} = 2.5 V	–5	–3	–1	dBm	50 Ω termination
Output Level Stability		ΔP (V_F)	V_{ML} = 0.5 V V_{ML} = 4.5 V	–2	—	+2	dB	V_{ML} = 2.5 V reference
Output Level Temperature Stability		ΔP (T_a)	V_{ML} = 2.5 V	–2	—	+2	dB	25°C reference, T_a = –20 to 70°C
Current Consumption		I_{CC}	—	—	—	10	mA	
Oscillation Frequency Power Supply Voltage Fluctuation		Δf (V_{CC})	V_{ML} = 2.5 V	–50	—	+50	ppm	±5% at V_{CC} = 5 V reference
Modulation Characteristic	Modulation Distortion (1 KHz tone)		1.75 KHz DEV	—	—	–40	dB	15 KHz LPF
			3.5 KHz DEV	—	—	–40	dB	
			5.0 KHz DEV	—	—	–40	dB	
	Signal to Noise Ratio		1.75 KHz DEV	—	—	–50	dB	300 to 3 KHz
	Modulator Input Impedance			10			KΩ	

PART NUMBERING SYSTEM

Designation Example

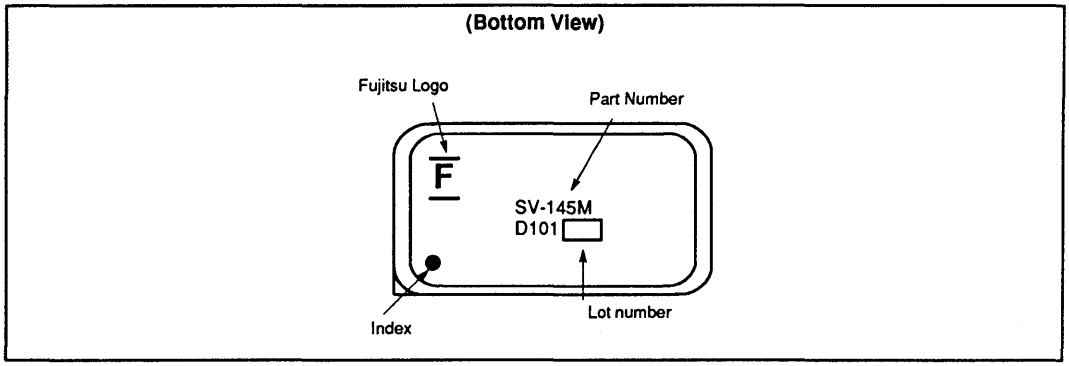
M3DA-□□□□□□ – D□□□

① ②

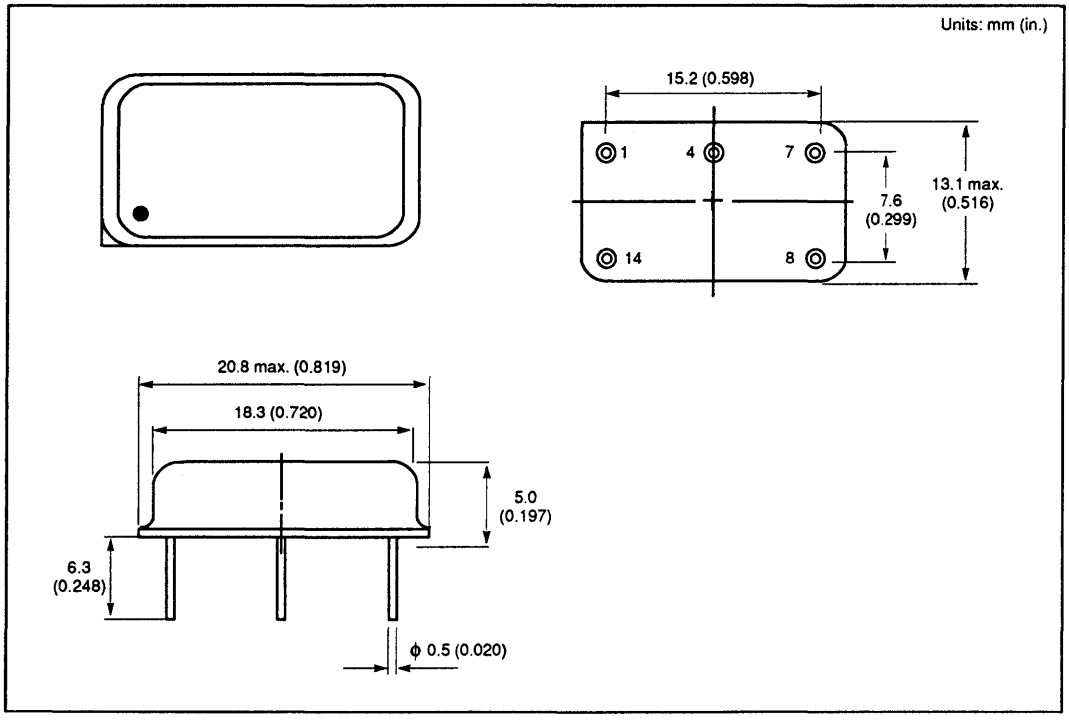
① Frequency Designation: The standard frequency is designated in six alphanumeric characters. M is used to designate the decimal point in MHz. Refer to STANDARD FREQUENCY. Example: 145.0 MHz device is designated as 145M00.

② Serial Number: The serial number is assigned from 101 to 199 (with 101 as the standard).

PACKAGE MARKING



PACKAGE DIMENSIONS



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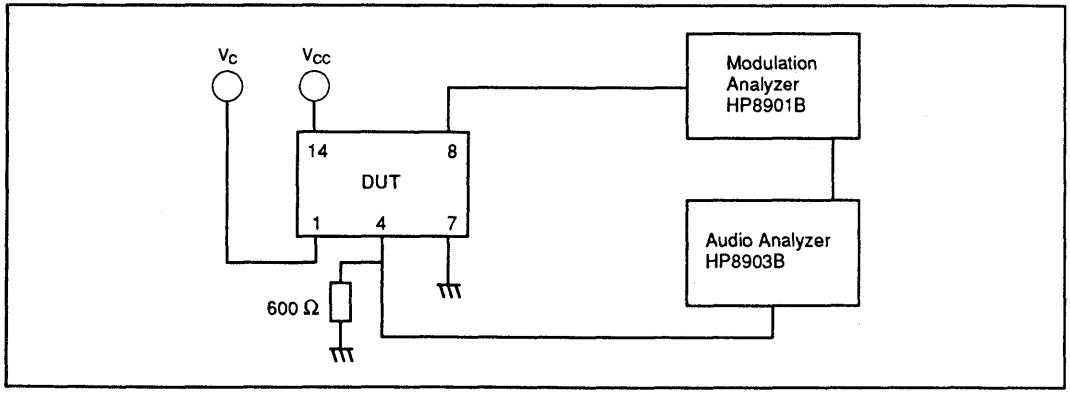
SAW MODULATOR CHARACTERISTICS

M3DA-145M00-D101

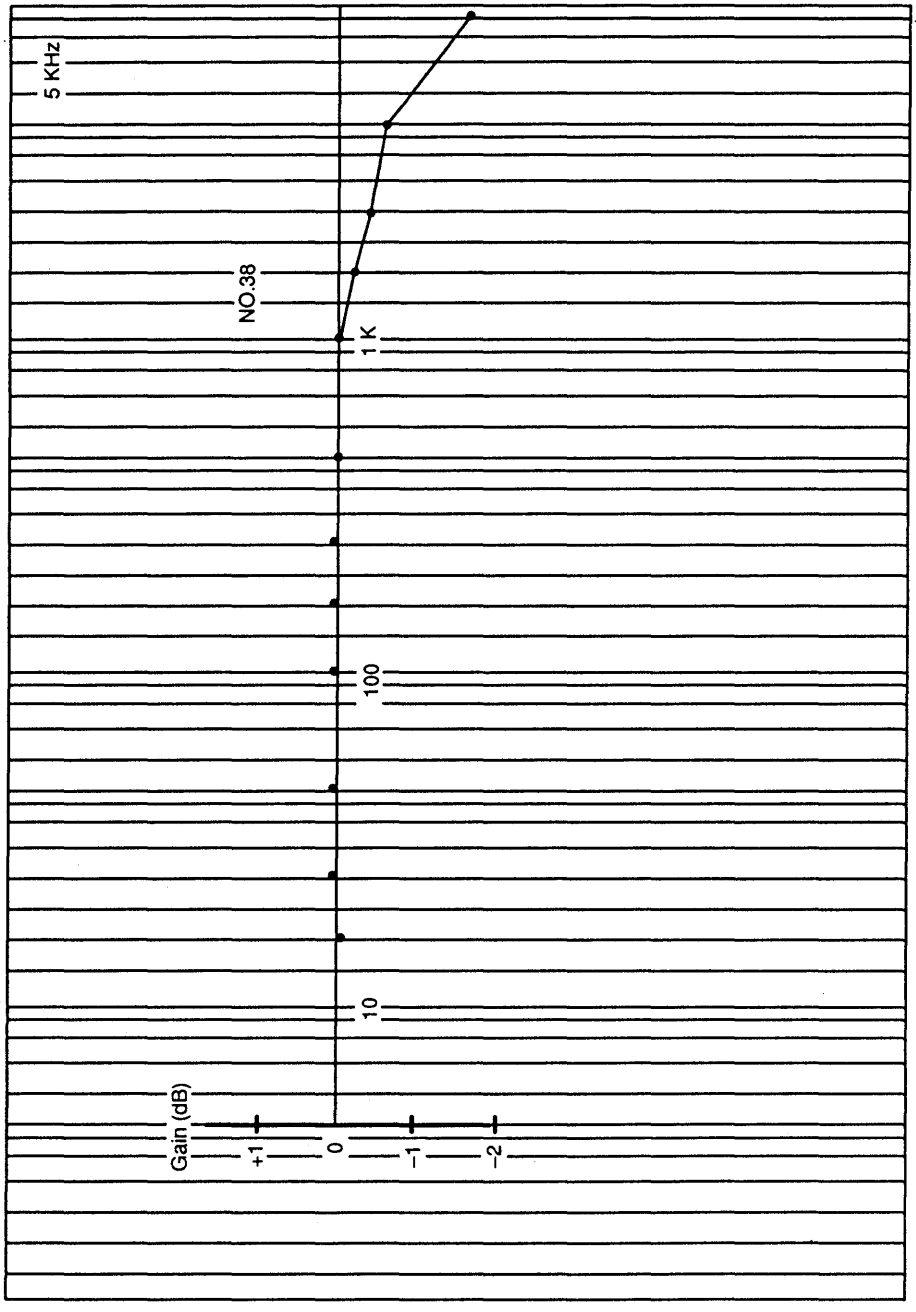
Item		Rating	Characteristics	Remarks
Output Frequency		145.0 MHz	144.997 MHz	V_C = 2.5 V
Current Consumption		10 mA or less (with buffer)	7.3 mA	
Output Level		–3 dBm ±2 dB	–2.00 dBm	V_C = 2.5 V
Spurious Response Ratio		Higher harmonic < 4 dB at 2 f_0 (290 MHz)	–7.3 dB	
Frequency Stability	Power Supply Fluctuation	Within ±50 ppm for 5 V ±0.25 V	+6.00 ppm –5.80 ppm	
	AFC-F-F Characteristic	±550 ppm or more for 2.5 V ±1 V	–789 ppm +1016 ppm	
	Temperature Characteristic	Within ±300 ppm for –35 to +85	+66 ppm +41 ppm	
AFC Voltage Versus Output Frequency Characteristics		At 25 ±5°C, the AFC voltage for the output frequency of 145 MHz is V_C = 2.5 V ±0.3 V	2.501 V	
		At –20 +85°C, the AFC voltage for the output frequency of 145 MHz is V_C = 2.5 V ±0.3 V	2.476 V 2.459 V	–20°C +85°C
Modulation Characteristic	Modulation Input Level	–28 dBm ±3 dB (600 W) 1 KHz ±3.5 KHz DEV*	–26.1 dB	15 KHz LPF
	Modulation Distortion Ratio	–35 dB or less 1 KHz (±1.75 KHz DEV)* –30 dB or less 1 KHz (±3.5 KHz DEV)* –20 dB or less 1 KHz (±5.0 KHz DEV)*	–46 dB –49 dB –48 dB	15 KHz LPF
	Modulation Characteristic	< ±1 dB/20 Hz to 5 KHz ±5 KHz DEV*		
	Signal Noise Characteristic	< –50 dB ±1.75 KHz DEV*	–55 dB	300 to 3 KHz

*Adjust the control voltage for an oscillation frequency of 145 MHz for the modulation characteristic.

Test Circuit

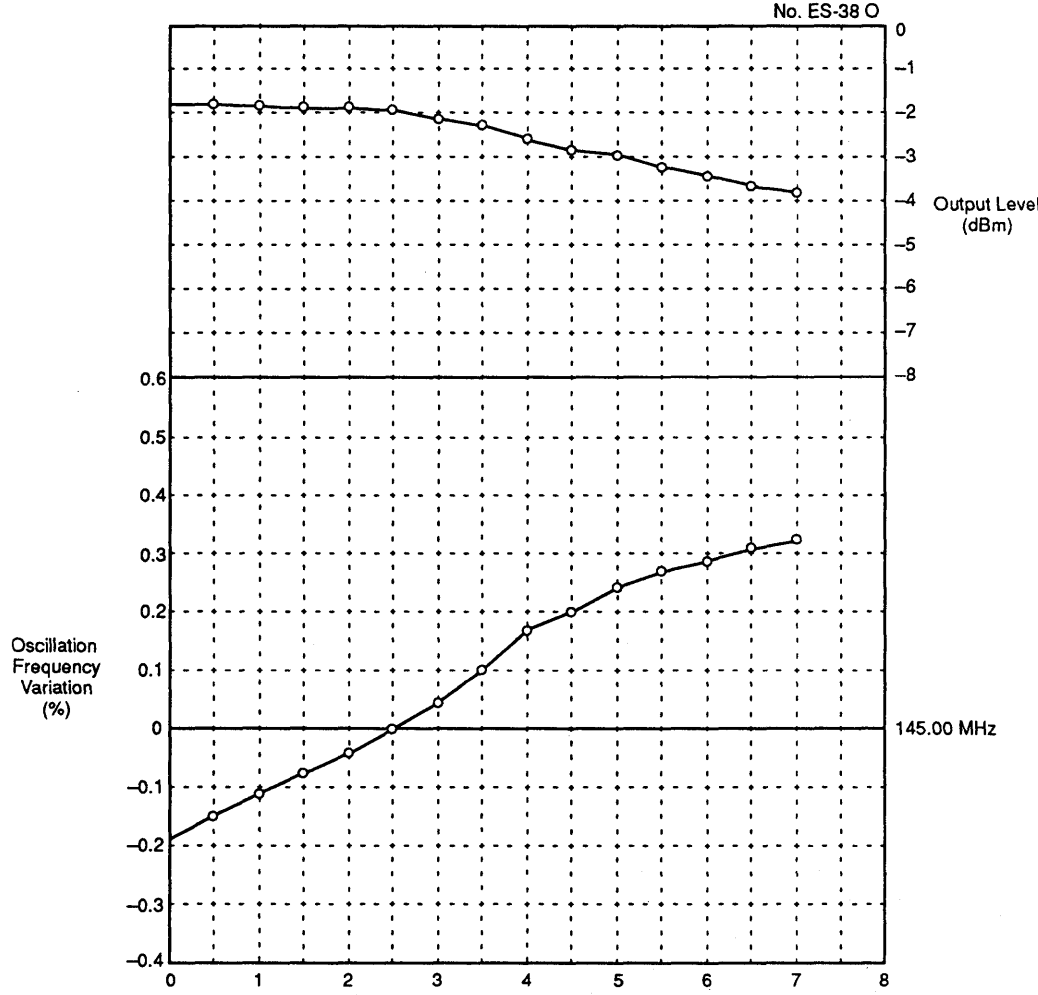


M30A-145M00-D101 MODULATION FREQUENCY CHARACTERISTICS



SAW MODULATOR CHARACTERISTIC DATA

M3DA-145M00-D101

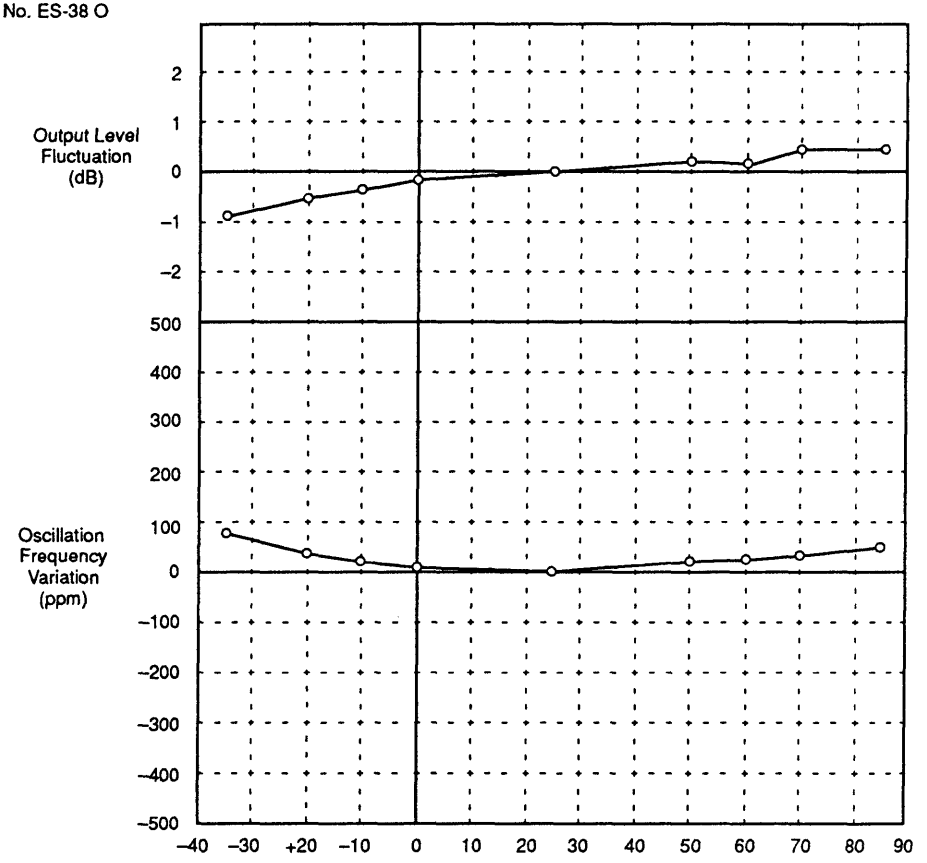


V–F Characteristic

SAW MODULATOR CHARACTERISTIC DATA (Continued)

M3DA-145M00-D101

No. ES-38 O



7

SECTION 8

Power Management Switches – *At a Glance*

The typical cellular handset typifies the recent trend towards compact, lightweight, battery dependent products that can be used anywhere, anytime. Fujitsu's innovative power management switches can effect a reduction of power consumption in the "OFF" state, thereby extending battery life.

Page Number	Part Number	'ON' Resistance	Maximum Handling Current	Comment
8-3	MB3802 (dual switches)	0.12 Ω	1.2 A per channel	Well suited for most portable radio applications
8-17	MB3807A (dual switches)	0.3 Ω (12 V port) 6.0 Ω (5 V port)	0.5 A (12V port) 0.1 A (5V port)	Designed for PCMCIA card controllers; will have niche application to wireless products

February 1995
Edition 1.0a

FUJITSU

DATA SHEET

MB3802
POWER MANAGEMENT SWITCH

DESCRIPTION

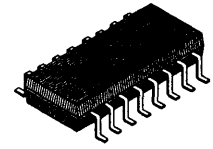
The MB3802 is a dual power management switch incorporating two identical switch circuits which have extremely low ON resistance and consume zero input current when the switches are turned OFF. These features effectively reduce power consumption and extend the battery life of portable, battery–driven products. The MB3802 can be used to efficiently control various power supply systems for Notebook Computers and typical peripheral devices such as Disk Drives and PCMCIA Cards.

The MB3802 switch blocks turn on at a very low input voltage (typical V_{IN} > 2.2 V) and a stable ON resistance is obtained irrespective of the switching voltage since the internal DC/DC converter applies the optimum voltage for the N-ch MOS gate at Switch–ON.

No external diode is required because the switch block is configured with an N-ch MOS structure to prevent the flow of reverse current at Switch–OFF.

Additionally, a load-side capacitor can be discharged at Switch–OFF by an internal discharge switch which is operated by an external control pin.

16-pin plastic SOP
(FPT-16P-M04)



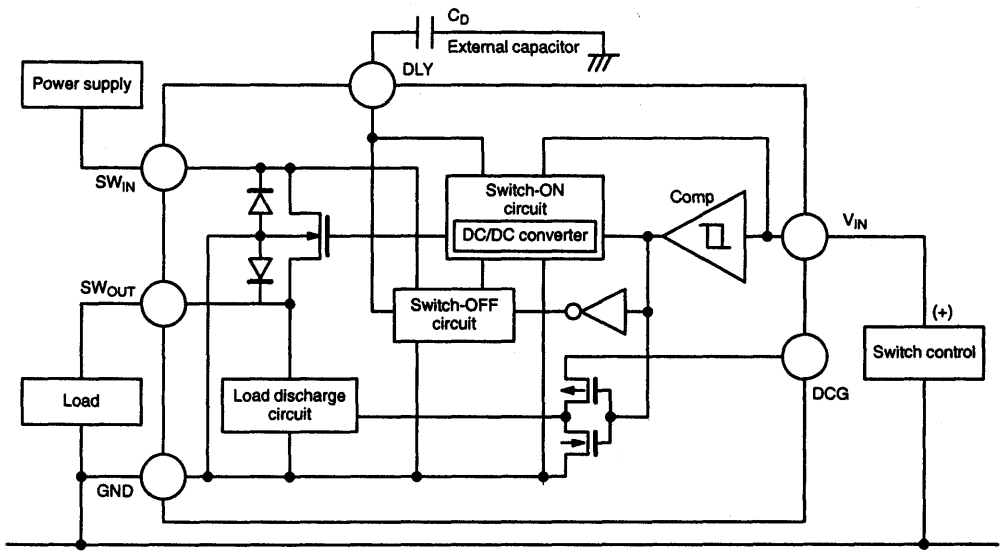
8

FEATURES

- Extremely low ON resistance:
  - R_{ON} = 0.12 Ω (typical)
  - R_{ON} = 0.06 Ω (typical for parallel connection)
- Reverse current protection at load side at Switch–OFF
- Operation start at low input voltage: V_{IN} > 2.2 V (typical)
- Low power consumption
  - At Switch–OFF: I_{IN} = 0 μA, V_{IN} = 0 V
  - At Switch–ON: I_{IN} = 230 μA, V_{IN} = 5 V
- Load discharge function
- External control of ON/OFF time
- Break-before-make operation
- 16 Pin Plastic Flat Package (Suffix: –PF)

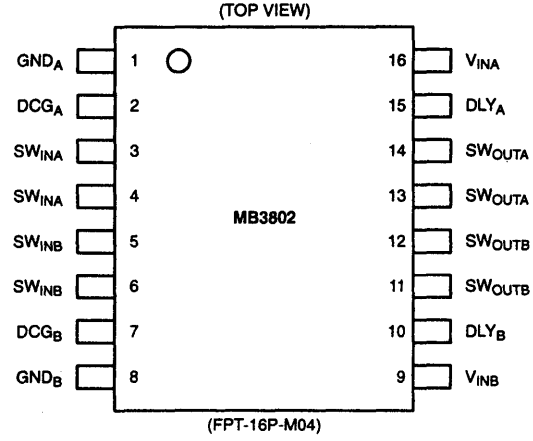
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM AND EXTERNAL CONNECTIONS



Note: The MB3802 incorporates two switch blocks as shown above. However, GND is common to both blocks.

PIN ASSIGNMENT



(FPT-16P-M04)

BLOCK DESCRIPTION

When V_{IN} exceeds 2.2 V, the Comparator starts driving the DC/DC converter which boosts the V_{IN} voltage in order to switch the N-ch MOS, applying the optimum voltage to the switch gate.

When V_{IN} is below 2.1 V, the Comparator stops the DC/DC converter, starts the Switch-OFF circuit, and discharges the voltage from the switch gate to GND. The Switch-OFF circuit is powered from the SW_{IN} and consumes 0.4 µA at 5 V.

Since the N-ch MOS back gate is connected to GND, Switch-OFF reverse current is prevented irrespective of the High level state between SW_{IN} and SW_{OUT}.

The load discharge circuit installed between SW_{OUT} and GND is powered by the DCG pin, and discharges the load-side capacitor at Switch–OFF. When it is not necessary to discharge the load, connect the DCG pin to GND.

The DLY pins are for connection to an external capacitor to delay the Switch-ON/OFF time. The surge current at the load side is reduced during power-on by controlling the Switch-ON time. The Switch-ON time is also dependent on the boot time of the DC/DC converter.

PIN DESCRIPTION

1. Power Management Switch

Pin No.	Pin Symbol	Description
16	V_{INA}	**Switch Control Pins:** These input control pins drive the Switch–ON with a High input level and Switch–OFF with a Low input level. They also serve as power-supply pins for the DC/DC converter to generate the switch gate voltage.
9	V_{INB}	
3, 4	SW_{INA}	**Switch input pins:** Two common pins are assigned to SW_{INA} and SW_{INB}. They serve as input power supply pins for the Load Switches and the Switch-OFF circuit.
5, 6	SW_{INB}	
13, 14	SW_{OUTA}	**Switch output pins:** Two common pins are assigned to SW_{OUTA} and SW_{OUTB}. They are typically connected to the high side of the controlled load. When DCGA or DCGB are at a High level, the respective load-discharge circuits implement the discharge function via these pins.
11, 12	SW_{OUTB}	
2	DCG_A	**SW_{OUTA}/SW_{OUTB} discharge control pins:** These pins are used to control the discharge of the load at Switch–OFF. Connect them to GND when the discharge function is not required.
7	DCG_B	
15	DLY_A	**Switch-ON/OFF time control pins:** The ON/OFF time can be delayed by connecting an external capacitor. Both times are delayed about three fold by installing a 500-pF capacitor between these pins and GND. Leave these pins open when they are not used. 10 V may be generated when these pins are open. To keep these pins at high impedance, take care to mount the device so that there is minimal current leakage (less than 0.1 µA).
10	DLY_B	
1	GND_A	***Ground pins for input threshold reference voltage and load discharge:*** When two switching circuits are used, ground both GND pins.
8	GND_B	

8

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(Ta = + 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Input voltage	V_{IN}	—	–0.3 to 7.0	V
Switching voltage	V_{SW}	At Switch–OFF	–0.3 to 7.0	V
		At Switch–ON	–0.3 to 7.0	
Switching current	I_{SW}	At Switch-ON peak	3.6	A
Total Power Dissipation	P_D	Ta ≤ +75 °C	290	mW
Storage temperature	Tstg	—	–55 to +125	°C

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			Min.	Typical	Max.	
Input voltage	V_{IN}	—	0	—	6.0	V
Switching level	V_{SWIN}	At Switch–ON	0	—	6.0	V
		At Switch–OFF	0	—	6.0	
Switching current	I_{SW}	At Switch–ON (for single switch)	—	—	1.2	A
DLY-pin connection capacitance	C_D	—	—	—	10	nF
DLY-pin mounting leak current	I_{DLY}	—	–0.1	—	0.1	µA
Input voltage to load discharge circuit	V_{DCG}	V_{IN} = 3 V, 5 V	2.5	—	6.0	V
Operating temperature	T_{OP}	—	–40	—	+75	°C

3. DC Characteristics

(Ta = +25°C)

Parameter	Symbol	Conditions	Ratings			Unit
			Min.	Typical	Max.	
Input Current	I_{IN1}	V_{IN} = 0 V	—	0	—	μA
	I_{IN2}	V_{IN} = 3 V	—	100	200	μA
		V_{IN} = 5 V	—	230	460	μA
Switching Resistance	R_{ON1}	V_{IN} = 3 V, I_{SW} = 0.5 A, V_{SWIN} = 3 V	—	120	160	mΩ
	R_{ON2}	V_{IN} = 5 V, I_{SW} = 0.5 A, V_{SWIN} = 3 V	—	130	175	mΩ
Switch–OFF leak current	I_L	V_{IN} = 0 V, V_{SWIN} = 6 V	—	0.5	2.0	μA
Input threshold voltage	V_{TH1}	At Switch–ON	2.0	2.2	2.4	V
	V_{TH2}	At Switch–OFF	1.9	2.1	2.3	V
Input hysteresis	V_{HYS}	—	50	100	—	mV
Switch resistance	R_{ON}	V_{IN} = 3 V, 5 V, I_{SW} = 0.5 A	—	—	210	mΩ
		Ta = –40° to +75°C				mΩ
Switch charge resistance	R_{DCG1}	V_{SWOUT} = 3 V, V_{DCG} = 3 V	—	750	1500	Ω
	R_{DCG2}	V_{SWOUT} = 5 V, V_{DCG} = 5 V	—	500	1000	Ω
Input current to switch discharge circuit	I_{DCG}	V_{DCG} = 5 V	—	0	2	μA

4. AC Characteristics

(Ta = +25°C)

Parameter	Symbol	Conditions	Ratings			Unit
			Min.	Typical	Max.	
Switch-ON time	t_{ON1}	V_{IN} = 0 V –> 3 V, V_{SWIN} = 3 V	100	300	900	μS
	t_{ON2}	V_{IN} = 0 V –> 5 V, V_{SWIN} = 5 V	50	150	450	μS
Switch-OFF time	t_{OFF1}	V_{IN} = 3 V –> 0 V, V_{SWIN} = 3 V	20	60	180	μS
	t_{OFF2}	V_{IN} = 5 V –> 0 V, V_{SWIN} = 5 V	10	30	150	μS
Switch-ON/OFF time lag	t_{HYS1}	V_{IN} = 3 V/0 V, V_{SWIN} = 3 V	80	240	720	μS
	t_{HYS2}	V_{IN} = 5 V/ 0 V, V_{SWIN} = 5 V	40	120	300	μS

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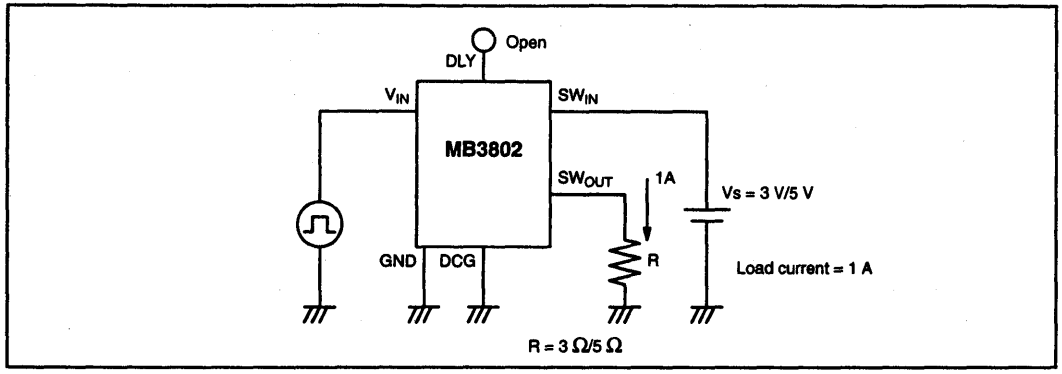
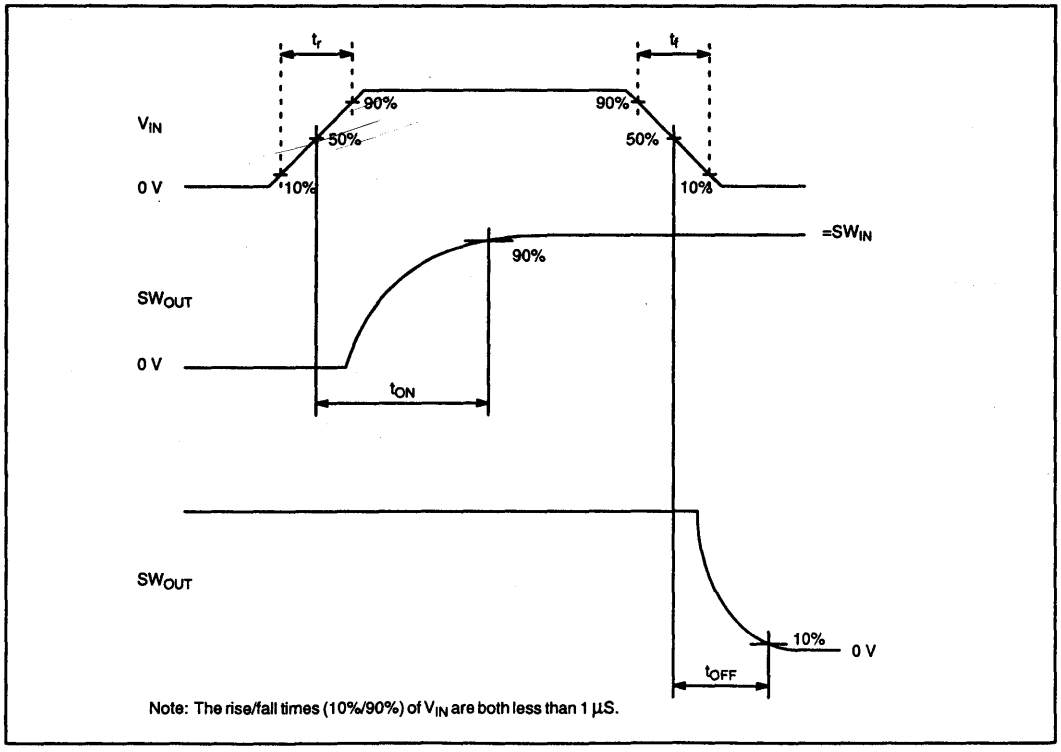
AC CHARACTERISTIC TEST DIAGRAMS

1. Test Condition



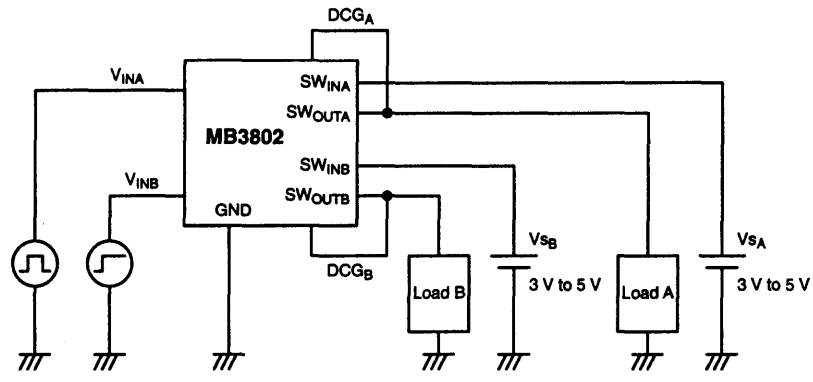
2. Switch-ON/OFF Timing Chart



Note: The rise/fall times (10%/90%) of V_{IN} are both less than 1 µS.

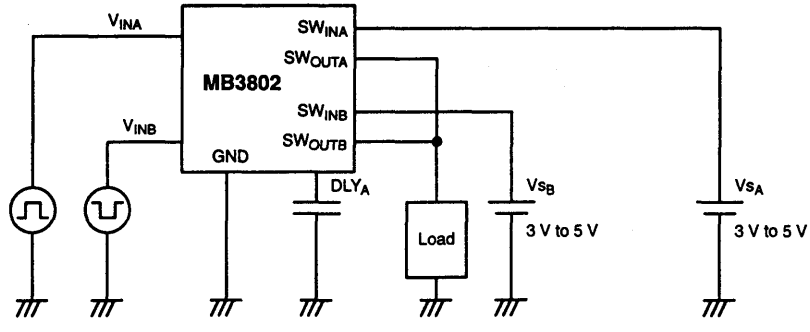
APPLICATIONS

1. Separate Use of Two Switching Circuits



Notes:
1. The two power supplies V_{SA} and V_{SB} can be used separately by controlling the voltages V_{INA} and V_{INB}.
2. Connect the DCG pin to GND when it is not used.

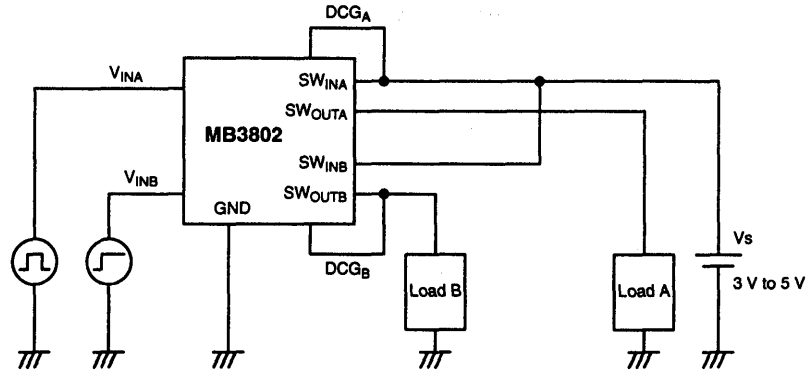
2. Switching Two Power Supplies



Note: When using different power supplies for a single load, control them by connecting an external capacitor so that both switches are not ON at the same time.

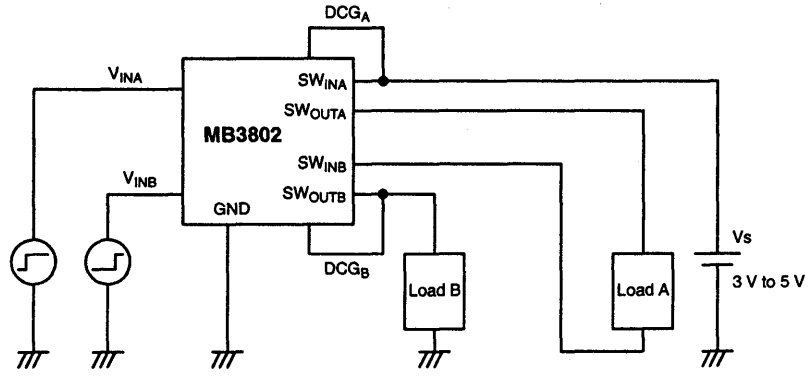
8

3. Switching Two Loads



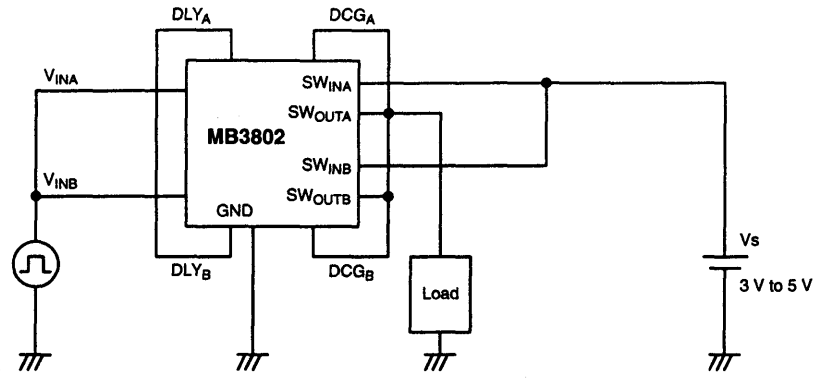
Note: Make this connection to control two different loads separately using a single power supply.

4. Connecting Serial Switches



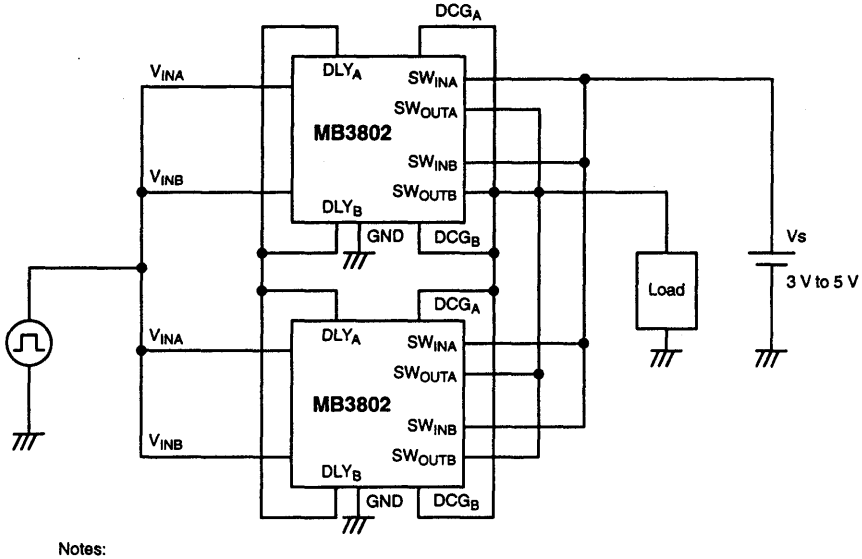
Note: Make this connection to supply power from V_S to load B via load A.

5. Connecting Parallel Switches



Note: Connect the circuits A and B in parallel to produce a low ON resistance (R_{ON} = 0.06 Ω). In this case, connect the DLYA and DLYB pins in common to give synchronous ON/OFF between both switches.

6. 25% ON Resistance

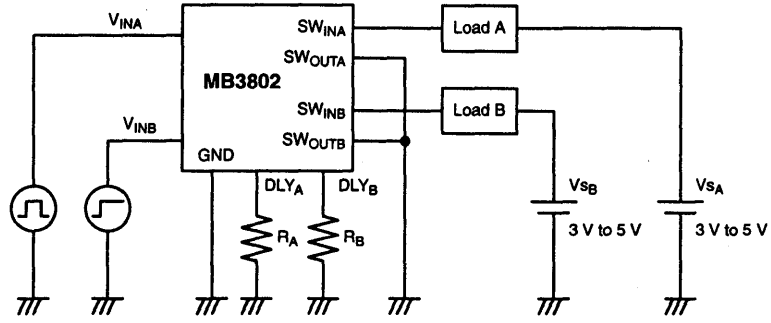


Notes:

1. Make this connection to produce an ON resistance that is much lower than the single device parallel switch connection (as shown in 5.) Also, connect the DLY pins in common.
2. Consider the differences between the ON resistances and the Switch-ON/OFF times between the two devices (MB3802) and insure that load control is not offset at one device.

8

7. Low-side Switch



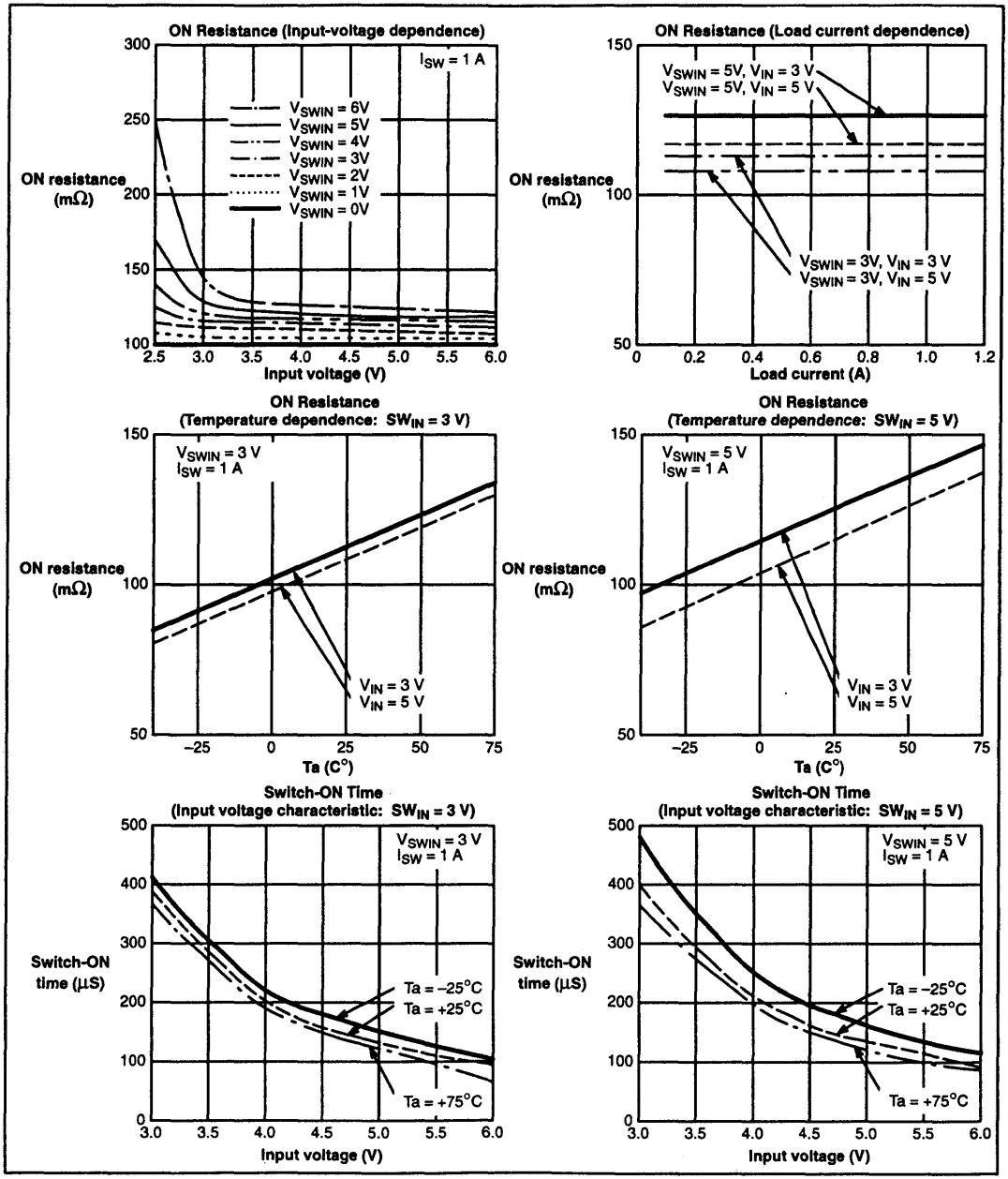
	V_{IN} = 3 V, V_S = 3 V	V_{IN} = 5 V, V_S = 5 V
Switch-ON time	80 µS	45 µS
Switch-OFF time	5.0 mS	3.5 mS

R_A and R_B = 10 MΩ

Notes:

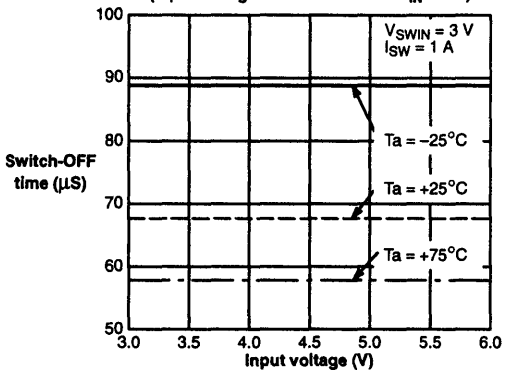
1. Make this connection to control the Switch–ON/OFF at the lower load side.
2. To assist the Switch-OFF circuit operation driven by the SW_{IN} power supply, connect high resistances (R_A and R_B = 5 to 10 MΩ) to the DLY pins without overloading the DC/DC converter.
3. With this connection, the Switch-OFF time is longer than the Switch-ON time.

TYPICAL CHARACTERISTICS CURVES

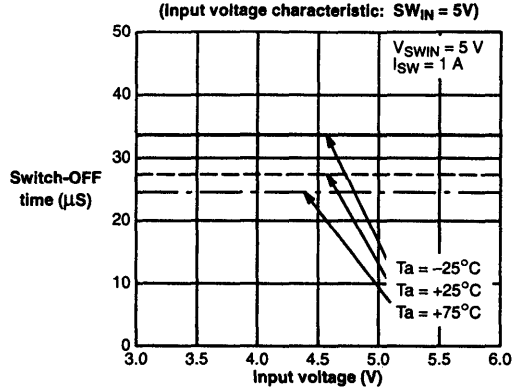


8

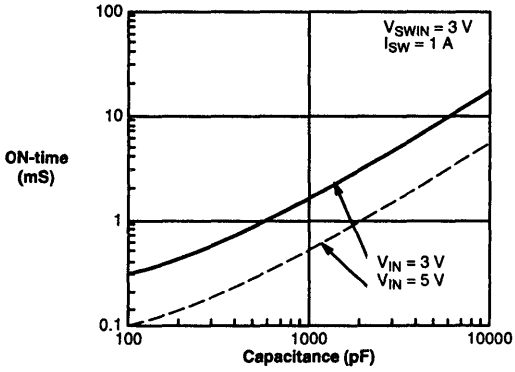
Switch-OFF Time
(Input voltage characteristic: SW_{IN} = 3 V)



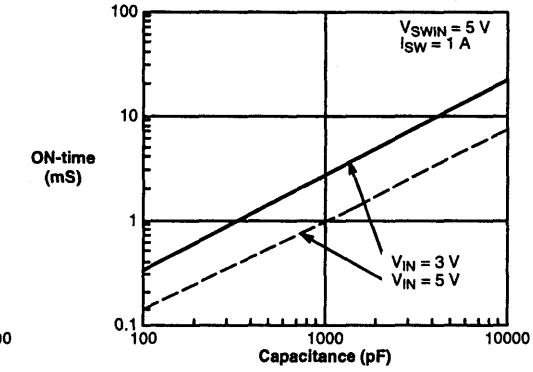
Switch-OFF Time
(Input voltage characteristic: SW_{IN} = 5V)



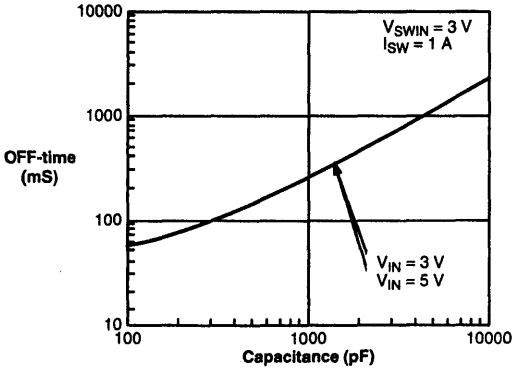
Switch-ON Time
(DLY-pin connection capacitance: SW_{IN} = 3 V)



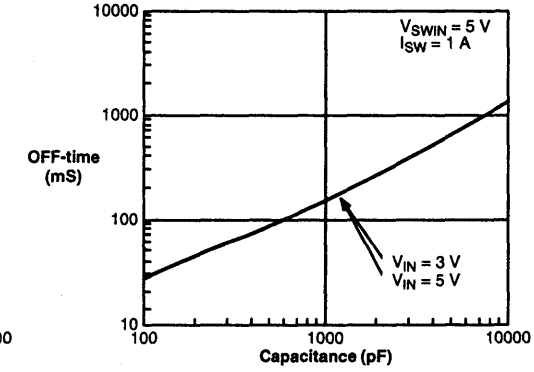
Switch-ON Time
(DLY-pin connection capacitance: SW_{IN} = 5 V)



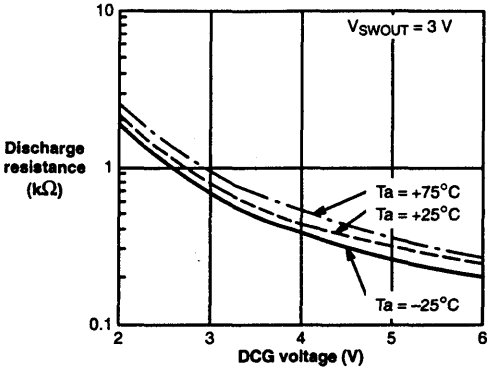
Switch-OFF Time
(DLY-pin connection capacitance: SW_{IN} = 3 V)



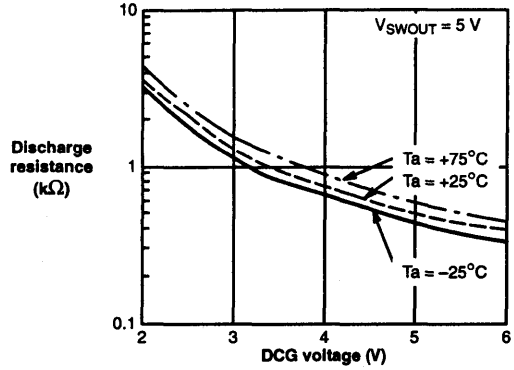
Switch-OFF Time
(DLY-pin connection capacitance: SW_{IN} = 5 V)



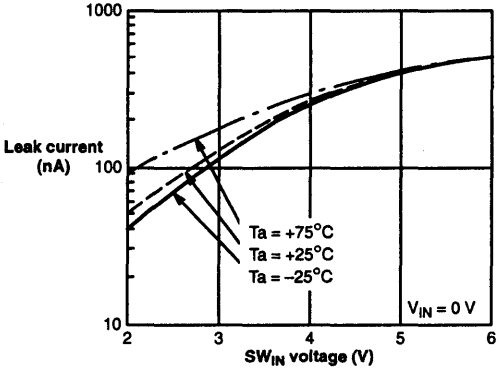
Discharge Resistance (DCG voltage dependence: SW_{OUT} = 3 V)



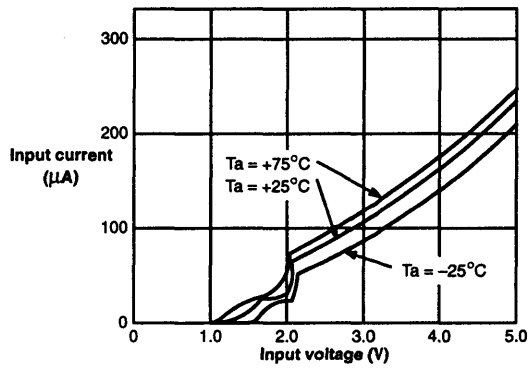
Discharge Resistance (DCG voltage dependence: SW_{OUT} = 5 V)



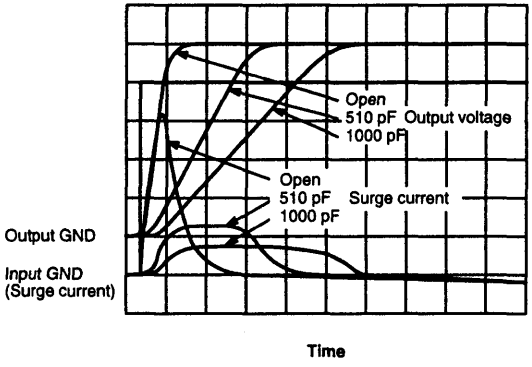
Output Leak Current (at Switch–OFF)



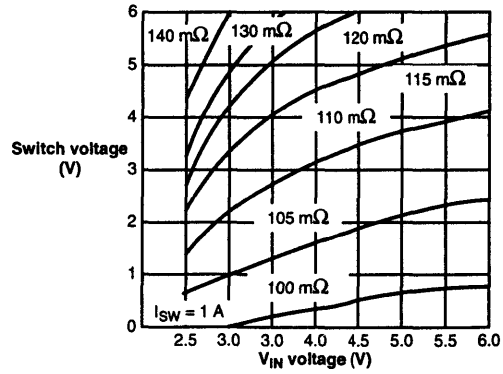
Input Current (Input voltage dependence)



Surge Current and Output Voltage Boot (DLY-pin connection capacitance dependence)



Switch-On resistance (relationship between V_{IN} and V_S)

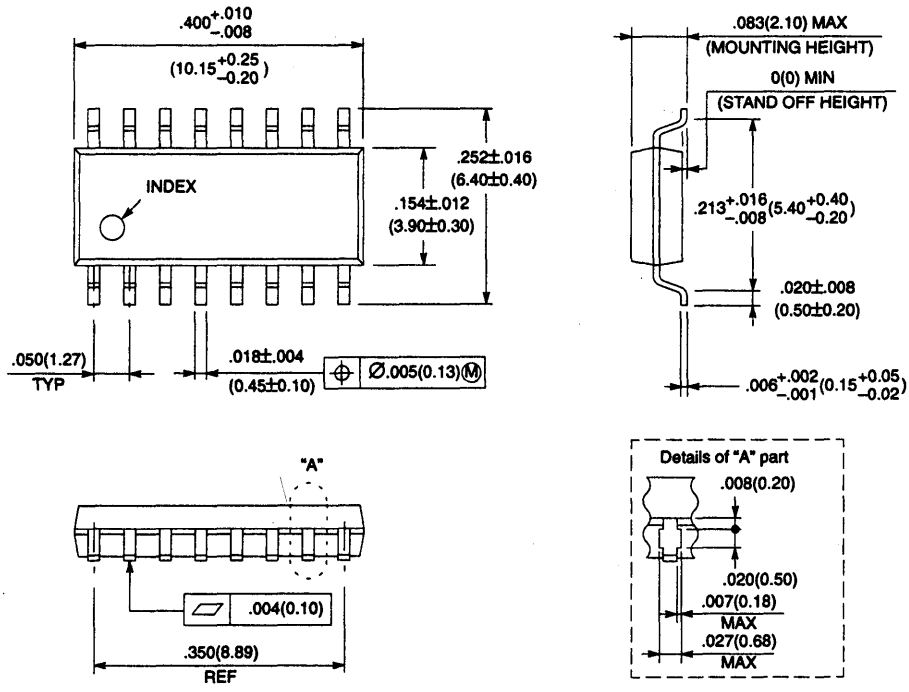


V_{IN} = 0 –> 5 V
SW_{IN} = 5 V
Load capacitance = 47 μF

V: 200 mA/div. (surge current)
V: 1.0 V/div. (output voltage)
H: 200 μS/div. (time axis)

8

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M04)



Dimensions in inches (millimeters)

DS04-27602-1E

DATA SHEET

FUJITSU

MB3807A *ASSP Power Supply* BIPOLAR *Power Management Switching IC*

(with flash memory power switching function)

■ DESCRIPTION

When data is written to or read from flash memory, it requires that the voltage at its power supply (V_{PP}) be switched (to 12 V for writing and to 3.3 or 5.0 V for reading).

The MB3807A is a power management switching IC, designed to be compatible with the PCMCIA digital controller, to switch the V_{PP} voltage of flash memory.

When the switch is turned on, optimum voltage is applied to the gate of the internal charge pump N-ch MOS switch, providing a constant amount of ON resistance. The ON resistance is also kept to be low to reduce voltage drop at the V_{PP} pin that is caused by large current flowing when data is written.

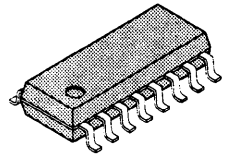
In addition, the OFF time is much shorter than the ON time to prevent short-circuiting between the reading and writing power supplies when the device switches the V_{PP} voltage for reading or writing data (break-before-make operation).

■ FEATURES

- Switching at low ON resistance
  For writing data: SWIN1 = 12 V, Ron = 0.3 Ω
  For reading data: SWIN2 = 5 V, Ron = 6.0 Ω
  SWIN2 = 3.3 V, Ron = 8.5 Ω
- Wide range of supply voltages: Vcc = 2.7 to 5.5 V
- Prevention of reverse current from the load at switch-off time
- ON time controllable with external pin
- Break-before-make operation

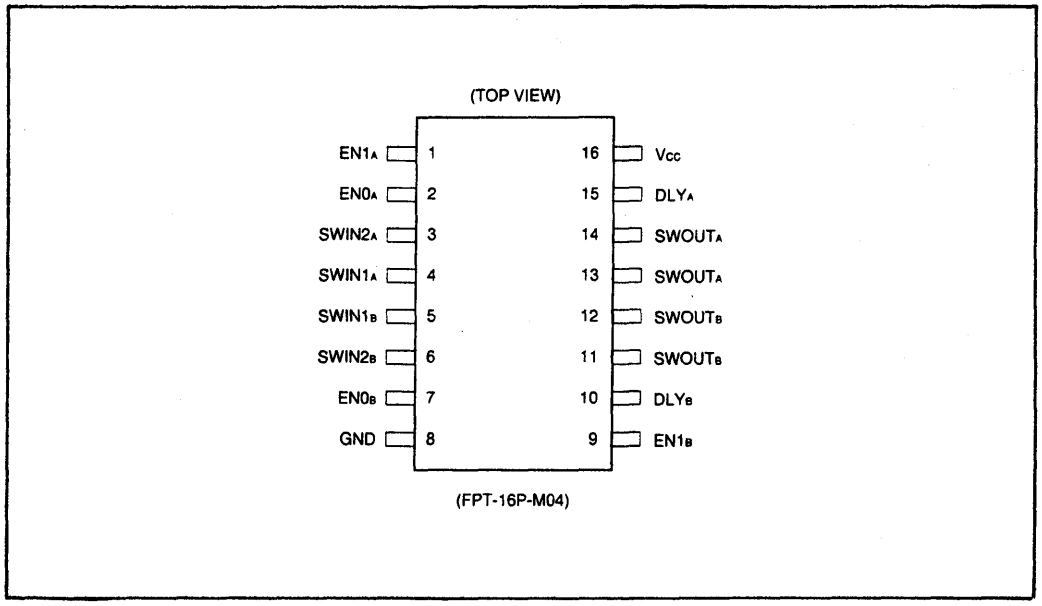
■ PACKAGE

16 pin Plastic SOP



(FPT-16P-M04)

■ PIN ASSIGNMENT



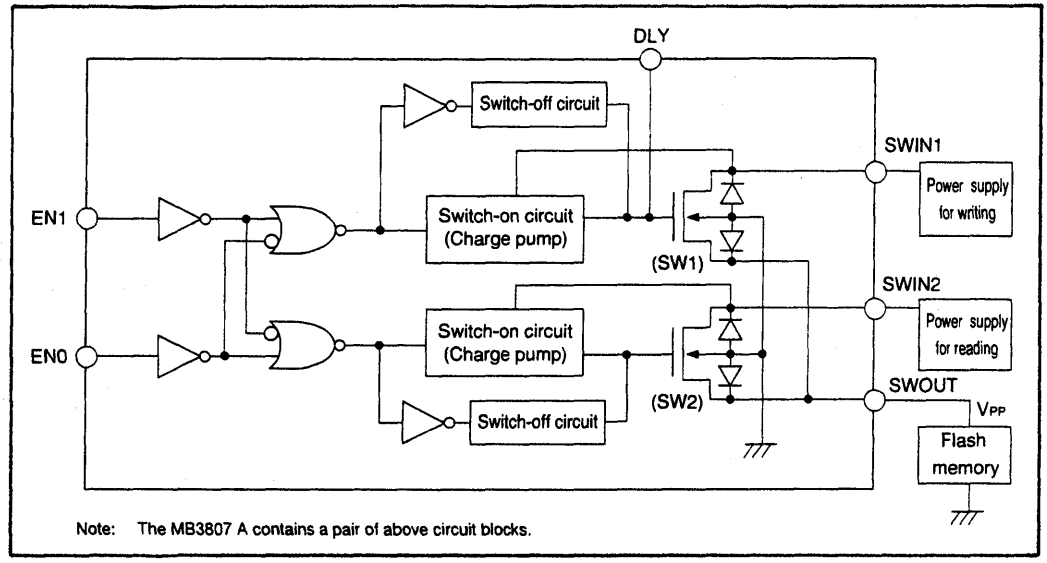
■ LOGICAL OPERATION TABLE

EN1	EN0	SW1	SW2
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	OFF	OFF

■ PIN DESCRIPTION

Pin No.	Pin name	Function
1	$EN1_A$	These pins turn the corresponding switches on and off depending on the PCMCIA compatible signals, as shown in "LOGICAL OPERATION TABLE."
9	$EN1_B$	
2	$EN0_A$	
7	$EN0_B$	
4	$SWIN1_A$	These pins connect the 12-V power supply for writing data to flash memory. When the SW1 is turned on, the voltage at the SWIN1 pin is output to the SWOUT pin. These pins also serve as power supply pins for the charge pump on the SW1 side. For switching, the pins require a voltage higher than V_{CC}.
5	$SWIN1_B$	
3	$SWIN2_A$	These pins connect the 3.3/5.0-V power supply for reading data from flash memory. When the SW2 is on, the voltage at the SWIN2 pin is output to the SWOUT pin. These pins also serve as power supply pins for the charge pump on the SW2 side. For switching, the pins require a voltage higher than V_{CC}.
6	$SWIN2_B$	
13, 14	$SWOUT_A$	These pins are output pins of the switch. A pair of two pins are used commonly as either $SWOUT_A$ or $SWOUT_B$ pins. These pins are connected to the V_{PP} pin of the flash memory.
11, 12	$SWOUT_B$	
15	DLY_A	These pins control the switch ON time. The ON time is controllable using an external capacitor. Leave these pins open when not in use. Note that a voltage of about 25 V is generated when the pins are open. Since high impedance is required, be careful when mounting the device not to generate current leakage.
10	DLY_B	
16	V_{CC}	Power supply pin
8	GND	Ground pin

■ BLOCK DIAGRAM



Note: The MB3807 A contains a pair of above circuit blocks.

■ BLOCK DESCRIPTION

The SWIN1 and SWIN2 pins are connected to the 12-V and 3.5/5.0-V power supplies, respectively. The SWOUT pin is connected to the V_{PP} power supply pin of the flash memory.

When conditions, EN1 = "H" and EN0 = "L" are established in an attempt to write data to flash memory, the switch-on circuit (charge pump) on the SW1 side is activated.

The charge pump applies optimum voltage to the SW1 gate to turn the switch on, causing the SWOUT pin to supply 12-V power from the SWIN1 pin to the V_{PP} pin of the flash memory. On the SW2 side, the switch-off circuit discharges the SW2 gate voltage to the GND to turn the switch off.

Reading data from flash memory assume the conditions EN1 = "L" and EN0 = "H." When the conditions are established, the switch-on circuit (charge pump) on the SW2 side and the switch-off circuit on the SW1 side are activated to cause the SWOUT pin to supply 3.3/5.0-V power from the SWIN2 pin to the V_{PP} pin of the flash memory.

Since the switch-on circuits are powered from the SWIN1 and SWIN2 pins, 80 to 350 μA current flows from the SWIN1 and SWIN2 pins to the GND when the switch is turned on.

The back gate of the N-channel MOS is connected to the GND. This prevents reverse current from flowing at switch-off time, regardless of the high potential of SWIN1 or SWIN2 pin and the SWOUT pin.

The DLY pin is an external capacitance connector to delay turning the switch on. Controlling the switch ON time minimizes surge current flowing to the capacitor connected to the load when the switch is turned on.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings		Unit
			Min.	Max.	
Input voltage	V_{IN}	—	–0.3	7	V
Switching voltage	V_{SWIN1}	—	–0.3	18	V
	V_{SWIN2}	—	–0.3	18	V
Switching current	I_{SWIN1}	Switch-on peak	—	1.5	A
	I_{SWIN2}		—	0.3	A
Permissible loss	P_D	Ta ≤ + 75°C	—	290	mW
Storage temperature	Tstg	—	–55	+125	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Values		Unit
			Min.	Min.	
Supply voltage	V_{CC}	—	2.7	5.5	V
High-level input voltage	V_{IH}	—	$V_{CC} \times 0.8$	V_{CC}	V
Low-level input voltage	V_{IL}	—	0	$V_{CC} \times 0.2$	V
Switching voltage	V_{SWIN1}	—	V_{CC}	15.0	V
		Switch OFF state	0	15.0	V
	V_{SWIN2}	—	V_{CC}	6.0	V
		Switch OFF state	0	6.0	V
Switching current	I_{SWIN1}	Switch ON state	—	500	mA
	I_{SWIN2}	Switch ON state	—	100	mA
DLY pin capacitance for connection	C_{DLY}	—	—	10	nF
DLY pin leakage current	I_{DLY}	—	–0.1	0.1	μA
Operating temperature	Top	—	–40	+75	°C

8

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Ta = −40°C to +75°C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typical*1	Max.	
Switch resistance (SW1)	R_{ON1}	V_{SWIN1} = 12 V, I_{SWIN1} = 500 mA V_{CC} = 3 V, 5 V, Ta = +25°C	—	300	450	mΩ
Switch resistance (SW2)	R_{ON2}	V_{SWIN2} = 3 to 5 V, I_{SWIN2} = 100 mA V_{CC} = 3 V2, 5 V, Ta = +25°C	—	6	10	Ω
Switch resistance	R_{ONT1}	V_{SWIN1} = 12 V, I_{SWIN1} = 500 mA V_{CC} = 3 V, 5 V	—	—	610	mΩ
	R_{ONT2}	V_{SWIN2} = 3 to 5 V, I_{SWIN2} = 100 mA V_{CC} = 3 V, 5 V	—	—	14	Ω
High-level input current	I_{IH}	V_{CC} = 5.5 V, V_{IH} = 5.5 V	—	0	10	μA
Low-level input current	I_{IL}	V_{CC} = 5.5 V, V_{IL} = 0 V	−10	0	—	μA
Switch-off leakage current	I_{L1}	EN0 = 0 V, EN1 = 0 V or EN0 = 3 V, EN1 = 3 V V_{SWIN1} = 15 V, V_{CC} = 3 V	—	0	10	μA
	I_{L2}	EN0 = 0 V, EN1 = 0 V or EN0 = 3 V, EN1 = 3 V V_{SWIN2} = 6 V, V_{CC} = 3 V	—	0	10	μA
Charge pump driving current*2	I_{SWON1}	EN0 = 0 V, EN1 = 5 V V_{CC} = 5 V, V_{SWIN1} = 12 V	175	350	700	μA
	I_{SWON2}	EN0 = 5 V, EN1 = 0 V V_{CC} = 5 V, V_{SWIN2} = 5 V	30	80	200	μA
DLY output voltage	V_{DLY}	V_{CC} = 5 V, V_{SWIN2} = 12 V	—	24	35	V
Supply current	I_{CC}	EN0 = 5 V, EN1 = 0 V or EN0 = 5 V, EN1 = 0 V V_{CC} = 5 V	50	100	300	μA

*1: Typical values assume V_{CC} = TYP, Ta = +25°C.
*2: The charge pump driving current flows from SWIN to GND when the switch is turned on.

2. AC Characteristics

(Ta = −40°C to +75°C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typical	Max.	
ON time	t_{ON1}	V_{SWIN1} = 12 V, R = 24 Ω, V_{CC} = 5 V	30	60	140	µs
	t_{ON2}	V_{SWIN1} = 12 V, R = 24 Ω, V_{CC} = 3 V	30	60	140	µs
	t_{ON3}	V_{SWIN2} = 5 V, R = 50 Ω, V_{CC} = 5 V	40	90	200	µs
	t_{ON4}	V_{SWIN2} = 3 V, R = 30 Ω, V_{CC} = 3 V	200	400	1200	µs
OFF time	t_{OFF1}	V_{SWIN1} = 12 V, R = 24 Ω, V_{CC} = 5 V	10	30	60	µs
	t_{OFF2}	V_{SWIN1} = 12 V, R = 24 Ω, V_{CC} = 3 V	10	40	70	µs
	t_{OFF3}	V_{SWIN2} = 5 V, R = 50 Ω, V_{CC} = 5 V	1	7	20	µs
	t_{OFF4}	V_{SWIN2} = 3 V, R = 30 Ω, V_{CC} = 3 V	1	7	20	µs
ON/OFF time difference	t_{HYS1}	—	29	53	130	µs
	t_{HYS2}	—	29	53	130	µs
	t_{HYS3}	—	30	60	190	µs
	t_{HYS4}	—	190	360	12000	µs

Note: ON/OFF time difference: $t_{HYS1} = t_{ON1} - t_{OFF3}$

$t_{HYS2} = t_{ON2} - t_{OFF4}$

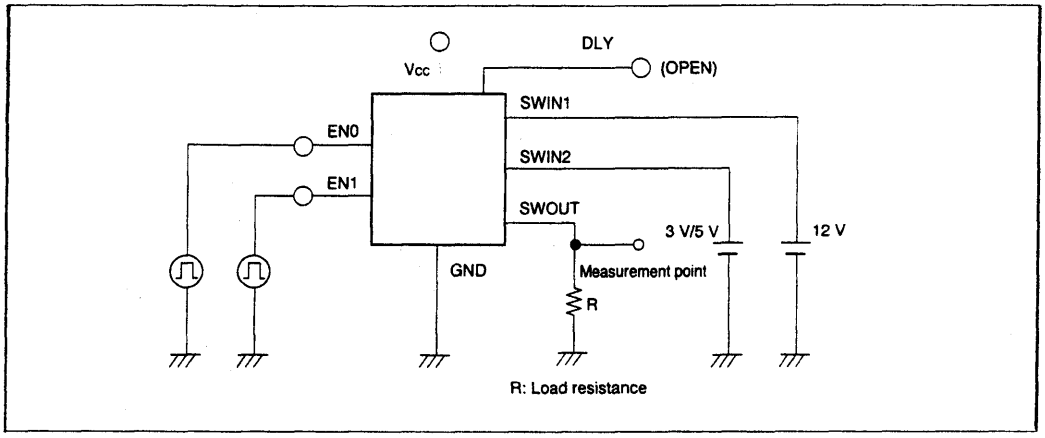
$t_{HYS3} = t_{ON3} - t_{OFF1}$

$t_{HYS4} = t_{ON4} - t_{OFF2}$

8

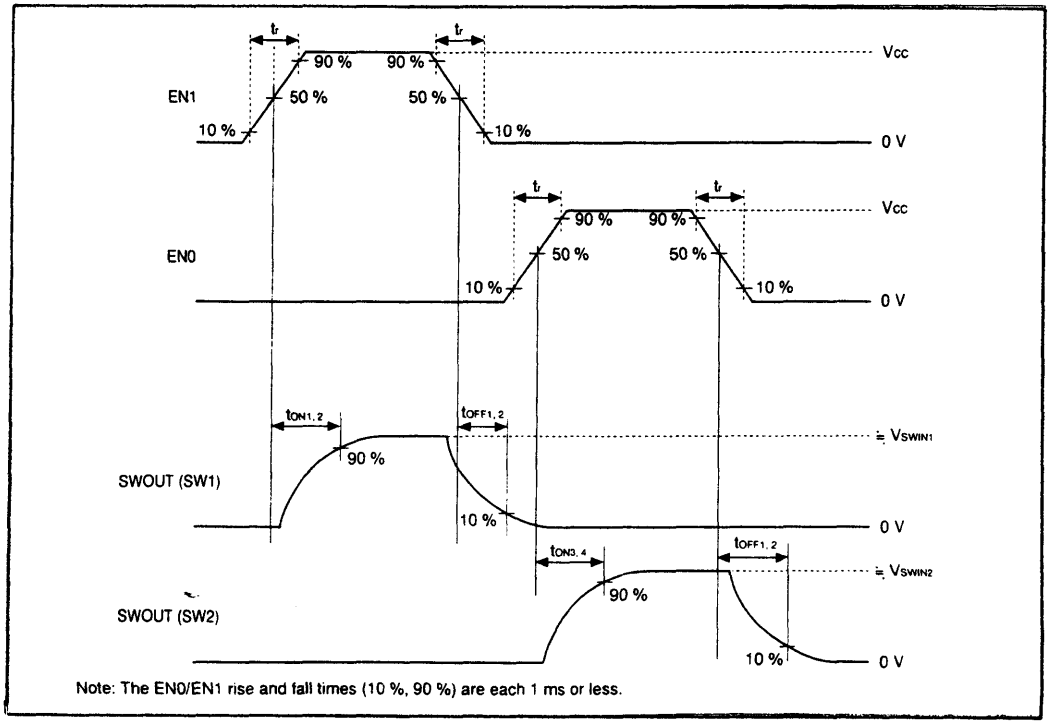
■ AC SPECIFICATION TEST DIAGRAM

- **Measurement Conditions**



■ TIMING DIAGRAM

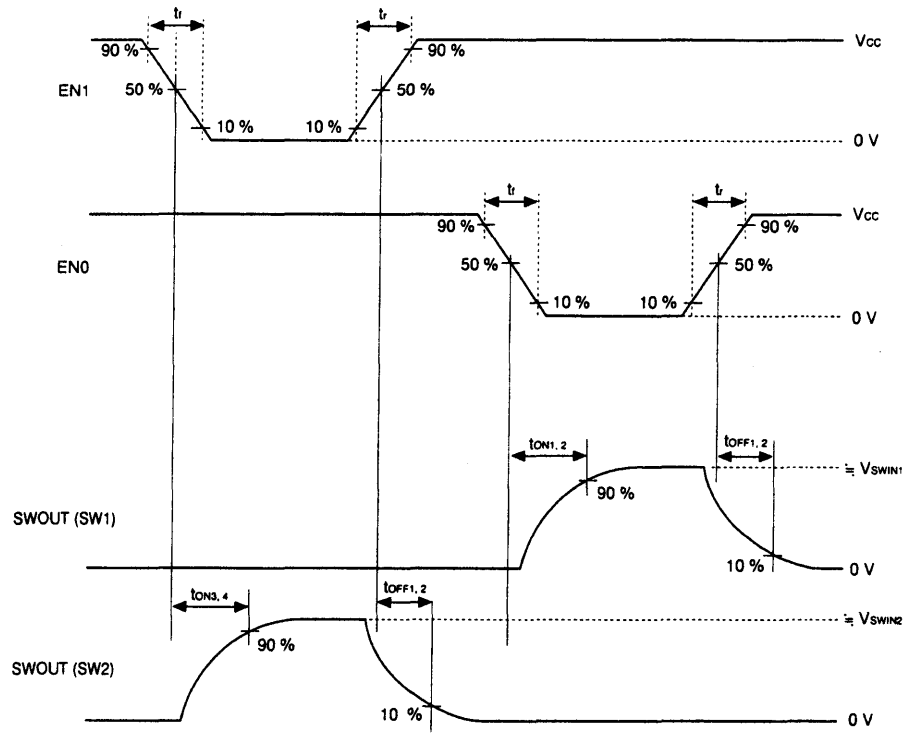
- **ON-time and OFF-time Waveforms**



Note: The EN0/EN1 rise and fall times (10 %, 90 %) are each 1 ms or less.

(Continued)

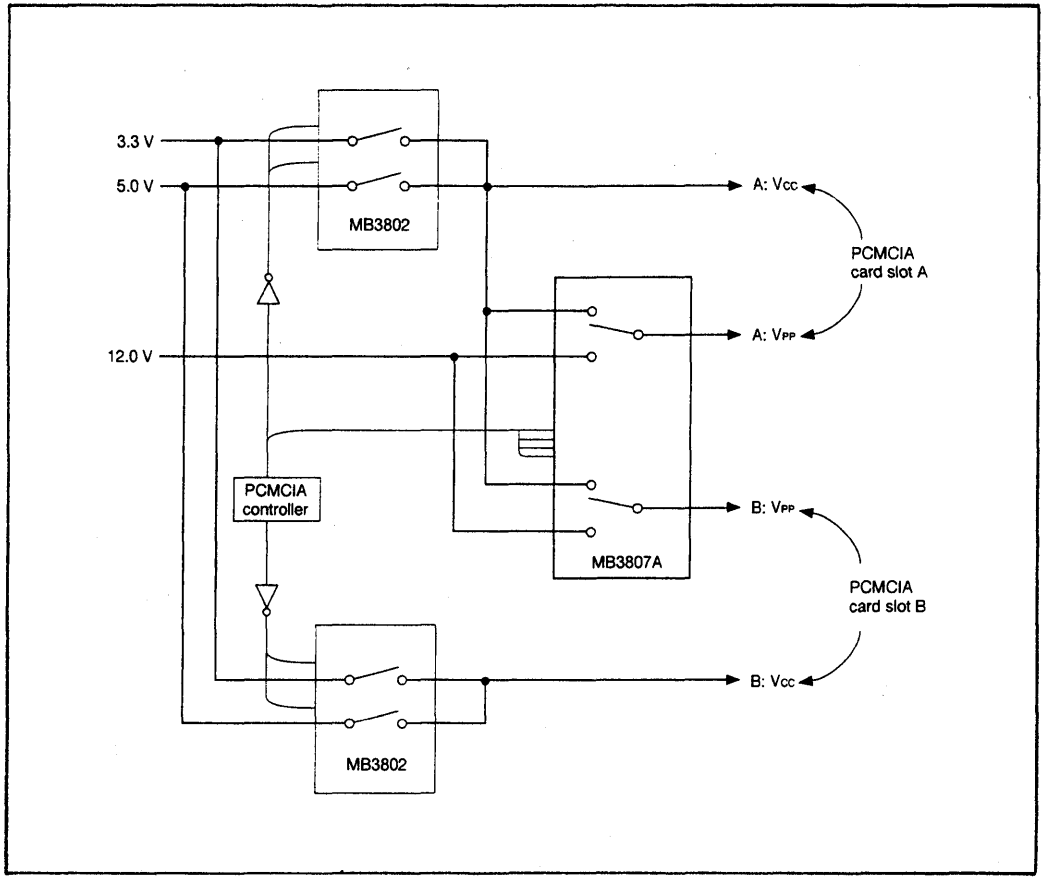
(Continued)



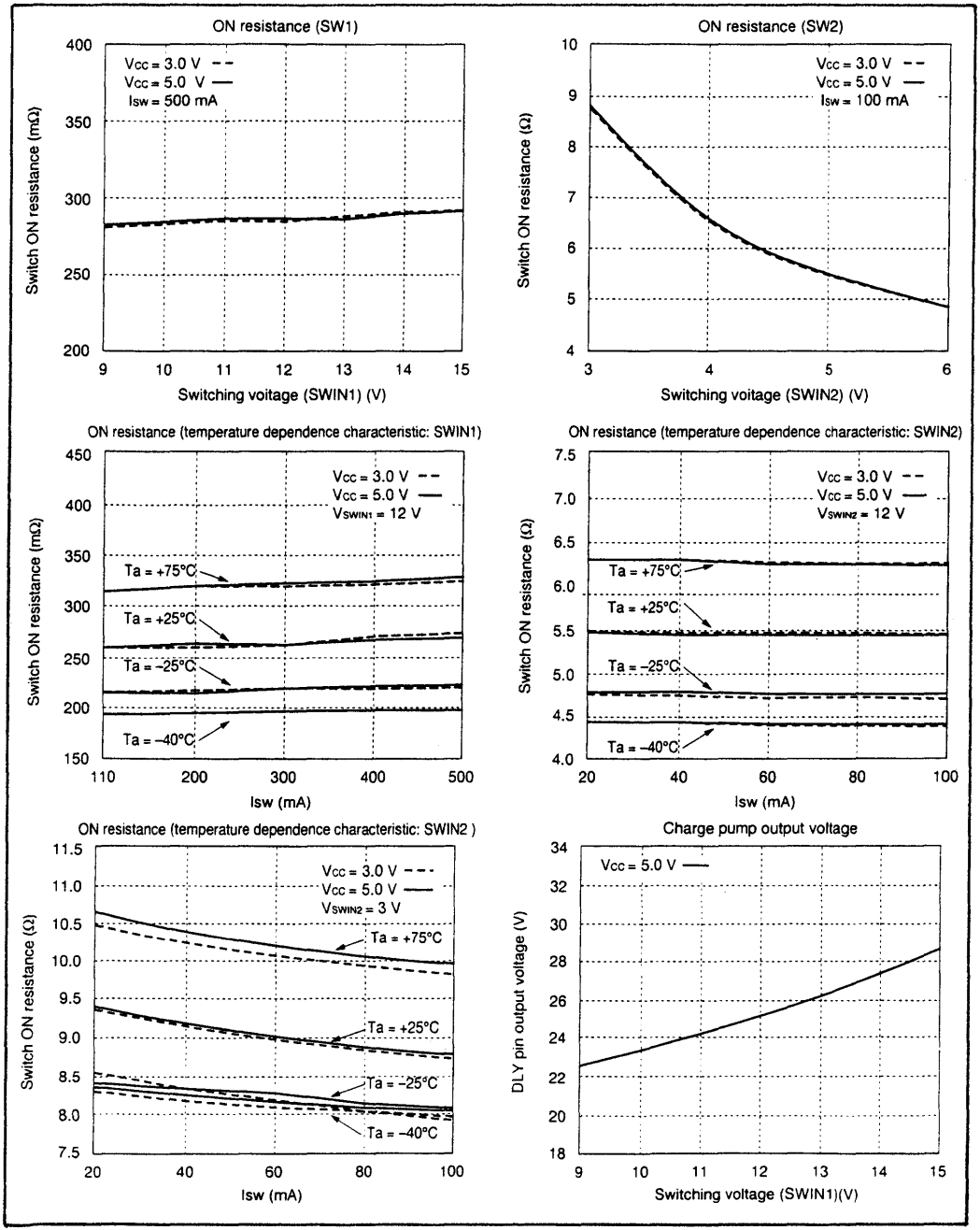
Note: The EN0/EN1 rise and fall times (10 %, 90 %) are each 1 ms or less

8

■ APPLICATION



■ TYPICAL CHARACTERISTIC CURVES



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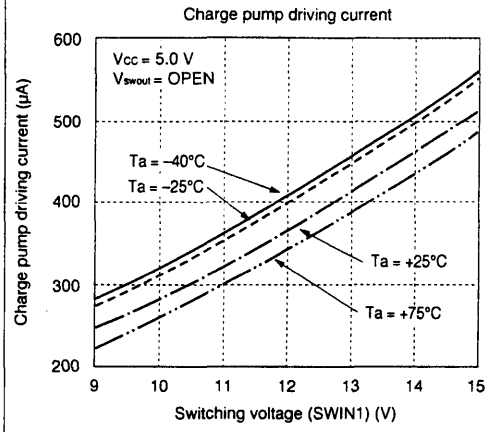
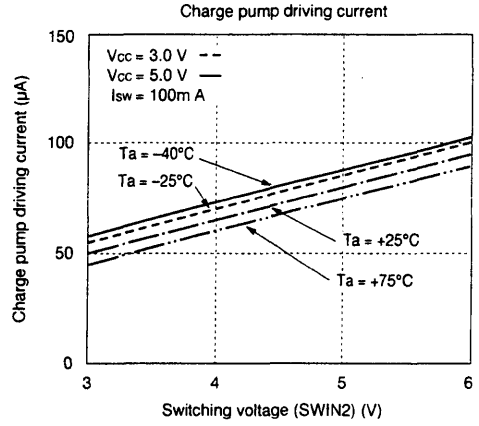
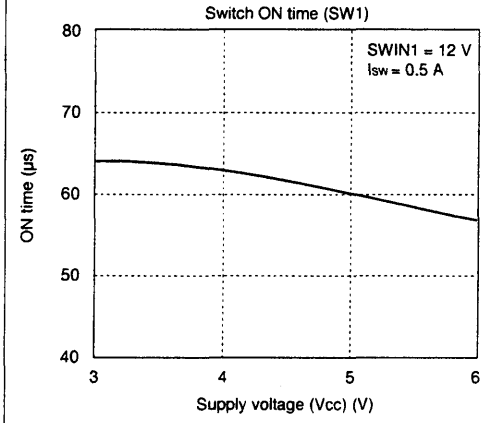
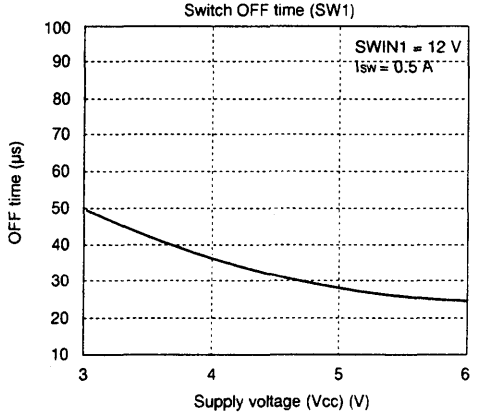
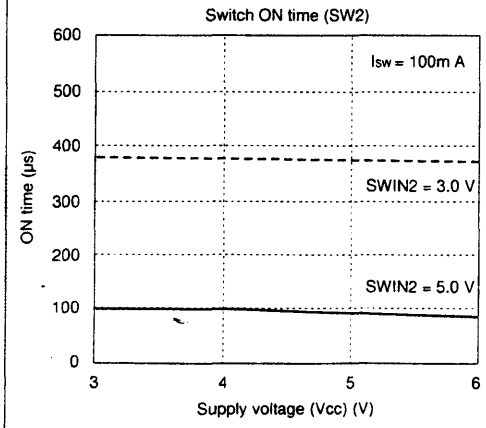
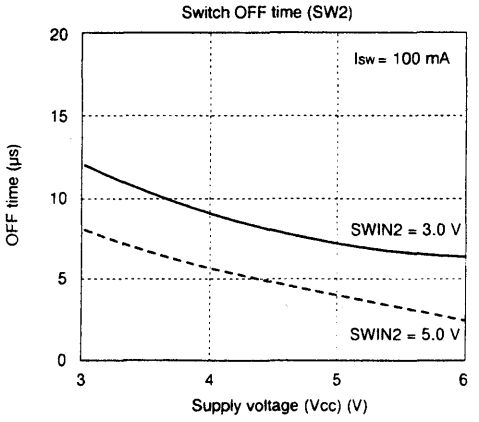

Charge pump driving current
Vcc = 5.0 V
Vswout = OPEN
Ta = −40°C
Ta = −25°C
Ta = +25°C
Ta = +75°C
Charge pump driving current (µA)
600
500
400
300
200
9
10
11
12
13
14
15
Switching voltage (SWIN1) (V)


Charge pump driving current
Vcc = 3.0 V
Vcc = 5.0 V
Isw = 100m A
Ta = −40°C
Ta = −25°C
Ta = +25°C
Ta = +75°C
Charge pump driving current (µA)
150
100
50
0
3
4
5
6
Switching voltage (SWIN2) (V)


Switch ON time (SW1)
SWIN1 = 12 V
Isw = 0.5 A
ON time (µs)
80
70
60
50
40
3
4
5
6
Supply voltage (Vcc) (V)


Switch OFF time (SW1)
SWIN1 = 12 V
Isw = 0.5 A
OFF time (µs)
100
90
80
70
60
50
40
30
20
10
3
4
5
6
Supply voltage (Vcc) (V)


Switch ON time (SW2)
Isw = 100m A
SWIN2 = 3.0 V
SWIN2 = 5.0 V
ON time (µs)
600
500
400
300
200
100
0
3
4
5
6
Supply voltage (Vcc) (V)

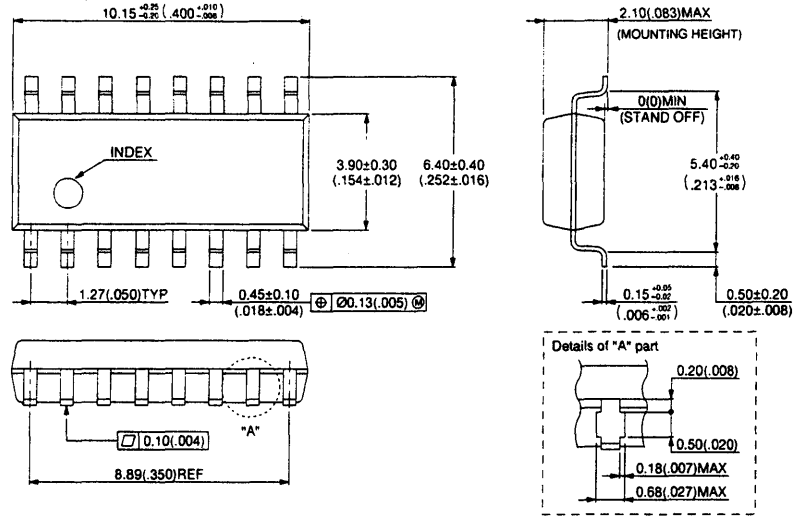

Switch OFF time (SW2)
Isw = 100 mA
SWIN2 = 3.0 V
SWIN2 = 5.0 V
OFF time (µs)
20
15
10
5
0
3
4
5
6
Supply voltage (Vcc) (V)

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3807APF	16 pin Plastic SOP (FPT-16P-M04)	

■ PACKAGE DIMENSION

16 pin Plastic SOP
(FPT-16P-M04)



Dimensions in mm (inches)

SECTION 9

Application Notes and Articles – *At a Glance*

Application Notes

Technical Articles

March 1991
Edition 2.0

FUJITSU

APPLICATION NOTE

Prescalers and PLLs

Fujitsu Prescalers and Phase-Locked Loops for VHF and UHF Frequency Synthesis

A Tutorial with Selection Guides

Fujitsu Microelectronics, Inc.
Field Applications Engineering

Abstract

This Application Note includes a broad introduction to the relevant high frequency synthesis theory and its application areas, a description of prescaler and phase-locked loop (PLL) components, and guidelines for selecting and designing with Fujitsu's extensive selection of prescaler and PLL IC products.

This document is published by the Publications Department, Fujitsu Microelectronics, Inc.,
3545 North First Street, San Jose, California, U.S.A. 95134–1804; U.S.A.

Printed in the U.S.A.

Edition 1.1

Contents

Contents (Continued)

Illustrations

Figures **Page**

Tables **Page**

Introduction

Phase-locked loops (PLLs) and prescalers are used for synthesizing and controlling frequencies in a multitude of high frequency systems. These systems range from radio and television broadcasting, cellular phones, computer local area networks (LANs), and measurement instrumentation to satellite and microwave systems.

Dedicated PLL integrated circuits (ICs) are manufactured in CMOS technology and typically operate in the 20-30 MHz range (maximum). Prescalers manufactured in bipolar ECL or GaAs technologies are considered interface ICs that allow the relatively slower PLLs to accurately control and select frequencies well into the microwave range (>1 GHz).

Fujitsu manufactures a broad range of high frequency telecommunication ICs that includes prescalers, PLLs, integrated PLLs, as well as microcontrollers with onboard PLL and prescaler circuits.

PLL Tuning Systems

Tuning of telecommunication senders and receivers is, by far, the largest application area for today's PLLs and prescalers. High frequency PLLs have largely replaced older methods such as direct tuning an RC or LC oscillator to the desired local oscillator frequency.

At the expense of a quantized (instead of a continuous frequency) resolution, PLLs and the so-called digital tuning circuits into which they are incorporated provide a cheaper, faster, more compact and reliable solution to tuning circuitry. The fact that PLLs only allow selection of frequencies in discrete steps, rather than over a continuous range, is not a concern because the available frequencies (for airwaves, long distance telephone cables, satellites, microwave links, ISDN etc.) are heavily regulated and limited to preassigned channel frequencies.

The frequency position and spacing between channels depends on the physical carrier medium and the program material involved. For example, U.S. airwaves regulations of the Federal Communications Commission (FCC) specify that:

AM radio must be broadcast at 530, 540, 550 to 1610, or 1620 kHz

FM radio must be broadcast at 87.9, 88.1 to 107.7, 107.9 MHz

TV (channels 2–69) must be broadcast at 55.25, 61.25, 67.25, 77.25, 83.25 to 795.25, 801.25 MHz.

These frequencies represent the center frequencies of each channel. The spacing of 10 KHz between assigned AM channels, 200 kHz between assigned FM channels, and 6 MHz between assigned TV channels reflects the progressively higher bandwidths necessary for FM and TV.

Other regulated frequencies worth mentioning within the VHF (30 - 300 MHz) and UHF (300 MHz – 3 GHz) bands include: 46/49 MHz for cordless telephones, 800-900 MHz for cellular phones (also known as land mobile radio services), 0.1-1.5 GHz for cable TV and >2 GHz for emerging Digital TV standards and Integrated Services Digital Network (ISDN). Fujitsu prescalers and PLL ICs are appropriate for most of these applications.

Figure 1 shows a superheterodyne FM broadcast receiver and some of the involved spectra and frequencies. For an example, let us examine the steps involved in tuning to the FM station at 88.1 MHz.

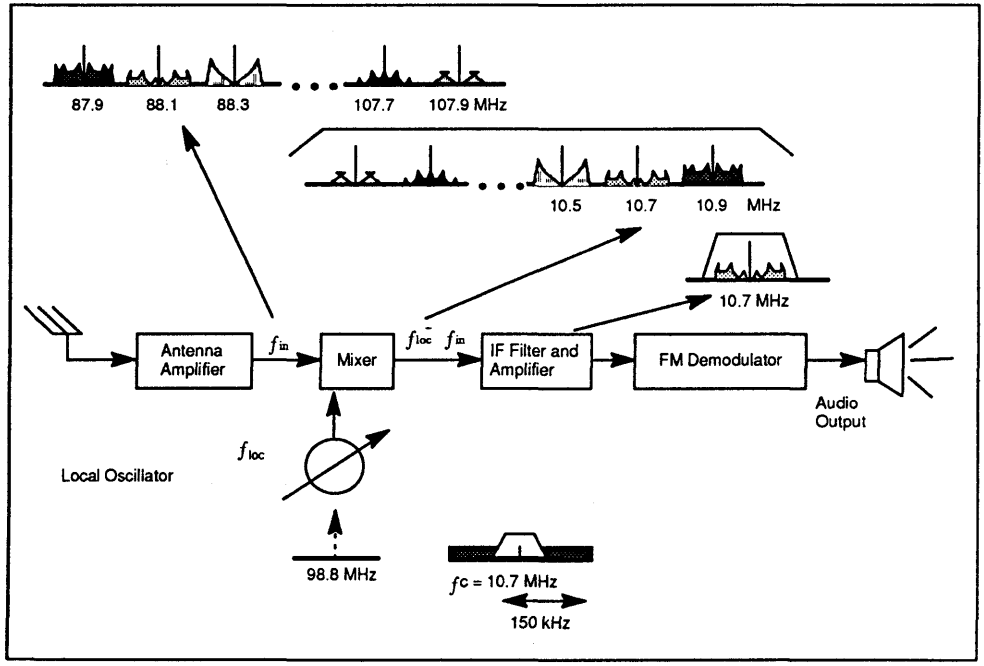


Figure 1. A Typical Heterodyne FM Receiver Tuned to the 88.1 MHz Signal

The antenna is exposed to a multitude of transmission frequencies. In order to retrieve the desired signal, several stages of amplification and progressive selective filtration must be applied. In FM broadcasting each radio station is allowed to use up to 150 kHz around the assigned center frequency. Since the spacing

between the assigned channels is 200 kHz, this leaves a 50-kHz wide isolation gap between the stations to avoid a spectral overlap. Thus, a 150-kHz wide filter can be used in the final stage to isolate the desired station from all the others. Accurate tuning of such a narrow filter over the 20-MHz wide FM frequency range is not an easy task. To achieve accurate tuning, the filter is kept at a constant frequency, the so-called Intermediate Frequency (IF), and the desired radio signal is shifted in frequency to fall exactly within the filter passband. 10.7 MHz is the broadly used value for IF in commercial FM tuners.

The antenna signal is converted to a lower frequency by mixing (or heterodyning) with an appropriately chosen local oscillator frequency f_{loc}. A PLL is employed for synthesizing f_{loc}. In order to place the desired radio station (originally located at f_{in}) exactly at the center of the IF bandpass filter, the PLL frequency f_{loc} must be set so that IF = $f_{loc} - f_{in}$. In other words, to tune to the 88.1 MHz signal, a f_{loc} of 88.1+10.7 MHz = 98.8 MHz is necessary. Tuning to another signal is accomplished by selecting a different f_{loc}.

An appropriate FM demodulator working at the IF provides the final restoration of the original signal.

On the sender side (see Figure 2) the sequence is reversed: a modulated IF signal is mixed with the local frequency oscillator up to the appropriate channel-frequency and broadcast.

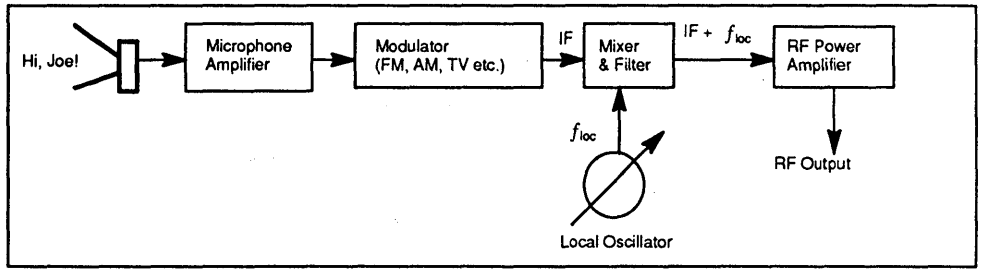


Figure 2. A Typical Heterodyne (Audio) Sender

Near-ideal PSK, PM, or FM demodulators can be implemented with PLLs as well as local oscillators.

What is a PLL?

A PLL is a control loop consisting of a phase detector (PD), low pass filter (LPF), voltage controlled oscillator (VCO), program counter(s), and, as necessary, single- or dual-modulus prescalers. (See Figure 3.)

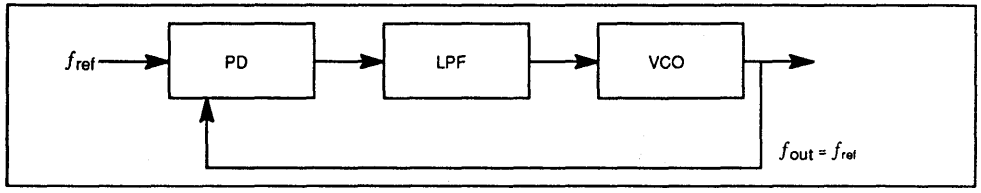


Figure 3. A Basic PLL Configuration

The output of the PD is a voltage indicating the phase difference between its two inputs.

The LPF smooths the PD output and determines the dynamic performance of the loop. The dynamic performance includes general servo loop issues, such as the capture and lock ranges, the noise suppression bandwidth and the transient response.

When the loop is out of lock, the PD voltage changes the frequency of the VCO in a direction that reduces the phase difference between the input signal and the local oscillator signal. When the loop is locked, the signals at both inputs are in phase and have the same frequency.

Generally speaking, the output of the VCO is considered the desired PLL output. It should be mentioned, however, that in some instances (such as when a PLL is used as an FM de-modulator), the filtered output of the PD, rather than the output of the VCO, can be viewed as the system output.

The bandwidth of the low-pass loop filter is crucial to the dynamic- and noise-filtering performance of the loop. The two performance requirements are conflicting, since faster lock-up times require wider LP filters while better noise characteristics are achieved with narrower filters. Therefore, a reasonable compromise has to be met for each application.

Narrow filter bandwidths provide long-loop averaging times and are useful in applications where a noisy, intermittent, or varying reference source must be cleaned up.

For example, in digital LANs, a PLL is used to regenerate a local clock rate from frame synchronization bits, which appear intermittently on most asynchronous communications networks.

In a similar way, the "flywheel synchronizers" for vertical and horizontal scan in today's TV receivers, are operated using PLL circuits. In both cases the "slow" lowpass filter maintains a relatively constant VCO frequency between occurrences of synchronization patterns on the input.

In frequency synthesis applications, the reference frequency source will typically be a high quality, relatively noise-free, crystal oscillator. The loop filter can be extensively wide to provide for fast switching times without compromising noise performance.

A novel approach to PLL design is to electronically bypass the loop filter during the bulk of a frequency switching period and then to activate it back into the loop for final lock-in.

As previously mentioned, the loop filter is the single most important factor in determining the dynamic performance of the servo loop. A thorough theoretical treatment of servo loop analysis is beyond the scope of this publication. References 1 through 4 listed in the back of this note are recommended for more in-depth information.

Frequency Synthesis With PLLs and Prescalers

Figure 4 shows a simple frequency-synthesizing configuration employing a PLL and a single program counter.

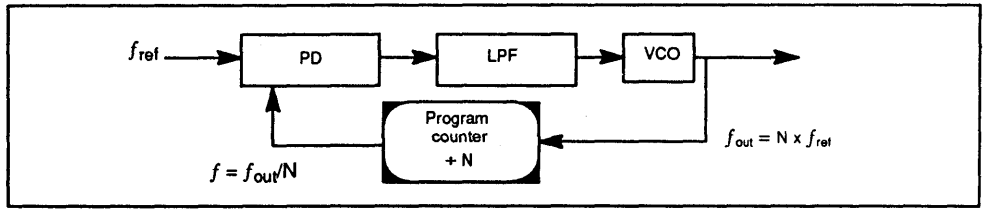


Figure 4. Frequency Synthesis with a Programmable Counter

When the loop is in lock, the two input frequencies of the PD are equal, hence:

$$f_{ref} = f_o/N <=> f_o = N \bullet f_{ref}$$

A reprogramming of "*N*" by +1 or –1 will result in selection of a new output frequency with channel separation of f_{ref}.

The scheme of Figure 4, although attractive in its simplicity, is only applicable to output frequencies below 40 MHz, since higher VCO frequencies will exceed the program counter's toggling rate.

Figure 5 shows a widely used remedy to the high frequency problem: a *1/M* prescaler is inserted in the feedback loop as a buffer between the VCO and the program counter. This lowers the program counter's input frequency to f_{out}/M instead of f_{out}.

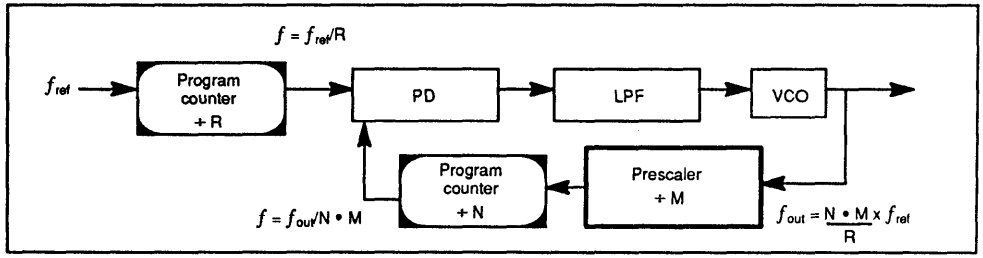


Figure 5. Prescaler Accommodating for a Slow Program Counter

Figure 5 also shows a reference frequency divider, 1/R, inserted in the reference frequency path to allow more flexibility in output frequency programming. Without the reference frequency divider, the presence of the prescaler would result in broadening the channel separation to $M \bullet f_{ref}$. A resolution of f_{ref} is maintained by setting *R* equal to *M*.

In many cases, the scheme of Figure 5 is a satisfactory solution, with one drawback. Compared to Figure 4, the operational frequency of the phase detector is lowered by the prescaling factor *M*. A lowered PD frequency necessitates use of a narrower low-pass filter to suppress spurious output signals from the phase detector at the comparison frequency and its harmonics. Especially in very high frequency synthesizers, where the divide ratio of the prescaler becomes substantial, the loop's lock-in and switching speed characteristics will be severely degraded as a result of narrowing the lowpass filter.

The Pulse Swallow Method

The widely used "multi-modulus division", also known as pulse swallowing (see Figure 6), offers a solution to previously mentioned problems. This method employs two programmable counters and a dual modulus prescaler inside the loop. (For simplicity the reference frequency divider is not shown.)

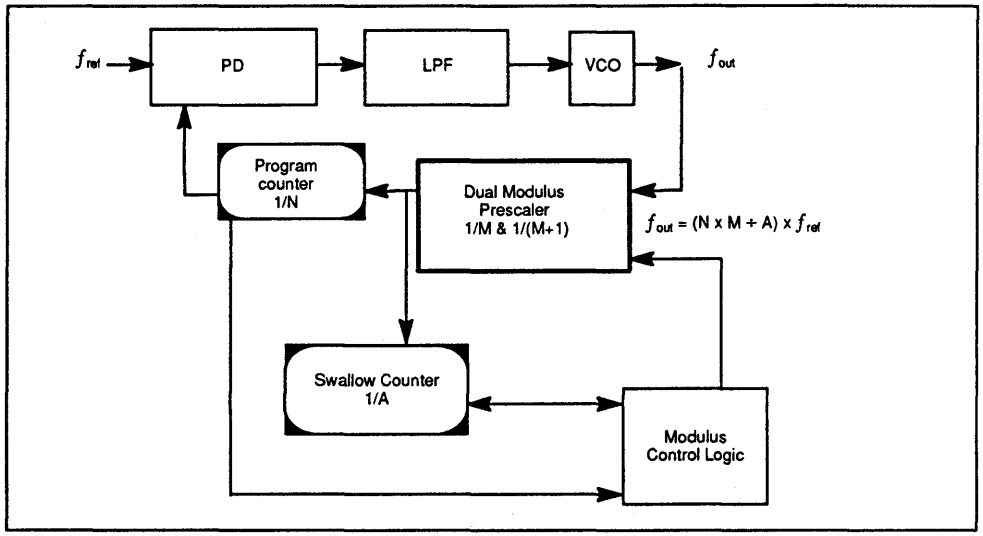


Figure 6. Pulse Swallow

A description of the pulse swallow method is as follows:

N must be larger than *A* (*N>A*). The dual modulus prescaler is initially set to divide by *M+1*. After *"A"* pulses out of the prescaler, the swallow counter is full and changes the prescaler modulus to *M*. After additional (*N-A*) pulses out of the prescaler, the program counter changes the prescaler modulus back to *M+1*, restarts the swallow counter and the cycle repeats.

In this way each cycle of the *1/N* counter is a result of:

$$A \bullet (M+1) + (N-A) \bullet M = N \bullet M+A$$

cycles of the f_{pit}.

In other words:

$$f_{out} = (N \bullet M + A) \bullet f_{ref}$$

Since *M* is multiplied by *N*, but not *A*, the frequency will change by f_{ref} when *A* is changed by *1*. In this way both the channel separation and the PD frequencies are maintained at f_{ref} to provide for an uncompromised loop performance.

As previously mentioned, more complex variations of the multi-modulus theme include: $N/N+Z$ prescalers (as in MB508 with 128/130, 256/258 and 512/514) and quad-modulus schemes involving multiple swallow counters and special prescalers.

Stand-alone PLLs and Integrated PLLs

Figure 7 shows a general purpose high frequency synthesizer and the functional blocks. These blocks are: the PD, the reference counter, the A and the N counters and modulus control logic. The MB87014, manufactured entirely in CMOS, includes an onboard 180 MHz prescaler.

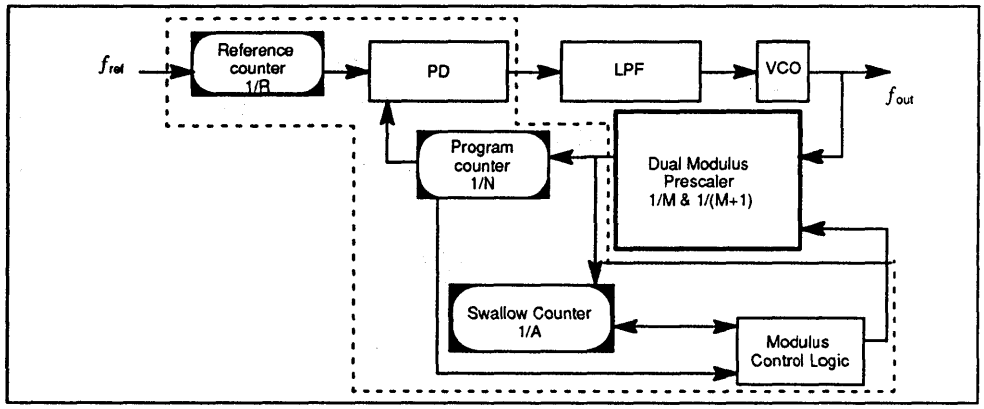


Figure 7. System Blocks

Advances in recent years in CMOS and BiCMOS (combined ECL and CMOS on one chip) have allowed integration of gigahertz prescalers on the same chip as the PLL. The architecture of these integrated PLL BiCMOS devices is illustrated in Figure 8.

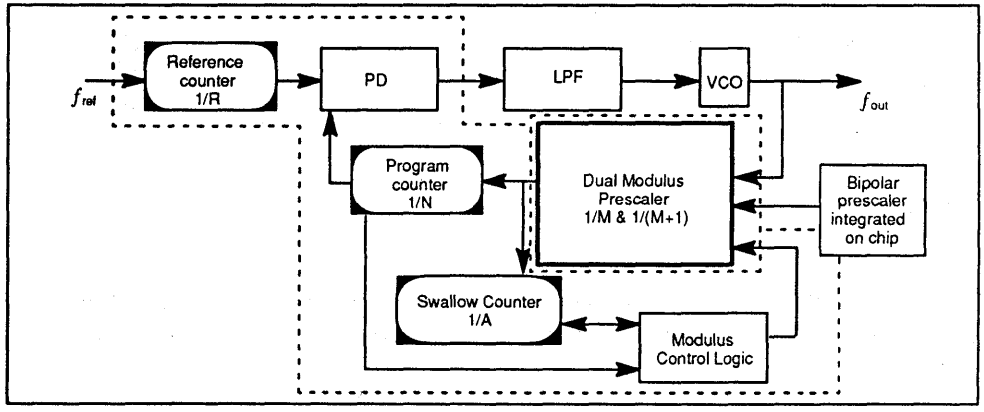


Figure 8. Fujitsu's Integrated PLL ICs

Before discussing the blocks on the PLL chip, let us briefly mention the circuits not found on it. As stated earlier, the low-pass filter must yield a good compromise between accommodating the desired noise and switching characteristics on one side and removing spurious components from the phase detector output on the other side. A charge pump output (see Figure 14) from the PLL is provided in most cases, allowing direct connection of an external passive RC

filter. The charge pump output is simply a very high impedance output ($Z_{out} \geq 400k\ \Omega$) well suited to drive high-Q resonant circuits found in the VCO. Optionally, an unbuffered PD output is often also made available for connection of custom external active filter configurations. Typical filter bandwidths for frequency synthesis are 1-10 kHz.

The prescaler and the VCO are the only two devices actually operating at the high output frequency f_{out}.

The VCO is frequently custom made for a specific application. Some popular oscillator types, in order of decreasing phase and frequency-stability, but increasing frequency coverage and linearity, are as follows:

- PLL IC with an on-chip inverter/buffer for an external reference frequency oscillator
- Voltage controlled crystal oscillator with varactor diode (also known as VCXO)
- LC oscillator with a varactor diode
- RC multivibrator

A list of crystal oscillator and VCXO manufacturers can be found in reference 11.

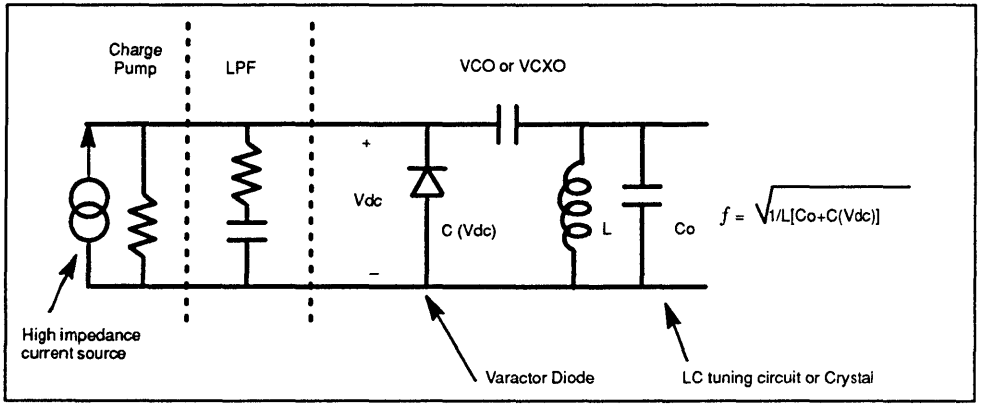


Figure 9. Varactor Diode in a VCO or a VCXO

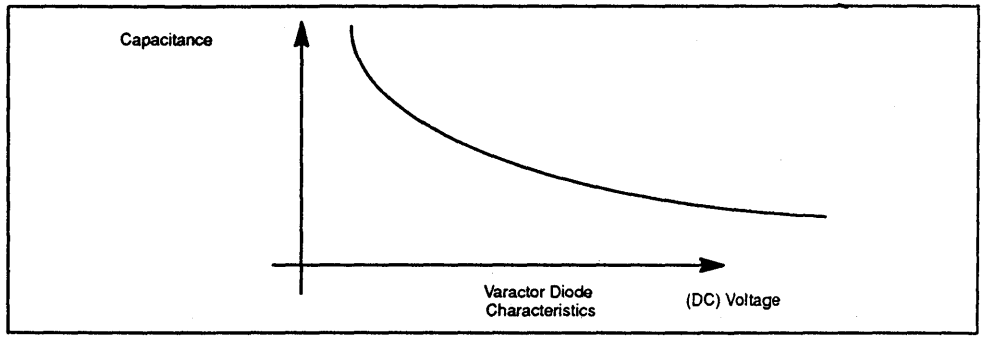


Figure 10. A Varactor Diode Acting as a Voltage-controlled Variable Capacitance

Selecting the Right PLL IC

Table 1 lists Fujitsu's family of CMOS PLL ICs and Table 2 lists the BiCMOS integrated PLL ICs.

Table 1. Fujitsu's Low Power CMOS PLLs

Please refer to the CMOS PLL's section.

Table 2. Fujitsu's Super PLLs

Please refer to the Super PLL's section.

Selecting A PLL

The specifications to consider when selecting a PLL are as follows:

Width of the counters

The most significant feature of the various PLL devices (since operating speed is practically the same for all), is the width of their counters. In general, the width (in bits) of the reference counter determines the frequency resolution ($\Delta f_{channel} = f_{ref}/R$) obtainable from the system. The width of the programmable counter, (*1/N*) (see Figure 7) and the swallow counter (*1/A*) determine the number of channels that can be covered. Fujitsu devices are available with up to 18-bit wide combined program and swallow counters, and 16-bit wide reference counters.

Selecting the N and A counters

It is easily observed from the dual-modulus equation [$f_{out} = (N \bullet M+A) \bullet \Delta f_{channel}$] that *A* need not assume values higher than the prescaler modulus *M*, since setting *A* equal to *M+X* is equivalent to setting *A* equal to *X* and increasing *N* by 1. Hence, all possible channels can be covered in a dual modulus configuration if the programmable swallow counter number (*A*) is allowed to assume all values from 0 to *M-1*, where *M* is the modulus of the *M/M+1* prescaler:

$$\bullet\ 0 \leq A \leq M-1$$

Under all circumstances the condition N≥A must be satisfied:

$$\bullet\ N_{min} = A_{max} = M\text{-}1.$$

To select the right PLL counters for your application, supply the information that is requested in the following guide.

PLL Counter Selection Guide

1. Identify maximum and minimum output frequency desired, $f_{out,\ max}$ and $f_{out,\ min}$.
2. Select a *M/M+1* prescaler, so that $f_{out,\ max}/M$ can be accommodated by the PLL (<20 MHz typically).
3. Identify desired channel spacing(s), $\Delta f_{channel}$.
4. Let $A = 0$, then $N_{min} = f_{out,\ min}/\Delta f_{channel}$ and $N_{max} = f_{out,\ max}/\Delta f_{channel}$.
5. Verify that $N_{min} \geq M\text{-}1$; if not, select a bigger prescaling modulus and go back to step 3.
6. Select an *N* program counter with enough bit-width to accommodate the value of N_{max}.
7. Select an *A* swallow counter with enough bit-width to accommodate the value *M-1*; set all higher bits to 0.
8. Select the reference frequency divider (*R*) and a crystal reference frequency so that $f_{ref}/R = \Delta f_{channel}$.

A Practical Example: Selecting the PLL IC for an FM Receiver

We are going to select the appropriate PLL IC and prescaler for the local oscillator of the superheterodyne FM receiver shown earlier in Figure 1. In order to receive an FM station at f_{in}, the local oscillator must be set to $f_{loc} = f_{in} + 10.7$ MHz. For receiving all FM stations, f_{loc} has to be selectable between 98.6 MHz and 118.6 MHz in 0.2 MHz steps; that is 101 positions in total.

To select a PLL for our example FM Receiver, we used the PLL Selection Guide, supplied the required information (see Example), and selected the appropriate PLL.

Example

1. $f_{out,\ max}$ = 118.6 MHz f_{out} = 98.6 MHz
2. Choose the MB503 prescaler *(M=16)*
   $f_{out,\ max}/M$ = 7.4 MHz < 20 MHz
3. $\Delta f_{channel}$ = 0.2 MHz
4. $N_{min} = f_{out,min}/\Delta f_{channel}$ = 493
   $N_{max} = f_{out,max}/\Delta f_{channel}$ = 593
5. N_{max} > 16, OK
6. N_{max} of 593 requires a 10-bit wide N-counter

7. A_{max} of 15 requires the following:
   - A 4-bit wide (swallow) counter
   - Either an MB87001A or an MB87006A
   - Choose MB87001A
8. Choose an f_{ref} of 3.2 MHz and set the R-counter to 16 to yield $\Delta f_{channel}$ = 0.2 MHz

Programming of the counters

In order to preserve board space, all Fujitsu PLLs have serially programmable counters. The divisor values are fed through a serial pin to a shift register and latched-in with a control pulse. This allows 16-pin packaging to be used for all devices.

Set-up and switching times of the counters and modulus control logic

These delays are important and can become a limiting factor, especially when operating in pulse swallow mode. When the circuit has counted down so that the N program counter is full, the whole counter system is reset. The reset function must be completed within the next cycle of the *M/M+1* prescaler or,

$$t_{reset} < M/f_{out,max}$$

Where t_{reset} equals the sum of propagation delays through the *A* and *N* counters, (the required modulus set-up time of the prescaler and release time of the modulus control logic).

Positive or negative edge triggering of counters

As previously mentioned, when the modulus of a dual-modulus prescaler is changed from 64 to 65, one half-cycle of the output (output low) will be extended to 33 input cycles. The other half-cycle will remain unchanged at 32 input cycles.

Therefore, modulus set-up time of the prescaler will be expressed relative to an edge of the affected half-cycle (in this case the negative-going edge). If the program counters and the modulus control logic are triggered on an opposite edge, valuable set-up time margin will be lost. (See Figures 11 and 12).

When necessary, insertion of a fast inverter between the prescaler and the program counter may provide some timing relief.

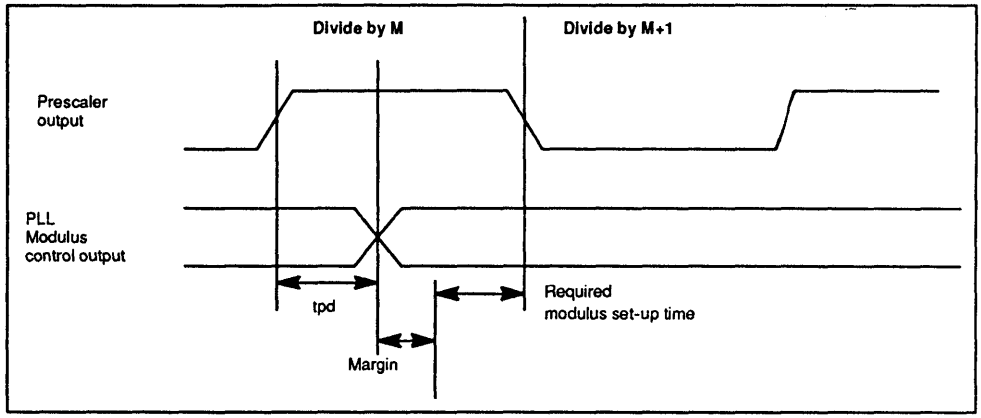


Figure 11. PLL Program Counter Triggered by Opposite Edge

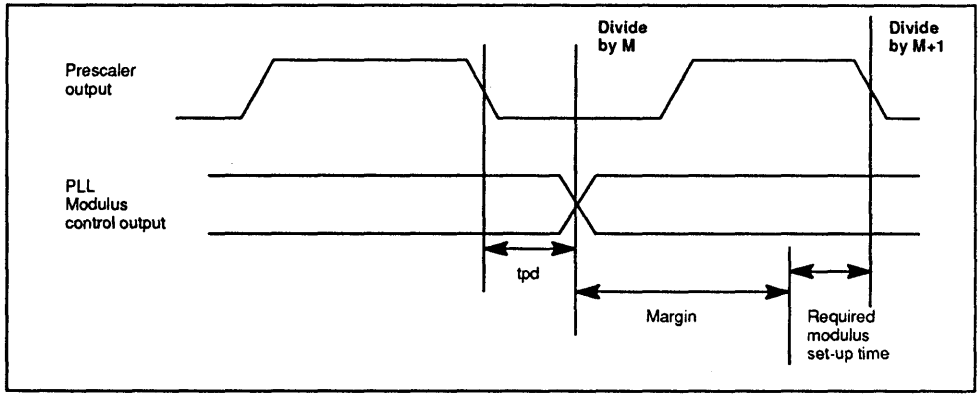


Figure 12. PLL Program Counter Triggered by Same Edge

Phase detector

There are some differences between analog and digital phase detectors.

An analog phase detector works on a so-called integrating multiplier principle (Gilbert Cell multiplier is one example) and reflects not only timing differences, but also (if the signals are not purely sinusoidal or square) differences in the shape of the input signals. Analog phase detectors can offer superior signal-to-noise (S/N) ratios and can react almost instantaneously to minute changes in input waveforms. However, they are relatively complex and lend themselves poorly to high speed CMOS integration.

The digital phase-frequency detector is a simple and extremely fast sequential circuit (4 flip-flops). The circuit detects only positive-going threshold crossings and indicates which of the two inputs is ahead of the other one. It is not dependent on the shape of the signals. The digital phase-frequency detector is in all Fujitsu PLLs.

Charge pump

The single-ended output from the phase detector is called the internal charge pump. The three-state charge pump output goes high when $f_{ref} > f_{vco}$, low when $f_{ref} < f_{vco}$ and high-impedance state when $f_{ref} = f_{vco}$. This output can be connected directly to an active or passive external filter. The MB87014 provides an inverted charge pump output as well.

The charge pump output is derived from two flip-flops out of the phase detector, ϕr and ϕv. In the case of MB87006A, MB87014 and the MB87086[1] when the loop is unlocked, the appropriate output terminal, ϕr or ϕv, pulls low to indicate which of the two inputs f_{ref} or f_{vco} is at a higher frequency.

The signals ϕr and ϕv would normally be considered an intermediate result; however, they are also made accessible on two output terminals allowing construction of an external charge pump.

A charge pump combines the two digital outputs (ϕr and ϕv) into one output. (See Figure 13.) The external configuration shown here also directly implements the lowpass filter. Note that due to different polarity assignments, this configuration is not appropriate for MB87001A, 87073, 87076, and the integrated PLLs. Also note that often a large resistor is inserted following the op-amp output to increase the output impedance.

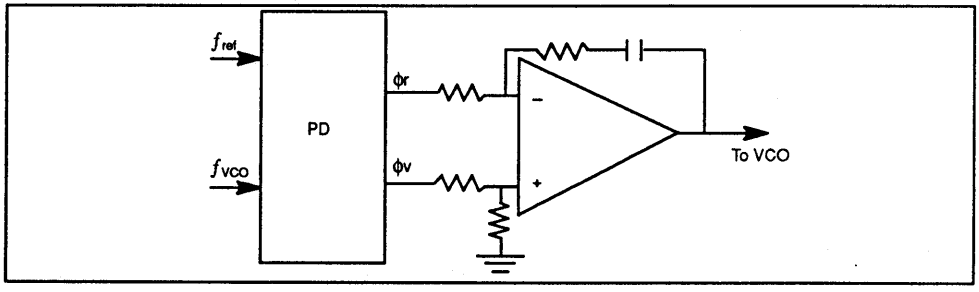


Figure 13. Active Low Pass Filter

A fast external charge pump implementation appropriate for the MB87001A, 87073, 87076 PLLs, ICs, and an integrated PLL is shown in Figure 14. The ϕr and ϕv outputs on these devices are of the open-drain type. (The rest of the PLL family provides push-pull outputs for ϕr and ϕv.)

[1]Note that the remaining Fujitsu PLL ICs (MB87001A, 87073, and 87076), as well as the single-chip PLL/Prescaler family (MB1500), have a different phase detector design and a different truth table for ϕr and ϕv:

	ϕr	ϕv
$f_r > f_v$:	Low	Low
$f_r = f_v$:	Low	High-Impedance
$f_r < f_v$:	High	High-Impedance

The ϕ-outputs of these devices are open drain.
An external charge pump allows use of faster transistors or op-amps (higher slew rates) and may offer improvement in lock-in performance.

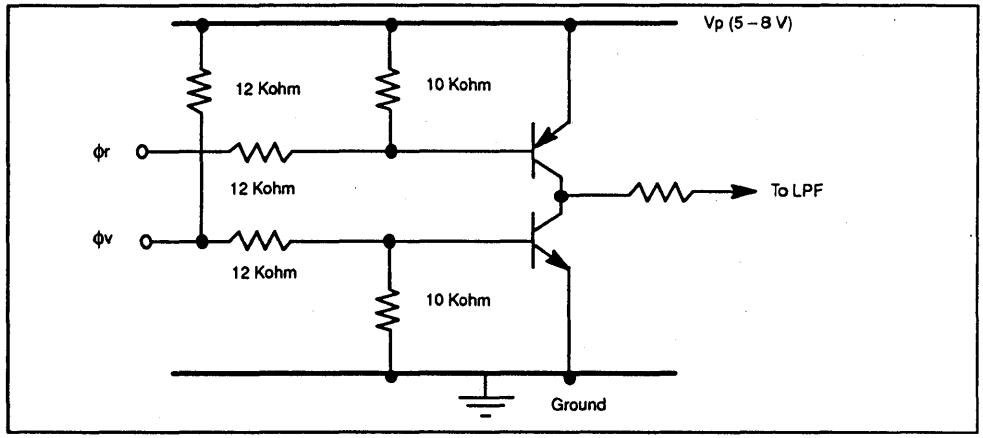


Figure 14. External Charge Pump Example

Charge pump waveforms and φr and φv

As previously mentioned, in the case of MB87006A, 87014 and 87086 (see footnote[1] on the preceeding page), when the loop is unlocked, the appropriate output terminal, φr or φv, pulls low to indicate which of the two inputs f_{ref} or f_{vco} is at a higher frequency. This active terminal, φr or φv, will not stay at a steady low but will occasionally toggle to a high state. Basically, its output provides a pulse-width modulated representation of the frequency difference between the inputs.

When the loop is in lock, φr and φv will both be in the "high" state. However, synchronously with the phase comparison frequency, a short spurious negative pulse will occur at both outputs.

The same pulse anomalies will also appear on the output from the internal charge pump. One of the tasks of the loop lowpass filter is to remove all spurious signals (pulses) from the PD output. The loop filter bandwidth must, therefore, always be below the phase comparison frequency. Conversely the phase comparison frequency should be kept as high as possible.

4-bit Microcontrollers with PLLs

Fujitsu also offers a family of 4-bit microcontrollers, the MB88560 family with an on-chip PLL.The MB88560 family consists of two 4-bit CMOS microcomputers: the MB88561 with a liquid crystal display (LCD) controller/driver and the MB88562 with a vacuum fluorescent display (VFD) driver. Both devices contain 21 I/O lines, an 8-bit timer/counter, an A/D converter with 6-bit resolution, display drivers, and a PLL with prescalers suitable for all broadcast and shortwave frequencies. Each device has independent AM (up to 32 MHz) and FM (up to 120 MHz) inputs. Up to 4 K by 8-bit ROM space and 256 K by 4-bit static RAM space is available on-chip.

Both chips allow extremely compact designs of car radios, personal stereos, personal communication equipment, etc.

A two-part MB88560 design guide and a demo board are both available from Fujitsu.

What is a Prescaler?

A prescaler is an integrated circuit that divides the frequency of an incoming signal by an integer M (see Figure15). The divisor, *M*, is called the Modulus.

Internally, a prescaler is a specialized ripple counter, which counts incoming pulses and performs one output cycle for every *M* received input cycle. If *M* is an even number the output is toggled following every *M*/2 input pulse. For *M* odd, one of the toggles is delayed an extra input cycle (e.g., 6 input pulses for output high and 5 input pulses for output low for *M* = *11*).

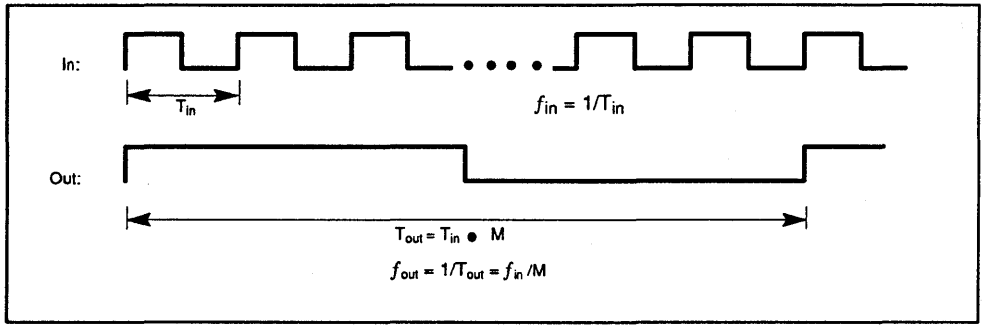


Figure15. Frequency Division

There are distinct differences between prescalers and general purpose divide-by-N counters. We will refer to the latter as program counters and substitute the letter N when referring to them for the remainder of this text.

Prescalers are comparatively simple devices. They contain a minimal amount of logic (less than approximately 100 gates) and offer a few, well chosen modulus numbers. This streamlined architecture allows implementation in the fastest bipolar and GaAs technologies without excessive power consumption or expense. For example, the MB510 dual modulus prescaler from Fujitsu offers a choice of four divide ratios (128, 144, 256 and 272). Manufactured in 0.8 µm bipolar technology, this 8-pin device is ECL compatible, accepts input frequencies up to 2.7 GHz, and dissipates only 0.05 watts of power.

Program counters, on the other hand, contain a fair amount of programming and decoding logic in order to allow a wide selection of *N* (any value of *N* between *0* and $2_q{}^{-1}$ is made selectable using a q-bit wide program input). The relatively high internal gate count generally limits program counters to TTL or CMOS technology with toggling speeds of less than 40 MHz.

The important point to be made is that there is no need to make program counters faster, or prescalers more programmable. The distinction between the two types of devices is intentional. Once the frequency is brought down sufficiently by a prescaler, sophisticated frequency manipulation is performed with CMOS program counters and a PLL. Prescalers are generally classified as either single or dual modulus.

Dual modulus prescalers

Dual modulus prescalers allow a very rapid transition from a divide-by-*M* mode to a divide-by-*M+1* mode (e.g., from 64 to 65); hence, they are often also called *M/M+1* prescalers (64/65). In conjunction with PLLs and the pulse swallow method (discussed on page 14), dual modulus prescalers allow finer frequency resolution than single modulus prescalers.

Single modulus prescalers

Single modulus prescalers are fixed, or semi-fixed dividers that only divide by a fixed number *M*. A semi-fixed single modulus prescaler allows a choice of more than one modulus (e.g., 32, 64 and 128), but is not necessarily optimized for fast switching between moduluses, and the modulus choices are not spaced one apart.

Less common varieties of prescalers include:

- *M/M+Z* (where $Z \neq 1$) dual modulus prescalers
- Four modulus prescalers
- Decimal single modulus prescalers

Figure 16 shows Fujitsu's bipolar prescaler ICs.

Please refer to the Quick Section Guide
In the front of this databook.

Figure 16. Selection Guide to the Fujitsu Bipolar Prescaler Family

Microwave Prescalers

Microwave prescalers manufactured in GaAs technology are available from specialized vendors, including Fujitsu. The microwave prescalers have frequencies above 3 GHz (microwave range) and toggle speeds of up to 10 GHz. The cost of GaAs parts, however, is considered high when compared to ECL bipolar parts.

Stand-alone Prescaler Application

Prescalers can be used as stand-alone components without a PLL.

A stand-alone application does not involve feedback of signals around the prescaler. The most common stand-alone application for a prescaler is in digital clock distribution networks, where a prescaler simply reduces an incoming clock rate and distributes it to slower analog or digital circuitry. (See Figure17.)

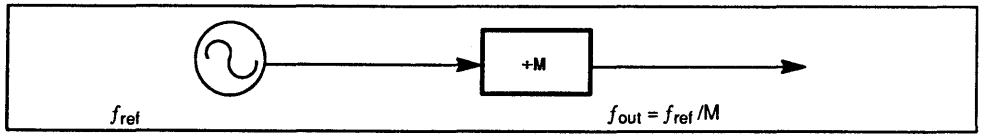


Figure 17. A Stand-alone Application of a Prescaler: Clock Rate Reduction

Prescalers offer several advantages as stand-alone elements. For example, consider an application that requires a high quality 1-MHz reference signal. For this application, a straightforward, high quality 1-MHz crystal oscillator might seem the most obvious choice; however, the highest quality will be achieved with a higher frequency reference signal (10 MHz) followed by a prescaler (1/10). This application is preferred because of the following reasons:

- Crystal resonators with higher oscillation frequency tend to have smaller dimensions, shorter oscillation stabilization times and narrower characteristic variations.
- A prescaler will clean up the incoming high frequency signal in two ways:
  - It will totally remove variations in the amplitude noise (amplitude envelope of the incoming signal), since its output amplitude is independent of the input.
  - It will reduce the phase noise (jitter of zero-crossings) of the incoming signal by approximately a factor of M since its output only switches synchronously with one out of every M/2 input pulses.

The above reasons apply up to a certain point, or as long as the prescaling factor is moderate. The frequency of the crystal should not be increased to the point where RF shielding or board layout has to be changed. Increasingly small dimensions or the price of the crystal can also become a problem.

Numerous digital LSI ICs take advantage of the beneficial properties of prescaling; e.g., they have on-board prescalers that allow a direct connection of high frequency crystal clocks to slower internal logic. For example, Fujitsu's line of 4-bit microprocessors offers a built-in, divide-by-2 prescaler as a recommended option. This option allows the user to drive the 2-MHz internal logic with a 4-MHz crystal rather than a 2-MHz crystal. With this option, the 4-MHz crystal clock will turn on and be fully operational (as well as recover from any external disturbances) in half the time required for a 2-MHz crystal.

Selecting the Right Prescaler

To select the appropriate prescaler, first determine the necessary modulus choices and input toggling speeds.

Toggling speed

One should be aware that a 1-GHz ($f_{in,max}$ typically) prescaler does not abruptly stop functioning when fed frequencies above 1 GHz. The 1-GHz prescaler will typically require higher input levels to trigger, and it may deliver a smaller output swing, but typically it will function up to a 20-50 percent higher frequency. See Figure 18.

These characteristics are important, since frequency switching in a PLL is normally accompanied by a fair amount of overshoot. A VCO intended to stabilize at 1 GHz may reach, for example, 1.4 GHz before settling down. It is important that the loop (including the prescaler) remains functional during that period. Charts like Figure 18 can be helpful in verifying such cases.

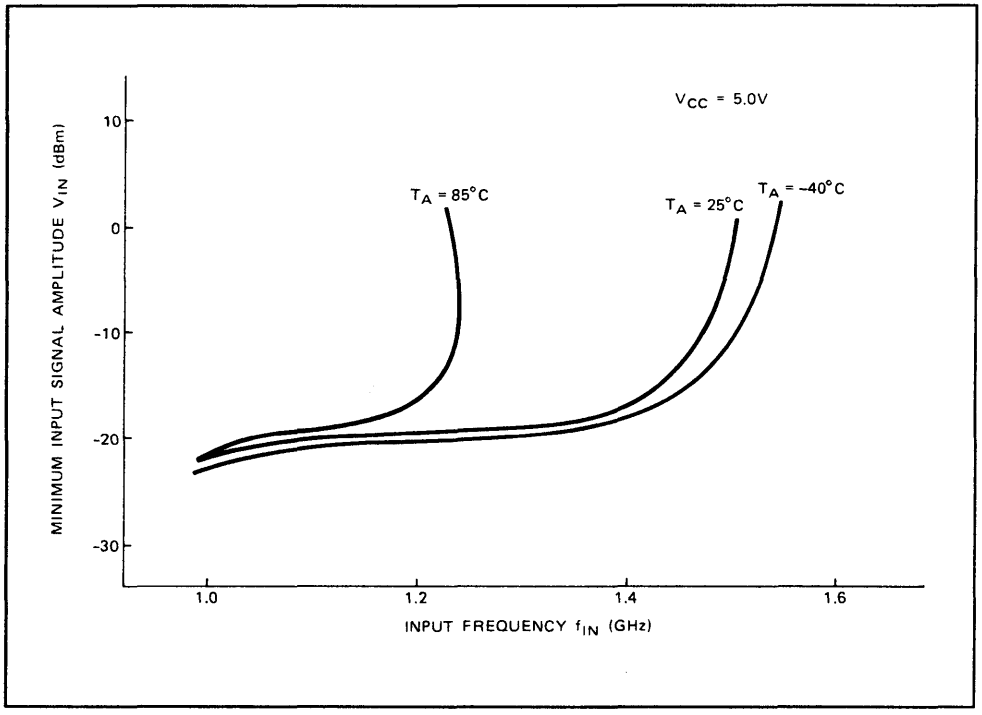


Figure 18. Input Signal Amplitude Versus Input Frequency for MB509 Dual Modulus Prescaler

Prescalers with higher frequency ratings will typically be associated with higher power dissipation and higher switching noise. For example, measurements of gallium arsenide dividers suggest noise performances 20 to 30 dB worse than for ECL dividers (reference 10).

Also note that the input coupling capacitance of a prescaler will limit the lowest useful frequency.

Termination resistor internal/external

All Fujitsu prescalers, except MB501LV, MB504LV, MB501SL, MB509, and MB510 have an open emitter output. Typically a 2.2k Ω resistor to ground for a load capacitance of 12 pF is recommended. By choosing a smaller or a larger external resistor, the prescaler's output can be tailored to drive higher or lower loads, respectively.

The prescalers with on-chip termination can drive output load capacitances of up to 8 pF undistorted. A shunt resistance can be added for driving larger loads.

In some situations it is desirable to "overdesign" the termination resistor. The limited current driving ability will tend to smooth the output signal, thus reducing its harmonic content and switching noise induced into supply lines.

Stability of V_{out}

One of the purposes of prescaling is to eliminate amplitude modulation from the output of the VCO. Therefore, it is absolutely mandatory that the output high and low are stable and guaranteed over a wide range of V_{in}, V_{cc}, and temperature.

Flexibility of the input voltage

A prescaler should be able to toggle properly with relatively widely varying input voltage levels (anywhere between 0.15 to 2 Vp-p for the Fujitsu MB 504), while maintaining a constant output level.

ECL level

For most Fujitsu prescalers the maximum allowable input voltage swing is 2 Vp-p. This means that a typical TTL voltage swing of 3 V will overload the prescaler, whereas ECL voltage levels can be accommodated without problems. The outputs of the prescaler are ECL compatible, too.

The statement "The outputs are 1.6 V peak on ECL level" found on the data sheet for MB501, 503, 504 etc. means that Fujitsu prescalers do not require negative supply voltages. In this sense they are not "true" ECL devices.

Flexibility of V_{cc}

A wide operational range of Vcc is essential (2.7 V to 4.5 V, 3.0 V typical for MB501LV), if a prescaler is to be used in a battery-powered system. Most Fujitsu prescalers, except the low voltage (LV-suffix) types which operate from a 3 V supply, operate from a single 5 V supply. The integrated PLLs, MB1501 and MB1504, however, operate from a 3 V supply (a higher supply voltage between V_{cc} and 8 V is required for the charge pump circuit).

Modulus set-up time

The time from application of appropriate voltage to the modulus select pin to appearance of the correctly prescaled waveform at the output is 10-50 ns. As previously discussed in the PLL section, fast modulus set-up times are necessary for correct implementation of the pulse swallow method.

Input impedance and reactance

Excessive reactance may affect performance of the VCO and require buffer circuitry between it and the prescaler. For very high frequencies (> 500 MHz), the input impedance should be given on a Smith chart. The nominal input impedance of Fujitsu's high frequency prescalers is 50Ω.

Smith chart

Signals on a printed circuit board travel at approximately 2/3 the speed of light. This means that at frequencies above 500 MHz, the signal wavelengths become less than 0.4 m and comparable in size to the board itself. At this point, circuit board traces start acting as transmission lines; i.e., the RMS voltage level will vary along the trace unless impedances of the termination and the trace are matched.

A Smith chart is a graphical impedance representation widely used in transmission theory. It is a tool allowing an easy assessment of impedance mismatch.

The chart consists of two sets of circles: the constant resistance circles (see Figure 19) and the constant reactance circles (see Figure 20). The values of these circles are normalized to the characteristic impedance of the system by dividing the actual value of resistance or reactance by the characteristic impedance, for example, in a 50 Ω system, a resistance of 100W is normalized to a value of 2.0.

A further series of circles may be plotted on the chart; these are the circles of constant voltage standing wave ratio (VSWR) and represent the degree of mismatch in the system. The VSWR is the ratio of the device impedance to the characteristic impedance. It is always expressed as a ratio greater than 1 (a 25 Ω device in a 50 Ω system gives rise to a 2:1 VSWR). See Figure 21.

Packaging

All Fujitsu prescalers are available in 8-pin DIP or surface mountable 8-pin plastic flat packages. Space saving and better stray capacitance performance are obtained with surface mounting.

CMOS PLLs and BiCMOS integrated PLLs are available in 16-pin DIP and Flatpacks.

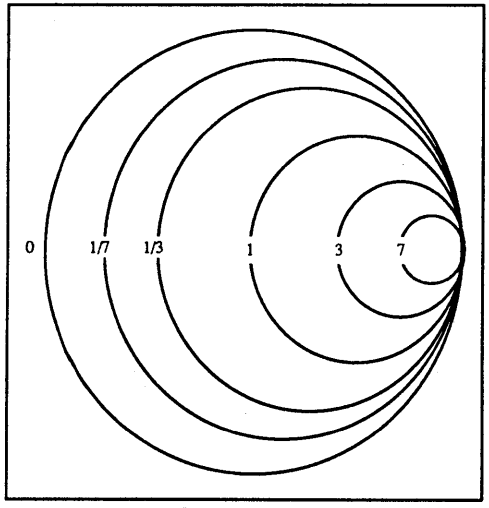


Figure 19. Smith Chart Constant Resistance

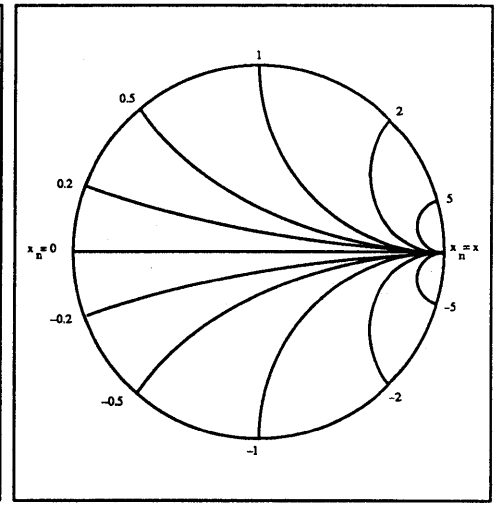
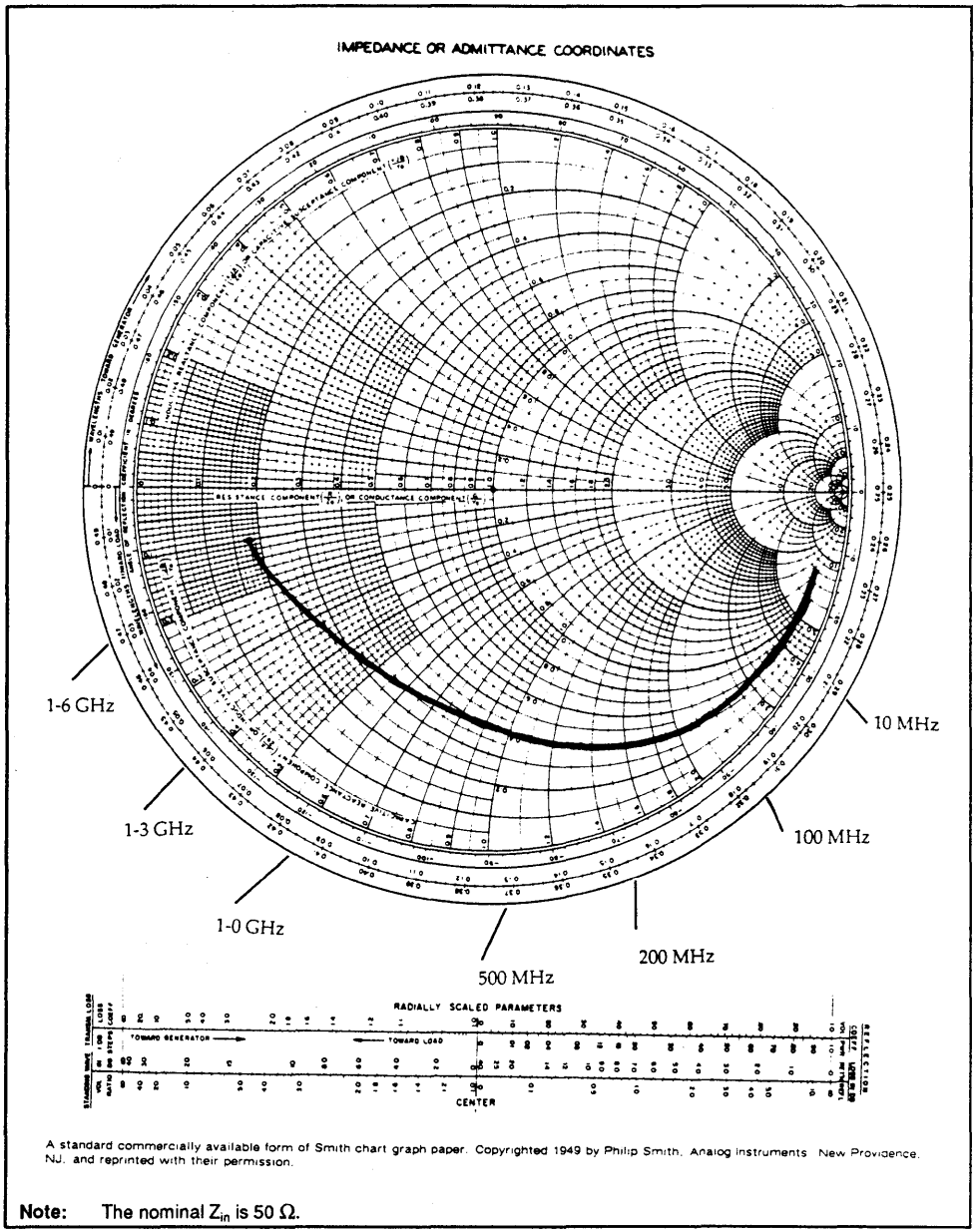


Figure 20. Smith Chart Constant Reactance



A standard commercially available form of Smith chart graph paper. Copyrighted 1949 by Philip Smith. Analog Instruments. New Providence, NJ. and reprinted with their permission.

Note: The nominal Z_{in} is 50 Ω.

Figure 21. Input Impedance of Fujitsu's MB501L Dual Modulus Prescaler as a Function of Frequency Shown on a Smith Chart

Signal propagation delay through the prescaler

Although a signal delay through the prescaler will affect the lock-in times of the loop, the prescaler is, in this respect, of little importance relative to the loop lowpass filter. Extensive phase shifts between the input and the output of the prescaler may, however, affect the PLL stability.

High capacitive loading will typically be the main cause for delays. This situation can be remedied by decreasing the output termination resistor value, thereby improving drive performance.

Self-oscillation problems can be caused by poor grounding, lack of decoupling, or cross-talk due to board layout. Fujitsu prescalers are guaranteed to be non-oscillatory under most conditions.

Balanced inputs

The ability to drive balanced inputs can be beneficial at high frequencies. All Fujitsu prescalers offer complementary inputs. The prescaler outputs, however, are single ended as they are intended to drive single-ended PLL inputs.

Output duty cycles

The output duty cycle should be 50 percent when the modulus is an even number (such as three input clock periods high and three input clock periods low for division with modulus 6). Division by an odd number should cause minimal deviation from 50 percent duty cycle (such as four input clocks high and three input clocks low for division with modulus 7). Rise and fall times are, of course, load dependent and deviations from idealized waveforms will occur. Also, clearly specify which of the output half-cycles (output low or output high) is the one that is extended in the M+1 mode of a dual modulus prescaler.

Power dissipation

Thanks to a proprietary, "third generation," 0.8 µm emitter self-align and polysilicon electrode and resistor (ESPER) manufacturing technology, Fujitsu can offer bipolar prescalers with the most beneficial frequency rating/power dissipation ratio available. See Table 3.

Table 3. Fujitsu Prescalers

Please refer to the Prescalers section
in the front of this databook.

Conclusion

For further technical assistance and product information, including updates, please contact your nearest Fujitsu Microelectronics Sales Office. You will find a listing of the offices at the back of this paper.

References

Books

1. Berlin, Howard M. *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis: Howard W. Sams & Co. 1978.
2. Blanchard, Alain. *Phase-Locked Loops: Application to Coherent Receiver Design.* New York: Wiley-Interscience, 1976.
3. Egan, William F. *Frequency Synthesis by Phase Lock.* New York: Wiley-Interscience, 1981.
4. Gardner, Floyd M. *Phaselock Techniques.* New York: John Wiley and Sons, 1979.
5. Kinley, Harold. *The PLL Synthesizer Cookbook.* Blue Ridge Summit: TAB Books, 1980.
6. Kroupa, V.F. *Frequency Synthesis.* New York: Wiley, 1973.
7 Lindsay, W. C. and M. K. Simon, eds. *Phase-Locked Loops and Their Application.* New York: IEEE Press, 1978.
8. Manassewitch, Vadim. *Frequency Synthesizers. Theory and Design.* New York: Wiley, 1976.
9. Plessey Semiconductors. *Radio Telecoms IC Handbook.* Irvine: Plessy Semiconductors, 1987.
10. Rohde, Ulrich L. *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs: Prentice-Hall, 1983.

Articles

11. Hillstrom, Tim L. "Design method yields low-noise, wide-range crystal oscillators." *EDN* (March 1988).
12. Ormond, Tom. "Crystal Oscillators." *EDN* (October 17, 1985).

Proc. Int. Symp. SAW Devices for Mobile Comm., 179-185, 1992

RESONATOR-TYPE LOW-LOSS FILTERS

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1. Introduction

The application of 800-900 MHz SAW filters as RF filters has contributed to the recent miniaturization trend in portable telephone terminals[1],[2]. SAW filters merit attention for their small size and sharp transition-band characteristics, and will find increased application for further reductions in size and power consumption and the higher sensitivity of portable telephone terminals. For example, an antenna duplexer implemented with SAW filters would greatly contribute the size reduction of telephone terminals. The conventional SAW filter's potential to implement these improvements will require work to decrease its insertion loss, obviate an external matching circuit, and increase its power handling ability.

These problems are difficult to solve with conventional transversal filters having the interdigitated interdigital transducer (IIDT) structure. From 800 to 900 MHz, the experimental insertion loss limit for IIDT filters is 3 to 4dB with an external matching circuit [1],[2]. The input or output impedance of IIDT filters is usually capacitive because of the large number of finger pairs and the high relative-permittivity of substrates such as $LiTaO_3$. Hence, conventional IIDT filters need inductive external matching elements. To overcome these limitations, we investigated the resonator-type SAW filter having a ladder structure similar to the ceramic or crystal filter. This filter can have a low insertion loss and does not require an external matching circiut, but the connection of many resonators increases tuning difficulty and size. Fortunately, these problems are resolvable with high-frequency SAW resonators because their frequency of resonance is controllable in the photolithographic fabrication process, and filter size remains small due to the short period of the IDT at high frequencies.

2. Principles

In the basic section of a ladder resonator filter (Figure 1), the impedance of the series-arm resonator (Z_s) and the admittance of the parallel-arm resonator (Y_p) are given in the following equations, assuming that they include no resistance:

$$Z_s = jX_s \quad (1)$$

$$Y_p = jB_p \quad (2)$$

The variations of X_s and B_p as a function of frequency are graphed in Figure 2. Here, the antiresonance angular frequency of the parallel-arm resonator (ω_{ap}) nearly equals the resonance angular frequency of the series-arm resonator (ω_{rs}).

The image transfer constant (γ) of the basic filter section (Figure 1) is expressed with X_s and Bp in the following equation:

$$\tanh(\gamma) = \sqrt{B_p \cdot X_s / (B_p \cdot X_s - 1)} \quad (3)$$

According to the theory of image-parameter filters, the basic section in Figure 1 shows a passband characteristic when equation 3 has an imaginary number. It does, however, show a stopband characteristic when it has a real number. Therefore, condition $0 < B_p \cdot X_s < 1$ gives the passband, and condition $B_p \cdot X_s > 1$ or $B_p \cdot X_s < 0$ gives the stopband (Figure 2). The vicinity of center frequency ω_o (= ω_{rs} = ω_{ap}) results in a passband and both sides out of a passband result in stopbands. Since X_s and B_p nearly equal to zero in the vicinity of the center frequency, the insertion loss is supposed theoretically to be zero and the input/output impedance equal to the line impedance.

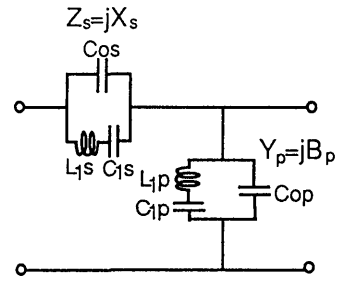

Fig.1 Basic section of a ladder filter

3. Simulation

We developed a simulation tool for the resonator-type filter based on the Smith's equivalent circuit model[3]. We modified its 3 x 3 admittance-matrix expression to a 4 x 4 chain-matrix expression as previously demonstrated[4]. The equivalent circuit used in our simulation (Figure 3) includes the electrode resistance R[5]. We assumed an electrode line and space ratio of 1:1. In this simulation, we added the following electrode effects to the previous simulation[2] :

(1) Aperture length of IDT: W
(2) Thickness of IDT: h

The aperture length of IDT W affects static capacitance C_o and resistance R of one finger as given from the following equations:

$$C_o = W \varepsilon_o \sqrt{\varepsilon_{11}\, \varepsilon_{33}}\, /2 \quad (4)$$

$$R = 4 W \rho_o / (p \cdot h) \quad (5)$$

Here,

ρ_o = 9 $\mu\Omega$ •cm (Al-2% Cu, at 1 GHz)
ε_{11} ε_{33} : Dielectric tensor components of the substrate
p: IDT period

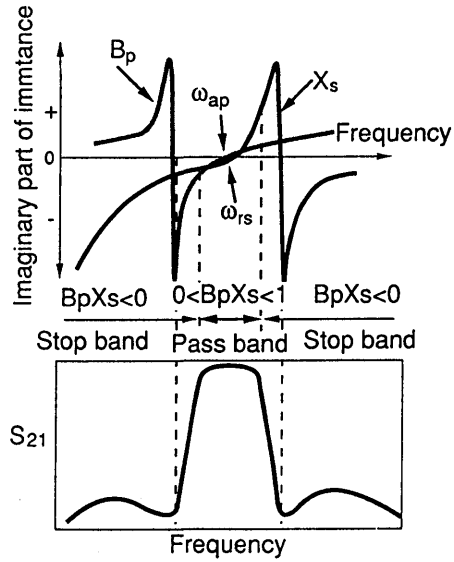

Fig.2 Bandpass filter using two kinds of SAW resonators

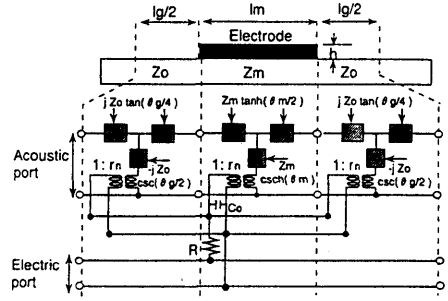

Fig.3 Equivalent circuit of IDT developed by Smith

The actual value of C_o is about 2 x 10^{-2} pF per a finger of 100-μm length on $LiTaO_3$ crystal. The effect of W on wave diffraction was not considered in our simulation, given that W is sufficiently large for diffraction.

The thickness of the electrode h affects the bulk wave radiation and the center-frequency shift i.e. mass loading effect as well as R in equation 5.

Because bulk wave radiation occurs mainly under the electrode, an acoustic transmission line supposedly has lossy paths under there. The series-arm impedance (Z_a) and the parallel-arm impedance (Z_b) of an acoustic transmission line under the electrode are replaced (Figure 3) by[6]

$$Z_a = Z_m \tan h\ (\theta_m/2) \qquad (6)$$

$$Z_b = Z_m \operatorname{cosec} h\ (\theta_m) \qquad (7)$$

where

$\theta_m = \alpha_m l_m + j\,\beta_m l_m$

l_m : Width of the finger electrode

α_m : Attenuation constant / finger

β_m : $\tau_v \pi f p / 2 V_o$

$\tau_v = V_o / V_m$

V_o: Acoustic velocity of the free surface

V_m: Acoustic velocity of the metal surface

Z_m: Acoustic impedance under the metal

The value of α_m was assumed proportional only to h, and its actual value was determined by fitting to the experimental value. The frequency dependence of α_m is neglected in this study.

The filter's center-frequency shift is due to the shift of the synchronous frequency of IDT (f_s) given by the equation[3]

$$f_s = 1/2\ (\ l_m / V_m + l_g / V_o\ )^{-1}$$

$$= 2(\ V_o / p\ ) / (1+\tau_v) \qquad (8)$$

where

l_g : Length of the gap between electrodes

From equation 8, note that fs varies towards the lower frequency with increasing τ_v. Since the relationship of τ_v to h is not clear, we tried experimentally to determine it for a 36° y-x $LiTaO_3$ crystal. We first measured the acoustic velocity under the metal film, obtaining τ_v as a function of the normalized thickness h/λ (dashed line, Figure 4). However, the linear variation of τ_v did not agree with

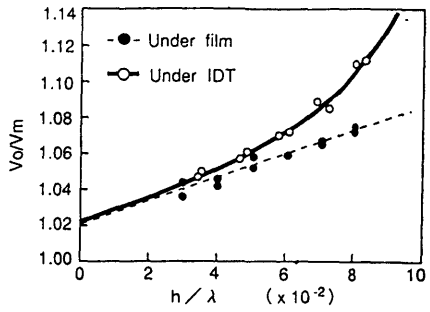

Fig.4 Dependence of τ_v on h/λ

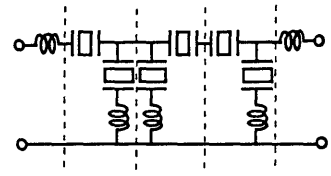

Fig.5 Filter structure consisting of three sections

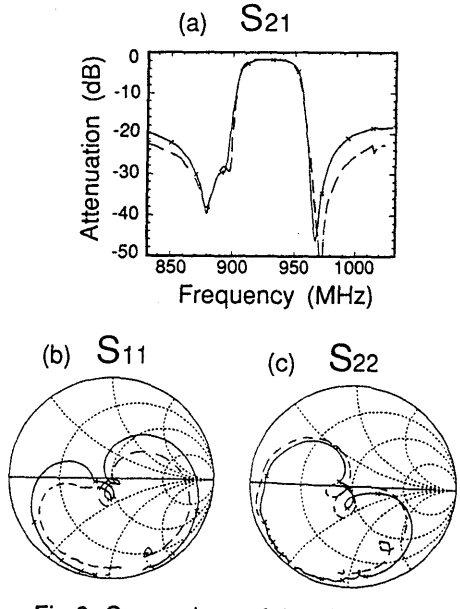

Fig.6 Comparison of the simulation (solid lines) and experiment (broken lines)

the actual center-frequency shift. We then measured the resonant frequency of one port resonator for various thicknesses and derived τ_v under IDT from it. Results are plotted by the solid line in Figure 4. The relationship of τ_v to the thickness under the IDT is obtained experimentally as

$$\tau_v = 1 + A + B(h/\lambda) + C(h/\lambda)^2 \quad (9)$$

Here, A=0.022, B=0.413, and C=7.66. We used this relationship for the simulations.

In the circuit comparing experimental and simulation results (Figure 5), each basic section is connected alternately to match image-impedances. Bonding wire inductance is about 1.5 nH. The structure had 150 finger pairs, 60 μm aperture, and 4.12-μm periods in the series-arm resonators, and 40 finger pairs, 160-μm aperture, and 4.30-μm periods in the parallel-arm resonators. Each SAW resonator had short-terminated reflectors. Results of comparison are shown in Figure 6 when h/λ is 0.073, α_m is $0.1X(h/\lambda)$ neper/finger, and k^2 is 7.5%. We fitted k^2 to the band width in passband and α_m to the insertion loss in the actual device. As shown, we obtained good agreement for three S-parameter sets.

4. Filter design

We used a simulation tool developed to investigate design rules for the resonator-type filter. The following parameters were important for controlling filter characteristics:

(1) Static capacitance ratio (C_{op}/C_{os}) of the parallel-arm resonator(C_{op}) to the series-arm resonator(C_{os})

(2) Static capacitance value for each individual resonator(C_{op},C_{os})

In designing filters, the static capacitance is determined by the product of finger pair number and aperture length W.

First, the static capacitance ratio (C_{op}/C_{os}) controls the insertion loss and stop band rejection --a tradeoff (Figure 7). This tendency is the same in a ceramic filter. If filter specifications call for a low insertion loss, we should select the lower value of C_{op}/C_{os}; for a high stop-band rejection, we would choose the higher C_{op}/C_{os} .

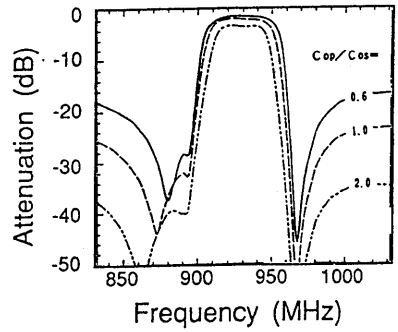

Fig.7 S_{21} dependence on static capacitance ratio C_{op}/C_{os}

We next found that the filter's input/output impedance can be controlled by changing the values of C_{op} and C_{os}, while keeping the value of C_{op}/C_{os} constant. Figures 8 to 10 show the variation of S parameters (S_{21} and S_{11}) when C_{op} and C_{os} are increased and C_{op}/C_{os}=0.75. Small dotted circles in the S_{11} charts indicate the borderline of Γ=0.33 (SWR=2.0). When the S_{11} values of the passband are within these circles, the filter is in the matching condition. Figures 8 and 10 show the unmatched

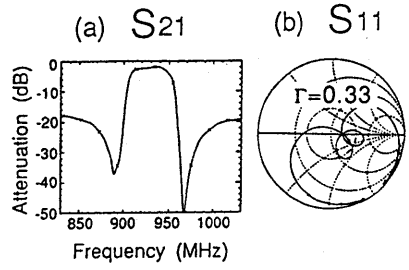

Fig.8 S-parameter characteristics under C_{op}=1.6 pF and C_{os}=2.1 pF

condition, while Figure 9 shows the matched condition. Therefore, C_{op} and C_{os} can be combined to optimize impedance matching (the shaded area in Figure 11). Figure11(a) is for a 933-MHz filter and (b) is a 1.5-GHz filter. Optimum values of C_{op} and C_{os} exist for almost all practical C_{op}/C_{os} values to the matching condition.

We considered the matching condition mechanism using a simple model. Since the resonator-type filter is simply expressed by the LC equivalent circuit (see Figure 1), each resonator's impedance, Z_s and Z_p, is given by the following equations, using the symbols from Figure 1,

$$Z_s=(\omega^2-\omega_{rs}^2) / j\omega C_{os}(\omega^2-\omega_{as}^2) \quad (10)$$

$$Z_p=(\omega^2-\omega_{rp}^2) / j\omega C_{op}(\omega^2-\omega_{ap}^2) \quad (11)$$

where

$\omega_{rs}=1/\sqrt{L_{1s}\,C_{1s}}$:
Resonant angular frequency of the series-arm resonator

$\omega_{as}=\omega_{rs}(1+C_{1s}/2C_{os})$:
Antiresonant angular frequency of the series-arm resonator

$\omega_{rp}=1/\sqrt{L_{1p}\,C_{1p}}$:
Resonant angular frequency of the parallel-arm resonator

$\omega_{ap}=\omega_{rp}(1+C_{1p}/2C_{op})$:
Antiresonant angular frequency of the parallel-arm resonator

For the matching condition of the constant K-type filter, the following relationship must be satisfied:

$$Z_s \times Z_p = R^2 \quad (12)$$

As shown in Figure 2, the following relationships is assumed,

$$\omega_{ap}\approx\omega_{rs}\approx\omega_0, \quad \omega_0-\omega_{rp}\approx\omega_{as}-\omega_0$$

$$2\omega_0 \gg \Delta\omega, \quad \Delta\omega\equiv(\omega_{as}-\omega_{rp})/2 \quad (13)$$

where ω_0 is the center frequency of the filter. From equations 12 and 13, the relationship becomes:

$$R^2\approx 1/(\omega_0^2\, C_{os}\, C_{op}) \quad (14)$$

The relationship of equation 14 is plotted by the solid line in Figures 11a, and b. Note that the matching areas shaded agree well with the equation 14, except for high C_{op}/C_{os} values.

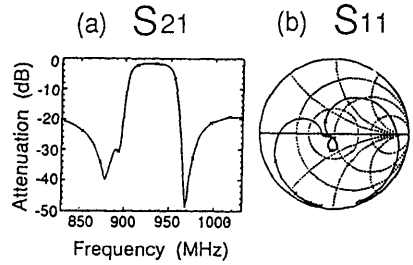

Fig.9 S-parameter characteristics under C_{op}=2.7 pF and C_{os}=3.6 pF

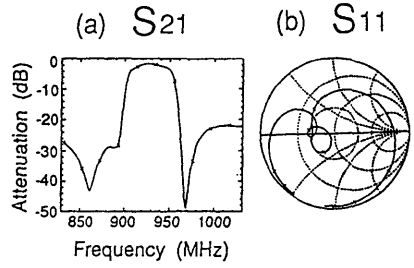

Fig.10 S-parameter characteristics under C_{op}=3.7 pF and C_{os}=5.0 pF

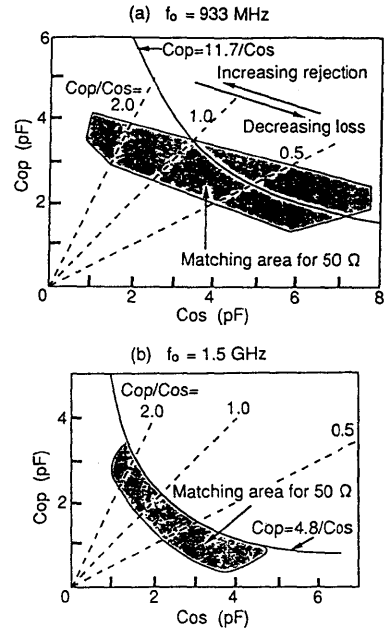

Fig.11 Optimum relations between C_{op} and C_{os} for impedance matching

5. Low-loss RF filter development

We designed and fabricated RF filters for portable telephone terminals using the rule we obtained on static capacitance. We used an Al-Cu sputtered film for the electrodes and a 36°y-x $LiTaO_3$ crystal for the piezoelectric substrate. As an example, Figures 12 and 13 show the S_{21} and SWR characteristic of a 900-MHz filter designed under capacitance conditions of C_{op}=3.0 pF, C_{os}=3.2 pF, and C_{op}/C_{os}=0.94. For comparison, the same characteristics of a conventional IIDT filter are also shown. Note that the insertion loss of the resonator-type filter is improved by 2 dB and that its SWR is less than 1.9, indicating no need for an external matching circuit. Figures 14 and 15 show the S_{21} and SWR characteristic of a 1.5-GHz band filter fabricated using an i-line stepper. The capacitance values are C_{op}=2.26 pF, C_{os}=1.6 pF, and C_{op}/C_{os}=1.4, giving us low-loss characteristics (IL<2.5 dB) and the matched condition (SWR<1.5). These filters are mounted in a 3.8 x 3.8 x 1.5 mm ceramic SMT package (Figure 16).

6. Conclusion

We investigated a bandpass filter using SAW resonators with a ladder structure. To calculate optimum design conditions, we developed a detailed simulation tool

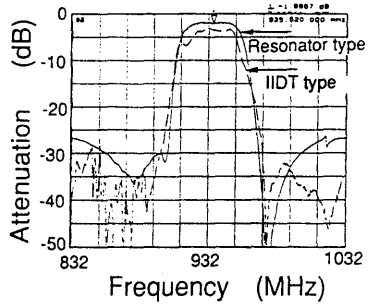

Fig.12 S_{21} characteristics of 900-MHz filters for portable telephones

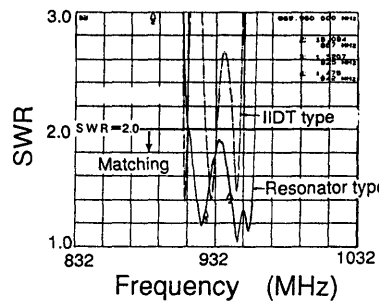

Fig.13 SWR characteristics of 900-MHz filters for portable telephones

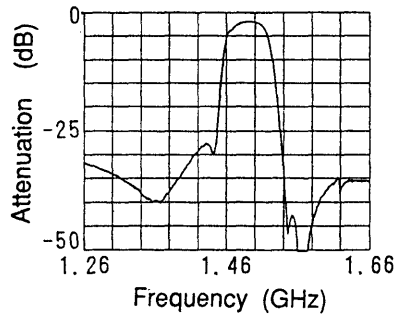

Fig.14 S_{21} characteristics of 1.5-GHz filters for portable telephones

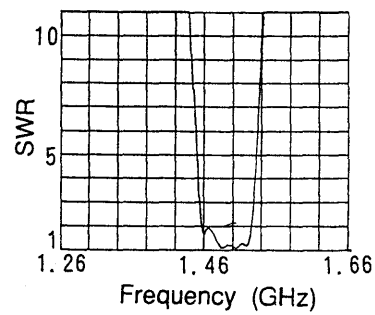

Fig.15 SWR characteristics of 1.5-GHz filters for portable telephones

which considered the aperture and electrode thickness. We fabricated 900-MHz and 1.5-GHz bandpass filters as examples, and confirmed that the insertion loss decreased compared to that for conventional IIDT filter, and that the input or output impedance was nearly 50 Ω. These features will be useful in the development of advanced portable telephone terminals.

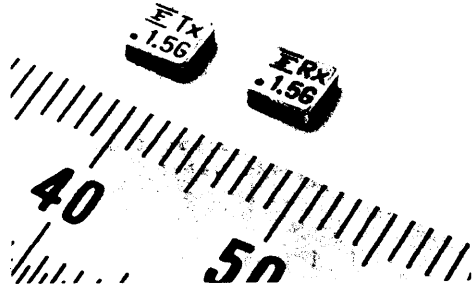

Fig.16 3.8 x 3.8 x 1.5 mm SMD package

Acknowledgements

The authors would like to thank K. Komenou for his encouragement, N. Wakatsuki for his helpful suggestions, Y. Fujiwara and H. Omori for their supply of SMD packages and many technical supports.

References

(1) M. Hikita, H. Kojima, T. Tabuchi, and Y. Kinoshita, "800-MHz high-performance SAW filter using new resonant configuration", IEEE Trans. on MTT, vol. MTT-33, No. 6, p. 510, 1985.
(2) O. Ikata, Y. Satoh, T. Miyashita, T. Matsuda, and Y. Fujiwara, "Development of 800-MHz band SAW filters using weighting for the number of finger pairs", 1990 Ultrasonics Symposium, Proceedings, p. 83, 1990.
(3) W. R. Smith, H. M. Gerard, and W. R. Jones, "Analysis and design of dispersive interdigital surface-wave transducers," IEEE Trans. on MTT, vol. MTT-20, No. 7, p. 458, 1972.
(4) H. Sato, K. Yamanouchi, and K. Shibayama, "Studies on the triple transit echo of acoustic surface wave filter", Paper of Technical Group, JIEICE, US-73-25, pp. 1-14, 1973(in Japanese).
(5) N. Nakayama, N. Wakatsuki, and M. Nakamura, "Effects of stray capacitance and electrode resistance on the acoustic surface wave transducers", Paper of Technical Group, JIEICE, US-73-48, pp. 1-10, 1973(in Japanese).
(6) T. Kojima and H. Hoshi, "Investigation of SAW resonators utilizing energy storage effect", Paper of Technical Group, JIEICE, US-86-21, pp. 61-68, 1986(in Japanese).

L and S Band Low-Loss Filters using SAW Resonators

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Abstract

This paper describes L and S band low-loss filters using one-port SAW resonators in a ladder circuit structure. Four kinds of filters were developed. Three types have a wide frequency band, with fractional bandwidth of about 4%. A 36° y-x $LiTaO_3$ substrate was used for these. The last type of filter has a narrow frequency band, with 0.03% of fractional bandwidth, and used an ST-cut quartz substrate. To design these ladder type SAW filters, several important factors were considered, the static capacitance of IDT, the period of IDT and film thickness. For fabrication, i-line stepper and reactive ion etching was used to delineate fine IDT patterns with line and gap width of 0.4 to 0.7 μm. Minimum insertion losses of 2 dB were obtained for the three wide band filters. The insertion loss of the narrow band filter was 6 dB. The input and output impedance of these filters were 50 Ω. The filters were mounted in 3 mm x 3 mm x 1 mm or 3.8 mm x 3.8 mm x 1.5 mm SMT packages.

1. Introduction

The worldwide spread of the mobile communication systems has increased the demand of SAW filters and this market will extend in the future. In order to accept a large number of subscribers, the frequency band of mobile communication systems has become higher. The recent increase in data communications has given further impetus to this market. For example, the personal digital cellular (PDC) in Japan uses the frequency range around 1.5 GHz, personal communication network (PCN) in Europe around 1.8 GHz, and wireless LAN system around 2.4 GHz. The filters used in these systems are required to have low-loss, wide band and sharp band edge characteristics with small package size. The ladder type SAW filters reported previously[1),2)] are suitable for these requirement. Figure 1 shows the filter frequency versus its fractional bandwidth, and areas which have been realized by using ladder type SAW filters. The 800 MHz filters for use in advanced mobile phone systems (AMPS) were reported in the previous paper[1)]. In this paper, these same techniques are applied to L and S band filters with a wide range of fractional bandwidths.

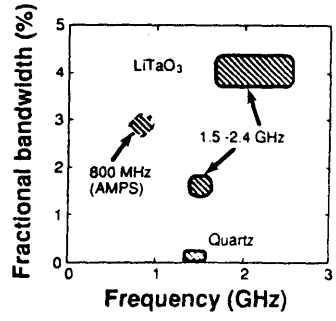


Figure 1 Filter frequency versus its fractional bandwidth. The shaded areas closed by solid line are described in the present paper.

2. Filter specifications

Japanese PDC, European PCN and wireless LAN were selected as targets for the wide band filter application. These three filters used $LiTaO_3$ as a substrate. For the narrow band pass filter application, the timing filter of HDTV was developed by using a quartz substrate. Table 1 shows these filter specifications. As shown in Table 1, each specification of four systems has a different design difficulty. PCN in Europe requires the widest fractional bandwidth of 4.3%. Wireless LAN in Europe requires high stopband rejection with wide bandwidth. HDTV requires the narrowest fractional bandwidth of 0.03%. .

3. The design of wide band-pass filters

Figure 2 shows the outline of a one-port SAW resonator and the these basic ladder circuit structure used. As suggested in the equivalent circuit of Figure 2, the one-port SAW resonator has dual resonance frequencies. In the ladder type filter design, the anti-resonance frequency of the parallel arm resonator nearly coincides with the resonance frequency of the series arm resonator. A number of basic ladder circuits are connected so as to minimize the impedance mismatching as shown in Figure 3. The character L in Figure 3 indicates the inductance of the bonding wire used in the connection to the SMT ceramic package. The resonance frequency of each resonator is designed by the period of IDT. In the design of the ladder type filter, the important factors that effect the filter's characteristics are described in the following example of the PCN filter design.

Table 1 SAW filter specifications

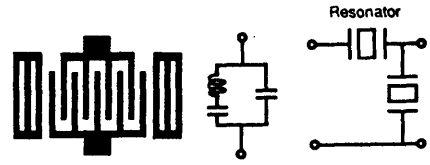
Item	PDC in Japan	PCN in Europe	Wireless LAN in Europe	Timing filter for HDTV
Center frequency	Tx:1.441 GHz Rx:1.489 GHz	Tx:1.7475 GHz Rx:1.8425 GHz	2.45 GHz	1.485 GHz
Bandwidth	24 MHz	75 MHz	100 MHz	400 kHz
Insertion loss at bandwidth	3 dB	4 dB	5 dB	7 dB
Stopband attenuation	30 dB	20 dB	40 dB	32 dB

(1) Resonators' capacitance product (CsCp)

When the series arm resonators' static capacitance and the parallel arm resonators' static capacitance are symbolized as Cs and Cp respectively, the product of Cp and Cs can control the input and output impedance of the ladder type filters[1),2)] as the equation.

$$Cp\,Cs \approx 1 / (\omega_0^2 R^2) \qquad (1)$$

Here, ω_0 is the center angular frequency of the filter and R is the line impedance which is usually 50 Ω. This relationship is plotted in Figure 4 for the center frequency (f_0) of 1.5 GHz, 1.8 GHz, 2.4 GHz. The higher f_0, the smaller the value of CpCs becomes. The static capacitance value is determined by the product of aperture length and finger pair number of IDT. Therefore, the small static capacitance results in the small size of IDT, that is, the small chip size. The ladder type SAW filter is suitable for high frequency filter in view of the package size.



a) A SAW resonator and its equivalent circuit.

(b) A basic ladder circuit structure.

Figure 2 The outline of a one-port SAW resonator and a basic ladder circuit structure used.

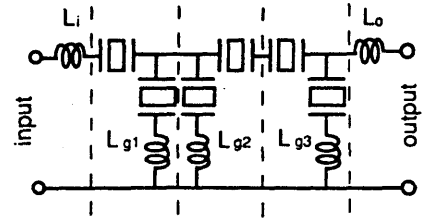


Figure 3 A filter structure connecting three basic sections. The character L indicates the inductance of bonding wire.

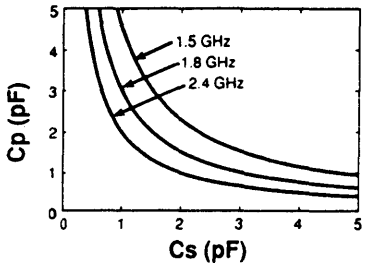


Figure 4 Optimum relations between Cp and Cs for impedance matching.

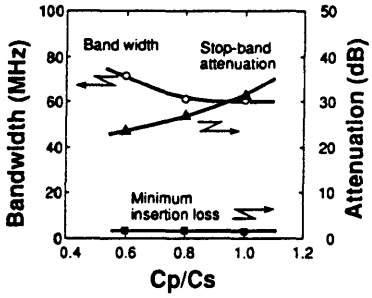


Figure 5 Dependence of bandwidth, the stopband attenuation and minimum insertion loss on Cp/Cs in the frequency range around 1.8 GHz.

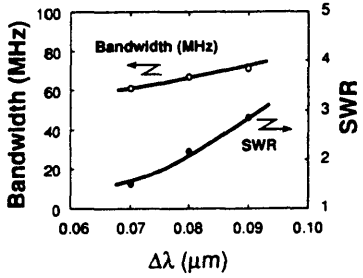


Figure 6 Dependence of band width and SWR on Δλ in the frequency range around 1.8 GHz.

(2) Resonators' capacitance ratio (Cp/Cs) and the number of basic ladder circuits

The filters' insertion loss and stopband attenuation are affected by the ratio Cp/Cs. Figure 5 shows dependencies of the bandwidth, the stopband attenuation and the minimum insertion loss on Cp/Cs in the frequency range around 1.8 GHz. As shown in Figure 5, if Cp/Cs becomes larger, bandwidth is narrower. The minimum insertion loss didn't change, but the nominal insertion loss averaged over the passband increased. It is necessary for the PCN specification that the stopband attenuation is larger than 20 dB and the bandwidth is wider than 82 MHz over a temperature range of -30 to 70 °C. It is noticed in Figure 5 that both the stopband attenuation and bandwidth specifications can't be satisfied together. A new development to solve this problem is described in the later section.

The number of basic ladder circuits show the same characteristics as Cp/Cs. By increasing the number, the stopband attenuation is improved, the insertion loss is increased and the bandwidth becomes narrower.

(3) The difference of period, Δλ

The anti-resonance frequency of the parallel arm resonator and the resonance frequency of the series arm resonator are controlled by Δλ which is the difference between IDT periods of the parallel arm resonator and the series arm resonator. The anti-resonance frequency of the parallel arm resonator doesn't need to be equal to the resonance frequency of the series arm resonator. The passband can be extended by increasing Δλ. The standing wave ratio (SWR), however, becomes larger by increasing Δλ. Figure 6 shows dependence of SWR and bandwidth on Δλ in the frequency range around 1.8 GHz. When the limit of SWR is less than 2.0, the bandwidth is limited to 70 MHz which is insufficient for the PCN specification.

(4) Film thickness, h

The number of basic ladder circuits, Δλ and Cp/Cs are related to each other as described above and the wide band filter for PCN can't be realized by

adjusting these factors. However, electromechanical coupling factor (k^2) of the piezoelectric substrate was noticed to relate the fractional bandwidth. If k^2 is larger, the bandwidth is wider. The electromechanical coupling factor is given in the following equation.

$$k^2 = 2(V_0 - V_m) / V_0 \qquad (2)$$

Here,

V_0 : free surface velocity

V_m : metal surface velocity

As apparent in this equation, if V_m become slower, k^2 become larger. The thicker film thickness of IDT is available to make V_m slower, but the nominal insertion loss may be increased by making the electrodes thicker. Figure 7 shows the experimental dependence of bandwidth, insertion loss and SWR on the film thickness. The values of Cp/Cs and $\Delta\lambda$ were constant in Figure 7, but the passband was extended and SWR became less than 2.0 by increasing the film thickness. Contrary to the anticipated result, the insertion loss didn't deteriorate for these film thicknesses. The reason for this characteristic may be that the insertion loss is recovered by increasing k^2 through making the electrodes thicker. For further increasing the film thickness, the insertion loss will deteriorate due to bulk wave radiation. For PCN specification, a sufficient bandwidth (85 MHz) and an SWR (<2.0) are obtained at 0.2 μm film thickness.

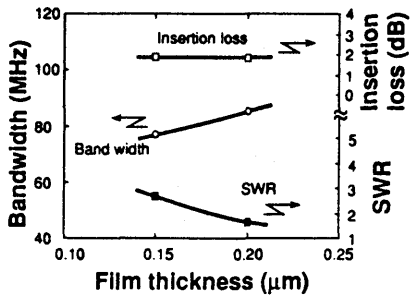


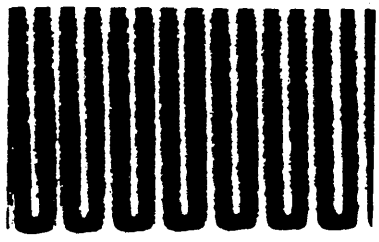
Figure 7 Dependence of bandwidth, insertion loss and SWR on the film thickness in the frequency range around 1.8 GHz.

4. The design of a narrow band-pass filter

This filter used an ST-cut quartz as substrate and SH-type SAW[3]. The dielectric constant of quartz is much smaller than that of $LiTaO_3$. Therefore, the size of IDT needs more space compared with $LiTaO_3$ substrate in order to design the impedance matching. The value of $\Delta\lambda$ is very small, about 0.01 μm. Some attention is therefore needed to control $\Delta\lambda$. To precisely control $\Delta\lambda$, the reticle is made with very high accuracy.

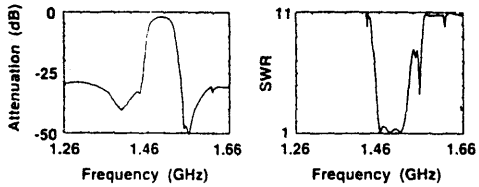
5. Fabrication and evaluation of filters

The electrode film consisted of Al-Cu alloy deposited by the DC sputter on piezoelectric substrates. The IDT photoresist patterns were exposed on an i-line stepper. Figure 8 shows IDT photoresist patterns for 2.4 GHz. The line and gap width of IDT patterns were 0.4 μm. The reactive ion etching was used to avoid surface damage of a substrate. Figure 9 shows the S_{21} and SWR characteristics of 1.5 GHz filter for PDC. This filter had 2 dB minimum insertion loss, 38 MHz bandwidth at 3 dB and about 30 dB stopband attenuation. The SWR was less than 2.0 in the passband. Figure 10 shows the same characteristics of 1.8 GHz filter for European PCN. The maximum fractional bandwidth in this study was obtained. Filter characteristics were 85 MHz bandwidth at 4 dB and about 20 dB stopband attenuation. The SWR was less than 2.0. Figure 11 shows the wireless LAN filter. The bandwidth was 110 MHz at 5 dB and the stopband attenuation was about 45 dB which was a very high value. The SWR was less than 2.5. Figure 12 shows a timing filter for HDTV. The bandwidth of 400 kHz at 6.5 dB, which was the minimum fractional bandwidth of 0.03% in this study, about 30 dB the stopband attenuation and the SWR of less than 2.0 were obtained. The HDTV filter and PDC filter were mounted in a 3.8 mm x 3.8 mm x 1.5 mm ceramic SMT packages. The other filters were mounted in 3 mm x 3 mm x 1 mm ceramic SMT packages.



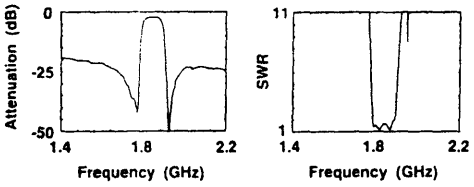
1 μm

Figure 8 IDT photoresist patterns for 2.4 GHz.



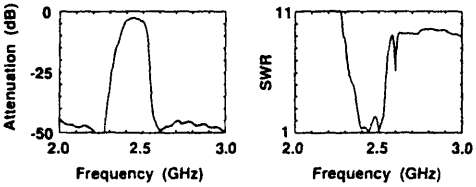
(a) S_{21} (b) SWR

Figure 9 S_{21} and SWR characteristics of 1.5 GHz filter for Japanese PDC.



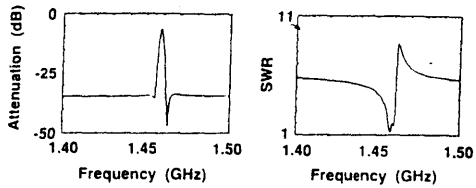
(a) S_{21} (b) SWR

Figure 10 S_{21} and SWR characteristics of 1.8 GHz filter for European PCN.



(a) S_{21} (b) SWR

Figure 11 S_{21} and SWR characteristics of 2.4 GHz filter for wireless LAN.



(a) S_{21} (b) SWR

Figure 12 S_{21} and SWR characteristics of 1.5 GHz filter for HDTV.

6. Conclusion

L and S band low-loss filters were developed using the ladder type filter made of one port SAW resonators. The filters for PDC in Japan, PCN in Europe and wireless LAN in Europe were successfully developed as wideband applications, and HDTV filter was developed as a narrow band application. These filters' characteristic impedances were all 50 Ω. The properties of these filters will be useful in the future development of the wireless communications systems discussed.

Acknowledgement

The author would like to thank Y. Fujiwara for his supply of SMT package and H. Omori for his helpful suggestions.

Reference

(1) O. Ikata, T. Miyashita, T. Matsuda, T. Nishihara and Y. Satoh, "Development of Low-Loss Band-Pass Filters Using SAW Resonators for Portable Telephones": IEEE, Ultrasonic symposium, pp. 111-115, (1992)

(2)Y. Satoh, O. Ikata, T. Matsuda, "A Band-Pass Filter Using One-Port SAW Resonators", FUJITSU Scientific & Technical Journal, Vol. 29, No. 4, pp.367-376 (December, 1993)

(3)T. Nishikawa, A. Tani, C. Takeuchi, "SH-Type Surface Acoustic Waves on Rotated Y-cut Quartz", FUJITSU Scientific & Technical Journal, Vol. 17 No. 4, pp.99-113 (December, 1981)

SECTION 10

Quality and Reliability

Fujitsu Quality Program

To ensure the best quality in our semiconductor products, Fujitsu conducts a complete program of inspections at every phase of processing.

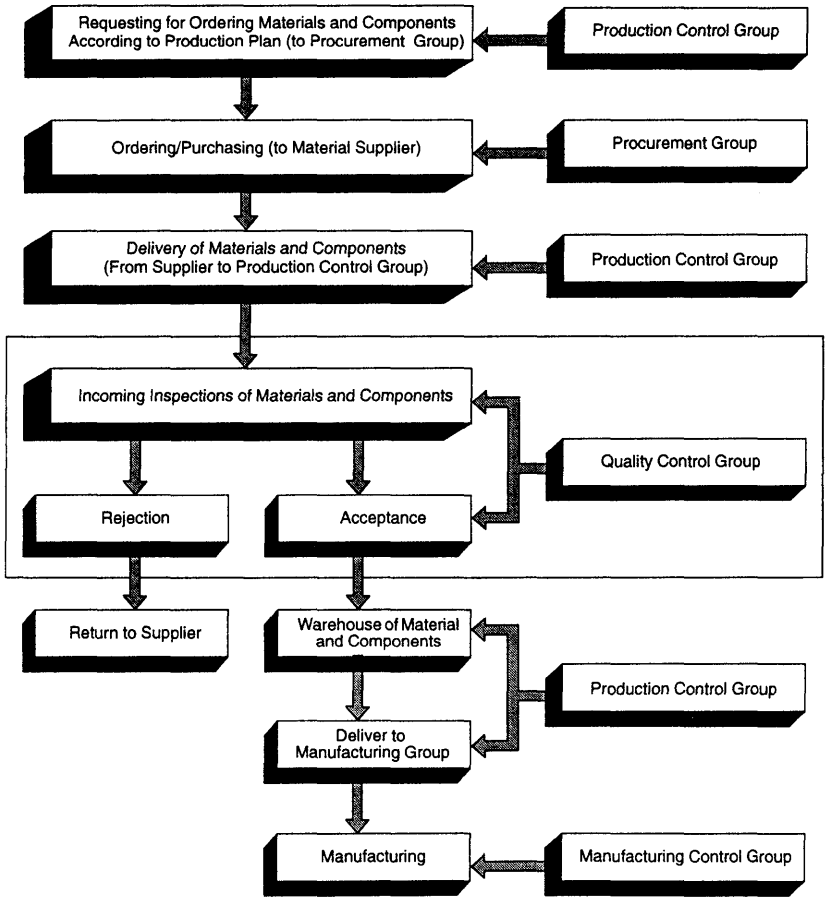
The wide range of inspections in our manufacturing programs ensures that every product has the quality and reliability for which it was designed Statistical analysis evaluates these results objectively.

Incoming Inspections

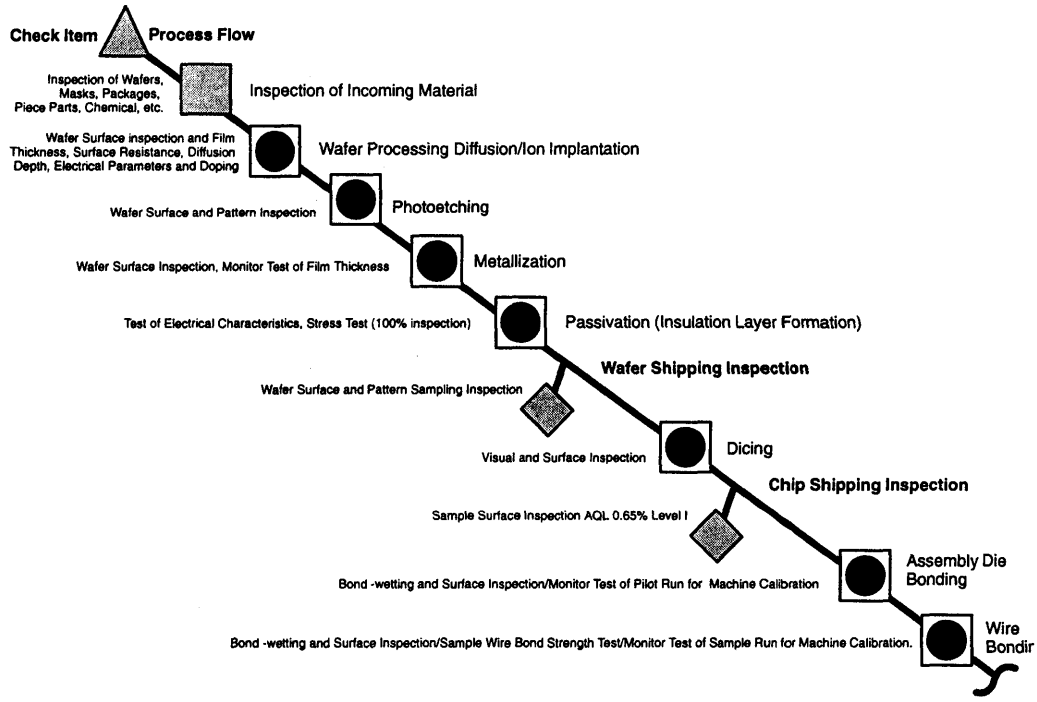
Whenever a Fujitsu plant purchases materials or components from another manufacturer, the Quality Control Group conducts an incoming inspection. The group visits the supplier's factories to convey the importance Fujitsu places on the quality of everything we buy. Moreover Fujitsu will work together with the suppliers to maintain and improve the quality of their products.

Every year, we award the best manufacturers to encourage all our suppliers to maintain and improve the quality of their products

Control Flow for the Purchase of Materials and Components



Quality Control Flow Chart



In-Process Manufacturing Group Inspections

Fujitsu's Manufacturing Groups implement these inspections to set control items and standards for each manufacturing process. Prompt feedback maintains and improves the quality consciousness throughout the groups.

Inspections occur regularly for each lot and/or each production line.

In-Process QC Group Inspections

The Quality Control Groups inspect at the end of each major manufacturing.

Using the sampling standards, the groups confirm the level of quality before the products proceed to the next phase.

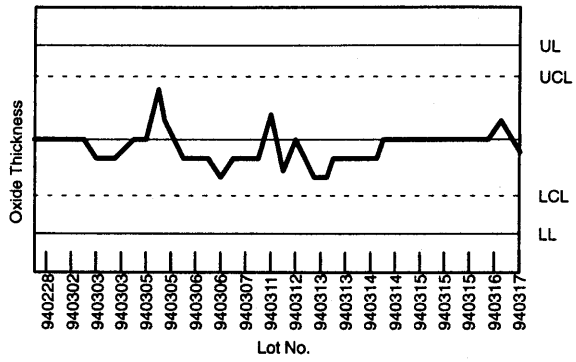
Statistical Process Control (SPC)

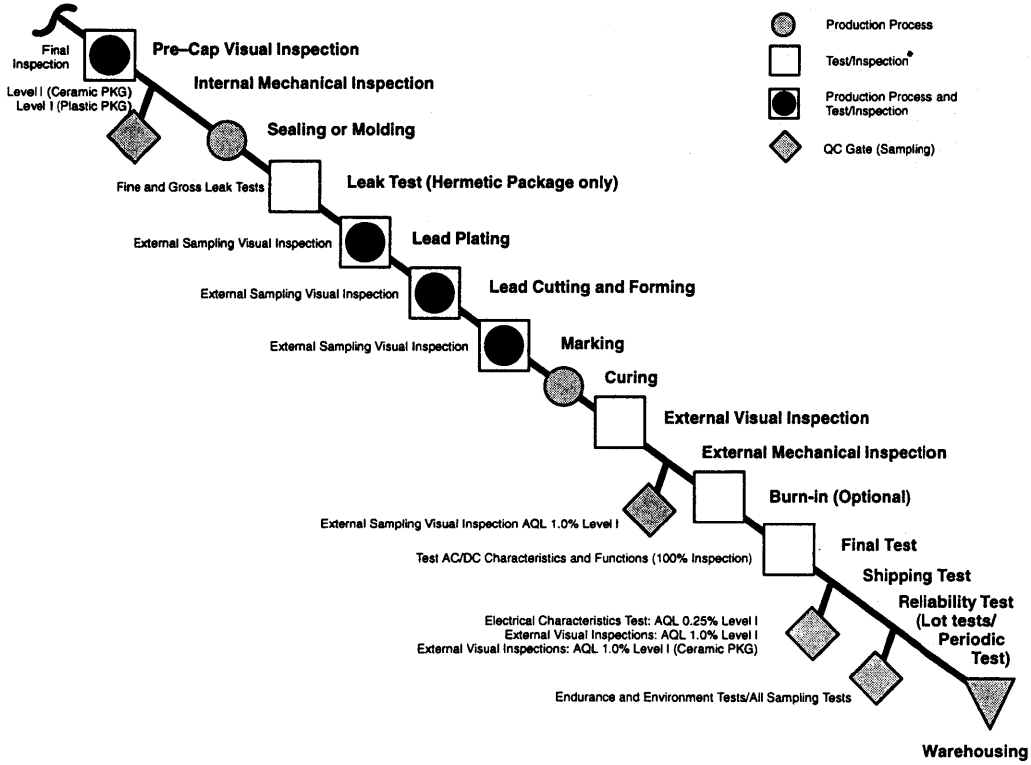
Fujitsu's SPC program uses statistical analysis. Engineering Groups set the major quality parameters and their spec value for the manufacturing processes to assure the proper quality. The Manufacturing Groups determine the control values for the equipment and conditions for the production process.

Once mass production begins, the Manufacturing Groups implement control plans to check and improve the product capability to each process.

Some important parameters are film thickness, monitor characteristics, bonding strength, electrical characteristics and yield (see figure at right). Computer software checks each parameter automatically.

16M DRAM Oxide Thick





SECTION 11

Ordering Information

Part Number	Description	Package Type	Options	Order Number
PRESCALERS				
MB501L	1.1 GHz Prescaler	DIP-08P-M01		MB501LP
		FPT-08P-M01		MB501LPF
		FPT-08P-M01	T&R	MB501LPF-ER
MB501LV	1.1 GHz Prescaler	DIP-08P-M01		MB501LVP
		FPT-08P-M01		MB501LVPF
MB501SL	1.1 GHz Prescaler	DIP-08P-M01		MB501SLP
		FPT-08P-M01		MB501SLPF
		FPT-08P-M01	T&R	MB501SLPF-ER
MB504	520 MHz Prescaler	DIP-08P-M01		MB504P
		FPT-08P-M01		MB504PF
		FPT-08P-M01	T&R	MB504PF-ER
MB504L	520 MHz Prescaler	DIP-08P-M01		MB504LP
		FPT-08P-M01		MB504LPF
		FPT-08P-M01	T&R	MB504LPF-ER
MB504LV	520 MHz Prescaler	DIP-08P-M01		MB504LVP
		FPT-08P-M01		MB504LVPF
MB505-16	1.6 GHz Prescaler	DIP-08P-M01		MB505-16P
		FPT-08P-M01		MB505-16PF
MB506	2.4 GHz Prescaler	DIP-08P-M01		MB506P
		FPT-08P-M01		MB506PF
		FPT-08P-M01	T&R	MB506PF-ER
MB507	1.6 GHz Prescaler	DIP-08P-M01		MB507P
		FPT-08P-M01		MB507PF
		FPT-08P-M01	T&R	MB507PF-ER
MB508	2.3 GHz Prescaler	DIP-08P-M01		MB508P
		FPT-08P-M01		MB508PF
		FPT-08P-M01	T&R	MB508PF-ER
MB509	1.1 GHz Prescaler	DIP-08P-M01		MB509P
		FPT-08P-M01		MB509PF
MB510	2.7 GHz Prescaler	DIP-08P-M01		MB510P
		FPT-08P-M01		MB510PF
		FPT-08P-M01	T&R	MB507PF-ER
MB511	2.7 GHz Prescaler	DIP-08P-M01		MB511P
		FPT-08P-M01		MB511PF
MB551	1.0 GHz Prescaler	FPT-08P-M01		MB551PF
	& VCO			

ORDERING INFORMATION FOR STANDARD PRODUCTS

Part Number	Description	Package Type	Options	Order Number
CMOS PLLs				
MB87001A	13 MHz PLL	DIP-16P-M04		MB87001AP
		FPT-16P-M06		MB87001APF
MB87006A	17 MHz PLL	DIP-16P-M04		MB87006AP
		FPT-16P-M06		MB87006APF
MB87014A	180 MHz PLL	DIP-16P-M04		MB87014AP
		FPT-16P-M06		MB87014APF
		FPT-16P-M06	T&R	MB87014APF-ER
MB87076	10 MHz PLL	FPT-16P-M06		MB87076PF
MB87086A	95 MHz PLL	DIP-16P-M04		MB87086AP
		FPT-16P-M06		MB87086APF
MB87087	17 MHz PLL	FPT-16P-M06		MB87087PF
MB87091	300 MHz PLL	FPT-16P-M06		MB87091PF
		FPT-20P-M03		MB87091PFV
MB87093A	145 MHz PLL	FPT-16P-M05		MB87093APFV
MB87094	15 MHz PLL	FPT-16P-M05		MB87094PFV
MB87095A	110 MHz PLL	FPT-16P-M05		MB87095APFV
MB87096A	90 MHz PLL	FPT-16P-M05		MB87096APFV
SUPER PLLs				
MB15A01	1.1 GHz SPLL	FPT-16P-M05		MB15A01PFV1
MB15B01	1.1 GHz D-SPLL	FPT-20P-M03		MB15B01PFV
MB1501	1.1 GHz SPLL	DIP-16P-M04		MB1501P
		FPT-16P-M06		MB1501PF
		FPT-16P-M06	T&R	MB1501PF-ER
MB1501H	1.1 GHz SPLL	FPT-16P-M06		MB1501HPF
		FPT-16P-M06	T&R	MB1501HPF-ER
MB1501L	1.1 GHz SPLL	FPT-16P-M06		MB1501LPF
		FPT-16P-M06	T&R	MB1501LPF-ER
MB15A02	1.1 GHz SPLL	FPT-16P-M06		MB15A02PF
		FPT-16P-M05		MB15A02PFV1
		FPT-20P-M03		MB15A02PFV2
MB1502	1.1 GHz SPLL	FPT-16P-M06		MB1502PF
		FPT-16P-M06	T&R	MB1502PF-ER
MB1502H	1.1 GHz SPLL	FPT-16P-M06		MB1502HPF
MB15B03	1.1/.3 GHz D-SPLL	FPT-16P-M05		MB15B03PFV1
MB15F03	2.0/.5 GHz D-SPLL	FPT-16P-M05		MB15F03PFV1
MB1503	1.1 GHz SPLL	FPT-16P-M06		MB1503PF

ORDERING INFORMATION FOR STANDARD PRODUCTS

Part Number	Description	Package Type	Options	Order Number
MB1504	520 MHz SPLL	DIP-16P-M04		MB1504P
		FPT-16P-M06		MB1504PF
		FPT-16P-M06	T&R	MB1504PF-ER
MB1504H	520 MHz SPLL	FPT-16P-M06		MB1504HPF
MB1504L	520 MHz SPLL	FPT-16P-M06		MB1504LPF
MB15E05	2.0 GHz SPLL	FPT-16P-M05		MB15E05PFV1
MB1505	600 MHz SPLL	FPT-16P-M02		MB1505PF
MB15E06	2.5 GHz SPLL	FPT-16P-M05		MB15E06PFV1
MB1506	2.0 GHz SPLL	FPT-20P-M03		MB1506PFV
MB1507	2.0 GHz SPLL	FPT-16P-M06		MB1507PF
MB1508	2.5 GHz SPLL	FPT-20P-M01		MB1508PF
MB1509	400 MHz D-SPLL	FPT-20P-M01		MB1509PF
MB15U10	1.1 GHz D-SPLL	FPT-20P-M03		MB15U10PFV
MB1510	1.1 GHz D-SPLL	FPT-20P-M01		MB1510PF
		FPT-20P-M01	T&R	MB1510PF-ER
MB15B11	1.1/.4 GHz D-SPLL	FPT-20P-M03		MB15B11PFV
MB1511	1.1 GHz SPLL	FPT-20P-M03		MB1511PFV
		FPT-20P-M03	T&R	MB1511PFV-ER
MB1512	1.1 GHz SPLL	FPT-20P-M03		MB1512PFV
		FPT-20P-M03	T&R	MB1512PFV-ER
MB15B13	1.1 GHz D-SPLL	FPT-20P-M03		MB15B13PFV
MB1513	1.1 GHz SPLL	FPT-20P-M03		MB1513PFV
		FPT-20P-M03	T&R	MB1513PFV-ER
MB1514	400 MHz D-SPLL	FPT-20P-M01		MB1514PF
MB1515	2.5 GHz SPLL	FPT-20P-M03		MB1515PFV
MB15A16	1.1 GHz SPLL	FPT-16P-M05		MB15A16PFV1
		FPT-16P-M05	T&R	MB15A16PFV1-ER
MB1516A	1.1 GHz SPLL	FPT-16P-M05		MB1516APFV1
		FPT-16P-M05	T&R	MB1516APFV1-ER
MB1517A	1.1 GHz SPLL	FPT-16P-M05		MB1517APFV1
		FPT-16P-M05	T&R	MB1517APFV1-ER
MB1518	2.5 GHz SPLL	FPT-16P-M06		MB1518PF
		FPT-16P-M06	T&R	MB1518PF-ER
MB15A19	600 MHz D-SPLL	FPT-20P-M01		MB15A19PF
MB1519	600 MHz D-SPLL	FPT-20P-M01		MB1519PF
MB15S02	300 MHz MASKED	SOP-8P-M03		MB15S02PFV

ORDERING INFORMATION FOR STANDARD PRODUCTS

Part Number	Description	Package Type	Options	Order Number
SUPER ANALOG				
MB531	1.1 GHz MIXER	FPT-8P-M01		MB531PF
MB539	1.6 GHz LNA	FPT-8P-M03		MB539PFV
MB54501	1.1 GHz LNA/MIX	FP-16P-M05		MB54501PFV
MB54502	1.1 GHz D-LNA	FP-16P-M05		MB54502PFV
MB54503	1.1 GHz AMP	FP-16P-M05		MB54503PFV
MB54609	1.0 GHz I/Q MOD	FPT-20P-M03		MB54609PFV
MB54619	2.0 GHz I/Q MOD	FPT-20P-M03		MB54619PFV
SAW FILTERS				
FAR-F5CB-836M50-G201	AMPS SAW	5 X 5 MM	3K T&R	F5CB-836M50G201R
			1K T&R	F5CB-836M50G201T
FAR-F5CB-881M50-G201	AMPS SAW	5 X 5 MM	3K T&R	F5CB-881M50G201R
			1K T&R	F5CB-881M50G201T
FAR-F5CB-881M50-G211	AMPS SAW	5 X 5 MM	3K T&R	F5CB-881M50G211R
FAR-F5CB-888M50-G201	ETACS SAW	5 X 5 MM	1K T&R	F5CB-888M50G201T
FAR-F5CB-933M50-G202	ETACS SAW	5 X 5 MM	1K T&R	F5CB-933M50G202T
FAR-F5CB-911M50-G201	NTACS SAW	5 X 5 MM	3K T&R	F5CB-911M50G201R
			1K T&R	F5CB-911M50G201T
FAR-F5CB-902M50-G201	NMT SAW	5 X 5 MM	1K T&R	F5CB-902M50G201T
FAR-F5CB-947M50-G201	NMT SAW	5 X 5 MM	1K T&R	F5CB-947M50G201T
FAR-F5CB-947M50-G211	NMT SAW	5 X 5 MM	1K T&R	F5CB-947M50G201T
FAR-F5CC-836M50-L2AA	AMPS SAW	3.8 X 3.8 MM	1K T&R	F5CC-836M50L2AAT
FAR-F5CC-836M50-L2AZ	AMPS SAW	3.8 X 3.8 MM	1K T&R	F5CC-836M50-L2AZT
FAR-F5CC-881M50-L2AB	AMPS SAW	3.8 X 3.8 MM	1K T&R	F5CC-881M50L2ABT
FAR-F5CC-881M50-L2AY	AMPS SAW	3.8 X 3.8 MM	1K T&R	F5CC-881M50-L2AYT
FAR-F5CC-933M50-L2BA	NTT SAW	3.8 X 3.8 MM	1K T&R	F5CC-933M50-L2BAT
FAR-F5CC-878M50-L2BB	NTT SAW	3.8 X 3.8 MM	1K T&R	F5CC-878M50-L2BBT
FAR-F5CC-888M50-L2CA	ETACS SAW	3.8 X 3.8 MM	1K T&R	F5CC-888M50-L2CAT
FAR-F5CC-933M50-L2CB	ETACS SAW	3.8 X 3.8 MM	1K T&R	F5CC-933M50-L2CBT
FAR-F5CC-911M50-L2DA	NTACS SAW	3.8 X 3.8 MM	1K T&R	F5CC-911M50-L2DAT
FAR-F5CC-856M50-L2DB	NTACS SAW	3.8 X 3.8 MM	1K T&R	F5CC-856M50-L2DBT
FAR-F5CC-902M50-L2EA	NMT SAW	3.8 X 3.8 MM	1K T&R	F5CC-902M50-L2EAT
FAR-F5CC-902M50-L2EZ	NMT SAW	3.8 X 3.8 MM	1K T&R	F5CC-902M50L2EZT
FAR-F5CC-902M50-L2EX	NMT SAW	3.8 X 3.8 MM	1K T&R	F5CC-902M50-L2EXT
FAR-F5CC-947M50-L2EY	NMT SAW	3.8 X 3.8 MM	1K T&R	F5CC-947M50-L2EYT
FAR-F5CC-897M50-L2KA	EGSM SAW	3.8 X 3.8 MM	1K T&R	F5CC-897M50L2KAT
FAR-F5CC-942M50-L2KB	EGSM SAW	3.8 X 3.8 MM	1K T&R	F5CC-942M50-L2KBT
FAR-F5CC-942M50-L2KY	EGSM SAW	3.8 X 3.8 MM	1K T&R	F5CC-942M50-L2KYT

ORDERING INFORMATION FOR STANDARD PRODUCTS

Part Number	Description	Package Type	Options	Order Number
FAR-F5CC-950M00-L2FA	PDC SAW	3.8 X 3.8 MM	1K T&R	F5CC-950M00L2FAT
FAR-F5CC-820M00-L2FB	PDC SAW	3.8 X 3.8 MM	1K T&R	F5CC-820M00L2FBT
FAR-F5CC-915M00-L2JA	ISM SAW (US)	3.8 X 3.8 MM	1K T&R	F5CC-915M00-L2JAT
FAR-F5CC-915M00-L2JZ	ISM SAW (US)	3.8 X 3.8 MM	1K T&R	F5CC-915M00-L2JZT
FAR-F5CC-935M00-L2LA	2-WAY PAGER	3.8 X 3.8 MM	1K T&R	F5CC-935M00L2LAT
FAR-F6CC-1G4410-L2ZA	PDC 1.5 GHz	3.8 X 3.8 MM	1K T&R	F6CC-1G4410-L2ZAT
FAR-F6CC-1G4890-L2ZB	PDC 1.5 GHz	3.8 X 3.8 MM	1K T&R	F6CC-1G4890-L2ZBT
FAR-F6CC-1G6190-L2ZN	PDC 1.5 GHz	3.8 X 3.8 MM	1K T&R	F6CC-1G6190-L2ZBT
FAR-F6CE-1G7475-L2YA	DCS 1800	3 X 3 MM	1K T&R	F6CE-1G7475-L2YAT
FAR-F6CE-1G8425-L2YB	DCS 1800	3 X 3 MM	1K T&R	F6CE-1G8425-L2YBT
FAR-F6CE-1G8800-L2XA	PCS SAW (US)	3 X 3 MM	1K T&R	F6CE-1G8800-L2XAT
FAR-F6CE-1G9600-L2XB	PCS SAW (US)	3 X 3 MM	1K T&R	F6CE-1G9600-L2XBT
FAR-F6CE-2G4500-L2WA	LAN 2.4 GHz	3 X 3 MM	1K T&R	F6CE-2G4500-L2WAT
POWER MANAGEMENT				
MB3802	PWR MGMT SW	FPT-16P-M04		MB3802PF
MB3807A	PWR MGMT SW	FPT-16P-M04		MB3807APF

SECTION 12

Sales Information

12

Introduction to Fujitsu

Fujitsu Limited (Japan)

Fujitsu Limited was founded as a telecommunications equipment manufacturer in 1935, and today is not only one of Japan's leading telecommunications companies, but also one of the world's largest computer manufacturers.

This leadership has resulted, at least in part, form the superb quality of the company's semiconductors and electronic components. Manufactured by the company's Electronics Devices Operations Group, these vital electronic devices also contribute to the high reliability and performance of products made by many other manufacturers around the world.

Today, Fujitsu is one of the world's top manufacturers of semiconductors and electronic components. In Japan, Fujitsu's R&D laboratories for semiconductor and electronic components are situated in Kawasaki and Mie, and manufacturing works are located in Iwate, Aizu, Wakamatsu and Suzaka. Fujitsu also has six affiliated manufacturing works in the country. Overseas facilities in the U.S., Europe, and Asia also help to meed the growing global demand for Fujitsu semiconductors and electronic components.

Fujitsu enforces strict quality control at all stages of production, from materials selection through manufacturing to final testing. As a result, Fujitsu's electronic devices are known for their extremely high reliability and excellent cost-to-performance ratio.

Fujitsu manufactures a full line of semiconductors and electronic components to meet the diverse applications of am wide variety of customers. Backed by Fujitsu's extensive R&D commitment equal to over 10 percent of annual sales, Fujitsu's electronic devices stay on the cutting edge of electronics technology.

Fujitsu Limited

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MIKROELEKTRONIK GmbH
Am Siebenstein 6-10,
63303 Dreieich-Buchschlag,
Germany
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Telex: 411963
FAX: (06103) 690-122

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MICROELECTRONICS ASIA
PTE LIMITED
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Telex: 55573
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408/432-9045
HERZING: 408/943-1204

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COLORADO

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Thornton, CO 80241
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Norcross, GA 30092
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MASSACHUSETTS

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MINNESOTA

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NEW YORK

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OREGON

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TEXAS

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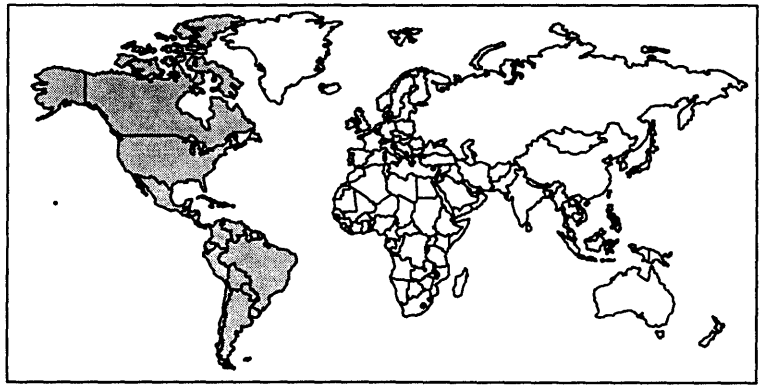
Houston
Two Chasewood Park, Ste. 250
20405 SH 249
Houston, TX 77070
Tel: 713/379-3030
FAX: 713/379-1059



FMI Sales Representatives — USA

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15230 N. 75th Street, Ste. 1031
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619/535-9300
FAX: 619/550-3707

26560 W. Agoura Road,
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818/880-6480
FAX: 818/880-1922

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1267 Oakmead Parkway
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408/733-7707
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8880 Wagon Way
Granite Bay, CA 95746
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2924 Robidoux Road
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FAX: 801/943-9522

IDAHO

Intermountain Technical Marketing
1310 E. First Street
Meridian, ID 83642
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OREGON

L-Squared Limited
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FAX: 513/890-5191

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Stow, OH 44224
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FAX: 619-587-1380

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9320 Telstar Avenue
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FAX: 407-834-6461

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FAX: 407-767-8676

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FAX: 305-977-4887

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813-573-0069

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FAX: 617-270-3279

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FAX: 508-435-6516

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FAX: 508-658-7608

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Milgray Electronics
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FAX: 410-730-8940

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FAX: 612-559-8321

Insight Electronics
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St. Louis Park, MN 55416
612-525-9999
FAX: 612-525-9998

MISSOURI

Marshall Industries
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FAX: 314-770-1486

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Marshall Industries
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FAX: 919-872-8851

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201-777-4100
FAX: 201-777-6194

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Marlton, NJ 08053
609 985-5556
FAX: 609-985-5895

Interface Electronics
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Marlton, NJ 08053
609-988-5448
FAX: 609-988-5566

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101 Fairfield Road
Fairfield, NJ 07004
201-882-0320
FAX: 201-882-0095

158 Gaither Drive #100
Mt. Laurel, NJ 08054
609-234-9100
FAX: 609-778-1819

Milgray Electronics
3001 Greentree Executive
Campus, Ste. C
Marlton, NJ 08053-1551
609-983-5010
FAX: 609-985-1607

3799 Route 46 East, Ste. 303
Parsippany, NJ 07054-1273
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FAX: 201-335-2110

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1056 West Jericho Turnpike
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FAX: 516-543-2030

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607-785-2345
FAX: 607-785-5546

1250 Scottsville Road
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FAX: 716-235-0052

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FAX: 716-381-9495

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FAX: 216-520-4322

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30700 Bainbridge Road, Unit A
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FMI Distributors — USA (continued)

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FAX: 503-641-0650

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Insight Electronics
11500 Metric Blvd., Ste. 215
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10777 Westheimer, Ste. 1100
Houston, TX 77042
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1778 N. Plano Road, Ste. 320
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10681 Haddington Drive,
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1551 N. Glenville Drive
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SECTION 13

Glossary

13

Wireless Communications Glossary

This section contains definitions for terms and phrases which are commonly used in discussions of wireless communications.

On the next page, we include a list of acronyms which are associated with wireless communications, as well as acronyms which are specific to Fujitsu's corporate structure or wireless product line. Following the list of acronyms is the definitions portion of the glossary.

AGC	Automatic Gain Control
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone System
ANSI	American National Standards Institute
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude Shift Keying
BiCMOS	Bipolar/Complementary Metal Oxide Semiconductor
B–PCS	Broadband Personal Communications Systems
CAGR	Compound Annual Growth Rate
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder/Decoder
CT1	Cordless Telephone – First Generation
CT2	Cordless Telephone – Second Generation
CTIA	Cellular Telephone Industry Association
DBS	Direct Broadcast Satellite
DCS1800	Digital Communication Service at 1800 MHz
DECT	Digital European Cordless Telephone
DQPSK	Differential Quadrature Phase Shift Keying
DSP	Digital Signal Processing
DSSS	Direct Sequence Spread Spectrum
ESPER	Emitter-Base Self-Aligned Polysilicon Electrode and Resistor
ETACS	Enhanced Total Access Communications System
ETSI	European Telecommunication Standards Inst.
FAI	Fujitsu America, Inc.
FBCS	Fujitsu Business Communication Sys., Inc.
FCC	Federal Communications Commission
FCPA	Fujitsu Computer Products of America, Inc.
FCPT	Fujitsu Computer Packaging Tech., Inc.
FCSI	Fujitsu Compound Semiconductor, Inc.
FDD	Frequency Division Duplexing
FDMA	Frequency Division Multiple Access
FHSS	Frequency Hopping Spread Spectrum
FJ	Fujitsu Japan
FM	Frequency Modulation
FMG	Fujitsu Microelectronics, GmbH
FMI	Fujitsu Microelectronics, Inc.
FML	Fujitsu Microelectronics, Ltd.
FNI	Fujitsu Networks Industry, Inc.
FNSA	Fujitsu Network Switching of America, Inc.
FNTS	Fujitsu Network Transmission Systems, Inc.
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GHz	Gigahertz
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning Satellite System
GSM	Global System for Mobile Communications (also known as Groupe Speciale Mobile)
IF	Intermediate Frequency
IS–54	Interim Standard Number 54
IS–95	Interim Standard Number 95
IS–136	Interim Standard Number 136
ISM	Industrial, Scientific, and Medical
JDC	Japanese Digital Cellular
kHz	Kilohertz
LAN	Local Area Network
LiTaO3	Lithium Tantalate
LNA	Low Noise Amplifier
LO	Local Oscillator
MCM	Multi-Chip Module
MHz	Megahertz
NF	Noise Figure
NMT	Nordic Mobile Telephone
N–PCS	Narrowband Personal Communications Systems
PA	Power Amplifier
PBX	Private Business Exchange
PC	Personal Computer
PCB	Printed Circuit Board
PCMCIA	PC Memory Card Interface Association
PCN	Personal Communications Network
PCS	Personal Communications System
PHS	Personal Handiphone System

PLL	Phase Lock Loop
PM	Phase Modulation
PQFP	Plastic Quad Flat Pack
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QFP	Quad Flat Pack
QPSK	Quadrature Phase Shift Keying
R&D	Research and Development
RF	Radio Frequency
SAW	Surface Acoustic Wave
SMR	Specialized Mobile Radio
TACS	Total Access Communications System
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
U–PCS	Unlicensed Personal Communications Systems
VCO	Voltage Controlled Oscillator
WAN	Wide Area Network
WLAN	Wireless Local Area Network

Terms and Phrases Associated with Wireless

Advanced Mobile Phone Service (AMPS)
The standard for analog cellular telephone service in the United States.

Amplitude Modulation (AM)
A method of analog modulation where the input data signal is used to vary the amplitude of the carrier.

Amplitude Shift Keying (ASK)
A method of digital modulation where the digital input data signal is used to vary the amplitude of the carrier. Very popular with remote car alarm applications.

Antenna
A device which converts electromagnetic radiation in the form of radio waves into an electrical signal, and vice versa.

Baseband controller
A CMOS or BiCMOS circuit which controls the operation of the analog sections of the radio. The baseband controller acts as the interface between the analog portion of the radio and the digital data and control functions. It is often an ASIC implementation.

Broadband Personal Communication Service (B-PCS)
A standard under development in the United States to provide digital wireless service in a manner similar to cellular telephony, in that the service will be available from infrastructure developed and operated by third-party companies. The system will provide wireless voice, data, and eventually video communication capability.

Cellular telephony
A wireless telephone service which allows a user to make and receive calls while driving, walking, or remaining stationary. This is accomplished via an infrastructure which has a number of base station antenna sites arrayed in such a way to create a number of individual 'cells' which cover a specified geographic area. The infrastructure allows users to move from cell to cell during a call by transferring the radio connection to the user's cellular telephone from one base station to another. This infrastructure is established by a third party, and a user must subscribe to the service and pay both monthly and air time charges to access the infrastructure.

Charge pump
A component of a phase lock loop system which produces pulses of electrical current. The polarity of the current and the time duration of the pulse are controlled by the phase detector. The output of a charge pump serves as the input to the loop filter of a PLL system.

Code Divided Multiple Access (CDMA)
A type of multiplexing for wireless systems developed by Qualcomm which uses spread spectrum techniques to allow many users to share the same frequency bands simultaneously.

Compression point (P1dB)
The maximum input signal strength that an amplifier can amplify in a linear manner.

Conversion gain
A measure of the gain of a mixer, measured from the signal input port to the output port.

Cordless Telephone – Second Generation (CT2)
A digital cordless telephone standard developed in France and Britain for residential and office use. Also very popular in Hong Kong and other Far East countries.

Cordless telephony
A cordless telephone is a device which serves the same basic function as an ordinary telephone, but without the restriction of a cord. They have a limited range of service, and are intended for use in and around the home. Cordless telephones do not require third party infrastructure or subscriber fees.

Differential Quadrature Phase Shift Keying (DQPSK)
A modified form of quadrature phase shift keying which offers a slight improvement in performance.

Digital Communications Service at 1800 MHz (DCS-1800)
A modification of the GSM protocol to allow operation at 1800 MHz for European PCS applications.

Terms and Phrases Associated with Wireless (Continued)

Digital Communications Service at 1900 MHz (DCS-1900)
A modification of the GSM protocol to allow operation at 1900 MHz. This is one of several proposed standards for broadband PCS and unlicensed PCS in the United States.

Digital European Cordless Telephone (DECT)
A standard for digital cordless telephones which is adopted throughout Europe. Originally designed for office applications, it has voice and data capability inherent to the standard. It is now becoming more common for residential use as well.

Direct Conversion Receiver
A radio receiver architecture where the local oscillator frequency is set equal to the carrier frequency of the signal of interest. This produces an output signal which is centered at 0 Hz, which means that the signal is directly converted to its baseband representation. This architecture is used most commonly in pagers. Also known as a homodyne receiver.

Dual Conversion Receiver
A radio receiver architecture which uses two frequency conversions (via two separate mixer/local oscillator combinations). Dual conversion receivers generally give superior performance, but at the expense of extra component count and cost. Also known as a dual superheterodyne receiver.

Dual modulus prescaler
A prescaler which has two distinct divide ratios. The choice of divide ratio is determined by a control input to the prescaler which is generated by the swallow counter of a PLL IC.

Duplexer
A device which is used in systems which utilize frequency division duplexing. It consists of two filters, one for the frequencies used for the received radio signals, and one for the frequencies used for the transmitted radio signals. The duplexer provides the receiver with isolation from interference from the transmitter for radio systems which use the same antenna for both transmit and receive.

Duplexing
The rules which determine how two radios transmit and receive signals to each other.

Dynamic Range
The range of input signal strength that a radio receiver can detect properly. It is bounded on the low end by the noise of the receiver, and on the high end by the distortion and nonlinearity of the receiver.

Frequency Division Duplexing (FDD)
A method of duplexing where a radio transmits on one carrier frequency, and receives on another frequency, so that the transmission and reception do not interfere with each other.

Frequency Division Multiple Access (FDMA)
A type of multiplexing for wireless systems where each radio conversation is assigned a unique carrier frequency exclusively for their use.

Frequency Modulation (FM)
A method of analog modulation where the input data signal is used to vary the frequency of the carrier.

Frequency Shift Keying (FSK)
A method of digital modulation where the frequency of the carrier alternates between two or more discrete frequencies based on the state of the digital input data signal. It is relatively easy and inexpensive to implement, but it has poor spectral efficiency.

Gain
The ratio of the signal strength at the output of a device to the signal strength at its input.

Gaussian Minimum Shift Keying (GMSK)
This is a special, tightly controlled version of frequency shift keying modulation designed for better spectral efficiency. It is the modulation method used for GSM and its derivatives.

Global System for Mobile Communications (GSM)
A standard for digital cellular telephone service which was originally developed for use in Europe. GSM is now being adopted as the digital cellular standard in many areas of the world, with the exception of Japan and the United States.

Terms and Phrases Associated with Wireless (Continued)

Low noise amplifier (LNA)
An amplifier used at the input of radio receivers which amplifies the radio frequency signals. LNAs are designed so that they add the smallest possible amount of noise to the received radio signal.

Messaging
A service which is functionally equivalent to wireless electronic mail. Moderate length text messages can be sent and received from a portable device, such as a personal digital assistant.

Mixer
A device which multiplies two input signals together. It is used in conjunction with a local oscillator to perform frequency translations on radio signals.

Multiplexing
The means by which wireless communication systems accommodate many users simultaneously.

Narrowband Advanced Mobile Phone Service (N-AMPS)
A modification to the AMPS cellular telephone standard in the United States which reduces the bandwidth of a frequency channel by a factor of three, thus increasing the capacity of a cellular system threefold.

Narrowband Personal Communication Service (N-PCS)
A standard which is being deployed in the United States which provides advanced digital messaging services, such as 2-way paging.

Noise
Random electrical signals which are generated in all electrical circuits. Excessive levels of noise prevent radios from detecting input signals with low signal strengths.

Noise Figure (NF)
A measure of the amount of noise that an amplifier or mixer adds to the input signal.

Nordic Mobile Telephone (NMT)
One of the first analog cellular systems developed, now in use in Norway, Sweden, Finland, and a number of other countries.

Paging
A basic form of wireless communication which allows a user to be notified, via a beeping sound from a small radio receiver known as a pager, that someone is trying to contact them. More sophisticated paging products have an alphanumeric display which allows small text messages to be sent to the user. Conventional pagers are receive-only devices, and do not contain a transmitter of any kind.

Passband
The input signal frequencies which a filter allows to pass through to its output.

Personal Communications Network (PCN)
see Personal Communications System

Personal Communications System (PCS)
A generic classification of digital wireless communications services which are under development in both the United States, Europe, and Japan. PCS is envisioned as a means to provide a ubiquitous "anytime, anywhere" communication service for voice, data, messaging/ paging, and eventually compressed video.

Phase detector
A component of a phase lock loop system which compares the relative placement in time of the positive edges of its two input signals. The results of this comparison are used to control the charge pump of a PLL system.

Phase lock loop (PLL)
A circuit which generates an output signal whose phase and frequency characteristics are controlled by an input reference signal. A basic PLL system consists of a reference signal, a phase detector, a charge pump, a loop filter, and a voltage controlled oscillator (VCO). Almost all PLL systems also include programmable counters and prescalers which allow the output frequency of the PLL to be set to a non-integer multiple of the reference signal.

In integrated circuit terms, a PLL refers to the integration of the phase detector, charge pump, programmable counters, and in some cases the prescaler, onto one IC. This is also known as a synthesizer.

Terms and Phrases Associated with Wireless (Continued)

Harmonics
Signals at frequencies which are integer multiples of the frequency of a sinusoidal signal. Harmonics are caused by nonlinearities in amplifiers and mixers which distort the fundamental signals.

Homodyne Receiver
see Direct Conversion Receiver

IF filter
A filter which is used on radio signals which have been converted down to an intermediate frequency. The IF filter has a passband width equal to the bandwidth of an individual frequency channel for the application. The IF filter selects which frequency channel will be demodulated by the radio.

Image filter
A filter used at the input of radio receivers which allows only the relevant frequencies for that application to pass through, and rejects all other frequencies.

Industrial, Scientific, and Medical (ISM)
Radio frequency bands available in the United States and some parts of Europe for unlicensed radio operation. The ISM bands are commonly used for digital cordless telephones and wireless local area networks (WLANs). Most applications using the ISM bands utilize spread spectrum techniques. The three ISM bands available in the US are 902–928 MHz, 2.4–2.483 GHz, and 5.725–5.85 GHz.

Insertion loss
A measure of how much signal strength is lost on signals within the passband of a filter.

Interim Standard 54 (IS-54)
see Interim Standard 136.

Interim Standard 95 (IS-95)
One of two competing standards for digital cellular telephone service in the United States. This standard specifies the use of code division multiple access (CDMA) as the method of multiplexing. This standard was originally developed by Qualcomm.

Interim Standard 136 (IS-136)
One of two competing standards for digital cellular telephone service in the United States. This standard, formerly known as IS-54, specifies the use of time division multiple access (TDMA) as the method of multiplexing. This standard was originally developed by a consortium of cellular service providers and equipment manufacturers led by Motorola.

Intermediate frequency (IF)
The frequency that the high frequency radio signal is translated to by the mixer and local oscillator.

Interstage filter
An interstage filter is used to filter signals between stages of a power amplifier. They are used to filter out any harmonics which may be generated by distortions in the power amplifier.

Japanese Digital Cellular (JDC)
The standard for digital cellular telephones in Japan. Also known as RCR-27.

Local oscillator (LO)
A pure sinusoidal signal which is used in conjunction with a mixer to perform precise frequency translations on radio signals. The local oscillator signal is often generated by using a voltage controlled oscillator (VCO) which is controlled by a phase lock loop (PLL). The tuning of a radio to a specific frequency channel is accomplished by setting the frequency of the LO to an appropriate value.

Lock time
The time that a phase lock loop takes to change its output frequency and have it become locked to the reference signal.

Loop bandwidth
A measure of how quickly a phase lock loop responds to keep its output signal locked to the reference signal.

Loop filter
A component of a phase lock loop system which converts the pulses of electrical current from the output of the charge pump into a voltage which is used as the input to a voltage controlled oscillator.

Terms and Phrases Associated with Wireless (Continued)

Phase noise
A measure of how much a fixed frequency oscillator signal varies in frequency due to the effects of random noise in the oscillator circuit.

Power amplifier (PA)
This device takes a modulated transmit signal at the RF frequency and amplifies it to a level which is appropriate to drive the antenna. It is often implemented as a series of amplifier stages.

Prescaler
A device which takes the high frequency output signal from a VCO and divides the frequency down to a value which can be used as an input to the program counter divider portion of a PLL.

Program counter (N-counter)
A component of a phase lock loop system which divides the output frequency of the voltage controlled oscillator, usually after it has already been divided by a prescaler, before presenting it as an input to the phase detector. The amount of frequency division performed by the program counter can be altered by programming the counter with a different value, which will result in a course change in the output frequency of the PLL system.

Quadrature Amplitude Modulation (QAM)
A complex method of digital modulation where the input data signal controls both the amplitude and phase of the carrier. It is difficult and expensive to implement, but is one of the most spectrally efficient form of modulation.

Quadrature modulator
A device which is used in radios which utilize complex digital modulation techniques such as QPSK and QAM. It takes a local oscillator signal and splits it into two components, identical in frequency but separated in phase by 90 degrees. These two signals are then modulated by two separate input signals (the I and Q data signals), and the resulting modulated signals are then combined into one signal and fed into a mixer to be upconverted in frequency to the proper RF frequency.

Quadrature Phase Shift Keying (QPSK)
A method of digital modulation where the phase of the carrier takes on one of four possible values, corresponding to the state of two digital input data bits which control the modulation. It is a popular form of modulation because it represents a good compromise of ease of implementation and spectral efficiency.

Reference counter (R-counter)
A component of a phase lock loop system which divides the frequency of the reference signal before presenting it as an input to the phase detector. Changing the value that is stored in the reference counter results in a change in the size of the frequency steps that the PLL output frequency can make.

Reference signal
The external signal used by a phase lock loop system as the reference from which the output signal of the PLL is derived.

Specialized Mobile Radio
Private, licensed mobile radio networks commonly used for dispatching services for taxis, delivery companies, etc.

Spectral Efficiency
A measure of the data rate which can be sent per 1 Hz of bandwidth. Units are in bits per second per Hz (bps/Hz). The greater the spectral efficiency, the greater the channel capacity.

Spread spectrum
A technique developed for military communications which essentially "spreads" a narrow bandwidth radio signal over a wide frequency band in order to make the signal less susceptible to interference. It is also used to improve the security of a wireless data transmission, as it is difficult to intercept.

Spurious signals, spurii
Unwanted signals at frequencies other than the desired frequency. Spurii result from the operation of a phase lock loop (due to the inherent operation of the phase detector), and from unwanted mixer output signals.

Stopband
The input signal frequencies which a filter prevents from passing through to its output.

Terms and Phrases Associated with Wireless (Continued)

Swallow counter (A-counter)
A component of a phase lock loop system which works in conjunction with the program counter to control the divide ratio of a dual modulus prescaler. Changing the value programmed in the swallow counter will result in a fine change in the output frequency of the PLL system.

Synthesizer
A common term for an phase lock loop integrated circuit.

Time Division Duplexing (TDD)
A method of duplexing where a radio transmits and receives on the same carrier frequency, but at different times, so that the transmission and reception do not interfere with each other.

Time Division Multiple Access (TDMA)
A type of multiplexing for wireless systems where multiple radios use the same carrier frequency, but only in certain specified timeslots, so that no two radios use the same carrier frequency at the same time.

Time Division Duplexing (TDD)
A method of duplexing where a radio transmits and receives on the same carrier frequency, but at different times, so that the transmission and reception do not interfere with each other.

Unlicensed Personal Communication Service (U-PCS)
A standard under development in the United States to provide digital wireless service in a manner similar to cordless telephony, in that the service will not require access to third-party infrastructure.

Voltage controlled oscillator (VCO)
A device which produces a sinusoidal output signal. The frequency of the output signal is controlled by a voltage at the input to the device.

Wireless Local Area Network (WLAN)
A computer network which allows the transfer of data and the ability to share resources without the need to physically connect each node with wires. Popular with users of portable computers, and in environments where it is impractical to install a wired LAN.

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