Data Book

Dynamic RAM Products

1991

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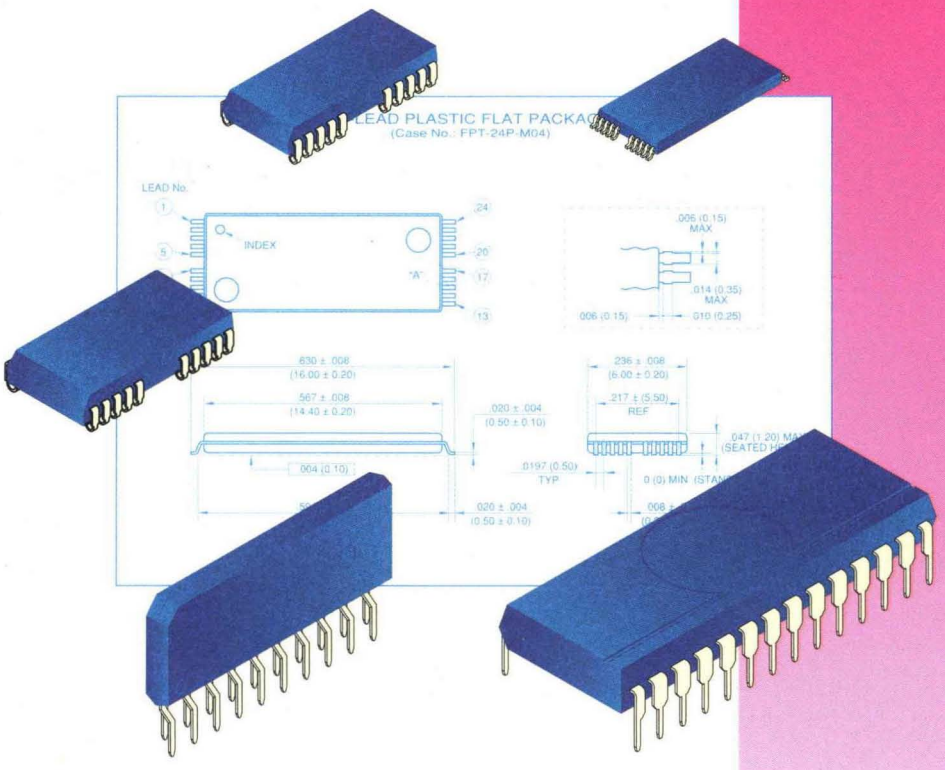

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Dynamic RAM Products

1991
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Fujitsu Limited
Tokyo, Japan

Fujitsu Microelectronics, Inc.
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PREFACE

This data book contains the latest product information for Fujitsu's line of DRAM ICs. This year's edition, however, does not include a section for DRAM modules. Both DRAM and SRAM modules are now in a Modules Data Book which you can obtain from your nearest Fujitsu Sales Office or Sales Rep. (See the Sales Information listing in this book.)

In addition to the collection of DRAM data sheets, you will find valuable information on ordering and expanded packaging descriptions, both in the Order Information section.

The Design Information section contains two new technical papers. *The 3D Stacked Capacitor Cell for Mega Bit DRAM* is a reprint of a technical paper from the **Fujitsu Scientific and Technical Journal**. We are pleased to be able to include an article from this highly respected journal. The second new paper is *The Soft Error Rate for 4M DRAM Devices*, a significant article on these new DRAM devices.

If you are interested in obtaining other Fujitsu product information, you will find the publications listing on the following pages quite useful. Once again, call one of our sales offices to obtain a copy of any of the documents.

FUJITSU PRODUCT PUBLICATIONS

The following is a list of the product publications available from Fujitsu. Call your nearest Fujitsu Sales Office or Sales Representative to order any document(s) you need. (See the Sales Information section for phone numbers.)

MEMORY PRODUCTS

Dynamic RAM Products Data Book	Contains product data sheets for NMOS and CMOS DRAMs, including 1M and 4M devices, and MOS application-specific RAMs.
Static RAM Products Data Book	Contains product data sheets for high-speed CMOS and BiCMOS SRAMs, low-power CMOS SRAMs and application-specific SRAMs.
ECL RAM Products Data Book	Contains product data sheets for ECL and TTL bipolar ECL RAMs, BiCMOS ECL RAMs, and application-specific RAMS including self-timed RAMs (STRAMs).
Programmable Memory Products Data Book	Contains product data sheets for programmable ROMs (including registered and wide-temperature range PROMs); CMOS mask-programmable ROMS, OTP ROMs, erasable PROMs, and EE-PROMs; NMOS erasable PROMs and non-volatile RAMs.
Memory Modules Data Book	Contains product data sheets for CMOS DRAM modules (including high density and low profile) and CMOS SRAM modules.
Memory Card Products Data Book	Contains product data sheets and programming information for 68-pin JEIDA and PCMCIA standard memory cards and connectors and for 38-pin memory cards.
Power Transistor Products Data Book	Contains product data sheets for RETs, Darlington arrays, and FETs.
Linear Products Data Book	Contains product data sheets for op amps, comparators, automotive audio amps, power supply controls, motor drivers, disk drivers, and converters (A/D, D/A, A/D-D/A, and F/V).
Linear Products Selector Guide	Presents an overview of linear products.
Telecommunication Devices Data Book	Contains product data sheets for bipolar prescalers and VCOs, CMOS PLLs, BiCMOS single-chip PLLs and Prescalers, CODECs, CMOS telephone ICs, and cellular mobile radio ICs.
Telecommunication Devices Selector Guide	Presents an overview of telecommunication products and piezoelectric devices.
Interface and Logic Products Selector Guide	Presents an overview of logic and interface devices.
CMOS 4-bit Microcontrollers Data Book, Vol. I	Contains product information, including the development tool for the MB8850 and MB88200 families of 4-bit microcontrollers.
CMOS 4-bit Microcontrollers Data Book, Vol. II	Contains product information, including the development tool for the MB88500 family of 4-bit microcontrollers.
CMOS 4-bit Microcontrollers Selector Guide	Presents an overview of the MB88500 (high end), MB8850 (mid-range), and MB88200 (low end) families of 4-bit microcontrollers.

FUJITSU PRODUCT PUBLICATIONS (Continued)

ASIC PRODUCTS

CMOS Channeled Gate Arrays Data Book and Design Evaluation Guide	Contains product information for UHB Series High Drive CMOS Gate Arrays and CG10 Series High Drive CMOS Gate Arrays.
CMOS Channelless Gate Arrays Data Book and Design Evaluation Guide	Contains product information for AU Series CMOS Series Gate Arrays and CG21 Series CMOS Gate Arrays.
CMOS Standard Cell Data Book and Design Evaluation Guide	Contains product information for AU Series Standard Cells.
ASIC CMOS Products Selector Guide	Presents an overview of CMOS channeled and channelless gate arrays and standard cell products.
BiCMOS Gate Arrays Data Book and Design Evaluation Guide	Contains product information for BC Series BiCMOS Gate Arrays and BC-H Series BiCMOS Gate Arrays.
ECL Gate Arrays Data Book and Design Evaluation Guide	Contains product information for ET Series ECL Gate Arrays, H Series ECL Gate Arrays, Ultra-High Performance ECL Gate Arrays, and VH Series ECL Gate Arrays.
ASIC Bipolar Products Selector Guide	Presents an overview of BiCMOS and ECL gate array products.

ASIC SOFTWARE

The ASIC Gallery (catalog)	Discusses the trend in ASICs: migration from using gates as primitives to using LSI and even VLSI macros as design elements.
The ASIC Design Environment (catalog)	Provides an overview of the third-party tools that work in concert with Fujitsu's proprietary tools, ViewCAD™, BankCAD™, ZephCAD, and FAME. Also included are product profiles explaining how the third-party tools fit within the design framework.
ViewCAD User's Guide	Provides a basic understanding of Fujitsu's proprietary CAD/CAE system, ViewCAD. This book provides information necessary to design, test, simulate, and analyze circuits using Fujitsu's unit cell libraries for AU, UHB, CG10, CG21, and CG31 CMOS technologies.
ViewCAD Installation Guide	Explains how to install Fujitsu's proprietary CAD/CAE system, ViewCAD.
CMOS ASIC Reference Manual for Validation	Provides a basic understanding of the Valid System on the Sun platform as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries for AU and UHB CMOS technologies.
FAME User's Guide	Provides a basic understanding of the Fujitsu ASIC Management Environment (FAME) software as it interfaces with third-party tools (Sun or PC) to build circuits using Fujitsu's unit cell libraries.
FAME Reference Manual	Provides installation and directory information for the Fujitsu ASIC Management Environment (FAME) software, which uses third-party tools (Sun or PC) to build circuits using Fujitsu's unit cell libraries.
Synopsys User's Guide	Provides a basic understanding of the Synopsys® system as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries.

FUJITSU PRODUCT PUBLICATIONS (Continued)

ASIC SOFTWARE (Continued)

Verilog-XL User's Guide	Provides a basic understanding of the Verilog-XL® system as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries.

Future Publications

For Fujitsu Microelectronics, Inc.:

Master Product Guide/Catalog (1991)	Presents an overview of the entire range of products offered by Fujitsu Microelectronics.

For Memory Products:

Hybrid Products (1991)	Presents Fujitsu's hybrid products and discusses thick- and thin-film capabilities.

For ASIC Software:

ASIC Design Environment Data Book (1991)	Provides detailed information about the ASIC Design Methodology at Fujitsu. It contains an overview of the third-party tools that work in concert with Fujitsu's proprietary tools, ViewCAD, BankCAD, ZephCAD, and FAME. Also included are product profiles explaining how the third-party tools fit within the design framework.
ASICOpen™ Catalog (1991)	Provides a small-scale ASIC Design Methodology at Fujitsu. It explains the design processes between two third-party tools, Synopsys and Verilog-XL, and Fujitsu's proprietary tools, ViewCAD, BankCAD, and ZephCAD.

Contents and Alphanumeric Product List

DRAM PRODUCTS

Contents and Alphanumeric Product List (Continued)

DRAM PRODUCTS

Contents and Alphanumeric Product List (Continued)

DRAM PRODUCTS

Alphanumeric List of Fujitsu Part Numbers

Introduction

Fujitsu's Dynamic RAM Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high–speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic RAMs. An extensive line of memory products includes volatile and non-volatile CMOS and ECL devices.

Fujitsu's Dynamic RAM product line offers devices for use in a wide range of applications. These memories are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

This data book includes product information on all of Fujitsu's currently available DRAM products.

NMOS and CMOS DRAMs

Fujitsu manufactures a complete family of leading technology dynamic random access memories for the data processing, telecom, and industrial markets. This family consists of the highest density devices currently available with a broad selection of organizations, access modes, and packages.

Application-Specific DRAMs

Fujitsu offers a family of multi-port dynamic random access memories tailored for video imaging and graphics applications. These devices adhere to JEDEC standards where applicable and are available in the popular packages.

NMOS DRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options		
1–3	MB81256–10	100	262144 bits	16-pin	Plastic	DIP, ZIP
	–12	120	(262144 x 1)	16-pin	Ceramic	DIP
	–15	150		18-pin	Plastic	PLCC
				18-pad	Ceramic	LCC
1–25	MB81256-80	80	262144 bits	16-pin	Plastic	DIP, ZIP
			(262144 x 1)	16-pin	Ceramic	DIP
				18-pin	Plastic	PLCC
1–45	MB81257–10	100	262144 bits	16-pin	Plastic	DIP, ZIP
	–12	120	(262144 x 1)	16-pin	Ceramic	DIP
	–15	150		18-pin	Plastic	PLCC
				18-pad	Ceramic	LCC
1–69	MB81257-80	80	262144 bits	16-pin	Plastic	DIP, ZIP
			(262144 x 1)	16-pin	Ceramic	DIP
				18-pin	Plastic	PLCC
1–93	MB81464–12	120	262144 bits	18-pin	Plastic	DIP, PLCC
	–15	150	(65536 x 4)	18-pin	Ceramic	DIP
				20-pin	Plastic	ZIP

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DATA SHEET

MB81256-10/-12/-15

MOS 262,144 BIT DYNAMIC RANDOM ACCESS MEMORY

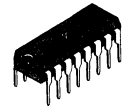
262,144 Bit Dynamic Random Access Memory

The Fujitsu MB81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and environments where low power dissipation and a compact layout are required.

Multiplexed row and column address inputs permit the MB81256 to be housed in standard 16-pin DIP and ZIP packages or an 18-pin PLCC package. Pinouts conform to JEDEC-approved pinouts. Additionally, the MB81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before-$\overline{RAS}$ refresh provides an on-chip refresh capability that is upwardly compatible with the MB8266A. The MB81256 also features page mode which allows high speed random access of up to 512 bits of data within the same row.

The MB81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible.

- 262,144 x 1 RAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time
  100 ns max. (MB 81256-10)
  120 ns max. (MB 81256-12)
  150 ns max. (MB 81256-15)
- Cycle Time
  200 ns min. (MB 81256-10)
  220 ns min. (MB 81256-12)
  260 ns min. (MB 81256-15)
- Page Cycle Time
  100 ns max. (MB 81256-10)
  120 ns max. (MB 81256-12)
  145 ns max. (MB 81256-15)
- Single +5 V Supply, ±10% tolerance
- Low Power
  385 mW max. (MB 81256-10)
  358 mW max. (MB 81256-12)
  314 mW max. (MB 81256-15)
  25 mW max. (standby)
- 256 refresh cycles every 4 ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-white-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} are eliminated
- Output unlatched cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-Pin Plastic Packages:
  DIP (MB81256-XXP)
  ZIP (MB81256-XXPSZ)
  Standard 18-Pin Plastic Package:
  PLCC(MB81256-XXPV)
  Standard 16-Pin Ceramic Packages:
  DIP (MB81256-XXC) Seam Weld
  DIP (MB81256-XXZ) Cerdip
  Standard 18-Pad Ceramic Package:
  LCC (MB81256-XXTV)



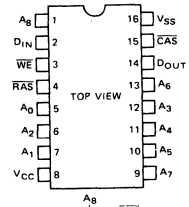
PLASTIC PACKAGE
DIP-16P-M03

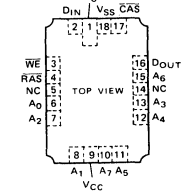
PLASTIC PACKAGE
LCC-18P-M04

PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 17
DIP-16C-A04: See Page 18
DIP-16C-C04: See Page 19
LCC-18C-F04: See Page 24

PIN ASSIGNMENT





Pin assignment for ZIP: See Page 21

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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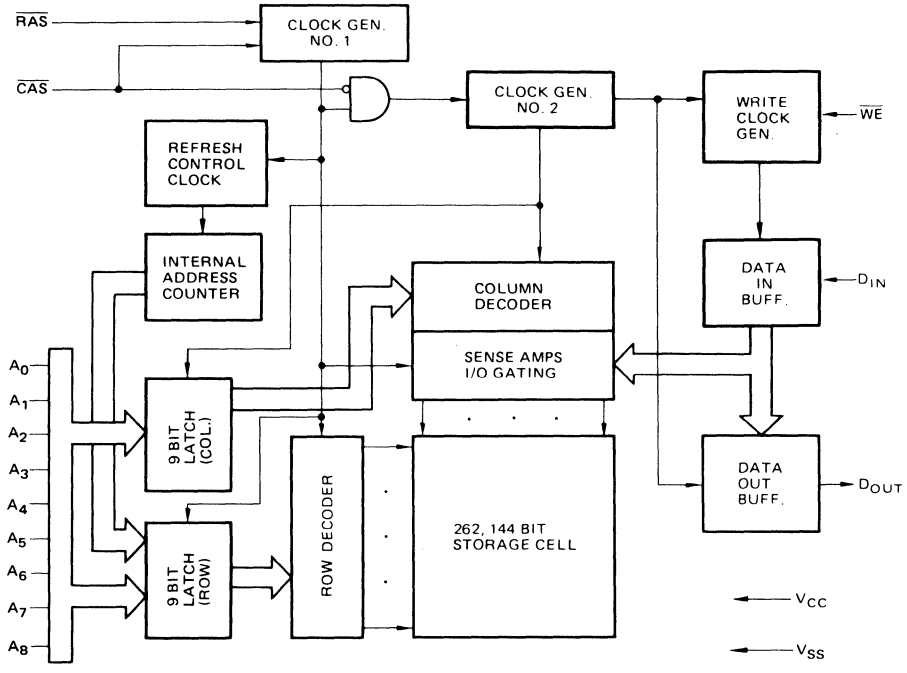
Fig. 1 – MB 81256 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		10	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81256-10	I_{CC1}			70	mA
	MB 81256-12				65	
	MB 81256-15				57	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$=V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81256-10	I_{CC3}			60	mA
	MB 81256-12				55	
	MB 81256-15				50	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	MB 81256-10	I_{CC4}			35	mA
	MB 81256-12				30	
	MB 81256-15				25	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81256-10	I_{CC5}			65	mA
	MB 81256-12				60	
	MB 81256-15				55	
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output high Voltage (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE * : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	MB 81256-10		MB 81256-12		MB 81256-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle Time		t_{RC}	200		220		260		ns
Read-Write Cycle Time		t_{RWC}	200		220		260		ns
Access Time from $\overline{RAS}$	4, 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5, 6	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7, 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		20		ns
Write Command Set Up Time	10	t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 81256-10		MB 81256-12		MB 81256-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Page Mode Read/Write Cycle Time		t_{PC}	100		120		145		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	100		120		145		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	40		50		60		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		375		430		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		60		70		ns

Notes:

1. An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.) If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5ns) + t_{ASC} (min).
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
    If $t_{CWD} \geqq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

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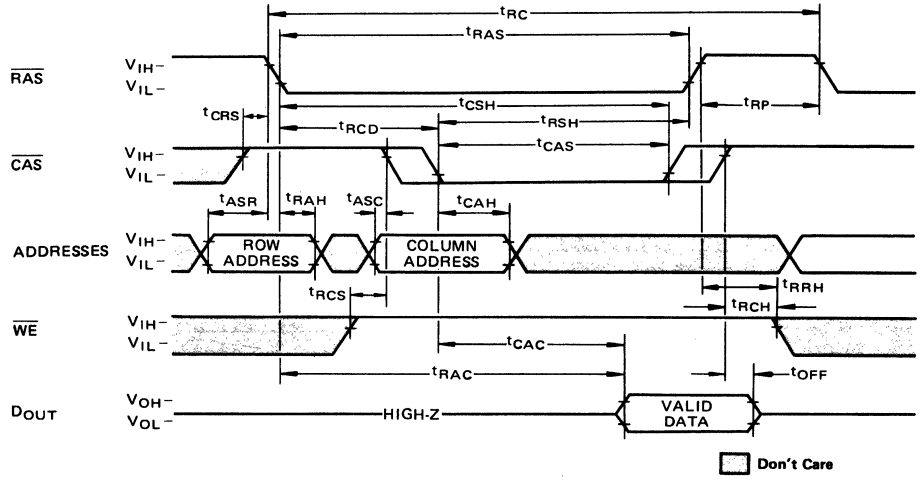
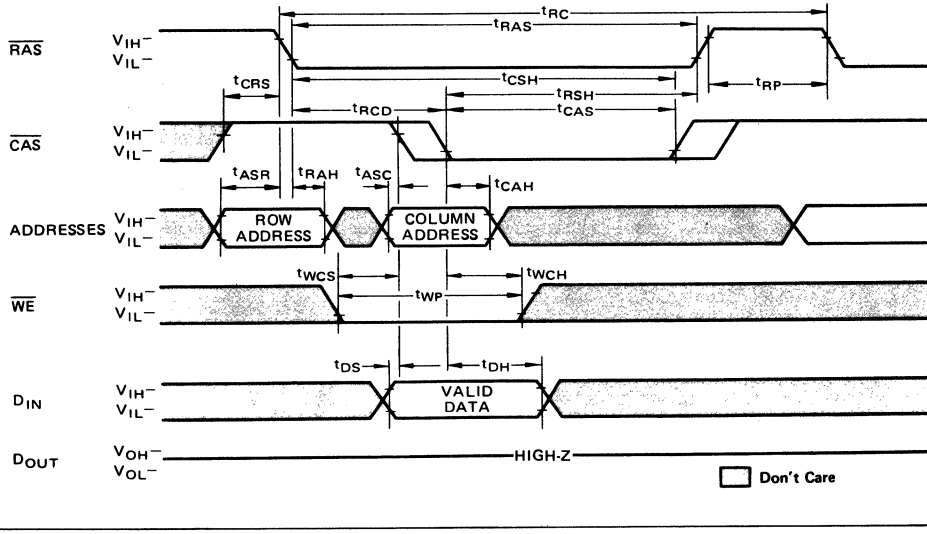
Read Cycle



Write Cycle (Early Write)



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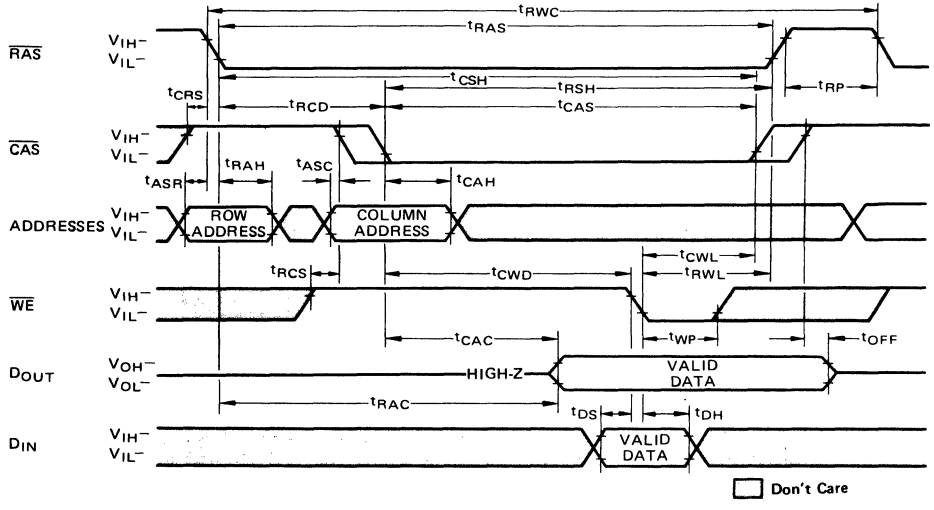
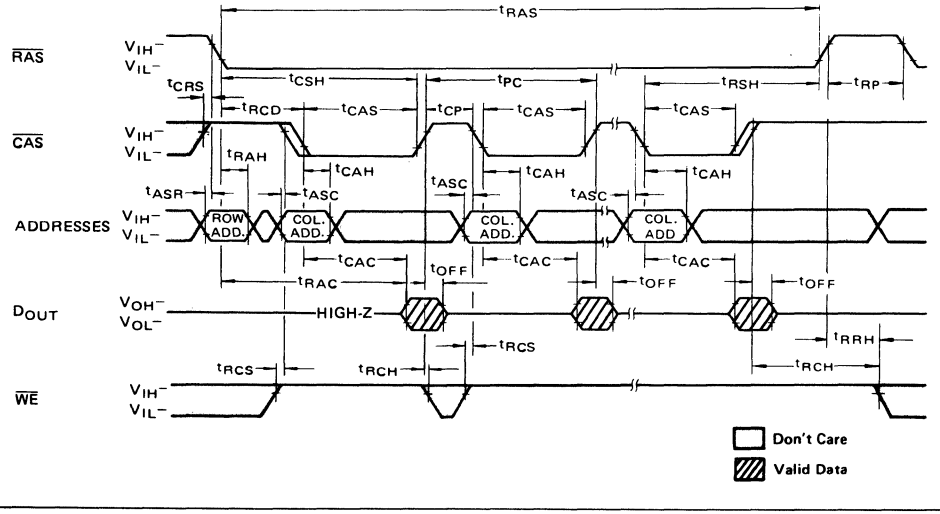
Read–Write/Read–Modify–Write Cycle



Page Mode Read Cycle



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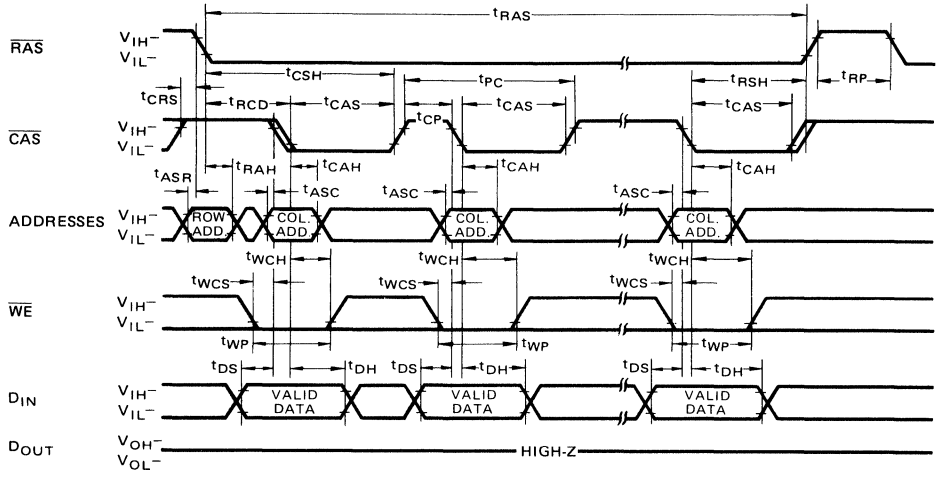
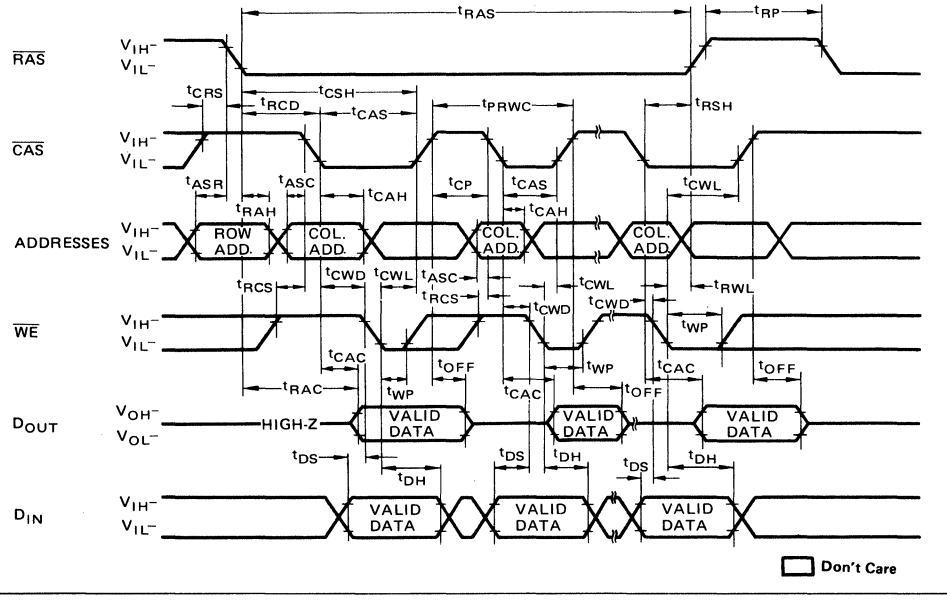
Page Mode Write Cycle

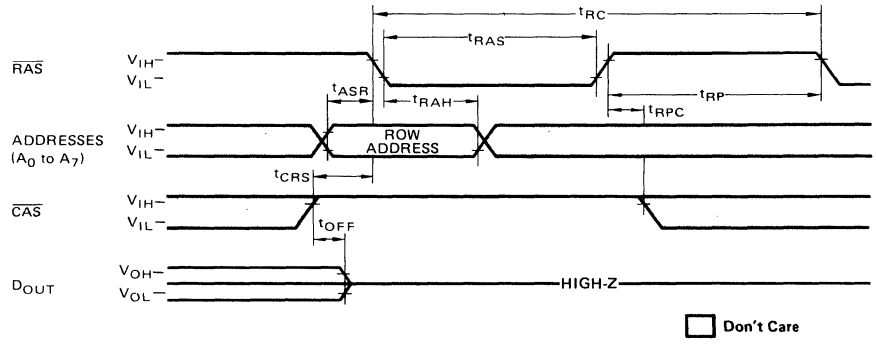


Page Mode Read-Write Cycle



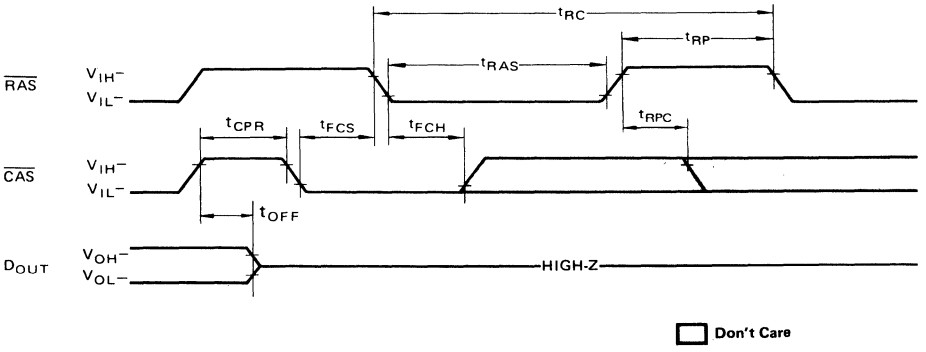
$\overline{RAS}$-only Refresh cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, $A_8 = V_{IH}$ or V_{IL}



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Address, $\overline{WE}$, D_{IN} = Don't care



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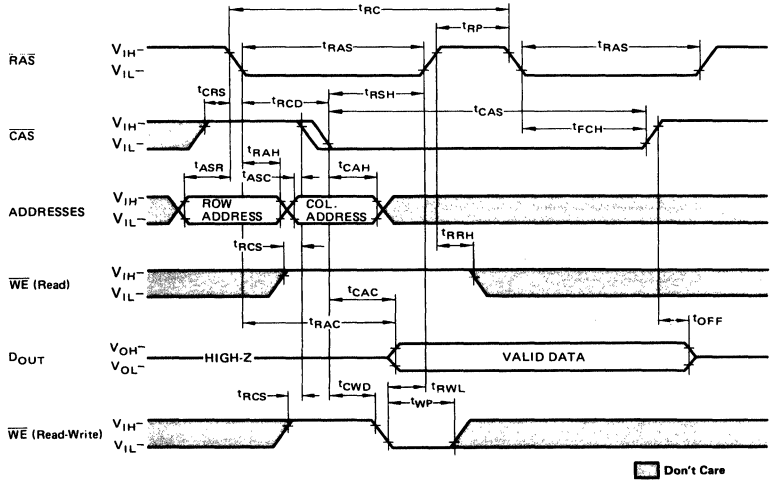
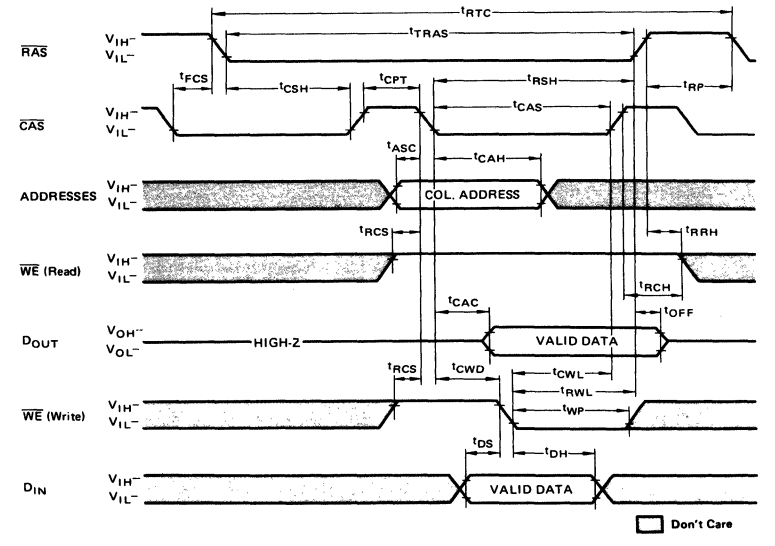
Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement
The MB 81256 has improved circuitry that eases timing requirements for high speed access operations. The MB 81256 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81256 has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ nonrestrictive and deleted them from the data sheet, these include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81256. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode; low selects write mode. The data input is disable when read mode is selected.

Data input:
Data is written into the MB 81256 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle
The MB 81256 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle (t_{RWC} = t_{RC}) is possible with the MB 81256.

Page Mode:
Page-mode operation permits strobing the row-address into the MB 81256 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4ms. The MB 81256 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low.
Strobing each of 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81256 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh;
A hidden refresh cycle may takes place while maintaining the latest valid data at the output by extending $\overline{CAS}$ active time.
For the MB 81256 a hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counters provide the refresh addresses, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-

1

before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.
After the $\overline{CAS}$-befor-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and then goes to low again while $\overline{RAS}$ is held low, the read and write operations are enabled.
This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and column address (9 bits) to be accessed can be defined as follows:

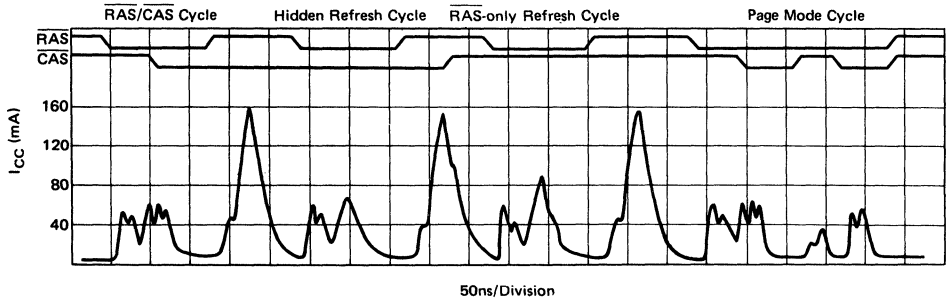
*A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.
*A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test cycles is used for the following operations:

(1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
(2) Throughout the test, use the same column address, and keep RA8 high.
(3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
(4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
(5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
(6) Complement the test pattern and repeat step 3), 4) and 5).

Fig. 2 – CURRENT WAVEFORM (V_{CC}=5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

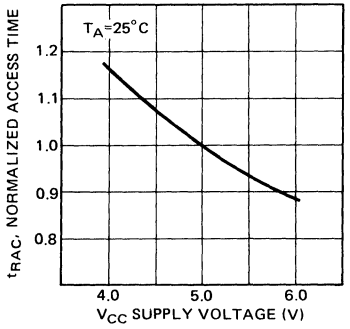


Fig. 4 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

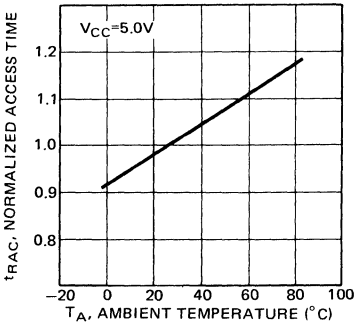


Fig. 5 – OPERATING CURRENT vs CYCLE RATE

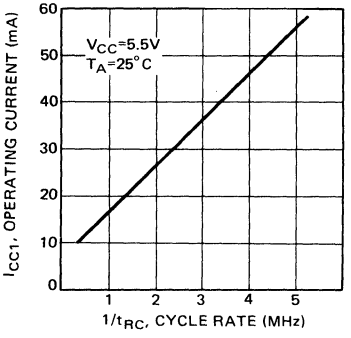


Fig. 6 – OPERATING CURRENT vs SUPPLY VOLTAGE

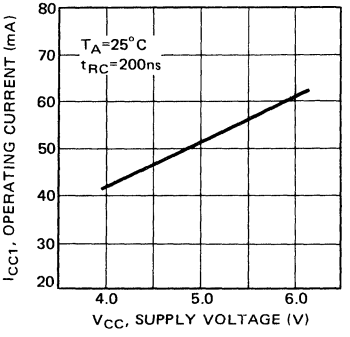


Fig. 7 – OPERATING CURRENT vs AMBIENT TEMPERATURE

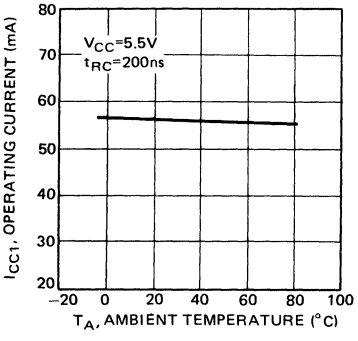


Fig. 8 – STANDBY CURRENT vs SUPPLY VOLTAGE

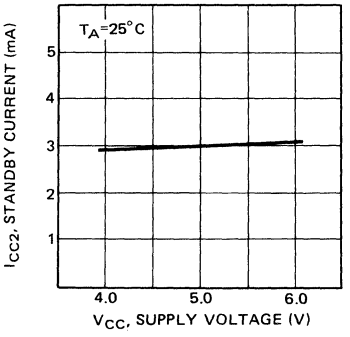


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Fig. 9 – STANDBY CURRENT vs AMBIENT TEMPERATURE

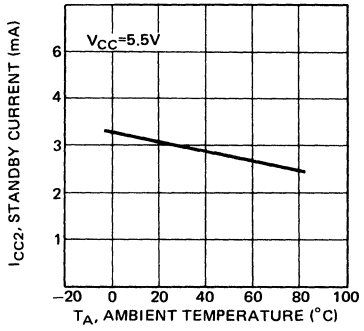

Fig. 10 – REFRESH CURRENT 1 vs CYCLE RATE

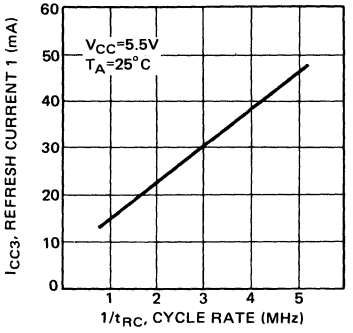

Fig. 11 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

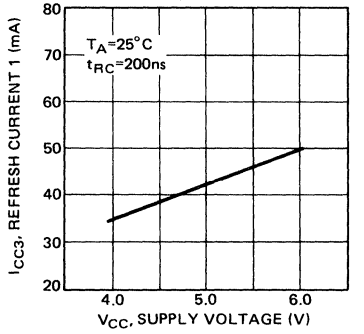

Fig. 12 – PAGE MODE CURRENT vs CYCLE RATE

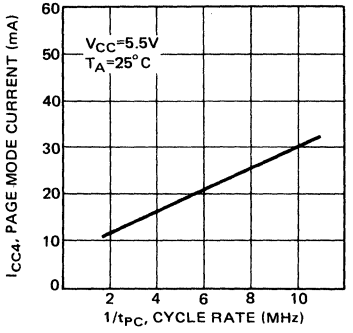

Fig. 13 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

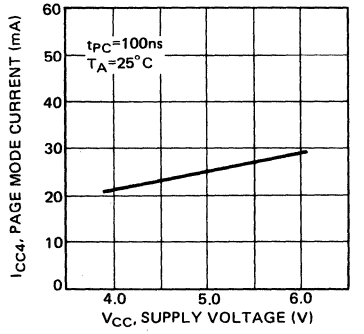

Fig. 14 – REFRESH CURRENT 2 vs CYCLE RATE

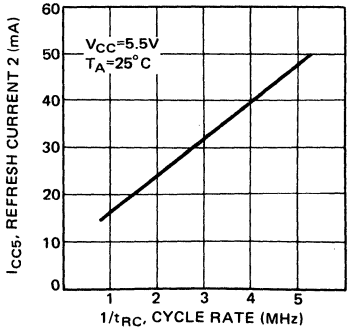

Fig. 15 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

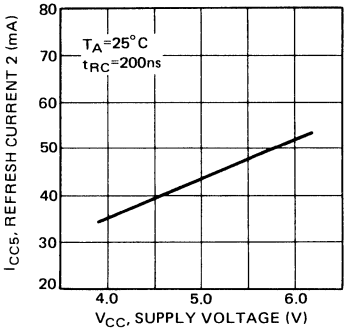

Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

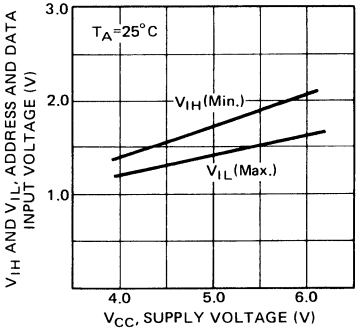

Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

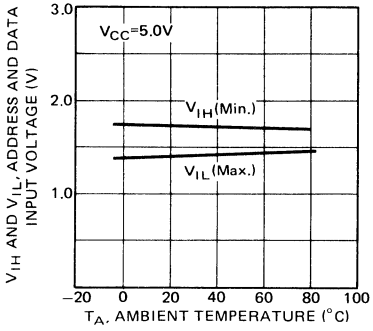

Fig. 18 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

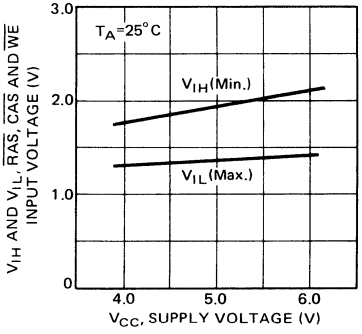

Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

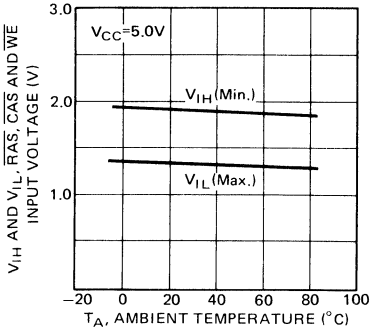

Fig. 20 – ACCESS TIME vs LOAD CAPACITANCE

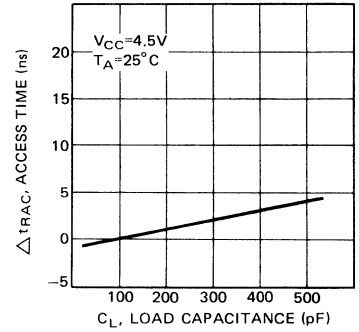

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Fig. 21 – OUTPUT CURRENT vs OUTPUT VOLTAGE

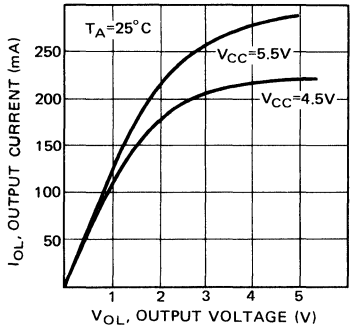


Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

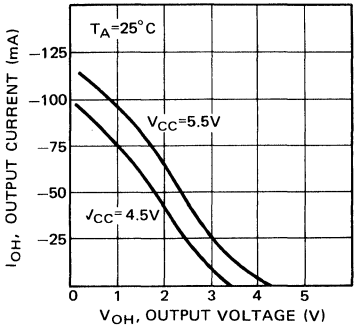


Fig. 23 – CURRENT WAVEFORM DURING POWER UP

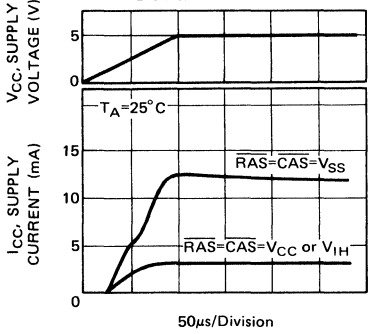
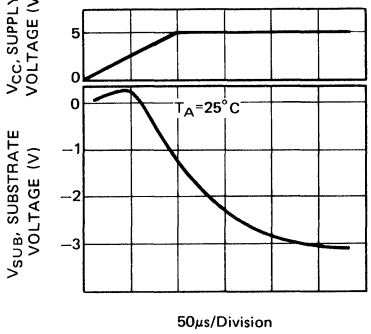
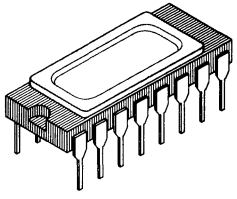


Fig. 24 – SUBSTRATE VOLTAGE DURING POWER UP



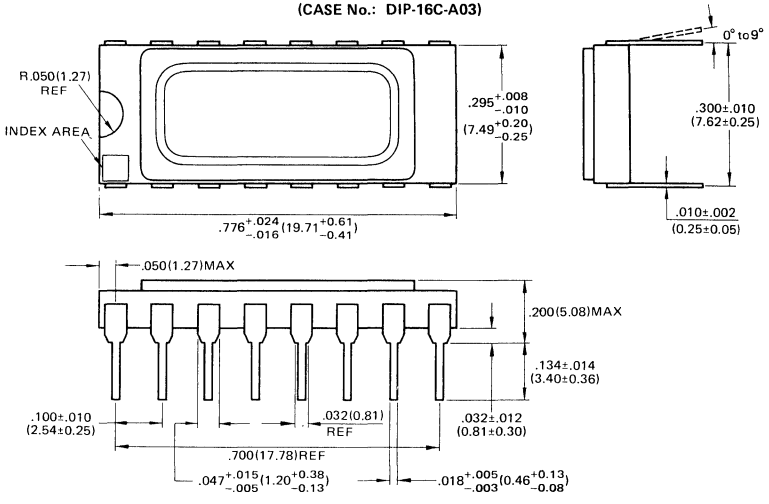
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A03

16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)

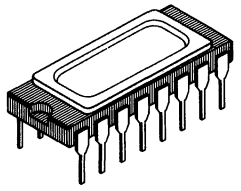


Dimensions in
inches (millimeters)

1

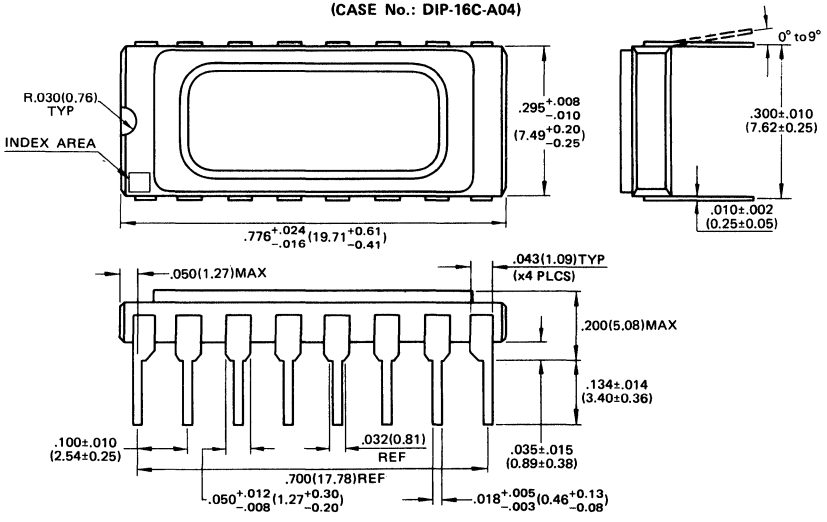
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A04

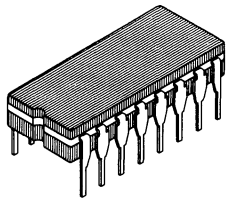
16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A04)



Dimensions in
inches (millimeters)

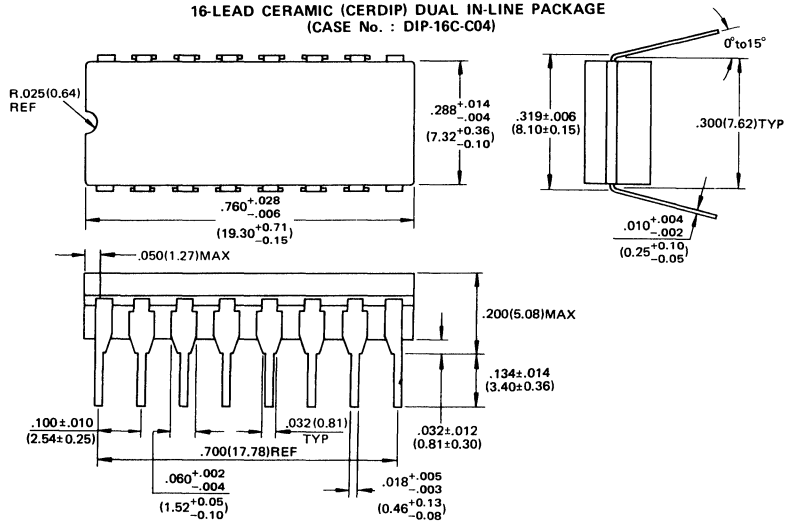
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -Z)



DIP-16C-C04

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C04)



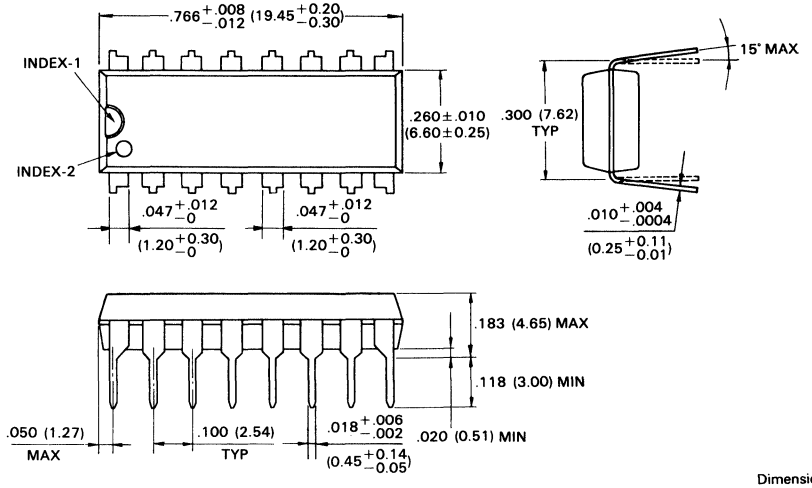
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Suffix: -P)

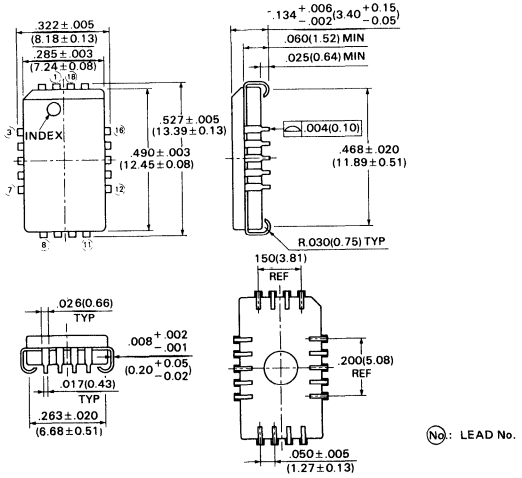
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Dimensions in inches (millimeters)

Standard 18-pin Plastic LCC (Suffix: -PD)

18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M04)



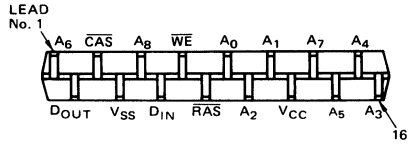
(No.): LEAD No.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

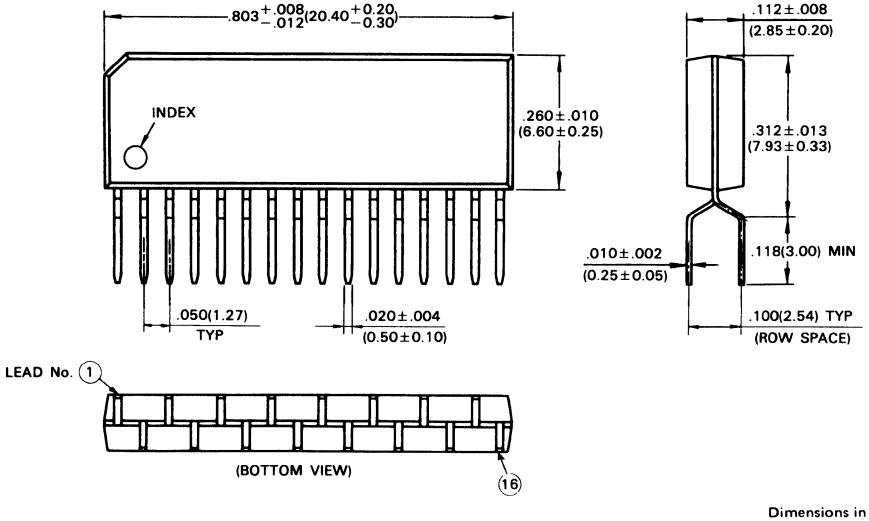
Standard 16-pin Plastic ZIP (Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

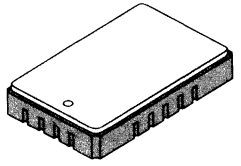
16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)



Dimensions in
inches (millimetres)

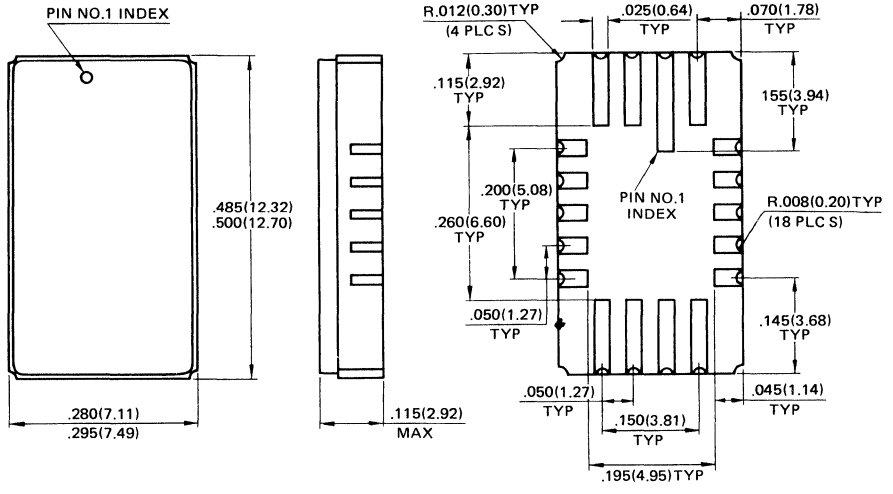
PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Suffix: -TV)



LCC-18C-F04

18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F04)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches (millimeters).

February 1990
Edition 2.0

FUJITSU

DATA SHEET

MB81256-80

MOS 262,144 BIT DYNAMIC RANDOM ACCESS MEMORY

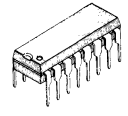
262,144 Bit Dynamic Random Access Memory

The Fujitsu MB81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and environments where low power dissipation and a compact layout are required.

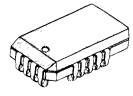
Multiplexed row and column address inputs permit the MB81256 to be housed in standard 16-pin DIP and ZIP packages or an 18-pin PLCC package. Pinouts conform to the JEDEC-approved pinouts. Additionally, the MB81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before-$\overline{RAS}$ refresh provides an on-chip refresh capability that is upwardly compatible with the MB8266A. The MB81256 also features page mode which allows high speed random access of up to 512 bits of data within the same row.

The MB81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible.

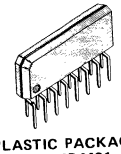
- 262,144 x 1 RAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time (t_{RAC}) 80 ns max. (MB 81256-80)
- Random Cycle Time (t_{RC}) 175 ns min. (MB 81256-80)
- Page Mode Cycle Time (t_{PC}) 100 ns max. (MB 81256-80)
- Single +5 V Supply, ±10% tolerance
- Low Power 385 mW max. (MB 81256-80) 25 mW max. (standby)
- 256 refresh cycles every 4 ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-white-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} are eliminated
- Output unlatched cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-Pin Plastic Packages: DIP (MB81256-XXP) ZIP (MB81256-XXPSZ)
  Standard 18-Pin Plastic Package: PLCC(MB81256-XXPV)
  Standard 16-Pin Ceramic Package: DIP (MB81256-XXC)



PLASTIC PACKAGE
DIP-16P-M03



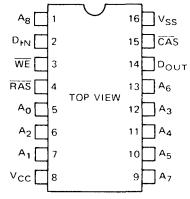
PLASTIC PACKAGE
LCC-18P-M04

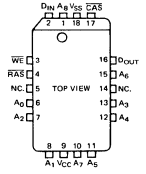


PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 17
DIP-16C-A04: See Page 18

PIN ASSIGNMENT





Pin assignment for ZIP: See Page 22

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

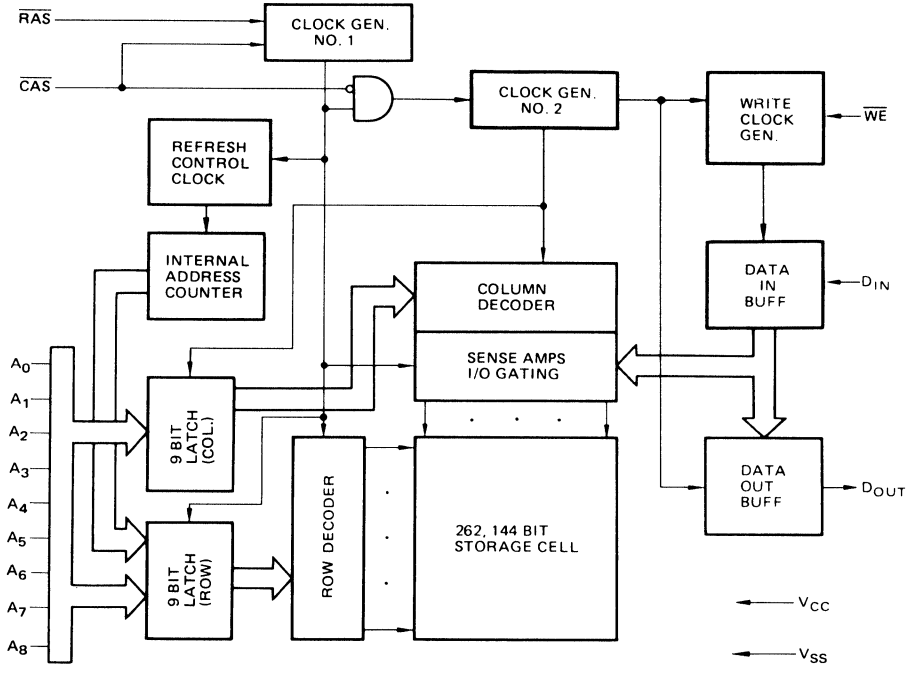
Absolute Maximum Ratings (See Note)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 – MB 81256 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		10	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81256-80	I_{CC1}			70	mA
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81256-80	I_{CC3}			60	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	MB81256-80	I_{CC4}			35	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81256-80	I_{CC5}			65	mA
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = -5.0mA)		V_{OH}	2.4			V

NOTE* : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
Time between Refresh		t_{REF}		4	ms
Random Read/Write Cycle Time		t_{RC}	175		ns
Read-Write Cycle Time		t_{RWC}	180		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		80	ns
Access Time from $\overline{CAS}$	4 6	t_{CAC}		45	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	ns
Transition Time		t_T	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	85	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	50	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	85		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	35	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		ns
Row Address Set Up Time		t_{ASR}	0		ns
Row Address Hold Time		t_{RAH}	10		ns
Column Address Set Up Time		t_{ASC}	0		ns
Column Address Hold Time		t_{CAH}	15		ns
Read Command Set Up Time		t_{RCS}	0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		ns
Write Command Set Up Time	10	t_{WCS}	0		ns
Write Command Pulse Width		t_{WP}	15		ns
Write Command Hold Time		t_{WCH}	15		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		ns
Data In Set Up Time		t_{DS}	0		ns
Data In Hold Time		t_{OH}	15		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

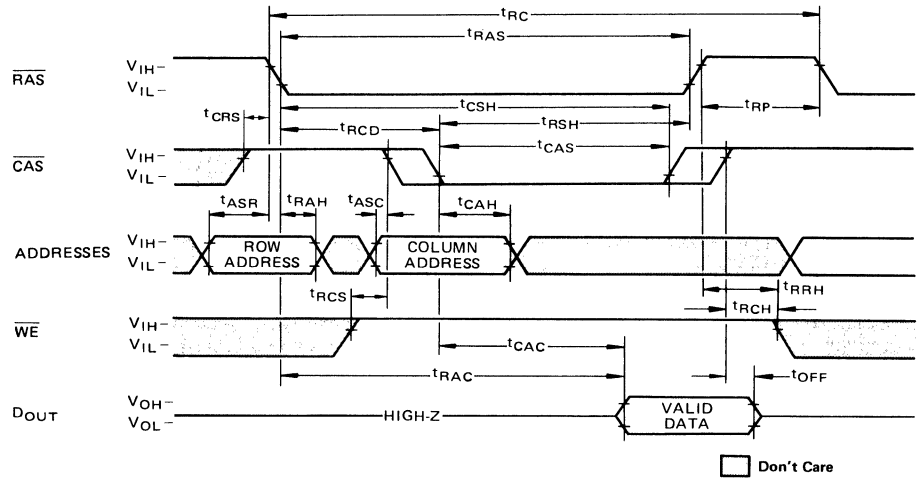
Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		ns
Page Mode Read/Write Cycle Time		t_{PC}	100		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	100		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	40		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		ms
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		ns

Notes:

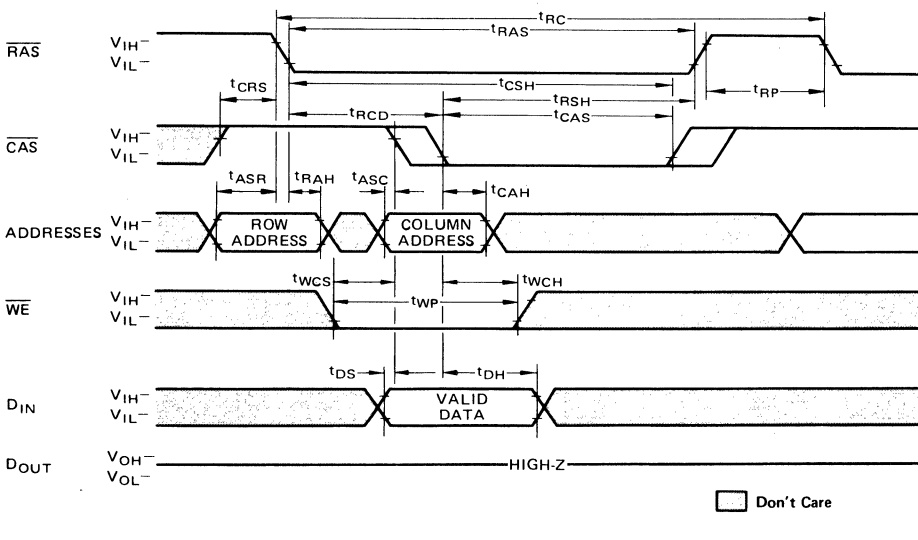
1. An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.) If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5ns) + t_{ASC} (min).
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
    If $t_{CWD} \geqq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

1

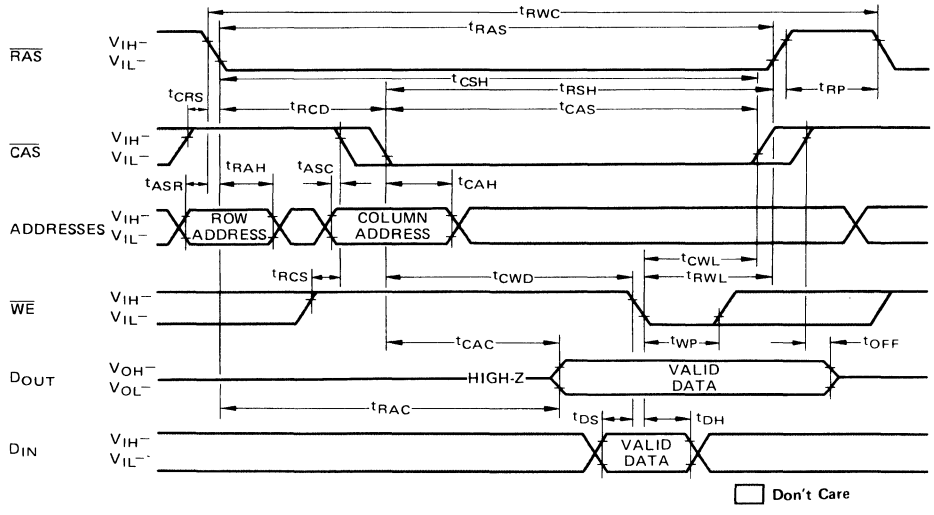
Read Cycle



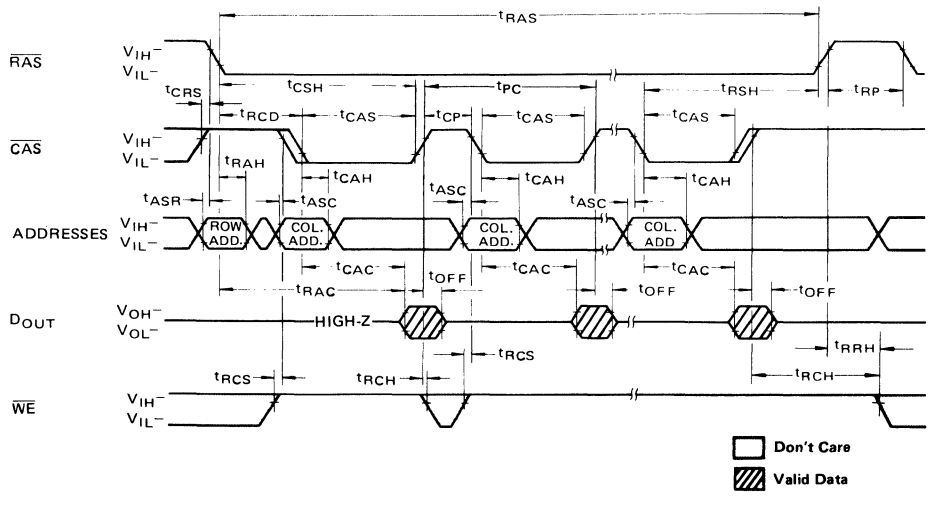
Write Cycle (Early Write)



Read–Write/Read–Modify–Write Cycle



Page Mode Read Cycle



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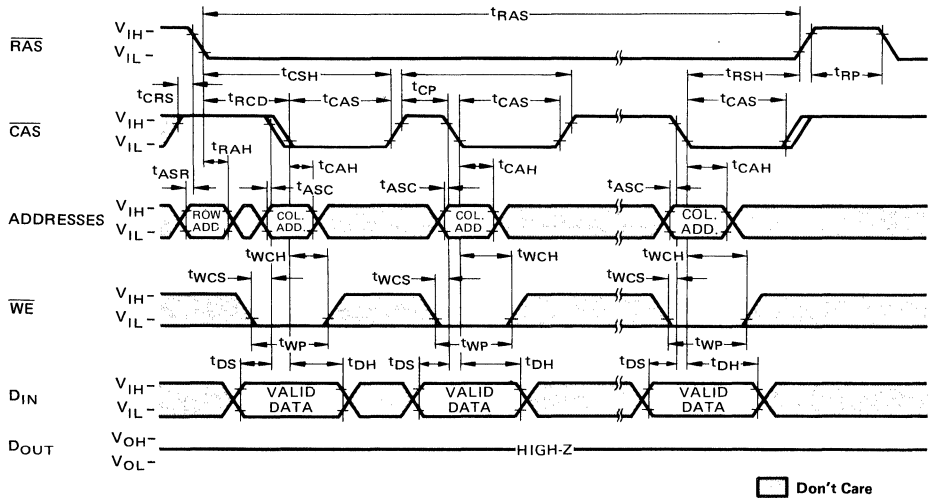
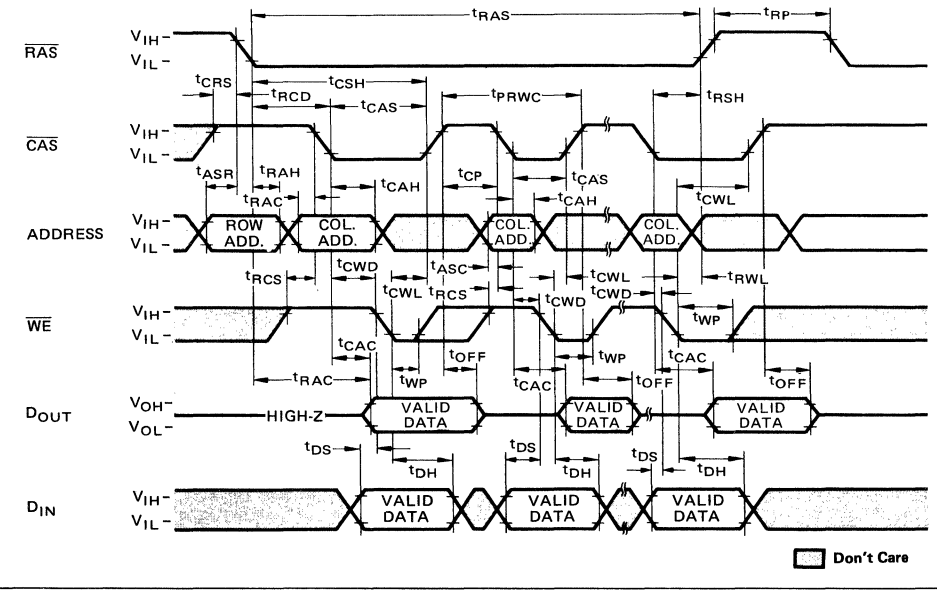
Page Mode Write Cycle (Early Write)

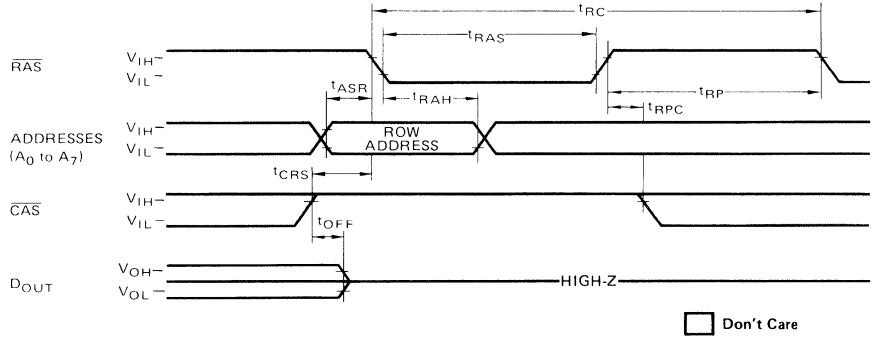


Page Mode Read-Write Cycle



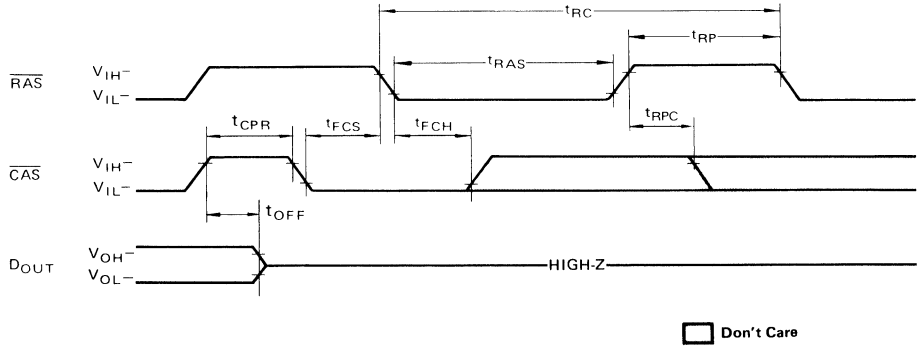
$\overline{RAS}$-only Refresh cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, $A_8 = V_{IH}$ or V_{IL}



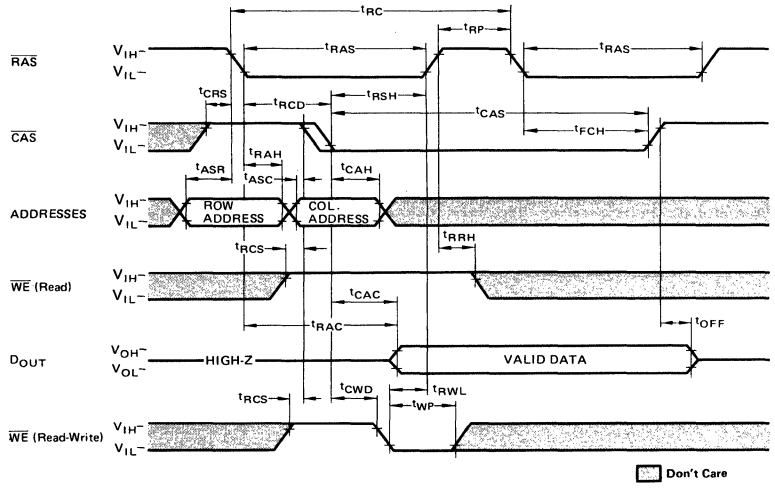
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Address, $\overline{WE}$, D_{IN} = Don't care

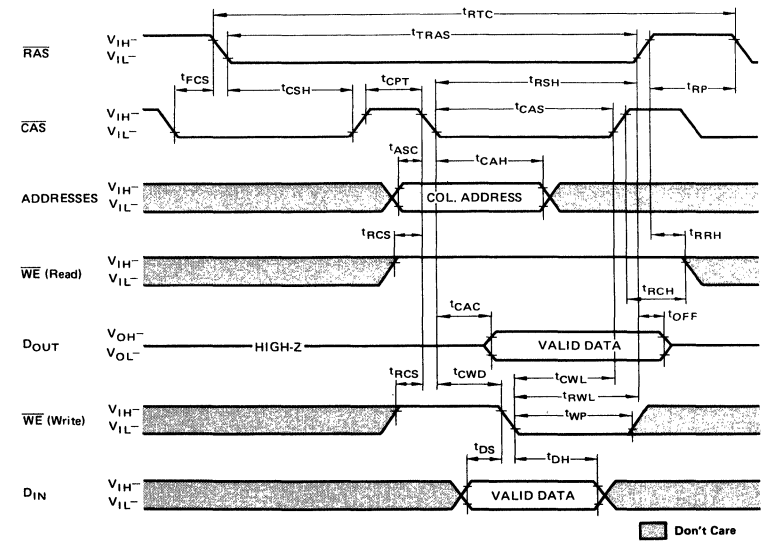


1

Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement

The MB 81256 has improved circuitry that eases timing requirements for high speed access operations. The MB 81256 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81256 has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ nonrestrictive and deleted them from the data sheet, these include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81256. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode; low selects write mode. The data input is disable when read mode is selected.

Data input:

Data is written into the MB 81256 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle

The MB 81256 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle is possible with the MB 81256.

Page Mode:

Page-mode operation permits strobing the row-address into the MB 81256 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4ms. The MB 81256 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;

$\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low.

Strobing each of 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81256 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh;

A hidden refresh cycle may takes place while maintaining the latest valid data at the output by extending $\overline{CAS}$ active time.

For the MB 81256 a hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counters provide the refresh addresses, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$-

before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-befor-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and then goes to low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and column address (9 bits) to be accessed can be defined as follows:

*A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.

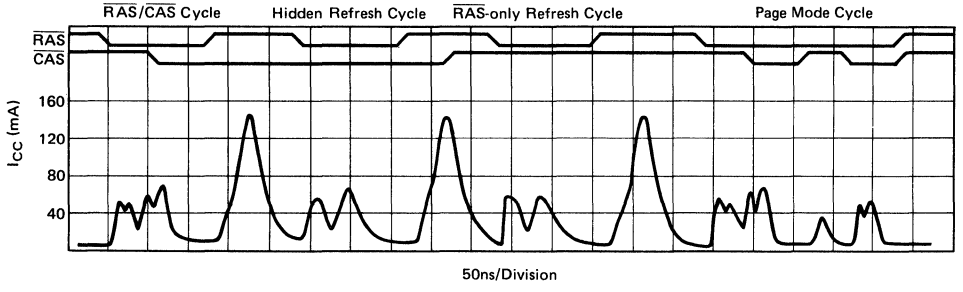
*A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test cycles is used for the following operations:

(1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
(2) Throughout the test, use the same column address, and keep RA8 high.
(3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
(4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
(5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
(6) Complement the test pattern and repeat step 3), 4) and 5).

Fig. 2 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

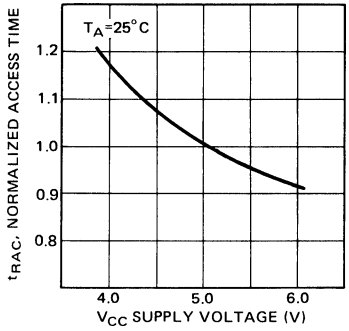


Fig. 4 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

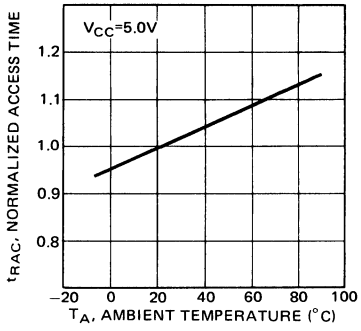


Fig. 5 – OPERATING CURRENT vs CYCLE RATE

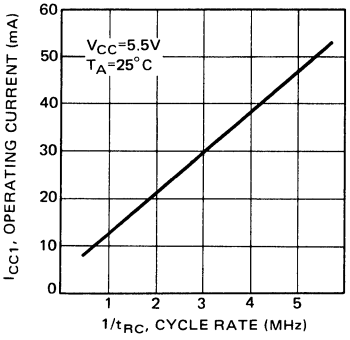


Fig. 6 – OPERATING CURRENT vs SUPPLY VOLTAGE

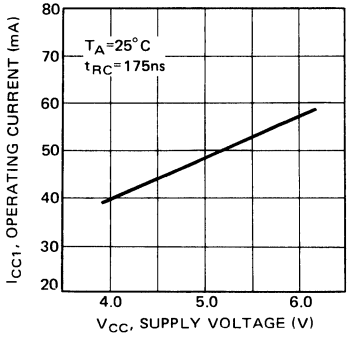


Fig. 7 – OPERATING CURRENT vs AMBIENT TEMPERATURE

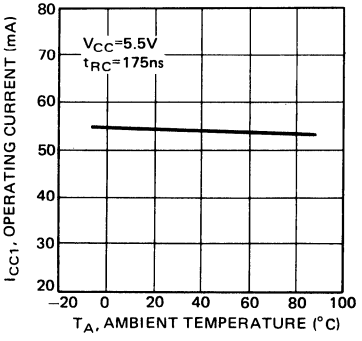
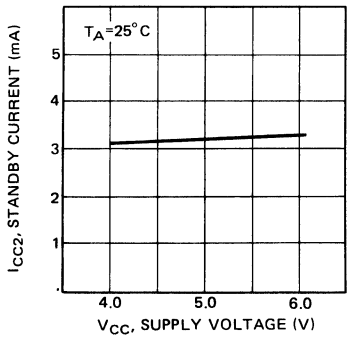


Fig. 8 – STANDBY CURRENT vs SUPPLY VOLTAGE



1

Fig. 9 – STANDBY CURRENT vs AMBIENT TEMPERATURE

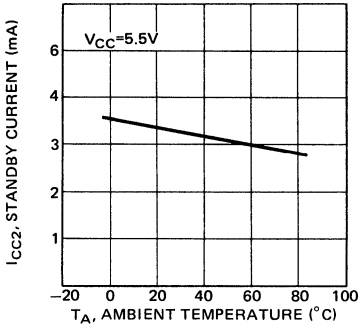


Fig. 10 – REFRESH CURRENT 1 vs CYCLE RATE

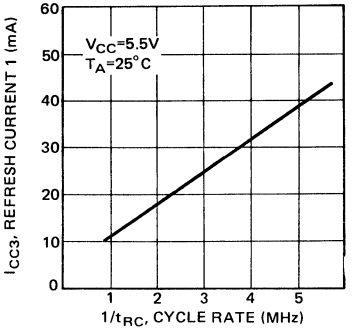


Fig. 11 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

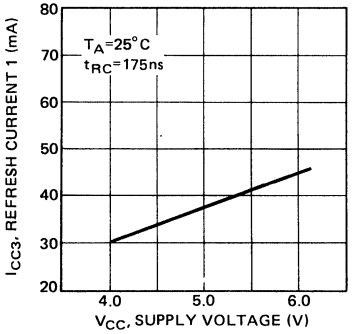


Fig. 12 – PAGE MODE CURRENT vs CYCLE RATE

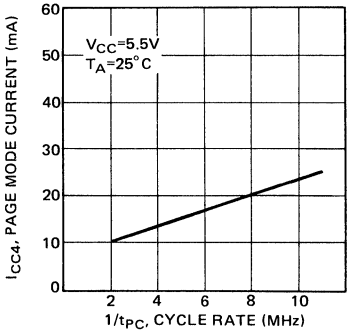


Fig. 13 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

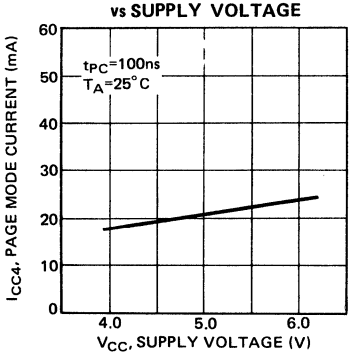


Fig. 14 – REFRESH CURRENT 2 vs CYCLE RATE

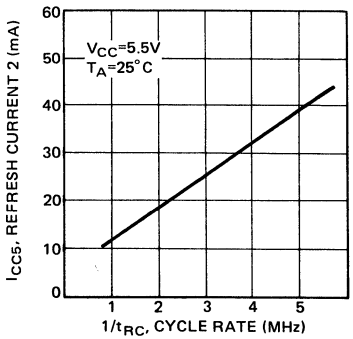


Fig. 15 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

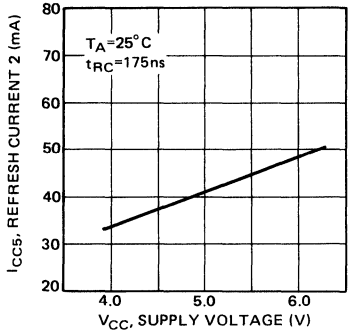


Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

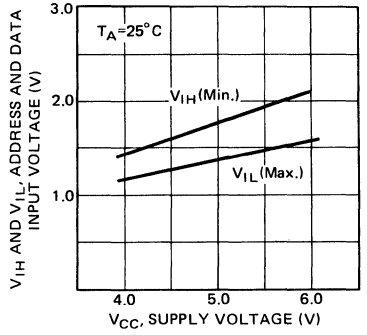


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

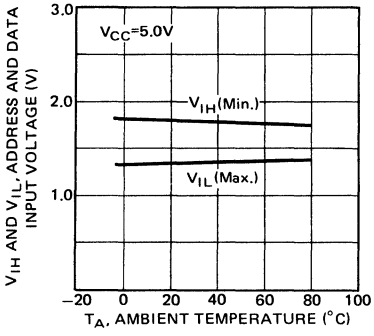


Fig. 18 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

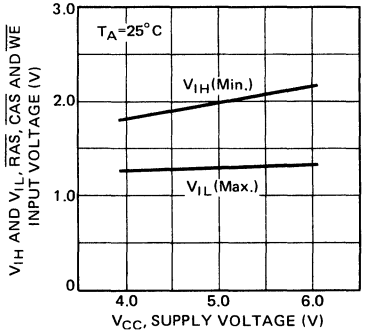


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

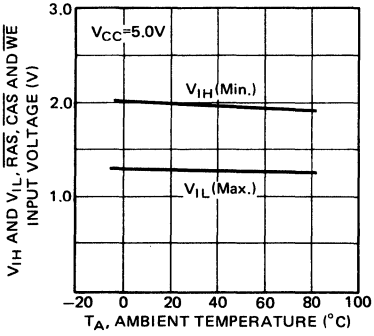
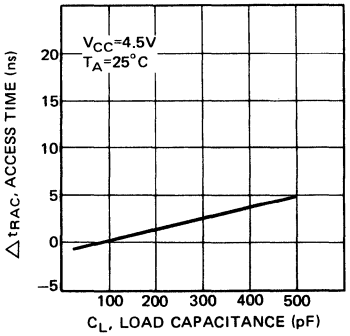


Fig. 20 – ACCESS TIME vs LOAD CAPACITANCE



1

1

Fig. 21 – OUTPUT CURRENT vs OUTPUT VOLTAGE

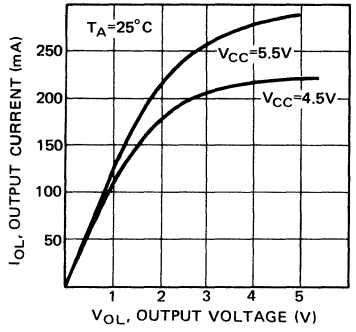


Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

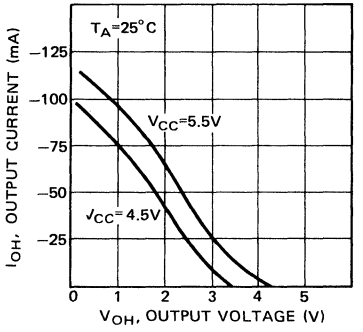


Fig. 23 – CURRENT WAVEFORM DURING POWER UP

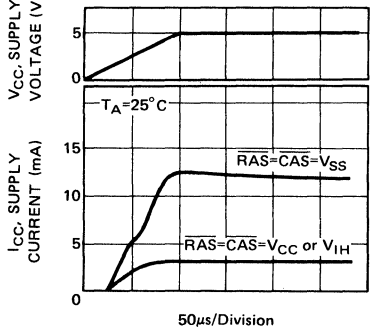
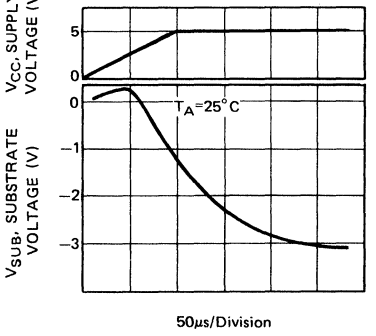
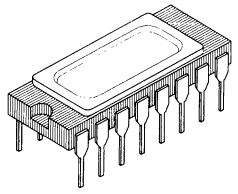


Fig. 24 – SUBSTRATE VOLTAGE DURING POWER UP



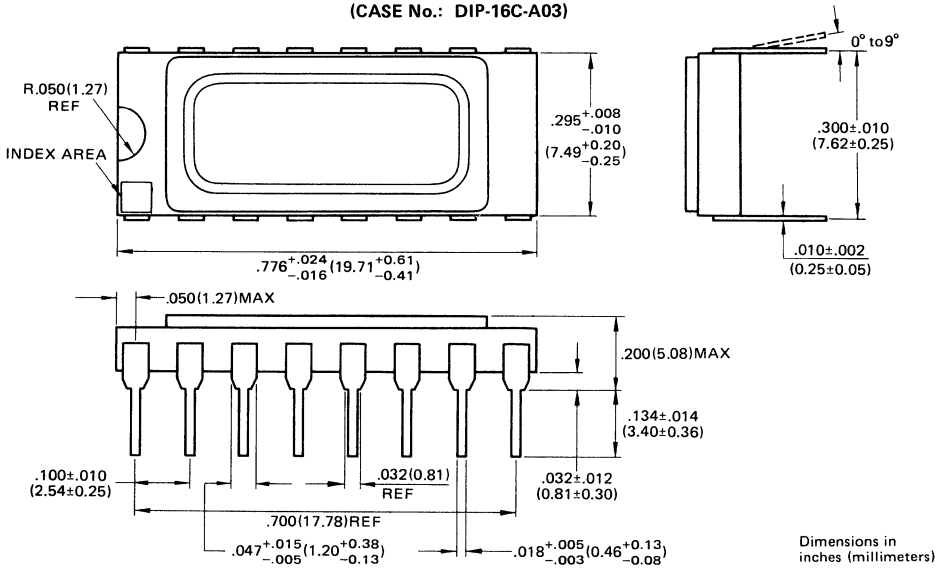
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-16C-A03

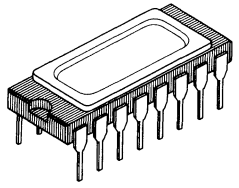
16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)



Dimensions in inches (millimeters)

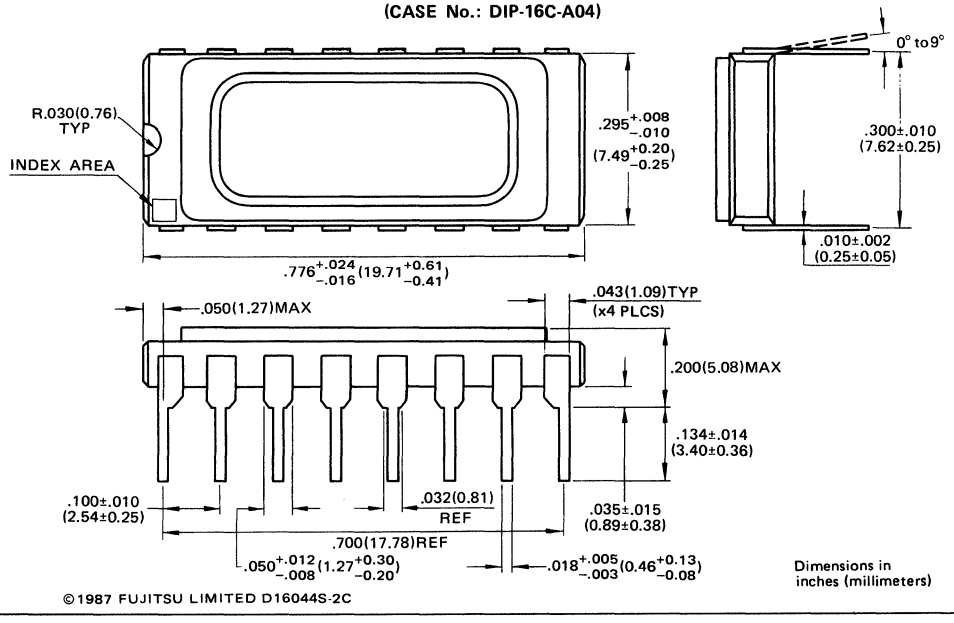
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-16C-A04

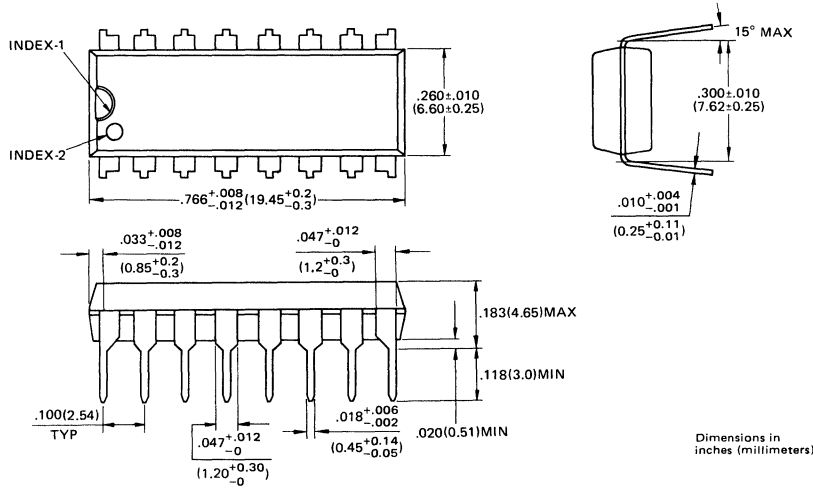
16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A04)



PACKAGE DIMENSIONS

(Suffix: -P)

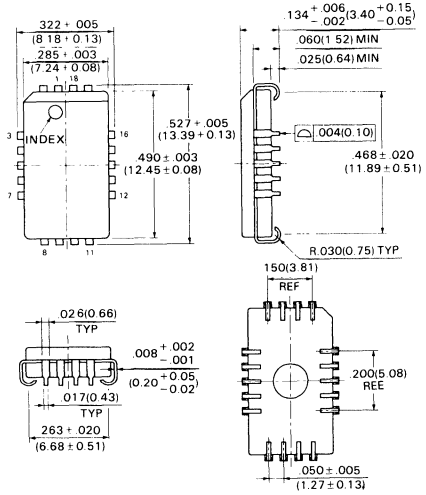
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Dimensions in inches (millimeters)

(Suffix: -PD)

18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M04)



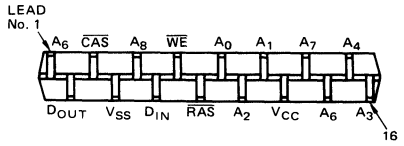
(No.): LEAD No.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

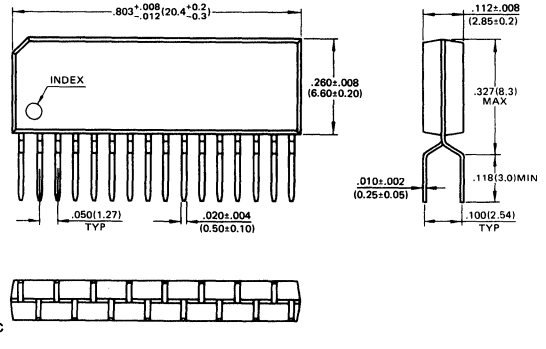
(Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

16-LEAD PLASTIC ZIGZAG-IN-LINE PACJAGE
(CASE No.: ZIP-16P-M01)



Dimensions in inches (millimeters)

February 1990
Edition 5.0

FUJITSU

DATA SHEET

MB81257-10/-12/-15

MOS 262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

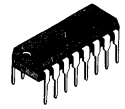
262,144-Bit Dynamic Random Access Memory

The Fujitsu MB81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and environments where low power dissipation and a compact layout are required.

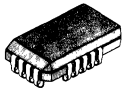
Multiplexed row and column address inputs permit the MB81257 to be housed in standard 16-pin DIP and ZIP packages or an 18-pin PLCC package. Pinouts conform to the JEDEC-approved pinouts. Additionally, the MB81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before-$\overline{RAS}$ refresh provides an on-chip refresh capability that is upwardly compatible with the MB8266A. The MB81257 also features nibble mode which allows high speed serial access of up to 4 bits of data.

The MB81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible.

- 262,144 x 1 RAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time
  100 ns max. (MB 81257-10)
  120 ns max. (MB 81257-12)
  120 ns max. (MB 81257-15)
- Cycle Time
  200 ns min. (MB 81257-10)
  220 ns min. (MB 81257-12)
  260 ns min. (MB 81257-15)
- Nibble Cycle Time
  45 ns max. (MB 81257-10)
  50 ns max. (MB 81257-12)
  60 ns max. (MB 81257-15)
- Single +5 V Supply, ±10% tolerance
- Low Power
  385 mW max. (MB 81257-10)
  358 mW max. (MB 81257-12)
  314 mW max. (MB 81257-15)
  25 mW max. (standby)
- 256 refresh cycles every 4 ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-white-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} are eliminated
- Output unlatched cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-Pin Plastic Packages:
  DIP (MB81257-XXP)
  ZIP (MB81257-XXPSZ)
  Standard 18-Pin Plastic Package:
  PLCC(MB81257-XXPV)
  Standard 16-Pin Ceramic Packages:
  DIP (MB81257-XXC) Seam Weld
  DIP (MB81257-XXZ) Cerdip
  Standard 18-Pad Ceramic Package:
  LCC (MB81257-XXTV)



PLASTIC PACKAGE
DIP-16P-M03

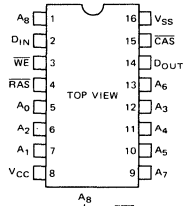


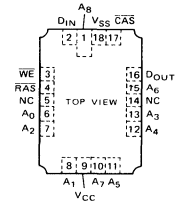
PLASTIC PACKAGE
LCC-18P-M04

PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 19
DIP-16C-A04: See Page 20
DIP-16C-C04: See Page 21
LCC-18C-F04: See Page 24

PIN ASSIGNMENT





Pin assignment for ZIP: See page 23

Absolute Maximum Ratings

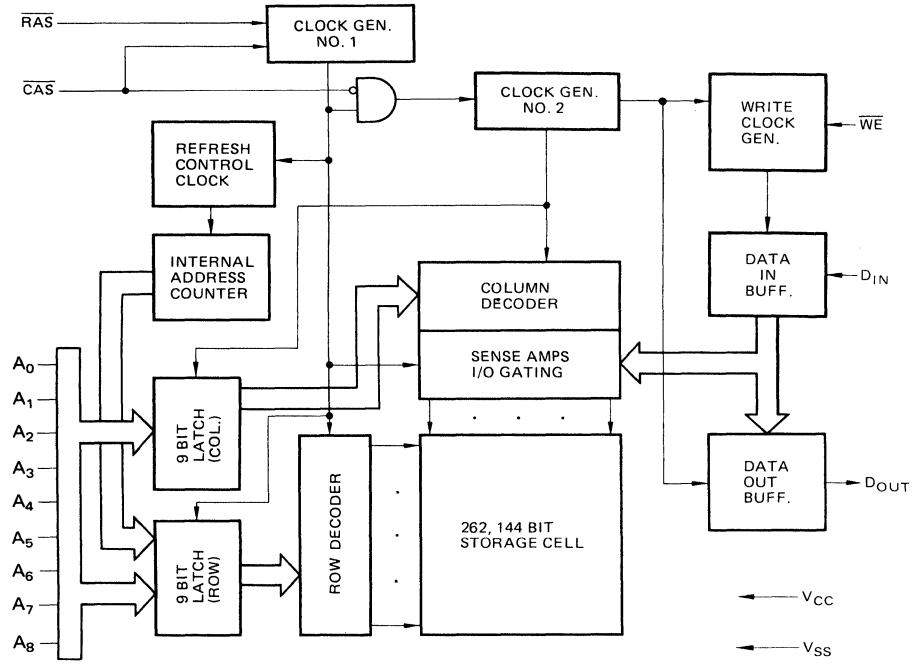
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MB 81257 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81257-10	I_{CC1}			70	mA
	MB 81257-12				65	
	MB 81257-15				57	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81257-10	I_{CC3}			60	mA
	MB 81257-12				55	
	MB 81257-15				50	
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = Min.)	MB 81257-10	I_{CC4}			22	mA
	MB 81257-12				20	
	MB 81257-15				18	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81257-10	I_{CC5}			65	mA
	MB 81257-12				60	
	MB 81257-15				55	
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output high Voltage (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE * : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

1

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter NOTES	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
		Min	Max	Min	Max	Min	Max	
Time between Refresh	t_{REF}		4		4		4	ms
Random Read/Write Cycle time	t_{RC}	200		220		260		ns
Read-Write Cycle Time	t_{RWC}	200		220		260		ns
Access Time from $\overline{RAS}$ 4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$ 5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay	t_{OFF}	0	25	0	25	0	30	ns
Transition Time	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse width	t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time 7 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	10		10		10		ns
Row Address Set Up Time	t_{ASR}	0		0		0		ns
Row Address Hold Time	t_{RAH}	10		12		15		ns
Column Address Set Up Time	t_{ASC}	0		0		0		ns
Column Address Hold Time	t_{CAH}	15		20		25		ns
Read Command Set Up Time	t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$ 9	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ 9	t_{RRH}	20		20		20		ns
Write Command Set Up Time 10	t_{WCS}	0		0		0		ns
Write Command Pulse Width	t_{WP}	15		20		25		ns
Write Command Hold Time	t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20		30		25		ns
Data In Set Up Time	t_{DS}	0		0		0		ns
Data In Hold Time	t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{WE}$ Delay 10	t_{CWD}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

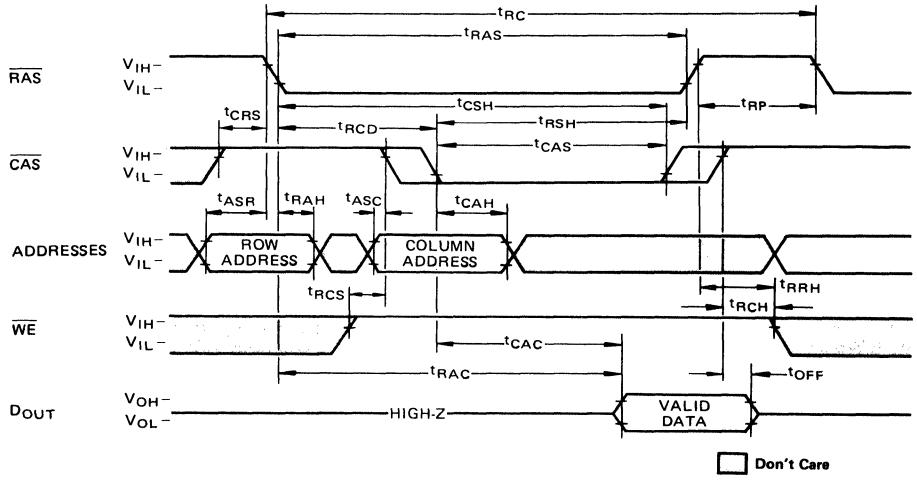
Parameter	NOTES	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	45		50		60		ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	45		50		60		ns
Nibble Mode Access Time		t_{NCAC}		20		25		30	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	20		25		30		ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15		15		20		ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	20		25		30		ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	35		40		45		
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	20		20		20		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		375		430		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		60		70		ns

Notes:

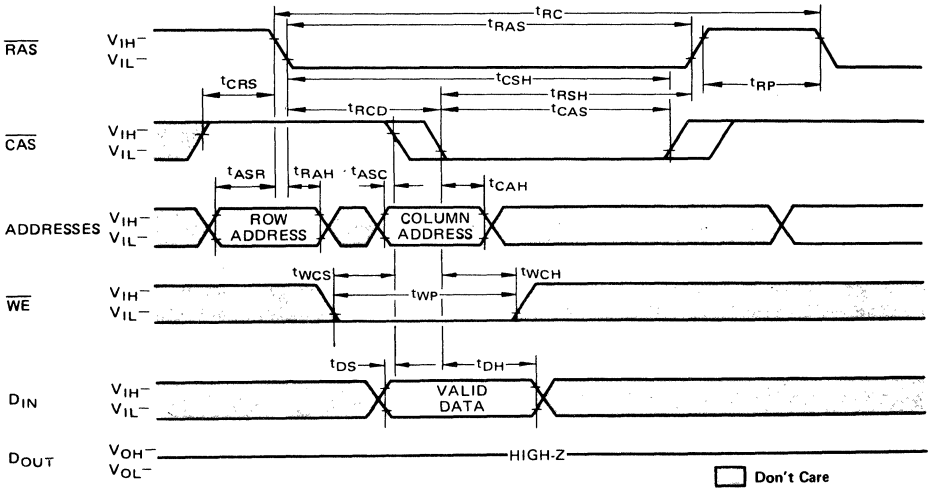
1. An initial pause of 200 μs is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

1

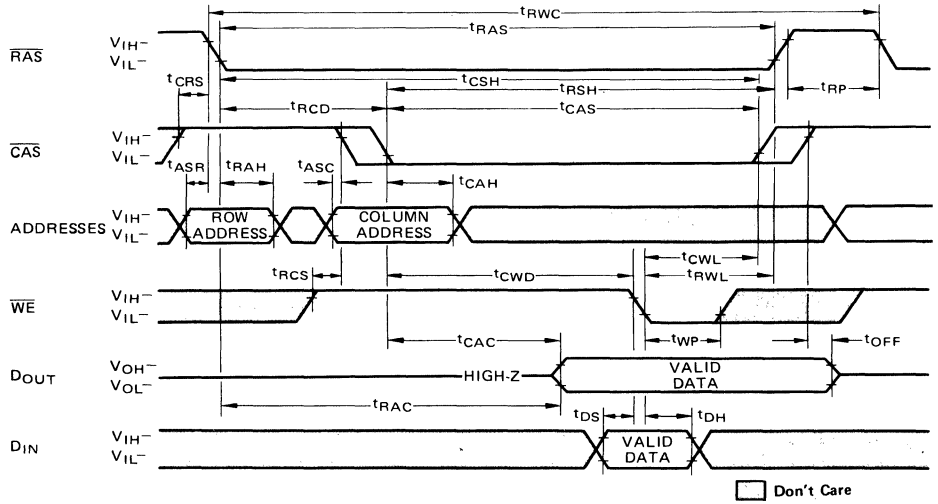
Read Cycle



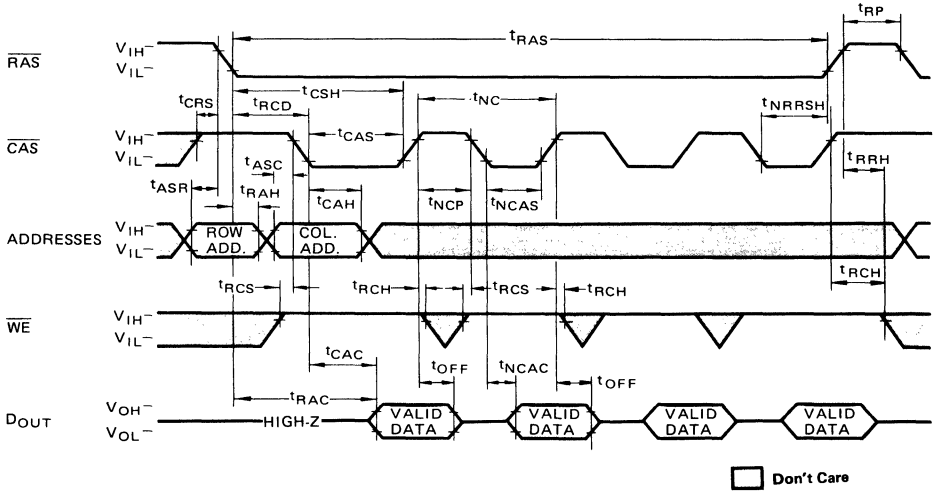
Write Cycle (Early Write)



Read–Write/Read–Modify–Write Cycle



Nibble Mode Read Cycle



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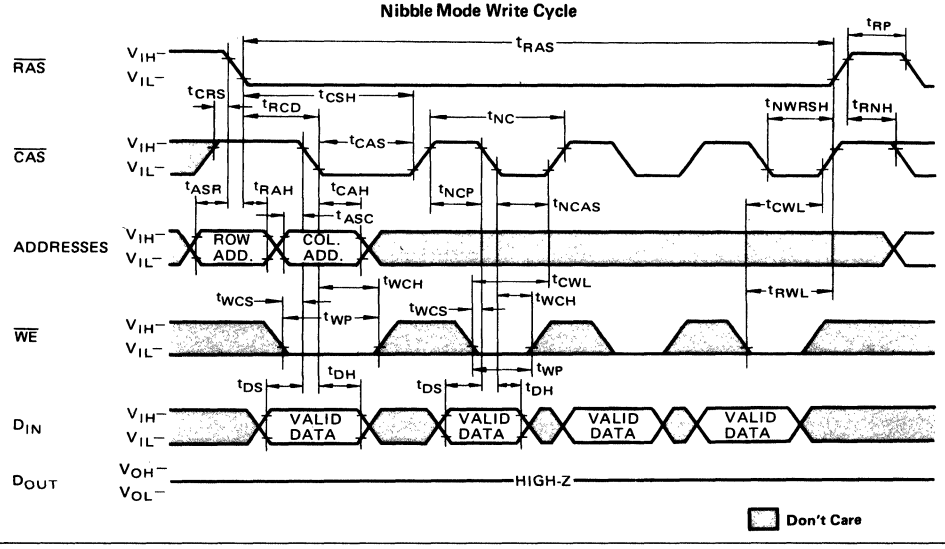
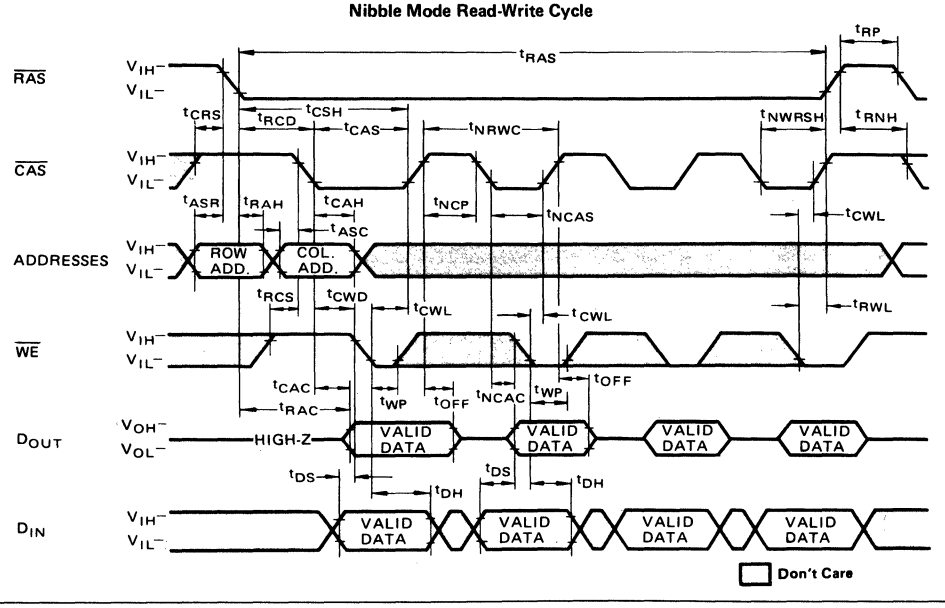
Nibble Mode Write Cycle

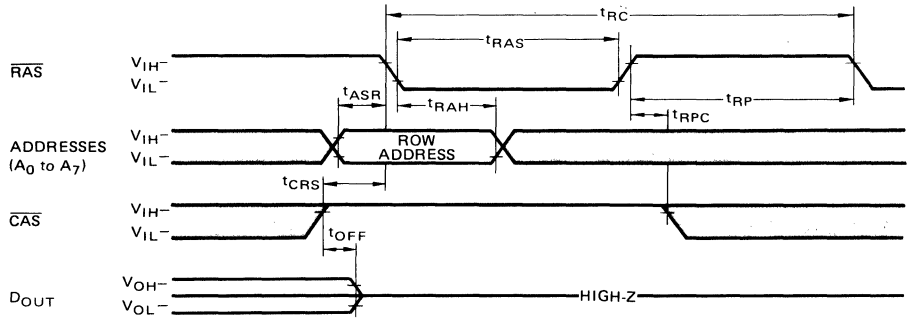


Nibble Mode Read-Write Cycle



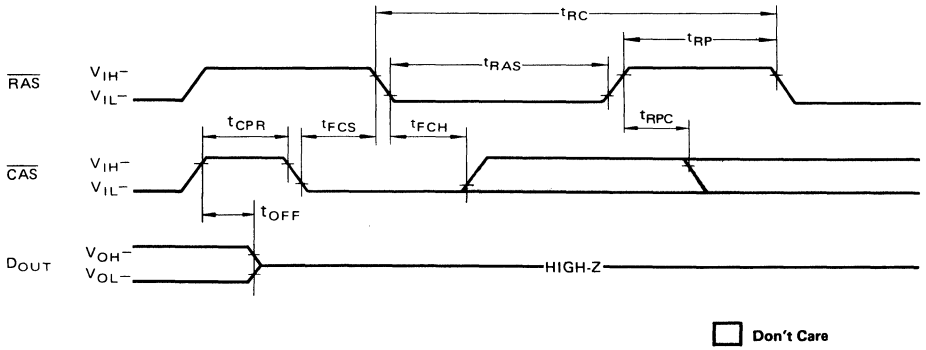
$\overline{RAS}$-only Refresh Cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, A_8 = V_{IH} or V_{IL}



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Address, $\overline{WE}$, D_{IN} = Don't care



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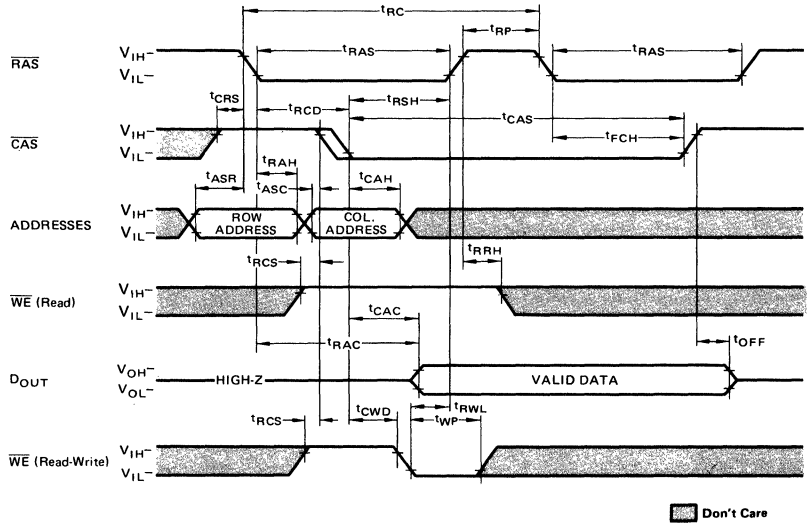
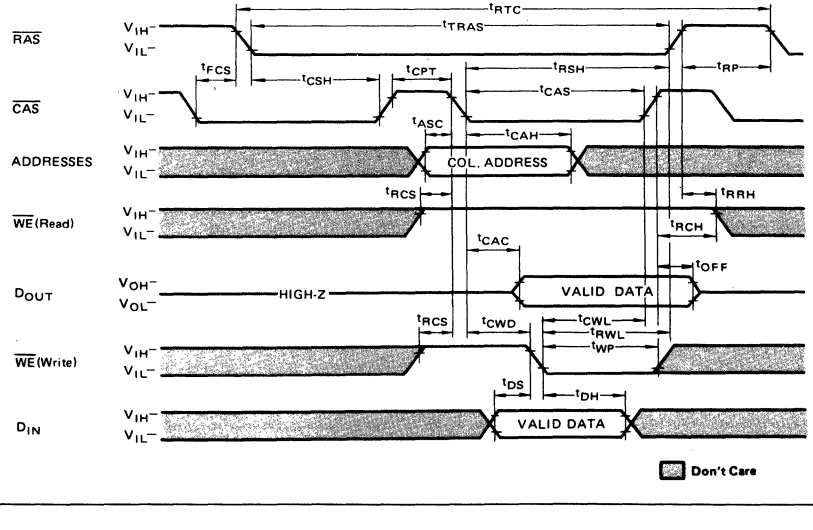
Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement
The MB 81257 has improved circuitry that eases timing requirements for high speed access operations. The MB 81257 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81257 has the minimal hold times of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81257 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81257. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode, low selects write mode. The data input is disabled when read mode is selected.

Data Input:
Data is written into the MB 81257 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.) Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle
The MB 81257 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings, described in the previous section. The output buffer is controlled by the sate of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle (t_{RWC} = t_{RC}) is possible with the MB 81257.

Nibble Mode:
Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).
If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.
In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.
The data output is controlled only by the $\overline{WE}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain high impedance state throughout the succeeding nibble cycle regardless of the $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{WE}$ state. The write operation is done during the period in which the $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit).
See Fig. 2.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 ms.
The MB 81257 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;
The $\overline{RAS}$ only refresh aboids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each

of 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81257 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh;
A hidden refresh cycle may takes place while maintaining latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB 81257, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh.

The internal refresh address counters provide the refresh addresses, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

CAS-before-RAS Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

* A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.
* A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for the following operations:

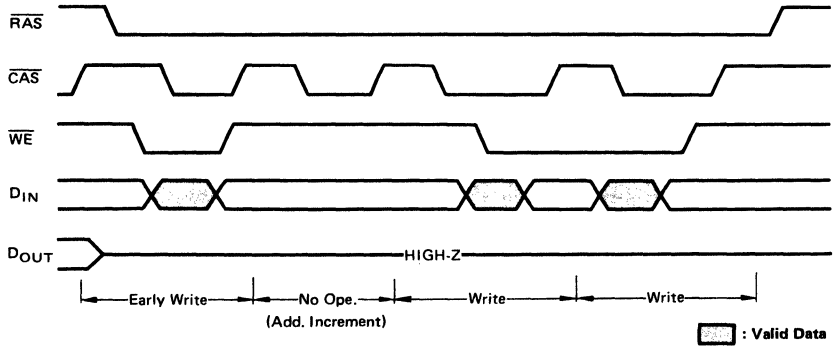
1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address, and keep RA8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

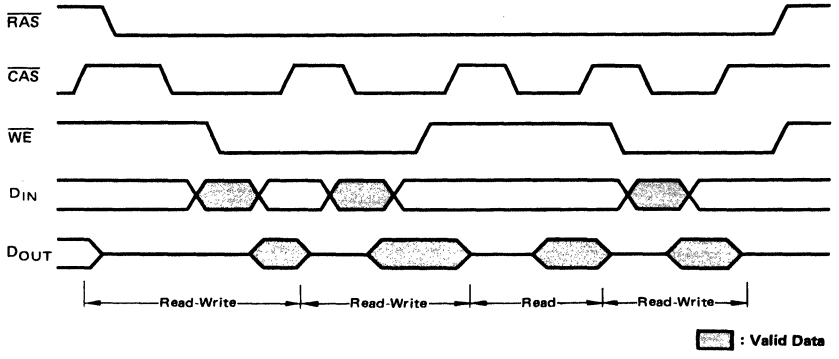
SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Fig. 2 – Nibble Mode

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)

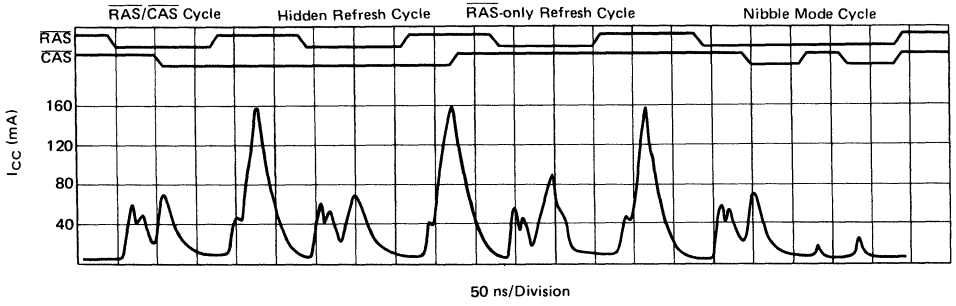


1

Table-2 FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geqq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write ($t_{WCS} \leqq t_{WCS}$ (min) or $t_{CWD} \geqq t_{CWD}$ (min))
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Fig. 3 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

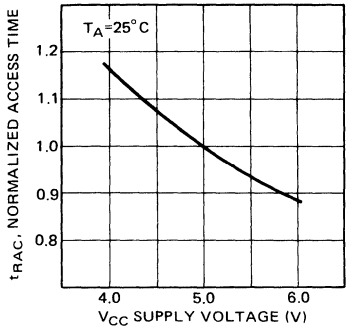


Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

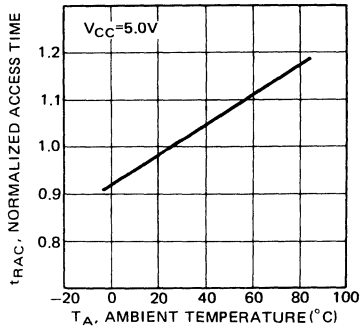


Fig. 6 – OPERATING CURRENT vs CYCLE RATE

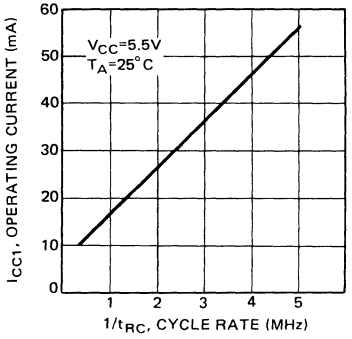


Fig. 7 – OPERATING CURRENT vs SUPPLY VOLTAGE

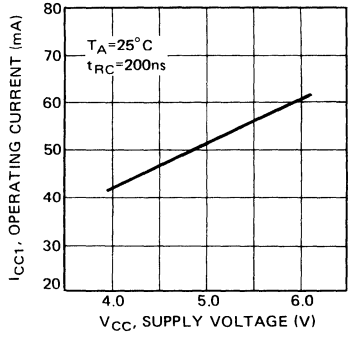


Fig. 8 – OPERATING CURRENT vs AMBIENT TEMPERATURE

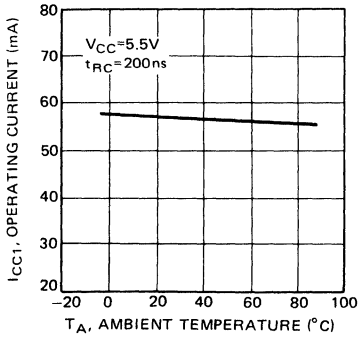
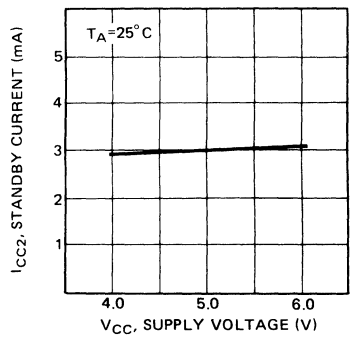


Fig. 9 – STANDBY CURRENT vs SUPPLY VOLTAGE



1

Fig. 10 – STANDBY CURRENT vs AMBIENT TEMPERATURE

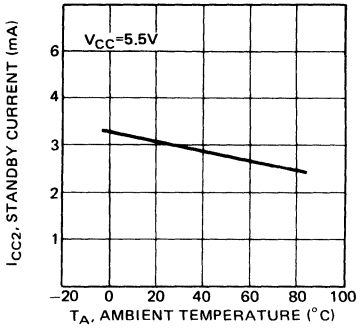


Fig. 11 – REFRESH CURRENT 1 vs CYCLE RATE

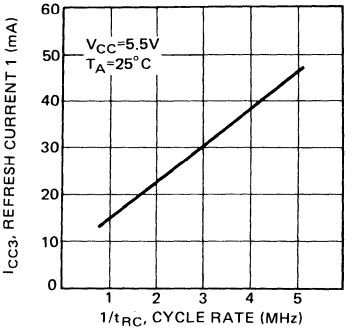


Fig. 12 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

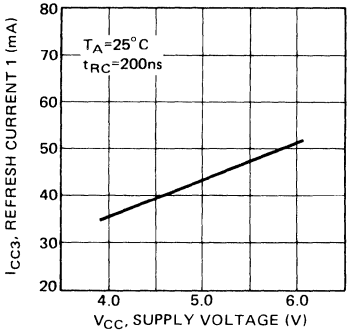


Fig. 13 – NIBBLE MODE CURRENT vs CYCLE RATE

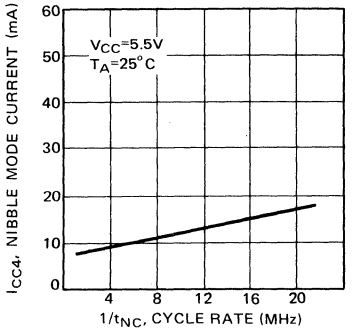


Fig. 14 – NIBBLE MODE CURRENT vs SUPPLY VOLTAGE

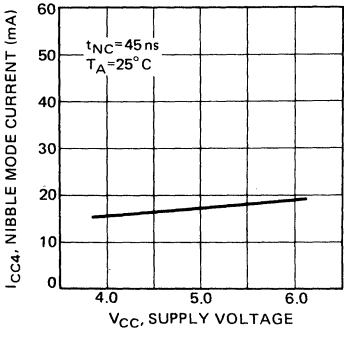


Fig. 15 – REFRESH CURRENT 2 vs CYCLE RATE

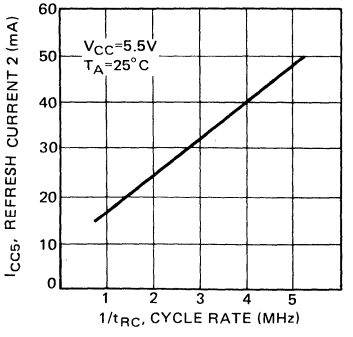


Fig. 16 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

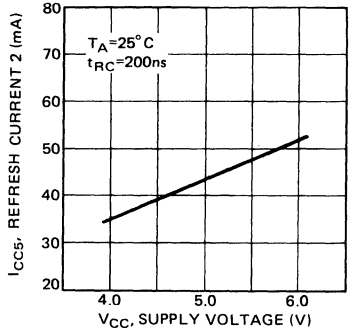


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

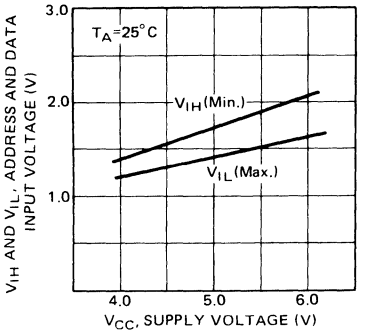


Fig. 18 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

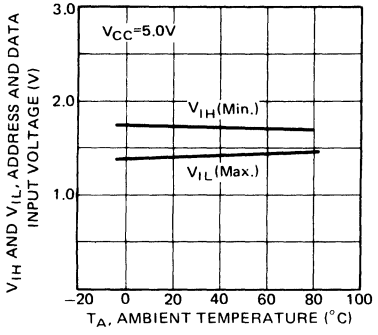


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

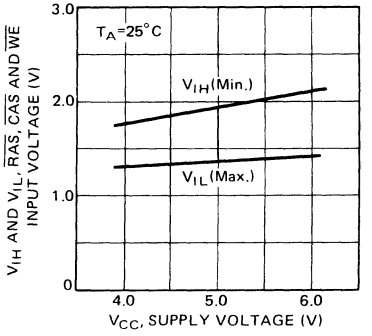


Fig. 20 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

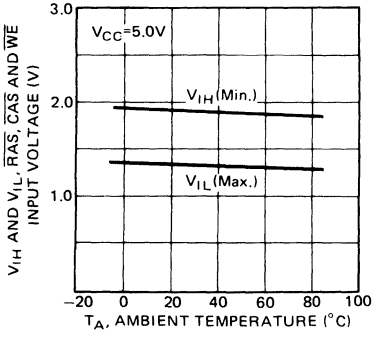
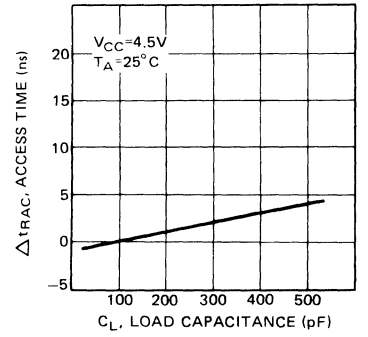


Fig. 21 – ACCESS TIME vs LOAD CAPACITANCE



1

Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

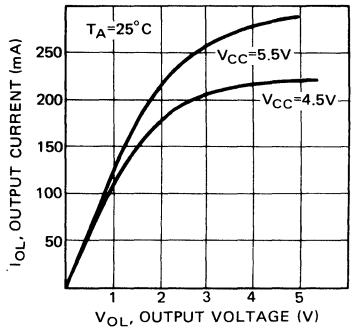


Fig. 23 – OUTPUT CURRENT vs OUTPUT VOLTAGE

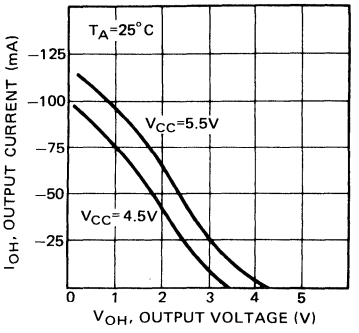


Fig. 24 – CURRENT WAVEFORM DURING POWER UP

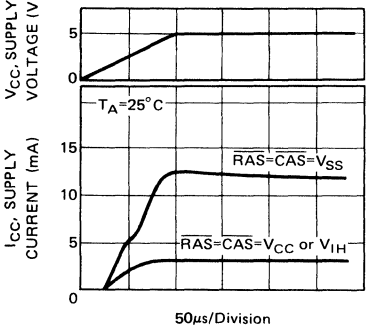
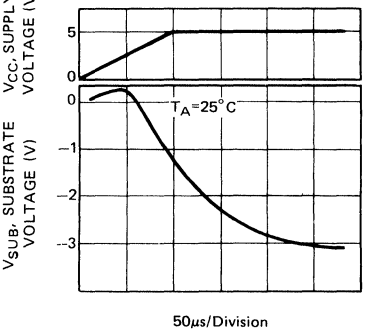
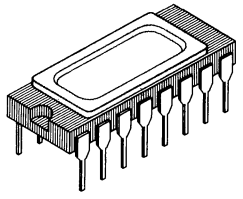


Fig. 25 – SUBSTRATE VOLTAGE DURING POWER UP



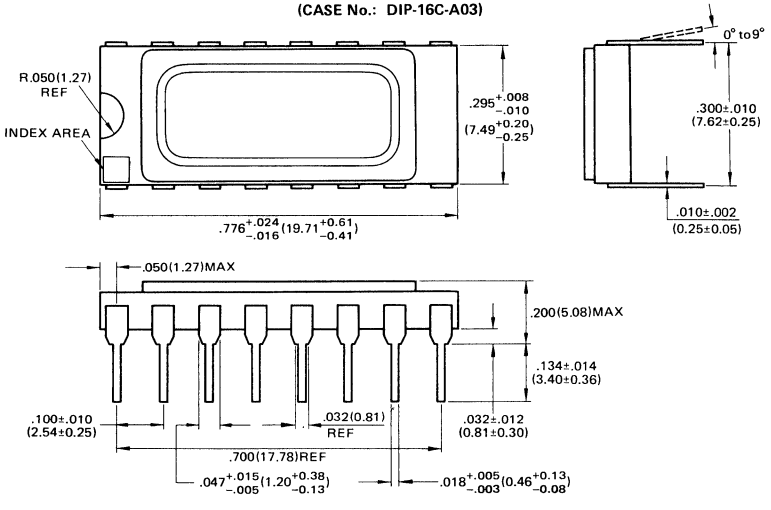
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A03

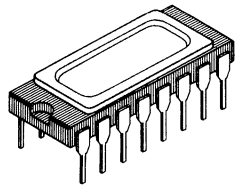
16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)



Dimensions in
inches (millimeters)

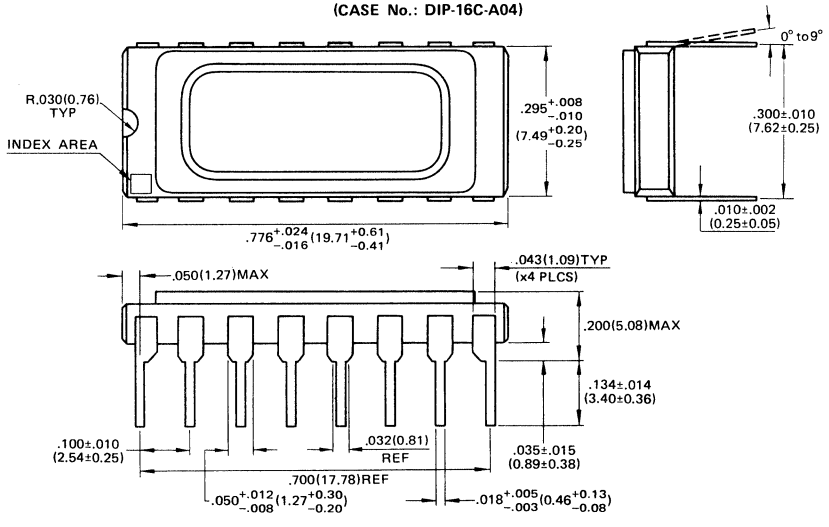
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A04

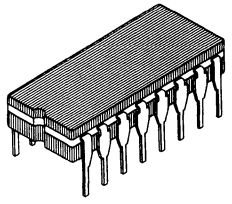
16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A04)



Dimensions in
inches (millimeters)

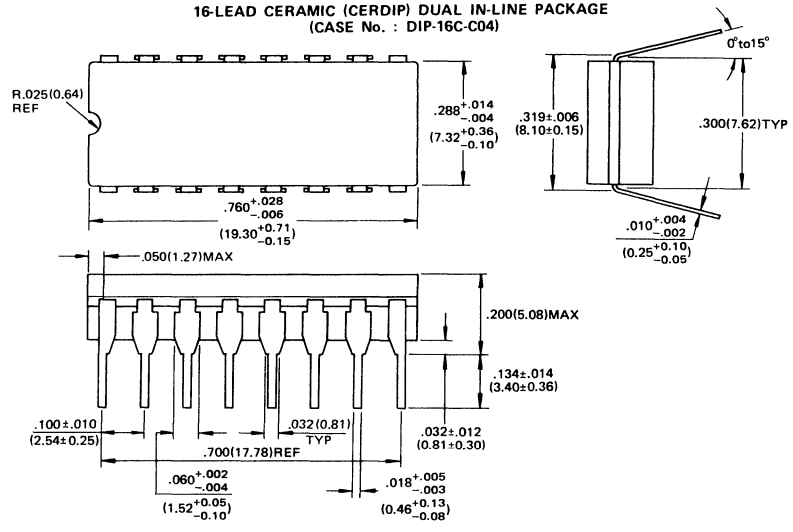
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -Z)



DIP-16C-C04

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C04)



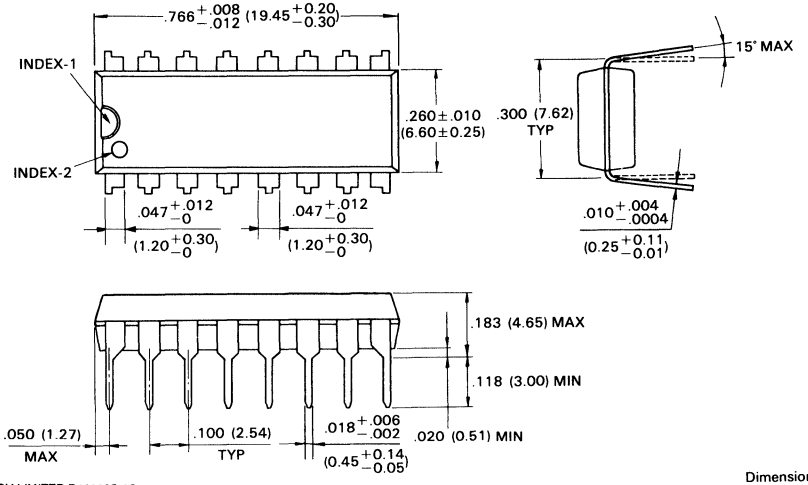
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Suffix: -P)

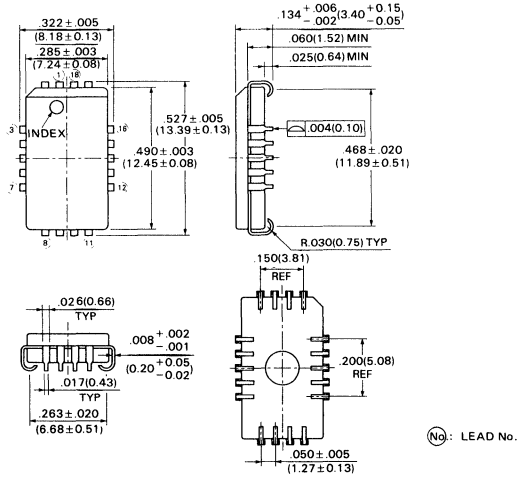
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Dimensions in inches (millimeters)

Standard 18-pin Plastic LCC (Suffix: -PD)

18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M04)

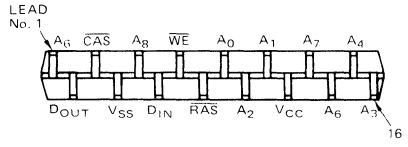


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

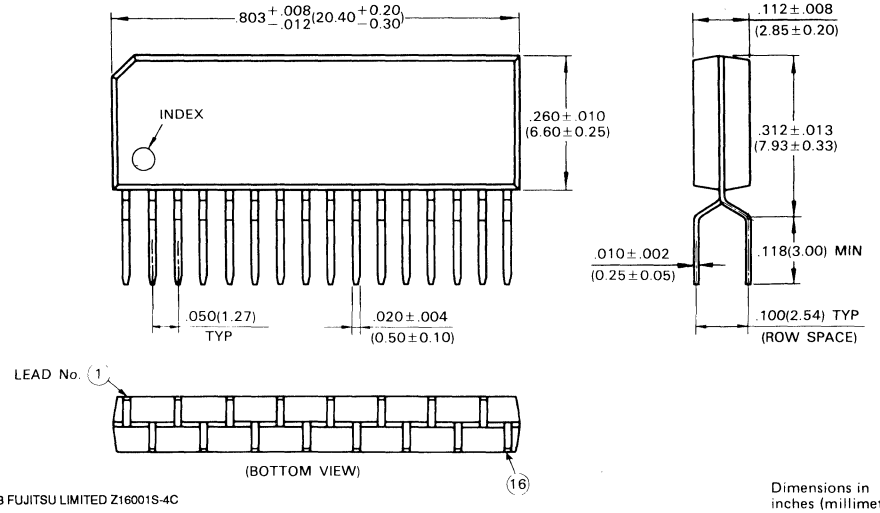
Standard 16-Pin Plastic ZIP(Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

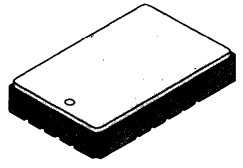
16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)



Dimensions in
inches (millimetres)

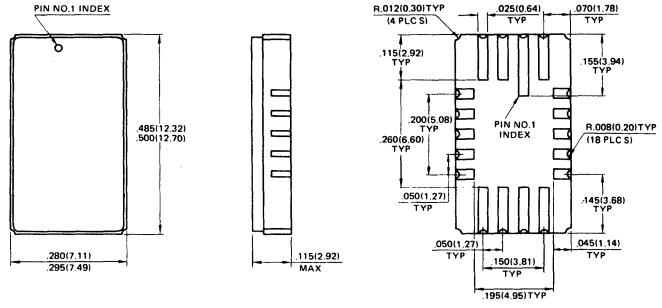
PACKAGE DIMENSIONS

Standard 18-pin Ceramic LCC (Suffix: -TV)



LCC-18C-F04

18-LEAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F04)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches (millimeters)

February 1990
Edition 1.0

FUJITSU

DATA SHEET

MB81257-80

MOS 262,144 BIT DYNAMIC RANDOM ACCESS MEMORY

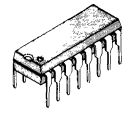
262,144 Bit Dynamic Random Access Memory

The Fujitsu MB81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and environments where low power dissipation and a compact layout are required.

Multiplexed row and column address inputs permit the MB81257 to be housed in standard 16-pin DIP and ZIP packages or an 18-pin PLCC package. Pinouts conform to the JEDEC- approved pinouts. Additionally, the MB81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before-$\overline{RAS}$ refresh provides an on-chip refresh capability that is upwardly compatible with the MB8266A. The MB81257 also features nibble mode which allows high speed serial access of up to 4 bits of data.

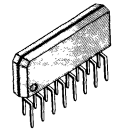
The MB81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible.

- 262,144 x 1 RAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time (t_{RAC}) 80 ns max. (MB 81257-80)
- Random Cycle Time (t_{RC}) 175 ns min. (MB 81257-80)
- Nibble Cycle Time 45 ns max. (MB 81257-80)
- Single +5 V Supply, ±10% tolerance
- Low Power 385 mW max. (MB 81257-80) 25 mW max. (standby)
- 256 refresh cycles every 4 ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-white-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} are eliminated
- Output unlatched cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-Pin Plastic Packages: DIP (MB81257-XXP) ZIP (MB81257-XXPSZ) Standard 18-Pin Plastic Package: PLCC(MB81257-XXPV) Standard 16-Pad Ceramic Package: DIP (MB81257-XXC)



PLASTIC PACKAGE
DIP-16P-M03

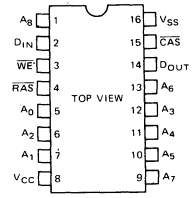
PLASTIC PACKAGE
LCC-18P-M04

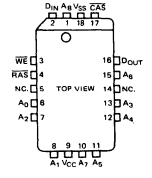


PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 19
DIP-16C-A04: See Page 20

PIN ASSIGNMENT





Pin assignment for ZIP: See page 23

Absolute Maximum Ratings (See Note)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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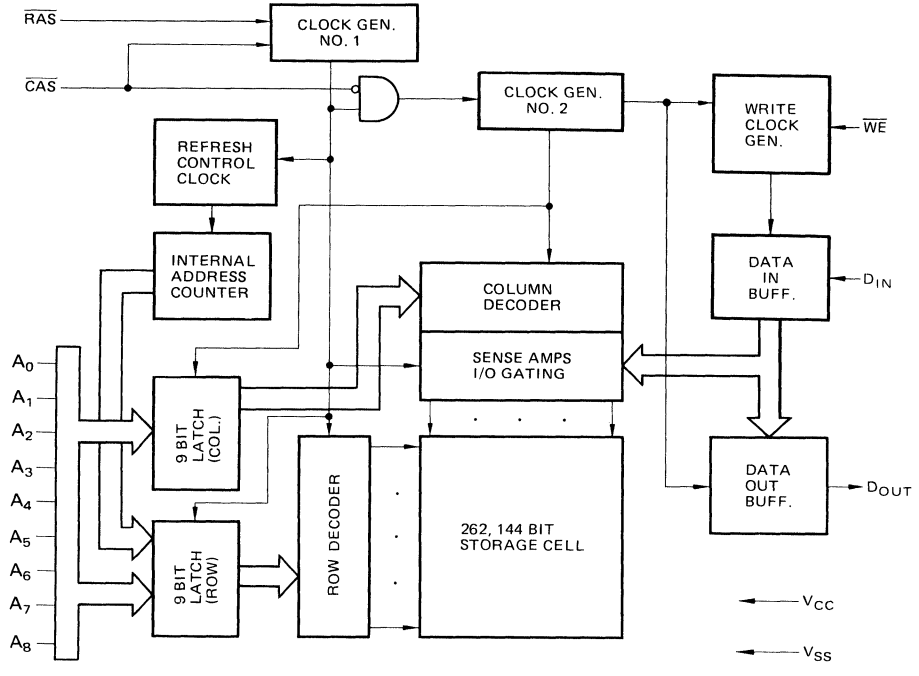
Fig. 1 – MB 81257 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		10	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.)	MB 81257-80	I_{CC1}			70	mA
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81257-80	I_{CC3}			60	mA
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = Min.)	MB 81257-80	I_{CC4}			22	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81257-80	I_{CC5}			65	mA
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = -5.0mA)		V_{OH}	2.4			V

NOTE* : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
Time between Refresh		t_{REF}		4	ms
Random Read/Write Cycle Time		t_{RC}	175		ns
Read-Write Cycle Time		t_{RWC}	180		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		80	ns
Access Time from $\overline{CAS}$	4 6	t_{CAC}		45	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	ns
Transition Time		t_T	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	85	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	50	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	85		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	35	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		ns
Row Address Set Up Time		t_{ASR}	0		ns
Row Address Hold Time		t_{RAH}	10		ns
Column Address Set Up Time		t_{ASC}	0		ns
Column Address Hold Time		t_{CAH}	15		ns
Read Command Set Up Time		t_{RCS}	0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		ns
Write Command Set Up Time	10	t_{WCS}	0		ns
Write Command Pulse Width		t_{WP}	15		ns
Write Command Hold Time		t_{WCH}	15		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		ns
Data In Set Up Time		t_{DS}	0		ns
Data In Hold Time		t_{OH}	15		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

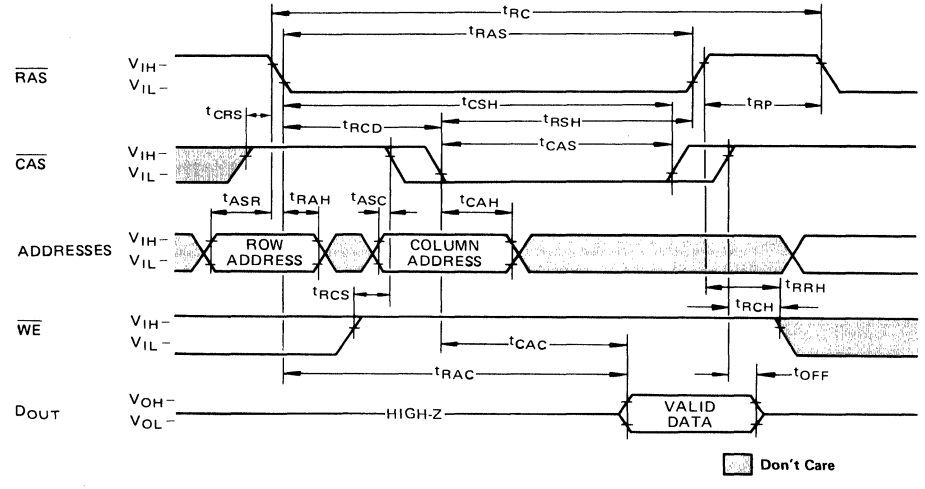
Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	45		ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	45		ns
Nibble Mode Access Time		t_{NCAC}		18	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	20		ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15		ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	20		ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	35		ns
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	20		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		ns

Notes:

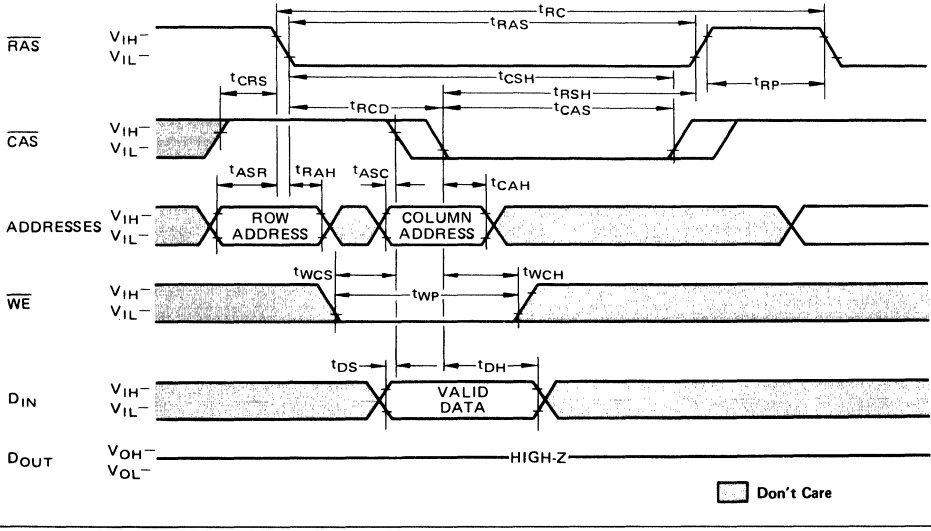
1. An initial pause of 200 μs is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

1

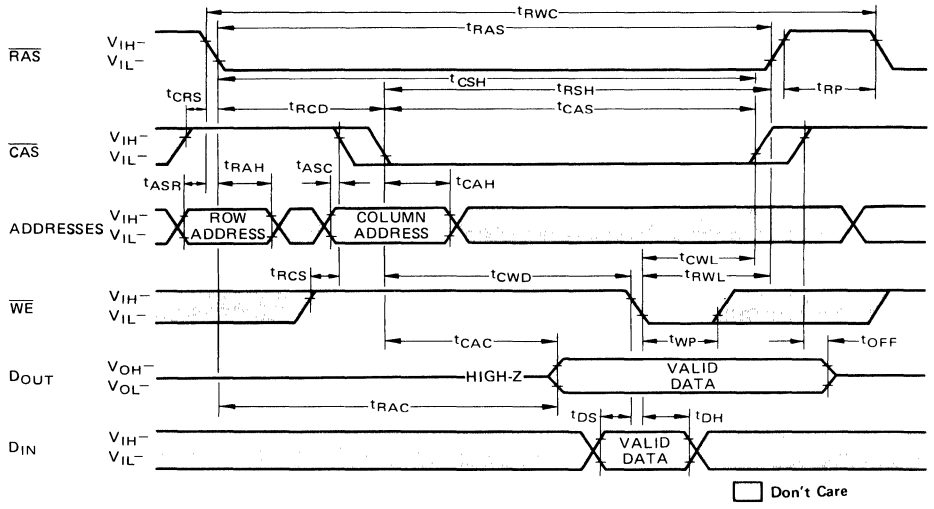
Read Cycle



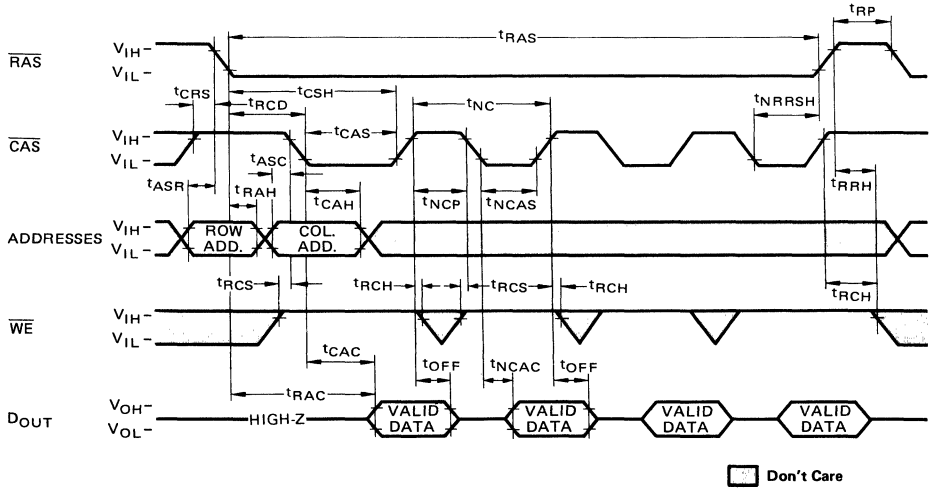
Write Cycle (Early Write)



Read–Write/Read–Modify–Write Cycle



Nibble Mode Read Cycle



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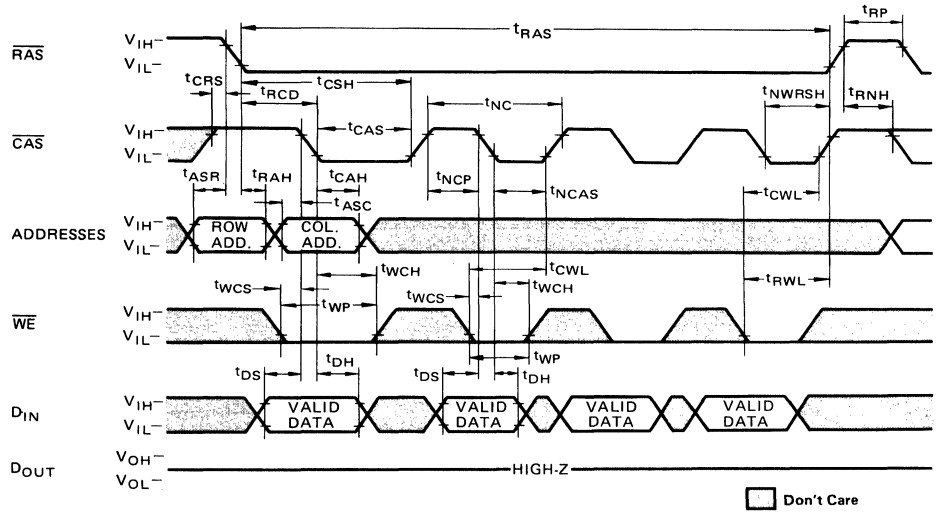
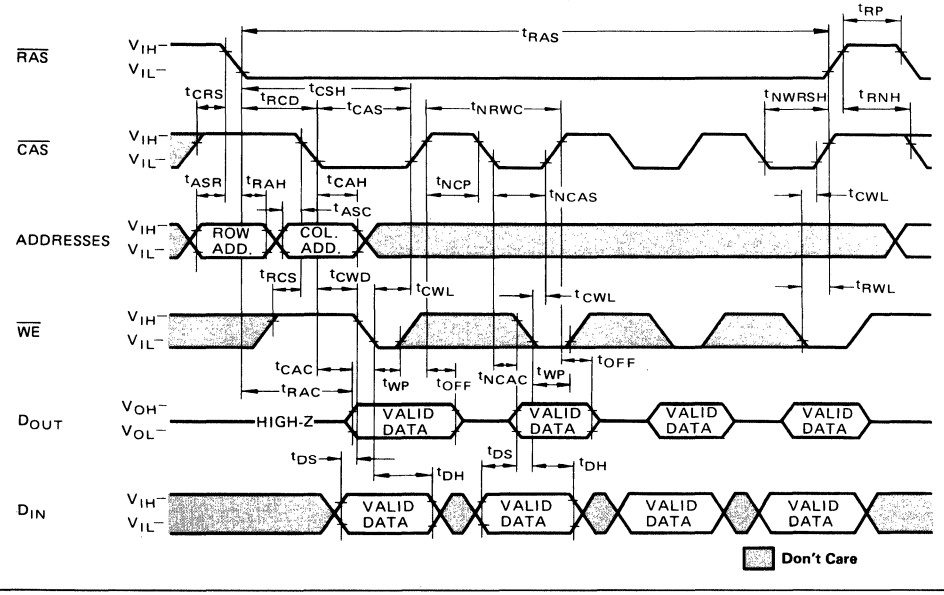
Nibble Mode Write Cycle (Early Write)

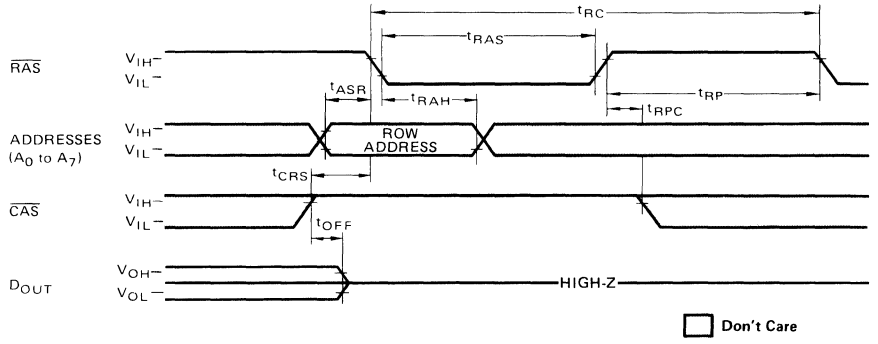


Nibble Mode Read-Write Cycle



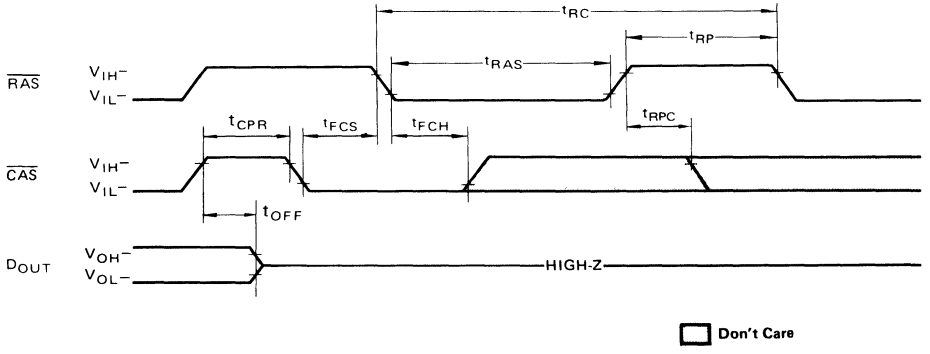
$\overline{RAS}$-only Refresh cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, $A_8 = V_{IH}$ or V_{IL}



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Address, $\overline{WE}$, D_{IN} = Don't care



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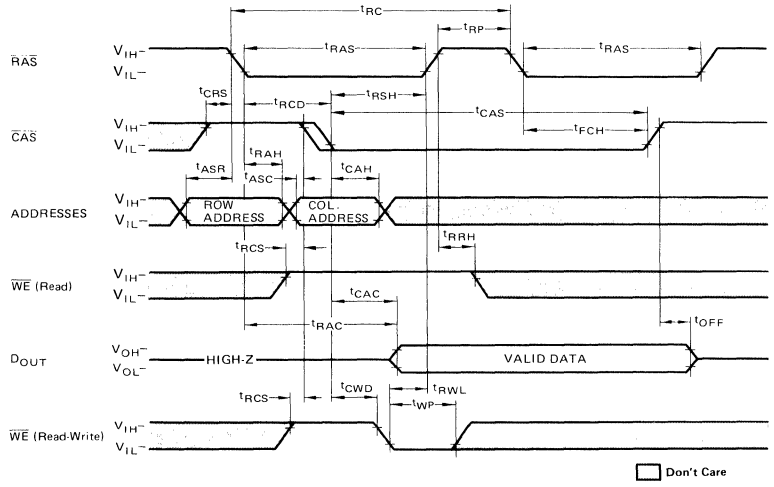
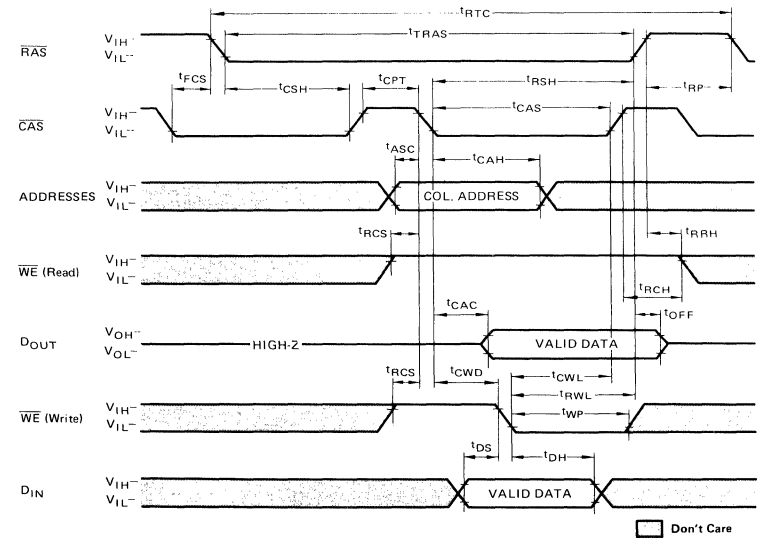
Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement
The MB 81257 has improved circuitry that eases timing requirements for high speed access operations. The MB 81257 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81257 has the minimal hold times of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81257 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81257. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode; low selects write mode. The data input is disabled when read mode is selected.

Data Input:
Data is written into the MB 81257 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.) Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle
The MB 81257 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings, described in the previous section. The output buffer is controlled by the sate of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle is possible with the MB 81257.

Nibble Mode:
Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).
If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.
In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.
The data output is controlled only by the $\overline{WE}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain high impedance state throughout the succeeding nibble cycle regardless of the $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{WE}$ state. The write operation is done during the period in which the $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit).
See Fig. 2.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 ms.
The MB 81257 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;
The $\overline{RAS}$ only refresh aboids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each

of 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81257 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh;
A hidden refresh cycle may takes place while maintaining latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB 81257, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counters provide the refresh addresses, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

CAS-before-RAS Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

- *A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.
- *A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for the following operations:

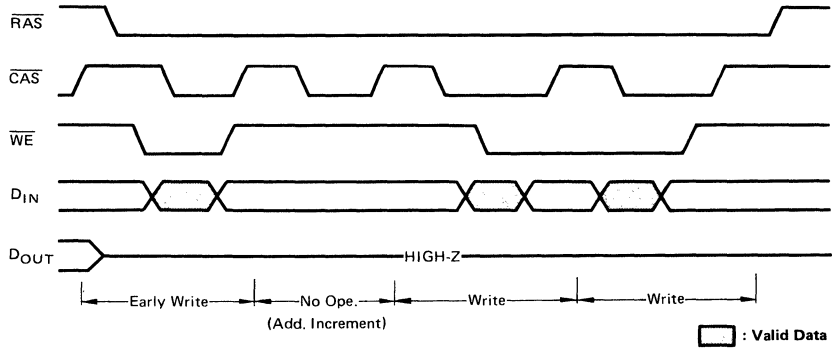
1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address, and keep RA8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

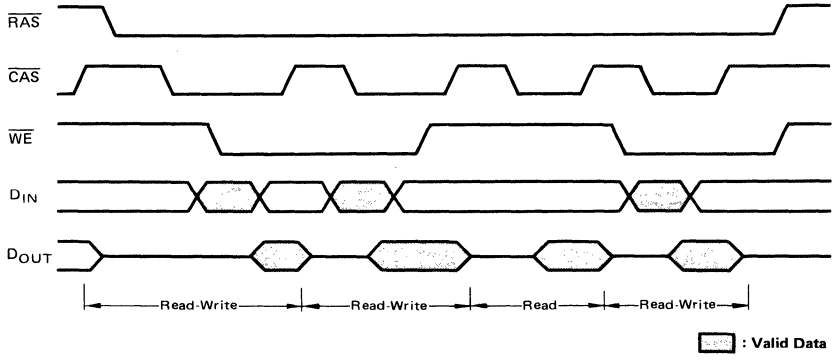
SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Fig. 2 – Nibble Mode

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)

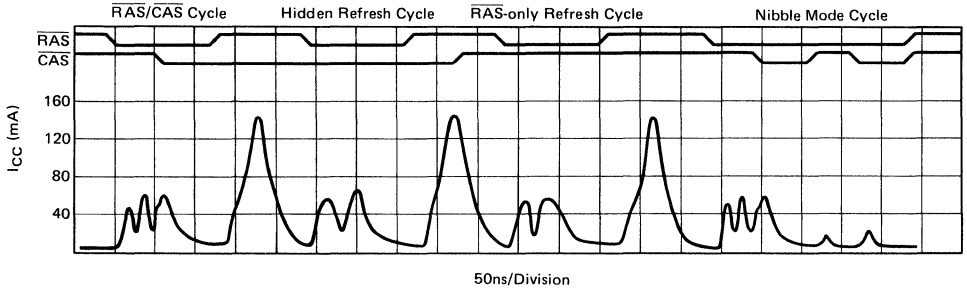


1

Table-2 FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geqq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write ($t_{CWD} \geqq t_{CWD}$ (min))
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Fig. 3 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

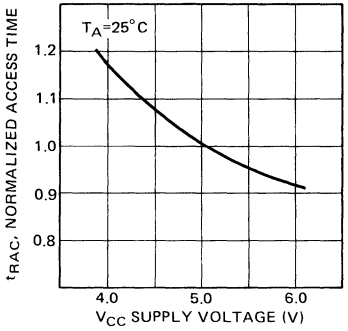


Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

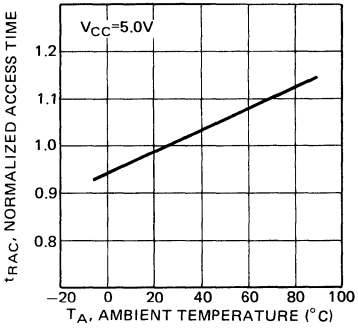


Fig. 6 – OPERATING CURRENT vs CYCLE RATE

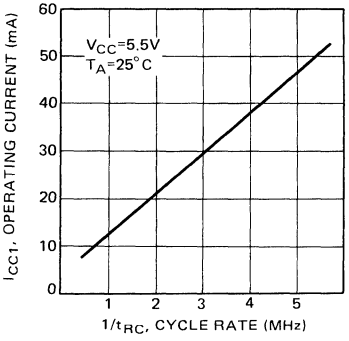


Fig. 7 – OPERATING CURRENT vs SUPPLY VOLTAGE

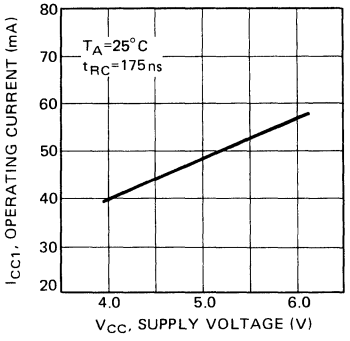


Fig. 8 – OPERATING CURRENT vs AMBIENT TEMPERATURE

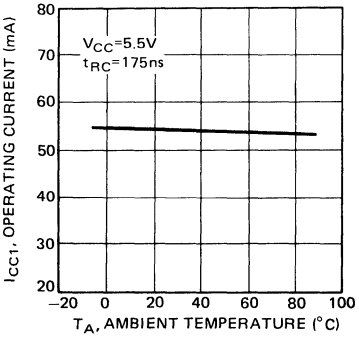


Fig. 9 – STANDBY CURRENT vs SUPPLY VOLTAGE

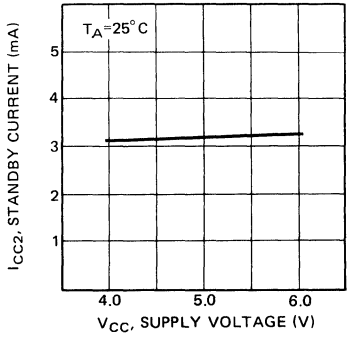


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Fig. 10 – STANDBY CURRENT vs AMBIENT TEMPERATURE

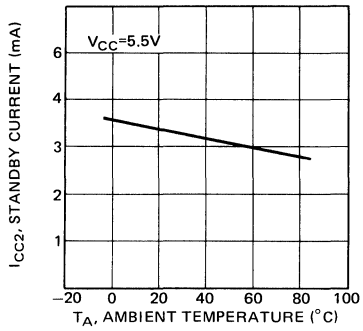


Fig. 11– REFRESH CURRENT 1 vs CYCLE RATE

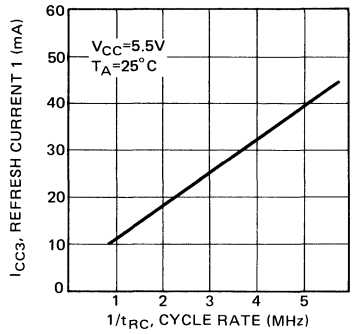


Fig. 12 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

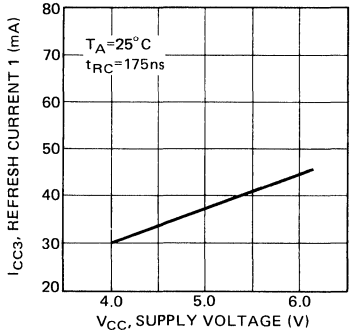


Fig. 13 – NIBBLE MODE CURRENT vs CYCLE RATE

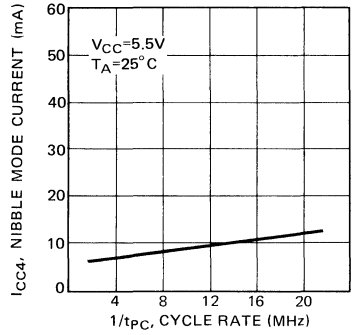


Fig. 14 – NIBBLE MODE CURRENT vs SUPPLY VOLTAGE

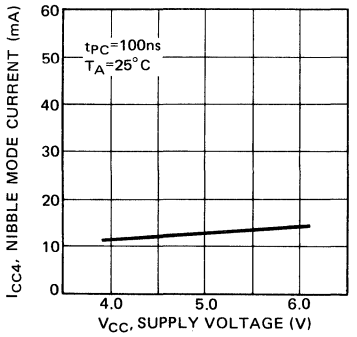


Fig. 15 – REFRESH CURRENT 2 vs CYCLE RATE

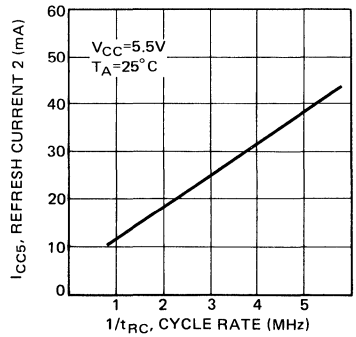


Fig. 16 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

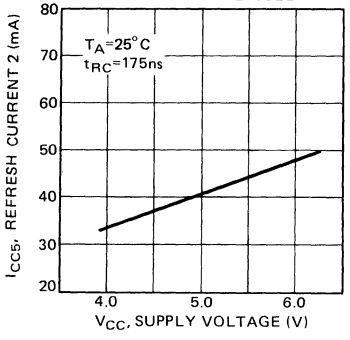


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

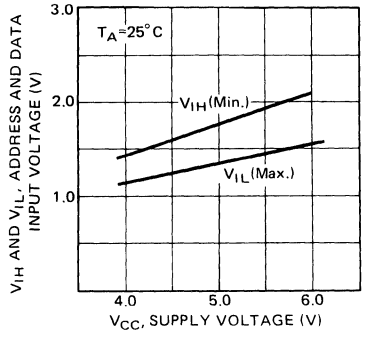


Fig. 18 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

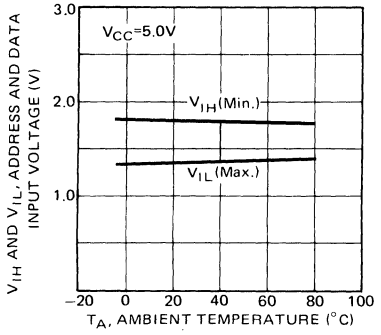


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

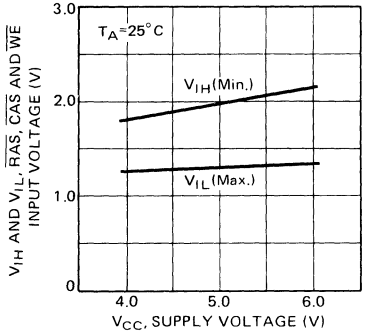


Fig. 20 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

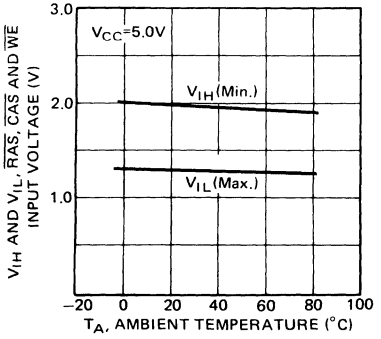
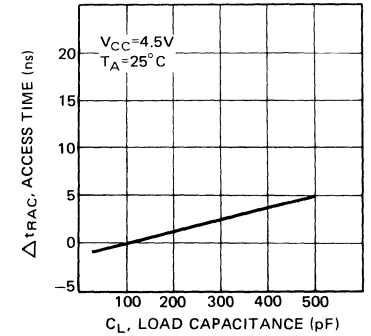


Fig. 21 – ACCESS TIME vs LOAD CAPACITANCE



1

Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

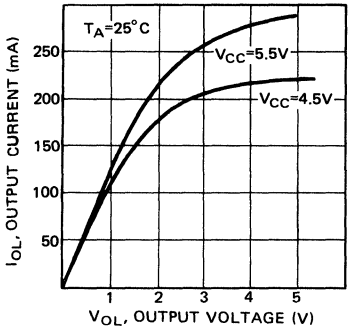


Fig. 23 – OUTPUT CURRENT vs OUTPUT VOLTAGE

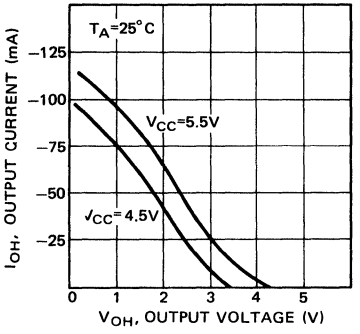


Fig. 24 – CURRENT WAVEFORM DURING POWER UP

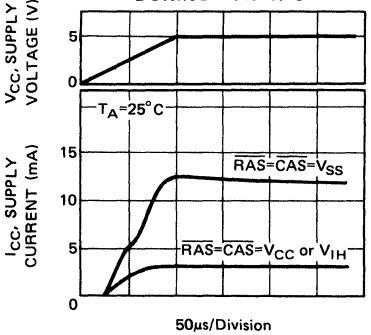
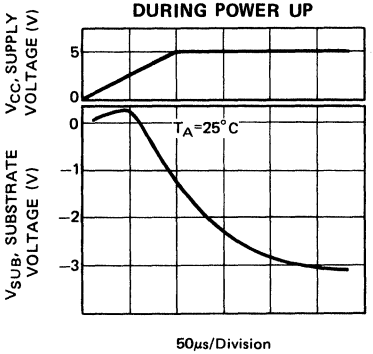
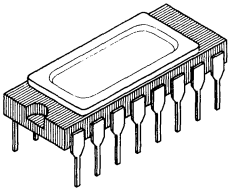


Fig. 25 – SUBSTRATE VOLTAGE DURING POWER UP



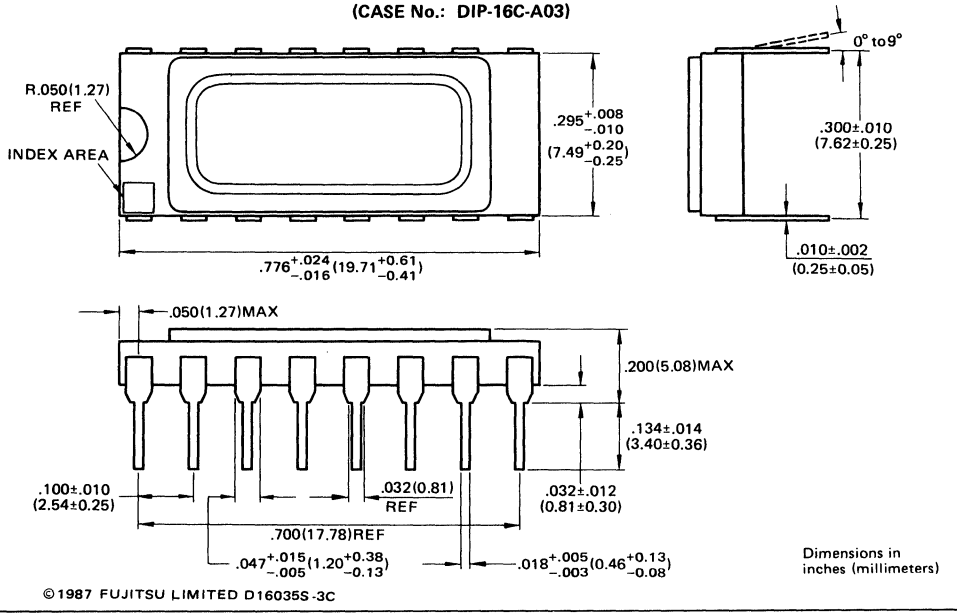
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-16C-A03

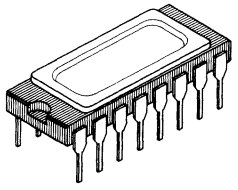
16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)



Dimensions in inches (millimeters)

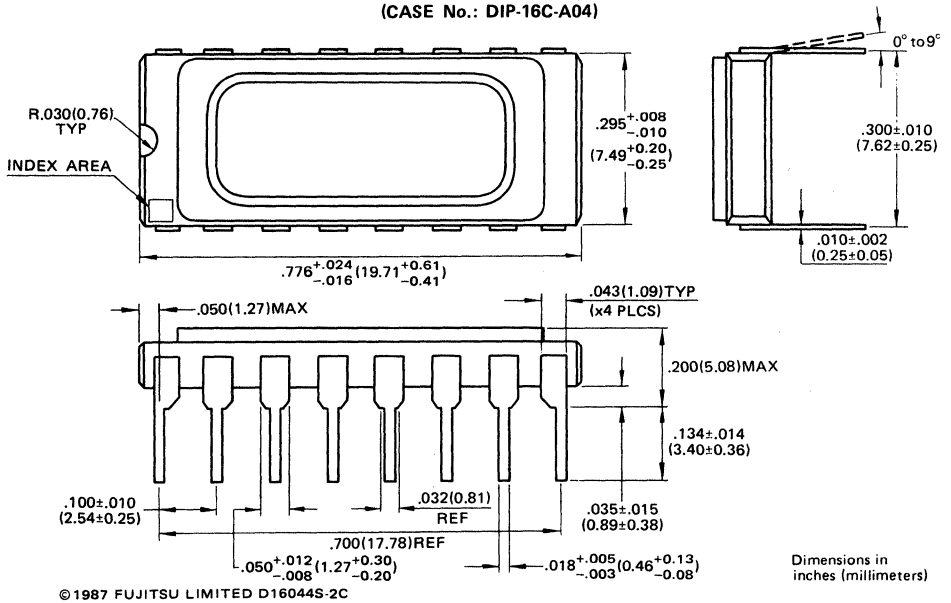
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-16C-A04

16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A04)

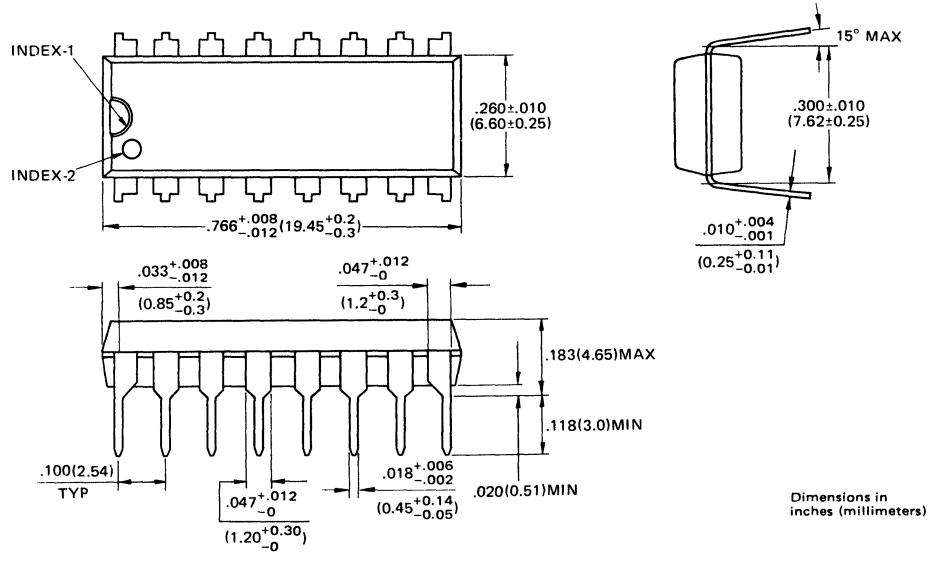


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Dimensions in inches (millimeters)

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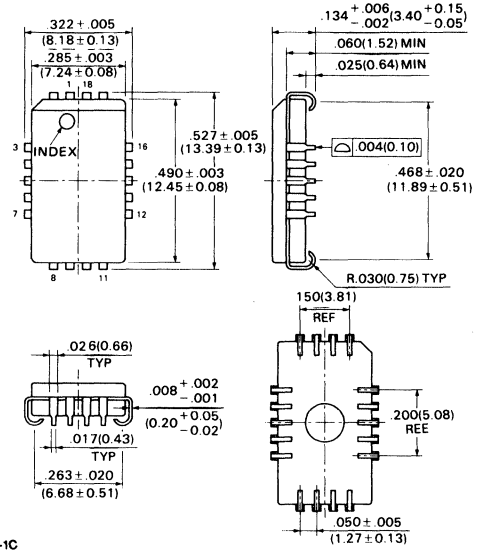
PACKAGE DIMENSIONS

(Suffix: -PD)

18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M04)

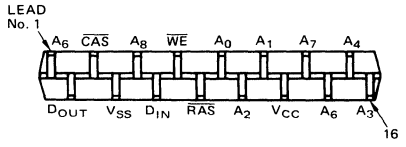


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

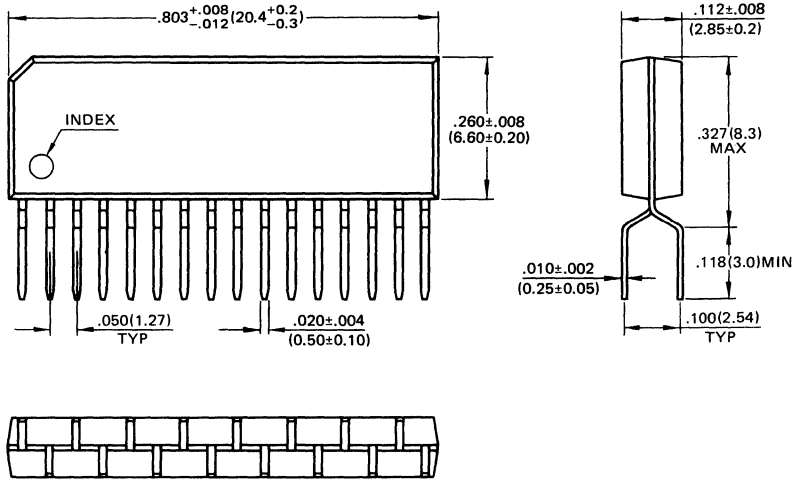
(Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)



Dimensions in
inches (millimeters)

1

October 1990
Edition 6.0

FUJITSU

DATA SHEET

MB81464-12/-15

MOS 262,144 BIT DYNAMIC RANDOM ACCESS MEMORY

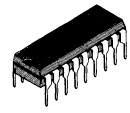
65,536 x 4 Bits Dynamic Random Access Memory

The Fujitsu MB81464 is a fully decoded, dynamic random access memory organized as 65,536 words by 4 bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and system memory for microprocessor units where low power dissipation and a compact layout is required.

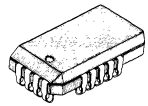
The multiplexed row and column address inputs permit the MB81464 to be housed in standard 18-pin DIP and PLCC, or 20-pin ZIP packages. Additionally, the MB81464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. The $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle provides an on-chip refresh capability. The MB81464 also features page mode which allows high speed random access of up to 256 bits within the same row.

The MB81464 uses silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process technology. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are non critical, and power supply tolerance is very wide. All inputs are TTL compatible.

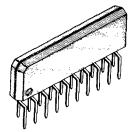
- 65,536 x 4 DRAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time (t_{RAC})
  120 ns max. (MB 81464-12)
  150 ns max. (MB 81464-15)
- Cycle Time (t_{RC})
  220 ns min. (MB 81464-12)
  260 ns min. (MB 81464-15)
- Page Cycle Time (t_{PC})
  120 ns max. (MB 81464-12)
  145 ns max. (MB 81464-15)
- Single +5 V Supply, ±10% tolerance
- Low Power
  358 mW max. (MB 81464-12)
  314 mW max. (MB 81464-15)
  27.5 mW max. (standby)
- On-chip substrate bias generator for high performance
- All inputs/outputs are TTL compatible
- 4 ms/256 refresh cycles
- Early write or $\overline{OE}$ controlled write capacity
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- Read write capability
- On-chip latches for addresses and DQs
- Compatible with μPD41254, HM50464, and TM4464
- Standard 18-Pin Plastic Packages:
  DIP (MB81464-XXP)
  PLCC (MB81464-XXPV)
  Standard 20-Pin Plastic Package:
  ZIP (MB81464-XXPSZ)
  Standard 18-Pin Ceramic Package:
  DIP (MB81464-XXC) Metal Seal



PLASTIC PACKAGE
DIP-18P-M03



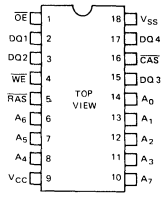
PLASTIC PACKAGE
LCC-18P-M04

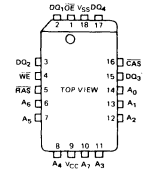


PLASTIC PACKAGE
ZIP-20P-M01

DIP-18C-A01: See Page 22

PIN ASSIGNMENT





Pin assignment for ZIP: See page 21

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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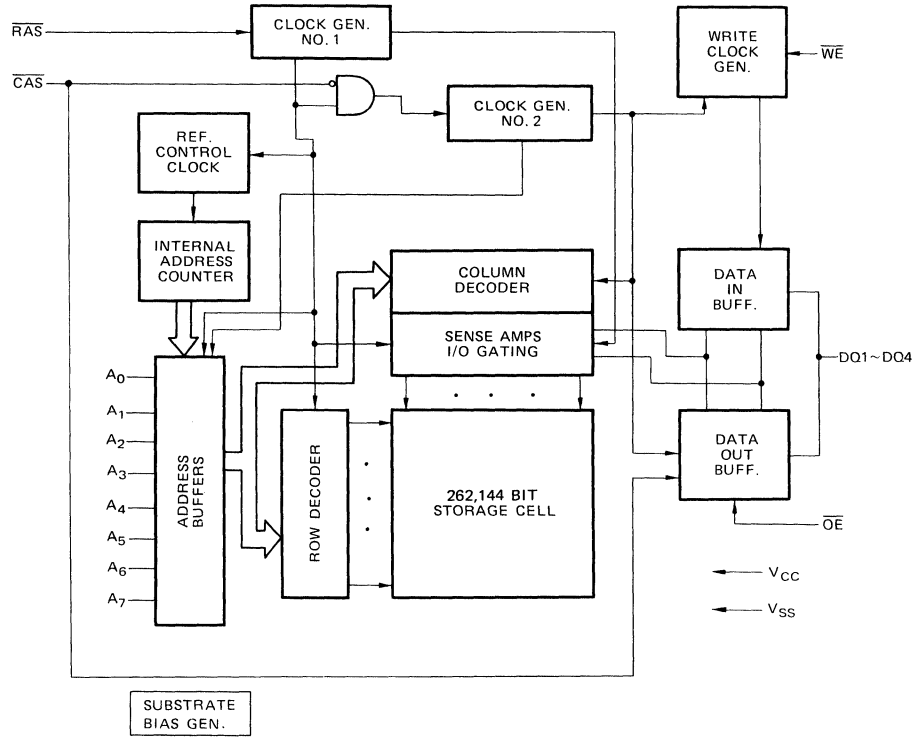
Fig. 1 – MB 81464 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance A_0 to A_7	C_{IN1}	–	7	pF
Input Capacitanct $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	–	10	pF
Data I/O Capacitance (DQ1 to DQ4)	C_{DQ}	–	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to 70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	-2.0	–	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	-1.0	–	0.8	V	

* The device will withstand undershoots to the -2.0 V level with a maximum pulse width of 20 ns at the -1.5 V level.

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81464-12	I_{CC1}			65	mA
	MB 81464-15				57	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}			5.0	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81464-12	I_{CC3}			55	mA
	MB 81464-15				50	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling; t_{PC} = min)	MB 81464-12	I_{CC4}			35	mA
	MB 81464-15				30	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81464-12	I_{CC5}			60	mA
	MB 81464-15				55	
INPUT LEAKAGE CURRENT any input (0V ≦ V_{IN} ≦ 5.5V, 4.5V ≦ V_{CC} ≦ 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0 V ≦ V_{OUT} ≦ 5.5 V)		$I_{DQ(L)}$	-10		10	μA
OUTPUT LEVEL Output High Voltage (I_{OH} = -5 mA)		V_{OH}	2.4			V
OUTPUT LEVEL Output Low Voltage (L_{OL} = 4.2 mA)		V_{OL}			0.4	V

* : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
I_{CC} is dependent on input low voltage level V_{ILD}, V_{ILD} > -0.5 V.

1

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter NOTES	Symbol	MB 81464-12		MB 81464-15		Unit
		Min	Max	Min	Max	
Time between Refresh	t_{REF}		4		4	ms
Random Read/Write Cycle Time	t_{RC}	220		260		ns
Read-Modify-Write Cycle Time	t_{RWC}	305		345		ns
Page Mode Cycle Time	t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$ 4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$ 5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay	t_{OFF}	0	25	0	30	ns
Transition Time	t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	60		75		ns
$\overline{CAS}$ Precharge Time (Page mode only)	t_{CP}	50		60		ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)	t_{CPN}	32		35		ns
$\overline{CAS}$ Pulse Width	t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time 7 8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	10		10		ns
Row Address Set Up Time	t_{ASR}	0		0		ns
Row Address Hold Time	t_{RAH}	12		15		ns
Column Address Set Up Time	t_{ASC}	0		0		ns
Column Address Hold Time	t_{CAH}	20		25		ns
Read Command Set Up Time	t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ 9	t_{RRH}	15		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$ 9	t_{RCH}	0		0		ns
Write Command Set Up Time 10	t_{WCS}	−5		−5		ns
Write Command Hold Time	t_{WCH}	30		35		ns
Write Command Pulse Width	t_{WP}	30		35		ns
Write Command to $\overline{RAS}$ Lead Time 10	t_{RWL}	40		45		ns

AC CHARACTERISTICS (cont'd)

(At recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 81464-12		MB 81464-15		Unit
			Min	Max	Min	Max	
Write Command to $\overline{CAS}$ Lead Time	10	t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from $\overline{OE}$		t_{OEA}		30		40	ns
$\overline{OE}$ to Data In Delay Time		t_{OED}	25		30		ns
Output Buffer Turn Off Delay from $\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$		t_{OEH}	0		0		ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCS}	20		20		ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time (Refresh cycles)		t_{RPC}	10		10		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycles)		t_{CPR}	30		30		ns
$\overline{OE}$ to $\overline{RAS}$ in active Set Up Time		t_{OES}	0		0		ns
D_{IN} to $\overline{CAS}$ Delay Time	11	t_{DZC}	0		0		ns
D_{IN} to $\overline{OE}$ Delay Time	11	t_{DZO}	0		0		ns
Refresh Counter Test Cycle Time	12	t_{RTC}	430		505		ns
Refresh Counter Test Cycle $\overline{RAS}$ Pulse Width	12	t_{TRAS}	330	10000	395	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	12	t_{CPT}	60		70		ns

Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5 ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. Even if $t_{WCS} \leqq t_{WCS}$(min), the write cycle can be excuted by satisfying t_{RWL} or t_{CWL} specification.
11. Either t_{DZC} or t_{DRO} must be satisfied for all cycles.
12. Refresh Counter Test Cycle only.

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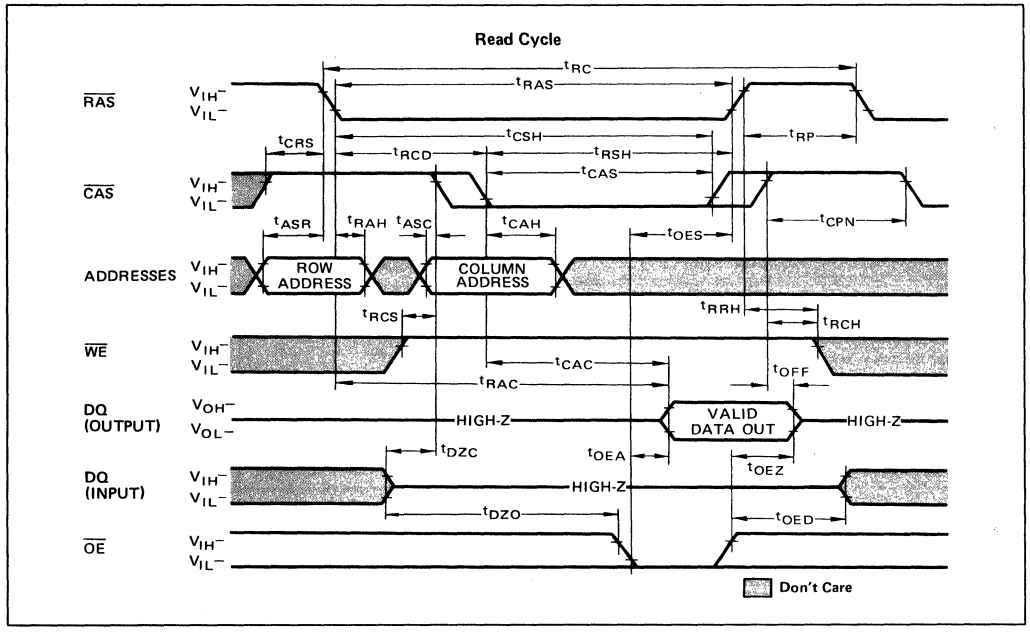
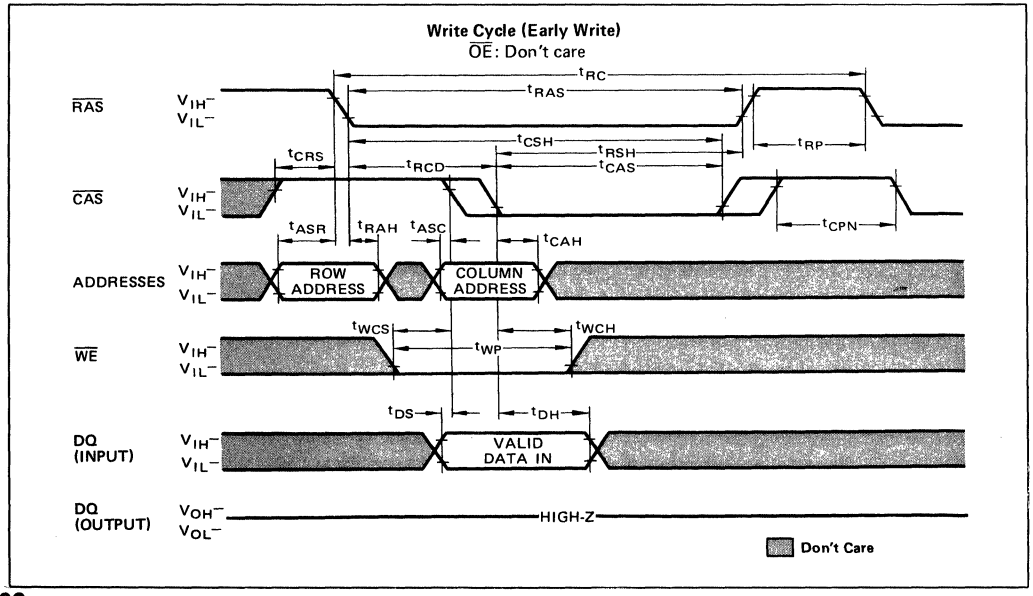
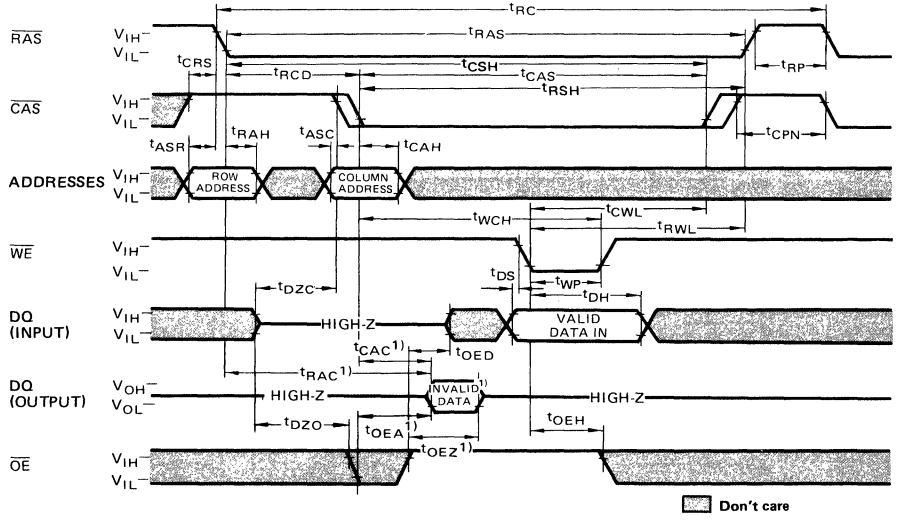
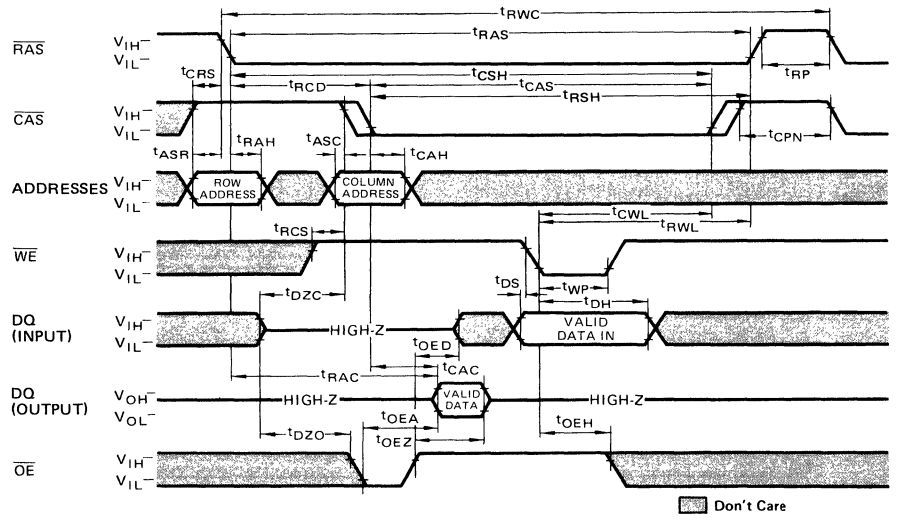

Read Cycle
RAS
CAS
ADDRESSES
WE
DQ (OUTPUT)
DQ (INPUT)
OE
VIH
VIL
VOH
VOL
tRC
tRAS
tRP
tCRS
tRCD
tCSH
tRSH
tCAS
tCPN
tASR
tRAH
tASC
tCAH
tOES
ROW ADDRESS
COLUMN ADDRESS
tRRH
tRCH
tRCS
tCAC
tOFF
tRAC
HIGH-Z
VALID DATA OUT
tDZC
tOEA
tOEZ
tDZO
tOED
Don't Care


Write Cycle (Early Write)
OE: Don't care
RAS
CAS
ADDRESSES
WE
DQ (INPUT)
DQ (OUTPUT)
VIH
VIL
VOH
VOL
tRC
tRAS
tRP
tCRS
tRCD
tCSH
tRSH
tCAS
tCPN
tASR
tRAH
tASC
tCAH
ROW ADDRESS
COLUMN ADDRESS
tWCS
tWCH
tWP
tDS
tDH
VALID DATA IN
HIGH-Z
Don't Care

$\overline{OE}$ Write Cycle



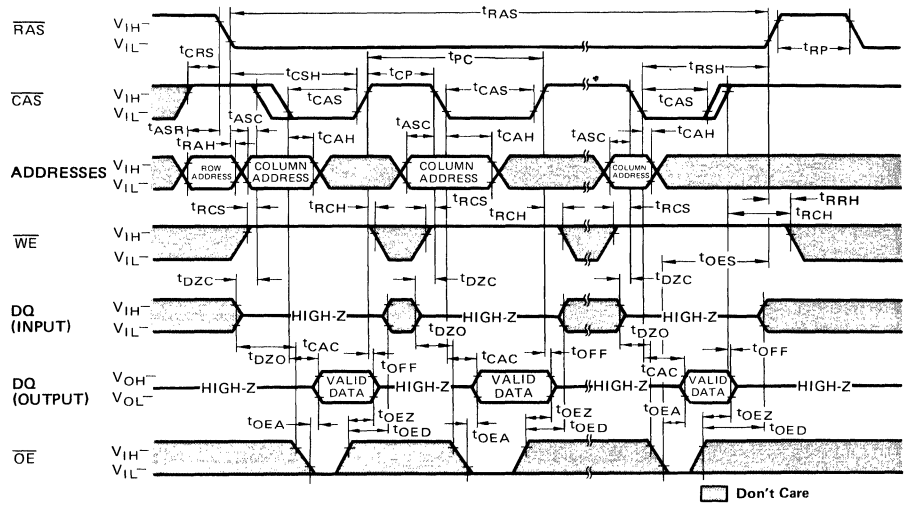
Read-Modify-Write Cycle



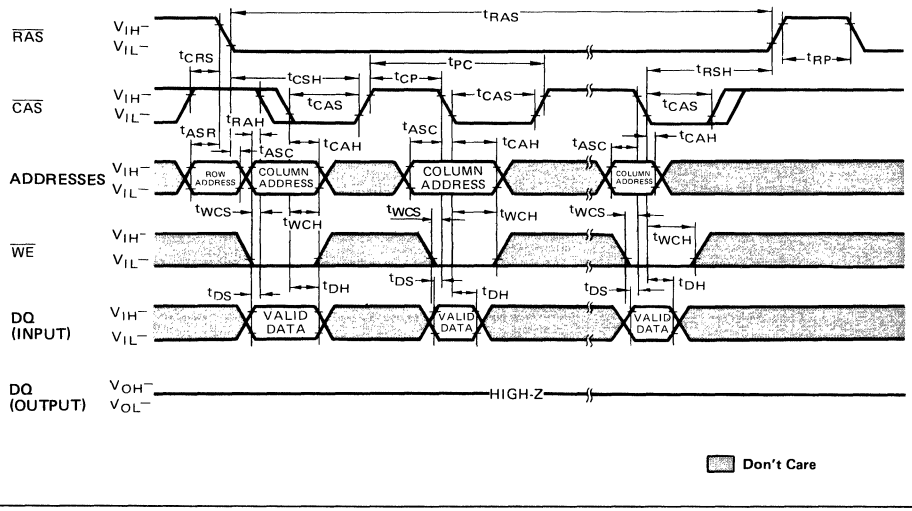
Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.

1

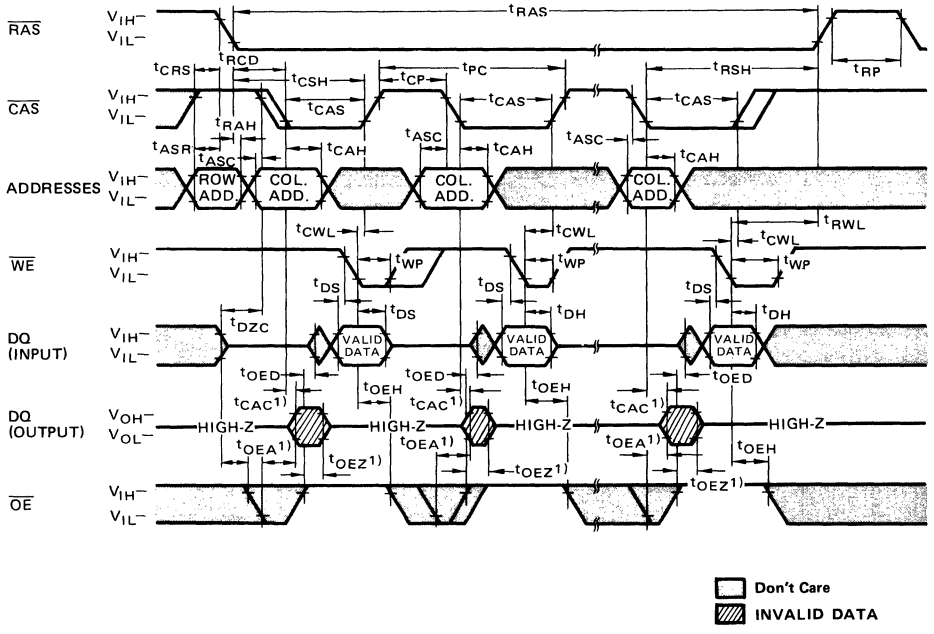
Page Mode Read Cycle



Page Mode Write Cycle
(OE=Don't Care)



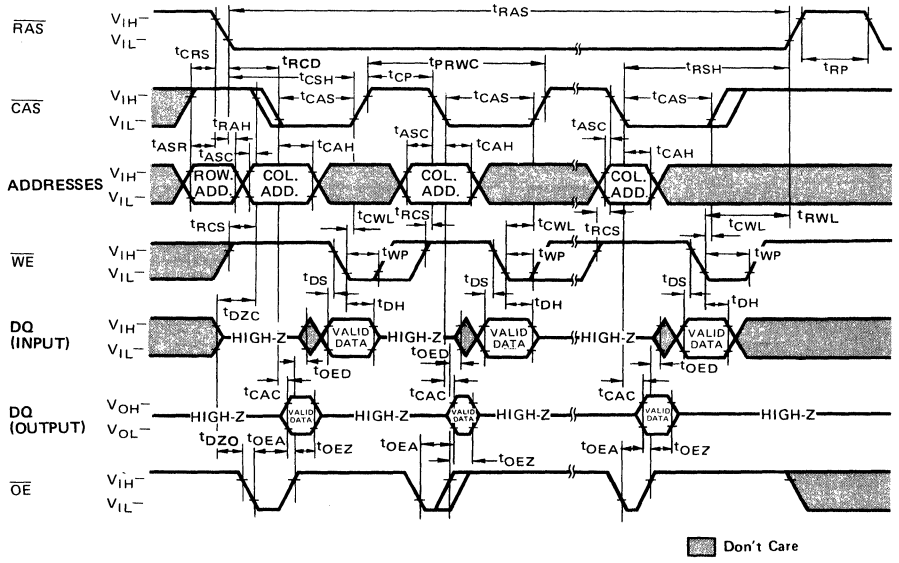
Page Mode $\overline{OE}$ Write Cycle



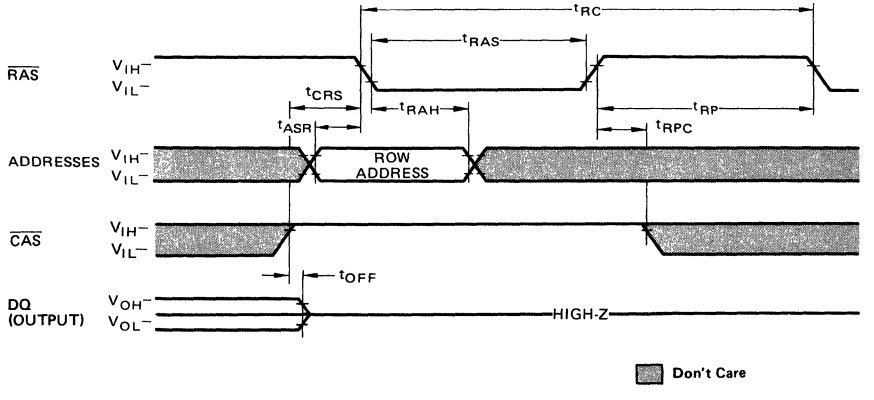
Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.

1

Page Mode Read Modify-Write Cycle

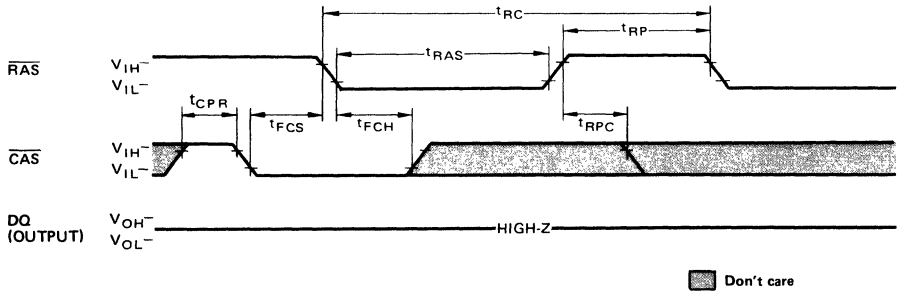


RAS-Only Refresh Cycle
(WE, OE=Don't Care)

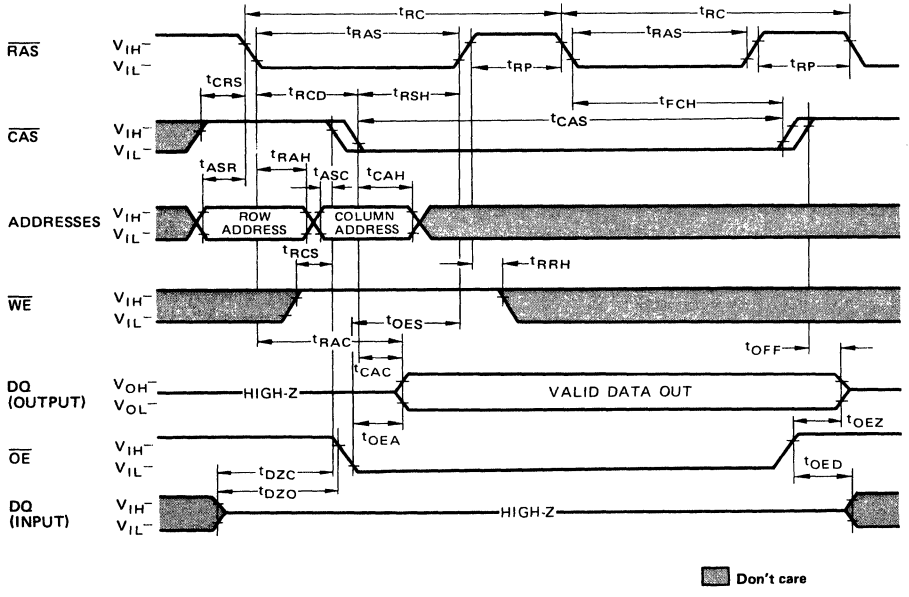


CAS-before-RAS Refresh Cycle

NOTE: Addresses, WE, OE = Don't care



Hidden Refresh Cycle



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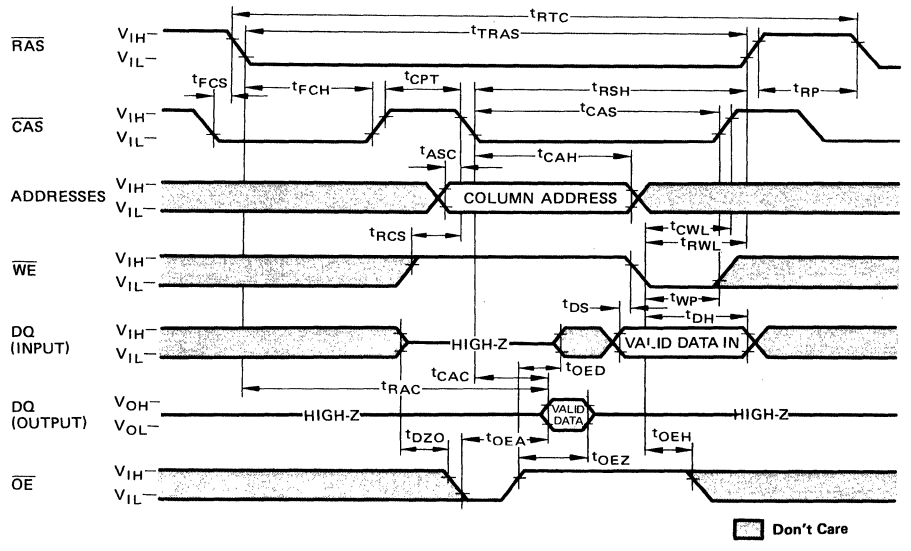
Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode parallel 4 bits of 262,144 storage cell locations within the MB 81464.

Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins (A_0 through A_7) and latched with the Column Address Strobe ($\overline{CAS}$).

The row and column address inputs must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the Write Enable ($\overline{WE}$) input. A high on $\overline{WE}$ selects read mode and low selects write mode. The data inputs are disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data-outs will remain in the high-impedance state allowing a write cycle.

Data Pins:

Data Inputs;

Data are written during a write or read-modify-write cycle. The later falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed by $\overline{CAS}$ with setup and hold times referenced to $\overline{CAS}$. In a read-modify-write cycle, thus the data will be strobed by $\overline{WE}$ with set-up and hold times referenced to $\overline{WE}$.

In a read-modify-write cycle, $\overline{OE}$ must be low after t_{DZO} to change the data pins from input mode to output mode and then $\overline{OE}$ must be changed to low before t_{OED} to return the data pins to input mode. In an early write cycle, data pins are in input mode regardless of the status of $\overline{OE}$.

Data Outputs;

The three-state output buffers provide direct TTL compatibility with a fan out of two standard TTL loads. Data-out are the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle, the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. In a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high brings the outputs into the high impedance state.

Output Enable:
The $\overline{OE}$ controls the impedance of the output buffers. In the high state on $\overline{OE}$, the output buffers are high impedance state. In the low state on $\overline{OE}$, the output buffers are low impedance state. But in early write cycle, the output buffers are in high impedance state even if $\overline{OE}$ is low. In the page mode read cycle, $\overline{OE}$ can be allowed low through the cycle. In the page mode early write cycle, $\overline{OE}$ can be allowed high throughout the cycle. In the page mode read-modify-write or delayed write cycle, $\overline{OE}$ must be changed from low to high with t_{OED}.

Page Mode:
Page Mode operation permits strobing the row-address into the MB 81464 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh;
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 through A_7) at least every four milliseconds.
The MB 81464 offeres the following three types of refresh.

$\overline{RAS}$-Only Refresh:
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffuers are in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81464 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and a internal refresh operation takes place.
After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh:
Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time.
In MB 81464, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses i.e., it doesn't need to apply refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in the cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

*A ROW ADDRESS – All bits are defined by the refresh counter.
*A COLUMN ADDRESS – All the bits A_0 to A_7 are defined by latching levels on A_0 to A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for the following operations:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

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Fig. 2 – CURRENT WAVEFORM (V_{CC} = 5.5 V, T_A = 25°C)

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

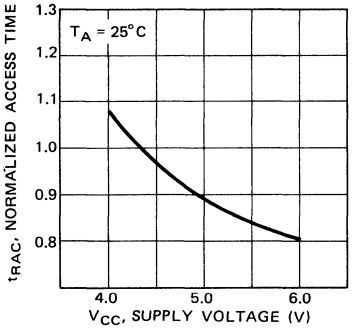

Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

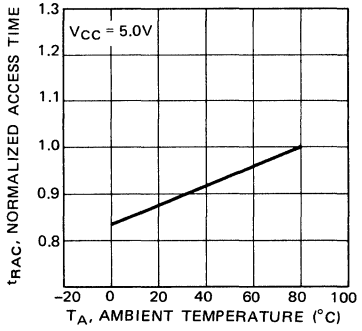

Fig. 5 – OPERATING CURRENT vs. CYCLE RATE

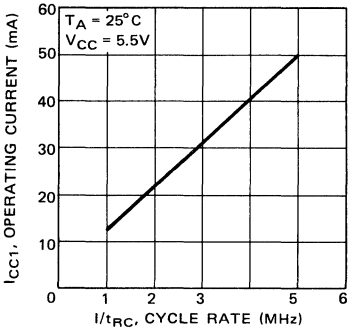

Fig. 6 – OPERATING CURRENT vs. SUPPLY VOLTAGE

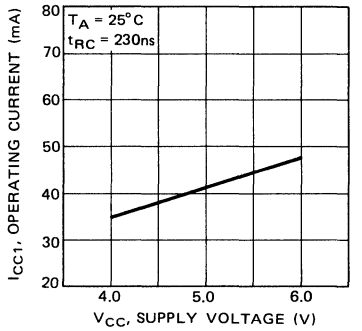

Fig. 7 – OPERATING CURRENT vs. AMBIENT TEMPERATURE

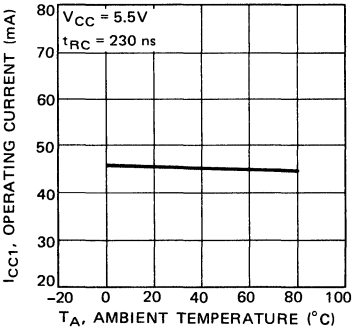

Fig. 8 – STANDBY CURRENT vs. SUPPLY VOLTAGE

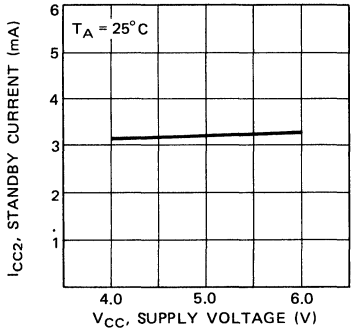

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Fig. 9 – STANDBY CURRENT vs. AMBIENT TEMPERATURE

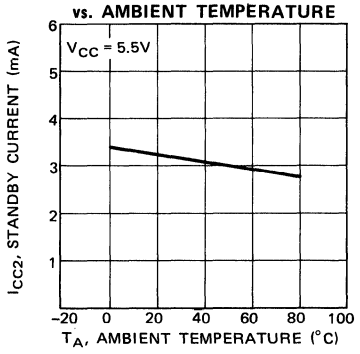


Fig. 10 – REFRESH CURRENT 1 vs. CYCLE RATE

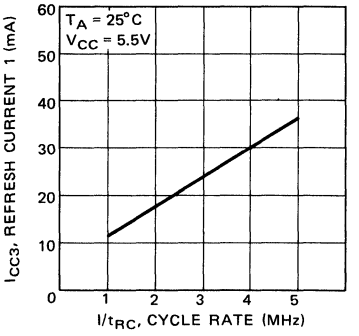


Fig. 11 – REFRESH CURRENT 1 vs. SUPPLY VOLTAGE

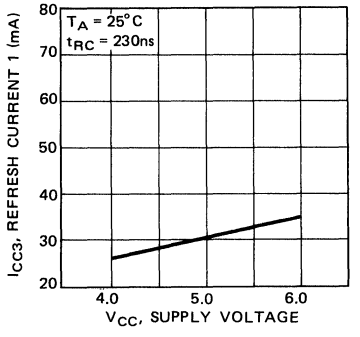


Fig. 12 – PAGE MODE CURRENT vs. CYCLE RATE

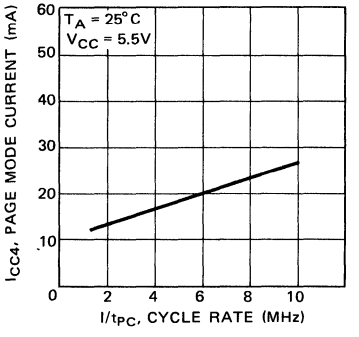


Fig. 13 – PAGE MODE CURRENT vs. CYCLE RATE

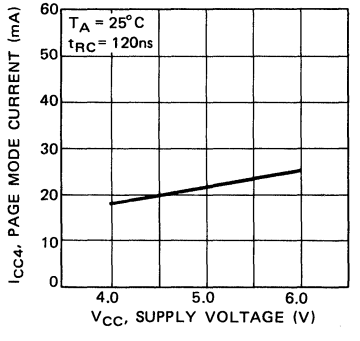


Fig. 14 – REFRESH CURRENT 2 vs. CYCLE RATE

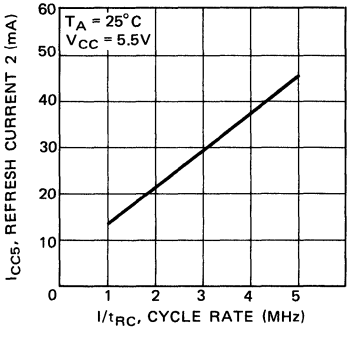


Fig. 15 – REFRESH CURRENT 2 vs. SUPPLY VOLTAGE

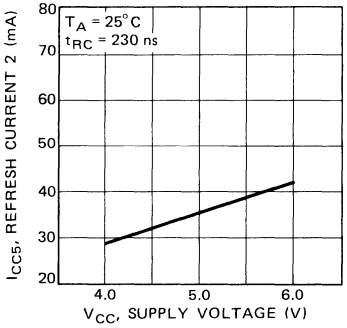


Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs. SUPPLY VOLTAGE

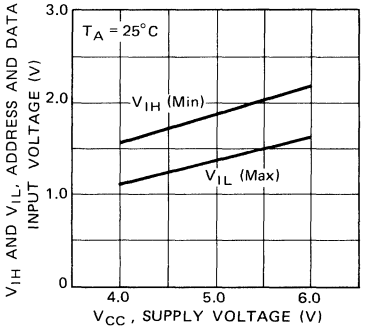


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs. AMBIENT TEMPERATURE

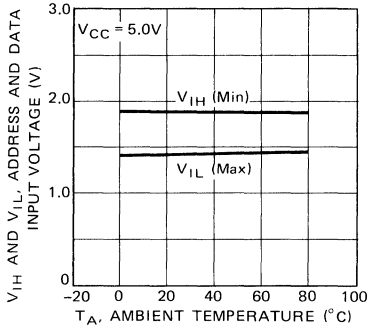


Fig. 18 – $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. SUPPLY VOLTAGE

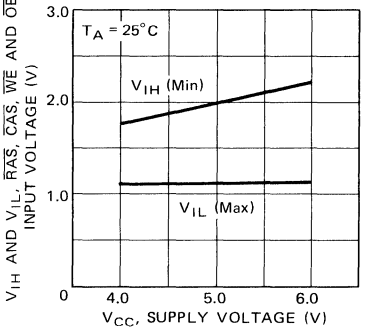


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. AMBIENT TEMPERATURE

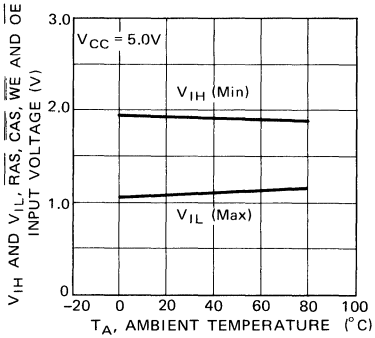
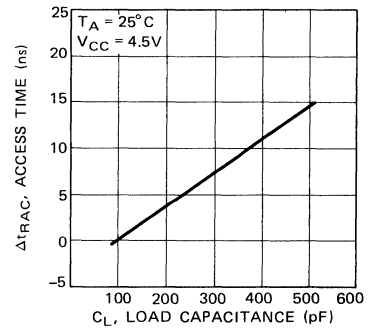


Fig. 20 – ACCESS TIME vs. LOAD CAPACITANCE



1

Fig. 21 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

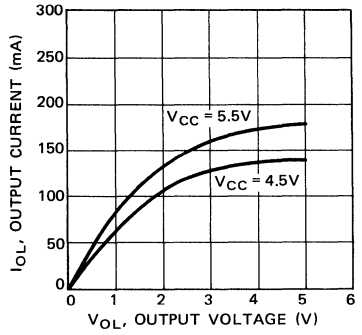


Fig. 22 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

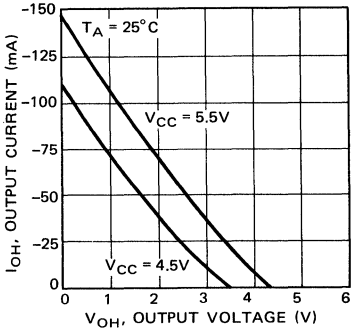


Fig. 23 – SUBSTRATE VOLTAGE DURING POWER UP

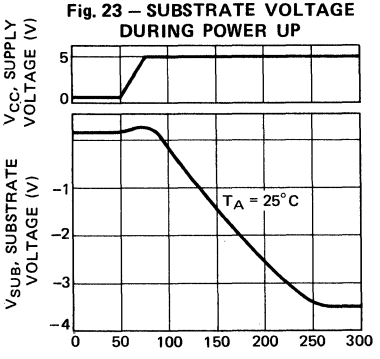
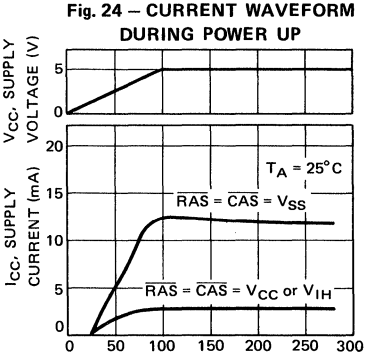


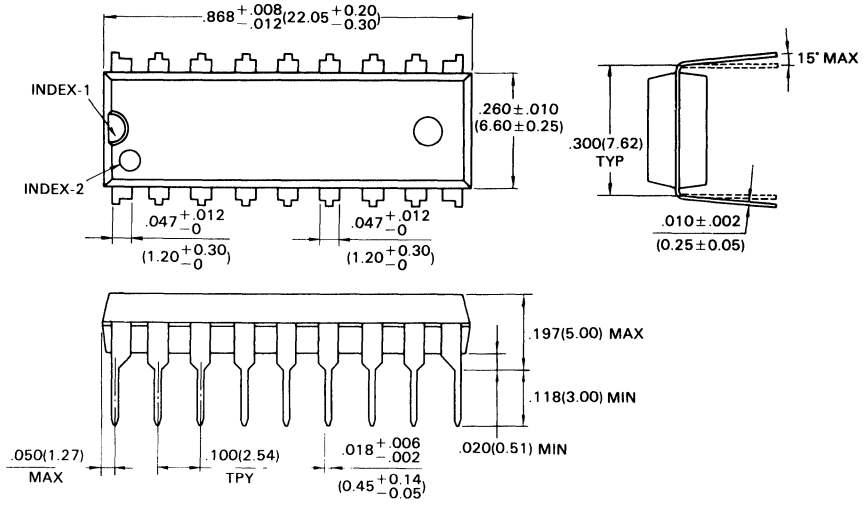
Fig. 24 – CURRENT WAVEFORM DURING POWER UP



PACKAGE DIMENSIONS

(Suffix: -P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M03)



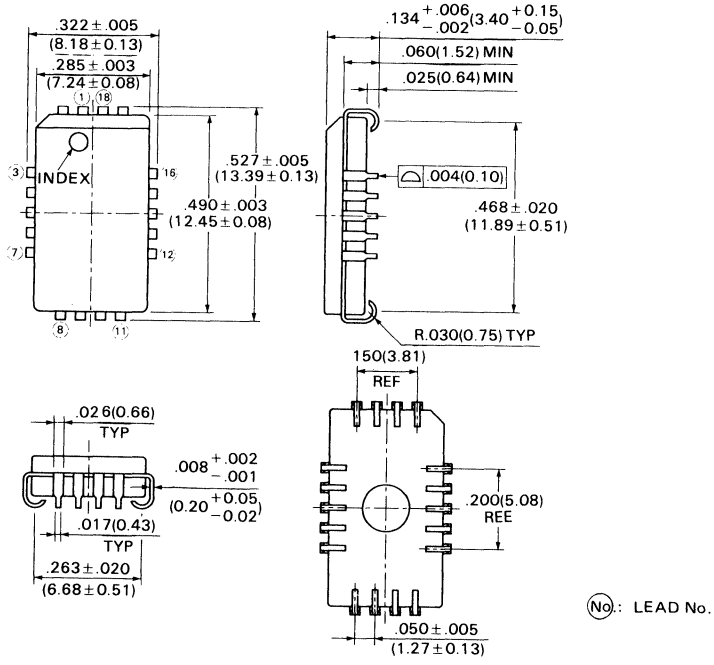
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS

(Suffix: -PD)

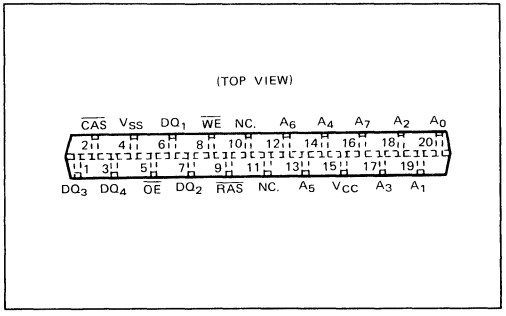
18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M04)



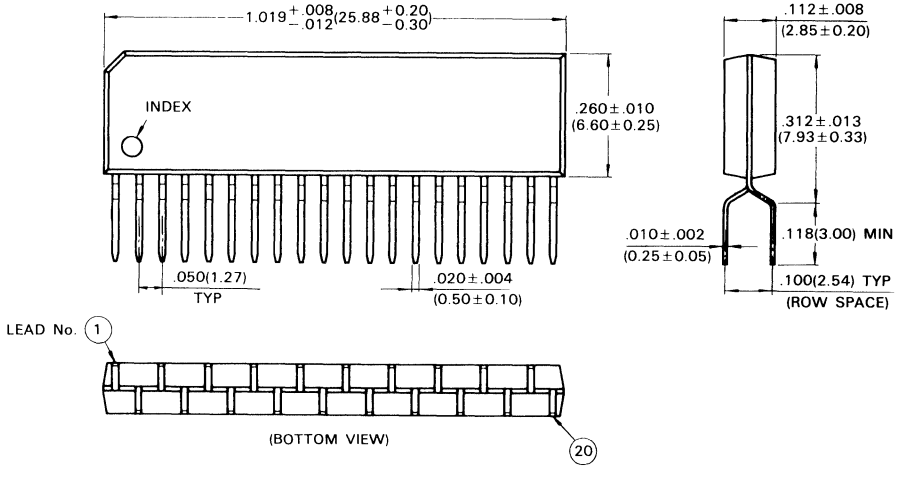
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PSZ)



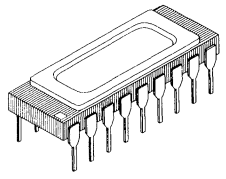
20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

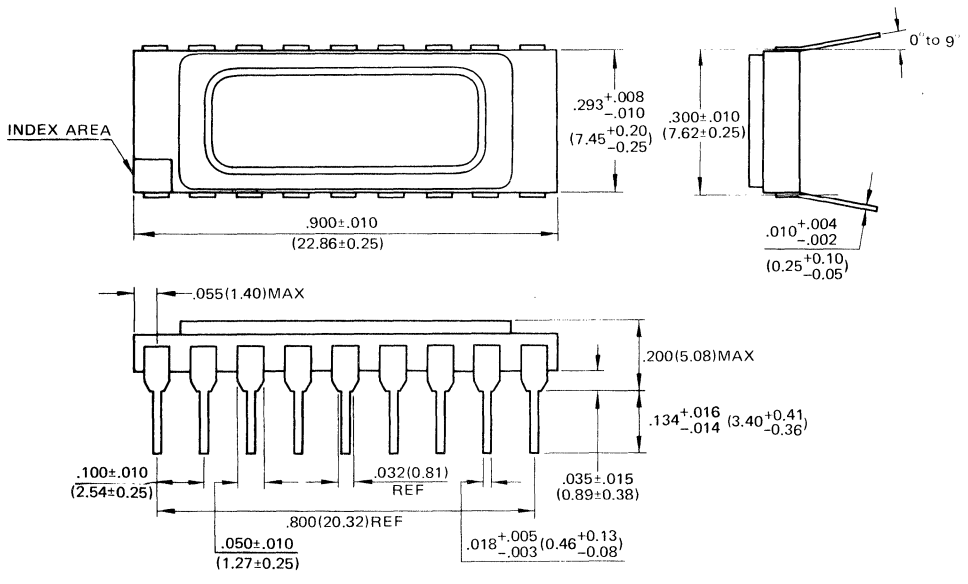
(Suffix: -C)



DIP-18C-A01

1

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



Dimensions in
inches (millimeters)

CMOS DRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
2-3	MB81C1000–70	70	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576 x 1)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
	–12	120		26-pin Plastic SOJ
2–25	MB81C1000-70L	70	1048576 bits	18-pin Plastic DIP
	-80L	80	(1048576 x 1)	18-pin Ceramic DIP
	-10L	100		20-pin Plastic ZIP
	-12L	120		26-pin Ceramic SOJ
2-47	MB81C1000A–60	60	1048576 bits	18-pin Plastic DIP
	–70	70	(1048576 x 1)	18-pin Ceramic DIP
	–80	80		20-pin Plastic ZIP
	–10	100		24-pin Plastic FPT
				26-pin Plastic SOJ
2–71	MB80C1000A-70L	70	1048576 bits	18-pin Plastic DIP
	-80L	80	(1048576 x 1)	18-pin Ceramic DIP
	-10L	100		20-pin Plastic ZIP
				24-pin Plastic FPT
				26-pin Plastic SOJ
2-95	MB81C1001–70	70	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576 x 1)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
	–12	120		26-pin Plastic SOJ
2–117	MB81C1001-70L	70	1048576 bits	18-pin Plastic DIP
	-80L	80	(1048576 x 1)	18-pin Ceramic DIP
	-10L	100		20-pin Plastic ZIP
	-12L	120		26-pin Plastic SOJ
2-139	MB81C1001A–60	60	1048576 bits	18-pin Plastic DIP
	–70	70	(1048576 x 1)	18-pin Ceramic DIP
	–80	80		20-pin Plastic ZIP
	–10	100		24-pin Plastic FPT
				26-pin Plastic SOJ
2–163	MB80C1001A-70L	70	1048576 bits	18-pin Plastic DIP
	-80L	80	(1048576 x 1)	18-pin Ceramic DIP
	-10L	100		20-pin Plastic ZIP
				24-pin Plastic FPT
				26-pin Plastic SOJ
2-187	MB81C4256–70	70	1048576 bits	20-pin Plastic DIP, ZIP
	–80	80	(262144 x 4)	20-pin Ceramic DIP
	–10	100		26-pin Plastic SOJ
	–12	120		
2–211	MB81C4256-70L	70	1048576 bits	20-pin Plastic DIP, ZIP
	-80L	80	(262144 x 4)	20-pin Ceramic DIP
	-10L	100		26-pin Plastic SOJ
	-12L	120		

CMOS DRAMs — *At a Glance* (Continued)

Page	Device	Maximum Access Time (ns)	Capacity	Package Options		
2-235	MB81C4256A-60	60	1048576 bits	20-pin	Plastic	DIP, ZIP
	-70	70	(262144 x 4)	20-pin	Ceramic	DIP
	-80	80		24-pin	Plastic	FPT
	-10	100		26-pin	Plastic	SOJ
2-261	MB81C4256A-70L	70	1048576 bits	20-pin	Plastic	DIP, ZIP
	-80L	80	(262144 x 4)	20-pin	Ceramic	DIP
	-10L	100		24-pin	Plastic	FPT
				26-pin	Plastic	SOJ
2-287	MB814100-80	80	4194304 bits	18-pin	Plastic	DIP
	-10	100	(4194304 x 1)	20-pin	Plastic	ZIP
	-12	120		26-pin	Plastic	SOJ
2-307	MB814100-80L	80	4194304 bits	18-pin	Plastic	DIP
	-10L	100	(4194304 x 1)	20-pin	Plastic	ZIP
	-12L	120		26-pin	Plastic	SOJ
2-309	MB814101-80	80	4194304 bits	18-pin	Plastic	DIP
	-10	100	(4194304 x 1)	20-pin	Plastic	ZIP
	-12	120		26-pin	Plastic	SOJ
2-329	MB814101-80L	80	4194304 bits	18-pin	Plastic	DIP
	-10L	100	(4194304 x 1)	20-pin	Plastic	ZIP
	-12L	120		26-pin	Plastic	SOJ
2-331	MB814400-80	80	4194304 bits	20-pin	Plastic	DIP, ZIP
	-10	100	(1048576 x 4)	26-pin	Plastic	SOJ
	-12	120				
2-353	MB814400-80L	80	4194304 bits	20-pin	Plastic	DIP, ZIP
	-10L	100	(1048576 x 4)	26-pin	Plastic	SOJ
	-12L	120				

January 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C1000-70/-80/-10/-12

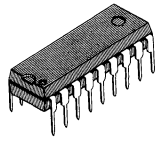
CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Fast Page Mode DRAM

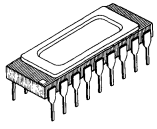
The Fujitsu MB81C1000 is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000 has been designed for mainframe memories, buffer memories, and peripheral storage applications requiring high speed, low power dissipation, or compact layout.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1000 high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

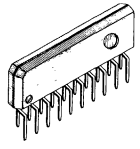


DIP–18P–M04



DIP–18C–A01

LCC–26P–M04



ZIP–20P–M02

Features

Parameter	MB81C1000 -70	MB81C1000 -80	MB81C1000 -10	MB81C1000 -12
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Fast Page Mode Cycle Time	53 ns min.	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	413 mW max.	385 mW max.	330 mW max.	275 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

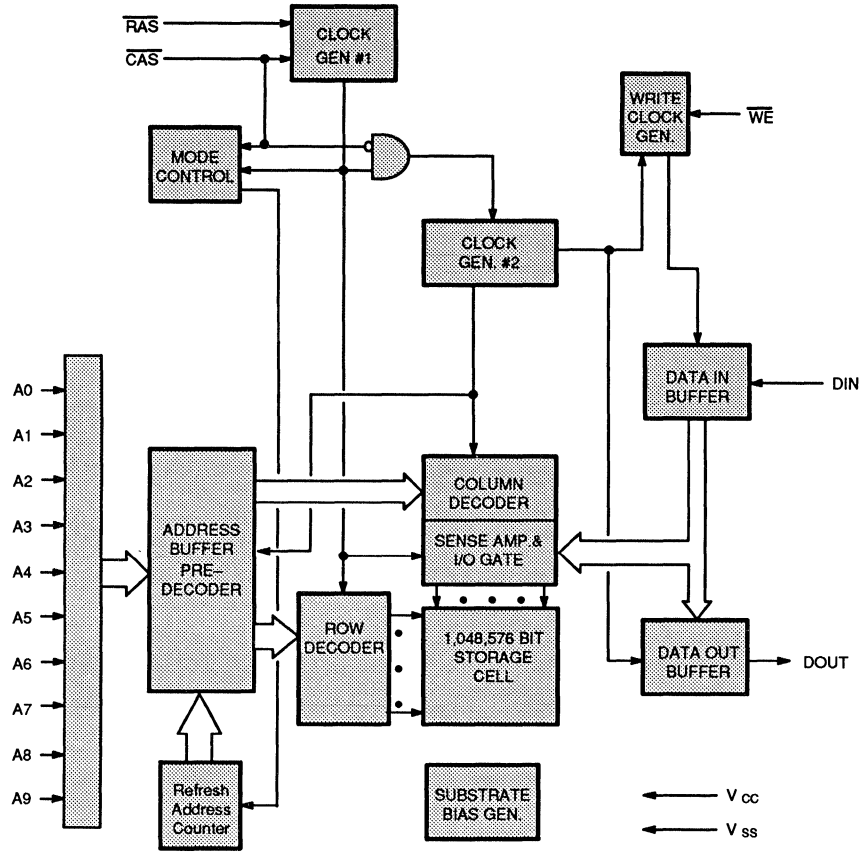
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 — MB81C1000 DYNAMIC RAM—BLOCK DIAGRAM

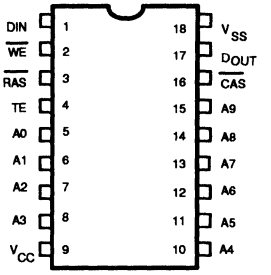


CAPACITANCE (T_A = 25°C, f = 1MHz)

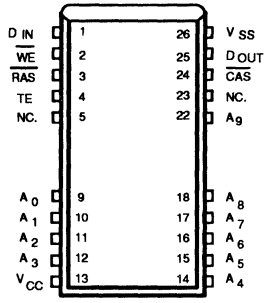
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

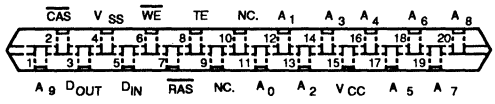
18-Pin DIP:
(TOP VIEW)



26-Pin SOJ:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Data is written into the MB81C1000 during write or read–modify–write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current)	MB81C1000–70	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C1000–80					70	
	MB81C1000–10					60	
	MB81C1000–12					50	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			1.0	
Refresh current #1 (Average power supply current)	MB81C1000–70	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	70	mA
	MB81C1000–80					65	
	MB81C1000–10					55	
	MB81C1000–12					45	
Fast Page Mode current	MB81C1000–70	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	47	mA
	MB81C1000–80					45	
	MB81C1000–10					40	
	MB81C1000–12					33	
Refresh current #2 (Average power supply current)	MB81C1000–70	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C1000–80					65	
	MB81C1000–10					55	
	MB81C1000–12					45	

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000-70		MB81C1000-80		MB81C1000-10		MB81C1000-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	167	—	182	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	25	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	75	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	25	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000-70		MB81C1000-80		MB81C1000-10		MB81C1000-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	70	—	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	25	—	25	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	43	—	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	53	—	55	—	60	—	70	—	ns
51	Fast Page Mode Read–Modify–Write Cycle Time		t_{PRWC}	75	—	77	—	85	—	100	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	53	—	55	—	60	—	70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200μs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

2

Fig. 2 – t_{RAC} vs. t_{RCD}

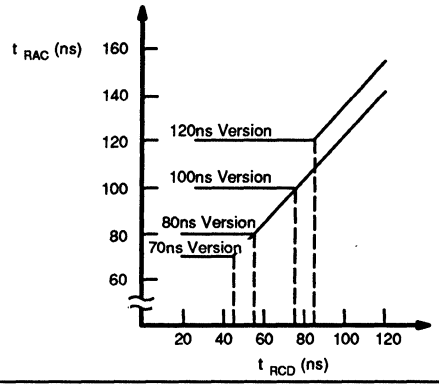
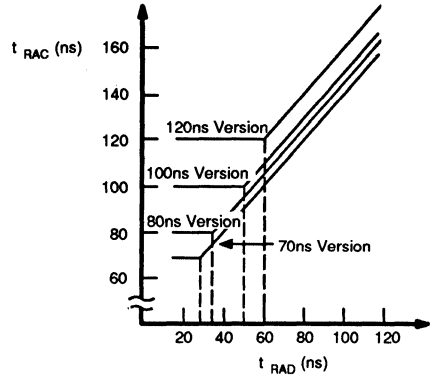


Fig. 3 – t_{RAC} vs. t_{RAD}



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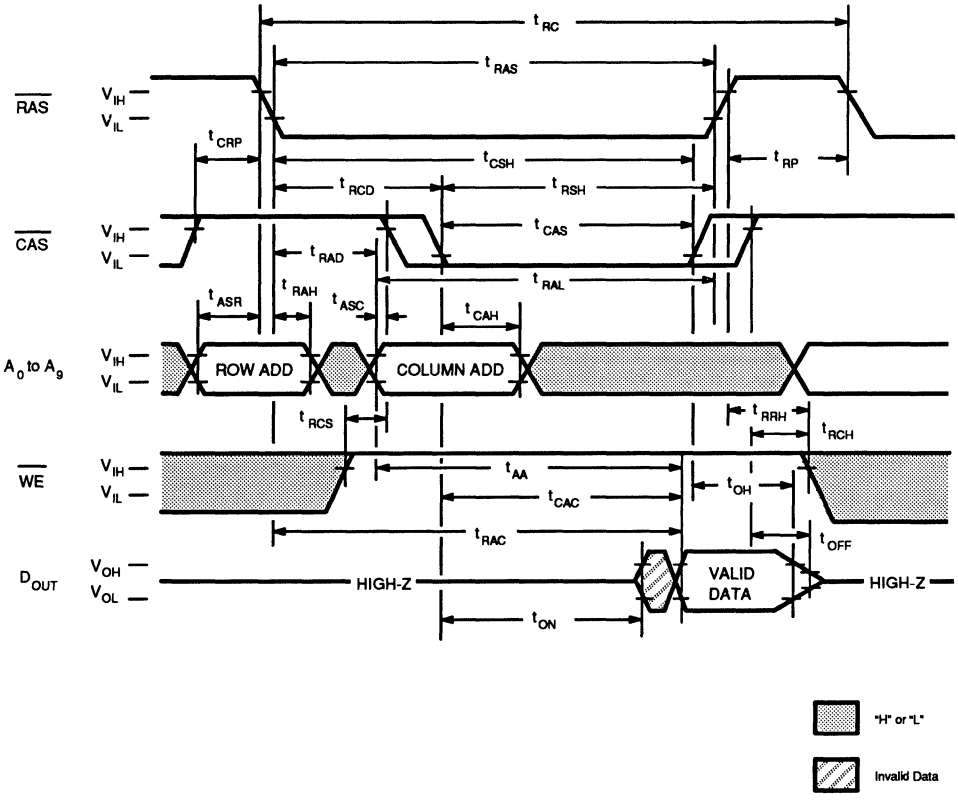
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Fast Page Mode.

Fig. 4 – READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

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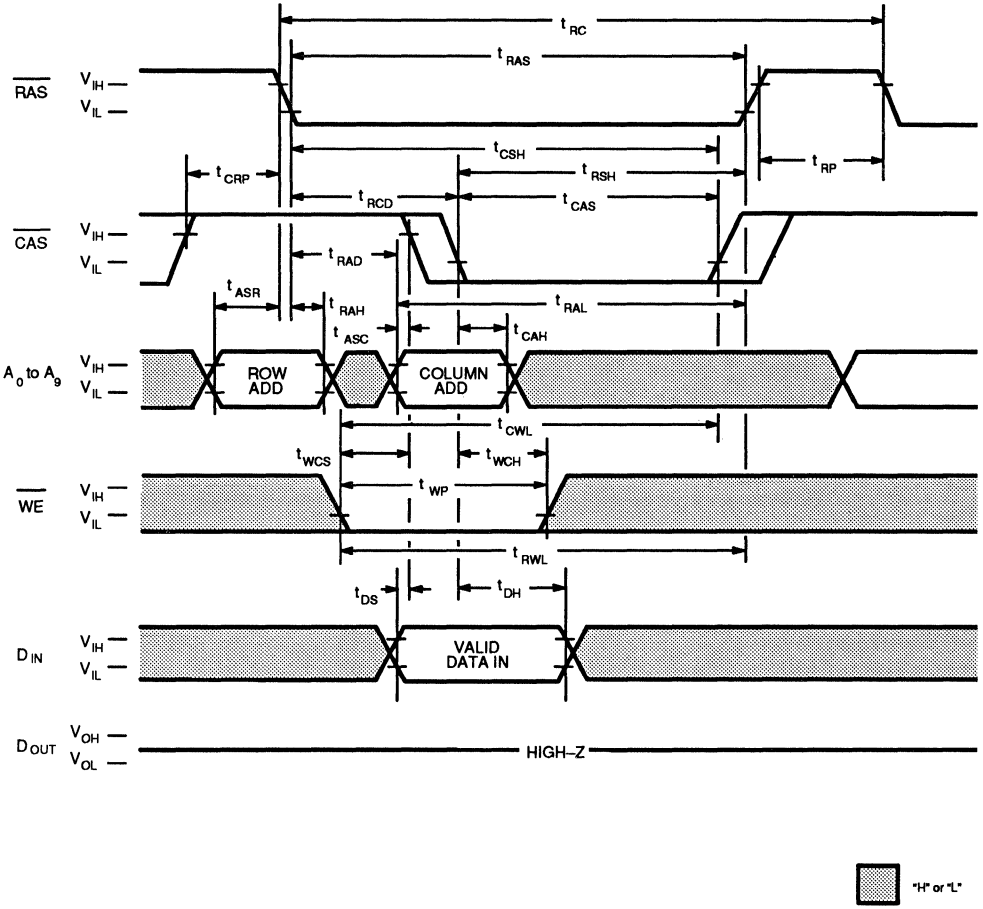
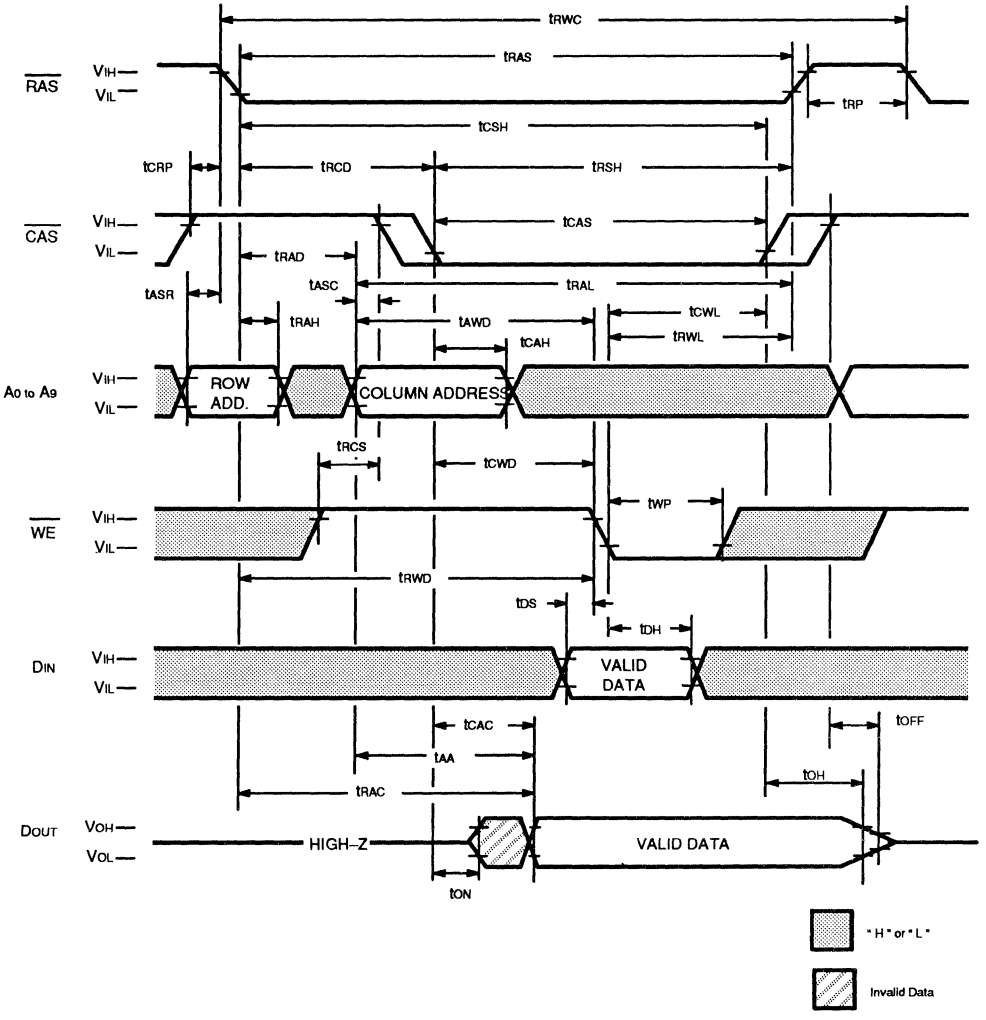
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin islatched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

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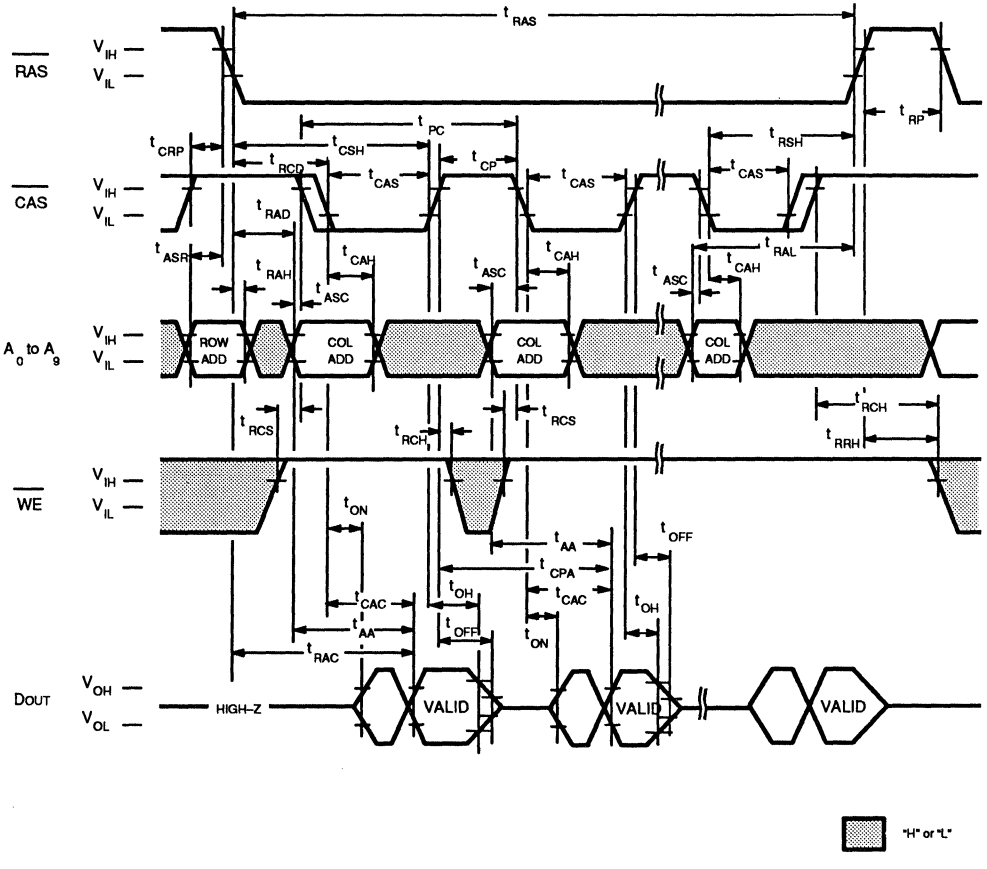
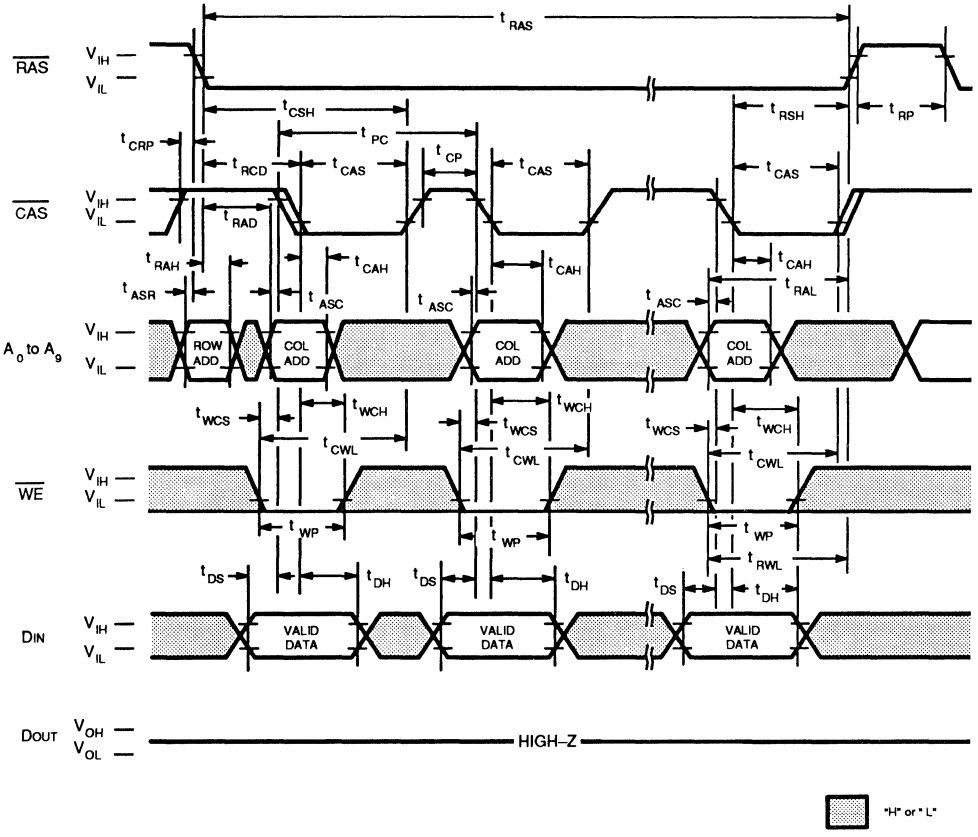
Fig. 7 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later.
Any of the 1024 bits belonging to each row can be accessed.

Fig. 8 – FAST PAGE MODE WRITE CYCLE (Early Write)



DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 1024 bits belonging to each row can be accessed.

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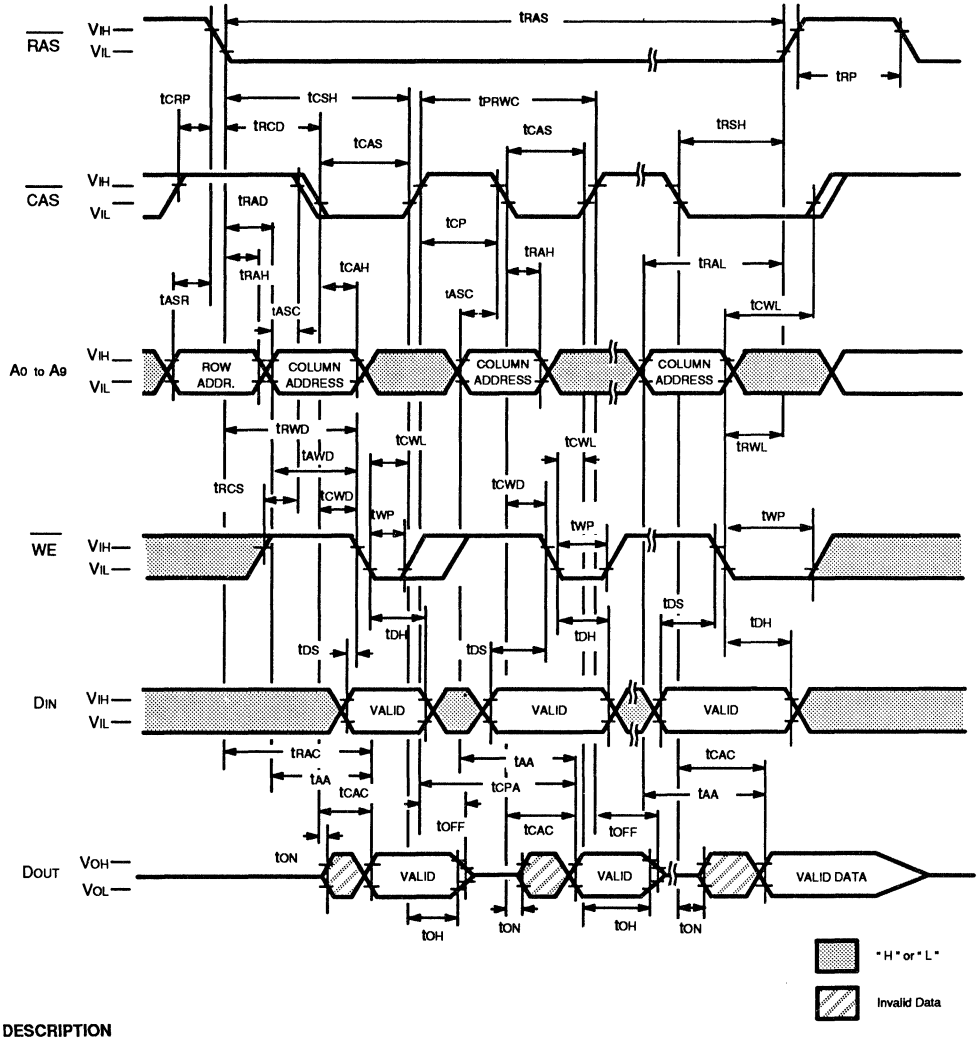
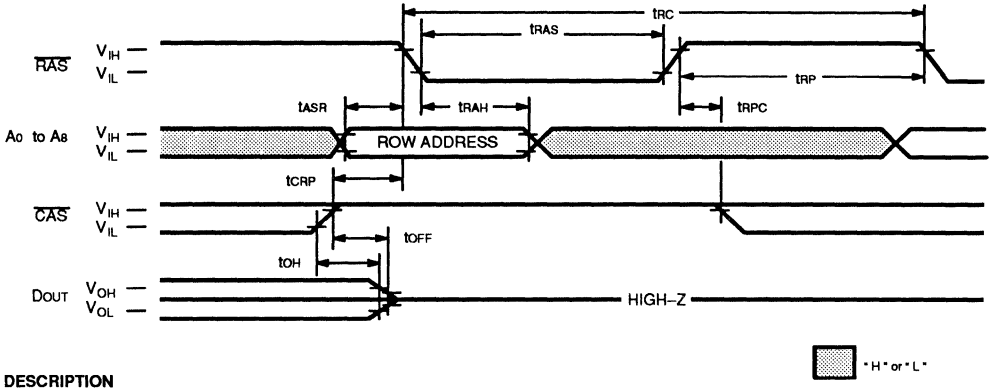
Fig. 9 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode, the read–modify–write cycle can be executed by changing $\overline{WE}$ high to low after the data appearsat DOUT pin as well as normal cycle. Any of the 1024 bits belonging to each row can be accessed.

Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

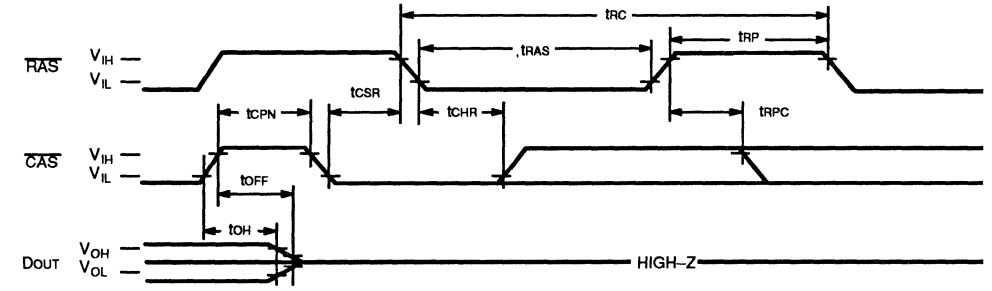


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

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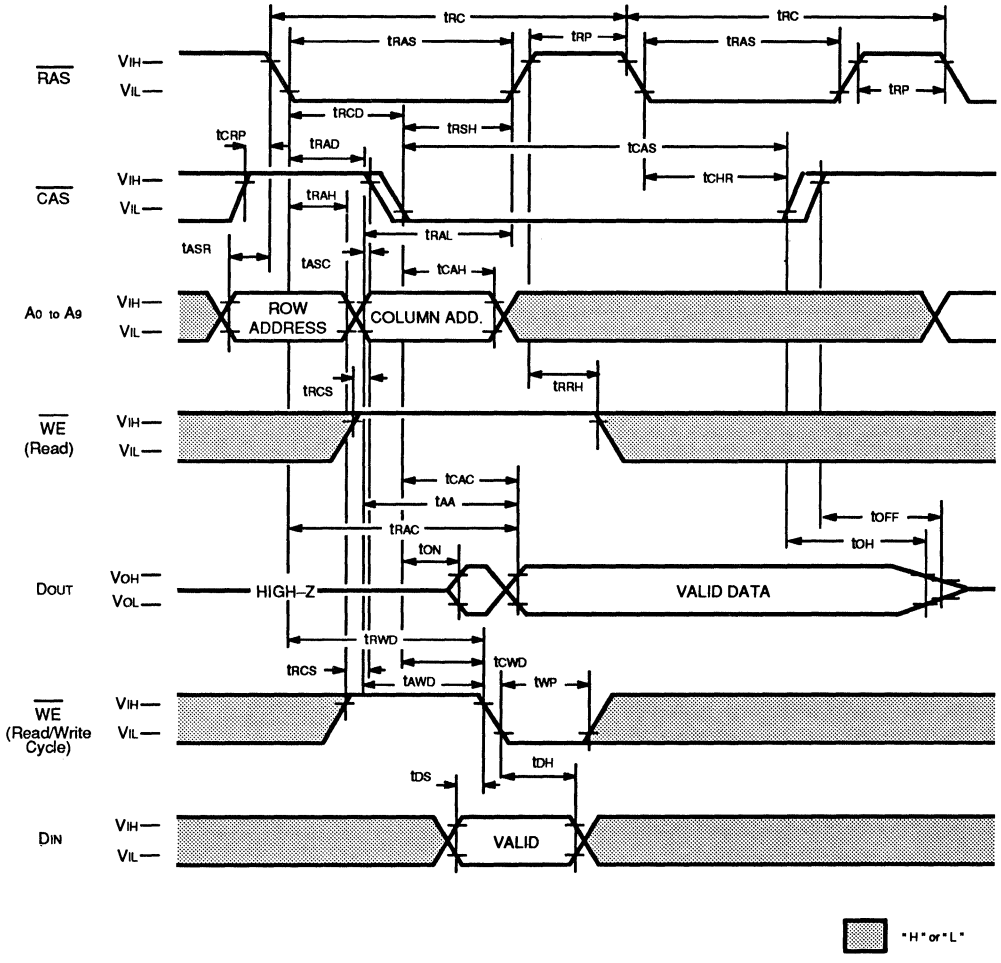
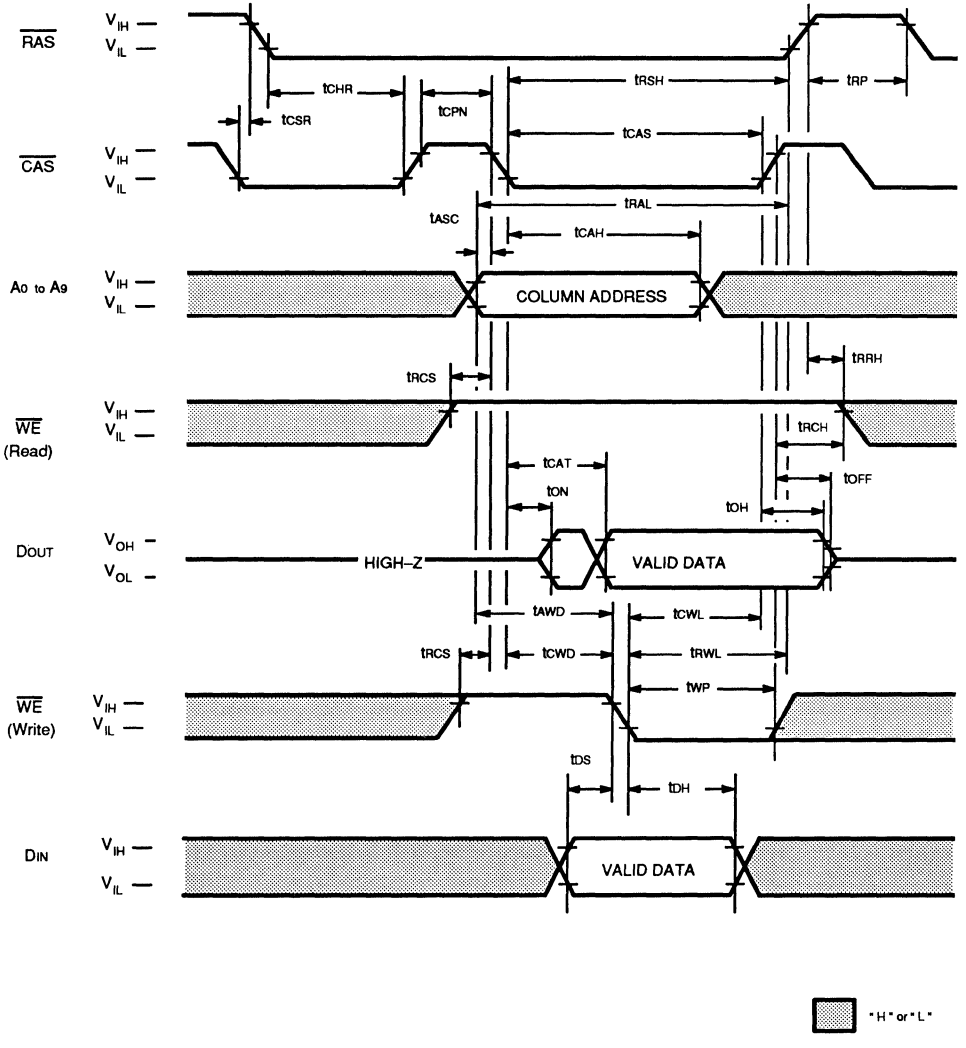
Fig. 13 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

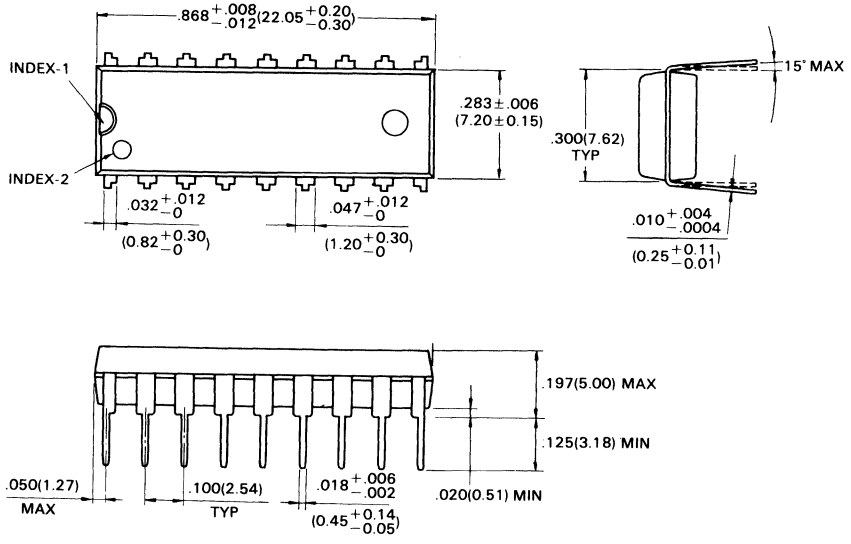


PACKAGE DIMENSIONS

(Suffix: –P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)

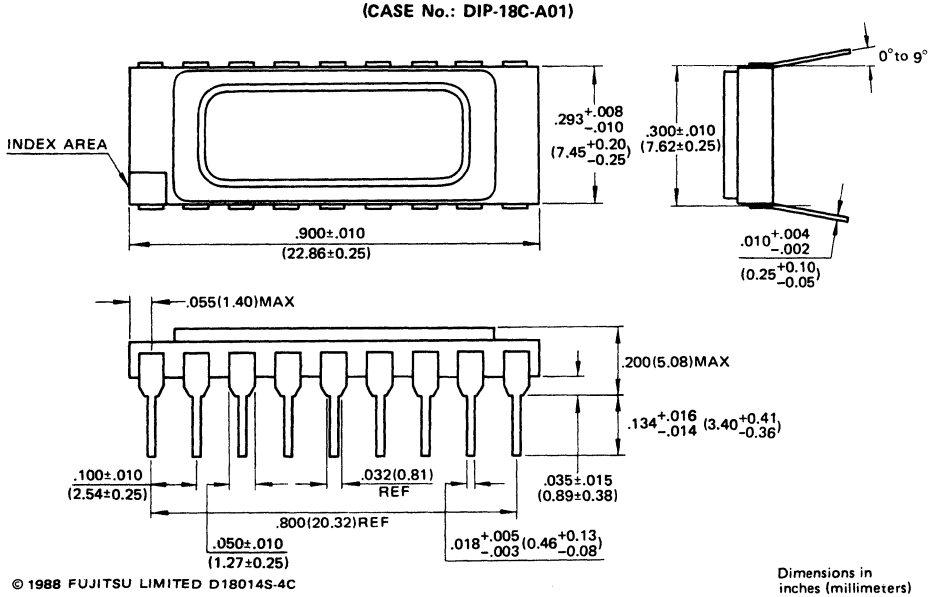


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



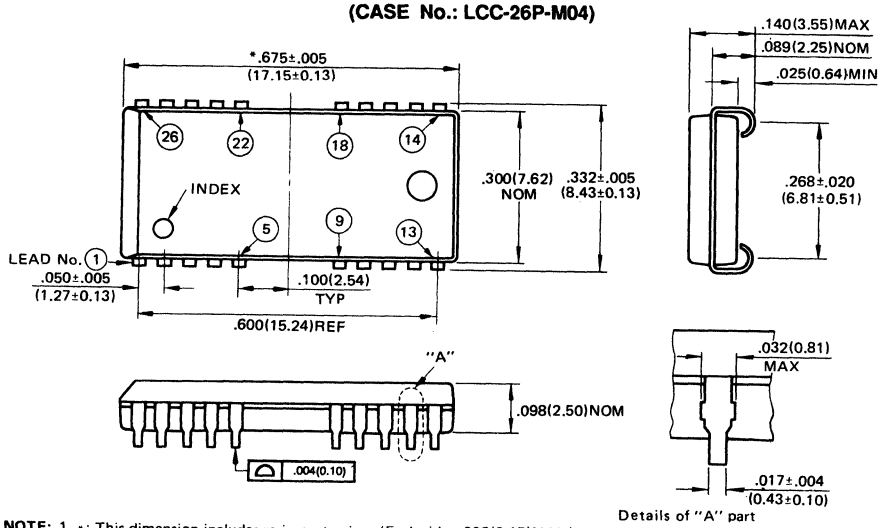
Dimensions in inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

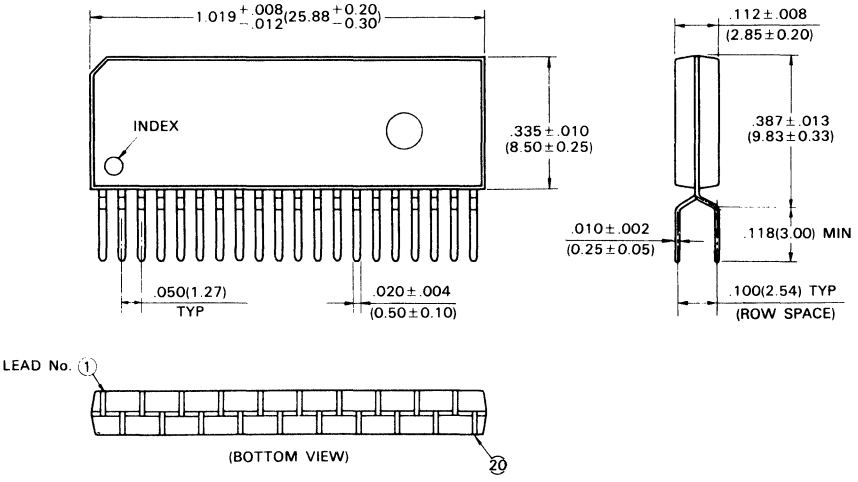
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

2

February 1990
Edition 1.0

FUJITSU

DATA SHEET

MB81C1000-70L/-80L/-10L/-12L

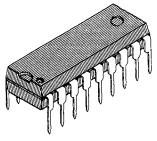
CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Fast Page Mode DRAM

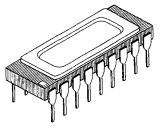
The Fujitsu MB81C1000 is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000 has been designed for mainframe memories, buffer memories, peripheral storage and memory systems of battery operated computers requiring very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1000 high α-ray soft error immunity and extended refresh time. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

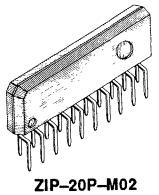


DIP-18P-M04



DIP-18C-A01

LCC-26P-M04



ZIP-20P-M02

2

Features

Parameter	MB81C1000 -70L	MB81C1000 -80L	MB81C1000 -10L	MB81C1000 -12L
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Fast Page Mode Cycle Time	53 ns min.	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	396 mW max.	358 mW max.	303 mW max.	259 mW max.
• Standby Current	8.3 mW max. (TTL level)/1.4 mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 64 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

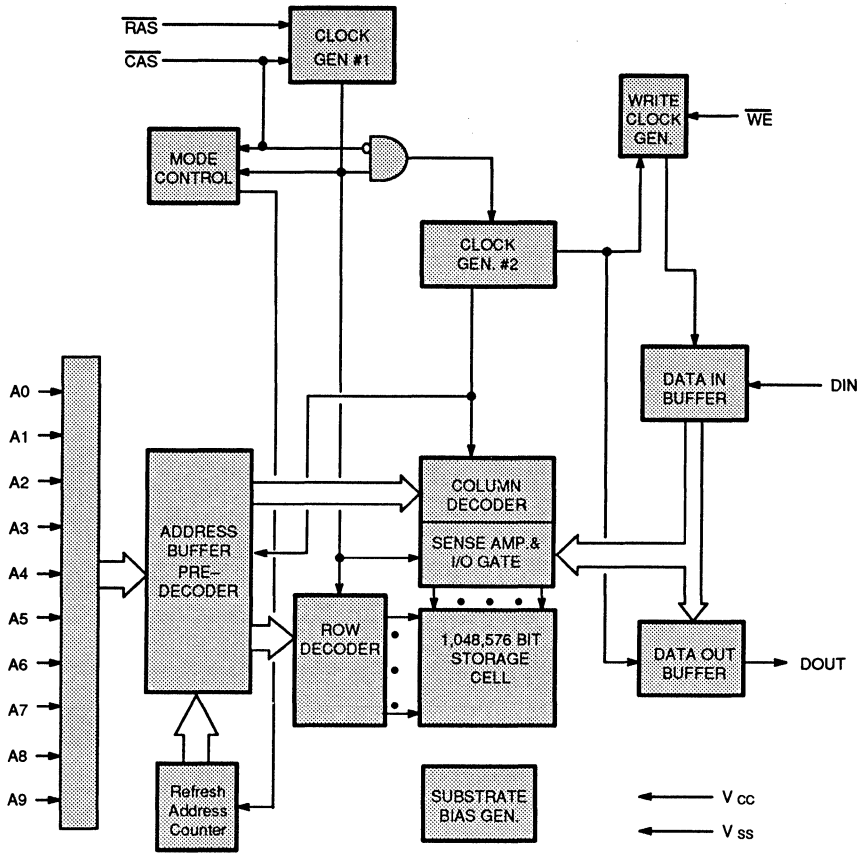
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 — MB81C1000 DYNAMIC RAM—BLOCK DIAGRAM

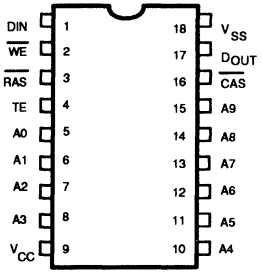


CAPACITANCE (T_A = 25°C, f = 1MHz)

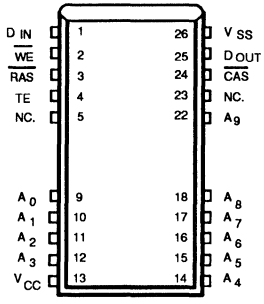
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

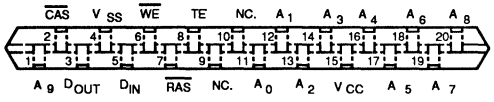
18–Pin DIP:
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Data is written into the MB81C1000 during write or read–modify–write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current) [2]	MB81C1000–70L	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	72	mA
	MB81C1000–80L					65	
	MB81C1000–10L					55	
	MB81C1000–12L					47	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	1.5	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			250	µA
Refresh current #1 (Average power supply current) [2]	MB81C1000–70L	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	60	mA
	MB81C1000–80L					56	
	MB81C1000–10L					50	
	MB81C1000–12L					45	
Fast Page Mode current [2]	MB81C1000–70L	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	39	mA
	MB81C1000–80L					37	
	MB81C1000–10L					33	
	MB81C1000–12L					28	
Refresh current #2 (Average power supply current) [2]	MB81C1000–70L	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	60	mA
	MB81C1000–80L					56	
	MB81C1000–10L					50	
	MB81C1000–12L					45	
Battery Back up current (Average power supply current)	MB81C1000–70L	ICC_6	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} =125 µs, t_{RAS} =min. to 1 µs, D_{OUT} =open. Other pin ≥ Vcc–0.2V or ≤ 0.2V	—	—	250	µA
	MB81C1000–80L						
	MB81C1000–10L						
	MB81C1000–12L						

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000–70L		MB81C1000–80L		MB81C1000–10L		MB81C1000–12L		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	64	—	64	—	64	—	64	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	167	—	182	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	25	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	75	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	25	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000–70L		MB81C1000–80L		MB81C1000–10L		MB81C1000–12L		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	70	—	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	25	—	25	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	43	—	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	53	—	55	—	60	—	70	—	ns
51	Fast Page Mode Read–Modify–Write Cycle Time		t_{PRWC}	75	—	77	—	85	—	100	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	53	—	55	—	60	—	70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	15	—	ns

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Notes:

1. Referenced to VSS
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a *minimum* of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation wit10.t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.hin the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, $t_{,RWD}$ and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

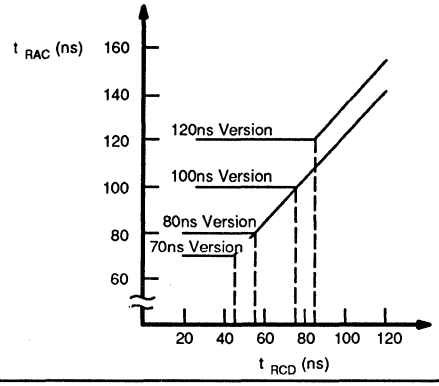
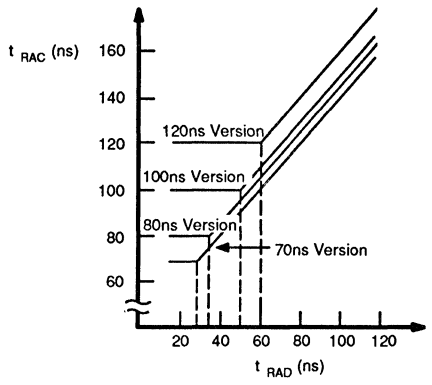


Fig. 3 – t_{RAC} vs. t_{RAD}



2

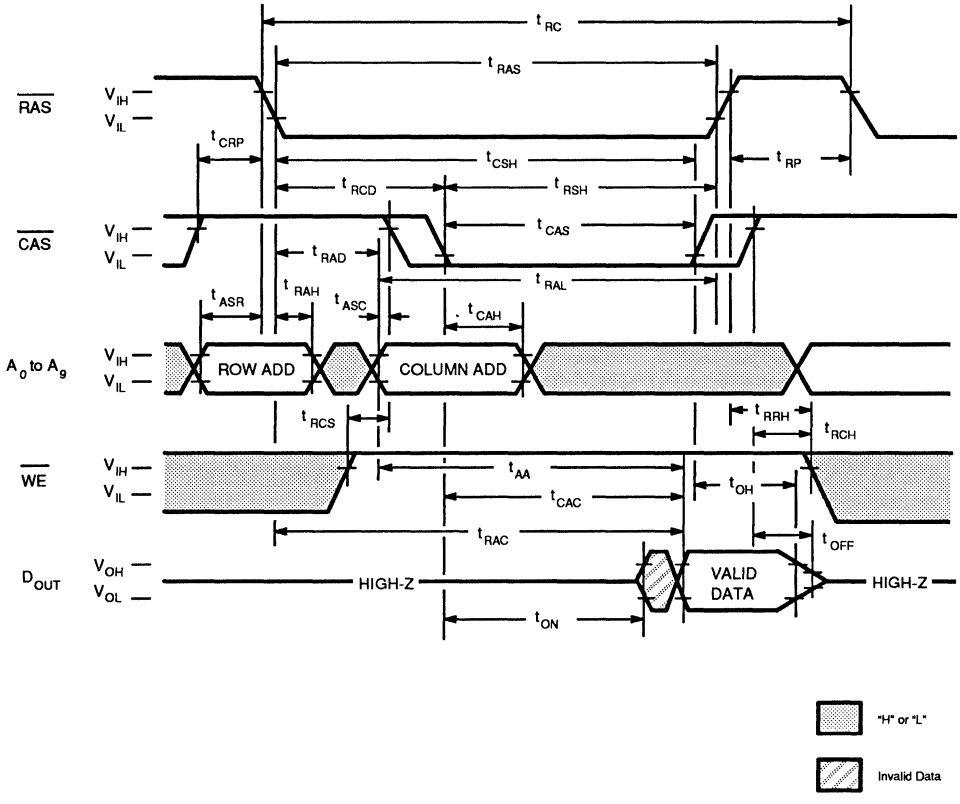
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Fast Page Mode.

Fig. 4 – READ CYCLE

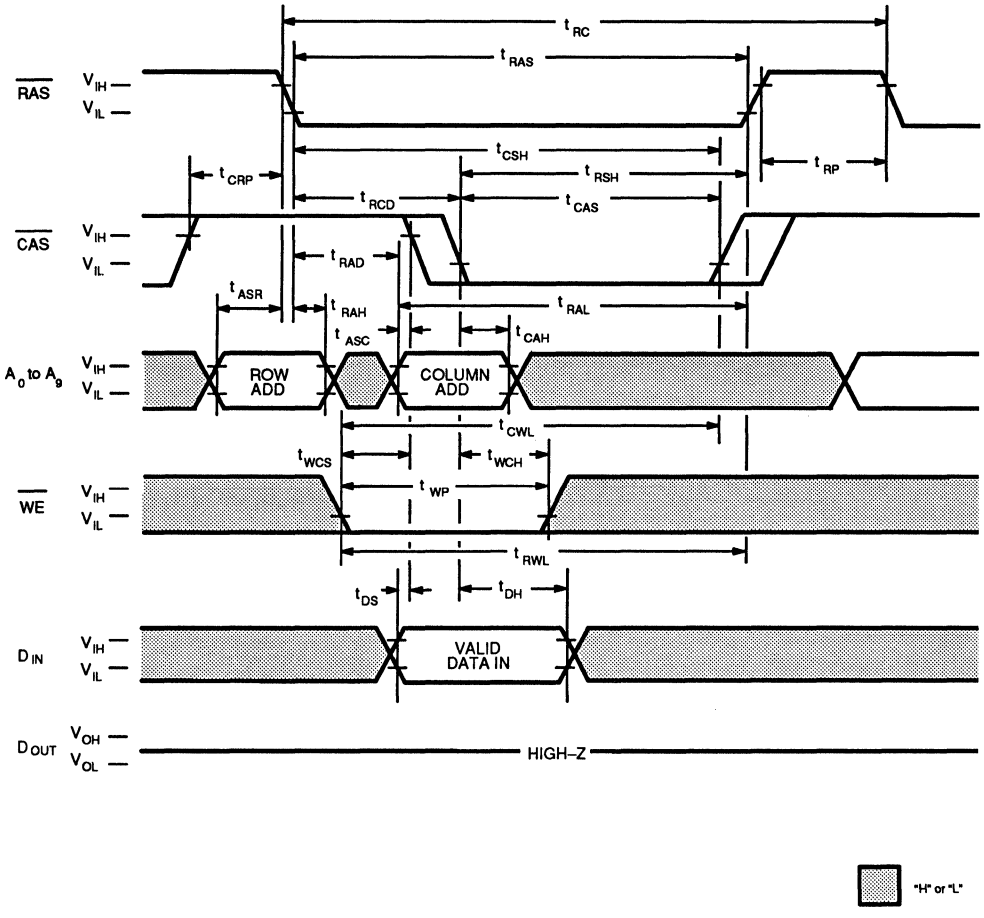


DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H" , the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

2

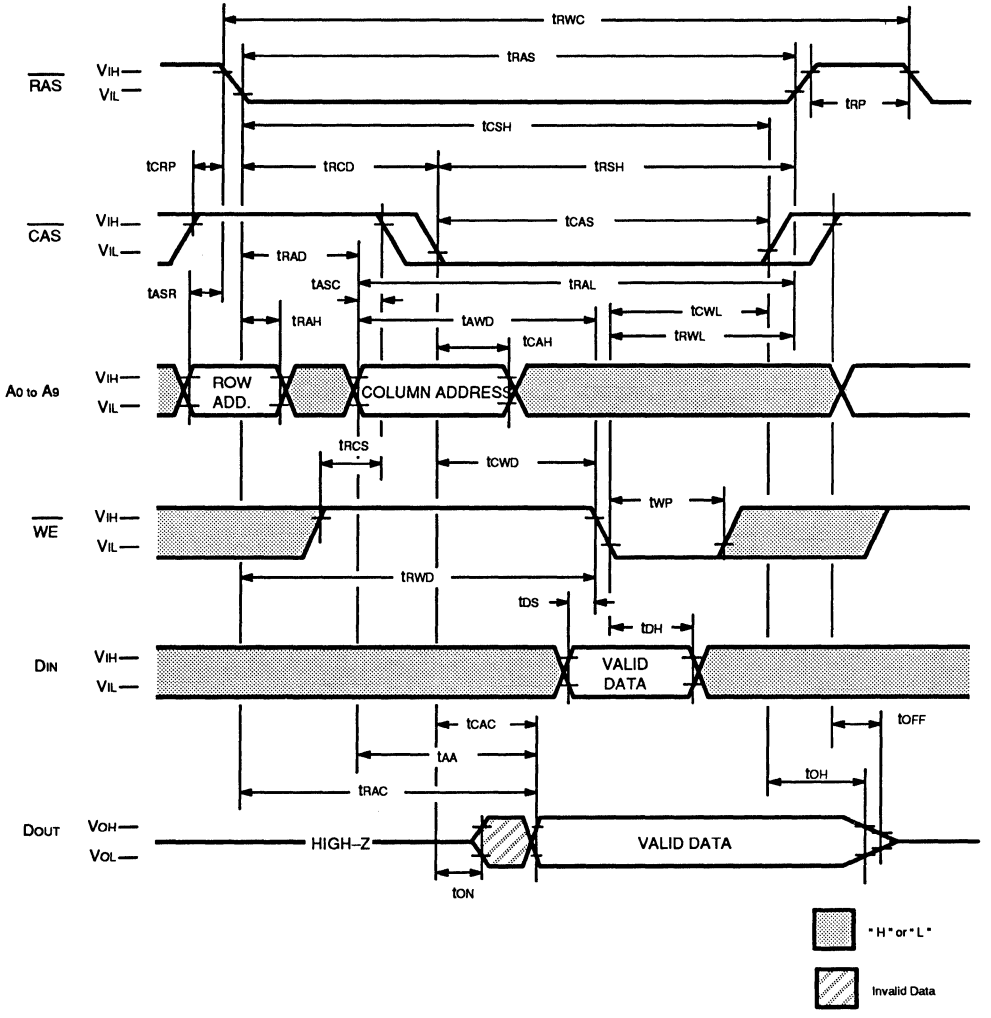
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE

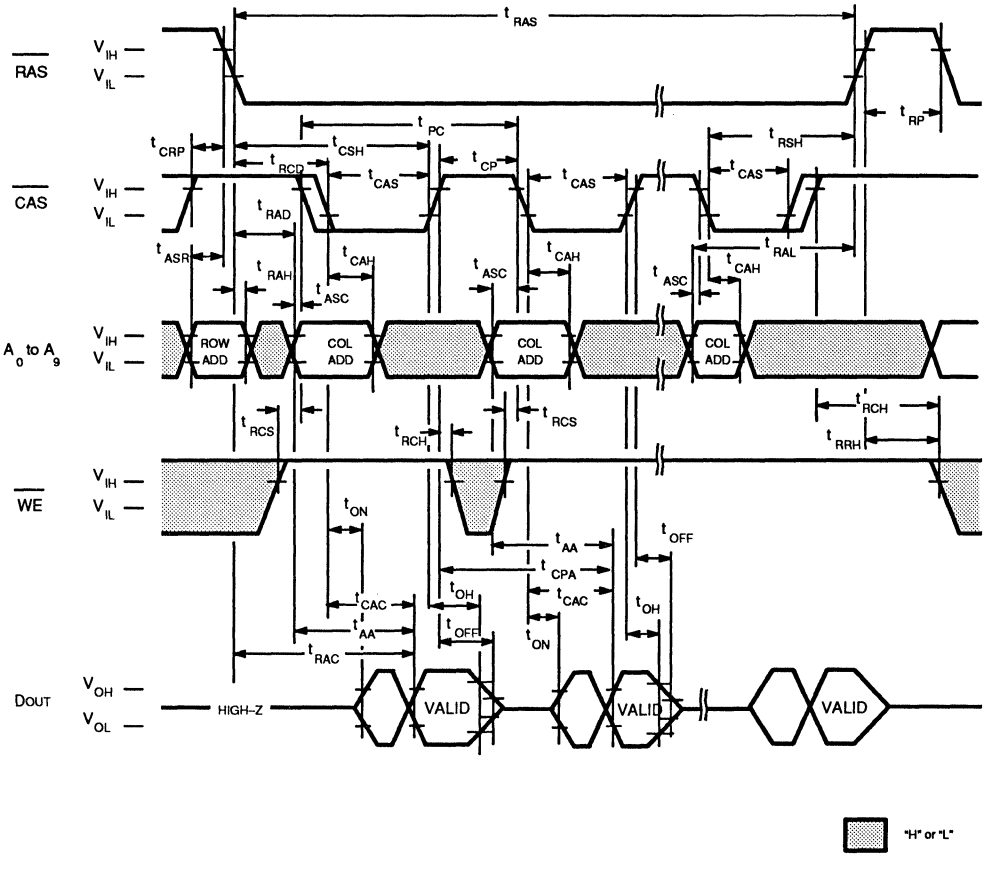


DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

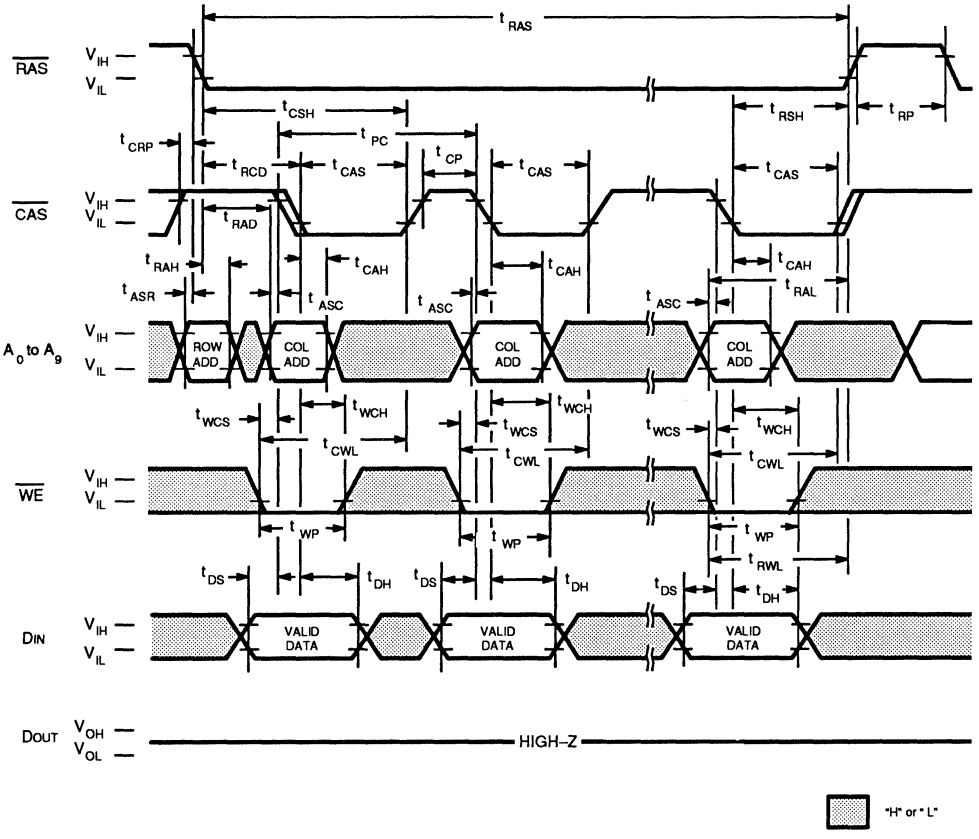
Fig. 7 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later.
Any of the 1024 bits belonging to each row can be accessed.

Fig. 8 – FAST PAGE MODE WRITE CYCLE (Early Write)

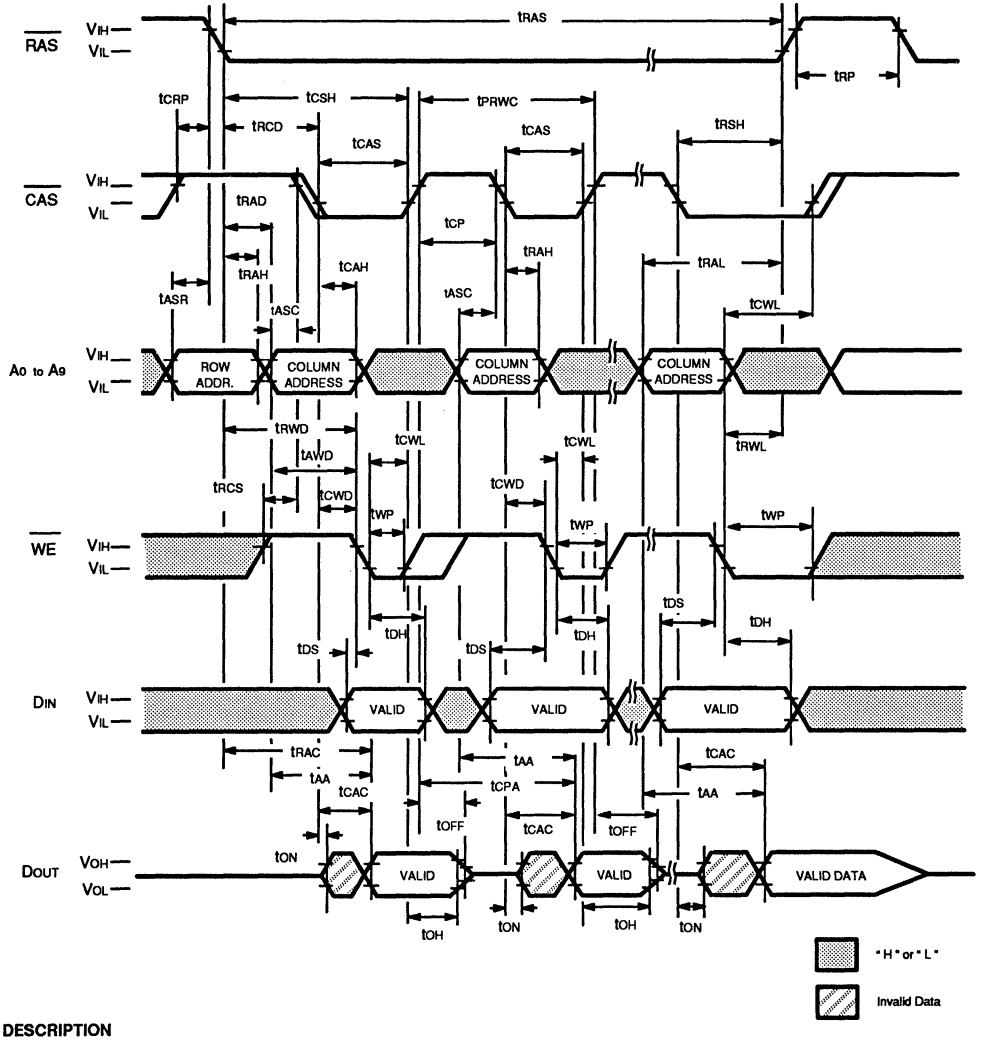


DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 1024 bits belonging to each row can be accessed.

2

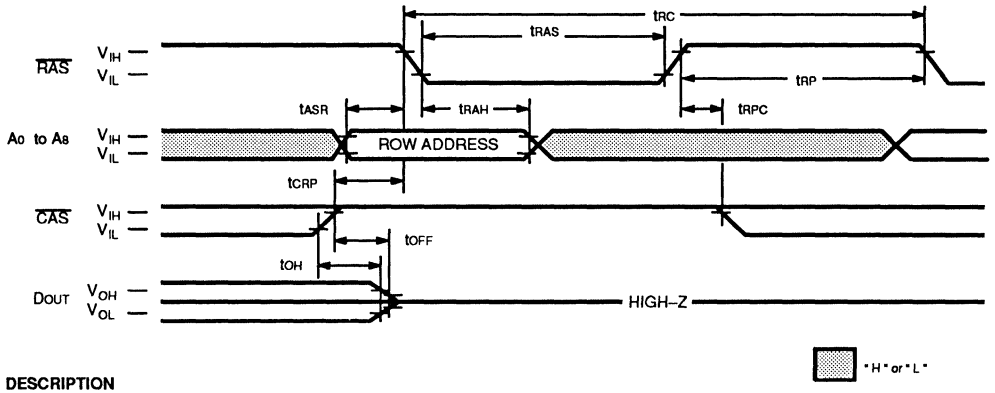
Fig. 9 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode, the read–modify–write cycle can be executed by changing $\overline{WE}$ high to low after the data appearsat DOUT pin as well as normal cycle. Any of the 1024 bits belonging to each row can be accessed.

Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

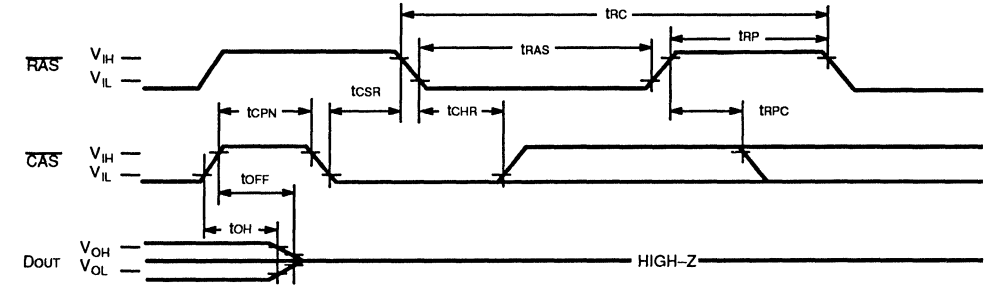


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 64–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "

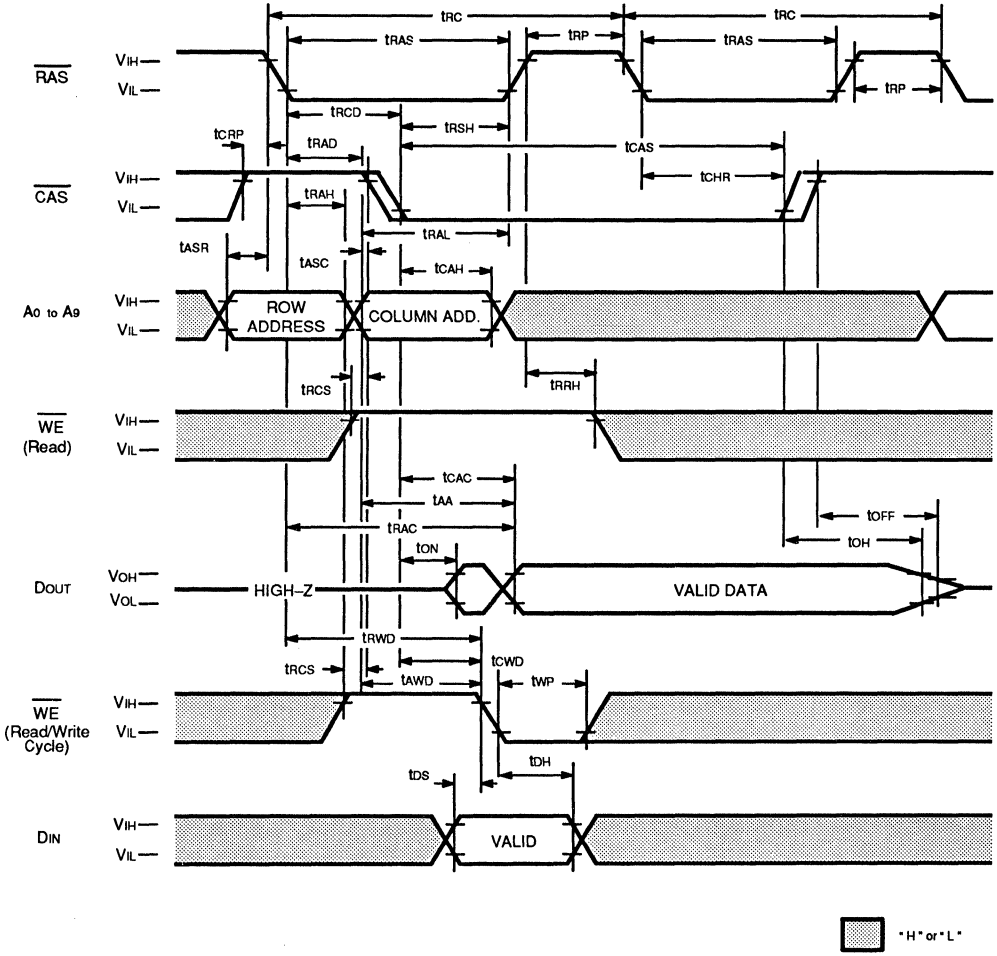


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

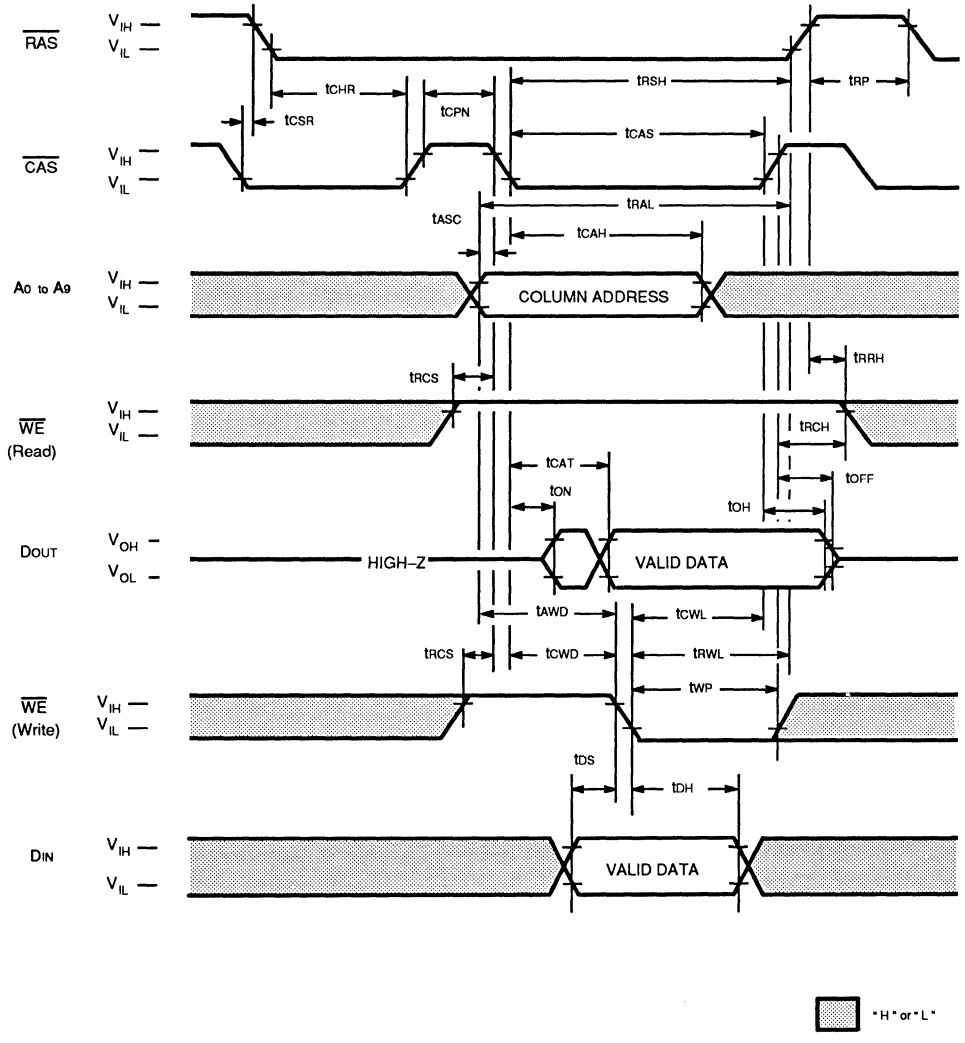
Fig. 13 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

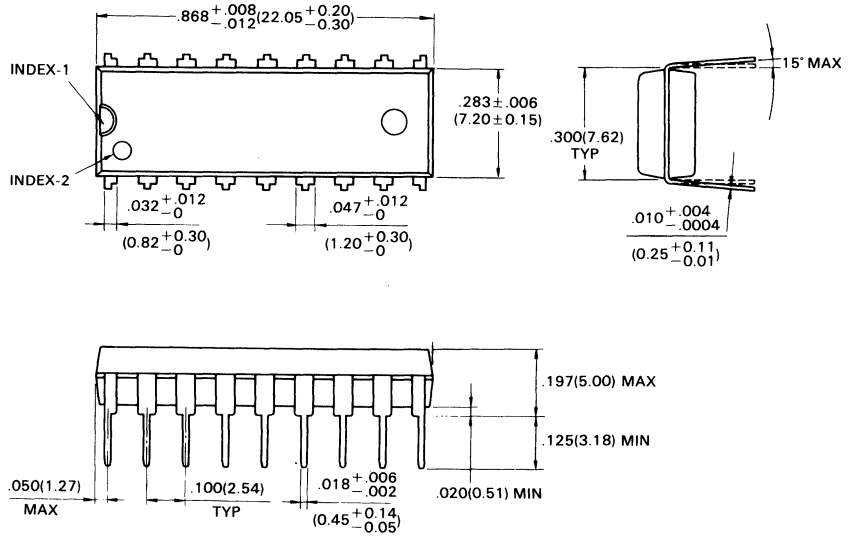


PACKAGE DIMENSIONS

(Suffix: -P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)



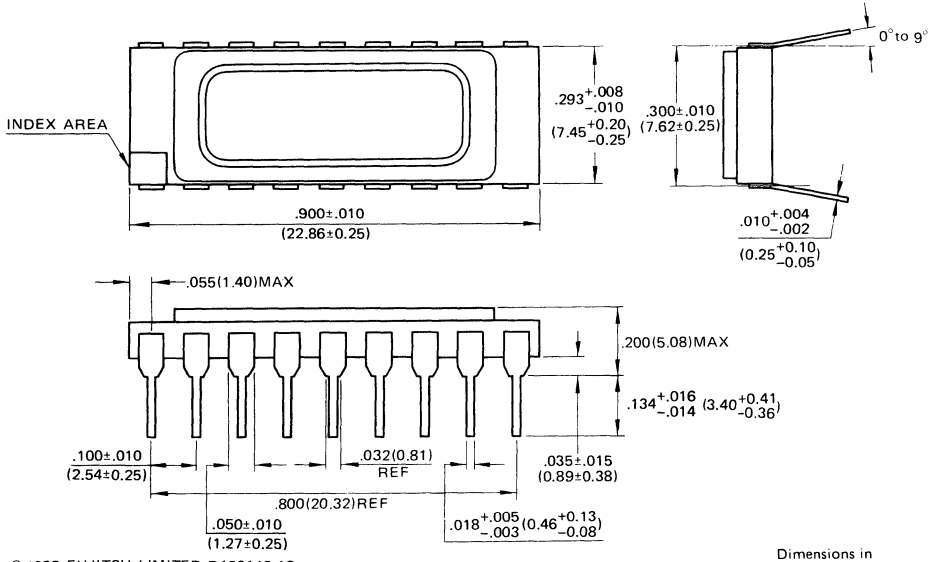
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



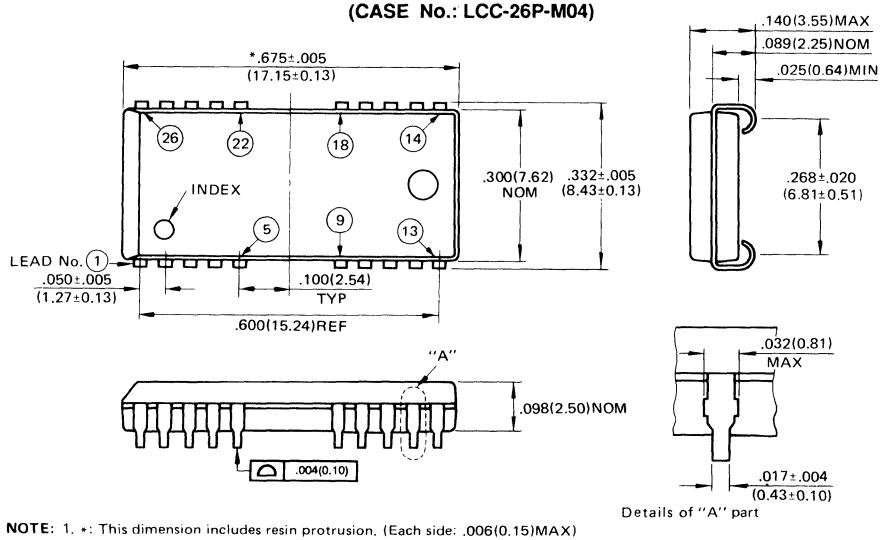
Dimensions in inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

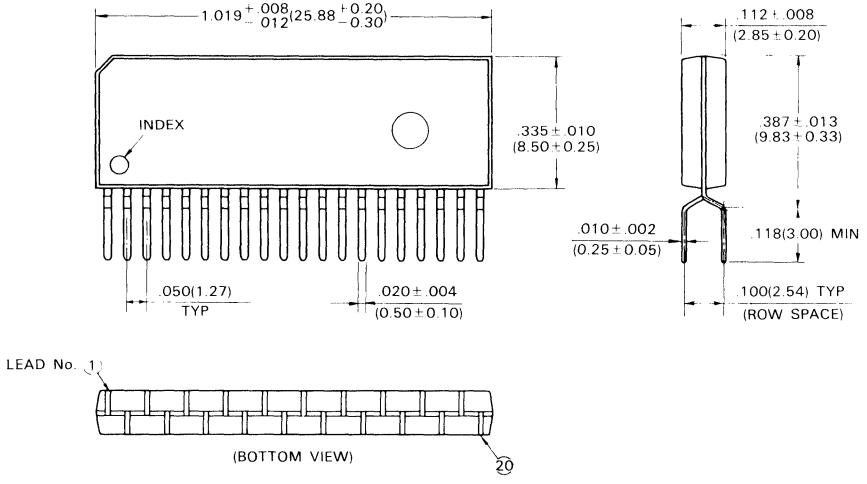
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

2

2

November 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C1000A-60/-70/-80/-10

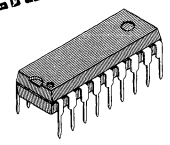
CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Fast Page Mode DRAM

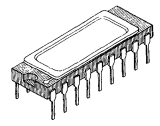
The Fujitsu MB81C1000A is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000A has been designed for mainframe memories, buffer memories, and peripheral storage applications requiring high speed, low power dissipation, or compact layout.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1000A high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

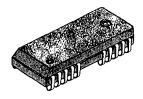
PRELIMINARY



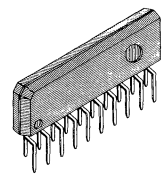
DIP–18P–M04



DIP–18C–A02



LCC–26P–M04



ZIP–20P–M02

*FPT–24P–M04 / *FPT–24P–M05
*: Available for 70/80/100ns versions

Features

Parameter	MB81C1000A -60	MB81C1000A -70	MB81C1000A -80	MB81C1000A -10
$\overline{RAS}$ Access Time	60 ns max.	70 ns max.	80 ns max.	100 ns max.
Random Cycle Time	130 ns min.	140 ns min.	155 ns min.	180 ns min.
Address Access Time	30 ns max.	35 ns max.	40 ns max.	50 ns max.
$\overline{CAS}$ Access Time	15 ns max.	20 ns max.	20 ns max.	25 ns max.
Fast Page Mode Cycle Time	45 ns min.	50 ns min.	55 ns min.	65 ns min.
Low Power Dissipation • Operating Current	407 mW max.	374 mW max.	341 mW max.	297 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

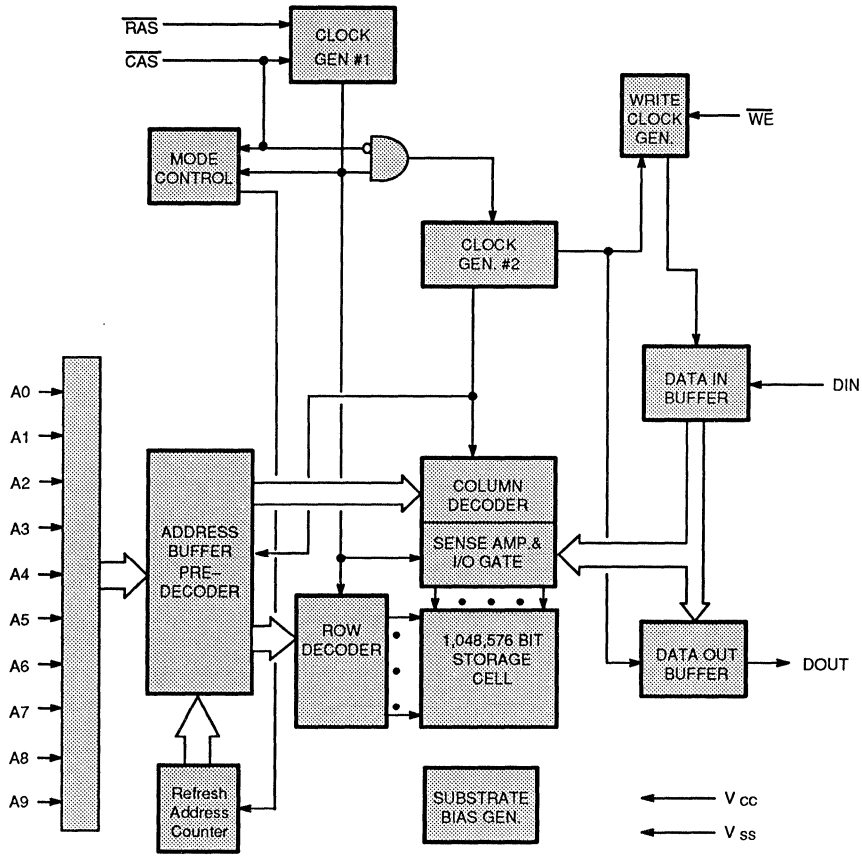
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 — MB81C1000A DYNAMIC RAM—BLOCK DIAGRAM

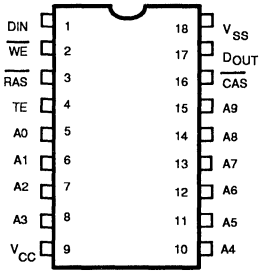


CAPACITANCE (T_A = 25°C, f = 1MHz)

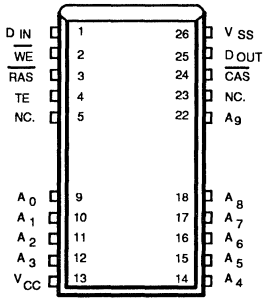
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

18–Pin DIP:
(TOP VIEW)

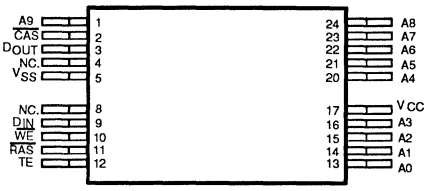


26–Pin SOJ:
(TOP VIEW)

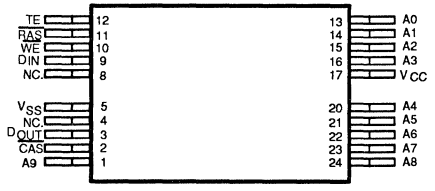


24–Pin FPT :
(TOP VIEW)

<Normal Bend : FPT–24P–M04>

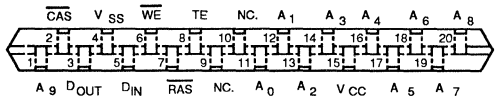


<Reverse Bend : FPT–24P–M05>



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
$\overline{TE}$	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

20–Pin ZIP:
(TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Data is written into the MB81C1000A during write or read–modify–write cycle. The inputdata is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current)	MB81C1000A–60	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	74	mA
	MB81C1000A–70					68	
	MB81C1000A–80					62	
	MB81C1000A–10					54	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			1.0	
Refresh current #1 (Average power supply current)	MB81C1000A–60	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	74	mA
	MB81C1000A–70					68	
	MB81C1000A–80					62	
	MB81C1000A–10					54	
Fast Page Mode current	MB81C1000A–60	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	60	mA
	MB81C1000A–70					55	
	MB81C1000A–80					50	
	MB81C1000A–10					43	
Refresh current #2 (Average power supply current)	MB81C1000A–60	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	74	mA
	MB81C1000A–70					68	
	MB81C1000A–80					62	
	MB81C1000A–10					54	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000A-60		MB81C1000A-70		MB81C1000A-80		MB81C1000A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	130	—	140	—	155	—	180	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	160	—	180	—	210	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	60	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	15	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	0	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	0	—	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	—	20	—	25	ns
10	Transition Time		t_T	2	50	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	60	—	65	—	70	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	20	50	22	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	20	—	20	—	20	—	20	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	12	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	17	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time		t_{WCH}	10	—	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	12	—	12	—	15	—	20	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000A-60		MB81C1000A-70		MB81C1000A-80		MB81C1000A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	60	—	70	—	80	—	100	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	15	—	20	—	20	—	25	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	30	—	35	—	40	—	50	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	12	—	15	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	45	—	50	—	55	—	65	—	ns
51	Fast Page Mode Read–Modify–Write Cycle Time		t_{PRWC}	62	—	67	—	75	—	90	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	40	—	45	—	50	—	60	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIH (min) and VIL (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

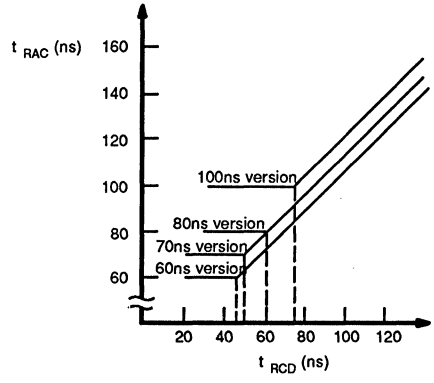
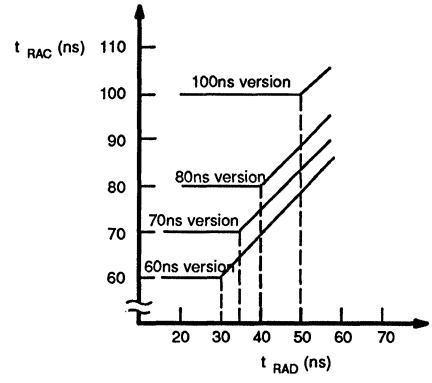


Fig. 3 – t_{RAC} vs. t_{RAD}



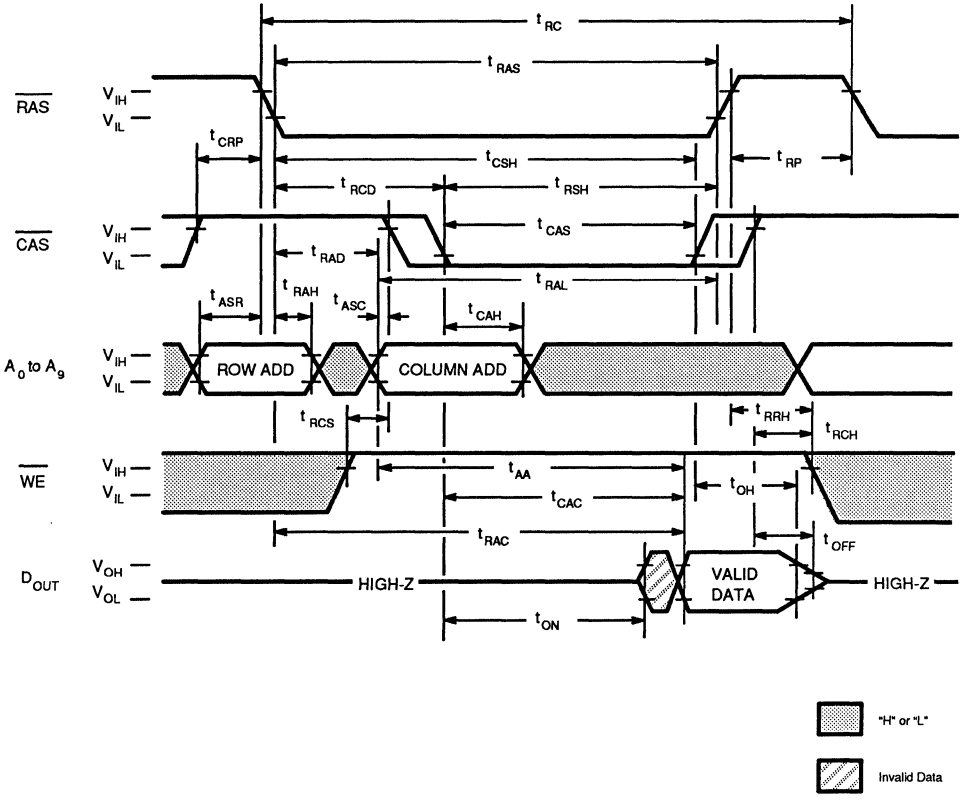
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Fast Page Mode.

Fig. 4 – READ CYCLE

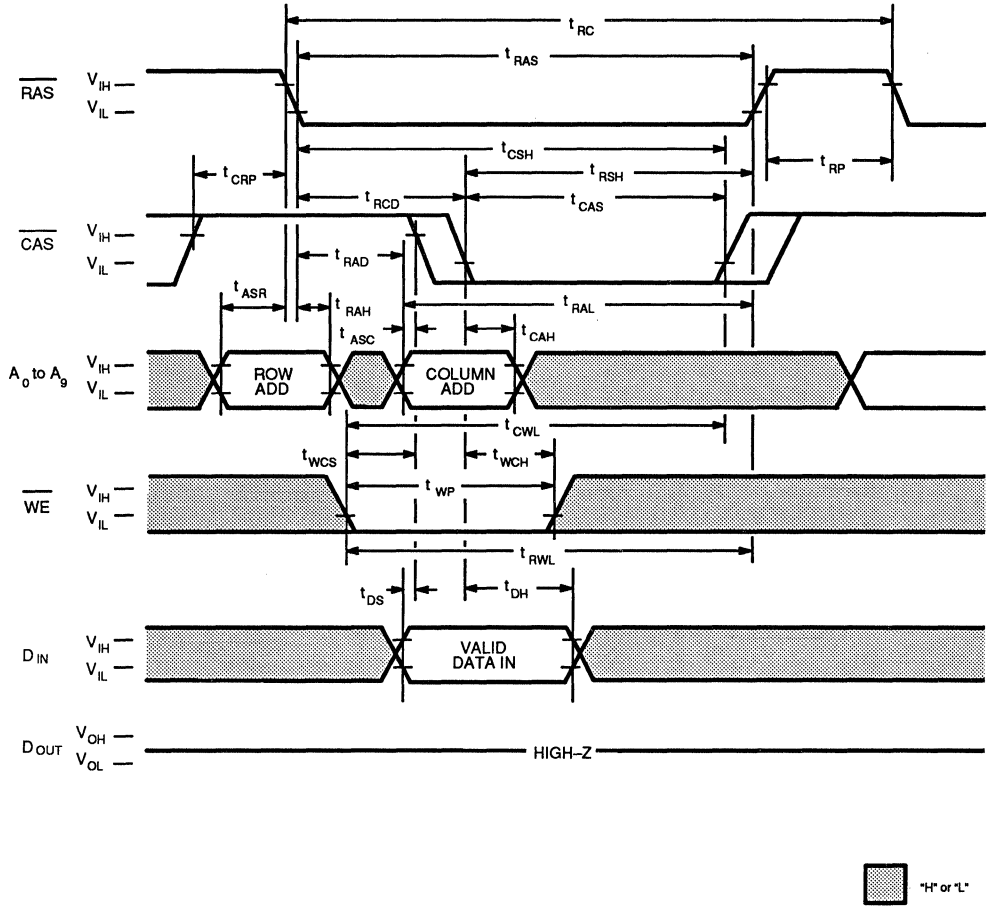


DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

2

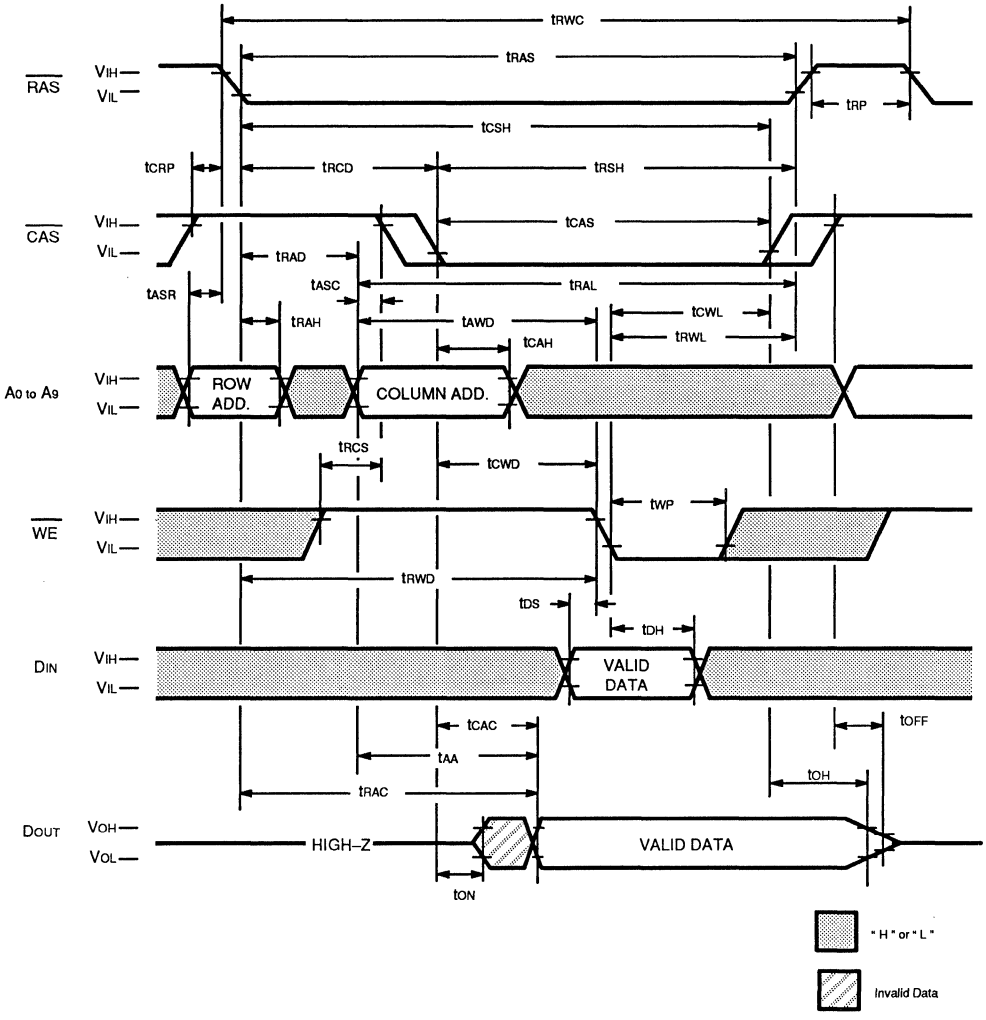
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin islatched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE

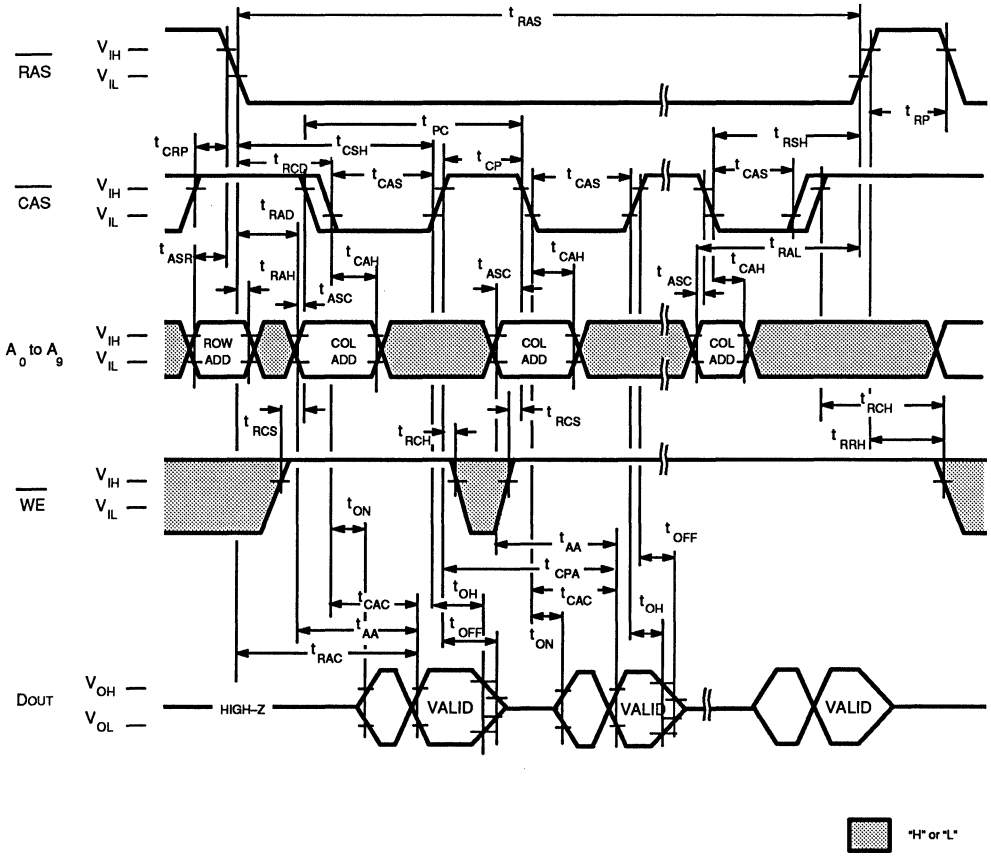


DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

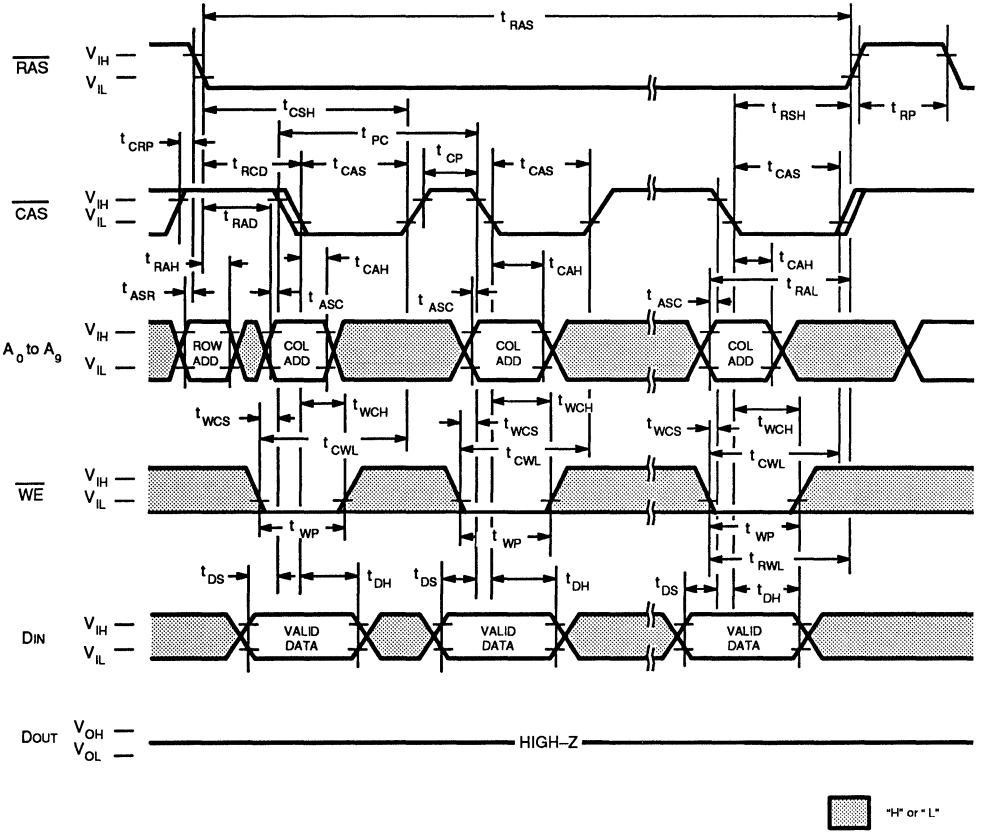
Fig. 7 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later.
Any of the 1024 bits belonging to each row can be accessed.

Fig. 8 – FAST PAGE MODE WRITE CYCLE (Early Write)

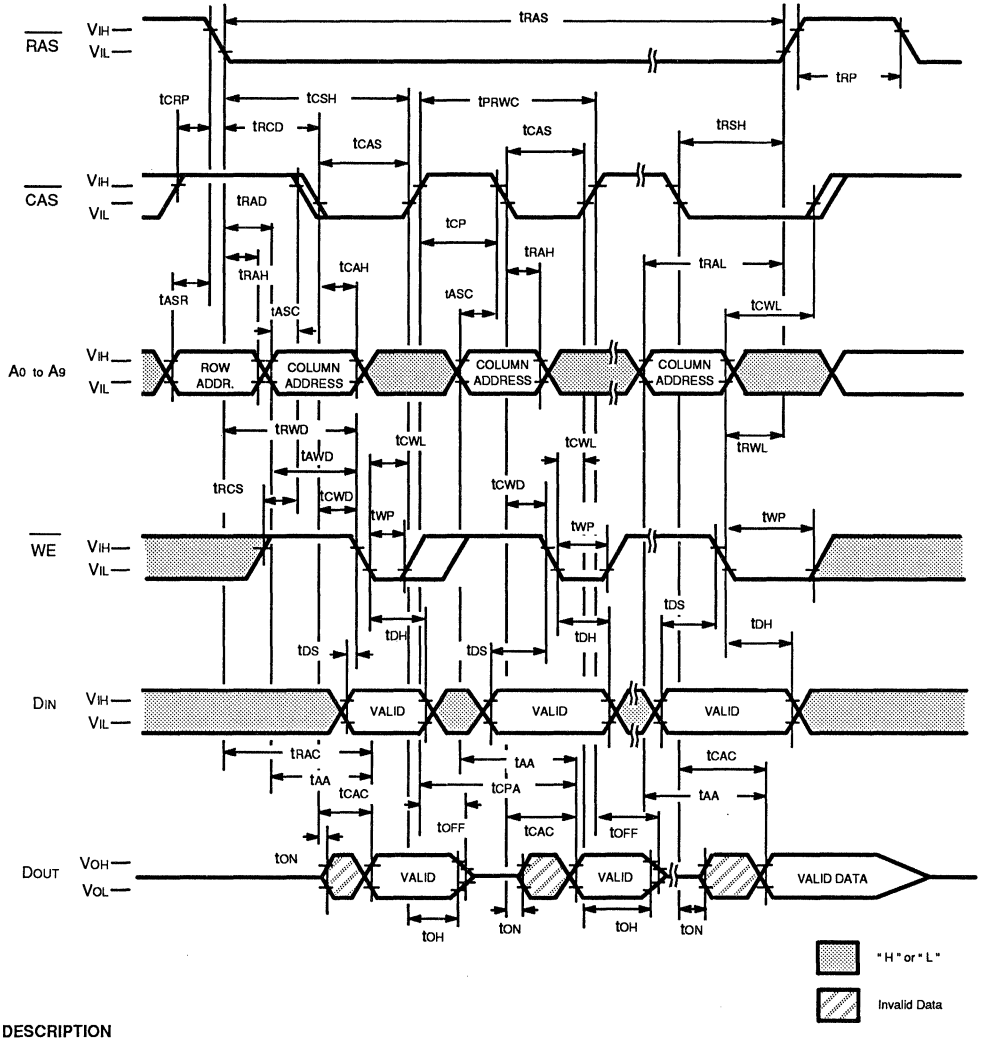


DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 1024 bits belonging to each row can be accessed.

2

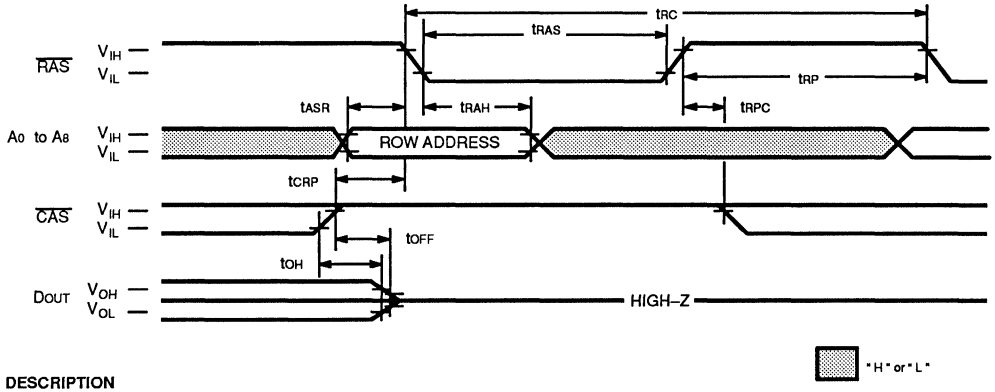
Fig. 9 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode, the read–modify–write cycle can be executed by changing $\overline{WE}$ high to low after the data appearsat DOUT pin as well as normal cycle. Any of the 1024 bits belonging to each row can be accessed.

Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

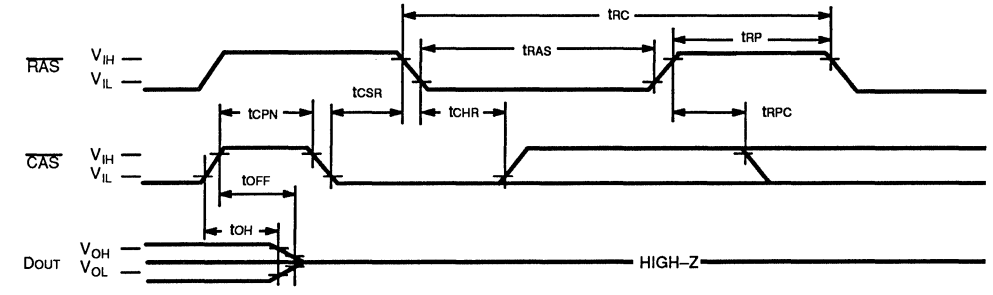


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "



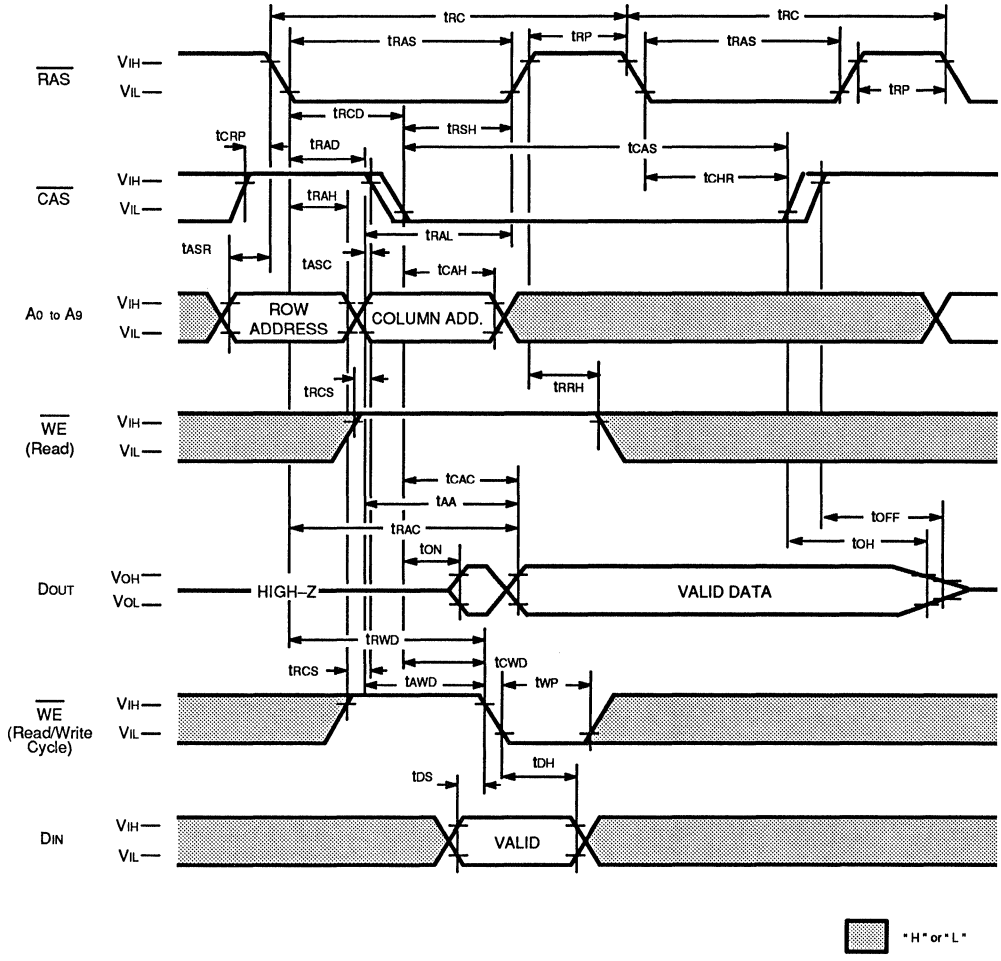
DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

2

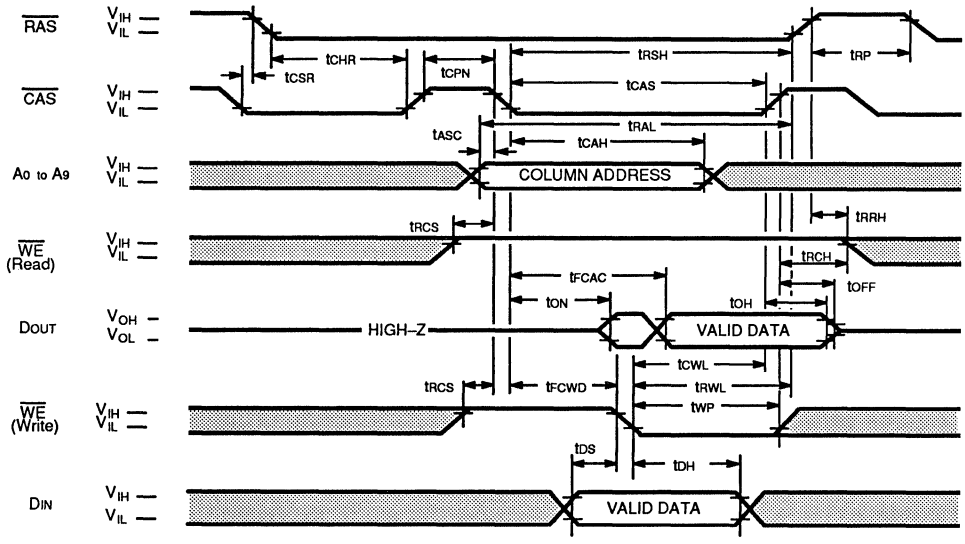
Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter. The bit A9 is set high internally.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (read–modify–write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

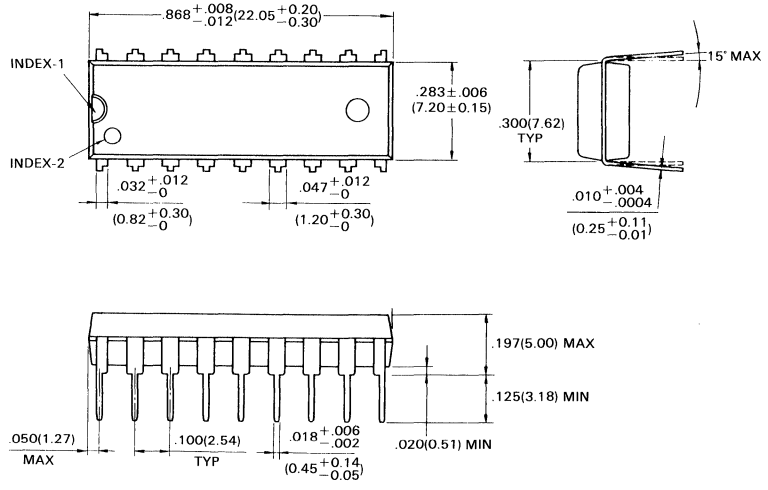
No.	Parameter	Symbol	MB81C1000A–60		MB81C1000A–70		MB81C1000A–80		MB81C1000A–10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	40	—	45	—	50	—	60	ns
91	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	40	—	45	—	50	—	60	—	ns

Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix: –P)

18–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–18P–M04)

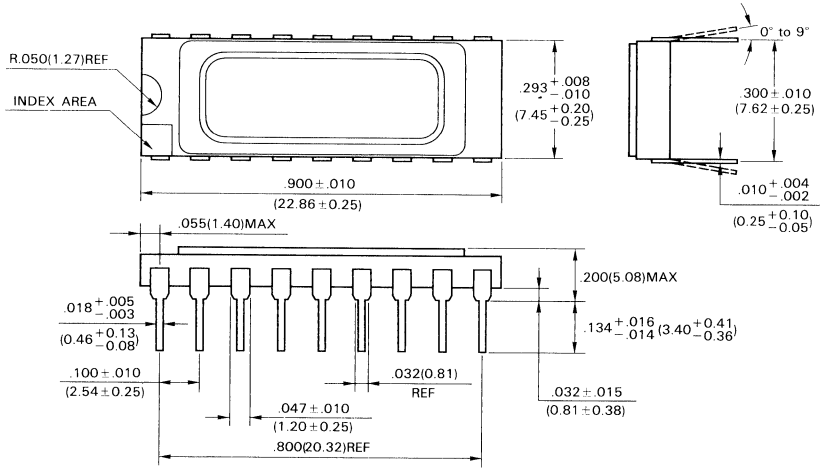


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18–LEAD CERAMIC (METAL SEAL) DUAL IN–LINE PACKAGE
(CASE No.: DIP–18C–A02)



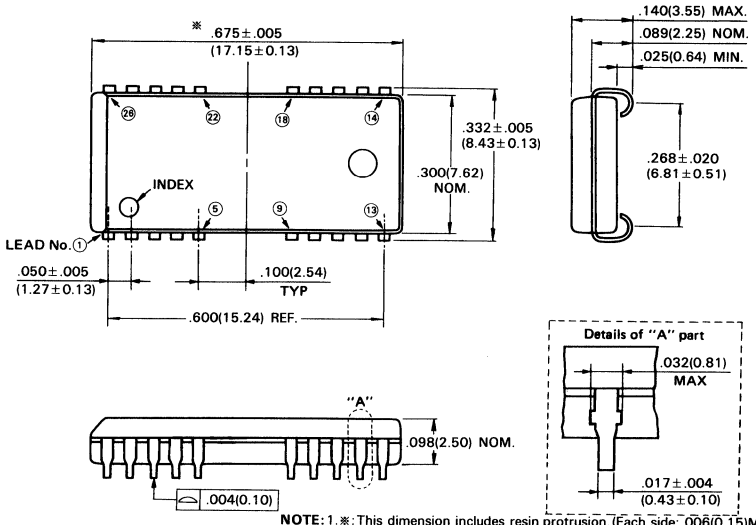
Dimensions in inches (millimeters).

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)
(CASE No.: LCC–26P–M04)

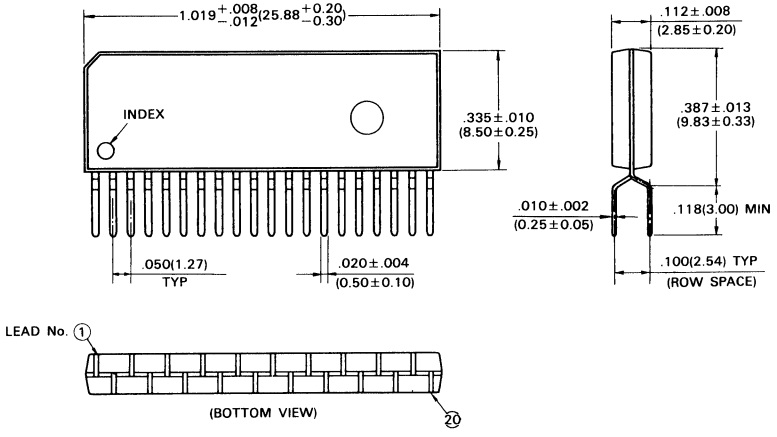


NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26 lead package.
3. Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20–LEAD PLASTIC ZIGZAG–IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



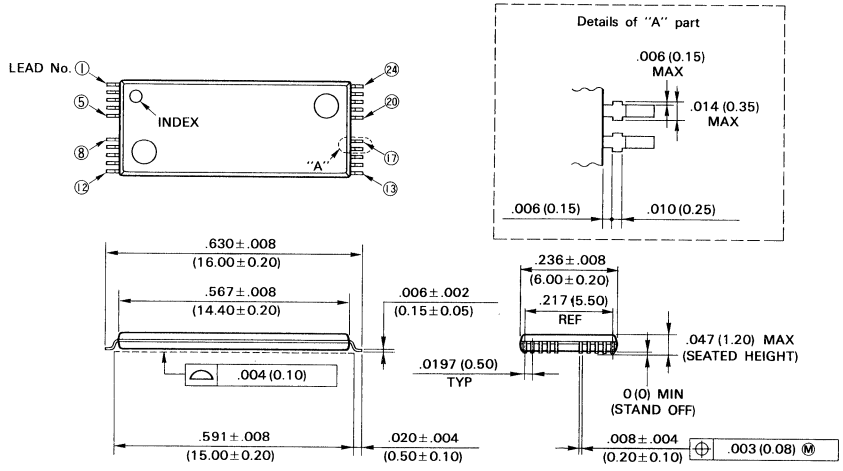
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PFTN)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M04)

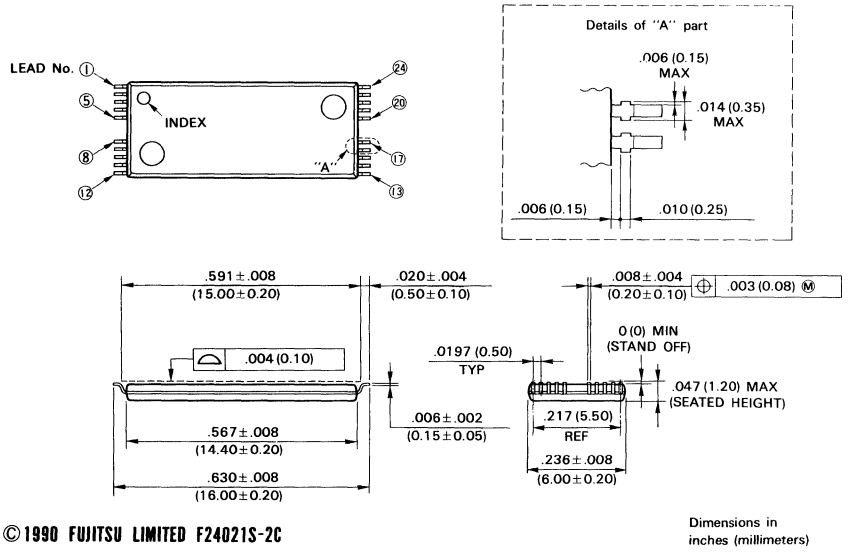


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M05)



Dimensions in inches (millimeters)

2

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November 1990
Edition 2.0

FUJITSU

DATA SHEET

MB81C1000A-70L/-80L/-10L

CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Fast Page Mode DRAM

The Fujitsu MB81C1000A is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000A has been designed for mainframe memories, buffer memories, peripheral storage and memory systems of battery operated computers requiring very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1000A high α-ray soft error immunity and extended refresh time. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

Features

Parameter	MB81C1000A -70L	MB81C1000A -80L	MB81C1000A -10L
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.
Address Access Time	35 ns max.	40 ns max.	50 ns max.
$\overline{CAS}$ Access Time	20 ns max.	20 ns max.	25 ns max.
Fast Page Mode Cycle Time	50 ns min.	55 ns min.	65 ns min.
Low Power Dissipation • Operating Current	374 mW max.	341 mW max.	297 mW max.
• Standby Current	5.5 mW max. (TTL level)/1.4 mW max. (CMOS level)		

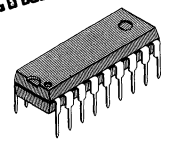
- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 64 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

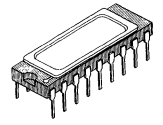
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

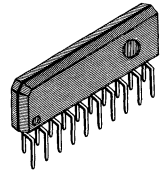


DIP–18P–M04



DIP–18C–A02

LCC–26P–M04



ZIP–20P–M02

FPT–24P–M04 / FPT–24P–M05

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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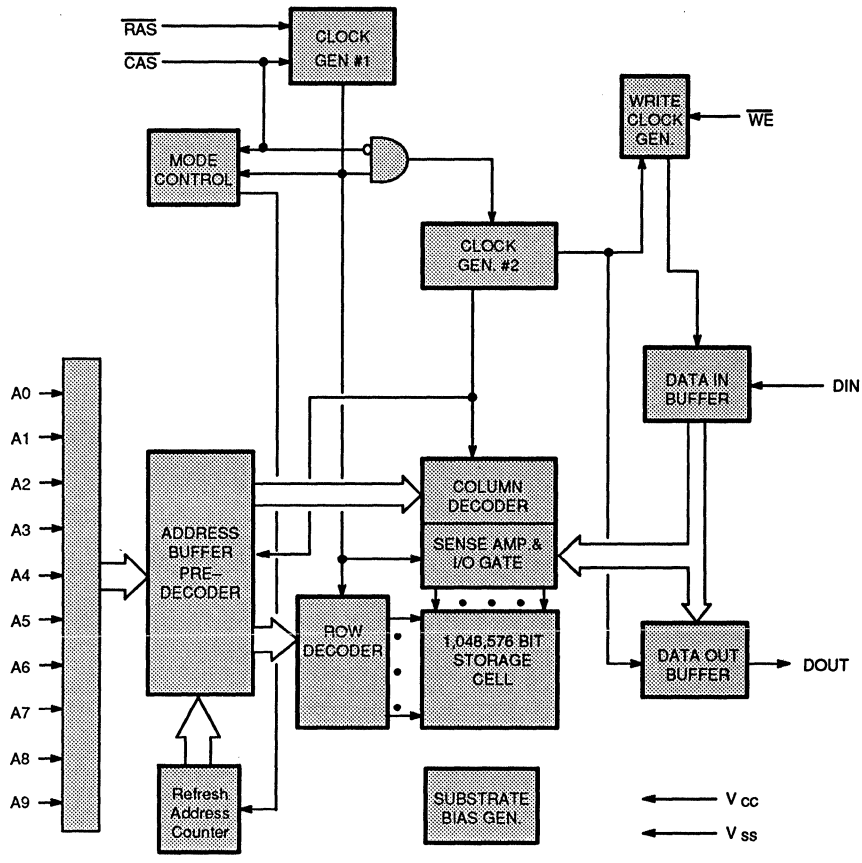
Fig. 1 — MB81C1000A DYNAMIC RAM—BLOCK DIAGRAM

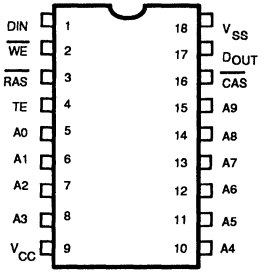


CAPACITANCE (T_A = 25°C, f = 1MHz)

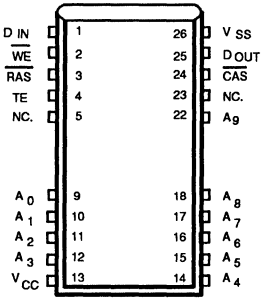
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

18–Pin DIP:
(TOP VIEW)

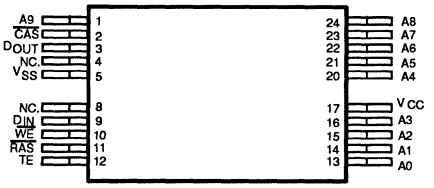


26–Pin SOJ:
(TOP VIEW)

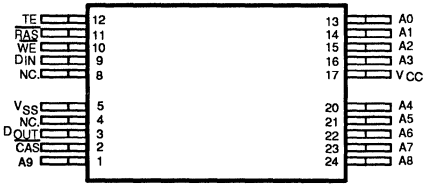


24–Pin FPT :
(TOP VIEW)

<Normal Bend : FPT–24P–M04>

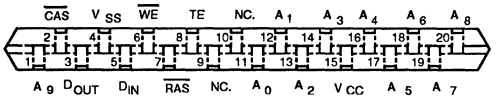


<Reverse Bend : FPT–24P–M05>



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

20–Pin ZIP:
(TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Data is written into the MB81C1000A during write or read–modify–write cycle. The inputdata is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current) [2]	MB81C1000A–70L	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	68	mA
	MB81C1000A–80L					62	
	MB81C1000A–10L					54	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	1.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			0.25	
Refresh current #1 (Average power supply current) [2]	MB81C1000A–70L	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	68	mA
	MB81C1000A–80L					62	
	MB81C1000A–10L					54	
Fast Page Mode current [2]	MB81C1000A–70L	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	55	mA
	MB81C1000A–80L					50	
	MB81C1000A–10L					43	
Refresh current #2 (Average power supply current) [2]	MB81C1000A–70L	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	68	mA
	MB81C1000A–80L					62	
	MB81C1000A–10L					54	
Battery Back up current (Average power supply current)	MB81C1000A–70L	ICC_6	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} =125 µs, t_{RAS} =min. to 1 µs, D_{OUT} =open. Other pin ≥ Vcc–0.2V or ≤ 0.2V	—	—	250	µA
	MB81C1000A–80L						
	MB81C1000A–10L						

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000A -70L		MB81C1000A -80L		MB81C1000A -10L		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	64	—	64	—	64	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	160	—	180	—	210	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	20	—	25	ns
10	Transition Time		t_T	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	50	22	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	20	—	20	—	20	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	35	17	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		ns
29	Write Command Hold Time		t_{WCH}	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	12	—	15	—	20	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000A -70L		MB81C1000A -80L		MB81C1000A -10L		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	70	—	80	—	100	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	20	—	20	—	25	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	35	—	40	—	50	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	10	—	12	—	15	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	50	—	55	—	65	—	ns
51	Fast Page Mode Read–Modify–Write Cycle Time		t_{PRWC}	67	—	75	—	90	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	45	—	50	—	60	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS.
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

2

Fig. 2 – t_{RAC} vs. t_{RCD}

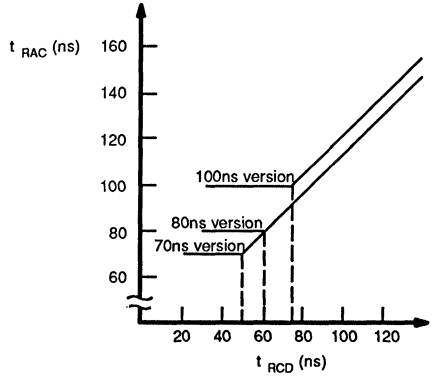
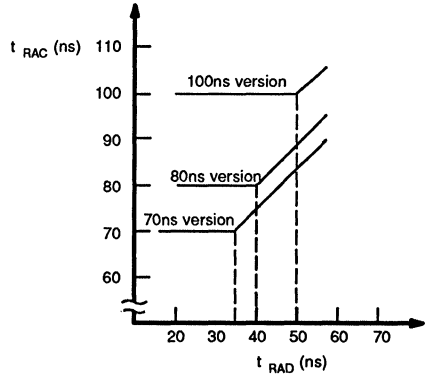


Fig. 3 – t_{RAC} vs. t_{RAD}



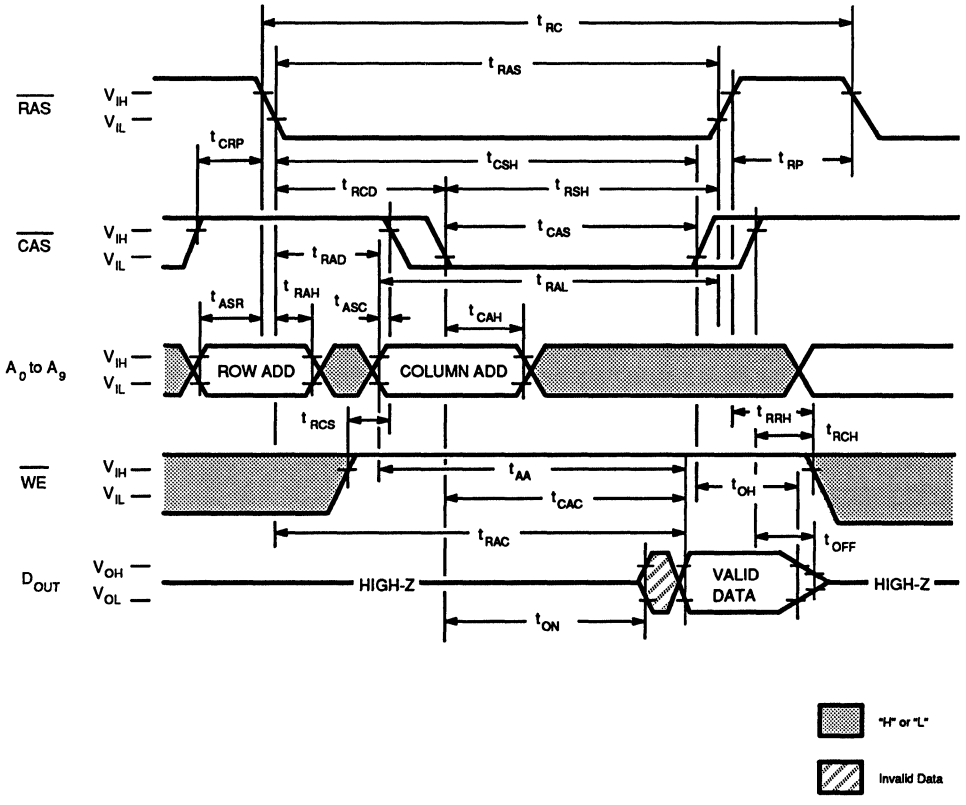
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Fast Page Mode.

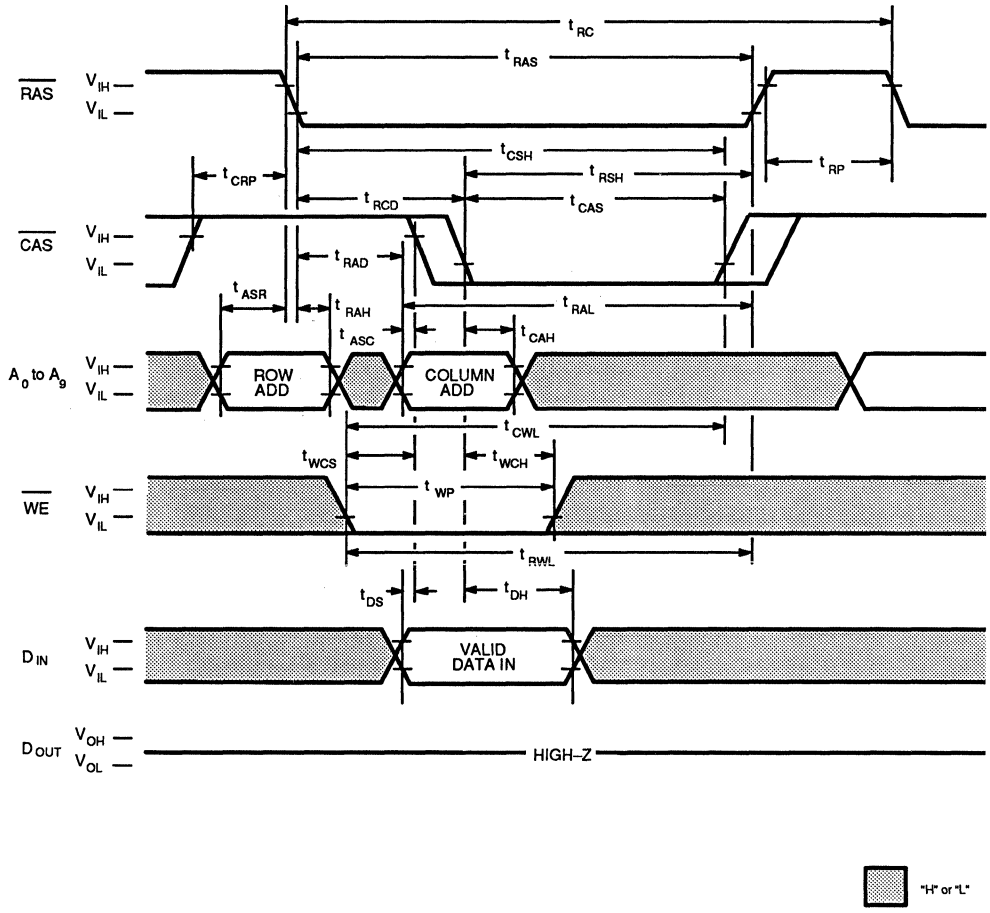
Fig. 4 – READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

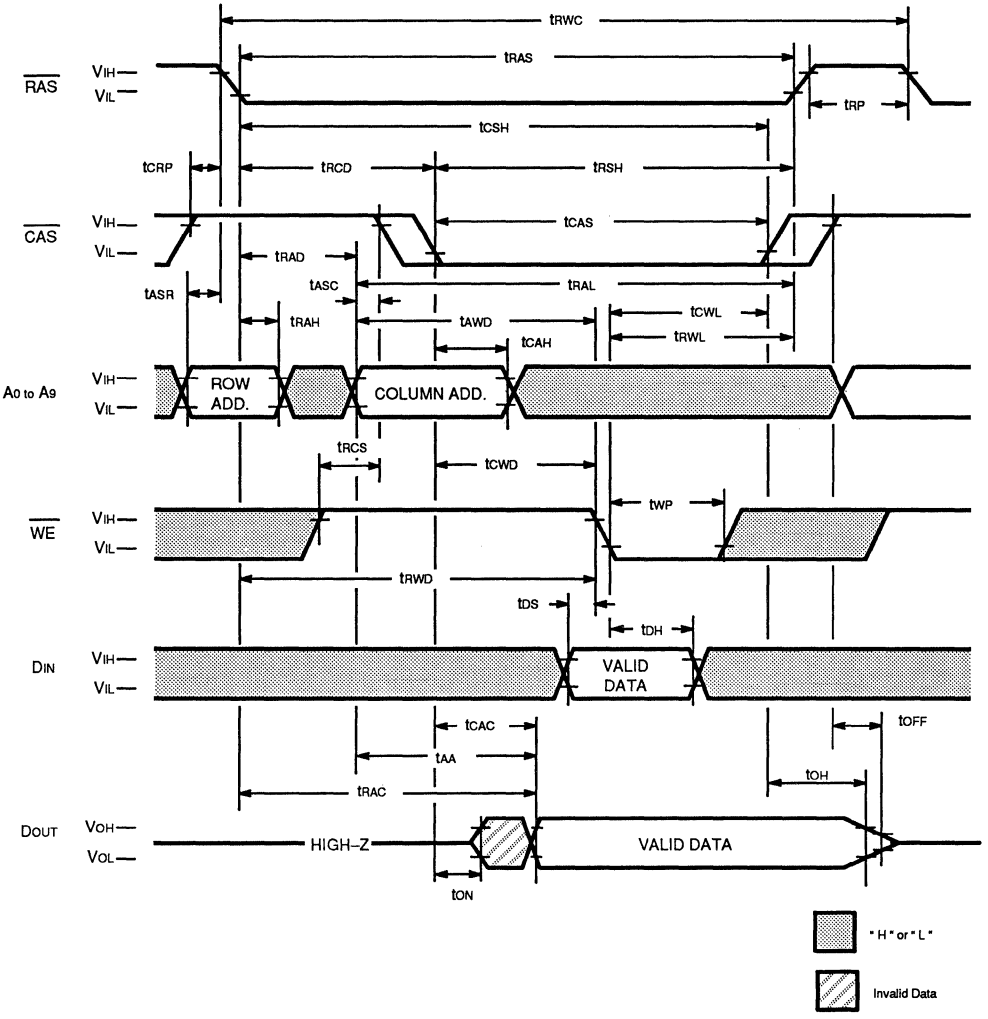
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin islatched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE

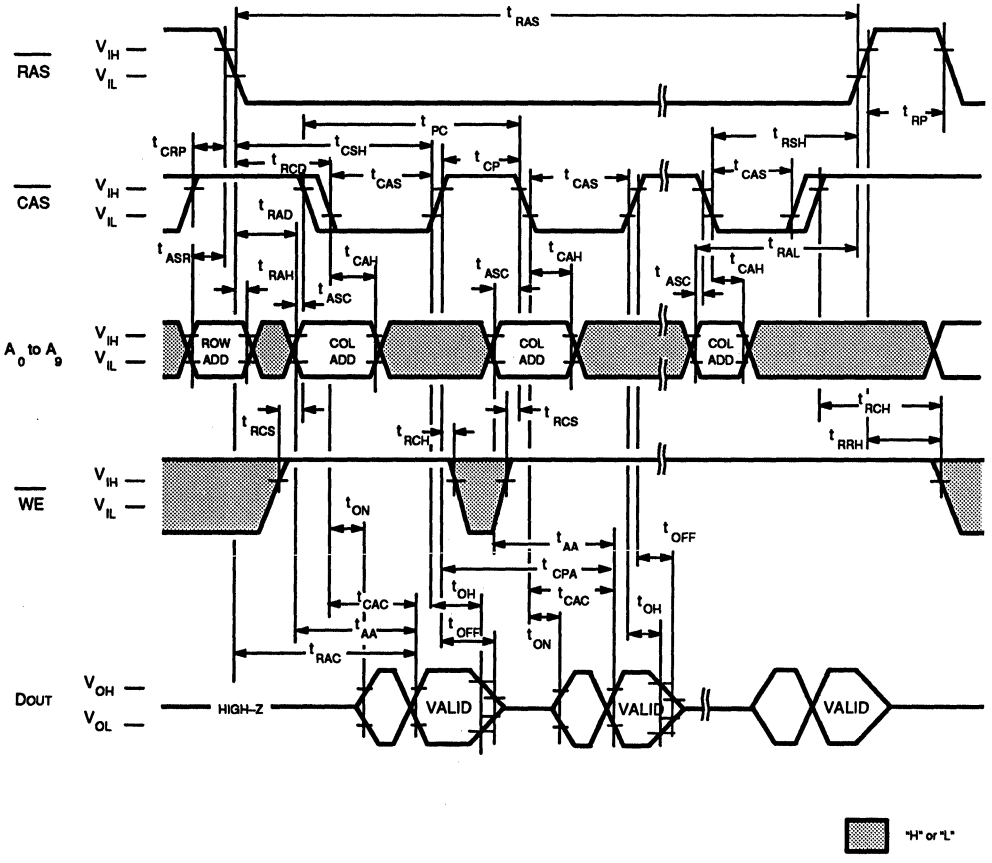


DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

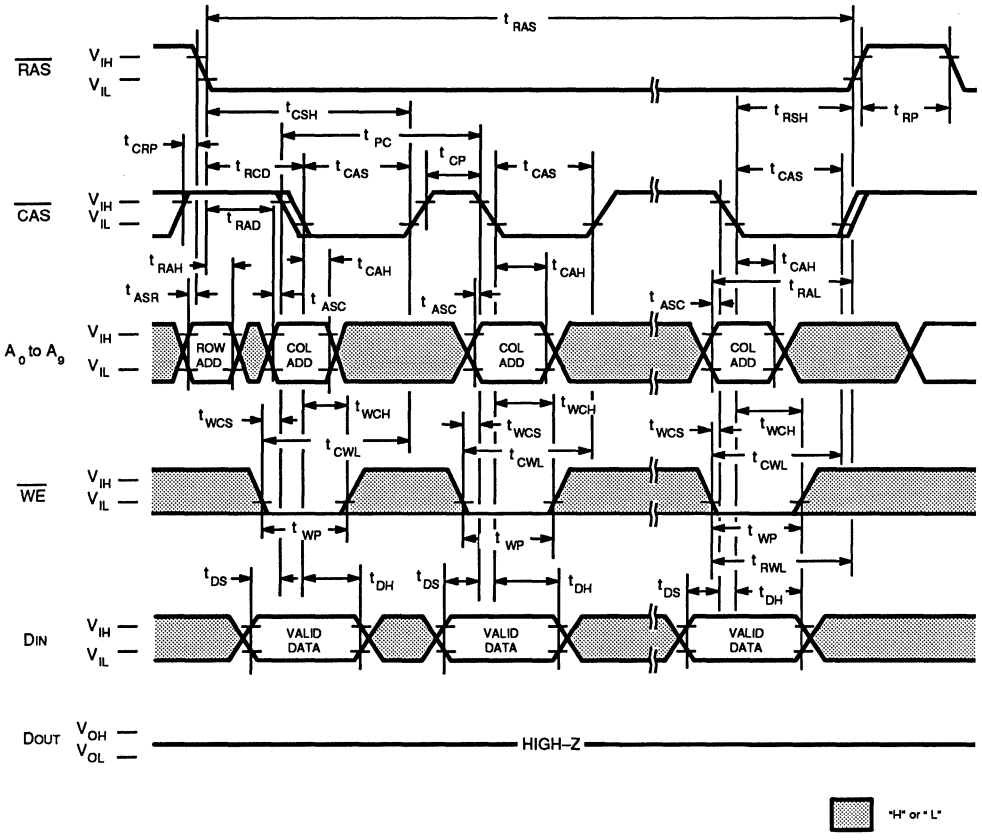
Fig. 7 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later.
Any of the 1024 bits belonging to each row can be accessed.

Fig. 8 – FAST PAGE MODE WRITE CYCLE (Early Write)

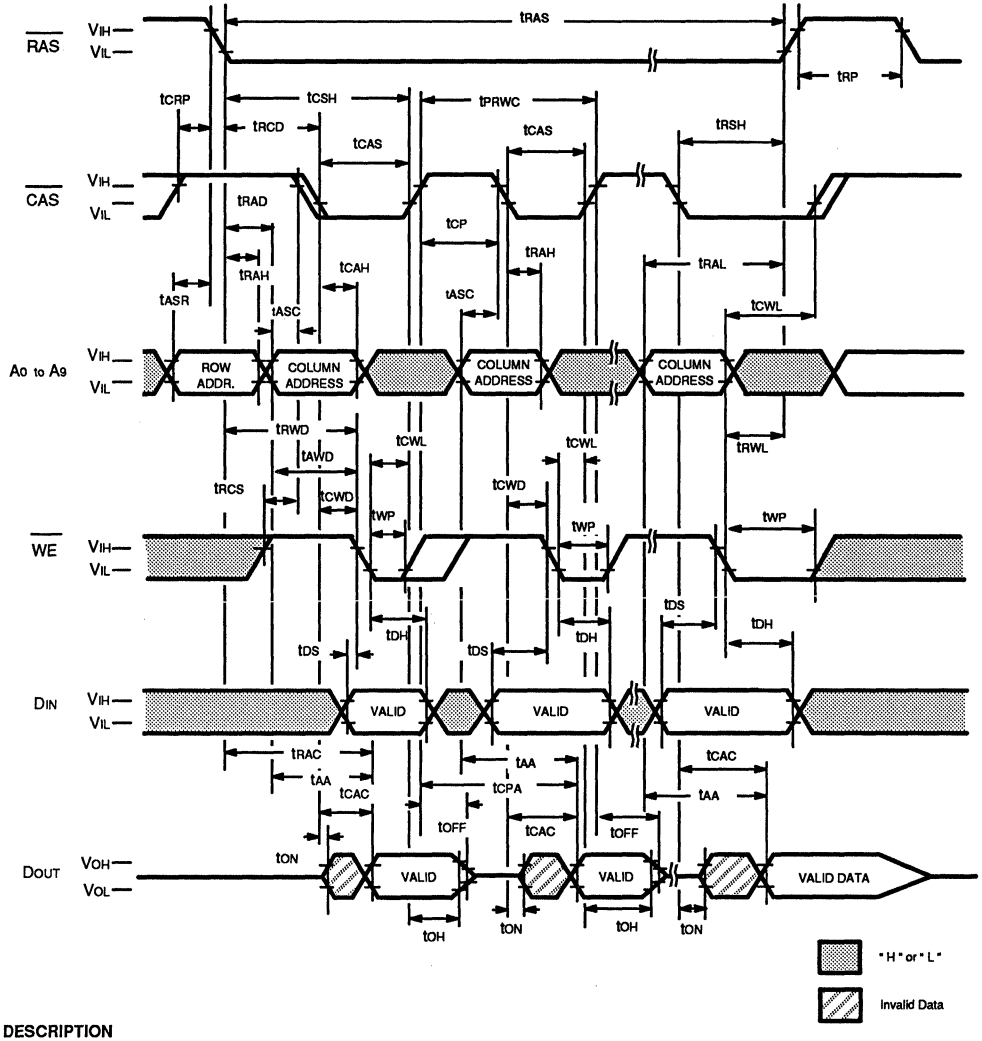


DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 1024 bits belonging to each row can be accessed.

2

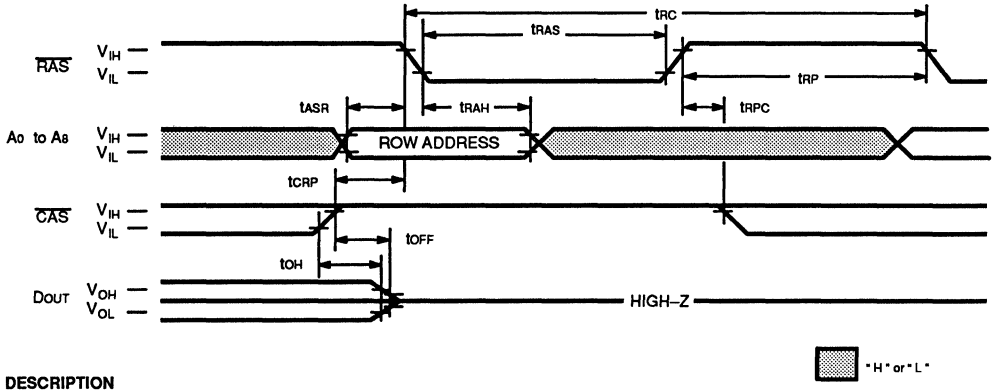
Fig. 9 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode, the read–modify–write cycle can be executed by changing $\overline{WE}$ high to low after the data appearsat DOUT pin as well as normal cycle. Any of the 1024 bits belonging to each row can be accessed.

Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

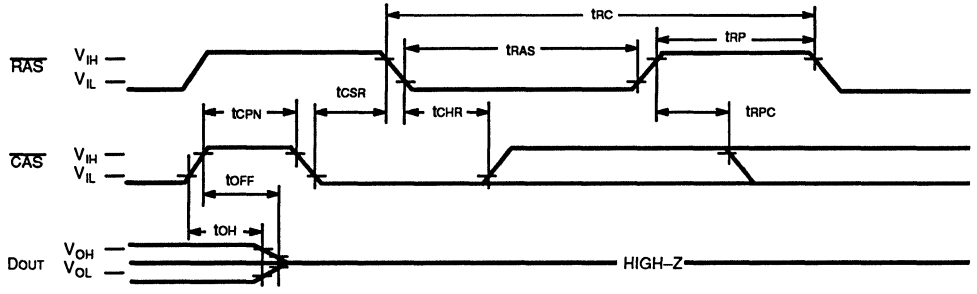


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "

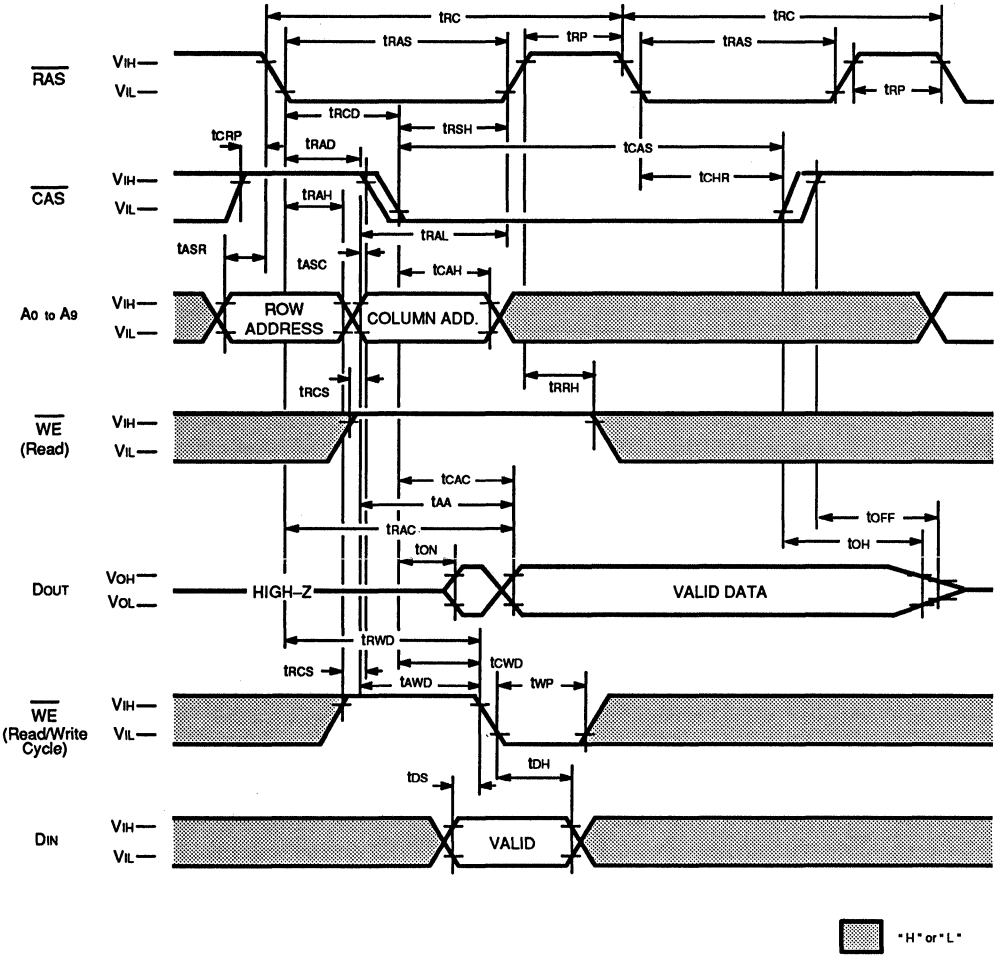


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

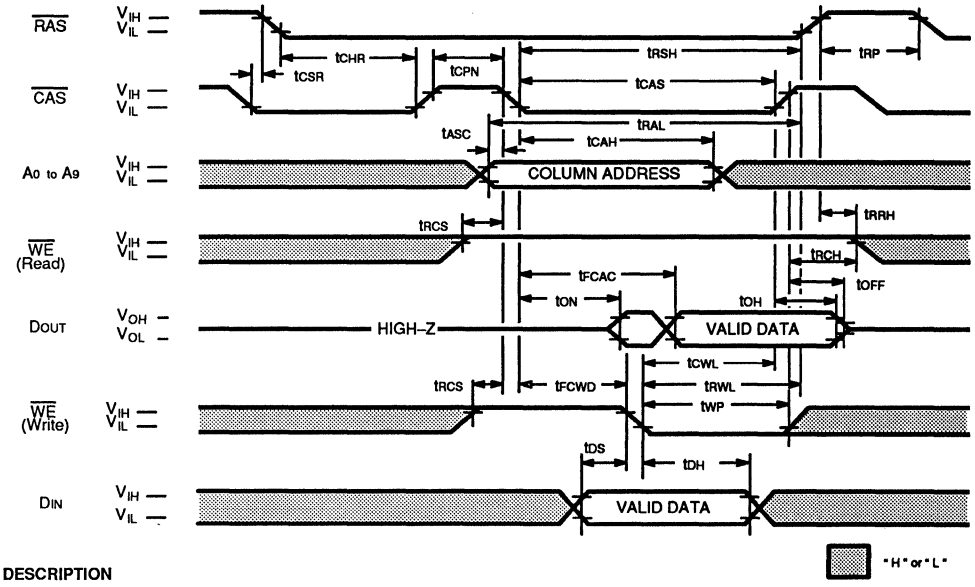
Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter. The bit A9 is set high internally.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (*read–modify–write cycles*). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

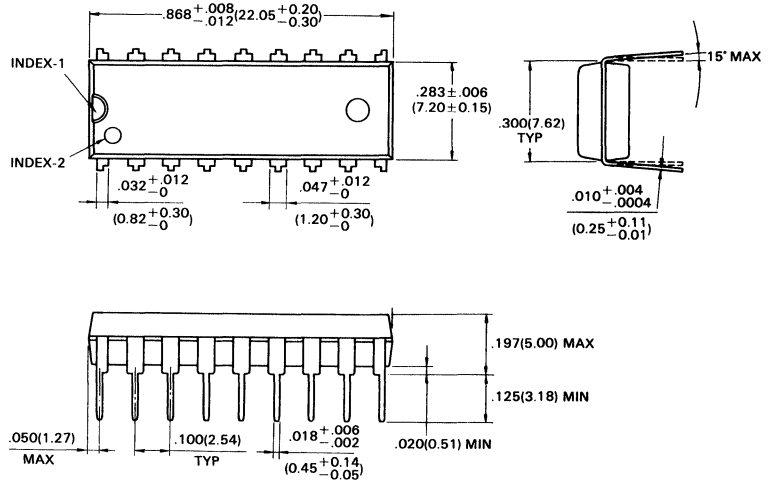
No.	Parameter	Symbol	MB81C1000A-70L		MB81C1000A-80L		MB81C1000A-10L		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	45	—	50	—	60	ns
91	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	45	—	50	—	60	—	ns

Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix: –P)

18–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–18P–M04)

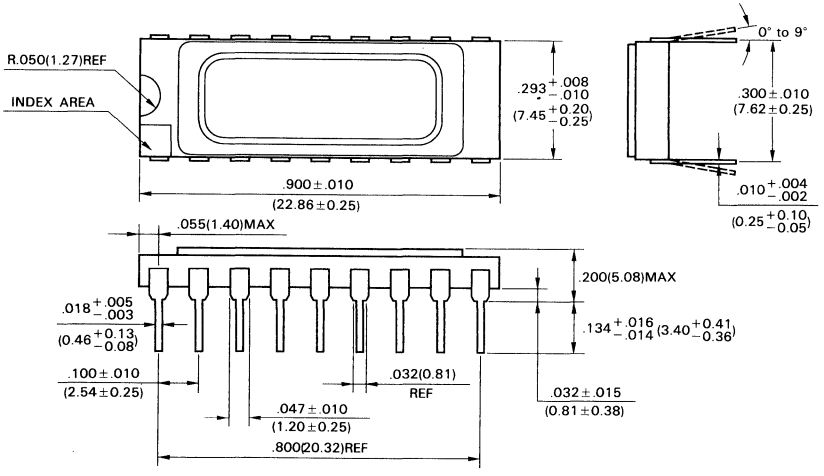


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18–LEAD CERAMIC (METAL SEAL) DUAL IN–LINE PACKAGE
(CASE No.: DIP–18C–A02)



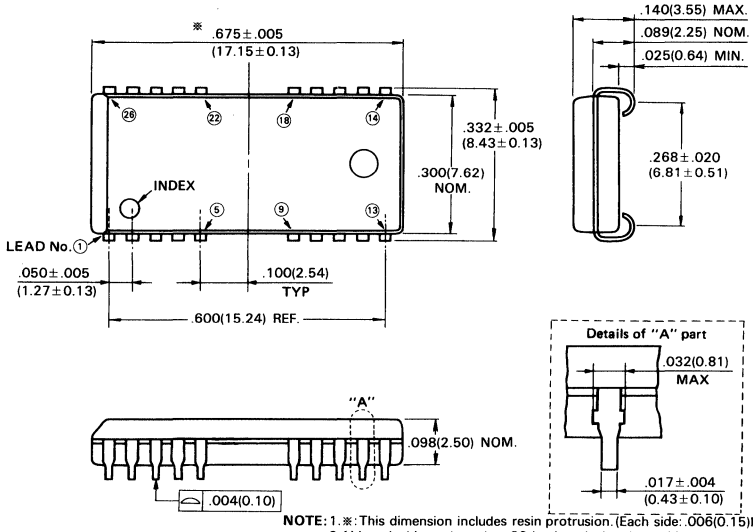
Dimensions in inches (millimeters).

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)
(CASE No.: LCC–26P–M04)

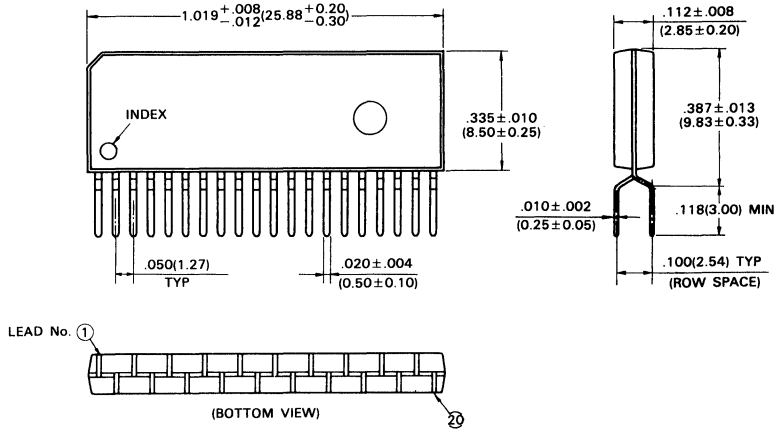


NOTE: 1. ※: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
3. Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20–LEAD PLASTIC ZIGZAG–IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



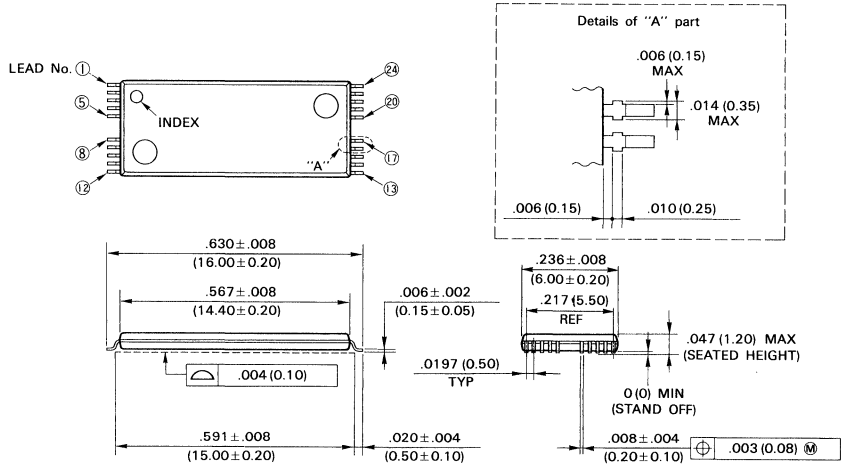
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PFTN)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M04)

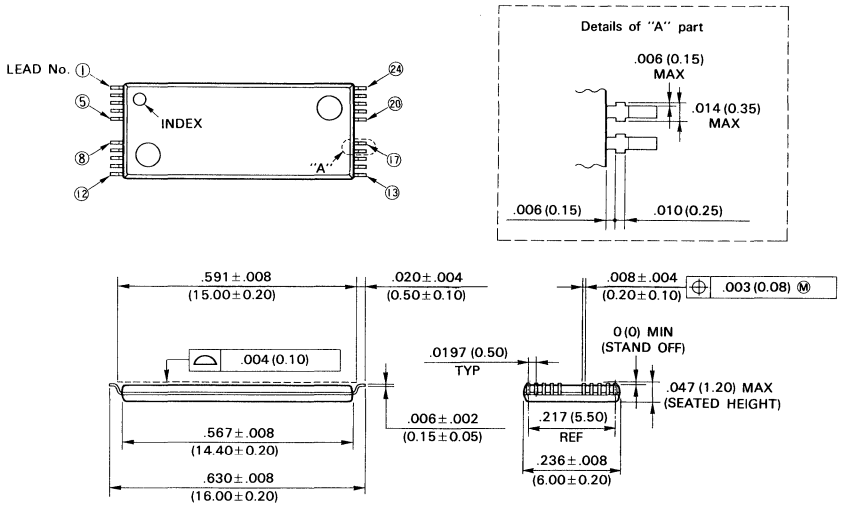


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: – PFTR)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M05)



Dimensions in inches (millimeters)

2

2

February 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C1001-70/-80/-10/-12

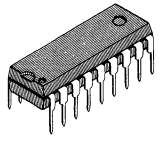
CMOS 1,048,576 BIT NIBBLE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Nibble Mode DRAM

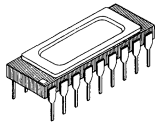
The Fujitsu MB81C1001 is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001 has been designed for mainframe memories, buffer memories, and peripheral storage applications requiring high speed, low power dissipation, and compact layout.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1001 high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

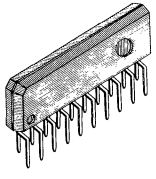


DIP–18P–M04



DIP–18C–A01

LCC–26P–M04



ZIP–20P–M02

Features

Parameter	MB81C1001 -70	MB81C1001 -80	MB81C1001 -10	MB81C1001 -12
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Nibble Mode Cycle Time	50 ns min.	50 ns min.	55 ns min.	60 ns min.
Low Power Dissipation • Operating Current	413 mW max.	385 mW max.	330 mW max.	275 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 16.4 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

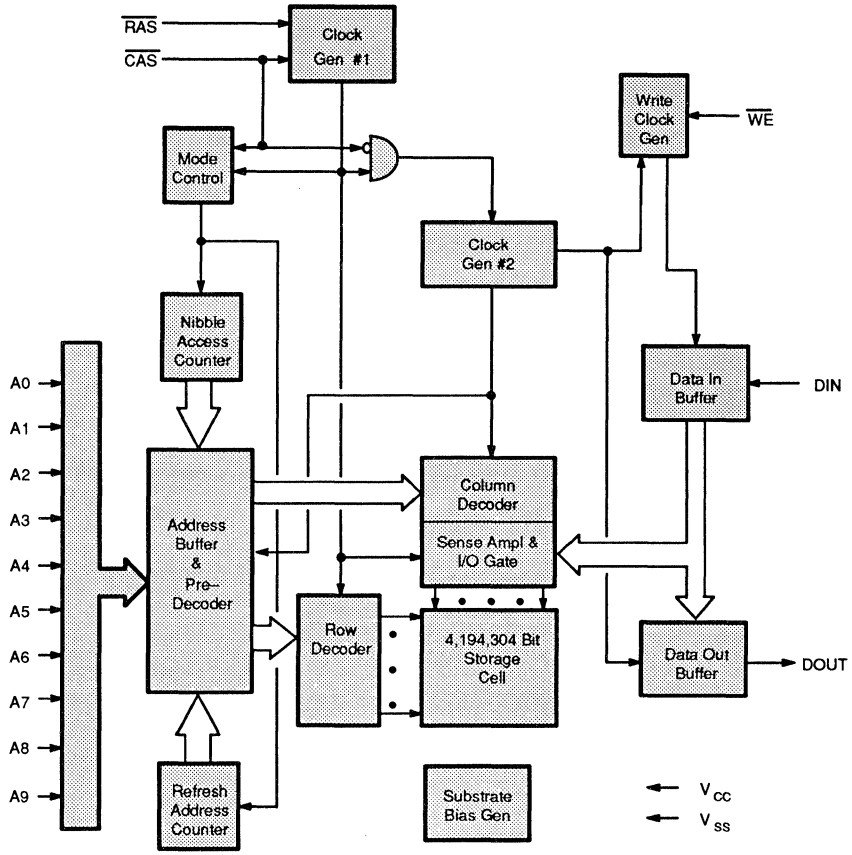
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB81C1001 DYNAMIC RAM – BLOCK DIAGRAM

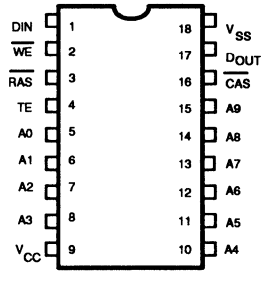


CAPACITANCE (T_A = 25°C, f = 1MHz)

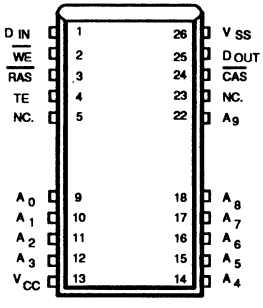
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

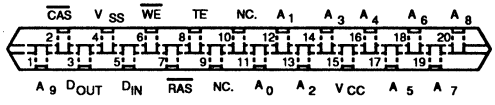
18–Pin DIP:
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Data is written into the MB81C1001 during write or read–modify–write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current) [2]	MB81C1001–70	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C1001–80					70	
	MB81C1001–10					60	
	MB81C1001–12					50	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB81C1001–70	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	70	mA
	MB81C1001–80					65	
	MB81C1001–10					55	
	MB81C1001–12					45	
Nibble Mode current [2]	MB81C1001–70	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{NC} = min	—	—	45	mA
	MB81C1001–80					45	
	MB81C1001–10					35	
	MB81C1001–12					25	
Refresh current #2 (Average power supply current) [2]	MB81C1001–70	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C1001–80					65	
	MB81C1001–10					55	
	MB81C1001–12					45	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	167	—	182	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	25	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	75	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	25	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	70	—	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	25	—	25	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	43	—	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Nibble Mode Read/Write Cycle Time		t_{NC}	45	—	45	—	45	—	60	—	ns
51	Nibble Mode Read–Modify–Write Cycle Time		t_{NRWC}	67	—	67	—	70	—	85	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{NPA}	—	40	—	40	—	40	—	55	ns
53	Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	10	—	10	—	10	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{NCP} is long, t_{NPA} is longer than t_{NPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

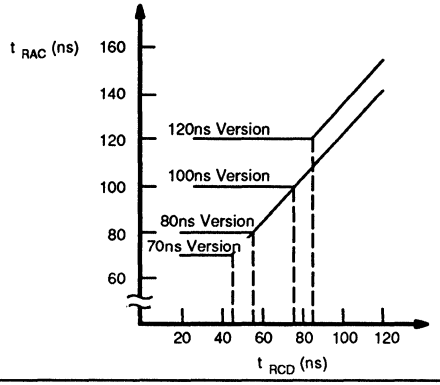
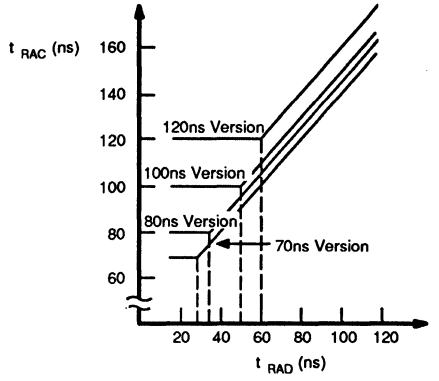


Fig. 3 – t_{RAC} vs. t_{RAD}



2

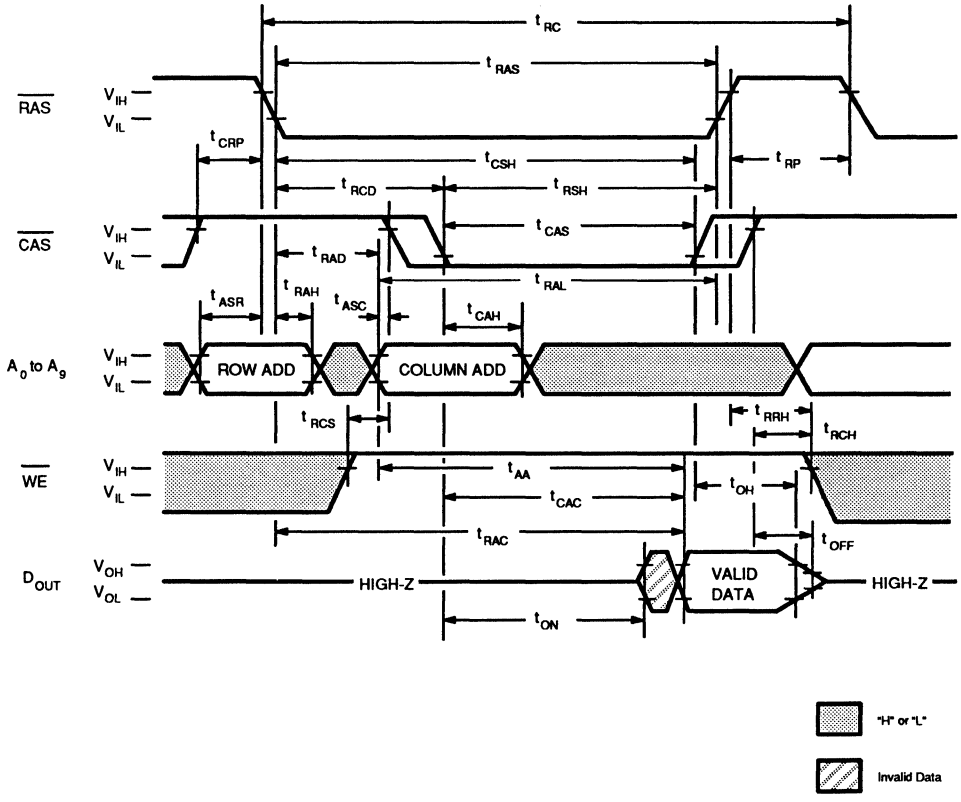
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Nibble Mode.

Fig. 4 – READ CYCLE

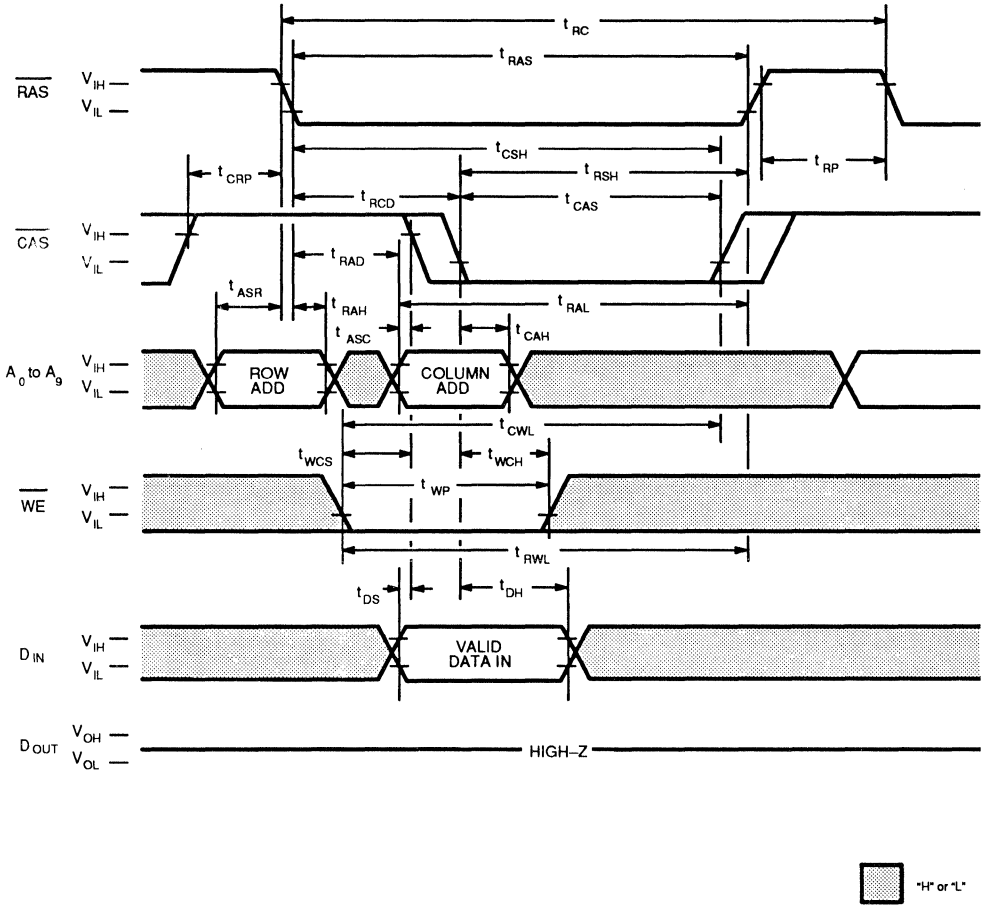


DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

2

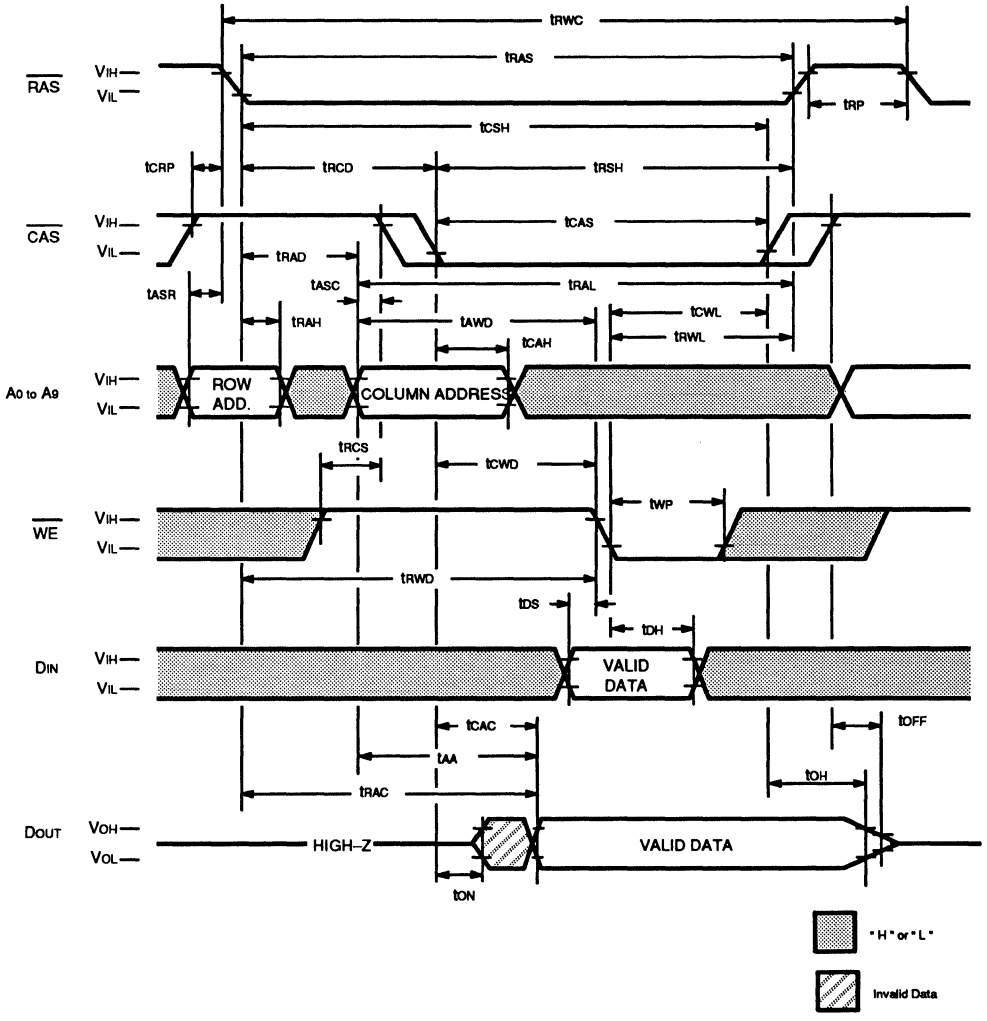
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

Fig. 7 – NIBBLE MODE READ CYCLE

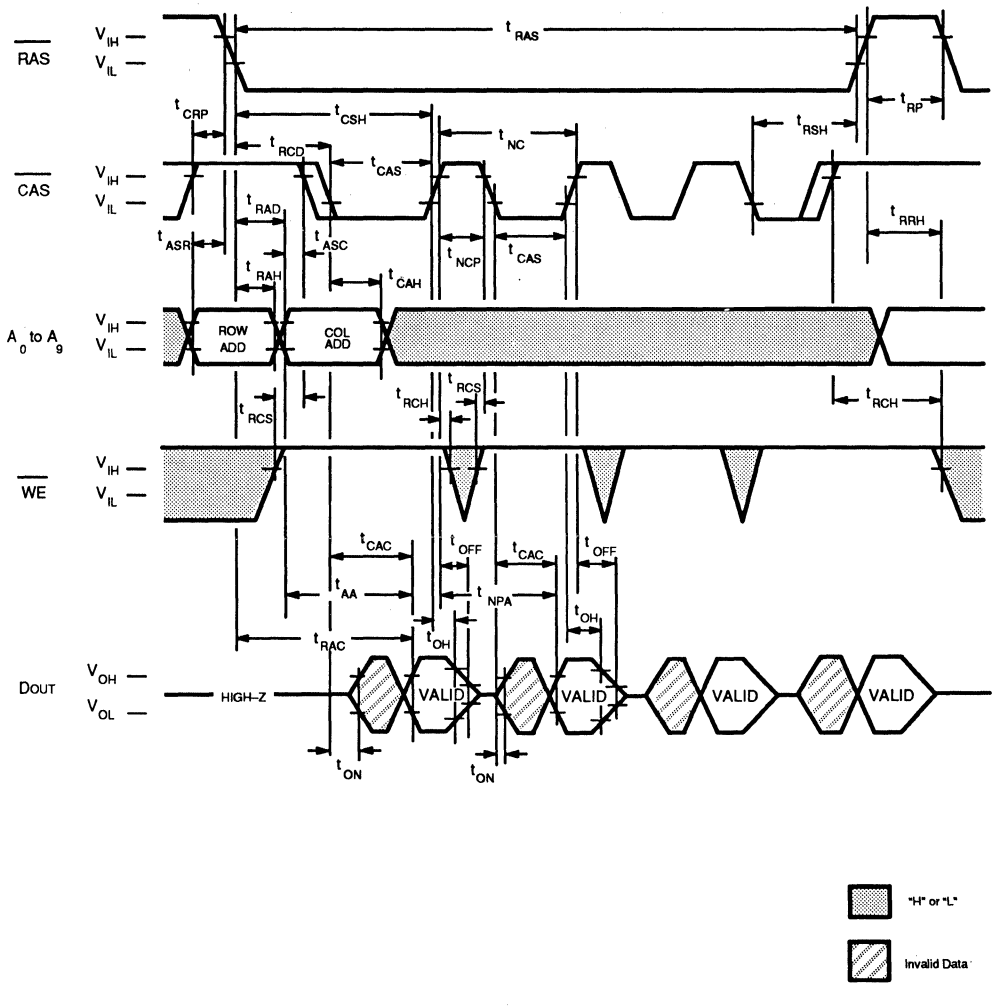
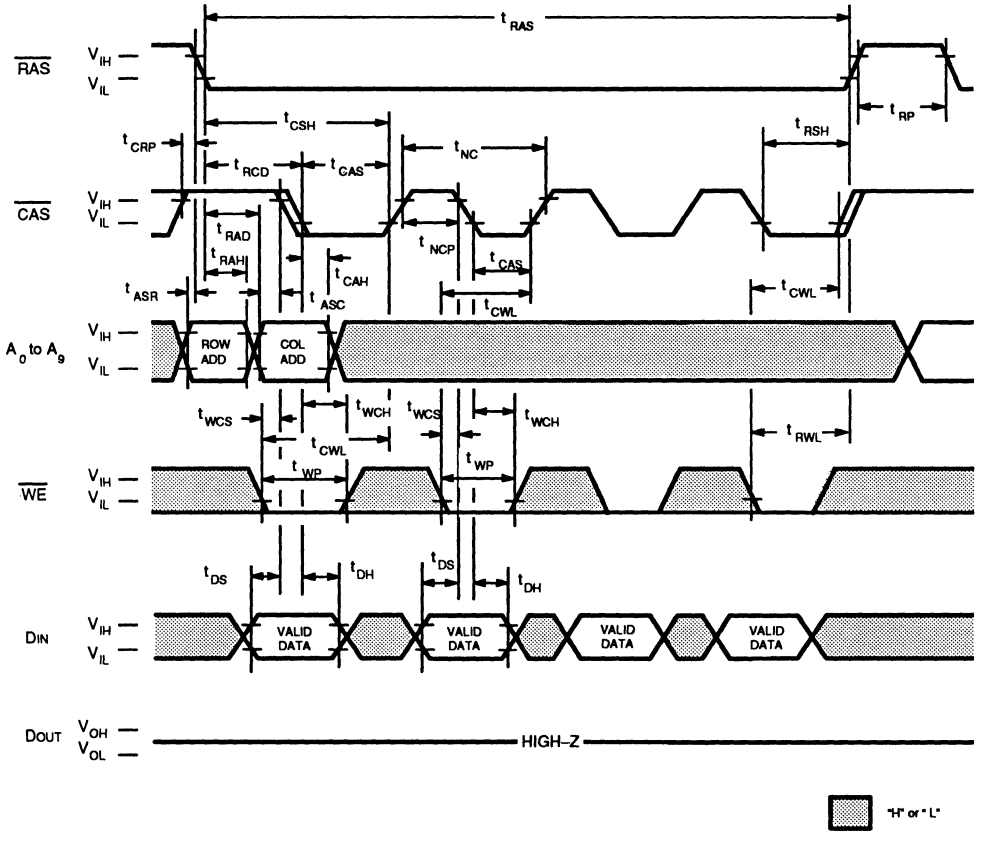


Fig. 8 – NIBBLE MODE WRITE CYCLE (Early Write)



2

Fig. 9 – NIBBLE MODE READ–MODIFY–WRITE CYCLE

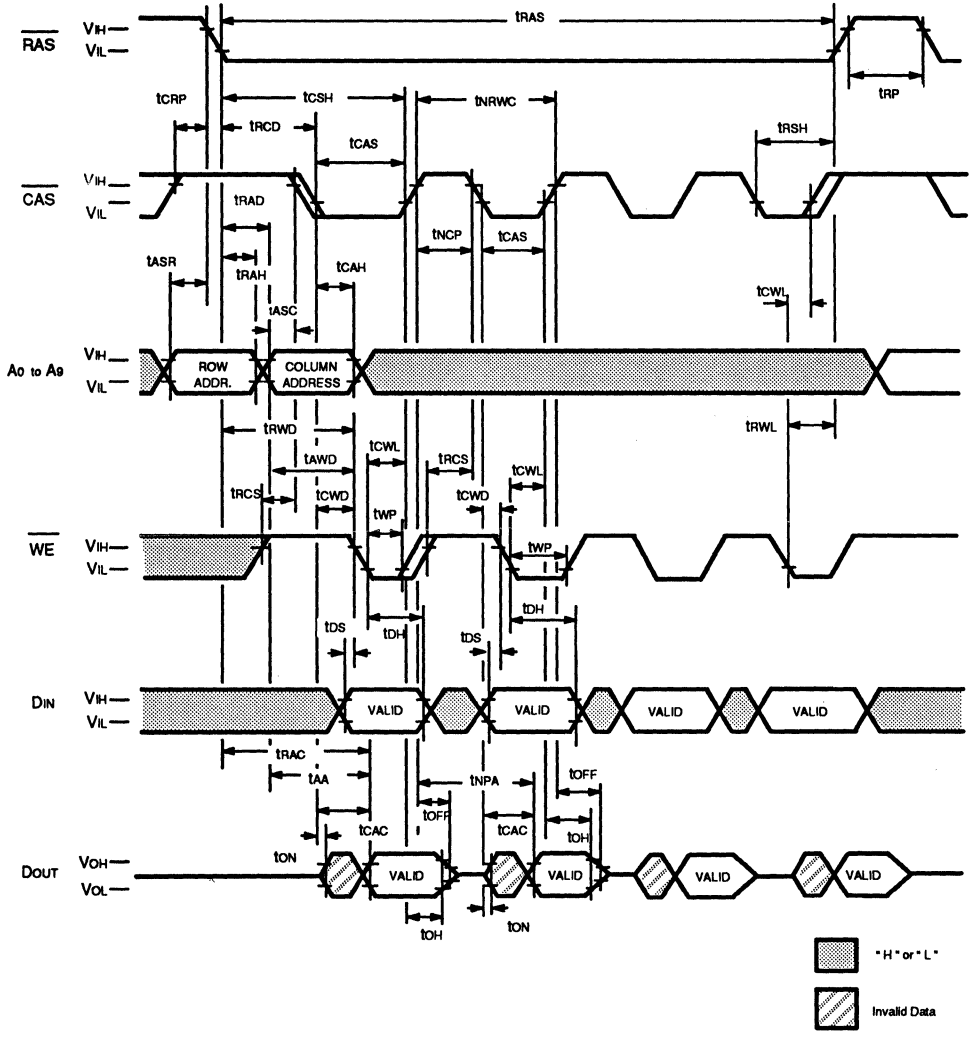
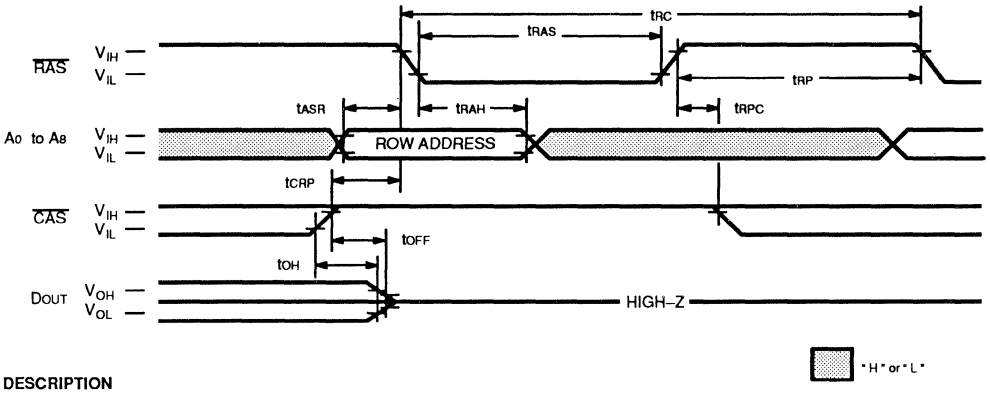


Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

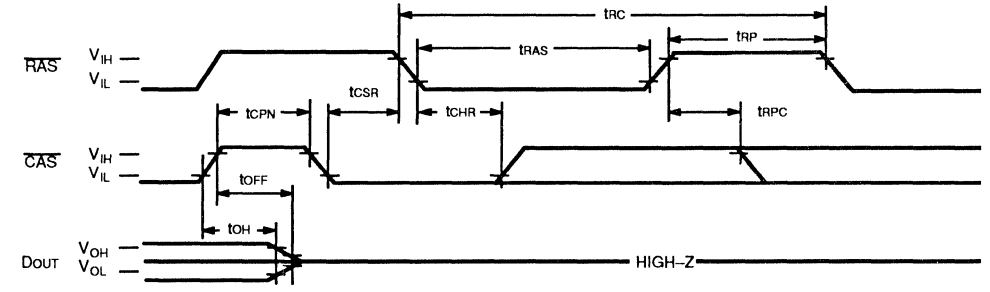


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "



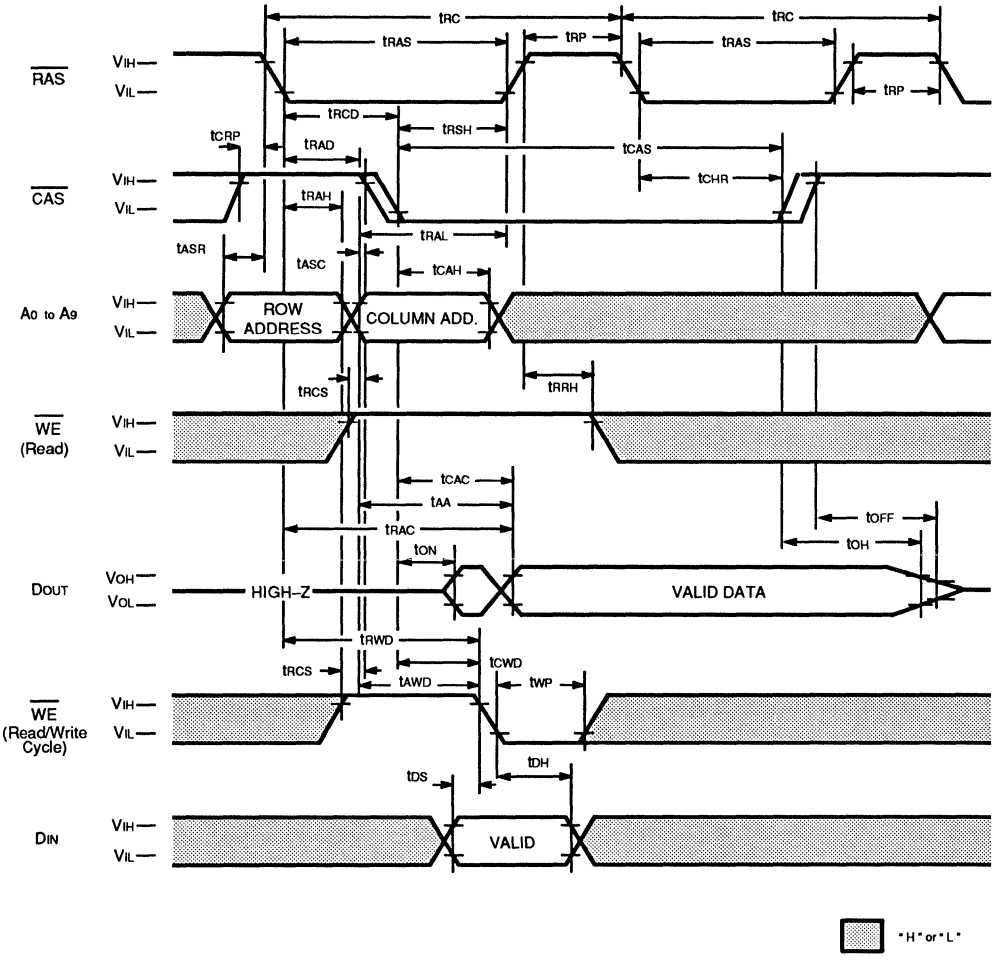
DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

2

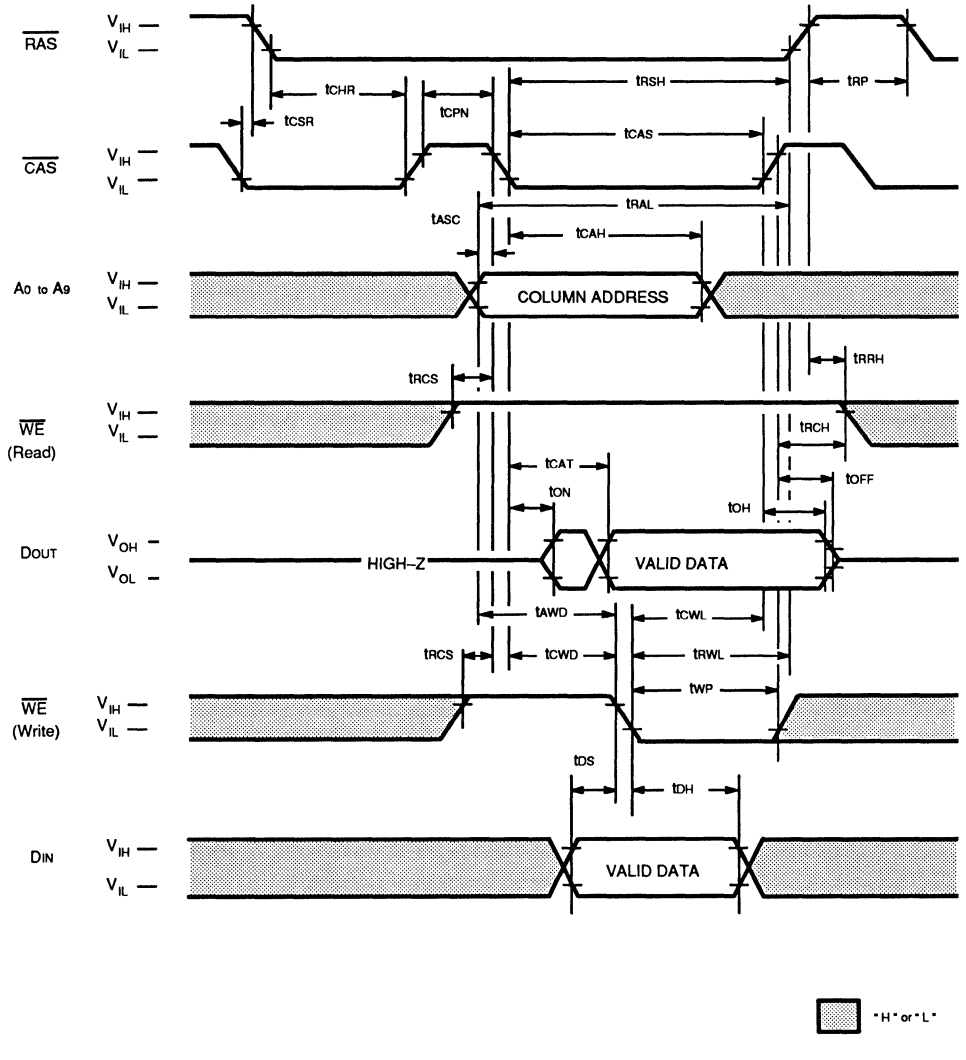
Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

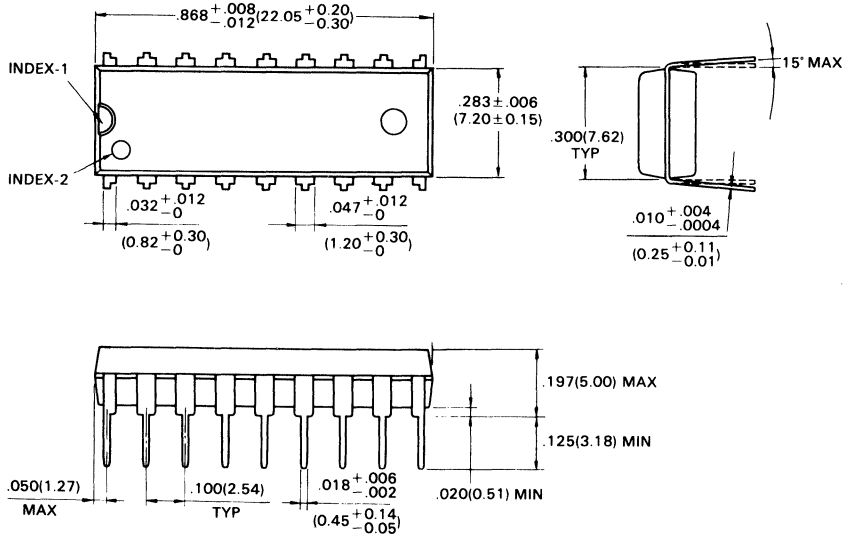


PACKAGE DIMENSIONS

(Suffix: –P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)

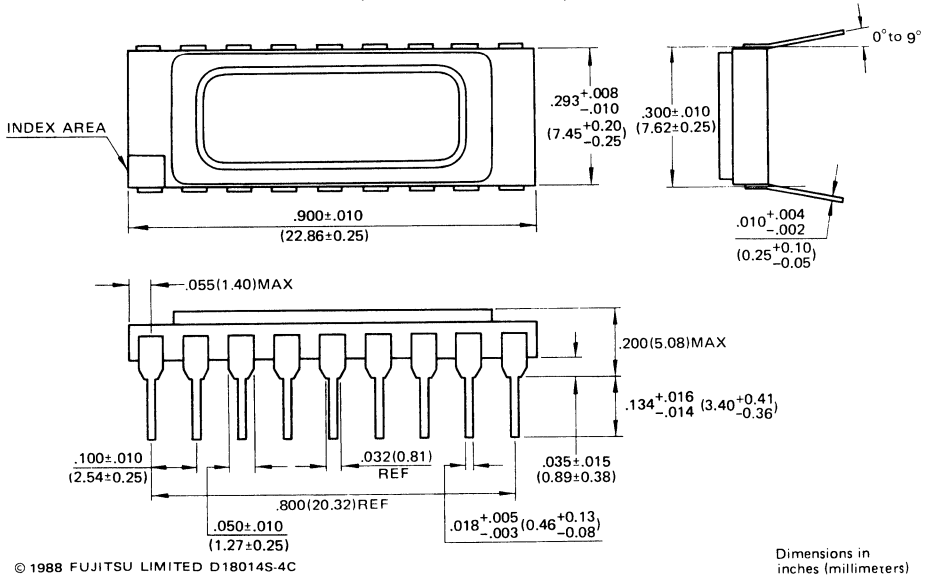


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



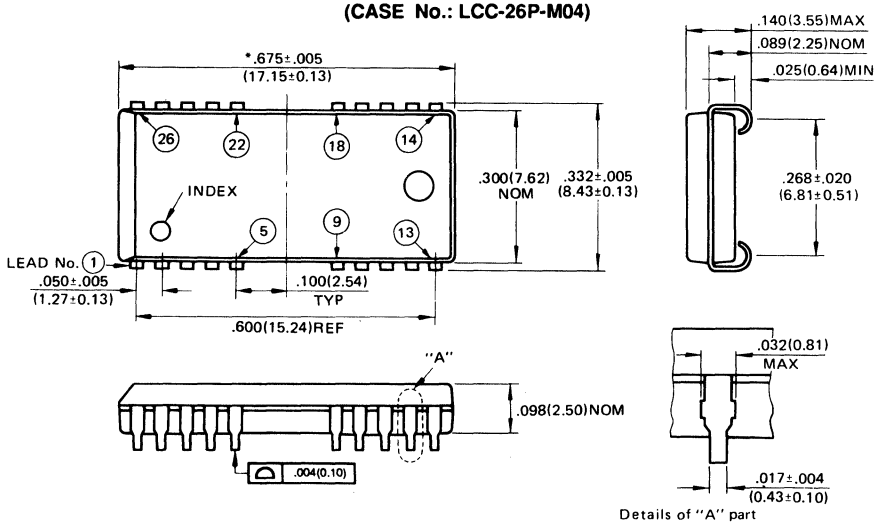
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



Details of "A" part

NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

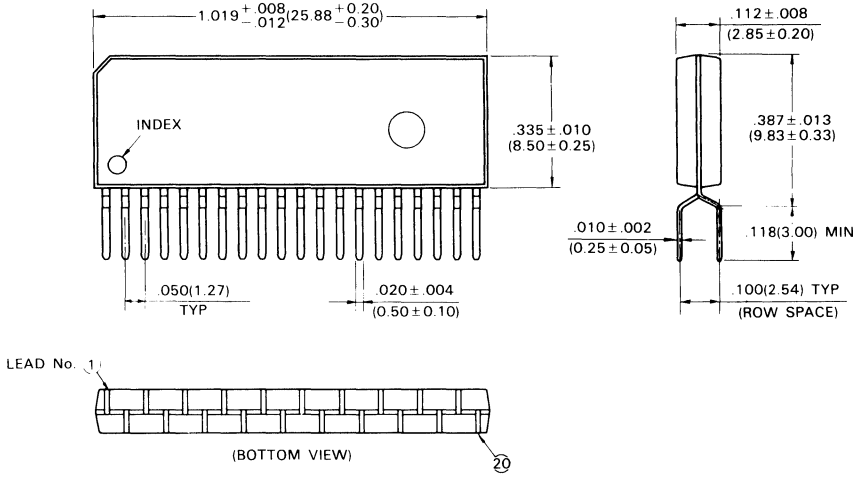
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

2

2

February 1990
Edition 1.0

FUJITSU

DATA SHEET

MB81C1001-70L/-80L/-10L/-12L

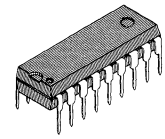
CMOS 1,048,576 BIT NIBBLE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Nibble Mode DRAM

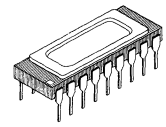
The Fujitsu MB81C1001 is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001 has been designed for mainframe memories, buffer memories, and peripheral storage and memory systems of battery operated computers requiring very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1001 high α-ray soft error immunity and extended refresh time. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

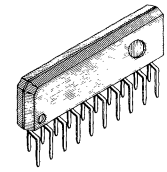


DIP-18P-M04



DIP-18C-A01

LCC-26P-M04



ZIP-20P-M02

Features

Parameter	MB81C1001 -70L	MB81C1001 -80L	MB81C1001 -10L	MB81C1001 -12L
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Nibble Mode Cycle Time	50 ns min.	50 ns min.	55 ns min.	60 ns min.
Low Power Dissipation • Operating Current	396 mW max.	358 mW max.	303 mW max.	259 mW max.
• Standby Current	8.3 mW max. (TTL level)/1.4 mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 64 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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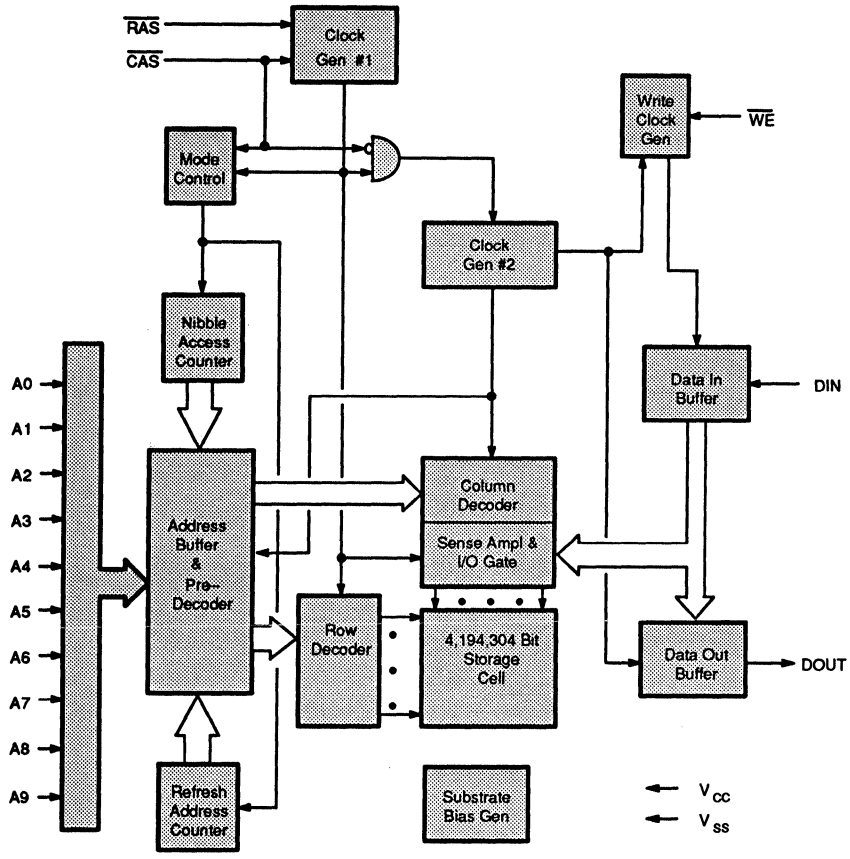
Fig. 1 – MB81C1001 DYNAMIC RAM – BLOCK DIAGRAM

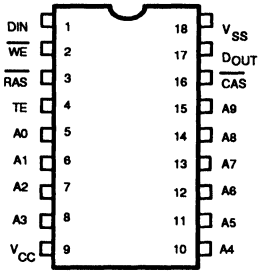


CAPACITANCE (T_A = 25°C, f = 1MHz)

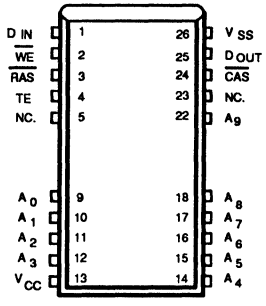
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

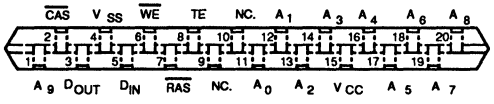
18-Pin DIP:
(TOP VIEW)



26-Pin SOJ:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

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DATA INPUT

Data is written into the MB81C1001 during write or read–modify–write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current)	MB81C1001–70L	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	72	mA
	MB81C1001–80L					65	
	MB81C1001–10L					55	
	MB81C1001–12L					47	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	1.5	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			250	µA
Refresh current #1 (Average power supply current)	MB81C1001–70L	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	60	mA
	MB81C1001–80L					56	
	MB81C1001–10L					50	
	MB81C1001–12L					45	
Nibble Mode current	MB81C1001–70L	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{NC} = min	—	—	38	mA
	MB81C1001–80L					38	
	MB81C1001–10L					28	
	MB81C1001–12L					20	
Refresh current #2 (Average power supply current)	MB81C1001–70L	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	60	mA
	MB81C1001–80L					56	
	MB81C1001–10L					50	
	MB81C1001–12L					45	
Battery Back up current (Average power supply current)	MB81C1001–70L	ICC_6	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} =125 µs, t_{RAS} =min. to 1 µs, D_{OUT} =open. Other pin ≥ Vcc–0.2V or ≤0.2V	—	—	250	µA
	MB81C1001–80L						
	MB81C1001–10L						
	MB81C1001–12L						

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001-70L		MB81C1001-80L		MB81C1001-10L		MB81C1001-12L		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	64	—	64	—	64	—	64	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	167	—	182	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	25	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	75	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	25	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001-70L		MB81C1001-80L		MB81C1001-10L		MB81C1001-12L		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	70	—	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	25	—	25	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	43	—	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Nibble Mode Read/Write Cycle Time		t_{NC}	45	—	45	—	45	—	60	—	ns
51	Nibble Mode Read–Modify–Write Cycle Time		t_{NRWC}	67	—	67	—	70	—	85	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{NPA}	—	40	—	40	—	40	—	55	ns
53	Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	10	—	10	—	10	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{NCP} is long, t_{NPA} is longer than t_{NPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

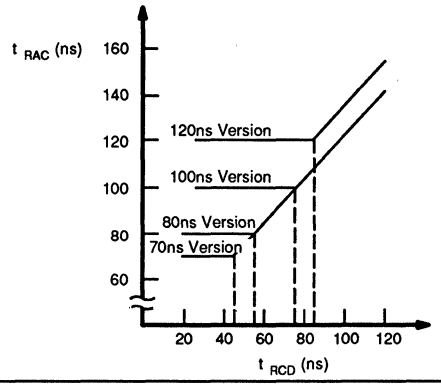
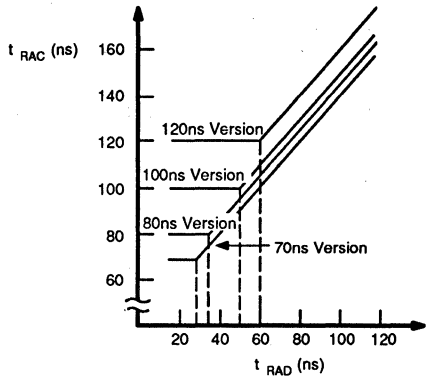


Fig. 3 – t_{RAC} vs. t_{RAD}



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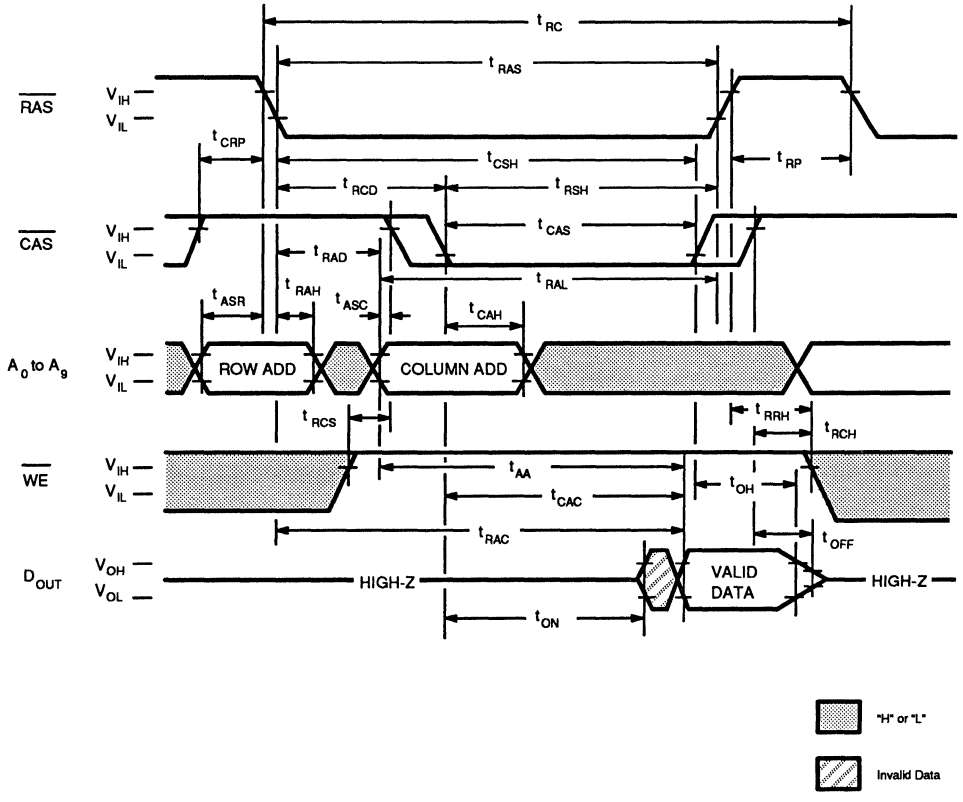
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X: "H" or "L"
*1: It is impossible in Nibble Mode.

Fig. 4 – READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

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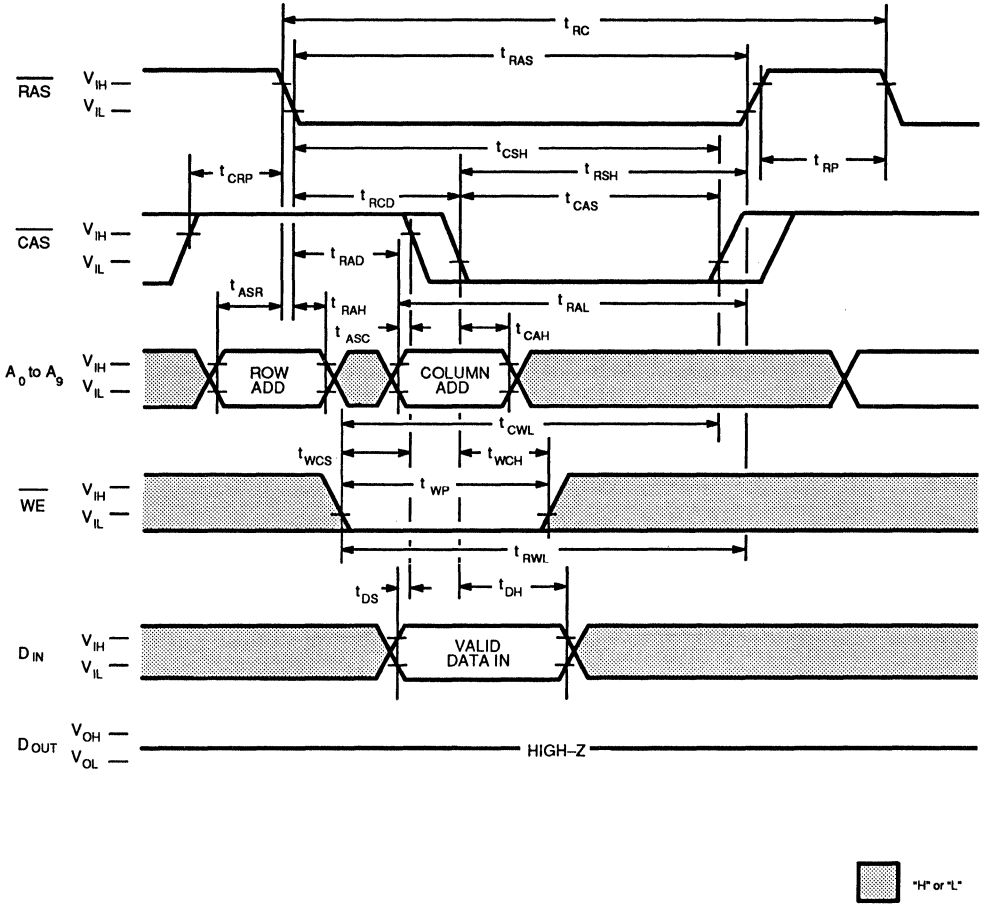
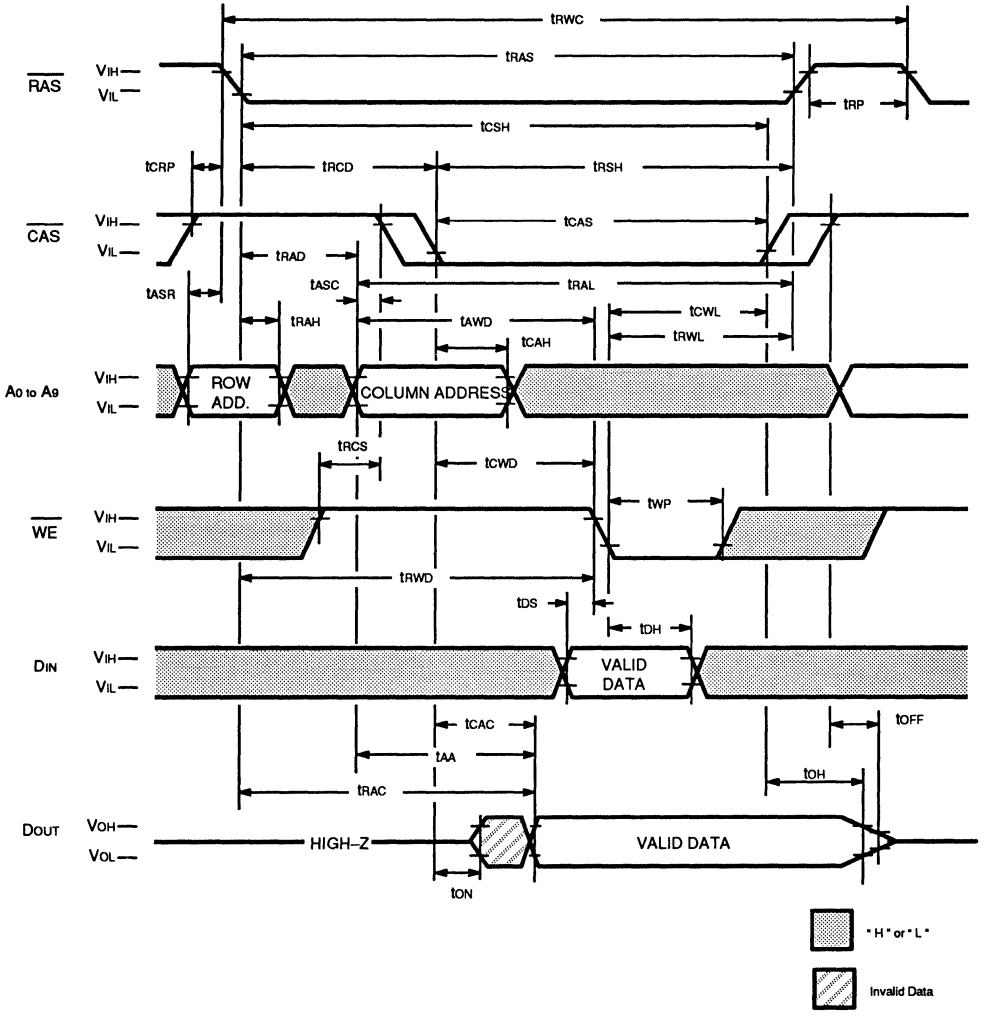
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin islatched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

Fig. 7 – NIBBLE MODE READ CYCLE

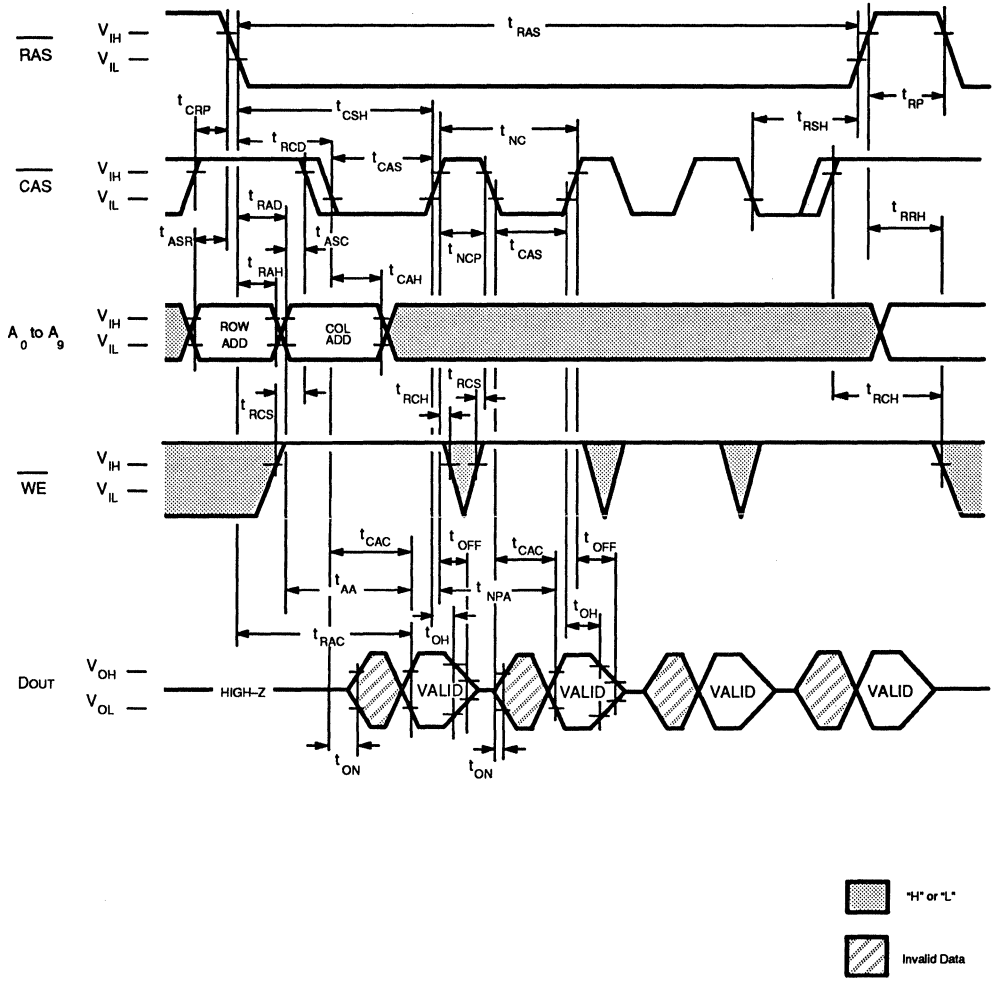
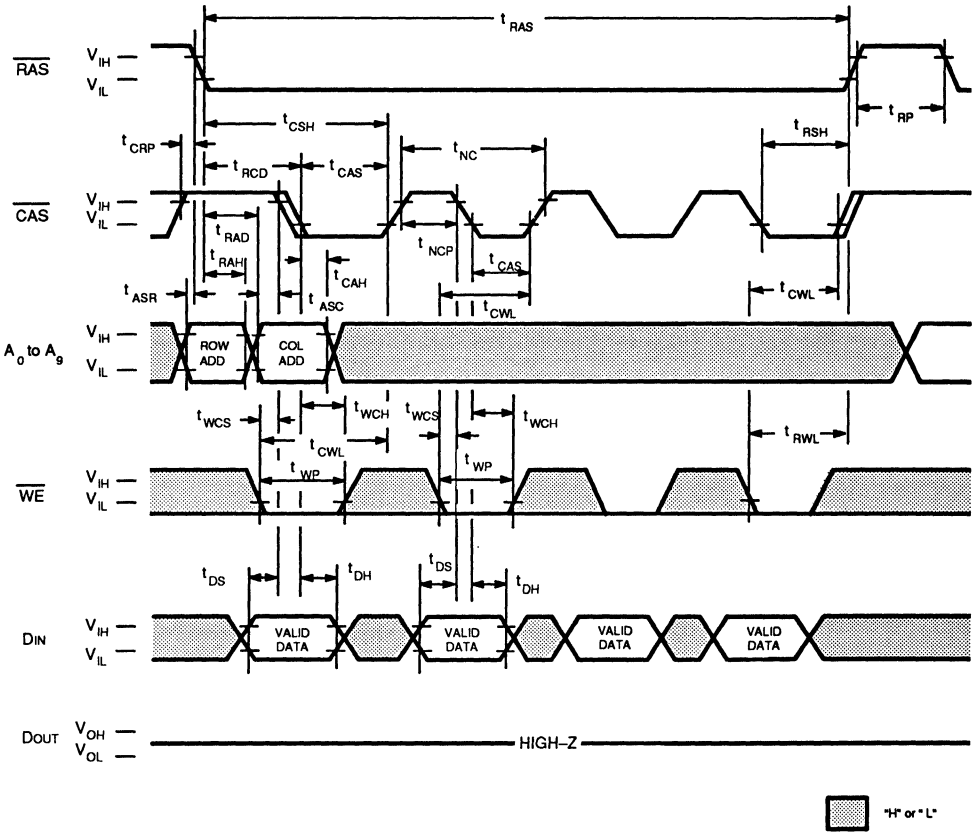


Fig. 8 – NIBBLE MODE WRITE CYCLE (Early Write)



2

Fig. 9 – NIBBLE MODE READ–MODIFY–WRITE CYCLE

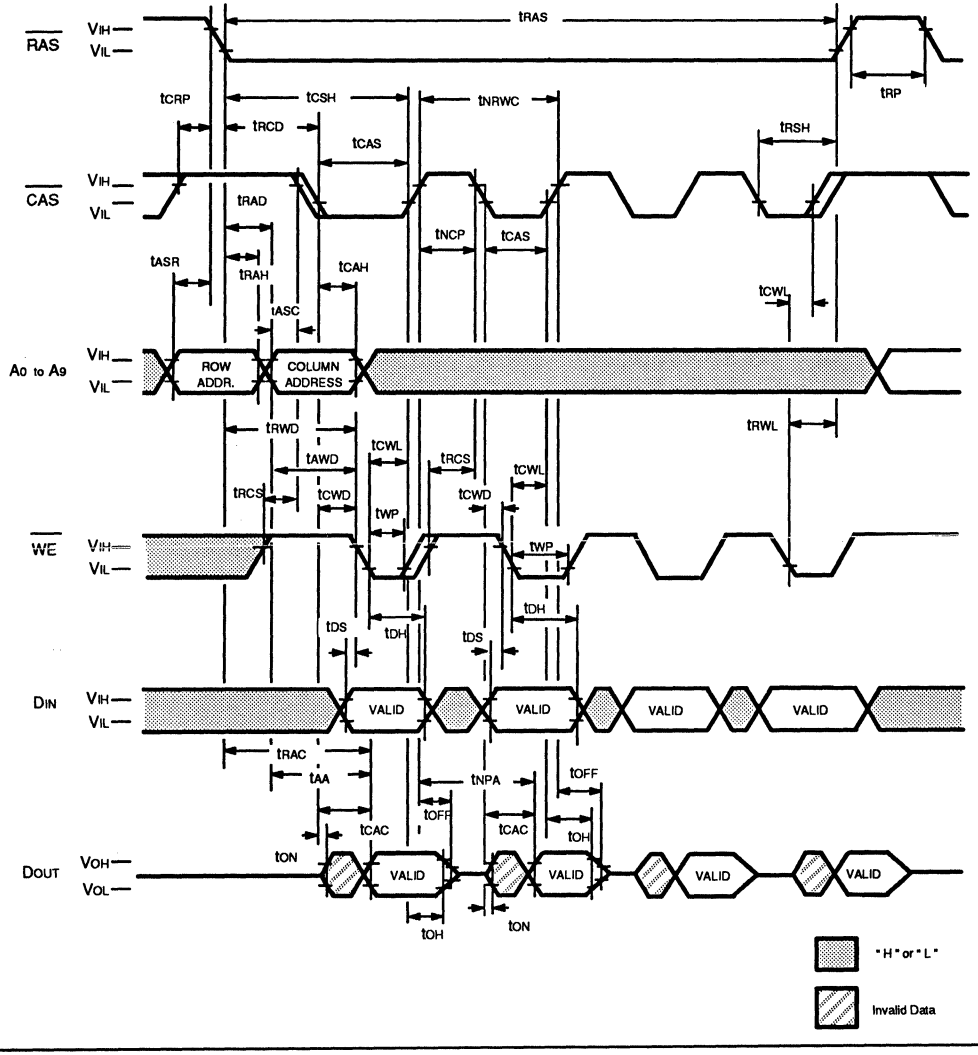
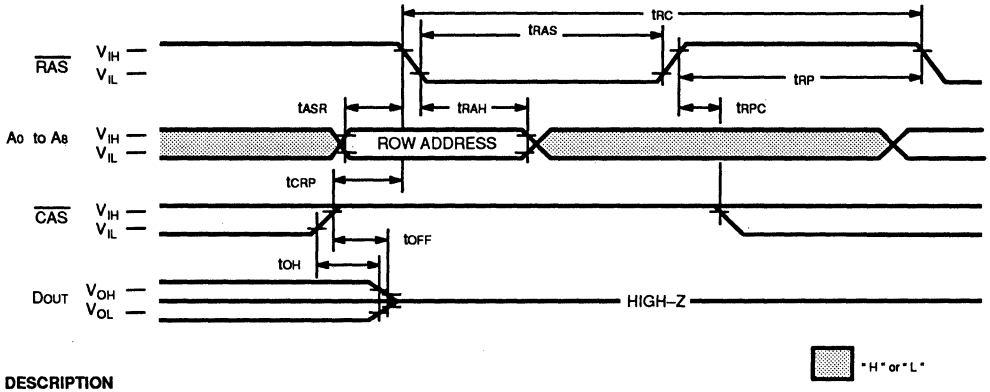


Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

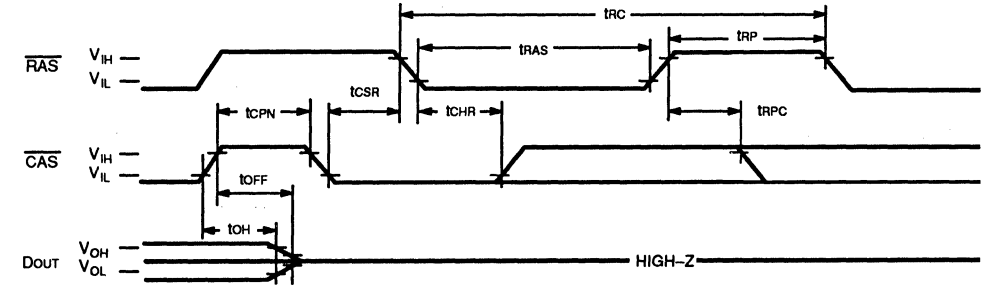


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 64–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "



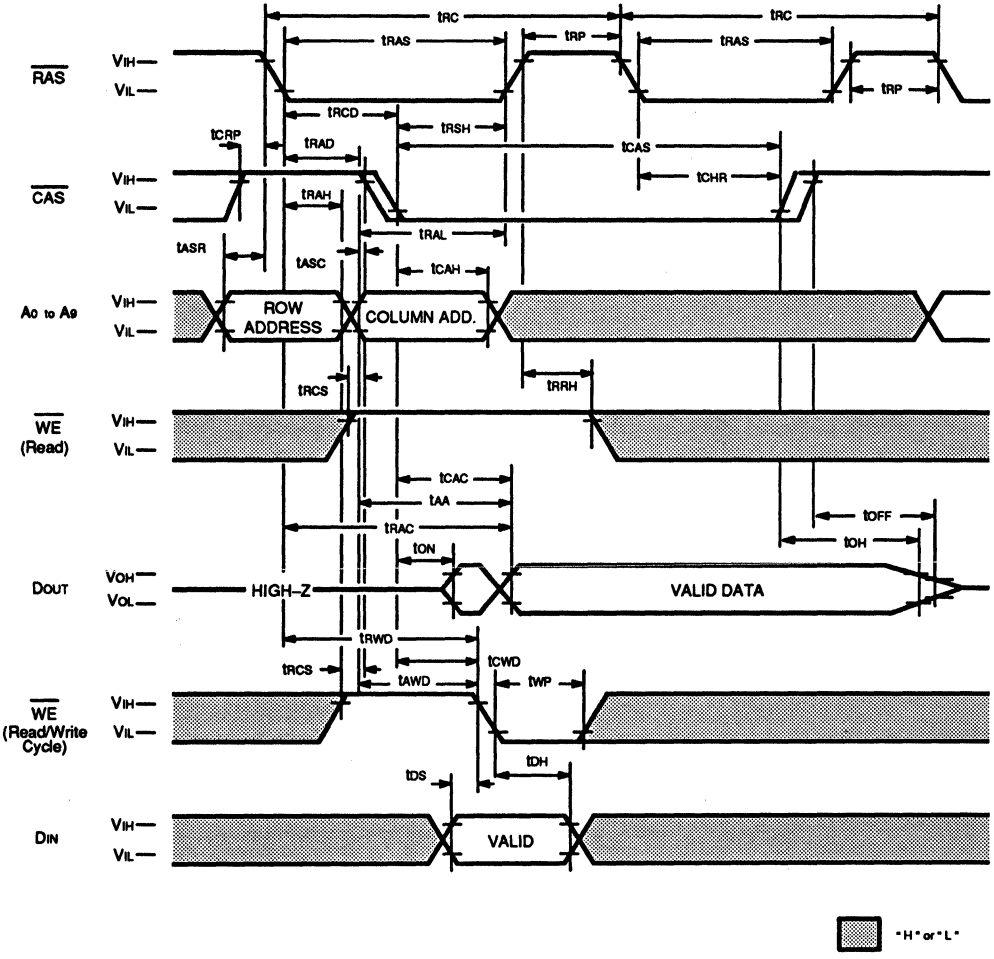
DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

2

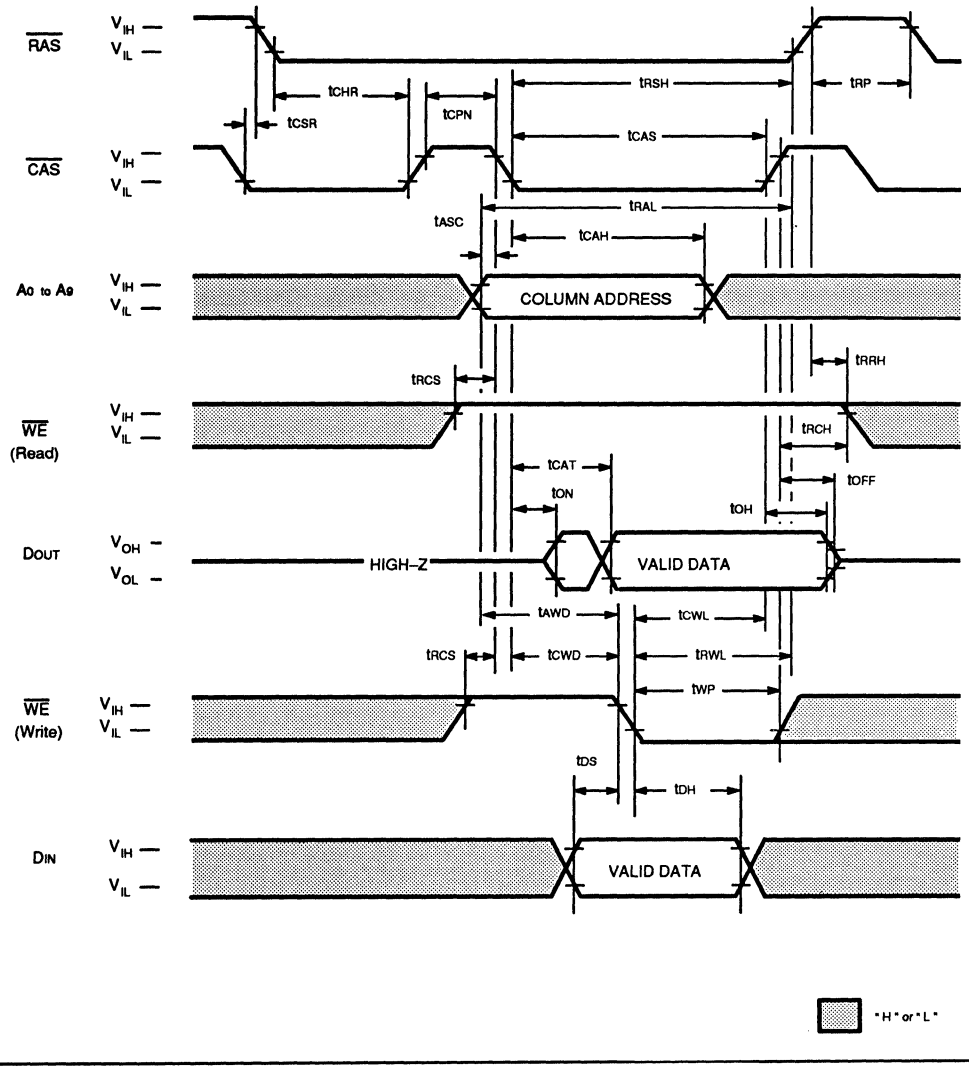
Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

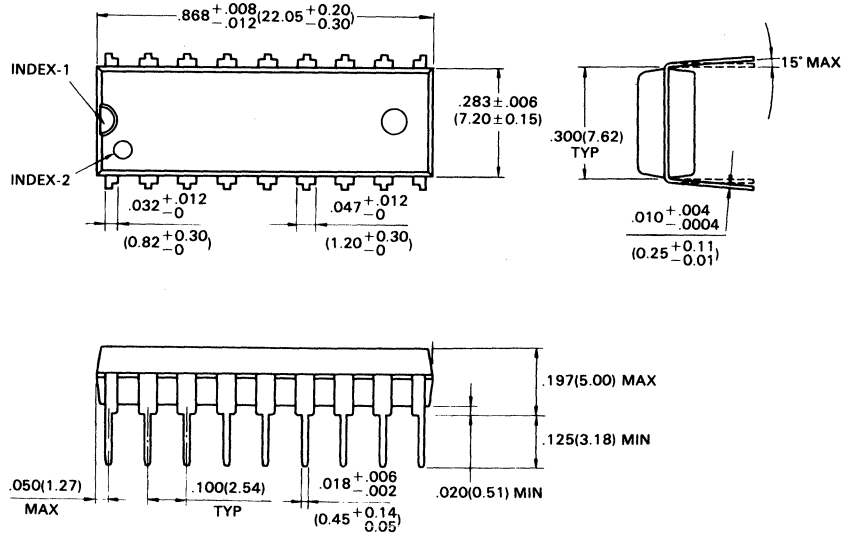


PACKAGE DIMENSIONS

(Suffix: –P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)



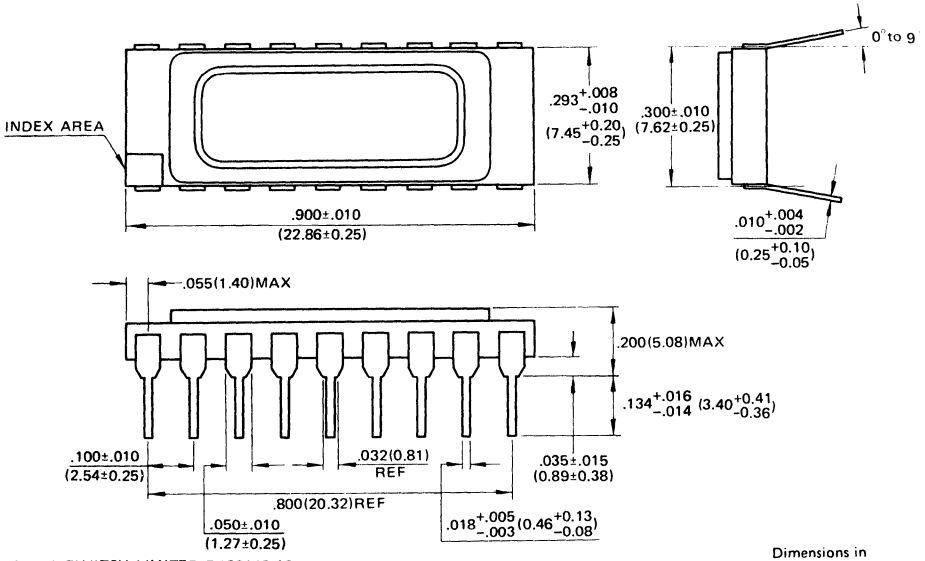
Dimensions in inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



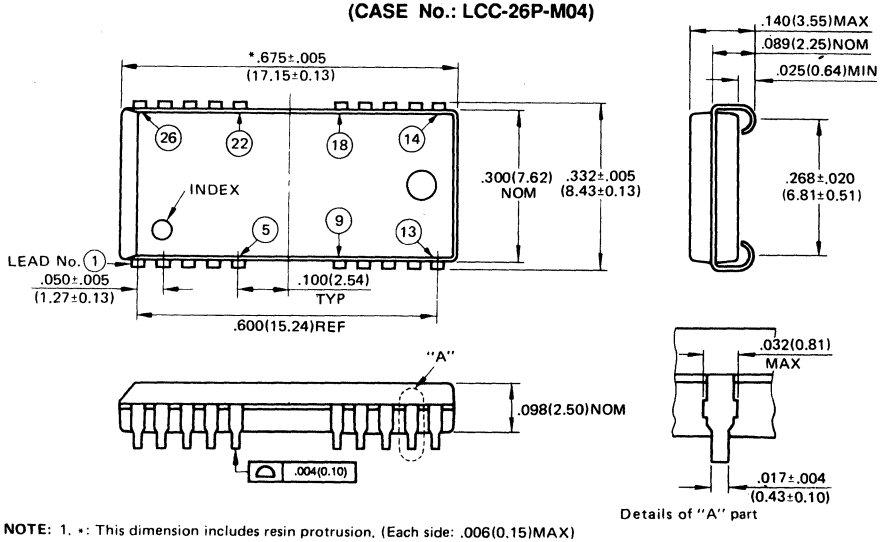
Dimensions in inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

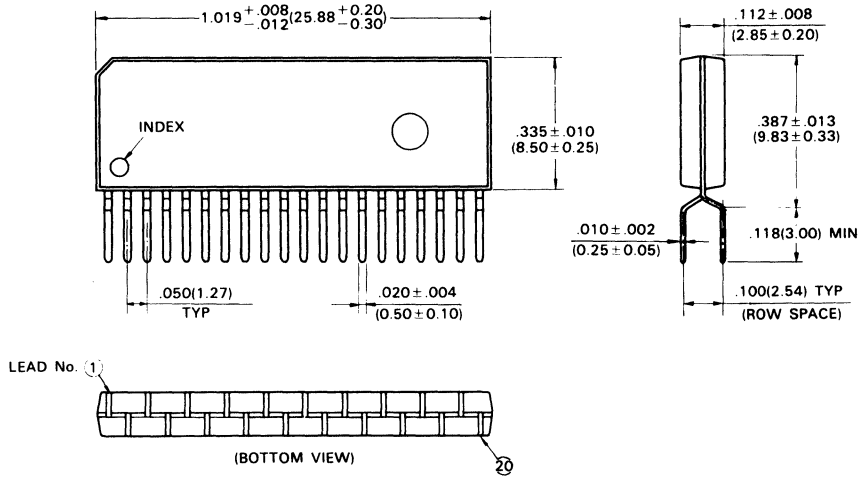
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

2

2

November 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C1001A-60/-70/-80/-10

CMOS 1,048,576 BIT NIBBLE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Nibble Mode DRAM

The Fujitsu MB81C1001A is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001A has been designed for mainframe memories, buffer memories, and peripheral storage applications requiring high speed, low power dissipation, or compact layout.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1001A high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

Features

Parameter	MB81C1001A -60	MB81C1001A -70	MB81C1001A -80	MB81C1001A -10
$\overline{RAS}$ Access Time	60 ns max.	70 ns max.	80 ns max.	100 ns max.
Random Cycle Time	130 ns min.	140 ns min.	155 ns min.	180 ns min.
Address Access Time	30 ns max.	35 ns max.	40 ns max.	50 ns max.
$\overline{CAS}$ Access Time	15 ns max.	20 ns max.	20 ns max.	25 ns max.
Fast Page Mode Cycle Time	45 ns min.	40 ns min.	40 ns min.	45 ns min.
Low Power Dissipation • Operating Current	407 mW max.	374 mW max.	341 mW max.	297 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

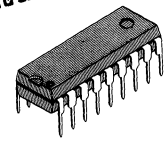
- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

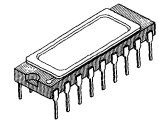
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

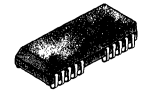
PRELIMINARY



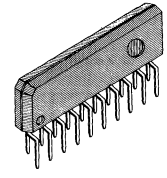
DIP–18P–M04



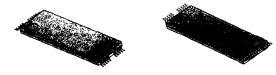
DIP–18C–A02



LCC–26P–M04



ZIP–20P–M02



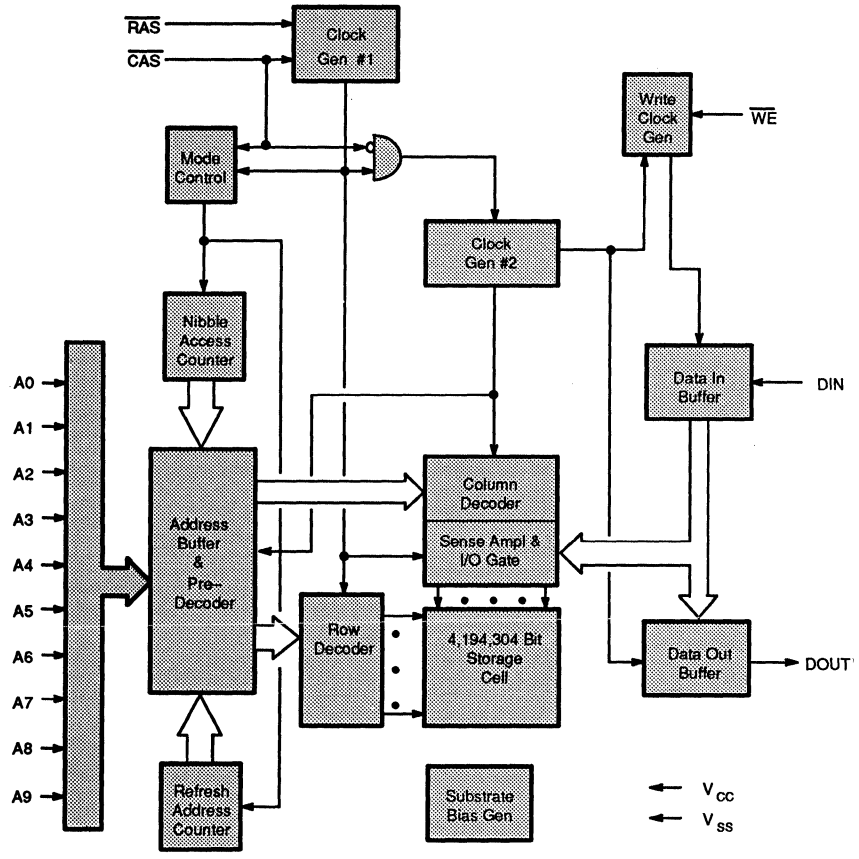
* FPT–24P–M04 / * FPT–24P–M05

* : Available for 70/80/100 ns versions

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

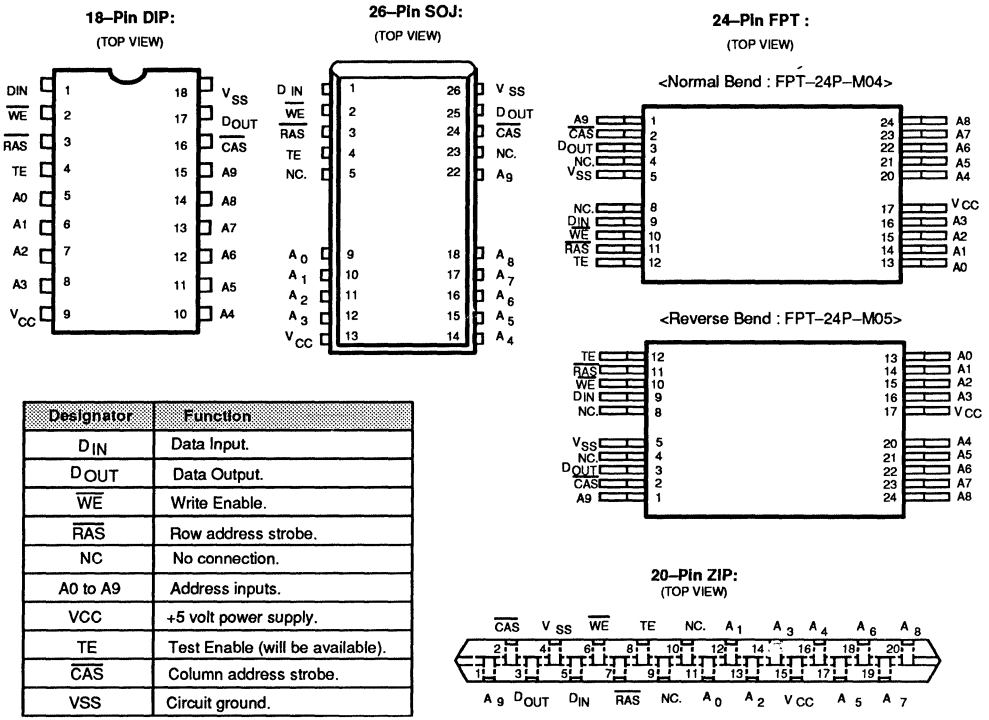
Fig. 1 – MB81C1001A DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Data is written into the MB81C1001A during write or read–modify–write cycle. The inputdata is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current)	MB81C1001A–60	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	74	mA
	MB81C1001A–70					68	
	MB81C1001A–80					62	
	MB81C1001A–10					54	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			1.0	
Refresh current #1 (Average power supply current)	MB81C1001A–60	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	74	mA
	MB81C1001A–70					68	
	MB81C1001A–80					62	
	MB81C1001A–10					54	
Nibble Mode current	MB81C1001A–60	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{NC} = min	—	—	60	mA
	MB81C1001A–70					55	
	MB81C1001A–80					50	
	MB81C1001A–10					43	
Refresh current #2 (Average power supply current)	MB81C1001A–60	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	74	mA
	MB81C1001A–70					68	
	MB81C1001A–80					62	
	MB81C1001A–10					54	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001A-60		MB81C1001A-70		MB81C1001A-80		MB81C1001A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	130	—	140	—	155	—	180	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	160	—	180	—	210	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	60	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	15	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	0	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	0	—	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	—	20	—	25	ns
10	Transition Time		t_T	2	50	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	60	—	65	—	70	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	20	50	22	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	20	—	20	—	20	—	20	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	12	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	17	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time		t_{WCH}	10	—	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	12	—	12	—	15	—	20	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001A-60		MB81C1001A-70		MB81C1001A-80		MB81C1001A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	60	—	70	—	80	—	100	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	15	—	20	—	20	—	25	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	30	—	35	—	40	—	50	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	12	—	15	—	ns
50	Nibble Mode Read/Write Cycle Time		t_{NC}	35	—	40	—	40	—	45	—	ns
51	Nibble Mode Read–Modify–Write Cycle Time		t_{NRWC}	52	—	60	—	60	—	70	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{NPA}	—	30	—	35	—	35	—	40	ns
53	Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	10	—	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{NCP} is long, t_{NPA} is longer than t_{NPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

2

Fig. 2 – t_{RAC} vs. t_{RCD}

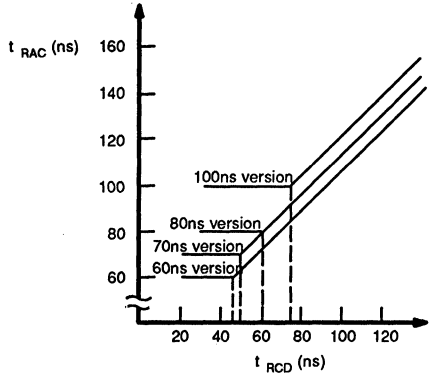
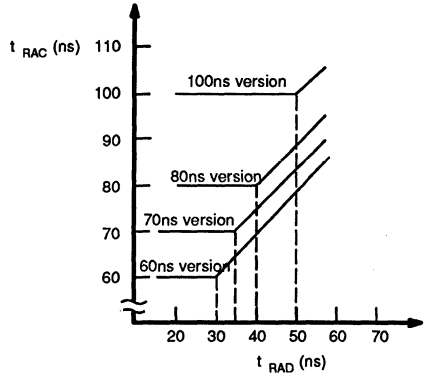


Fig. 3 – t_{RAC} vs. t_{RAD}



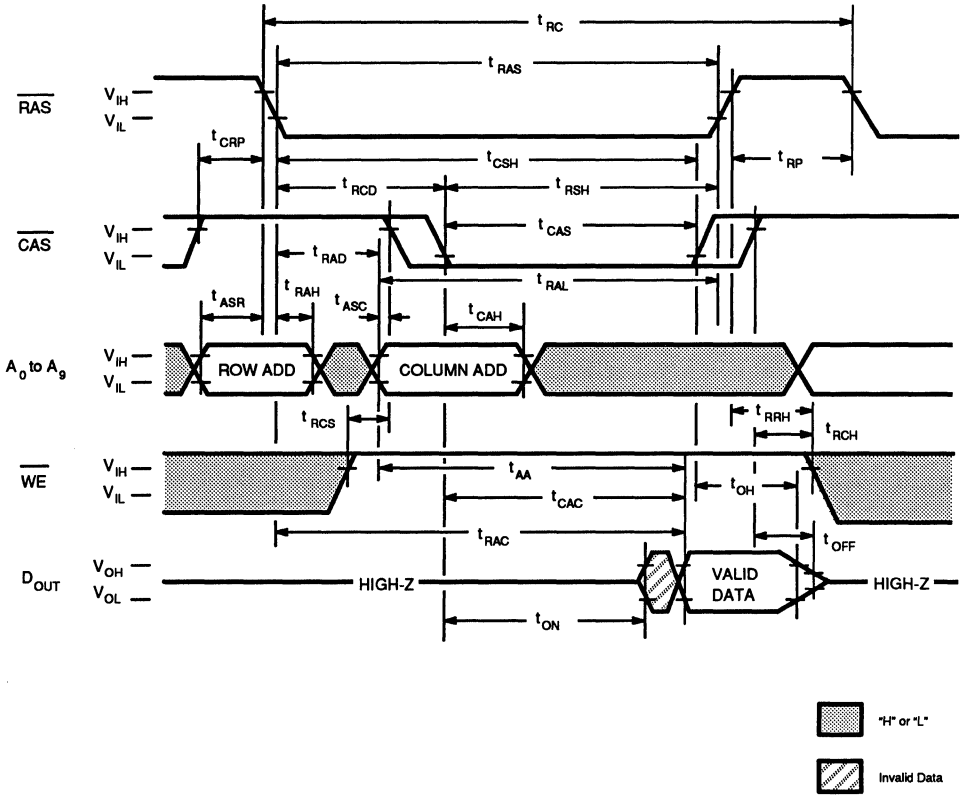
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Nibble Mode.

Fig. 4 – READ CYCLE

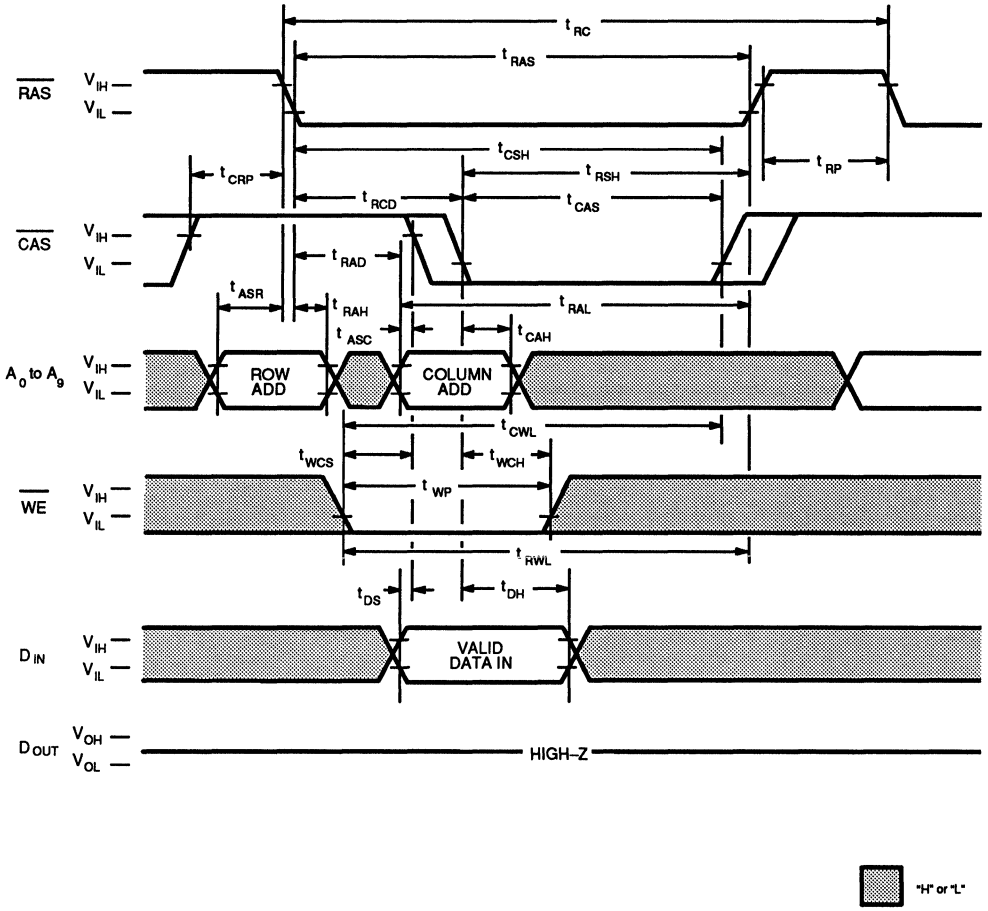


DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

2

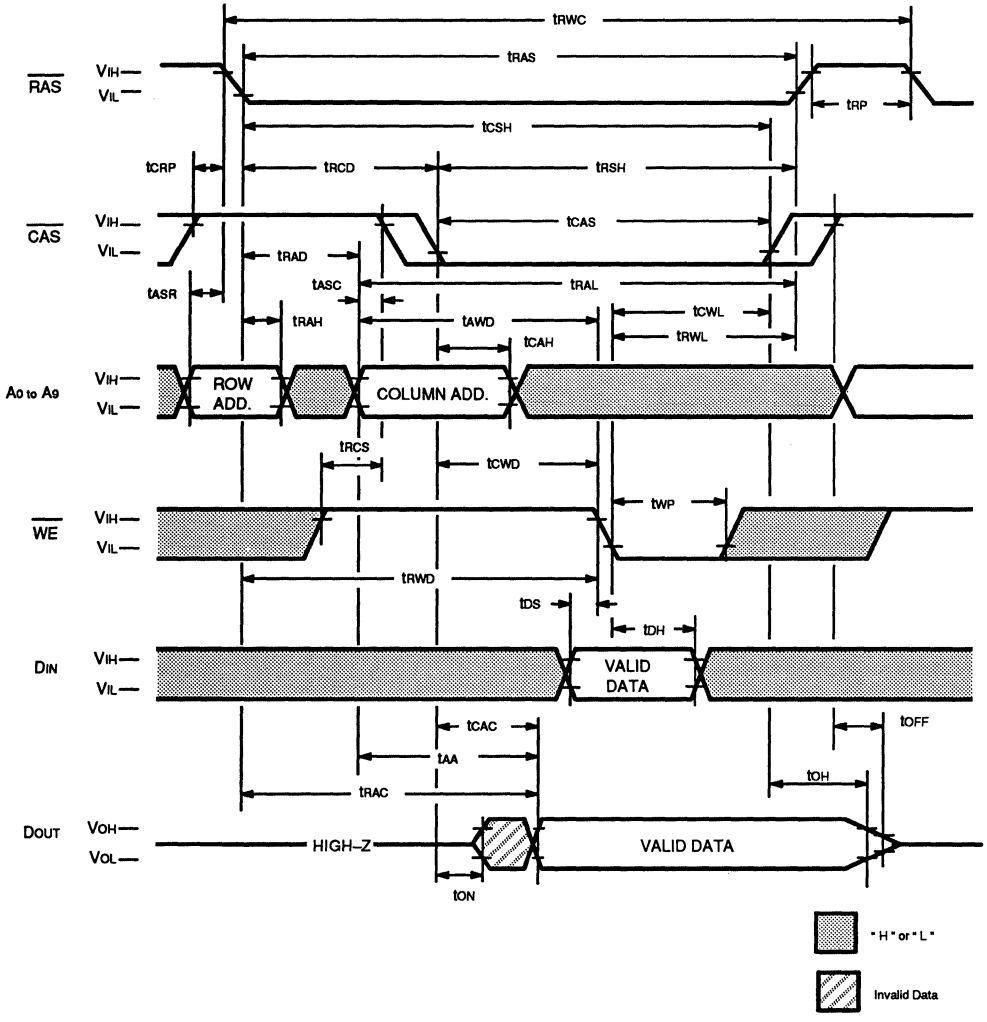
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin islatched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

Fig. 7 – NIBBLE MODE READ CYCLE

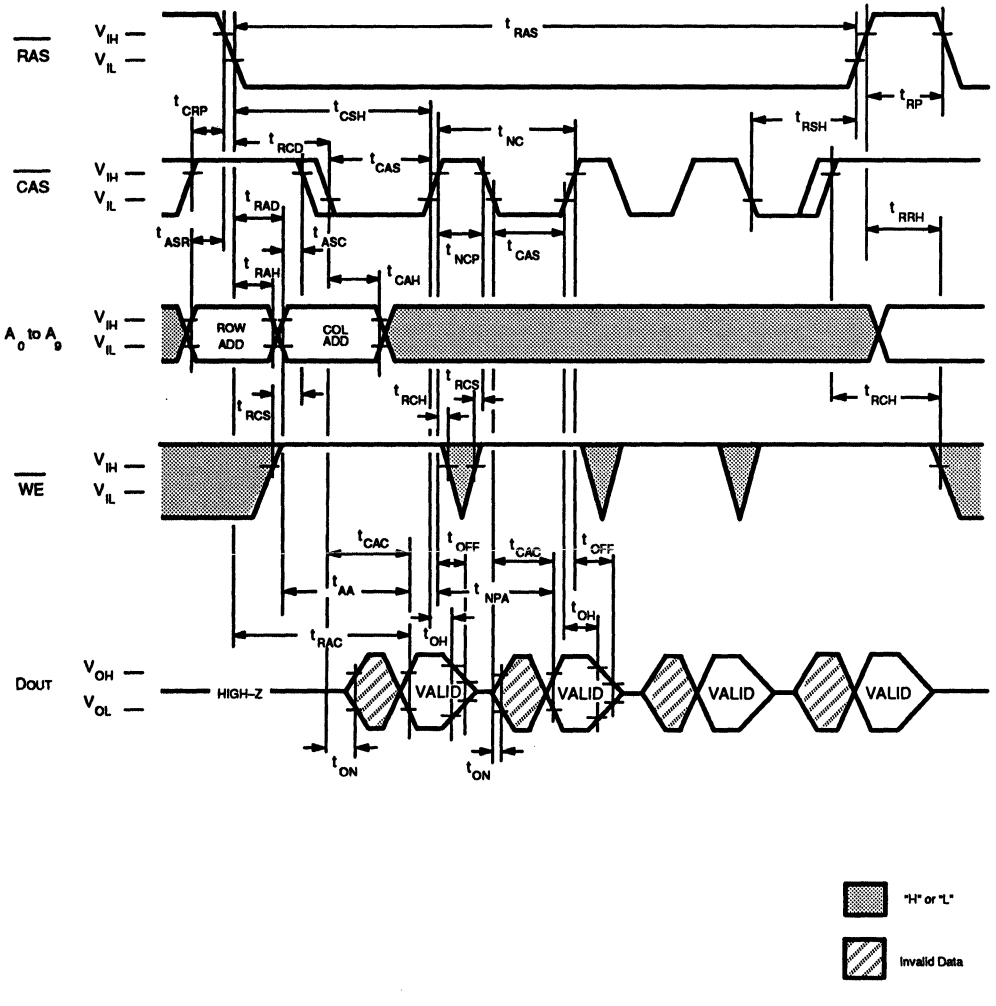
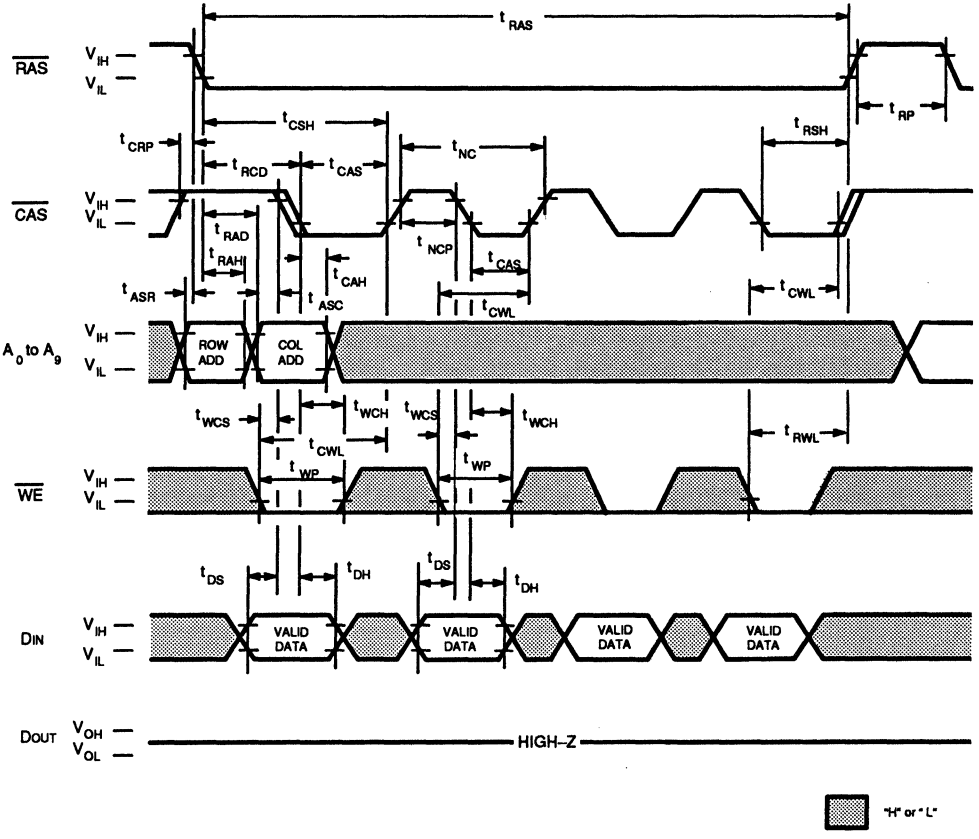


Fig. 8 – NIBBLE MODE WRITE CYCLE (Early Write)



2

Fig. 9 – NIBBLE MODE READ–MODIFY–WRITE CYCLE

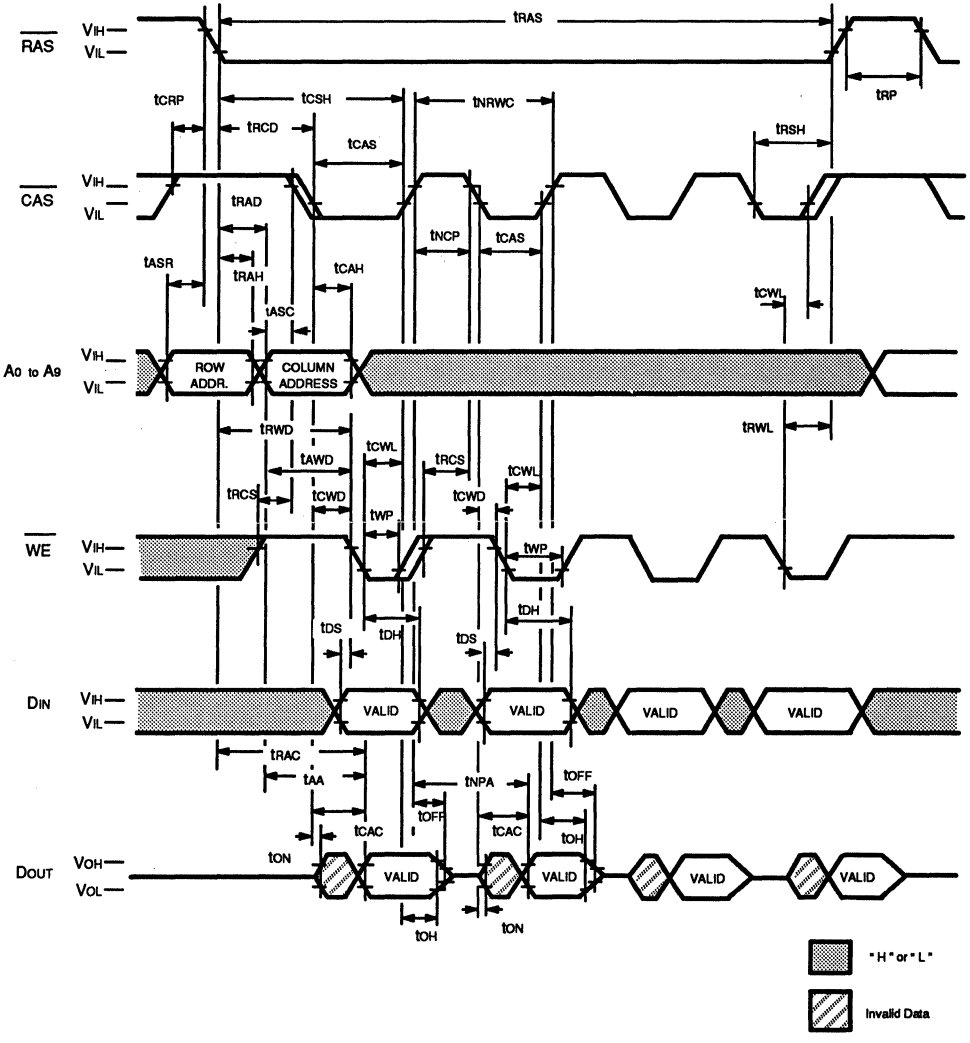
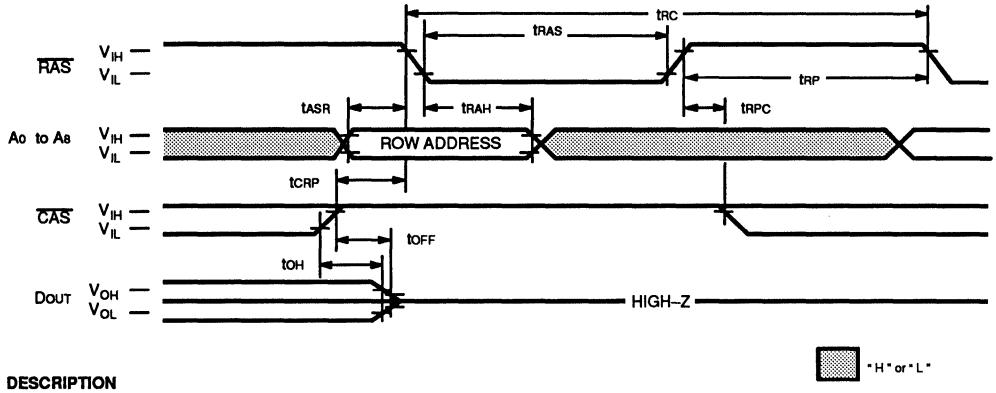


Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

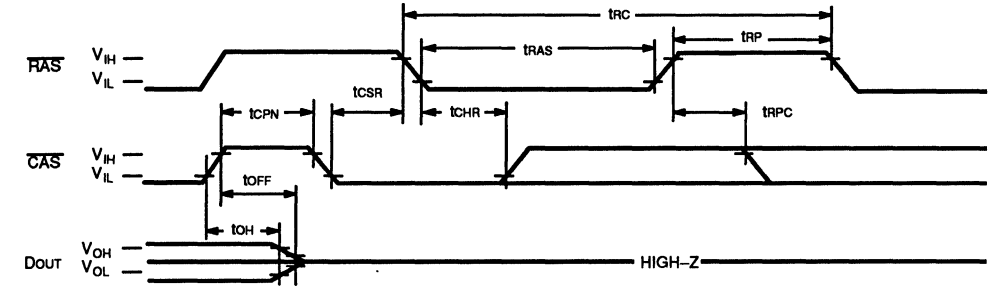


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "



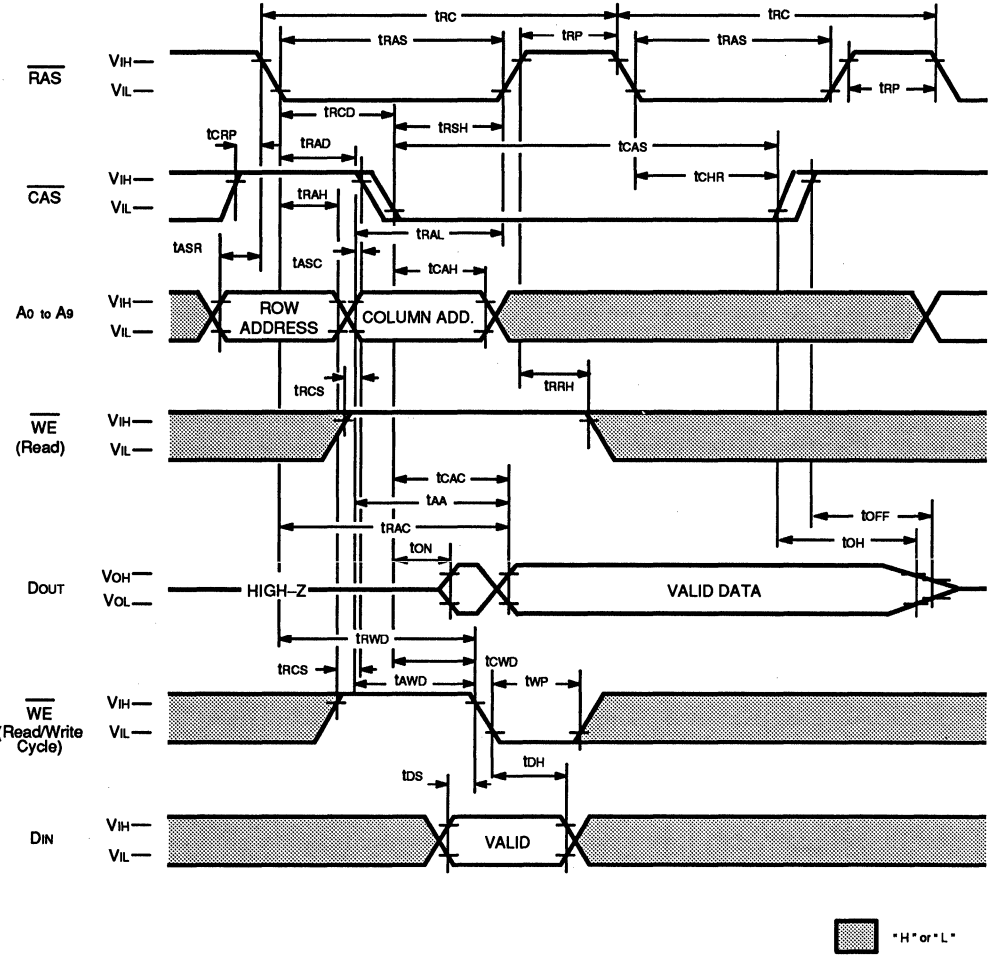
DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

2

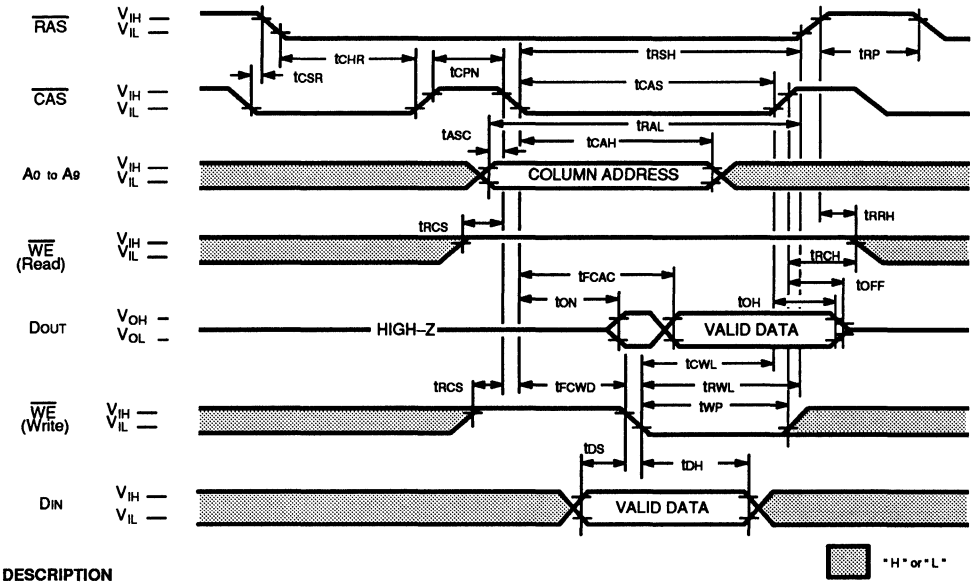
Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter. The bit A9 is set high internally.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (read–modify–write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81C1001A–60		MB81C1001A–70		MB81C1001A–80		MB81C1001A–10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	40	—	45	—	50	—	60	ns
91	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	40	—	45	—	50	—	60	—	ns

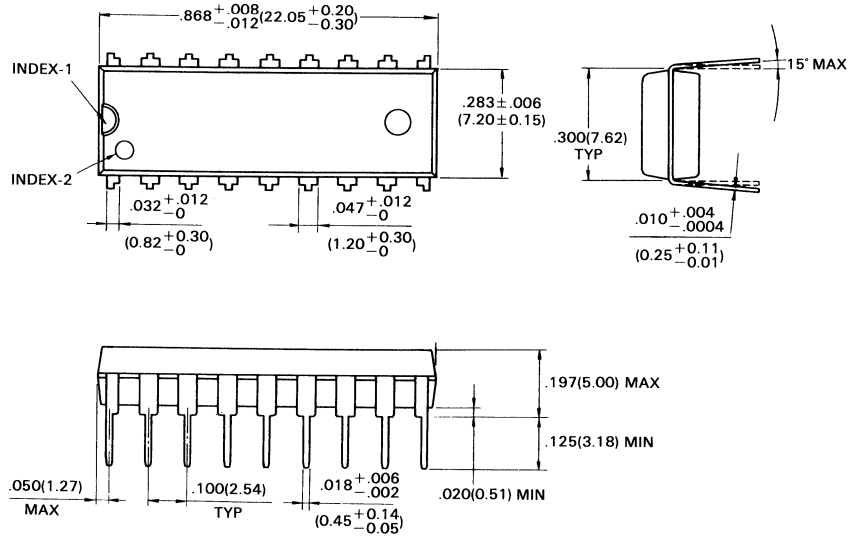
Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

2

PACKAGE DIMENSIONS

(Suffix: –P)

18–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–18P–M04)



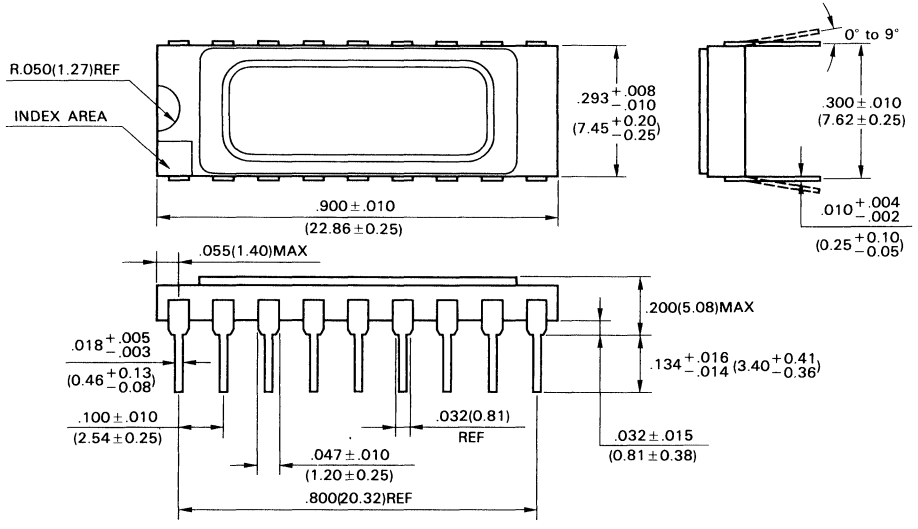
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18–LEAD CERAMIC (METAL SEAL) DUAL IN–LINE PACKAGE
(CASE No.: DIP–18C–A02)



Dimensions in inches (millimeters).

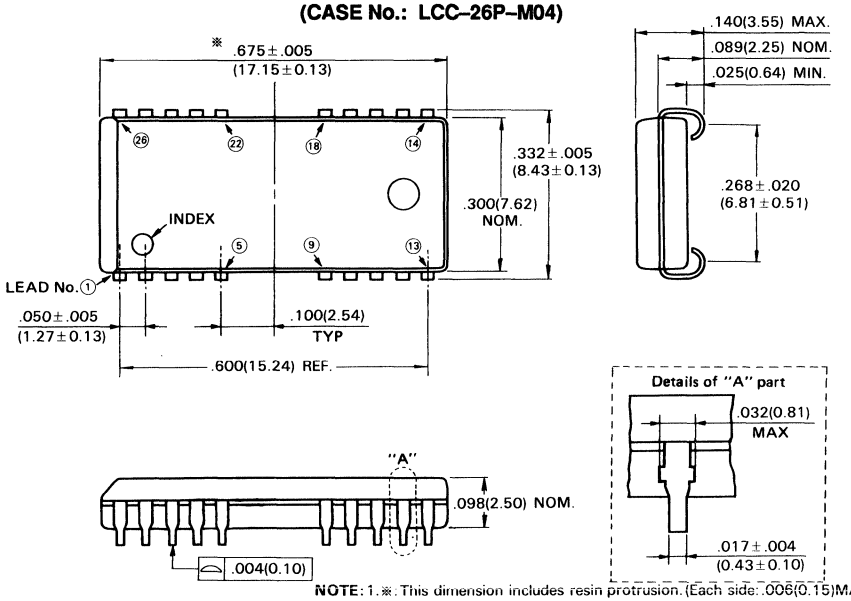
2

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)

(CASE No.: LCC–26P–M04)

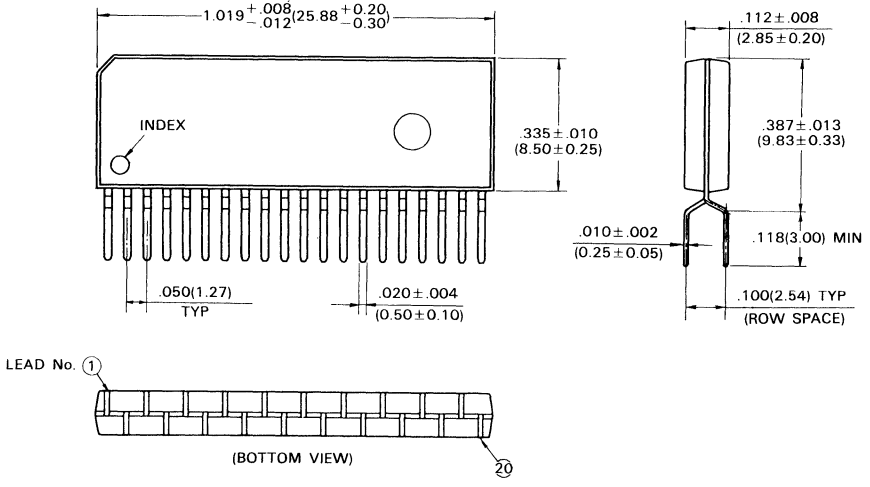


NOTE: 1. ※: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
3. Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20–LEAD PLASTIC ZIGZAG–IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



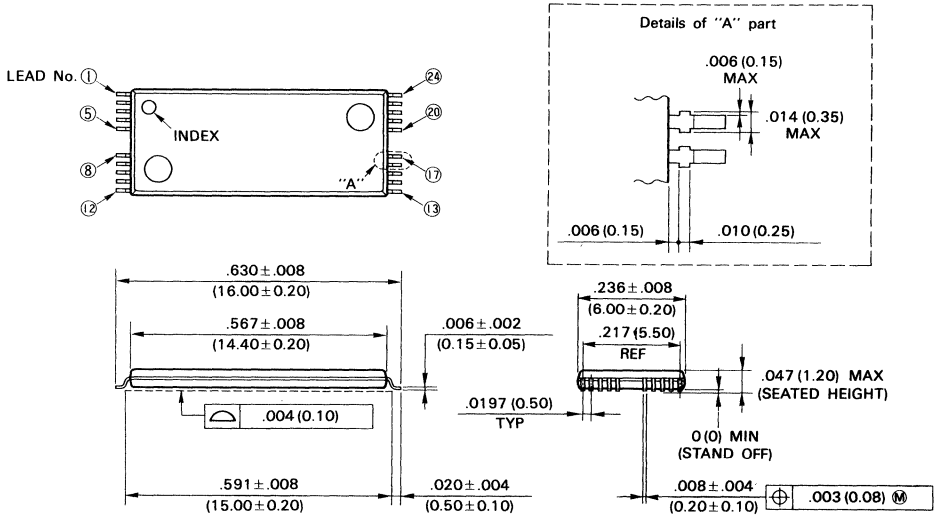
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M04)

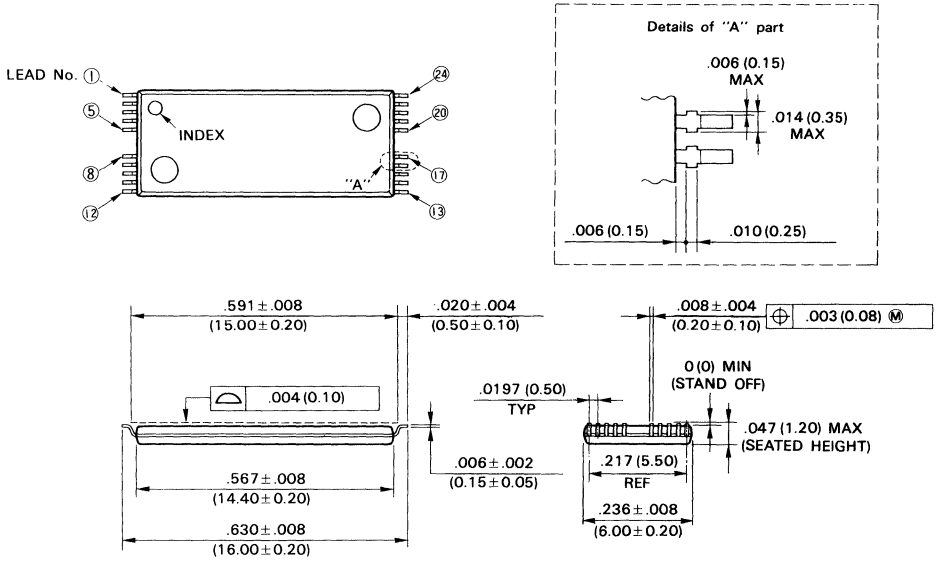


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PFTR)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M05)



Dimensions in inches (millimeters)

2

2

November 1990
Edition 2.0

FUJITSU

DATA SHEET

MB81C1001A-70L/-80L/-10L

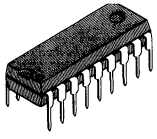
CMOS 1,048,576 BIT NIBBLE MODE DYNAMIC RAM

CMOS 1M x 1 Bit Nibble Mode DRAM

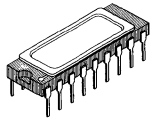
The Fujitsu MB81C1001A is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001A has been designed for mainframe memories, buffer memories, and peripheral storage applications requiring high speed, low power dissipation, or compact layout.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1001A high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

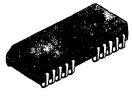
PRELIMINARY



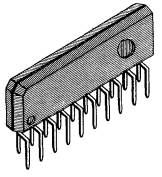
DIP-18P-M04



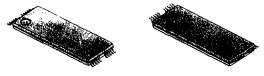
DIP-18C-A02



LCC-26P-M04



ZIP-20P-M02



FPT-24P-M04 / FPT-24P-M05

Features

Parameter	MB81C1001A -70L	MB81C1001A -80L	MB81C1001A -10L
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.
Address Access Time	35 ns max.	40 ns max.	50 ns max.
$\overline{CAS}$ Access Time	20 ns max.	20 ns max.	25 ns max.
Fast Page Mode Cycle Time	40 ns min.	40 ns min.	45 ns min.
Low Power Dissipation • Operating Current	374 mW max.	341 mW max.	297 mW max.
• Standby Current	5.5 mW max. (TTL level)/1.4 mW max. (CMOS level)		

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

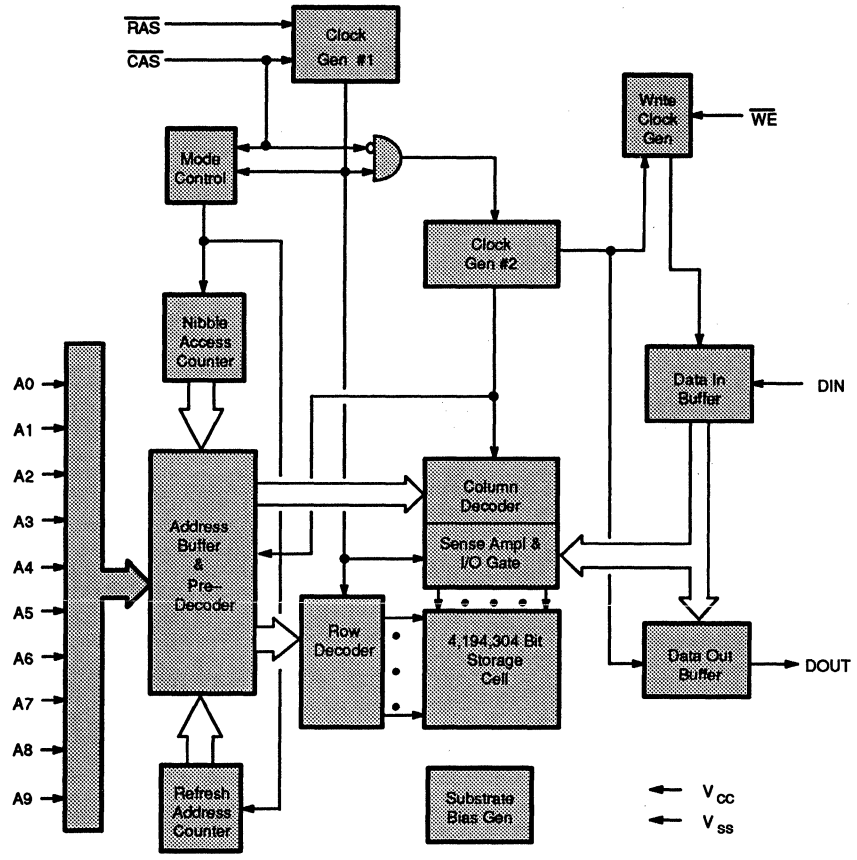
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

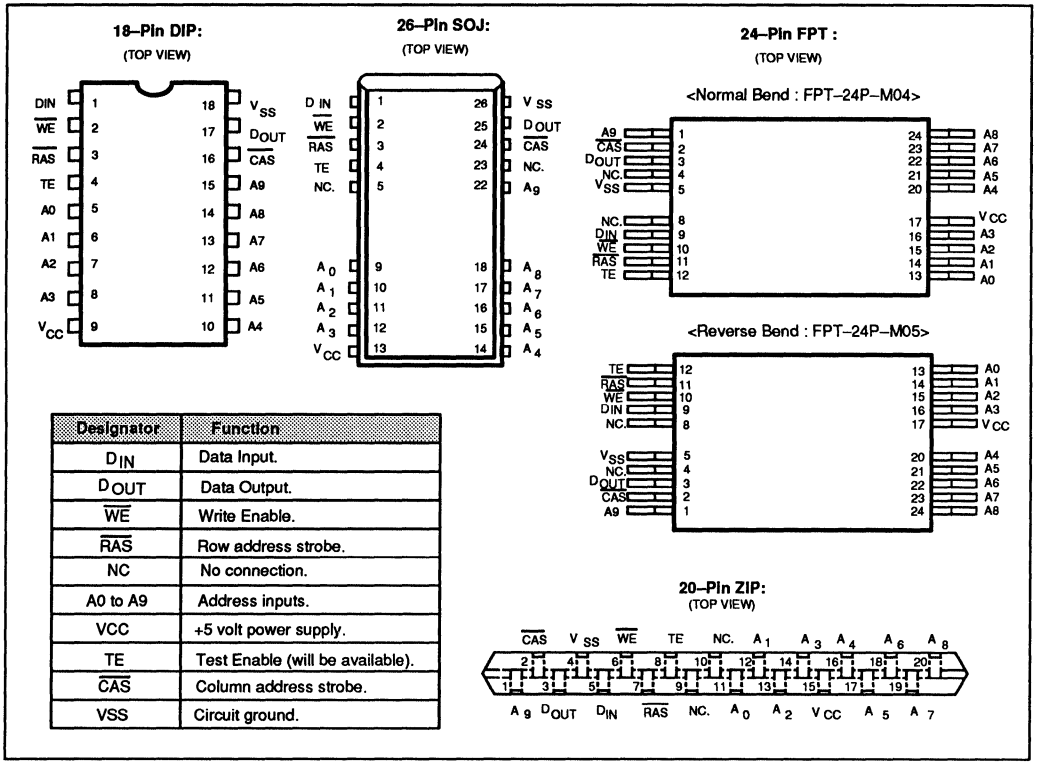
Fig. 1 – MB81C1001A DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Data is written into the MB81C1001A during write or read–modify–write cycle. The inputdata is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current)	MB81C1001A–70L	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	68	mA
	MB81C1001A–80L					62	
	MB81C1001A–10L					54	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	1.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			0.25	
Refresh current #1 (Average power supply current)	MB81C1001A–70L	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	68	mA
	MB81C1001A–80L					62	
	MB81C1001A–10L					54	
Nibble Mode current	MB81C1001A–70L	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{NC} = min	—	—	55	mA
	MB81C1001A–80L					50	
	MB81C1001A–10L					43	
Refresh current #2 (Average power supply current)	MB81C1001A–70L	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	68	mA
	MB81C1001A–80L					62	
	MB81C1001A–10L					54	
Battery Back up current (Average power supply current)	MB81C1001A–70L	ICC_6	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} =125 µs, t_{RAS} =min. to 1 µs, D_{OUT} =open. Other pin ≥ Vcc–0.2V or ≤ 0.2V	—	—	250	µA
	MB81C1001A–80L						
	MB81C1001A–10L						

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001A -70L		MB81C1001A -80L		MB81C1001A -10L		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	64	—	64	—	64	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	160	—	180	—	210	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	20	—	25	ns
10	Transition Time		t_T	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	50	22	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	20	—	20	—	20	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	35	17	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		ns
29	Write Command Hold Time		t_{WCH}	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	12	—	15	—	20	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001A -70L		MB81C1001A -80L		MB81C1001A -10L		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	70	—	80	—	100	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	20	—	20	—	25	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	35	—	40	—	50	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	10	—	12	—	15	—	ns
50	Nibble Mode Read/Write Cycle Time		t_{NC}	40	—	40	—	45	—	ns
51	Nibble Mode Read–Modify–Write Cycle Time		t_{NRWC}	60	—	60	—	70	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{NPA}	—	35	—	35	—	40	ns
53	Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200μs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{NCP} is long, t_{NPA} is longer than t_{NPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

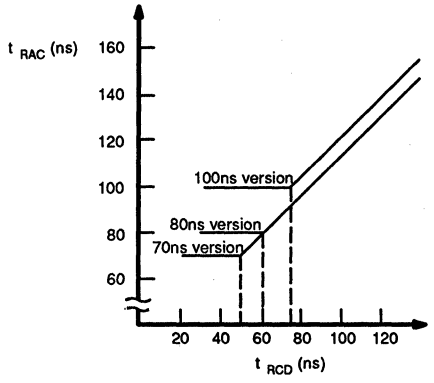
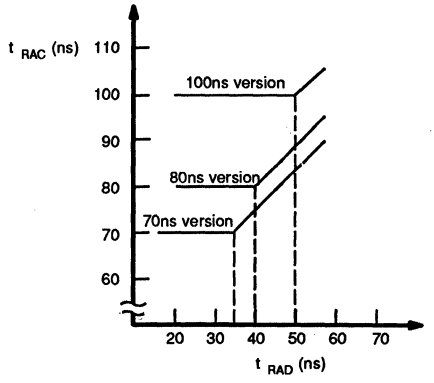


Fig. 3 – t_{RAC} vs. t_{RAD}



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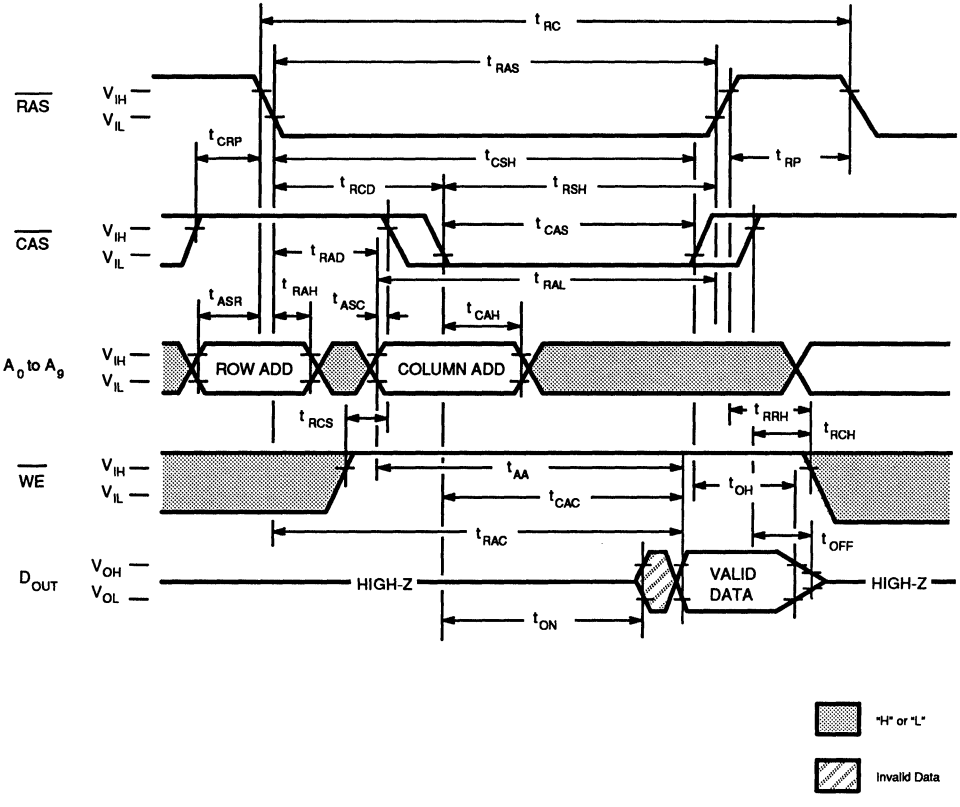
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Nibble Mode.

Fig. 4 – READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

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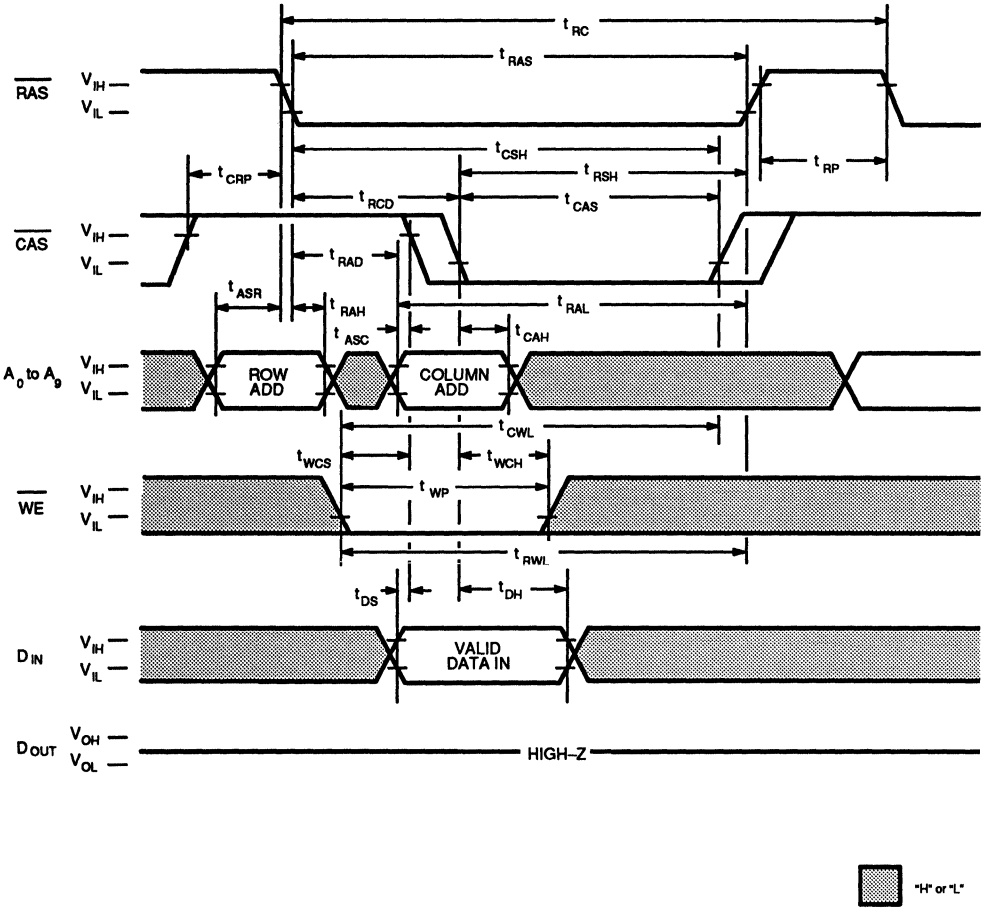
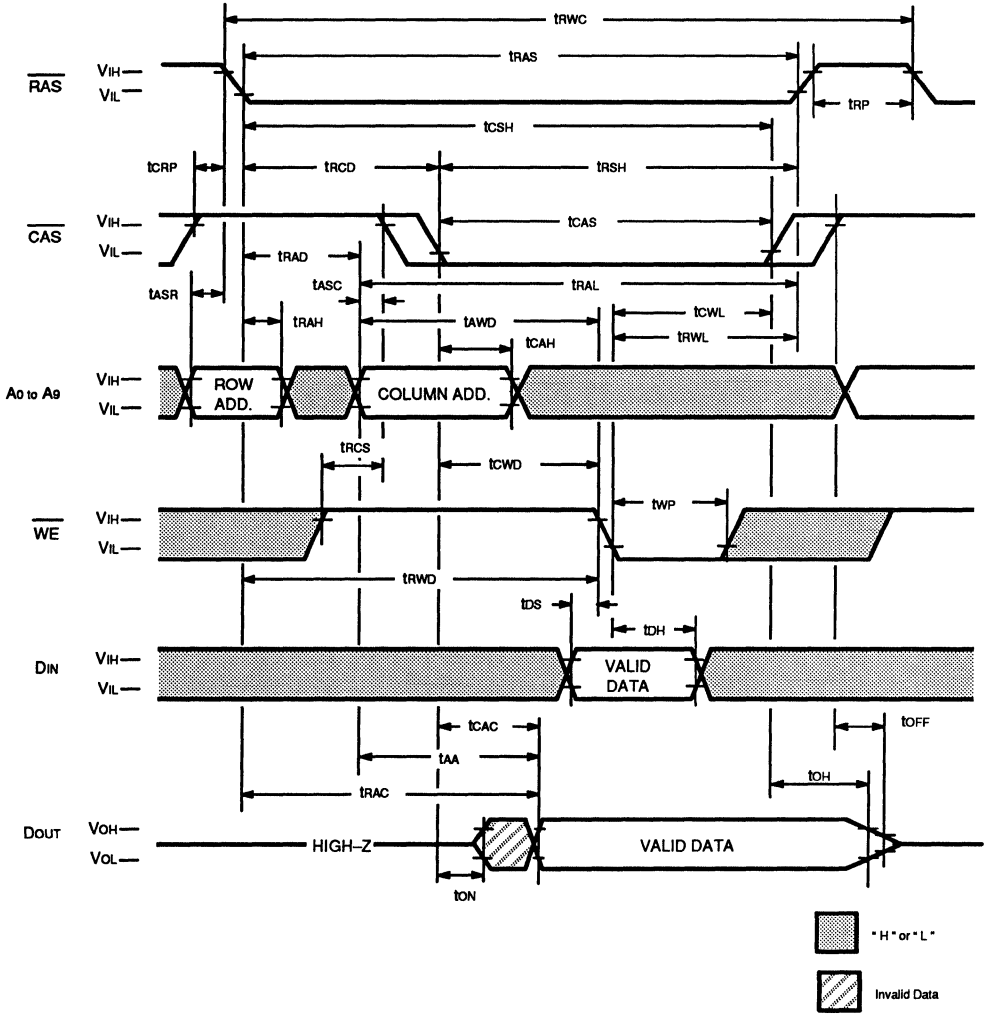
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

Fig. 7 – NIBBLE MODE READ CYCLE

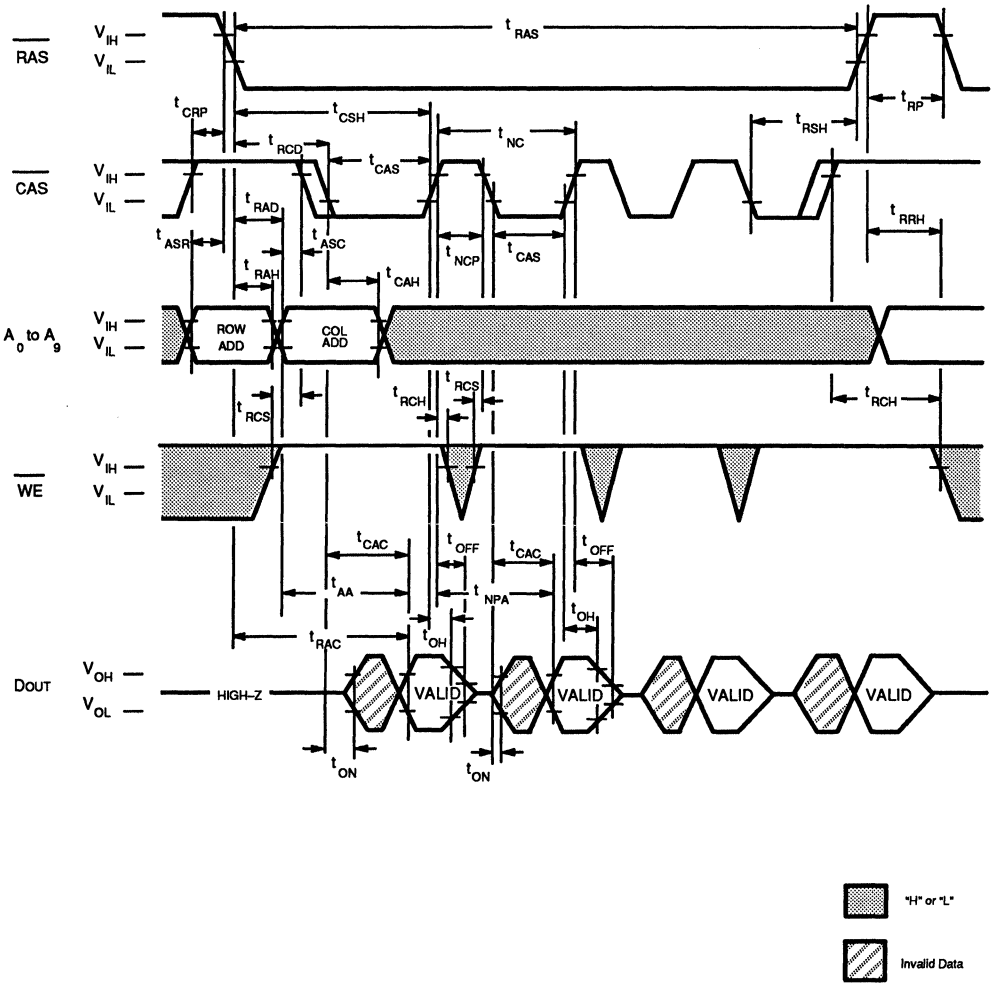


Fig. 8 – NIBBLE MODE WRITE CYCLE (Early Write)

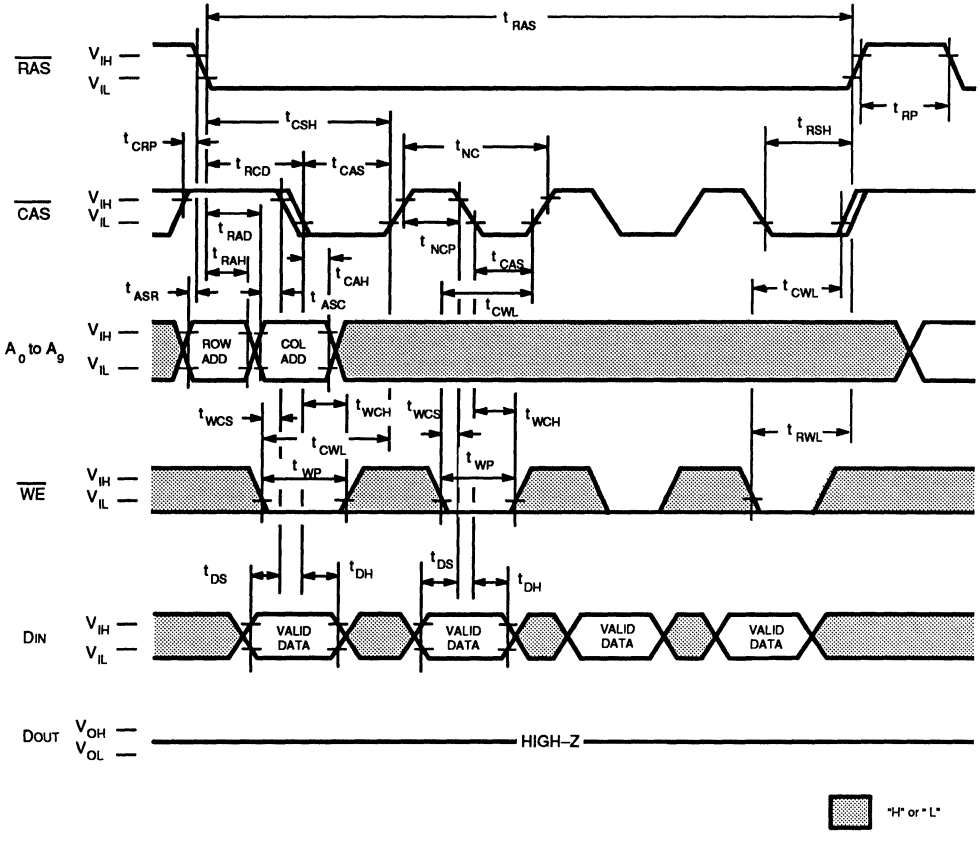


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Fig. 9 – NIBBLE MODE READ–MODIFY–WRITE CYCLE

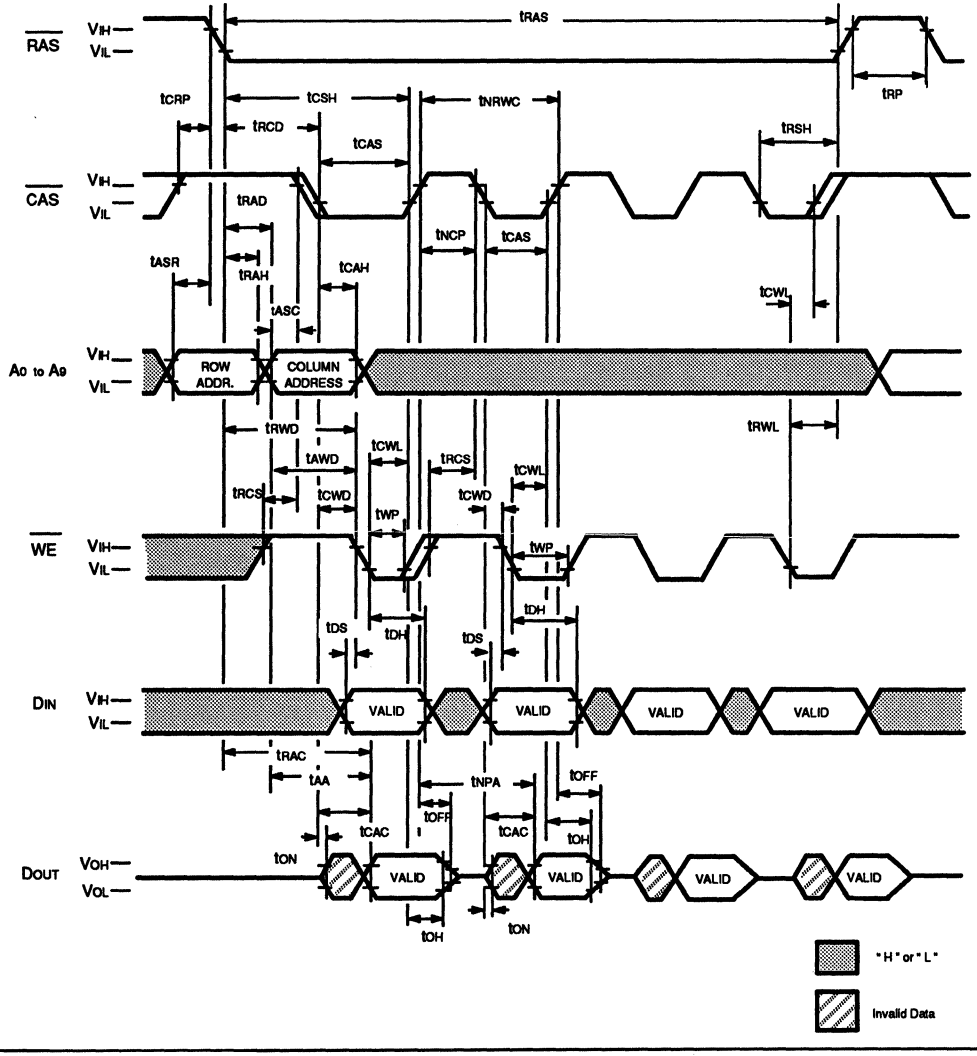
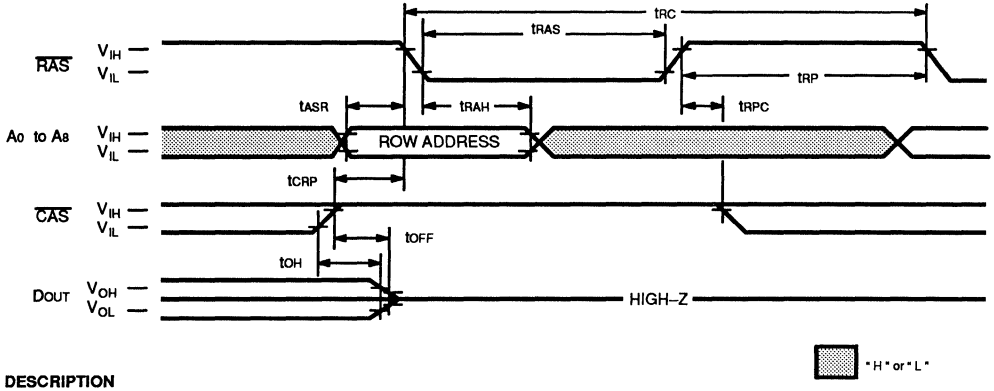


Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

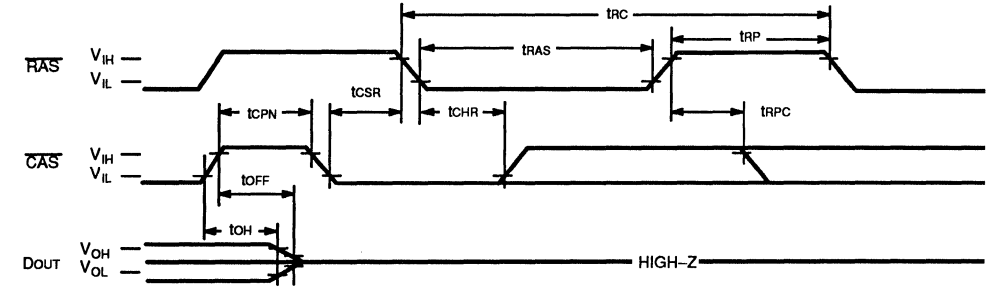


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "

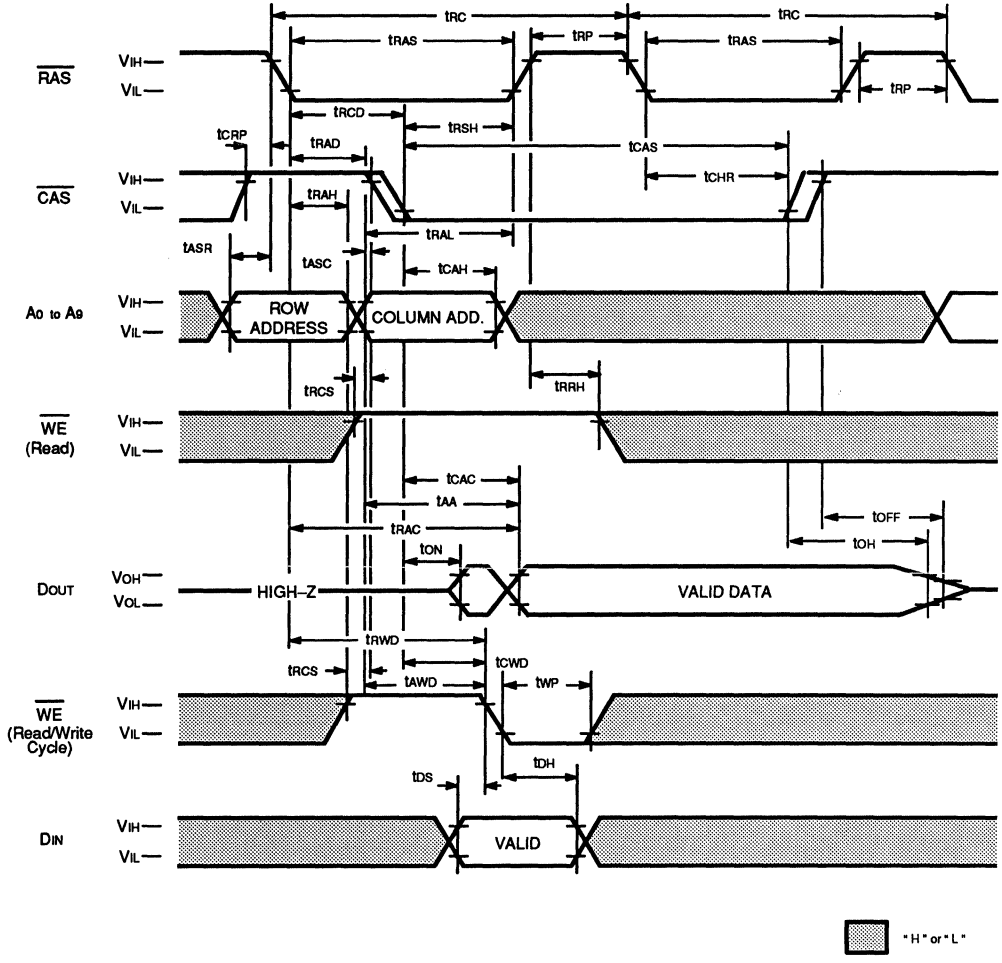


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

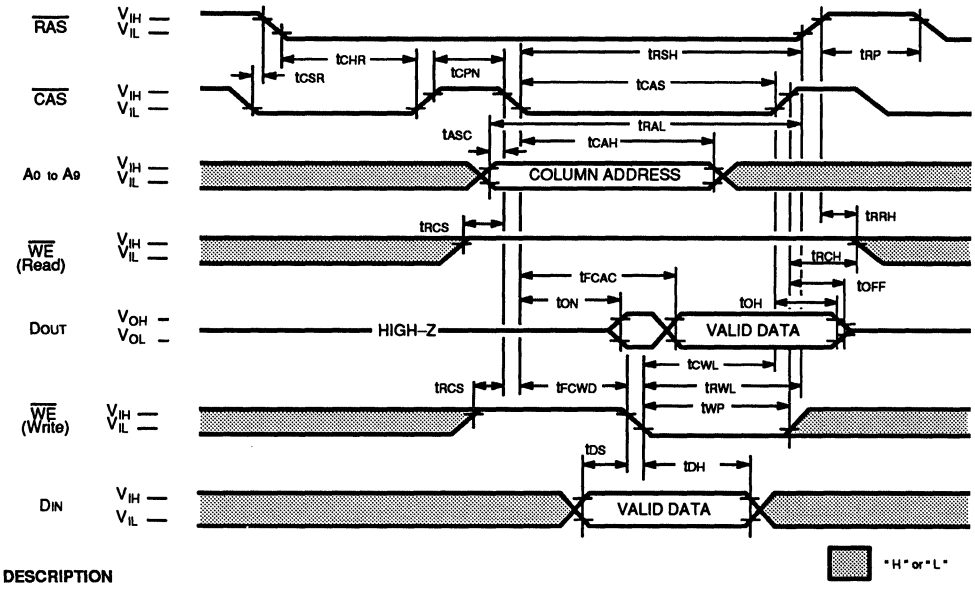
Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter. The bit A9 is set high internally.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (read–modify–write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

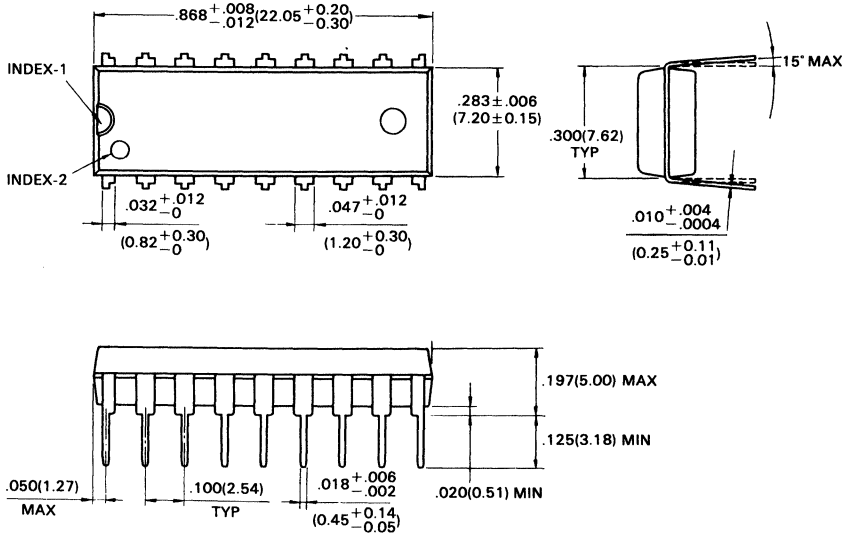
No.	Parameter	Symbol	MB81C1001A-70L		MB81C1001A-80L		MB81C1001A-10L		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	45	—	50	—	60	ns
91	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	45	—	50	—	60	—	ns

Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix: –P)

18–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–18P–M04)

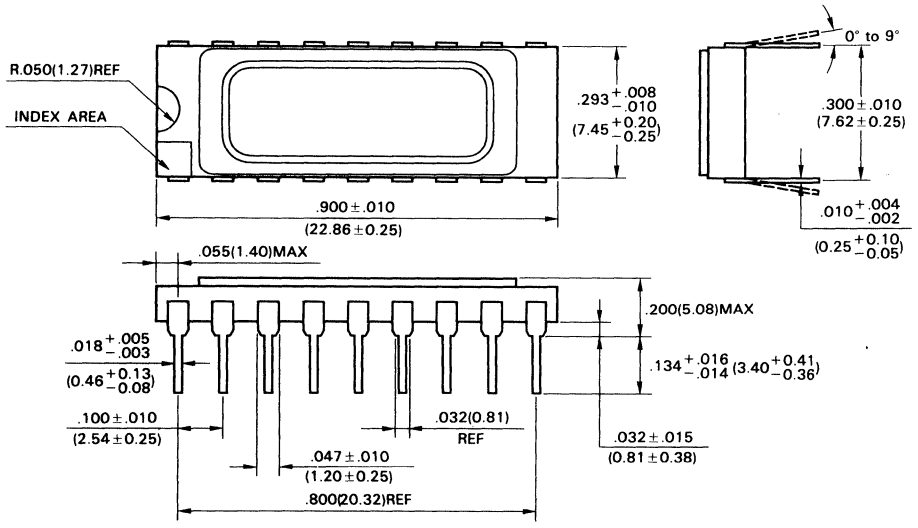


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18–LEAD CERAMIC (METAL SEAL) DUAL IN–LINE PACKAGE
(CASE No.: DIP–18C–A02)



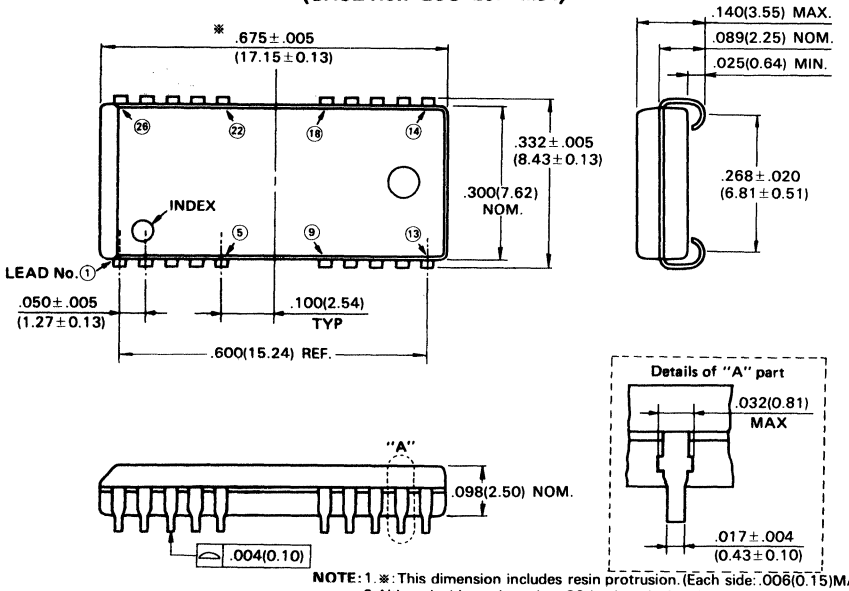
Dimensions in inches (millimeters).

2

PACKAGE DIMENSIONS (Continued)

(Suffix: -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M04)

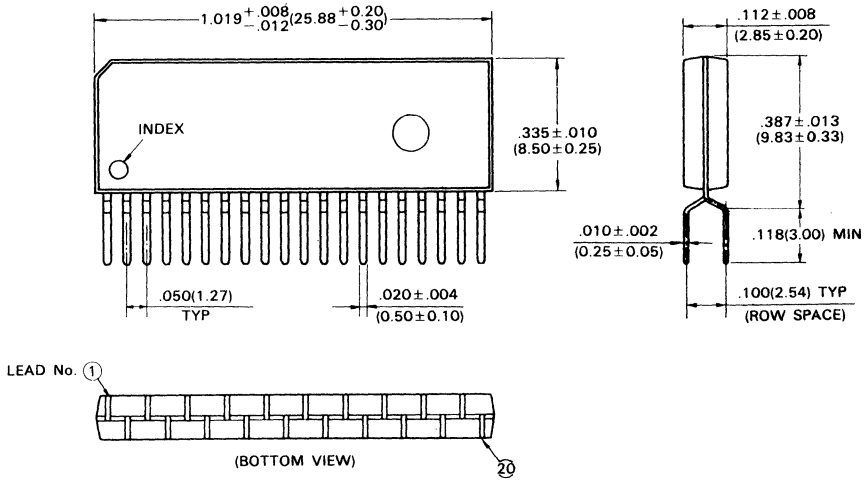


NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
3. Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PSZ)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)

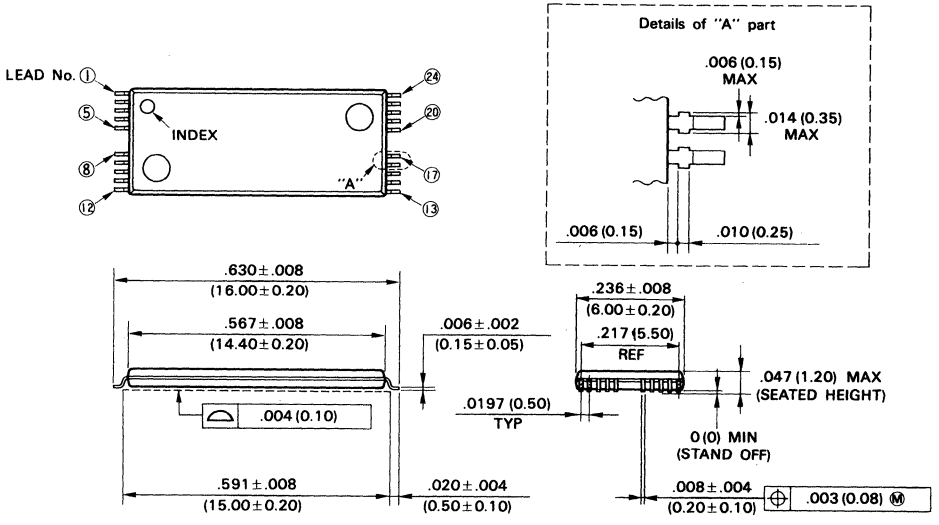


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PFTN)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M04)

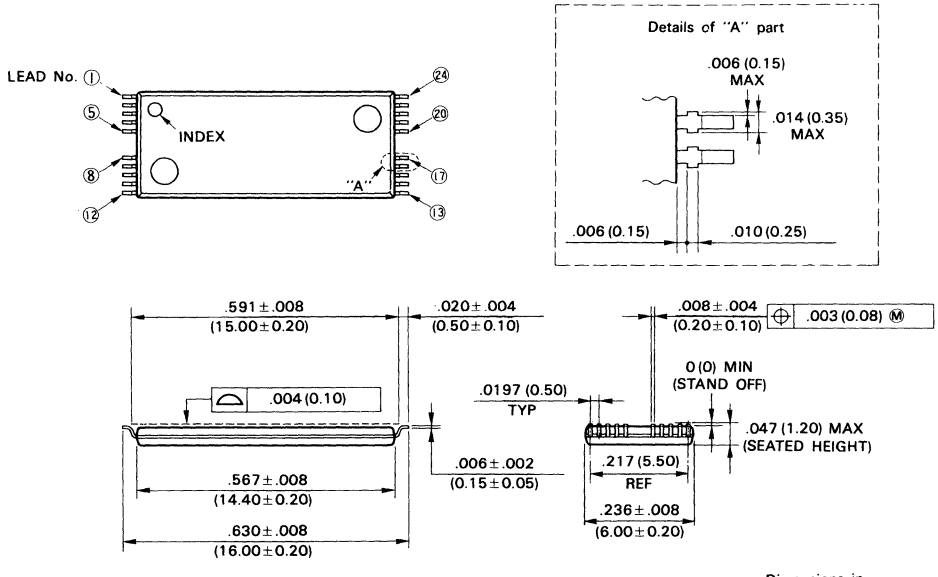


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PFTR)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M05)



Dimensions in inches (millimeters)

2

March1990
Edition 2.2

FUJITSU

DATA SHEET

MB81C4256-70/-80/-10/-12

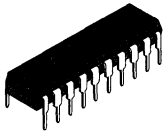
CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 256 x 4 Bits Fast Page Mode DRAM

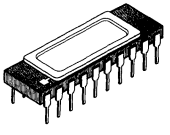
The Fujitsu MB81C4256 is a CMOS, fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4256 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed and high bandwidth output with low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C4256 high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

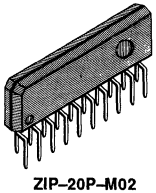


DIP–20P–M03



DIP–20C–A03

LCC–26P–M04



ZIP–20P–M02

Features

Parameter	MB81C4256 -70	MB81C4256 -80	MB81C4256 -10	MB81C4256 -12
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Fast Page Mode Cycle Time	53 ns min.	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	413 mW max.	385 mW max.	330 mW max.	275 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

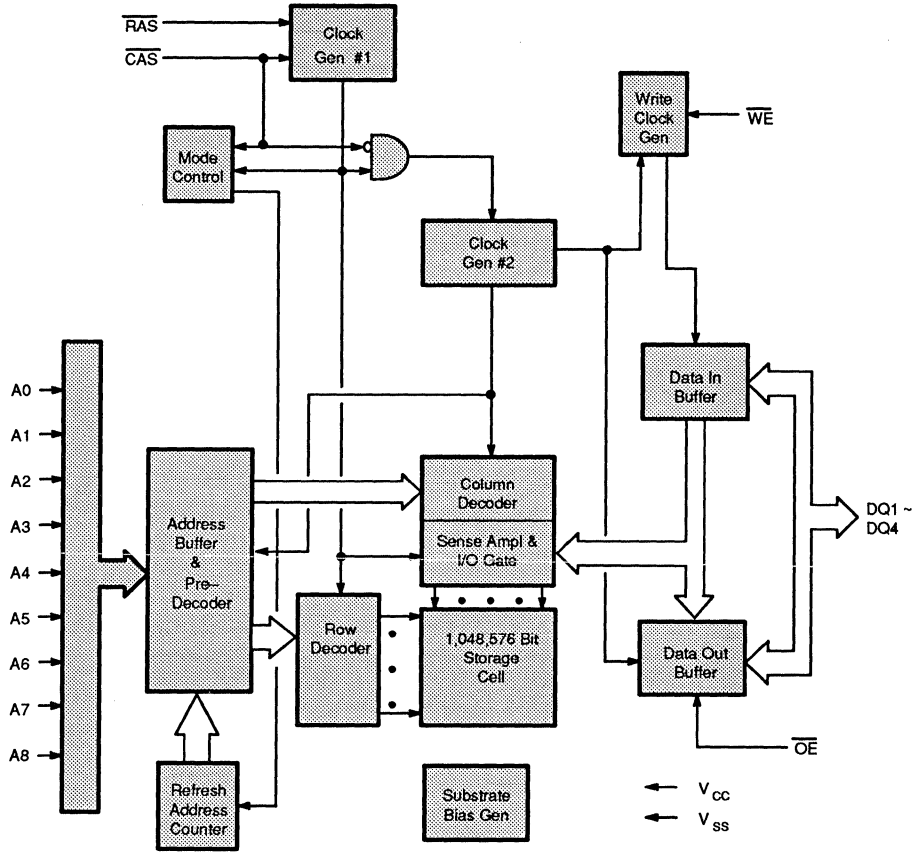
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB81C4256 DYNAMIC RAM – BLOCK DIAGRAM

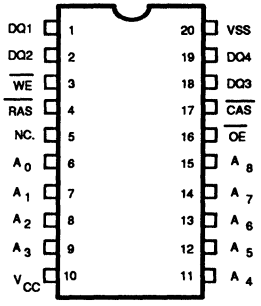


CAPACITANCE (T_A = 25°C, f = 1MHz)

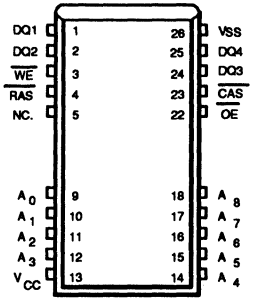
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

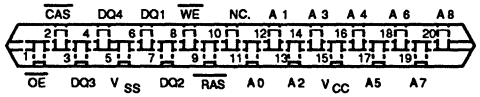
20–Pin DIP :
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 celladdresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the fallingedge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins under test = 0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average Power supply Current) [2]	MB81C4256–70	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C4256–80					70	
	MB81C4256–10					60	
	MB81C4256–12					50	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ =V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB81C4256–70	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	70	mA
	MB81C4256–80					65	
	MB81C4256–10					55	
	MB81C4256–12					45	
Fast Page Mode current [2]	MB81C4256–70	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	47	mA
	MB81C4256–80					45	
	MB81C4256–10					40	
	MB81C4256–12					33	
Refresh current #2 (Average power supply current) [2]	MB81C4256–70	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C4256–80					65	
	MB81C4256–10					55	
	MB81C4256–12					45	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256-70		MB81C4256-80		MB81C4256-10		MB81C4256-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	197	—	212	—	240	—	275	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	25	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	75	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	25	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	19	t_{CPN}	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256-70		MB81C4256-80		MB81C4256-10		MB81C4256-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
38	Access Time from $\overline{OE}$	9	t_{OEA}	—	22	—	22	—	22	—	30	ns
39	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	25	—	25	—	25	—	25	ns
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	0	—	ns
42	$\overline{OE}$ to Data In Delay Time		t_{OED}	25	—	25	—	25	—	25	—	ns
43	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	0	—	ns
44	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	0	—	ns
45	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	53	—	55	—	60	—	70	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	105	—	107	—	115	—	130	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	53	—	55	—	60	—	70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	15	—	ns

Notes:

1. Referenced to VSS
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200μs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min)
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh, $\overline{CAS}$ -before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

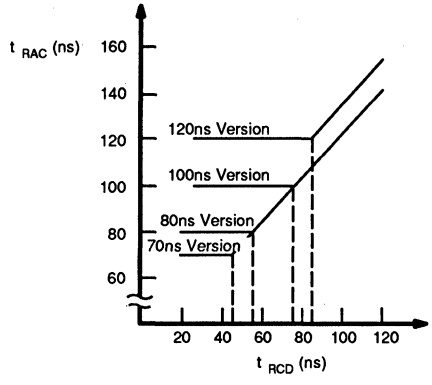
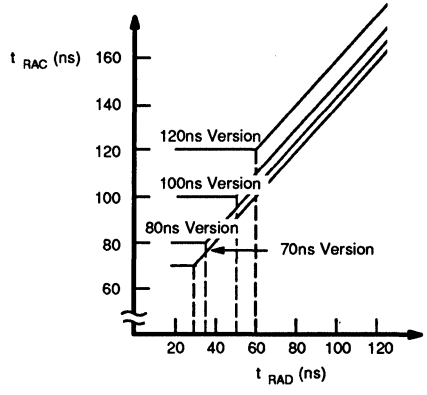


Fig. 3 – t_{RAC} vs. t_{RAD}



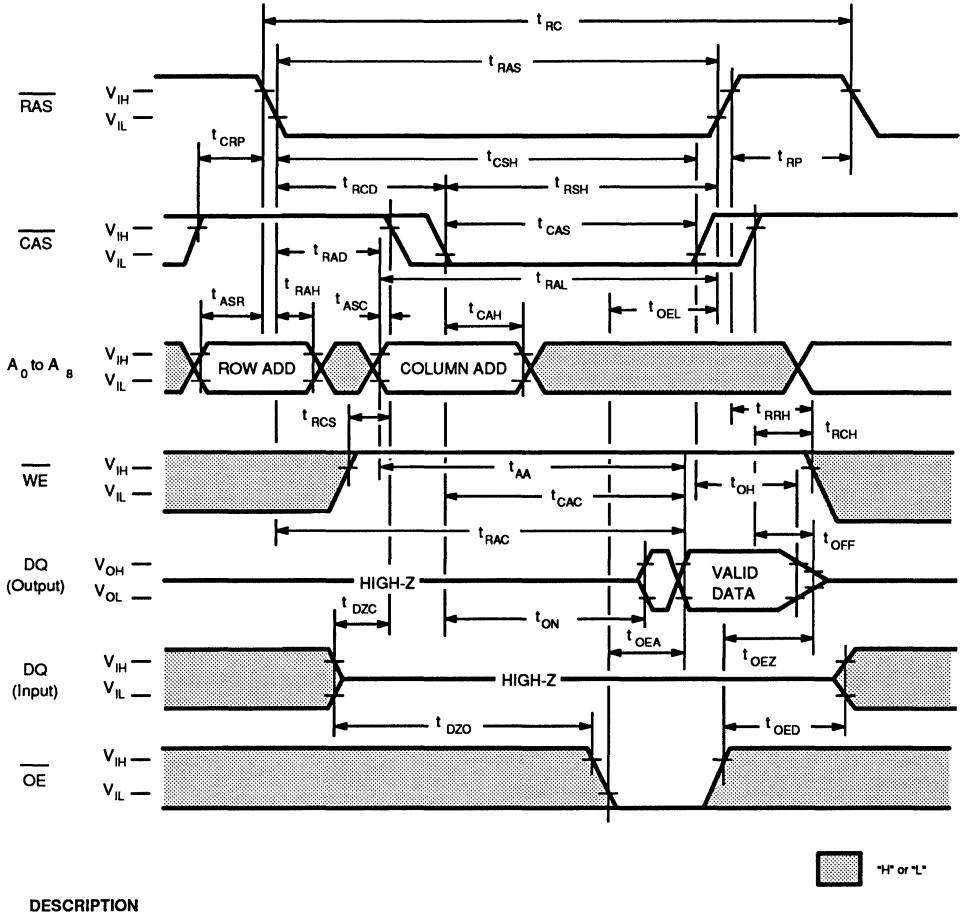
2

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High–Z	Yes	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$(tRAC), $\overline{CAS}$(tCAC), $\overline{OE}$ (tOEA) or column addresses (tAA) under the following conditions:

If tRCD > tRCD (max), access time = tCAC.

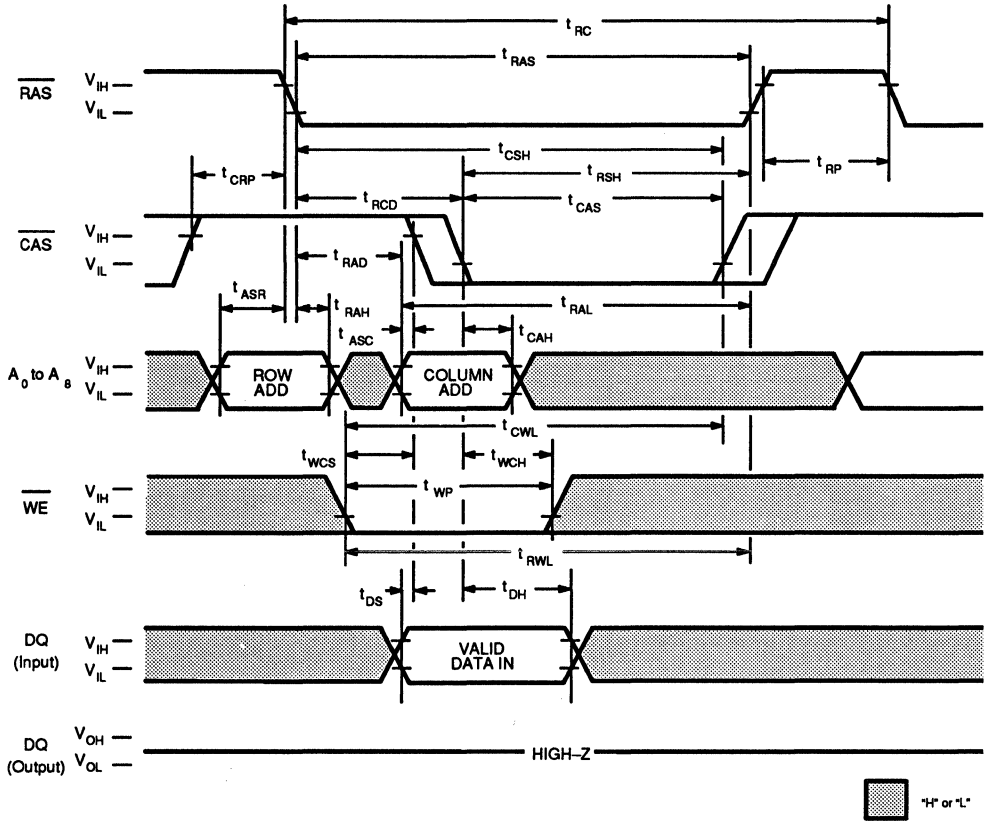
If tRAD > tRAD (max), access time = tAA.

If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high–impedance state after tOH is satisfied.

2

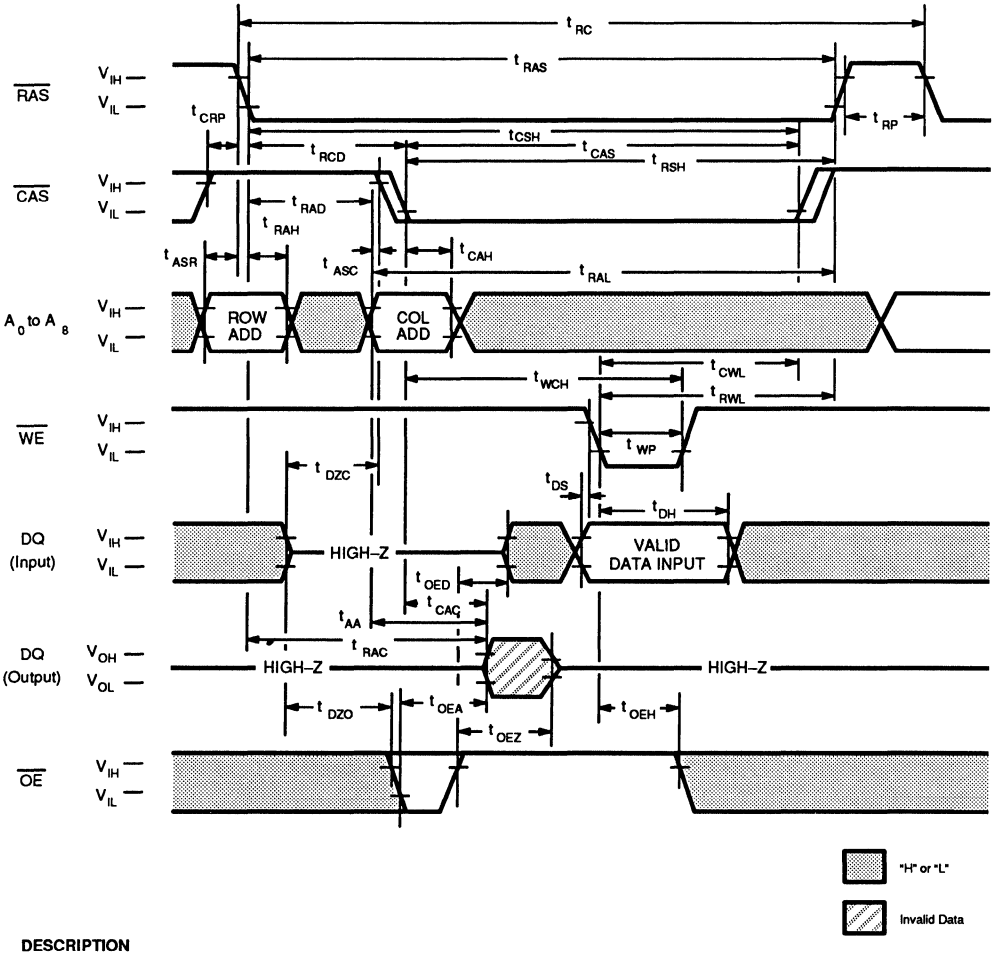
Fig. 5 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above tWCS satisfied, data on the DQ pin is latched with the falling edge of $\overline{CAS}$ and written into memory.

Fig. 6 – $\overline{OE}$ (DELAYED WRITE CYCLE)

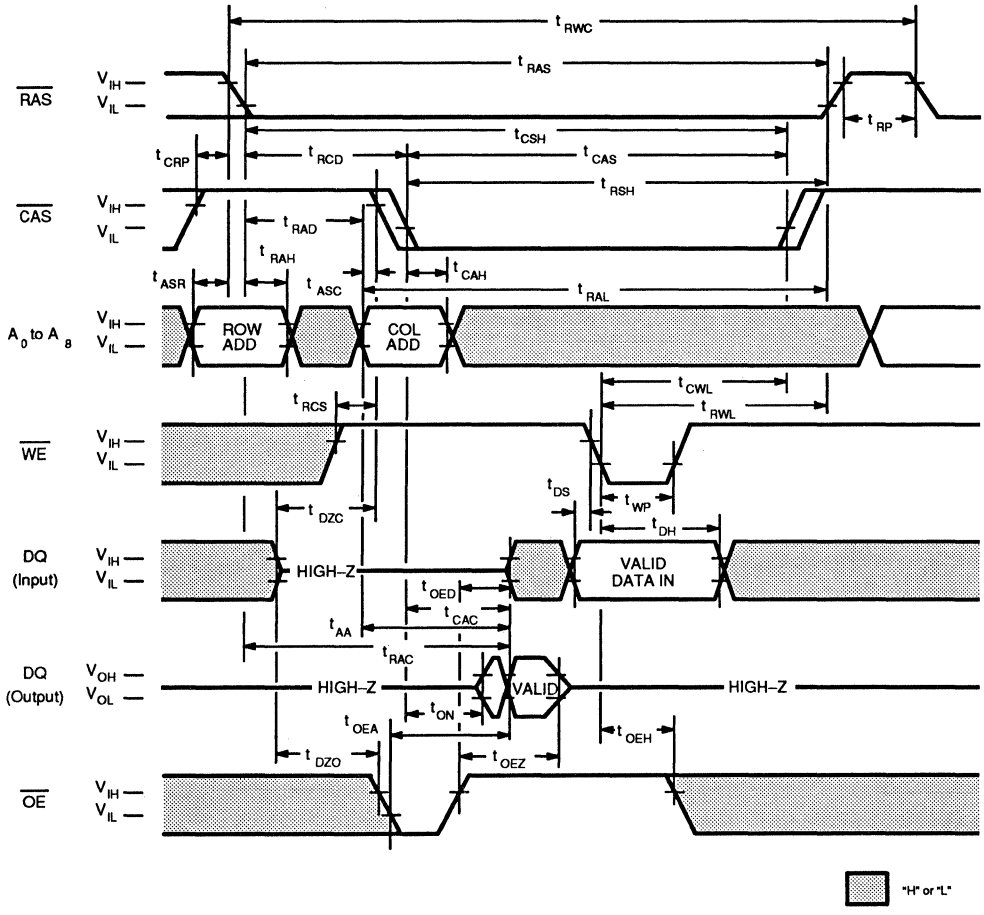


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, tWCS is not satisfied ; thus, the data on the DQpins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

2

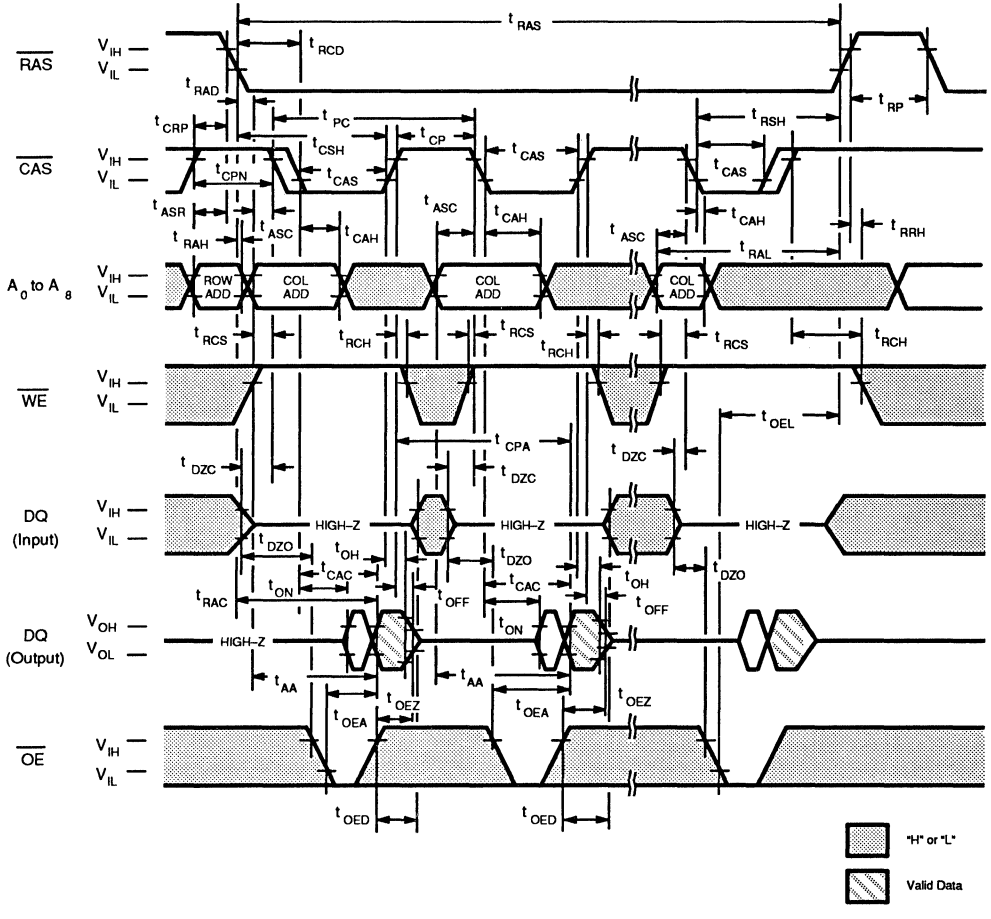
Fig. 7 – READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 8 – FAST PAGE MODE READ CYCLE

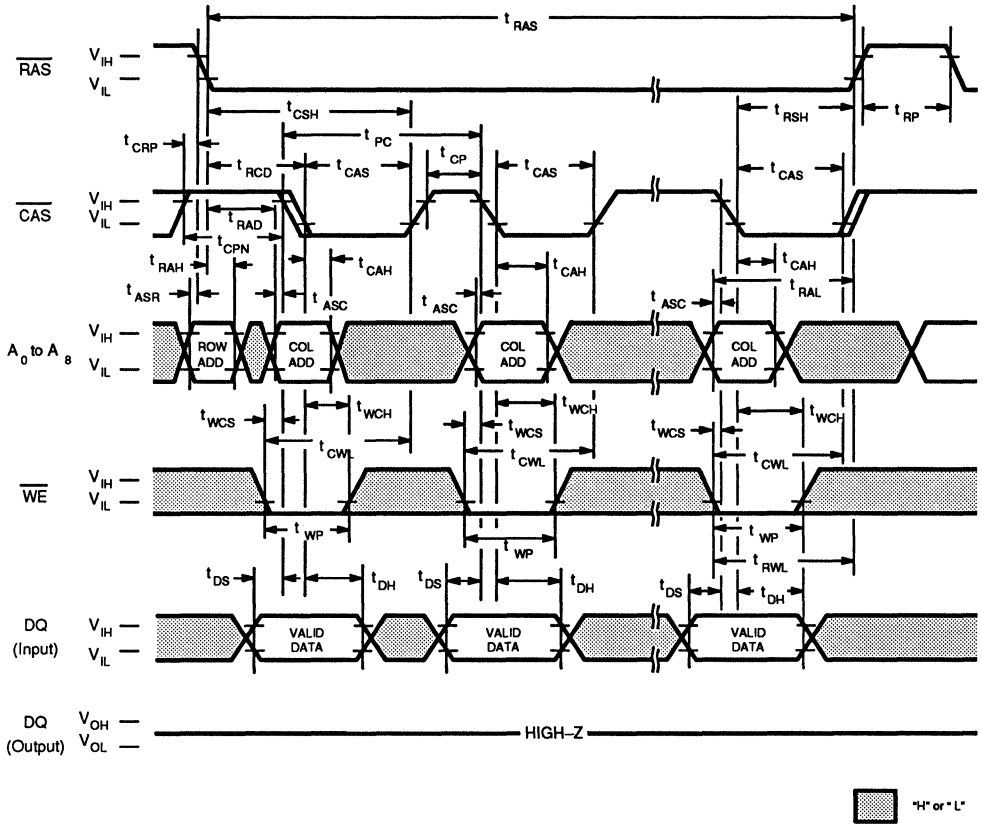


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occuring.

2

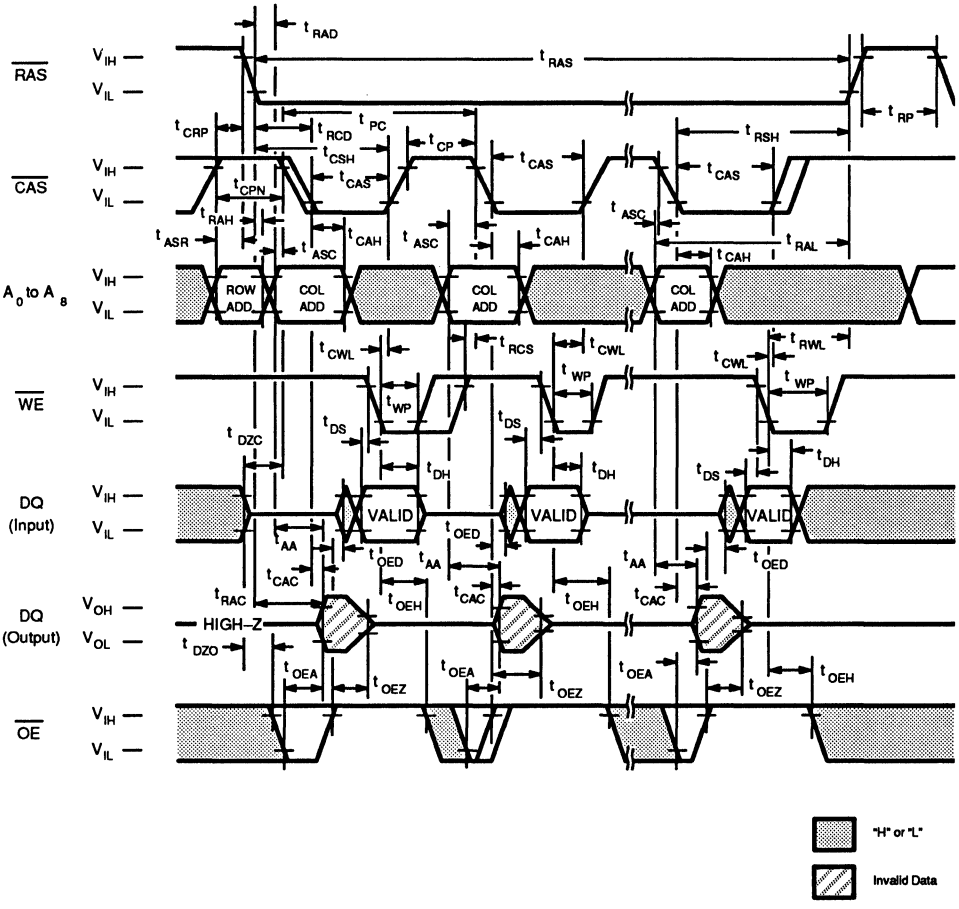
Fig. 9 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fastpage mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, tCWL must be satisfied.

Fig. 10 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

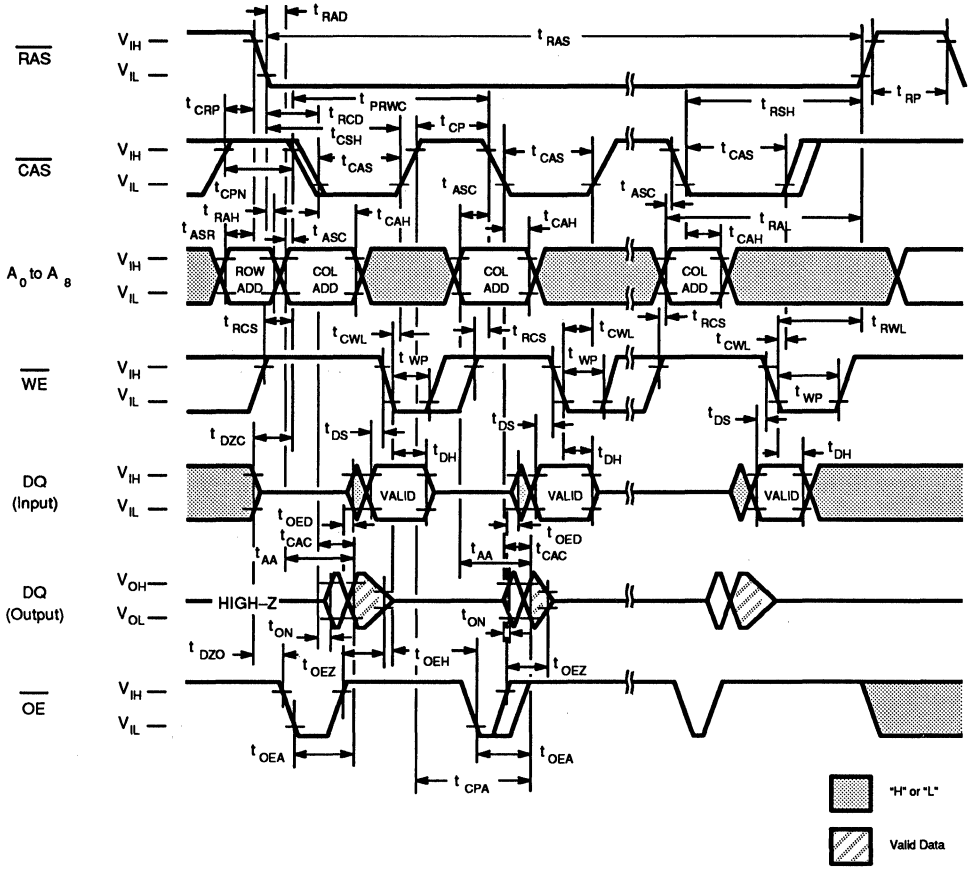


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

2

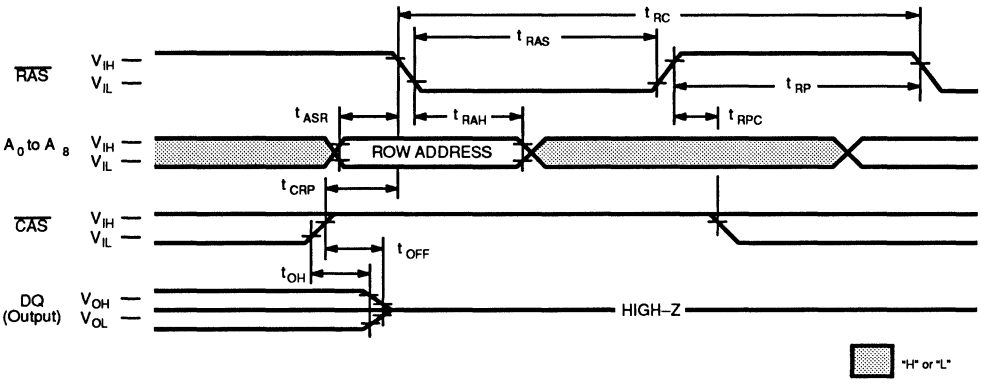
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

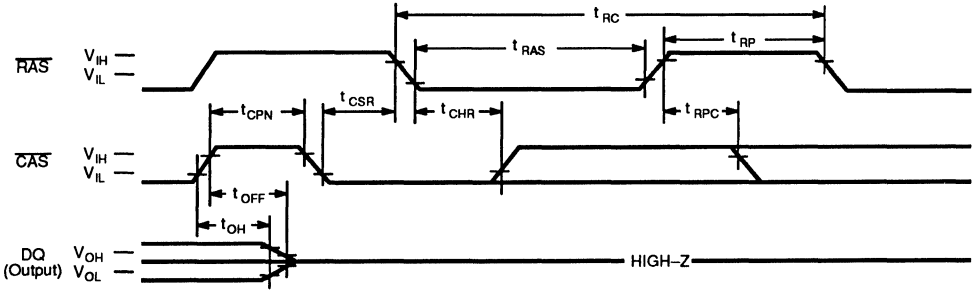


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, D_{OUT} pin is kept in a high-impedance state.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

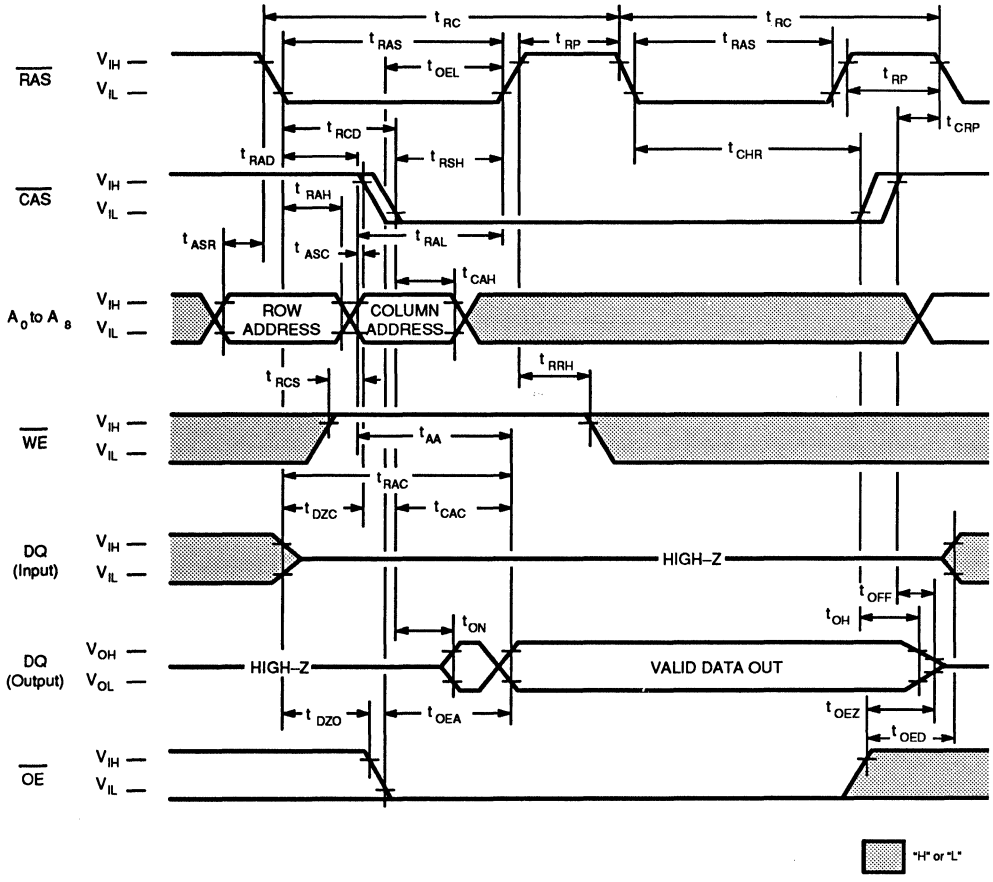


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

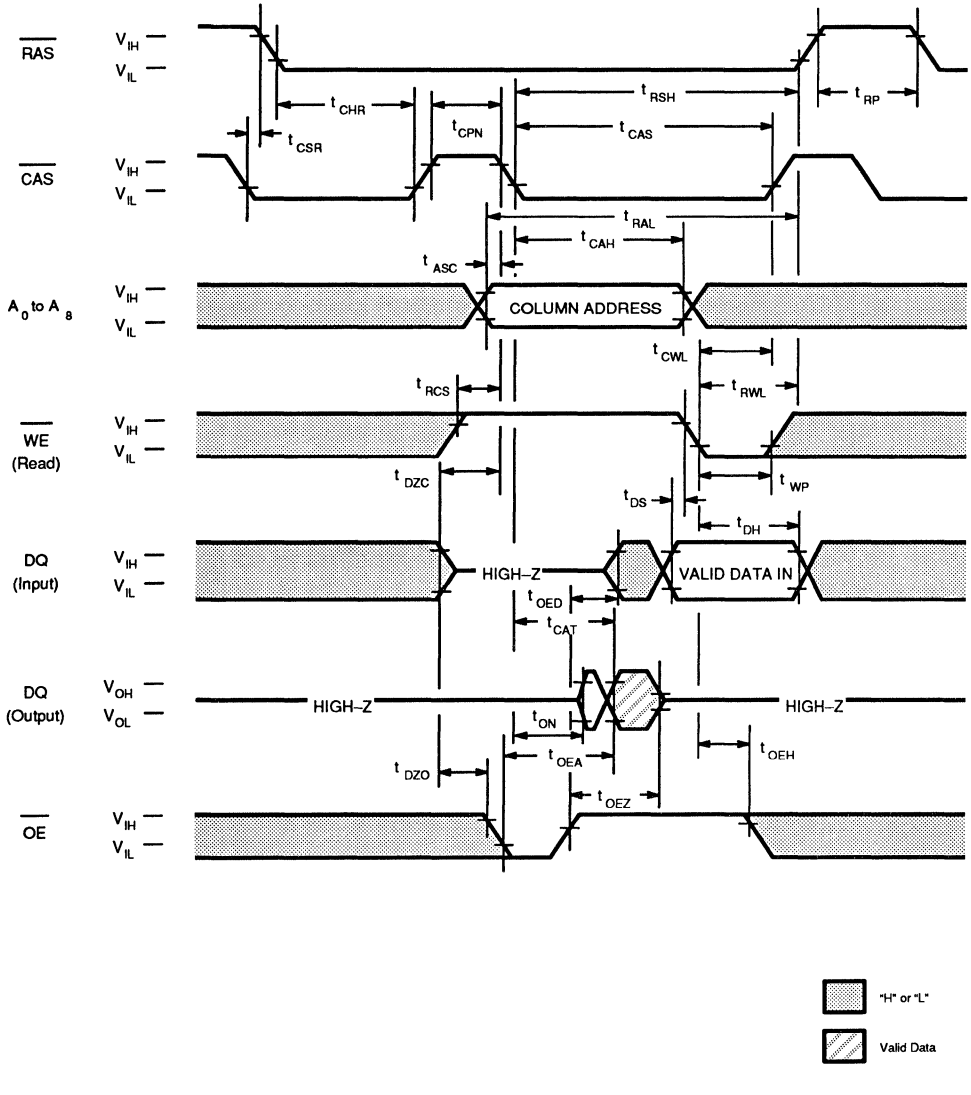
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh addresscounter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 15 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

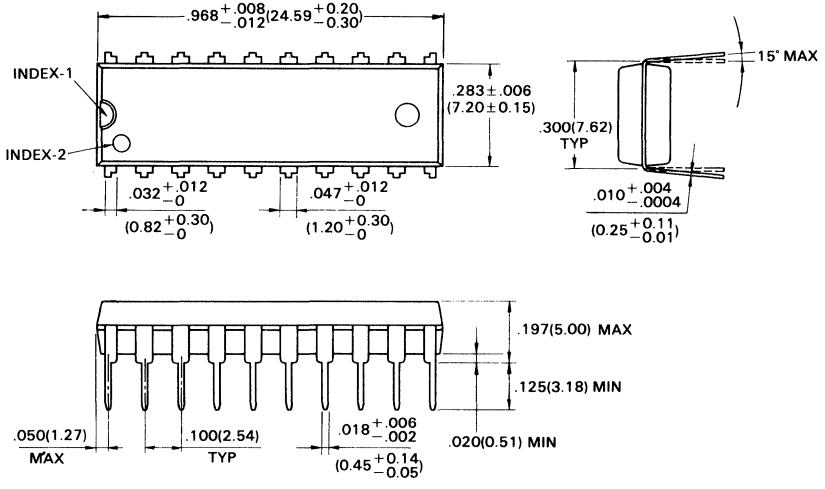


PACKAGE DIMENSIONS

(Suffix : –P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M03)

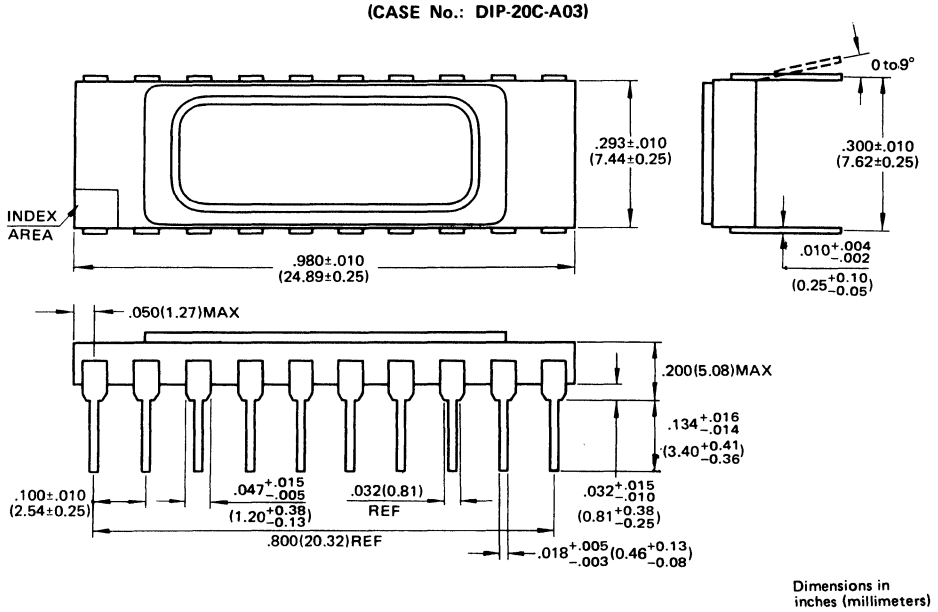


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-A03)

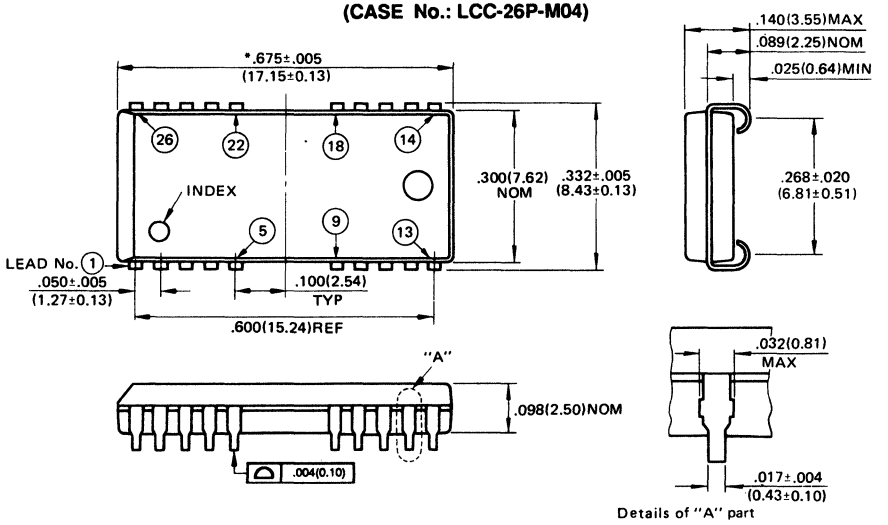


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

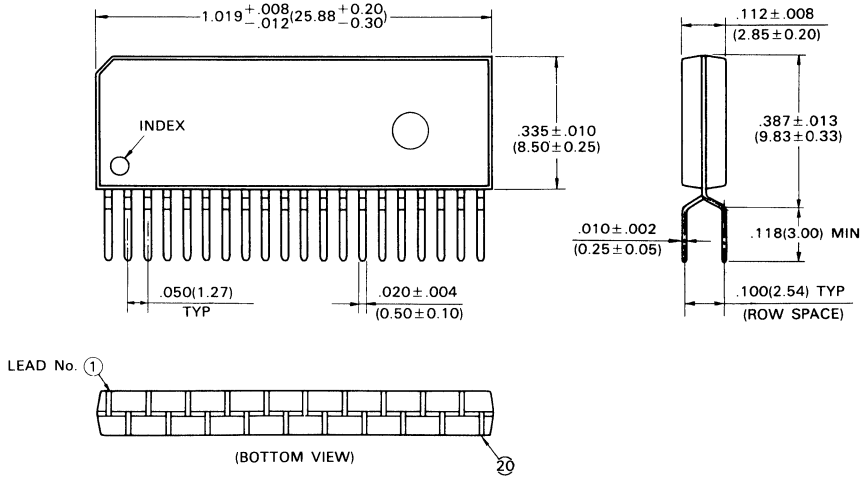
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

2

2

February 1990
Edition 1.0

FUJITSU

DATA SHEET

MB81C4256-70L/-80L/-10L/-12L

CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 256 x 4 Bits Fast Page Mode DRAM

The Fujitsu MB81C4256 is a CMOS, fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4256 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed and high bandwidth output with very low power dissipation for battery operated applications.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C4256 high α-ray soft error immunity and extended refresh time. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

Features

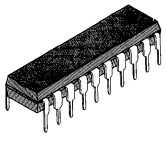
Parameter	MB81C4256 -70L	MB81C4256 -80L	MB81C4256 -10L	MB81C4256 -12L
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Fast Page Mode Cycle Time	53 ns min.	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	396 mW max.	358 mW max.	303 mW max.	259 mW max.
• Standby Current	8.3 mW max. (TTL level)/1.4 mW max. (CMOS level)			

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 64 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

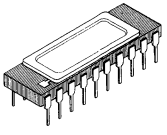
Absolute Maximum Ratings (See Note)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

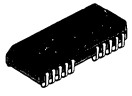
Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



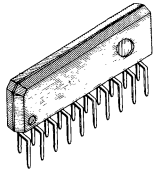
DIP–20P–M03



DIP–20C–A03



LCC–26P–M04

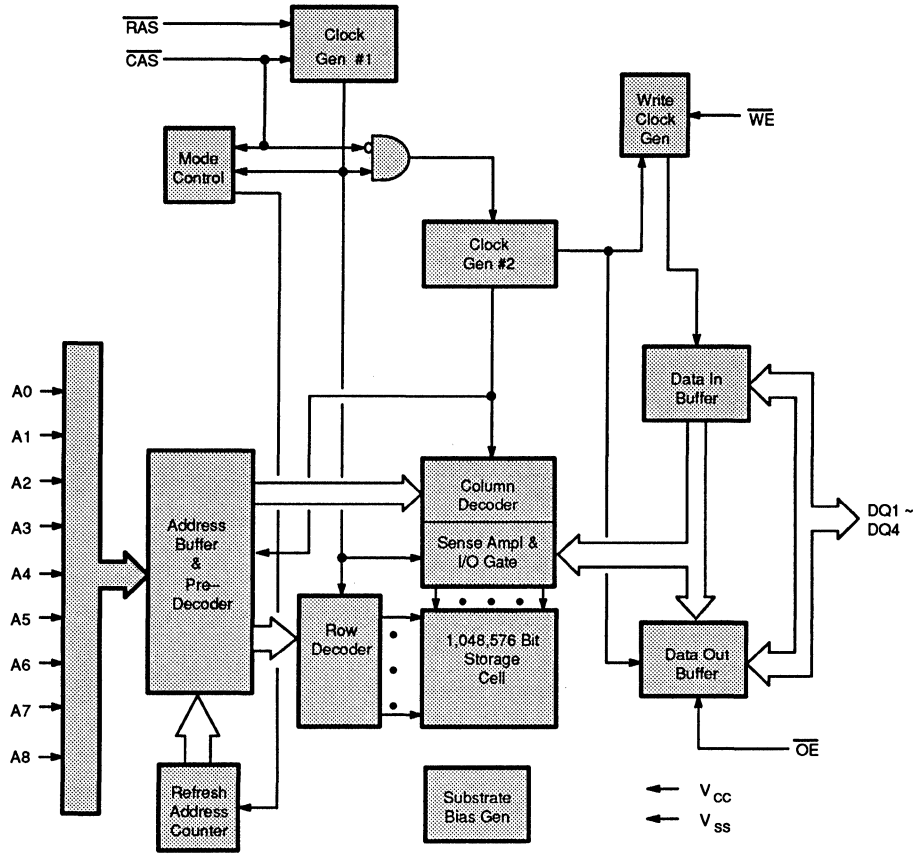


ZIP–20P–M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB81C4256 DYNAMIC RAM – BLOCK DIAGRAM

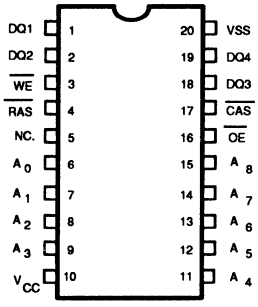


CAPACITANCE (T_A = 25°C, f = 1MHz)

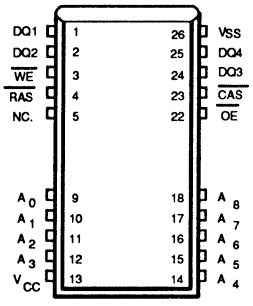
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

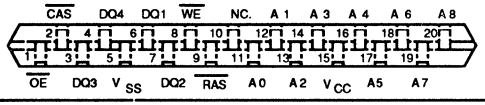
20–Pin DIP :
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

2

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins under test = 0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average Power supply Current)	MB81C4256–70L	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	72	mA
	MB81C4256–80L					65	
	MB81C4256–10L					55	
	MB81C4256–12L					47	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ =V_{IH}	—	—	1.5	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			250	µA
Refresh current #1 (Average power supply current) [2]	MB81C4256–70L	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	60	mA
	MB81C4256–80L					56	
	MB81C4256–10L					50	
	MB81C4256–12L					45	
Fast Page Mode current [2]	MB81C4256–70L	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	39	mA
	MB81C4256–80L					37	
	MB81C4256–10L					33	
	MB81C4256–12L					28	
Refresh current #2 (Average power supply current) [2]	MB81C4256–70L	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	60	mA
	MB81C4256–80L					56	
	MB81C4256–10L					50	
	MB81C4256–12L					45	
Battery Back up current (Average power supply current)	MB81C4256–70L	I_{CC6}	$\overline{RAS}$ cycling ; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} =125 µs, t_{RAS} =min. to 1 µ s, DQ1 to 4 ≥ Vcc –0.2V or ≤ 0.2V or Open Other pin ≥Vcc–0.2V or ≤ 0.2V	—	—	250	µA
	MB81C4256–80L						
	MB81C4256–10L						
	MB81C4256–12L						

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256-70L		MB81C4256-80L		MB81C4256-10L		MB81C4256-12L		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	64	—	64	—	64	—	64	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	197	—	212	—	240	—	275	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	25	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	75	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	25	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	19	t_{CPN}	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256-70L		MB81C4256-80L		MB81C4256-10L		MB81C4256-12L		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
38	Access Time from $\overline{OE}$	9	t_{OEA}	—	22	—	22	—	22	—	30	ns
39	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	25	—	25	—	25	—	25	ns
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	0	—	ns
42	$\overline{OE}$ to Data In Delay Time		t_{OED}	25	—	25	—	25	—	25	—	ns
43	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	0	—	ns
44	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	0	—	ns
45	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	53	—	55	—	60	—	70	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	105	—	107	—	115	—	130	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	53	—	55	—	60	—	70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min)
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

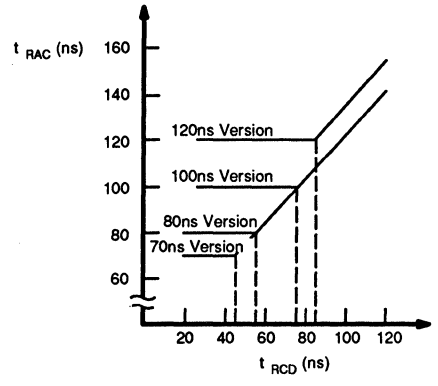
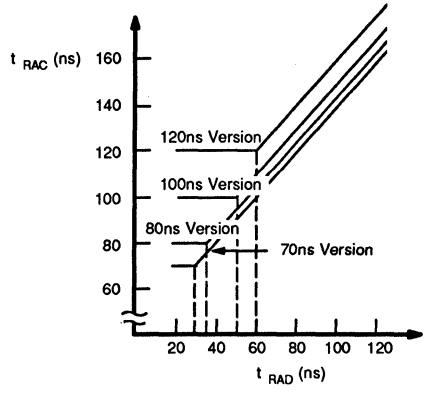


Fig. 3 – t_{RAC} vs. t_{RAD}



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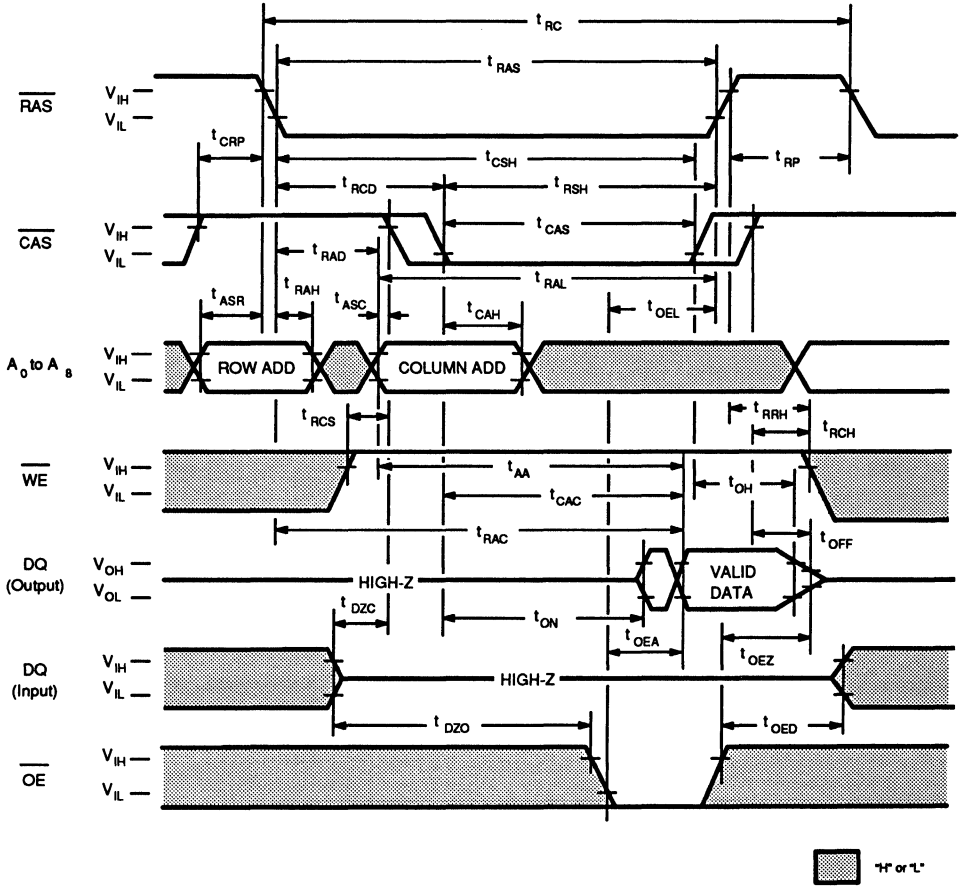
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High–Z	Yes	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$(tRAC), $\overline{CAS}$(tCAC), $\overline{OE}$ (tOEA) or column addresses (tAA) under the following conditions:

If tRCD > tRCD (max), access.time = tCAC.

If tRAD > tRAD (max), access time = tAA.

If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high–impedance state after tOH is satisfied.

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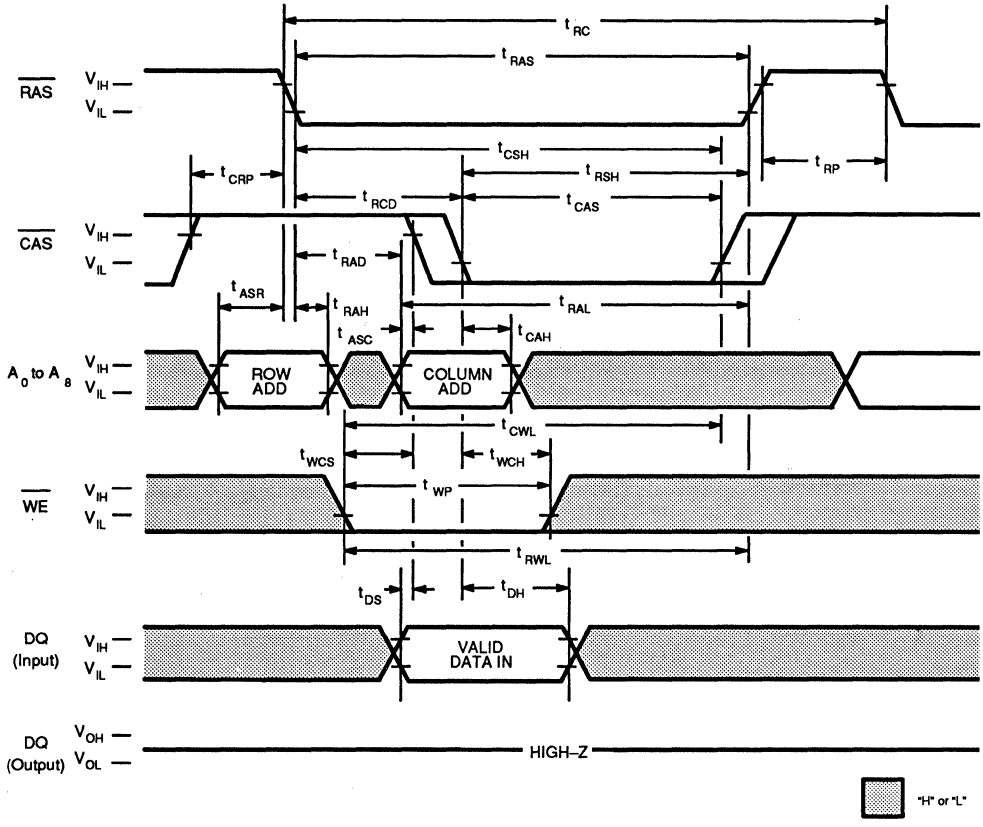
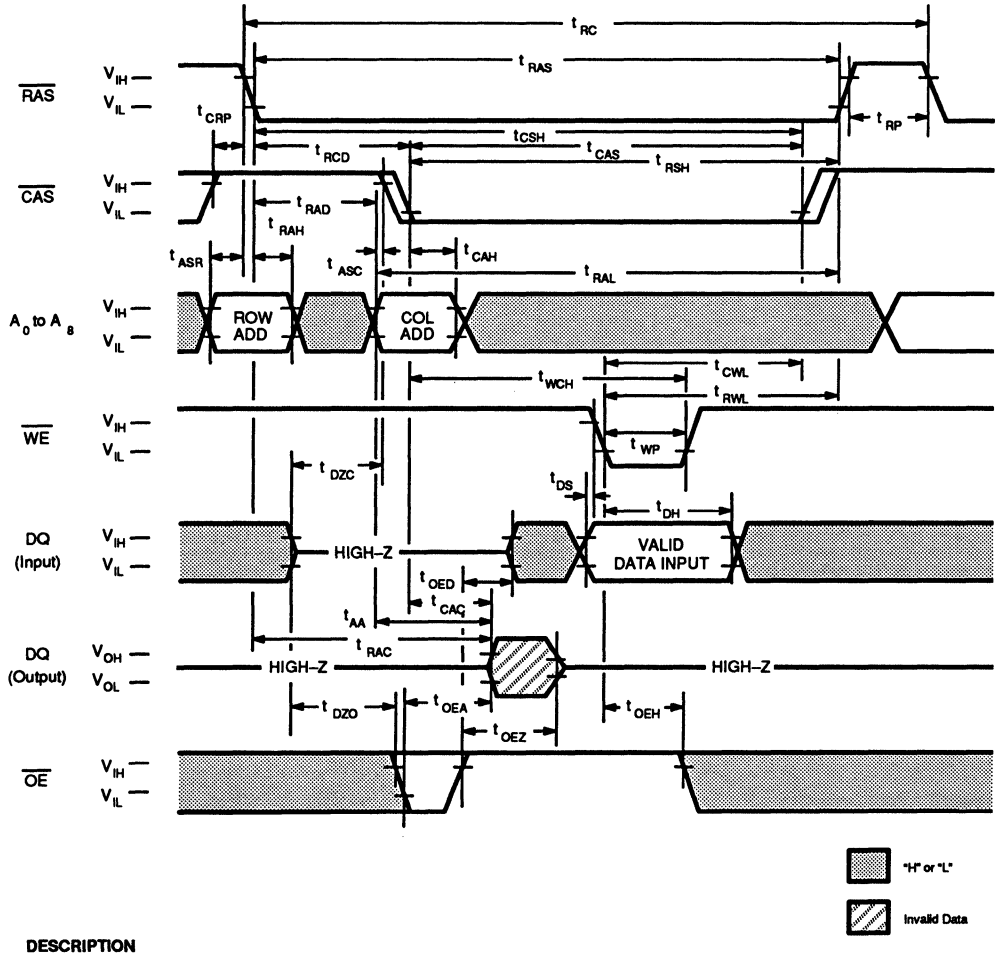
Fig. 5 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above tWCS satisfied, data on the DQ pin is latched with the falling edge of $\overline{CAS}$ and written into memory.

Fig. 6 – $\overline{OE}$ (DELAYED WRITE CYCLE)



DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, tWCS is not satisfied ; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

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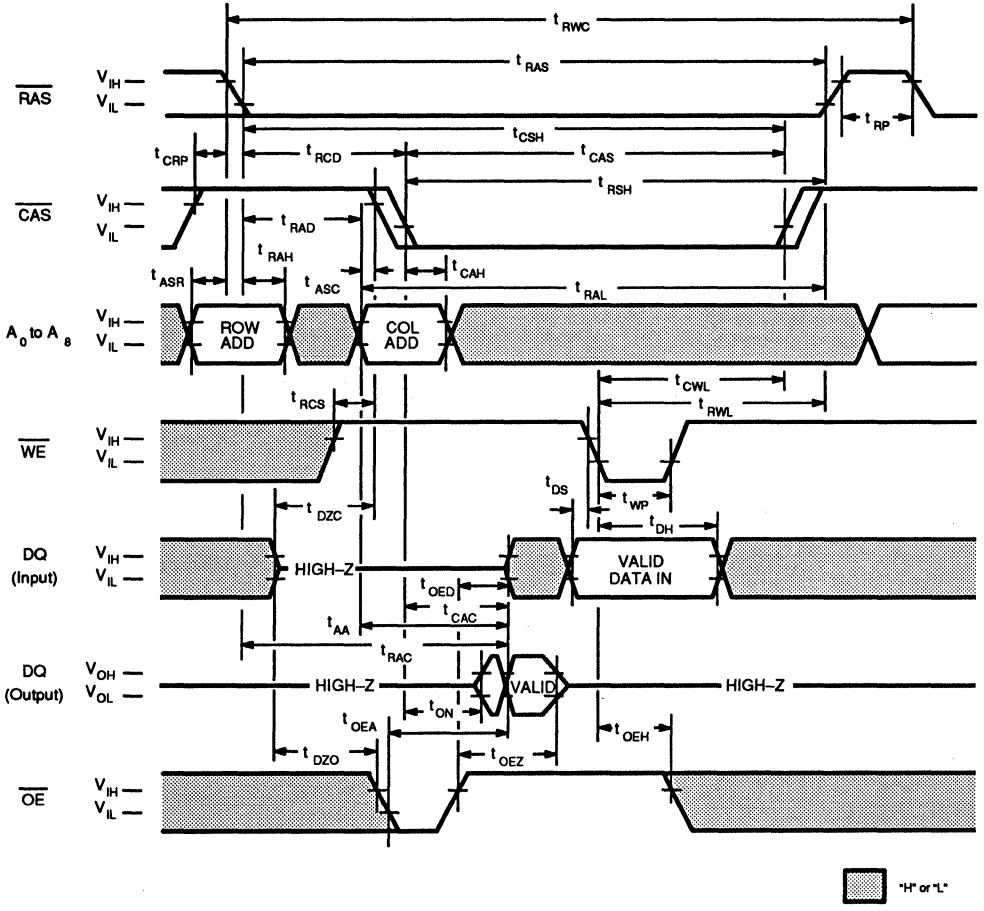
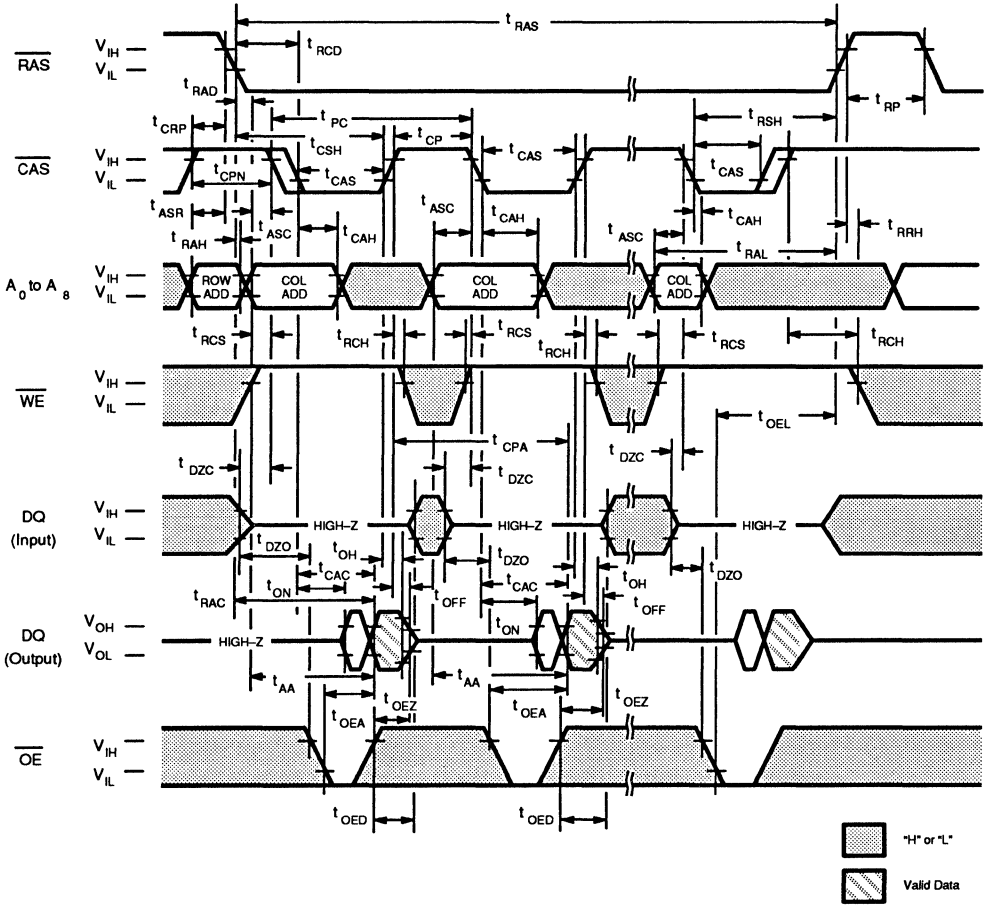
Fig. 7 – READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 8 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occuring.

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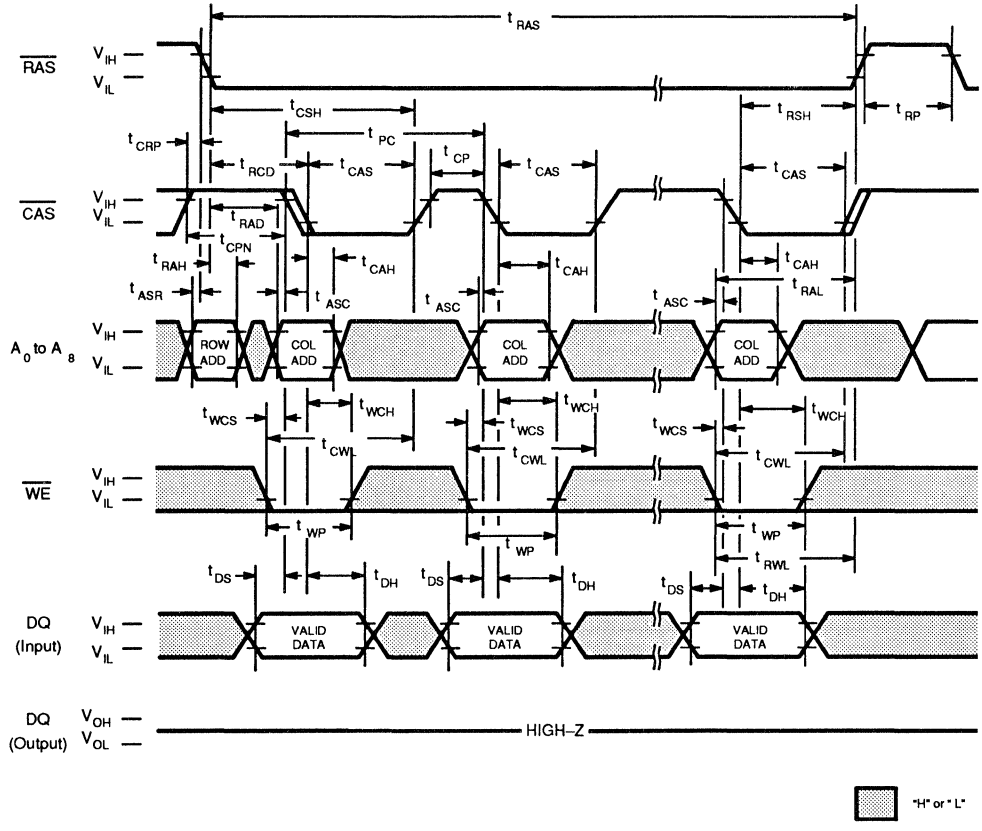
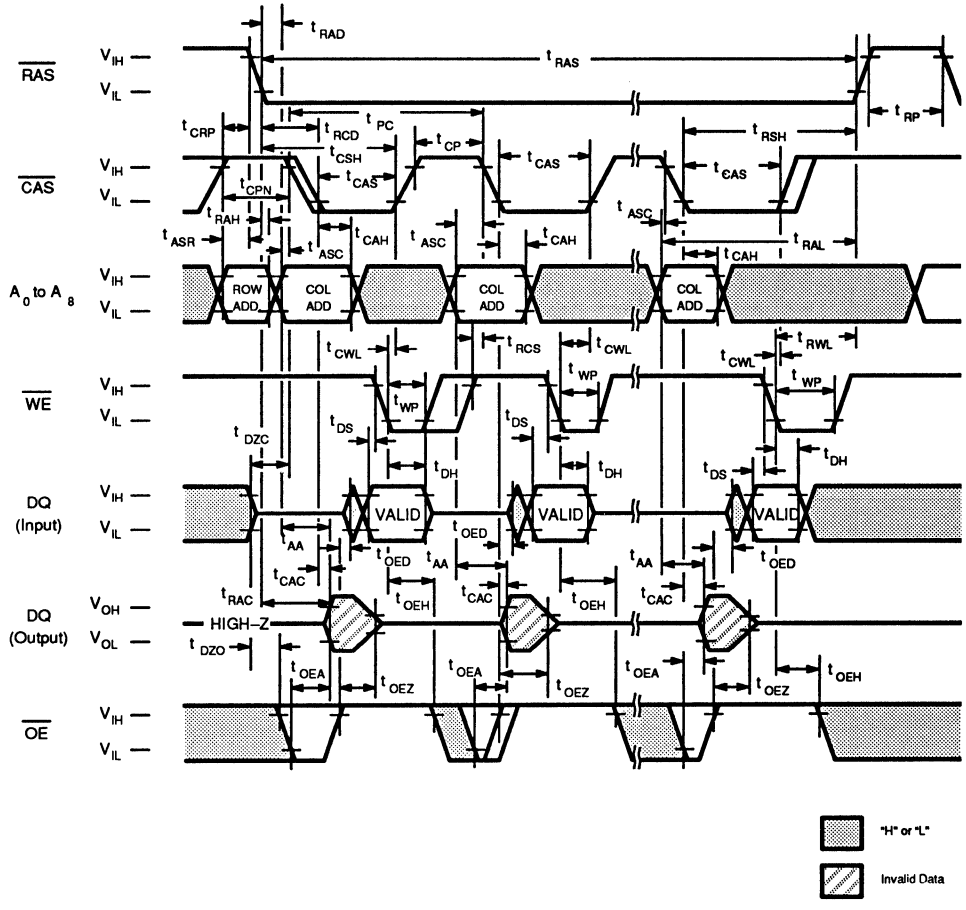
Fig. 9 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fastpage mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, tCWL must be satisfied.

Fig. 10 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE



DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

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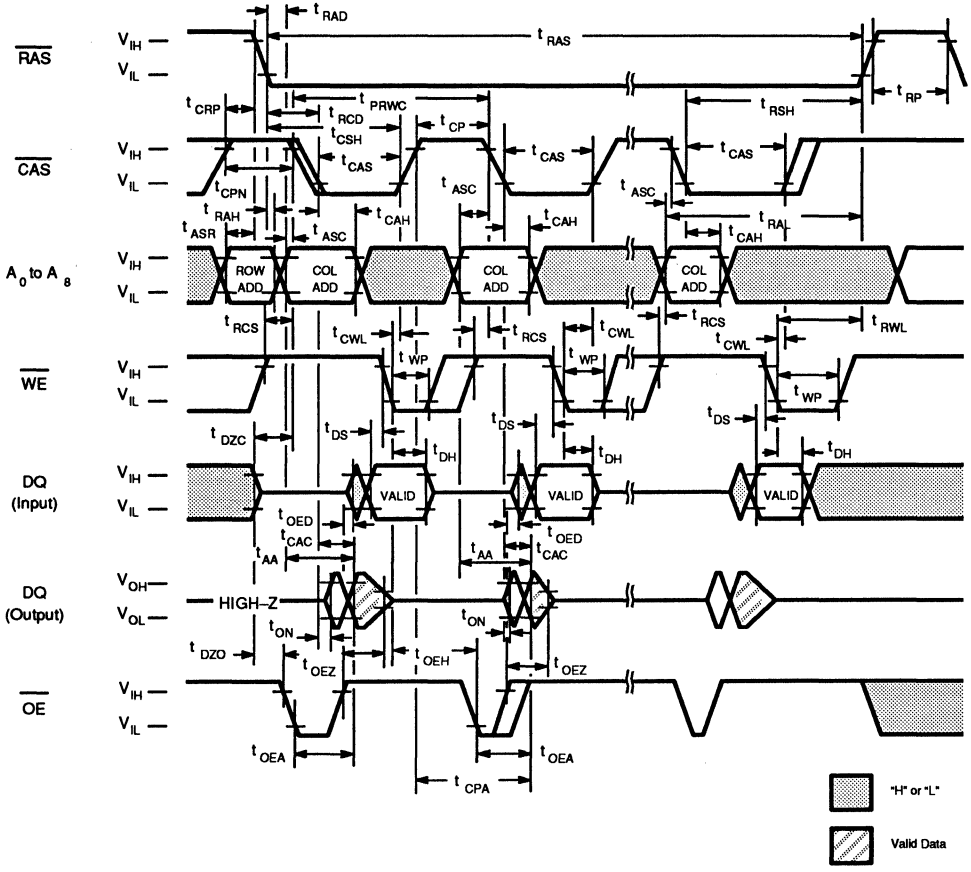
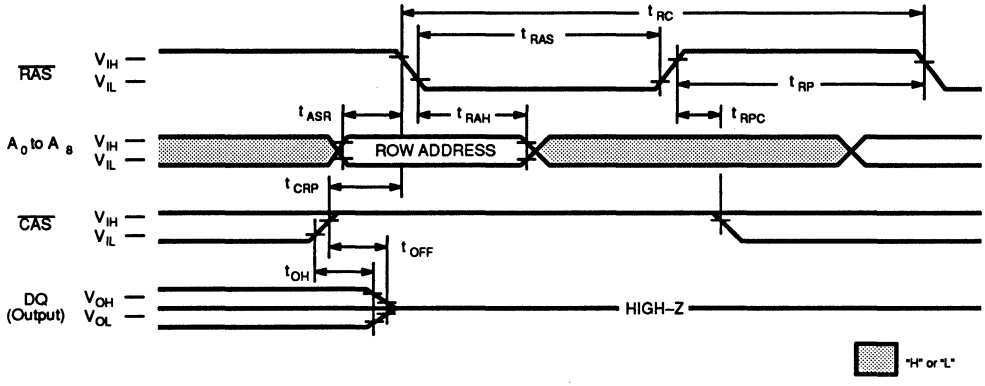
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 — $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

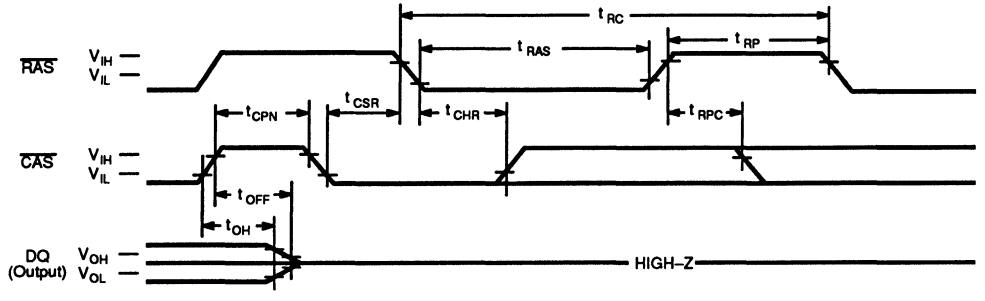


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 64–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 13 — $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

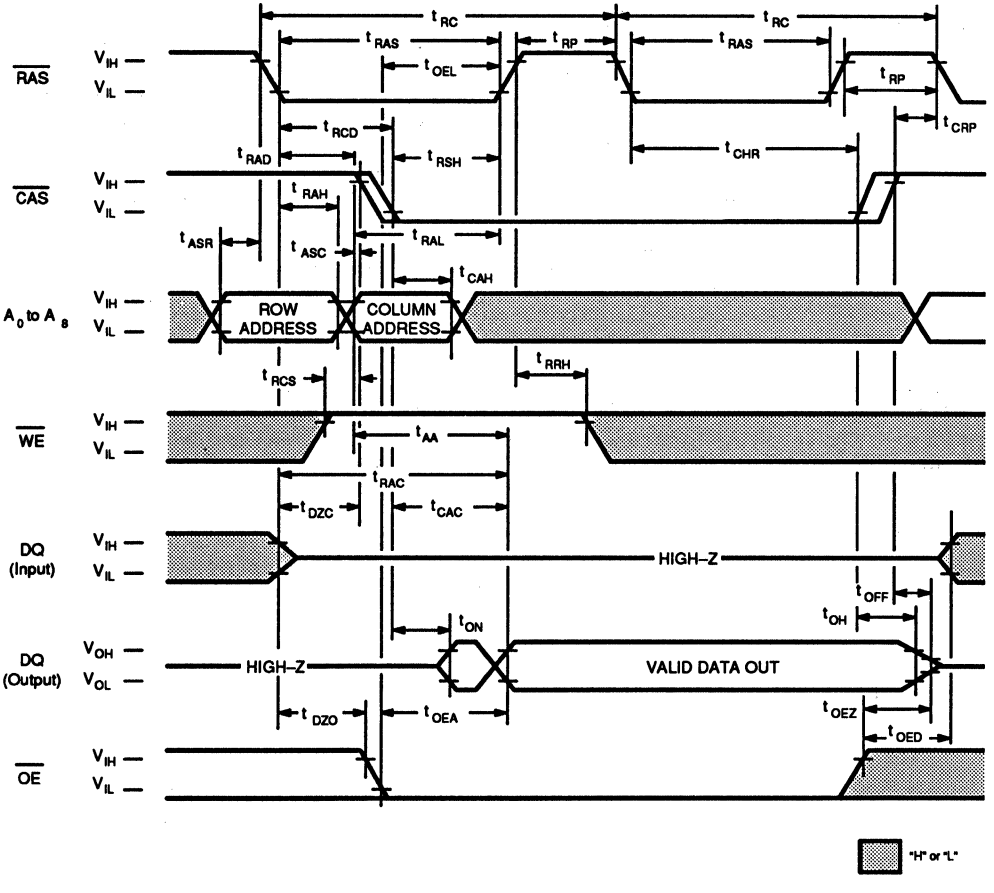


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

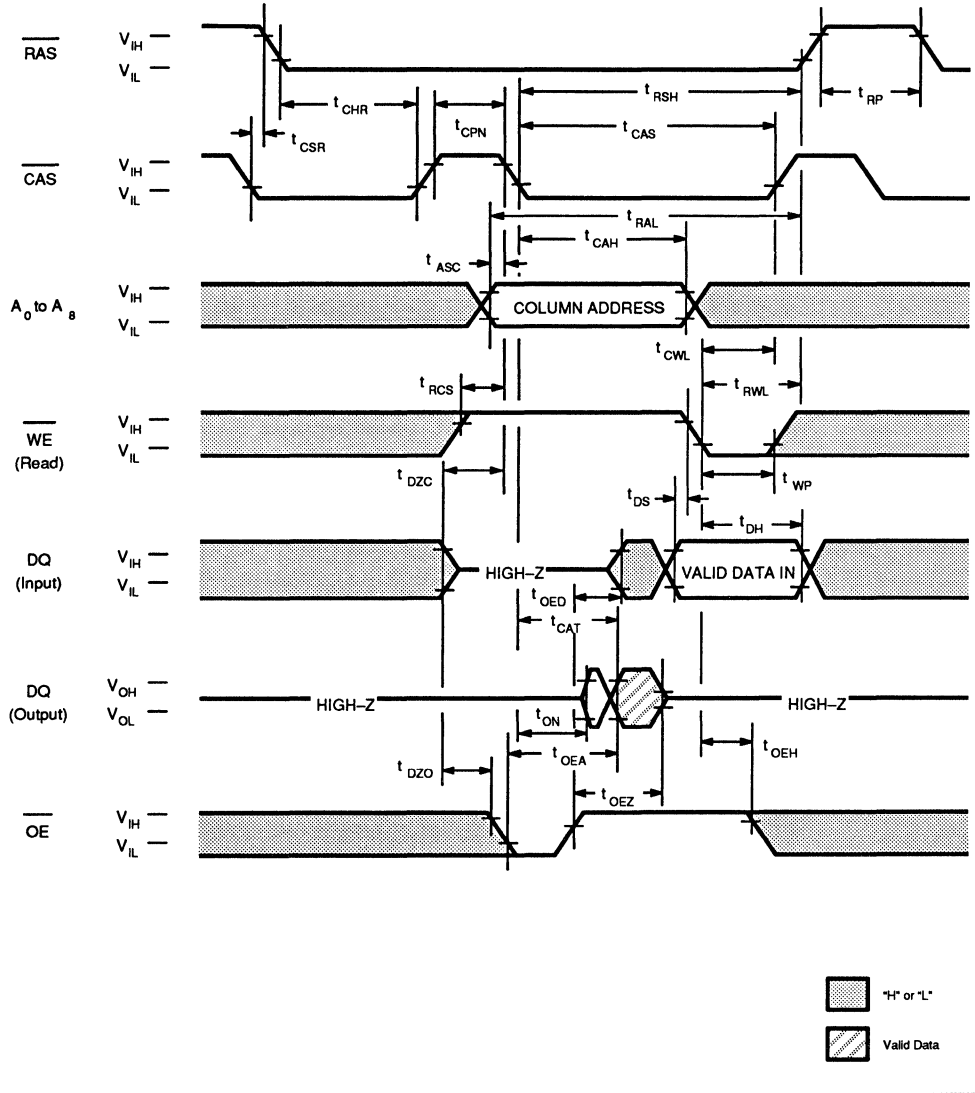
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh addresscounter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 15 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

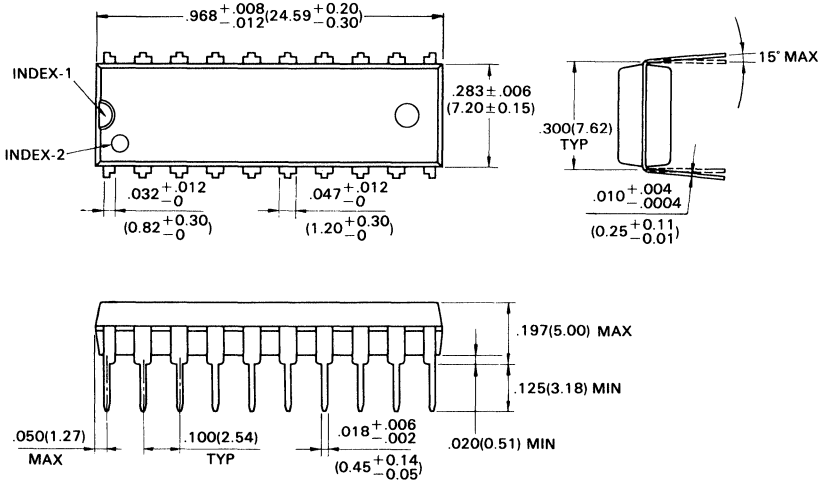


PACKAGE DIMENSIONS

(Suffix : –P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M03)

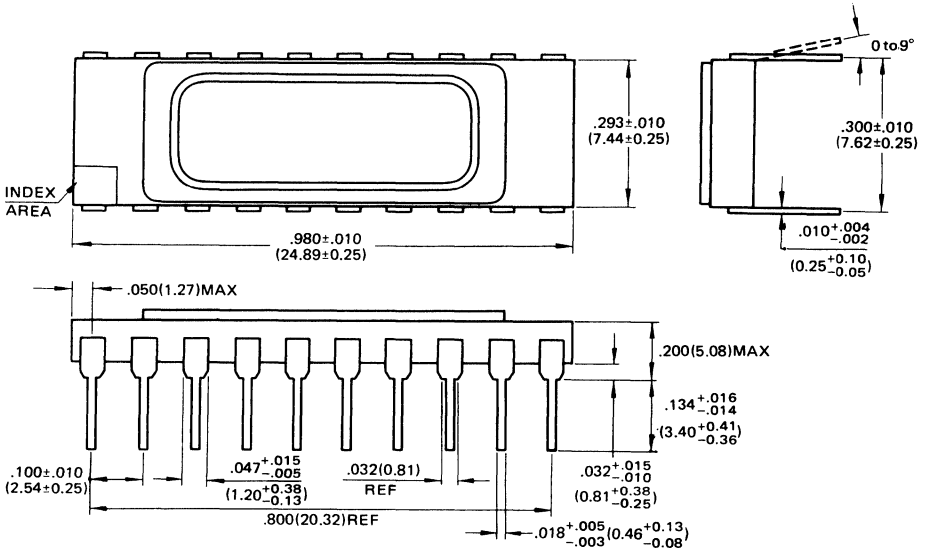


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-A03)



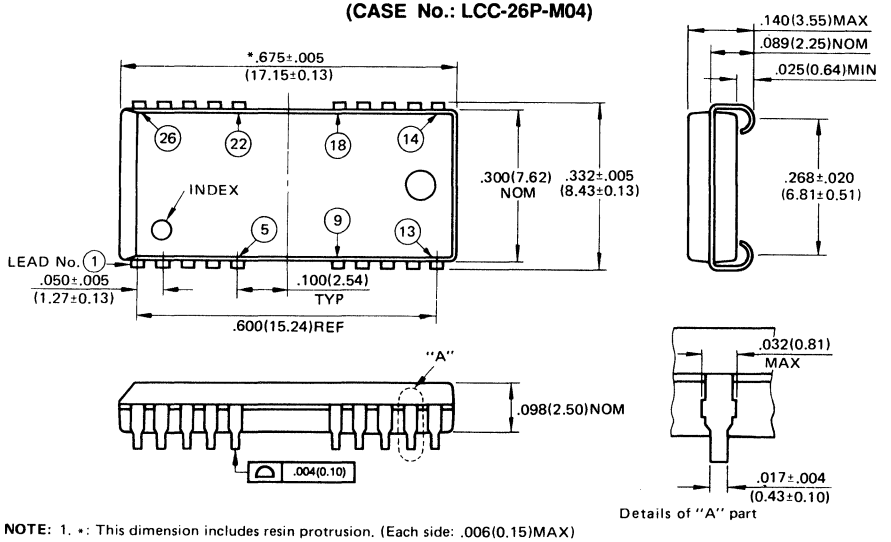
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

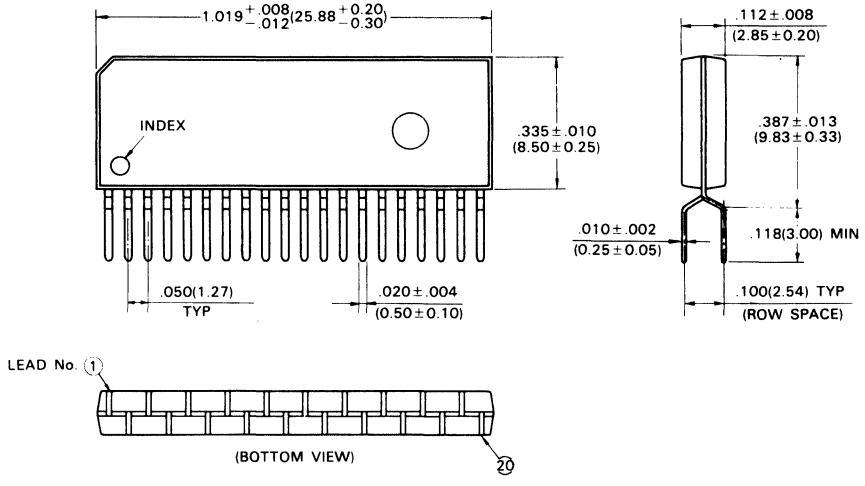
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

2

2

November 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C4256A-60/-70/-80/-10

CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

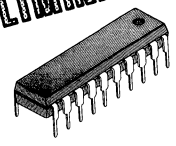
CMOS 256 x 4 Bits Fast Page Mode DRAM

The Fujitsu MB81C4256A is a CMOS, fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4256A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed and high bandwidth output with low power dissipation.

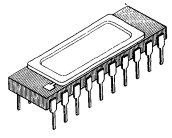
Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C4256A high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

PRELIMINARY

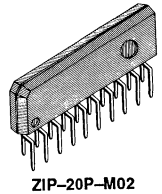


DIP-20P-M03



DIP-20C-A03

LCC-26P-M04



ZIP-20P-M02

* FPT-24P-M04 /*FPT-24P-M05
*: Available for 70/80/100ns versions

Features

Parameter	MB81C4256A -60	MB81C4256A -70	MB81C4256A -80	MB81C4256A -10
$\overline{RAS}$ Access Time	60 ns max.	70 ns max.	80 ns max.	100 ns max.
Random Cycle Time	130 ns min.	140 ns min.	155 ns min.	180 ns min.
Address Access Time	30 ns max.	35 ns max.	40 ns max.	50 ns max.
$\overline{CAS}$ Access Time	15 ns max.	20 ns max.	20 ns max.	25 ns max.
Fast Page Mode Cycle Time	45 ns min.	50 ns min.	55 ns min.	65 ns min.
Low Power Dissipation • Operating Current	407 mW max.	374 mW max.	341 mW max.	297 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

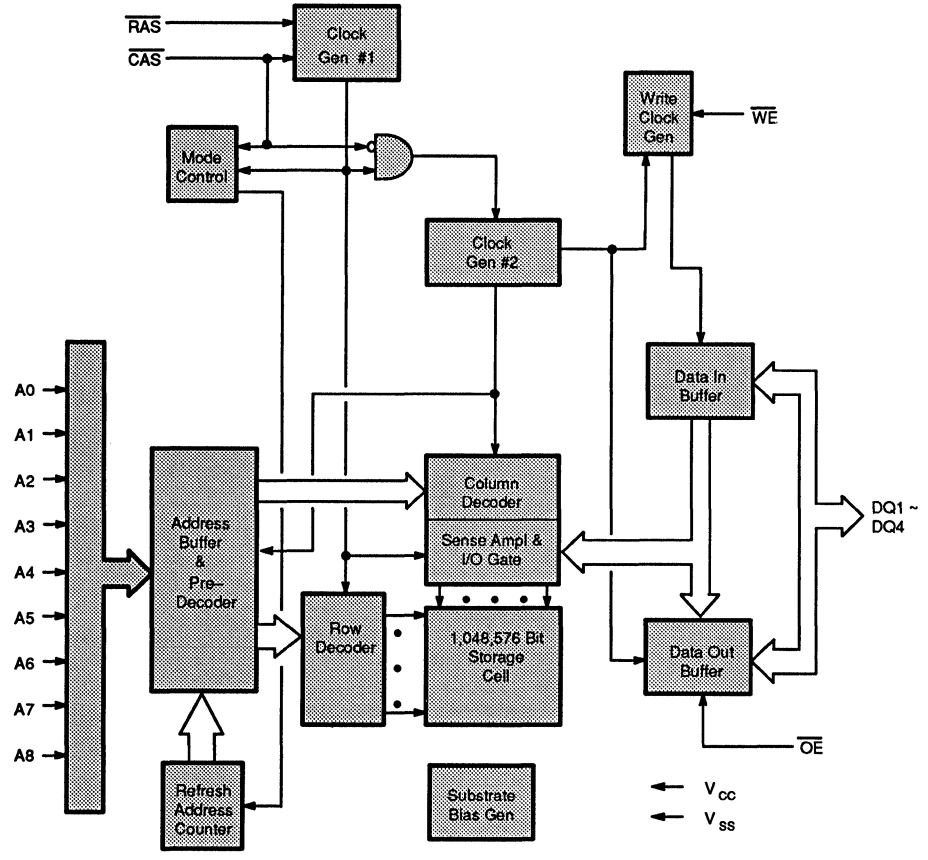
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB81C4256A DYNAMIC RAM – BLOCK DIAGRAM

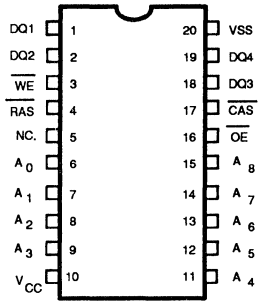


CAPACITANCE (T_A = 25°C, f = 1MHz)

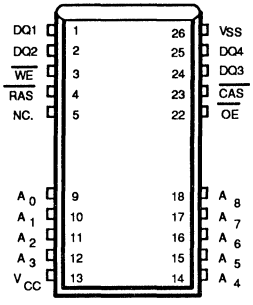
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

20–Pin DIP :
(TOP VIEW)

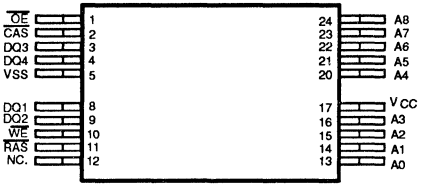


26–Pin SOJ:
(TOP VIEW)

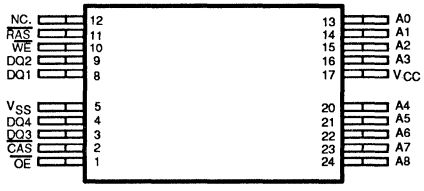


24–Pin FPT :
(TOP VIEW)

<Normal Bend : FPT–24P–M04>

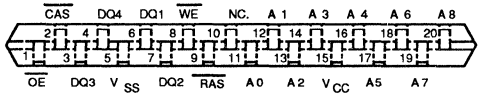


<Reverse Bend : FPT–24P–M05>



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

20–Pin ZIP:
(TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

2

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins under test = 0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average Power supply Current) [2]	MB81C4256A–60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	74	mA
	MB81C4256A–70					68	
	MB81C4256A–80					62	
	MB81C4256A–10					54	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ =V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB81C4256A–60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	74	mA
	MB81C4256A–70					68	
	MB81C4256A–80					62	
	MB81C4256A–10					54	
Fast Page Mode current [2]	MB81C4256A–60	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	60	mA
	MB81C4256A–70					55	
	MB81C4256A–80					50	
	MB81C4256A–10					43	
Refresh current #2 (Average power supply current) [2]	MB81C4256A–60	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	74	mA
	MB81C4256A–70					68	
	MB81C4256A–80					62	
	MB81C4256A–10					54	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256A-60		MB81C4256A-70		MB81C4256A-80		MB81C4256A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	130	—	140	—	155	—	180	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	170	—	180	—	205	—	240	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	60	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	15	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	—	20	—	25	ns
10	Transition Time		t_T	2	50	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	60	—	65	—	70	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	20	50	22	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	19	t_{CPN}	20	—	20	—	20	—	20	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	12	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	17	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	10	—	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	12	—	12	—	15	—	20	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256A-60		MB81C4256A-70		MB81C4256A-80		MB81C4256A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	12	—	15	—	ns
38	Access Time from $\overline{OE}$	9	t_{OEA}	—	15	—	20	—	20	—	25	ns
39	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	15	—	15	—	20	—	25	ns
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	0	—	ns
42	$\overline{OE}$ to Data In Delay Time		t_{OED}	15	—	15	—	20	—	25	—	ns
43	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	0	—	ns
44	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	0	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	45	—	50	—	55	—	65	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	82	—	87	—	100	—	120	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	40	—	45	—	50	—	60	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200μs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min)
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh, $\overline{CAS}$ -before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

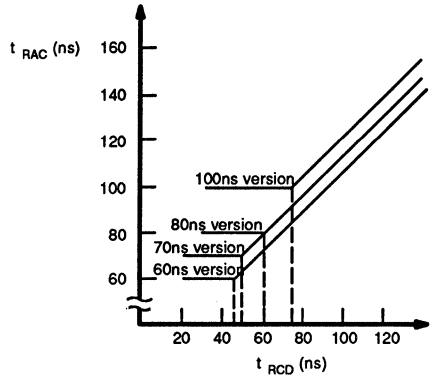
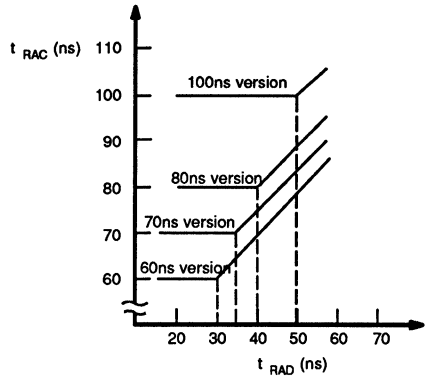


Fig. 3 – t_{RAC} vs. t_{RAD}



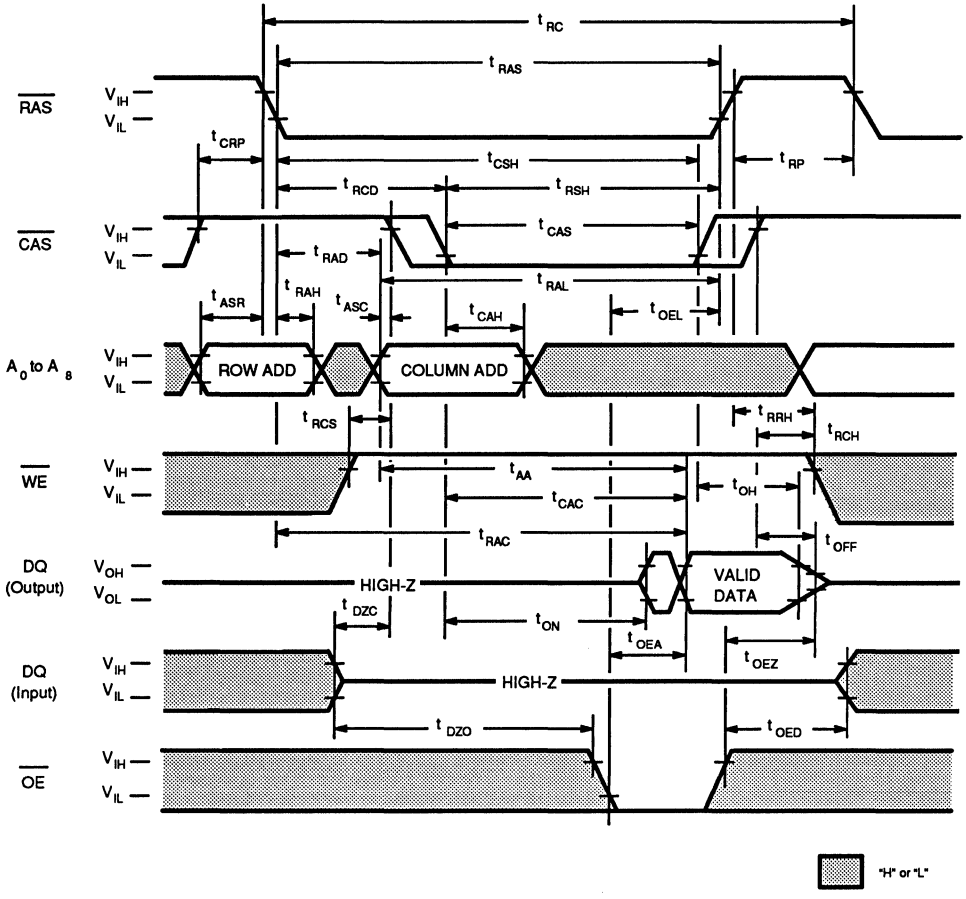
2

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	WE	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High–Z	Yes	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$(tRAC), $\overline{CAS}$(tCAC), $\overline{OE}$ (tOEA) or column addresses (tAA) under the following conditions:

If tRCD > tRCD (max), access time = tCAC.

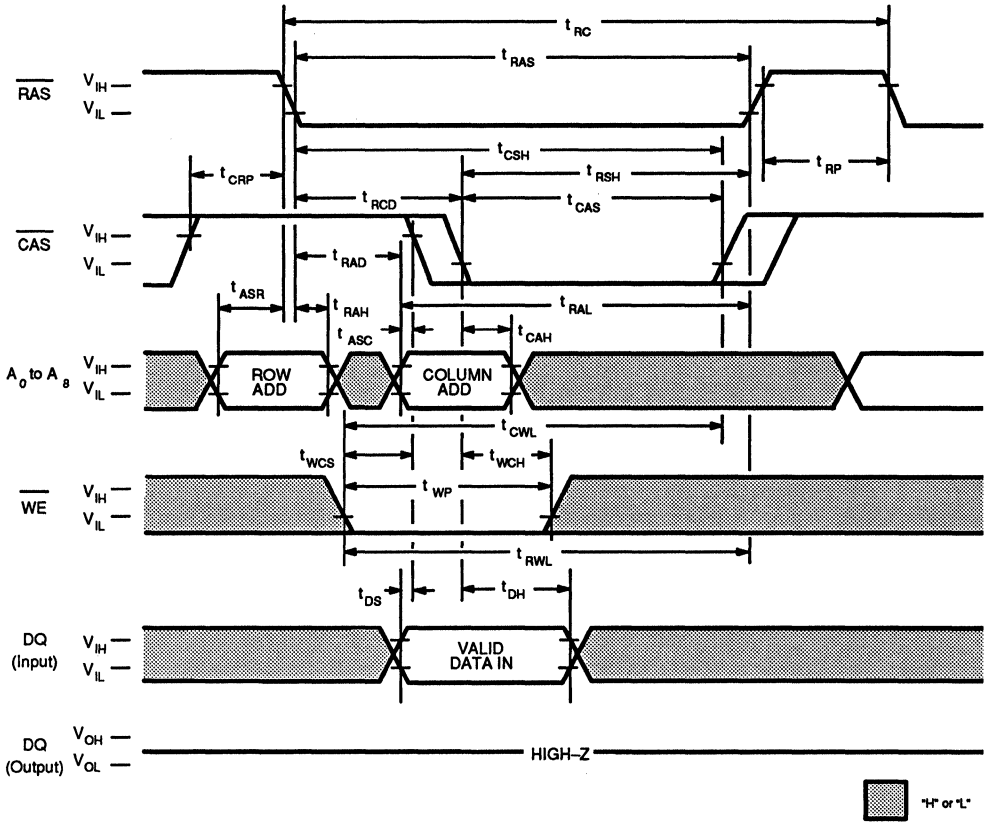
If tRAD > tRAD (max), access time = tAA.

If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after tOH is satisfied.

2

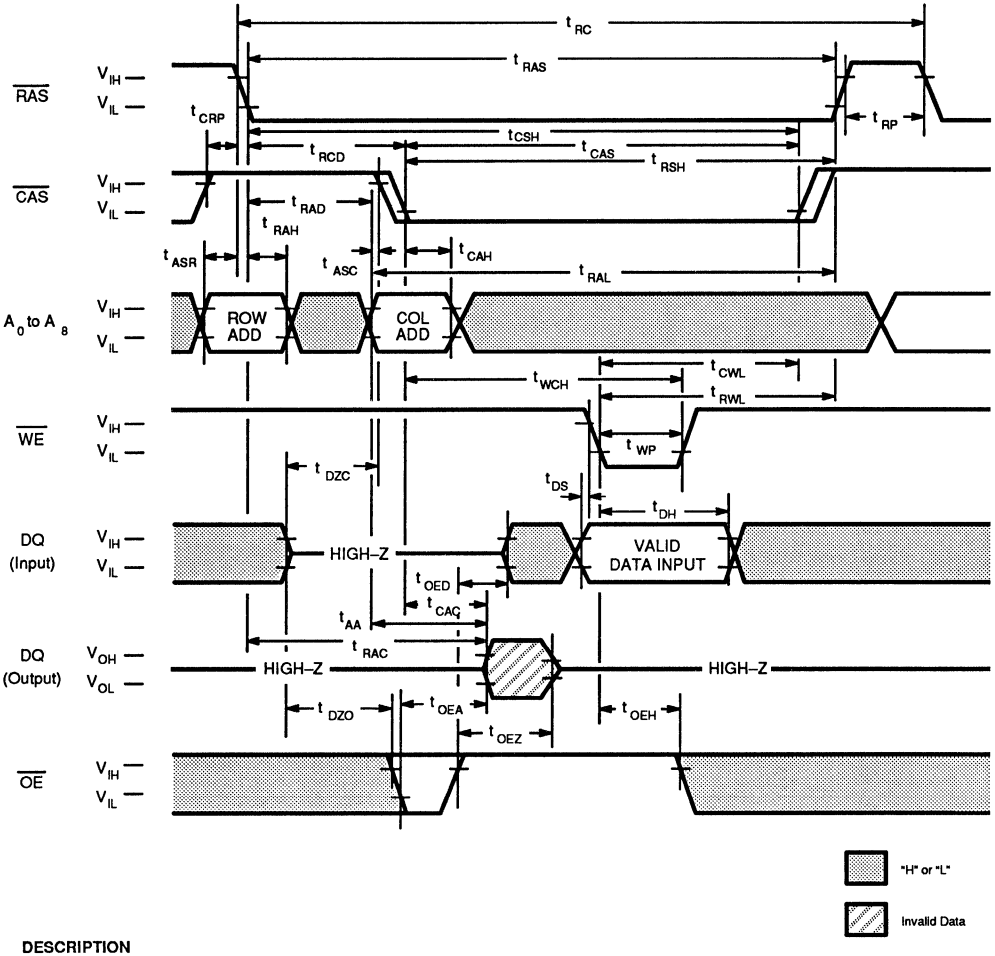
Fig. 5 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above tWCS satisfied, data on the DQ pin is latched with the falling edge of $\overline{CAS}$ and written into memory.

Fig. 6 – $\overline{OE}$ (DELAYED WRITE CYCLE)

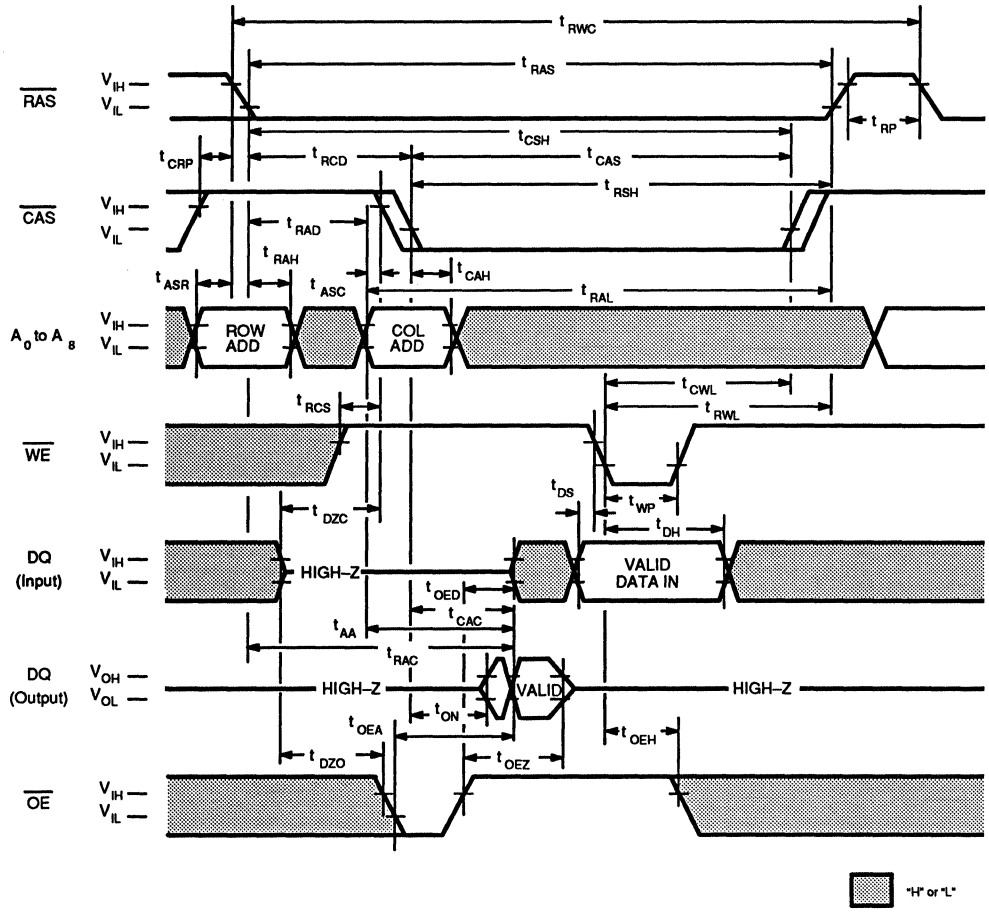


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, tWCS is not satisfied ; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

2

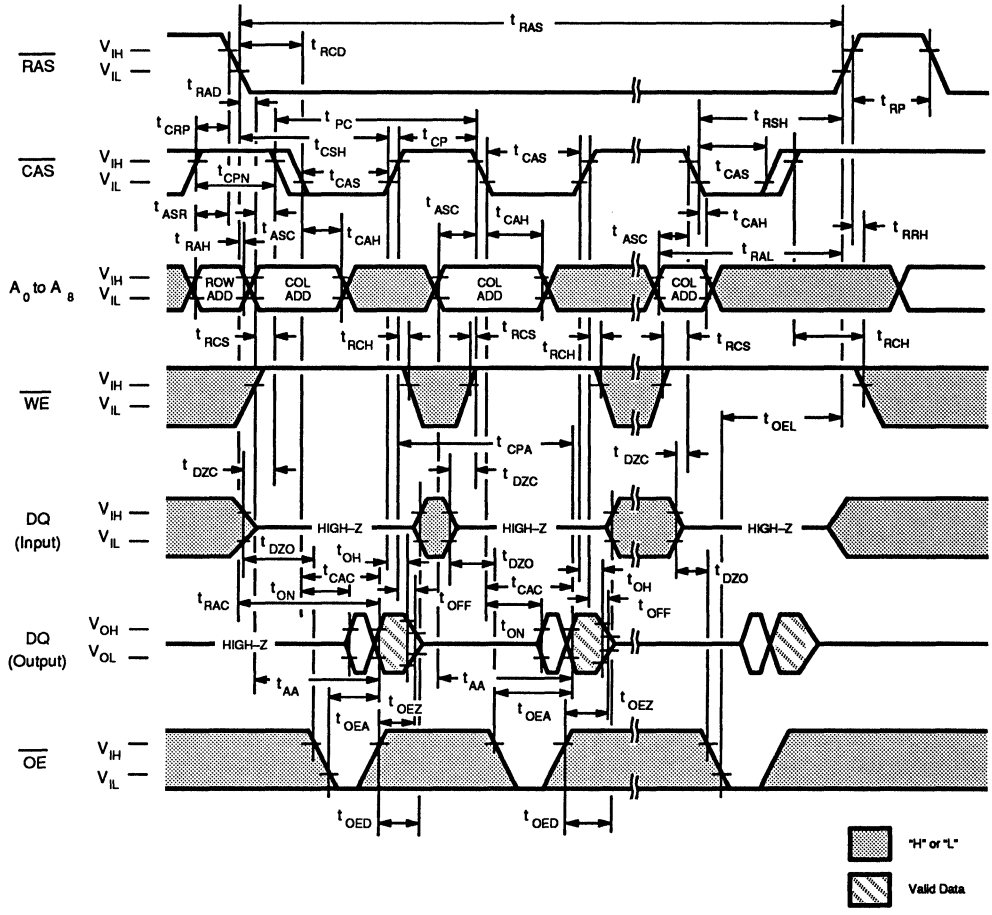
Fig. 7 – READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 8 – FAST PAGE MODE READ CYCLE

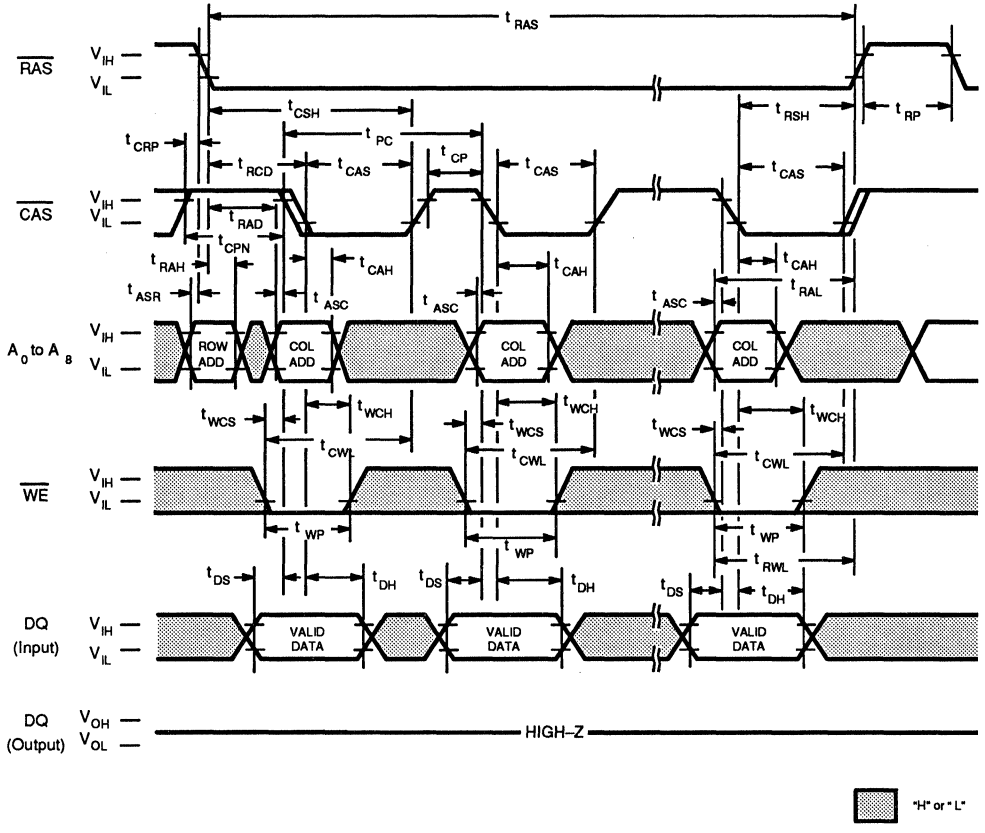


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occuring.

2

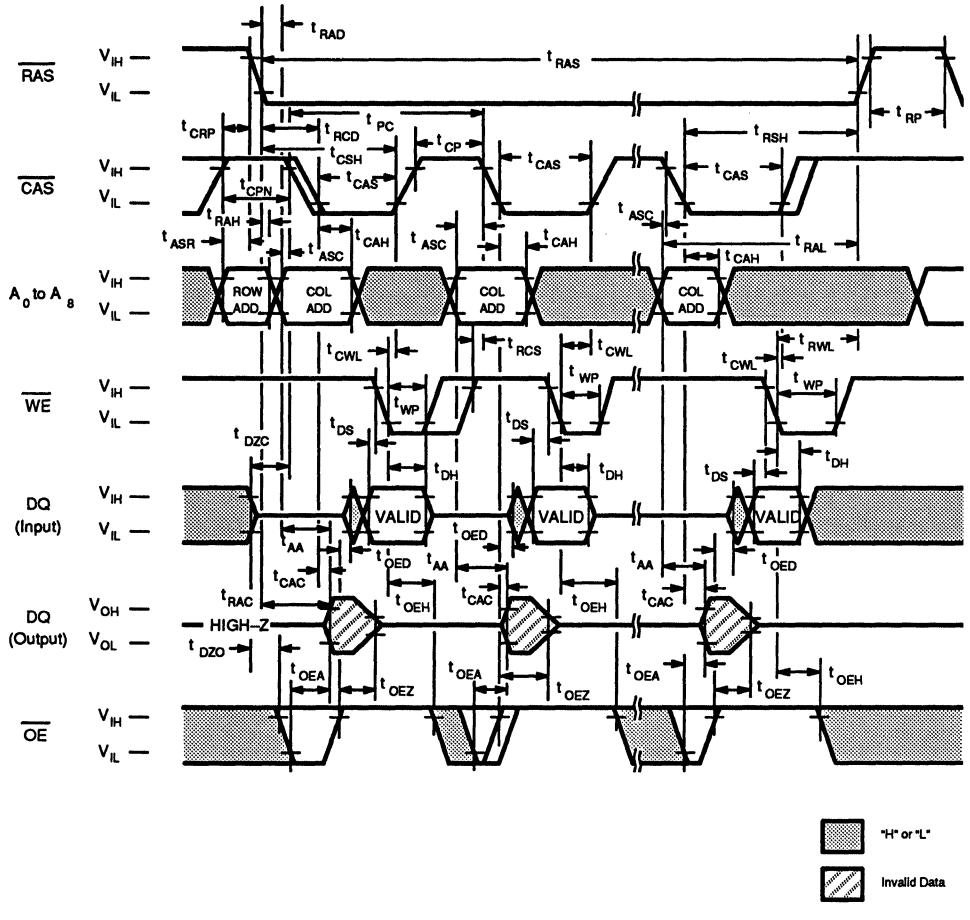
Fig. 9 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fastpage mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, tCWL must be satisfied.

Fig. 10 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

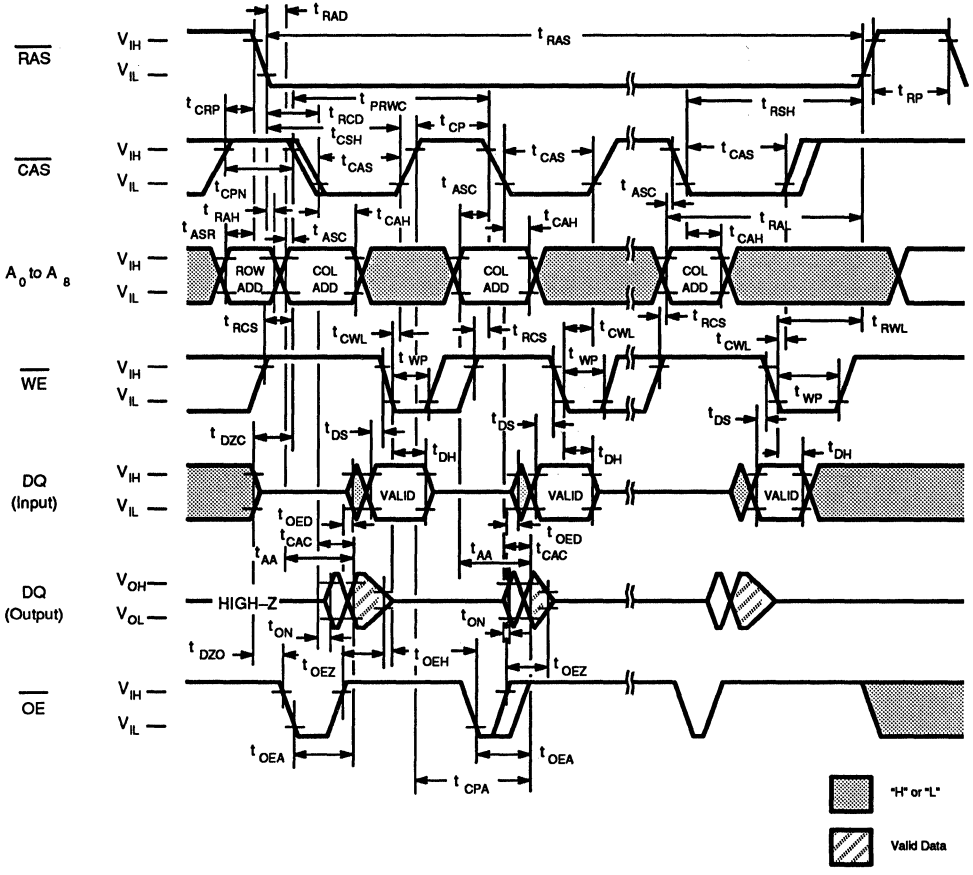


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

2

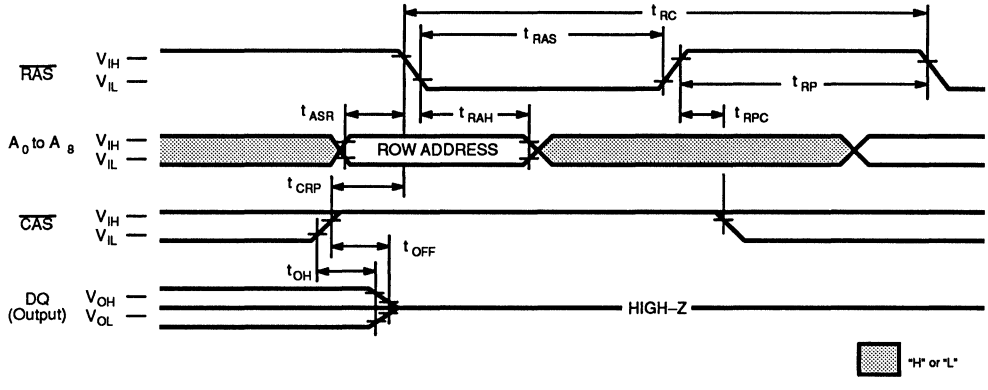
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

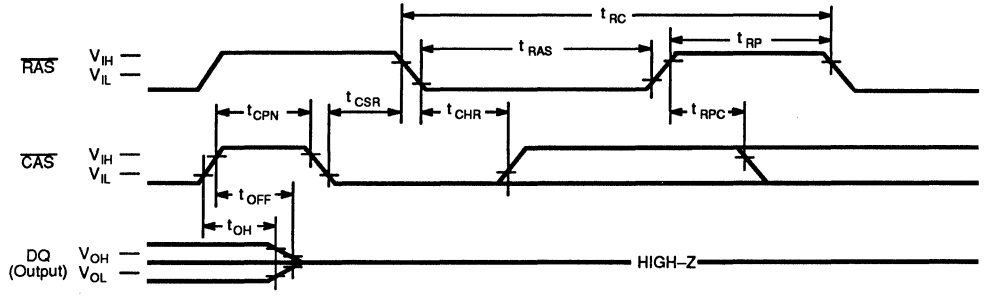


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

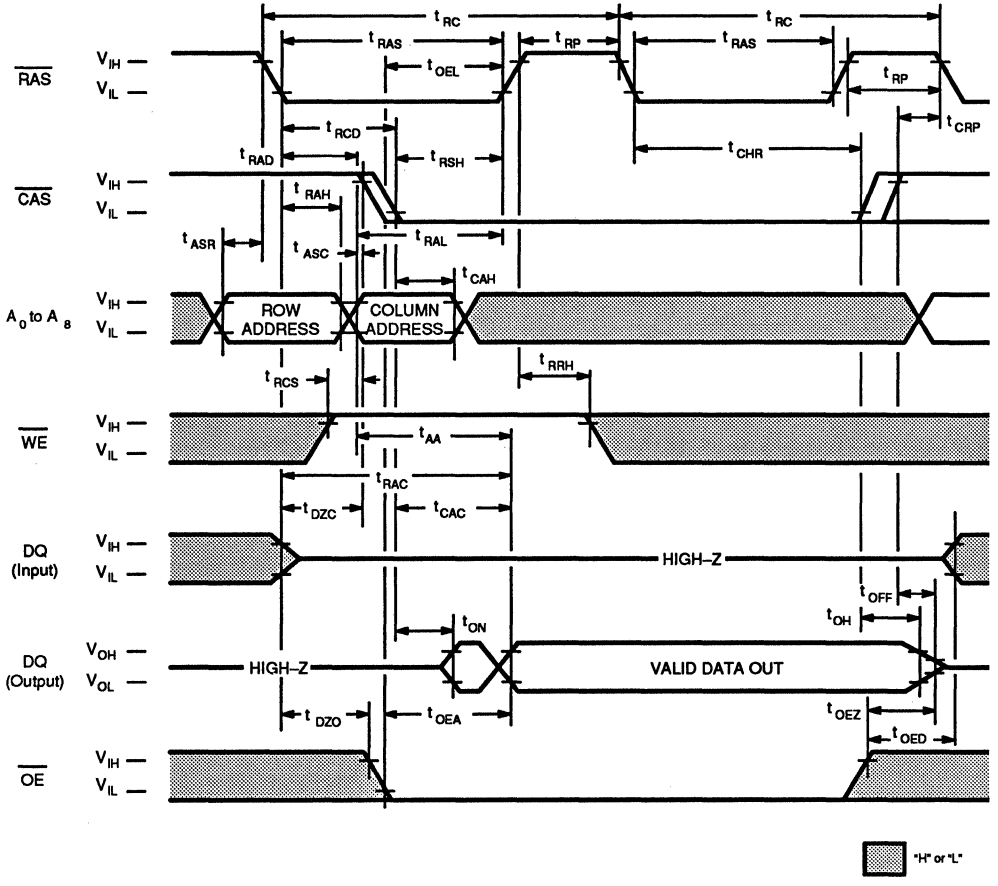
Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

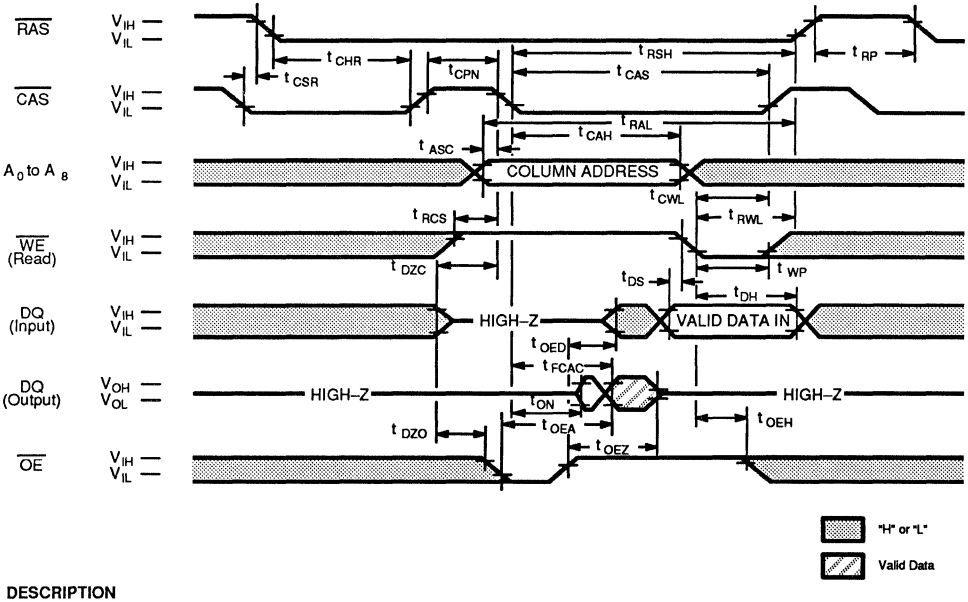
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh addresscounter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 15 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses (DQ1 to DQ4) at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (read–modify–write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 (DQ1 to DQ4) memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

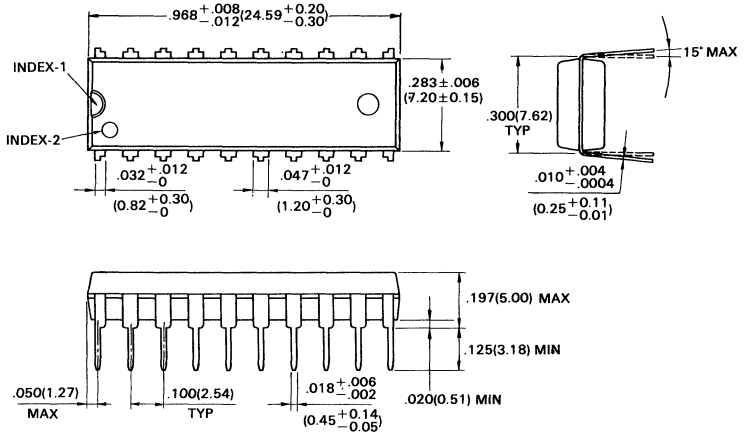
No.	Parameter	Symbol	MB81C4256A–60		MB81C4256A–70		MB81C4256A–80		MB81C4256A–10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	40	—	45	—	50	—	60	ns

Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix : –P)

20–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20P–M03)

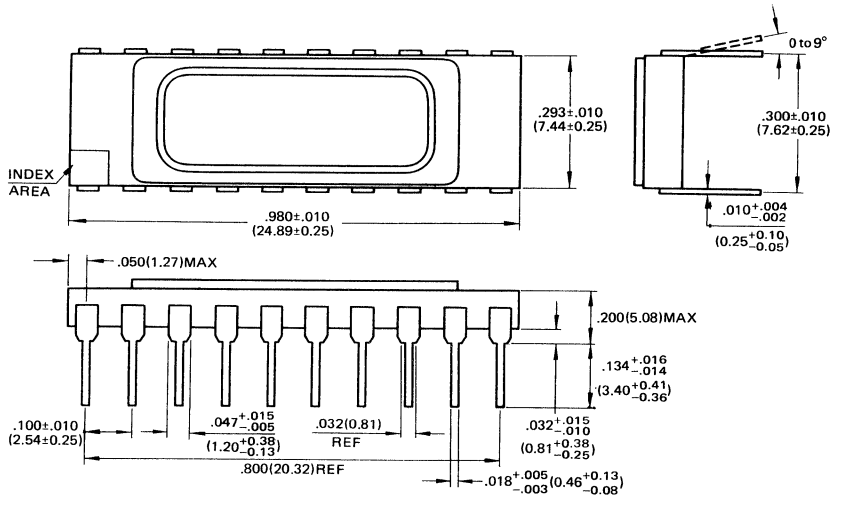


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20–LEAD CERAMIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20C–A03)

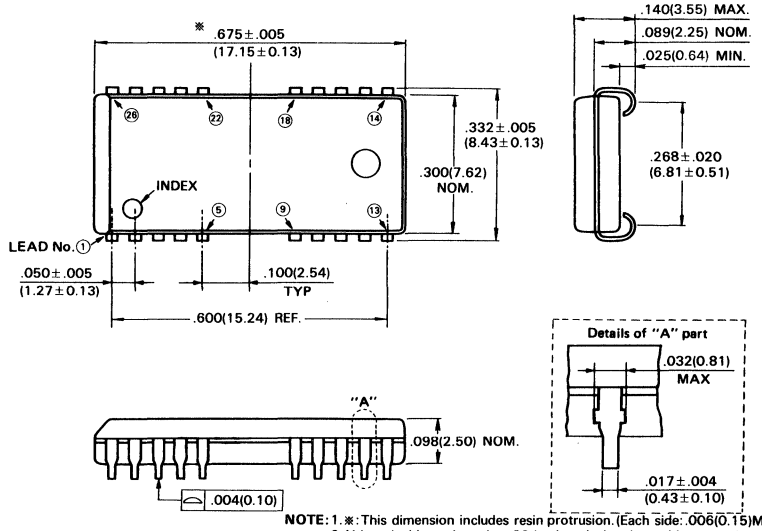


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)
(CASE No.: LCC–26P–M04)

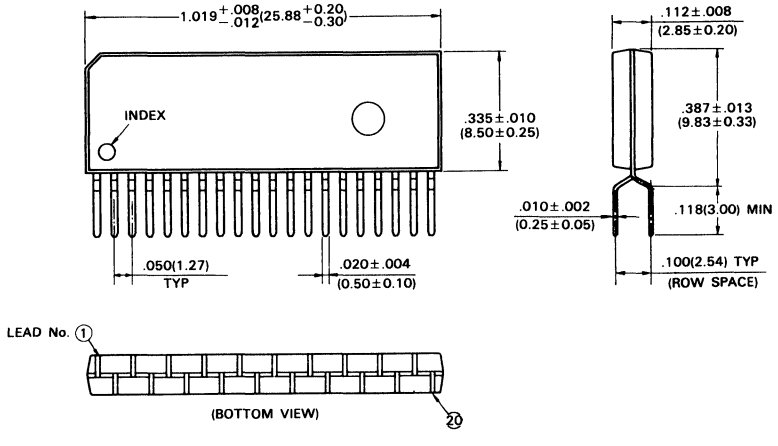


NOTE: 1.※: This dimension includes resin protrusion.(Each side: .006(0.15)MAX)
2.Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
3.Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



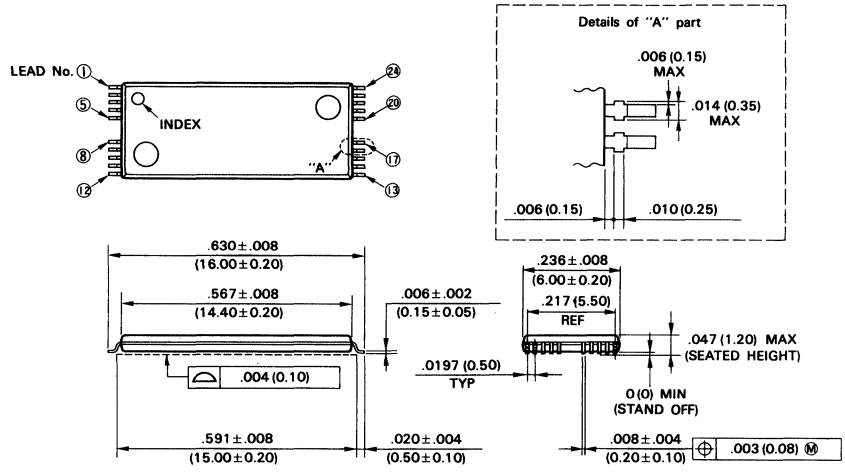
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: – PFTN)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M04)

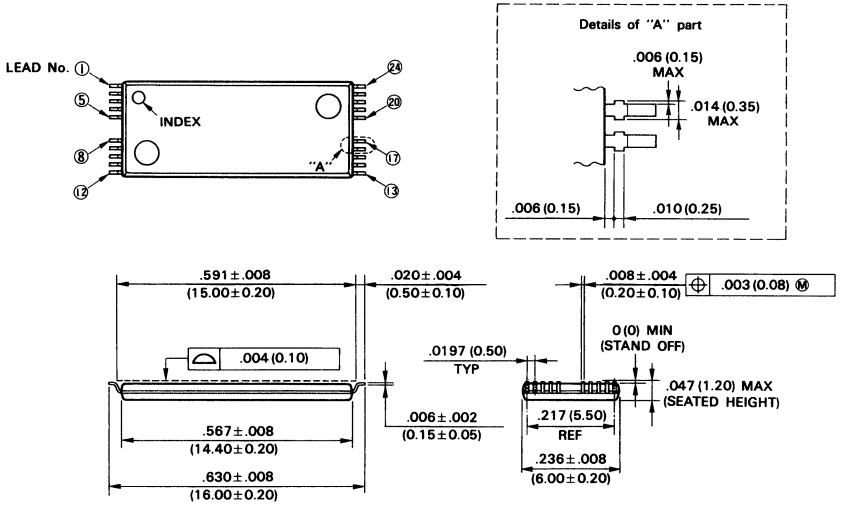


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: – PFTR)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M05)



Dimensions in inches (millimeters)

2

2

November 1990
Edition 2.0

FUJITSU

DATA SHEET

MB81C4256A-70L/-80L/-10L

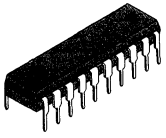
CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 256K x 4 Bits Fast Page Mode DRAM

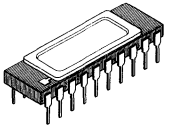
The Fujitsu MB81C4256A is a CMOS, fully decoded dynamic RAM organized as 256K words x 4 bits. The MB81C4256A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed and high bandwidth output with low power dissipation, as well as for memory systems of battery operated computers requiring very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C4256A high α-ray soft error immunity and extended refresh time. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

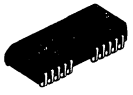
PRELIMINARY



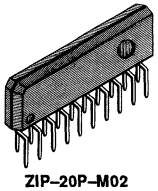
DIP-20P-M03



DIP-20C-A03



LCC-26P-M04



ZIP-20P-M02

FPT-24P-M04 / FPT-24P-M05

2

Features

Parameter	MB81C4256A -70L	MB81C4256A -80L	MB814256A -10L
$\overline{RAS}$ Access Time	70 ns max.	80 ns max.	100 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.
Address Access Time	35 ns max.	40 ns max.	50 ns max.
$\overline{CAS}$ Access Time	20 ns max.	20 ns max.	25 ns max.
Fast Page Mode Cycle Time	50 ns min.	55 ns min.	65 ns min.
Low Power Dissipation • Operating Current	374 mW max.	341 mW max.	297 mW max.
• Standby Current	5.5 mW max. (TTL level)/1.4 mW max. (CMOS level)		

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 64 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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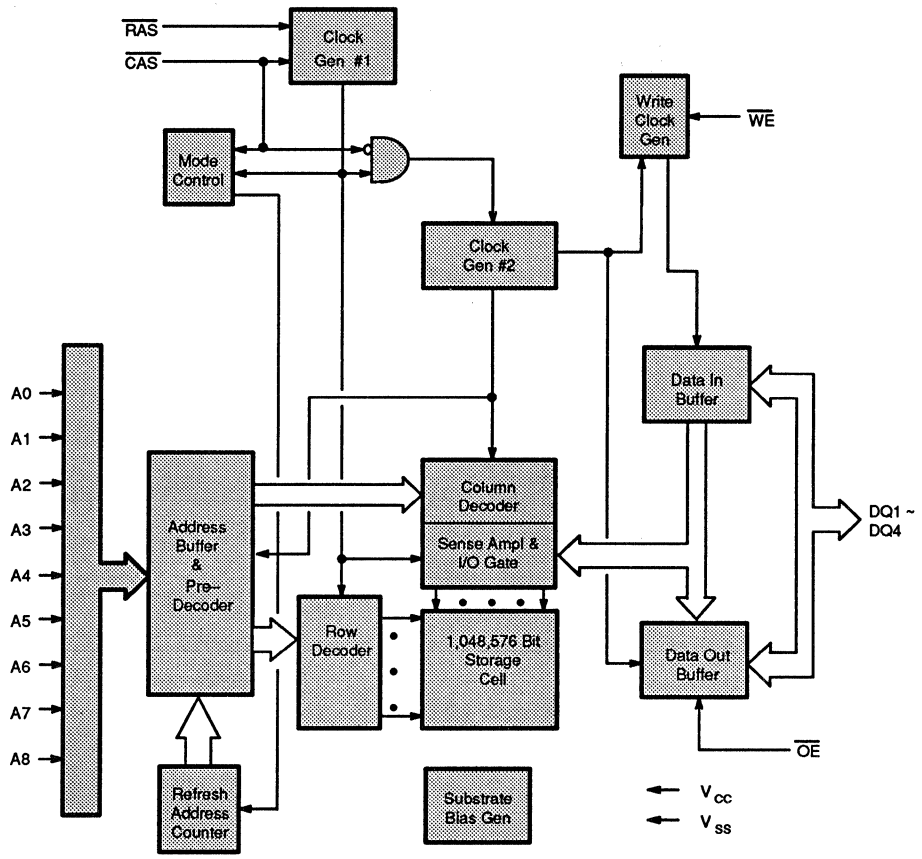
Fig. 1 – MB81C4256A DYNAMIC RAM – BLOCK DIAGRAM

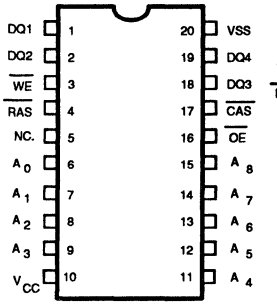


CAPACITANCE (T_A = 25°C, f = 1MHz)

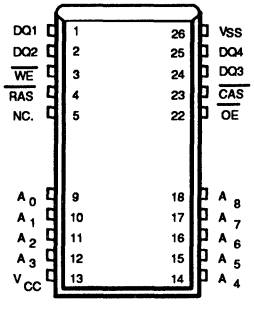
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

20–Pin DIP :
(TOP VIEW)

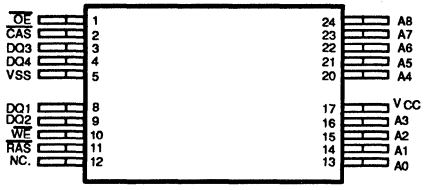


26–Pin SOJ:
(TOP VIEW)

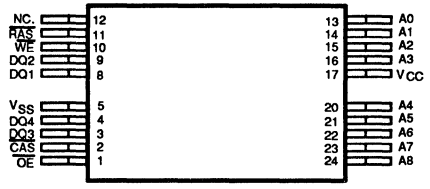


24–Pin FPT :
(TOP VIEW)

<Normal Bend : FPT–24P–M04>

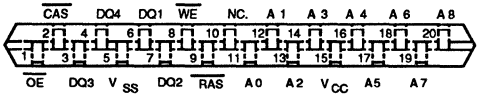


<Reverse Bend : FPT–24P–M05>



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

20–Pin ZIP:
(TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 celladdresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the fallingedge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

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DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an$\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins under test = 0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average Power supply Current) [2]	MB81C4256A–70L	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	68	mA
	MB81C4256A–80L					62	
	MB81C4256A–10L					54	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	1.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			0.25	
Refresh current #1 (Average power supply current) [2]	MB81C4256A–70L	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	68	mA
	MB81C4256A–80L					62	
	MB81C4256A–10L					54	
Fast Page Mode current [2]	MB81C4256A–70L	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	55	mA
	MB81C4256A–80L					50	
	MB81C4256A–10L					43	
Refresh current #2 (Average power supply current) [2]	MB81C4256A–70L	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	68	mA
	MB81C4256A–80L					62	
	MB81C4256A–10L					54	
Battery Back up current (Average power supply current)	MB81C4256A–70L	I_{CC6}	$\overline{RAS}$ cycling ; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} =125 µs, t_{RAS} =min. to 1 µ s, DQ1 to 4 ≥ Vcc –0.2V or ≤ 0.2V or Open Other pin ≥Vcc–0.2V or ≤ 0.2V	—	—	250	µA
	MB81C4256A–80L						
	MB81C4256A–10L						

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256A -70L		MB81C4256A -80L		MB81C4256A -10L		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	64	—	64	—	64	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	180	—	205	—	240	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	20	—	25	ns
10	Transition Time		t_T	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	50	22	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	19	t_{CPN}	20	—	20	—	20	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	35	17	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	12	—	15	—	20	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256A -70L		MB81C4256A -80L		MB81C4256A -10L		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	12	—	15	—	ns
38	Access Time from $\overline{OE}$	9	t_{OEA}	—	20	—	20	—	25	ns
39	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	15	—	20	—	25	ns
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	ns
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	ns
42	$\overline{OE}$ to Data In Delay Time		t_{OED}	15	—	20	—	25	—	ns
43	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	ns
44	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	50	—	55	—	65	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	87	—	100	—	120	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	45	—	50	—	60	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min)
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

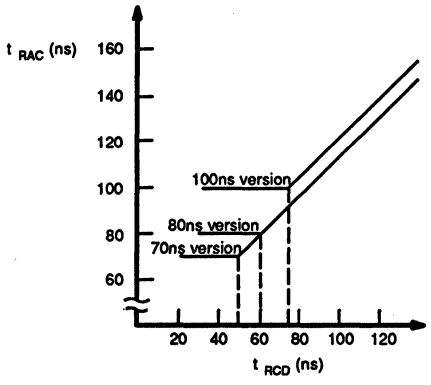
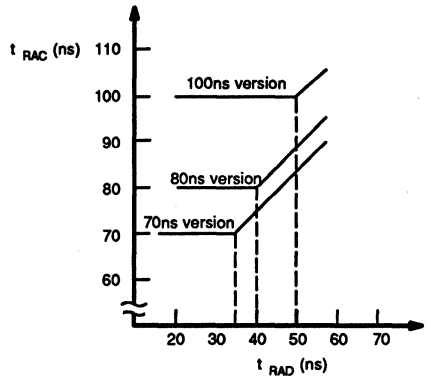


Fig. 3 – t_{RAC} vs. t_{RAD}



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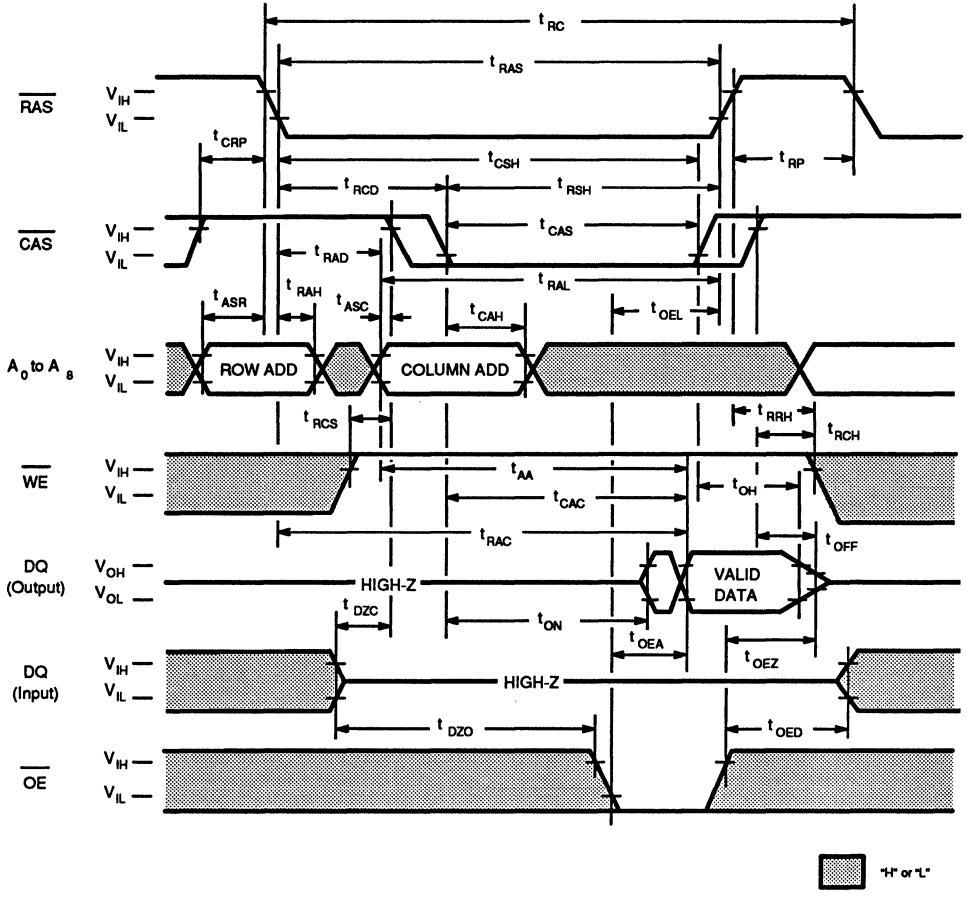
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	WE	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High–Z	Yes	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$(tRAC), $\overline{CAS}$(tCAC), $\overline{OE}$ (tOEA) or column addresses (tAA) under the following conditions:

If tRCD > tRCD (max), access time = tCAC.

If tRAD > tRAD (max), access time = tAA.

If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high–impedance state after tOH is satisfied.

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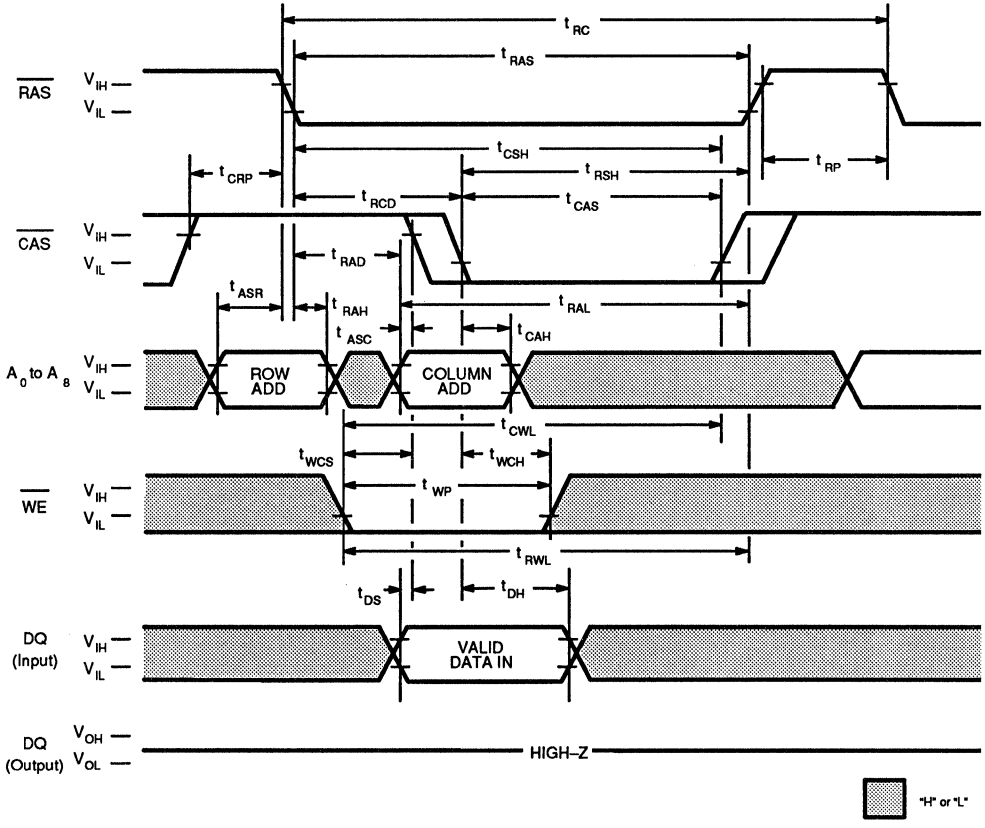
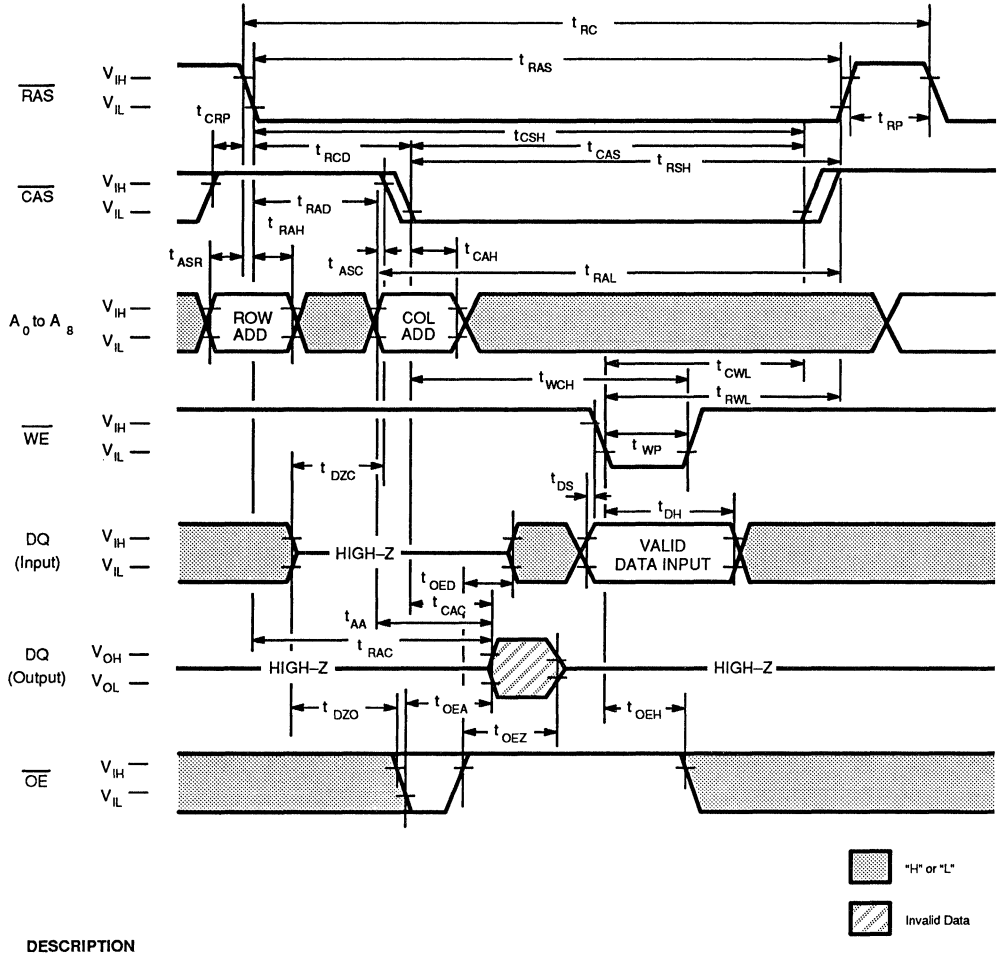
Fig. 5 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above tWCS satisfied, data on the DQ pin is latched with the falling edge of $\overline{CAS}$ and written into memory.

Fig. 6 – $\overline{OE}$ (DELAYED WRITE CYCLE)

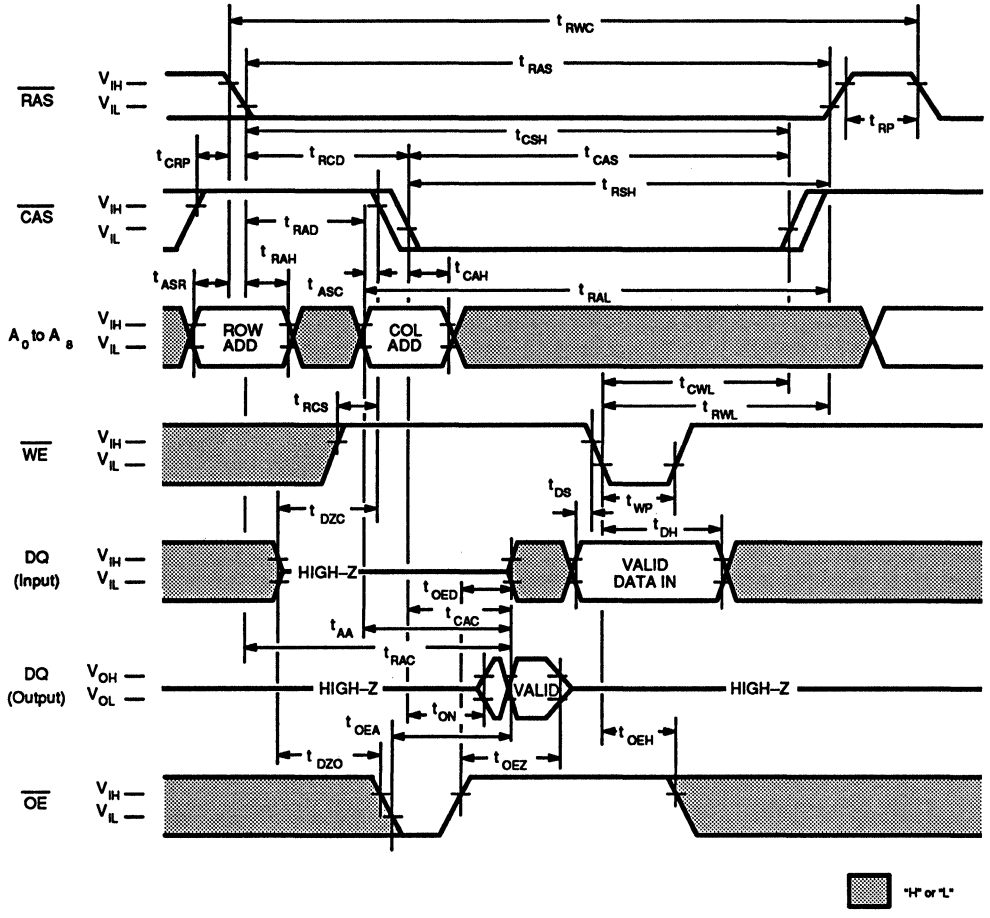


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, tWCS is not satisfied ; thus, the data on the DQpins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

2

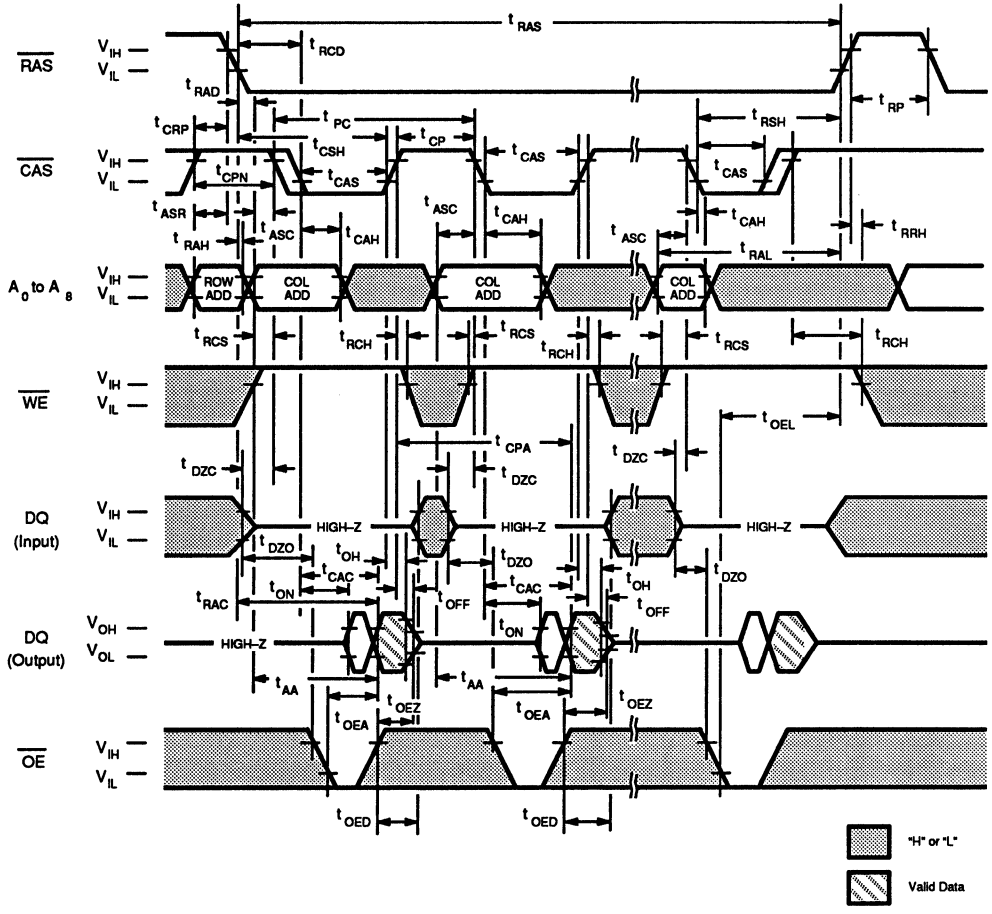
Fig. 7 – READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 8 – FAST PAGE MODE READ CYCLE

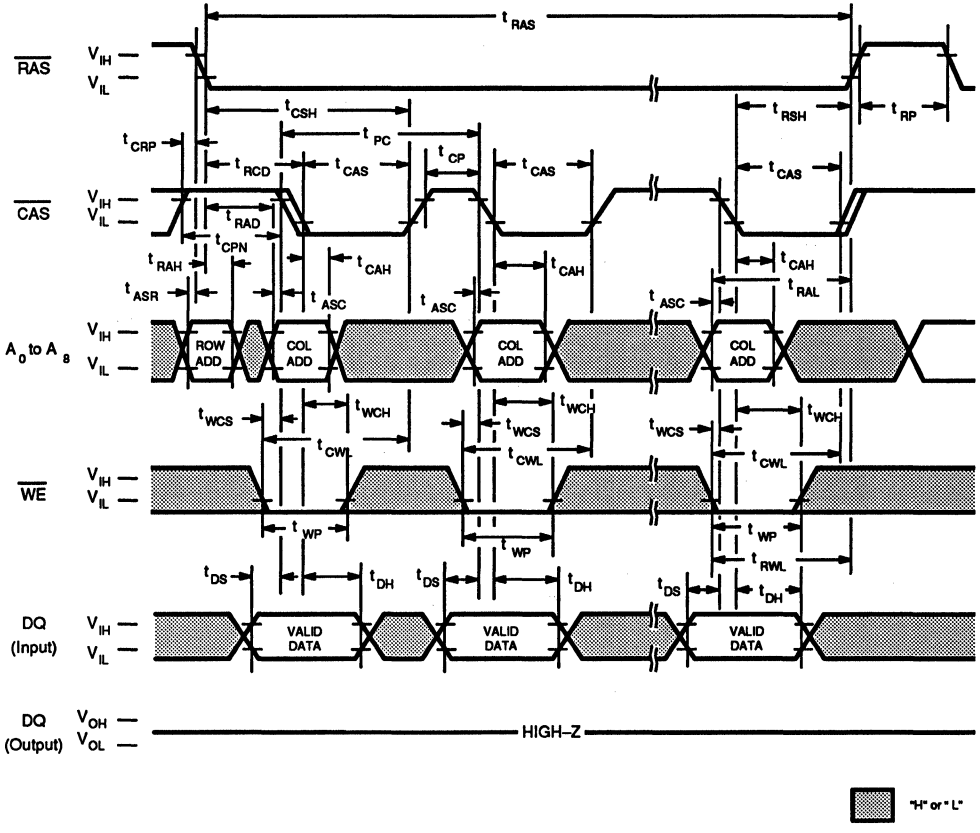


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occuring.

2

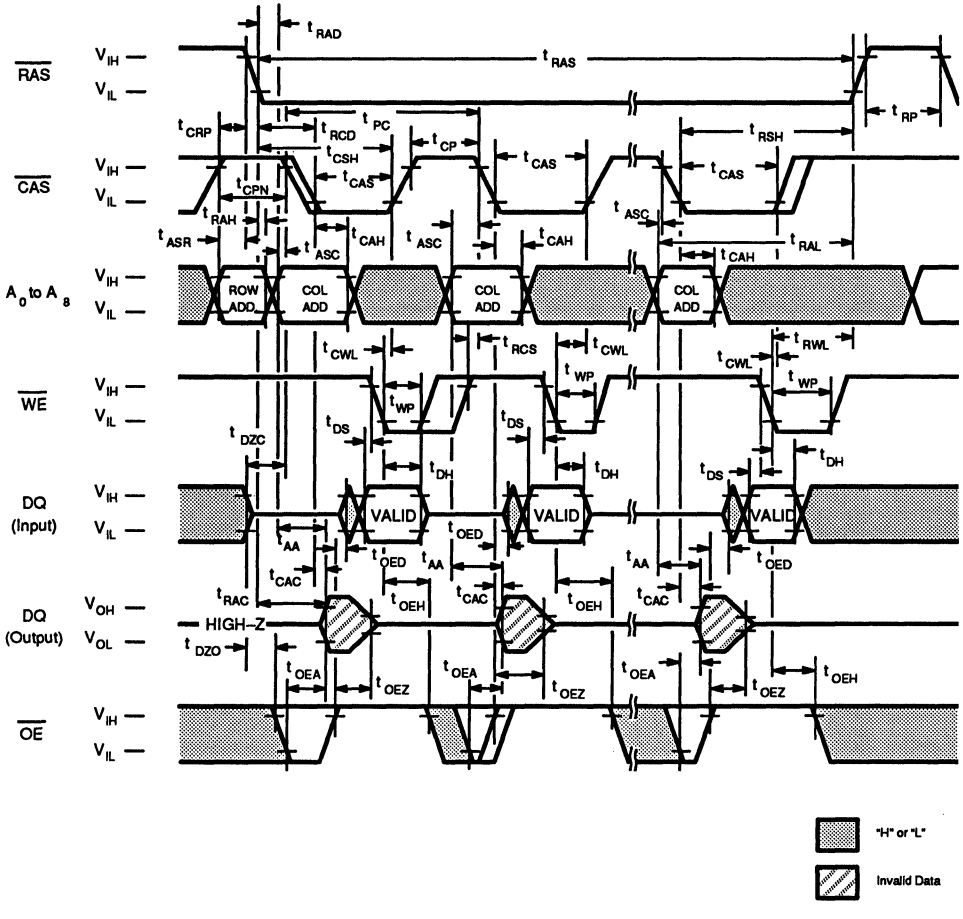
Fig. 9 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fastpage mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, tCWL must be satisfied.

Fig. 10 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

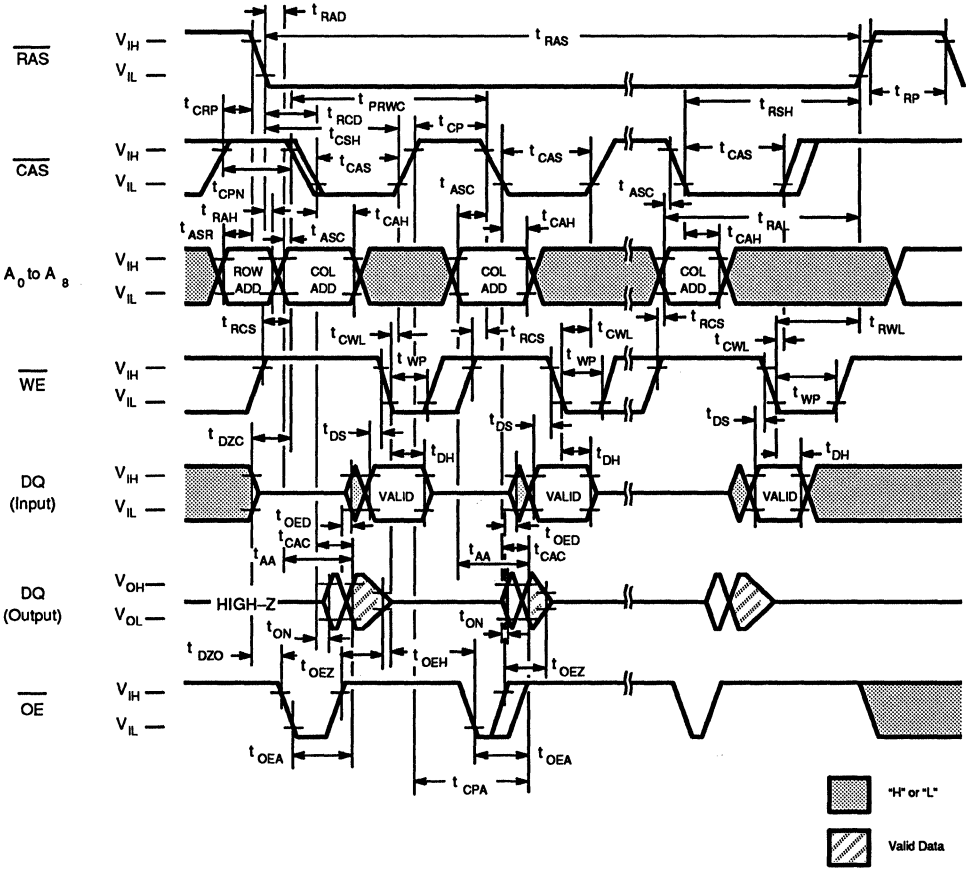


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low (tOED + tDS).

2

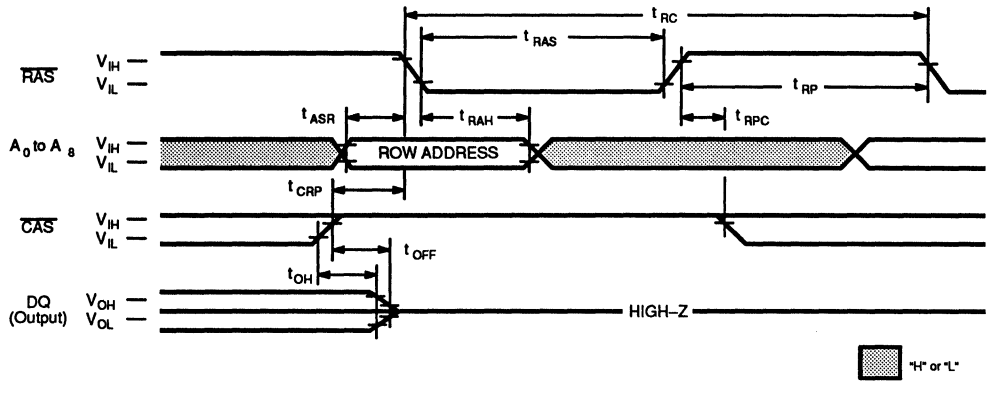
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

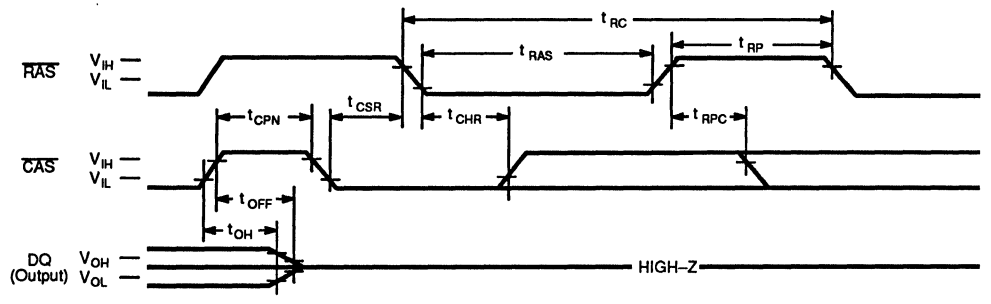


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing aread, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

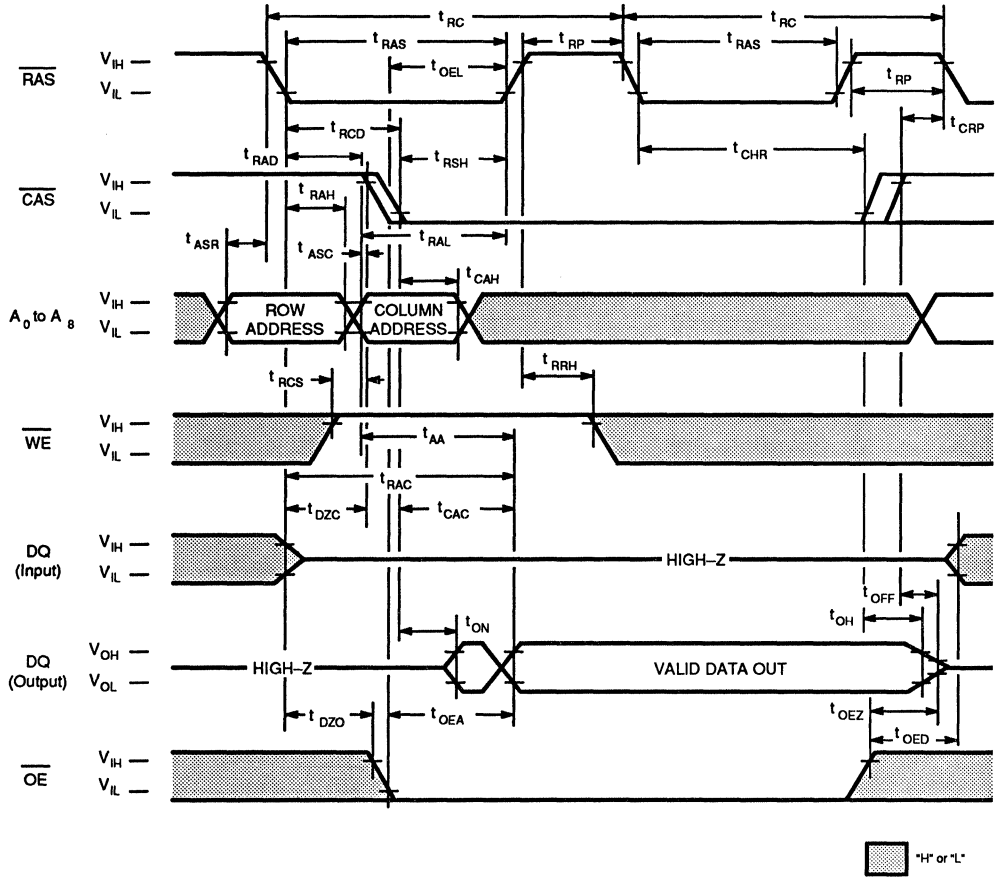


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

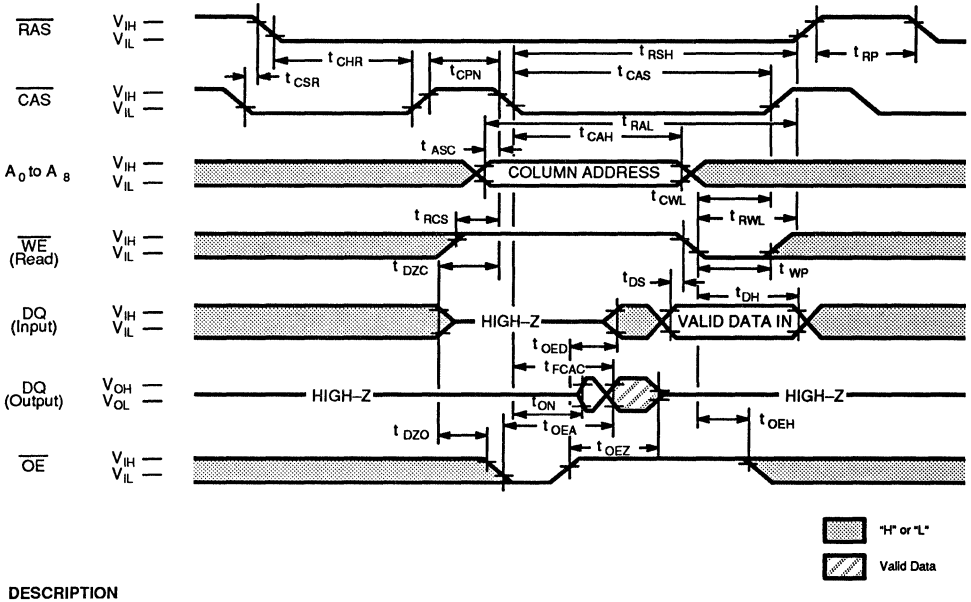
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh addresscounter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 15 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses (DQ1 to DQ4) at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (read–modify–write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 (DQ1 to DQ4) memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

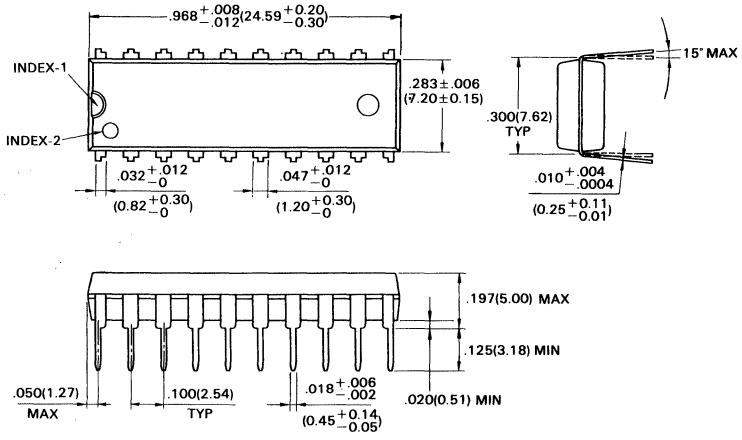
No.	Parameter	Symbol	MB81C4256A -70L		MB81C4256A -80L		MB81C4256A -10L		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	45	—	50	—	60	ns

Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix : –P)

20–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20P–M03)

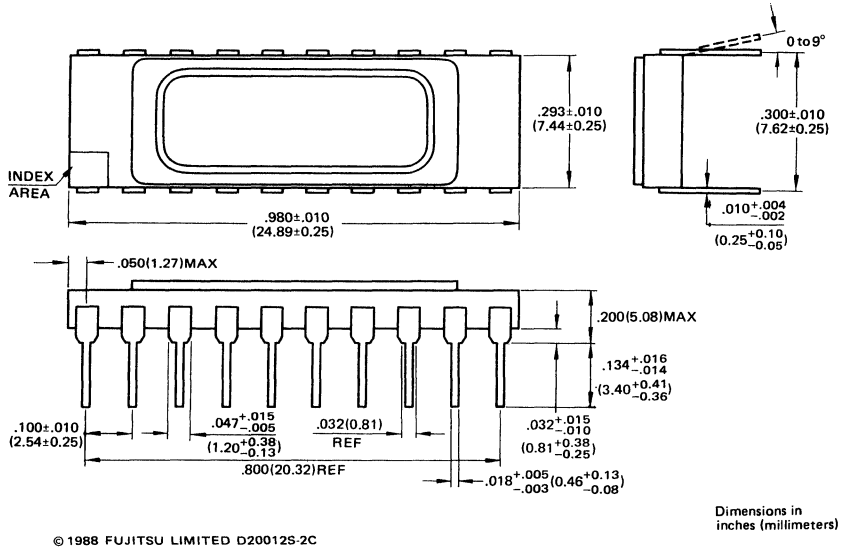


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20–LEAD CERAMIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20C–A03)



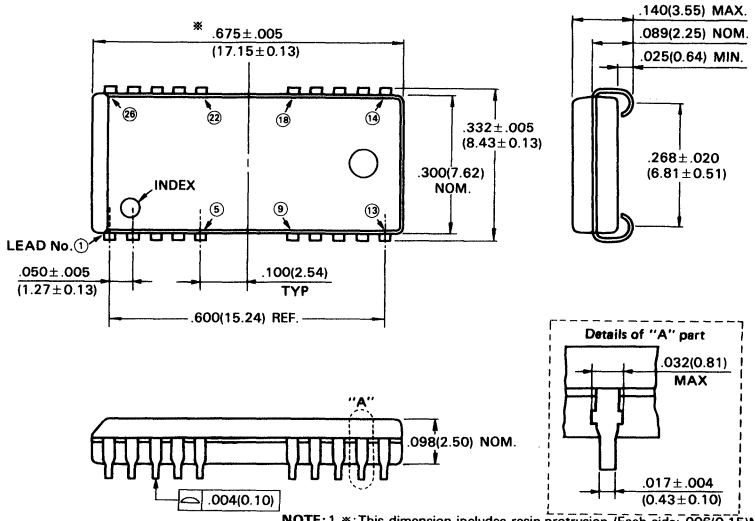
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M04)

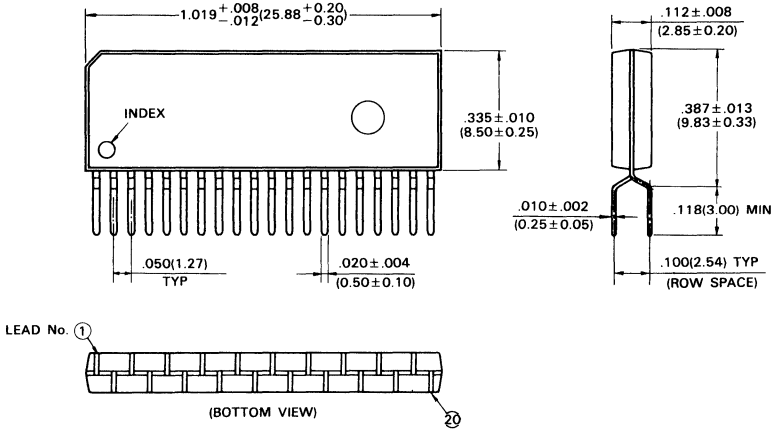


NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
3. Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



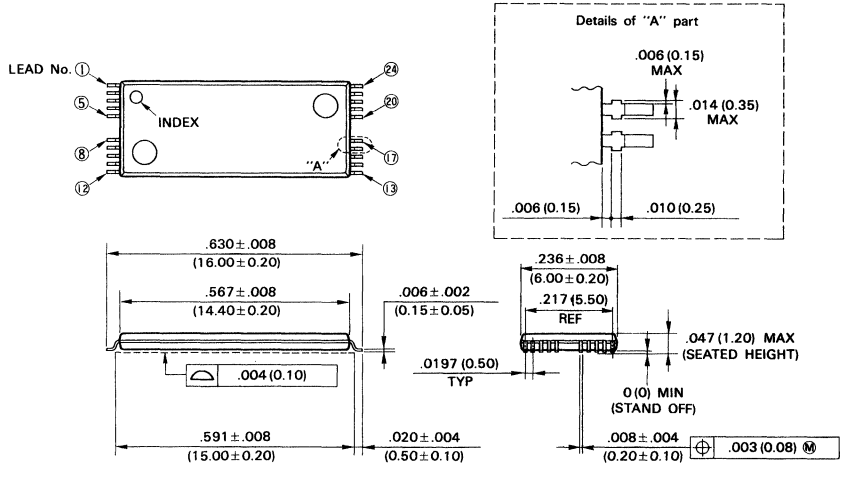
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M04)

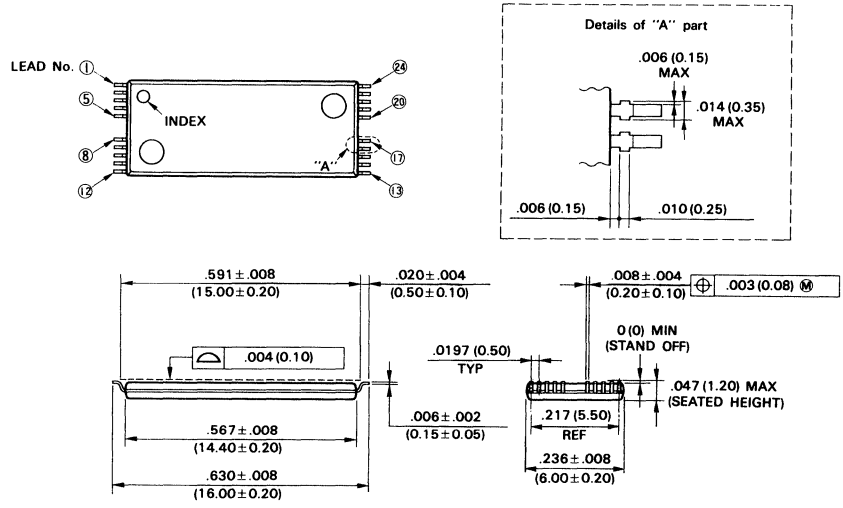


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: – PFTR)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M05)



Dimensions in inches (millimeters)

2

June 1990
Edition 1.0

FUJITSU

DATA SHEET

MB814100-80/-10/-12

CMOS 4,194,304 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 4,194,304 x 1 Bit Fast Page Mode Dynamic RAM

The Fujitsu MB814100 is a fully decoded CMOS dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x 1 configuration. The MB814100 features a fast page mode of operation whereby high-speed, random access of up to 2,048-bits of data within the same row can be selected. The MB814100 DRAM is ideally suited for mainframes, buffers, hand-held computers, and other memory applications where very low power dissipation and compact layout are basic requirements of the design. Since the standby current of the MB814100 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

The MB814400 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814100 are not critical and all inputs are TTL compatible.

Features

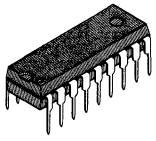
Parameter	MB814100-80	MB814100-10	MB814100-12
$\overline{RAS}$ Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	30 ns max.	35 ns max.
Fast Page Mode Cycle Time	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)		

- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

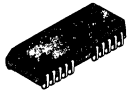
Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

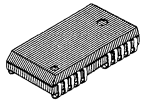
Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



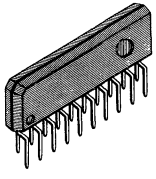
DIP–18P–M04



LCC–26P–M04



LCC–26P–M03

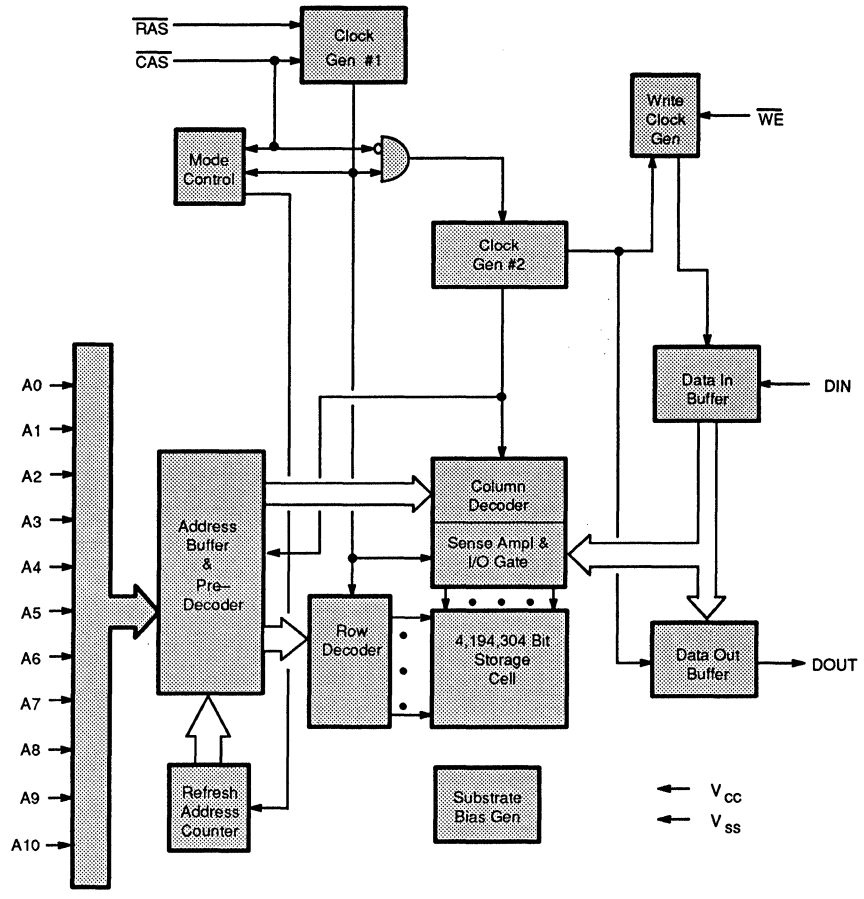


ZIP–20P–M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB814100 DYNAMIC RAM – BLOCK DIAGRAM

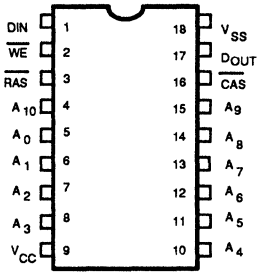


CAPACITANCE (T_A = 25°C, f = 1MHz)

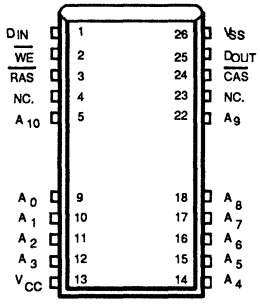
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, DIN	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, DOUT	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

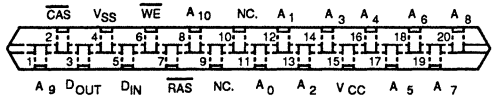
18-Pin DIP:
(TOP VIEW)



26-Pin SOJ:
(TOP VIEW)



20-Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A10	Address inputs.
VCC	+5 volt power supply.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty–two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits (A0–A10) are available, the column and row inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 4. First, eleven row address bits are applied on pins A0–through–A10 and latched with the row address strobe ($\overline{RAS}$) then, eleven column address bits are applied and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or beforethe falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of two basic ways—an early write cycle and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

The data remains valid until either $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 2,048–bits can be accessed and, when multiple MB 814100s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = −5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	−10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	−10	—	10	µA
Operating current (Average Power supply current)	MB814100-80	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814100-10					65	
2	MB814100-12					55	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} −0.2V			1.0	
Refresh current #1 (Average power supply current)	MB814100-80	I_{CC3}	$\overline{CAS}$ = VIH, $\overline{RAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814100-10					65	
2	MB814100-12					55	
Fast Page Mode current	MB814100-80	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	75	mA
	MB814100-10					65	
2	MB814100-12					55	
Refresh current #2 (Average power supply current)	MB814100-80	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	75	mA
	MB814100-10					65	
2	MB814100-12					55	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100-80		MB814100-10		MB814100-12		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	185	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	30	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	5	—	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	20	—	25	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	20	—	25	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100-80		MB814100-10		MB814100-12		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	30	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	10	—	10	—	10	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	20	—	ns
41	$\overline{WE}$ Set Up Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
42	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	15	—	15	—	20	—	ns
51	Fast Page Mode Read/Write Cycle Time		t_{PC}	55	—	60	—	70	—	ns
52	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	85	—	90	—	105	—	ns
53	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	55	—	60	—	70	ns
54	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	—	15	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify-write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh.

Fig. 2 – t_{RAC} vs. t_{RCD}

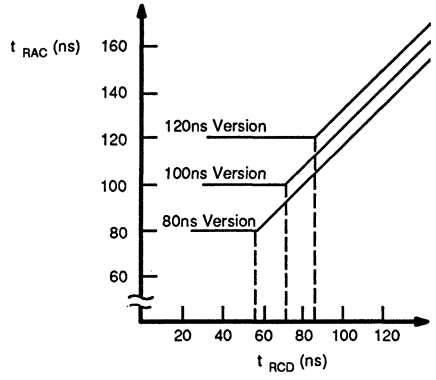
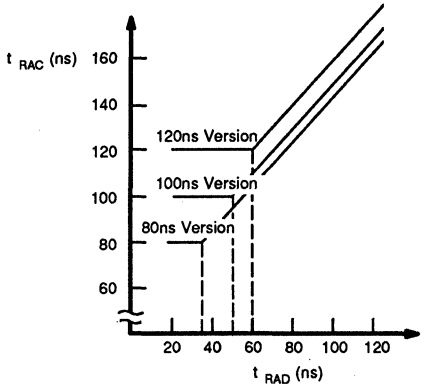


Fig. 3 – t_{RAC} vs. t_{RAD}



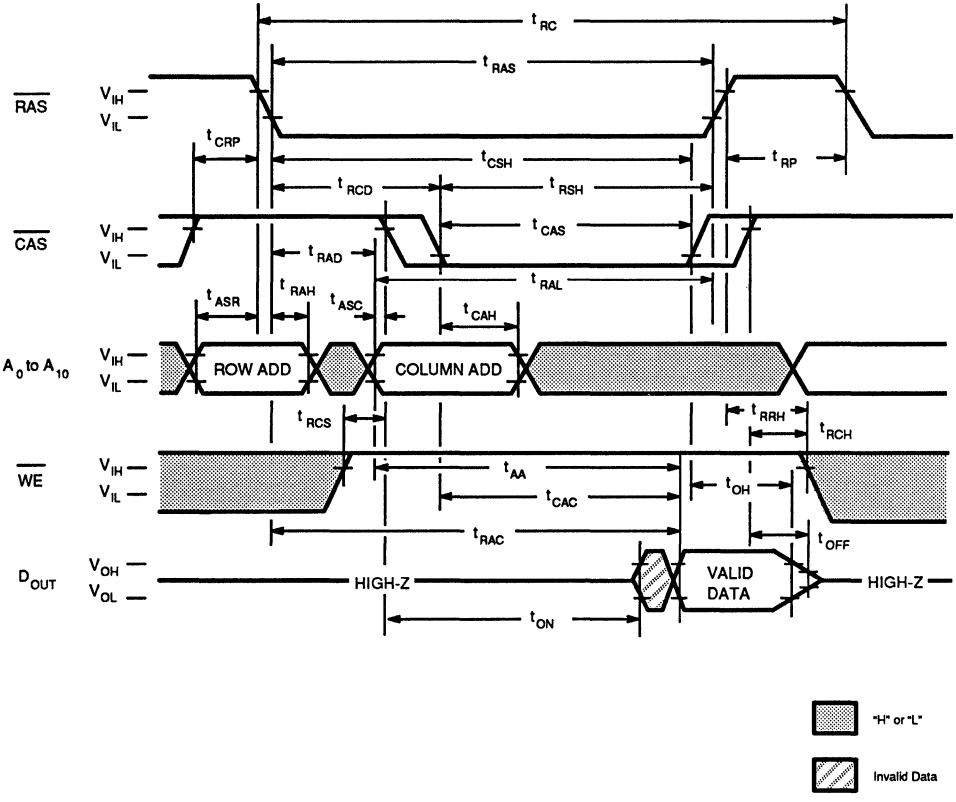
2

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	H	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	H	—	—	—	Valid	Yes	Previous data is kept

Notes:
X : "H" or "L"
*1: It is impossible in Fast Page Mode.

Fig. 4 – READ CYCLE

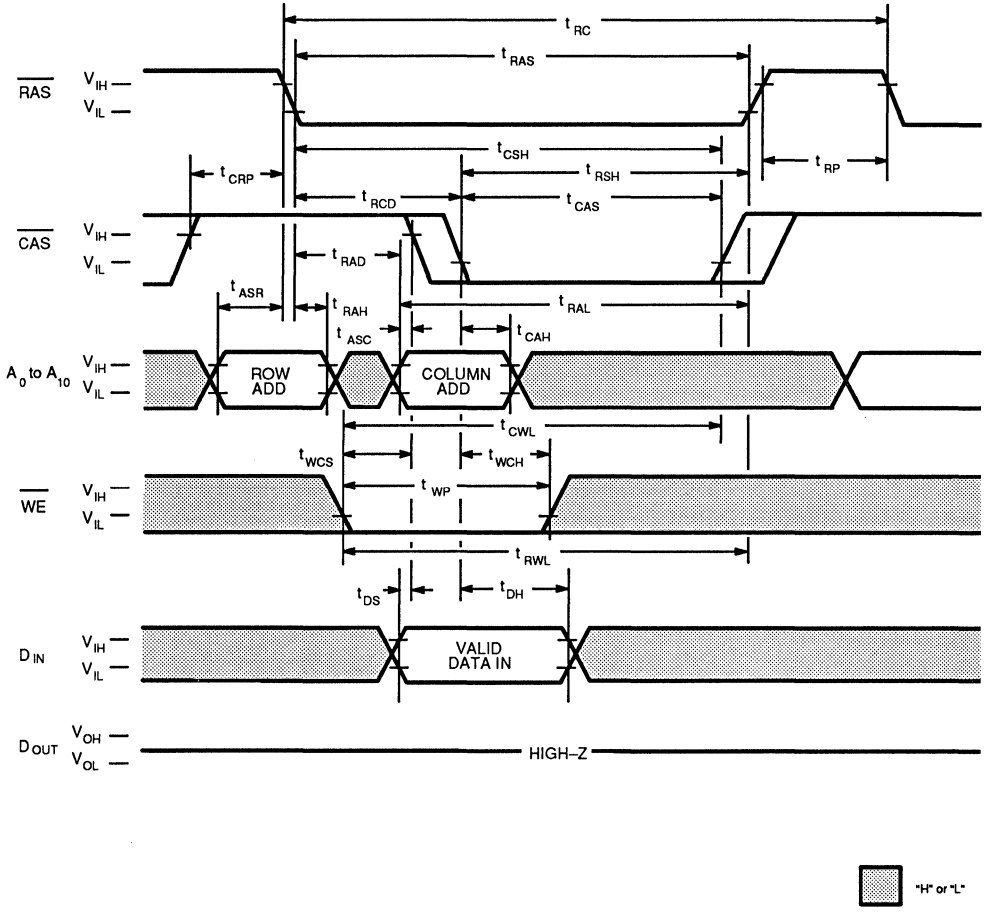


DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

2

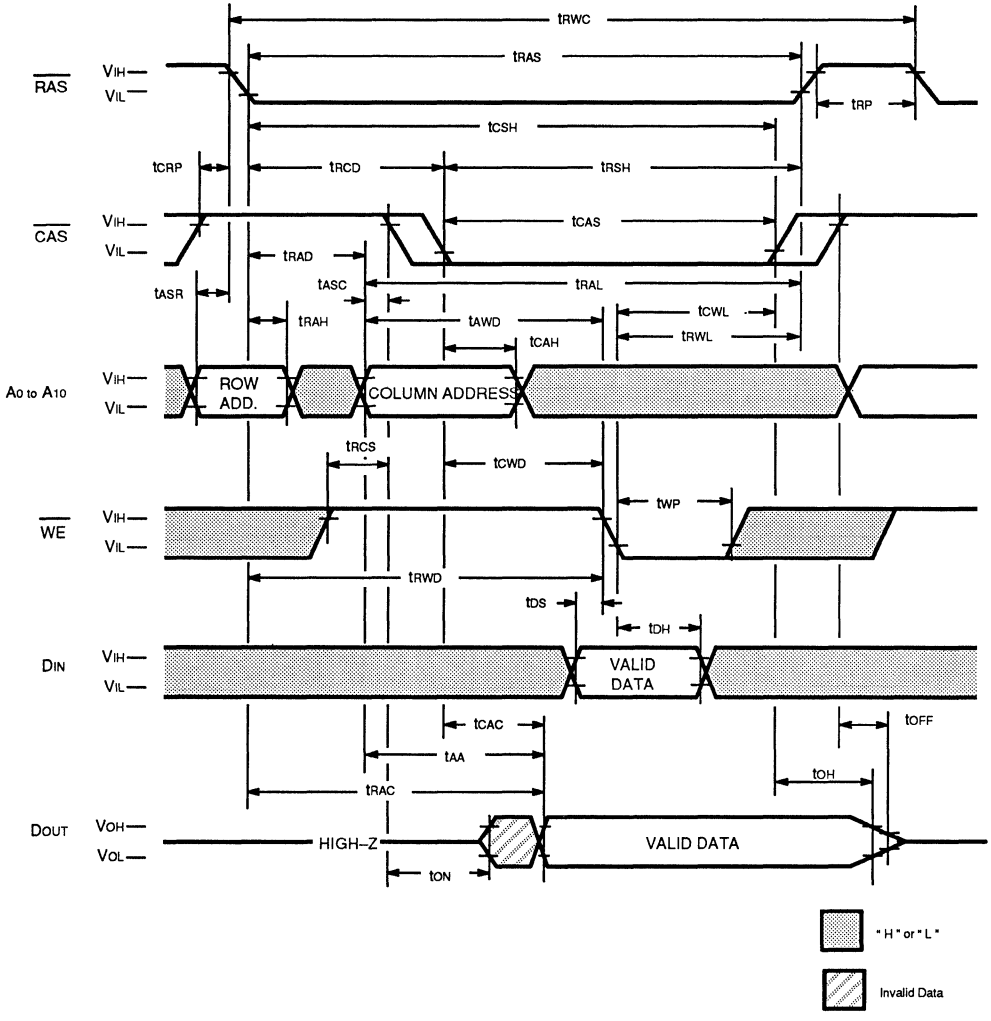
Fig. 5 — WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin islatched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE

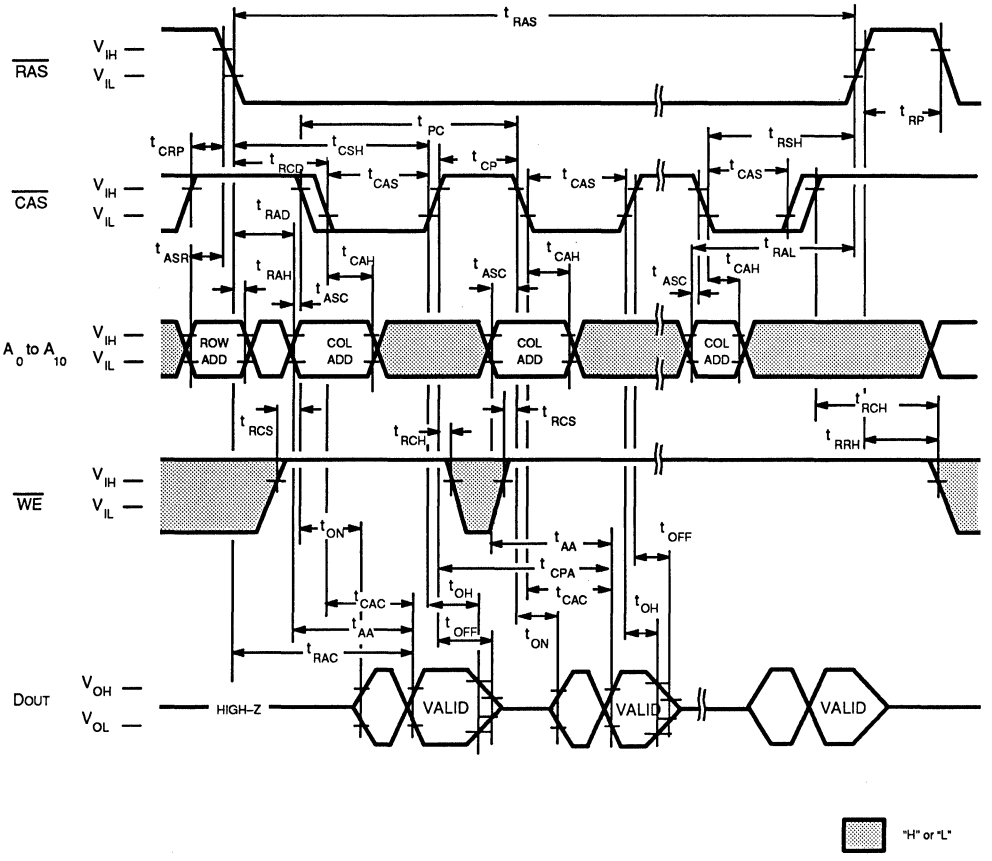


DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

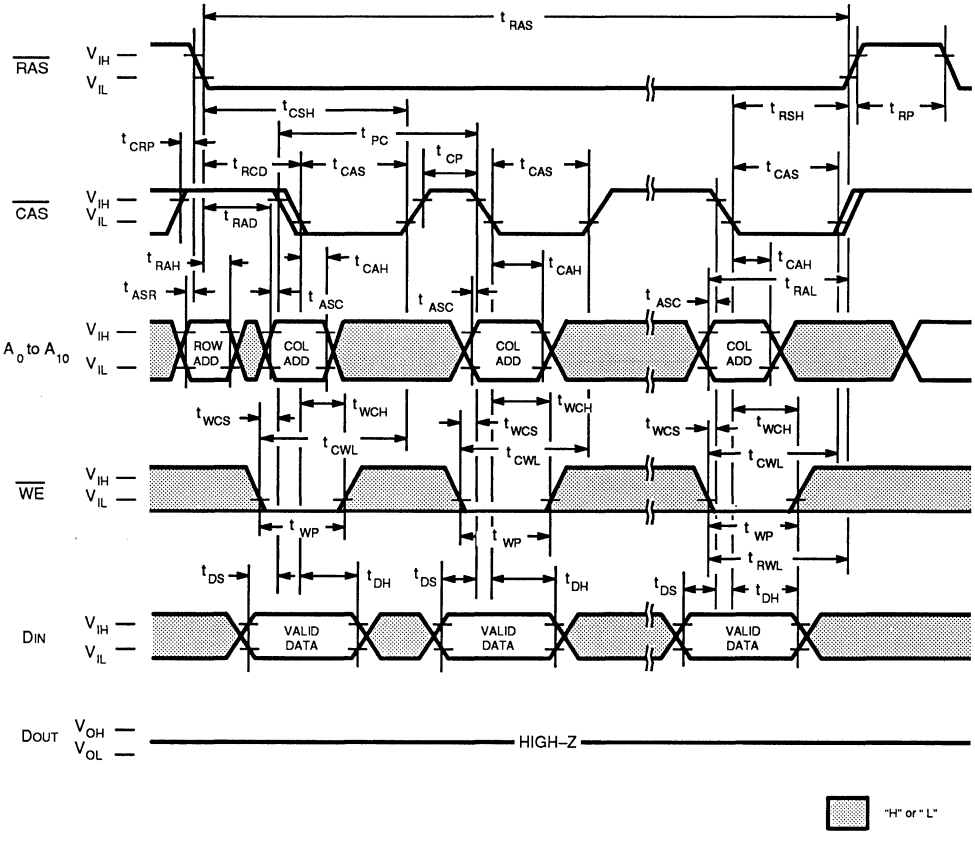
Fig. 7 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later.
Any of the 2048 bits belonging to each row can be accessed.

Fig. 8 – FAST PAGE MODE WRITE CYCLE (Early Write)

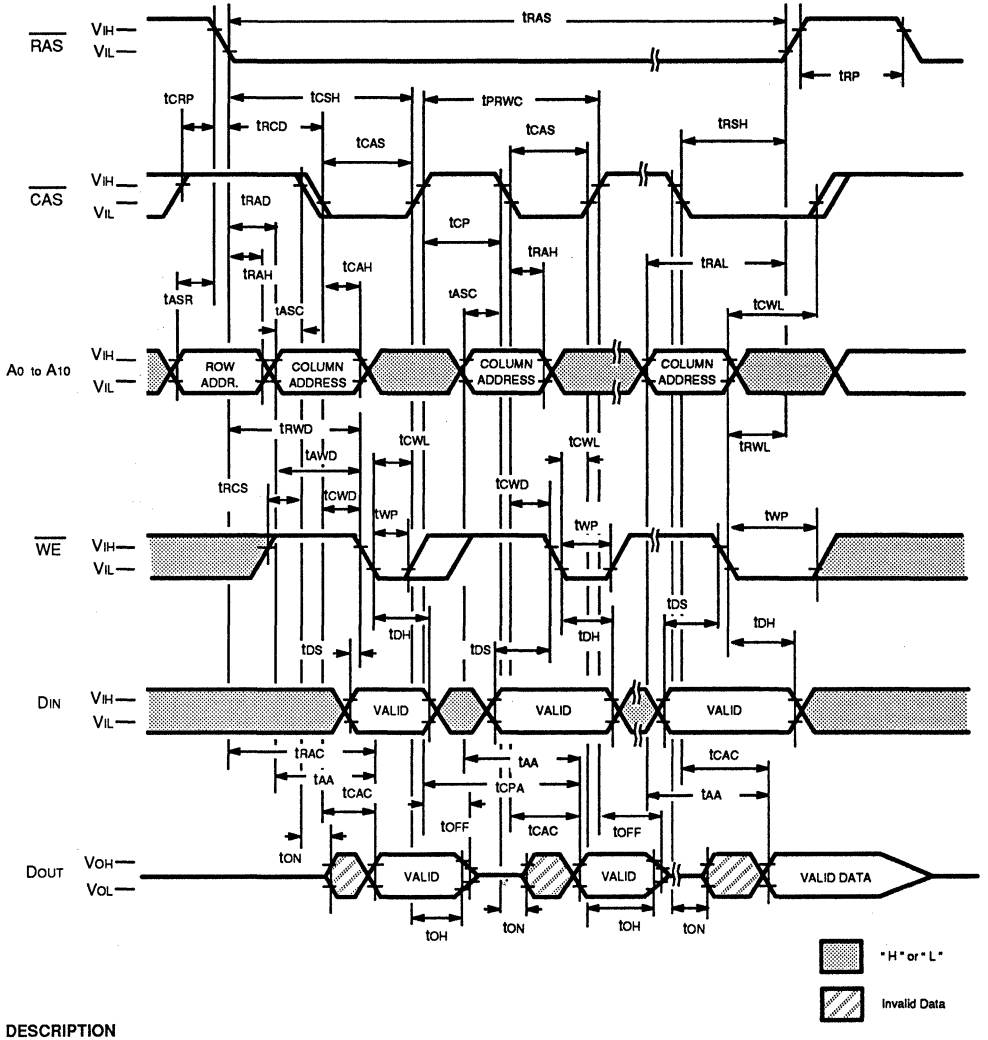


DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 2048 bits belonging to each row can be accessed.

2

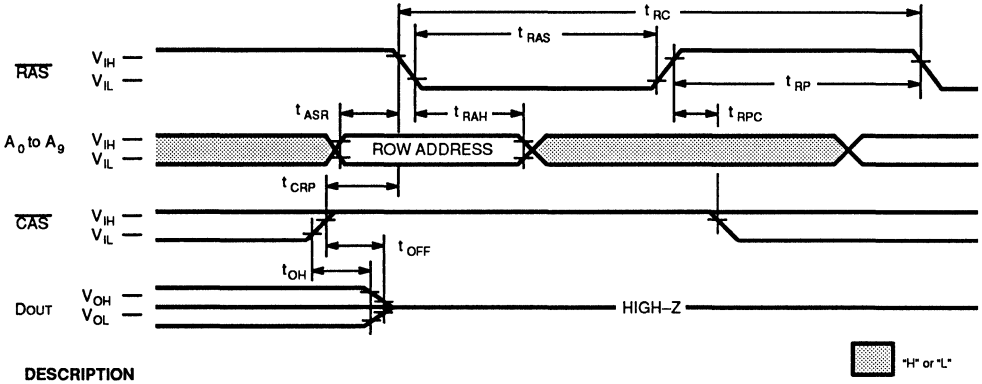
Fig. 9 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode, the read–modify–write cycle can be executed by changing $\overline{WE}$ high to low after the data appearsat DOUT pin as well as normal cycle. Any of the 2048 bits belonging to each row can be accessed.

Fig. 10 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$, DIN, A10 = "H" or "L")

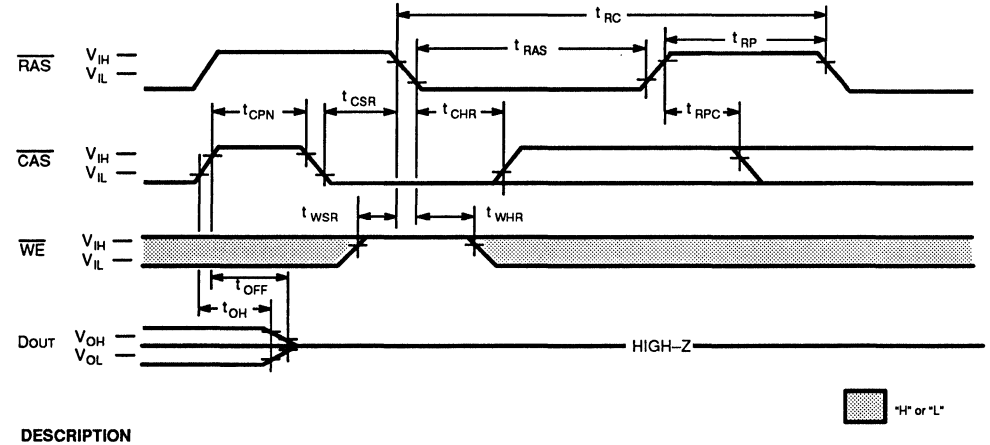


DESCRIPTION

The refresh of DRAM is executed by normal read, write or read–modify–write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 1024 row address must be refreshed every 16.4ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re–written to the cell. The MB814100 has three types of refresh modes, $\overline{RAS}$–only refresh, $\overline{CAS}$–before–$\overline{RAS}$ refresh, and Hidden refresh.

The $\overline{RAS}$ only refresh is executed by keeping $\overline{RAS}$ "L" and $\overline{CAS}$ "H" throughout the cycle. The row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, the DOUT pin is kept in a high impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (A0 to A10, DIN="H" or "L")



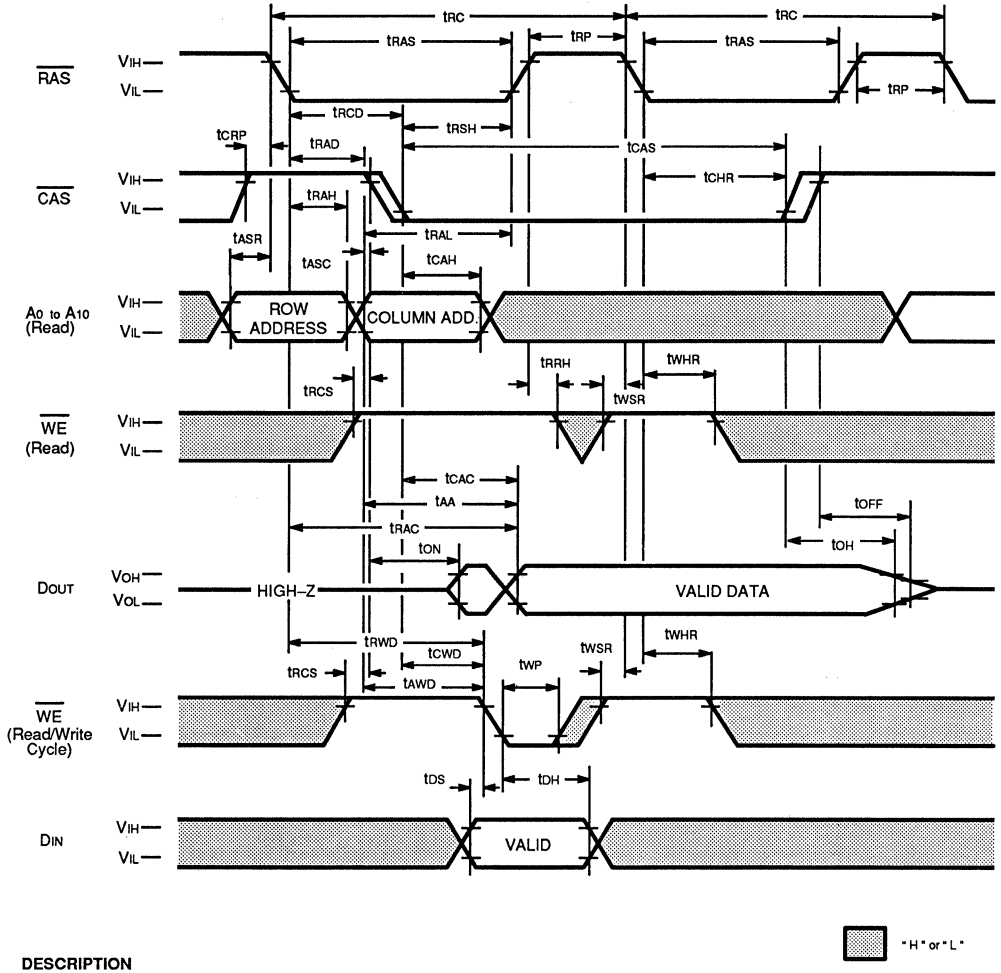
DESCRIPTION

The $\overline{CAS}$–before–$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB814100 executes $\overline{CAS}$–before–$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" in order not to enter "test mode" to be specified later.

2

Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

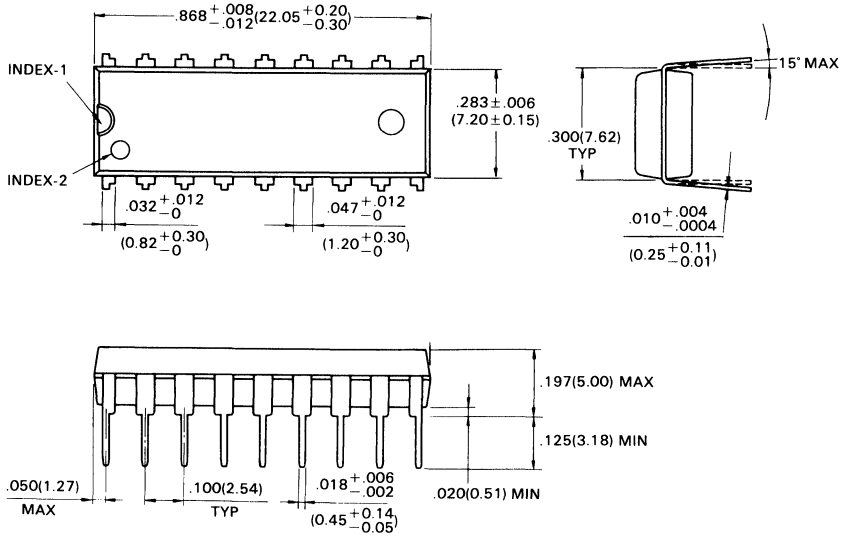
The hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$–before–$\overline{RAS}$ refresh.
$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" for the secound time in order not to enter "test mode" to be specified later.

PACKAGE DIMENSIONS

(Suffix : –P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)



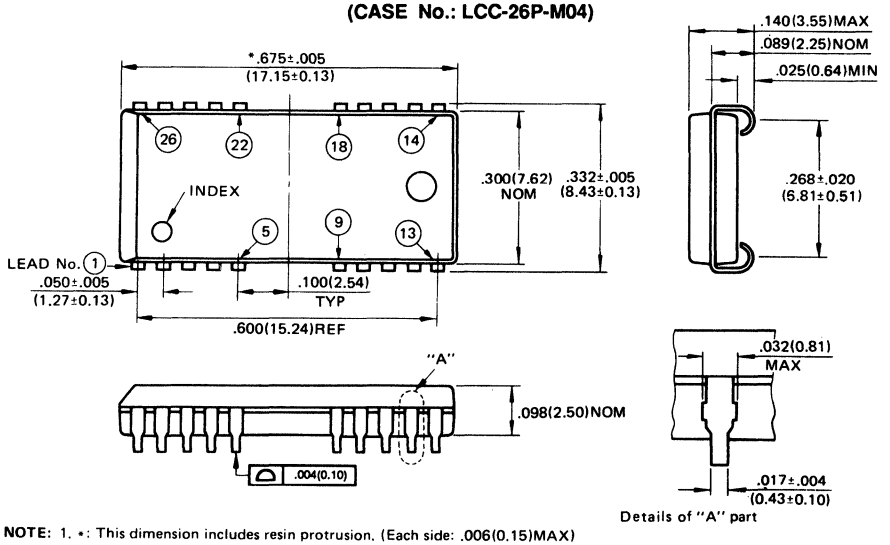
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

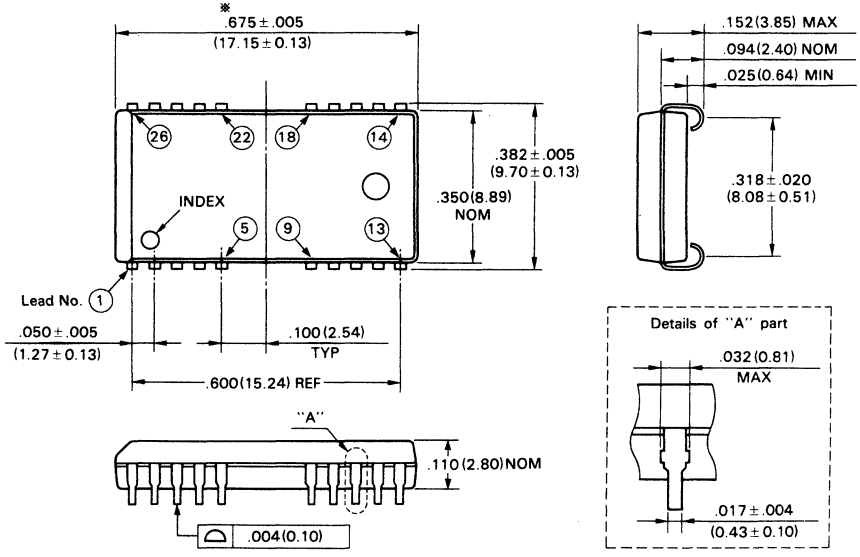
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-26P-M03)



※ Remaining Resin .006(0.15) MAX

Dimensions in inches (millimeters).

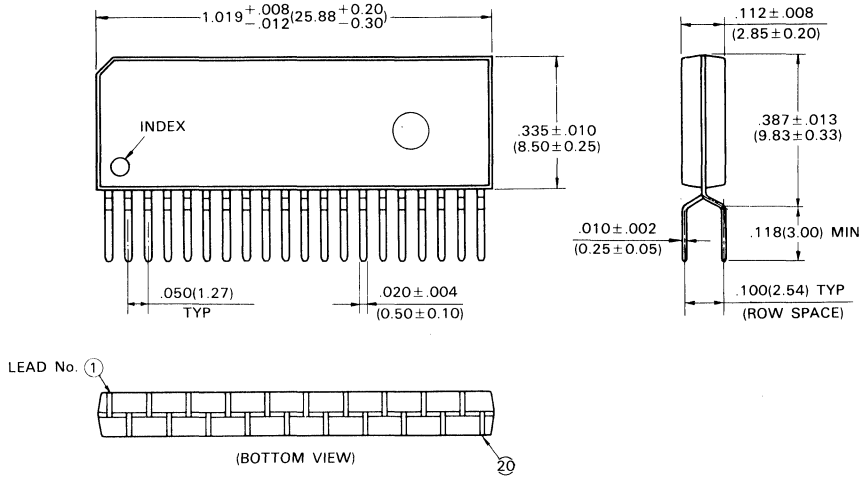
2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

November 1990
Edition 1.0

FUJITSU

DATA SHEET

MB814100-80L/-10L/-12L

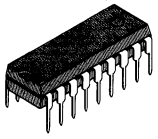
CMOS 4M x 1 BIT FAST PAGE MODE LOW POWER DYNAMIC RAM

CMOS 4M x 1 Bit Fast Page Mode Low Power Dynamic RAM

The Fujitsu MB814100 is a fully decoded CMOS dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x 1 configuration. The MB814100 features a fast page mode of operation whereby high-speed, random access of up to 2,048-bits of data within the same row can be selected. The MB814100 DRAM is ideally suited for mainframes, buffers, hand-held computers, and other memory applications where very low power dissipation and compact layout are basic requirements of the design. Since the standby current of the MB814100 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

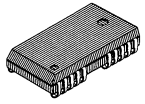
The MB814400 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814100 are not critical and all inputs are TTL compatible.

ADVANCE INFORMATION

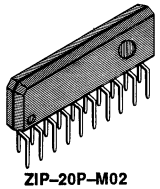


DIP–18P–M04

LCC–26P–M04



LCC–26P–M03



ZIP–20P–M02

T.B.D. T.B.D.

FPT–26P–M01 FPT–26P–M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Features

Parameter	MB814100-80L	MB814100-10L	MB814100-12L
$\overline{RAS}$ Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	25 ns max.	30 ns max.
Fast Page Mode Cycle Time	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/1.1 mW max. (CMOS level)		

- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 128 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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June 1990
Edition 2.0

FUJITSU

DATA SHEET

MB814101-80/-10/-12

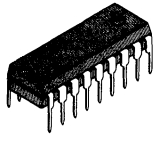
CMOS 4,194,304 BIT NIBBLE MODE DYNAMIC RAM

CMOS 4,194,304 x 1 Bit Nibble Mode Dynamic RAM

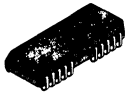
The Fujitsu MB814101 is a fully decoded CMOS dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x 1 configuration. The MB814101 features a nibble mode of operation whereby high-speed serial access of up to 4 bits of data can be selected. The MB814101 DRAM is ideally suited for mainframes, buffers, hand-held computers, and other memory applications where very low power dissipation and compact layout are basic requirements of the design. Since the standby current of the MB814101 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

The MB814101 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814101 are not critical and all inputs are TTL compatible.

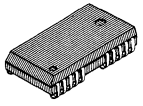
PRELIMINARY



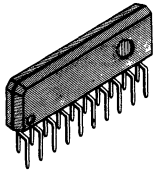
DIP–18P–M04



LCC–26P–M04



LCC–26P–M03



ZIP–20P–M02

2

Features

Parameter	MB814101-80	MB814101-10	MB814101-12
$\overline{RAS}$ Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	30 ns max.	35 ns max.
Nibble Mode Cycle Time	50 ns min.	55 ns min.	60 ns min.
Low Power Dissipation • Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)		

- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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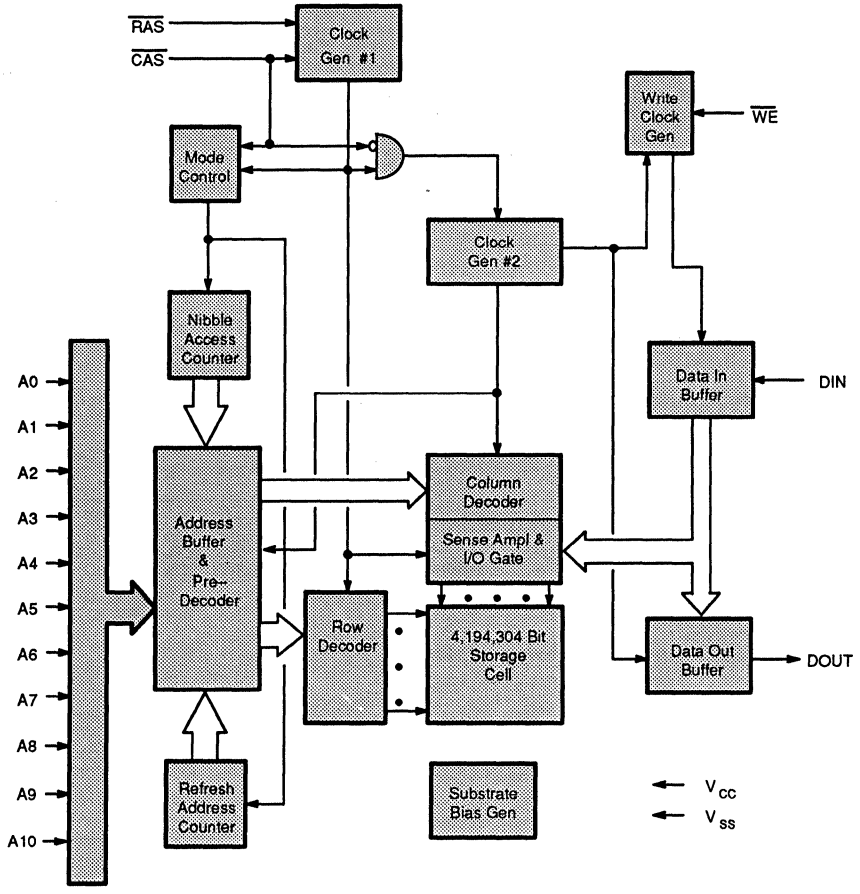
Fig. 1 – MB814101 DYNAMIC RAM – BLOCK DIAGRAM

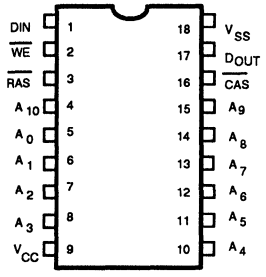


CAPACITANCE (T_A = 25°C, f = 1MHz)

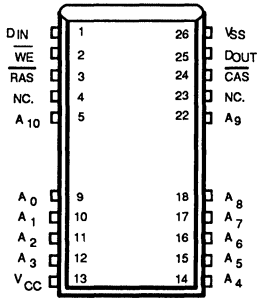
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, DIN	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, DOUT	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

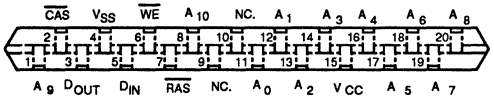
18–Pin DIP:
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A10	Address inputs.
VCC	+5 volt power supply.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty–two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits (A0–A10) are available, the column and row inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 4. First, eleven row address bits are applied on pins A0–through–A10 and latched with the row address strobe ($\overline{RAS}$) then, eleven column address bits are applied and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

2

Input data is written into memory in either of two basic ways—an early write cycle and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

The data remains valid until either $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = −5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	−10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	−10	—	10	
Operating current (Average Power supply current) [2]	MB814101-80	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814101-10					65	
	MB814101-12					55	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ =V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} −0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB814101-80	I_{CC3}	$\overline{CAS}$ = VIH, $\overline{RAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814101-10					65	
	MB814101-12					55	
Nibble Mode current [2]	MB814101-80	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{NC} = min	—	—	50	mA
	MB814101-10					45	
	MB814101-12					40	
Refresh current #2 (Average power supply current) [2]	MB814101-80	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	75	mA
	MB814101-10					65	
	MB814101-12					55	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814101-80		MB814101-10		MB814101-12		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	185	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	30	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	5	—	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	20	—	25	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	20	—	25	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814101-80		MB814101-10		MB814101-12		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	30	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	10	—	10	—	10	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	20	—	ns
41	$\overline{WE}$ Set Up Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
42	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	15	—	15	—	20	—	ns
51	Nibble Mode Read/Write Cycle Time		t_{NC}	50	—	55	—	60	—	ns
52	Nibble Mode Read-Modify-Write Cycle Time		t_{NRWC}	75	—	80	—	90	—	ns
53	Access Time from $\overline{CAS}$ Precharge	9,16	t_{NPA}	—	45	—	50	—	55	ns
54	Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15	—	15	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify-write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh.

Fig. 2 – t_{RAC} vs. t_{RCD}

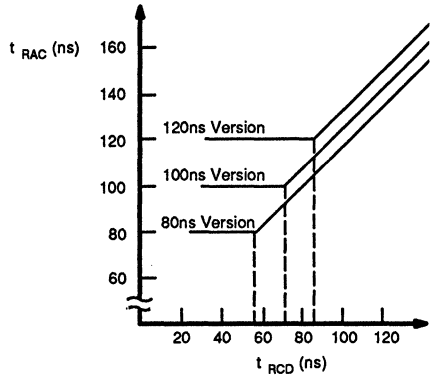
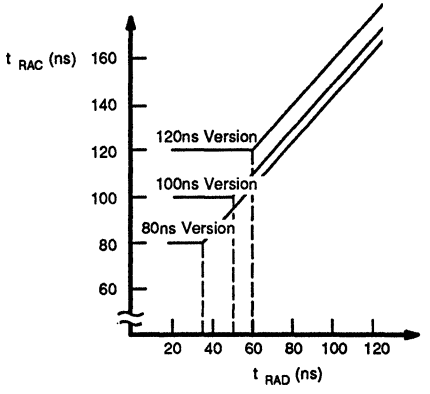


Fig. 3 – t_{RAC} vs. t_{RAD}



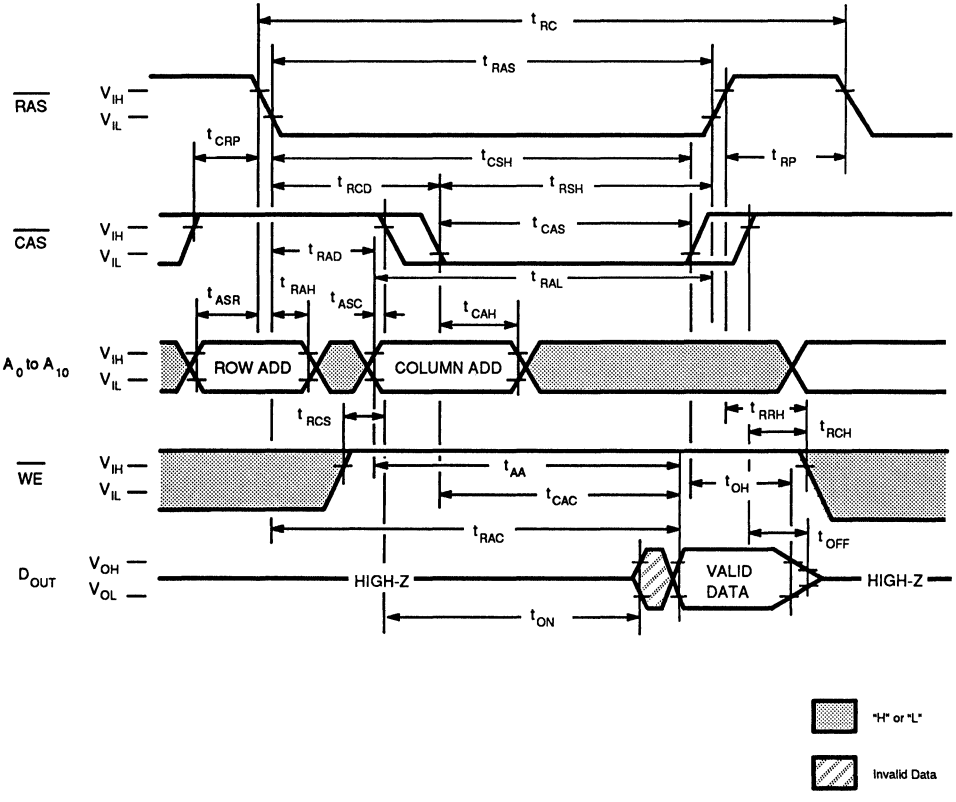
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$(min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	H	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	H	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Nibble Mode.

Fig. 4 – READ CYCLE

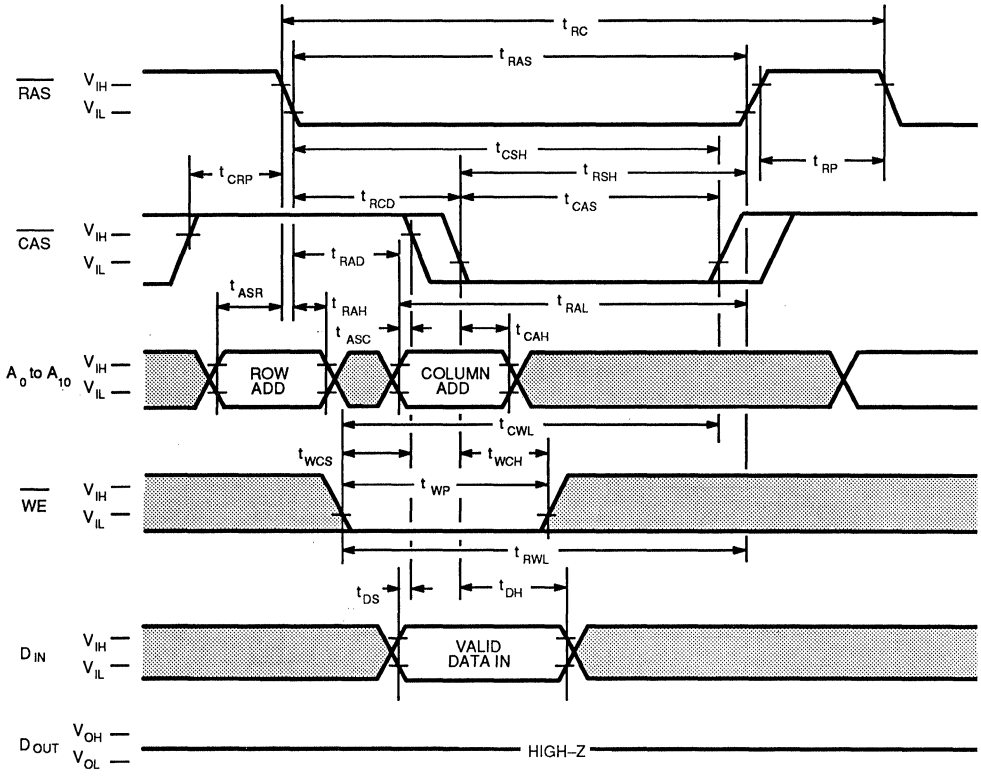


DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

2

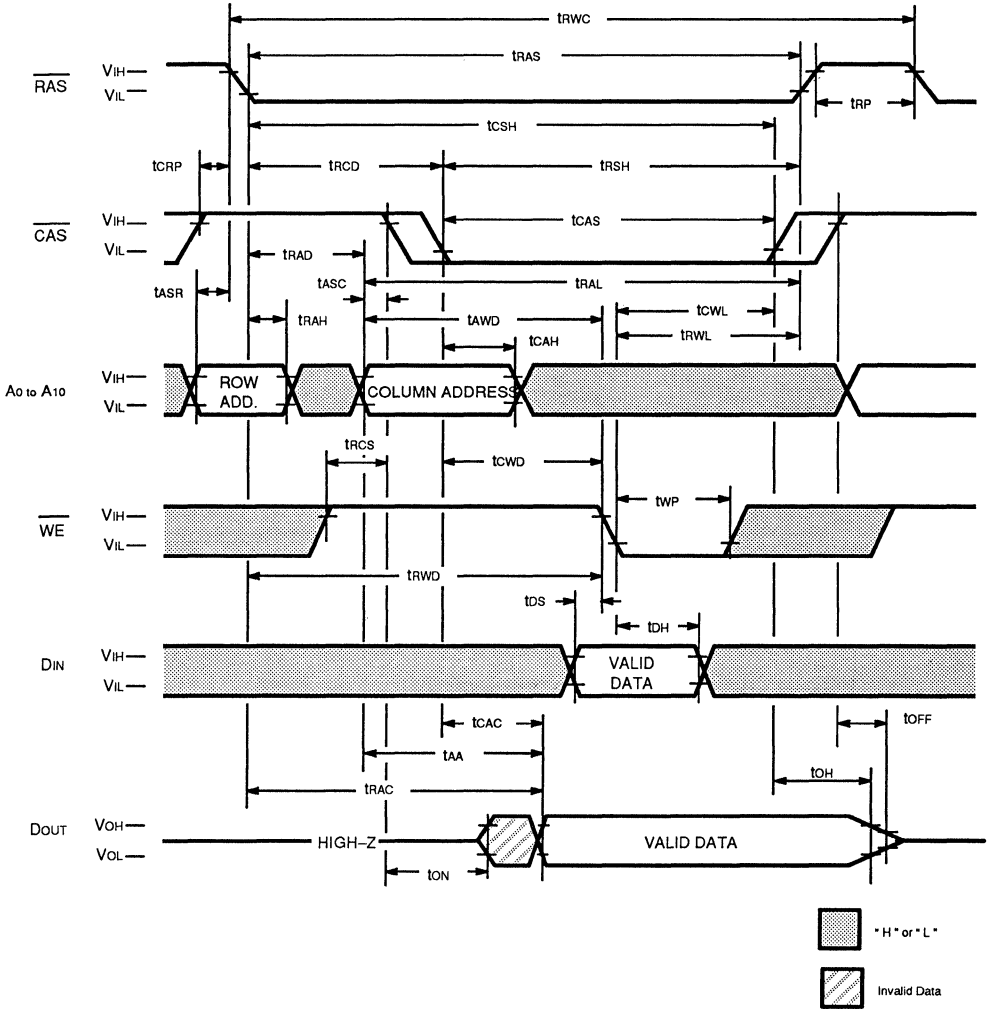
Fig. 5 — WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

Fig. 7 – NIBBLE MODE READ CYCLE

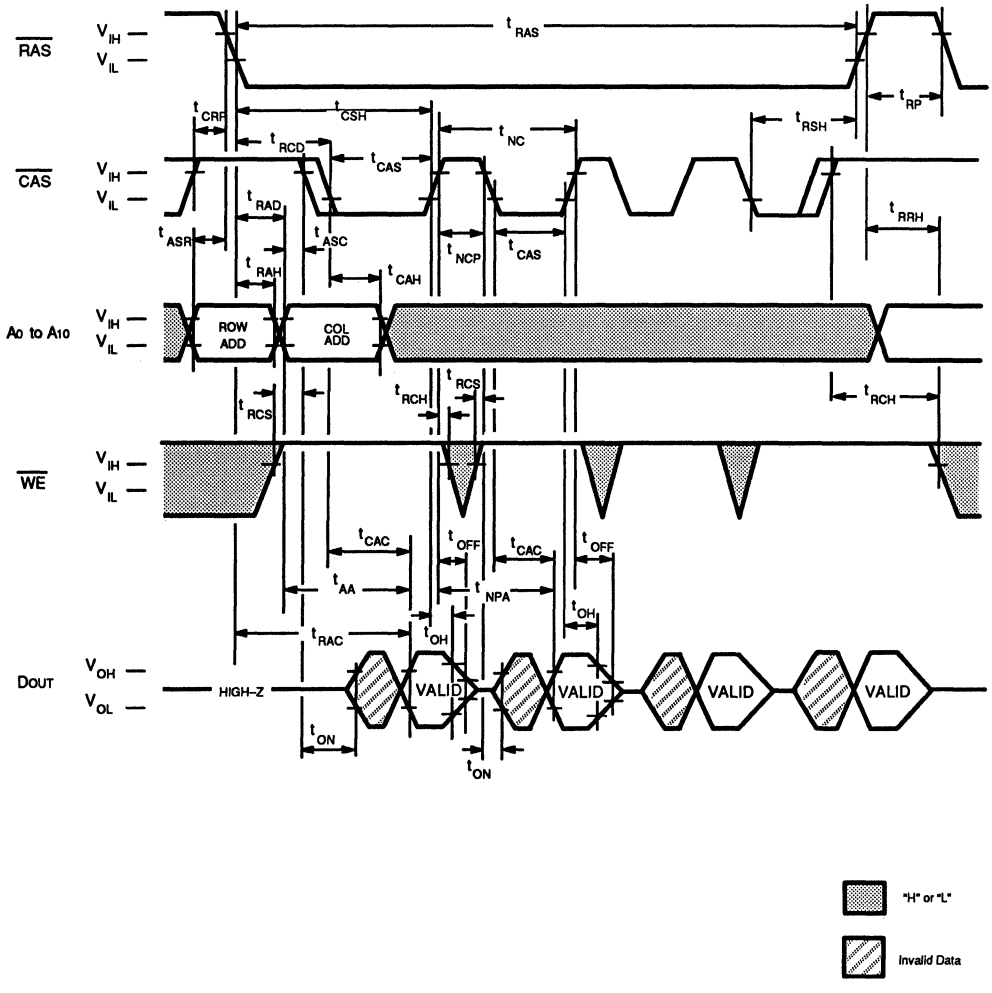
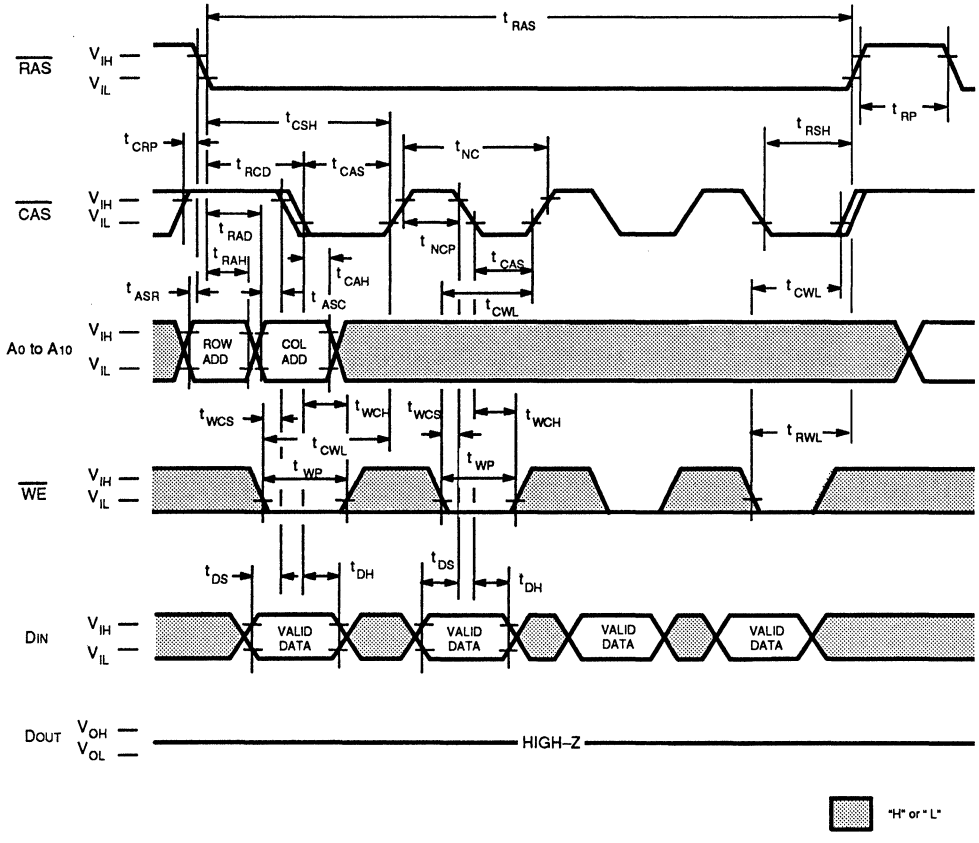


Fig. 8 – NIBBLE MODE WRITE CYCLE (Early Write)



2

Fig. 9 – NIBBLE MODE READ–MODIFY–WRITE CYCLE

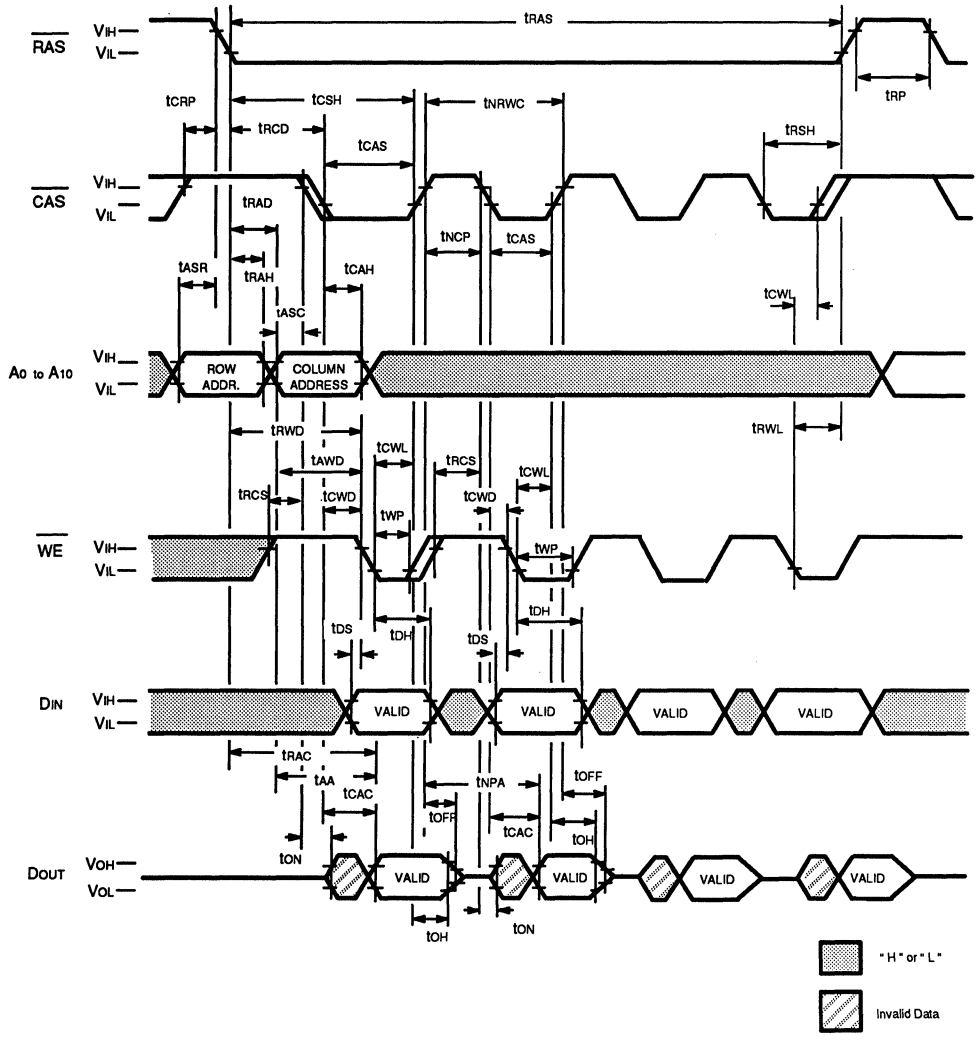
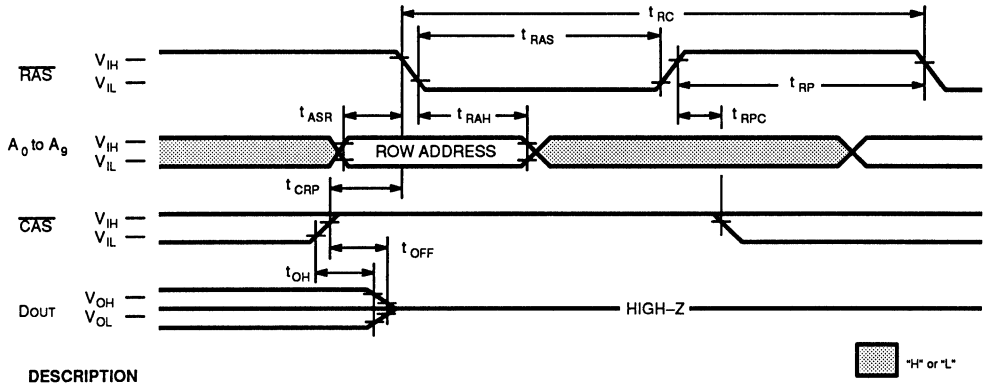


Fig. 10 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$, DIN, A10 = "H" or "L")

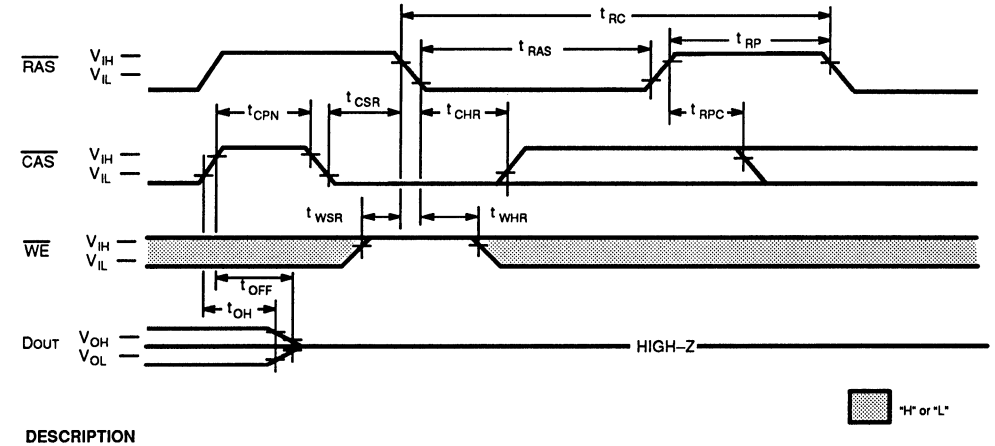


DESCRIPTION

The refresh of DRAM is executed by normal read, write or read–modify–write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 1024 row address must be refreshed every 16.4ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re–written to the cell. The MB814100 has three types of refresh modes, $\overline{RAS}$–only refresh, $\overline{CAS}$–before–$\overline{RAS}$ refresh, and Hidden refresh.

The $\overline{RAS}$ only refresh is executed by keeping $\overline{RAS}$ "L" and $\overline{CAS}$ "H" throughout the cycle. The row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, the DOUT pin is kept in a high impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (A0 to A10, DIN="H" or "L")



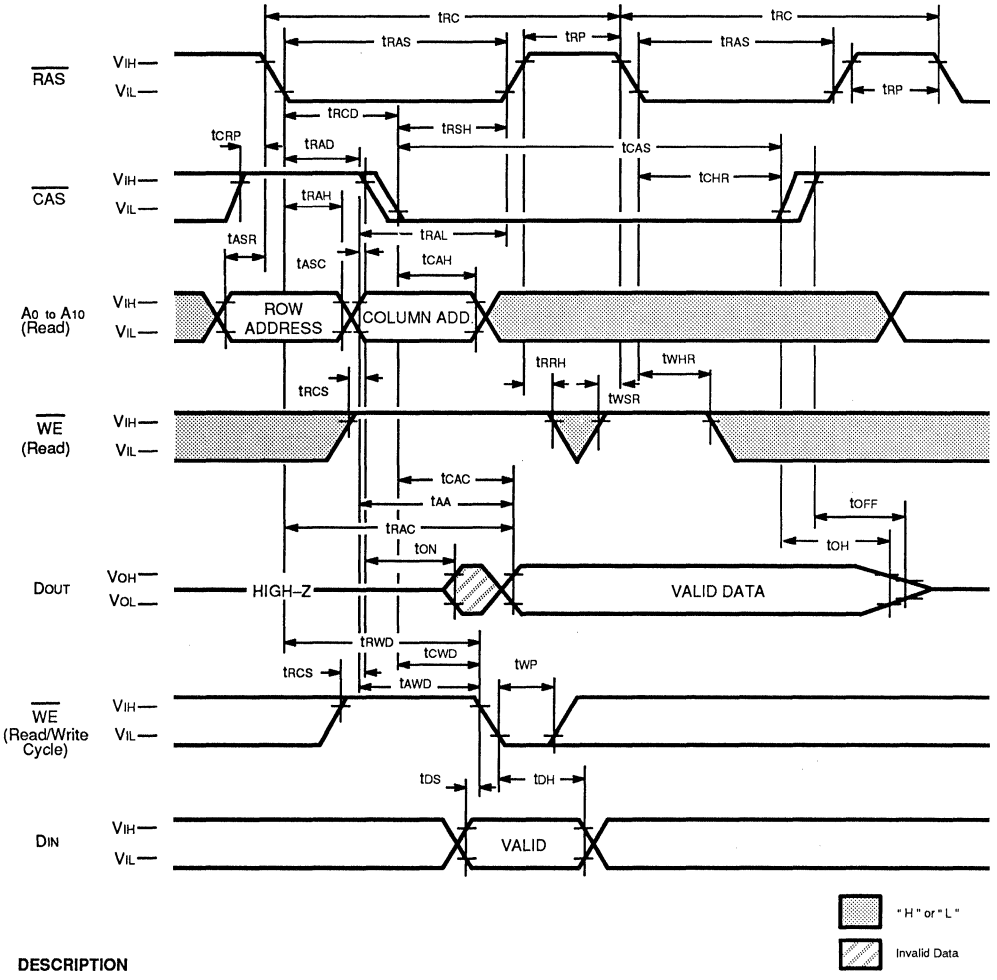
DESCRIPTION

The $\overline{CAS}$–before–$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB814100 executes $\overline{CAS}$–before–$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" in order not to enter "test mode" to be specified later.

2

Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

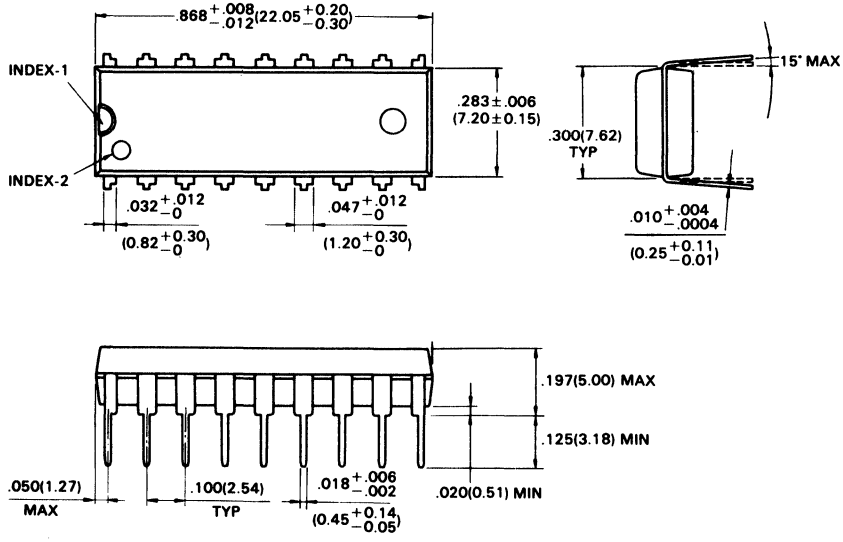
The hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$–before–$\overline{RAS}$ refresh.
$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" for the secound time in order not to enter "test mode" to be specified later.

PACKAGE DIMENSIONS

(Suffix : -P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)



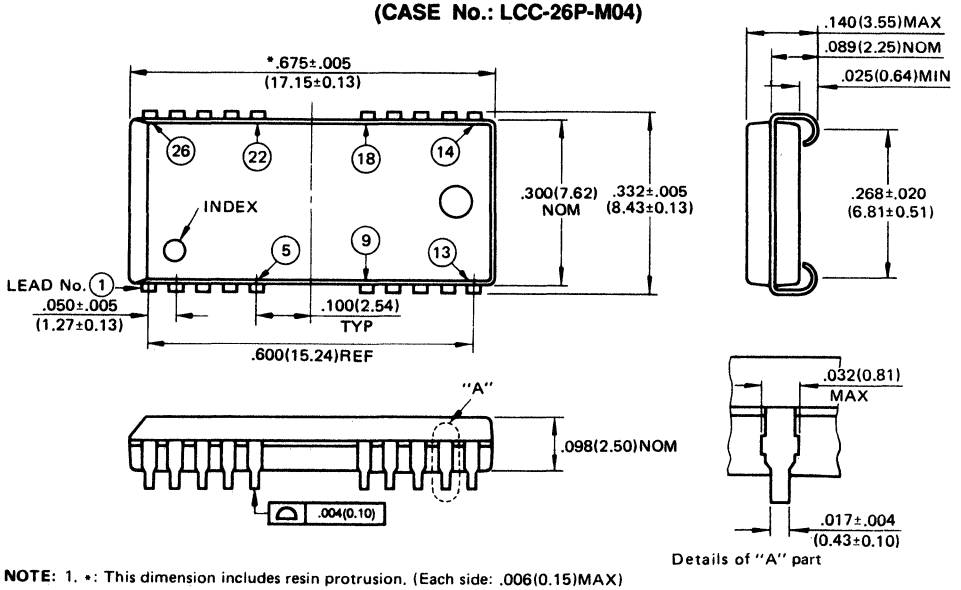
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

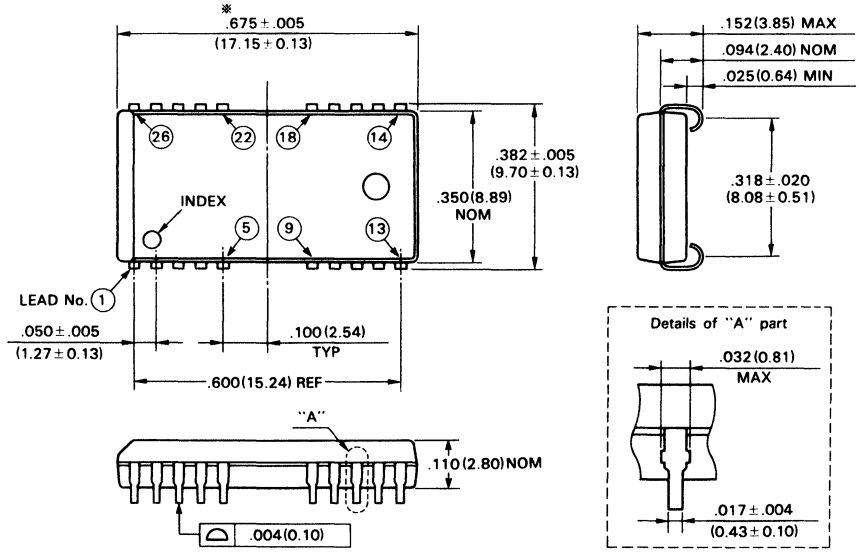
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-26P-M03)



*This dimension includes resin protrusion.(Each side: .006(0.15) MAX.)

Dimensions in inches (millimeters).

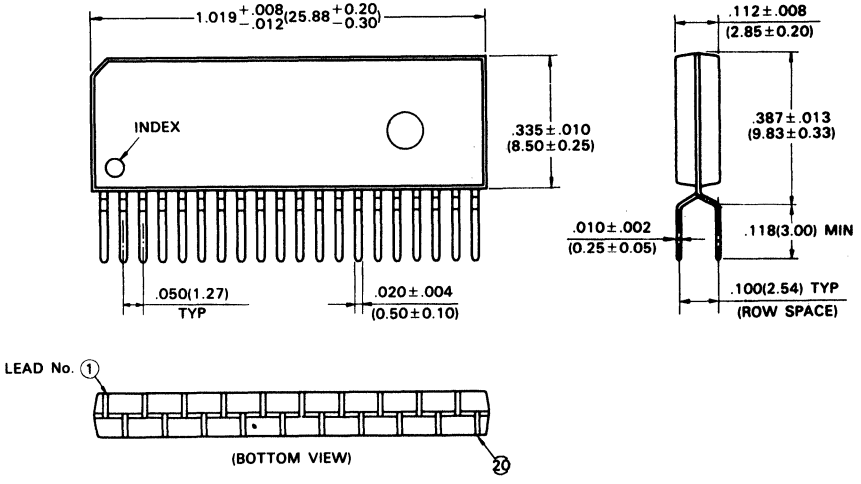
2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

November 1990
Edition 1.0

FUJITSU

DATA SHEET

MB814101-80L/-10L/-12L

CMOS 4M x 1 BIT NIBBLE MODE LOW POWER DYNAMIC RAM

CMOS 4M x 1 Bit Nibble Mode Low Power Dynamic RAM

The Fujitsu MB814101 is a fully decoded CMOS dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x 1 configuration. The MB814101 features a nibble mode of operation whereby high-speed serial access of up to 4 bits of data can be selected. The MB814101 DRAM is ideally suited for mainframes, buffers, hand-held computers, and other memory applications where very low power dissipation and compact layout are basic requirements of the design. Since the standby current of the MB814101 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

The MB814101 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814101 are not critical and all inputs are TTL compatible.

Features

Parameter	MB814101-80L	MB814101-10L	MB814101-12L
$\overline{RAS}$ Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	20 ns max.	25 ns max.	30 ns max.
Nibble Mode Cycle Time	50 ns min.	55 ns min.	60 ns min.
Low Power Dissipation • Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/1.1 mW max. (CMOS level)		

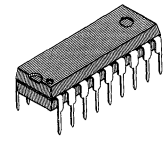
- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 128 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

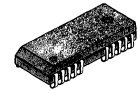
Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

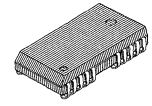
ADVANCE INFORMATION



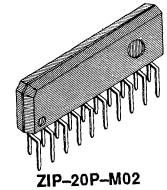
DIP–18P–M04



LCC–26P–M04



LCC–26P–M03



ZIP–20P–M02

T.B.D. T.B.D.

FPT–26P–M01 FPT–26P–M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

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June 1990
Edition 1.0

FUJITSU

DATA SHEET

MB814400-80/-10/-12

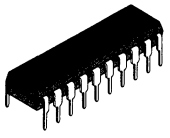
CMOS 4,194,304 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 1,048,576 x 4 Bits Fast Page Mode Dynamic RAM

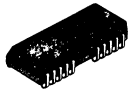
The Fujitsu MB814400 is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells accessible in 4-bit increments. The MB814400 features a fast page mode of operation whereby high-speed, random access of up to 1,024-bits of data within the same row can be selected. The MB814400 DRAM is ideally suited for mainframes, buffers, hand-held computers, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814400 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

The MB814400 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81400 are not critical and all inputs are TTL compatible.

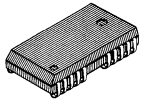
PRELIMINARY



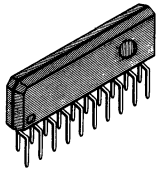
DIP–20P–M03



LCC–26P–M04



LCC–26P–M03



ZIP–20P–M02

2

Features

Parameter	MB814400-80	MB814400-10	MB814400-12
$\overline{RAS}$ Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	25 ns max.	30 ns max.	35 ns max.
Fast Page Mode Cycle Time	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)		

- 1,048,576 words x 4 bits organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

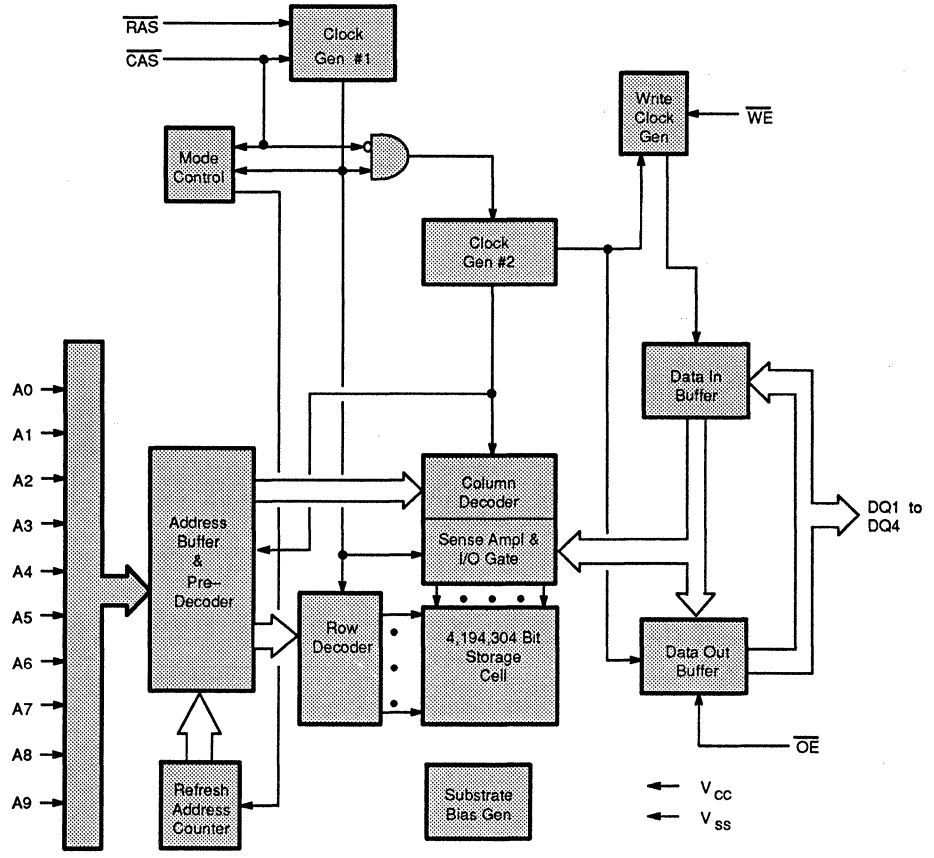
Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

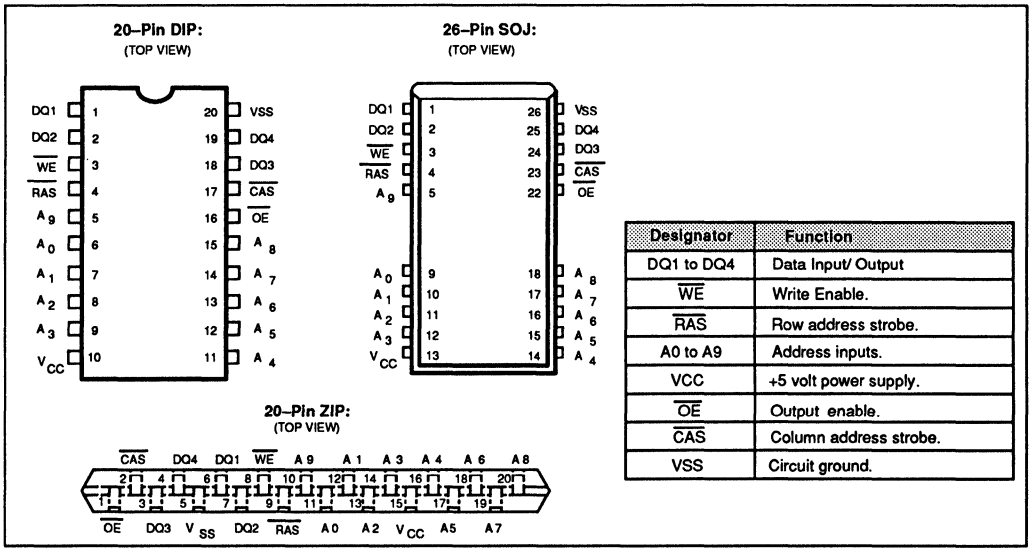
Fig. 1 – MB814400 DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	−1.0	—	0.8	V	

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any four of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, ten row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

2

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024–bits can be accessed and, when multiple MB 814400s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = −5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	−10	—	10	µA
Output leakage current		$I_{DQ(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	−10	—	10	µA
Operating current (Average Power supply current) [2]	MB814400-80	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814400-10					65	
	MB814400-12					55	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} −0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB814400-80	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814400-10					65	
	MB814400-12					55	
Fast Page Mode current [2]	MB814400-80	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	75	mA
	MB814400-10					65	
	MB814400-12					55	
Refresh current #2 (Average power supply current) [2]	MB814400-80	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	75	mA
	MB814400-10					65	
	MB814400-12					55	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814400-80		MB814400-10		MB814400-12		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	220	—	245	—	280	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	30	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	5	—	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	t_{CPN}	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	20	—	25	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	20	—	25	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814400-80		MB814400-10		MB814400-12		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	10	—	10	—	10	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	20	—	ns
38	$\overline{WE}$ Set Up Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	15	—	15	—	20	—	ns
40	Access Time from $\overline{OE}$	9	t_{OEA}	—	22	—	25	—	30	ns
41	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	25	—	25	—	25	ns
42	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	ns
43	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	10	—	10	—	10	—	ns
44	$\overline{OE}$ to Data In Delay Time		t_{OED}	25	—	25	—	25	—	ns
45	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	ns
46	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	55	—	60	—	70	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	120	—	125	—	140	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	55	—	60	—	70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	—	15	—	15	—	ns

Notes:

1. Referenced to VSS.
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH, VIL > -0.5V.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200μs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min).
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
19. Assuemes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh.

Fig. 2 – t_{RAC} vs. t_{RCD}

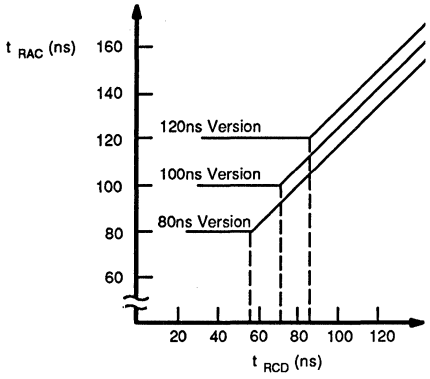
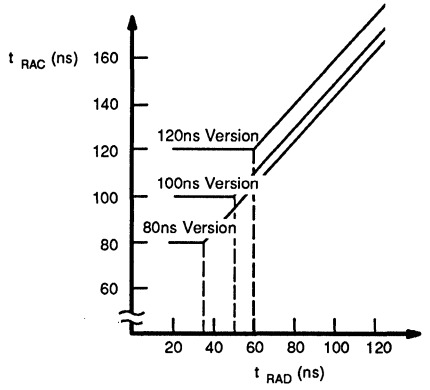


Fig. 3 – t_{RAC} vs. t_{RAD}



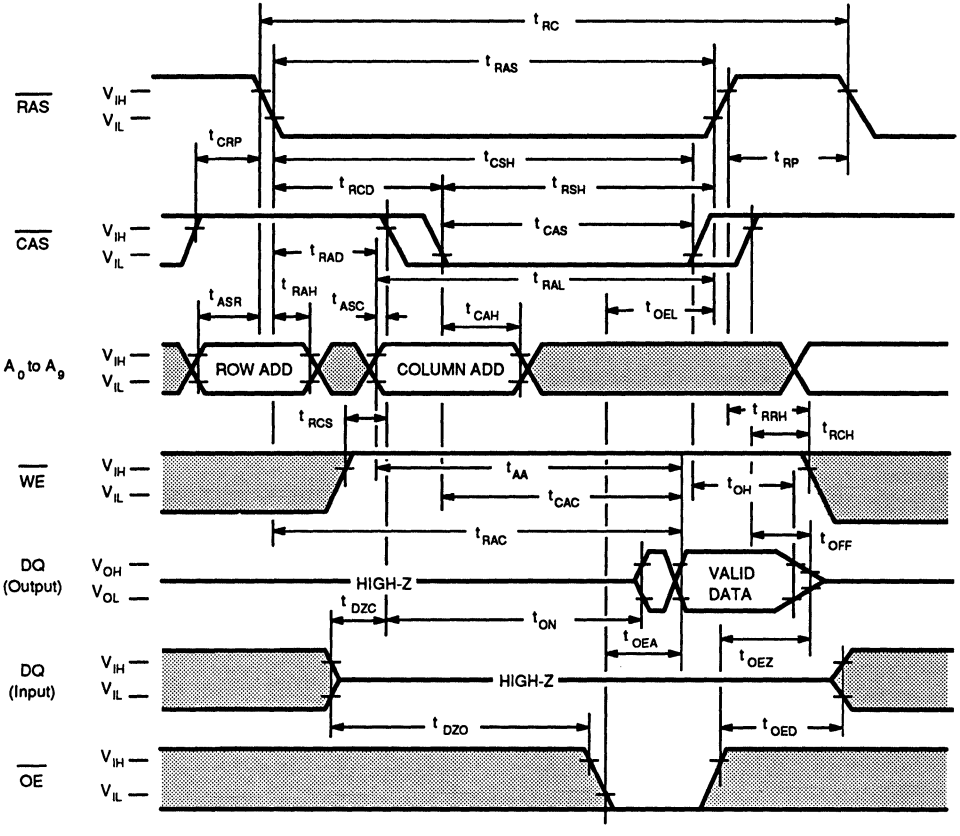
2

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	H	X	—	—	—	High–Z	Yes	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh Cycle	H→L	L	H	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



DESCRIPTION

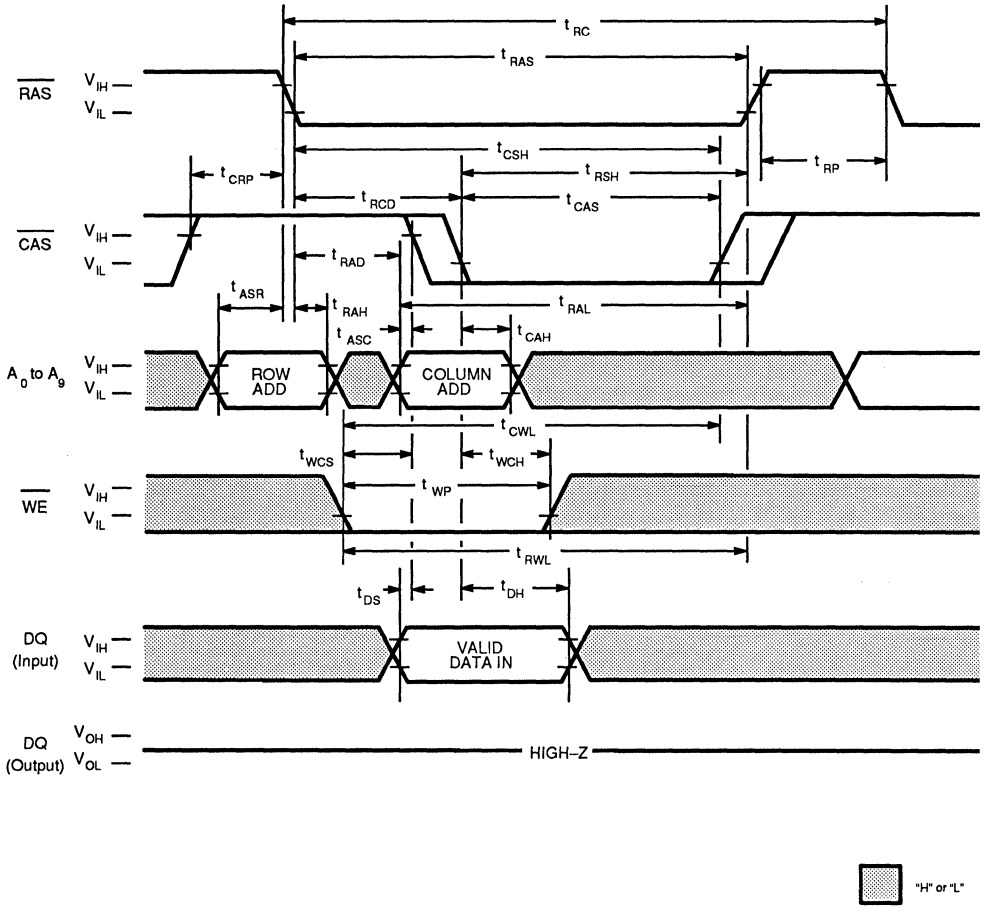
To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), $\overline{OE}$, (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

- If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
- If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
- If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

2

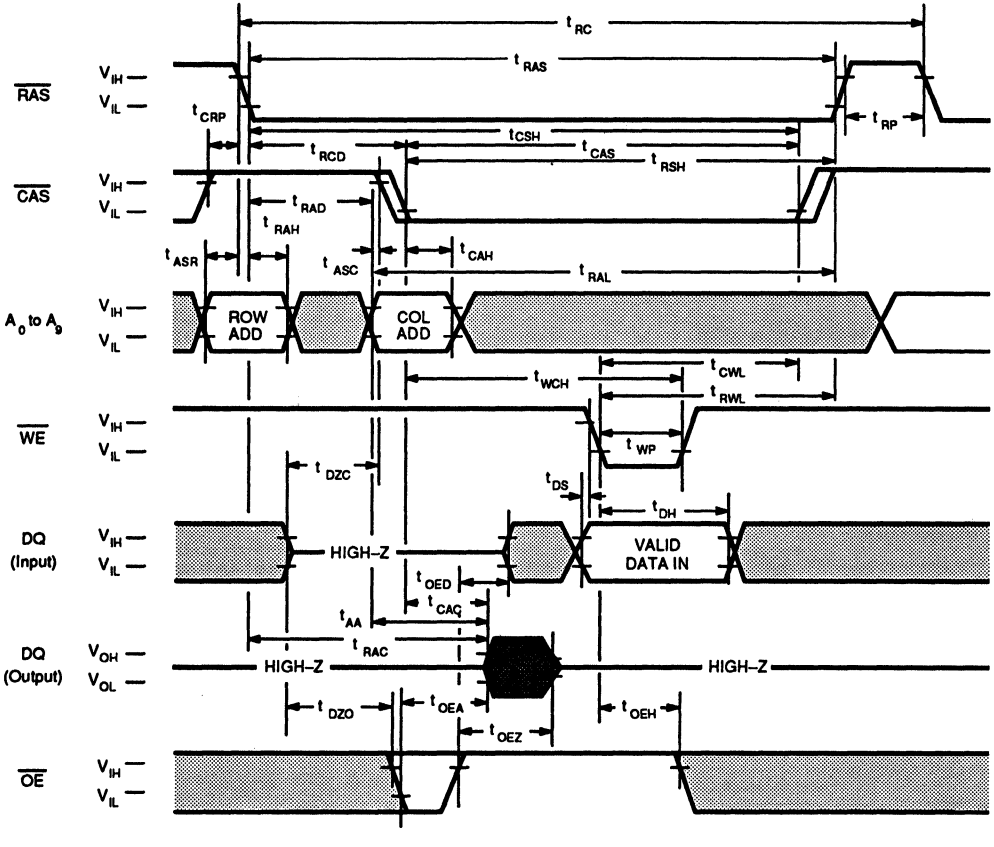
Fig. 5 — EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways — early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters t_{RWL}, t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

Fig. 6 — $\overline{OE}$ (DELAYED WRITE CYCLE)

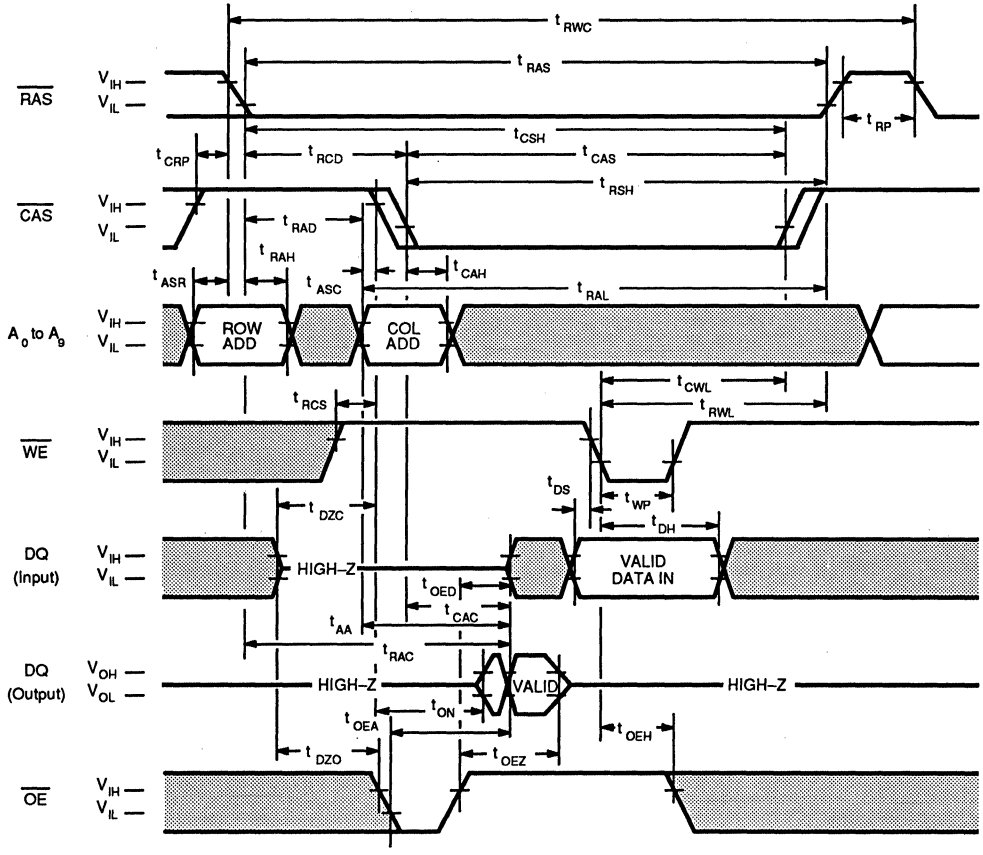


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

2

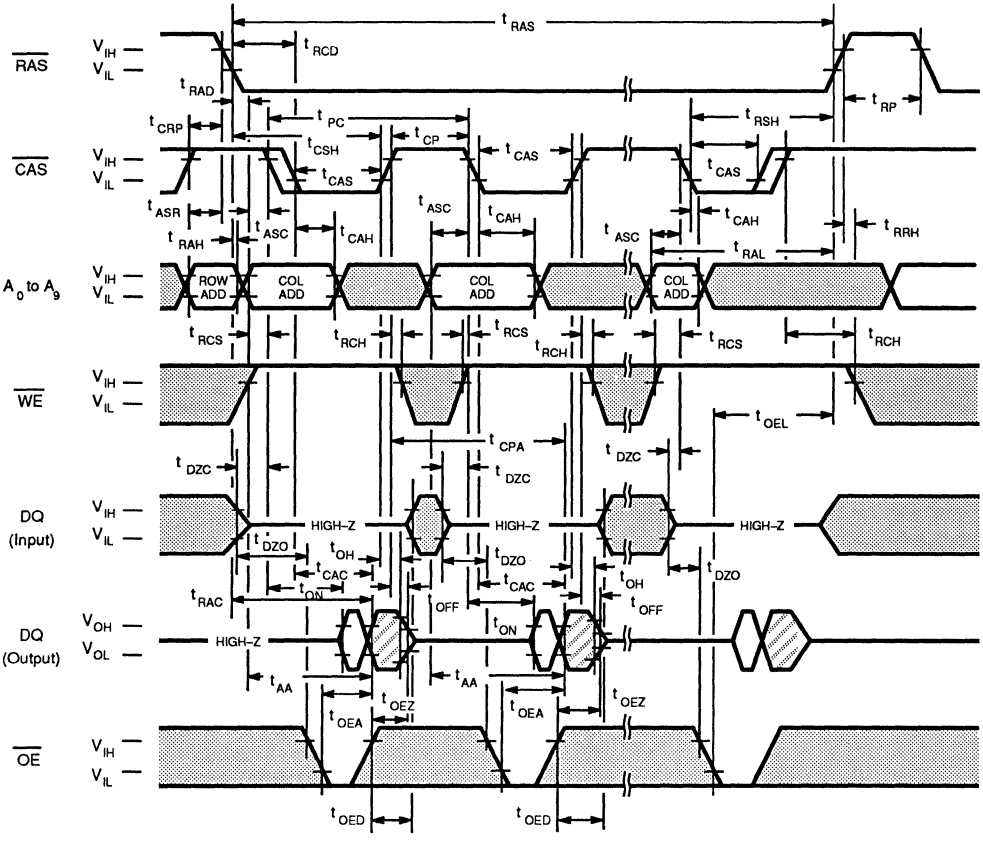
Fig. 7 — READ–MODIFY–WRITE–CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 8 – FAST PAGE MODE READ CYCLE

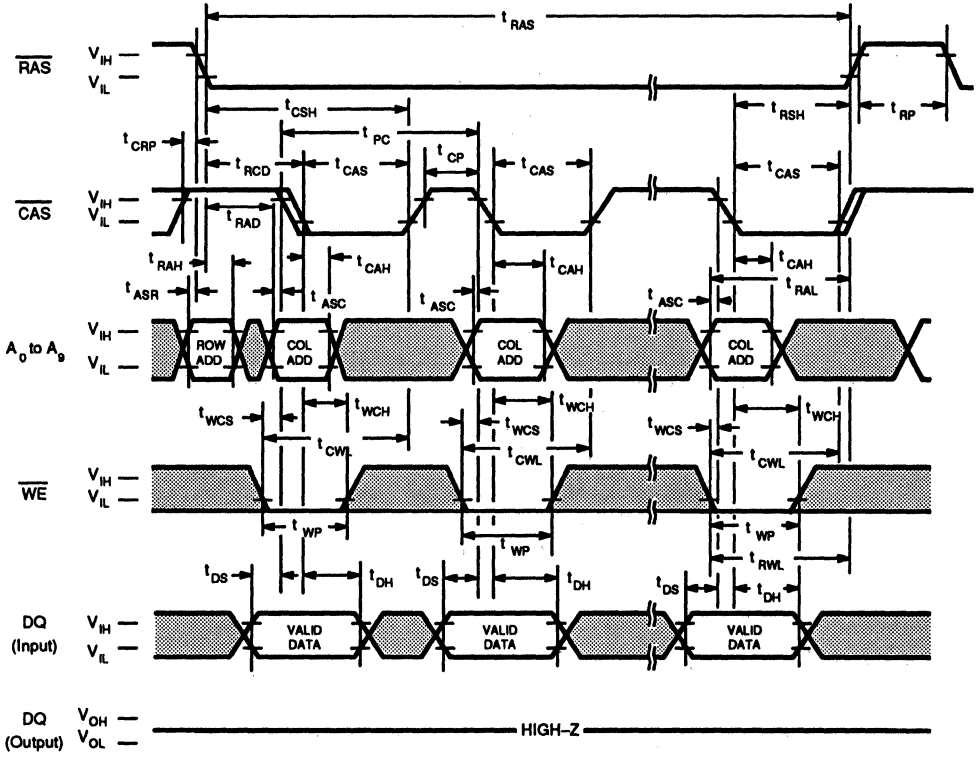


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occuring.

2

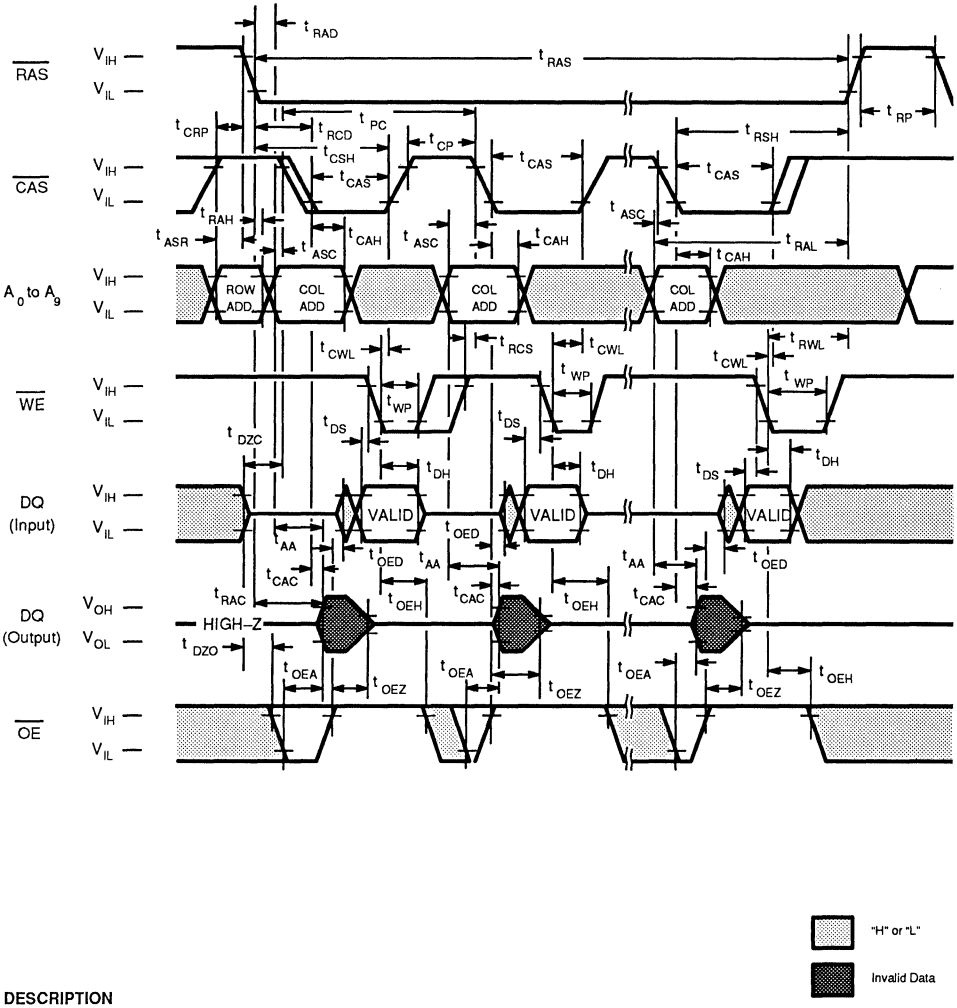
Fig. 9 — FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, t_{CWL} must be satisfied.

Fig. 10 — FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

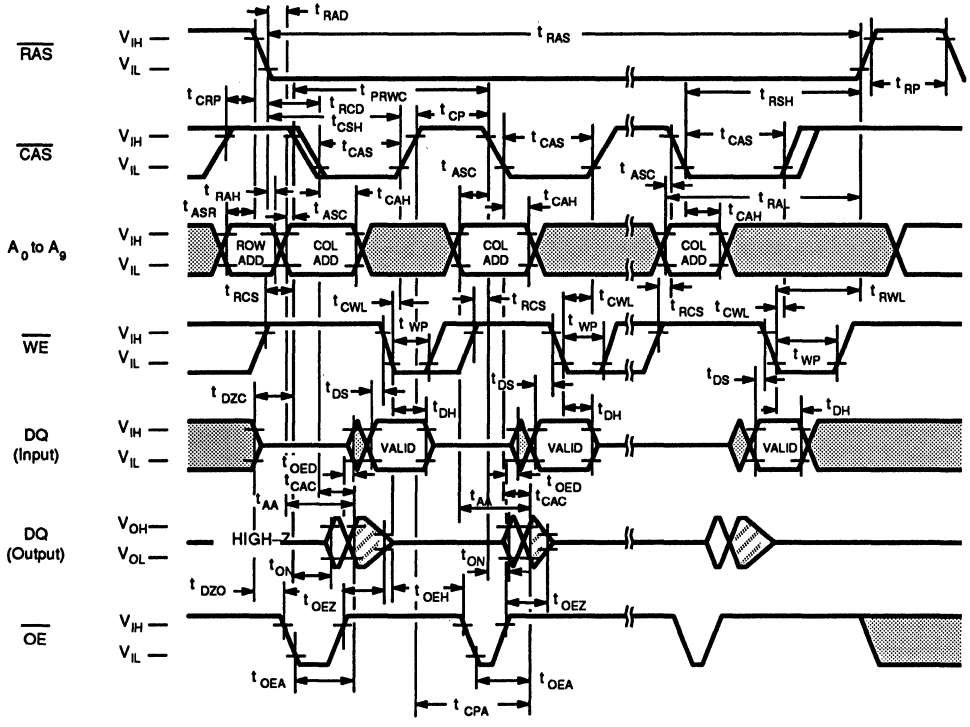


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

2

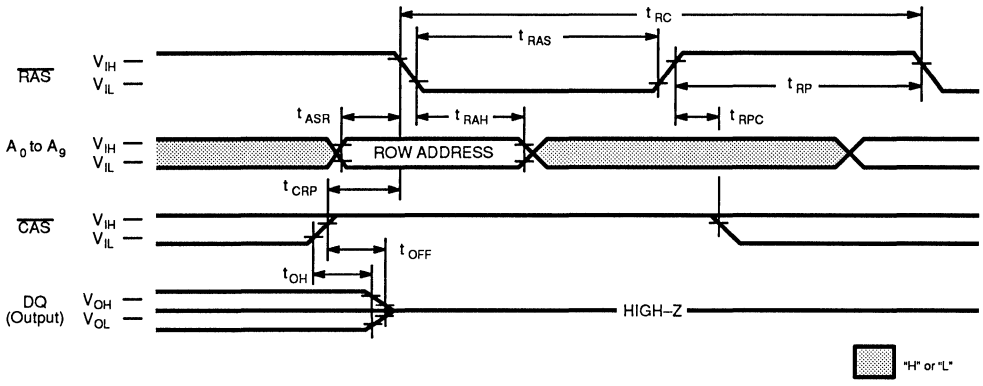
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 — $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

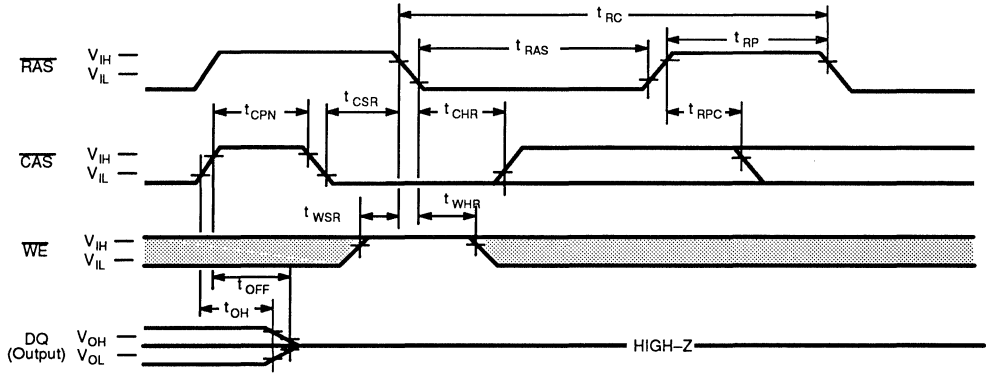


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read–modify–write cycle at each of 1024 row addresses every 16.4–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$–before–$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DQ pins are kept in a high–impedance state.

Fig. 13 — $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{OE}$ = "H " or "L")



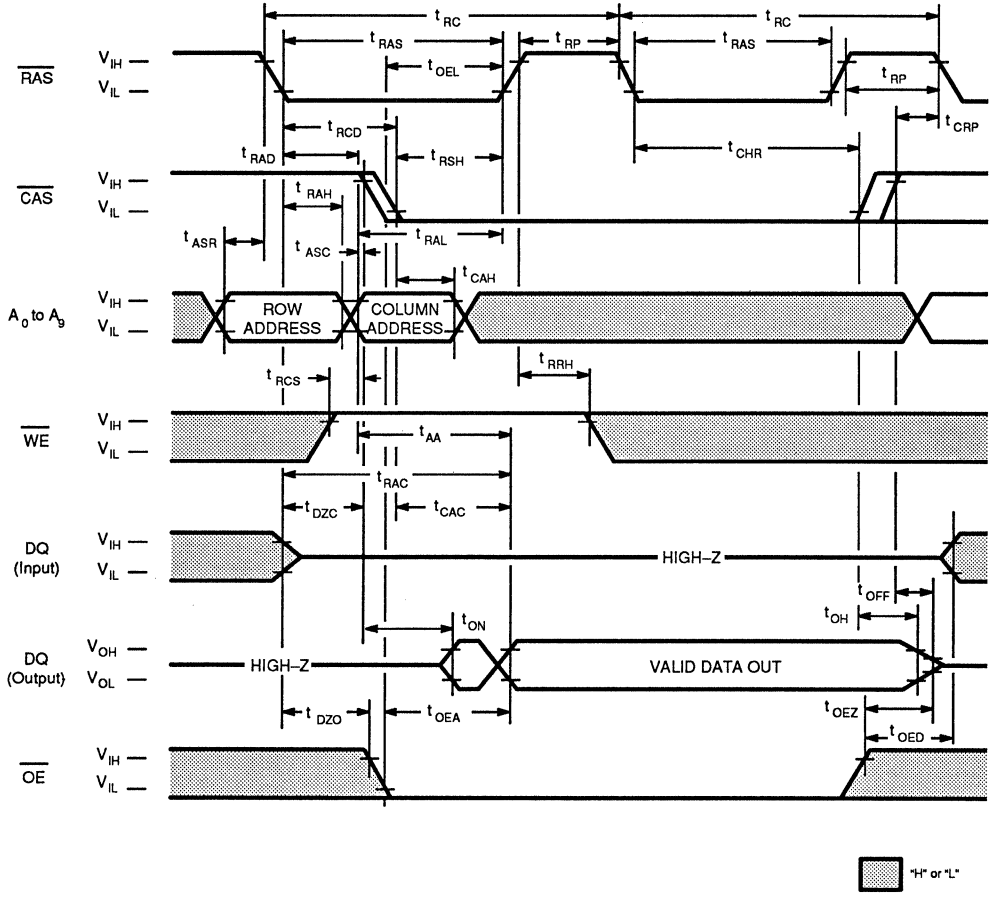
DESCRIPTION

$\overline{CAS}$–before–$\overline{RAS}$ refresh is an on–chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on–chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$ –before–$\overline{RAS}$ refresh operation.

$\overline{WE}$ must be held High for the specified set up time (tWSR) before RAS goes Low in order not to enter "test mode" to be specified later.

2

Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

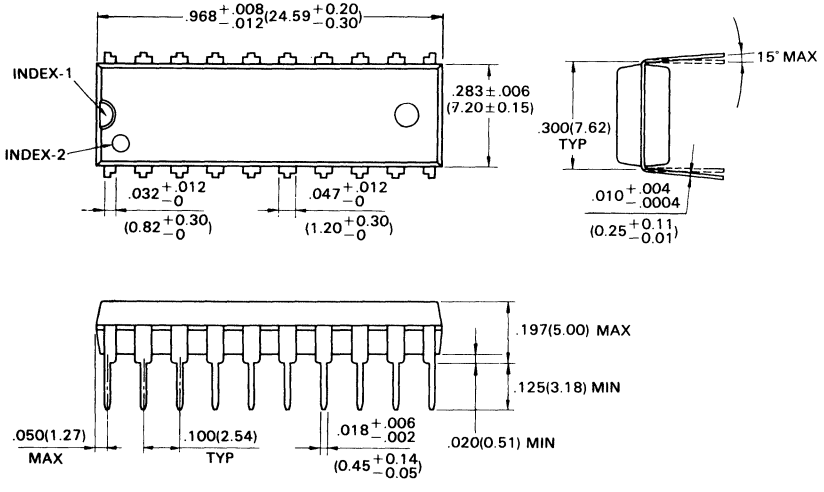
A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on–chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$–before–$\overline{RAS}$ refresh capability.

$\overline{WE}$ must be held High for the specified set up time (tWSR) before RAS goes Low in order not to enter "test mode" to be specified later.

PACKAGE DIMENSIONS

(Suffix : –P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. : DIP-20P-M03)



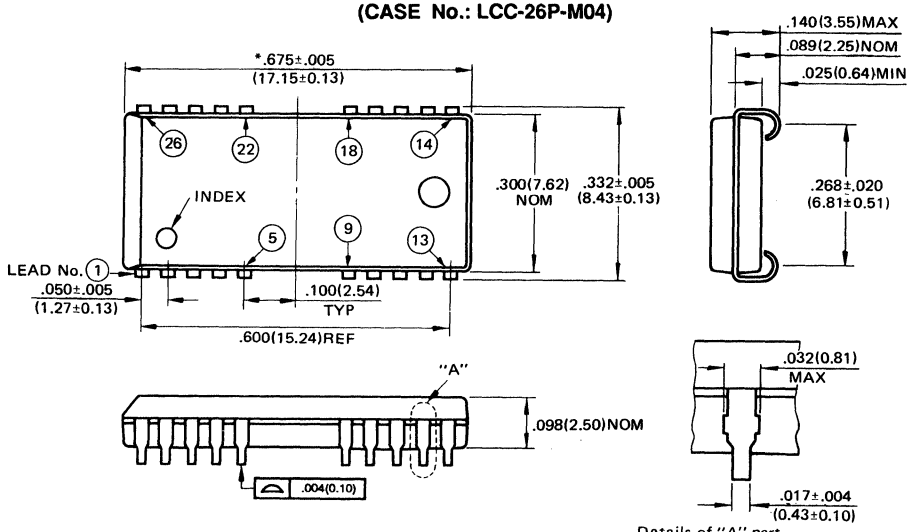
Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



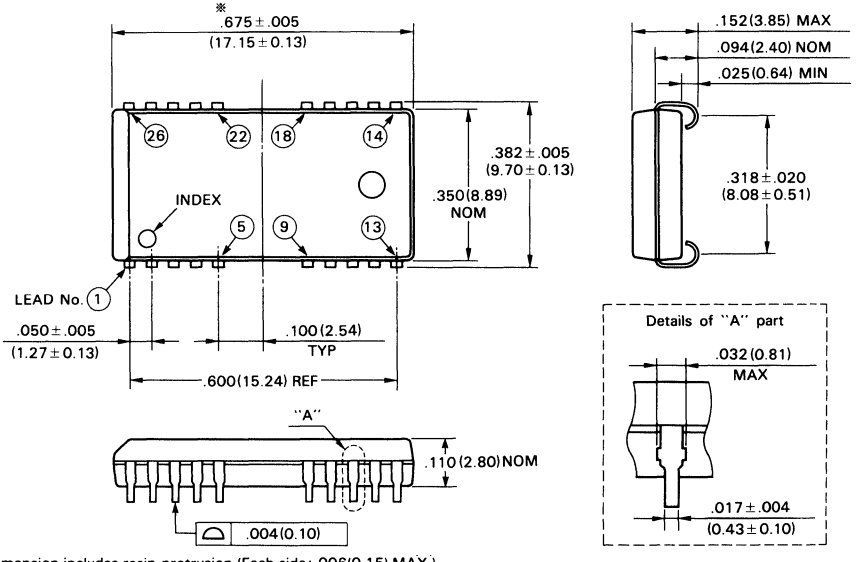
NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(Case No. : LCC-26P-M03)



※This dimension includes resin protrusion.(Each side: .006(0.15) MAX.)

Dimensions in
inches (millimeters).

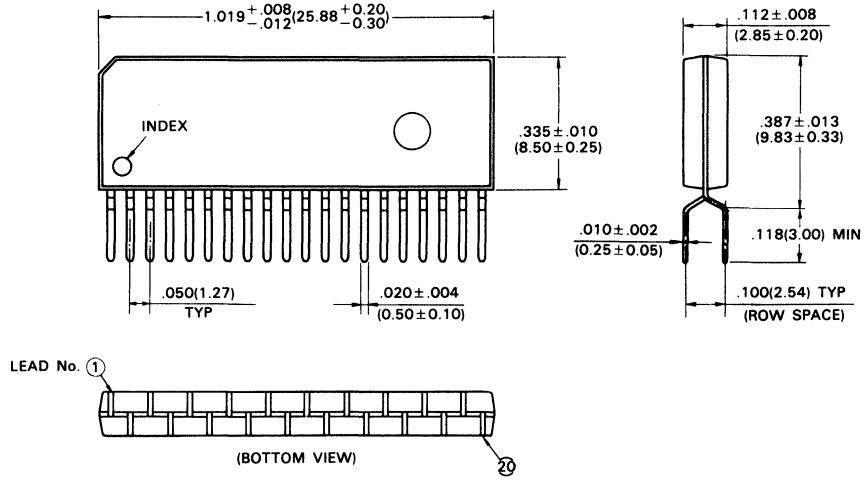
2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

November 1990
Edition 1.0

FUJITSU

DATA SHEET

MB814400-80L/-10L/-12L

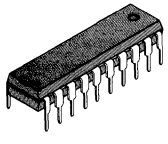
CMOS 1M x 4 BITS FAST PAGE MODE DYNAMIC RAM

CMOS 1M x 4 Bits Fast Page Mode Low Power Dynamic RAM

The Fujitsu MB814100 is a fully decoded CMOS dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x 1 configuration. The MB814100 features a fast page mode of operation whereby high-speed, random access of up to 2,048-bits of data within the same row can be selected. The MB814100 DRAM is ideally suited for mainframes, buffers, hand-held computers, and other memory applications where very low power dissipation and compact layout are basic requirements of the design. Since the standby current of the MB814100 is very low, the device can be used in equipment that uses batteries for primary and/or auxiliary power.

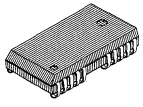
The MB814400 is fabricated using silicon gate CMOS and Fujitsu's advanced Four-layer Polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814100 are not critical and all inputs are TTL compatible.

ADVANCE INFORMATION

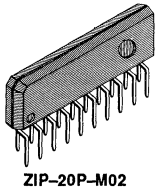


DIP–20P–M03

LCC–26P–M04



LCC–26P–M03



ZIP–20P–M02

T.B.D. T.B.D.

FPT–26P–M01 FPT–26P–M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Features

Parameter	MB814100-80L	MB814100-10L	MB814100-12L
$\overline{RAS}$ Access Time	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	155 ns min.	180 ns min.	210 ns min.
Address Access Time	45 ns max.	50 ns max.	60 ns max.
$\overline{CAS}$ Access Time	20 ns max.	25 ns max.	30 ns max.
Fast Page Mode Cycle Time	55 ns min.	60 ns min.	70 ns min.
Low Power Dissipation • Operating Current	413 mW max.	358 mW max.	303 mW max.
• Standby Current	11 mW max. (TTL level)/1.1 mW max. (CMOS level)		

- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 128 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Section 3

Application Specific DRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
3–3	MB81461–12 –15	120 150	DRAM: 262144 bits (64K x 4) SAM: 1024 bits (256 x 4)	24-pin Plastic DIP, ZIP
3–35	MB81461B–12 –15	120 150	DRAM: 262144 bits (64K x 4) SAM: 1024 bits (256 x 4)	24-pin Plastic DIP, ZIP
3–67	MB81C1501	25	Write: 1175040 bits (293760 x 4 x 1) Read: 1175040 bits (293760 x 4 x 2)	38-pin Plastic FPT

3

January 1990
Edition 3.1

FUJITSU

DATA SHEET

MB81461-12/-15

262,144-BIT DUAL PORT DYNAMIC RANDOM ACCESS MEMORY

262,144 Bit Dual Port DRAM

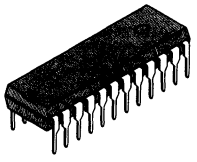
The Fujitsu MB81461 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits dynamic RAM port and 256 words by 4 bits serial access memory (SAM) port.

The DRAM port is identical to the Fujitsu MB81464 with four bits of parallel random access I/O while the SAM port is designed as four 256-bit registers, each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

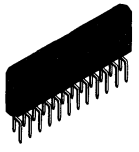
The MB81461 offers complementary asynchronous access of both the DRAM and SAM ports, except when data is transferred between them internally. The design is optimized for high speed and performance making the MB81461 the most efficient solution for implementing the frame buffer of a bit-mapped video display system. Multiplexed row and column address inputs permit the MB81461 to be housed in a 400-mil wide 24-pin DIP or ZIP package. Pinouts conform to the JEDEC-approved pinouts.

The MB81461 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process technology. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimum chip size. All inputs and outputs are TTL compatible.

- Dual Port Organization
  64 K x 4 Dynamic RAM port (DRAM)
  256 x 4 Serial Access Memory port (SAM)
- 24-pin DIP and ZIP packages
- Silicon-gate, Triple Poly NMOS, single transistor cell
- DRAM Port
  Access Time (t_{RAC})
  120 ns max. (MB 81461-12)
  150 ns max. (MB 81461-15)
  Cycle Time (t_{SAC})
  230 ns max. (MB 81461-12)
  260 ns max. (MB 81461-15)
- SAM Port
  Access Time (t_{SAC})
  40 ns max. (MB 81461-12)
  60 ns max. (MB 81461-15)
  Cycle Time (t_{SC})
  40 ns max. (MB 81461-12)
  60 ns max. (MB 81461-15)
- Single +5 V Supply, ±10% tolerance
- Real Time, Read Transfer capability
- Page Mode capability
- Power Dissipation
  DRAM; Act/SAM; Stby
  523 mW max. (MB 81461-12)
  468 mW max. (MB 81461-15)
  DRAM; Stby/SAM; Act
  275 mW max. (MB 81461-12)
  220 mW max. (MB 81461-15)
  DRAM; Stby/SAM; Stby
  110 mW max.
- Bi-directional data transfer between DRAM and SAM
- Fast serial access asynchronous to DRAM except transfer operation
- Bit Masked Write Mode capabiltiy
- 256 refresh cycles every 4 ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, Hidden Refresh capability
- Delayed write and Read-Modify-Write capability
- Standard 24-Pin Plastic Packages:
  DIP (MB81461-XXP)
  ZIP (MB81461-XXPSZ)

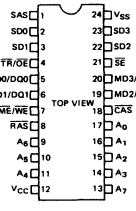


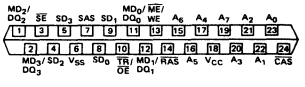
PLASTIC PACKAGE
DIP-24P-M04



PLASTIC PACKAGE
ZIP-24P-M02

PIN ASSIGNMENT





BOTTOM VIEW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

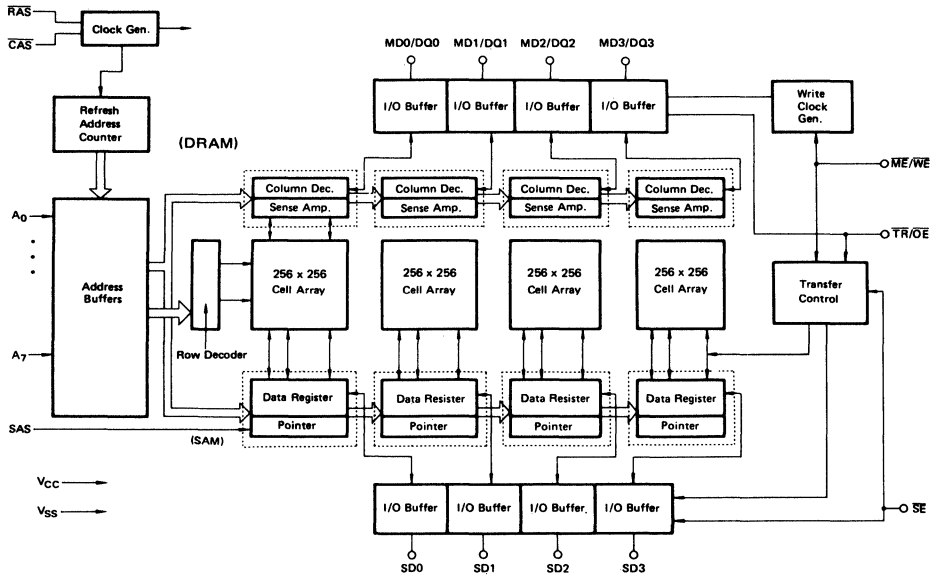
Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 – BLOCK DIAGRAM OF MB 81461 and PIN DESCRIPTION

Block Diagram



Pin Description

Pin Number		Symbol	Parameter	Mode
DIP	ZIP			
1	7	SAS	Serial Access Memory Strobe	Input
2,3,22,23	8,9,4,5	SD0 to SD3	Serial Data I/O	I/O
4	10	$\overline{TR}/\overline{OE}$	Transfer Enable/ Output Enable	Input
5,6,19,20	11,12,1,2	MD0/DQ0 to MD3/DQ3	Mask Data/Data I/O	I/O
7	13	$\overline{ME}/\overline{WE}$	Mask Mode Enable/Write Enable	Input
8	14	$\overline{RAS}$	Row Address Strobe	Input
17, 16, 15 14, 11, 10 9, 13	23,22,21, 20,17,16, 15,19	A_0 to A_7	Address Input	Input
12	18	V_{CC}	Supply Voltage +5 V	Power Supply
18	24	$\overline{CAS}$	Column Address Strobe	Input
21	3	$\overline{SE}$	Serial port Enable	Input
24	6	V_{SS}	Ground	Power Supply

DESCRIPTION

DRAM OPERATION

$\overline{RAS}$;

This pin is used to strobe eight row-address inputs from A0 to A7 pins and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by $\overline{TR}/\overline{OE}$ and bit mask write cycle or not (by $\overline{ME}/\overline{WE}$ and MD0/DQ0 to MD3/DQ3). Since $\overline{RAS}$ = "L" is the active condition of circuit, to maintain $\overline{RAS}$ = "H" (standby condition) is effective to save power dissipation.

$\overline{CAS}$;

This pin is used to strobe eight column address inputs at the falling edge. $\overline{CAS}$ pin has the function to enable and disable the output at "L" and "H" respectively during the read operation.

Another function of $\overline{CAS}$ is to select "early write" mode conditioned by $\overline{ME}/\overline{WE}$ = "L".

$\overline{ME}/\overline{WE}$;

This pin is used to select read or write cycle. $\overline{ME}/\overline{WE}$ = "L" select write mode and $\overline{ME}/\overline{WE}$ = "H" select read mode. This pin is also used to enable bit mask write cycle. If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write is enabled.

$\overline{TR}/\overline{OE}$;

This pin is used to select Transfer operation or not at the falling edge of $\overline{RAS}$, $\overline{TR}/\overline{OE}$ = "H" enables DRAM operation and $\overline{TR}/\overline{OE}$ = "L" enables Transfer operation between DRAM and SAM. After the falling of $\overline{RAS}$ with t_{YH}, this pin is used for output enable.

The $\overline{TR}/\overline{OE}$ controls the impedance of the output buffers. $\overline{TR}/\overline{OE}$ = "H" forces the output buffers at high impedance state. $\overline{TR}/\overline{OE}$ = "L" leads the output buffers at low impedance state. But in early write cycle, the output buffers are high impedance state even if $\overline{TR}/\overline{OE}$ is low.

A0 to A7;

These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB 81461. The eight row address inputs are strobed by $\overline{RAS}$ and followed eight column address inputs are strobed by $\overline{CAS}$. These are used to select the start address of serial access memory also.

MD0/DQ0 to MD3/DQ3

These are common I/O pins of DRAM port. I/O mode is as specified for each function mode in the truth table.

Data Outputs:

The output buffers have three-state capability "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read" or "read-modify-write" mode. During a refresh cycle, either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ mode is selected, output buffers are set in "High-Z" state.

Data inputs:

These are used as data input pins when a data write mode such as "Early-Write", "Delayed Write" or "Read-modify-Write" is selected. In any of the above cases, these pins are set at "High-Z" state to enable data-in without any bus conflict.

In any operation mode, read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$ and/or $\overline{TR}/\overline{OE}$. When "Bit mask write" mode is set, these pins are used as a control signal for write inhibit with MDi/DQi = "L" on the selected bit i.

Page Mode;

The page mode operation is to strobe the column address by $\overline{CAS}$ while $\overline{RAS}$ is maintained at "L" through all the successive memory operations if the row address doesn't change. This mode can save power dissipation and get the faster access time due to the elimination of $\overline{RAS}$ falling edge function.

Refresh;

Refresh of the DRAM cells is performed for every 256 rows per every 4 milliseconds.

The MB 81461 offers the following three types of refresh.

1) $\overline{RAS}$-Only refresh; The $\overline{RAS}$-Only refresh is performed with $\overline{CAS}$="H" condition. Strobing every 256 row addresses with $\overline{RAS}$ will complete all bits of memory cell to be refreshed while all outputs are invalid due to "High-Z" state. Further $\overline{RAS}$-only refresh saves the power dissipation substantially.
2) $\overline{CAS}$-before-$\overline{RAS}$ refresh; The $\overline{CAS}$-before-$\overline{RAS}$ refresh offers an alternate refresh method. If $\overline{CAS}$ is set low for the specified period (t_{FCS}) before the falling edge of $\overline{RAS}$, refresh control clock generator and refresh address counter are enabled, and an refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3) Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending $\overline{CAS}$ low. The hidden refresh is equivalent to $\overline{CAS}$-before-$\overline{RAS}$ refresh because $\overline{CAS}$ stays low when $\overline{RAS}$ goes to low in the next cycle.

Bit Mask Write;

This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$ during write mode (early, delayed write or read-modify-write cycle). The bits to be masked (or inhibited to write) is determined by MD/DQ state at the falling edge of $\overline{RAS}$, for example, if MD0/DQ0 and $\overline{ME}/\overline{WE}$ are both low at the falling edge of $\overline{RAS}$, the data on MD0/DQ0 pin is not written into the cell during the cycle. Refer to the Fig. 2.

3

EXAMPLE OF BIT MASK WRITE OPERATION

Falling edge of $\overline{RAS}$						Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	Write enable
	L	H	L	H	L	Write enable for DQ0 and DQ2 Write disable for DQ1 and DQ3

X: Don't Care

FUNCTIONAL TRUTH TABLE FOR DRAM OPERATION

$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$	$\overline{TR}/\overline{OE}$	ADDRESSES	MD0/DQ0 to MD3/DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L*	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H → X → H	Valid	Valid Data In	Delayed Write
L	L	H→L	H→L→H	Valid	Valid Data Out → Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	$\overline{RAS}$-Only Refresh
H→L	L	X	H→X	X	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh

*: If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write mode is enabled.

3

TRANSFER OPERATION:

The transfer operation is featured in the MB 81461B. This mode is used to transfer simultaneously 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of $\overline{ME}/\overline{WE}$ at the falling edge of $\overline{RAS}$. $\overline{ME}/\overline{WE}$="H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and $\overline{ME}/\overline{WE}$="L" defines the transfer from SAM to DRAM (Write Transfer Cycle).

I/O mode of SD0 to SD3 determined while the transfer operation is set ($\overline{TR}/\overline{OE}$="L") conjunctioned with $\overline{ME}/\overline{WE}$ state.

After Read Transfer Cycle, please apply two or more SAS Clock.

$\overline{TR}/\overline{OE}$;

This pin is used to enable transfer operation at the falling edge of $\overline{RAS}$.

$\overline{ME}/\overline{WE}$;

This pin is used to select the direction of transfer at the falling edge of $\overline{RAS}$.

A0 to A7;

These pins are used to select the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by $\overline{RAS}$ and the start address is strobed by $\overline{CAS}$.

Pseudo Write Transfer:

To start serial write cycle, the SD pins must be set in input mode. To do this, write transfer cycle should be executed. The pseudo write transfer cycle is to change the SD pins into input mode without data transfer from SAM to DRAM. Refer to Fig. 3.

Refresh during transfer cycle;

DRAM and SAM are refreshed during transfer cycle as shown below.

1) Read transfer cycle:
   During read transfer cycle, the selected row address of DRAM to be transfered to SAM is refreshed. SAM data are kept by applying 256 SAS clocks within 4 ms after the read transfer cycle.
2) Write transfer cycle:
   During write transfer cycle, the new data are written from SAM to DRAM and this row address should be refreshed within 4 ms.
   But SAM data are not refreshed during write transfer cycle. Therefore, the SAM refresh (applying 256 SAS clocks within 4 ms) must be executed. Especially, when the write transfer cycle is executed continuously, 256 SAS clock should be applied within 4 ms.

SERIAL ACCESS OPERATION:

The MB 81461 has 256 words by 4 bits Serial Acess Memory (SAM) corresponding to 64K words by 4 bits DRAM and the fast serial read/write access is achieved by SAM architecture. Read or write cycle is determined when the last read or write transfer operation is executed. If the last transfer operation was read transfer, the serial read cycle is performed until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write or pseudo write transfer, the serial write cycle is performed. In the serial write operation, 256 words by 4 bits data stored in the SAM can be transfered to DRAM under $\overline{SE}$="L" condition, and $\overline{SE}$="H" condition disables data transfer from SAM to DRAM. The serial access operation can be done asynchronously from DRAM port.

SAS;

This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data of the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, out-

put data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returnes to #0 (Least Significant Address).

$\overline{SE}$;
This pin is used to enable serial access operation by bit to bit. $\overline{SE}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{SE}$ = "H" leads SD pins to "High-Z" state. $\overline{SE}$ = "L" leads SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by last occured transfer operation, if last transfer operation was read transfer mode, they are output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is constructed by dynamic circuitry, the refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4ms in either output or input mode. $\overline{SE}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is applicable to obtain valid data continuously when row address is changed without any timing loss from the last bit of previous row to the first bit of new row. Data transfer from DRAM to SAM is triggered by rising edge of $\overline{TR/OE}$ after the preparation of internal circuit for this operation, while SAM port can continue read operation asynchronously from the above mentioned internal move. Once $\overline{TR/OE}$ returns to "H" with the restricted timing specification t_{TSL} and t_{TSD} refered to SAS clock, SD pins can get the valid output data continuously as shown in Fig. 4. The key issue to achieve this feature is to apply SAS clock continuously with the timing consideration to the rising edge of $\overline{TR/OE}$.

3

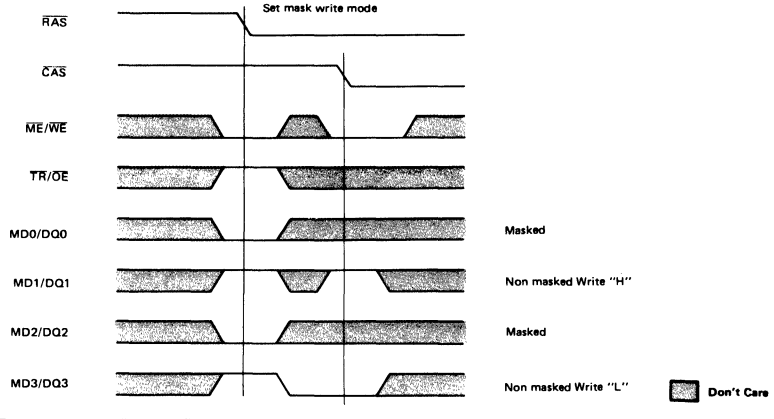
FUNCTIONAL TRUTH TABLE FOR SERIAL ACCESS (Asynchronous from DRAM port)

Falling edge of $\overline{RAS}$		SAS	$\overline{SE}$	SD0 to SD3	Function
$\overline{TR/OE}$	$\overline{ME/WE}$				
H	X	Clock	L	Input/Output*	Sequential access enable
		Clock	H	Input/Output*	Sequential access disable

*: The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.

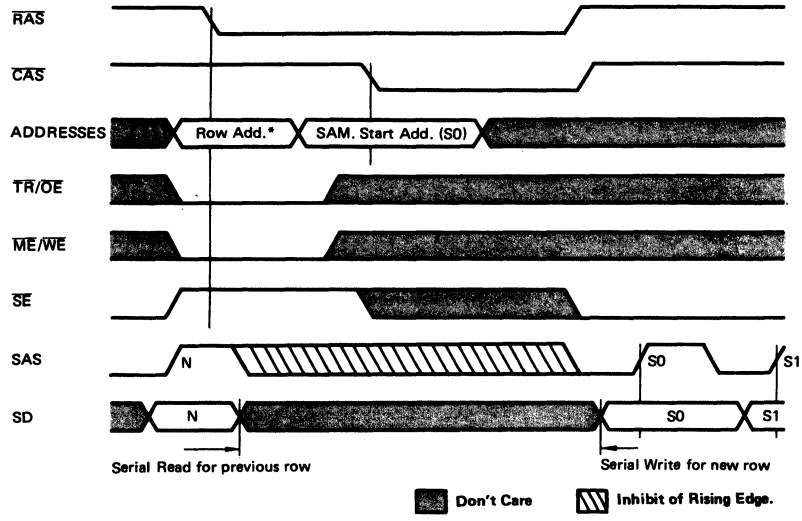
X; Don't Care

Fig. 2 – EXAMPLE OF BIT MASK WRITE OPERATION



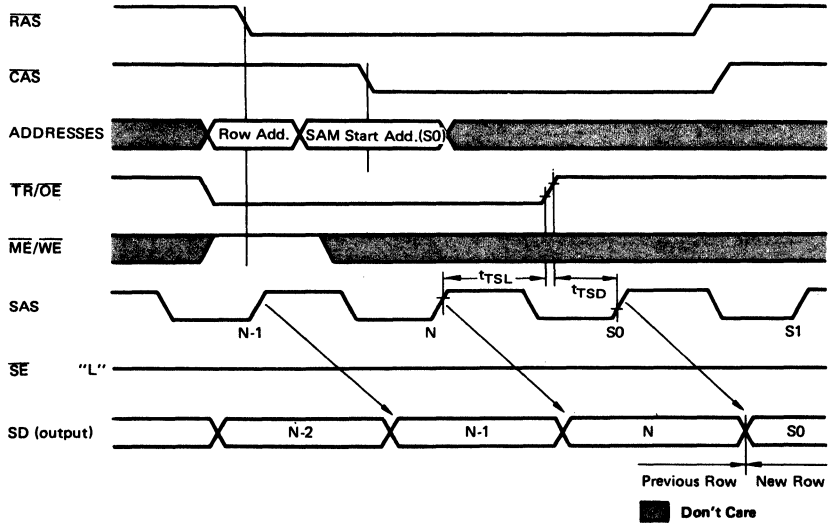
3

Fig. 3 – EXAMPLE OF PSEUDO WRITE TRANSFER CYCLE



*The DRAM data of this row address are refreshed during pseudo write transfer cycle.

Fig. 4 – EXAMPLE OF REAL TIME READ TRNASFER OPERATION



RECOMMENDED OPERATING CONDITIONS
(Referenced to V_{SS})

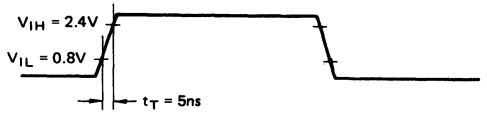
Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}	-2.0		0.8	V	

CAPACITANCE (T_A=25°C)

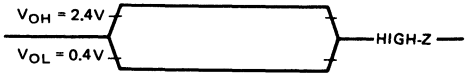
Paramter	Symbol	Typ	Max		Unit
			DIP	ZIP	
Input Capacitance (A0 to A7)	C_{IN1}		7	8	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{SE}$, $\overline{TR}$/$\overline{OE}$)	C_{IN2}		10	12	pF
Input Capacitance (SAS)	C_{IN3}		7	7	pF
Input/Output Capacitance (MD0/DQ0 to MD3/DQ3)	C_{IO1}		7	8	pF
Input/Output Capacitance (SD0 to SD3)	C_{IO2}		7	8	pF

AC TEST CONDITIONS

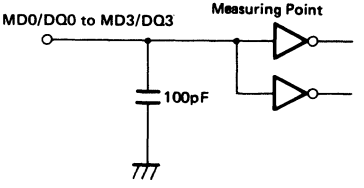
1) Input

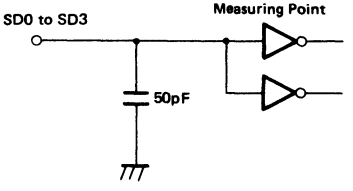


2) Output



3) Output Load





DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
SAM STANDBY $\overline{SE}$ = V_{IH}, SAS = V_{IL}					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC1}		95	mA
	MB 81461-15			85	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		20	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC3}		77	mA
	MB 81461-15			70	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min)	MB 81461-12	I_{CC4}		50	mA
	MB 81461-15			45	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC5}		77	mA
	MB 81461-15			70	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC6}		110	mA
	MB 81461-15			100	
SAM ACTIVE $\overline{SE}$ = V_{IL}, t_{SC} = min					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC7}		130	mA
	MB 81461-15			110	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MB 81461-12	I_{CC8}		50	mA
	MB 81461-15			40	
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC9}		112	mA
	MB 81461-15			95	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)	MB 81461-12	I_{CC10}		85	mA
	MB 81461-15			70	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC11}		112	mA
	MB 81461-15			95	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC12}		145	mA
	MB 81461-15			125	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, V_{CC}=5.5V, V_{SS}=0V, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH}=-5mA/-2mA for DQi/SDi) Output low voltage (I_{OL}=4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

3

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1 2 3

Parameter	NOTES	Symbol	MB 81461-12		BM 81461-15		Unit
			Min	Max	Min	Max	
Time between Refresh (RAM/SAM)		t_{REF}		4		4	ms
Random Read/Write Cycle Time		t_{RC}	230		260		ns
Read-Modify-Write Cycle Time		t_{RWC}	305		345		ns
Page Mode Cycle Time		t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	25	0	35	ns
Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	60000	150	60000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60		75		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time (Normal cycle)		t_{CPN}	40		50		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50		60		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$)		t_{CPR}	25		30		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	60000	75	60000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		ns
Write Command Set Up Time		t_{WCS}	-5		-5		ns
Write Command Hold Time		t_{WCH}	30		35		ns
Write Command Pulse Width		t_{WP}	30		35		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from $\overline{TR}/\overline{OE}$	6	t_{OEA}		35		40	ns
$\overline{TR}/\overline{OE}$ to Data In Delay Time		t_{OED}	25		30		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Output Buffer Turn Off Delay from $\overline{TR}/\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{TR}/\overline{OE}$ Hold Time Referenced to $\overline{ME}/\overline{WE}$		t_{OEH}	0		0		ns
$\overline{TR}/\overline{OE}$ to $\overline{RAS}$ inactive Set Up Time		t_{OES}	0		0		ns
Data In to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		ns
Data In to $\overline{TR}/\overline{OE}$ Delay Time	16	t_{DZO}	0		0		ns
Refresh Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCS}	25		30		ns
Refresh Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	20		20		ns
Serial Clock Cycle Time		t_{SC}	40	50000	60	50000	ns
Access Time from SAS	10	t_{SAC}		40		60	ns
Access Time from $\overline{SE}$	10	t_{SEA}		40		50	ns
SAS Precharge Time		t_{SP}	10		20		ns
SAS Pulse Width		t_{SAS}	10		20		ns
$\overline{SE}$ Precharge Time		t_{SEP}	25		45		ns
$\overline{SE}$ Pulse Width		t_{SE}	25		45		ns
Serial Data Out Hold Time after SAS High		t_{SOH}	10		10		ns
Serial Output Buffer Turn Off Delay from $\overline{SE}$		t_{SEZ}	0	25	0	30	ns
Serial Data In Set Up Time	11	t_{SDS}	0		0		ns
Serial Data In Hold Time	11	t_{SDH}	20		25		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{TS}	0		0		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{RTH}	90		110		ns
Write Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time	12	t_{RTHW}	12		15		ns
Transfer Command ($\overline{TR}$) to $\overline{CAS}$ Hold Time		t_{CTH}	30		35		ns
Transfer Command ($\overline{TR}$) to SAS Lead Time		t_{TSL}	5		10		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Lead Time		t_{TRL}	130		140		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Delay Time		t_{TRD}	-65		-50		ns
First SAS Edge to Transfer Command Delay Time		t_{TSD}	25		35		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Set Up Time		t_{WSR}	0		0		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Hold Time		t_{RWH}	12		15		ns
Mask Data (MD) to $\overline{RAS}$ Set Up Time		t_{MS}	0		0		ns
Mask Data (MD) to $\overline{RAS}$ Hold Time		t_{MH}	35		45		ns
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	12	t_{SDZ}	10	60	10	75	ns
Serial Output Buffer Turn On Delay from $\overline{RAS}$	13	t_{SRO}	0		0		ns
SAS to $\overline{RAS}$ Set Up Time	11	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS Delay Time	12	t_{SRD}	30		45		ns
Serial Data Input to $\overline{SE}$ Delay Time		t_{SZE}	0		0		ns
Serial Data Input Delay from $\overline{RAS}$	12	t_{SDD}	60		75		ns

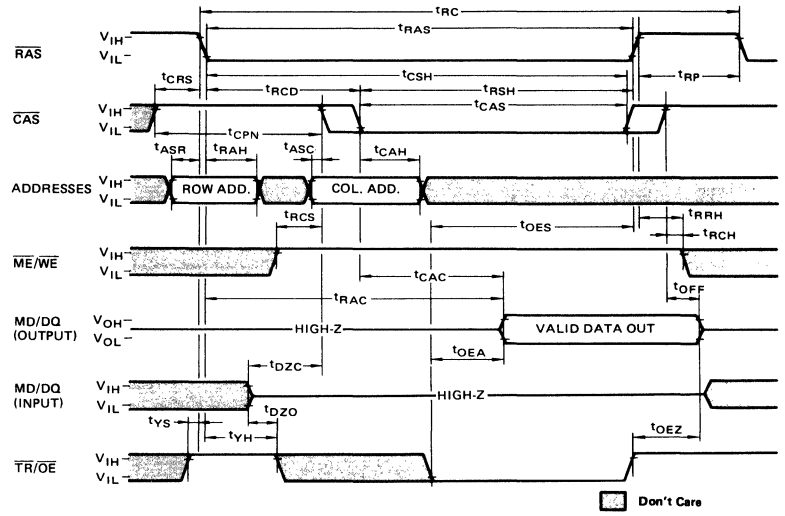
AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Serial Data Input to $\overline{RAS}$ Delay Time	13	t_{SZS}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Set up Time	14	t_{ESR}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	14	t_{REH}	12		15		ns
Serial Write Enable Set up Time	11	t_{SWS}	20		30		ns
Serial Write Enable Hold Time	11	t_{SWH}	80		120		ns
Serial Write Disable Set Up Time	11	t_{SWIS}	20		30		ns
Serial Write Disable Hold Time	11	t_{SWIH}	40		60		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{YS}	0		0		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{YH}	12		15		ns
Time between Transfer	15	t_{REFT}		4		4	ms

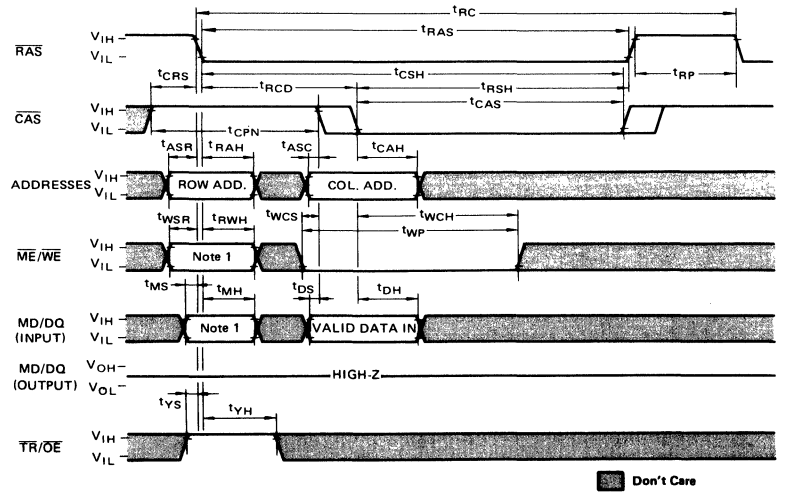
NOTES;

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 transfer, and 8 SAS cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycle are required
2. AC characteristics assume
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Measured with a load equivalent to 2 TTL loads and 50pF.
11. Input mode only
12. Write transfer and pseuso write transfer only.
13. Read transfer only in the case that the previous transfer was write transfer.
14. Pseudo write transfer only.
15. If t_{REFT} is not satisfied, 8 transfer and 8 SAS cycles before proper device operation is needed.
16. Either t_{DZC} or t_{DZO} must be satisfied.

READ CYCLE

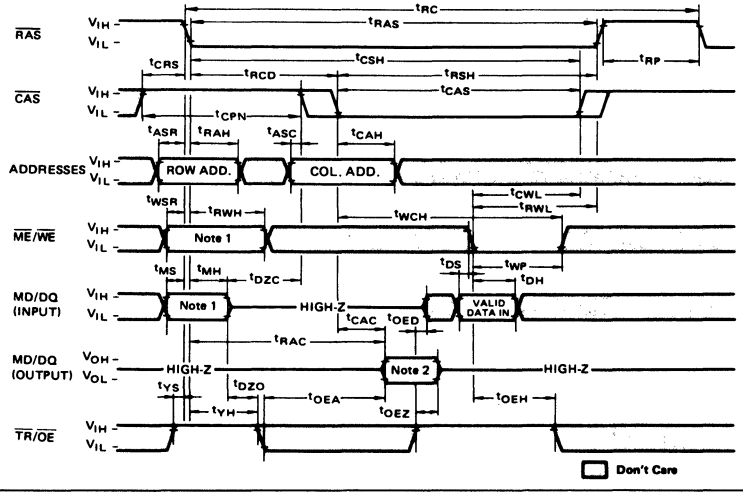


WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

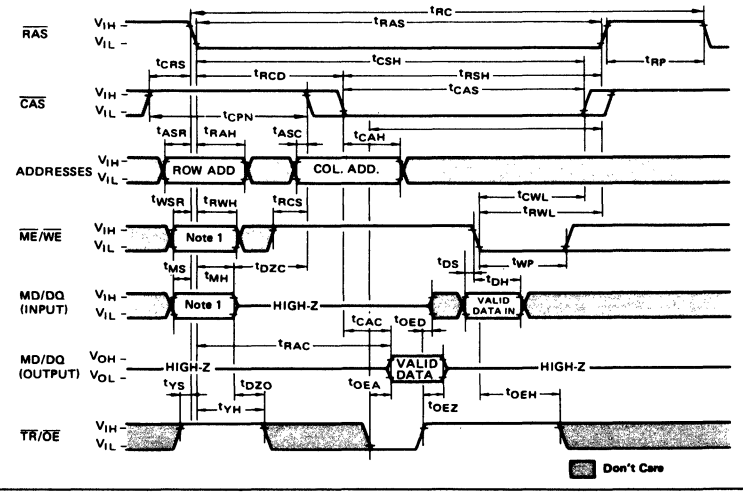
DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

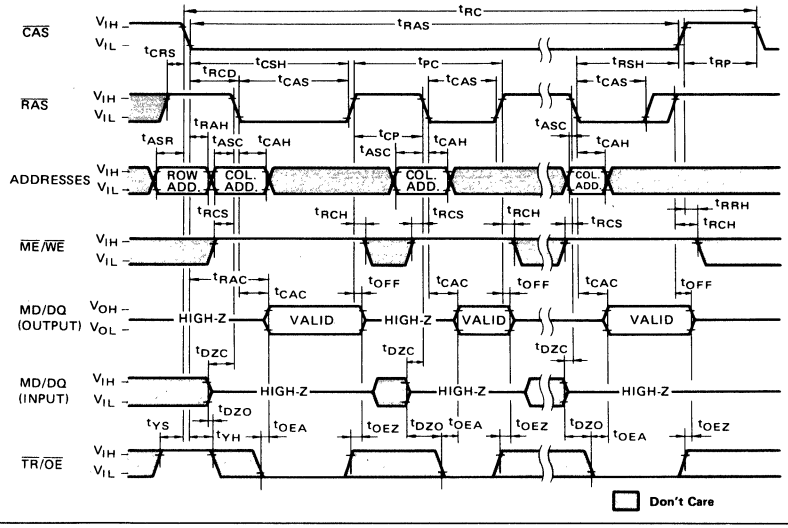
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

READ-MODIFY-WRITE CYCLE

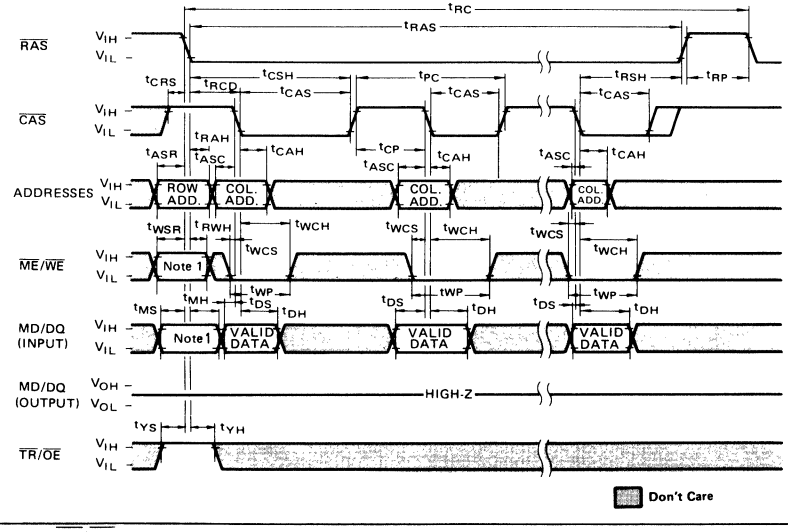


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

PAGE MODE READ CYCLE

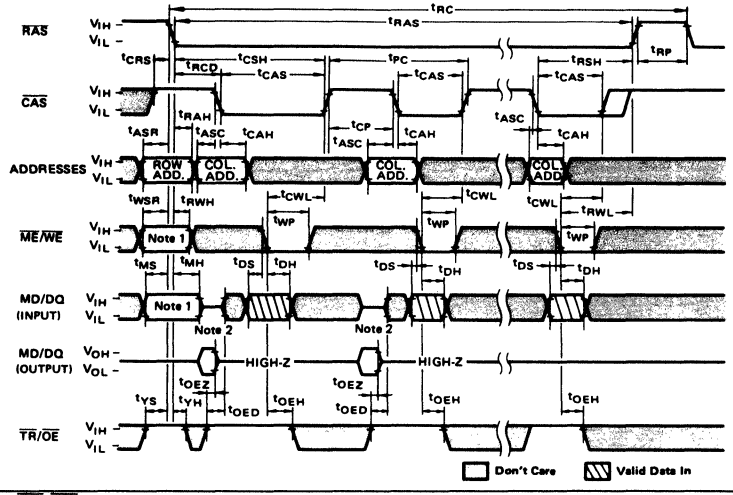


PAGE MODE WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

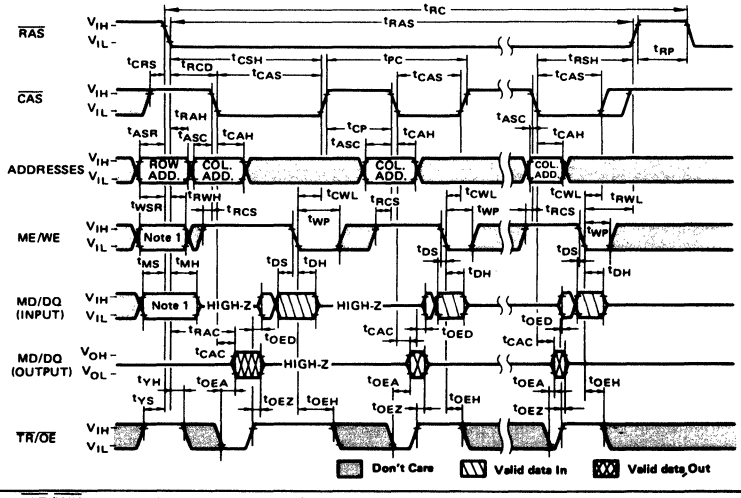
PAGE MODE DELAYED WRITE CYCLE



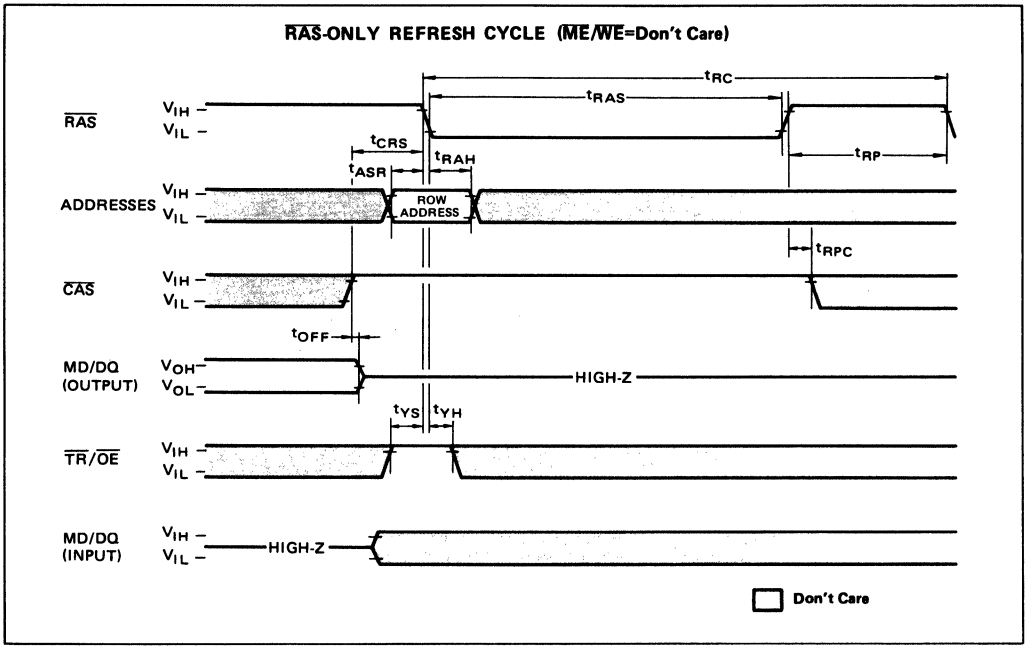
Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

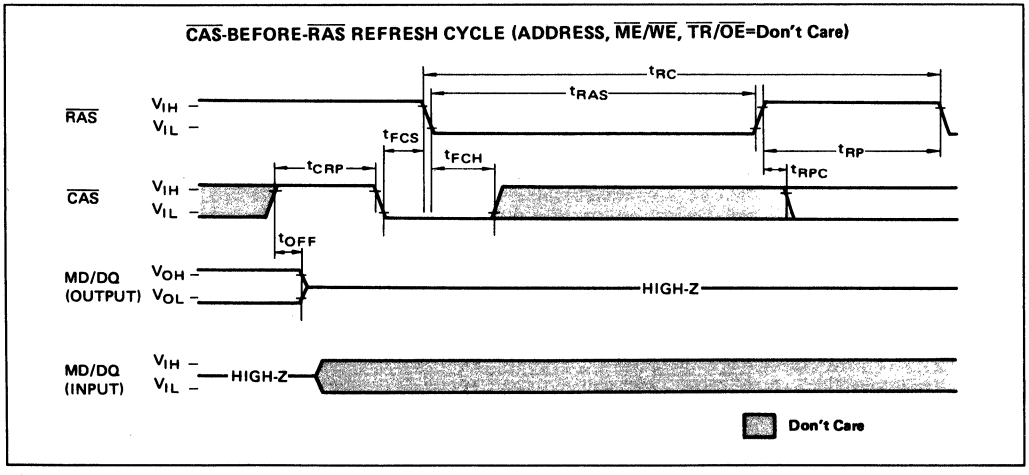
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

PAGE MODE READ-MODIFY-WRITE CYCLE

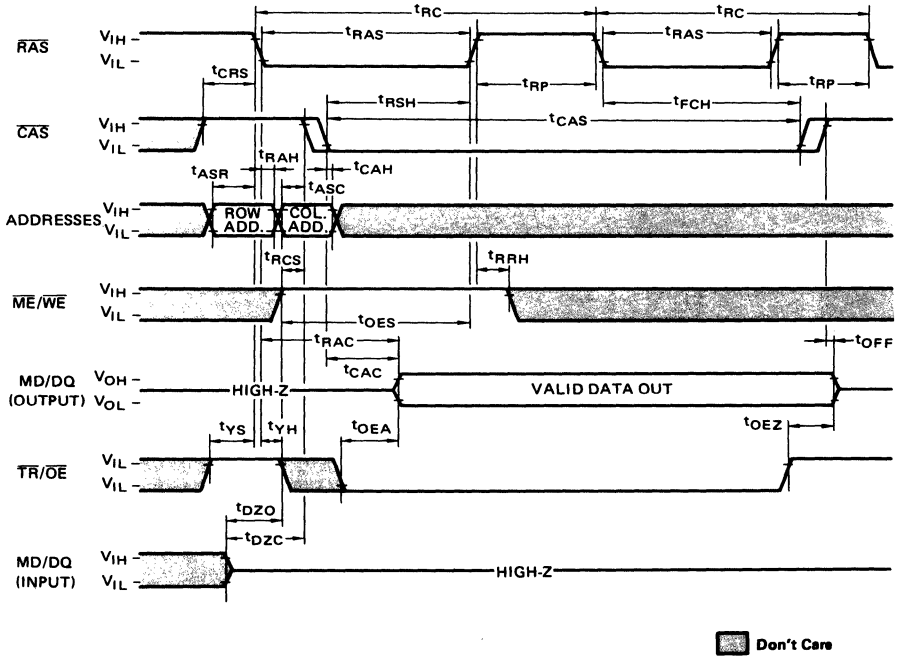


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.


RAS-ONLY REFRESH CYCLE (ME/WE=Don't Care)
tRC
tRAS
RAS
VIH
VIL
tCRS
tRAH
tASR
tRP
ADDRESSES
ROW ADDRESS
tRPC
CAS
tOFF
MD/DQ (OUTPUT)
VOH
VOL
HIGH-Z
tYS
tYH
TR/OE
MD/DQ (INPUT)
Don't Care


CAS-BEFORE-RAS REFRESH CYCLE (ADDRESS, ME/WE, TR/OE=Don't Care)
tRC
tRAS
RAS
VIH
VIL
tFCS
tFCH
tRP
tCRP
tRPC
CAS
tOFF
MD/DQ (OUTPUT)
VOH
VOL
HIGH-Z
MD/DQ (INPUT)
Don't Care

HIDDEN REFRESH CYCLE



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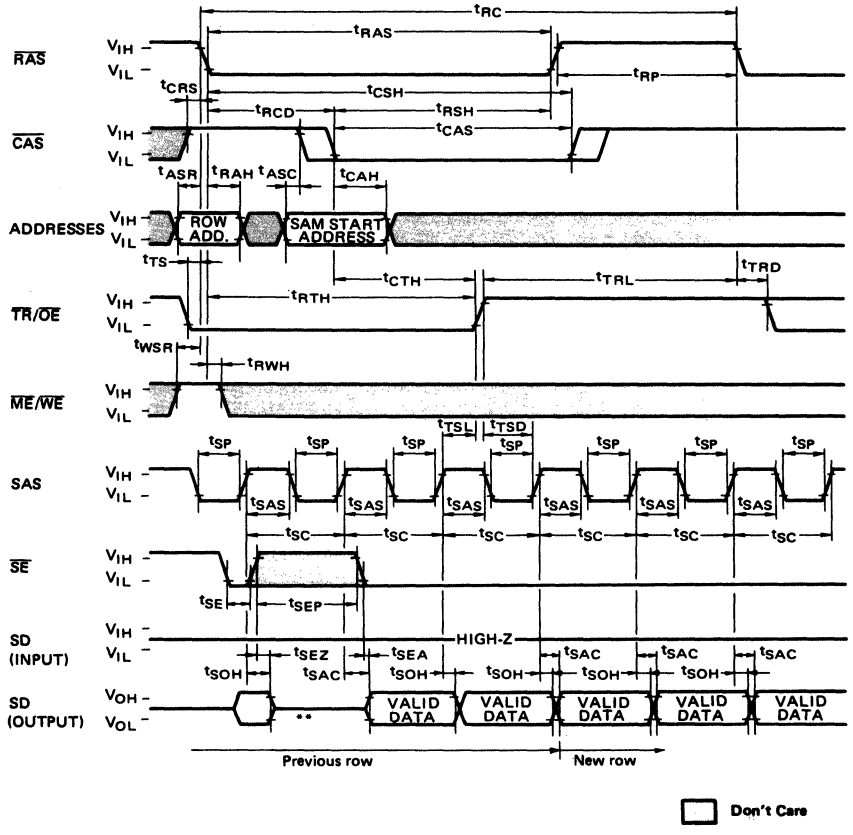
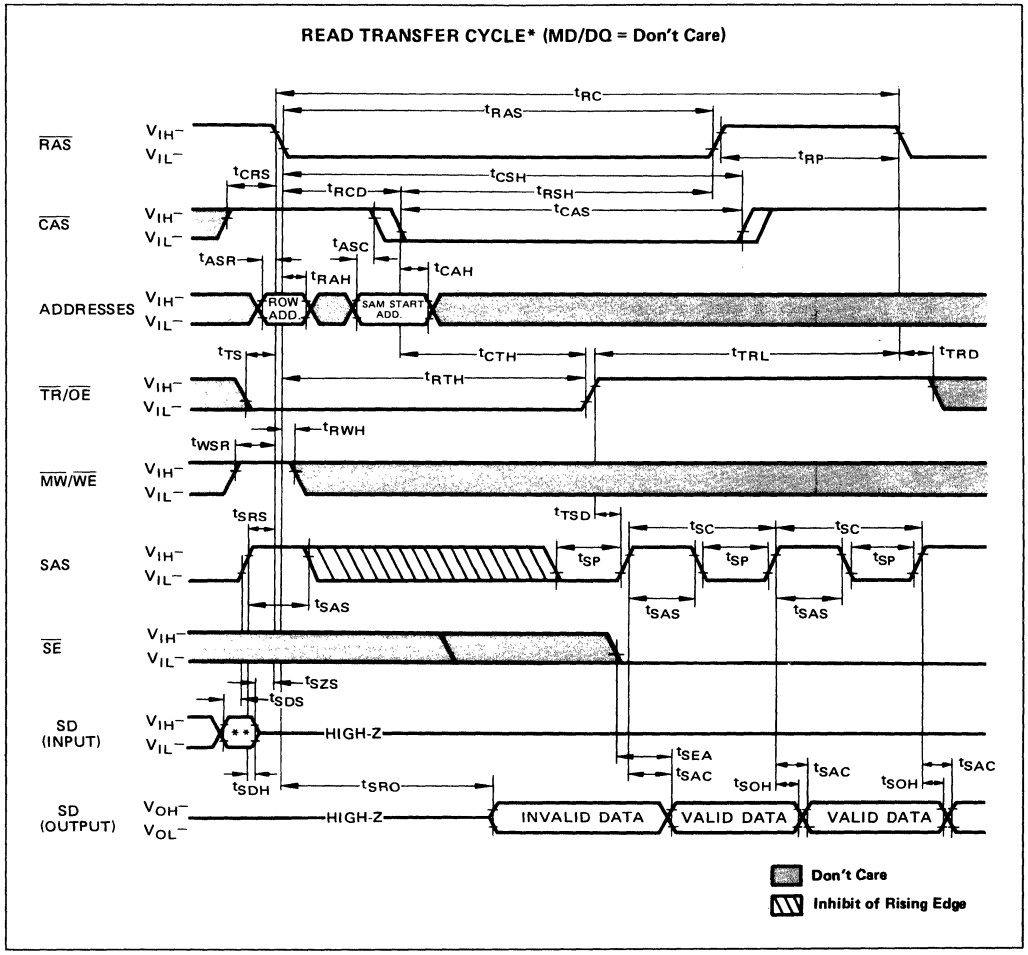
3

READ TRANSFER CYCLE* (MD/DQ = Don't Care)



*: In the case that the previous transfer is read transfer.
**: If $\overline{SE}$ is low, the valid data will appear within t_{SAC} or t_{SEA}.

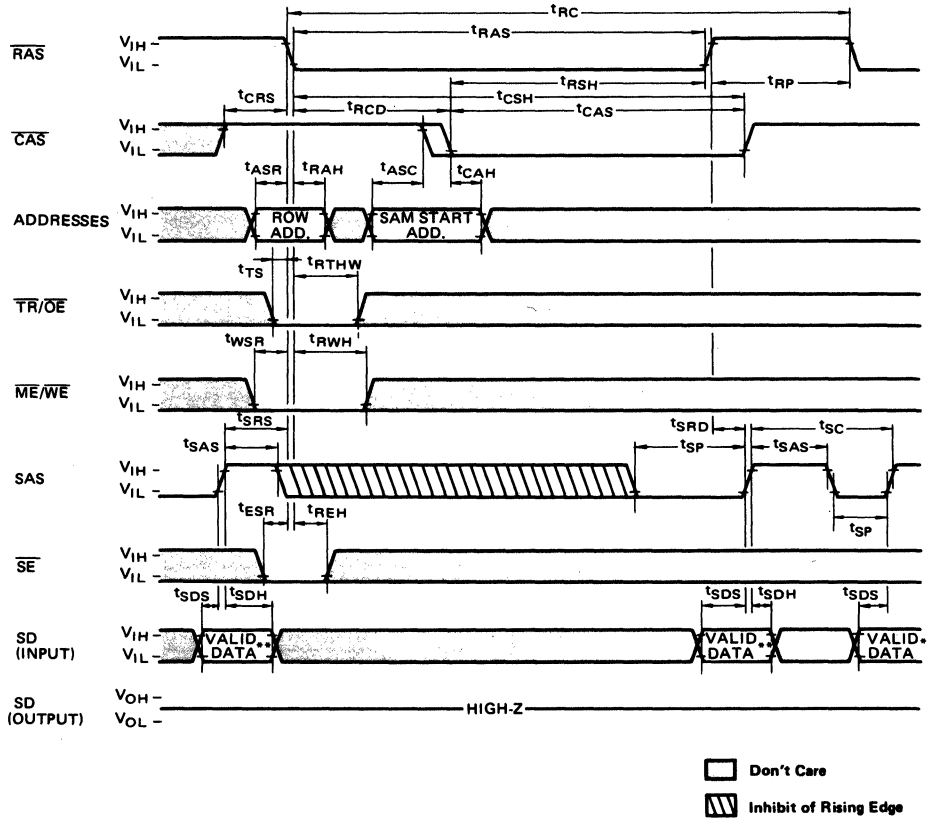


*; In the case that the previous transfer is write transfer.

**; If $\overline{SE}$ is low and the previous cycle is serial write cycle, this should be valid data input.

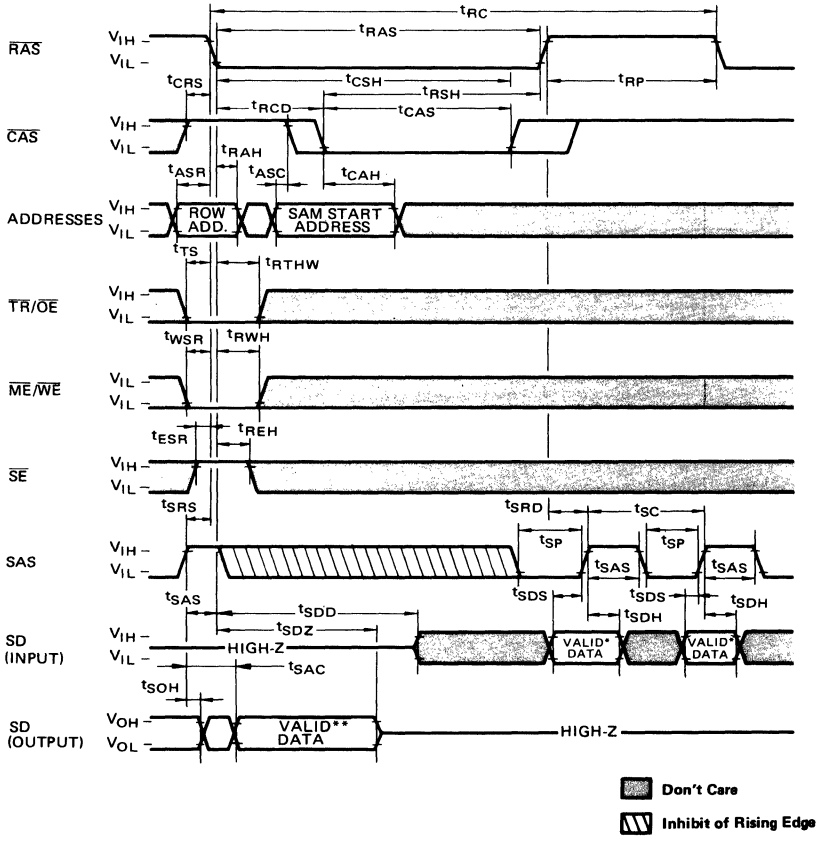
3

WRITE TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is high these data are not written into the SAM.

PSEUDO WRITE TRANSFER CYCLE (MD/ DQ = Don't Care)

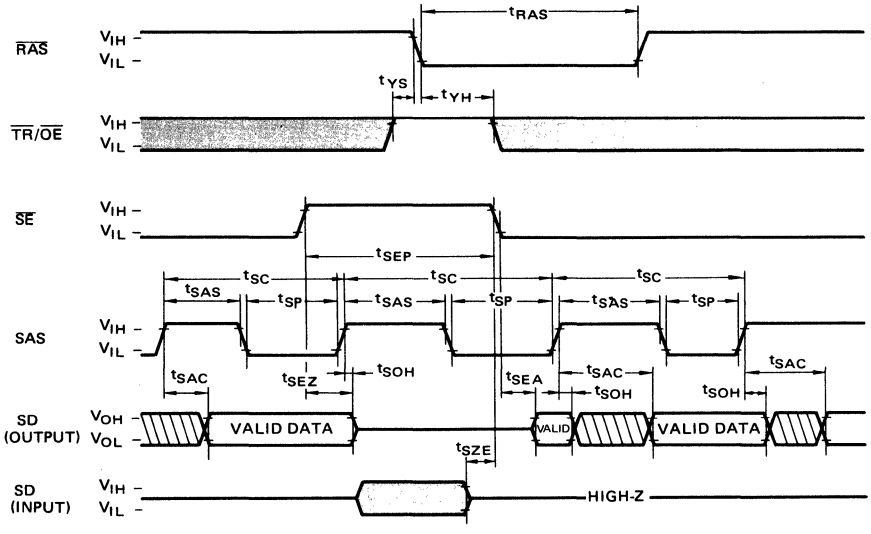


*: If $\overline{SE}$ is high, these data are not written into SAM.

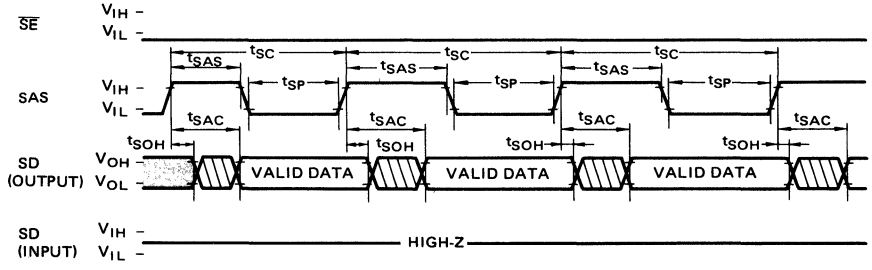
**: If $\overline{SE}$ is high, SD (SD0 to SD3) are in High-Z state after t_{SEZ}.
If $\overline{SE}$ becomes low, the valid data will appear meeting t_{SAC} and t_{SEA}.

3

SERIAL READ CYCLE

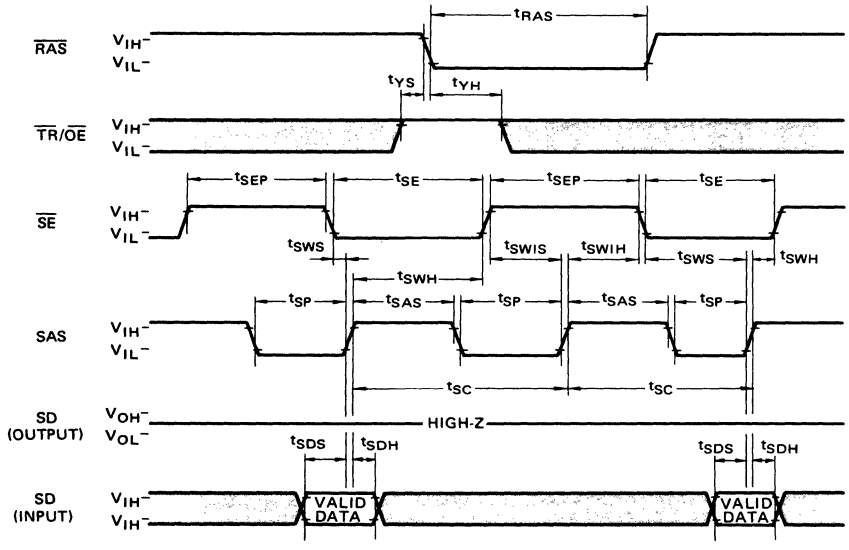


In the case of $\overline{SE}$="L" while the operation;

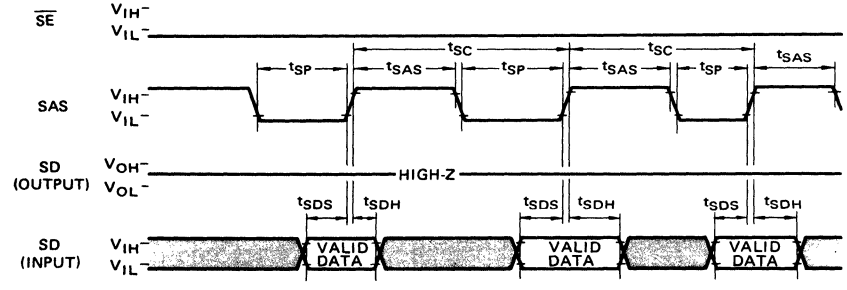


Invalid Data Don't Care

SERIAL WRITE CYCLE



In the case of $\overline{SE}$="L" while the operation;



Don't Care

Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

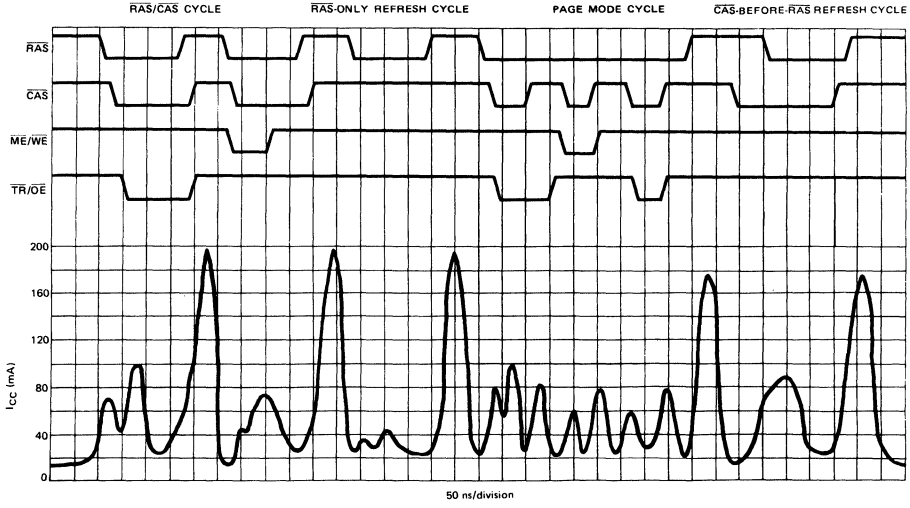
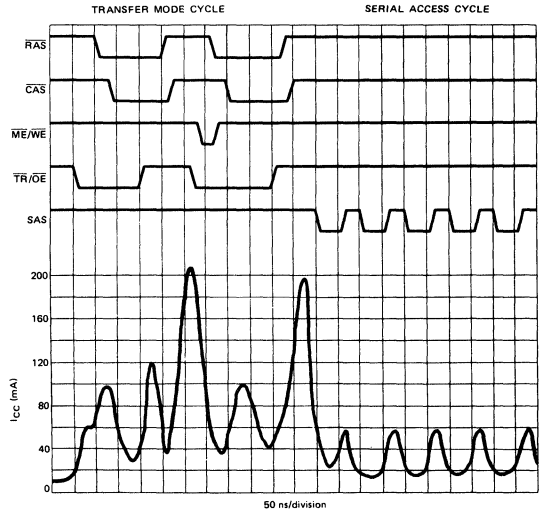


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C) (cont'd)



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

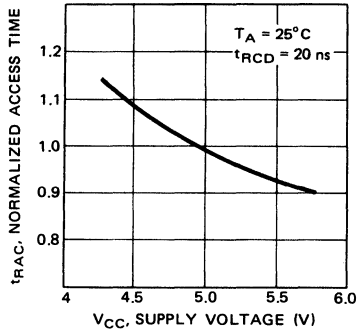


Fig. 7 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

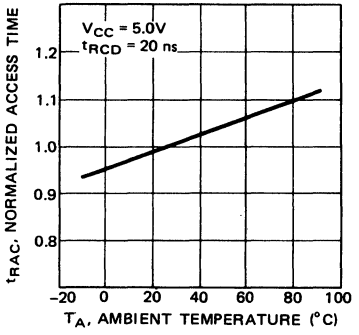


Fig. 8 – OPERATING CURRENT vs CYCLE RATE

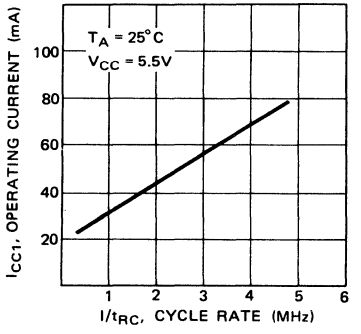


Fig. 9 – OPERATING CURRENT vs SUPPLY VOLTAGE

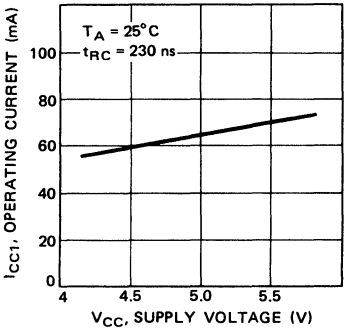


Fig. 10 – OPERATING CURRENT vs AMBIENT TEMPERATURE

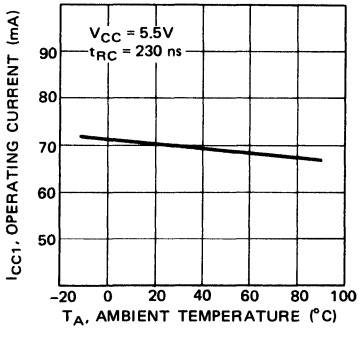
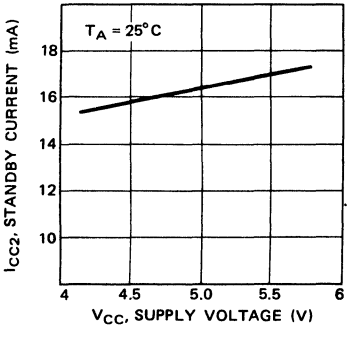


Fig. 11 – STANDBY SURRENT vs SUPPLY VOLTAGE



3

Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

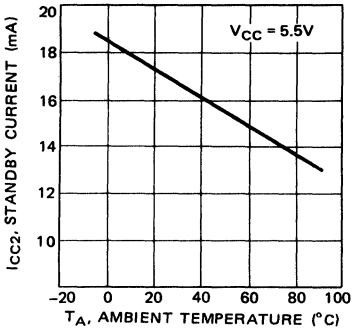
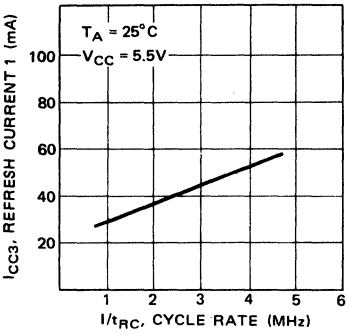


Fig. 13 – REFRESH CURRENT 1 vs CYCLE RATE



3

Fig. 14 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

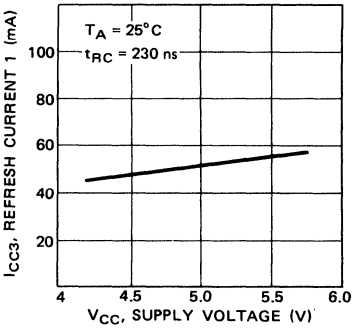


Fig. 15 – PAGE MODE CURRENT vs CYCLE RATE

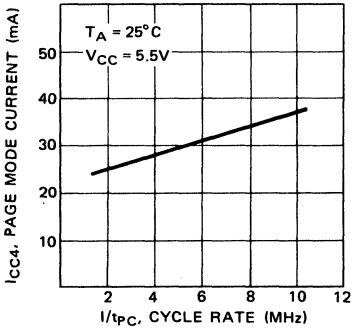


Fig. 16 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

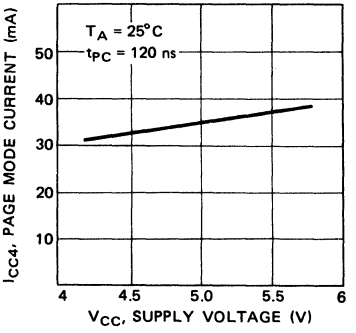


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

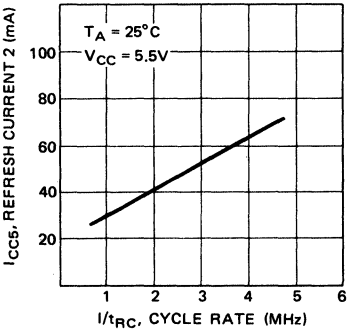


Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

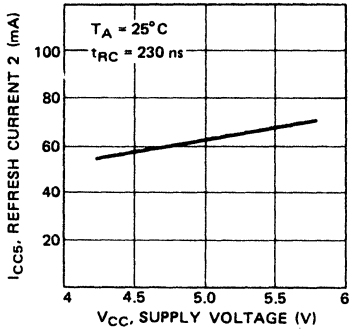
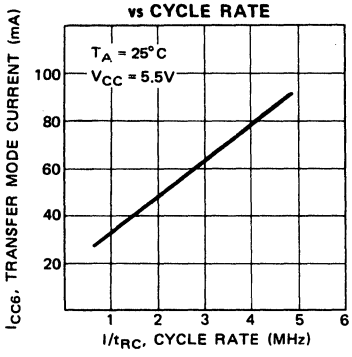


Fig. 19 – TRANSFER MODE CURRENT vs CYCLE RATE



3

Fig. 20 – TRANSFER MODE CURRENT vs SUPPLY VOLTAGE

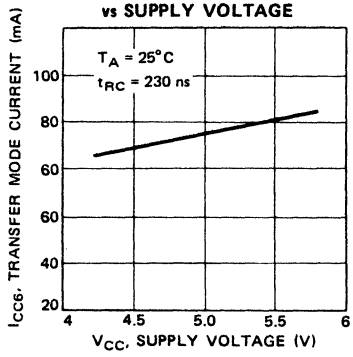


Fig. 21 – RAM STANDBY/SAM ACTIVE CURRENT vs CYCLE RATE

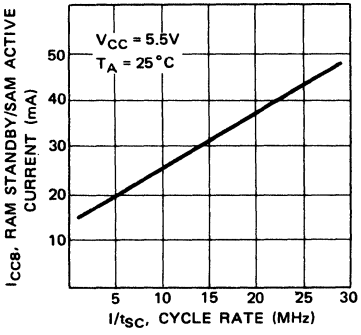


Fig. 22 – RAM STANDBY/SAM ACTIVE CURRENT vs SUPPLY VOLTAGE

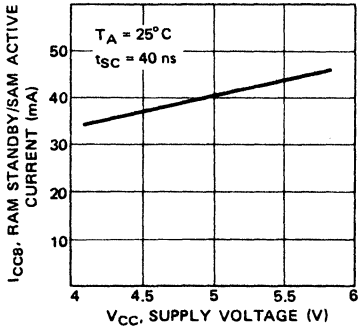


Fig. 23 – RAM STANDBY/SAM ACTIVE CURRENT vs AMBIENT TEMPERATURE

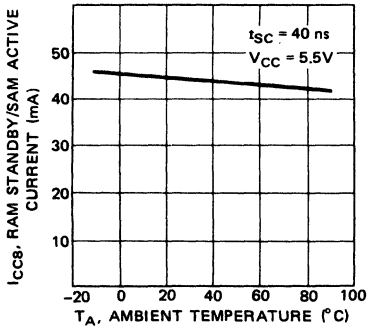


Fig. 24 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

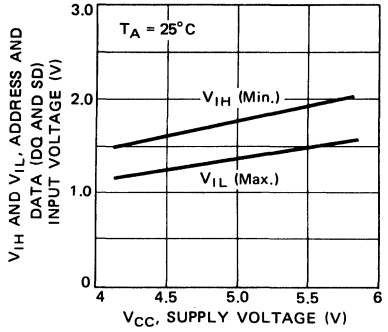


Fig. 25 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

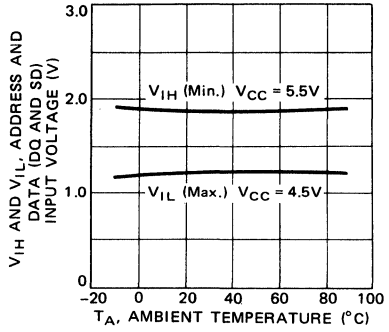


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Fig. 26 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs SUPPLY VOLTAGE

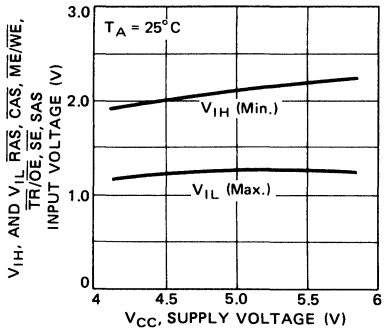


Fig. 27 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs AMBIENT TEMPERATURE

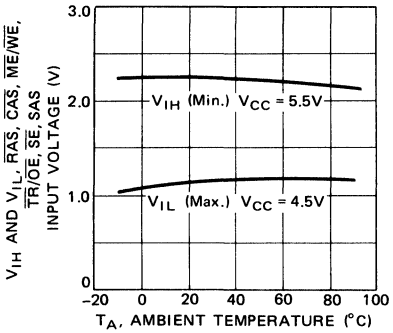


Fig. 28 – ACCESS TIME (RAM) vs LOAD CAPACITANCE

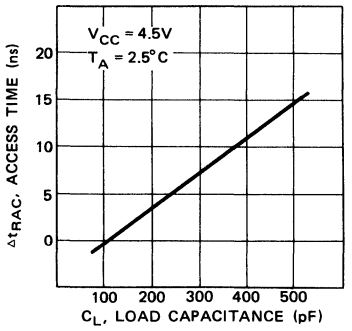


Fig. 29 – ACCESS TIME (SAM) vs LOAD CAPACITANCE

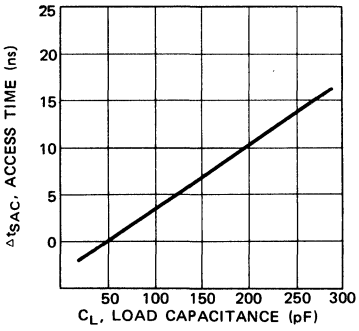


Fig. 30 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

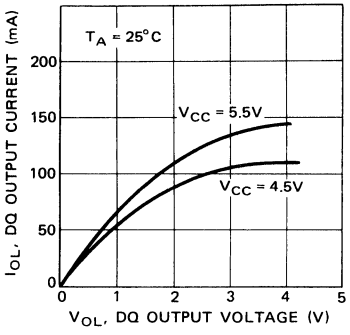


Fig. 31 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

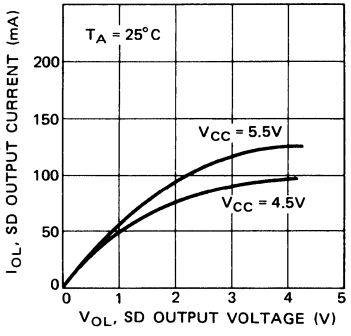


Fig. 32 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

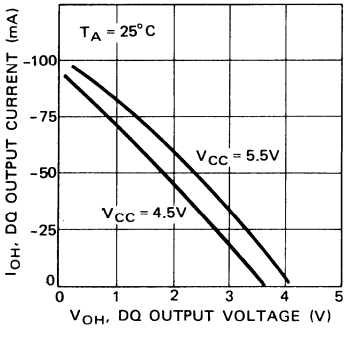


Fig. 33 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

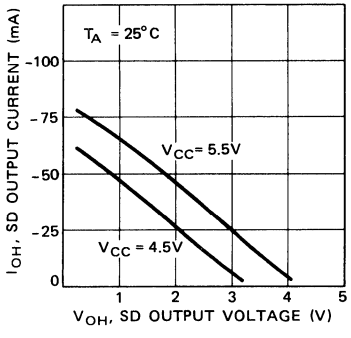
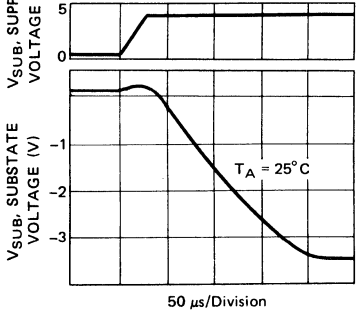


Fig. 34 – SUBSTRATE VOLTAGE DURING POWER UP

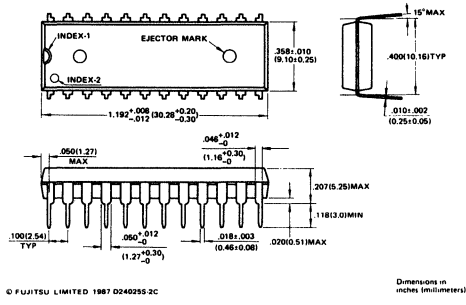


3

PACKAGE DIMENSIONS

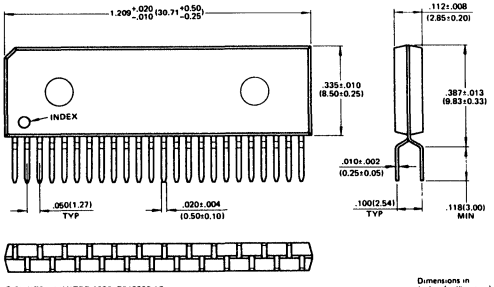
PLASTIC DIP (Suffix: -P) PLASTIC ZIP (Suffix: -PSZ)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M04)



Dimensions in inches (millimeters)

24-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-24P-M02)



Dimensions in inches (millimeters)

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January 1990
Edition 2.0

FUJITSU

DATA SHEET

MB81461B-12/-15

262,144-BIT DUAL PORT DYNAMIC RANDOM ACCESS MEMORY

262,144 Bit Dual Port DRAM

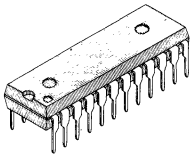
The Fujitsu MB81461B is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits dynamic RAM port and 256 words by 4 bits serial access memory (SAM) port.

The DRAM port is identical to the Fujitsu MB81464 with four bits of parallel random access I/O while the SAM port is designed as four 256-bit registers, each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

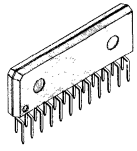
The MB81461B offers complementary asynchronous access of both the DRAM and SAM ports, except when data is transferred between them internally. The design is optimized for high speed and performance making the MB81461B the most efficient solution for implementing the frame buffer of a bit-mapped video display system. Multiplexed row and column address inputs permit the MB81461B to be housed in a 400-mil wide 24-pin DIP or ZIP package. Pinouts conform to the JEDEC-approved pinouts.

The MB81461B is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process technology. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimum chip size. All inputs and outputs are TTL compatible. Some transfer cycle timing specifications are different from MB81461.

- Dual Port Organization
  64 K x 4 Dynamic RAM port (DRAM)
  256 x 4 Serial Access Memory port (SAM)
- 24-pin DIP and ZIP packages
- Silicon-gate, Triple Poly NMOS, single transistor cell
- DRAM Port
  Access Time (t_{RAC})
  120 ns max. (MB 81461B-12)
  150 ns max. (MB 81461B-15)
  Cycle Time (t_{SAC})
  230 ns max. (MB 81461B-12)
  260 ns max. (MB 81461B-15)
- SAM Port
  Access Time (t_{SAC})
  40 ns max. (MB 81461B-12)
  60 ns max. (MB 81461B-15)
  Cycle Time (t_{SC})
  40 ns max. (MB 81461B-12)
  60 ns max. (MB 81461B-15)
- Single +5 V Supply, ±10% tolerance
- Real Time, Read Transfer capability
- Page Mode capability
- Power Dissipation
  DRAM; Act/SAM; Stby
  523 mW max. (MB 81461B-12)
  468 mW max. (MB 81461B-15)
  DRAM; Stby/SAM; Act
  275 mW max. (MB 81461B-12)
  220 mW max. (MB 81461B-15)
  DRAM; Stby/SAM; Stby
  110 mW max.
- Bi-directional data transfer between DRAM and SAM
- Fast serial access asynchronous to DRAM except transfer operation
- Bit Masked Write Mode capabiltiy
- 256 refresh cycles every 4 ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, Hidden Refresh capability
- Delayed write and Read-Modify-Write capability
- Standard 24-Pin Plastic Packages:
  DIP (MB81461B-XXP)
  ZIP (MB81461B-XXPSZ)

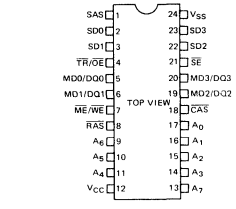


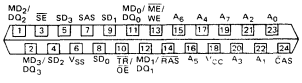
PLASTIC PACKAGE
DIP-24P-M04



PLASTIC PACKAGE
ZIP-24P-M02

PIN ASSIGNMENT





BOTTOM VIEW

Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	—	50	mA

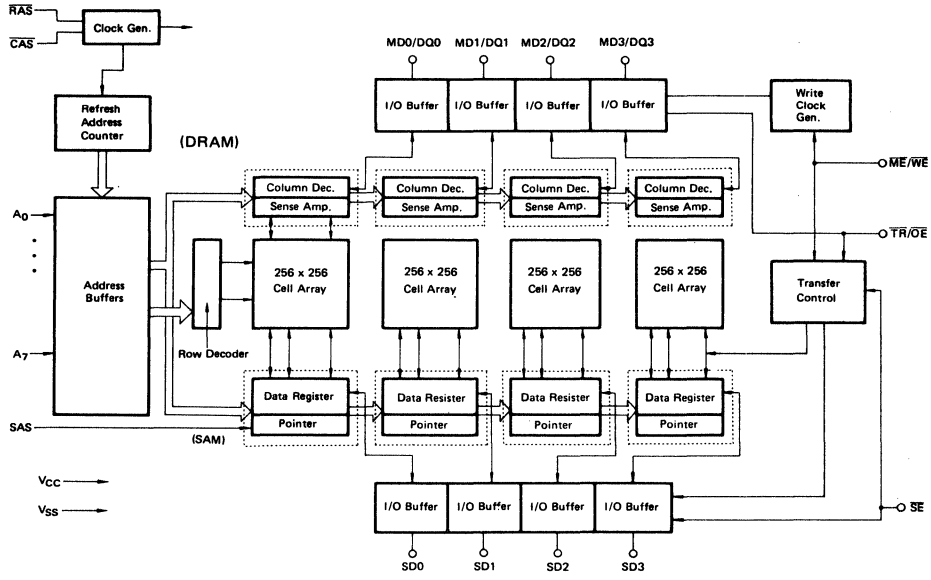
Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – BLOCK DIAGRAM OF MB 81461B and PIN DESCRIPTION

Block Diagram



Pin Description

Pin Number		Symbol	Parameter	Mode
DIP	ZIP			
1	7	SAS	Serial Access Memory Strobe	Input
2,3,22,23	8,9,4,5	SD0 to SD3	Serial Data I/O	I/O
4	10	$\overline{TR}/\overline{OE}$	Transfer Enable/ Output Enable	Input
5,6,19,20	11,12,1,2	MD0/DQ0 to MD3/DQ3	Mask Data/Data I/O	I/O
7	13	$\overline{ME}/\overline{WE}$	Mask Mode Enable/Write Enable	Input
8	14	$\overline{RAS}$	Row Address Strobe	Input
17, 16, 15 14, 11, 10 9, 13	23,22,21, 20,17,16, 15,19	A_0 to A_7	Address Input	Input
12	18	V_{CC}	Supply Voltage +5 V	Power Supply
18	24	$\overline{CAS}$	Column Address Strobe	Input
21	3	$\overline{SE}$	Serial port Enable	Input
24	6	V_{SS}	Ground	Power Supply

DESCRIPTION

DRAM OPERATION

$\overline{RAS}$;

This pin is used to strobe eight row-address inputs from A0 to A7 pins and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by $\overline{TR}/\overline{OE}$ and bit mask write cycle or not (by $\overline{ME}/\overline{WE}$ and MD0/DQ0 to MD3/DQ3). Since $\overline{RAS}$ = "L" is the active condition of circuit, to maintain $\overline{RAS}$ = "H" (standby condition) is effective to save power dissipation.

$\overline{CAS}$;

This pin is used to strobe eight column address inputs at the falling edge. $\overline{CAS}$ pin has the function to enable and disable the output at "L" and "H" respectively during the read operation.

Another function of $\overline{CAS}$ is to select "early write" mode conditioned by $\overline{ME}/\overline{WE}$ = "L".

$\overline{ME}/\overline{WE}$;

This pin is used to select read or write cycle. $\overline{ME}/\overline{WE}$ = "L" select write mode and $\overline{ME}/\overline{WE}$ = "H" select read mode. This pin is also used to enable bit mask write cycle. If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write is enabled.

$\overline{TR}/\overline{OE}$;

This pin is used to select Transfer operation or not at the falling edge of $\overline{RAS}$, $\overline{TR}/\overline{OE}$ = "H" enables DRAM operation and $\overline{TR}/\overline{OE}$ = "L" enables Transfer operation between DRAM and SAM. After the falling of $\overline{RAS}$ with t_{YH}, this pin is used for output enable.

The $\overline{TR}/\overline{OE}$ controls the impedance of the output buffers. $\overline{TR}/\overline{OE}$ = "H" forces the output buffers at high impedance state. $\overline{TR}/\overline{OE}$ = "L" leads the output buffers at low impedance state. But in early write cycle, the output buffers are high impedance state even if $\overline{TR}/\overline{OE}$ is low.

A0 to A7;

These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB81461B The eight row address inputs are strobed by $\overline{RAS}$ and followed eight column address inputs are strobed by $\overline{CAS}$. These are used to select the start address of serial access memory also.

MD0/DQ0 to MD3/DQ3

These are common I/O pins of DRAM port. I/O mode is as specified for each function mode in the truth table.

Data Outputs:

The output buffers have three-state capability "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read" or "read-modify-write" mode. During a refresh cycle, either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ mode is selected, output buffers are set in "High-Z" state.

Data inputs:

These are used as data input pins when a data write mode such as "Early-Write", "Delayed Write" or "Read-modify-Write" is selected. In any of the above cases, these pins are set at "High-Z" state to enable data-in without any bus conflict.

In any operation mode, read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$ and/or $\overline{TR}/\overline{OE}$. When "Bit mask write" mode is set, these pins are used as a control signal for write inhibit with MDi/DQi = "L" on the selected bit i.

Page Mode;

The page mode operation is to strobe the column address by $\overline{CAS}$ while $\overline{RAS}$ is maintained at "L" through all the successive memory operations if the row address doesn't change. This mode can save power dissipation and get the faster access time due to the elimination of $\overline{RAS}$ falling edge function.

Refresh;

Refresh of the DRAM cells is performed for every 256 rows per every 4 milliseconds.

The MB81461B offers the following three types of refresh.

1) $\overline{RAS}$-Only refresh; The $\overline{RAS}$-Only refresh is performed with $\overline{CAS}$="H" condition. Strobing every 256 row addresses with $\overline{RAS}$ will complete all bits of memory cell to be refreshed while all outputs are invalid due to "High-Z" state. Further $\overline{RAS}$-only refresh saves the power dissipation substantially.
2) $\overline{CAS}$-before-$\overline{RAS}$ refresh; The $\overline{CAS}$-before-$\overline{RAS}$ refresh offers an alternate refresh method. If $\overline{CAS}$ is set low for the specified period (t_{FCS}) before the falling edge of $\overline{RAS}$, refresh control clock generator and refresh address counter are enabled, and an refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3) Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending $\overline{CAS}$ low. The hidden refresh is equivalent to $\overline{CAS}$-before-$\overline{RAS}$ refresh because $\overline{CAS}$ stays low when $\overline{RAS}$ goes to low in the next cycle.

Bit Mask Write;

This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$ during write mode (early, delayed write or read-modify-write cycle). The bits to be masked (or inhibited to write) is determined by MD/DQ state at the falling edge of $\overline{RAS}$, for example, if MD0/DQ0 and $\overline{ME}/\overline{WE}$ are both low at the falling edge of $\overline{RAS}$, the data on MD0/DQ0 pin is not written into the cell during the cycle. Refer to the Fig. 2.

EXAMPLE OF BIT MASK WRITE OPERATION

Falling edge of $\overline{RAS}$						Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	Write enable
	L	H	L	H	L	Write enable for DQ0 and DQ2 Write disable for DQ1 and DQ3

X: Don't Care

FUNCTIONAL TRUTH TABLE FOR DRAM OPERATION

$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$	$\overline{TR}/\overline{OE}$	ADDRESSES	MD0/DQ0 to MD3/DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L*	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H→X→H	Valid	Valid Data In	Delayed Write
L	L	H→L	H→L→H	Valid	Valid Data Out → Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	$\overline{RAS}$-Only Refresh
H→L	L	X	H→X	X	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh

*: If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write mode is enabled.

TRANSFER OPERATION:

The transfer operation is featured in the MB 81461B. This mode is used to transfer simultaneously 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of $\overline{ME}/\overline{WE}$ at the falling edge of $\overline{RAS}$. $\overline{ME}/\overline{WE}$="H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and $\overline{ME}/\overline{WE}$="L" defines the transfer from SAM to DRAM (Write Transfer Cycle).

I/O mode of SD0 to SD3 determined while the transfer operation is set ($\overline{TR}/\overline{OE}$="L") conjunctioned with $\overline{ME}/\overline{WE}$ state.

After Read Transfer Cycle, please apply two or more SAS Clock.

$\overline{TR}/\overline{OE}$;

This pin is used to enable transfer operation at the falling edge of $\overline{RAS}$.

$\overline{ME}/\overline{WE}$;

This pin is used to select the direction of transfer at the falling edge of $\overline{RAS}$.

A0 to A7;

These pins are used to select the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by $\overline{RAS}$ and the start address is strobed by $\overline{CAS}$.

Pseudo Write Transfer:

To start serial write cycle, the SD pins must be set in input mode. To do this, write transfer cycle should be executed. The pseudo write transfer cycle is to change the SD pins into input mode without data transfer from SAM to DRAM. Refer to Fig. 3.

Refresh during transfer cycle;

DRAM and SAM are refreshed during transfer cycle as shown below.

1) Read transfer cycle:
   During read transfer cycle, the selected row address of DRAM to be transfered to SAM is refreshed. SAM data are kept by applying 256 SAS clocks within 4 ms after the read transfer cycle.
2) Write transfer cycle:
   During write transfer cycle, the new data are written from SAM to DRAM and this row address should be refreshed within 4 ms.
   But SAM data are not refreshed during write transfer cycle. Therefore, the SAM refresh (applying 256 SAS clocks within 4 ms) must be executed. Especially, when the write transfer cycle is executed continuously, 256 SAS clock should be applied within 4 ms.

SERIAL ACCESS OPERATION:

The MB 81461B has 256 words by 4 bits Serial Acess Memory (SAM) corresponding to 64K words by 4 bits DRAM and the fast serial read/write access is achieved by SAM architecture. Read or write cycle is determined when the last read or write transfer operation is executed. If the last transfer operation was read transfer, the serial read cycle is performed until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write or pseudo write transfer, the serial write cycle is performed. In the serial write operation, 256 words by 4 bits data stored in the SAM can be transfered to DRAM under $\overline{SE}$="L" condition, and $\overline{SE}$="H" condition disables data transfer from SAM to DRAM. The serial access operation can be done asynchronously from DRAM port.

SAS;

This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data of the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, out-

put data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returnes to #0 (Least Significant Address).

$\overline{SE}$;
This pin is used to enable serial access operation by bit to bit. $\overline{SE}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{SE}$ = "H" leads SD pins to "High-Z" state. $\overline{SE}$ = "L" leads SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by last occured transfer operation, if last transfer operation was read transfer mode, they are output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is constructed by dynamic circuitry, the refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4ms in either output or input mode. $\overline{SE}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is applicable to obtain valid data continuously when row address is changed without any timing loss from the last bit of previous row to the first bit of new row. Data transfer from DRAM to SAM is triggered by rising edge of $\overline{TR}/\overline{OE}$ after the preparation of internal circuit for this operation, while SAM port can continue read operation asynchronously from the above mentioned internal move. Once $\overline{TR}/\overline{OE}$ returns to "H" with the restricted timing specification t_{TSL} and t_{TSD} refered to SAS clock, SD pins can get the valid output data continuously as shown in Fig. 4. The key issue to achieve this feature is to apply SAS clock continuously with the timing consideration to the rising edge of $\overline{TR}/\overline{OE}$.

3

FUNCTIONAL TRUTH TABLE FOR SERIAL ACCESS (Asynchronous from DRAM port)

Falling edge of $\overline{RAS}$		SAS	$\overline{SE}$	SD0 to SD3	Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$				
H	X	Clock	L	Input/Output*	Sequential access enable
		Clock	H	Input/Output*	Sequential access disable

*: The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.

X; Don't Care

Fig. 2 – EXAMPLE OF BIT MASK WRITE OPERATION

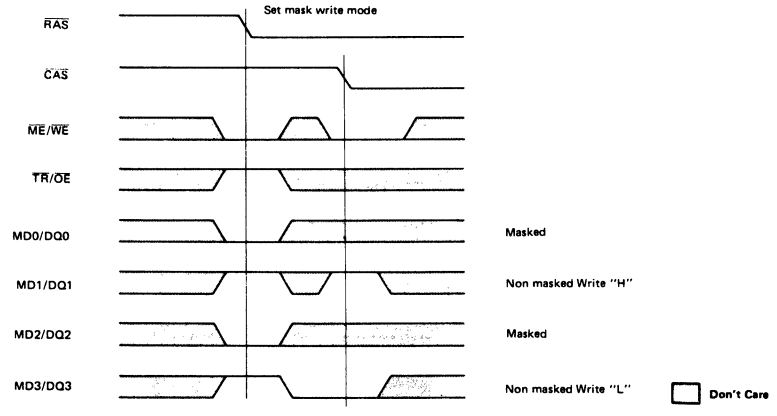
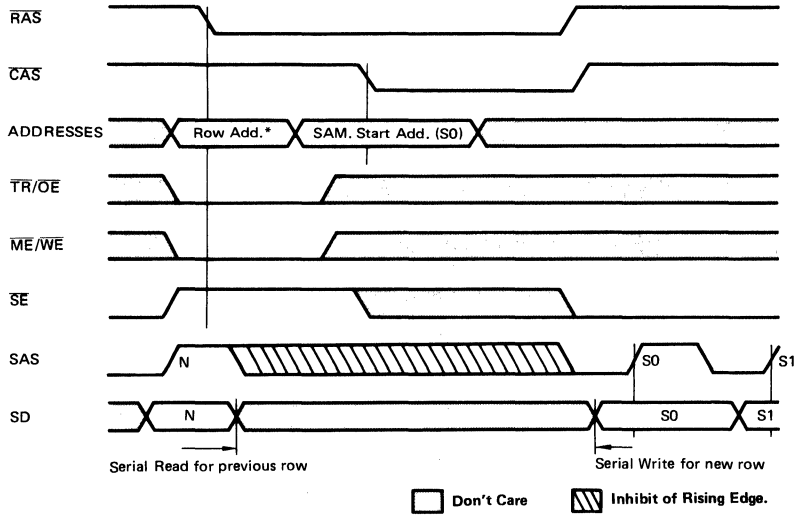
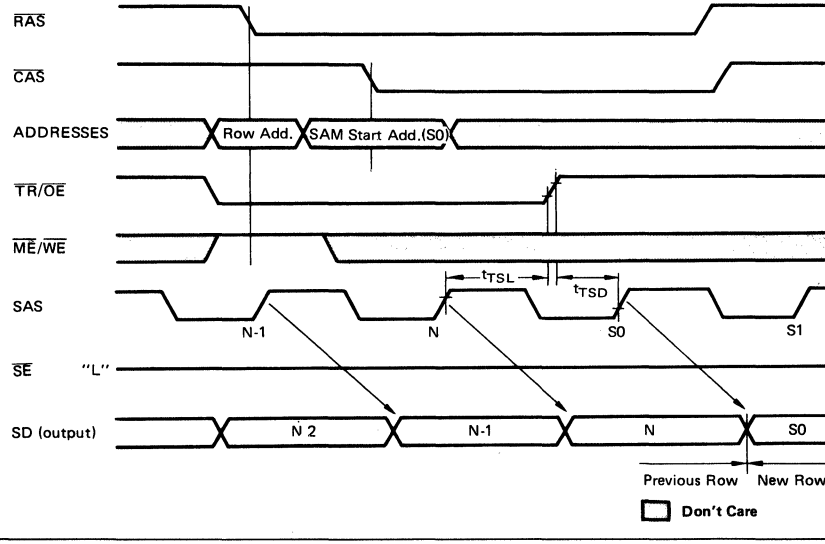


Fig. 3 – EXAMPLE OF PSEUDO WRITE TRANSFER CYCLE



*The DRAM data of this row address are refreshed during pseudo write transfer cycle.

Fig. 4 – EXAMPLE OF REAL TIME READ TRNASFER OPERATION



RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}	-2.0		0.8	V	

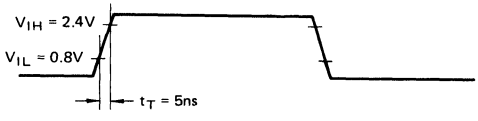
CAPACITANCE (T_A=25°C)

Paramter	Symbol	Typ	Max		Unit
			DIP	ZIP	
Input Capacitance (A0 to A7)	C_{IN1}		7	8	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{SE}$, $\overline{TR}$/$\overline{OE}$)	C_{IN2}		10	12	pF
Input Capacitance (SAS)	C_{IN3}		7	7	pF
Input/Output Capacitance (MD0/DQ0 to MD3/DQ3)	C_{IO1}		7	8	pF
Input/Output Capacitance (SD0 to SD3)	C_{IO2}		7	8	pF

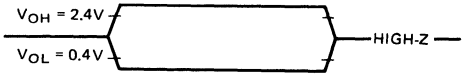
3

AC TEST CONDITIONS

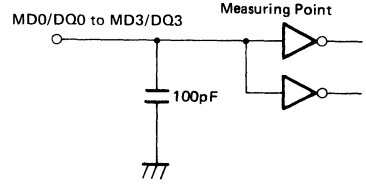
1) Input

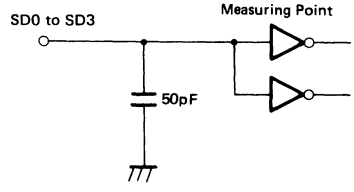


2) Output



3) Output Load





DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
SAM STANDBY $\overline{SE}$ = V_{IH}, SAS = V_{IL}					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC1}		95	mA
	MB 81461B-15			85	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		20	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC3}		77	mA
	MB 81461B-15			70	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min)	MB 81461B-12	I_{CC4}		50	mA
	MB 81461B-15			45	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461B-12	I_{CC5}		77	mA
	MB 81461B-15			70	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC6}		110	mA
	MB 81461B-15			100	
SAM ACTIVE $\overline{SE}$ = V_{IL}, t_{SC} = min					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC7}		130	mA
	MB 81461B-15			110	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MB 81461B-12	I_{CC8}		50	mA
	MB 81461B-15			40	
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC9}		112	mA
	MB 81461B-15			95	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)	MB 81461B-12	I_{CC10}		85	mA
	MB 81461B-15			70	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461B-12	I_{CC11}		112	mA
	MB 81461B-15			95	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC12}		145	mA
	MB 81461B-15			125	

3

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, V_{CC}=5.5V, V_{SS}=0V, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH}=-5mA/-2mA for DQi/SDi) Output low voltage (I_{OL}=4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

3

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1 2 3

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Time between Refresh (RAM/SAM)		t_{REF}		4		4	ms
Random Read/Write Cycle Time		t_{RC}	230		260		ns
Read-Modify-Write Cycle Time		t_{RWC}	305		345		ns
Page Mode Cycle Time		t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	25	0	35	ns
Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	60000	150	60000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60		75		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time (Normal cycle)		t_{CPN}	40		50		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50		60		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$)		t_{CPR}	25		30		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	60000	75	60000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		ns
Write Command Set Up Time		t_{WCS}	-5		-5		ns
Write Command Hold Time		t_{WCH}	30		35		ns
Write Command Pulse Width		t_{WP}	30		35		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from $\overline{TR}/\overline{OE}$	6	t_{OEA}		35		40	ns
$\overline{TR}/\overline{OE}$ to Data In Delay Time		t_{OED}	25		30		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Output Buffer Turn Off Delay from $\overline{TR}/\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{TR}/\overline{OE}$ Hold Time Referenced to $\overline{ME}/\overline{WE}$		t_{OEH}	0		0		ns
$\overline{TR}/\overline{OE}$ to $\overline{RAS}$ inactive Set Up Time		t_{OES}	0		0		ns
Data In to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		ns
Data In to $\overline{TR}/\overline{OE}$ Delay Time	16	t_{DZO}	0		0		ns
Refresh Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCS}	25		30		ns
Refresh Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	20		20		ns
Serial Clock Cycle Time		t_{SC}	40	50000	60	50000	ns
Access Time from SAS	10	t_{SAC}		40		60	ns
Access Time from $\overline{SE}$	10	t_{SEA}		40		50	ns
SAS Precharge Time		t_{SP}	10		20		ns
SAS Pulse Width		t_{SAS}	10		20		ns
$\overline{SE}$ Precharge Time		t_{SEP}	25		45		ns
$\overline{SE}$ Pulse Width		t_{SE}	25		45		ns
Serial Data Out Hold Time after SAS High		t_{SOH}	10		10		ns
Serial Output Buffer Turn Off Delay from $\overline{SE}$		t_{SEZ}	0	25	0	30	ns
Serial Data In Set Up Time	11	t_{SDS}	0		0		ns
Serial Data In Hold Time	11	t_{SDH}	20		25		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{TS}	0		0		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{RTH}	90		110		ns
Write Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time	12	t_{RTHW}	12		15		ns
Transfer Command ($\overline{TR}$) to $\overline{CAS}$ Hold Time		t_{CTH}	30		35		ns
Transfer Command ($\overline{TR}$) to SAS Lead Time		t_{TSL}	5		10		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Lead Time	17	t_{TRRL}	25		35		ns
Transfer Command ($\overline{TR}$) Hold Time from $\overline{RAS}$	17	t_{TRRH}	25		35		ns
First SAS Edge to Transfer Command Delay Time		t_{TSD}	25		35		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Set Up Time		t_{WSR}	0		0		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Hold Time		t_{RWH}	12		15		ns
Mask Data (MD) to $\overline{RAS}$ Set Up Time		t_{MS}	0		0		ns
Mask Data (MD) to $\overline{RAS}$ Hold Time		t_{MH}	35		45		ns
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	12	t_{SDZ}	10	60	10	75	ns
Serial Output Buffer Turn On Delay from $\overline{RAS}$	13	t_{SRO}	0		0		ns
SAS to $\overline{RAS}$ Set Up Time	11	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS Delay Time	12	t_{SRD}	30		45		ns
Serial Data Input to $\overline{SE}$ Delay Time		t_{SZE}	0		0		ns
Serial Data Input Delay from $\overline{RAS}$	12	t_{SDD}	60		75		ns

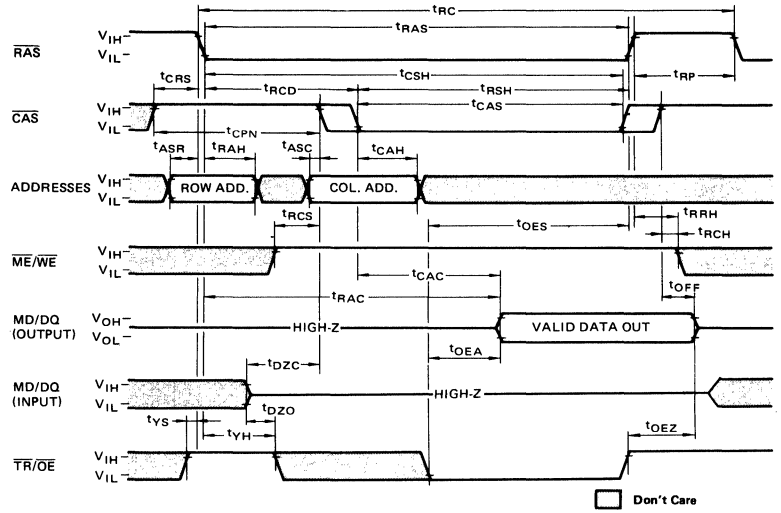
AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Serial Data Input to $\overline{RAS}$ Delay Time	13	t_{SZS}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Set up Time	14	t_{ESR}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	14	t_{REH}	12		15		ns
Serial Write Enable Set up Time	11	t_{SWS}	20		30		ns
Serial Write Enable Hold Time	11	t_{SWH}	80		120		ns
Serial Write Disable Set Up Time	11	t_{SWIS}	20		30		ns
Serial Write Disable Hold Time	11	t_{SWIH}	40		60		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{YS}	0		0		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{YH}	12		15		ns
Time between Transfer	15	t_{REFT}		4		4	ms

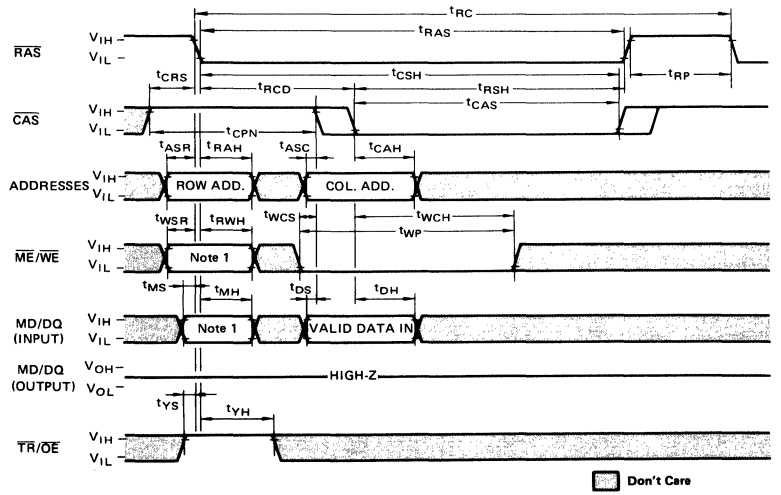
NOTES:

1. An initial pause of 200μs is required after power-up followed by any 8 RAS, 8 transfer, and 8 SAS cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycle are required.
2. AC characteristics assume.
3. V_{IH} (min) and L_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the pecified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Measured with a load equivalent to 2 TTL loads and 50pF.
11. Input mode only
12. Write transfer and pseuso write transfer only.
13. Read transfer only in the case that the previous transfer was write transfer.
14. Pseudo write transfer only.
15. If t_{REFT} is not satisfied, 8 transfer and 8 SAS cycles before proper device operation is needed.
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. This timing specification is different from that of MB 81461.

READ CYCLE

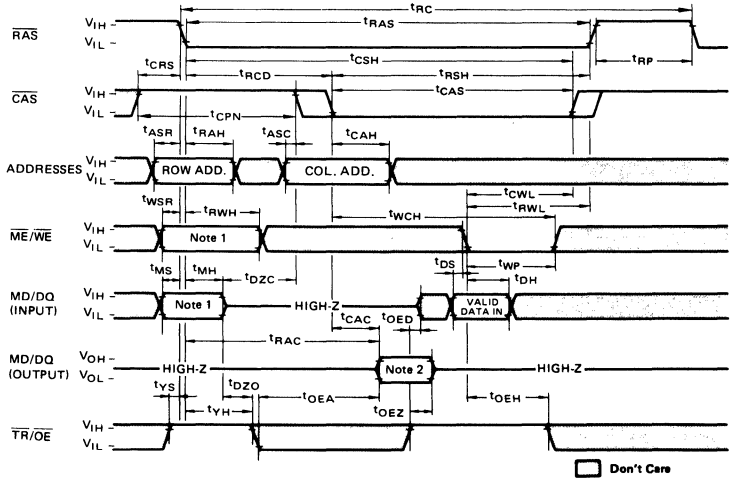


WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

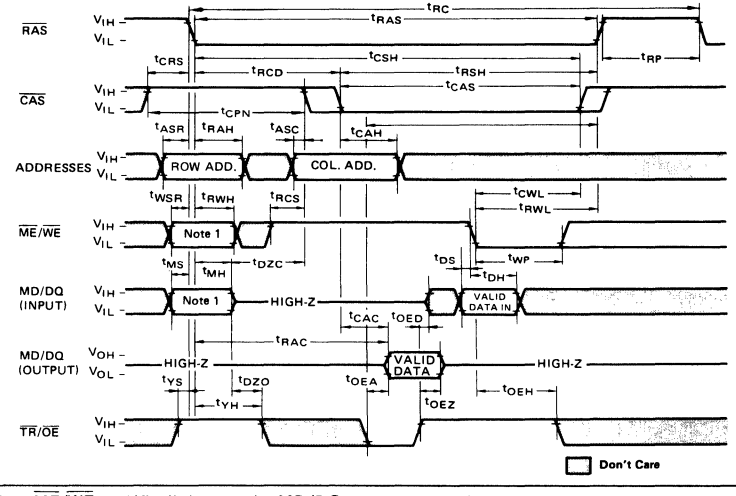
DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

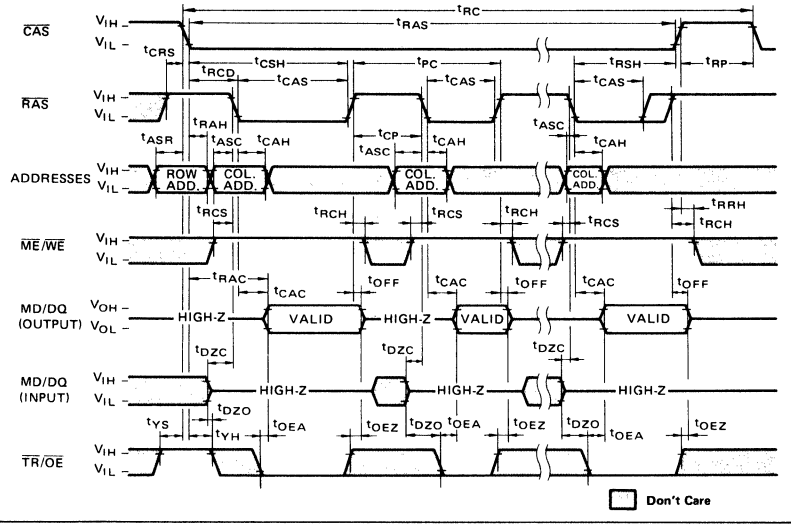
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

READ-MODIFY-WRITE CYCLE

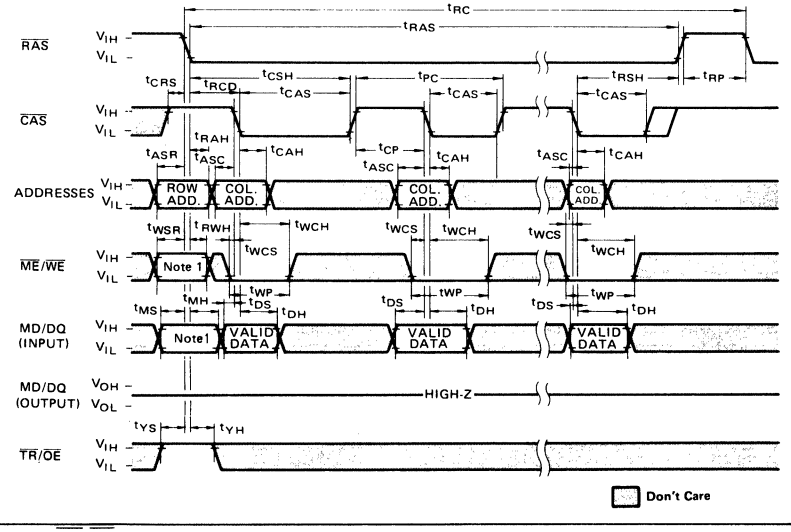


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

PAGE MODE READ CYCLE

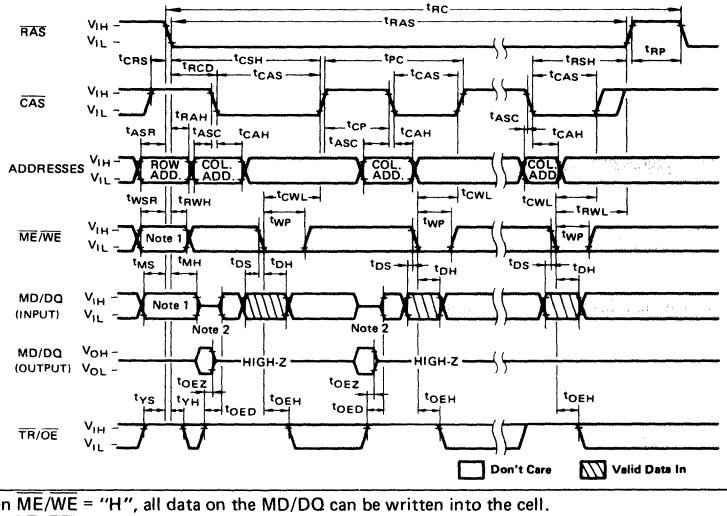


PAGE MODE WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

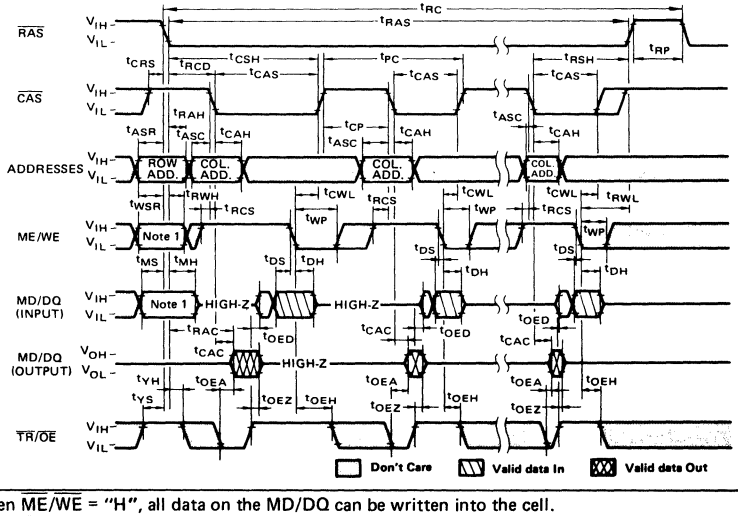
PAGE MODE DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

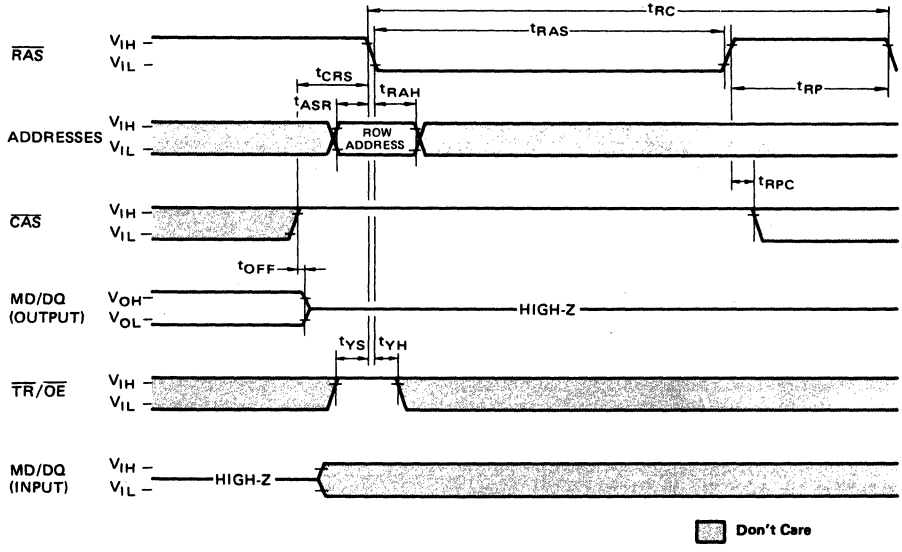
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

PAGE MODE READ-MODIFY-WRITE CYCLE

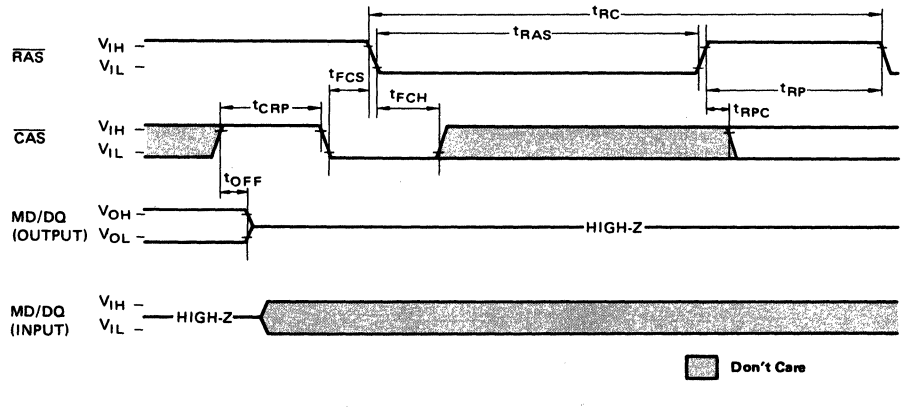


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

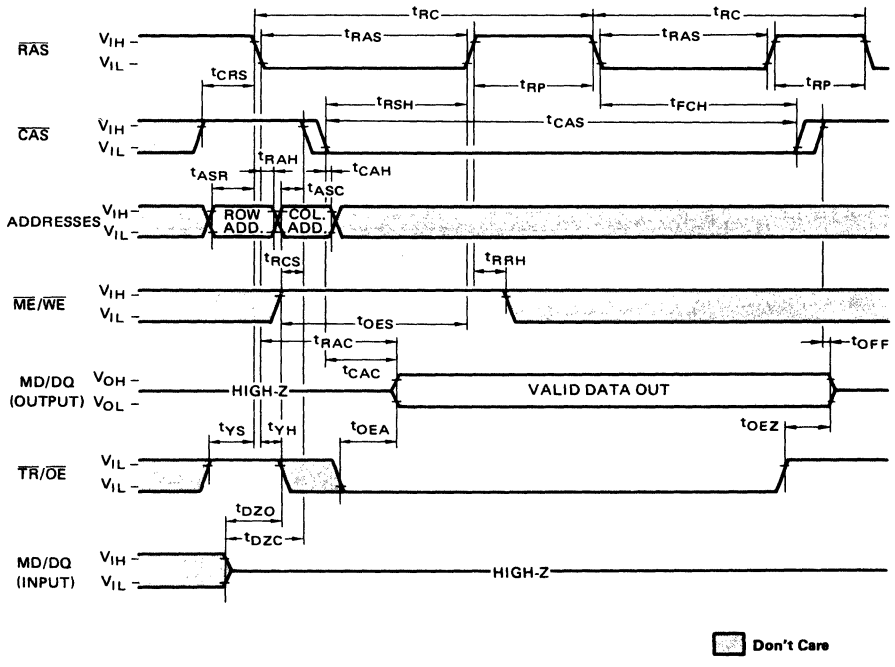
$\overline{RAS}$-ONLY REFRESH CYCLE ($\overline{ME}$/$\overline{WE}$=Don't Care)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (ADDRESS, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$=Don't Care)

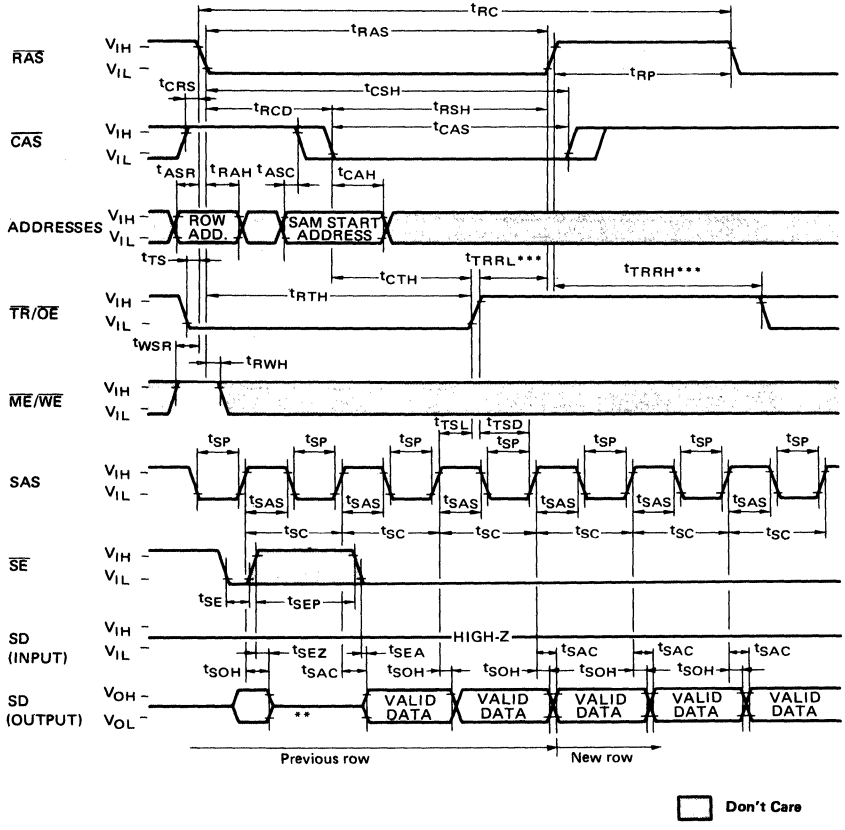


HIDDEN REFRESH CYCLE



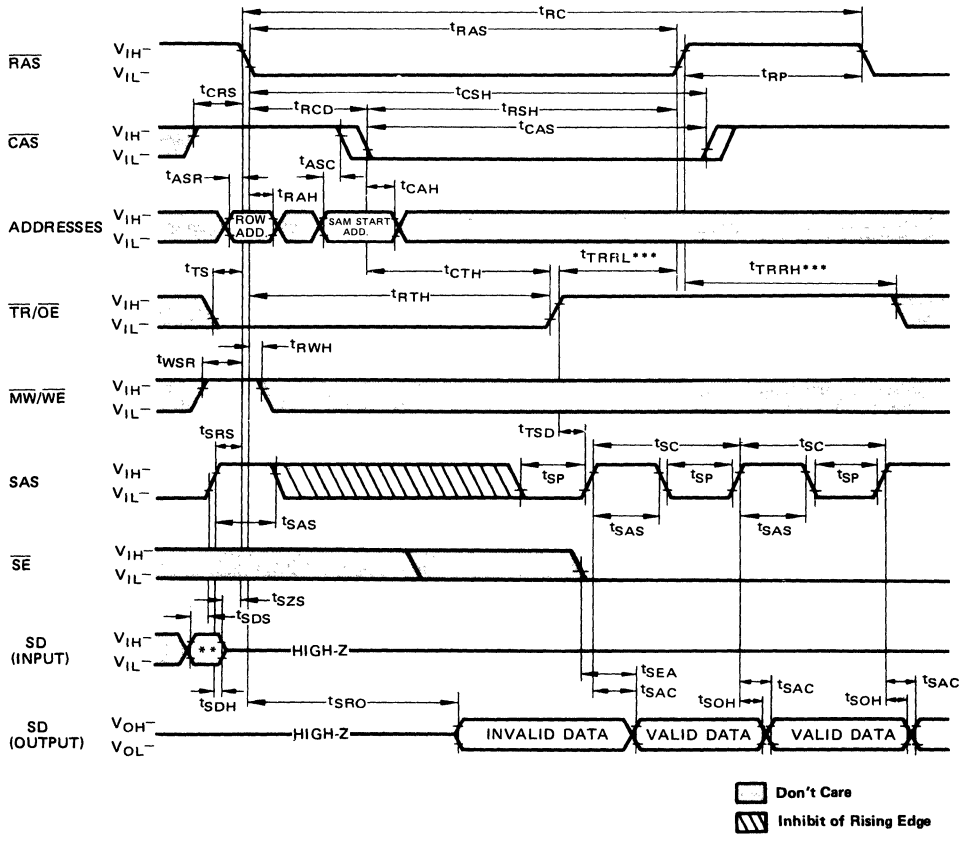
3

READ TRANSFER CYCLE* (MD/DQ = Don't Care)



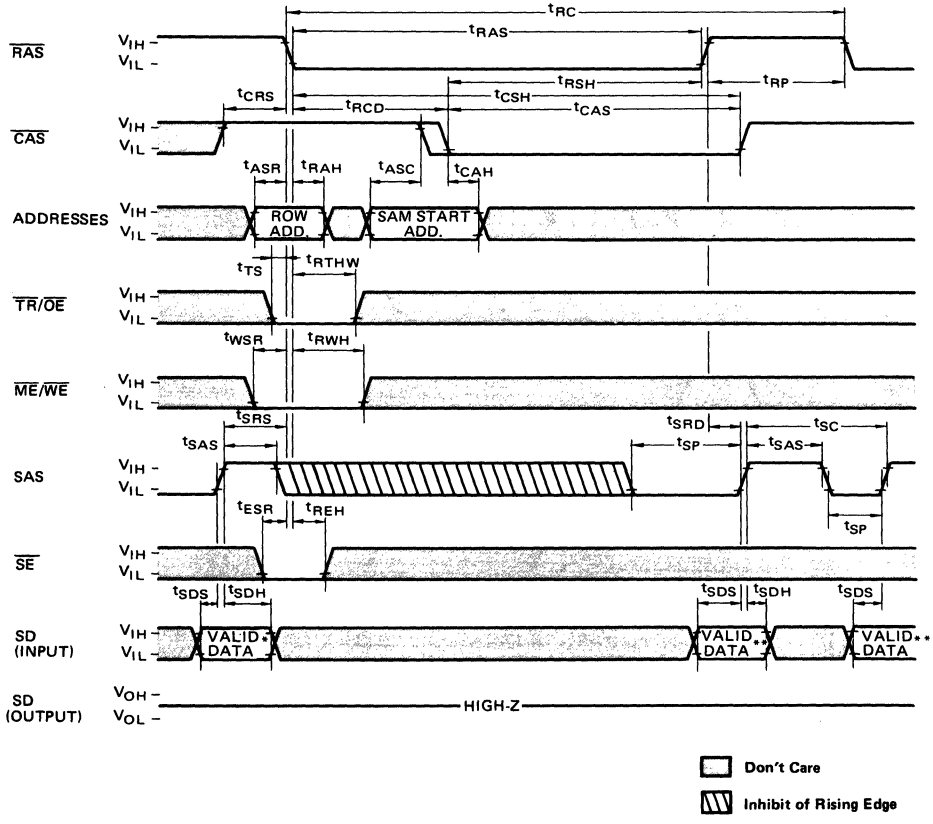
*: In the case that the previous transfer is read transfer.
**: If $\overline{SE}$ is low, the valid data will appear within t_{SAC} or t_{SEA}.
***: These parameters are different from that of MB 81461.

READ TRANSFER CYCLE* (MD/DQ = Don't Care)



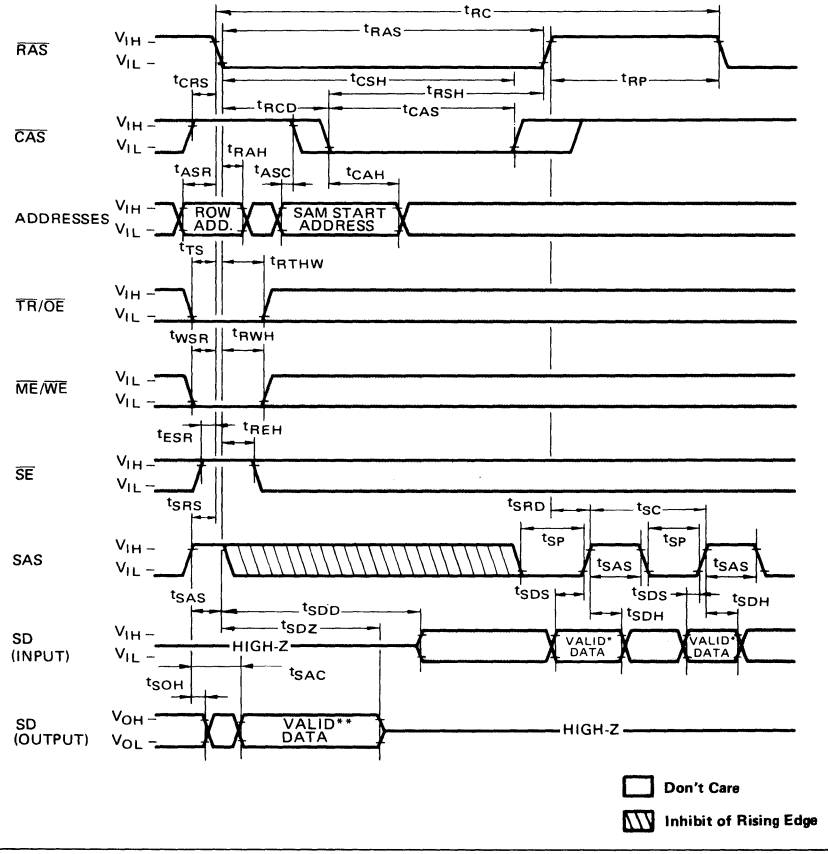
*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is low and the previous cycle is serial write cycle, this should be valid data input.
***; These parameters are different from that of MB 81461.

WRITE TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is high these data are not written into the SAM.

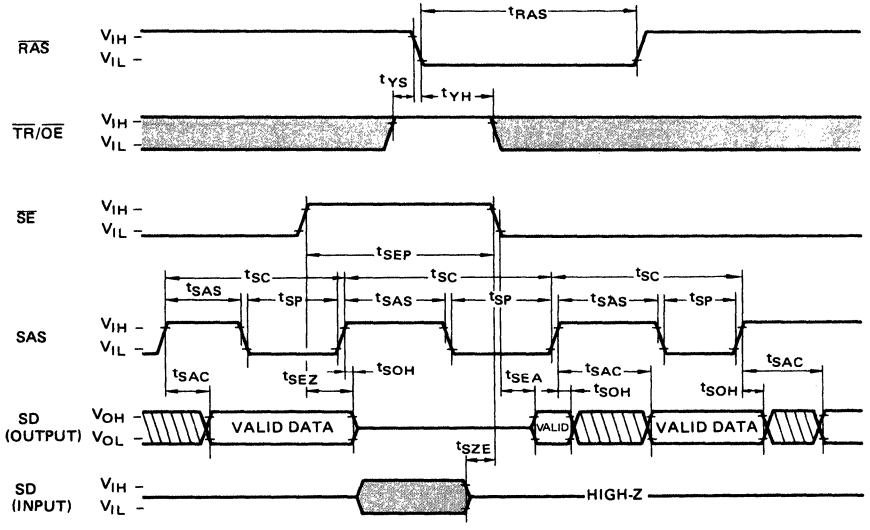
PSEUDO WRITE TRANSFER CYCLE (MD/ DQ = Don't Care)



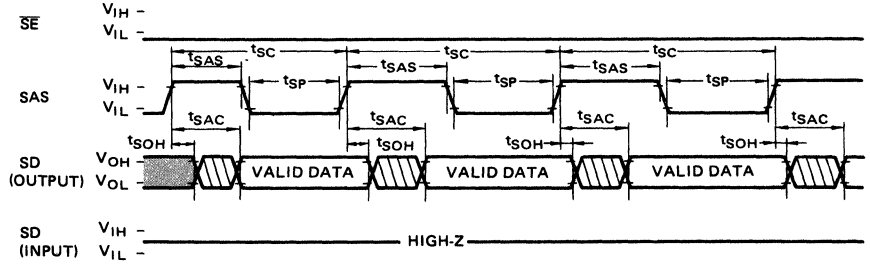
*: If $\overline{SE}$ is high, these data are not written into SAM.
**: If $\overline{SE}$ is high, SD (SD0 to SD3) are in High-Z state after t_{SEZ}.
If $\overline{SE}$ becomes low, the valid data will appear meeting t_{SAC} and t_{SEA}.

3

SERIAL READ CYCLE

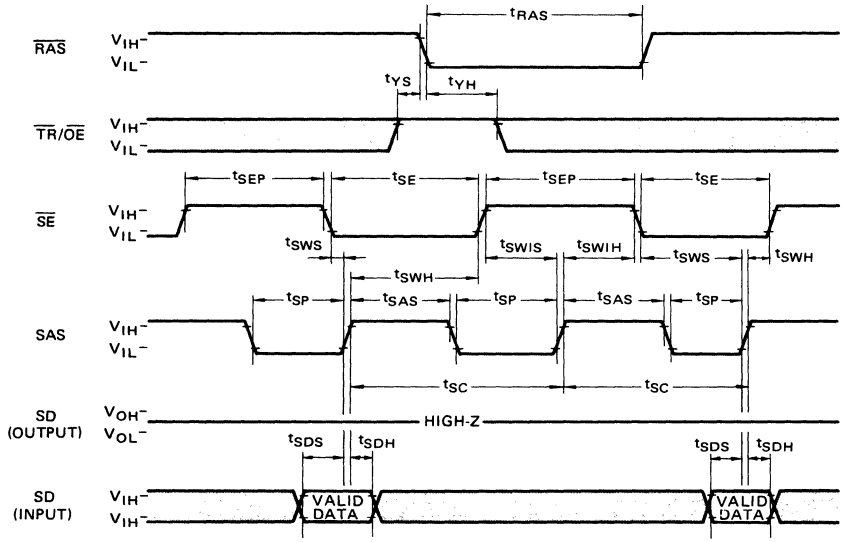


In the case of $\overline{SE}$="L" while the operation;

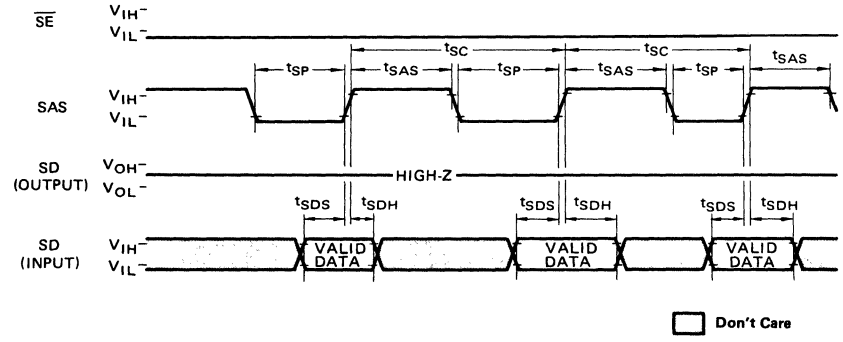


Invalid Data Don't Care

SERIAL WRITE CYCLE



In the case of $\overline{SE}$="L" while the operation;



Don't Care

3

Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

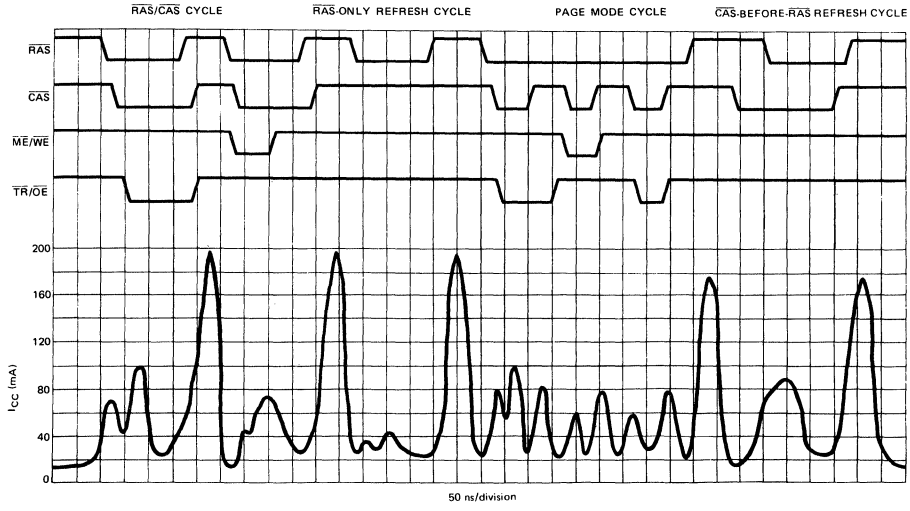
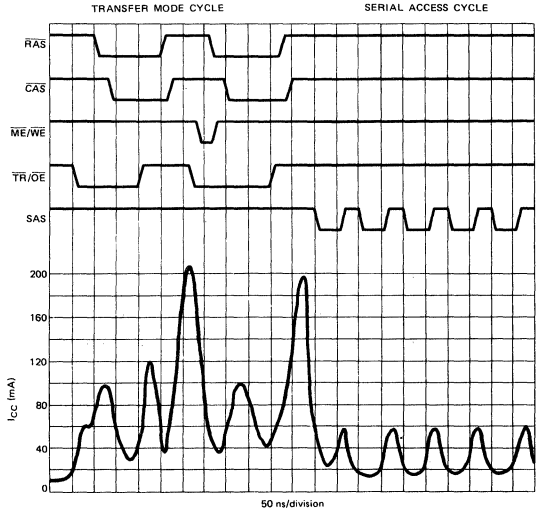


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C) (cont'd)



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

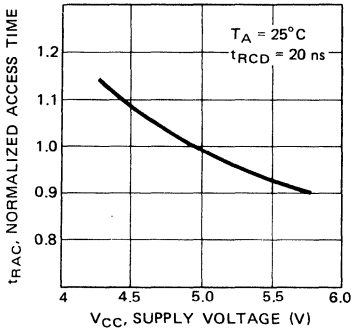


Fig. 7 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

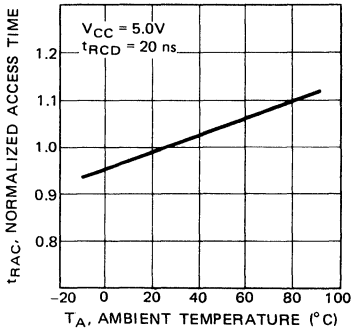


Fig. 8 – OPERATING CURRENT vs CYCLE RATE

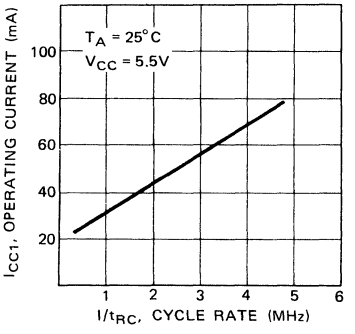


Fig. 9 – OPERATING CURRENT vs SUPPLY VOLTAGE

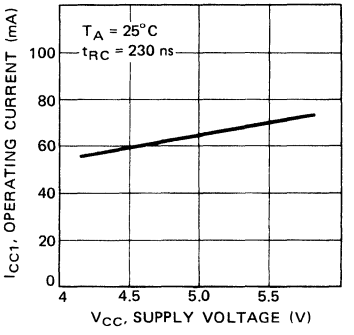


Fig. 10 – OPERATING CURRENT vs AMBIENT TEMPERATURE

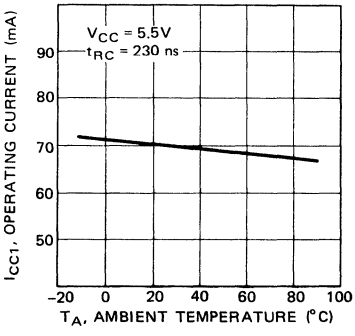
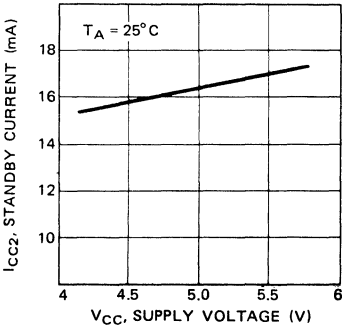


Fig. 11 – STANDBY SURRENT vs SUPPLY VOLTAGE



3

Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

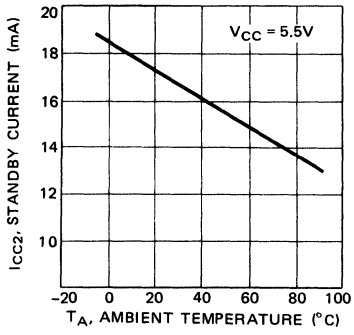


Fig. 13 – REFRESH CURRENT 1 vs CYCLE RATE

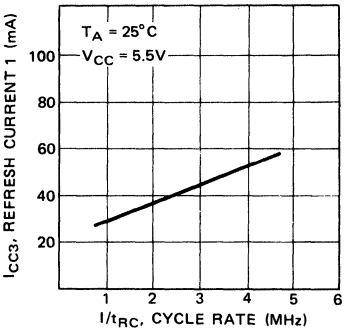


Fig. 14 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

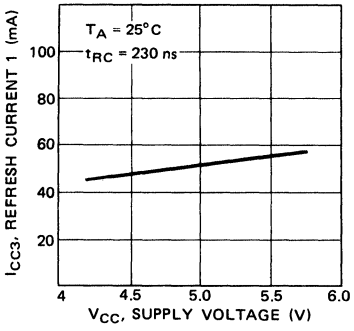


Fig. 15 – PAGE MODE CURRENT vs CYCLE RATE

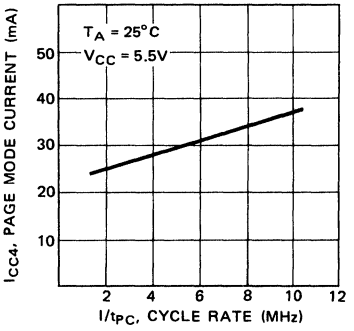


Fig. 16 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

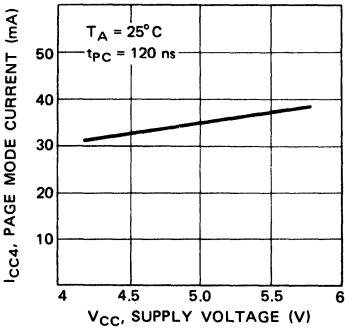


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

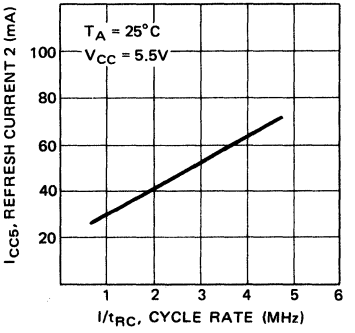


Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

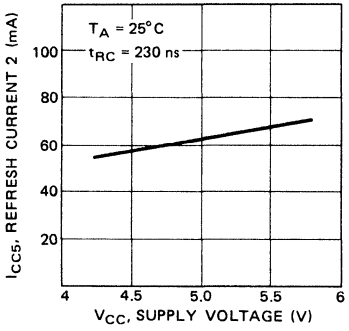
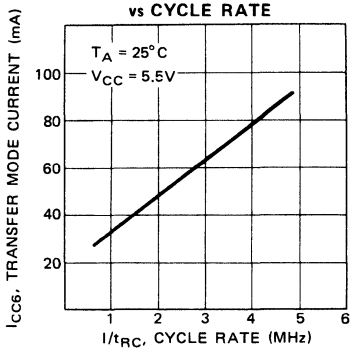


Fig. 19 – TRANSFER MODE CURRENT vs CYCLE RATE



3

Fig. 20 – TRANSFER MODE CURRENT vs SUPPLY VOLTAGE

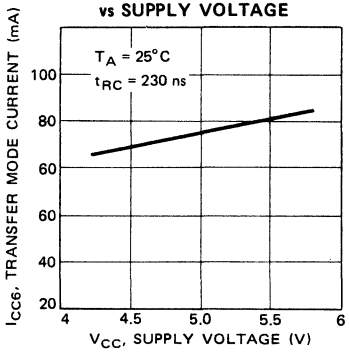


Fig. 21 – RAM STANDBY/SAM ACTIVE CURRENT vs CYCLE RATE

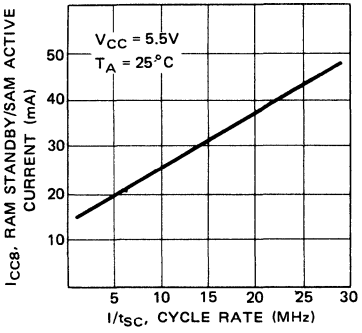


Fig. 22 – RAM STANDBY/SAM ACTIVE CURRENT vs SUPPLY VOLTAGE

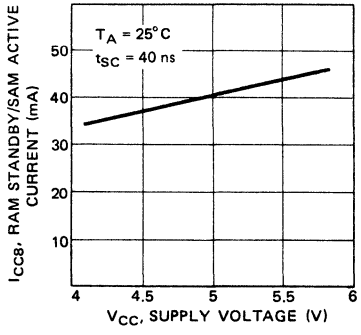


Fig. 23 – RAM STANDBY/SAM ACTIVE CURRENT vs AMBIENT TEMPERATURE

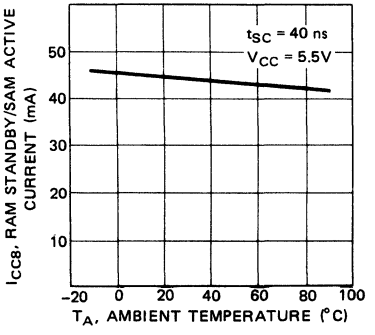


Fig. 24 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

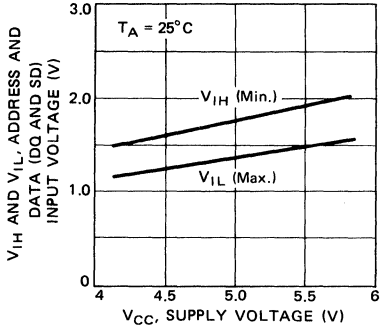


Fig. 25 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

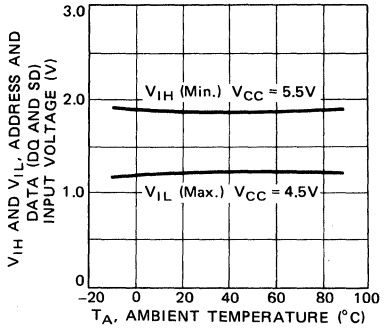


Fig. 26 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs SUPPLY VOLTAGE

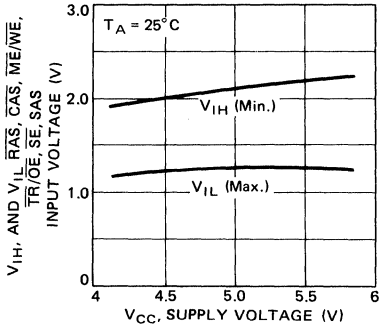


Fig. 27 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs AMBIENT TEMPERATURE

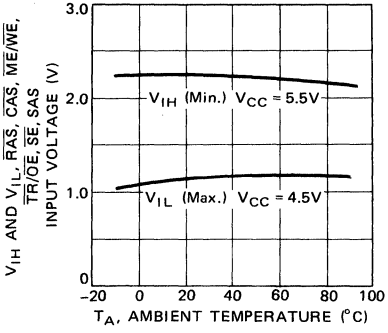


Fig. 28 – ACCESS TIME (RAM) vs LOAD CAPACITANCE

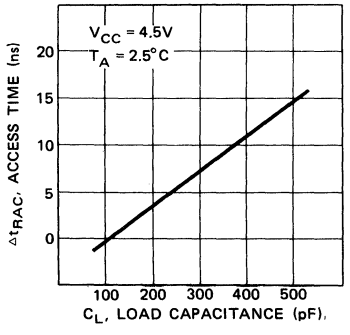


Fig. 29 – ACCESS TIME (SAM) vs LOAD CAPACITANCE

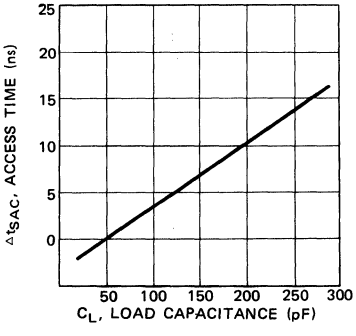


Fig. 30 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

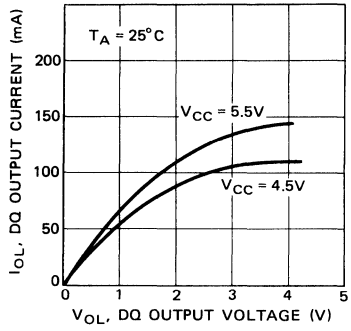


Fig. 31 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

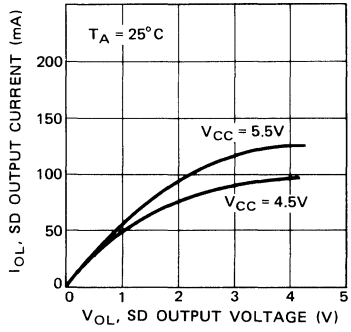


Fig. 32 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

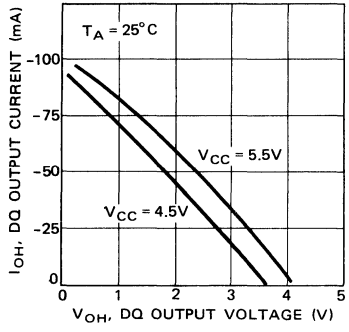


Fig. 33 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

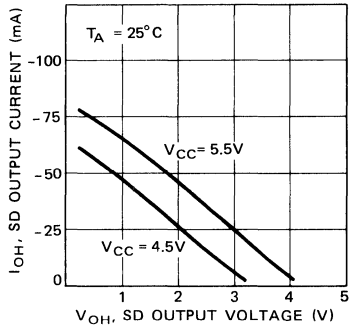
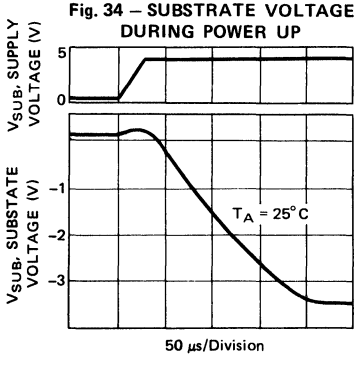


Fig. 34 – SUBSTRATE VOLTAGE DURING POWER UP

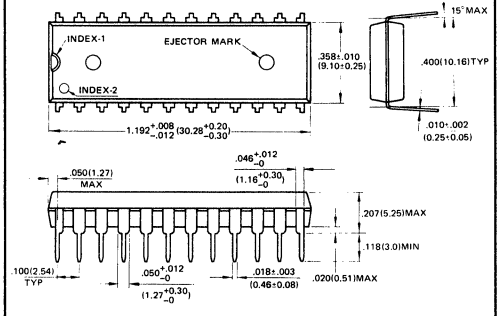


3

PACKAGE DIMENSIONS

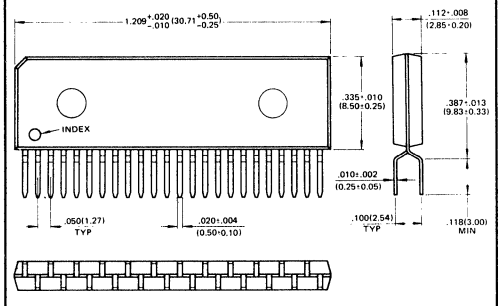
PLASTIC DIP (Suffix: -P) PLASTIC ZIP (Suffix: -PSZ)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE (CASE No.: DIP-24P-M04)



Dimentsions in inches (millimeters)

24-LEAD PLASTIC ZIGZAG-IN-LINE PACJAGE (CASE No.: ZIP-24P-M02)



Dimensions in inches (millimeters)

November 1990
Edition 2.0

FUJITSU

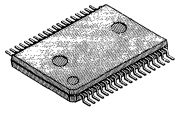
DATA SHEET

MB81C1501

1 M BIT 3 PORT CMOS DYNAMIC FIELD MEMORY

1, 175, 040 Bit 3 Port CMOS Dynamic Field Memory

The Fujitsu MB81C1501 is a 293, 760-word x 4 bit (960 pixels x 306 lines) field memory.
The MB81C1501 has a 3-port set-up (serial input: 1 port, serial output: 3 ports) allowing completely asynchronous and independent operation.
This device supports both the FIFO image operation mode which requires no external address input, and memory mapping in 60 bits units.
The MB81C1501 memory cell contains a dynamic refresh circuit. Refresh is performed during the routine read operation, eliminating the need for a special refresh cycle.
When used, this device facilitates digital imagery processing for TV and VTR, which allows plotting of high resolution multi-functions.
When two MB81C1501 units are used, (8 bit) field images compatible with both NTSC and PAL systems can be stored.
The MB81C1501 features a three-dimensional stacked capacitor cell, which has exceptional tolerance to alpha ray soft error and uses CMOS processing technology and high performance CMOS circuitry in peripheral circuits for low power consumption and high speed.



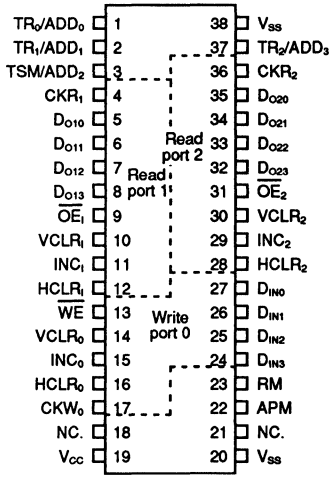
(FPT-38P-M01)

3

FEATURES

- 3 port organization
  One–293,760 word x 4 bit (serial write port)
  Two–293,760 word x 4 bit (serial read port) for common memory cell array
  960 x 306 x 4 bit
- Asynchronous input and output operation
- NTSC and PAL compatible
- Recursive mode:
  Automatic increment for vertical and horizontal address counter
- Nonrecursive mode:
  Specifiable vertical address and horizontal address
- Synchronous signal transfer capability between multiple chips.
- Gate function for input clock on the write side using $\overline{WE}$
- Silicon gate 3-layer polysilicon CMOS, 1-transistor cell
- Power : +5 V ±10%
- Input and output are TTL compatible. Low input capacitance
- 293,760 bit refresh cycle / 21 ms
- Internal substrate bias generator
- Standard 38-pin flat package

PIN ASSIGNMENT
(TOP VIEW)



Item		Symbol	Min.	Max.	Unit
Access time		t_{SAC}	–	25	ns
Cycle time	Read port	t_{SCR}	30	70 (Note 9)	ns
	Write port	t_{SCW}	50	$2t_{SCR}$ (Note 10)	ns

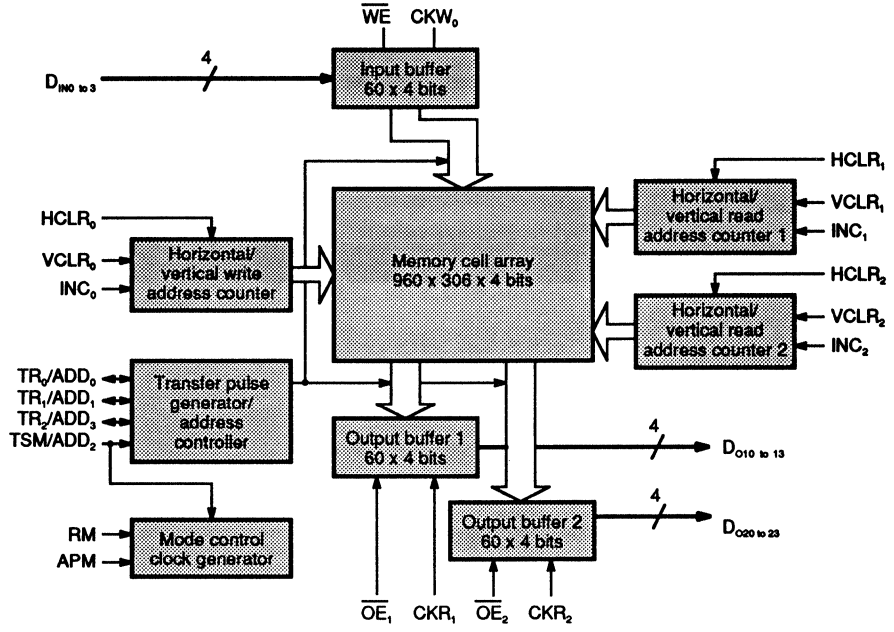
ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	–1 to + 7	V
Voltage of VCC supply relative to VSS	V_{CC}	–1 to+ 7	V
Power Dissipation	PD	1.0	V
Short Circuit Output Current	I_{OUT}	50	V
Storage Temperature	T_{STG}	–55 to + 125	°C

Note : Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM & PIN DESCRIPTION



Symbol	Port name	Mode	Symbol	Port name	Mode
RM	Recursive mode enable	Input	$VCLR_1$	Port 1, vertical clear signal	Input
APM	Address preset mode enable	Input	$HCLR_1$	Port 1, horizontal clear signal	Input
TSM	Transfer synchronous mode enable	Input	INC_1	Port 1, line increment signal	Input
TR_0	Write port 0, transfer synchronous signal	I/O	$\overline{OE}_1$	Port 1, output enable	Input
TR_1	Read port 1, transfer synchronous signal	I/O	D_{O10} to D_{O13}	Port 1, data output	Output
TR_2	Read port 2, transfer synchronous signal	I/O	CKR_2	Port 2, shift signal	Input
ADD_0 to ADD_3	Address input	Input	$VCLR_2$	Port 2, vertical clear signal	Input
CKW_0	Port 0, shift signal	Input	$HCLR_2$	Port 2, horizontal clear signal	Input
$VCLR_0$	Port 0, vertical clear signal	Input	INC_2	Port 2, line increment signal	Input
$HCLR_0$	Port 0, horizontal clear signal	Input	$\overline{OE}_2$	Port 2, output enable	Input
INC_0	Port 0, line increment signal	Input	D_{O20} to D_{O23}	Port 2, data output	Output
$\overline{WE}$	Port 0, write enable	Input	V_{CC}	Power (+5 V)	—
D_{IN0} to D_{IN3}	Port 0, data input	Input	V_{SS}	Power (0 V)	—
CKR_1	Port 1, shift signal	Input	NC.	No connection	—

EXPLANATION OF FUNCTIONS

RM

Depending on the state of this pin, the operation mode of the MB81C1501 splits into two paths: recursive mode when "H" and nonrecursive mode when "L".

Recursive mode: This mode is used to access the 960 x 306 memory cell sequentially from 0 to 293,759. Initialization is performed by input to the $VCLR_0$ to $_2$ pin. When writing, serial data is input when "H" on $VCLR_0$ is latched to CKW_0 and is treated as 0 line 0 block data input. When reading, serial data is output as 0 line 0 block data after a 64 clock delay from when an "H" on $VCLR_1$ to $_2$ is latched to CKR_1 to $_2$.

Nonrecursive mode: This mode treats the 960 x 306 memory cell as 1 line and 16 blocks (60 bits). This mode controls lines with $VCLR_0$ to $_2$ and INC_0 to $_2$, and controls blocks with $HCLR_0$ to $_2$. The difference between the two modes is as follows: for write operations, serial data input when an "H" on $HCLR_0$ is latched to CKW_0 is treated as data for line 0 block 0 in nonrecursive mode. In read operations, serial data output, delayed 64 clocks from when an "H" on $HCLR_1$ to $_2$ is latched to CKR_1 to $_2$, is output as data for line 0 block 0 from read port 1 and 2 respectively in nonrecursive mode.

APM

This pin is required for the mode in which block addresses are present in one line of the write port. The address preset mode is valid only when RM is "L" (nonrecursive mode). When $HCLR_0$ is latched to CKW_0 and this pin is "H", one of the sixteen blocks is selected by the 4 bits of ADD_0 to $_3$. The pin must be "L" when the address-preset mode is not used. Multi-function pins (TR_0/ADD_0, TR_1/ADD_1, TSM/ADD_2, and TR_2/ADD_3,) can be used in this case for TSM and TR_0 to $_2$.

3

TR_0/ADD_0, TR_1/ADD_1, TSM/ADD_2, and TR_2/ADD_3

These pins act as block address preset pins in the nonrecursive mode (RM = "L"), and when APM is "H" (address preset mode). When APM is "L", the pins act as synchronous transfer mode pins.

- In address preset mode, using 4-bit binary data fed to input pins ADD_0 to $_3$, a horizontal line block (60 bits) of the write port can be selected from among sixteen blocks.
- When TSM is "L" (master chip), a synchronizing signal for internal transfer timing with another MB81C1501 is output from TR_0 to $_2$. When TSM is "H" (slave chip), the synchronizing signal is received from the other device.
- TR_0 is an input-output pin for synchronous write transfer of the write port..
- TR_1 is an input-output pin for synchronous read transfer of read port 1.
- TR_2 is an input-output pin for synchronous read transfer of read port 2.
- When synchronous transfer mode is used, all of TR_0, TR_1, and TR_2, must be connected between master chip and slave chip.
- But when there are unused ports (for example, in case that read port isn't used), slave side synchronous transfer signal input pins (for example, TR_2) of the ports must be set "L" certainly.

CKW_0

The rise timing of this pin generates the signal that latches data onto the shift register of the input pins D_{IN0} to $_3$ and the input of each internal address point control pin ($VCLR_0$, $HCLR_0$, INC_0). This signal is also the basic signal for activation control of the internal clock-synchronization logic circuit and of the dynamic RAM. Therefore, the clock must operate whether there is a write operation or not.

$VCLR_0$

This pin has different functions for recursive mode (when RM = "H") and for nonrecursive mode (when RM = "L").
The number of $VCLR_0$ is not counted until "H" is latched to each CKW_0 after "L" is recognized. Even if "H" continues, it will only be counted once.

In recursive mode: When the "H" on $VCLR_0$ is latched to CKW_0, serial write data input is read as (0, 0). Input data of less than one block (60 bits) entered is disregarded.

In nonrecursive mode: When the "H" on $VCLR_0$ is latched to CKW_0, the shift register advances until the block (60 bits) during the current serial write operation is filled. Then the line is cleared. When $VCLR_0$ is input during serial write operations, after the input of 60 bits is completed, the serial write data is transferred to the memory cell of (v, h), and the subsequent data for serial write operation is transferred to the memory cell of (0, h+1).

$HCLR_0$

When an "H" on this pin is latched to CKW_0, the input data is read as data of (v, 0) data from the input data at that time. Data of less than one block (60 bits) entered up to that point is eliminated. But, input to this pin is invalid in recursive mode (when RM = "H").
The count number of $HCLR_0$ is not counted unless the "H" is latched to each CKW_0 after "L" is recognized. Even if "H" continues, it is only counted once.

INC_0

A line is incremented for each time this pin's "H" is latched to CKW_0. There are two ways that the incremented line can be valid: first, when an "H" on $HCLR_0$ is latched, and second, when the shift register advances up to the end of a block after the "H" on $VCLR_0$ is latched. But, signals to this pin have no meaning in recursive mode (when RM = "H").
The count number of INC_0 is not counted unless the "H" is latched to each CKW_0 after "L" is recognized. Even if "H" continues, it is only counted once.
When combined with $VCLR_0$, the next 60 bits data is input into the (n, h+1) memory cell. n is the count number of INC_0 counted from the status that $VCLR_0$ is latched to CKW_0 until the current write in shift register is filled up to 60 bits.
But, if INC_0 and $VCLR_0$ occur at the same time, INC_0 is invalid.
When combined with $HCLR_0$, the next 60 bits data is input into the (v+n, 0) memory cell. n is the count number of INC_0 counted from the status that $HCLR_0$ is latched to CKW_0 last time to the current latch status.
But, if INC_0 and $HCLR_0$ occur at the same time, INC_0 is invalid.

$CKR_{1,2}$

At the rise timing of this pin the shift register of the read port operates, and the signals to output data to the output pins D_{O10} to $_{13}$ and D_{O20} to $_{23}$, and to latch the input of each internal address pointer control pins ($VCLR_{1,2}$, $HCLR_{1,2}$, $INC_{1,2}$) are generated.

$VCLR_{1,2}$

This terminal has different functions in the recursive mode (RM = "H") and the nonrecursive mode (RM = "L").
The $VCLR_{1,2}$ count number is not counted unless the "H" is latched to each $CKR_{1,2}$ after "L" is recognized. Even if "H" continues, it is only counted once.

In recursive mode: When the "H" on $VCLR_{1,2}$ is latched to $CKR_{1,2}$, (0, 0) data is output with 64 clocks delay from that time. Meanwhile the shift register data (60 bits) in shift is output to its end, and the final output is saved.

In nonrecursive mode: When the "H" on $VCLR_{1,2}$ is latched to $CKR_{1,2}$, the current serial read block is output, and after output of the next 60 bit block, the block which continues the cleared line begins to be output. Therefore, $VCLR_{1,2}$ is latched and a line of the internal address counter is cleared. At this time, data for the next serial output (v, h+1) has already been transferred to the data register from the memory cell, and the data (0, h+2) is transferred with the data (v, h+1) is output, and next the (0, h+2) data is output.

$HCLR_{1,2}$

When the "H" of this pin is latched to $CKR_{1,2}$, the data (v, 0) is output with 64 clocks delay from that time. Meanwhile, shift register data in shift is output to its end and the last output is saved. When the RM pin is "H", signals to this pin have no meaning.
The $HCLR_{1,2}$ count number is not counted unless the "H" is latched to each $CKR_{1,2}$ after "L" is recognized. Even if "H" continues, it is only counted once.

$INC_{1,2}$

A line is incremented for each time this pin's "H" is latched to $CKR_{1,2}$. There are two ways for the incremented line to be valid: first, when the "H" on $HCLR_{1,2}$ is latched, and second, when the line address is latched at 56 clocks of the block after the "H" on $VCLR_{1,2}$ is latched. But, signals to this pin have no meaning in recursive mode (when RM = "H").
The $INC_{1,2}$ count number is not counted unless the "H" is latched to each $CKR_{1,2}$ after "L" is recognized. Even if "H" continues, it is only counted once.
When combined with $VCLR_{1,2}$, after the next data from the shift register should be output into the (n, h+2) memory cell. n is the count number of $INC_{1,2}$ counted while $VCLR_{1,2}$ is latched to each $CKR_{1,2}$ before 55 clocks block.
When $INC_{1,2}$ and $VCLR_{1,2}$ occurs at the same time, $INC_{1,2}$ is invalid.
When combined with $HCLR_{1,2}$, the shift register data is output from $HCLR_{1,2}$ with 64 clocks delay into (v+n, 0) memory cell. n is count number of $INC_{1,2}$ counted from when $HCLR_{1,2}$ is latched to each $CKR_{1,2}$ last time until $HCLR_{1,2}$ is latched at this time.
When $INC_{1,2}$ and $HCLR_{1,2}$ occur at the same time, $INC_{1,2}$ is valid.

DATA INPUT (D_{IN0} to $_3$)

Information to the data input pin is accepted and input into the shift register on the rising edge timing of CKW_0 with $\overline{WE}$ is the "L" state. When $\overline{WE}$ is "H", input data is not accepted and the write shift register does not operate (gate function of write clock).
Shift register input is executed immediately but after one block (60 bits) has been input into the memory cell, it is loaded into the data register, and is transferred from the data register to the memory cell until the shift register is fulled with new data. Thus, serial write data input delay serial write, is transferred to the memory cell with a one block delay.

INPUT CONTROL ($\overline{WE}$)

$\overline{WE}$ excutes input control to D_{IN0} to $_3$. When $\overline{WE}$ is "L", synchronous input to CKW_0 is enabled. When $\overline{WE}$ is "H", input is not acceptable and the operation of the shift of the write shift register is stopped. This is used when data input is sparse ($\overline{WE}$ gate function of on the write side of the input cycle (CKW_0)).

DATA OUTPUT (D_{O10} to $_{13}$, D_{O20} to $_{23}$)

The output buffer employs a three state TTL level, output is enabled when $\overline{OE}_{1,2}$ is "L" and data is output synchronous with $CKR_{1,2}$. Output goes to high impedance for "H", the shift register operates synchronously with $CKR_{1,2}$ and executes transfer between memory cell and data register and loading between data register and shift register.
Output from the shift register is always executed, data during output is data transferred to the shift register from a memory cell one block before the current output block.

OUTPUT CONTROL ($\overline{OE}_{1,2}$)

$\overline{OE}_1$ controls only the output pins D_{O10} to $_{13}$. $\overline{OE}_2$ controls only the output of pins D_{O20} to $_{23}$ and does not stop the operation of the read port shift register. When $\overline{OE}_{1,2}$ is "L", D_{O10} to $_{13}$ and D_{O20} to $_{23}$ output is enabled, a synchronous with $CKR_{1,2}$. When $\overline{OE}_{1,2}$ is "H", the output is high impedance state, and a synchronous with $CKR_{1,2}$.

FUNCTION TABLE

FUNCTION TABLE–1 <OPERATION MODE>

Operation mode	Control input			Address input	Transfer synchronous I/O
	RM	TSM	APM	$ADD_{0 to 3}$	$TR_{0 to 3}$
Recursive mode, transfer synchronous mode output	H	L	L	—	Valid Data Output
Recursive mode, transfer synchronous mode input	H	H	L	—	Valid Data Input
Nonrecursive mode, transfer synchronous mode output	L	L	L	—	Valid Data Output
Nonrecursive mode, transfer synchronous mode input	L	H	L	—	Valid Data Input
Nonrecursive mode, address preset mode	L	–	H	Valid Data Input	—

H : High level L : Low level

3

ADDRESS – BLOCK CORRESPONDENCE TABLE

Block number	ADD_3	ADD_2	ADD_1	ADD_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H : High level L : Low level

NOTE: The block number increases with each write or read of a line.

FUNCTION TABLE–2 <WRITE>

Mode description	No.	Cycle description	RM	$VCLR_0$	$HCLR_0$	INC_0	APM	ADD_{0-3}	Internal address pointer
Recursive mode	1	Initial cycle	H	H	–	–	L	—	(v, h) is cleared to (0, 0).
	2	Normal cycle		L					Cycles from (0, 0) to (305, 15).
Nonrecursive mode	1	Initial cycle	L	H	H	L			(v, h) is cleared to (0, 0).
	2	Normal cycle		L	L	L			Stops at (v, 15).
	3	First block cycle		L	H	L			(v, h)h is cleared to (v, 0).
	4	Line address cycle		L	H	nH			(v, h)v is set and h is cleared to (v+n, 0).
	5	$VCLR_0$ special cycle No. 1		H	L	L			(v, h)v is cleared to (0, h+1).
		$VCLR_0$ special cycle No. 2		H	L	nH			(v, h)v is set to (v+n, h+1).
		$VCLR_0$ special cycle No. 3		H	H	nH			(v, h)v is set and h is cleared to (n, 0).
Nonrecursive address preset mode	1	Initial cycle		H	H	L	H	Valid data	(v, h)v is cleared and h is set to (0, ADD).
	2	Normal cycle		L	L	L		—	Stops at (v, 15).
	3	First block cycle		L	H	L		Valid data	(v, h)h is set to (v, ADD).
	4	Line address cycle		L	H	nH		Valid data	(v, h)v and h are set to (v+n, ADD).
	5	$VCLR_0$ special cycle No. 1		H	L	L		—	(v, h)v is cleared to (0, h+1).
		$VCLR_0$ special cycle No. 2		H	L	nH		—	(v, h)v is set to (n, h+1).
		$VCLR_0$ special cycle No. 3		H	H	nH		Valid data	(v, h)v and h are set to (n, ADD).

Note.

1. (v, h)v : Line address (0 to 305) at control signal input
   (v, h)h : Block address (0 to 15) at control signal input
2. Directly set the mode design signal (RM, APM) to "H" or "L".
3. H : "H" level is latched by CKW_0.
   nH : "H" level is latched n times by CKW_0.
4. 60 bits of input data are read from $VCLR_0$, in recursive mode. In nonrecursive mode, data read starts with the data latched by CKW simultaneously with $HCLR_0$. If $VCLR_0$ and $HCLR_0$ are input before the full 60 bits of data is input, the data is invalid.
5. When the APM signal is low, the TSM pin is invalid and both the read port and the write port enter the transfer synchronous mode. A low on the TSM pin puts the MB81C1501 into the master operation mode. In this mode the device outputs an internal transfer timing synchronization signal to the slave MB81C1501. A high on the TSM pin puts the device into the slave mode: and it receives the synchronization signal from the master MB81C1501.
6. Block address (ADD0 to 3) at address preset mode must be latched with CKW_0 and $HCLR_0$ at the same time.

FUNCTION TABLE–3 <READ>

Mode description	No.	Cycle description	RM	$VCLR_{1,2}$	$HCLR_{1,2}$	$INC_{1,2}$	APM	ADD_{0-3}	Internal address pointer
Recursive mode	1	Initial cycle	H	H	–	–	–	–	(v, h) is cleared to (0, 0).
	2	Normal cycle		L					Cycles from (0, 0) to (305, 15).
Nonrecursive mode	1	Initial cycle	L	H	H	L			(v, h) is cleared to (0, 0).
	2	Normal cycle		L	L	L			Stops at (v, 15).
	3	First block cycle		L	H	L			(v, h) h is cleared to (v, 0).
	4	Line address cycle		L	H	nH			(v, h)v is set and h is cleared to (v+n, 0).
	5	$VCLR_{1,2}$ special cycle No. 1		H	L	L			Advances to (v, h) (v, h+1), and v is cleared to (0, h+2).
		$VCLR_{1,2}$ special cycle No. 2		H	L	nH			Advances to (v, h) (v, h+1), and v is set to (n, h+2).
		$VCLR_{1,2}$ special cycle No. 3		H	H	nH			(v, h)v is set and h are cleared to (n, 0).

Note.

*1. H : "H" level is latched by $CKR_{1,2}$.
nH : "H" level is latched n times by $CKR_{1,2}$.

*2. 60 bits of output data are output from $VCLR_{1,2}$, in recursive mode, or from $HCLR_{1,2}$ in nonrecursive mode with a 64-clock-cycle delay.

*3. If $VCLR_{1,2}$ or $HCLR_{1,2}$ is input during output of a block, the data of the output block or the next block is protected in 60 bit units. Until the new data is output, the latest data is protected.

*4. When the number of blocks ($VCLR_{1,2}$ to $VCLR_{1,2}$, $HCLR_{1,2}$ to $HCLR_{1,2}$) is set to a multiple of 60 clock cycles, continuous data access is possible.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	1	V_{CC}	4.5	5.0	5.5	V
		V_{SS}	0	0	0	V
Operating temperature		T_A	0	–	70	°C

CAPACITANCE

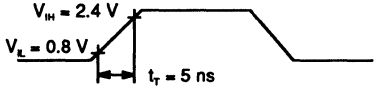
(T_A = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input capacitance	C_{IN}	–	7	pF
Output capacitance (D_{O10} to D_{O23})	C_D	–	7	pF
I/O capacitance (TR_0 to TR_2)	C_T	–	10	pF

3

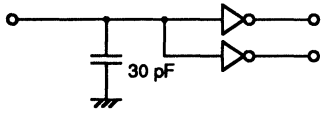
AC TEST CONDITIONS

1) Input

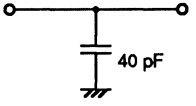


2) Output

3) Data output load (D_{O10} to D_{O23})



4) Transfer synchronous output load (TR_0 to TR_2)



DC CHARACTERISTICS

(Under recommended operating conditions unless otherwise noted.) Notes 4

Parameter	Notes	Conditions				
Operating current #1	2	t_{SCWO} = 70 ns, $t_{SCR1,2}$ = 70 ns	I_{CC1}	–	45	mA
Operating current #2	2	t_{SCWO} = 70 ns, $t_{SCR1,2}$ = 35 ns		–	60	mA
Operating current #3	2	t_{SCWO} = 50 ns, $t_{SCR1,2}$ = 50 ns		–	60	mA
Operating current #4	2	t_{SCWO} = 50 ns, $t_{SCR1,2}$ = 30 ns		–	75	mA
Refresh current	2, 3	t_{SCWO} = 420 ns, $t_{SCR1,2}$ = 70 ns	I_{CC2}	–	20	mA
Input leakage current		0 V ≤ V_{IN} ≤ 5.5 V, VCC=5.5V, VSS=0V All other pins not under test is 0V	$I_{I(L)}$	–10	10	µA
Output leakage current		output impedance, 0 V ≤ V_{OUT} ≤ 5.5 V	$I_{O(L)}$	–10	10	µA
Input High Voltage	1	all input pins	V_{IH}	2.4	6.5	V
Input Low Voltage	1	all input pins	V_{IL}	–2.0	0.8	V
Output High Voltage	1	I_{OH} = –2 mA	V_{OH}	2.4	–	V
Output Low Voltage	1	I_{OL} = 4.2 mA	V_{OL}	–	0.4	V

3

AC CHARACTERISTICS

(Under recommended operating conditions unless otherwise noted.) Notes 4, 5

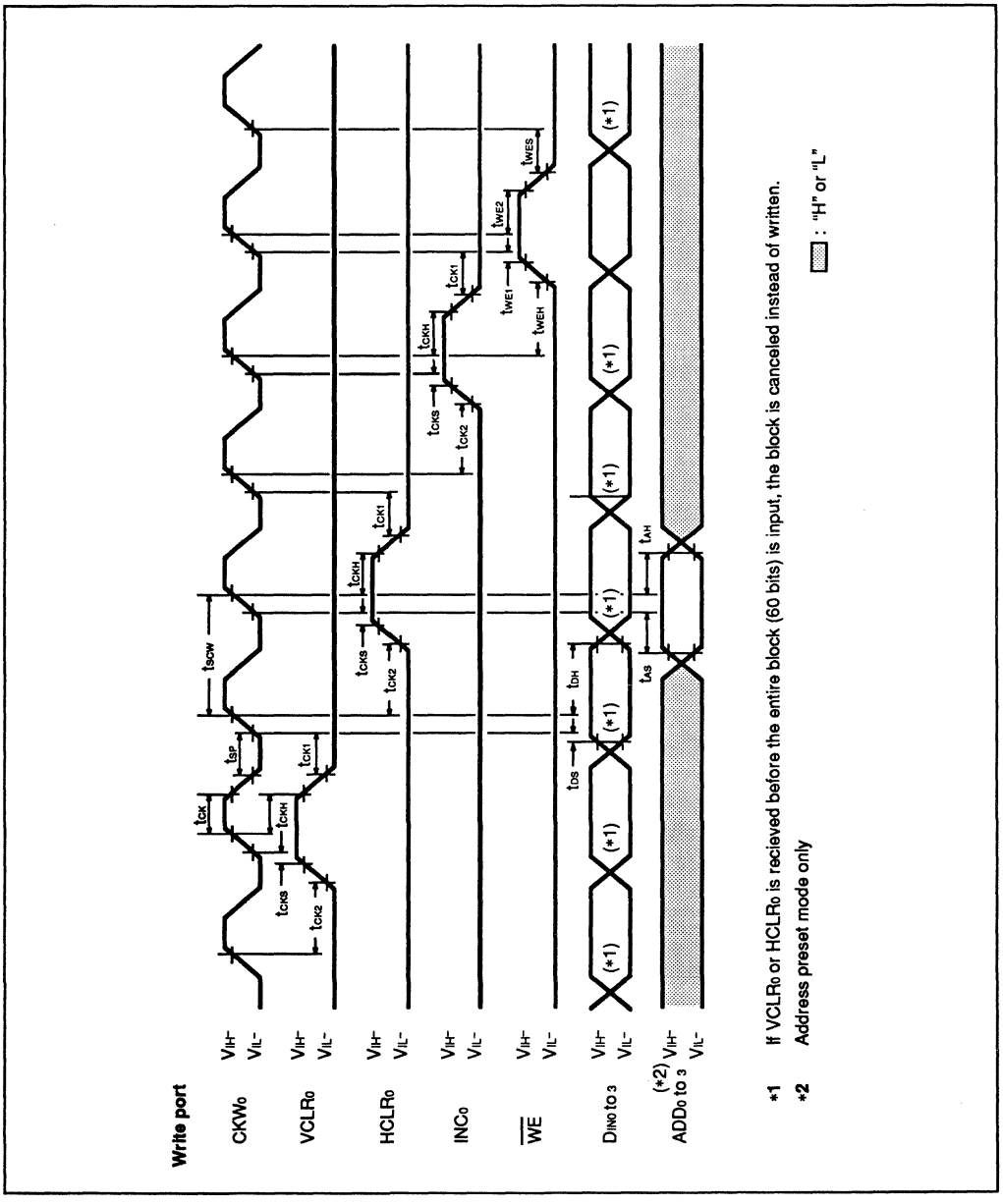
Parameter	Symbol	Min	Max	Unit	Notes
Time Between Refresh	t_{REF}	–	21	ms	
CKR Cycle time	t_{SCR}	30	70	ns	*9
Pulse width for CKW and CKR (CKW, CKR Pulse width)	t_{CK}	8	–	ns	
Precharge time for CKW and CKR (CKW, CKR Precharge time)	t_{SP}	8	–	ns	
Access time from CKR	t_{SAC}	–	25	ns	*6
Data output hold time from CKR	t_{SOH}	5	–	ns	*6
Access time from $\overline{OE}$	t_{OEA}	–	20	ns	*6
$\overline{OE}$ data output hold time	t_{OEH}	5	–	ns	*6
Data output turn-off delay time from $\overline{OE}$	t_{OEZ}	–	20	ns	*6
Active setup time for VCLR, HCLR, INC-CKR, and CKW	t_{CKS}	5	–	ns	
Active hold time for VCLR, HCLR, INC-CKR, and CKW	t_{CKH}	7	–	ns	
Inactive setup time for VCLR, HCLR, INC-CKR, and CKW	t_{CK1}	5	–	ns	
Inactive hold time for VCLR, HCLR, INC-CKR, and CKW	t_{CK2}	7	–	ns	
CKW Cycle time	t_{SCW}	50	2 t_{SCR}	ns	*10
Setup time for D_{IN} and CKW	t_{DS}	5	–	ns	
Hold time for D_{IN} and CKW	t_{DH}	7	–	ns	
Active setup time for $\overline{WE}$ and CKW	t_{WES}	5	–	ns	
Active hold time for $\overline{WE}$ and CKW	t_{WEH}	7	–	ns	
Inactive setup time for $\overline{WE}$ and CKW	t_{WE1}	5	–	ns	
Inactive hold time for $\overline{WE}$ and CKW	t_{WE2}	7	–	ns	
Setup time for ADD and CKW	t_{AS}	10	–	ns	
Hold time for ADD and CKW	t_{AH}	8	–	ns	
Access time for transfer synchronous output from CKW	t_{TAC}	–	25	ns	*7
Number of transfer synchronous output pulses TR_0 TR_1, TR_2	t_{TWOP} t_{TROP}	5 4	5 4		*7, *8
Turn-off delay time for transfer synchronous output from CKW	t_{TZ}	–	25	ns	*7
Number of transfer synchronous output interval pulses	t_{TO1}	1	–		*8
Active setup time for TR_0, TR_1, and TR_2-CKW	t_{TS}	15	–	ns	
Active hold time for TR_0, TR_1, and TR_2-CKW	t_{TH}	7	–	ns	
Inactive setup time for TR_0, TR_1, and TR_2-CKW	t_{TSS1}	7	–	ns	
Inactive hold time for TR_0, TR_1, and TR_2-CKW	t_{TSS2}	7	–	ns	
Number of transfer synchronous input pulses TR_0 TR_1, TR_2	t_{TWIP} t_{TRIP}	5 4	5 4		*8
Number of transfer synchronous input interval pulses	t_{TII}	1	–		*8
Rise and fall time for input pulse	t_T	3	40	ns	

3

Notes :

1. Referenced to V_{ss}
2. I_{CC} depends on cycle time and output load conditions. The specified values are obtained with the output open.
3. $\overline{WE}$ = "H" : one read port active
4. An initial pause of 200μs is required after power–up followed by dummy cycle before proper device operation For dummy cycle, a minimum of one VCLR is required in recursive mode, and VCLR and HCLR for non-recursive mode.
5. AC test conditions :
   - Input pulse level : 0 V to 3 V
   - Rise and fall time of input pulse : t_T = 5 ns
   - Standard voltage level for timing calibrations : Input V_{IH} = 2.4 V, V_{IL} = 0.8 V; Output V_{OH} = 2.4 V, V_{OL} = 0.6 V
6. 2 TTL + 30 pF load
7. 40 pF load
8. Number of t_{SCW} pulses
9. This parameter for a read port assures the refresh operation. When two read ports are used, one of them is controlled by this parameter, and the other one is not.
10. The maximum cycle time of the write port (t_{SCW}) can be extended to twice the cycle time (t_{SCR}) of the faster read port. For the refresh operation, when $\overline{WE}$ is "H" and one of the read ports is active, the write cycle time (t_{SCW}) can be extended to six times the read cycle time(t_{SCR}). When refresh power is minimal, the read cycle time (t_{SCR}) is 70 ns and write cycle time (t_{SCW}) is 420 ns.

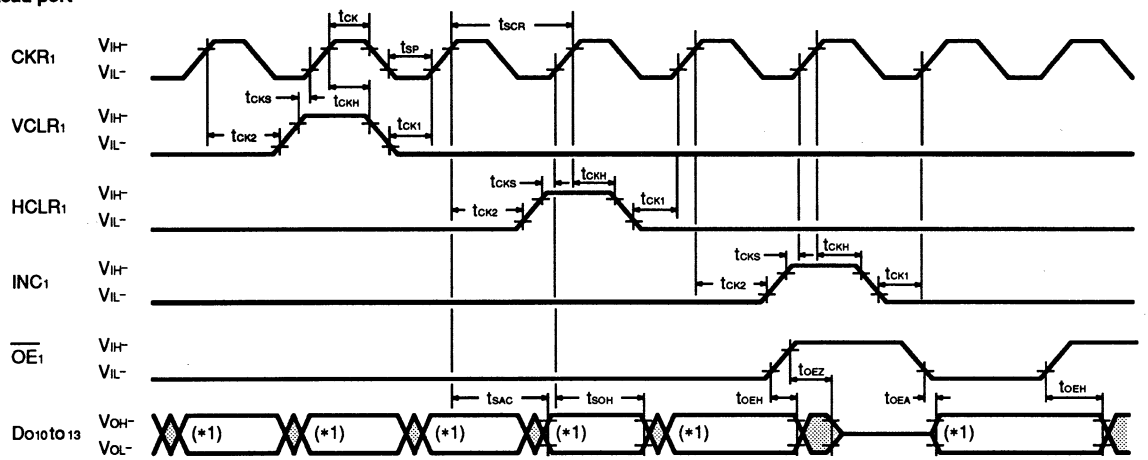
TIMING DIAGRAM



*1 If VCLR0 or HCLR0 is recieved before the entire block (60 bits) is input, the block is canceled instead of written.

*2 Address preset mode only

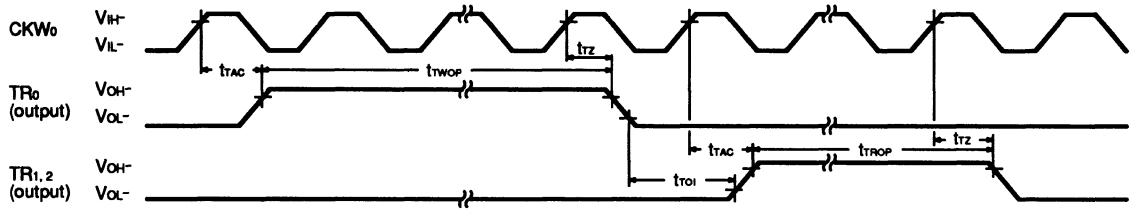
Read port



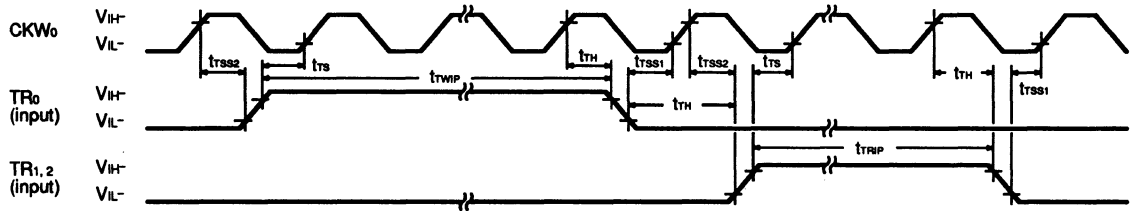
*1 Period of fixed output

▒ : Invalid data

TRANSFER SYNCHRONOUS MODE (MASTER CHIP)

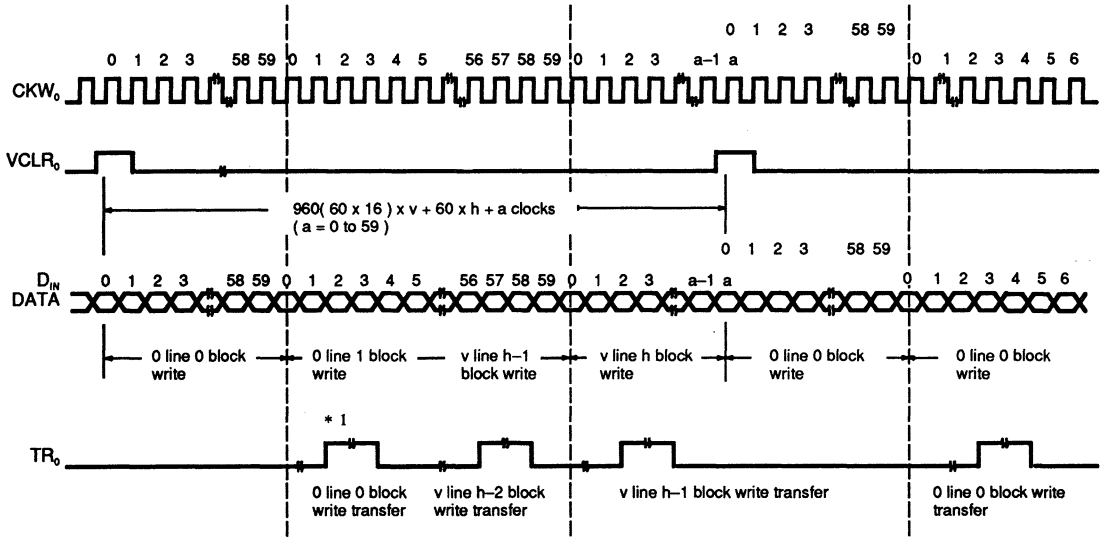


TRANSFER SYNCHRONOUS MODE (SLAVE CHIP)



RECURSIVE MODE (WRITE)

1) **INITIAL CYCLE ($\overline{WE}$ = "L", $HCLR_0$ AND INC_0 ARE DISABLE.)**



NOTE

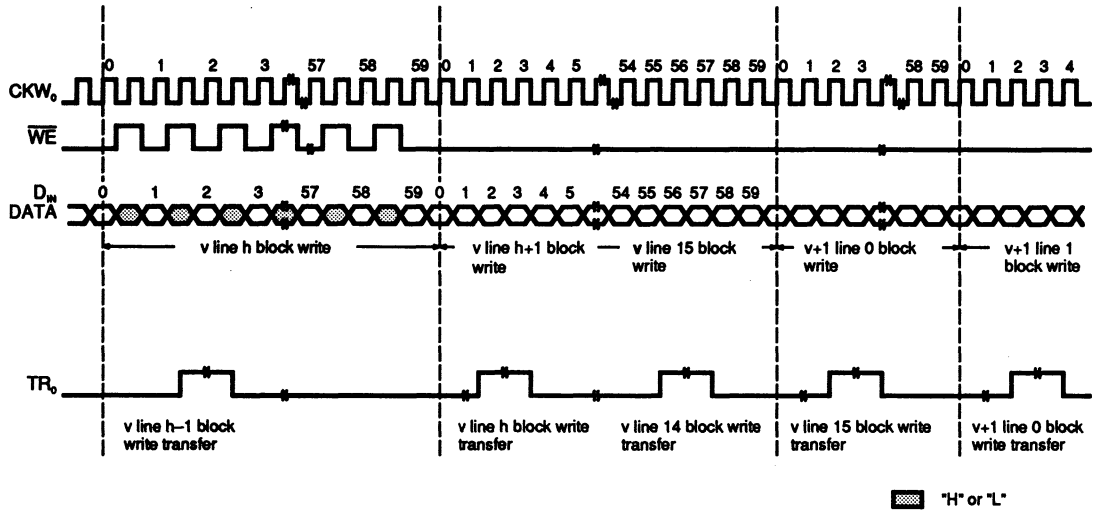
1) In case that $VCLR_0$ is input at 960 x v + 60 x h + a (a = 0 to 59) clock from the previous $VCLR_0$ clock, the input data at the same time with $VCLR_0$ is input from 0 block as the data of 0 line.

2) Input data in write cycle of v line h block are invalid.

*1 In case that TSM pin = "L", TR_0 is automatically output synchronously with CKW_0.
In case of synchronous transfer between two chips, TR_0 is automatically transfered between two chips.

RECURSIVE MODE (WRITE)

2) **NORMAL CYCLE ($VCLR_0$ = "L", $HCLR_0$ AND INC_0 ARE DISABLE .)**



NOTE

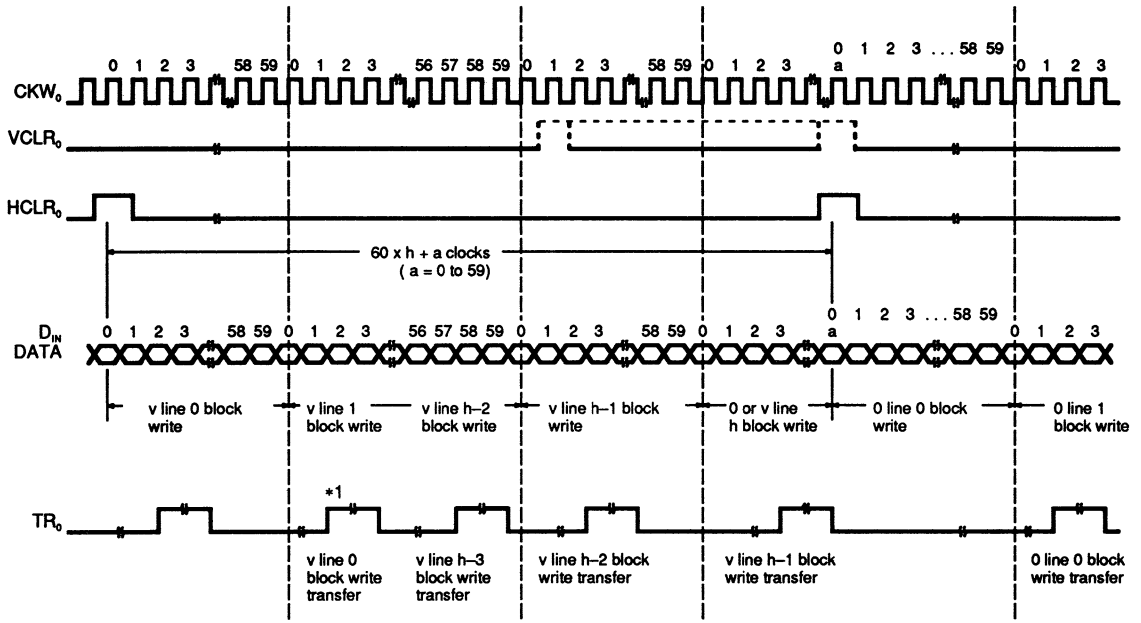
1) After v line 15 block write, next data is automatically written from 0 block of next line.

2) After 305 line 15 block write, next data is automatically written from 0 block of next line.

3) In case that $\overline{WE}$ = "H", input data is invalid.

NON-RECURSIVE MODE (WRITE)

1) **INITIAL CYCLE (INC$_o$ = $\overline{WE}$ = "L")**



NOTE

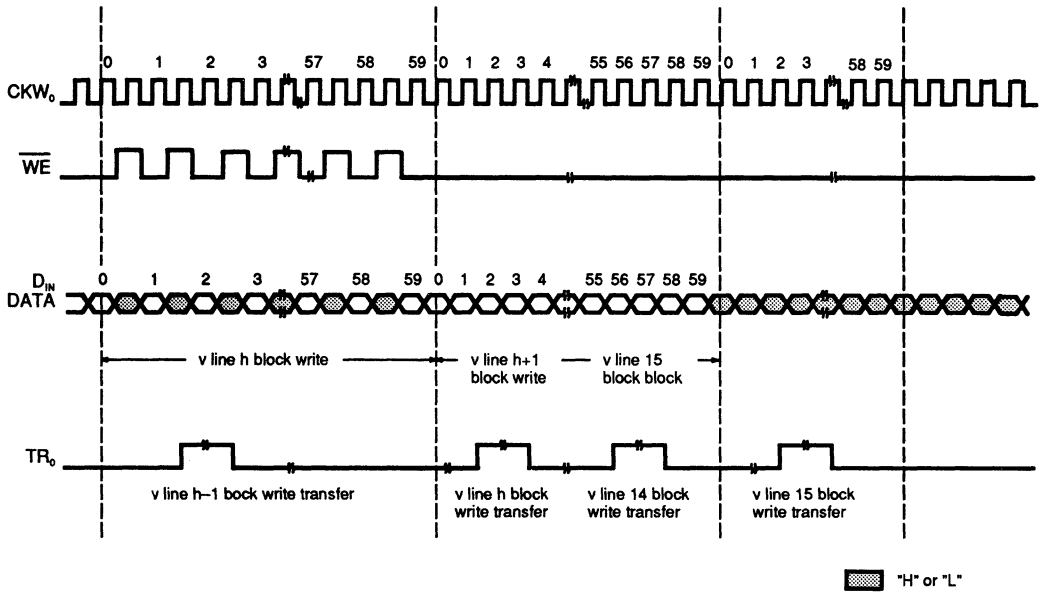
1) In case that HCLR$_o$ is input at the same time or after VCLR$_o$ at 60 x h + a (a=0 to 59) clock from the previous HCLR$_o$ clock, the input data concurrently with HCLR$_o$ is input from 0 line as the data of 0 line. However, it is necessary to input VCLR$_o$ between 60 x (h–1) + 1 clock and 60 x h + a clock from the previous HCLR$_o$ clock.

2) Input data in write cycle of v line h block is invalid.

* 1 In case that TSM pin = "L", TR$_o$ is automatically output synchronously with CKW$_o$.
In case of synchronous transfer between two chips, TR$_o$ is automatically transfered between two chips.

NON-RECURSIVE MODE (WRITE)

2) **NORMAL CYCLE ($VCLR_0$ = $HCLR_0$ = INC_0 = "L")**

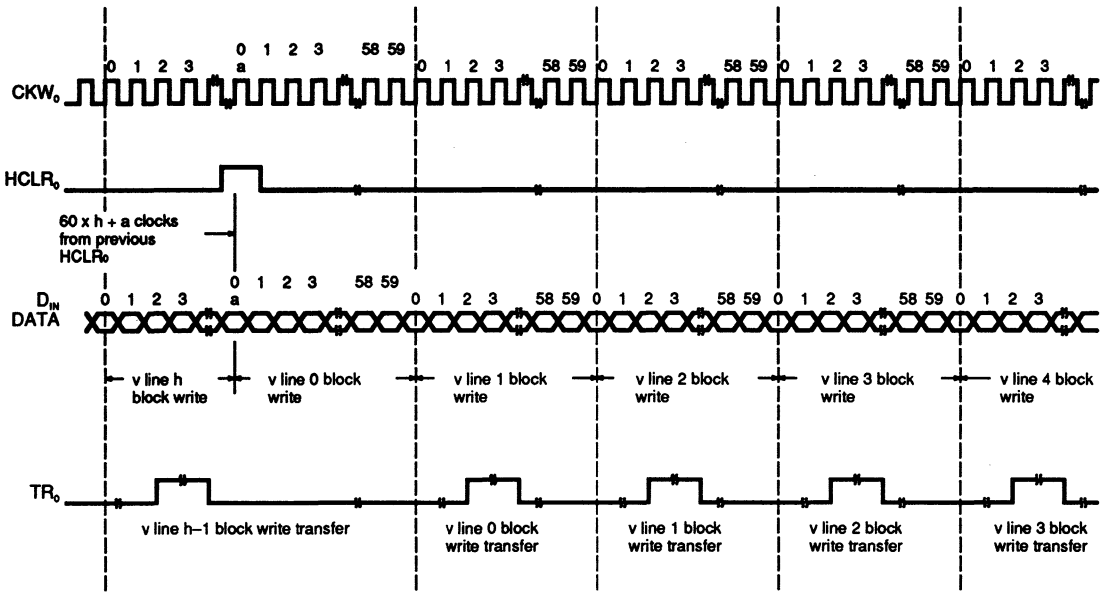


1) The input data after v line 15 block write is invalid. And the device re–operates by $HCLR_0$ clock.

2) In case that $\overline{WE}$ = "L", input data is invalid.

NON-RECURSIVE MODE (WRITE)

3) FIRST BLOCK CYCLE ($VCLR_0$ = INC_0 = $\overline{WE}$ = "L")



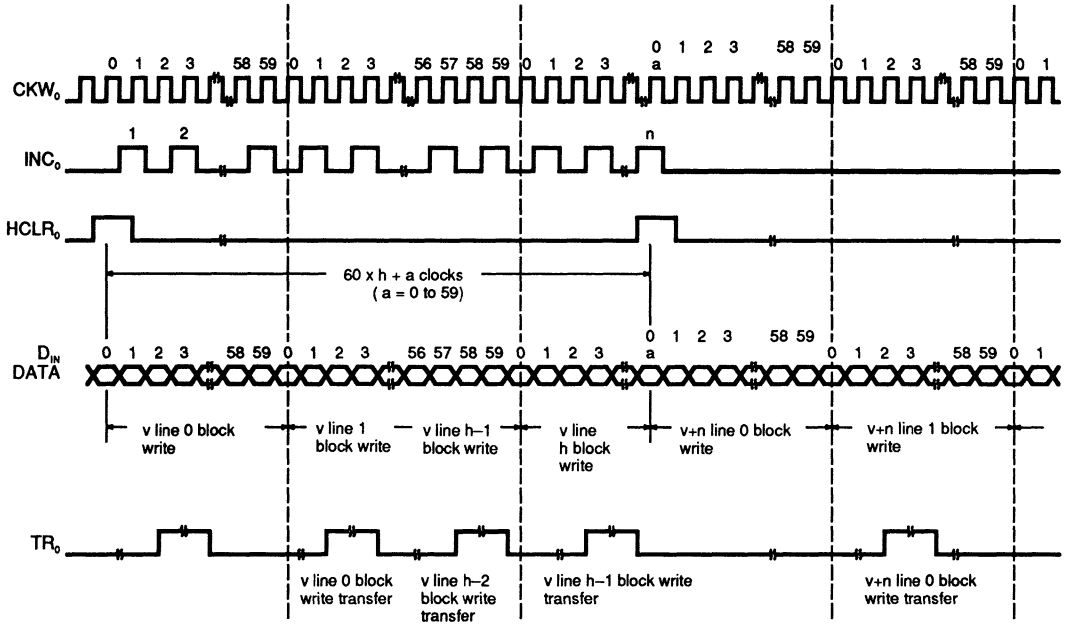
NOTE

1) In case that $HCLR_0$ is input at 60 x h + a (a = 0 to 59) clock from the previous $HCLR_0$ clock, the data is input from input data at the same with $HCLR_0$ to 0 block as data of v line.

2) Input data in write cycle of v line h block is invalid.

NON-RECURSIVE MODE (WRITE)

4) LINE ADDRESS CYCLE ($VCLR_0$ = $\overline{WE}$ = "L")



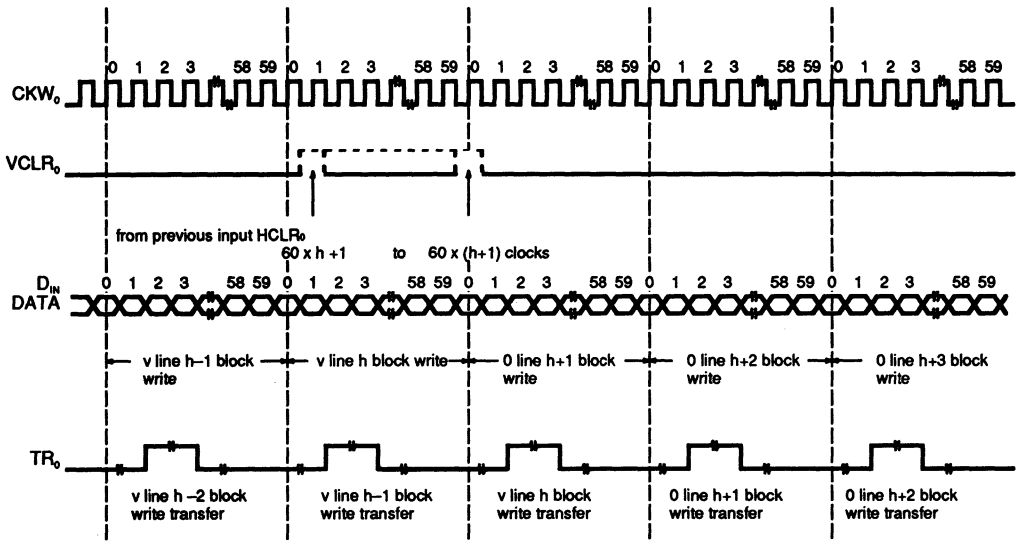
NOTE

1) In case that INC_0 is input n times while $HCLR_0$ is input at 60 x h + a (a = 0 to 59) clock from the clock input previous $HCLR_0$ clock, the data is input from input data at the same time with $HCLR_0$ to 0 block as data of v+n line.

2) The input INC_0 input after $HCLR_0$ clock is invalid.

NON-RECURSIVE MODE (WRITE)

5) **$VCLR_T$ SPECIAL CYCLE No. 1 ($HCLR_0 = INC_0 = \overline{WE}$ = "L")**

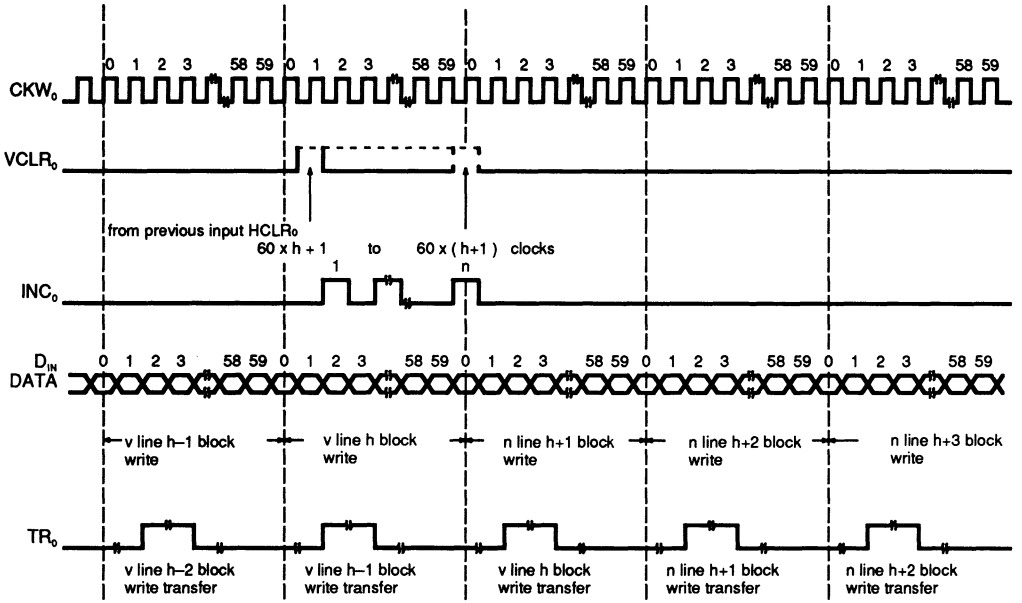


NOTE

1) In case that $VCLR_0$ is input between 60 x h + 1 and 60 x (h + 1) clock from the previous $HCLR_0$ clock, after v line h block write, line address is reset only and written at h + 1 block as the data of 0 line continuously.

NON-RECURSIVE MODE (WRITE)

5) $VCLR_1$ SPECIAL CYCLE No. 2 ($HCLR_0 = \overline{WE}$ = "L")

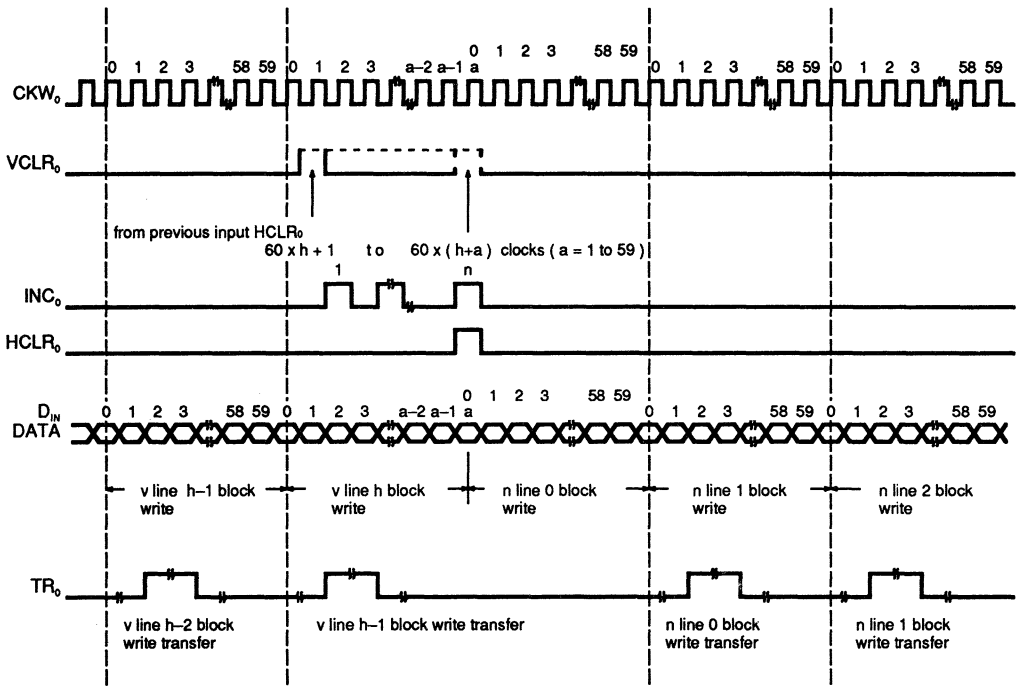


NOTE

1) In case that INC_0 is input n times after $VCLR_0$ is input between 60 x h + 1 and 60 x (h+1) clock from the previous $HCLR_0$ clock, line address is reset only after v line h block write and written at h + 1 block as data of 0 line.

2) The input INC_0 at the same time with $VCLR_0$ clock is invalid.

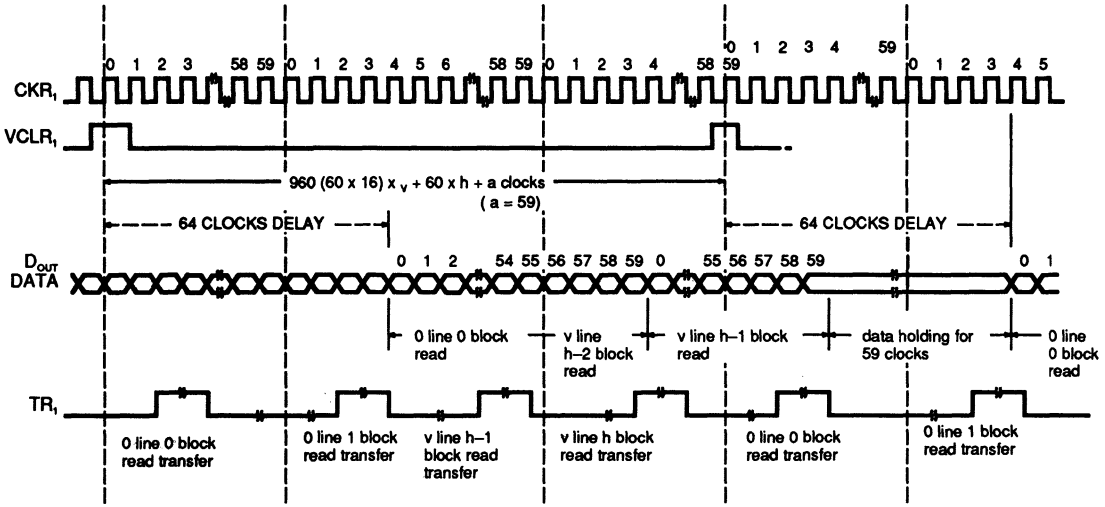
NON-RECURSIVE MODE (WRITE)
5) VCLR$_1$ SPECIAL CYCLE No. 3 ($\overline{WE}$ = "L")



NOTE
1) In case that HCLR$_o$ is input after INC$_o$ is input n times while VCLR$_o$ is input at 60 x h + a (a = 1 to 59) clock from the previous HCLR$_o$ clock , the data is input at the same time with HCLR$_o$ from 0 block as data of 0 line.
2) The input INC$_o$ at the same time or before VCLR$_o$ clock is invalid. And the input INC$_o$ at the same time or before HCLR$_o$ clock is valid.
3) Input data in write cycle of v line h block is invalid.

RECURSIVE MODE (READ)

1) **INITIAL CYCLE ($HCLR_1$ = INC_1 = $\overline{OE}_1$ = "L")**



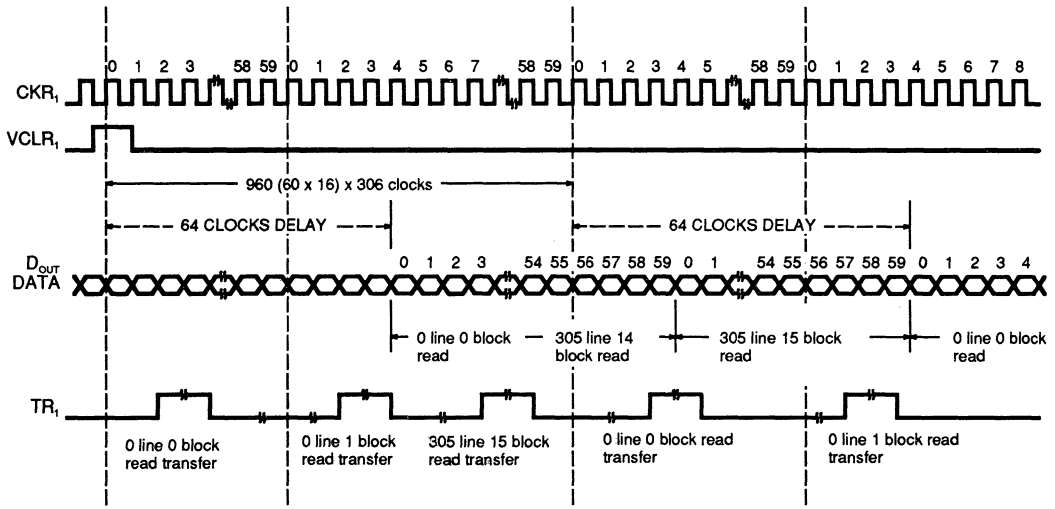
NOTE

1) In case that $VCLR_1$ is input at 960 x v + 60 x h + a (a = 0 to 59) clock from the previous $VCLR_1$ clock, the last output data in v line h–1 block is held during a (a = 0 to 59) clocks . Then the data of 0 line is output from 0 block.
(The data of 0 line 0 block is output 64 clocks later after $VCLR_1$.)

2) Transfer data of v line h block is invalid.

RECURSIVE MODE (READ)

2) **NORMAL CYCLE ($HCLR_1 = INC_1 = \overline{OE_1}$ = "L")**



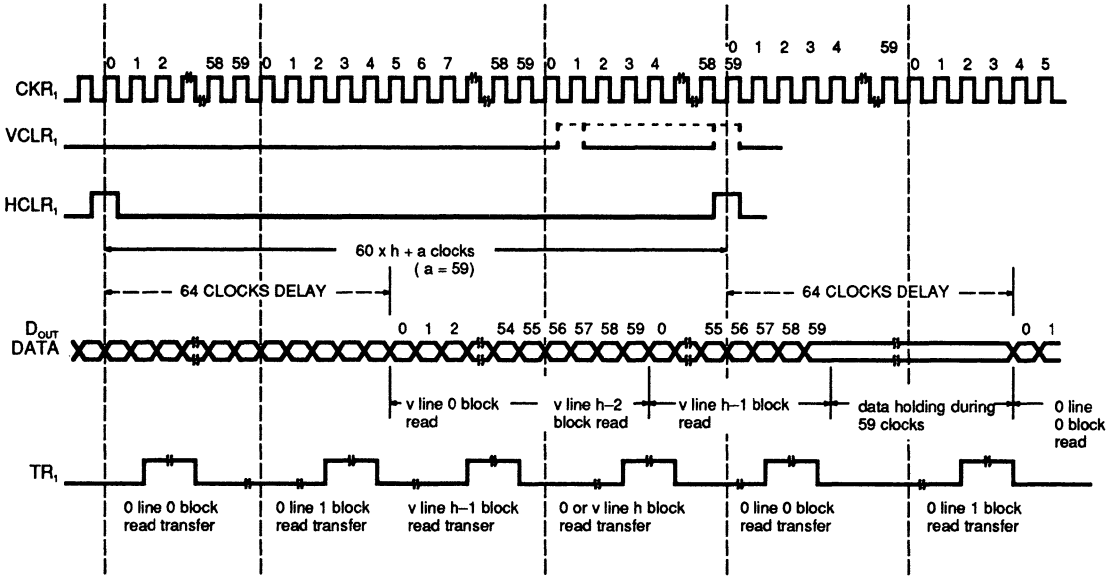
NOTE

1) In recursive mode, it is possible to read 306 line 16 block in sequence by clock input only.

2) The data of 0 line is output from 0 block 64 clocks later after $VCLR_1$ clock.

NON-RECURSIVE MODE (READ)

1) **INITIAL CYCLE ($INC_1 = \overline{OE_1}$ = "L")**



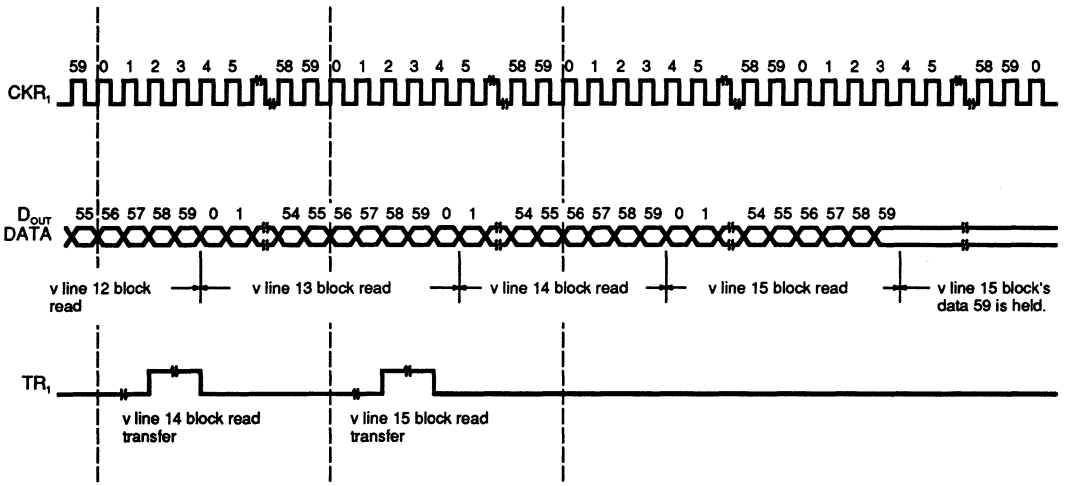
NOTE

1) In case that $HCLR_1$ is input at 60 x h + a (a = 0 to 59) clock from the previous $HCLR_1$ clock at the same time or after $VCLR_1$ clock, the last output data in v line h–1 block is held during a (a = 0 to 59) clocks. Then the data of 0 line is output from 0 block.
(The data of 0 line 0 block is output 64 clocks later after $HCLR_1$.)
However, it is necessary to input $VCLR_1$ between 60 x (h–1) + 1 and 60 x h + a clock from the previous $VCLR_1$.

2) Transfer cycle of 0 or v line h block is invalid.

NON-RECURSIVE MODE (READ)

2) **NORMAL CYCLE ($VCLR_1 = HCLR_1 = INC_1 = \overline{OE_1}$ = "L")**

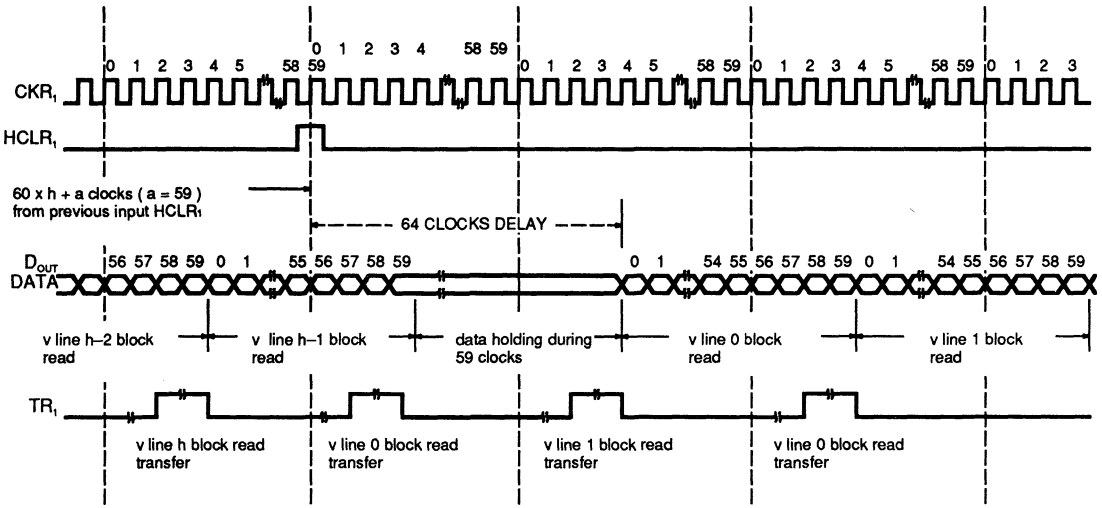


NOTE

1) In case that data is output till v line 15 block, the last output data of 15 block is held till new data is output by $HCLR_1$.

NON-RECURSIVE MODE (READ)

3) **FIRST BLOCK CYCLE ($HCLR_1 = INC_1 = \overline{OE}_1$ = "L")**



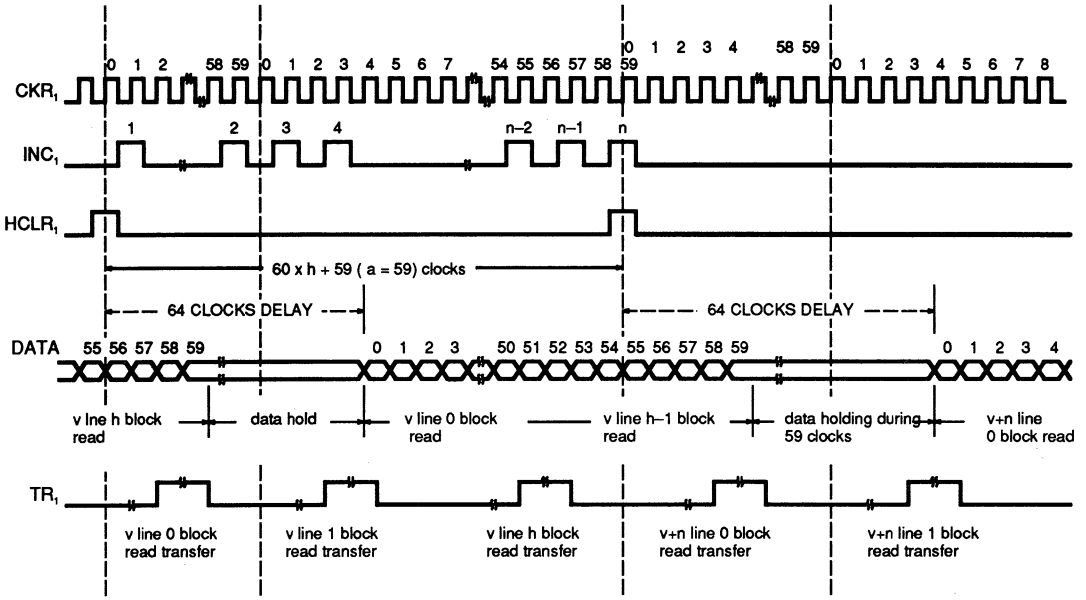
NOTE

1) In case that $HCLR_1$ is input at 60 x h + a (a = 0 to 59) clock from the previous $HCLR_1$ clock, the last output data of v line h–1 block is held during a (a = 0 to 59) clocks. Then the data of v line is output from 0 block.
(The data of v line 0 block is output 64 clock later after $HCLR_1$.)

2) Read transfer cycle of v line h block is invalid.

NON-RECURSIVE MODE (READ)

4) **LINE ADDRESS CYCLE (VCLR$_1$ = $\overline{OE}_1$ = "L")**



NOTE

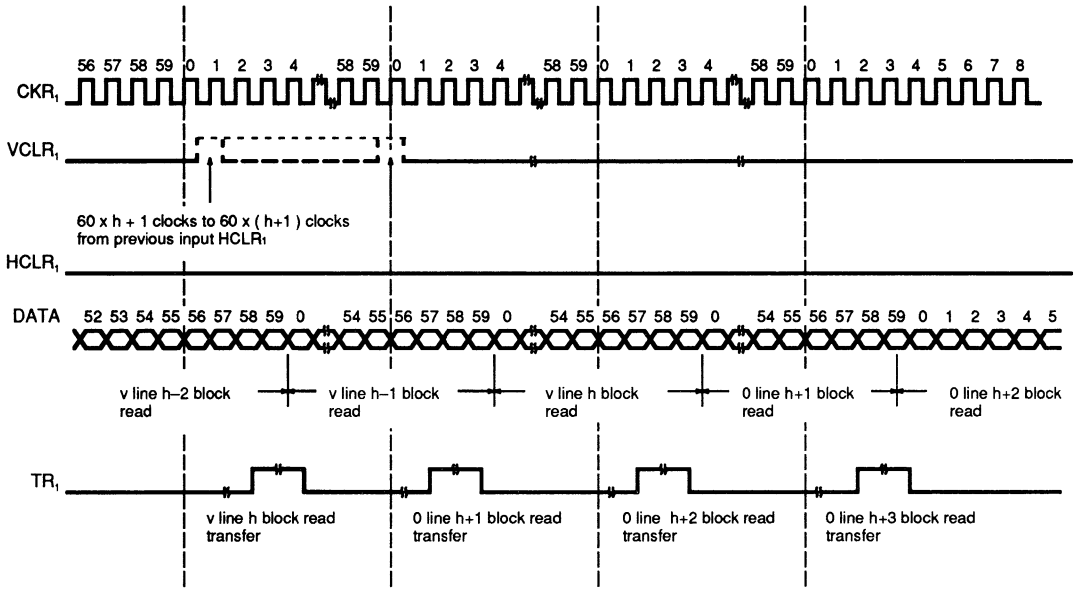
1) In case that INC$_1$ is input n times before HCLR$_1$ is input at 60 x h + a (a = 0 to 59) clock from the previous HCLR$_1$ clock, the last output data of v line h–1 block is held during a (a = 0 to 59) clocks. Then the data of v+n line is output from 0 block.
(The data of v+n line 0 block is output 64 clocks later after HCLR$_1$.)

2) The input INC$_1$ after HCLR$_1$ clock is invalid.

3) Read transfer cycle of v line h block is invalid.

NON-RECURSIVE MODE (READ)

5) $VCLR_1$ SPECIAL CYCLE No.1 ($INC_1 = \overline{OE_1}$ ="L")

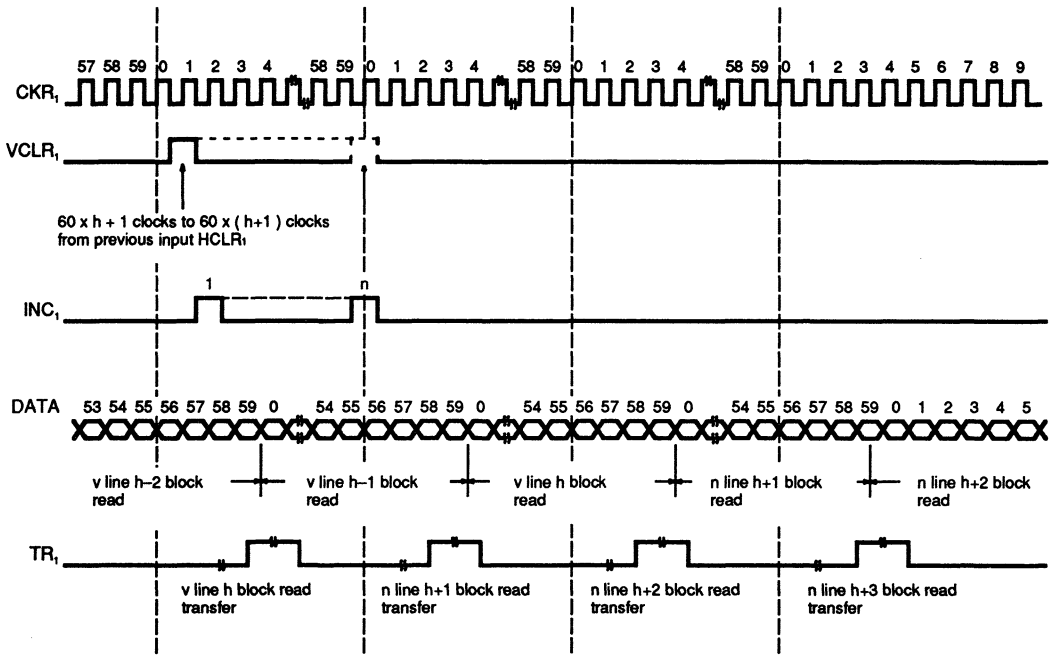


NOTE

1) In case that $VCLR_1$ is input between 60 x h + 1 clock and 60 x (h+1) clock from the previous $HCLR_1$ clock, line address is reset only after the data is output in v line h block. Then the data of 0 line is output continuously from h+1 block.

NON-RECURSIVE MODE (READ)

5) **VCLR$_1$ SPECIAL CYCLE No. 2 (HCLR$_1$ = $\overline{OE}_1$ = "L")**

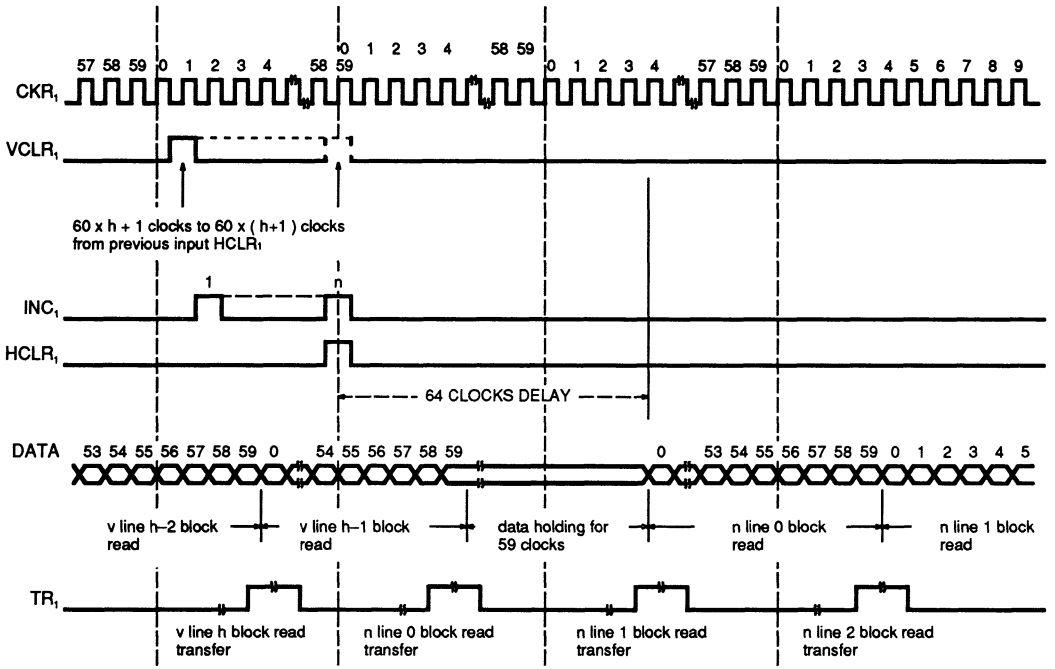


NOTE

1) In case that INC$_1$ is input n times after VCLR$_1$ is input between 60 x h + 1 clock and 60 x (h + 1) clock from the previous HCLR$_1$ clock, line address is reset only after the data of v line h bock is output. Then the data of n line is output continuously from h+1 block.

2) The input INC$_1$ at the same time with VCLR$_1$ clock is invalid.

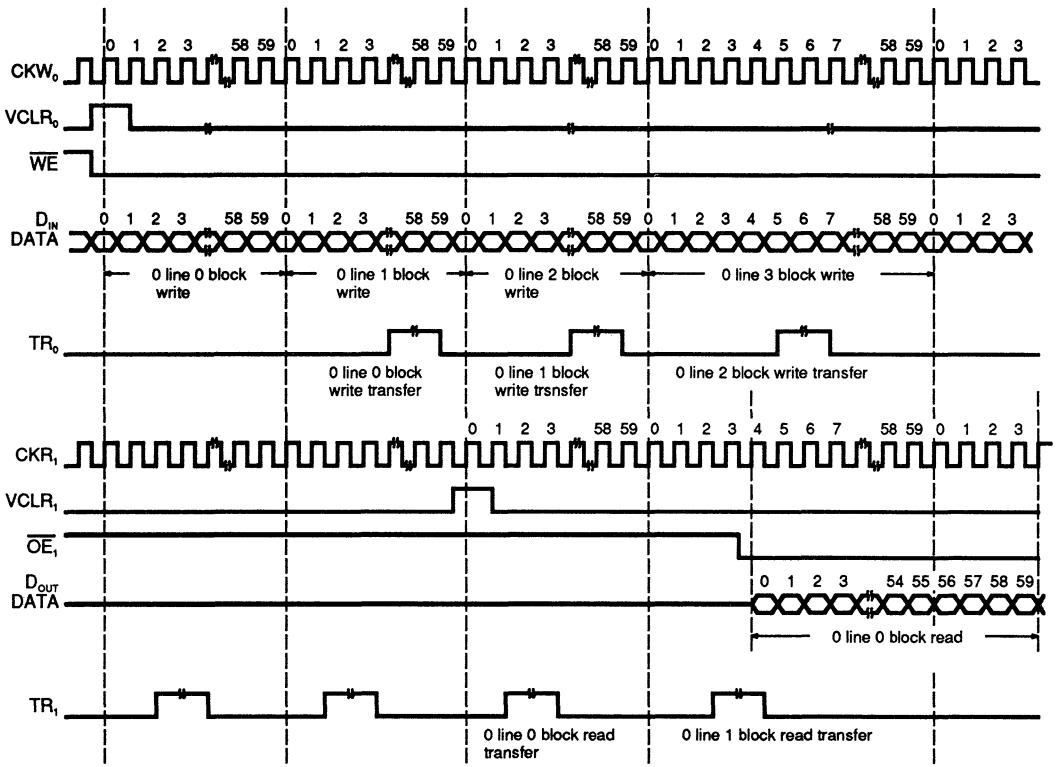
NON-RECURSIVE MODE (READ)
5) $VCLR_1$ SPECIAL CYCLE No. 3 ($\overline{OE}_1$ = "L")



NOTE
1) In case that INC_1 is input after INC_0 is input n times while $VCLR_1$ is input at 60 x h + a (a = 1 to 59) clock from the previous $HCLR_1$ clock, the last output data in v line h–1 block is held during a (a = 1 to 59) clocks. Then the data of n line is output from 0 block.
(The data of n line 0 block is output 64 clocks later after $HCLR_1$.)
2) The input INC_1 at the same time with $VCLR_1$ clock is invalid. And the input INC_1 at the same time or before $HCLR_1$ clock is valid.
3) Transfer cycle of V line h block is invalid.

RECURSIVE MODE (IN CASE OF NON-RECURSIVE MODE, VCLR = HCLR)

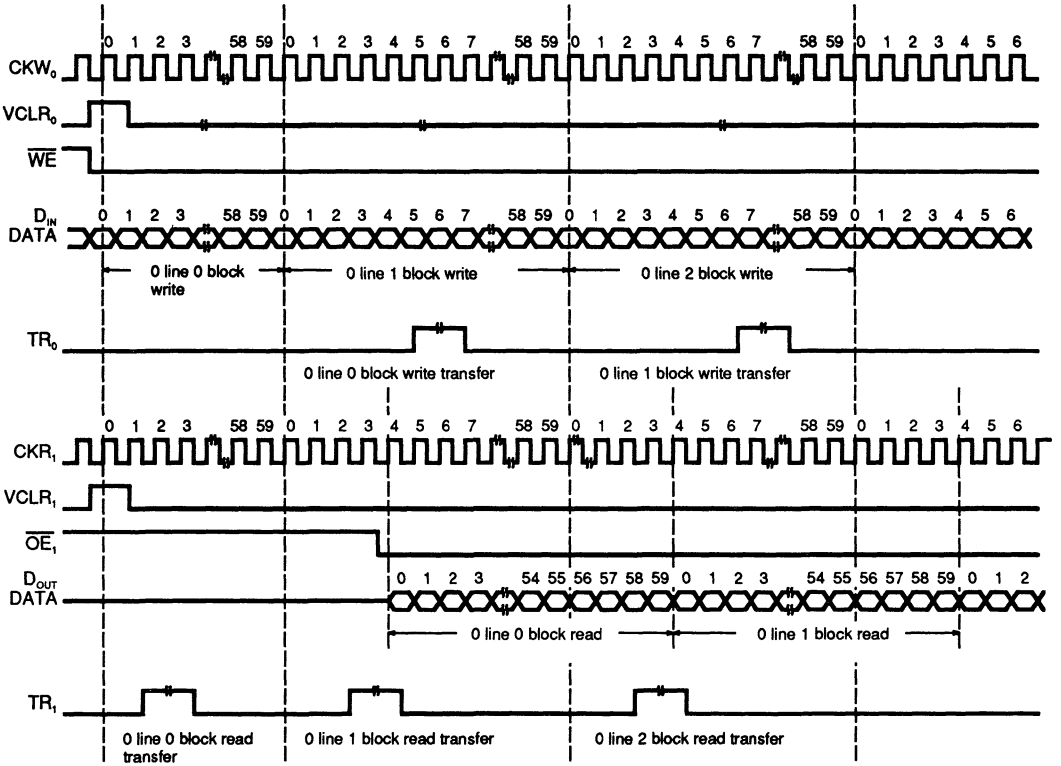
- **ACCESS MODE TO NEWLY INPUT DATA**



1) In order to get newly input data, it is necessary to get delay of $VCLR_1$ to $VCLR_0$ more than 120 clocks
(The delay of read data to write data is more than 184 clocks.)

RECURSIVE MODE (IN CASE OF NON-RECURSIVE MODE, VCLR = HCLR)

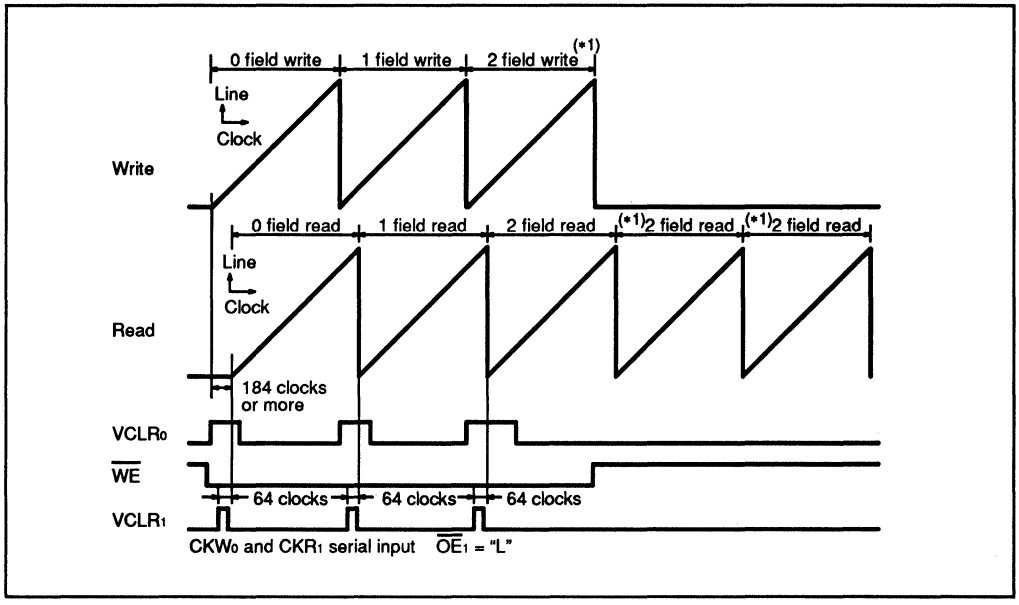
- **ACCESS MODE TO PREVIOUS DATA**



1) In order to get previous data, it is necessary to get delay of $VCLR_1$ to $VCLR_1$ less than 0 clock.
(The delay of read data to write data is less than 64 clocks.)
2) In case that the delay of $VCLR_1$ to $VCLR_1$ is more than 1 clock and less than 119 clocks, it is not sure wheter or not new data (previous data) is got.

APPLICATION EXAMPLE

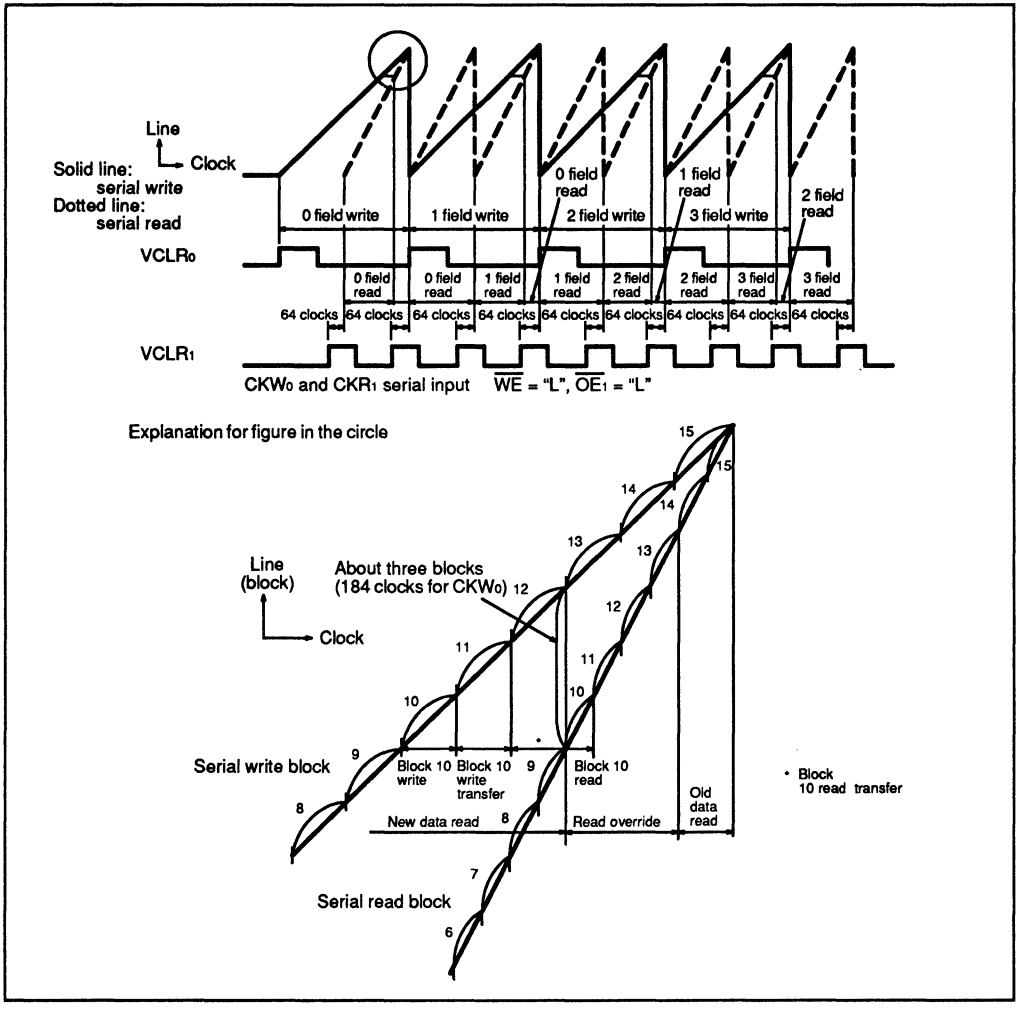
1. Delay line, field memory: In recursive mode



- If the cycle times of CKW_0 and CKR_1 are the same, asynchronous operation is also possible.
- If the cycle times of CKW_0 and CKR_1 are different, see application example 2, where read override may occur.
- In nonrecursive mode, lines must be advanced for each line with combinations of INC and HCLR input.

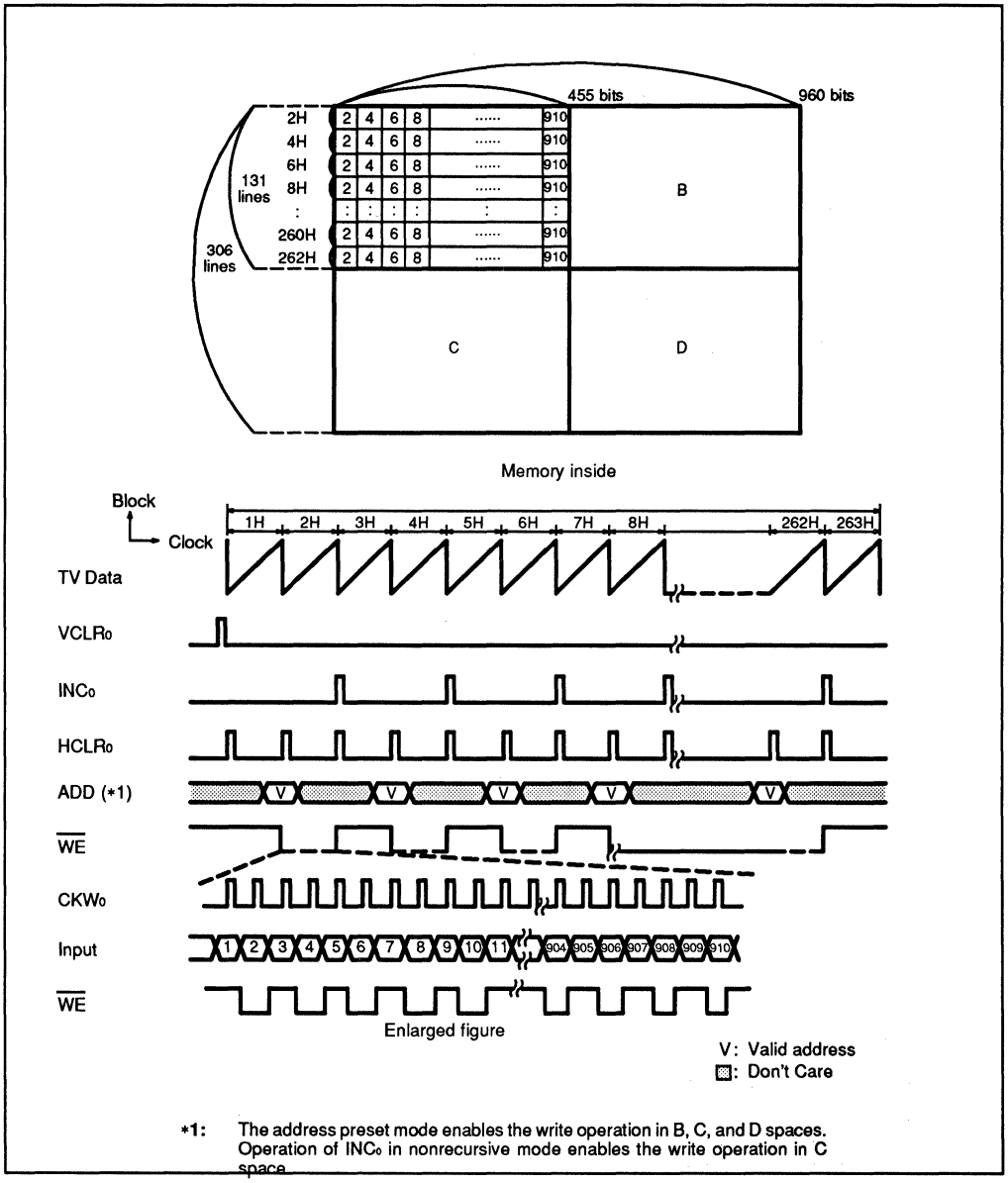
* 1 : When using 306 line/16 block/60 bits, the serial read operation is possible only through input of CKR1 and CKW0, even if VCLR1 is not input.

2. Double-speed conversion: In recursive mode



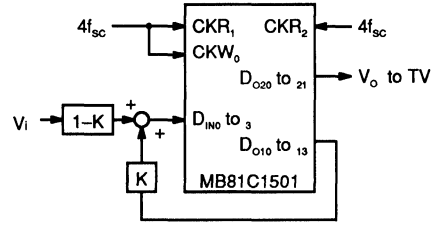
- **Read override**
  When block data written with double-speed conversion is read, the phase delay of the read operation versus the write operation requires about three write blocks (184 clocks for CKW).
- When two chips are used for the X8 configuration, if the two chips are operated independently, read override between the two chips may shift. Therefore, caution should be exercised. To synchronize read override between two chips, the synchronous transfer mode which sets one chip as a master chip and the other as a slave chip should be used.

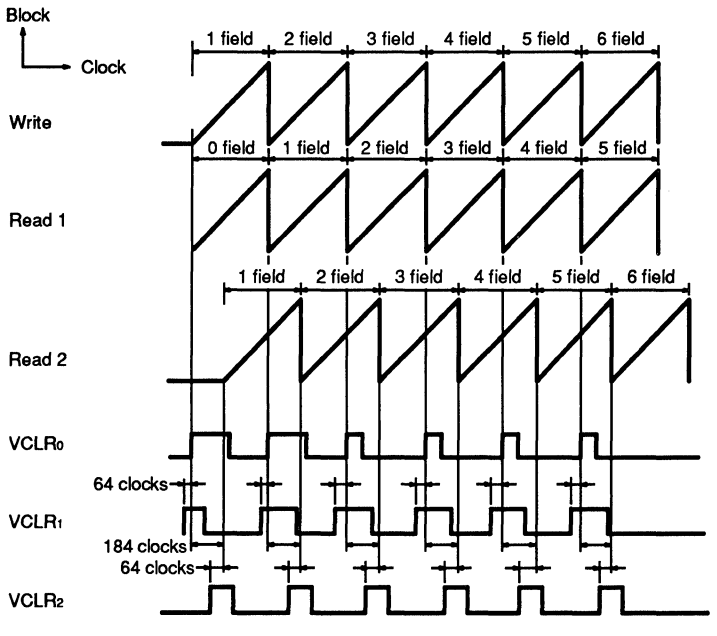
3. Write operation of 1/2 compressed data to memory:
   In nonrecursive mode, address preset mode



*1: The address preset mode enables the write operation in B, C, and D spaces. Operation of INC_0 in nonrecursive mode enables the write operation in C space.

4. Noise reduces between fields



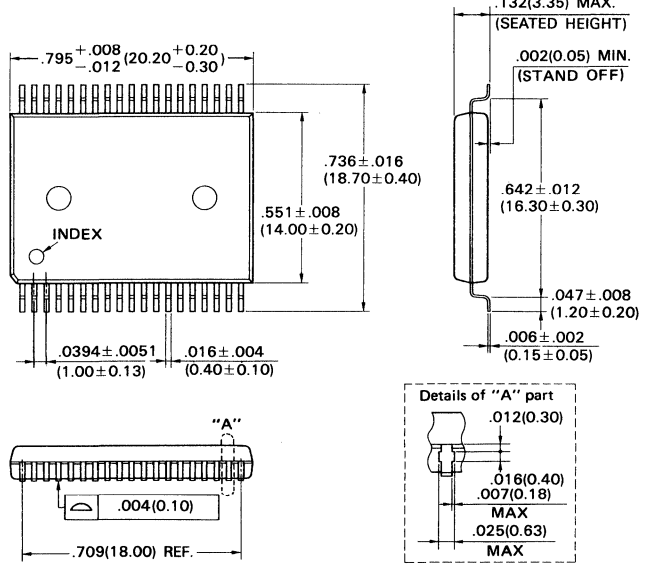


In the field memory (three ports) is used, stable output can be obtained, regardless of jitter from the write clock. In addition, the correlation between frames or lines can be calculated.

EXTERNAL DIMENSION

38-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-38P-M01)



3

Section 4

Quality and Reliability — *At a Glance*

4

Quality Control at Fujitsu

Built-In Quality and Reliability

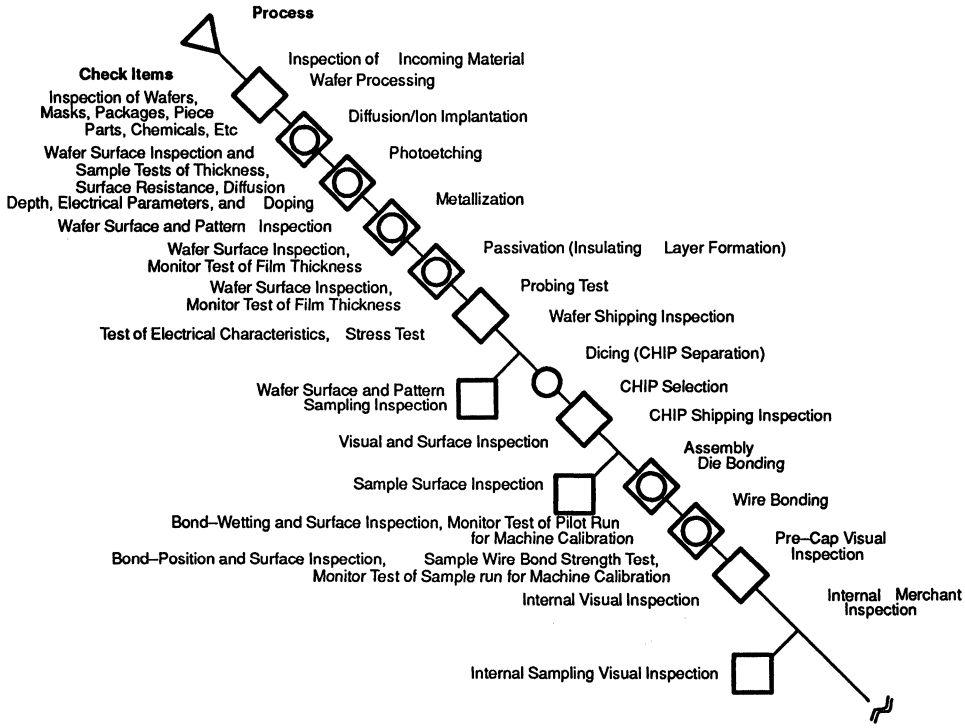
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

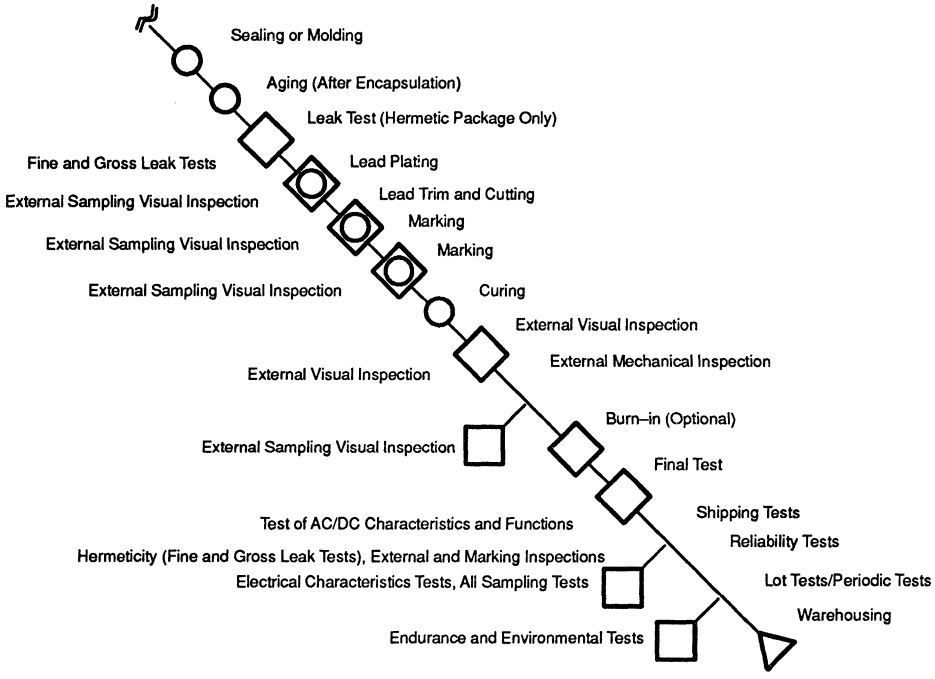
Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Processes at Fujitsu



Continued on next page

Quality Control Processes at Fujitsu (Continued)



Legend:

- Production Process
- Test/Inspection
- Production Process and Test/Inspection
- QC Gate (Sampling)

Note:
The flow sequence may vary slightly with individual product type.

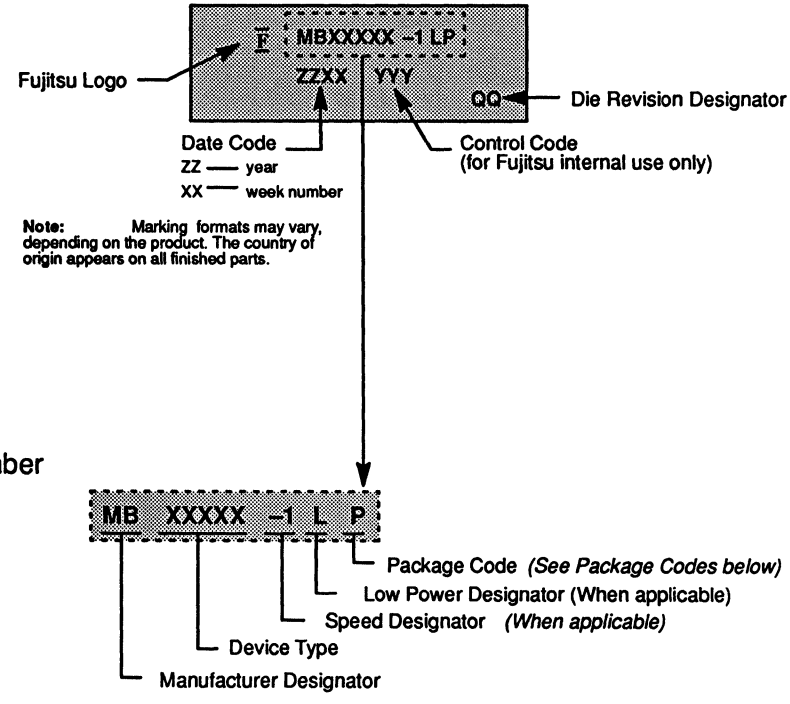
4

Section 5

Ordering Information — *At a Glance*

5

IC Package Marking



MB Identifies an IC designed and manufactured by Fujitsu with a Fujitsu-designated device number.

MBM Identifies an IC designed and manufactured by Fujitsu with a device number, designated by the industry, that is the industry standard number.

Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

5

IC Package Marking and Ordering Information

This ordering information is presented as a guide to Fujitsu's package options. The codes shown here indicate the current selections available for IC packaging. Since device packages are subject to changes and updating, you should contact your closest Fujitsu Sales Office or Representative for the latest package information.

Plastic Packages

Description	Type	Fujitsu Ordering Code[1,2,3]
Dual In-line Package, 600 mil Wide	DIP	P or M[3]
Dual In-line Package, 300 mil Wide	Skinny DIP	P-SK or P
Dual In-line Package, 400 mil Wide	Slim DIP	P-SL or P
Dual In-line Package, 70 mil Lead Pitch	Shrink DIP	P-SH or P
Flatpack, 0.5 mm Lead Pitch	SSOP or SQFP	PFV
Leaded Chip Carrier	PLCC	PD or PV
Pin Grid Array Package	PGA	PR
Quad Flatpack	QFP	PFQ or PF
Single In-line Package	SIP	PS
Small Outline J-Leads	SOJ	PJ or PJN
Small Outline Package	SOP	PF or PNF
Thin Small Outline (with Normal Bend Leads) Package	TSOP	PFTN
Thin Small Outline (with Reverse Bend Leads) Package	TSOP	PFTR
Zig-zag In-line Package	ZIP	PSZ

[1]Package ordering code appears as a suffix to Fujitsu's part number and speed designator (MBXXXXX–XXPKG).
[2]Package codes in the U.S.A do not use the "–"; e.g., PSK is the same as P–SK.
[3]M is used on bipolar devices only.

Continued on next page

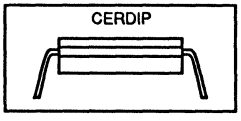
5

IC Package Marking and Ordering Information (Continued)

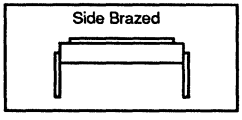
Ceramic Packages		
Description	**Type**	**Fujitsu Ordering Code[1,2]**
Dual In-line Package with CERDIP[3]	CERDIP	Z
Dual In-line Package with Glass Frit Seal	DIP	T
Dual In-line Package with Metal Seal (Side Brazed[4])	DIP	C
Dual In-line Package, 400 mil Wide	Slim DIP	Z-SL or Z T-SL or T C-SL or C
Dual In-line Package, 300 mil Wide	Skinny DIP	Z-SK or Z T-SK or T C-SK or C
Dual In-line Package, 1.778 mm Lead Pitch	Shrink DIP	Z-SH or Z T-SH or T C-SH or C
Flat Package with CERPACK	CERPACK	ZF
Flat Package with Glass Frit Seal	FPT	TF
Flat Package with Metal Seal	FPT	CF
Leadless Chip Carrier with Glass Frit Seal	LCC	TV
Leadless Chip Carrier with Metal Seal	LCC	CV
Pin Grid Array	PGA	CR
Quad Flat J-lead Package with CERPACK	QFJ	ZJ
Quad Flat, Gullwing Lead, Package with CERPACK	QFP	ZFL or ZF
Quad Flat, Gullwing Lead, Package with Metal Seal	QFP	CFL or CF
Small Outline, Gullwing Lead, Package with CERPACK	SOP	ZFL or ZF
Small Outline, Gullwing Lead, Package with Metal Seal	SOP	CFL or CF
Small Outline J-lead Package with Metal Seal	SOJ	CJ

[1]Package ordering code appears as a suffix to Fujitsu's part number and speed designator (MBXXXXX–XXPKG)
[2]Package codes in the U.S.A do not use the "–"; e.g., ZSK is the same as Z–SK.

3 CERDIP



4 Side Brazed



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5

Section 6

Sales Information — *At a Glance*

6

Introduction to Fujitsu

Fujitsu Limited (Japan)

Fujitsu Limited was founded as a telecommunications equipment manufacturer in 1935, and today is not only one of Japan's leading telecommunications companies, but also one of the world's largest computer manufacturers.

This leadership has resulted, at least in part, from the superb quality of the company's semiconductors and electronic components. Manufactured by the company's Electronics Devices Operations Group, these vital electronic devices also contribute to the high reliability and performance of products made by many other manufacturers around the world.

Today, Fujitsu is one of the world's top manufacturers of semiconductors and electronic components. In Japan, Fujitsu's R&D laboratories for semiconductor and electronic components are situated in Kawasaki and Mie, and manufacturing works are located in Iwate, Aizu, Wakamatsu and Suzaka. Fujitsu also has six affiliated manufacturing works in the country. Overseas facilities in the U.S, Europe, and Asia also help to meet the growing global demand for Fujitsu semiconductors and electronic components.

Fujitsu enforces strict quality control at all stages of production, from materials selection through manufacturing to final testing. As a result, Fujitsu's electronic devices are known for their extremely high reliability and excellent cost-to-performance ratio.

Fujitsu manufactures a full line of semiconductors and electronic components to meet the diverse applications of a wide variety of customers. Backed by Fujitsu's extensive R&D commitment equal to over 10 percent of annual sales, Fujitsu's electronic devices stay on the cutting edge of electronics technology.

Continued on next page

Introduction to Fujitsu

Fujitsu Microelectronics, Inc. (U.S.A.)

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers throughout North and South America.

The Advanced Products Division (APD) is responsible for designing and selling a full line of SPARC processors and peripheral chips. APD also sells the EtherStar™ LAN controller that was designed by APD. It is the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs FETs and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD) which markets the following standard devices, components, and ASICs.

Memory Products	DRAMs EPROMs EEPROMs NOVRAMs CMOS masked ROMs CMOS SRAMs BiCMOS SRAMs Bipolar PROMs ECL RAMs STRAMs (self-timed RAM) Hi-Rel PROMs and SRAMs Memory cards Memory modules
Telecommunication Products	PLLs Prescalers Piezoelectric devices CODECs VCOs Telephone ICs Modems

Continued on next page

Introduction to Fujitsu

Microprocessor Products	4-bit microcontrollers DSPs
Logic Products	Ultra high-speed ECL/ECL TTL translator circuits
Analog Products	Linear ICs Transistors
Hybrid Products	Thick- and Thin-film Custom modules Stepper motor drivers
Special Purpose Controller Products	SCSI controllers Serial protocol controllers Video controllers (TV text, CRT, and picture-in-picture)
ASIC Products	CMOS gate arrays ECL gate arrays BiCMOS gate arrays GaAs gate arrays CMOS standard cells ASIC Gallery™ (SuperMacros™, Compiled Cells) ASICOpen™ CAD Software Framework (ViewCAD™, a design and verification tool that integrates with third-party CAD tools) Third-party EWS (engineering workstation) support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division (SMD) assembles and tests memory devices. The Gresham Manufacturing Division (GMD) began manufacturing in 1988.GMD fabricates wafers, and produces ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Component of America**, markets connectors, keyboards, thermal printers, plasma displays, and relays.

Continued on next page

Introduction to Fujitsu

Fujitsu Electronic Devices Europe:

Fujitsu Mikroelektronik GmbH (FMG), West Germany
Fujitsu Microelectronics Limited (FML), U.K.
Fujitsu Microelectronics Italia S.R.L (FMIL), Italy
Fujitsu Microelectronics Ireland, Ltd. (FME), Ireland

Fujitsu Mikroelektronik GmbH (FMG) was established in June 1980 in Frankfurt, West Germany, as Fujitsu's European headquarters and is a totally owned subsidiary of Fujitsu Limited, Tokyo. Fujitsu Microelectronics Limited (FML) is a sister company based in Maidenhead, England and dedicated to serving the U.K., Ireland, and Scandanavia. Fujitsu Microelectronics Italia (FMIL) is based in Milan, Italy and serves Italy, Spain, Portugal, and the rest of Southern Europe. Together, FMG, FML, and FMIL supply the European market with a full range of semiconductors and electronic components. Sales offices are located in Munich, Frankfurt, Stuttgart, Paris, Eindhoven, Milan, Maidenhead, and Stockholm.

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in Dublin, Ireland, as Fujitsu's European Assembly Center for integrated circuits. FME produces DRAMs, EPROMs, and other LSI memory products.

Fujitsu has two European VLSI design centers, both in the U.K. The Manchester Design Center, in operation since 1983, is equipped with two mainframe computers and is linked by satellite to production plants in Japan and the U.S. Staffed with a team of experienced engineers, the center is involved in the design of VLSI standard products, SuperMacros, CAD tools and ASICs. A second design center was set up in London in 1990 for designing telecommunication ICs. Additionally, Fujitsu offers a network of 17 ASIC design centers in eight European countries.

Fujitsu has further demonstrated its commitment to the European market by commencing construction of a full wafer fabrication plant in Durham in the North of England. The new plant is due to start production of 4 megabyte DRAMs and ASICs in 1991.

Continued on next page

Introduction to Fujitsu

The range of semiconductor products offered by FMG, FML, and FMIL for the European market includes:

Memory Products	DRAMs SRAMs EPROMs EEPROMs Mask ROMs Bipolar PROMs Video RAMs ECL RAMs Memory modules Memory cards
ASIC Products	CMOS gate arrays BiCMOS gate arrays Bipolar (ECL) gate arrays Gallium Arsenide gate arrays CMOS standard cells ECL gate masterslice devices Wide range of ASIC design software
Microprocessor Products	4-Bit Microcontrollers 4- 8- and 16-bit F^2MC^{TM} flexible Microcontrollers 32-Bit SPARC™ RISC microprocessors 32-Bit GMICRO™ TRON-based CISC microprocessors
Telecommunication Products	Prescalers PLLs CODECs LAN devices DSPs ISDN products SCSI and LAN devices ISDN products Telecom devices for the GSM Pan-European digital cellular telephone system.
Analog Products	OP Amps Comparators A/D and D/A Converters Application Specific ICs

The range of electronic components offered by FMG, FML, and FMIL incudes relays, connectors, keyboards, thermal printers, plasma displays, liquid crystal displays, hybrid ICs, and piezoelectric devices.

Continued on next page

Introduction to Fujitsu

Fujitsu Microelectronics Asia PTE Ltd. (Singapore)

Fujitsu Microelectronics Asia PTE Ltd. (FMAP) opened in August 1986, in Hong Kong, as a wholly-owned Fujitsu subsidiary for sales of electronic devices to the Asian, Australian, and Southwest Pacific markets. In 1990, FMAP moved to a new location in Singapore.

FMAP offers memory, ASIC, microprocessor, and telecommunication products along with Fujitsu's wide range of electronic components.

Integrated Circuits Corporate Headquarters — Worldwide

International Corporate Headquarters

FUJITSU LIMITED
Marunouchi Headquarters
6–1, Marunouchi 1–chome
Chiyoda–ku, Tokyo 100
Japan
Tel: (03) 216-3211
Telex: 781–22833
FAX: (03) 213-7174

For integrated circuits marketing information please contact the following:

Headquarters for Japan

FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
6–1, Marunouchi 2–chome
Chiyoda–ku, Tokyo 100
Japan
Tel: (03) 216-3211
Telex: 781–2224361
FAX: (03) 211-3987

Headquarters for North and South America

FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street
San Jose, CA 95134–1804
USA
Tel: (408) 922–9000
Telex: 910–338–0190
FAX: (408) 432–9044

Headquarters for Europe

FUJITSU MIKROELEKTRONIK GmbH
Lyoner Strasse 44–48
Arabella Centre 9. OG
6000 Frankfurt 71
Federal Republic of Germany
Tel: (69) 66320
Telex: 411963
FAX: (69) 6632122

Headquarters for Asia, Australia and Oceania

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
06-04/-07 Plaza By The Park
No. 51 Bras Basah Road
Singapore 0718
Tel: (65) 336–1600
Telex: RS 55573 FESPL
FAX: (65) 336–1609

Fujitsu Microelectronics, Inc. (FMI) Sales Offices for North and South America

NORTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
10600 N. De Anza Blvd.
Suite 225
Cupertino, CA 95014
Tel: (408) 996–1600
FAX: (408) 725–8746

SOUTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
Century Centre
2603 Main Street
Suite 510
Irvine, CA 92714
Tel: (714) 724–8777
FAX: (714) 724–8778

COLORADO (Denver)

Fujitsu Microelectronics, Inc.
5445 DTC Parkway
Suite 300
Englewood, CO 80111
Tel: (303) 740–8880
FAX: (303) 740–8988

GEORGIA (Atlanta)

Fujitsu Microelectronics, Inc.
3500 Parkway Lane
Suite 210
Norcross, GA 30092
Tel: (404) 449–8539
FAX: (404) 441–2016

ILLINOIS (Chicago)

Fujitsu Microelectronics, Inc.
One Pierce Place
Suite 910
Itasca, IL 60143–2681
Tel: (708) 250–8580
FAX: (708) 250–8591

MASSACHUSETTS (Boston)

Fujitsu Microelectronics, Inc.
75 Wells Avenue
Suite 5
Newton Center, MA 02159–3251
Tel: (617) 964–7080
FAX: (617) 964–3301

MINNESOTA (Minneapolis)

Fujitsu Microelectronics, Inc.
3460 Washington Drive
Suite 209
Eagan, MN 55122–1303
Tel: (612) 454–0323
FAX: (612) 454–0601

NEW JERSEY (Cherry Hill)

Fujitsu Microelectronics, Inc.
Horizon Corporate Center
3000 Atrium Way
Suite 100
Mt. Laurel, NJ 08054
Tel: (609) 727–9700
FAX: (609) 727–9797

NEW YORK (Long Island)

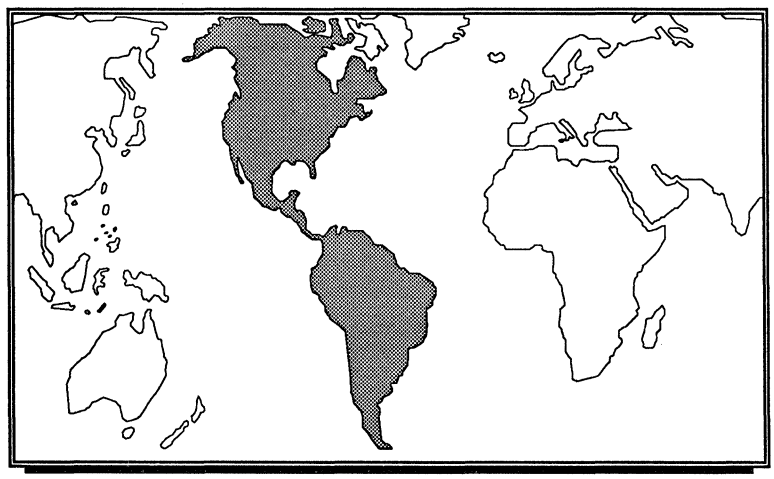
Fujitsu Microelectronics, Inc.
898 Veterans Memorial Highway
Bldg. 2, Suite 310
Hauppauge, NY 11788
Tel: (516) 582–8700
FAX: (516) 582–3855

OREGON (Portland)

Fujitsu Microelectronics, Inc.
15220 NW Greenbrier Pkwy.
Suite 360
Beaverton, OR 97006
Tel: (503) 690–1909
FAX: (503) 690–8074

TEXAS (Dallas)

Fujitsu Microelectronics, Inc.
14785 Preston Road
Suite 670
Dallas, TX 75240
Tel: (214) 233–9394
FAX: (214) 386–7917



FMI Representatives — USA

For product information, contact your nearest Representative.

Alabama

CSR Electronics
303 Williams Avenue
Suite 931
Huntsville, AL 35801
Tel: (205) 533–2444
FAX: (205) 536–4031

Arizona

Aztech Component Sales Inc.
15230 N 75th Street
Suite 1031
Scottsdale, AZ 85260
Tel: (602) 991–6300
FAX: (602) 991–0563

California

Harvey King, Inc.
6393 Nancy Ridge Drive
San Diego, CA 92121
Tel: (619) 587–9300
FAX: (619) 587–0507

Infinity Sales, Inc.
4500 Campus Drive
Suite 300
Newport Beach, CA 92660
Tel: (714) 833–0300
FAX: (714) 833–0303

Norcomp
3350 Scott Blvd.,
Suite 24
Santa Clara, CA 95054
Tel: (408) 727–7707
FAX: (408) 986–1947

Norcomp
2140 Professional Drive
Suite 200
Roseville, CA 95661
Tel: (916) 782–8070
FAX: (916) 782–8073

Sonika Electronica of America
2240 Main Street
Suite 19
Chula Vista, CA 92011
Tel: (619) 424–9190
FAX: (619) 424–9191

Colorado

Talisman Assoc.
6860 S. Yosemite Court
Suite 2143
Englewood, CO 80112
Tel: (303) 773–2533
FAX: (303) 796–0545

Connecticut

Conntech Sales, Inc.
605 Washington Avenue
Suite 33
New Haven, CT 06473
Tel: (203) 234–0577
FAX: (203) 234–0576

Florida

Semtronic Associates, Inc.
657 Maitland Avenue
Altamonte Springs, FL 32701
Tel: (407) 831–8233
FAX: (407) 831–2844

Semtronic Associates, Inc.
1467 S. Missouri Avenue
Clearwater, FL 33516
Tel: (813) 461–4675
FAX: (813) 442–2234

Semtronic Associates, Inc.
3471 NW 55th Street
Ft. Lauderdale, FL 33309
Tel: (305) 731–2484
FAX: (305) 731–1019

Georgia

CSR Electronics
1651 Mt. Vernon Road
Suite 200
Tel: (404) 396–3720
FAX: (404) 394–8387

Idaho

Intermountain Technical Marketing
1406 E. First Street
Suite 101
Meridan, ID 83642
Tel: (208) 888–6071
FAX: (208) 888 6074

Illinois

Beta Technology
1009 Hawthorne Drive
Itasca, IL 60143
Tel: (708) 256–9586
FAX: (708) 256–9592

Indiana

Fred Dorsey & Associates
3518 Eden Place
Carmel, IN 46032
Tel: (317) 844–4842
FAX: (317) 844–4843

Iowa

Electromec Sales
Executive Plaza
4403 First Avenue, S.E.
Suite 302
Cedar Rapids, IA 52402
Tel: (319) 393–1637
FAX: (319) 393–1752

Kansas

Rothkopf & Associates, Inc.
1948 E. Santa Fe
Suite H
Olathe, KS 66062
Tel: (913) 829–8897
FAX: (913) 829–1664

Kentucky

Spectro-Com
303 UHL Road
Melbourne, KY 41059
Tel: (606) 781–3904

Maryland

Arbotek Associates
1404 E. Joppa Road
Towson, MD 21204
Tel: (301) 825–0775
FAX: (301) 337–2781

Massachusetts

Mill–Bern Associates
2 Mack Road
Woburn, MA 01801
Tel: (617) 932–3311
FAX: (617) 932–0511

FMI Representatives — USA (Continued)

Michigan

Greiner Associates, Inc.
15324 E. Jefferson Avenue
Suite 12
Grosse Point Park, MI 48230
Tel: (313) 499–0188
FAX: (313) 499–0665

Minnesota

Electromec Sales
1601 E. Highway 13
Suite 200
Burnsville, MN 55337
Tel: (612) 894–8200
FAX: (612) 894–9352

Missouri

Rothkopf & Associates, Inc.
8721 Manchester Road
St. Louis, MO 63144
Tel: (314) 961–4485
FAX: (314) 961–4736

New Jersey

BGR Associates
Evesham Commons
525 Route 73
Suite 100
Marlton, NJ 08053
Tel: (609) 983–1020
FAX: (609) 983–1879

Technical Applications & Marketing
91 Clinton Road
Suite 1D
Fairfield, NJ 07006
Tel: (201) 575–4130
FAX: (201) 575–4563

New York

Quality Components
3343 Harlem Road
Buffalo, NY 14225
Tel: (716) 837–5430
FAX: (716) 837–0662

Quality Components
116 Fayette Street
Manlius, NY 13104
Tel: (315) 682–8885
FAX: (315) 682–2277

Quality Components
2318 Titus Ave.
Rochester, NY 14622
Tel: (716) 342–7229
FAX: (716) 342–7227

North Carolina

CSR Electronics
8020 Crockett Court
Mathews, NC 28226
Tel: (704) 847–7878
FAX: (704) 847–0056

CSR Electronics
5848 Farington Place
Suite 2
Raleigh, NC 27609
Tel: (919) 878–9200
FAX: (919 878–9117

Oregon

L–Squared Limited
15234 NW Greenbrier Pkwy
Beaverton, OR 97006
Tel: (503) 629–8555
FAX: (503) 645–6196

Tennessee

CSR Electronics
3133 Curtis Lane
Knoxville, TN 37918
Tel: (615) 698–7511
FAX: (615) 698–7932

Texas

Technical Marketing, Inc.
3320 Wiley Post Road
Carrollton, TX 75006
Tel: (214) 387–3601
FAX: (214) 387–3605

Technical Marketing, Inc.
2901 Wilcrest Drive
Suite 139
Houston, TX 77042
Tel: (713) 783–4497
FAX: (713) 783–5307

Technical Marketing, Inc.
1315 Sam Bass Circle
Suite B–3
Round Rock, TX 78681
Tel: (512) 244–2291
FAX: (512) 338–1596

Utah

R–Squared Marketing
340 W. 500 South
Suite 105
Salt Lake City, UT 84101
Tel: (801) 595–0631
FAX: (801) 595–0435

Washington

L–Squared Limited
105 Central Way
Suite 203
Kirkland, WA 98033
Tel: (206) 827–8555
FAX: (206) 828–6102

Wisconsin

Beta Technology
9401 W Beloit Street
Suite 304C
Milwaukee, WI 53227
Tel: (414) 543–6609
FAX: (414) 543–9288

FMI Representatives — Canada, Mexico and Puerto Rico

Canada

Pipe-Thompson Limited
5468 Dundas Street W.
Suite 206
Islington, Ontario M9B 6E3
Tel: (416) 236–2355
FAX: (416) 236–3387

Pipe-Thompson Limited
17 Brandy Creek Crescent
Kandata, Ontario K2M 2B8
Tel: (613) 591–1821
FAX: (613) 591–0461

Mexico

Solano Electronica (Sonika)
Ermita 1039-10
Colonia Chapalita
Guadalajara, JAL. 45042
Tel: (52) 3647–4250
FAX: (52) 3647–3433

Solano Electronics, S.A. De C.V.
Cienfuego #651–A
07300 Mexico City, D.F.
FAX: (52) 5586–8443

Puerto Rico

Semtronic Associates
Mercantil Plaza Building
Suite 816
Hato Rey, Puerto Rico 00918
Tel: (809) 766–0700

FMI Distributors — USA

Alabama

Marshall Industries
3313 S. Memorial Highway
Suite 150
Huntsville, AL 35801
(205) 881–9235

Repton Electronics
4950 Corporate Drive
Suite 105C
Huntsville, AL 35805
(205) 722–9565

Arizona

Insight Electronics
1515 W. University Drive
Suite 103
Tempe, AZ 85281
(602) 829–1800

Marshall Industries
9830 S. 51st Street
Suite B121
Phoenix, AZ 85044
(602) 496–0290

California

Bell Microproducts
18350 Mt. Langley
Suite 207
Fountain Valley, CA 92708
(714) 963–0667

Bell Microproducts
550 Sycamore Drive
Milpitas, CA 95035
(408) 434–1150

Insight Electronics
28035 Dorothy Drive
Suite 2
Agoura, CA 91301
(818) 707–2100

Insight Electronics
15635 Alton Parkway
Suite 120
Irvine, CA 92718
(714) 727–2111

Insight Electronics
6885 Flanders Drive
Suite C
San Diego, CA 92126
(619) 587–9757

Marshall Industries
9710 Desoto Ave.
Chatsworth, CA 91311
(818) 407–4100

Marshall Industries
9320 Telstar Ave.
El Monte, CA 91731
(818) 307–6094

Marshall Industries
One Morgan
Irvine, CA 92718
(714) 458–5308

Marshall Industries
336 Los Coches Street
Milpitas, CA 95035
(408) 942–4600

Marshall Industries
3039 Kilgore Ave.
Suite 140
Rancho Cordova, CA 95670
(916) 635–9700

Marshall Industries
10105 Carroll Canyon Road
San Diego, CA 92131
(619) 578–9600

Merit Electronics
2070 Ringwood Avenue
San Jose, CA 95131
(408) 434–0800

Micro Gensis, Inc.
2880 Lakeside Drive
Suite 101
Santa Clara, CA 95054
(408) 727–5050

Milgray Electronics
912 Pancho Road
Suite C
Camarillo, CA 93010
(805) 484–4055

Milgray Electronics
16 Technology Drive
Irvine, CA 92718
(714) 753–1282

Western Microtechnology
28720 Roadside Dr.
Suite 175
Agoura Hills, CA 91301
(818) 356–0180

Western Microtechnology
1637 North Brian
Orange, CA 92667
(714) 637–0200

Western Microtechnology
6837 Nancy Ridge Drive
San Diego, CA 92121
(619) 453–8430

Western Microtechnology
12900 Saratoga Ave.
Saratoga, CA 95070
(408) 725–1660

Colorado

Marshall Industries
12351 N. Grant Road
Suite A
Thornton, CO 80241
(303) 451–8383

Connecticut

Marshall Industries
20 Sterling Drive
Wallingford, CT 06492
(203) 265–3822

Milgray Electronics
326 W. Main Street
Milford, CT 06460
(203) 878–5538

Florida

Marshall Industries
380 S. Northlake Blvd
Suite 1024
Altamonte Springs, FL 32701
(407) 767–8585

Marshall Industries
2700 W. Cypress Creek Rd.
Suite D 114
Ft. Lauderdale, FL 33309
(305) 977–4880

Marshall Industries
2840 Sherer Drive
St. Petersburg, FL 33716
(813) 573–1399

Milgray Electronics
1850 Lee Road
Suite 104
Winter Park, FL 32789
(407) 647–5747

Reptron Electronics
3320 N.W. 53rd Street
Suite 206
Ft. Lauderdale, FL 33309
(305) 735–1112

Reptron Electronics
14501 McCormick Drive
Tampa, FL 33626
(813) 855–4656

FMI Distributors — USA (Continued)

Georgia

Marshall Industries
5300 Oakbrook Pkwy
Suite 140
Norcross, GA 30093
(404) 923–5750

Milgray Electronics
3000 Northwoods Parkway
Suite 270
Norcross, GA 30071
(404) 446–9777

Reptron Electronics
3040 H Business Park Drive
Norcross, GA 30071
(404) 446–1300

Illinois

Classic Components
3336 Commercial Ave.
Northbrook, IL 60062
(312) 272–9650

Marshall Industries
50 E. Commerce Dr.
Suite I
Schaumburg, IL 60173
(312) 490–0155

Milgray Electronics
1530 E. Dundee Road
Suite 310
Palatine, IL 60067
(708) 202–1900

Reptron Electronics
1000 E. State Hwy
Suite K
Schaumburg, IL 60173
(312) 882–1700

Indiana

Marshall Industries
6990 Corporate Drive
Indianapolis, IN 46278
(317) 297–0483

Kansas

Marshall Industries
10413 W. 84th Terrace
Lenexa, KS 66214
(913) 492–3121

Milgray Electronics
6400 Glenwood
Suite 313
Overland Park, KS 66202
(913) 236–8800

Maryland

Marshall Industries
2221 Broadbirch
Suite G
Silver Springs, MD 20910
(301) 622–1118

Milgray Electronics
9801 Broken Land Parkway
Columbia, MD 21045
(301) 995–6169

Vantage Components, Inc.
6925-R Oakland Mills Road
Columbia, MD 21045
(301) 720–5100

Massachusetts

Bell Microproducts
16 Upton Drive
Wilmington, MA 01887
(508) 658–0222

Interface Electronic Corp.
228 South Street
Hopkinton, MA 01748
(508) 435–6858

Marshall Industries
33 Upton Drive
Wilmington, MA 01887
(508) 658–0810

Milgray Electronics
187 Ballardvale Street
Wilmington, MA 01887
(508) 657–5900

Vantage Components, Inc.
200 Bulfinch Drive
Andover, MA 01810
(508) 687-3900

Western Microtechnology
20 Blanchard Road
9 Corporate Place
Burlington, MA 01803
(617) 273–2800

Michigan

Marshall Industries
31067 Schoolcraft Road
Livonia, MI 48150
(313) 525–5850

Reptron Electronics
34403 Glendale
Livonia, MI 48150
(313) 525–2700

Minnesota

Marshall Industries
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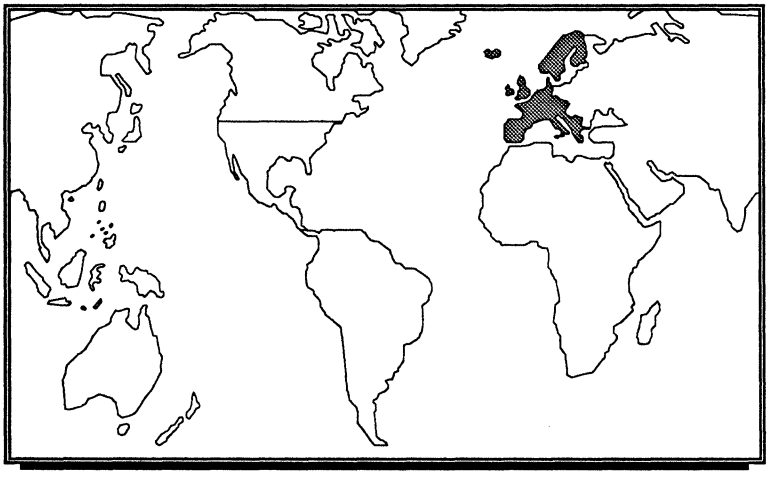

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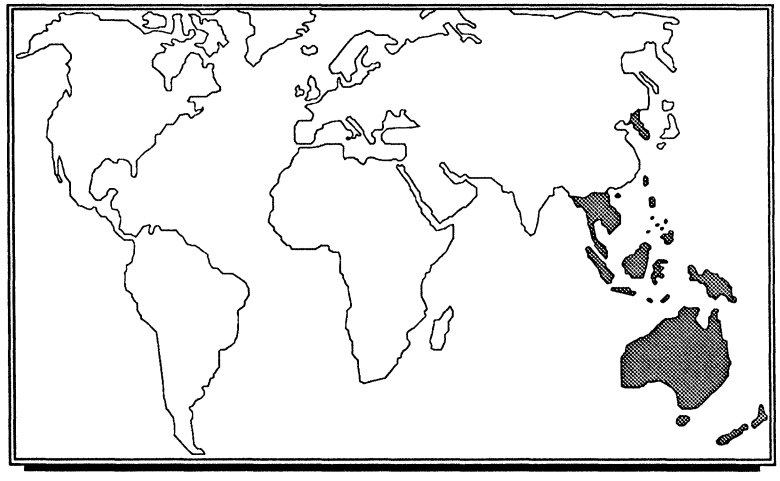

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Section 7

Design Information — *At a Glance*

7

Appendix 1

Application Note

November 1989
Edition 1.1

FUJITSU

APPLICATION NOTE

Dynamic RAMs

Various Features of Fujitsu DRAMs

Applications Engineering Department
Fujitsu Microelectronics, Inc.
Integrated Circuits Division

Abstract

DRAMs are not only becoming denser, but also increasingly varied in scope. This note comprehensively describes the assorted features and various refresh modes available in Fujitsu DRAMs. Also discussed are standard memory board design tips and a 32-bit microprocessor application.

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Introduction

DRAMs are almost as old as the first microprocessor-based computers, yet new features are continually being introduced to DRAM technology. This publication consolidates and explains many of the various features found on present day DRAMs. Although all these features are not found on a single DRAM, they are available in Fujitsu's extensive DRAM family.

DRAM Features

Fast Page Mode

Fast page mode (also known as ripple mode) is a unique mode designed to decrease power consumption and access times between memory read or write cycles. Quick access to different columns in the same row is accomplished by keeping the Row Address Strobe ($\overline{RAS}$) low throughout the operation. Then a new column address is applied and the Column Address Strobe ($\overline{CAS}$) is brought low and valid data is either read from or written to the memory cell depending upon the value of the Write Enable ($\overline{WE}$). $\overline{CAS}$ is then brought high and a new address is applied. $\overline{CAS}$ is again brought low to latch the address. A timing diagram for the CMOS 1-megabit DRAM (MB81C1000) is shown in Figure 1.

Nibble Mode

Nibble mode allows high-speed reading and writing of data. An example of 1-megabit DRAM address generation using nibble mode is shown in Table 1 where the starting address is 0. The procedure represented by this table is to access a memory cell, in either the normal read or write manner, then to toggle $\overline{CAS}$, which enables an internal address generator that automatically sets row address (RA) 9 to high (1) yet leaves all other bits unchanged. By toggling $\overline{CAS}$ once more the internal address generator causes RA9 to go to low (0) and column address (CA) 9 to go to high (1). Another toggle of $\overline{CAS}$ causes RA9 to go to high (1) and CA9 to remain high (1). One last toggle of $\overline{CAS}$ causes RA9 and CA9 to return to their original state and the entire process repeats.

There are two advantages to using this method of internal address generation. The first advantage is that read/write cycle times are reduced to 50 ns (for Fujitsu's MB81C1001–80, a 1,048,576 x 1 bit Nibble Mode DRAM), which is faster than comparable DRAM cycle times by at least a factor of three. The second advantage is that the system chip count is reduced since there is no longer a need for external glue logic. One practical implementation of nibble mode is accomplished by grounding A9, thereby making RA9 and CA9 the least significant bits (LSBs) in an address. Once A9 is grounded, sequential memory accesses can be made simply by toggling $\overline{CAS}$.

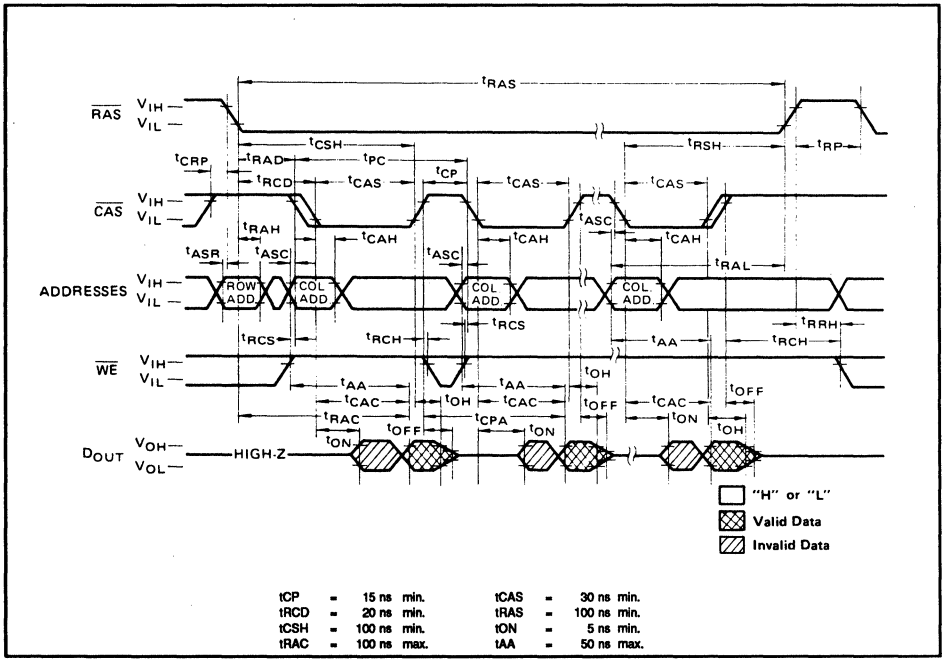


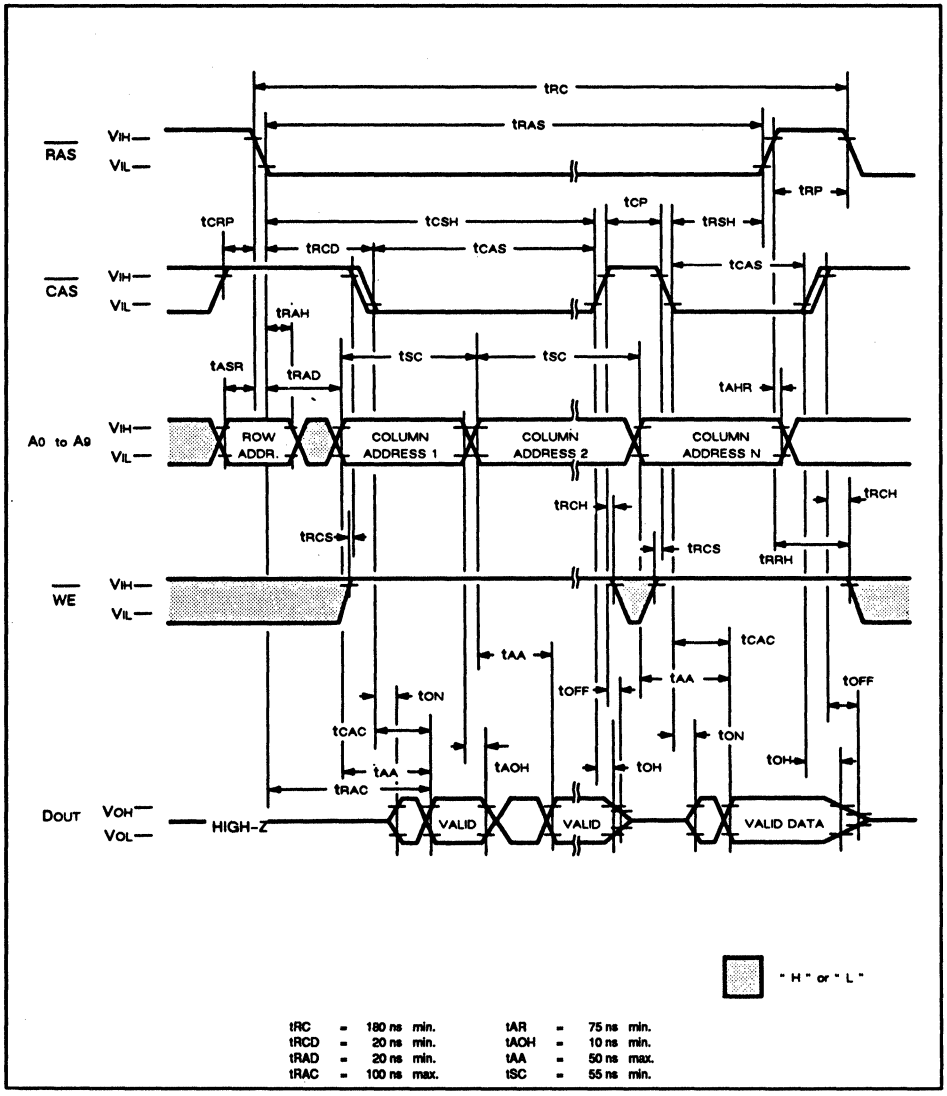
Figure 1. Fast Page Mode Read Cycle

Table 1. Address Generation Using Nibble Mode

Sequence	Bit Accessed	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Normal $\overline{CAS}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{CAS}$	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{CAS}$	3	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
$\overline{CAS}$	4	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Normal $\overline{CAS}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Static Column Mode

A Static Column DRAM (SCRAM) offers a significant speed advantage. Sequential accesses are made in nearly 50 percent of the time it takes to make random accesses. A typical read/write cycle can be done in 55 ns (Fujtsu's MB81C1002-10, a 1,048,576 x 1 bit Static Column DRAM). This is the closest a DRAM comes to being operated as a less complex, fast SRAM. The procedure followed by a SCRAM is to apply a row address, latch it by dropping the $\overline{RAS}$, then apply a column address and latch it by dropping the $\overline{CAS}$. To access more column addresses there is no need to strobe a column address anymore. Instead, the new column address is applied at any time and new data becomes available after a short delay time (t_{AA}). To access any random column, apply the column address and the data appears after a short delay time. A comparison of static column mode versus fast page mode reveals that random column addresses for fast page mode are latched by dropping the $\overline{CAS}$, while column addresses for the static column mode are randomly applied while the $\overline{CAS}$ is low. See Figure 2 for a timing diagram.



tRC	= 180 ns min.		tAR	= 75 ns min.	
tRCD	= 20 ns min.		tAOH	= 10 ns min.	
tRAD	= 20 ns min.		tAA	= 50 ns max.	
tRAC	= 100 ns max.		tSC	= 55 ns min.	

Figure 2. Typical Static Mode Read Cycle

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Comparison of DRAMs

Table 2 lists the specifications of the various DRAM features.

Table 2. Comparison of DRAMs

Type of DRAM	Mode Access Time (ns)	Cycle Time (ns)	Type of Access	Total Accessible Bits
Fast page mode (–80)	t_{cac} = 25 ns	t_{pc} = 55 ns	Random columns	1024
Nibble mode (–80)	t_{cac} = 25 ns	t_{nc} = 50 ns	Sequential columns	4
Static column mode (–80)	t_{AA} = 50 ns	t_{sc} = 55 ns	Random columns	1024

Internal DRAM Operation

To the average user, DRAMs are thought of as a simple storage device. However, DRAMs consist not only of storage capacitors but also internal decoders, sense amplifiers, buffers and address transition detectors (ATD). The following paragraphs will discuss DRAM inner circuitry in more detail.

Multiplexed Addressing

Present day DRAMs have exactly half the number of actual address pins needed to address all the words in the DRAM. Clever use of multiplexed address pins makes it possible to address 1 megabit of words with only 10 actual addresses in the pin assignment. This is accomplished by latching RA0 through RA9 (the row address) on the fall of the $\overline{RAS}$ and then applying new addresses to CA0 through CA9 (the column address) and latching them on the fall of the $\overline{CAS}$, thereby accessing 1 megabit of words by applying only 10 address lines at one time. This approach allows for more compact packages.

Word Line versus Bit Line

Even though a 1-megabit DRAM is physically arranged as 1024 rows and 1024 columns, for refresh purposes the operation is that of 512 rows and 2048 columns. This effectively halves the number of refresh cycles needed from 1024 to 512 thereby decreasing the amount of time the system wastes in refreshing.

A schematic of a single cell is given in Figure 3. Access to each cell in the DRAM is accomplished by connecting to one of 512 row lines (referred to as word lines), and to one of 2048 column lines (referred to as bit lines). The input row address is applied to a row decoder which selects one of the 512 rows. The input column address is applied to a column decoder which selects one of the 2048 columns. By this method one of the 1,048,576 storage cells is singled out.

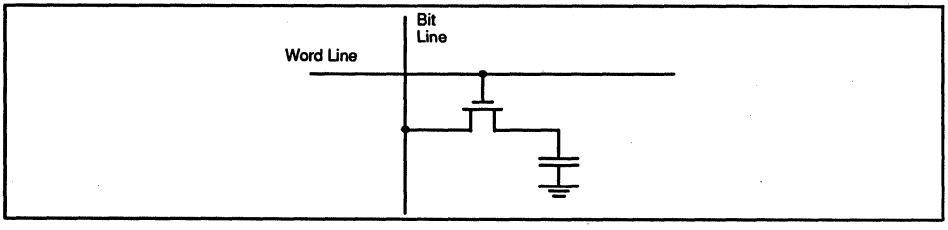

Figure 3. One Transistor (and One Capacitor) RAM Cell

Sense Amplifiers

Sense amplifiers are necessary to correctly read the stored value in each cell storage capacitor. Since each cell capacitance has a value in the femtofarad (10^{-15} farads) range, while the interconnecting lines have capacitance values in the picofarad (10^{-12} farads) range, it is not difficult to understand why the stored voltage can be corrupted by noise during transfer to the output buffers. This obstacle is overcome by comparing the stored or unstored charge to a known charge in a "dummy cell." Once the comparison is completed the output is amplified by the sense amplifiers resulting in better noise immunity.

Memory Board Design Rules of Thumb

Decoupling and Isolation Capacitors

An inherent system-level problem in DRAM designs is transient noise resulting from switching internal currents during refresh cycles. During refresh, DRAMs can require peak currents in the 50- to 100-mA range. Most of the instantaneous current demand is supplied by the decoupling capacitor. In addition to supplying instantaneous current, the capacitor must also meet the following requirements:

- Low inductance and low effective series resistance to minimize the voltage drop across the device. (These parameters are a function of the capacitor type.)
- A capacity to absorb the voltage bumps that occur due to fast edge rates during DRAM access.

Ceramic capacitors have been found to best meet the above requirements. Using a 0.22 µF decoupling capacitor for each DRAM in a 1-megabit application yields the following acceptable voltage undershoot for a 250 ns cycle:

$$V_{under} = (I * t)/C = (100\ mA * 250\ ns)/0.22\ \mu F = 114\ mV$$

Another necessary capacitor needed on a DRAM memory board is the isolation capacitor for the incoming main power bus. Since wiring from the power supply to the memory card can have significant resistance and inductance, which results in power supply ripple and noise, it is recommended that a 50- to 100-mF electrolytic capacitor be inserted.

Power Up Recommendations

DRAMs have historically needed multiple input voltages for substrate bias generation. Currently, all that is needed is 5 V because the substrate bias generator is internal to the chip. The bias generator takes approximately 200 ms to stabilize the substrate voltage hence it is recommended that the $\overline{CAS}$ and $\overline{RAS}$ be on high during this time period. There are two reasons for keeping the $\overline{RAS}$ and $\overline{CAS}$ high in a dense memory board. The first is that if the $\overline{RAS}$ and $\overline{CAS}$ were both low, the DRAMs would draw much larger currents, which could result in a system failure. The second reason is that all the DRAM output levels during power up are unknown, so if the $\overline{RAS}$ and $\overline{CAS}$ were low, there could be data contention in the case of wired AND outputs. However, if the $\overline{RAS}$ and $\overline{CAS}$ were high then the outputs would not conflict since they are guaranteed to be in the high-impedance state.

Once power up has been established, it is necessary to perform eight dummy cycles to stabilize the internal circuitry. The type of cycle (read, write, $\overline{CAS}$-before-$\overline{RAS}$, hidden refresh) required depends on

whether the internal refresh counter will be implemented or not. (Check the data sheet of the specific device.)

Undershoot and Ringing

Undershoot and ringing occur only when line voltages go from high to low or from low to high respectively and not during static state operation. Undershoot and ringing are caused by noise, inherent transistor switching characteristics, and mismatched impedances between the driver output, the signal line, and the load.

Undershoot and ringing due to mismatched impedances can be effectively eliminated by understanding their cause and implementing good design techniques. In present high-frequency applications, line impedance is a function of line capacitance and line inductance is as given by the following equation:

$$Z = (L/C)^{1/2}$$

There is approximately 10 nH of inductance per inch in a 13-mil wide trace. Similarly, there is approximately 4 pF of capacitance per inch in a 13-mil wide trace. So it is easy to see how the impedance of traces can be 50 ohms.

From physics we know that if an initial voltage (Vo) meets a mismatch between the line impedance (Zo) and the load impedance (Zl), Vo will break into two separate components: transmitted voltage (Vt) and reflected voltage (Vr). The reflected voltage equation is as follows:

$$Vr = [Vo\ (Zl - Zo)]/(Zl + Zo)$$

When load impedance is equal to line impedance there is no reflected voltage wave. When there is mismatch between load and line impedance, the reflected wave causes oscillations in Vo resulting in ringing and undershoot.

The best way to prevent ringing and undershoot is to put a 20- to 30-ohm series damping resistor in all trace circuits to the DRAM. This generally decreases load and line impedance mismatch enough to significantly decrease undershoot and ringing.

The Difference Between Soft and Hard Errors

A soft error is a bit error that disappears when a system is rebooted. A hard error causes permanent damage to a particular cell, or group of cells, in a memory device. Consequently, random soft errors are much more difficult to trace and fix, whereas hard errors are only remedied by replacing the entire chip.

Soft Error Causes

There are two major causes of soft errors. The first cause is alpha particles emitted by radioactive impurities in memory component packages. The stray alpha particles cause ionization along their paths, thus changing the charge stored in the memory cell. The second cause of soft errors is internal noise in the die. Internal noise problems can only be eliminated by prudent and proven transistor design techniques such as those used by Fujitsu's Design Engineering Group in Kawasaki, Japan. Fujitsu has taken extensive steps to decrease soft errors due to alpha particles by implementing the following design techniques:

- Using metal bit lines which physically reduce the size of alpha particle-sensitive portions on the die.
- Applying a thin layer of polyamide (which is known to absorb alpha particles) to the die. For example, a 3.5-mil thick polyamide coating can stop most alpha particles from entering and corrupting cells.

Fujitsu has also designed and manufactured a full line of CMOS DRAMs since CMOS has better noise immunity and it is also inherently less prone to soft errors than NMOS.

The number of failures that can be expected due to soft and hard errors is minute. Table 3 displays the number of expected soft errors per device for a time period of one billion device hours. The industry nomenclature for device failures is failures in time (FITs).

Table 3. Failures Per Billion Device Hours

Fujitsu Device	Soft Errors
256 k DRAM	<500 FITs
1 Mbit DRAM	<1000 FITs
4 Mbit DRAM	<1000 (target) FITs

Hard Error Causes

Latchup

One of the disadvantages of CMOS is the inherent problem of latchup. Latchup occurs from parasitic bipolar actions and results in excessive current-sinking logic which destroys the device. Fujitsu reduces the possibility of latchup by using the following preventative measures:

- Incorporating substrate bias generators on the die so that uniform substrate potential of the transistors is maintained. This prevents the parasitic diodes from forward biasing (which would permit excess current to flow) when undershoot occurs.
- Clamping diodes on the inputs which prevents excessive undershoot voltages from occurring.

Electrostatic Discharge

Since MOS has high input impedance and low breakdown voltage, another inherent CMOS disadvantage is device sensitivity to electrostatic discharge (ESD). Fujitsu offers ESD protection in the thousands of volts range, in addition to undershoot and overshoot protection. The input protection circuitry for 1-megabit DRAMs is shown in Figure 4. Grounding any people or machinery that touch the device will nearly eliminate ESD failures.

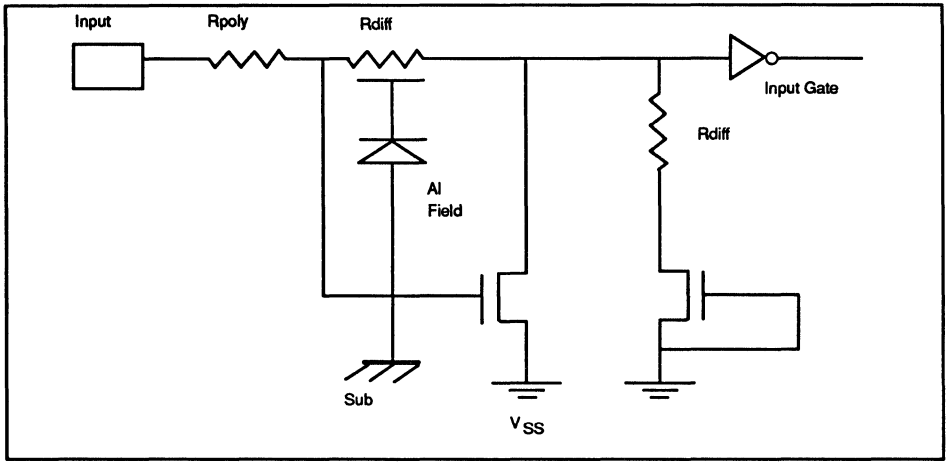

Figure 4. 1-megabit CMOS DRAM Input Protection Circuit

Dual-Port DRAMs

Since memory is inherently parallel and video data is inherently serial, graphics systems have always needed parallel-to-serial shift registers. The extra logic needed to perform graphics tasks increased delay times, used board space, and was not very efficient in high-end graphics applications. These drawbacks have completely vanished with the introduction of Dual-Port DRAMs.

Dual-Port DRAMs are designed to bridge the parallel-to-serial gap by having separate parallel and serial ports. This feature permits image memory to be updated while previous data is being shifted out to the display. The transfer of parallel data to serial data is accomplished by an on-board parallel-to-serial shift register. Conversely, because the serial port has its own clock, it is possible to load the serial port, then shift the data to the parallel access RAM. This type of data manipulation reduces the problem of bus contention especially apparent in display applications. In fact, the Dual-Port DRAM is almost exclusively used for video applications; it is also called a Video RAM.

Bit Masking

Bit masking is used to inhibit (mask) writing to certain bits of nibbles. It is found only in Dual-Port DRAMs where it is most useful in quickly manipulating and operating on individual pixel data.
The advantage of bit masking is that instead of doing a read-compare-modify-write cycle, only a masked write is necessary. The pins used in masking are $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ mask enable ($\overline{ME}$), masked data (MD) <0...3>/data out (DQ) <0...3>, and output enable ($\overline{OE}$). Figure 5 shows the timing for bit masking.

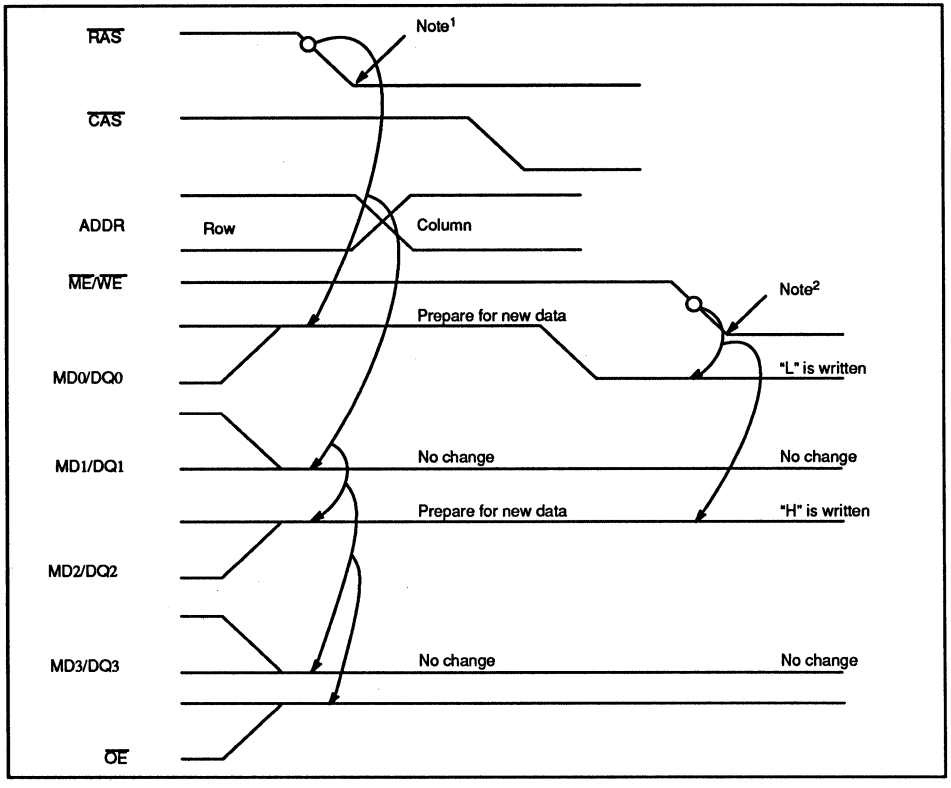

Figure 5. Bit Masking

Notes: [1]At the fall of $\overline{RAS}$ (and if $\overline{OE}$ = H and $\overline{ME}$ = H), all MD inputs that are high will be prepared to receive new data. MD inputs that are low at the fall of $\overline{RAS}$ will not be prepared to be rewritten.

[2]At the fall of $\overline{ME}$ the new data present on all MD pins that were high at the fall of $\overline{RAS}$ will be written to the appropriate bit of the memory.

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DRAM Refresh Methods

DRAMs are basically made up of decoders, latches and capacitors. Capacitors store charges applied to them. Due to leakage, capacitors also dissipate that charge. Consequently, in order to retain their data, all DRAMs need to be periodically refreshed with a pulse to each cell. Methods of refreshing vary from device to device. Some of these methods are discussed in the following paragraphs.

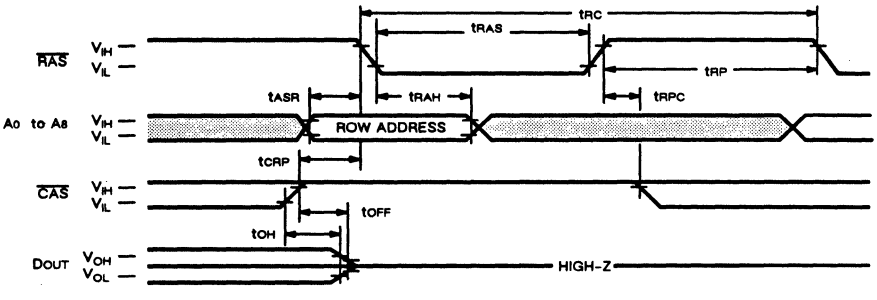
$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh causes the output buffer to remain in a high-impedance state until certain $\overline{RAS}$ and $\overline{CAS}$ timing parameters are met. This type of refresh cycle is ideal for wired-OR outputs. External glue logic

generates row addresses and timing parameters so that all rows are refreshed within the allotted refresh cycle time. Also, whenever a row is accessed for a read or write operation it is refreshed. A two-step process is required to refresh all the cells.

1. Initially the $\overline{RAS}$ and $\overline{CAS}$ are high. Then a row address is applied and the $\overline{RAS}$ is brought low, thereby refreshing all cells in that row.
2. After the $\overline{RAS}$ is brought high, a new row address is applied and the procedure repeats.

A timing diagram is shown in Figure 6.



DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DOUT pin is kept in a high-impedance state.

Figure 6. Typical $\overline{RAS}$-Only Refresh Cycle

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

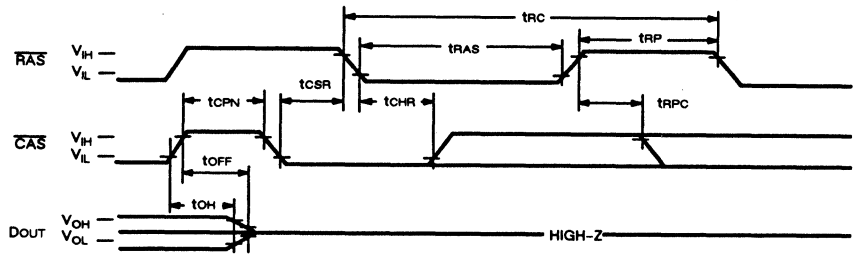
$\overline{CAS}$ before $\overline{RAS}$ refresh eliminates the need for external logic to generate refresh addresses. When using the $\overline{CAS}$ before $\overline{RAS}$ refresh, a one-time start-up procedure must be undertaken enabling this feature and ensuring proper device operation. This procedure initializes the internal address generator.

One requirement of the procedure is that when power is applied, the $\overline{CAS}$ and $\overline{RAS}$ should be high. After power stabilization, the $\overline{CAS}$ should go low before the $\overline{RAS}$ goes low. This cycle has certain setup and hold time constraints, depending on the particular chip being used, but generally speaking at least eight $\overline{CAS}$ before $\overline{RAS}$ cycles must occur to initialize the internal counter.

Once this procedure is completed the normal $\overline{CAS}$ before $\overline{RAS}$ refresh operation is as follows:

1. The $\overline{CAS}$ is brought low then the $\overline{RAS}$ is brought low.
2. The refresh address is supplied by an internal address generator.

A timing diagram is shown in Figure 7.



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

tCHR	=	15 ns min.	tRAS	=	105 ns min.
tCSR	=	0 ns min.	tRC	=	200 ns min.
tOFF	=	25 ns max.	tRPC	=	20 ns min.

Figure 7. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

Hidden $\overline{CAS}$ Before $\overline{RAS}$ On-Chip Refresh

Hidden $\overline{CAS}$ before $\overline{RAS}$ on-chip refresh is similar to a $\overline{CAS}$ before $\overline{RAS}$ refresh except that data remains valid on the data pins as long as the $\overline{CAS}$ is low. Because the internal address counter is used in this cycle, at least eight dummy $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles should occur immediately after power-up. For this type of refresh, keep the $\overline{CAS}$ low at the end of a normal read or read-write cycle, and then bring the $\overline{RAS}$ high, then back to low. Since data remains valid on the output until the $\overline{CAS}$ goes high, this cycle is an extended read or write cycle in the foreground and a "hidden" refresh cycle in the background. A timing diagram is shown in Figure 8.

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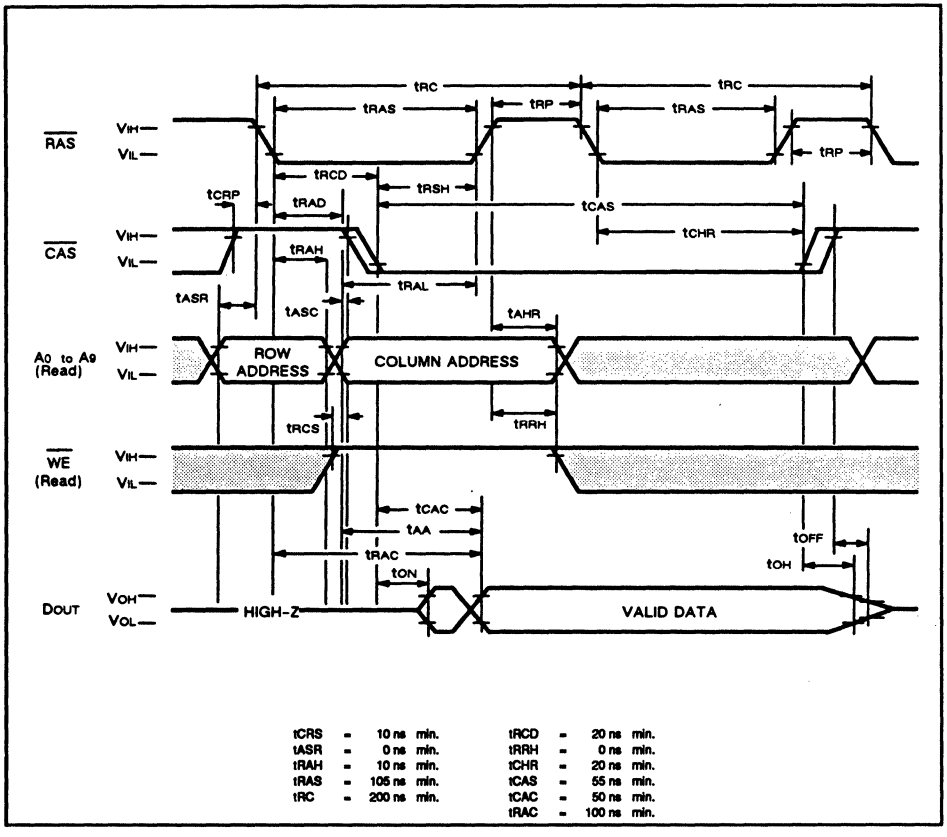

Figure 8. Typical Hidden $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

DRAM Implementation in an MBL80286 Environment

Figure 9 shows a typical implementation of an MBL80286 microprocessor, an MB1430A DRAM controller, an MBL82288 bus controller and several 1-megabit DRAMs. The memory is organized in two banks; one bank contains the data of odd addresses and the other bank contains the data of even addresses. This type of configuration is known as interleaving memory. The main advantage to such an organization is that while one bank of memory is in tRP (RAS precharge time) the second bank is accessed by the bus. Then, while the second bank is in tRP the first bank is accessed by the bus. This decreases the perceived DRAM cycle time. Interleaving memory is an optimum configuration as long as the same bank of memory cells doesn't need to be accessed sequentially.

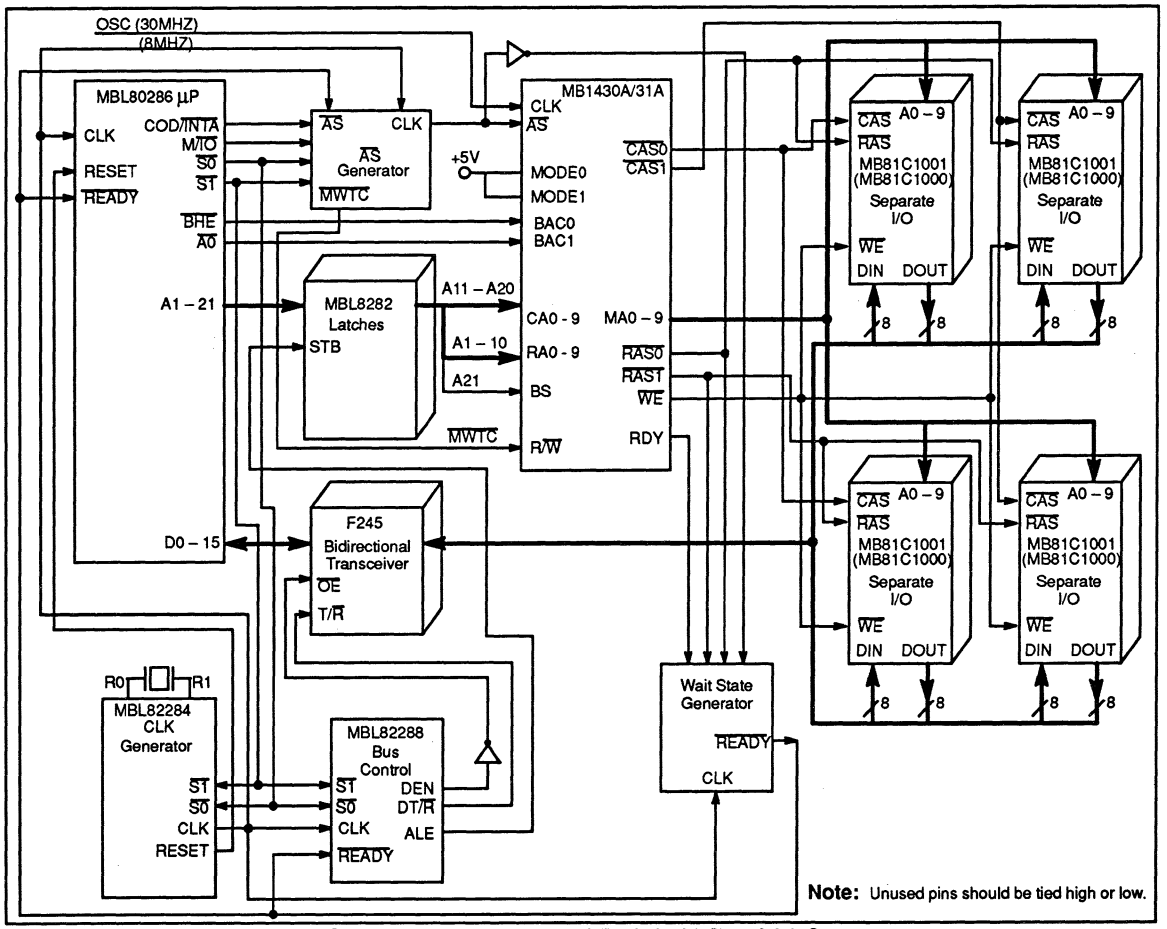

Figure 9. Schematic of 1 megabit x 32 DRAM with Zero Wait States

Figure 10 shows the RAS0 and RAS1 timing that allows interleaving. If the same bank is accessed sequentially then the microprocessor must generate wait states and endure the tRP. The odd or even bank is selected depending on the value of bus high enable ($\overline{BHE}$) and A0. The size of the operation taking place (word or byte) can also be determined by polling $\overline{BHE}$ and A0. This relationship is shown in Table 4.

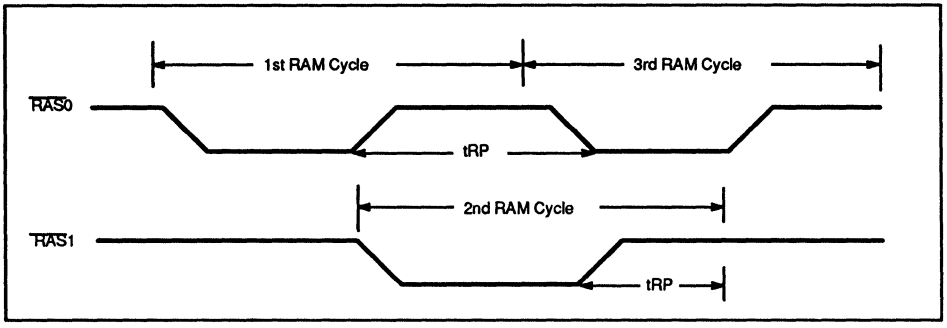

Figure 10. $\overline{RAS}$ Timing of Interleaving Memory

Table 4. Relationship Between $\overline{BHE}$, A0, and Size of Operation

$\overline{BHE}$	A0	Operation
0	0	Word Transfer
0	1	Byte Transfer on Upper Half of Data Bus (D15–D8)
1	0	Byte Transfer on Lower Half of Data Bus (D7–D0)
1	1	Reserved

The purpose of the octal latches in the Figure 9 schematic (MBL8282) is two-fold: first to demultiplex the address lines and secondly to increase the total drive capability to 32 mA. Once the address lines have been demultiplexed they become inputs to a DRAM controller. The DRAM controller generates the necessary $\overline{RAS}$ and $\overline{CAS}$ timing on the $\overline{RAS0}$, $\overline{CAS0}$, $\overline{RAS1}$, and $\overline{CAS1}$ lines. The MB1430A DRAM controller can accommodate various microprocessors including the Motorola 68000. In addition, the MB1430A can drive up to 44 DRAMs without the use of drivers.

There are also two purposes for using the bus transceivers in the Figure 9 schematic is two-fold: first to demultiplex the data lines from the multiplexed address-data lines, and second to allow microprocessor read-writes. In the case of a write operation, once the data has been demultiplexed it is put through a bidirectional bus driver which allows data to be read and increases the drive capability. The direction of data flow is determined by the data transmit/receive (DT/$\overline{R}$) pin. The bus controller in the Figure 9 schematic orchestrates the entire system under the control of the microprocessor, MBL80286. The signals output by the microprocessor determine the operation taking place (see Table 5).

Table 5. MBL80286 Bus Cycle Status Definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0 (low)	0	0	0	Interrupt Acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None: Not a Status Cycle
0	1	0	0	If A1 = 1 Then Halt; Else Shutdown
0	1	0	1	Memory Data Read
0	1	1	0	Memory Data Write
0	1	1	1	None: Not a Status Cycle
1 (high)	0	0	0	Reserved
1	0	0	1	I/O Read
1	0	1	0	I/O Write
1	0	1	1	None: Not a Status Cycle
1	1	0	0	Reserved
1	1	0	1	Memory Instruction Read
1	1	1	0	Reserved
1	1	1	1	None: Not a Status Cycle

DRAM Modules

DRAM modules are dense memory packages that are a fraction of the size of the same memory structure in a board design. Some of the common module sizes are 1M x 9, 256 k x 9, and 16 k x 32.

Summary

Fujitsu DRAMs offer a selection of features that include: fast page mode, nibble mode, and static column mode. Fujitsu also manufactures dual-port DRAMs and DRAM modules.

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7

Appendix 2

Application Note

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FUJITSU

APPLICATION NOTE

The Soft Error Rate for 4M DRAM Devices

By Adrian B. Cosoroaba
Standard Products Marketing Department
Fujitsu Microelectronics, Inc.
Integrated Circuits Division

Abstract

Alpha particles (helium nuclei) emitted by trace quantities of radiative elements in the DRAM packaging materials can cause temporary errors in a memory array and its operation. These errors result from changes in the amount of electron charge stored on the capacitor of the memory cell, as well as changes in voltage levels of activated bit lines. The changes are temporary, in that a write to the affected memory cell can correct the error, which is called a soft error. This application note explains the process of soft errors and estimates the soft error rate (SER) for Fujitsu's 4M DRAM devices under accelerated conditions. The 4M DRAM is compared with Fujitsu's 256K and 1M devices to show the improvement in soft error rate.

The Soft Error Phenomenon

The package material of DRAMs contains trace quantities of uranium and thorium which can emit alpha particles of various energy levels. These alpha particles (helium nuclei consisting of two protons and two neutrons), upon impact with the silicon crystal lattice, produce electron-hole pairs. The dislocated electrons can be attracted to the potential well (that forms the capacitor plates of the memory cell) and change the electrical state of the memory cell. The capacitor becomes charged and the logic state changes from "1" to "0" (Figure 1);. i.e., the memory cell mode of producing a soft error.

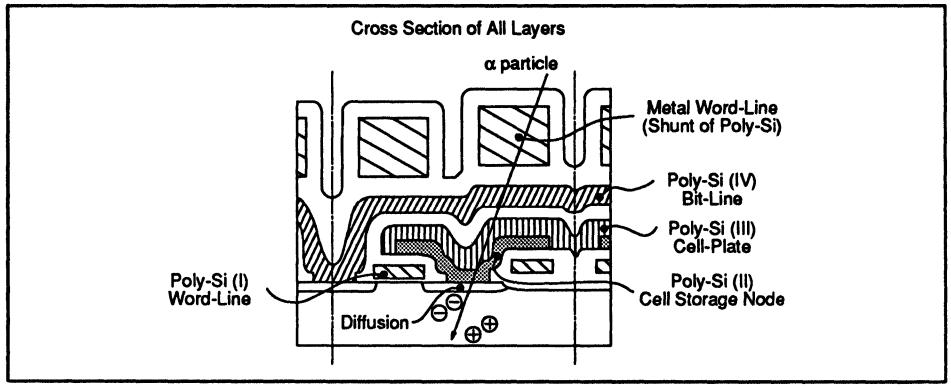

Figure 1. 4M DRAM Stacked Capacitor Cell

Soft errors can also be produced by alpha particles through another mechanism, one that involves the bit lines. When the information in the memory cell is read out to the bit line, a potential comparison is made. When electrons generated by alpha particles flow into the bit line during this comparison process, they cause the reference potential to drop. As a result of this a "0" to "1" inversion occurs.

Soft errors caused by this bit line mode are inversely proportional to the cycle time: the longer the cycle, the less frequent are the bit line activations and resultant exposure time to alpha particles. The memory cell mode error rate is independent of the cycle time. The following figure (Figure 2) illustrates the composite rate.

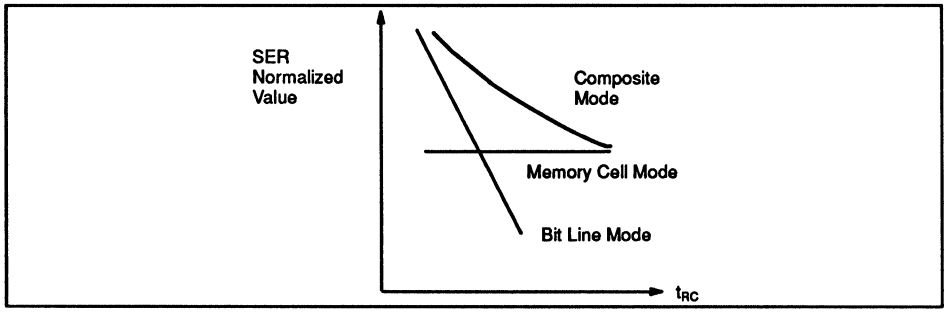

Figure 2. Soft Error Rate vs. Cycle Time

Soft Error Rate Estimation

The soft error rate of a particular device can be analyzed in relationship with other device parameters (V_{CC} and t_{RC}) using an accelerated test scheme. For an example of soft error rate estimation, see Figure 3 which shows a Fujitsu MB814100 4M DRAM die exposed to an americium 241 source.

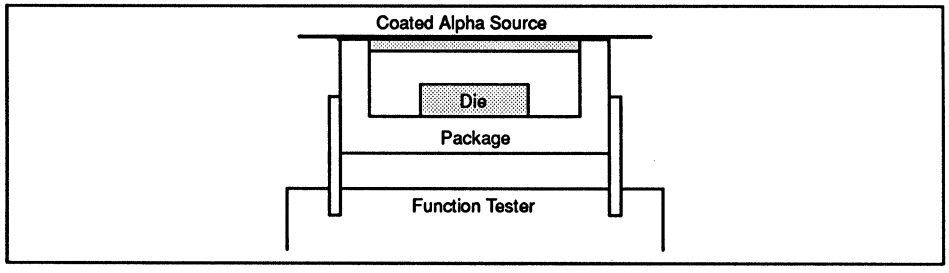

Figure 3. Alpha Source Acceleration Test

The alpha particles are generated by the americium source, and under the following conditions:

Alpha source element : Am 241
Alpha source intensity : 10μCi (1.4 x10^9 alpha/cm^2/hour)
Alpha source energy : 5.35 MeV
Geometrical condition: 2 mm vertically above the chip
V_{CC} : *4.0 – 6.0 V*
t_{RC} : *0.5 – 10 μS*
Test data pattern : checkerboard
Test address pattern : linear sequence

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The results can be expressed in two forms, SER vs. V_{CC} and SER vs. t_{RC}. The following graph (Figure 4) shows the soft error rate (normalized value) vs. V_{CC} (supply voltage) when cycle time t_{RC} = 500 ns.

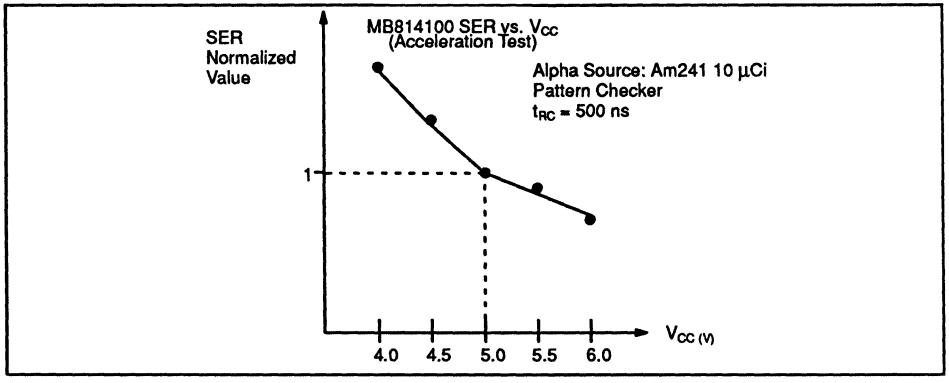
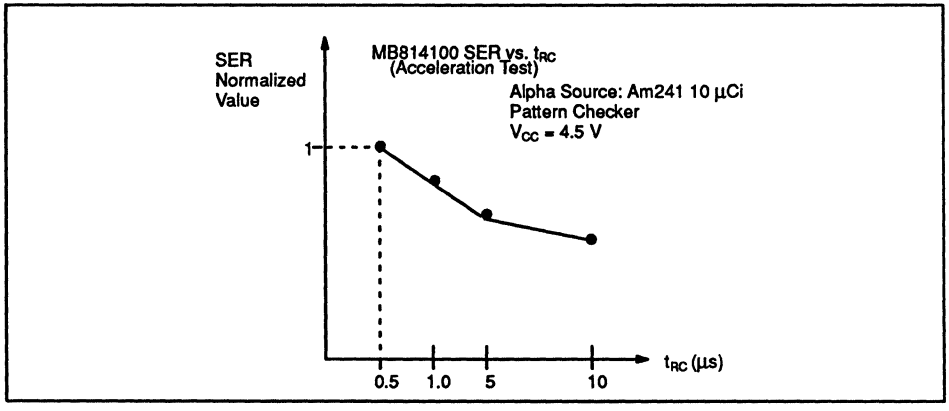


Figure 4. Soft Error Rate vs. V_{CC} (MB814100)

Figure 4 demonstrates that the lower the voltage V_{CC}, the higher the rate of soft errors. This is due to the lower potential that has to be changed by the alpha particle-induced electrons.

The next graph (Figure 5) shows the dependency of the composite soft error rate on the cycle time, t_{RC}.



Figue 5. Soft Error Rate vs. t_{RC} (MB814100)

In this case, the SER is inversely proportional to the cycle time. The longer the cycle, the less frequent are the bit line activations and resultant exposure time to alpha particles. Hence, the SER decreases with the increase in t_{RC}.

Soft Error Rate Comparison

The accelerated test data that has been compiled can be used to compare the SER of MB814100 to similar devices from other manufacturers or to compare the soft error rate of several Fujitsu DRAMs, from the 256K to the present 4M devices.

In order to compare the SER for the Fujitsu 256K, 1M and 4M devices, the SER values can be normalized to reflect the same alpha particle flux densities. The following figure, Figure 6, represents a comparison between the SER of 256K, 1M and 4M DRAM devices. The marked improvement shown between the 256K and 1M is due to the stacked capacitor cell design. This design technique was adopted by Fujitsu for DRAM cell designs and the 1M DRAM was the first device fabricated using this design technique.

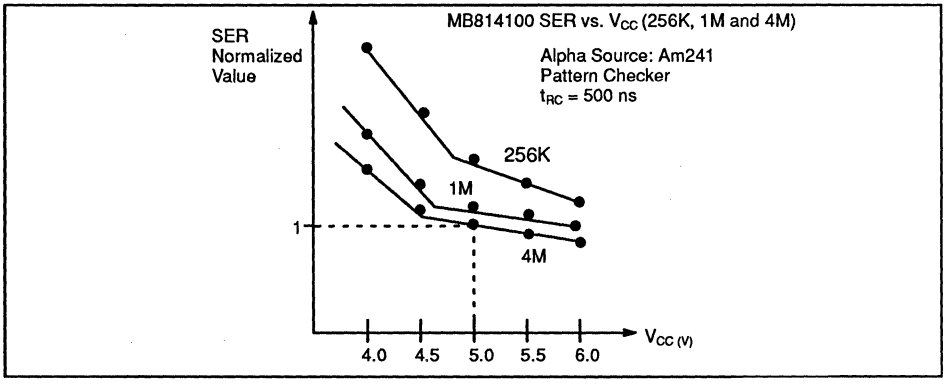


Figure 6. Relative Soft Error Rate vs. V_{CC} (256K, 1M, 4M)

To improve the 4M DRAM, various methods, including an advanced stacked capacitor cell design and an improved circuit design, were used to decrease the SER. Figure 6 shows the SER of the 4M DRAM significantly reduced when compared to that of the 1M and 256K DRAMs.

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Conclusion

The soft error rate for the Fujitsu 4M DRAM, the MB814100, was estimated under accelerated conditions. The results were compared with the previous products, the 256K and 1M DRAMs. The SER for the 4M is an improvement over previous DRAM generations and this is due to various design methods used by Fujitsu such as:

- reduction of trace radioactive elements in package materials
- improved circuit design to minimize the impact of dislocated electrons.

Soft errors in DRAM devices cannot be completely eliminated, but they can be reduced to very small numbers. Fujitsu will continue to develop improved methods that will reduce the soft error rate of present and future DRAM memory products.

Appendix 3

Technical Paper

UDC 621.377.621:681.327.67

3D Stacked Capacitor Cell for Mega Bit DRAM

• Tomio Nakano • Takashi Yabu *(Manuscript received December 16, 1988)*

This paper discusses the three-dimensional stacked capacitor (3D STC) cell technology that Fujistu used in 1-Mbit DRAMs (Fujitsu was the first to do this), and the development of 1-Mbit and 4-Mbit DRAMs using the 3D STC technology. 3D STC technology is the key to cell area reduction enabling densities higher than 1-Mbit. This technology provides mass production capability and a high immunity to alpha-particle-induced soft errors. To respond to market demands for low power consumption, high speed, and high reliability, 1-Mbit DRAMs were designed using CMOS technology. A 4-Mbit DRAM having an access time of 56 ns and low power consumption of 175 mW was also developed.

1. Introduction

Since the 1-Kbit dynamic memory (DRAM) was developed, the density and performance of MOS DRAMs have steadily improved and have led the semiconductor technologies of Fujitsu. In 1985, a three-dimensional stacked capacitor cell was developed [1] and first used in a 1-Mbit DRAM.

The three-dimensional design of a capacitor using this cell technology results in a large cell capacitance in a very small cell area and high scalability. These features have attracted much attention to this cell technology and it is being widely used for 4-Mbit DRAMs[2),3)]. This report discusses the three-dimensional stacked capacitor cell (3D STC) technology and the 1-Mbit and 4-Mbit DRAMs that use this technology.

2. Development of DRAMs having capacities up to 256 Kbits

Figure 1 shows the DRAM developments by Fujitsu. Since the development of the 1-Kbit DRAM in 1971, integration has quadrupled every three years. A 4-Mbit DRAM may be introduced to the market in 1989. The major points of this steady progress in high integration is reviewed below.

Figure 2 shows that the cell area has been reduced by a factor of 400 in the last 18 years. This area reduction was mainly due to the progress in fine lithography techniques, cell structure, and circuit technology. The standard DRAM design rule for fine lithography has been to make the lithography 0.7 times finer in each generation. The 4-Mbit DRAM must now be processed in units of submicrons. In each generation of DRAM, a cell area reduction technology has been developed (see Table 1).

The general progress of DRAMs can be viewed as the advance of memory cell technology. The memory cell of a 1-Kbit DRAM consists of three (or four) transistors (see Fig. 3a)[4)]. Although this cell has a large area, it has the advantages of current amplification capability and is easy to read. In the single-transistor cell system that was first incorporated in the 4-Kbit DRAM, a one-bit memory cell consists of a transistor as a switch and a capacitor that stores information as an electric charge (see Fig. 3b).

Because the single-transistor cell does not have current amplification capability, the signal voltage on a bit line is very small (100 V to 200 mV). Advances in circuit technology, including the sense amplifier, has enabled this small signal to be detected at high speeds and has provided the basis for DRAMs ever since.

Table 1. Development of DRAM technology for each generation.

Capacity (bit)	Lithography technology		Cell structure	Circuit technology
	Design rule (μm)	Etching		
1K	9	Wet	3 transistors	pMOS Dynamic
4K	8	Wet	1 transistor	nMOS Dynamic
16K	6	Wet	Double poly-Si	MPX add. 16 pin PKG
64K	3	Dry	Double poly-Si	Single 5 V supply
256K	2.5	Dry	Triple poly-Si	Redundancy, high speed
1M	1.8	Dry	3D STC cell	CMOS Dynamic
4M	0.8	Dry	4 layer poly-Si STC	Blocknized peripheral

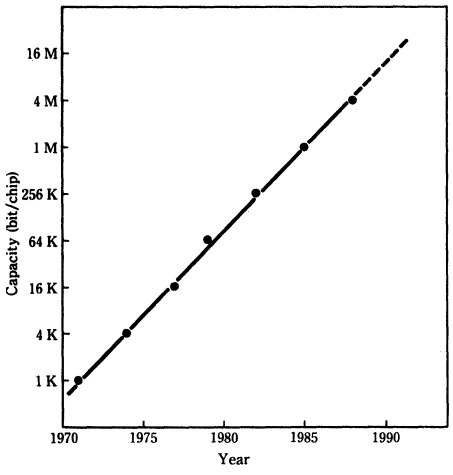

Fig. 1—DRAM development of Fujitsu.

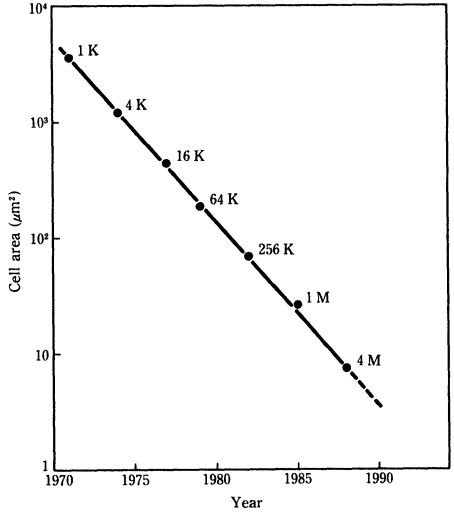

Fig. 2—History of cell area reduction (Cell area reduced by a factor of 400 in 18 years).

7

The following section explains the principle of operation of the sense amplifier for the single-transistor cell using the circuit of the 256-Kbit DRAM MB81256[5] as an example.

2.1 Sense amplifier for single-transistor cell

Figures 4 and 5 show the major circuits of the sense amplifier and their operating waveforms. A sense amplifier consists of a dynamic flip-flop circuit having a pair of transistors (Q_1 and Q_2). A small differential voltage between the left and right bit lines is quickly amplified. That is, sense amplifier activation clocks A and B are set to a high level sequentially at time t_1 (see Fig. 5), and the differential voltage between nodes N_1 and N_2 increases. At time t_2 after amplification, the active restore circuit operates to recharge the bit line to the high level V_{CC}, and the series of read operations is completed.

The cell read signal voltage can significantly affect the stability of sense amplifier operation. This is analyzed in a simplified manner below. In Fig. 4, the bit line capacitance is C_{BL}, cell capacitance is C_S, dummy cell capacitance is C_D, and the cell potential at time t_0 is V_S. The

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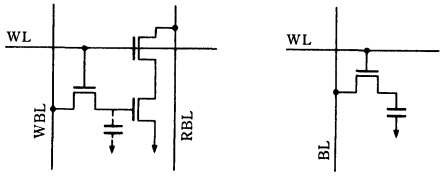

a) 3 transistor cell b) 1 transistor cell

Fig. 3—DRAM memory cell circuit.

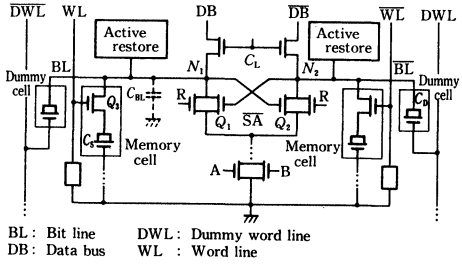

Fig. 4—Sense amplifier circuitry of 254-K DRAM.

potential difference (or signal voltage) V_{sig} between sense amplifier input nodes N_1 and N_2 at time t_1 is determined by the ratio of cell and bit line capacitances and is expressed as follows.

$$V_{sig} = -\frac{Cs}{C_{BL} + C_S}(V_{CC} - V_S) \bullet \gamma + \frac{C_D}{C_{BL} + C_D} V_{CC} \bullet \gamma \pm V_n$$

In the above expression, γ is the cell read efficiency and V_n is the noise voltage to the sense amplifier. From the above expression and the MB81256 cell capacity, the relation between cell potential V_S and signal voltage V_{sig} is obtained as shown in Fig. 6. In this example, the reference voltage is set to 2 V and the read margin at the high level is set above the read margin at the low level because of the leakage at the p-n junction and the cell charge loss due to alpha particles[6].

2.2 DRAMs and cell technology before 1-Mbit DRAM

The 64-Kbit DRAM can be operated by a

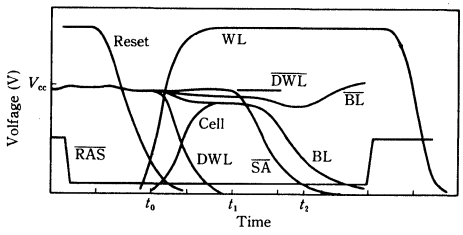

Fig. 5—Operational waveforms of sense amplifier.

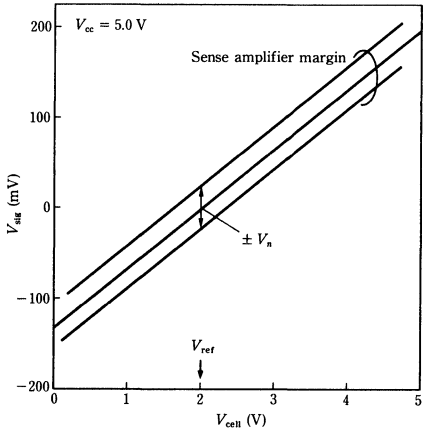

Fig. 6—Relation between V_{cell} and V_{sig} (Dummy cell is adjusted to fit V_{ref} = 2 V).

single 5 V power supply while conventional-DRAMs require three power supplies (+12 V ± 5 V). This design enabled the DRAM to be connected to peripheral circuitry more easily and expanded the field of DRAM applications from main storage in large computers to personal computers. This resulted in a dramatic increase in the demand for DRAMs nMOS technology, which had been used for DRAMs having capacities of 4 Kbits to 256 Kbits, was replaced by CMOS technology when 1-Mbit DRAMs were developed to reduce power consumption and increase speed.

The objective of cell structure development at this time was the promotion of multilayer and

three-dimensional designs. For DRAMs having 4 Kbits or less, the capacitor and transistor consist of a single poly-silicon layer whose capacitor area occupies only a small portion of the cell area. Double poly-silicon layer technology was first used for a 16-Kbit DRAM. The double poly-silicon layer structure provides the first-layer for the capacitor electrode and the second layer for the transistor gates. This increases the capacitor area occupancy ratio. In addition, the function of each poly-silicon layer can be limited, enabling the optimum gate oxide thickness for the capacitor transistor to be selected individually. Thus the maximum capacitance can be provided in a very small cell area.

The multilayer poly-silicon design was further advanced. The resulting three-layer poly-silicon technology developed for the 256-Kbit DRAM has increased the speed even more. This technology provided the basis for the smooth development of 1-Mbit three-dimensional stacked capacitor (3D STC) cells. The cells of DRAMs having 256 Kbits or less use the surface of the silicon substrate for the capacitor and transistor and are classified as planar cells. If the cell area was reduced by using only fine lithography together with the planar technique to obtain capacities of 1 Mbits to 4 Mbits, the cell capacity required to guarantee immunity from alpha-particle-induced soft errors could not be achieved. To solve this problem, the three-dimensional design was employed based on the concept of a stacked capacitor cell which overlays the capacitor on the transistor for efficient use of the silicon surface.

7

3. Stacked capacitor cell technology

3.1 Features of mega bit DRAM cells

Various cell structures have been proposed for mega bit DRAM memory cells having three-dimensional structures. The stacked cell forms a capacitor on a single-transistor cell access transistor. The trench cell forms a capacitor in a trench dug in the silicon substrate. Many of the suggested cell structures were trench cell types, but planar cells, which were mainly used for DRAMs having capacities of 256 Kbits or less, are generally used for the 1-Mbit DRAMs now in mass production.

However, the planar cell is reaching the limit of its capability. When the future capacity of DRAMs is considered, it is now necessary to select other cell types as the memory cells for 4-Mbit to 16-Mbit DRAMs. Recently, the developments in stacked capacitor cells have gained attention for their applicability to fine lithography and high scalability.

Fujitsu led other manufacturers by developing the three-dimensional stacked capacitor cell and using it for 1-Mbit DRAMs. Fujitsu subsequently developed a memory cell for a 4-Mbit DRAM having the smallest cell area reported so far using fine lithography technology. Furthermore, Fujitsu has promoted the development of stacked capacitor cell technology combined with a dielectrically encapsulated trench (DIET) capacitor cell[7] which combines the advantages of trench cells and stacked cells.

3.2 Three-dimensional stacked capacitor cell

The memory cell structure is most important for the design of a DRAM. The memory cell almost determines the performance and mass producibility of the DRAM. The memory cell size of the 1-Mbit DRAM must be reduced to about one-third that of the 256-Kbit DRAM. The memory cell size of the 4-Mbit DRAM must be reduced to about one-third that of the 1-Mbit DRAM by using a scaling factor of 0.6 to 0.7. When Fujitsu developed the 1-Mbit DRAM, it planned to develop a basic structure for the memory cell that could be used for at least two generations. After investigating various memory cell structures such as the stacked cell, trench cell, and planar cell, Fujitsu selected the stacked capacitor cell structure due to its high scalability and thus the expandability to 4-Mbit DRAMs.

3.2.1 Folded bit line configuration

The basic idea of stacked cell has existed since 1978[8),9)]. This idea, however, simply stacks the capacitor on the access transistor of the cell and has an open bit line configuration.

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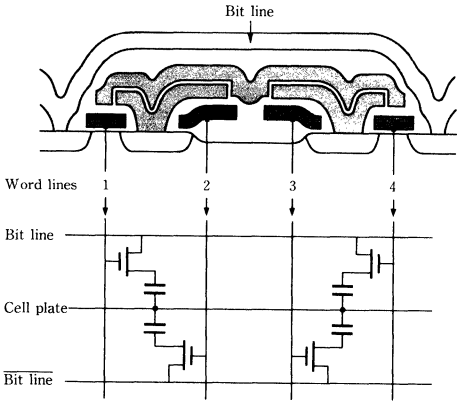

Fig. 7—3D stacked capacitor cell.

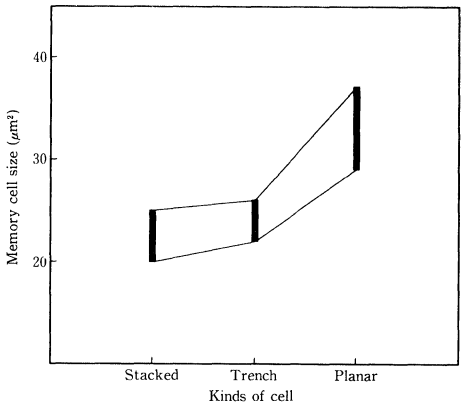

Fig. 8—Comparison of cell size for three types of cell structure.

Fujitsu has also used the open bit line configuration for its 64-Kbit and 256-Kbit DRAMs. However, mega bit DRAMs which have reduced memory cell size require a cell structure that enables the folded bit line configuration for an improved noise margin. Fujitsu has improved the conventional stacked capacitor cell structure by locating word lines under the second polysilicon layer that forms the charge storage electrode (see Fig. 7). This structure forms a memory cell at every other intersection of a bit line and a word line and enables the folded bit line configuration.

3.2.2 Cell Size

A planar cell forms a flat capacitor on the surface of a substrate. The capacitor area is reduced in proportion to the reduction of memory cell size. Even when the fine lithography technique is fully implemented, it has a limited ability to provide a large capacitance in a small area. Because a trench cell has a trench in the substrate in which the capacitor is formed, the capacitor is also formed on the surface of the side walls within the trench. If the trench is deep, a relatively large memory cell capacitance can easily be provided.

A stacked cell forms the capacitor on the access transistor. Therefore, the memory cell capacitance can be increased because the capacitor is formed on the top and sides of the poly-silicon layer for storage node. The bent shape of the storage node also contributes to the capacitance increase.

The memory cell areas of the stacked cell, trench cell, and planar cell were compared when the same lithography technique was used and the capacitor areas were the same (see Fig. 8). The results show that the three-dimensional stacked capacitor cell is the best for reducing the memory cell size.

3.2.3 Soft error immunity

A soft error is an event in which cell information is destroyed. The charge generated by an alpha particle beneath the charge storage region of the cell is absorbed in the diffusion layer, and the voltage potential of the cell is lowered causing cell information to be destroyed.

The first method to prevent soft errors is to suppress the generation of alpha particles by increasing the purity of the package material or by preventing alpha particles from entering the silicon substrate. The second method is to increase the charge storage capacitance to reduce the adverse effect of the charges generated by the alpha particles. The third method is to design a memory cell structure having high resistance to soft errors by lowering the charge collection efficiency of the diffusion layer.

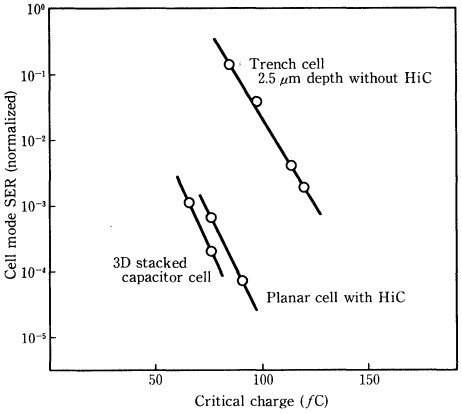

Fig. 9—Comparison of SER for three types of cell structure.

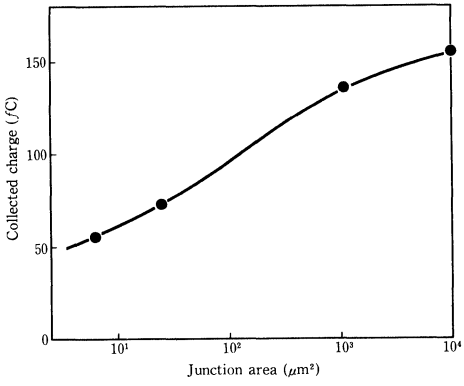

Fig. 10—Dependence of collected charge on junction area.

To increase the storage capacitance, the thickness of the capacitor film must be reduced and the storage electrode areas must be increased. To lower the charge collection efficiently, the diffusion layer area must be reduced or a potential barrier must be formed. For example, a HiC structure[10] or memory cell formation in a p-well[11] is required.

When the stacked capacitor cell was developed, three test devices having the stacked capacitor cell, planar cell, and trench cell structure were made and actual soft error rates were measured (see Fig. 9). The results show that the stacked cell caused fewer soft errors even though it has a small memory cell capacitance.

Because the capacitor is formed on polysilicon in the stacked cell structure, its diffusion area is very small and the collected charge amount is reduced. On the other hand, the capacitor area in a planar or trench cell is equivalent to the diffusion layer area and the edge of the drain is added to this area. The diffusion layer in the charge storage region is therefore enlarged and the collected charge amount become large. Although a large memory cell capacity can theoretically be maintained by the trench cell structure, the critical charge amount must be increased because the diffusion layer area increases according to the increase in the capacity. For this reason, an additional countermeasure, including a potential barrier on the side walls of the capacitor, is required.

This characteristic can also be illustrated by the results of an experiment in which collected charge amounts are measured using test devices having various junction areas (see Fig. 10). If the junction area is small in comparison to the charge amount to be collected, the collected charge amount is reduced because the effective funneling length is shortened by the electric field distortion at the junction edges, and because adjacent cells partially absorb the charge.

3.2.4 Charge retention characteristic

The charge retention characteristic of the memory cell is important in relation to the refresh time of the DRAM. In a 256-Kbit DRAM, the refresh time is 256 cycles/4 ms. That is 1024 memory cells are refreshed by one refresh operation and the operation must be executed 256 times in 4 ms. In a 1-Mbit DRAM, the refresh time is 512 cycles/8 ms, and the refresh time of a 4-Mbit DRAM is 16 ms if the refresh overhead time is the same as that of the 1-Mbit DRAM. The refresh time doubles for each DRAM generation.

To prolong the charge storage time, all sources of leakage current must be reduced.

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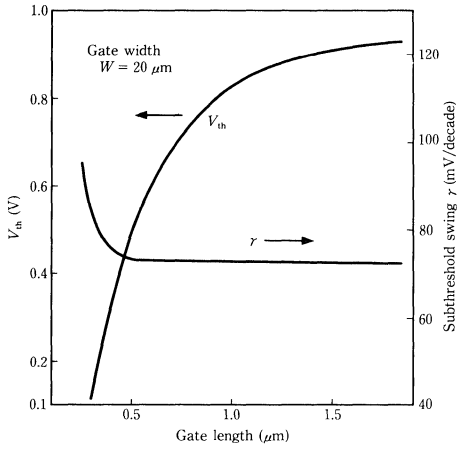

Fig.11 – Threshold voltage as a function of gate length.

When compared with other cell structures, the stacked capacitor cell has a small p-n junction area of the capacitor and lower leakage current. The stacked capacitor cell can also incorporate conventional isolation techniques, resulting in sufficient isolation width and a lower leakage current.

The leakage current of the capacitor dielectirc film on the poly-silicon is not more than 10^{-16} A per cell when the film thickness is 5 nm (effective oxide thickness) and the electric field in the insulating film is 5 MV/cm.

When the transistor becomes very small, the characteristic degradation due to hot carriers and short and narrow channel effects become a problem. The stacked cell can use a large access transistor in comparison with the planar and trench cells. Alternatively, if the same size transistor is used, the stacked cell can have a smaller memory cell size than that of other memory cell structures. Figure 11 shows that the subthreshold swing even in the submicron gate length is 80 mV/decade and the leakage current can be suppressed enough to eliminate the adverse effect on the charge retention characteristic.

3.3 Development of 4-Mbit DRAM memory cell

A 4-Mbit DRAM memory cell was developedby further scaling the three-dimensional stacked capacitor cell developed for 1-Mbit DRAMs. The basic memory cell structure is common to 1-Mbit and 4-Mbit DRAMs. The 1-Mbit DRAM incorporates three-layers poly-silicon and one-layer Al process technology, where polycide us used for word lines, and Al wiring is used for bit lines. The 4-bit DRAM uses further advanced technology having four-layer polysilicon and a one-layer Al process.

In the 4-Mbit DRAM, contacts with the Al word lines are made at eight positions in the cell array to minimize the delay time due to the polycide word lines on the first poly-silicon layer. The bit line is formed by the 4th layer of polycide on which it is easy to form a fine bit line pitch. This eliminates stray capacitances that would be occur if thick Al bit lines were formed. This design resulted in a ratio of bit line capacitance to cell capacitance C_B/C_S of about eleven, which is sufficient for signal sensing.

In addition, a cell capacitance of 27fF was realized by the development of a capacitor insulating film having a thickness of 10 nm (effective exide thickness) or less and by virtue of the three-dimensional structure of the stacked cell. Thus, a 7.5 μm^2 cell was developed and put into use in a practical device.

3.3.1 Four-layer poly-silicon process

Figure 12 shows the process to make the 4-Mbit DRAM memory cell. The substrate is p-type silicon. After isolation and formation of the n-well of CMOS for peripheral circuitry using conventional methods, gate electrodes, including those for the access transistor, are formed on the first poly-silicon layer (polycide). Then the source drain area is formed by ion implantation in Fig. 12a). After oxide film is grown by the CVD method and the contact holes are formed by imprinting a mask pattern, the second poly-silicon layer for the storage nodes is grown. To process the second poly-silicon layer, which affects the storage capacity, accurate patterning was performed while avoiding the influence of the first poly-silicon layer in Fig. 12b). For this process, new lithography and etching techniques to delineate an exact pattern of the reticule and a new

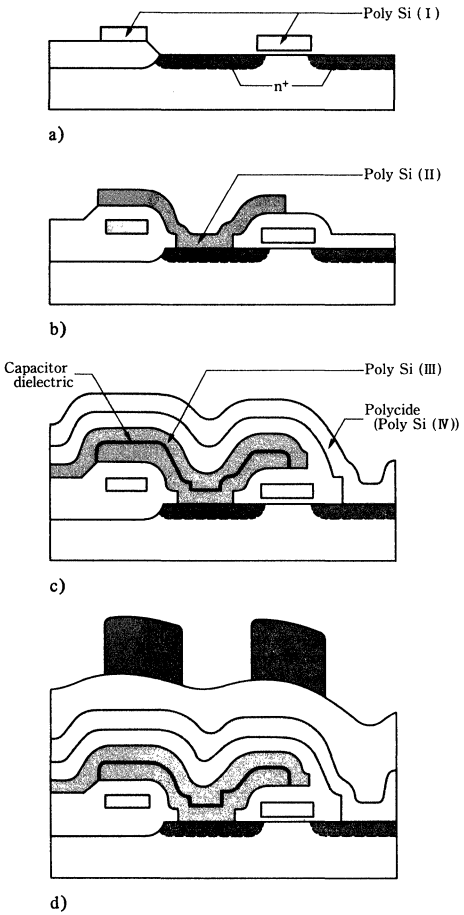

Fig. 12—Schematic veiw of 3D stacked capacitor cell and fabrication process.

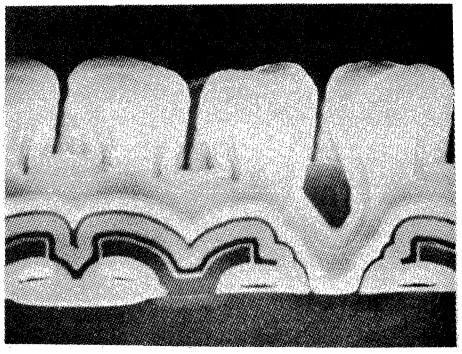

Fig. 13—SEM cross sectional view of 3D stacked capacitor cell.

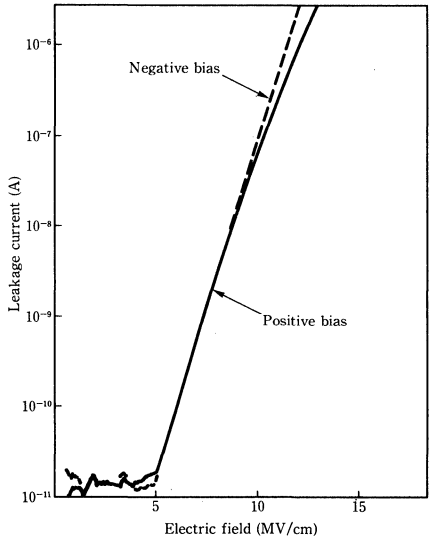

Fig. 14—Leakage current of capacitor film.

technique of producing accurate and defectless reticules were developed.

After the capacitor dielectric film is formed, the third poly-silicon layer for the cell plate is grown. After the oxide films between layers are grown, the bit line contact holes are opened and bit lines are formed by the fourth silicon layer (polycide) in Fig. 12c). Then, aluminum word lines are formed by the conventional method in Fig. 12d). Figure 13 shows the cross-sectional SEM view.

3.3.2 Capacitor dielectric film

A key technique of the process for the stacked capacitor cell is the formation of the capacitor dielectric film on the poly-silicon. The 4-Mbit DRAM requires a film thickness not more than10 nm (effective oxide thickness). There is also a physical limit for the silicon oxide film thickness. When the thickness becomes

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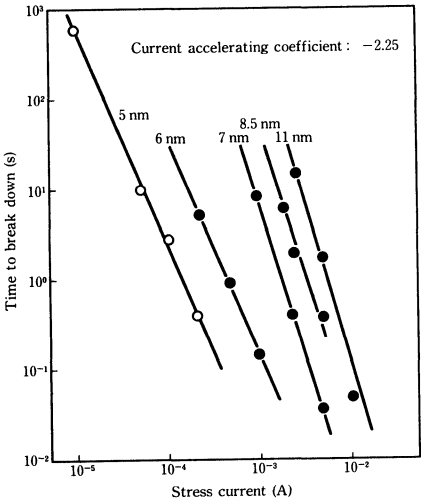


Fig. 15—Stress current on lifetime (0.1% cumulative failure).

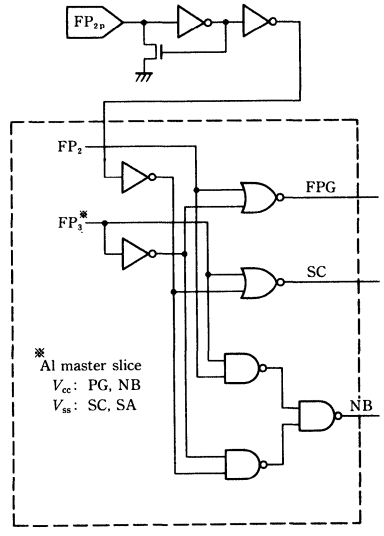


Fig. 16—Master slice/wire bond option control circuitry.

5 nm or less, the conductivity mechanism of the film is changed and its dielectric characteristics rapidly deteriorate. Therefore, the film cannot be thinner than this limit.

To determine the minimum limit of film thickness, I-V characteristics were measured as shown in Fig. 14 using a film 5 nm thick (effective oxide thickness) which is close to the physical limit, and by using a test pattern having a 40 mm^2 capacitor area and having the equivalent steps as a 4-Mbit DRAM. This measurement confirmed that the leakage current per cell under the device operating conditions is not more than 10^{-16} A.

In addition, the time dependent dielectric breakdown (TDDB) of the capacitor film was estimated by an accelerated test using constant-current stress (see Fig. 15). The operating life of the capacitor film calculated using the current acceleration factor obtained from the test result was essentially infinite even for a film thickness of 5 nm.

The results of these measurements showed that the capacitor dielectric film on the poly-silicon has sufficient charge retention characteristics and operating life even when its thickness is close to the physical limit. Consequently, a capacitor film having a 7 nm to 8 nm thickness was selected considering fluctuations in the production process.

4. Development of mega bit CMOS DRAM

4.1 Eight types of 1-Mbit DRAM on the same chip

This section explains the circuits and features of Fujitsu's CMOS DRAMs that use the three-dimensional stacked capacitor cell and CMOS peripheral circuits described in the preceding chapter.

The MB81C1000/1/2/3 series having 1-Mbit x 1-bit organization and the MB81C4256/7/8/9 series having 256-Kbit x 4-bit organization from eight different types of 1-Mbit DRAM are fabricated on the same bulk chip. The type of DRAM product is selected by means of the aluminum master-slice and wire bonding in the assembly step. Figure 16 shows the control circuit for these DRAMs. When PF_2 and FP_3 are pulled up to V_{CC} or down to V_{SS}, the FAST PAGE (FPG), NIBBLE (NB), STATIC COLUMN (SC),

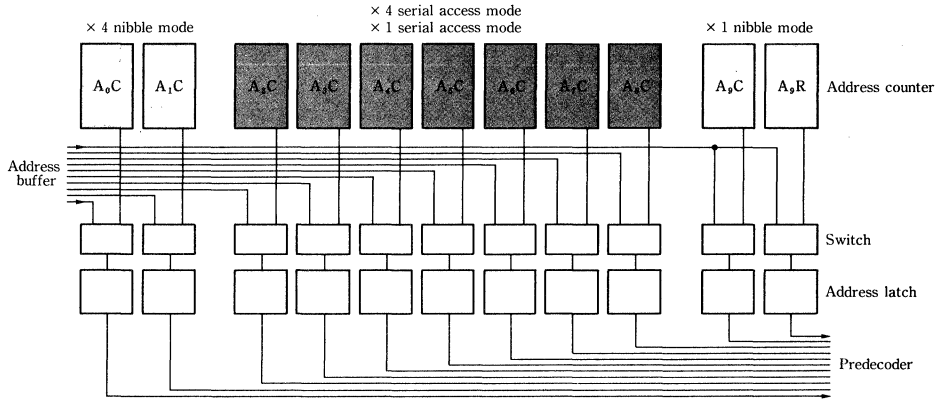
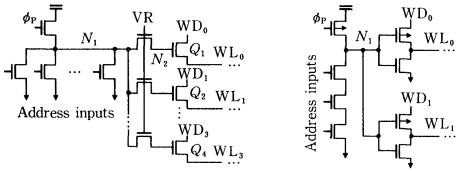


Fig. 17—Address counter block diagram for nibble mode and serial access mode.



a) Row decoder of 256-K DRAM

b) Row decoder of 1-M DRAM

Fig. 18—Compariosn of row decoder between nMOS and

or SERIAL ACCESS (SA) mode can be selected.

Figure 17 shows the address counter connections to provide the SA mode. In the 256-Kbit x 41-bit organization, continuous 2-Kbit data can be accessed at high speed by operating all counter bits A_0C to A_8C. If two low order bits of this counter are used, the NB mode can provided. In the 1-Mbit x 1-bit organization, the counter operation is the same as in the 256-Kbit x 4-bit organization except that the address boundary is A_0C to A_9C.

4.1.1 Power consumption

The MB81C1000 series uses a p-type substrate and n-well CMOS technology to provide low power consumption and high speed operation at the same time. Figure 18a) shows the circuit of the row decoders used in MB81256 based on conventional nMOS technology. During address decoding in MB81256, all other decoders, except the selected one, repeat charging and discharging at every memory cycle. In the MB81C1000 shown in Fig. 18b), only the selected 1-bit decoder repeats charging and discharging. All other decoders are in the standby state (NODE N_1 = H). Because of this feature, the gate capacitances of large transistors Q_1 to Q_4 are not charged and discharged every cycle, and unnecessary power consumption is avoided. Furthermore, ground noise and substrate noise caused by discharging can be eliminated, resulting in stable operation of the sense amplifier.

Because the reset level of the bit lines is set to about 1/2 V_{CC}, the charging and discharging current (which significantly affects the power consumption of the DRAM) is reduced to about 35 percent that of the conventional V_{CC} resetting method. In addition, each bit line is divided into four sections by the shared sense amplifiers located on both sides of the column decoder in the middle. This enables the elimination of charging and discharging bit lines that are not operated for reading and writing. With this design an effective reduction in power consumption is also achieved.

4.1.2 Reliability

Setting the bit line reset voltage to 1/2 V_{CC} results not only in low power consumption but also improved reliability.

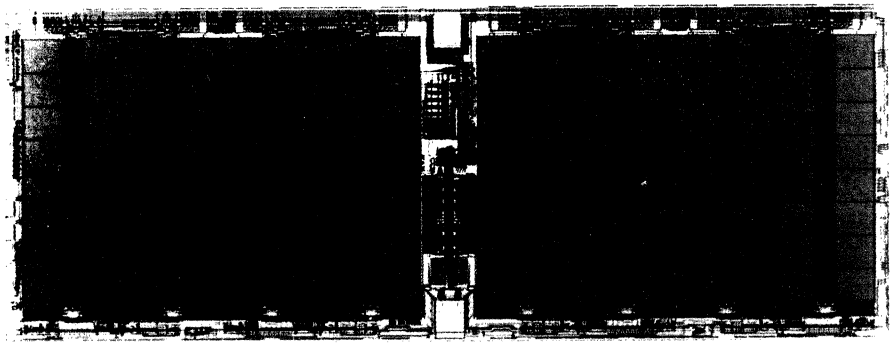


Fig. 19–Photomicrograph of 4M DRAM (Chip size is (4.92 x 13.22 mm^2).

First, by making the voltage potential of the bit line reset level equal to that of the capacitor plate of the cell, the electric field at the capacitor film is reduced by half. This enables the capacitor film to be much thinner, reduces alpha-particle-induced soft errors, and improves the time dependent dielectric breakdown (TDDB) of the capacitor film itself.

Second, the potential of the capacitor plate of the cell and the bit line reset voltage are set to follow the fluctuation in the power supply (V_{CC}). This stabilizes the read signal voltage to the sense amplifiers regardless of fluctuations in V_{CC}, and makes the device highly resistant to V_{CC} noise (V bump).

Third, boost circuits, including the word driver, can be eliminated and fully static circuits are used for all internal circuits. As a result, the memory not only has the advantageous feature of a CMOS circuit that is highly resistive to small leakage current, but also eliminates the characteristic degradation, including that due to hot carriers.

The fourth advantage of the 1/2 V_{CC} reset system is the reduction in the peak current of V_{CC} power supply. Excessive peak current causes noise which adversely affects memory device operation. This has frequently caused troubles in users' boards.

In the MB81C1000 series, the peak current is lowered to 100 mA or less by using the 1/2 V_{CC} reset system as well as other techniques, making it possible to produce a device easy to use.

4.2 Development of 4-Mbit DRAM MB814100/814400 series

A 4-Mbit DRAM that can be mounted in a 300 mil dual in-line package (DIP) has been developed[12] through the incorporation of a memory cell having the three-dimensional stacked capacitor structure using four-layers of poly-silicon and the scaling of CMOS devices. Figure 19 shows a photograph of the chip.

The major technical issue when mounting a 4-Mbit DRAM to a 300 mil DIP is how to assure the cell area under the restrictions imposed by the package while maintaining cell capacitance and immunity to alpha-particle-induced soft errors. Considering the immunity to alpha-particle-induced soft errors of the stacked capacitor cell, Fujitsu has set the cell area at 7.5 μm^2; this is the minimum reported cell area for 4-Mbit DRAM. This cell area was selected because it enables a chip area of less than 70 mm^2 and because the memory device can be mounted in a conventional package.

The development of the 4-Mbit DRAM MB814100/814400 series had three objectives:

1) Electric characteristics, including the alpha-particle-induced soft error rate, must be at least equivalent to those of existing DRAMs.

2) The 4-Mbit DRAM must be compatible with various packages and capable of being

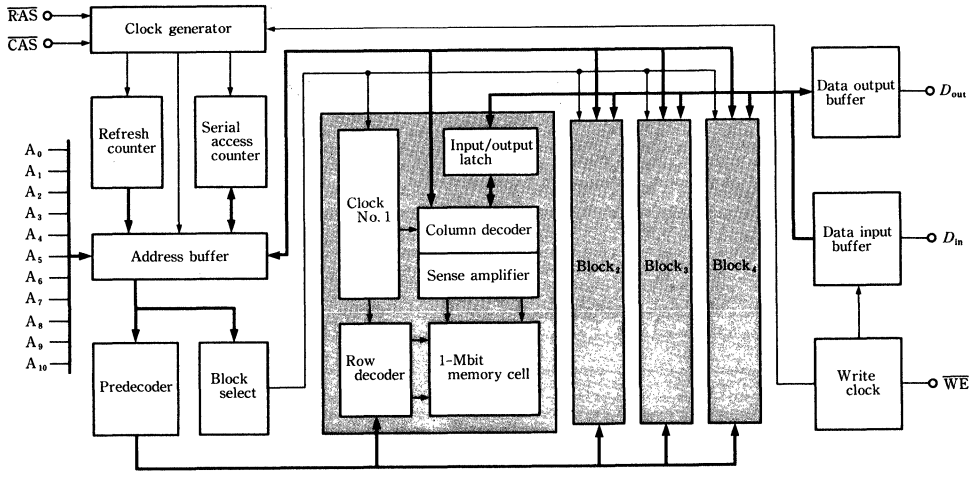


Fig. 20—Block diagram of 4M DRAM (Address clocks shape whole chip, but each 1-Mbit blocks has its own clock generator).

3) **High-quality and inexpensive memory must be supplied to users by using stacked capacitor cells which have already been mass produced.**

4.2.1 Design concept fo 4-Mbit DRAM

The chip area of the newly developed 4-Mbit DRAM is small (65 mm). It can be mounted not only to the 300 mil DIP but also to various packages such as the Small Outline J-leaded package (SOJ) and Zigzag In-line Package (ZIP) which have the same size as a 1-Mbit DRAM. The circuit design followed that of the 1-Mbit DRAM as much as possible, but with improved power consumption and operating speed. The design improvements are the 1/2 V_{CC} reset system for the cell plate and bit lines, determination of word x bit organization by wire bonding, and positioning of partial peripheral circuits in the middle of the chip.

For large-capacity DRAMs of 1-Mbit or more, the division of the memory cell array is very important for determining the overall characteristics of the DRAM. This is because the length of aluminum wiring in a chip is increased from 10 mm to 20 mm and the delay time in wiring becomes an important factor in the DRAM speed. In many cases, the power supply and ground line may receive the noise generated when all decoders and sense amplifiers in the array are operated at the same time. This restricts the margin of device operation. In addition, electro-migration must be considered in order to determine the power line width.

4.2.2 1-Mbit blocking organization

Because the sense amplifier pitch in the 4-Mbit DRAM can be reduced due to the use of polycide bit lines, 1024 sense amplifiers are positioned in an array in the *Y* direction (direction of shorter side). Therefore, the length of the shorter side of the chip is 4.84 mm; this is less than the maximum length for a plastic 300 mil DIP. A cell array of 1024 columns x 512 words (512 Kbits) is considered a unit. Eight blocks of this array are laid in the *X* direction (direction of longer side) to configure a 4-Mbit array. When compared with the 1-Mbit DRAM, the chip area of the 4-Mbit DRAM is increased by only 28 percent (comparison between Fujitsu products).

Although the bit line reset voltage is set to 1/2 V_{CC} to reduce the power consumption, the charging or discharging current of bit lines reaches 70 mA (t_{RC} = 180 ns) when all arrays of

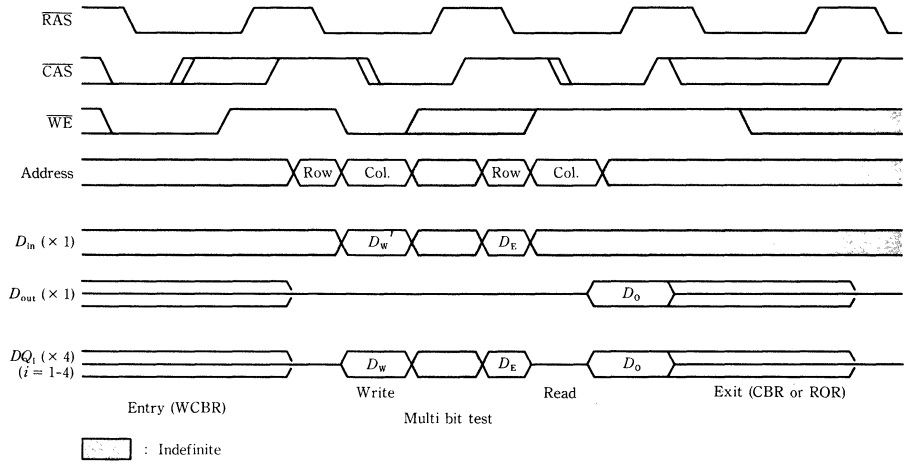


Fig. 21—Timing diagram of 16-bit multi bit test (D_W, D_R, D_E are write, read, expected data).

the 4-Mbit DRAM operate at the same time. In the 1-Mbit DRAM, the charge and discharge current were reduced to three-fourths of the conventional value through the divisional driving of arrays. In the 4-Mbit DRAM, only one-fourth of the arrays are driven and the current consumption by bit lines is reduced to about 18 mA. After current consumption by arrays is reduced, the power consumption of peripheral circuits becomes the next problem.

The increase in power consumption due to the increase of DRAM capacitance, and the deterioration in access time due to the wiring delay time have been suppressed by improving the DRAM performance through the scaling of the transistor size. However, for a large capacity of 4-Mbits, the improvement in memory device performance made only by scaling the transistor is approaching its limit. This is because the wiring delay time becomes the dominant performance factor as described before.

To solve this problem, the blocking of circuits, including peripheral circuits, is used and the power delay product in the peripheral circuits is greatly improved (see Fig. 20). A 1-Mbit array containing a cell array and a clock generator circuit to drive the array is considered a unit block. The 4-Mbit memory is configured by four such blocks. During normal reading or writing, only the selected 1-Mbit block is operated. Consequently, the chip can maintain high speed and low power consumption because it operates under an internal load as small as that of a 1-Mbit DRAM.

4.2.3 Test mode

Since the development of the 1-Mbit DRAM, the issue of increasing the test time as the memory capacity increases has arisen. This is a serious problem even for the 4-Mbit DRAM. For example, when a DRAM of 4-Mbit x 1-organization is tested with a cycle time of 300 ns, a test time of about 15 s is required even when a simple marching pattern is used. For the 1-Mbit DRAM, the parallel test mode is activated by applying a voltage higher than V_{CC} to the Test Enable (TE) pin which used to be an NC pin. However, for the 4-Mbit DRAM, reduction of the test time is strongly desired at the board level and there is no unused pin. Therefore, the 4-Mbit DRAM is designed to have an 8-bit parallel test mode controlled by the TTL logic input.

Table 2 lists the test functions employed for the 4-Mbit DRAM. Figure 21 shows their timing charts. The parallel test mode entry is done by

Table 2. Function of Multi bit test

Organization	Test entry	Test exit	Result	No. of MBT
4-M x 1	WE, CAS before RAS (WCBR)	CAS before RAS or RAS only refrech	Pass = 1 Fail = 0 from D_{out}	8
1-M x 4	Ditto above		Pass = 1 Fail = 0 from DOs	8

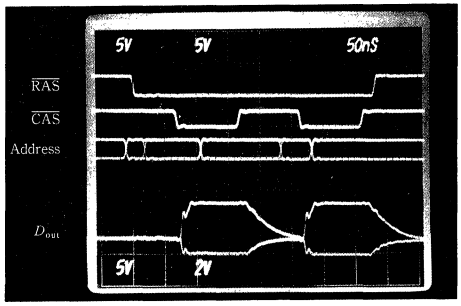


Fig. 22—Output wave form operating in a fast page mode.

the WE, CAS before RAS (WCBR) cycle. The exit cycle is done by the RAS only refresh or CAS before RAS cycle. During test mode operation, refresh can be executed in either the simple read cycle or WCBR entry cycle.

For the test result output, the D_{out} pin outputs "1" for "pass" when all data of the eight parallel read bits matches, and "0" for "fail" when at least one bit of data does not match. The 3-state output method which uses a high impedance state for test result output is not used, thus the test can be executed easily on the board.

4.3 Characteristics of 4-Mbit DRAM

The 4-Mbit DRAM designed as described above operates at high speed with low power consumption. Figure 22 shows the output waveform of the DRAM in the fast page mode. The measurement conditions are: power voltage V_{CC} is 5 V, ambient temperature is 25 °C, and RAS-CAS delay time t_{RCD} is $t_{RCD_{max}}$. As shown in the figure, the RAS access time is typically 56 ns. This is faster than that of 256-Kbit and 1-Mbit DRAMs.

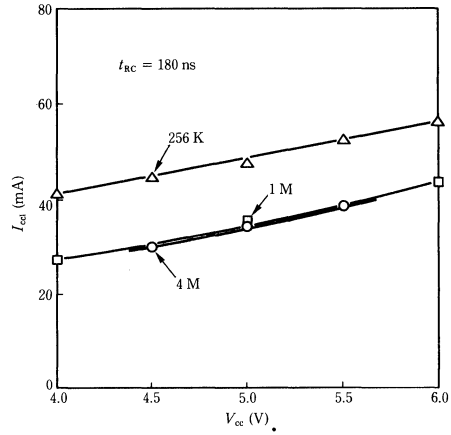


Fig. 23—Average V_{CC} current (I_{CC1}) vs V_{CC} voltage.

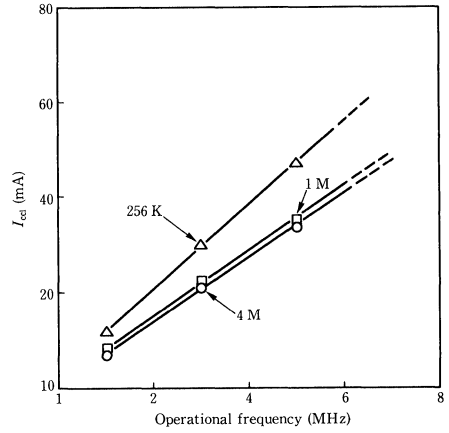


Fig. 24—Average V_{CC} current (I_{CC1}) vs operational frequency.

Figure 23 shows the average operating current (V_{CC}) dependency of the power voltage (I_{CC1}). Figure 24 shows the cycle time dependency of I_{CC1}. For reference, data of a 4-Mbit DRAM is compared with data of a 256-Kbit DRAM (MB81256) using nMOS technology. Under typical conditions, the operating current of the 4-Mbit DRAM is 34 mA, while that of the 256-Kbit

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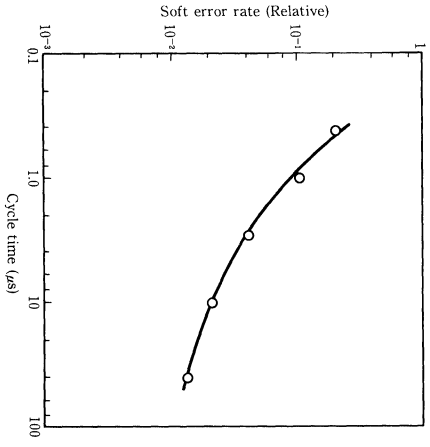

Fig. 25 – Accelerated alpha particle induced soft error result.

DRAM is 48 mA. The comparison reveals a large reduction in the operating current. This results from the array division. The memory cell array is divided into eight sections and configured in four blocks consisting of independent 1-Mbit blocks, including the peripheral circuits to drive the arrays.

The 4-Mbit DRAM has the same power consumption as a 1-Mbit DRAM because it executes operations equivalent to that of a 1-Mbit DRAM using its internal circuits, including peripheral circuits. This is a large advantage for PC board assembly. The memory board capacity can be increased four times by using the 4-Mbit DRAM without changing the power supply or cooling system.

The peak current of the 4-Mbit DRAM is rather low (100 mA) compared to a 256-Kbit DRAM.

Reduction of the alpha-particle-induced soft error rate is a large problem if the reliability of mega-bit DRAMs is to be increased. Figure 25 shows an example of the test results for soft errors using an accelerated test. In this test, alpha rays were irradiated onto the chip surface and the soft error rate was measured while altering the DRAM operation cycle time. As shown in the figure, the major cause of soft errors is the bit line mode. Few soft errors are observed in the cell mode partly because only a small charge is collected by the stacked capacitor cell[13]: It has already been confirmed that the soft error rate of the 4-Mbit DRAM is lower than that of the 1-Mbit DRAM because of the scaling of the p-n junction area[14].

Regarding the packages for the MB814100/814400 series, the 300 x 675 mil^2 SOJ can be used as described previously. In addition, new 300 mil DIP and 400 mil ZIP are under development. The JEDEC standard for the 4-Mbit DRAM package has not yet been established (except 350 x 675 mil^2 SOJ) because of the large restriction imposed by the various chip sizes of different manufacturers. If the JEDEC standard is established, Fujitsu will develop the corresponding package. In addition, Fujitsu plans to study the possibility of using a 300 mil SOJ having compatibility with a 1-Mbit DRAM in order to realize a single in-line module (SIM) mounted with 4-Mbit DRAM.

5. Future objectives

Currently, 1-Mbit DRAMs are mass-produced, 4-Mbit DRAMs are being accepted in the market, and the concept of 16-Mbit DRAMs is being considered. In this age of mega-bit capacities, the device and process technologies are changing rapidly.

As the process technology improves, a new concept of memory cell technology is required. Fujitsu plans to promote the further miniaturization of stacked capacitor cells to be used for 16-Mbit DRAM memory cells.

As part of this advance in technology, Fujitsu presented a DIET capacitor cell at IEDM in 1986. DIET combines the advantages of both the stacked cell and trench cell. It can theoretically achieve a large cell capacitance and could be realized by burying a three-dimensional capacitor cell into an insulated trench capsule. In addition, a system to supply cell-plate voltage from the capsule layer in the substrate has been developed. To supply cell-plate voltage from inside

the substrate is a new system.

As shown by the above discussion, the process technology to realize a new memory cell must be found by trying various process technologies and looking at all possibilities. Such methods of development do not determine one choice only, but also expand the overall potential. Fujitsu will continue to develop the technologies for those device designs that respond to the diverse needs of the market.

In device technology, Fujitsu plans to develop products having added value and more functions in the field of ASICs (including video products) that are based on the general purpose products described in this report. Fujitsu will continue to introduce high-quality, high-performance devices for the market.

6. Conclusion

Quadruple integration every three years has still been maintained in the Mega bit era. The 3D STC was the key technology for this steady progress of DRAM development. To develop this type of DRAM cell, overall process design was needed, such as fine lithography, ultra thin capacitor film, cell capacitance, and α-immune cell structure.

Combining the high performance CMOS DRAM circuits with the STC cell technology, we developed the industry's smallest 4-Mbit DRAM having an access time of 56 ns.

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FUJITSU LIMITED

Marunouchi Headquarters
6-1, Marunouchi 1-chome
Chiyoda-ku, Tokyo 100, Japan
Tel: (03) 216-3211
Telex: 781-22833
FAX: (03) 213-7174

For further information, please contact:

Japan

FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
6-1, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Tel: (03) 3216-3211
Telex: 781-2224361
FAX: (03) 3211-3987

Europe

FUJITSU MIKROELEKTRONIK GmbH
Lyoner Strasse 44-48
Arabella Centre 9. 0G
D-6000 Frankfurt 71
Federal Republic of Germany
Tel: (49) (069) 66320
Telex: 411-963
FAX: (069) 663-2122

Asia

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
06-04/06-07 Plaza By the Park
No. 52 Bras Basah Road
Singapore 0718
Tel: (65) 336-1600
Telex: 55573
FAX: (65) 336-1609

North and South America

FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street
San Jose, CA 95134-1804 USA
Tel: (408) 922-9000
Telex: 910-338-0190
FAX: (408) 432-9044

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