Data Book

ECL RAM Products

1990

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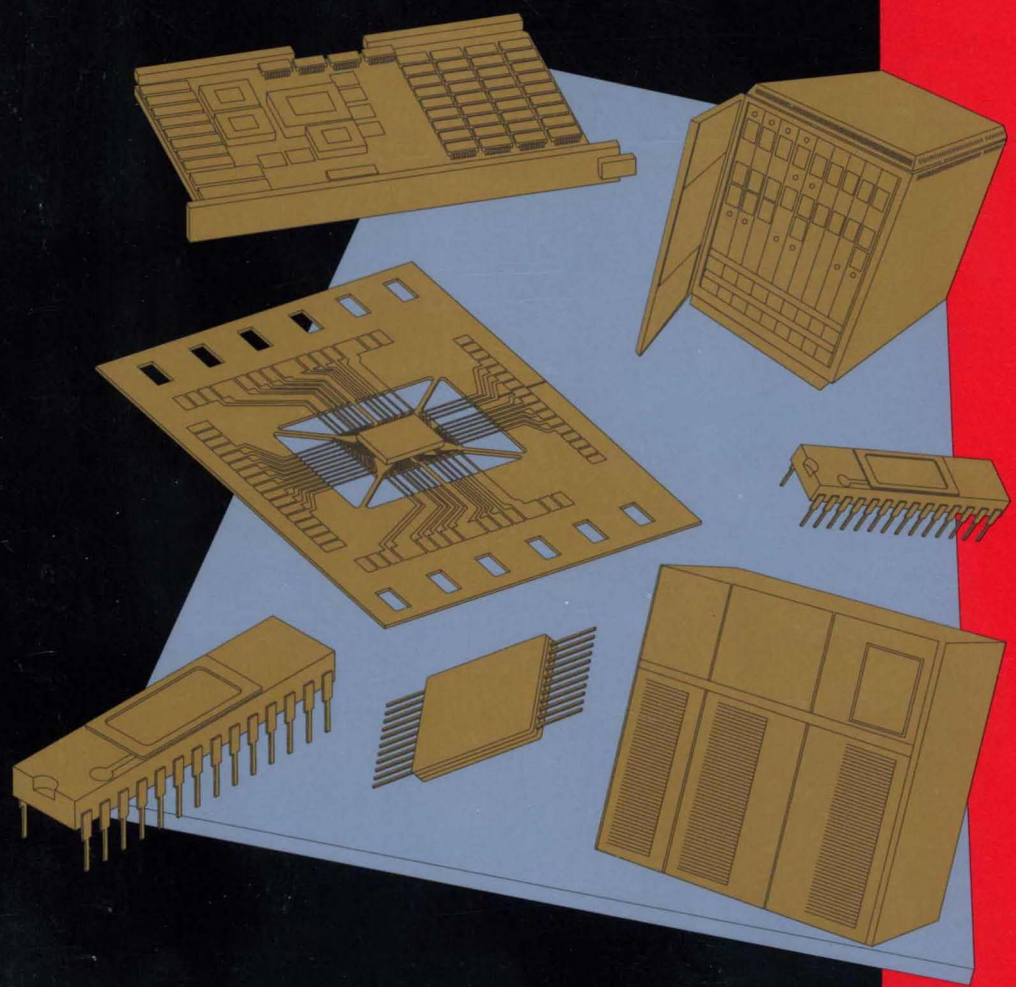
DATA
BOOK



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ECL RAM Products

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Edition 1.0

Contents and Alphanumeric Product List

ECL RAM Products

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ECL RAM Products

Contents and Alphanumeric Product List (Continued)

ECL RAM PRODUCTS

Contents and Alphanumeric Product List (Continued)

ECL RAM PRODUCTS

Alphanumeric List of Fujitsu Part Numbers

Introduction

Fujitsu's ECL RAM Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high–speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic RAMs.

The ECL RAM product line offers devices for use in a wide range of applications. These memories are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

This data book includes product information on the following DRAM products:

ECL and TTL Bipolar RAMs

FMI currently offers fast ECL I/O RAMs ranging in density from 1K to 256K. The pure ECL RAMs are available in the following organizations: 512 x 4 to 16K x 4 and 4K x 1 to 64K x 1. Fujitsu has the fastest pure ECL RAMs available, with speeds as fast as 3 ns, 5 ns, and 7 ns for 4K, 16K, and 64K densities, respectively.

BiCMOS ECL RAMs

Fujitsu offers BiCMOS ECL I/O RAMs in both 64K and 256K densities. The 64K devices are pin compatible with the pure ECL devices and are also offered in 16K x 4 and 64K x 1 organizations. The 256K BiCMOS ECL I/O RAMs have both the x1 and x4 organizations and have a T_{AA} of 15 ns maximum.

Application Specific RAMs

To address the increasing system speed of high performance mainframes and minicomputers, Fujitsu is improving access time with process improvements on conventional ECL RAMs. Fujitsu has also addressed timing problems associated with conventional RAMs. Self-timed RAMs (STRAMs) are pipelined memory devices that shrink access times, cut board space and reduce the number of connections between discrete parts.

ECL RAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
1–3	MBM10422A–5	5	1024 bits	24-pin Ceramic DIP, FPT
	–7	7	(256w x 4b)	24-pad Ceramic LCC
1–9	MBM100422A–5	5	1024 bits	24-pin Ceramic DIP, FPT
	–7	7	(256w x 4b)	24-pad Ceramic LCC
1–17	MBM10470A–7	7	4096 bits	18-pin Ceramic DIP, FPT
			(4096w x 1b)	18-pad Ceramic LCC
1–27	MBM100470A–7	7	4096 bits	18-pin Ceramic DIP, FPT
			(4096w x 1b)	18-pad Ceramic LCC
1–37	MBM10470A–10	10	4096 bits	18-pin Ceramic DIP, FPT
	–15	15	(4096w x 1b)	18-pad Ceramic LCC
	–20	20		
1–47	MBM100470A–10	10	4096 bits	18-pin Ceramic DIP, FPT
	–15	15	(4096w x 1b)	18-pad Ceramic LCC
1–57	MBM10A474–3	3	4096 bits	24-pin Ceramic DIP, FPT
			(1024w x 4b)	
1–65	MBM101474A–3	3	4096 bits	24-pin Ceramic DIP, FPT
			(1024w x 4b)	
1–73	MBM10474A–5	5	4096 bits	24-pin Ceramic DIP, FPT
	–7	7	(1024w x 4b)	24-pad Ceramic LCC
1–83	MBM100474A–5	5	4096 bits	24-pin Ceramic DIP, FPT
	–7	7	(1024w x 4b)	24-pad Ceramic LCC
1–93	MBM10474A–10	10	4096 bits	24-pin Ceramic DIP, FPT
	–15	15	(1024w x 4b)	24-pad Ceramic LCC
1–103	MBM100474A–10	10	4096 bits	24-pin Ceramic DIP, FPT
	–15	15	(1024w x 4b)	24-pad Ceramic LCC
1–113	MBM10480A–8	8	16384 bits	20-pin Ceramic DIP, FPT
			(16384w x 1b)	20-pad Ceramic LCC
1–123	MBM100480A–8	8	16384 bits	20-pin Ceramic DIP, FPT
			(16384w x 1b)	20-pad Ceramic LCC
1–133	MBM10480A–10	10	16384 bits	20-pin Ceramic DIP, FPT
			(16384w x 1b)	20-pad Ceramic LCC
1–143	MBM100480A–10	10	16384 bits	20-pin Ceramic DI, FPTP
			(16384w x 1b)	20-pad Ceramic LCC
1–153	MBM10480–15	15	16384 bits	20-pin Ceramic DIP, FPT
	–25	25	(16384w x 1b)	20-pad Ceramic LCC
1–165	MBM100480–15	15	16384 bits	20-pin Ceramic DIP, FPT
	–25	25	(16384w x 1b)	20-pad Ceramic LCC
1–177	MBM10A484–5	5	16384 bits	28-pin Ceramic DIP, FPT
			(4096w x 4b)	
1–185	MBM101A484-5	5	16384 bits	28-pin Ceramic DIP, FPT
			(4096w x 4b)	

ECL RAMs — *At a Glance* (Continued)

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
1–193	MBM10484A–8	8	16384 bits (4096w x 4b)	28-pin Ceramic DIP, FPT 28-pad Ceramic LCC
1–203	MBM100484A–8	8	16384 bits (4096w x 4b)	28-pin Ceramic DIP, FPT 28-pad Ceramic LCC
1–213	MBM10484A–10	10	16384 bits (4096w x 4b)	28-pin Ceramic DIP, FPT 28-pad Ceramic LCC
1–225	MBM100484A–10	10	16384 bits (4096w x 4b)	28-pin Ceramic DIP, FPT 28-pad Ceramic LCC
1–237	MBM10484–15	15	16384 bits (4096w x 4b)	28-pin Ceramic DIP, FPT
1–245	MBM100484–15	15	16384 bits (4096w x 4b)	28-pin Ceramic DIP, FPT
1–253	MBM10490–15 –25	15 25	65536 bits (65536w x 1b)	22-pin Ceramic DIP, FPT
1–261	MBM100490–15 –25	15 25	65536 bits (65536w x 1b)	22-pin Ceramic DIP, FPT
1–269	MBM10494–7 –8	7 8	65536 bits (16384w x 4b)	28-pin Ceramic DIP, FPT
1–277	MBM101494–7 –8	7 8	65536 bits (16384w x 4b)	28-pin Ceramic DIP, FPT

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10422A-5
MBM 10422A-7

April 1986
Edition 3.0

1

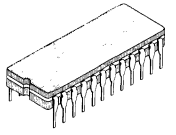
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10422A is fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

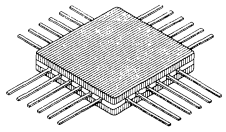
The MBM 10422A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10422A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 256 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 5 ns max. (MBM 10422A-5)
  7 ns max. (MBM 10422A-7)
- Block select access time: 3 ns max. (MBM 10422A-5)
  4 ns max. (MBM 10422A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.7 mW/bit typ.
- DOPOS and IOP-II processing
- Pin compatible with the F10422



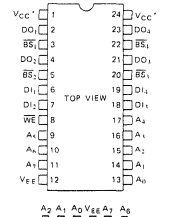
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 9

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 9

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

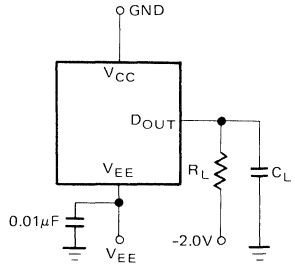
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

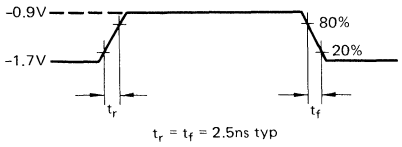
Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ± 5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

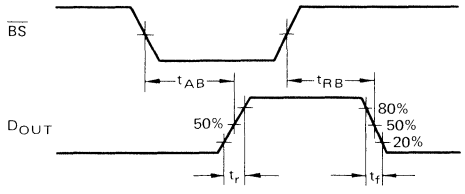
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

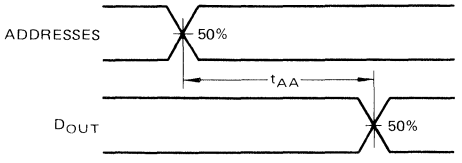
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10422A-5			MBM 10422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			5		5	7	ns
Block Select Access Time	t_{AB}			3		2.5	4	ns
Block Select Recovery Time	t_{RB}			3		2.5	4	ns

READ CYCLE TIMING DIAGRAMS

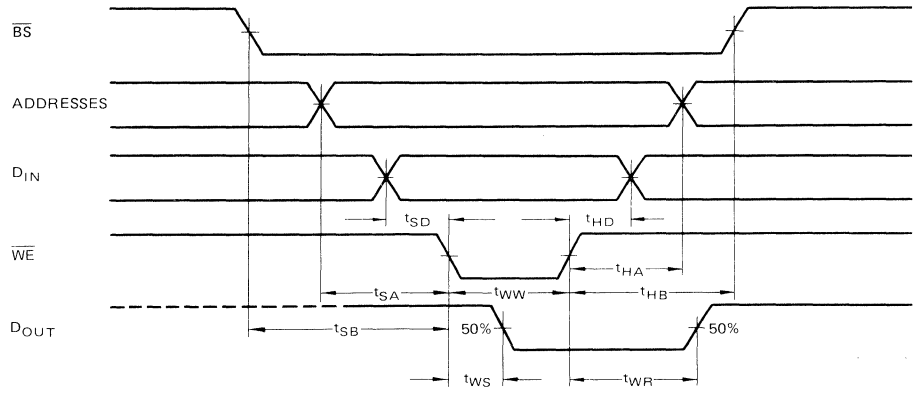




WRITE CYCLE

Parameter	Symbol	MBM 10422A-5			MBM 10422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	3.5			5			ns
Write Disable Time	t_{WS}			3.5			4	ns
Write Recovery Time	t_{WR}			3.5			8	ns
Address Set Up Time	t_{SA}	0.5			1			ns
Block Select Set Up Time	t_{SB}	0.5			1			ns
Data Set Up Time	t_{SD}	0.5			1			ns
Address Hold Time	t_{HA}	1.0			1			ns
Block Select Hold Time	t_{HB}	1.0			1			ns
Data Hold Time	t_{HD}	1.0			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

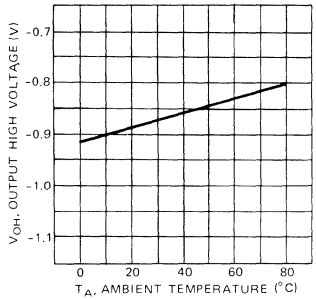


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

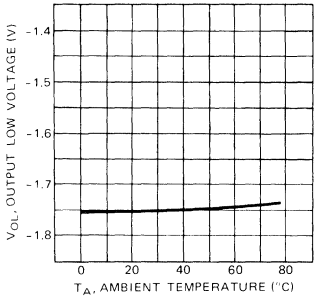


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

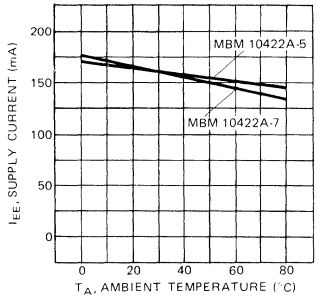


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

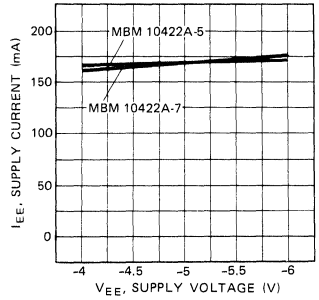


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

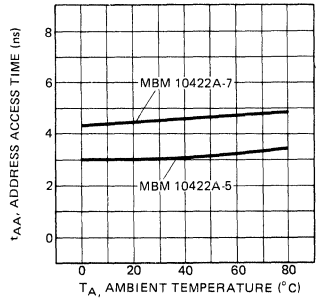


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

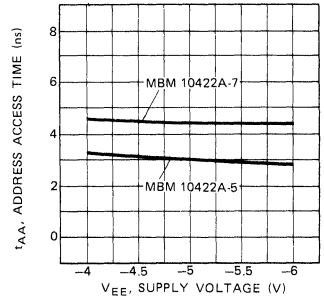


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

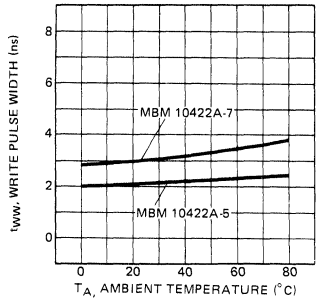
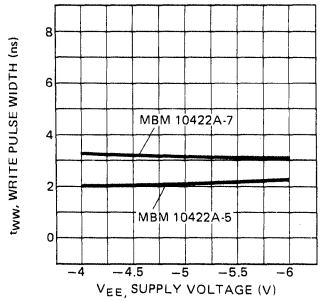


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

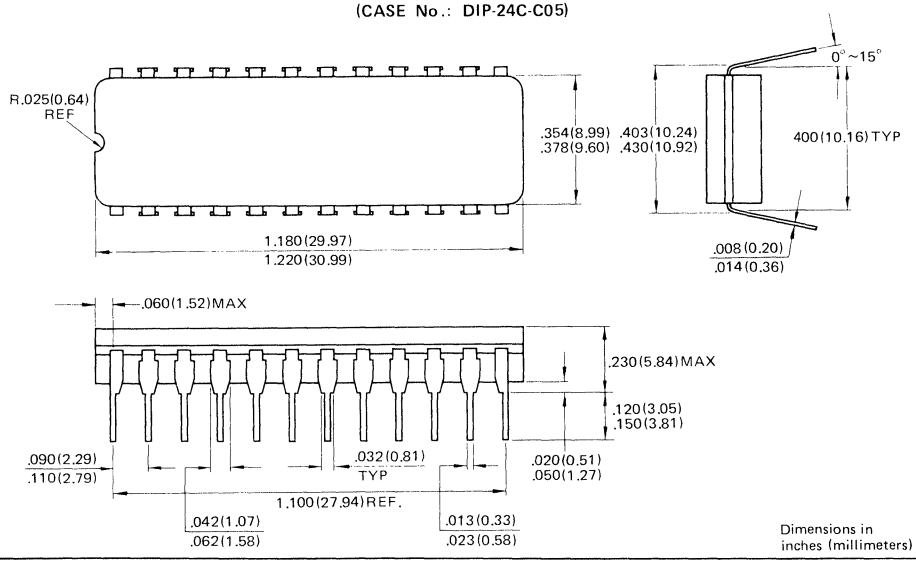


1

PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

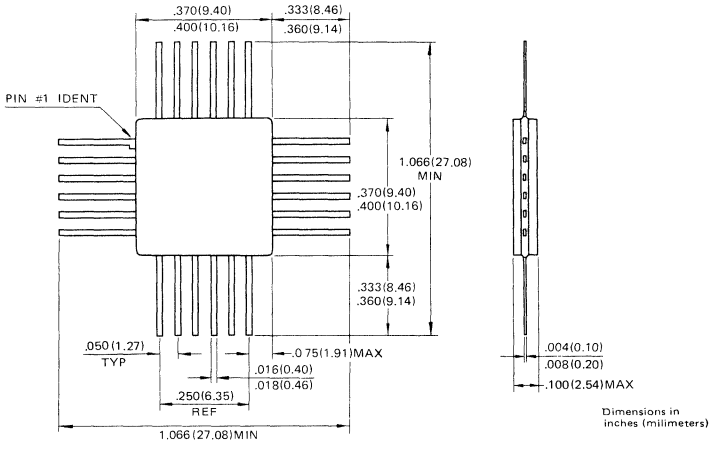
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



Dimensions in inches (millimeters)

CERAMIC FPT (: -ZF)

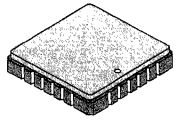
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



Dimensions in inches (millimeters)

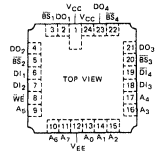
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)



LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
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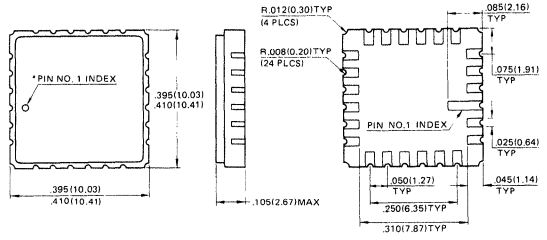


*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100422A-5
MBM 100422A-7

April 1987
Edition 3.0

1

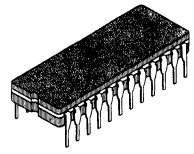
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100422A is fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

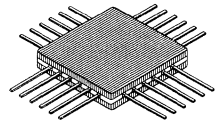
The MBM 100422A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 100422A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 256 words x 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K-series ECL families
- Address access time: 5 ns max. (MBM 100422A-5)
  7 ns max. (MBM 100422A-7)
- Block select access time: 3 ns max. (MBM 100422A-5)
  4 ns max. (MBM 100422A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.7mW/bit
- DOPOS and IOP-II processing.
- Pin compatible with the F100422.



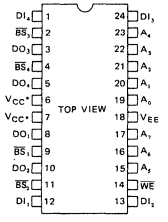
CERAMIC PACKAGE
DIP-24C-C05

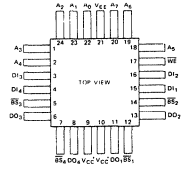


CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 8

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 8

ABSOLUTE MAXIMUM RATINGS (See NOTE)

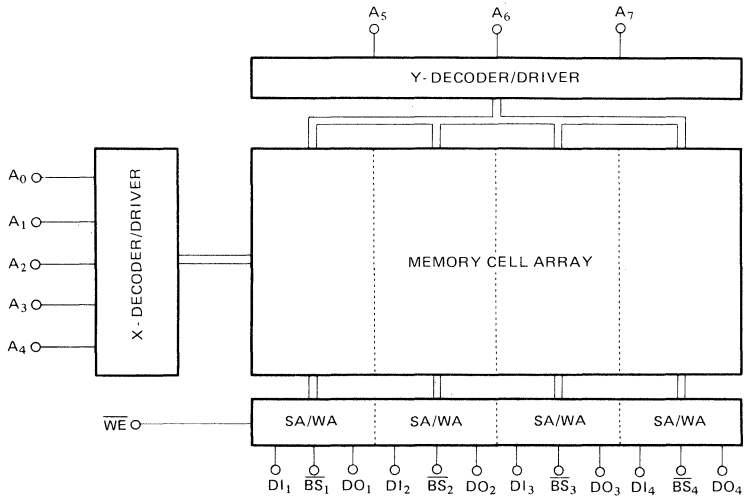
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A for DIP	−55 to +125	°C
	T_C for Flat Package and LCC		
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100422A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100422A is fully decoded 1024-bit read/write random access memory organized as 256 words by 4 bits. Memory cell selection is achieved by means of a 8-bit address designated A_0 through A_7. The active low Block Select ($\overline{BS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{BS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Value			Unit	Ambient Temperature for DIP Case Temperature for Flat Package and LCC
		Min	Typ	Max		
Supply Voltage	V	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V, T_A = 0°C to 85°C for DIP, Air flow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output High Voltage (V_{IN} = $V_{IH\,max}$ or $V_{IL\,min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\,max}$ or $V_{IL\,min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\,min}$ or $V_{IL\,max}$)	V_{OHC}	-1035			mV
Output Low Voltage · (V_{IN} = $V_{IH\,min}$ or $V_{IL\,max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\,max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\,min}$)	I_{IL}	-50			μA
$\overline{BS}$ Input Low Current (V_{IN} = $V_{IL\,min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-200			mA

CAPACITANCE

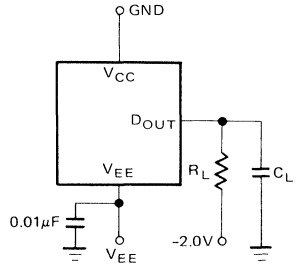
Parameter	Symbol	MBM 100422A-5			MBM 100422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Pin Capacitance	C_{IN}			6			5	pF
Output Pin Capacitance	C_{OUT}			7			8	pF

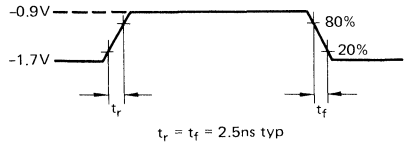
1

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ± 5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Air flow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

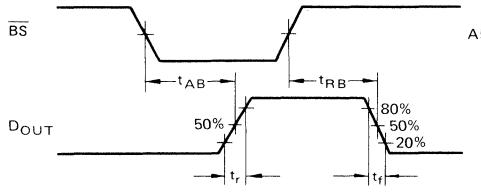
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

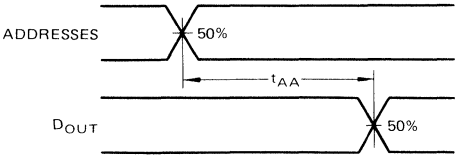
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100422A-5			MBM 100422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	1.5		5			7	ns
Block Select Access Time	t_{AB}	0.5		3			4	ns
Block Select Recovery Time	t_{RB}	0.5		3			4	ns

READ CYCLE TIMING DIAGRAMS

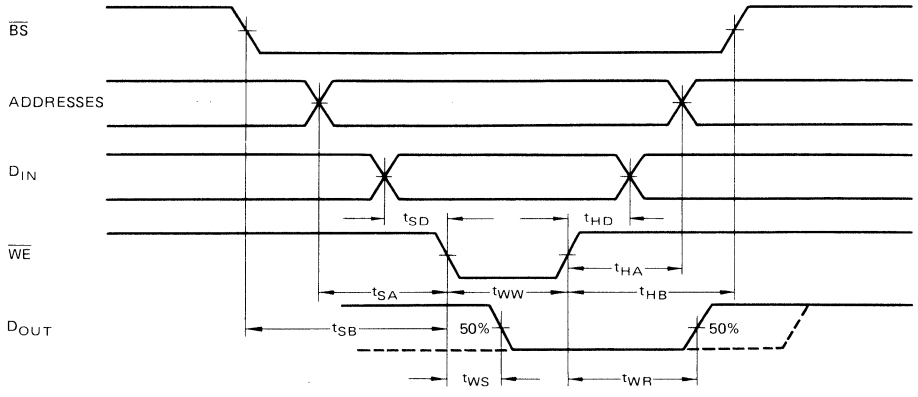




WRITE CYCLE

Parameter	Symbol	MBM 100422A-5			MBM 100422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	3.5			5			ns
Write Disable Time	t_{WS}	0.5		3.5			4	ns
Write Recovery Time	t_{WR}	0.5		3.5			8	ns
Address Set Up Time	t_{SA}	0.5			1			ns
Block Select Set Up Time	t_{SB}	0.5			1			ns
Data Set Up Time	t_{SD}	0.5			1			ns
Address Hold Time	t_{HA}	1.0			1			ns
Block Select Hold Time	t_{HB}	1.0			1			ns
Data Hold Time	t_{HD}	1.0			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

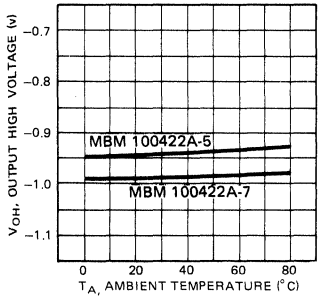


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

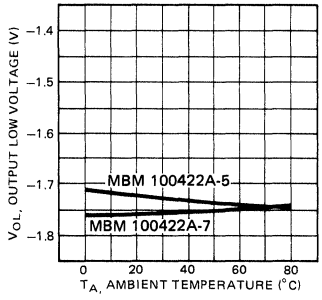


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

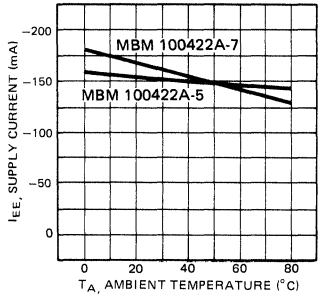


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

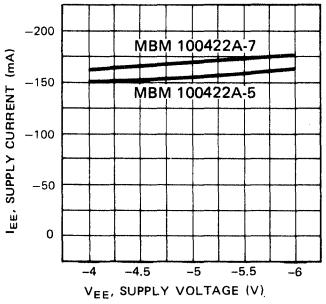


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

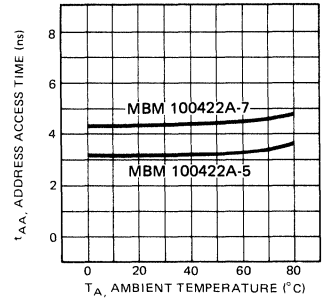


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

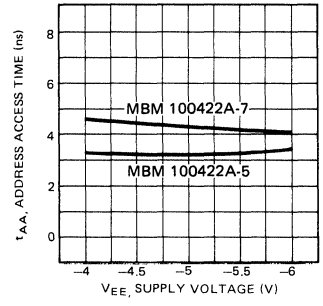


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

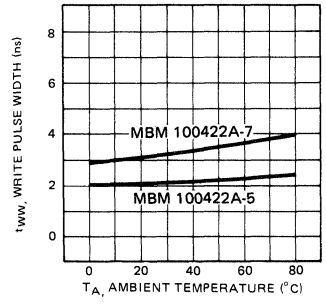
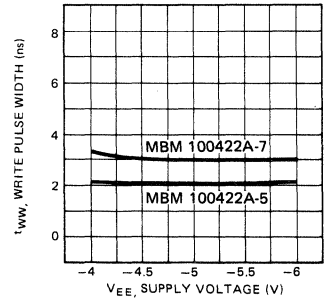


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

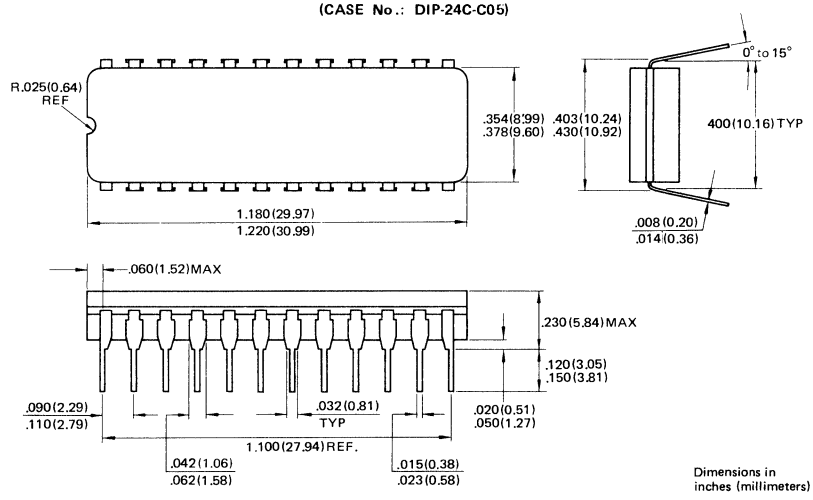


1

PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

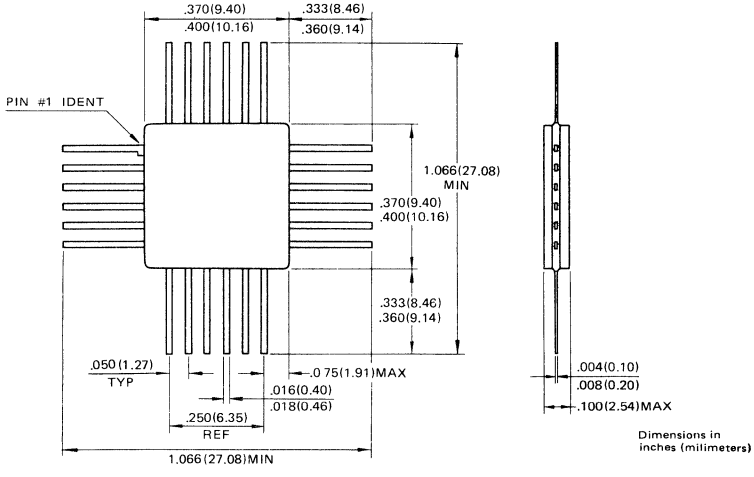
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



Dimensions in inches (millimeters)

CERAMIC FPT (: -ZF)

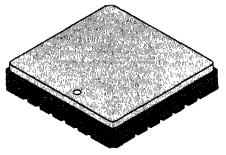
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



Dimensions in inches (milimeters)

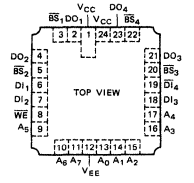
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

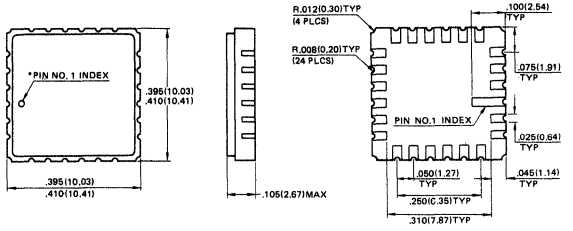


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10470A-7

August 1988
Edition 1.0

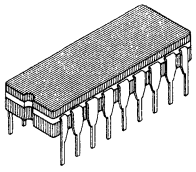
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10470A is a fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage compensation for improved noise margin.

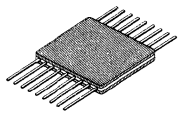
The MBM10470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10470A is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time :7 ns max.
- Chip select access time :3.5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation :0.22 mW/bit (typ.)
- DOPOS and IOP-II processing
- Pin compatible with the F10470



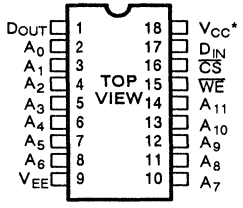
CERAMIC PACKAGE
DIP-18C-C01

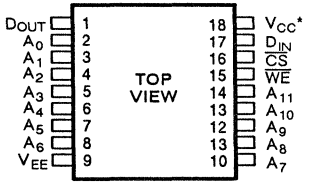


CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01 See Page 10

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 10

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

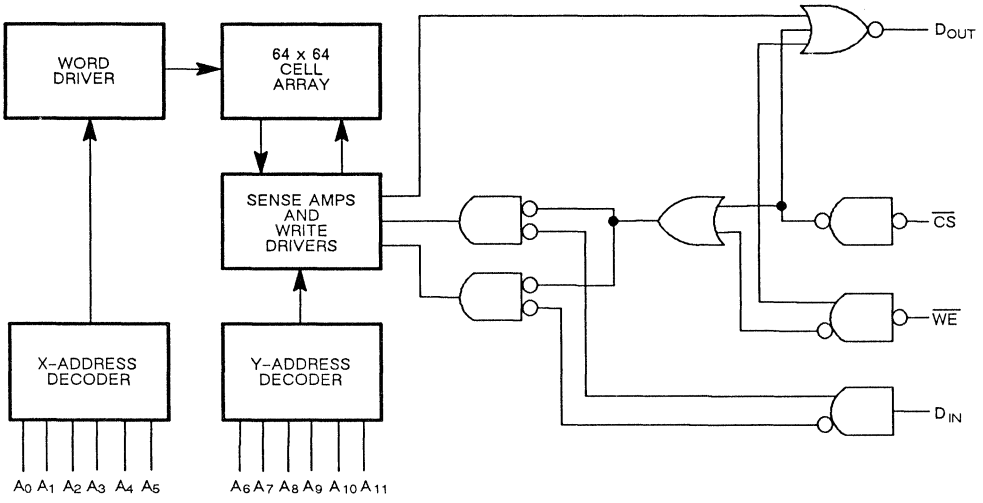
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

1

Fig. 1 — MBM10470A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0 °C 25 °C 75 °C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0 °C 25 °C 75 °C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OHC}	-1020 -980 -920			mV	0 °C 25 °C 75 °C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OLC}			-1645 -1630 -1605	mV	0 °C 25 °C 75 °C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0 °C 25 °C 75 °C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0 °C 25 °C 75 °C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			-220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-200			mA	0°C to 75°C

CAPACITANCE

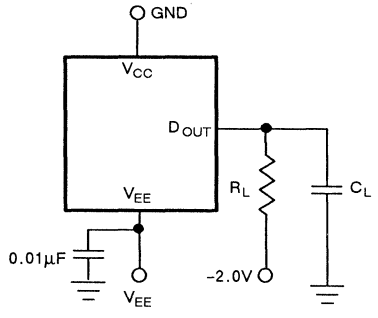
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

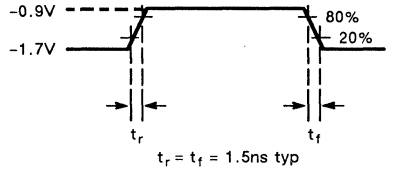
1

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V ±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITION





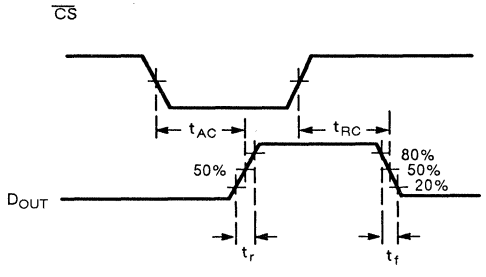
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

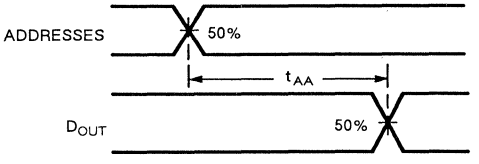
Note: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10470A-7			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}			7	ns
Chip Select Access Time	t_{AC}			3.5	ns
Chip Select Recovery Time	t_{RC}			3.5	ns

READ CYCLE TIMING DIAGRAMS

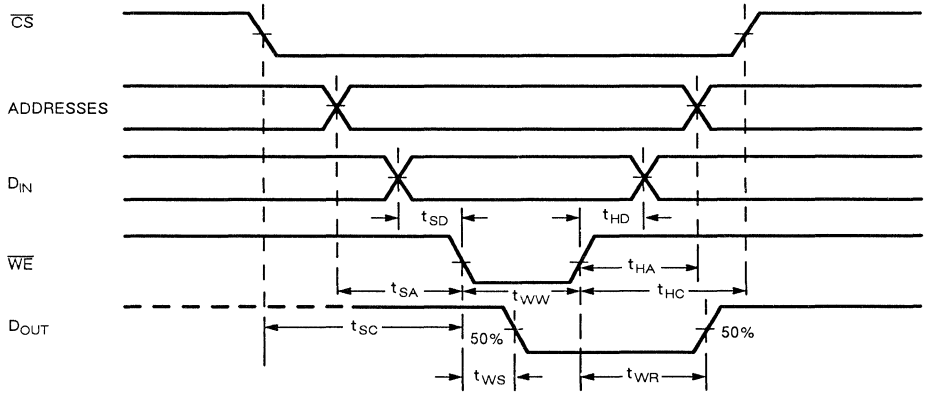




WRITE CYCLE

Parameter	Symbol	MBM10470A-7			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	7			ns
Write Disable Time	t_{WS}			3.5	ns
Write Recovery Time	t_{WR}			8	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	0			ns
Data Set Up Time	t_{SD}	0			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	0			ns
Data Hold Time	t_{HD}	0			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	MBM10470A-7			Unit
		Min	Typ	Max	
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 3 – OUTPUT HIGH VOLTAGE VS AMBIENT TEMPERATURE

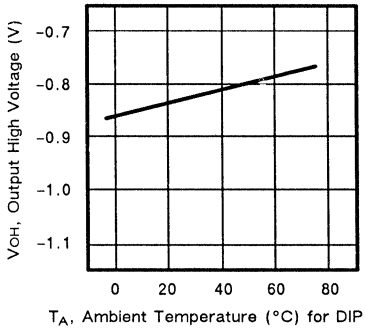


FIG. 4 – OUTPUT HIGH VOLTAGE VS SUPPLY VOLTAGE

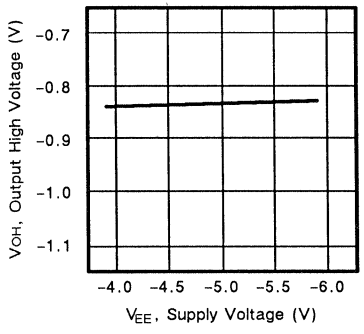


FIG. 5 – OUTPUT LOW VOLTAGE VS AMBIENT TEMPERATURE

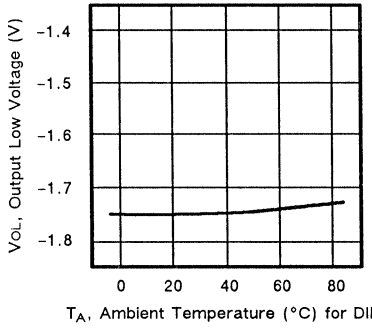


FIG. 6 – OUTPUT LOW VOLTAGE VS SUPPLY VOLTAGE

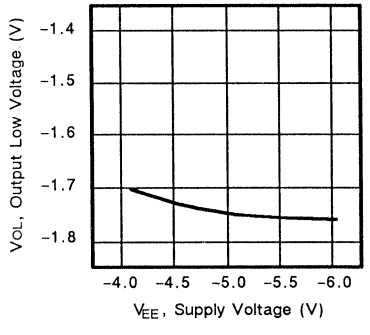
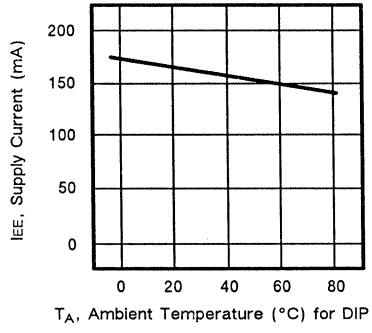


FIG. 7 – SUPPLY CURRENT VS AMBIENT TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 8 – ADDRESS ACCESS TIME VS AMBIENT TEMPERATURE

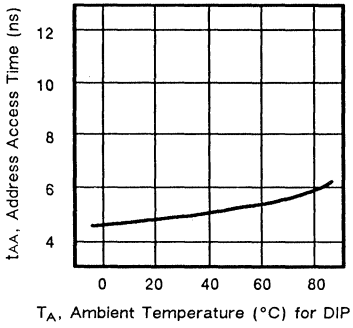


FIG. 9 – ADDRESS ACCESS TIME VS SUPPLY VOLTAGE

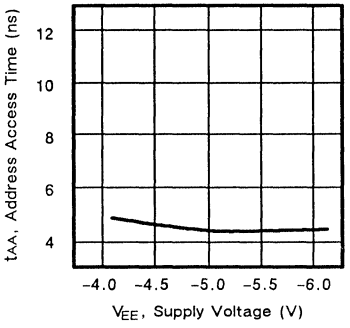


FIG. 10 – WRITE PULSE WIDTH VS AMBIENT TEMPERATURE

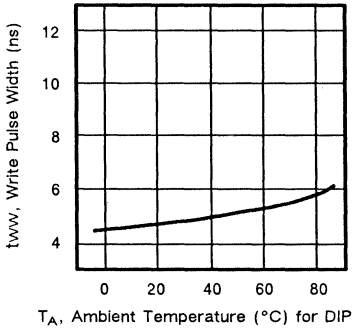
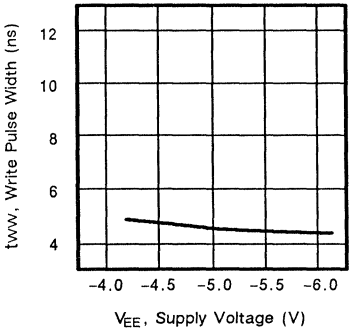
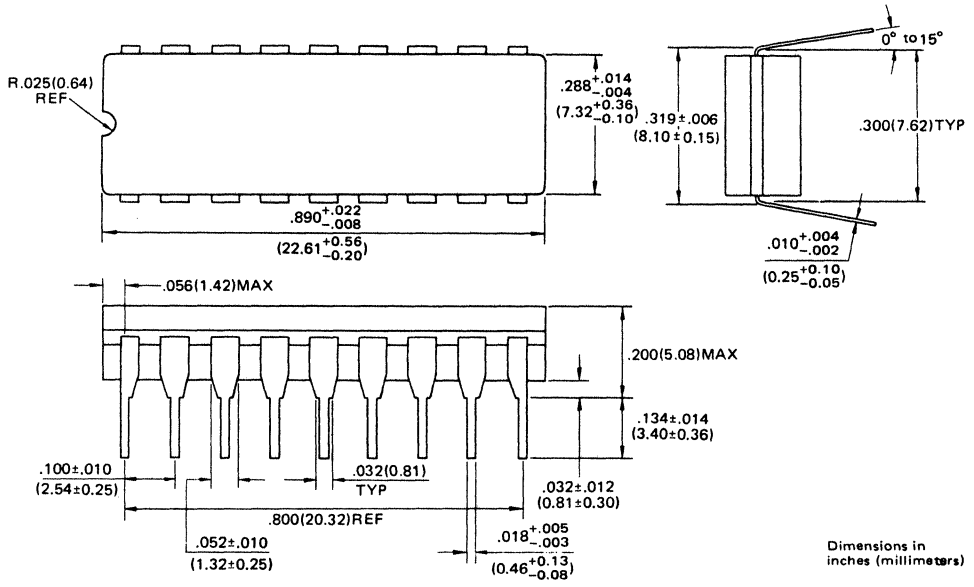


FIG. 11 – WRITE PULSE WIDTH VS SUPPLY VOLTAGE



PACKAGE DIMENSIONS

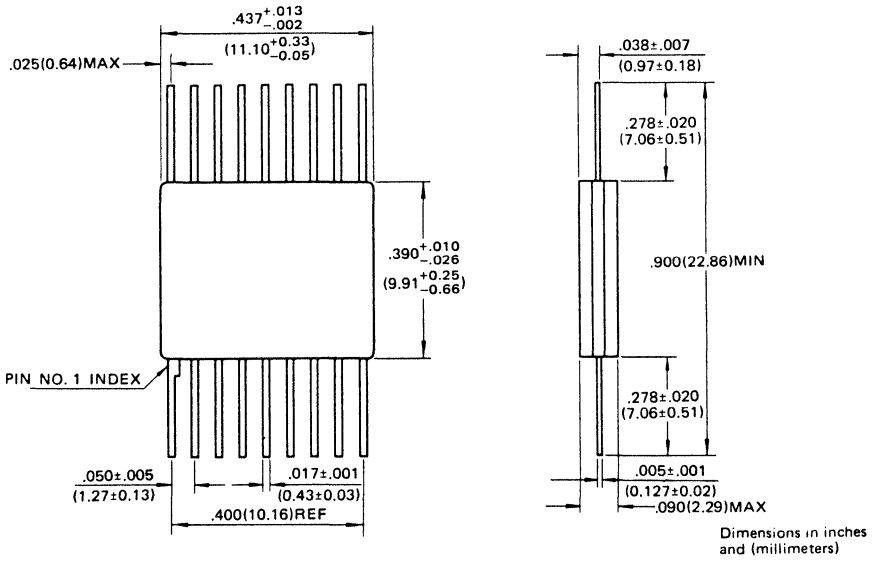
18-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18C-C01)



Dimensions in inches (millimeters)

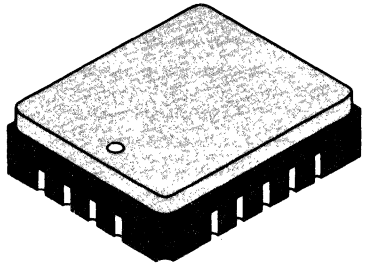
PACKAGE DIMENSIONS (continued)

18-LEAD CERAMIC (AXIAL) FLAT PACKAGE
(CASE No.: FPT-18C-C01)



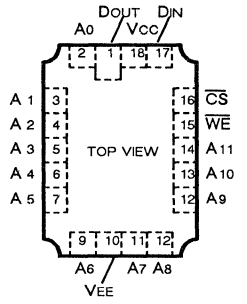
Dimensions in inches
and (millimeters)

PACKAGE DIMENSIONS (continued)

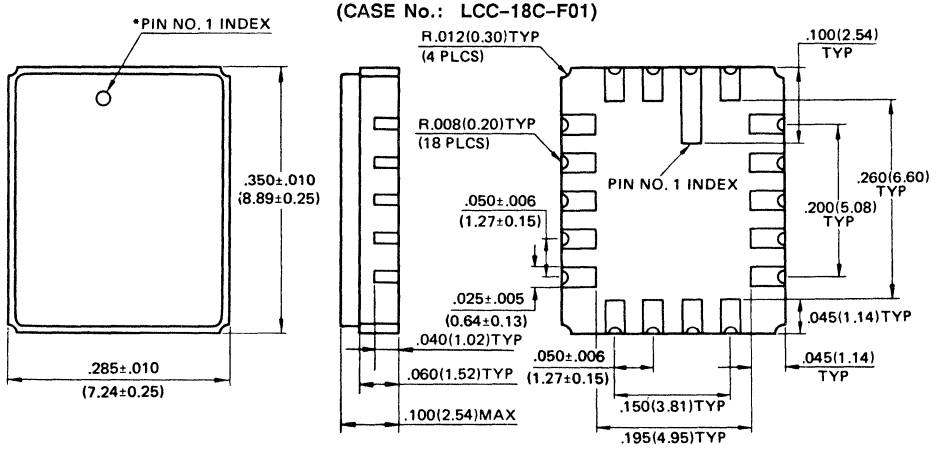


LCC-18C-F01

PAD CONFIGURATION



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches
and (millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100470A-7

August 1988
Edition 1.0

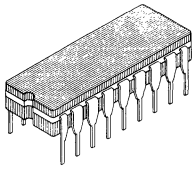
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100470A is a fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

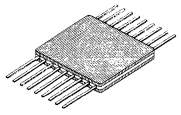
The MBM100470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100470A is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K-series ECL families
- Address access time :7 ns max.
- Chip select access time :3.5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation :0.19 mW/bit (typ.)
- DOPOS and IOP-II processing
- Pin compatible with the F100470



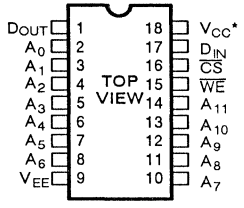
CERAMIC PACKAGE
DIP-18C-C01

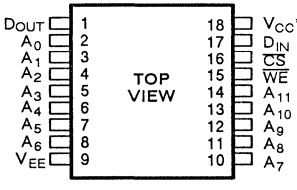


CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01: See Page 10

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 10

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

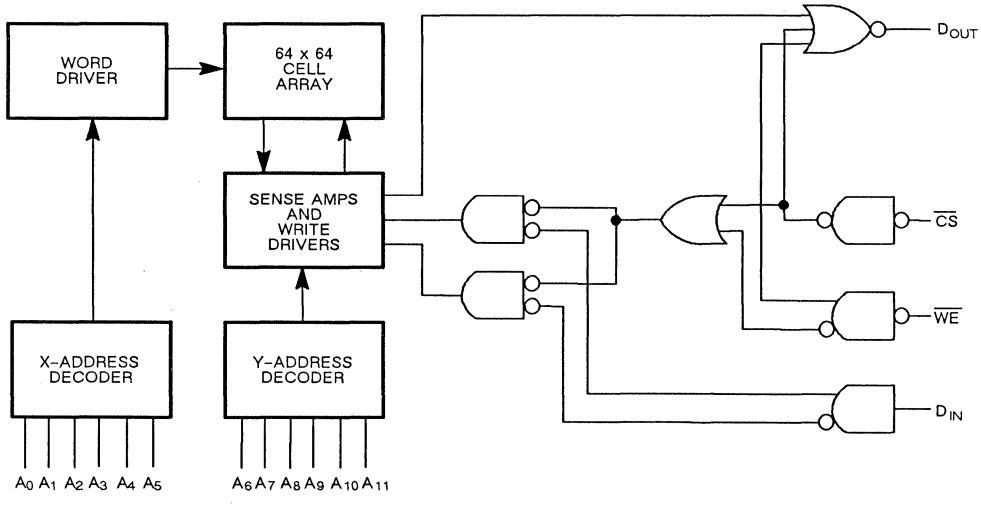
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

1

Fig. 1 — MBM100470A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Ope emitter outputs are provided to allow for maximum flexibility i output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-200			mA

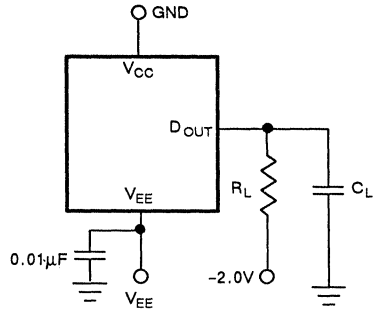
CAPACITANCE

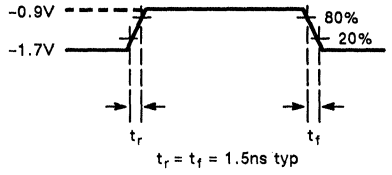
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS



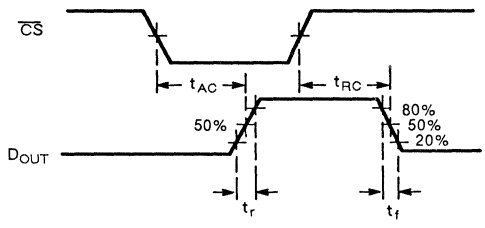


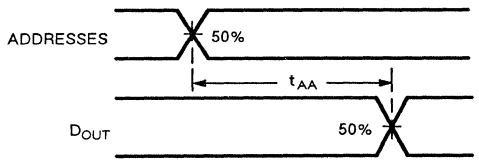
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

Note: All timing measurements referenced to 50% input levels.

READ CYCLE					
Parameter	Symbol	MBM100470A-7			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}			7	ns
Chip Select Access Time	t_{AC}			3.5	ns
Chip Select Recovery Time	t_{RC}			3.5	ns

READ CYCLE TIMING DIAGRAMS

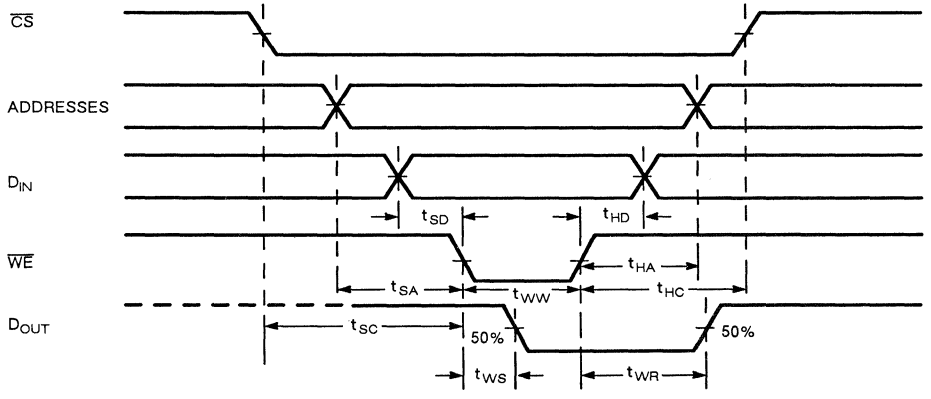




WRITE CYCLE

Parameter	Symbol	MBM100470A-7			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	7			ns
Write Disable Time	t_{WS}			3.5	ns
Write Recovery Time	t_{WR}			8	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	0			ns
Data Set Up Time	t_{SD}	0			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	0			ns
Data Hold Time	t_{HD}	0			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	MBM100470A-7			Unit
		Min	Typ	Max	
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

1

TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 3 - OUTPUT HIGH VOLTAGE VS AMBIENT TEMPERATURE

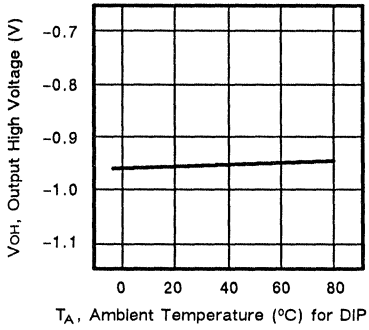


FIG. 4 - OUTPUT HIGH VOLTAGE VS SUPPLY VOLTAGE

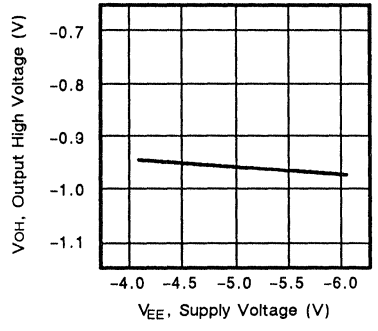


FIG. 5 - OUTPUT LOW VOLTAGE VS AMBIENT TEMPERATURE

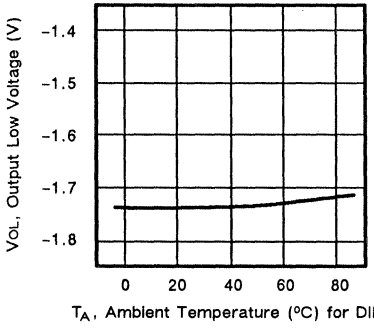


FIG. 6 - OUTPUT LOW VOLTAGE VS SUPPLY VOLTAGE

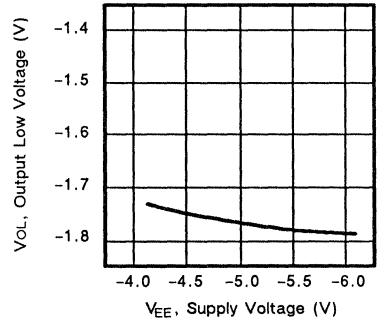
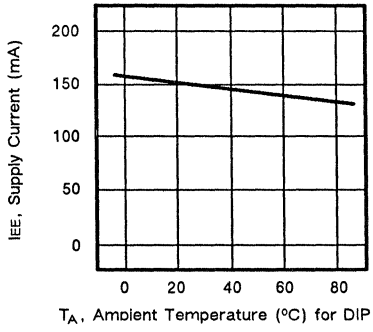


FIG. 7 - SUPPLY CURRENT VS AMBIENT TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 8 - ADDRESS ACCESS TIME VS AMBIENT TEMPERATURE

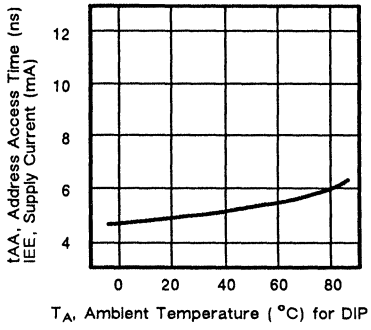


FIG. 9 - ADDRESS ACCESS TIME VS SUPPLY VOLTAGE

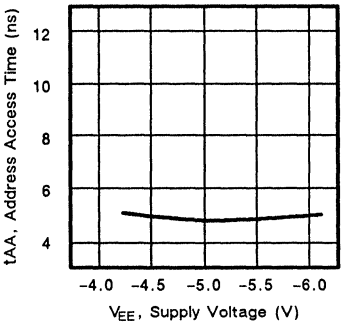


FIG. 10 - WRITE PULSE WIDTH VS AMBIENT TEMPERATURE

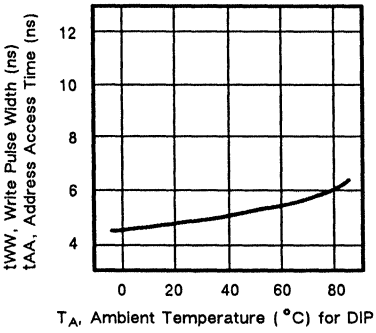
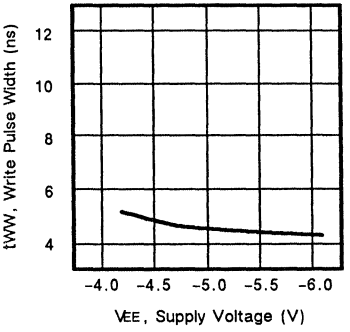


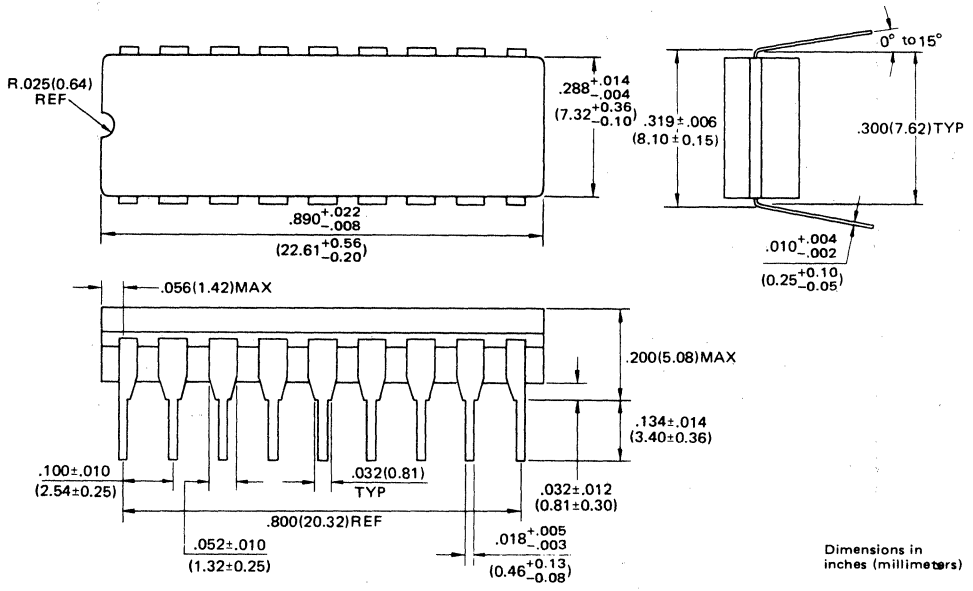
FIG. 11 - WRITE PULSE WIDTH VS SUPPLY VOLTAGE



1

PACKAGE DIMENSIONS

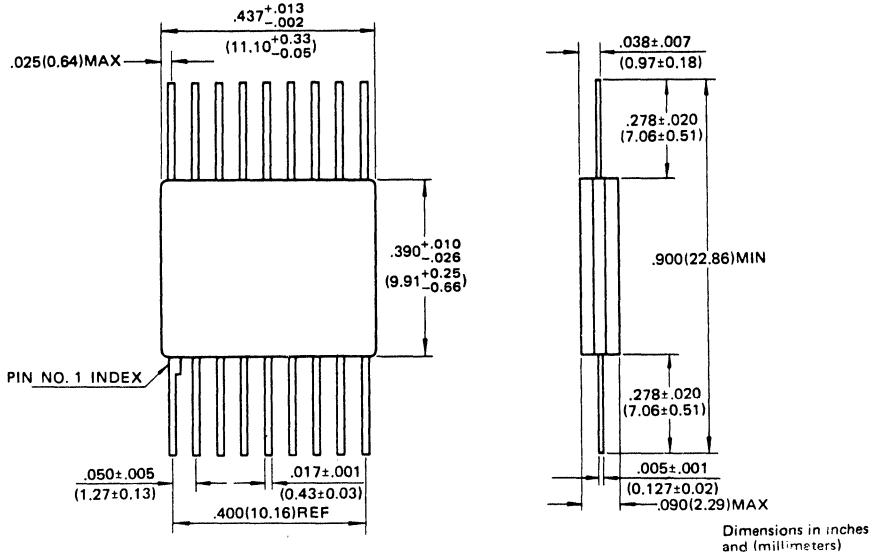
18-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18C-C01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (continued)

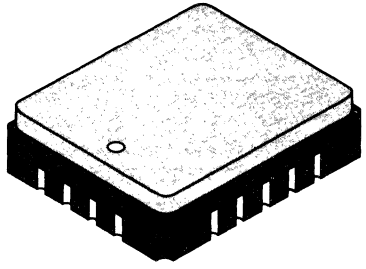
18-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-18C-C01)



Dimensions in inches and (millimeters)

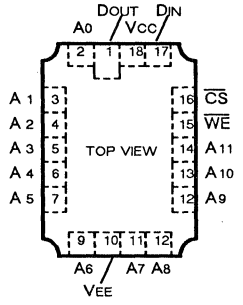
1

PACKAGE DIMENSIONS (continued)

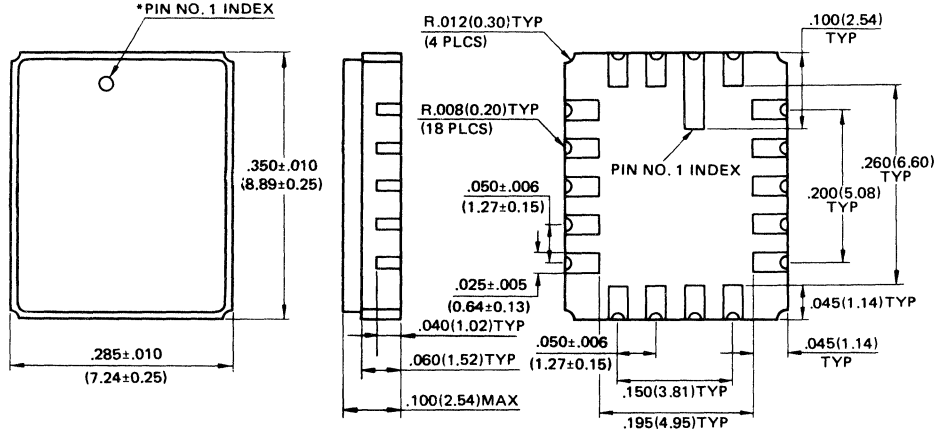


LCC-18C-F01

PAD CONFIGURATION



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches
and (millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10470A-10
MBM 10470A-15
MBM 10470A-20

July 1984
Edition 2.0

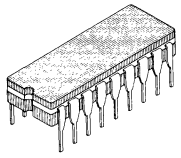
1

4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

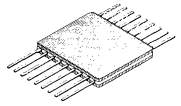
The Fujitsu MBM 10470A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage compensation for improved noise margin.

The MBM 10470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10470A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.



CERAMIC PACKAGE
DIP-18C-C01

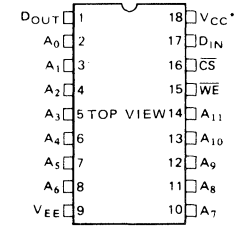


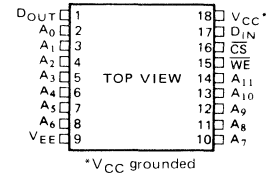
CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01 : See Page 10

- 4096 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 10 nsec. max. (MBM 10470A-10)
  15 nsec. max. (MBM 10470A-15)
  20 nsec. max. (MBM 10470A-20)
- Chip select access time: 6 nsec. max. (MBM 10470A-10)
  8 nsec. max. (MBM 10470A-15)
  15 nsec max. (MBM 10470A-20)
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.22mW/bit
- DOPOS and IOP-II processing
- Pin compatible with the F10470

PIN ASSIGNMENT





*VCC grounded

LCC PAD CONFIGURATION : See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

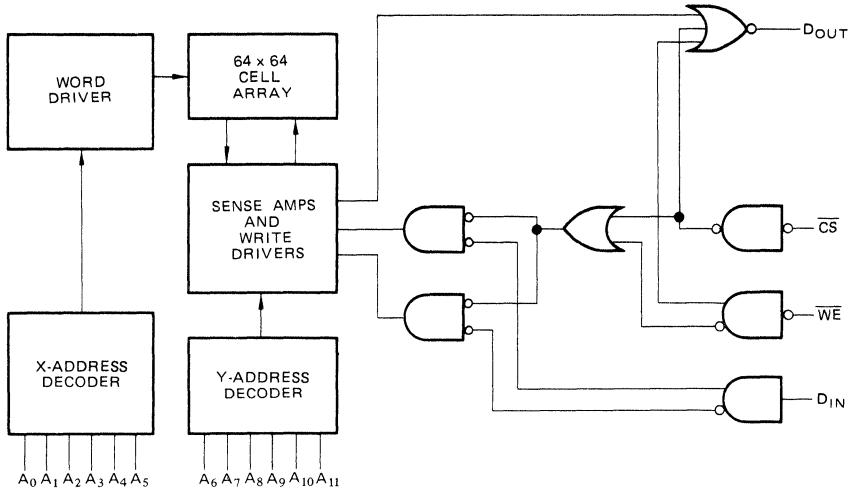
Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10470A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 75°C for DIP, Airflow≧2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max}$)	I_{IH}			−220	μA	0°C to 75°C
Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	−200			mA	0°C to 75°C

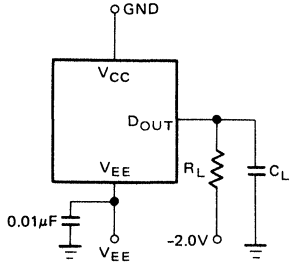
CAPACITANCE

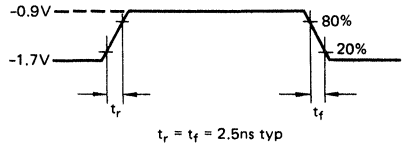
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V ± 5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

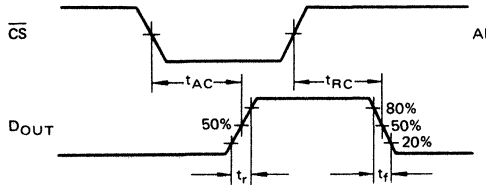
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

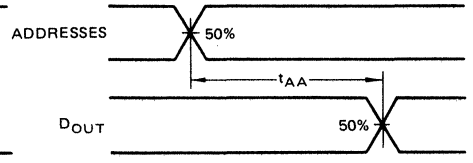
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10470A-10			MBM 10470A-15			MBM 10470A-20			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			10			15			20	ns
Chip Select Access Time	t_{AC}			6			8			15	ns
Chip Select Recovery Time	t_{RC}			6			8			15	ns

READ CYCLE TIMING DIAGRAMS

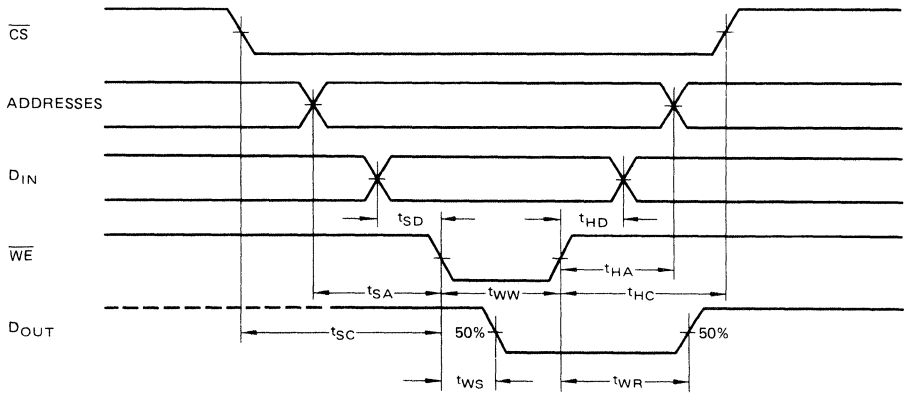




WRITE CYCLE

Parameter	Symbol	MBM 10470A-10			MBM 10470A-15			MBM 10470A-20			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			15			ns
Write Disable Time	t_{WS}			6			8			15	ns
Write Recovery Time	t_{WR}			10			10			15	ns
Address Set Up Time	t_{SA}	1			1			3			ns
Chip Select Set Up Time	t_{SC}	1			1			2			ns
Data Set Up Time	t_{SD}	1			1			2			ns
Address Hold Time	t_{HA}	2			2			2			ns
Chip Select Hold Time	t_{HC}	2			2			2			ns
Data Hold Time	t_{HD}	2			2			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	MBM 10470A-10			MBM 10470A-15			MBM 10470A-20			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Rise Time	t_r		1.5			1.5			1.5		ns
Output Fall Time	t_f		1.5			1.5			1.5		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

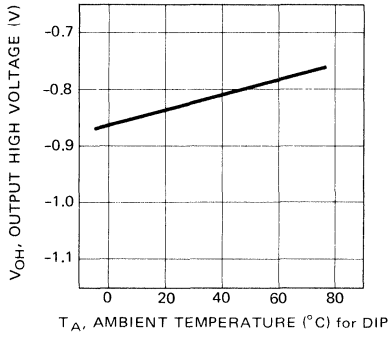


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

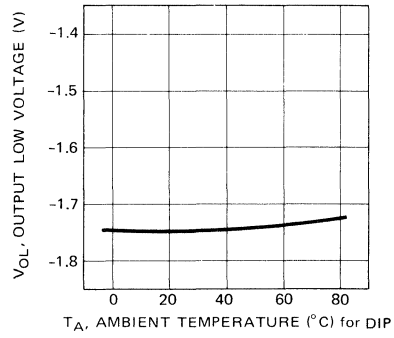


Fig. 5 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

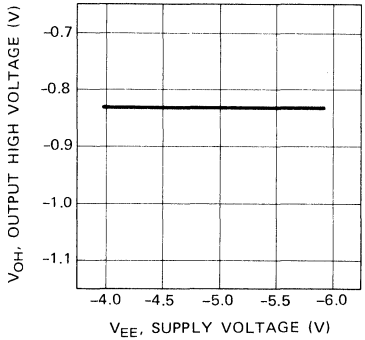


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

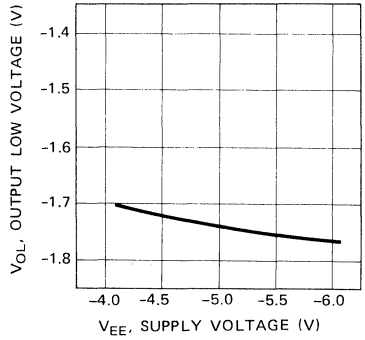


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

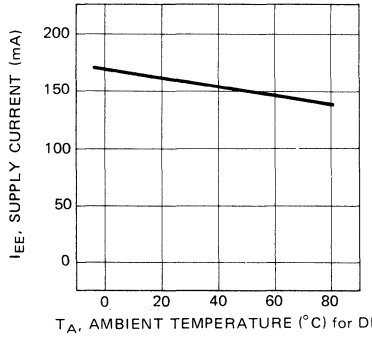


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

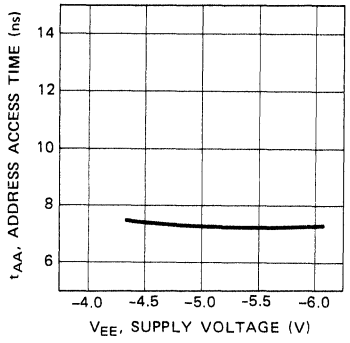


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

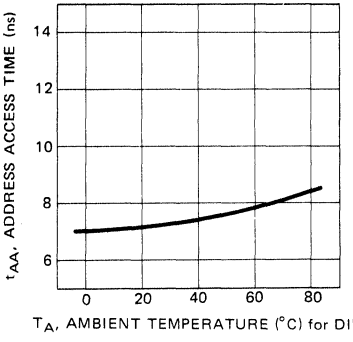


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

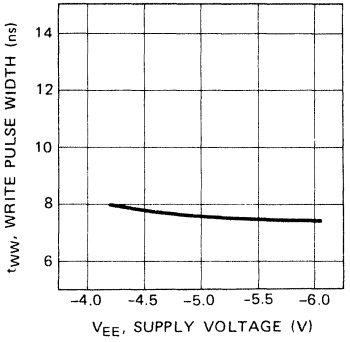
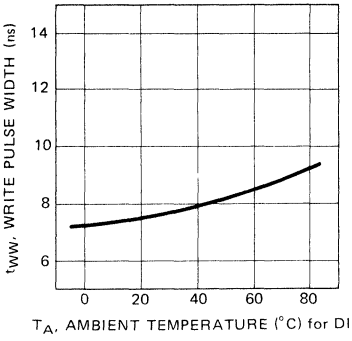


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



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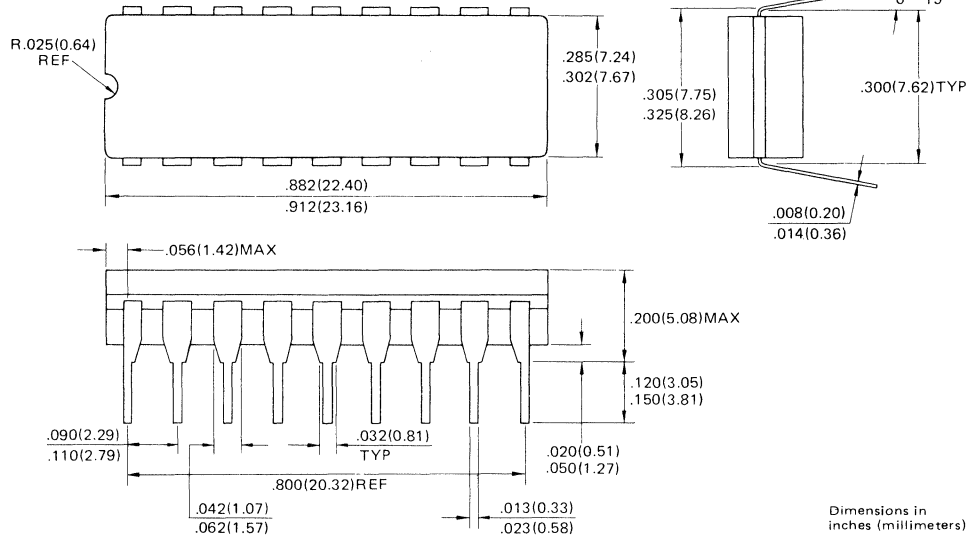
PACKAGE DIMENSIONS

18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

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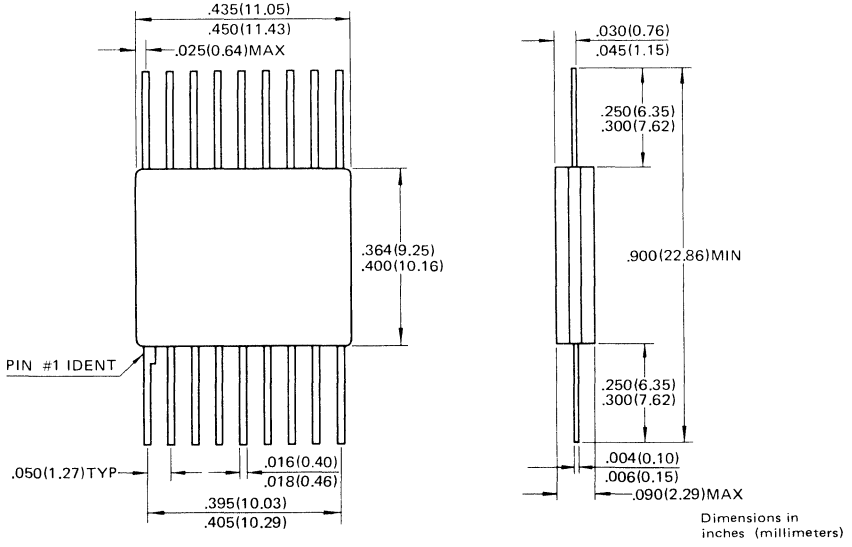

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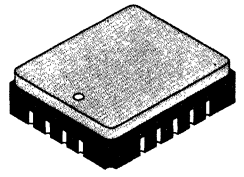
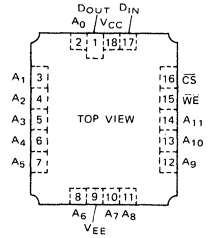
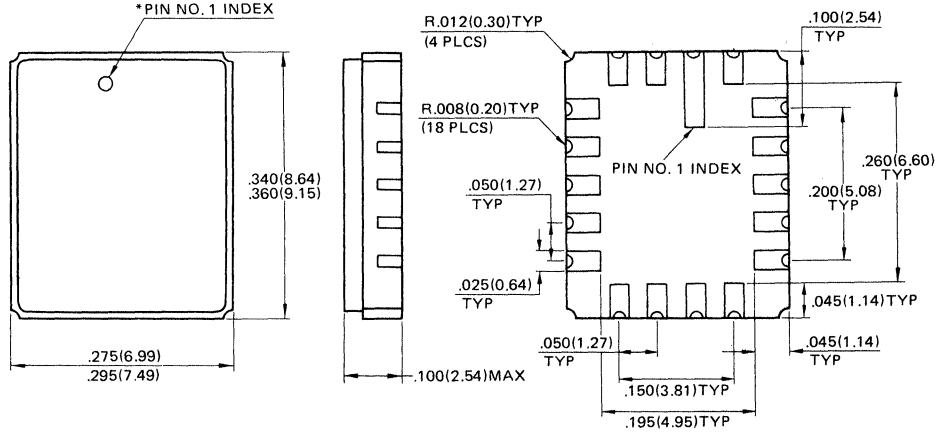


LCC-18C-F01

PAD ASSIGNMENT



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100470A-10
MBM 100470A-15

July 1984
Edition 2.0

1

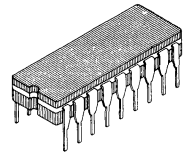
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100470A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

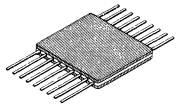
The MBM 100470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100470A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin.
- Fully compatible with industry-standard 100K-series ECL families
- Address access time: 10 nsec.max. (MBM 100470A-10)
  15 nsec.max. (MBM 100470A-15)
- Chip select access time: 6 nsec.max. (MBM 100470A-10)
  8 nsec.max. (MBM 100470A-15)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.19mW/bit
- DOPOS and IOP-II processing
- Pin compatible with the F100470



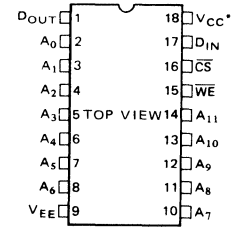
CERAMIC PACKAGE
DIP-18C-C01

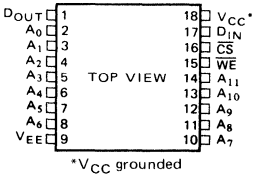


CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01 : See Page 10

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION : See Page10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

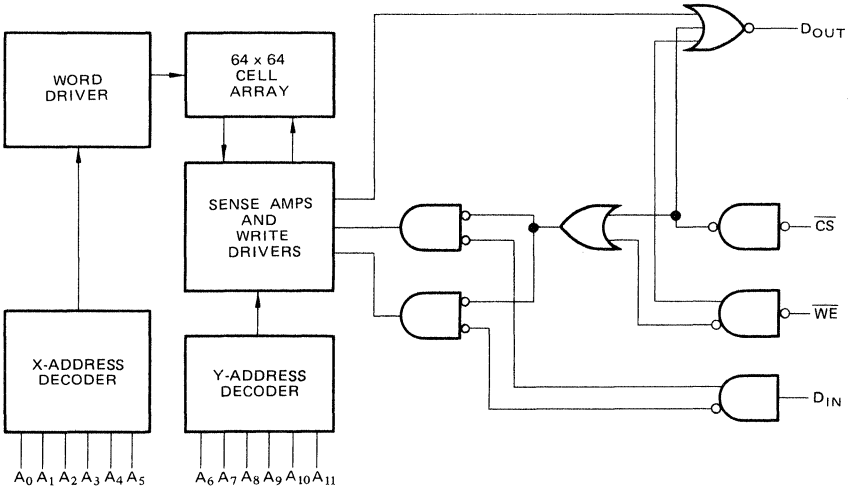
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100470A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is proveded for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 85°C for DIP, airflow≧2.5m/s, T_C=0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-200			mA

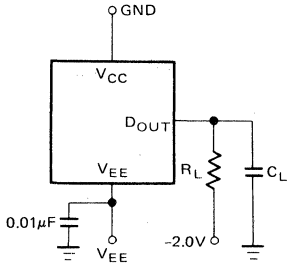
CAPACITANCE

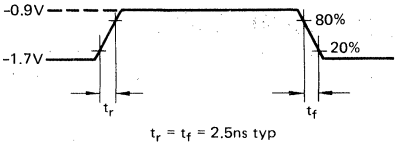
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V ± 5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧2.5m/s
T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

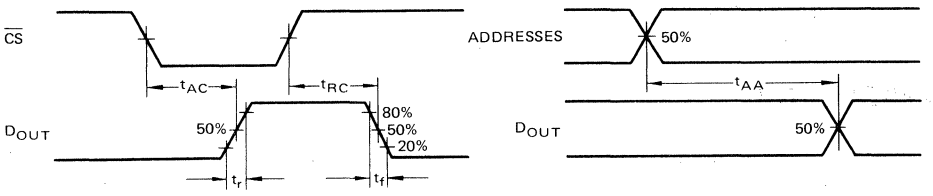
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100470A-10			MBM 100470A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			10			15	ns
Chip Select Access Time	t_{AC}			6			8	ns
Chip Select Recovery Time	t_{RC}			6			8	ns

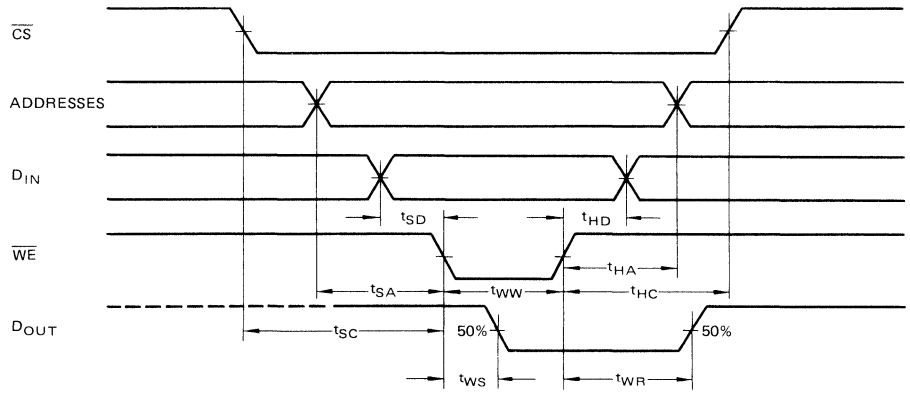
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 100470A-10			MBM 100470A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			ns
Write Disable Time	t_{WS}			6			8	ns
Write Recovery Time	t_{WR}			12			12	ns
Address Set Up Time	t_{SA}	1			1			ns
Chip Select Set Up Time	t_{SC}	1			1			ns
Data Set Up Time	t_{SD}	1			1			ns
Address Hold Time	t_{HA}	2			2			ns
Chip Select Hold Time	t_{HC}	2			2			ns
Data Hold Time	t_{HD}	2			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

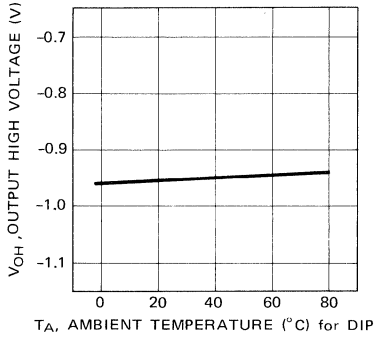


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

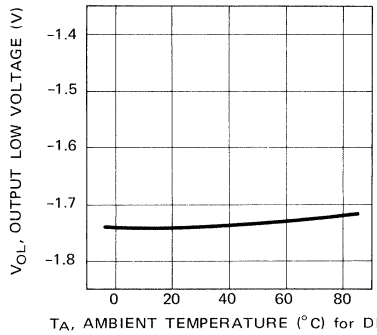


Fig. 5 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

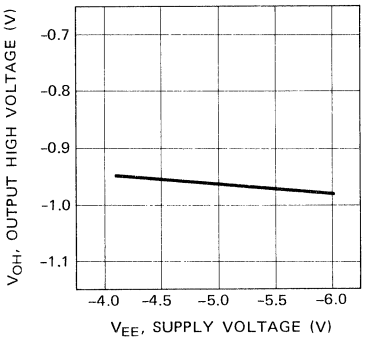


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

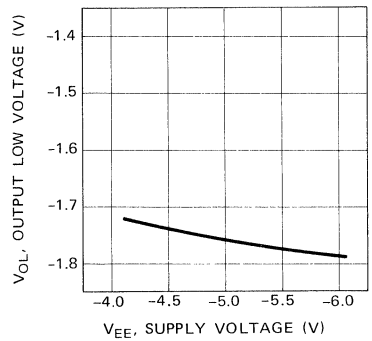


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

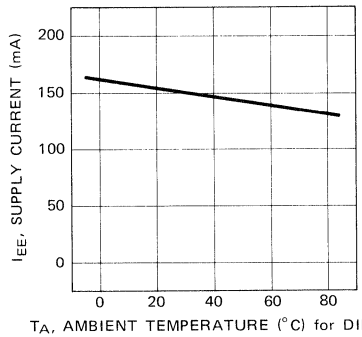


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

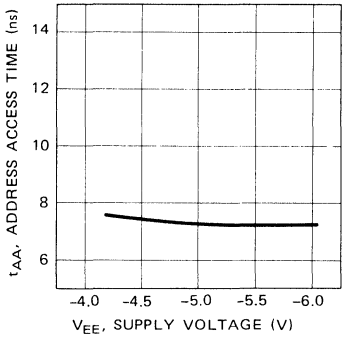


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

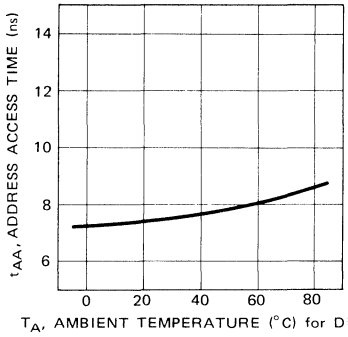


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

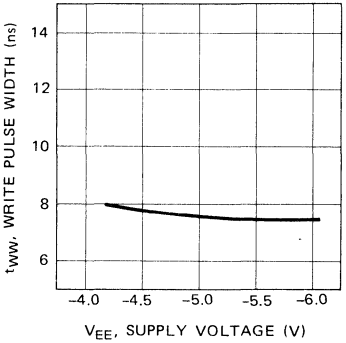
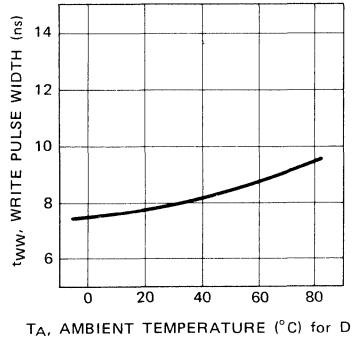


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



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PACKAGE DIMENSIONS

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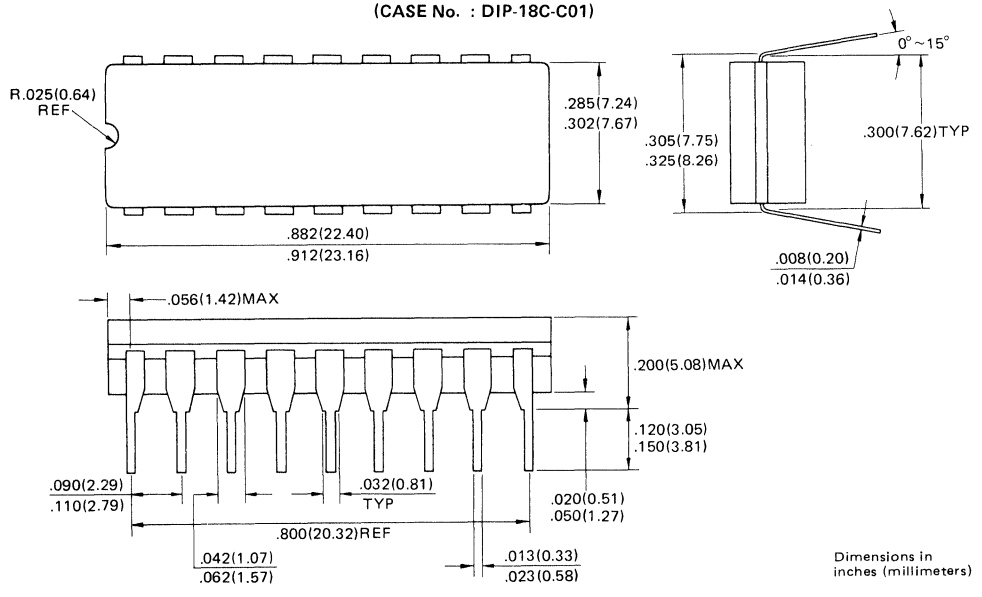

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

18-LEAD CERAMIC (CERDIP) FLAT PACKAGE
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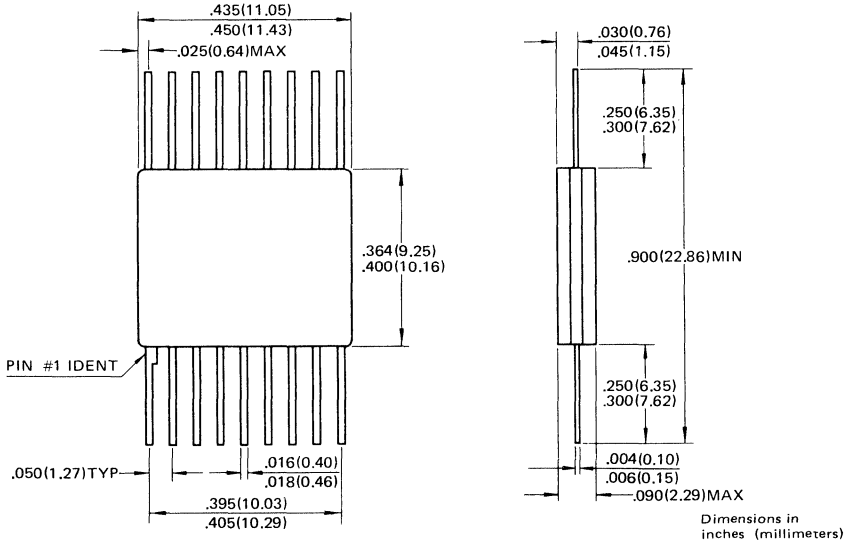

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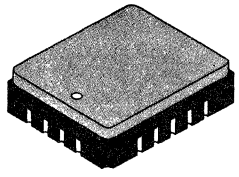
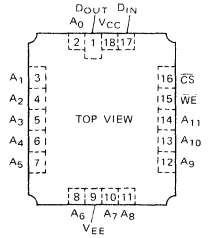
PACKAGE DIMENSIONS

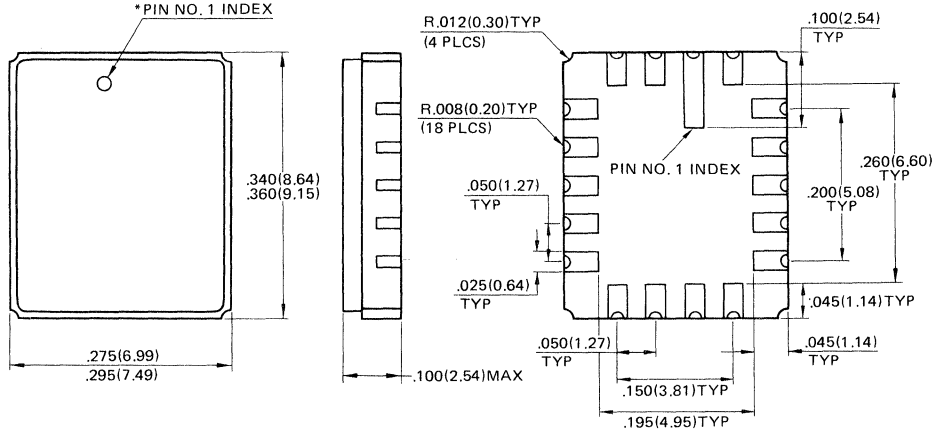


LCC-18C-F01

PAD ASSIGNMENT



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

October 1989
Edition 1.0

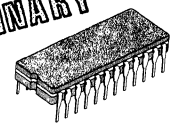
FUJITSU

DATA SHEET

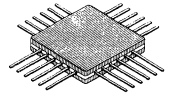
MBM10A474-3

4096–BIT BIPOLAR ECL RANDOM ACCESS MEMORY

PRELIMINARY



CERAMIC PACKAGE
DIP–24C–C05



CERAMIC PACKAGE
FPT–24C–C02

LCC–24C–F02 : See Page 8

DESCRIPTION

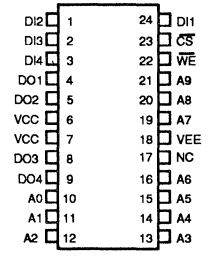
The Fujitsu MBM10A474 is fully decoded 4096–bit ECL read/write random access memory designed for high–speed scratch pad, control and buffer storage applications. The device is organized as 1024 words by 4 bits, and it features on–chip voltage compensation for improved noise margin.

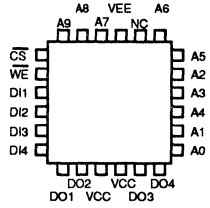
The MBM10A474 offers extremely small cell size, realized through theuse of Fujitsu's patented DOPOS (Doped Polysilicon), as well as ESPER (Emitter–base Self aligned structure with Polysilicon Electrodes and Resistors.) processing.

Operation for the MBM10A474 is specified over a case temperature range of from 0°C to 55°C (Tc). It also features 24–pin DIP, Flat Package or LCC. It is fully compatible with Industry standard 10K–ECK families.

- 1024 words by 4 bits organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Address access time : 3ns
- Chip select access time : 2ns
- Power dissipation : 1560mW max
- Open emitter output for ease of memory expansion
- DOPOS and ESPER processing

PIN ASSIGNMENT





Vcc grounded

LCC Pad Configuration : See Page 8

ABSOLUTE MAXIMUM RATINGS (See NOTE)

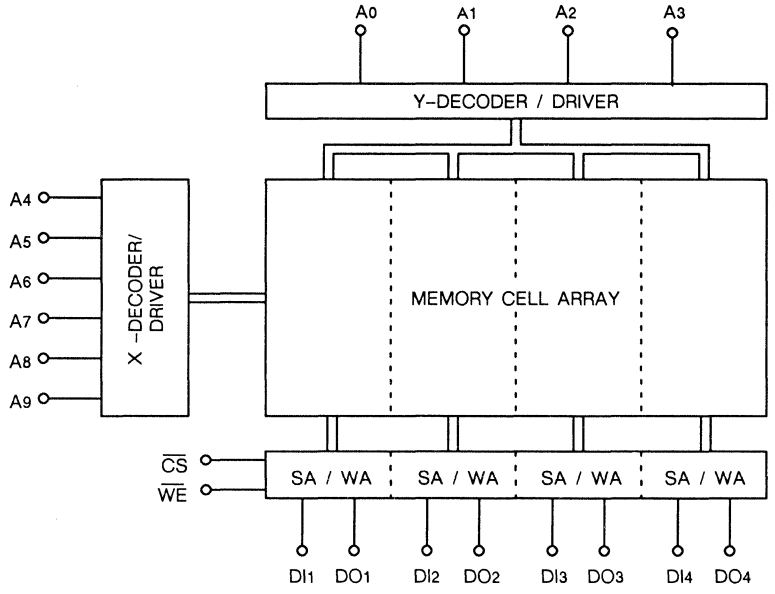
Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –6.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

1

Fig.1 – MBM10A474 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10A474 is fully decoded read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 though A9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(Vcc = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, Tc = 0°C to 55°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TC
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 55°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 55°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 55°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 55°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°C to 55°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°C to 55°C
$\overline{CS}$ Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°C to 55°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-330			mA	0°C to 55°C

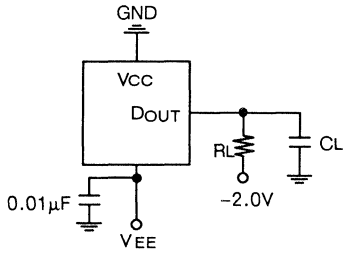
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4.0		pF
Output Pin Capacitance	C_{OUT}		5.0		pF

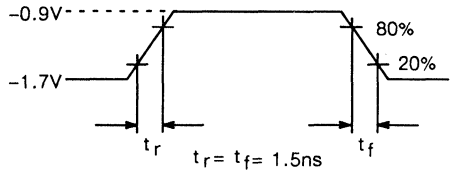
AC CHARACTERISTICS

(VCC = 0V, VEE = −5.2V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, TC = 0°C to 55°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

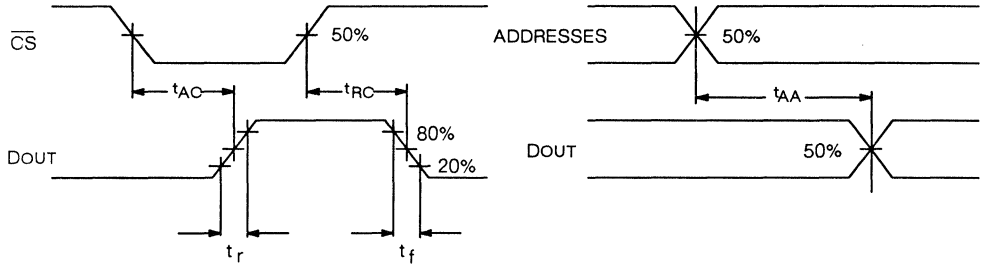


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			3.0	ns
Chip Select Access Time	t_{AC}			2.0	ns
Chip Select Recovery Time	t_{RC}			2.0	ns

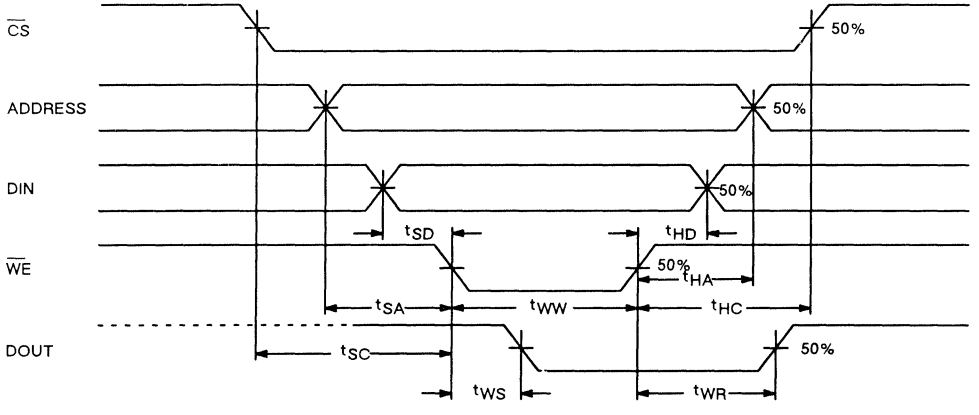
Fig. 3 – READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	5.0			ns
Write Disable Time	t_{WS}			2.0	ns
Write Recovery Time	t_{WR}			4.0	ns
Address Set Up Time	t_{SA}	0.5			ns
Chip Select Set Up Time	t_{SC}	0.0			ns
Data Set Up Time	t_{SD}	0.0			ns
Address Hold Time	t_{HA}	0.5			ns
Chip Select Hold Time	t_{HC}	0.5			ns
Data Hold Time	t_{HD}	0.5			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM

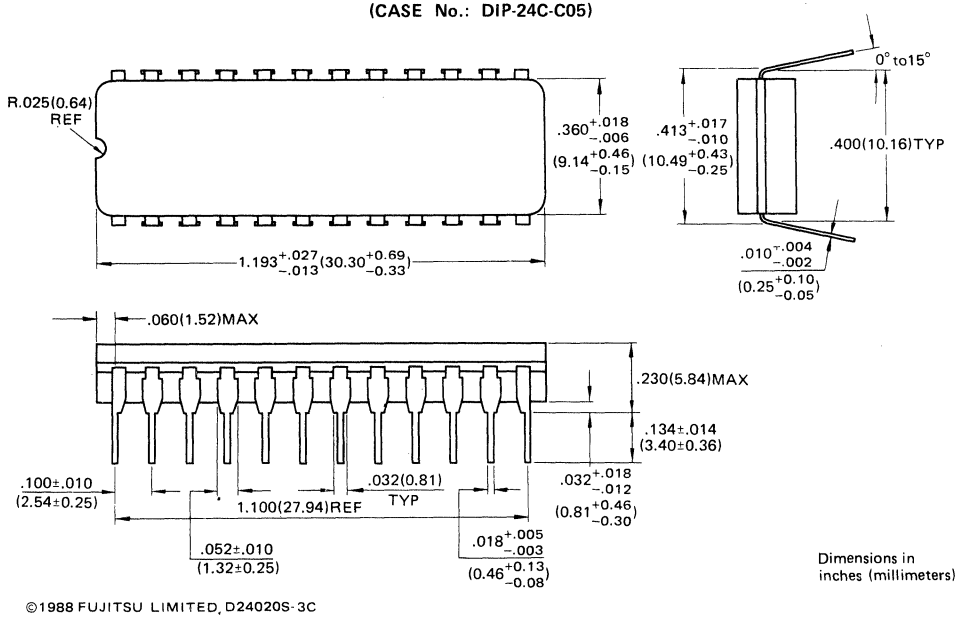


READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

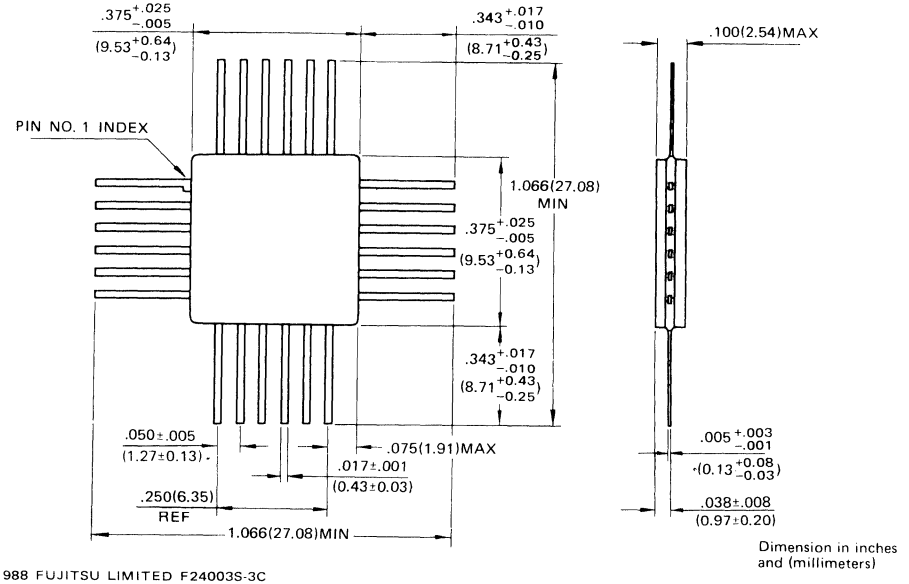
PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)

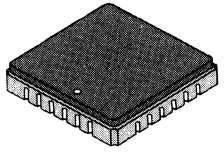


Dimensions in
inches (millimeters)

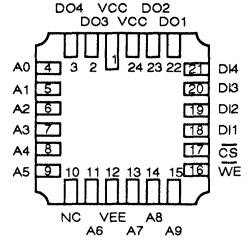
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



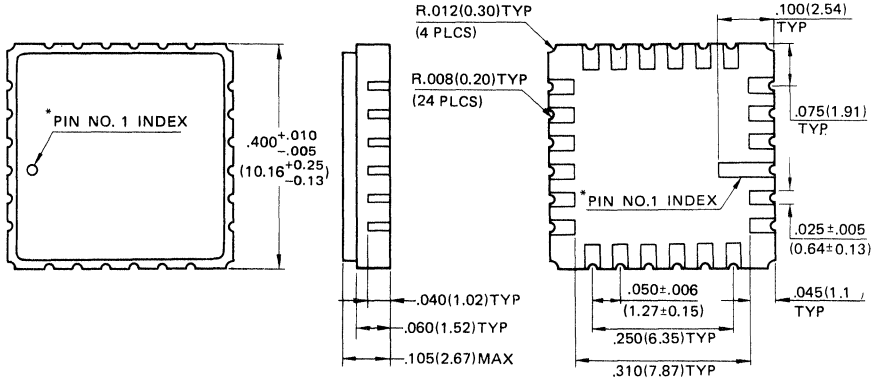
Dimension in inches
and (millimeters)



PIN ASSIGNMENT



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

October 1989
Edition 1.0

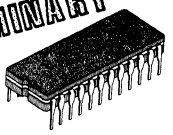
FUJITSU

DATA SHEET

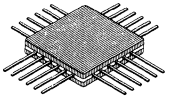
MBM101474A-3

4096–BIT BIPOLAR ECL RANDOM ACCESS MEMORY

PRELIMINARY



CERAMIC PACKAGE
DIP–24C–C05



CERAMIC PACKAGE
FPT–24C–C02

LCC–24C–F02 : See Page 8

DESCRIPTION

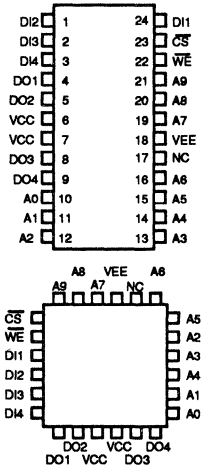
The Fujitsu MBM101474A is fully decoded 4096–bit ECL read/write random access memory designed for high–speed scratch pad, control and buffer storage applications. The device is organized as 1024 words by 4 bits, and it features on–chip voltage/temperature compensation for improved noise margin.

The MBM101474A offers extremely small cell size, realized through theuse of Fujitsu's patented DOPOS (Doped Polysilicon), as well as ESPER (Emitter–base Self aligned structure with Polysilicon Electrodes and Resistors.) processing.

Operation for the MBM101474A is specified over a case temperature range of from 0°C to 55°C (Tc). It also features 24–pin DIP, FlatPackage or LCC. It is fully compatible with Industry standard 100K–ECK families.

- 1024 words by 4 bits organization
- On–chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Address access time : 3ns
- Chip select access time : 2ns
- Power dissipation : 1560mW max
- Open emitter output for ease of memory expansion
- DOPOS and ESPER processing

PIN ASSIGNMENT



V cc grounded

LCC Pad Configuration : See Page 8

ABSOLUTE MAXIMUM RATINGS (See NOTE)

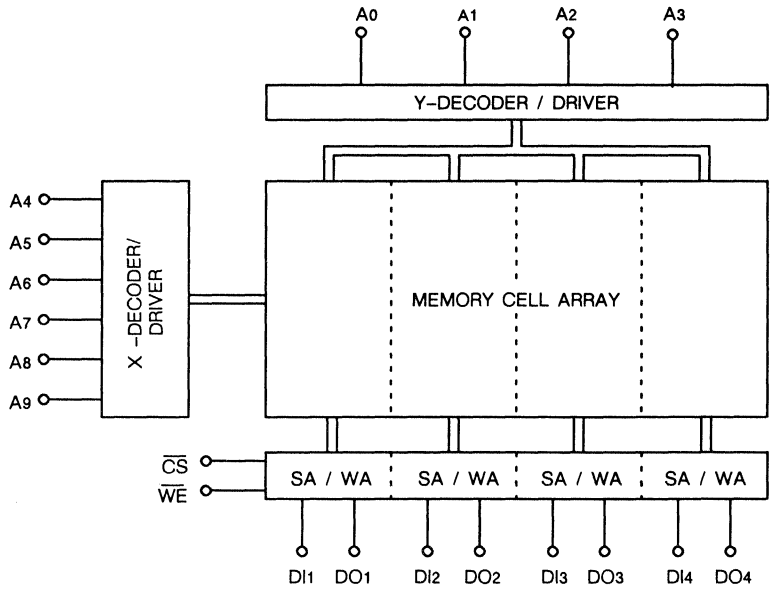
Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –6.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

1

Fig.1 – MBM101474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM101474A is fully decoded read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 though A9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 55°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-330			mA

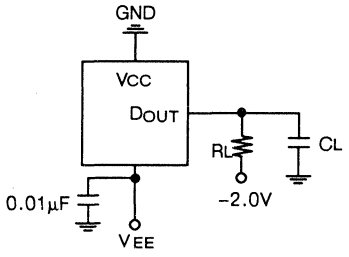
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4.0		pF
Output Pin Capacitance	C_{OUT}		5.0		pF

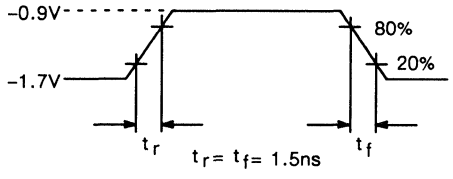
AC CHARACTERISTICS

(VCC = 0V, VEE = −5.2V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, TC = 0°C to 55°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

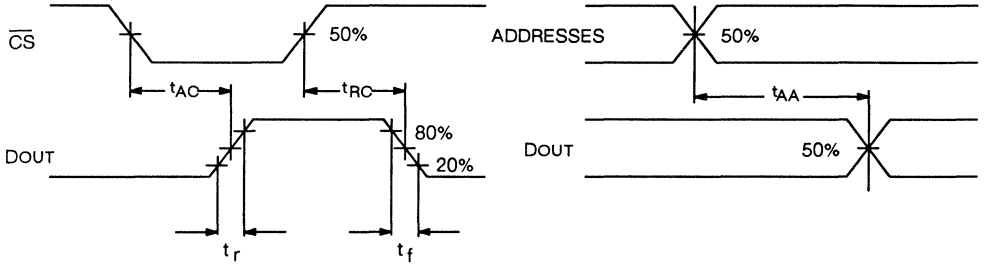


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			3.0	ns
Chip Select Access Time	t_{AC}			2.0	ns
Chip Select Recovery Time	t_{RC}			2.0	ns

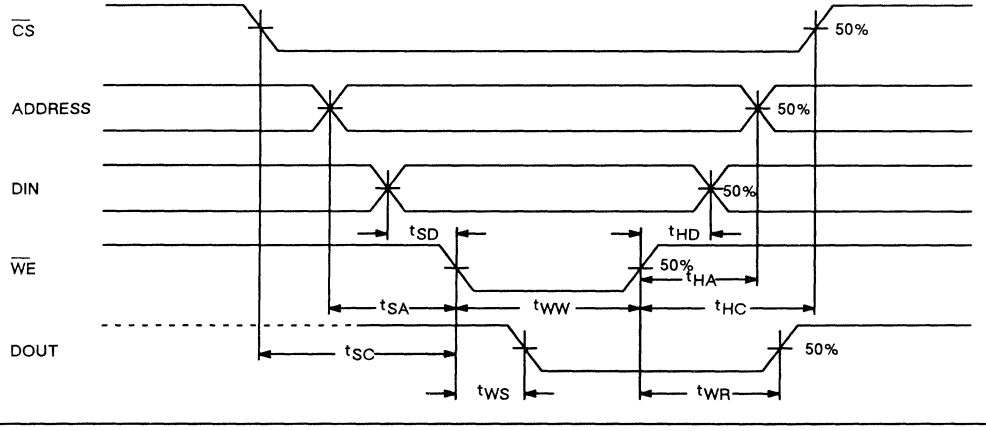
Fig. 3 – READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	5.0			ns
Write Disable Time	t_{WS}			2.0	ns
Write Recovery Time	t_{WR}			4.0	ns
Address Set Up Time	t_{SA}	0.5			ns
Chip Select Set Up Time	t_{SC}	0.0			ns
Data Set Up Time	t_{SD}	0.0			ns
Address Hold Time	t_{HA}	0.5			ns
Chip Select Hold Time	t_{HC}	0.5			ns
Data Hold Time	t_{HD}	0.5			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM

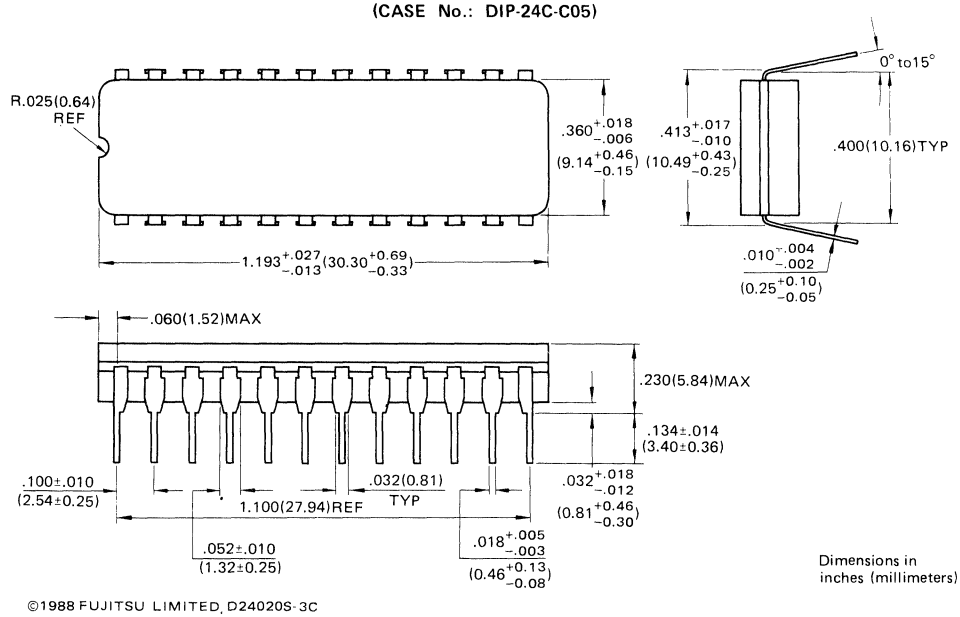


READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

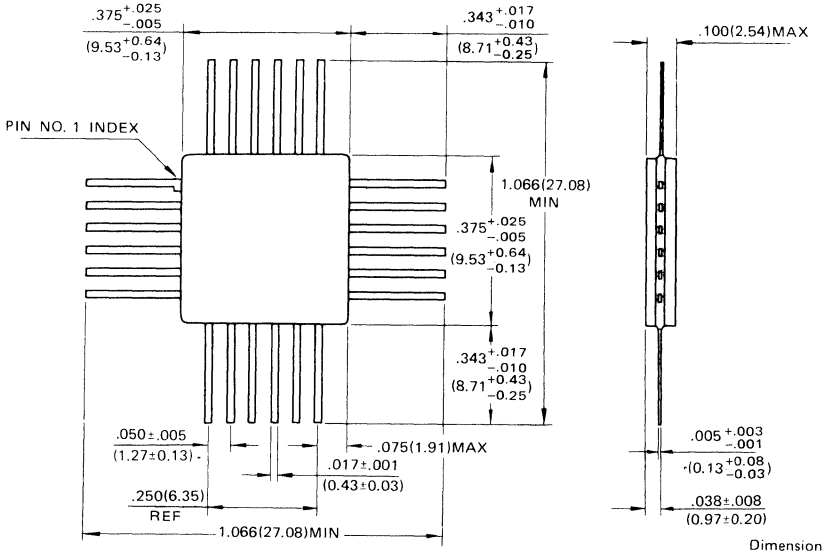
PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



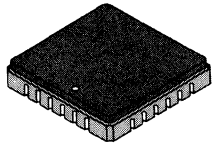
Dimensions in
inches (millimeters)

24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)

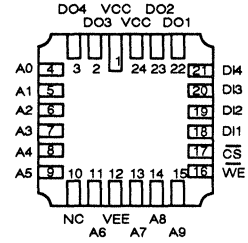


Dimension in inches and (millimeters)

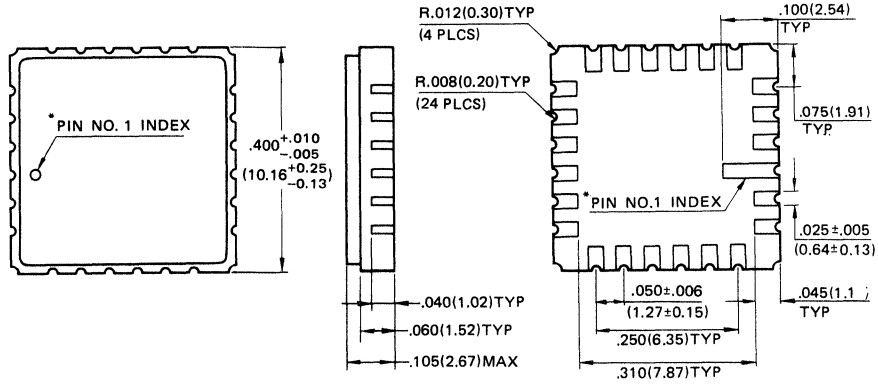
LCC-24C-F02



PIN ASSIGNMENT



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10474A-5
MBM 10474A-7

June 1987
Edition 1.0

1

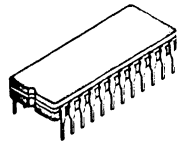
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

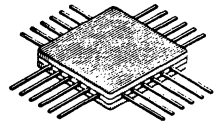
The MBM 10474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as U-Fox (U-groove isolation with thick field oxide) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10474A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 5 ns max. (MBM 10474A-5)
  7 ns max. (MBM 10474A-7)
- Chip select access time: 3 ns max. (MBM 10474A-5)
  5 ns max. (MBM 10474A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.33 mW/bit typ. (MBM 10474A-5)
  0.24 mW/bit typ. (MBM 10474A-7)
- DOPOS and U-Fox processing
- Pin compatible with the F10474



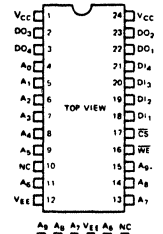
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT



V_{CC} grounded

LCC PAD CONFIGURATION : See page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

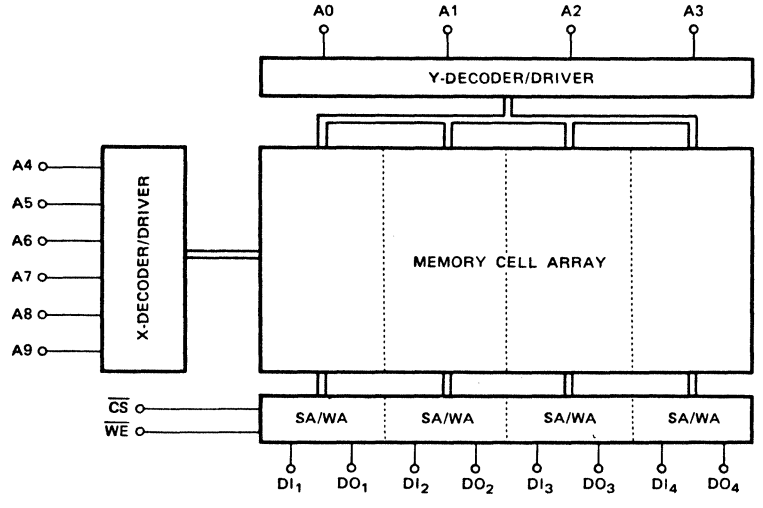
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0° C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-5	I_{EE}	-300			mA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-7	I_{EE}	-220			mA	0°C to 75°C

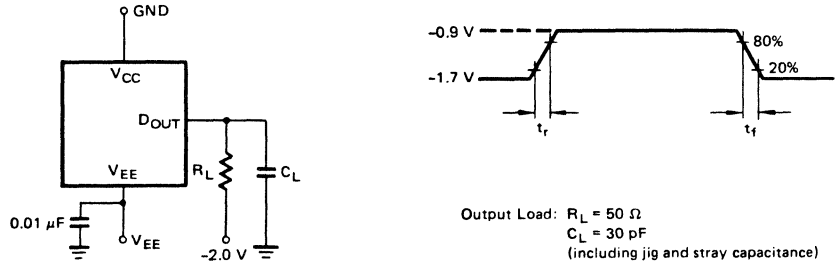
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capcitance	C_{OUT}		5	6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −5.2 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



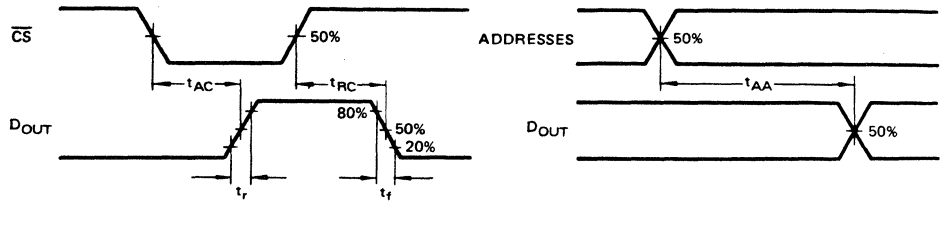
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10474A-5			MBM 10474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	1.2		5	1.2		7	ns
Chip Select Access Time	t_{AC}	0.5		3	0.5		5	ns
Chip Select Recovery Time	t_{RC}	0.5		3	0.5		5	ns

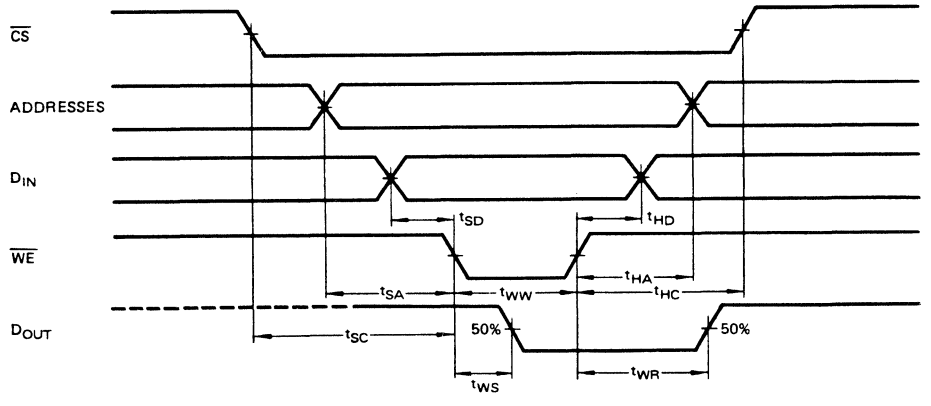
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10474A-5			MBM 10474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	8			5			ns
Write Disable Time	t_{WS}	0.3		3	0.3		6.5	ns
Write Recovery Time	t_{WR}	0.5		7	0.5		8	ns
Address Set Up Time	t_{SA}	1			1			ns
Chip Select Set Up Time	t_{SC}	0			0			ns
Data Set Up Time	t_{SD}	0			0			ns
Address Hold Time	t_{HA}	1			1			ns
Chip Select Hold Time	t_{HC}	1			1			ns
Data Hold Time	t_{HD}	1			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

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CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

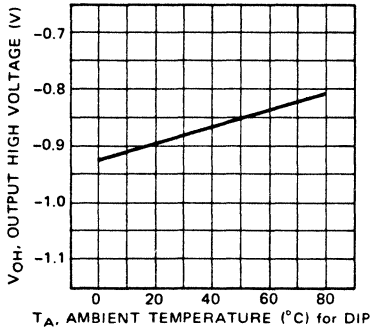


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

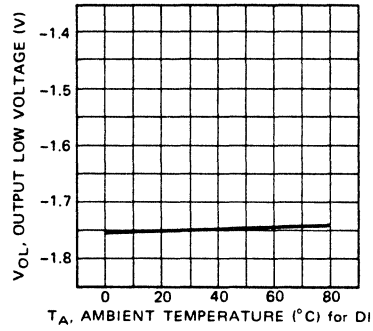


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

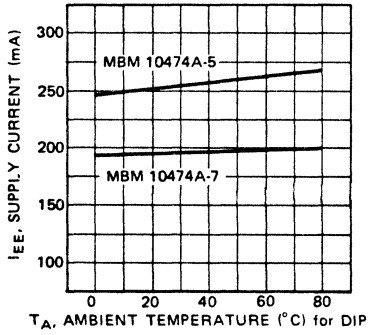


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

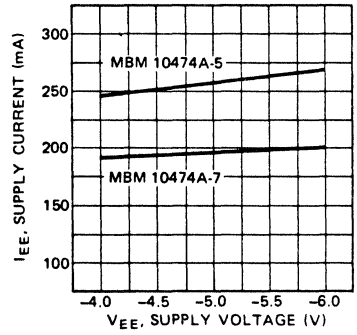


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

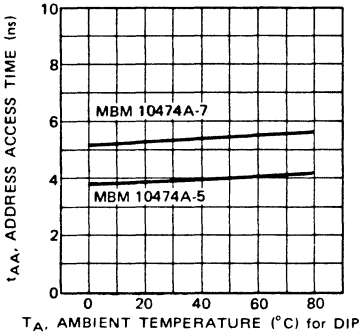


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

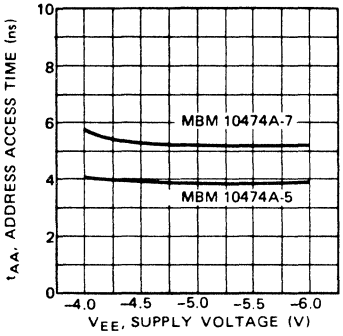


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

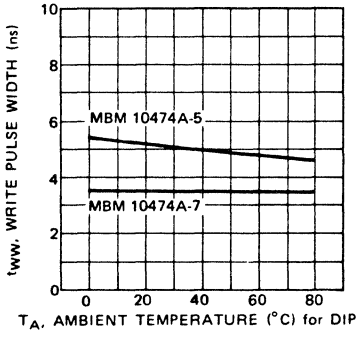
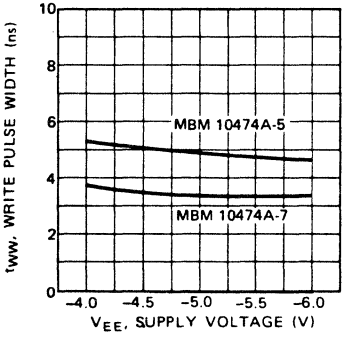


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



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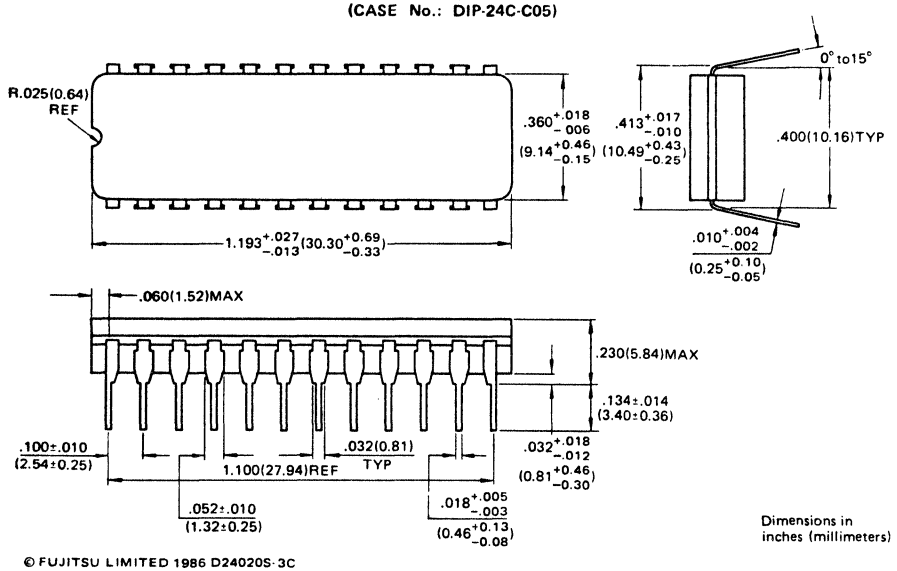
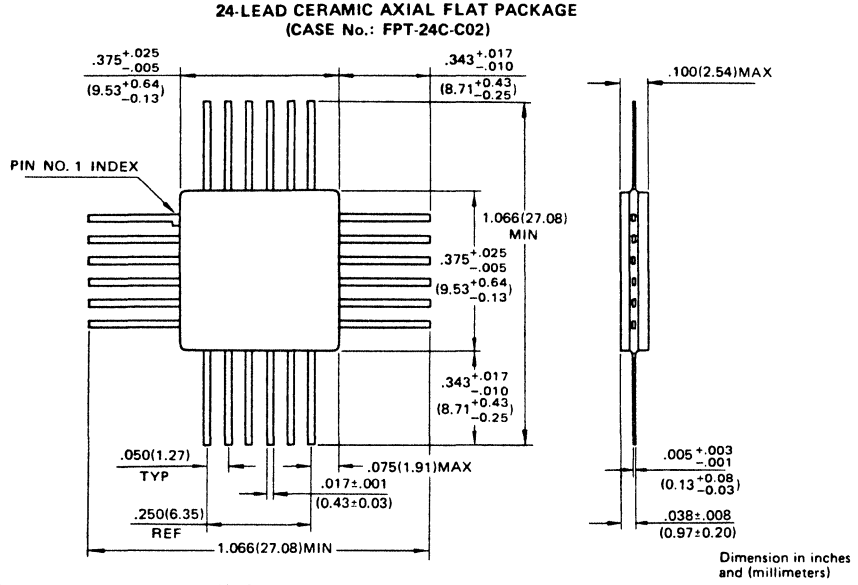
PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)

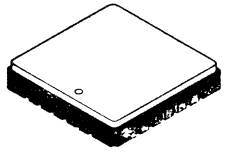


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

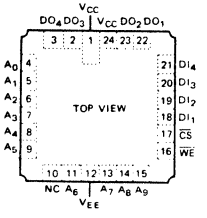


PACKAGE DIMENSIONS

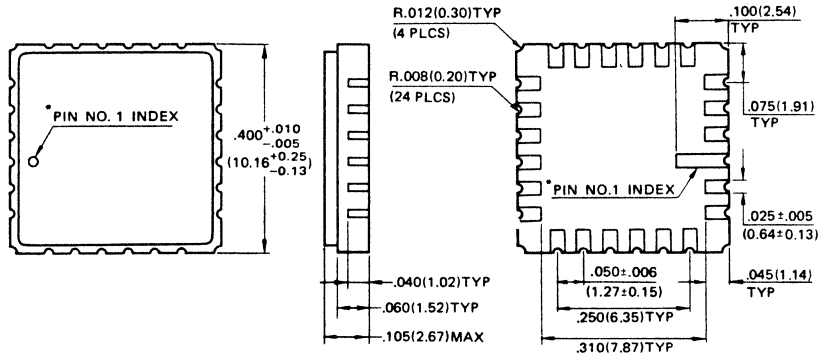


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100474A-5
MBM 100474A-7

June 1987
Edition 1.0

4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

The MBM 100474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as U-Fox (U-groove isolation with thick field oxide) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

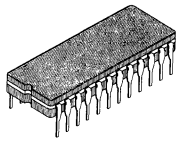
Operation for the MBM 100474A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat package, or LCC. It is fully compatible with industry-standard 100 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 5 ns max. (MBM 100474A-5)
  7 ns max. (MBM 100474A-7)
- Chip select access time: 3 ns max. (MBM 100474A-5)
  5 ns max. (MBM 100474A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.28 mW/bit typ. (MBM 100474A-5)
  0.20 mW/bit typ. (MBM 100474A-7)
- DOPOS and U-Fox processing
- Pin compatible with the F100474

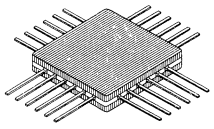
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.



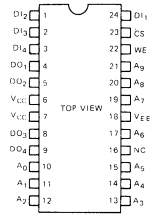
CERAMIC PACKAGE
DIP-24C-C05

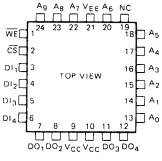


CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT





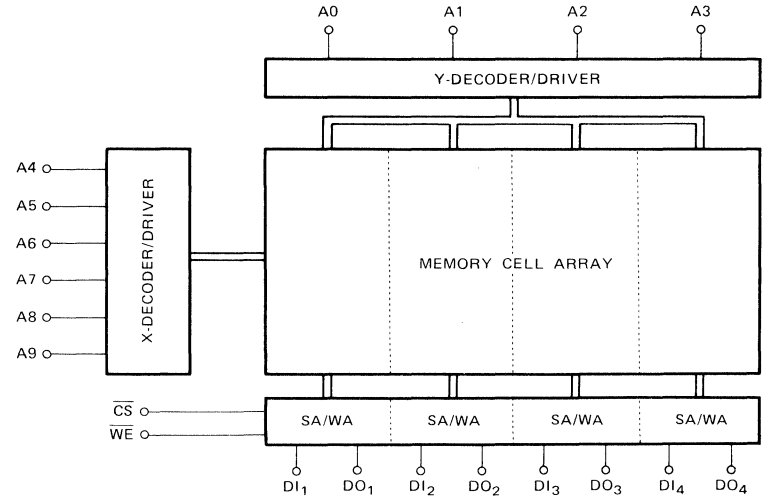
V_{CC} grounded

LCC PAD CONFIGURATION : See page 10

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC.
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50Ω to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	-1810		-1620	mV
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)		V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage for All Inputs)		V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All inputs and Outputs Open)	MBM 100474A-5	I_{EE}	-300			mA
	MBM 100474A-7		-220			

CAPACITANCE

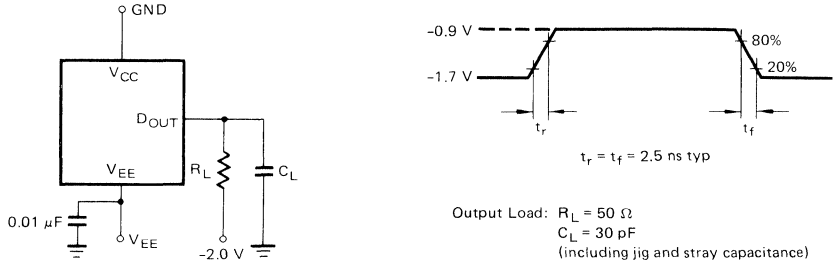
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capacitance	C_{OUT}		5	6	pF

1

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS

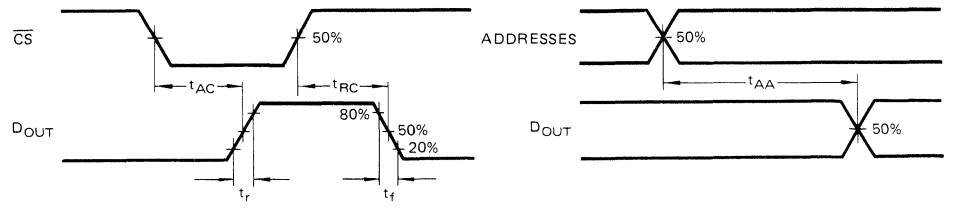


NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100474A-5			MBM 100474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	1.2		5	1.2		7	ns
Chip Select Access Time	t_{AC}	0.5		3	0.5		5	ns
Chip Select Recovery Time	t_{RC}	0.5		3	0.5		5	ns

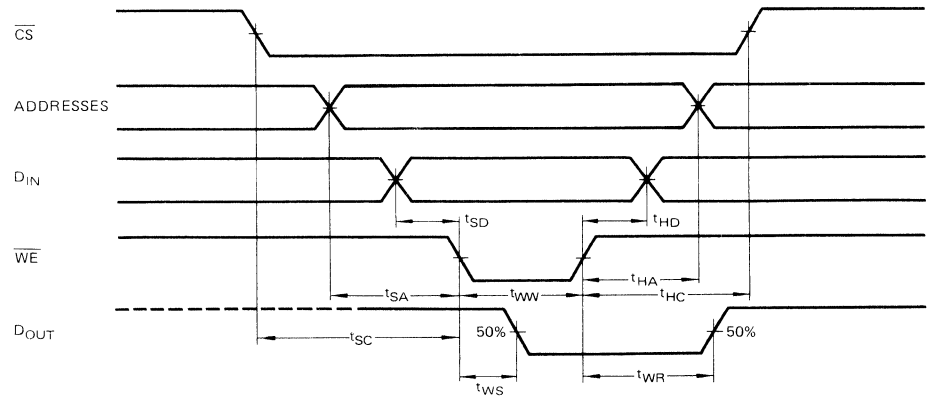
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 100474A-5			MBM 100474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	8			5			ns
Write Disable Time	t_{WS}	0.3		3	0.3		6.5	ns
Write Recovery Time	t_{WR}	0.5		7	0.5		8	ns
Address Set Up Time	t_{SA}	1			1			ns
Chip Select Set Up Time	t_{SC}	0			0			ns
Data Set Up Time	t_{SD}	0			0			ns
Address Hold Time	t_{HA}	1			1			ns
Chip Select Hold Time	t_{HC}	1			1			ns
Data Hold Time	t_{HD}	1			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

1

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

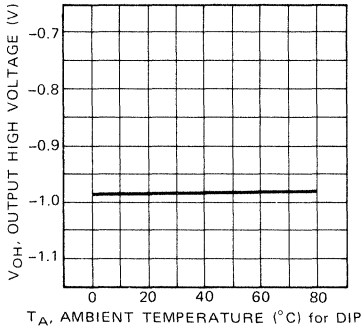


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

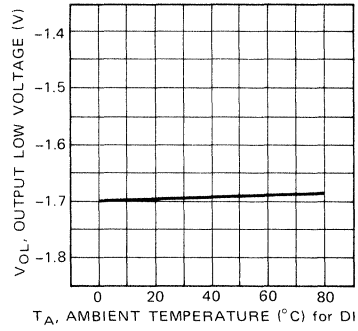


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

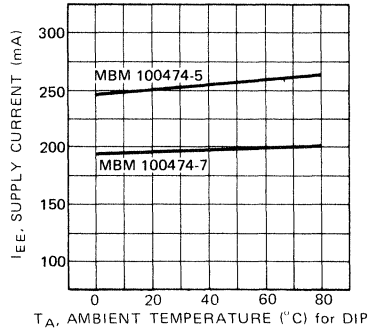


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

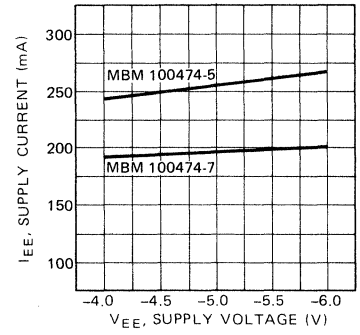


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

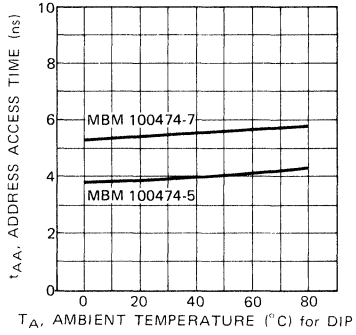


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

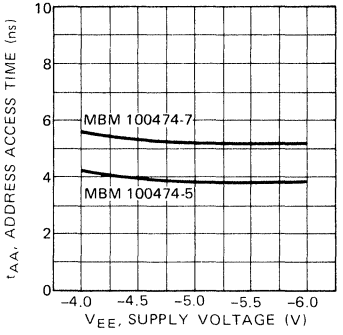


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

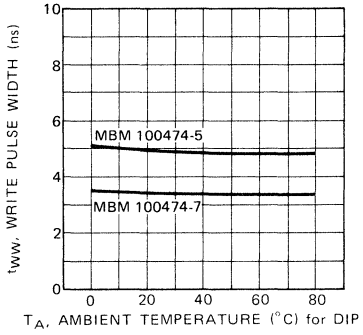
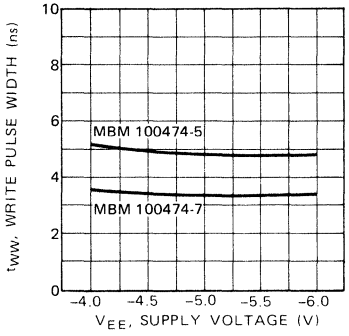


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

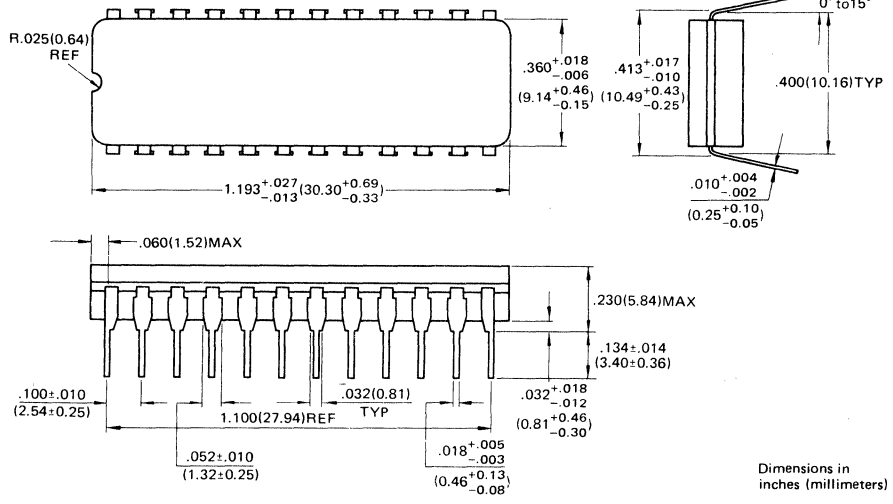


1

PACKAGE DIMENSIONS

(Suffix: -CZ)

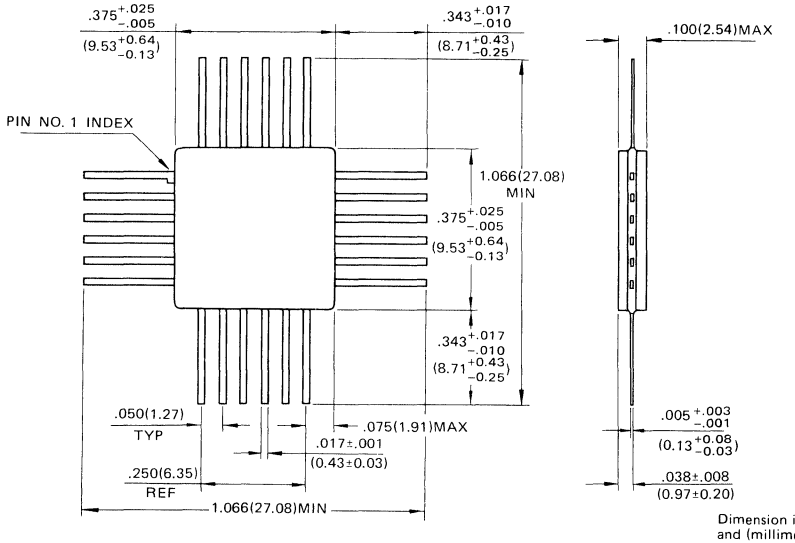
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



PACKAGE DIMENSIONS

(Suffix: -ZF)

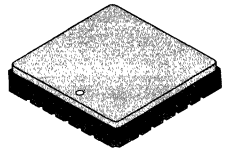
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



Dimension in inches and (millimeters)

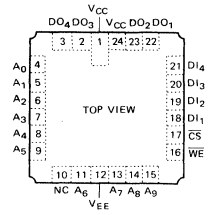
PACKAGE DIMENSIONS

(Suffix: -TV)

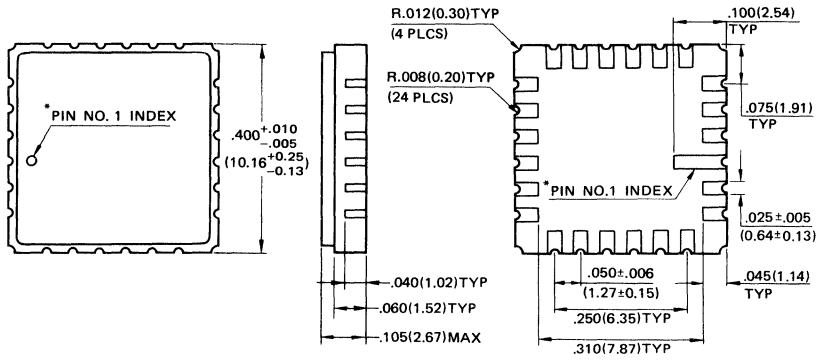


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10474A-10
MBM 10474A-15

August 1985
Edition 2.0

1

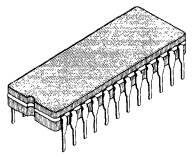
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

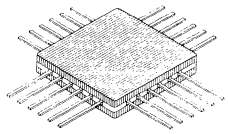
The MBM 10474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10474A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 10 ns max. (MBM 10474A-10)
  15 ns max. (MBM 10474A-15)
- Chip select access time: 6 ns max. (MBM 10474A-10)
  8 ns max. (MBM 10474A-15)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.26 mW/bit typ. (MBM 10474A-10)
  0.20 mW/bit typ. (MBM 10474A-15)
- DOPOS and IOP-II processing
- Pin compatible with the F10474



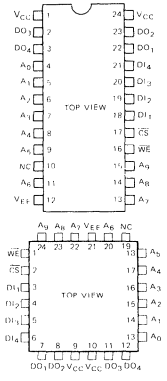
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT



V_{CC} grounded
LCC PAD CONFIGURATION : See page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

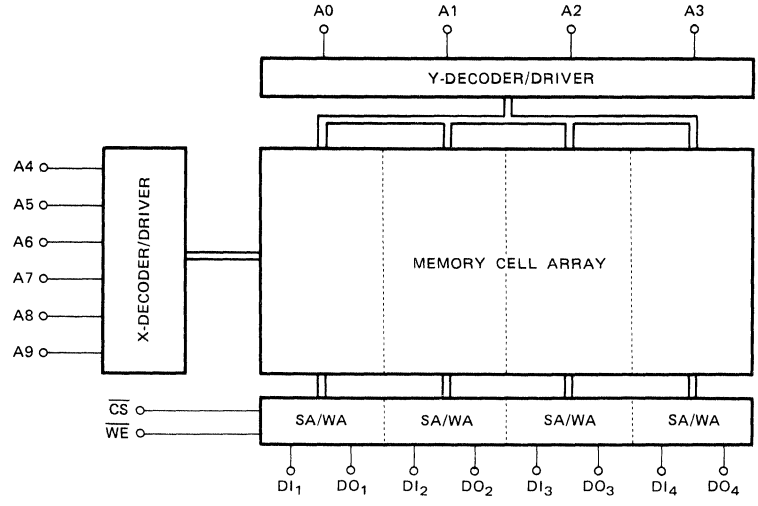
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0° C to 75°C

1

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-10	I_{EE}	-230			mA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-15	I_{EE}	-200			mA	0°C to 75°C

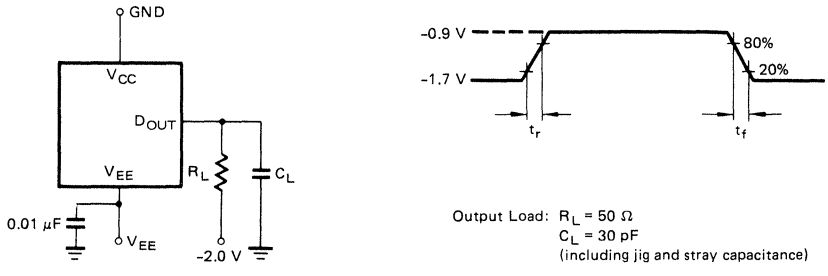
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capcitance	C_{OUT}		6	8	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



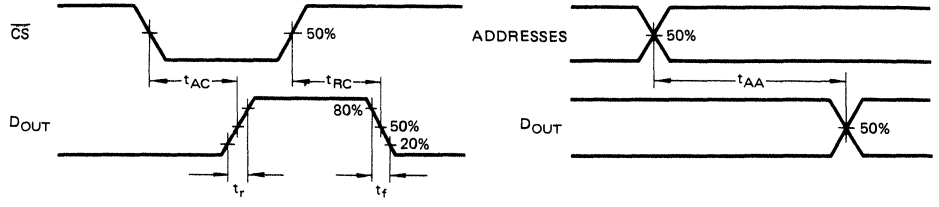
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10474A-10			MBM 10474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	2	7	10	3	10	15	ns
Chip Select Access Time	t_{AC}	1.5	3	6	2	4	8	ns
Chip Select Recovery Time	t_{RC}	1.5	3	6	2	4	8	ns

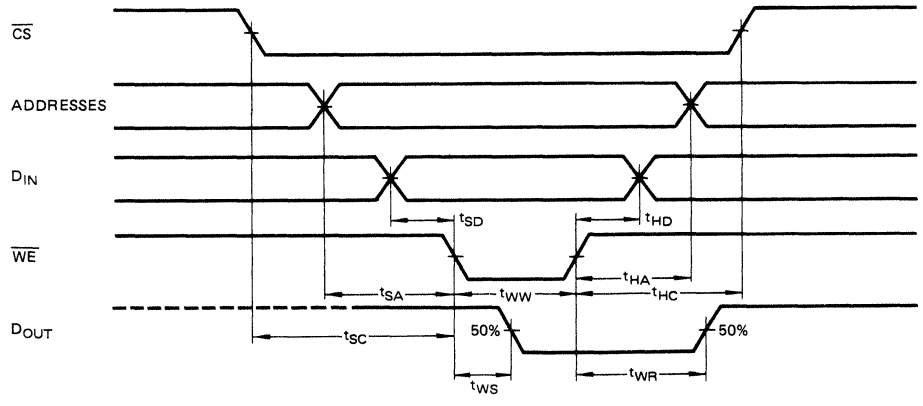
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10474A-10			MBM 10474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			ns
Write Disable Time	t_{WS}			6			8	ns
Write Recovery Time	t_{WR}			10			15	ns
Address Set Up Time	t_{SA}	2			2			ns
Chip Select Set Up Time	t_{SC}	1			2			ns
Data Set Up Time	t_{SD}	1			2			ns
Address Hold Time	t_{HA}	1			3			ns
Chip Select Hold Time	t_{HC}	1			2			ns
Data Hold Time	t_{HD}	1			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	1		3.5	ns
Output Fall Time	t_f	1		3.5	ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

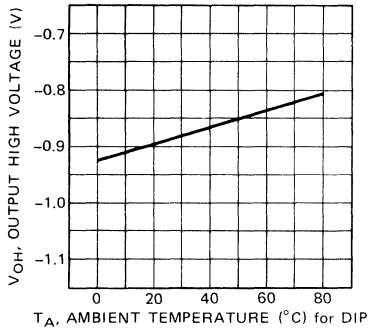


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

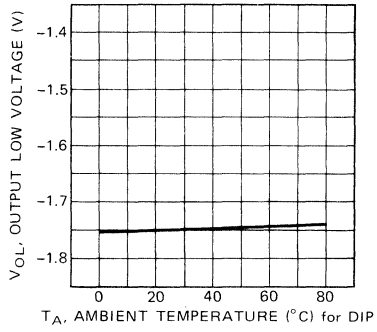


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

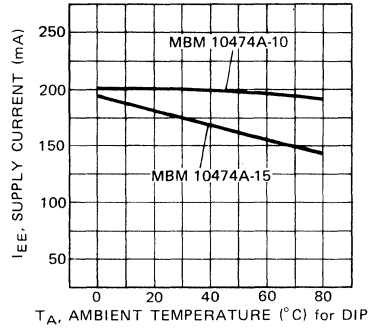


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

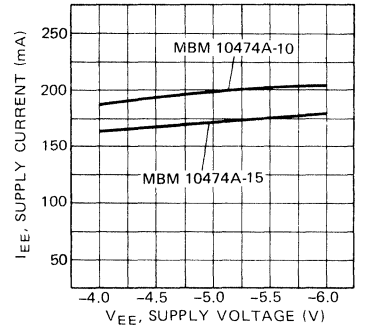


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

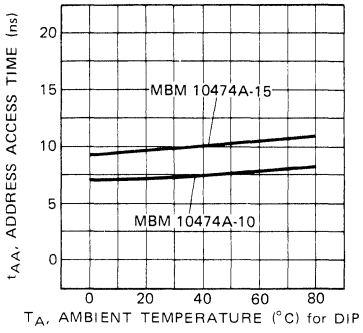


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

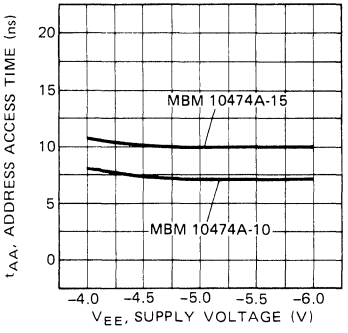


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

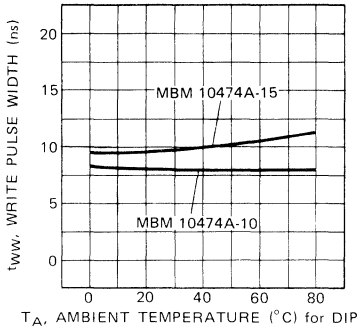
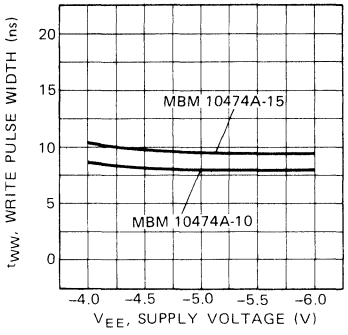


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



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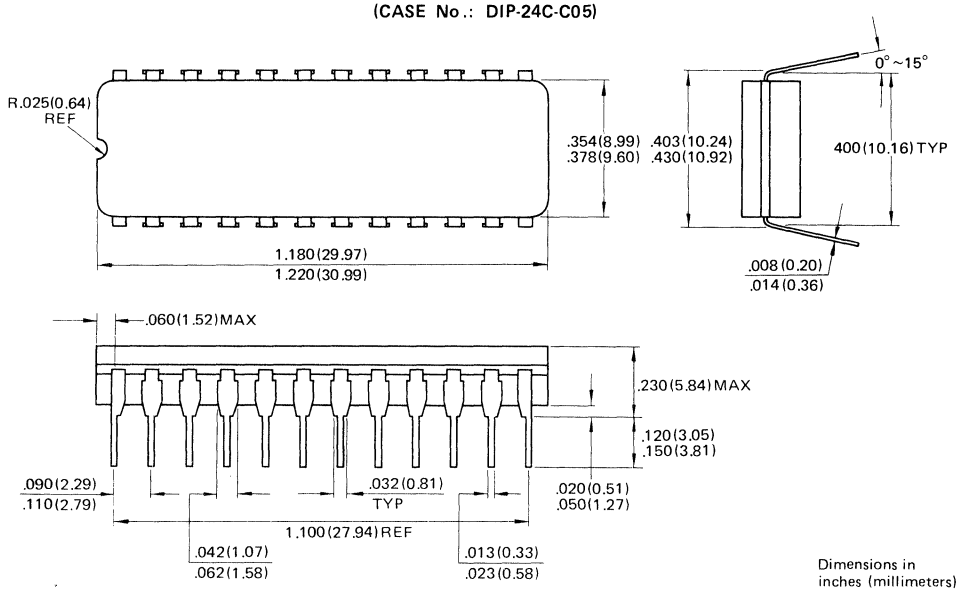
PACKAGE DIMENSIONS

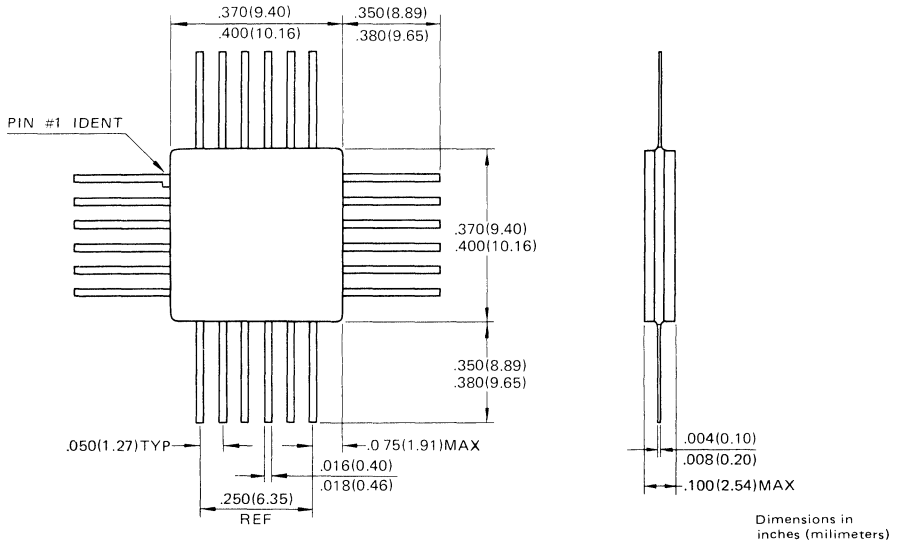
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



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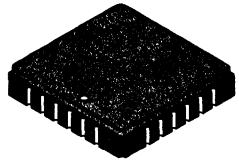
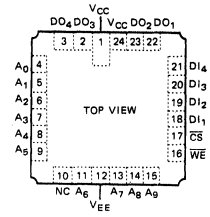
PACKAGE DIMENSIONS

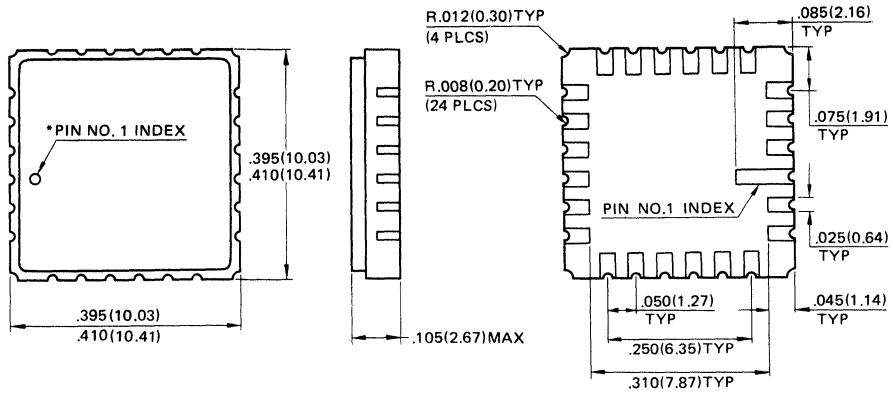


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100474A-10
MBM 100474A-15

August 1985
Edition 2.0

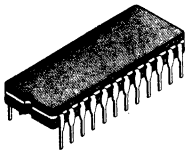
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

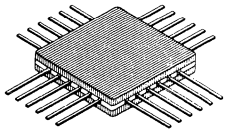
The MBM 100474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Ioslation by Oxide and Polysilicon) processing.

Operation for the MBM 100474A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat package, or LCC. It is fully compatible with industry-standard 100 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 10 ns max. (MBM 100474A-10)
  15 ns max. (MBM 100474A-15)
- Chip select access time: 6 ns max. (MBM 100474A-10)
  8 ns max. (MBM 100474A-15)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.22 mW/bit typ. (MBM 100474A-10)
  0.20 mW/bit typ. (MBM 100474A-15)
- DOPOS and IOP-II processing
- Pin compatible with the F 100474



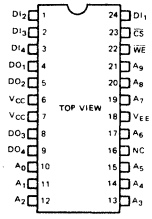
CERAMIC PACKAGE
DIP-24C-C05

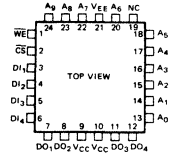


CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT





V_{CC} grounded

LCC PAD CONFIGURATION : See page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

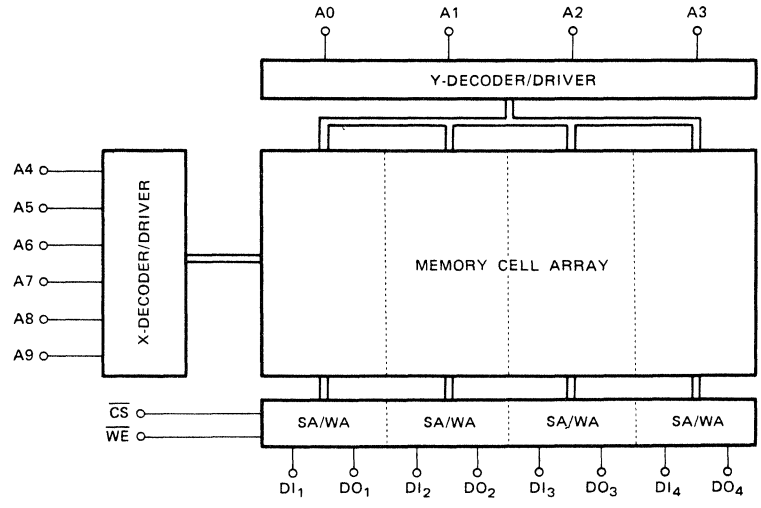
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC.
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

1

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50Ω to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	-1810		-1620	mV
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)		V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage for All Inputs)		V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All inputs and Outputs Open)	MBM 100474A-10	I_{EE}	-230			mA
	MBM 100474A-15		-200			

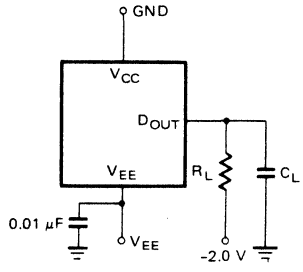
CAPACITANCE

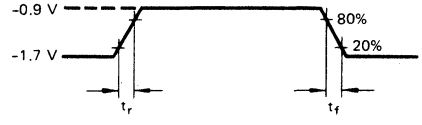
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capacitance	C_{OUT}		6	8	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = –4.5 V ±5%, Output Load = 50 Ω to –2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f$ = 2.5 ns typ

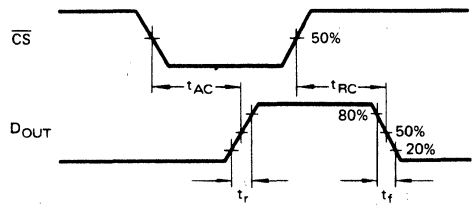
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

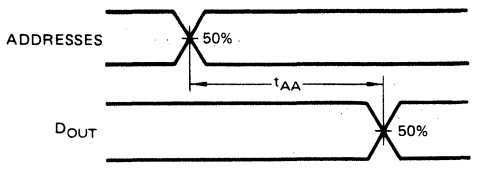
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100474A-10			MBM 100474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	2	7	10	3	10	15	ns
Chip Select Access Time	t_{AC}	1.5	3	6	2	4	8	ns
Chip Select Recovery Time	t_{RC}	1.5	3	6	2	4	8	ns

READ CYCLE TIMING DIAGRAMS

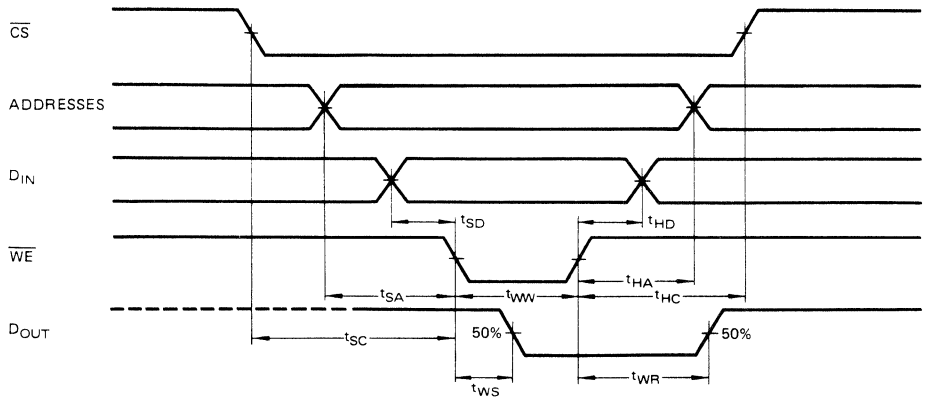




WRITE CYCLE

Parameter	Symbol	MBM 100474A-10			MBM 100474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			ns
Write Disable Time	t_{WS}			6			8	ns
Write Recovery Time	t_{WR}			10			15	ns
Address Set Up Time	t_{SA}	2			2			ns
Chip Select Set Up Time	t_{SC}	1			2			ns
Data Set Up Time	t_{SD}	1			2			ns
Address Hold Time	t_{HA}	1			3			ns
Chip Select Hold Time	t_{HC}	1			2			ns
Data Hold Time	t_{HD}	1			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	1		3.5	ns
Output Fall Time	t_f	1		3.5	ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

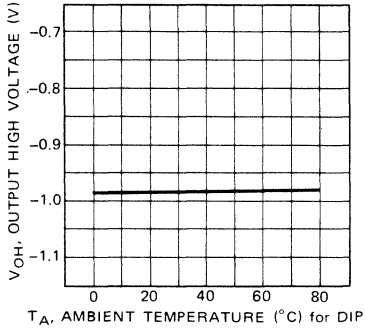


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

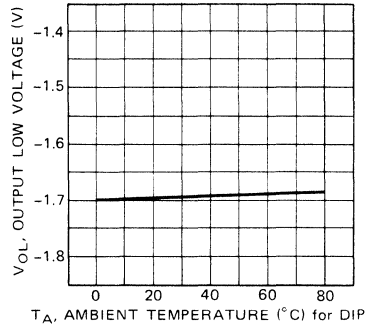


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

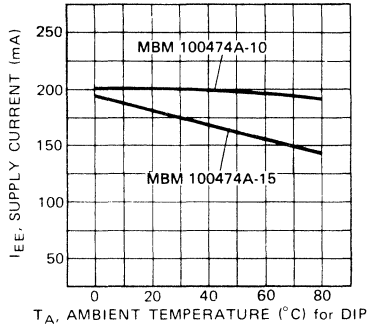


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

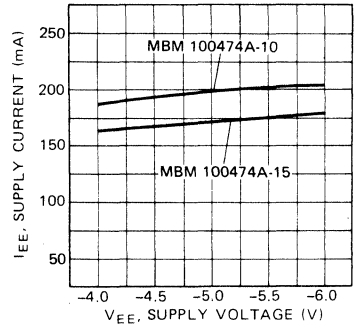


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

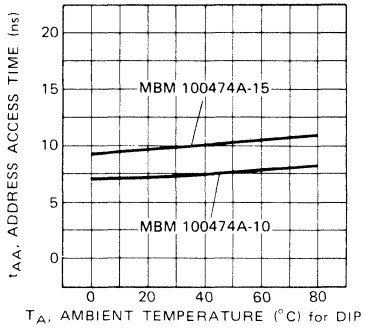


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

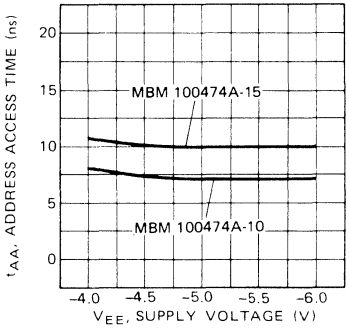


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

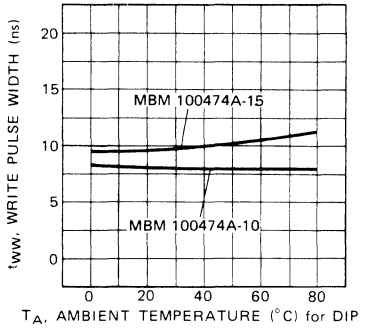
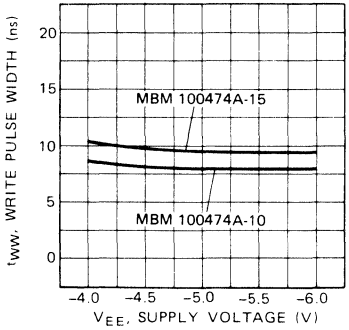


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



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PACKAGE DIMENSIONS

(Suffix: -CZ)

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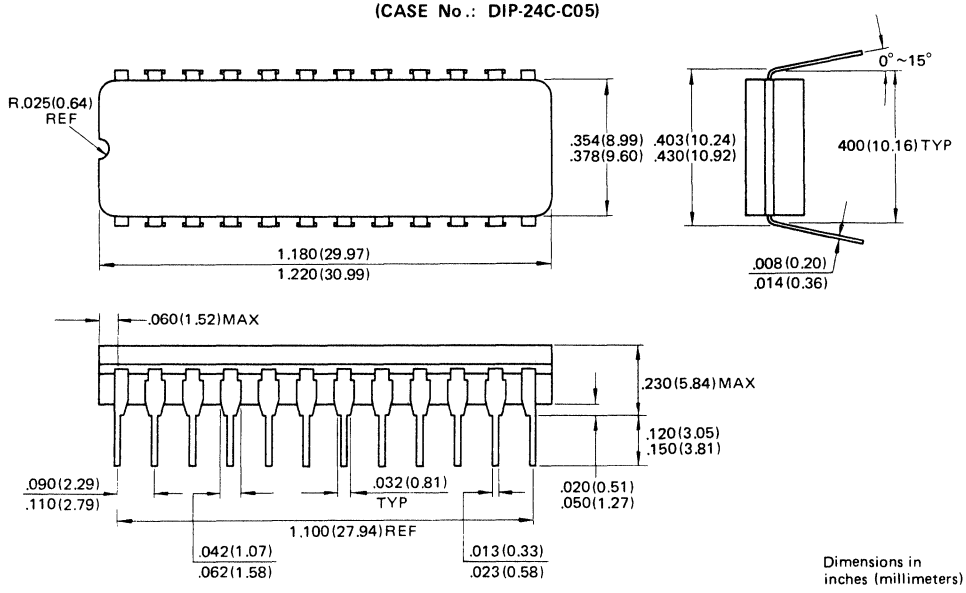
(CASE No.: DIP-24C-C05)



Dimensions in
inches (millimeters)

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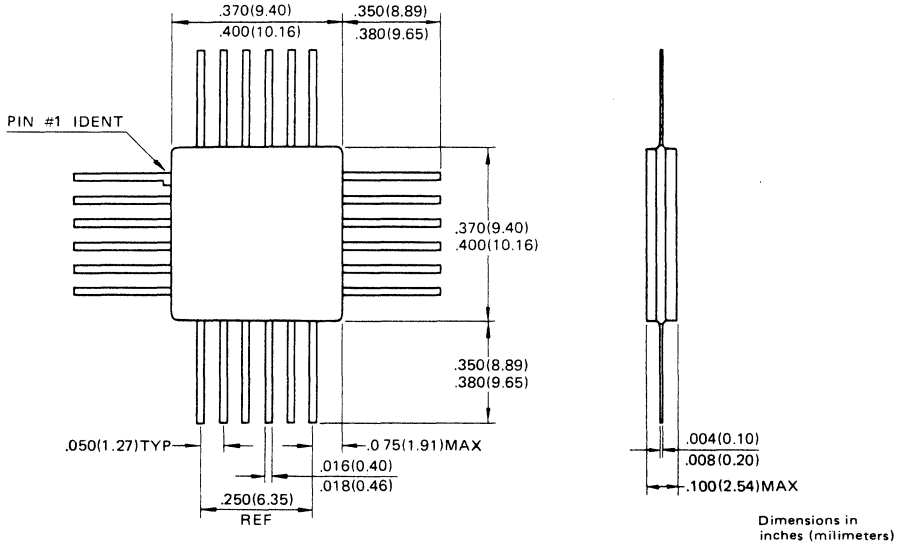
PACKAGE DIMENSIONS

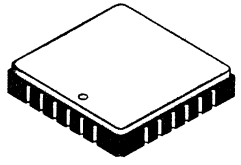
(Suffix: -ZF)

24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



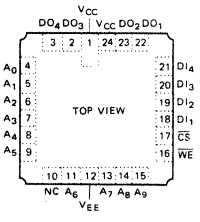
PACKAGE DIMENSIONS

(Suffix: -TV)

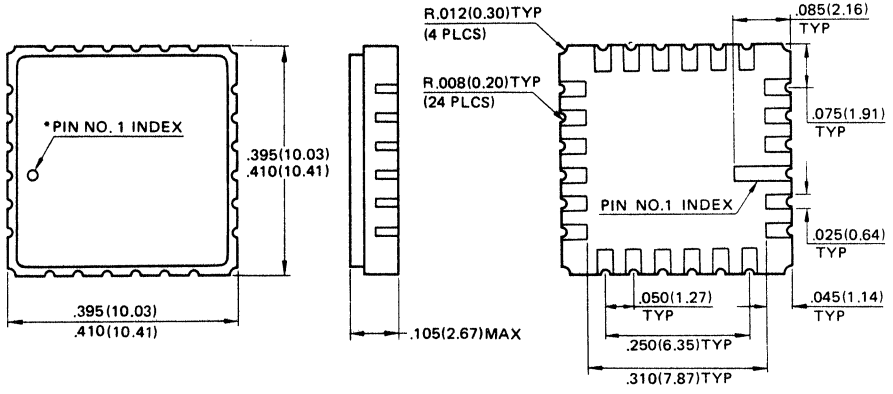


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index: Subject to change without notice

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10480A-8

May 1988
Edition 1.0

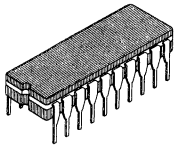
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

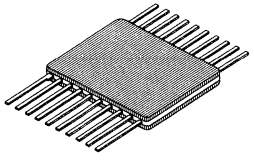
The MBM10480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM10480A is specified over a temperature range of 0°C to 55°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 8 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.07 mW/bit typ
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



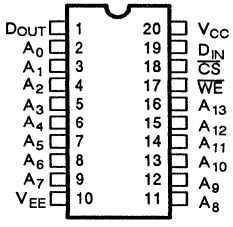
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC PAD CONFIGURATION: See Page 10

ABSOLUTE MAXIMUM RATINGS (see NOTE)

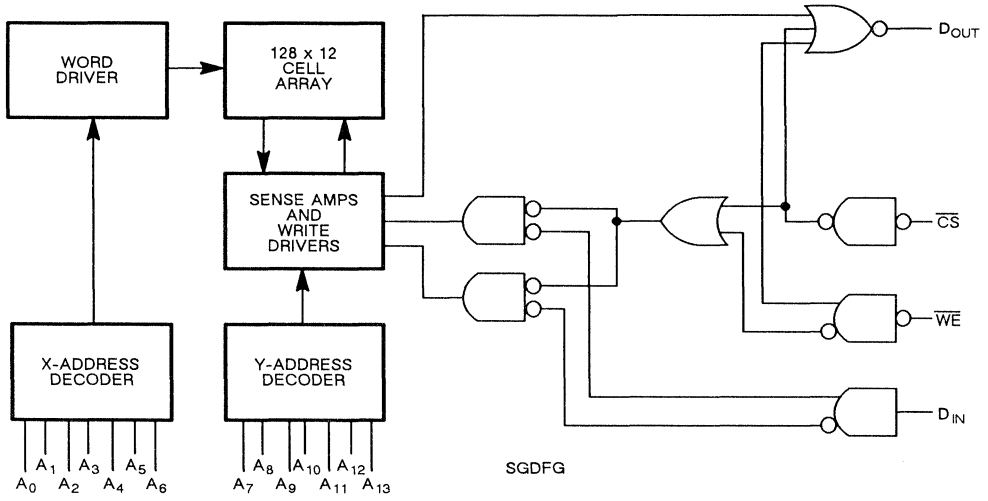
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MBM10480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10480A is a fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, TA = 0°C to 55°C for DIP, Airflow≥ 2.5 m/s, TC=0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -925	—	-840 -810 -760	mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830	—	-1665 -1650 -1625	mV	0°C 25°C 55°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -945	—	—	mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OLC}	—	—	-1645 -1630 -1605	mV	0°C 25°C 55°C
Input High voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1070	—	-840 -810 -760	mV	0°C 25°C 55°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1840	—	-1490 -1475 -1460	mV	0°C 25°C 55°C
Input High Current (VIN=VIH max)	I_{IH}	—	—	220	µA	0°C to 55°C
Input Low Current (VIN=VIL min)	I_{IL}	-50	—	90	µA	0°C to 55°C
CS Input Low Current (VIN=VIL min)	I_{IL}	0.5	—	170	µA	0°C to 55°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-260	—		mA	0°C to 55°C

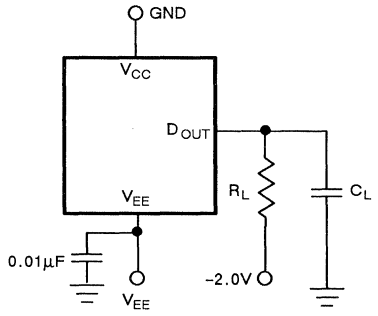
CAPACITANCE

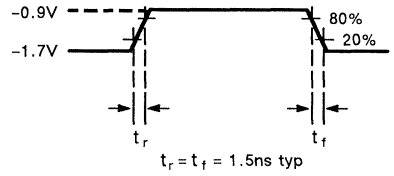
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

AC CHARACTERISTICS

(V_{CC} = 0V, VEE=-5.2V, Output Load=50Ω and 30pF and -2.0V, TA = 0°C to 55°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions



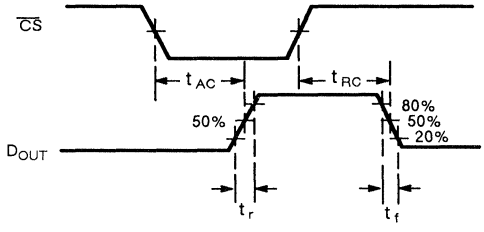


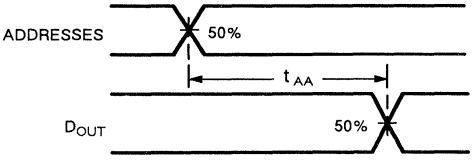
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

Note: All timing measurements referenced to 50% input levels.

Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
READ CYCLE					
Address Access Time	t_{AA}	2	—	8	ns
Chip Select Access Time	t_{AC}	1	—	4	ns
Chip Select Recovery Time	t_{RC}	1	—	4	ns

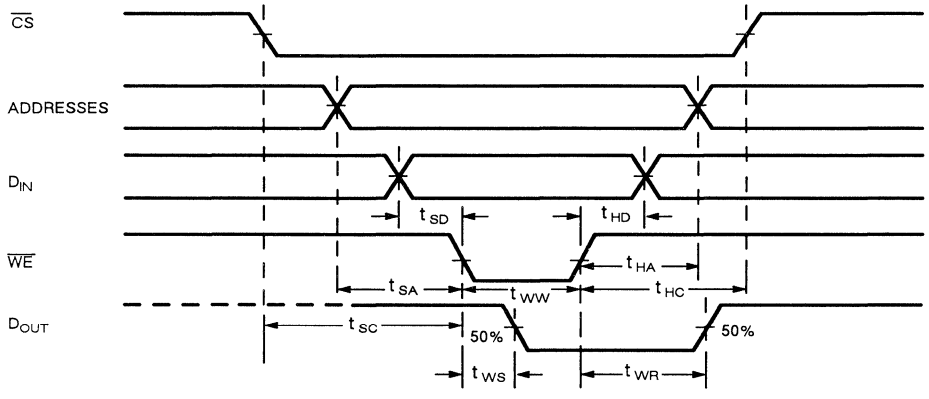
READ CYCLE TIMING DIAGRAMS





Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
WRITE CYCLE					
Write Pulse Width	t_{WW}	10	—	—	ns
Write Disable Time	t_{WS}	—	—	4	ns
Write Recovery Time	t_{WR}	—	—	11	ns
Address Set Up Time	t_{SA}	2	—	—	ns
Chip Select Set Up Time	t_{SC}	2	—	—	ns
Data Set Up Time	t_{SD}	2	—	—	ns
Address Hold Time	t_{HA}	1	—	—	ns
Chip Select Hold Time	t_{HC}	1	—	—	ns
Data Hold Time	t_{HD}	1	—	—	ns

WRITE CYCLE TIMING DIAGRAMS



Parameter	Symbol	Min	Typ	Max	Unit
RISE TIME and FALL TIME					
Output Rise Time	t_r	—	2	—	ns
Output Fall Time	t_f	—	2	—	ns

TYPICAL PERFORMANCE CHARACTERISTICS

1

Fig. 3 — OUTPIT HIGH VOLTAGE vs AMBIENT TEMPERATURE

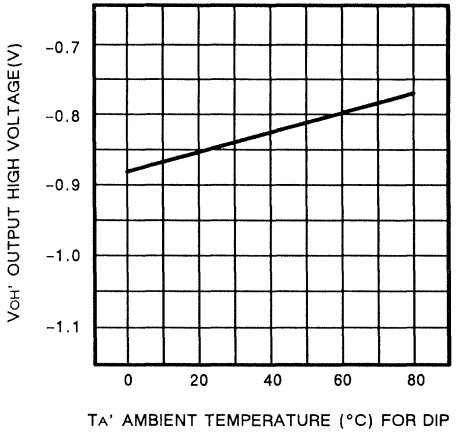


Fig. 4 — OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

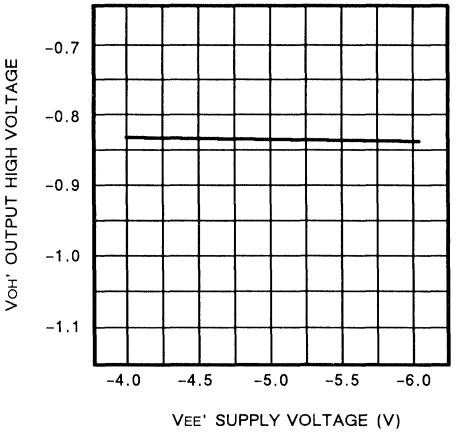


Fig. 5 — OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

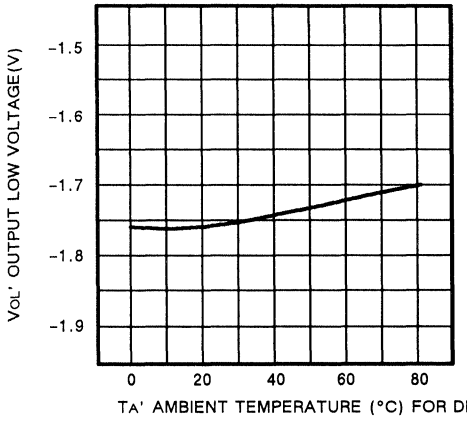
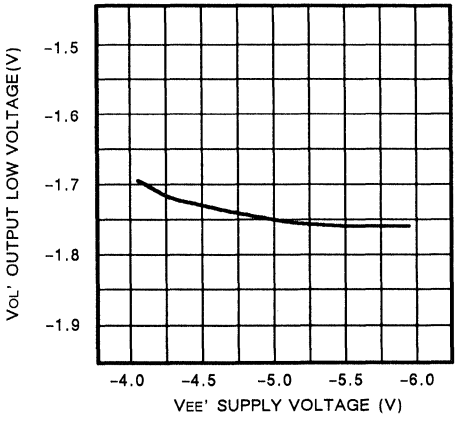


Fig. 6 — OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 7 — SUPPLY CURRENT vs AMBIENT TEMPERATURE

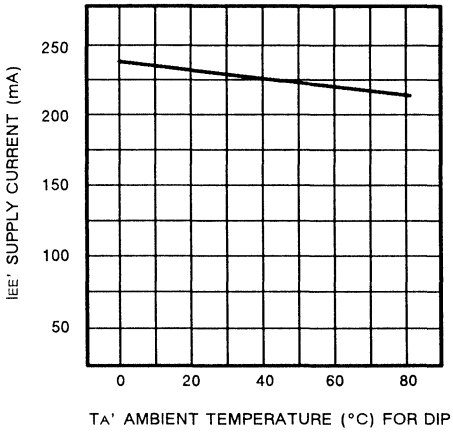


Fig. 8 — SUPPLY CURRENT vs SUPPLY VOLTAGE

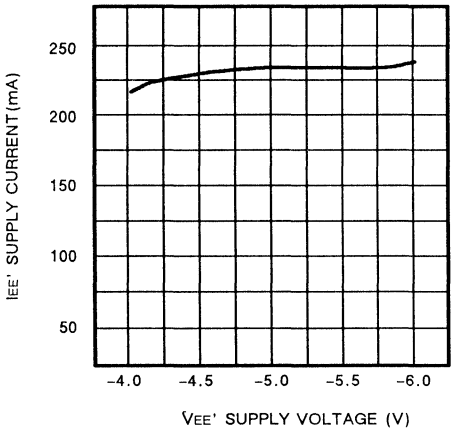


Fig. 9 — ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

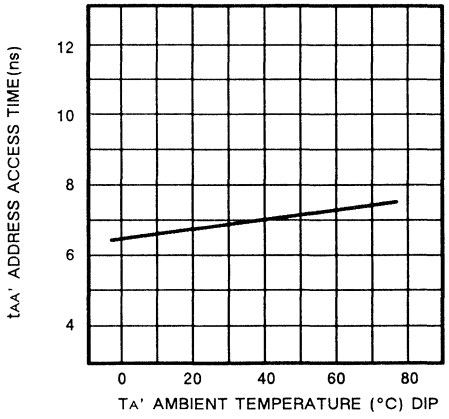
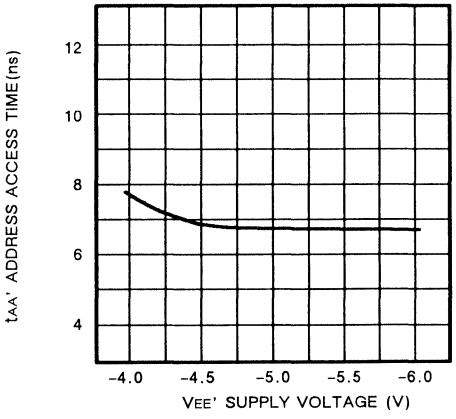


Fig. 10 — ADDRESS ACCESS TIME vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 11 — WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

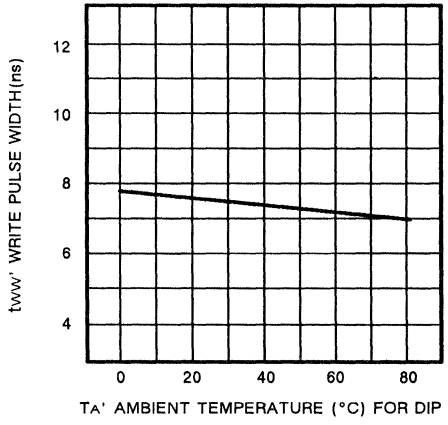
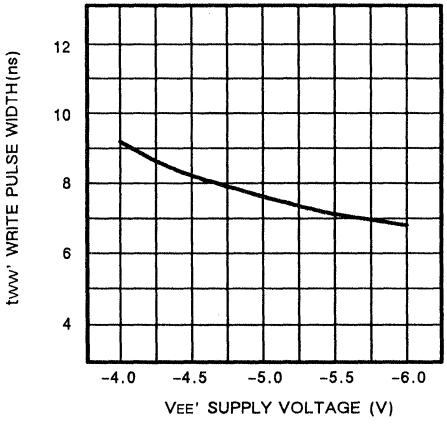
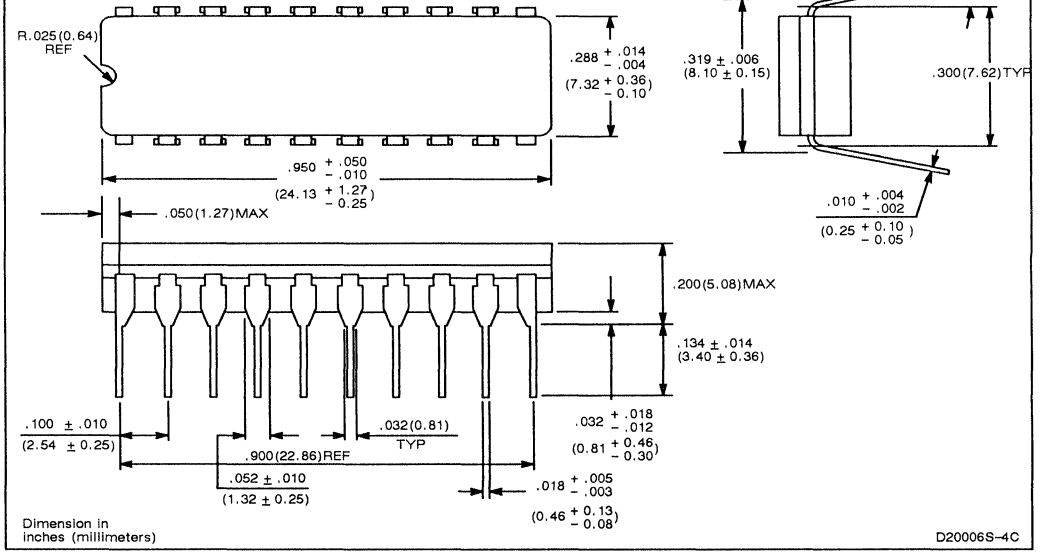


Fig. 12 — WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

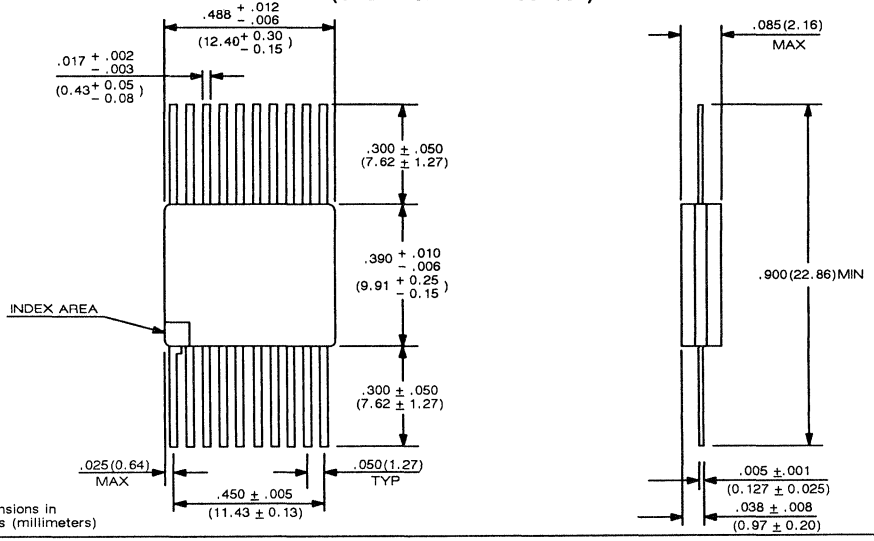
20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimension in inches (millimeters)

D20006S-4C

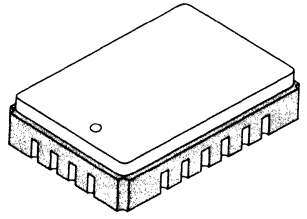
20-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-20C-C01)



Dimensions in inches (millimeters)

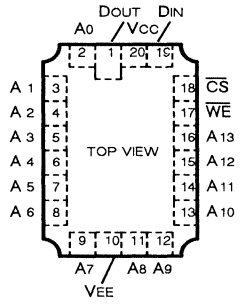
F20004S-2C

PACKAGE DIMENSIONS (Continued)

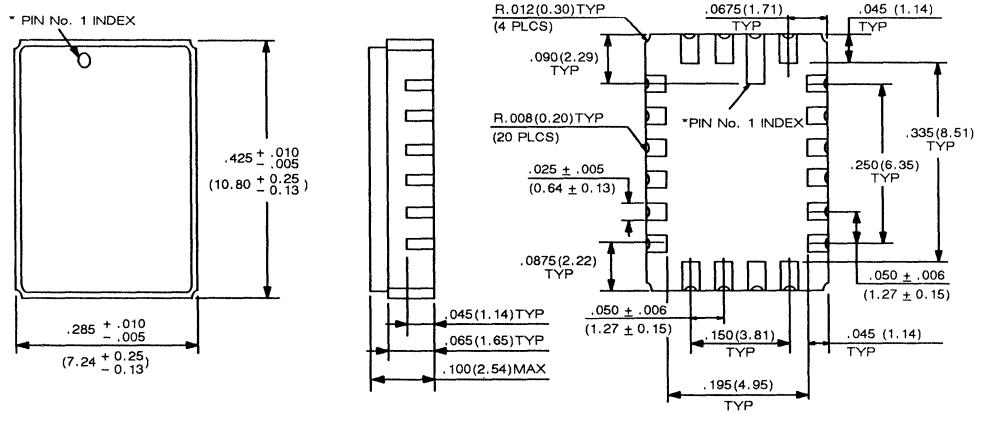


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIERS
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100480A-8

May 1988
Edition 1.0

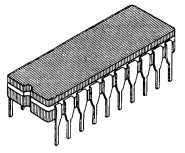
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

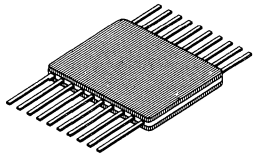
The MBM100480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) Processing.

Operation for the MBM100480A is specified over a temperature range of from 0°C to 65°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 16384 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K series ECL families
- Address access time: 8 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.06 mW/bit (typ.)
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



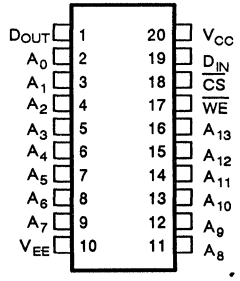
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC Pad Configuration: See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

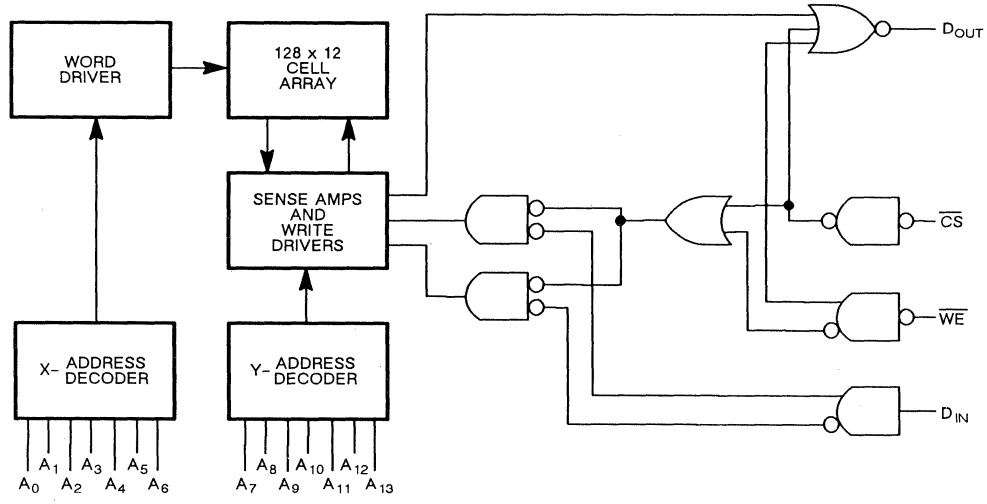
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to **Absolute Maximum Rating** conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

1

Fig. 1 — MBM100480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100480A is fully decoded 16384 bit read/write random access memory organized as 16384 words by 1 bit. Memory cell selection is achieved by means of a 14-bit address designated A0 through A13. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 65°C

DC CHARACTERISTICS

(VCC=0V, VEE=-4.5V, Output Load=50Ω and 30pF to -2.0V, TA=0°C to 65°C for DIP, Airflow≥ 2.5m/s, TC=0°C to 5°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025	—	-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810	—	-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035	—	—	mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}	—	—	-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165	—	-880	
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810	—	-1475	
Input High Current (VIN = VIH max)	I_{IH}	—	—	220	μA
Input Low Current (VIN = VIL min)	I_{IL}	—	—	90	μA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5	—	170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-260	—	—	mA

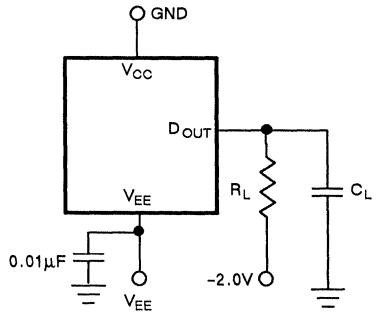
CAPACITANCE

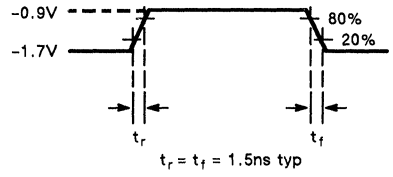
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V ±5%, Output Load=50Ω to -2.0V and 30 pF to GND, TA=0°C to 65°C for DIP, Airflow ≧ 2.5m/s, TC=0°C to 65°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions



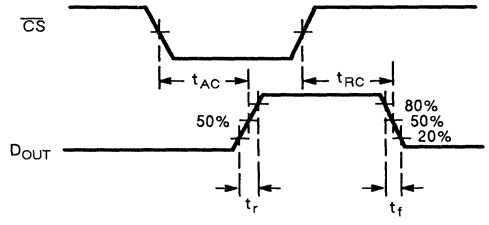


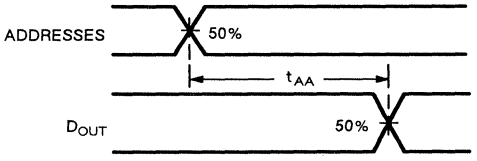
Output Load: R_L = 50Ω
C_L = 30pF
(including spoce and jig)

Note: All timing measurements referenced to 50% input levels.

Parameter	Symbol	MBM100480A-8			Unit
		Min	Typ	Max	
READ CYCLE					
Address Access Time	t_{AA}	2	—	8	ns
Chip Select Access Time	t_{AC}	1	—	4	ns
Chip Select Recovery Time	t_{RC}	1	—	4	ns

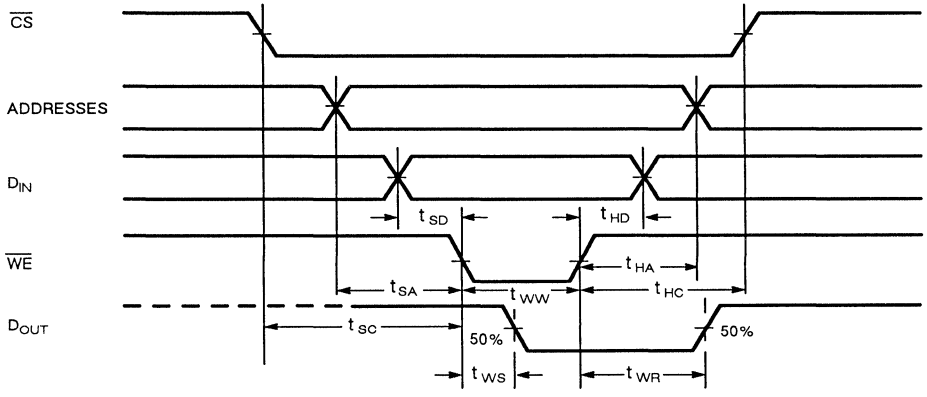
READ CYCLE TIMING DIAGRAMS





Parameter	Symbol	MBM100480A-8			Unit
		Min	Typ	Max	
WRITE CYCLE					
Write Pulse Width	t_{WW}	10	—		ns
Write Disable Time	t_{WS}	—	—	4	ns
Write Recovery Time	t_{WR}	—	—	11	ns
Address Set Up Time	t_{SA}	2	—	—	ns
Chip Select Set Up Time	t_{SC}	2	—	—	ns
Data Set Up Time	t_{SD}	2	—	—	ns
Address Hold Time	t_{HA}	1	—	—	ns
Chip Select Hold Time	t_{HC}	1	—	—	ns
Data Hold Time	t_{HD}	1	—	—	ns

WRITE CYCLE TIMING DIAGRAMS



Parameter	Symbol	Min	Typ	Max	Unit
RISE TIME and FALL TIME					
Output Rise Time	t_r	—	2	—	ns
Output Fall Time	t_f	—	2	—	ns

TYPICAL PERFORMANCE CHARACTERISTICS

1

Fig. 3 — OUTPIT HIGH VOLTAGE vs AMBIENT TEMPERATURE

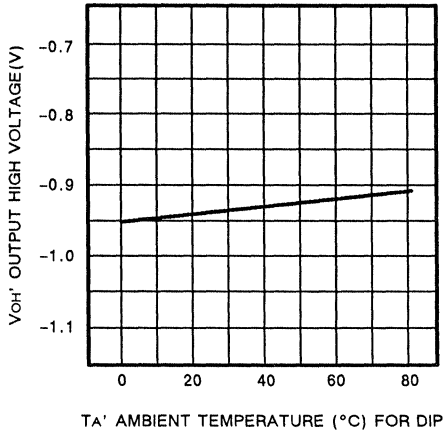


Fig. 4 — OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

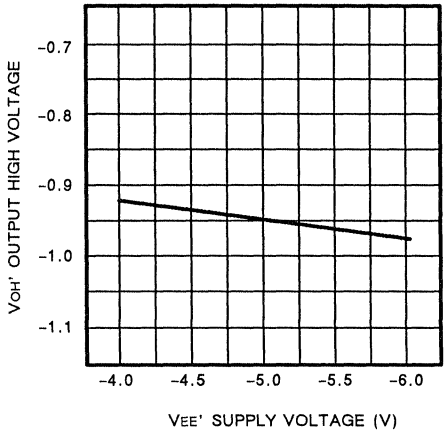


Fig. 5 — OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

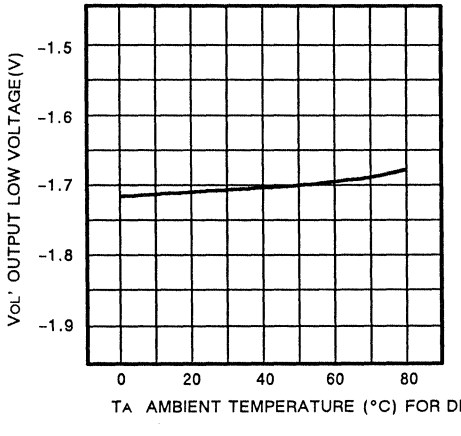
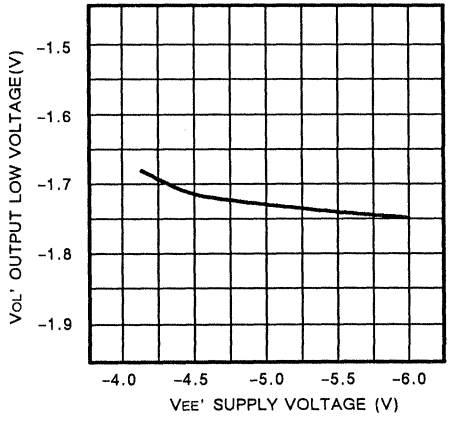


Fig. 6 — OUYPUT LOW VOLTAGE vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 7 — SUPPLY CURRENT vs AMBIENT TEMPERATURE

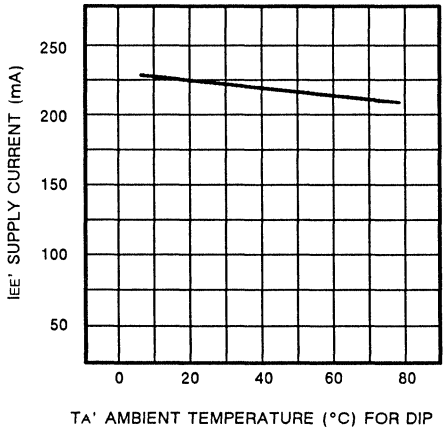


Fig. 8 — SUPPLY CURRENT vs SUPPLY VOLTAGE

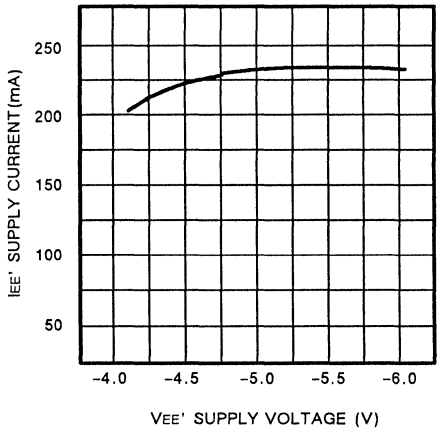


Fig. 9 — ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

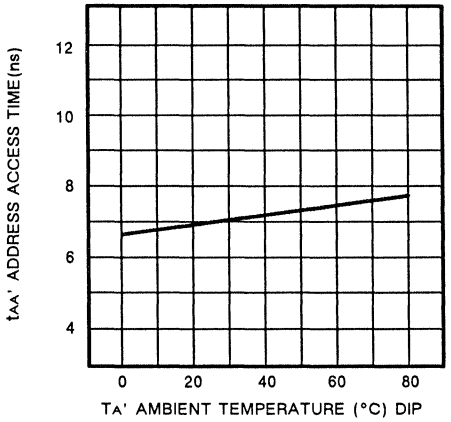
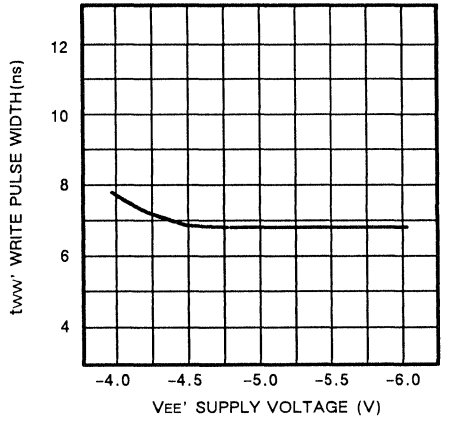


Fig. 10 — ADDESS ACCESS TIME vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 11 — WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

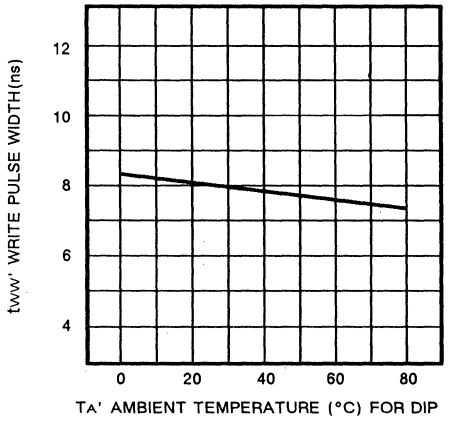
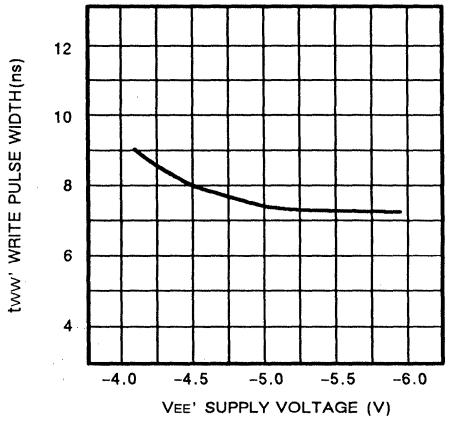
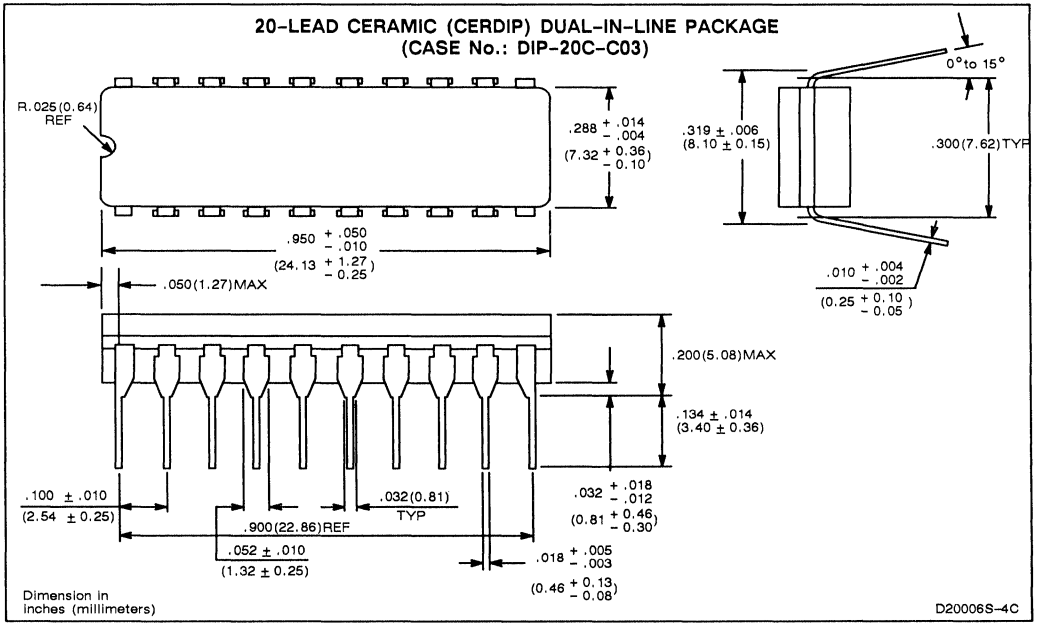


Fig. 12 — WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

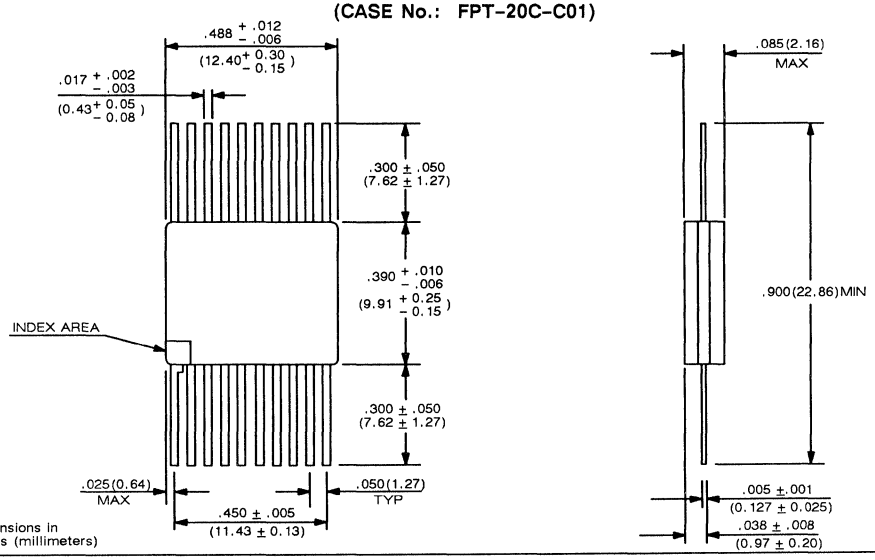
20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimension in inches (millimeters)

D20006S-4C

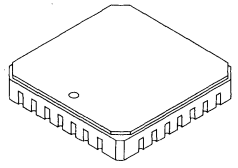
20-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-20C-C01)



Dimensions in inches (millimeters)

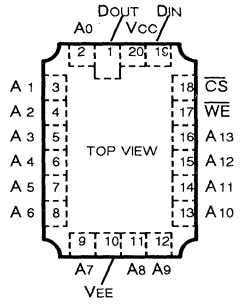
F20004S-2C

PACKAGE DIMENSIONS (Continued)

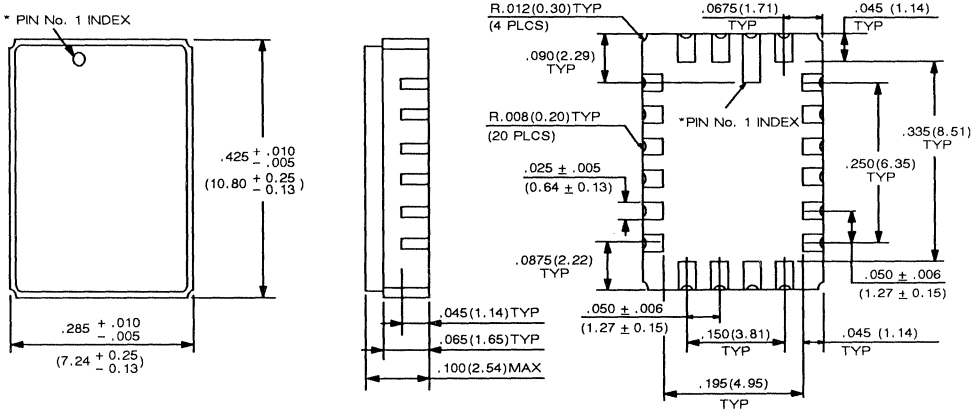


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10480A-10

May 1988
Edition 1.0

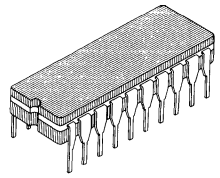
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

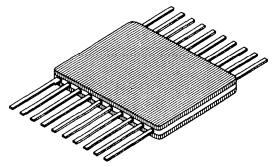
The MBM10480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM10480A is specified over a temperature range of 0°C to 55°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 10 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.07 mW/bit typ
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



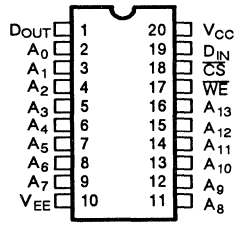
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC Pad Configuration: See Page 10

ABSOLUTE MAXIMUM RATINGS (see NOTE)

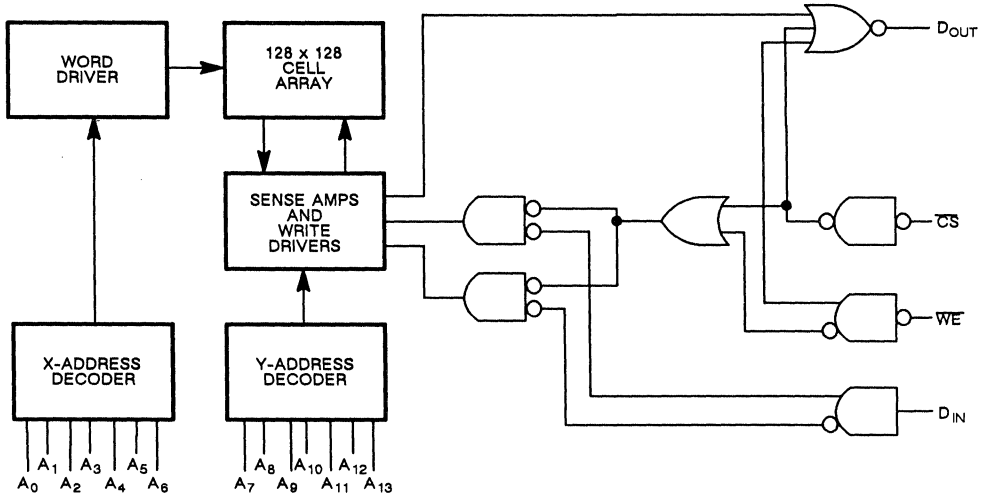
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MBM10480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

Notes:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10480A is a fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data in D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-or connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω and 30 pF to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Inout High Voltage (Guarenteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Inout Low Voltage (Guarenteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-220			mV	0°C to 75°C

CAPACITANCE

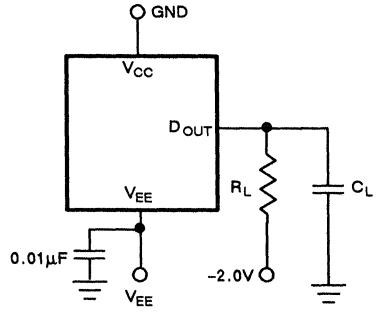
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

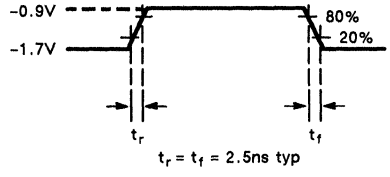
1

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions





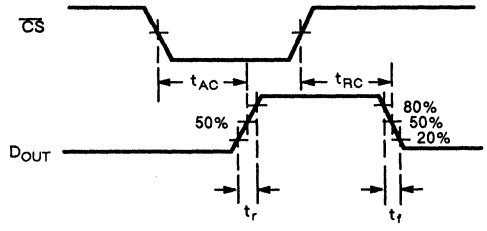
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

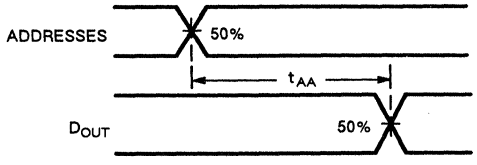
Note: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

READ CYCLE TIMING DIAGRAMS

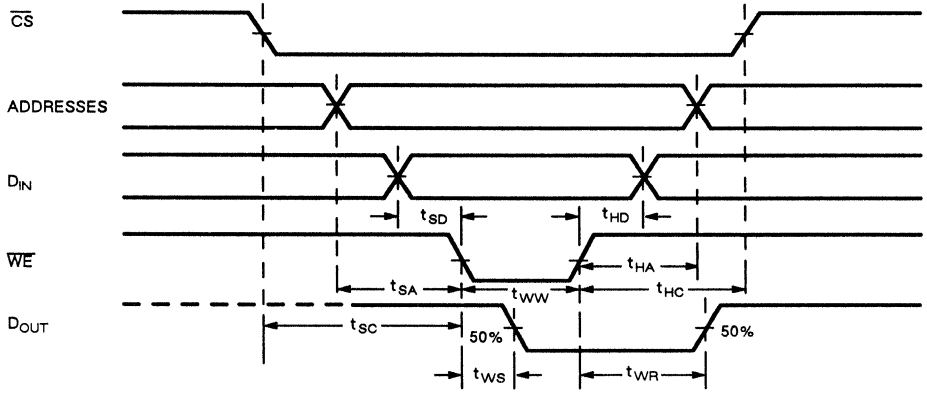




WRITE CYCLE

Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

1

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Output High Voltage vs Ambient Temperature

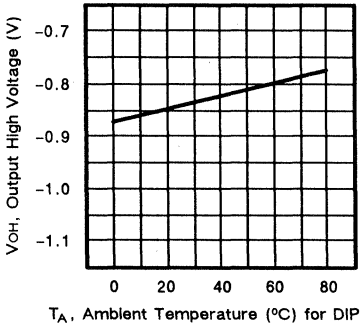


Fig. 4 – Output High Voltage vs Supply Voltage

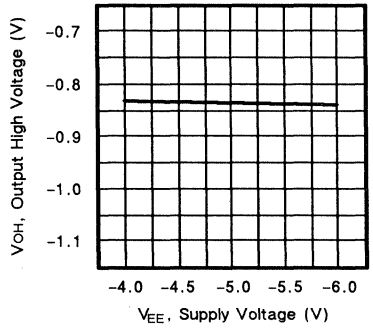


Fig. 5 – Output Low Voltage vs Ambient Temperature

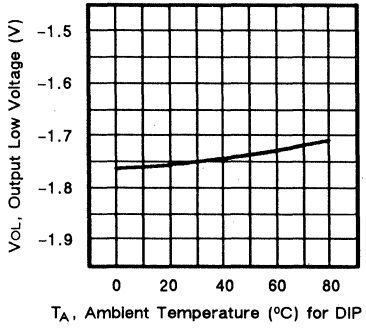


Fig. 6 – Output Low Voltage vs Supply Voltage

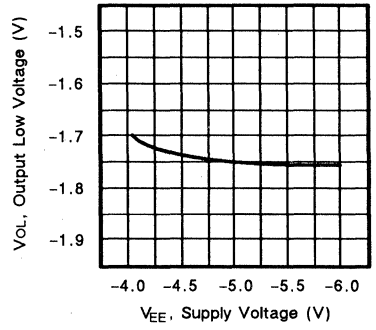


Fig. 7 – Supply Current vs Ambient Temperature

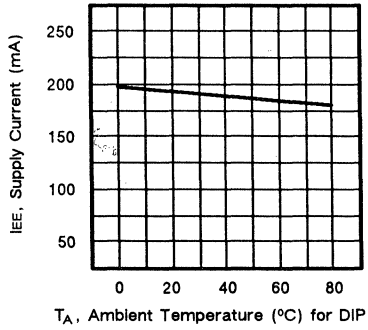
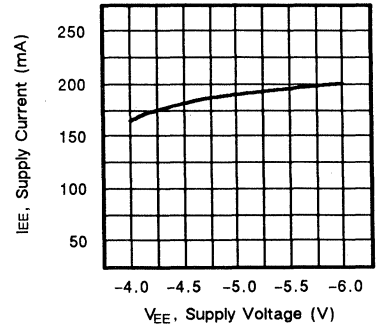


Fig. 8 – Supply Current vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 – Address Access Time vs Ambient Temperature

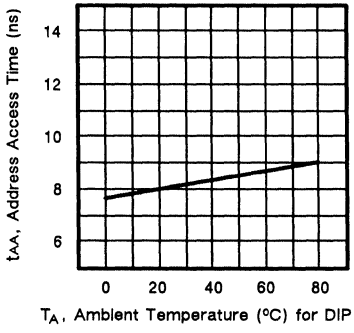


Fig. 10 – Address Access Time vs Supply Voltage

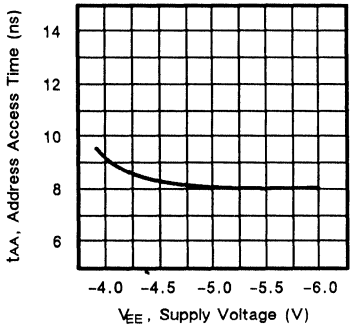


Fig. 11 – Write Pulse Width vs Ambient Temperature

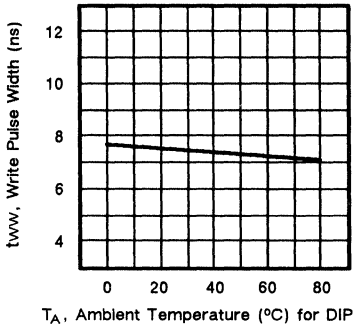
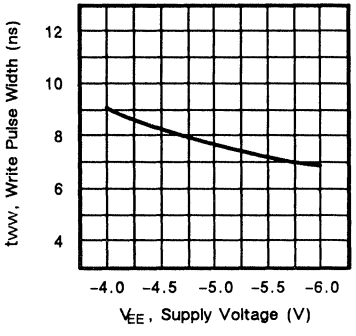


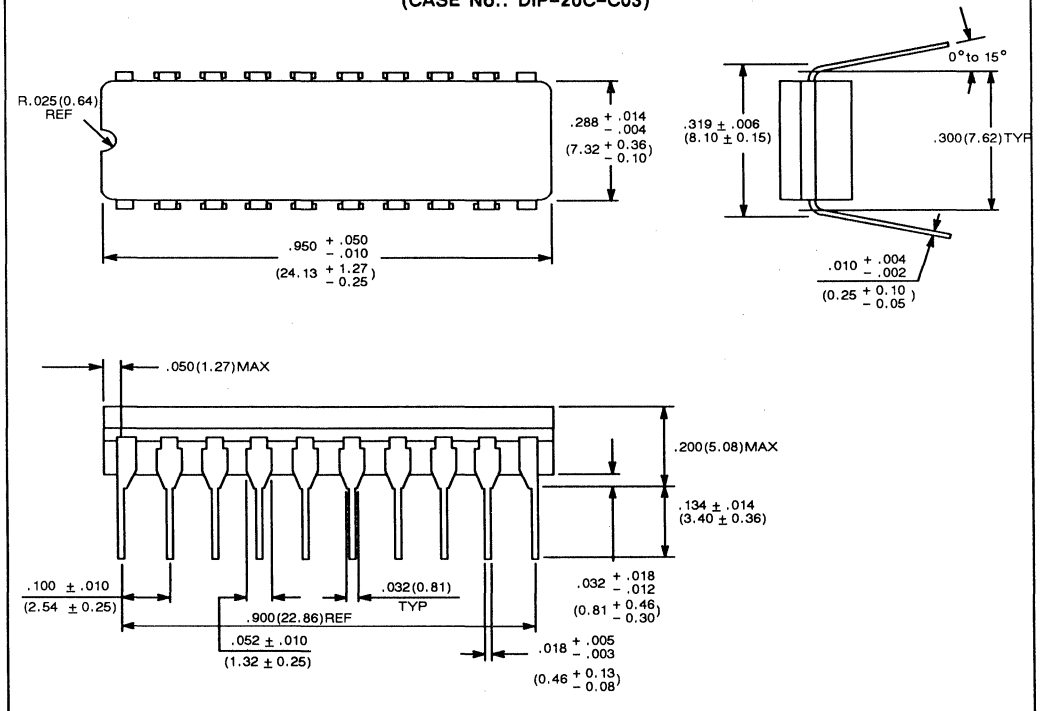
Fig. 12 – Write Pulse Width vs Supply Voltage



1

PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

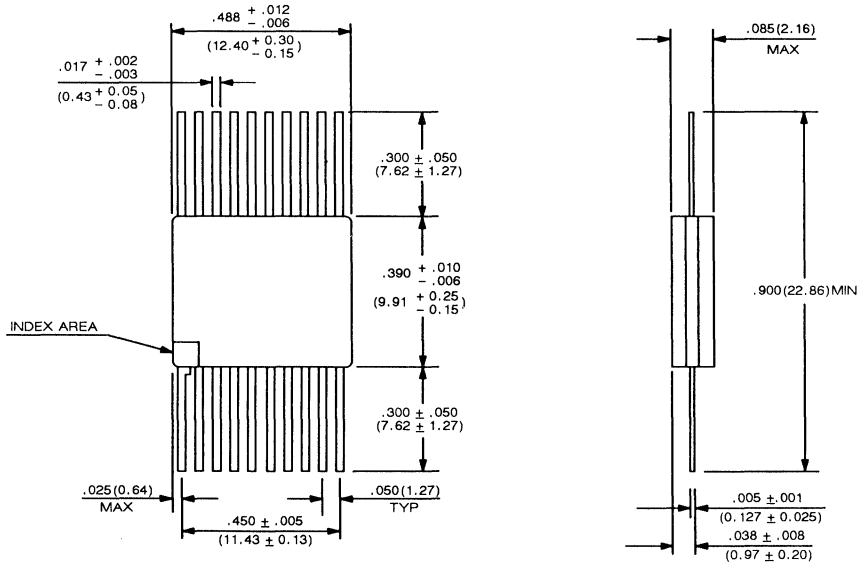


Dimension in inches (millimeters)

D20006S-4C

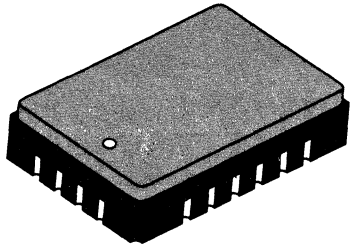
PACKAGE DIMENSIONS (continued)

20-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-20C-C01)



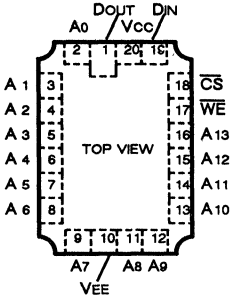
Dimensions in
inches (millimeters)

F20004S-2C

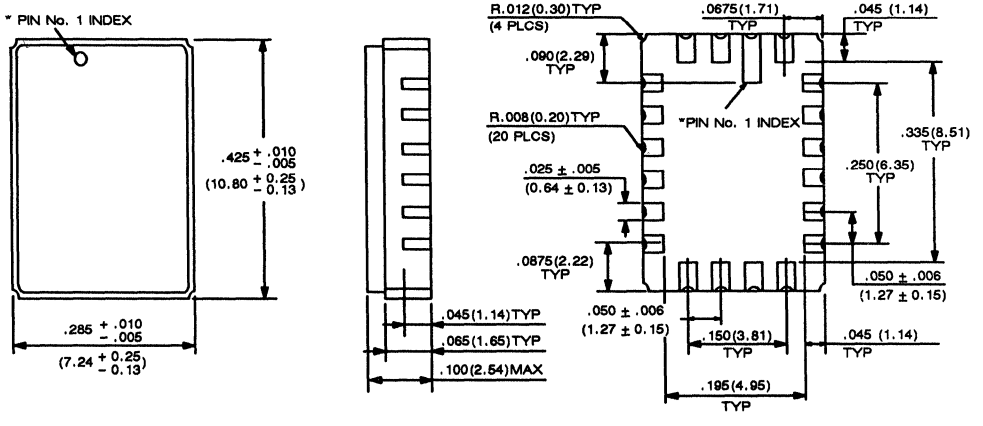


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100480A-10

May 1988
Edition 1.0

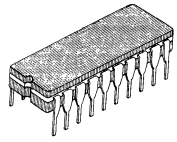
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

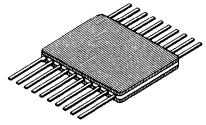
The MBM100480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) Processing.

Operation for the MBM100480A is specified over a temperature range of from 0°C to 65°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 16384 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K series ECL families
- Address access time: 8 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.06 mW/bit (typ.)
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



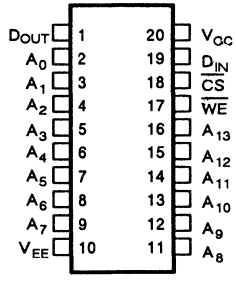
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC Pad Configuration: See Page 10

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

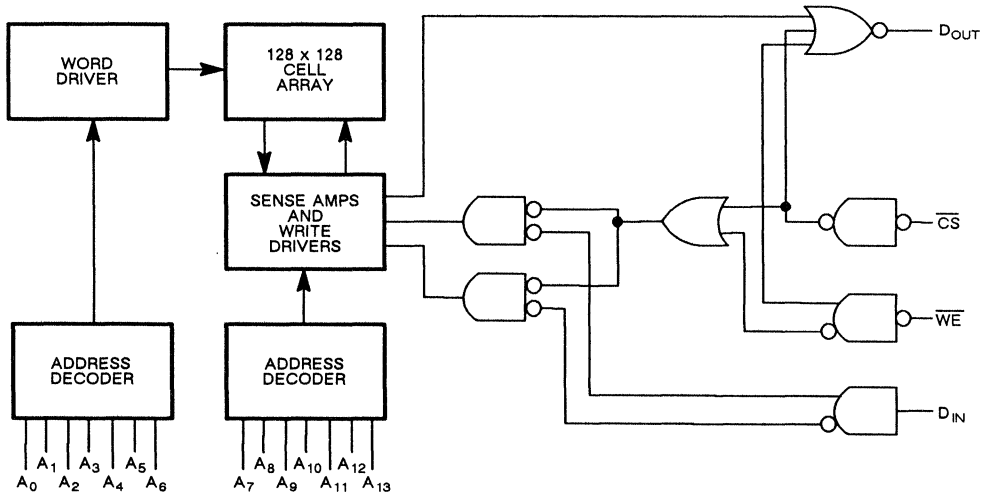
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to **Absolute Maximum Rating** conditions for extended periods may affect device reliability.

1

Fig. 1 — MBM100480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

Notes:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100480A is fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then trasferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50 Ω and 30 pF to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	µA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-220			mA

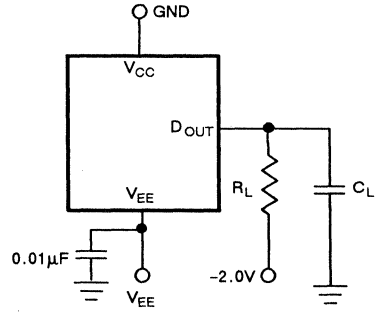
CAPACITANCE

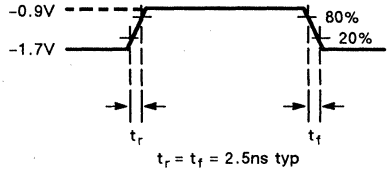
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions





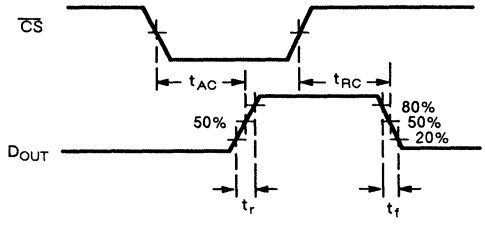
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

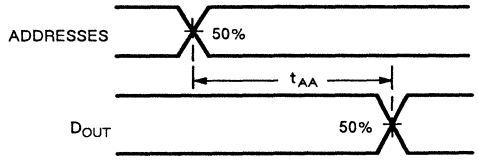
Note: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM100480A-10			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

READ CYCLE TIMING DIAGRAMS





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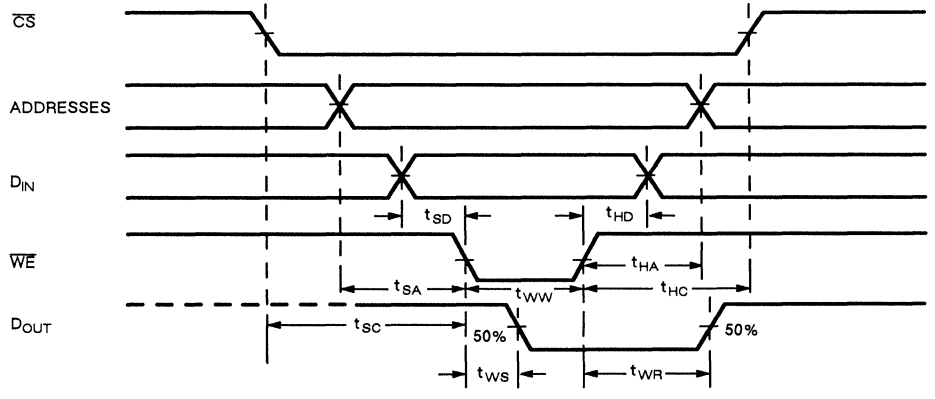
WRITE CYCLE

Parameter	Symbol	MBM100480A-10			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Output High Voltage vs Ambient Temperature

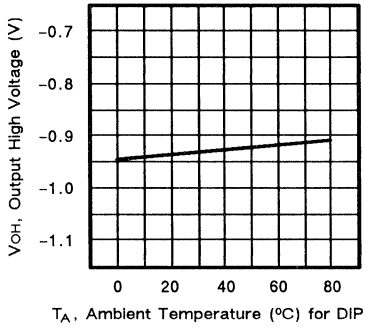


Fig. 4 – Output High Voltage vs Supply Voltage

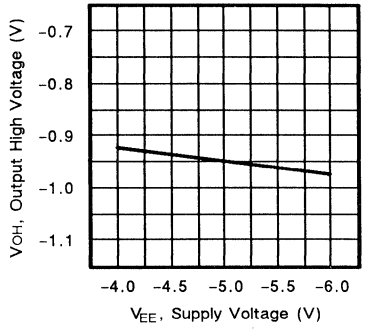


Fig. 5 – Output Low Voltage vs Ambient Temperature

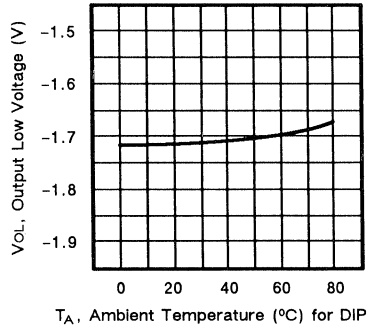


Fig. 6 – Output Low Voltage vs Supply Voltage

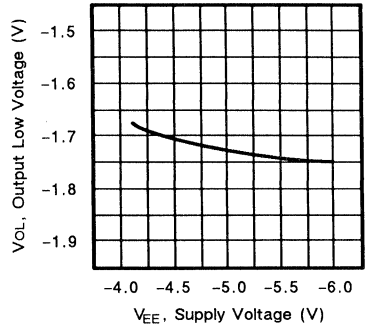


Fig. 7 – Supply Current vs Ambient Temperature

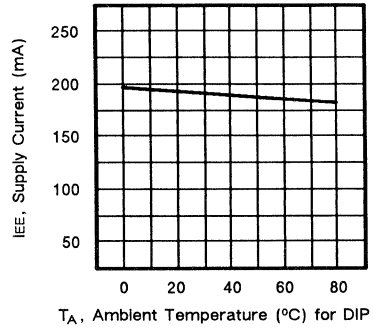
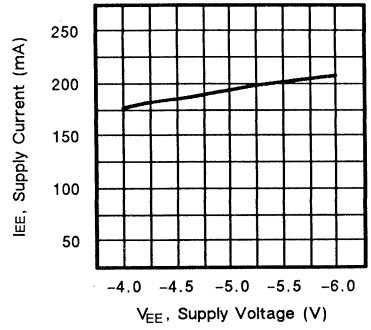


Fig. 8 – Supply Current vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 – Address Access Time vs Ambient Temperature

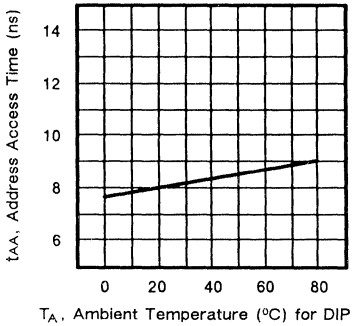


Fig. 10 – Address Access Time vs Supply Voltage

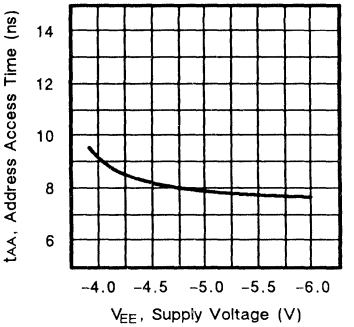


Fig. 11 – Write Pulse Width vs Ambient Temperature

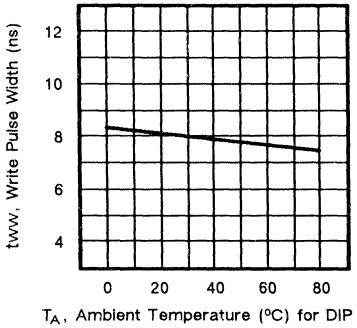
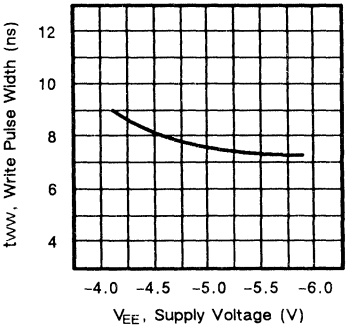


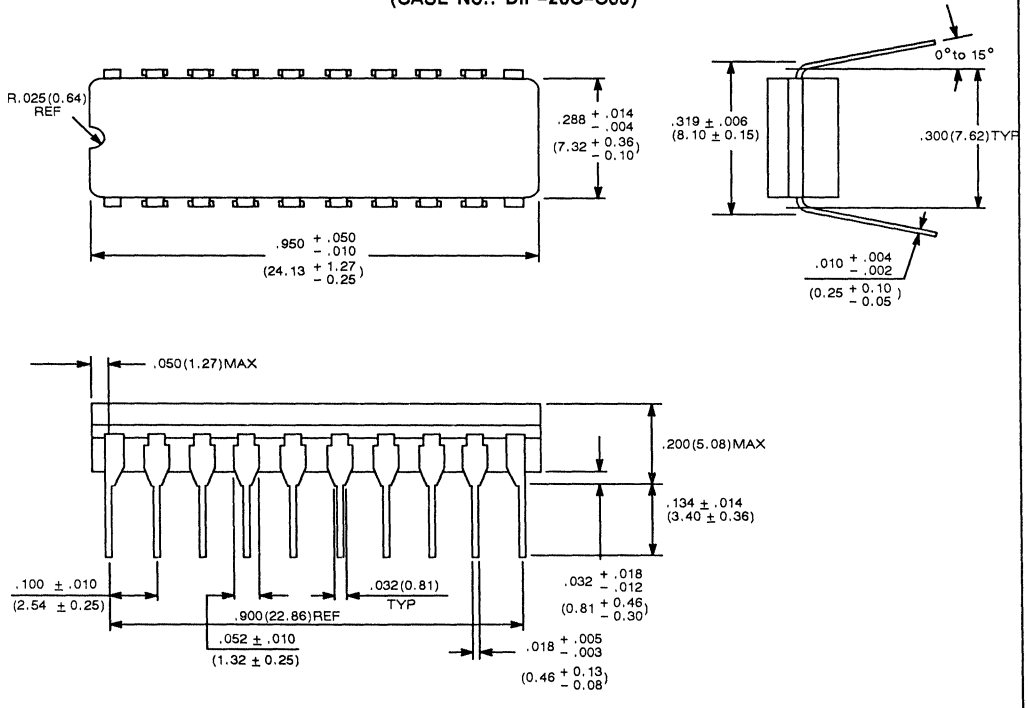
Fig. 12 – Write Pulse Width vs Supply Voltage



1

PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

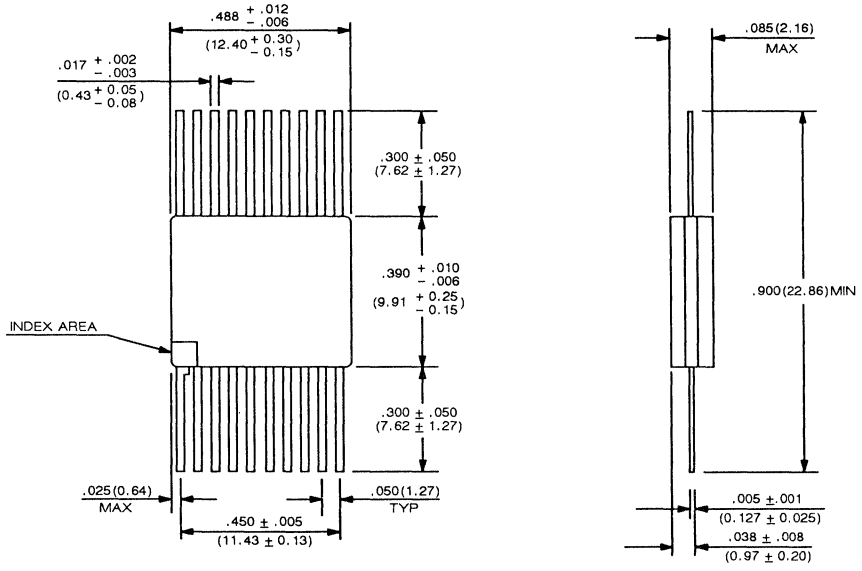


Dimension in inches (millimeters)

D20006S-4C

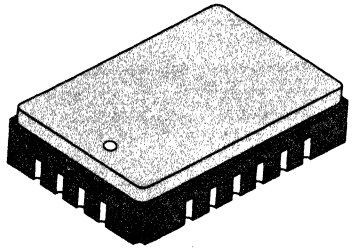
PACKAGE DIMENSIONS (continued)

20-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-20C-C01)



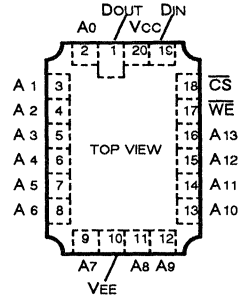
Dimensions in
inches (millimeters)

F20004S-2C

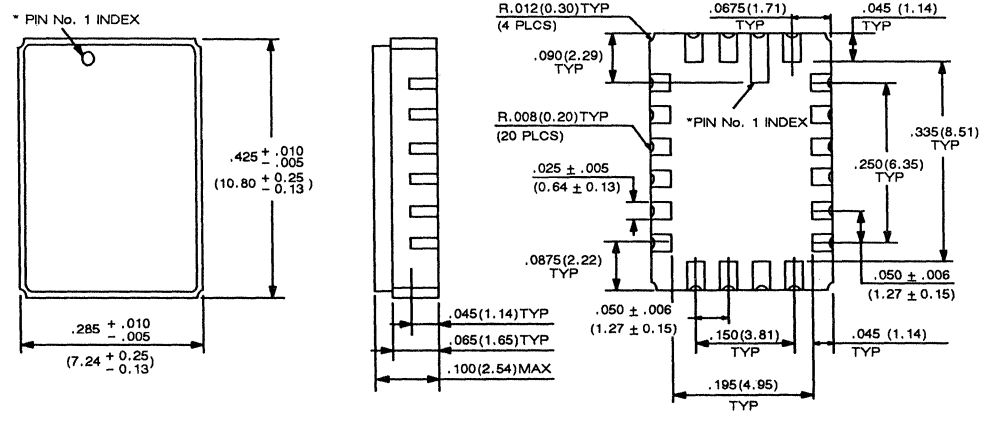


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10480-15
MBM 10480-25

September 1984
Edition 3.0

1

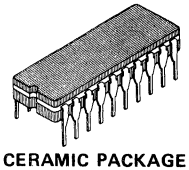
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10480 is fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

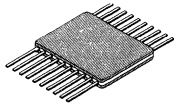
The MBM 10480 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 10480 is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage compensation for improved noise margin.
- Fully compatible with industry-standard 10K-series ECL families
- Address access time : 15 ns max. (MBM 10480-15)
  : 25 ns max. (MBM 10480-25)
- Chip select access time : 8 ns max. (MBM 10480-15)
  : 10 ns max. (MBM 10480-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.05 mW/bit
- DOPOS and IOP-II
- Pin compatible with the F10480

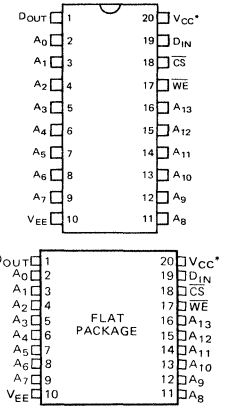


CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01
LCC-20C-F01: See Page 11

PIN ASSIGNMENT



*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

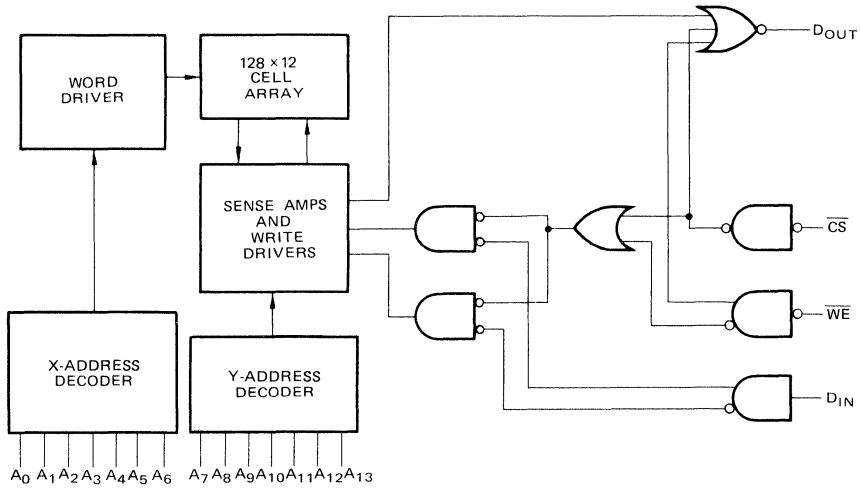
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10480 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10480 is fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data in D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-or connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

1

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10480-15	I_{EE}	-220			mA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10480-25	I_{EE}	-200			mA	0°C to 75°C

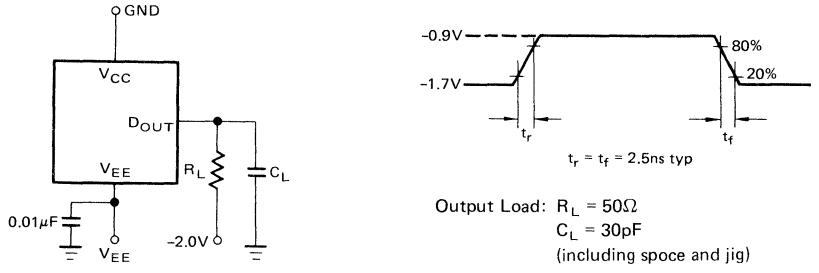
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		5		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=−5.2V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A=0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C=0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS



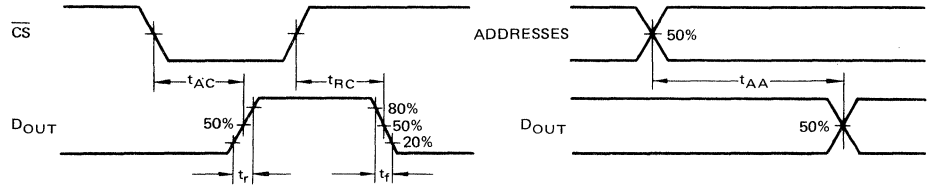
Output Load: R_L = 50Ω
C_L = 30pF
(including spoce and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10480-15			MBM 10480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			8			10	ns
Chip Select Recovery Time	t_{RC}			8			10	ns

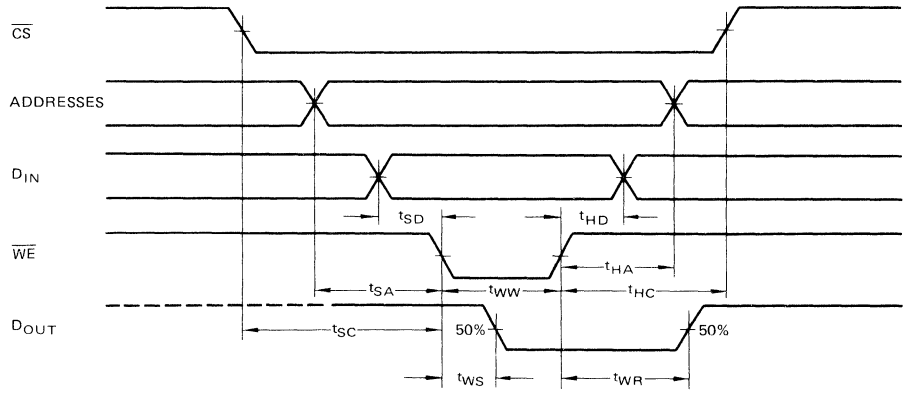
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10480-15			MBM 10480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			25			ns
Write Disable Time	t_{WS}			8			10	ns
Write Recovery Time	t_{WR}			18			20	ns
Address Set Up Time	t_{SA}	2			5			ns
Chip Select Set Up Time	t_{SC}	2			5			ns
Data Set Up Time	t_{SD}	2			5			ns
Address Hold Time	t_{HA}	3			5			ns
Chip Select Hold Time	t_{HC}	3			5			ns
Data Hold Time	t_{HD}	3			5			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		3		ns
Output Fall Time	t_f		3		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

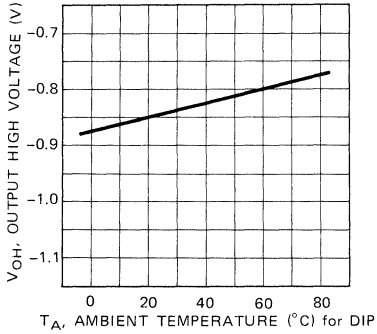


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

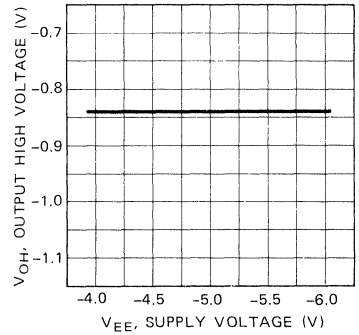


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

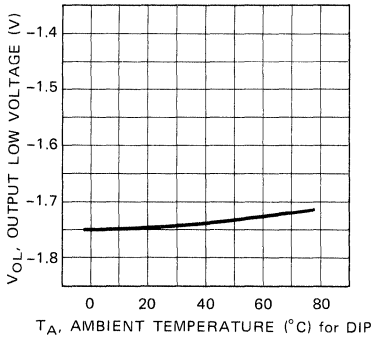


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

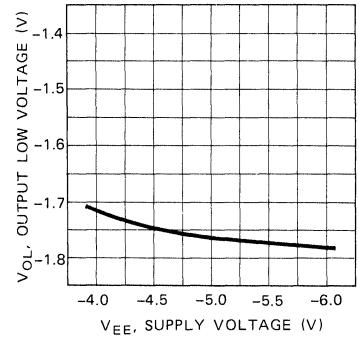


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

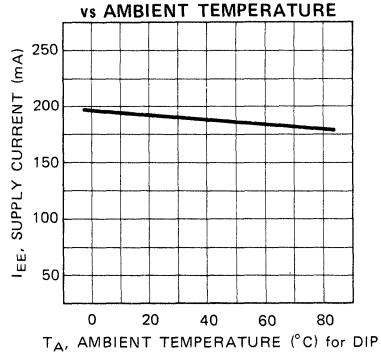


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

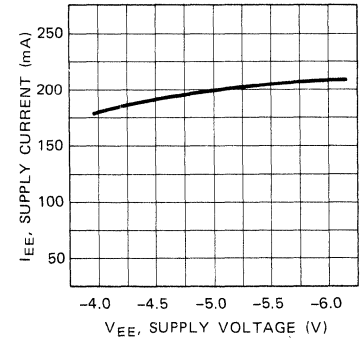


Fig.9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

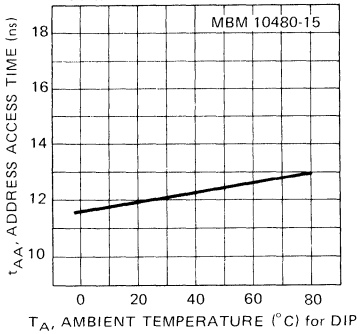


Fig. 10 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

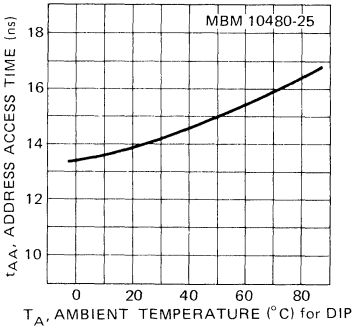


Fig.11 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

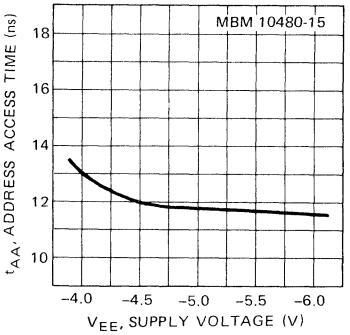


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

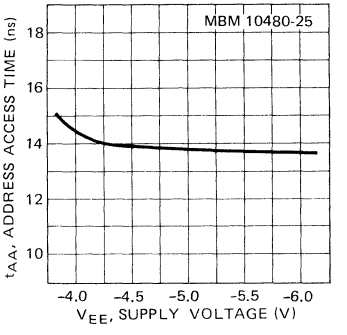


Fig.13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

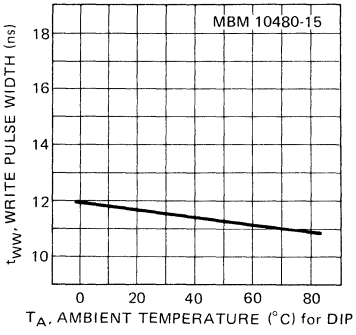
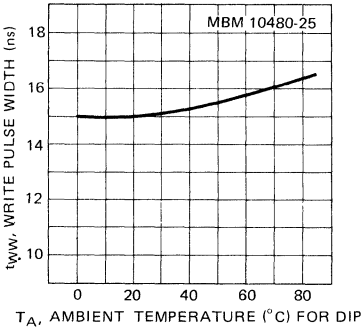


Fig. 14 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



1

Fig.15 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

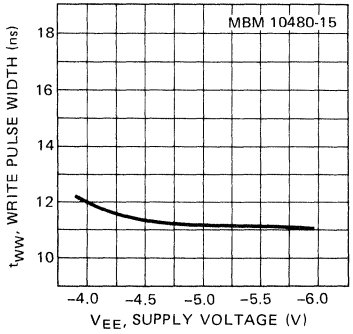
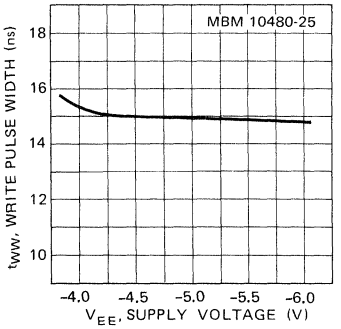
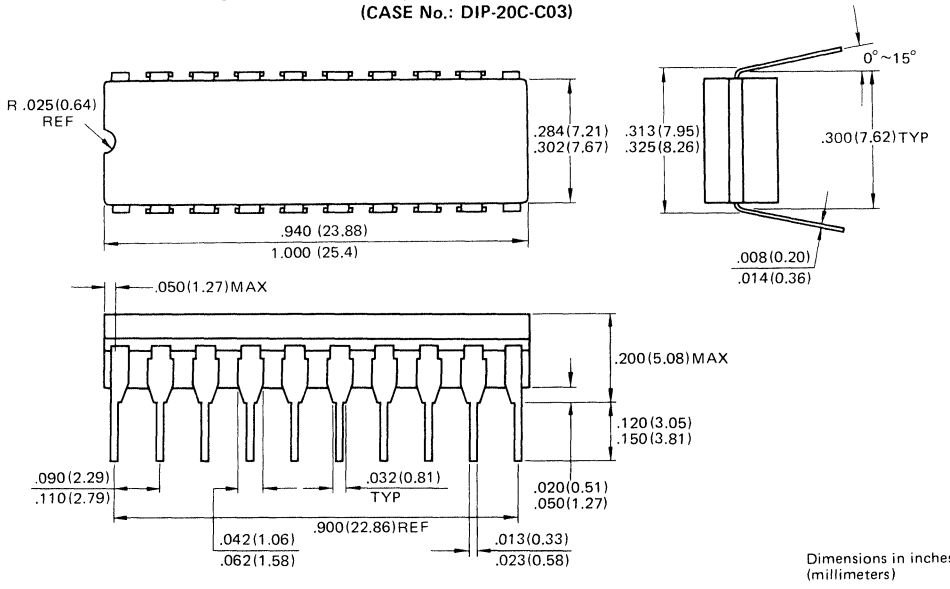


Fig. 16 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

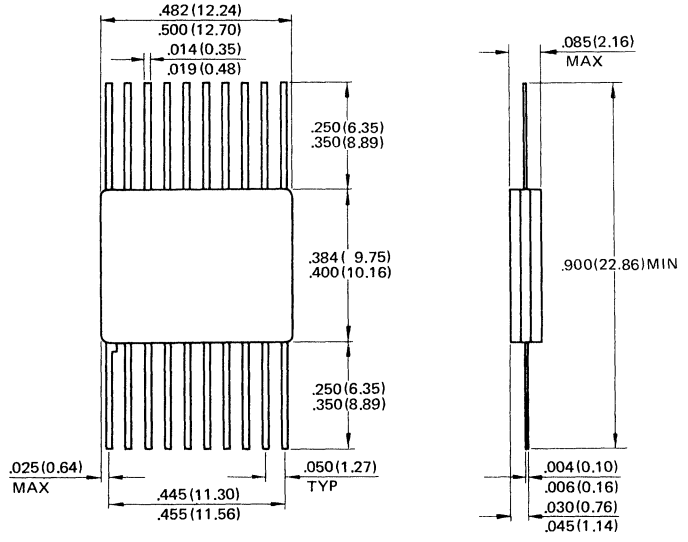
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in inches
(millimeters)

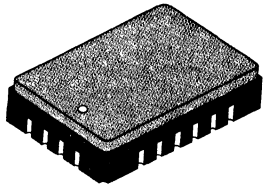
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-20C-C01)



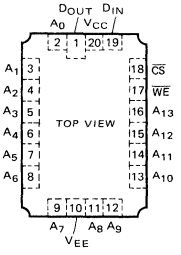
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

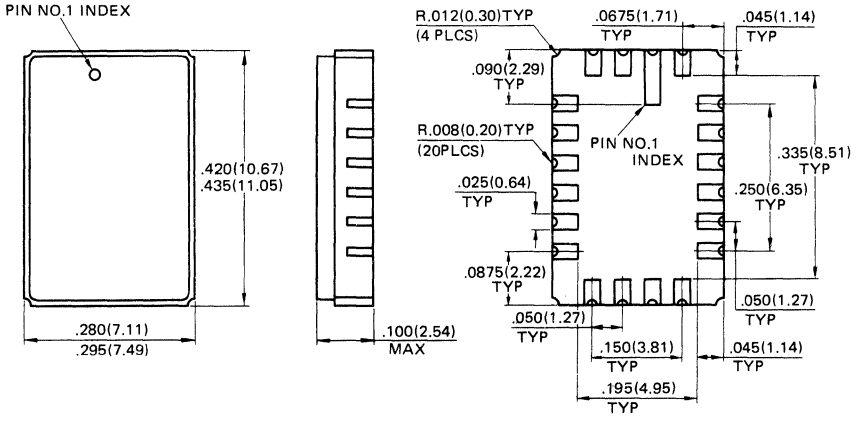


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in
inches (millimeters)

1

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100480-15
MBM 100480-25

September 1984
Edition 3.0

1

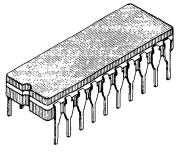
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100480 is fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

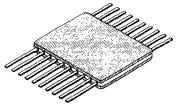
The MBM 100480 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100480 is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K-series ECL families
- Address access time : 15 ns max. (MBM 100480-15)
  : 25 ns max. (MBM 100480-25)
- Chip select access time : 8 ns max. (MBM 100480-15)
  : 10 ns max. (MBM 100480-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.04 mW/bit
- DOPOS and IOP-II
- Pin compatible with the F100480



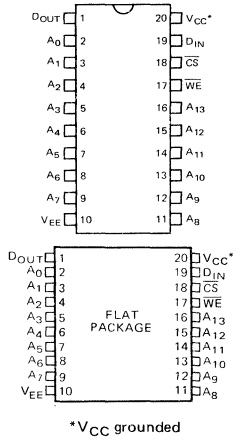
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01 : See Page 11

PIN ASSIGNMENT



*V_{CC} grounded

LCC PAD CONFIGURATION : See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

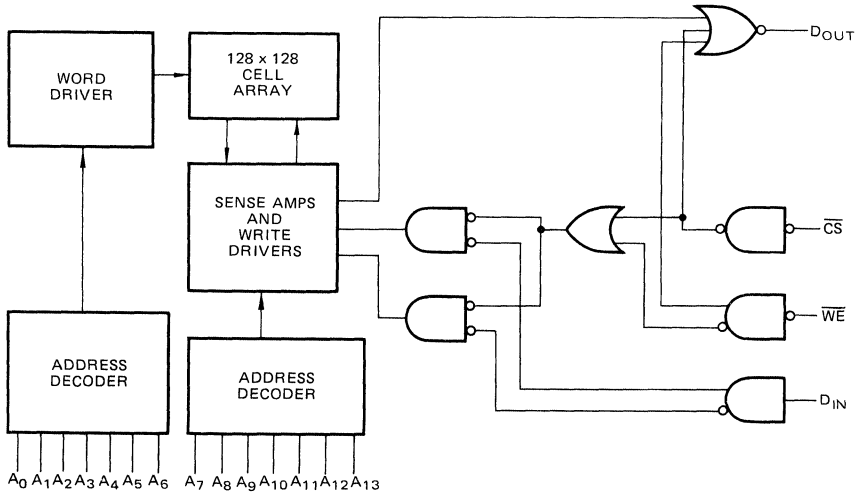
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature under Bias	T_A for DIP	−55 to +125	°C
	Tc for Flat Package and LCC	−55 to +125	
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100480 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100480 is fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

1

DC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=-4.5V, Output Load = 50Ω and 30pF to -2.0V, T_A=0°C to 85°C for DIP, Airflow ≧ 2.5m/s, T_C=0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)		V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	MBM 100480-15	I_{EE}	-220			mA
	MBM 100480-25		-200			

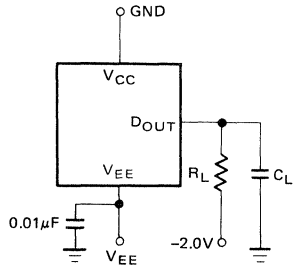
CAPACITANCE

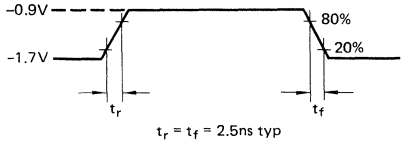
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		5		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=−4.5V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A=0°C to 85°C for DIP, Airflow ≧ 2.5m/s, T_C=0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

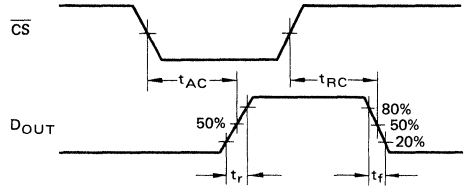
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

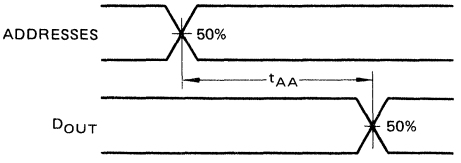
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100480-15			MBM 100480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			8			10	ns
Chip Select Recovery Time	t_{RC}			8			10	ns

READ CYCLE TIMING DIAGRAMS



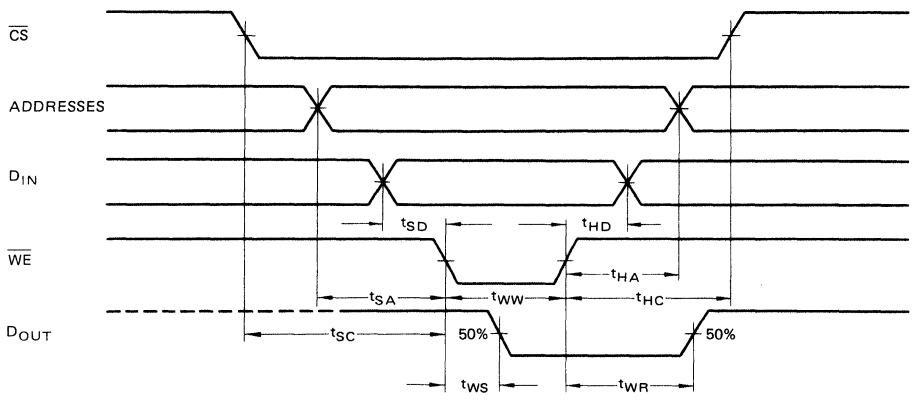


1

WRITE CYCLE

Parameter	Symbol	MBM 100480-15			MBM 100480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			25			ns
Write Disable Time	t_{WS}			8			10	ns
Write Recovery Time	t_{WR}			18			20	ns
Address Set Up Time	t_{SA}	2			5			ns
Chip Select Set Up Time	t_{SC}	2			5			ns
Data Set Up Time	t_{SD}	2			5			ns
Address Hold Time	t_{HA}	3			5			ns
Chip Select Hold Time	t_{HC}	3			5			ns
Data Hold Time	t_{HD}	3			5			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		3		ns
Output Fall Time	t_f		3		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

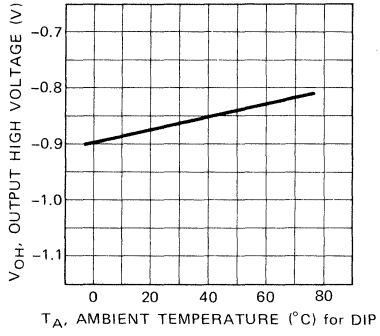


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

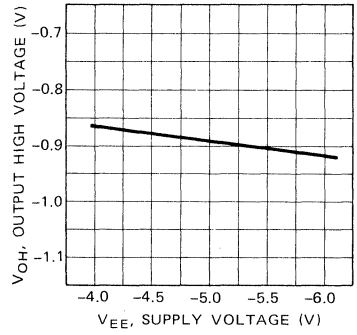


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

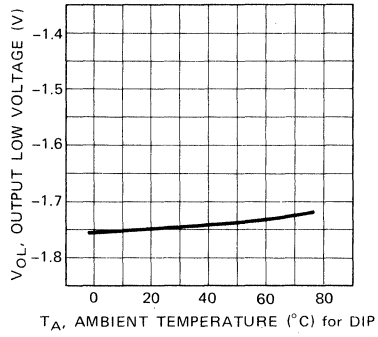


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

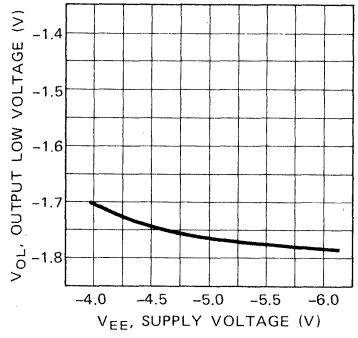


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

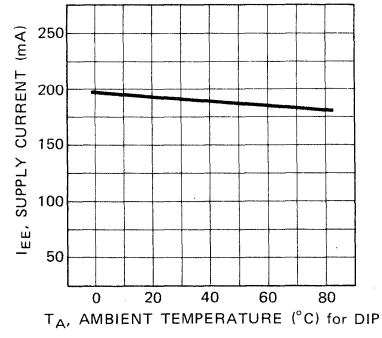


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

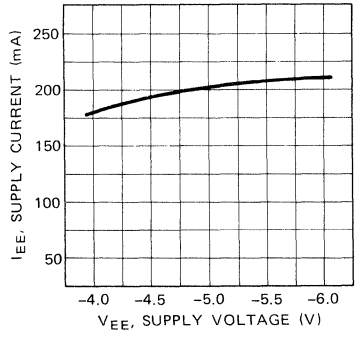


Fig.9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

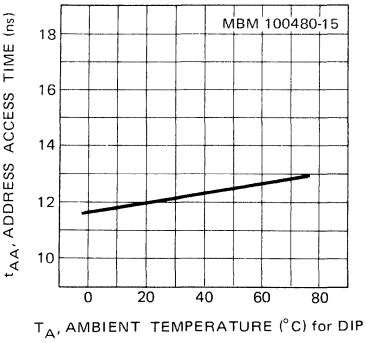


Fig.10 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

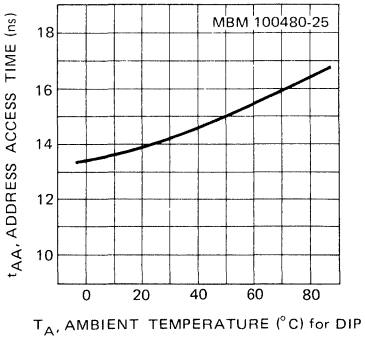


Fig.11 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

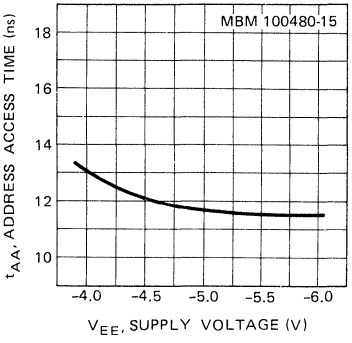


Fig.12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

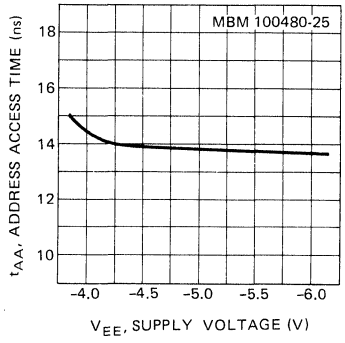


Fig.13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

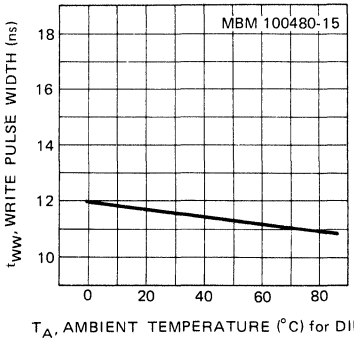


Fig.14 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

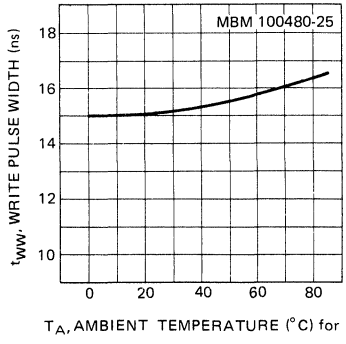


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Fig.15 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

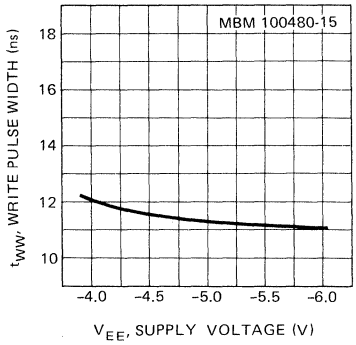
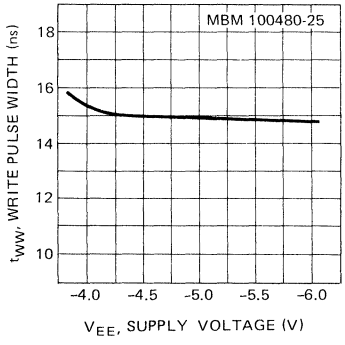


Fig.16 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



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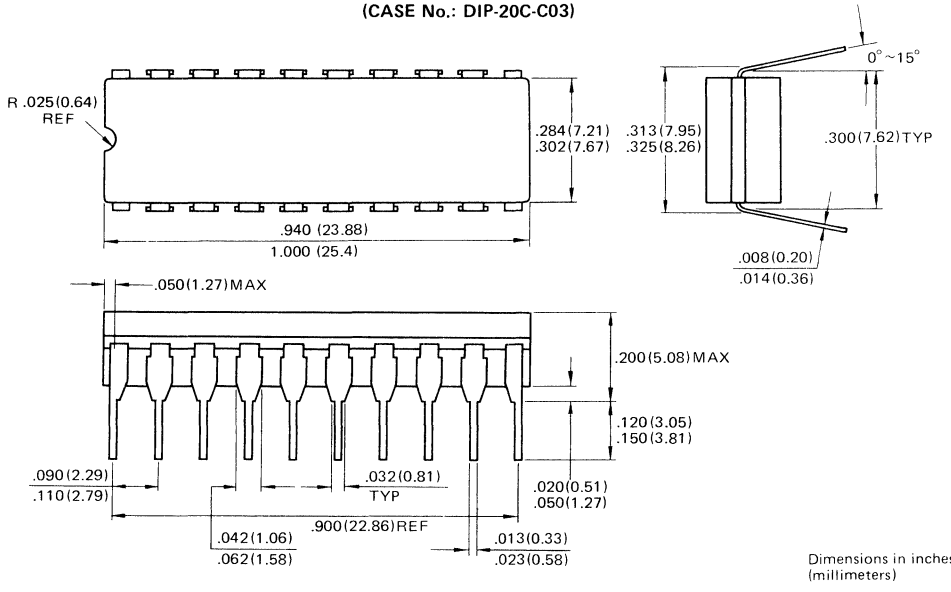
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

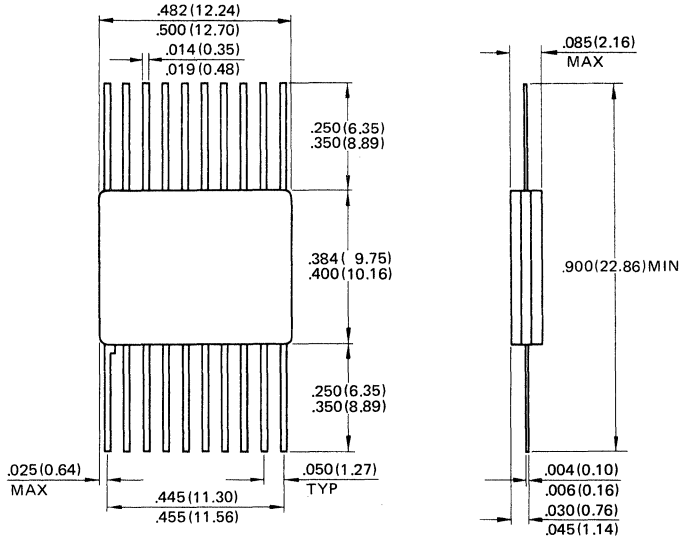


Dimensions in inches
(millimeters)

1

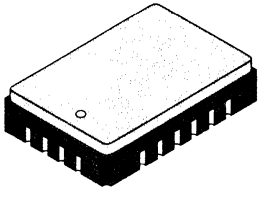
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-20C-C01)



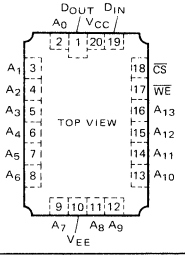
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

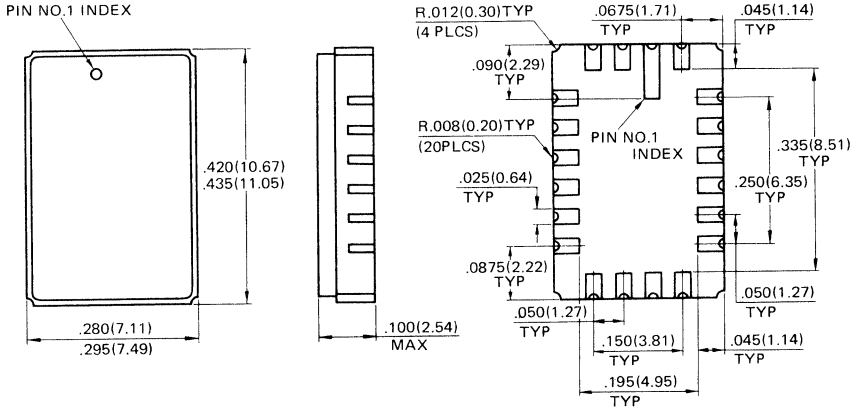


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in
inches (millimeters)

October 1989
Edition 1.0

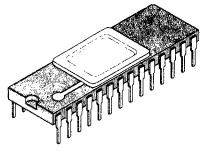
FUJITSU

DATA SHEET

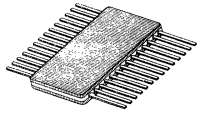
MBM10A484-5

16384–BIT BIPOLAR ECL RANDOM ACCESS MEMORY

PRELIMINARY



CERAMIC PACKAGE
DIP–28C–A06



CERAMIC PACKAGE
FPT–28C–C03

DESCRIPTION

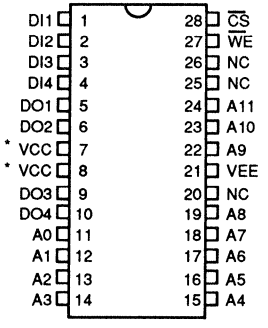
The Fujitsu MBM10A484 is fully decoded 16384–bit ECL read/write random access memory designed for high–speed scratch pad, control and buffer storage applications. The device is organized as 4096 words by 4 bits, and it features on–chip voltage compensation for improved noise margin.

The MBM10A484 offers extremely small cell size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as ESPER (Emitter–base Self aligned structure with Polysilicon Electrodes and Resistors.) processing.

Operation for the MBM10A484 is specified over a case temperature range of from0°C to 55°C (Tc). It also features 28–pin DIP or Flat Package, and is fully compatible with Industry standard 10K–ECL families.

- 4096 words by 4 bits organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10K series ECL families
- Address access time : 5ns
- Chip select access time 3ns
- Power dissipation : 1820mW max
- Open emitter output for ease of memory expansion
- DOPOS and ESPER processing

PIN ASSIGNMENT (TOP VIEW)



* V cc grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

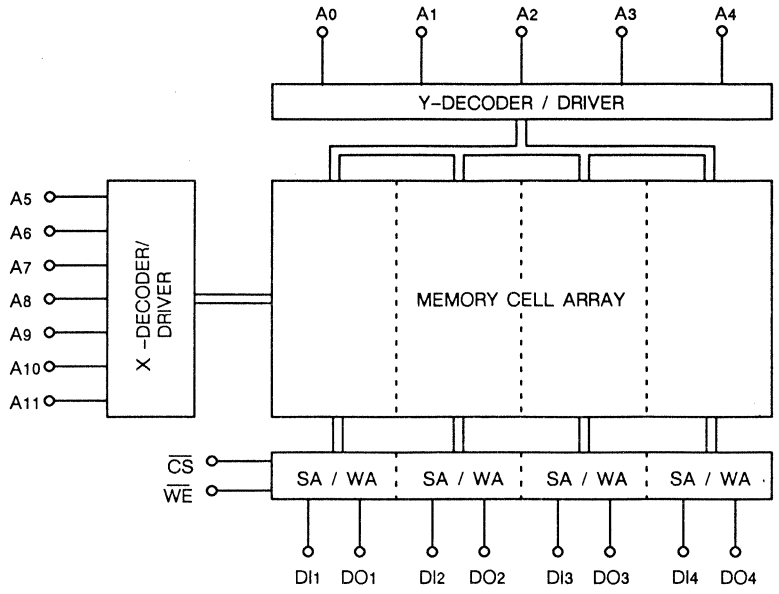
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –6.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

1

Fig.1 – MBM10A484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10A484 is fully decoded read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designated A0 though A11. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS
(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS
(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 55°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TC
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 55°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 55°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 55°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 55°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 55°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 55°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	μA	0°C to 55°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			μA	0°C to 55°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	μA	0°C to 55°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-350			mA	0°C to 55°C

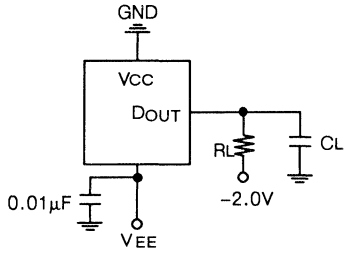
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

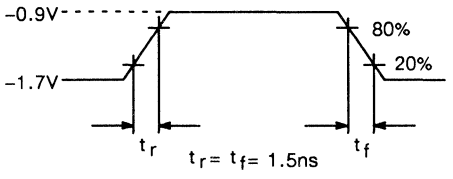
AC CHARACTERISTICS

(VCC = 0V, VEE = −5.2V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, TC = 0°C to 55°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

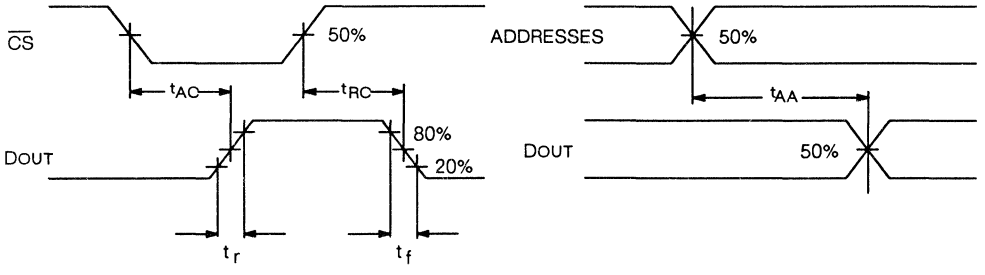


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	1.0		5.0	ns
Chip Select Access Time	t_{AC}	1.0		3.0	ns
Chip Select Recovery Time	t_{RC}	1.0		3.0	ns

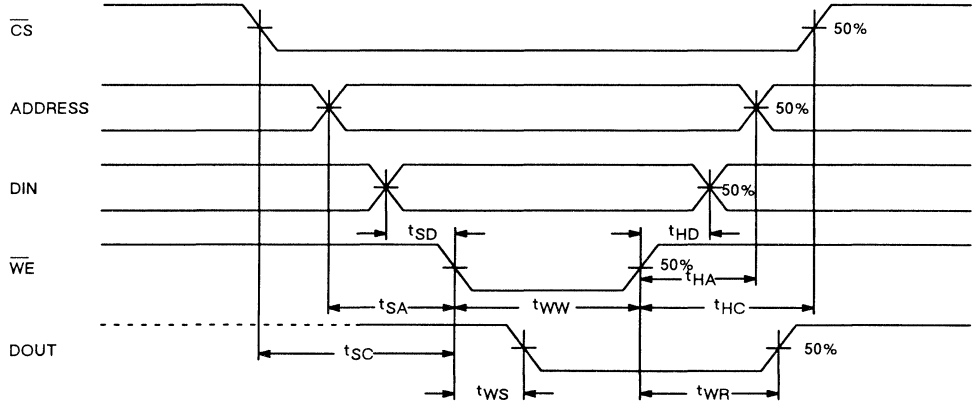
Fig. 3 – READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	7.0			ns
Write Disable Time	t_{WS}			3.0	ns
Write Recovery Time	t_{WR}			6.0	ns
Address Set Up Time	t_{SA}	1.0			ns
Chip Select Set Up Time	t_{SC}	1.0			ns
Data Set Up Time	t_{SD}	1.0			ns
Address Hold Time	t_{HA}	1.0			ns
Chip Select Hold Time	t_{HC}	1.0			ns
Data Hold Time	t_{HD}	1.0			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



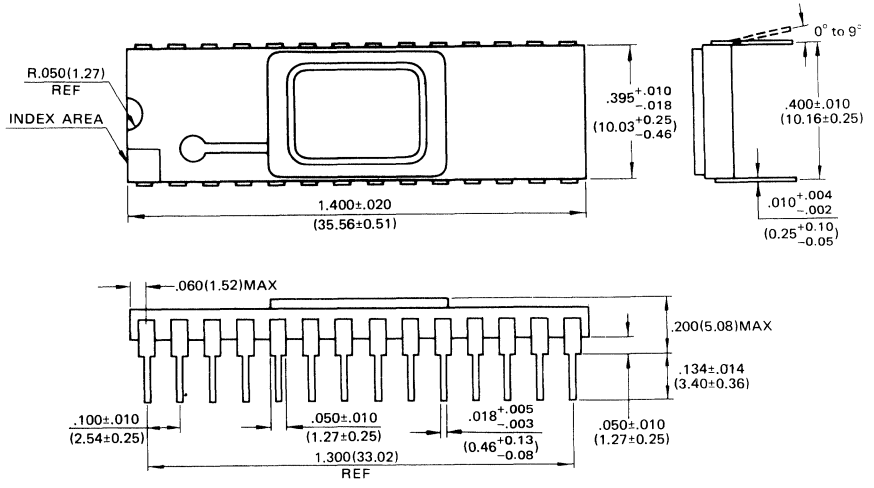
RISING TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

PACKAGE DIMENSIONS

(Suffix : –C)

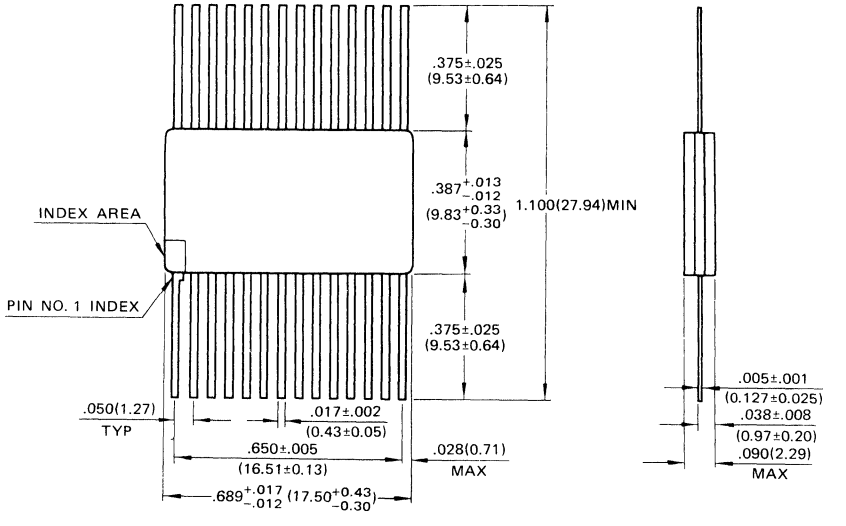
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

(Suffix : -ZF)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

1

October 1989
Edition 1.0

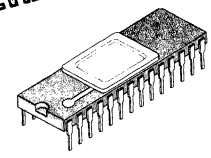
FUJITSU

DATA SHEET

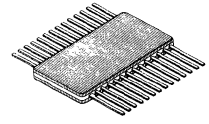
MBM101A484-5

16384–BIT BIPOLAR ECL RANDOM ACCESS MEMORY

PRELIMINARY



CERAMIC PACKAGE
DIP–28C–A06



CERAMIC PACKAGE
FPT–28C–C03

1

DESCRIPTION

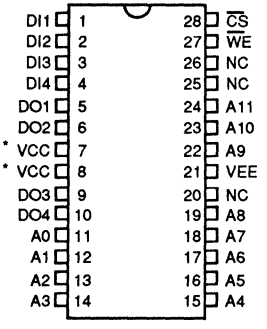
The Fujitsu MBM101A484 is fully decoded 16384–bit ECL read/write random access memory designed for high–speed scratch pad, control and buffer storage applications. The device is organized as 4096 words by 4 bits, and it features on–chip voltage/temperature compensation for improved noise margin.

The MBM101A484 offers extremely small cell size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as ESPER (Emitter–base Self aligned structure with Polysilicon Electrodes and Resistors.) processing.

Operation for the MBM101A484 is specified over a case temperature range of from 0°C to 55°C (Tc). It also features 28–pin DIP or Flat Package, and is fully compatible with Industry standard 100K–ECL families.

- 4096 words by 4 bits organization
- On–chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry standard 100K series ECL families
- Address access time : 5ns
- Chip select access time 3ns
- Power dissipation : 1820mW max
- Open emitter output for ease of memory expansion
- DOPOS and ESPER processing

PIN ASSIGNMENT (TOP VIEW)



* Vcc grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

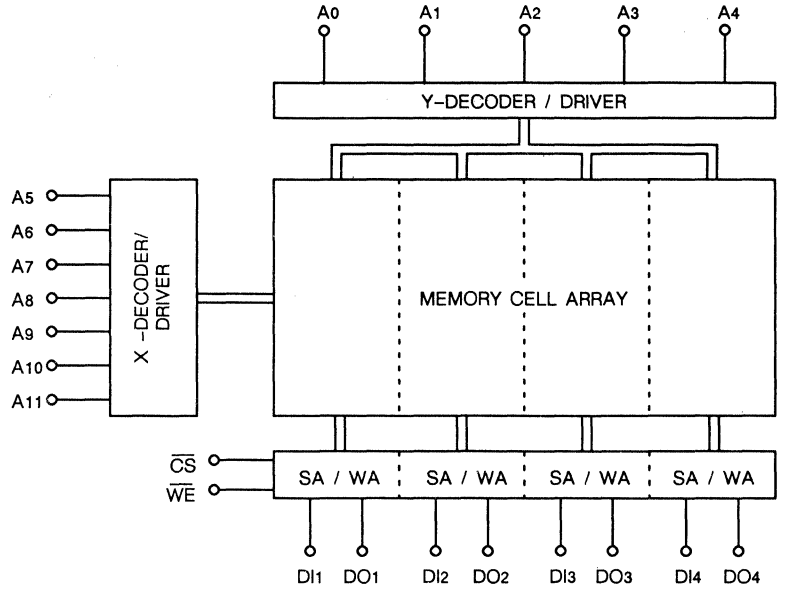
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –6.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

1

Fig.1 - MBM101A484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM101A484 is fully decoded read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designated A0 though A11. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 55°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-350			mA

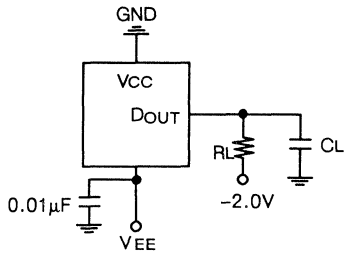
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

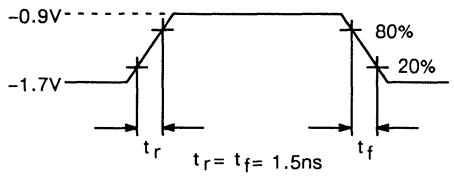
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 55°C, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

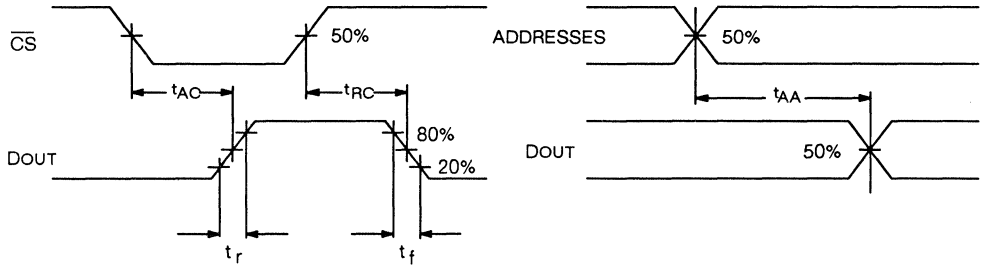


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	1.0		5.0	ns
Chip Select Access Time	t_{AC}	1.0		3.0	ns
Chip Select Recovery Time	t_{RC}	1.0		3.0	ns

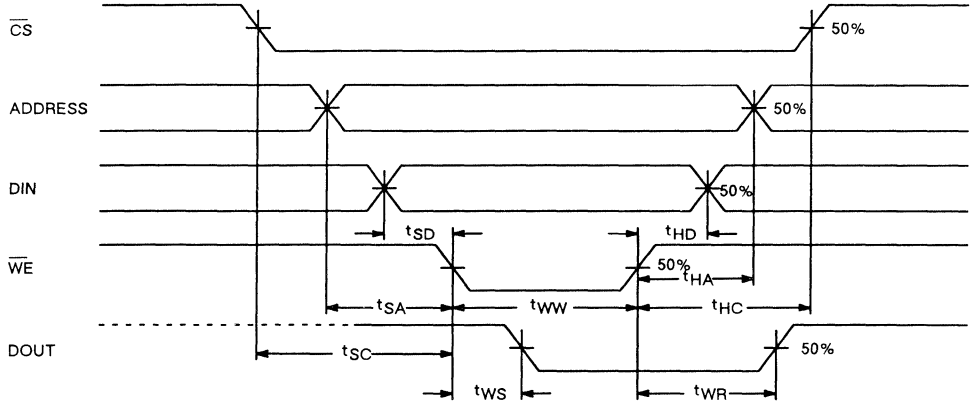
Fig. 3 - READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	7.0			ns
Write Disable Time	t_{WS}			3.0	ns
Write Recovery Time	t_{WR}			6.0	ns
Address Set Up Time	t_{SA}	1.0			ns
Chip Select Set Up Time	t_{SC}	1.0			ns
Data Set Up Time	t_{SD}	1.0			ns
Address Hold Time	t_{HA}	1.0			ns
Chip Select Hold Time	t_{HC}	1.0			ns
Data Hold Time	t_{HD}	1.0			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



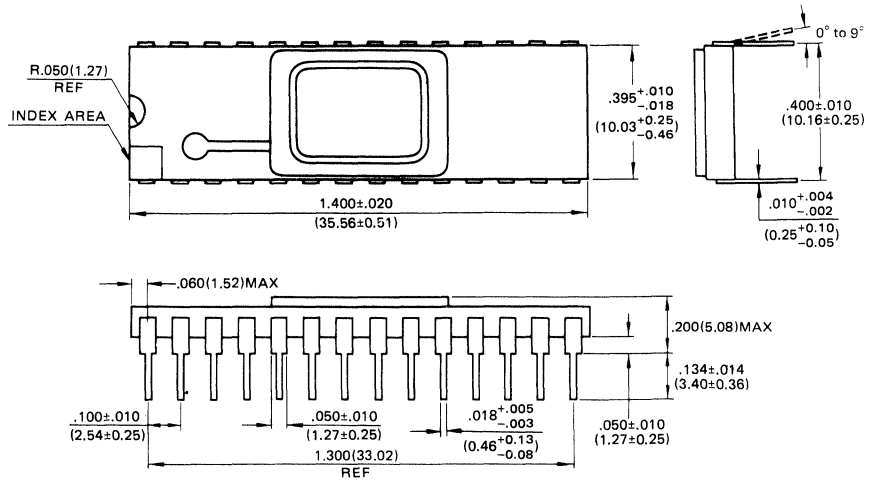
RISING TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

PACKAGE DIMENSIONS

(Suffix : -C)

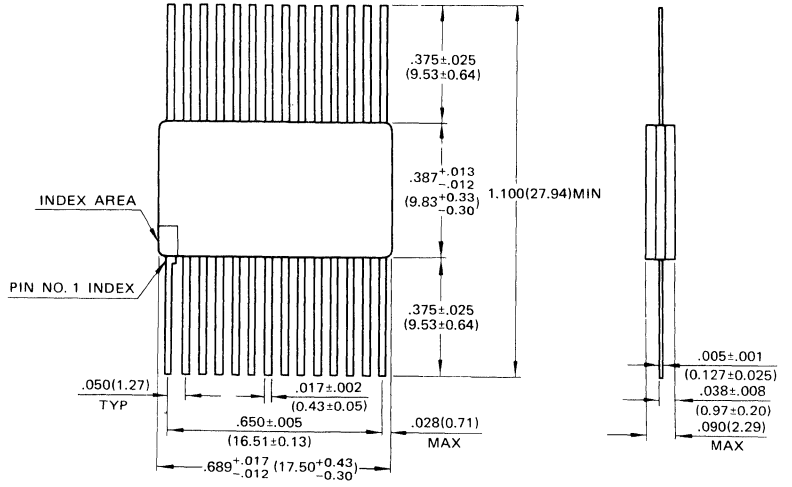
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

(Suffix : -ZF)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

1

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10484A-8

August 1988
Edition 2.0

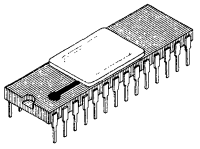
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

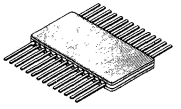
The MBM 10484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484A is specified over a temperature range of from 0°C to 55°C (T_A for DIP T_C for Flat Package and LCC). It also features 28-pin ceramic DIP, Flat package, or LCC and is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 8 ns max.
- Chip select access time: 4 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.10 mW/bit typ.
- DOPOS and IOP-II processing



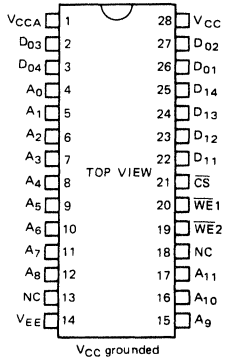
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F02: See Page 10

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

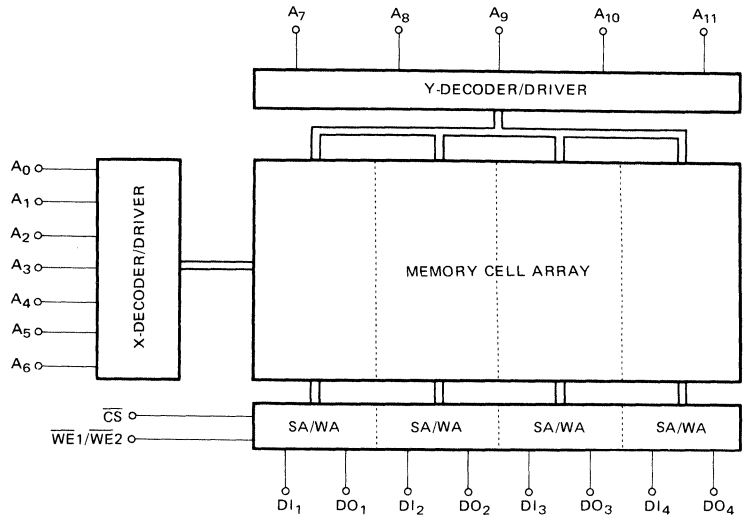
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 10484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM10484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 55°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 55°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 55°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 55°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 55°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 55°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 55°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 55°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 55°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 55°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-330			mA	0°C to 55°C

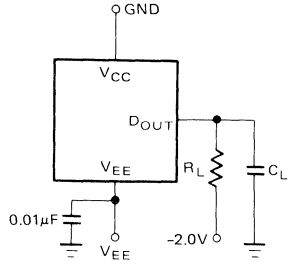
CAPACITANCE

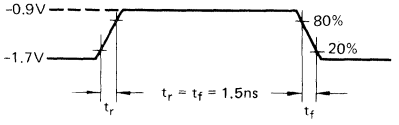
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 55°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





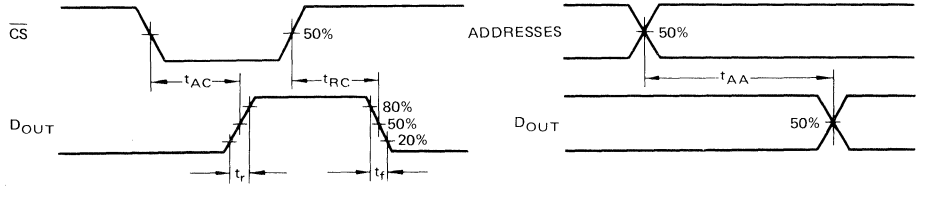
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			8	ns
Chip Select Access Time	t_{AC}			4	ns
Chip Select Recovery Time	t_{RC}			4	ns

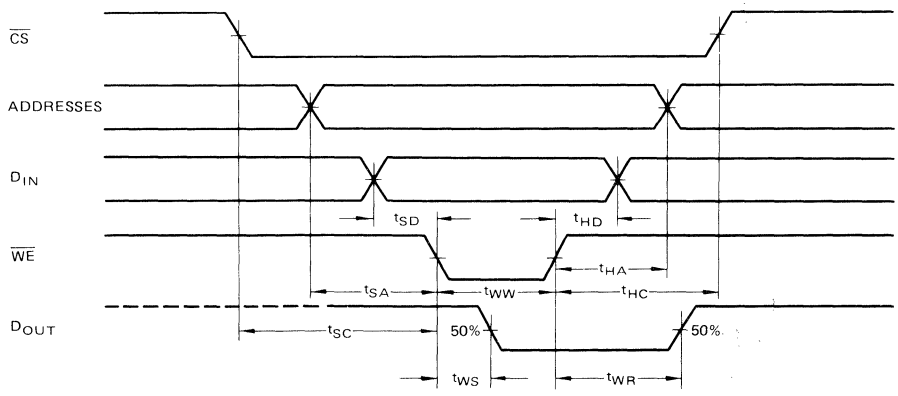
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			4	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

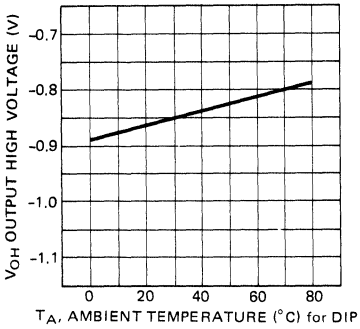


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

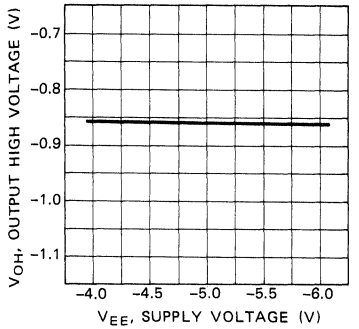


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

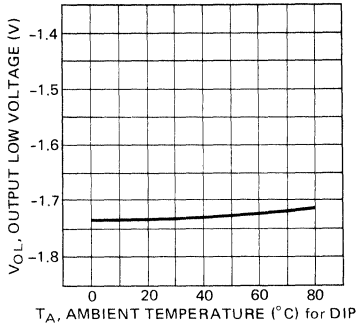


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

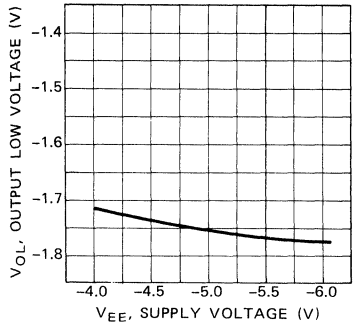


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

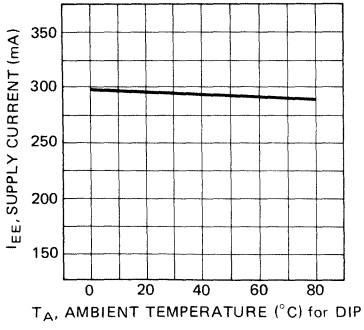


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

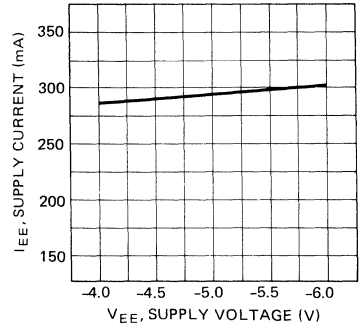


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

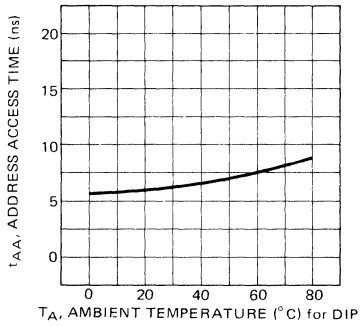


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

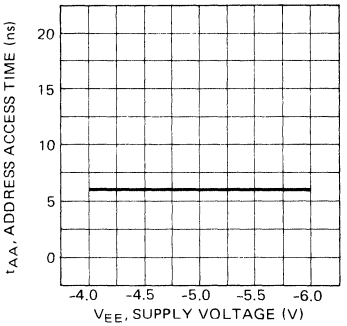


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

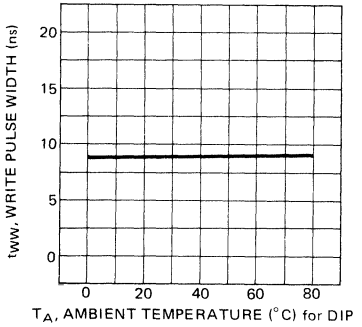
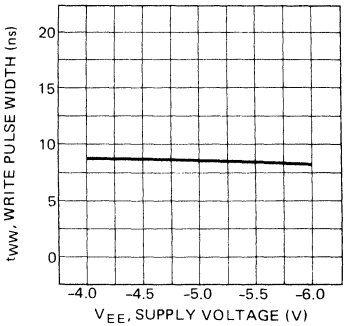


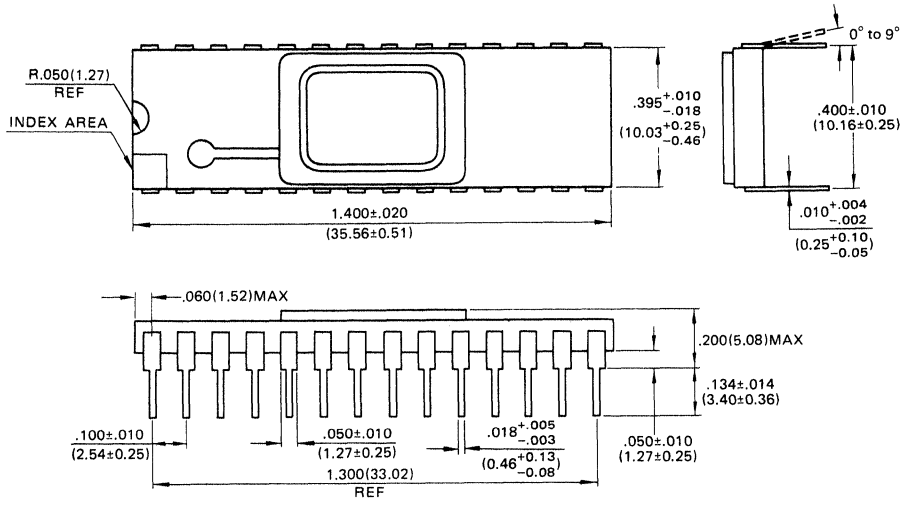
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



1

PACKAGE DIMENSIONS

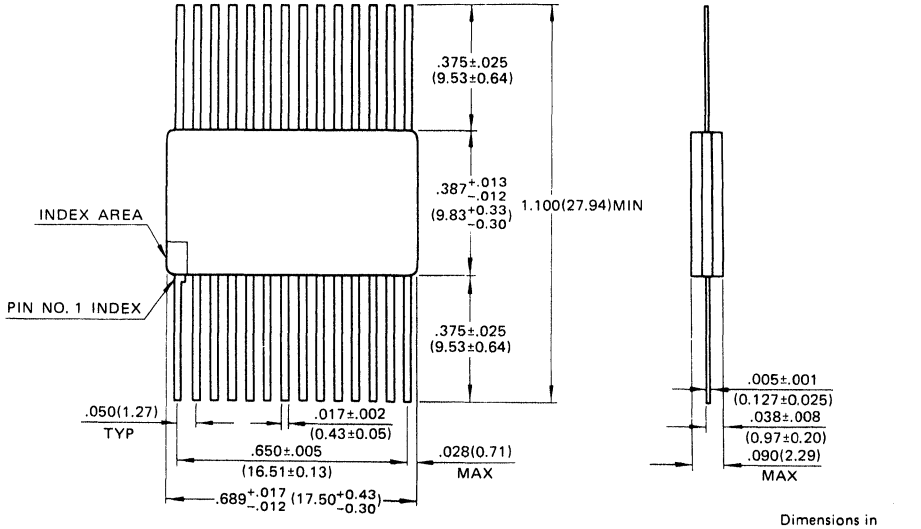
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

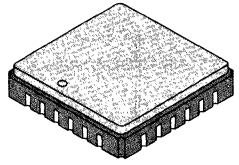
PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



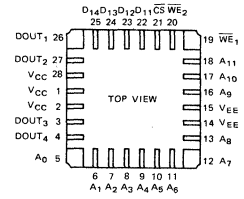
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

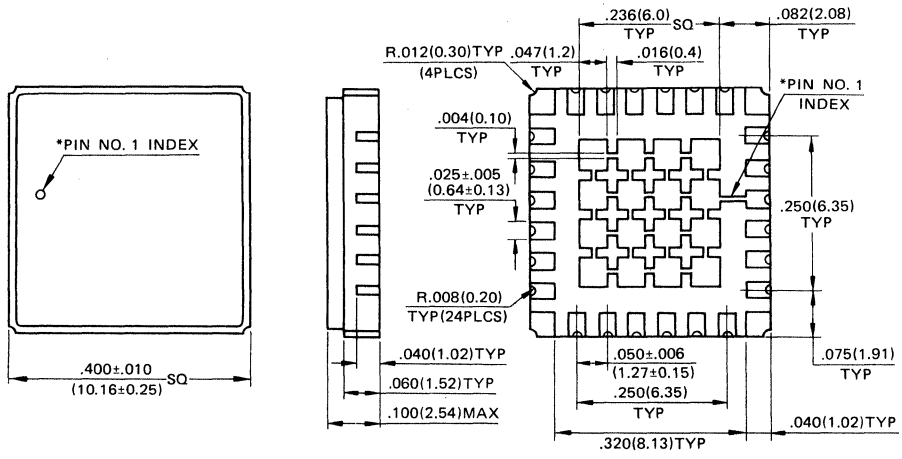


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100484A-8

August 1988
Edition 2.0

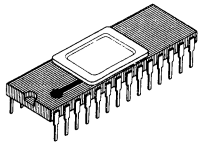
16384-BIT BIPPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

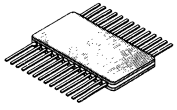
The MBM 100484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100484A is specified over a temperature range of from 0°C to 65°C (T_A for DIP, T_C for Flat Package and LCC). It also features 28-pin DIP or Flat package and LCC, and is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 8 ns max.
- Chip select access time: 4 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.091 mW/bit typ.
- DOPOS and IOP-II processing



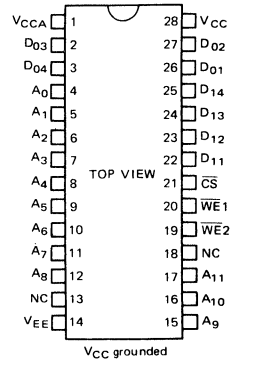
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F02: See Page 10

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

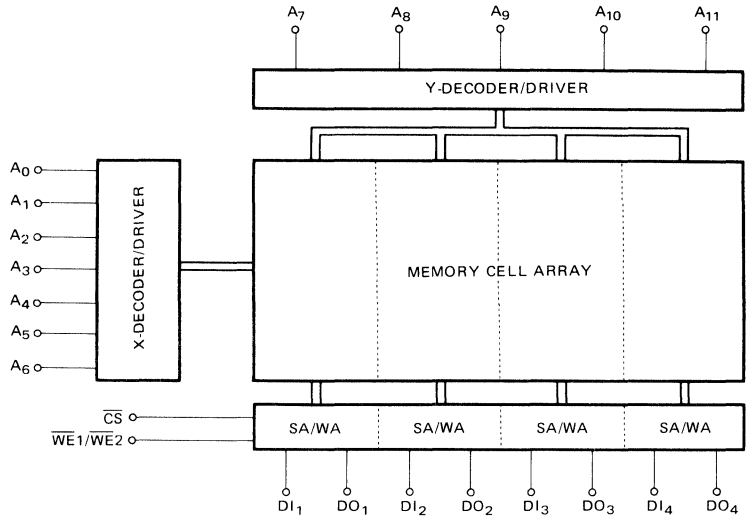
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 100484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM 100484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs. With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambinet Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 65°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 65°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 65°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-330			mA

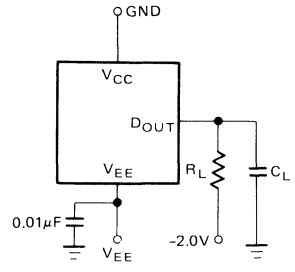
CAPACITANCE

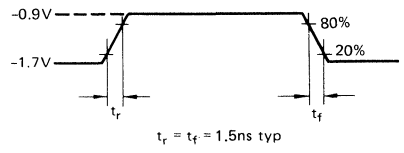
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 65°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 65°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f = 1.5ns$ typ

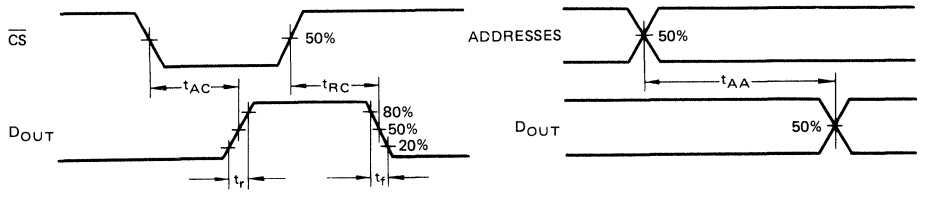
Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			8	ns
Chip Select Access Time	t_{AC}			4	ns
Chip Select Recovery Time	t_{RC}			4	ns

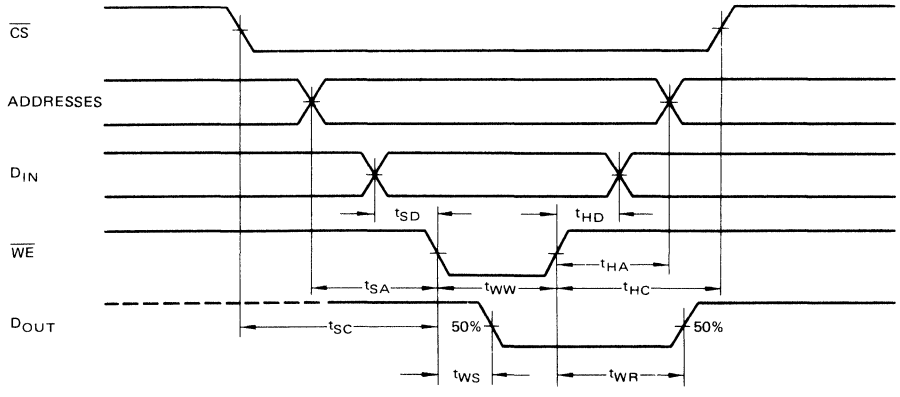
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			4	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

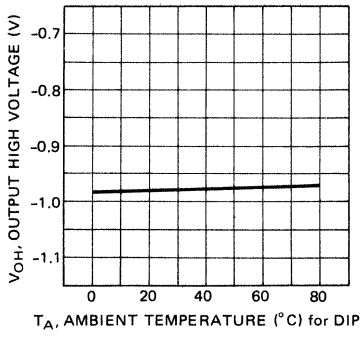


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

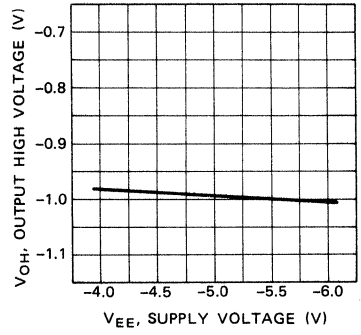


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

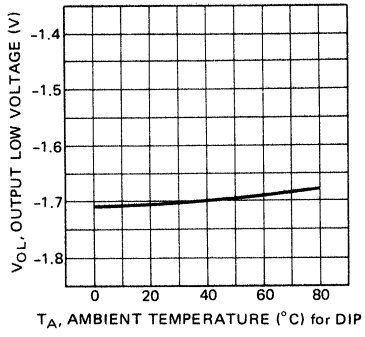


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

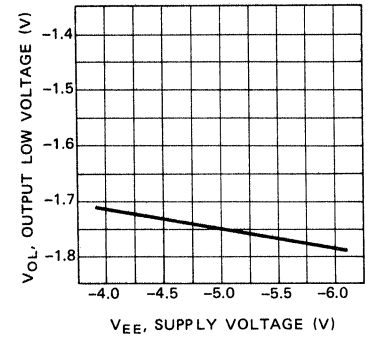


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

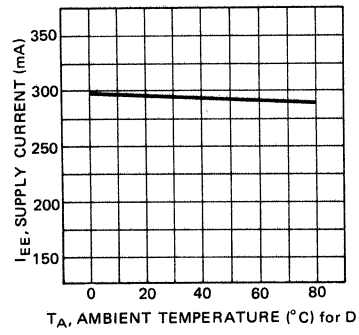


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

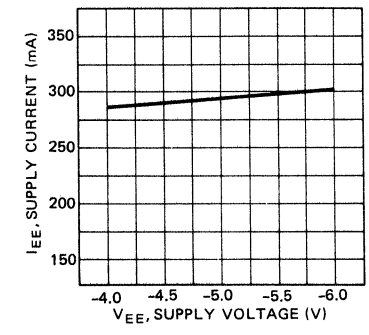


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

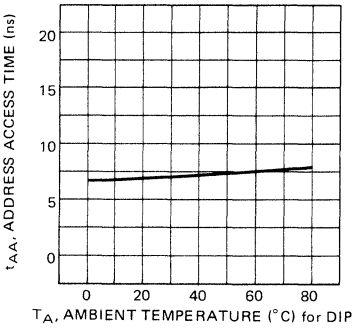


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

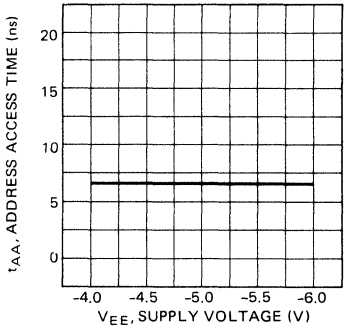


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

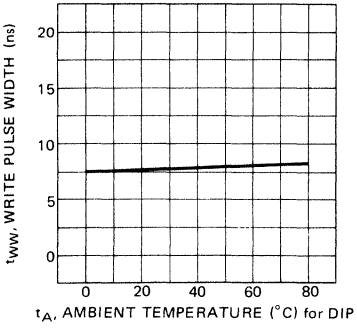
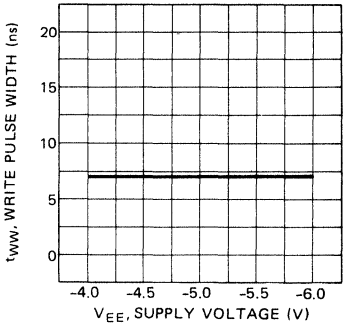


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



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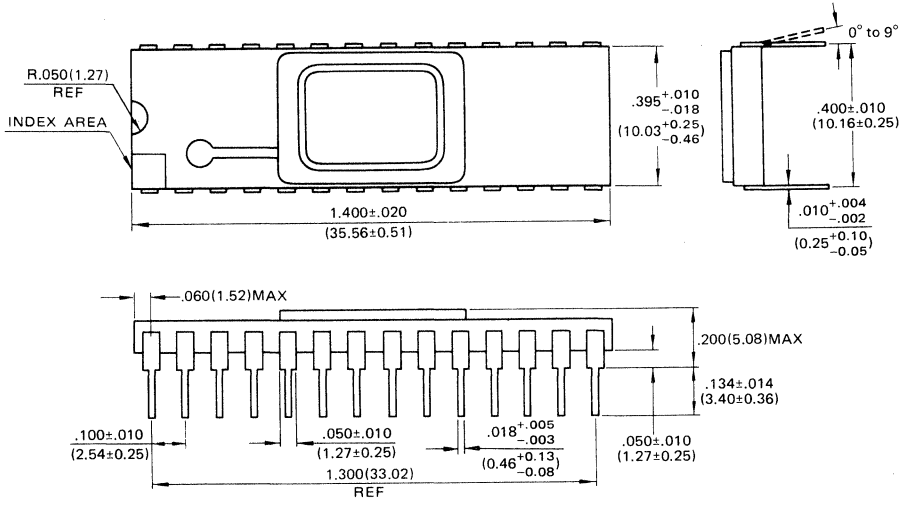
1

PACKAGE DIMENSIONS

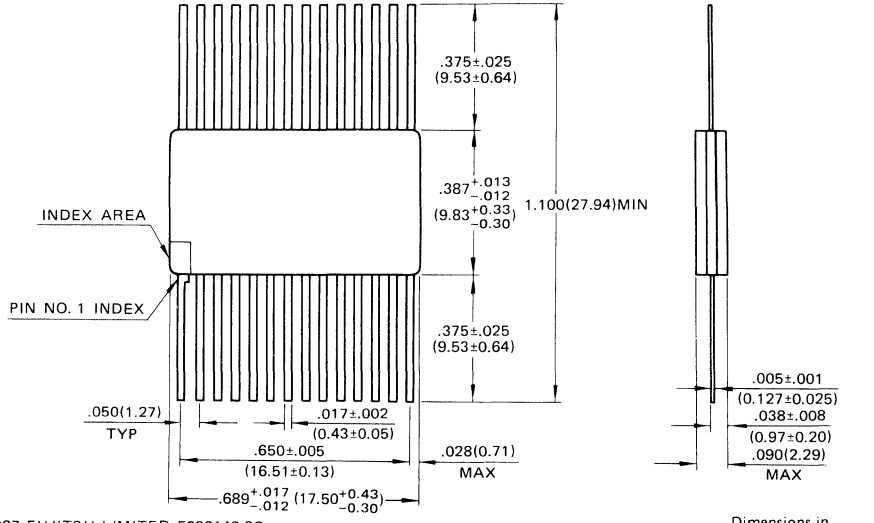
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

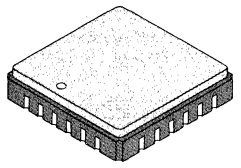
PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



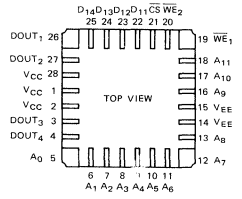
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

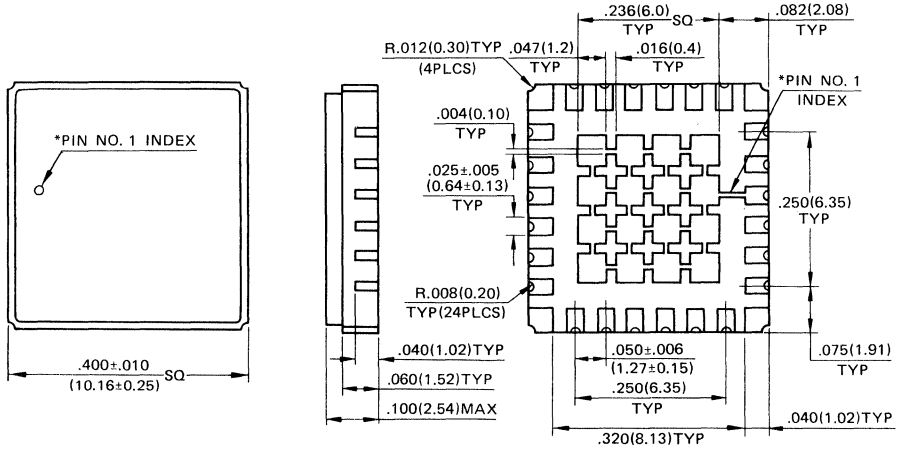


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10484A-10

August 1988
Edition 2.0

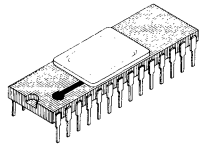
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

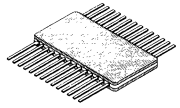
The MBM 10484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high hields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484A is specified over a temperature range of from 0°C to 75°C (T_A for DIP T_C for Flat Package and LCC). It also features 28-pin ceramic DIP, Flat package, or LCC and is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 10 ns max.
- Chip select access time: 5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.07 mW/bit typ.
- DOPOS and IOP-II processing



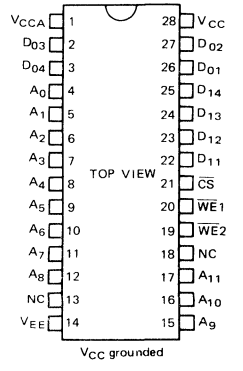
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F01 : See Page 10
LCC-28C-F02 : See Page 11

PIN ASSIGNMENT



See Page 10
LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

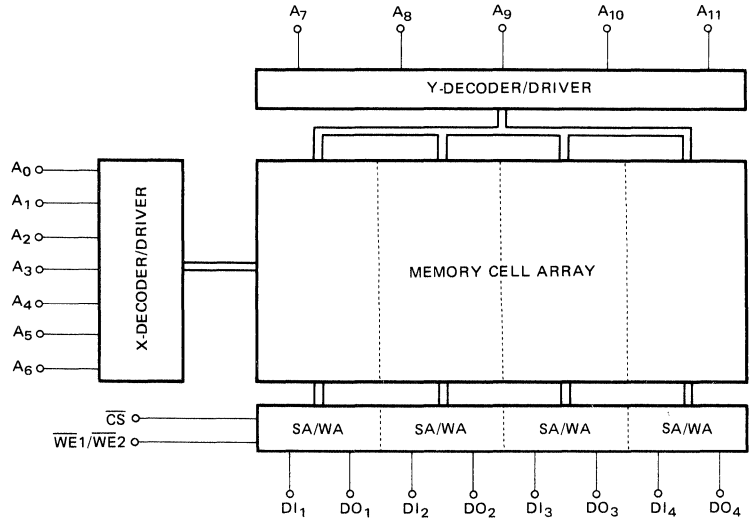
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 10484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}1/\overline{WE}2$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE}1$ and $\overline{WE}2$ are low.
*H = Either $\overline{WE}1$ or $\overline{WE}2$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM10484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}1/\overline{WE}2$) inputs With both $\overline{WE}1/\overline{WE}2$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE}1$ or $\overline{WE}2$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-260			mA	0°C to 75°C

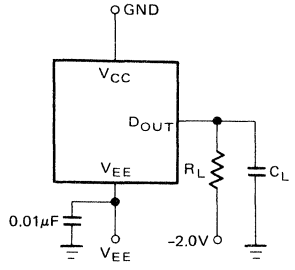
CAPACITANCE

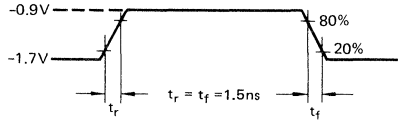
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





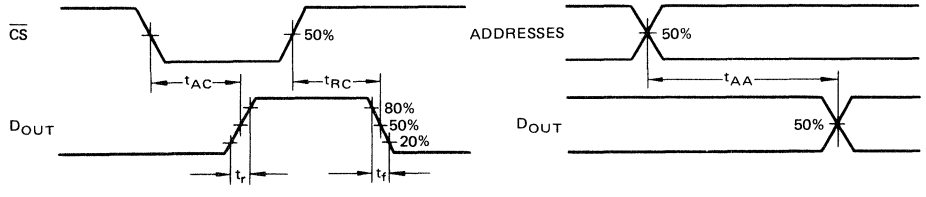
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

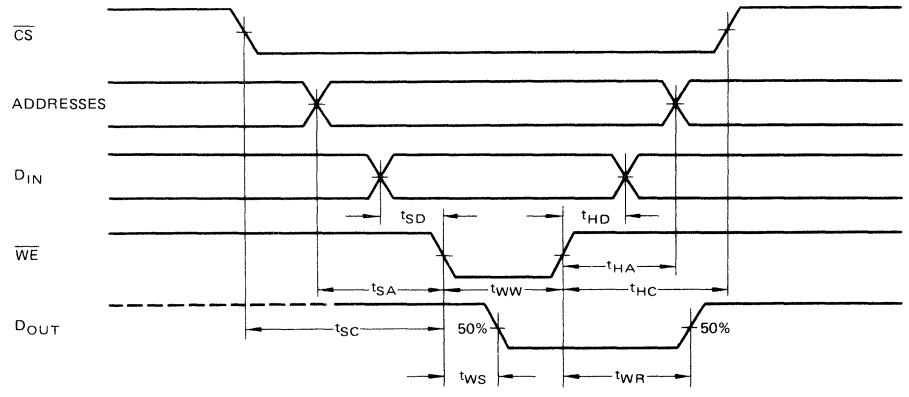
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

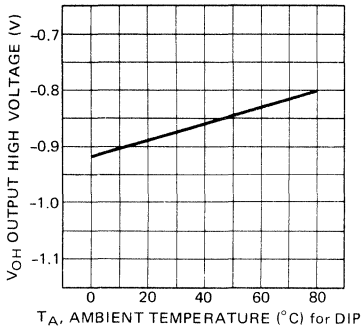


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

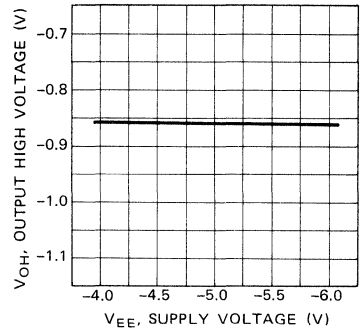


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

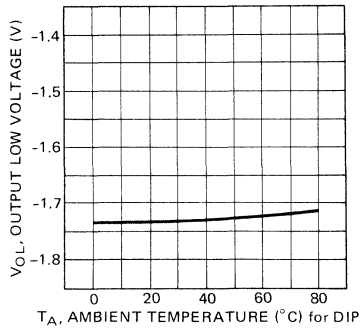


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

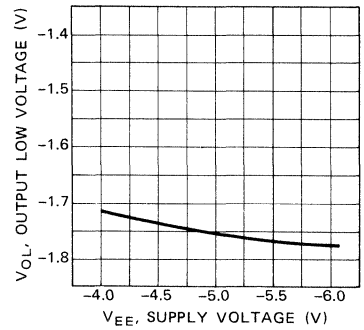


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

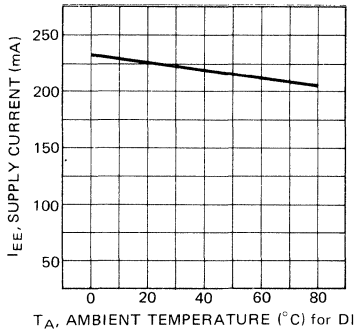


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

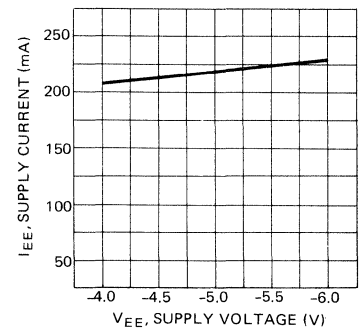


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

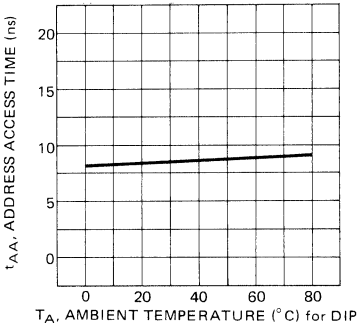


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

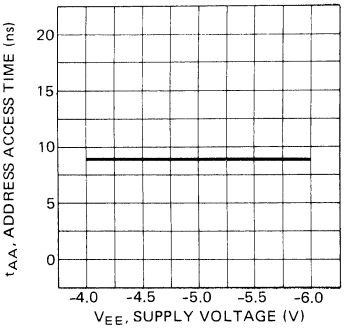


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

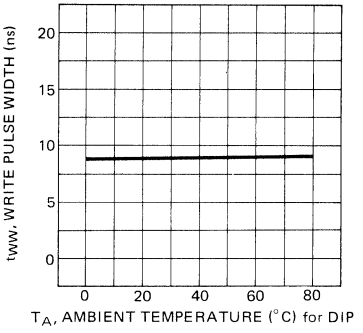
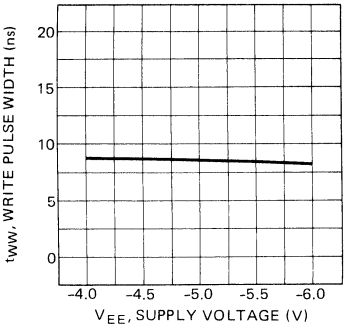
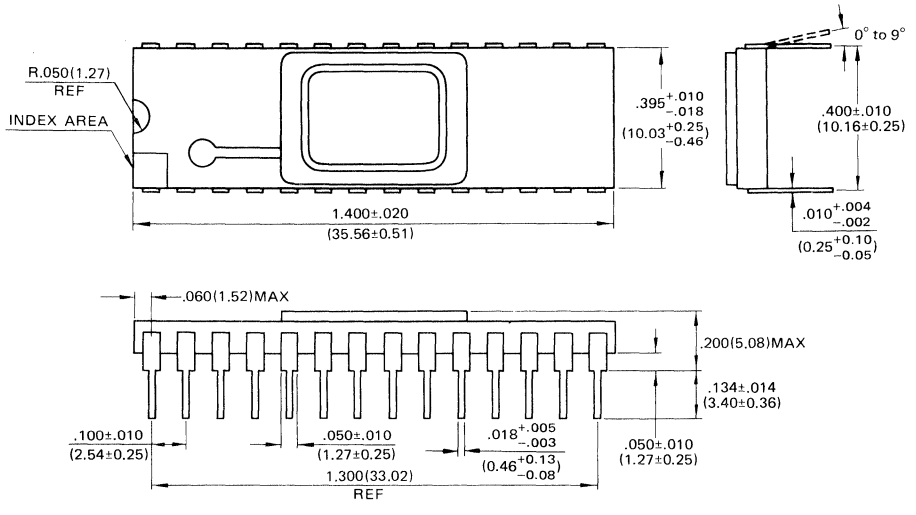


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



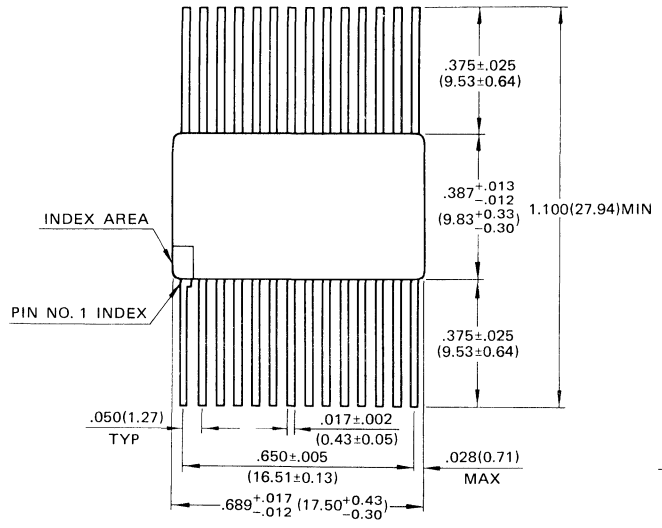
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



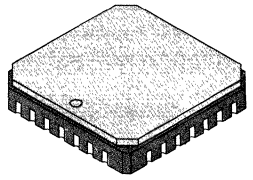
Dimensions in
inches and (millimeters)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



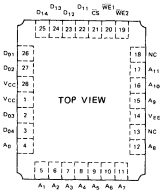
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

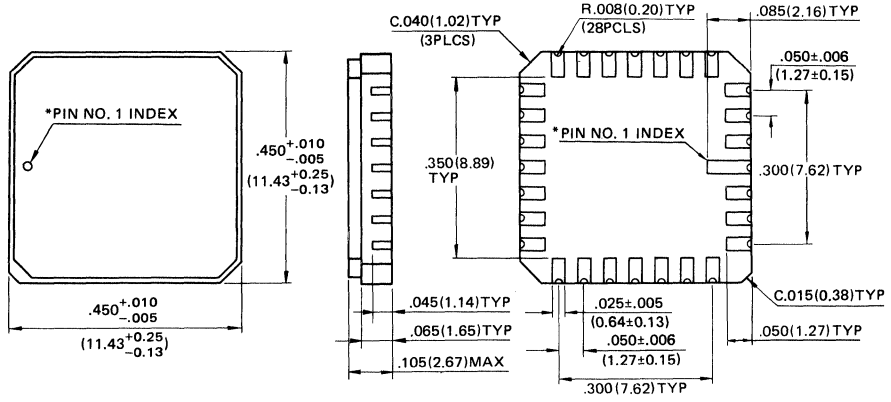


LCC-28C-F01

PAD CONFIGURATION

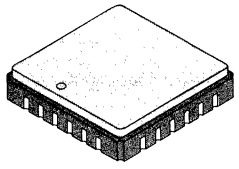


28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F01)



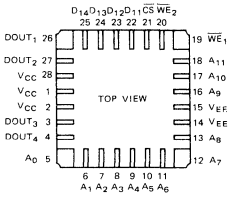
*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in
inches (millimeters)

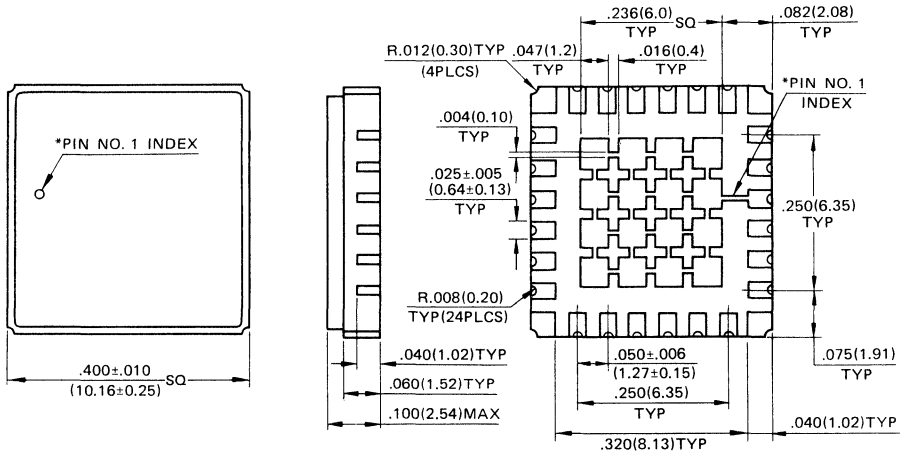


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER (CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

1

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100484A-10

August 1988
Edition 2.0

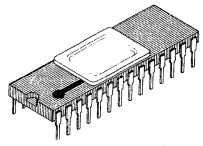
16384-BIT BIPPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

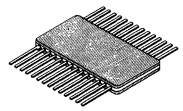
The MBM 100484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100484A is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 28-pin DIP or Flat package and LCC, and is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 10 ns max.
- Chip select access time: 5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.06 mW/bit typ.
- DOPOS and IOP-II processing



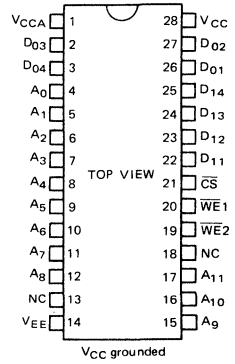
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F01 : See Page 10
LCC-28C-F02 : See Page 11

PIN ASSIGNMENT



See Page 10
LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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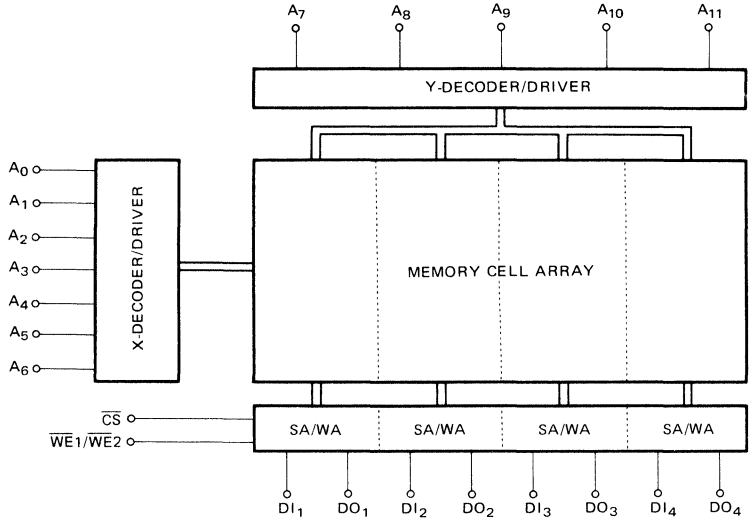
Fig. 1 – MBM 100484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM 100484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs. With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambinet Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_A = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-260			mA

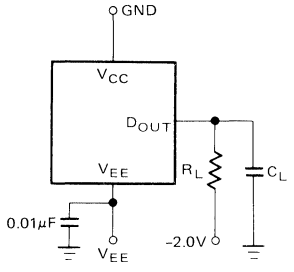
CAPACITANCE

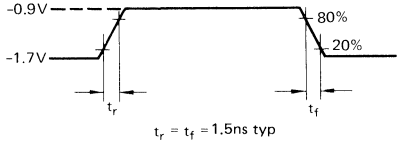
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f = 1.5$ns typ

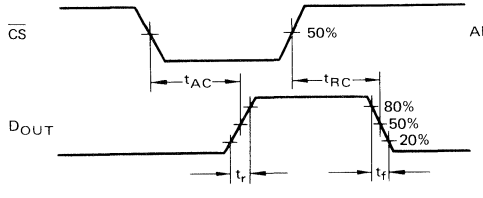
Output Load: $R_L = 50\Omega$
$C_L = 30$pF
(including jig and stray capacitance)

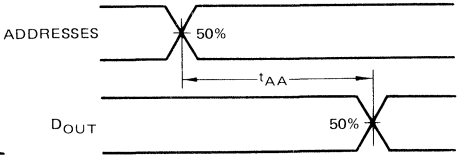
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

READ CYCLE TIMING DIAGRAMS





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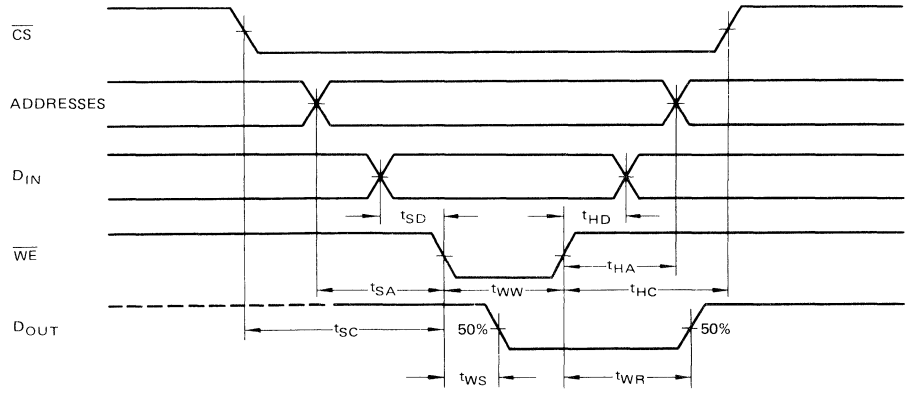
WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

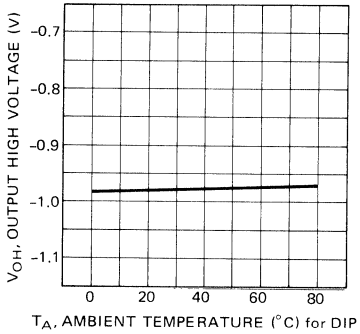


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

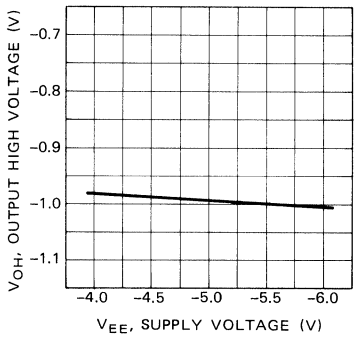


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

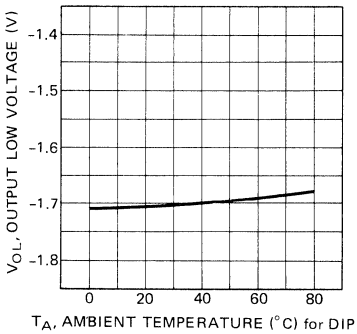


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

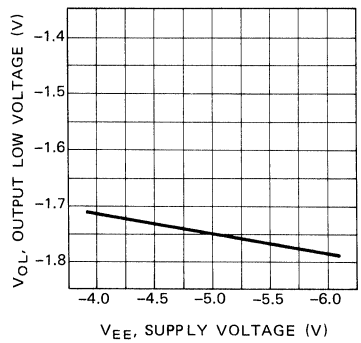


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

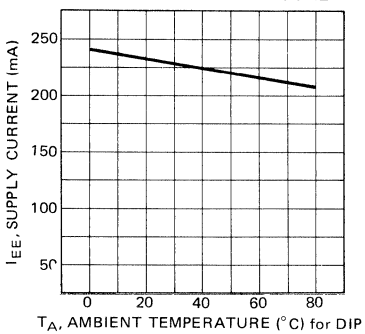


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

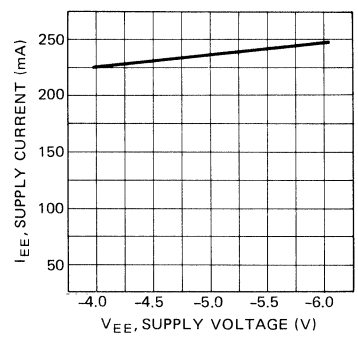


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

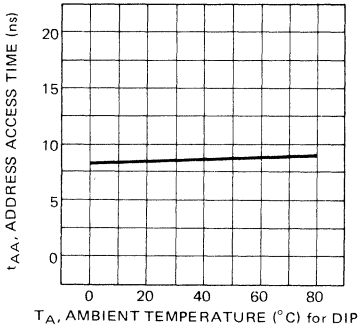


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

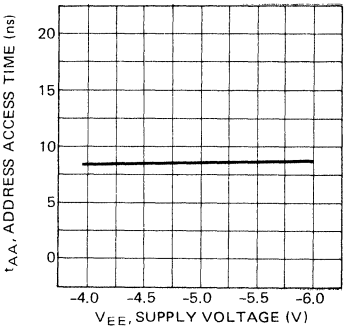


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

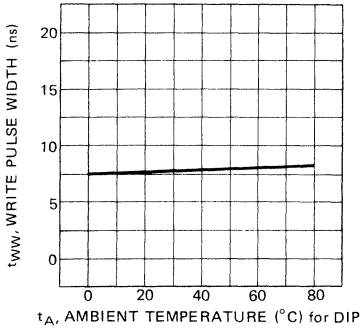
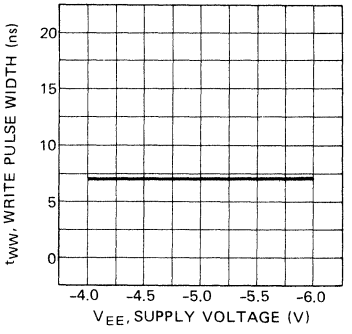


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



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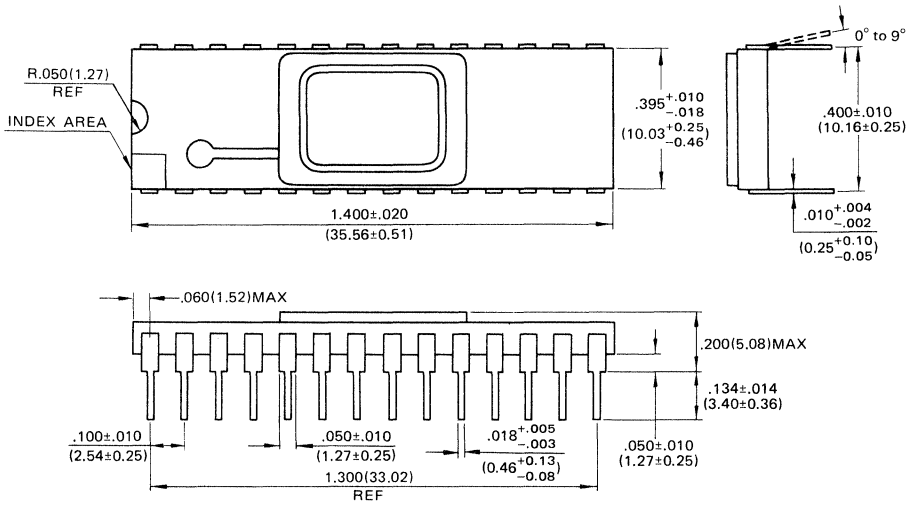
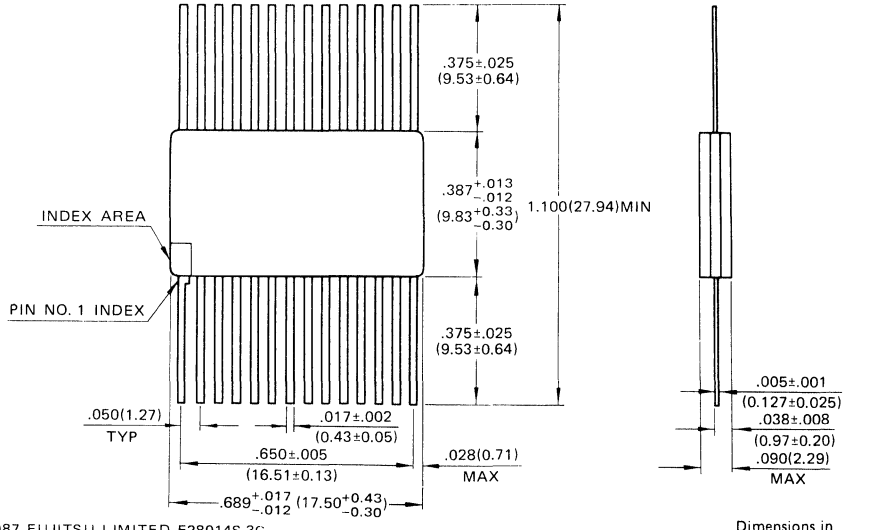
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

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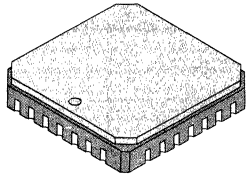
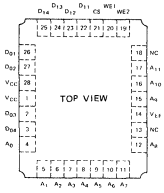
PACKAGE DIMENSIONS (continued)

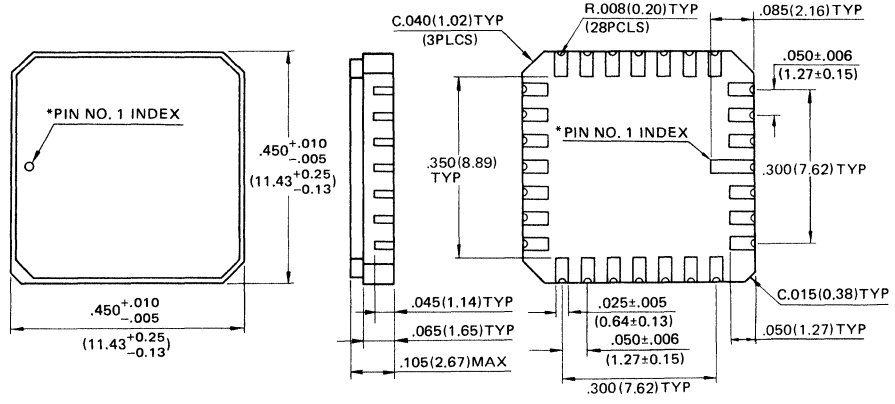


LCC-28C-F01

PAD CONFIGURATION

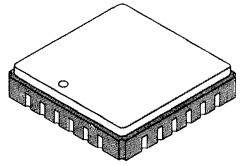


28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F01)



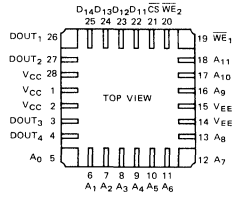
*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

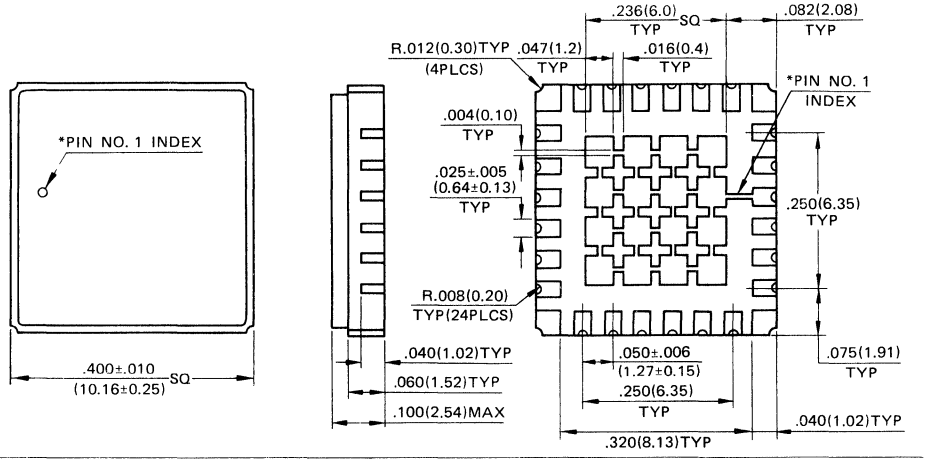


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

1

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10484-15

February 1988
Edition 2.0

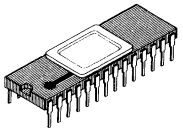
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484 is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

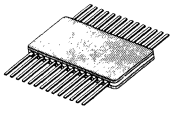
The MBM 10484 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484 is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package). It also features 28-pin ceramic DIP or Flat package, and is fully compatible with industry-standard 10 K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 15 ns max.
- Chip select access time: 8 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.07 mW/bit typ.
- DOPOS and IOP-II processing

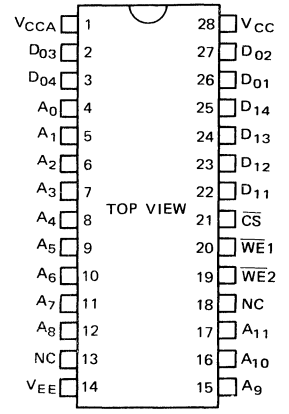


CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

PIN ASSIGNMENT



VCC grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

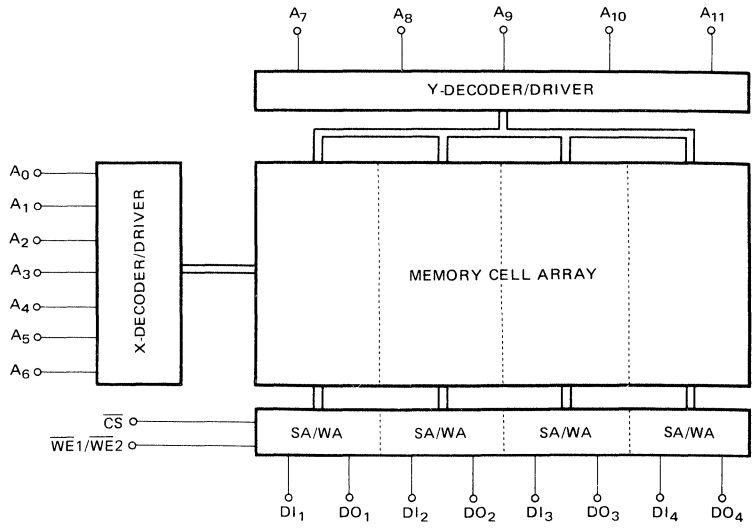
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 10484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}1/\overline{WE}2$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE}1$ and $\overline{WE}2$ are low.
*H = Either $\overline{WE}1$ or $\overline{WE}2$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM 10484 is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}1/\overline{WE}2$) inputs With both $\overline{WE}1/\overline{WE}2$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE}1$ or $\overline{WE}2$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

1

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-240			mA	0°C to 75°C

CAPACITANCE

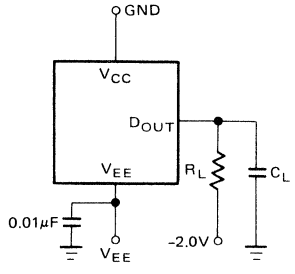
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

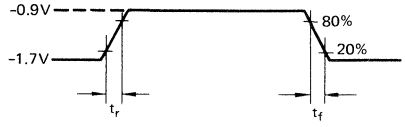
1

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





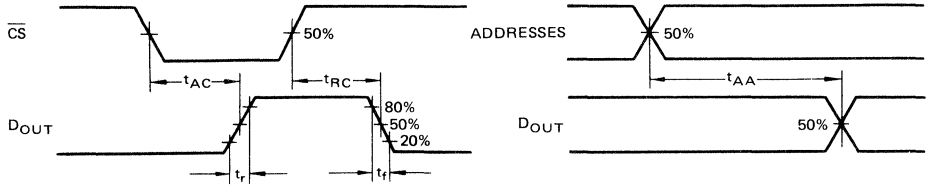
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15	ns
Chip Select Access Time	t_{AC}			8	ns
Chip Select Recovery Time	t_{RC}			8	ns

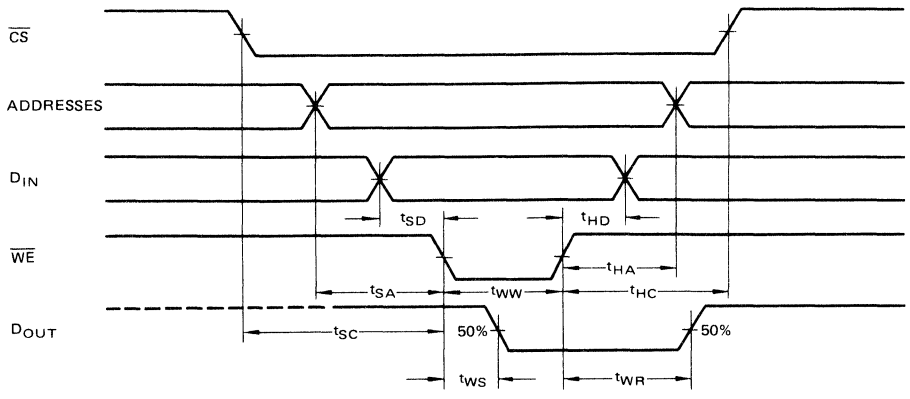
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15			ns
Write Disable Time	t_{WS}			8	ns
Write Recovery Time	t_{WR}			17	ns
Address Set Up Time	t_{SA}	3			ns
Chip Select Set Up Time	t_{SC}	3			ns
Data Set Up Time	t_{SD}	3			ns
Address Hold Time	t_{HA}	2			ns
Chip Select Hold Time	t_{HC}	2			ns
Data Hold Time	t_{HD}	2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.5		ns
Output Fall Time	t_f		2.5		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

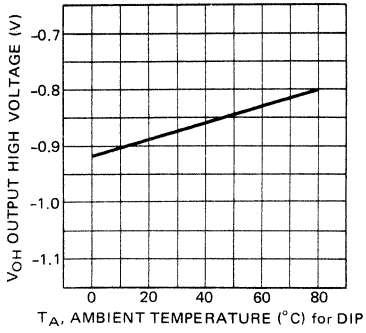


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

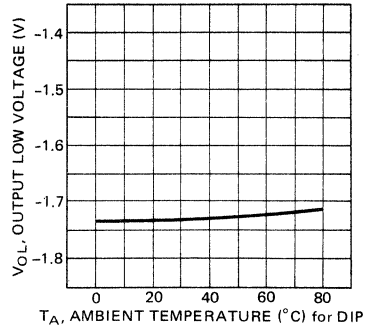


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

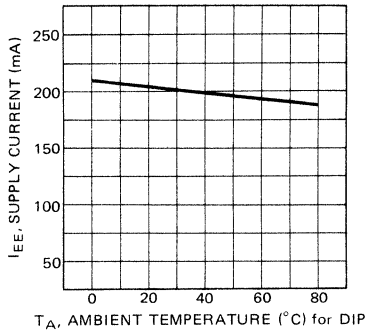


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

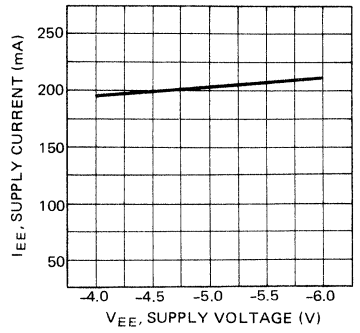


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

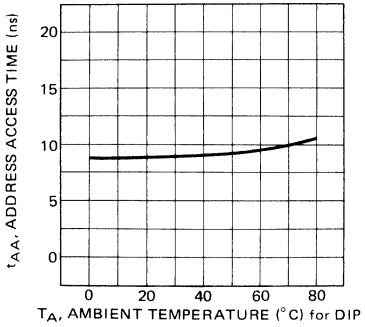


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

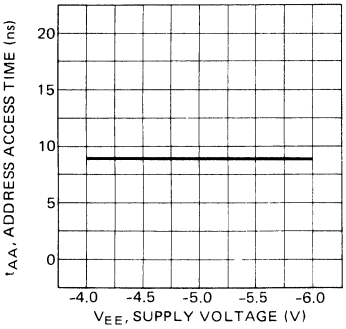


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

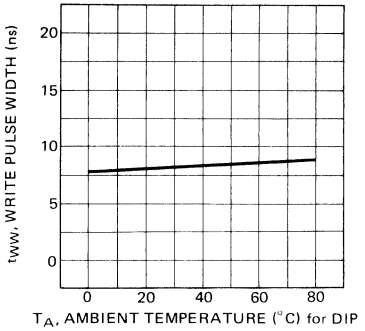
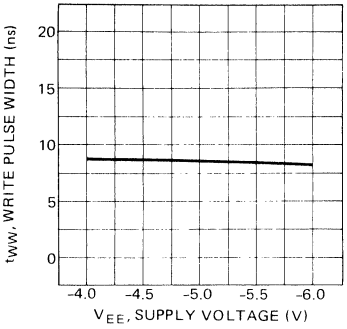
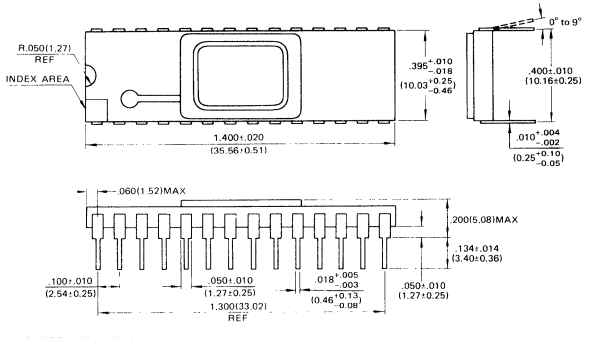


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



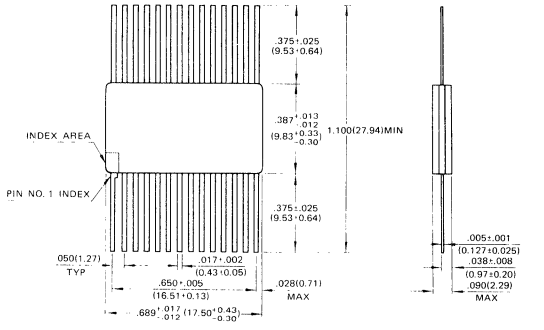
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100484-15

February 1988
Edition 2.0

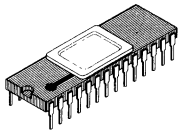
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100484 is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

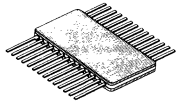
The MBM 100484 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100484 is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package). It also features 28-pin DIP or Flat package, and is fully compatible with industry-standard 100 K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 15 ns max.
- Chip select access time: 8 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.06 mW/bit typ.
- DOPOS and IOP-II processing

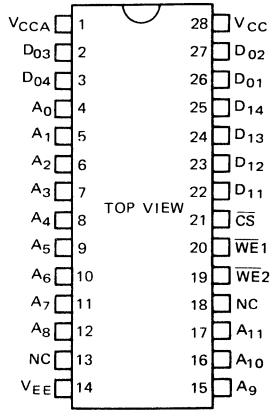


CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

PIN ASSIGNMENT



VCC grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

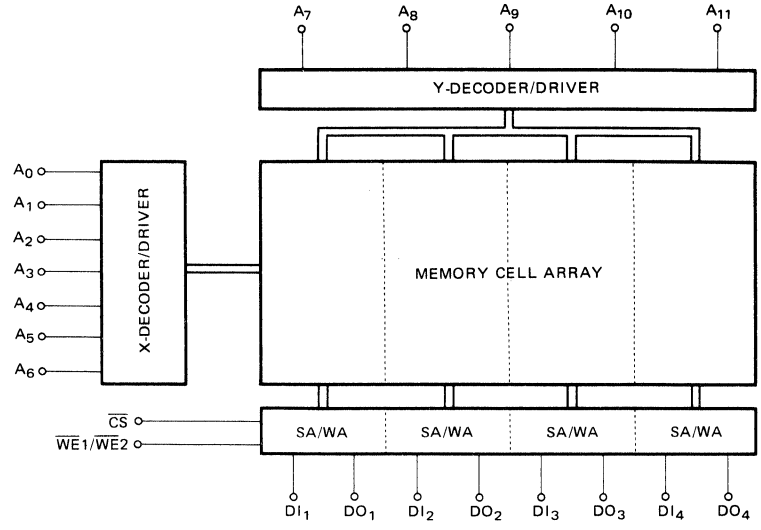
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 100484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM 100484 is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs. With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = –4.5 V, Output Load = 50 Ω to –2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-240			mA

CAPACITANCE

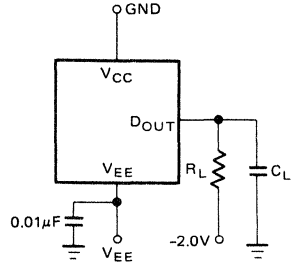
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

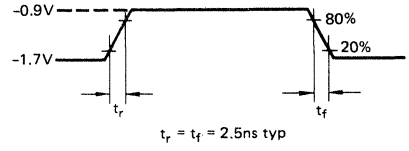
1

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

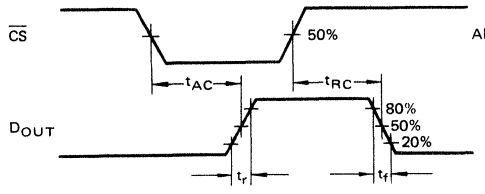
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

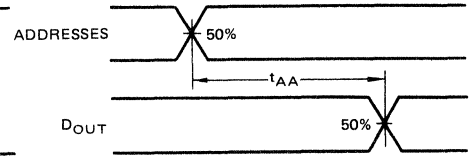
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15	ns
Chip Select Access Time	t_{AC}			8	ns
Chip Select Recovery Time	t_{RC}			8	ns

READ CYCLE TIMING DIAGRAMS

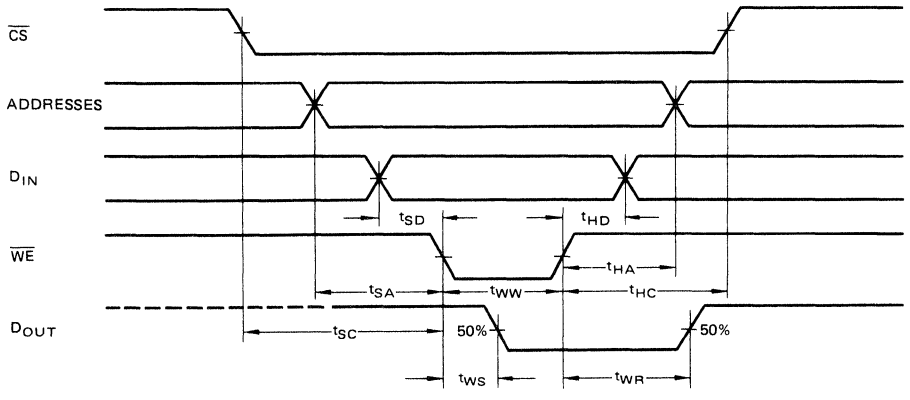




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15			ns
Write Disable Time	t_{WS}			8	ns
Write Recovery Time	t_{WR}			17	ns
Address Set Up Time	t_{SA}	3			ns
Chip Select Set Up Time	t_{SC}	3			ns
Data Set Up Time	t_{SD}	3			ns
Address Hold Time	t_{HA}	2			ns
Chip Select Hold Time	t_{HC}	2			ns
Data Hold Time	t_{HD}	2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.5		ns
Output Fall Time	t_f		2.5		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

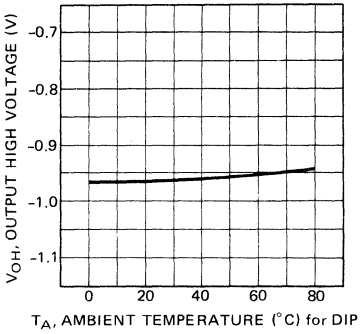


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

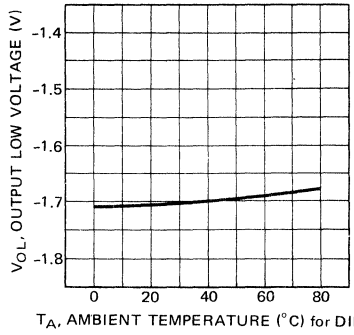


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

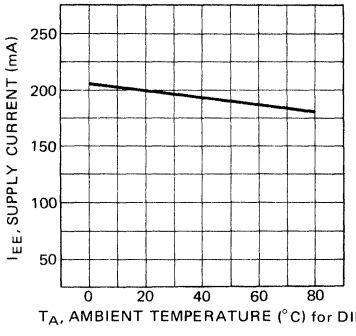


Fig. 6 – SUPPLY CURRENT vs. SUPPLY VOLTAGE

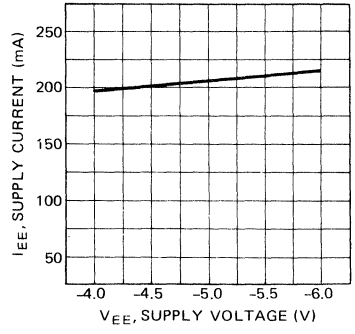


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

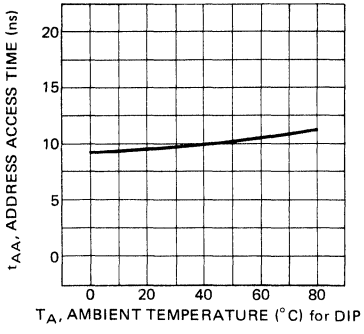


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

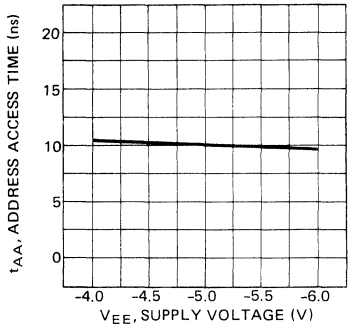


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

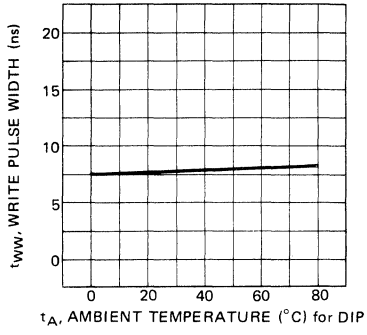
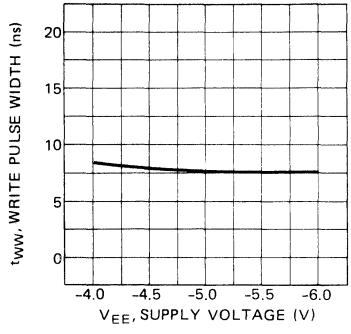
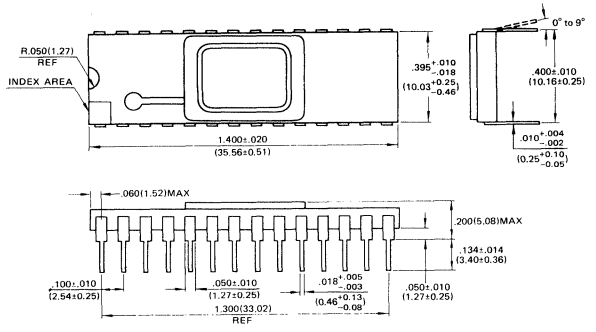


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



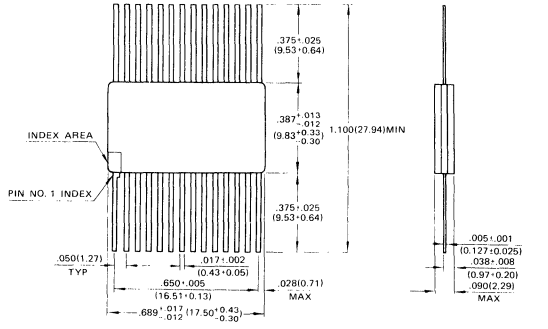
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in inches and (millimeters)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in inches (millimeters)

FUJITSU

ECL 65536-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10490-15
MBM10490-25

July 1987
Edition 3.0

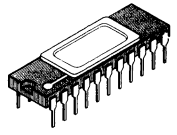
65536-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10490 is fully decoded 65536-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on-chip voltage compensation for improved noise margin.

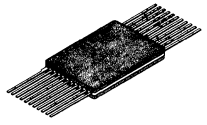
The MBM 10490 offers extremely small cell and chip size, realized through the use of Fujitsu's patented IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10490 is specified over a temperature range of from 0°C to 75°C (T_C). It also features 22 pin Ceramic DIP or Flat Package. It is fully compatible with industry-standard 10K-series ECL familes.

- 65536 words x 1 bit organization
- On-chip voltage compensation for improved noise margin.
- Fully compatible with industry-standard 10K-series ECL families.
- Address access time: : 15 ns max. (MBM 10490-15)
  25 ns max. (MBM 10490-25)
- Chip select access time : 10 ns max. (MBM 10490-15)
  15 ns max. (MBM 10490-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.017 mW/bit typ. (MBM 10490-15)
  0.012 mW/bit typ. (MBM 10490-25)
- IOP-II

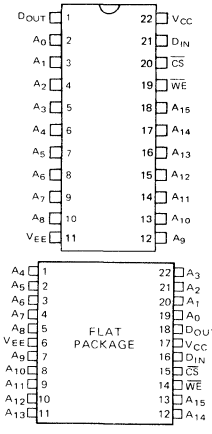


CERAMIC PACKAGE
DIP-22C-A02



CERAMIC PACKAGE
FPT-22C-C01

PIN ASSIGNMENT



*V_{CC} grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

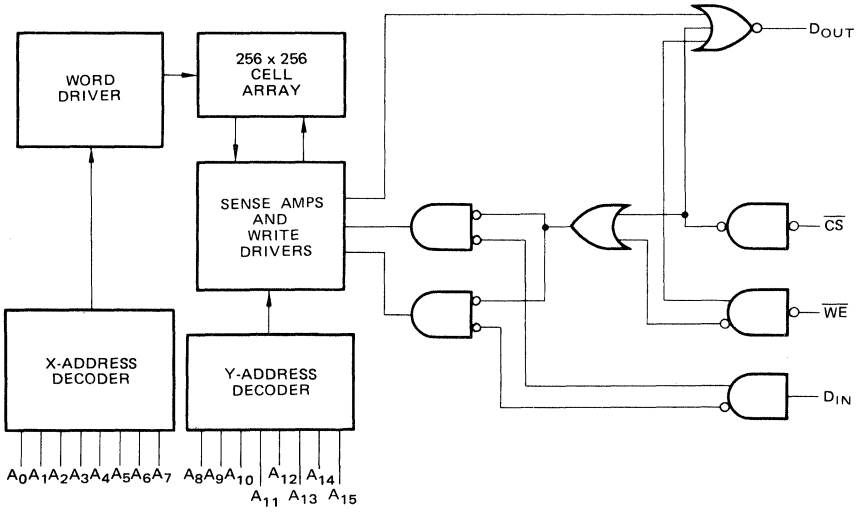
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 10490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by one bit. Memory cell selection is achieved by means of a 16 bit address designated A_0 through A_{15}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_C = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10490-15	I_{EE}	-300			mA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10490-25	I_{EE}	-200			mA	0°C to 75°C

CAPACITANCE

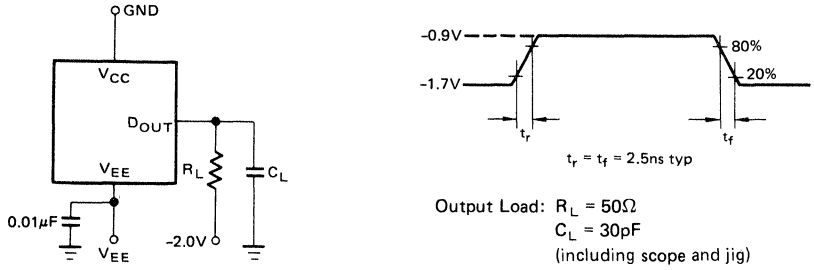
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		4	7	pF

1

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_C = 0°C to 85°C, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS



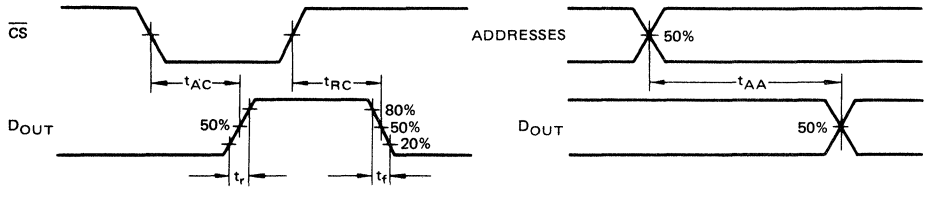
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			10			15	ns
Chip Select Recovery Time	t_{RC}			10			15	ns

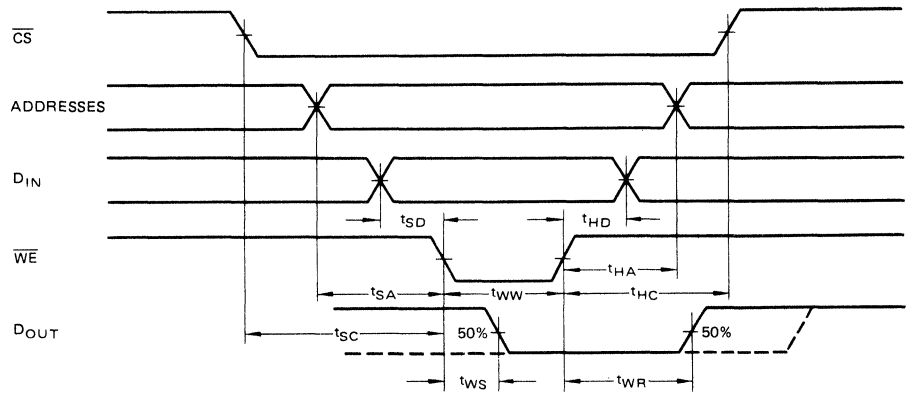
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			20			ns
Write Disable Time	t_{WS}			10			15	ns
Write Recovery Time	t_{WR}			15			25	ns
Address Set Up Time	t_{SA}	2			3			ns
Chip Select Set Up Time	t_{SC}	2			3			ns
Data Set Up Time	t_{SD}	2			3			ns
Address Hold Time	t_{HA}	2			2			ns
Chip Select Hold Time	t_{HC}	2			2			ns
Data Hold Time	t_{HD}	2			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

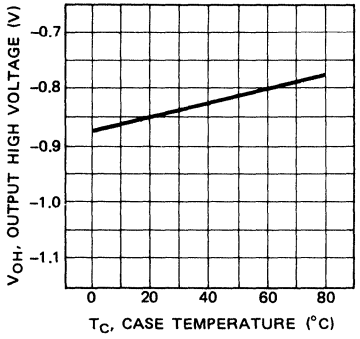


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

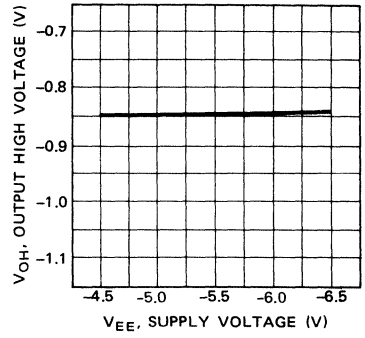


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

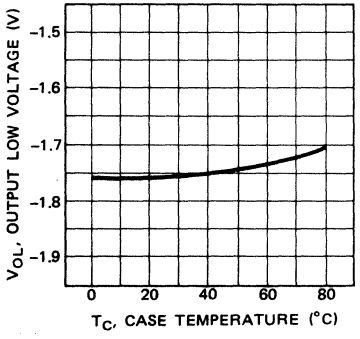


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

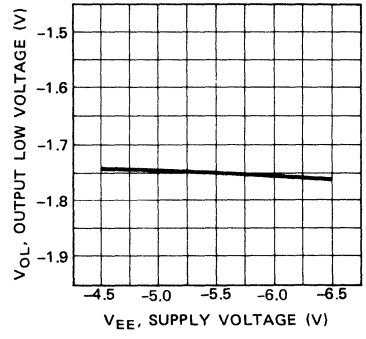


Fig. 7 – SUPPLY CURRENT vs CASE TEMPERATURE

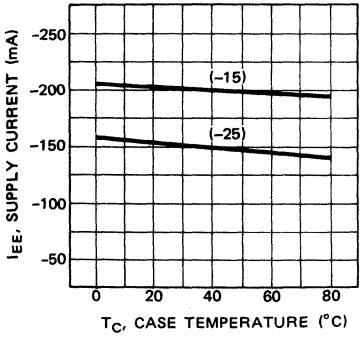


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

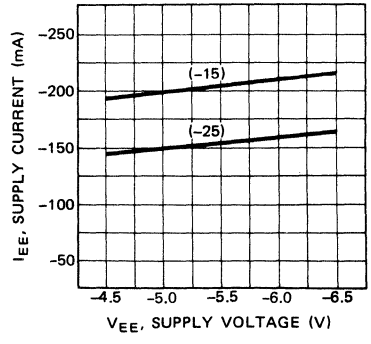


Fig. 9 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

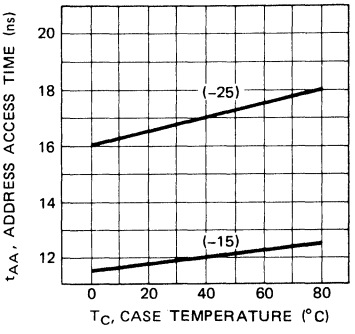


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

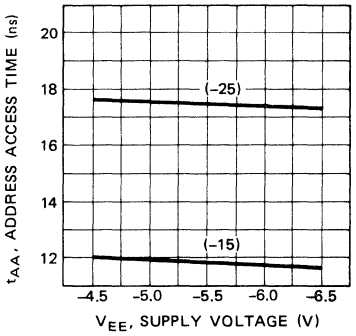


Fig. 11 – WRITE PULSE WIDTH vs CASE TEMPERATURE

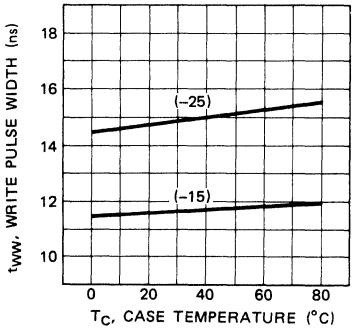
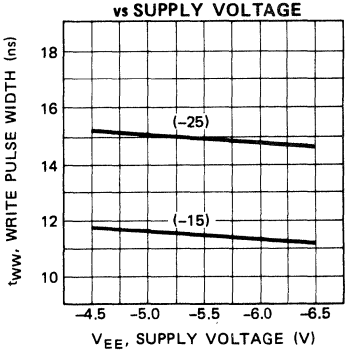


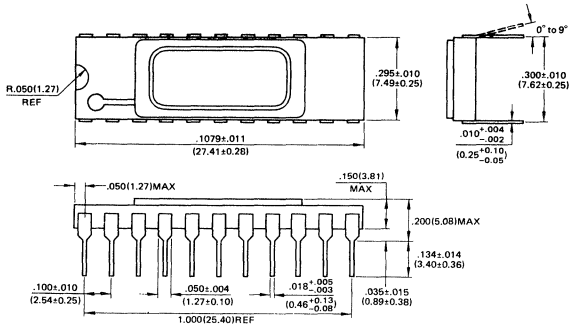
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



1

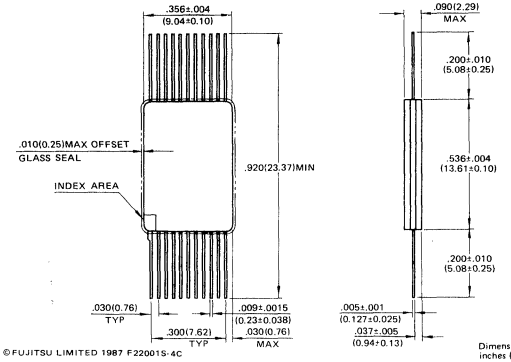
PACKAGE DIMENSIONS

22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-22C-A02)



Dimensions in inches (millimeters)

22-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-22C-C01)



Dimensions in inches (millimeters)

FUJITSU

ECL 65536-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100490-15
MBM100490-25

July 1987
Edtion 1.0

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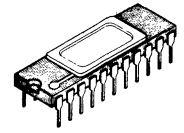
65536-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100490 is fully decoded 65536-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on-chip voltage temperature compensation for improved noise margin.

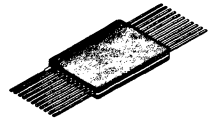
The MBM 100490 offers extremely small cell and chip size, realized through the use of Fujitsu's patened IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 100490 is specified over a temperature range of from 0°C to 85°C (T_C). It also features 22 pin Ceremic DIP or Flat Package. It is fully compatible with industry-standard 100K-series ECL familes.

- 65536 words x 1 bit organization
- On-chip voltage temperature compensation for improved noise margin.
- Fully compatible with industry-standard 100K-series ECL families.
- Address access time: 15 ns max. (MBM 100490-15)
  25 ns max. (MBM 100490-25)
- Chip select access time: 10 ns max. (MBM 100490-15)
  15 ns max. (MBM 100490-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.017 mW/bit typ. (MBM 100490-15)
  0.012 mW/bit typ. (MBM 100490-25)
- IOP-II

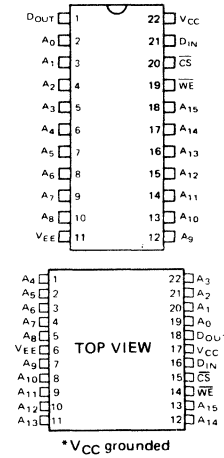


CERAMIC PACKAGE
DIP-22C-A02



CERAMIC PACKAGE
FPT-22C-C01

PIN ASSIGNMENT



*V_{CC} grounded

LCC PAD CONFIGURATION : SeePage 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature under Bias	T_C	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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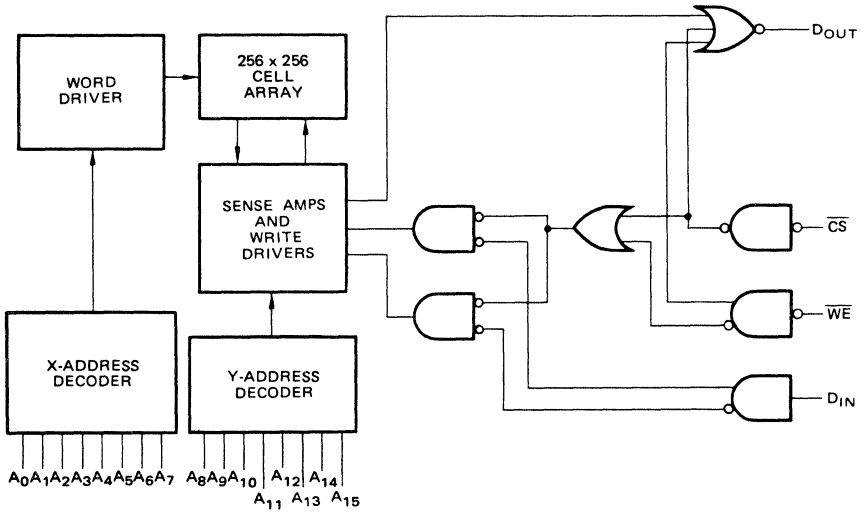
Fig. 1 – MBM 100490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by one bit. Memory cell selection is achieved by means of a 16 bit address designated A_0 through A_{15}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature
Supply Voltage	V_{EE}	5.7	4.5	4.2	V	0°C to 85°C

1

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = –4.5V, Output Load = 50Ω and 30pF to –2.0V, T_C = 0°C to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	–1025		–880	mV
Ouput Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	–1810		–1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OHC}	–1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			–1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	–1165		–880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)		V_{IL}	–1810		–1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	–50			μA
CS Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	MBM 100490-15	I_{EE}	–300			mA
	MBM 100490-25		–200			

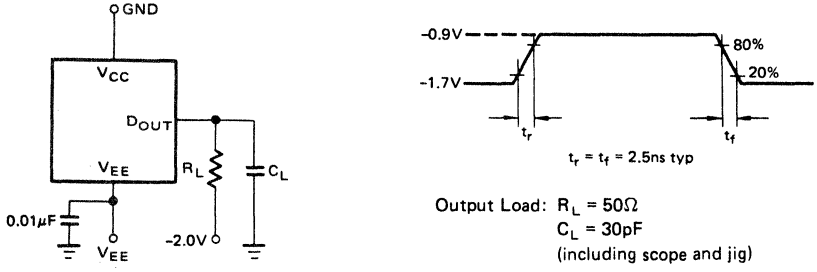
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		4	7	pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_C = 0°C to 85°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



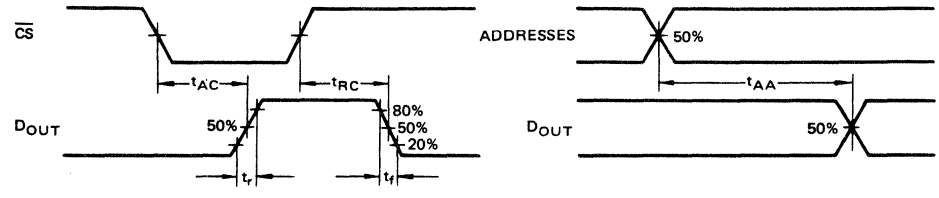
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			10			15	ns
Chip Select Recovery Time	t_{RC}			10			15	ns

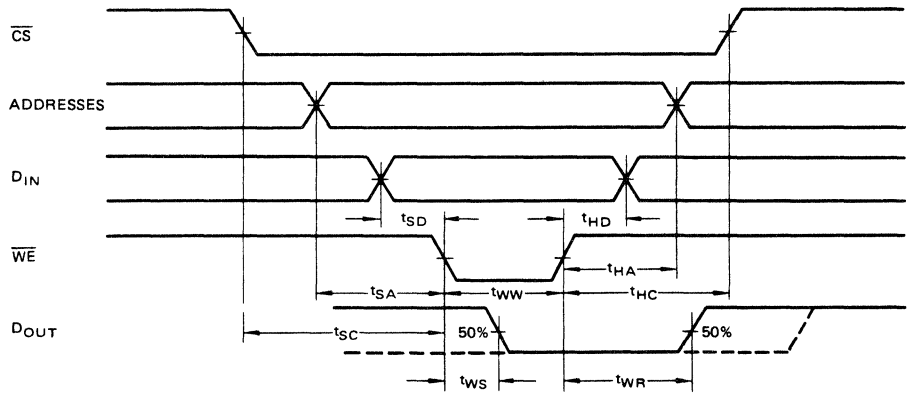
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			20			ns
Write Disable Time	t_{WS}			10			15	ns
Write Recovery Time	t_{WR}			15			25	ns
Address Set Up Time	t_{SA}	2			3			ns
Chip Select Set Up Time	t_{SC}	2			3			ns
Data Set Up Time	t_{SD}	2			3			ns
Address Hold Time	t_{HA}	1			2			ns
Chip Select Hold Time	t_{HC}	1			2			ns
Data Hold Time	t_{HD}	1			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

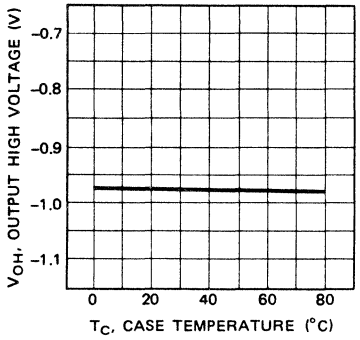


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

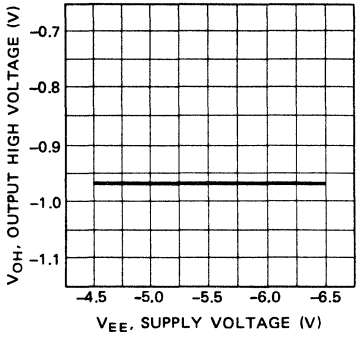


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

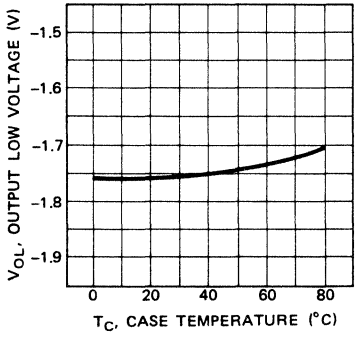


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

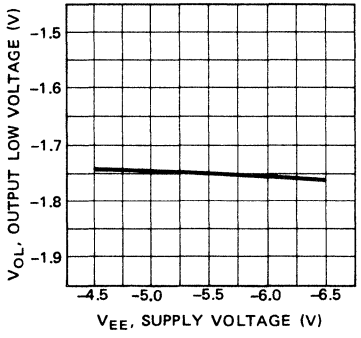


Fig. 7 – SUPPLY CURRENT vs CASE TEMPERATURE

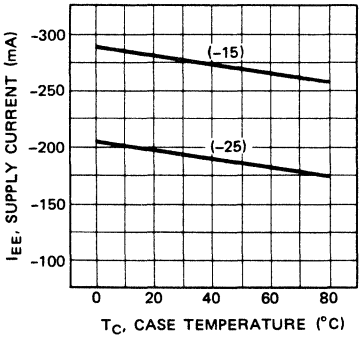


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

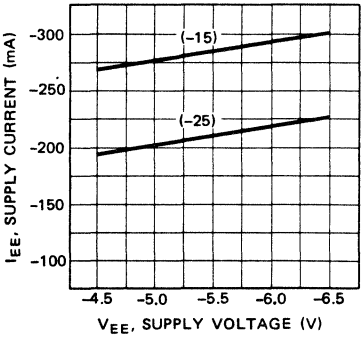


Fig. 9 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

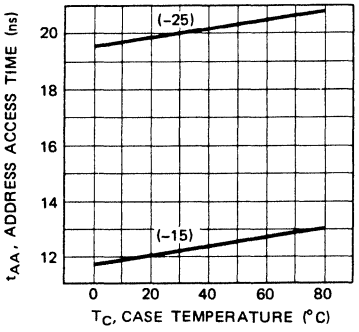


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

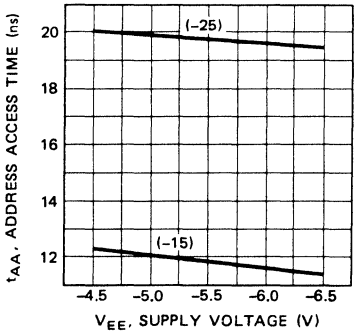


Fig. 11 – WRITE PULSE WIDTH vs CASE TEMPERATURE

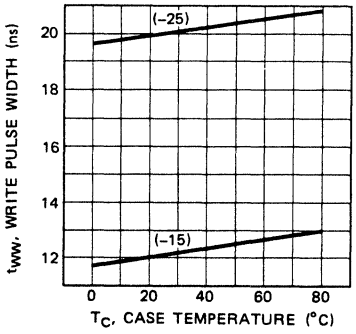
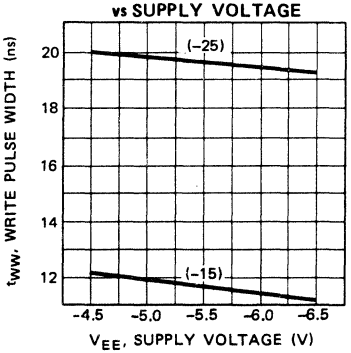
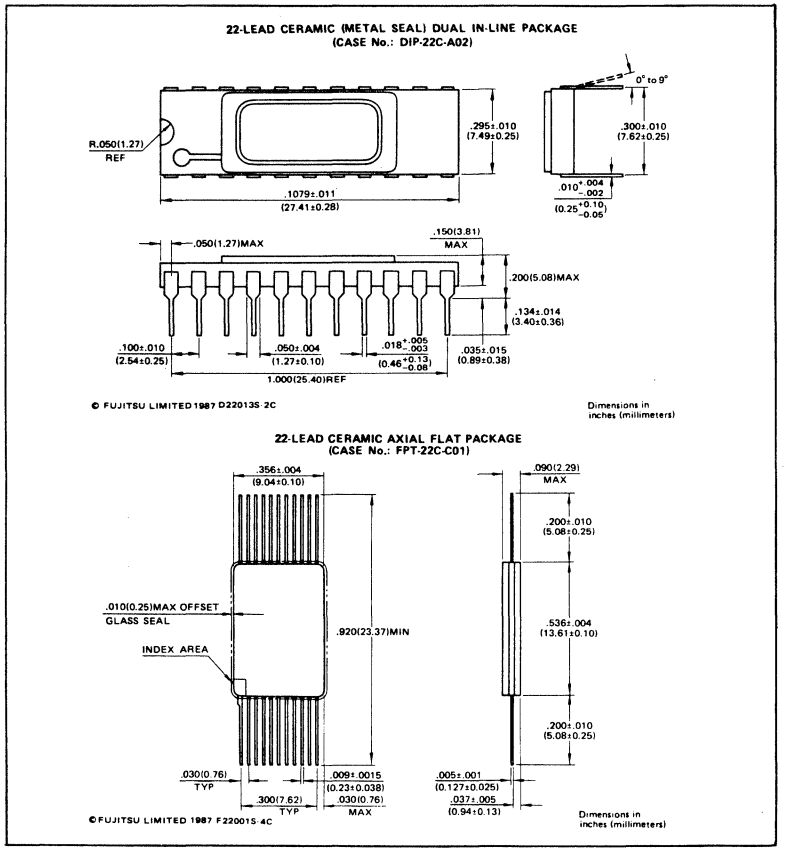


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS



October 1989
Edition 2.0

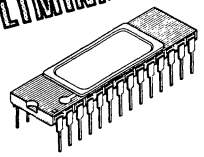
FUJITSU

DATA SHEET

MBM10494-7/-8

65536–BIT BIPOLAR ECL RANDOM ACCESS MEMORY

PRELIMINARY

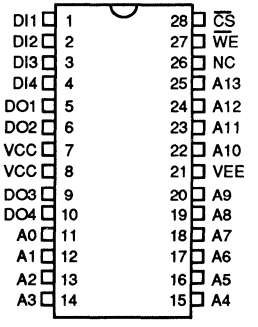


CERAMIC PACKAGE
DIP–28C–A10

CERAMIC PACKAGE
FPT–28C–C03

FPT–28C–A02 : See Page 7

PIN ASSIGNMENT
(TOP VIEW)



* V cc grounded

FPT–28C–A02 : See Page 7

DESCRIPTION

The Fujitsu MBM10494 is fully decoded 65536–bit ECL read/write random access memory designed for high–speed scratch pad, control and buffer storage applications. The device is organized as 16384 words by 4 bits, and it features on–chip voltage compensation for improved noise margin.

The MBM10494 offers extremely small cell size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as ESPER (Emitter–base Self aligned structure with Polysilicon Electrodes and Resistors.) processing.

Operation for the MBM10494 is specified over a case temperature range of from 0°C to 55°C (TC). It also features 28–pin DIP or Flat Package, and is fully compatible with Industry standard 10K–ECL families.

- 16384 words by 4 bits organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10K series ECL families
- Address access time : 7ns (MBM10494–7)
  8ns (MBM10494–8)
- Chip select access time : 5ns (MBM10494–7)
  5ns (MBM10494–8)
- Power dissipation : 1716mW max
- Open emitter output for ease of memory expansion
- DOPOS and ESPER processing

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –6.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

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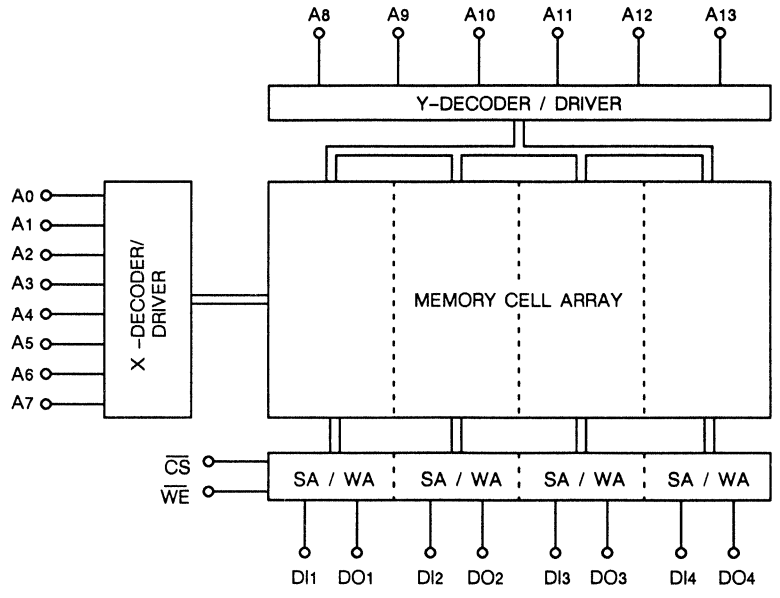
Fig.1 – MBM10494 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10494 is fully decoded read/write random access memory organized as 16384 words by 4 bits. Memory cell selection is achieved by means of a 14 bit address designated A_0 though A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω to -2.0V, T_C = 0°C to 55°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TC
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 55°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 55°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 55°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 55°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 55°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 55°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	μA	0°C to 55°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			μA	0°C to 55°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	μA	0°C to 55°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-330			mA	0°C to 55°C

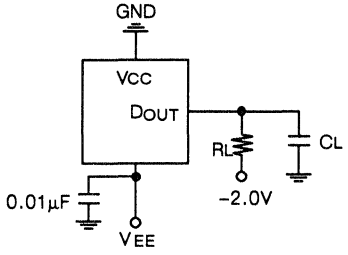
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4.0		pF
Output Pin Capacitance	C_{OUT}		5.0		pF

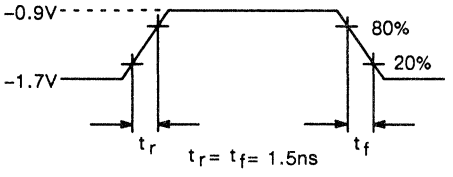
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 55°C, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

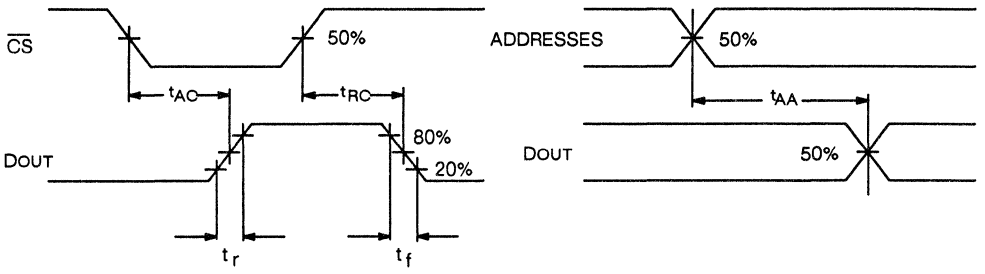


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10494-7			MBM0494-8			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			7.0			8.0	ns
Chip Select Access Time	t_{AC}			5.0			6.0	ns
Chip Select Recovery Time	t_{RC}			5.0			6.0	ns

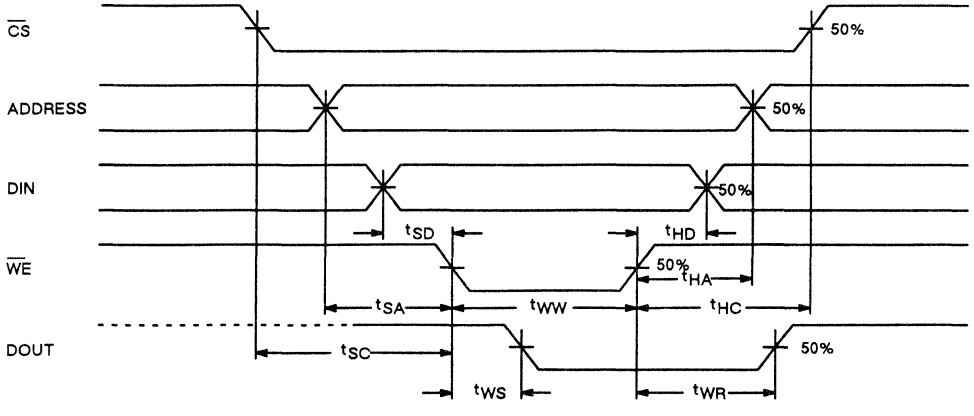
Fig. 3 - READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	MBM10494-7			MBM10494-8			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	7.0			8.0			ns
Write Disable Time	t_{WS}			5.0			5.0	ns
Write Recovery Time	t_{WR}			8.0			9.0	ns
Address Set Up Time	t_{SA}	1.0			1.0			ns
Chip Select Set Up Time	t_{SC}	1.0			1.0			ns
Data Set Up Time	t_{SD}	1.0			1.0			ns
Address Hold Time	t_{HA}	1.0			1.0			ns
Chip Select Hold Time	t_{HC}	1.0			1.0			ns
Data Hold Time	t_{HD}	1.0			1.0			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



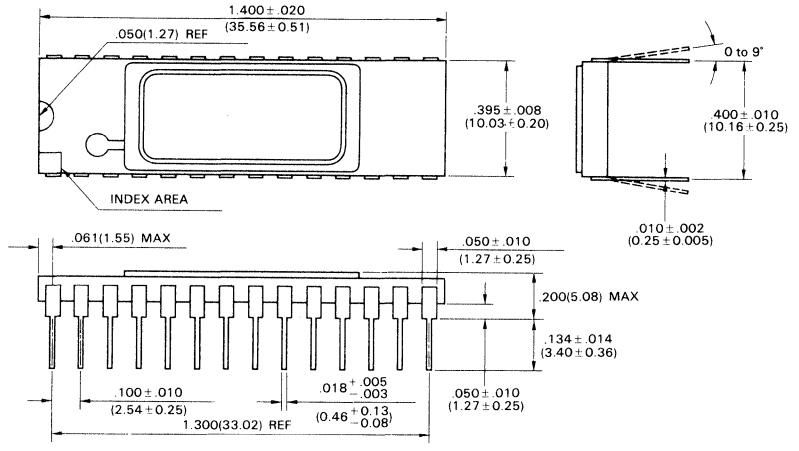
RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

PACKAGE DIMENSIONS

(Suffix : -C)

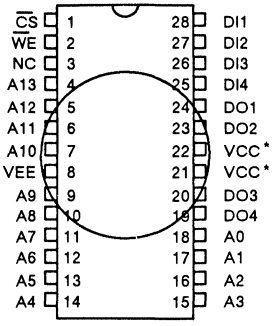
28-LEAD CERAMIC DUAL IN-LINE PACKAGE
(Case No. : DIP-28C-A10)



Dimensions in inches
(millimeters)

(Suffix : -CFF)

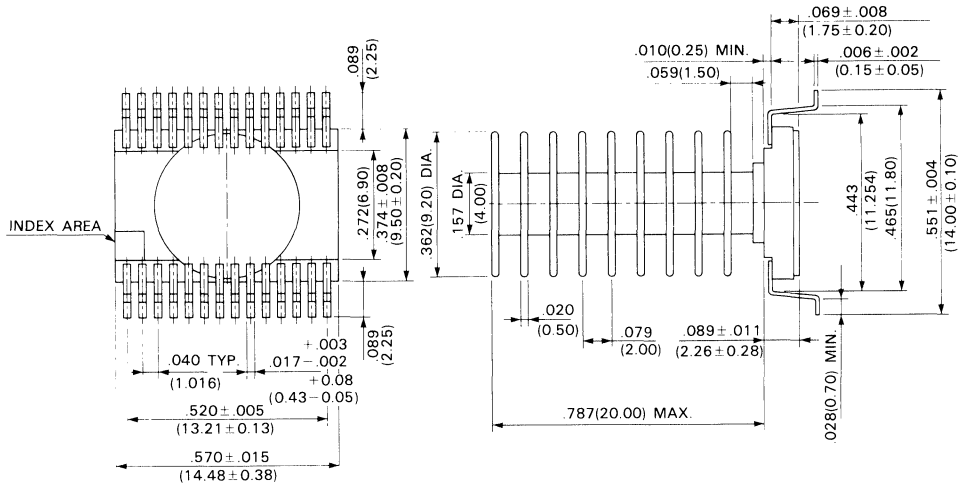
PIN ASSIGNMENT



* V_{CC} grounded

28-LEAD CERAMIC FLAT PACKAGE

(Code No. : FPT-28C-A02)



Dimensions in inches
(millimeters)

1

October 1989
Edition 2.0

FUJITSU

DATA SHEET

MBM101494-7/-8

65536–BIT BIPOLAR ECL RANDOM ACCESS MEMORY

PRELIMINARY

1

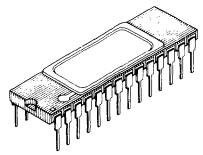
DESCRIPTION

The Fujitsu MBM101494 is fully decoded 65536–bit ECL read/write random access memory designed for high–speed scratch pad, control and buffer storage applications. The device is organized as 16384 words by 4 bits, and it features on–chip voltage/temperature compensation for improved noise margin.

The MBM101494 offers extremely small cell size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as ESPER (Emitter–base Self aligned structure with Polysilicon Electrodes and Resistors.) processing.

Operation for the MBM101494 is specified over a case temperature range of from 0°C to 55°C (Tc). It also features 28–pin DIP or Flat Package, and is fully compatible with Industry standard 100K–ECL families.

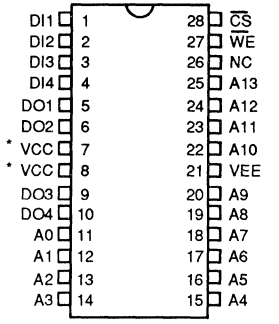
- 16384 words by 4 bits organization
- On–chip voltage/temperatuere compensation for improved noise margin
- Fully compatible with industry standard 100K series ECL families
- Address access time : 7ns (MBM10494–7)
  8ns (MBM10494–8)
- Chip select access time : 5ns (MBM10494–7)
  5ns (MBM10494–8)
- Power dissipation : 1716mW max
- Open emitter output for ease of memory expansion
- DOPOS and ESPER processing



CERAMIC PACKAGE
DIP–28C–A10

FPT–28C–A02 : See Page 7

PIN ASSIGNMENT
(TOP VIEW)



* V cc grounded

FPT–28C–A02 : See Page 7

ABSOLUTE MAXIMUM RATINGS (See NOTE)

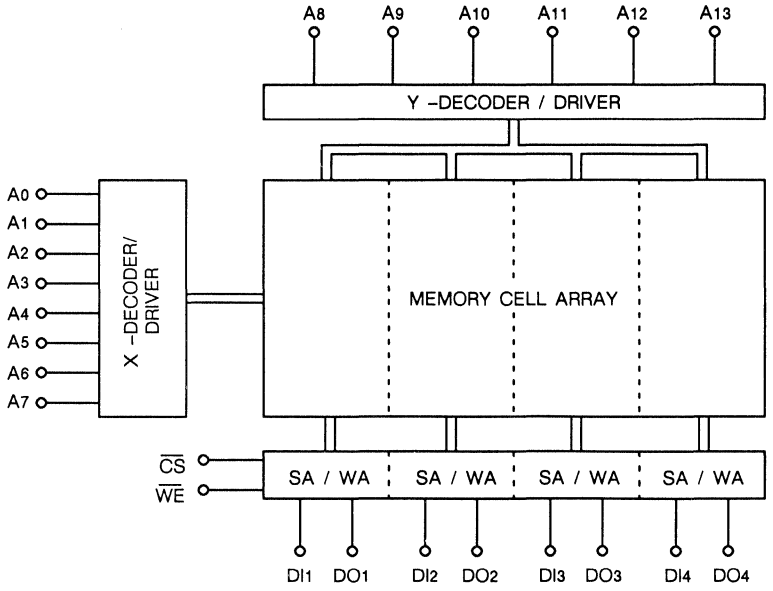
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –6.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

1

Fig.1 - MBM101494 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM101494 is fully decoded read/write random access memory organized as 16384 words by 4 bits. Memory cell selection is achieved by means of a 14 bit address designated A0 though A13. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(Vcc = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, Tc = 0°C to 55°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-330			mA

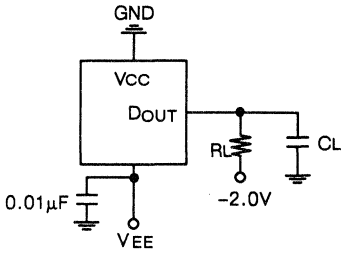
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4.0		pF
Output Pin Capacitance	C_{OUT}		5.0		pF

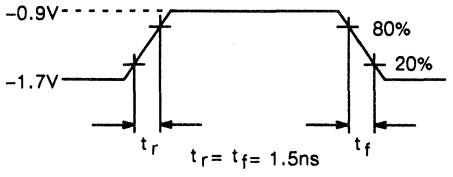
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 55°C, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

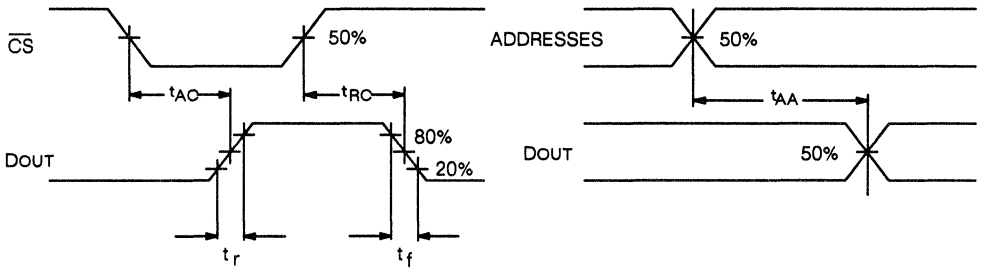


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM101494-7			MBM101494-8			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			7.0			8.0	ns
Chip Select Access Time	t_{AC}			5.0			5.0	ns
Chip Select Recovery Time	t_{RC}			5.0			5.0	ns

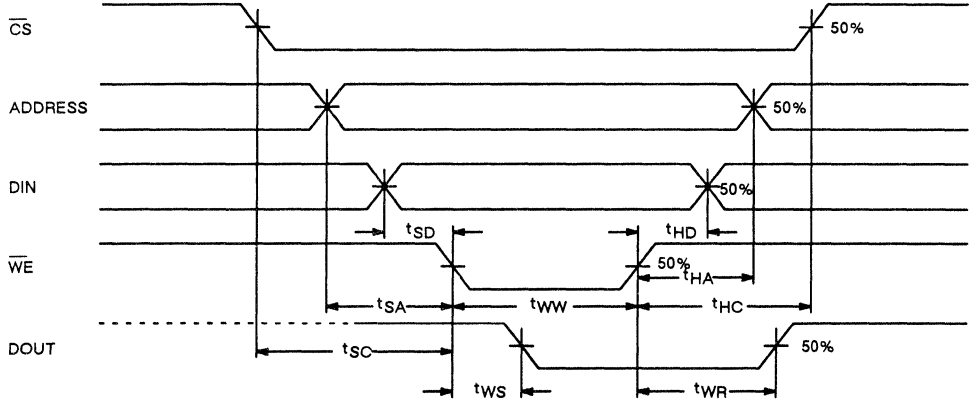
Fig. 3 - READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	MBM101494-7			MBM101494-8			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	7.0			8.0			ns
Write Disable Time	t_{WS}			5.0			5.0	ns
Write Recovery Time	t_{WR}			8.0			9.0	ns
Address Set Up Time	t_{SA}	1.0			1.0			ns
Chip Select Set Up Time	t_{SC}	1.0			1.0			ns
Data Set Up Time	t_{SD}	1.0			1.0			ns
Address Hold Time	t_{HA}	1.0			1.0			ns
Chip Select Hold Time	t_{HC}	1.0			1.0			ns
Data Hold Time	t_{HD}	1.0			1.0			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

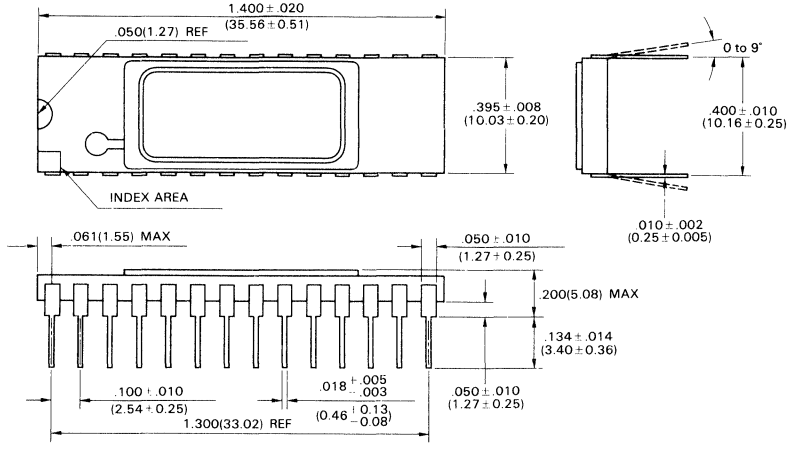
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

PACKAGE DIMENSIONS

(Suffix : -C)

28-LEAD CERAMIC DUAL IN-LINE PACKAGE

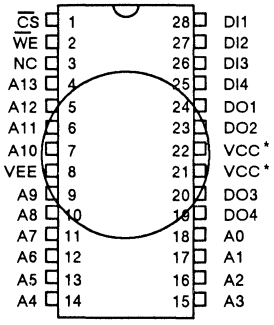
(Case No. : DIP-28C-A10)



Dimensions in inches
(millimeters)

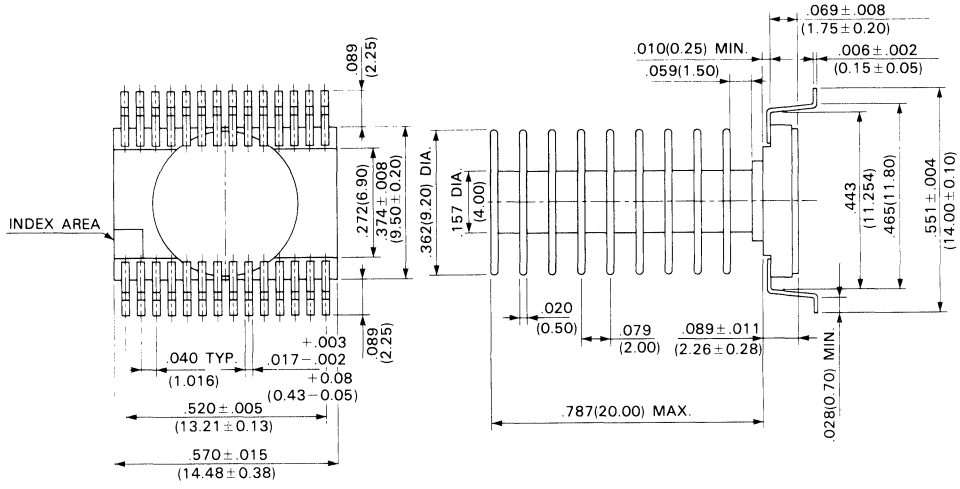
(Suffix : -CFF)

PIN ASSIGNMENT



* V_{CC} grounded

28-LEAD CERAMIC FLAT PACKAGE
(Code No. : FPT-28C-A02)



Dimensions in inches
(millimeters)

1

Section 2

BiCMOS ECL RAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options		
2–3	MBM10C490–15	15	65536 bits (65536w x 1b)	22-pin	Ceramic	DIP, FPT
2–13	MBM100C490–15	15	65536 bits (65536w x 1b)	22-pin	Ceramic	DIP, FPT
				24-pad	Plastic	LCC
				24-pad	Ceramic	LCC
2–23	MBM10C494–15	15	65536 bits (16384w x 4b)	28-pin	Ceramic	DIP, FPT
				28-pin	Plastic	FPT
				28-pad	Ceramic	LCC
2–33	MBM100C494–15	15	65536 bits (16384w x 4b)	28-pin	Ceramic	DIP, FPT
				28-pad	Ceramic	LCC
2–43	MBM10C500–15	15	262144 bits (262144w x 1b)	24-pin	Ceramic	DIP, FPT
				24-pad	Ceramic	LCC
2–53	MBM100C500–15	15	262144 bits (262144w x 1b)	24-pin	Ceramic	DIP, FPT
	–17	17		24-pad	Ceramic	LCC
2–61	MBM101C500–15	15	262144 bits (262144w x 1b)	24-pin	Ceramic	DIP, FPT
				24-pad	Ceramic	LCC
2–71	MBM100C504–15	15	262144 bits (65536w x 4b)	32-pin	Ceramic	DIP, FPT
				28-pin	Ceramic	FPT

2

October 1989
Edition 2.0

FUJITSU

DATA SHEET

MBM10C490-15

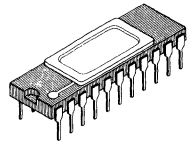
65536–BIT BICMOS ECL RANDOM ACCESS MEMORY

DESCRIPTION

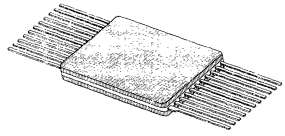
The Fujitsu MBM10C490 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on chip voltage compensation for improvednoise margin.

Operation for the MBM10C490 is specified over an ambient temperature range of from 0°C to 75°C (T_A). It is packaged in 22–pin ceramic DIP, Flatpackage or LCC and is fully compatible with industory standard 10K series ECL families.

- 65536 words by 1 bit organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Address access time : 15ns
- Chip select access time : 15ns
- Power dissipation : 728mW max (at minimum cycle)
- Open emitter output for ease of memory expansion
- BICMOS processing



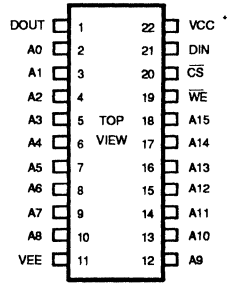
CERAMIC PACKAGE
DIP–22C–A02



CERAMIC PACKAGE
FPT–22C–C01

LCC–22C–A01 : See page 10

PIN ASSIGNMENT



* VCC grounded

LCC PAD configuration : See page 10

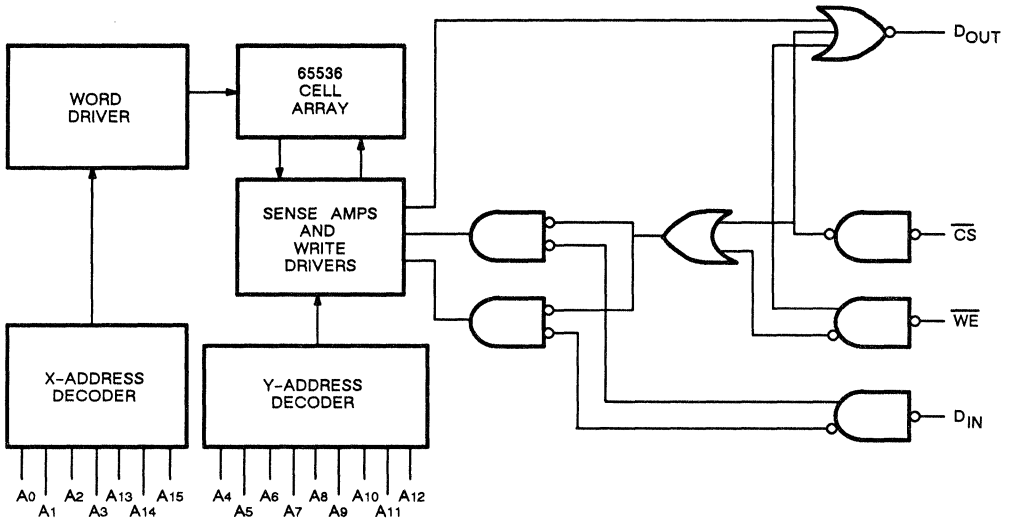
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MBM10C490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{IN}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10C490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by 1 bit. Memory cell selection is achieved by means of a 16-bit address designed A_0 through A_{15}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75

DC CHARACTERISTICS

(Vcc = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (VIN = VILmin)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-140			mA	0°C to 75°C

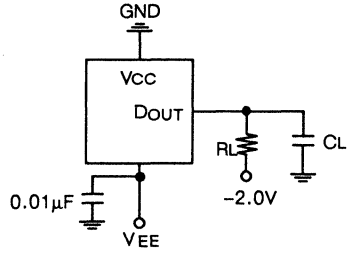
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	2.0		6.0	pF
Output Pin Capacitance	C_{OUT}	2.0		6.0	pF

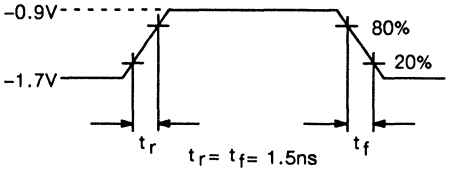
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V ±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



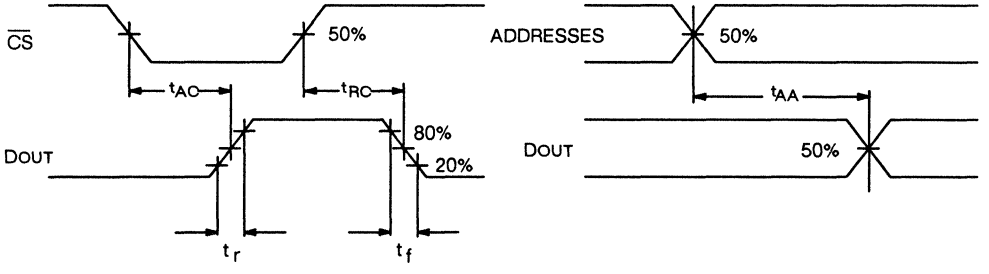
Note : All timing measurements referenced to 50% input levels.

2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	3.0		15.0	ns
Chip Select Access Time	t_{AC}	1.0		15.0	ns
Chip Select Recovery Time	t_{RC}	1.0		10.0	ns

Fig. 3 - READ CYCLE TIMING DIAGRAM

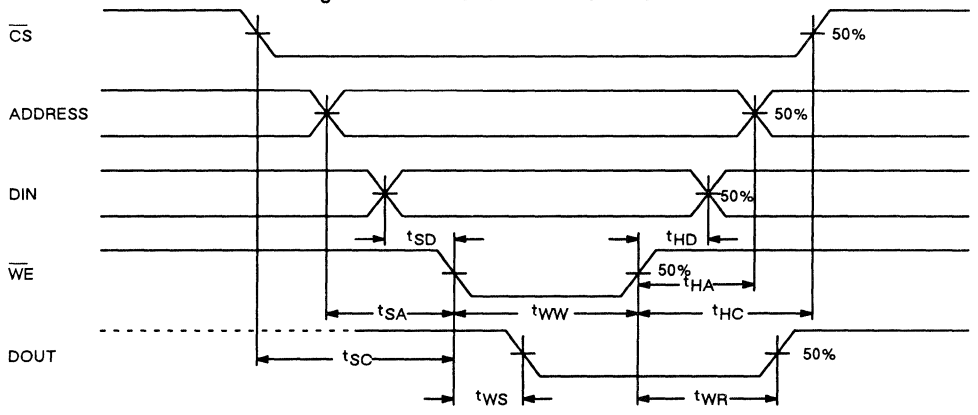


WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}	1.0		10.0	ns
Write Recovery Time	t_{WR}	1.0		18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

2

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	0.5		3.0	ns
Output Fall Time	t_f	0.5		3.0	ns

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

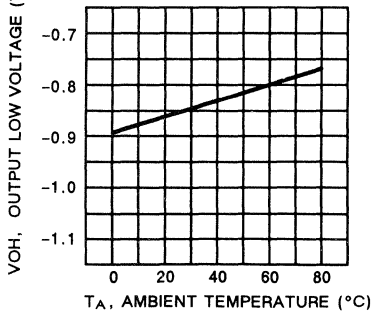


Fig. 6 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

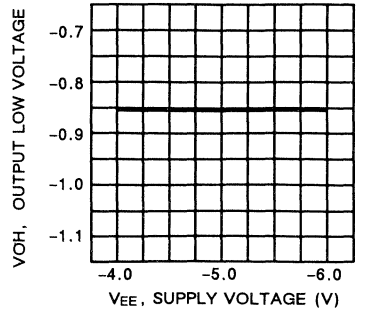


Fig. 7 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

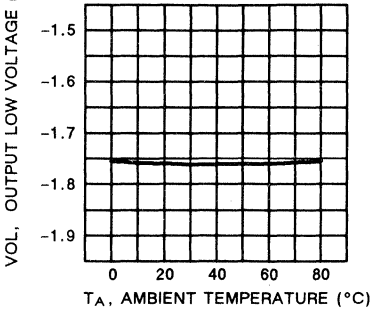


Fig. 8 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

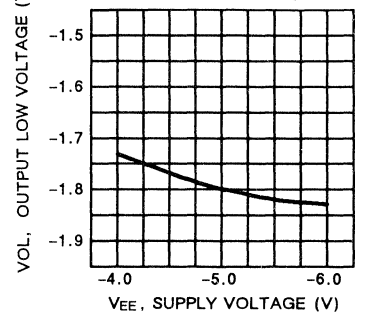


Fig. 9 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

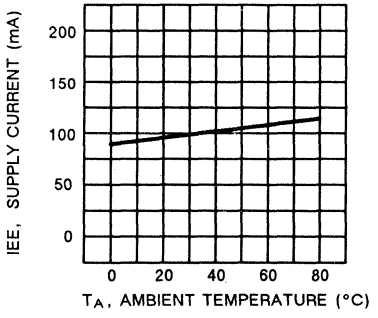


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

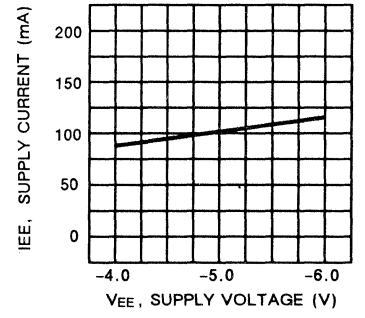


Fig. 11 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

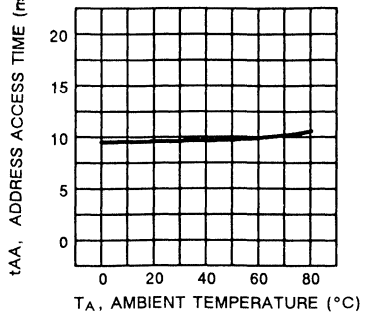


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

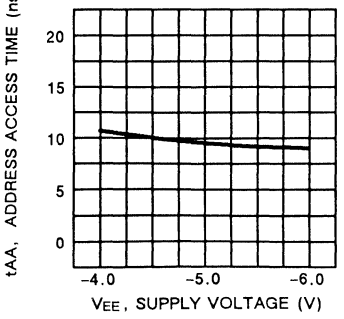


Fig. 13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

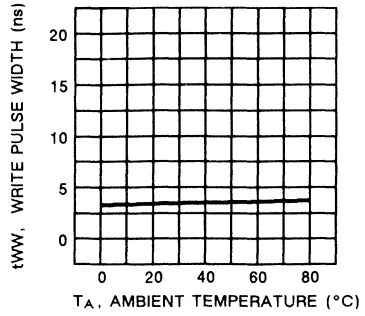
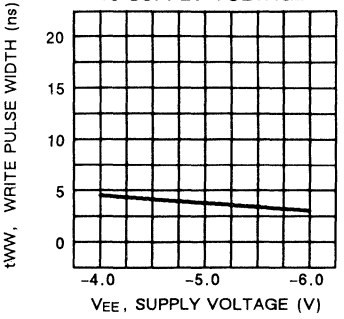


Fig. 14 – WITE PULSE WIDTH vs SUPPLY VOLTAGE

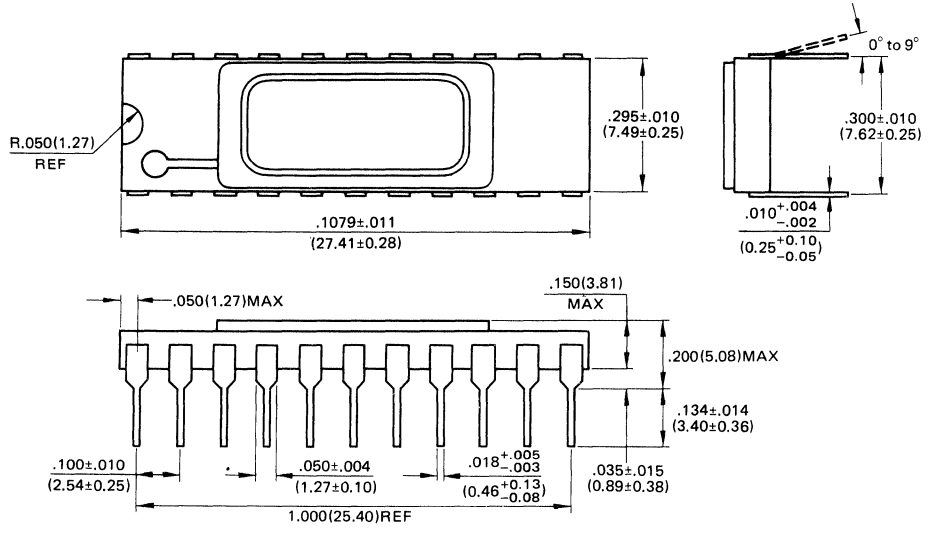


2

PACKAGE DIMENSIONS

(Suffix : -C)

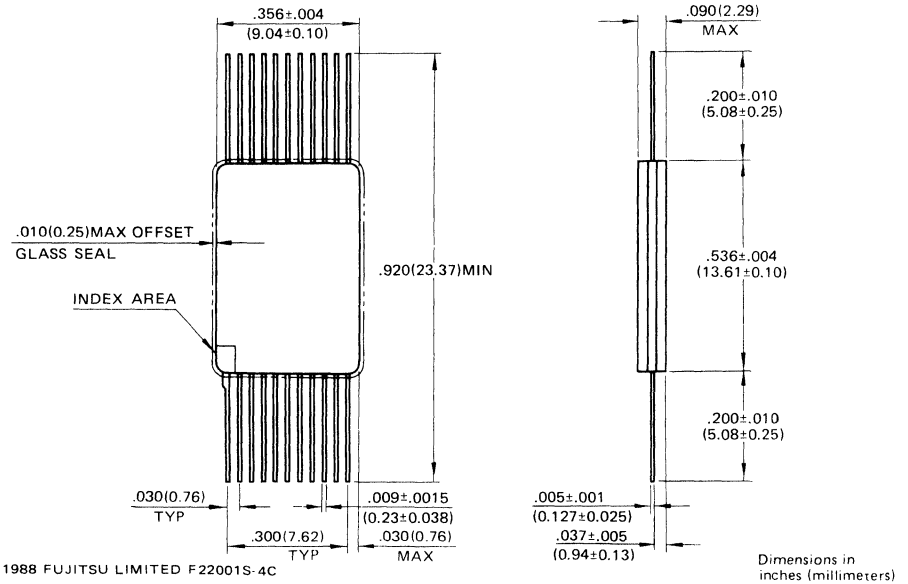
22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-22C-A02)



Dimensions in
inches (millimeters)

(Suffix : -ZF)

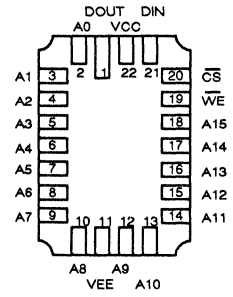
22-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-22C-C01)



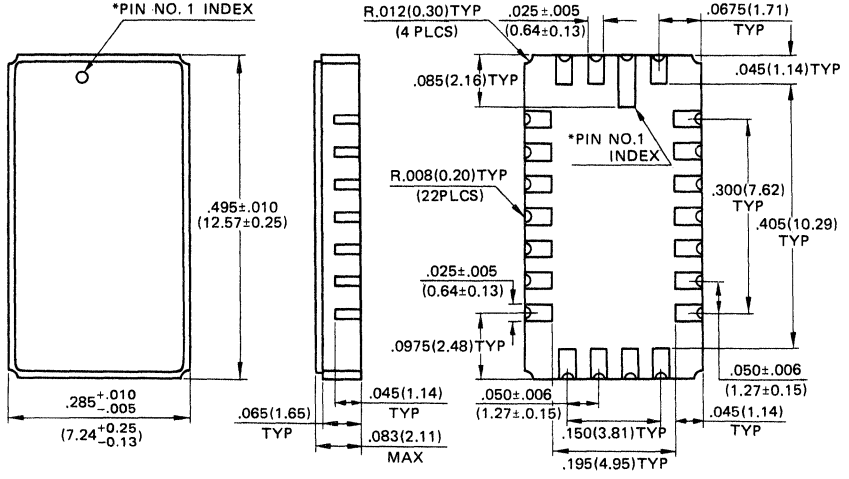
2

(Suffix : -CV)

PIN ASSIGNMENT



22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

October 1989
Edition 2.0

FUJITSU

DATA SHEET

MBM100C490-15

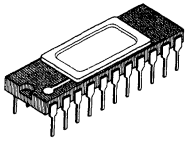
65536–BIT BICMOS ECL RANDOM ACCESS MEMORY

DESCRIPTION

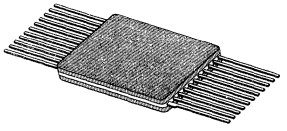
The Fujitsu MBM100C490 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on chip voltage/temperature compensation for improved noise margin.

Operation for the MBM100C490 is specified over an ambient temperature range of from 0°C to 85°C (T_A). It is packaged in 22–pin ceramic DIP, Flatpackage or LCC and is fully compatible with industory standard 100K series ECL families.

- 65536 words by 1 bit organization
- On–chip voltage/temperatuere compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Address access time : 15ns
- Chip select access time : 15ns
- Power dissipation : 540mW max (at minimum cycle)
- Open emitter output for ease of memory expansion
- BICMOS processing



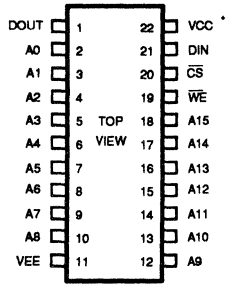
CERAMIC PACKAGE
DIP–22C–A02



CERAMIC PACKAGE
FPT–22C–C01

LCC–22C–A01 : See page 10

PIN ASSIGNMENT



* VCC grounded

LCC PAD configuration : See page 10

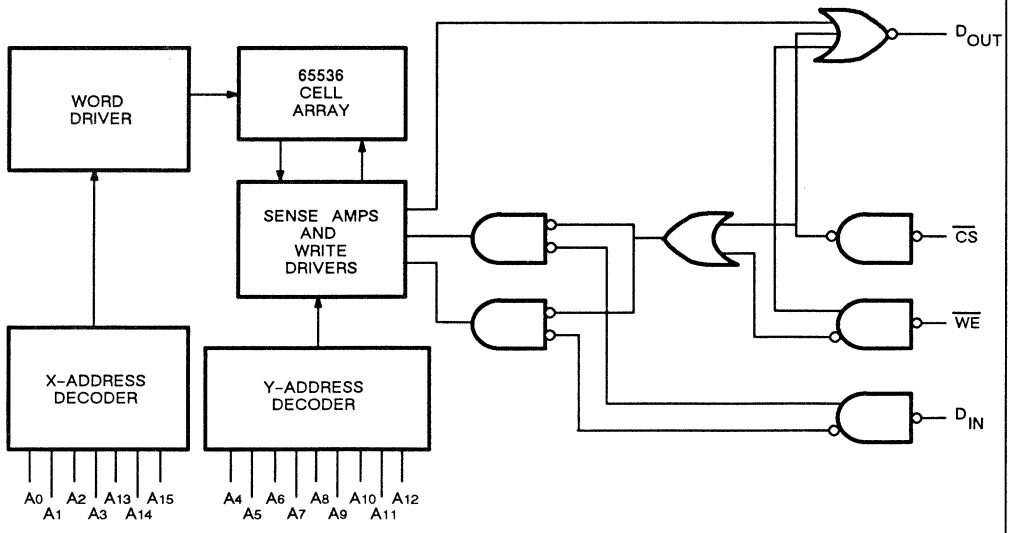
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MBM100C490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{IN}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100C490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by 1 bit. Memory cell selection is achieved by means of a 16-bit addresses designed A_0 through A_{15}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limit over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(Vcc = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TA = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-120			mA

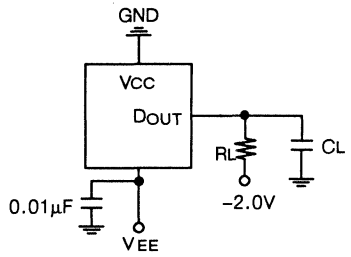
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	2.0		6.0	pF
Output Pin Capacitance	C_{OUT}	2.0		6.0	pF

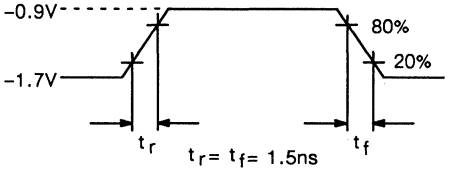
AC CHARACTERISTICS

(VCC = 0V, VEE = −4.5V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, TA = 0°C to 85°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



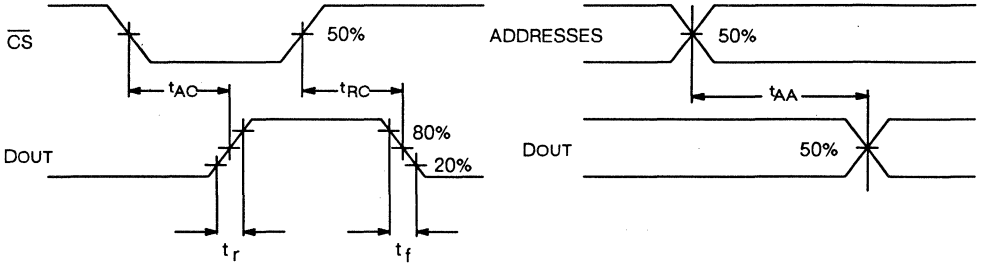
Note : All timing measurements referenced to 50% input levels.

2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	3.0		15.0	ns
Chip Select Access Time	t_{AC}	1.0		15.0	ns
Chip Select Recovery Time	t_{RC}	1.0		10.0	ns

Fig. 3 – READ CYCLE TIMING DIAGRAM

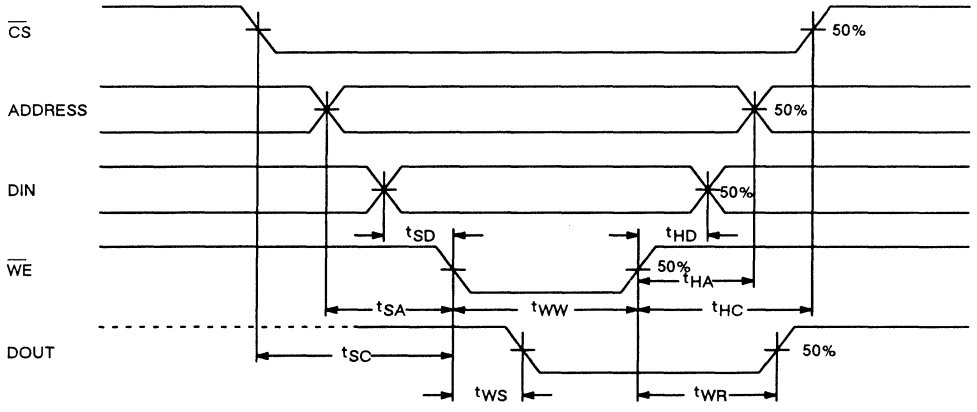


WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}	1.0		10.0	ns
Write Recovery Time	t_{WR}	1.0		18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

2

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	0.5		3.0	ns
Output Fall Time	t_f	0.5		3.0	ns

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

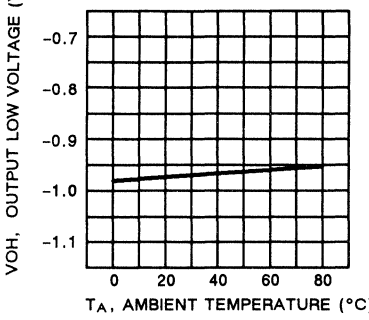


Fig. 6 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

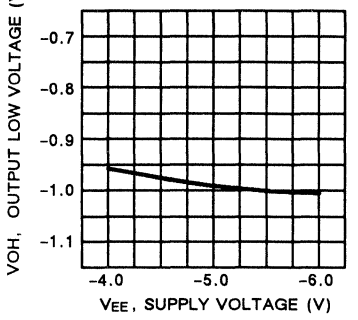


Fig. 7 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

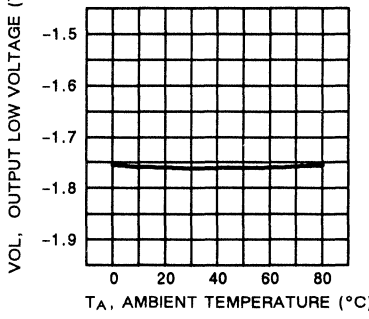


Fig. 8 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

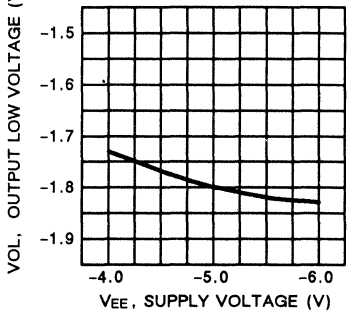


Fig. 9 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

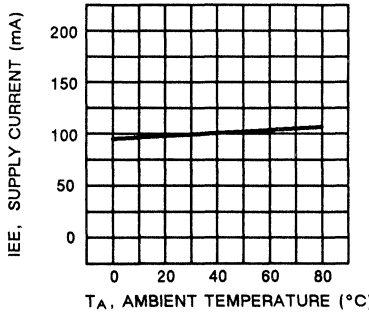


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

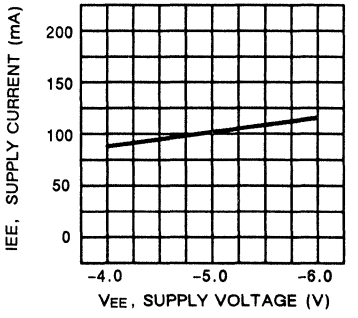


Fig. 11 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

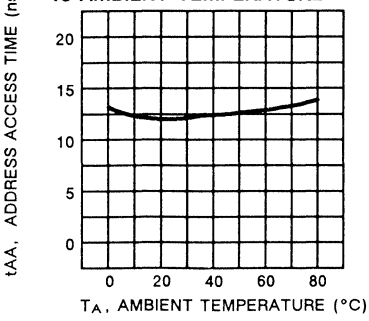


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

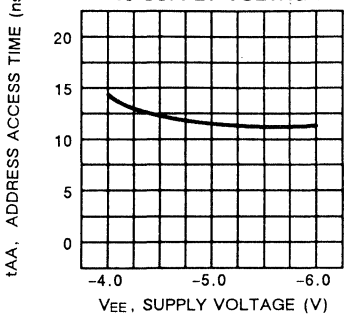


Fig. 13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

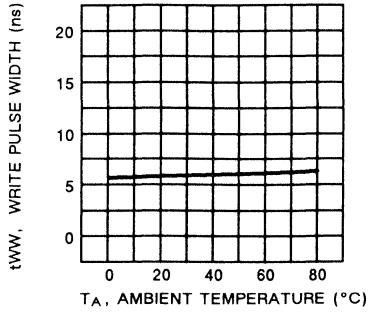
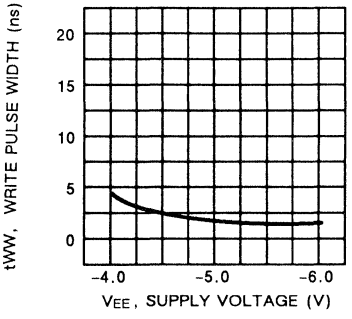


Fig. 14 – WITE PULSE WIDTH vs SUPPLY VOLTAGE



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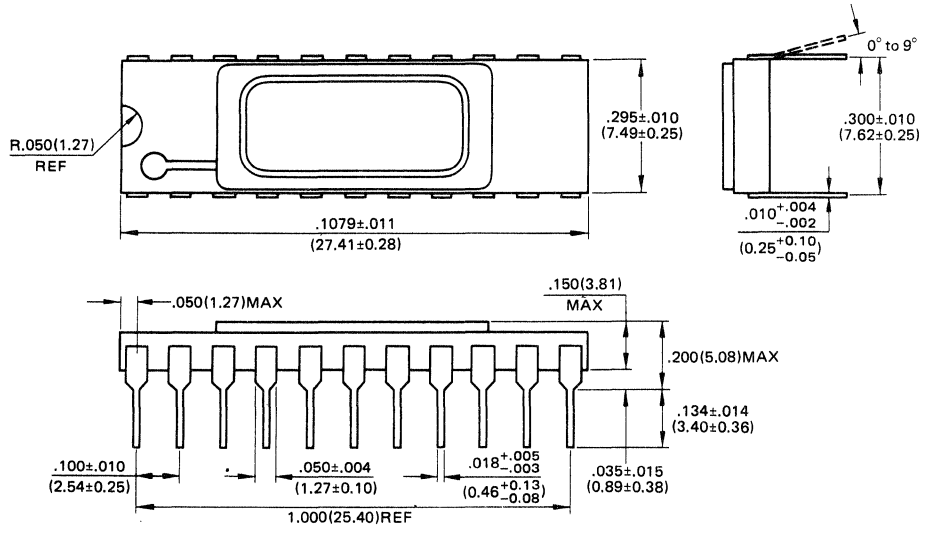
PACKAGE DIMENSIONS

(Suffix : -C)

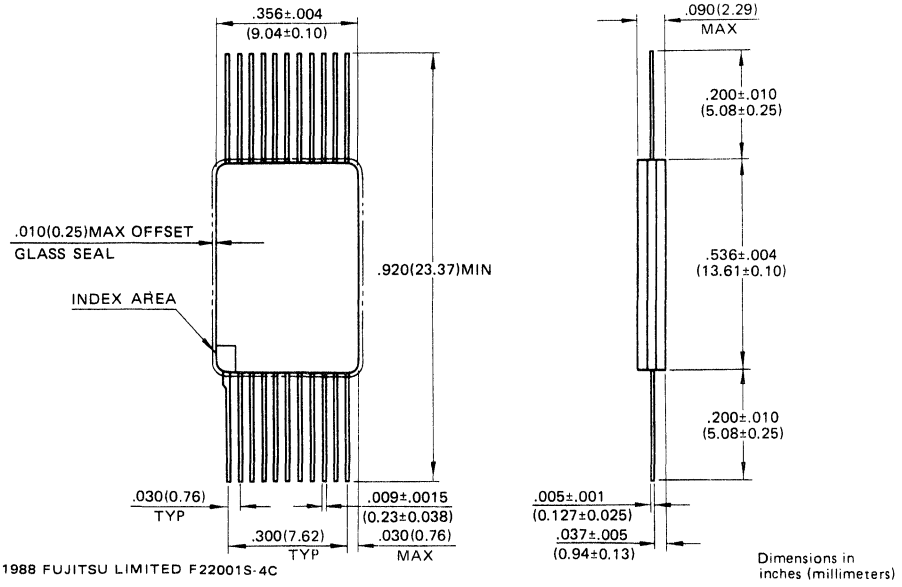
22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-22C-A02)



Dimensions in
inches (millimeters)

(Suffix : -ZF)

22-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-22C-C01)

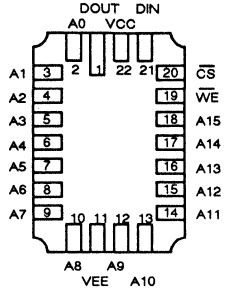


Dimensions in
inches (millimeters)

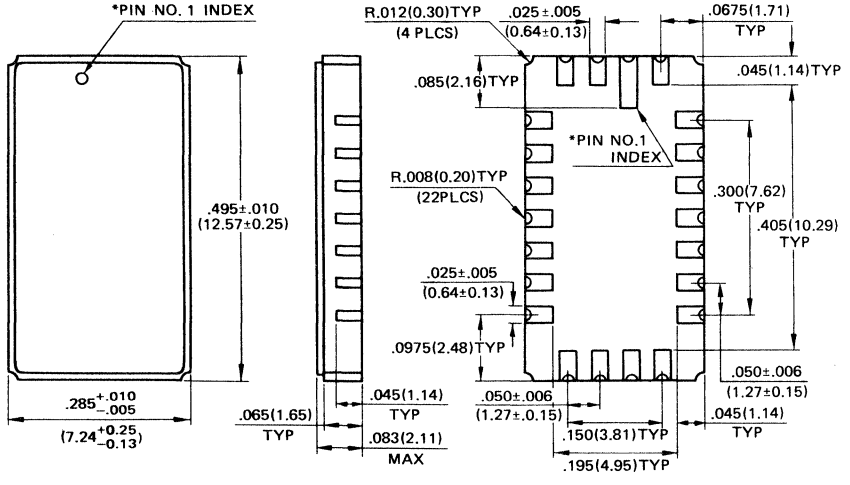
2

(Suffix : -CV)

PIN ASSIGNMENT



22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

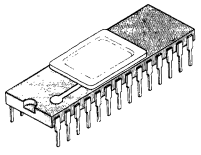
MBM10C494-15

65536–BIT BICMOS ECL RANDOM ACCESS MEMORY

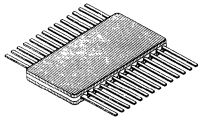
DESCRIPTION

The Fujitsu MBM10C494 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by 4 bits, and it features on chip voltage compensation for improved noise margin.

Operation for the MBM10C494 is specified over an ambient temperature range of from 0°C to 75°C (T_A). It is packaged in 28–pin ceramic DIP or Flatpackage, and is fully compatible with industory standard 10K series ECL families.



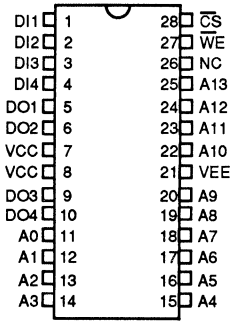
DIP–28C–A06



FPT–28C–C03

- 16384 words by 4 bits organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Address access time : 15ns
- Chip select access time : 15ns
- Power dissipation : 936mW max (at minimum cycle)
- Open emitter output for ease of memory expansion
- BICMOS processing

PIN ASSIGNMENT (TOP VIEW)



* V_{CC} grounded

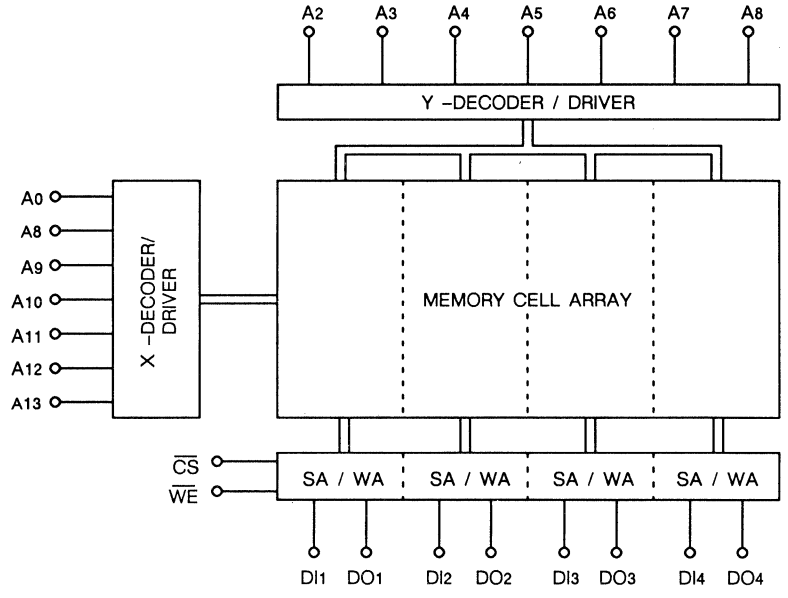
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 – MBM10C494 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10C494 is fully decoded 65536 bit read/write random access memory organized as 16384 words by 4 bits. Memory cell selection is achieved by means of a 14-bit address designed A0 through A13. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (VIN = VILmin)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-180			mA	0°C to 75°C

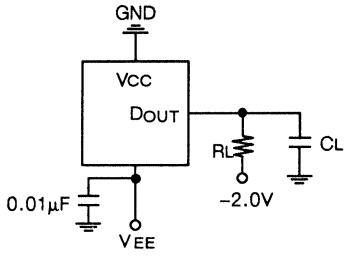
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	2.0		6.0	pF
Output Pin Capacitance	C_{OUT}	2.0		6.0	pF

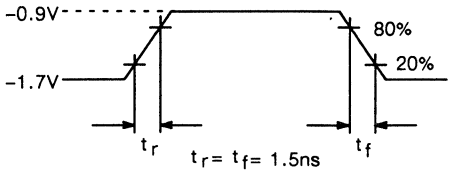
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



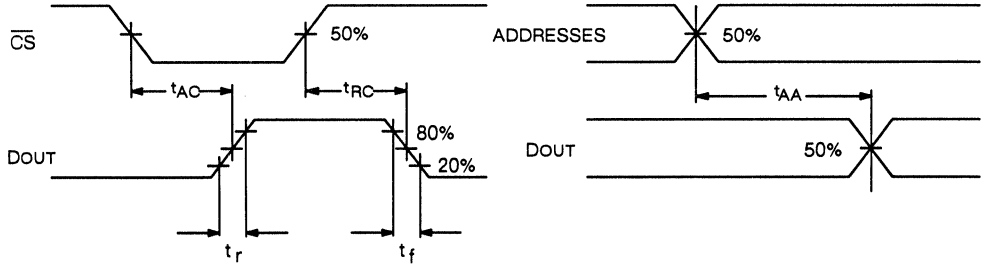
Note : All timing measurements referenced to 50% input levels.

2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	3.0		15.0	ns
Chip Select Access Time	t_{AC}	1.0		15.0	ns
Chip Select Recovery Time	t_{RC}	1.0		10.0	ns

Fig. 3 - READ CYCLE TIMING DIAGRAM

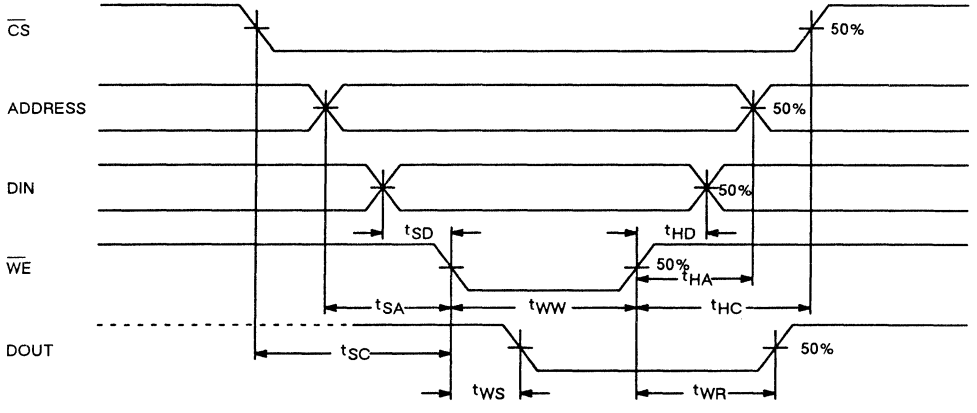


WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}	1.0		10.0	ns
Write Recovery Time	t_{WR}	1.0		18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

2

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	0.5		3.0	ns
Output Fall Time	t_f	0.5		3.0	ns

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

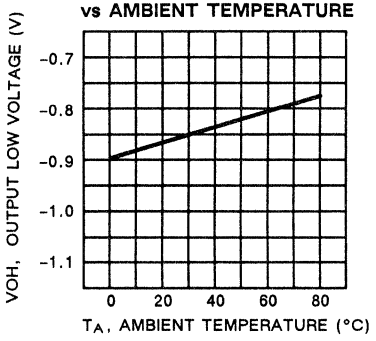


Fig. 6 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

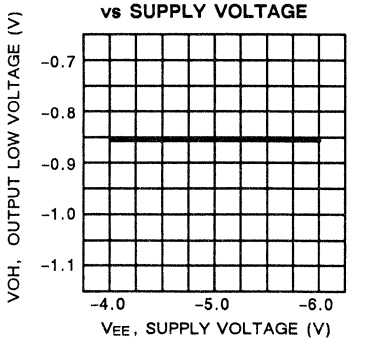


Fig. 7 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

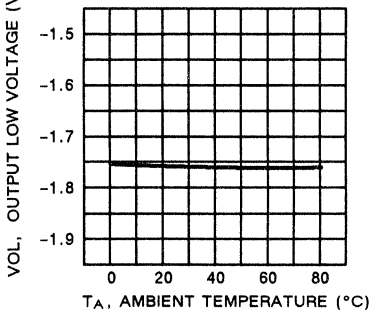


Fig. 8 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

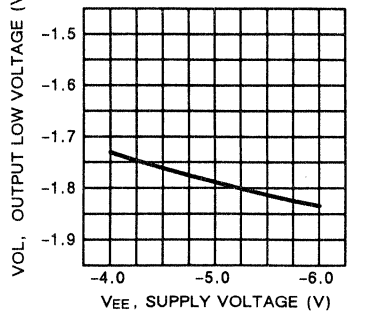


Fig. 9 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

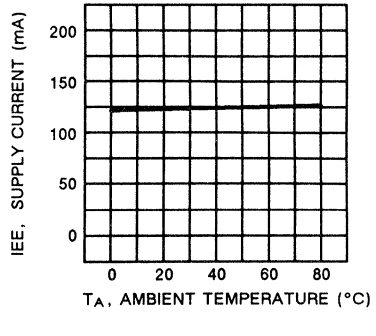


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

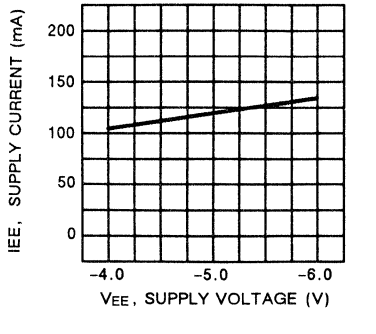


Fig. 11 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

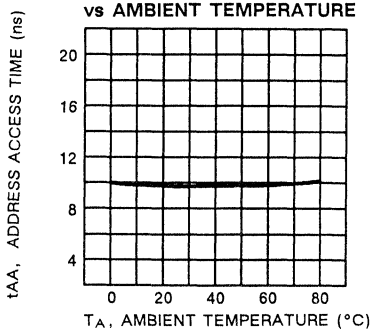


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

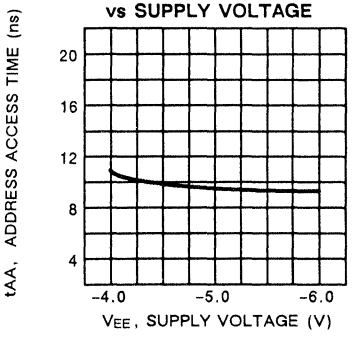


Fig. 13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

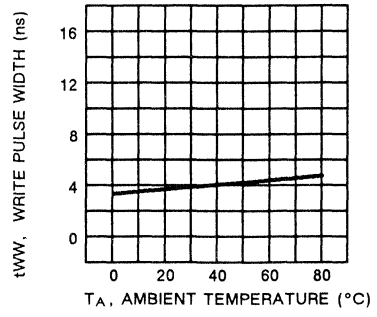
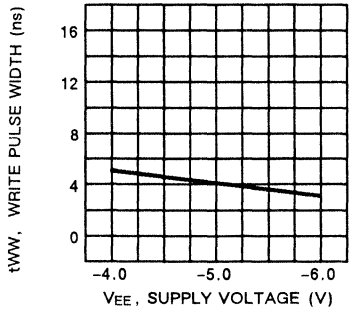


Fig. 14 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

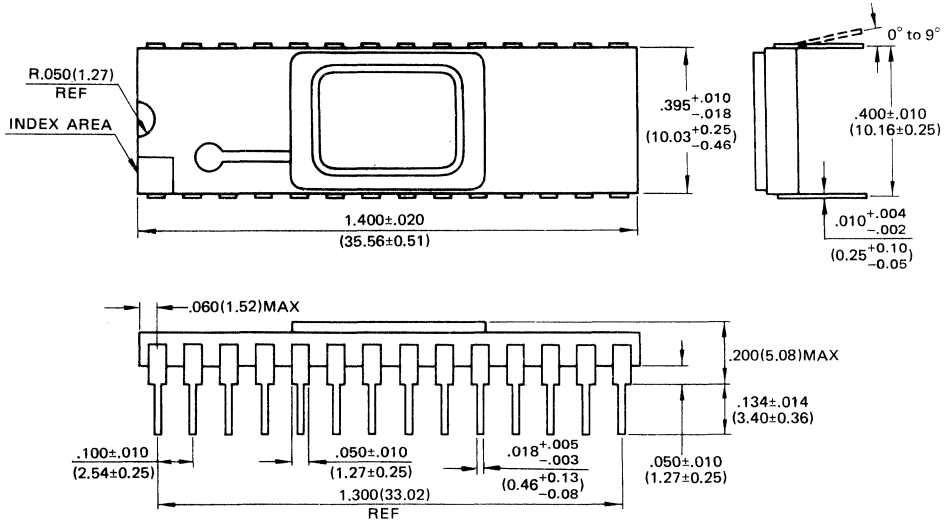


2

PACKAGE DIMENSIONS

(Suffix : -C)

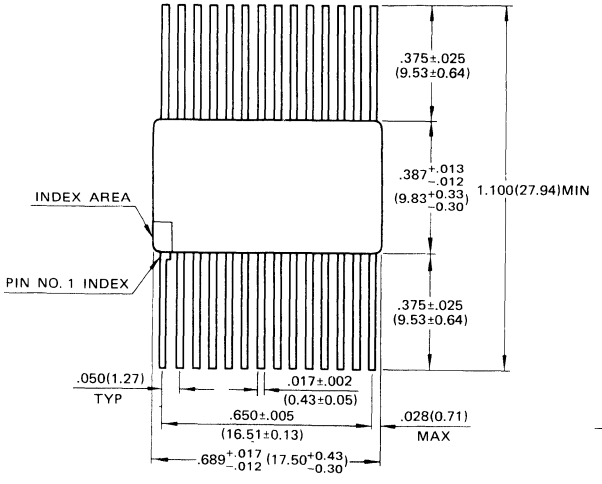
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

(Suffix : -ZF)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

2

October 1989
Edition 2.0

FUJITSU

DATA SHEET

MBM100C494-15

65536–BIT BICMOS ECL RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM100C494 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by 4 bits, and it features on chip voltage/temperature compensation for improved noise margin.

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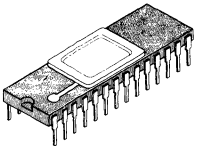
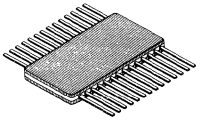


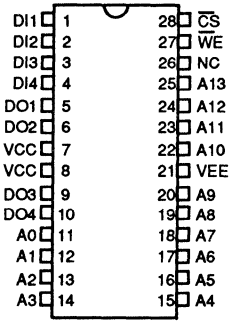
DIP–28C–A06



FPT–28C–C03

- 16384 words by 4 bits organization
- On–chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Address access time : 15ns
- Chip select access time : 15ns
- Power dissipation : 810mW max (at minimum cycle)
- Open emitter output for ease of memory expansion
- BICMOS processing

PIN ASSIGNMENT (TOP VIEW)



* VCC grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

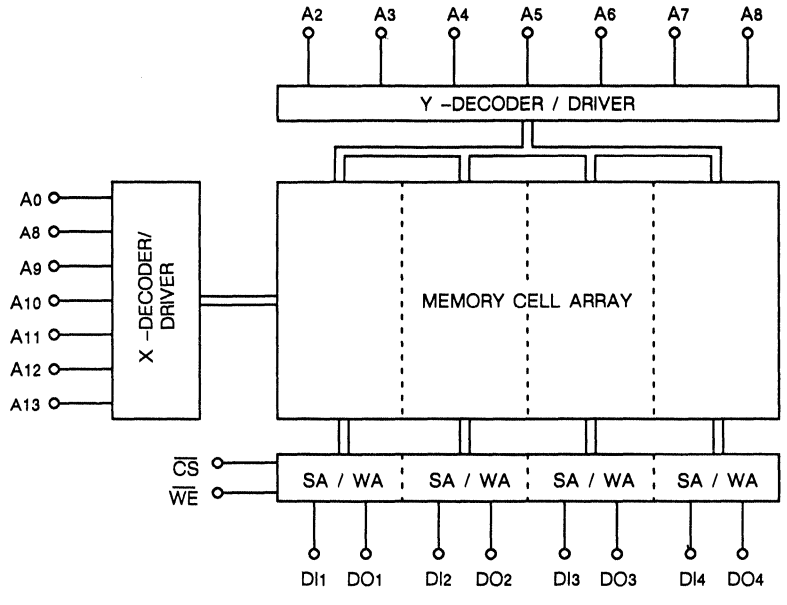
Parameter	Symbol	Value	Unit
VEE Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

2

Fig.1 - MBM100C494-15 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100C494 is fully decoded 65536 bit read/write random access memory organized as 16384 words by 4 bits. Memory cell selection is achieved by means of a 14-bit address designed A0 through A13. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limit over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TA = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-180			mA

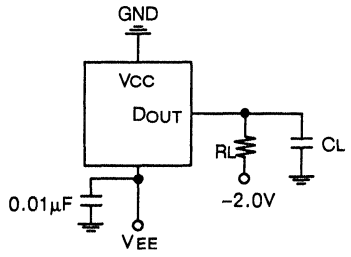
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	2.0		6.0	pF
Output Pin Capacitance	C_{OUT}	2.0		6.0	pF

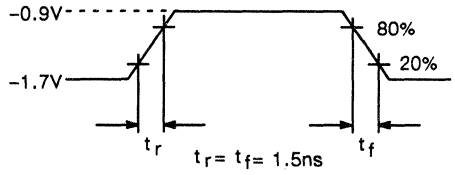
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TA = 0°C to 85°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



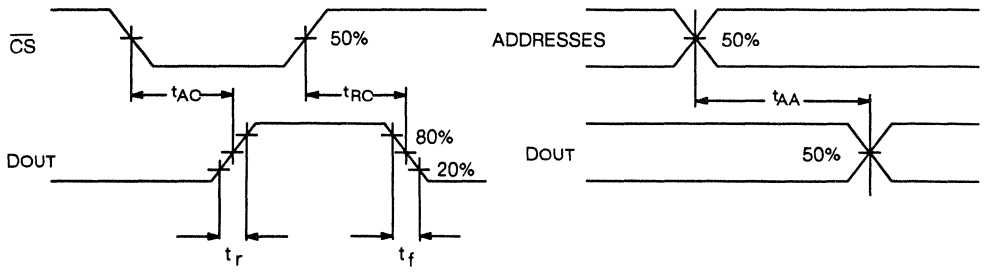
Note : All timing measurements referenced to 50% input levels.

2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	3.0		15.0	ns
Chip Select Access Time	t_{AC}	1.0		15.0	ns
Chip Select Recovery Time	t_{RC}	1.0		10.0	ns

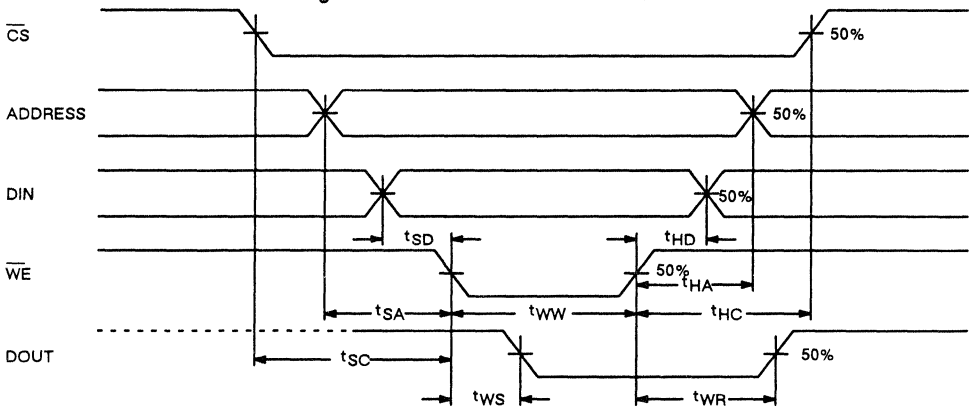
Fig. 3 – READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}	1.0		10.0	ns
Write Recovery Time	t_{WR}	1.0		18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	0.5		3.0	ns
Output Fall Time	t_f	0.5		3.0	ns

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

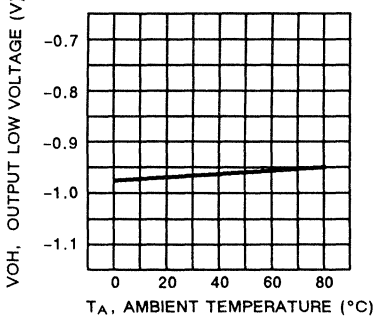


Fig. 6 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

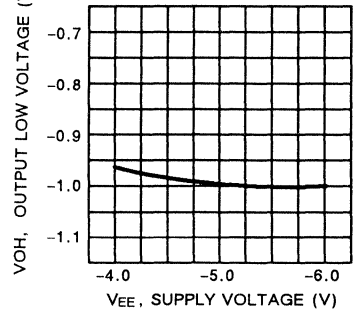


Fig. 7 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

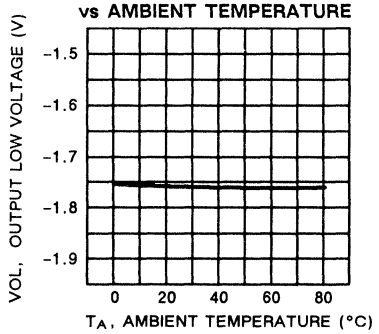


Fig. 8 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

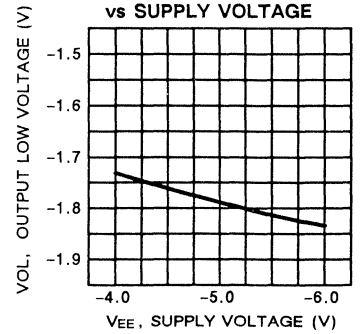


Fig. 9 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

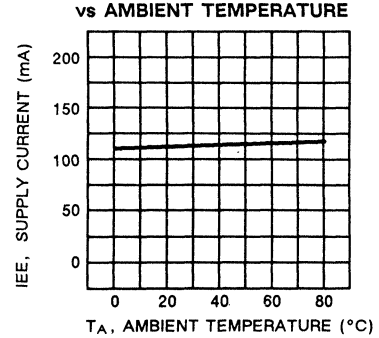


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

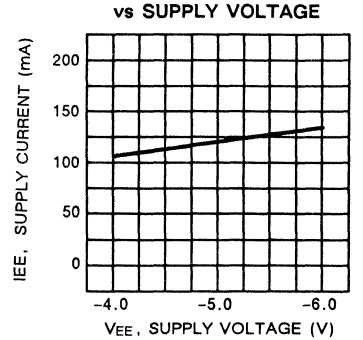


Fig. 11 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

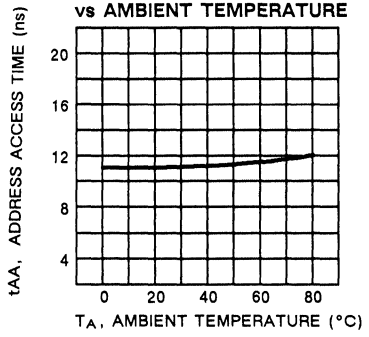


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

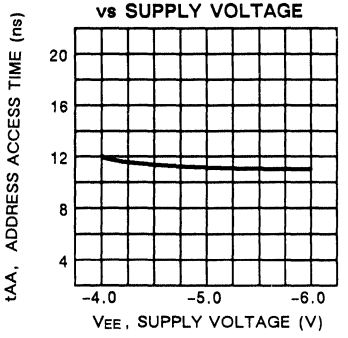


Fig. 13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

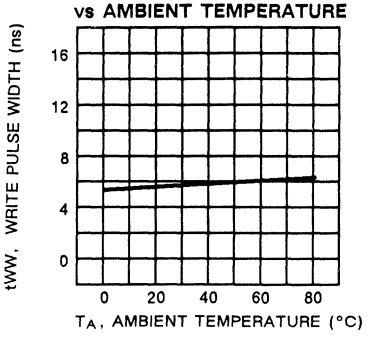
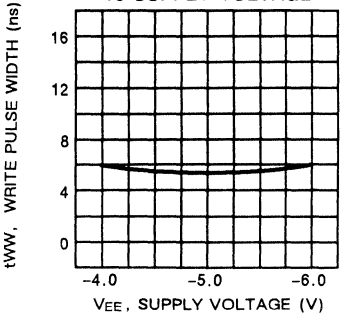


Fig. 14 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

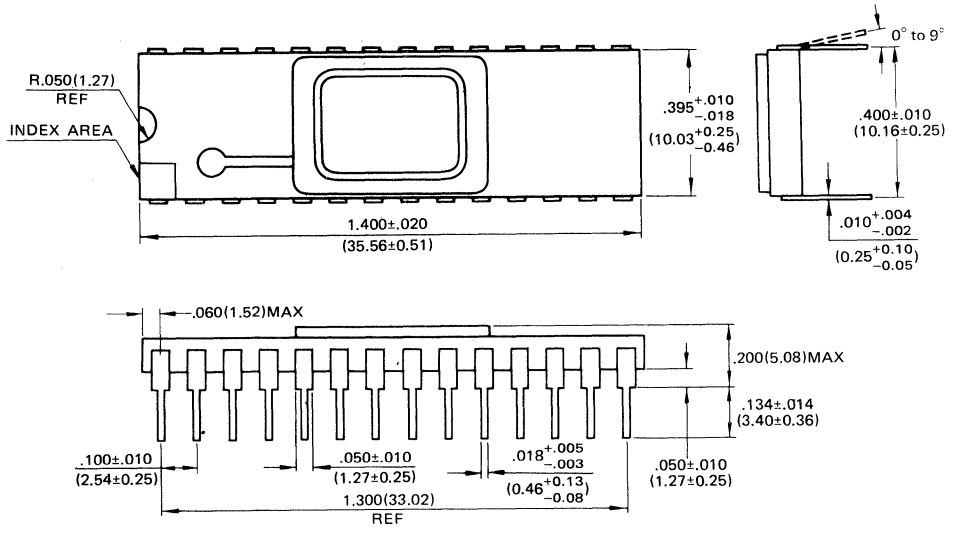


2

PACKAGE DIMENSIONS

(Suffix : -C)

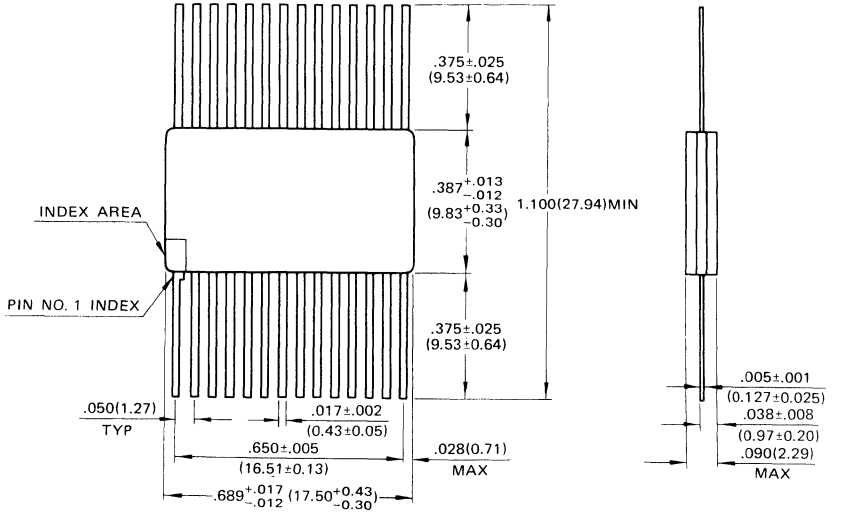
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

(Suffix : -ZF)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

2

October 1989
Edition 2.0

FUJITSU

DATA SHEET

MBM10C500-15

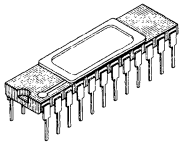
262144–BIT BICMOS ECL RANDOM ACCESS MEMORY

DESCRIPTION

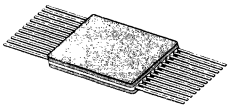
The Fujitsu MBM10C500 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 262144 words by one bit, and it features on chip voltage/temperature compensation for improved noise margin.

Operation for the MBM10C500 is specified over an ambient temperature range of from 0°C to 75°C (TA). It is packaged in 24–pin ceramic DIP, Flatpackage or LCC and is fully compatible with industory standard 10K series ECL families.

- 262144 words by 1 bit organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Address access time : 15ns
- Chip select access time : 15ns
- Power dissipation : 1040mW max (at minimum cycle)
- Open emitter output for ease of memory expansion
- BICMOS processing



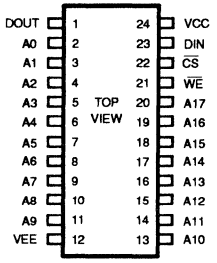
CERAMIC PACKAGE
DIP–24C–A09

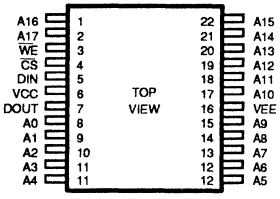


CERAMIC PACKAGE
FPT–24C–C04

LCC–24C–A02 : See page 10

PIN ASSIGNMENT





* VCC grounded

LCC PAD Configuration : See page 10

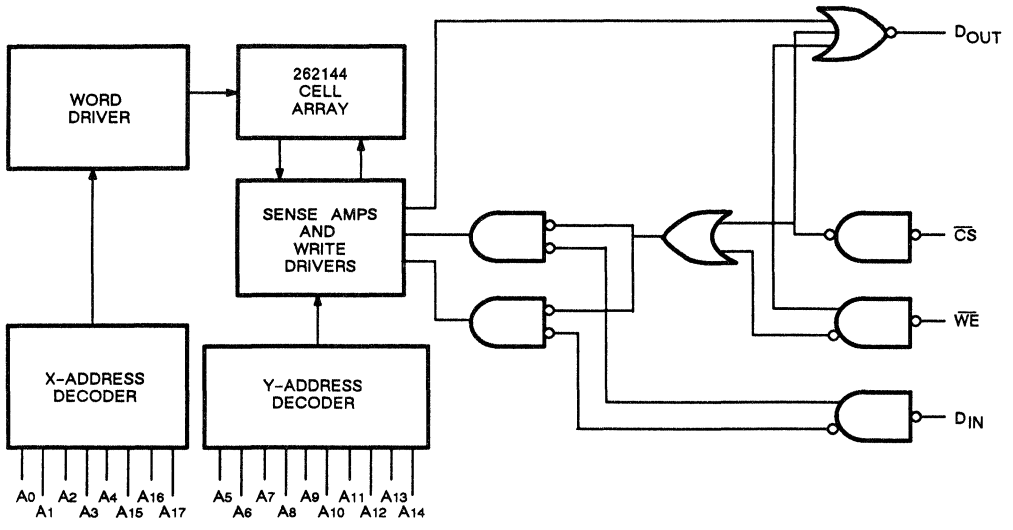
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 - MBM10C500-15 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{IN}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10C500 is fully decoded 262144 bit read/write random access memory organized as 262144 words by 1 bit. Memory cell selection is achieved by means of a 18-bit address designed A_0 through A_{17}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75

DC CHARACTERISTICS

(Vcc = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (VIN = VILmin)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-200			mA	0°C to 75°C

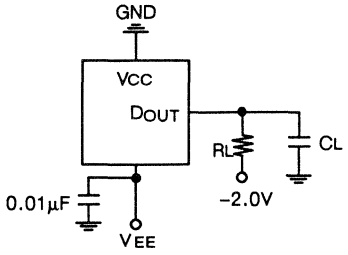
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	2.0		6.0	pF
Output Pin Capacitance	C_{OUT}	2.0		6.0	pF

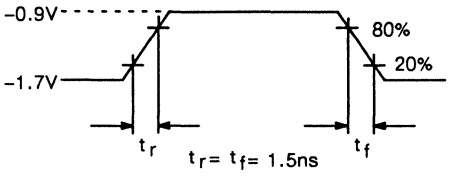
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

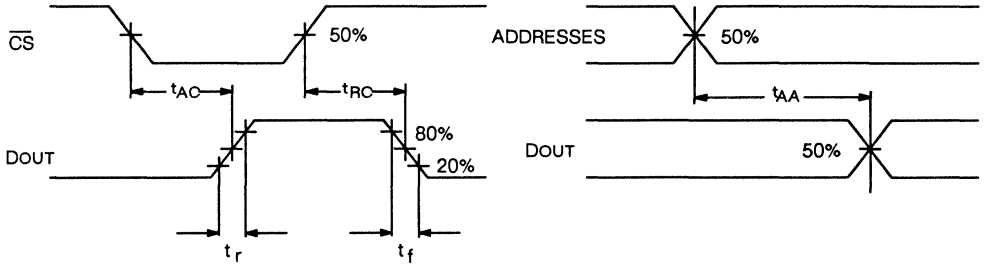


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	5.0		15.0	ns
Chip Select Access Time	t_{AC}	1.0		15.0	ns
Chip Select Recovery Time	t_{RC}	1.0		10.0	ns

Fig. 3 - READ CYCLE TIMING DIAGRAM

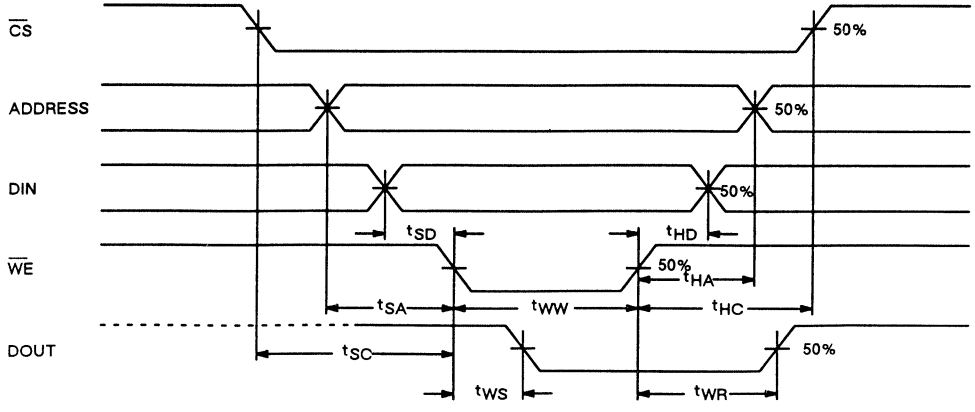


WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}	1.0		10.0	ns
Write Recovery Time	t_{WR}	1.0		18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

2

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	0.5		3.0	ns
Output Fall Time	t_f	0.5		3.0	ns

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

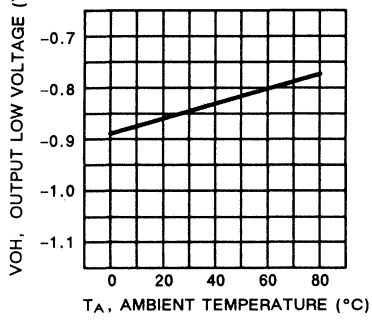


Fig. 6 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

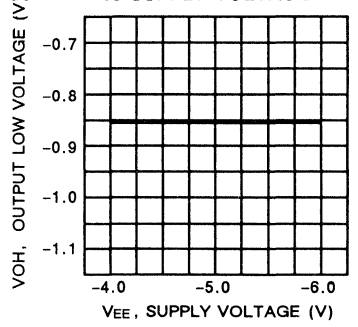


Fig. 7 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

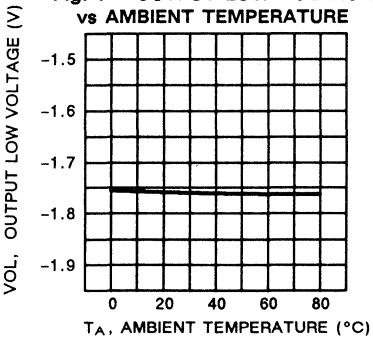


Fig. 8 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

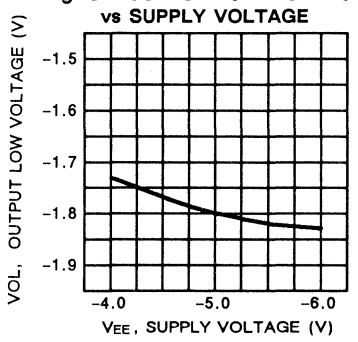


Fig. 9 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

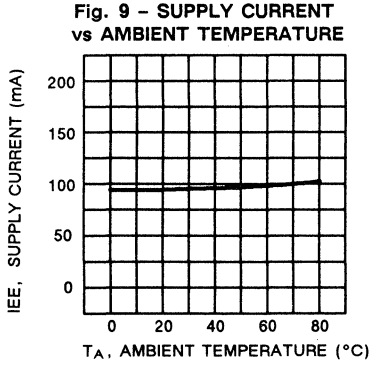


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

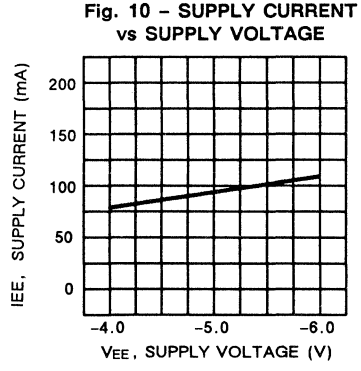


Fig. 11 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

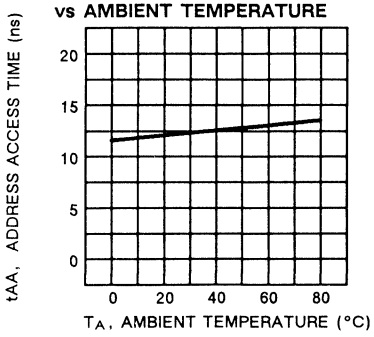


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

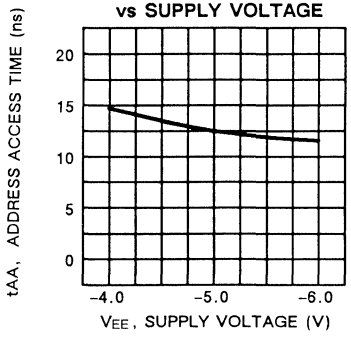


Fig. 13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

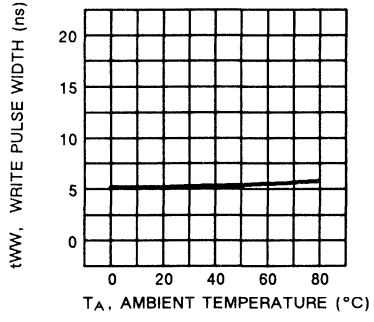
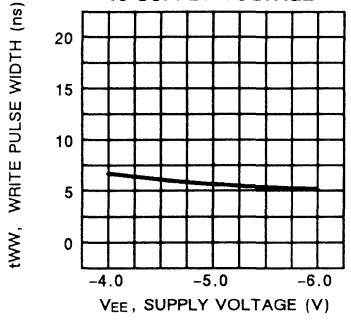


Fig. 14 – WITE PULSE WIDTH vs SUPPLY VOLTAGE

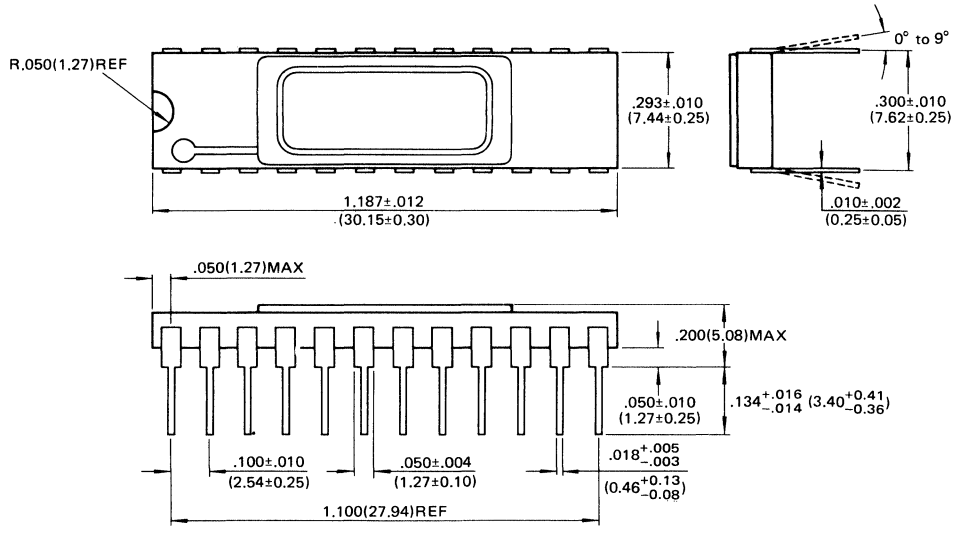


2

PACKAGE DIMENSIONS

(Suffix : -C)

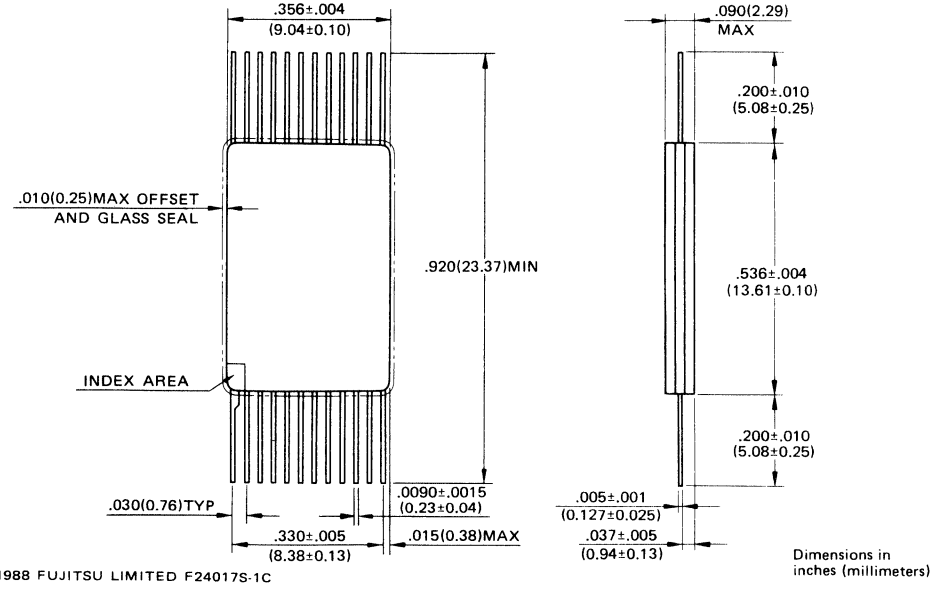
24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No. : DIP-24C-A09)



Dimensions in
inches (millimeters)

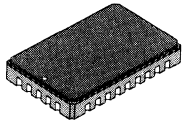
(Suffix : -ZF)

24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C04)

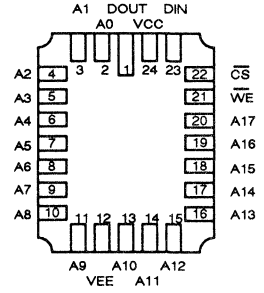


2

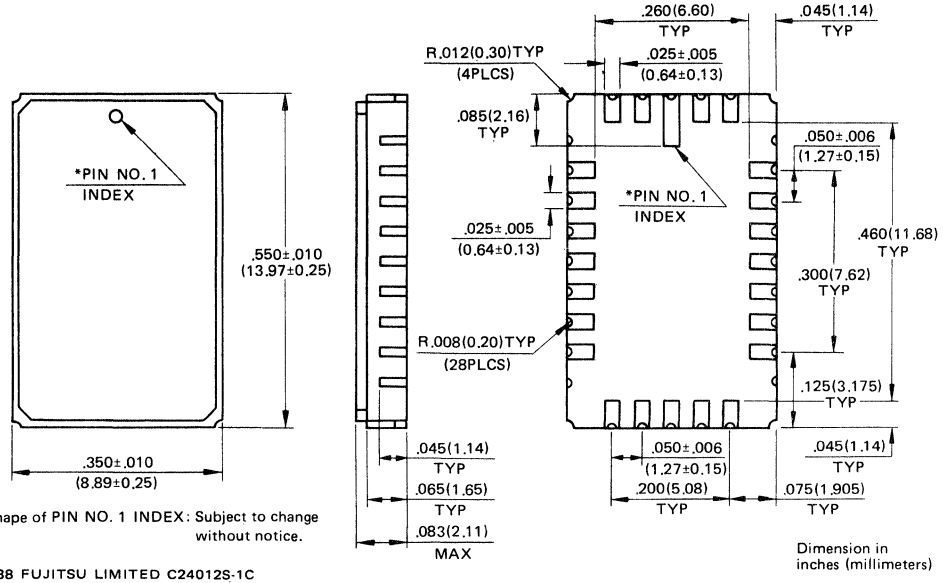
(Suffix : -CV)



PIN ASSIGNMENT



24-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

October 1989
Edition 2.0

FUJITSU

DATA SHEET

MBM100C500-15/-17

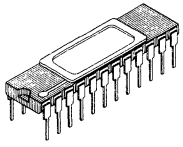
262144–BIT BICMOS ECL RANDOM ACCESS MEMORY

DESCRIPTION

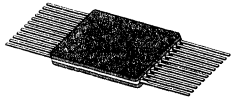
The Fujitsu MBM100C500 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 262144 words by one bit, and it features on chip voltage/temperature compensation for improved noise margin.

Operation for the MBM100C500 is specified over an ambient temperature range of from 0°C to 75°C (T_A). It is packaged in 24–pin ceramic DIP, Flatpackage or LCC and fully compatible with industory standard 100K series ECL families.

- 262144 words by 1 bit organization
- On–chip voltage / temperatuere compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Address access time : 15ns (MBM100C500–15)
  17ns (MBM100C500–17)
- Chip select access time : 15ns
- Power dissipation : 900mW max (at minimum cycle)
- Open emitter output for ease of memory expansion
- BICMOS processing



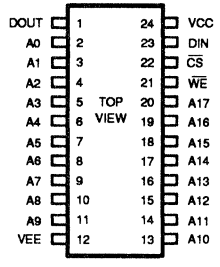
CERAMIC PACKAGE
DIP–24C–A09

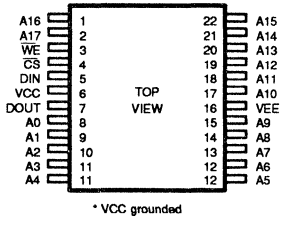


CERAMIC PACKAGE
FPT–24C–C04

LCC–24C–A02 : See page 10

PIN ASSIGNMENT





* VCC grounded

LCC PAD Configuration : See page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

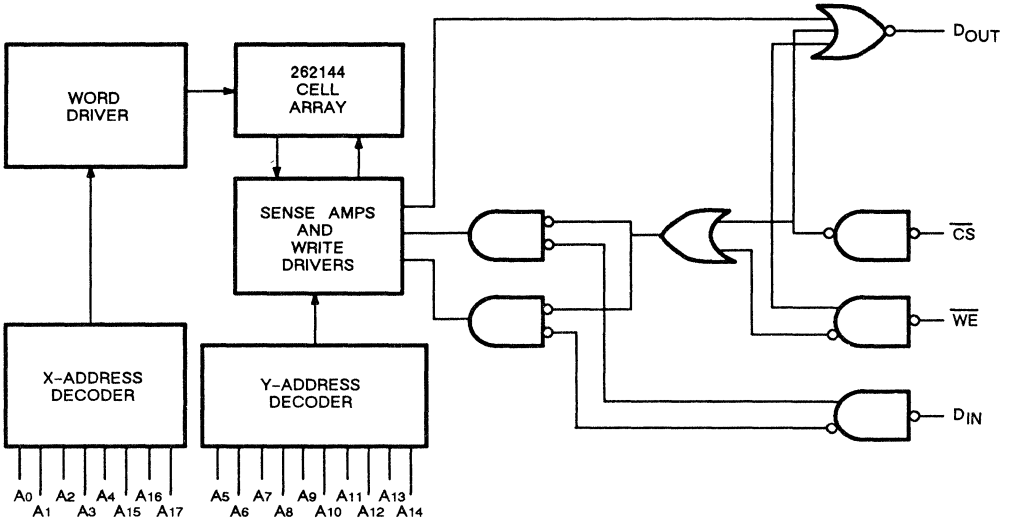
Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

2

Fig. 1 – MBM100C500 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{IN}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100C500 is fully decoded 262144 bit read/write random access memory organized as 262144 words by 1 bit. Memory cell selection is achieved by means of a 18-bit address designed A_0 through A_{17}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 75°C

*Guaranteed Operating Conditions define those limit over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V, T_A = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-200			mA

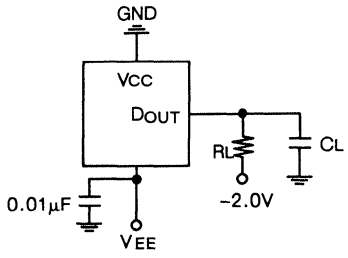
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	2.0		6.0	pF
Output Pin Capacitance	C_{OUT}	2.0		6.0	pF

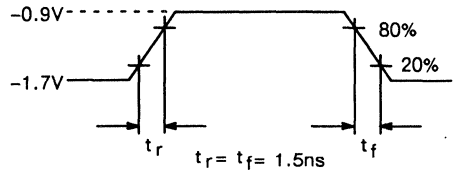
AC CHARACTERISTICS

(VCC = 0V, VEE = −4.5V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, TA = 0°C to 75°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

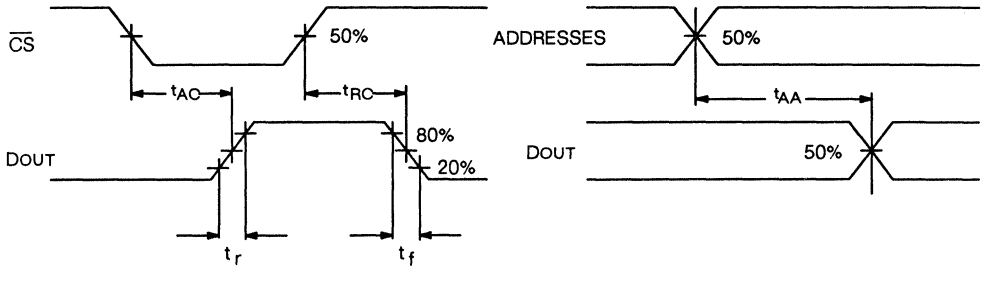


Note : All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM100C500-15			MBM100C500-17			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	5.0		15.0	5.0		17.0	ns
Chip Select Access Time	t_{AC}	1.0		15.0	1.0		15.0	ns
Chip Select Recovery Time	t_{RC}	1.0		10.0	1.0		10.0	ns

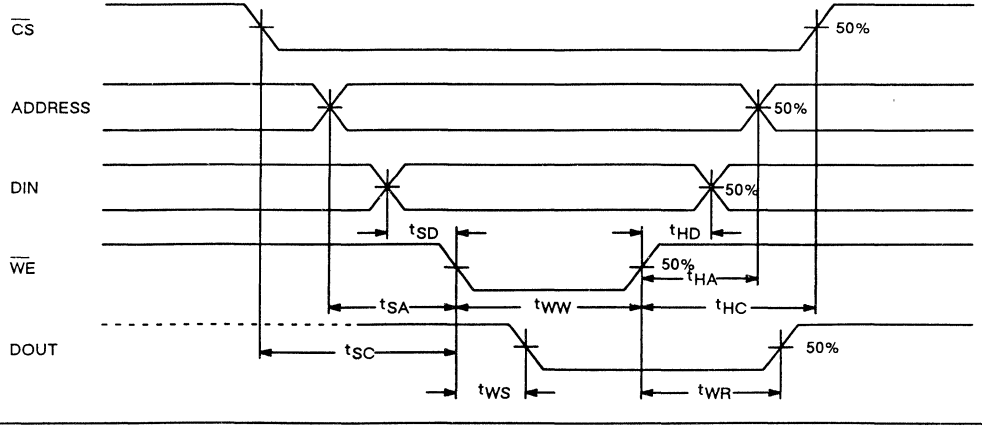
Fig. 3 – READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	MBM100C500-15			MBM100C500-17			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	10.0			10.0			ns
Write Disable Time	t_{WS}	1.0		10.0			10.0	ns
Write Recovery Time	t_{WR}	1.0		18.0			20.0	ns
Address Set Up Time	t_{SA}	2.0			2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			2.0			ns
Data Set Up Time	t_{SD}	2.0			2.0			ns
Address Hold Time	t_{HA}	3.0			3.0			ns
Chip Select Hold Time	t_{HC}	3.0			3.0			ns
Data Hold Time	t_{HD}	3.0			3.0			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



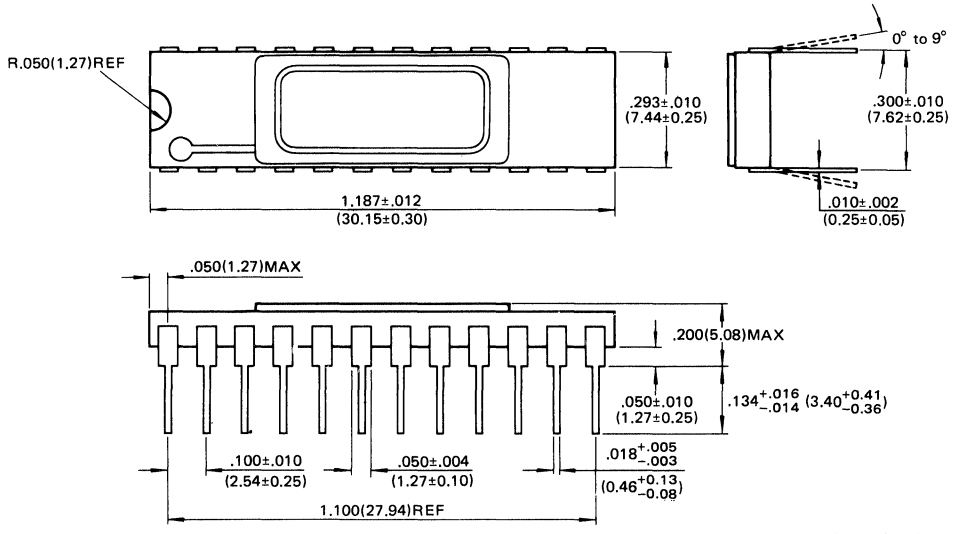
READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	0.5		3.0	ns
Output Fall Time	t_f	0.5		3.0	ns

PACKAGE DIMENSIONS

(Suffix : -C)

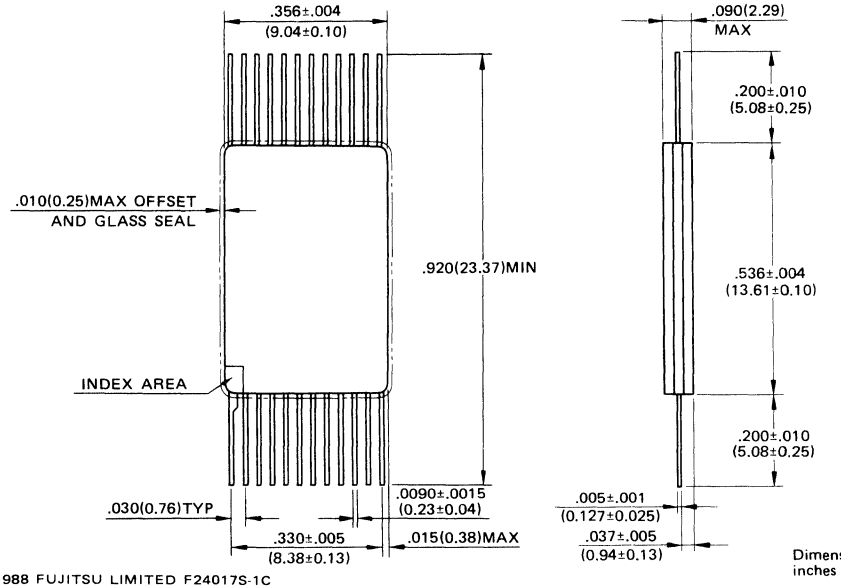
24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No. : DIP-24C-A09)



Dimensions in
inches (millimeters)

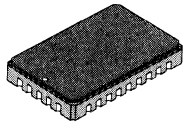
(Suffix : -ZF)

24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C04)

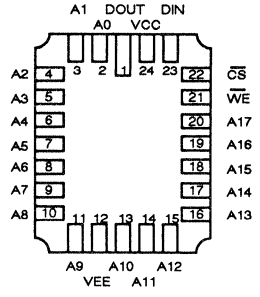


Dimensions in
inches (millimeters)

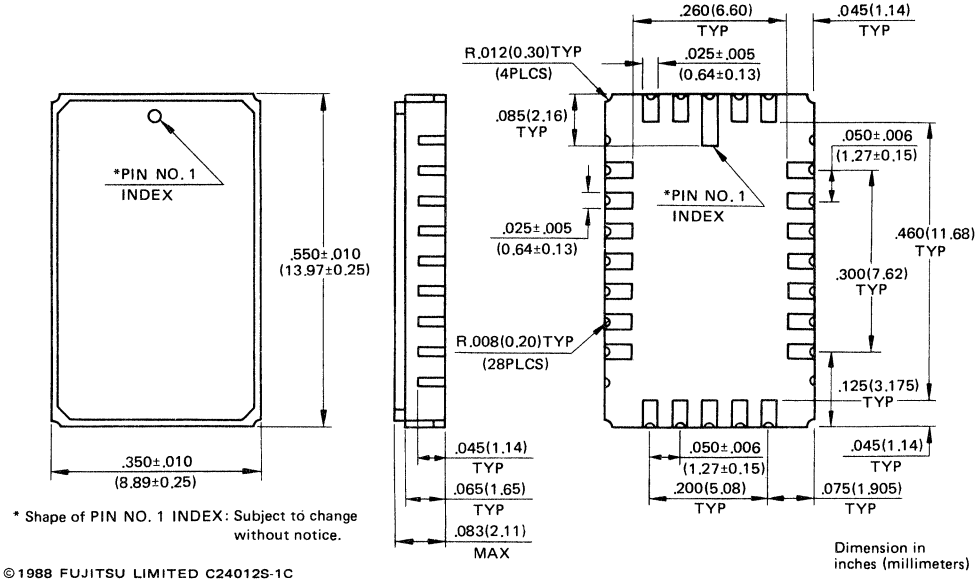
(Suffix : -CV)



PIN ASSIGNMENT



24-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MBM101C500-15

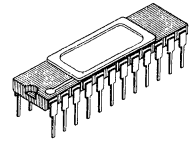
262144–BIT BICMOS ECL RANDOM ACCESS MEMORY

DESCRIPTION

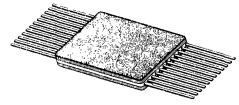
The Fujitsu MBM101C500 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 262144 words by one bit, and it features on chip voltage/temperature compensation for improved noise margin.

Operation for the MBM101C500 is specified over an ambient temperature range of from 0°C to 75°C (TA). It is packaged in 24–pin ceramic DIP, Flatpackage or LCC and is fully compatible with industory standard 100K series ECL families.

- 262144 words by 1 bit organization
- On–chip voltage/temperatuere compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Address access time : 15ns
- Chip select access time : 15ns
- Power dissipation : 1040mW max (at minimum cycle)
- Open emitter output for ease of memory expansion
- BICMOS processing



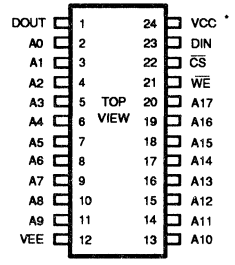
CERAMIC PACKAGE
DIP–24C–A09

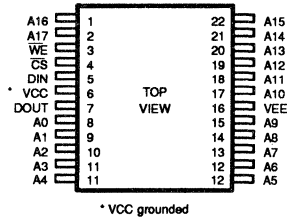


CERAMIC PACKAGE
FPT–24C–C04

LCC–24C–A02 : See page 10

PIN ASSIGNMENT





* VCC grounded

LCC PAD Configuration : See page 10

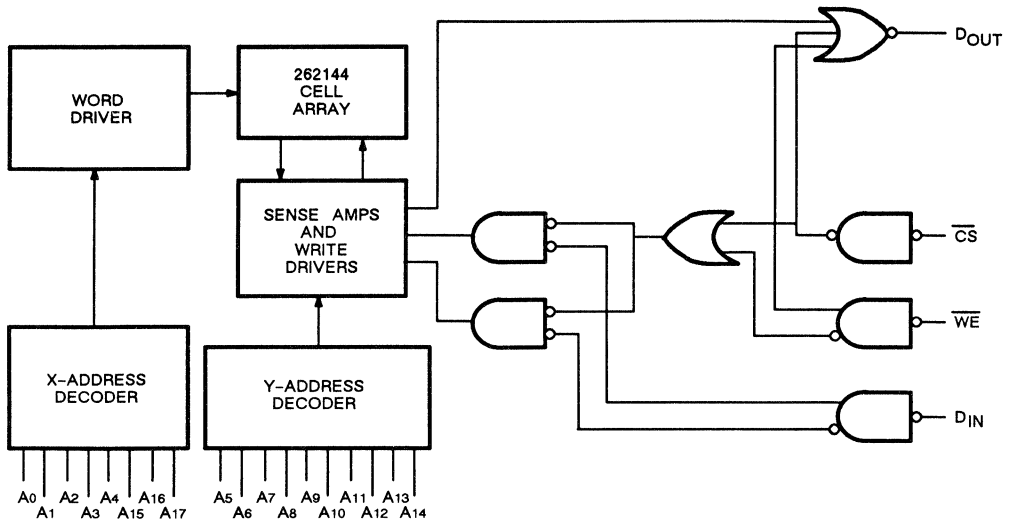
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
VEE Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Case Temperature under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig. 1 – MBM101C500 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{IN}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM101C500 is fully decoded 262144 bit read/write random access memory organized as 262144 words by 1 bit. Memory cell selection is achieved by means of a 18-bit address designed A0 through A17. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75

DC CHARACTERISTICS

(Vcc = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-200			mA

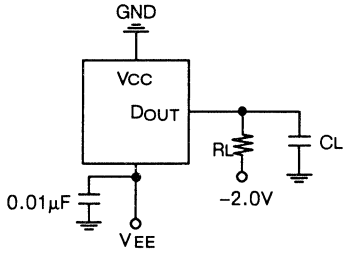
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	2.0		6.0	pF
Output Pin Capacitance	C_{OUT}	2.0		6.0	pF

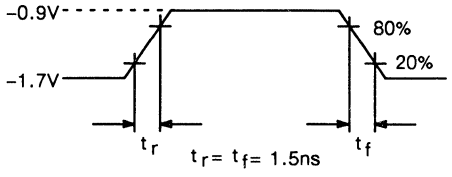
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



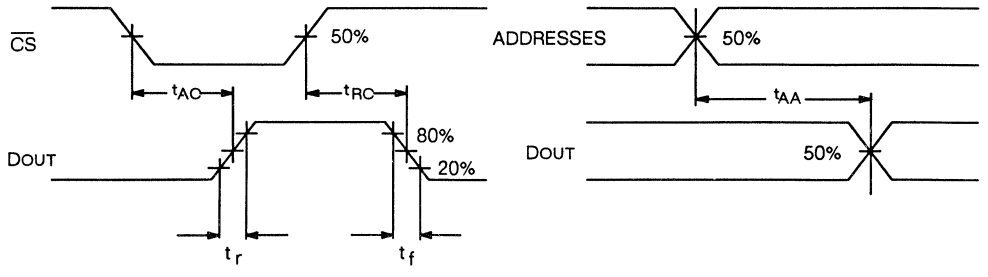
Note : All timing measurements referenced to 50% input levels.

2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	5.0		15.0	ns
Chip Select Access Time	t_{AC}	1.0		15.0	ns
Chip Select Recovery Time	t_{RC}	1.0		10.0	ns

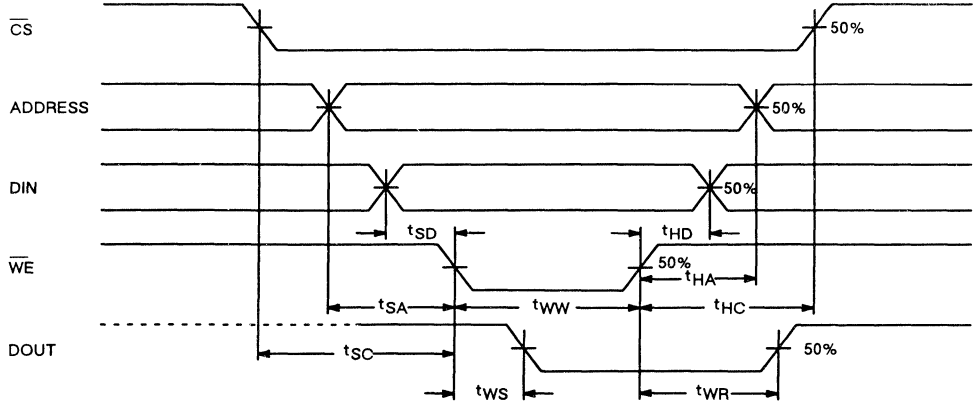
Fig. 3 - READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}	1.0		10.0	ns
Write Recovery Time	t_{WR}	1.0		18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

Fig. 4 – WRITE CYCLE TIMING DIAGRAM



READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	0.5		3.0	ns
Output Fall Time	t_f	0.5		3.0	ns

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

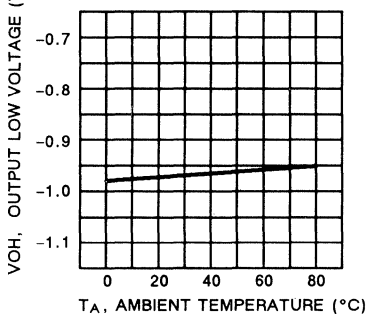


Fig. 6 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

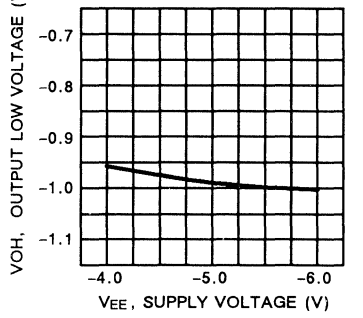


Fig. 7 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

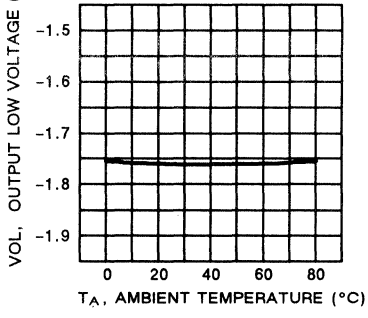


Fig. 8 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

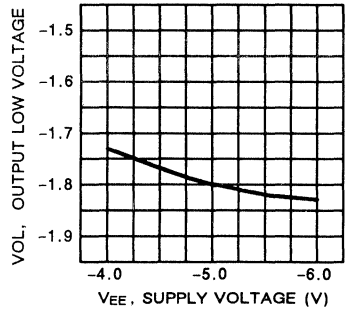


Fig. 9 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

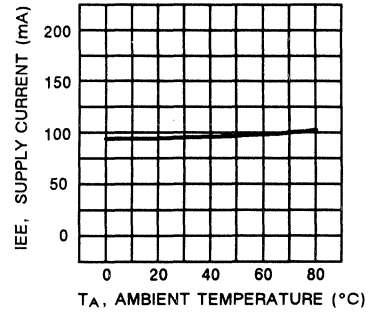


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

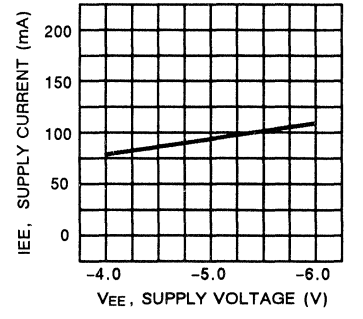


Fig. 11 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

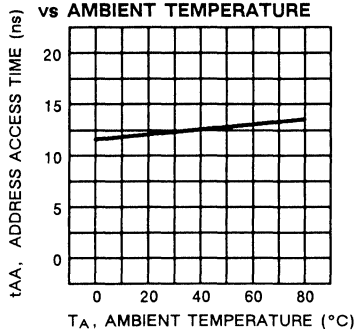


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

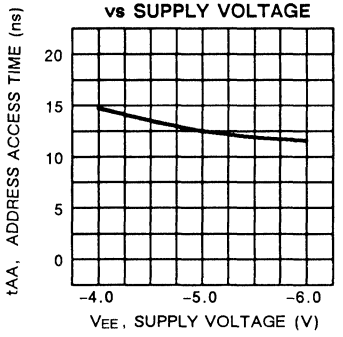


Fig. 13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

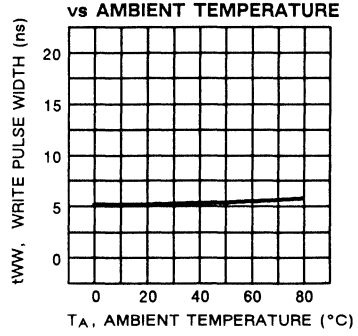
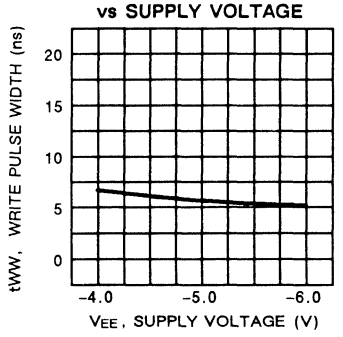


Fig. 14 – WITE PULSE WIDTH vs SUPPLY VOLTAGE

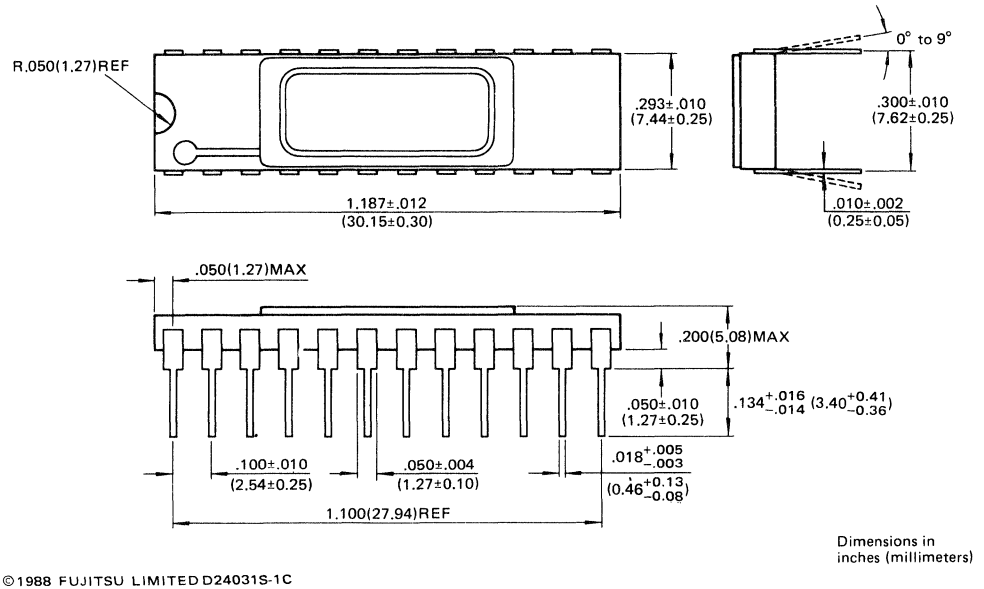


2

PACKAGE DIMENSIONS

(Suffix : -C)

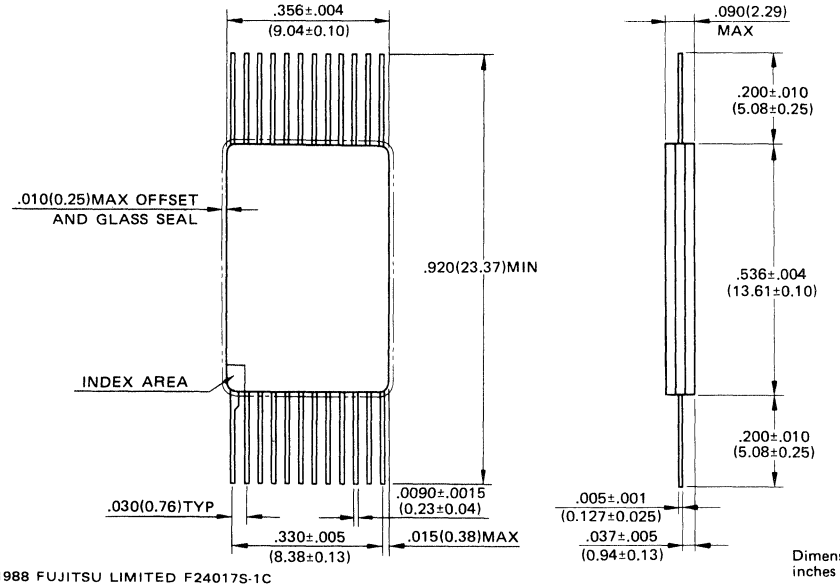
24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No. : DIP-24C-A09)



Dimensions in
inches (millimeters)

(Suffix : -ZF)

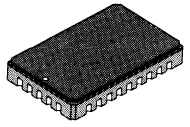
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C04)



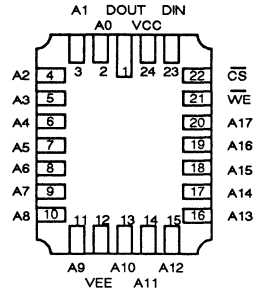
Dimensions in
inches (millimeters)

2

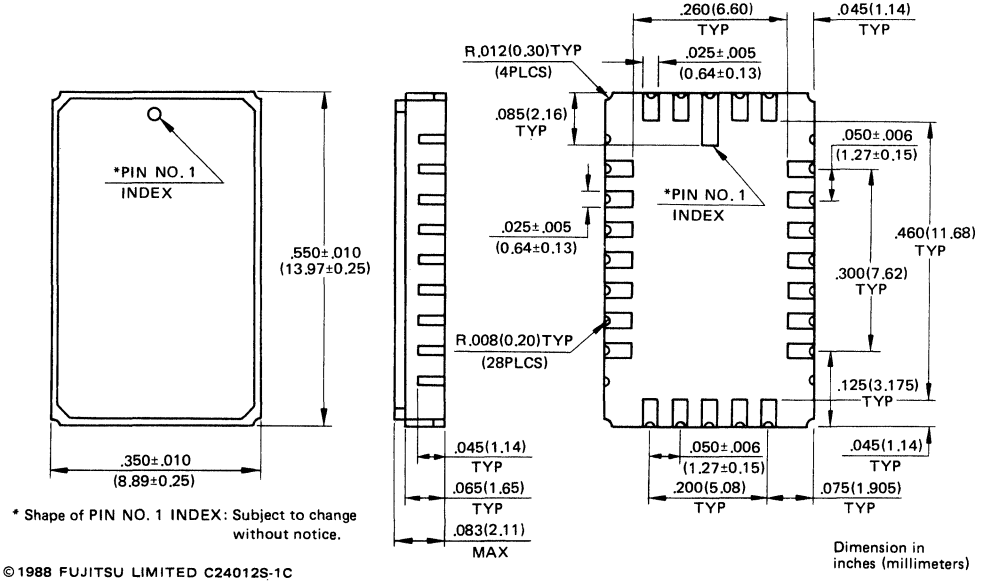
(Suffix : -CV)



PIN ASSIGNMENT



24-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

FUJITSU

BICMOS 262144-BIT ECL RANDOM ACCESS MEMORY

MBM100C504-15

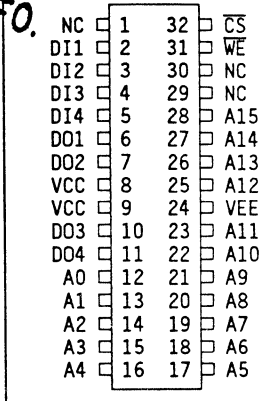
TS324-A888
August 1988

262144-BIT BICMOS ECL RANDOM ACCESS MEMORY ADVANCE INFO.

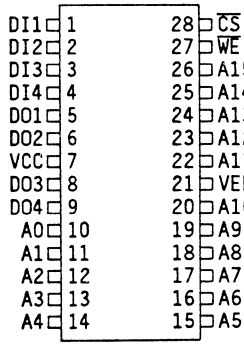
The Fujitsu MBM100C504 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by 4 bit, and it features on chip voltage/temperature compensation for improved noise margin. Operation for the MBM100C504 is specified over a temperature range of from 0°C to 85°C (TA for DIP and TC for FPT). It is packaged in 32-pin ceramic DIP and 28-pin ceramic FPT and fully compatible with industory standard 100K series ECL families.

- 65536 words x 4 organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standard 100K series ECL families
- Address access time: 15ns max
  Chip select access time: 15ns max
- Power dissipation: -220mA min
- Open emitter output for ease of memory expansion
- BICMOS Processing
- Package: 32-pin ceramic DIP (Suffix: C)
  28-pin ceramic FPT (Suffix: ZF)

Pin Assignments for DIP



Pin Assignments for FPT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

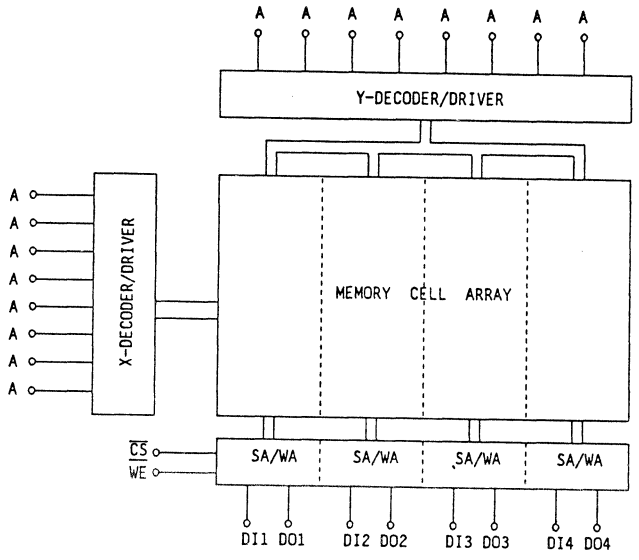
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFO.

Fig.1 - MBM100C504 BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

Notes:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100C504 is fully decoded 262144 bit read/write random access memory organized as 65536 words by 4 bit. Memory cell selection is achieve by means of a 16-bit address designated A0 through A15. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

ADVANCE INFO.

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient temperature(TA)
Supply Voltage	V_{EE}	-4.725	-4.5	-4.275	V	0°C to 85°C

DC CHARACTERISTICS
(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TA = 0°C to 85°C for DIP, Airfloe ≥ 2.5m/s, TC = 0°C to 85°C for Flat Package, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50		90	µA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Outputs Biased)	I_{EE}	-220			mA

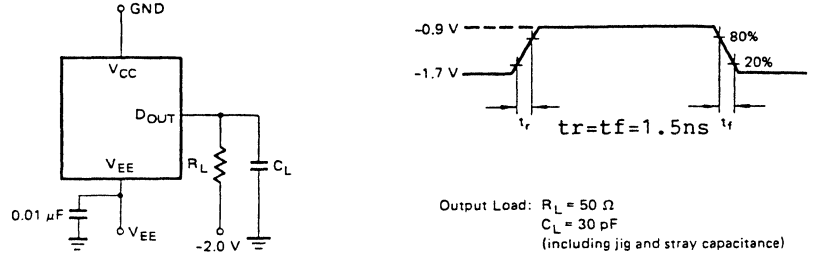
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		TBD		pF
Output Pin Capacitance	C_{OUT}		TBD		pF

ADVANCE INFO

AC CHARACTERISTICS
(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA=0°C to 85°C for DIP, Airflow ≥ 2.5 m/s, TC=0°C to 85°C for Flat Package, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



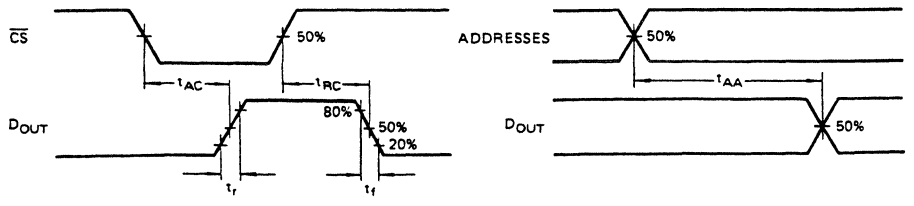
NOTE: All timing measurements referenced to 50% input levels.

2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15.0	ns
Chip Select Access Time	t_{AC}			15.0	ns
Chip Select Recovery Time	t_{RC}			10.0	ns

READ CYCLE TIMING DIAGRAM

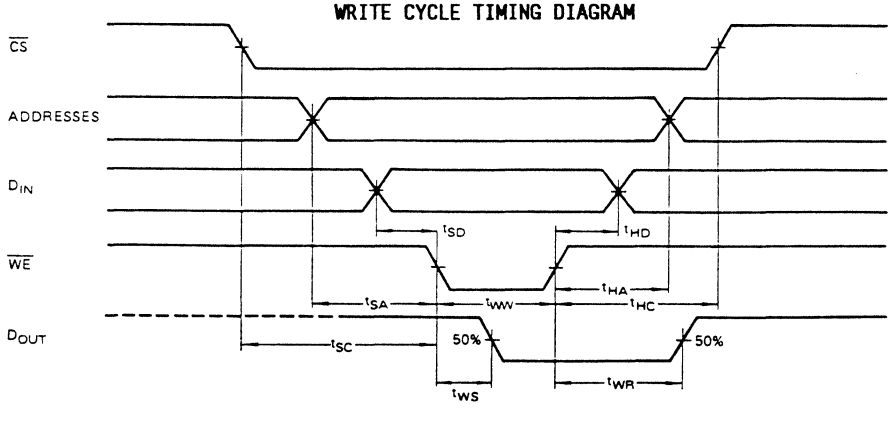


ADVANCE INFO.

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}			10.0	ns
Write Recovery Time	t_{WR}			15.0	ns
Address Set Up Time	t_{SA}	3.0			ns
Chip Select Set Up Time	t_{SC}	3.0			ns
Data Set Up Time	t_{SD}	3.0			ns
Address Hold Time	t_{HA}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

2

Section 3

Application Specific Bipolar ECL RAMs — *At a Glance*

Page	Device	Cycle Time (ns)	Capacity	Package Options
3–3	MBM10423LL–6	6	1024 bits (256w x 4b)	24-pin Ceramic DIP, FPT 24-pad Ceramic LCC
3–15	MBM100423LL–6	6	1024 bits (256w x 4b)	24-pin Ceramic DIP, FPT 24-pad Ceramic LCC
3–27	MBM10476LL–9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3–39	MBM10476RR–9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3–47	MBM10476RL–9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3–57	MBM100476LL–9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3–69	MBM100476RR–9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3–79	MBM100476RL–9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3–89	MBM10486LL–13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3–101	MBM10486RR–13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3–109	MBM10486RL–13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3–117	MBM100486LL–13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3–129	MBM100486RR–13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3–137	MBM100486RL–13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP

3

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10423LL-6

October 1987
Edition 2.0

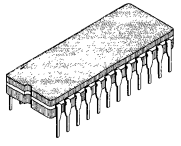
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10423LL is fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits with address input and output latches. Generally in the system, preceeding logic IC is needed for the synchronous entry of asynchronous address signal inputs of the RAM. MBM 10423LL contains internal latch circuits so that it can take synchronous address input and output timing, which contribute to higher system performance and save of power dissipation and board area. And it features on-chip voltage compensation for improved noise margin.

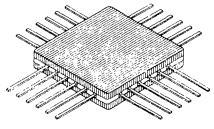
The MBM 10423LL offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 10423LL is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin Ceramic DIP, Flat Package, or LCC and is fully compatible with industry standard 10K-series ECL families.

- 256 words x 4 bits organization
- Address input and output latches which can be controlled separately
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10K-series ECL families
- Latch cycle time: 6 ns max.
- Address access time: 5 ns max.
- Block select access time: 3 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.84 mW/bit
- DOPOS and IOP-II



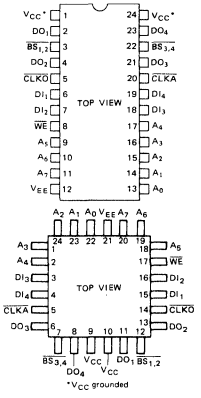
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 11

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

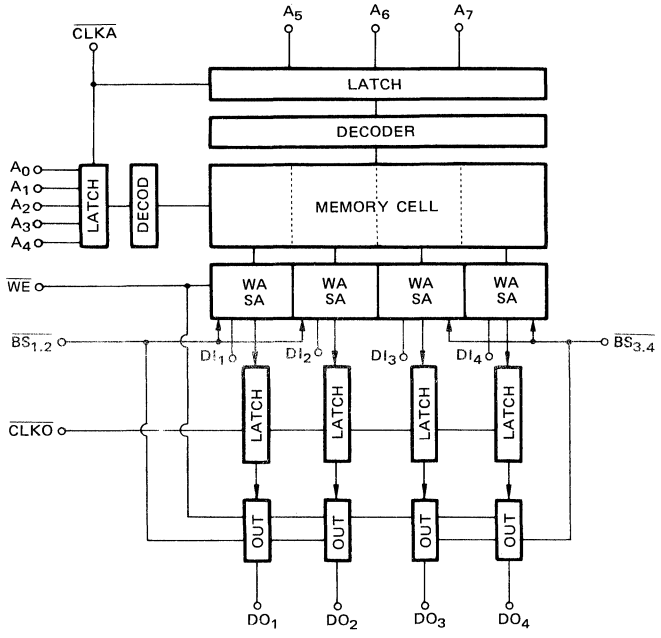
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MBM 10423LL BLOCK DIAGRAM



Symbol	Pin Name	Symbol	Pin Name
$A_0 \sim A_7$	Address Input	$\overline{CLKA}$	Address Latch Clock
$DI_1 \sim DI_4$	Data Input	$\overline{CLKO}$	Output Latch Clock
$DO_1 \sim DO_4$	Data Output	V_{EE}	Power Supply (–5.2V)
$\overline{WE}$	Write Enable	V_{CC}	Power Supply (0V)
$\overline{BS_{1.2}}, \overline{BS_{3.4}}$	Block Select		

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10423LL is fully decoded 1024 bit read/write random access memory organized as 256 words by 4 bits with address input and output latches which can be controlled separately by $\overline{CLKA}$ and $\overline{CLKO}$ pins. When clock is in high state, data is latched, while clock is held low, data goes through the latches like as conventional MBM 10422A. Memory cell selection is achieved by means of a 8-bit address designated A_0 through A_7. The active low Block Select inputs are provided for memory expansion. Two separate blocks are selected simultaneously by $\overline{BS_{1.2}}$ or $\overline{BS_{3.4}}$ pin. The read and write operation are controlled by the state of active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$, $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94 V	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for flat package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{BS}$ and $\overline{CLKA}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-220			mA	0°C to 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		6	7	pF

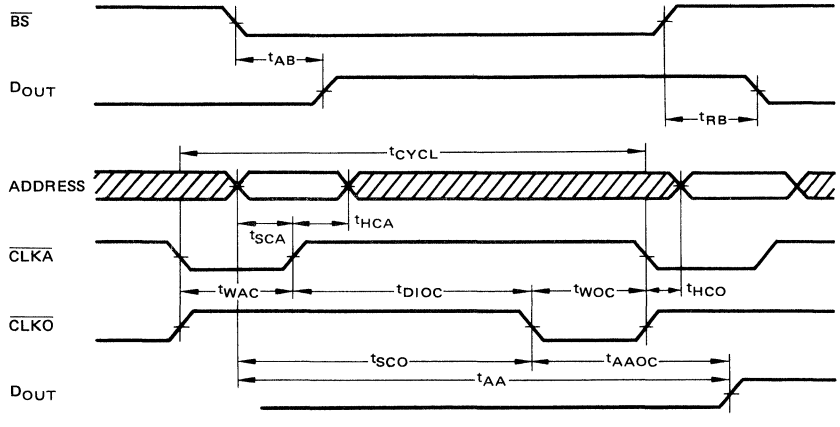
AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = –5.2V ± 5%, Output Load = 50Ω to –2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≥ 2.5m/s, T_C = 0°C to 75°C for Flatpackage and LCC, unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	1.5		5.0	ns
Output Latch Access Time	t_{AAOC}	0.5		3.0	ns
Block Select Access Time	t_{AB}	0.5		3.0	ns
Block Select Recovery Time	t_{RB}	0.5		3.0	ns
Address Latch Clock Pulse Width	t_{WAC}	2.5			ns
Output Latch Clock Pulse Width	t_{WOC}	2.5			ns
Address Latch Clock Setup Time	t_{SCA}	1.5			ns
Address Latch Clock Hold Time	t_{HCA}	2.0			ns
Output Latch Clock Setup Time	t_{SCO}	2.5			ns
Output Latch Clock Hold Time	t_{HCO}	1.0			ns
Delay Time Between Input Clock and Output Clock	t_{DIOC}	1.0			ns
Latch Cycle Time	t_{CYCL}	6.0			ns

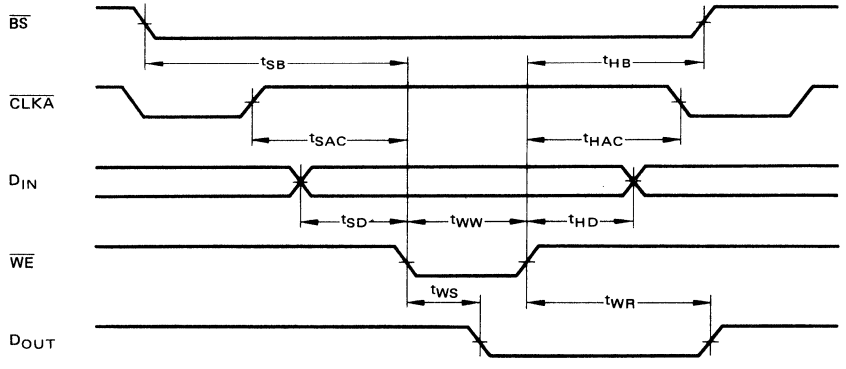
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	3.5			ns
Write Disable Time	t_{WS}	0.5		3.5	ns
Write Recovery Time	t_{WR}	0.5		3.5	ns
Write Clock Setup Time	t_{SAC}	−1.5			ns
Block Select Setup Time	t_{SB}	0.5			ns
Data Setup Time	t_{SD}	0.5			ns
Write Clock Hold Time	t_{HAC}	1.5			ns
Block Select Hold Time	t_{HB}	1.0			ns
Data Hold Time	t_{HD}	1.0			ns

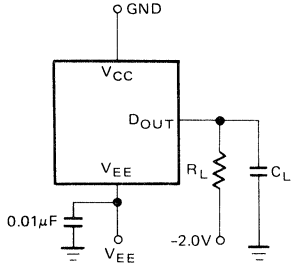
WRITE CYCLE TIMING DIAGRAM

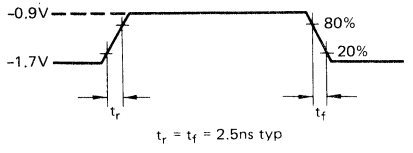


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f = 2.5ns$ typ

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

3

FUNCTIONAL TRUTH TABLE

$\overline{BS}$	$\overline{WE}$	DI	$\overline{CLKA}$	$\overline{CLKO}$	OUTPUT	MODE
H	X	X	X	X	L	DISABLED
L	L	L	L	L	L	THROUGH, WRITE "L"
L	L	H	L	L	L	THROUGH, WRITE "H"
L	H	X	L	L	DO	THROUGH, READ
L	L	L	H	X	L	LATCHED, WRITE "L"
L	L	H	H	X	L	LATCHED, WRITE "H"
L	H	X	H	L	DO^{-I}	LATCHED, READ
L	H	X	X	H	DO^{-O}	LATCHED, READ

L : Low Voltage Level
H : High Voltage Level
X : Don't care
DO^{-I} : Data Out at the Location Addressed Before $\overline{CLKA}$ Goes From "L" to "H"
DO^{-O} : Data Out at the Location Addressed Before $\overline{CLKO}$ Goes From "L" to "H"

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

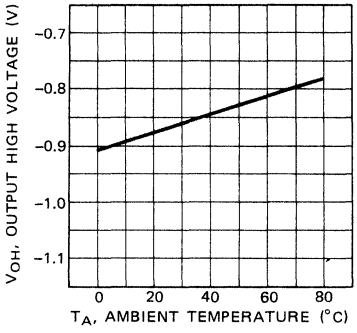


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

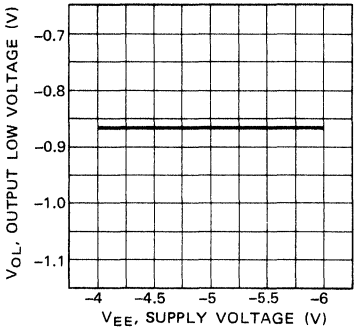


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

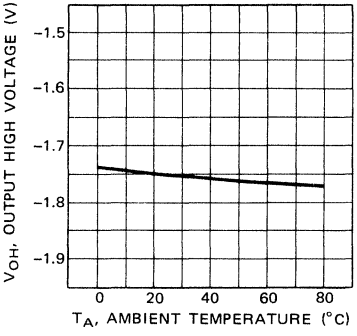


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

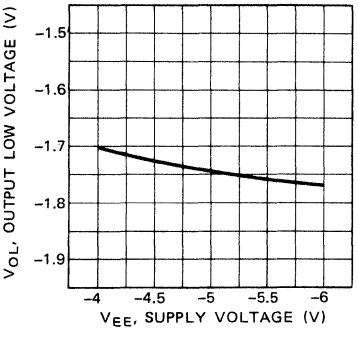


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

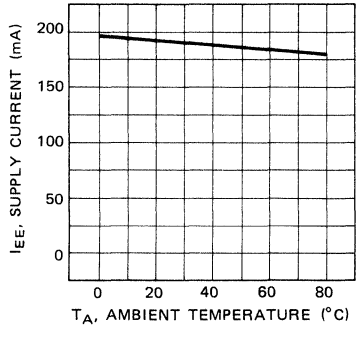
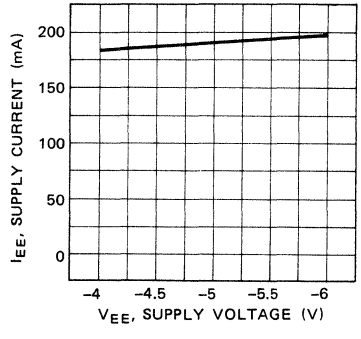


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE



3

Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

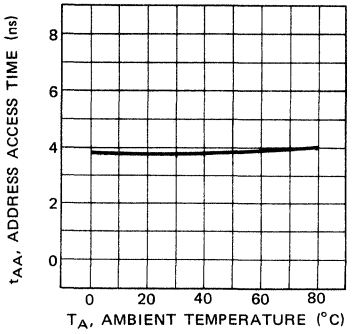


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

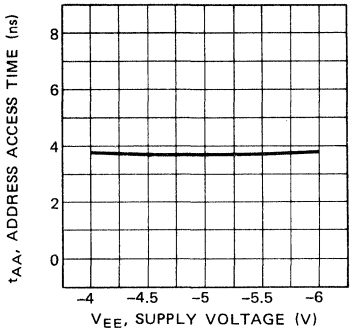


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

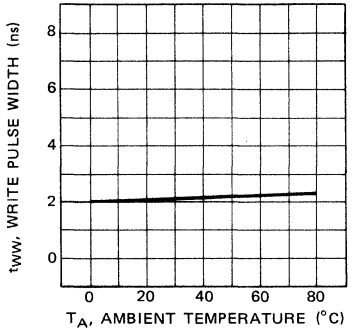
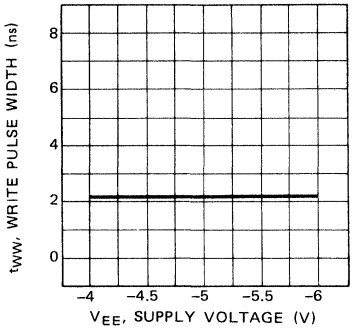


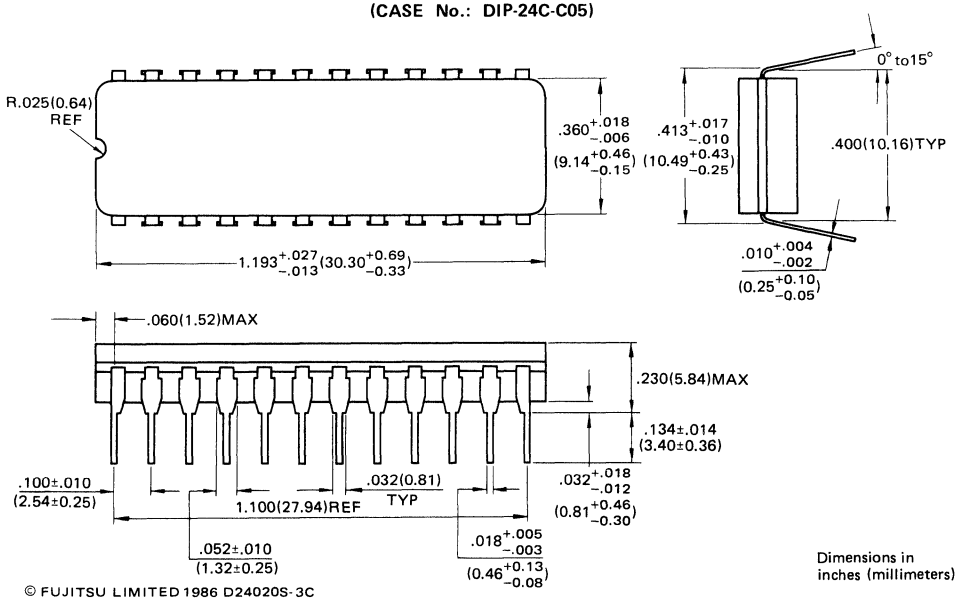
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)

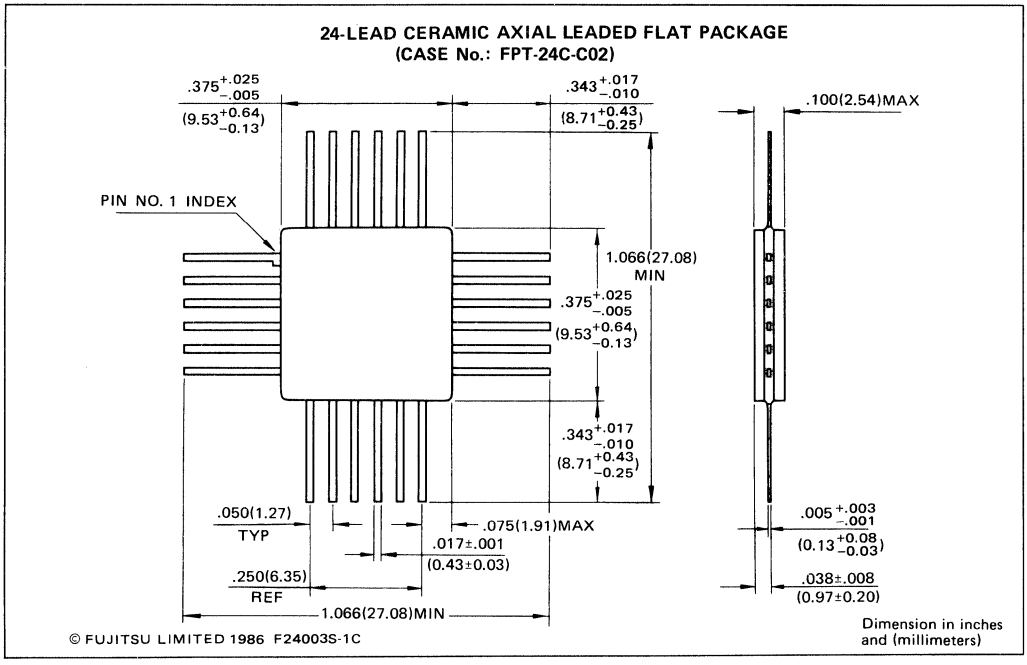


Dimensions in
inches (millimeters)

3

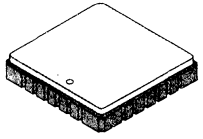
PACKAGE DIMENSIONS

CERAMIC FPT (: -ZF)



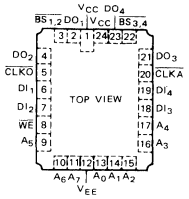
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

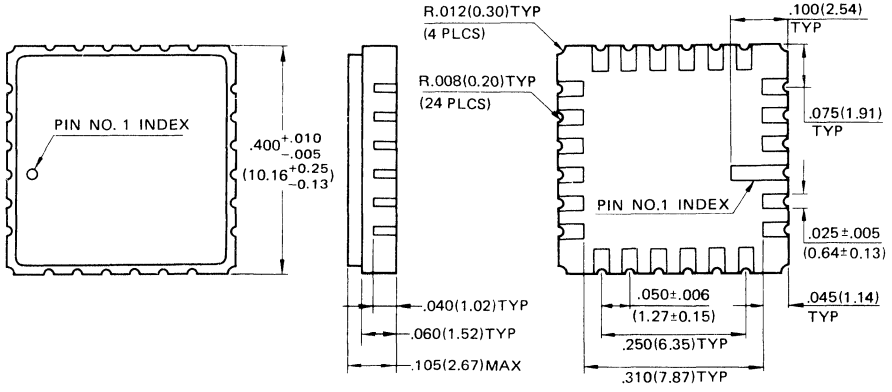


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

3

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100423LL-6

October 1987
Edition 2.0

1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

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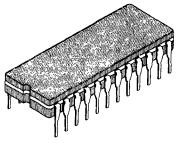
Operation for the MBM 100423LL is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin Ceramic DIP, Flat Package, or LCC and is fully compatible with industry standard 100K-series ECL families.

- 256 words x 4 bits organization
- Address input and output latches which can be controlled separately
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry standard 100K-series ECL families
- Latch cycle time: 6 ns max.
- Address access time: 5 ns max.
- Block select access time: 3 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.73 mW/bit
- DOPOS and IOP-II

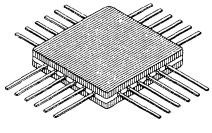
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



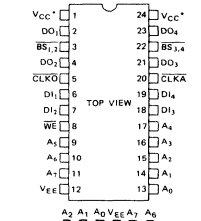
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 11

PIN ASSIGNMENT

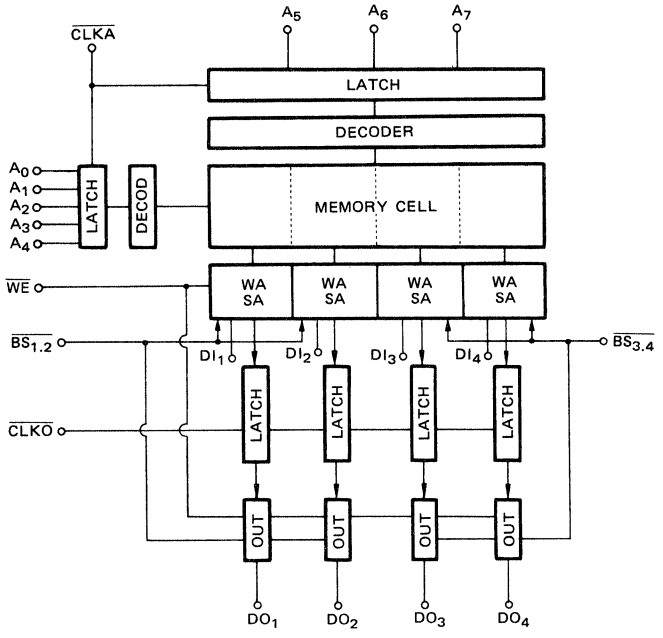


LCC PAD CONFIGURATION: See Page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MBM 100423LL BLOCK DIAGRAM



Symbol	Pin Name	Symbol	Pin Name
$A_0 \sim A_7$	Address Input	$\overline{CLKA}$	Address Latch Clock
$DI_1 \sim DI_4$	Data Input	$\overline{CLKO}$	Output Latch Clock
$DO_1 \sim DO_4$	Data Output	V_{EE}	Power Supply (–5.2V)
$\overline{WE}$	Write Enable	V_{CC}	Power Supply (0V)
$\overline{BS_{1.2}}$,$\overline{BS_{3.4}}$	Block Select		

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100423LL is fully decoded 1024 bit read/write random access memory organized as 256 words by 4 bits with address input and output latches which can be controlled separately by $\overline{CLKA}$ and $\overline{CLKO}$ pins. When clock is in high state, data is latched, while clock is held low, data goes through the latches like as conventional MBM100422A. Memory cell selection is achieved by means of a 8-bit address designated A_0 through A_7. The active low Block Select inputs are provided for memory expansion. Two separate blocks are selected simultaneously by $\overline{BS_{1.2}}$ or $\overline{BS_{3.4}}$ pin. The read and write operation are controlled by the state of active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$, $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for flat package and LCC, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{BS}$ and $\overline{CLKA}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-220			mA

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		6	7	pF

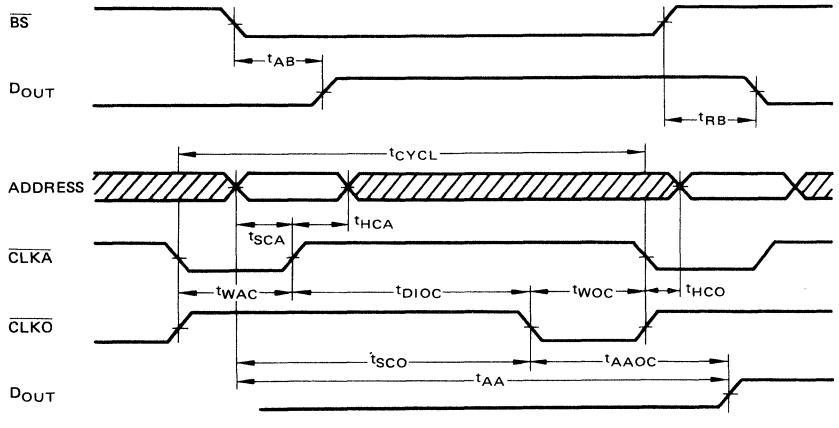
AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ± 5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≥ 2.5m/s, T_C = 0°C to 85°C for Flatpackage and LCC, unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	1.5		5.0	ns
Output Latch Access Time	t_{AAOC}	0.5		3.0	ns
Block Select Access Time	t_{AB}	0.5		3.0	ns
Block Select Recovery Time	t_{RB}	0.5		3.0	ns
Address Latch Clock Pulse Width	t_{WAC}	2.5			ns
Output Latch Clock Pulse Width	t_{WOC}	2.5			ns
Address Latch Clock Setup Time	t_{SCA}	1.5			ns
Address Latch Clock Hold Time	t_{HCA}	2.0			ns
Output Latch Clock Setup Time	t_{SCO}	2.5			ns
Output Latch Clock Hold Time	t_{HCO}	1.0			ns
Delay Time Between Input Clock and Output Clock	t_{DIOC}	1.0			ns
Latch Cycle Time	t_{CYCL}	6.0			ns

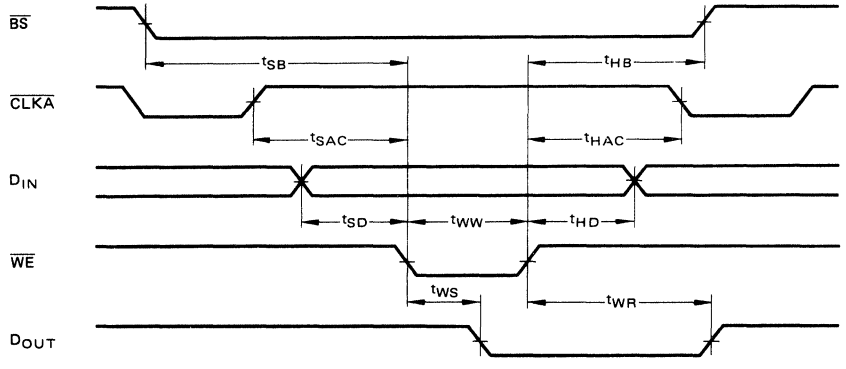
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	3.5			ns
Write Disable Time	t_{WS}	0.5		3.5	ns
Write Recovery Time	t_{WR}	0.5		3.5	ns
Write Clock Setup Time	t_{SAC}	−1.5			ns
Block Select Setup Time	t_{SB}	0.5			ns
Data Setup Time	t_{SD}	0.5			ns
Write Clock Hold Time	t_{HAC}	1.5			ns
Block Select Hold Time	t_{HB}	1.0			ns
Data Hold Time	t_{HD}	1.0			ns

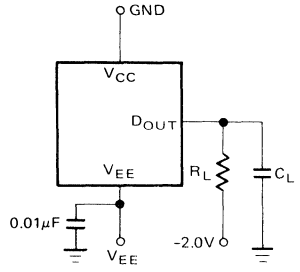
WRITE CYCLE TIMING DIAGRAM

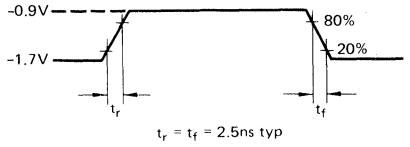


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f = 2.5ns$ typ

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

3

FUNCTIONAL TRUTH TABLE

$\overline{BS}$	$\overline{WE}$	DI	$\overline{CLKA}$	$\overline{CLKO}$	OUTPUT	MODE
H	X	X	X	X	L	DISABLED
L	L	L	L	L	L	THROUGH, WRITE "L"
L	L	H	L	L	L	THROUGH, WRITE "H"
L	H	X	L	L	DO	THROUGH, READ
L	L	L	H	X	L	LATCHED, WRITE "L"
L	L	H	H	X	L	LATCHED, WRITE "H"
L	H	X	H	L	DO^{-I}	LATCHED, READ
L	H	X	X	H	DO^{-O}	LATCHED, READ

L : Low Voltage Level
H : High Voltage Level
X : Don't care
DO^{-I} : Data Out at the Location Addressed Before $\overline{CLKA}$ Goes From "L" to "H"
DO^{-O} : Data Out at the Location Addressed Before $\overline{CLKO}$ Goes From "L" to "H"

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

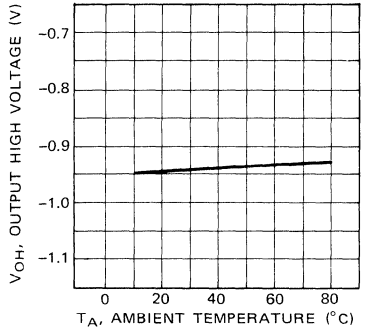


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

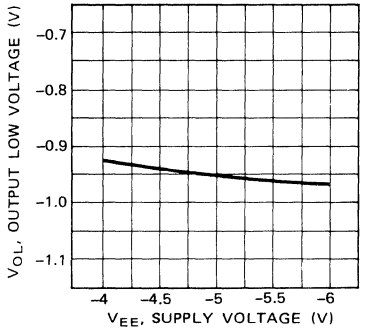


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

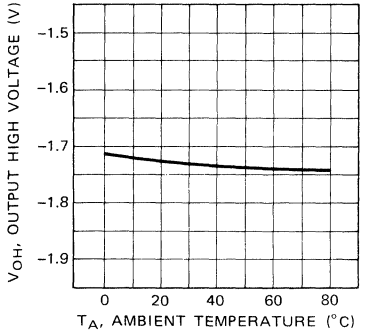


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

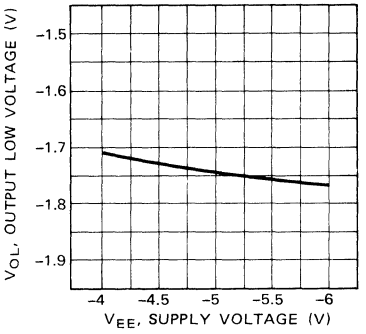


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

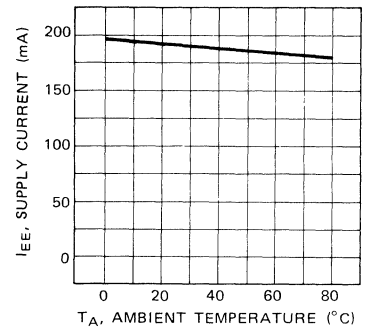


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

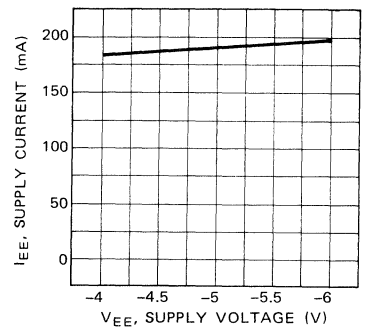


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Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

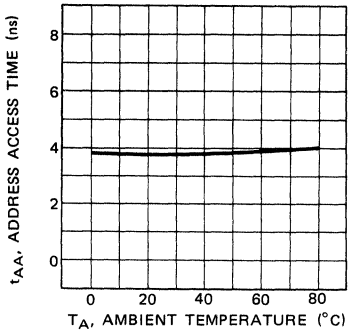

Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

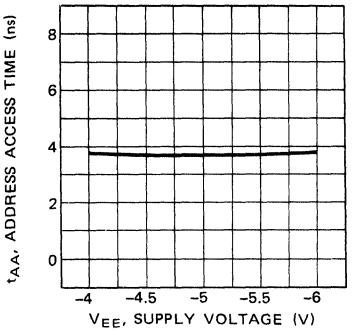

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Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

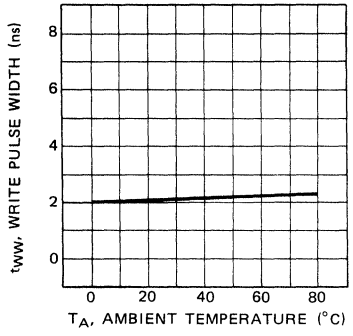
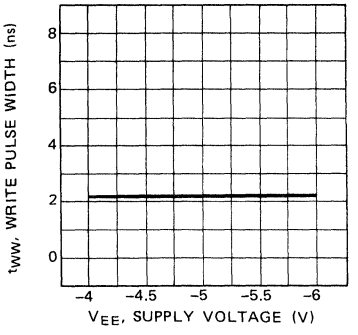


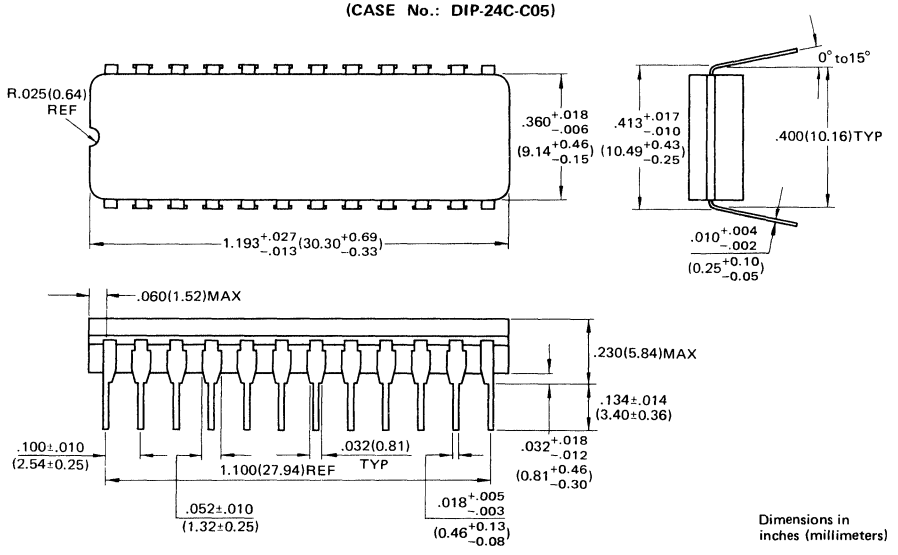
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

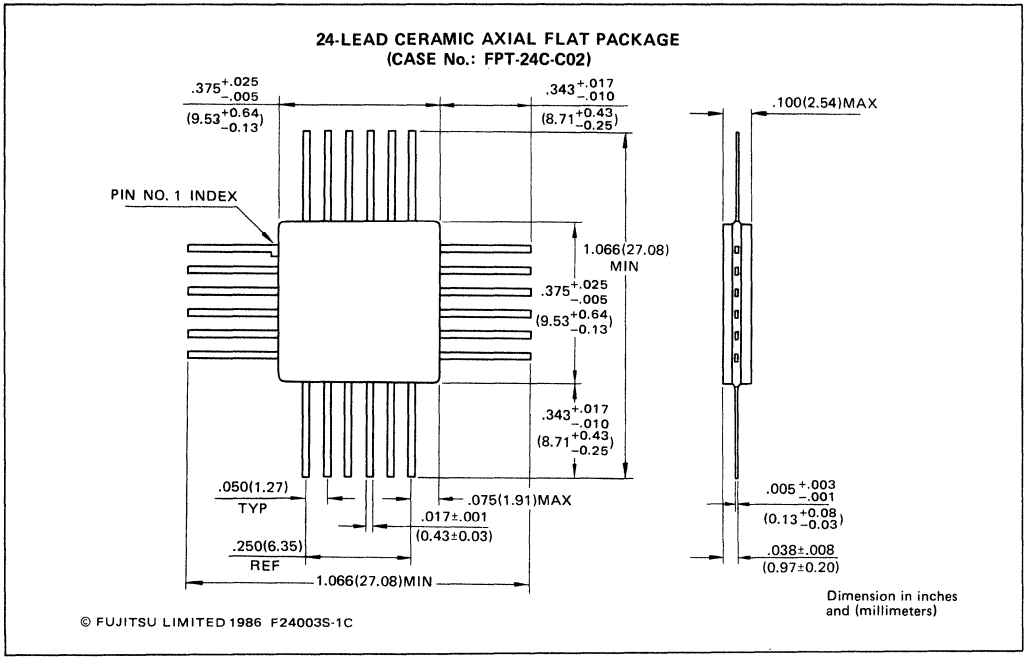
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



3

PACKAGE DIMENSIONS

CERAMIC FPT (: -ZF)



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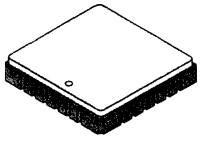
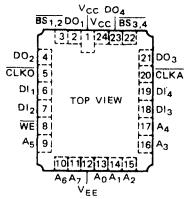
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

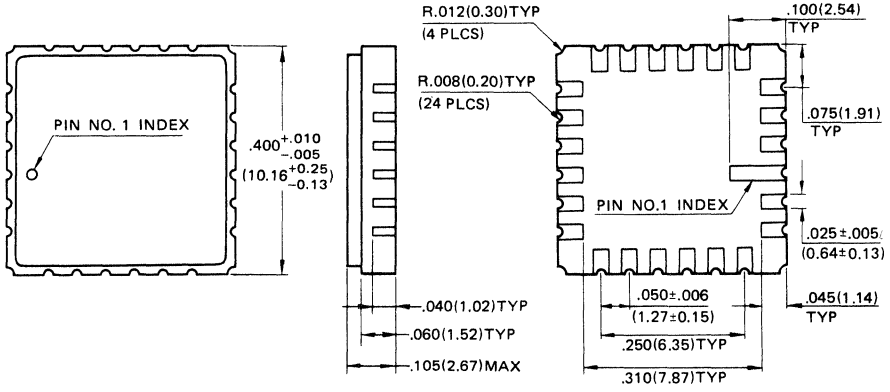


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

3

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10476LL-9

4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

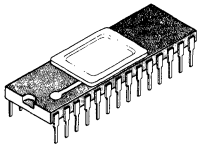
December, 1988
Edition 2.0

The Fujitsu MBM10476LL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

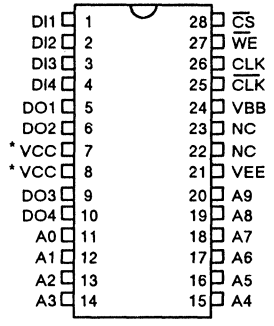
Operation for the MBM10476LL is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 9ns
  Address access time : 7ns
- Power dissipation : 1976mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

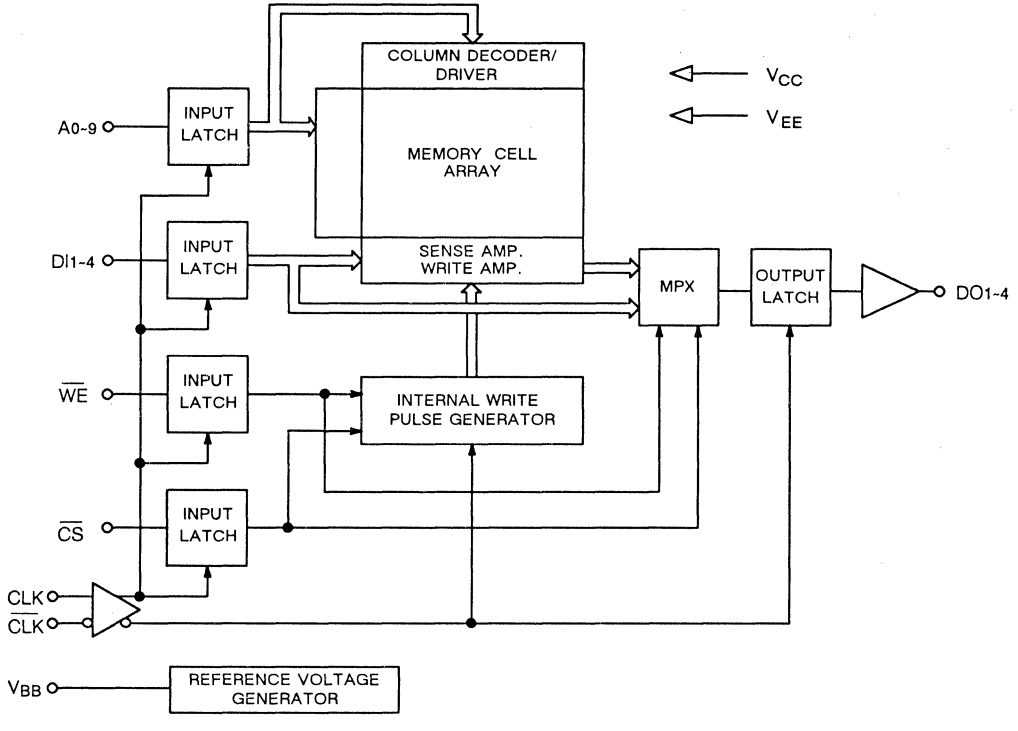
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10476LL BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address inputs
DI1 thru DI4	Data inputs
DO1 thru DO4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
CLK, $\overline{CLK}$	Clock inputs
VBB	Reference voltage (-1.29V)
VEE	Supply voltage (-5.2V)
VCC	Supply voltage (0V)
NC	No connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

3

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10476LL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

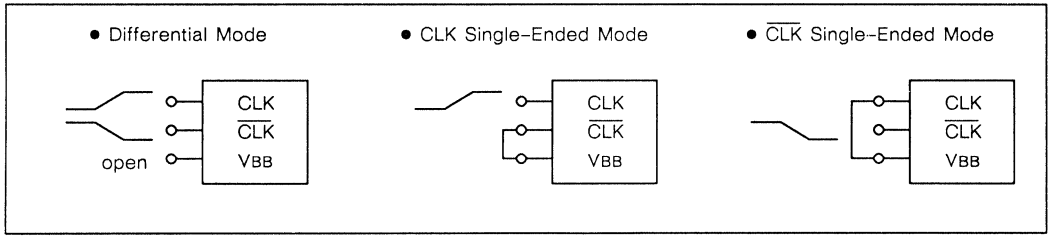
When setup time is wide enough, output data becomes valid in the short delay time (tDR) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time (tA(ADD)) similar to the traditional RAM.

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



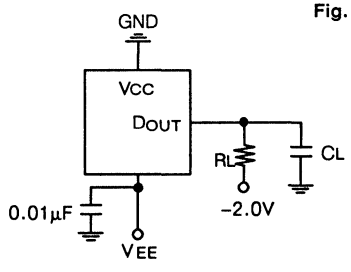
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

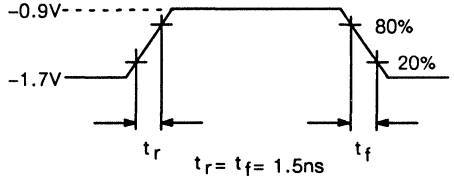
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	6.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	9.0			ns
Address Access Time	$t_{A(ADD)}$			7.0 *1	ns
Data Access Time	$t_{A(DI)}$			4.0 *2	ns
Write Access Time	$t_{A(W)}$			4.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			4.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			8.0 *5	ns
Output Delay Time	t_{DR}			3.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tSA = 1.0ns
*2 Specified at tSD = 1.0ns
*3 Specified at tSW = 1.0ns
*4 Specified at tSC = 1.0ns
*5 Specified at tWL(CLK) = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)\ max}$, $t_{SA} > t_{A(ADD)\ max}$, $t_{SC} > t_{A(CS)\ max}$, $t_{SD} > t_{A(DI)\ max}$, $t_{SW} > t_{A(W)\ max}$.

Fig. 2 - AC TEST CONDITIONS



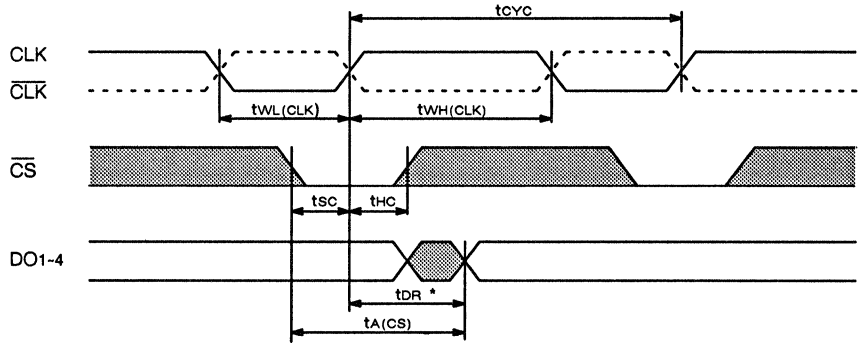
Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

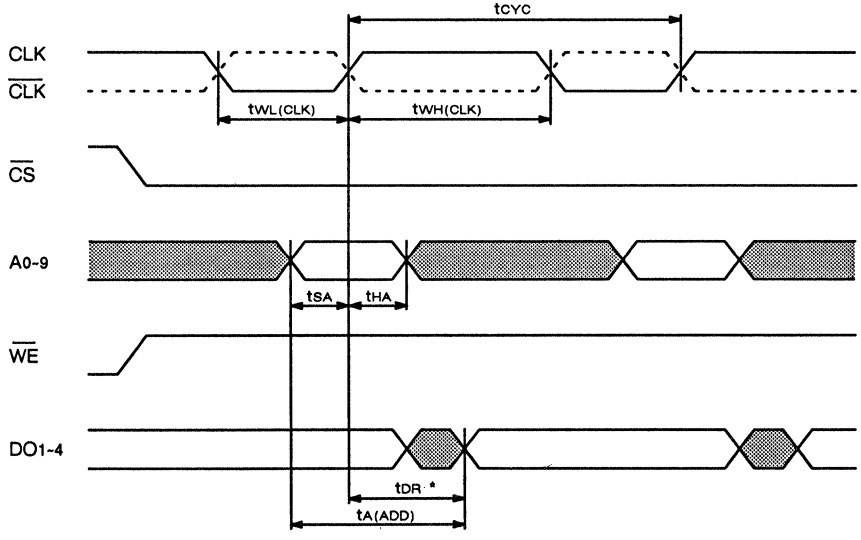
READ CYCLE TIMING DIAGRAMS

• CHIP SELECT ACCESS MODE



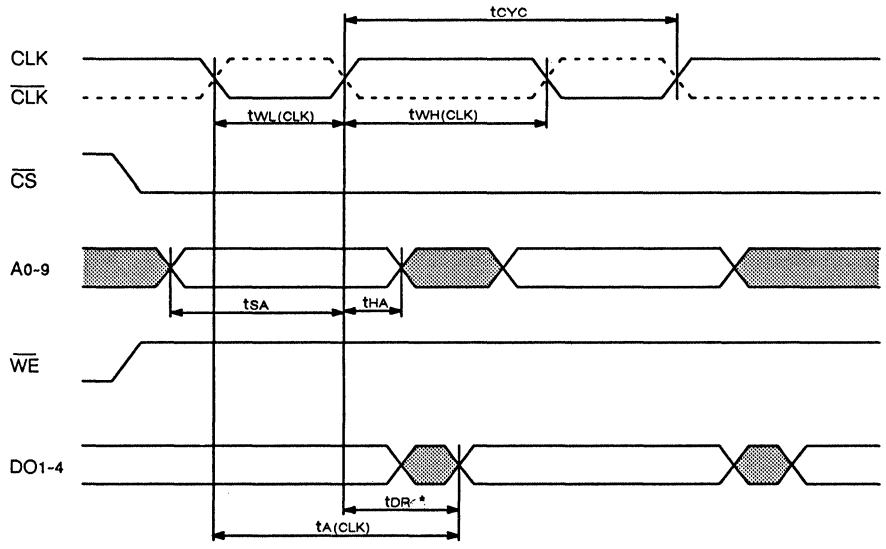
* Output is valid at tDR when tSC > tA(CS) max − tDR max.

• ADDRESS ACCESS MODE



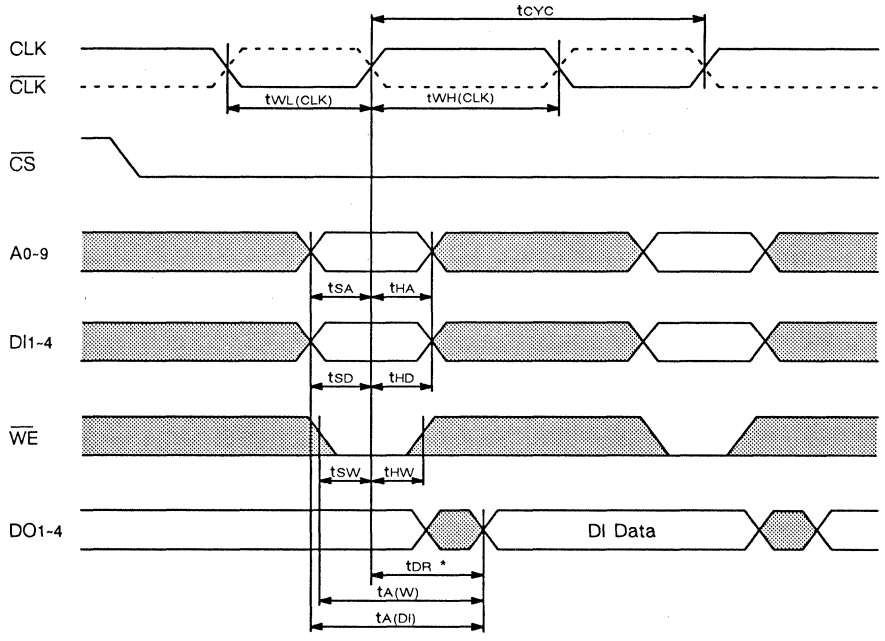
* Output is valid at tDR when tSA > tA(ADD) max − tDR max.

● CLOCK ACCESS MODE



* Output is valid at tDR when tWL(CLK) > tA(CLK) max − tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at t_{DR} when $t_{SW} > t_{A(W)\ max} - t_{DR\ max}$ and $t_{SD} > t_{A(DI)\ max} - t_{DR\ max}$

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

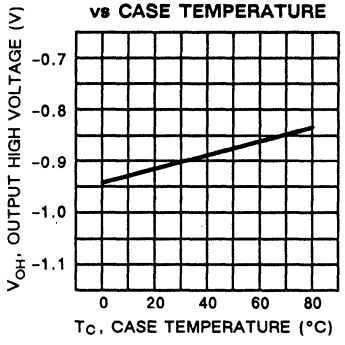


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

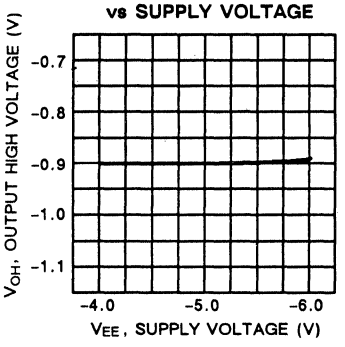


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

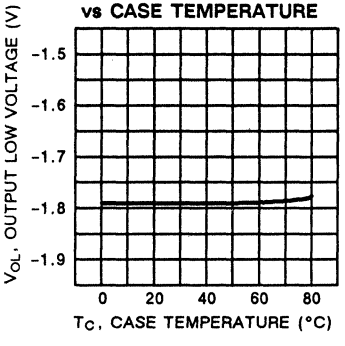


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

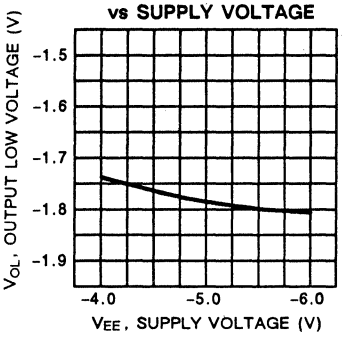


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

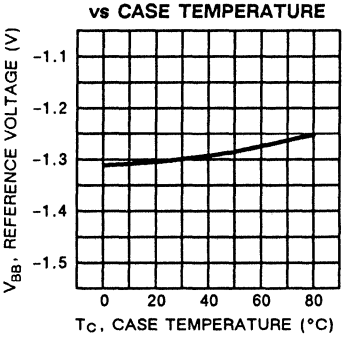


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE

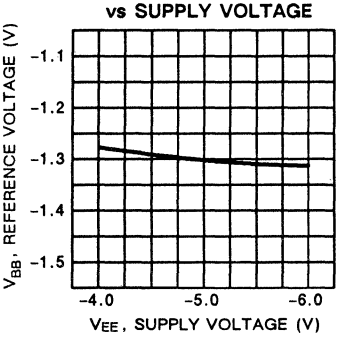


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Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

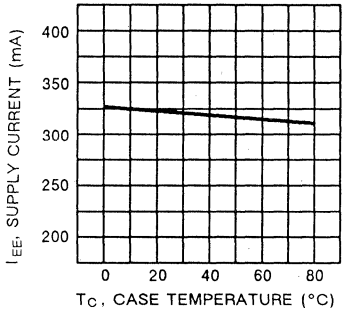


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

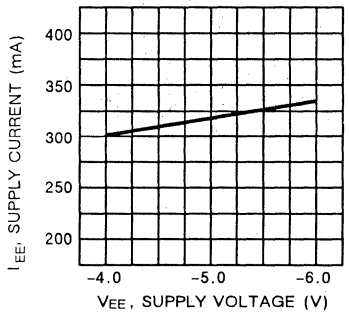


Fig. 11 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

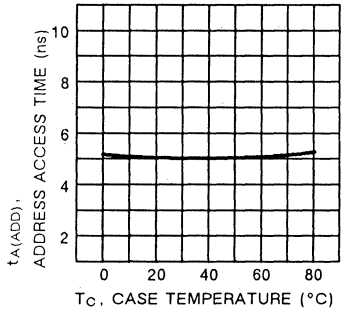


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

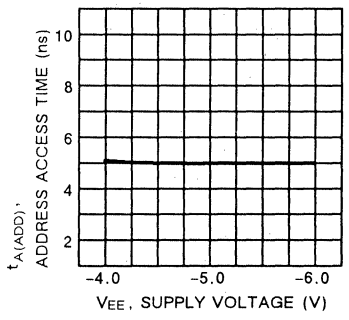


Fig. 13 – CLOCK ACCESS TIME vs CASE TEMPERATURE

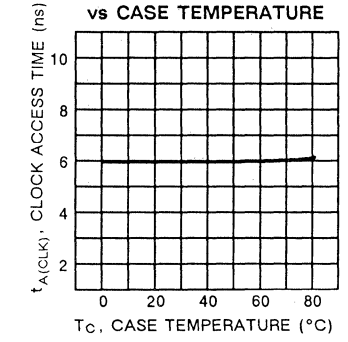


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

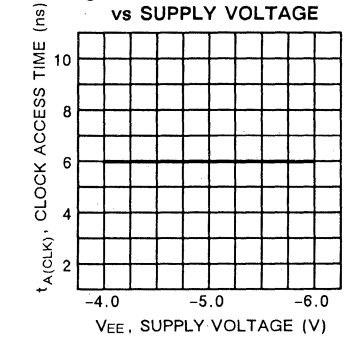


Fig. 15 – OUTPUT DELAY TIME vs CASE TEMPERATURE

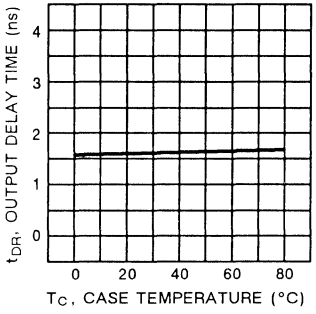


Fig. 16 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE

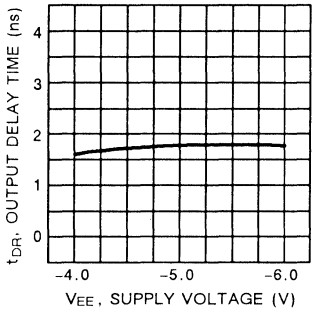


Fig. 17 – CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

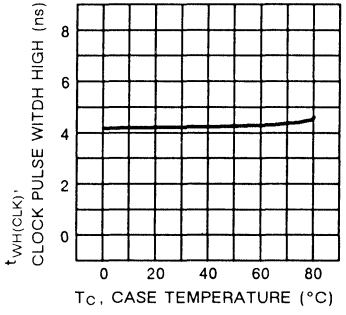
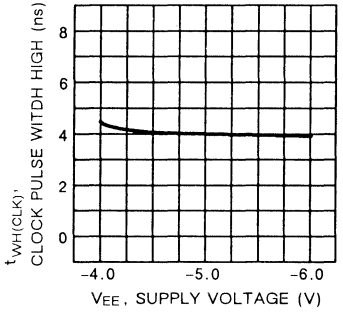


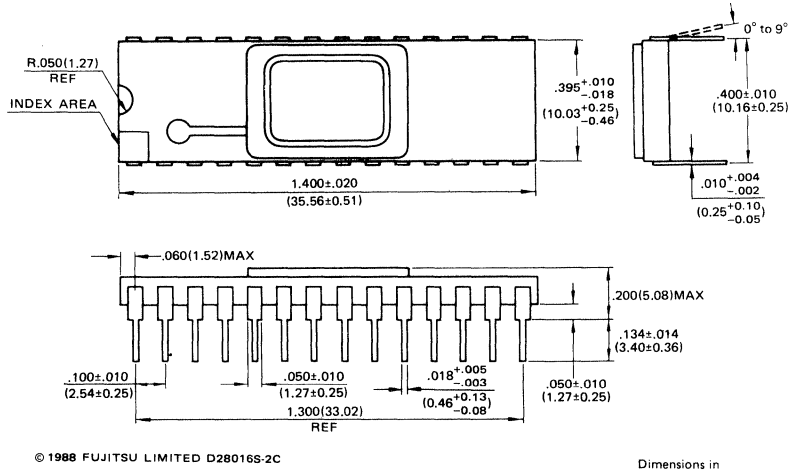
Fig. 18 – CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

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FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10476RR-9

December, 1988
Edition 1.0

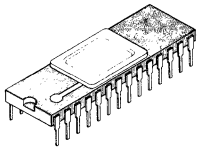
4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM10476RR-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allows to decrease the number of device on the board.

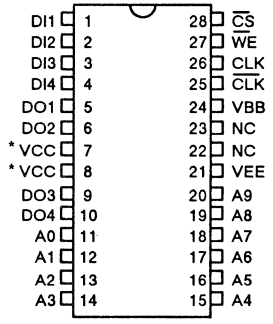
Operation for the MBM10476RR is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 2080mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

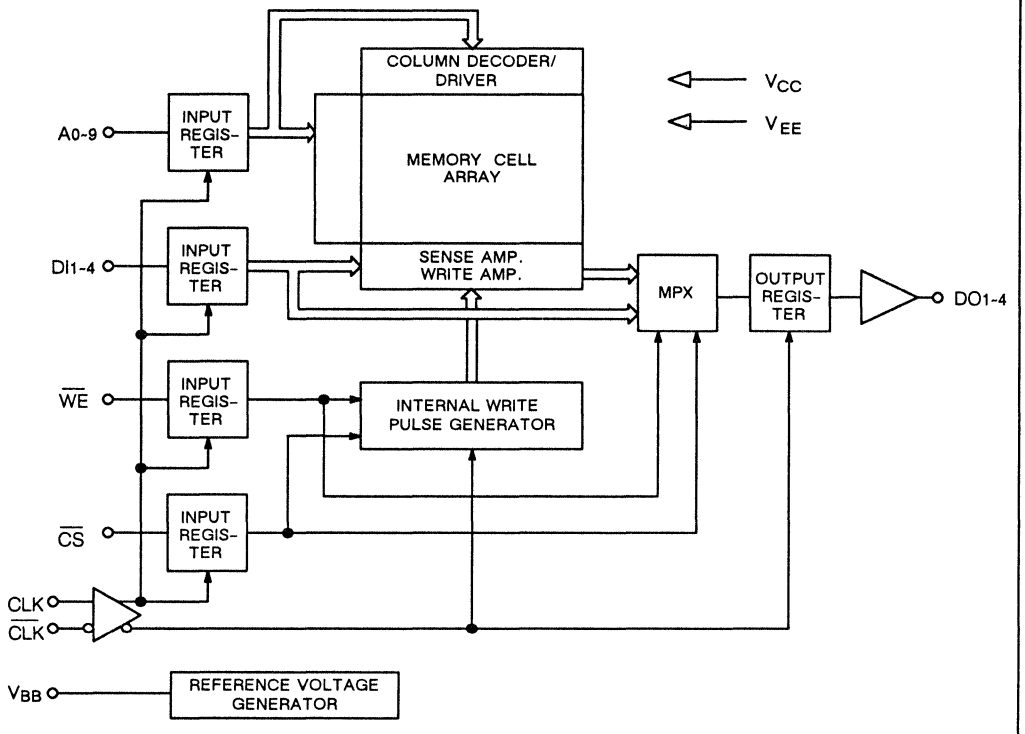
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10476RR-9 BLOCK DIAGRAM



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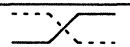
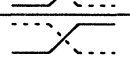
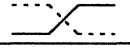
FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

 : Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.29V)
VEE	Supply Voltage (-5.2V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TC
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10476RR is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are edge triggered registered controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input and output registers are transparent when CLK ($\overline{CLK}$) goes high (low), and close to hold the data when CLK($\overline{CLK}$) goes low (high).

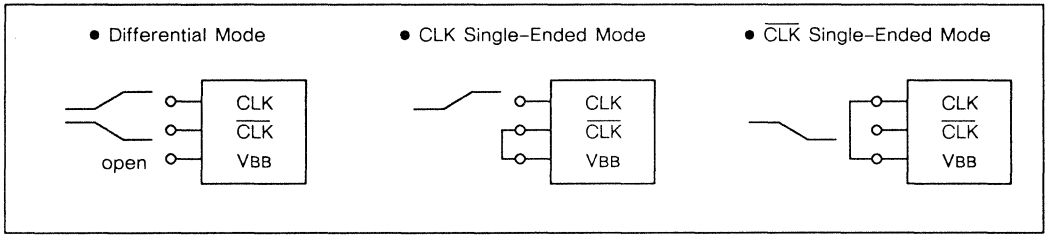
When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may not be stable during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes low (high), address data is held at output, while output data is kept valid during the same cycle. Thus, the output data becomes available at the next rising (falling) edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), inputs are transparent while previous read data appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the output by the CLK($\overline{CLK}$) rising (falling) edge of the next cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



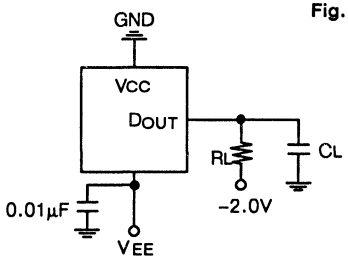
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

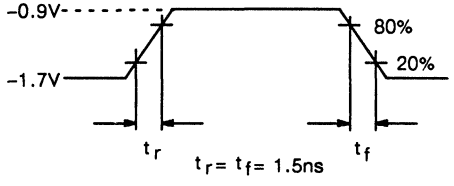
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Output Delay Time	t_{DR}			3.0	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 6.0ns
*2 Specified at tWH(CLK) > 6.0ns

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

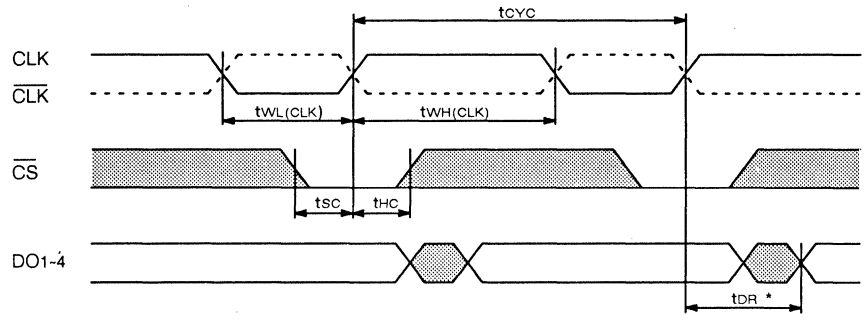


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

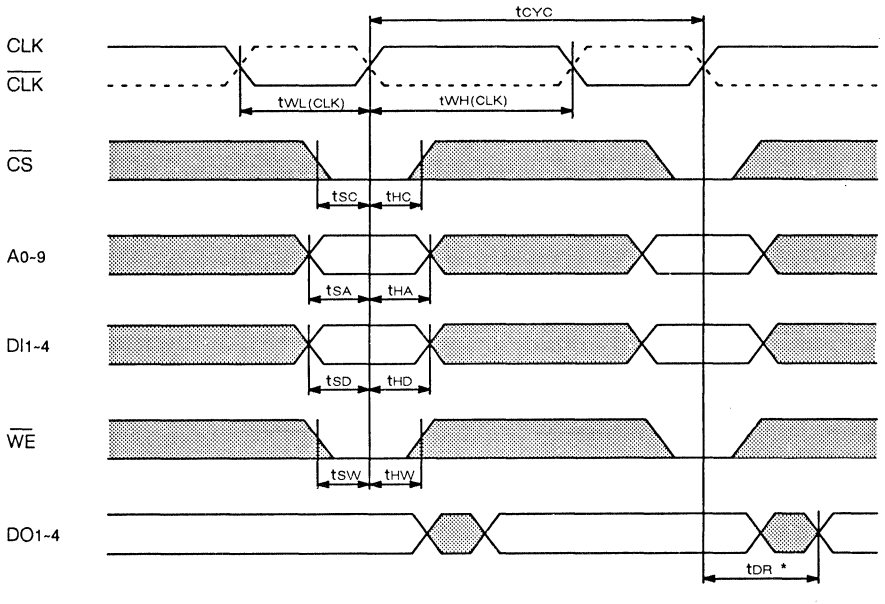
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

WRTE CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

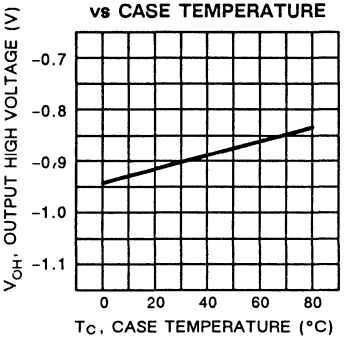


Fig. 4 - OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

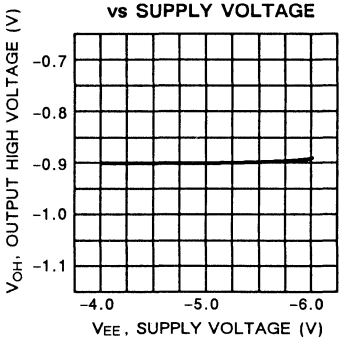


Fig. 5 - OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

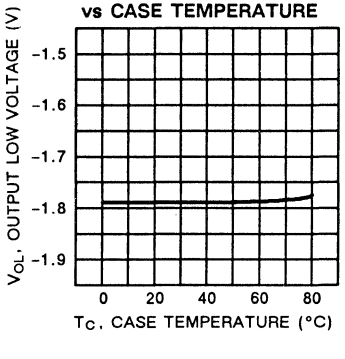


Fig. 6 - OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

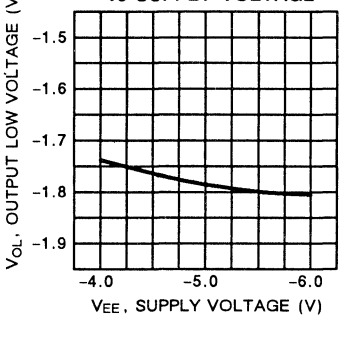


Fig. 7 - REFERENCE VOLTAGE vs CASE TEMPERATURE

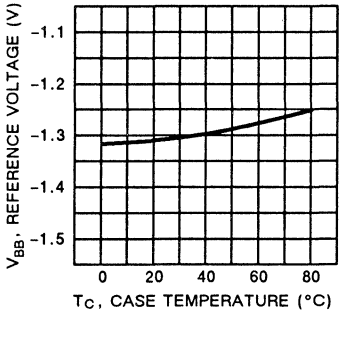
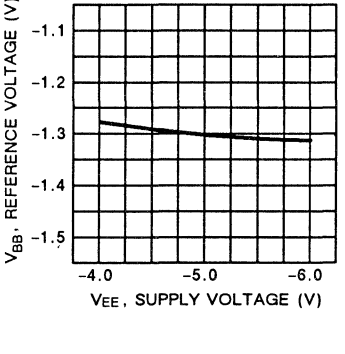


Fig. 8 - REFERENCE VOLTAGE vs SUPPLY VOLTAGE



3

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10476RL-9

4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

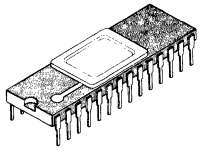
December, 1988
Edition 1.0

The Fujitsu MBM10476RL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

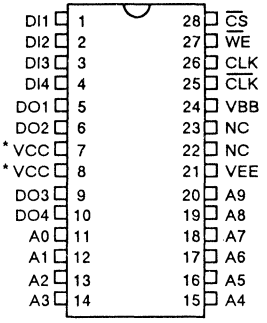
Operation for the MBM10476RL is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 2080mW max
- Open emitter output for ease of memory expansion
- Level-sensitive D-type latch for outputs and edge triggered registers for inputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

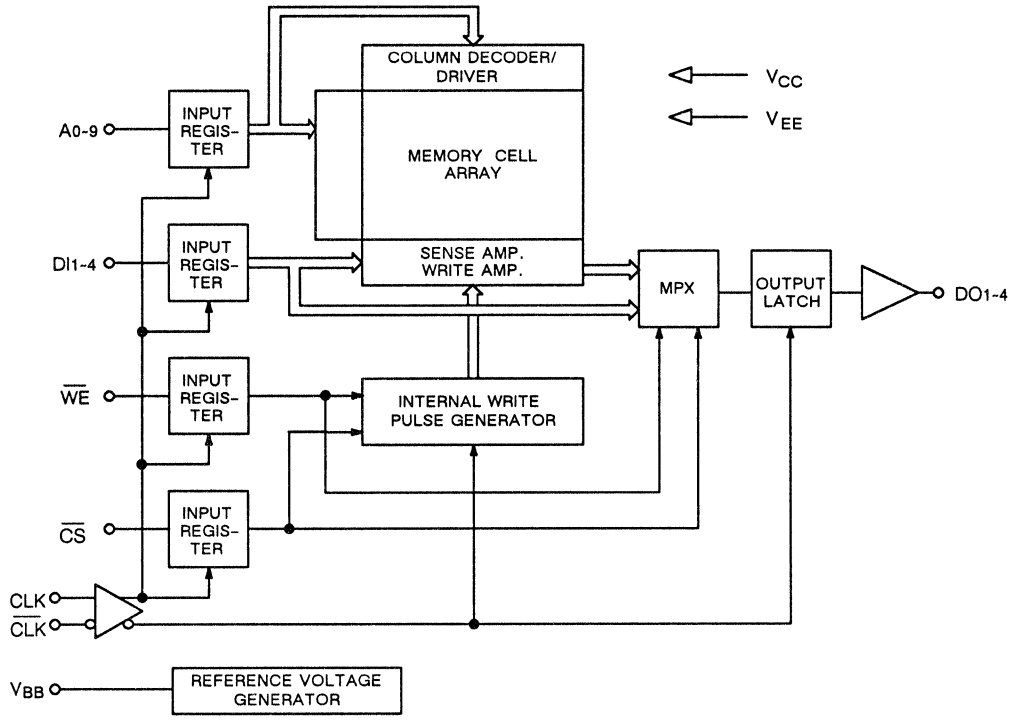
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10476RL-9 BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.29V)
VEE	Supply Voltage (-5.2V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10476RL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) furnish edge triggered registers, whereas outputs (DOUT) have level sensitive transparent latches.

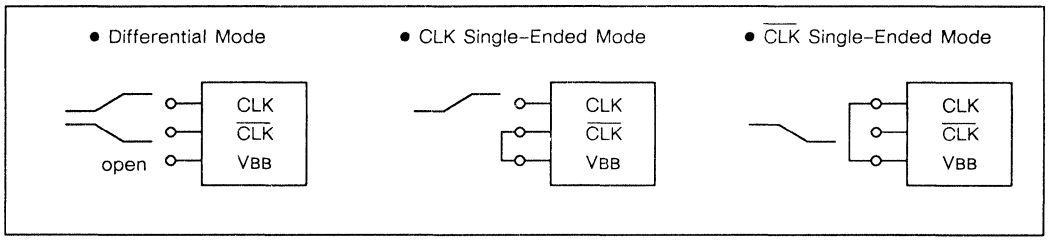
When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. All input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels are free to change for the rest of the cycle timeonce input data is held into the input register. Read out data becomes available during CLK low state in which output latches are transpatent. When CLK ($\overline{CLK}$) state is wide enough than the internal RAM access time, output data become valid in the short delay time (tDR) after the falling (rising)edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



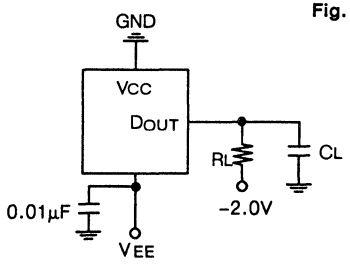
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

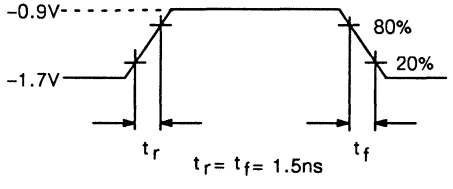
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Clock Access Time	$t_{A(CLK)}$			8.0 *3	ns
Output Delay Time	t_{DR}			3.0 *4	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at $t_{WL(CLK)}$ > 6.0ns
*2 Specified at $t_{WH(CLK)}$ > 6.0ns
*3 Specified at $t_{WH(CLK)}$ = 3.0ns
*4 Specified at $t_{WH(CLK)}$ > $t_{A(CLK)}$ max

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



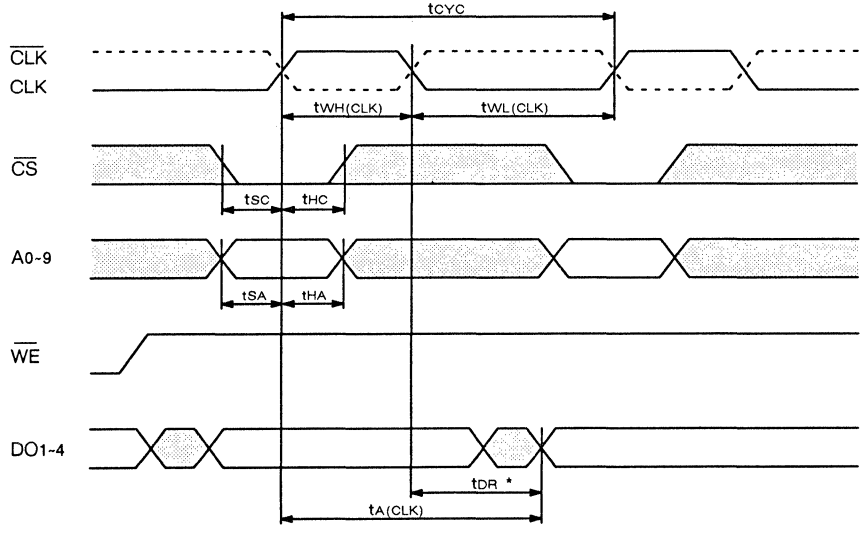
Note : All timing measurements referenced to 50% input levels.

3

Rise Time and Fall Time

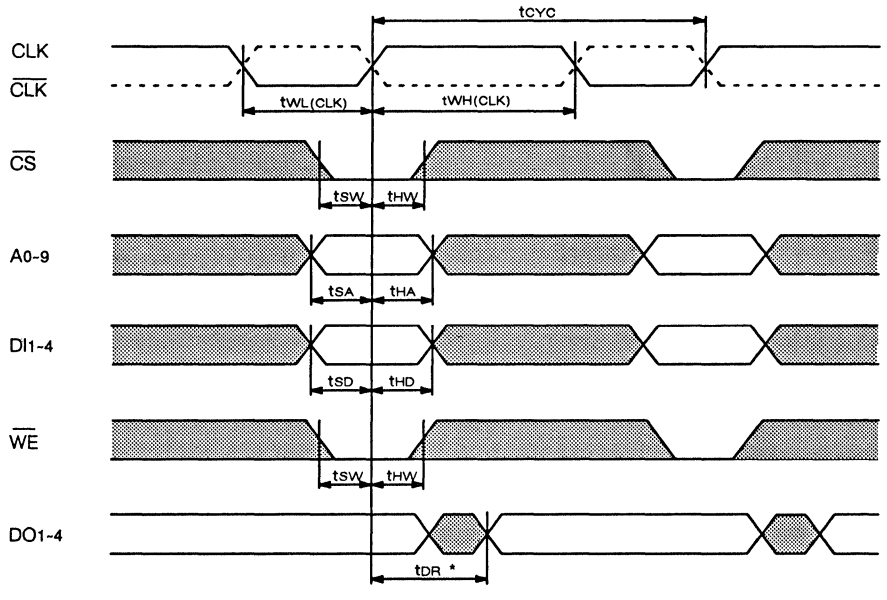
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max − tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max − tDR max.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

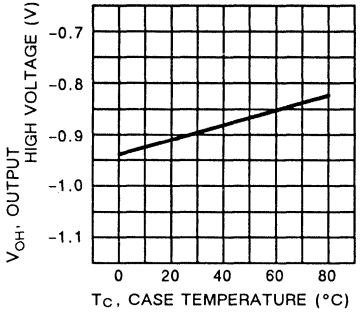


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

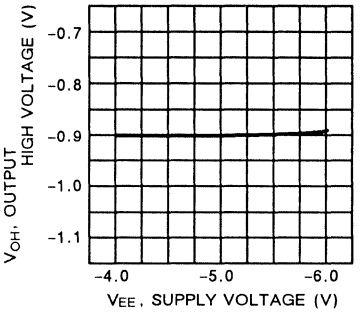


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

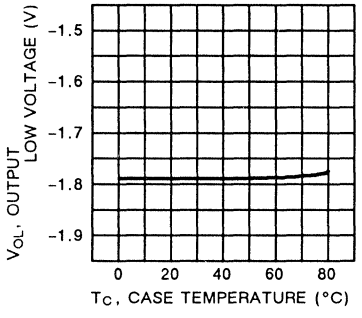


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

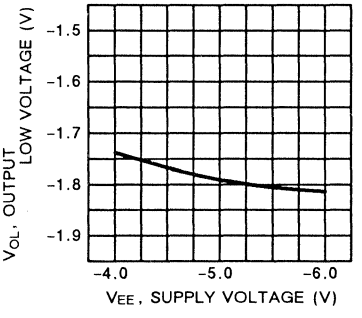


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

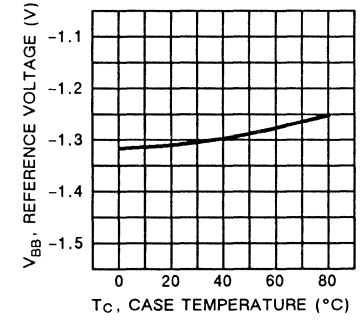


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE

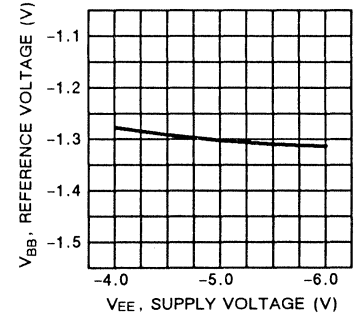


Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

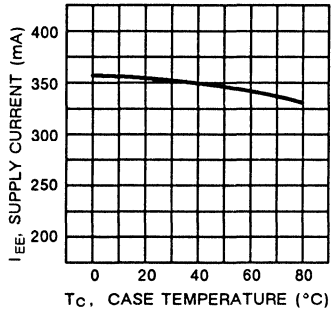


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

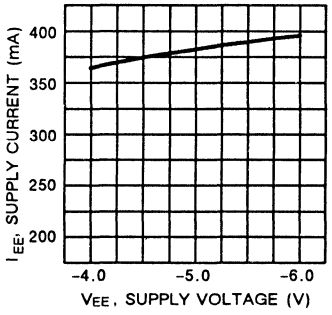


Fig. 11 – CLOCK ACCESS TIME vs CASE TEMPERATURE

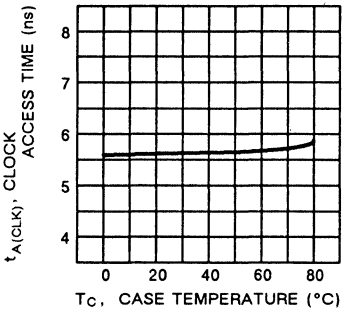


Fig. 12 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

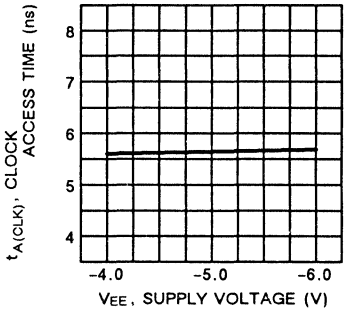


Fig. 13 – OUTPUT DELAY TIME vs CASE TEMPERATURE

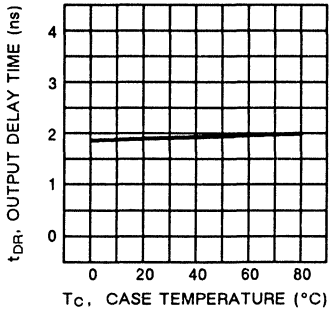
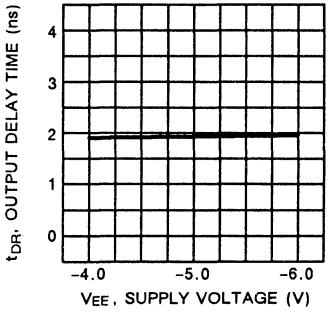


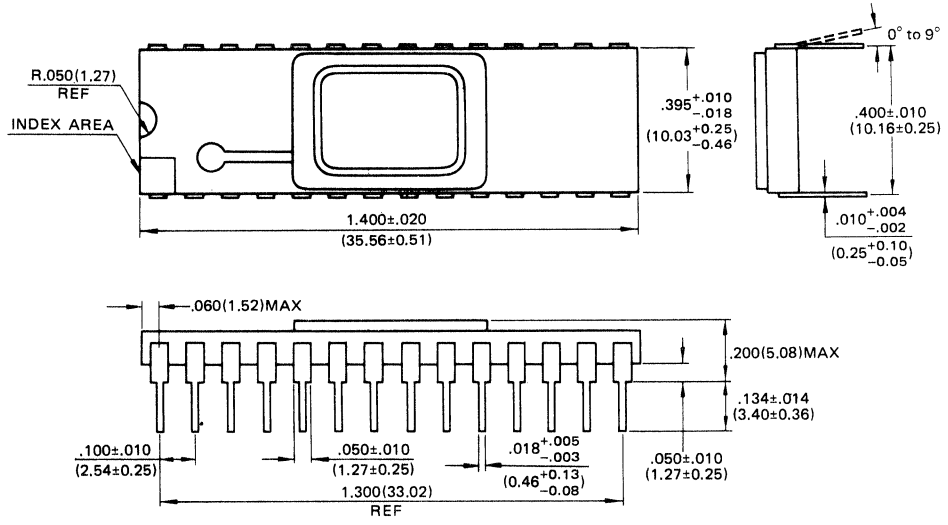
Fig. 14 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100476LL-9

December, 1988
Edition 2.0

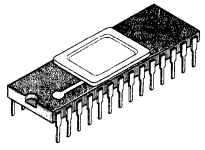
4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM100476LL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

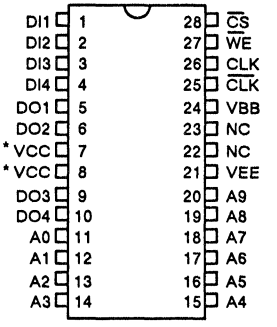
Operation for the MBM100476LL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage/temperatuere compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 9ns
  Address access time : 7ns
- Power dissipation : 1710mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

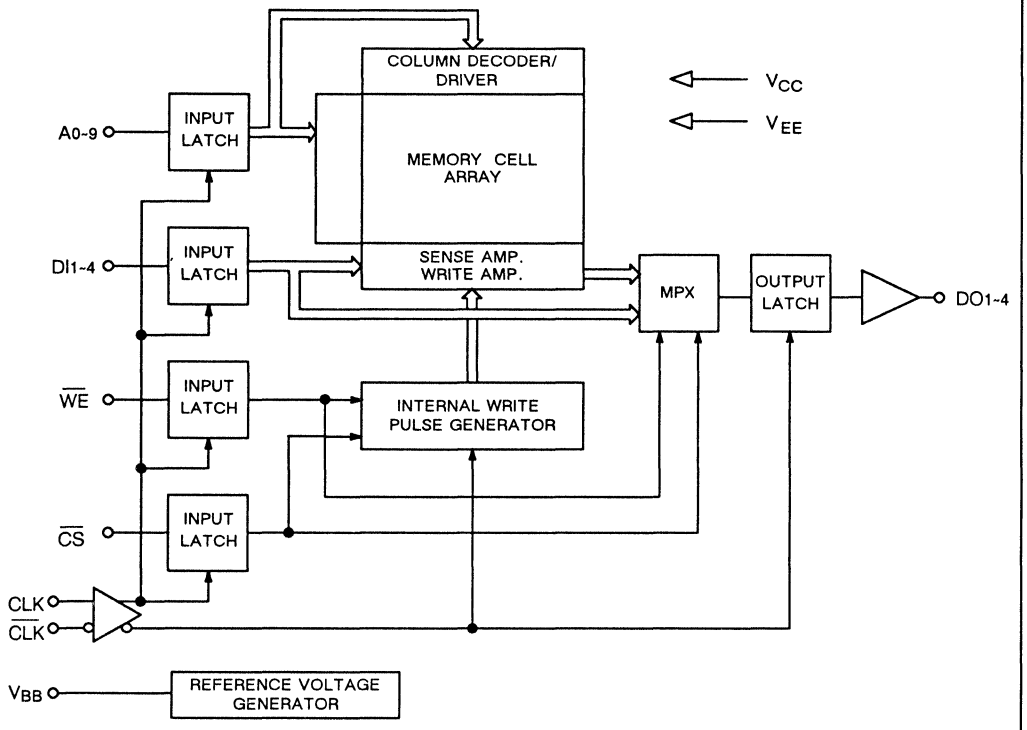
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM100476LL BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.32V)
VEE	Supply Voltage (-4.5V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TC = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100476LL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

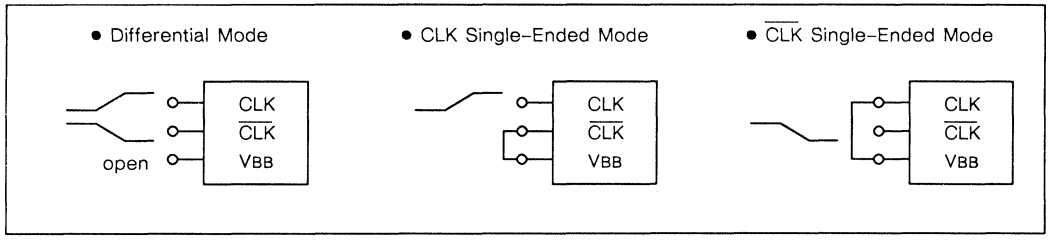
When setup time is wide enough, output data becomes valid in the short delay time (tDR) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time (tA(ADD)) similar to the traditional RAM.

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



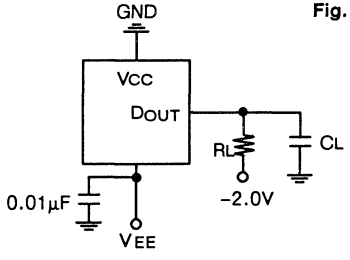
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

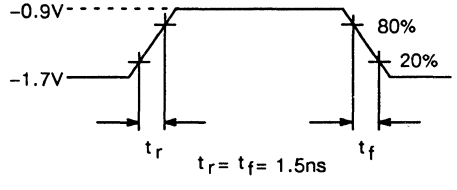
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	6.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	9.0			ns
Address Access Time	$t_{A(ADD)}$			7.0 *1	ns
Data Access Time	$t_{A(DI)}$			4.0 *2	ns
Write Access Time	$t_{A(W)}$			4.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			4.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			8.0 *5	ns
Output Delay Time	t_{DR}			3.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tSA = 1.0ns
*2 Specified at tSD = 1.0ns
*3 Specified at tSW = 1.0ns
*4 Specified at tSC = 1.0ns
*5 Specified at tWL(CLK) = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)}$ max, $t_{SA} > t_{A(ADD)}$ max, $t_{SC} > t_{A(CS)}$ max, $t_{SD} > t_{A(DI)}$ max, $t_{SW} > t_{A(W)}$ max.

Fig. 2 - AC TEST CONDITIONS



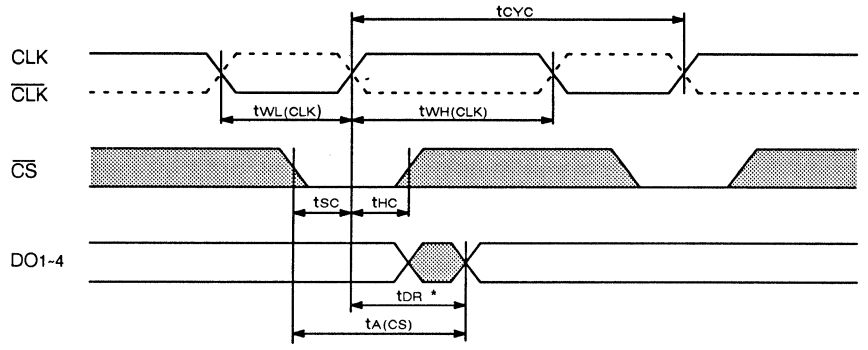
Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

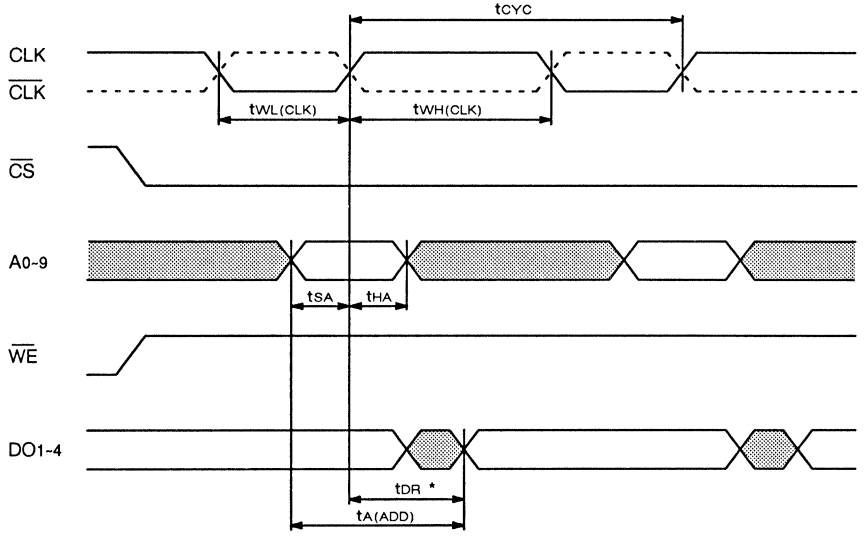
READ CYCLE TIMING DIAGRAMS

• CHIP SELECT ACCESS MODE



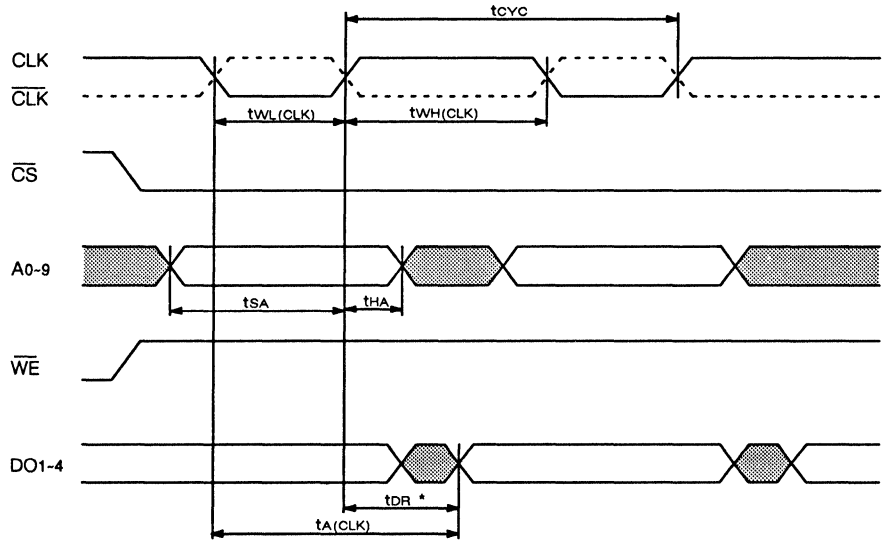
* Output is valid at tDR when tSC > tA(CS) max − tDR max.

• ADDRESS ACCESS MODE



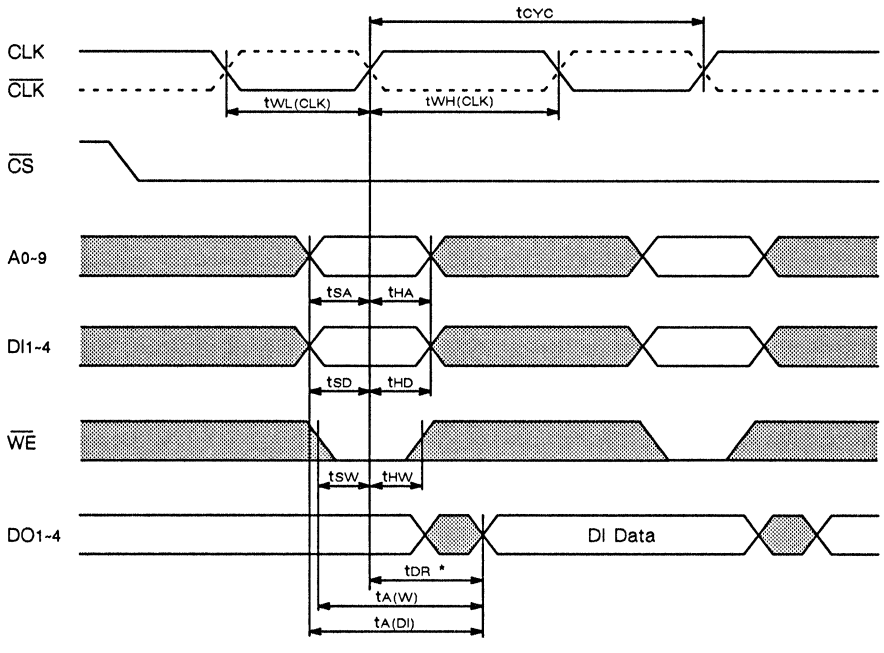
* Output is valid at tDR when tSA > tA(ADD) max − tDR max.

• CLOCK ACCESS MODE



* Output is valid at tDR when tWL(CLK) > tA(CLK) max – tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tSW > tA(W) max − tDR max and tSD > tA(DI) max − tDR max

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

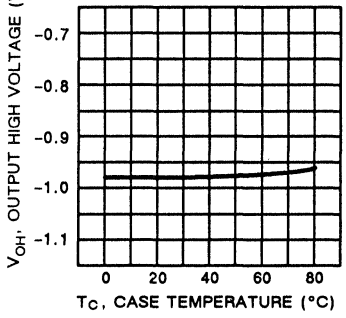


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

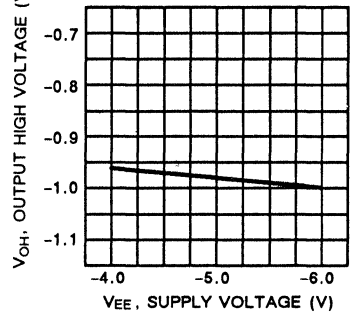


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

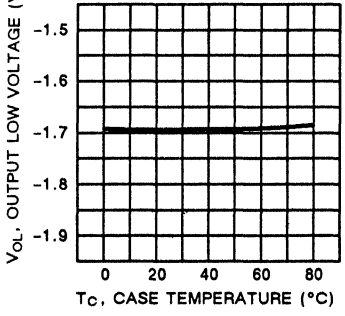


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

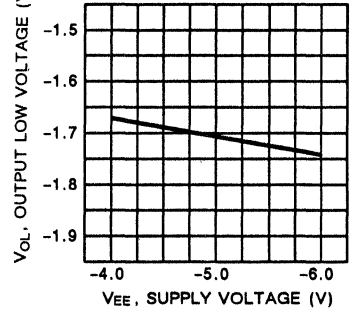


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

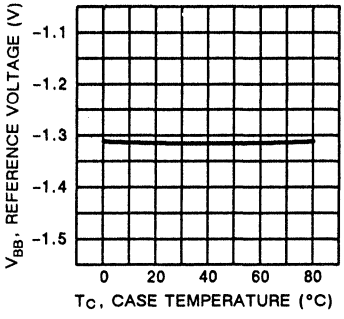
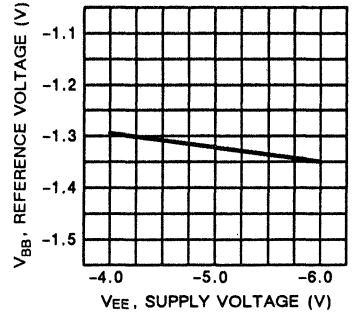


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE



3

3

Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

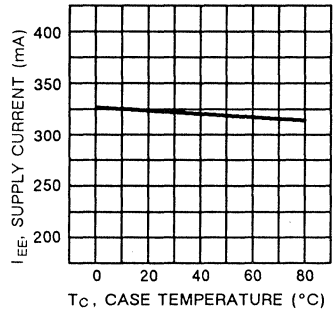


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

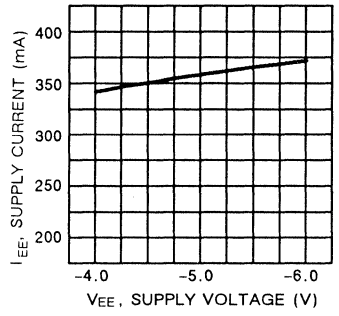


Fig. 11 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

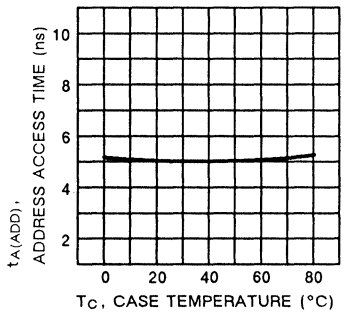


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

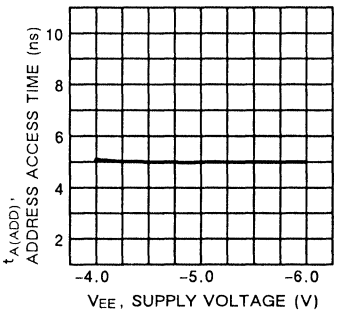


Fig. 13 – CLOCK ACCESS TIME vs CASE TEMPERATURE

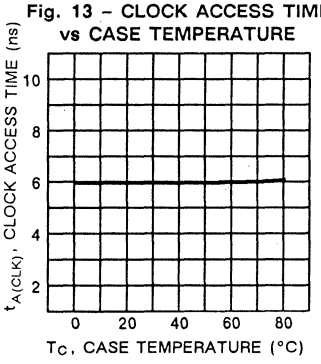


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

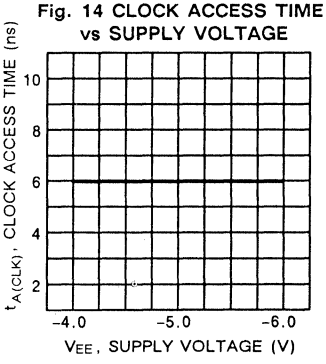


Fig. 15 - OUTPUT DELAY TIME vs CASE TEMPERATURE

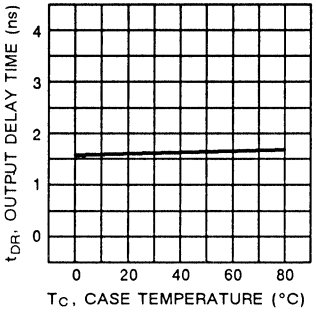


Fig. 16 - OUTPUT DELAY TIME vs SUPPLY VOLTAGE

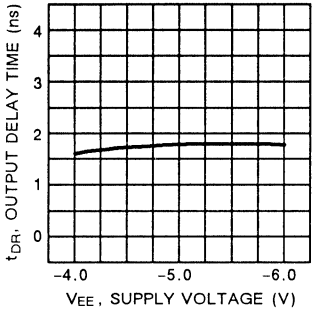


Fig. 17 - CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

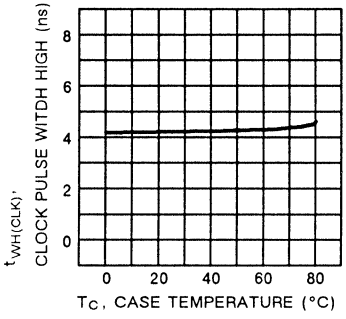
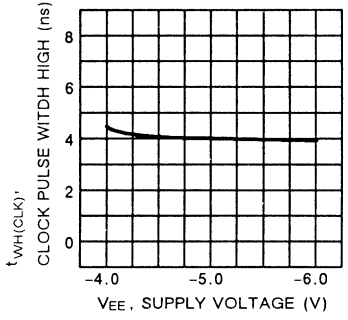


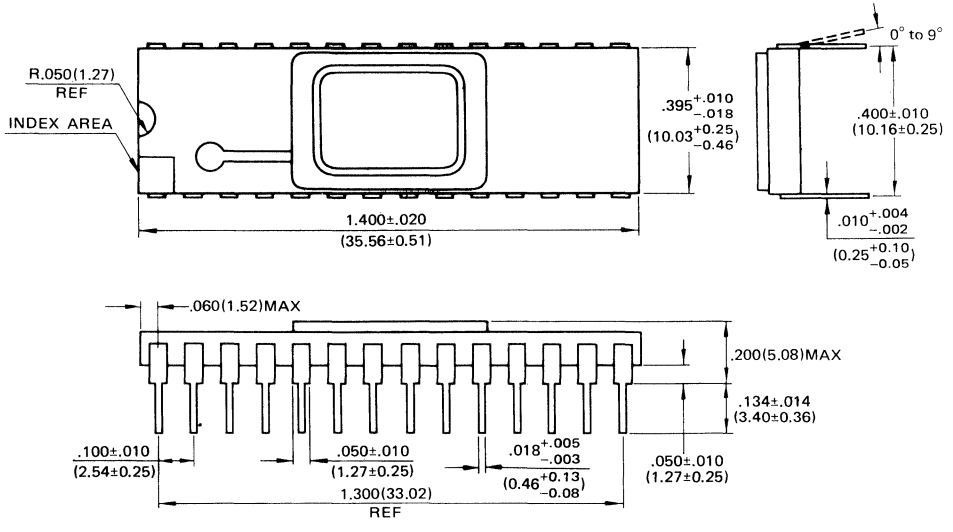
Fig. 18 - CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100476RR-9

December, 1988
Edition 1.0

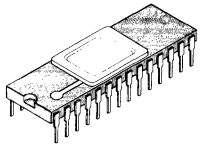
4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM100476RR-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allows to decrease the number of device on the board.

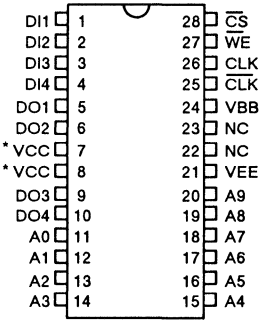
Operation for the MBM100476RR is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 1800mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

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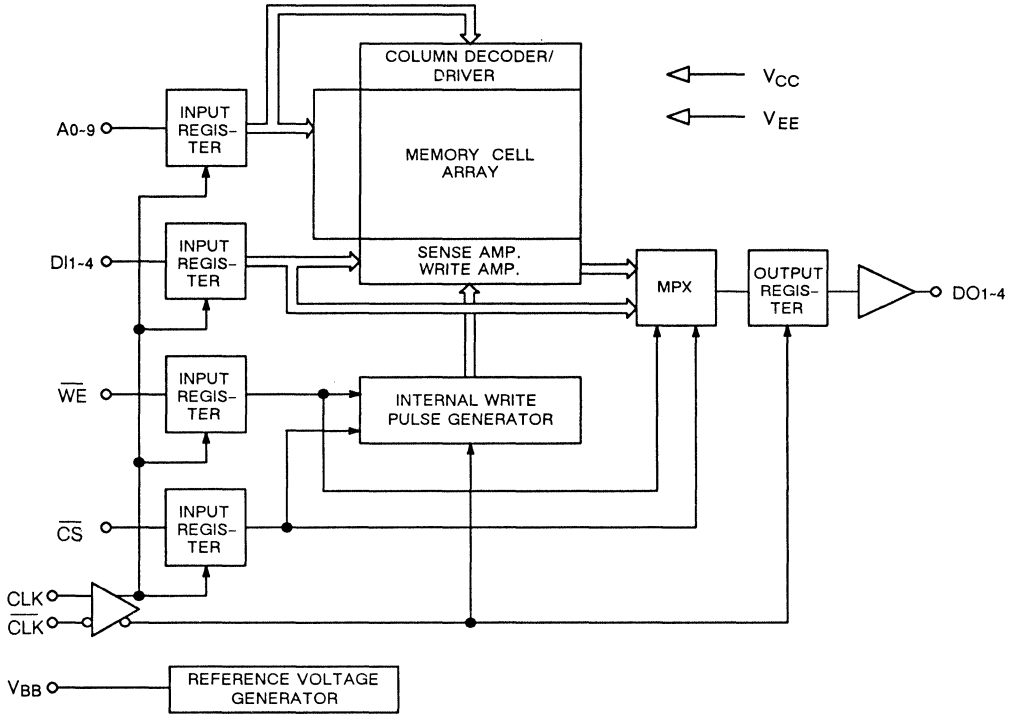
Fig.1 - MBM100476RR-9 BLOCK DIAGRAM



FUNCTION TRUTH TABLE

CS	WE	DI	CLK/CLK	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK (CLK).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
WE	Write Enable
CS	Chip Select
CLK, CLK	Clock Inputs
VBB	Reference Voltage (-1.32V)
VEE	Supply Voltage (-4.5V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V, T_C = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100476RR is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are edge triggered registered controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input and output registers are transparent when CLK ($\overline{CLK}$) goes high (low), and close to hold the data when CLK($\overline{CLK}$) goes low (high).

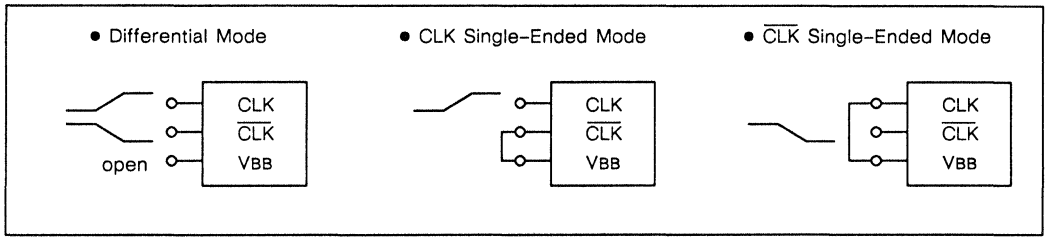
When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may not be stable during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes low (high), address data is held at output, while output data is kept valid during the same cycle. Thus, the output data becomes available at the next rising (falling) edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), inputs are transparent while previous read data appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the output by the CLK($\overline{CLK}$) rising (falling) edge of the next cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



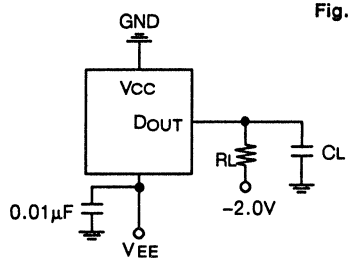
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

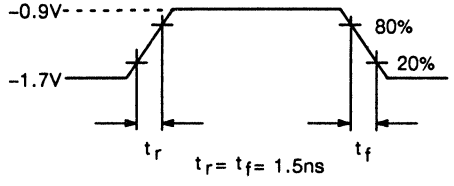
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Output Delay Time	t_{DR}			3.0	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 6.0ns
*2 Specified at tWH(CLK) > 6.0ns

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

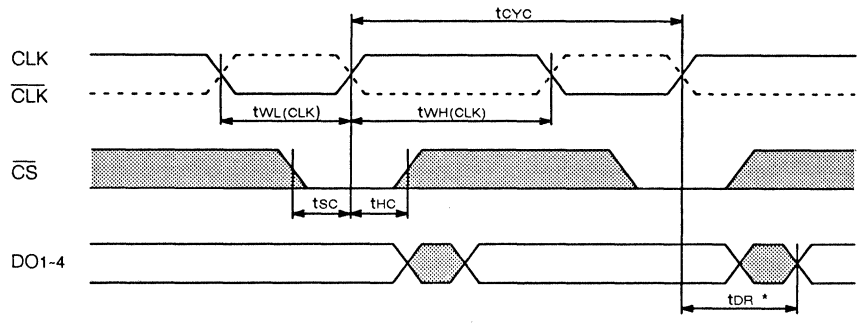


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

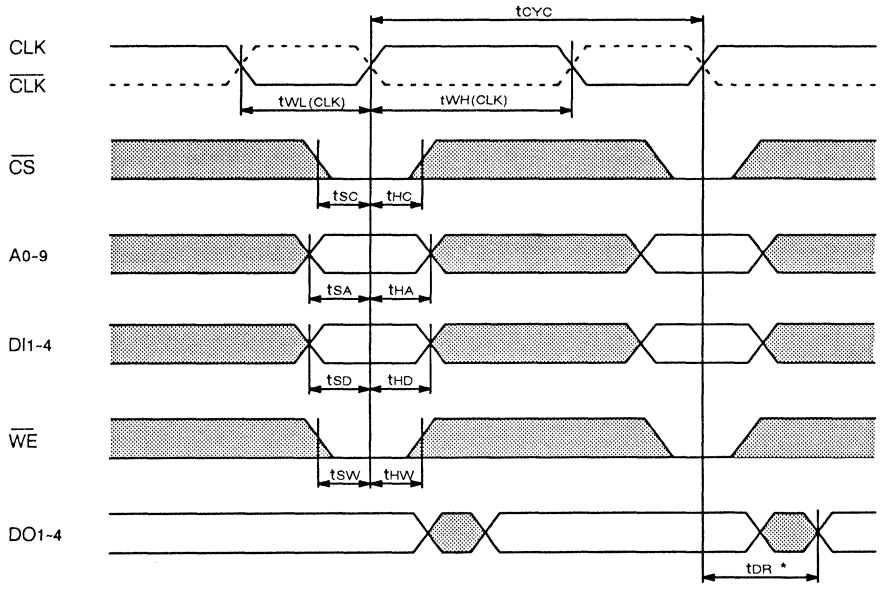
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

WRTE CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

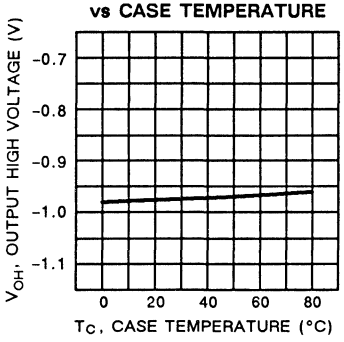


Fig. 4 - OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

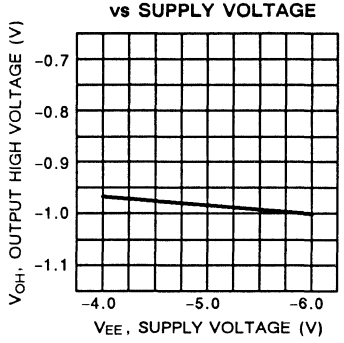


Fig. 5 - OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

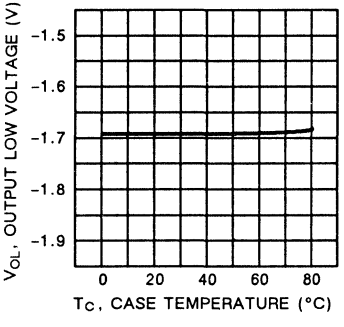


Fig. 6 - OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

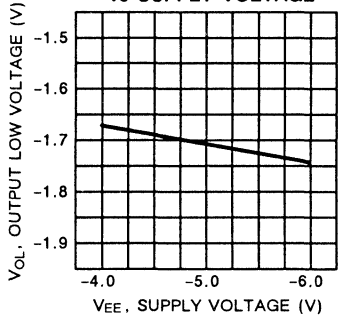


Fig. 7 - REFERENCE VOLTAGE vs CASE TEMPERATURE

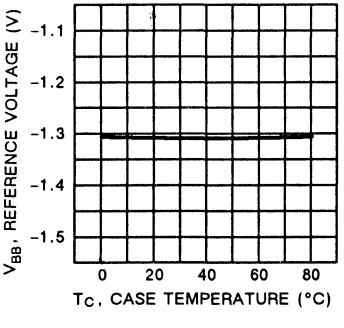


Fig. 8 - REFERENCE VOLTAGE vs SUPPLY VOLTAGE

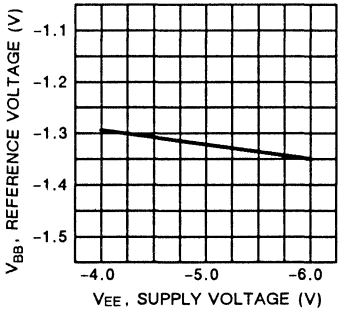


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Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

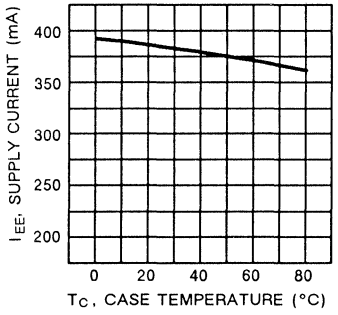


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

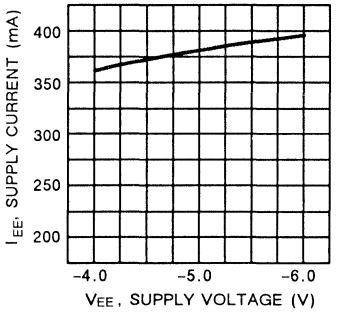


Fig. 11 – OUTPUT DELAY TIME vs CASE TEMPERATURE

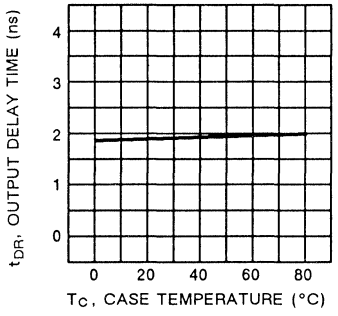
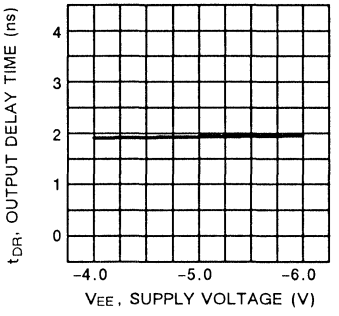


Fig. 12 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE



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PACKAGE DIMENSIONS

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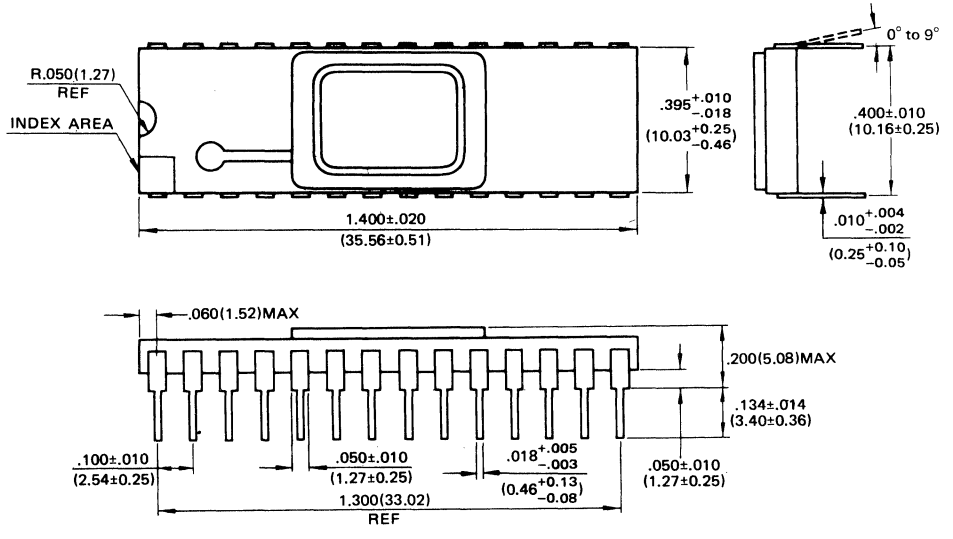
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100476RL-9

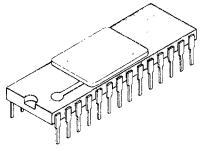
4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

December, 1988
Edition 1.0

The Fujitsu MBM100476RL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

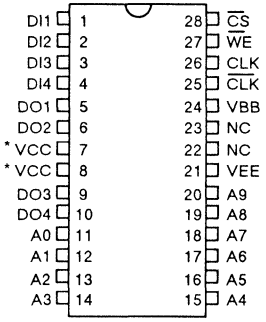
Operation for the MBM100476RL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.



CERAMIC PACKAGE
DIP-28C-A06

- 1024 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 1800MW max
- Open emitter output for ease of memory expansion
- Level-sensitive D-type latch for outputs and edge triggered registers for inputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

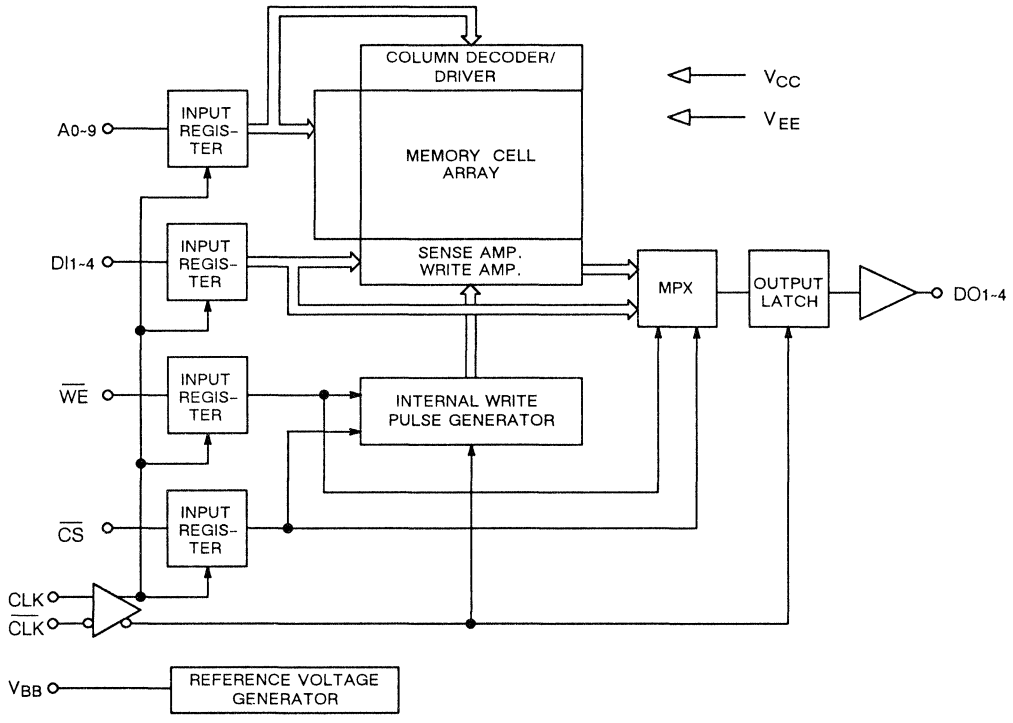
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM100476RL-9 BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

CS	WE	DI	CLK/CLK	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK (CLK).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
WE	Write Enable
CS	Chip Select
CLK, CLK	Clock Inputs
VBB	Reference Voltage (-1.32V)
VEE	Supply Voltage (-4.5V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TC = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100476RL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) furnish edge triggered registers, whereas outputs (DOUT) have level sensitive transparent latches.

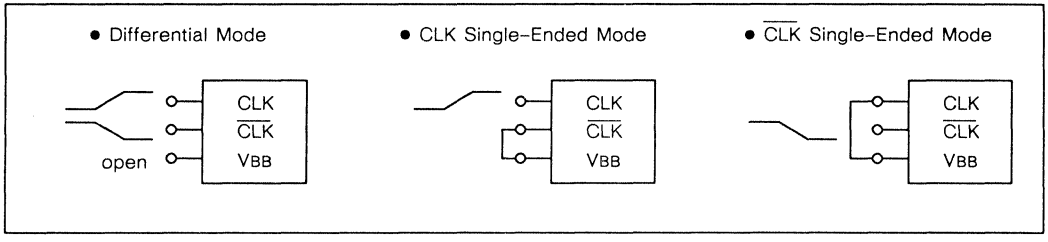
When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. All input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels are free to change for the rest of the cycle time once input data is held into the input register. Read out data becomes available during CLK low state in which output latches are transpatent. When CLK ($\overline{CLK}$) state is wide enough than the internal RAM access time, output data become valid in the short delay time (tDR) after the falling (rising) edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



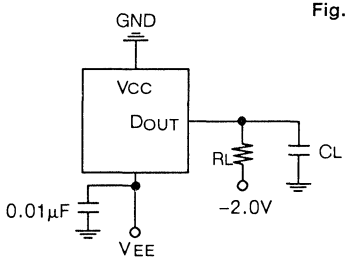
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V ±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

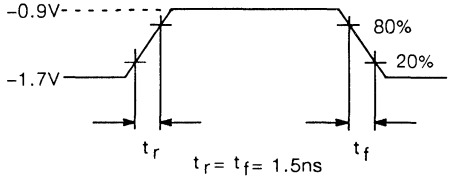
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Clock Access Time	$t_{A(CLK)}$			8.0 *3	ns
Output Delay Time	t_{DR}			3.0 *4	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 6.0ns
*2 Specified at tWH(CLK) > 6.0ns
*3 Specified at tWH(CLK) = 3.0ns
*4 Specified at tWH(CLK) > tA(CLK) max

Fig. 2 - AC TEST CONDITIONS



Output Lead : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

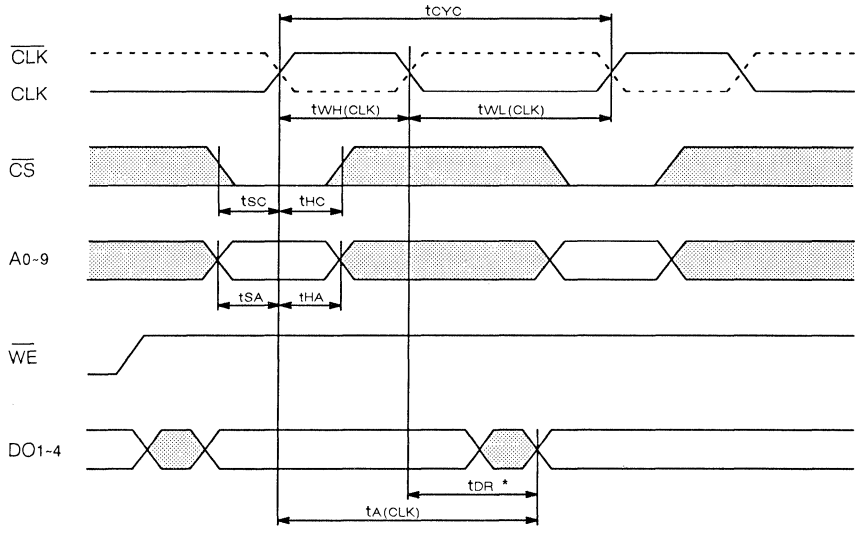


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

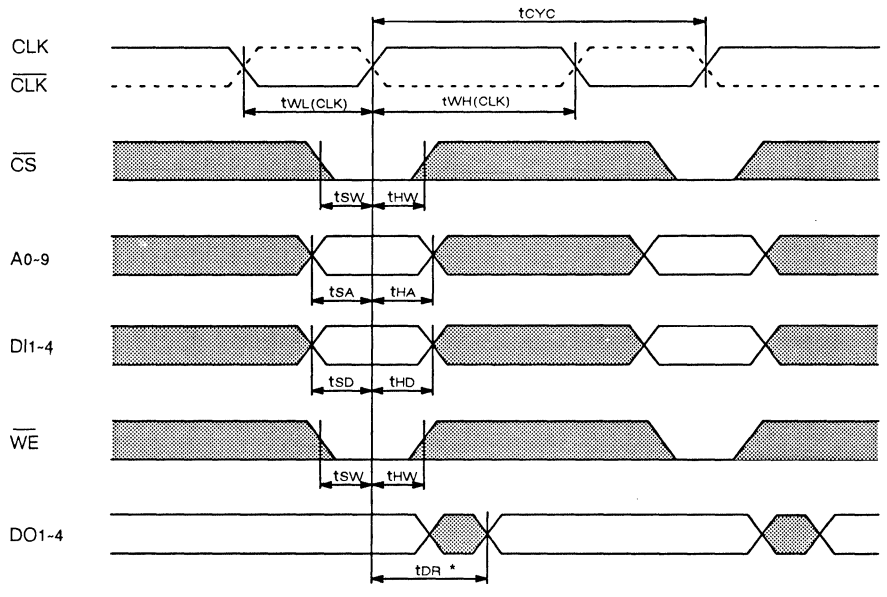
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max − tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max − tDR max.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

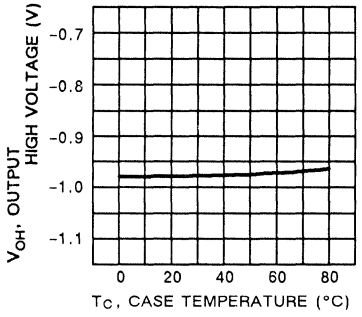


Fig. 4 - OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

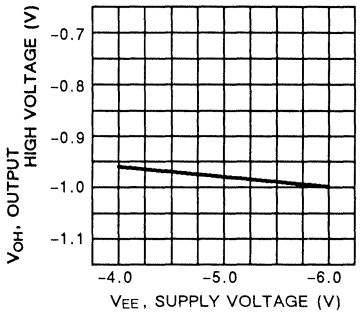


Fig. 5 - OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

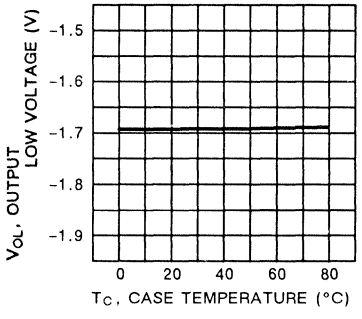


Fig. 6 - OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

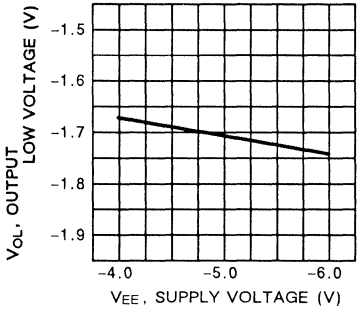


Fig. 7 - REFERENCE VOLTAGE vs CASE TEMPERATURE

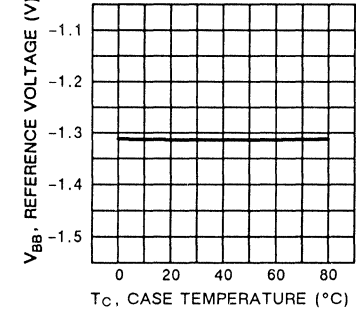


Fig. 8 - REFERENCE VOLTAGE vs SUPPLY VOLTAGE

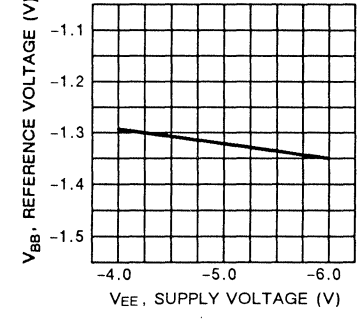


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Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

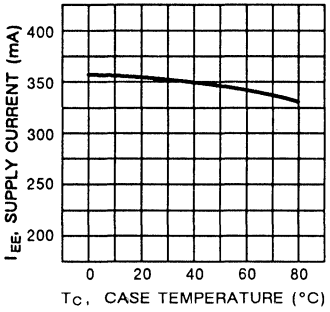


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

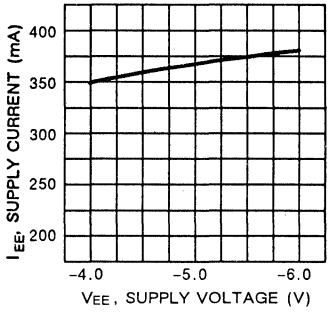


Fig. 11 – CLOCK ACCESS TIME vs CASE TEMPERATURE

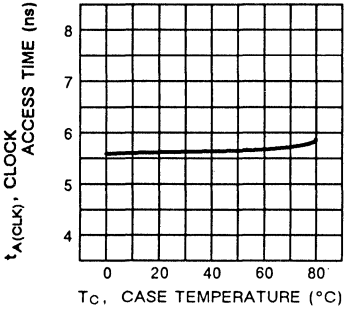


Fig. 12 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

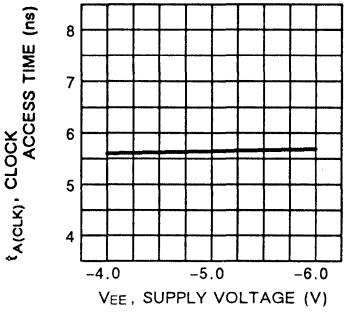


Fig. 13 – OUTPUT DELAY TIME vs CASE TEMPERATURE

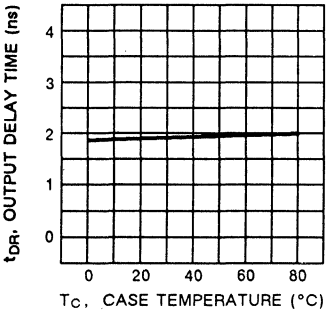
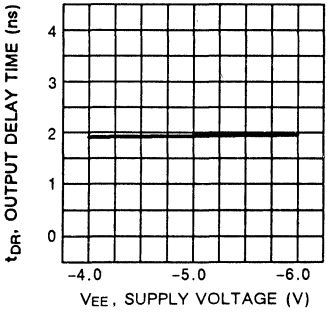


Fig. 14 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE



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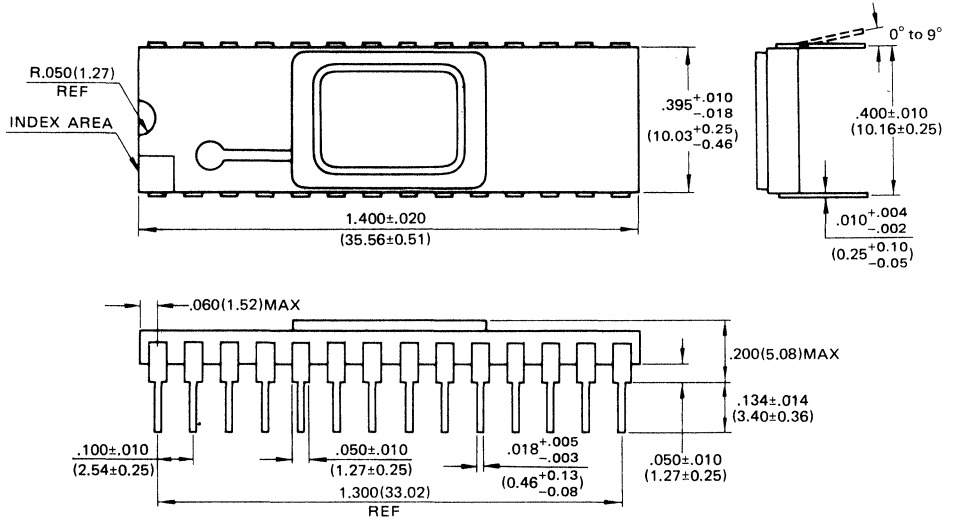
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10486LL-13

16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

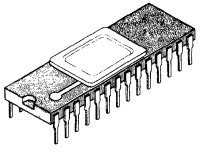
December, 1988
Edition 2.0

The Fujitsu MBM10486LL-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

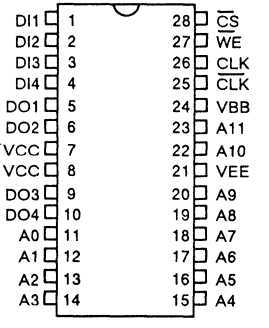
Operation for the MBM10486LL is specified over a case temperature range of from 0°C to 75°C (T_C). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 4096 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 13ns
  Address access time : 10ns
- Power dissipation : 1976mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

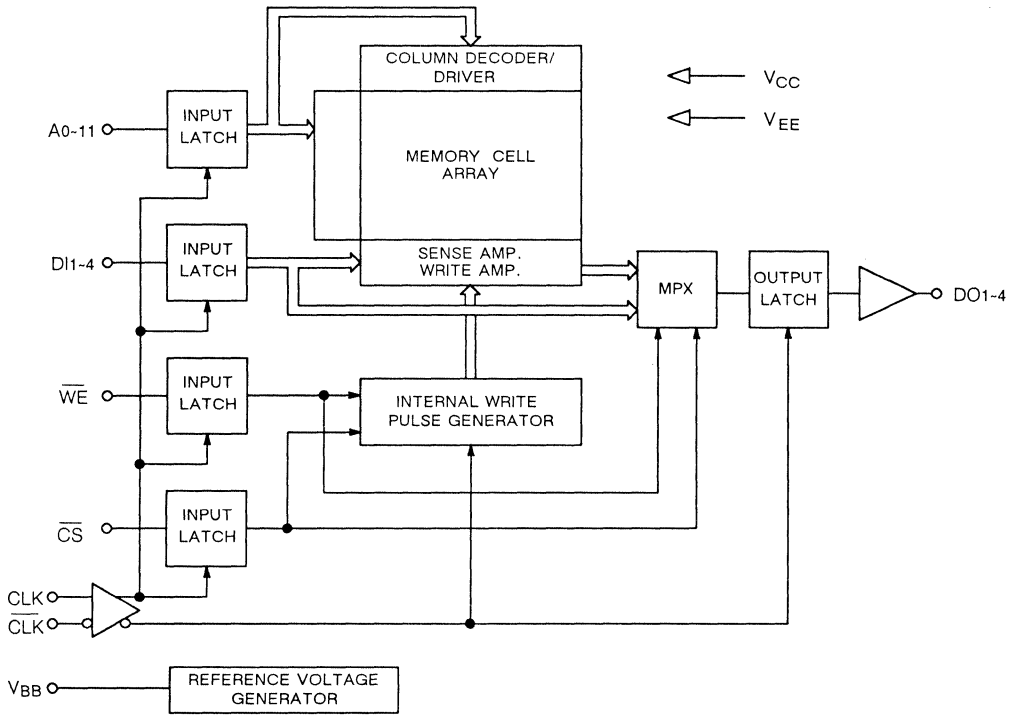
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10486LL BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.29V)
VEE	Supply Voltage (-5.2V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10486LL is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A11. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (t_S) and the hold time (t_H) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input level may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

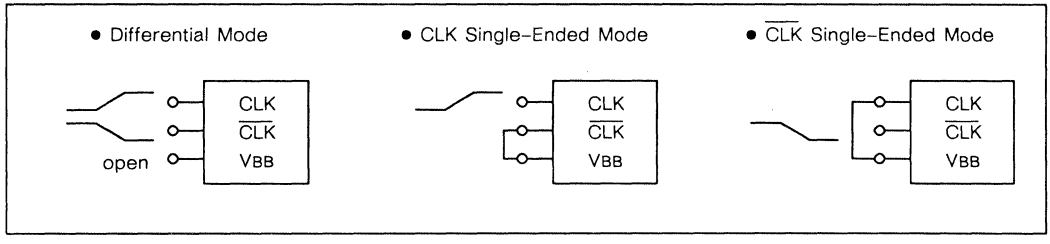
When setup time is wide enough, output data becomes valid in the short delay time (t_{DR}) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time ($t_{A(ADD)}$) similar to the traditional RAM.

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (V_{BB}) pin. When CLK and $\overline{CLK}$ are used as differential inputs, V_{BB} pin is left open.



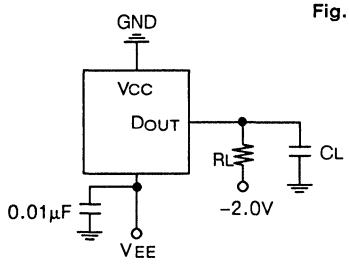
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

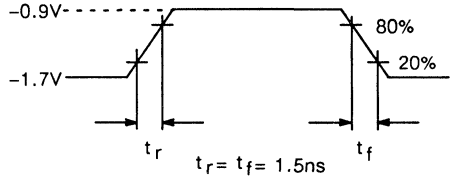
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	10.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	13.0			ns
Address Access Time	$t_{A(ADD)}$			10.0 *1	ns
Data Access Time	$t_{A(DI)}$			5.0 *2	ns
Write Access Time	$t_{A(W)}$			5.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			5.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			11.0 *5	ns
Output Delay Time	t_{DR}			4.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tSA = 1.0ns
*2 Specified at tSD = 1.0ns
*3 Specified at tSW = 1.0ns
*4 Specified at tSC = 1.0ns
*5 Specified at tWL(CLK) = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)\ max}$, $t_{SA} > t_{A(ADD)\ max}$, $t_{SC} > t_{A(CS)\ max}$, $t_{SD} > t_{A(DI)\ max}$, $t_{SW} > t_{A(W)\ max}$.

Fig. 2 - AC TEST CONDITIONS



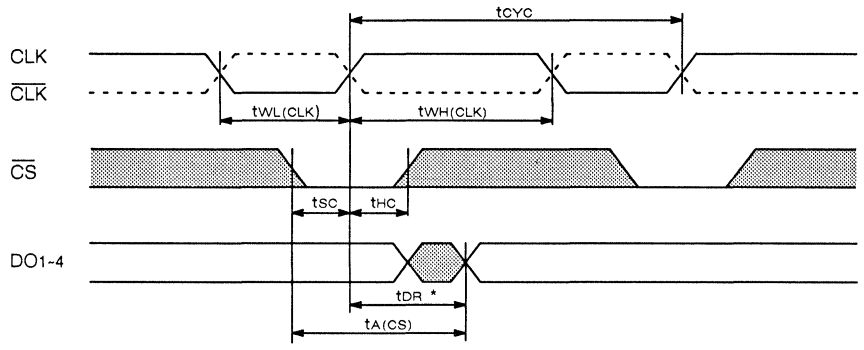
Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

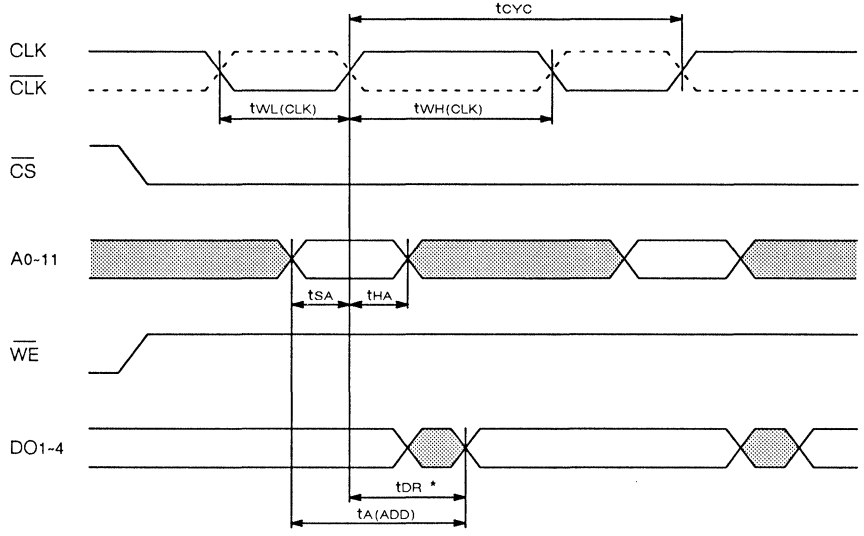
READ CYCLE TIMING DIAGRAMS

- CHIP SELECT ACCESS MODE



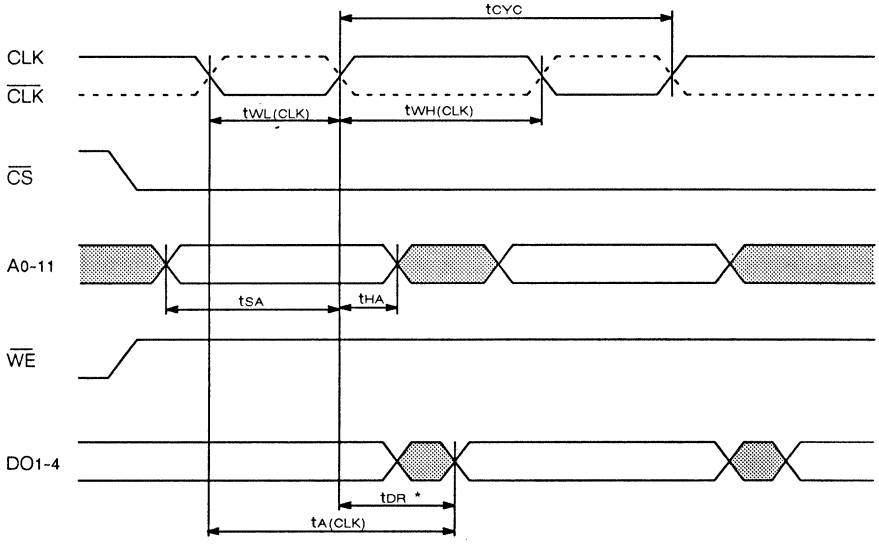
* Output is valid at t_{DR} when $t_{SC} > t_{A(CS)\ max} - t_{DR\ max}$.

- ADDRESS ACCESS MODE



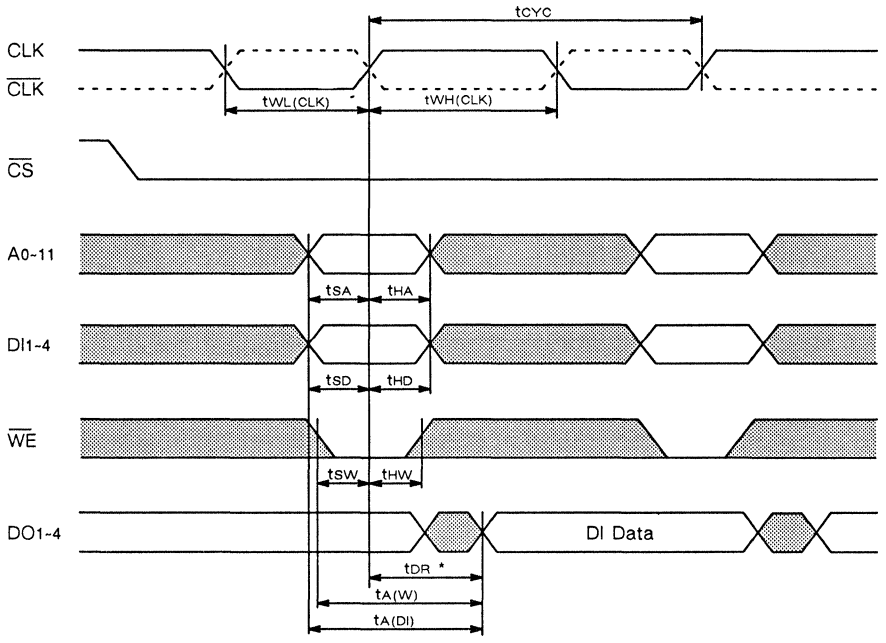
* Output is valid at t_{DR} when $t_{SA} > t_{A(ADD)\ max} - t_{DR\ max}$.

● CLOCK ACCESS MODE



* Output is valid at tDR when tWL(CLK) > tA(CLK) max − tDR max

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tSW > tA(W) max − tDR max and tSD > tA(DI) max − tDR max

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

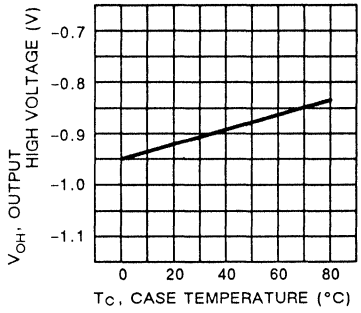


Fig. 4 - OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

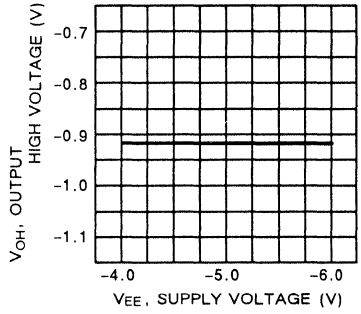


Fig. 5 - OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

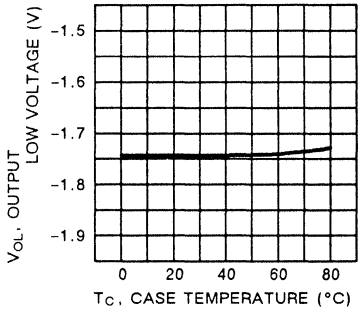


Fig. 6 - OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

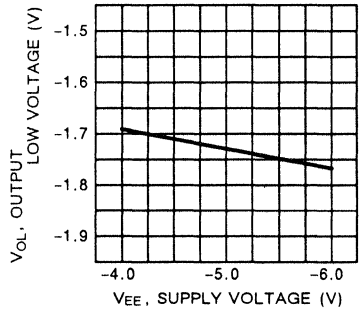


Fig. 7 - REFERENCE VOLTAGE vs CASE TEMPERATURE

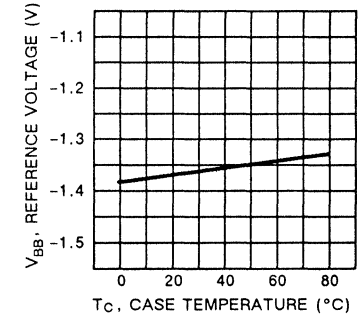
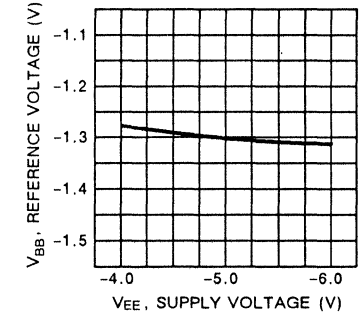


Fig. 8 - REFERENCE VOLTAGE vs SUPPLY VOLTAGE



3

Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

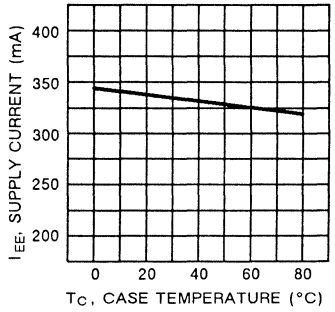


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

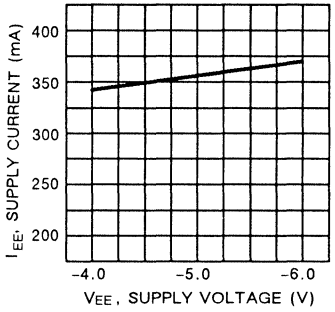


Fig. 11 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

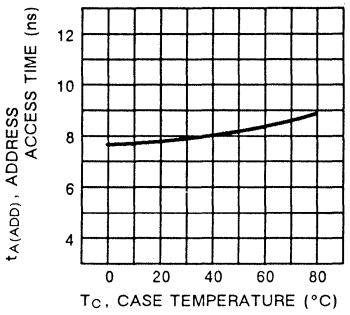


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

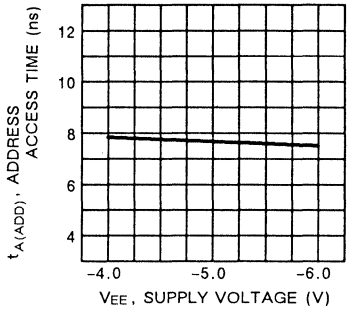


Fig. 13 – CLOCK ACCESS TIME vs CASE TEMPERATURE

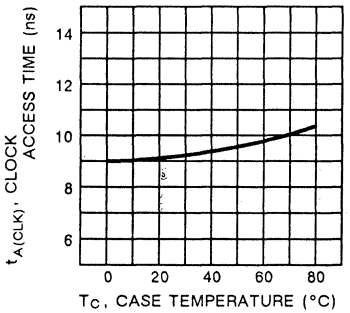


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

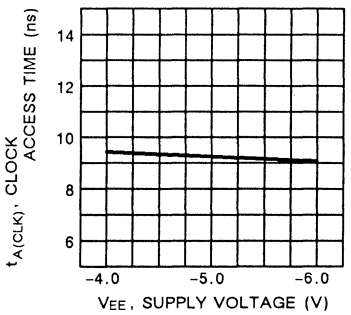


Fig. 15 - OUTPUT DELAY TIME vs CASE TEMPERATURE

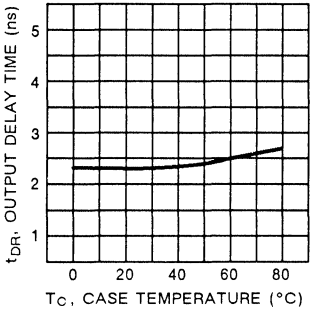


Fig. 16 - OUTPUT DELAY TIME vs SUPPLY VOLTAGE

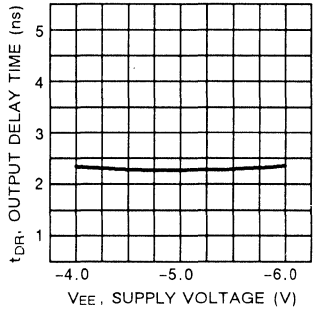


Fig. 17 - CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

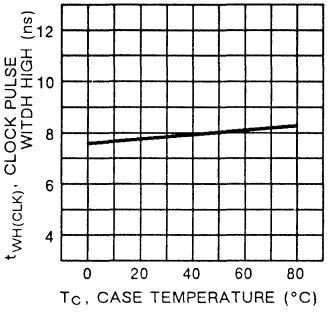
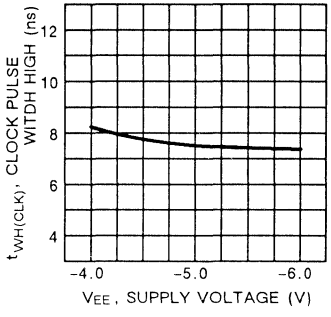


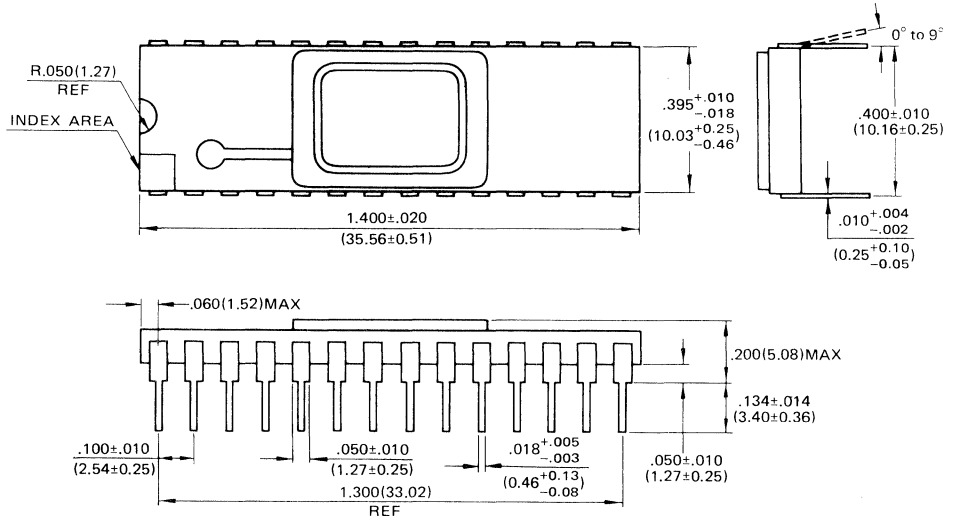
Fig. 18 - CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MBM10486RR-13

16384–BIT BIPOLAR SELF–TIMED RAMDOM ACCESS MEMORY

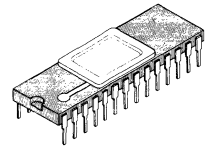
DESCRIPTION

The Fujitsu MBM10486RR–13 is fully decoded 16384–bit ECL self–timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on–chip voltage compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allowsto decrease the number of device on the board.

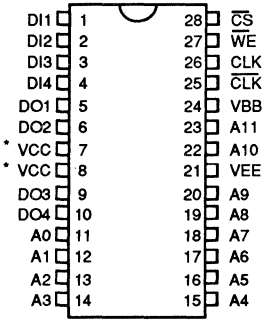
Operation for the MBM10486RR is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28–pin ceramic side brazed DIP and fully compatible with industry standard 10K–series ECL families.

- 4096 words by 4 bits organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 13ns
  Output delay time : 4ns
- Power dissipation : 2184mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Option clock inputs : single ended or differential
- DOPOS and IOP–II processing
- 28–pin ceramic side–brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP–28C–A06

PIN ASSIGNMENT
(TOP VIEW)



* V cc grounded

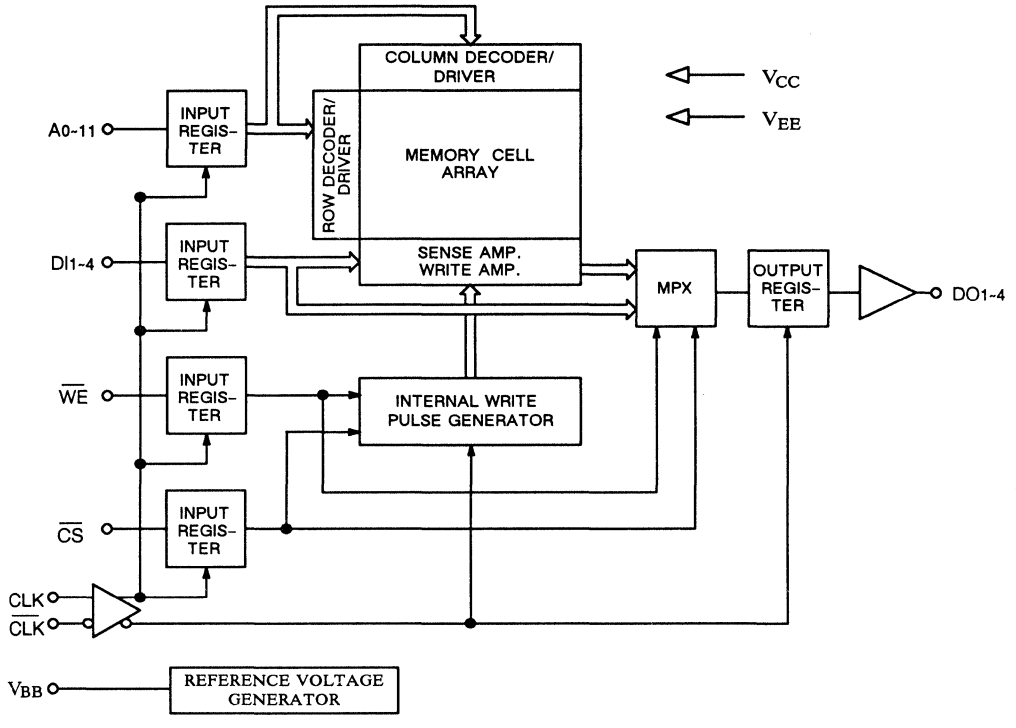
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Temperature under bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10486RR-13 BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address inputs
DI1 thru DI4	Data inputs
DO1 thru DO4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
CLK, $\overline{CLK}$	Clock inputs
VBB	Reference voltage (-1.32V)
VEE	Supply voltage (-4.5V)
VCC	Supply voltage (0V)
NC	No connection

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω to -2.0V, T_C = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-420			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10486RR is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are edge triggered registered controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input and output registers are transparent when CLK ($\overline{CLK}$) goes high (low), and close to hold the data when CLK($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may not be stable during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes low (high), address data is held at output, while output data is kept valid during the same cycle. Thus, the output data becomes available at the next rising (falling) edge of CLK ($\overline{CLK}$).

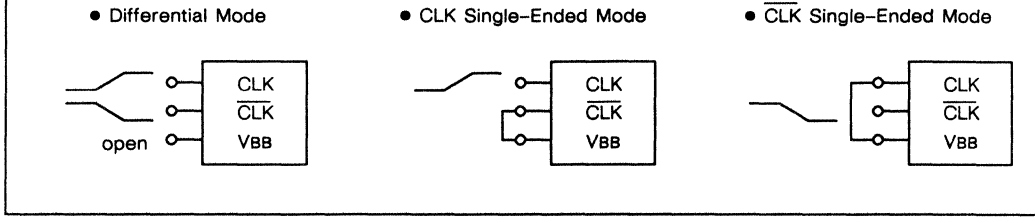
The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), inputs are transparent while previous read data appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the output by the CLK($\overline{CLK}$) rising (falling) edge of the next cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.

Fig. 2 - OPTION CLOCK INPUTS



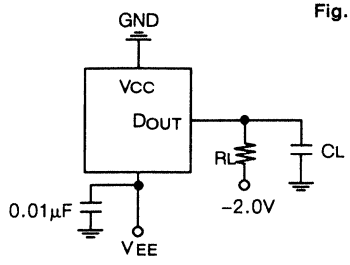
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

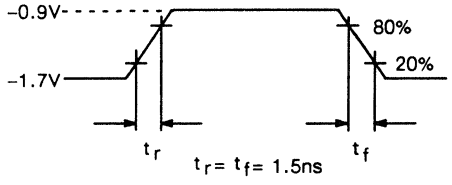
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	5.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	5.0 *2			ns
Cycle Time	t_{CYC}	13.0			ns
Output Delay Time	t_{DR}			4.0	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 8.0ns
*2 Specified at tWH(CLK) > 8.0ns

Fig. 3 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

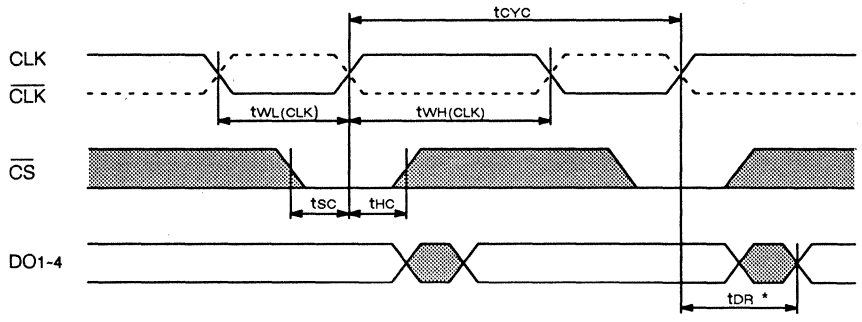


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

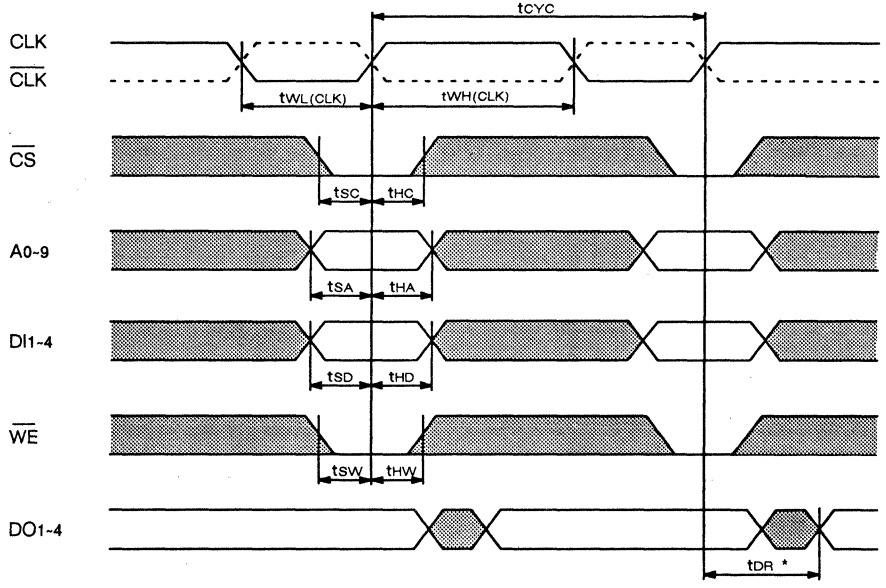
READ CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

3

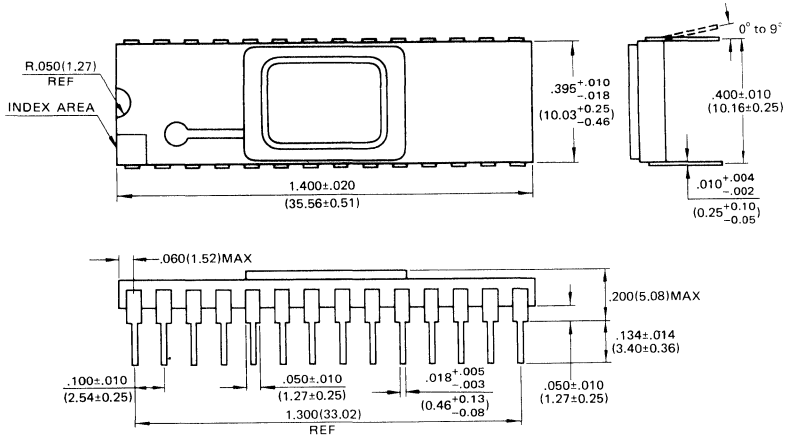
WRTE CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MBM10486RL-13

16384–BIT BIPOLAR SELF–TIMED RAMDOM ACCESS MEMORY

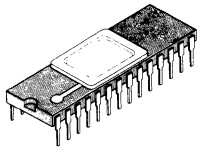
DESCRIPTION

The Fujitsu MBM10486RL–13 is fully decoded 16384–bit ECL self–timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on–chip voltage compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

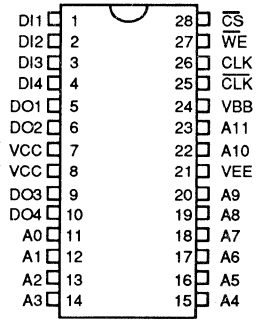
Operation for the MBM10486RL is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28–pin ceramic side brazed DIP and fully compatible with industry standard 10K–series ECL families.

- 4096 words by 4 bits organization
- On–chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 13ns
  Output delay time : 4ns
- Power dissipation : 2.08W max
- Open emitter output for ease of memory expansion
- Level–sensitive D–type latch for outputs and edge triggered registers for inputs
- Internal write pulse generator
- Option clock inputs : single ended or differential
- DOPOS and IOP–II processing
- 28–pin ceramic side–brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP–28C–A06

PIN ASSIGNMENT
(TOP VIEW)



* V cc grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

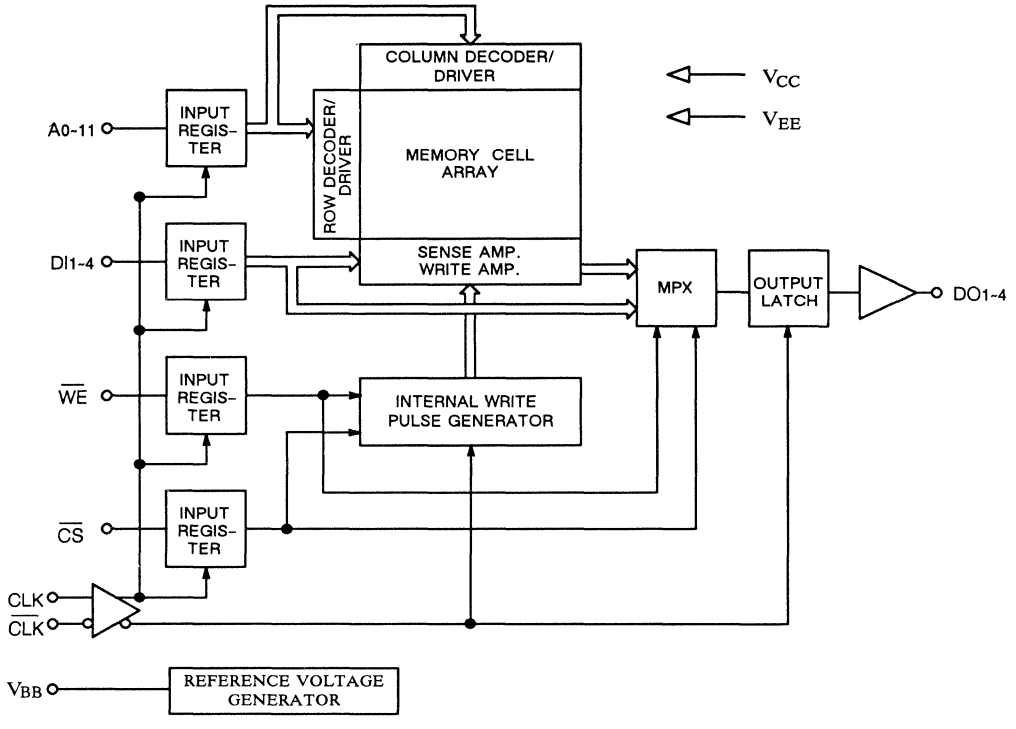
Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Temperature under bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

3

Fig.1 - MBM10486RL-13 BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address inputs
DI1 thru DI4	Data inputs
DO1 thru DO4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
CLK, $\overline{CLK}$	Clock inputs
VBB	Reference voltage (-1.29V)
VEE	Supply voltage (-5.2V)
VCC	Supply voltage (0V)
NC	No connection

GUARANTEED OPERATING CONDITIONS

(Referenced to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10486RL is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A11. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) furnish edge triggered registers, whereas outputs (DOUT) have level sensitive transparent latches.

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. All input data such as $\overline{CS}$ $\overline{WE}$, Address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input level are free to change for the rest of the cycle time once input data is held into the input register. Read out data becomes available during CLK low state in which output latches are transpatent. When CLK ($\overline{CLK}$) state is wide enough than the internal RAM access time, output data become valid in the short delay time (tDR) after the falling (rising)edge of CLK ($\overline{CLK}$).

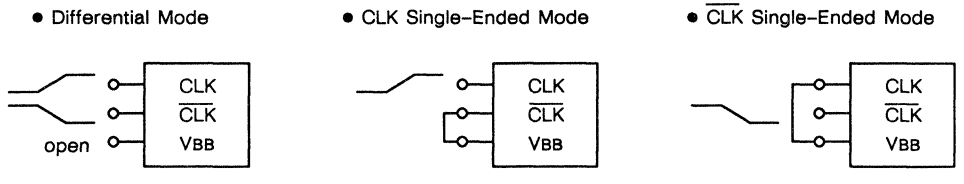
The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the address location. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.

Fig. 2 - OPTION CLOCK INPUTS



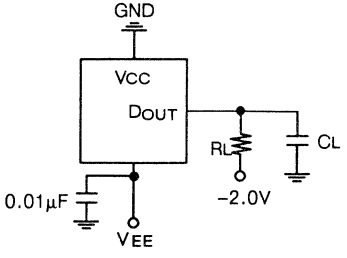
AC CHARACTERISTICS

(VCC = 0V, VEE = −5.2V±5%, Output Load = 50Ω to −2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

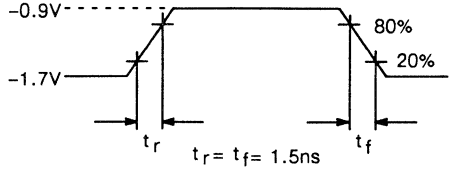
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	5.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	5.0 *2			ns
Cycle Time	t_{CYC}	13.0			ns
Clock Access Time	$t_{A(CLK)}$			12.0 *3	ns
Output Delay Time	t_{DR}			4.0 *4	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) >8.0ns
*2 Specified at tWH(CLK) > 8.0ns
*3 Specified at tWH(CLK) = 5.0ns
*4 Specified at tWH(CLK) > tA(CLK) max

Fig. 3 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

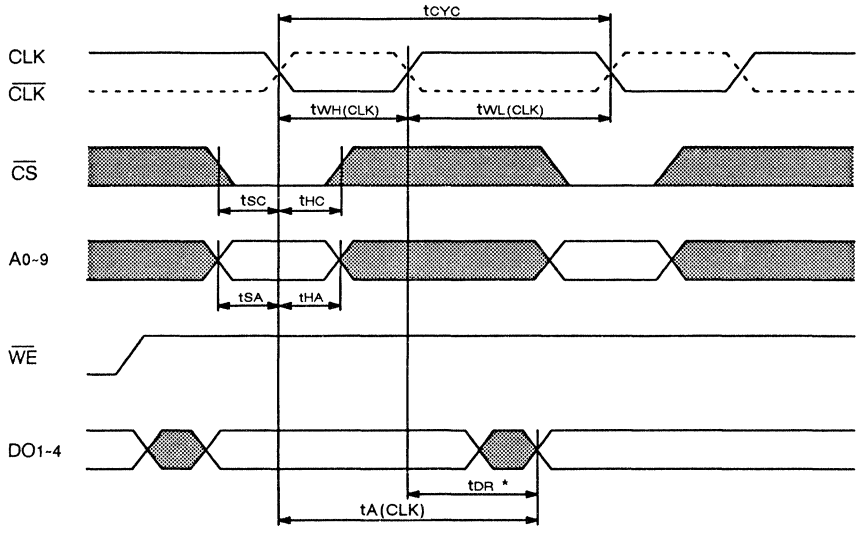


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

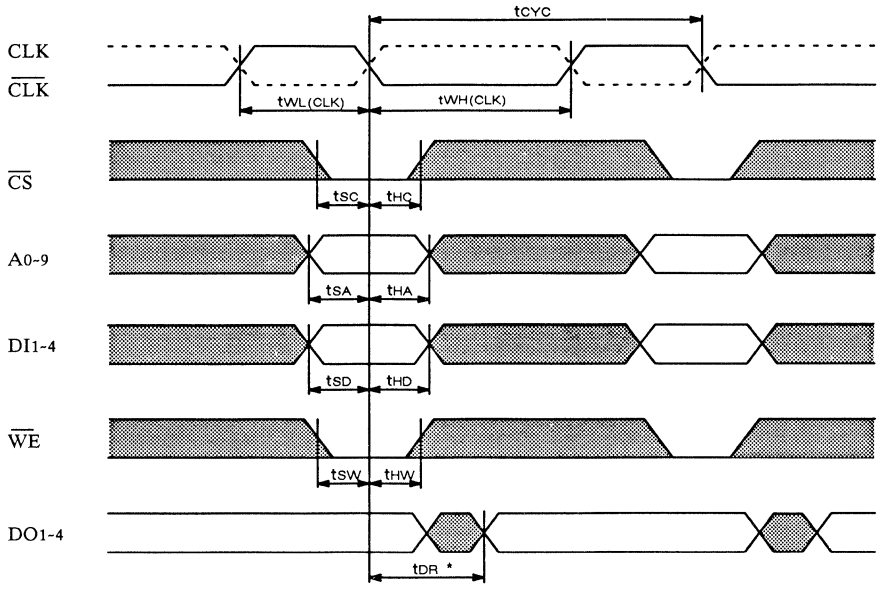
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

Fig. 4– READ CYCLE TIMING DIAGRAMS



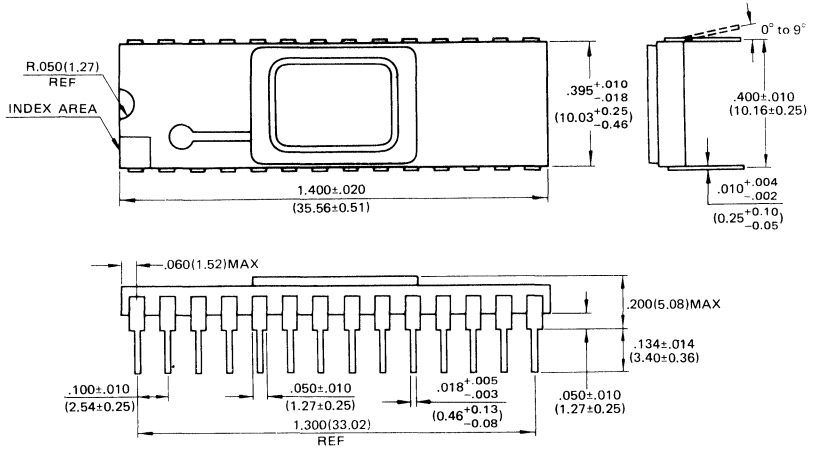
* Output is valid at tDR when tWH(CLK) > tA(CLK) max – tDR max.

Fig. 5 – WRTE CYCLE TIMING DIAGRAMS



PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

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FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100486LL-13

16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

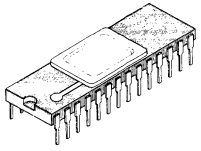
December, 1988
Edition 2.0

The Fujitsu MBM100486LL-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

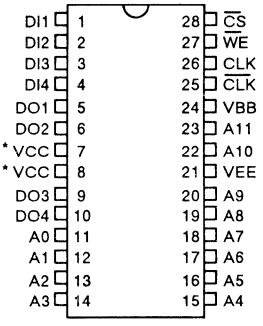
Operation for the MBM100486LL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 4096 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 13ns
  Address access time : 10ns
- Power dissipation : 1710mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

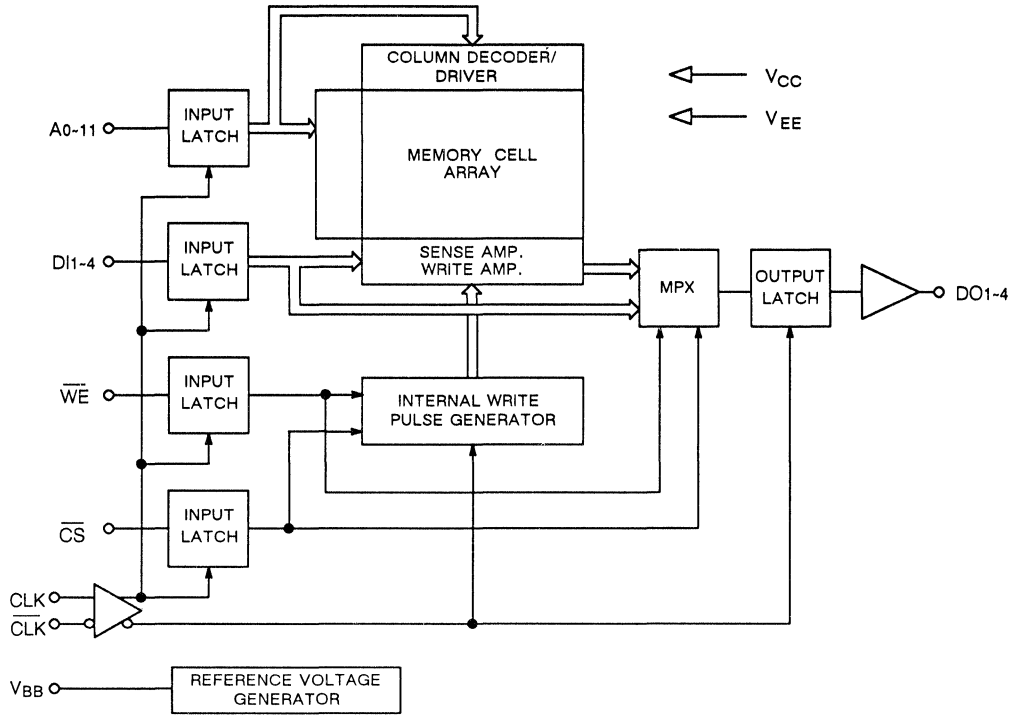
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM100486LL BLOCK DIAGRAM



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FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

 : Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.32V)
VEE	Supply Voltage (-4.5V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TC = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10486LL is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A11. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input level may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

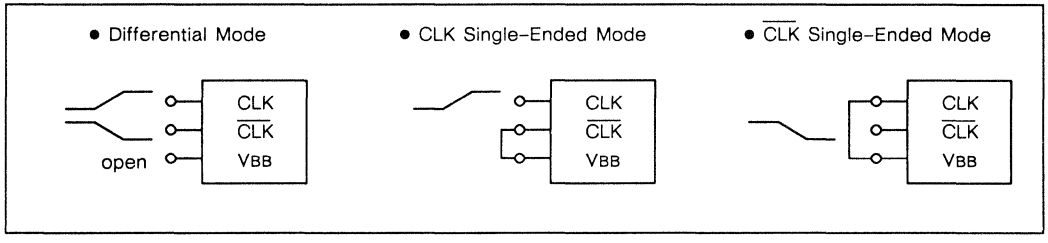
When setup time is wide enough, output data becomes valid in the short delay time (tDR) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time (tA(ADD)) similar to the traditional RAM.

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



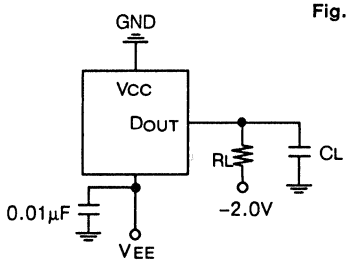
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

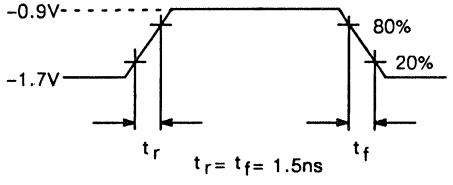
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	10.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	13.0			ns
Address Access Time	$t_{A(ADD)}$			10.0 *1	ns
Data Access Time	$t_{A(DI)}$			5.0 *2	ns
Write Access Time	$t_{A(W)}$			5.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			5.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			11.0 *5	ns
Output Delay Time	t_{DR}			4.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tSA = 1.0ns
*2 Specified at tSD = 1.0ns
*3 Specified at tSW = 1.0ns
*4 Specified at tSC = 1.0ns
*5 Specified at tWL(CLK) = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)\ max}$, $t_{SA} > t_{A(ADD)\ max}$, $t_{SC} > t_{A(CS)\ max}$, $t_{SD} > t_{A(DI)\ max}$, $t_{SW} > t_{A(W)\ max}$.

Fig. 2 - AC TEST CONDITIONS



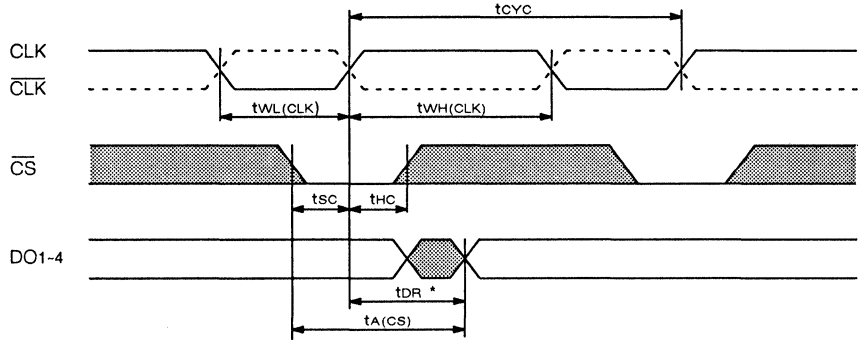
Output Lead : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

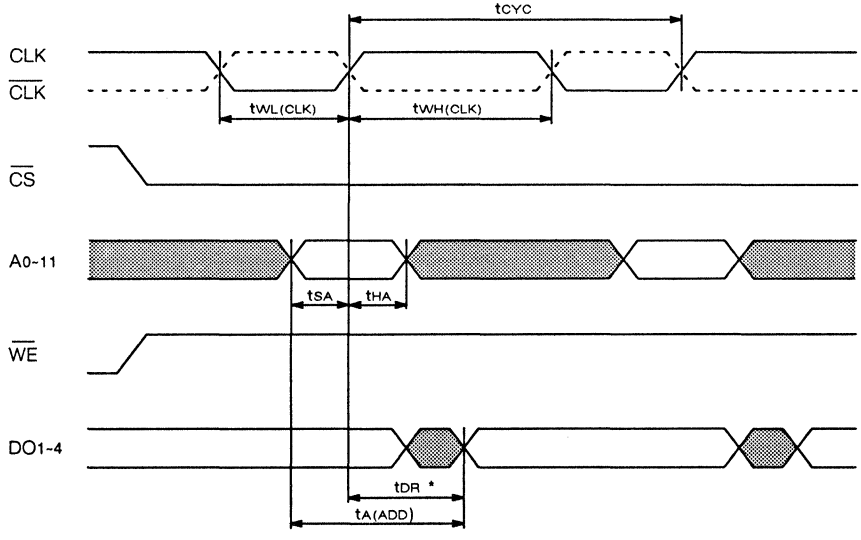
READ CYCLE TIMING DIAGRAMS

• CHIP SELECT ACCESS MODE



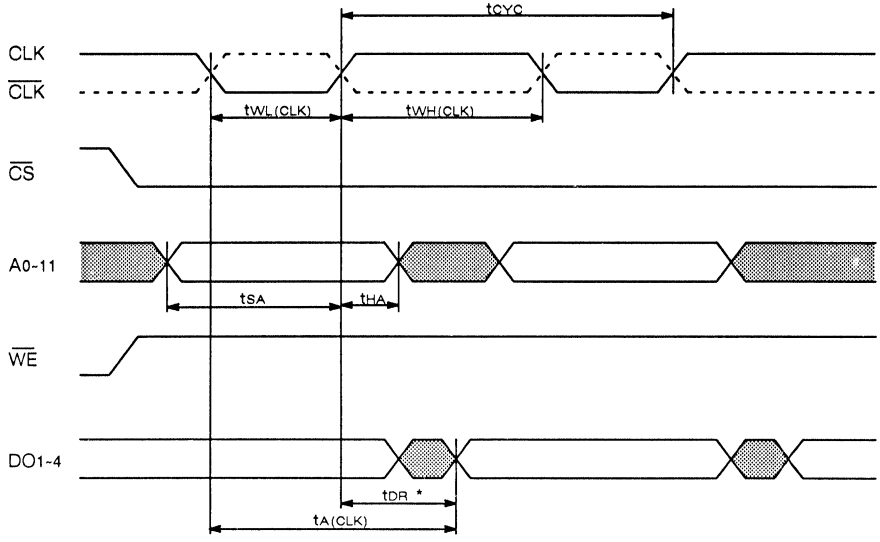
* Output is valid at tDR when tSC > tA(CS) max – tDR max.

• ADDRESS ACCESS MODE



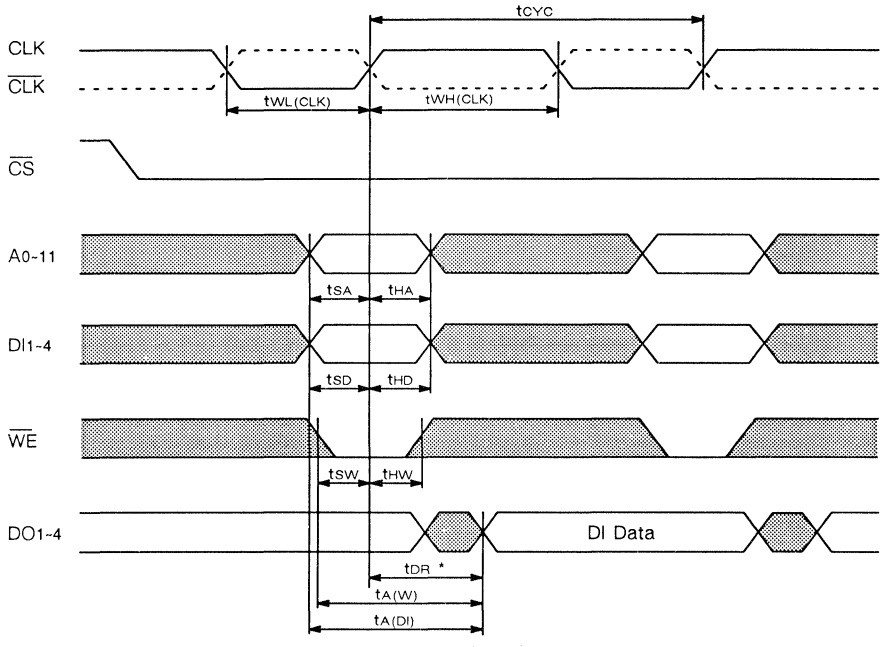
* Output is valid at tDR when tSA > tA(ADD) max – tDR max.

• CLOCK ACCESS MODE



* Output is valid at t_{DR} when $t_{WL(CLK)} > t_{A(CLK)\ max} - t_{DR\ max}$

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tSW > tA(W) max − tDR max and tSD > tA(DI) max − tDR max

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

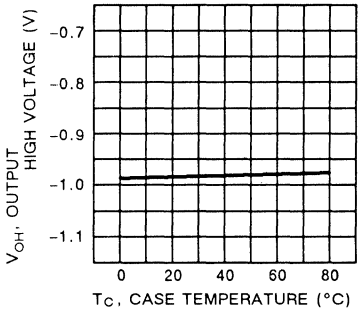


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

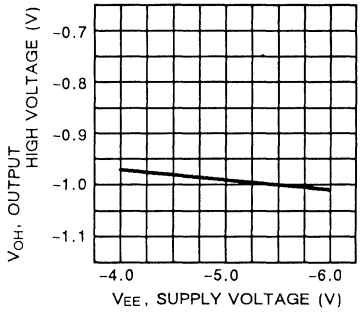


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

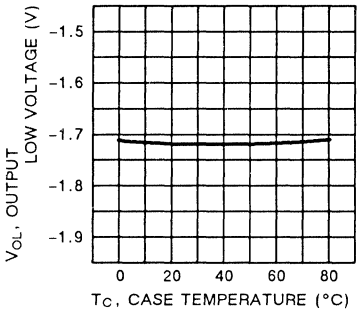


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

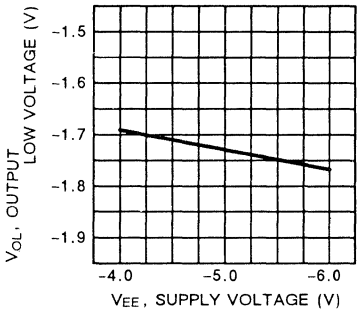


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

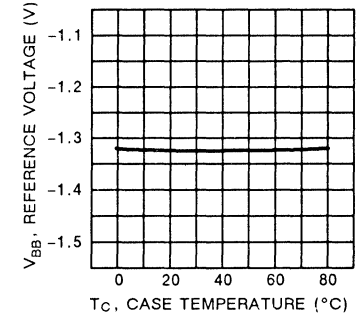


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE

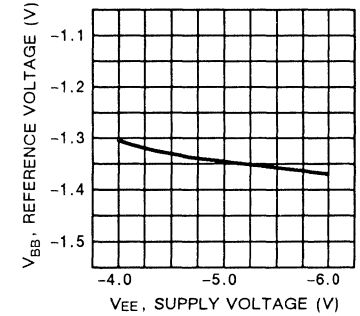


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Fig. 9 - SUPPLY CURRENT vs CASE TEMPERATURE

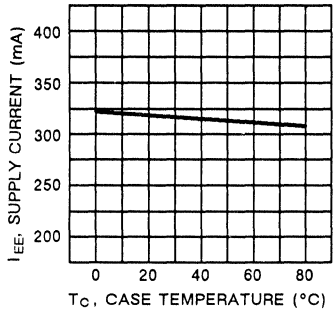


Fig. 10 - SUPPLY CURRENT vs SUPPLY VOLTAGE

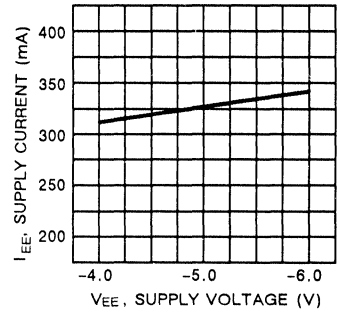


Fig. 11 - ADDRESS ACCESS TIME vs CASE TEMPERATURE

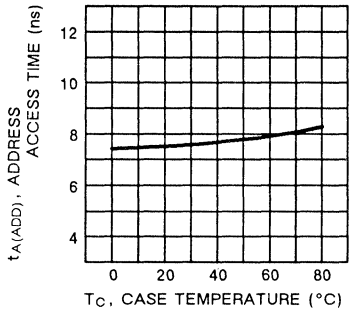


Fig. 12 - ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

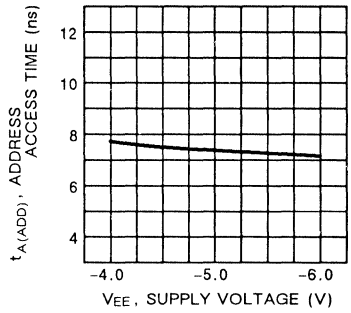


Fig. 13 - CLOCK ACCESS TIME vs CASE TEMPERATURE

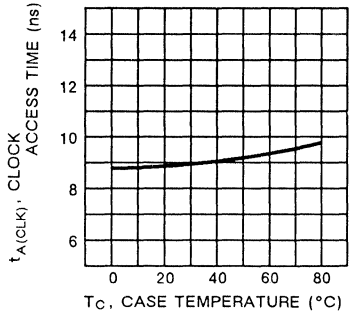


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

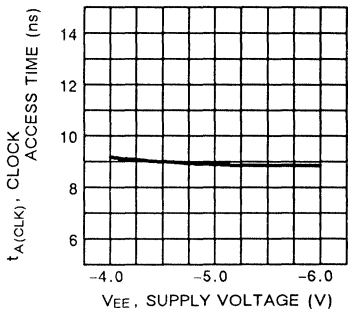


Fig. 15 – OUTPUT DELAY TIME vs CASE TEMPERATURE

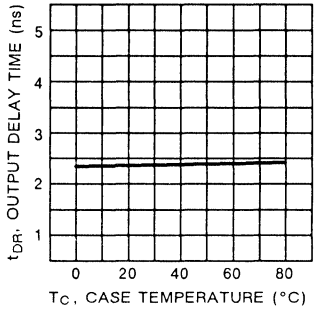


Fig. 16 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE

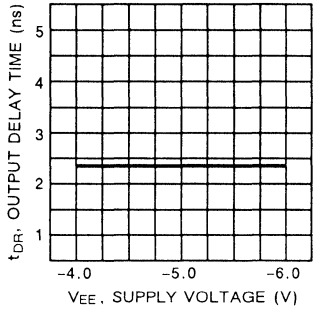


Fig. 17 – CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

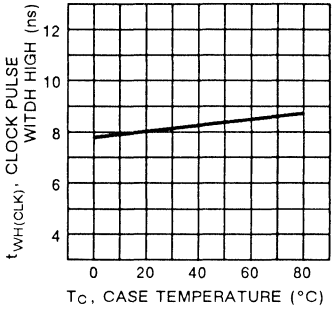
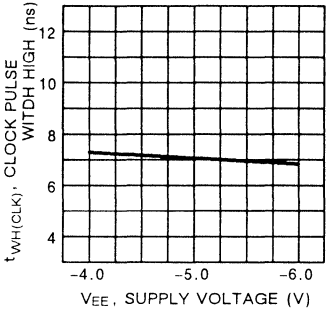


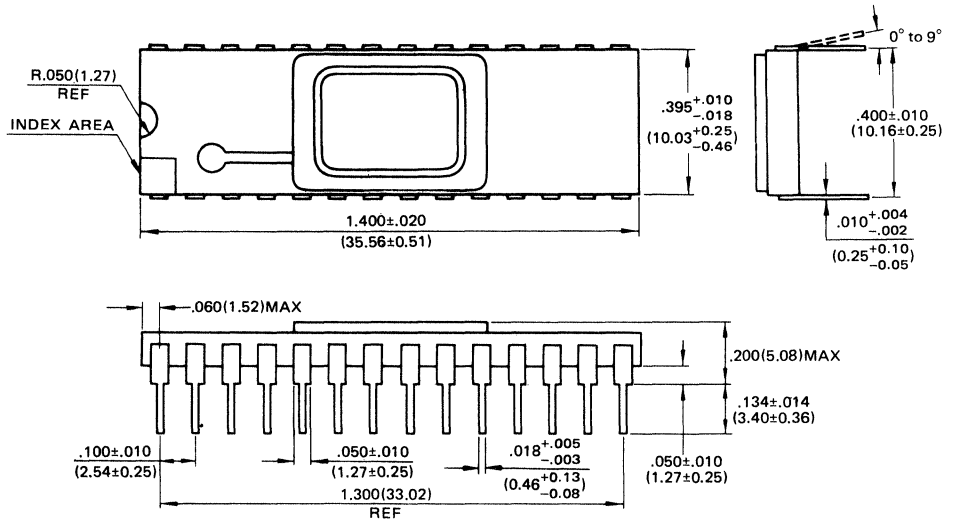
Fig. 18 – CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MBM100486RR-13

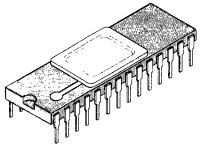
16384–BIT BIPOLAR SELF–TIMED RAMDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM100486RR–13 is fully decoded 16384–bit ECL self–timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on–chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allowsto decrease the number of device on the board.

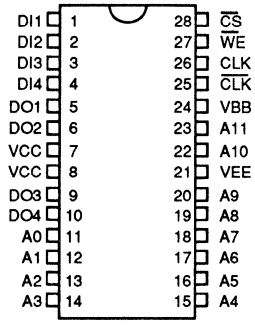
Operation for the MBM100486RR is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28–pin ceramic side brazed DIP and fully compatible with industry standard 100K–series ECL families.



CERAMIC PACKAGE
DIP–28C–A06

- 4096 words by 4 bits organization
- On–chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 13ns
  Output delay time : 4ns
- Power dissipation : 2184mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Option clock inputs : single ended or differential
- DOPOS and IOP–II processing
- 28–pin ceramic side–brazed DIP (Suffix: C)

PIN ASSIGNMENT
(TOP VIEW)



* V cc grounded

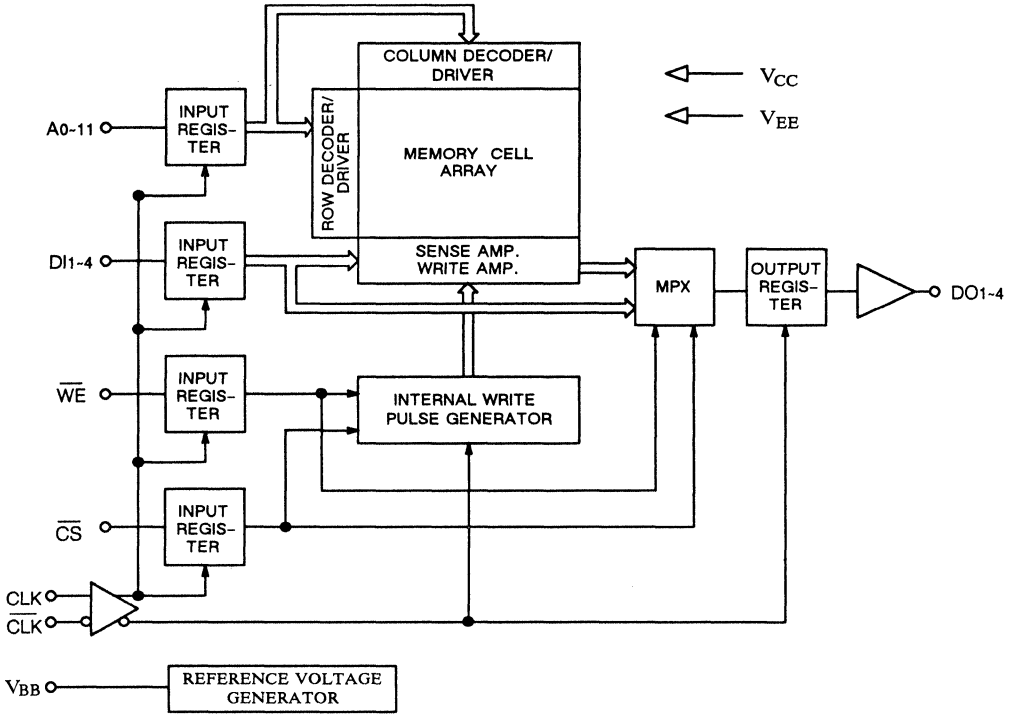
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Temperature under bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 – MBM100486RR-13



FUNCTION TRUTH TABLE

CS	WE	DI	CLK/CLK	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK (CLK).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address inputs
DI1 thru DI4	Data inputs
DO1 thru DO4	Data outputs
WE	Write enable
CS	Chip select
CLK, CLK	Clock inputs
VBB	Reference voltage (-1.32V)
VEE	Supply voltage (-4.5V)
VCC	Supply voltage (0V)
NC	No connection

GUARANTEED OPERATING CONDITIONS

(Reference to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limit over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(Vcc = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, Tc = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			µA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100486RR is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are edge triggered registered controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input and output registers are transparent when CLK ($\overline{CLK}$) goes high (low), and close to hold the data when CLK($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may not be stable during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes low (high), address data is held at output, while output data is kept valid during the same cycle. Thus, the output data becomes available at the next rising (falling) edge of CLK ($\overline{CLK}$).

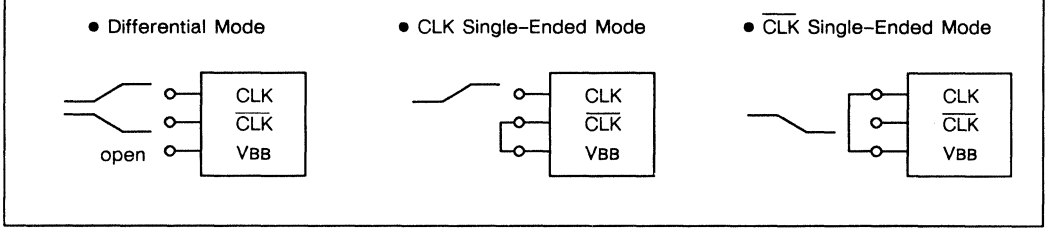
The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), inputs are transparent while previous read data appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the output by the CLK($\overline{CLK}$) rising (falling) edge of the next cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.

Fig. 2 – OPTION CLOCK INPUTS



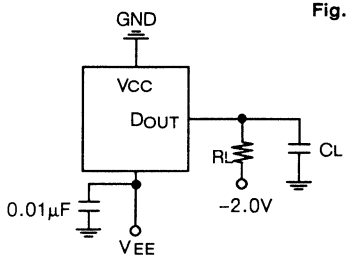
AC CHARACTERISTICS

(VCC = 0V, VEE = −4.5V ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

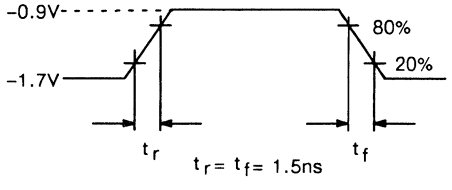
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	5.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	5.0 *2			ns
Cycle Time	t_{CYC}	13.0			ns
Output Delay Time	t_{DR}			4.0	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at $t_{WL(CLK)}$ > 8.0ns
*2 Specified at $t_{WH(CLK)}$ > 8.0ns

Fig. 3 – AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

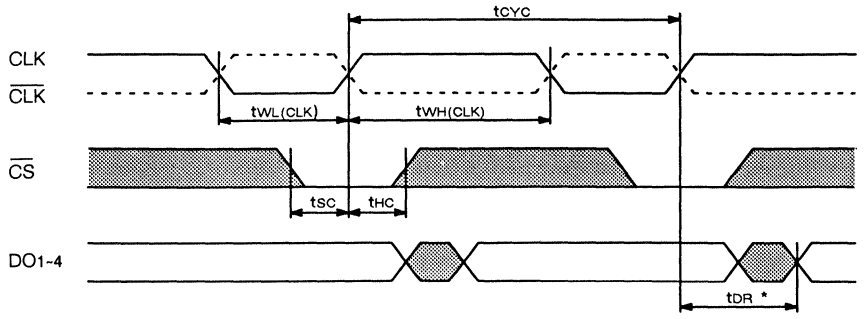


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

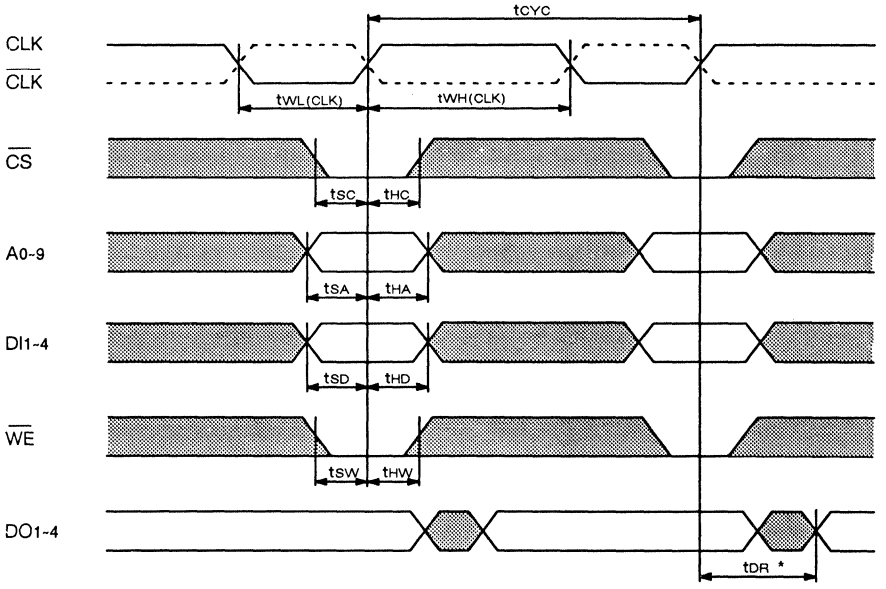
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

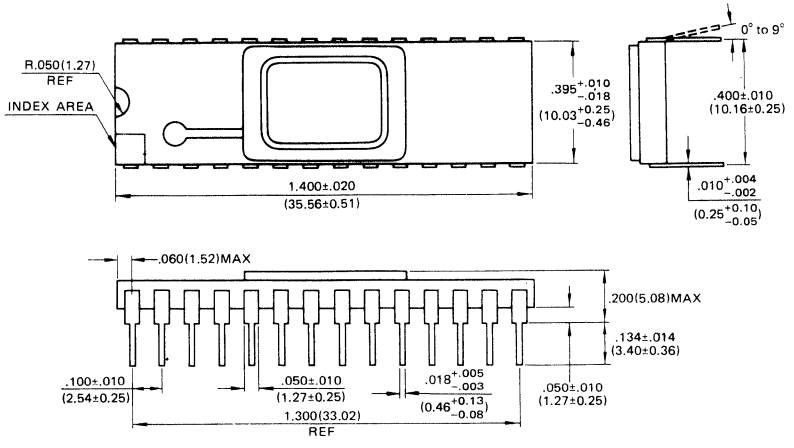
WRTE CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MBM100486RL-13

16384–BIT BIPOLAR SELF–TIMED RAMDOM ACCESS MEMORY

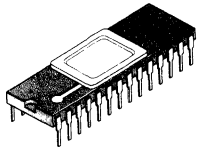
DESCRIPTION

The Fujitsu MBM100486RL–13 is fully decoded 16384–bit ECL self–timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on–chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

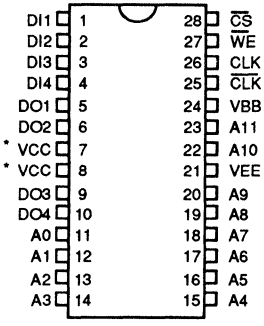
Operation for the MBM100486RL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28–pin ceramic side brazed DIP and fully compatible with industry standard 100K–series ECL families.

- 4096 words by 4 bits organization
- On–chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 13ns
  Output delay time : 4ns
- Power dissipation : 1.80W max
- Open emitter output for ease of memory expansion
- Level–sensitive D–type latch for outputs and edge triggered registers for inputs
- Internal write pulse generator
- Option clock inputs : single ended or differential
- DOPOS and IOP–II processing
- 28–pin ceramic side–brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP–28C–A06

PIN ASSIGNMENT
(TOP VIEW)



* V cc grounded

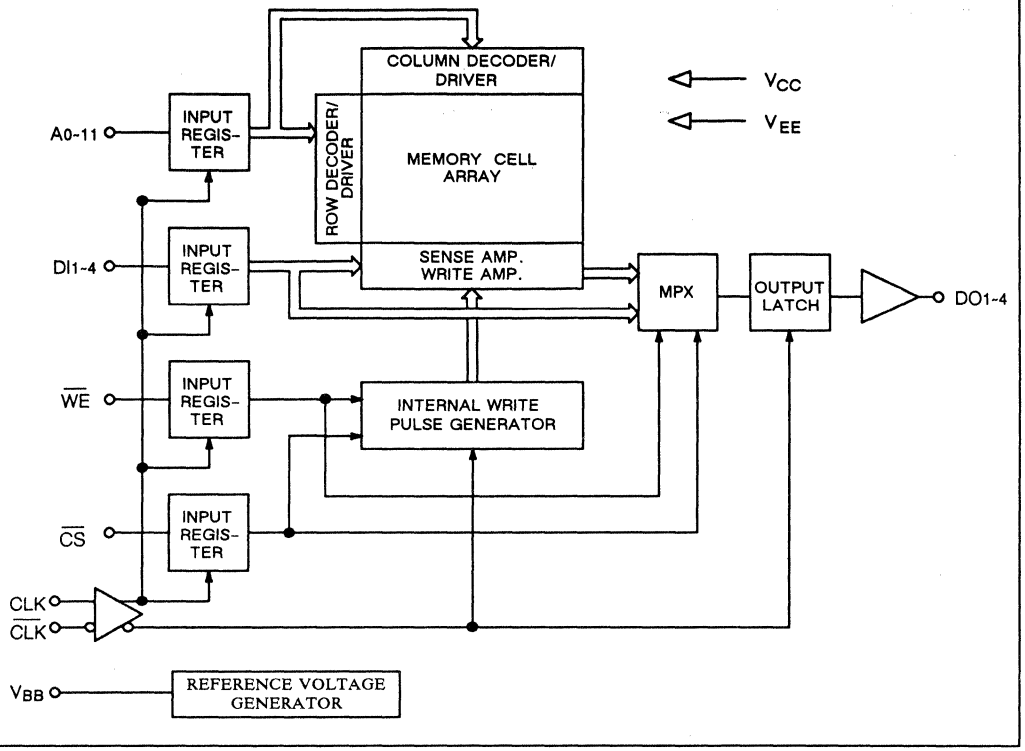
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to –7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	–30	mA
Temperature under bias	T_C	–55 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM100486RL-13 BLOCK DIAGRAM



FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

 : Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address inputs
DI1 thru DI4	Data inputs
DO1 thru DO4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
CLK, $\overline{CLK}$	Clock inputs
V_{BB}	Reference voltage (-1.32V)
V_{EE}	Supply voltage (-4.5V)
V_{CC}	Supply voltage (0V)
NC	No connection

GUARANTEED OPERATING CONDITIONS

(Reference to Vcc)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limit over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TC = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			µA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100486RL is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A11. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) furnish edge triggered registers, whereas outputs (DOUT) have level sensitive transparent latches.

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. All input data such as $\overline{CS}$ $\overline{WE}$. Address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input level are free to change for the rest of the cycle time once input data is held into the input register. Read out data becomes available during CLK low state in which output latches are transpatent. When CLK ($\overline{CLK}$) state is wide enough than the internal RAM access time, output data become valid in the short delay time (tDR) after the falling (rising)edge of CLK ($\overline{CLK}$).

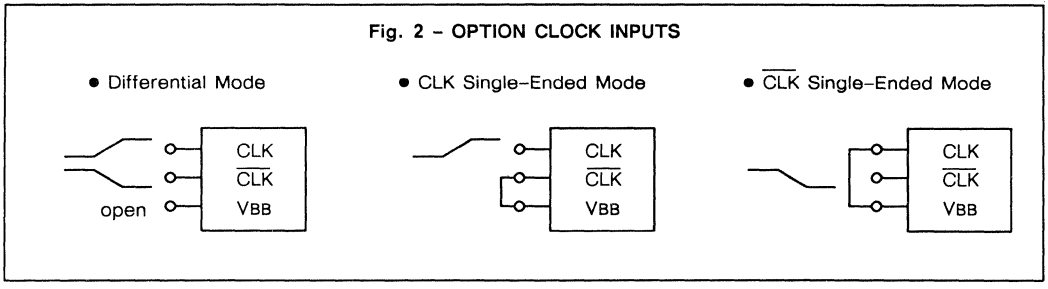
The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the address location. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

CLOCK INPUT

3

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.

Fig. 2 - OPTION CLOCK INPUTS



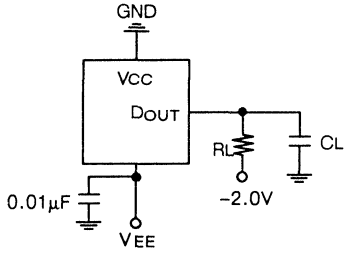
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V ±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

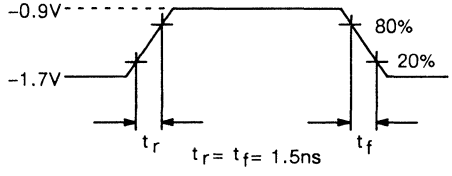
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	5.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	5.0 *2			ns
Cycle Time	t_{CYC}	13.0			ns
Clock Access Time	$t_{A(CLK)}$			12.0 *3	ns
Output Delay Time	t_{DR}			4.0 *4	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) >8.0ns
*2 Specified at tWH(CLK) > 8.0ns
*3 Specified at tWH(CLK) = 5.0ns
*4 Specified at tWH(CLK) > tA(CLK) max

Fig. 3 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

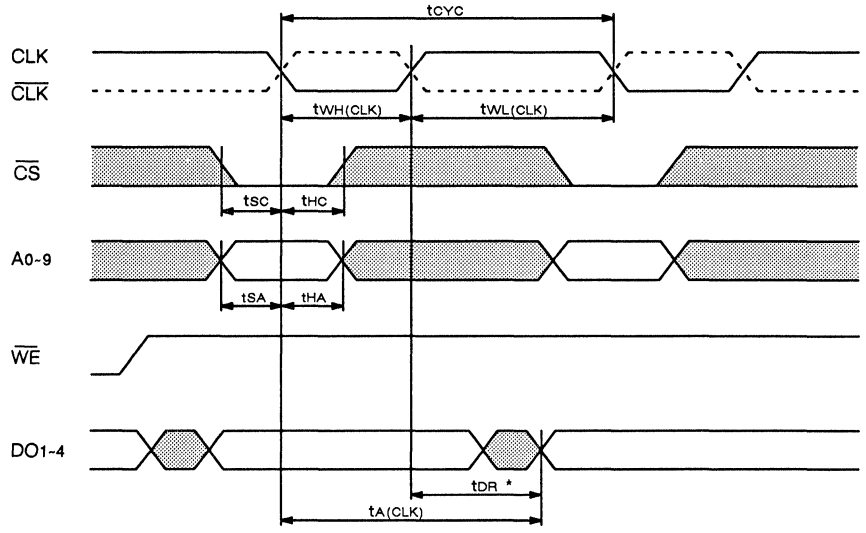


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

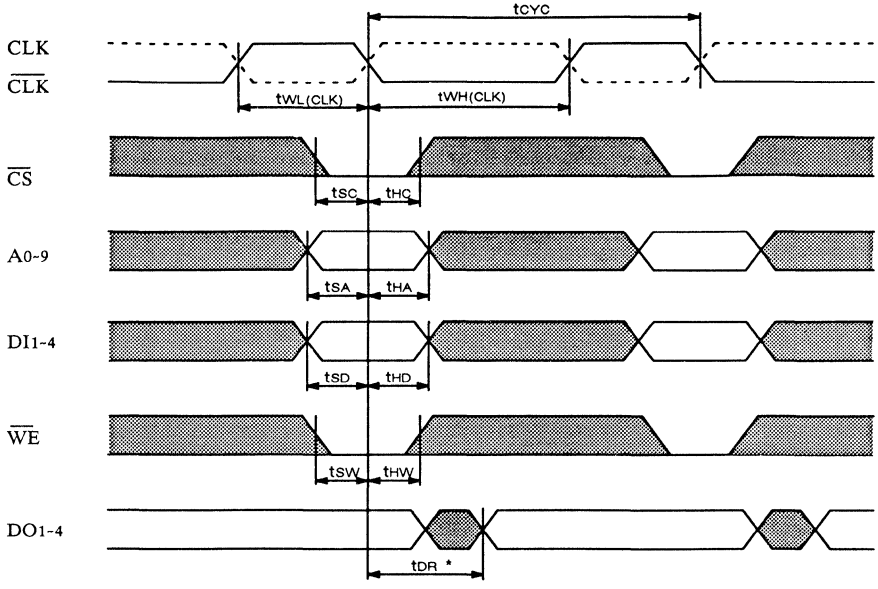
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

Fig. 4 – READ CYCLE TIMING DIAGRAMS



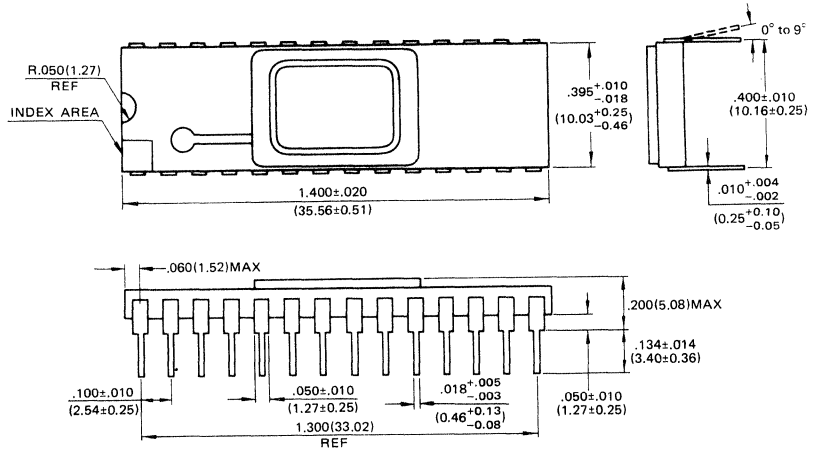
* Output is valid at tDR when tWH(CLK) > tA(CLK) max – tDR max.

Fig. 5 – WRTE CYCLE TIMING DIAGRAMS



PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

Section 4

Quality and Reliability — *At a Glance*

Quality Control at Fujitsu

Built-in Quality and Reliability

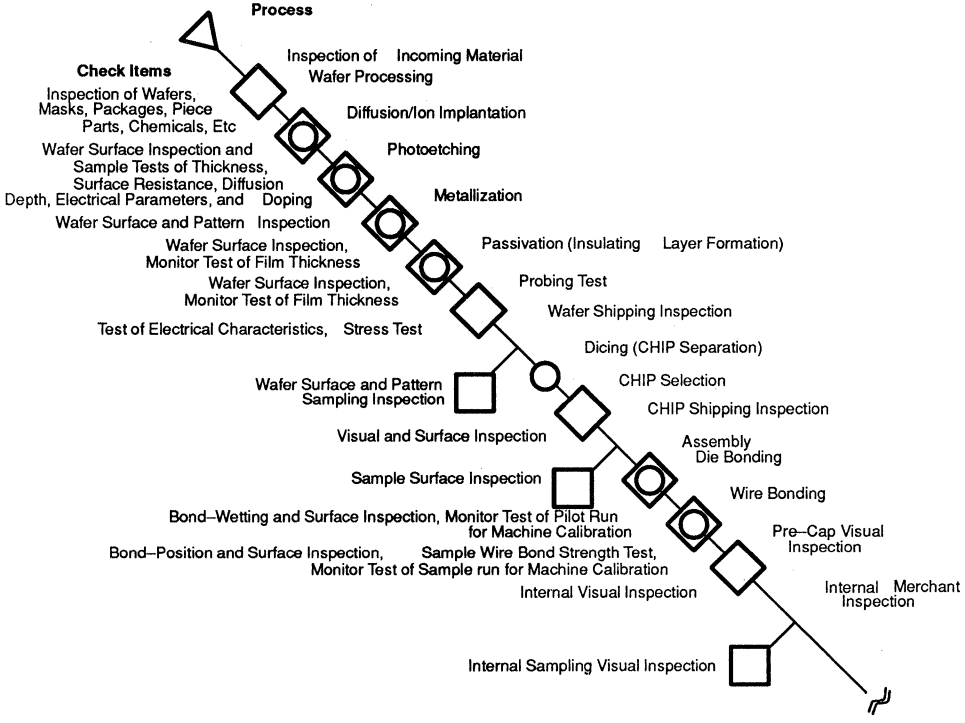
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

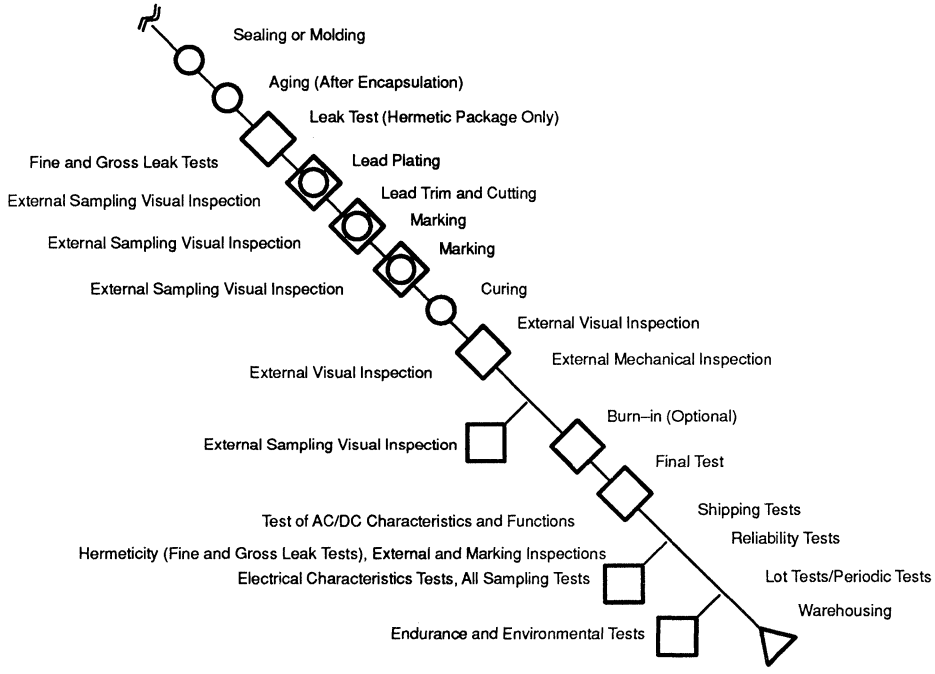
Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Processes at Fujitsu



Continued on next page

Quality Control Processes at Fujitsu (Continued)



Legend:

- Production Process
- Test/Inspection
- Production Process and Test/Inspection
- QC Gate (Sampling)

Note:
The flow sequence may vary slightly with individual product type.

4

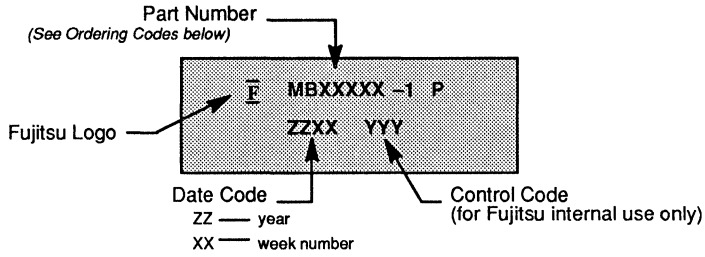
4

Section 5

Ordering Information — *At a Glance*

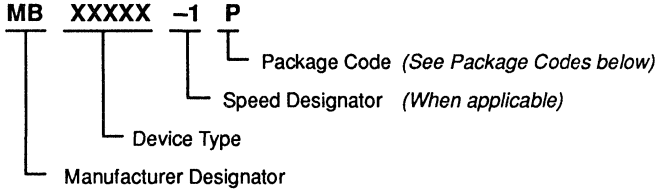
5

IC Product Marking



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

IC Ordering Code (Part Number)



MB Identifies an IC designed and manufactured by Fujitsu that uses a Fujitsu-designated device number.
MBM Identifies an IC designed and manufactured by Fujitsu that uses a device number designated by the industry to be the industry standard number.
Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

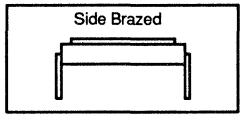
5

IC Package Codes

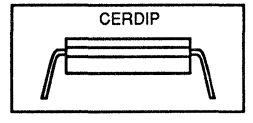
Ceramic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	TV,CV
PGA (Pin Grid Array)	CR
DIP (Side Brazed)[1]	C
DIP (CERDIP)[2]	Z
Shrink DIP	CSH
Flatpack, Metal Seal	CF
Flatpack, Glass Seal	ZF
SOJ (Single Outline Junction)	CJ

Plastic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	PV
PLCC (Leaded Chip Carrier)	PD
PGA (Pin Grid Array)	PR
DIP (Dual In-line Package)	P,M
Shrink DIP	PSH
Flatpack	PF
Single In-line, straight leads	PS
Single in-line, zig-zag leads	PSZ,PZ
SOJ (Single Outline Junction)	PJ

1 Side Brazed



2 CERDIP



Section 6

Sales Information — *At a Glance*

Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

- DRAMs and DRAM Modules
- EPROMs
- EEPROMs
- NOVRAMs
- CMOS masked ROMs
- CMOS SRAMs and CMOS SRAM Modules
- BiCMOS SRAMs
- Bipolar PROMs
- ECL RAMs
- STRAMs (self-timed RAM)
- Hi-Rel PROMs and SRAMs
- Ultra High-speed ECL/ECL—TTL Translator Circuits
- Linear ICs and Transistors

Introduction to Fujitsu (Continued)

ASIC products offered by ICD include the following:

CMOS, ECL, and BiCMOS gate arrays
CMOS standard cells
Design Software Support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs
Memory Cards

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

Fujitsu Mikroelektronik GmbH (European Sales Operation)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics Ireland, Ltd. (European Production Operation)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in the suburbs of Dublin, as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European ASIC Design Operation)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Asia PTE Ltd. (Asian/Oceanian Sales Operation)

Fujitsu Microelectronics Asia PTE Ltd. (FMA) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

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SPARC™ is a trademark of Sun Microsystems, Inc.
Ethernet® is a registered trademark of Xerox Corporation.
EtherStar™ is a trademark of Fujitsu Microelectronics, Inc.
StarLAN™ is a trademark of AT&T.

Integrated Circuits Corporate Headquarters — Worldwide

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For integrated circuits marketing information please contact the following:

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Telex: 781–2224361
FAX: (03) 211-3987

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FAX: (069) 6632122

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Fujitsu Microelectronics, Inc.
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ILLINOIS (Chicago)

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One Pierce Place
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MASSACHUSETTS (Boston)

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MINNESOTA (Minneapolis)

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NEW YORK (Hauppauge)

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OREGON (Portland)

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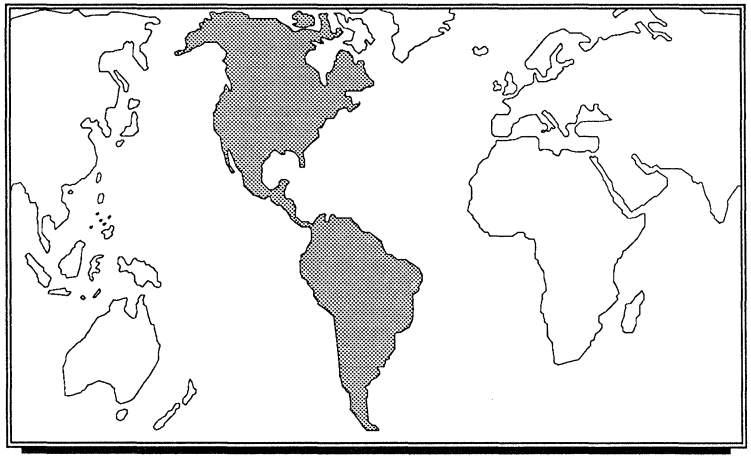

FMI Representatives — USA

For product information, contact your nearest Representative.

Alabama

The Novus Group, Inc.
2905 Westcorp Blvd.
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FAX: (205) 534–0186

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California

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Infinity Sales, Inc.
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FAX: (714) 833–0303

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Vantage Components, Inc.
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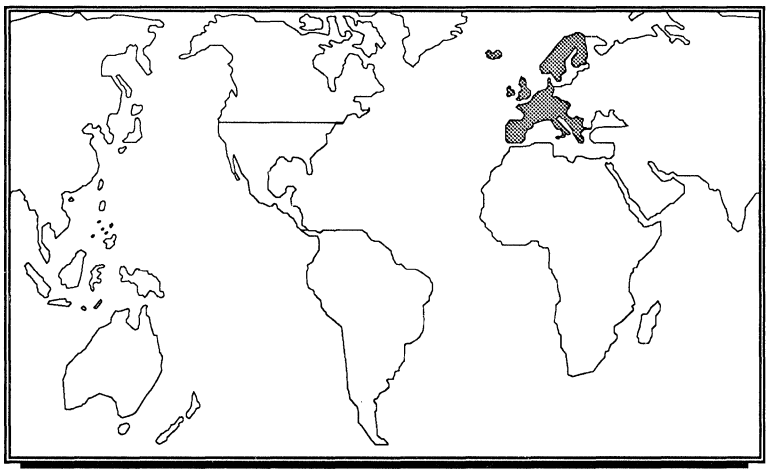

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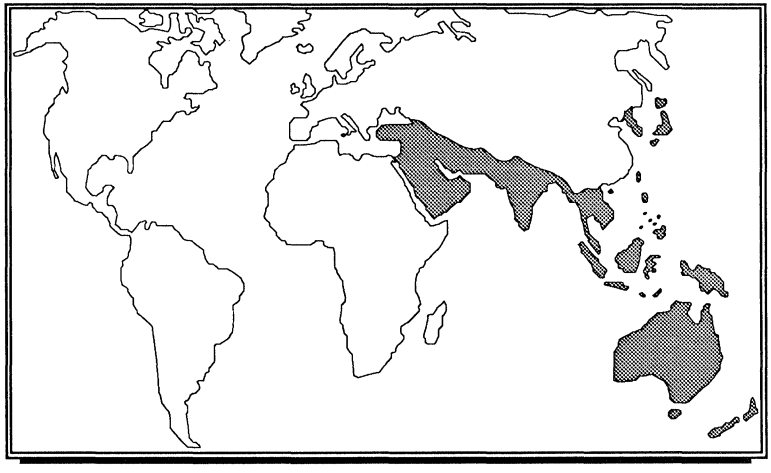

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Section 7

Design Information — *At a Glance*

Appendix 1

ECL RAMs

FUJITSU

Introduction to Emitter-Coupled Logic

Emitter Coupled Logic (ECL) refers to a type of circuit in which the signal is coupled from the emitter of the transistor(s) of one stage, to the base(s) of the next stage. This interconnection pattern differs from normal bipolar practice in that the collectors of the transistors are used to couple the signal from one stage to the next. The ECL arrangement is necessary because, unlike normal bipolar circuitry, ECL transistors are, ideally, never saturated, or turned fully on. In actual practice, however, there may be instances where saturation does occur.

The benefit of ECL circuit non-saturated operation is speed.The ECL transistor can turn on and off much faster than a transistor operating in a saturated mode. All other things being equal, ECL memories are five to ten times as fast as the nearest competitor, CMOS. This gap is narrowing, however, as some of the faster CMOS memories have reached the 35- to 25-ns range. This is beginning to encroach on ECL territory, which ranges at present from 25 ns for some of the slower ECL devices to 3 ns for the fastest, state-of-the-art integrated circuits.

10K Versus 100K—What Is the Difference

ECL logic and memories come in the following two basic family groups: 10K and 100K. These can usually be differentiated by the use of the numbers 10 or 100 in the part number (for example, Fujitsu's MBM10480 and MBM100480). In most cases, the 10K part and the 100K part are the same die with the 100K modification being a mask option.

Because ECL transistors usually are not saturated, the voltage level of the transistor is a function of more than just the drive level of the base. When a transistor is driven into saturation, enough drive is applied to the base of the transistor to turn it fully on. At this point, the collector and emitter of the transistor are at the supply voltage level or V_{CC}. In a non-saturated transistor, the collector is at V_{CC}, but the emitter is at some voltage below that level.

For example, imagine the transistor as a valve in a water pipe. The base drive is represented by the force on the valve handle. When the handle is turned fully clockwise, the water pressure on one side of the closed valve is high and the pressure on the other side of the valve is zero. As the valve handle is turned counter-clockwise, the water pressure on the controlled side of the valve starts to increase. When the valve is turned fully counter-clockwise, the water flow is essentially unrestricted, therefore, the pressure measures the same on one side of the valve as it does on the other.

A transistor works in a similar manner. As the base drive (or force on the valve handle) increases, the voltage across the collector-emitter (the water flow) also increases until the point is reached where the resistance to current flow cannot be reduced further. At this point, the transistor is said to be saturated (fully on). In the saturated state, the stability of the current being conducted by the transistor is largely unaffected by such factors as temperature and power supply regulation.

In ECL design, however, the opposite is true. Because the transistor is never saturated, the emitter voltage is a function of the base drive. The relationship between the base drive and the output level of the transistor is dependent upon both power supply and temperature. This means that for a given drive voltage, the output of the transistor can vary over a voltage and temperature range. In 10K ECL parts, voltage is specified over temperature. The specified temperatures are usually given as 0 degrees C, 25 degrees C, and 75 degrees C. The 100K ECL parts do not have temperature specified over voltage because ECL integrated circuits have built-in voltage/temperature compensation.

The major difference between the 10K and the 100K products is that the 100K parts have temperature compensation components on board the integrated circuit as well as voltage regulation. This makes the 100K ECL much more stable over extremes of temperature and voltage.

ECL Soft Error

Generally, aside from the non-saturated transistor's susceptibility to voltage and temperature variations, there are no inherent disadvantages to ECL circuitry. However, as ECL devices have become larger and more dense, a problem has come to light that was not previously associated with ECL.

This problem, called soft error, is caused by the memory cell's state being altered by the intrusion of an alpha particle. Unfortunately this phenomenon, caused by increasingly smaller cell geometries, is aggravated by the non-saturated mode of the cell's transistors. To overcome this problem, many ECL manufacturers are changing to a cell structure that contains one or more saturated transistors. While this may seem a contradictory move, it must be remembered that only one of two transistors per cell are affected. The actual cell pair itself is not saturated. Any speed lost due to the saturation of the added transistor pull-ups will be regained by further reductions in actual cell size due to design improvements. The important consideration is the reduction, or in some cases, the virtual elimination of soft errors.

Source: Fujitsu Microelectronics, Inc.
Integrated Circuits Division
Applications Engineering Department
1989

Appendix 2

PNP Load Cell Design

FUJITSU

PNP Load Cell Design: A Design Strategy to Eliminate Soft Errors

With access times in the five nanosecond range, present Emitter Coupled Logic (ECL) Static Random Access Memories (RAMs) are the fastest computer memories available. Their circuitry is designed primarily for speed.

ECL Memory in Computers

ECL memories are usually used in large processing systems where the lightning fast speeds of individual integrated circuits (ICs) make up for the complex circuitry that these machines contain. The complexity of mainframe computers make it desirable for designers to save power and board space by using very dense memories. A single large memory chip can do the same job as many smaller ones, at a fraction of the power dissipation and with only one package. Therefore, the desire to squeeze as much ECL memory as possible into one single package is the driving force in ECL memory design today.

In order to meet the market requirements for larger ECL RAM ICs, it has become necessary to reduce the physical size of the on-chip components to levels thought impossible a few years ago. As the size of the individual memory cells shrinks to smaller dimensions, a problem formerly associated with the much slower MOS designs has started to plague ECLs. This problem is alpha-induced soft error.

Hard and Soft Errors

In IC memories, an error can either be hard or soft. A hard error is one which is device-related, that is, an error caused by a fault in the chip itself. Hard errors are usually repeatable and are generally corrected by replacement of the faulty IC. A soft error is caused by an outside source, usually random, which cannot be repeated easily in a test. Sources of soft errors in memories are usually either disturbances on the power lines, sometimes called glitches, or alpha particles. Power glitches can be controlled by power supply design or by adding special filters to the computer's AC line. However, alpha particle-induced soft errors cannot be so easily eliminated.

The Alpha Particle

Alpha particles continuously bombard the earth from outer space. Our atmosphere filters most of the alpha particles out, but a few still manage to make it to the earth's surface. These particles have very little mass and, under most circumstances, have little or no effect on human technical endeavor. However, in the case of modern high-density IC technology, alpha particles can create real problems.

In ECL memories, the cell is usually made up of two transistors, which in older technologies were large enough that an alpha particle passing through didn't cause any problems. But as the cells have gotten smaller, so have the transistors that comprise the cell. Therefore, an alpha particle passing through one of the new, small cells has more than enough energy to cause change. A one becomes a zero and a zero becomes a one, thereby creating inaccuracies.

An alpha particle penetrating a standard ECL memory cell creates a temporary conductive path along its trajectory through the cell. This conductive path bleeds away the charge that is keeping the on transistor in that state. When the on transistor starts to turn off, the memory cell flips and produces an error, resulting in bad data.

To illustrate the point, imagine that your company's payroll service has a large mainframe that uses ECL memories to handle payrolls. One soft error could change someone's paycheck by a factor of ten. To avoid this, most computers using ECL memory in sensitive locations use a hardware fix called error correction. Error correction works, but it is at best a treatment for the symptom rather than a cure for the disease. Error correction works by using a redundant bit of data that can take the place of any data that has been lost or altered by a soft failure. While this technique can be successfully applied to ECL system design, it is often not desirable to do so because the resultant increase in complexity and decrease in speed makes error correction impractical. By not using this approach to soft error correction, the mainframe computer designers have placed the burden of eliminating or controlling alpha-induced soft errors squarely on the shoulders of the ECL memory manufacturer.

Solving the Alpha Particle Error Problem

The problem of alpha particle soft error increases with each newer and larger ECL memory. ECL producers have tried to solve the problem in several ways. In the past, the most practical approach has been to shield the memory area of the die with some material through which alpha particles could not pass, such as polyamide. The major problem with this approach is that many of the most successful alpha shield materials are also low level alpha sources. This means that when an alpha particle is stopped by the shield material, the energy is sometimes transferred to that material on a sub-atomic level and can knock an electron loose. The accelerated electron then penetrates the die. This doesn't happen very often and generally alpha shields do a fairly good job of reducing alpha-induced soft error to acceptable levels.

The Best Solution

The best method for controlling alpha particle circuit disruption is to change the cell design. Fujitsu Microelectronics, Inc. has done just that. The PNP pull-up cell design developed by Fujitsu allows for further reduction of overall cell size with an accompanying increase in the cell's transistor stability.

An ECL memory cell contains two NPN transistors connected so that when one is turned on, the other is turned off. The cell's memory state, (that is, whether it contains a logic one or a logic zero), is determined by which transistor in the cell is on and which one is off. This arrangement of transistors is called a monostable multivibrator, or a flip-flop. One of the major characteristics of flip-flop is that the state of one transistor cannot be altered without changing the state of the other transistor. So, if the on transistor is turned off, then the off transistor will automatically turn on.

How The Classic ECL Memory Cell (NPN) Works

As explained above, the traditional ECL memory cell is constructed from a pair of NPN transistors connected together as a monostable multivibrator called a Parallel Diode Cell (Figure 1–1). The two

transistors in the cell are connected so that they are pulled up to the word line via a pair of resistors in parallel with a pair of Schottky diodes. This diode pull-up configuration is the classic ECL memory cell design and, until recently, was the basis of almost all ECL static RAMs.

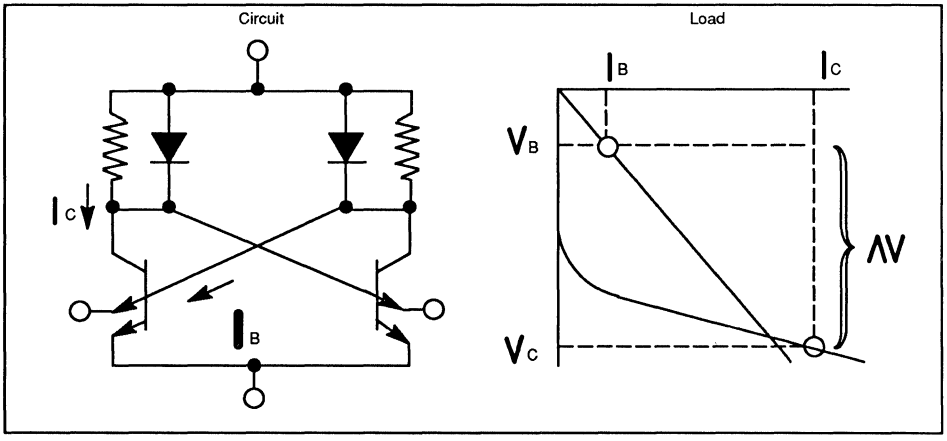

Figure 1–1. Parallel Diode Cell

This design has the advantage of being fast because the two multivibrator transistors are biased so that when they are turned on, neither is in a saturated state. Being non-saturated, they are able to turn on and off very quickly. As long as the cell is designed with relatively large geometries, this traditional architecture is problem-free. Problems do occur however, when the geometries are shrunk to make larger and larger ECL organizations.

As cell geometries get smaller, the individual cell transistors become more susceptible to soft error because the other on transistor in the cell is held high by its base capacitance charge. Since the base areas of these devices have now become much smaller than they once were, they hold a very small charge (on the order of approximately 75000 electrons). This charge is easily dispersed, and an alpha particle has enough energy to do so. The voltage drop at the load resistor in the standby mode

$$(DV = iC \times RL)$$

is limited by the forward voltage applied to the Schottky diode. Therefore, there is a chance that due to alpha particle penetration, the charge on the on transistor

$$(Q = C \times DV)$$

could become as small as the charge on the off transistor, causing the cell to flip.

How the New PNP Load Cell Works

In an effort to solve this problem and to supply very fast, virtually error-free ECL memories to its customers, Fujitsu has developed a new design that is a radical departure from the classic diode pull-up cell. This new design is called the PNP load cell because it replaces the diode-resistor pull-up with a PNP load cell (Figure 1–2). The PNP load cell places a PNP transistor between the collector of the cell transistor and the pull-up's emitter is also tied to the word line.

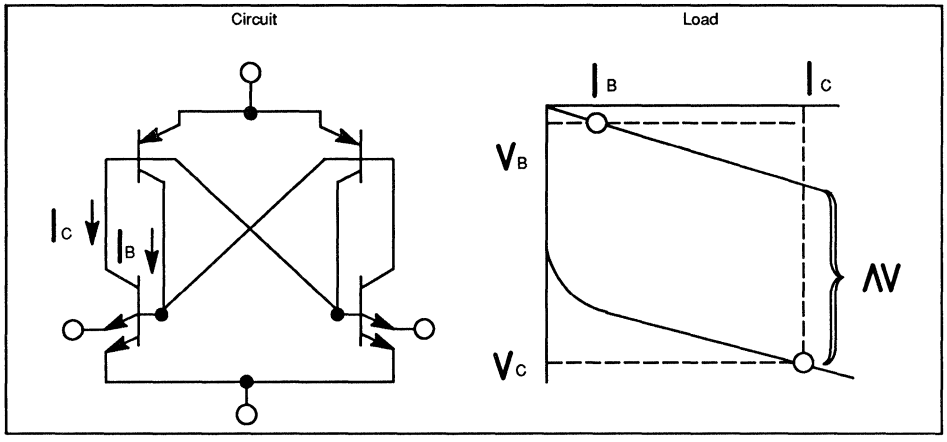

Figure 1–2. PNP Load Cell

The result of this design change is a decrease in noise and an increase in alpha particle immunity. The increased protection from soft error is due to the difference between the dynamic characteristics of the Schottky diode in the standard pull-up configuration and the PNP transistor in the PNP load cell.

Since the voltage drop across the PNP transistor is greater than across the Schottky diode, the /\V for the new design is twice the /\V of the diode cell. The internal capacitance for the two designs is about equal, the base-collector capacitance is about equal, but the base-emitter capacitance is much greater for the PNP cell design because both transistors are saturated. Since the cell noise immunity, or "Q" is the product of the base-emitter capacitance and the DV of the design, the PNP load cell enjoys a large increase in noise and alpha particle immunity over the diode-resistor design (on the order of a ten to the fifth or a ten to the sixth improvement).

Fujitsu's new design has made it almost impossible for the transistors in a memory cell to be changed by an alpha particle because the size of the charge that holds the on transistor in that state has been increased. If an alpha particle cannot bleed away enough charge to flip the cell, then soft errors cannot occur.

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Are There Tradeoffs

The new PNP cell design uses saturated, active components to achieve the high noise immunity that ordinarily would cause a loss of speed. However, in the case of the Fujitsu ECL family, the performance of the ECL Static RAMs has been retained and, in some organizations, improved. Fujitsu has reconciled these two diametrically opposed concepts of high noise immunity and high performance by recovering lost speed through the reduction of propagation delays on the chip itself via improved design rules.

Fujitsu's Improved Design—IOP II and ESPER

Fujitsu uses Isolation by Oxide and Polysilicon (IOP) in its ECL memory designs. The original IOP design had a V-groove isolation channel between cells. The width across the top of the groove was a function of the depth to which the groove had to be etched (see Figure 1–3).

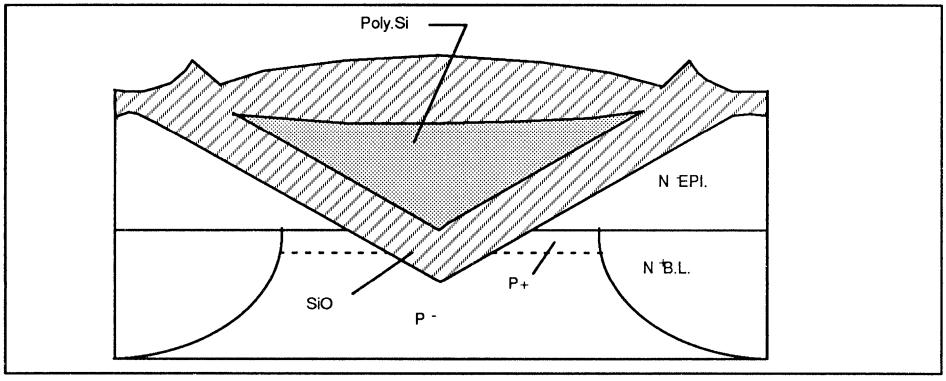

Figure 1–3. Original IOP Design

The new PNP pull-up cell design features a U-shaped isolation channel instead of a V-shaped one. The IOP II design is shown in Figure 1-4. When a U-shape is used, both the width and the depth of the channel can be carefully controlled. The resultant groove is about one-half the width of the old V-groove. This allows for a reduction in overall die size and a shortening of both row and column lines, while allowing decoders and other peripheral circuitry to be located closer to the cell area. This new set of design rules will be used for all future Fujitsu ECL memory designs.

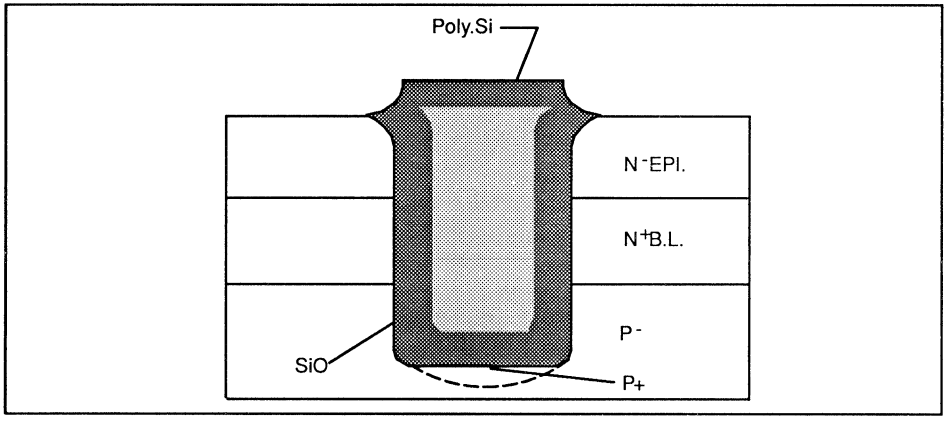

Figure 1-4. IOP II Design

Fujitsu has now developed an improved, second generation PNP load cell design known as ESPER that offers high soft error immunity, smaller die size, lower power dissipation and performance uncompromised by the presence of saturated components in the cell.

Summary

In summary, an ECL memory design that nearly eliminates alpha particle-induced soft error is invaluable to designers of large, fast, mainframe computers, processors, testers, and other systems in which errors cannot be tolerated. The PNP pull-up design of Fujitsu's ECL Static RAMs, when coupled with new technologies such as IOP II and ESPER, achieves this goal with little or no overall loss of ECL performance.

Source: Fujitsu Microelectronics, Inc.
Integrated Circuits Division
Applications Engineering Department
1989

Appendix 3

Application Note

November 1989
Edition 1.1

APPLICATION NOTE

FUJITSU

ECL RAMs

How to Design Efficient ECL RAM Systems

Applications Engineering Department
Fujitsu Microelectronics, Inc.
Integrated Circuits Division

ABSTRACT

ECL (Emitter Coupled Logic) devices offer some of the fastest performances available. The purpose of this document is to acquaint designers with the ECL technology and recommended steps for implementing an ECL design. This document covers several aspects of ECL system design. In order to understand the basic rules for designing with ECL, it is worthwhile to have a brief discussion of what ECL is and how the basic gates are designed.

7

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Edition 1.1

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ECL: What is it?

ECL (Emitter-Coupled-Logic) is one form of current mode logic. The basic current switch for Fujitsu's ECL RAM is shown in Figure 1. There is a constant current source or resistor at the base of this switch. (The current source is programmable for ECL gate arrays.) The collectors are also connected to resistors.

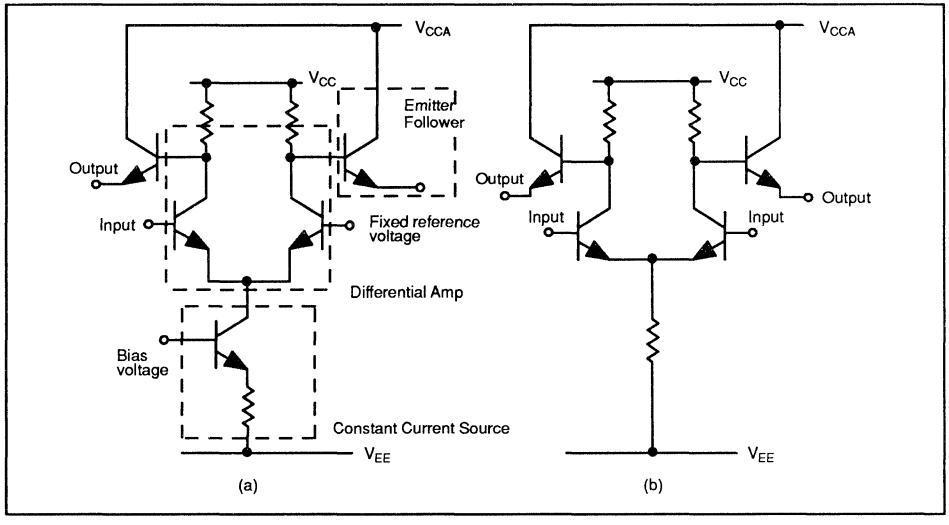


Figure 1. Basic Current Switch for ECL RAM

The inputs can be driven in two different ways. In the first method (Figure 1a), a differential input is used on both the bases of the transistors to form a current switch. In the second method (Figure 1b), an input voltage is applied to one transistor base, while a fixed reference voltage is applied to the other transistor base to drive the input. The second method is very common because it has twice the input

voltage swing when compared with the first method. Emitter-follower outputs are connected to the collectors to provide high driving capability.

ECL Inputs

Fujitsu's ECL RAMs have a pulldown resistor on the chip select input, tied internally to VEE. This input is an assertive LOW signal when left open. Therefore, if the input is left floating, the pulldown resistor ensures that the device is held in an active state. On the other hand, the write enable, the address inputs, and the data input pins do not have a pulldown resistor connected internally to V_{EE}. Thus, these pins should never be left floating, because the input level may change due to leakage current. Therefore, it is recommended that the specified level on these inputs be maintained.

Wire-ORing the ECL Outputs

Like the input pins, the output pins do not have pulldown resistors. Therefore, wired-OR connections are supported by ECL outputs. ECL RAMS also support this feature. However, wired-OR connections will increase propagation delays because of greater capacitive loading. Propagation delays increase about 30 ps for each output load increase of 1 pF. Since the output capacitance for the current ECL RAMs is 6 pF maximum, the propagation delay caused by one wired-OR connection is about 180 ps. Compared to address access time, the delay is negligible. Fujitsu guarantees the AC characteristics for an output load of 30 pF; thus, five wired-OR connections can be used without causing noticeable propagation delays. For ECL gate arrays, Fujitsu recommends using cutoff mode output buffers to wire-OR ECL outputs in order to minimize reflections.

In using the wired-OR capability, the designer must be aware that the output transistor is never completely at cutoff, so in the high-impedance state, current leakage is possible. If a large number of drivers are combined in a wired-OR arrangement, the sum of their leakage currents can pull the output voltage out of the logic 0 state. Hence with every additional driver wired to an output, a slight loss in noise margin is incurred. (Reference 1). Before discussing noise margins and their effects, let's look at the differences between 100K and 10K families.

Difference Between 10K and 100K

Basic differences between these two families are circuit stability and performance with variations in supply voltage and ambient temperature. 100K ECL parts are both temperature-compensated and voltage compensated; 10K parts are only voltage compensated.

In addition to these two basic families, there is 10KH whose I/O level is slightly different from that of the 10K family. Therefore when 10K devices are connected with 10KH devices, difference of noise margin should be paid attention to. (See the next section, Noise Margins.) Power supply voltage (V_{EE}) is –5.2 V for 10K and 10KH and –4.5 V for 100K. Recently requests for temperature compensated devices working at –5.2 V have increased. But generally speaking, noise margin decreases when 100K devices are operated at –5.2 V. So Fujitsu has developed 101K series whose I/O level is adjusted to keep sufficient noise margin.

ECL is a current mode logic, that is, it relies on voltage changes to generate changes in current. ECL has only a 1-volt logic swing with appropriately small noise margins. Before further discussions, an explanation of noise margins is in order.

Noise Margin

Noise margin is a DC voltage specification which measures the immunity of a circuit to adverse operating conditions. This is defined as the difference between the worst-case input logic level (V_{IH} min or V_{IL} max) and the worst-case output (V_{OH} min or V_{OL} max) for the corresponding input logic level. Guaranteed noise margins (*NM*) for 10K at 25 degrees Centigrade are:

$$\begin{aligned} \textit{Logic 1 NM} &= V_{OH}\ min - V_{IH}\ min \\ &= -0.960 - (-1.105) \\ &= 145\ mV \end{aligned}$$

$$\begin{aligned} \textit{Logic 0 NM} &= V_{IL}\ max - V_{OL}\ max \\ &= -1.475 - (-1.650) \\ &= 175\ mV \end{aligned}$$

For 100K they are as follows:

$$\textit{Logic 1 NM} = 1.025 - (-1.165) = 140\ mV$$

$$\textit{Logic 0 NM} = 1.475 - (-1.620) = 145\ mV$$

For system design, worst case conditions are always considered. If so, the *145 mV* noise margin becomes the design limit. In system design, the user is concerned with the noise margin when devices at different temperatures and different power supply voltages interface with each other. This is because the 10K logic level thresholds of ECL parts drift with temperature. Therefore, unless the ECL family being used is temperature compensated, a hot driver may not be able to send data to a cold receiver due to threshold differences. This is the result of noise margin impairment due to the ambient temperature differential existing between the receiver and the transmitter circuit. When several hundreds or thousands of ECL circuits are present in the same cabinet, it becomes difficult to provide sufficient cooling so that all of these circuits are essentially at the same temperature. The bottom line of Table 1 shows the benefit of using the 100K family with built-in temperature compensation.

Table 1. Noise Margin (at 25°C)

Interface	V_{EE}	LOGIC 1			LOGIC 0		
		V_{OH} min.	V_{IH} min.	Noise Margin	V_{OH} min.	V_{IH} min.	Noise Margin
10K→10K	–5.2	–960	–1105	145	–1475	–1650	175
10KH→10KH	–5.2	–980	–1130	150	–1480	–1630	150
10KH→10K	–5.2	–980	–1105	125	–1475	–1630	155
10K→10KH	–5.2	–960	–1130	170	–1480	–1650	170
100K→100K	–4.5	–1025	–1165	140	–1475	–1620	145

Without voltage compensation, output thresholds and switching parameters vary from part to part, thereby decreasing noise margins. Also, power dissipation is the product of the supply current I_{EE}

and the supply voltage V_{EE}; uncompensated ECL circuits will experience rapid power dissipation changes as V_{EE} varies.

High and Low Level for ECL RAM Inputs

A high level for 100K is –880mV to –1025mV. In order to preset the inputs to a high level, the designer should not tie them directly to the ground which is the higher of the two voltage planes available on the board. If the input is tied directly to ground it will drive the input transistors into saturation, which will drastically slow down the gate's switching time in response to changing signal levels at the inputs which are not tied high. Hence, Fujitsu recommends the following circuit for presetting the inputs (both 10K and 100K) to a high or a low level. The value of the output termination depends upon factors which will be discussed later in the section on terminating techniques.

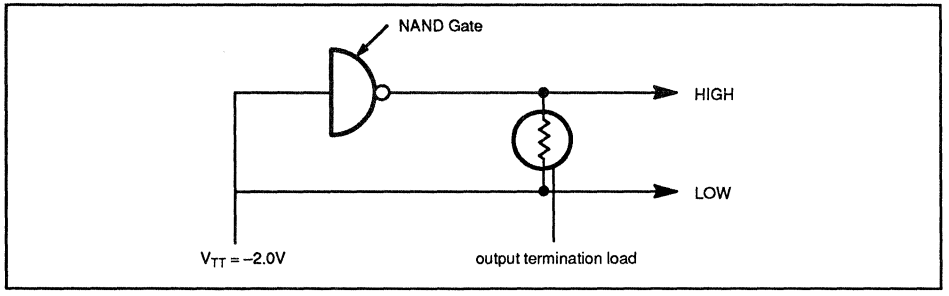


Figure 2. Presetting the Inputs to a High or Low Level

Switching Multiple Inputs and Outputs

The base current flowing through the ECL inputs is very small. Therefore, when multiple inputs are switched simultaneously it does not cause any specific problem. However, when multiple outputs are switched certain precautions should be taken. This is because output current changes drastically when switching from high to low or from low to high (for a 50-ohm termination resistor and termination voltage at –2.0 V, I_{OH} = 22 mA and I_{OL} = 5 mA). Thus, when multiple outputs (4-bit wide and 8-bit wide devices) are switched simultaneously, current spikes may occur at the V_{CCO} terminal. This in turn induces voltage spikes on V_{CC} (ground) and decreases input and output noise immunity.

Before going into precautions for spikes on the ground lines, let's look at the power supply lines on Fujitsu's ECL devices. All ECL devices have a V_{EE} supply line (a negative power supply, –4.5V for 100K and –5.2V for 10K devices) and a V_{CC} ground line. In some ECL RAMs, there are two V_{CC} pins. As shown in Figure 3, V_{CCO} supplies the output drivers while V_{CC} supplies the remaining circuits.

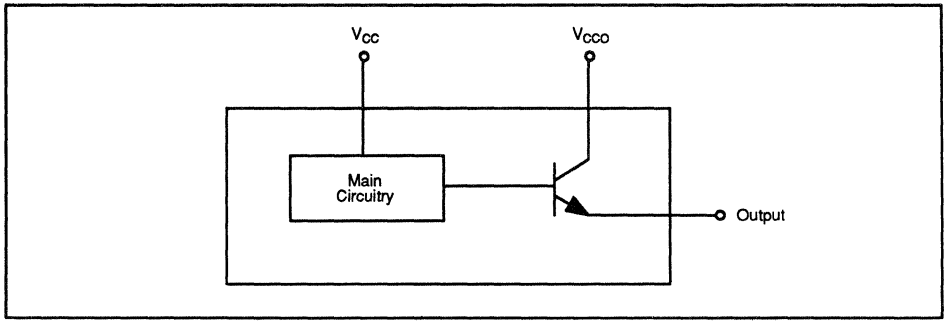


Figure 3. V_{CC} and V_{CCO}

Due to the separation of V_{CC} and V_{CCO}, changes in load currents while the outputs are switching do not cause glitches on the power supply ground bus which is connected to the V_{CC}. This can, however, cause ringing on the outputs.

The ringing can be eliminated by internal connection of V_{CC} and V_{CCO} pins but it may cause spikes on the power supply ground lines when multiple outputs are switching. This is due to the current noise caused by the switching of multiple outputs. These spikes will produce glitches on the output waveforms. Glitches may also be observed when the impedance of the V_{CC} pin is too large.

To prevent ringing on the outputs and glitches on the V_{CC} and V_{CCO} lines, Fujitsu recommends that the V_{CC} and V_{CCO} pins be connected to the nearest place outside the package. A thick cable for V_{CC} on the printed circuit board is also recommended to reduce the V_{CC} impedance as much as possible.

The preceding discussion focused on ECL gates and the 10K/100K families of parts. The remainder of this Application Note is devoted to system design details when switching from TTL to ECL.

Effect of Rise and Fall Time

As devices operate faster and faster, rise and fall times become shorter and shorter. For TTL, the voltage swings are typically 2 to 3 volts, while ECL voltage swings are 750 to 1000 millivolts. These TTL swings are harder to deal with than the ECL swings, in which rise and fall times are only a few nanoseconds. Crosstalk current I which flows between signal paths through a coupling capacitor C is proportional to dV.

$$I = CdV/dt$$

I = cross talk current
C = coupling capacitor
dt = given rise/fall time
dV = logic swing

For a given set of rise and fall times, the crosstalk for TTL is more than for ECL because dV for TTL is greater.

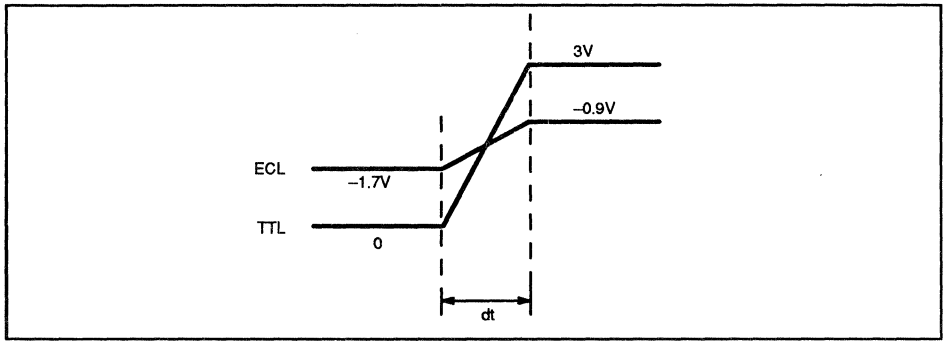


Figure 4. Voltage Swings for ECL and TTL Signals

Another problem is that at very high speeds it becomes difficult for circuit designers to develop satisfactory output buffers to drive realistic signal line impedances with full TTL voltage swings (Reference 1).

Terminating Techniques for the ECL Devices

Any signal path on a circuit board may be considered as a form of transmission line. If the line propagation delay is short with respect to the rise time of the signal, any reflections are masked out during rise time and are not seen as overshoot or ringing (Reference 2). Thus when the edge speed increases with faster forms of logic, the line lengths should be shorter in order to retain signal integrity.

When high-speed signals are transmitted over long lines, terminations should be used to minimize line distortion and reflections. These reflections cause ringing on the signal line, which, if severe, will affect system noise immunity. The reflections appear as undershoot and overshoot, as shown in Figure 5.

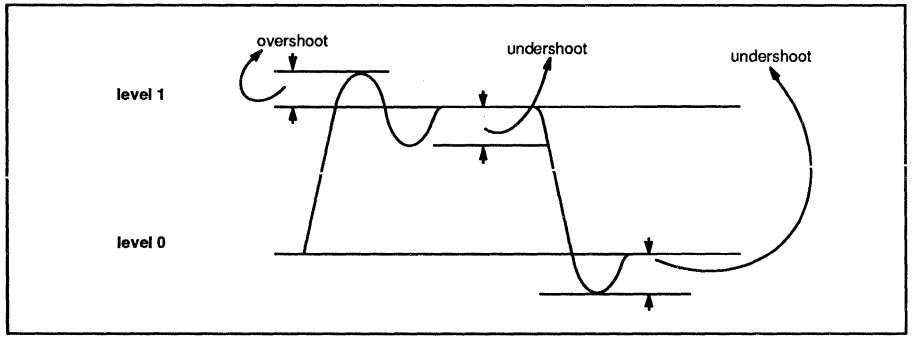


Figure 5. Definition of Overshoot and Undershoot

For best system performance the designer should consider using termination resistors when the two-way propagation time of the line is greater than the rise time of the signal on the line.

In ECL systems, every output must be terminated in the characteristic impedance of the signal interconnection which is being driven. However, these terminations depend on the physical parameters of the circuit boards. Realistic values are 50 to 75 ohms for multilayer etched boards, 100 ohms for Multi-

wire® boards, and 100 to 120 ohms for wirewrap boards (Reference 1). Standard, prepackaged termination resistors are available with values of 50 ohms, 68 ohms, 75 ohms, and 100 ohms.

There are two principal methods of termination: parallel termination and series termination. These two methods are required for impedance matching and damping, respectively.

Parallel Termination

Parallel termination lines are used for the fastest circuit performance. There are two methods of parallel termination. In the first method, the termination resistor can be connected to a termination supply voltage V_{TT} of –2.0 V as shown in Figure 6. The value of the termination resistor Rp should match the transmission line impedance Zo. If there is an appreciable mismatch, line reflections will be present with an increase in both noise and propagation delay. In parallel terminated lines, the line termination supplies the output pulldown. Consequently, no pulldown resistor is required at the output of the driving gate.

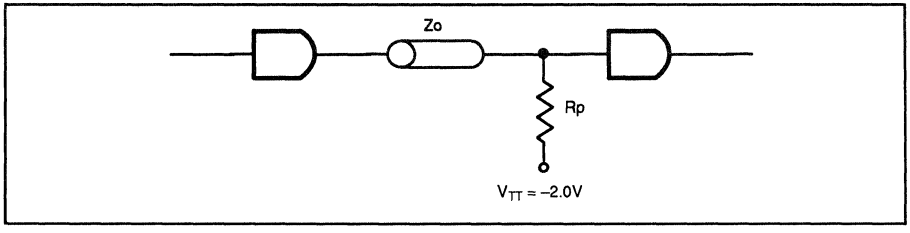


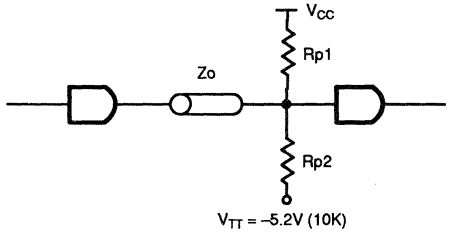
Figure 6. Parallel Termination Using Separate Termination Voltage Plane V_{TT}.

However, equivalent Zo may decrease when the loads are distributed over the transmission line. Therefore, the designer should consider each case separately. The recommended value of Rp is 50, 75, 100 or 150 ohms depending on the estimated value of Zo.* For large systems where total power is a consideration, the lines are normally terminated with a –2.0 V DC supply. When power consumption is a major concern, this is the most efficient manner of terminating ECL circuits. The drawback, of course, is the requirement of an additional power supply voltage.

7

*The values of Zo can be calculated for various transmission lines as shown in Chapter 3 of Reference 2.

In the second method, a pair of resistors is connected in series between ground (V_{CC}) and V_{EE}, providing a Thevenin's equivalent resistance and voltage. In this case $V_{TT} = V_{EE} = -5.2$ V (10K) as shown in Figure 7.



Zo (Ω)	Rp1 (Ω)	Rp2 (Ω)
50	81	130
70	113	182
75	121	195
80	130	208
90	146	234
100	162	260
120	194	312
150	243	390

Figure 7. Parallel Termination Using Thevenin's Equivalent

Rp1 and Rp2 are selected so that they satisfy the following equation:

$$1/Zo = 1/Rp1 + 1/Rp2$$

then:

$$Rp1 = 1.625$$

$$Rp2 = 2.6\ Zo$$

for

$$V_{TT} = -5.2\ V\ (10K)$$

In contrast to the first method, this technique requires about 11 times more power per termination (because the drop across the termination resistance is not as large) and uses twice as many components per termination. The advantage, however, is the non-requirement of a special power supply or a separate voltage plane per circuit board.

Series Termination

Overshoot and ringing on longer lines may be controlled by using series damping or series terminating techniques. Series damping is accomplished by inserting a small resistor Rs in series with the output of the gate as shown in Figure 8. In this case, the value of Rp is such that it can drive 5 to 15 mA of current. As for V_{TT}, –2.0 V is not compulsory, hence –5.2 V(10K) can be used. It is mandatory that Rs be equal to Zo. Signal transmitted from (A) is reflected at (B). But due to the presence of Rs (Rs=Zo), this signal is not seen at (B). The advantage of this method is that the power does not increase as much as in the parallel termination method even when multiple lines are connected to (A).

(**Note:** This advantage is not effective if the load is distributed on the signal lines.)

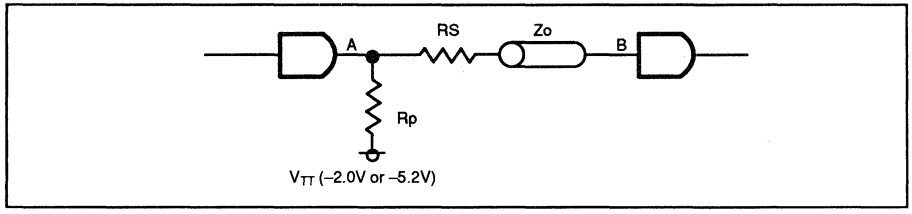


Figure 8. Series Termination

For efficient ECL system design, it is important to know not only the termination techniques but also power supply considerations (tolerances and decoupling), as well as board layout techniques.

Power Supply Voltage Tolerances

Power supply voltage tolerances must be equal to or better than ±5 percent for 10K ECL parts. 100K ECL parts are designed to operate over the range of –4.2 to –5.7 volts, which includes the 10K voltage range and also includes the 100K range of –4.5 volts ±7 percent.

Power Supply Decoupling

Power supply decoupling is required at the point of board entry and at every ECL device. In order to block low frequency noise from entering the board, a tantalum electrolytic capacitor of 22 µF or more is placed across the main power supply terminals. To block high frequency noise, Rf grade ceramic disk capacitors of 0.1 µF are placed across the main power pins of each device (Reference 1). It is recommended that a 0.1 µF capacitor be placed at the end of each row of packages for additional decoupling. If the ground plane is not good, then a 0.1 µF bypass capacitor should be used for every two packages.

For good design, the power supply ground line noise should be limited to less than 50 mV peak to peak. Also V_{EE} power supply voltage should be maintained with less than 10 mV difference among all logic cards to which the signals must interconnect (Reference 2).

For dealing with very high frequency noise, boards are available which have internal power supply voltage planes separated from each other by a few mils thickness of mylar, to provide a distributed capacitor for the whole board.

Circuit Boards and Layout

Standard double-sided circuit boards with good ground distribution may be used. A low impedance ground is necessary because any noise which is present on the ground lines is coupled into the signal lines. Any voltage drop across the ground impedance will increase noise response of the ECL circuits (Reference 2).

In the past, most of the ECL work has been done with multilayer, custom-designed etched PC boards. If proper care is used in designing, Multiwire boards or wirewrap boards can also be used. Several vendors offer wirewrap boards which are specifically designed for ECL work.

One thing worth mentioning about the ground and voltage planes on these boards is that to ensure clean signals, at least 50 percent or more of the board area should be occupied by ground and

For high-speed systems, signal lines should be kept as short as possible to minimize ringing and overshoot. Ringing and overshoot are due to the intrinsic inductance and capacitance of the line itself and can be reduced by shortening the lines, which minimizes propagation delays and makes critical timing parameters easier to achieve. Also because ringing on logic level 1 is critical for ECL circuits, it subtracts from noise immunity.

Fanout Limitations for ECL Outputs

An important consideration in laying out a circuit board is device fanout. Fanout is the number of inputs which can be driven by a single output. This is greater in the ECL world than in the TTL world. For gold-doped TTL, a fanout of 10 is assumed. In case of ECL, if one looks at the ratio of external output currents to input currents in ECL specifications, the fanout is about 100, so there are no fanout limitations. Although there are other disadvantages, each additional input which is connected to a given output adds more capacitance. This in turn will cause switching time delays as well as decrease in the output transmission line impedance, which causes reflections. In case of MBM10480-15, this delay is about 30 ps/1pF.

Also, input capacitance of an ECL RAM varies depending on the package type and the pin location. For the MBM10480, typical input capacitance is as follows:

	PACKAGE CENTER	PACKAGE CORNER
DIP	3.5 pF	4.8 pF
FPT	3.0 pF	3.8 pF

For other ECL RAMs, these values can be requested from Fujitsu. In addition to fanout limitations for the ECL outputs, another factor that should be considered while working with ECL devices is the voltage swings and the slew rate.

Edge Rates for the ECL Families

In ECL circuits, the output logic swing is typically 900 mV. Rise and fall times are defined as the transition time between 20 percent and 80 percent reference points as shown in Figure 9. The difference of the voltage level between the 20 percent point and the 80 percent point is about 540 mV (900 mV x 60 percent). The voltage slew rate is 0.54/tr or 0.54/tf (V/ns).

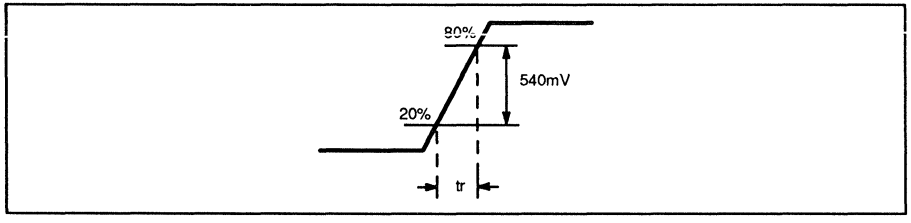


Figure 9. Rise Time

In most system designs, ECL, TTL, and CMOS devices are intermixed; thus, the designer should understand the "whats", "whys", and "hows" of interfacing these technologies.

Intermixing of 10K and 100K ECL Families

ECL is used to obtain the required circuit speed and provide the circuit features necessary to optimize high-speed system design. All ECL of the same family interface directly with each other. As mentioned previously, the power supply range of 100K ECL includes the range of 10K parts, so no basic physical problems are encountered when interfacing these two families. The real problem is when a 100K output is connected to a 10K input. At high temperatures, the V_{OH} min of 100K approaches the V_{IH} max of 10K. This results in a decrease in noise margin. However, this type of connection is allowed if the operating ambient temperature of all the ECL devices is under control. Another important fact is that when 100K is operated at –5.2 V, V_{OH} is shifted to a low level by about 30 mV. The devices can still function as indicated by the data sheet specification, although max/min limits of each parameter cannot be guaranteed.

Interfacing ECL RAMs with TTL

Circuits of the 10K ECL family normally operate with ground on V_{CC} and a –5.2 V DC power supply on V_{EE}. The negative supply operation has a noise immunity advantage and is recommended for large systems. Circuits of the 100K ECL family normally operate on V_{CC} and –4.5 V DC power applied to V_{EE}.

With the –5.2 V power supply for 10K ECL, the high logic level is about –0.96 V and the low logic level is about –1.65 V. This provides a small voltage swing of 690 mV. So for this reason, the 10K ECL and 100K ECL are not directly compatible with common slower-speed logic types such as TTL and MOS. Translators should be used when interfacing ECL with these devices.

The most common interface requirement for ECL is with TTL logic levels. This occurs when ECL system must interface with an existing TTL system or when both ECL and TTL are used in the same system design. The interface requirements between ECL and TTL depends on how the circuits are being used.

The normal ECL/TTL interface occurs when ECL is powered with a –5.2 V power supply (10K devices) or –4.5V power supply (100K devices) and TTL is powered with a +5 V power supply. The use of common ground and separate power supplies will isolate the TTL-generated noise from ECL supply lines. Translators are used at the outputs of the ECL devices to convert ECL level to TTL level.

Similarly, for interfacing TTL to ECL devices, TTL-to-ECL translators are used. These devices usually have a propagation delay in the order of 1.6 ns. The devices from Fujitsu are shown in Table 2.

Table 2. TTL to ECL Translators

PART #	INPUT	OUTPUT	t_{PD} (TYP)	NO. OF CKT PER PACKAGE	PACKAGE
MB766	ECL 10KH	TTL	5 ns at 75 pF	8	DIP-20
MB767	TTL	ECL 10KH	1.6 ns	8	DIP-20

Usually the ECL-to-TTL translators have a propagation delay which is dependent on fanout loading. Thus, if more devices are being driven, t_{PD} of these translators increases. For ECL gate arrays on which on-chip translators are used, intermixing of ECL with TTL can be easily accomplished.

Interfacing with TTL on a Common Power Supply

In many system designs, where only a small number of ECL devices are used, it is desirable to operate both ECL and TTL on a +5 V DC power supply. ECL works well in this mode (pseudo-ECL) if care is taken to isolate the TTL-generated noise from the ECL +5 V supply line. Translators for interfacing TTL and ECL in this mode are built out of discrete components because integrated circuit translators do not operate on +5 V. Typical discrete translators (ECL/TTL and TTL/ECL) are shown in Figure 10(a) and (b) (Reference 2). The ECL/TTL translator uses one PNP transistor for translation and the typical translation delay time is less than 10 ns when one high-speed TTL load is driven. The TTL/ECL translator consists of three resistors in series to attenuate TTL outputs to ECL requirements. The translation is very fast, normally under 1 ns, depending on wiring delays and stray capacitance.

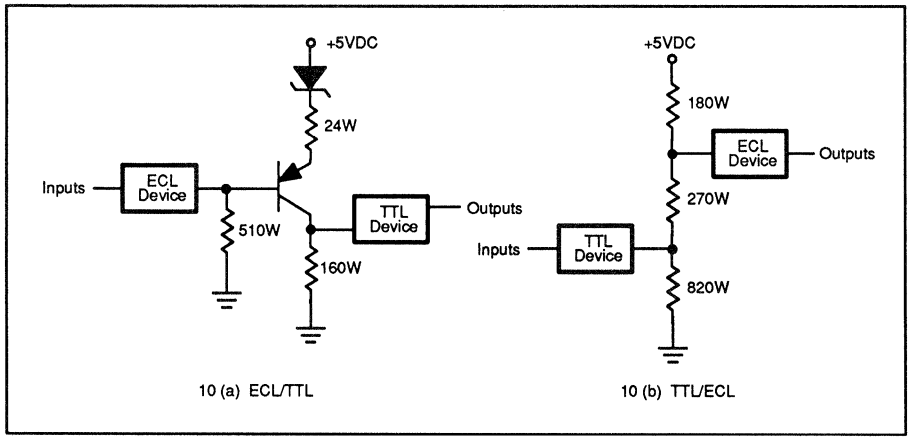


Figure 10. Discrete Translators

Interfacing ECL to CMOS

The ECL/MOS interface varies with the MOS power supply voltage. For P-channel MOS circuits operating between ground and a -VE voltage, a discretely built translator is used. Modern N-channel circuits are commonly TTL compatible, so CMOS at +5V operates with TTL logic levels. For such cases, TTL/ECL translators are used.

ECL devices offer an efficient solution to a high-performance system design compared to TTL and CMOS, with only one extra requirement: system cooling. The reason for this is that ECL devices consume more power than TTL devices. Thus, it is important for ECL system design to consider the thermal characteristics of the ECL devices and the different cooling techniques normally used.

Thermal Considerations for ECL Circuits

The electrical power dissipated in any integrated circuit forms a heat source in the package. This heat source increases the temperature of the circuit die relative to some reference point (normally 25 degrees Centigrade ambient) in an amount which depends upon the net thermal resistance between the heat source and the reference point. Thermal resistance, theta, is the difference between the temperature of the junction and the temperature of the reference point, per unit power dissipation. Thermal resistance is the primary figure of merit for power handling capability of any integrated circuit package. Thermal

resistance from "junction to case", theta JC, and/or the thermal resistance from "junction to ambient", theta JA, are the thermal parameters most often specified for integrated circuit packages. The junction temperature T_j for a given junction-to-ambient thermal resistance theta J_A, power dissipation P_D, and ambient temperature T_A, is given by :

(i) $$T_j = P_D\ \theta_{JA} + T_A$$

If a heat sink is used and it has the thermal resistance θ_{SA} (sink to ambient), the thermal resistance from junction to case, θ_{JC}, is given by :

(ii) $$T_j = P_D\ (\theta_{JA}+\theta_{CS}+\theta_{SA}) + T_A$$

where θ_{CS} = thermal resistance from integrated circuit (case) to heat sink.

The values of θ_{JC}, and θ_{JA} for Fujitsu's ECL RAMs and different ECL gate arrays are available upon request.

Thermal resistance is not usually specified for digital ICs, though maximum power dissipation is generally defined. The maximum ambient temperature rating is the usual point of interest for users of digital integrated circuits. Regardless of the ambient temperature, the system designer using ECL should be aware of the device junction temperature. The lower the junction temperature of the device, the higher the reliability and consequently the life of the device. For every 10 degree rise in junction temperature, the MTBF (Mean Time Between Failure) decreases by a factor of 2.

Cooling Techniques

ECL products dissipate a lot of heat. The power dissipated in an integrated circuit is the heat source for thermal purposes. This power dissipation is somewhere in the vicinity of 1W. This means that to have their systems stay within the operating range of 0 to 75 degrees Centigrade, designers have to pay special attention to heat dissipation.

The majority of ECL users provide some form of air flow cooling in medium and large size systems. Fujitsu specifies a constant air flow of more than 500 linear feet per minute across the package. As air passes over devices on a printed circuit board, it absorbs heat from each package. Thus, the ambient temperature of the air will increase as it flows from the inlet to the outlet. The heat gradient from the first package to the last package is a function of the package density, air flow rate, and the individual package dissipation.

The major means of heat transfer from the top of the die to the outside surface of the package is by conduction through the solids. Heat transfer through the bonding wire from die to lead frame is negligible. Once heat is transmitted to the package, transfer to ambient air depends upon the package mounting techniques and its environment. If the integrated circuit package is installed in, or attached to a heat sink, the heat transfer is mainly due by conduction to the heat sink, and then by convection and radiation from the heat sink to the ambient air. Figure 11 shows the different types of heat sinks recommended by Fujitsu. The material used is usually aluminum. The number of fins is dependent upon the theta JA of the device. If the theta JA is large then more fins are required.

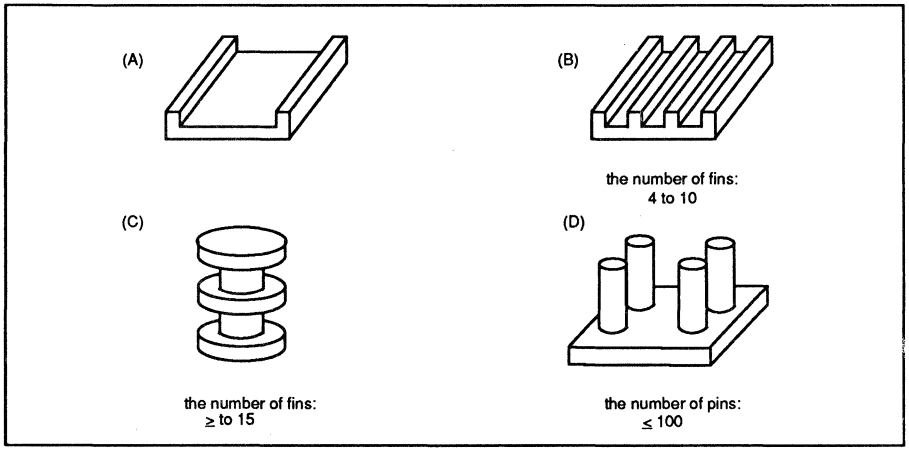


Figure 11. Recommended Heat Sinks

Besides air cooling together with heat sinks, some designers use emergent cooling techniques when the system generates a lot of heat.

Liquid Coolants

As mentioned earlier, cooling is used to prevent excessive temperatures in ECL circuits, since higher power together with reduced size often results in detrimentally high heat dissipation density.

A common technique for cooling high performance and high voltage electronic equipment uses a dielectric liquid. This method is used in many applications where forced air cooling is not adequate. The liquid cooling techniques commonly used are divided into four categories.

1. Ebullient (boiling) cooling
2. Free (natural) convection
3. Forced convection laminar flow
4. Forced convection turbulent flow

In the first two techniques, the sealed package with electronic components is immersed in fluid.

In the second two techniques, the coolant is circulated through or around the outside of the package.

The main considerations in selecting a coolant for electronic system are:

1. Properties relating to heat transfer (density, thermal conductivity, specific heat, viscosity, etc.)
2. Properties relating to handling (boiling point, freeze point, toxicity, etc.)
3. Properties relating to electrical characteristics (dielectric strength, dielectric constant, etc.)
4. Properties relating to reliability (compatibility with components, thermal stability)
5. Cost

The classes of liquids considered suitable as dielectric coolants are petroleum oil, diester synthetic oil, polyglycols, phosphate esters, chlorinated hydrocarbon, fluorocarbons (Fluorinert® liquids) and chlorofluorocarbons, silicones, and silicate esters. Most ECL designers using liquid cooling techniques use Fluorinert (Reference 3). The Fluorinert liquids provide effective heat transfer in free or forced convection. Cooling by boiling using Fluorinert liquids is even more effective. Because of their ability to remove heat so rapidly, especially in boiling, the Fluorinert liquids keep component temperatures lower and thus reduce failure rates and increase reliability. This also means that the components can be packaged closer together to maximize power densities and minimize equipment size.

Fujitsu's ECL RAM Family

Fujitsu offers an extensive line of different organizations and speeds of ECL SRAMs, in 10K, 100K, and 101K. The deepest configuration now available is the 64K x 1 at 15 ns and the fastest ECL RAM available is 5 ns at 4K and 1K depth. In addition to this, Fujitsu also offers 16-bit wide ECL RAMs which are 256 and 1024 words deep. In addition to the Buffer Address Array, the Color Display Palette and Self-Timed RAMs are offered as Application Specific memories.

ECL Gate Arrays

Fujitsu offers a wide variety of ECL gate arrays. The largest gate array available at present is over 30,000 gates (ET30000VH). This array features typical propagation delay times per gate of only 80 picoseconds unloaded and 300 picoseconds loaded (3 mm wire loaded).

Conclusion

This Application Note has covered many of the questions which may occur to a system designer planning to work with ECL system design instead of the usual TTL environment. Efficient implementation of ECL technology brings a new dimension of problem-solving ability to an already advanced field. Furthermore, a common benefit encountered by both the experienced and inexperienced designer will be a major gain in system speed over standard TTL designs.

® Multiwire is a registered trademark of Kollmorgen Company
® Fluorinert is a registered trademark of 3M Company

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